TEXAS INSTRUMENTS

High-Performance Networking Components

ATM, Ethernet™, Token Ring, SONET/SDH, and Bus Functions

Data Book

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1995

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Networking Products Group

High-Performance Networking Components Data Book

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INTRODUCTION

Texas Instruments (TI) is pleased to introduce our 1995 product families of high-performance networking products and related devices. The families of ATM, SONET/SDH, and Ethernet™ devices are named with the prefix TNET. The token-ring, bus-logic, and FIFO families keep their current naming conventions.

The 1995 networking product portfolio demonstrates robust introductions in token ring and Ethernet, as well as aggressive new product rollouts in advanced technologies such as 100Base-T, 100VG-AnyLAN, and ATM. These are complemented by highly integrated products for SONET/SDH, T3, E3 and other wide-area network interfaces. TI is investing heavily in and will continue to deliver leading technology, innovation, products, and support for the networking market.

Networking Architectures

TI has developed the following networking architectures that form the foundation for our approach to networking in the 1990s:

- ThunderLAN – A single architecture to address 10Base-T, 100Base-T, and 100VG-AnyLAN protocols. This flexible architecture addresses multiple price/ performance points with very high performance.
- ThunderCell – The ATM architecture for a family of products that addresses both local- and wide-area network solutions. ThunderCell provides conformance to standards, leadership cost/performance, and an evolutionary path from legacy LANs to ATM networks.
- TI380 Token Ring – The leading token-ring chipset family. TI will continue to invest in TI380 for PCI compatibility, integration, and enhancements to support newer-switched services.
- WAN Access – SONET/SDH, T3, and E3 devices for WAN access. As public and private networks begin to merge, the ability to connect the WAN to the LAN is becoming increasingly important. TI is committed to developing solutions to enable an easy migration from LAN to WAN and from WAN to LAN.

These architectures represent innovative solutions for network requirements today and will continue to receive aggressive investment from TI, along with major networking companies in the future. The flexibility and scalability of network functions, possible with the Thunder series, is unique in the industry.

This data book is a collection of several product lines designed for the networking environment. In addition to our ATM, SONET/SDH, Ethernet™, and token-ring products, TI has included information on FIFOs, bus interfaces, and logic products typically used in today's network systems. This makes it easier for our customers to have the necessary information to design their systems. Application notes, where appropriate, have also been included.

For more information on TI's networking products, please contact your local TI field sales office or authorized distributor.

For data sheets, application reports, board schematics, and questions and answers on TI's ATM and SONET/SDH products, you can contact the ATM Marketing Group at:

*4ATM@timsg.csc.ti.com or on the Internet at

http://www–mkt.sc.ti.com/sc/docs/schome.htm

For the latest information on TI's token-ring and Ethernet solutions, please send E-mail to:

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This support hotline can provide data sheets, application notes, schematics, and answers to product specific questions. Also, a free monthly electronic newsletter TI380 Tech Tips, is available. To subscribe, forward your E-mail address to:

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Contents

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a . . . h	=	the level of steady-state inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎴	=	one low-level pulse
Toggle	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎴, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

EXPLANATION OF FUNCTION TABLES

Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	H	H	H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	L	L	L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D, respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

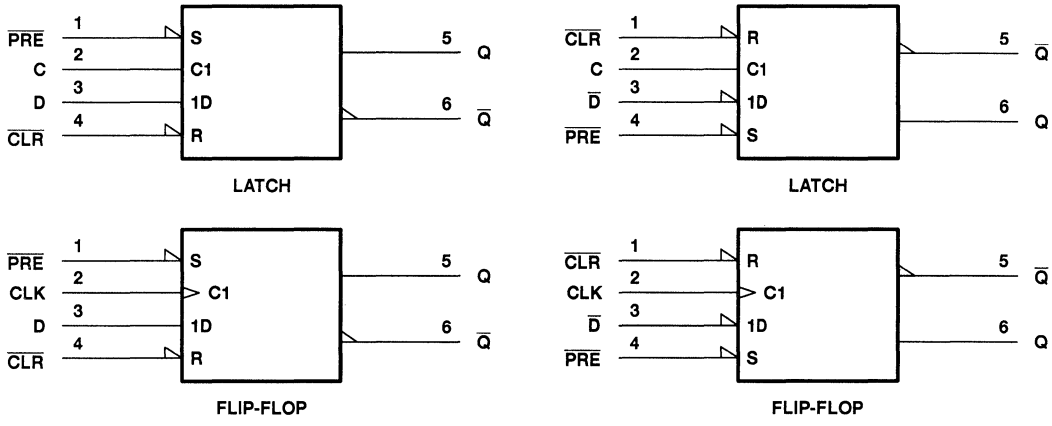
The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

The function table functional tests do not reflect all possible combinations or sequential modes.

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called preset (PRE). An input that causes a $\overline{Q}$ output to go high or a Q output to go low is called clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active low.

The devices on several data sheets are second-source designs, and the pin name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits $\overline{D}$ and Q.

In some applications, it may be advantageous to redesignate the data input from D to $\overline{D}$ or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.



The figures show that when Q and $\overline{Q}$ exchange names, the preset and clear pins also exchange names. The polarity indicators (⊾) on $\overline{PRE}$ and $\overline{CLR}$ remain, as these inputs are still active low, but the presence or absence of the polarity indicator changes at D (or $\overline{D}$), Q, and $\overline{Q}$. Pin 5 (Q or $\overline{Q}$) is still in phase with the data input (D or $\overline{D}$); their active levels change together.

In digital-system design, consideration must be given to thermal management of components. The small size of the small-outline package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures. In general, the junction temperature for any device can be calculated using using the following equation:

$$T_J = R_{\Theta JA} \times P_T + T_A$$

where:

T_J = virtual junction temperature
$R_{\theta JA}$ = thermal resistance, junction to free air
P_T = total power dissipation of the device
T_A = free-air temperature

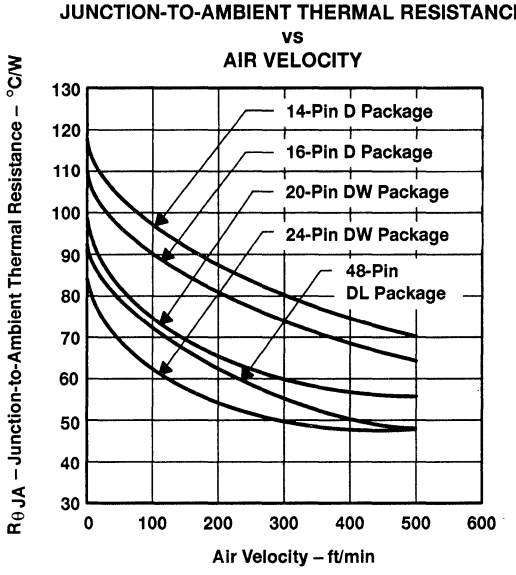


Figure 1

Derating curves for 210-mil shrink small-outline package are shown in Figures 2 through 5.

DERATING CURVES FOR 210-MIL SHRINK SMALL-OUTLINE PACKAGE (DB)

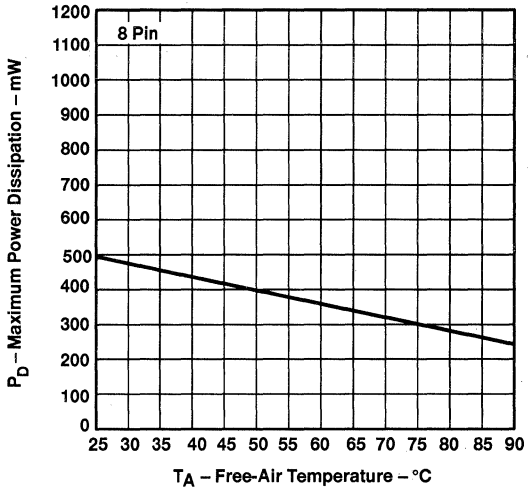


Figure 2

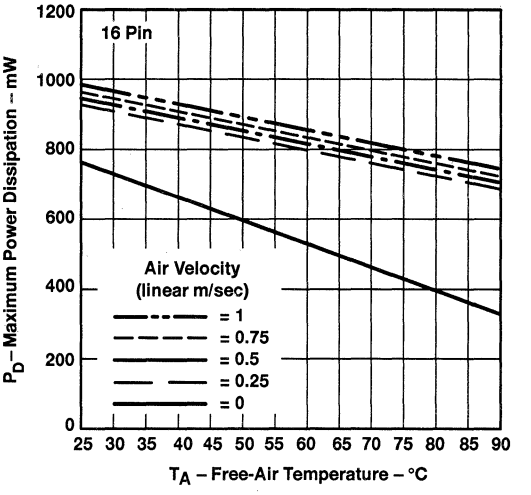


Figure 3

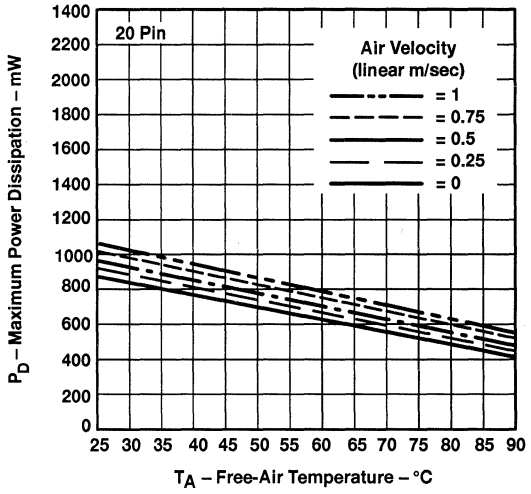


Figure 4

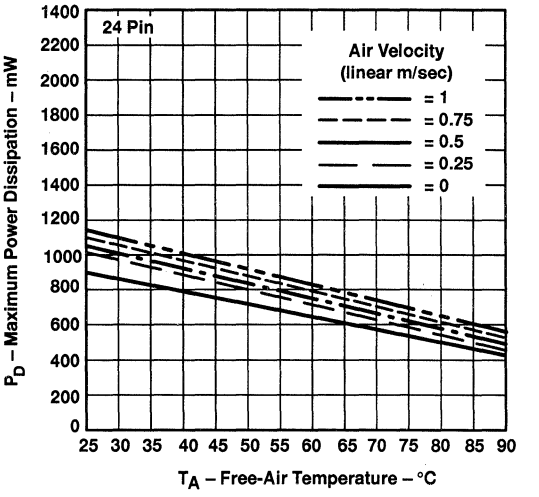


Figure 5

Contents

SDNS021B – MARCH 1994 – REVISED JANUARY 1995

- **Single-Chip Receiver/Transmitter for Transporting 53-Byte ATM Cells Via STS-3c/STM-1 Frame (155.52 Mbit/s)**
- **On-Chip Analog Phase-Locked Loop (APLL) Provides:**
  - **Recovery of Receive Clock From Incoming Serial-Data Stream**
  - **Transmit Clock Generation From External 19.44-MHz Clock Source**
- **Inserts and Extracts ATM Cells Into/From SONET/SDH STS-3c/STM-1 SPE**
- **Detects Multiple-Bit Errors and Corrects Single-Bit Errors in the 5-Byte ATM Headers of Incoming ATM Cells**
- **Generates Alarms for:**
  - **Loss of Incoming Serial Signal (LOS)**
  - **Out of Frame (OOF)**
  - **Loss of Frame (LOF)**
  - **B1-Byte Parity Error (B1ERR)**
  - **Loss of ATM Cell Alignment (LOCA)**
  - **Line Far-End Receive Failure (LFERF)**
  - **Receive Loss of Pointer (LOP)**
  - **Line Alarm Indication Signal (LAIS)**
- **Meets ATM Forum ATM User-Network Interface Specification Requirement**
- **BiCMOS Device Packaged in 144-Pin Plastic Quad Flat Package (PQFP)**

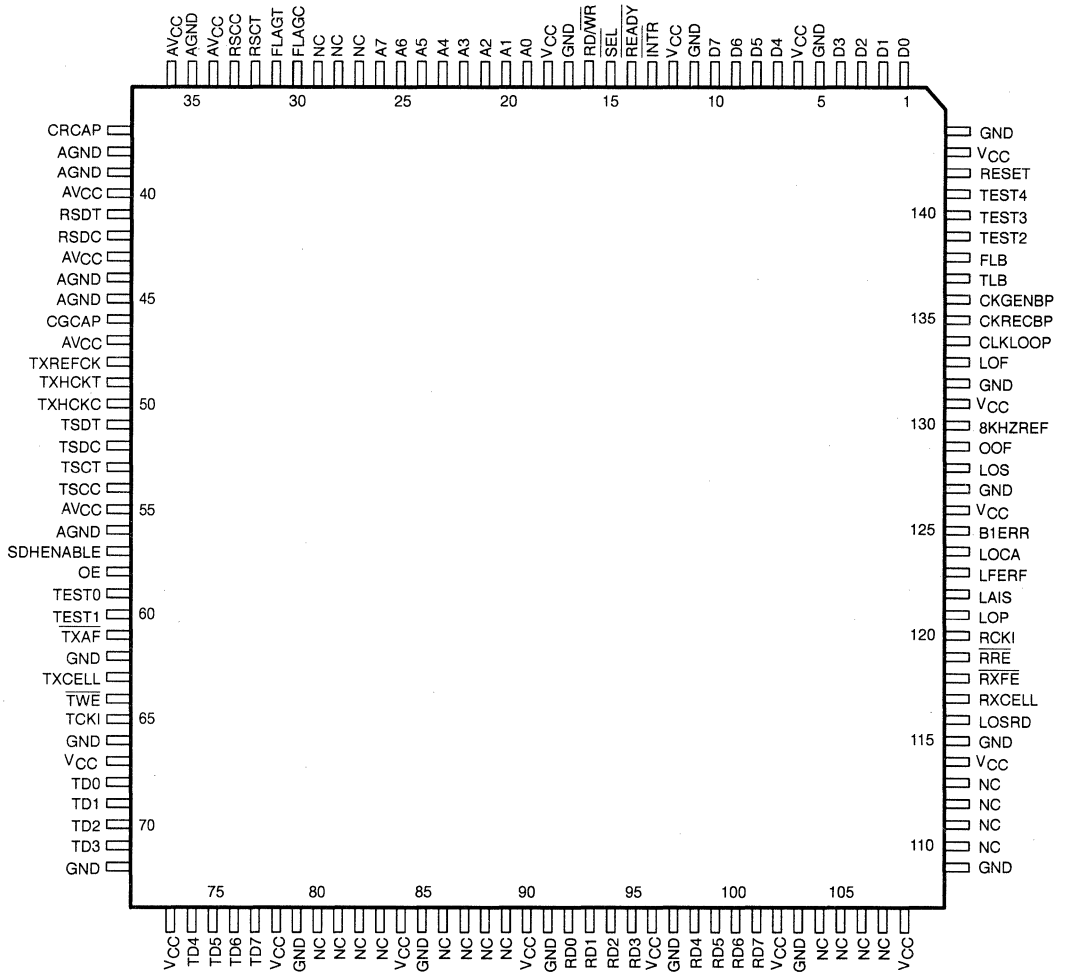
description

The synchronous optical network (SONET)/synchronous digital hierarchy (SDH) asynchronous transport mode (ATM) line-interface receiver/transmitter provides a single-chip implementation for transporting ATM cells over the SONET/SDH network at the STS-3c/STM-1 rate of 155.52 Mbit/s. This device provides all the functionality required to insert and extract 53-byte ATM cells into/from a STS-3c/STM-1 synchronous payload envelope (SPE), including clock recovery and clock generation using analog phase-locked loops (APLL).

On the receive side, the TNETA1500 accepts 155.52-Mbit/s serial data, recovers the embedded clock signal, performs SONET/SDH frame alignment and serial-to-parallel conversion, identifies the SONET/SDH payload, and establishes the ATM-cell boundaries. The ATM cells are extracted from the payload, descrambled, and passed to the receive output FIFO for output to the next device (e.g., a reassembly device). On the transmit side, complete 53-byte ATM cells are placed into the transmit input FIFO, scrambled, and inserted into an STS-3c/STM-1 SPE. The SONET/SDH frame is scrambled and converted to a serial-data stream for output. An APLL is used to generate the 155.52-MHz output clock from a low-speed 19.44-MHz oscillator, eliminating the need for a high-speed 155.52-MHz oscillator.

PRODUCT PREVIEW

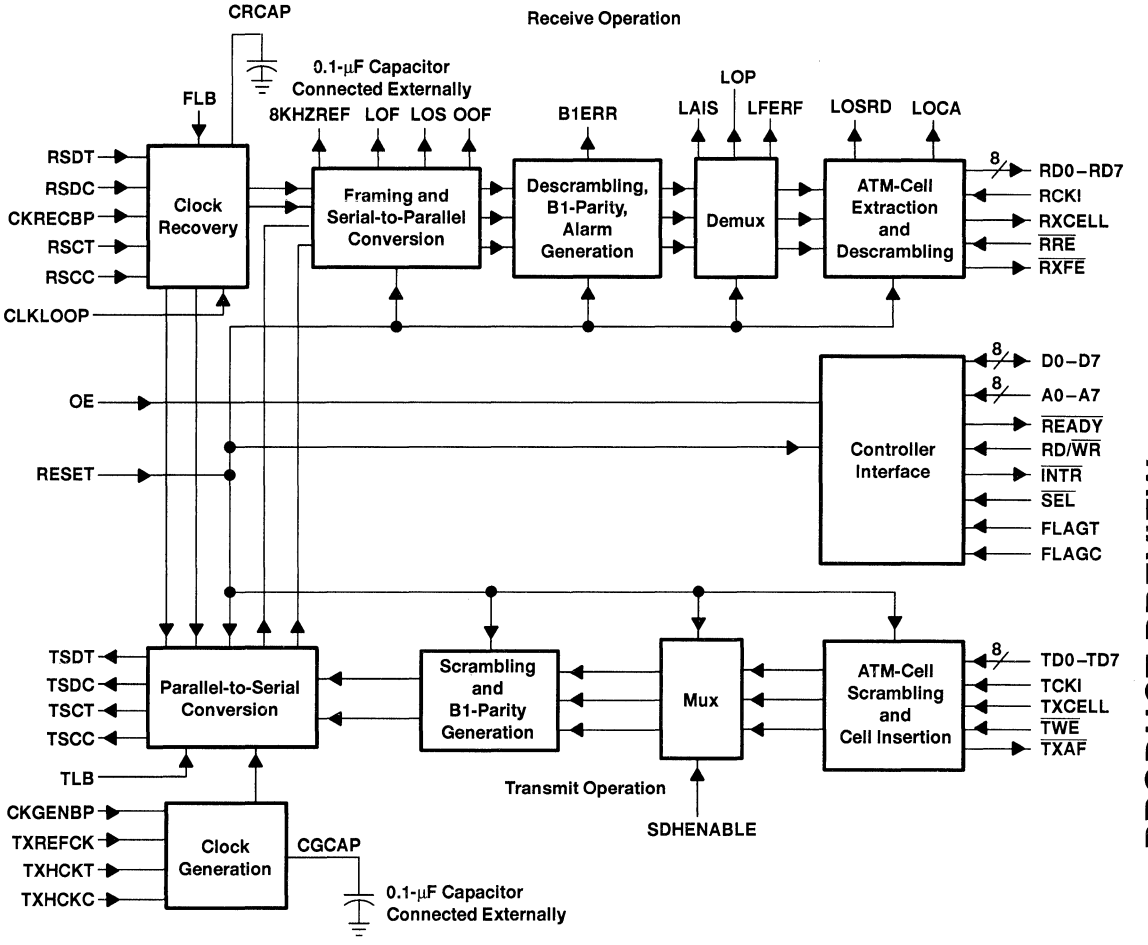
PCM PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

detailed description

transmit operation

The transmit-cell interface consists of the byte-wide input data (TD0–TD7), input clock (TCKI), start of ATM-cell input (TXCELL), transmit write-enable input ($\overline{\text{TWE}}$), and transmit-input FIFO almost-full output ($\overline{\text{TXAF}}$). Input data is clocked into the TNETA1500 on low-to-high transitions of TCKI when $\overline{\text{TWE}}$ is low. The transmit-input FIFO almost-full flag ($\overline{\text{TXAF}}$) goes active when the transmit FIFO is within five bytes of filling up (the FIFO holds three complete ATM cells).

The 48-byte information field of the ATM cell is scrambled using a self-synchronizing scrambler polynomial of $x^{43} + 1$ to improve the efficiency of the cell-delineation procedure. At startup, the scrambler is initialized to an all 1s state. The five-byte ATM header is not scrambled at this step. The TXCELL input identifies the first byte of the ATM cell and disables the scrambler. The input data is stored in the transmit-input FIFO and multiplexed into the SONET/SDH payload after all 53 bytes have been received. If the FIFO does not contain 53 bytes of information at the start of a cell-insertion cycle, an idle or unassigned cell is sent dependent on the status of the control registers. An idle cell is defined as an ATM cell with the 5-byte header set to 00 00 00 01 52 (hex) and the 48-byte payload set to 6A (hex). An unassigned cell is defined as an ATM cell with the 5-byte header set to 00 00 00 00 55 (hex) and the 48-byte payload set to 6A (hex) (see the controller interface section for more information on the operation of the control registers).

The transmit section calculates the header-error check (HEC) byte in the ATM header by default. This implies that the fifth byte of the ATM cell that is input through the transmit-cell interface is ignored. The HEC byte is calculated in accordance with the ANSI T1.624-1993 and CCITT recommendation I.432. This feature can be disabled by setting a bit in the control register.

The transmit operation can be programmed to send either a SONET STS-3c frame or a SDH STM-1 frame. When the SDHENABLE input is low, a SONET STS-3c frame is transmitted. When the SDHENABLE input is high, a STM-1 frame is transmitted. For both the STS-3c and STM-1 frames, the location of the J1 byte in the path overhead is fixed; the J1 byte always comes after the third C1 byte of the transport overhead (this is known as location 522). The data-communication channels (D1 through D12 bytes) in the transport overhead (TOH) are set to a hex value of FF 00 00. The values for the transport- and path-overhead bytes for both a STS-3c frame and a STM-1 frame are given in Table 1.

transmit operation (continued)

Table 1. Transmit Transport-Overhead and Path-Overhead Bytes

OVERHEAD BYTE		SONET FRAME VALUE WHEN SDHENABLE = LOW		SDH FRAME VALUE WHEN SDHENABLE = HIGH	
A1		1111 0110 (F6h)		1111 0110 (F6h)	
A2		0010 1000 (28h)		0010 1000 (28h)	
C1 Bytes		01 02 03 (h)		01 00 00 (h)	
B1		Calculated		Calculated	
B2					
B3					
First H1		0110 0010 (62h)		0110 1010 (6Ah)	
Second H1 (H1*)		1001 0011 (93h)		1001 1011 (9Bh)	
Third H1 (H1*)					
First H2		0000 1010 (0Ah)		0000 1010 (0Ah)	
Second H2 (H2*)		1111 1111 (FFh)		1111 1111 (FFh)	
Third H2 (H2*)					
Three H3 Bytes		0000 0000 (00h)		0000 0000 (00h)	
First K2		Normal operation: 0000 0000 Line FERF: 0000 0110		Normal operation: 0000 0000 Line FERF: 0000 0110	
Third Z2		B2 error count: 0000 0000 – 0001 1000		B2 error count: 0000 0000 – 0001 1000	
J1		0000 0000		0000 0000	
C2		0001 0011		0001 0011	
G1	Bits 1 – 4	B3 error count: 0000 – 1000	Path FERF: 1001	B3 error count: 0000 – 1000	Path FERF: 1001
	Bit 5	Path RDI: 1		Path RDI: 1	
	Bits 6 – 8	000		000	
H4		0000 0000		0000 0000	

The parity byte B1, B2 (three bytes), and B3 are calculated as follows:

B1 — B1 is a bit-interleaved parity-8 code (BIP-8) using even parity. B1 is calculated over all bits of the previous STS-3c frame after scrambling. The calculated value of B1 is placed in the STS-3c frame before the frame is scrambled.

B2 — For an STS-3c frame, the three B2 bytes combine to form a BIP-24 code; however, each B2 byte is calculated as if the frame is composed of three individual STS-1s. Each B2 is calculated over all bits of the line overhead and STS-1 envelope capacity of the previous STS-1 frame before scrambling using even parity. The computed value is placed in the appropriate B2 byte location before scrambling. The line overhead consists of the six rows of transport-overhead bytes beginning with the first H1 byte and ending before the row containing the first A1 byte (see Table 1).

B3 — For an STS-3c frame, the B3 byte is calculated over all bits of the previous STS-3c SPE before scrambling. B3 is a BIP-8 code using even parity. The computed value is placed in the B3 location prior to scrambling.

transmit operation (continued)

Prior to transmission, the STS-3c frame is scrambled using a generating polynomial of $x^7 + x^6 + 1$. The A1, A2, and C1 overhead bytes are not scrambled, and the scrambler is reset to 1111111 on the most significant bit of the byte immediately following the third C1 byte. The scrambler runs continuously throughout the complete STS-3c frame.

After the STS-3c frame has been scrambled, the bytes are converted to a serial-data stream using a parallel-to-serial converter. An APLL is used to generate the 155.52-MHz output clock from a 19.44-MHz oscillator connected to the TXREFCK input. Two other sources can be used for the 155.52-MHz clock. The CKGENBP and CLKLOOP inputs are used to select either a 155.52-MHz external clock source or the clock recovered from the incoming serial-data stream APLL (loop timing). The functions for selecting the transmit-clock source are shown in Table 2. The clock generation APLL requires that an external 0.1-µF capacitor be connected from the CGCAP terminal to ground.

Table 2. Functions for CKGENBP and CLKLOOP Inputs

CKGENBP	CLKLOOP	CLOCK SOURCE
L	L	TXREFCK (19.44 MHz)
L	H	Receive recovered clock (loop timing)
H	H or L	TXHCKT, TXHCKC (155.52 MHz)

Both true and complementary pseudo-ECL-compatible serial data and clock outputs are available. The serial data is output on the rising edge of the true clock signal (falling edge of the complement clock). The outputs are designed to drive a 50-Ω line terminated through a 50-Ω resistor to 3 V (or its equivalent).

A terminal-loopback feature is also provided on the device. When the terminal-loopback input is high, the ATM cells received on the transmit input are looped back to the receive output. The ATM cells received are blocked. The transmit operation is not affected in this mode and operates as previously described.

receive operation

The receive serial inputs to the TNETA1500 consist of 155.52-Mbit/s true and complementary PECL data and an optional 155.52-MHz true and complementary pseudo-ECL clock. The 155.52-MHz clock inputs are needed only if the clock-recovery-bypass input (CKRECBP) is high, which disables the clock-recovery circuit. This feature is used typically for test purposes and is not normally used in a system application.

The clock-recovery circuit is used to recover the embedded clock signal from the serial nonreturn-to-zero (NRZ) data inputs RSDT and RSDC. The clock-recovery circuit consists of a transition detector, an analog phase-locked loop (APLL), and a retiming circuit. The transition detector is used to double the frequency of the incoming serial-data stream. This is necessary because the NRZ-data stream does not contain a second harmonic, which is necessary to recover the transmit clock. The APLL consists of a phase-frequency detector, a charge pump/loop filter, and an internal voltage-controlled oscillator (VCO). The phase-frequency detector compares the output of the transition detector to the output of the VCO and generates a signal to the charge pump/loop filter that is used to change the frequency of the VCO. The frequency of the VCO is adjusted until it matches the frequency of the transition detector. When this occurs, the APLL is locked to the frequency of the embedded-input clock signal.

The clock-recovery circuit also contains a circuit that retimes the input serial data to the recovered output clock. The only external component required for the clock-recovery circuit is a 0.1-µF capacitor that is connected from the CRCAP terminal to ground. This capacitor is part of the charge-pump/loop-filter circuit.

receive operation (continued)

The clock signal recovered from the incoming serial-data stream can also be used as the transmit clock for the transmit section. This is known as clock looping. The advantage of using the recovered receive clock as the transmit clock is that the transmit clock is frequency locked to the same clock source that is used to generate the incoming data stream. If this clock source provides a highly accurate low-PPM (low parts per million) clock, the transmit clock is also a very accurate clock. The drawback to using clock looping is that if the receive signal is lost for any reason, the transmit clock is also lost.

A facility-loopback (FLB) input loops the input data and recovered clock to the transmit output data and clock. This provides a method of testing the function of the clock-recovery circuit and its jitter performance. It can also be used for system-loopback testing.

The PECL inputs FLAGT and FLAGC are provided for interfacing to the loss-of-optical-signal outputs on optical receivers. If the optical signal is lost, the loss-of-optical-carrier bit in the interrupt register is set and the interrupt output ($\overline{\text{INTR}}$) becomes active low.

The recovered clock signal and retimed input data are passed from the clock-recovery circuit to the framing circuit. The framing circuit searches for the SONET framing bytes A1 and A2 where A1 has a set value of F6h and A2 has a value of 28h. The exact framing pattern for a STS-3c frame is A1A1A1A2A2A2 (F6F6F6282828h). These bytes are not scrambled by the transmitter.

The TNETA1500 provides loss-of-signal (LOS), out-of-frame (OOF), and loss-of-frame (LOF) alarms in accordance with BellCore specification TR-NWT-000253, Issue 2, December 1991. The LOS alarm goes active when no transitions are detected on the receive serial data for 3.3 µs. The LOS alarm goes inactive when two consecutive framing patterns have been detected, and during the intervening time (one frame time), no transitionless 3.3-µs period is detected. The OOF alarm goes active when four consecutive-errored framing patterns are received. The OOF alarm clears when two successive error-free framing patterns are received. If the out-of-frame condition fails to clear within 3 ms, the LOF alarm goes active. The LOF alarm goes inactive when eight consecutive error-free SONET frames are identified. The LOS, OOF, and LOF alarms are indicated by external signals and by setting a bit in the interrupt registers. This causes the $\overline{\text{INTR}}$ output of the controller interface to go active low signaling an interrupt.

After the SONET frame is established and the serial data converted to byte-wide data, the B1 BIP-8 parity is calculated over the scrambled SONET frame. This value is compared with the value of B1 contained in the next (n + 1) frame. The value of B1 calculated over the previous frame (n – 1) is compared to the value B1 in this frame (frame n). If the two values do not match, the B1ERR output goes active, denoting that a B1 parity error has occurred. In addition, the B1 parity-error bit in the interrupt register is set and $\overline{\text{INTR}}$ goes active low.

Next, the SONET frame is unscrambled (except for the A1, A2, and C1 bytes, which were not scrambled by the transmitter). The B2 BIP-24 value is calculated over all the bits of the line overhead and the STS-3c envelope capacity and compared to the value contained in the next frame. If a B2 parity error occurs, the B2 parity-error bit in the interrupt register is set and the interrupt line ($\overline{\text{INTR}}$) goes active low to notify the controller that a parity error has occurred.

The TNETA1500 monitors the receive K2 byte for line alarm-indication signal (LAIS) and line far-end receive failure (LFERF) alarms. A LAIS alarm occurs when bits 6 – 8 of the receive K2 byte are set to a value of 111 for five consecutive frames. The LAIS alarm goes inactive when bits 6 – 8 of the receive K2 byte are set to a value of 000 for five consecutive frames. The LFERF alarm goes active when bits 6 – 8 of the receive K2 byte are set to a value of 110 for five consecutive frames. The LFERF alarm goes inactive when bits 6 – 8 of the receive K2 byte are set to a value of 000 for five consecutive frames. Both the LAIS and LFERF alarms are indicated on an external terminal and by setting a bit in interrupt register 2.

receive operation (continued)

The location of the J1 byte in the SPE is determined from the H1 and H2 bytes in the transport overhead. The location of the J1 byte does not change from the previous frame unless the first four bits of H1 are set to 1001 (the new data flag) or the pointer value contained in H1 and H2 is different for three consecutive frames. The location of J1 can also be incremented or decremented one-byte position by inverting certain bits in the H1 and H2 byte pointer. If bits 7, 9, 11, 13, and 15 are inverted, the location of J1 is incremented one time slot. If bits 8, 10, 12, 14, and 16 are inverted, the location of J1 is decremented one time slot. Subsequent pointers contain the new offset.

The TNETA1500 provides a loss-of-pointer (LOP) alarm to indicate that either an invalid pointer was detected in the incoming H1 and H2 bytes or a new data flag NDF (set to a value of 1001 — the first four bits of H1) was found in eight consecutive frames. The LOP alarm goes inactive when a valid pointer with the NDF set to 0110 is detected in three consecutive frames. The device also provides a path-AIS alarm to indicate that a path-AIS condition has been detected in the H1 and H2 bytes. A path-AIS condition is detected as an all 1s condition in bytes H1 and H2 for three consecutive frames. The path-AIS alarm goes inactive when a valid pointer, with the NDF set to 0110 is detected for three consecutive frames. The LOP alarm is not set if a path-AIS condition is detected. The LOP alarm is indicated by an external signal and by the interrupt register. The path-AIS alarm is indicated only by the interrupt register.

The B3 BIP-8 byte is calculated over the contents of the STS-3c SPE, which begins with the J1 byte. The value calculated for B3 is compared with the value found in the next frame. If a B3 parity error occurs, the B3 parity-error bit is set in the interrupt register and $\overline{\text{INTR}}$ goes active low to notify the controller.

The TNETA1500 monitors the receive G1 byte for a path far-end receive failure (path FERF) and path remote defect indication (path RDI) alarms. A path FERF occurs when bits 1 – 4 of the G1 byte are set to a value of 1001. The path FERF alarm goes inactive when bits 1 – 4 of the G1 byte are set to a non-1001 value. A path RAI occurs when bit 5 of the G1 byte is set to a value of 1 for 10 consecutive frames. The path RDI alarm goes inactive when bit 5 of the G1 byte is set to a value of 0 for 10 consecutive frames. Both the path FERF and path RDI alarms are indicated through interrupt register 3.

Once the STS-3c SPE is located, the ATM cells are identified and extracted. Cell delineation is accomplished by computing the header-error check (HEC) for the first four bytes after the J1 byte and comparing the calculated value with the fifth byte. If the values do not match, the process advances one byte and then repeats. This process continues until a match between the calculated value and the fifth byte occurs. Cell alignment is assumed to have occurred when seven consecutive matches occur. Until cell alignment occurs, the loss-of-cell-alignment alarm (LOCA) remains active. Once cell alignment is established, it is monitored constantly for a loss-of-cell-alignment condition. A loss-of-cell-alignment condition is declared (LOCA goes active) when seven consecutive cells occur with header errors. At this point, the hunting process starts over.

The receive side detects multiple-bit errors and corrects single-bit errors occurring in the 5-byte ATM header of incoming ATM cells by using the HEC byte. This feature is deactivated by setting a bit in control register 1 (see Table 6). The ATM cells with multiple-bit header errors are dropped, unless a bit is set in control register 1 (see Table 6) to disable the dropping of cells with uncorrectable errors. An 8-bit saturating counter (accessible through the controller interface) counts the number of ATM cells with multiple-bit ATM header errors.

After the ATM cells are extracted, they are descrambled. The 48-byte payload in the ATM cell is scrambled at the transmitter using a $x^{43} + 1$ polynomial to further distinguish the payload from the header bytes and improve the efficiency of the cell-delineation algorithm. The $x^{43} + 1$ polynomial is also used to descramble the payload so that it can be sent to the next device.

The TNETA1500 has the capability of dropping idle and unassigned cells from the receive data stream. An idle cell is defined as a cell with a 5-byte ATM header set to a value of 00 00 00 01 52 (hex) and an unassigned cell is defined as a cell with a 5-byte header of 00 00 00 00 55 (hex). In both cases, the payload is ignored. The dropping of idle and/or unassigned cells can be disabled through control register 1 (CR1) in the controller interface.

receive operation (continued)

After descrambling, the ATM cell is passed to the output buffer, which operates as a FIFO. The receive-cell interface consists of the output data (RD0–RD7), receive-clock input (RCKI), receive-read-enable input ($\overline{RRE}$), receive-FIFO-empty output ($\overline{RXFE}$), beginning-of-ATM-cell indicator (RXCELL), and loss-of-receive-data alarm (LOSRD). Data is sent out from the device on the rising edge of RCKI when $\overline{RRE}$ is low. The LOSRD alarm goes active when the output FIFO overflows. In this case, the last cell placed into the FIFO is overwritten. The output FIFO holds three complete ATM cells.

Cumulative counts of receive B1, B2, and B3 errors are provided by registers accessible through the controller interface. These registers maintain running totals of B1, B2, and B3 block errors and coding violations. The block-error counters maintain a count of the number of frames that are received with B1, B2, and B3 errors. The coding-violation counters count the exact number of B1, B2, and B3 bit-interleaved parity (BIP) errors that occur. It is possible for a single frame to contain 8 B1, 24 B2, and 8 B3 BIP errors. When any of the block-error or coding-violation counters reach maximum count, a bit is set in the interrupt registers and an interrupt is generated. These counters are rollover counters that roll over to zero after the maximum count occurs and an interrupt is generated (see the controller-interface section for additional information).

When the receive side enters a loss-of-cell alignment (LOCA) state, a path remote-defect indication (path RDI) may need to be sent out the transmit side through the outgoing G1 byte. A path-RDI alarm is declared when a LOCA state is persistent for an amount of time (also known as soak time) that has not yet been specified by any industry standards. To provide maximum flexibility with regard to this unspecified soak time, an 8-bit counter is provided through the controller interface that allows the user to program the amount of soak time for a path-RDI alarm in increments of 125 µs. This counter is preset (when a device reset occurs) to a value of 4 ms, which is the anticipated soak time for a path-RDI alarm.

controller-interface operation

The controller interface provides access to the internal memory locations that contain the control registers, interrupt registers, interrupt-mask registers, and the ID register. Table 3 shows a memory map of the locations of the various registers in the TNETA1500.

Table 3. TNETA1500 Register Memory Map

ADDRESS (HEX VALUE)	REGISTER	ADDRESS (HEX VALUE)	REGISTER
00	Interrupt register 1	0D	B1 block error counter
01	Interrupt register 2	0E	Not implemented
02	Interrupt register 3	0F	B2 block error counter
03	ID register	10	Not implemented
04	Not implemented	11	B3 block error counter
05	Control register 1	12	B1 coding-violation counter (LSB)
06	Control register 2	13	B1 coding-violation counter (MSB)
07	Interrupt-mask register 1	14	B2 coding-violation counter (LSB)
08	Interrupt-mask register 2	15	B2 coding-violation counter
09	Interrupt-mask register 3	16	B2 coding-violation counter (MSB)
0A	Multierrored cell counter	17	B3 coding-violation counter (LSB)
0B	Path-RDI soak counter	18	B3 coding-violation counter (MSB)
0C	Not implemented	>18	Not implemented

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interrupt registers

The interrupt registers located at hex addresses 00, 01, and 02 contain information on the condition of the receive data stream that causes the interrupt flag ($\overline{INTR}$) to become active low. The coding for the interrupt registers is given in Table 4.

Table 4. Interrupt-Register Coding

CAUSE OF INTERRUPT	IR1 CODING (ADDRESS 00)	IR2 CODING (ADDRESS 01)	IR3 CODING (ADDRESS 02)
B1 parity error	XXXX XXX1	—	—
B2 parity error	XXXX XX1X	—	—
B3 parity error	XXXX X1XX	—	—
Loss-of-cell alignment	XXXX 1XXX	—	—
Loss-of-incoming signal	XXX1 XXXX	—	—
Out of frame	XX1X XXXX	—	—
Loss of frame	X1XX XXXX	—	—
Loss-of-optical carrier	1XXX XXXX	—	—
Line AIS	—	XXXX XXX1	—
Line FERF	—	XXXX XX1X	—
Loss-of-receive data	—	XXXX X1XX	—
Loss of pointer	—	XXXX 1XXX	—
Path AIS	—	XXX1 XXXX	—
B1 block error overflow	—	XX1X XXXX	—
B2 block error overflow	—	X1XX XXXX	—
B3 block error overflow	—	1XXX XXXX	—
B1 CV overflow	—	—	XXXX XXX1
B2 CV overflow	—	—	XXXX XX1X
B3 CV overflow	—	—	XXXX X1XX
Path RDI	—	—	XXXX 1XXX
Path FERF	—	—	XXX1 XXXX

The alarm conditions or errors set bits in the interrupt register that cause the open-drain ouput $\overline{INTR}$ to go active low. All of these conditional actions are associated with the receive data stream and are described below.

LOS, OOF, LOF, LAIS, LOP, LFERF, LOCA, LOSRD

These alarm conditions cause an external signal to go active and set a bit in one of the interrupt registers (see terminal functions table for description of the individual alarms). The status of the bit in the interrupt register for these alarms mirrors the status of the external signal. For example, as long as a loss-of-frame condition exists, both the LOF output and the loss-of-frame bit in IR1 (the value for LOF is x1xx xxxx) are set. When the logic in the TNETA1500 detects that the LOF condition has cleared, the external output and the status bit in the interrupt registers are cleared. A change in the status bit in the interrupt registers for these alarms cause the $\overline{INTR}$ output to go active low. When the status bit makes a low-to-high transition, the $\overline{INTR}$ output goes active low. The $\overline{INTR}$ output also goes active low when the status bit makes a high-to-low transition. Reading the interrupt register does not clear the status bit for these particular alarms. However, the $\overline{INTR}$ output goes inactive high on a read of any of the interrupt registers.

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loss-of-optical carrier, path AIS, path RDI

These alarm conditions cause a status bit in one of the interrupt registers to go active. As long as the alarm condition exists, the status bit remains set. When the logic in the TNETA1500 detects that the alarm condition has cleared, the status bit is cleared. A change in the status bit in the interrupt registers for these alarms causes the $\overline{\text{INTR}}$ output to go active low. When the status bit makes a low-to-high transition, the $\overline{\text{INTR}}$ output goes active low. The $\overline{\text{INTR}}$ output also goes active low when the status bit makes a high-to-low transition. Reading the interrupt register does not clear the status bit for these particular alarms. However, the $\overline{\text{INTR}}$ output goes inactive high on a read of any of the interrupt registers.

B1/B2/B3 parity error, B1/B2/B3 block error overflow, B1/B2/B3 CV overflow

The status bits for these errors indicate that the specified error condition has occurred. The status bits in the interrupt registers for these conditions are set when the error conditions occur and remain set until the interrupt register is read. If a B1, B2, or B3 parity error is detected on an incoming frame, the corresponding status bit is set in the interrupt register, the $\overline{\text{INTR}}$ output goes active low, and the status bit remains set until a read of any interrupt register occurs. Once a read of any interrupt register occurs, the status bit for one of these error conditions is cleared until the next time that this error condition is detected.

interrupt-mask registers

All of the interrupts in the three interrupt registers can be masked by setting bits in the corresponding interrupt-mask registers. The coding for the interrupt-mask registers is the same as the coding for the interrupt registers. To mask only the interrupt associated with a B2 parity error, a value of 0000 0010 is written to the interrupt mask register 1 (IMR1). To mask all the interrupts in interrupt register 1, a value of 1111 1111 is written to the interrupt mask register 1. After reset, all three interrupt-mask registers are cleared (set to 00 hex). Table 5 shows the coding for the interrupt-mask registers.

Table 5. Interrupt-Mask-Register Coding

INTERRUPT TO BE MASKED	IMR1 CODING (ADDRESS 07)	IMR2 CODING (ADDRESS 08)	IMR3 CODING (ADDRESS 09)
B1 parity error	XXXX XXX1	—	—
B2 parity error	XXXX XX1X	—	—
B3 parity error	XXXX X1XX	—	—
Loss-of-cell alignment (LOCA)	XXXX 1XXX	—	—
Loss-of-incoming signal (LOS)	XXX1 XXXX	—	—
Out of frame (OOF)	XX1X XXXX	—	—
Loss of frame (LOF)	X1XX XXXX	—	—
Loss-of-optical carrier	1XXX XXXX	—	—
Line AIS	—	XXXX XXX1	—
Line FERF	—	XXXX XX1X	—
Loss-of-receive data	—	XXXX X1XX	—
Loss of pointer	—	XXXX 1XXX	—
Path AIS	—	XXX1 XXXX	—
B1 block error overflow	—	XX1X XXXX	—
B2 block error overflow	—	X1XX XXXX	—
B3 block error overflow	—	1XXX XXXX	—
B1 CV overflow	—	—	XXXX XXX1
B2 CV overflow	—	—	XXXX XX1X
B3 CV overflow	—	—	XXXX X1XX
Path RDI	—	—	XXXX 1XXX
Path FERF	—	—	XXX1 XXXX

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control registers

The control registers are located at addresses 05 and 06 (hex). The control registers provide a means of controlling the operation of the device through the controller interface. A reset operation, initiated either by taking the RESET signal high or by performing a write operation to the ID register, clears both control registers. The bit definition for the two control registers is shown in Table 6.

Table 6. Coding for Control Registers

ACTION	CONTROL REGISTER 1 (ADDRESS 05)	CONTROL REGISTER 2 (ADDRESS 06)
Disable error correction for receive ATM cell headers	XXXX XXX1	—
Disable transmit ATM-cell header HEC-byte generation	XXXX XX1X	—
Enable terminal loopback (TLB)	XXXX X1XX	—
Enable facility (serial) loopback (FLB)	XXXX 1XXX	—
Disable the dropping of ATM cells with multiple-bit header errors	XXX1 XXXX	—
Disable the dropping of ATM idle cells from the receive data stream	XX1X XXXX	—
Disable the dropping of ATM unassigned cells from the receive data stream	X1XX XXXX	—
Transmit STM-1 frame	1XXX XXXX	—
Enable receive clock looping	—	XXXX XXX1
Transmit ATM unassigned cells as filler	—	XXXX XX1X

Descriptions of the various control functions of the control registers are given below:

disable error correction for receive ATM cell headers

When set to a high level, this bit causes the error-detection and correction block to stop correcting single-bit errors that are detected in the headers of incoming ATM cells. When a reset operation is performed, this bit is cleared (set to 0). The normal operating state of the TNETA1500 provides single-bit error correction on the headers of incoming ATM cells, and an action must be taken to disable this operation.

disable transmit ATM-cell header HEC-byte generation

When set to a high level, this bit causes the transmit section to stop generating the header error check (HEC) byte in the five-byte header of ATM cells that are being transmitted. When a reset operation occurs, this bit is cleared (set to 0). The normal operating mode of the TNETA1500 calculates the HEC byte from the first four bytes of the ATM cell that is transmitted and inserts the calculated value in the HEC byte location. This bit is used to disable the generation of the HEC byte.

enable terminal loopback (TLB)

When set to a high level, this bit causes the ATM-cells input (through the transmit-cell interface) to loop through the device and be sent out through the receive-cell interface. The receive serial-data stream is blocked when this mode of operation is chosen. However, the transmit section operates normally and the device continues to transmit ATM cells that are inserted in a STS-3c/STM-1 frame. Internally, this bit is logically ORed with the TLB input, which allows a terminal loopback to be enabled through either the external input or through the control register. When a reset operation occurs, the bit in the control register is cleared.

enable facility (serial) loopback (FLB)

When set to a high level, this bit causes the receive serial data and clock inputs to loop through the device and be sent out through the transmit serial data and clock outputs. The transmit serial data stream is blocked when this mode of operation is chosen. However, the receive section operates normally, and the device continues to extract ATM cells from the incoming STS-3c/STM-1 frame. Internally, this bit is logically ORed with the FLB input, which allows a facility loopback to be enabled through either the external input terminal or through the control register. When a reset operation occurs, the bit in the control register is cleared.

disable the dropping of ATM cells with multiple-bit header errors

When set to a high level, this bit causes the receive section to stop dropping ATM cells that contain multiple-bit header errors. When a reset operation occurs, this bit is cleared. The normal operation of the TNETA1500 drops ATM cells that contain multiple-bit header errors by not placing them into the receive output FIFO.

disable the dropping of ATM idle cells from the receive data stream

When this bit is set, the receive section does not drop ATM idle cells from the receive data stream. An idle cell is defined as an ATM cell with the 5-byte header set to a value of 00 00 00 01 52 (hex). When a reset operation occurs, this bit is cleared. The normal operation of the TNETA1500 is to drop idle cells from the receive data stream.

disable the dropping of ATM unassigned cells from the receive data stream

When this bit is set, the receive section does not drop ATM unassigned cells from the receive data stream. An unassigned cell is defined as an ATM cell with the 5-byte header set to a value of 00 00 00 00 55 (hex). When a reset operation occurs, this bit is cleared. The normal operation of the TNETA1500 is to drop unassigned cells from the receive data stream.

transmit STM-1 frame

When this bit is set, the transmit section transmits an STM-1 frame instead of a STS-3c frame. Internally, this bit is logically ORed with SDHENABLE, which allows this mode of operation to be enabled either through the control register or the external input. When a reset operation occurs, this bit is cleared and causes the TNETA1500 to transmit a STS-3c frame.

enable receive clock looping

When this bit is set, the receive clock is used as the clock for the transmit side (clock looping). The receive clock is either the receive serial clock or the clock recovered from the receive serial-data stream depending upon the state of the CLKRECBP input. Internally, this bit is logically ORed with CLKLOOP, which allows the clock-loop function to be enabled either through the control register or the external input. When a reset operation occurs, this bit is cleared, which disables the clock loop.

transmit ATM unassigned cells as filler

When this bit is set, the transmit side sends ATM unassigned cells for cell rate decoupling when a user data cell is not available in the transmit FIFO. An unassigned cell is defined as a cell with the 5-byte header set to a value of 00 00 00 00 55 (hex). The payload is set to 6A (hex). When this bit is not set, the device sends idle cells as filler cells for cell rate decoupling. An idle cell is defined as a cell with the 5-byte header set to a value of 00 00 00 01 52 (hex) and the payload set to 6A (hex). When a reset operation occurs, this bit is cleared.

ID register

The ID register is located at address 03 (hex). This register identifies the device revision and also provides a means of performing a software reset. The contents of this register are hardwired to a hexadecimal value of Ax (x denotes the chip revision). A software reset on the TNETA1500 is initiated by writing to the ID register through the controller interface. Since the contents of the ID register are firmware, the write does not change the contents of the register. The software reset function is logically ORed with RESET. A reset of the TNETA1500 device is initiated through either the external input or the ID register.

multierrored cell header counter

The multierrored cell header counter is a saturating 8-bit counter that counts the number of ATM cells that are received with multiple-bit errors in the 5-byte ATM header. This counter resets to zero when the register is read. This counter does not cause the $\overline{\text{INTR}}$ output to go active low when the counter reaches maximum count. This counter is set to zero when a reset operation occurs.

path RDI soak counter

This counter provides a count of the amount of time, in increments of 125 µs, that a loss-of-cell-alignment (LOCA) condition must be present before a path RDI condition is sent via the outgoing G1 byte. The amount of time required is not currently specified by any industry standard. This counter is preset to a value of four milliseconds when a reset operation occurs. The counter value is modified by writing a new value to the counter through the controller interface. For instance, to set the value in the counter to one millisecond, a value of eight (8×125 µs = 1 ms) is written in the counter. However, the value in the counter is rewritten if a reset operation occurs because the counter is reset to four milliseconds.

B1/B2/B3 block error counters

These counters maintain the total number of frames received with B1, B2, and B3 errors. These counters track the number of frames with errors, not the number of actual B1, B2, and B3 bits in error. All three counters are 8-bit counters. These 8-bit counters are read only and a reset operation clears all three counters. When these counters reach their maximum count, the $\overline{\text{INTR}}$ goes active low and a bit is set high in the interrupt register IR2. The host system reads the IR2 register to determine the cause of the interrupt. The host reads the counters to reset them to zero, and finally, the host system reads IR2 again to clear the $\overline{\text{INTR}}$ line.

B1/B2/B3 coding violation counters

These counters maintain the total number of receive B1, B2, and B3 bit-interleaved parity (BIP) bits that are in error. The B1 and B3 counters are 16-bit counters, and the B2 counter is a 19-bit counter. When one of the counters reaches its maximum count, the $\overline{\text{INTR}}$ output goes active low and a bit in the interrupt register is set. The counters automatically reset to zero when they reach their maximum count. To clear the interrupt condition, the host system has to read the LSB counter first and then read the MSB counter. After the host reads both counters in this sequence, both LSB and MSB counters are reset and the interrupt condition goes inactive. A reset operation clears all three counters. Since these counters are read only, a value cannot be written to any of the three counters.

Terminal Functions

high-speed serial interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
FLAGC, FLAGT	30, 31	I (PECL)	Loss-of-optical-carrier alarm (true and complement). This differential input is connected to a fiber-optic receiver loss-of-optical-carrier output to provide an interrupt through the controller interface when the incoming optical signal is lost.
RSCT, RSCC	32, 33	I (PECL)	Receive serial clock (true and complement). This differential input is used to clock in serial data on RSDT/RSDC when the clock-recovery phase-lock loop is bypassed by taking CKRECBP high.
RSDT, RSDC	41, 42	I (PECL)	Receive serial data (true and complement). RSDT and RSDC are differential PECL inputs.
TSCT, TSCC	53, 54	O (PECL)	Transmit serial clock (true and complement). This differential output provides the transmit serial output clock. This clock is derived from either the receive serial clock, the output of the clock generation phase-lock loop, or the transmit high-speed clock depending upon the state of CKGENBP and CLKLOOP.
TSDT, TSDC	51, 52	O (PECL)	Transmit serial data (true and complement). The differential serial data is output on the transition of TSCT/TSCC.
TXHCKT, TXHCKC	49, 50	I (PECL)	Transmit high-speed clock (true and complement). This 155.52-MHz input provides the transmit serial clock when CKGENBP is high.

alarm indicators

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
B1ERR	125	O	B1 error. A high on B1ERR indicates that a B1 parity-byte error is detected on the incoming frame.
LAIS	122	O	Line alarm-indication signal. A high on LAIS indicates that bits 6–8 of the receive K2 byte are set to 111 for five consecutive frames. The alarm clears when the pattern 000 is detected in bits 6–8 of the receive K2 byte for five consecutive frames.
LFERF	123	O	Line far-end receive failure. A high on LFERF indicates that bits 6–8 of the receive K2 bytes were set to 110 for five consecutive frames. The alarm clears when the pattern 000 is detected in bits 6–8 of the receive K2 byte for five consecutive frames.
LOCA	124	O	Loss-of-cell alignment. A high on LOCA indicates that ATM cells could not be found in the incoming data stream. LOCA goes inactive when the cell-delineation algorithm finds seven consecutive ATM cells and goes active when no valid ATM cells are found in seven consecutive cell slots.
LOF	133	O	Loss of frame. LOF goes active when the framing circuit is unable to find two consecutive SONET frames for 3 ms. The alarm is cleared when eight consecutive error-free SONET frames are identified.
LOP	121	O	Loss-of-incoming pointer. LOP goes active to indicate that an invalid pointer was found in the H1, H2 pointer bytes of the incoming frame. LOP also goes active when a new data flag (NDF) is detected for eight consecutive frames. The LOP alarm deactivates when a valid pointer with a normal NDF is detected in three consecutive frames.
LOS	128	O	Loss of signal. LOS goes active when no signal transitions are detected on the incoming serial signal for 3.3 μs. The alarm is cleared when two consecutive valid SONET framing patterns are detected, and no transitionless 3.3-μs period is detected.
OOF	129	O	Out of frame. OOF goes active when four consecutive errored SONET frames are received. The alarm clears when two consecutive error-free SONET frames are identified.
LOSRD	116	O	Loss-of-receive data. LOSRD goes active when the receive output FIFO overflows. The receive output FIFO can store a maximum of three complete ATM cells. If a cell is not sent to the next device before a fourth cell arrives, the newest cell is discarded to make room in the FIFO for the next arriving cell.

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Terminal Functions (Continued)

control signals

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CKGENBP	136	I (TTL)	Clock generation phase-locked loop bypass. When CKGENBP is high, the clock-generation PLL is bypassed and the high-speed clock input (TXHCKT/TXHCKC) is used for the transmit clock. When CKGENBP is low, the 19.44-MHz TXREFCK is used to generate the transmit clock.
CKRECBP	135	I (TTL)	Clock recovery phase-locked loop bypass. When CKRECBP is high, the clock-recovery PLL is bypassed. RSCT/RSCC is used to clock RSDT/RSDC into the device.
CLKLOOP	134	I (TTL)	Receive clock loop. When CLKLOOP is high and CKGENBP is low, the receive serial clock is looped to the transmit side and used for the transmit-serial clock. The received clock is either the clock recovered from the incoming data stream or RSCT/RSCC as determined by the state of CKRECBP.
FLB	138	I (TTL)	Facility loopback. When FLB is high, the receive serial data and clock is looped to the transmit-serial clock and data output. The receive-serial clock is either the clock recovered from the incoming data stream or RSCT/RSCC as determined by the state of CKRECBP.
OE	58	I (TTL)	Output enable. When OE is low, all outputs on the TNETA1500, except for the high-speed PECL outputs, are placed in the high-impedance state. This feature facilitates board-level testing. OE contains an internal pullup resistor so that it can be left open for normal operation.
RESET	142	I (TTL)	Device reset. When RESET goes high, the device is reset. Reset causes the receive side to restart the frame-search algorithm and forces OOF, LOF, and LOCA high. RESET also flushes any ATM cells stored in the input and output FIFOs and causes the transmit side to begin building SONET frames from the A1 byte.
SDHENABLE	57	I (TTL)	SDH enable. When SDHENABLE is high, the frame transmitted by the TNETA1500 has the 3 C1 bytes set to the sequence 01 00 00 (hex). In addition, the 3 H1 bytes in the transmit frame set to the values 6A, 9B, 9B (hex). When SDHENABLE is low, the transmit C1 bytes are set to the sequence 01 02 03 (hex) and the H1 bytes are set to the values 62, 93, 93 (hex). These conditions are necessary to comprehend the differences between a SONET STS-3c frame and a SDH STM-1 frame. SDHENABLE has an internal pulldown resistor so that it can be left open for SONET operation.
TLB	137	I (TTL)	Terminal loopback. When TLB is taken high, the data received at the transmit-cell interface is looped through the device and out the receive-cell interface. Data appearing at the receive serial data input is blocked in this mode.
TXREFCK	48	I (TTL)	Transmit reference clock. TXREFCK is used to provide a 19.44-MHz reference clock to the clock-generation phase-locked loop when CKGENBP and CLKLOOP are low. The clock-generation PLL multiplies this clock by eight to generate the 155.52-MHz transmit-serial clock.

Terminal Functions (Continued)

receive-cell interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
RCKI	120	I (TTL)	Receive clock input. Output signals are clocked out of the receive-cell interface on positive transitions of RCKI when $\overline{\text{RRE}}$ is low.
RD0–RD07	92–95 98–101	O	Receive byte data. The ATM cells are clocked out of the TNETA1500 through RD0–RD7 one byte at a time on positive transitions of RCKI, which begins with the first byte of the ATM-cell header.
$\overline{\text{RRE}}$	119	I (TTL)	Receive read enable. A low level on $\overline{\text{RRE}}$ enables the reading of data from the receive-cell interface.
RXCELL	117	O	Receive ATM-cell indicator. RXCELL goes high to identify the first byte (start) of an ATM cell. RXCELL is low during the remainder of the output.
$\overline{\text{RXFE}}$	118	O	Receive FIFO empty. $\overline{\text{RXFE}}$ goes low to denote that the receive FIFO is empty and that the current output byte is not a valid byte. $\overline{\text{RXFE}}$ goes high when a complete ATM cell is available for output.

transmit-cell interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TCKI	65	I (TTL)	Transmit clock input. Input signals are clocked into the transmit-cell interface and output signals are clocked out of the transmit-cell interface on positive transitions of TCKI when $\overline{\text{TWE}}$ is low.
TD0–TD7	68–71 74–77	I (TTL)	Transmit byte data. The ATM cells are clocked into the transmit-cell interface one byte at a time on positive transitions of TCKI when $\overline{\text{TWE}}$ is low.
$\overline{\text{TWE}}$	64	I (TTL)	Transmit write enable. A low level on $\overline{\text{TWE}}$ enables the writing of ATM cells into the transmit-cell interface.
$\overline{\text{TXAF}}$	61	O	Transmit FIFO almost full. $\overline{\text{TXAF}}$ goes low when the transmit cell input FIFO can store only five additional input bytes. $\overline{\text{TXAF}}$ goes high when storage is available in the FIFO to store a complete 53-byte ATM cell.
TXCELL	63	I (TTL)	Transmit start-of-cell indicator. A high level on TXCELL identifies the first byte of an incoming ATM cell. TXCELL should be low during the remainder of the cell input.

Terminal Functions (Continued)

controller interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
A0–A7	19–26	I (TTL)	Address lines. A0–A7 provide the address for accessing the internal registers. A7 is the most significant bit.
D0–D7	1–4 7–10	I/O	Data I/O. D0–D7 provide access to the contents of the device's internal registers. D7 is the most significant bit.
$\overline{\text{INTR}}$	13	O	Interrupt (open drain). $\overline{\text{INTR}}$ goes low to indicate that a nonmasked interrupt has occurred.
RD/$\overline{\text{WR}}$	16	I (TTL)	Read/write control. A high-level input on RD/$\overline{\text{WR}}$ indicates a read operation and a low-level input indicates a write operation.
$\overline{\text{READY}}$	14	O	Ready. $\overline{\text{READY}}$ goes low to indicate that the device is ready to complete the requested transaction.
$\overline{\text{SEL}}$	15	I (TTL)	Device select. A low-level input on $\overline{\text{SEL}}$ enables the access of the device's internal registers.

miscellaneous signals

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CGCAP	46		Clock-generation loop-filter external capacitor connection. A 0.1-μF capacitor is connected from CGCAP to ground.
CRCAP	37		Clock-recovery loop-filter external capacitor connection. A 0.1-μF capacitor is connected from CRCAP to ground.
AGND	35,38,39,44,45,56		Analog ground. AGND is the 0-V reference connection for analog phase-lock loops.
AV_{CC}	34,36,40,43,47,55		Analog supply voltage. AV_{CC} is the 5 V ± 5% connection for analog phase-lock loops.
NC	27–29,80–83, 86–89,104–107, 110–113		No connection. These terminals are left open.
GND	5,11,17,62,66,72,79, 85,91,97, 103,109,115, 127,132,144		Ground. GND is the 0-V reference for digital logic.
V_{CC}	6,12,18,67, 73,78,84,90,96, 102,108,114,126, 131,143		Supply voltage. V_{CC} is the 5 V ± 5% supply for digital logic.
TEST0–TEST3	59,60,139,140	I	Manufacturing test. TEST0–TEST3 are connected to V_{CC} for normal operation.
TEST4	141	I	Test. TEST4 is tied low for normal operation.
8KHZREF	130	O	8KHZREF produces a pulse that is synchronized to the receive-side framing bytes. 8KHZREF serves as an indication that a frame is being received. When frames are continuously received, 8KHZREF acts like an 8-kHz clock.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, TTL, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Supply voltage range, PECL, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Supply voltage range, analog, AV_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range: TTL ..... −1.2 V to 7 V
PECL ..... 0 V to PV_{CC}
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage	TTL	4.75	5.25	V
		PECL	4.75	5.25	
AV_{CC}	Supply voltage, analog		4.75	5.25	V
V_{IH}	High-level input voltage	TTL	2		V
		PECL (see Note 2)	$V_{CC}-1.1$	$V_{CC}-0.8$	
V_{IL}	Low-level input voltage	TTL		0.8	V
		PECL (see Note 2)	$V_{CC}-1.9$	$V_{CC}-1.5$	
T_A	Operating free-air temperature		0	70	°C

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage		V_{CC} = 4.75 V,	I_{IK} = −18 mA			−1.2	V
V_{OH}	High-level output voltage	TTL	V_{CC} = 4.75 V,	I_{OH} = −4 mA	4.25			V
		PECL	PV_{CC} = 5 V,	I_{OH} = −22.4 mA	4		4.3	
V_{OL}	Low-level output voltage	TTL	V_{CC} = 4.75 V,	I_{OL} = 4 mA			0.5	V
		PECL	PV_{CC} = 5 V,	I_{OL} = 7.6 mA	3		3.4	
I_I	Input current	TTL	V_{CC} = 5.25 V,	$V_I = V_{CC}$ or GND			±300	µA
I_{IH}	High-level input current	All other PECL inputs	V_{CC} = 5.25 V,	V_I = 4.45 V			25	µA
		FLAGT, FLAGC PECL inputs					250	
I_{IL}	Low-level input current	All other PECL inputs	V_{CC} = 5.25 V,	V_I = 3.35 V			±25	µA
		FLAGT, FLAGC PECL inputs					±250	
I_{CC1}	Supply current§		V_{CC} = 5.25 V, f = 155.52 Mbit/s	I_O = 0,		175		mA
I_{CC2}	Supply current¶		V_{CC} = 5.25 V,	f = 155.52 Mbit/s		230		mA
C_i	Input capacitance	TTL				4		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ PECL outputs are unterminated.
¶ PECL outputs are terminated with a 50-Ω resistor to 3 V.

PRODUCT PREVIEW

timing requirements (see Figure 1)

NO.			MIN	MAX	UNIT
1	$t_{w(SELL)}$	Pulse duration, $\overline{SEL}$ low	35		ns
2	$t_{su(RD/WR)}$	Setup time, RD/$\overline{WR}$ high before $\overline{SEL}$ ↓	3		ns
3	$t_{su(A0-A7)}$	Setup time, A0–A7 valid before $\overline{SEL}$ ↓	3		ns
4	$t_{h(A0-A7)}$	Hold time, A0–A7 valid after $\overline{SEL}$ ↑	0		ns

switching characteristics (see Figure 1)

NO.			MIN	MAX	UNIT
5	$t_{d(SL-DV)}$	Delay time from $\overline{SEL}$ ↓ to D0–D7 valid	7	25	ns
6	$t_{d(SH-DX)}$	Delay time from $\overline{SEL}$ ↑ to D0–D7 invalid	5	18	ns
7	$t_{d(SL-RL)}$	Delay time from $\overline{SEL}$ ↓ to $\overline{READY}$ ↓	7	26	ns
8	$t_{d(SH-RH)}$	Delay time from $\overline{SEL}$ ↑ to $\overline{READY}$ ↑	3	15	ns

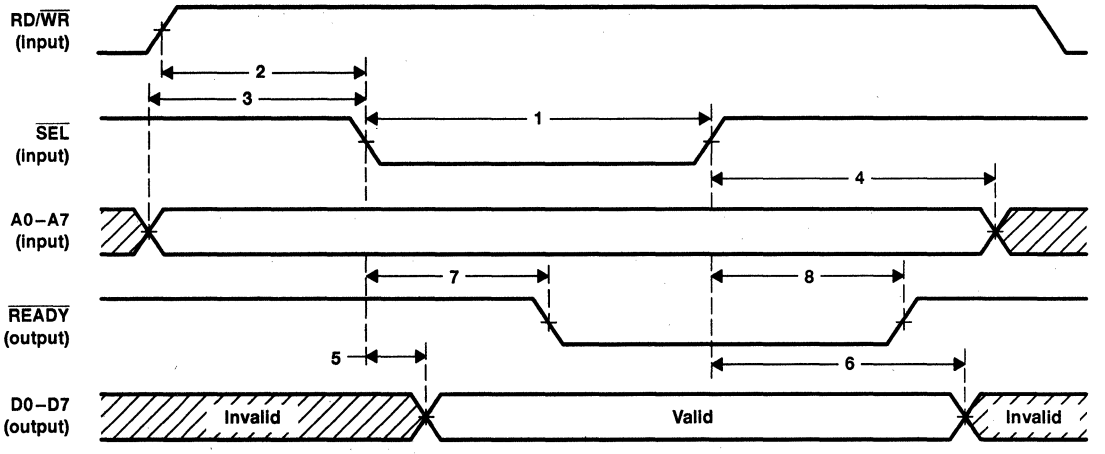

Figure 1. Controller-Interface Read Cycle

PRODUCT PREVIEW

timing requirements (see Figure 2)

NO.			MIN	MAX	UNIT
1	$t_{w(SELL)}$	Pulse duration, $\overline{SEL}$ low	35		ns
2	$t_{su(RD/WR)}$	Setup time, RD/$\overline{WR}$ low before $\overline{SEL}$ ↓	3		ns
3	$t_{su(A0-A7)}$	Setup time, A0–A7 valid before $\overline{SEL}$ ↓	3		ns
4	$t_{su(D0-D7)}$	Setup time, D0–D7 valid before $\overline{SEL}$ ↑	3		ns
5	$t_{h(D0-D7)}$	Hold time, D0–D7 valid after $\overline{SEL}$ ↑	2		ns

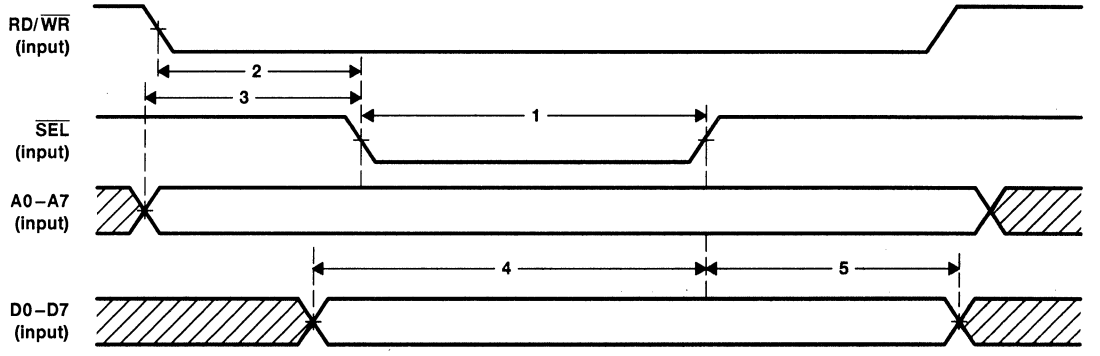

Figure 2. Controller-Interface Write Cycle

PRODUCT PREVIEW

timing requirements (see Note 3 and Figure 3)

NO.			MIN	MAX	UNIT
1	$t_{w(RCKIH)}$	Pulse duration, RCKI high	10		ns
2	$t_{w(RCKIL)}$	Pulse duration, RCKI low	10		ns
3	$t_{su(RRE)}$	Setup time, $\overline{RRE}$ high before RCKI ↑	8		ns
4	$t_{h(RRE)}$	Hold time, $\overline{RRE}$ high after RCKI ↑	0		ns

NOTE 3: All output signals are generated on the rising edge of RCKI. All input signals are sampled on the rising edge of RCKI.

switching characteristics (see Note 3 and Figure 3)

NO.			MIN	MAX	UNIT
5	$t_{d(RCH-RXCH)}$	Delay time from RCKI ↑ to RXCELL ↑	8	18	ns
6	$t_{d(RCH-RDV)}$	Delay time from RCKI ↑ to RD0–RD7 valid	8	16	ns
7	$t_{d(RCH-RXFH)}$	Delay time from RCKI ↑ to $\overline{RXFE}$ ↑	5	12	ns
8†	$t_{d(RCH-RXFL)}$	Delay time from RCKI ↑ to $\overline{RXFE}$ ↓	5	11	ns

† $\overline{RXFE}$ goes active low when no complete cell is available in the receive cell FIFO. When a complete cell is available, $\overline{RXFE}$ is deactivated. The pulse duration of this signal depends on the pulse duration of the RCKI clock and on the cell availability of the FIFO. The minimum pulse duration is equal to the RCKI width. The maximum width is dependent on the RCKI clock pulse duration and cell availability.

NOTE 3. All output signals are generated on the rising edge of RCKI. All input signals are sampled on the rising edge of RCKI.

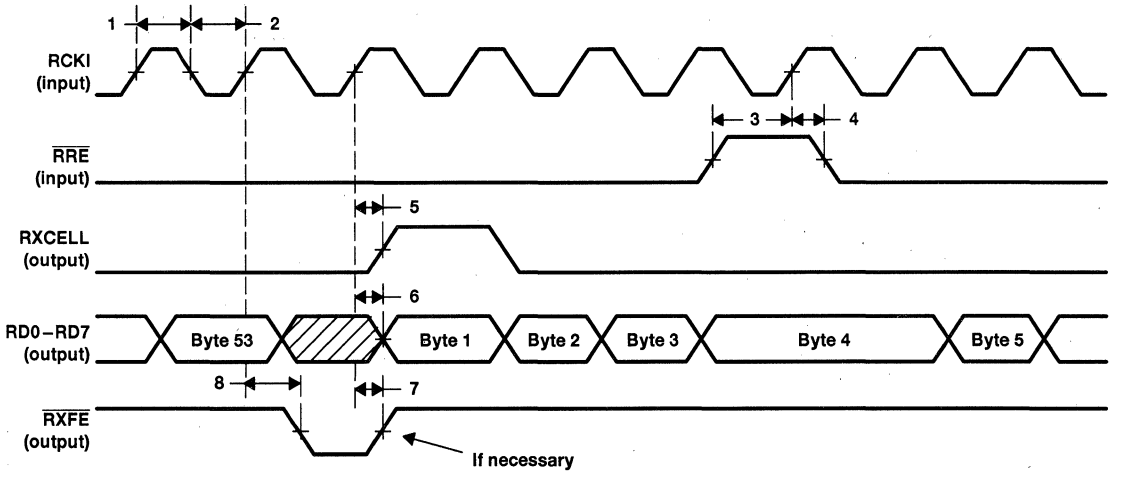

Figure 3. Receive-Cell Interface

PRODUCT PREVIEW

timing requirements (see Note 4 and Figure 4)

NO.			MIN	MAX	UNIT
1	$t_{w(TCKIH)}$	Pulse duration, TCKI high	10		ns
2	$t_{w(TCKIL)}$	Pulse duration, TCKI low	10		ns
3	$t_{su(TWE)}$	Setup time, $\overline{TWE}$ high before TCKI ↑	12		ns
4	$t_{h(TWE)}$	Hold time, $\overline{TWE}$ high after TCKI ↑	0		ns
5	$t_{su(TXCELL)}$	Setup time, TXCELL high before TCKI ↑	12		ns
6	$t_{su(TD0-TD7)}$	Setup time, TD0–TD7 valid before TCKi ↑	12		ns
7	$t_{h(TXCELL)}$	Hold time, TXCELL high after TCKI ↑	0		ns
8	$t_{h(TD0-TD7)}$	Hold time, TD0–TD7 valid after TCKI ↑	0		ns

NOTE 4: All output signals are generated on the rising edge of TCKI. All input signals are sampled on the rising edge of TCKI.

switching characteristics (see Note 4 and Figure 4)

NO.			MIN	MAX	UNIT
9	$t_{d(TCH-TXAL)}$	Delay time from TCKI ↑ to $\overline{TXAF}$ ↓	5	12	ns

NOTE 4: All output signals are generated on the rising edge of TCKI. All input signals are sampled on the rising edge of TCKI.

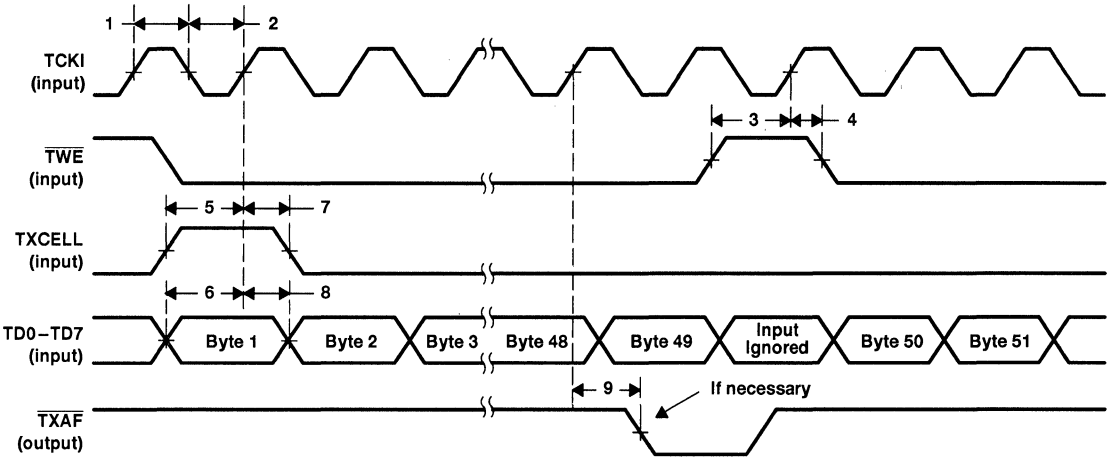

Figure 4. Transmit-Cell Interface

timing requirements (see Figure 5)

NO.			MIN	MAX	UNIT
1	$t_{w(8KHREL)}$	Pulse duration, 8KHZREF low			ns

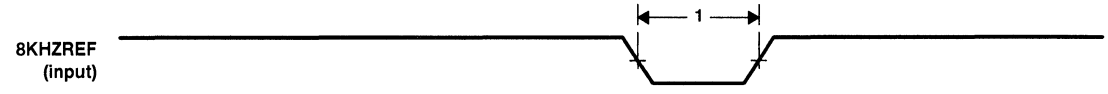

Figure 5. 8-kHz Reference Signal

PRODUCT PREVIEW

APPLICATION INFORMATION

introduction

The TNETA1500 SONET/SDH ATM BiCMOS receiver/transmitter is designed to insert/extract ATM cells into/from a 155.52-Mbit/s STS-3c/STM-1 frame. The device contains two analog phase-locked loops (APLL) and the digital logic necessary to process the incoming frame and build the output frame. The two APLLs are used to:

- Recover a 155.52-MHz receive clock from the incoming serial-data stream
- Generate a 155.52-MHz transmit clock from an external 19.44-MHz signal

The device is fabricated from a 0.8-micron BiCMOS process. The BiCMOS process provides the capability of designing true differential PECL (ECL referenced to 5 V instead of ground) serial inputs and outputs. The advantages of providing true PECL inputs and outputs are:

- The device interfaces directly to fiber-optic receivers and transmitters and UTP-5 transceivers without external buffering.
- The device outputs can directly drive a 50-Ω line terminated with 50 Ω to 3 V or the Thevenin equivalent (121 Ω to ground and 82 Ω to V_{CC}). This eliminates transmission-line reflections and improves performance.
- The differential PECL inputs provide a high common-mode noise-rejection ratio (CMRR), which improves noise immunity of the device.
- The reduced output voltage swing of the differential PECL outputs (approximately 800 mV) reduces the internal noise generated when the high-speed serial outputs switch. This is especially important since the outputs are switching at 155.52 Mbit/s.

Internally, the two analog PLLs are isolated from each other and the digital logic blocks (see Figure 6). Each analog PLL has its own V_{CC} and ground connections that are not connected internally to the V_{CC} and ground connections of the other blocks. From a power and ground connection viewpoint, this forms three blocks: the digital logic block, the analog clock-recovery block, and the analog clock-generation block.

general layout considerations for the TNETA1500

The major considerations in laying out a board for the TNETA1500 are:

- Decouple the analog supply (AV_{CC} terminals) from the digital supply (V_{CC} terminals) using an inductor or ferrite bead. This can be accomplished by one of two methods:
  - Connect the AV_{CC} terminals for the clock-recovery block together and use an inductor/ferrite bead to connect them to the digital plane. Then, connect the AV_{CC} terminals for the clock-generation block together and use a second inductor/ferrite bead to connect these pins to the digital-supply plane.
  - Connect each AVCC terminal to the digital-supply plane using an inductor or ferrite bead and a 0.1-μF bypass capacitor.
- Use low-inductance bypass capacitors, such as 0.1-μF surface-mount devices, to reduce V_{CC} noise due to output switching. The recommended bypassing is one bypass capacitor for each AV_{CC} terminal and one bypass capacitor for each two V_{CC} terminals.

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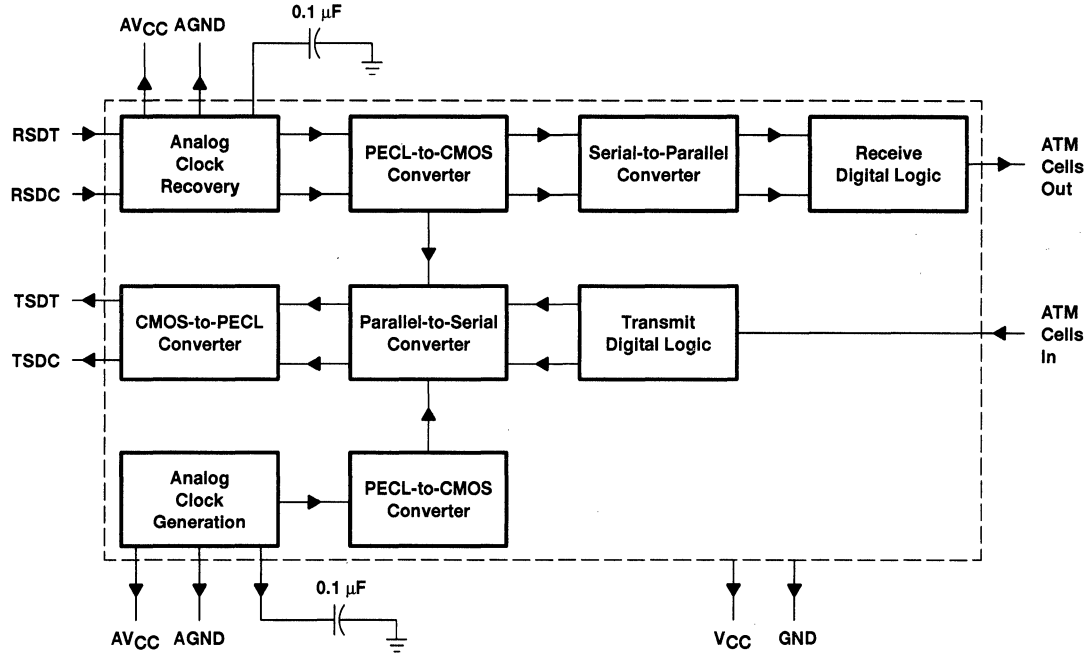
APPLICATION INFORMATION

general layout considerations for the TNETA1500 (continued)

The PECL inputs to the device are terminated using a split-resistor termination of 121 Ω to ground and 82 Ω to V_{CC}. Placing the termination resistors close to the input terminals reduces the possibility of signal reflections and maintains the integrity of the signal waveform. The PECL outputs are also terminated using a split-resistor termination of 121 Ω to ground and 82 Ω to V_{CC}. The termination resistors should be placed as close as possible to the input terminals of the device that the TNETA1500 is driving to prevent reflections and maintain signal integrity.

External capacitors must be connected to the analog PLLs to provide the loop-filter capacitance. One capacitor is required for each APLL. The recommended size of the capacitor is 0.001 – 0.1 µF. Since there is no measurable performance increase over the range of 0.001 – 0.1 µF, any size can be used.

Figure 7 shows a typical connection between the TNETA1500 and fiber-optic or UTP-5 transceiver with PECL inputs and outputs. In this diagram, the AV_{CC} terminals are broken out between the analog clock-recovery block and the analog clock-generation block.

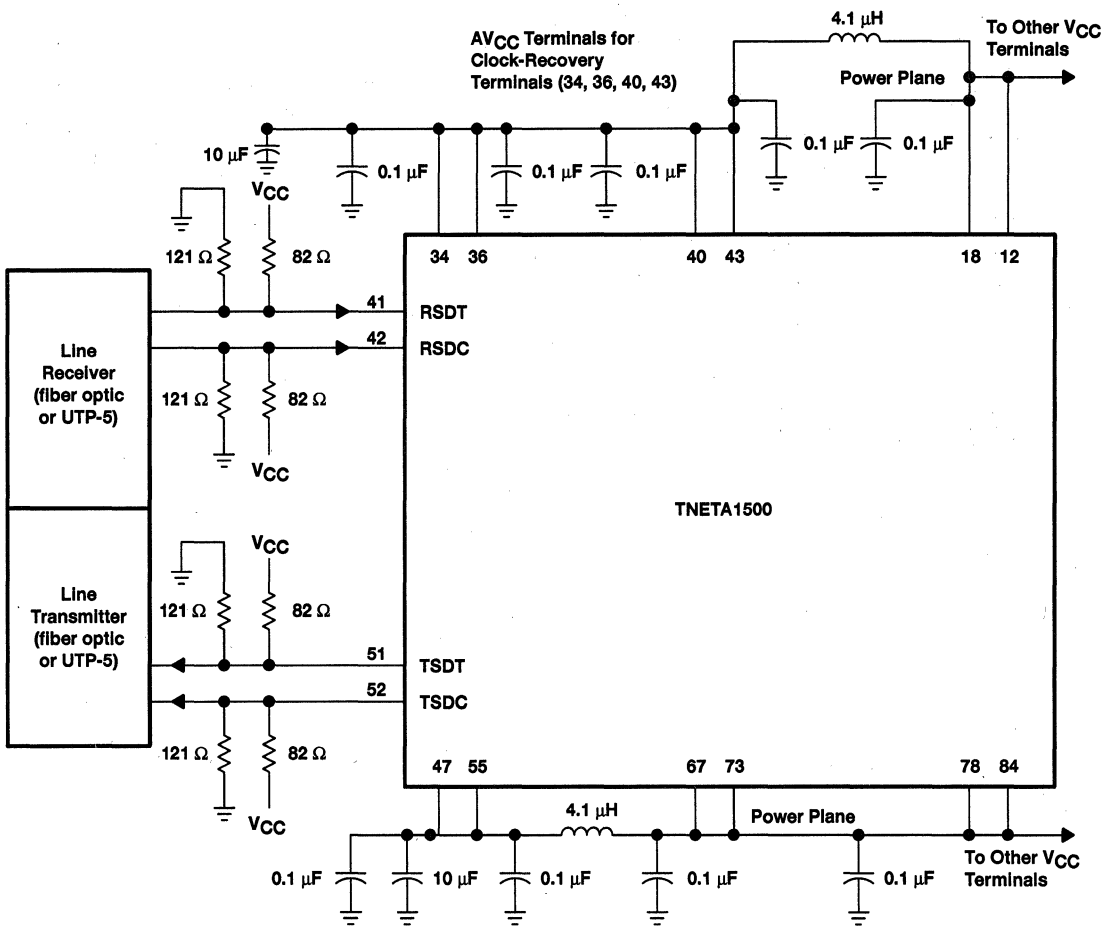


NOTE A: The 0.1-µF capacitors are external and connected to the analog PLLs.

Figure 6. Analog and Digital Blocks in TNETA1500

PRODUCT PREVIEW

APPLICATION INFORMATION



AVCC Terminals for Clock-Generation Terminals (47, 55)

NOTES: A. If the TXHCKT, TXHCKC, RSCT, and RSCC inputs are not used, they need to be terminated as follows:
- TXHCKT (terminal 49) – 1-kΩ resistor to V_{CC}
- TSHCKC (terminal 50) – 1-kΩ resistor to GND
- RSCT (terminal 32) – 1-kΩ resistor to V_{CC}
- RSCC (terminal 33) – 1-kΩ resistor to GND

B. The FLAGT and FLAGC inputs contain internal pullup/pulldown resistors and can be left open.
C. All AGND and GND terminals are connected to the same ground plane.
D. It is recommended that one 0.1-µF capacitor be used for each two V_{CC} terminals (digital-power terminals).
E. Ferrite beads can be used in place of the 4.1-µH inductors. Listed below are the part numbers of beads from Fair-Rite Corporation that can be used. Other beads from other manufacturers may work as well:
- Surface-mount ferrite beads:
  - Fair-Rite P/N 2743021447 (long bead)
  - Fair-Rite P/N 2743019447 (short bead)
- Leaded ferrite bead:
  - Fair-Rite P/N 2743002111

Figure 7. Board Layout for the TNETA1500

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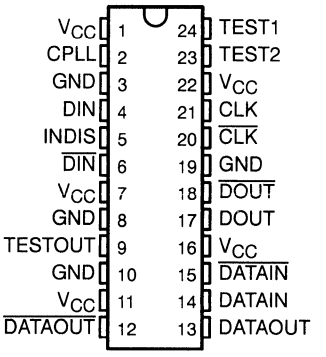
SDNS001B – SEPTEMBER 1992 – REVISED DECEMBER 1994

- **Recovers a 155.52-MHz Clock Signal From a 155.52-Mbit/s STS-3/STM-1 NRZ Data Stream**
- **Accepts Pseudo-ECL (PECL) Input Voltage Levels on the Input Data Stream**
- **Provides a Separate Pseudo-ECL-to-True-ECL Converter for an Additional Data Signal Requiring Conversion**
- **Requires a Single 5-V Supply**

DW PACKAGE
(TOP VIEW)



description

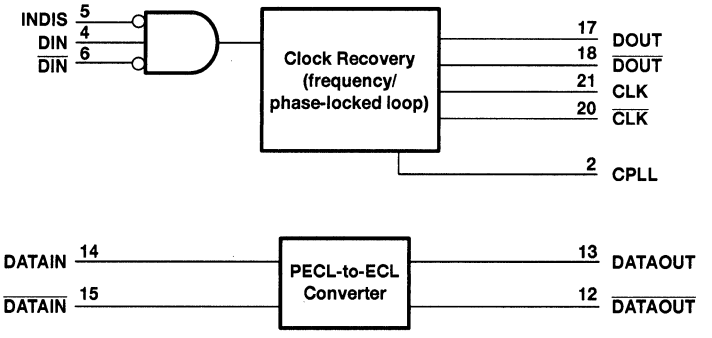
The TNETA1555 device recovers an embedded clock signal from a 155.52-Mbit/s STS-3/STM-1 nonreturn-to-zero (NRZ) data stream using a frequency/phase-locked loop. The device accepts PECL (ECL signals referenced to 5 V instead of GND) input-voltage levels. The recovered clock and data outputs are PECL compatible. The serial data input and recovered clock and data outputs are differential to provide maximum noise immunity.

The input disable (INDIS) disconnects the incoming serial-data stream from the clock-recovery circuitry. When the INDIS input is high, the data output is forced low and the clock-recovery circuitry maintains the output frequency present at the time the input was disabled for a specific amount of time. This time is dependent upon the value of the capacitor in the loop filter.

A PECL-to-ECL converter is included in the device for those applications where an interface between the two different voltage levels is required. An example of such an application is an optical transmitter that requires ECL input voltage levels and a parallel-to-serial converter with pseudo-ECL-level outputs.

The TNETA1555 requires only a positive 5-V supply (5 V ± 5 %) for operation. The device is characterized for operation over a temperature range of –40°C to 85°C.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{CLK}$, CLK	20, 21	O	Recovered clock output. PECL compatible.
CPLL	2	I	Capacitor connection for phase-locked-loop filter (C_{PLL} = 0.1 μF recommended)
DATAIN, $\overline{DATAIN}$,	14, 15	I	PECL-compatible input for PECL-to-ECL converter
$\overline{DATAOUT}$, DATAOUT	12, 13	O	ECL-compatible output for PECL converter
DIN, $\overline{DIN}$	4, 6	I	Serial data input. PECL compatible.
$\overline{DOUT}$, DOUT	18, 17	O	Serial data output. PECL compatible.
GND	3, 8, 10, 19		Ground (0-V reference)
INDIS	5	I	Input disable terminal (TTL compatible). The device ignores the input data when INDIS is active and forces DOUT low and $\overline{DOUT}$ high.
TESTOUT	9	O	Manufacturing test output. Leave open.
TEST2	23	I	Manufacturing test input. Tied to GND.
TEST1	24	I	Manufacturing test input. Tied to GND.
V_{CC}	1, 7, 11, 16, 22		Supply voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range, TTL ..... −1.2 V to 7 V
Input voltage range, ECL ..... −5.5 V to 0 V
Input voltage range, pseudo-ECL ..... 0 V to 7 V
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage, TTL	2			V
V_{IL}	Low-level input voltage, TTL			0.8	V
I_{IK}	Input clamp current, TTL			−18	mA
V_{IH}	High-level input voltage, PECL (see Note 2)	V_{CC} −1.1		V_{CC} −0.8	V
V_{IL}	Low-level input voltage, PECL (see Note 2)	V_{CC} −1.9		V_{CC} −1.5	V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	DOUT, $\overline{\text{DOUT}}$, CLK, $\overline{\text{CLK}}$	V_{CC} = 4.75 V to 5.25 V,	See Notes 2 and 3	V_{CC} –1.03		V_{CC} –0.85	V
		DATAOUT, $\overline{\text{DATAOUT}}$	V_{CC} = 4.75 V,	See Notes 2 and 4	–1.02		–0.75	
V_{OL}	Low-level output voltage	DOUT, $\overline{\text{DOUT}}$, CLK, $\overline{\text{CLK}}$	V_{CC} = 4.75 V to 5.25 V,	See Notes 2 and 3	V_{CC} –1.85		V_{CC} –1.62	V
		DATAOUT, $\overline{\text{DATAOUT}}$	V_{CC} = 4.75 V,	See Notes 2 and 4	–1.81		–1.58	
V_{IK}	Input clamp voltage	INDIS	V_{CC} = 4.75 V,	I_I = –18 mA			–1.2	V
I_I	Input current	INDIS	V_{CC} = 5.25 V,	V_I = V_{CC} or GND			±1	µA
I_{IH}	High-level input current	DIN, $\overline{\text{DIN}}$, DATAIN, $\overline{\text{DATAIN}}$	V_{CC} = 5.25 V,	V_I = 4.45 V			50	µA
I_{IL}	Low-level input current	DIN, $\overline{\text{DIN}}$, DATAIN, $\overline{\text{DATAIN}}$	V_{CC} = 5.25 V,	V_I = 3.35 V			50	µA
I_{CC}	Supply current		V_{CC} = 5.25 V, Outputs open	f_i = 155.52 Mbit/s,		71	100	mA
			V_{CC} = 5.25 V, See Note 5	f_i = 155.52 Mbit/s,		112	150	mA

NOTES: 2. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.
3. These outputs are terminated through a 50-Ω resistor to V_{CC} –2 V.
4. These outputs are terminated through a 50-Ω resistor to –2 V.
5. DOUT, $\overline{\text{DOUT}}$, CLK, and $\overline{\text{CLK}}$ are each terminated with a 50-Ω resistor to V_{CC} –2 V. DATAOUT and $\overline{\text{DATAOUT}}$ are each terminated with a 50-Ω resistor to –2 V.

operating characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Acquisition time	See Note 6	C_{PLL} = 330 pF		1		ms
		C_{PLL} = 0.1 µF		3		
Deviation of clock sampling point, t_{csp}	See Figure 1		–800		800	ps
RMS jitter, recovered clock	See Note 7			1.5°	4°	°RMS
Input data rate				155.52		Mb/s
Duty cycle, recovered clock	See Note 3		45%		55%	
Maximum number of consecutive bits (1 or 0) in input data stream	See Note 8		100	450		

NOTES: 3. These outputs are terminated through a 50-Ω resistor to V_{CC} –2 V.
6. Acquisition time is the time required to achieve a valid clock output while applying a 2^7 –1 pseudo-random bit sequence.
7. RMS jitter is measured with a 2^{31} –1 pseudo-random bit sequence.
8. This measurement is made with a 2^{13} –1 pseudo-random bit sequence with string substitution.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{PLH}	DATAIN or $\overline{\text{DATAIN}}$	DATAOUT or $\overline{\text{DATAOUT}}$	1.5	4.5	ns
t_{PHL}	DATAIN or $\overline{\text{DATAIN}}$	DATAOUT or $\overline{\text{DATAOUT}}$	1.5	4.5	ns

PARAMETER MEASUREMENT INFORMATION

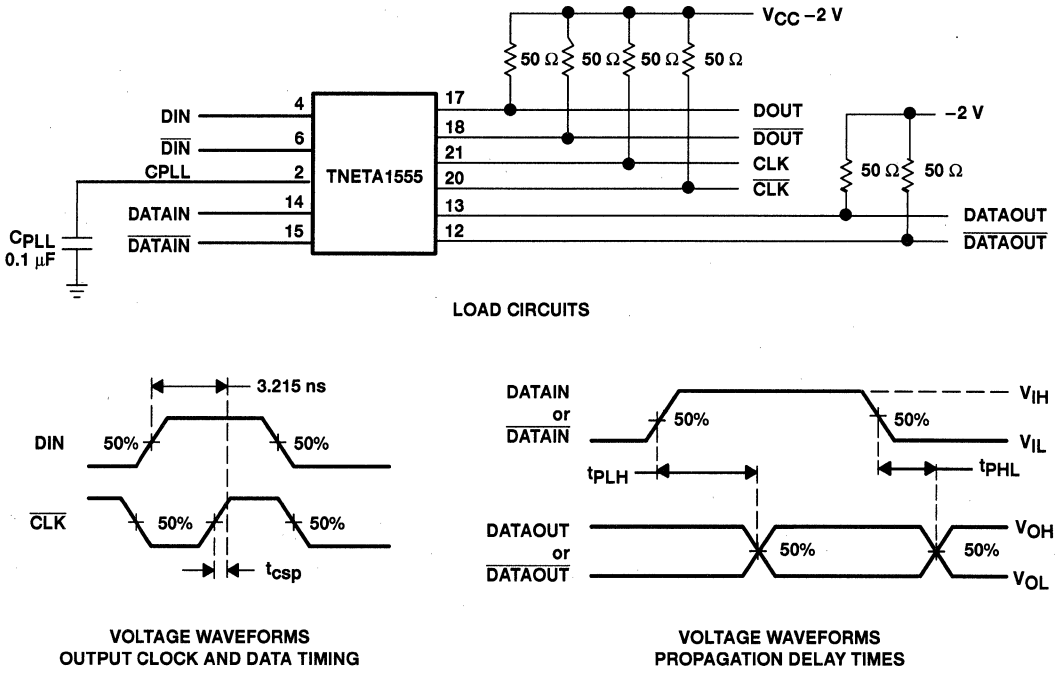


Figure 1. Load Circuits and Voltage Waveforms

APPLICATION INFORMATION

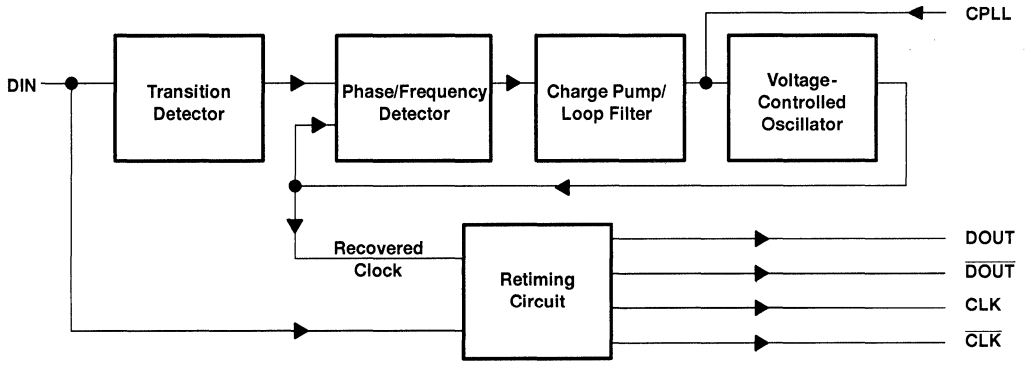
introduction

The TNETA1555 clock-recovery device provides clock recovery and data retiming on a nonreturn to zero (NRZ) serial input data stream. The device uses an analog phase-locked loop (APLL) with an integrated voltage controlled oscillator (VCO) to recover the imbedded clock signal from incoming data. A loop-filter capacitor is the only external component required for the proper operation of the device. The TNETA1555 is designed for operation with a 155.52-Mbit/s serial-data stream. The device has pseudo-ECL compatible inputs and outputs and operates from a single 5-V supply. Pseudo-ECL levels are referenced to 5 V instead of ground.

Since the incoming 155.52-Mbit/s data stream does not contain a 155.52-MHz frequency component, a transition detector, shown on the clock-recovery block diagram, is used as a frequency doubler to generate this frequency. The output of the transition detector is passed to a phase/frequency detector where it is compared to the output of the VCO. The phase/frequency detector is actually comprised of two circuits. One circuit provides a coarse frequency-detection capability and a second provides a finer phase adjustment. The phase/frequency detector compares the signal from the transition detector to the VCO output and generates signals to either increase or decrease the VCO frequency, depending upon whether the VCO frequency is less than or greater than the frequency of the signal from the transition detector. The up/down pulses are sent to the charge pump/loop filter for conversion to a bias voltage that sets the VCO output frequency.

The process of comparing the input signal frequency and the VCO output frequency is continuous and eventually results in the VCO output frequency equaling the frequency of the input signal. It also allows the VCO output to react to changes in the input signal due to jitter. The recovered clock output is sent from the VCO to the retiming circuit where the input data is retimed to the recovered clock. The retiming circuit centers the output clock in the middle of the output data.

clock-recovery block diagram



performance measurements

Measuring the performance of a clock-recovery circuit involves determining how well the circuit operates in the presence of jitter. Jitter is defined as the short-term variations of digital signals significant instants from their ideal positions in time (see Note 9). For testing purposes, jitter is usually generated by modulating a digital data sequence with a sinusoidal waveform of a known frequency. This results in a digital data stream where the widths of the individual data pulses vary with time. The amount of pulse-width variation can be changed by altering the frequency and amplitude of the modulating signal, which changes the amount of jitter in the data stream. The following paragraphs describe the test results obtained from the TNETA1555 for various performance measurements.

NOTE 9: Bellcore technical reference TR-TSY-000499 Issue 3, December 1989, page 7-1.

APPLICATION INFORMATION

RMS jitter

This test provides a measure of the internal jitter performance of the clock-recovery circuit. A data stream with very low jitter (all data generators have a small amount of jitter) is input to the clock-recovery device, and the jitter of the recovered clock is measured. A $2^{31}-1$ pseudo-random bit sequence (PRBS) is used for the input data stream. For this test, the worst-case jitter performance was measured with V_{CC} = 4.75 V at an operating free-air temperature of 85°C. Table 1 summarizes these test results.

Table 1. Worst-Case RMS Jitter Measurement, V_{CC} = 4.75, T_A = 85°C

Device No.	1	2	3	4	5	6	7	8	9
Jitter (° RMS)	3.5	3.2	3.5	3.3	3.1	3.5	3.1	3.0	3.4

jitter tolerance

Jitter tolerance is a measure of the ability of the clock-recovery circuit to tolerate an input signal without experiencing a bit error. For this test, the Bellcore SONET category II jitter-tolerance mask was used (Bellcore specification TR-NWT-000253). The worst-case performance was measured with V_{CC} = 5.25 V at an operating free-air temperature of 85°C. Table 2 and Figure 2 show the results of this test.

Table 2. Jitter Tolerance Values Used in the Graph of Figure 2

Frequency H_z	Bellcore	TNETA1555
10	15	N.A.
30	15	N.A.
300	1.5	10
1k	1.5	10
2k	1.5	10
5k	0.81	10
10k	0.3	1
20k	0.15	1
50k	0.15	1
100k	0.15	0.658
200k	0.15	0.382
500k	0.15	0.34
1M	0.15	0.536
2M	0.15	0.515
3.5M	0.15	0.486
4M	0.15	0.493

APPLICATION INFORMATION

jitter tolerance (continued)

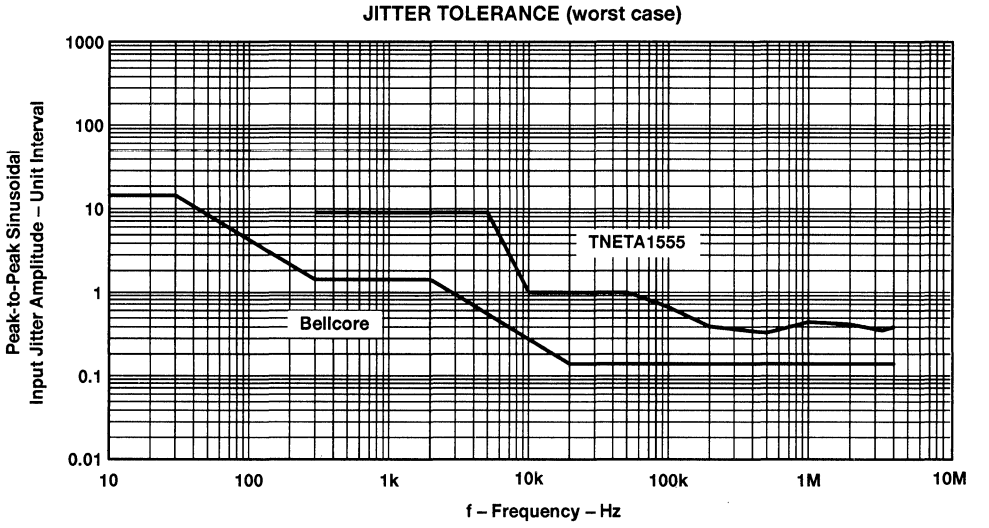


Figure 2

transitionless bit periods

The SONET/SDH specifications do not use a line code that limits the number of transitionless bit periods in a bit stream to a specific number. Instead, a scrambler is used to provide some randomization of the line signal. As long as the output data stream does not match the output of the scrambler, this technique works fairly well. However, it is possible for the scrambled data stream to contain a large number of transitionless bit periods, depending upon the data being transmitted. It is important that the clock-recovery device handle large numbers of transitionless bit periods without causing a bit error. Figures 3 and 4 show the results of tests conducted on the TNETA1555 for transitionless bit periods. The y-axis shows the number of transitionless bit periods that the devices can accept before a bit error is recorded on the bit-error rate tester.

APPLICATION INFORMATION

transitionless bit periods (continued)

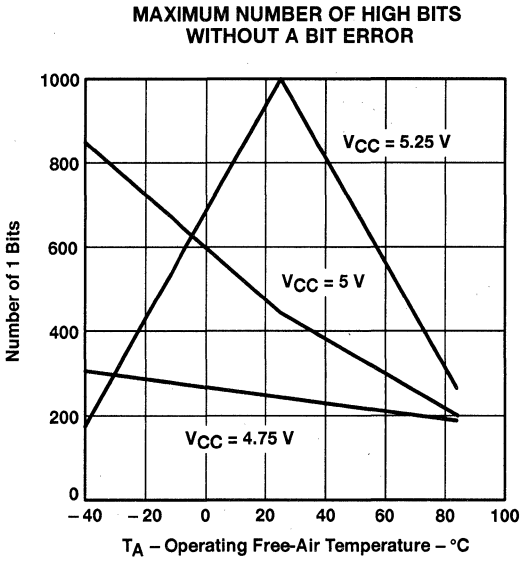


Figure 3

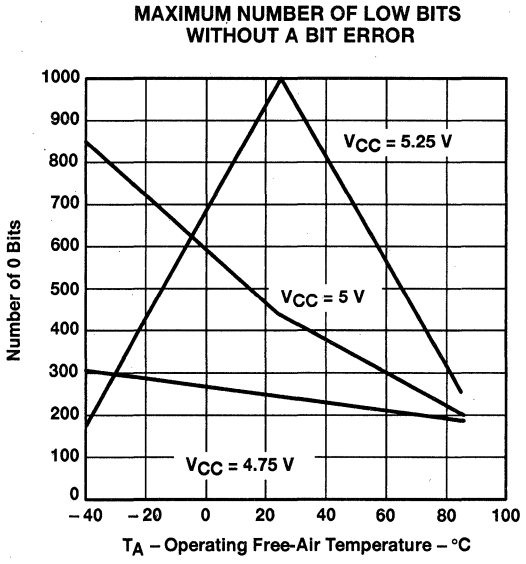


Figure 4

jitter transfer (peaking and bandwidth)

SONET/SDH regenerator interfaces are required to meet jitter-transfer requirements. Jitter transfer is the ratio of measured output jitter to applied input jitter, and it is measured in decibels. Meeting the jitter-transfer requirement in SONET/SDH regenerators requires either a clock-recovery circuit with a voltage-controlled crystal oscillator (VCXO) or a similar technique that provides extremely low jitter. The TNETA1555 provides a typical jitter-transfer bandwidth of approximately 2 MHz. This is where the device begins to attenuate the input jitter so that the output jitter is less than the input jitter. The device exhibits minimal jitter peaking when a capacitor of approximately 0.1 μF is used in the loop filter. The peaking is less than 0.3 dB, which is the resolution of the test equipment used to measure this parameter.

external connections

loop-filter capacitor

The capacitor for the loop filter is connected from terminal 2 of the TNETA1555 to ground. It is recommended that a 0.1-μF chip capacitor be used. A smaller capacitor reduces the amount of acquisition time required for the device to lock on to the input data stream while it increases the amount of jitter peaking that can occur. A larger capacitor results in a longer acquisition time and does not provide any noticeable increase in jitter performance.

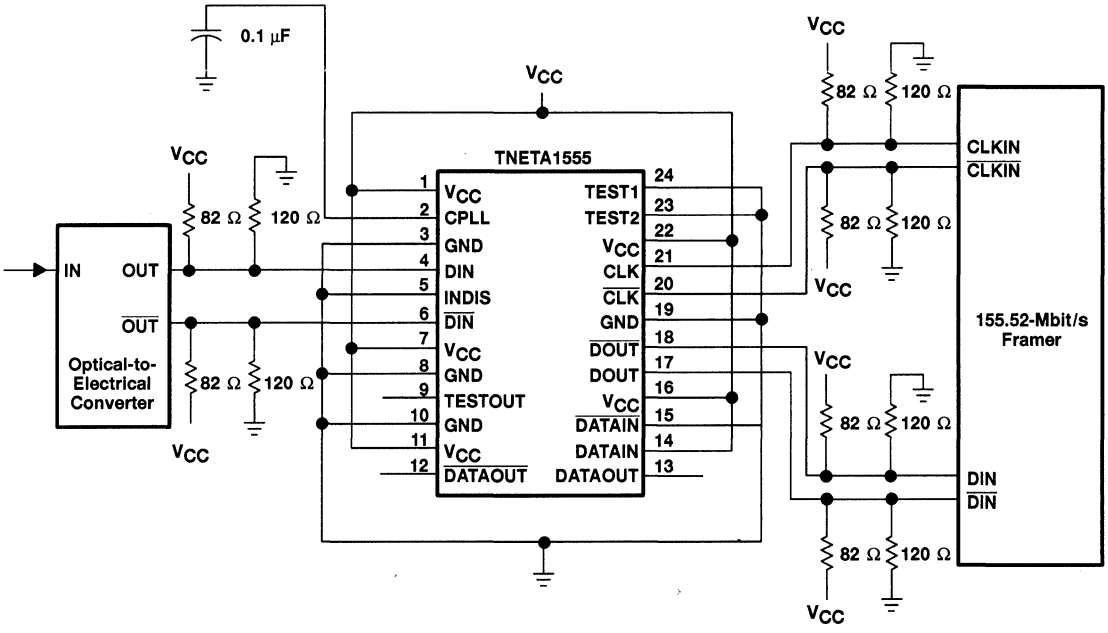
signal connections

Figure 5 shows a typical connection between the TNETA1555 clock-recovery device, an optical-to-electrical converter, and a framer device. The TNETA1555 clock-recovery circuit accepts pseudo-ECL compatible signals at the serial data inputs DIN and $\overline{\text{DIN}}$. The retimed pseudo-ECL clock outputs are provided at outputs $\overline{\text{CLK}}$ and CLK. The pseudo-ECL inputs and outputs require a 50-Ω termination to V_{CC} –2 V (or a Thevenin equivalent). The Thevenin equivalent circuit consists of an 82-Ω resistor to V_{CC} and 120-Ω resistor to ground.

APPLICATION INFORMATION

signal connections (continued)

A separate pseudo-ECL to ECL converter is also provided on the TNETA1555. The pseudo-ECL inputs require a 50-Ω to V_{CC} –2 V termination (or a Thevenin equivalent) and the ECL outputs require a 50-Ω to –2 V termination (or its equivalent). Figure 6 shows the external connections for the pseudo-ECL to ECL converter.



NOTES: A. Terminating resistors should be placed as close to the input terminal as possible.
B. The 0.1-µF bypass capacitors should be connected from the V_{CC} terminals to ground.

Figure 5. TNETA1555 External Connections (PECL-to-ECL converter not used)

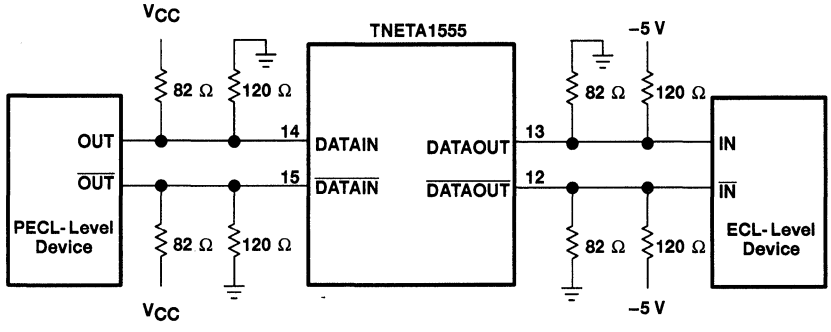


Figure 6. External Connections for PECL-to-ECL Converter

- **SBus Device That Provides Asynchronous Transfer-Mode Interface**
- **Single-Chip Segmentation and Reassembly (SAR) for Full-Duplex ATM Adaptation-Layer (AAL) Processing**
- **On-Chip SBus Host Interface Allows Use of Host Memory for Packet SAR**
- **53-Byte ATM Cells Are Transparent to the User**
- **Provides Complete Encapsulation and Termination of AAL5 and Limited AAL3/4**
- **Features a Null AAL That Provides Functions for Constant-Bit-Rate Services**
- **Supports 1023 Unique Virtual Circuits (VCs) on Receive Side**
- **Explicit Cell-Level Interleaving Between Groups of VCs**
- **Packet Interface Is Managed by Efficient Descriptor Rings**
- **Physical (PHY)-Layer Interface Is Full Duplex and Compliant to the ATM Forum UTOPIA Contribution**
- **Supports PHY-Layer Data Rates in the Range of 25.6 Mbit/s to 155.52 Mbit/s**
- **Interfaces Directly to the TNETA1500 SONET ATM BiCMOS Receiver/Transmitter (SABRE)**
- **Recognizes ATM-Layer Operation and Maintenance (OAM) Cells**
- **No External Logic Required for Host Bus to Ensure Simple Design**

description

The TNETA1560 is an asynchronous transfer mode (ATM) segmentation and reassembly (SAR) device with an SBus interface. This device incorporates ATM adaptation-layer (AAL) processing, ATM SAR processing for full-duplex operation up to the STS-3c rate of 155.52 Mbit/s, and the controls for the register interface on the physical (PHY) layer. The device provides a packet interface that is managed by descriptor rings, making the 53-byte ATM-framing format transparent to the user. The device passes the payload of 48 bytes, constituting the payload of each cell, across the SBus-host interface. All packets are segmented and reassembled in host memory and accessed by the chip via the descriptor-ring mechanism. This operation reduces the memory requirements for network-interface cards (NICs). The TNETA1560 requires no local processor on the card, which enables very compact solutions.

The applications for the TNETA1560 include NICs for client workstations and servers, embedded applications like LAN emulation, and multiprotocol systems like video servers. The TNETA1560 provides complete AAL5 encapsulation and termination in hardware. In addition, limited support is provided for AAL 3/4, and a null AAL is provided to facilitate real-time data transfer. The TNETA1560 recognizes ATM-layer operation and maintenance (OAM) cells.

In the transmit direction, the TNETA1560 generates data via a special bit-rate control table that provides explicit cell-level interleaving between groups of virtual circuits (VCs). This mechanism brings a higher degree of flexibility when specifying peak rates for each group (up to 155.52 Mbit/s at a resolution greater than 32 kbit/s). The VCs within a group are serviced via a first-in, first-out (FIFO) discipline on a per-packet basis.

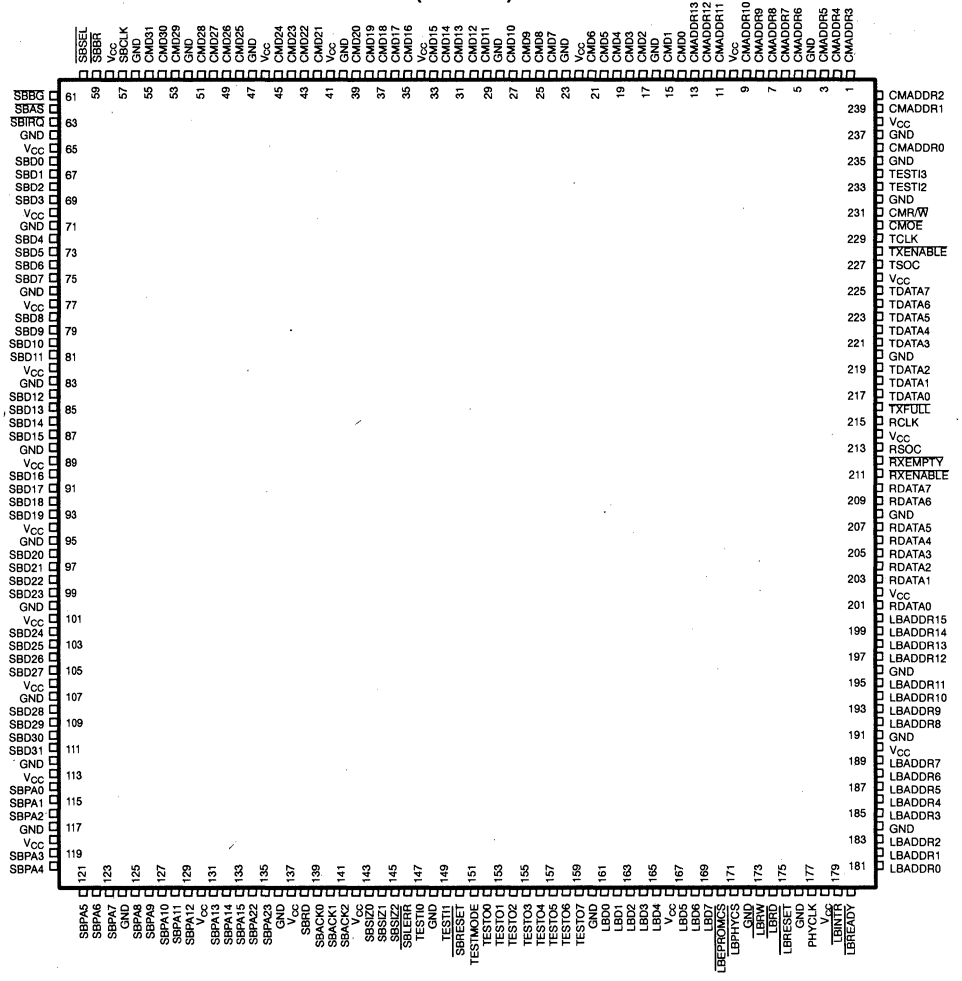
In the receive direction, the TNETA1560 allows multiple virtual paths (VPs) with the condition that each VC is unique. The device is primarily intended for AAL5 encapsulation and termination that is supported in hardware.

The TNETA1560 has four interfaces that include: the SBus interface with a 32-bit-wide data bus, the cell interface based on the universal test and operations interface for ATM (UTOPIA), a control-memory interface to access the local SRAM, and the local-bus interface to access the PHY-layer register and an EPROM. The UTOPIA interface to the PHY layer consists of an 8-bit-wide data path and associated control signals in both the transmit and receive directions. The 53-byte ATM cells pass between the ATM and PHY layers.

PRODUCT PREVIEW

PRODUCT PREVIEW

PGC PACKAGE
(TOP VIEW)



description (continued)

The native clock for the TNETA1560 is the SBus clock, which can range between 16.67 MHz and 25 MHz. The native word size for the device is 32 bits, corresponding to the data width for the SBus. The control-memory interface is 32 bits wide. This interface allows the device to access the local memory to obtain the control information on the packets being segmented and reassembled and to obtain their locations in host memory. Each packet queued for transmission can be distributed across multiple buffers in host memory with each starting at any byte boundary. This is supported in hardware by the device. Every received package is placed in a single buffer in the host memory and is aligned to a 16-byte boundary. The TNETA1560 operation is explained in detail in the Principles of Operation section.

Terminal Functions

SBus interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
SBACK2–SBACK0	139–141	I/O	SBus acknowledge. SBACK2–SBACK0 are used to indicate SBus word acknowledgement for word operations on the TNETA1560 registers and control memory if set to 011. If set to 101, the SBus byte acknowledgement is for local bus operations. An error acknowledgement is indicated if set to 110. SBACK2–SBACK0 can be driven by the system or by the TNETA1560 in slave mode.
$\overline{\text{SBAS}}$	62	I	SBus address strobe. When $\overline{\text{SBAS}}$ is low, an address is loaded in the TNETA1560.
$\overline{\text{SBBG}}$	61	I	SBus bus grant. $\overline{\text{SBBG}}$ is asserted by the SBus controller to make the TNETA1560 the master.
$\overline{\text{SBBR}}$	59	O	SBus request. $\overline{\text{SBBR}}$ is asserted by the TNETA1560 to request operation as the SBus master.
SBCLK	57	I	SBus clock
SBD31–SBD0	66–69, 72–75, 78–81, 84–87, 90–93, 96–99, 102–105, 108–111	I/O	SBus data bus. SBD31–SBD0 provide access from the host to the contents of the TNETA1560 internal registers.
$\overline{\text{SBIRQ}}$	63	O	SBus interrupt request. $\overline{\text{SBIRQ}}$ is asserted by the TNETA1560 to send an interrupt request to the host.
$\overline{\text{SBLERR}}$	146	I	SBus late error. $\overline{\text{SBLERR}}$ is considered a fatal error. $\overline{\text{SBLERR}}$ causes the TNETA1560 to terminate the ongoing master-bus cycle. If $\overline{\text{SBLERR}}$ is a burst transfer, it completes the burst.
SBPA15–SBPA0 SBPA22–SBPA23	114–116, 119–123, 125–129, 131–133 134–135	I	SBus physical address. SBPA15–SBPA0 and SBPA22–SBPA23 provide the address for the host to access the peripheral devices and the TNETA1560 internal registers via SBus slave-mode transactions.
$\overline{\text{SBRESET}}$	150	I	SBus reset. $\overline{\text{SBRESET}}$ is active low.
SBRD	138	I/O	SBus read. SBRD can be driven by the system or by the TNETA1560 when SBRD is operating as the master. SBRD indicates a read when high and a write when low.
$\overline{\text{SBSEL}}$	60	I	SBus select. $\overline{\text{SBSEL}}$ is active low and enables the host to access the TNETA1560 device.
SBSIZ2–SBSIZ0	143–145	I/O	SBus data-transfer size signals. SBSIZ2–SBSIZ0 are used to indicate the size of data transfers between the TNETA1560 and the host.

PRODUCT PREVIEW

Terminal Functions (Continued)

PHY-layer receive interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
RCLK	215	O	Receive clock. RCLK is equivalent to the internal clock at 19.44 MHz. RCLK is sent to the PHY layer.
RDATA7–RDATA0	201. 203–207, 209–210	I	Receive data. RDATA7–RDATA0 are connected to the PHY-layer receive interface.
RSOC	213	I	Receive start of cell. The PHY layer sends RSOC with the output data.
$\overline{\text{RXEMPTY}}$	212	I	Receive buffer empty in PHY layer. $\overline{\text{RXEMPTY}}$ acts as an inverted enable signal on the PHY-layer receive.
$\overline{\text{RXENABLE}}$	211	O	Receive enable. $\overline{\text{RXENABLE}}$ is active low and is driven by the TNETA1560.

PHY-layer transmit interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TCLK	229	O	Transmit clock. The TNETA1560 generates TCLK at the SBus frequency and sends it to the PHY layer. TCLK is an inverted version of the internal clock.
TDATA7–TDATA0	217–219, 221–225	O	Transmit data. TDATA7–TDATA0 are sent at the rate of the SBus clock and are driven by the TNETA1560.
TSOC	227	O	Transmit start of cell. TSOC is sent to the PHY layer with the transmit output data and indicates that the first byte of an ATM cell was transmitted to the PHY layer.
$\overline{\text{TXENABLE}}$	228	O	Transmit enable. The TNETA1560 turns off $\overline{\text{TXENABLE}}$ when the PHY layer sends the $\overline{\text{TXFULL}}$ signal.
$\overline{\text{TXFULL}}$	216	I	Transmit buffer full in the PHY layer. The PHY layer asserts $\overline{\text{TXFULL}}$ at least four cycles before any internal buffers are full. This makes the TNETA1560 stop the data transmission to the PHY layer.

control-memory interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CMADDR13–CMADDR0	236 239–240, 1–3, 5–9, 11–13	O	Control-memory address. CMADDR13–CMADDR0 are used to access the data structures in control memory.
CMD31–CMD0	14–15 17–21, 24–27, 29–33, 35–39, 42–45, 48–51, 53–55	I/O	Control-memory data bus. CMD31–CMD0 are 32-bit data bus. This control-memory interface is designed for 20-ns asynchronous SRAMs. The TNETA1560 uses CMD31–CMD0 to write and read data from its data structures in the control memory.
$\overline{\text{CMOE}}$	230	O	Control-memory output enable. $\overline{\text{CMOE}}$ is an active-low signal.
CMR/$\overline{\text{W}}$	231	O	Control-memory read/write. CMR/$\overline{\text{W}}$ determines a read or write operation. If CMR/$\overline{\text{W}}$ is low, it is a write operation. If CMR/$\overline{\text{W}}$ is high, it is a read operation.

PRODUCT PREVIEW

Terminal Functions (Continued)

local-bus interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
LBADDR15–LBADDR0	181–183, 185–189, 192–195, 197–200	O	Local-bus address. LBADDR15–LBADDR0 are the lower 16 bits of the SBus address bus and are routed directly to the local-bus address lines.
LBD7 – LBD0	161–165, 167–169	I/O	Local-bus data. LBD7–LBD0 are used to transfer data to/from local slave devices.
$\overline{\text{LBEPROMCS}}$	170	O	Local-bus EPROM chip-select. $\overline{\text{LBEPROMCS}}$ is an active-low signal.
$\overline{\text{LBINTR}}$	179	I	Local-bus interrupt. $\overline{\text{LBINTR}}$ is generated by a local-bus device.
$\overline{\text{LBPHYCS}}$	171	O	Local-bus PHY-layer chip select. $\overline{\text{LBPHYCS}}$ is used to interface with PHY-layer devices.
$\overline{\text{LBRD}}$	174	O	Local-bus read. $\overline{\text{LBRD}}$ is an active-low signal that indicates a read operation.
$\overline{\text{LBREADY}}$	180	I	Local-bus-ready. $\overline{\text{LBREADY}}$ is driven by local slave devices. The bus transaction must be completed after eight SBus cycles regardless of $\overline{\text{LBREADY}}$. $\overline{\text{LBREADY}}$ is accepted by the TNETA1560 as a handshake from the devices on the bus.
$\overline{\text{LBRESET}}$	175	O	Local-bus reset output. $\overline{\text{LBRESET}}$ is an active-low signal.
$\overline{\text{LBRW}}$	173	O	Local-bus write. $\overline{\text{LBRW}}$ is an active-low signal that indicates a write operation.

control and configuration

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
PHYCLOCK	177	I	PHY-layer clock. PHYCLOCK is a 19.44-MHz clock signal driven by a PHY-layer clock crystal.
TESTI3–TESTI0	147, 149, 233–234	I/O	Test signals. TEST13–TESTI0 are for manufacturer use only. These signals are tied low for normal operation.
TESTMODE	151	I	Test-mode configuration. TESTMODE is tied low for normal operation. TESTMODE is for manufacturer use only.
TESTO7–TESTO0	152–159	I/O	Test signals. TESTO7 – TESTO0 are left open for normal operation. TESTO7–TESTO0 are for manufacturer use only.

power and ground

NAME	TERMINAL NO.	DESCRIPTION
GND	4, 16, 23, 28, 40, 47, 52, 56, 64, 71, 76, 83, 88, 95, 100, 107, 112, 117, 124, 136, 148, 160, 172, 176, 184, 191, 196, 208, 220, 232, 235, 237	Ground
V_{CC}	10, 22, 34, 41, 46, 58, 65, 70, 77, 82, 89, 94, 101, 106, 113, 118, 130, 137, 142, 166, 178, 190, 202, 214, 226, 238	Supply voltage

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 6 V
Input voltage range, V_I ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 2) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 3) ..... ±20 mA
Operating free air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the GND terminals.
2. Applies for external input and bidirectional buffers
3. Applies for external output and bidirectional buffers

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			4.75	5	5.25	V
V_{IH}	High-level input voltage	CMOS	V_{CC} = 4.75 V	3.325			V
			V_{CC} = 5.25 V	3.675			
		TTL		2			
V_{IL}	Low-level input voltage	CMOS	V_{CC} = 4.75 V			0.95	V
			V_{CC} = 5.25 V			1.05	
		TTL				0.8	
T_A	Operating free-air temperature			0		70	°C

electrical characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 8 mA	V_{CC}−0.8		V
		I_{OL} = 4 mA	V_{CC}−0.8		
V_{OL}	Low-level output voltage	I_{OH} = 8 mA		0.5	V
		I_{OL} = 4 mA		0.5	
I_{OZ}	High-impedance state output current	V_I = V_{CC} or GND		±10	µA
I_{IL}	Low-level input current	V_I = GND		−1	µA
I_{IH}	High-level input current	V_I = V_{CC}		1	µA

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timing requirements (see Note 4 and Figure 1)

NO.			MIN	MAX	UNIT
1	$t_{w(RCLKH)}$	Pulse duration, RCLK high	12		ns
2	$t_{w(RCLKL)}$	Pulse duration, RCLK low	12		ns
3	$t_{su(RSOC)}$	Setup time, RSOC high before RCLK↑	10		ns
4	$t_{su(RXEMPTY)}$	Setup time, $\overline{\text{RXEMPTY}}$ low before RCLK↑	10		ns
5	$t_{su(RDATA)}$	Setup time, RDATA valid before RCLK↑	10		ns
6	$t_{h(RSOC)}$	Hold time, RSOC high after RCLK↑	1		ns
7	$t_{h(RXEMPTY)}$	Hold time, $\overline{\text{RXEMPTY}}$ low after RCLK↑	1		ns

NOTE 4: All output signals are generated on the rising edge of RCLK.

operating characteristics (see Note 4 and Figure 1)

NO.			MIN	MAX	UNIT
8	$t_{d(RXENABLE)}$	Delay time, RCLK↑ to $\overline{\text{RXENABLE}}$↑	1	20	ns

NOTE 4: All output signals are generated on the rising edge of RCLK.

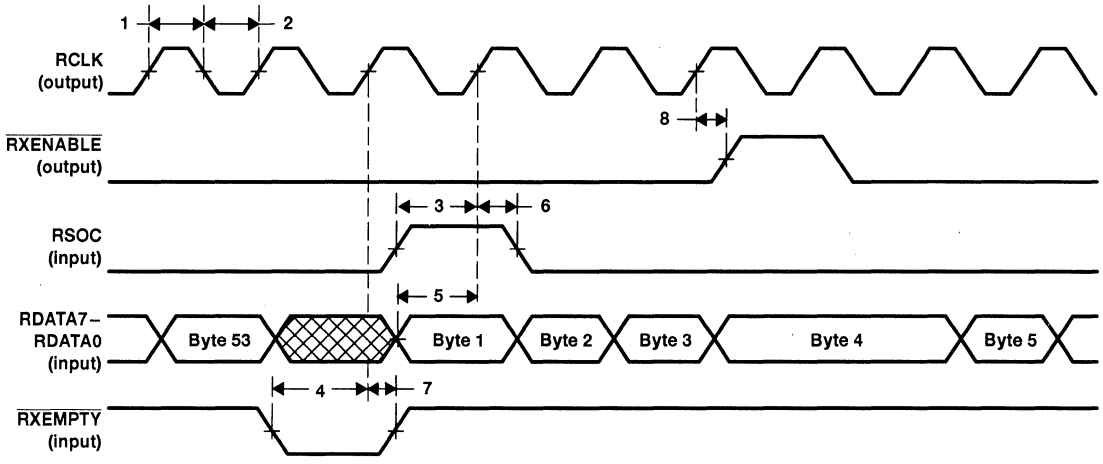

Figure 1. Receive-Cell Interface

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timing requirements (see Note 5 and Figure 2)

NO.			MIN	MAX	UNIT
1	$t_{w(TCLKH)}$	Pulse duration, TCLK high	12		ns
2	$t_{w(TCLKL)}$	Pulse duration, TCLK low	12		ns
3	$t_{su(TXFULL)}$	Setup time, $\overline{TXFULL}$ low before TCLK↑	10		ns
4	$t_{h(TXFULL)}$	Hold time, $\overline{TXFULL}$ low after TCLK↑	1		ns

NOTE 5: All output signals are generated on the rising edge of RCLK. All inputs are sampled on the rising edge of TCLK.

operating characteristics (see Note 5 and Figure 2)

NO.			MIN	MAX	UNIT
5	$t_{d(TXENABLE)}$	Delay time, TCLK↑ to $\overline{TXENABLE}$↓	1	20	ns
6	$t_{d(TSOC)}$	Delay time, TCLK↑ to TSOC↑	1	20	ns
7	$t_{d(TDATA)}$	Delay time, TCLK↑ to TDATA valid	1	20	ns

NOTE 5: All output signals are generated on the rising edge of RCLK. All inputs are sampled on the rising edge of TCLK.

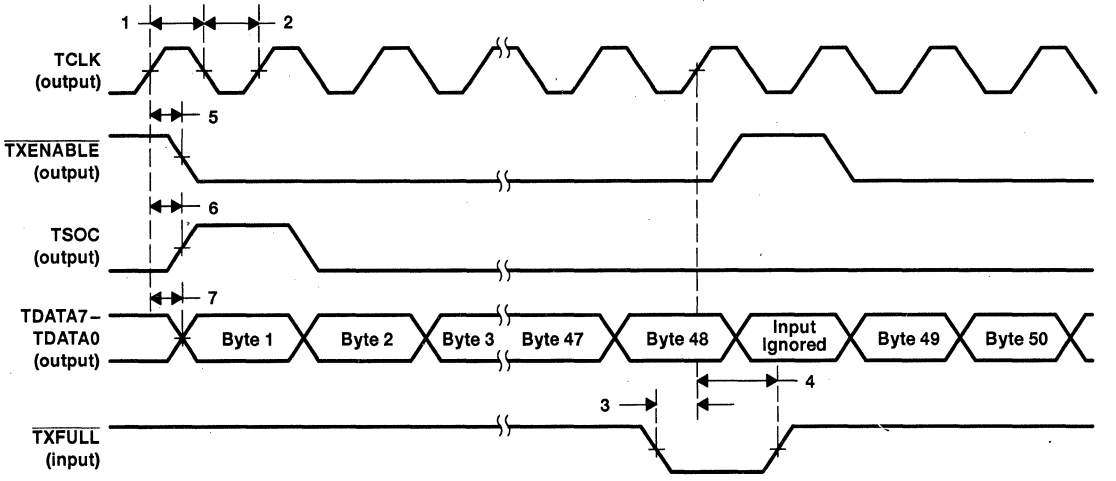

Figure 2. Transmit-Cell Interface

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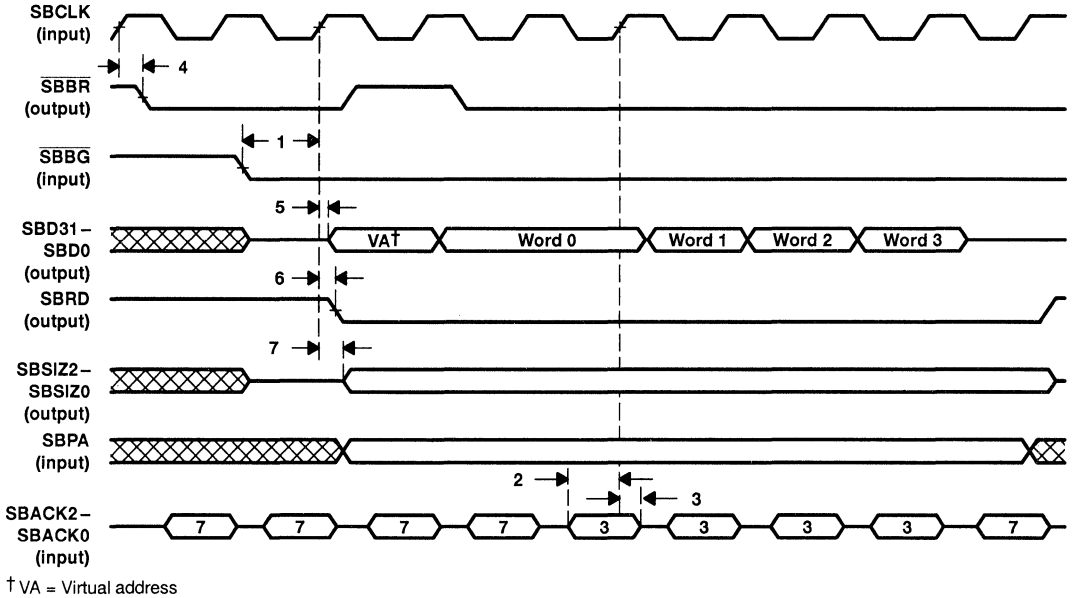
timing requirements (see Figure 3)

NO.			MIN	MAX	UNIT
1	$t_{su(SBBG)}$	Setup time, $\overline{SBBG}$ low before SBCLK↑	15		ns
2	$t_{su(SBACK)}$	Setup time, SBACK2–SBACK0 valid before SBCLK↑	15		ns
3	$t_{h(SBACK)}$	Hold time, SBACK2–SBACK0 valid after SBCLK↑	0		ns

operating characteristics (see Figure 3)

NO.			MIN	MAX	UNIT
4†	$t_{d(SBBR)}$	Delay time, SBCLK↑ to $\overline{SBBR}$↓	2.5	22	ns
5†	$t_{d(SBD)}$	Delay time, SBCLK↑ to SBD31–SBD0 valid	2.5	22	ns
6†	$t_{d(SBRD)}$	Delay time, SBCLK↑ to SBRD↓	2.5	22	ns
7†	$t_{d(SBSIZ)}$	Delay time, SBCLK↑ to SBSIZ2–SBSIZ0 valid	2.5	22	ns

† Numbers are given for SBus clock frequency of 25 MHz.



† VA = Virtual address

Figure 3. TNETA1560 Write Operation (TNETA1560 as Master in This Burst Operation)

PRODUCT PREVIEW

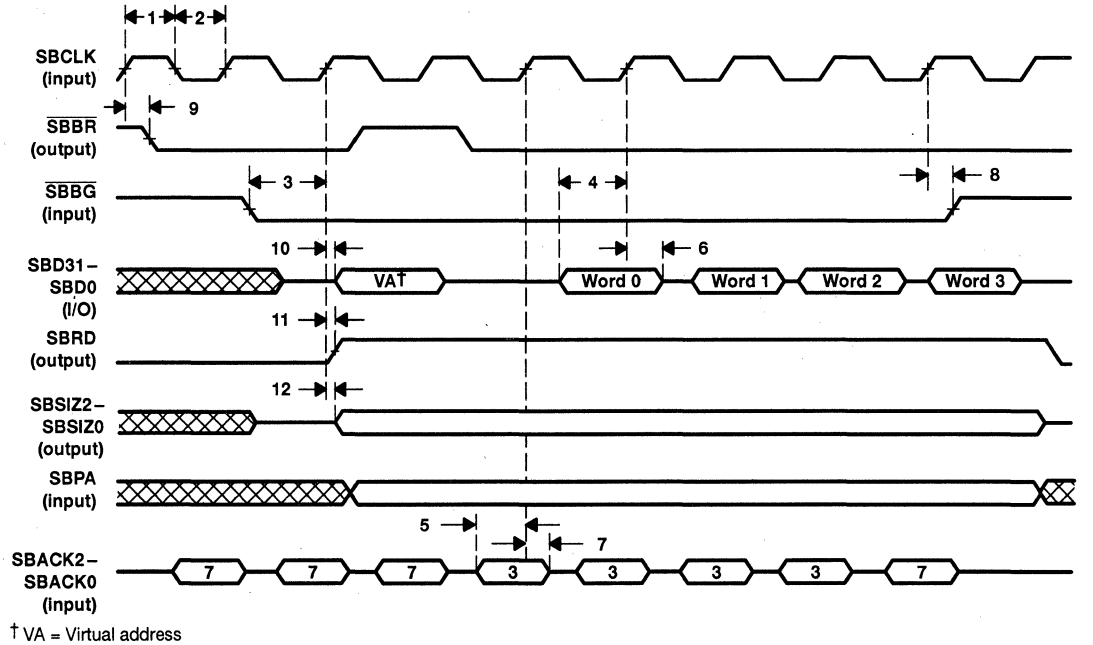
timing requirements (see Figure 4)

NO.			MIN	MAX	UNIT
1	$t_{w(SBCLKH)}$	Pulse duration, SBCLK high	17		ns
2	$t_{w(SBCLKL)}$	Pulse duration, SBCLK low	17		ns
3	$t_{su(SBBG)}$	Setup time, $\overline{SBBG}$ low before SBCLK↑	15		ns
4	$t_{su(SBD)}$	Setup time, SBD31–SBD0 valid before SBCLK↑	15		ns
5	$t_{su(SBACK)}$	Setup time, SBACK2–SBACK0 valid before SBCLK↑	15		ns
6	$t_{h(SBD)}$	Hold time, SBD31–SBD0 valid after SBCLK↑	0		ns
7	$t_{h(SBACK)}$	Hold time, SBACK2–SBACK0 valid after SBCLK↑	0		ns
8	$t_{h(SBBG)}$	Hold time, $\overline{SBBG}$ low after SBCLK↑	0		ns

operating characteristics (see Figure 4)

NO.			MIN	MAX	UNIT
9†	$t_{d(SBBR)}$	Delay time, SBCLK↑ to $\overline{SBBR}$↓	2.5	22	ns
10†	$t_{d(SBD)}$	Delay time, SBCLK↑ to SBD31–SBD0 valid	2.5	22	ns
11†	$t_{d(SBRD)}$	Delay time, SBCLK↑ to SBRD↑	2.5	22	ns
12†	$t_{d(SBSIZ)}$	Delay time, SBCLK↑ to SBSIZ2–SBSIZ0 valid	2.5	22	ns

† Numbers are given for SBus clock frequency of 25 MHz.



† VA = Virtual address

Figure 4. TNETA1560 Read Operation (TNETA1560 as Master in This Burst Transfer)

timing requirements (see Figure 5)

NO.			MIN	MAX	UNIT
1	$t_{su(SBD)}$	Setup time, SBD31–SBD0 valid before SBCLK↑	15		ns
2	$t_{su(SBRD)}$	Setup time, SBRD high before SBCLK↑	15		ns
3	$t_{su(SBSIZ)}$	Setup time, SBSIZ2–SBSIZ0 valid before SBCLK↑	15		ns
4	$t_{su(SBPA)}$	Setup time, SBPA valid before SBCLK↑	15		ns
5	$t_{su(SBSEL)}$	Setup time, $\overline{\text{SBSEL}}$ low before SBCLK↑	15		ns
6	$t_{su(SBAS)}$	Setup time, $\overline{\text{SBAS}}$ low before SBCLK↑	15		ns
7	$t_{h(SBD)}$	Hold time, SBD31–SBD0 valid after SBCLK↑	0		ns
8	$t_{h(SBSIZ)}$	Hold time, SBSIZ2–SBSIZ0 valid after SBCLK↑	0		ns
9	$t_{h(SBPA)}$	Hold time, SBPA valid after SBCLK↑	0		ns
10	$t_{h(SBSEL)}$	Hold time, $\overline{\text{SBSEL}}$ low after SBCLK↑	0		ns

operating characteristics (see Figure 5)

NO.			MIN	MAX	UNIT
11†	$t_{d(SBACK)}$	Delay time, SBCLK↑ to SBACK2–SBACK0 valid	2.5	22	ns

† Numbers are given for SBus clock frequency of 25 MHz.

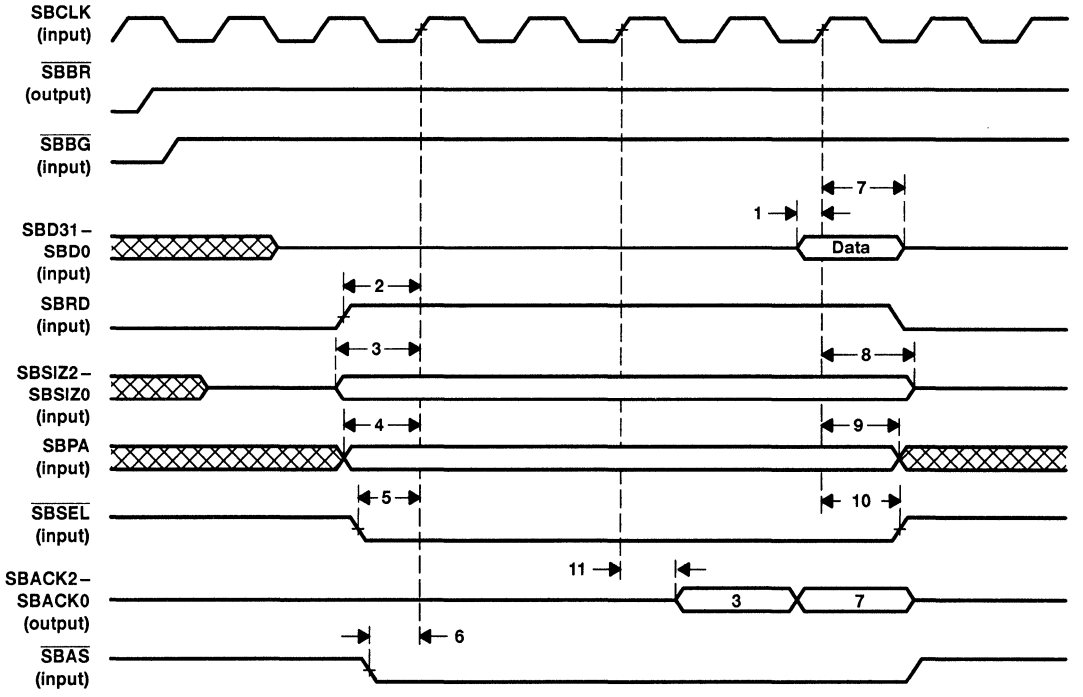


Figure 5. TNETA1560 Read Operation (TNETA1560 as Slave)

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timing requirements (see Figure 6)

NO.			MIN	MAX	UNIT
1	$t_{su(SBRD)}$	Setup time, SBRD low before SBCLK↑	15		ns
2	$t_{su(SBSIZ)}$	Setup time, SBSIZ2–SBSIZ0 valid before SBCLK↑	15		ns
3	$t_{su(SBPA)}$	Setup time, SBPA valid before SBCLK↑	15		ns
4	$t_{su(SBSEL)}$	Setup time, $\overline{\text{SBSEL}}$ low before SBCLK↑	15		ns
5	$t_{su(SBAS)}$	Setup time, $\overline{\text{SBAS}}$ low before SBCLK↑	15		ns
6	$t_{h(SBSEL)}$	Hold time, $\overline{\text{SBSEL}}$ low after SBCLK↑	0		ns
7	$t_{h(SBAS)}$	Hold time, $\overline{\text{SBAS}}$ low after SBCLK↑	0		ns
8	$t_{h(SBPA)}$	Hold time, SBPA valid after SBCLK↑	0		ns

operating characteristics (see Figure 6)

NO.			MIN	MAX	UNIT
9	$t_{d(SBD)}$	Delay time, SBCLK↑ to SBD31–SBD0 valid	2.5	22	ns
10	$t_{d(SBACK)}$	Delay time, SBCLK↑ to SBACK2–SBACK0 valid	2.5	22	ns

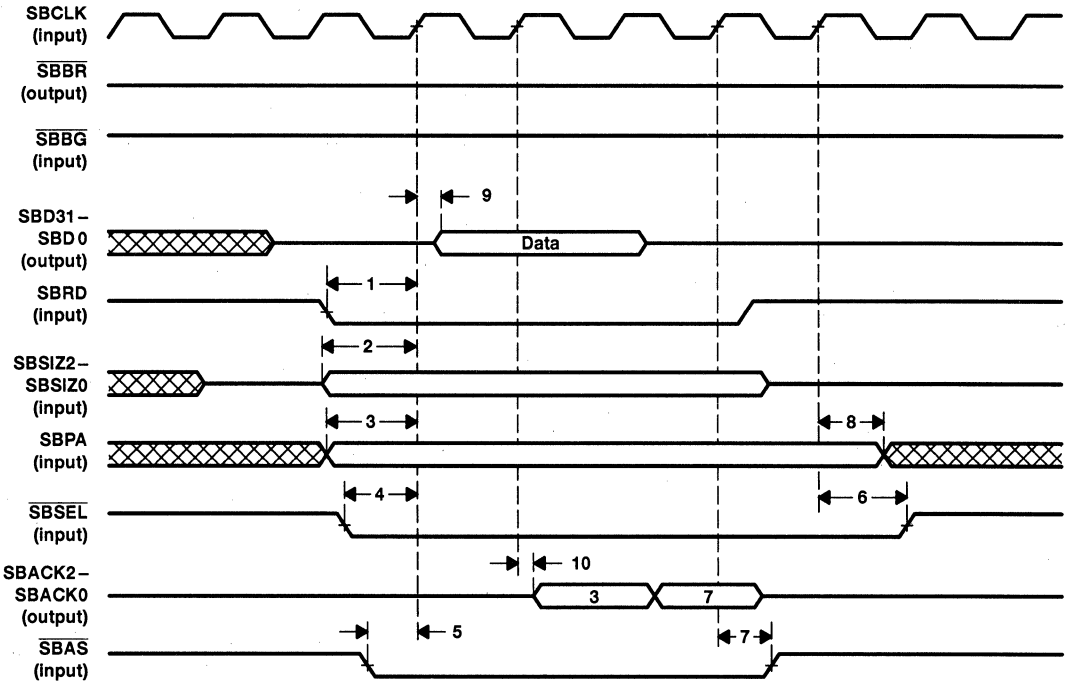

Figure 6. TNETA1560 Write Operation (TNETA1560 as Slave)

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operating characteristics (see Figure 7)

NO.			MIN	TYP	MAX	UNIT
1	$t_{d(LBPHYCS)1}$	Delay time, $\overline{LBRD}\downarrow$ to $\overline{LBPHYCS}\downarrow$		7		ns
2	$t_{d(LBPHYCS)2}$	Delay time, LBADDR15 – LBADDR0 valid to $\overline{LBPHYCS}\downarrow$		7		ns
3	$t_{d(LBREADY)1}$	Delay time, $\overline{LBPHYCS}\downarrow$ to $\overline{LBREADY}\downarrow$		17		ns
4	$t_{d(LBD)1}$	Delay time, $\overline{LBPHYCS}\downarrow$ to LBD7–LBD0 valid		16		ns
5	$t_{d(LBD)2}$	Delay time, $\overline{LBPHYCS}\uparrow$ to LBD7–LBD0 invalid		11		ns
6	$t_{d(LBREADY)2}$	Delay time, $\overline{LBPHYCS}\uparrow$ to $\overline{LBREADY}\uparrow$		9		ns
7	$t_{d(LBADDR)}$	Delay time, $\overline{LBPHYCS}\uparrow$ to LBADDR15 – LBADDR0 invalid		2		ns

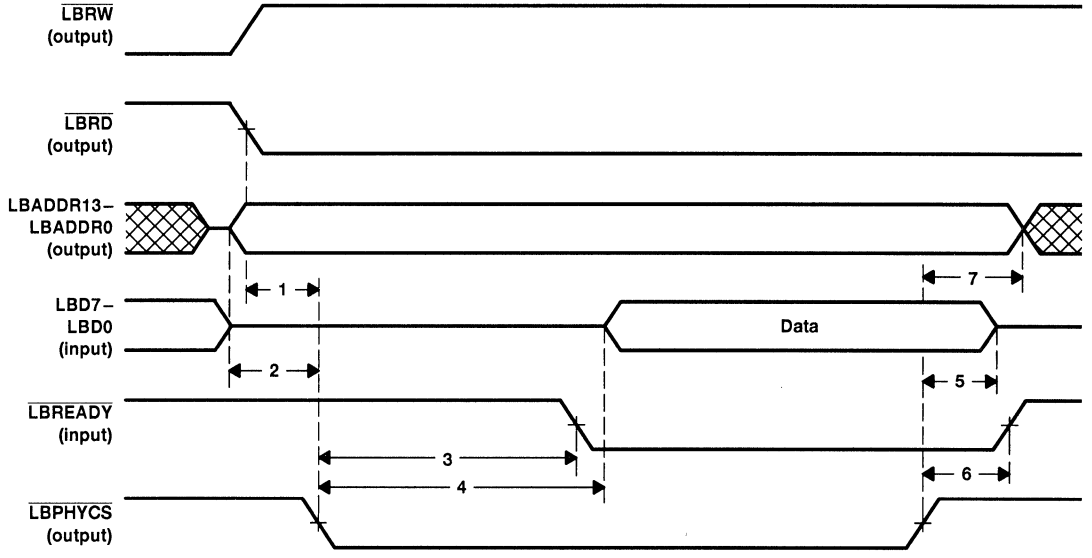

Figure 7. Local-Bus-Interface Read Operation (TNETA1560 as Slave)

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operating characteristics (see Figure 8)

NO.			MIN	TYP	MAX	UNIT
1	$t_{d(LBPHYCS)1}$	Delay time, $\overline{LBRW}\uparrow$ to $\overline{LBPHYCS}\downarrow$		7		ns
2	$t_{d(LBPHYCS)2}$	Delay time, LBADDR15–LBADDR0 valid to $\overline{LBPHYCS}\downarrow$		7		ns
3	$t_{d(LBPHYCS)3}$	Delay time, LBD7–LBD0 invalid to $\overline{LBPHYCS}\uparrow$		7		ns
4	$t_{d(LBPHYCS)4}$	Delay time, LBADDR15–LBADDR0 invalid to $\overline{LBPHYCS}\uparrow$		6		ns

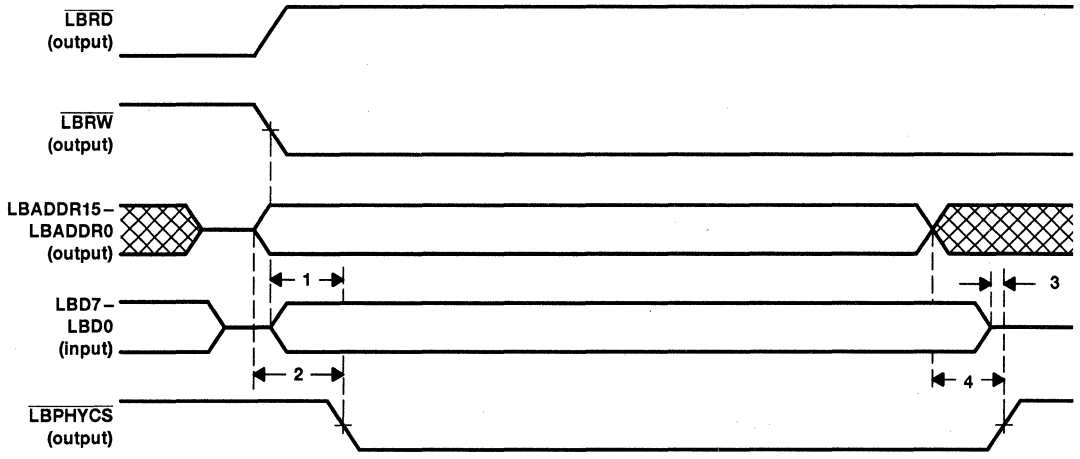

Figure 8. Local-Bus-Interface Write Operation (TNETA1560 as Slave)

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operating characteristics (see Figure 9)

NO.			MIN	MAX	UNIT
1	$t_{w(CMR/WL)}$	Pulse duration, CMR/$\overline{W}$ low			ns
2	$t_{d(CMR/W)1}$	Delay time, CMADDR13–CMADDR0 valid to CMR/$\overline{W}\downarrow$			ns
3	$t_{d(CMR/W)2}$	Delay time, CMD31–CMD0 valid to CMR/$\overline{W}\uparrow$			ns
4	$t_{d(CMD)}$	Delay time, CMR/$\overline{W}\uparrow$ to CMD31–CMD0 invalid			ns

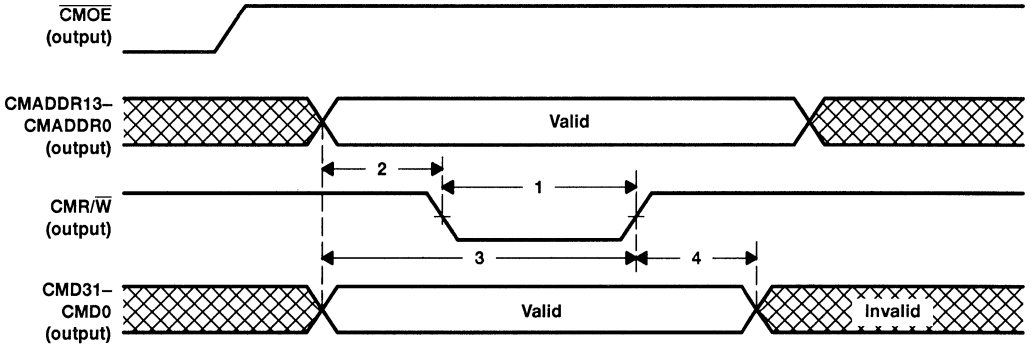

Figure 9. Control-Memory-Interface Write Operation

timing requirements (see Figure 10)

NO.			MIN†	MAX	UNIT
1	$t_{su(CMD)}$	Setup time, CMD31–CMD0 valid before $\overline{CMOE}\uparrow$			ns
2	$t_{h(CMD)}$	Hold time, CMD31–CMD0 valid after $\overline{CMOE}\uparrow$			ns

† These numbers are for a 20-ns asynchronous SRAM control memory.

operating characteristics (see Figure 10)

NO.			MIN	MAX	UNIT
3	$t_{d(CMOE)}$	Delay time, CMADDR13–CMADDR0 valid to $\overline{CMOE}\downarrow$			ns

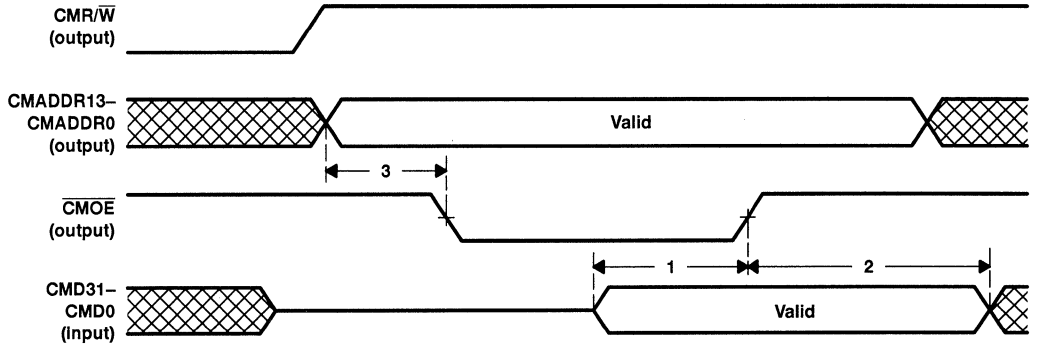

Figure 10. Control-Memory-Interface Read Operation

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PRINCIPLES OF OPERATION

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functional overview

SBus SAR refers to an SBus device (TNETA1560) that provides an ATM interface. The device provides an interface to SBus, ATM adaptation layer processing, ATM SAR processing for full-duplex ATM at the STS-3c rate of 155.52 Mbit/s, and the controls for the register interface on the physical (PHY) layer. Figure 11 shows a typical connection to the SBus SAR in an adaptor-card application.

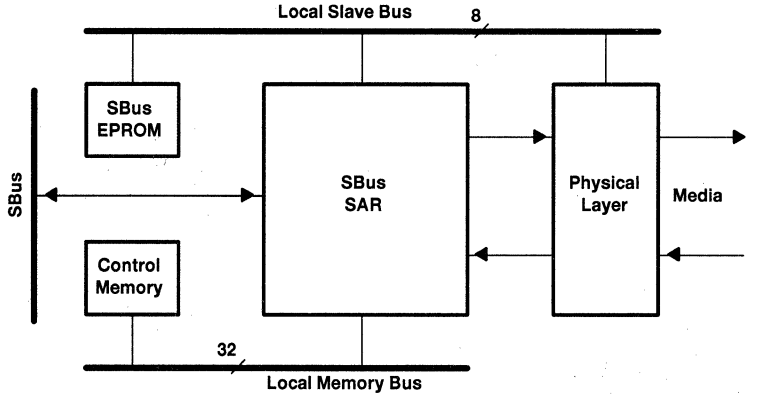

Figure 11. SBus SAR External Connections

The SBus SAR provides a packet interface managed by descriptor rings, making the 53-byte ATM framing format transparent to the user. The device passes the 48-byte payload of each cell across the SBus. All packets are stored in host memory and accessed by the chip via the descriptor-ring mechanism.

The SBus SAR generates data in the transmit direction via a special bit-rate control table that provides explicit cell-level interleaving between groups of VCs. This mechanism provides a high degree of flexibility in specifying peak rates for each group, up to 155.52 Mbit/s at a resolution greater than 32 kbit/s. VCs within a group are serviced via a FIFO discipline on a per-packet basis.

The SBus SAR supports 1023 unique VCs, typically all associated with virtual path identifer (VPI) 0. The SBus SAR allows multiple VPs with the caveat that each VC is unique. Limited support is provided to recognize ATM layer OAM cells.

The device is primarily intended for ATM adaptation layer type 5 (AAL5) encapsulation and termination, which is fully supported in hardware. Limited support is provided for ATM adaptation layer type 3/4 (AAL3/4) with 48-byte transfers across the SBus interface and hardware recognition of the EOM indicator on the receive side. Finally, a null AAL is also supported to facilitate real-time data transfer.

The interface to the PHY layer consists of an 8-bit-wide data path and associated control signals in both the transmit and receive directions. The 53-byte ATM cells pass between the ATM and PHY layers.

functional overview (continued)

The native clock for the SBus SAR is the SBus clock, which can range between 16.67 MHz and 25 MHz. The 8-bit-wide data path on the PHY-layer receive interface requires a clock rate of at least 19.44 MHz when interacting with a 155.52 Mbit/s PHY-layer. The PHY-layer receive interface uses the the PHY-layer clock. The native word size for the device is 32 bits, corresponding to the data-bus width for SBus.

glossary and conventions

This section presents several special terms and conventions used throughout this document. It is not a complete list of abbreviations.

transmit direction

The direction of data flow from SBus to the ATM PHY layer

receive direction

The direction of data flow from ATM PHY-layer to SBus

two's-complement value

A number in two's complement is given by (0 – actual positive value) modulo (2^n), where n is the number of bits in the field.

GFC

Generic flow control field. Appears in the upper four bits of the ATM cell header at the UNI.

EOM

End of message

EOP

End of packet

NCE

Network control engine

functional description

packet interface

The SBus SAR uses host memory to store the 48-byte payload units that constitute a packet in both the transmit and receive directions. The device initiates the 48-byte data transfers containing packet data over the SBus for both transmit and receive operations. The packet does not include AAL5 encapsulation while in host memory. This is provided by the SBus SAR. The buffering within the device is limited to that required to match the ATM-PHY transfer protocol to the transaction-oriented SBus transfer protocol. The chip contains an 8-cell transmit FIFO and a 32-cell receive FIFO.

Each packet queued for transmission may be distributed across multiple buffers in host memory with each starting at any byte boundary. This is supported in hardware by the device. Each received packet is placed in a single buffer in host memory (either small or big) aligned to a 16-byte boundary.

PRINCIPLES OF OPERATION

bandwidth group (BWG) table mechanism

The SBus SAR generates data via a special bit-rate control table known as the BWG table. Each BWG consists of one or more virtual circuit identifiers (VCIs), and each VCI is served via a FIFO discipline on a per-packet basis. Each entry in the BWG table consists of an 8-bit BWG index, and BWGs are serviced based on the composition of the BWG table. The size of the BWG table is programmable with a maximum of 4800 entries, organized as 1200 words, to provide a resolution greater than 32 kbit/s (see Figure 12).

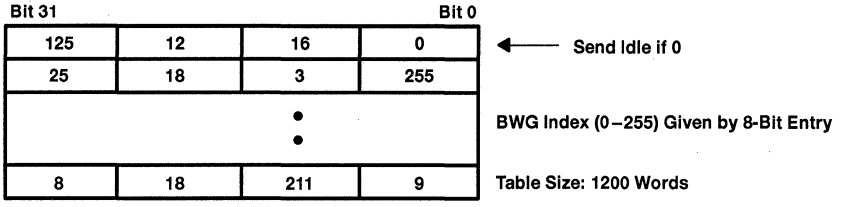

Figure 12. BWG Table

AAL-type processing

The SBus SAR supports various types of AAL processing. AAL3/4, AAL5, null-AAL, GFC, and OAM processing are described in this section.

AAL3/4 processing

Since 48 bytes are provided across the SBus interface, all AAL3/4 packet data processing is performed by the host in software. AAL5 processing is disabled on VCIs using AAL3/4. The AAL3/4 EOM indicator, which is located in the first byte of the ATM payload (see Figure 13), is recognized in hardware, initiating an interrupt to the host.

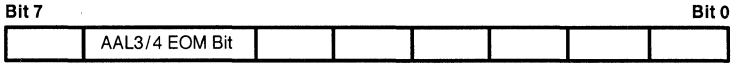

Figure 13. AAL3/4 Processing

AAL5 processing

The primary support is for AAL5 with encapsulation in the transmit direction and termination in the receive direction. AAL5 packets are converted to cells by the SBus SAR before delivery to the PHY layer. Similarly, the device recovers 53-byte ATM cells from the PHY layer before it performs AAL5 termination.

The SBus SAR adds the pad, the control/length field, and the cyclic redundancy check (CRC) for transmit packets. The SBus SAR does not interpret the field length in the AAL5 frame in the receive direction; therefore, the entire AAL5 packet is forwarded to host memory allowing the driver to remove the correct payload. This also allows the host to examine the control field in software, necessary in a time of evolving standards in this area. The device performs CRC checks in the receive direction and indicates EOP processing to the host based on the EOP indication in AAL5.

null-AAL processing

Null-AAL processing uses the same mechanism as the AAL3/4 in the transmit direction to disable AAL5 processing. The control entry associated with each BWG (VCI) in the receive direction has an entry to indicate an interval defined in units of cells received. The SBus SAR then provides an interrupt to the host when the number of cells received on the VCI is equal to that indicated by the table entry. This counter is reset after each interrupt (at the end of each interval). This interval is also referred to as a packet, although it does not encapsulate a well-defined unit of information.

PRINCIPLES OF OPERATION

high-order VPI/ VCI bits GFC processing

The lower ten bits of the VCI are used to encode the 1023 possible VCIs. VCI 0 is not used since it indicates unassigned cells. The upper-order bits of the VCI and the VPI field are programmable on a per-VC basis on transmit. The GFC field is always set to zero.

The upper-order bits of the VCI, the VPI field, and the GFC field are ignored on all cells that are received. These cells pass to the SBus SAR if the header error control (HEC) field is correct, the upper-order bits of the header are set intentionally, or the cell is misrouted. The probability of misrouting is small and such an event would be detected via the CRC check in AAL5. The advantage of this scheme is that any VPI/VCI combination is supported if the lower ten bits of the VCI are unique.

OAM processing

ATM-layer OAM processing does not require any real-time intervention and is processed in software. OAM cells received on the link must be identified by the device. Table 1 summarizes ATM-layer OAM encoding as described by various standards bodies.

Table 1. ATM-Layer OAM Encoding

NO.	ITEM	VCI	PTI
1	VP level: link-associated OAM cell	3	—
2	VP level: end-to-end OAM cell	4	—
3	VC level: link-associated OAM cell	Any	4
4	VC level: end-to-end OAM cell	Any	5

Each OAM cell forms a fully encapsulated packet. ATM-layer OAM cells transcend AAL protocols and are recognized differently. The end system recognizes all four ATM-layer OAM flows. OAM cells received in VCI 3 and 4 do not interfere with the normal data stream. The only special processing necessary is to initiate EOP processing for each cell. The software drivers must configure VCI 3 and 4 as null-AAL channels with a packet length equal to one cell in the receive direction. OAM cells are transmitted as null-AAL packets with length equal to one cell. VC-level OAM cells are specially interpreted. They are diverted to receive direct-memory access (DMA)
channel 0 and the 4-byte ATM header is passed on to a receive-completion ring in host memory during normal EOP processing.

transmit descriptor rings and DMA

Each transmit BWG is supported by a corresponding DMA channel and its own descriptor ring. The SBus SAR supports 255 BWGs, 255 descriptor rings, and 255 DMA channels in the transmit direction. BWG 0 represents null, indicating that an idle cell should be transmitted. This limits the number of packets and VCs active simultaneously in the transmit direction to 255.

Each descriptor ring holds up to 256 entries corresponding to 256 buffers that may be queued for transmission in the ring. The total number of buffers that can be queued for transmission by the device is 64K. The buffers within a descriptor ring (each BWG) are serviced in FIFO order on a per-buffer basis. Each packet consists of one or more byte-aligned buffers in host memory.

Each descriptor-ring entry contains a control bit that indicates whether a buffer is queued for transmission. The DMA entry for each BWG contains a pointer to the first item in the queue in the corresponding descriptor ring. An idle cell is transmitted if the control bit in the next entry of the descriptor ring indicates an inactive entry.

A field in each DMA entry allows the BWG to be disabled by the host. This may be used by the host to respond to back-pressure mechanisms in software.

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receive free-buffer rings and DMA

The SBus SAR uses buffer pointers from two free-buffer rings to place incoming packets in the host memory. These are called small free-buffer ring and the big free-buffer ring. Each receive BWG has a control bit indicating the type of buffer it uses: small or big. BWGs are unable to preallocate buffers for the next packet, which prevents user processes from managing their own buffer space.

The SBus SAR supports 1023 receive DMA channels and 1023 VCs. The incoming VCI indexes the receive DMA channels directly. BWG 0 is reserved to process special information for OAM cells. The drivers must configure VCI 0 as a null-AAL VCI with a packet length equal to one cell.

completion rings

The SBus SAR indicates completion of packet processing in either direction to the host via an interrupt and by posting entries to receive- and transmit-completion rings. Each completion ring accepts up to 256 entries. A control bit in each entry of the completion ring prevents the device from overwriting an entry that has not been processed by the host.

packet-size restrictions

The SBus SAR supports a maximum packet size of 64K bytes in either direction. The maximum buffer size for transmit is also 64K bytes.

SBus interaction and burst-transfer size requirements

The SBus SAR behaves both as an SBus direct virtual memory access (DVMA) master and as a slave. Table 2 classifies the interaction between the device and SBus into seven groups. This also quantifies the support required from the DMA controller on the host machine.

Table 2. SBus Transactions

NO.	TRANSACTION TYPE	SAR ROLE	TRANSFER SIZE	ACK. SIZE
1	Host accesses SAR registers or control memory	Slave	Word	Word
2	Host accesses PHY-layer registers	Slave	Word	Word
3	Host accesses EPROM	Slave	Byte/Word	Byte
4	SAR transmits control-information transactions and receives free-buffer ring transactions	Master	Word	Word
5	SAR receive completion-ring entries posted to the host	Master	4 Word	4 Word
6	SAR cell-payload transfers (default)	Master	8, 4, and 1 Word	8, 4, and 1 Word
7	SAR cell-payload transfers (NCE)	Master	4 Word	4 Word

It is efficient to transfer the 48-byte payload via successive transfers of 32 and 16 bytes if the data is on even burst boundaries. This is the algorithm followed by the SAR in the default mode for all transfers on receive and for all transfers on transmit except those on buffer boundaries.

The NCE is based on a SPARCstation 1+ platform that does not support 32-byte bursts. A configuration register bit on the SBus SAR programmed by the host is set to indicate that the platform is the NCE or any system that does not support 32-byte bursts. The device then uses 16-byte bursts exclusively to transfer cell-payload data in each direction.

Since there is at least a 4-cycle overhead associated with each transfer for a DVMA master, the number of cycles required to transfer a cell in the default mode in either direction with no overhead for packet processing is at least 20 SBus cycles. The time to transfer the 48-byte cell payload on the NCE in either direction is at least 24 SBus cycles.

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SBus interaction and burst-transfer size requirements (continued)

Burst transfers in the transmit direction are optimized to yield the fewest SBus cycles based on buffer, packet, cell boundaries, and their location in host memory.

commands, registers, and interrupts

The SBus SAR has several internal registers for configuration and storage of operational state information. The information contained in the registers is described in a later section.

The SAR generates an interrupt, connected on the adapter to SBus interrupt request terminal, on packet completion and on a variety of error conditions.

PHY data interface

The ATM-cell-transfer rate is full-duplex 149.76 Mbit/s, but data may arrive in bursts at 155.52 Mbit/s due to the framing scheme described by the PHY layer. A clock rate of at least 19.44 MHz is essential in the receive direction to prevent cell loss due to buffer overflow in the PHY layer. The SBus SAR decouples the SBus clock from the ATM clock in the receive direction via an asynchronous FIFO memory, which holds up to 32 cells. The SAR transmits data to the PHY layer at the SBus clock rate.

PHY-layer control interface

Figure 11 shows that the local bus is used to connect the SBus EPROM to the register interface on the PHY-layer device.

interfaces

The terminal layout and the terminal functions table fully describe the terminal assignments and functions of the Sbus SAR (TNETA1560).

SBus interface

The SBus SAR behaves both as an SBus DVMA master and slave. The SBus SAR is selected as the slave if the $\overline{\text{SBSEL}}$ signal is asserted. The system accesses the control-memory block, the local bus, and the user registers with SBus slave accesses to the SAR. The transfer size is determined by SBSIZ2 – SBSIZ0, which must be set to 000 to represent a one-word transfer. The physical address is given by the SBPA signals and must fall within the ranges specified in Table 2. The SBus SAR generates an error acknowledgment given by SBACK2 – SBACK0 set to 110 if either of these two conditions is violated. The $\overline{\text{SBAS}}$ signal is used as described in the SBus specification, and the SBRD signal indicates a read or write operation. Finally, SBACK2 – SBACK0 are set to 011 to indicate SBus word acknowledgment for operations on the SAR registers and control memory; SBACK2 – SBACK0 are set to 101 to indicate SBus byte acknowledgment on local-bus operations.

The SBus SAR can initiate transactions as master only when no slave transactions are active. The SAR asserts the dedicated $\overline{\text{SBBR}}$ signal to request an operation as the SBus master. The SBus controller asserts the SAR dedicated $\overline{\text{SBBG}}$ signal making the SAR the master. The SAR sets the SBSIZ2 – SBSIZ0 signals to indicate a 1-word, 16-byte, or 32-byte transfer, the SBRD signal indicates a read or write operation, and the DVMA address is placed on the SBD31 – SBD0 lines. The TNETA1560 monitors the SBACK2 – SBACK0 lines anticipating the appropriate acknowledgment value. The SBus SAR considers either an error acknowledgment on the SBACK2 – SBACK0 lines or a late error on the $\overline{\text{SBLERR}}$ line as a fatal error, disables all data-transfer processing, and generates a SBus interrupt via the $\overline{\text{SBIRQ}}$ signal.

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control-memory interface

The control memory is set up in a 16K × 32 configuration with the cycle time given by the SBus clock. The interface is designed for an asynchronous SRAM with a 32-bit data bus, a 14-bit address bus, a CMR/$\overline{W}$ signal determine read or write, and an output-enable signal ($\overline{CMOE}$).

PHY-layer interface

The SBus SAR generates a transmit clock at the SBus frequency and a 19.44-MHz receive clock. The transmit clock sent to the PHY layer is an inverted version of the internal clock. This ensures that all setup and hold-time restrictions are met. The receive clock sent to the PHY layer is equivalent to the internal clock.

The SBus SAR generates output data along with a start-of-cell indicator in the transmit direction. This data is sent at the rate of the SBus clock. The PHY layer can respond with a full signal, which is asserted at least four cycles before any internal buffers are full. The SAR then turns off the transmit-enable signal until the full signal is deasserted. The PHY layer sends a start-of-cell indicator with output data. The empty signal acts as an inverted enable signal on this interface.

The PHY-layer interrupt signal is directly connected to the SBus interrupt signal; therefore, the SBus interrupt is asserted when the PHY-layer interrupt signal is asserted.

local-bus interface

Since there could be several devices on the local bus, the SBus SAR accepts a ready signal from devices on the bus as a handshake. The bus transaction is assumed to be complete eight SBus cycles (at least 320 ns) after the transaction is initiated, regardless of the ready signal. This accommodates slow devices such as EPROMs and also can be used to relax timing constraints on the register interface for the PHY-layer devices.

The local bus is accessed exclusively via SBus transactions with the SAR as the slave with the exception of the local-bus interrupt signal. The lower 16 bits of the SBus address bus are directly routed to the local-bus (LBus) address bus. The SBus address must remain stable while the local bus is active. This is achieved by not returning an acknowledgment signal on SBus until the LBus transaction is complete.

PRINCIPLES OF OPERATION

architecture

Figure 14 depicts a data-flow representation of the SBus SAR architecture.

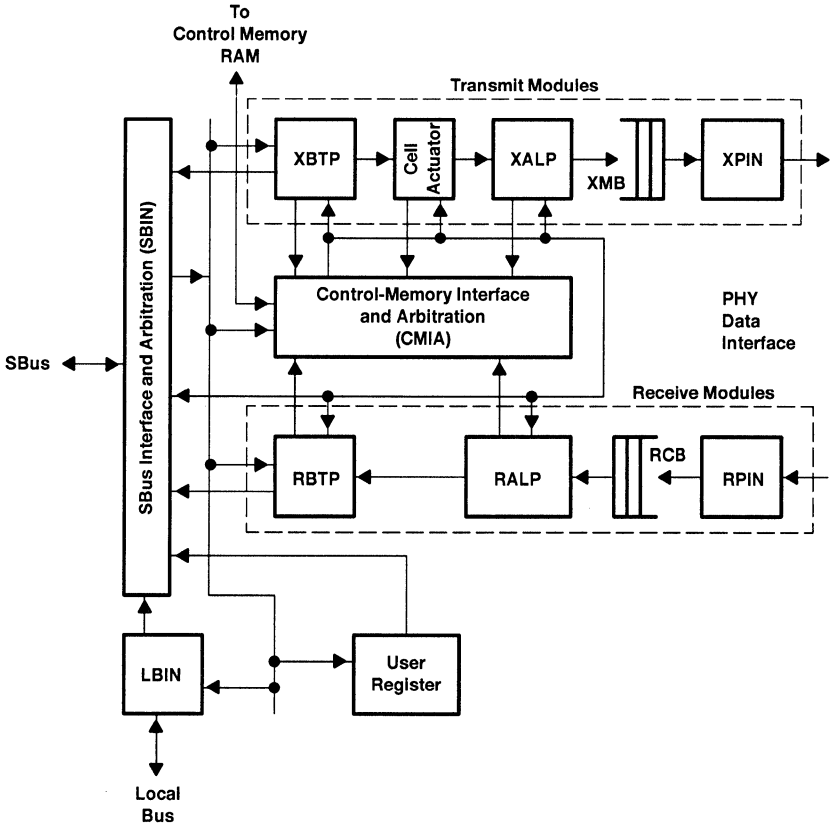

Figure 14. SBus SAR Architecture

transmit modules

The transmit host and buffer transaction processor (XBTP) is responsible for all host-related functions on the transmit side and requests 16- and 32-byte transfers from the SBus-interface block. The cell actuator accesses the BWG table and determines the next VC to be serviced. The transmit adaptation layer processor (XALP) processes all AAL-related functions and adds the four bytes of the ATM header to each cell. The XALP identifies the AAL5 CRC and determines if it should be appended to the packet. The transmit buffer (XMB) is an 8-cell buffer that receives 13 words per cell. Idle cells are also placed in this buffer. The transmit PHY interface (XPIN) does word-to-byte unpacking and interacts with the PHY layer using the SBus clock.

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receive modules

The receive PHY interface (RPIN) performs byte-to-word packing, filters idle cells, and interacts with the PHY layer using the system's PHY-layer clock crystal. The receive buffer (RCB) performs rate synchronization from the PHY-layer clock to the SBus clock and buffers up to 32 cells. The receive ATM processor (RAT) and the receive ATM adaptation layer processor (RALP) operate in parallel and are part of the same module. The RALP terminates the AAL5 CRC and processes various EOP indicators. The RAT block is responsible for deleting the ATM header and accessing the correct receive DMA entry. Finally, the receive host and buffer transaction processor (RBTP) performs all host-specific functions on the receive side.

SBus interface module

The SBus interface module (SBIN) is responsible for implementing the details of the SBus protocol. The XBTP and the RBTP are the only two modules that require SBus transactions involving the SAR as a master; therefore, SBIN arbitrates between requests from the two blocks. The SAR is the SBus slave when the host accesses control memory, the local bus, or the user registers internal to the SAR.

control-memory interface and arbitration

The control-memory interface and arbitration (CMIA) block performs memory arbitration for all the blocks that access control memory. Since each access is a 1-word access, no module can hold up the memory for a long time. CMIA imposes a strict priority mechanism and services various blocks in the following order: RALP, XALP, cell actuator, RBTP, SBTP, SBIN.

local bus-interface module

The local bus-interface (LBIN) module is used to access the EPROM and the registers on the PHY-layer device.

user register

The user-register block stores a number of configuration and operational registers. The user registers also generate SBus interrupts on packet completion or when an error condition is detected.

data management

The SAR architecture uses two memory subsystems: host memory and on-board control memory. The control memory provides fast multichannel memory-based DMA channels and a temporary storage area used as virtual auxiliary registers. Some transmit and receive data-management components reside in control memory for immediate access to critical real-time events isolated from host memory, which is tied to SBus latency. The AAL5 CRC is also encapsulated in the control memory. The control memory is accessible by the host for initialization and monitoring the hardware and network status. Figure 15 shows the organization of the SAR data structures across control and host memory.

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data management (continued)

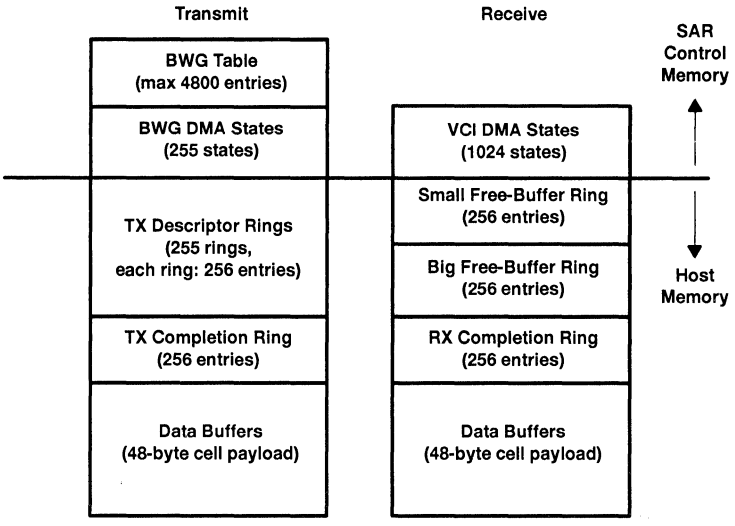

Figure 15. SBus SAR Data Organization

Several registers stored in the control memory indicate the address of the next entry in the two free-buffer rings and the two completion rings. The descriptor rings apply to packet- or buffer-level processing, whereas the DMA channels apply to per-cell processing. The transmit DMA state for each BWG indicates the location of each transmit-descriptor ring.

programmer's reference

This section presents the SBus SAR data structures in detail. The contents of various physical locations are summarized in Table 3. A large part of this information is presented in Figure 15 but is duplicated here for convenience.

Table 3. Location of SBus SAR Data Structures

CONTROL MEMORY	HOST MEMORY	SAR REGISTERS	EPROM
BWG table	TX descriptor rings (255)	Configuration registers	Boot code
TX DMA states	TX completion ring	Operation registers	48-bit address
RX DMA states	Small free-buffer ring		Diagnostics
Initialization block	Big free-buffer ring		SBus ID
	RX completion ring		
	Data buffers		

The system has a bus width of four bytes and all transactions are conducted on 4-byte boundaries. The SBus SAR uses big-endian addressing by definition as an SBus device. All addresses are in hexadecimal notation unless otherwise specified.

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programmer's reference (continued)

Each descriptor ring has 256 entries as shown in Figure 15. Each descriptor-ring entry consists of four words. Each descriptor ring is aligned to a 4K-byte boundary in host memory with each entry aligned to a 16-byte boundary. The SAR has two receive free-buffer rings, one transmit completion ring, and one receive completion ring. The current pointer to each of these rings is stored in the initialization block in SAR control memory. An entry in each transmit DMA channel points to one of the 255 transmit-descriptor rings in host memory.

Each DMA-channel entry consists of eight words and is located in control memory. The DMA entries on both transmit and receive have an OWN bit that is set when the DMA channel is active. The descriptor-ring entries, the completion-ring entries, and the free-buffer ring entries have an OWN bit that is set when the entry belongs to the SAR.

control-memory map and access

Table 4 shows a control-memory map. The address bus to memory is 14 bits wide. The physical SBus offset address on the SAR for control memory is C00000 hex. All SBus accesses to control are 1-word accesses at word boundaries.

Table 4. Control-Memory Map

MEMORY REGIONS	CONTROL-MEMORY BASE POINTERS (hex)	SBus PHYSICAL ADDRESS (hex)
Initialization block	0000	C00000
Transmit BWG 0 – 255 – DMA block	0100	C00400
BWG table (1200 words, 4800 entries)	0900	C02400
Receive BWG/VCI 0 – 1023 – DMA block	1000	C04000

initialization block

The initialization block contains exactly four entries and resides in control memory. Table 5 shows the configuration of the initialization block.

Table 5. Initialization Block

SBus PHYSICAL ADDRESS (hex)	CONTROL-MEMORY ADDRESS (hex)	BITS 27 – 8	BITS 7 – 0
C00000	0000	TX completion-ring offset pointer	Index 0 – 255
C00004	0001	RX completion-ring offset pointer	Index 0 – 255
C00008	0002	Small free-buffer-ring offset pointer	Index 0 – 255
C0000C	0003	Big free-buffer-ring offset pointer	Index 0 – 255

The pointers are mapped to SBus DVMA addresses by appending the lower-order four bits representing the offset within each 16-byte descriptor-ring entry. Since accesses are only permitted on a word basis, the lower-order two bits are always set to zero.

PRINCIPLES OF OPERATION

transmit-data descriptor rings

Each of the 255 transmit-data descriptor rings holds 256 entries and each ring represents one transmit packet queued for transmission. A packet is composed of one or more transmit buffers. The host posts entries to the rings and the SAR processes each entry within the given ring. Table 6 shows the composition of the four-word entry.

Table 6. Transmit-Data Descriptor-Ring Summary

ENTRY	DESCRIPTION
Word 0	Control field, packet length, buffer length
Word 1	Start-of-buffer pointer – 32 bits
Word 2	4-byte ATM header
Word 3	AAL5 tail – control and length fields

TX descriptor-ring word 0 – configuration

Control (bits 31 – 27)	Packet length (bits 26 – 16)	Buffer length (bits 15 – 0)

OWN (bit 31)

The descriptor is owned by the SBus SAR when the OWN bit is set. The descriptor is owned by the host when the OWN bit is zero. The OWN bit is set by the host when a buffer/packet is queued for transmission. When the next BWG index from the BWG table does not have an active buffer location in the transmit DMA entry, the SBus SAR attempts to recover a new-buffer descriptor entry from the transmit-data descriptor ring. This entry is loaded into the DMA entry if the OWN bit is set. If the OWN bit for the first descriptor in the transmit-data descriptor ring is zero, no data is queued for transmission and an idle cell is transmitted.

The host places all the buffers for a packet in the descriptor ring before setting the OWN bits on the entries representing each buffer in sequence from the last buffer to the first buffer (in reverse order). The SBus SAR clears the OWN bit after if finishes transmitting/processing the bytes associated with the buffer pointed to by the DMA entry. When the OWN bit is cleared by the host, word 0 is not meaningful and is overwritten by the host.

start of chain (SOC) (bit 30)

The SOC bit indicates that this is the first buffer of a packet, which consists of one or more buffers. This bit is also set in packets with single buffers.

end of chain (EOC) (bit 29)

The EOC bit indicates that this is the last buffer of a packet. Single buffer packets have both the SOC and EOC bits set. Packets with multiple buffers have the SOC bit set on the first buffer and the EOC bit set on the last buffer.

AAL type – AAL5 indicator (bit 27)

The AAL-type bit indicates the packet/buffer described in this descriptor-ring entry is an AAL5 packet. When zero, this bit indicates to the SAR that AAL5 processing should be performed in the transmit direction. This includes addition of the pad, the control- and packet-length fields, and the 32-bit CRC. The total size of the AAL5 packet is a multiple of 48 bytes.

The SBus SAR does not perform any packet-level encapsulation similar to that used in AAL5 for either AAL3/4 or the null AAL. The host provides packets correctly formatted into 48-byte cells to the SAR.

PRINCIPLES OF OPERATION

packet length (bits 26 – 16)

The packet-length field is expressed in units of cells in the packet. The host computes the correct number of cells in the packet including the additional cell sometimes needed for AAL5 to accommodate the 8-byte tail. This field represents the value used by the SBus SAR to determine the number of cells in a packet and enable EOP processing.

The field is programmed in two's complement. Incrementing the value by one each time a cell is sent results in zero when the entire packet is transmitted. The maximum size of a packet is 64K bytes; therefore, 11 bits are adequate to describe the largest packet.

Since this is a packet-level field as opposed to one that applies to individual buffers, it is only placed in the first buffer descriptor of a packet in the transmit-data descriptor rings. The DMA channel only updates the packet-length field on a per-packet basis. The packet-length field is general in that it is used for all three AAL modes supported. In each case, the SAR enables EOP processing to notify the host when the EOP is detected on transmit via the packet-length field.

buffer length (bits 15 – 0)

The buffer-length field specifies the number of bytes in the buffer represented by this descriptor-ring entry. The maximum buffer size is 64K bytes, which is the largest packet size and allows an entire packet in one buffer. This field is programmed in two's complement and is equal to zero when all the bytes in a buffer are retrieved by the SAR.

TX descriptor-ring word 1 – start-of-buffer pointer

Byte-aligned start-of-buffer pointer (bits 31 – 0)

The start-of-buffer pointer is 32 bits. Each buffer can be aligned on byte boundaries.

TX descriptor-ring word 2 – ATM header

PTI2 (bits 31 – 29)	CLP2 (bit 28)	VPI (bits 27 – 20)	VCI (bits 19 – 4)	PTI1 (bits 3 – 1)	CLP1 (bit 0)

Word 2 contains the 4-byte header for every cell of the packet. The upper-order four bits of the ATM header, representing the GFC at the user-to-network interface (UNI), are set to zero in every outgoing cell. Bits (3 – 0) in word 2 represent the payload-type indicator (PTI) and cell-loss priority (CLP) fields used in every cell of the packet except the last one (the cell that contains the EOP indication). Bits (31 – 28) in word 2 represent the PTI and CLP fields used in the last cell of the packet.

The PTI field in the last cell of an AAL5 packet is set either to 001 or 011. The CLP is programmable and the cell containing the EOP indication can have a different priority level from the other cells. This field is required only in the first descriptor for the packet. In AAL3/4 or null-AAL packets, the PTI and CLP fields in both the upper- and lower-order bits of word 2 are the same.

TX descriptor-ring word 3 – AAL5 control/length

AAL5 control field (bits 31 – 16)	AAL5 length field (bits 15 – 0)

The AAL5 control and length fields apply to packets, not to buffers, and this entry is required only in the first descriptor for the packet. The AAL5 length field is not used to determine the length of the packet during transmit processing. Both fields are placed in the descriptor ring in an AAL5 packet in the proper position (in the four bytes preceding the AAL5 32-bit CRC). These fields are not used if the packet is either an AAL3/4 or a null-AAL packet.

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transmit BWG DMA block

The control memory contains 255 transmit BWG DMA entries, each containing eight words. Table 7 summarizes the contents of each entry.

Table 7. Transmit BWG DMA Entry

ENTRY	DESCRIPTION	STATIC/ DYNAMIC
Word 0	Control field, packet length, buffer length	Dynamic
Word 1	Current-buffer pointer – 32 bits	Dynamic
Word 2	4-byte ATM header	Dynamic
Word 3	Static bits – BWG ON/OFF (BWG_ON bit)	Static
Word 4	BWG data-ring pointer, descriptor pointer	Dynamic
Word 5	BWG cell-counter place holder – not implemented	Dynamic
Word 6	Partial 32-bit packet CRC	Dynamic
Word 7	AAL5 tail – control and length fields	Static

The SBus SAR initiates host transactions affecting the DMA table, except those required for one-time configuration of a channel for normal operation based on cell-transmission opportunities from the BWG table. Each DMA entry represents a buffer under segmentation.

During initialization, the host has to configure word 0, word 3, and word 4 in the transmit DMA states table for each BWG selected for transmission in the BWG table, including the BWG0. These words allow the TNETA1560 to start a transmission of a new packet. After configuration, the TNETA1560 reads word 3 to check if the BWG_ON bit is set. If it is set, the device reads word 0 to determine if the OWN bit is set. When the OWN bit is not set, it indicates that this is the first buffer of a new packet. The TNETA1560 then reads word 4 to obtain a transmit descriptor-ring pointer that indicates the memory address in host memory for the transmit descriptor-ring pointer. The following sections explain each TX DMA table word in detail.

TX DMA word 0 – state/configuration

Control (bits 31 – 27)	Current packet length (bits 26 – 16)	Current buffer length (bits 15 – 0)

The contents of word 0 are copied directly from the corresponding transmit-data descriptor-ring entry at the start of each new buffer. This applies to all the fields in this status word, and the host must ensure consistency across the fields.

OWN (bit 31)

The OWN bit is set when the DMA channel for the BWG is active, and all related state information in the DMA entry is current. The OWN bit indicates a packet is currently being segmented and transmitted for this BWG. This OWN bit is cleared by the SAR after the entire packet is transmitted, a completion-ring entry is posted, and an interrupt generated to the host.

The host sets the OWN bits for individual buffers in a packet in the transmit-data descriptor rings in order from last to first. This ensures that the DMA block is not held up while waiting to acquire the next buffer from a partially transmitted packet.

start of chain (SOC) (bit 30)

The SOC bit indicates that this is the first buffer of a packet which may consist of one or more buffers. This bit is also set in packets with single buffers. The SOC bit is cleared by the SAR after all processing for the first buffer is complete.

PRINCIPLES OF OPERATION

end of chain (EOC) (bit 29)

The EOC bit indicates that this is the last buffer of a packet. Every packet has at least one buffer with the EOC bit set.

AAL type – AAL5 indicator (bit 27)

The AAL-type bit is set to zero to indicate that the packet described in this descriptor-ring entry is an AAL5 packet. This bit is a configuration item rather than a bit carrying state information. This bit is set in every buffer of a packet, and the software driver ensures that all buffers within a packet use the same AAL type.

current packet length (bits 26 – 16)

The SBus SAR increments this two's-complement value with every cell transmitted until the counter is equal to zero, which indicates to the SAR that the entire packet has been transmitted.

current-buffer length (bits 15 – 0)

The buffer-length field specifies the number of remaining bytes in the buffer currently being processed in this BWG. The SAR adds to the value of this two's-complement field with every transfer of payload data to the XMB until it is equal to zero, which indicates to the SAR that all the bytes in this buffer are processed and queued for transmission.

TX DMA word 1 – current-buffer pointer

Byte-aligned current-buffer pointer (bits 31 – 0)

The current-buffer pointer is copied directly from the start-of-buffer pointer in the corresponding transmit-data descriptor-ring entry at the start of each new buffer. The field is 32 bits, which implies that the buffer is aligned to a byte boundary. The pointer is adjusted to point to the current location after each transfer of payload data from the host to the XMB.

TX DMA word 2 – ATM header

PTI2 (bits 31 – 29)	CLP2 (bit 28)	VPI (bits 27 – 20)	VCI (bits 19 – 4)	PTI1 (bits 3 – 1)	CLP1 (bit 0)

The 4-byte ATM header field is copied directly from the corresponding transmit-data descriptor entry at the start of each new packet. Bits (28 – 0) are concatenated to the 4-bit GFC field that is set to zero for every cell in the packet except the last one. Bits (31 – 28) provide the PTI and CLP fields in the last cell of each packet.

TX DMA word 3 – configuration

BWG_ON (bit 31)	Unused (bits 30 – 0)

This bit allows the host to enable data transmission on a per-BWG basis. The BWG_ON bit from the current BWG index is examined by the SAR on each cell opportunity. BWG_ON (31) is directly set by the host to indicate that the BWG is enabled and that normal data processing is followed. If the bit is zero, no processing of transmit data on the BWG is performed and an idle cell is transmitted on the link. This idle cell is used by the host to respond to congestion indicators.

TX DMA word 4 – descriptor-ring address

TX-data descriptor-ring pointer (bits 31 – 12)	TX descriptor-ring entry (bits 11 – 4)	0000 (bits 3 – 0)

This pointer is a direct DVMA address to the location of the current entry (there are 256 entries in each ring) in the corresponding transmit-data descriptor ring (one of 255 rings) for this BWG. Each descriptor ring is aligned to a 4K-byte boundary in host memory with each entry aligned to a 16-byte boundary.

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TX DMA word 4 – descriptor-ring address (continued)

The address of the 4K-byte boundary in host memory is provided by bits (31 – 12). The entry number between 0 and 255 is provided by bits (11 – 4). The low-order four bits are set to zero, and each entry is 16 byte aligned. Bits (11 – 0) are initialized by the host to zero to correspond with the first entry used by the host in the transmit-data descriptor ring.

TX DMA word 5 – place holder

Place holder (bits 31 – 0)

TX DMA word 6 – transmit CRC

Partial AAL5 transmit CRC (bits 31 – 0)

This field stores the 32-bit CRC calculated over the entire payload of each AAL5 packet. The CRC is placed in the last four bytes of the last cell of the corresponding packet.

TX DMA word 7 – AAL5 tail

AAL5 control field (bits 31 – 16)	AAL5 length field (bits 15 – 0)

The AAL5 control and length fields are copied directly from the corresponding transmit-data descriptor entry at the start of each new packet. The length field is not used for any control functions within the SAR. Both fields are used exclusively for placement in the tail of an AAL5-protocol data unit (PDU).

transmit-completion ring

Table 8 shows the composition of the 4-word entry. The transmit-completion ring is a free ring with 256 entries. The SAR posts an item to the next entry in the completion ring when it completes the transmission of each packet. The transmit-completion ring pointer maintains the value of the current entry within the SAR. The host can recalibrate to this by reading the value from the initialization section in control memory.

Table 8. Transmit-Completion-Ring Summary

ENTRY	DESCRIPTION		
Word 0	OWN (bit 31)	Unused (bits 30 – 8)	BWG index (bits 7 – 0)
Word 1	Reserved		
Word 2	Reserved		
Word 3	Reserved		

TX-completion-ring word 0

OWN (bit 31)

This completion-ring entry is owned by the SBus SAR when the OWN bit is set. The completion-ring entry is owned by the host when the OWN bit is zero. The SAR uses the next completion-ring entry in the ring if the OWN bit is set. The TNETA1560 clears the OWN bit after updating the entry. The host then receives an interrupt and retrieves the next entry in the completion ring to post the completion of packet transmission for a BWG and the release of the buffer space occupied by the buffers constituting the packet. The host clears the OWN bit to allow the SAR to use the completion-ring entry. If the OWN bit is not set when the SAR is ready to post a completed packet, a status bit is set in the hardware-status register and an interrupt is generated if the error condition is unmasked.

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BWG index (bits 7 – 0)

The only item that is posted to the transmit-completion ring when the SAR completes transmission of a packet is the BWG index. This is adequate for the host to locate the transmit-buffer pointers to the buffer locations where data for the packet was stored and reclaim the buffer space.

receive free-buffer-ring format

Table 9 shows the composition of each free-buffer-ring entry. Each of the two rings has 256 entries. The host places free-buffer pointers in each ring. The SAR removes a pointer when it starts processing each new packet from the link.

Table 9. Receive Free-Buffer-Ring Summary

ENTRY	DESCRIPTION		
Word 0	OWN (bit 31)	Unused (bits 30 – 28)	Start-of-buffer pointer (bits 27 – 0)
Word 1		Reserved	
Word 2		Reserved	
Word 3		Reserved	

RX free-buffer-ring word 0

OWN (bit 31)

Each free-buffer-ring entry is owned by the SAR when the OWN bit is set and it is owned by the host when the OWN bit is zero. The host sets the OWN bit for new entries placed in the free-buffer rings. The SBus SAR uses the next free-buffer-ring entry in the respective ring if the OWN bit is set. The SBus SAR clears the OWN bit after acquiring the buffer and releasing the ring location to the host. The buffer is not freed until a packet is posted to the receive-completion ring. If the OWN bit is not set when the SAR polls a free-buffer ring for a new entry, a status bit is set in the hardware-status register and an interrupt is generated if the error condition is unmasked.

start-of-buffer pointer (bits 27 – 0)

A pointer to a buffer, aligned to a 16-byte boundary, is the only information placed in each free-buffer ring.

receive DMA block

The SAR supports 1024 receive DMA-channel entries with each containing eight words. Each DMA channel represents a VCI on which data is received, and DMA entries in the control memory are indexed by incoming VCIs. The SAR initiates all transactions affecting the DMA table, except those required for one-time configuration of a channel in word 3, during normal operation based on the header of cells received from the link. Table 10 summarizes a receive DMA-channel entry.

Table 10. Receive DMA-Virtual-Channel Entry

ENTRY	DESCRIPTION	STATIC/DYNAMIC
Word 0	Control, status, EFCN cell count, current packet length	Dynamic
Word 1	Current buffer pointer – 28 bits	Dynamic
Word 2	Start-of-buffer pointer – 28 bits	Static
Word 3	Control, packet length	Static
Word 4	Reserved	
Word 5	AAL5 partial CRC – 32 bits	Dynamic
Word 6	Reserved	
Word 7	Reserved	

PRINCIPLES OF OPERATION

receive DMA block (continued)

Data with the PTI field equal to 10X, representing VC-level OAM cells, is diverted to DMA channel 0 that operates in the null-AAL mode with a packet length of one cell. Word 0 in each receive DMA-channel entry is copied from word 3 at the start of each new packet. A number of the fields in word 0 represent the dynamic state of the reassembly process for a cell. The fields in word 3 represent one-time configuration values for the VC entered by the host. SAR accesses word 0 during normal cell-level processing to retrieve configuration items.

RX DMA word 0 – VC status/configuration

Control (bits 31 – 23)	Unused (bit 22)	Current congestion number (bits 21 – 11)	Current packet length (bits 10 – 0)

OWN (31)

The OWN bit is set when the DMA channel for this BWG is active and all DMA parameters such as the receive-data pointer, buffer length, and packet length are current. The OWN bit is set by the SAR when word 3 is copied to word 0 at the start of each new packet. The bit is cleared by the SAR when the entire packet has been posted to a buffer in host memory. The BWG is inactive when the OWN bit is zero. Then, the free-buffer ring indicated in word 3 is used to poll a new buffer on the arrival of the first cell of a new packet on the VCI used to index this BWG.

static-configuration bits from word 3

Table 11 summarizes six static-configuration bits copied from word 3 at the start of each packet. Each is described in detail in the section on word 3 of this DMA block.

Table 11. RX DMA Word 0 Static-Configuration Bit Summary

LOCATION	FIELD
Bit 30	VC_ON
Bit 29	Buffer type: small or big
Bit 28	Null-AAL5 indication
Bit 25	AAL3/4 indication
Bit 24	End-of-packet wait
Bit 23	Enable-end-of-packet wait

explicit forward congestion notification (EFCN) cell counter (bits 21 – 11)

The number of cells received with the EFCN indicator set in each packet is counted and the value stored in this field. The EFCN indication is given a logic value of 01x in the PTI field of the ATM header. This value is passed to the receive-completion ring at the end of each packet. Since this field is copied from word 3 at the start of each new packet, it is reset to zero at this time.

packet length (bits 10 – 0)

The packet-length field in word 0 is set up with the two's-complement value for the buffer size used by this BWG at the start of each new packet. The counter is incremented with each new cell until the EOP signal or until the value is zero. Null-AAL packets are terminated when the value of this counter reaches zero. If either the AAL5 or AAL3/4 packet fills the buffer to capacity, the counter reaches zero and the packet is terminated with the buffer-overflow indicator set in the receive completion-ring entry.

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RX DMA word 1 – current-buffer pointer

Unused (bits 31 – 28)	Current-buffer pointer – 16 byte aligned (bits 27 – 0)

The current-buffer pointer is 28 bits, which implies that the buffer is aligned to 16-byte boundaries. This is a dynamic field that is updated with every RCB-to-SBus transaction.

RX DMA word 2 – start-of-buffer pointer

Unused (bits 31 – 28)	Start-of-buffer pointer – 16 byte aligned (bits 27 – 0)

The start-of-buffer pointer is 28 bits because the buffer is aligned to 16-byte boundaries. This field is copied from the corresponding 28-bit field in word 0 of a free-buffer-ring entry.

RX DMA word 3 – configuration

Configuration (bits 31 – 23)	Unused (bits 22 – 11)	Null-AAL packet length (bits 10 – 0)

OWN bit position (bit 31)

The OWN bit is set high for each valid receive channel. It is copied into the corresponding OWN bit location in word 0 at the start of each new packet to indicate that the DMA channel is active.

VC_ON (bit 30)

The VC_ON bit enables packet-reassembly processing. The bit is set in the default mode to indicate that the VC is enabled. The SAR discards cells received on the corresponding VC when the VC_ON bit is deasserted on a per-cell basis.

buffer type – small or big (bit 29)

The SAR supports only two buffer sizes on receive: small and big. The host determines the sizes of the small and big buffers. The buffer-type bit is used to select between a buffer pointer from the small free-buffer ring or the big free-buffer ring for each new packet, which allows the host to target small or big buffers for all packets on a given VC. The small free-buffer ring is used when the bit is set and the big free-buffer ring is used in the default (zero) state.

null-AAL indication (bit 28)

This field is set to indicate that null-AAL packets are received on this BWG (VC). The null-AAL packet-length field in bits (10 – 0) is used to determine the end of a packet. CRC errors are ignored for null-AAL packets. The CRC-error indicator in the receive-completion ring is not used.

AAL3/4 indication (bit 25)

This field is set to indicate that AAL3/4 packets are received on this BWG (VC). This indicates the EOM field in byte 6 (bit 6 of an ATM cell is used as the EOP indicator). CRC errors are ignored for AAL3/4 packets. The CRC-error indicator in the receive-completion ring is not used.

end-of-packet wait (bit 24)

This bit must be set to zero by the device driver during initialization. This gives the SAR the responsibility of setting the bit to one in DMA word 0 (when this feature is enabled). This bit is a status bit used by the TNETA1560 during operation.

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enable end-of-packet wait (bit 23)

When a start of a packet is detected by the TNETA1560, the TNETA1560 requests a buffer from the host memory. If the buffer is not available, the first cell of this packet is dropped. The rest of the packet is dropped after it is received. The host can set bit 23 to 1 enabling the TNETA1560 to drop the cells of a packet that had the first cell dropped. Once the TNETA1560 detects the end packet, it begins to receive packets in this VCI. This feature only works for AAL5 and AAL3/4. For null-AAL and OAM cells, bit 23 must be set to zero.

EFCN cell counter place holder (bits 21 – 11)

This field is set to zero since it is a place holder for the EFCN cell counter in word 0 of this DMA block.

AAL-packet length (bits 10 – 0)

The AAL-packet-length field in word 3 indicates the length of the buffer in cells for each packet in this BWG. This is used in different ways based on whether the BWG supports AAL5 or AAL3/4 packets or null-AAL packets. This field indicates the length of the buffer size allocated by entries in the free-buffer ring used by this BWG for AAL5 or AAL3/4 packets. This is used to detect buffer overflow.

When the null-AAL indicator is set, this field programmed in two's-complement notation represents the number of cells in each null-AAL packet. Since receive DMA channel 0 operates off the null-AAL mode with each packet of size equal to one cell, this field is programmed with the value 1 in two's-complement notation (7FFhex).

RX DMA word 5 – AAL5 partial CRC

Partial AAL5 receive CRC (bits 31 – 0)

This field stores the 32-bit CRC that is calculated over the entire payload of each received AAL5 packet. The CRC is stored in the last four bytes of the last cell in the AAL5 frame. The CRC check results in a unique polynomial, if the frame is error free.

receive-completion ring

Table 12 shows the composition of a 4-word receive-completion-ring entry. The receive-completion ring is a free ring with 256 entries. The SAR posts an item to the next entry in the completion ring when it completes reassembly on a packet. The receive-completion-ring pointer maintains the value of the current entry within the SAR. The host can recalibrate to this by reading the value from the initialization section in control memory.

Table 12. Receive-Completion-Ring Summary

ENTRY	DESCRIPTION
Word 0	Control field, EFCN cells received, packet length
Word 1	Start-of-buffer pointer – 28 bits
Word 2	4-byte ATM header
Word 3	Reserved

RX completion-ring word 0 – control

Control (bits 31 – 29)	Unused (bits 28 – 22)	Congestion cells received (bits 21 – 11)	Packet length (bits 10 – 0)

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OWN (bit 31)

This completion-ring entry is owned by the SAR when the OWN bit is set and it is owned by the host when the OWN bit is zero. If the OWN bit of the next entry in the respective receive-completion ring is zero when the SAR polls it to post the completion-of-packet processing, an error indicator in the status register is set and an interrupt generated. This causes the buffer that the SAR attempted to post to be lost. The SAR clears the OWN bit in the receive-completion ring after it posts the packet. The host then owns the entry and may retrieve various pointers to the packet.

packet overflow (bit 30)

The packet-overflow bit is set if the receive buffer overflowed while processing the current packet. Every packet that ends in a buffer overflow is immediately terminated and a completion-ring entry is posted to the host.

CRC condition (bit 29)

The SAR forwards AAL5 packets with a CRC error to the host. This bit is set when a packet is received with an AAL CRC error.

congestion cells received (bits 21 – 11)

The number of cells received in the packet with the EFCN indication set is forwarded to the host to implement associated feedback mechanisms to squelch the source.

packet length (bits 10 – 0)

All received data is passed to the host in units of 48 bytes. The packet length in 48-byte payload units from word 0 of the receive DMA block is passed to the host in two's-complement notation. This value is always zero for null-AAL packets. The length of AAL5 or AAL3/4 packets in integer units is obtained by subtracting this value from the reassembly-buffer length reserved for the packet.

RX completion-ring word 1 – start-of-buffer pointer

Unused (bits 31 – 28)	Start-of-buffer pointer – 16 byte aligned (bits 27 – 0)

The 28-bit start-of-buffer pointer is provided to the host in the RX completion ring to enable it to locate the reassembled packet.

RX completion-ring word 2 – ATM header

ATM header byte 1	ATM header byte 2	ATM header byte 3	ATM header byte 4

The 4-byte header from the last cell in the reassembled packet is passed to the host.

user registers

This section describes several host-accessible internal SAR registers. Host-write accesses to nonexistent registers are ignored. A null word (32 zeroes) is returned to the host on a read access from a nonexistent register.

configuration register

The configuration register holds various values pertaining to overall SAR configuration. The host may read the register and is allowed to program the EN_RX and the EN_TX bits.

Unused (bits 31 – 5)	NCE_M (bit 4)	0 (bit 3)	EN_RX (bit 2)	EN_TX (bit 1)	0 (bit 0)

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EN_TX – enable transmit operation

The EN_TX bit allows the host to disable packet-to-cell segmentation and any payload data transfer from the host to the link. It is set high to enable normal transmit processing and set to zero to disable such processing. It is set to zero on reset, disabling transmit operation until various configuration register, the BWG table, and the DMA blocks are configured by the host. The transfer of the new cells from SBus to the SAR is inhibited when the enable transmit bit is disabled; however, cells already in the output buffer are forwarded to the PHY layer.

EN_RX – enable receive operation

The EN_RX bit allows the host to disable packet reassembly. All cells from the PHY layer are dropped when the EN_RX bit is zero. The EN_RX bit is set high to enable normal processing. It is set to zero on reset, disabling receive operation until various configuration and the DMA blocks are reconfigured by the host. The transfer of new cells from the ATM link to the receive buffer is inhibited when the enable receive bit is disabled.

NCE mode indicator

The NCE bit is set to indicate to the SAR that cell payloads must be transferred exclusively via 16-byte SBus bursts. The value at the input of the NCE-mode terminal is shifted into this indicator bit on every clock cycle. Internal operation of the SBus SAR is based on the value of this register.

status register

The SAR status register is read only for the host. All the bits except the TX_freeze bit and the SBus error flags are cleared when the register is read. The SAR generates an SBus interrupt to the host if one of the bits in the register is set and if the condition represented by the bit is enabled by the interrupt-enable-mask register. The SBus interrupt is an asynchronous signal that is held until the system clears the condition that caused the interrupt.

Unused (bits 31 – 11)	LB_intr (bit 10)	SB_lerr (bit 9)	SB_err_ack (bit 8)
RX_freeze (bit 7)	TX_freeze (bit 6)	TX_comp_notav (bit 5)	RX_comp_notav (bit 4)
RX_bfree_notav (bit 3)	RX_sfree_notav (bit 2)	TX_comp_update (bit 1)	RX_comp_update (bit 0)

TX_comp_update, RX_comp_update (bits 1 – 0)

The transmit or receive completion update bit is set when the hardware releases a transmit or receive descriptor, respectively, to the completion ring. This is initiated when the OWN bits in the respective DMA blocks are cleared by the SAR.

RX_bfree_notav, RX_sfree_notav (bits 3 – 2)

The appropriate receive free-buffer not-available bit is set when the first entry in the corresponding receive free-buffer ring is not available. This is indicated when the OWN bit in the first entry of the free ring is zero.

The incoming cell is deleted since there is no buffer available in which to place it. This eventually causes the loss of the entire packet due to the resultant CRC error. The buffer-allocation-error bit in the DMA block is set, indicated by a zero in the first free-buffer-ring entry.

RX_comp_notav (bit 4)

The receive completion-ring not-available bit is set when the next descriptor in the receive completion ring has not been released by the host. This is indicated when the OWN bit in the entry is zero. This packet and buffer are both lost to host memory.

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TX_comp_notav (bit 5)

The transmit completion-ring not-available bit is set when the next descriptor in the receive completion ring has not been released by the host. This is indicated when the OWN bit in the entry is zero. The transmit-freeze bit is set when this bit is set, disabling all transmit operation until the transmit-freeze bit is cleared via an active command from the host.

TX_freeze (bit 6)

The transmit-freeze bit is set when the TX_comp_notav bit is set, disabling all transmit operation until the transmit-freeze bit is cleared via an active command from the host. This has the same effect on the transmit circuitry as disabling the enable-transmit bit.

RX_freeze (bit 7)

The receive-freeze bit is set when the RX_comp_notav bit is set, disabling all receive operation until the receive freeze bit is cleared via an active command by the host. The buffer that could not be posted is effectively lost, and the host must find some way to recover it while the freeze is in operation. The receive-freeze indicator has the same effect on the receive path as disabling the enable-receive bit.

SB_err_ack (bit 8)

The SBus-error-acknowledgment bit is set to indicate that the SAR detected the SBus-error-acknowledgment signal; i.e., SBACK2 – SBACK0 set to 110 during the SBus DMA cycle. The SAR then terminates the ongoing master-bus cycle, even if it is a burst transfer, and freezes all DMA-channel operation until a hardware or software reset. This is a fatal error.

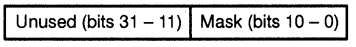
SB_lerr (bit 9)

The SBus-late-error bit is set to indicate that the SAR detected the SBus-late-error ($\overline{\text{SBLERR}}$) signal during the SBus DMA cycle. The SBus SAR then terminates the ongoing master-bus cycle unless it is a burst transfer, in which case, it completes the burst. It then freezes all DMA-channel operation until a hardware or software reset. This is a fatal error.

LB_intr (bit 10)

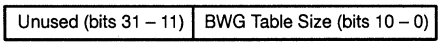
The LBus-interrupt bit is set if an interrupt is generated on the local bus.

interrupt-enable-mask register



The interrupt-enable-mask-register bit has a bit to correspond to every entry in the status register. When a bit in the mask register is set, an interrupt is generated if a corresponding bit in the status register is also set.

BWG-table-configuration register



The 11-bit BWG-table-size register allows the user to configure the size of the BWG table in 4-byte words. Each word in the table consists of four 8-bit entries. The maximum table size is 1200 decimal, allowing for 4800 entries. A resolution greater than 32 kb/s is achieved with 4800 entries. The number of entries in the table is one more than the number programmed in this register; therefore, there is one entry in the table when the register is set to zero.

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FIFO-maximum-depth registers

Unused (bits 31 – 20)	Max_RX_FIFO_Depth (bits 19 – 10)	Max_TX_FIFO_Depth (bits 9 – 0)

This is the only set of statistics collected by the SAR, which is useful information for queuing analysis in different platforms with varying SBus clock speeds and latencies. These registers are not of the read-and-reset variety and must be explicitly set to zero to restart the measurement.

SBus physical-address mapping (in SBus-slave mode)

The SAR allows the host to access various peripheral devices and internal registers via an SBus-slave mode. The device connects to the SBus physical-address bits (15–0) and (24–23).

peripheral devices

Table 13 specifies the SAR-slave mode SBus physical-address ranges for the SAR peripheral devices.

Table 13. SBus Physical Addresses for SAR Peripheral Devices

ADDRESS – 24 BITS (hex)	DESCRIPTION	ADDRESS BITS	READ/WRITE
000000-00FFFF	EPROM addresses	16	Read only
400000-40FFFF	PHY-layer register addresses	16	Read/write
C00000-C03FFF	Control-memory addresses	14	Read/write

SBus SAR registers

The SBus SAR internal registers have an SBus physical-address base value of hex 800000. Table 14 specifies the offset from this address for various SAR registers.

Table 14. SBus Physical Addresses for SAR Registers

OFFSET – 8 BIT (hex)	DESCRIPTION	READ/WRITE
00	Software reset	Write only
04	Status register	Read only
08	Interrupt-mask register	Read/write
0C	Configuration register	Read/write
10	Reserved	
14	BWG-table-size register	Read/write
18	TX/RX FIFO-maximum-depth register	Read/write
1C	Reserved	
20	Clear-transmit-freeze command	Write only
24	Clear-receive-freeze command	Write only

PRODUCT PREVIEW

- **Peripheral Component Interconnect (PCI) Device That Provides Asynchronous Transfer-Mode (ATM) Interface**
- **Single-Chip Segmentation and Reassembly (SAR) for Full-Duplex ATM Adaptation-Layer (AAL) Processing**
- **On-Chip PCI Host Interface Allows Use of Host Memory for Packet SAR**
- **53-Byte ATM Cells Are Transparent to the User**
- **Provides Complete Encapsulation and Termination of AAL5 and Limited AAL3/4**
- **Features a Null AAL That Provides Functions for Constant-Bit-Rate Services**
- **Supports 1023 Unique Virtual Circuits (VCs) on Receive Side**
- **Explicit Cell-Level Interleaving Between Groups of VCs**
- **Packet Interface Is Managed by Efficient Descriptor Rings**
- **Physical (PHY)-Layer Interface Is Full Duplex and Compliant to the ATM Forum UTOPIA Contribution**
- **Supports PHY-Layer Data Rates in the Range of 25.6 Mbit/s to 155.52 Mbit/s**
- **Interfaces Directly to the TNETA1500 SONET ATM BiCMOS Receiver/Transmitter (SABRE)**
- **Recognizes ATM-Layer Operation and Maintenance (OAM) Cells**
- **No External Logic Required for Host or Local Buses to Ensure Simple Design**

description

The TNETA1561 (PCI SAR) is an asynchronous transfer mode (ATM) segmentation and reassembly (SAR) device with a peripheral component interconnect (PCI)-bus interface. This device incorporates ATM adaptation-layer (AAL) processing, ATM SAR processing for full-duplex operation up to STS-3c rate of 155.52 Mbit/s, and the controls for the register interface on the physical (PHY) layer. The TNETA1561 provides a packet interface that is managed by descriptor rings, making the 53-byte ATM-framing format transparent to the user. The device passes the payload of 48 bytes, constituting the payload of each cell, across the PCI-host interface. All packets are segmented and reassembled in host memory and accessed by the chip via the descriptor-ring mechanism. The device reduces the memory requirements for network-interface cards (NICs). The TNETA1561 requires no local processor on the card, which enables very compact solutions.

The applications for the TNETA1561 include NICs for client workstations and servers, embedded applications like LAN emulation, and multiprotocol systems like video servers. The TNETA1561 provides complete AAL5 encapsulation and termination in hardware. In addition, limited support is provided for AAL 3/4, and a null AAL is provided to facilitate real-time data transfer. The TNETA1561 recognizes ATM-layer operation and maintenance (OAM) cells.

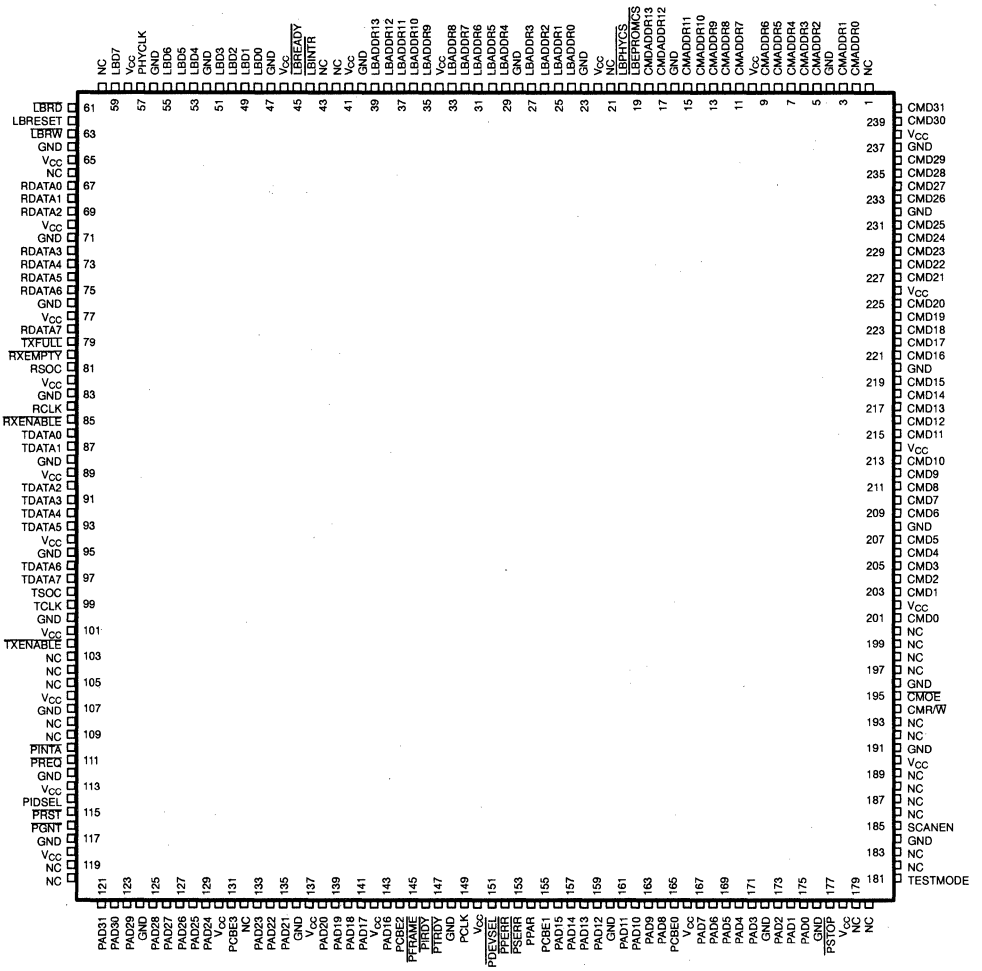
In the transmit direction, the TNETA1561 generates data via a special bit-rate control table that provides explicit cell-level interleaving between groups of virtual circuits (VCs). This mechanism brings a higher degree of flexibility when specifying peak rates for each group (up to 155.52 Mbit/s at a resolution greater than 32 kbit/s). The VCs within a group are serviced via a first-in, first-out (FIFO) discipline on a per-packet basis.

In the receive direction, the TNETA1561 allows multiple virtual paths (VPs) with the condition that each VC is unique. The device is primarily intended for AAL5 encapsulation and termination that is supported in hardware.

The TNETA1561 has four interfaces that include the following: the PCI-bus interface with a 32-bit-wide data bus, the cell interface based on the universal test and operations interface for ATM (UTOPIA specification), a control-memory interface to access the local SRAM, and the local-bus interface to access the PHY-layer registers. The UTOPIA interface to the PHY layer consists of an 8-bit-wide data path and associated control signals in both the transmit and receive directions. The fifty-three-byte ATM cells pass between the ATM and PHY layers through the UTOPIA interface.

PRODUCT PREVIEW

PGC PACKAGE
(TOP VIEW)



NC – No internal connection

description (continued)

The native clock for the TNETA1561 is the PCI clock, which operates up to 33 MHz. The native word size for the device is 32 bits, corresponding to the data width for the PCI bus. The TNETA1561 is compliant to the PCI-local-bus specifications (revision 2.0). The control-memory interface is 32 bits wide. This interface allows the device to access the local memory to obtain the control information on the packets being segmented and reassembled and to obtain their locations in host memory. Each packet queued for transmission can be distributed across multiple buffers in host memory with each starting at any byte boundary. This is supported in hardware by the device. Every received package is placed in a single buffer in the host memory and is aligned to a 16-byte boundary. The TNETA1561 operation is explained in detail in the Principles of Operation section.

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Terminal Functions

PCI-bus interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{PINTA}}$	110	O (open drain)	PCI interrupt. $\overline{\text{PINTA}}$ is an interrupt request from PCI SAR.
PAD31–PAD0	121–123, 125–129, 133–135, 138–141, 143, 156–159, 161–164, 167–170, 171, 173–175	I/O (3 state)	PCI address bus and data bus. PAD31–PAD0 is multiplexed on the same PCI terminals. During the first phase of a transaction (address phase), PAD31–PAD0 contains a 32-bit physical address. This phase is the clock cycle when $\overline{\text{PFRAME}}$ is asserted. During the data phase, PAD7–PAD0 contains the least significant byte and PAD31–PAD24 contains the most significant byte. Write data is stable when $\overline{\text{PIRDY}}$ is asserted. Read data is stable when $\overline{\text{PTRDY}}$ is asserted. Data is transferred during those clock cycles when both $\overline{\text{PIRDY}}$ and $\overline{\text{PTRDY}}$ are asserted.
PCBE3–PCBE0	131, 144, 155, 165	I/O (3 state)	PCI-bus command and byte enable. PCBE3–PCBE0 lines are multiplexed on the same PCI terminals. During the address phase of a transaction, PCBE (3–0) lines define the bus command. During the data phase, PCBE3–PCBE0 lines define which bytes are valid.
PCLK	149	I	PCI clock. PCLK provides timing for all transactions on PCI.
$\overline{\text{PDEVSEL}}$	151	I/O (3 state)	PCI device select. $\overline{\text{PDEVSEL}}$, when actively driven, indicates that the driving device has decoded its address as the target of the current access. As an input, $\overline{\text{PDEVSEL}}$ indicates whether any device on the bus is selected.
$\overline{\text{PFRAME}}$	145	I/O (3 state)	PCI frame. $\overline{\text{PFRAME}}$ is driven by the current master to indicate the beginning and duration of an access. $\overline{\text{PFRAME}}$ is asserted at the beginning of the bus transaction and remains asserted during data transfer. When $\overline{\text{PFRAME}}$ is deasserted, the transaction is in the final data phase.
$\overline{\text{PGNT}}$	116	I	PCI bus grant. $\overline{\text{PGNT}}$ indicates to the agent that the arbiter has granted access to the bus. $\overline{\text{PGNT}}$ is a point-to-point signal and every master has its own.
PIDSEL	114	I	PCI initialization and device select. PIDSEL is used as a chip select during configuration read and write transactions.
$\overline{\text{PIRDY}}$	146	I/O (3 state)	PCI initiator ready. $\overline{\text{PIRDY}}$ indicates the initiating agent's (bus master) ability to complete the current data phase of the transaction. During a write, $\overline{\text{PIRDY}}$ indicates valid data on PAD31–PAD0. During a read, $\overline{\text{PIRDY}}$ indicates the master is prepared to accept the data. $\overline{\text{PIRDY}}$ is used with $\overline{\text{PTRDY}}$ when wait cycles are inserted until both $\overline{\text{PIRDY}}$ and $\overline{\text{PTRDY}}$ are asserted.
PPAR	154	I/O (3 state)	PCI parity. PPAR is even across PAD31–PAD0 and PCBE3–PCBE0. For data phases, PPAR is valid one clock after either $\overline{\text{PIRDY}}$ is asserted on a write or $\overline{\text{PTRDY}}$ is asserted on a read. Once asserted, PPAR remains valid until one clock after the completion of the current data phase. The master drives the PPAR for address-and write-data phases. The target drives PPAR for the read-data phase.
$\overline{\text{PPERR}}$	152	I/O (3 state)	PCI parity error. $\overline{\text{PPERR}}$ reports a data-parity error on all commands except special cycle. An agent cannot report a $\overline{\text{PPERR}}$ until it has claimed the access by $\overline{\text{PDEVSEL}}$ and completed a data phase.
$\overline{\text{PREQ}}$	111	O	PCI request. $\overline{\text{PREQ}}$ indicates to the arbiter that this agent desires use of the bus. Every master has its own $\overline{\text{PREQ}}$.
$\overline{\text{PRST}}$	115	I	PCI reset. $\overline{\text{PRST}}$ forces the PCI sequence of each device to a known state.
$\overline{\text{PSERR}}$	153	I/O (open drain)	PCI system error. $\overline{\text{PSERR}}$ reports address-parity errors and data-parity errors on special-cycle commands.
$\overline{\text{PSTOP}}$	177	I/O (3 state)	PCI stop. $\overline{\text{PSTOP}}$ indicates the current target is requesting the master to stop the current transaction.
$\overline{\text{PTRDY}}$	147	I/O (3 state)	PCI target ready. $\overline{\text{PTRDY}}$ indicates the target agent's (selected device) ability to complete the current data phase of the transaction. During a read, $\overline{\text{PTRDY}}$ indicates that valid data is present on PAD31–PAD0. During a write, $\overline{\text{PTRDY}}$ indicates that the target is prepared to accept data.

PRODUCT PREVIEW

Terminal Functions (Continued)

PCI SAR and local-bus interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
LBRESET	62	O	Local-bus reset. LBRESET is an active-high signal that is driven by the PCI SAR.
$\overline{\text{LBPHYCS}}$	20	O	Local-bus PHY-layer chip select. $\overline{\text{LBPHYCS}}$ is used to interface with PHY-layer devices and is driven by PCI SAR.
$\overline{\text{LBEPROMCS}}$	19	O	Local-bus EPROM chip select. $\overline{\text{LBEPROMCS}}$ is an active-low signal that is driven by PCI SAR.
$\overline{\text{LBRW}}$	63	O	Local-bus write. $\overline{\text{LBRW}}$ is an active-low write signal that indicates a write operation and is driven by PCI SAR.
$\overline{\text{LBRD}}$	61	O	Local-bus read. $\overline{\text{LBRD}}$ is an active-low read signal that indicates a read operation and is driven by PCI SAR.
$\overline{\text{LBINTR}}$	44	I	Local-bus interrupt. $\overline{\text{LBINTR}}$ is an interrupt that is generated and driven by a local-bus device.
$\overline{\text{LBREADY}}$	45	I	Local-bus ready. $\overline{\text{LBREADY}}$ is driven by local-slave devices. The bus transaction is completed after eight PCI bus cycles regardless of $\overline{\text{LBREADY}}$. $\overline{\text{LBREADY}}$ is accepted by the SAR as a handshake from the devices on the bus.
LBD7–LBD0	51–48, 55–53, 59	I/O	Local-bus data. LBD7–LBD0 are used to transfer data from and to local-slave devices and are driven by PCI SAR or local-slave devices.
LBADDR13–LBADDR0	39–35, 33–29, 27–24	O	Local-bus address. LBADDR13–LBADDR0 are the lower 14 bits of the PCI address bus and are directly routed to the local-bus address lines. LBADDR13–LBADDR0 are driven by PCI SAR.

PHY-layer receive interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
RCLK	84	O	Receive clock. RCLK is equivalent to the internal clock at 19.44 MHz. RCLK is sent to the PHY layer.
RDATA7–RDATA0	78, 75–72, 69–67	I	Receive data. RDATA7–RDATA0 are connected to the PHY-layer receive interface and are driven by the PHY-layer device.
RSOC	81	I	Receive start of cell. RSOC is a start-of-cell signal from the PHY layer that indicates the first byte of an ATM cell was sent to the TNETA1561.
$\overline{\text{RXEMPTY}}$	80	I	Receive buffer empty in the PHY layer. $\overline{\text{RXEMPTY}}$ is a receive buffer-empty signal that acts as an inverted enable signal on this interface and is driven by the PHY layer.
$\overline{\text{RXENABLE}}$	85	O	Receive enable. $\overline{\text{RXENABLE}}$ is active low and is driven by the TNETA1561.

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Terminal Functions (Continued)

PHY-layer transmit interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TCLK	99	O	Transmit clock. The TNETA1561 generates TCLK at the PCI clock frequency and sends it to the PHY layer. TCLK is an inverted version of the internal clock.
TDATA7–TDATA0	97–96, 93–90, 87–86	O	Transmit data. TDATA7–TDATA0 are sent at the rate of the PCI clock and are driven by the TNETA1561.
TSOC	98	O	Transmit start of cell. TSOC is sent by the PCI SAR to the PHY layer and indicates that the first byte of an ATM cell was transmitted to the PHY layer.
$\overline{\text{TXENABLE}}$	102	O	Transmit enable. The SAR turns off $\overline{\text{TXENABLE}}$ when the PHY layer sends the $\overline{\text{TXFULL}}$ signal.
$\overline{\text{TXFULL}}$	79	I	Transmit buffer full in the PHY layer. The PHY layer asserts $\overline{\text{TXFULL}}$ at least four cycles before any internal buffers are full. This makes the TNETA1561 stop the data transmission to the PHY layer.

PCI SAR and control-memory interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CMADDR13–CMADDR0	18–17, 15–11, 9–5, 3–2	O	Control-memory address. CMADDR13–CMADDR0 is a 14-bit address bus and is driven by the PCI SAR.
CMD31–CMD0	240–239, 236–233, 231–227, 225–221, 219–215, 213–209, 207–203, 201	I/O	Control-memory data. The control-memory interface has a 32-bit data bus. CMD31–CMD0 are designed for 20-ns asynchronous SRAMs. The TNETA1561 uses this interface to access the data structures and pointers in the control memory.
$\overline{\text{CMOE}}$	195	O	Control-memory output enable. $\overline{\text{CMOE}}$ is an active-low signal and is driven by the PCI SAR.
CMR/$\overline{\text{W}}$	194	O	Control-memory read/write. CMR/$\overline{\text{W}}$ determines a read or write operation. If the output is low, it is a write operation. If the output is high, it is a read operation. CMR/$\overline{\text{W}}$ is driven by the PCI SAR.

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PCI SAR and test/control interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
PHYCLK	57	I	PHY-layer clock. PHYCLK is a 19.44-MHz clock signal driven by a PHY-layer clock crystal.
NC	1, 21, 43, 44, 60, 66, 103–105, 108, 109, 119, 120, 132, 179, 180, 182, 183, 186–189, 192, 193, 197–200	O	No connection. Leave open.
SCANEN	185	I	SCAN enable. Connect to ground for normal operation.
TESTMODE	181	I	Test mode. TESTMODE is driven by the test system. Leave grounded for normal operation.

power and ground

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
GND	4, 16, 23, 28, 40, 47, 52, 56, 64, 71, 76, 83, 88, 95, 100, 107, 112, 117, 124, 136, 148, 160, 172, 176, 184, 191, 196, 208, 220, 232, 237	Ground
V_{CC}	10, 22, 34, 41, 46, 58, 65, 70, 77, 82, 89, 94, 101, 106, 113, 118, 130, 137, 142, 150, 166, 178, 190, 202, 214, 226, 238	Supply voltage

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 6 V
Input voltage range, V_I ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 2) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 3) ..... ±20 mA
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the GND terminals.
2. Applies for external input and bidirectional buffers
3. Applies for external output and bidirectional buffers

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			4.75	5	5.25	V
V_{IH}	High-level input voltage	CMOS	V_{CC} = 4.75 V	3.325			V
			V_{CC} = 5.25 V	3.675			
		TTL		2			
V_{IL}	Low-level input voltage	CMOS	V_{CC} = 4.75 V			0.95	V
			V_{CC} = 5.25 V			1.05	
		TTL				0.8	
T_A	Operating free-air temperature			0		70	°C

electrical characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 8 mA	V_{CC}−0.8		V
		I_{OL} = 4 mA	V_{CC}−0.8		
V_{OL}	Low-level output voltage	I_{OH} = 8 mA		0.5	V
		I_{OL} = 4 mA		0.5	
I_{OZ}	High-impedance-state output current	$V_I = V_{CC}$ or GND		±10	µA
I_{IL}	Low-level input current	V_I = GND		−1	µA
I_{IH}	High-level input current	$V_I = V_{CC}$		1	µA

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timing requirements (see Note 4 and Figure 1)

NO.			MIN	MAX	UNIT
1	$t_{w(RCLKH)}$	Pulse duration, RCLK high	12		ns
2	$t_{w(RCLKL)}$	Pulse duration, RCLK low	12		ns
3	$t_{su(RSOC)}$	Setup time, RSOC high before RCLK↑	10		ns
4	$t_{su(RXEMPTY)}$	Setup time, $\overline{\text{RXEMPTY}}$ low before RCLK↑	10		ns
5	$t_{su(RDATA)}$	Setup time, RDATA valid before RCLK↑	10		ns
6	$t_{h(RSOC)}$	Hold time, RSOC high after RCLK↑	1		ns
7	$t_{h(RXEMPTY)}$	Hold time, $\overline{\text{RXEMPTY}}$ low after RCLK↑	1		ns

NOTE 4: All output signals are generated on the rising edge of RCLK.

operating characteristics (see Note 4 and Figure 1)

NO.			MIN	MAX	UNIT
8	$t_{d(RXENABLE)}$	Delay time, RCLK ↑ to $\overline{\text{RXENABLE}}$↑	1	20	ns

NOTE 3: All output signals are generated on the rising edge of RCLK.

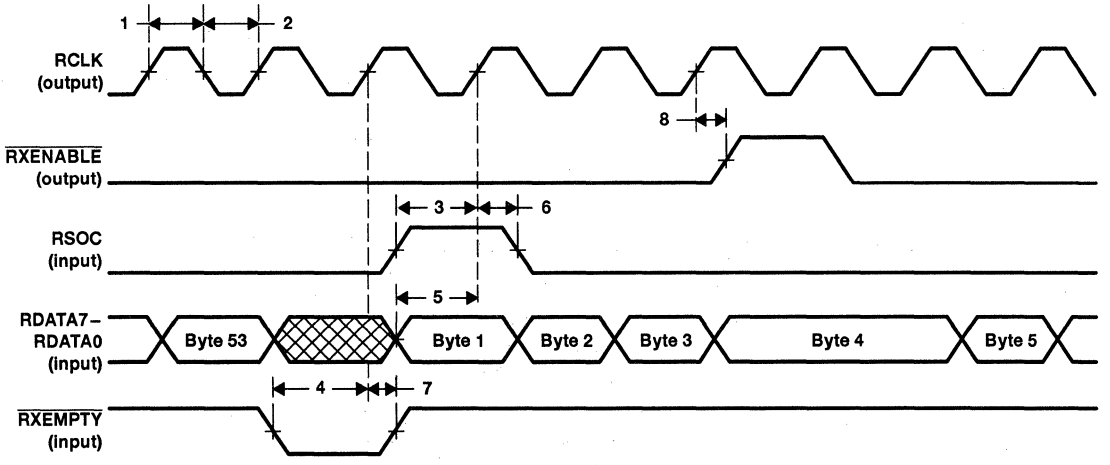

Figure 1. Receive-Cell Interface

timing requirements (see Note 5 and Figure 2)

NO.			MIN	MAX	UNIT
1	$t_{w(TCLKH)}$	Pulse duration, TCLK high	12	18	ns
2	$t_{w(TCLKL)}$	Pulse duration, TCLK low	12	18	ns
3	$t_{su(TXFULL)}$	Setup time, $\overline{\text{TXFULL}}$ low before TCLK↑	10		ns
4	$t_{h(TXFULL)}$	Hold time, $\overline{\text{TXFULL}}$ low after TCLK↑	1		ns

NOTE 5: All output signals are generated on the rising edge of RCLK. All inputs are sampled on the rising edge of TCLK.

operating characteristics (see Note 5 and Figure 2)

NO.			MIN	MAX	UNIT
5	$t_{d(TXENABLE)}$	Delay time, TCLK↑ to $\overline{\text{TXENABLE}}$↓	1	20	ns
6	$t_{d(TSOC)}$	Delay time, TCLK↑ to TSOC↑	1	20	ns
7	$t_{d(TDATA)}$	Delay time, TCLK↑ to TDATA valid	1	20	ns

NOTE 4: All output signals are generated on the rising edge of RCLK. All inputs are sampled on the rising edge of TCLK.

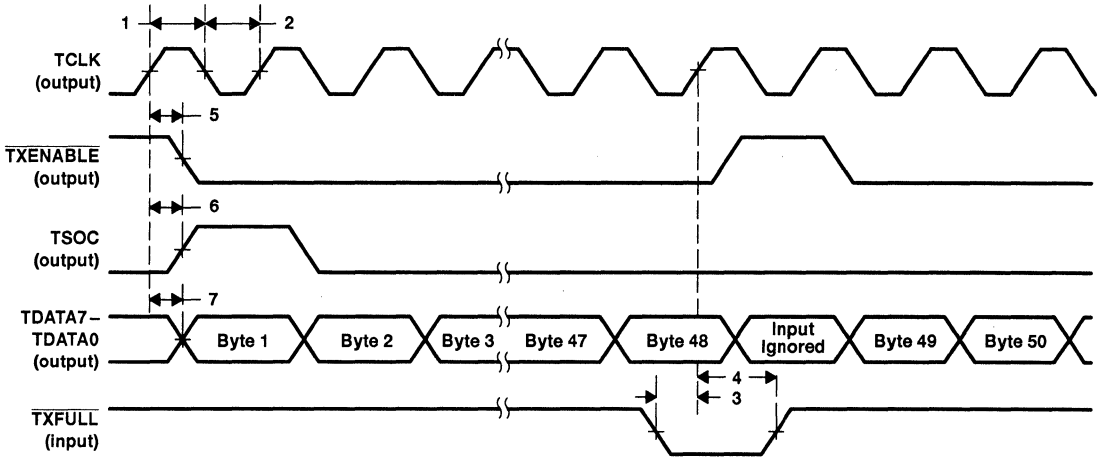

Figure 2. Transmit-Cell Interface

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timing requirements (see Figure 3)

NO.			MIN	NOM	MAX	UNIT
1	$t_{su(PGNT)}$	Setup time, $\overline{PGNT}$ low before PCLK↑	10			ns
2	$t_{su(PTRDY)}$	Setup time, $\overline{PTRDY}$ low before PCLK↑	7			ns
3	$t_{su(PDEVSEL)}$	Setup time, $\overline{PDEVSEL}$ low before PCLK↑	7			ns
4	$t_{h(PTRDY)}$	Hold time, $\overline{PTRDY}$ low after PCLK↑	0			ns
5	$t_{h(PDEVSEL)}$	Hold time, $\overline{PDEVSEL}$ low after PCLK↑	0			ns

operating characteristics (see Figure 3)

NO.			MIN	TYP	MAX	UNIT
6	$t_{d(PREQ)}$	Delay time, PCLK↑ to $\overline{PREQ}$↓	2		12	ns
7	$t_{d(PFRAME)}$	Delay time, PCLK↑ to $\overline{PFRAME}$↓	2		11	ns
8	$t_{d(PCBE)}$	Delay time, PCLK↑ to PCBE valid	2		11	ns
9	$t_{d(PIRDY)}$	Delay time, PCLK↑ to $\overline{PIRDY}$↓	2		11	ns
10	$t_{d(PAD)}$	Delay time, PCLK↑ to PAD31–PAD0 valid	2		11	ns

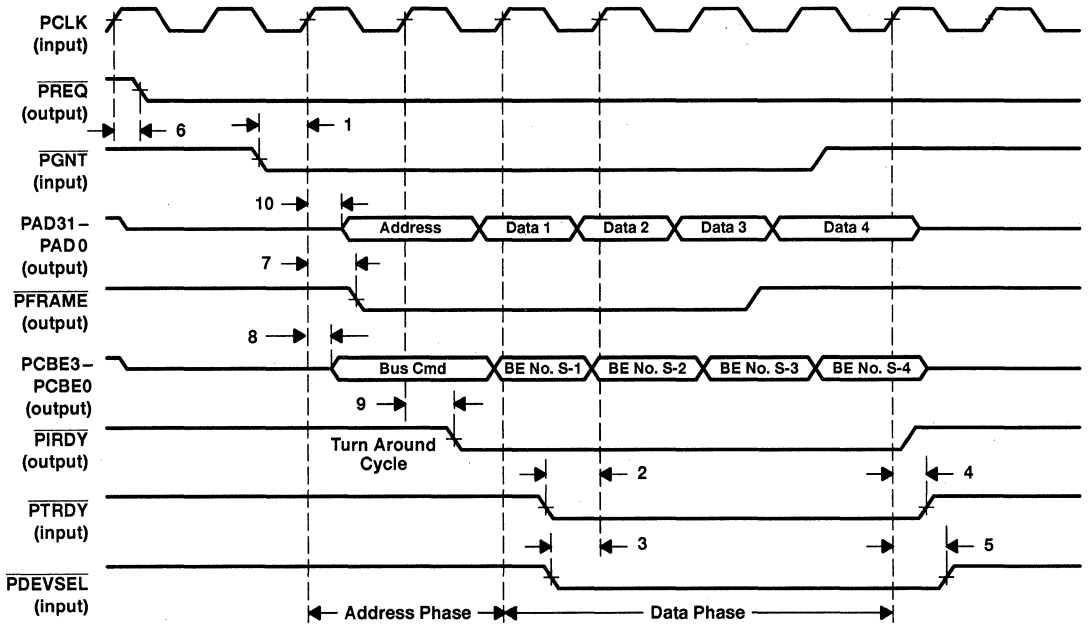

Figure 3. TNETA1561 Write Operation (PCI SAR as Master)

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timing requirements (see Figure 4)

NO.			MIN	NOM	MAX	UNIT
1	$t_{w(PCLKH)}$	Pulse duration, PCLK high	12			ns
2	$t_{w(PCLKL)}$	Pulse duration, PCLK low	12			ns
3	$t_{su(PGNT)}$	Setup time, PGNT low before PCLK↑	10			ns
4	$t_{su(PAD)}$	Setup time, PAD31–PAD0 valid before PCLK↑	7			ns
5	$t_{su(PTRDY)}$	Setup time, $\overline{\text{PTRDY}}$ low before PCLK↑	7			ns
6	$t_{su(PDEVSEL)}$	Setup time, $\overline{\text{PDEVSEL}}$ low before PCLK↑	7			ns
7	$t_{h(PAD)}$	Hold time, PAD31 – PAD0 valid after PCLK↑	0			ns
8	$t_{h(PTRDY)}$	Hold time, $\overline{\text{PTRDY}}$ low after PCLK↑	0			ns
9	$t_{h(PDEVSEL)}$	Hold time, $\overline{\text{PDEVSEL}}$ low after PCLK↑	0			ns

operating characteristics (see Figure 4)

NO.			MIN	TYP	MAX	UNIT
10	$t_{d(PFRAME)}$	Delay time, PCLK↑ to $\overline{\text{PFRAME}}$↓	2		11	ns
11	$t_{d(PAD)}$	Delay time, PCLK↑ to PAD31–PAD0 valid	2		11	ns
12	$t_{d(PCBE)}$	Delay time, PCLK↑ to PCBE3–PCBE0 valid	2		11	ns
13	$t_{d(PIRDY)}$	Delay time, PCLK↑ to $\overline{\text{PIRDY}}$↓	2		11	ns
14	$t_{d(PREQ)}$	Delay time, PCLK↑ to $\overline{\text{PREQ}}$↓	2		12	ns

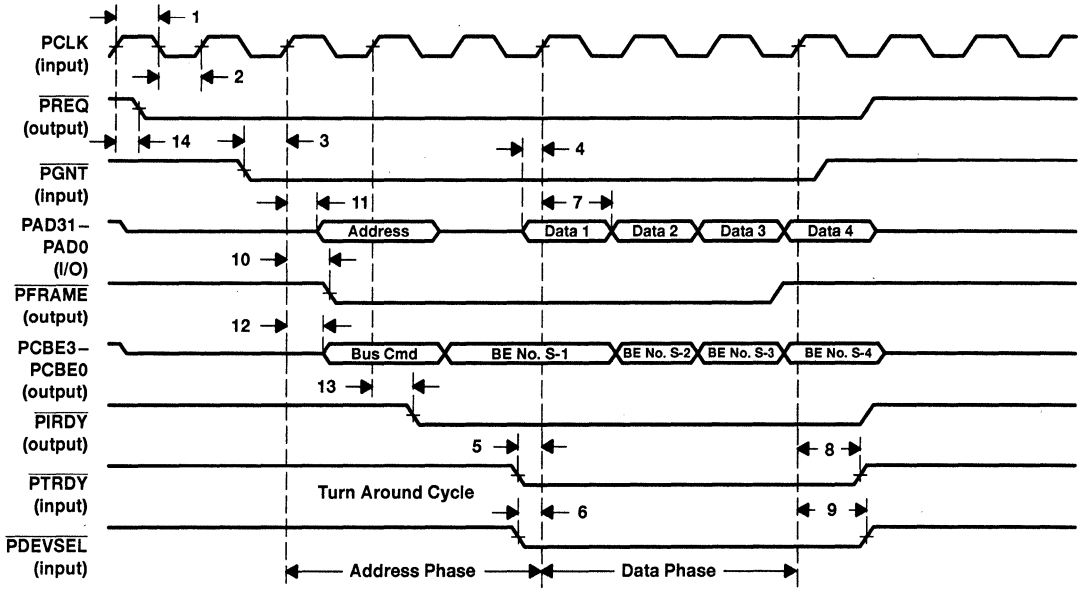

Figure 4. TNETA1561 Read Operation (PCI SAR as Master)

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timing requirements (see Figure 5)

NO.			MIN	NOM	MAX	UNIT
1	$t_{su(PIDSEL)}$	Setup time, PIDSEL high before PCLK↑	7			ns
2	$t_{su(PAD)}$	Setup time, PAD31–PAD0 valid before PCLK↑	7			ns
3	$t_{su(PCBE)}$	Setup time, PCBE3–PCBE0 valid before PCLK↑	7			ns
4	$t_{su(PIRDY)}$	Setup time, $\overline{\text{PIRDY}}$ low before PCLK↑	7			ns
5	$t_{su(PDEVSEL)}$	Setup time, PDEVSEL low before PCLK↑	7			ns
6	$t_{h(PIDSEL)}$	Hold time, PIDSEL valid after PCLK↑	0			ns
7	$t_{h(PAD)}$	Hold time, PAD31–PAD0 valid after PCLK↑	0			ns
8	$t_{h(PCBE)}$	Hold time, PCBE3–PCBE0 valid after PCLK↑	0			ns
9	$t_{h(PIRDY)}$	Hold time, $\overline{\text{PIRDY}}$ low after PCLK↑	0			ns
10	$t_{h(PDEVSEL)}$	Hold time, $\overline{\text{PDEVSEL}}$ low after PCLK↑	0			ns

operating characteristics (see Figure 5)

NO.			MIN	TYP	MAX	UNIT
11	$t_{d(PAD)}$	Delay time, PCLK↑ to PAD31–PAD0 valid	2		11	ns
12	$t_{d(PFRAME)}$	Delay time, PCLK↑ to $\overline{\text{PFRAME}}$↓	2		11	ns
13	$t_{d(PTRDY)}$	Delay time, PCLK↑ to $\overline{\text{PTRDY}}$↓	2		11	ns

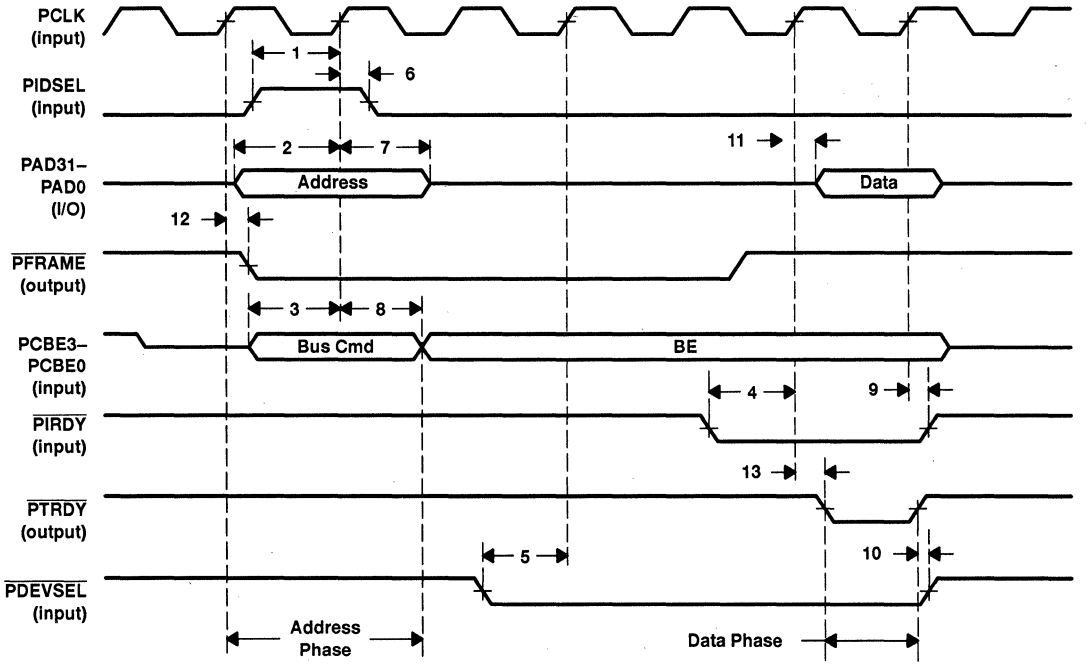

Figure 5. TNETA1561 Read Operation (PCI SAR as Slave)

timing requirements (see Figure 6)

NO.			MIN	NOM	MAX	UNIT
1	$t_{su(PIDSEL)}$	Setup time, PIDSEL high before PCLK↑	7			ns
2	$t_{su(PAD)}$	Setup time, PAD31 – PAD0 valid before PCLK↑	7			ns
3	$t_{su(PFRAME)}$	Setup time, $\overline{\text{PFRAME}}$ low before PCLK↑	7			ns
4	$t_{su(PIRDY)}$	Setup time, $\overline{\text{PIRDY}}$ low before $\overline{\text{PCLK}}$↑	7			ns
5	$t_{su(PDEVSEL)}$	Setup time, $\overline{\text{PDEVSEL}}$ low before PCLK↑	7			ns
6	$t_{h(PIDSEL)}$	Hold time, PIDSEL high after PCLK↑	0			ns
7	$t_{h(PIRDY)}$	Hold time, $\overline{\text{PIRDY}}$ low after PCLK↑	0			ns

operating characteristics (see Figure 6)

NO.			MIN	TYP	MAX	UNIT
8	$t_{d(PTRDY)}$	Delay time, PCLK↑ to $\overline{\text{PTRDY}}$↓	2		11	ns

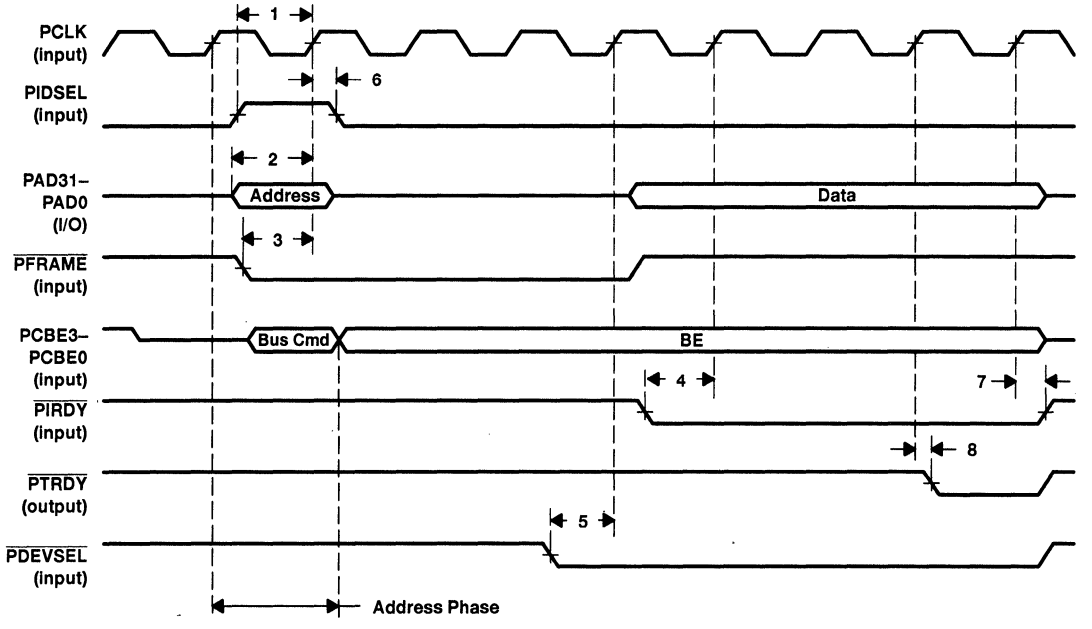

Figure 6. TNETA1561 Write Operation (PCI SAR as Slave)

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operating characteristics (see Figure 7)

NO.			MIN	TYP	MAX	UNIT
1	$t_{d(LBPHYCS)1}$	Delay time, $\overline{LBRD}\downarrow$ $\overline{LBPHYCS}\downarrow$		7		ns
2	$t_{d(LBPHYCS)2}$	Delay time, LBADDR13 – LBADDR0 valid to $\overline{LBPHYCS}\downarrow$		7		ns
3	$t_{d(LBREADY)1}$	Delay time, $\overline{LBPHYCS}\downarrow$ to $\overline{LBREADY}\downarrow$		17		ns
4	$t_{d(LBD)V}$	Delay time, $\overline{LBPHYCS}\downarrow$ to LBD7 – LBD0 valid		16		ns
5	$t_{d(LBD)I}$	Delay time, $\overline{LBPHYCS}\uparrow$ to LBD7 – LBD0 invalid		11		ns
6	$t_{d(LBREADY)2}$	Delay time, $\overline{LBPHYCS}\uparrow$ to $\overline{LBREADY}\uparrow$		9		ns
7	$t_{d(LBADDR)}$	Delay time, $\overline{LBPHYCS}\uparrow$ to LBADDR13 – LBADDR0 invalid		2		ns

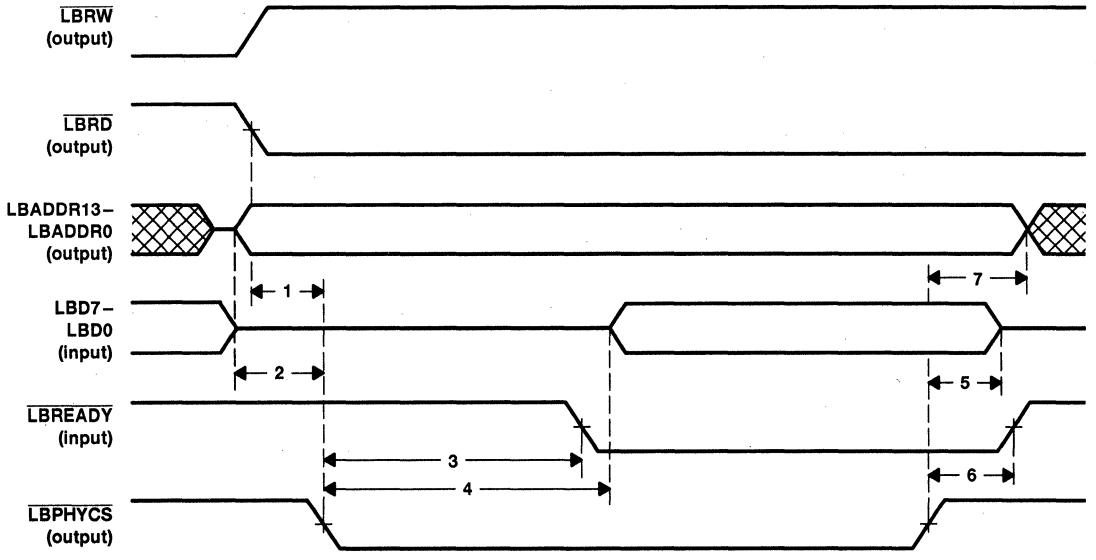

Figure 7. Local-Bus-Interface Read Operation (TNETA1561 as Slave)

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operating characteristics (see Figure 8)

NO.			MIN	TYP	MAX	UNIT
1	$t_{d(LBPHYCS)}$	Delay time, $\overline{LBRW}\downarrow$ to $\overline{LBPHYCS}\downarrow$		7		ns
2	$t_{d(LBPHYCS)2}$	Delay time, LBADDR13 – LBADDR0 valid to $\overline{LBPHYCS}\downarrow$		7		ns
3	$t_{d(LBPHYCS)3}$	Delay time, LBD7 – LBD0 invalid to $\overline{LBPHYCS}\uparrow$		7		ns
4	$t_{d(LBPHYCS)4}$	Delay time, LBADDR13 – LBADDR0 invalid to $\overline{LBPHYCS}\uparrow$		6		ns

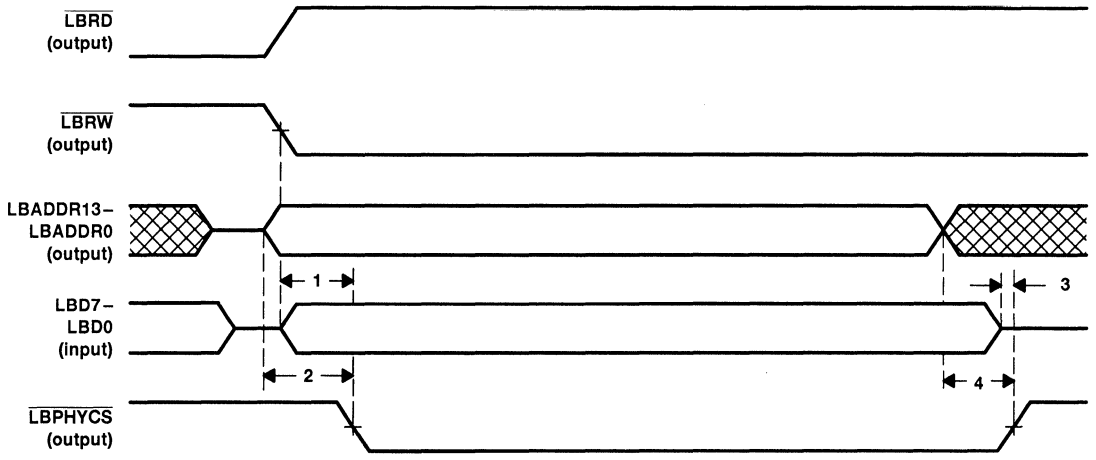

Figure 8. Local-Bus-Interface Write Operation (TNETA1561 as Slave)

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operating characteristics (see Figure 9)

NO.			MIN	MAX	UNIT
1	$t_{w(CMR/WL)}$	Pulse duration, CMR/$\overline{W}$ low			ns
2	$t_{d(CMR/W)1}$	Delay time, CMADDR13 – CMADDR0 valid to CMR/$\overline{W}\downarrow$			ns
3	$t_{d(CMR/W)2}$	Delay time, CMD31 – CMD0 valid to CMR/$\overline{W}\uparrow$			ns
4	$t_{d(CMD)}$	Delay time, CMR/$\overline{W}\uparrow$ to CMD31 – CMD0 invalid			ns

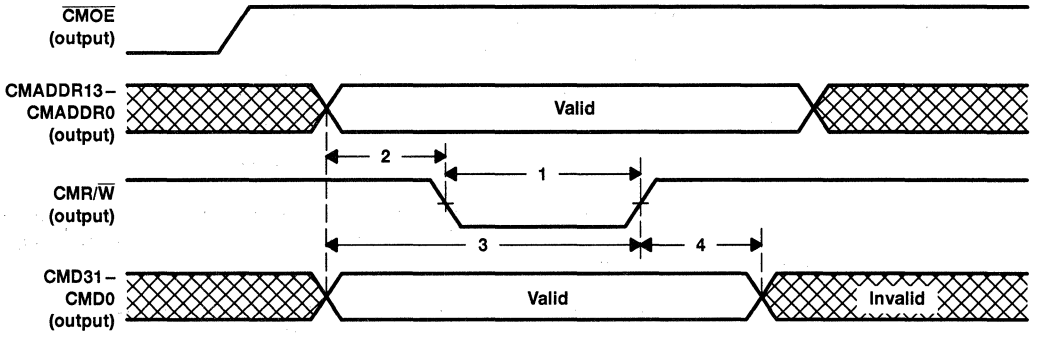

Figure 9. Control-Memory-Interface Write Operation

timing requirements (see Figure 10)

NO.			MIN†	MAX	UNIT
1	$t_{su(CMD)}$	Setup time, CMD31 – CMD0 valid before $\overline{CMOE}\uparrow$			ns
2	$t_{h(CMD)}$	Hold time, CMD31 – CMD0 valid after $\overline{CMOE}\uparrow$			ns

† These numbers are for a 20-ns asynchronous SRAM control memory.

operating characteristics (see Figure 10)

NO.			MIN	MAX	UNIT
3	$t_{d(CMOE)}$	Delay time, CMADDR13 – CMADDR0 valid to $\overline{CMOE}\downarrow$			ns

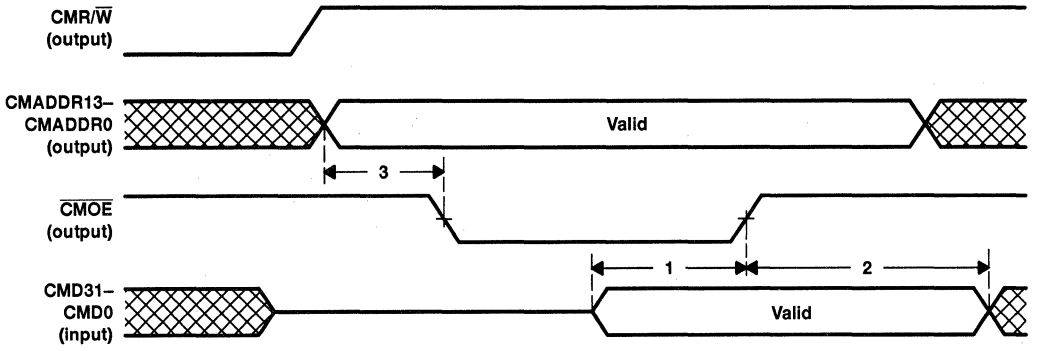

Figure 10. Control-Memory-Interface Read Operation

PRINCIPLES OF OPERATION

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functional overview (see Figure 11)

The TNETA1561 (PCI SAR) is fully compatible with the PCI-bus requirements for connecting a peripheral device to a PCI-bus host system (mapped in memory space) and is designed for the PCI plug-in card concept. The central-resource functions, such as PCI-bus arbitration, are implemented by the host processor using the PCI SAR adapter.

The PCI SAR provides the PCI-configuration space to support its configuration and initialization. This configuration space specifies data for initialization software and error-handling software. The PCI SAR supports the mechanism to implement an external-EPROM interface for device-specific initialization and other booting mechanisms.

The PCI bus uses bursts as the basic mechanism to transfer data. The TNETA1561 supports data-burst sizes up to 52 bytes for a PCI-bus access requiring a total of 13 data-phase transfers. The typical latency for PCI-bus access is 2 μs, but this PCI SAR provides adequate data buffering for a worst-case latency of up to 30 μs.

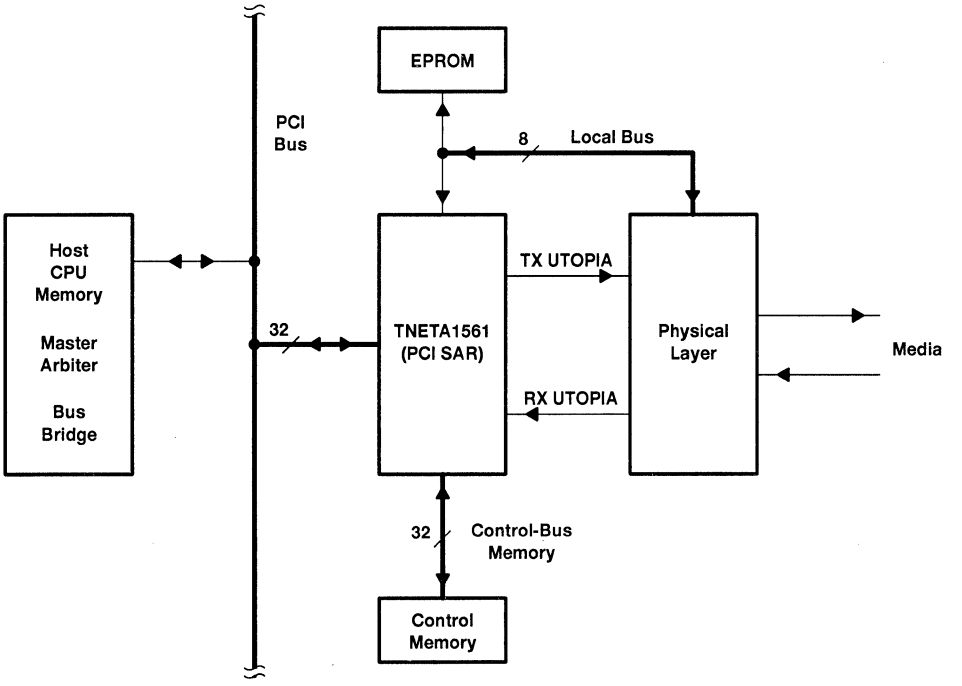

Figure 11. TNETA1561 Architecture

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functional overview (see Figure 11) (continued)

The TNETA1561 provides a packet interface that is managed by descriptor rings to make the 53-byte ATM framing format transparent to the user. The PCI SAR passes the 48-byte payload of each cell across the PCI bus. All packets are stored in host memory and accessed by PCI SAR by the descriptor-ring mechanism.

The PCI SAR generates data in the transmit direction via a special bit-rate control table that provides explicit cell-level interleaving between groups of virtual circuits (VCs). This mechanism provides a high degree of flexibility in specifying peak rates for each group of up to 155 Mbit/s at a resolution greater than 32 kbit/s. VCs within a group are serviced via a FIFO discipline on a per-packet basis.

The PCI SAR supports 1023 unique VCs, typically all associated with virtual path identifier (VPI) 0. VPI 0 allows multiple virtual paths (VPs) with the reminder that each VC is unique. Limited support is provided to recognize ATM-layer OAM cells. The PCI SAR is primarily intended for ATM AAL5 encapsulation and termination that is fully supported in hardware. Limited support is provided for AAL3/4 with 48-byte transfers across the PCI-bus interface and hardware recognition of the EOM indicator on the receive side. In addition, a null AAL is supported to facilitate real-time data transfer. The interface to the PHY layer consists of an 8-bit-wide data path and associated control signals in both the transmit and receive directions. The 53-byte cells pass between the ATM and PHY layers. The native clock for PCI SAR is the PCI-bus clock frequency of 33 MHz. The 8-bit-wide data path on the receive ATM-PHY interface requires a clock rate of at least 19.44 MHz when interacting with a 155.52-Mbit/s physical layer. The receive interface uses the PHY-layer clock. The native word size for PCI SAR is 32 bits, corresponding to the data-bus width for the PCI bus.

functional description

The PCI SAR implements the functions of the transmit and receive modules. The implementation of these modules is described in terms of their functional blocks. The PCI SAR has the following basic blocks: PCIMAC, PMIF, LBIN, USR REG, transmit block (XBTP, CA, XALP, XMB FIFO, XPIN), and receive block (RBTP, RALP, RMB FIFO, RPIN) (see Figure 12).

transmit modules

The transmit host-and-buffer transaction processor (XBTP) is responsible for all host-related functions on the transmit side. It requests 48-byte transfers from the PCI bus-interface block, PCIMAC. The cell actuator (CA) accesses the BWG table and determines the next VC to be serviced. The transmit adaptation-layer processor (XALP) processes all AAL-related functions and adds the 4 bytes of the ATM header to each cell. The AAL5 cyclic redundancy check (CRC) is generated by the XBTP module and it is appended to the packet. The transmit buffer (XMB), a FIFO, is an 8-cell buffer that receives 13 words per cell. Idle cells are also placed in this buffer. The transmit PHY interface (XPIN) does word-to-byte unpacking and interacts with the PHY layer using the PCI-bus clock.

receive modules

The receive PHY interface (RPIN) performs byte-to-word packing, filters idle cells, and interacts with the PHY layer using the system PHY-layer clock crystal. The receive buffer (RMB) performs rate synchronization from the PHY-layer clock to the PCI-bus clock and buffers up to 32 cells. The receive ATM processor (RAT) and the receive ATM adaptation-layer processor (RALP) operate in parallel and are part of the same module. The RALP terminates the AAL5 CRC and processes various EOP indicators. The RAT function is responsible for deleting the ATM header and accessing the correct receive direct-memory access (DMA) entry. Finally, the receive host-and-buffer transaction processor (RBTP) performs all host-specific functions on the receive side.

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PCIMAC

The PCIMAC block is an interface unit between a PCI-based host system and PMIF block of PCI SAR. It masters the PCI bus in its master mode and allows the host to access the PCI SAR in its slave-mode operation. This block provides the PCI-bus host interface with all the interface signals for master and slave operations. This block implements a 32-bit data buffer to provide a data path to and from the host. This data buffer has an interface with the XMB FIFO for transmit data and with RMB FIFO for receive data. This module also has a PCI-configuration space implemented as 32-bit registers.

The PMIF has another interface with PMIF (internal to PCI SAR) that provides all the necessary control signals enabling PCI SAR to operate in master mode. The operation in slave mode is controlled by the host system.

PMIF

The PMIF block provides interfaces to LBIN, CMIA, XBTP, RBTP, and USR REG blocks. The LBIN function provides access to the PHY layer and EPROM. The CMIA interface provides a data path to access control-memory data. The XBTP and RBTP interfaces provide appropriate signals that make the PCI SAR device a PCI-bus master for the transmit or receive function.

The USR REG interface provides status and control data for PCI SAR functions. This block also has a SAR configuration register that is written by the host to enable transmit or receive operation. This block is only a carrier of data and control signals in either its master- or slave-mode operation. It does not initiate any operation except generating PCI-bus requests.

CMIA

The CMIA block provides an interface to the control memory using the local memory bus. It performs memory arbitration for all the functions that access control memory. Each access is a one (32-bit) word access. The priority mechanism to service various functions is in the following order: RALP, XALP, CA, RBTP, XBTP, and PMIF.

PHY layer

The PHY-layer interface is serviced by the XPIN and RPIN modules for either reading data from the XMB FIFO in the transmit direction or writing data to RMB FIFO in the receive direction. Figure 12 depicts the data-flow representation of the PCI SAR functional block diagram.

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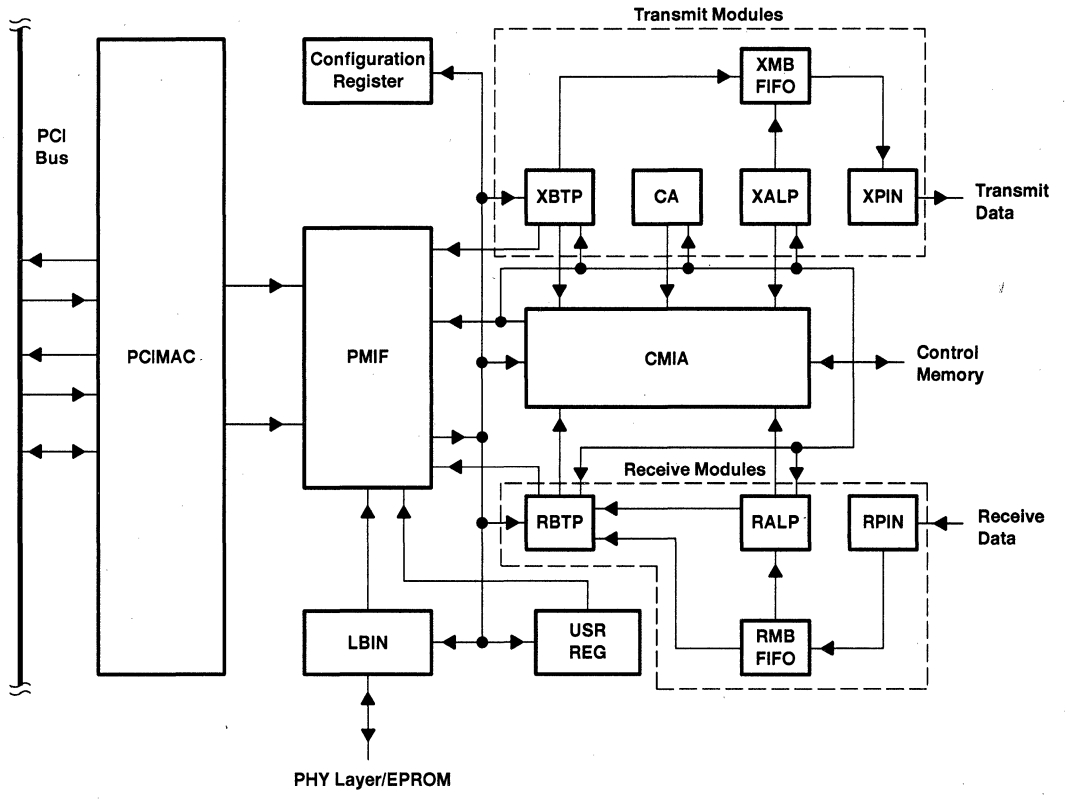

Figure 12. PCI SAR Functional Block Diagram

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interfaces

The PCI SAR (TNETA1561) has the interfaces shown in Figure 13. The PCI-bus interface communicates with any other host on the PCI bus. The local-bus interface allows PCI SAR to have access to PHY-layer device registers and to an external EPROM. The control-memory interface allows the host and other internal functions of the PCI SAR to access the control memory. The PHY-layer interface allows the PCI SAR to transmit packets to a PHY-layer device or receive cells from it.

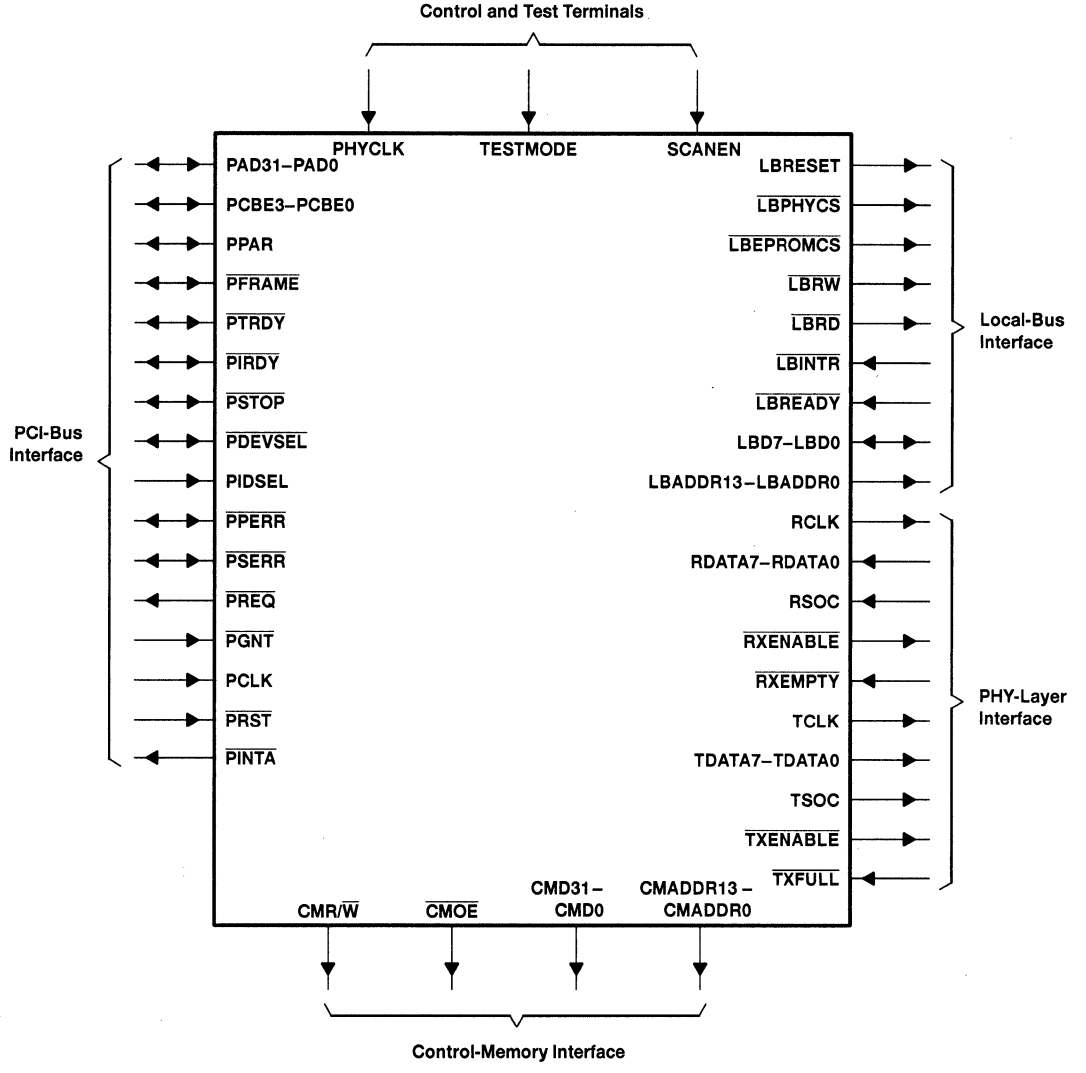

Figure 13. PCI SAR Interface to Other Hosts on the PCI Bus

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PCI-bus interface

The PCI-bus interface is provided by the PCIMAC block of the PCI SAR device. The system terminals are for the PCI-clock and reset function. The address and data terminals are for a 32-bit interface with the least significant byte [LSB] being the bits (7 – 0) and the most significant byte [MSB] being the bits (31 – 24). The bus command and byte enable are used to indicate the valid byte of the data. The device fully supports all bus commands (per PCI Local-Bus Specification. Rev 2.0 April 30, 1993) except for the interrupt acknowledge, special-cycle command, and I/O commands. In the slave mode, the memory-read multiple and the memory-read lines are treated as the memory-read command. The memory write and invalidate commands are treated as the memory-write command. In the master mode, it does not support memory-read multiple and memory-read line commands. The device also provides all the interface control terminals; $\overline{\text{PFRAME}}$ $\overline{\text{PIRDY}}$, $\overline{\text{PTRDY}}$, $\overline{\text{PSTOP}}$, PIDSEL, and $\overline{\text{PDEVSEL}}$. The $\overline{\text{PLOCK}}$ feature is not supported. For bus-master operation, the $\overline{\text{PREQ}}$ and $\overline{\text{PGNT}}$ terminals are provided. The error reporting terminal $\overline{\text{PPERR}}$ is for reporting parity errors (except on a special cycle) and $\overline{\text{PSSER}}$ is for reporting address-and-data parity errors or any other catastrophic system error. The PCIMAC also generates $\overline{\text{PSERR}}$ when it is self selected as the target.

The PCI SAR keeps track of the number of times it has retried a PCI-master transaction. This feature is externally programmable up to a maximum of 15 retries. Once the number of retries exceeds this count value, the TNETA1561 asserts $\overline{\text{PSERR}}$ low. The interrupt $\overline{\text{PINTA}}$ is defined for the PCI SAR. The PCI SAR does not support any JTAG or boundary-scan function. The PCI SAR implements the following functions: the PCI-memory bus master for DMA transfers responds as a PCI slave for local-memory accesses and supports disconnection with retry for PCI. As a PCI-bus master, it supports burst and nonburst data accesses; however, in slave mode it supports only nonburst data transfers. The PC SAR is designed to meet the worst-case latency of the PCI BUS up to 30 µs. A minimum bus-grant value ensures the PCI-bus access for a minimum duration that is long enough to transfer a cell (48 bytes). The PCI macro terminates a transaction when the TNETA1561 is acting as a bus master and no device-select return is detected after it has initiated a transaction.

local-bus interface

The local-bus interface is between the PMIF and LBIN modules. The local bus allows access to the EPROM and the registers on the PHY-layer device. Since several devices are allowed on the local bus, the PCI SAR accepts a ready signal from devices on the bus as a handshake. This accommodates slow devices such as EPROMs and is used to relax timing constraints on the register interface for PHY-layer devices. The local bus is only accessed via PCI-bus transactions with the PCI SAR as the slave (with the exception of the local-bus interrupt signal). The lower 14 bits of the PCI-bus address lines are used to address the local bus. The PCI-bus address must remain stable while the local bus is active.

control-memory interface

The control-memory interface is between the control-memory interface and arbitration (CMIA) and all other modules that access the control memory. The control memory is set up in a 16K × 32 configuration with the cycle time given by the PCI-bus clock. The control-memory interface is designed for an asynchronous SRAM with a 32-bit data bus, a 14-bit address bus, a read or write signal, and an output-enable signal (CMOE).

PHY-layer interface

The ATM-cell-transfer rate is full-duplex 149.76 Mbit/s, but data may arrive in bursts at 155.52 Mbit/s due to the framing scheme described by the PHY layer. A clock rate of at least 19.44 MHz is essential in the receive direction to prevent cell loss due to buffer overflow in the PHY layer. The PCI SAR decouples the PCI-bus clock from the PHY-layer clock in the receive direction via an asynchronous FIFO, which holds up to 32 cells. The PCI SAR transmits data to the PHY layer at the PCI-bus clock rate.

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PHY-layer interface (continued)

The PCI SAR sends a transmit clock at the PCI clock frequency and a receive clock at 19.44 MHz to the PHY layer. The transmit clock sent to the PHY layer is an inverted version of the internal clock. This ensures that all setup- and hold-time restrictions are met. The PCI SAR generates output data along with a start-of-cell indicator in the transmit direction. This data is sent at the rate of the PCI-bus clock. The PHY layer can respond with a full signal, which is asserted at least four cycles before any internal buffers are full. The PCI SAR then turns off the transmit-enable signal until the full signal is deasserted. The PHY layer sends a start-of-cell indicator with output data. The empty signal acts as an inverted enable signal on this interface.

The PHY-layer interrupt signal is directly connected to the PCI-bus interrupt signal; therefore, PCI-bus interrupt is asserted when the PHY-layer interrupt signal is asserted.

operation

The memory mapping of the PCI SAR local-memory elements is mapped in the host-memory space. The host memory-block location, which is determined by the host, is not predefined. The host writes the starting address in the base-address register located in the configuration space. The PCI SAR during read-from or write-to host memory uses the little-endian addressing scheme. This requires byte swapping of data into big endian and writing into the XMB FIFO during the transmit operation. The received data bytes from the RMB FIFO must also be swapped from big endian into little endian.

PCI-bus and data-transfer requirements

The PCI SAR behaves as a PCI-bus DMA master and as a slave. The PCI SAR supports a maximum AAL5 buffer size of 64K bytes, which corresponds to a maximum AAL5 packet length of 64K bytes. In burst mode, the data transfer between the PCI SAR and the host is cell based (48 bytes). This transfer is completed in a single access of the PCI bus, but this is dependent upon the bus latency of the host system. This transfer is always initiated by the PCI SAR as a master. The data transfer across the PCI bus is word based (4 bytes). The PCI SAR also supports nonburst transfers as a master and as a slave for host accesses (as defined in the PCI-bus transaction).

PCI-bus interaction and transfer size

TRANSACTION	PCI SAR ROLE	TRANSFER SIZE
Host access – PCI SAR registers, PHY-layer registers and control memory	Slave	Word
Host access – PCI-configuration space	Slave	Byte/Word
Host access – EPROM	Slave	Word
PCI SAR access – Transmit-completion ring, transmit-descriptor ring, and receive free-buffer ring transactions	Master	Word
PCI SAR access – Posting to host-receive completion-ring entry	Master	4 Word
PCI SAR access – Cell-payload transfers	Master	1–13 Words Latency Dependent

byte swapping

The payload-data (48 bytes per cell) processing by the PCI SAR requires byte swapping to meet the PCI-bus little-endian format. This swapping is required as the transmit and receive data in the local-buffer FIFO is stored in big-endian format. The two formats are described for comparison.

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little-endian addressing

If the starting address to retrieve data is 1232h, the required byte from the word readout is bytes 2 and 3. The next word readout is bytes 4, 5, 6, and 7.

Data Bits	31 – 24	23 – 16	15 – 8	7 – 0	
Addressing Bits	31 (MSB) . . .	. . .	. . .	. . .	0 (LSB)
Byte Addresses	[0–1233]	[0–1232]	[0–1231]	[0–1230]	

Byte 3	Byte 2	Byte 1	Byte 0
Byte 7	Byte 6	Byte 5	Byte 4

big-endian addressing

If the starting address to retrieve data is 1232h, the required byte from the word readout is bytes 2 and 3. The next word readout is bytes 4, 5, 6, and 7.

Data Bits	31 – 24	23 – 16	15 – 8	7 – 0
Addressing Bits	0 (MSB)	. . .	. . .	31 (LSB)
Byte Addresses	[0–1230]	[0–1231]	[0–1232]	[0–1233]

Byte 0	Byte 1	Byte 2	Byte 3
Byte 4	Byte 5	Byte 6	Byte 7

The data bytes, starting from the least significant byte, are located in the LSB position for the little-endian format and in the MSB position for big-endian formats.

memory-map table

The following memory-map table defines the offset-address range for the various blocks of the control memory as they are mapped into host memory. The host-memory base address of the control-memory block is obtained from the base register 0. This is defined in the paragraph for the PCI SAR configuration-space registers. The host-memory base address of the EPROM-memory block is obtained from the expansion-ROM base-address register. These base addresses are defined in the PCI-SAR configuration-space register section.

control-memory block – maximum size of 64K bytes

The first 48K bytes of this block are in the control memory (external to the PCI SAR) and are divided into the first 16K bytes for the transmit-side information and the next 32K bytes for the receive-side information. The remaining 16K bytes are divided into 8K bytes each for the USR register (within the PCI SAR) and PHY-layer register (PHY-layer device external to PCI SAR).

OFFSET ADDRESS BITS	DESCRIPTION		READ/WRITE REGISTER
00000000h – 000003FFh	Initialization block	(256 words)	R/W
00000400h – 000023FFh	Transmit DMA states	(2K words)	R/W
00002400h – 00003FFFh	BWG table	(1.2K words)	R/W
00004000h – 0000BFFFh	Receive DMA states	(8K words)	R/W
0000C000h – 0000DFFFh	PHY-layer register	(2K words)	R/W
0000E000h – 0000FFFFh	USR register	(2K words)	R/W

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indirect local-memory block – maximum size of 8K bytes

The indirect control-memory block includes the following registers for addressing, data, and status information:

REGISTER	SIZE	DESCRIPTION
Control-memory address register	32 bit	Contains the address of the control-memory block
Control-memory data register	32 bit	Buffer that provides data read from or written to the control-memory block
Control-memory control register 1 – register 8	32 bit	Display PCI SAR register information

EPROM memory block

The maximum size for the EPROM is 8K bytes.

PHY-layer registers access

The TNETA1561 uses the local-bus interface to access the PHY-layer registers. The host system must use the PCI interface to address the register in the PHY layer; therefore, a 32-bit address has to be generated from the host and passed to the TNETA1561. To access a byte-wide address offset for the PHY-layer device registers, the host software has to increment the PCI-offset address by four bytes because the lower two address bits are always ignored. The TNETA1561 converts this address to a byte-wide offset allowing easy access to the registers. The data in the PHY-layer registers is byte wide, so the reads and writes carry a byte of information. The TNETA1561 copies this byte four times into a 4-byte word and transfers this word to the host. The host then extracts one of the four bytes.

PCI-OFFSET ADDRESS BITS	PHY-REGISTER OFFSET ADDRESS
0000C000h	00
0000C004h	01
0000C008h	02
0000C00Ch	03
0000C010h	04

control-memory access

The control memory is accessed by using the offset-address bit of the PCI-bus address. This provides a 14-bit-wide address bus to the control memory. All PCI-bus accesses to control memory are one-word accesses at word boundaries.

control-memory address map

The data below specifies the memory regions and base pointers of the control-memory address map.

MEMORY REGIONS	CONTROL-MEMORY BASE POINTERS (HEX)
Initialization block	0000h
Transmit BWG 0 – 255 – DMA block	0100h
BWG table (1200 words, 4800 entries)	0900h
Receive BWG/VCI 0 –1023 – DMA block	1000h

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PCI-bus physical addresses for PCI SAR peripheral devices

The data below specifies the PCI SAR slave-mode PCI-bus physical-address ranges for peripheral devices.

DESCRIPTION	ADDRESS BITS	READ/WRITE REGISTER
EPROM addresses	14	R
PHY-layer register addresses	14	R/W
Control-memory addresses	14	R/W

packet-interface information

Packet interface, BWG-table mechanism, AAL5 processing, AAL3/4 processing, null-AAL processing, VPI/VCI/GFC processing, OAM processing, and details on the transmit-descriptor rings/DMA, receive free-buffer rings/DMA, and completion rings is described in this section.

The PCI SAR uses host memory to store a packet (48-byte cells) in both transmit and receive directions. The PCI SAR initiates the data transfer for the PCI bus for both transmit and receive operations. The packet does not include AAL5 encapsulation while in host memory. The PCI SAR provides this header data. The buffering of data within the PCI SAR is limited to an 8-cell FIFO for transmit and a 32-cell FIFO for receive.

Each packet queued for transmission may be distributed across multiple buffers in host memory with each starting on a one-byte boundary. Packets that are received over ATM are placed in a single buffer in host memory (either big or small) aligned to a 16-byte boundary.

bandwidth group (BWG) table mechanism

The PCI SAR generates data via a special bit-rate control table known as the BWG table. Each BWG consists of one or more virtual circuit identifiers (VCIs), and each VCI is served via a FIFO discipline on a per-packet basis. Each entry in the BWG table consists of an 8-bit BWG index, and BWGs are serviced based on the composition of the BWG table. The size of the BWG table is programmable with a maximum of 4800 entries, organized as 1200 words, to provide a resolution greater than 32 kbit/s (see Figure 14).

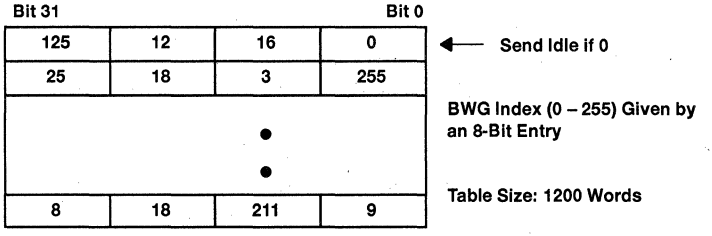

Figure 14. BWG Table

AAL-type processing

The PCI SAR supports various types of AAL processing. AAL3/4, AAL5, null-AAL, GFC, and OAM processing are described in this section.

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AAL5 processing

The primary support is for AAL5 with encapsulation in the transmit direction and termination in the receive direction. AAL5 packets are converted to cells by the PCI SAR before delivery to the PHY layer. Similarly, the device recovers the 53-byte ATM cells from the PHY layer before it performs AAL5 termination.

Since 48 bytes are provided across the PCI-bus interface, all AAL3/4 packet data processing is performed by the host in software. AAL5 processing is disabled on VCIs using AAL3/4. The AAL3/4 EOM indicator, which is located in the first byte of the ATM payload (see Figure 15), is recognized in hardware, initiating an interrupt to the host. This is used by the host to retrieve successive 48-byte payload segments from the appropriate buffer.

AAL3/4 processing

The PCI SAR adds the pad, the control/length field, and the cyclic redundancy check (CRC) for transmit packets. The PCI SAR does not interpret the field length in the AAL5 frame in the receive direction; therefore, the entire AAL5 packet is forwarded to host memory allowing the driver to remove the correct payload. This also allows the host to examine the control field in software, necessary in a time of evolving standards in this area. The PCI SAR performs CRC checks in the receive direction and indicates EOP processing to the host based on the EOP indication in AAL5.

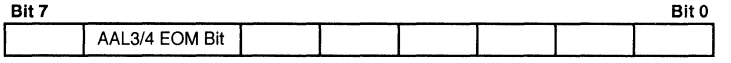

Figure 15. AAL3/4 Processing

null-AAL processing

Null-AAL processing uses the same mechanism as AAL3/4 in the transmit direction to disable AAL5 processing. The control entry associated with each BWG (VCI) in the receive direction has an entry to indicate an interval defined in units of cells received. The PCI SAR then provides an interrupt to the host when the number of cells received on the VCI is equal to that indicated by the table entry. This counter is reset after each interrupt (at the end of each interval). This interval is also referred to as a packet, although it does not encapsulate a well-defined unit of information.

high-order VPI/VCI bits and GFC processing

The lower ten bits of the VCI are used to encode the 1023 possible VCIs. VCI 0 is not used since it indicates unassigned cells. The upper-order bits of the VCI and the VPI field are programmable on a per-VC basis on transmit.The generic flow control (GFC) field is always set to zero.

The upper-order bits of the VCI, the VPI field, and the GFC field are ignored on all cells that are received. These cells are only passed to the PCI SAR if the header error control (HEC) field is correct, the upper-order bits of the header are set intentionally, or the cell is misrouted. The probability of misrouting is small and such an event would be detected via the CRC check in AAL5. The advantage of this scheme is that any VPI/VCI combination is supported if the lower ten bits of the VCI are unique.

OAM processing

ATM-layer OAM processing does not require real-time intervention and is processed in software. OAM cells received on the link are identified by the PCI SAR.

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ATM-layer OAM encoding

NO.	ITEM	VCI	PTI
1	VP level: link-associated OAM cell	3	–
2	VP level: end-to-end OAM cell	4	–
3	VC level: link-associated OAM cell	Any	4
4	VC level: end-to-end OAM cell	Any	5

Each OAM cell forms a fully encapsulated packet. ATM-layer OAM cells transcend AAL protocols and are recognized differently. The end system recognizes all four ATM-layer OAM flows. OAM cells received on VCI 3 and 4 do not interfere with the normal data stream. The only special processing necessary is to initiate EOP processing for each cell. The software driver must configure VCI 3 and 4 as null-AAL channels with a packet length equal to one cell in the receive direction. OAM cells are transmitted as null-AAL packets with length equal to one cell. VC-level OAM cells are specially interpreted. They are diverted to receive DMA channel 0 and the 4-byte ATM header is passed on to a receive-completion ring in host memory during normal EOP processing.

transmit descriptor rings and DMA

Each transmit BWG is supported by a corresponding DMA channel and its own descriptor ring. The PCI SAR supports 255 BWGs, 255 descriptor rings, and 255 DMA channels in the transmit direction. This implies that the number of packets and VCs that are active simultaneously is limited to 255. BWG 0 represents null and a null cell is transmitted. This null cell is generated by the PCI SAR and no data is buffered in the FIFO memory for transmission.

Each descriptor ring holds up to 256 entries corresponding to 256 buffers that may be queued for transmission for that ring. The total number of buffers that can be queued for transmission is approximately 64K (256 buffers per descriptor ring x 255 descriptor rings). The buffers within a descriptor ring are serviced in FIFO order on a per-buffer basis.

Each descriptor-ring entry contains a control bit that indicates whether a buffer is queued up for transmission. The DMA entry for each BWG contains a pointer to the first item in the queue in the corresponding descriptor ring. An idle cell is transmitted if the control bit in the descriptor entry indicates an inactive entry. The DMA entry has a bit that allows the host to disable any BWG.

receive free-buffer rings and DMA

The PCI SAR uses buffer pointers from two free-buffer rings to place the incoming packet data in the host memory. These are called small free-buffer ring and big free-buffer ring. Each receive BWG has a control bit indicating the type of buffer it uses: small or big. These buffers are preallocated by the host application for the next packet and not by the BWG.

The PCI SAR supports 1023 receive DMA channels and 1023 VCIs. The incoming VCI indexes the receive DMA channels. BWG 0 is reserved to process information for OAM cells.

completion rings

The PCI SAR indicates completion of packet processing in either direction to the host via an interrupt and by posting entries to receive- and transmit-completion rings. Each completion ring accepts up to 256 entries. A control bit in each entry of the completion ring prevents the PCI SAR from overwriting an entry that has not been processed by the host.

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data structure

The PCI SAR data structure and contents of various physical locations are summarized below:

CONTROL MEMORY	HOST MEMORY	INTERNAL REGISTERS
BWG table	TX descriptor rings (255)	PCI SAR operational registers
TX DMA states	TX completion ring	PCI SAR configuration registers
RX DMA states	Small free-buffer ring	PCI configuration space
Initialization block	Big free-buffer ring	
	RX completion ring	
	Data buffers	

The parameters necessary for booting the device are stored in the PCI configuration space. The system requiring use of an external EPROM contains the booting sequence.

The system has a bus width of four bytes and all transactions are conducted on 4-byte boundaries. The PCI SAR uses little-endian addressing as a PCI-bus device. Each descriptor ring has 256 entries and each descriptor-ring entry consists of four words. Each descriptor ring is aligned to a 4K-byte boundary in host memory with each entry aligned to a 16-byte boundary.

The PCI SAR has two receive free-buffer rings, one transmit-completion ring, and one receive-completion ring. The current pointer to each of these rings is stored in the initialization block in the control memory. An entry in each transmit DMA channel points to one of the 255 transmit-descriptor rings in host memory.

Each DMA-channel entry consists of eight words and is located in control memory. The DMA entries on both transmit and receive have an OWN bit that is set when the DMA channel is active. The descriptor-ring entries, the completion-ring entries, and the free-buffer ring entries have an OWN bit that is set when the entry belongs to the PCI SAR.

initialization block

The initialization block contains exactly four entries and resides in control memory. The following data shows the configuration of the initialization block.

initialization block table

PCI-BUS ADDRESS OFFSET (HEX)	CONTROL MEMORY ADDRESS (HEX)	BITS 31 – 0
0000	0000	TX completion-ring offset pointer
0004	0001	RX completion-ring offset pointer
0008	0002	Small free-buffer-ring offset pointer
000C	0003	Big free-buffer-ring offset pointer

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initialization block (continued)

The PCI-bus address offsets for control memory have the lower-order two address bits always set to zero since accesses to control memory are permitted only on a word basis. The software driver must setup all of these structures on 16-byte boundaries in host memory. In addition, the driver must write the pointers to the data structures in the initialization block as follows:

- Tx completion-ring offset pointer, small free-buffer ring pointer, and big free-buffer ring pointer.
  The driver selects a host memory address and writes it to control memory by shifting it two bits to the right.
  Example: The host address 4EFF0000 (hex) is written to the control-memory initialization block as 13BFC000 (hex).
- Rx completion-ring offset pointer.
  This pointer is written by shifting the address four bits to the right.
  Example: The host address 4EFF0000 (hex) is written to the control-memory initialization block as 04EFF0000 (hex).

transmit-data descriptor rings

Each of the 255 transmit-data descriptor rings holds 256 entries and each ring represents one transmit packet queued for transmission. A packet is composed of one or more transmit buffers. The host posts entries to the rings and the PCI SAR processes each entry within the given ring.

transmit-data descriptor-ring summary

The data below shows the composition of the four-word entry.

ENTRY	DESCRIPTION
Word 0	Control field, packet length, buffer length
Word 1	Start-of-buffer pointer – 32 bits
Word 2	4-byte ATM header
Word 3	AAL5 tail – control and length fields

TX descriptor-ring word 0 – configuration

Control (bits 31 – 27)	Current packet length (bits 26 –16)	Current buffer length (bits 15 – 0)

OWN (bit 31)

The descriptor is owned by the PCI SAR when the OWN bit is set. The descriptor is owned by the host when the OWN bit is zero. The OWN bit is set by the host when a buffer/packet is queued for transmission. When the next BWG index from the BWG table does not have an active buffer location in the transmit DMA entry, the PCI SAR attempts to recover a new-buffer descriptor entry from the transmit-data descriptor ring. This entry is loaded into the DMA entry if the OWN bit is set. If the OWN bit for the first descriptor in the transmit-data descriptor ring is zero, no data is queued for transmission and an idle cell is transmitted.

The host places all the buffers for a packet in the descriptor ring before setting the OWN bits on the entries representing each buffer in sequence from the last buffer to the first buffer (in reverse order). The PCI SAR clears the OWN bit after it finishes transmitting/processing the bytes associated with the buffer that is pointed to by the DMA entry. When the OWN bit is cleared by the host, word 0 is not meaningful and is overwritten by the host.

start of chain (SOC) (bit 30)

The SOC bit indicates that this is the first buffer of a packet, which consists of one or more buffers. This bit is also set in packets with single buffers.

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end of chain (EOC) (bit 29)

The EOC bit indicates that this is the last buffer of a packet. Single buffer packets have both the SOC and EOC bits set. Packets with multiple buffers have the SOC bit set on the first buffer and the EOC bit set on the last buffer.

interrupt control bit (ICB) (bit 28)

The ICB bit controls interrupt posting by the PCI SAR to the host. The setting of ICB to active high disables posting of interrupts to the host by the PCI SAR.

AAL-type – AAL5 indicator (bit 27)

The AAL-type bit indicates that the packet/buffer described in this descriptor-ring entry is an AAL5 packet. When zero, this bit indicates to the PCI SAR that AAL5 processing is being performed in the transmit direction. This includes addition of the pad, the control- and packet-length fields, and the 32-bit CRC. The total size of the AAL5 packet is a multiple of 48 bytes. The PCI SAR implements the functions related to packet length and the generation of the pad. The PCI SAR does not perform any packet-level encapsulation similar to that used in AAL5 for either AAL3/4 or the null AAL. The host provides packets correctly formatted into 48-byte cells to the PCI SAR.

packet length (bits 26 – 16)

The packet-length field is expressed in units of cells in the packet. The host computes the correct number of cells in the packet including additional cells that are sometimes needed for AAL5 to accommodate the 8-byte tail. This field represents the value used by the PCI SAR in silicon to determine the number of cells in a packet and enable EOP processing. The field is programmed in two's complement. Incrementing the value by one each time a cell is sent results in zero when the entire packet is transmitted. The maximum size of a packet is 64K bytes; therefore,11 bits are adequate to describe the largest packet.

Since this is a packet-level field as opposed to one that applies to individual buffers, it is placed only in the first buffer descriptor of a packet in the transmit-data descriptor rings. The DMA channel only updates the packet-length field on a per-packet basis. The packet-length field is used for all three AAL modes that are supported. In each case, the PCI SAR enables EOP processing to notify the host when the EOP is detected on transmit via the packet-length field.

buffer length (bits 15 – 0)

The buffer-length field specifies the number of bytes in the buffer represented by this descriptor-ring entry. The maximum buffer size is 64K bytes, which is the largest packet size and allows an entire packet in one buffer. This field is programmed in two's complement and is equal to zero when all the bytes in a buffer are retrieved by the PCI SAR.

TX descriptor-ring word 1 – start-of-buffer pointer

Byte-aligned start-of-buffer pointer (bits 31 – 0)

The start-of-buffer pointer is 32 bits. Each buffer is aligned on byte boundaries.

TX descriptor-ring word 2 – ATM header

PTI (bits 31 – 29)	CLP (bit 28)	VPI (bits 27 – 20)	VCI (bits 19 – 4)	PTI (bits 3 – 1)	CLP (bit 0)

Word 2 contains the 4-byte header for every cell of the packet. The upper-order four bits of the ATM header, representing the GFC at the user-to-network interface (UNI), are set to zero in every outgoing cell. Bits (3 – 0) in word 2 represent the payload-type indicator (PTI) and cell-loss priority (CLP) fields used in every cell of the packet except the last one (the cell that contains the EOP indication). Bits (31 – 28) in word 2 represent the PTI and CLP fields used in the last cell of the packet.

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TX descriptor-ring word 2 – ATM header (continued)

The PTI field in the last cell of the AAL5 packet is set either to 001 or 011. The CLP is programmable and the cell containing the EOP indication can have a different priority level from the other cells. This field is required only in the first descriptor for the packet. In AAL3/4 or null-AAL packets, the PTI and CLP fields are the same in both the upper- and lower-order bits of word 2.

TX descriptor-ring word 3 – AAL5 control/length

AAL5 control field (bits 31 – 16)	AAL5 length field (bits 15 – 0)

The AAL5 control and length fields apply to packets, not to buffers, and this entry is required only in the first descriptor for the packet. The AAL5 length field is not used to determine the length of the packet during transmit processing. Both fields are placed in the descriptor ring in an AAL5 packet in the proper position (in the four bytes preceding the AAL5 32-bit CRC). These fields are not used if the packet is either in AAL3/4 or a null-AAL packet.

transmit BWG DMA block

The control memory on the PCI SAR contains 255 transmit BWG DMA entries, each containing eight words. The contents of each entry are summarized in the following table.

transmit BWG DMA entry table

ENTRY	DESCRIPTION	STATIC/DYNAMIC
Word 0	Control field, packet length, buffer length	Dynamic
Word 1	Current-buffer pointer – 32 bits	Dynamic
Word 2	4-byte ATM header	Dynamic
Word 3	Static bits – BWG ON/OFF (BWG_ON bit)	Static
Word 4	BWG data-ring pointer, descriptor pointer	Dynamic
Word 5	Reserved	Dynamic
Word 6	Partial 32-bit packet CRC	Dynamic
Word 7	AAL5 tail – control and length fields	Static

The PCI SAR initiates all transactions affecting the DMA table during normal operation based on cell-transmission opportunities from the BWG table. During initialization, the host has to configure word 0, word 3, and word 4 (shown in the transmit BWG DMA entry table) for each BWG selected for transmission in the BWG table including the BWG0. These words allow the TNETA1561 to start a transmission of a new packet. After configuration, the TNETA1561 reads word 3 to check if the BWG_ON bit is set. If it is set, the device reads word 0 to determine if the OWN bit is set. When the OWN bit is not set, it indicates that this is the first buffer of a new packet. The TNETA1561 then reads word 4 to obtain a transmit descriptor-ring pointer that indicates the memory address in host memory for the transmit descriptor-ring pointer. The following sections explain each TX DMA table word in detail.

TX DMA word 0 – state/configuration

Control (bits 31 – 27)	Current packet length (bits 26 –16)	Current buffer length (bits 15 – 0)

The contents of word 0 are copied directly from the corresponding transmit-data descriptor-ring entry at the start of each new buffer. This applies to all the fields in this status word, and the host must ensure consistency across the fields.

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OWN (bit 31)

The OWN bit is set when the DMA channel for the BWG is active, and all related state information in the DMA entry is current. The OWN bit indicates a packet is currently being segmented and transmitted for this BWG. This OWN bit is cleared by the PCI SAR after the entire packet is transmitted, a completion-ring entry is posted, and an interrupt is generated to the host.

The host sets the OWN bits for individual buffers in a packet in the transmit-data descriptor rings in order from last to first. This ensures that the DMA block is not held up while waiting to acquire the next buffer from a partially transmitted packet.

start of chain (SOC) (bit 30)

The SOC bit indicates that this is the first buffer of a packet which consists of one or more buffers. The SOC bit is also set in packets with single buffers. The SOC bit is cleared by the PCI SAR after all processing for the first buffer is complete.

end of chain (EOC) (bit 29)

The EOC bit indicates that this is the last buffer of a packet. Every packet has at least one buffer with the EOC bit set.

AAL-type – AAL5 indicator (bit 27)

The AAL-type bit is set to zero to indicate that the packet described in this descriptor-ring entry is an AAL5 packet. This bit is a configuration item rather than a bit carrying state information. This bit is set in every buffer of a packet, and the software driver must ensure that all the buffers in a packet use the same AAL type.

current-packet length (bits 26–16)

The PCI SAR increments this two's-complement value with every cell transmitted until the counter is equal to zero, which indicates to the PCI SAR that the entire packet has been transmitted.

current-buffer length (bits 15–0)

The buffer-length field specifies the number of remaining bytes in the buffer currently being processed in this BWG. The PCI SAR adds to the value of this two's-complement field with every transfer of payload data to the XMB until it is equal to zero, which indicates to the PCI SAR that all the bytes in this buffer are processed and queued for transmission.

TX DMA word 1 – current-buffer pointer

Byte-aligned current-buffer pointer (bits 31–0)

The current-buffer pointer is copied directly from the start-of-buffer pointer in the corresponding transmit-data descriptor-ring entry at the start of each new buffer. The field is 32 bits, which implies that the buffer is aligned to a byte boundary. The pointer is adjusted to point to the current location after each transfer of payload data from the host to the XMB.

TX DMA word 2 – ATM header

PTI (bits 31 – 29)	CLP (bit 28)	VPI (bits 27 – 20)	VCI (bits 19 – 4)	PTI (bits 3–1)	CLP (bit 0)

The 4-byte ATM header field is copied directly from the corresponding transmit-data descriptor entry at the start of each new packet. Bits (28–0) are concatenated to the 4-bit GFC field that is set to zero for every cell in the packet except the last one. Bits (31–28) provide the PTI and CLP fields in the last cell of each packet.

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TX DMA word 3 – configuration

BWG_ON (bit 31)	Unused (bits 30–0)

This bit allows the host to enable data transmission on a per-BWG basis. The BWG_ON bit from the current BWG index is examined by the PCI SAR on each cell opportunity. BWG_ON (31) is directly set by the host to indicate that the BWG is enabled, and that normal data processing is followed. If the bit is zero, no processing of transmit data on the BWG is performed and an idle cell is transmitted on the link. This idle cell is used by the host to respond to congestion indicators.

TX DMA word 4 – descriptor-ring address

TX-data descriptor-ring pointer (bits 31–12)	TX descriptor-ring entry (bits 11–4)	0000 (bits 3–0)

This pointer is a DMA address to the location of the current entry (there are 256 entries in each ring) in the corresponding transmit-data descriptor ring (one of 255 rings) for this BWG. Each descriptor ring is aligned to a 4K-byte boundary in host memory with each entry aligned to a 16-byte boundary.

The address of the 4K-byte boundary in host memory is provided by bits (31–12). The entry number between 0 and 255 is provided by bits (11–4). The low-order four bits are set to zero, and each entry is 16 byte aligned. Bits (11–0) are initialized by the host to zero to correspond with the first entry used by the host in the transmit-data descriptor ring.

TX DMA word 5 – reserved

Reserved

TX DMA word 6 – transmit CRC

Partial AAL5 transmit CRC (bits 31–0)

This field stores the 32-bit CRC calculated over the entire payload of each AAL5 packet. The CRC is placed in the last four bytes of the last cell of the corresponding packet.

TX DMA word 7 – AAL5 tail

AAL5 control field (bits 31 – 16)	AAL5 length field (bits 15 – 0)

The AAL5 control and length fields are copied directly from the corresponding transmit-data descriptor entry at the start of each new packet. The length field is not used for any control functions within the PCI SAR. Both fields are used exclusively for placement in the tail of an AAL5-protocol data unit (PDU).

transmit-completion ring

This entry contains only one word. The transmit-completion ring is a descriptor ring with 256 entries. The PCI SAR posts an item to the next entry in the completion ring when it completes the transmission of each packet. The transmit-completion ring pointer maintains the value of the current entry within the PCI SAR. The host can recalibrate to this by reading the value from the initialization block in control memory.

transmit-completion-ring summary

ENTRY	DESCRIPTION		
Word 0	OWN (bit 31)	Unused (bits 30–8)	BWG index (bits 7–0)

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TX-completion-ring word 0

OWN (bit 31)

This completion-ring entry is owned by the PCI SAR when the OWN bit is set. The completion-ring entry is owned by the host when the OWN bit is zero. The PCI SAR uses the next completion-ring entry in the ring if the OWN bit is set. The TNETA1561 clears the OWN bit after updating the entry. The host then receives an interrupt and retrieves the next entry in the completion ring to post the completion of packet transmission for a BWG and the release of the buffer space occupied by the buffers constituting the packet. The host then sets the OWN bit to allow the PCI SAR to use the completion-ring entry when it has queued a packet for transmission. If the OWN bit is not set when the PCI SAR is ready to post a completed packet, a status bit is set in the hardware-status register and an interrupt is generated if the error condition is unmasked.

BWG index (bits 7–0)

The only item that is posted to the transmit-completion ring when the PCI SAR completes transmission of a packet is the BWG index. This is adequate for the host to locate the transmit-buffer pointers to the buffer locations where data for the packet was stored and reclaim the buffer space.

receive free-buffer-ring format

There are two free-buffer rings. A receive free-buffer-ring entry consists of one word. Each of the two rings has 256 entries. The host places free-buffer pointers in the entries of each ring. The PCI SAR removes a pointer when it starts processing each new packet from the link.

receive free-buffer-ring summary

ENTRY	DESCRIPTION		
Word 0	OWN (bit 31)	Unused (bit 30)	Start-of-buffer pointer (bits 29–0)

RX free-buffer-ring word 0

OWN (bit 31)

Each free-buffer-ring entry is owned by the PCI SAR when the OWN bit is set and it is owned by the host when the OWN bit is zero. The host sets the OWN bit for new entries placed in the free-buffer rings. The PCI SAR uses the next free-buffer-ring entry in the respective ring if the OWN bit is set. The PCI SAR clears the OWN bit after acquiring the buffer and releasing the ring location to the host. The buffer is not freed until a packet is posted to the receive-completion ring. If the OWN bit is not set when the PCI SAR polls a free-buffer ring for a new entry, a status bit is set in the hardware-status register and an interrupt to host is generated if the error condition is unmasked.

start-of-buffer pointer (bits 29–0)

A pointer to a buffer, aligned to a 4-byte boundary, is the only information placed in each free-buffer ring.

receive DMA block

The PCI SAR supports 1024 receive DMA-channel entries with each containing eight words. Each DMA channel represents a VCI on which data is received, and DMA entries in the control memory are indexed by incoming VCIs. The PCI SAR initiates all transactions affecting the DMA table, except those required for one-time configuration of a channel in word 3, during normal operation based on the header of cells received from the link.

Data with the PTI field equal to 10X, representing VC-level OAM cells, is diverted to DMA channel 0 that operates in the null-AAL mode with a packet length of one cell. Word 0 in each receive DMA-channel entry is copied from word 3 at the start of each new packet. A number of the fields in word 0 represent the dynamic state of the reassembly process for a cell. The fields in word 3 represent one-time configuration values for the VC entered by the host. PCI SAR accesses word 0 during normal cell-level processing to retrieve configuration items.

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receive DMA-virtual-channel entry summary

ENTRY	DESCRIPTION	STATIC/ DYNAMIC
Word 0	Control, status, EFCN cell count, current packet length	Dynamic
Word 1	Current-buffer pointer – 28 bits	Dynamic
Word 2	Start-of-buffer pointer – 28 bits	Static
Word 3	Control, packet length	Static
Word 4	Reserved	
Word 5	AAL5 partial CRC – 32 bits	Dynamic
Word 6	Reserved	
Word 7	Reserved	

RX DMA word 0 – VC status/configuration

Control (bits 31–23)	Unused (bit 22)	Current congestion number (bits 21–11)	Current packet length (bits 10–0)

OWN (bit 31)

The OWN bit is set when the DMA channel for this BWG is active and all DMA parameters such as the receive-data pointer, buffer length, and packet length are current. The OWN bit is set by the PCI SAR when word 3 is copied to word 0 at the start of each new packet. The bit is cleared by the PCI SAR when the entire packet has been posted to a buffer in host memory. The BWG is inactive when the OWN bit is zero. Then, the free-buffer ring indicated in word 3 is used to poll a new buffer on the arrival of the first cell of a new packet on the VCI used to index this BWG.

static-configuration bits from word 3

The next summary lists five static-configuration bits copied from word 3 at the start of each packet. Each is described in detail in the section on RX DMA word 3.

RX DMA word 0 static-configuration bit summary

LOCATION	FIELD
Bit 31	OWN
Bit 30	VCON
Bit 29	Buffer type: small or big
Bit 28	Null-AAL indication
Bit 25	AAL3/4 indication
Bit 24	End-of-packet wait
Bit 23	Enable end-of-packet wait

explicit forward congestion notification (EFCN) cell counter (bits 21–11)

The number of cells received with the EFCN indicator set in each packet is counted and the value is stored in this field. The EFCN indication is given a logic value of 01x in the PTI field of the ATM header. This value is passed to the receive-completion ring at the end of each packet. Since this field is copied from word 3 at the start of each new packet, it is reset to zero at this time.

packet length (bits 10–0)

The packet-length field in word 0 is set up with the two's-complement value for the buffer size used by this BWG at the start of each new packet. The counter is incremented with each new cell until the EOP signal or the value is zero. Null-AAL packets are terminated when the value of this counter reaches zero. If either the AAL5 or AAL3/4 packet fills the buffer to capacity, the counter reaches zero and the packet is terminated with the buffer-overflow indicator set in the receive-completion-ring entry.

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RX DMA word 1 – current-buffer pointer

Unused (bits 31–28)	Current-buffer pointer – 16 byte aligned (bits 27–0)

The current-buffer pointer is 28 bits, which implies that the buffer is aligned to 16-byte boundaries. This is a dynamic field that is updated with every RCB-to-PCI-bus transaction.

RX DMA word 2 – start-of-buffer pointer

Unused (bits 31–30)	Start-of-buffer pointer – 4 byte aligned (bits 29–0)

The start-of-buffer pointer is 30 bits because the buffer is aligned to 4-byte boundaries. This field is copied from the corresponding 30-bit field in word 0 of a free-buffer-ring entry.

RX DMA word 3 – configuration

Configuration (bits 31–23)	Unused (bits 22–11)	Null-AAL packet length (bits 10–0)

OWN bit position (bit 31)

The OWN bit is set high for each valid receive channel. It is copied into the corresponding OWN bit location in word 0 at the start of each new packet to indicate that the DMA channel is active. This OWN bit is automatically reset to a 0 after the end-of-packet indicator is received.

VC_ON (bit 30)

The VC_ON bit enables packet-reassembly processing. The bit is set in the default mode to indicate that the VC is enabled. The PCI SAR discards cells received on the corresponding VC when the VC_ON bit is deasserted on a per-cell basis.

buffer type – small or big (bit 29)

The PCI SAR supports only two buffer sizes on receive: small and big. The host determines the sizes of the small and big buffers. The buffer-type bit is used to select between a buffer pointer from the small free-buffer ring or the big free-buffer ring for each new packet, which allows the host to target small or big buffers for all packets on a given VC. The small free-buffer ring is used when the bit is set, and the big free-buffer ring is used in the default (zero) state.

null-AAL indication (bit 28)

This field is set to indicate that null-AAL packets are received on this BWG (VC). The null-AAL packet-length field in bits (10–0) is used to determine the end of a packet. CRC errors are ignored for null-AAL packets. The CRC-error indicator in the receive-completion ring is not used.

AAL3/4 indication (bit 25)

This field is set to indicate that AAL3/4 packets are received on this BWG (VC). This indicates the EOM field in byte 6 (bit 6 of an ATM cell is used as the EOP indicator). CRC errors are ignored for AAL3/4 packets. The CRC-error indicator in the receive-completion ring is not used.

end-of-packet wait (bit 24)

This bit must be set to zero by the device driver during initialization. This gives the SAR the responsibility of setting it to one in DMA word 0 (when this feature is enabled). This bit is a status bit used by the TNETA1561 during operation.

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enable end-of-packet wait (bit 23)

When a start of a packet is detected by the TNETA1561, the TNETA1561 requests a buffer from the host memory. If the buffer is not available, the first cell of this packet is dropped. The rest of the packet is dropped after it is received. The host can set bit 23 to 1 to enable the TNETA1561 to drop the cells of a packet that had the first cell dropped. Once the TNETA1561 detects the end packet, it begins to receive packets in this VCI. This feature only works for AAL5 and ALL3/4. For null-AAL and OAM cells, bit 23 must be set to zero.

EFCN cell-counter place holder (bits 21–11)

This field is set to zero since it is a place holder for the EFCN cell counter in word 0 of this DMA block.

AAL-packet length (bits 10–0)

The AAL-packet-length field in word 3 indicates the length of the buffer in cells for each packet in this BWG. This is used in different ways based on whether the BWG supports AAL5 or AAL3/4 packets or null-AAL packets. This field indicates the length of the buffer size allocated by entries in the free-buffer ring used by this BWG for AAL5 or AAL3/4 packets. This is used to detect buffer overflow.

When the null-AAL indicator is set, this field programmed in two's-complement notation represents the number of cells in each null-AL packet. Since receive DMA channel 0 operates off the null-AAL mode with each packet size equal to one cell, this field is programmed with the value one in two's-complement notation (7FFhex).

RX DMA word 5 – AAL5 partial CRC)

Partial AAL5 receive CRC (bits 31–0)

This field stores the 32-bit CRC that is calculated over the entire payload of each received AAL5 packet. The CRC is stored in the last four bytes of the last cell in the AAL5 frame. The CRC check results in a unique polynomial.

receive-completion ring

The following table shows the composition of a 4-word receive-completion-ring entry. The receive-completion ring has 256 entries. The PCI SAR posts an item to the next entry in the completion ring when it completes reassembly on a packet. The receive-completion-ring pointer maintains the value of the current entry within the PCI SAR. The host can recalibrate to this by reading the value from the initialization section in control memory.

receive-completion-ring summary

ENTRY	DESCRIPTION
Word 0	Reserved
Word 1	Start-of-buffer pointer – 28 bits
Word 2	4-byte ATM header
Word 3	Control field, EFCN cells received, packet length

RX completion-ring word 0 – reserved

This word is not used or defined.

RX completion-ring word 1 – start-of-buffer pointer

Unused (bits 31–28)	Start-of-buffer pointer – 16 byte aligned (bits 27–0)

The 28-bit start-of-buffer pointer is provided to the host in the RX completion ring to enable it to locate the reassembled packet.

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RX completion-ring word 2 – ATM header

ATM header byte 1	ATM header byte 2	ATM header byte 3	ATM header byte 4

The 4-byte header from the last cell in the reassembled packet is passed to the host.

RX completion-ring word 3 – control

Control (bits 31–29)	Unused (bits 28–22)	Congestion cells received (bits 21–11)	Packet length (bits 10–0)

OWN (bit 31)

This completion-ring entry is owned by the PCI SAR when the OWN bit is set and it is owned by the host when the OWN bit is zero. If the OWN bit of the next entry in the respective receive-completion ring is zero when the PCI SAR polls it to post the completion-of-packet processing, an error indicator in the status register is set and an interrupt is generated. This causes the buffer that the PCI SAR attempted to post to be lost. The PCI SAR clears the OWN bit in the receive-completion ring after it posts the packet. The host then owns the entry and may retrieve various pointers to the packet.

packet overflow (bit 30)

The packet-overflow bit is set if the receive buffer overflowed while processing the current packet. Every packet that ends in a buffer overflow is immediately terminated and a completion-ring entry is posted to the host.

CRC condition (bit 29)

The PCI SAR forwards AAL5 packets with a CRC error to the host. This bit is set when a packet is received with an AAL CRC error.

congestion cells received (bits 21 – 11)

The number of cells received in the packet with the EFCN indication set is forwarded to the host to implement associated feedback mechanisms to squelch the source.

packet length (bits 10 – 0)

All received data is passed to the host in units of 48 bytes. The packet length in 48-byte payload units from word 0 of the receive DMA block is passed to the host in twos-complement notation. This value is always zero for null-AAL packets. The length of an AAL5 or AAL3/4 packet in integer units is obtained by subtracting this value from the reassembly-buffer length reserved for the packet.

registers

The PCI SAR has defined two types of registers: the PCI configuration-space registers and control and status registers. The PCI-SAR internal registers have a PCI bus physical-address base value read from BASE REG 0 of the PCI configuration space. This section describes several host-accessible internal PCI-SAR registers. Host-write accesses to nonexistent registers are ignored. A null word (32 zeros) is returned to the host on a read access from a nonexistent register.

- PCI SAR configuration-space registers:
  These registers are initialized by the system-initialization procedure (BIOS device-initialization routine) to program the operation of the PCI SAR device with a PCI-bus interface.
- PCI SAR control and status registers:
  These registers provide PCI SAR device status and control information.

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TNETA1561 configuration-space registers

The TNETA1561 supports the 64-byte header that is defined by the PCI specification revision 2.0. None of the device-specific registers in locations 64–255 are used. The predefined header region has a size of 64 bytes. The layout of the PCI configuration-space registers is shown below.

ADDRESS	BYTE 3	BYTE 2	BYTE 1	BYTE 0	READ/WRITE
0x00	Device ID		Vendor ID		R
0x04	Status		Command		R/W
0x08	Class code			Revision ID	R
0x0C	BIST	Header type	Latency timer	Cache line size†	R/W
0x10	Base address 0				R/W
0x14	Base address 1†				R/W
0x18	Base address 2†				R/W
0x1C	Base address 3†				R/W
0x20	Base address 4†				R/W
0x24	Base address 5†				R/W
0x28	Reserved (returns 0 when read)				
0x2C	Reserved (returns 0 when read)				
0x30	Expansion ROM base address				R/W
0x34	Reserved (returns 0 when read)				
0x38	Reserved (returns 0 when read)				
0x3C	Maximum latency	Minimum grant	Interrupt pin	Interrupt line	R/W
0x40	Reserved (returns 0 when read)				
0x44–0xFF	Reserved (returns 0 when read)				R

† Registers not implemented and return 0

The PCI configuration-space registers are accessible only by PCI-configuration cycles. All multibyte numeric fields follow little-endian byte format.

vendor-ID register (offset address 00h)

The vendor-ID register is a 16-bit register that identifies the manufacturer of the TNETA1561. The Texas Instruments (TI) vendor ID is 104C. The vendor ID is assigned by the PCI special interest group. The vendor-ID register is located at offset address 00h in the PCI configuration space and is read only.

device-ID register (offset address 02h)

The device-ID register is a 16-bit register that uniquely identifies the TNETA1561 device within TI's product line. The device ID is assigned by TI and is not the same as the device part number. The device-ID register is located at offset address 02h in the PCI configuration space and is read only.

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command register (offset address 04h)

The command register is a 16-bit register that provides coarse control for the device functionality to generate and respond to PCI-bus cycles.

The command register is located at offset address 04h in the PCI configuration space. It is read and written by the host. The bit definition is given below:

- Control bit 0 = I/O space
- Control bit 1 = memory space
- Control bit 2 = bus master
- Control bit 3 = special cycle operations
- Control bit 4 = memory write and invalidate enable (this bit is set according to the requirements of PCI SAR).
- Control bit 5 = VGA palette snoop (this bit always returns 0).
- Control bit 6 = parity-error response
- Control bit 7 = wait cycle control (this bit is hardwired to 0).
- Control bit 8 = $\overline{\text{PSERR}}$ enable
- Control bit 9 = fast back-to-back enable
- Control bit 10 = bit 15 = reserved

status register (offset address 06h)

The status register is a 16-bit register that contains status information for the PCI-bus related events. The status register is located at offset address 06h in the PCI configuration space. The bit definition is given below:

- Status bit 0–6 = reserved
- Status bit 7 = fast back-to-back enable
- Status bit 8 = data parity reported
- Status bit 9–10 = DEVSEL timing (the PCISLV decode logic supports medium DEVSEL timing and these bits return 01).
- Status bit 11 = signaled target abort
- Status bit 12 = received target abort
- Status bit 13 = initiated master abort (the PCIMST logic sets this bit to a 1 when it generates a master abort).
- Status bit 14 = signaled-system error
- Status bit 15 = detected-parity error

revision-ID register (offset address 08h)

The revision-ID register is an 8-bit register that specifies a device-specific revision-identifier number. The current value of the register is 00h. The revision ID register is located at offset address 08h in the PCI configuration space and is read only.

class-code register (offset address 09h)

The class-code register is a 24-bit register that specifies the generic function of the device. The class code register is located at offset address 09h in the PCI configuration space and is read only.

cache line-size register (offset address 0Ch)

The PCIMAC supports write and invalidate as a master. The host writes the cache line size into this byte-wide register.

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

latency-timer register (offset address 0Dh)

The latency-timer register is an 8-bit register that specifies the maximum time TNETA1561 device can continue with bus-master transfers. The PCIMAC supports a burst of more than one data cycle. The host sets the latency requirements of the system in this register in PCI-bus clock units. When the current-time value (00h) stored in the latency-timer register expires, the TNETA1561 immediately releases the bus after finishing the current data phase.

header-type register (offset address 0Eh)

The header-type register is an 8-bit register that describes the format of the PCI configuration-space locations 10h to 3Ch. The header defined here is referred to as type 0. The header-type register is located at offset address 0Eh in the PCI configuration space and is read only.

built-in self-test register (BIST) (offset address 0Fh)

BIST is not supported by the PCI SAR. Reading this register returns 0.

base-address register 0 (offset address 10h)

Base register 0 (32 bits)	Host-memory address block for direct control-memory mapping	Read only by PCI SAR Read and write by host

Base-address register 0 is a 32-bit register. The base-address registers provide the base address of the control-memory blocks mapped into host memory. The complete address is the sum of base and offset addresses. The base address is written by the host during power-on reset time. The typical format for the base-address register is given below:

- Bit (0) = 0, memory-space indicator
- Bit (2–1) = 00, locate anywhere in 32-bit address space
  01, locate below 1M byte
  10, locate anywhere in 64-bit space
  11, reserved
- Bit (3) = 0 (set to 1 only for prefetching)
- Bit (31–4) = 28-bit address

Base-address register 0 defines the starting address of the direct mapping of control memory and internal registers in host memory.

expansion ROM base-address register (offset address 30h)

EPROM base register (32 bits)	Host-memory address block for EPROM	Read only by host

The expansion ROM base-address register is a 32-bit register. The EPROM register defines the starting address of the external EPROM mapped in the host memory. The expansion ROM base-address format is given below:

- Bit (0) = 1 enable EPROM
- Bit (10–1) = reserved
- Bit (31–11) = expansion EPROM base address

Bits (31 – 16) are read-only bits. These bits are written by the host after initialization to allocate the memory block in the host memory for mapping EPROM. The remaining bits (15 – 0) are hardwired to zero. This allows EPROM addressing up to a maximum size of 64K bytes.

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

interrupt-line register (offset address 3Ch)

The interrupt-line register is an 8-bit register that is used to communicate the routing of the interrupt. This register is written by the HOST software during system initialization. The value in this 8-bit register indicates which input of the system-interrupt controller is connected to the PCI-SAR interrupt terminal. The typical value is between 0 and 15. The interrupt-line register is located at offset address 3Ch in the PCI configuration space and is read and written by the host.

interrupt-pin register (offset address 3Dh)

The interrupt-pin register is an 8-bit register indicating the interrupt pin that the TNETA1561 is using. The PCI SAR is defined as a single-function device, uses only interrupt A, and has a value of 1. The interrupt-pin register is located at offset address 3Dh in the PCI configuration space and is read only.

minimum-grant register (offset address 3Eh)

The minimum-grant register is an 8-bit register that specifies the length of the data burst required by the TNETA1561 for every PCI-bus grant. This specifies the length of the burst period that the PCI-SAR device needs in 0.25-µs units. The typical value of 0.75 µs (decimal 3) is defined for PCI SAR. The minimum-grant register is located at offset address 3Eh in the PCI configuration space.

maximum-latency register (offset address 3Fh)

The maximum-latency register is an 8-bit register that defines the maximum latency value for the PCI SAR. This specifies how often the PCI-SAR gains access to PCI bus in 0.25-µs units. A typical value of 10 µs (decimal 40) is defined for PCI SAR. The maximum-latency register is located at offset address 3Fh in the PCI configuration space.

PCI-SAR control and status registers

The PCI SAR has defined the following registers for status and control information.

OFFSET ADDRESS (24 BIT HEX)	DESCRIPTION	WIDTH IN BITS	READ/WRITE
00E000	Software reset	32	Write only
00E004	SAR-status register	32	Read only
00E008	Interrupt-enable mask register	32	Read/write
00E010	Reserved	32	—
00E00C	SAR-configuration register	32	Read/write
00E014	BWG-table-size register	32	Read/write
00E018	Transmit/receive FIFO maximum-depth register	32	Read/write
00E01C	Reserved	32	—
00E020	Clear-transmit-freeze command	32	Write only
00E024	Clear-receive-freeze command	32	Write only

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

PCI-SAR-status register (offset address 00E004)

The PCI-SAR-status register is read only for the host. All the bits, except the transmit-freeze bit and the PCI-bus error flags, are cleared when the register is read. PCI SAR generates a PCI-bus interrupt to the host if one of the bits in the register is set and if the condition represented by the bit is enabled by the interrupt-enable mask register. The PCI-bus interrupt is an asynchronous signal that is held until the system clears the condition that caused the interrupt. The bit format is shown in following table:

ADDRESS PARITY ERROR (BIT11)	TARGET REPORTED PARITY ERROR (BIT10)	RETRY COUNT EXPIRED (BIT9)	LOCAL-BUS INTERRUPT (BIT 8)
Receive freeze (bit 7)	Transmit freeze (bit 6)	Transmit completion not available (bit 5)	Receive completion not available (bit 4)
Receive big-free buffer not available (bit 3)	Receive small-free buffer not available (bit 2)	Transmit completion update (bit 1)	Receive completion update (bit 0)

transmit completion update and receive completion update (bits 1–0)

The transmit or receive completion update bit is set when the hardware releases a transmit or receive descriptor, respectively, to the completion ring. This is initiated when the OWN bits in the respective DMA blocks are cleared by TNETA1561.

receive big free-buffer not available and receive small free-buffer not available (bits 3–2)

The appropriate receive free-buffer not-available bit is set when the first entry in the corresponding receive free-buffer ring is not available. This is indicated when the OWN bit in the first entry of the free ring is zero. The incoming cell is deleted because there is no buffer available to hold it. This eventually causes the loss of the entire packet due to the resultant CRC error. The buffer allocation-error bit in the DMA block is set. This is indicated by a zero in the first free-buffer ring entry.

receive completion-ring not available (bit 4)

The receive completion-ring not-available bit is set when the next descriptor in the receive completion ring is not released by the host. This is indicated when the OWN bit in the entry is zero (host owns it). This packet and buffer are both lost to host memory.

transmit completion-ring not available (bit 5)

The transmit completion-ring not-available bit is set when the next descriptor in the receive completion-ring is not released by the host. This is indicated when the OWN bit in the entry is zero. The transmit-freeze bit is set when this bit is set, disabling all transmit operation until the transmit-freeze bit is cleared via an active command from the host.

transmit freeze (bit 6)

The transmit-freeze bit is set when the transmit completion-ring not-available bit is set, disabling all transmit operation until the transmit-freeze bit is cleared via an active command from the host. This has the same effect on the transmit circuitry as disabling the transmit-enable bit.

receive freeze (bit 7)

The receive-freeze bit is set when the receive completion-ring not-available bit is set, disabling all receive operation until the receive-freeze bit is cleared via an active command by the host. The buffer that could not be posted is effectively lost, and the host must find some way to recover it while the freeze is in operation. The receive-freeze indicator has the same effect on the receive path as disabling the receive-enable bit.

PRINCIPLES OF OPERATION

local-bus interrupt (bit 8)

The local-bus interrupt bit is set if an interrupt is generated on the local bus.

retry count expired (bit 9)

The retry count expired is set to a 1 logic state when the macro exceeds the maximum retry count with a master transaction. This bit is set to a 0 logic state after reset.

target-reported parity error (bit 10)

The target-reported parity error is set to a 1 logic state when the macro receives a data-parity error (receives $\overline{\text{PERR}}$ during a master write or detects a parity error during master read). This bit is set to a 0 logic state after reset.

address-parity error (bit 11)

The address-parity error is set to a 1 logic state when the macro is a PCI target and detects an address parity (target). This bit is set to a 0 logic state after reset.

interrupt-enable mask register (offset address 00E008)

Unused (bits 31–12)	Mask bits (bits 11–0)

An interrupt-enable mask-register bit has a bit that corresponds to every entry in the PCI-SAR status register. When a bit is set in the status register, an interrupt is generated if a corresponding bit in the status register is also set.

SAR-configuration register (offset address 00E00C)

The SAR-configuration register holds various values pertaining to the overall PCI-SAR configuration. The host can read the register and is allowed to program the EN receive and the EN transmit bits. In addition, two more bits are defined for posted write-buffer enable (PWBE) and software reset (SR).

Unused (bits 31–5)	SDH (bit 5)	Unused (bits 4–3)	EN receive (bit 2)	EN transmit (bit 1)	0 (bit 0)

enable-transmit operation (EN transmit) (bit 1)

The EN-transmit bit allows the host to disable packet-to-cell segmentation and any payload-data transfer from the host to the link. The EN-transmit bit is set high to enable normal transmit processing and set to zero to disable such processing. The EN-transmit bit is set to zero on reset, disabling transmit operation until various configuration registers, the BWG table, and DMA blocks are configured by the host. The transfer of the new cells from PCI bus to PCI SAR is inhibited when the enable-transmit bit is disabled. Cells already in the output buffer are forwarded to the PHY layer.

enable-receive operation (EN receive) (bit 2)

The EN-receive bit allows the host to disable packet reassembly. All cells from the PHY layer are dropped when the EN-receive bit is zero. The EN-receive bit is set high to enable normal processing and is set to zero on reset, disabling receive operation until various configuration registers and the DMA blocks are reconfigured by the host. The transfer of new cells from the ATM link to the receive buffer is inhibited when the enable-receive bit is disabled.

SDH bit (bit 5)

If the SDH bit is set to 0, the TNETA1561 transmits null cells (unassigned cells) when no valid cells are ready for transmission. If SDH bit is set to 1, the device transmits idle cells as fillers.

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

BWG table-size register (offset address 00E014)

Unused (bits 31–11)	BWG table size (bits 10–0)

The 11-bit BWG table-size register allows the user to configure the size of the BWG table in 4-byte words. Each word in the table consists of four 8-bit entries. The maximum table size is 1200 (decimal) allowing 4800 entries. A resolution of 32 kbit/s is achieved with 4800 entries. The number of entries in the table is one more than the number programmed in this register, and there is one entry in the table when the register is set to zero.

transmit/receive FIFO maximum-depth register (offset address 00E018)

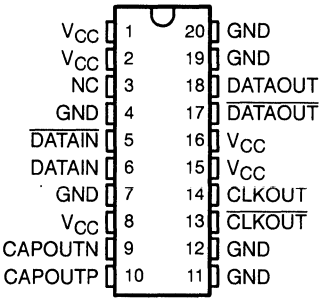
Unused (bits 31–20)	Maximum receive FIFO depth (bits 19–10)	Maximum transmit FIFO depth (bits 9–0)

This is the only set of statistics collected by the TNETA1561 because it is useful information for queuing analysis in different platforms with varying PCI-bus clock speeds and latencies. These registers are not of the read and reset variety and must be set to zero to restart the measurement.

SDNS017B – FEBRUARY 1994 – REVISED DECEMBER 1994

- **Recovers a 622.08-MHz Clock Signal From a 622.08-Mbit/s STS-12/STM-4 NRZ Data Stream**
- **Accepts Pseudo-ECL (PECL) Input Voltage Levels on the Input Data Stream**
- **Requires a Single 5-V Supply**
- **Provides PECL-Clock and PECL-Data Outputs**

DW PACKAGE
(TOP VIEW)



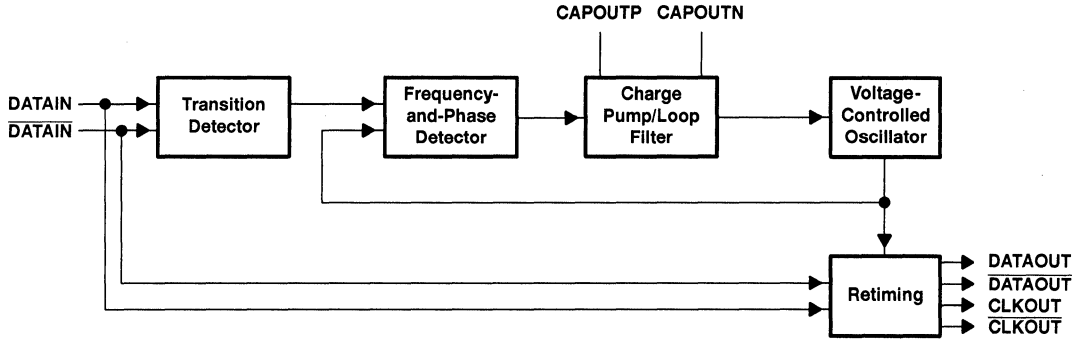
NC – No internal connection

description

The TNETA1622 recovers an embedded clock signal from a 622.08-Mbit/s STS-12/STM-4 nonreturn-to-zero (NRZ) data stream using a frequency/phase-locked loop. The device accepts PECL (ECL signals referenced to 5 V instead of GND) input-voltage levels. The recovered clock and data outputs are PECL compatible. The serial data input and recovered clock and data outputs are differential to provide maximum noise immunity.

The TNETA1622 requires only a positive 5-V supply (5 V ± 5%) for operation. The TNETA1622 is specified for operation over a temperature range of –40°C to 85°C.

functional block diagram



PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CAPOUTN CAPOUTP	9 10	I	Capacitor connection for phase-locked-loop filter
$\overline{\text{CLKOUT}}$ CLKOUT	13 14	O	Recovered clock output, PECL compatible
$\overline{\text{DATAIN}}$ DATAIN	5 6	I	Serial data input, PECL compatible
$\overline{\text{DATAOUT}}$ DATAOUT	17 18	O	Serial data output, PECL compatible
GND	4, 7, 11, 12, 19, 20		Ground (0-V reference)
V_{CC}	1, 2, 8, 15, 16		Supply voltage
NC	3		No connection. Leave floating (open).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range, PECL ..... 0 V to 7 V
Power dissipation ..... 562 mW
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	PECL (see Note 2)	$V_{CC}-1.1$		$V_{CC}-0.8$	V
V_{IL}	Low-level input voltage	PECL (see Note 2)	$V_{CC}-1.9$		$V_{CC}-1.5$	V
T_A	Operating free-air temperature		−40		85	°C

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.

PRODUCT PREVIEW

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (see Figure 1)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	CLKOUT, $\overline{\text{CLKOUT}}$, DATAOUT, $\overline{\text{DATAOUT}}$	V_{CC} = 4.75 V to 5.25 V, See Notes 2 and 3	$V_{CC}-1.03$	$V_{CC}-0.85$	V
V_{OL}	Low-level output voltage	CLKOUT, $\overline{\text{CLKOUT}}$, DATAOUT, $\overline{\text{DATAOUT}}$	V_{CC} = 4.75 V to 5.25 V, See Notes 2 and 3	$V_{CC}-1.85$	$V_{CC}-1.62$	V
I_{IH}	High-level input current	DATAIN, $\overline{\text{DATAIN}}$	V_{CC} = 5.25 V, V_I = 4.45 V			µA
I_{IL}	Low-level input current	DATAIN, $\overline{\text{DATAIN}}$	V_{CC} = 5.25 V, V_I = 3.35 V			µA
I_{CC}	Supply current		V_{CC} = 5.25 V, f = 622.08 Mbit/s, Outputs open		107	mA
			V_{CC} = 5.25 V, f = 622.08 Mbit/s, See Note 4		107	

NOTES: 2. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.
3. These outputs are terminated through a 50-Ω resistor to V_{CC} –2 V.
4. CLKOUT, $\overline{\text{CLKOUT}}$, DATAOUT, and $\overline{\text{DATAOUT}}$ each are terminated with a 50-Ω resistor to V_{CC} –2 V.

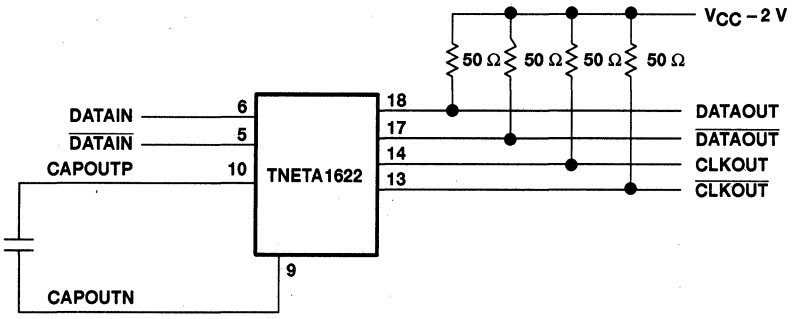
operating characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Acquisition time	See Note 5				ms
Deviation of clock sampling point, t_{csp}	See Figure 1				ps
RMS jitter, recovered clock	See Note 6				°RMS
Input data rate			622.08		Mbit/s
Duty cycle, recovered clock	See Note 3	45%		55%	
Maximum number of consecutive bits (1 or 0) in input data stream	See Note 7				

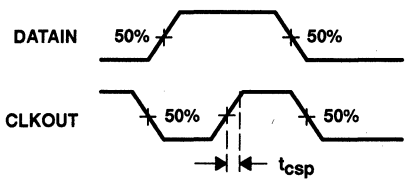
NOTES: 3. These outputs are terminated through a 50-Ω resistor to V_{CC} – 2 V.
5. Acquisition time is the time required to achieve a valid clock output while applying a 2^7 – 1 pseudo-random bit sequence.
6. RMS jitter is measured with a 2^{31} – 1 pseudo-random bit sequence.
7. This measurement is made with a 2^{13} – 1 pseudo-random bit sequence with string substitution.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

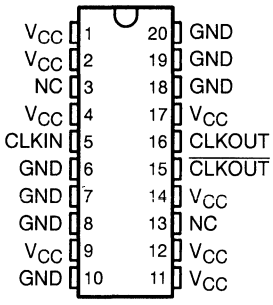
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

- **Generates a 622.08-MHz Clock From a TTL Clock of 19.44 MHz**
- **Provides Differential Pseudo-ECL (PECL) Outputs**
- **Operates From a Single 5-V Power Supply**
- **Packaged in 20-Pin Plastic Small-Outline (DW) Package**

DW PACKAGE
(TOP VIEW)

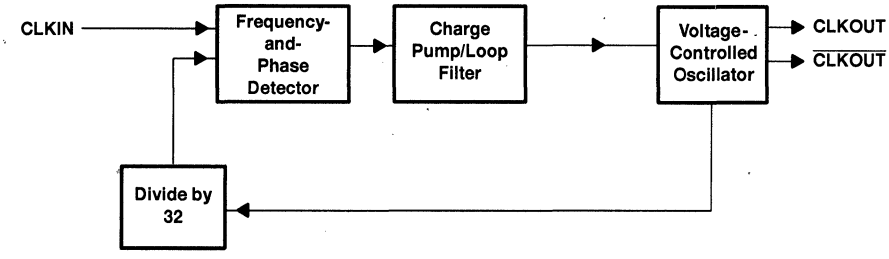


NC – No internal connection

description

The TNETA1630 is a 622.08-MHz clock-generation device that utilizes a TTL clock input at 19.44 MHz. The 622.08-MHz clock is provided on differential pseudo-ECL (PECL) outputs. The TNETA1630 operates from a single 5-V power supply. An internal second-order low-pass filter is used to reduce jitter.

functional block diagram



PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLKIN	5	I	19.44-MHz TTL-input clock
CLKOUT	16	O	622.08-MHz PECL-output clock true
$\overline{\text{CLKOUT}}$	15	O	622.08-MHz PECL-output clock complement
GND	6, 7, 8, 10, 18, 19, 20		Ground (0-V reference)
V_{CC}	1, 2, 4, 9, 11, 12, 14, 17		Supply voltage
NC	3, 13		No connection (leave floating)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range ..... −1.2 V to 7 V
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

PRODUCT PREVIEW

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	TTL (see Note 2)	2			V
V_{IL}	Low-level input voltage	TTL (see Note 2)			0.8	V
I_{IK}	Input clamp current	TTL			−18	mA
T_A	Operating free-air temperature		−40		85	°C

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage, PECL	V_{CC} = 4.75 V to 5.25 V,	See Notes 2 and 3	V_{CC} −1.03	V_{CC} −0.88	V
V_{OL}	Low-level output voltage, PECL	V_{CC} = 4.75 V to 5.25 V,	See Notes 2 and 3	V_{CC} −1.85	V_{CC} −1.62	V
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_L = −18 mA		−1.2	V
I_I	Input current, TTL	V_{CC} = 5.25 V,	V_I = V_{CC} or GND		−1	µA
I_{CC}	Supply current	V_{CC} = 5.25 V, Outputs open	f = 622.08 MHz,		50	mA
		V_{CC} = 5.25 V, See Note 4	f = 622.08 MHz,		50	

NOTES: 2. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.
3. These outputs are terminated to V_{CC}−2 V.
4. These outputs are terminated with a 50-Ω resistor to V_{CC}−2 V.

operating characteristics over recommended operating free-air temperature range (unless otherwise noted)

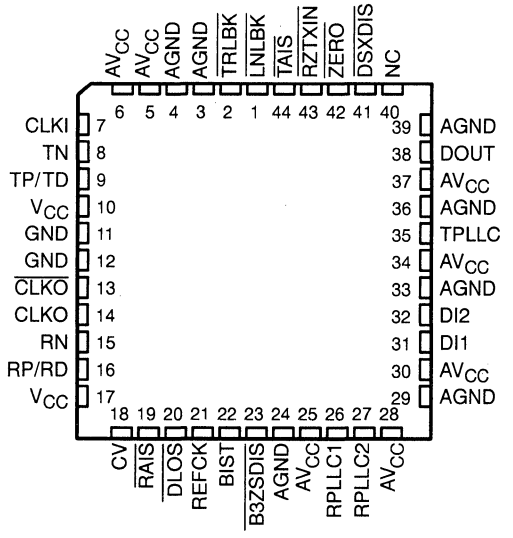
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Duty cycle, generated clock	See Note 4				
RMS jitter, recovered clock	See Note 5				°RMS

NOTES: 4. These outputs are terminated with a 50-Ω resistor to $V_{CC}-2$ V.
5. RMS jitter is measured with a $2^{31}-1$ pseudo-random bit sequence.

SDNS006C – APRIL 1992 – REVISED DECEMBER 1994

- Member of Texas Instruments Line of Standard DS-3 and SONET Devices
- Provides the Functions Necessary to Receive and Transmit a DS-3 or STS-1 Signal Including:
  - Selectable B3ZS Codec and Corresponding P- and N-Rail Inputs/Outputs or Combined NRZ Input/Output
  - On-Chip Clock Recovery
  - Loss-of-Signal Detection and DS-3 Alarm-Indication-Signal (AIS) Generation
- Adaptive-Equalizer and AGC Circuits Help Recover Attenuated DS-3/STS-1 Signals
- Provides Both Terminal-Side and Line-Side Loopbacks
- Meets the Applicable ANSI, Bellcore, and CCITT Standards:
  - ANSI T1.102-1989
  - TR-TSY-000499 Issue 3, Dec 1989
  - TR-TSY-000191 Issue 1, May 1986
  - TR-NWT-000253 Issue 6, Sept 1990
  - CCITT Rec. G.703, 1985
- Packaged in 44-Pin Plastic Leaded Chip Carrier

FN PACKAGE
(TOP VIEW)



NC – No internal connection

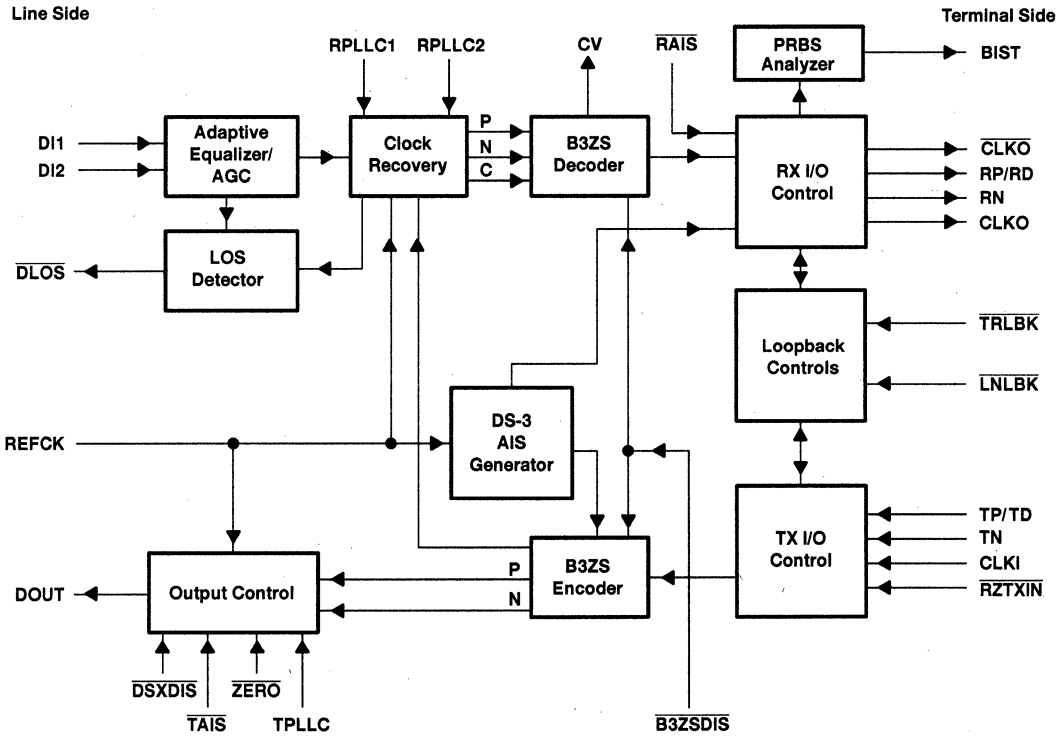
description

The TNETS2020A provides the functionality required to transmit and receive a DS-3 or STS-1 line signal. The device requires a minimum of external passive components (resistors and capacitors) for the on-chip phase-locked loops and line terminations. The device includes AGC and adaptive-equalizer circuits that help recover attenuated DS-3/STS-1 signals and an analog phase-locked loop to recover the imbedded clock signal from the incoming serial-data stream. The device also includes the filtering and processing required to meet the ANSI and Bellcore DS-3 and STS-1 pulse templates and eye patterns.

The TNETS2020A provides an optional B3ZS codec that converts the DS-3/STS-1 line code to an NRZ digital format and vice versa. When the B3ZS codec is bypassed, the device provides (accepts) P- and N-rail outputs (inputs). A high on the P-rail I/O represents a bipolar + 1 and a high on the N-rail I/O represents a bipolar – 1. This feature is useful for applications where the B3ZS codec is implemented in a corresponding framer device. The TNETS2020A also provides loss-of-signal detection, alarm-indication-signal (AIS) generation, and line-side and terminal-side loopback capability.

PRODUCT PREVIEW

functional block diagram



detailed description

line-side bipolar data to terminal-side digital data

The TNETS2020A accepts a bipolar line-side signal with a rate of 44.736 or 51.84 Mbit/s and converts the signal to one of two digital data formats depending upon the state of $\overline{\text{B3ZSDIS}}$. If $\overline{\text{B3ZSDIS}}$ is high, the B3ZS codec is enabled and NRZ data is sent to RP/RD. RN in this state is held at a low level. If $\overline{\text{B3ZSDIS}}$ is low, the B3ZS codec is disabled and the data is sent to both RP/RD and RN. RP/RD is high when a positive pulse occurs on the incoming bipolar signal, and RN is high when a negative pulse occurs. In both cases, the recovered clock signal appears on CLKO and $\overline{\text{CLKO}}$, where $\overline{\text{CLKO}}$ is an inverted version of CLKO.

The TNETS2020A line-side input contains an adaptive equalizer and AGC circuit. This circuit provides the necessary gain and pulse shaping to recover DS-3/STS-1 signals transmitted over coaxial cable. The input signal should conform to the DSX-3 pulse as defined in T1.102 or the STSX-1 pulse defined in TR-NWT-000253 Issue 2, December 1991, when driven over zero to 450 feet of AT&T 728A/734A coaxial cable (or the equivalent) with an additional flat loss of 20 dB maximum. The maximum input level is 1-V peak.

The line-side inputs to the TNETS2020A operate in either differential or single-ended mode. For differential-mode operation, both inputs are used. For single-ended mode operation, either input can receive the line signal with the other input connected to GND through a capacitor (see Figure 1).

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line-side bipolar data to terminal-side digital data (continued)

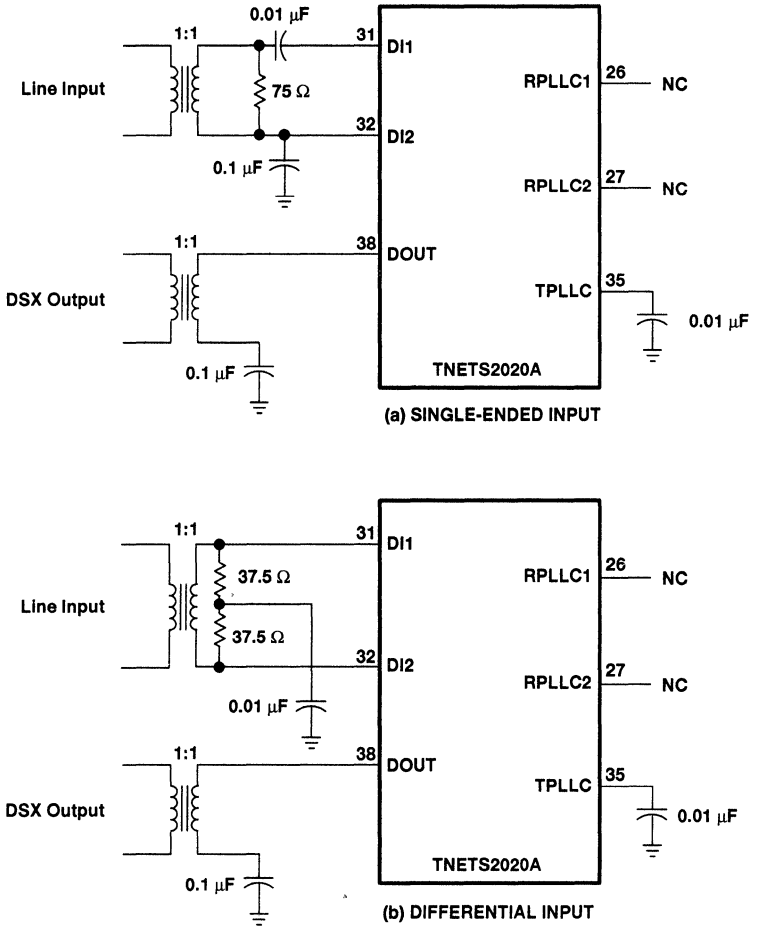

Figure 1. External Component Connections

The TNETS2020A uses a phase-locked loop (PLL) to recover the clock signal from the incoming bipolar line signal. REFCK is used to calibrate the PLL and requires an input signal with a frequency of 44.736 MHz ±200 ppm for DS-3 operation. A tolerance of ±20 ppm is required for a DS-3 AIS signal. For STS-1 operation, a clock frequency of 51.84 MHz ±200 ppm is required. The data output from the clock-recovery circuit consists of two signals representing the positive and negative pulses of the bipolar signal. If the B3ZS decoder is enabled ($\overline{\text{B3ZSDIS}}$ is high), the data is restored to its original NRZ digital data format. A coding-violation pulse is generated when the input signal violates the B3ZS encoding sequence defined in Table 6 of ANSI T1.102-1989. If the B3ZS decoder is disabled, the P and N signals are passed on to the output stage.

The TNETS2020A detects a loss-of-signal condition and sets $\overline{\text{DLOS}}$ low to indicate the loss has occurred. $\overline{\text{DLOS}}$ becomes active when 175 ±75 consecutive zeros occur on the input. $\overline{\text{DLOS}}$ remains active until an average pulse density of 33% or greater is detected over a period of 175 ±75 clock cycles, starting with the receipt of a pulse.

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terminal-side digital data to line-side transmit

The TNETS2020A accepts terminal-side digital data that is in one of two forms and converts it to either a DS-3 or STS-1 line format. The device accepts either NRZ data or P and N data. A high on the P-data input represents a positive pulse in the B3ZS encoded line data, and a high on the N-data input represents a negative pulse. The P- and N-data streams must be encoded to meet the B3ZS line code required for DS-3 or STS-1 transmission prior to being sent to the TNETS2020A. For NRZ data, the TNETS2020A performs the B3ZS encoding. The choice of NRZ or P- and N-data input is made with $\overline{\text{B3ZSDIS}}$, which is also used to determine whether the terminal-side output is NRZ or P- and N-data. Both the terminal-side input and output are in either NRZ or P- and N-data format. When the combined NRZ data input is chosen, the data is input through TP/TD and TN should be tied to ground. A phase-locked loop is used in the input to desensitize the output pulse duration and amplitude to changes in the input-clock duty cycle.

The TNETS2020A contains the filtering and processing required to transform the B3ZS encoded NRZ data into pulses that meet the DS-3 or STS-1 output masks. The output is buffered enabling the device to directly drive a line transformer via DOUT. DOUT can be disabled by taking $\overline{\text{DSXDIS}}$ low.

An additional feature offered by the TNETS2020A is the transmit DS-3 AIS generation that is compliant to BellCore specification TR-TSY-000191. When $\overline{\text{TAIS}}$ goes low, the TNETS2020A transmits a DS-3 AIS line signal. To meet the AIS-transmission stability requirements, an input clock stable to ±20 ppm must be used as the input to REFCK (±200 ppm is allowed for non-AIS operation). Since the STS-1 AIS signal is different from the DS-3 AIS signal, this feature should not be used for STS-1 applications.

loopback

The TNETS2020A provides line-side and terminal-side loopback paths. The line-side (bipolar-to-bipolar) loopback is activated when $\overline{\text{LNLBK}}$ goes low and enables a loopback from DI1/DI2 to DOUT via the adaptive equalizer/AGC, clock recovery, B3ZS decoder, B3ZS encoder, TX I/O control, and output control functions. The terminal-side (digital-to-digital) loopback is activated when $\overline{\text{TRLBK}}$ goes low and enables a loopback from the transmitter inputs to the receiver outputs via the RX I/O control function only. These loopbacks can be operated simultaneously or independently.

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Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	3, 4, 24, 29, 33, 36, 39		Analog ground (0-V reference)
AV_{CC}	5, 6, 25, 28, 30, 34, 37		Analog supply voltage, 5 V ± 5%
$\overline{B3ZSDIS}$	23	I	B3ZS codec disable. Disables B3ZS encoder and decoder.
BIST	22	O	Built-in self test. Manufacturing test output.
CLKI	7	I	Terminal-side data clock input
CLKO	14	O	Recovered output clock
$\overline{CLKO}$	13	O	Recovered output clock inverted
CV	18	O	B3ZS coding violation indicator
DI1, DI2	31, 32	I	Line-side inputs
$\overline{DLOS}$	20	O	Digital loss-of-line input signal indicator. $\overline{DLOS}$ becomes active when 175 ± 75 consecutive zeros occur on the line and becomes inactive upon detection of an average pulse density of 33% or more over a period of 175 ± 75 clock cycles after an input pulse is detected.
DOUT	38	O	DSX line-side output
$\overline{DSXDIS}$	41	I	DSX output disable. Disables DOUT.
GND	11, 12		Digital ground (0-V reference)
$\overline{LNLBK}$	1	I	Line-side loopback enable
$\overline{RAIS}$	19	I	Receive alarm-indication signal enable. If $\overline{RAIS}$ is low, the generation of a DS-3 alarm-indication signal on the receiver output lines is enabled. If $\overline{RAIS}$ is high, normal receiver outputs are enabled.
REFCK	21	I	Reference clock. When the DS-3 AIS generator is not needed, the REFCK tolerance is ± 200 ppm. When the DS-3 AIS generator is needed, the REFCK tolerance is ± 20 ppm.
RN	15	O	Terminal-side output for N data
RPLLC1	26		CLK recovery PLL filter. NC (leave floating).
RPLLC2	27		CLK recovery calibration PLL filter. NC (leave floating).
RP/RD	16	O	Terminal-side output for combined NRZ data; P-data output for split P- and N-data stream
$\overline{RZTXIN}$	43	I	Transmit RZ input enable. $\overline{RZTXIN}$ enables the B3ZS encoded return-to-zero pulses (that are properly timed) on the transmitter TP/TD and TN inputs when low. CLKI and $\overline{B3ZSDIS}$ must be connected low in this mode.
$\overline{TAIS}$	44	I	Transmit alarm-indication signal enable. If $\overline{TAIS}$ is low, the generation of a DS-3 alarm-indication signal on the transmit output lines is enabled. If $\overline{TAIS}$ is high, normal transmit outputs are enabled.
TN	8	I	Terminal-side input for N-data input stream; tie to ground if unused
TP/TD	9	I	Terminal-side input for combined NRZ data; P data input for split P and N data stream
TPLLC	35		Transmitter calibration PLL capacitor, 0.01 µF to ground
$\overline{TRLBK}$	2	I	Terminal-side loopback enable
V_{CC}	10, 17		Digital supply voltage, 5 V ± 5%
$\overline{ZERO}$	42	I	Short cable-line buildout control. Improved DOUT for short cables (< 50 ft).
NC	40		No connection (leave floating)

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absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range, V_I ..... −0.5 V to V_{CC} +0.5 V
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Power dissipation ..... 1.1 W

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the AGND terminals.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
V_{IH}	High-level input voltage	CMOS	3.15		V
		TTL	2		
V_{IL}	Low-level input voltage	CMOS		1.65	V
		TTL		0.8	
T_A	Operating free-air temperature		−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.75 V,	I_{OH} = −4 mA	4.25			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V,	I_{OL} = 4 mA			0.5	V
V_{IK}	Input clamp voltage		V_{CC} = 4.75 V,	I_I = −18 mA			−1.2	V
I_I	Input current	TTL	V_{CC} = 5.25 V				0.55	mA
		CMOS					10	µA
I_{CC}	Supply current		Outputs terminated			180	220	mA
C_i	Input capacitance						10	pF

‡ All typical values are at V_{CC} = 5 V.

switching characteristics

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	CMOS	C_L = 15 pF	1.7	2.7	4.2	ns
t_f	Fall time			1.9	2.8	4.1	

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timing requirements, C_L = 15 pF max (see Note 2 and Figure 2)

NO.			MIN	NOM	MAX	UNIT
		Duty cycle, CLKO	45%		55%	
1	$t_{c(CLKO)1}$	Clock cycle time, CLKO, DS-3		22.353		ns
2	$t_{c(CLKO)2}$	Clock cycle time, CLKO, STS-1		19.290		ns

NOTE 2: Timing parameters are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

operating characteristics, C_L = 15 pF max (see Note 2 and Figure 2)

NO.			MIN	MAX	UNIT
3	$t_{d(CL-RPV)}$	Delay time from CLKO↓ to RP valid	0.5	5	ns
3	$t_{d(CL-RDV)}$	Delay time from CLKO↓ to RD valid	0.5	5	ns
3	$t_{d(CL-RNV)}$	Delay time from CLKO↓ to RN valid	0.5	5	ns

NOTE 2: Timing parameters are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

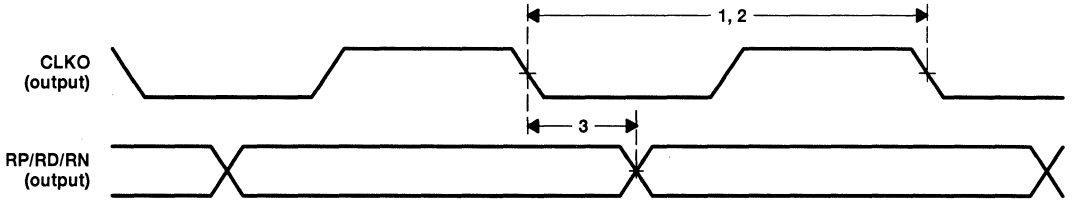

Figure 2. Receiver CLKO to Data Output

timing requirements, C_L = 15 pF max (see Note 2 and Figure 3)

NO.			MIN	NOM	MAX	UNIT
		Duty cycle, $\overline{CLKO}$	45%		55%	
1	$t_{c(CLKO)1}$	Clock cycle time, $\overline{CLKO}$, DS-3		22.353		ns
2	$t_{c(CLKO)2}$	Clock cycle time, $\overline{CLKO}$, STS-1		19.290		ns

NOTE 2: Timing parameters are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

operating characteristics, C_L = 15 pF max (see Note 2 and Figure 3)

NO.			MIN	MAX	UNIT
3	$t_{d(CH-RPV)}$	Delay time from $\overline{CLKO}$↑ to RP valid	0.75	5	ns
3	$t_{d(CH-RDV)}$	Delay time from $\overline{CLKO}$↑ to RD valid	0.75	5	ns
3	$t_{d(CH-RNV)}$	Delay time from $\overline{CLKO}$↑ to RN valid	0.75	5	ns

NOTE 2: Timing parameters are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

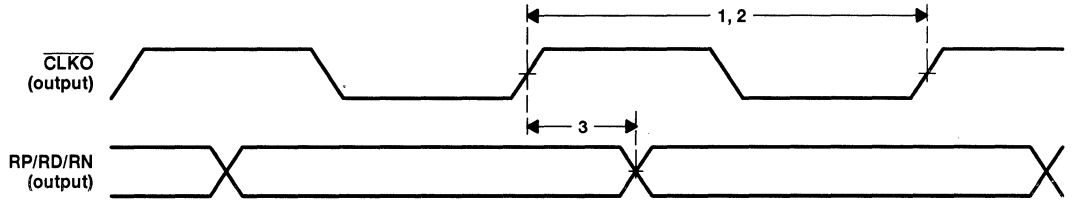

Figure 3. Receiver $\overline{CLKO}$ to Data Output

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timing requirements, C_L = 15 pF max (see Note 2 and Figure 4)

NO.			MIN	NOM	MAX	UNIT
		Duty cycle, CLKI	40%		60%	
1	$t_{c(CLKI)1}$	Clock cycle time, CLKI, DS-3		22.353		ns
2	$t_{c(CLKI)2}$	Clock cycle time, CLKI, STS-1		19.290		ns
3	$t_{su(TP)}$	Setup time, TP valid before CLKI↑	3			ns
3	$t_{su(TD)}$	Setup time, TD valid before CLKI↑	3			ns
3	$t_{su(TN)}$	Setup time, TN valid before CLKI↑	3			ns
4	$t_{h(TP)}$	Hold time, TP valid after CLKI↑	2			ns
4	$t_{h(TD)}$	Hold time, TD valid after CLKI↑	2			ns
4	$t_{h(TN)}$	Hold time, TN valid after CLKI↑	2			ns

NOTE 2: Timing parameters are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

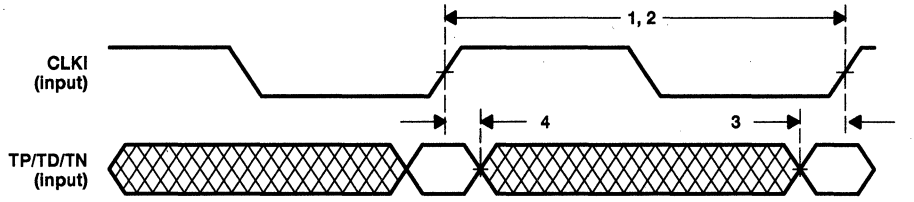

Figure 4. Transmitter-Input Timing

operating characteristics, C_L = 15 pF max (see Note 2 and Figure 5)

NO.			MIN	TYP	MAX	UNIT†
	t_d	Delay time from occurrence of violation to CV valid		7		UI
1‡	$t_{w(CVH)1}$	Pulse duration, CV high	0.9	1	1.1	UI
2§	$t_{w(CVH)2}$	Pulse duration, CV high	0.8	0.9	1	UI

† UI (unit interval) = 1/system clock frequency
‡ Pulse duration is measured at $(V_{OH} - V_{OL})/2$.
§ Pulse duration is measured at V_{OH}.
NOTE 2: Timing parameters are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

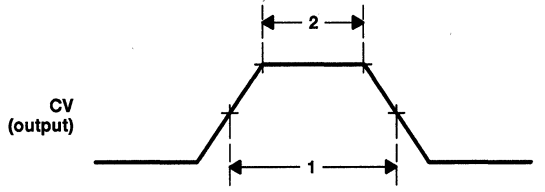

Figure 5. Coding-Violation Pulse

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APPLICATION INFORMATION

receiver-operation input requirements (see Figure 10 and Note 3)

PARAMETER		VALUE
Interface cable		AT&T 728A/734A coaxial (or equivalent)
Bit rate	DS-3	44.736 Mbit/s ± 20 ppm
	STS-1	51.840 Mbit/s ± 20 ppm
Line code		B3ZS
Input-signal amplitude	Single ended	35 mV – 1 V
	Differential	35 mV – 1 V (differential amplitude between DI1 and DI2)
Cable length		0 – 450 ft
Input-return loss	DS-3	> 26 dB at 22.368 MHz with external 75-Ω resistor (effect of external transformer excluded)
	STS-1	> 26 dB at 25.920 MHz with external 75-Ω resistor (effect of external transformer excluded)
Input resistance		> 5 kΩ
Signal-to-noise tolerance		No greater than either the value produced by adjacent pulses in the data stream or ± 10% of the peak-pulse amplitude (whichever is greater)
Input-jitter tolerance, DS-3 and STS-1		See Figures 6 and 7
Jitter transfer		As shown in Figure 8 (typical)
Interferring-signal tolerance		A sinusoidal signal at one-half the system frequency whose amplitude is at a maximum level of –18 dB (see Figure 9).
Signal coupling		The input signal must be ac coupled to the device via a transformer or capacitor.

NOTE 3: A 75-Ω ±5% output load is assumed in these specifications.

receiver-operation output specifications (see Figure 10 and Note 3)

PARAMETER	VALUE
Clock recovery jitter peaking	1 dB max
Clock recovery PLL pull-in time	< 100 µs
Sequences reported as coding violations	++, −−, not BOV, not 00V, and three or more consecutive zeros (excessive zeros)

NOTE 3: A 75-Ω ±5% output load is assumed in these specifications.

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transmitter-operation specifications (see Figure 10 and Note 3)

PARAMETER		VALUE
DOUT output characteristics ($\overline{ZERO}$ high)	Pulse shape (DS-3)	As defined by Figure 2 in ANSI TI.404-19xx, TIE1.2/93-004
	Pulse shape (STS-1)	As defined by Figure 4-10 in TR-NWT-000253, Issue 8, October 1993
	Amplitude	±0.81 V ±10% for DS-3, ±0.95 V ±10% for STS-1
	Output jitter	0.05 UI max with jitter-free input clock on CLKI
DOUT output characteristics ($\overline{ZERO}$ low)	Pulse shape (DS-3)	As defined by Figure 2 in ANSI TI.404-19xx, TIE1.2/93-004
	Pulse shape (STS-1)	As defined by Figure 4-10 in TR-TSY-000253 with 0 to 50 ft of output cable
	Amplitude	±0.67 V ±10% for DS-3, ±0.8 V ±10% for STS-1
	Pulse shape (DS-3)	As defined by Figure 9.6 in TR-TSY-000499

NOTE 3: A 75-Ω ±5% output load is assumed in these specifications.

AIS and loopback-control signal arbitration

$\overline{RAIS}$	$\overline{TAIS}$	$\overline{LNLBK}$	$\overline{TRLBK}$	TERMINAL OUTPUT	LINE OUTPUT
1	1	1	1	Normal	Normal
1	0	X	1	Normal	AIS
1	0	X	0	Terminal loopback	AIS
0	1	1	X	AIS	Normal
0	1	0	X	AIS	Line loopback
0	0	X	X	AIS	AIS
1	1	1	0	Terminal loopback	Normal
1	1	0	1	Normal	Line loopback
1	1	0	0	Terminal loopback	Line loopback

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power-down mode

To reduce the current required by the device when either the transmitter or receiver is not used, the following power terminals must be tied to ground:

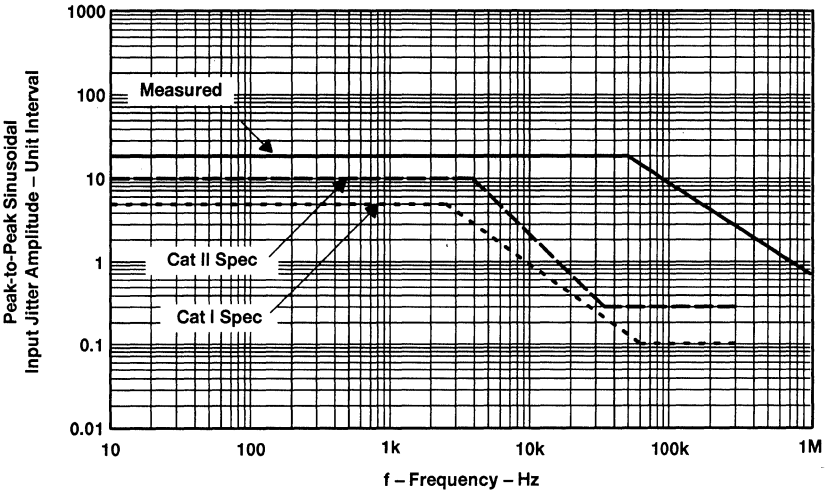
- Receiver-only operation: Ground terminals 5, 6, and 37 for a supply current reduction of approximately 10 mA
- Transmitter-only operation: Ground terminals 25, 28, and 30 for a supply current reduction of approximately 80 mA

jitter performance

Preliminary tests have been executed on the TNETS2021A device to qualitatively characterize jitter performance. Typical data is provided in Figures 6, 7, and 8. This information is for reference only and is not intended to be used as precise performance parameters for these devices. Although the data was taken on the TNETS2021A, the results are also valid for the TNETS2020A. For STS-1, jitter-tolerance requirements (as specified in Bellcore TR-NWT-000253) are exceeded (see Figure 7).

receiver jitter tolerance

Receiver jitter-tolerance data is plotted in Figure 6 and Figure 7. The device meets DS-3 jitter-tolerance requirements (as specified in Bellcore TR-TSY-000499) for both Category I and Category II equipment (see Figure 6). The flat tolerance exhibited from 10 Hz to 40 kHz results from an overrange condition in the test equipment. Actual jitter tolerance in this range exceeded 20 UI, peak-to-peak.



Test setup:

Instrument:	HP3784A	Transmit interface:	XCON 75 B3ZS	Receive interface:	Binary TTL
Temperature:	Room	Transmit clock:	Standard rate DS-3 + 0 ppm	Receive clock:	DS-3
Supply:	5 V	Transmit pattern:	PRBS 15 zero substitution 000	Receive pattern:	As per transmit
Filtering:	None			Receive hit threshold:	0.500 UIP

Figure 6. DS-3 Receive Jitter-Tolerance Data

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receive jitter tolerance (continued)

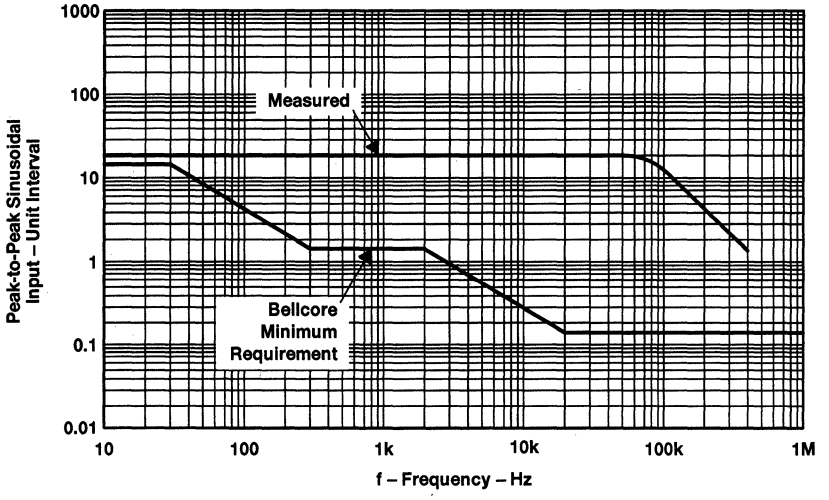

Figure 7. STS-1 Receive Jitter-Tolerance Data

jitter transfer

Typical jitter-transfer data for both the receiver and transmitter sections of the TNETS2021A is plotted in Figure 8. The device does not, and is not designed to, meet the TR-TSY-000499 jitter-transfer requirements (< 0.1 dB) for Category II equipment (regenerators). TR-TSY-000499 does not impose requirements for Category I equipment of this type. Such requirements are application dependent.

In a looped-back configuration (through the receive path and externally looped back through the transmit path), in the absence of applied input jitter, the amount of jitter introduced by the TNETS2020A is a maximum 0.065 UIs of peak-to-peak jitter over a jitter-frequency range of 20 Hz to 1 MHz (filter with high pass of 10 Hz and a low pass of 1.1 MHz). With applied input jitter, the maximum output jitter is the applied input jitter plus the above jitter introduced by the TNETS2020A.

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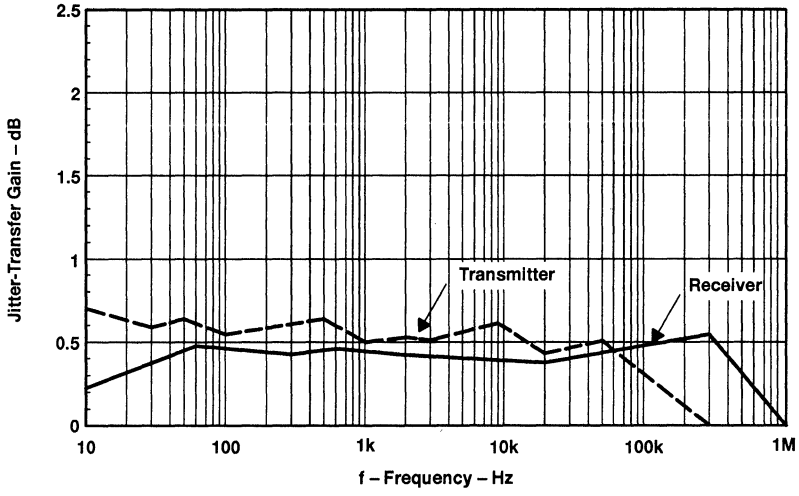
jitter transfer (continued)



Test setup (for receive-jitter testing; transmit similar):

Instrument:	HP3784A	Jitter input:	0.75 UI p-p	Receive interface:	Binary TTL
Temperature:	Room	Transmit interface:	XCON 75 B3ZS	Receive clock:	DS-3
Supply:	5 V	Transmit clock:	Std rate DS-3 + 0 ppm	Receive pattern:	As per transmit
Filtering:	10 Hz HP	Transmit pattern:	PRBS 15 zero substitution 000	Receive hit threshold:	0.500 UIP

Figure 8. Typical Jitter-Transfer Data

jitter generation

For DS-3, Bellcore Technical Reference TR-TSY-000499, Issue 3, December 1989 specifies the maximum-jitter generation to be 1 UI peak-to-peak at the output of the terminal receiver for Category I equipment.

For STS-1, Bellcore Technical Reference TR-NWT-000253, Issue 2, December 1991 specifies the maximum-jitter generation to be 1.5 UI peak-to-peak maximum at the output of the terminal receiver for Category I equipment.

In a looped-back configuration (through the transmit path and externally looped back through the receive path), the DS-3/STS-1 jitter generation within the TNETS2020A is 0.145 UI peak-to-peak maximum for all frequencies specified in these two standards.

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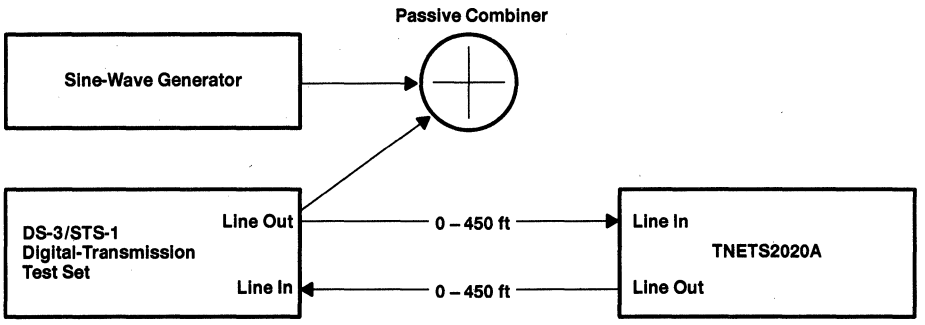
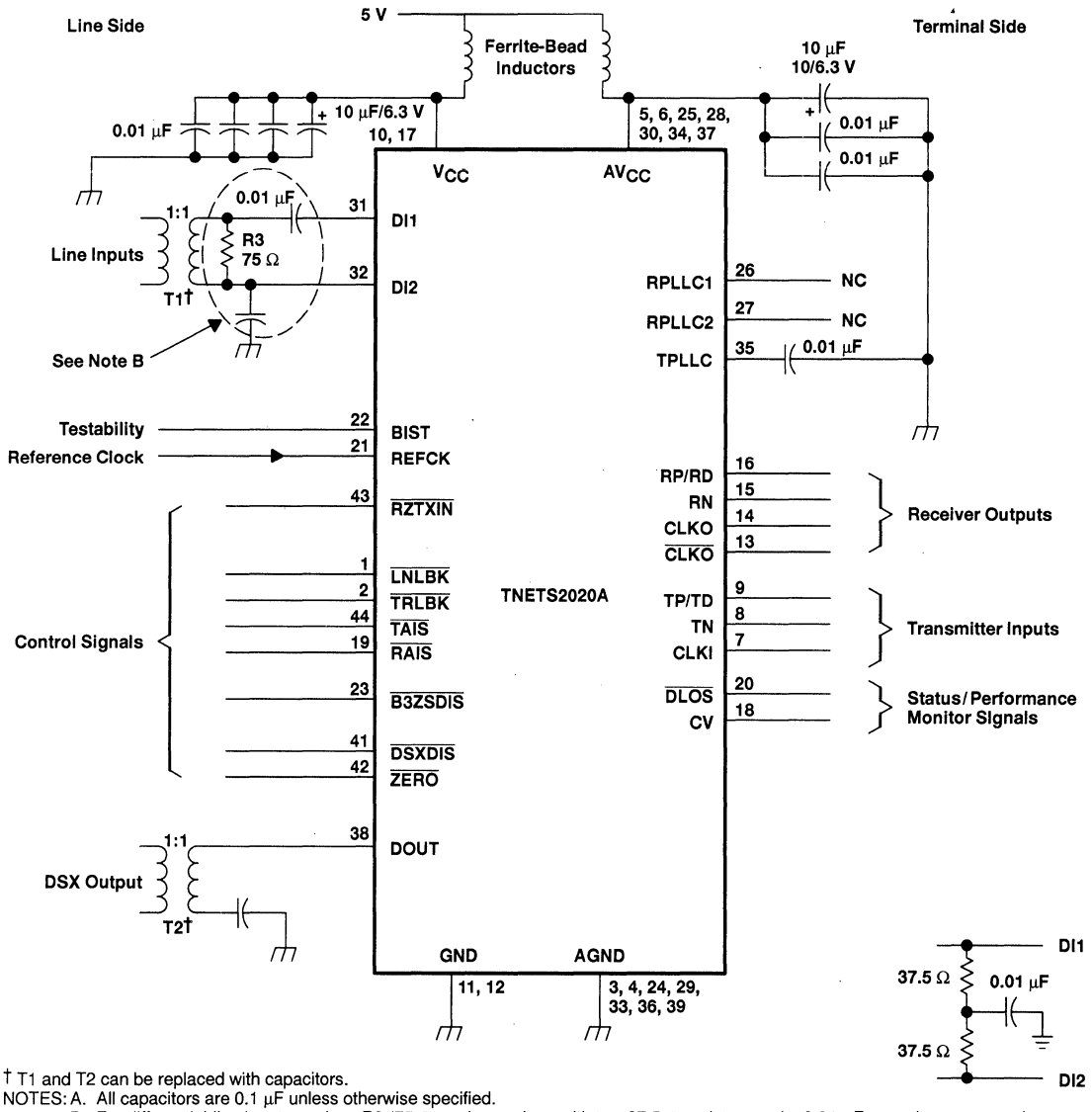


Figure 9. Interference-Margin Test Configuration

APPLICATION INFORMATION



† T1 and T2 can be replaced with capacitors.

NOTES: A. All capacitors are 0.1 µF unless otherwise specified.

B. For differential-line inputs, replace R3 (75 Ω) and capacitors with two 37.5-Ω resistors and a 0.01-µF capacitor connected as shown.

Figure 10. External Connections for Operation

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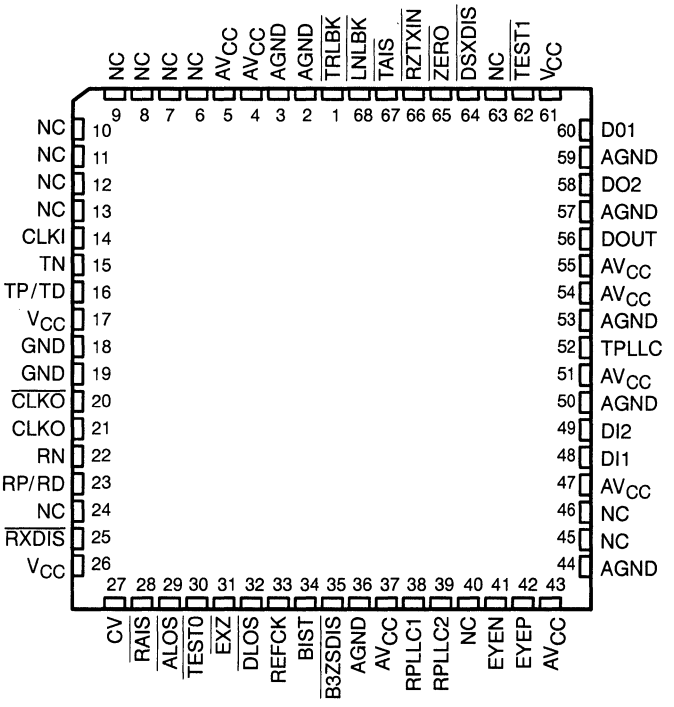
SDNS018B – MARCH 1994 – REVISED DECEMBER 1994

- Line- and Terminal-Side DS-3 Alarm Indication Signal (AIS) Insertion
- Full-Loopback Capability
- Coding-Violation and Excessive-Zeros Monitors
- Loss-of-Signal Monitor
- On-Chip Line Buffer/Filter and Line Build-Out Bypass
- Power-Down Mode
- Packaged in 68-Pin Plastic Leaded Chip Carrier (FN)
- Single-Chip Line Interface for DS-3 and STS-1 Signals
- Single 5-V Power Supply
- Meets Crossconnect-Frame Mask Requirements
- Adaptive Equalization of 0 to 450 Feet of Cable
- Input Dynamic Range of 29 dB (35 mV – 1 V)
- Meets Approved DS-3/STS-1 Jitter Requirements
- Selectable B3ZS Line Encoding/Decoding

FN PACKAGE
(TOP VIEW)



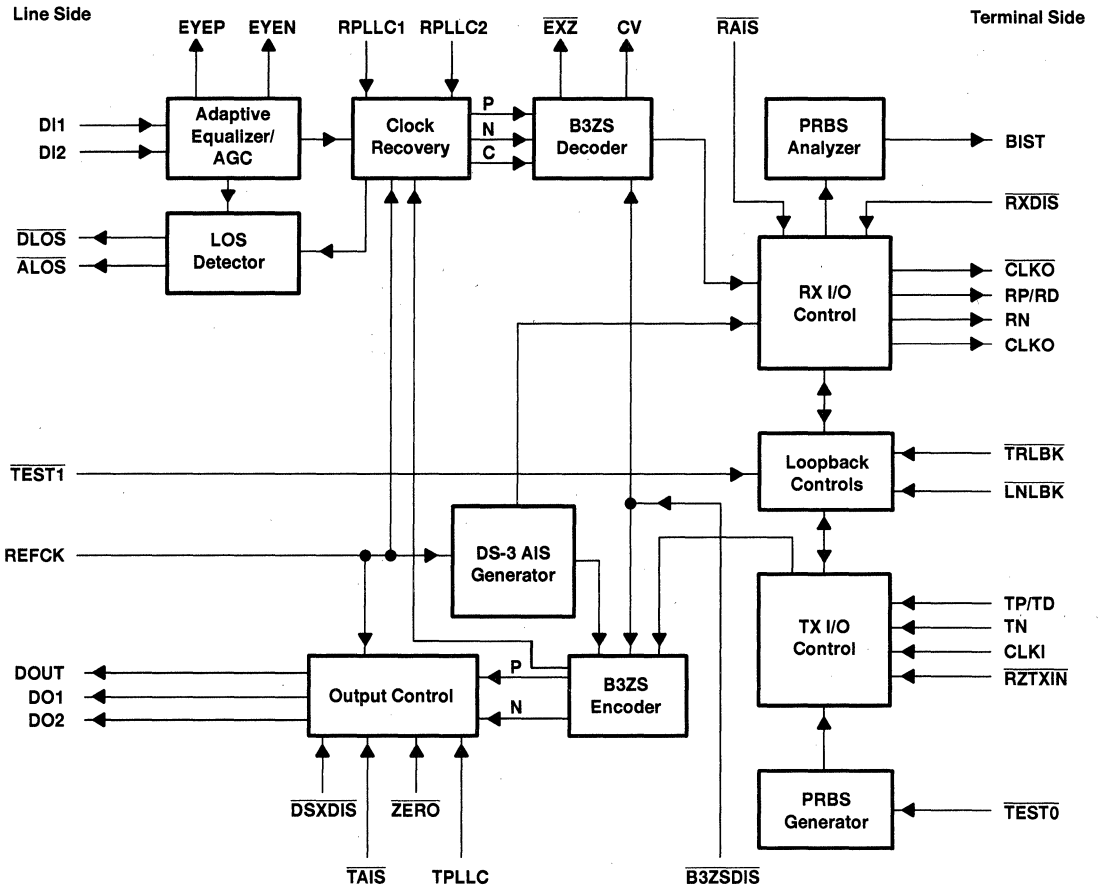
NC – No internal connection

description

The advanced STS-1/DS-3 receiver/transmitter TNETS2021A performs the transmit and receive line-interface functions required for transmission of STS-1 (51.840 Mbit/s) and DS-3 (44.736 Mbit/s) signals across a coaxial interface. The TNETS2021A operates from a single 5-V supply with a minimum number of passive external components. Performance monitoring, loopbacks, AIS generation, and B3ZS encoding/decoding functions are included. A single-chip solution is used for interfacing DS-3 or STS-1 signals to DSX or STS-X cross-connect frames. The TNETS2021A meets all applicable ANSI, Bellcore, and CCITT interconnection specifications for a wide range of system applications.

PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

detailed description

receiver functions

The adaptive equalizer/AGC in the receiver channel is used to recover CMOS-level P- and N-rail data from the bipolar B3ZS-encoded input pulses. The AGC has a dynamic range of 29 dB (35 mV to 1 V). This allows the device to be used in applications where the input signal is attenuated beyond the level of the TR499 template (such as bridging repeaters or protection switches). Adaptive equalization is included to restore the integrity of the signal after it has been attenuated by the frequency-dependent loss due to 450 feet of coaxial cable. The equalized and gain-controlled differential signals can be monitored at the EYEP and EYEN terminals.

Differential inputs DI1 and DI2 allow optimum performance of the device in noisy environments. Alternatively, single-ended operation can be used in less critical environments or where the use of a transformer is not desired (the input signal can be ac coupled through a capacitor). When the differential mode is used, the maximum single-ended ac input level on either input pin is 0.5 V (1 V differential). For larger input levels, a step-down transformer or resistive attenuation should be used.

The PLL-based clock-recovery circuit is used to recover a CMOS-level clock from the equalized and sliced input pulses.

receiver functions (continued)

The B3ZS decoder circuit decodes the B3ZS-encoded line-side signal and detects coding errors and excessive zeros in the incoming data stream. An active-high pulse is generated on the coding violation (CV) output when the input signal violates the B3ZS-encoding sequence. An active-low pulse is generated on the $\overline{EXZ}$ output when a string of three or more zeros is detected and it remains low until a one is detected. The $\overline{B3ZSDIS}$ control input is used to disable this function.

The RX I/O-control circuit multiplexes the appropriate signals to the receiver terminal-side outputs. The output NRZ data formats include:

- B3ZS-decoded outputs that are recovered from the line (RP/RD contains recovered data and RN is held low).
- Encoded outputs from the clock-recovery circuit (RP/RD contains positive data and RN contains negative data). This mode allows an external device such as a DS-3 framer to perform the B3ZS-encoding and decoding functions. $\overline{B3ZSDIS}$ enables this mode.
- Loopback signals from the transmitter terminal-side inputs when $\overline{TRLBK}$ is low.
- AIS format signals when $\overline{RAIS}$ is low.

CLKO and $\overline{CLKO}$ provide true and inverted clocks for the above formats. $\overline{RXDIS}$ forces RP/RD and RN to a low state. The LOS-detector circuit generates outputs that indicate the presence of the line-side input signal(s). $\overline{DLOS}$ goes low when a string of 175 ± 75 consecutive zeros occurs on the line. This output is reset when the detected ones density or quantity is 33% or greater for 175 ± 75 pulses. $\overline{ALOS}$ goes high when the ones density is greater than 33% for 175 ± 75 pulses and goes low when the ones density is less than 28% for 175 ± 75 pulses. $\overline{ALOS}$ can toggle when the ones density is between 28% and 33%.

transmitter functions

The TX I/O-control circuit multiplexes the appropriate signals for use by the transmitter. The selectable formats include:

- Unencoded-NRZ input data (TP/TD contains data and TN must be grounded).
- B3ZS-encoded NRZ input data (TP/TD contains positive data and TN contains negative data). $\overline{B3ZSDIS}$ enables this mode.
- B3ZS-encoded RZ input data (TP/TD contains positive data and TN contains negative data). This mode is enabled by $\overline{RZTXIN}$.
- Loopback signals from the B3ZS decoder when $\overline{LNLBK}$ is low.
- AIS format signals when $\overline{TAIS}$ is low.
- PRBS generator outputs when $\overline{TEST0}$ is low.

CLKI is the input clock for the above formats. When $\overline{RZTXIN}$ is low, CLKI is ignored.

The B3ZS-encoder circuit encodes the input NRZ data to be compliant with ANSI Specification T1.102A. The $\overline{B3ZSDIS}$ control input can be used to disable this circuit. $\overline{B3ZSDIS}$ must be low when $\overline{RZTXIN}$ is low. The output-control circuit contains the formatting circuitry required to transform the B3ZS-encoded data into pulses that meet the requirements for the DS-3 and STS-1 line rates. An internal line driver enables the TNETS2021A to drive these signals directly into the 75-Ω load of the output cable.

transmitter functions (continued)

$\overline{\text{DSXDIS}}$ determines which of two output types is enabled. DOUT is a single-ended output that meets the STS-1/DS-3 templates. An internal transversal filter is used to create this output. DO1 and DO2 are rectangular pulses representing level-translated versions of the input P/N digital signals. An external transformer is required to translate these signals to the appropriate polarity. When $\overline{\text{DSXDIS}}$ is high, DOUT is enabled. When $\overline{\text{DSXDIS}}$ is low, DO1/DO2 are enabled.

An external capacitor connected to TPLLC is required for the internal PLL, which is used to calibrate the transversal-filter circuit. $\overline{\text{ZERO}}$ improves the DOUT pulse shape for short cable.

loopbacks and AIS insertion

The loopback-control circuit enables the input signals of the TNETS2021A to loopback on both the line and terminal sides of the device. When $\overline{\text{TRLBK}}$ is low, TP/TD, TN, and CLKI are directly looped back to RP/RD, TN, and CLKO via the RX I/O-control circuit. When $\overline{\text{LNLBK}}$ is low, DI1/DI2 are looped back to the DOUT or DO1/DO2 outputs via the adaptive equalizer/AGC, clock-recovery, B3ZS-decoder, B3ZS-encoder, TX I/O control, and output-control functions. These loopbacks can be operated independently or simultaneously.

The DS-3 AIS-generator circuit generates a DS-3 alarm indication signal (AIS) that is compliant with TR191 on the line or terminal sides of the device (select with $\overline{\text{TAIS}}$ or $\overline{\text{RAIS}}$). For STS-1 operation, inputs to the device must contain the correct overhead required for path sectionalization (this circuit generates DS-3 format AIS only).

testability

The PRBS generator and PRBS analyzer provide an internal BIST function on the TNETS2021A. When $\overline{\text{TEST0}}$ is low, the output of the PRBS generator is driven through the TX I/O control, B3ZS-encoder, and output-control circuits to DOUT. This output can be looped back to the receiver DI1 or DI2 inputs via an external capacitor. A PRBS analyzer monitors the output of the RX I/O-control circuit. If the output signals conform to the correct 2^{15} pattern, BIST goes high. The PRBS analyzer always functions regardless of the state of $\overline{\text{TEST0}}$. When a valid 2^{15} pattern appears at the receiver outputs, BIST goes high. Since this function sends signals through all of the datapath blocks in the device, it is particularly useful for screening die during a wafer test. This test must be run with $\overline{\text{B3ZSDIS}}$ held high.

$\overline{\text{TEST1}}$ enables an auxiliary terminal-side loopback primarily intended for use during device debug. Signals from the transmitter inputs are routed through the TX I/O control, B3ZS-encoder, clock-recovery, B3ZS-decoder, and RX I/O control circuits to the receiver outputs.

input reference clock

An input CMOS-level clock applied to REFCK is required for the TNETS2021A to operate. Typically, this is supplied by a local oscillator on the board. The tolerance required is ±200 ppm for operation when the DS-3 AIS generator is not used. To generate a valid AIS pattern, a tolerance of ±20 ppm is required.

Terminal Functions

power supply and ground

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	2, 3, 36, 44, 50, 53, 57, 59		Analog ground (0-V reference)
AV_{CC}	4, 5, 37, 43, 47, 51, 54, 55		Analog supply voltage, 5 V ± 5%
GND	18, 19		Digital ground (0-V reference)
V_{CC}	17, 26, 61		Digital supply voltage, 5 V ± 5%

receive interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{ALOS}$	29	O (CMOS)	Analog loss of signal. $\overline{ALOS}$ goes low when pulse density is <28% for 175 ± 75 pulses and clears when pulse density is >33% for 175 ± 75 pulses. $\overline{ALOS}$ can toggle when between 28% and 33%.
BIST	34	O (CMOS)	Built-in self-test. BIST goes high when a valid PRBS pattern is detected.
CLKO	21	O (CMOS)	Clock output. CLKO is the receive clock.
$\overline{CLKO}$	20	O (CMOS)	Inverted clock output. $\overline{CLKO}$ is the inverted receive clock.
CV	27	O (CMOS)	Coding violation. CV goes high when incoming data violates B3ZS code.
DI1	48	I (analog)	Data in 1. Line-side input. For single-ended operation, DI1 or DI2 must be ac coupled to ground via a capacitor. For differential operation, DI1 and DI2 are tied directly to a transformer.
DI2	49	I (analog)	Data in 2. Line-side input. For single-ended operation, DI2 or DI1 must be ac coupled to ground via a capacitor. For differential operation, DI1 and DI2 are tied directly to a transformer.
$\overline{DLOS}$	32	O (CMOS)	Digital loss of signal. $\overline{DLOS}$ goes low when 175 ± 75 consecutive zeros appear in the incoming data stream and clears when pulse density is >33% for 175 ± 75 pulses.
$\overline{EXZ}$	31	O (CMOS)	Excessive zeros. $\overline{EXZ}$ goes low when three or more consecutive zeros occur in the input data stream.
EYEN	41	O (analog)	Negative eye-pattern monitor. EYEN monitors the inverted AGC and equalized output from the adaptive-equalizer/AGC circuit.
EYEP	42	O (analog)	Positive eye-pattern monitor. EYEP monitors the noninverted AGC and equalized output from the adaptive-equalizer/AGC circuit.
RN	22	O (CMOS)	Receiver negative. RN generates negative rail data when $\overline{B3ZSDIS}$ is low and is held low when $\overline{B3ZSDIS}$ is high.
RPLLC1 RPLLC2	38 39	I (analog)	Receiver PLL capacitor 1 and capacitor 2. Leave floating.
RP/RD	23	O (CMOS)	Receiver positive/data. RP/RD generates B3ZS decoded combined data ($\overline{B3ZSDIS}$ high) or positive rail data ($\overline{B3ZSDIS}$ low).

PRODUCT PREVIEW

Terminal Functions (Continued)

transmit interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLKI	14	I (CMOS)	Transmitter input clock
DO1	60	O (analog)	Data out positive. DO1 is the rectangular positive-pulse output enabled when $\overline{\text{DSXDIS}}$ is low.
DO2	58	O (analog)	Data out negative. DO2 is the rectangular negative-pulse output enabled when $\overline{\text{DSXDIS}}$ is low.
DOUT	56	O (analog)	Data out. DOUT is the DSX filtered single-ended output enabled when $\overline{\text{DSXDIS}}$ is high.
TN	15	I (CMOS)	Transmitter negative. TN is the input for negative-rail data when $\overline{\text{B3ZSDIS}}$ is low. TN must be tied low when $\overline{\text{B3ZSDIS}}$ is high.
TPLLC	52	I (analog)	Transmit PLL capacitor. TPLLC is the capacitor input for transversal-filter calibration PLL (see Figure 9).
TP/TD	16	I (CMOS)	Transmitter positive/data. TP/TD is the input for unencoded combined data ($\overline{\text{B3ZSDIS}}$ high) or positive-rail data ($\overline{\text{B3ZSDIS}}$ low).

control/reference inputs (see Note 1)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{B3ZSDIS}}$	35	I (TTL)	B3ZS codec disable. $\overline{\text{B3ZSDIS}}$ disables the internal B3ZS encoder and decoder functions.
$\overline{\text{DSXDIS}}$	64	I (TTL)	Transmit DSX output disable. $\overline{\text{DSXDIS}}$ disables DOUT and enables DO1/DO2.
$\overline{\text{LNLBK}}$	68	I (TTL)	Line-loopback enable. $\overline{\text{LNLBK}}$ enables a loopback from DI1/DI2 to DOUT or DO1/DO2 via the adaptive-equalizer/AGC, clock-recovery, B3ZS-decoder, B3ZS-encoder, TX I/O-control and output-control circuits.
$\overline{\text{RAIS}}$	28	I (TTL)	Receive alarm indication signal enable. $\overline{\text{RAIS}}$ enables generation of DS-3 AIS on the receiver outputs (see Note 1).
REFCK	33	I (CMOS)	Reference clock input. REFCK is the input reference clock at the system frequency required for chip operation. Required tolerance is ± 200 ppm when DS-3 AIS generation is not required and ± 20 ppm when DS-3 AIS generation is required.
$\overline{\text{RXDIS}}$	25	I (TTL)	Receive output disable. $\overline{\text{RXDIS}}$ forces RP/RD and RN to a low state.
$\overline{\text{RZTXIN}}$	66	I (TTL)	Transmit RZ input enable. $\overline{\text{RZTXIN}}$ goes low to accept B3ZS-encoded return-to-zero pulses on TP/TD and TN. CLKI and $\overline{\text{B3ZSDIS}}$ must be tied low in this mode.
$\overline{\text{TAIS}}$	67	I (TTL)	Transmit AIS enable. $\overline{\text{TAIS}}$ enables generation of DS-3 AIS on the transmitter outputs (see Note 1).
$\overline{\text{TEST0}}$	30	I (TTL)	Test in 0. $\overline{\text{TEST0}}$ enables internal BIST function (PRBS generator/analyzer).
$\overline{\text{TEST1}}$	62	I (TTL)	Test in 1. $\overline{\text{TEST1}}$ enables a terminal-side loopback from TP/TD and TN to the receiver outputs via the TX I/O control, B3ZS-encoder, clock-recovery, B3ZS-decoder, and RX I/O-control circuits.
$\overline{\text{TRLBK}}$	1	I (TTL)	Terminal loopback enable. $\overline{\text{TRLBK}}$ enables a loopback from the transmitter inputs to the receiver outputs via the RX I/O-control circuits only.
$\overline{\text{ZERO}}$	65	I (TTL)	Transmit zero cable enable. $\overline{\text{ZERO}}$ improves DOUT output mask for short cable lengths (<50 ft).

NOTE 1: DS-3 AIS is defined as a valid M-frame with proper subframe structure. The data payload is 1011 . . . sequence starting with a 1 after each overhead bit. Overhead bits are: F0 = 0, F1 = 1, M0 = 0, M1 = 1; C bits are set to 0; X bits are set to 1; and P bits are set for valid parity.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 2) ..... −0.3 V to 7 V
Input voltage range, V_I ..... −0.3 V to V_{CC} + 0.3 V
Operating free-air temperature range, T_A ..... −40°C to 85°C
Operating junction temperature, T_J ..... 150°C
Storage temperature range ..... −55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: All voltage values are with respect to the AGND terminals.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
AV_{CC}	Analog supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	CMOS	3.15			V
		TTL (see Note 3)	2			
V_{IL}	Low-level input voltage	CMOS		1.65		V
		TTL (see Note 3)			0.8	
I_{OH}	High-level output current				4	mA
I_{OL}	Low-level output current				4	mA
T_A	Operating free-air temperature		−40		85	°C

NOTE 3: Input pad has a 20-kΩ internal pullup resistor.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	4-mA CMOS	I_{OH} = −4 mA	V_{CC}−0.5		V
V_{OL}	Low-level output voltage	4-mA CMOS	I_{OL} = −4 mA		0.5	V
I_{IH}	High-level input current	CMOS	V_{CC} = 5.25 V		10	µA
		TTL (see Note 3)			10	
I_{IL}	Low-level input current	CMOS	V_{CC} = 5.25 V		10	µA
		TTL (see Note 3)			550	
I_{CC}	Supply current		Outputs terminated		220	mA
P_D	Power dissipation		Inputs are switching		1.1	W
C_i	Input capacitance				10	pF

NOTE 3: Input pad has a 20-kΩ internal pullup resistor.

switching characteristics

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	CMOS	C_L = 15 pF	1.7	2.7	4.2	ns
t_f	Fall time			1.9	2.8	4.1	

PRODUCT PREVIEW

operating characteristics, C_L = 15 pF max (see Note 4 and Figure 1)

NO.			MIN	TYP	MAX	UNIT
		Duty cycle, CLKO	45%		55%	
1	$t_{c(CLKO)1}$	Clock cycle time, CLKO, DS-3		22.353		ns
2	$t_{c(CLKO)2}$	Clock cycle time, CLKO, STS-1		19.290		ns
3	$t_{d(CL-RPV)}$	Delay time, CLKO↓ to RP valid	0.5		5	ns
3	$t_{d(CL-RDV)}$	Delay time, CLKO↓ to RD valid	0.5		5	ns
3	$t_{d(CL-RNV)}$	Delay time, CLKO↓ to RN valid	0.5		5	ns

NOTE 4: Timing parameters are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

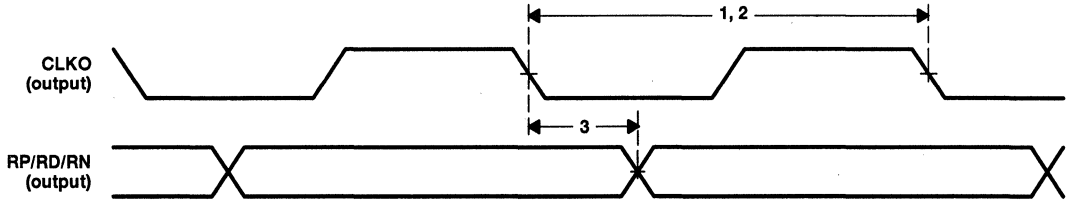


Figure 1. Receiver CLKO to Data Output

operating characteristics, C_L = 15 pF max (see Note 4 and Figure 2)

NO.			MIN	TYP	MAX	UNIT
		Duty cycle, $\overline{\text{CLKO}}$	45%		55%	
1	$t_{c(CLKO)1}$	Clock cycle time, $\overline{\text{CLKO}}$, DS-3		22.353		ns
2	$t_{c(CLKO)2}$	Clock cycle time, $\overline{\text{CLKO}}$, STS-1		19.290		ns
3	$t_{d(CH-RPV)}$	Delay time, $\overline{\text{CLKO}}$↑ to RP valid	0.75		5	ns
3	$t_{d(CH-RDV)}$	Delay time, $\overline{\text{CLKO}}$↑ to RD valid	0.75		5	ns
3	$t_{d(CH-RNV)}$	Delay time, $\overline{\text{CLKO}}$↑ to RN valid	0.75		5	ns

NOTE 4: Timing parameters are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

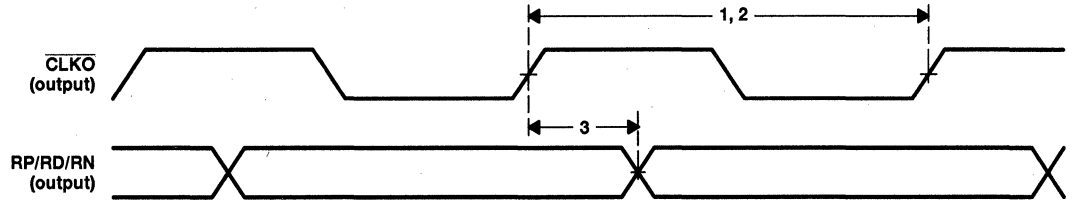


Figure 2. Receiver $\overline{\text{CLKO}}$ to Data Output

PRODUCT PREVIEW

timing requirements, C_L = 15 pF max (see Note 4 and Figure 3)

NO.			MIN	NOM	MAX	UNIT
		Duty cycle, CLKI	40%		60%	
1	$t_{c(CLKI)1}$	Clock cycle time, CLKI, DS-3		22.353		ns
2	$t_{c(CLKI)2}$	Clock cycle time, CLKI, STS-1		19.290		ns
3	$t_{su(TP)}$	Setup time, TP valid before CLKI↑	3			ns
3	$t_{su(TD)}$	Setup time, TD valid before CLKI↑	3			ns
3	$t_{su(TN)}$	Setup time, TN valid before CLKI↑	3			ns
4	$t_{h(TP)}$	Hold time, TP valid after CLKI↑	2			ns
4	$t_{h(TD)}$	Hold time, TD valid after CLKI↑	2			ns
4	$t_{h(TN)}$	Hold time, TN valid after CLKI↑	2			ns

NOTE 4: Timing parameters are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

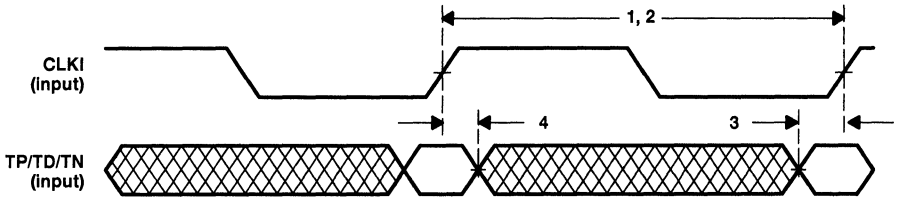


Figure 3. Transmitter-Input Timing

operating characteristics, C_L = 15 pF max (see Note 4 and Figure 4)

NO.			MIN	TYP	MAX	UNIT†
	t_d	Delay time from occurrence of violation to CV valid		7		UI
1‡	$t_{w(CVH)1}$	Pulse duration, CV high	0.9	1.0	1.1	UI
2§	$t_{w(CVH)2}$	Pulse duration, CV high	0.8	0.9	1	UI

† UI (unit interval) = 1/system clock frequency
‡ Pulse duration is measured at $(V_{OH} - V_{OL})/2$.
§ Pulse duration is measured at V_{OH}.
NOTE 4: Timing parameters are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

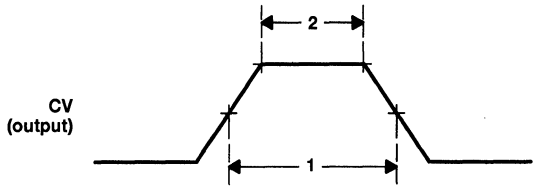


Figure 4. Coding-Violation Pulse

PRODUCT PREVIEW

operating characteristics, C_L = 15 pF max (see Note 4 and Figure 5)

NO.			MIN	TYP	MAX	UNIT†
	t_d	Delay time from occurrence of violation to $\overline{EXZ}$ valid		7		UI
1‡	$t_{w(EXZL)1}$	Pulse duration, $\overline{EXZ}$ low	0.9	1.0	1.1	UI
2§	$t_{w(EXZL)2}$	Pulse duration, $\overline{EXZ}$ low	0.8	0.9	1	UI

† UI (unit interval) = 1/system clock frequency
‡ Pulse duration is measured at $(V_{OH} - V_{OL})/2$.
§ Pulse duration is measured at V_{OL}.
NOTE 4: Timing parameters are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

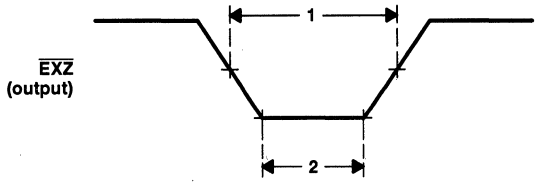


Figure 5. Excessive-Zeros Pulse

PRODUCT PREVIEW

APPLICATION INFORMATION

receiver-operation input requirements (see Note 5 and Figure 10)

PARAMETER		VALUE
Interface cable		AT&T 728A/734A coaxial (or equivalent)
Bit rate	DS-3	44.736 Mbit/s ± 20 ppm
	STS-1	51.840 Mbit/s ± 20 ppm
Line code		B3ZS
Input-signal amplitude	Single ended	35 mV – 1 V (relative to terminal used for dc bias)
	Differential	35 mV – 1 V (differential amplitude between DI1 and DI2)
Cable length		0 – 450 ft
Input-return loss	DS-3	> 26 dB at 22.368 MHz with external 75-Ω resistor (effect of external transformer excluded)
	STS-1	> 26 dB at 25.920 MHz with external 75-Ω resistor (effect of external transformer excluded)
Input resistance		> 5 kΩ
Signal-to-noise tolerance		No greater than either the value produced by adjacent pulses in the data stream or ±10% of the peak pulse amplitude (whichever is greater)
Input-jitter tolerance, DS-3 and STS-1		See Figures 6 and 7
Jitter transfer		As shown in Figure 8 (typical)
Interferring-signal tolerance		A sinusoidal signal at one-half the system frequency whose amplitude is at a maximum level of –18 dB (see Figure 9).
Signal coupling		The input signal must be ac coupled to the device via a transformer or capacitor.

NOTE 5: A 75-Ω ± 5% output load is assumed in these specifications.

receiver-operation output specifications (see Note 5 and Figure 10)

PARAMETER	VALUE
Clock-recovery jitter peaking	1 dB max
Clock-recovery PLL pull-in time	< 100 μs
Sequences reported as coding violations	++, −−, not BOV, not 00V, and three or more consecutive zeros (excessive zeros)

NOTE 5: A 75-Ω ± 5% output load is assumed in these specifications.

PRODUCT PREVIEW

APPLICATION INFORMATION

transmitter-operation specifications (see Note 5 and Figure 10)

PARAMETER		VALUE
DO1/DO2 output characteristics	Amplitude	±1.75 V ±10%
	Puse duration	1/2 UI ±10%
	Rise time	2.5 ±1.5 ns
	Overshoot/undershoot	< 10%
	Output power	Between –1.8 and 5.7 dBm for an all-ones pattern measured in a 3-kHz band centered at 1/2 the system frequency
	AIS-output power	Between –4.7 and 3.6 dBm for an AIS signal measured through a low-pass filter with a 3-dB cutoff or 200 MHz with cable lengths between 225 and 450 ft
	Pulse imbalance	Ratio of positive and negative pulse amplitudes: 0.9 – 1.10
	Pulse symmetry	Output power at system frequency > 20 dB below the level at 1/2 the system frequency
	Output jitter	0.1 UI maximum with jitter-free input clock on CLKI
DOUT output characteristics ($\overline{\text{ZERO}}$ high)	Pulse shape (DS-3)	As defined by Figure 2 in ANSI TI.404-19xx, TIE1.2/93-004
	Pulse shape (STS-1)	As defined by Figure 4.10 in TR-NWT-000253, Issue 8, October 1993
	Amplitude	± 0.81 V ±10% for DS-3 ± 0.95 V ±10% for STS-1
	Output jitter	0.05 UI max with jitter-free input clock on CLKI
DOUT output characteristics ($\overline{\text{ZERO}}$ low)	Pulse shape (DS-3)	As defined by Figure 2 in ANSI TI.404-19xx, TIE1.2/93-004
	Pulse shape (STS-1)	As defined by Figure 4.10 in TR-TSY-000253 with 0 to 50 ft of output cable
	Amplitude	± 0.67 V ± 10% for DS-3, ± 0.8 V ± 10% for STS-1
	Pulse shape (DS-3)	As defined by Figure 9.6 in TR-TSY-000499

NOTE 5: A 75-Ω ± 5% output load is assumed in these specifications.

AIS and loopback-control signal arbitration

$\overline{\text{RAIS}}$	$\overline{\text{TAIS}}$	$\overline{\text{LNLBK}}$	$\overline{\text{TRLBK}}$	TERMINAL OUTPUT	LINE OUTPUT
1	1	1	1	Normal	Normal
1	0	X	1	Normal	AIS
1	0	X	0	Terminal loopback	AIS
0	1	1	X	AIS	Normal
0	1	0	X	AIS	Line loopback
0	0	X	X	AIS	AIS
1	1	1	0	Terminal loopback	Normal
1	1	0	1	Normal	Line loopback
1	1	0	0	Terminal loopback	Line loopback

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power-down mode

To reduce the current required by the device when either the transmitter or receiver is not used, the following power terminals must be tied to ground:

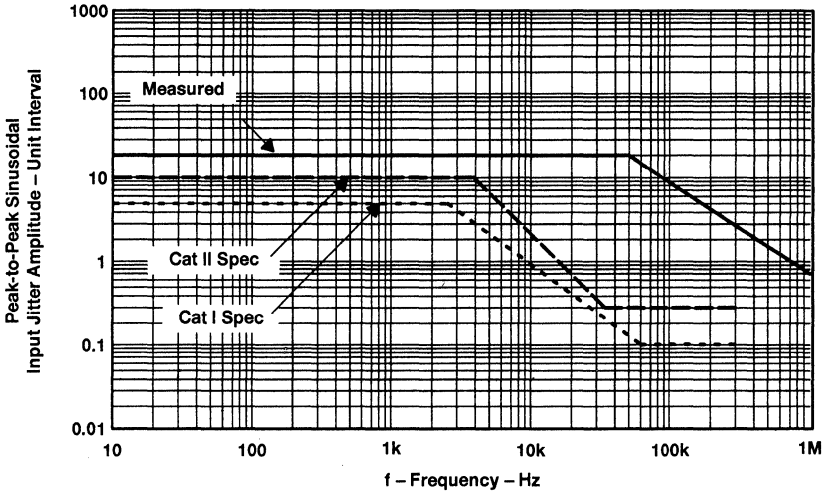
- Receiver-only operation: Ground terminals 4, 5, 54, and 55 for a supply current reduction of approximately 10 mA
- Transmitter-only operation: Ground terminals 37, 43, and 47 for a supply current reduction of approximately 80 mA

jitter performance

Preliminary tests have qualitatively characterized jitter performance of the TNETS2021A device. Typical data from such tests is provided below. This information is for reference only and is not intended to be used as precise performance parameters for these devices.

receiver jitter tolerance

Receiver jitter-tolerance data is plotted in Figure 6 and Figure 7. The device meets DS-3 jitter-tolerance requirements (as specified in Bellcore TR-TSY-000499) for both Category I and Category II equipment (see Figure 6). The flat tolerance exhibited from 10 Hz to 40 kHz results from an overrange condition in the test equipment. Actual jitter tolerance in this range exceeded 20 UI, peak-to-peak. For STS-1, jitter-tolerance requirements (as specified in Bellcore TR-NWT-000253) are exceeded (see Figure 7).



Test setup:					
Instrument:	HP3784A	Transmit interface:	XCON 75 B3ZS	Receive interface:	Binary TTL
Temperature:	Room	Transmit clock:	Standard rate DS-3 + 0 ppm	Receive clock:	DS-3
Supply:	5 V	Transmit pattern:	PRBS 15 zero substitution 000	Receive pattern:	As per transmit
Filtering:	None			Receive hit threshold:	0.500 UIP

Figure 6. DS-3 Receiver Jitter-Tolerance Data

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receiver jitter tolerance (continued)

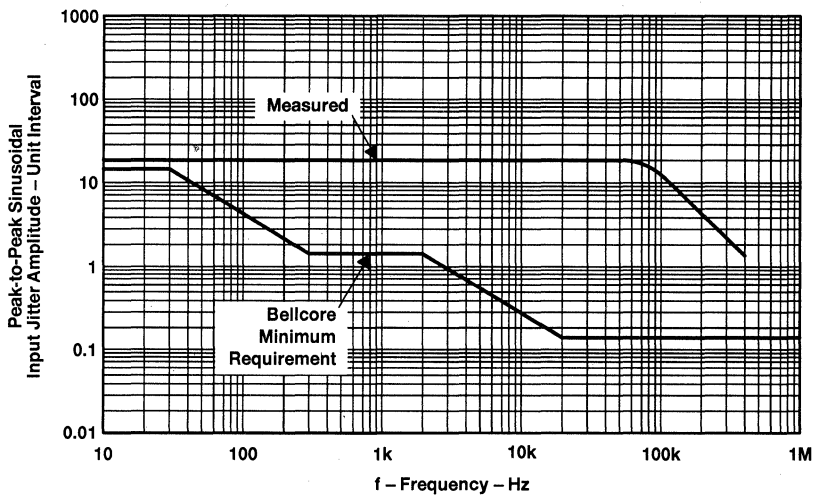

Figure 7. STS-1 Receive Jitter-Tolerance Measurement

jitter transfer

Jitter-transfer data for the receiver and transmitter sections of the TNETS2021A is plotted in Figure 8. The device does not, and is not designed to, meet the TR-TSY-000499 jitter-transfer requirements (<0.1 dB) for Category II equipment (regenerators). TR-TSY-000499 does not impose requirements for Category I equipment of this type. Such requirements are application dependent.

In a looped-back configuration (through the receive path and externally looped back through the transmit path), in the absence of applied input jitter, the amount of jitter introduced by the TNETS2021A is a maximum 0.065 UIs of peak-to-peak jitter over a jitter frequency range of 20 Hz to 1 MHz (filter with high pass of 10 Hz and a low pass of 1.1 MHz). With applied input jitter, the maximum output jitter is the applied input jitter plus the above jitter introduced by the TNETS2021A.

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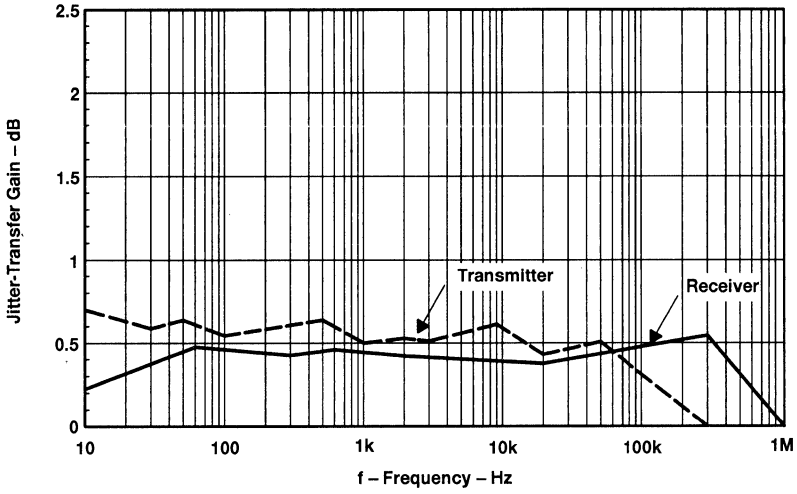
jitter transfer (continued)



Test setup (for receive-jitter testing; transmit similar):

Instrument:	HP3784A	Jitter input:	0.75-UI peak to peak	Receive interface:	Binary TTL
Temperature:	Room	Transmit interface:	XCON 75 B3ZS	Receive clock:	DS-3
Supply:	5 V	Transmit clock:	Standard rate DS-3 + 0 ppm	Receive pattern:	As per transmit
Filtering:	10-Hz HP	Transmit pattern:	PRBS 15 zero substitution 000	Receive hit threshold:	0.500 UIP

Figure 8. Typical Jitter-Transfer Data

jitter generation

For DS-3, Bellcore Technical Reference TR-TSY-000499, Issue 3, December 1989 specifies the maximum-jitter generation to be 1 UI peak-to-peak at the output of the terminal receiver for Category I Equipment.

For STS-1, Bellcore Technical Reference TR-NWT-000253, Issue 2, December 1991 specifies the maximum-jitter generation to be 1.5 UI peak-to-peak maximum at the output of the terminal receiver for Category I equipment.

In a looped-back configuration (through the transmit path and externally looped back through the receive path), the DS-3/STS-1 jitter generation within the TNETS2021A is 0.145 UI peak-to-peak maximum for all frequencies specified in these two standards.

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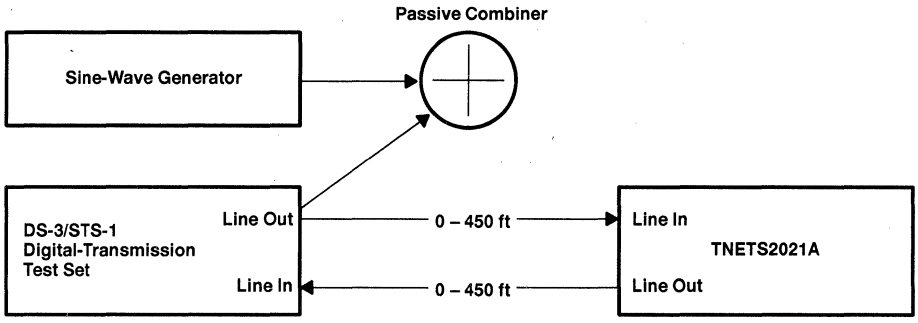

Figure 9. Interference-Margin Test Configuration

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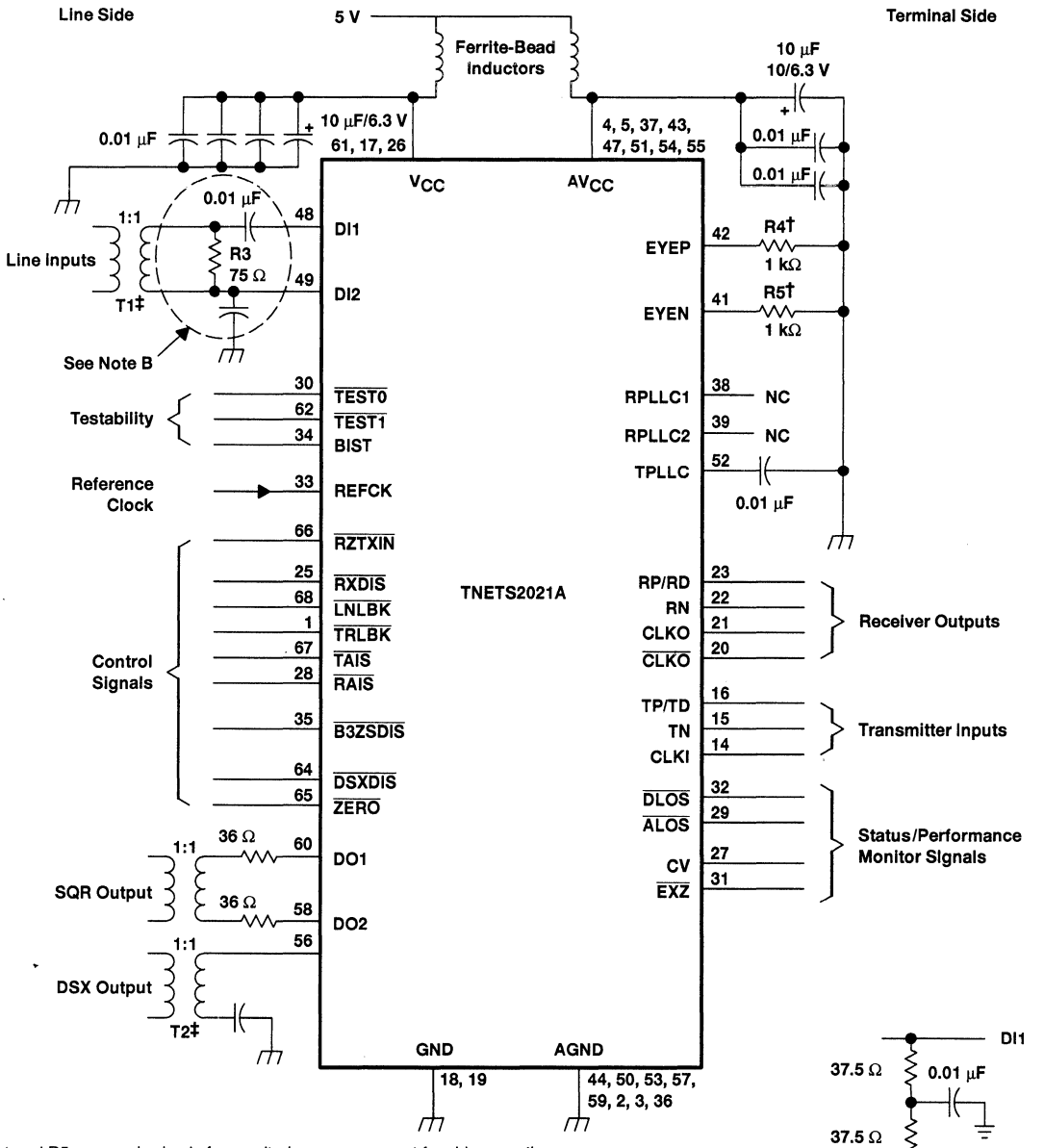

† R4 and R5 are required only for monitoring purposes, not for chip operation.
‡ T1 and T2 can be replaced with capacitors.
NOTES: A. All capacitors are 0.1 µF unless otherwise specified.
B. For differential-line inputs, replace R3 (75 Ω) and capacitors with two 37.5-Ω resistors and a 0.01-µF capacitor connected as shown.

Figure 10. External Connections for Operation

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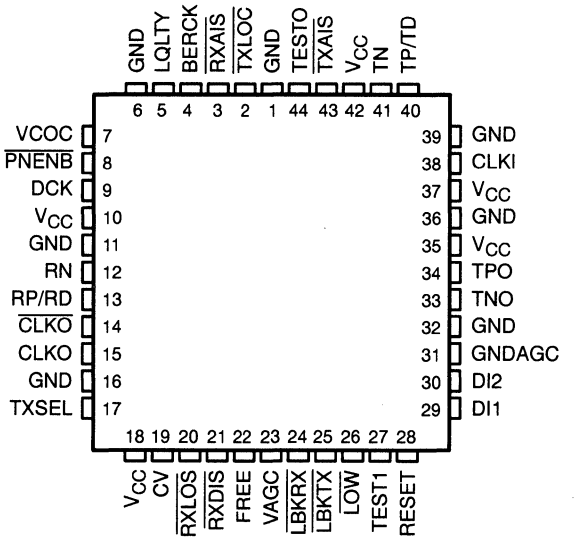
SDNS012A – AUGUST 1994 – REVISED DECEMBER 1994

- 6 312-kbit/s, 8 448-kbit/s, and 34 368-kbit/s Line Interface
- Automatic Gain Control (AGC)
- Line-Quality Monitor (10^{-6} Error Rate)
- Receive Loss-of-Signal and Transmit Loss-of-Clock Alarms
- Optional HDB3 Encoder/Decoder
- Two Loopbacks:
  - Receive to Transmit (Digital)
  - Transmit to Receive (Analog)
- Optional Transmit and Receive Alarm-Indication-Signal (AIS) Generators
- Rail or NRZ Terminal-Side I/O
- Meets CCITT Recommendation G.703
- Applications Include
  - Digital Cross-Connect Equipment
  - Remote Terminals
  - Terminal Interface for Multiplexers/ Demultiplexers
  - Switching Systems
  - GSU/DSU
- Packaged in 44-Lead Plastic Leaded Chip Carrier (FN)

FN PACKAGE
(TOP VIEW)



description

The TNETS2050 multirate receiver/transmitter provides the functions needed for terminating two (CCITT) line rates, 8 448 kbit/s and 34 368 kbit/s that are recommended by the International Telegraph and Telephone Consultative Committee (CCITT). It also provides a 6 312-kbit/s rate, which is specified in the Japanese NTT technical reference for high-speed digital-leased circuits. The device also provides an optional HDB3 encoder/decoder for 8 448-kbit/s and 34 368-kbit/s operation.

The device has automatic gain control (AGC). The TNETS2050 provides either a rail or nonreturn-to-zero (NRZ) data input/output, HDB3 error-rate monitor, alarm detection, and alarm-indication-signal (AIS) generators. Testing capability is provided by transmit and receive loopbacks.

The TNETS2050 is characterized for operation over the temperature range of –40°C to 85°C.

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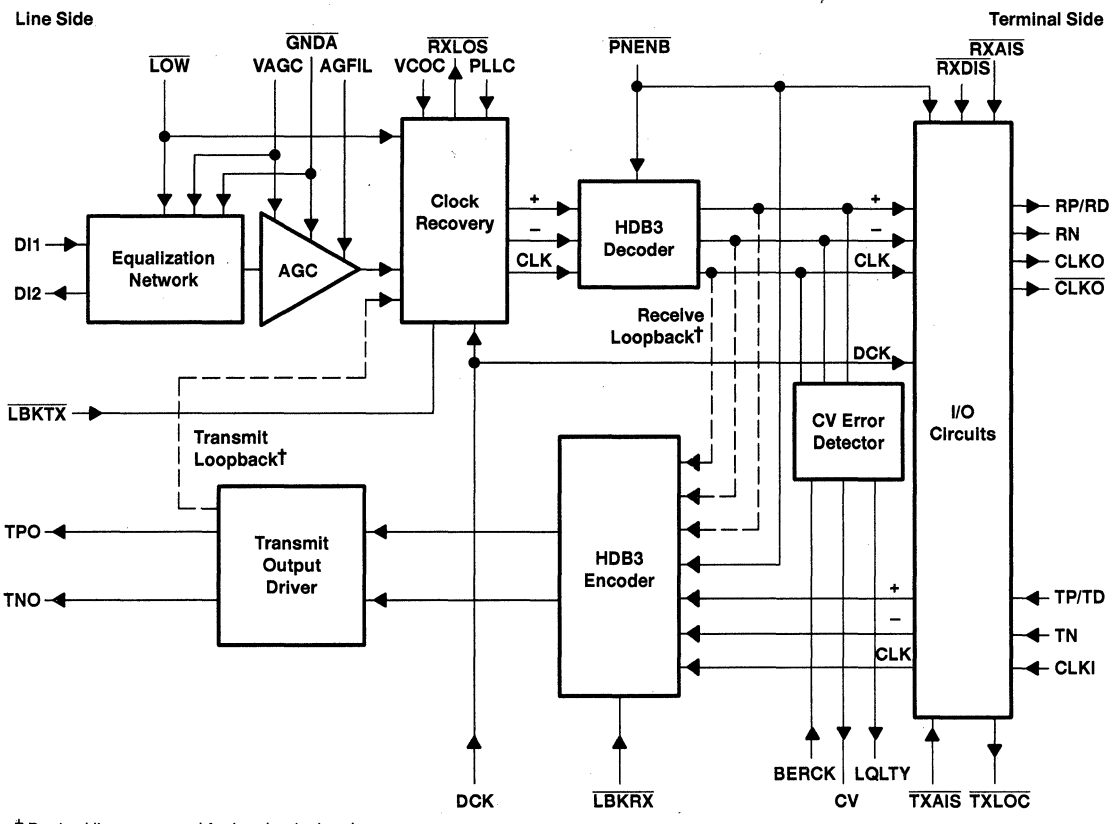
functional block diagram



† Dashed lines are used for loopback signals.

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detailed description

A symmetrical bipolar signal is applied to the data input DI1 on the line side, which requires an external 75-Ω termination. DI2 is a dc-reference voltage output that serves as an ac ground.

The equalization network is connected to an AGC circuit, which has a 20-dB dynamic range. The AGC has separate voltage and ground leads for noise immunity and uses an external capacitor as part of an AGC filter. The AGC output is connected to the clock-recovery function.

The clock-recovery circuit contains a phase-locked loop and supporting logic that generates a clock signal from the line signal. The signal input $\overline{\text{LOW}}$ selects the appropriate circuit in the clock-recovery function for the operating frequency and provides input attenuation for the receive-line signal. The line signal is monitored for loss of signal and provides an alarm indication on the $\overline{\text{RXLOS}}$ output. The clock-recovery circuit requires an external input reference clock (DCK) at the operating frequency. DCK is also used for generating and sending a receive alarm-indication signal (AIS). The generation and sending of AIS for recovered data is controlled by $\overline{\text{RXAIS}}$.

detailed description (continued)

The output of the clock-recovery circuit is connected to the HDB3 decoder or the I/O circuits. When the decoder is enabled, indications of coding-violation errors other than the normal HDB3 zero-substitution codes are provided as pulses on the output signal CV. An external input clock (BERCK) is used to generate a 10-second sampling window for detecting a 10^{-6} or greater error rate. The line-quality indication is provided on the output signal LQLTY.

Two terminal-side interfaces are provided, a positive- and negative-rail (RP and RN) or NRZ (D) interface. The selection is determined by the state placed on the input signal $\overline{\text{PNENB}}$. When a low is applied to $\overline{\text{PNENB}}$, the HDB3 decoder and HDB3 encoder are bypassed and terminal-side I/O is a positive- and negative-rail interface. When a high is applied to $\overline{\text{PNENB}}$, an NRZ (RD) interface is provided. Data is clocked out of TNETS2050 on negative edges of CLKO. Receive data and the clock signals are disabled and forced to the high-impedance state by placing a low on the receive disable input ($\overline{\text{RXDIS}}$). For a receive positive- and negative-rail interface, an inverted clock output ($\overline{\text{CLKO}}$) is also provided.

The terminal-side interface for the transmitter can either be positive- and negative-rail (TP and TN) or NRZ (TD) data, depending on the state of $\overline{\text{PNENB}}$. Data is clocked into the TNETS2050 on positive transitions of CLKI. The input clock is monitored for the loss of clock. When the input clock remains high or low, $\overline{\text{TXLOC}}$ is set low. The TNETS2050 also provides the capability to generate and insert AIS (an all 1s signal) that is independent of the transmit data. A low placed on $\overline{\text{TXAIS}}$ enables the transmit AIS generator.

Two loopbacks, transmit loopback and receive loopback, are provided. The transmit loopback connects the data path from the transmitter output driver to the clock-recovery circuit and disables the external receiver input. The transmit loopback is activated by placing a low on $\overline{\text{LBKTX}}$. The receive loopback connects the receive-data path to the transmit-output circuits and disables the transmit input. The receive loopback is activated by placing a low on $\overline{\text{LBKRX}}$.

For 6-Mbit/s operation, the device should be operated in the positive- and negative-rail mode to bypass the HDB3 decoder/encoder.

Terminal Functions

power supply and ground

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
GND	1, 6, 11, 16 32, 36, 39	Ground (0-V reference)
GNDAGC	31	Ground, AGC (0-V reference)
VAGC	23	Supply voltage, AGC. Isolate from V_{CC} using 1N914 or 1N4148 diode.
V_{CC}	10, 18, 35, 37, 42	Supply voltage, 5 V ± 5%

line-side I/O

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DI1	29	I (analog)	Data in 1. HDB3- or B8ZS-encoded bipolar receive data input.
DI2	30	O (analog)	Data in 2. The dc voltage reference for data input DI1. The TNETS2050 uses an internally generated voltage reference as an ac ground for the received data input. An external 0.1-µF capacitor in parallel with a 10-µF (6.3-V) tantalum capacitor is connected between DI2 and ground. No other connection should be made to DI2.
TNO	33	O 24 mA (TTL)	Transmit negative out. Line-side TNO is active low.
TPO	34	O 24 mA (TTL)	Transmit positive out. Line-side TPO is active low.

terminal-side I/O

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLKI	38	I (TTL)	Clock in. CLKI is the transmit-clock input for P- and N-rail and NRZ data. Transmit data is clocked into the TNETS2050 on the rising edge. CLKI must have a frequency tolerance of ±20 ppm for the 34 368-kbit/s operation and ±30 ppm for the 6 312- or 8 448-kbit/s operation (CCITT recommendation G.703). The duty cycle requirement for CLKI is 50% ±5% and is measured at the 1.4-V TTL threshold level.
$\overline{\text{CLKO}}$	14	O 8 mA (TTL)	Clock out. $\overline{\text{CLKO}}$ is inverted and positive- and negative-rail data is clocked out on the rising edge. $\overline{\text{CLKO}}$ is disabled in the NRZ mode.
CLKO	15	O 8 mA (TTL)	Clock out. CLKO is not inverted and receive positive- and negative-rail and NRZ data is clocked out on the falling edge.
RN	12	O 4 mA (TTL)	Receive negative. When $\overline{\text{PNENB}}$ is low, the HDB3 codec is bypassed and N-rail (RN) data is provided on RN. When $\overline{\text{PNENB}}$ is high, RN is forced to the high-impedance state.
RP/RD	13	O 4 mA (TTL)	Receive positive/receive data. When $\overline{\text{PNENB}}$ is low, the HDB3 codec is bypassed and P-rail (RP) data is provided on RP/RD. When $\overline{\text{PNENB}}$ is high, NRZ data (RD) is provided.
TN	41	I (TTL)	Transmit negative. When $\overline{\text{PNENB}}$ is low, the HDB3 codec is bypassed and transmit N-rail (TN) data is applied to TN. When $\overline{\text{PNENB}}$ is high, TN is disabled.
TP/TD	40	I (TTL)	Transmit positive/transmit data. When $\overline{\text{PNENB}}$ is low, the HDB3 codec is bypassed and transmit P-rail (TP) data is applied to TP/TD. When $\overline{\text{PHENB}}$ is high, NRZ transmit data (TD) is applied to TP/TD.

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Terminal Functions (Continued)

alarm signal outputs

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CV	19	O 2 mA (TTL)	Coding violation. CV is an active-high output. CV occurs when an HDB3 coding violation is detected in the received line-side data input. A coding violation is not part of the HDB3 zero-substitution code. A coding violation occurs because of noise or other impairments affecting the line-side signal. CV is disregarded in the P and N mode.
LQLTY	5	O 2 mA (TTL)	Line quality. LQLTY represents a gross estimate of the line quality, which is determined by counting the coding violations for 34-Mbit/s or 8-Mbit/s operation. If the line error rate exceeds a 10^{-6} threshold during a 10-second interval for the 34-Mbit/s rate or during a 40-second interval for the 8-Mbit/s rate, LQLTY goes active high. LQLTY is active low when coding violations do not exceed the 10^{-6} threshold for the correct interval. LQLTY is only valid when the appropriate clock signal is applied to BERCK. LQLTY is disregarded in the P and N mode of operation.
$\overline{\text{RXLOS}}$	20	O 2 mA (TTL)	Receive loss of signal. $\overline{\text{RXLOS}}$ is an active-low output. $\overline{\text{RXLOS}}$ occurs when the input data is zero for 20 to 32 clock cycles. Recovery occurs when the receive signal returns.
$\overline{\text{TXLOC}}$	2	O 2 mA (TTL)	Transmit loss of clock. $\overline{\text{TXLOC}}$ is an active-low output. $\overline{\text{TXLOC}}$ alarm occurs when the CLKI remains high or low for 20 to 32 clock cycles. Recovery occurs on the first input-clock transition.

control inputs

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BERCK	4	I (TTL)	Bit error-rate clock. BERCK establishes the time base for estimating the coding-violation error rate. For 34-Mbit/s operation, the clock frequency must be 6 kHz; for 8-Mbit/s operation, the clock frequency must be 1.5 kHz. BERCK should be left open for P- and N-mode operation.
DCK	9	I (TTL)	Reference clock. DCK is an operating frequency reference clock. For receive-signal clock recovery, ± 200-ppm frequency accuracy is adequate. If the transmit and receive AIS features are used, the frequency accuracy is ±20 ppm for 34 368 kbit/s and ±30 ppm for 8 448-kbit/s and 6 312-kbit/s operation. The duty cycle requirement for DCK is 50% ±5% as measured at the 1.4-V (TTL) threshold level.
$\overline{\text{LBKRX}}$	24	I (CMOS)	Loopback receive. When $\overline{\text{LBKRX}}$ is low, the TNETS2050 loops back receive data as transmit data. The receive data is sent to the terminal side, but the transmit data input on the terminal side is disabled (see Note 1).
$\overline{\text{LBKTX}}$	25	I (CMOS)	Loopback transmit. When $\overline{\text{LBKTX}}$ is low, the TNETS2050 loops back transmit data as receive data. The transmit data is sent on the line side, but the receive data input on the line side is disabled (see Note 1).
$\overline{\text{LOW}}$	26	I (CMOS)	Low frequency. When $\overline{\text{LOW}}$ is low, the TNETS2050 enables equalization- and input-attenuator settings for 6 312-kbit/s or 8 448-kbit/s operation. $\overline{\text{LOW}}$ also controls the clock-recovery high- or low-frequency range circuit.
$\overline{\text{PNENB}}$	8	I (CMOS)	P and N enable. When $\overline{\text{PNENB}}$ is low, the positive- and negative-rail interface is enabled and the HDB3 codec is bypassed. When $\overline{\text{PNENB}}$ is high, the terminal-side I/O data is NRZ and the HDB3 codec is enabled. $\overline{\text{PNENB}}$ must be held low for 6-Mbit/s operation.
RESET	28	I (CMOS)	Logic reset. RESET is enabled by TEST0 high.
$\overline{\text{RXAIS}}$	3	I (CMOS)	Receive alarm-indication signal. When $\overline{\text{RXAIS}}$ is low, the TNETS2050 generates AIS (all-ones signal) for the terminal-side receive output data. The line-side receive data path is disabled. DCK provides the clock source required for generating AIS.
$\overline{\text{RXDIS}}$	21	I (CMOS)	Receive disable. When $\overline{\text{RXDIS}}$ is low, the receive side of the TNETS2050 is disabled and the RN, RP/RD, CLKO, and $\overline{\text{CLKO}}$ outputs are forced to the high-impedance state.

NOTE 1: Simultaneously setting $\overline{\text{LBKTX}}$ and $\overline{\text{LBKRX}}$ low causes invalid outputs at the receive terminal-side and transmit line-side ports.

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Terminal Functions (Continued)

control inputs (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TEST1	27	I (CMOS)	Test mode. TEST1 is enabled by TEST0 high.
$\overline{\text{TXAIS}}$	43	I (CMOS)	Transmit AIS. When $\overline{\text{TXAIS}}$ is low, the TNETS2050 sends an AIS (all ones signal) for the line-side transmit output data. The terminal-side transmit data path is disabled. DCK provides the clock required for generating AIS.

miscellaneous

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
FREE	22		Not dedicated
TESTO	44	I (CMOS)	Test output. A high logic level enables chip-test modes. A low logic level enables normal operation.
TXSEL	17	I (CMOS)	Transmitter select. TXSEL high selects the old transmitter, which is the default for backward compatibility. TXSEL is used to select between the old and new transmitter designs.
VCOC	7	I/O (analog)	Leave floating

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 2) ..... −0.3 V to 7 V
Supply voltage range, AGC ..... −0.5 V to 6.5 V
Input voltage range, V_I ..... −0.5 V to V_{CC} +0.5 V
Operating free-air temperature range, T_A ..... −40°C to 85°C
Operating junction temperature, T_J ..... 150°C
Storage temperature range ..... −55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: All voltage values are with respect to GND.

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recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{AGC}	Supply voltage, AGC		$V_{CC}-0.5$		$V_{CC}-0.5$	V
V_{IH}	High-level input voltage	CMOS†	2			V
		TTL†	2			
		TTL	2			
V_{IL}	Low-level input voltage	CMOS†			0.8	V
		TTL†			0.8	
		TTL			0.8	
I_{OH}	High-level output current	8-mA CMOS			−8	mA
		2-mA TTL			−1	
		4-mA TTL			−2	
		24-mA TTL			−12	
I_{OL}	Low-level output current	8-mA CMOS			8	mA
		2-mA TTL			2	
		4-mA TTL			4	
		24-mA TTL			24	
T_A	Operating free-air temperature		−40		85	°C

† Input has a 100-kΩ internal pullup resistor.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	8-mA CMOS	V_{CC} = 4.75 V	I_{OH} = −8 mA	$V_{CC}-0.5$			V
		2-mA TTL		I_{OH} = −1 mA	$V_{CC}-0.5$			
		4-mA TTL		I_{OH} = −2 mA	$V_{CC}-0.5$			
		24-mA TTL		I_{OH} = −12 mA	$V_{CC}-0.5$			
V_{OL}	Low-level output voltage	8-mA CMOS	V_{CC} = 4.75 V	I_{OL} = 8 mA			0.4	V
		2-mA TTL		I_{OL} = 2 mA			0.4	
		4-mA TTL		I_{OL} = 4 mA			0.4	
		24-mA TTL		I_{OL} = 24 mA			0.4	
I_I	Input current	CMOS†	V_{CC} = 5.25 V			50		µA
		TTL†				50		
		TTL						
I_{CC}	Supply current		V_{CC} = 5.25 V					mA
I_{AGC}	Supply current, AGC		V_{AGC} = 4.75 V					mA
P_D	Power dissipation		V_{CC} = 5.25 V					mW
P_{AGC}	Power dissipation, AGC		V_{AGC} = 4.75 V					mW
C_i	Input capacitance	CMOS†				5.5		pF
		TTL†				5.5		
		TTL				5.5		

† Input has a 100-kΩ internal pullup resistor.

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switching characteristics

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
t_r	Rise time	8-mA CMOS	CL = 25 pF			ns
		2-mA TTL	CL = 15 pF			
		4-mA TTL	CL = 15 pF			
		24-mA TTL	CL = 25 pF			
t_f	Fall time	8-mA CMOS	CL = 25 pF			ns
		2-mA TTL	CL = 15 pF			
		4-mA TTL	CL = 15 pF			
		24-mA TTL	CL = 25 pF			

timing diagrams

Detailed timing diagrams are shown in Figures 4 through 7. All output times are measured with the following load capacitances:

OUTPUT	C_L MAX
8-mA CMOS	25 pF
24-mA TTL	25 pF
4-mA TTL	15 pF
2-mA TTL	15 pF

Timing requirements are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

line-side timing

The TNETS2050 line-side timing requirements are designed so that the line-side output mask at the transformer output meets the wave shapes specified in CCITT recommendation G.703 for 34-Mbit/s and 8-Mbit/s operation and NTT technical reference for high-speed digital-leased circuit service for 6-Mbit/s operation. The pulse masks for each of the three modes of operation are shown in Figures 1, 2, and 3 (refer to the corresponding standard cited in each case for further details regarding the interface).

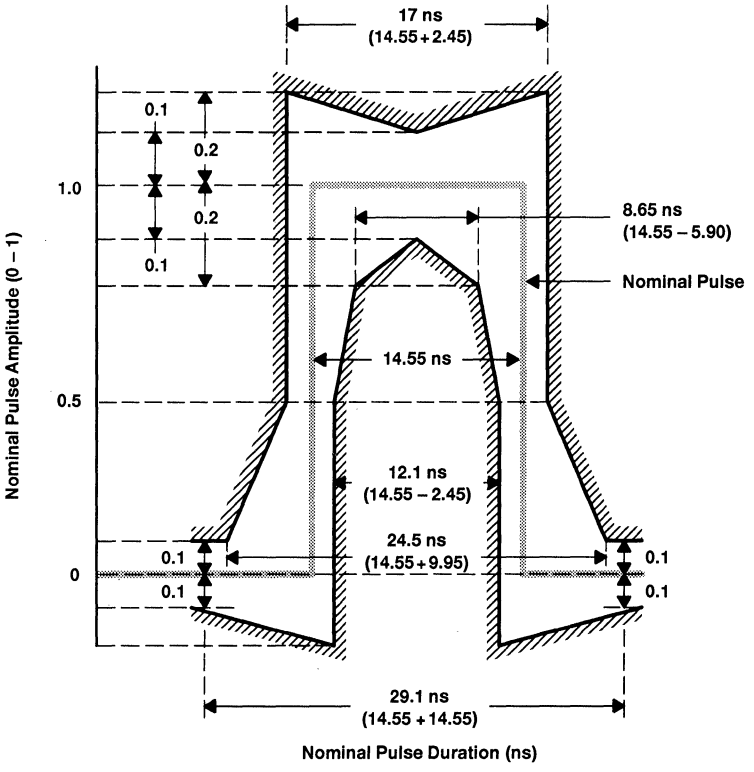


Figure 1. Line-Side Pulse Mask at the 34 368-kbit/s Interface

PRODUCT PREVIEW

line-side timing (continued)

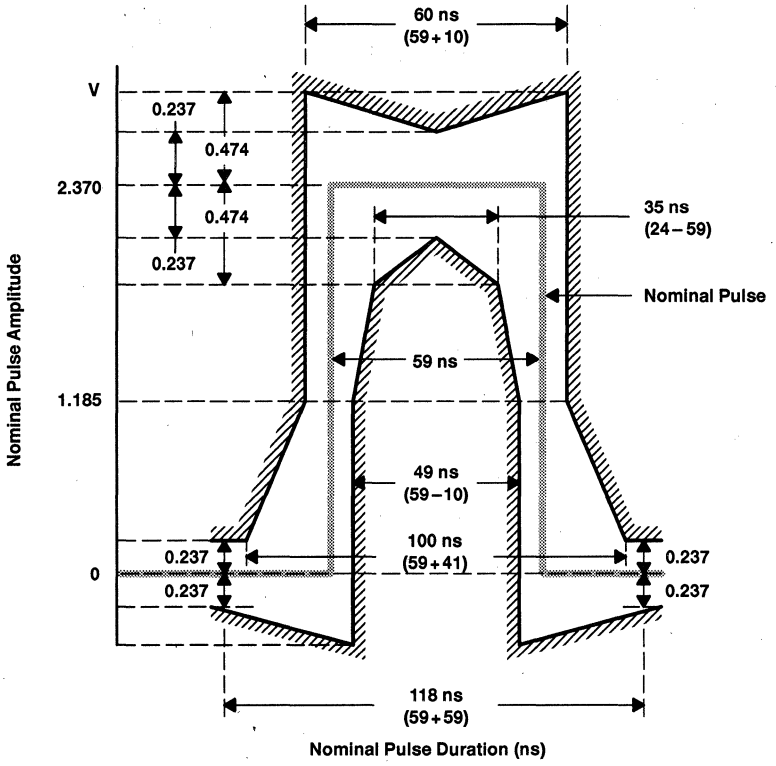


Figure 2. Line-Side Pulse Mask at the 8 448-kbit/s Interface

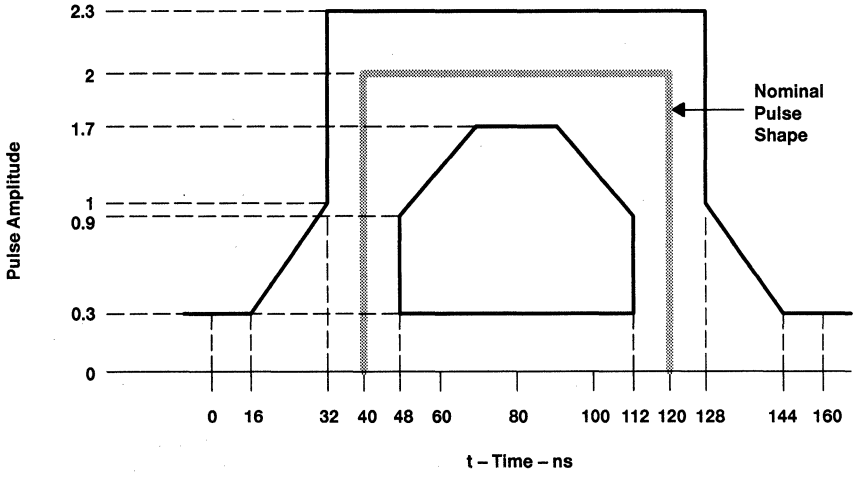


Figure 3. Line-Side Pulse Mask at the 6 312-kbit/s Interface

PRODUCT PREVIEW

terminal-side timing

timing requirements (see Notes 3 and 4 and Figure 4)

NO.			MIN	NOM	MAX	UNIT
		Duty cycle, CLKI	45%		55%	
1	$t_{c(CLKI)1}$	Clock cycle time, CLKI, 34 368 kbit/s interface		29.10		ns
2	$t_{c(CLKI)2}$	Clock cycle time, CLKI, 8 448 kbit/s interface		118.37		ns
3	$t_{c(CLKI)3}$	Clock cycle time, CLKI, 6 312 kbit/s interface		158.43		ns
4	$t_{su(TP/TD)}$	Setup time, TP/TD valid before CLKI↑	3			ns
5	$t_{h(TP/TD)}$	Hold time, TP/TD valid after CLKI↑	2			ns

NOTES: 3. CLKI symmetry is measured at the 1.4-V threshold to assure symmetrical output waveforms.
4. CLKI can be 6, 8, or 34 MHz.

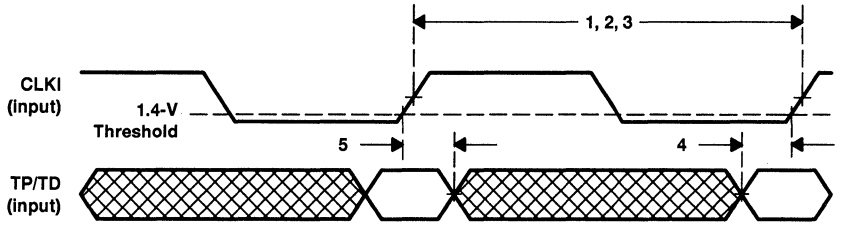


Figure 4. Terminal-Side NRZ Transmit Input

operating characteristics (see Notes 5 and 6 and Figure 5)

NO.			MIN	TYP	MAX	UNIT
		Duty cycle, CLKO	45%		55%	
1	$t_{c(CLKO)1}$	Clock cycle time, CLKO, 34 368 kbit/s interface		29.10		ns
2	$t_{c(CLKO)2}$	Clock cycle time, CLKO, 8 448 kbit/s interface		118.37		ns
3	$t_{c(CLKO)3}$	Clock cycle time, CLKO, 6 312 kbit/s interface		158.43		ns
4	$t_{d(RP/RD)}$	Delay time from CLKO↓ to RP/RD valid	−5		5	ns
5	$t_{d(CV)}$	Delay time from CLKO↓ to CV↑	−5		5	ns

NOTES: 5. CLKO can be 6, 8, or 34 MHz.
6. CLKO symmetry is measured at the 50% amplitude level.

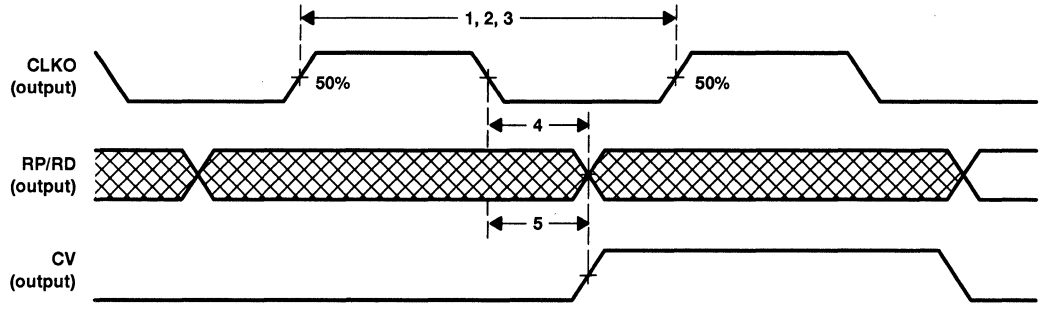


Figure 5. Terminal-Side NRZ Receive Output

PRODUCT PREVIEW

terminal-side timing (continued)

timing requirements (see Notes 3 and 4 and Figure 6)

NO.			MIN	NOM	MAX	UNIT
		Duty cycle, CLKO	45%		55%	
1	$t_{c(CLKI)1}$	Clock cycle time, CLKI, 34 368 kbit/s interface		29.10		ns
2	$t_{c(CLKI)2}$	Clock cycle time, CLKI, 8 448 kbit/s interface		118.37		ns
3	$t_{c(CLKI)3}$	Clock cycle time, CLKI, 6 312 kbit/s interface		158.43		ns
4	$t_{su(TP)}$	Setup time, TP valid before CLKI↑	3			ns
4	$t_{su(TD)}$	Setup time, TD valid before CLKI↑	3			ns
4	$t_{su(TN)}$	Setup time, TN valid before CLKI↑	3			ns
5	$t_{h(TP)}$	Hold time, TP valid after CLKI↑	2			ns
5	$t_{h(TD)}$	Hold time, TD valid after CLKI↑	2			ns
5	$t_{h(TN)}$	Hold time, TN valid after CLKI↑	2			ns

NOTES: 3. CLKI symmetry is measured at the 1.4-V threshold to ensure symmetrical output waveforms.
4. CLKI can be 6, 8, or 34 MHz.

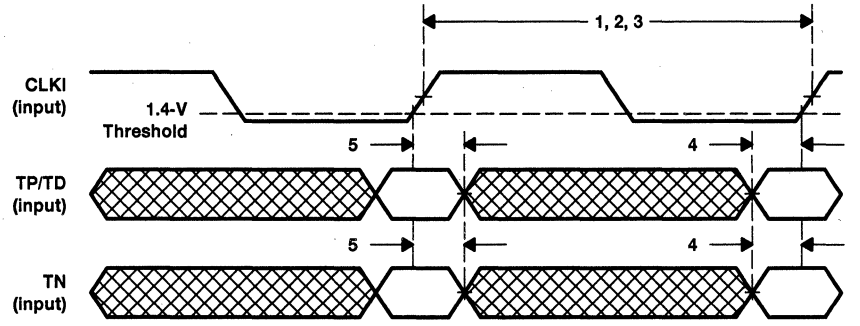


Figure 6. Terminal-Side P- and N-Rail Transmit Input

PRODUCT PREVIEW

operating characteristics (see Notes 5 and 6 and Figure 7)

NO.			MIN	TYP	MAX	UNIT
		Duty cycle, CLKO	45%		55%	
1	$t_{c(CLKO)1}$	Clock cycle time, CLKO, 34 368 kbit/s interface		29.10		ns
2	$t_{c(CLKO)2}$	Clock cycle time, CLKO, 8 448 kbit/s interface		118.37		ns
3	$t_{c(CLKO)3}$	Clock cycle time, CLKO, 6 312 kbit/s interface		158.43		ns
4	$t_{d(CLKO)4}$	Delay time from $\overline{CLKO}\uparrow$ to CLKO$\downarrow$			2	ns
5	$t_{d(CL-RPV)}$	Delay time from CLKO$\downarrow$ to RP valid	−5		6	ns
5	$t_{d(CL-RDV)}$	Delay time from CLKO$\downarrow$ to RD valid	−5		6	ns
5	$t_{d(CL-RNV)}$	Delay time from CLKO$\downarrow$ to RN valid	−5		6	ns

NOTES: 5. CLKO can be 6, 8, or 34 MHz.
6. CLKO symmetry is measured at the 50% amplitude level.

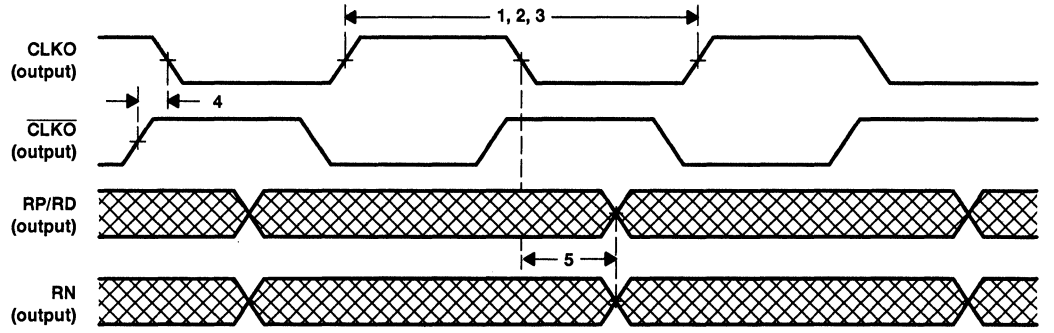


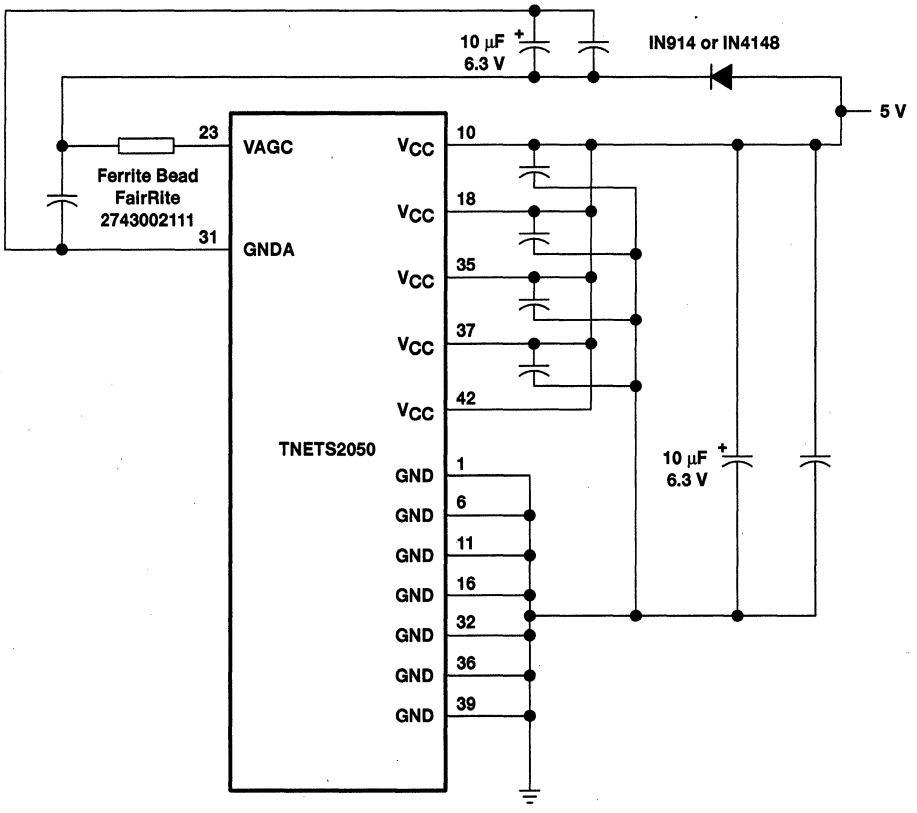
Figure 7. Terminal-Side P- and N-Rail Receive Output

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

power supply

The TNETS2050 has separate power-supply terminals labeled V_{CC} and VAGC. The VAGC supply voltage is connected to the internal AGC amplifier and requires isolation from the V_{CC} supply voltage as indicated in Figure 8. Separate bypass networks are used for connecting V_{CC} and VAGC to 5 V. The bypass network for the VAGC consists of an IN4148 or IN914 diode and a 10-µF (6.3-V) tantalum capacitor connected in parallel with a 0.1-µF capacitor as shown in Figure 8. The 0.1-µF decoupling capacitors should be of radio-frequency quality and connected adjacent to the device.



All capacitors are 0.1 µF unless otherwise specified.

Figure 8. TNETS2050 Supply-Voltage Connections

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

overview

line-side input impedance

The TNETS2050 line-side input impedance depends on the state of the $\overline{\text{LOW}}$ input and the value of the operating rate. Table 1 lists the input impedance of the TNETS2050 at the operating line rates, which are 1/2 the value of the bit rates.

Table 1. TNETS2050 Input Impedance

CONDITION	MINIMUM INPUT IMPEDANCE (OHMS)
$\overline{\text{LOW}}$ = 1, Line-side rate = 17 184 kbit/s	1260
$\overline{\text{LOW}}$ = 0, Line-side rate = 4 224 kbit/s	2390
$\overline{\text{LOW}}$ = 0, Line-side rate = 3 156 kbit/s	3670

line-side input sensitivity

The TNETS2050 input-voltage sensitivity depends on the state of the $\overline{\text{LOW}}$ input as shown in Table 2.

Table 2. TNETS2050 Input Sensitivity

$\overline{\text{LOW}}$ INPUT STATE	INPUT SENSITIVITY (PEAK VOLTS)	
	MIN	MAX
0	0.5	2.7 (6 and 8 Mbit/s)
1	0.15	1.1 (34 Mbit/s)

line-side input circuit

Figure 9 illustrates the components required for operating the TNETS2050 at 34 368, 8 448, or 6 312 kbit/s. The transformer should have a frequency response of 0.2 to 80 MHz with an insertion loss of 1 dB maximum. A Coilcraft transformer (part no. WB-1010 or equivalent) is used in the circuit. This gives return-loss and isolation-voltage values that meet or exceed requirements.

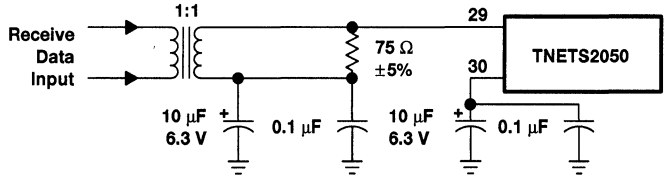


Figure 9. Line-Side Input Circuit

line-side output characteristics

The TNETS2050 line-side output switches from rail to rail on both TPO and TNO. This provides the maximum voltage swing and makes the output voltage depend on the 5-V power-supply input to the device. The external circuit must be designed to ensure that amplitude requirements are met.

PRODUCT PREVIEW

PRINCIPLES OF OPERATION

line-side output circuits

Figure 10 illustrates the output circuit required for operating the TNETS2050 for a 34 368-kbit/s application. The transformer and resistors shown ensure that the output waveform meets the CCITT mask for 34 368-kbit/s transmission and that the device is operated within the current limits of the TTL 24-mA outputs. The transformer should have a frequency response of 0.1–100 MHz with an insertion loss of 1dB maximum.

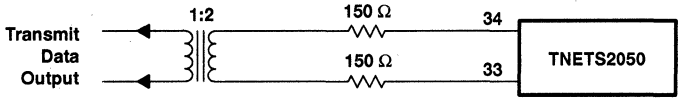


Figure 10. Line-Side Output Circuit (34 368 kbit/s)

Figure 11 shows a variation of the circuit in Figure 10. This circuit improves performance in applications where a plastic device is mounted in a socket. The additional low-pass filter compensates for possible overshoot caused by inductance created by the device/socket interface. The transformer should have a frequency response of 0.1–100 MHz with an insertion loss of 1 dB maximum.

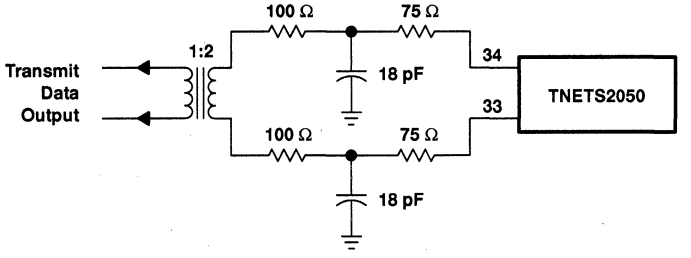
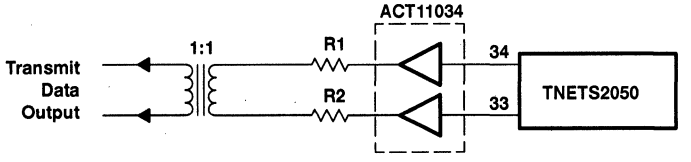


Figure 11. Line-Side Output Circuit (34 368 kbit/s)

line-side output circuits

The peak voltage and current output requirements for 6312 and 8448 kbit/s operation are different from those required for 34 368-kbit/s operation. Figure 12 illustrates the output circuit required for 6 312-kbit/s and 8 448-kbit/s operation. The transformer should have a frequency response of 0.01–50 MHz with an insertion loss of 1 dB maximum. The transformer, drivers, and resistors ensure that the output waveform meets the CCITT masks for these rates and that the TNETS2050 device is operated within the current limits of the TTL 24-mA outputs.



For 8 448-kbit/s operation: R1 and R2 = 27 Ω
For 6 312-kbit/s operation: R1 and R2 = 36 Ω

Figure 12. Line-Side Output Circuit (8 448 and 6 312 kbit/s)

PRODUCT PREVIEW

APPLICATION INFORMATION

jitter tolerance

CCITT recommendation G.823 specifies that network equipment must be able to accommodate and tolerate levels of jitter up to certain specified limits. The TNETS2050 accommodates and tolerates more input jitter than the level of input jitter specified by the CCITT.

With input jitter applied to the TNETS2050 line-side receive input DI1, the TNETS2050 properly recovers the clock, decodes the HDB3, and outputs error-free NRZ data beyond the CCITT-specified jitter input and frequency ranges. Performance characteristics are shown in Figure 13 for 34.368-Mbit/s operation and in Figure 14 for 8.448-Mbit/s operation.

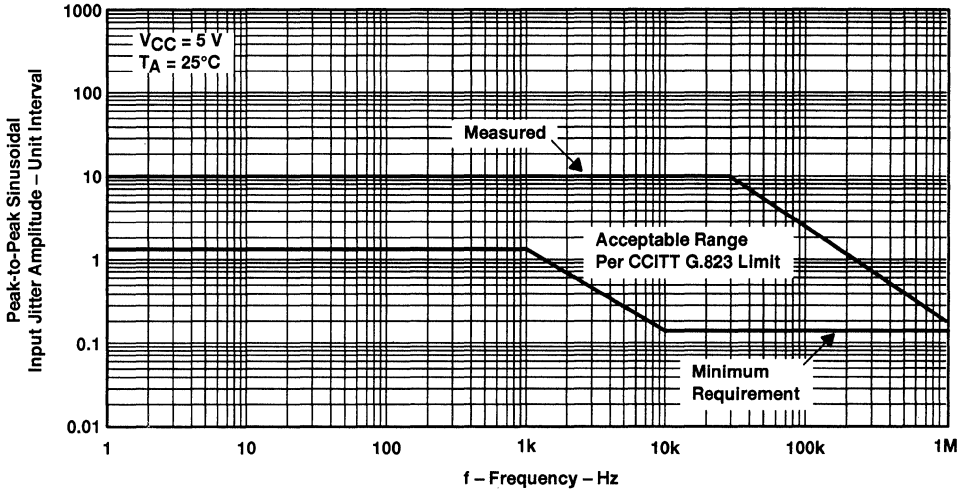


Figure 13. TNETS2050 Jitter Tolerance (Worst Case) at 34.368 Mbit/s

PRODUCT PREVIEW

APPLICATION INFORMATION

jitter tolerance (continued)

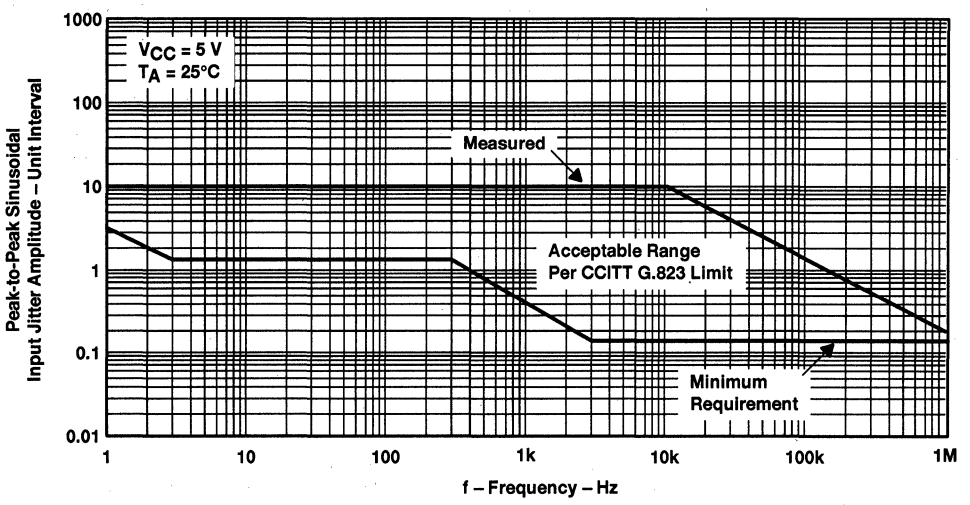


Figure 14. TNETS2050 Jitter Tolerance (Worst Case) at 8.448 Mbit/s

maximum output jitter in absence of input jitter

CCITT recommendation G.823 specifies that it is necessary to restrict the amount of jitter generated by individual equipment. Actual limits depend on the type of equipment and application.

In the absence of applied jitter, the receive path of the TNETS2050 introduces a maximum of 0.05 unit intervals (UIs) peak-to-peak sinusoidal jitter over the following frequency ranges:

At 8.448 Mbit/s: 20 Hz to 400 kHz
At 34.368 Mbit/s: 100 Hz to 800 kHz

This operation is with the TNETS2050 terminated by the external components and component values specified in the terminal functions table for VCOC.

jitter transfer

Transfer of jitter through the individual equipment is characterized by the relationship between the applied input jitter and the resulting output jitter as a function of frequency. CCITT recommendation G.823 specifies that it is important to restrict jitter gain.

With applied input jitter at the TNETS2050 receive terminals, the maximum output jitter is no greater than the level of input jitter plus 0.05-UI peak-to-peak sinusoidal jitter.

This operation is over the same CCITT specified frequency ranges and external terminations as described in the maximum output jitter section.

PRODUCT PREVIEW

APPLICATION INFORMATION

interfering-tone tolerance

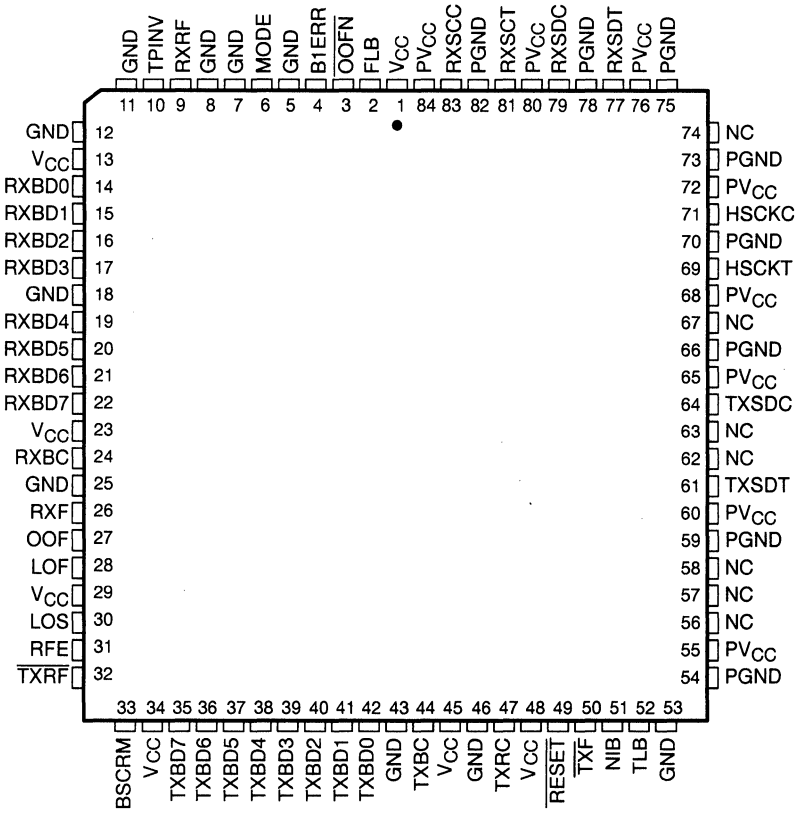
The TNETS2050 recovers the clock and presents error-free output to the receive terminal-side interface in the presence of a pseudorandom binary-sequence (PRBS) interfering tone. The PRBS interfering tone has the same data sequence as the data input for the line rates in Table 3.

Table 3. Interfering-Tone Tolerance

DATA RATE (Mbit/s)	TONE RATE (Mbit/s)	MAXIMUM TONE LEVEL (dB)	DATA SEQUENCE
34.368	34.368 ± 100 ppm	−18	$2^{23}-1$
8.448	8.448 ± 100 ppm	−4	$2^{15}-1$
6.312	6.312 ± 100 ppm	−4	$2^{15}-1$

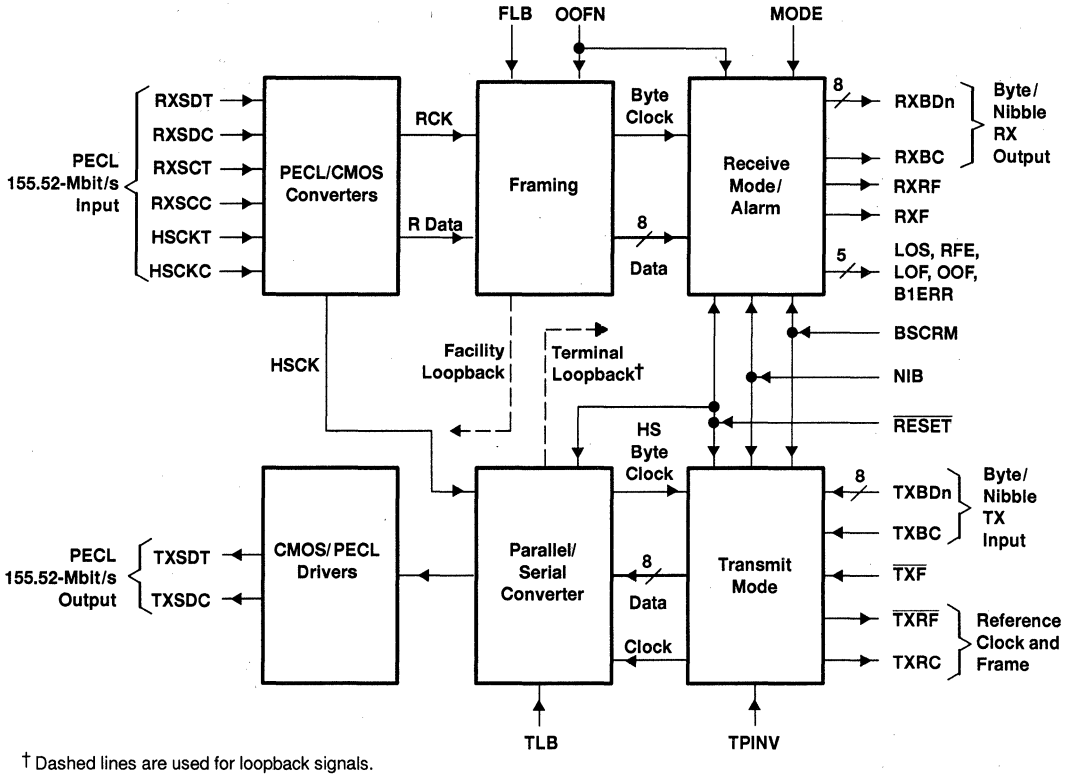
- Member of the Texas Instruments Digital Communication Series of Standard DS-3 and SONET Devices
- Transmits and Receives at the STS-3/STM-1 Rate of 155.52 Mbit/s
- Converts 155.52-Mbit/s Data and Clock to Byte/Nibble Data and Clock
- Provides Pseudo-ECL (PECL) Levels for 155.52-Mbit/s Data and Clock
- Detects the Frame of the Incoming Signal and Transmits a Frame-Indication Signal
- Provides User-Selectable Options for:
  - Signal Scrambling/Descrambling
  - B1 Parity Calculation
- Provides Loss-of-Signal (LOS), Loss-of-Frame (LOF), and Receive Frame-Error (RFE) Flags for 155.52-Mbit/s Data
- Packaged in 84-Pin Plastic Leaded Chip Carrier (PLCC) Using 50-mil Center-to-Center Spacings

FN PACKAGE
(TOP VIEW)



NC – No internal connection

functional block diagram



† Dashed lines are used for loopback signals.

description

The TNETS2301C provides a complete frame-synchronization function for a STS-3/STM-1 line interface. The device frame aligns the incoming 155.52-Mbit/s serial-data stream and converts it to a byte or nibble data output. A byte or nibble clock output is also provided along with a frame-indication signal. In the transmit direction, the TNETS2301C accepts byte or nibble data and clock and outputs a 155.52-Mbit/s serial-data stream. The device can be programmed to provide signal descrambling/scrambling and B1 byte parity checking/generation. The TNETS2301C also monitors the incoming serial data and provides a loss-of-signal (LOS) indicator. In addition, loopback of both the facility serial line input and the terminal byte/nibble input is provided.

The TNETS2301C provides two modes of frame synchronization: tracking or nontracking. When the tracking mode is activated, the device finds the frame of the incoming signal and monitors the signal continuously for frame-alignment errors. In this operating mode, outputs are provided to indicate a receive frame error (RFE), out-of-frame error (OOF), or loss-of-frame error (LOF). If the nontracking mode is activated, the device finds the frame of the incoming signal but no subsequent monitoring of the signal is provided. In this mode, the RFE, OOF, and LOF outputs are deactivated.

The serial data and clock inputs and outputs operate at PECL levels (ECL levels referenced to 5 V instead of 0 V). Of the remaining I/O signals, the inputs are TTL compatible and the outputs are CMOS. The TNETS2301C is specified for operation over a temperature range of –40°C to 85°C.

serial data input to byte/nibble output

The serial inputs to the TNETS2301C consist of a 155.52-Mbit/s data stream and a corresponding 155.52-MHz clock signal from an optical-to-electrical converter, clock-recovery circuit, or similar function. Both the serial data and clock inputs operate at differential PECL levels. The serial data is clocked into the device on a positive transition of the clock signal. A serial search for the framing bytes (A1, A2) is performed on the incoming data in accordance with the selected frame-synchronization mode. If the tracking mode is selected (MODE = low), the device continues to monitor the incoming data stream after the frame has been established and the LOF, OOF, and RFE indicators are enabled. If the nontracking mode is selected (MODE = high), the incoming data is not monitored after the frame has been found and the LOF, OOF, and RFE indicators are disabled.

If the tracking mode is selected and an out-of-frame (OOF) condition exists, the TNETS2301C initiates a search for the framing pattern. The framing pattern is defined in ANSI standards and CCITT recommendations as six bytes (F6, F6, F6, 28, 28, 28) for an STS-3/STM-1 signal. These bytes occupy the A1 and A2 byte positions in the SONET/SDH frame. Once the frame has been found, the serial data is converted to parallel data and output in either nibble or byte format depending on the state of the nibble (NIB) input. If NIB is high, the data is output in nibble format along with a 38.88-MHz clock. If NIB is low, the data is output in byte format along with a 19.44-MHz clock. The device also provides a framing pulse output (RXF) that goes high when the third A2 byte appears on the data output.

When tracking mode is selected, the RFE, LOF, and OOF indicators are enabled. RFE is synchronous with the third A2 byte and becomes active high when a framing bit error is detected. The signal is active for one clock cycle when byte format is selected and two clock cycles when nibble format is selected. If four consecutive frames have framing errors, OOF goes high. This output remains high for at least two frames. If OOF remains high for 24 frames, LOF goes high. LOF remains high until eight consecutive error-free frames are received. When an out-of-frame condition occurs (OOF goes high), the device begins a new search for the framing pattern. The device also begins a new search for the framing pattern if $\overline{\text{OOFN}}$ is taken low for two RXBC clock cycles.

The TNETS2301C provides signal scrambling/descrambling and B1 parity checking/generation if the tracking mode is selected. When BSCRM is high, signal scrambling/descrambling and B1 parity checking/generation are both enabled and all the bytes after the third C1 byte are scrambled. The B1 parity errors are indicated with B1ERR. A positive output pulse is sent out for each bit of the B1 byte in error. The pulses are clocked out with the RXBC receive clock, and each pulse is one-byte clock period long. There can be up to eight pulses on the B1ERR lead in a given frame. The ordering of the bit-error pulses is from bit 7 to bit 0. For example, if the pulses out of B1ERR form the sequence 01000100, errors are detected in bit 6 and bit 2 of the B1 byte.

The data and clock outputs of the TNETS2301C can be selected to follow either a nibble or byte format when the tracking mode is enabled. If the nibble mode is selected (NIB is high), the clock output frequency is 38.88 MHz and the data byte is output as two nibbles on RXBD3–RXBD0. The most significant nibble is transmitted first with the most significant bit of the data-byte output on RXBD3. The least significant bit of the data byte is transmitted on RXBD0 of the second nibble. If the byte mode is selected (NIB is low), the clock output frequency is 19.44 MHz and the most significant bit is output on RXBD7.

When the nontracking mode is selected, the TNETS2301C begins a search for the framing pattern when $\overline{\text{OOFN}}$ is taken low for two RXBC clock periods. The RXBDn output data is set to zero on the rising edge of $\overline{\text{OOFN}}$. Valid data is transmitted after the framing pattern is detected. The RFE, OOF, and LOF alarm indicators are disabled when the nontracking mode is selected. In addition, the scrambler/descrambler is disabled, and the data can be output only in byte format.

The serial input data can be looped to the serial data output (facility loopback) independent of whether tracking mode or nontracking mode is selected. To implement a facility loopback, the facility loopback (FLB) input is taken high. The received data is passed to the terminal side and looped back to the serial output. The terminal transmit data is blocked by the looped signal and ignored.

byte/nibble data input to serial data output

Nibble or byte data is clocked into the TNETS2301C on negative transitions of the data input clock (TXBC). If nibble mode is selected, the data is input using the TXBD3–TXBD0 inputs with TXBD3 being the most significant bit. If byte mode is selected, the data is input using the TXBD7–TXBD0 inputs with TXBD7 being the most significant bit. For a given byte, the most significant bit is transmitted first on the serial data output. If the scrambling and B1 parity generation functions are to be performed by the TNETS2301C, a framing pulse ($\overline{\text{TXF}}$) identifying the location of the third A2 byte in the incoming data is required. To facilitate the generation of TXBC and $\overline{\text{TXF}}$, the TNETS2301C provides a reference byte or nibble clock (TXRC) and a reference frame ($\overline{\text{TXRF}}$) output that are generated from the 155.52-MHz clock inputs (HSCKT and HSCKC). $\overline{\text{TXRF}}$ is active low, has a nominal width of 51.44 ns, and occurs at the frame rate of 8 kHz. TXRC occurs at a rate of 19.44 MHz or 38.88 MHz depending upon the state of the NIB input.

The byte/nibble input data is looped back to the byte/nibble output data if the terminal loopback (TLB) input is high. When TLB is selected, the byte/nibble input data is passed to the line-side serial data output and looped back to the terminal-side output. The received line data is blocked by the looped signal and ignored. The byte/nibble input data is scrambled and the B1 parity byte is generated if the BSCRM input is high. If BSCRM is low, these functions are bypassed. The byte/nibble input data is converted to serial format for output via the serial output clock (TXSC).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BSCRM	33	I (TTL)	B1 generation/checking and scramble/descramble. When BSCRM is high, the TNETS2301C provides B1 checking and descrambling of the receive incoming data and B1 generation and scrambling of the transmit output data. To generate B1 errors for test purposes, the value for B1 calculated for the transmit frame is exclusive ORed with the value of B1 received on the transmit terminal-side input. To ensure that the correct value for B1 is transmitted for normal operation, the value for B1 received on the transmit terminal-side input must be 00 (hex). To disable B1 generation/checking and scrambling/descrambling by this device, BSCRM is taken low.
B1ERR	4	O (CMOS)	B1 parity-error indication. A positive-pulse error indication is provided for each B1 bit parity error, up to a maximum of eight error indications. Each error indication is one clock-cycle wide in the byte mode and two clock-cycles wide in the nibble mode.
FLB	2	I (TTL)	Facility loopback. When FLB is high, the serial input data is looped backed to the serial output. The received serial data is also passed to the terminal-side output. The facility and terminal loopbacks cannot be used at the same time. This produces erroneous results.
GND	5, 7, 8, 11, 12, 18, 25, 43, 46, 53		Ground (0-V reference)
HSCKC	71	I (PECL)	High-speed clock complement. HSCKC is used with HSCKT to provide a differential input clock.
HSCKT	69	I (PECL)	High-speed clock true. HSCKT is used in conjunction with HSCKC to provide the 155.52-MHz reference and transmit clock.
LOF	28	O (CMOS)	Loss of frame. LOF goes high when an out-of-frame (OOF) condition persists for three milliseconds (24 frames) or longer. LOF goes low when eight error-free framing patterns are detected after the OOF state is exited. This indication is valid only when MODE is low (tracking mode).
LOS	30	O (TTL)	Loss of signal. LOS goes high when the incoming receive data signal stays high or low for 100 µs (or greater) or if the incoming receive clock stays high or low for one microsecond ±750 ns. LOS goes low when two consecutive error-free framing patterns are detected and a loss of the second condition is not detected between the framing patterns.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
MODE	6	I (TTL)	MODE selects either the tracking or the nontracking mode of operation for the receive side. When MODE is low, the device operates in the tracking mode. In this mode of operation, the device searches for and tracks frame alignment. The framing pulse output RXF is held low when out of frame occurs while byte or nibble data is provided. When MODE is high, the device enters the nontracking mode and frame alignment is declared valid on the first indication of the framing pattern (not the second). If external circuitry finds that an invalid framing pattern has occurred, MODE sends a low signal to $\overline{\text{OOFN}}$ to reinitiate the frame search.
NC	56, 57, 58, 62, 63, 67, 74		No connection
NIB	51	I (TTL)	Nibble/byte control. If NIB is high, the terminal interface is nibble wide; if NIB is low, the terminal interface is byte wide.
OOF	27	O (CMOS)	Out of frame. OOF goes high when errors are detected in the three A2 bytes of four consecutive framing patterns (when A2A2A2 ≠ 282828 while in frame alignment). OOF goes low when two error-free consecutive framing patterns are detected (when A1A1A1A2A2A2 = F6F6F6282828). This indication is valid only when MODE is low (tracking mode).
$\overline{\text{OOFN}}$	3	I (CMOS)	Out-of-frame negative. A low-level signal on $\overline{\text{OOFN}}$ for two RXBC clock periods starts a new frame search. $\overline{\text{RESET}}$ and $\overline{\text{OOFN}}$ should be applied after a mode change occurs. $\overline{\text{OOFN}}$ must occur either at the same time as the $\overline{\text{RESET}}$ or after the $\overline{\text{RESET}}$ becomes inactive.
PGND	54, 59, 66, 70, 73, 75, 78, 82		PECL ground (0-V reference)
PV_{CC}	55, 60, 65, 68, 72, 76, 80, 84		PECL supply voltage, 5 V ± 5%
$\overline{\text{RESET}}$	49	I (CMOS)	The device is reset when $\overline{\text{RESET}}$ is held low for a minimum of 105 ns. The device should be reset after power is applied or the state of BSCRM, MODE, or NIB is changed.
RFE	31	O (CMOS)	Receive framing error. RFE goes high when any bit in the receive-framing pattern is in error and the device is not in an out-of-frame state. When present, the indication occurs at the start of the third A2 framing byte in the framing pattern in the receive-side data. This indication is valid only when MODE is low (tracking mode).
RXBC	24	O (CMOS)	Receive clock. RXBC outputs the data from the TNETS2301C on the falling edge of this signal. The clock frequency is either 19.44 MHz (byte clock) or 38.88 MHz (nibble clock).
RXBD7–RXBD0	22–19, 17–14	O (CMOS)	Receive data. RXBD7–RXBD0 is the terminal-side output data, either byte or nibble wide that depends on the state of NIB. Receive data is still provided when OOF occurs.
RXF	26	O (CMOS)	Receive frame. RXF provides a positive pulse in synchronization with the third A2 byte of the SONET/SDH frame. When OOF occurs, RXF is held low.
RXRF	9	O (TTL)	Receive reference frame. RXRF is an 8-kHz output derived from the differential input serial clock RXSC. RXRF is one clock-cycle wide.
RXSCC	83	I (PECL)	Receive serial clock complement. RXSCC is used with RXSCT to provide a differential clock input.
RXSCT	81	I (PECL)	Receive serial clock true. RXSCT is used with RXSCC to provide a differential clock input that accompanies the serial data input.
RXSDC	79	I (PECL)	Receive serial data input complement. RXSDC is used with RXSDT to provide a differential data input.
RXSDT	77	I (PECL)	Receive serial data input true. RXSDT is used with RXSDC to provide a differential data input.
TLB	52	I (TTL)	Terminal loopback. When TLB is high, the transmit terminal input is looped back to the receive terminal output. The transmit terminal input data is also sent to the transmit serial output. The facility and terminal loopbacks cannot be activated at the same time. This produces erroneous results.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TPINV	10	I (TTL)	Transmit path invert. When TPINV is low, $\overline{\text{TXRF}}$ is active low and clocked out on the rising edge of TXRC. In addition, $\overline{\text{TXF}}$ is active low and clocked into the TNETS2301C, along with TXBDn, on the falling edge of TXBC. When TPINV is high, $\overline{\text{TXRF}}$ becomes an active-high output that is clocked out on the falling edge of TXRC. Also, $\overline{\text{TXF}}$ becomes an active-high input that is clocked into the TNETS2301C, along with TXBDn, on the rising edge of TXBC.
TXBC	44	I (CMOS)	Transmit byte/nibble clock. The clock rate is either 19.44 MHz (byte data) or 38.88 MHz (nibble data). The data on TXBDn is clocked into the TNETS2301C on the falling edge of TXBC when TPINV is low and on the rising edge when TPINV is high.
TXBD7–TXBD0	35–42	I (CMOS)	Transmit data. TXBD7 – TXBD0 is the terminal-side input data (either byte or nibble wide). TXBD7 is the most significant bit for byte-wide input. TXBD3 is the most significant bit for nibble-wide input.
$\overline{\text{TXF}}$	50	I (CMOS)	Transmit frame. $\overline{\text{TXF}}$ is synchronous with the third A2 byte of the terminal-side input and is required to perform signal scrambling. $\overline{\text{TXF}}$ is active low when TPINV is low and active high when TPINV is high.
TXRC	47	O (CMOS)	Transmit reference clock. TXRC is a clock occurring at the rate of 19.44 MHz or 38.88 MHz depending on the state of NIB. $\overline{\text{TXRF}}$ is clocked out on the positive transition of TXRC when TPINV is low and on the negative transition of TXRC when TPINV is high.
$\overline{\text{TXRF}}$	32	O (CMOS)	Transmit reference frame. $\overline{\text{TXRF}}$ is a one-byte clock-wide pulse occurring at the frame rate of 8 kHz. $\overline{\text{TXRF}}$ is active low when TPINV is low and active high when TPINV is high.
TXSDC	64	O (PECL)	Transmit serial data output complement. TXSDC has an inverted PECL data output.
TXSDT	61	O (PECL)	Transmit serial data output true. TXSDT has a noninverted PECL data output.
V_{CC}	1, 13, 23, 29, 34, 45 48		Supply voltage, 5 V ± 5%

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Supply voltage range, PV_{CC}, PECL ..... −0.5 V to 7 V
Input voltage range: TTL ..... −1.2 V to 7 V
PECL ..... 0 V to PV_{CC}
Input/output clamp current range ..... −50 mA to 50 mA
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
PV_{CC}	Supply voltage, PECL		4.75	5.25	V
V_{IH}	High-level input voltage	TTL	2		V
		PECL (see Note 2)	3.8		V
V_{IH}	High-level input voltage, CMOS	V_{CC} = 4.75 V	3.32		V
		V_{CC} = 5.25 V	3.67		
V_{IL}	Low-level input voltage, CMOS	V_{CC} = 4.75 V		1.42	V
		V_{CC} = 5.25 V		1.57	
V_{IL}	Low-level input voltage	TTL		0.8	V
		PECL (see Note 2)		3.4	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage, TTL		V_{CC} = 4.75 V,	I_{IK} = −18 mA			−1.2	V
V_{OH}	High-level output voltage	CMOS	V_{CC} = 4.75 V,	I_{OH} = −4 mA	4.25			V
		TTL	V_{CC} = 4.75 V,	I_{OH} = −2 mA	4.25			V
		PECL	PV_{CC} = 5 V,	I_{OH} = −22.4 mA	4		4.3	V
V_{OL}	Low-level output voltage	TTL	V_{CC} = 4.75 V,	I_{OL} = 4 mA			0.5	V
		CMOS	V_{CC} = 4.75 V,	I_{OL} = 4 mA			0.5	V
		PECL	PV_{CC} = 5 V,	I_{OL} = 7.6 mA	3		3.4	V
I_I	Input current, TTL/CMOS		V_{CC} = 5.25 V,	V_I = V_{CC} or GND			±1	µA
I_{IH}	High-level input current, PECL		V_{CC} = 5.25 V,	V_I = 4.45 V			25	µA
I_{IL}	Low-level input current, PECL		V_{CC} = 5.25 V,	V_I = 3.35 V			25	µA
I_{CC1}	Supply current‡		V_{CC} = 5.25 V, f = 155.52 Mbit/s	I_O = 0,			100	mA
I_{CC2}	Supply current§		V_{CC} = 5.25 V,	f = 155.52 Mbit/s			175	mA
C_i	Input capacitance, TTL					4		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ PECL outputs are unterminated.
§ PECL outputs are terminated with a 50-Ω resistor to 3 V.

timing requirements, C_L = 25 pF (see Notes 3 and 4 and Figure 1)

		MIN	NOM	MAX	UNIT
$t_{w(RXSCH)}$	Pulse duration, RXSC high	2.9			ns
$t_{w(RXSCL)}$	Pulse duration, RXSC low	2.9			ns
$t_{c(RXSC)}$	Clock cycle time, RXSC		6.43		ns
$t_{su(RXSD)}$	Setup time, RXSD before RXSC↑	2			ns
$t_{h(RXSD)}$	Hold time, RXSD after RXSC↑	1			ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

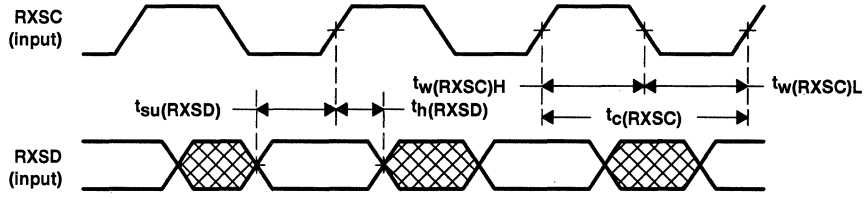


Figure 1. Line-Side Input Clock and Data

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 2)

		MIN	TYP	MAX	UNIT
$t_{w(RXF)}$	Pulse duration, RXF		51.44		ns
$t_{w(RXBCH)}$	Pulse duration, RXBC high	23			ns
$t_{w(RXBCL)}$	Pulse duration, RXBC low	23			ns
$t_{c(RXBC)}$	Clock cycle time, RXBC		51.44		ns
$t_{d(RCL-RDV)}$	Delay time after RXBC↓ to RXBD valid	–1		6	ns
$t_{d(RCL-RFH)}$	Delay time after RXBC↓ to RXF↑	0		6	ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

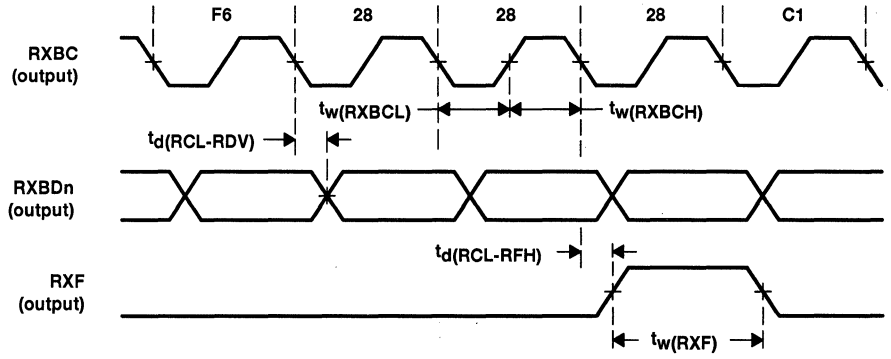


Figure 2. Terminal-Side Byte Output

timing requirements, C_L = 25 pF (see Notes 3 and 4 and Figure 3)

		MIN	NOM	MAX	UNIT
$t_{w(TXBCH)}$	Pulse duration, TXBC high	18			ns
$t_{w(TXBCL)}$	Pulse duration, TXBC low	18			ns
$t_{c(TXBC)}$	Clock cycle time, TXBC		51.44		ns
$t_{su(TXBD)1}$	Setup time before TXBC↓, TXBD	5			ns
$t_{h(TXBD)1}$	Hold time after TXBC↓, TXBD	5			ns
$t_{su(TXF)1}$	Setup time before TXBC↓, $\overline{TXF}$	5			ns
$t_{h(TXF)1}$	Hold time before TXBC↓, $\overline{TXF}$	5			ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

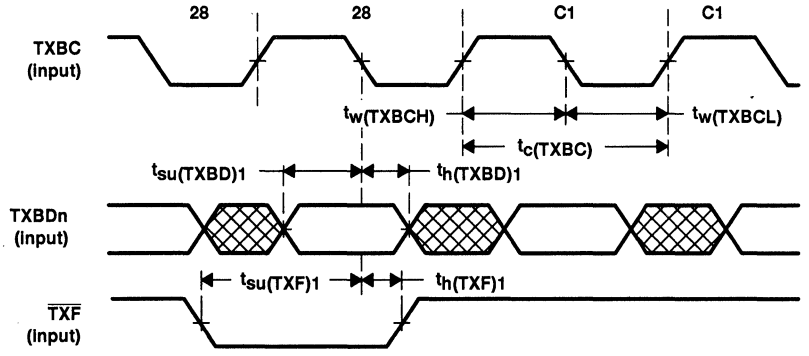


Figure 3. Terminal-Side Byte Input (TPINV low)

timing requirements, C_L = 25 pF (see Notes 3 and 4 and Figure 4)

		MIN	NOM	MAX	UNIT
$t_{w(TXBCH)}$	Pulse duration, TXBC high	18			ns
$t_{w(TXBCL)}$	Pulse duration, TXBC low	18			ns
$t_{c(TXBC)}$	Clock cycle time, TXBC		51.44		ns
$t_{su(TXBD)2}$	Setup time before TXBC↑, TXBD	5			ns
$t_{h(TXBD)2}$	Hold time after TXBC↑, TXBD	5			ns
$t_{su(TXF)2}$	Setup time before TXBC↑, $\overline{TXF}$	5			ns
$t_{h(TXF)2}$	Hold time after TXBC↑, $\overline{TXF}$	5			ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

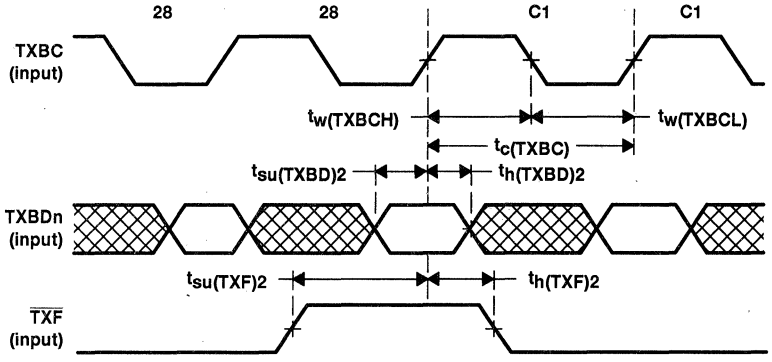


Figure 4. Terminal-Side Byte Input (TPINV high)

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 5)

		MIN	TYP	MAX	UNIT
$t_{w(RXF)}$	Pulse duration, RXF high		51.44		ns
$t_{w(RXBCH)}$	Pulse duration, RXBC high	9			ns
$t_{w(RXBCL)}$	Pulse duration, RXBC low	9			ns
$t_{c(RXBC)}$	Clock cycle time, RXBC		25.72		ns
$t_{d(RCL-RDV)}$	Delay time after RXBC↓ to RXBD valid	–1		6	ns
$t_{d(RCL-RFH)}$	Delay time after RXBC↓ to RXF↑	0		6	ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

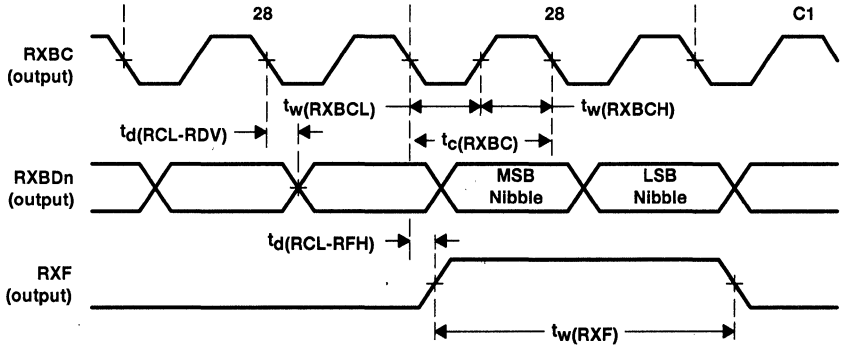


Figure 5. Terminal-Side Nibble Output

timing requirements, C_L = 25 pF (see Notes 3 and 4 and Figure 6)

		MIN	NOM	MAX	UNIT
$t_{w(TXBCH)}$	Pulse duration, TXBC high	9			ns
$t_{w(TXBCL)}$	Pulse duration, TXBC low	9			ns
$t_{c(TXBC)}$	Clock cycle time, TXBC		25.72		ns
$t_{su(TXBD)3}$	Setup time before TXBC↓, TXBD	5			ns
$t_{h(TXBD)3}$	Hold time after TXBC↓, TXBD	5			ns
$t_{su(TXF)3}$	Setup time before TXBC↓, $\overline{TXF}$	5			ns
$t_{h(TXF)3}$	Hold time after TXBC↓, $\overline{TXF}$	5			ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

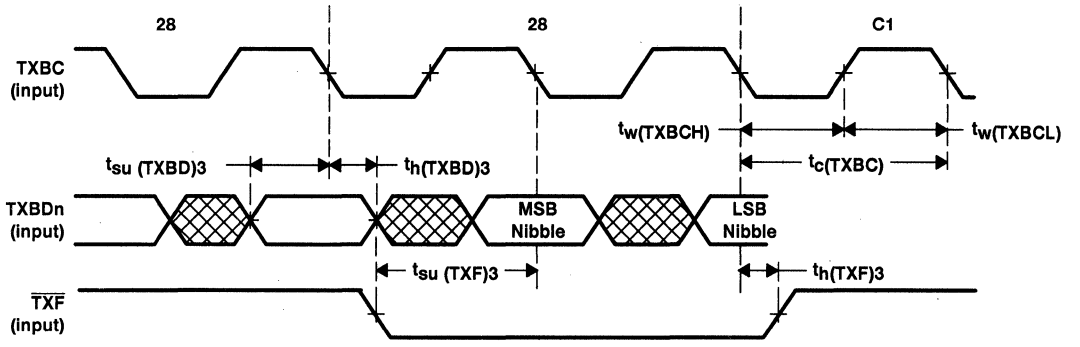


Figure 6. Terminal-Side Nibble Input (TPINV low)

timing requirements, C_L = 25 pF (see Notes 3 and 4 and Figure 7)

		MIN	NOM	MAX	UNIT
$t_{w(TXBCH)}$	Pulse duration, TXBC high	9			ns
$t_{w(TXBCL)}$	Pulse duration, TXBC low	9			ns
$t_{c(TXBC)}$	Clock cycle time, TXBC		25.72		ns
$t_{su(TXBD)4}$	Setup time before TXBC↑, TXBD	5			ns
$t_{h(TXBD)4}$	Hold time after TXBC↑, TXBD	5			ns
$t_{su(TXF)4}$	Setup time before TXBC↑, $\overline{TXF}$	5			ns
$t_{h(TXF)4}$	Hold time before TXBC↑, $\overline{TXF}$	5			ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

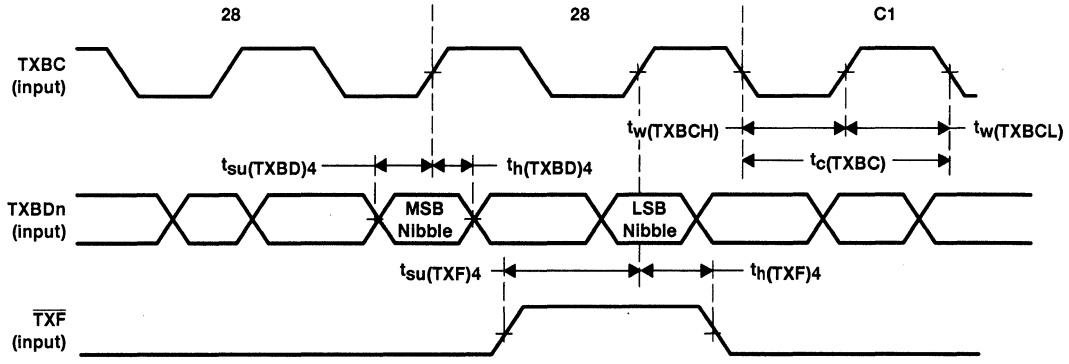


Figure 7. Terminal-Side Nibble Input (TPINV high)

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 8)

		MIN	TYP	MAX	UNIT
$t_{w(TXRFL)}$	Pulse duration, $\overline{TXRF}$ low		51.44		ns
$t_{w(TXRCH)}$	Pulse duration, TXRC high	23			ns
$t_{w(TXRCL)}$	Pulse duration, TXRC low	23			ns
$t_{c(TXRC)}$	Clock cycle time, TXRC		51.44		ns
$t_{d(TCH-TFL)}$	Delay time after TXRC↑ to $\overline{TXRF}$↓	0		6	ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

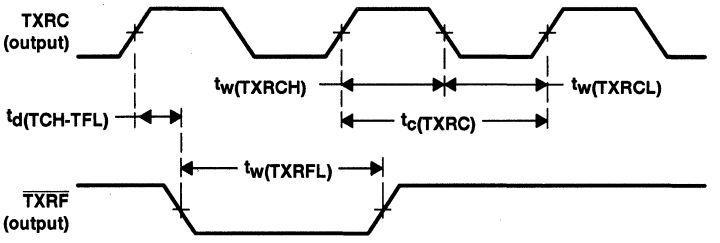


Figure 8. Terminal-Side Byte Reference Signals Output (TPINV low)

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 9)

		MIN	TYP	MAX	UNIT
$t_{w(TXRFH)}$	Pulse duration, $\overline{TXRF}$ high		51.44		ns
$t_{w(TXRCH)}$	Pulse duration, TXRC high	23			ns
$t_{w(TXRCL)}$	Pulse duration, TXRC low	23			ns
$t_{c(TXRC)}$	Clock cycle time, TXRC		51.44		ns
$t_{d(TCH-TPH)}$	Delay time after TXRC↑ to $\overline{TXRF}$↑	0		6	ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

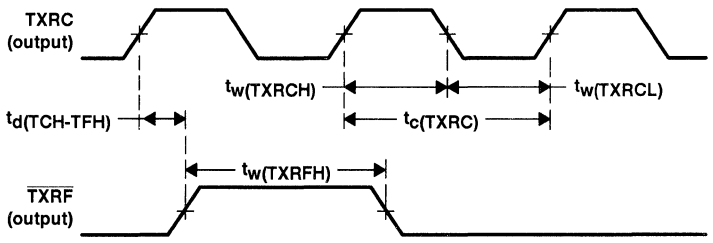


Figure 9. Terminal-Side Byte Reference Signals Output (TPINV high)

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 10)

		MIN	TYP	MAX	UNIT
$t_{w(TXRFL)}$	Pulse duration, $\overline{TXRF}$ low		25.72		ns
$t_{w(TXRCH)}$	Pulse duration, TXRC high	9			ns
$t_{w(TXRCL)}$	Pulse duration, TXRC low	9			ns
$t_{c(TXRC)}$	Clock cycle time, TXRC		25.72		ns
$t_{d(TCH-TFL)}$	Delay time after TXRC↑ to $\overline{TXRF}$↓	0		6	ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

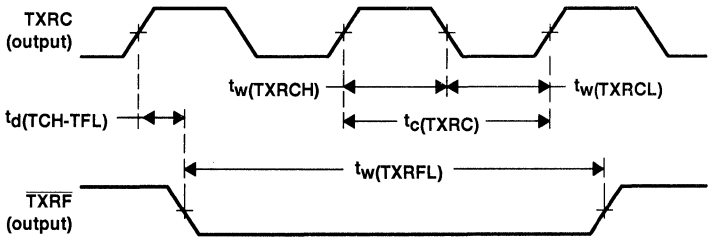


Figure 10. Terminal-Side Nibble Reference Signals Output (TPINV low)

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 11)

		MIN	TYP	MAX	UNIT
$t_{w(TXRFH)}$	Pulse duration, $\overline{TXRF}$ high		25.72		ns
$t_{w(TXRCH)}$	Pulse duration, TXRC high	9			ns
$t_{w(TXRCL)}$	Pulse duration, TXRC low	9			ns
$t_{c(TXRC)}$	Clock cycle time, TXRC		25.72		ns
$t_{d(TCL-TFH)}$	Delay time after TXRC↓ to $\overline{TXRF}$↑	0		6	ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

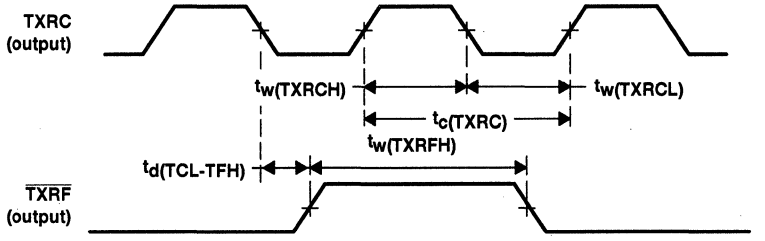


Figure 11. Terminal-Side Nibble Reference Signals Output (TPINV high)

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 12)

		MIN	MAX	UNIT
$t_{d(OFH-OOH)}$	Delay time after $\overline{OOFN}$↑ to OOF↑	0	312	ns
$t_{d(OFH-LOH)}$	Delay time after $\overline{OOFN}$↑ to LOF↑	0	312	ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

timing requirements, C_L = 25 pF (see Notes 3 and 4 and Figure 12)

		MIN	MAX	UNIT
$t_{w(OOFNL)}$	Pulse duration, $\overline{OOFN}$ low	105		ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

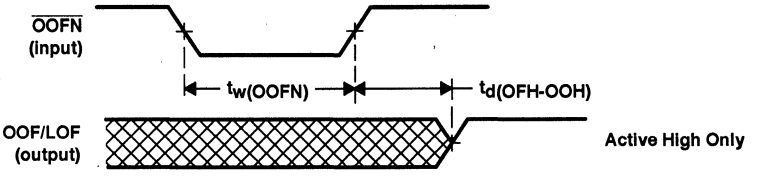


Figure 12. $\overline{OOFN}$ Resetting Frame

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 13)

		MIN	MAX	UNIT
$t_{d(RSH-TCH)}$	Delay time after $\overline{RESET}\uparrow$ to TXRC↑	6	30	ns
$t_{d(TCH-TFL)}$	Delay time after TXRC↑ to $\overline{TXRF}\downarrow$	0	6	ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

timing requirements, C_L = 25 pF (see Notes 3, 4, and Figure 13)

		MIN	MAX	UNIT
$t_{w(RESETL)}$	Pulse duration, $\overline{RESET}$ low	105		ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

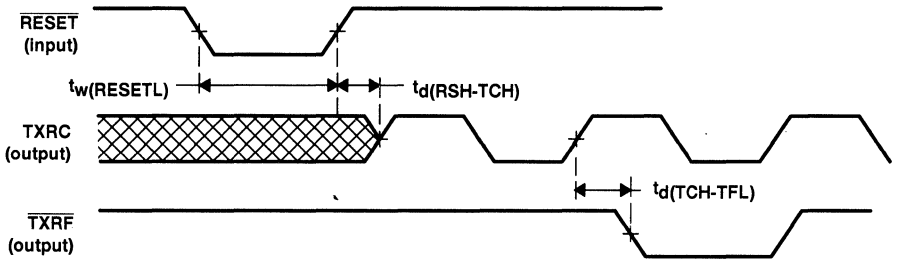


Figure 13. $\overline{RESET}$ Effect of Reference Clock and Frame (TPINV low)

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 14)

		MIN	MAX	UNIT
$t_{d(RSH-TCH)}$	Delay time after $\overline{RESET}\uparrow$ to TXRC↑	6	30	ns
$t_{d(TCH-TFH)}$	Delay time after TXRC↑ to $\overline{TXRF}\uparrow$	0	6	ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

timing requirements, C_L = 25 pF (see Notes 3 and 4 and Figure 14)

		MIN	MAX	UNIT
$t_{w(RESETL)}$	Pulse duration, $\overline{RESET}$ low	105		ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

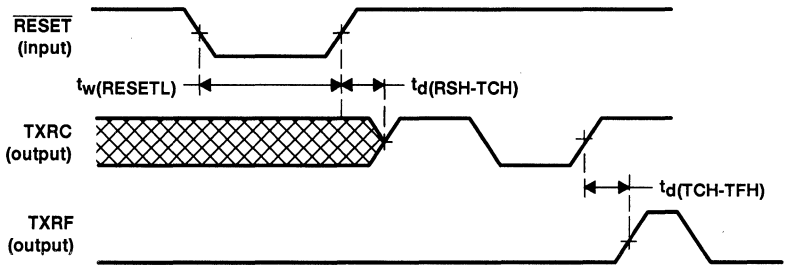
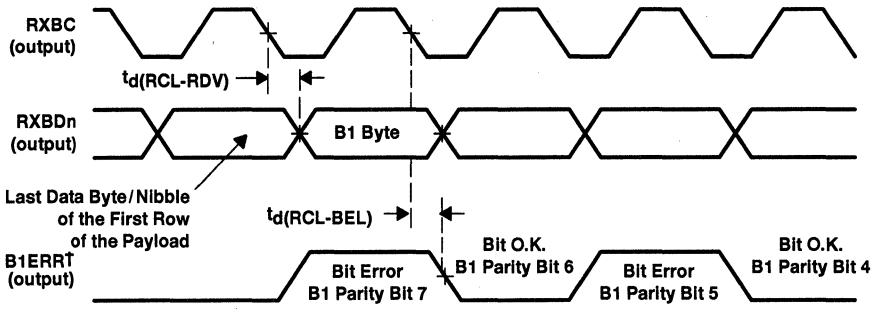


Figure 14. $\overline{RESET}$ Effect of Reference Clock and Frame (TPINV high)

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 15)

		MIN	MAX	UNIT
$t_{d(RCL-RDV)}$	Delay time after RXBC↓ to RXBD valid	0	6	ns
$t_{d(RCL-BEL)}$	Delay time after RXBC↓ to B1ERR↓	0	6	ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.



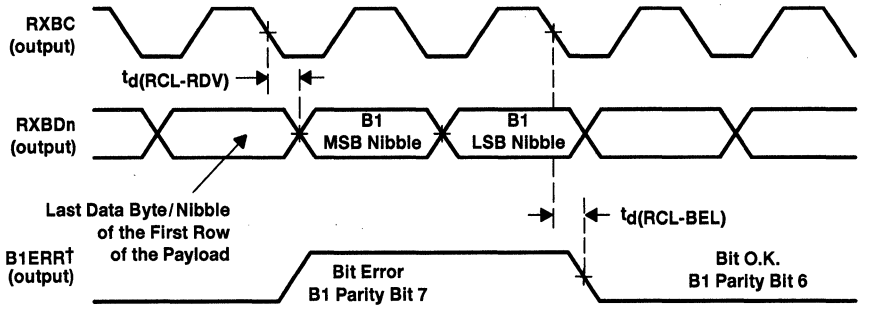
† Four time slots of B1ERR are shown; up to eight bits can be in error in a given frame.

Figure 15. B1 Error-Pulse Timing – Byte Mode

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 16)

		MIN	MAX	UNIT
$t_{d(RCL-RDV)}$	Delay time after RXBC↓ to RXBD valid	0	6	ns
$t_{d(RCL-BEL)}$	Delay time after RXBC↓ to B1ERR↓	0	6	ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.



† Four time slots of B1ERR are shown; up to eight bits can be in error in a given frame.

Figure 16. B1 Error-Pulse Timing – Nibble Mode

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 17)

		MIN	TYP	MAX	UNIT
$t_{d(RSH-RFH)}$	Delay time after $\overline{RESET}\uparrow$ to RXRF↑	51.44		130	ns
$t_{w(RXRF)}$	Pulse duration, RXRF		51.44		ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

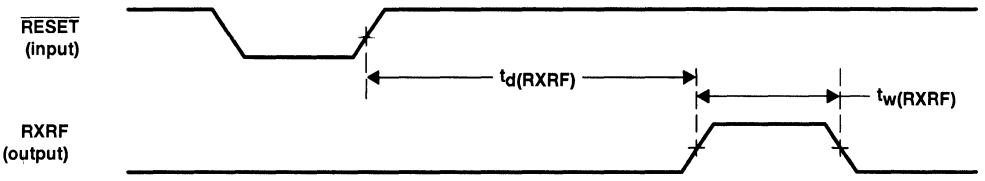


Figure 17. $\overline{RESET}$ Receive Reference

timing requirements, C_L = 25 pF (see Notes 3 and 4 and Figure 18)

		MIN	NOM	MAX	UNIT
$t_{c(HSCK)}$	Clock cycle time, HSCK		6.43		ns
$t_{w(HSCKH)}$	Pulse duration, HSCK high	2.9			ns
$t_{w(HSCKL)}$	Pulse duration, HSCK low	2.9			ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

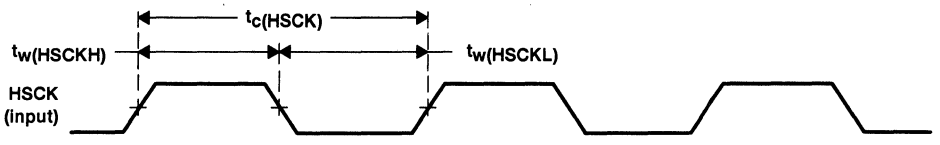
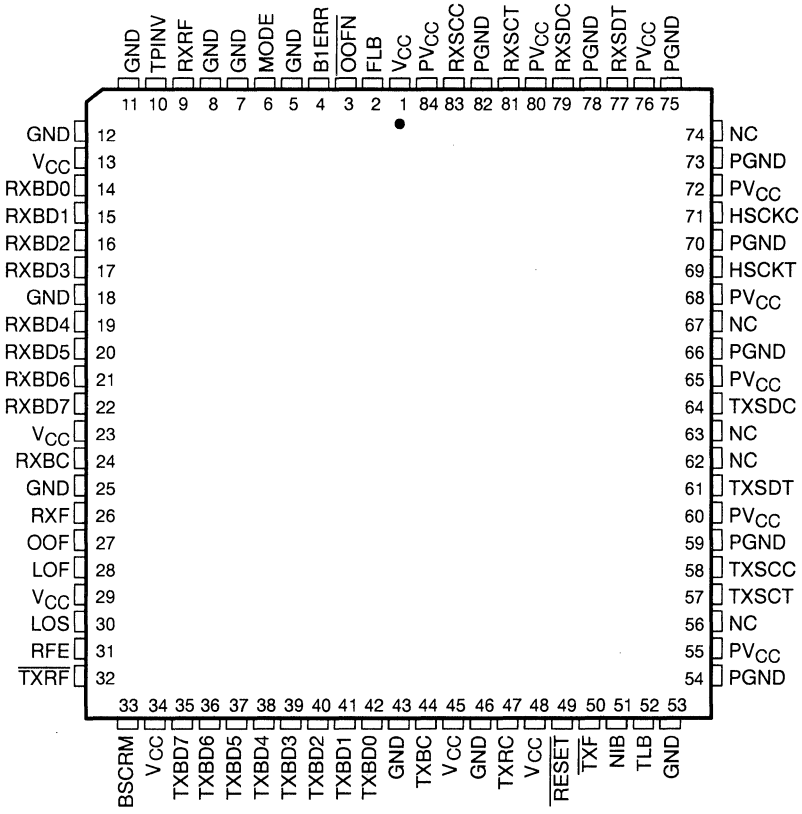


Figure 18. HSCK Input

SDNS020B – SEPTEMBER 1992 – REVISED DECEMBER 1994

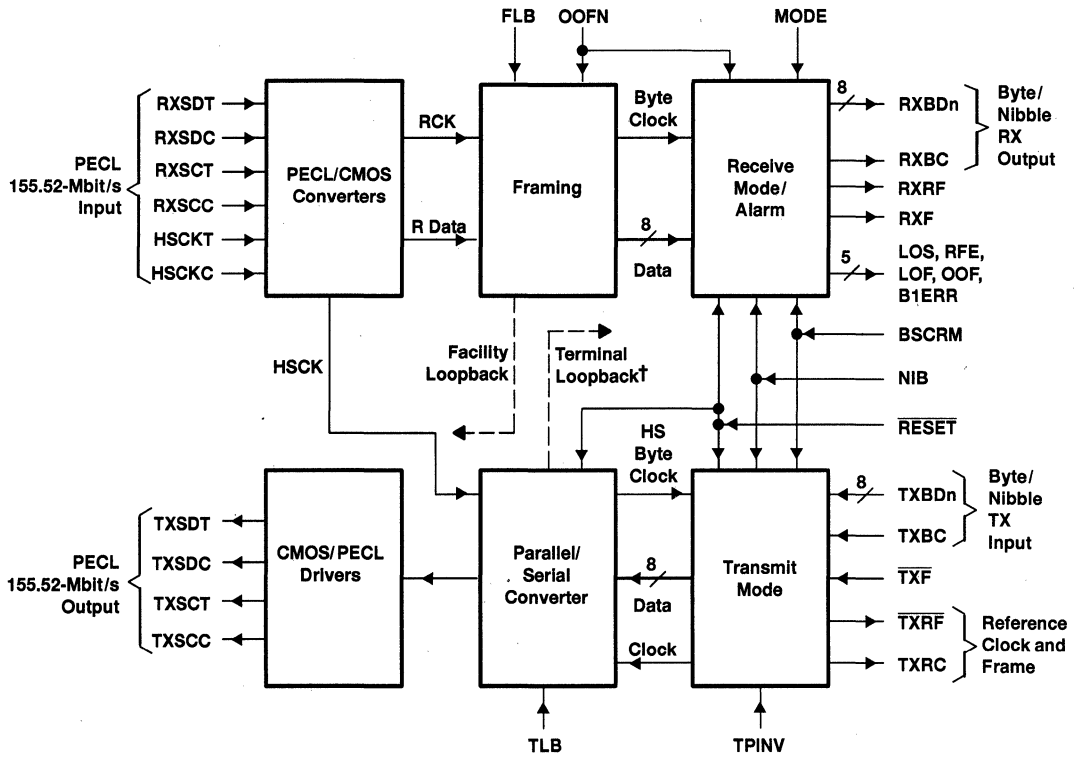
- Member of the Texas Instruments Digital Communication Series of Standard DS-3 and SONET Devices
- Transmits and Receives at the STS-3/STM-1 Rate of 155.52 Mbit/s
- Converts 155.52-Mbit/s Data and Clock to Byte/Nibble Data and Clock and Vice Versa
- Provides Pseudo-ECL (PECL) Levels for 155.52-Mbit/s Data and Clock
- Detects the Frame of the Incoming Signal and Transmits a Frame-Indication Signal
- Provides User-Selectable Options for:
  - Signal Scrambling/Descrambling
  - B1 Parity Calculation
- Provides Loss-of-Signal (LOS), Loss-of-Frame (LOF), and Receive Frame Error (RFE) Flags for 155.52-Mbit/s Data
- Packaged in 84-Pin Plastic Leaded Chip Carrier (PLCC) Using 50-mil Center-to-Center Spacings

FN PACKAGE
(TOP VIEW)



NC – No internal connection

functional block diagram



† Dashed lines are used for loopback signals.

description

The TNETS2302C provides a complete frame-synchronization function for a STS-3/STM-1 line interface. The device frame aligns the incoming 155.52-Mbit/s serial-data stream and converts it to a byte or nibble data output. A byte or nibble clock output is also provided along with a frame-indication signal. In the transmit direction, the TNETS2302C accepts byte or nibble data and clock and outputs a 155.52-Mbit/s serial-data stream. The device can be programmed to provide signal descrambling/scrambling and B1 byte parity checking/generation. The TNETS2302C also monitors the incoming serial data and provides a loss-of-signal (LOS) indicator. In addition, loopback of both the facility serial line input and the terminal byte/nibble input is provided.

The TNETS2302C provides two modes of frame synchronization: tracking or nontracking. When the tracking mode is activated, the device finds the frame of the incoming signal and monitors the signal continuously for frame-alignment errors. In this operating mode, outputs are provided to indicate a receive frame error (RFE), out-of-frame error (OOF), or loss-of-frame error (LOF). If the nontracking mode is activated, the device finds the frame of the incoming signal but no subsequent monitoring of the signal is provided. In this mode, the RFE, OOF, and LOF outputs are deactivated.

The serial data and clock inputs and outputs operate at PECL levels (ECL levels referenced to 5 V instead of 0 V). Of the remaining I/O signals, the inputs are TTL compatible and the outputs are CMOS. The TNETS2302C is specified for operation over a temperature range of –40°C to 85°C.

serial data input to byte/nibble output

The serial inputs to the TNETS2302C consist of a 155.52-Mbit/s data stream and a corresponding 155.52-MHz clock signal from an optical-to-electrical converter, clock-recovery circuit, or similar function. Both the serial data and clock inputs operate at differential PECL levels. The serial data is clocked into the device on a positive transition of the clock signal. A serial search for the framing bytes (A1, A2) is performed on the incoming data in accordance with the selected frame-synchronization mode. If the tracking mode is selected (MODE = low), the device continues to monitor the incoming data stream after the frame has been established and the LOF, OOF, and RFE indicators are enabled. If the nontracking mode is selected (MODE = high), the incoming data is not monitored after the frame has been found and the LOF, OOF, and RFE indicators are disabled.

If the tracking mode is selected and an out-of-frame (OOF) condition exists, the TNETS2302C initiates a search for the framing pattern. The framing pattern is defined in ANSI standards and CCITT recommendations as six bytes (F6, F6, F6, 28, 28, 28) for an STS-3/STM-1 signal. These bytes occupy the A1 and A2 byte positions in the SONET/SDH frame. Once the frame has been found, the serial data is converted to parallel data and output in either nibble or byte format depending on the state of the nibble (NIB) input. If NIB is high, the data is output in nibble format along with a 38.88-MHz clock. If NIB is low, the data is output in byte format along with a 19.44-MHz clock. The device also provides a framing pulse output (RXF) that goes high when the third A2 byte appears on the data output.

When tracking mode is selected, the RFE, LOF, and OOF indicators are enabled. RFE is synchronous with the third A2 byte and becomes active high when a framing bit error is detected. The signal is active for one clock cycle when byte format is selected and two clock cycles when nibble format is selected. If four consecutive frames have framing errors, OOF goes high. This output remains high for at least two frames. If OOF remains high for 24 frames, LOF goes high. This output remains high until eight consecutive error-free frames are received. When an out-of-frame condition occurs (OOF goes high), the device begins a new search for the framing pattern. The device also begins a new search for the framing pattern if $\overline{\text{OOFN}}$ is taken low for two RXBC clock cycles.

The TNETS2302C provides signal scrambling/descrambling and B1 parity checking/generation if the tracking mode is selected. When BSCRM is high, signal scrambling/descrambling and B1 parity checking/generation are both enabled and all the bytes after the third C1 byte are scrambled. The B1 parity errors are indicated with B1ERR. A positive output pulse is sent out for each bit of the B1 byte in error. The pulses are clocked out with the RXBC receive clock, and each pulse is one-byte clock period long. There can be up to eight pulses on the B1ERR lead in a given frame. The ordering of the bit-error pulses is from bit 7 to bit 0. For example, if the pulses out of B1ERR form the sequence 01000100, errors are detected in bit 6 and bit 2 of the B1 byte.

The data and clock outputs of the TNETS2302C can be selected to follow either a nibble or byte format when the tracking mode is enabled. If the nibble mode is selected (NIB is high), the clock output frequency is 38.88 MHz and the data byte is output as two nibbles on RXBD3–RXBD0. The most significant nibble is transmitted first with the most significant bit of the data byte output on RXBD3. The least significant bit of the data byte is transmitted on RXBD0 of the second nibble. If the byte mode is selected (NIB is low), the clock output frequency is 19.44 MHz and the most significant bit is output on RXBD7.

When the nontracking mode is selected, the TNETS2302C begins a search for the framing pattern when $\overline{\text{OOFN}}$ is taken low for two RXBC clock periods. The RXBDn output data is set to zero on the rising edge of $\overline{\text{OOFN}}$. Valid data is transmitted after the framing pattern is detected. The RFE, OOF, and LOF alarm indicators are disabled when the nontracking mode is selected. In addition, the scrambler/descrambler is disabled, and the data can be output only in byte format.

The serial input data can be looped to the serial data output (facility loopback) independent of whether tracking mode or nontracking mode is selected. To implement a facility loopback, the facility loopback (FLB) input is taken high. The received data is passed to the terminal side and looped back to the serial output. The terminal transmit data is blocked by the looped signal and ignored.

byte/nibble data input to serial data output

Nibble or byte data is clocked into the TNETS2302C on negative transitions of the data input clock (TXBC). If nibble mode is selected, the data is input using the TXBD3–TXBD0 inputs with TXBD3 being the most significant bit. If byte mode is selected, the data is input using the TXBD7– TXBD0 inputs with TXBD7 being the most significant bit. For a given byte, the most significant bit is transmitted first on the serial data output. If the scrambling and B1 parity generation functions are to be performed by the SYNC155, a framing pulse ($\overline{\text{TXF}}$) identifying the location of the third A2 byte in the incoming data is required. To facilitate the generation of TXBC and $\overline{\text{TXF}}$, the TNETS2302C provides a reference byte or nibble clock (TXRC) and a reference frame ($\overline{\text{TXRF}}$) output that are generated from the 155.52-MHz clock inputs (HSCKT and HSCKC). $\overline{\text{TXRF}}$ is active low, has a nominal width of 51.44 ns, and occurs at the frame rate of 8 kHz. TXRC occurs at a rate of 19.44 MHz or 38.88 MHz depending upon the state of the NIB input.

The byte/nibble input data is looped back to the byte/nibble output data if the terminal loopback (TLB) input is high. When TLB is selected, the byte/nibble input data is passed to the line-side serial data output and looped back to the terminal-side output. The received line data is blocked by the looped signal and ignored. The byte/nibble input data is scrambled and the B1 parity byte is generated if the BSCRM input is high. If the BSCRM input is low, these functions are bypassed. The byte/nibble input data is converted to serial format and output via the serial output clock, TXSC.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BSCRM	33	I (TTL)	B1 generation/checking and scramble/descramble. When BSCRM is high, the TNETS2302C provides B1 checking and descrambling of the receive incoming data and B1 generation and scrambling of the transmit output data. To generate B1 errors for test purposes, the value for B1 calculated for the transmit frame is exclusive ORed with the value of B1 received on the transmit terminal-side input. To ensure that the correct value for B1 is transmitted for normal operation, the value for B1 received on the transmit terminal-side input must be 00 (hex). To disable B1 generation/checking and scrambling/descrambling by this device, BSCRM is taken low.
B1ERR	4	O (CMOS)	B1 parity-error indication. A positive-pulse error indication is provided for each B1 bit parity error, up to a maximum of eight error indications. Each error indication is one clock-cycle wide in the byte mode and two clock-cycles wide in the nibble mode.
FLB	2	I (TTL)	Facility loopback. When FLB is high, the serial input data is looped backed to the serial output. The received serial data is also passed to the terminal-side output. The facility and terminal loopbacks cannot be used at the same time. This produces erroneous results.
GND	5, 7, 8, 11, 12, 18, 25, 43, 46, 53		Ground (0-V reference)
HSCKC	71	I (PECL)	High-speed clock complement. HSCKC is used with HSCKT to provide a differential input clock.
HSCKT	69	I (PECL)	High-speed clock true. HSCKT is used in conjunction with HSCKC to provide the 155.52-MHz reference and transmit clock.
LOF	28	O (CMOS)	Loss of frame. LOF goes high when an out-of-frame (OOF) condition persists for three milliseconds (24 frames) or longer. LOF goes low when eight error-free framing patterns are detected after the OOF state is exited. This indication is valid only when MODE is low (tracking mode).
LOS	30	O (TTL)	Loss of signal. LOS goes high when the incoming receive data signal stays high or low for 100 µs (or greater) or if the incoming receive clock stays high or low for one microsecond ±750 ns. LOS goes low when two consecutive error-free framing patterns are detected and a loss of the second condition is not detected between the framing patterns.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
MODE	6	I (TTL)	MODE selects either the tracking or the nontracking mode of operation for the receive side. When MODE is low, the device operates in the tracking mode. In this mode of operation, the device searches for and tracks frame alignment. The framing pulse output RXF is held low when out of frame occurs while byte or nibble data is provided. When MODE is high, the device enters the nontracking mode and frame alignment is declared valid on the first indication of the framing pattern (not the second). If external circuitry finds that an invalid framing pattern has occurred, MODE sends a low signal to $\overline{\text{OOFN}}$ to reinitiate the frame search.
NC	56, 62, 63, 67, 74		No connection
NIB	51	I (TTL)	Nibble/byte control. If NIB is high, the terminal interface is nibble wide; if NIB is low, the terminal interface is byte wide.
OOF	27	O (CMOS)	Out of frame. OOF goes high when errors are detected in the three A2 bytes of four consecutive framing patterns (when A2A2A2 $\neq$ 282828 while in frame alignment). OOF goes low when two error-free consecutive framing patterns are detected (when A1A1A1A2A2A2 = F6F6F6282828). This indication is valid only when MODE is low (tracking mode).
$\overline{\text{OOFN}}$	3	I (CMOS)	Out-of-frame negative. A low-level signal on $\overline{\text{OOFN}}$ for two RXBC clock periods starts a new frame search. $\overline{\text{RESET}}$ and $\overline{\text{OOFN}}$ should be applied after a mode change occurs. $\overline{\text{OOFN}}$ must occur either at the same time as the $\overline{\text{RESET}}$ or after the $\overline{\text{RESET}}$ becomes inactive.
PGND	54, 59, 66, 70, 73, 75, 78, 82		PECL ground (0-V reference)
PV_{CC}	55, 60, 65, 68, 72, 76, 80, 84		PECL supply voltage, 5 V ± 5%
$\overline{\text{RESET}}$	49	I (CMOS)	The device is reset when $\overline{\text{RESET}}$ is held low for a minimum of 105 ns. The device should be reset after power is applied or the state of BSCRM, MODE, or NIB is changed.
RFE	31	O (CMOS)	Receive framing error. RFE goes high when any bit in the receive-framing pattern is in error and the device is not in an out-of-frame state. When present, the indication occurs at the start of the third A2 framing byte in the framing pattern in the receive-side data. This indication is valid only when MODE is low (tracking mode).
RXBC	24	O (CMOS)	Receive clock. RXBC outputs the data from the TNETS2302C on the falling edge of this signal. The clock frequency is either 19.44 MHz (byte clock) or 38.88 MHz (nibble clock).
RXBD7–RXBD0	22–19, 17–14	O (CMOS)	Receive data. TXBD7–RXBD0 is the terminal-side output data, either byte or nibble wide that depends on the state of NIB. Receive data is still provided when OOF occurs.
RXF	26	O (CMOS)	Receive frame. RXF provides a positive pulse in synchronization with the third A2 byte of the SONET/SDH frame. When OOF occurs, RXF is held low.
RXRF	9	O (TTL)	Receive reference frame. RXRF is an 8-kHz output derived from the differential input serial clock RXSC. RXRF is one clock-cycle wide.
RXSCC	83	I (PECL)	Receive serial clock complement. RXSCC is used with RXSCT to provide a differential clock input.
RXSCT	81	I (PECL)	Receive serial clock true. RXSCT is used with RXSCC to provide a differential clock input that accompanies the serial data input.
RXSDC	79	I (PECL)	Receive serial data input complement. RXSDC is used with RXSDT to provide a differential data input.
RXSDT	77	I (PECL)	Receive serial data input true. RXSDT is used with RXSDC to provide a differential data input.
TLB	52	I (TTL)	Terminal loopback. When TLB is high, the transmit terminal input is looped back to the receive terminal output. The transmit terminal input data is also sent to the transmit serial output. The facility and terminal loopbacks cannot be activated at the same time. This produces erroneous results.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TPINV	10	I (TTL)	Transmit path invert. When TPINV is low, $\overline{\text{TXRF}}$ is active low and clocked out on the rising edge of TXRC. In addition, $\overline{\text{TXF}}$ is active low and clocked into the TNETS2302C, along with TXBDn, on the falling edge of TXBC. When TPINV is high, $\overline{\text{TXRF}}$ becomes an active-high output that is clocked out on the falling edge of TXRC. Also, $\overline{\text{TXF}}$ becomes an active-high input that is clocked into the TNETS2302C, along with TXBDn, on the rising edge of TXBC.
TXBC	44	I (CMOS)	Transmit byte/nibble clock. The clock rate is either 19.44 MHz (byte data) or 38.88 MHz (nibble data). The data on TXBDn is clocked into the TNETS2302C on the falling edge of TXBC when TPINV is low and on the rising edge when TPINV is high.
TXBD7–TXBD0	35–42	I (CMOS)	Transmit data. TXBD7 – TXBD0 is the terminal-side input data (either byte or nibble wide). TXBD7 is the most significant bit for byte-wide input. TXBD3 is the most significant bit for nibble-wide input.
$\overline{\text{TXF}}$	50	I (CMOS)	Transmit frame. $\overline{\text{TXF}}$ is synchronous with the third A2 byte of the terminal-side input and is required to perform signal scrambling. $\overline{\text{TXF}}$ is active low when TPINV is low and active high when TPINV is high.
TXRC	47	O (CMOS)	Transmit reference clock. TXRC is a clock occurring at the rate of 19.44 MHz or 38.88 MHz depending on the state of NIB. $\overline{\text{TXRF}}$ is clocked out on the positive transition of TXRC when TPINV is low and on the negative transition of TXRC when TPINV is high.
$\overline{\text{TXRF}}$	32	O (CMOS)	Transmit reference frame. $\overline{\text{TXRF}}$ is a one-byte clock-wide pulse occurring at the frame rate of 8 kHz. $\overline{\text{TXRF}}$ is active low when TPIN is low and active high when TPINV is high.
TXSCC	58	O (PECL)	Transmit serial clock output complement. TXSCC has an inverted PECL clock output.
TXSCT	57	O (PECL)	Transmit serial clock output true. TXSCT has a noninverted PECL clock output.
TXSDC	64	O (PECL)	Transmit serial data output complement. TXSDC has an inverted PECL data output.
TXSDT	61	O (PECL)	Transmit serial data output true. TXSDT has a noninverted PECL data output.
V_{CC}	1, 13, 23, 29, 34, 45 48		Supply voltage, 5 V ± 5%

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Supply voltage range, PV_{CC}, PECL ..... −0.5 V to 7 V
Input voltage range: TTL ..... 0 V to PV_{CC}
PECL ..... −1.2 V to 7 V
Input/output clamp current range ..... −50 mA to 50 mA
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

recommended operating conditions

				MIN	MAX	UNIT
V_{CC}	Supply voltage			4.75	5.25	V
PV_{CC}	Supply voltage, PECL			4.75	5.25	V
V_{IH}	High-level input voltage	TTL		2		V
		CMOS	V_{CC} = 4.75 V	3.32		
			V_{CC} = 5.25 V	3.67		
		PECL (see Note 2)		3.8		
V_{IL}	Low-level input voltage	TTL			0.8	V
		CMOS	V_{CC} = 4.75 V		1.42	
			V_{CC} = 5.25 V		1.57	
		PECL (see Note 2)			3.4	
T_A	Operating free-air temperature			−40	85	°C

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage, TTL		V_{CC} = 4.75 V,	I_{IK} = −18 mA			−1.2	V
V_{OH}	High-level output voltage	CMOS	V_{CC} = 4.75 V,	I_{OH} = −4 mA	4.25			V
		TTL	V_{CC} = 4.75 V,	I_{OH} = −2 mA	4.25			
		PECL	PV_{CC} = 5 V,	I_{OH} = −22.4 mA	4		4.3	
V_{OL}	Low-level output voltage	CMOS	V_{CC} = 4.75 V,	I_{OL} = 4 mA			0.5	V
		TTL	V_{CC} = 4.75 V,	I_{OL} = 4 mA			0.5	
		PECL	PV_{CC} = 5 V,	I_{OL} = 7.6 mA	3		3.4	
I_I	Input current, TTL/CMOS		V_{CC} = 5.25 V,	V_I = V_{CC} or GND			±1	µA
I_{IH}	High-level input current, PECL		V_{CC} = 5.25 V,	V_I = 4.45 V			25	µA
I_{IL}	Low-level input current, PECL		V_{CC} = 5.25 V,	V_I = 3.35 V			25	µA
I_{CC1}	Supply current‡		V_{CC} = 5.25 V, f = 155.52 Mbit/s	I_O = 0,			100	mA
I_{CC2}	Supply current§		V_{CC} = 5.25 V,	f = 155.52 Mbit/s			175	mA
C_i	Input capacitance, TTL					4		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ PECL outputs are unterminated.
§ PECL outputs are terminated with a 50-Ω resistor to 3 V.

timing requirements, C_L = 25 pF (see Notes 3 and 4 and Figure 1)

		MIN	NOM	MAX	UNIT
$t_{w(RXSCH)}$	Pulse duration, RXSC high	2.9			ns
$t_{w(RXSCL)}$	Pulse duration, RXSC low	2.9			ns
$t_{c(RXSC)}$	Clock cycle time, RXSC		6.43		ns
$t_{su(RXSD)}$	Setup time, RXSD before RXSC↑	2			ns
$t_{h(RXSD)}$	Hold time, RXSD after RXSC↑	1			ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

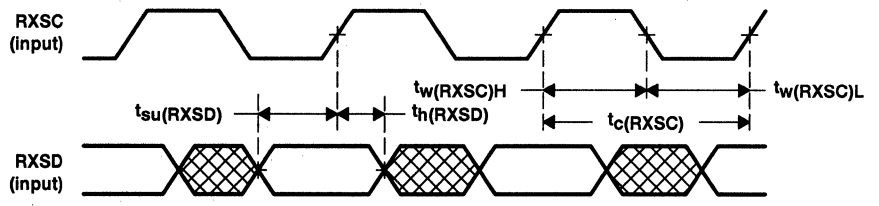


Figure 1. Line-Side Input Clock and Data

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 2)

		MIN	TYP	MAX	UNIT
$t_{w(RXF)}$	Pulse duration, RXF		51.44		ns
$t_{w(RXBCH)}$	Pulse duration, RXBC high	23			ns
$t_{w(RXBCL)}$	Pulse duration, RXBC low	23			ns
$t_{c(RXBC)}$	Clock cycle time, RXBC		51.44		ns
$t_{d(RCL-RDV)}$	Delay time after RXBC↓ to RXBD valid	−1		6	ns
$t_{d(RCL-RFH)}$	Delay time after RXBC↓ to RXF↑	0		6	ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

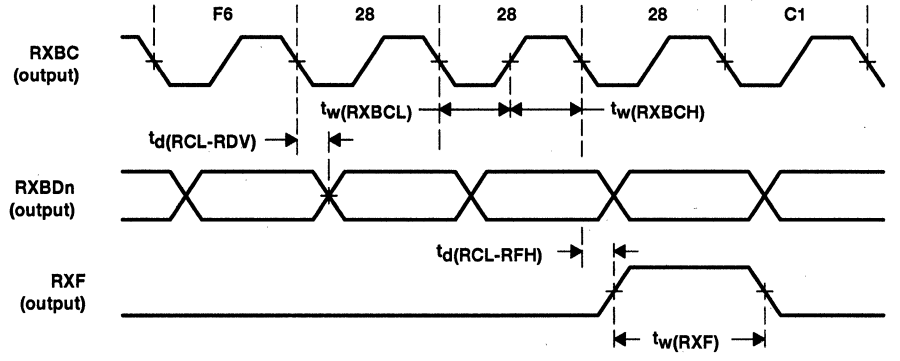


Figure 2. Terminal-Side Byte Output

timing requirements, C_L = 25 pF (see Notes 3 and 4 and Figure 3)

		MIN	NOM	MAX	UNIT
$t_{w(TXBCH)}$	Pulse duration, TXBC high	18			ns
$t_{w(TXBCL)}$	Pulse duration, TXBC low	18			ns
$t_{c(TXBC)}$	Clock cycle time, TXBC		51.44		ns
$t_{su(TXBD)1}$	Setup time before TXBC↓, TXBD	5			ns
$t_{h(TXBD)1}$	Hold time after TXBC↓, TXBD	5			ns
$t_{su(TXF)1}$	Setup time before TXBC↓, $\overline{TXF}$	5			ns
$t_{h(TXF)1}$	Hold time before TXBC↓, $\overline{TXF}$	5			ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

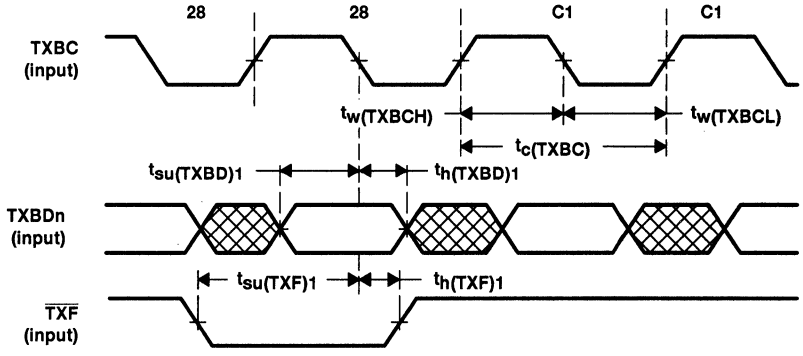


Figure 3. Terminal-Side Byte Input (TPINV low)

timing requirements, C_L = 25 pF (see Notes 3 and 4 and Figure 4)

		MIN	NOM	MAX	UNIT
$t_{w(TXBCH)}$	Pulse duration, TXBC high	18			ns
$t_{w(TXBCL)}$	Pulse duration, TXBC low	18			ns
$t_{c(TXBC)}$	Clock cycle time, TXBC		51.44		ns
$t_{su(TXBD)2}$	Setup time before TXBC↑, TXBD	5			ns
$t_{h(TXBD)2}$	Hold time after TXBC↑, TXBD	5			ns
$t_{su(TXF)2}$	Setup time before TXBC↑, $\overline{TXF}$	5			ns
$t_{h(TXF)2}$	Hold time after TXBC↑, $\overline{TXF}$	5			ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

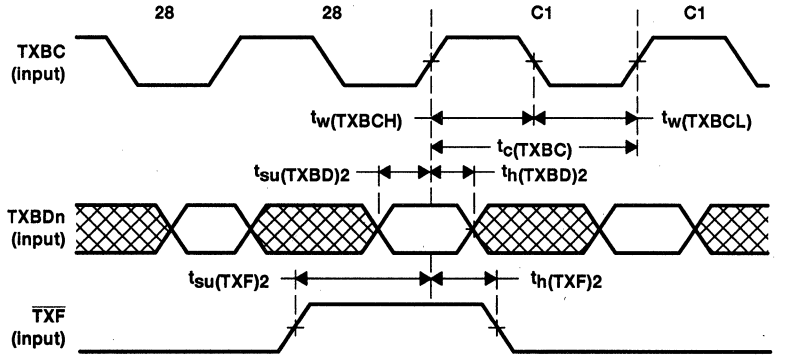


Figure 4. Terminal-Side Byte Input (TPINV high)

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 5)

		MIN	TYP	MAX	UNIT
$t_{w(RXF)}$	Pulse duration, RXF high		51.44		ns
$t_{w(RXBCH)}$	Pulse duration, RXBC high	9			ns
$t_{w(RXBCL)}$	Pulse duration, RXBC low	9			ns
$t_{c(RXBC)}$	Clock cycle time, RXBC		25.72		ns
$t_{d(RCL-RDV)}$	Delay time after RXBC↓ to RXBD valid	−1		6	ns
$t_{d(RCL-RFH)}$	Delay time after RXBC↓ to RXF↑	0		6	ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

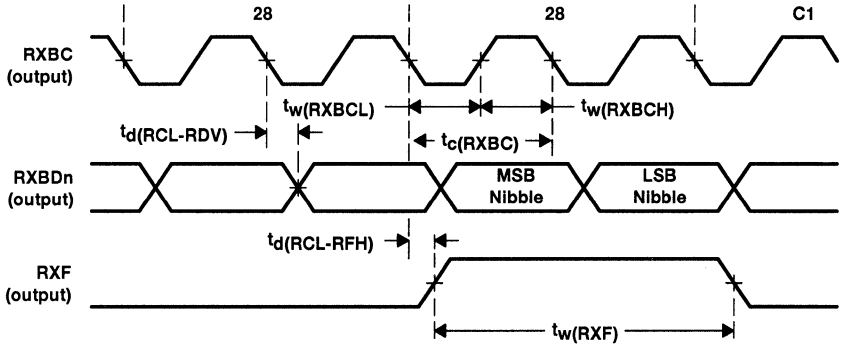


Figure 5. Terminal-Side Nibble Output

timing requirements, C_L = 25 pF (see Notes 3 and 4 and Figure 6)

		MIN	NOM	MAX	UNIT
$t_{w(TXBCH)}$	Pulse duration, TXBC high	9			ns
$t_{w(TXBCL)}$	Pulse duration, TXBC low	9			ns
$t_{c(TXBC)}$	Clock cycle time, TXBC		25.72		ns
$t_{su(TXBD)3}$	Setup time before TXBC↓, TXBD	5			ns
$t_{h(TXBD)3}$	Hold time after TXBC↓, TXBD	5			ns
$t_{su(TXF)3}$	Setup time before TXBC↓, $\overline{TXF}$	5			ns
$t_{h(TXF)3}$	Hold time after TXBC↓, $\overline{TXF}$	5			ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

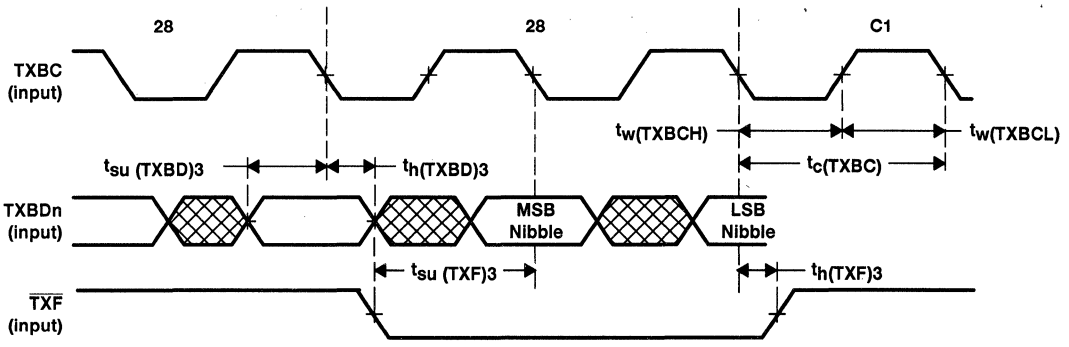


Figure 6. Terminal-Side Nibble Input (TPINV low)

timing requirements, C_L = 25 pF (see Notes 3 and 4 and Figure 7)

		MIN	NOM	MAX	UNIT
$t_{w(TXBCH)}$	Pulse duration, TXBC high	9			ns
$t_{w(TXBCL)}$	Pulse duration, TXBC low	9			ns
$t_{c(TXBC)}$	Clock cycle time, TXBC		25.72		ns
$t_{su(TXBD)4}$	Setup time before TXBC↑, TXBD	5			ns
$t_{h(TXBD)4}$	Hold time after TXBC↑, TXBD	5			ns
$t_{su(TXF)4}$	Setup time before TXBC↑, $\overline{TXF}$	5			ns
$t_{h(TXF)4}$	Hold time before TXBC↑, $\overline{TXF}$	5			ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

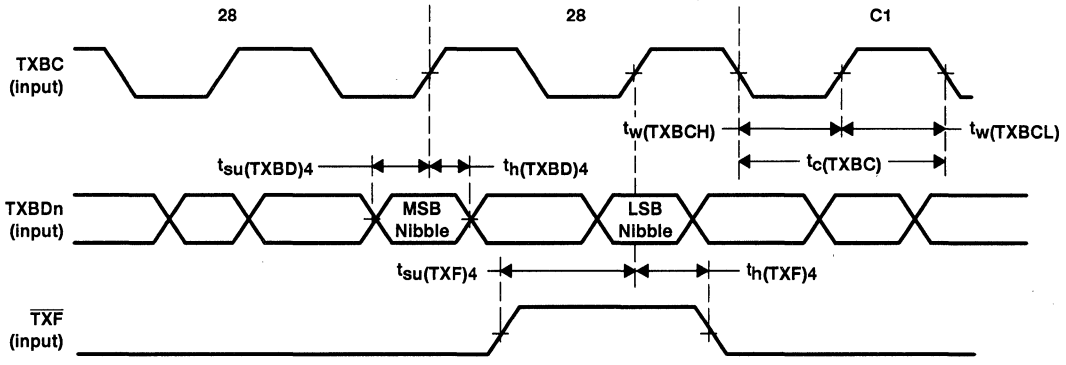


Figure 7. Terminal-Side Nibble Input (TPINV high)

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 8)

		MIN	TYP	MAX	UNIT
$t_{w(TXRFL)}$	Pulse duration, $\overline{TXRF}$ low		51.44		ns
$t_{w(TXRCH)}$	Pulse duration, TXRC high	23			ns
$t_{w(TXRCL)}$	Pulse duration, TXRC low	23			ns
$t_{c(TXRC)}$	Clock cycle time, TXRC		51.44		ns
$t_{d(TCH-TFL)}$	Delay time after TXRC↑ to $\overline{TXRF}$↓	0		6	ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

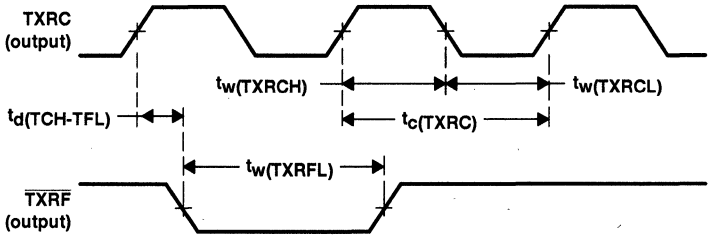


Figure 8. Terminal-Side Byte Reference Signals Output (TPINV low)

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 9)

		MIN	TYP	MAX	UNIT
$t_{w(TXRFH)}$	Pulse duration, $\overline{TXRF}$ high		51.44		ns
$t_{w(TXRCH)}$	Pulse duration, TXRC high	23			ns
$t_{w(TXRCL)}$	Pulse duration, TXRC low	23			ns
$t_{c(TXRC)}$	Clock cycle time, TXRC		51.44		ns
$t_{d(TCH-TPH)}$	Delay time after TXRC↑ to $\overline{TXRF}$↑	0		6	ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

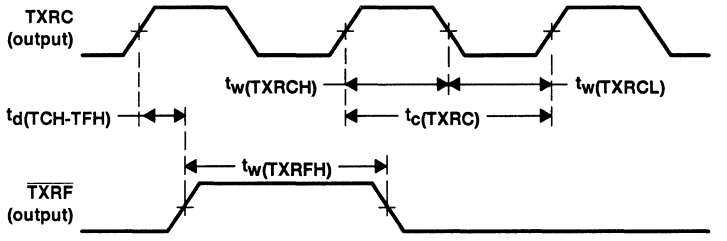


Figure 9. Terminal-Side Byte Reference Signals Output (TPINV high)

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 10)

		MIN	TYP	MAX	UNIT
$t_{w(TXRFL)}$	Pulse duration, $\overline{TXRF}$ low		25.72		ns
$t_{w(TXRCH)}$	Pulse duration, TXRC high	9			ns
$t_{w(TXRCL)}$	Pulse duration, TXRC low	9			ns
$t_{c(TXRC)}$	Clock cycle time, TXRC		25.72		ns
$t_{d(TCH-TFL)}$	Delay time after TXRC↑ to $\overline{TXRF}$↓	0		6	ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

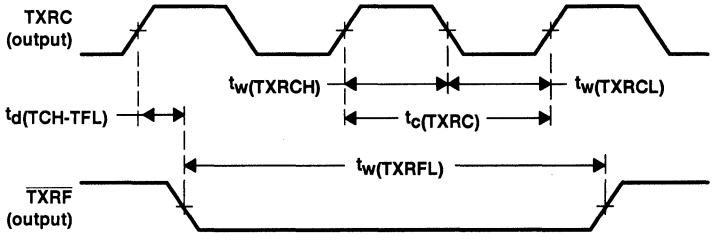


Figure 10. Terminal-Side Nibble Reference Signals Output (TPINV low)

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 11)

		MIN	TYP	MAX	UNIT
$t_{w(TXRFH)}$	Pulse duration, $\overline{TXRF}$ high		25.72		ns
$t_{w(TXRCH)}$	Pulse duration, TXRC high	9			ns
$t_{w(TXRCL)}$	Pulse duration, TXRC low	9			ns
$t_{c(TXRC)}$	Clock cycle time, TXRC		25.72		ns
$t_{d(TCL-TFH)}$	Delay time after TXRC↓ to $\overline{TXRF}$↑	0		6	ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

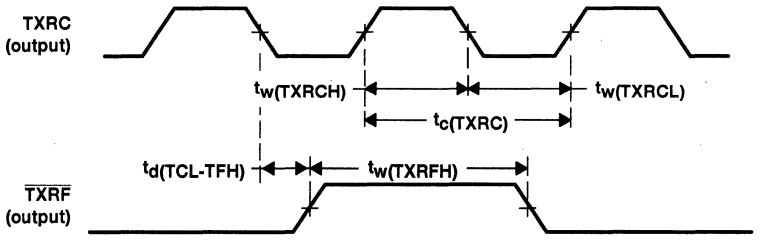


Figure 11. Terminal-Side Nibble Reference Signals Output (TPINV high)

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 12)

		MIN	MAX	UNIT
$t_{d(OFH-OOH)}$	Delay time after $\overline{OOFN}$↑ to OOF↑	0	312	ns
$t_{d(OFH-LOH)}$	Delay time after $\overline{OOFN}$↑ to LOF↑	0	312	ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

timing requirements, C_L = 25 pF (see Notes 3 and 4 and Figure 12)

		MIN	MAX	UNIT
$t_{w(OOFNL)}$	Pulse duration, $\overline{OOFN}$ low	105		ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

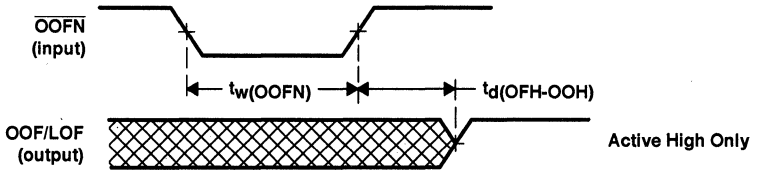


Figure 12. $\overline{OOFN}$ Resetting Frame

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 13)

		MIN	MAX	UNIT
$t_{d(RSH-TCH)}$	Delay time after $\overline{RESET}\uparrow$ to TXRC↑	6	30	ns
$t_{d(TCH-TFL)}$	Delay time after TXRC↑ to $\overline{TXRF}\downarrow$	0	6	ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

timing requirements, C_L = 25 pF (see Notes 3 and 4 and Figure 13)

		MIN	MAX	UNIT
$t_{w(RESETL)}$	Pulse duration, $\overline{RESET}$ low	105		ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

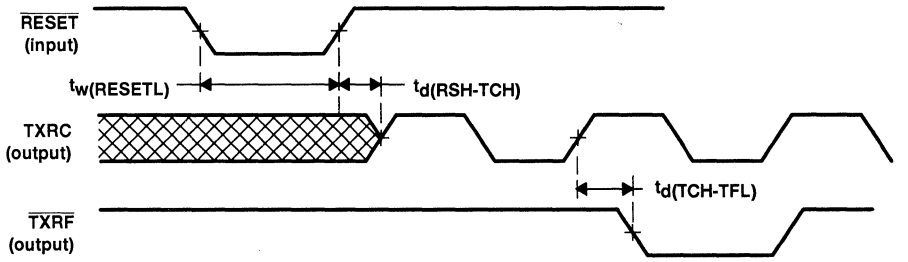


Figure 13. $\overline{RESET}$ Effect of Reference Clock and Frame (TPINV low)

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 14)

		MIN	MAX	UNIT
$t_{d(RSH-TCH)}$	Delay time after $\overline{RESET}\uparrow$ to TXRC↑	6	30	ns
$t_{d(TCH-TFH)}$	Delay time after TXRC↑ to $\overline{TXRF}\uparrow$	0	6	ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

timing requirements, C_L = 25 pF (see Notes 3 and 4 and Figure 14)

		MIN	MAX	UNIT
$t_{w(RESETL)}$	Pulse duration, $\overline{RESET}$ low	105		ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

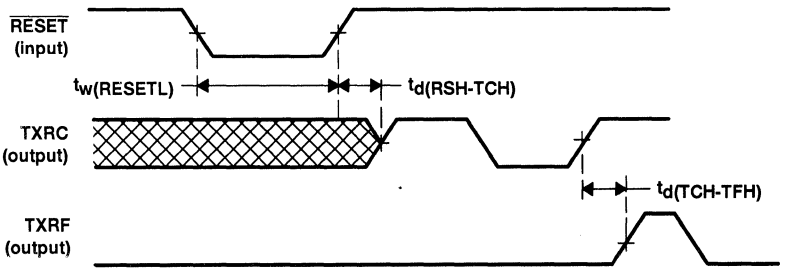
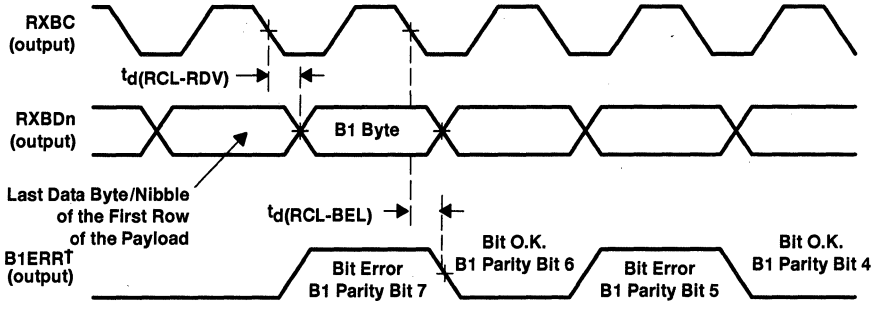


Figure 14. $\overline{RESET}$ Effect of Reference Clock and Frame (TPINV high)

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 15)

		MIN	MAX	UNIT
$t_{d(RCL-RDV)}$	Delay time after RXBC↓ to RXBD valid	0	6	ns
$t_{d(RCL-BEL)}$	Delay time after RXBC↓ to B1ERR↓	0	6	ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.



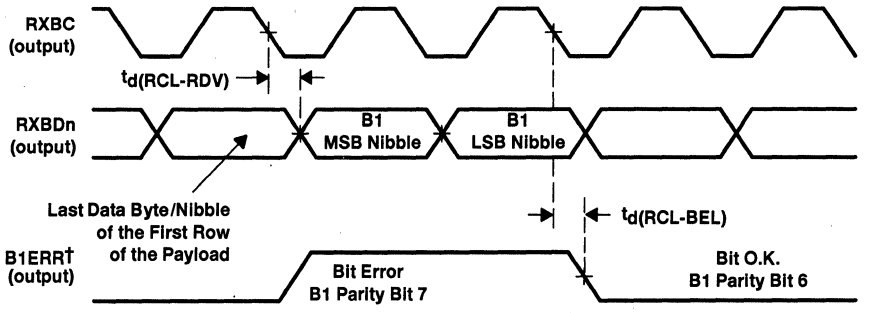
† Four time slots of B1ERR are shown; up to eight bits can be in error in a given frame.

Figure 15. B1 Error-Pulse Timing – Byte Mode

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 16)

		MIN	MAX	UNIT
$t_{d(RCL-RDV)}$	Delay time after RXBC↓ to RXBD valid	0	6	ns
$t_{d(RCL-BEL)}$	Delay time after RXBC↓ to B1ERR↓	0	6	ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.



† Four time slots of B1ERR are shown; up to eight bits can be in error in a given frame.

Figure 16. B1 Error-Pulse Timing – Nibble Mode

timing requirements, C_L = 25 pF (see Notes 3 and 4 and Figure 17)

		MIN	NOM	MAX	UNIT
$t_{w(TXSCL)}$	Pulse duration, TXSC low	2.9			ns
$t_{w(TXSCH)}$	Pulse duration, TXSC high	2.9			ns
$t_{c(TXSC)}$	Clock cycle time, TXSC		6.43		ns
$t_{su(TXSD)}$	Setup time, TXSD before TXSC↑	1			ns
$t_{h(TXSD)}$	Hold time, TXSD after TXSC↑	1.25			ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

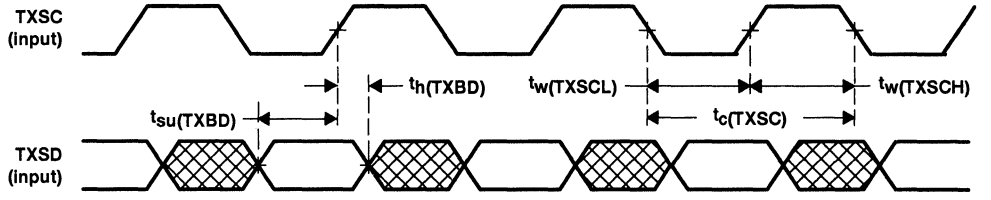


Figure 17. Line-Side PECL Output

operating characteristics, C_L = 25 pF (see Notes 3 and 4 and Figure 18)

		MIN	TYP	MAX	UNIT
$t_{d(RSH-RFH)}$	Delay time after $\overline{RESET}$↑ to RXRF↑	51.44		130	ns
$t_{w(RXRF)}$	Pulse duration, RXRF		51.44		ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

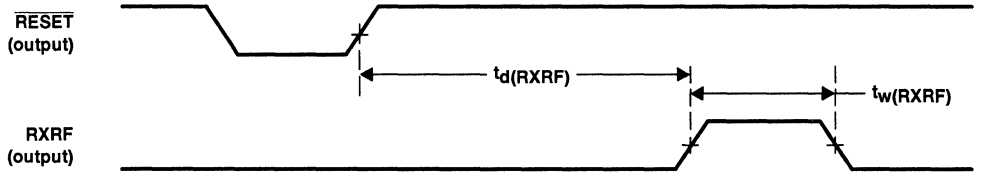


Figure 18. $\overline{RESET}$ Receive Reference

timing requirements, C_L = 25 pF (see Notes 3 and 4 and Figure 19)

		MIN	NOM	MAX	UNIT
$t_{c(HSCK)}$	Clock cycle time, HSCK		6.43		ns
$t_{w(HSCKH)}$	Pulse duration, HSCK high	2.9			ns
$t_{w(HSCKL)}$	Pulse duration, HSCK low	2.9			ns

NOTES: 3. PECL outputs are terminated with a 50-Ω resistor to 3 V.
4. Timing intervals are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

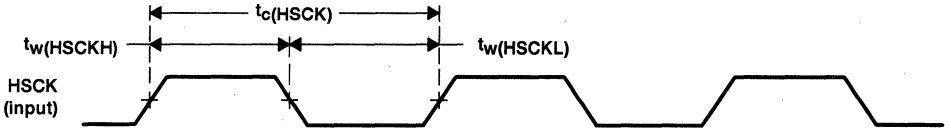


Figure 19. HSCK Input

Contents

ADVANCE INFORMATION

- Single-Chip Ethernet™ Adapter for the Peripheral Component Interconnect (PCI) Local Bus
  - 32-Bit PCI† Glueless Host Interface
  - Compliant With PCI Local-Bus Specification (Revision 2.0)
  - 33-MHz Operation
  - 3-V or 5-V I/O Operation
  - Adaptive Performance Optimization™ (APO) for Highest Available PCI Bandwidth
  - High-Performance Bus Master Architecture With Byte-Aligning DMA Controller for Low Host CPU and Bus Utilization
  - Plug-and-Play Compatible
- Supports 32-Bit Data Streaming on PCI Bus
  - Time Division Multiplexed SRAM
  - 2-Gbps Internal Bandwidth
- Switched Ethernet Compatible
- Full-Duplex Compatible
  - Independent Transmit and Receive Channels
  - Two Transmit Channels for Demand Priority
- Supports Multiple Protocols With a Single Driver Suite
  - Automatic Transmit Padding
  - Optimized Shared Interrupts
- No On-Board Memory Required
- Auto-Negotiation (N-Way) Compatible
- Multimedia-Ready Architecture
- cLAN (Configurable LAN) Technology
- Integrated 10 Base-T and 10 Base-5 (AUI) Physical Layer Interface
  - Single-Chip IEEE 802.3 and Blue Book Ethernet-Compliant Solution
  - DSP-Based Digital Phase-Locked Loop
  - Smart Squelch Allows for Transparent Link Testing
  - Transmission Waveshaping
  - Autopolarity (Reverse Polarity Correction)
  - External/Internal Loopback Including Twisted Pair and AUI
- Media Independent Interface (MII) for Connecting 100-Mbps External Transceivers
  - Compliant MII for IEEE 802.3u Transceivers
  - Super Set Supports IEEE 802.12 Transceivers
  - Supports Ethernet and Token-Ring Framing Formats for 100VG-AnyLAN
  - Link Pulse Detection for Determining Wire Rate
- Low-Power CMOS Technology
  - Green PC Compatible
  - Microsoft™ Advanced Power Management
- EEPROM Interface Supports Jumperless Design and Autoconfiguration
- Hardware Statistics Registers for Management Information Base (MIB)
- DMTF (Desktop Management Task Force) Compatible
- IEEE Standard 1149.1‡ Test Access Port (JTAG)
- 144-Pin Quad Flat Package

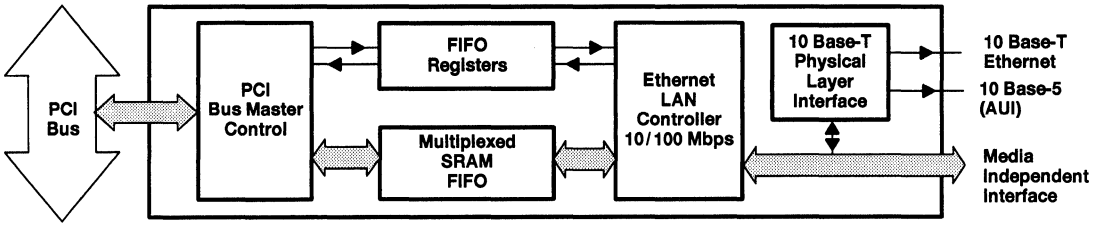


Figure 1. ThunderLAN Architecture

† The PCI Local-Bus Specification, Revision 2.0 should be used as a reference with this document.
‡ IEEE Standard 1149.1–1990, IEEE Standard Test-Access Port and Boundary-Scan Architecture
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Ethernet is a trademark of Xerox Corporation.
Microsoft is a trademark of Microsoft Corporation.

description

ThunderLAN is a high-speed networking architecture that provides a complete PCI-to-10 Base-T/AUI Ethernet solution with the flexibility to handle 100-Mbps Ethernet protocols as the user's networking demands grow.

The TNETE100, one implementation of the ThunderLAN architecture, is an intelligent protocol network interface. The ThunderLAN SRAM FIFO-based architecture eliminates the need for external memory and offers a single-chip glueless PCI-to-10 Base-T/AUI (IEEE 802.3) solution with an on-board physical layer interface. Modular support for 100 Base-T (IEEE 802.3u), and 100VG-AnyLAN (IEEE 802.12) is provided via a superset of the industry-standard Media Independent Interface (MII). ThunderLAN uses a single driver suite to support multiple networking protocols.

The glueless PCI interface supports 32-bit streaming, operates at speeds up to 33 MHz and is capable of internal data transfer rates up to 2 Gbps, taking full advantage of all available PCI bandwidth. The TNETE100 offers jumperless autoconfiguration using PCI configuration read/write cycles. Customizable configuration registers, which can be autoloaded from an external serial EEPROM, allow designers of TNETE100-based systems to give their systems a unique identification code. The TNETE100 PCI interface, developed in conjunction with other leaders in the semiconductor and computer industries, has been vigorously tested on multiple platforms to ensure compatibility across a wide array of available PCI products. In addition, the ThunderLAN drivers and ThunderLAN architecture use TI's patented Adaptive Performance Optimization (APO) technology to dynamically adjust critical parameters for minimum latency, minimum host CPU utilization, and maximum system performance. This technology ensures that the maximum capabilities of the PCI interface are used by automatically tuning the adapter to the specific system in which it is operating.

The Media Independent Interface (MII), an industry-standard interface for connecting a variety of external IEEE 802.3u physical layer interfaces, is fully supported by the TNETE100. In addition, the TNETE100 features an IEEE 802.12-compliant superset of the MII to allow for support of 100VG-AnyLAN physical layer interfaces. This allows TNETE100-based systems to support 100 Base-TX, 100 Base-T4, and 100VG-AnyLAN cabling schemes for maximum flexibility as each new physical layer interface becomes available in the marketplace.

An intelligent protocol handler (PH) implements the serial protocols of the network. The PH is designed for minimum overhead related to multiple protocols, using common state machines to implement 95% of the total protocol handler. On transmit, the PH serializes data, adds framing and cyclic redundancy check (CRC) fields, and interfaces to the network physical layer (PHY) chip. On receive, it provides address recognition, CRC and error checking, frame disassembly, and deserialization. Data for multiple channels is passed to and from the PH by way of circular buffer FIFOs in the FIFO SRAM.

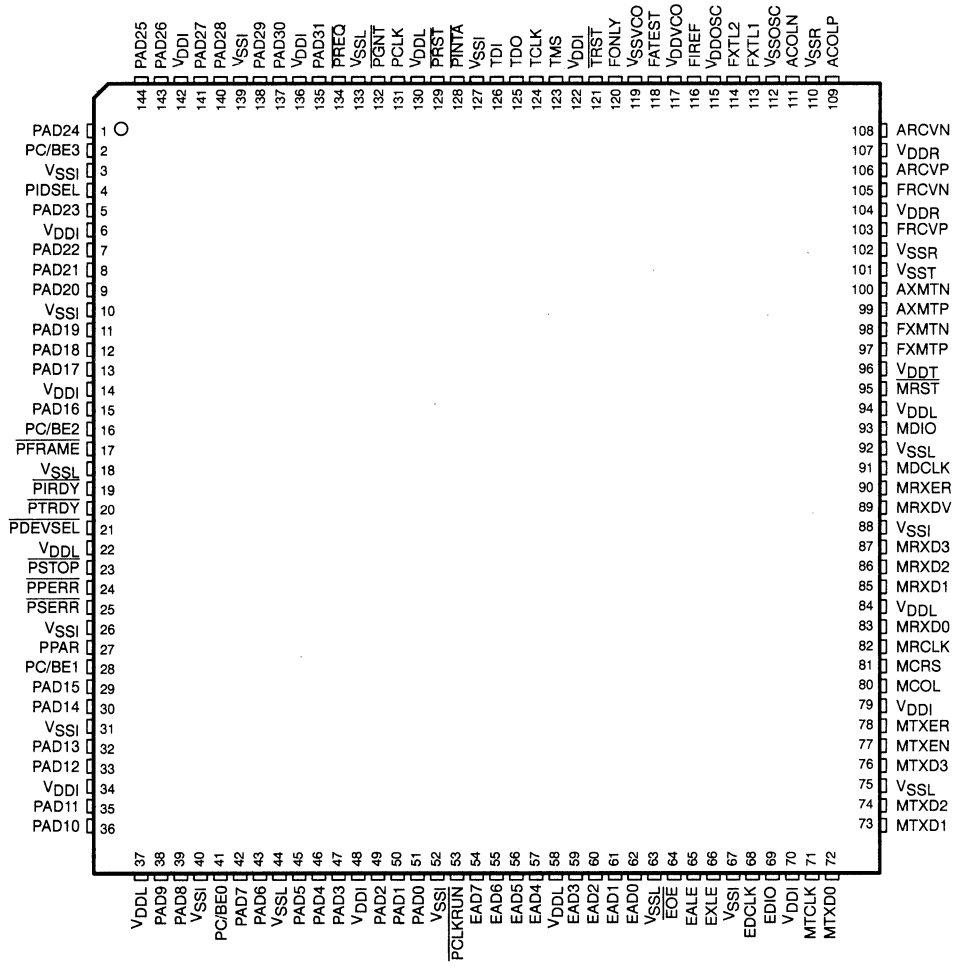
ThunderLAN is the first multimedia-ready architecture and is capable of prioritized data regardless of the selected protocol. The demand priority protocol supports two priorities of frames, *normal* and *priority.* The two transmit channels provide independent host channels for these two frame types. Carrier-sense multiple access with collision detection (CSMA/CD) protocols only support a single priority of frame, but the two channels can be used to prioritize network access. All received frames pass through the single receive channel.

Compliant with IEEE Standard 1149.1 (JTAG), the TNETE100 provides a 5-pin test-access port that is used for boundary-scan testing.

The TNETE100 is available in a 144-pin quad flat package.

pin assignments

PCE PACKAGE
(TOP VIEW)



ADVANCE INFORMATION

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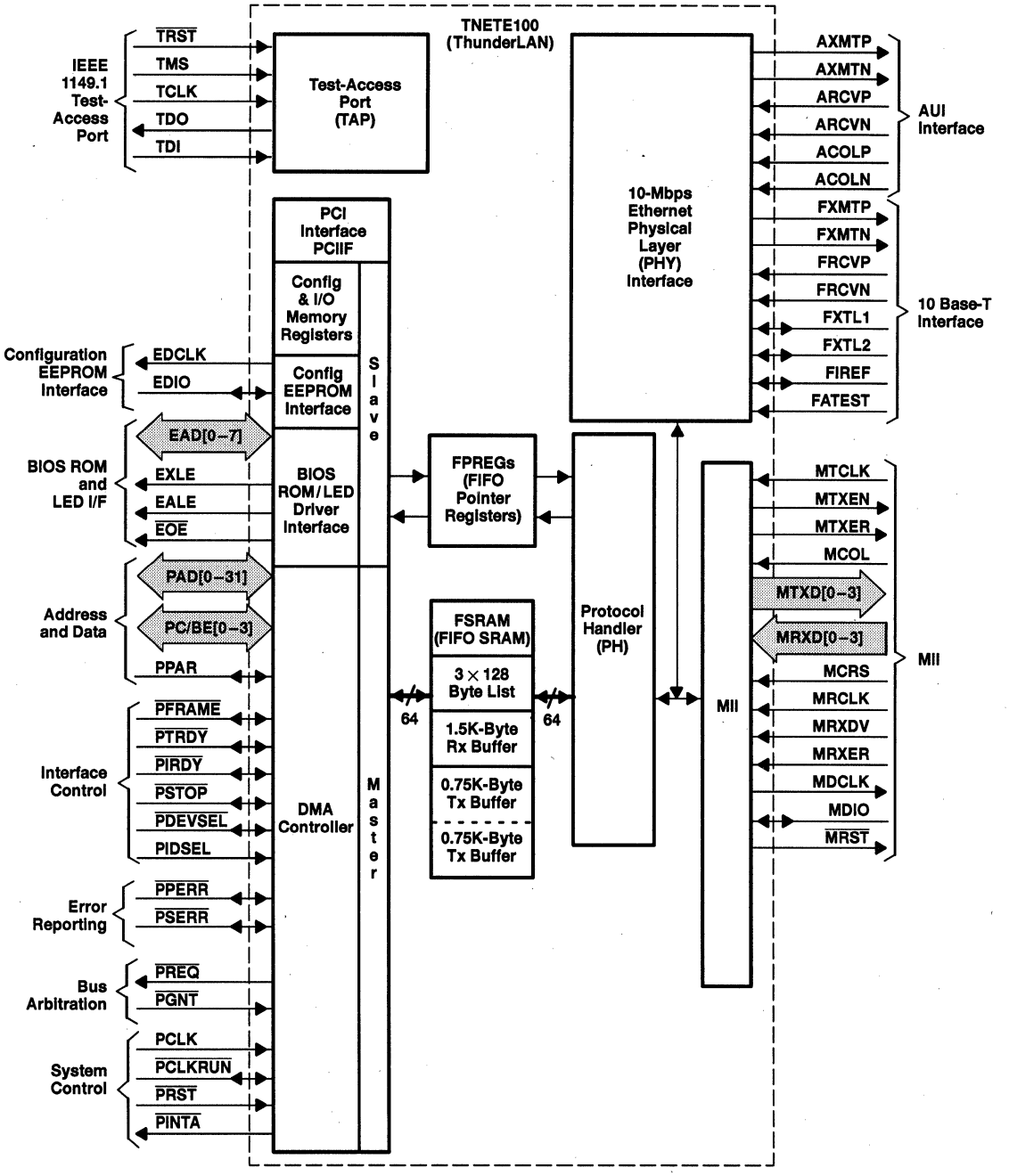
functional block diagram



TEXAS INSTRUMENTS
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Pin Functions

PIN NAME	PIN NO.	TYPE†	DESCRIPTION
TEST PORT			
TCLK	124	I	Test clock. TCLK is used to clock state information and test data into and out of the device during operation of the test port.
TDI	126	I	Test data input. TDI is used to serially shift test data and test instructions into the device during operation of the test port.
TDO	125	O	Test data output. TDO is used to serially shift test data and test instructions out of the device during operation of the test port.
TMS	123	I	Test mode select. TMS is used to control the state of the test port controller within TNETE100.
$\overline{\text{TRST}}$	121	I	Test reset. $\overline{\text{TRST}}$ is used for asynchronous reset of the test port controller.
PCI INTERFACE			
PAD31	135	I/O	PCI address/data bus. Byte 3 (most significant) of the PCI address/data bus.
PAD30	137		
PAD29	138		
PAD28	140		
PAD27	141		
PAD26	143		
PAD25	144		
PAD24	1		
PAD23	5	I/O	PCI address/data bus. Byte 2 of the PCI address/data bus.
PAD22	7		
PAD21	8		
PAD20	9		
PAD19	11		
PAD18	12		
PAD17	13		
PAD16	15		
PAD15	29	I/O	PCI address/data bus. Byte 1 of the PCI address/data bus.
PAD14	30		
PAD13	32		
PAD12	33		
PAD11	35		
PAD10	36		
PAD9	38		
PAD8	39		

† I = input, O = output, I/O = 3-state input/output

ADVANCE INFORMATION

Pin Functions (Continued)

PIN NAME	PIN NO.	TYPE†	DESCRIPTION
PCI INTERFACE (CONTINUED)			
PAD7	42	I/O	PCI address/data bus. Byte 0 (least significant) of the PCI address/data bus.
PAD6	43		
PAD5	45		
PAD4	46		
PAD3	47		
PAD2	49		
PAD1	50		
PAD0	51		
PCLK	131	I	PCI clock. PCLK is the clock reference for all PCI bus operations. All other PCI pins except $\overline{\text{PRST}}$ and $\overline{\text{PINTA}}$ are sampled on the rising edge of PCLK. All PCI bus timing parameters are defined with respect to this edge.
$\overline{\text{PCLKRUN}}$	53	I/O‡	Clock run control. $\overline{\text{PCLKRUN}}$ is the active-low PCI clock request/grant signal that allows the TNETE100 to indicate when an active PCI clock is required. (This is an open drain.)
PC/BE3	2	I/O	PCI bus command and byte enables. PC/BE3 enables byte 3 (MSB) of the PC/BE pins.
PC/BE2	16		PCI bus command and byte enables. PC/BE2 enables byte 2 of PCI address/data bus.
PC/BE1	28		PCI bus command and byte enables. PC/BE1 enables byte 1 of PCI address/data bus.
PC/BE0	41		PCI bus command and byte enables. PC/BE0 enables byte 0 of PCI address/data bus.
$\overline{\text{PDEVSEL}}$	21	I/O	PCI device select. $\overline{\text{PDEVSEL}}$ indicates that the driving device has decoded one of its addresses as the target of the current access. The TNETE100 drives $\overline{\text{PDEVSEL}}$ when it decodes an access to one of its registers. As a bus master, the TNETE100 monitors $\overline{\text{PDEVSEL}}$ to detect accesses to illegal memory addresses.
$\overline{\text{PFRAME}}$	17	I/O	PCI cycle frame. $\overline{\text{PFRAME}}$ is driven by the active bus master to indicate the beginning and duration of an access. It is asserted to indicate the start of a bus transaction. $\overline{\text{PFRAME}}$ remains asserted during the transaction, only being deasserted in the final data phase.
$\overline{\text{PGNT}}$	132	I	PCI bus grant. $\overline{\text{PGNT}}$ is asserted by the system arbiter to indicate that the TNETE100 has been granted control of the PCI bus.
PIDSEL	4	I	PCI initialization device select. PIDSEL is the chip select for access to PCI configuration registers.
$\overline{\text{PINTA}}$	128	O/D	PCI interrupt. $\overline{\text{PINTA}}$ is the interrupt request from the TNETE100. PCI interrupts are shared, so this is an open-drain (wired-OR) output.
$\overline{\text{PIRDY}}$	19	I/O	PCI initiator ready. $\overline{\text{PIRDY}}$ is driven by the active bus master to indicate that it is ready to complete the current data phase of a transaction. A data phase is not completed until both $\overline{\text{PIRDY}}$ and $\overline{\text{PTRDY}}$ are sampled asserted. When the TNETE100 is a bus master, it uses $\overline{\text{PIRDY}}$ to align incoming data on reads or outgoing data on writes with its internal RAM access synchronization (maximum one cycle at the beginning of burst). When the TNETE100 is a bus slave, it extends the access appropriately until both $\overline{\text{PIRDY}}$ and $\overline{\text{PTRDY}}$ are asserted.
$\overline{\text{PTRDY}}$	20	I/O	PCI target ready. $\overline{\text{PTRDY}}$ is driven by the selected device (bus slave or target) to indicate that it is ready to complete the current data phase of a transaction. A data phase is not completed until both $\overline{\text{PIRDY}}$ and $\overline{\text{PTRDY}}$ are sampled asserted. ThunderLAN uses $\overline{\text{PTRDY}}$ to ensure every direct I/O (DIO) operation is correctly interlocked.
PPAR	27	I/O	PCI parity. PPAR carries even parity across PAD[0–31] and PC/BE[0–3]. It is driven by the TNETE100 during all address and write cycles as a bus master and during all read cycles as a bus slave.
$\overline{\text{PPERR}}$	24	I/O	PCI parity error. $\overline{\text{PPERR}}$ indicates a data parity error on all PCI transactions except special cycles.

† I = input, I/O = 3-state input/output, O/D = open-drain output
‡ Open drain

Pin Functions (Continued)

PIN NAME	PIN NO.	TYPE†	DESCRIPTION
PCI INTERFACE (CONTINUED)			
$\overline{\text{PREQ}}$	134	I/O	PCI bus request. $\overline{\text{PREQ}}$ is asserted by the TNETE100 to request control of the PCI bus. This is not a shared signal.
$\overline{\text{PRST}}$	129	I	PCI reset signal.
$\overline{\text{PSERR}}$	25	O/D	PCI system error. $\overline{\text{PSERR}}$ indicates parity errors, or special cycle data parity errors.
$\overline{\text{PSTOP}}$	23	I/O	PCI stop. $\overline{\text{PSTOP}}$ indicates the current target is requesting the master to stop the current transaction.
BIOS ROM/LED DRIVER INTERFACE			
EAD7 EAD6 EAD5 EAD4 EAD3 EAD2 EAD1 EAD0	54 55 56 57 59 60 61 62	I/O	EPROM address/data. EAD[0–7] is a multiplexed byte bus that is used to address and read data from an external BIOS ROM. • On the cycle when EXLE is asserted low, EAD[0–7] is driven with the high byte of the address. • On the cycle when EALE is asserted low, EAD[0–7] is driven with the low byte of the address. • When $\overline{\text{EOE}}$ is asserted, BIOS ROM data should be placed on the bus. These pins can also be used to drive external status LEDs. Low-current (2–5 mA) LEDs can be connected directly (through appropriate resistors). High-current LEDs can be driven through buffers or from the BIOS ROM address latches.
EALE	65	O	EPROM address latch enable. EALE is driven low to latch the low (least significant) byte of the BIOS ROM address from EAD[0–7].
$\overline{\text{EOE}}$	64	O	EPROM output enable. When $\overline{\text{EOE}}$ is active (low) EAD[0–7] is 3-stated and the output of the BIOS ROM should be placed on EAD[0–7].
EXLE	66	O	EPROM extended address latch enable. EXLE is driven low to latch the high (most significant) byte of the BIOS ROM address from EAD[0–7].
CONFIGURATION EEPROM INTERFACE			
EDCLK	68	O	EEPROM data clock. EDCLK transfers serial clocked data to the 2K-bit serial EEPROMs (24C02) (see Note 1).
EDIO	69	I/O	EEPROM data I/O. EDIO is the bidirectional serial data/address line to the 2K-bit serial EEPROM (24C02). EDIO requires an external pullup for EEPROM operation. Tying EDIO to ground disables the EEPROM interface and prevents autoconfiguration of the PCI configuration register.
MEDIA INDEPENDENT INTERFACE (100-Mbps CSMA/CD AND DEMAND PRIORITY)			
MCOL	80	I	Collision sense • In CSMA/CD mode, assertion of MCOL indicates a network collision. • In demand priority mode, MCOL (active low) is used to acknowledge a transmission request. The TNETE100 begins frame transmission 50 MTCLK cycles after the assertion (low) of MCOL.
MCRS	81	I	Carrier sense. MCRS indicates a frame carrier signal is being received.
MDCLK	91	O	Management data clock. MDCLK is part of the serial management interface to physical media independent (PMI)/PHY chip.
MDIO	93	I/O	Management data I/O. MDIO is part of the serial management interface to PMI/PHY chip.
MRCLK	82	I	Receive clock. MRCLK is the receive clock source from the attached PHY and PMI device.
$\overline{\text{MRST}}$	95	O	MII reset. $\overline{\text{MRST}}$ is the reset signal to the PMI/PHY front-end (active low).

† I = input, O = output, I/O = 3-state input/output, O/D = open-drain output

NOTE 1: This pin should be tied to V_{DD} with a 4.7-kΩ – 10-kΩ pullup resistor.

ADVANCE INFORMATION

Pin Functions (Continued)

PIN NAME	PIN NO.	TYPE†	DESCRIPTION
MEDIA INDEPENDENT INTERFACE (100-Mbps CSMA/CD AND DEMAND PRIORITY) (CONTINUED)			
MRXD0 MRXD1 MRXD2 MRXD3	83 85 86 87	I	Receive data. MRXD[0–3] is the nibble receive data from the physical media dependent (PMD) front end. In demand priority mode, ThunderLAN reads the frame priority of incoming frames on these pins on the cycle before assertion of MRXDV (the cycle before frame reception begins). • MRXD1 indicates the transmission priority of the received frame. A value of zero indicates normal transmission, and a value of one indicates priority transmission. Data on these pins is always synchronous to MRCLK.
MRXDV	89	I	Receive data valid. MRXDV indicates data on MRXD[0–3] is valid.
MRXER	90	I	Receive error. MRXER indicates reception of a coding error on received data.
MTCLK	71	I	Transmit clock. MTCLK is the transmit clock source from the attached PHY and PMI device.
MTXD0 MTXD1 MTXD2 MTXD3	72 73 74 76	O	Transmit data. MTXD[0–3] is the nibble transmit data from TNETE100; when MTXEN is asserted these pins carry transmit data. In demand priority mode, the TNETE100 drives the request state of the adapter on these pins when MXTEN is not asserted (frame transmission not in progress). • MXTD0 asserted indicates the TNETE100 is requesting frame transmission. • MXTD1 indicates the transmission priority required. A value of zero indicates normal transmission, and a value of one priority transmission. Data on these pins is always synchronous to MTCLK.
MTXER	78	O	Transmit error. MTXER allows coding errors to be propagated across the MII.
MXTEN	77	O	Transmit enable. MXTEN indicates valid transmit data on MTXD[0–3].
NETWORK INTERFACE (10 Base-T AND AUI)			
ACOLN ACOLP	111 109	A	AUI receive pair. ACOLN and ACOLP are differential line receiver inputs and connect to receive pair via transformer isolation, etc.
ARCVN ARCVP	108 106	A	AUI receive pair. ARCVN and ARCVP are differential line receiver inputs and connect to receive pair via transformer isolation, etc.
AXMTP AXMTN	99 100	A	AUI transmit pair. AXMTP and AXMTN are differential line transmitter outputs.
FATEST	118	A	Analog test pin. FATEST provides access to the filter of the reference PLL.
FIREF	116	A	Current reference. FIREF is used to set a current reference for the analog circuitry.
FONLY	120	A	Front-end only pin. When FONLY is tied high, all TNETE100 functions other than the on-chip front end are disabled. The MII interface pins allow the PHY to be used as a stand-alone 10 Base-T front end.
FRCVN FRCVP	105 103	A	10 Base-T transmit pair. FRCVN and FRCVP are differential line receiver inputs and connect to receive pair via transformer isolation, etc.
FXTL1 FXTL2	113 114	A	Crystal oscillator pins. Connect 20-MHz crystal across these two pins, or drive FXTL1 from a 20-MHz crystal oscillator module.
FXMTP FXMTN	97 98	A	10 Base-T transmit pair. FXMTP and FXMTN are differential line transmitter outputs.

† I = input, O = output, A = Analog

Pin Functions (Continued)

PIN NAME	PIN NO.	TYPE†	DESCRIPTION
			POWER
V_{DDI}	6, 14, 34, 48, 70, 79, 122, 136, 142	PWR	PCI V_{DD} pins. V_{DDI} pins provide power for the PCI I/O pin drivers. Connect V_{DDI} pins to a 5-volt power supply when using 5-V signals on the PCI bus. Connect V_{DDI} pins to a 3-volt power supply when using 3-V signals on the PCI bus.
V_{DDL}	22, 37, 58, 84, 94, 130	PWR	Logic V_{DD} pins (5 V). V_{DDL} pins provide power for internal TNETE100 logic, and they should always be connected to 5 V.
V_{DDOSC}	115	PWR	Analog power pin. V_{DDOSC} is the 5-V power for the crystal oscillator circuit.
V_{DDR}	104 107	PWR	Analog power pin. V_{DDR} is the 5-V power for the receiver circuitry.
V_{DDT}	96	PWR	Analog power pin. V_{DDT} is the 5-V power for the transmitter circuitry.
V_{DDVCO}	117	PWR	Analog power pin. V_{DDVCO} is the 5-V power for the voltage controller oscillator (VCO) and filter input.
V_{SSI}	3, 10, 26, 31, 40, 52, 67, 88, 127, 139	PWR	PCI I/O ground pins
V_{SSL}	18, 44, 63, 75, 92, 133	PWR	Logic ground pins
V_{SSOSC}	112	PWR	Analog power pin. Ground for crystal oscillator circuit
V_{SSR}	102 110	PWR	Analog power pin. Ground for receiver circuitry
V_{SST}	101	PWR	Analog power pin. Ground for transmitter circuitry
V_{SSVCO}	119	PWR	Analog power pin. Ground for VCO and filter input

† PWR = power

ADVANCE INFORMATION

architecture

The major blocks of the TNETE100 include the PCI interface (PCIIF), protocol handler (PH), physical layer (PHY), FIFO pointer registers (FPREGS), FIFO SRAM (FSRAM), and a test-access port (TAP). The functionality of these blocks is described in the following sections.

PCI interface (PCIIF)

The TNETE100 PCIIF contains a byte-aligning DMA controller that allows frames to be fragmented into any byte length and transferred to any byte address while supporting 32-bit data streaming. For multipriority networks it can provide multiple data channels, each with separate lists, commands, and status. Data for the channels is passed to and from the PH by way of circular buffer FIFOs in the SRAM, controlled through FIFO registers. The configuration EEPROM interface (CEI), BIOS ROM/LED driver interface (BRI), configuration and I/O memory registers (CIOREGS), and DMA controller are subblocks of the PCIIF. The features of these subblocks are as follows:

configuration EEPROM interface (CEI)

The CEI provides a means for autoconfiguration of the PCI configuration registers. Certain registers in the PCI configuration space may be loaded using the CEI. Autoconfiguration allows builders of TNETE100-based systems to customize the contents of these registers to identify their own system, rather than using the TI defaults. The EEPROM is read at power up and can then be read from, and written to, under program control.

BIOS ROM/LED driver interface (BRI)

The BRI addresses and reads data from an external BIOS ROM via a multiplexed byte-wide bus. The ROM address/data pins can also be multiplexed to drive external status LEDs.

configuration and I/O memory registers (CIOREGS)

The CIOREGS reside in the configuration space, which is 256 bytes in length. The first 64 bytes of the configuration space is the header region, which is explicitly defined by the PCI standard.

DMA controller (DMAC)

The DMAC is responsible for coordinating TNETE100 requests for mastership of the PCI bus. The DMAC provides byte-aligning DMA control allowing byte-size fragmented frames to be transferred to any byte address while supporting 32-bit data streaming.

protocol handler (PH)

The PH implements the serial protocols of the network. On transmit, it serializes data, adds framing and CRC fields, and interfaces to the network PHY. On receive, it provides address recognition, CRC and error checking, frame disassembly, and deserialization. Data for multiple channels is passed to and from the PH by way of circular buffer FIFOs in the FSRAM controlled through FPREGS. The PH supports a Media Independent Interface (MII) that is compatible with the IEEE 802.12 and IEEE 802.3u logic.

media independent interface (MII)

The MII provides both MAC-level 100 Base-T (IEEE 802.3u) and 100VG-AnyLAN (IEEE 802.12) controller functions to external PHY chips that handle the PHY layer functions for 100-Mbps CSMA/CD and demand priority. The MII also is used to communicate with the on-chip 10 Base-T PHY.

10 Base-T physical layer (PHY)

The PHY acts as an on-chip front-end providing physical layer functions for both 10 Base-5 (AUI) and 10 Base-T (twisted pair). The PHY provides Manchester encoding/decoding from MII nibble format data, smart squelch, jabber detection, link pulse detection, autopolarity control, 10 Base-T transmission waveshaping, and antialiasing filtering. Connection to the AUI drop cable for the 10 Base-T twisted pair is made via simple isolation transformers (see Figure 2) and no external filter networks are required. Suitable external termination components allow the use of either shielded or unshielded twisted-pair cable (150 Ω or 100 Ω). Some of the key features of the on-chip PHY are listed below.

- Integrated filters
- Integrated MII interface including encoder/decoder
- 10 Base-T transceiver
- AUI transceiver
- Autopolarity (reverse polarity correction)
- Loopback for twisted pair and AUI
- Full-duplex mode for simultaneous 10 Base-T transmission and reception
- Low power

10 Base-T physical layer (continued)

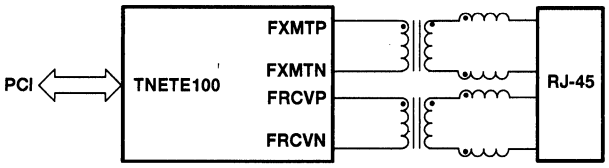

Figure 2. Schematic for 10 Base-T Network Interface Using TNETE100

FIFO pointer registers (FPREGS)

The FPREGS are used to implement circular buffer FIFOs in the SRAM. They are a collection of pointer and counter registers used to maintain the FIFO operation. Both the PCIIF and PH use FPREGS to determine where to read or write data in the SRAM and to determine how much data the FIFO contains. Unique receive and transmit FIFO.registers are needed for each data channel supported.

FIFO SRAM (FSRAM)

The FSRAM is a conventional SRAM array accessed synchronously to the PCI bus clock. Access to the RAM is allocated on a time-division multiplexed (TDM) basis, rather than through a conventional shared bus. This removes the need for bus arbitration and provides guaranteed bandwidth. Half the RAM accesses (every other cycle) are allocated to the PCI controller. It has a 64-bit access port to the RAM, giving it 1 Gbps of bandwidth, sufficient to support 32-bit data streaming on the PCI bus. The PH has one quarter the RAM accesses, and its port may be up to 64 bits wide. A 64-bit port for the PH provides 512 Mbps of bandwidth, more than sufficient for a full-duplex 100-Mbps network. The remaining RAM accesses can be allocated toward providing even more PH bandwidth. The RAM is also accessible (for diagnostic purposes) from the TNETE100 internal data bus. Host DIO (mapped I/O) accesses are used by the host to access internal TNETE100 registers and for adapter test.

- 3.375K bytes of FSRAM
  - 1.5K-byte FIFO for receive
  - Two 0.75K-byte FIFOs for the two transmit channels
  - Three 128-byte lists
- In *one-channel* mode, the two transmit channels are combined giving a single 1.5K-byte FIFO for a single transmit channel

Supporting 1.5K byte of FIFO per channel allows full frame buffering of Ethernet frames. PCI latency is such that a minimum of 500 bytes of storage is required to support 100-Mbps LANs.

test-access port (TAP)

Compliant with IEEE Standard 1149.1, the TAP is comprised of five pins that are used to interface serially with the device and the board on which it is installed for boundary-scan testing.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 2) ..... – 0.5 V to 7 V
Input voltage range (see Note 2) ..... – 0.5 V to 7 V
Output voltage range ..... – 0.5 V to 7 V
Power dissipation ..... 2 W
Maximum operating case temperature ..... 95°C
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: Voltage values are with respect to V_{SS}, and all V_{SS} pins should be routed so as to minimize inductance to system ground.

The recommended operating conditions and the electrical characteristics tables are divided into groups, depending on pin function:

- PCI interface pins
- Logic pins
- Physical layer pins

The PCI signal pins may be operated in one of two modes shown in the PCI tables.

- 5-V signal mode
- 3-V signal mode

recommended operating conditions (PCI interface pins only) (see Note 3)

			3-V SIGNALING OPERATION			5-V SIGNALING OPERATION			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{DD}	Supply voltage (PCI)		3	3.3	3.6	4.75	5	5.25	V
V_{IH}	High-level input voltage		$0.5 \times V_{DD}$		$V_{DD}+0.5$	2.0		$V_{DD}+0.5$	V
V_{IL}	Low-level input voltage, TTL-level signal (see Note 4)		−0.5		$0.3 \times V_{DD}$	−0.5		0.8	V
I_{OH}	High-level output current	TTL outputs			−0.5			−2	mA
I_{OL}	Low-level output current (see Note 5)	TTL outputs			1.5			6	mA
T_A	Operating free-air temperature		0		70	0		70	°C

NOTES: 3. PCI interface pins include V_{DDI}, $\overline{\text{PCLKRUN}}$, $\overline{\text{PFRAME}}$, $\overline{\text{PTRDY}}$, $\overline{\text{PIRDY}}$, $\overline{\text{PSTOP}}$, $\overline{\text{PDEVSEL}}$, PIDSEL, $\overline{\text{PPERR}}$, $\overline{\text{PSERR}}$, $\overline{\text{PREQ}}$, $\overline{\text{PGNT}}$, PCLK, PPAR, $\overline{\text{PRST}}$, $\overline{\text{PINTA}}$, PAD[0–31], PC/$\overline{\text{BE}}$[0–3], $\overline{\text{TRST}}$, TMS, TCLK, TDO, TDI.

4. The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used for logic-voltage levels only.

5. Output current of 2 mA is sufficient to drive five low-power Schottky TTL loads or ten advanced low-power Schottky TTL loads (worst case).

ADVANCE INFORMATION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (PCI interface pins)

PARAMETER		TEST CONDITIONS†		3-V SIGNALING OPERATION		5-V SIGNALING OPERATION		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage, TTL-level signal (see Note 6)	V_{DD} = MIN,	I_{OH} = MAX	0.9 × V_{DD}		2.4		V
V_{OL}	Low-level output voltage, TTL-level signal	V_{DD} = MAX,	I_{OL} = MAX		0.1 × V_{DD}		0.5	V
I_{OZ}	High-impedance output current	V_{DD} = MAX,	V_O = 0 V		10		10	µA
		V_{DD} = MAX,	V_O = V_{DD}		−10		− 10	
I_I	Input current, any input or input/output	V_I = V_{SS} to V_{DD}			± 10		± 70	µA
I_{DD}	Supply current	V_{DD} = MAX			50		60	mA
C_i	Input capacitance, any input	f = 1 MHz,	Others at 0 V		10		10	pF
C_O	Output capacitance, any output or input/output	f = 1 MHz,	Others at 0 V		10		10	pF

† For conditions shown as MIN/MAX, use the appropriate value specified under the recommended operating conditions.
NOTE 6: The following signals require an external pullup resistor: $\overline{PSERR}$, $\overline{PINTA}$.

recommended operating conditions (logic pins) (see Note 7)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage (5 V only)		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		V_{DD}+0.3	V
V_{IL}	Low-level input voltage, TTL-level signal (see Note 4)		−0.3		0.8	V
I_{OH}	High-level output current	TTL outputs			−4	mA
I_{OL}	Low-level output current (see Note 5)	TTL outputs			4	mA
T_A	Operating free-air temperature		0		70	°C

NOTES: 4. The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used for logic-voltage levels only.
5. Output current of 2 mA is sufficient to drive five low-power Schottky TTL loads or ten advanced low-power Schottky TTL loads (worst case).
7. Logic pins include V_{DDL}, EAD[0–7], EXLE, EALE, $\overline{EOE}$, EDCLK, EDIO, FONLY, MTCLK, MTXEN, MTXER, MCOL, MTXD[0–3], MRXD[0–3], MCRS, MRCLK, MRXDV, MRXER, MDCLK, MDIO, $\overline{MRST}$.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (logic pins)

PARAMETER		TEST CONDITIONS†		MIN	MAX	UNIT
V_{OH}	High-level output voltage, TTL-level signal	V_{DD} = MIN,	I_{OH} = MAX	2.4		V
V_{OL}	Low-level output voltage, TTL-level signal	V_{DD} = MAX,	I_{OL} = MAX		0.5	V
I_O	High-impedance output current	V_{DD} = MIN,	V_O = V_{DD}		10	µA
		V_{DD} = MIN,	V_O = 0 V		−10	
I_I	Input current	V_I = V_{SS} to V_{DD}			±1	µA
I_{DD}	Supply current	V_{DD} = MAX			400	mA
C_i	Input capacitance, any input	f = 1 MHz,	Others at 0 V		10	pF
C_o	Output capacitance, any output or input/output	f = 1 MHz,	Others at 0 V		10	pF

† For conditions shown as MIN/MAX, use the appropriate value specified under the recommended operating conditions.

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recommended operating conditions (physical layer pins) (see Note 8)

PARAMETER		JEDEC SYMBOL	MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.75	5	5.25	V
V_B	Receiver input bias voltage (see Note 9)	V_{IB}	$V_{SB}-1$		$V_{SB}+1$	V
T_A	Operating free-air temperature		0		70	°C

NOTES: 8. Physical layer pins include V_{DDOSC}, V_{DDR}, V_{DDT}, V_{DDVCO}, ACOLN, ACOLP, ARCVN, ARCVP, AXMTP, AXMTN, FATEST, FIREF, FRCVN, FRCVP, FXTL1, FXTL2, FXMTP, and FXMTN.

9. V_{SB} is the self-bias voltage of the input pairs ARCVP and ARCVN, ACOLP and ACOLN, and FRCVP and FRCVN. It is defined as $V_{SB} = (V_{SB+} + V_{SB-}) + 2$ (where V_{SB+} is the self-bias voltage of the positive receive pins; V_{SB-} is the self-bias voltage of the negative receive pins). The self-bias voltage of both pins is approximately $V_{DD} + 2$.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (physical interface pins)

10 Base-T receiver input (FRCVP, FRCVN)

PARAMETER		JEDEC SYMBOL	TEST CONDITIONS		MIN	MAX	UNIT
$V_{(CM)}$	Common-mode input voltage	V_{IC}			1.8	3.2	V
$V_{I(DIFF)}$	Differential input voltage	V_{ID}			0.6	2.8	V
$I_{(CM)}$	Common-mode current	I_{IC}				4	mA
V_{SQ+}	Rising input pair squelch threshold		$V_{CM} = V_{SB}$,	See Note 10	270		mV
V_{SQ-}	Falling input pair squelch threshold		$V_{CM} = V_{SB}$,	See Note 10	−270		mV

NOTE 10: V_{SB} is the self-bias of the input FRCVP and FRCVN.

10 Base-T transmitter drive characteristics (FXMTP, FXMTN)

PARAMETER		JEDEC SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
$V_{O(DIFF)NWAV}$	Differential output voltage, transmit waveshaping inactive	$V_{OD(NWAV)}$			±1.77	V
$V_{O(DIFF)WAV}$	Differential uncompensated signal amplitude, waveshaping active	$V_{OD(WAV)}$			±1.253	V
V_{SLW}	Differential voltage at specified slew rate	$V_{OD(SLEW)}$		±2.2	±2.8	V
$V_{O(CM)}$	Common-mode output voltage	V_{OC}	See Figure 3d	0	4	V
$V_{O(DIFF)}$	Differential voltage output	V_{OD}	Into open circuit		5.25	V
$V_{O(I)}$	Output idle differential voltage	$V_{OD(IDLE)}$			±50	mV
$I_{O(I)}$	Output idle differential current	$I_{OD(IDLE)}$			±0.5	mA
$I_{O(FC)}$	Output current, fault condition	$I_{O(FC)}$			300	µA

ADVANCE INFORMATION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (physical interface pins) (continued)

AUI receiver input (ARCVP, ARCVN, ACOLP, ACOLN)

PARAMETER			JEDEC SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
$V_{(CM1)}$	Common-mode input voltage 1		$V_{IC(1)}$	dc + ac, See Note 11	1	4.2	V
$V_{(CM2)}$	Common-mode input voltage 2		$V_{IC(2)}$	dc + ac, See Note 11	1	2.5	V
$V_{I(DIFF)1}$	Differential input voltage 1		$V_{ID(1)}$	See Note 12	0	3	V
$V_{I(DIFF)2}$	Differential input voltage 2		$V_{ID(2)}$	See Note 13	0	100	mV
$I_{(CM)}$	Common-mode current		I_{IC}	See Note 14		1	mA
I_{IFC}	Input current, fault condition		$I_{I(FC)}$			10	mA
$V_{(SQ)}$	Input squelch threshold	To activate		See Note 15, 20 ns < X < 35 ns	−325	−175	mV
		Not to activate			−175	0	mV

NOTES: 11. This parameter means the composite ac signal plus the dc common-mode voltage shall not exceed the indicated limits. These limits are peak maximum values and are not to be exceeded.
12. Common-mode frequency range – 0 Hz to 40 kHz
13. Common-mode frequency range – 40 kHz to 10 MHz
14. Input bias over the common mode dc voltage range
15. This parameter is a range that is allowed to vary over operating conditions. The reference point for the timing period is from the input pair reaching –175 mV on the falling edge to reaching –175 mV on the rising edge.

AUI transmitter drive characteristics (AXMTP, AXMTN)

PARAMETER		JEDEC SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
$V_{O(DIFF)1}$	Differential output voltage	$V_{OD(1)}$	See Note 16	±500	±1315	mV
$V_{O(CM)}$	Common-mode output voltage	V_{OC}	See Figure 3b	1	4.2	V_{DC}
$V_{OI(DIFF)}$	Output idle differential voltage	$V_{OD(IDLE)}$			±40	mV
$I_{OI(DIFF)}$	Output idle differential current	$I_{OD(IDLE)}$			4	mA
$V_{OI(DIFF)U}$	Output differential undershoot	$V_{OD(IDLE)U}$			100	mV
$V_{O(DIFF)2}$	Output differential voltage into an open circuit	$V_{OD(2)}$	Into open circuit		5	V
$I_{O(FC)}$	Output current, fault condition	$I_{O(FC)}$			150	mA

NOTE 16: The differential voltage is measured across a pair of 39-Ω, ±1% resistors bypassed to signal ground with a 0.01-μF capacitor.

PLL characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{FILT}	Reference PLL operating filter voltage	$t_{c(FXTL1)}$ = 50 ns	0.8	2	V

crystal oscillator characteristics

PARAMETER		JEDEC SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
$V_{SB(FXTL1)}$	Input self-bias voltage	V_{IB}		0.8	2	V
$I_{OH(FXTL2)}$	High-level output current	I_{OH}	$V_{(FXTL2)} = V_{SB(FXTL1)}$ $V_{(FXTL1)} = V_{SB(FXTL1)} + 0.5$ V	−3.5	−6.5	mA
$I_{OL(FXTL2)}$	Low-level output current	I_{OL}	$V_{(FXTL2)} = V_{SB(FXTL1)}$ $V_{(FXTL1)} = V_{SB(FXTL1)} - 0.5$ V	0.7	1.3	mA

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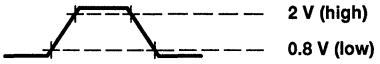
PARAMETER MEASUREMENT INFORMATION

Outputs are driven to a minimum high-logic level of 2.4 V and to a maximum low-logic level of 0.6 V. These levels are compatible with TTL devices.

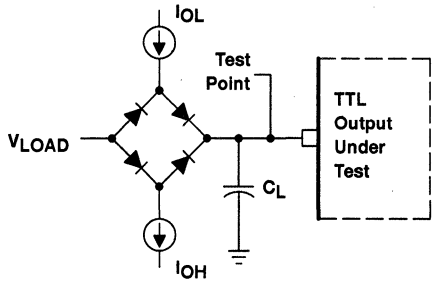
Output transition times are specified as follows: For a high-to-low transition on either an input or output signal, the level at which the signal is said to be no longer high is 2 V and the level at which the signal is said to be low is 0.8 V. For a low-to-high transition, the level at which the signal is said to be no longer low is 0.8 V and the level at which the signal is said to be high is 2 V, as shown below.

The rise and fall times are not specified but are assumed to be those of standard TTL devices, which are typically 1.5 ns.

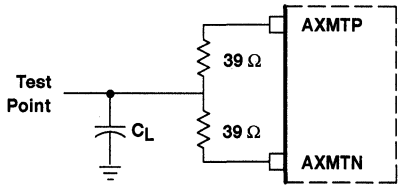


test measurement

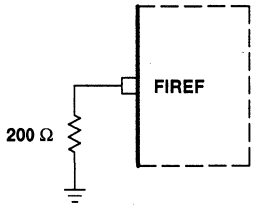
The test-load circuit shown in Figure 3 represents the programmable load of the tester pin electronics that are used to verify timing parameters of the TNETE100 output signals.



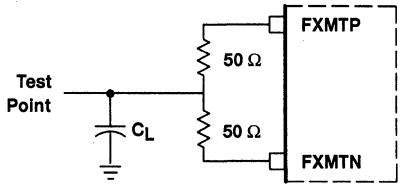
(a) TTL OUTPUT TEST LOAD



(b) AXMTP AND AXMTN TEST LOAD



(c) FIREF TEST CIRCUIT



(d) FXMTP AND FXMTN TEST LOAD

Where: I_{OL} = Refer to I_{OL} in recommended operating conditions
I_{OH} = Refer to I_{OH} in recommended operating conditions
V_{LOAD} = 1.5 V, typical dc-level verification or 0.7 V, typical timing verification
C_L = 18 pF, typical load-circuit capacitance

Figure 3. Test and Load Circuit

PCI 5-V and 3.3-V switching characteristics (see Note 17 and Figure 4)

PARAMETER		MIN	MAX	UNIT
t_{VAL}	Delay time, PCLK to bused signals valid (see Notes 18 and 19)	2	11	ns
$t_{VAL(PTP)}$	Delay time, PCLK to bused signals valid point-to-point (see Notes 18 and 19)	2	12	ns
t_{on}	Float to active delay	2		ns
t_{off}	Active to float delay		28	ns

NOTES: 17. Some of the timing symbols in this table are not currently listed with EIA or JEDEC standards for semiconductor symbology but are consistent with the PCI Local-Bus Specification, Revision 2.0.
18. Minimum times are measured with a 0-pF equivalent load; maximum times are measured with a 50-pF equivalent load. Actual test capacitance may vary, but results should be correlated to these specifications.
19. $\overline{\text{PREQ}}$ and $\overline{\text{PGNT}}$ are point-to-point signals and have different output valid delay and input setup times than do bused signals. $\overline{\text{PGNT}}$ has a setup time of 10 ns; $\overline{\text{PREQ}}$ has a setup time of 12 ns. All other signals are bused.

PCI 5-V and 3.3-V timing requirements (see Note 17 and Figure 4)

			MIN	MAX	UNIT
t_{su}	Setup time, bused signals valid to PCLK (see Note 19)		7		ns
$t_{su(PTP)}$	Setup time to PCLK—point-to-point (see Note 19)		10, 12		ns
t_h	Input hold time from PCLK		0		ns
t_c	Cycle time, PCLK (see Note 20)	100 Mbps	30	50	ns
		10 Mbps	30	500	ns
$t_{w(H)}$	Pulse duration, PCLK high		12		ns
$t_{w(L)}$	Pulse duration, PCLK low		12		ns
t_{slew}	Slew rate, PCLK (see Note 21)		1	4	V/ns

NOTES: 17. Some of the timing symbols in this table are not currently listed with EIA or JEDEC standards for semiconductor symbology but are consistent with the PCI Local-Bus Specification, Revision 2.0.
19. $\overline{\text{PREQ}}$ and $\overline{\text{PGNT}}$ are point-to-point signals and have different output valid delay and input setup times than do bused signals. $\overline{\text{PGNT}}$ has a setup time of 10 ns; $\overline{\text{PREQ}}$ has a setup time of 12 ns. All other signals are bused.
20. As a requirement for frame transmission/reception, the minimum PCLK frequency varies with network speed. The clock may only be stopped in a low state.
21. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform.

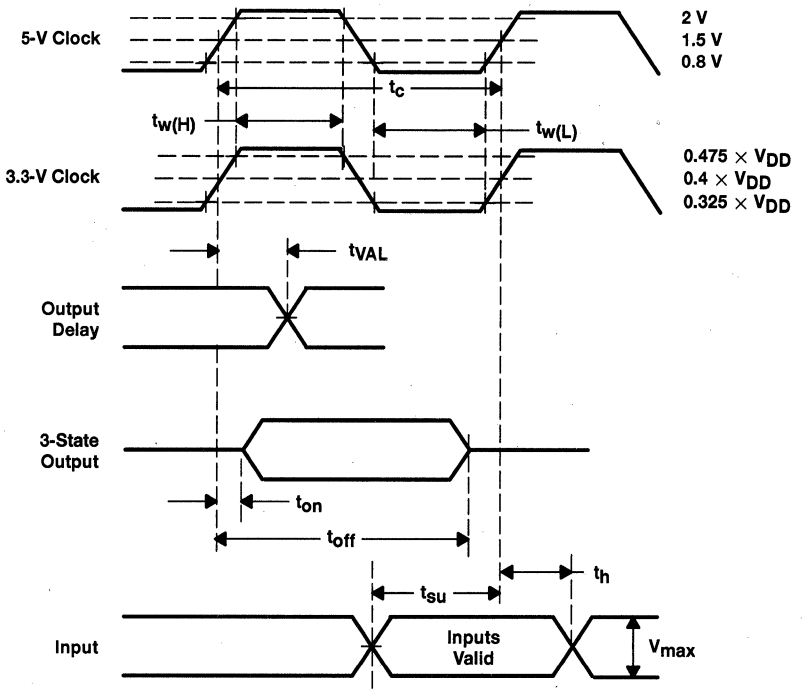


Figure 4. PCI 5-V and 3.3-V Timing

MII receive timing requirements (see Figure 5)†

		MIN	MAX	UNIT
$t_{su(MRX\ pins)}$	Setup time, MRXD[0–3], MRXDV, MRXER (see Note 22)	10		ns
$t_{h(MRX\ pins)}$	Hold time, MTX[0–3], MRXDV, MRXER (see Note 22)	10		ns

MII transmit switching characteristics (see Figure 5)†

PARAMETER		MIN	MAX	UNIT
$t_{d(MTX\ pins)}$	Delay time, MTCLK to MTXD[0–3], MTXEN, and MTXER outputs (see Note 23)	0	25	ns

† Both MCRS and MCOL are driven asynchronously by the PHY.

NOTES: 22. MRXD[0–3] is driven by the PHY on the falling edge of MRXCLK. It is sampled by the reconciliation sublayer synchronous to the edge of MRXCLK. MRXD[0–3] timing must be met during clock periods where MRXDV is asserted. MRXDV is asserted and deasserted by the PHY on the falling edge of MRXCLK. It is sampled by the reconciliation sublayer synchronous to the rising edge of MRXCLK. MRXER is driven by the PHY on the falling edge of MRXCLK. It is sampled by the reconciliation sublayer synchronous to the rising edge of MRXCLK. MRXER timing must be met during clock periods when MRXDV is asserted.

23. MTXD[0–3] is driven by the reconciliation sublayer synchronous to the MTCLK. MTXEN is asserted and deasserted by the reconciliation sublayer synchronous to the MTCLK rising edge. MTXER is driven synchronous to the rising edge of MTCLK.

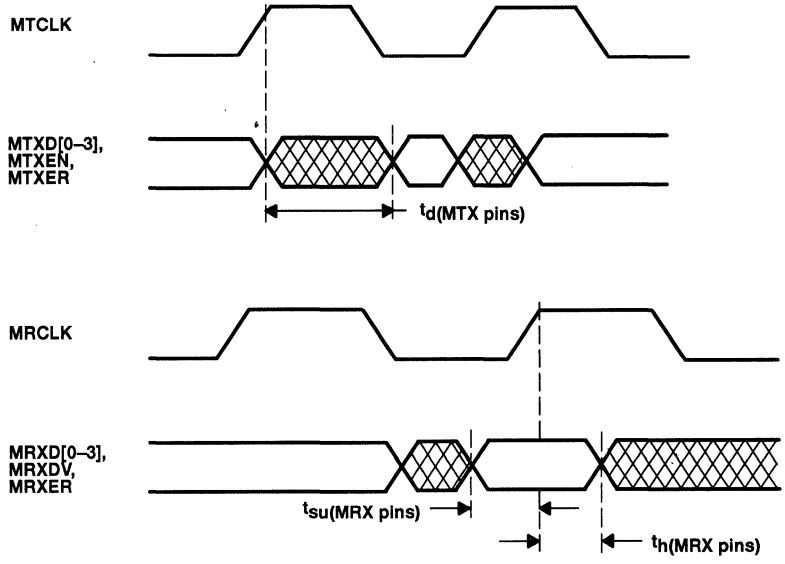


Figure 5. MII Transmit and Receive Timing

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MDIO timing requirements (see Figure 6)

		MIN	MAX	UNIT
$t_{a(MDCLKH-MDIOV)}$	Access time, MDIO valid from MDCLK high (see Note 24)	0	300	ns

MDIO switching characteristics (see Figure 7)

PARAMETER		MIN	MAX	UNIT
$t_{d(MDIOV-MDCLKH)}$	Delay time, MDIO valid to MDCLK high (see Note 25)	10		ns
$t_{d(MDCLKH-MDIOX)}$	Delay time, MDCLK high to MDIO changing (see Note 25)	10		ns

NOTES: 24. When the MDIO signal is sourced by the PMI/PHY, it is sampled by TNETE100 synchronous to the rising edge of MDCLK.
25. MDIO is a bidirectional signal that can be sourced by TNETE100 or the PMI/PHY. When TNETE100 sources the MDIO signal, TNETE100 asserts MDIO synchronous to the rising edge of MDCLK.

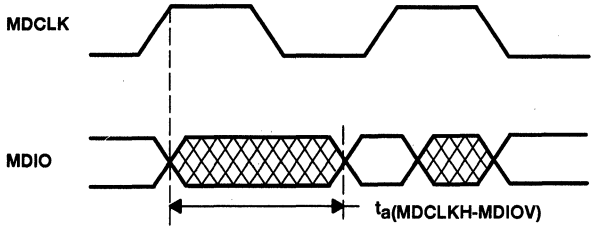

Figure 6. Management Data I/O Timing (Sourced by PHY)

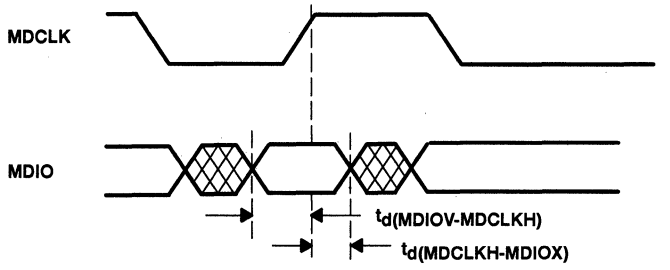

Figure 7. Management Data I/O Timing (Sourced by TNETE100)

BIOS ROM and LED interface timing requirements (see Figure 8)†

		MIN	MAX	UNIT
t_{su}	Setup time, data		250	ns
t_h	Hold time, data	0		ns

BIOS ROM and LED interface switching characteristics (see Figure 8)†

PARAMETER		MIN	MAX	UNIT
$t_{d(EADV-EXLEL)}$	Delay time, address high byte valid to EXLE low (address high byte setup time for external latch)	0		ns
$t_{d(EXLEL-EADZ)}$	Delay time, EXLE low to address high byte invalid (address high byte hold time for external latch)	10		ns
$t_{d(EADV-EALEL)}$	Delay time, address low byte valid to EALE low (address low byte setup time for external latch)	0		ns
$t_{d(EALEL-EADZ)}$	Delay time, EALE low to address low byte invalid (address low byte hold time for external latch)	10		ns
t_a	Access time, address	288		ns

† The EPROM interface, consisting of 11 pins, requires only two TTL '373 latches to latch the high and low addresses.

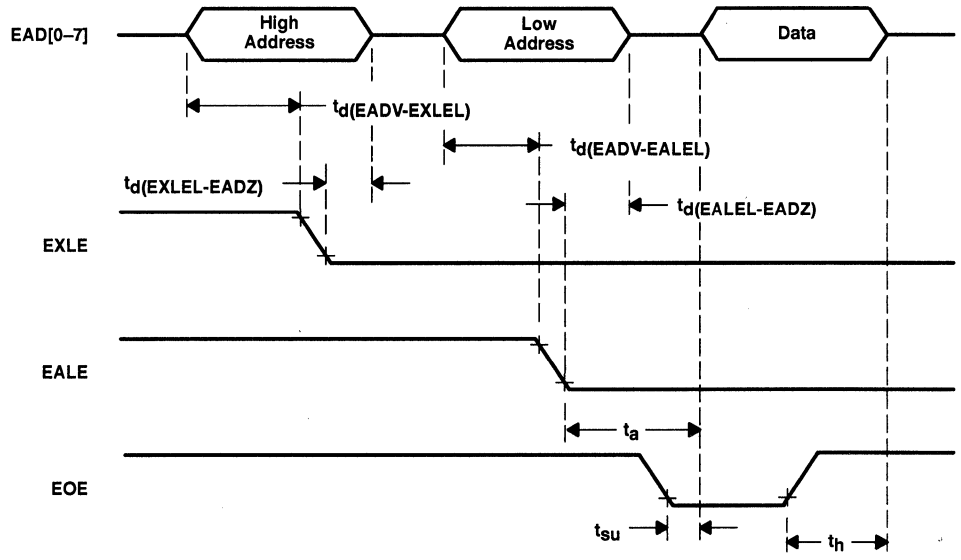

Figure 8. BIOS ROM and LED Interface Timing

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configuration EEPROM interface switching characteristics (see Figure 9)

PARAMETER		MIN	MAX	UNIT
$f_{CLK(EDCLK)}$	Clock frequency, EDCLK	0	100	kHz
$t_{d(EDCLKL-EDIOV)}$	EDCLK low to EDIO data in valid	0.3	3.5	µs
$t_{d(EDIO\ free)}$	Time the bus must be free before a new transmission can start	4.7		µs
$t_{d(EDIOV-EDCLKL)}$	Delay time, EDIO valid after EDCLK low (start condition hold time for EEPROM)	4		µs
$t_{w(L)}$	Low period, clock	4.7		µs
$t_{w(H)}$	High period, clock	4		µs
$t_{d(EDCLKH-EDIOV)}$	Delay time, EDCLK high to EDIO valid (start condition setup time)	4.7		µs
$t_{d(EDCLKL-EDIOX)}$	Delay time, EDCLK low to EDIO changing (data out hold time)	0		µs
$t_{d(EDIOV-EDCLKH)}$	Delay time, EDIO valid to EDCLK high (data out setup time)	250		ns
t_r	Rise time, EDIO and EDCLK		1	µs
t_f	Fall time, EDIO and EDCLK		300	ns
$t_{d(EDCLKH-EDIOH)}$	Delay time, EDCLK high to EDIO high (stop condition setup time)	4.7		µs
$t_{d(EDCLKL-EDIOX)}$	Delay time, EDCLK low to EDIO changing (data in hold time)	300		ns

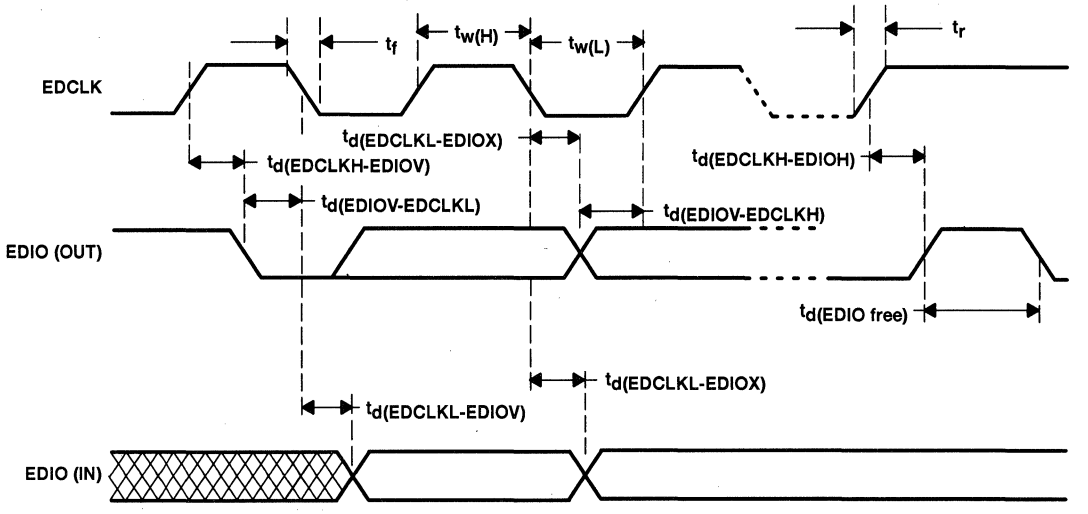

Figure 9. Configuration EEPROM Interface Timing

crystal oscillator timing requirements (see Figure 10)†

		MIN	TYP	MAX	UNIT
$t_{d(VDDH–FXTL1V)}$	Delay time from minimum V_{DD} high level to first valid FXTL1V full swing period (see Note 26)			100	ms
$t_{w(H)}$	Pulse duration at FXTL1 high	13			ns
$t_{w(L)}$	Pulse duration at FXTL1 low	13			ns
t_t	Transition time of FXTL1		7		ns
t_c	Cycle time, FXTL1		50		ns
	Tolerance of FXTL1 input frequency		±0.01		%

† The FXTL signal may be implemented by either connecting a 20-MHz crystal across the FXTL1 and FXTL2 pins or by driving the FXTL1 from a 20-MHz crystal oscillator module.

NOTE 26: This specification is provided as an aid to board design. This specification is not guaranteed during manufacturing testing.

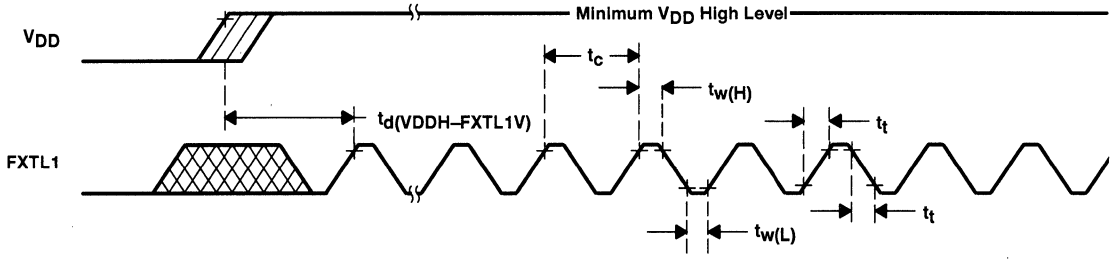

Figure 10. Crystal Oscillator Timing

ADVANCE INFORMATION

- Single-Chip Ethernet™ Adapter for the Peripheral Component Interconnect (PCI) Local Bus
  - 32-Bit PCI† Glueless Host Interface
  - Compliant With PCI Local-Bus Specification (Revision 2.0)
  - 33-MHz Operation
  - 3-V or 5-V I/O Operation
  - Adaptive Performance Optimization™ (APO) for Highest Available PCI Bandwidth
  - High-Performance Bus Master Architecture With Byte-Aligning DMA Controller for Low Host CPU and Bus Utilization
  - Plug-and-Play Compatible
- Supports 32-Bit Data Streaming on PCI Bus
  - Time Division Multiplexed SRAM
  - 2-Gbps Internal Bandwidth
- Switched Ethernet Compatible
- Full-Duplex Compatible With Independent Transmit and Receive Channels
- No On-Board Memory Required
- Auto-Negotiation (N-Way) Compatible
- cLAN (Configurable LAN) Technology
- Integrated 10 Base-T and 10 Base-5 (AUI) Physical Layer Interface
  - Single-Chip IEEE 802.3 and Blue Book Ethernet-Compliant Solution
  - DSP-Based Digital Phase-Locked Loop
  - Smart Squelch Allows for Transparent Link Testing
  - Transmission Waveshaping
  - Autopolarity (Reverse Polarity Correction)
  - External/Internal Loopback Including Twisted Pair and AUI
- Low-Power CMOS Technology
  - Green PC Compatible
  - Microsoft™ Advanced Power Management
- EEPROM Interface Supports Jumperless Design and Autoconfiguration
- Hardware Statistics Registers for Management Information Base (MIB)
- DMTF (Desktop Management Task Force) Compatible
- IEEE Standard 1149.1‡ Test Access Port (JTAG)
- 144-Pin Quad Flat Package

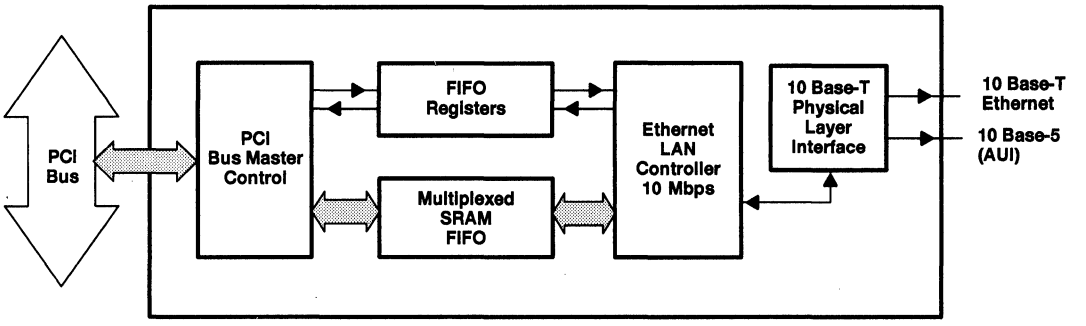

Figure 1. ThunderLAN Architecture

† The PCI Local-Bus Specification, Revision 2.0 should be used as a reference with this document.
‡ IEEE Standard 1149.1–1990, IEEE Standard Test-Access Port and Boundary-Scan Architecture
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Ethernet is a trademark of Xerox Corporation.
Microsoft is a trademark of Microsoft Corporation.

description

ThunderLAN is a high-speed networking architecture that provides a complete PCI-to-10 Base-T/AUI Ethernet solution. The TNETE110, one implementation of the ThunderLAN architecture, is an intelligent protocol network interface. The ThunderLAN SRAM FIFO-based architecture eliminates the need for external memory and offers a single-chip glueless PCI-to-10 Base-T/AUI (IEEE 802.3) solution with an on-board physical layer interface.

The glueless PCI interface supports 32-bit streaming, operates at speeds up to 33 MHz and is capable of internal data transfer rates up to 2 Gbps, taking full advantage of all available PCI bandwidth. The TNETE110 offers jumperless autoconfiguration using PCI configuration read/write cycles. Customizable configuration registers, which can be autoloaded from an external serial EEPROM, allow designers of TNETE110-based systems to give their systems a unique identification code. The TNETE110 PCI interface, developed in conjunction with other leaders in the semiconductor and computer industries, has been vigorously tested on multiple platforms to ensure compatibility across a wide array of available PCI products. In addition, the ThunderLAN drivers and ThunderLAN architecture use TI's patented Adaptive Performance Optimization (APO) technology to dynamically adjust critical parameters for minimum latency, minimum host CPU utilization, and maximum system performance. This technology ensures that the maximum capabilities of the PCI interface are used by automatically tuning the adapter to the specific system in which it is operating.

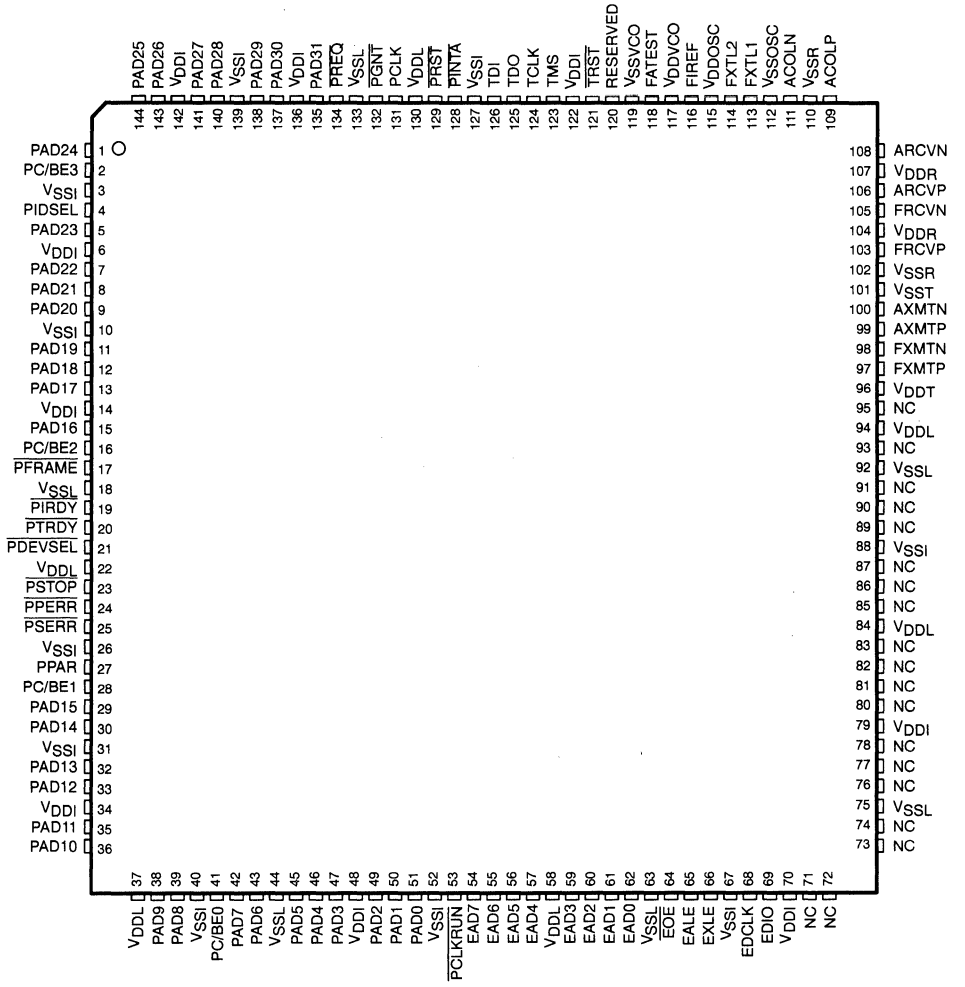
An intelligent protocol handler (PH) implements the serial protocols of the network. The PH is designed for minimum overhead related to multiple protocols, using common state machines to implement 95% of the total protocol handler. On transmit, the PH serializes data, adds framing and cyclic redundancy check (CRC) fields, and interfaces to the network physical layer (PHY) chip. On receive, it provides address recognition, CRC and error checking, frame disassembly, and deserialization. Data for multiple channels is passed to and from the PH by way of circular buffer FIFOs in the FIFO SRAM.

Compliant with IEEE Standard 1149.1, the TNETE110 provides a 5-pin test-access port that is used for boundary-scan testing.

The TNETE110 is available in a 144-pin quad flat package.

pin assignments

PCE PACKAGE
(TOP VIEW)



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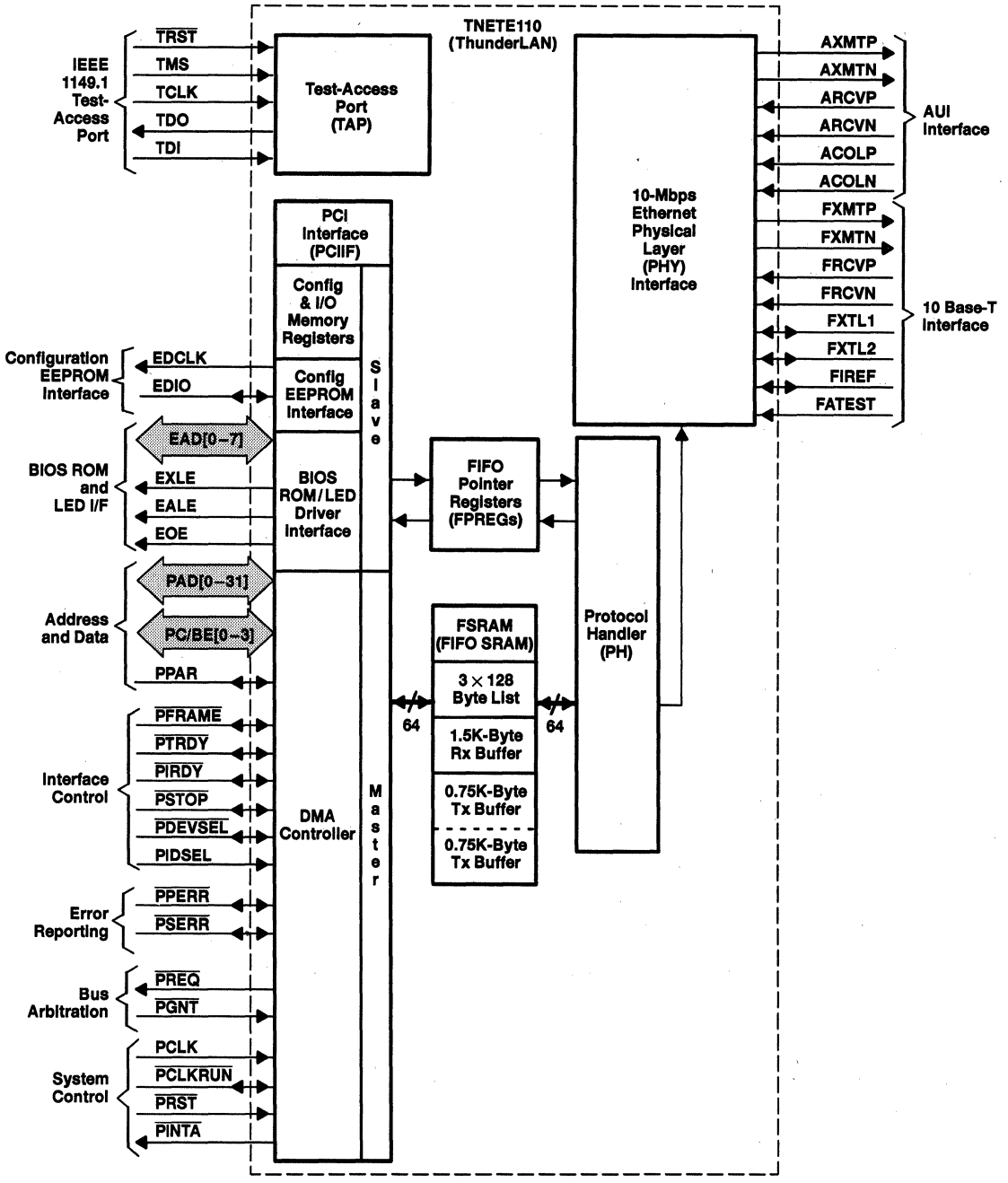
functional block diagram



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Pin Functions

PIN NAME	PIN NO.	TYPE†	DESCRIPTION
TEST PORT			
TCLK	124	I	Test clock. TCLK is used to clock state information and test data into and out of the device during operation of the test port.
TDI	126	I	Test data input. TDI is used to serially shift test data and test instructions into the device during operation of the test port.
TDO	125	O	Test data output. TDO is used to serially shift test data and test instructions out of the device during operation of the test port.
TMS	123	I	Test mode select. TMS is used to control the state of the test port controller within TNETE110.
$\overline{\text{TRST}}$	121	I	Test reset. $\overline{\text{TRST}}$ is used for asynchronous reset of the test port controller.
PCI INTERFACE			
PAD31	135	I/O	PCI address/data bus. Byte 3 (most significant) of the PCI address/data bus.
PAD30	137		
PAD29	138		
PAD28	140		
PAD27	141		
PAD26	143		
PAD25	144		
PAD24	1		
PAD23	5	I/O	PCI address/data bus. Byte 2 of the PCI address/data bus.
PAD22	7		
PAD21	8		
PAD20	9		
PAD19	11		
PAD18	12		
PAD17	13		
PAD16	15		
PAD15	29	I/O	PCI address/data bus. Byte 1 of the PCI address/data bus.
PAD14	30		
PAD13	32		
PAD12	33		
PAD11	35		
PAD10	36		
PAD9	38		
PAD8	39		

† I = input, O = output, I/O = 3-state input/output

Pin Functions (Continued)

PIN NAME	PIN NO.	TYPE†	DESCRIPTION
PCI INTERFACE (CONTINUED)			
PAD7	42	I/O	PCI address/data bus. Byte 0 (least significant) of the PCI address/data bus.
PAD6	43		
PAD5	45		
PAD4	46		
PAD3	47		
PAD2	49		
PAD1	50		
PAD0	51		
PCLK	131	I	PCI clock. PCLK is the clock reference for all PCI bus operations. All other PCI pins except $\overline{\text{PRST}}$ and $\overline{\text{PINTA}}$ are sampled on the rising edge of PCLK. All PCI bus timing parameters are defined with respect to this edge.
$\overline{\text{PCLKRUN}}$	53	I/O‡	Clock run control. $\overline{\text{PCLKRUN}}$ is the active-low PCI clock request/grant signal that allows the TNETE110 to indicate when an active PCI clock is required. (This is an open drain.)
PC/BE3	2	I/O	PCI bus command and byte enables. PC/BE3 enables byte 3 (MSB) of the PC/BE pins.
PC/BE2	16		PCI bus command and byte enables. PC/BE2 enables byte 2 of PCI address/data bus.
PC/BE1	28		PCI bus command and byte enables. PC/BE1 enables byte 1 of PCI address/data bus.
PC/BE0	41		PCI bus command and byte enables. PC/BE0 enables byte 0 of PCI address/data bus.
$\overline{\text{PDEVSEL}}$	21	I/O	PCI device select. $\overline{\text{PDEVSEL}}$ indicates that the driving device has decoded one of its addresses as the target of the current access. The TNETE110 drives $\overline{\text{PDEVSEL}}$ when it decodes an access to one of its registers. As a bus master, the TNETE110 monitors $\overline{\text{PDEVSEL}}$ to detect accesses to illegal memory addresses.
$\overline{\text{PFRAME}}$	17	I/O	PCI cycle frame. $\overline{\text{PFRAME}}$ is driven by the active bus master to indicate the beginning and duration of an access. It is asserted to indicate the start of a bus transaction. $\overline{\text{PFRAME}}$ remains asserted during the transaction, only being deasserted in the final data phase.
$\overline{\text{PGNT}}$	132	I	PCI bus grant. $\overline{\text{PGNT}}$ is asserted by the system arbiter to indicate that the TNETE110 has been granted control of the PCI bus.
PIDSEL	4	I	PCI initialization device select. PIDSEL is the chip select for access to PCI configuration registers.
$\overline{\text{PINTA}}$	128	O/D	PCI interrupt. $\overline{\text{PINTA}}$ is the interrupt request from the TNETE110. PCI interrupts are shared, so this is an open-drain (wired-OR) output.
$\overline{\text{PIRDY}}$	19	I/O	PCI initiator ready. $\overline{\text{PIRDY}}$ is driven by the active bus master to indicate that it is ready to complete the current data phase of a transaction. A data phase is not completed until both $\overline{\text{PIRDY}}$ and $\overline{\text{PTRDY}}$ are sampled asserted. When the TNETE110 is a bus master, it uses $\overline{\text{PIRDY}}$ to align incoming data on reads or outgoing data on writes with its internal RAM access synchronization (maximum one cycle at the beginning of burst). When the TNETE110 is a bus slave, it extends the access appropriately until both $\overline{\text{PIRDY}}$ and $\overline{\text{PTRDY}}$ are asserted.
$\overline{\text{PTRDY}}$	20	I/O	PCI target ready. $\overline{\text{PTRDY}}$ is driven by the selected device (bus slave or target) to indicate that it is ready to complete the current data phase of a transaction. A data phase is not completed until both $\overline{\text{PIRDY}}$ and $\overline{\text{PTRDY}}$ are sampled asserted. ThunderLAN uses $\overline{\text{PTRDY}}$ to ensure every direct I/O (DIO) operation is correctly interlocked.
PPAR	27	I/O	PCI parity. PPAR carries even parity across PAD[0–31] and PC/BE[0–3]. It is driven by the TNETE110 during all address and write cycles as a bus master and during all read cycles as a bus slave.
$\overline{\text{PPERR}}$	24	I/O	PCI parity error. $\overline{\text{PPERR}}$ indicates a data parity error on all PCI transactions except special cycles.

† I = input, I/O = 3-state input/output, O/D = open-drain output
‡ Open drain

Pin Functions (Continued)

PIN NAME	PIN NO.	TYPE†	DESCRIPTION
			PCI INTERFACE (CONTINUED)
$\overline{\text{PREQ}}$	134	I/O	PCI bus request. $\overline{\text{PREQ}}$ is asserted by the TNETE110 to request control of the PCI bus. This is not a shared signal.
$\overline{\text{PRST}}$	129	I	PCI reset signal.
$\overline{\text{PSERR}}$	25	O/D	PCI system error. $\overline{\text{PSERR}}$ indicates parity errors, or special cycle data parity errors.
$\overline{\text{PSTOP}}$	23	I/O	PCI stop. $\overline{\text{PSTOP}}$ indicates the current target is requesting the master to stop the current transaction.
			BIOS ROM/LED DRIVER INTERFACE
EAD7 EAD6 EAD5 EAD4 EAD3 EAD2 EAD1 EAD0	54 55 56 57 59 60 61 62	I/O	EPROM address/data. EAD[0–7] is a multiplexed byte bus that is used to address and read data from an external BIOS ROM. • On the cycle when EXLE is asserted low, EAD[0–7] is driven with the high byte of the address. • On the cycle when EALE is asserted low, EAD[0–7] is driven with the low byte of the address. • When $\overline{\text{EOE}}$ is asserted, BIOS ROM data should be placed on the bus. These pins can also be used to drive external status LEDs. Low-current (2–5 mA) LEDs can be connected directly (through appropriate resistors). High-current LEDs can be driven through buffers or from the BIOS ROM address latches.
EALE	65	O	EPROM address latch enable. EALE is driven low to latch the low (least significant) byte of the BIOS ROM address from EAD[0–7].
$\overline{\text{EOE}}$	64	O	EPROM output enable. When $\overline{\text{EOE}}$ is active (low) EAD[0–7] is 3-stated and the output of the BIOS ROM should be placed on EAD[0–7].
EXLE	66	O	EPROM extended address latch enable. EXLE is driven low to latch the high (most significant) byte of the BIOS ROM address from EAD[0–7].
			CONFIGURATION EEPROM INTERFACE
EDCLK	68	O	EEPROM data clock. EDCLK transfers serial clocked data to the 2K-bit serial EEPROMs (24C02) (see Note 1).
EDIO	69	I/O	EEPROM data I/O. EDIO is the bidirectional serial data/address line to the 2K-bit serial EEPROM (24C02). EDIO requires an external pullup for EEPROM operation. Tying EDIO to ground disables the EEPROM interface and prevents autoconfiguration of the PCI configuration register.
			NETWORK INTERFACE (10 Base-T AND AUI)
ACOLN ACOLP	111 109	A	AUI receive pair. ACOLN and ACOLP are differential line receiver inputs and connect to receive pair via transformer isolation, etc.
ARCVN ARCVP	108 106	A	AUI receive pair. ARCVN and ARCVP are differential line receiver inputs and connect to receive pair via transformer isolation, etc.
AXMTP AXMTN	99 100	A	AUI transmit pair. AXMTP and AXMTN are differential line transmitter outputs.
FATEST	118	A	Analog test pin. FATEST provides access to the filter of the reference PLL.
FIREF	116	A	Current reference. FIREF is used to set a current reference for the analog circuitry.
FRCVN FRCVP	105 103	A	10 Base-T transmit pair. FRCVN and FRCVP are differential line receiver inputs and connect to receive pair via transformer isolation, etc.
FXTL1 FXTL2	113 114	A	Crystal oscillator pins. Connect 20-MHz crystal across these two pins, or drive FXTL1 from a 20-MHz crystal oscillator module.

† I = input, O = output, I/O = 3-state input/output, O/D = open-drain output, A = analog

NOTE 1: This pin should be tied to V_{DD} with a 4.7-kΩ – 10-kΩ pullup resistor.

Pin Functions (Continued)

PIN NAME	PIN NO.	TYPE†	DESCRIPTION
NETWORK INTERFACE (10 Base-T AND AUI) (CONTINUED)			
FXMTP FXMTN	97 98	A	10 Base-T transmit pair. FXMTP and FXMTN are differential line transmitter outputs.
RESERVED	120	I	Reserved. Tie this pin low.
POWER			
V_{DDI}	6, 14, 34, 48, 70, 79, 122, 136, 142	PWR	PCI V_{DD} pins. V_{DDI} pins provide power for the PCI I/O pin drivers. Connect V_{DDI} pins to a 5-volt power supply when using 5-V signals on the PCI bus. Connect V_{DDI} pins to a 3-volt power supply when using 3-V signals on the PCI bus.
V_{DDL}	22, 37, 58, 84, 94, 130	PWR	Logic V_{DD} pins (5 V). V_{DDL} pins provide power for internal TNETE110 logic, and they should always be connected to 5 V.
V_{DDOSC}	115	PWR	Analog power pin. V_{DDOSC} is the 5-V power for the crystal oscillator circuit.
V_{DDR}	104 107	PWR	Analog power pin. V_{DDR} is the 5-V power for the receiver circuitry.
V_{DDT}	96	PWR	Analog power pin. V_{DDT} is the 5-V power for the transmitter circuitry.
V_{DDVCO}	117	PWR	Analog power pin. V_{DDVCO} is the 5-V power for the voltage controller oscillator (VCO) and filter input.
V_{SSI}	3, 10, 26, 31, 40, 52, 67, 88, 127, 139	PWR	PCI I/O ground pins
V_{SSL}	18, 44, 63, 75, 92, 133	PWR	Logic ground pins
V_{SSOSC}	112	PWR	Analog power pin. Ground for crystal oscillator circuit
V_{SSR}	102 110	PWR	Analog power pin. Ground for receiver circuitry
V_{SST}	101	PWR	Analog power pin. Ground for transmitter circuitry
V_{SSVCO}	119	PWR	Analog power pin. Ground for VCO and filter input

† I = input, A = analog, PWR = power

architecture

The major blocks of the TNETE110 include the PCI interface (PCIIF), protocol handler (PH), physical layer (PHY), FIFO pointer registers (FPREGS), FIFO SRAM (FSRAM), and a test-access port (TAP). The functionality of these blocks is described in the following sections.

PCI interface (PCIIF)

The TNETE110 PCIIF contains a byte-aligning DMA controller that allows frames to be fragmented into any byte length and transferred to any byte address while supporting 32-bit data streaming. For multipriority networks it can provide multiple data channels, each with separate lists, commands, and status. Data for the channels is passed to and from the PH by way of circular buffer FIFOs in the SRAM, controlled through FIFO registers. The configuration EEPROM interface (CEI), BIOS ROM/LED driver interface (BRI), configuration and I/O memory registers (CIOREGS), and DMA controller are subblocks of the PCIIF. The features of these subblocks are as follows:

configuration EEPROM interface (CEI)

The CEI provides a means for autoconfiguration of the PCI configuration registers. Certain registers in the PCI configuration space may be loaded using the CEI. Autoconfiguration allows builders of TNETE110-based systems to customize the contents of these registers to identify their own system, rather than using the TI defaults. The EEPROM is read at power up and can then be read from, and written to, under program control.

BIOS ROM/LED driver interface (BRI)

The BRI addresses and reads data from an external BIOS ROM via a multiplexed byte-wide bus. The ROM address/data pins can also be multiplexed to drive external status LEDs.

configuration and I/O memory registers (CIOREGS)

The CIOREGS reside in the configuration space, which is 256 bytes in length. The first 64 bytes of the configuration space is the header region, which is explicitly defined by the PCI standard.

DMA controller (DMAC)

The DMAC is responsible for coordinating TNETE110 requests for mastership of the PCI bus. The DMAC provides byte-aligning DMA control allowing byte-size fragmented frames to be transferred to any byte address while supporting 32-bit data streaming.

protocol handler (PH)

The PH implements the serial protocols of the network. On transmit, it serializes data, adds framing and CRC fields, and interfaces to the network PHY. On receive, it provides address recognition, CRC and error checking, frame disassembly, and deserialization. Data for multiple channels is passed to and from the PH by way of circular buffer FIFOs in the FSRAM controlled through FPREGS.

10 Base-T physical layer (PHY)

The PHY acts as an on-chip front-end providing physical layer functions for both 10 Base-5 (AUI) and 10 Base-T (twisted pair). The PHY provides Manchester encoding/decoding from smart squelch, jabber detection, link pulse detection, autopolarity control, 10 Base-T transmission waveshaping, and antialiasing filtering. Connection to the AUI drop cable for the 10 Base-T twisted pair is made via simple isolation transformers (see Figure 2) and no external filter networks are required. Suitable external termination components allow the use of either shielded or unshielded twisted-pair cable (150 Ω or 100 Ω). Some of the key features of the on-chip PHY are listed below.

- Integrated filters
- 10 Base-T transceiver
- AUI transceiver
- Autopolarity (reverse polarity correction)
- Loopback for twisted pair and AUI
- Full-duplex mode for simultaneous 10 Base-T transmission and reception
- Low power

10 Base-T physical layer (continued)

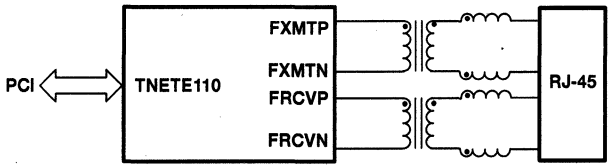


Figure 2. Schematic for 10 Base-T Network Interface Using TNETE110

FIFO pointer registers (FPREGS)

The FPREGS are used to implement circular buffer FIFOs in the SRAM. They are a collection of pointer and counter registers used to maintain the FIFO operation. Both the PCIIF and PH use FPREGS to determine where to read or write data in the SRAM and to determine how much data the FIFO contains.

FIFO SRAM (FSRAM)

The FSRAM is a conventional SRAM array accessed synchronously to the PCI bus clock. Access to the RAM is allocated on a time-division multiplexed (TDM) basis, rather than through a conventional shared bus. This removes the need for bus arbitration and provides guaranteed bandwidth. Half the RAM accesses (every other cycle) are allocated to the PCI controller. It has a 64-bit access port to the RAM, giving it 1 Gbps of bandwidth, sufficient to support 32-bit data streaming on the PCI bus. The PH has one quarter the RAM accesses, and its port may be up to 64 bits wide. A 64-bit port for the PH provides 512 Mbps of bandwidth, more than sufficient for a full-duplex 100-Mbps network. The remaining RAM accesses can be allocated toward providing even more PH bandwidth. The RAM is also accessible (for diagnostic purposes) from the TNETE110 internal data bus. Host DIO (mapped I/O) accesses are used by the host to access internal TNETE110 registers and for adapter test.

- 3.375K bytes of FSRAM
  - 1.5K-byte FIFO for receive channel
  - One 1.5K-byte FIFO for transmit channel
  - Three 128-byte lists

Supporting 1.5K byte of FIFO per channel allows full frame buffering of Ethernet frames.

test-access port (TAP)

Compliant with IEEE Standard 1149.1, the TAP is comprised of five pins that are used to interface serially with the device and the board on which it is installed for boundary-scan testing.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 2) ..... – 0.5 V to 7 V
Input voltage range (see Note 2) ..... – 0.5 V to 7 V
Output voltage range ..... – 0.5 V to 7 V
Power dissipation ..... 2 W
Maximum operating case temperature ..... 95°C
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: Voltage values are with respect to V_{SS}, and all V_{SS} pins should be routed so as to minimize inductance to system ground.

The recommended operating conditions and the electrical characteristics tables are divided into groups, depending on pin function:

- PCI interface pins
- Logic pins
- Physical layer pins

The PCI signal pins may be operated in one of two modes shown in the PCI tables.

- 5-V signal mode
- 3-V signal mode

recommended operating conditions (PCI interface pins) (see Note 3)

			3-V SIGNALING OPERATION			5-V SIGNALING OPERATION			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{DD}	Supply voltage (PCI)		3	3.3	3.6	4.75	5	5.25	V
V_{IH}	High-level input voltage		0.5 × V_{DD}		V_{DD}+0.5	2.0		V_{DD}+0.5	V
V_{IL}	Low-level input voltage, TTL-level signal (see Note 4)		–0.5		0.3 × V_{DD}	–0.5		0.8	V
I_{OH}	High-level output current	TTL outputs			–0.5			–2	mA
I_{OL}	Low-level output current (see Note 5)	TTL outputs			1.5			6	mA
T_A	Operating free-air temperature		0		70	0		70	°C

NOTES: 3. PCI interface pins include V_{DDI}, $\overline{\text{PCLKRUN}}$, $\overline{\text{PFRAME}}$, $\overline{\text{PTRDY}}$, $\overline{\text{PIRDY}}$, $\overline{\text{PSTOP}}$, $\overline{\text{PDEVSEL}}$, PIDSEL, $\overline{\text{PPERR}}$, $\overline{\text{PSERR}}$, $\overline{\text{PREQ}}$, $\overline{\text{PGNT}}$, PCLK, PPAR, $\overline{\text{PRST}}$, $\overline{\text{PINTA}}$, PAD[0–31], PC/$\overline{\text{BE}}$[0–3], $\overline{\text{TRST}}$, TMS, TCLK, TDO, TDI.

4. The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used for logic-voltage levels only.

5. Output current of 2 mA is sufficient to drive five low-power Schottky TTL loads or ten advanced low-power Schottky TTL loads (worst case).

ADVANCE INFORMATION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (PCI interface pins)

PARAMETER		TEST CONDITIONS†		3-V SIGNALING OPERATION		5-V SIGNALING OPERATION		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage, TTL-level signal (see Note 6)	V_{DD} = MIN,	I_{OH} = MAX	0.9 × V_{DD}		2.4		V
V_{OL}	Low-level output voltage, TTL-level signal	V_{DD} = MAX,	I_{OL} = MAX		0.1 × V_{DD}		0.5	V
I_{OZ}	High-impedance output current	V_{DD} = MAX,	V_O = 0 V		10		10	µA
		V_{DD} = MAX,	V_O = V_{DD}		−10		− 10	
I_I	Input current, any input or input/output	V_I = V_{SS} to V_{DD}			± 10		± 70	µA
I_{DD}	Supply current	V_{DD} = MAX			50		60	mA
C_i	Input capacitance, any input	f = 1 MHz,	Others at 0 V		10		10	pF
C_O	Output capacitance, any output or input/output	f = 1 MHz,	Others at 0 V		10		10	pF

† For conditions shown as MIN/MAX, use the appropriate value specified under the recommended operating conditions.
NOTE 6: The following signals require an external pullup resistor: $\overline{PSERR}$, $\overline{PINTA}$.

recommended operating conditions (logic pins) (see Note 7)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage (5 V only)		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		V_{DD}+0.3	V
V_{IL}	Low-level input voltage, TTL-level signal (see Note 4)		−0.3		0.8	V
I_{OH}	High-level output current	TTL outputs			−4	mA
I_{OL}	Low-level output current (see Note 5)	TTL outputs			4	mA
T_A	Operating free-air temperature		0		70	°C

NOTES: 4. The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used for logic-voltage levels only.
5. Output current of 2 mA is sufficient to drive five low-power Schottky TTL loads or ten advanced low-power Schottky TTL loads (worst case).
7. Logic pins include V_{DDL}, EAD[0–7], EXLE, EALE, $\overline{EOE}$, EDCLK, EDIO.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (logic pins)

PARAMETER		TEST CONDITIONS†		MIN	MAX	UNIT
V_{OH}	High-level output voltage, TTL-level signal	V_{DD} = MIN,	I_{OH} = MAX	2.4		V
V_{OL}	Low-level output voltage, TTL-level signal	V_{DD} = MAX,	I_{OL} = MAX		0.5	V
I_O	High-impedance output current	V_{DD} = MIN,	V_O = V_{DD}		10	µA
		V_{DD} = MIN,	V_O = 0 V		−10	
I_I	Input current	V_I = V_{SS} to V_{DD}			±1	µA
I_{DD}	Supply current	V_{DD} = MAX			400	mA
C_i	Input capacitance, any input	f = 1 MHz,	Others at 0 V		10	pF
C_o	Output capacitance, any output or input/output	f = 1 MHz,	Others at 0 V		10	pF

† For conditions shown as MIN/MAX, use the appropriate value specified under the recommended operating conditions.

recommended operating conditions (physical layer pins) (see Note 8)

PARAMETER		JEDEC SYMBOL	MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.75	5	5.25	V
V_B	Receiver input bias voltage (see Note 9)	V_{IB}	$V_{SB}-1$		$V_{SB}+1$	V
T_A	Operating free-air temperature		0		70	°C

NOTES: 8. Physical layer pins include V_{DDOSC}, V_{DDR}, V_{DDT}, V_{DDVCO}, ACOLN, ACOLP, ARCVN, ARCVP, AXMTP, AXMTN, FATEST, FIREF, FRCVN, FRCVP, FXTL1, FXTL2, FXMTP, and FXMTN.

9. V_{SB} is the self-bias voltage of the input pairs ARCVP and ARCVN, ACOLP and ACOLN, and FRCVP and FRCVN. It is defined as $V_{SB} = (V_{SB+} + V_{SB-}) + 2$ (where V_{SB+} is the self-bias voltage of the positive receive pins; V_{SB-} is the self-bias voltage of the negative receive pins). The self-bias voltage of both pins is approximately $V_{DD} + 2$.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (physical interface pins)

10 Base-T receiver input (FRCVP, FRCVN)

PARAMETER		JEDEC SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
$V_{(CM)}$	Common-mode input voltage	V_{IC}		1.8	3.2	V
$V_{I(DIFF)}$	Differential input voltage	V_{ID}		0.6	2.8	V
$I_{(CM)}$	Common-mode current	I_{IC}			4	mA
V_{SQ+}	Rising input pair squelch threshold		$V_{CM} = V_{SB}$, See Note 10	270		mV
V_{SQ-}	Falling input pair squelch threshold		$V_{CM} = V_{SB}$, See Note 10	−270		mV

NOTE 10: V_{SB} is the self-bias of the input FRCVP and FRCVN.

10 Base-T transmitter drive characteristics (FXMTP, FXMTN)

PARAMETER		JEDEC SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
$V_{O(DIFF)NWAV}$	Differential output voltage, transmit waveshaping inactive	$V_{OD(NWAV)}$			±1.77	V
$V_{O(DIFF)WAV}$	Differential uncompensated signal amplitude, waveshaping active	$V_{OD(WAV)}$			±1.253	V
V_{SLW}	Differential voltage at specified slew rate	$V_{OD(SLEW)}$		±2.2	±2.8	V
$V_{O(CM)}$	Common-mode output voltage	V_{OC}	See Figure 3d	0	4	V
$V_{O(DIFF)}$	Differential output voltage	V_{OD}	Into open circuit		5.25	V
$V_{O(I)}$	Output idle differential voltage	$V_{OD(IDLE)}$			±50	mV
$I_{O(I)}$	Output idle differential current	$I_{OD(IDLE)}$			±0.5	mA
$I_{O(FC)}$	Output current, fault condition	$I_{O(FC)}$			300	µA

ADVANCE INFORMATION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (physical interface pins) (continued)

AUI receiver input (ARCVP, ARCVN, ACOLP, ACOLN)

PARAMETER			JEDEC SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
$V_{(CM1)}$	Common-mode input voltage 1		$V_{IC(1)}$	dc + ac, See Note 11	1	4.2	V
$V_{(CM2)}$	Common-mode input voltage 2		$V_{IC(2)}$	dc + ac, See Note 11	1	2.5	V
$V_{I(DIFF)1}$	Differential input voltage 1		$V_{ID(1)}$	See Note 12	0	3	V
$V_{I(DIFF)2}$	Differential input voltage 2		$V_{ID(2)}$	See Note 13	0	100	mV
$I_{(CM)}$	Common-mode current		I_{IC}	See Note 14		1	mA
I_{IFC}	Input current, fault condition		$I_{I(FC)}$			10	mA
$V_{(SQ)}$	Input squelch threshold	To activate		See Note 15, 20 ns < X < 35 ns	−325	−175	mV
		Not to activate			−175	0	mV

NOTES: 11. This parameter means the composite ac signal plus the dc common-mode voltage shall not exceed the indicated limits. These limits are peak maximum values and are not to be exceeded.
12. Common-mode frequency range – 10 Hz to 40 kHz
13. Common-mode frequency range – 40 kHz to 10 MHz
14. Input bias over the common mode dc voltage range
15. This parameter is a range that is allowed to vary over operating conditions. The reference point for the timing period is from the input pair reaching −175 mV on the falling edge to reaching −175 mV on the rising edge.

AUI transmitter drive characteristics (AXMTP, AXMTN)

PARAMETER		JEDEC SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
$V_{O(DIFF)1}$	Differential output voltage	$V_{OD(1)}$	See Note 16	±500	±1315	mV
$V_{O(CM)}$	Common-mode output voltage	V_{OC}	See Figure 3b	1	4.2	V_{DC}
$V_{OI(DIFF)}$	Output idle differential voltage	$V_{OD(IDLE)}$			±40	mV
$I_{OI(DIFF)}$	Output idle differential current	$I_{OD(IDLE)}$			4	mA
$V_{OI(DIFF)U}$	Output differential undershoot	$V_{OD(IDLE)U}$			100	mV
$V_{O(DIFF)2}$	Output differential voltage into an open circuit	$V_{OD(2)}$	Into open circuit		5	V
$I_{O(FC)}$	Output current, fault condition	$I_{O(FC)}$			150	mA

NOTE 16: The differential voltage is measured across a pair of 39-Ω, ±1% resistors bypassed to signal ground with a 0.01-μF capacitor.

PLL characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{FILT}	Reference PLL operating filter voltage	$t_{c(FXTL1)}$ = 50 ns	0.8	2	V

crystal oscillator characteristics

PARAMETER		JEDEC SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
$V_{SB(FXTL1)}$	Input self-bias voltage	V_{IB}		0.8	2	V
$I_{OH(FXTL2)}$	High-level output current	I_{OH}	$V_{(FXTL2)} = V_{SB(FXTL1)}$ $V_{(FXTL1)} = V_{SB(FXTL1)} + 0.5\,V$	−3.5	−6.5	mA
$I_{OL(FXTL2)}$	Low-level output current	I_{OL}	$V_{(FXTL2)} = V_{SB(FXTL1)}$ $V_{(FXTL1)} = V_{SB(FXTL1)} - 0.5\,V$	0.7	1.3	mA

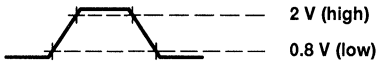
ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

Outputs are driven to a minimum high-logic level of 2.4 V and to a maximum low-logic level of 0.6 V. These levels are compatible with TTL devices.

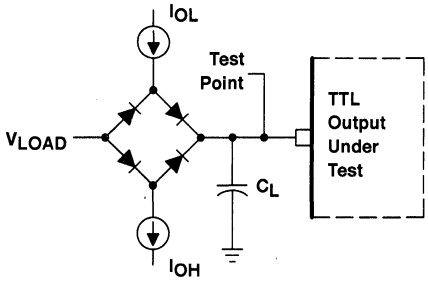
Output transition times are specified as follows: For a high-to-low transition on either an input or output signal, the level at which the signal is said to be no longer high is 2 V and the level at which the signal is said to be low is 0.8 V. For a low-to-high transition, the level at which the signal is said to be no longer low is 0.8 V and the level at which the signal is said to be high is 2 V, as shown below.

The rise and fall times are not specified but are assumed to be those of standard TTL devices, which are typically 1.5 ns.

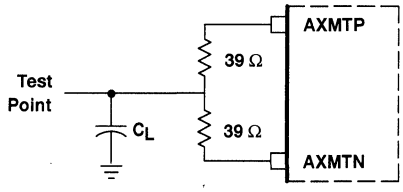


test measurement

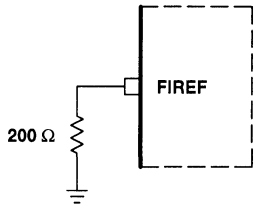
The test-load circuit shown in Figure 3 represents the programmable load of the tester pin electronics that are used to verify timing parameters of the TNETE110 output signals.



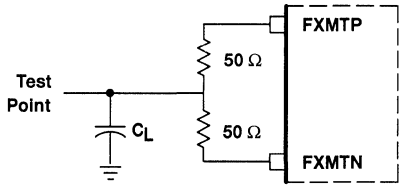
(a) TTL OUTPUT TEST LOAD



(b) AXMTP AND AXMTN TEST LOAD



(c) FIREF TEST CIRCUIT



(d) FXMTP AND FXMTN TEST LOAD

Where: I_{OL} = Refer to I_{OL} in recommended operating conditions
I_{OH} = Refer to I_{OH} in recommended operating conditions
V_{LOAD} = 1.5 V, typical dc-level verification or
0.7 V, typical timing verification
C_L = 18 pF, typical load-circuit capacitance

Figure 3. Test and Load Circuit

ADVANCE INFORMATION

PCI 5-V and 3.3-V switching characteristics (see Note 17 and Figure 4)

PARAMETER		MIN	MAX	UNIT
t_{VAL}	Delay time, PCLK to bused signals valid (see Notes 18 and 19)	2	11	ns
$t_{VAL(PTP)}$	Delay time, PCLK to bused signals valid point-to-point (see Notes 18 and 19)	2	12	ns
t_{on}	Float to active delay	2		ns
t_{off}	Active to float delay		28	ns

NOTES: 17. Some of the timing symbols in this table are not currently listed with EIA or JEDEC standards for semiconductor symbology but are consistent with the PCI Local-Bus Specification, Revision 2.0.
18. Minimum times are measured with a 0-pF equivalent load; maximum times are measured with a 50-pF equivalent load. Actual test capacitance may vary, but results should be correlated to these specifications.
19. $\overline{\text{PREQ}}$ and $\overline{\text{PGNT}}$ are point-to-point signals, and have different output valid delay and input setup times than do bused signals. $\overline{\text{PGNT}}$ has a setup time of 10 ns; $\overline{\text{PREQ}}$ has a setup time of 12 ns. All other signals are bused.

PCI 5-V and 3.3-V timing requirements (see Note 17 and Figure 4)

PARAMETER		MIN	MAX	UNIT
t_{su}	Setup time, bused signals valid to PCLK (see Note 19)	7		ns
$t_{su(PTP)}$	Setup time to PCLK—point-to-point (see Note 19)	10, 12		ns
t_h	Input hold time from PCLK	0		ns
t_c	Cycle time, PCLK (see Note 20)	30	500	ns
$t_{w(H)}$	Pulse duration, PCLK high	12		ns
$t_{w(L)}$	Pulse duration, PCLK low	12		ns
t_{slew}	Slew rate, PCLK (see Note 21)	1	4	V/ns

NOTES: 17. Some of the timing symbols in this table are not currently listed with EIA or JEDEC standards for semiconductor symbology but are consistent with the PCI Local-Bus Specification, Revision 2.0.
19. $\overline{\text{PREQ}}$ and $\overline{\text{PGNT}}$ are point-to-point signals, and have different output valid delay and input setup times than do bused signals. $\overline{\text{PGNT}}$ has a setup time of 10 ns; $\overline{\text{PREQ}}$ has a setup time of 12 ns. All other signals are bused.
20. As a requirement for frame transmission/reception, the minimum PCLK frequency varies with network speed. The clock may only be stopped in a low state.
21. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform.

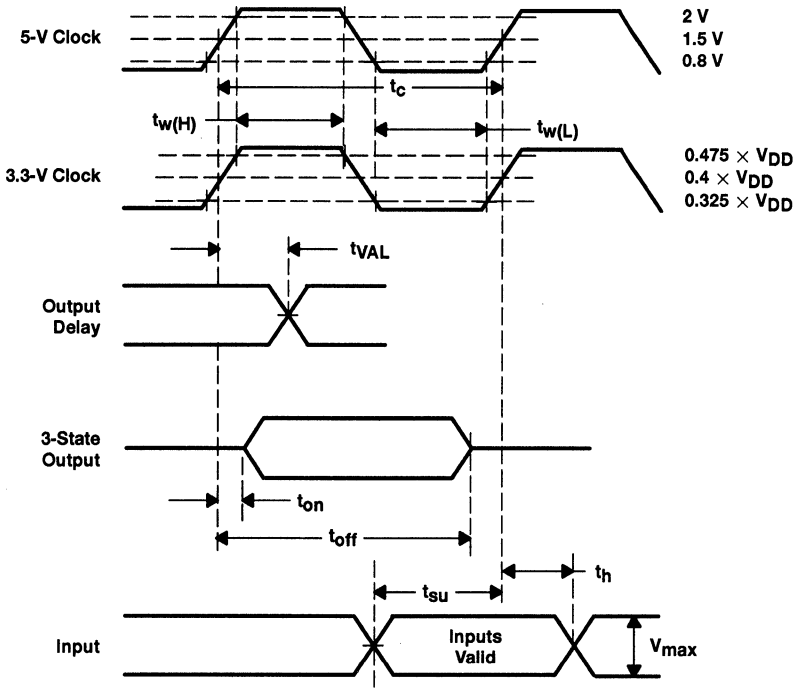


Figure 4. PCI 5-V and 3.3-V Timing

ADVANCE INFORMATION

BIOS ROM and LED interface timing requirements (see Figure 5)†

		MIN	MAX	UNIT
t_{su}	Setup time, data		250	ns
t_h	Hold time, data	0		ns

BIOS ROM and LED interface switching characteristics (see Figure 5)†

PARAMETER		MIN	MAX	UNIT
$t_{d(EADV-EXLEL)}$	Delay time, address high byte valid to EXLE low (address high byte setup time for external latch)	0		ns
$t_{d(EXLEL-EADZ)}$	Delay time, EXLE low to address high byte invalid (address high byte hold time for external latch)	10		ns
$t_{d(EADV-EALEL)}$	Delay time, address low byte valid to EALE low (address low byte setup time for external latch)	0		ns
$t_{d(EALEL-EADZ)}$	Delay time, EALE low to address low byte invalid (address low byte hold time for external latch)	10		ns
t_a	Access time, address	288		ns

† The EPROM interface, consisting of 11 pins, requires only two TTL '373 latches to latch the high and low addresses.

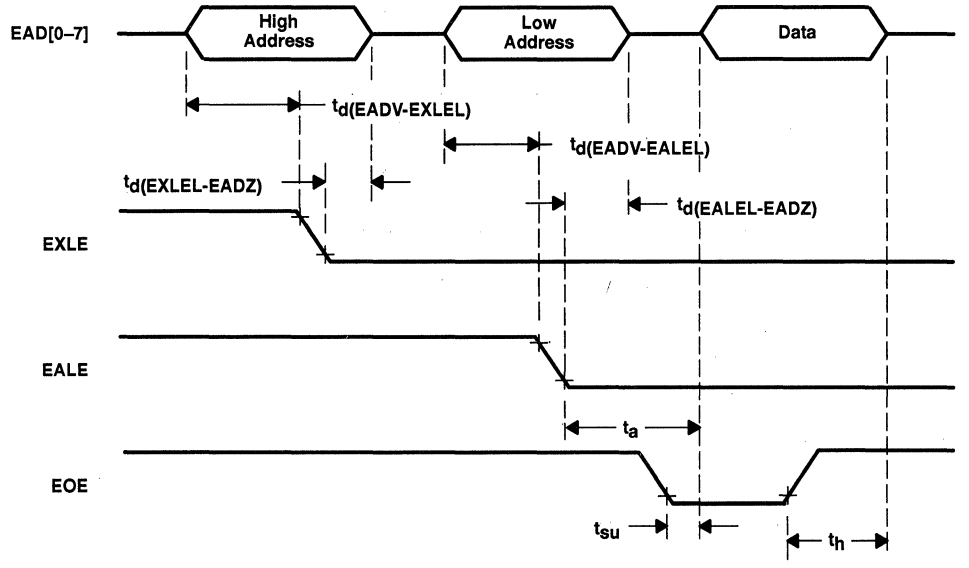


Figure 5. BIOS ROM and LED Interface Timing

ADVANCE INFORMATION

configuration EEPROM interface switching characteristics (see Figure 6)

PARAMETER		MIN	MAX	UNIT
$f_{CLK(EDCLK)}$	Clock frequency, EDCLK	0	100	kHz
$t_{d(EDCLKL-EDIOV)}$	EDCLK low to EDIO data in valid	0.3	3.5	µs
$t_{d(EDIO\ free)}$	Time the bus must be free before a new transmission can start	4.7		µs
$t_{d(EDIOV-EDCLKL)}$	Delay time, EDIO valid after EDCLK low (start condition hold time for EEPROM)	4		µs
$t_{w(L)}$	Low period, clock	4.7		µs
$t_{w(H)}$	High period, clock	4		µs
$t_{d(EDCLKH-EDIOV)}$	Delay time, EDCLK high to EDIO valid (start condition setup time)	4.7		µs
$t_{d(EDCLKL-EDIOX)}$	Delay time, EDCLK low to EDIO changing (data out hold time)	0		µs
$t_{d(EDIOV-EDCLKH)}$	Delay time, EDIO valid to EDCLK high (data out setup time)	250		ns
t_r	Rise time, EDIO and EDCLK		1	µs
t_f	Fall time, EDIO and EDCLK		300	ns
$t_{d(EDCLKH-EDIOH)}$	Delay time, EDCLK high to EDIO high (stop condition setup time)	4.7		µs
$t_{d(EDCLKL-EDIOX)}$	Delay time, EDCLK low to EDIO changing (data in hold time)	300		ns

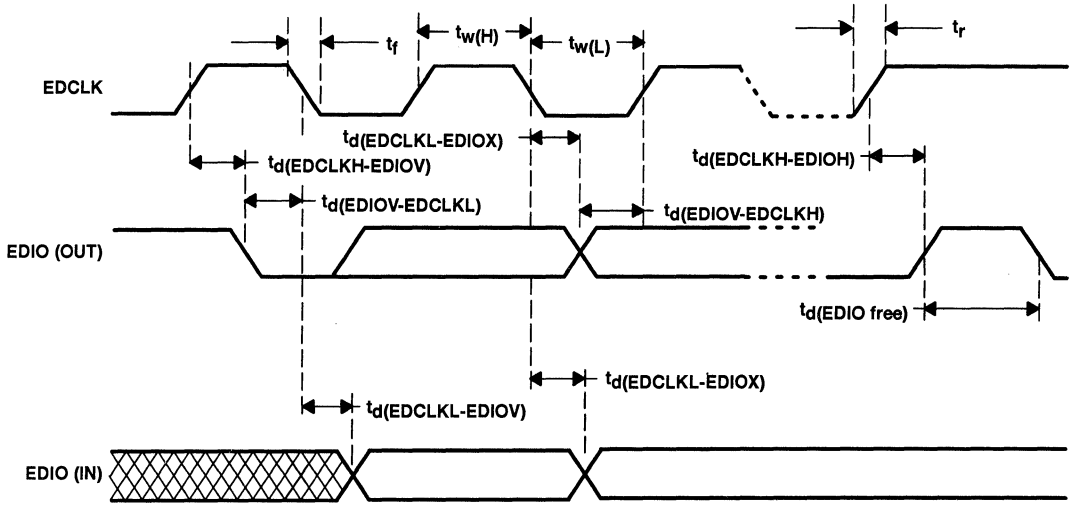


Figure 6. Configuration EEPROM Interface Timing

ADVANCE INFORMATION

crystal oscillator timing requirements (see Figure 7)†

		MIN	TYP	MAX	UNIT
$t_{d(VDDH-FXTL1V)}$	Delay time from minimum V_{DD} high level to first valid FXTL1V full swing period (see Note 22)			100	ms
$t_{w(H)}$	Pulse duration at FXTL1 high	13			ns
$t_{w(L)}$	Pulse duration at FXTL1 low	13			ns
t_t	Transition time of FXTL1		7		ns
t_c	Cycle time, FXTL1		50		ns
	Tolerance of FXTL1 input frequency		±0.01		%

† The FXTL signal may be implemented by either connecting a 20-MHz crystal across the FXTL1 and FXTL2 pins or by driving the FXTL1 from a 20-MHz crystal oscillator module.

NOTE 22: This specification is provided as an aid to board design. This specification is not guaranteed during manufacturing testing.

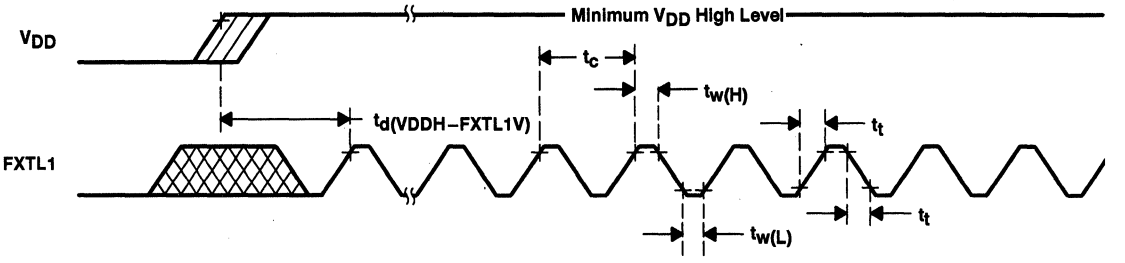


Figure 7. Crystal Oscillator Timing

Contents

- IEEE 802.5 and IBM Token-Ring Network™ Compatible
- Compatible With TI380FPA FNL PacketBlaster™
- Token-Ring Features
  - 16- or 4-Megabit-per-Second Data Rates
  - Supports up to 18K-Byte Frame Size (16-Mbps Operation Only)
  - Supports Universal-and Local-Network Addressing
  - Early Token-Release Option (16-Mbps Operation Only)
  - Compatible With the TMS38054
- Expandable Local LAN-Subsystem Memory Space up to 2 Megabytes
- Glueless Interface to DRAMs
- High-Performance 16-Bit CPU for Communications-Protocol Processing
- 1- to 16.5-Megabyte-per-Second High-Speed Bus Master DMA Interface
- Low-Cost Host-Slave I/O Interface Option
- Up to 32-Bit Host Address Bus
- Selectable Host System-Bus Options
- Adapter Local-Bus Speed Is Switchable Between 4 MHz and 6 MHz
- 80x8x or 68xxx-Type Bus and Memory Organization
  - 8- or 16-Bit Data Bus on 80x8x Buses
  - Optional Parity Checking
- Dual-Port DMA and Direct I/O Transfers to Host Bus
- Supports 8- or 16-Bit Pseudo-DMA Operation
- Enhanced-Address-Copy-Option (EACO) Interface Supports External Address-Checking Logic for Bridging or External Custom Applications
- Support for Module High-Impedance In-Circuit Testing
- Built-In Real-Time Error Detection
- Bring-Up and Self-Test Diagnostics With Loopback
- Automatic Frame-Buffer Management
- 2- to 33-MHz System-Bus Clock
- Slow-Clock Low-Power Mode
- Single 5-V Supply
- 0.8-μm CMOS Technology
- 250-mA Typical Latch-Up Immunity at 25°C
- ESD Protection Exceeds 2000 V
- 144-Pin Plastic Thin Quad Flat Package (PGE Suffix)
- Operating Temperature Range 0°C to 70°C

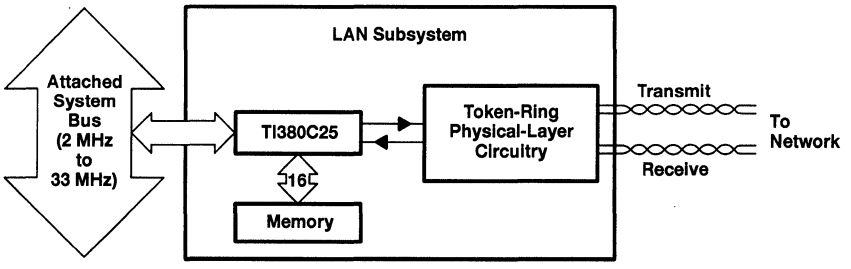


Figure 1. Network-Commprocessor Applications Diagram

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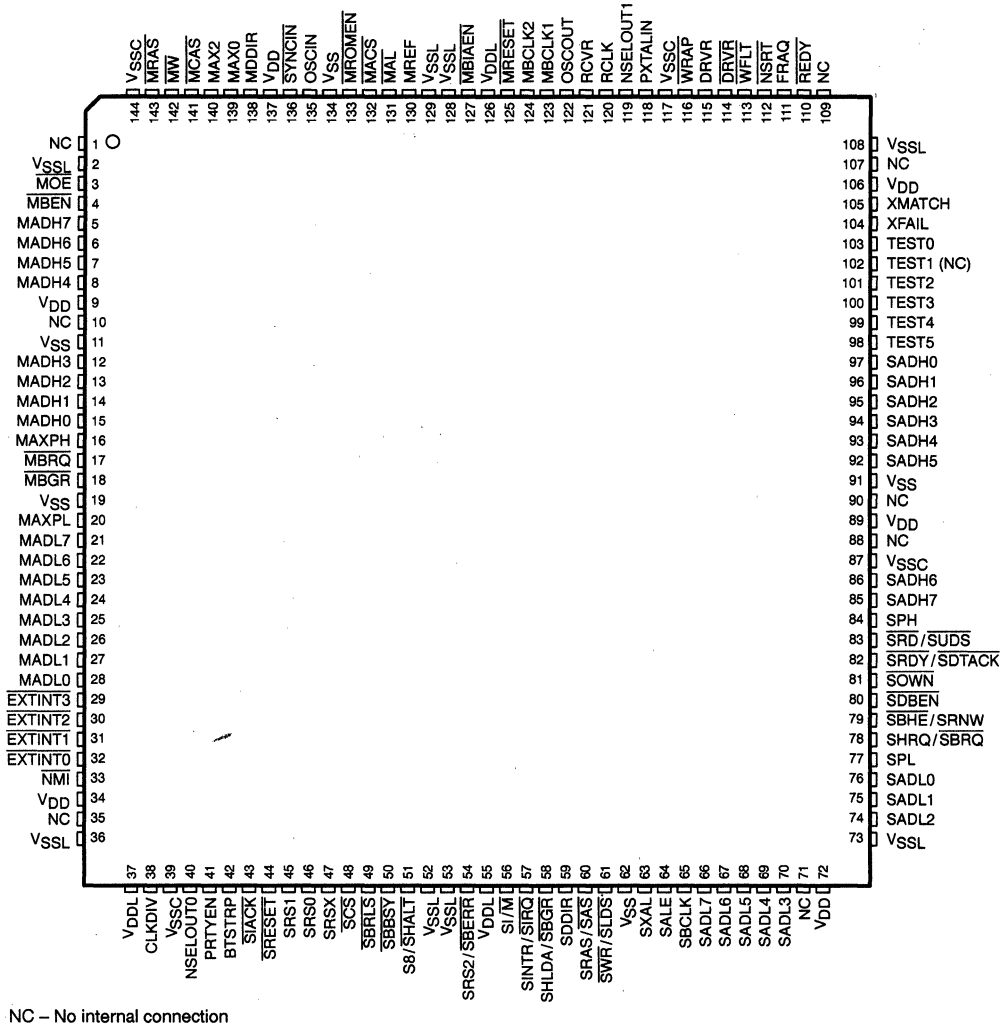
PacketBlaster is a trademark of Texas Instruments Incorporated.

pin assignments

PGE PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TI380C25 is a single-chip network-communications processor (commprocessor) that supports token-ring local area networks (LANs) at data rates of 16 Mbps or 4 Mbps. The TI380C25 conforms to ISO 8802–5/IEEE 802.5–1992 standards and has been verified to be completely IBM Token-Ring Network compatible. By integrating the essential control building blocks needed on a LAN-subsystem card into one device, the TI380C25 ensures that this IBM compatibility is maintained in silicon.

The high degree of integration of the TI380C25 makes it a virtual LAN subsystem on a single chip. Protocol handling, host-system interfacing, memory interfacing, and communications processing are all provided through the TI380C25. To complete LAN-subsystem design, only the network-interface hardware, local memory, and minimal additional components such as PAL® devices and crystal oscillators need to be added.

The TI380C25 provides a 32-bit system-memory address reach with a high-speed bus-master DMA interface that supports rapid communications with the host system. In addition, the TI380C25 supports direct I/O and a low-cost 8- or 16-bit pseudo-DMA interface that requires only a chip select to work directly on an 80x8x 8-bit slave I/O interface. Finally, selectable 80x8x or 68xxx-type host-system bus and memory organization add to design flexibility.

The TI380C25 supports addressing for up to 2M bytes of local memory. This expanded memory capacity can improve LAN-subsystem performance by allowing larger blocks of information to be transferred at one time and minimizing the frequency of host LAN-subsystem communications. The support of large local memory is important in applications that require large data transfers (such as graphics or database transfers) and in heavily loaded networks where the extra memory can provide data buffers to store data until it can be processed by the host.

The proprietary CPU used in the TI380C25 allows protocol software to be downloaded into RAM or stored in ROM in the local-memory space. By moving protocols (such as LLC) to the LAN-subsystem, overall system performance is increased. This is accomplished by offloading the processing from the host system to the TI380C25, which can also reduce LAN-subsystem-to-host communications. As other protocol software is developed, greater differentiation of end products with enhanced system performance is possible.

In addition, the TI380C25 includes hardware counters that provide real-time error detection and automatic frame-buffer management. These counters control system-bus retries and burst size, and track host and LAN-subsystem buffer status. Previously, these counters needed to be maintained in software. Integrating them into hardware removes software overhead and improves LAN-subsystem performance.

The TI380C25 implements a TI-patented enhanced-address-copy-option (EACO) interface. This interface supports external address-checking devices, such as the TMS380SRA source-routing accelerator. The TI380C25 has a 128-word external I/O space in its memory to support external address-checker devices and other hardware extensions to the TMS380 architecture.

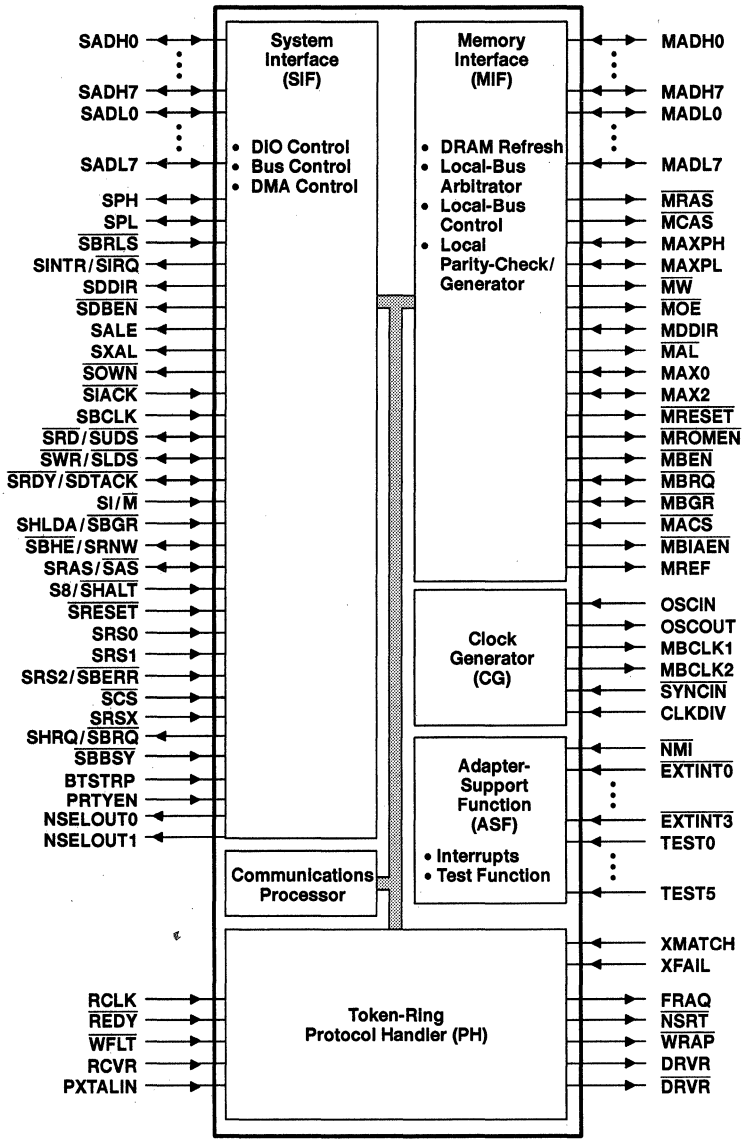
The major blocks of the TI380C25 include the communications processor (CP), the system interface (SIF), the memory interface (MIF), the protocol handler (PH), the clock generator (CG), and the adapter-support function (ASF), as shown in the functional block diagram.

The TI380C25 is available in a 144-pin plastic thin quad flat package (PGE suffix) and is characterized for operation from 0°C to 70°C.

The TI380C25 has a bus interface to the host system, a bus interface to local memory, and an interface to the physical-layer circuitry. Pin names starting with the letter S attach to the host-system bus, and pin names starting with the letter M attach to the local-memory bus.

PAL® is a registered trademark of Advanced Micro Devices, Inc. Other companies also manufacture programmable array logic devices.

functional block diagram



Pin Functions

PIN NAME	PIN NO.	I/O†	DESCRIPTION
BTSTRP	42	I	Bootstrap. The value on BTSTRP is loaded into the BOOT bit of the SIFACL register at reset (i.e., when $\overline{\text{SRESET}}$ is asserted or the $\overline{\text{ARESET}}$ bit in the SIFACL register is set) to form a default value. BTSTRP indicates whether chapters 0 and 31 of the memory map are RAM or ROM. If these chapters are RAM, the TI380C25 is denied access to the local-memory bus until the CPHALT bit in the SIFACL register is cleared. H = Chapters 0 and 31 of local memory are RAM based (see Note 1). L = Chapters 0 and 31 of local memory are ROM based.
CLKDIV	38	I	Clock divider select (see Note 2) H = 64-MHz OSCIN for 4-MHz local bus L = 32-MHz OSCIN for 4-MHz local bus or 48-MHz OSCIN for 6-MHz local bus
$\overline{\text{EXTINT0}}$ $\overline{\text{EXTINT1}}$ $\overline{\text{EXTINT2}}$ $\overline{\text{EXTINT3}}$	32 31 30 29	I/O	Reserved; must be pulled high (see Note 3)
$\overline{\text{MACS}}$	132	I	Reserved; must be tied low (see Note 4)
MADH0 MADH1 MADH2 MADH3 MADH4 MADH5 MADH6 MADH7	15 14 13 12 8 7 6 5	I/O	Local-memory address, data, and status bus — high byte. For the first quarter of the local-memory cycle, these bus lines carry address bits AX4 and A0 to A6; for the second quarter, they carry status bits; and for the third and fourth quarters, they carry data bits 0 to 7. The most significant bit is MADH0 and the least significant bit is MADH7. Memory Cycle 1Q: Signal = AX4, A0–A6 2Q: Signal = Status 3Q: Signal = D0–D7 4Q: Signal = D0–D7
MADL0 MADL1 MADL2 MADL3 MADL4 MADL5 MADL6 MADL7	28 27 26 25 24 23 22 21	I/O	Local-memory address, data, and status bus — low byte. For the first quarter of the local-memory cycle, these bus lines carry address bits A7 to A14; for the second quarter, they carry address bits AX4 and A0 to A6; and for the third and fourth quarters, they carry data bits 8 to 15. The most significant bit is MADL0 and the least significant bit is MADL7. Memory Cycle 1Q: Signal = A7–A14 2Q: Signal = AX4, A0–A6 3Q: Signal = D8–D15 4Q: Signal = D8–D15
$\overline{\text{MAL}}$	131	O	Memory-address latch. $\overline{\text{MAL}}$ is a strobe signal for sampling the address at the start of the memory cycle; it is used by SRAMs and EPROMs. The full 20-bit word address is valid on MAX0, MAXPH, MAX2, MAXPL, MADH0–MADH7, and MADL0–MADL7. Three 8-bit transparent latches can be used to retain a 20-bit static address throughout the cycle. Rising edge = No signal latching Falling edge = Allows the above address signals to be latched
MAX0	139	I/O	Local-memory-extended address bit. MAX0 drives AX0 at row-address time and drives A12 at column-address and data-valid times for all cycles. This signal can be latched by $\overline{\text{MRAS}}$. Driving A12 eases interfacing to a BIA ROM. Memory Cycle 1Q: Signal = AX0 2Q: Signal = A12 3Q: Signal = A12 4Q: Signal = A12

† I = input, O = output

NOTES: 1. Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).
2. The TI380FPA and TMS380SRA are currently supported only with the 4-MHz local bus in either CLKDIV state. Expansion to support the 6-MHz local bus is under development.
3. Each pin must be individually tied to V_{CC} with a 1-kΩ pullup resistor.
4. Pin should be connected to ground.

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O†	DESCRIPTION
MAX2	140	I/O	Local-memory-extended address bit. MAX2 drives AX2 at row-address time, which can be latched by $\overline{MRAS}$ and A14 at column-address and data-valid times for all cycles. Driving A14 eases interfacing to a BIA ROM. Memory Cycle 1Q 2Q 3Q 4Q Signal AX2 A14 A14 A14
MAXPH	16	I/O	Local-memory-extended address and parity — high byte. For the first quarter of a memory cycle, MAXPH carries the extended-address bit AX1; for the second quarter of a memory cycle, it carries the extended-address bit AX0; and for the last half of the memory cycle, it carries the parity bit for the high data byte. Memory Cycle 1Q 2Q 3Q 4Q Signal AX1 AX0 Parity Parity
MAXPL	20	I/O	Local-memory-extended address and parity — low byte. For the first quarter of a memory cycle, MAXPL carries the extended-address bit AX3; for the second quarter of a memory cycle, it carries extended-address bit AX2; and for the last half of the memory cycle, it carries the parity bit for the low data byte. Memory Cycle 1Q 2Q 3Q 4Q Signal AX3 AX2 Parity Parity
MBCLK1 MBCLK2	123 124	O	Local-bus clock 1 and local-bus clock 2. MBCLK1 and MBCLK2 are referenced for all local-bus transfers. MBCLK2 lags MBCLK1 by a quarter of a cycle. These clocks operate according to: MBCLK[1:2] OSCIN CLKDIV 8 MHz 64 MHz H 8 MHz 32 MHz L 12 MHz 48 MHz L
$\overline{MBEN}$	4	O	Buffer enable. $\overline{MBEN}$ enables the bidirectional buffer outputs on the MADH, MAXPH, MAXPL, and MADL buses during the data phase. $\overline{MBEN}$ is used in conjunction with MDDIR, which selects the buffer output direction. H = Buffer output disabled L = Buffer output enabled
$\overline{MBGR}$	18	I/O	Reserved; must be left unconnected.
$\overline{MBIAEN}$	127	O	Burned-in address enable. $\overline{MBIAEN}$ is an output signal used to provide an output enable for the ROM containing the adapter's burned-in address (BIA). H = $\overline{MBIAEN}$ is driven high for any write accesses to the addresses between >00.0000 and >00.000F, or any accesses (read/write) to any other address. L = $\overline{MBIAEN}$ is driven low for any read from addresses between >00.0000 and >00.000F.
$\overline{MBRQ}$	17	I/O	Reserved; must be pulled high (see Note 3).

† I = input, O = output

NOTE 3: Each pin must be individually tied to V_{CC} with a 1-kΩ pullup resistor.

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O†	DESCRIPTION
$\overline{\text{MCAS}}$	141	O	Column-address strobe for DRAMs. The column address is valid for the 3/16 of the memory cycle following the row-address portion of the cycle. $\overline{\text{MCAS}}$ is driven low every memory cycle while the column address is valid on MADL0–MADL7, MAXPH, and MAXPL, except when one of the following conditions occurs: 1) When the address accessed is in the BIA ROM (>00.0000 – >00.000F) 2) When the address accessed is in the EPROM memory map (i.e., when the BOOT bit in the SIFACL register is zero and an access is made between >00.0010 – >00.FFFF or >1F.0000 – >1F.FFFF) 3) When the cycle is a refresh cycle, in which case $\overline{\text{MCAS}}$ is driven at the start of the cycle before $\overline{\text{MRAS}}$ (for DRAMs that have $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh). For DRAMs that do not support $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, it may be necessary to disable $\overline{\text{MCAS}}$ with MREF during the refresh cycle.
MDDIR	138	I/O	Data direction. MDDIR is used as a direction control for bidirectional bus drivers. MDDIR becomes valid before $\overline{\text{MBEN}}$ becomes active. H = TI380C25 memory-bus write L = TI380C25 memory-bus read
$\overline{\text{MOE}}$	3	O	Memory output enable. $\overline{\text{MOE}}$ is used to enable the outputs of the DRAM memory during a read cycle. $\overline{\text{MOE}}$ is high for EPROM or BIA ROM read cycles. H = Disable DRAM outputs L = Enable DRAM outputs
$\overline{\text{MRAS}}$	143	O	Row-address strobe for DRAMs. The row address lasts for the first 5/16 of the memory cycle. $\overline{\text{MRAS}}$ is driven low every memory cycle while the row address is valid on MADL0–MADL7, MAXPH, and MAXPL for both RAM and ROM cycles. It is also driven low during refresh cycles when the refresh address is valid on MADL0–MADL7.
MREF	130	O	DRAM refresh cycle in progress. MREF is used to indicate that a DRAM refresh cycle is occurring. It is also used for disabling $\overline{\text{MCAS}}$ to all DRAMs that do not use a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh. H = DRAM refresh cycle in process L = Not a DRAM refresh cycle
$\overline{\text{MRESET}}$	125	O	Memory-bus reset. $\overline{\text{MRESET}}$ is a reset signal generated when either the ARESET bit in the SIFACL register is set or $\overline{\text{SRESET}}$ is asserted. This signal is used for resetting external local-bus glue logic. H = External logic not reset L = External logic reset
$\overline{\text{MROMEN}}$	133	O	ROM enable. During the first 5/16 of the memory cycle, $\overline{\text{MROMEN}}$ is used to provide a chip select for ROMs when the BOOT bit of the SIFACL register is zero (i.e., when code is resident in ROM, not RAM). It can be latched by $\overline{\text{MAL}}$. $\overline{\text{MROMEN}}$ goes low for any read from addresses >00.0010 – >00.FFFF or >1F.0000 – >1F.FFFF when the BOOT bit in the SIFACL register is zero. $\overline{\text{MROMEN}}$ stays high for writes to these addresses, accesses of other addresses, or accesses of any address when the BOOT bit is 1. During the final three quarters of the memory cycle, $\overline{\text{MROMEN}}$ outputs the A13 address signal for interfacing to a BIA ROM. This means $\overline{\text{MBIAEN}}$, MAX0, $\overline{\text{ROMEN}}$, and MAX2 together form a glueless interface for the BIA ROM. H = ROM disabled L = ROM enabled

† I = input, O = output

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O†	DESCRIPTION
$\overline{MW}$	142	O	Local-memory write. $\overline{MW}$ is used to specify a write cycle on the local-memory bus. The data on the MADH0–MADH7 and MADL0–MADL7 buses is valid while $\overline{MW}$ is low. DRAMs latch data on the falling edge of $\overline{MW}$, while SRAMs latch data on the rising edge of $\overline{MW}$. H = Not a local-memory write cycle L = Local-memory write cycle
$\overline{NMI}$	33	I	Nonmaskable interrupt request. NMI must be left unconnected.
OSCIN	135	I	External oscillator input. OSCIN provides the clock frequency to the TI380C25 for a 4-MHz or 6-MHz internal bus (see Notes 5 and 6). CLKDIV OSCIN H 64 MHz for a 4-MHz local bus L 32 MHz for a 4-MHz local bus or 48 MHz for a 6-MHz local bus
OSCOUT	122	O	Oscillator output CLKDIV OSCOUT L OSCIN / 4 (if OSCIN = 32 MHz, OSCOUT = 8 MHz; if OSCIN = 48 MHz, OSCOUT = 12 MHz) H OSCIN/8 (if OSCIN = 64 MHz, OSCOUT = 8 MHz)
PRTYEN	41	I	Parity enable. The value on PRTYEN is loaded into the PEN bit of the SIFACL register at reset (i.e., when $\overline{SRESET}$ is asserted or the ARESET bit in the SIFACL register is set) to form a default value. PRTYEN enables parity checking for the local memory. H = Local-memory data bus checked for parity (see Note 1). L = Local-memory data bus not checked for parity.
NSELOUT0 NSELOUT1	40 119	O O	Network selection outputs. NSELOUT0 and NSELOUT1 are controlled by the host through the corresponding bits of the SIFACL register. The value of these bits/signals can be changed only while the TI380C25 is reset. NSELOUT0 NSELOUT1 DESCRIPTION L H 16-Mbps token ring H H 4-Mbps token ring
SADH0 SADH1 SADH2 SADH3 SADH4 SADH5 SADH6 SADH7	97 96 95 94 93 92 86 85	I/O	System address/data bus—high byte (see Note 1).These lines make up the most significant byte of each address word (32-bit address bus) and data word (16-bit data bus). The most significant bit is SADH0, and the least significant bit is SADH7. Address multiplexing: Bits 31 – 24 and bits 15 – 8 Data multiplexing: Bits 15 – 8
SADL0 SADL1 SADL2 SADL3 SADL4 SADL5 SADL6 SADL7	76 75 74 70 69 68 67 66	I/O	System address/data bus—low byte (see Note 1). These lines make up the least significant byte of each address word (32-bit address bus) and data word (16-bit data bus). The most significant bit is SADL0 and the least significant bit is SADL7. Address multiplexing: Bits 23 – 16 and bits 7 – 0 Data multiplexing: Bits 7 – 0

† I = input, O = output

NOTES: 1. Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).
5. Pin has an expanded input voltage specification.
6. A maximum of two TI380C25 devices can be connected to any one oscillator.

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O†	DESCRIPTION
SALE	64	O	System address-latch enable. SALE is the enable pulse used to externally latch the 16 LSBs of the address from the SADH0 – SADH7 and SADL0 – SADL7 buses at the start of the DMA cycle. Systems that implement address parity can also externally latch the parity bits (SPH and SPL) for the latched address.
$\overline{\text{SBBSY}}$	50	I	System bus busy. The TI380C25 samples the value on $\overline{\text{SBBSY}}$ during arbitration (see Note 1). The sample has one of two values: H = Not busy. The TI380C25 can become bus master if the grant condition is met. L = Busy. The TI380C25 cannot become bus master.
SBCLK	65	I	System bus clock. The TI380C25 requires SBCLK to synchronize its bus timings for all DMA transfers. Valid frequencies are 2 MHz–33 MHz.
SBHE/SRNW	79	I/O	**Intel Mode:** $\overline{\text{SBHE}}$ is used for system byte high enable. $\overline{\text{SBHE}}$ is a 3-state output driven during DMA; it is an input at all other times. H = System byte high not enabled (see Note 1) L = System byte high enabled **Motorola Mode:** SRNW is used for system read not write. SRNW serves as a control signal to indicate a read or write cycle. H = Read cycle (see Note 1) L = Write cycle
$\overline{\text{SBRLS}}$	49	I	System bus release. $\overline{\text{SBRLS}}$ indicates to the TI380C25 that a higher-priority device requires the system bus. The value on $\overline{\text{SBRLS}}$ is ignored when the TI380C25 is not perfoming DMA. $\overline{\text{SBRLS}}$ is internally synchronized to SBCLK. H = The TI380C25 can hold onto the system bus (see Note 1). L = The TI380C25 should release the system bus upon completion of current DMA cycle. If the DMA transfer is not yet complete, the SIF rearbitrates for the system bus.
$\overline{\text{SCS}}$	48	I	System chip select. $\overline{\text{SCS}}$ activates the system interface of the TI380C25 for a DIO read or write. H = Not selected (see Note 1) L = Selected
$\overline{\text{SDBEN}}$	80	O	System data-bus enable. $\overline{\text{SDBEN}}$ signals to the external data buffers to begin driving data. $\overline{\text{SDBEN}}$ is activated during both DIO and DMA. H = Keep external data buffers in the high-impedance state L = Cause external data buffers to begin driving data
SDDIR	59	O	System data direction. SDDIR provides the external data buffers with a signal indicating the direction the data is moving. During DIO writes and DMA reads, SDDIR is low (data direction is into the TI380C25). During DIO reads and DMA writes, SDDIR is high (data direction is out from the TI380C25). When the system interface is not involved in a DIO or DMA operation, SDDIR is high by default. SDDIR: H = DATA DIRECTION output, DIO read, DMA write SDDIR: L = DATA DIRECTION input, DIO write, DMA read

† I = input, O = output

NOTE 1: Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O†	DESCRIPTION	
SHLDA/$\overline{\text{SBGR}}$	58	I	Intel Mode	SHLDA is used for system-hold acknowledge. SHLDA indicates that the system DMA hold request has been acknowledged. It is internally synchronized to SBCLK (see Note 1). H = Hold request acknowledged L = Hold request not acknowledged
			Motorola Mode	$\overline{\text{SBGR}}$ is used for system bus grant. $\overline{\text{SBGR}}$ is an active-low bus grant, as defined in the standard 68xxx interface, and is internally synchronized to SBCLK (see Note 1). H = System bus not granted L = System bus granted
SHRQ/$\overline{\text{SBRQ}}$	78	O	Intel Mode	SHRQ is used for system-hold request. SHRQ is used to request control of the system bus in preparation for a DMA transfer. SHRQ is internally synchronized to SBCLK. H = System bus requested L = System bus not requested
			Motorola Mode	$\overline{\text{SBRQ}}$ is used for system-bus request. SBRQ is used to request control of the system bus in preparation for a DMA transfer. SBRQ is internally synchronized to SBCLK. H = System bus not requested L = System bus requested
$\overline{\text{SIACK}}$	43	I	System-interrupt acknowledge. $\overline{\text{SIACK}}$ is from the host processor to acknowledge the interrupt request from the TI380C25. H = System interrupt not acknowledged (see Note 1) L = System interrupt acknowledged: The TI380C25 places its interrupt vector onto the system bus.	
SI/$\overline{\text{M}}$	56	I	System Intel/Motorola mode select. The value on SI/$\overline{\text{M}}$ specifies the system-interface mode. H = Intel-compatible interface mode selected. Intel interface can be 8-bit or 16-bit mode (see S8/$\overline{\text{SHALT}}$ description and Note 1). L = Motorola-compatible interface mode selected. Motorola interface mode is always 16 bits.	
SINTR/$\overline{\text{SIRQ}}$	57	O	Intel Mode	SINTR is used for system-interrupt request. TI380C25 activates SINTR to signal an interrupt request to the host processor. H = Interrupt request by TI380C25 L = No interrupt request
			Motorola Mode	$\overline{\text{SIRQ}}$ is used for system-interrupt request. TI380C25 activates $\overline{\text{SIRQ}}$ to signal an interrupt request to the host processor. H = No interrupt request L = Interrupt request by TI380C25
$\overline{\text{SOWN}}$	81	O	System bus owned. $\overline{\text{SOWN}}$ indicates to external devices that TI380C25 has control of the system bus. $\overline{\text{SOWN}}$ drives the enable signal of the bus-transceiver chips that drive the address and bus-control signals. H = TI380C25 does not have control of the system bus. L = TI380C25 has control of the system bus.	

† I = input, O = output

NOTE 1: Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O†	DESCRIPTION	
SPH	84	I/O	System parity high. The optional odd-parity bit for each address or data byte transmitted over SADH0–SADH7 (see Note 1).	
SPL	77	I/O	System parity low. The optional odd-parity bit for each address or data byte transmitted over SADL0–SADL7 (see Note 1).	
SRAS/$\overline{\text{SAS}}$	60	I/O	Intel Mode	SRAS is used for system memory-address strobe (see Note 7). SRAS is used to latch the $\overline{\text{SCS}}$ and SRSX – SRS2 register input signals. In a minimum-chip system, SRAS is tied to the SALE output of the system bus. The latching capability can be defeated because the internal latch for these inputs remains transparent as long as SRAS remains high. This permits SRAS to be pulled high and the signals at $\overline{\text{SCS}}$, SRSX – SRS2, and $\overline{\text{SBHE}}$ to be applied independently of the SALE strobe from the system bus. During DMA, SRAS remains an input. H = Transparent mode L = Holds latched values of $\overline{\text{SCS}}$, SRSX–SRS2, and $\overline{\text{SBHE}}$ Falling edge = Latches $\overline{\text{SCS}}$, SRSX – SRS2, and $\overline{\text{SBHE}}$
			Motorola Mode	$\overline{\text{SAS}}$ is used for sytem-memory address strobe (see Note 7). $\overline{\text{SAS}}$ is an active-low address strobe that is an input during DIO (although ignored as an address strobe) and an output during DMA. H = Address is not valid. L = Address is valid and a transfer operation is in progress.
$\overline{\text{SRD}}$/$\overline{\text{SUDS}}$	83	I/O	Intel Mode	$\overline{\text{SRD}}$ is used for system-read strobe (see Note 7). $\overline{\text{SRD}}$ is the active-low strobe indicating that a read cycle is performed on the system bus. $\overline{\text{SRD}}$ is an input during DIO and an output during DMA. H = Read cycle is not occurring. L = If DMA, host provides data to system bus. If DIO, SIF provides data to system bus.
			Motorola Mode	$\overline{\text{SUDS}}$ is used for upper-data strobe (see Note 7). $\overline{\text{SUDS}}$ is the active-low upper-data strobe. $\overline{\text{SUDS}}$ is an input during DIO and an output during DMA. H = Not valid data on SADH0–SADH7 lines L = Valid data on SADH0–SADH7 lines
$\overline{\text{SRDY}}$/$\overline{\text{SDTACK}}$	82	I/O	Intel Mode	$\overline{\text{SRDY}}$ is used for system bus ready (see Note 7). $\overline{\text{SRDY}}$ indicates to the bus master that a data transfer is complete. $\overline{\text{SRDY}}$ is asynchronous but during DMA and pseudo-DMA cycles, it is internally synchronized to SBCLK. During DMA cycles, $\overline{\text{SRDY}}$ must be asserted before the falling edge of SBCLK in state T2 to prevent a wait state. $\overline{\text{SRDY}}$ is an output when the TI380C25 is selected for DIO; otherwise; it is an input. H = System bus is not ready. L = Data transfer is complete; system bus is ready.
			Motorola Mode	$\overline{\text{SDTACK}}$ is used for system data-transfer acknowledge (see Note 7). The purpose of $\overline{\text{SDTACK}}$ is to indicate to the bus master that a data transfer is complete. $\overline{\text{SDTACK}}$ is internally synchronized to SBCLK. During DMA cycles, $\overline{\text{SDTACK}}$ must be asserted before the falling edge of SBCLK in state T2 in order to prevent a wait state. $\overline{\text{SDTACK}}$ is an output when the TI380C25 is selected for DIO; otherwise, it is an input. H = System bus is not ready. L = Data transfer is complete; system bus is ready.

† I = input, O = output

NOTES: 1. Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).
7. Pin should be tied to V_{CC} with a 4.7-kΩ pullup resistor.

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O†	DESCRIPTION	
$\overline{\text{SRESET}}$	44	I	System reset. $\overline{\text{SRESET}}$ is activated to place the TI380C25 into a known initial state. Hardware reset puts most of the TI380C25 outputs into the high-impedance state and places all blocks into the reset state. The Intel mode DMA bus-width selection (S8) is latched on the rising edge of $\overline{\text{SRESET}}$. H = No system reset L = System reset Rising edge = Latch bus width for DMA operations (for Intel-mode applications)	
SRSX SRS0 SRS1 SRS2/$\overline{\text{SBERR}}$	47 46 45 54	I	Intel Mode	SRSX and SRS0–SRS2 are used for system-register select. These inputs select the word or byte to be transferred during a system DIO access. The most significant bit is SRSX and the least significant bit is SRS2 (see Note 1). MSb LSb Register selected = SRSX SRS0 SRS1 SRS2/$\overline{\text{SBERR}}$
			Motorola Mode	SRSX, SRS0 and SRS1 are used for system-register select. These inputs select the word or byte to be transferred during a system DIO access. The most significant bit is SRSX and the least significant bit is SRS1 (see Note 1). MSb LSb Register selected = SRSX SRS0 SRS1 $\overline{\text{SBERR}}$ is used for bus error. This signal corresponds to the bus-error signal of the 68xxx microprocessor. $\overline{\text{SBERR}}$ is internally synchronized to SBCLK. This input is driven low during a DMA cycle to indicate to the TI380C25 that the cycle must be terminated (see Section 3.4.5.3 of the *TMS380 Second-Generation Token Ring User's Guide* (SPWU005) for more information).
$\overline{\text{SWR}}$/$\overline{\text{SLDS}}$	61	I/O	Intel Mode	$\overline{\text{SWR}}$ is used for system-write strobe (see Note 7). $\overline{\text{SWR}}$ is an active-low write strobe that is an input during DIO and an output during DMA. H = Write cycle is not occurring. L = If DMA, data to be driven from SIF to host bus. If DIO, on the rising edge, the data is latched and written to the selected register.
			Motorola Mode	$\overline{\text{SLDS}}$ is used for lower-data strobe (see Note 7). $\overline{\text{SLDS}}$ is an input during DIO and an output during DMA. H = Not valid data on SADL0–SADL7 lines L = Valid data on SADL0–SADL7 lines
SXAL	63	O	System-extended-address latch. SXAL provides the enable pulse used to externally latch the most significant 16 bits of the 32-bit system address during DMA. SXAL is activated prior to the first cycle of each block DMA transfer, and thereafter as necessary (whenever an increment of the DMA address counter causes a carry out of the lower 16 bits). Systems that implement parity on addresses can use SXAL to externally latch the parity bits (available on SPL and SPH) for the DMA address extension.	
$\overline{\text{SYNCIN}}$	136	I	Reserved. $\overline{\text{SYNCIN}}$ must be left unconnected (see Note 1).	

† I = input, O = output

NOTES: 1: Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).
7. Pin should be tied to V_{CC} with a 4.7-kΩ pullup resistor.

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O†	DESCRIPTION	
S8/$\overline{\text{SHALT}}$	51	I	Intel Mode	S8 is used for system 8/16-bit bus select. S8 selects the bus width used for communications through the system interface. On the rising edge of $\overline{\text{SRESET}}$, the TI380C25 latches the DMA bus width; otherwise, the value on S8 dynamically selects the DIO bus width. H = Selects 8-bit mode (see Note 1) L = Selects 16-bit mode
			Motorola Mode	$\overline{\text{SHALT}}$ is used for system halt/bus error retry. If $\overline{\text{SHALT}}$ is asserted along with $\overline{\text{SBERR}}$, the adapter retries the last DMA cycle. This is the rerun operation as defined in the 68xxx specification. The BERETRY counter is not decremented by $\overline{\text{SBERR}}$ when $\overline{\text{SHALT}}$ is asserted (see Section 3.4.5.3 of the *TMS380 Second-Generation Token Ring User's Guide* (SPWU005) for more information).
V_{DDL}	37 55 126	I	Positive-supply voltage for digital logic. All V_{DDL} pins must be attached to the common-system power-supply plane.	
V_{DD}	9 34 72 89 106 137	I	Positive-supply voltage for output buffers. All V_{DD} pins must be attached to the common-system power-supply plane.	
V_{SSC}	39 87 117 144	I	Ground reference for output buffers (clean ground). All V_{SSC} pins must be attached to the common-system ground plane.	
V_{SSL}	2 52 53 73 36 108 128 129	I	Ground reference for digital logic. All V_{SSL} pins must be attached to the common-system ground plane.	
V_{SS}	11 19 62 91 134	I	Ground connections for output buffers. All V_{SS} pins must be attached to system ground plane.	
NC	1 10 35 71 88 90 107 109		These pins should be left unconnected.	

† I = input, O = output

NOTE 1: Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).

Pin Functions (Continued)

Token-Ring Media Interface

PIN NAME	PIN NO.	I/O†	DESCRIPTION
DRVR $\overline{\text{DRVR}}$	115 114	O	Differential-driver data output. DRVR and $\overline{\text{DRVR}}$ are the differential outputs that send the TI380C25 transmit data to the TMS38054 for driving onto the ring-transmit-signal pair.
FRAQ	111	O	Frequency-acquisition control. FRAQ determines the use of frequency- or phase-acquisition mode in the TMS38054. H = Wide range. Frequency centering to PXTALIN by TMS38054. L = Narrow range. Phase lock onto the incoming data (RCVINA and RCVINB) by the TMS38054.
$\overline{\text{NSRT}}$	112	O	Insert-control signal to the TMS38054. $\overline{\text{NSRT}}$ enables the phantom-driver outputs (PHOUTA and PHOUTB) of the TMS38054, through the watchdog timer, for insertion onto the token ring. Static high = Inactive, phantom current removed (due to watchdog timer) Static low = Inactive, phantom current removed (due to watchdog timer) $\overline{\text{NSRT}}$ low and pulsed high = Active, current output on PHOUTA and PHOUTB
PXTALIN	118	I	Ring-interface clock-frequency control (see Note 5). At 16-Mbps ring speed, PXTALIN must be supplied a 32-MHz signal. At 4-Mbps ring speed, PXTALIN must be 8 MHz and can be the output from OSCOUT.
RCLK	120	I	Ring-interface recovered clock (see Note 5). RCLK is the clock recovered by the TMS38054 from the token-ring received data. For 16-Mbps operation, RCLK is a 32-MHz clock; for 4-Mbps operation, RCLK is an 8-MHz clock.
RCVR	121	I	Ring-interface received data (see Note 5). RCVR contains the data received by the TMS38054 from the token ring.
$\overline{\text{REDY}}$	110	I	Ring-interface ready. $\overline{\text{REDY}}$ indicates the presence of received data as monitored by the TMS38054 energy-detect capacitor. H = Not ready. Ignore received data. L = Ready. Received data.
$\overline{\text{WFLT}}$	113	I	Wire-fault detect. $\overline{\text{WFLT}}$ is an input to the TI380C25 driven by the TMS38054. $\overline{\text{WFLT}}$ indicates a current imbalance of the TMS38054 PHOUTA and PHOUTB pins. H = No wire fault detected L = Wire fault detected
$\overline{\text{WRAP}}$	116	O	Internal wrap select. $\overline{\text{WRAP}}$ is an output from the TI380C25 to the ring interface to activate an internal attenuated feedback path from the transmitted data (DRVR) to receive data (RCVR) signals for bring-up diagnostic testing. When active, the TMS38054 also cuts off the current drive to the transmission pair. H = Normal ring operation L = Transmit data drives receive data (loopback).

† I = input, O = output
NOTE 5: Pin has an expanded input-voltage specification.

Pin Functions (Continued)

Token-Ring Media Interface

PIN NAME	PIN NO.	I/O†	DESCRIPTION
TEST0 TEST1 TEST2	103 102 101	I	Network select inputs. TEST0–TEST2 are used to select the network speed and type to be used by the TI380C25. These inputs should be changed only during adapter reset. Connect TEST2 to V_{DDL}. TEST0 TEST1 TEST2 DESCRIPTION L NC H 16-Mbps token ring H NC H 4-Mbps token ring X X L Reserved
TEST3 TEST4 TEST5	100 99 98	I	Test inputs. TEST3–TEST5 should be left unconnected (see Note 1). Module-in-place test mode is achieved by tying TEST3 and TEST4 to ground. In this mode, all TI380C25 outputs are in the high-impedance state. Internal pullups on all TI380C25 inputs are disabled (except TEST3–TEST5).
XFAIL	104	I	External fail-to-match signal. An enhanced-address-copy-option (EACO) device uses XFAIL to indicate to the TI380C25 that it should not copy the frame nor set the ARI/FCI bits in a token-ring frame due to an external address match.The ARI/FCI bits in a token-ring frame can be set due to an internal address-matched frame. If an EACO device is not used, XFAIL must be left unconnected. XFAIL is ignored when CAF mode is enabled [see table in XMATCH description (see Note 1)]. H = No address match by external address checker L = External address-checker-armed state
XMATCH	105	I	External match signal. An enhanced-address-copy-option (EACO) device uses XMATCH to indicate to the TI380C25 to copy the frame and set the ARI/FCI bits in a token-ring frame. If an EACO device is not used, XMATCH must be left unconnected. XMATCH is ignored when CAF mode is enabled (see Note 1). H = Address match recognized by external address checker L = External address-checker-armed state XMATCH XFAIL FUNCTION 0 0 Armed (processing frame data) 0 1 Do not externally match the frame (XFAIL takes precedence). 1 0 Copy the frame 1 1 Do not externally match the frame (XFAIL takes precedence). Hi-Z Hi-Z Reset state (adapter not initialized)

† I = input, O = output

NOTE 1: Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).

architecture

The major blocks of the TI380C25 include the communications processor (CP), system interface (SIF), memory interface (MIF), protocol handler (PH), clock generator (CG), and adapter-support function (ASF). The functionality of each block is described in the following sections.

communications processor (CP)

The CP performs the control and monitoring of the other functional blocks in the TI380C25. The control and monitoring protocols are specified by the software (downloaded or ROM based) in local memory. Available protocols include:

- Media access control (MAC) software
- Logical link control (LLC) software
- Copy all frames (CAF) software

The CP is a proprietary 16-bit central processing unit (CPU) with data cache and a single prefetch pipe for pipelining of instructions. These features enhance the TI380C25 maximum performance capability to about 8 million instructions per second (MIPS) with an average of about 5 MIPS.

system interface (SIF)

The SIF performs the interfacing of the LAN subsystem to the host system. This interface may require additional logic depending on the application. The system interface can transfer information/data using any of these three methods:

- Direct memory access (DMA)
- Direct input/output (DIO)
- Pseudo-direct memory access (PDMA)

DMA (or PDMA) is used to transfer all data to/from host memory from/to local memory. The main uses of DIO are for loading the software to local memory and for initializing the TI380C25. DIO also allows command/status interrupts to occur to and from the TI380C25.

The system interface can be hardware selected for either of two modes by use of SI/$\overline{M}$. The mode selected determines the memory organizations and control signals used. These modes are as follows:

- The Intel 80x8x families: 8-, 16-, and 32-bit bus devices
- The Motorola 68xxx microprocessor family: 16- and 32-bit bus devices

The system interface supports host-system memory addressing up to 32 bits (32-bit reach into the host-system memory). This allows greater flexibility in using/accessing host-system memory. System designers can customize the system interface to their particular bus by using one of the following:

- Programmable burst transfers or cycle-steal DMA operations
- Optional parity protection

These features are implemented in hardware to reduce system overhead, facilitate automatic rearbitration of the bus after a burst, or repeat a cycle when errors occur (parity or bus). Bus retries are also supported.

The system-interface hardware also includes features to enhance the integrity of the TI380C25 and the data. These features include the following:

- Always internally maintain odd-byte parity regardless of parity being disabled
- Monitor for the presence of a clock failure
- Can switch SIF speeds from 2 MHz to 33 MHz

On every cycle, the system interface compares all the system clocks to a reference clock. If any of the clocks become invalid, the TI380C25 enters the slow-clock mode, which prevents latch-up of the TI380C25. If the SBCLK is invalid, any DMA cycle is terminated immediately; otherwise, the DMA cycle is completed and the TI380C25 is placed in slow-clock mode.

system interface (SIF) (continued)

When the TI380C25 enters the slow-clock mode, the clock that failed is replaced by a slow free-running clock and the device is placed into a low-power reset state. When the failed clock(s) return to valid operation, the TI380C25 must be reinitialized.

For DMA with a 16-MHz clock, a continuous transfer rate of 64 megabits per second (8 Mbps) can be obtained. For DMA with a 25-MHz clock, a continuous transfer rate of 96 megabits per second (12 Mbps) can be obtained. For DMA with a 33-MHz clock, a continuous transfer rate of 128 megabits per second (16 Mbps) can be obtained. For 8-bit and 16-bit pseudo-DMA, the following data rates can be obtained:

LOCAL BUS SPEED	8-BIT PDMA	16-BIT PDMA
4 MHz	48 Mbps	64 Mbps
6 MHz	72 Mbps	96 Mbps

Since the main purpose of DIO is for downloading and initialization, the DIO transfer rate is not a significant issue.

memory interface (MIF)

The MIF performs the memory management to allow the TI380C25 to address 2M bytes in local memory. Hardware in the MIF allows the TI380C25 to be directly connected to DRAMs without additional circuitry. This glueless-DRAM connection includes the DRAM refresh controller. The MIF also handles all internal bus arbitration between these blocks. When required, the MIF then arbitrates for the external bus.

The MIF is responsible for the memory mapping of the CPU of a task. The memory maps of DRAMs, EPROMs, burned-in addresses (BIA), and external devices are appropriately addressed when required by the system interface, protocol handler, or for a DMA transfer.

The memory interface is capable of a 64-Mbps continuous transfer rate when using a 4-MHz local bus (64-MHz device crystal) and a 96-Mbps continuous transfer rate when using a 6-MHz local bus.

protocol handler (PH)

The PH performs the hardware-based real-time protocol functions for a token-ring LAN. Network type is determined by TEST0–TEST2. Token-ring network is determined by software and can be either 16 Mbps or 4 Mbps. These speeds are not fixed by the hardware but by the software.

The PH converts the parallel-transmit data to serial-network data of the appropriate coding and converts the received serial data to parallel data. The PH data-management state machines direct the transmission / reception of data to / from local memory through the MIF. The PH buffer-management state machines automatically oversee this process, directly sending / receiving linked lists of frames without CPU intervention.

The protocol handler contains many state machines that provide the following features:

- Transmit and receive frames
- Capture tokens
- Provide token-priority controls
- Manage the TI380C25 buffer memory
- Provide frame-address recognition (group, specific, functional, and multicast)
- Provide internal parity protection
- Control and verify the PHY-layer circuitry-interface signals

Integrity of the transmitted and received data is assured by cyclic redundancy checks (CRC), detection of network data violations, and parity on internal data paths. All data paths and registers are optionally parity protected to assure functional integrity.

adapter-support function (ASF)

The ASF performs support functions not contained in the other blocks. The support functions are:

- The TI380C25 base timer
- Identification, management, and service of internal and external interrupts
- Test-pin mode control, including the unit-in-place mode for board testing
- Illegal state check (checks for illegal states such as parity and illegal opcodes)

clock generator (CG)

The CG performs the generation of all the internal clocks required by the other functional blocks, including the local memory-bus clocks (MBCLK1, MBCLK2). The CG also generates the reference timer used to sample all input clocks (SBCLK, OSCIN, RCLK, and PXTALIN). If no transition is detected within the period of the reference timer on any input clock signal, the CG places the TI380C25 into slow-clock mode. The frequency of the reference timer is in the range of 10 kHz–100 kHz.

user-accessible hardware registers and TI380C25 internal pointers

The following tables show how to access internal data via pointers and how to address the registers in the host interface. The SIFACL register, which directly controls device operation, is described in detail. The adapter-internal pointers table on the following page is defined only after TI380C25 initialization and until the OPEN command is issued. These pointers are defined by the TI380C25 software (microcode), and this table describes the release 2.x of the TI380C25 software.

Adapter-Internal Pointers for Token Ring†

ADDRESS	DESCRIPTION
>00.FFF8‡	Pointer to software raw microcode level in chapter 0
>00.FFFA‡	Pointer to starting location of copyright notices. Copyright notices are separated by a >0A character and terminated by a >00 character in chapter 0.
>01.0A00	Pointer to burned-in address in chapter 1
>01.0A02	Pointer to software level in chapter 1
>01.0A04	Pointer to TI380C25 addresses in chapter 1: Pointer + 0 node address Pointer + 6 group address Pointer + 10 functional address
>01.0A06	Pointer to TI380C25 parameters in chapter 1: Pointer + 0 physical-drop number Pointer + 4 upstream neighbor address Pointer + 10 upstream physical-drop number Pointer + 14 last ring-poll address Pointer + 20 reserved Pointer + 22 transmit access priority Pointer + 24 source class authorization Pointer + 26 last attention code Pointer + 28 source address of the last received frame Pointer + 34 last beacon type Pointer + 36 last major vector Pointer + 38 ring status Pointer + 40 soft-error timer value Pointer + 42 ring-interface error counter Pointer + 44 local ring number Pointer + 46 monitor error code Pointer + 48 last beacon-transmit type Pointer + 50 last beacon-receive type Pointer + 52 last MAC-frame correlator Pointer + 54 last beaconing-station UNA Pointer + 60 reserved Pointer + 64 last beaconing-station physical-drop number
>01.0A08	Pointer to MAC buffer (a special buffer used by the software to transmit adapter-generated MAC frames) in chapter 1
>01.0A0A	Pointer to LLC counters in chapter 1: Pointer + 0 MAX_SAPs Pointer + 1 open SAPs Pointer + 2 MAX_STATIONs Pointer + 3 open stations Pointer + 4 available stations Pointer + 5 reserved
>01.0A0C	Pointer to 4-/16-Mbps word flag. If zero, the adapter is set to run at 4 Mbps. If nonzero, the adapter is set to run at 16 Mbps.
>01.0A0E	Pointer to total TI380C25 RAM found in 1K bytes in RAM allocation test in chapter 1.

† This table describes the pointers for release 2.x of the TI380C25 software.
‡ This address valid only for microcode release 2.x

User-Access Hardware Registers

80x8x 16-BIT MODE: (SI / $\overline{M}$ = 1, S8 / $\overline{SHALT}$ = 0)†						
WORD TRANSFERS			NORMAL MODE $\overline{SBHE}$ = 0 SRS2 = 0		PSEUDO-DMA MODE ACTIVE $\overline{SBHE}$ = 0 SRS2 = 0	
BYTE TRANSFERS			$\overline{SBHE}$ = 0 SRS2 = 1	$\overline{SBHE}$ = 1 SRS2 = 0	$\overline{SBHE}$ = 0 SRS2 = 1	$\overline{SBHE}$ = 1 SRS2 = 0
SRSX	SRS0	SRS1				
0	0	0	SIFDAT MSB	SIFDAT LSB	SDMADAT MSB	SDMADAT LSB
0	0	1	SIFDAT / INC MSB	SIFDAT / INC LSB	DMALEN MSB	DMALEN LSB
0	1	0	SIFADR MSB	SIFADR LSB	SDMAADR MSB	SDMAADR LSB
0	1	1	SIFCMD	SIFSTS	SDMAADX MSB	SDMAADX LSB
1	0	0	SIFACL MSB	SIFACL LSB	SIFACL MSB	SIFACL LSB
1	0	1	SIFADR MSB	SIFADR LSB	SIFADR MSB	SIFADR LSB
1	1	0	SIFADX MSB	SIFADX LSB	SIFADX MSB	SIFADX LSB
1	1	1	DMALEN MSB	DMALEN LSB	DMALEN MSB	DMALEN LSB

† $\overline{SBHE}$ = 1 and SRS2 = 1 are not defined

80x8x 8-BIT MODE: (SI / $\overline{M}$ = 1, S8/SHALT = 1)					
SRSX	SRS0	SRS1	SRS2	NORMAL MODE $\overline{SBHE}$ = X	PSEUDO-DMA MODE ACTIVE $\overline{SBHE}$ = X
0	0	0	0	SIFDAT LSB	SDMADAT LSB
0	0	0	1	SIFDAT MSB	SDMADAT MSB
0	0	1	0	SIFDAT/INC LSB	DMALEN LSB
0	0	1	1	SIFDAT/INC MSB	DMALEN MSB
0	1	0	0	SIFADR LSB	SDMAADR LSB
0	1	0	1	SIFADR MSB	SDMAADR MSB
0	1	1	0	SIFSTS	SDMAADX LSB
0	1	1	1	SIFCMD	SDMAADX MSB
1	0	0	0	SIFACL LSB	SIFACL LSB
1	0	0	1	SIFACL MSB	SIFACL MSB
1	0	1	0	SIFADR LSB	SIFADR LSB
1	0	1	1	SIFADR MSB	SIFADR MSB
1	1	0	0	SIFADX LSB	SIFADX LSB
1	1	0	1	SIFADX MSB	SIFADX MSB
1	1	1	0	DMALEN LSB	DMALEN LSB
1	1	1	1	DMALEN MSB	DMALEN MSB

68xxx MODE: (SI/$\overline{M}$ = 0)‡						
WORD TRANSFERS			NORMAL MODE $\overline{SUDS}$ = 0 $\overline{SLDS}$ = 0		PSEUDO-DMA MODE ACTIVE $\overline{SUDS}$ = 0 $\overline{SLDS}$ = 0	
BYTE TRANSFERS			$\overline{SUDS}$ = 0 $\overline{SLDS}$ = 1	$\overline{SUDS}$ = 1 $\overline{SLDS}$ = 0	$\overline{SUDS}$ = 0 $\overline{SLDS}$ = 1	$\overline{SUDS}$ = 1 $\overline{SLDS}$ = 0
SRSX	SRS0	SRS1				
0	0	0	SIFDAT MSB	SIFDAT LSB	SDMADAT MSB	SDMADAT LSB
0	0	1	SIFDAT/INC MSB	SIFDAT/INC LSB	DMALEN MSB	DMALEN LSB
0	1	0	SIFADR MSB	SIFADR LSB	SDMAADR MSB	SDMAADR LSB
0	1	1	SIFCMD	SIFSTS	SDMAADX MSB	SDMAADX LSB
1	0	0	SIFACL MSB	SIFACL LSB	SIFACL MSB	SIFACL LSB
1	0	1	SIFADR MSB	SIFADR LSB	SIFADR MSB	SIFADR LSB
1	1	0	SIFADX MSB	SIFADX LSB	SIFADX MSB	SIFADX LSB
1	1	1	DMALEN MSB	DMALEN LSB	DMALEN MSB	DMALEN LSB

‡ 68xxx mode is always 16 bit.

SIF adapter-control register (SIFACL)

The SIFACL register allows the host processor to control and to some extent reconfigure the TI380C25 under software control.

SIFACL Register

Bit #	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	TEST0	TEST1	TEST2	—	SWHLDA	SWDDIR	SWHRQ	PSDMAEN	ARESET	CPHALT	BOOT	LBP	SINTEN	PEN	NSEL OUT0	NSEL OUT1
	R	R	R		RP–0	R–u	R–0	RS–0	RW–0	RP–b	RP–b	RW –0	RW–1	RP–p	RP–0	RP–1

Legend:

R	=	Read
W	=	Write
P	=	Write during ARESET = 1 only
S	=	Set only
–n	=	Value after reset
b	=	Value on BTSTRP
p	=	Value on PRTYEN
u	=	Indeterminate

Bits 0–2: Value on TEST0 and TEST2 pins

These bits are read only and always reflect the value on the corresponding device pins. This allows the host S/W to determine speed configuration. If the network speed and type are software configurable, these bits can be used to determine which configurations are supported by the network hardware.

TEST0	TEST1	TEST2	Description
L	NC	H	16-Mbps token ring
H	NC	H	4-Mbps token ring
X	X	L	Reserved

Bit 3: **Reserved.** Read data is indeterminate.

Bit 4: SWHLDA — Software Hold Acknowledge

This bit allows the function of SHLDA / $\overline{\text{SBGR}}$ to be emulated from software control for pseudo-DMA mode.

PSDMAEN	SWHLDA	SWHRQ	RESULT
0†	X	X	SWHLDA value in the SIFACL register cannot be set to a one.
1†	0	0	No pseudo-DMA request pending
1†	0	1	Indicates a pseudo-DMA request interrupt
1†	1	X	Pseudo-DMA process in progress

† The value on SHLDA / $\overline{\text{SBGR}}$ is ignored.

Bit 5: **SWDDIR — Current SDDIR Signal Value**

This bit contains the current value of the pseudo-DMA direction. This enables the host to easily determine the direction of DMA transfers, which allows system DMA to be controlled by system software.

0 = Pseudo DMA from host system to TI380C25
1 = Pseudo DMA from TI380C25 to host system

Bit 6: **SWHRQ — Current SHRQ Signal Value**

This bit contains the current value on SHRQ/$\overline{\text{SBRQ}}$ when in Intel mode, and the inverse of the value on SHRQ/$\overline{\text{SBRQ}}$ when in Motorola mode. This enables the host to easily determine if a pseudo-DMA transfer is requested.

	INTEL MODE (SI/$\overline{\text{M}}$ = H)	MOTOROLA MODE (SI/$\overline{\text{M}}$ = L)
0 =	System bus not requested	System bus not requested
1 =	System bus requested	System bus requested

Bit 7: **PSDMAEN — Pseudo-System-DMA Enable**

This bit enables pseudo-DMA operation.

0 = Normal bus-master DMA operation is possible.
1 = Pseudo-DMA operation selected. Operation dependent on the values of the SWHLDA and SWHRQ bits in the SIFACL register.

Bit 8: **ARESET — Adapter Reset**

This bit is a hardware reset of the TI380C25. This bit has the same effect as $\overline{\text{SRESET}}$ except that the DIO interface to the SIFACL register is maintained. This bit is set to 1 if a clock failure is detected (OSCIN, PXTALIN, RCLK, or SBCLK not valid).

0 = The TI380C25 operates normally.
1 = The TI380C25 is held in the reset condition.

Bit 9: **CPHALT — Communications-Processor Halt**

This bit controls the TI380C25 processor access to the internal TI380C25 buses. This prevents the TI380C25 from executing instructions before the microcode has been downloaded.

0 = The TI380C25 processor can access the internal TI380C25 buses.
1 = The TI380C25 processor is prevented from accessing the internal adapter buses.

Bit 10: **BOOT — Bootstrap CP Code**

This bit indicates whether the memory in chapters 0 and 31 of the local-memory space is RAM or ROM/PROM/EPROM. This bit controls the operation of $\overline{\text{MCAS}}$ and $\overline{\text{MROMEN}}$.

0 = ROM/PROM/EPROM memory in chapters 0 and 31
1 = RAM memory in chapters 0 and 31

Bit 11: **LBP — Local-Bus Priority**

This bit controls the priority levels of devices on the local bus.

0 = No external devices (such as TI380FPA) are used with the TI380C25.
1 = An external device (such as TI380FPA) is used with the TI380C25. This allows the external bus master to operate at the necessary priorities on the local bus.

If the system uses the TMS380SRA only, the bit must be set to 0. If the system uses both the TMS380SRA and the TI380FPA, the bit must be set to 1.

Bit 12: **SINTEN — System-Interrupt Enable**

This bit allows the host processor to enable or disable system-interrupt requests from the TI380C25. The system-interrupt request from the TI380C25 is on SINTR/$\overline{\text{SIRQ}}$. The following equation shows how SINTR/$\overline{\text{SIRQ}}$ is driven. The table also explains the results of the states.

SINTR/$\overline{\text{SIRQ}}$ = (PSDMAEN * SWHRQ * !SWHLDA) + (SINTEN * SYSTEM_INTERRUPT)

PSDMAEN	SWHRQ	SWHLDA	SINTEN	SYSTEM INTERRUPT (SIFSTS REGISTER)	RESULT
1†	1	1	X	X	Pseudo DMA is active.
1†	1	0	X	X	The TI380C25 generated a system interrupt for a pseudo DMA.
1†	0	0	X	X	Not a pseudo-DMA interrupt
X	X	X	1	1	The TI380C25 generates a system interrupt.
0	X	X	1	0	The TI380C25 does not generate a system interrupt.
0	X	X	0	X	The TI380C25 cannot generate a system interrupt.

† The value on SHLDA / $\overline{\text{SBGR}}$ is ignored.

Bit 13: **PEN — Parity Enable**

This bit determines whether data transfers within the TI380C25 are checked for parity.

0 = Data transfers are not checked for parity.
1 = Data transfers are checked for correct odd parity.

Bit 14 – 15: **NSELOUT0, NSELOUT0 1 — Network-Selection Outputs**

The values in these bits control NSELOUT0 and NSELOUT1. These bits can be modified only while the ARESET bit is set.

These bits can be used to software configure a TI380C25 as follows: NSELOUT0 should be connected to TEST0 (TEST1 should be left unconnected and TEST2 should be tied high). NSELOUT0 and NSELOUT1 are used to select network speed as shown below:

NSELOUT0	NSELOUT1	SELECTION
0	0	Reserved
0	1	16-Mbps token ring
1	0	Reserved
1	1	4-Mbps token ring

At power up, these bits are set corresponding to 16-Mbps token ring (NSELOUT1 = 1, NSELOUT0 = 0).

SIFACL control for pseudo-DMA operation

Pseudo DMA is software controlled by the use of five bits in the SIFACL register. The logic model for the SIFACL register control of pseudo-DMA operation is shown in Figure 2.

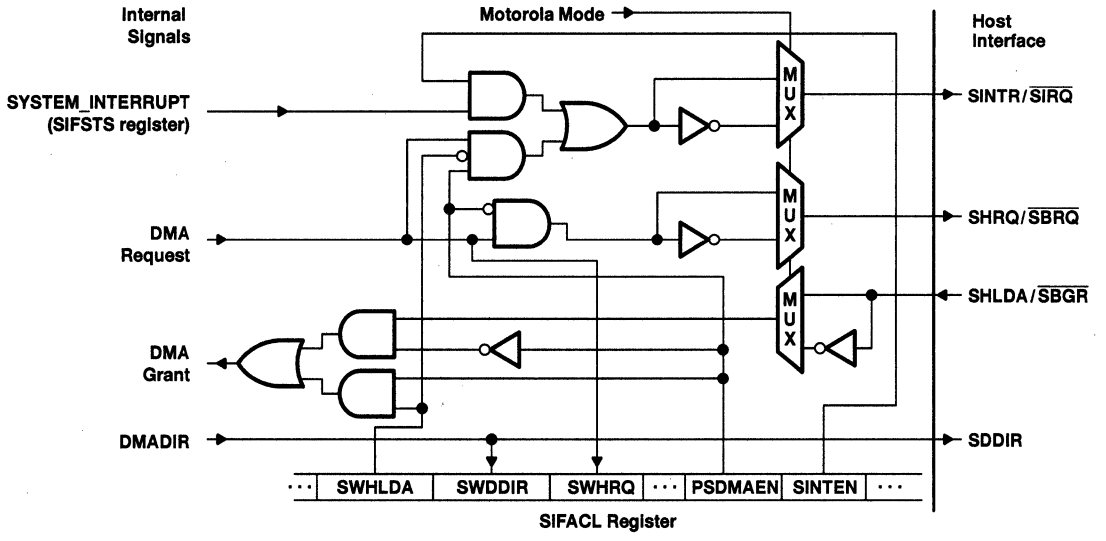


Figure 2. Pseudo-DMA Logic Related to SIFACL Bits

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 8) ..... 7 V
Input voltage range, V_I (see Note 8) ..... – 0.3 V to 20 V
Output voltage range ..... – 2 V to 7 V
Power dissipation ..... 0.9 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 8: Voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.75	5	5.25	V
V_{SS}	Supply voltage (see Note 9)		0	0	0	V
V_{IH}	High-level input voltage	TTL-level signal	2		V_{DD}+0.3	V
		OSCIN	2.4		V_{DD}+0.3	
		RCLK, PXTALIN, RCVR	2.6		V_{DD}+0.3	
V_{IL}	Low-level input voltage, TTL-level signal (see Note 10)		–0.3		0.8	V
I_{OH}	High-level output current				–400	µA
I_{OL}	High-level output current (see Note 11)				2	mA
T_A	Operating free-air temperature		0		70	°C
T_C	Operating case temperature				100	°C

NOTES: 9. All V_{SS} pins should be routed to minimize inductance to system ground.
10. The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used for logic-voltage levels only.
11. Output current of 2 mA is sufficient to drive five low-power Schottky TTL loads or ten advanced low-power Schottky TTL loads (worst case).

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, TTL-level signal (see Note 12)	V_{DD} = MIN,	I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage, TTL-level signal	V_{DD} = MIN,	I_{OL} = MAX			0.6	V
I_O	High-impedance output current	V_{DD} = MAX,	V_O = 2.4 V			20	µA
		V_{DD} = MAX,	V_O = 0.4 V			–20	
I_I	Input current, any input or input / output	V_I = V_{SS} to V_{DD}				±20	µA
I_{DD}	Supply current	V_{DD} = MAX				160	mA
I_{SCM}	Supply current, slow-clock mode	V_{DD} = 5 V			3		mA
C_i	Input capacitance, any input	f = 1 MHz,	Others at 0 V			15	pF
C_o	Output capacitance, any output or input/output	f = 1 MHz,	Others at 0 V			15	pF

‡ For conditions shown as MIN/MAX, use the appropriate value specified under the recommended operating conditions.

NOTE 12: The following signals require an external pullup resistor: SRAS/$\overline{\text{SAS}}$, $\overline{\text{SRDY}}$/$\overline{\text{SDTACK}}$, $\overline{\text{SRD}}$/$\overline{\text{SUDS}}$, $\overline{\text{SWR}}$/$\overline{\text{SLDS}}$, $\overline{\text{EXTINT0}}$–$\overline{\text{EXTINT3}}$, and $\overline{\text{MBRQ}}$.

PARAMETER MEASUREMENT INFORMATION

timing parameters

The timing parameters for all the signals of the TI380C25 are shown in the following tables and are illustrated in the accompanying figures. The purpose of these figures and tables is to quantify the timing relationships among the various signals. The parameters are numbered for convenience.

static signals

The following table lists signals that are not allowed to change dynamically and therefore have no timing associated with them. They should be strapped high, low, or left unconnected as required.

SIGNAL	FUNCTION
SI/$\overline{M}$	Host-processor select (Intel/Motorola)
CLKDIV	Reserved
BTSTRP	Default-bootstrap mode (RAM/ROM)
PRTYEN	Default-parity select (enabled/disabled)
TEST0	Test terminal indicates network type
TEST1	NC
TEST2	Test terminal indicates network type
TEST3	Test terminal for TI manufacturing test †
TEST4	Test terminal for TI manufacturing test †
TEST5	Test terminal for TI manufacturing test †

† For unit-in-place test

timing parameter symbology

Some timing parameter symbols have been created in accordance with JEDEC Standard 100-A. In order to shorten the symbols, some of the signal names and other related terminology have been abbreviated as shown below:

DR	DRVR	RS	$\overline{SRESET}$
DRN	$\overline{DRVR}$	VDD	V_{DDL}, V_{DD}
OSC	OSCIN		
SCK	SBCLK		

Lower case subscripts are defined as follows:

c	cycle time	r	rise time
d	delay time	sk	skew
h	hold time	su	setup time
w	pulse duration (width)	t	transition time

The following additional letters and phrases are defined as follows:

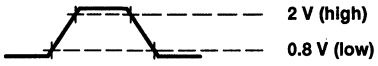
H	High	Z	High impedance
L	Low	Falling edge	No longer high
V	Valid	Rising edge	No longer low

PARAMETER MEASUREMENT INFORMATION

Outputs are driven to a minimum high-logic level of 2.4 V and to a maximum low-logic level of 0.6 V. These levels are compatible with TTL devices.

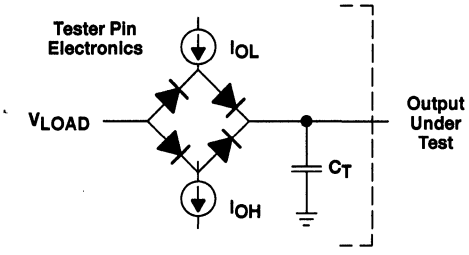
Output transition times are specified as follows: For a high-to-low transition on either an input or output signal, the level at which the signal is said to be no longer high is 2 V and the level at which the signal is said to be low is 0.8 V. For a low-to-high transition, the level at which the signal is said to be no longer low is 0.8 V and the level at which the signal is said to be high is 2 V, as shown below.

The rise and fall times are not specified but are assumed to be those of standard TTL devices, which are typically 1.5 ns.



test measurement

The test-load circuit shown in Figure 3 represents the programmable load of the tester pin electronics that are used to verify timing parameters of TI380C25 output signals.



Where: I_{OL} = 2 mA, dc-level verification (all outputs)
I_{OH} = 400 μA (all outputs)
V_{LOAD} = 1.5 V, typical dc-level verification or 0.7 V, typical timing verification
C_T = 65 pF, typical load-circuit capacitance

Figure 3. Test-Load Circuit

power up, SBCLK, OSCIN, MBCLK1, MBCLK2, $\overline{\text{SYNCIN}}$, and $\overline{\text{SRESET}}$ timing

NO.				MIN	NOM	MAX	UNIT
100†	$t_{r(VDD)}$	Rise time, 1.2 V to minimum V_{DD}-high level				1	ms
101†‡	$t_{d(VDDH-SCKV)}$	Delay time, minimum V_{DD}-high level to first valid SBCLK no longer high				1	ms
102†‡	$t_{d(VDDH-OSCV)}$	Delay time, minimum V_{DD}-high level to first valid OSCIN high				1	ms
103	$t_{c(SCK)}$	Cycle time, SBCLK (see Note 13)		30.3		500	ns
104	$t_{w(SCKH)}$	Pulse duration, SBCLK high		13		500	ns
105	$t_{w(SCKL)}$	Pulse duration, SBCLK low		13		500	ns
106†	$t_{t(SCK)}$	Transition time, SBCLK				2	ns
107	$t_{c(OSC)}$	Cycle time, OSCIN (see Note 14)			1/OSCIN		ns
108	$t_{w(OSCH)}$	Pulse duration, OSCIN high (see Note 15)	OSCIN = 64 MHz	5.5			ns
			OSCIN = 48 MHz	8			
			OSCIN = 32 MHz	8			
109	$t_{w(OSCL)}$	Pulse duration, OSCIN low (see Note 15)	OSCIN = 64 MHz	5.5			ns
			OSCIN = 48 MHz	8			
			OSCIN = 32 MHz	8			
110†	$t_{t(OSC)}$	Transition time, OSCIN				3	ns
111†	$t_{d(OSCV-CKV)}$	Delay time, OSCIN valid to MBCLK1 and MBCLK2 valid				1	ms
117†	$t_{h(VDDH-RSL)}$	Hold time, $\overline{\text{SRESET}}$ low after V_{DD} reaches minimum high level		5			ms
118†	$t_{w(RSH)}$	Pulse duration, $\overline{\text{SRESET}}$ high		14			µs
119†	$t_{w(RSL)}$	Pulse duration, $\overline{\text{SRESET}}$ low		14			µs
288†	$t_{su(RST)}$	Setup time, DMA size to $\overline{\text{SRESET}}$ high (Intel mode only)		10			ns
289†	$t_{h(RST)}$	Hold time, DMA size from $\overline{\text{SRESET}}$ high (Intel mode only)		10			ns
	t_M	One-eighth of a local memory cycle	CLKDIV = H	$2t_{c(OSC)}$			ns
			CLKDIV = L	$2t_{c(OSC)}$			

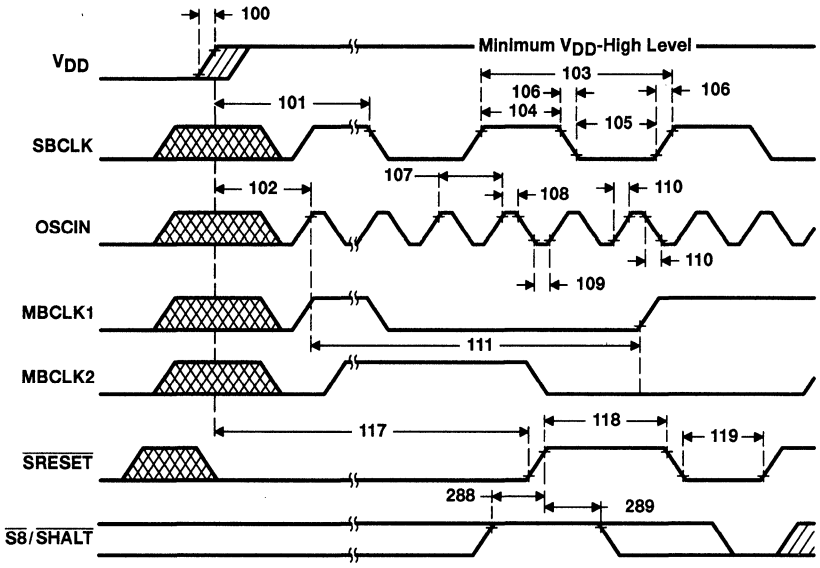
† This specification is provided as an aid to board design. It is not assured during manufacturing testing.

‡ If parameter 101 or 102 cannot be met, parameter 117 must be extended by the larger difference: real value of parameter 101 or 102 minus the max value listed.

NOTES: 13. SBCLK can be any value between 2 MHz to 33 MHz. This data sheet describes the system interface (SIF) timing parameters for the case of SBCLK at 25 MHz and at 33 MHz.

14. The value of OSCIN can be 64 MHz ±1%, 32 MHz ± 1%, or 48 MHz ± 1%. If OSCIN is used to generate PXTALIN, the OSCIN tolerance must be ±0.01%.

15. This is to assure a ± 5% duty-cycle crystal, provided that OSCIN meets the recommended operating conditions for V_{IH} and V_{IL}.



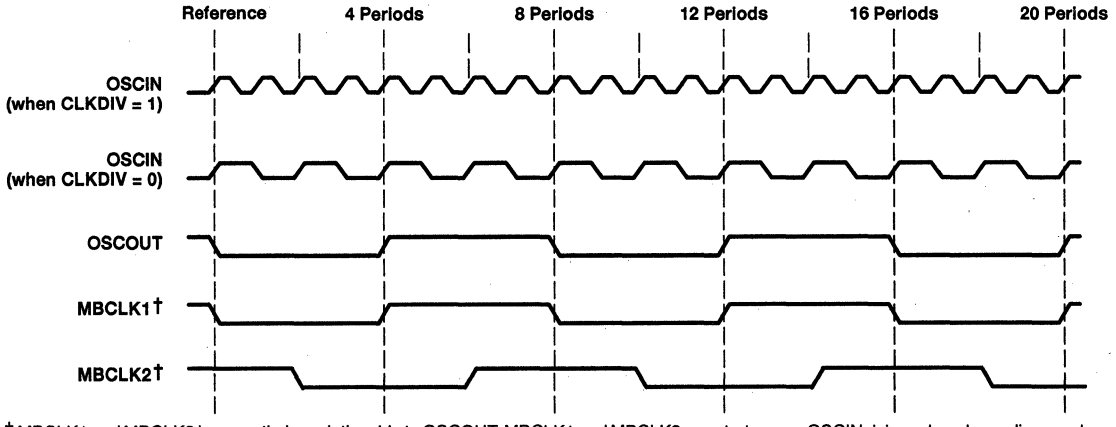
NOTE A: In order to represent the information in one illustration, nonactual phase and timebase characteristics are shown. Refer to specified parameters for precise information.

Figure 4. Timing for Power Up, System Clocks, SYNCIN, and SRESET

memory-bus timing: local-memory clocks, $\overline{\text{MAL}}$, $\overline{\text{MROMEN}}$, $\overline{\text{MBIAEN}}$, $\overline{\text{NMI}}$, $\overline{\text{MRESET}}$, and ADDRESS

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

NO.		MIN	MAX	UNIT
1	Period of MBCLK1 and MBCLK2	$4t_M$		ns
2	Pulse duration, clock high	$2t_M-9$		ns
3	Pulse duration, clock low	$2t_M-9$		ns
4	Hold time, MBCLK2 low after MBCLK1 high	t_M-9		ns
5	Hold time, MBCLK1 high after MBCLK2 high	t_M-9		ns
6	Hold time, MBCLK2 high after MBCLK1 low	t_M-9		ns
7	Hold time, MBCLK1 low after MBCLK2 low	t_M-9		ns
8	Setup time, address/enable on MAX0, MAX2, and $\overline{\text{MROMEN}}$ before MBCLK1 no longer high	t_M-9		ns
9	Setup time, row address on MADL0–MADL7, MAXPH, and MAXPL before MBCLK1 no longer high	t_M-14		ns
10	Setup time, address on MADH0–MADH7 before MBCLK1 no longer high	t_M-14		ns
11	Setup time, $\overline{\text{MAL}}$ high before MBCLK1 no longer high	13		ns
12	Setup time, address on MAX0, MAX2, and $\overline{\text{MROMEN}}$ before MBCLK1 no longer low	$0.5t_M-9$		ns
13	Setup time, column address on MADL0–MADL7, MAXPH, and MAXPL before MBCLK1 no longer low	$0.5t_M-9$		ns
14	Setup time, status on MADH0–MADH7 before MBCLK1 no longer low	$0.5t_M-9$		ns
120	Setup time, $\overline{\text{NMI}}$ valid before MBCLK1 low	30		ns
121	Hold time, $\overline{\text{NMI}}$ valid after MBCLK1 low	0		ns
126	Delay time, MBCLK1 no longer low to $\overline{\text{MRESET}}$ valid	0	20	ns
129	Hold time, column address/status after MBCLK1 no longer low	t_M-7		ns



† MBCLK1 and MBCLK2 have no timing relationship to OSCOUT. MBCLK1 and MBCLK2 can start on any OSCIN rising edge, depending on when the memory cycle starts execution.

Figure 5. Clock Waveforms After Clock Stabilization

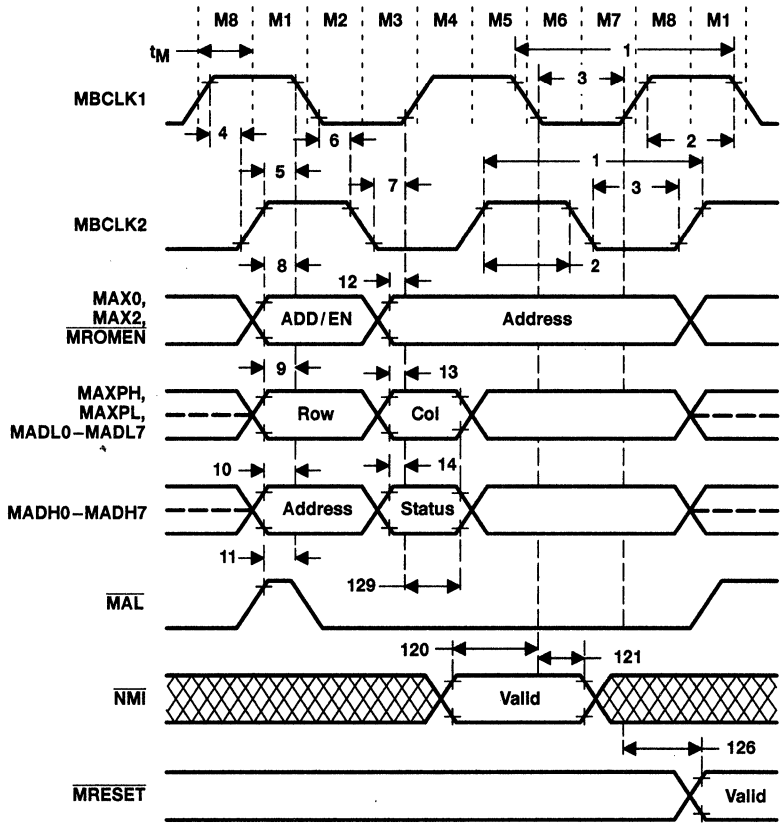


Figure 6. Memory-Bus Timing: Local-Memory Clocks, MAL, MROMEN, MBIAEN, NMI, MRESET, and AD DRESS

memory-bus timing: clocks, $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, and $\overline{\text{MAL}}$ to ADDRESS

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

NO.		MIN	MAX	UNIT
15	Setup time, row address on MADL0–MADL7, MAXPH, and MAXPL before $\overline{\text{MRAS}}$ no longer high	$1.5t_M - 11.5$		ns
16	Hold time, row address on MADL0–MADL7, MAXPH, and MAXPL after $\overline{\text{MRAS}}$ no longer high	$t_M - 6.5$		ns
17	Delay time, $\overline{\text{MRAS}}$ no longer high to $\overline{\text{MRAS}}$ no longer high in the next memory cycle	$8t_M$		ns
18	Pulse duration, $\overline{\text{MRAS}}$ low	$4.5t_M - 5$		ns
19	Pulse duration, $\overline{\text{MRAS}}$ high	$3.5t_M - 5$		ns
20	Setup time, column address (MADL0–MADL7, MAXPH, and MAXPL) and status (MADH0–MADH7) before $\overline{\text{MCAS}}$ no longer high	$0.5t_M - 9$		ns
21	Hold time, column address (MADL0–MADL7, MAXPH; and MAXPL) and status (MADH0–MADH7) after $\overline{\text{MCAS}}$ low	$t_M - 5$		ns
22	Hold time, column address (MADL0–MADL7, MAXPH, and MAXPL) and status (MADH0–MADH7) after $\overline{\text{MRAS}}$ no longer high	$2.5t_M - 6.5$		ns
23	Pulse duration, $\overline{\text{MCAS}}$ low	$3t_M - 9$		ns
24	Pulse duration, $\overline{\text{MCAS}}$ high, refresh cycle follows read or write cycle	$2t_M - 9$		ns
25	Hold time, row address on MAXL0–MAXL7, MAXPH, and MAXPL after $\overline{\text{MAL}}$ low	$1.5t_M - 9$		ns
26	Setup time, row address on MAXL0–MAXL7, MAXPH, and MAXPL before $\overline{\text{MAL}}$ no longer high	$t_M - 9$		ns
27	Pulse duration, $\overline{\text{MAL}}$ high	$t_M - 9$		ns
28	Setup time, address/enable on MAX0, MAX2, and $\overline{\text{MROMEN}}$ before $\overline{\text{MAL}}$ no longer high	$t_M - 9$		ns
29	Hold time, address/enable of MAX0, MAX2, and $\overline{\text{MROMEN}}$ after $\overline{\text{MAL}}$ low	$1.5t_M - 9$		ns
30	Setup time, address on MADH0–MADH7 before $\overline{\text{MAL}}$ no longer high	$t_M - 9$		ns
31	Hold time, address on MADH0–MADH7 after $\overline{\text{MAL}}$ low	$1.5t_M - 9$		ns

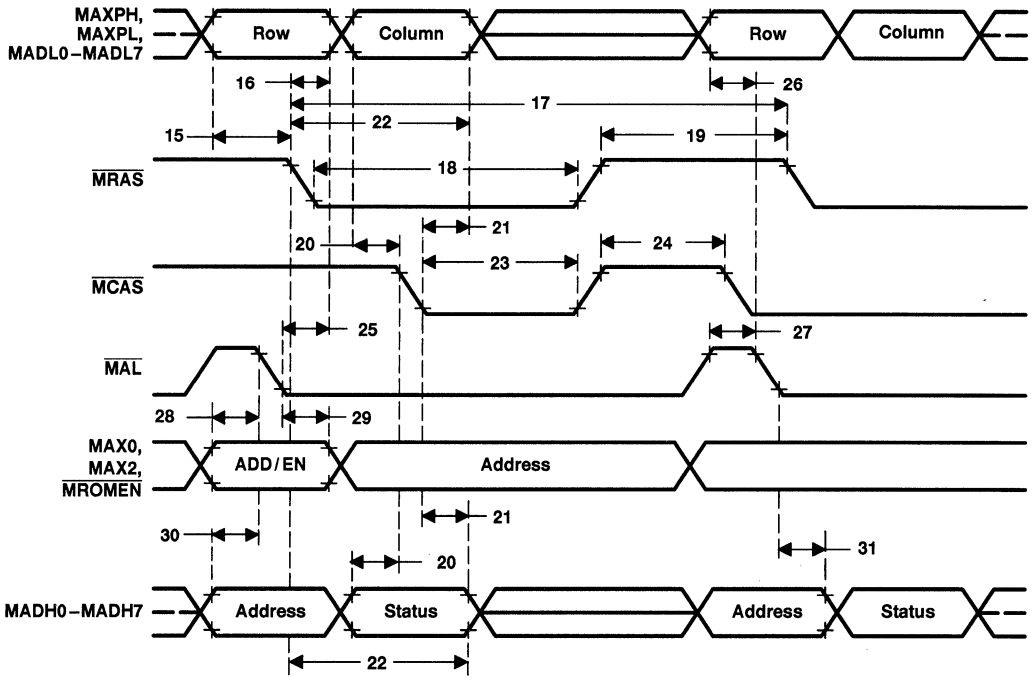


Figure 7. Memory-Bus Timing: Clocks, $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, and $\overline{\text{MAL}}$ to ADDRESS

memory-bus timing: read cycle

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

NO.		MIN	MAX	UNIT
32	Access time, address/enable valid on MAX0, MAX2, and $\overline{\text{MROMEN}}$ to valid data/parity		$6t_M - 23$	ns
33	Access time, address valid on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 to valid data/parity		$6t_M - 23$	ns
35	Access time, $\overline{\text{MRAS}}$ low to valid data/parity		$4.5t_M - 21.5$	ns
36	Hold time, valid data/parity after $\overline{\text{MRAS}}$ no longer low	0		ns
37†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7 and MADL0–MADL7 after $\overline{\text{MRAS}}$ high (see Note 16)	$2t_M - 10.5$		ns
38	Access time, $\overline{\text{MCAS}}$ low to valid data/parity		$3t_M - 23$	ns
39	Hold time, valid data/parity after $\overline{\text{MCAS}}$ no longer low	0		ns
40†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{\text{MCAS}}$ high (see Note 16)	$2t_M - 13$		ns
41	Delay time, $\overline{\text{MCAS}}$ no longer high to $\overline{\text{MOE}}$ low		$t_M + 13$	ns
42†	Setup time, address/status in the high-impedance state on MAXPH, MAXPL, MADL0–MADL7, and MADH0–MADH7 before $\overline{\text{MOE}}$ no longer high	0		ns
43	Access time, $\overline{\text{MOE}}$ low to valid data/parity		$2t_M - 20$	ns
44	Pulse duration, $\overline{\text{MOE}}$ low	$2t_M - 9$		ns
45	Delay time, $\overline{\text{MCAS}}$ low to $\overline{\text{MOE}}$ no longer low	$3t_M - 9$		ns
46	Hold time, valid data/parity in after $\overline{\text{MOE}}$ no longer low	0		ns
47†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{\text{MOE}}$ high (see Note 16)	$2t_M - 15$		ns
48†	Setup time, address/status in the high-impedance state on MAXPH, MAXPL, MADL0–MADL7, and MADH0–MADH7, before $\overline{\text{MBEN}}$ no longer high	0		ns
48a†	Setup time, address/status in the high-impedance state on MAXPH, MAXPL, MADL0–MADL7, and MADH0–MADH7 and before $\overline{\text{MBIAEN}}$ no longer high	0		ns
49	Access time, $\overline{\text{MBEN}}$ low to valid data/parity		$2t_M - 25$	ns
49a	Access time, $\overline{\text{MBIAEN}}$ low to valid data/parity		$2t_M - 25$	ns
50	Pulse duration, $\overline{\text{MBEN}}$ low	$2t_M - 9$		ns
50a	Pulse duration, $\overline{\text{MBIAEN}}$ low	$2t_M - 9$		ns
51	Hold time, valid data/parity after $\overline{\text{MBEN}}$ no longer low	0		ns
51a	Hold time, valid data/parity after $\overline{\text{MBIAEN}}$ no longer low	0		ns
52†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{\text{MBEN}}$ high (see Note 16)	$2t_M - 15$		ns
52a†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{\text{MBIAEN}}$ high	$2t_M - 15$		ns
53	Hold time, MDDIR high after $\overline{\text{MBEN}}$ high, read follows write cycle	$1.5t_M - 12$		ns
54	Setup time, MDDIR low before $\overline{\text{MBEN}}$ no longer high	$3t_M - 5$		ns
55	Hold time, MDDIR low after $\overline{\text{MBEN}}$ high, write follows read cycle	$3t_M - 12$		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.

NOTE 16: The data/parity that exists on the address lines will most likely reach the high-impedance state sometime later than the rising edge of $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, $\overline{\text{MOE}}$, or $\overline{\text{MBEN}}$ (between MIN and MAX of timing parameter 36) and will be a function of the memory being read. The MIN time given represents the time from the rising edge of $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, $\overline{\text{MOE}}$, or $\overline{\text{MBEN}}$ to the beginning of the next address, and does not represent the actual high-impedance period on the address bus.

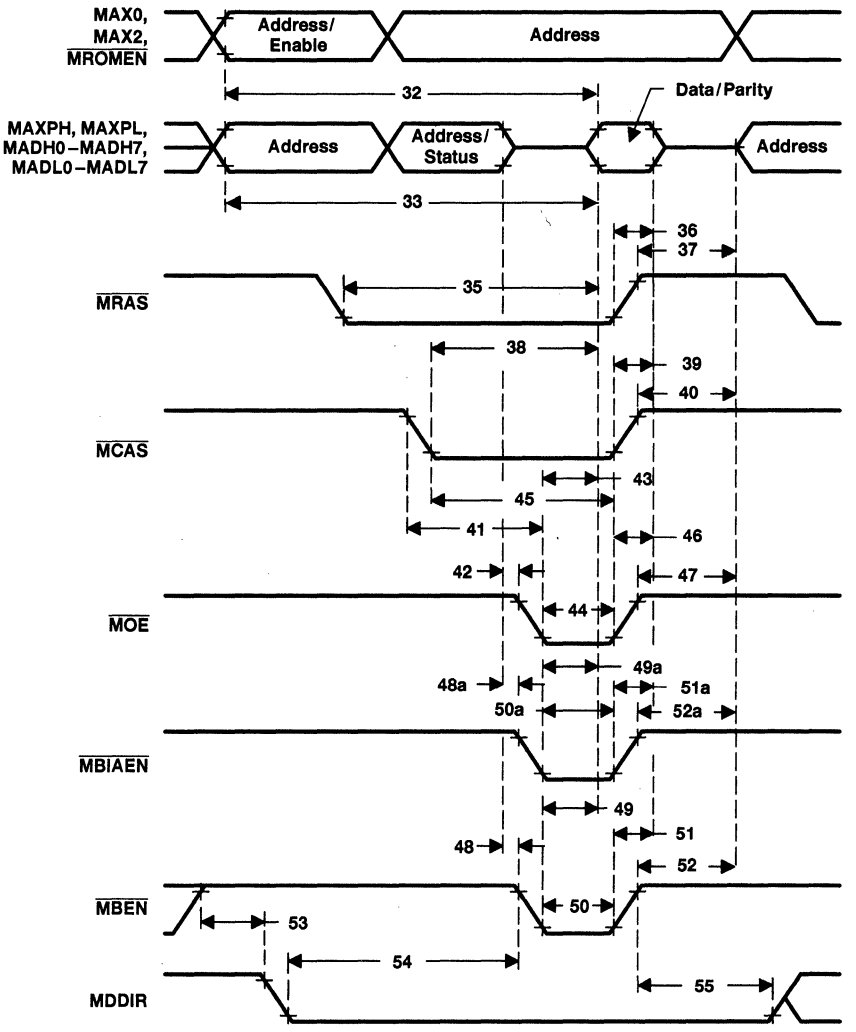


Figure 8. Memory-Bus Timing: Read Cycle

memory-bus timing: write cycle

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

NO.		MIN	MAX	UNIT
58	Setup time, $\overline{MW}$ low before $\overline{MRAS}$ no longer low	t_M		ns
60	Setup time, $\overline{MW}$ low before $\overline{MCAS}$ no longer low	$1.5t_M-6.5$		ns
63	Setup time, valid data/parity before $\overline{MW}$ no longer high	5.1		ns
64	Pulse duration, $\overline{MW}$ low	$2.5t_M-9$		ns
65	Hold time, data/parity out valid after $\overline{MW}$ high	$0.5t_M-10.5$		ns
66	Setup time, address valid on MAX0, MAX2, and $\overline{MROMEN}$ before $\overline{MW}$ no longer low	$7t_M-11.5$		ns
67	Hold time, $\overline{MRAS}$ low to $\overline{MW}$ no longer low	$5.5t_M-9$		ns
69	Hold time, $\overline{MCAS}$ low to $\overline{MW}$ no longer low	$4t_M-11.5$		ns
70	Setup time, $\overline{MBEN}$ low before $\overline{MW}$ no longer high	$1.5t_M-13.5$		ns
71	Hold time, $\overline{MBEN}$ low after $\overline{MW}$ high	$0.5t_M-6.5$		ns
72	Setup time, MDDIR high before $\overline{MBEN}$ no longer high	$2t_M-9$		ns
73	Hold time, MDDIR high after $\overline{MBEN}$ high	$1.5t_M-12$		ns

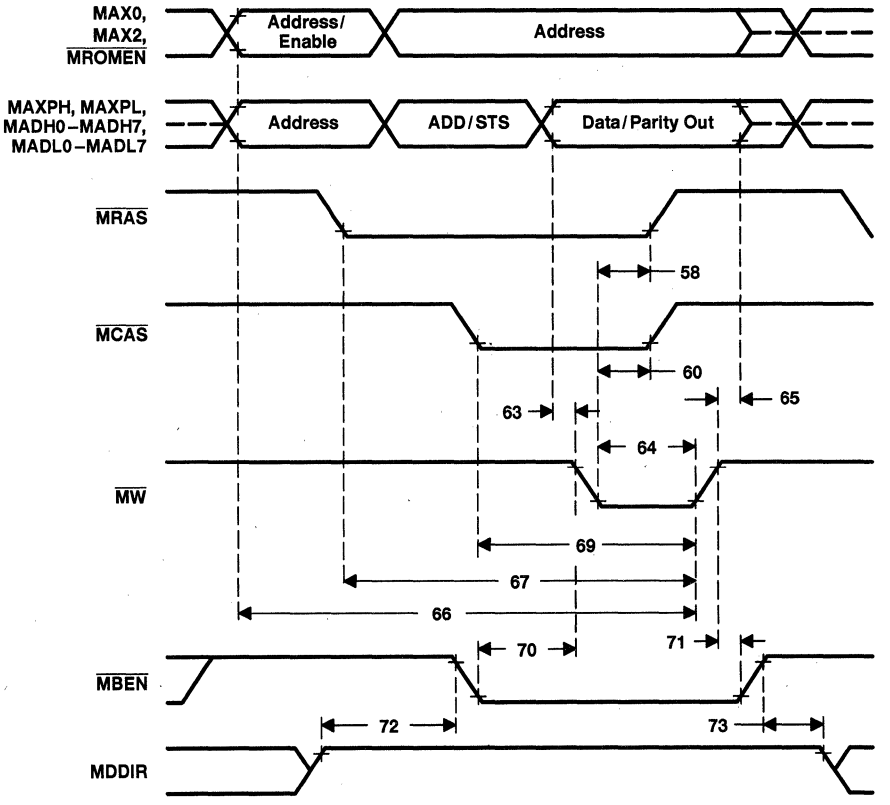


Figure 9. Memory-Bus Timing: Write Cycle

memory-bus timing: DRAM-refresh timing

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

NO.		MIN	MAX	UNIT
15	Setup time, row address on MADL0–MADL7, MAXPH, and MAXPL before $\overline{MRAS}$ no longer high	$1.5t_M-11.5$		ns
16	Hold time, row address on MADL0–MADL7, MAXPH, and MAXPL after $\overline{MRAS}$ no longer high	$t_M-6.5$		ns
18	Pulse duration, $\overline{MRAS}$ low	$4.5t_M-5$		ns
19	Pulse duration, $\overline{MRAS}$ high	$3.5t_M-5$		ns
73a	Setup time, $\overline{MCAS}$ low before $\overline{MRAS}$ no longer high	$1.5t_M-11.5$		ns
73b	Hold time, $\overline{MCAS}$ low after $\overline{MRAS}$ low	$4.5t_M-6.5$		ns
73c	Setup time, MREF high before $\overline{MCAS}$ no longer high	14		ns
73d	Hold time, MREF high after $\overline{MCAS}$ high	t_M-9		ns

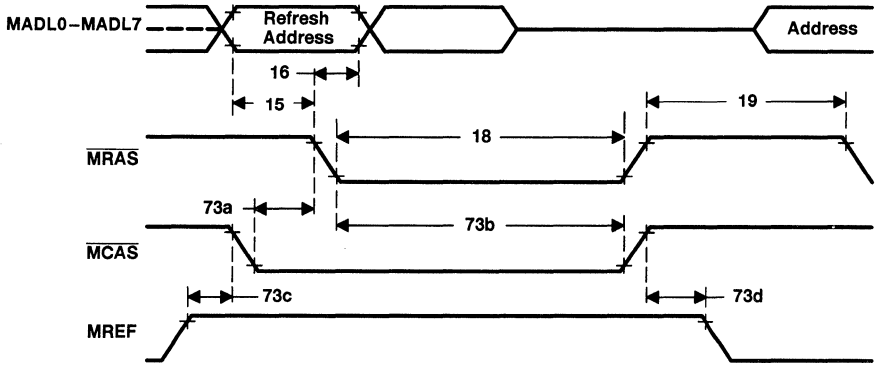


Figure 10. Memory-Bus Timing: DRAM-Refresh Cycle

XMATCH and XFAIL timing

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

NO.		MIN	MAX	UNIT
127	Delay time, status bit 7 high to XMATCH and XFAIL recognized	$7t_M$		ns
128	Pulse duration, XMATCH or XFAIL high	50		ns

Figure 11. XMATCH and XFAIL Timing

token ring: ring-interface timing

NO.			MIN	TYP	MAX	UNIT
153	Period of RCLK (see Note 17)	4Mbps		125		ns
		16 Mbps		31.25		ns
154L	Pulse duration, RCLK low	4 Mbps nominal: 62.5 ns	46			ns
		16 Mbps nominal: 15.625 ns	15			ns
154H	Pulse duration, RCLK high	4 Mbps nominal: 62.5 ns	35			ns
		16 Mbps nominal: 15.625 ns	8			ns
155	Setup time, RCVR valid before rising edge (1.8 V) of RCLK at 16 Mbps		10			ns
156	Hold time, RCVR valid after rising edge (1.8 V) of RCLK at 16 Mbps		4			ns
158L	Pulse duration, ring baud clock low	4 Mbps	40			ns
		16 Mbps	8			ns
158H	Pulse duration, ring baud clock high	4 Mbps	40			ns
		16 Mbps	8			ns
165	Period of OSCOUT and PXTALIN (see Note 17)	4 Mbps		125		ns
		16 Mbps (for PXTALIN only)		31.25		ns
	Tolerance of PXTALIN input frequency (see Note 17)				± 0.01	%

NOTE 17: This parameter is not tested but is required by the IEEE 802.5 specification.

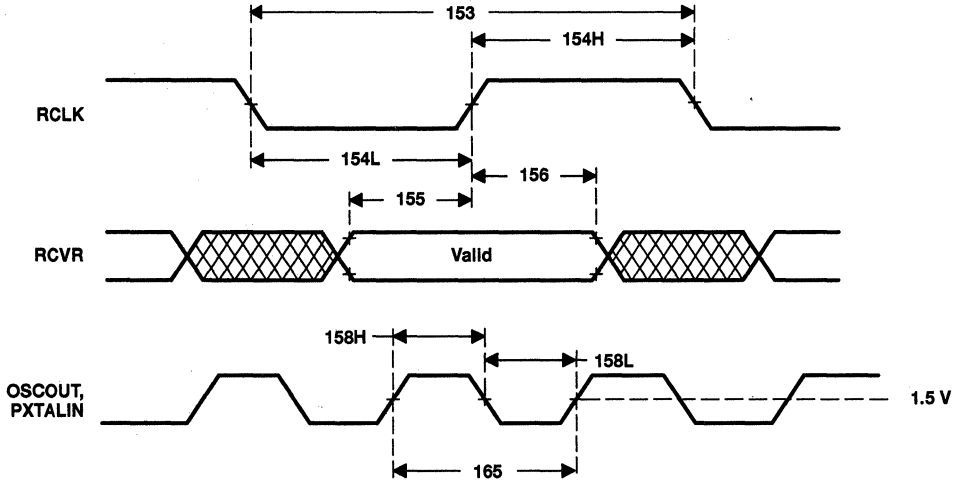


Figure 12. Ring-Interface Timing

token ring: transmitter timing

NO.			MIN MAX	UNIT
159	$t_{sk(DR)}$	Delay from DRVR rising edge (1.8 V) to $\overline{DRVR}$ falling edge (1 V) or DRVR falling edge (1 V) to $\overline{DRVR}$ rising edge (1.8 V)	±2	ns
160	$t_{d(DR)H}$†	Delay from RCLK (or PXTALIN) falling edge (1 V) to DRVR rising edge (1.8 V)	See Note 18	ns
161	$t_{d(DR)L}$†	Delay from RCLK (or PXTALIN) falling edge (1 V) to DRVR falling edge (1 V)	See Note 18	ns
162	$t_{d(DRN)H}$†	Delay from RCLK (or PXTALIN) falling edge (1 V) to $\overline{DRVR}$ falling edge (1 V)	See Note 18	ns
163	$t_{(DRN)L}$†	Delay from RCLK (or PXTALIN) falling edge (1 V) to $\overline{DRVR}$ rising edge (1.8 V)	See Note 18	ns
164	DRVR / $\overline{DRVR}$ asymmetry	$\frac{t_{d(DR)L} + t_{d(DRN)H}}{2} - \frac{t_{d(DR)H} + t_{d(DRN)L}}{2}$	±1.5	ns

† When in active-monitor mode, the clock source is PXTALIN; otherwise, the clock source is either RCLK or PXTALIN.
NOTE 18: This parameter is not tested to a minimum or a maximum but is measured and used as a component required for parameter 164.

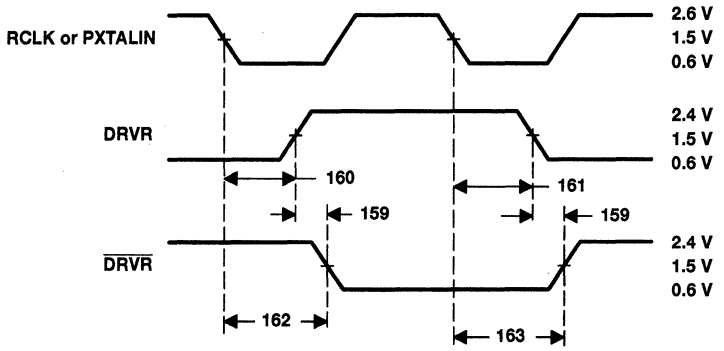


Figure 13. Skew and Asymmetry From RCLK or PXTALIN to DRVR and $\overline{DRVR}$

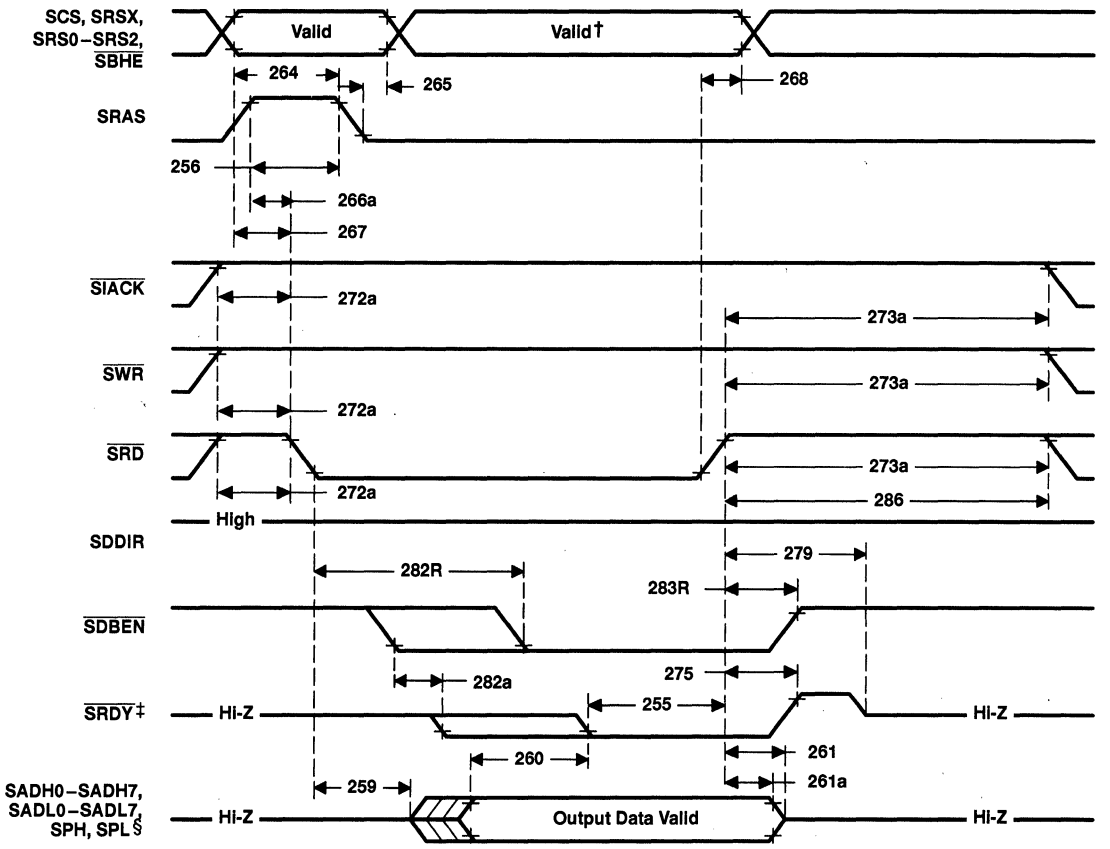
80x8x DIO read-cycle timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
255	Delay time, $\overline{SRDY}$ low to either $\overline{SCS}$ or $\overline{SRD}$ high	15		15		ns
256	Pulse duration, SRAS high	30		30		ns
259†	Hold time, SAD in the high-impedance state after $\overline{SRD}$ low (see Note 19)	0		0		ns
260	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before $\overline{SRDY}$ low	0		0		ns
261†	Delay time, $\overline{SRD}$ or $\overline{SCS}$ high to SAD in the high-impedance state (see Note 19)		35		35	ns
261a	Hold time, output data valid after $\overline{SRD}$ or $\overline{SCS}$ high (see Note 19)	0		0		ns
264	Setup time, SRSX, SRS0–SRS2, $\overline{SCS}$, and $\overline{SBHE}$ valid to SRAS no longer high (see Note 20)	30		30		ns
265	Hold time, SRSX, SRS0–SRS2, $\overline{SCS}$, and $\overline{SBHE}$ valid after SRAS low	10		10		ns
266a	Setup time, SRAS high to $\overline{SRD}$ no longer high (see Note 20)	15		15		ns
267‡	Setup time, SRSX, SRS0–SRS2 valid before $\overline{SRD}$ no longer high (see Note 19)	15		15		ns
268	Hold time, SRSX, SRS0–SRS2 valid after $\overline{SRD}$ no longer low (see Note 20)	0		0		ns
272a	Setup time, $\overline{SRD}$, $\overline{SWR}$, and $\overline{SIACK}$ high from previous cycle to $\overline{SRD}$ no longer high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
273a	Hold time, $\overline{SRD}$, $\overline{SWR}$, and $\overline{SIACK}$ high after $\overline{SRD}$ high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
275	Delay time, $\overline{SRD}$ and $\overline{SWR}$, or $\overline{SCS}$ high to $\overline{SRDY}$ high (see Note 19)	0	25	0	25	ns
279†	Delay time, $\overline{SRD}$ and $\overline{SWR}$, high to $\overline{SRDY}$ in the high-impedance state	0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
282a	Delay time, $\overline{SDBEN}$ low to $\overline{SRDY}$ low in a read cycle	0	$t_{c(SCK)} / 2 + 4$	0	$t_{c(SCK)} / 2 + 4$	ns
282R	Delay time, $\overline{SRD}$ low to $\overline{SDBEN}$ low (see *TMS380 Second Generation Token-Ring User's Guide*, SPWU005, subsection 3.4.1.1.1), provided previous cycle completed	0	$t_{c(SCK)} + 3$	0	$t_{c(SCK)} + 3$	ns
283R	Delay time, $\overline{SRD}$ high to $\overline{SDBEN}$ high (see Note 19)	0	$t_{c(SCK)} / 2 + 4$	0	$t_{c(SCK)} / 2 + 4$	ns
286	Pulse duration, $\overline{SRD}$ high between DIO accesses (see Note 19)	$t_{c(SCK)}$		$t_{c(SCK)}$		ns

† This specification is provided as an aid to board design. It is not assured during manufacturing testing.
‡ It is the later of $\overline{SRD}$ and $\overline{SWR}$ or $\overline{SCS}$ low that indicates the start of the cycle.

NOTES: 19. The inactive chip select is $\overline{SIACK}$ in DIO read and DIO write cycles, and $\overline{SCS}$ is the inactive chip select in interrupt-acknowledge cycles.

20. In 80x8x mode, SRAS can be used to strobe the values of $\overline{SBHE}$, SRSX, SRS0 – SRS2, and $\overline{SCS}$. When used to do so, SRAS must meet parameter 266a, and $\overline{SBHE}$, SRS0–SRS2, and $\overline{SCS}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.



† In 80x8x mode, SRAS can be used to strobe the values of $\overline{\text{SBHE}}$, SRSX, SRS0–SRS2, and $\overline{\text{SCS}}$. When used to do so, SRAS must meet parameter 266a, and $\overline{\text{SBHE}}$, SRS0–SRS2, and $\overline{\text{SCS}}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.

‡ When the TMS380C25 begins to drive $\overline{\text{SDBEN}}$ inactive, it has already latched the write data internally. Parameter 263 must be met to the input of the data buffers.

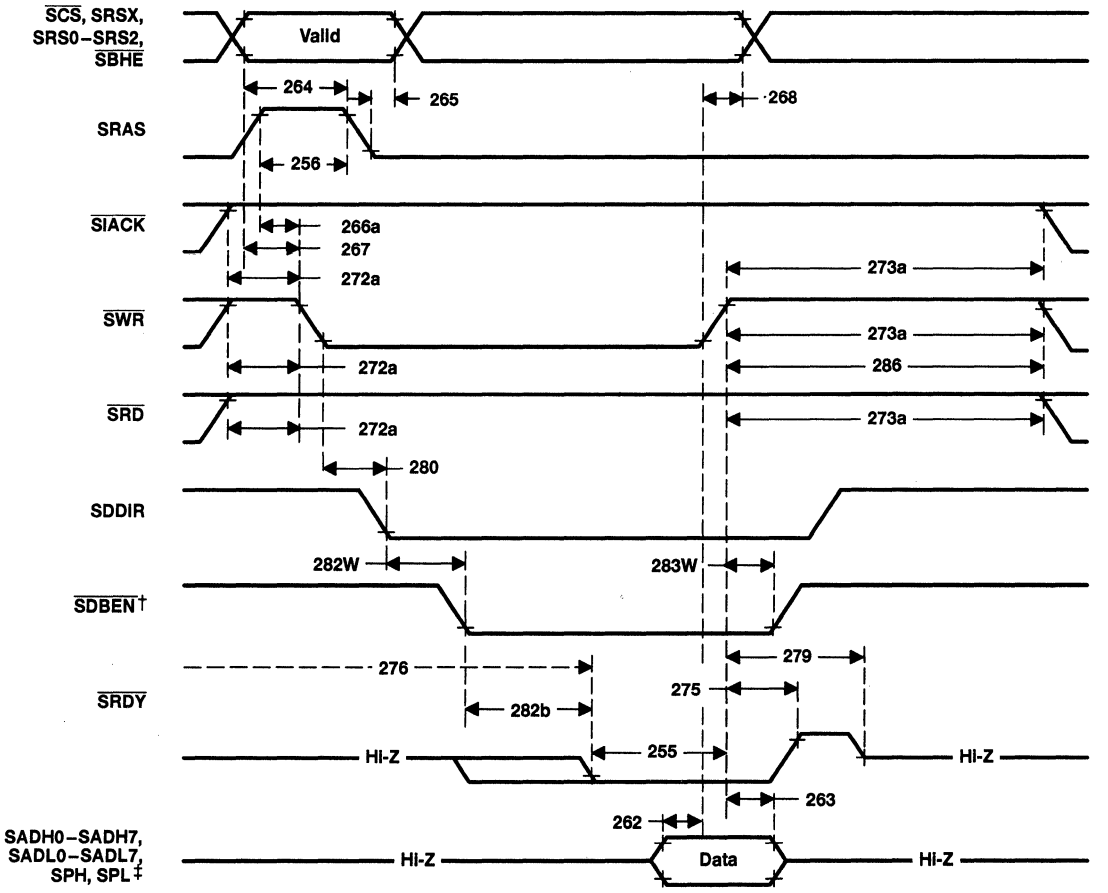
§ In 8-bit 80x8x mode DIO reads, the SADH0–SADH7 contain don't care data.

Figure 14. 80x8x DIO Read-Cycle Timing

80x8x DIO write-cycle timing

NO.			25-MHz OPERATION		33-MHz OPERATION		UNIT
			MIN	MAX	MIN	MAX	
255	Delay time, $\overline{SRDY}$ low to either $\overline{SCS}$ or $\overline{SWR}$ high		15		15		ns
256	Pulse duration, SRAS high		30		30		ns
262	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before $\overline{SCS}$ or $\overline{SWR}$ no longer low		15		15		ns
263	Hold time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid after $\overline{SCS}$ or $\overline{SWR}$ high		15		15		ns
264	Setup time, SRSX, SRS0–SRS2, $\overline{SCS}$, and $\overline{SBHE}$ to SRAS no longer high (see Note 20)		30		30		ns
265	Hold time, SRSX, SRS0–SRS2, $\overline{SCS}$, and $\overline{SBHE}$ after SRAS low		10		10		ns
266a	Setup time, SRAS high to $\overline{SWR}$ no longer high (see Note 19)		15		15		ns
267†	Setup time, SRSX, SRS0–SRS2 before $\overline{SWR}$ no longer high (see Note 19)		15		15		ns
268	Hold time, SRSX, SRS0–SRS2 valid after $\overline{SWR}$ no longer low (see Note 20)		0		0		ns
272a	Setup time, $\overline{SRD}$, $\overline{SWR}$, and $\overline{SIACK}$ high from previous cycle to $\overline{SWR}$ no longer high		$t_{c(SCK)}$		$t_{c(SCK)}$		ns
273a	Hold time, $\overline{SRD}$, $\overline{SWR}$, and $\overline{SIACK}$ high after $\overline{SWR}$ high		$t_{c(SCK)}$		$t_{c(SCK)}$		ns
276‡	Delay time, $\overline{SRDY}$ low in the first DIO access to the SIF register to $\overline{SRDY}$ low in the immediately following access to the SIF (see *TMS380 Second-Generation Token Ring User's Guide*, SPWU005, subsection 3.4.1.1.1)			4000		4000	ns
275	Delay time, $\overline{SWR}$ or $\overline{SCS}$ high to $\overline{SRDY}$ high (see Note 19)		0	25	0	25	ns
279§	Delay time, $\overline{SWR}$ high to $\overline{SRDY}$ in the high-impedance state		0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
280	Delay time, $\overline{SWR}$ low to SDDIR low (see Note 19)		0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
282b	Delay time, SDBEN low to SRDY low (see *TMS380 Second Generation Token-Ring User's Guide*, SPWU005, subsection 3.4.1.1.1)	If SIF register is ready (no waiting required)	0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
		If SIF register is not ready (waiting required)	0	4000	0	4000	
282W	Delay time, SDDIR low to $\overline{SDBEN}$ low		0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
283W	Delay time, $\overline{SCS}$ or $\overline{SWR}$ high to $\overline{SDBEN}$ no longer low		0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
286	Pulse duration, $\overline{SWR}$ high between DIO accesses (see Note 19)		$t_{c(SCK)}$		$t_{c(SCK)}$		ns

† It is the later of $\overline{SRD}$ and $\overline{SWR}$ or $\overline{SCS}$ low that indicates the start of the cycle.
‡ This specification has been characterized to meet stated value. It is not assured during manufacturing testing.
§ This specification is provided as an aid to board design. It is not assured during manufacturing testing.
NOTES: 19. The inactive chip select is $\overline{SIACK}$ in DIO read and DIO write cycles, and $\overline{SCS}$ is the inactive chip select in interrupt-acknowledge cycles.
20. In 80x8x mode, SRAS can be used to strobe the values of $\overline{SBHE}$, SRSX, SRS0–SRS2, and $\overline{SCS}$. When used to do so, SRAS must meet parameter 266a, and $\overline{SBHE}$, SRS0–SRS2, and $\overline{SCS}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.



† When the TMS380C25 begins to drive $\overline{\text{SDBEN}}$ inactive, it has already latched the write data internally. Parameter 263 must be met to the input of the data buffers.

‡ In 8-bit 80x8x-mode DIO writes, the value placed on SADH0–SADH7 is a don't care.

Figure 15. 80x8x DIO Write-Cycle Timing

80x8x interrupt-acknowledge-cycle timing: first $\overline{\text{SIACK}}$ pulse

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
286	Pulse duration, $\overline{\text{SIACK}}$ high between DIO accesses (see Note 19)	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
287	Pulse duration, $\overline{\text{SIACK}}$ low on first pulse of two pulses	$t_{c(SCK)}$		$t_{c(SCK)}$		ns

NOTE 19: The inactive chip select is $\overline{\text{SIACK}}$ in DIO read and DIO write cycles, and $\overline{\text{SCS}}$ is the inactive chip select in interrupt acknowledge cycles.

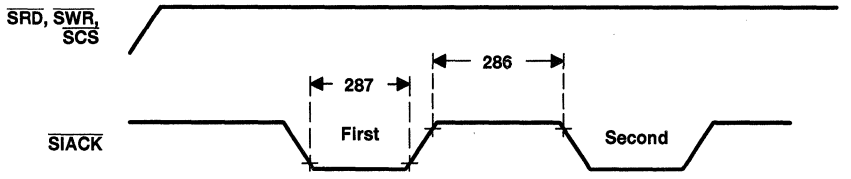
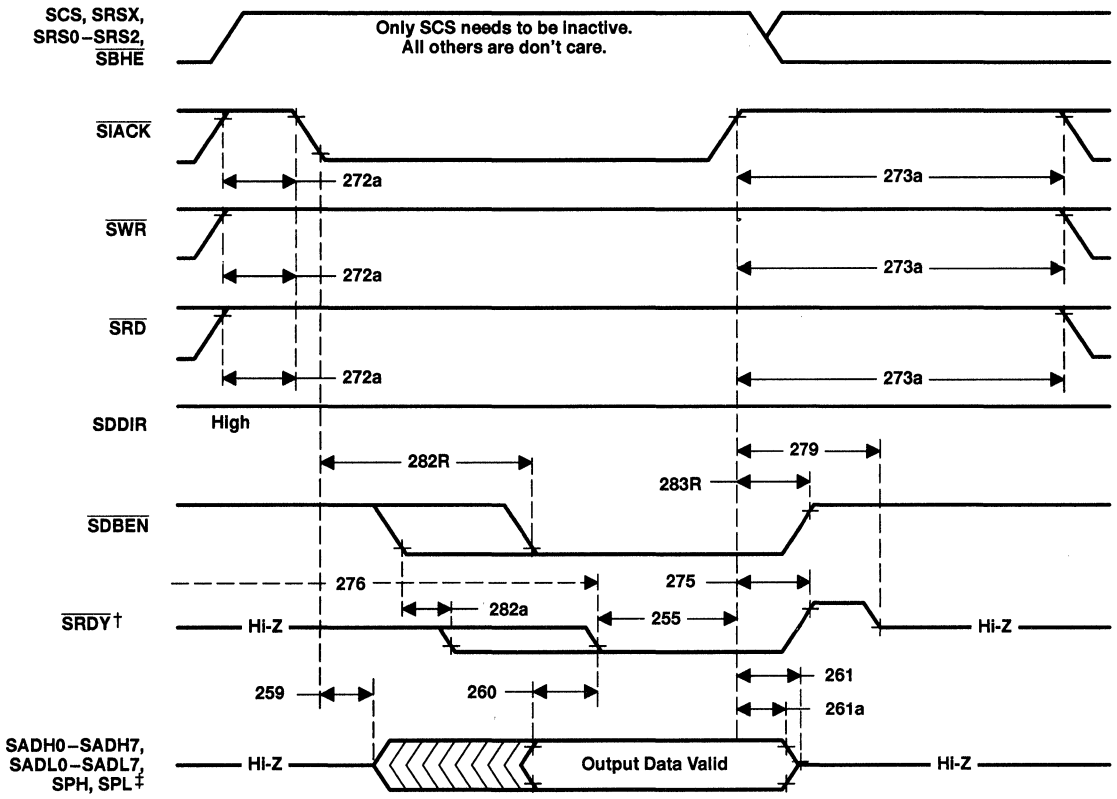


Figure 16. 80x8x Interrupt-Acknowledge-Cycle Timing: First $\overline{\text{SIACK}}$ Pulse

80x8x interrupt-acknowledge-cycle timing: second $\overline{\text{SIACK}}$ pulse

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
255	Delay time, $\overline{\text{SRDY}}$ low to $\overline{\text{SCS}}$ high	15		15		ns
259†	Hold time, SAD in the high-impedance state after $\overline{\text{SIACK}}$ low (see Note 19)	0		0		ns
260	Setup time, output data valid before $\overline{\text{SRDY}}$ low	0		0		ns
261†	Delay time, $\overline{\text{SIACK}}$ high to SAD in the high-impedance state (see Note 19)		35		35	ns
261a	Hold time, output data valid after $\overline{\text{SIACK}}$ high (see Note 19)	0		0		ns
272a	Setup time, inactive data strobe high to $\overline{\text{SIACK}}$ no longer high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
273a	Hold time, inactive data strobe high after $\overline{\text{SIACK}}$ high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
275	Delay time, $\overline{\text{SIACK}}$ high to $\overline{\text{SRDY}}$ high (see Note 19)	0	25	0	25	ns
276‡	Delay time, $\overline{\text{SRDY}}$ low in the first DIO access to the SIF register to $\overline{\text{SRDY}}$ low in the immediately following access to the SIF		4000		4000	ns
279†	Delay time, $\overline{\text{SIACK}}$ high to $\overline{\text{SRDY}}$ in the high-impedance state	0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
282a	Delay time, $\overline{\text{SDBEN}}$ low to $\overline{\text{SRDY}}$ low in a read cycle	0	$t_{c(SCK)} / 2 + 4$	0	$t_{c(SCK)} / 2 + 4$	ns
282R	Delay time, $\overline{\text{SIACK}}$ low to $\overline{\text{SDBEN}}$ low (see *TMS380 Second Generation Token-Ring User's Guide*, SPWU005, subsection 3.4.1.1.1), provided previous cycle completed	0	$t_{c(SCK)} + 3$	0	$t_{c(SCK)} + 3$	ns
283R	Delay time, $\overline{\text{SIACK}}$ high to $\overline{\text{SDBEN}}$ high (see Note 19)	0	$t_{c(SCK)} / 2 + 4$	0	$t_{c(SCK)} / 2 + 4$	ns

† This specification is provided as an aid to board design. It is not assured during manufacturing.
‡ This specification has been characterized to meet stated value. It is not assured during manufacturing.
NOTE 19: The inactive chip select is $\overline{\text{SIACK}}$ in DIO read and DIO write cycles, and $\overline{\text{SCS}}$ is the inactive chip select in interrupt-acknowledge cycles.



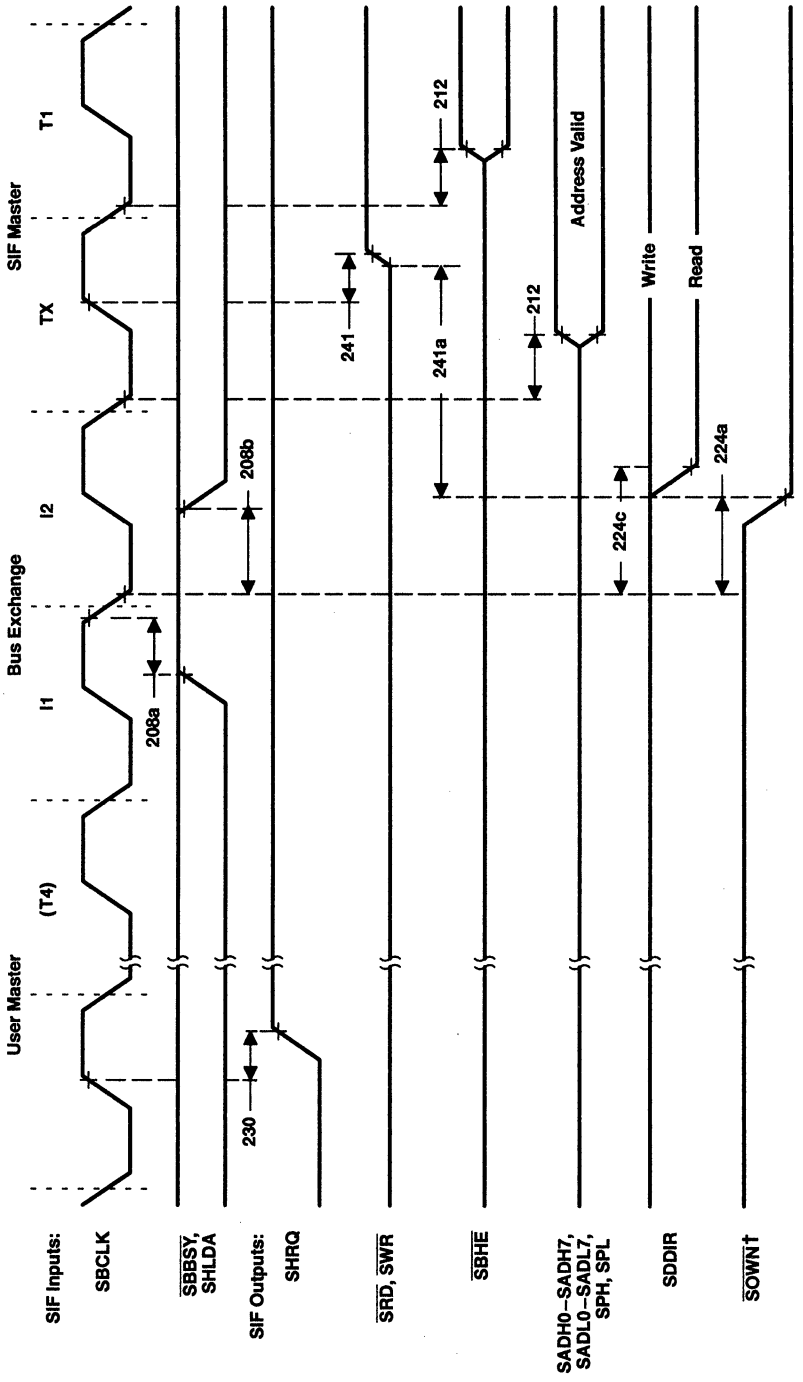
† $\overline{\text{SRDY}}$ is an active-low bus ready signal. It must be asserted before data output.
‡ In 8-bit 80x8x mode DIO writes, the value placed on SADH0–SADH7 is a don't care.

Figure 17. 80x8x Interrupt-Acknowledge-Cycle Timing: Second $\overline{\text{SIACK}}$ Pulse

80x8x-mode bus-arbitration timing, SIF takes control

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous signal $\overline{\text{SBBSY}}$ and SHLDA before SBCLK no longer high to assure recognition on that cycle	10		10		ns
208b	Hold time, asynchronous signal $\overline{\text{SBBSY}}$ and SHLDA after SBCLK low to assure recognition on that cycle	10		10		ns
212	Delay time, SBCLK low to SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid		20		20	ns
224a	Delay time, SBCLK low in cycle I2 to $\overline{\text{SOWN}}$ low	0	20	0	15	ns
224c	Delay time, SBCLK low in cycle I2 to SDDIR low in DMA read		28		23	ns
230	Delay time, SBCLK high to SHRQ high		20		15	ns
241	Delay time, SBCLK high in TX cycle to $\overline{\text{SRD}}$ and $\overline{\text{SWR}}$ high, bus acquisition		25		25	ns
241a†	Hold time, SRD and $\overline{\text{SWR}}$ in the high-impedance state after $\overline{\text{SOWN}}$ low, bus acquisition	$t_{c(SCK)}-15$		$t_{c(SCK)}-15$		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.



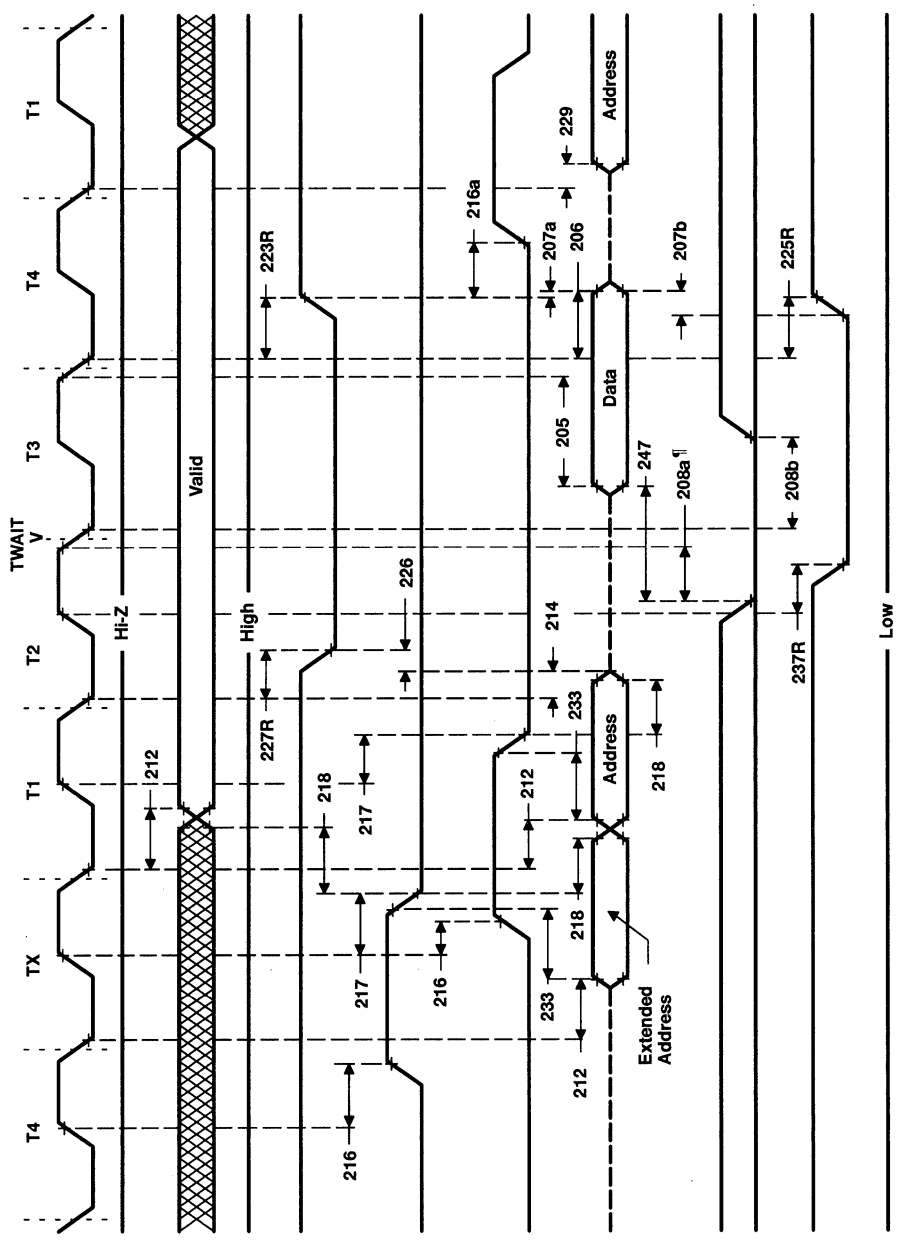
† While the system interface DMA controls are active (i.e., $\overline{SOWN}$ is asserted), the $\overline{SCS}$ input is disabled.

Figure 1. 80x8x-Mode Bus-Arbitration Timing, SIF Takes Control

80x8x-mode DMA read-cycle timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
205	Setup time, SADL0–SADL7, SADH0–SADH7, SPH, and SPL valid before SBCLK in T3 cycle no longer high	10		10		ns
206	Hold time, SADL0–SADL7, SADH0–SADH7, SPH, and SPL valid after SBCLK low in T4 cycle if parameters 207a and 207b not met	10		10		ns
207a	Hold time, SADL0–SADL7, SADH0–SADH7, SPH, and SPL valid after $\overline{SRD}$ high	0		0		ns
207b	Hold time, SADL0–SADL7, SADH0–SADH7, SPH, and SPL valid after $\overline{SDBEN}$ no longer low	0		0		ns
208a	Setup time, asynchronous signal $\overline{SRDY}$ before SBCLK no longer high to assure recognition on this cycle	10		10		ns
208b	Hold time, asynchronous signal $\overline{SRDY}$ after SBCLK low to assure recognition on this cycle	10		10		ns
212	Delay time, SBCLK low to address valid		20		20	ns
214†	Delay time, SBCLK low in T1 cycle to SADH0–SADH7, SADL0–SADL7, SPH, and SPL in the high-impedance state		20		15	ns
216	Delay time, SBCLK high to SALE or SXAL high		20		20	ns
216a	Hold time, SALE or SXAL low after $\overline{SRD}$ high	0		0		ns
217	Delay time, SBCLK high to SXAL low in the TX cycle or SALE low in the T1 cycle	0	25	0	25	ns
218	Hold time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid after SALE or SXAL low	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	ns
223R	Delay time, SBCLK low in T4 cycle to $\overline{SRD}$ high (see Note 21)	0	16	0	11	ns
225R	Delay time, SBCLK low in T4 cycle to $\overline{SDBEN}$ high		16		11	ns
226†	Delay time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL in the high-impedance state to $\overline{SRD}$ low	0		0		ns
227R	Delay time, SBCLK low in T2 cycle to $\overline{SRD}$ low	0	15	0	15	ns
229†	Hold time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL in the high-impedance state after SBCLK low in T1 cycle	0		0		ns
231	Pulse duration, $\overline{SRD}$ low	$2t_{c(SCK)}-25$		$2t_{c(SCK)}-25$		ns
233	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before SALE, SXAL no longer high	10		10		ns
237R	Delay time, SBCLK high in the T2 cyle to $\overline{SDBEN}$ low		16		11	ns
247	Setup time, data valid before $\overline{SRDY}$ low if parameter 208a not met	0		0		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.
NOTE 21: While the system-interface DMA controls are active (i.e., $\overline{SOWN}$ is asserted), $\overline{SCS}$ is disabled.

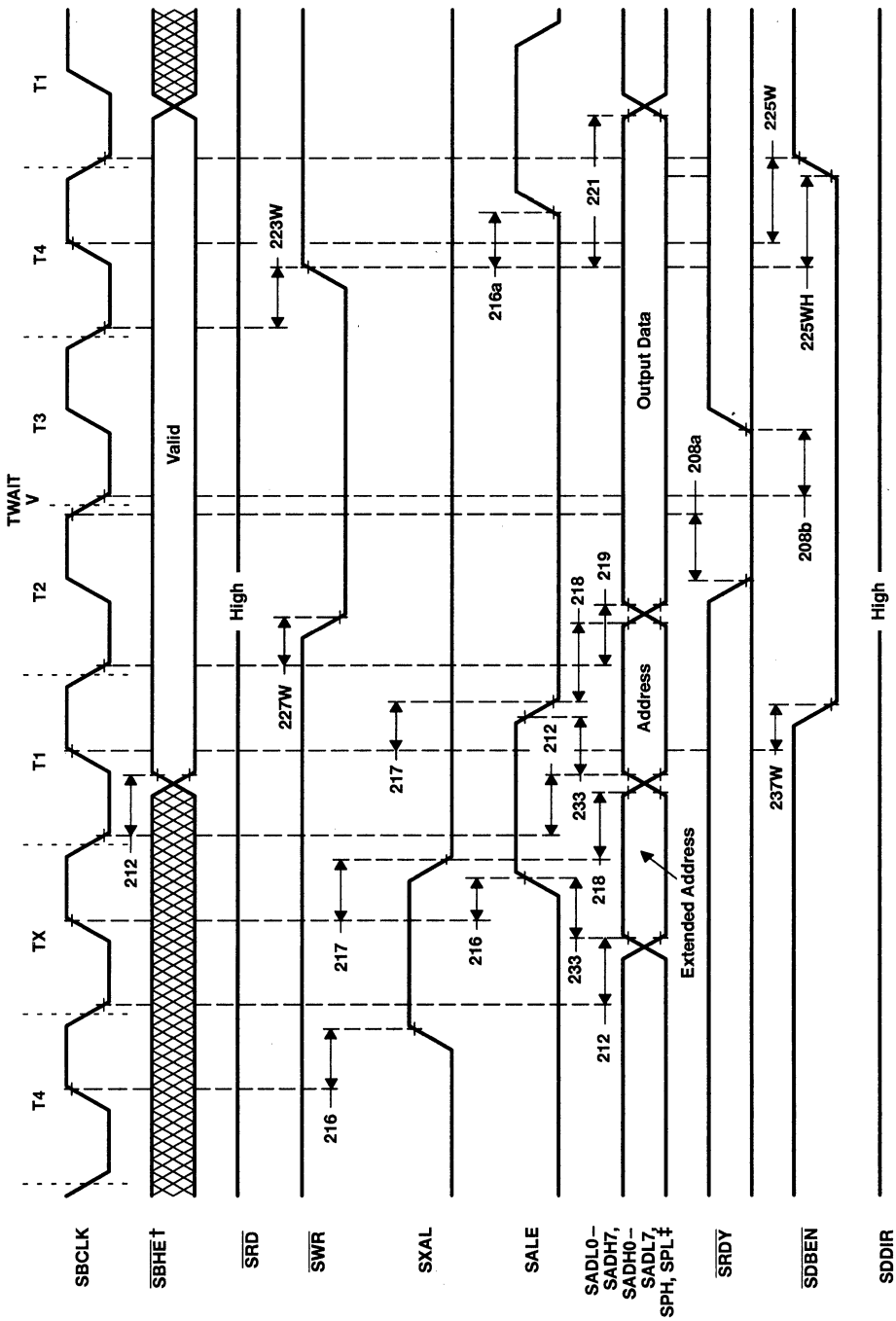


† In 8-bit 80x8x mode, $\overline{SBHE}$/SRNW is a don't care input during DIO and an inactive (high) output during DMA.
‡ Motorola-style bus slaves hold $\overline{SDTACK}$ active until the bus master deasserts SAS.
§ In 8-bit 80x8x mode, the most significant byte of the address is maintained on SADH for T2, T3, and T4. The address is maintained according to parameter 21; i.e., held after T4 high.
¶ If parameter 208A is not met, valid data must be present before $\overline{SRDY}$ goes low.

Figure 19. 80x8x-Mode DMA Read-Cycle Timing

80x8x-mode DMA write-cycle timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous signal $\overline{SRDY}$ before SBCLK no longer high to assure recognition on that cycle	10		10		ns
208b	Hold time, asynchronous signal $\overline{SRDY}$ after SBCLK low to assure recognition on that cycle	10		10		ns
212	Delay time, SBCLK low to SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid		20		20	ns
216	Delay time, SBCLK high to SALE or SXAL high		20		20	ns
216a	Hold time, SALE or SXAL low after $\overline{SWR}$ high	0		0		ns
217	Delay time, SBCLK high to SXAL low in the TX cycle or SALE low in the T1 cycle	0	25	0	25	ns
218	Hold time, address valid after SALE, SXAL low	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	ns
219	Delay time, SBCLK low in T2 cycle to output data and parity valid		29		29	ns
221	Hold time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid after $\overline{SWR}$ high	$t_{c(SCK)}-12$		$t_{c(SCK)}-12$		ns
223W	Delay time, SBCLK low to $\overline{SWR}$ high	0	16	0	11	ns
225W	Delay time, SBCLK high in T4 cycle to $\overline{SDBEN}$ high		16		11	ns
225WH	Hold time, $\overline{SDBEN}$ low after $\overline{SWR}$, $\overline{SUDS}$, and $\overline{SLDS}$ high	$t_{c(SCK)}/2-7$		$t_{c(SCK)}/2-7$		ns
227W	Delay time, SBCLK low in T2 cycle to $\overline{SWR}$ low	0	20	0	15	ns
233	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before SALE, SXAL no longer high	10		10		ns
237W	Delay time, SBCLK high in T1 cycle to $\overline{SDBEN}$ low		16		11	ns



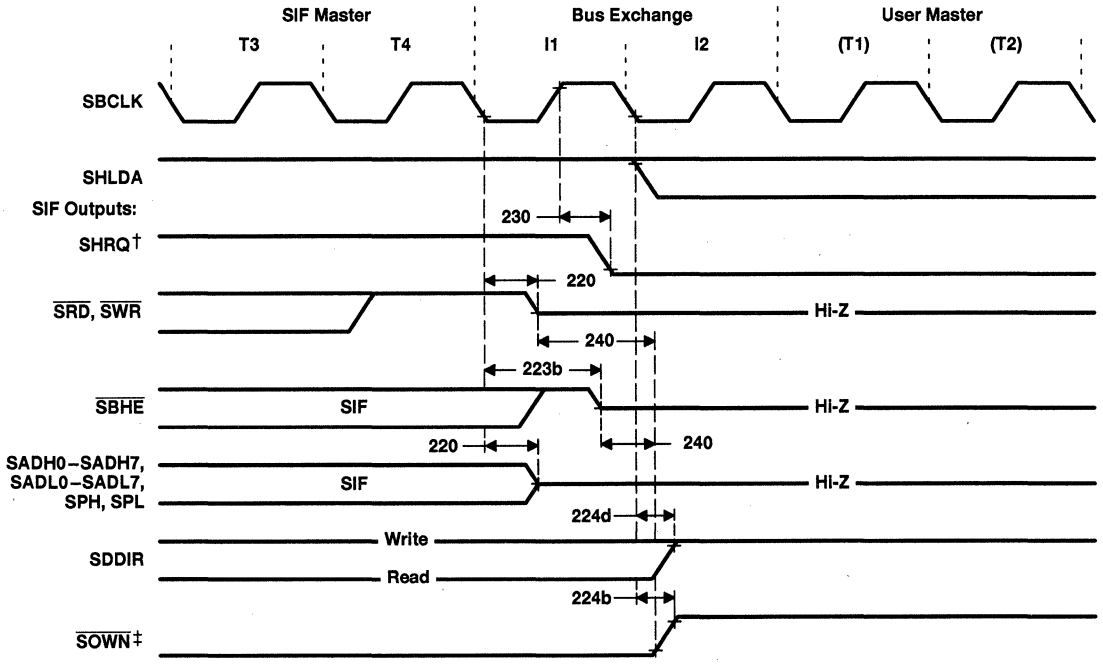
† In 8-bit 80x8x mode, $\overline{SBHE}$/SRNW is a don't care input during DIO and an inactive (high) output during DMA.
‡ In 8-bit 80x8x mode, the most significant byte of the address is maintained on SADH for T2, T3, and T4. The address is maintained according to parameter 21; i.e., held after T4 high.

Figure 20. 80x8x-Mode DMA Write-Cycle Timing

80x8x-mode bus-arbitration timing, SIF returns control

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
220†	Delay time, SBCLK low in I1 cycle to SADH0–SADH7, SADL0–SADL7, SPL, SPH, $\overline{SRD}$, and $\overline{SWR}$ in the high-impedance state		35		35	ns
223b†	Delay time, SBCLK low in I1 cycle to $\overline{SBHE}$ in the high-impedance state		45		45	ns
224b	Delay time, SBCLK low in cycle I2 to $\overline{SOWN}$ high	0	20	0	15	ns
224d	Delay time, SBCLK low in cycle I2 to SDDIR high		27		22	ns
230	Delay time, SBCLK high in cycle I1 to SHRQ low		20		15	ns
240†	Setup time, $\overline{SRD}$, $\overline{SWR}$, and $\overline{SBHE}$ in the high-impedance state before $\overline{SOWN}$ no longer low	0		0		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.

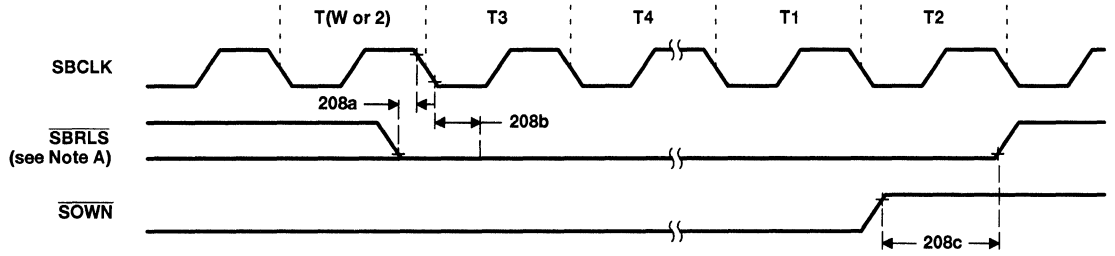


† In 80x8x mode, the system interface deasserts SHRQ on the rising edge of SBCLK following the T4 state of the last system bus transfer it controls. In 68xxx mode, the system interface deasserts $\overline{SBRQ}$ on the rising edge of SBCLK in state T2 of the first system bus transfer it controls.
‡ While the system-interface DMA controls are active (i.e., $\overline{SOWN}$ is asserted), $\overline{SCS}$ is disabled.

Figure 21. 80x8x-Mode Bus-Arbitration Timing, SIF Returns Control

80x8x-mode bus-release timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous input $\overline{\text{SBRLS}}$ low before SBCLK no longer high to assure recognition	10		10		ns
208b	Hold time, asynchronous input $\overline{\text{SBRLS}}$ low after SBCLK low to assure recognition	10		10		ns
208c	Hold time, $\overline{\text{SBRLS}}$ low after $\overline{\text{SOWN}}$ high	0		0		ns



NOTES: A. The system interface ignores the assertion of $\overline{\text{SBRLS}}$ if it does not own the system bus. If it does own the bus, when it detects the assertion of $\overline{\text{SBRLS}}$, it completes any internally started DMA cycle and relinquishes control of the bus. If no DMA transfer has internally started, the system interface releases the bus before starting another.

B. If $\overline{\text{SBERR}}$ is asserted when the system interface controls the system bus, the current bus transfer is completed regardless of the value of $\overline{\text{SRDY}}$. If the BERETRY register is nonzero, the cycle is retried. If the BERETRY register is zero, the system interface releases control of the system bus. The system interface ignores the assertion of $\overline{\text{SBERR}}$ if it is not performing a DMA bus cycle on the system bus. When $\overline{\text{SBERR}}$ is properly asserted and BERETRY is zero, the system interface releases the bus upon completion of the current bus transfer and halts all further DMA on the system side. The error is synchronized to the local bus and DMA stops on the local sides. The value of the SDMAADR, SDMADDRX, and SDMALEN registers in the system interface are not defined after a system-bus error.

C. In cycle-steal mode, state TX is present on every system bus transfer. In burst mode, state TX is present on the first bus transfer and whenever the increment of the DMA address register carries beyond the least significant 16 bits.

D. $\overline{\text{SDTACK}}$ is not sampled to verify that it is deasserted.

E. Unless otherwise specified, for all signals specified as a maximum delay from the end of an SBCLK transition to the signal valid, the signal is also specified to hold its previous value (including high impedance) until the start of that SBCLK transition.

Figure 22. 80x8x-Mode Bus-Release Timing

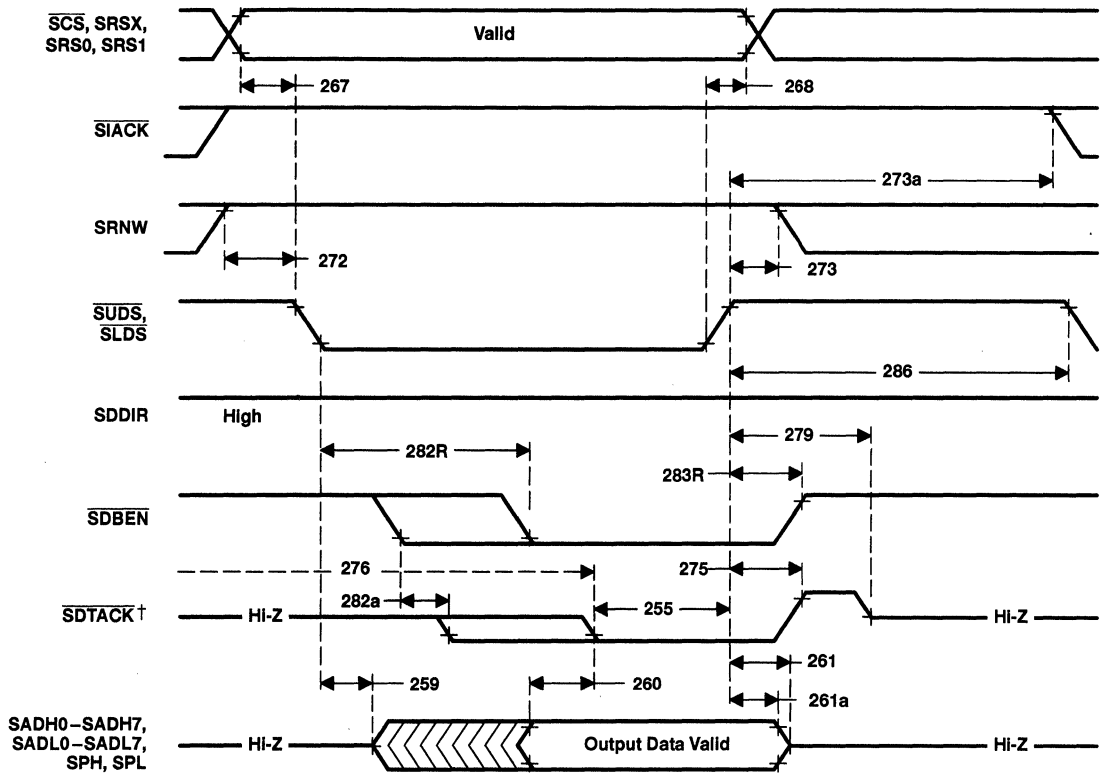
68xxx DIO read-cycle timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
255	Delay time, $\overline{SDTACK}$ low to either $\overline{SCS}$, $\overline{SUDS}$, or $\overline{SLDS}$ high	15		15		ns
259†	Hold time, SAD in the high-impedance state after $\overline{SUDS}$ or $\overline{SLDS}$ low (see Note 19)	0		0		ns
260	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before $\overline{SDTACK}$ low	0		0		ns
261†	Delay time, $\overline{SCS}$, $\overline{SUDS}$, or $\overline{SLDS}$ high to SADH0–SADH7, SADL0–SADL7, SPH, and SPL in the high-impedance state (see Note 19)		35		35	ns
261a	Hold time, output data valid after $\overline{SUDS}$ or $\overline{SLDS}$ no longer low (see Note 19)	0		0		ns
267	Setup time, register address before $\overline{SUDS}$ or $\overline{SLDS}$ no longer high (see Note 19)	15		15		ns
268	Hold time, register address valid after $\overline{SUDS}$ or $\overline{SLDS}$ no longer low (see Note 20)	0		0		ns
272	Setup time, SRNW before $\overline{SUDS}$ or $\overline{SLDS}$ no longer high (see Note 19)	12		12		ns
273	Hold time, SRNW after $\overline{SUDS}$ or $\overline{SLDS}$ high	0		0		ns
273a	Hold time, $\overline{SIACK}$ high after $\overline{SUDS}$ or $\overline{SLDS}$ high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
275	Delay time, $\overline{SCS}$, $\overline{SUDS}$, or $\overline{SLDS}$ high to $\overline{SDTACK}$ high (see Note 19)	0	25	0	25	ns
276‡	Delay time, $\overline{SDTACK}$ low in the first DIO access to the SIF register to $\overline{SDTACK}$ low in the immediately following access to the SIF		4000		4000	ns
279†	Delay time, $\overline{SUDS}$ or $\overline{SLDS}$ high to $\overline{SDTACK}$ in the high-impedance state	0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
282a	Delay time, $\overline{SDBEN}$ low to $\overline{SDTACK}$ low	0	$t_{c(SCK)}/2 + 4$	0	$t_{c(SCK)}/2 + 4$	ns
282R	Delay time, $\overline{SUDS}$ or $\overline{SLDS}$ low to $\overline{SDBEN}$ low (see *TMS380 Second Generation Token-Ring User's Guide*, SPWU005, subsection 3.4.1.1.1) provided the previous cycle completed	0	$t_{c(SCK)} + 3$	0	$t_{c(SCK)} + 3$	ns
283R	Delay time, $\overline{SUDS}$ or $\overline{SLDS}$ high to $\overline{SDBEN}$ high (see Note 19)	0	$t_{c(SCK)}/2 + 4$	0	$t_{c(SCK)}/2 + 4$	ns
286	Pulse duration, $\overline{SUDS}$ or $\overline{SLDS}$ high between DIO accesses (see Note 19)	$t_{c(SCK)}$		$t_{c(SCK)}$		ns

† This specification is provided as an aid to board design. It is not assured during manufacturing testing.
‡ This specification has been characterized to meet stated value. It is not assured during manufacturing testing.

NOTES: 19. The inactive chip select is $\overline{SIACK}$ in DIO read and DIO write cycles, and $\overline{SCS}$ is the inactive chip select in interrupt acknowledge cycles.

20. In 80x8x mode, SRAS may be used to strobe the values of $\overline{SBHE}$, SRSX, SRS0–SRS2, and $\overline{SCS}$. When used to do so, SRAS must meet parameter 266a, and $\overline{SBHE}$, SRS0–SRS2, and $\overline{SCS}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.



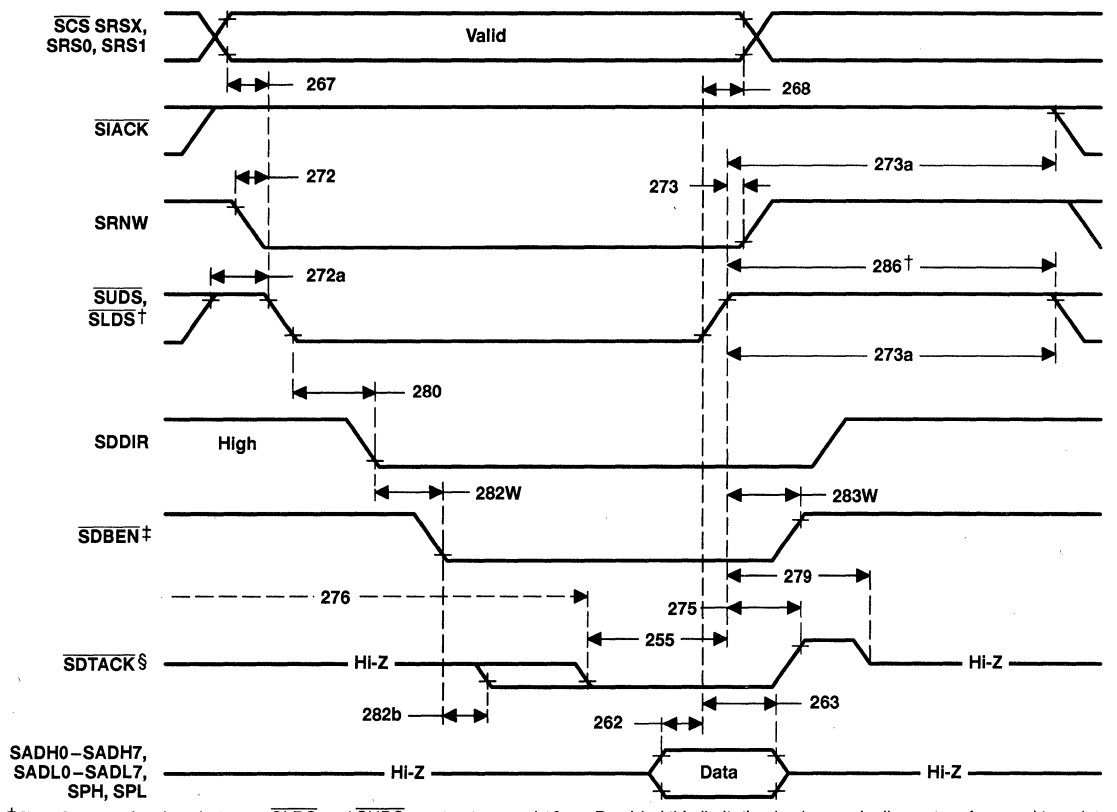
† $\overline{\text{SDTACK}}$ is an active-low bus ready signal. It must be asserted before data output.

Figure 23. 68xxx DIO Read-Cycle Timing

68xxx DIO write-cycle timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
255	Delay time, $\overline{SDTACK}$ low to either $\overline{SCS}$, SUDS or $\overline{SLDS}$ high	15		15		ns
262	Setup time, write data valid before $\overline{SUDS}$ or $\overline{SLDS}$ no longer low	15		15		ns
263	Hold time, write data valid after $\overline{SUDS}$ or $\overline{SLDS}$ high	15		15		ns
267†	Setup time, register address before $\overline{SUDS}$ or $\overline{SLDS}$ no longer high (see Note 19)	15		15		ns
268	Hold time, register address valid after $\overline{SUDS}$ or $\overline{SLDS}$ no longer low (see Note 20)	0		0		ns
272	Setup time, SRNW before $\overline{SUDS}$ or $\overline{SLDS}$ no longer high (see Note 19)	12		12		ns
272a	Setup time, inactive $\overline{SUDS}$ or $\overline{SLDS}$ high to active data strobe no longer high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
273	Hold time, SRNW after $\overline{SUDS}$ or $\overline{SLDS}$ high	0		0		ns
273a	Hold time, inactive $\overline{SUDS}$ or $\overline{SLDS}$ high after active data strobe high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
275	Delay time, $\overline{SCS}$, $\overline{SUDS}$ or $\overline{SLDS}$ high to $\overline{SDTACK}$ high (see Note 19)	0	25	0	25	ns
276‡	Delay time, $\overline{SDTACK}$ low in the first DIO access to the SIF register to $\overline{SDTACK}$ low in the immediately following access to the SIF		4000		4000	ns
279§	Delay time, $\overline{SUDS}$ or $\overline{SLDS}$ high to $\overline{SDTACK}$ in the high-impedance state	0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
280	Delay time, $\overline{SUDS}$ or $\overline{SLDS}$ low to SDDIR low (see Note 19)	0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
282b	Delay time, SDBEN low to SDTACK low (see *TMS380 Second Generation Token-Ring User's Guide,* SPWU005, subsection 3.4.1.1.1) — If SIF register is ready (no waiting required)	0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
	If SIF register is not ready (waiting required)	0	4000	0	4000	
282W	Delay time, SDDIR low to $\overline{SDBEN}$ low	0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
283W	Delay time, $\overline{SUDS}$ or $\overline{SLDS}$ high to $\overline{SDBEN}$ no longer low	0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
286	Pulse duration, $\overline{SUDS}$ or $\overline{SLDS}$ high between DIO accesses (see Note 19)	$t_{c(SCK)}$		$t_{c(SCK)}$		ns

† It is the later of $\overline{SRD}$ and $\overline{SWR}$ or $\overline{SCS}$ low that indicates the start of the cycle.
‡ This specification has been characterized to meet stated value. It is not assured during manufacturing testing.
§ This specification is provided as an aid to board design. It is not assured during manufacturing testing.
NOTES: 19. The inactive chip select is $\overline{SIACK}$ in DIO read and DIO write cycles, and $\overline{SCS}$ is the inactive chip select in interrupt-acknowledge cycles.
20. In 80x8x mode, SRAS may be used to strobe the values of $\overline{SBHE}$, SRSX, SRS0–SRS2, and $\overline{SCS}$. When used to do so, SRAS must meet parameter 266a, and $\overline{SBHE}$, SRS0–SRS2, and $\overline{SCS}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.



† For 68xxx mode, skew between $\overline{\text{SLDS}}$ and $\overline{\text{SUDS}}$ must not exceed 10 ns. Provided this limitation is observed, all events referenced to a data strobe edge use the later occurring edge. Events defined by two data strobes edges, such as parameter 286, are measured between latest and earlier edges.

‡ When the TMS380C25 begins to drive $\overline{\text{SDBEN}}$ inactive, it has already latched the write data internally. Parameter 263 must be met to the input of the data buffers.

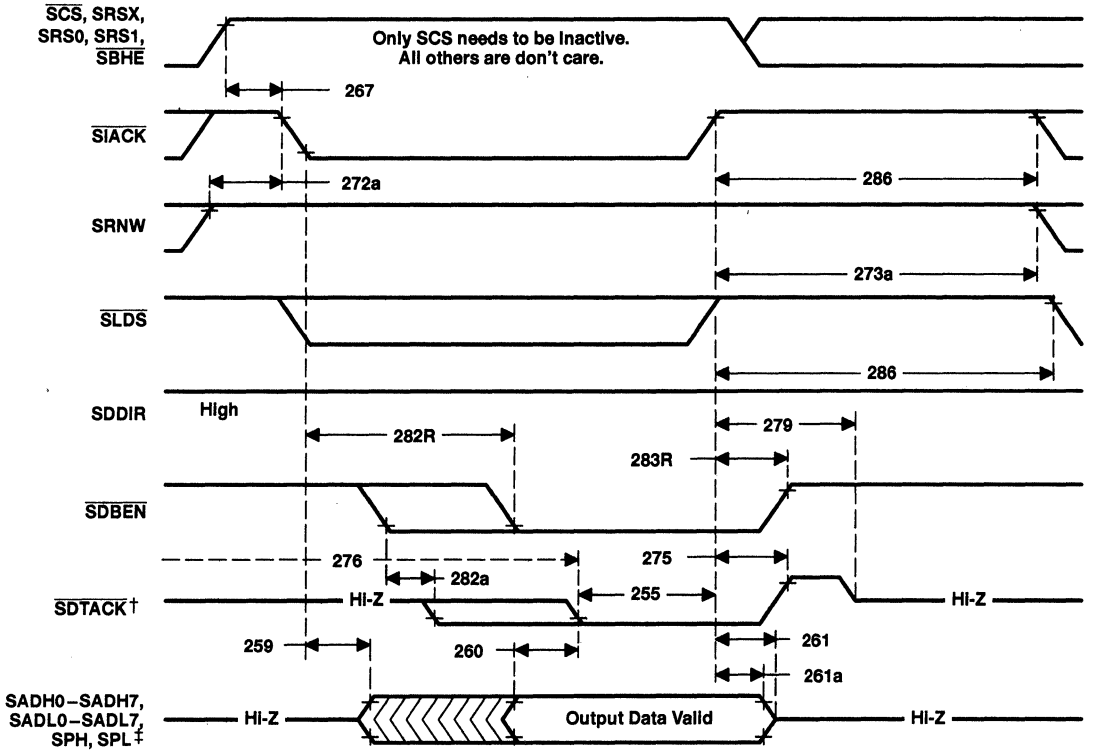
§ $\overline{\text{SDTACK}}$ is an active-low bus ready signal. It must be asserted before data output.

Figure 24. 68xxx DIO Write-Cycle Timing

68xxx interrupt-acknowledge-cycle timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
255	Delay time, $\overline{SDTACK}$ low to either $\overline{SCS}$ or $\overline{SUDS}$, or $\overline{SIACK}$ high	15		15		ns
259†	Hold time, SAD in the high-impedance state after $\overline{SIACK}$ no longer high (see Note 19)	0		0		ns
260	Setup time, output data valid before $\overline{SDTACK}$ no longer high	0		0		ns
261†	Delay time, $\overline{SIACK}$ high to SAD in the high-impedance state (see Note 19)		35		35	ns
261a	Hold time, output data valid after $\overline{SCS}$ or $\overline{SIACK}$ no longer low (see Note 19)	0		0		ns
267§	Setup time, register address before $\overline{SIACK}$ no longer high (see Note 19)	15		15		ns
272a	Setup time, inactive high $\overline{SIACK}$ to active data strobe no longer high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
273a	Hold time, inactive SRNW high after active data strobe high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
275	Delay time, $\overline{SCS}$ or $\overline{SRNW}$ high to $\overline{SDTACK}$ high (see Note 19)	0	25	0	25	ns
276‡	Delay time, $\overline{SDTACK}$ low in the first DIO access to the SIF register to $\overline{SDTACK}$ low in the immediately following access to the SIF	0	4000	0	4000	ns
279†	Delay time, $\overline{SIACK}$ high to $\overline{SDTACK}$ in the high-impedance state	0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
282a	Delay time, $\overline{SDBEN}$ low to $\overline{SDTACK}$ low in a read cycle	0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
282R	Delay time, $\overline{SIACK}$ low to $\overline{SDBEN}$ low (see *TMS380 Second Generation Token-Ring User's Guide*, SPWU005, subsection 3.4.1.1.1) provided the previous cycle completed	0	$t_{c(SCK)}+3$	0	$t_{c(SCK)}+3$	ns
283R	Delay time, $\overline{SIACK}$ high to $\overline{SDBEN}$ high (see Note 19)	0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
286	Pulse duration, $\overline{SIACK}$ high between DIO accesses (see Note 19)	$t_{c(SCK)}$		$t_{c(SCK)}$		ns

† This specification is provided as an aid to board design. It is not assured during manufacturing testing.
‡ This specification has been characterized to meet stated value. It is not assured during manufacturing testing.
§ It is the later of $\overline{SRD}$ and $\overline{SRD}$ or $\overline{SCS}$ low that indicates the start of the cycle.
NOTE 19: The inactive chip select is $\overline{SIACK}$ in DIO read and DIO write cycles, and $\overline{SCS}$ is the inactive chip select in interrupt-acknowledge cycles.



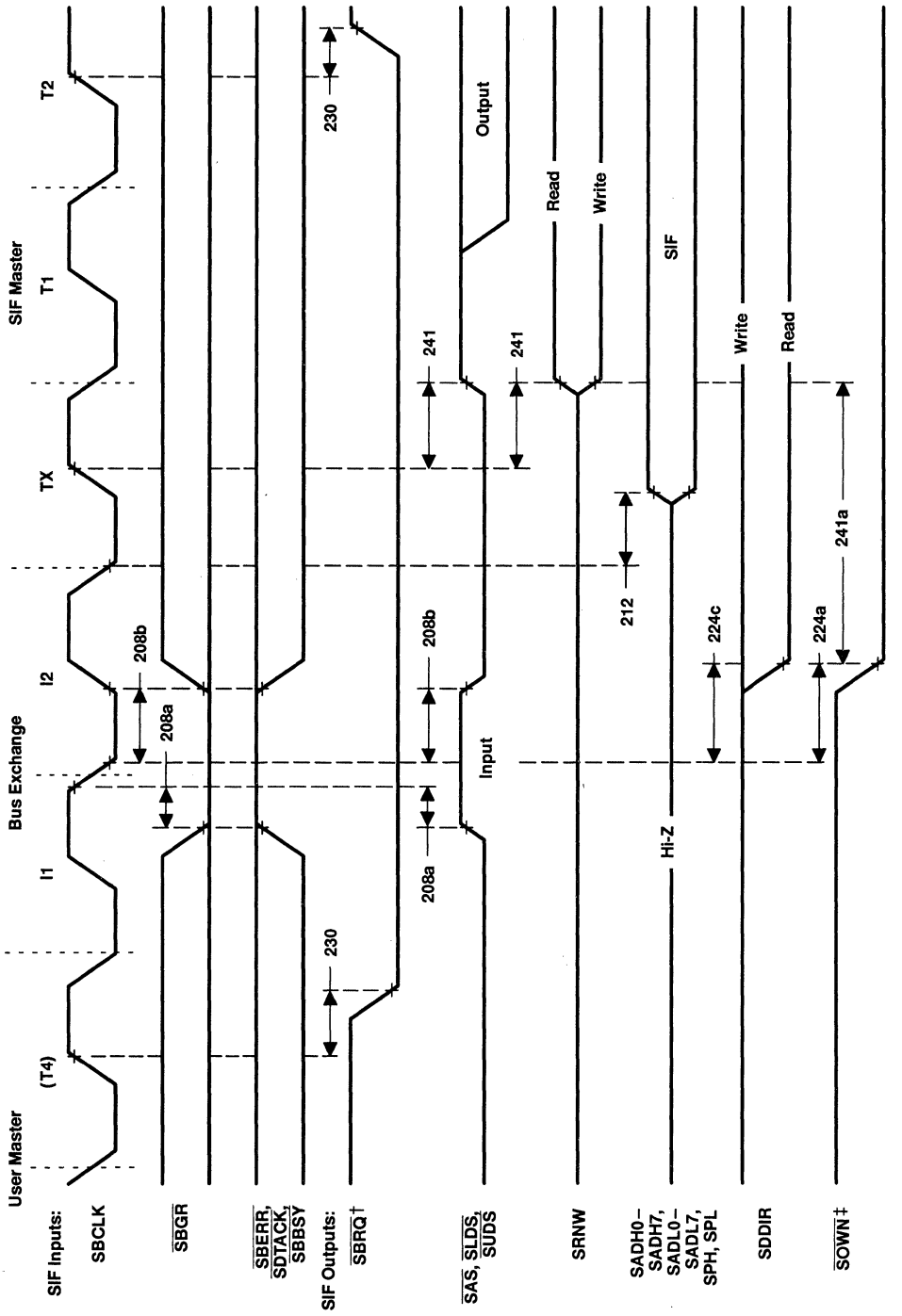
† $\overline{\text{SDTACK}}$ is an active-low bus ready signal. It must be asserted before data output.
‡ Internal logic drives $\overline{\text{SDTACK}}$ high and verifies that it has reached a valid high level before making it a 3-state signal.

Figure 25. 68xxx Interrupt-Acknowledge-Cycle Timing

68xxx-mode bus-arbitration timing, SIF takes control

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous input $\overline{\text{SBGR}}$ before SBCLK no longer high to assure recognition on this cycle	10		10		ns
208b	Hold time, asynchronous input $\overline{\text{SBGR}}$ after SBCLK low to assure recognition on this cycle	10		10		ns
212	Delay time, SBCLK low to address valid	0	20	0	20	ns
224a	Delay time, SBCLK low in cycle I2 to $\overline{\text{SOWN}}$ low (see Note 22)	0	20	0	15	ns
224c	Delay time, SBCLK low in cycle I2 to SDDIR low in DMA read		28		23	ns
230	Delay time, SBCLK high to either SHRQ low or $\overline{\text{SBRQ}}$ high		20		15	ns
241	Delay time, SBCLK high in TX cycle to $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$ high		25		25	ns
241a†	Hold time, $\overline{\text{SUDS}}$, $\overline{\text{SLDS}}$, SRNW, and $\overline{\text{SAS}}$ in the high-impedance state after $\overline{\text{SOWN}}$ low, bus acquisition	$t_{c(SCK)}-15$		$t_{c(SCK)}-15$		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.
NOTE 22: Motorola-style bus slaves hold $\overline{\text{SDTACK}}$ active until the bus master deasserts $\overline{\text{SAS}}$.



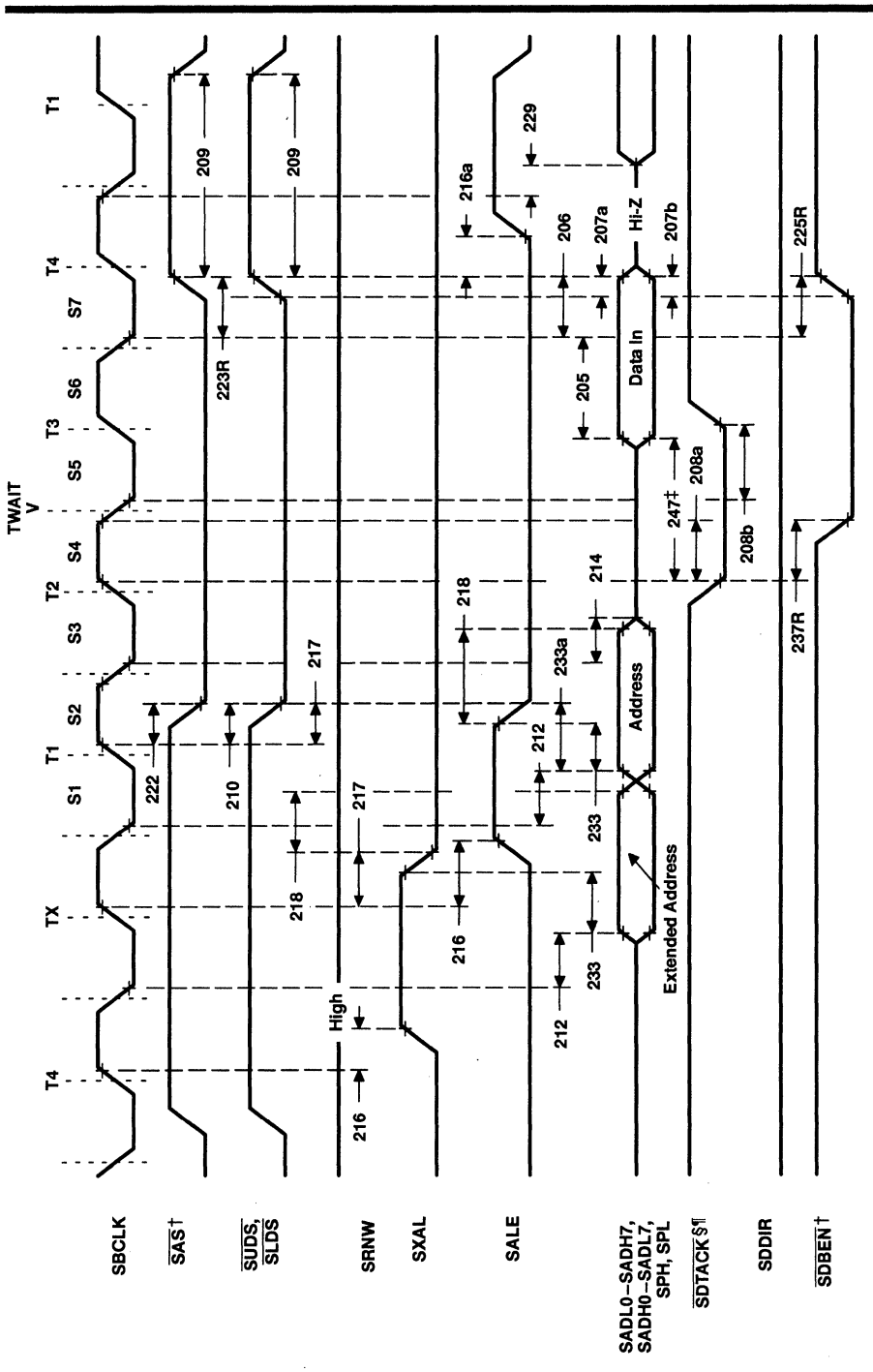
† In 80x8x mode, the system interface deasserts SHRQ on the rising edge of SBCLK following the T4 state of the last system bus transfer it controls. In 68xxx mode, the system interface deasserts $\overline{SBRQ}$ on the rising edge of SBCLK in state T2 of the first system bus transfer it controls.
‡ While the system-interface DMA controls are active (i.e., $\overline{SOWN}$ is asserted), $\overline{SCS}$ is disabled.

Figure 26. 68xxx-Mode Bus-Arbitration Timing, SIF Takes Control

68xxx-mode DMA read-cycle timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
205	Setup time, input data valid before SBCLK in T3 cycle no longer high	10		10		ns
206	Hold time, input data valid after SBCLK low in T4 cycle if parameters 207a and 207b not met	10		10		ns
207a	Hold time, input data valid after data strobe no longer low	0		0		ns
207b	Hold time, input data valid after $\overline{\text{SDBEN}}$ no longer low	0		0		ns
208a	Setup time, asynchronous input $\overline{\text{SDTACK}}$ before SBCLK no longer high to assure recognition on this cycle	10		10		ns
208b	Hold time, asynchronous input $\overline{\text{SDTACK}}$ after SBCLK low to assure recognition on this cycle	10		10		ns
209	Pulse duration, $\overline{\text{SAS}}$, $\overline{\text{SUDS}}$, and $\overline{\text{SLDS}}$ high	$t_{c(SCK)}+t_{w(SCKL)}-18$		$t_{c(SCK)}+t_{w(SCKL)}-18$		ns
210	Delay time, SBCLK high in T2 cycle to $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$ active		16		11	ns
212	Delay time, SBCLK low to address valid		20		20	ns
214†	Delay time, SBCLK low in T2 cycle to SAD in the high-impedance state		20		15	ns
216	Delay time, SBCLK high to SALE or SXAL high		20		20	ns
216a	Hold time, SALE or SXAL low after $\overline{\text{SUDS}}$ and $\overline{\text{SAS}}$ high	0		0		ns
217	Delay time, SBCLK high to SXAL low in the TX cycle or SALE low in the T1 cycle	0	25	0	25	ns
218	Hold time, address valid after SALE, SXAL low	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	ns
222	Delay time, SBCLK high to $\overline{\text{SAS}}$ low		20		15	ns
223R	Delay time, SBCLK low in T4 cycle to $\overline{\text{SUDS}}$, $\overline{\text{SLDS}}$, and $\overline{\text{SAS}}$ high (see Note 23)	0	16	0	11	ns
225R	Delay time, SBCLK low in T4 cycle to $\overline{\text{SDBEN}}$ high		16		11	ns
229†	Hold time, SAD in the high-impedance state after SBCLK low in T4 cycle	0		0		ns
233	Setup time, address valid before SALE or SXAL no longer high	10		10		ns
233a	Setup time, address valid before $\overline{\text{SAS}}$ no longer high	$t_{w(SCKL)}-15$		$t_{w(SCKL)}-15$		ns
237R	Delay time, SBCLK high in the T2 cycle to $\overline{\text{SDBEN}}$ low		16		11	ns
247	Setup time, data valid before $\overline{\text{SDTACK}}$ low if parameter 208a not met	0		0		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.
NOTE 23: While the system-interface DMA controls are active (i.e., $\overline{\text{SOWN}}$ is asserted), $\overline{\text{SCS}}$ is disabled.

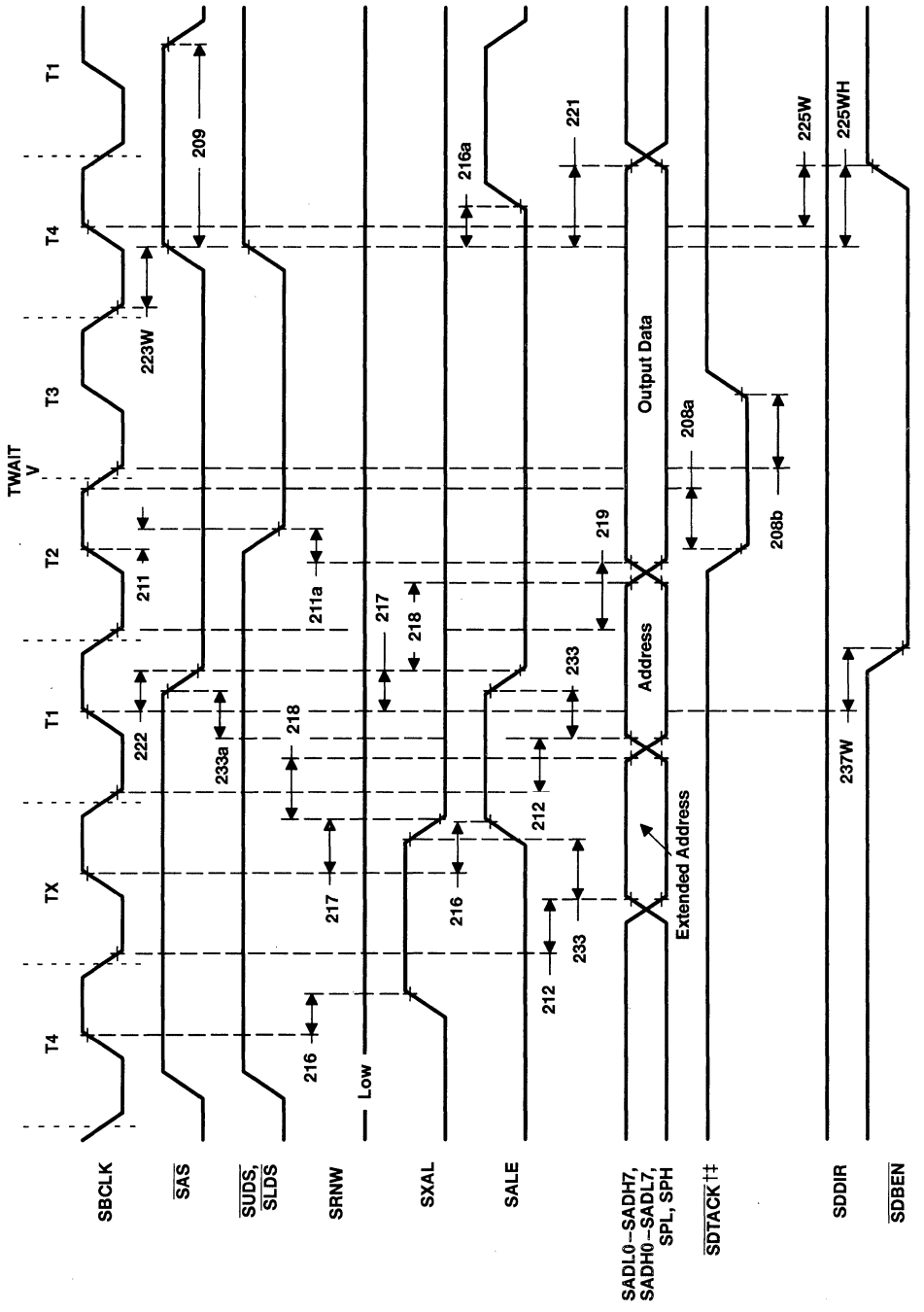


† On a read cycle, the read strobe remains active until the internal sample of incoming data is completed. Input data may be removed when either the read strobe or SDBEN becomes no longer active.
‡ If parameter 208a is not met, valid data must be present before SDTACK goes low.
§ Motorola-style bus slaves hold SDTACK active until the bus master deasserts SAS.
¶ All V_{SS} pins should be routed to minimize inductance to system ground.

Figure 27. 68xxx-Mode DMA Read-Cycle Timing

68xxx-mode DMA write-cycle timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous input $\overline{SDTACK}$ before SBCLK no longer high to assure recognition on this cycle	10		10		ns
208b	Hold time, asynchronous input $\overline{SDTACK}$ after SBCLK low to assure recognition on this cycle	10		10		ns
209	Pulse duration, $\overline{SAS}$, $\overline{SUDS}$, and $\overline{SLDS}$ high	$t_{c(SCK)}+t_{w(SCKL)}-18$		$t_{c(SCK)}+t_{w(SCKL)}-18$		ns
211	Delay time, SBCLK high in T2 cycle to $\overline{SUDS}$ and $\overline{SLDS}$ active		25		25	ns
211a	Delay time, output data valid to $\overline{SUDS}$ and $\overline{SLDS}$ no longer high	$t_{w(SCKL)}-15$		$t_{w(SCKL)}-15$		ns
212	Delay time, SBCLK low to address valid		20		20	ns
216	Delay time, SBCLK high to SALE or SXAL high		20		20	ns
216a	Hold time, SALE or SXAL low after $\overline{SUDS}$ and $\overline{SAS}$ high	0		0		ns
217	Delay time, SBCLK high to SXAL low in the TX cycle or SALE low in the T1 cycle	0	25	0	25	ns
218	Hold time, address valid after SALE, SXAL low	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	ns
219	Delay time, SBCLK low in T2 cycle to output data and parity valid		29		29	ns
221	Hold time, output data, parity valid after $\overline{SUDS}$ and $\overline{SLDS}$ high	$t_{c(SCK)}-12$		$t_{c(SCK)}-12$		ns
222	Delay time, SBCLK high to $\overline{SAS}$ low		20		15	ns
223W	Delay time, SBCLK low to $\overline{SUDS}$, $\overline{SLDS}$, and $\overline{SAS}$ high	0	16	0	11	ns
225W	Delay time, SBCLK high in T4 cycle to $\overline{SDBEN}$ high		16		11	ns
225WH	Hold time, $\overline{SDBEN}$ low after $\overline{SUDS}$ and $\overline{SLDS}$ high	$t_{c(SCK)}/2-7$		$t_{c(SCK)}/2-7$		ns
233	Setup time, address valid before SALE or SXAL no longer high	10		10		ns
233a	Setup time, address valid before $\overline{SAS}$ no longer high	$t_{w(SCKL)}-15$		$t_{w(SCKL)}-15$		ns
237W	Delay time, SBCLK high in T1 cycle to $\overline{SDBEN}$ low		16		11	ns



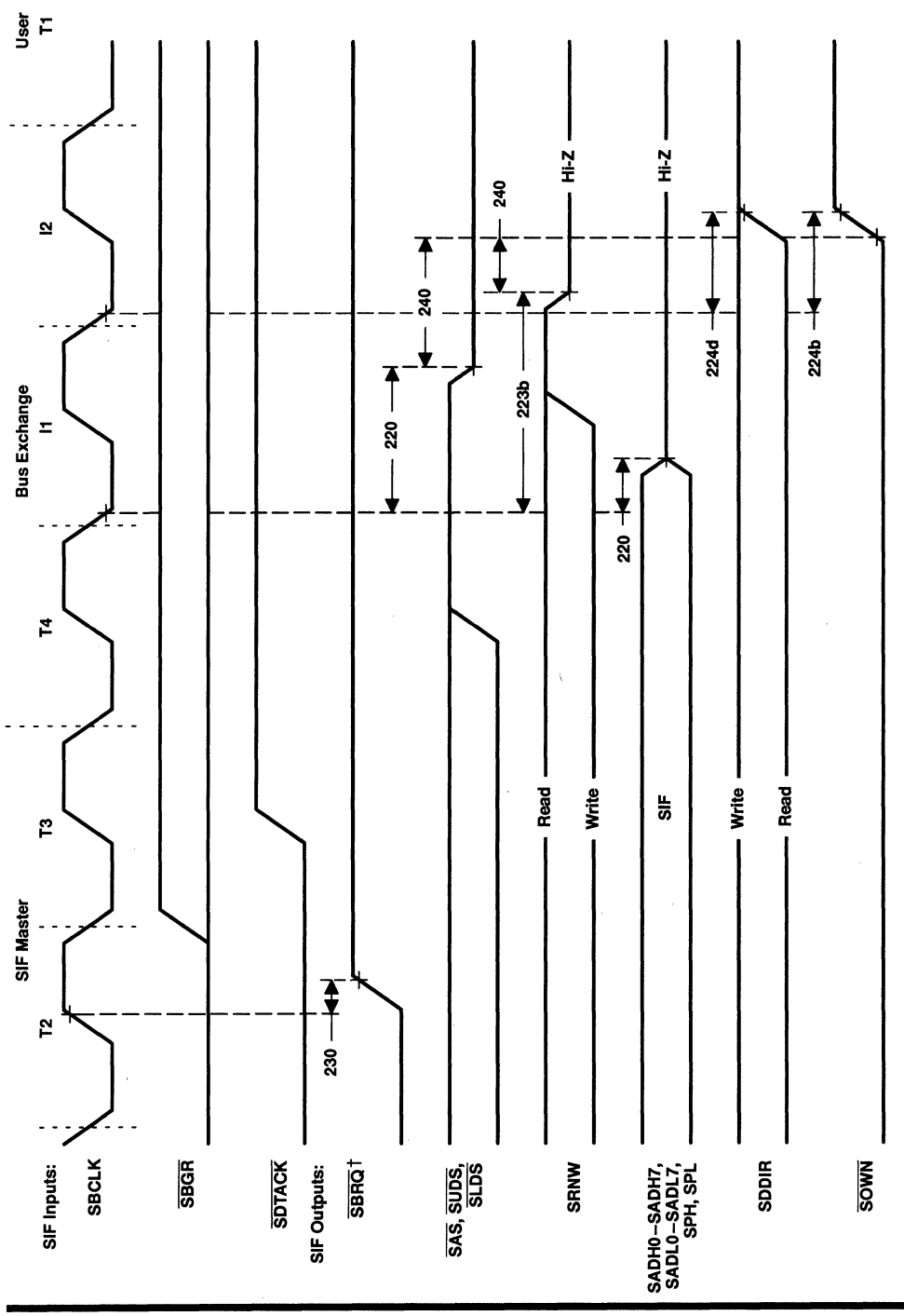
† All V_{SS} pins should be routed to minimize inductance to system ground.
‡ On a read cycle, the read strobe remains active until the internal sample of incoming data is completed. Input data can be removed when either the read strobe or $\overline{SDBEN}$ becomes no longer active.

Figure 28. 68xxx-Mode DMA Write-Cycle Timing

68xxx-mode bus-arbitration timing, SIF returns control

NO.		25-MHz OPERATION		25-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
220†	Delay time, SBCLK low in I1 cycle to SAD, SPL, SPH, $\overline{SUDS}$, and $\overline{SLDS}$ in the high-impedance state, bus release		35		35	ns
223b†	Delay time, SBCLK low in I1 cycle to $\overline{SBHE}$/SRNW in the high-impedance state		45		45	ns
224b	Delay time, SBCLK low in cycle I2 to $\overline{SOWN}$ high	0	20	0	15	ns
224d	Delay time, SBCLK low in cycle I2 to SDDIR high		27		22	ns
230	Delay time, SBCLK high to either SHRQ low or $\overline{SBRQ}$ high		20		15	ns
240†	Setup from, $\overline{SUDS}$, $\overline{SLDS}$, SRNW, and $\overline{SAS}$ control signals in the high-impedance state before $\overline{SOWN}$ no longer low	0		0		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.

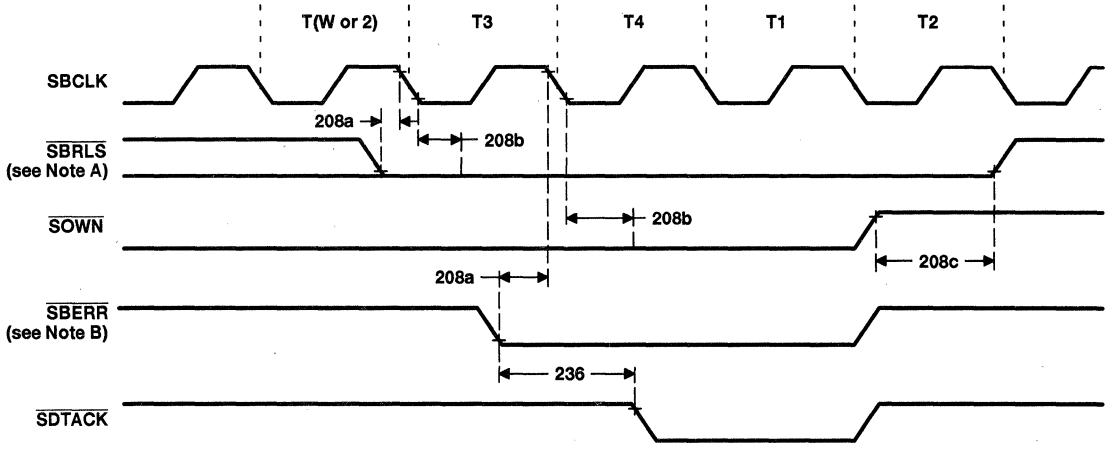


† In 80x8x mode, the system interface deasserts SHRQ on the rising edge of SBCLK following the T4 state of the last system bus transfer it controls. In 68xxx mode, the system interface deasserts SBRQ on the rising edge of SBCLK in state T2 of the first system bus transfer it controls.

Figure 29. 68xxx-Mode Bus-Arbitration Timing, SIF Returns Control

68xxx-mode bus-release and error timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous input before SBCLK no longer high to assure recognition	10		10		ns
208b	Hold time, asynchronous input $\overline{\text{SBRLS}}$, $\overline{\text{SOWN}}$, or $\overline{\text{SBERR}}$ after SBCLK low to assure recognition	10		10		ns
208c	Hold time, $\overline{\text{SBRLS}}$ low after $\overline{\text{SOWN}}$ high	0		0		ns
236	Setup time, $\overline{\text{SBERR}}$ low before $\overline{\text{SDTACK}}$ no longer high if parameter 208a not met	30		30		ns



NOTES: A. The system interface ignores the assertion of $\overline{\text{SBRLS}}$ if it does not own the system bus. If it does own the bus, when it detects the assertion of $\overline{\text{SBRLS}}$, it completes any internally started DMA cycle and relinquishes control of the bus. If no DMA transfer has internally started, the system interface releases the bus before starting another.

B. If $\overline{\text{SBERR}}$ is asserted when the system interface controls the system bus, the current bus transfer is completed regardless of the value of $\overline{\text{SDTACK}}$. If the BERETRY register is nonzero, the cycle is retried. If the BERETRY register is zero, the system interface releases control of the system bus. The system interface ignores the assertion of $\overline{\text{SBERR}}$ if it is not performing a DMA bus cycle on the system bus. When $\overline{\text{SBERR}}$ is properly asserted and BERETRY is zero, the system interface releases the bus upon completion of the current bus transfer and halts all further DMA on the system side. The error is synchronized to the local bus, and DMA stops on the local sides. The value of the SDMAADR, SDMADDRX, and SDMALEN registers in the system interface are not defined after a system-bus error.

C. In cycle-steal mode, state TX is present on every system bus transfer. In burst mode, state TX is present on the first bus transfer and whenever the increment of the DMA address register carries beyond the least significant 16 bits.

D. $\overline{\text{SDTACK}}$ is not sampled to verify that it is deasserted.

E. Unless otherwise specified, for all signals specified as a maximum delay from the end of an SBCLK transition to the signal valid, the signal is also specified to hold its previous value (including high impedance) until the start of that SBCLK transition.

Figure 30. 68xxx-Mode Bus-Release and Error Timing

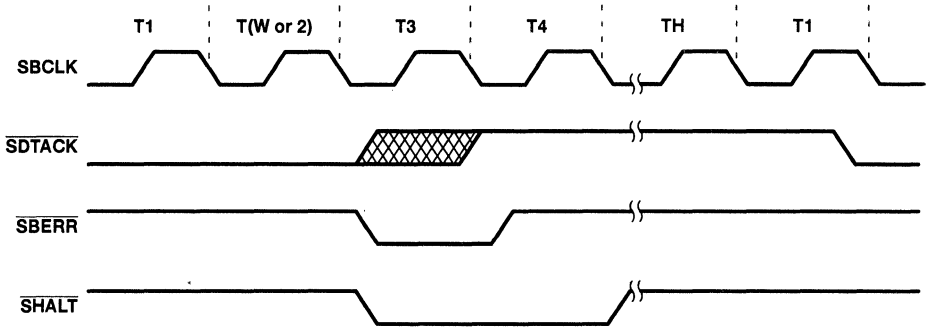


Figure 31. 68xxx-Mode Bus Halt and Retry, Normal Completion With Delayed Start†

† Only the relative placement of the edges to SBCLK falling edge is shown. Actual signal edge placement can vary from waveforms shown.

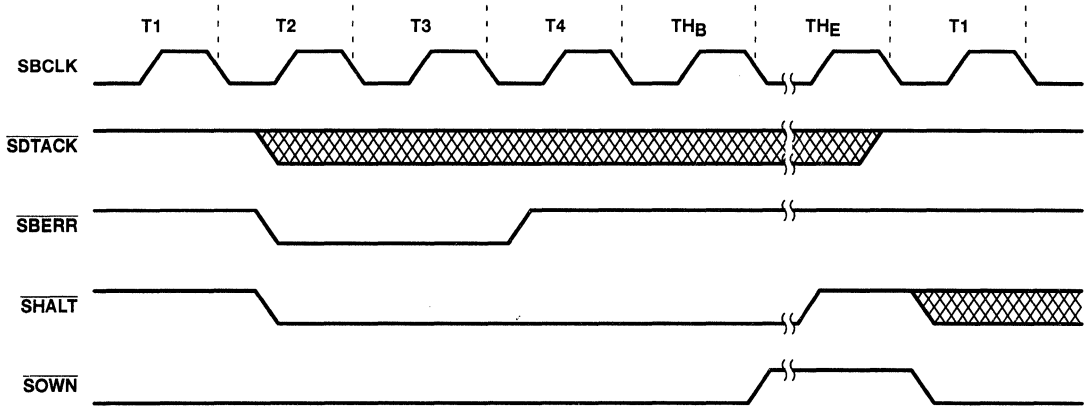


Figure 32. 68xxx-Mode Bus Halt and Retry, Rerun Cycle With Delayed Start†

† Only the relative placement of the edges to SBCLK falling edge is shown. Actual signal edge placement can vary from waveforms shown.

- Single-Chip Token-Ring Solution
- IBM Token-Ring Network™ Compatible
- Compatible With ISO/IEC IEEE Std. 802.5:1992 Token-Ring Access-Method and Physical-Layer Specifications
- Compatible With TI380FPA FNL PacketBlaster™
- Glueless Memory Interface
- Digital Phase-Locked Loop
  - Precise Control of Bandwidths
  - Improved Jitter Tolerance
  - Minimizes Accumulated Phase Slope
- Phantom Drive for Physical Insertion Onto Ring
- Differential Line Receiver With Level-Dependent Frequency Equalization
- Low-Impedance Differential Line Driver to Ease Transmit-Filter Design
- On-Chip Watchdog Timer
- Internal Crystal Oscillator for Reference-Clock Generation
- Expandable LAN-Subsystem Memory Up to 2 Mbytes
- 32-Bit Host Address Bus
- 80x8x or 68xxx-Type Bus and Memory Organization
- Dual-Port DMA and Direct I/O Transfers to Host Bus
- Supports 8- or 16-Bit Pseudo-DMA Operation
- 176-Pin Thin Quad Flat Package (PGF Suffix)
- 0.8-μm CMOS Technology
- ESD Protection Exceeds 2000 V
- Operating Temperature Range 0°C to 70°C
- Token-Ring Features
  - 16- or 4-Mbps Data Rates
  - Supports up to 18-KByte Frame Size (16 Mbps Only)
  - Supports Universal and Local Addressing
  - Early Token-Release Option (16 Mbps Only)
  - Built-In Real-Time Error Detection
  - Automatic Frame-Buffer Management
  - 2- to 33-MHz System-Bus Clock
  - Slow-Clock Low-Power Mode

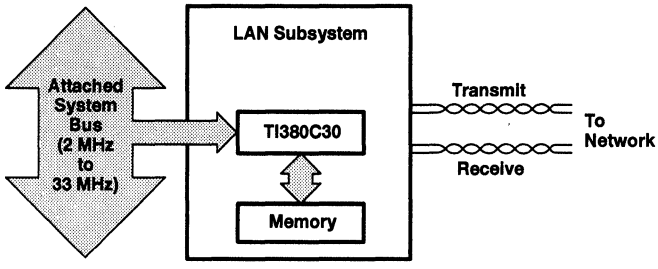


Figure 1. Network-Commprocessor Applications Diagram

ADVANCE INFORMATION

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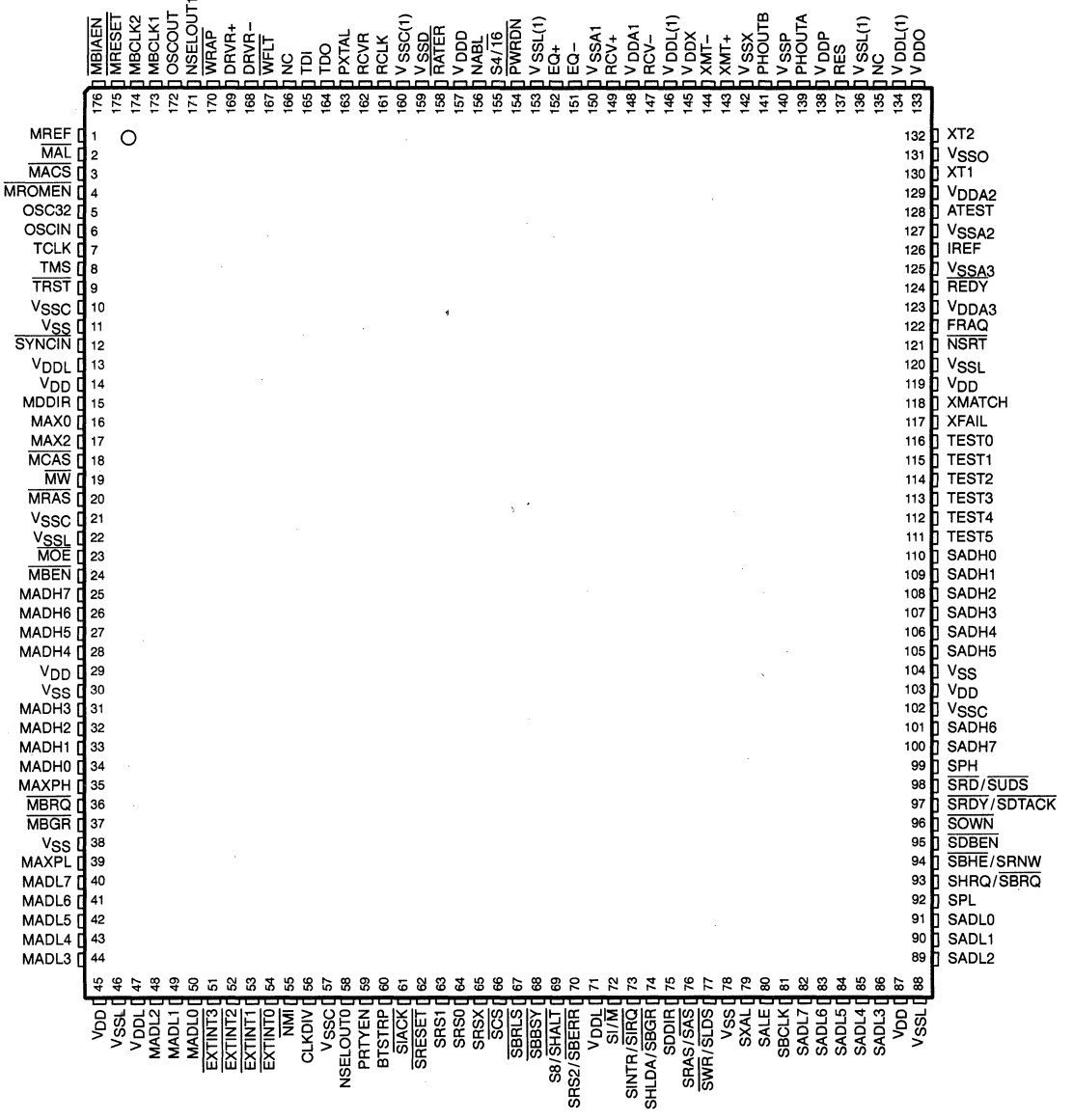
PacketBlaster is a trademark of Texas Instruments Incorporated.

ADVANCE INFORMATION

pin assignments

PGF PACKAGE
(TOP VIEW)



TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251–1443

description

The TI380C30 is a single-chip token-ring solution, combining both the commprocessor and the physical-layer interface onto a single device. The TI380C30 supports both 16 and 4 Mbps of operation, conforms to ISO 8802–5/ IEEE 802.5–1992 standards, and has been verified to be completely IBM Token-Ring Network compatible.

The TI380C30 provides a high degree of integration as it combines the functions of the TI380C25 and the TI380C60 onto a single chip. With this chip, only local memory and minimal additional components such as PAL® devices and crystal oscillators need to be added to complete the LAN-subsystem design.

The TI380C30 provides a 32-bit system-memory address reach with a high-speed bus-master DMA interface that supports rapid communications with the host system. In addition, the TI380C30 supports direct I/O and a low-cost 8- or 16-bit pseudo-DMA interface that requires only a chip select to work directly on an 80x8x 8-bit slave I/O interface. Selectable 80x8x or 68xxx-type host-system bus and memory organization add to design flexibility.

The TI380C30 supports addressing for up to 2 Mbytes of local memory. This expanded memory capacity can improve LAN-subsystem performance by minimizing the frequency of host LAN-subsystem communications by allowing larger blocks of information to be transferred at one time. The support of large local memory is important in applications that require large data transfers (such as graphics or data-base transfers) and in heavily loaded networks where the extra memory can provide data buffers to store data until it can be processed by the host.

The proprietary CPU used in the TI380C30 allows protocol software to be downloaded into RAM or stored in ROM in the local-memory space. By moving protocols [such as logical link control (LLC)] to the LAN-subsystem, overall system performance is increased. This is accomplished by offloading processing from the host-system to the TI380C30, which can also reduce LAN-subsystem-to-host communications. As other protocol software is developed, greater differentiation of end products with enhanced system performance is possible.

The TI380C30 includes hardware counters that provide real-time error detection and automatic frame-buffer management. These counters control system-bus retries and burst size, and track host- and LAN-subsystem-buffer status. Previously, these counters needed to be maintained in software. By integrating them into hardware, software overhead is removed and LAN-subsystem performance is improved.

The TI380C30 implements a TI-patented enhanced-address-copy-option (EACO) interface. This interface supports external address-checking devices, such as the TMS380SRA source-routing accelerator. The TI380C30 has a 128-word external I/O space in its memory to support external address-checker devices and other hardware extensions to the TMS380 architecture.

At the physical-layer interface, the Manchester-encoded data stream is received and phase aligned using an on-chip dual-digital phase-locked loop (PLL). Both the recovered clock and data are passed on to the protocol-handling circuits on the TI380C30 for serial-to-parallel conversion and data processing. On transmit, the TI380C30 buffers the output from the protocol-handling circuit and drives the media via suitable isolation and waveform-shaping components.

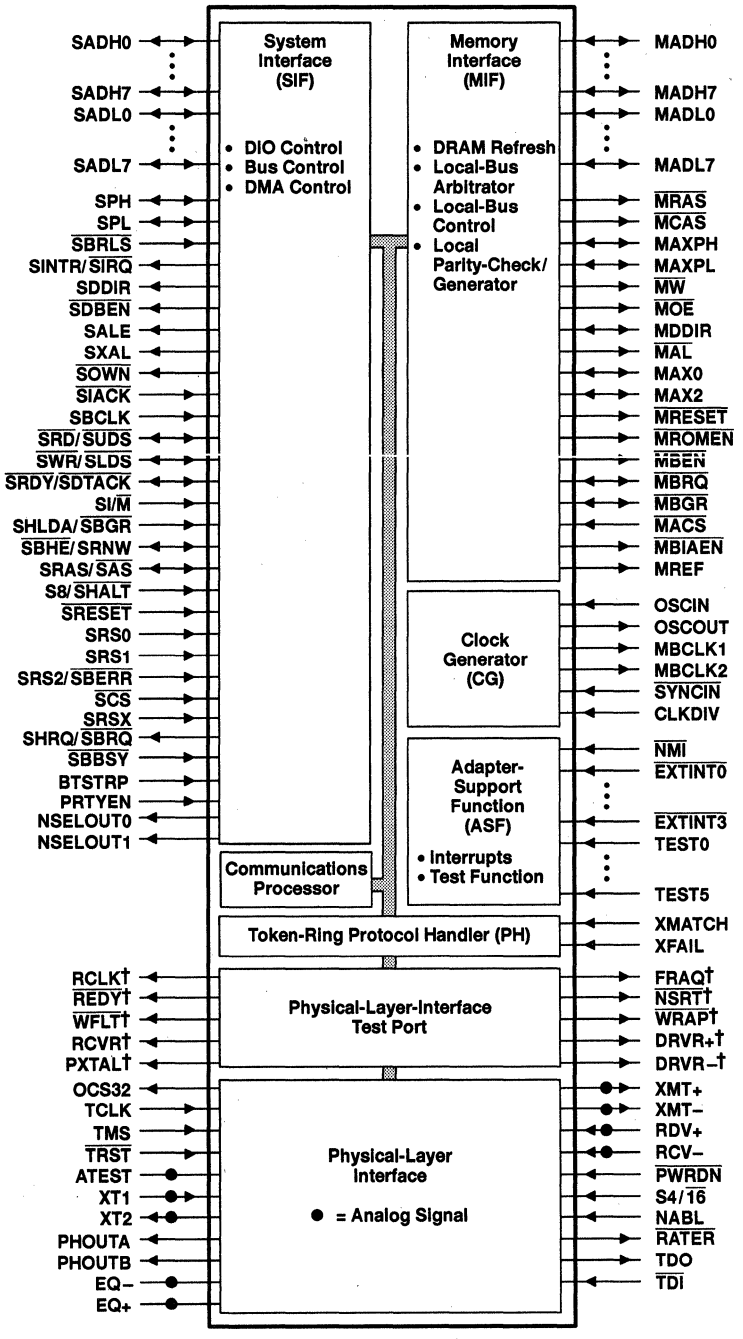
The TI380C30 uses CMOS technology to reduce power consumption to PCMCIA-compatible levels. Power-management features are incorporated to support Green PC compatibility.

In addition to the PLL, all other functions required to interface to an IEEE-802.5 token ring are provided. These functions include the phantom drive to control the relays within a trunk-coupling unit and wire-fault detection circuits; an internal-wrap function for self-test; and a watchdog timer to provide fail-safe deinsertion from the ring in the event of a station, microcode or commprocessor failure.

The major blocks of the TI380C30 include the communications processor (CP), the system interface (SIF), the memory interface (MIF), the protocol handler (PH), the clock generator (CG), the adapter-support function (ASF), and the physical-layer interface (PHY), as shown in the functional block diagram.

PAL® is a registered trademark of Advanced Micro Devices Inc. Other companies also manufacture programmable array logic devices.

functional block diagram



† Signals are provided for test monitoring purposes.

Pin Functions

PIN NAME	PIN NO.	I/O/E†	DESCRIPTION
ATEST	128	E	Analog test. Should be left unconnected.
BTSTRP	60	I	Bootstrap. The value on BTSTRP is loaded into the BOOT bit of the SIFACL register at reset (i.e., when $\overline{\text{SRESET}}$ is asserted or the $\overline{\text{ARESET}}$ bit in the SIFACL register is set) to form a default value. BTSTRP indicates whether chapters 0 and 31 of the memory map are RAM or ROM. If these chapters are RAM, the TI380C30 is denied access to the local-memory bus until the CPHALT bit in the SIFACL register is cleared. H = Chapters 0 and 31 of local memory are RAM-based (see Note 1). L = Chapters 0 and 31 of local memory are ROM-based.
CLKDIV	56	I	Clock divider select (see Note 2) H = 64-MHz OSCIN for 4-MHz local bus L = 32-MHz OSCIN for 4-MHz local bus or 48-MHz OSCIN for 6-MHz local bus
DRVR+ DRVR–	169 168	O O	Differential-driver data outputs (reserved)
EQ+ EQ–	152 151	E E	Equalization/gain points. Connections to allow frequency tuning of equalization circuit.
$\overline{\text{EXTINT0}}$ $\overline{\text{EXTINT1}}$ $\overline{\text{EXTINT2}}$ $\overline{\text{EXTINT3}}$	54 53 52 51	I/O	Reserved; must be pulled high (see Note 3)
FRAQ	122	O	Frequency-acquisition control. FRAQ is driven by the TI380C30 PH. H = Clock recovery PLL is initialized. L = Normal operation
IREF	126	E	Internal reference. IREF allows the internal bias current of analog circuitry to be adjusted via an external resistor.
$\overline{\text{MACS}}$	3	I	Reserved; must be tied low (see Note 4)
MADH0 MADH1 MADH2 MADH3 MADH4 MADH5 MADH6 MADH7	34 33 32 31 28 27 26 25	I/O	Local-memory address, data, and status bus — high byte. For the first quarter of the local-memory cycle, these bus lines carry address bits AX4 and A0 to A6; for the second quarter, they carry status bits; and for the third and fourth quarters, they carry data bits 0 to 7. The most significant bit is MADH0 and the least significant bit is MADH7. Memory Cycle 1Q 2Q 3Q 4Q Signal AX4, A0–A6 Status D0–D7 D0–D7
MADL0 MADL1 MADL2 MADL3 MADL4 MADL5 MADL6 MADL7	50 49 48 44 43 42 41 40	I/O	Local-memory address, data, and status bus — low byte. For the first quarter of the local-memory cycle, these bus lines carry address bits A7 to A14; for the second quarter, they carry address bits AX4 and A0 to A6; and for the third and fourth quarters, they carry data bits 8 to 15. The most significant bit is MADL0 and the least significant bit is MADL7. Memory Cycle 1Q 2Q 3Q 4Q Signal A7–A14 AX4, A0–A6 D8–D15 D8–D15

† I = input, O = output, E = provides external-component connection to the internal circuitry for tuning

NOTES: 1. Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).
2. The TI380FPA and TMS380SRA are currently supported only with the 4-MHz local bus in either CLKDIV state. Expansion to support the 6-MHz local bus is under development.
3. Each pin must be individually tied to V_{DD} with a 1-kΩ pullup resistor.
4. Pin should be connected to ground.

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O/E†	DESCRIPTION
$\overline{MAL}$	2	O	Memory-address latch. $\overline{MAL}$ is a strobe signal for sampling the address at the start of the memory cycle; it is used by SRAMs and EPROMs. The full 20-bit word address is valid on MAX0, MAXPH, MAX2, MAXPL, MADH0–MADH7, and MADL0–MADL7. Three 8-bit transparent latches can be used to retain a 20-bit static address throughout the cycle. Rising edge = No signal latching Falling edge = Allows the above address signals to be latched
MAX0	16	I/O	Local-memory extended-address bit. MAX0 drives AX0 at row-address time and A12 at column-address and data-valid times for all cycles. MAX0 can be latched by $\overline{MRAS}$. Driving A12 eases interfacing to a burn-in address (BIA) ROM. Memory Cycle: 1Q / 2Q / 3Q / 4Q Signal: AX0 / A12 / A12 / A12
MAX2	17	I/O	Local-memory extended-address bit. MAX2 drives AX2 at row-address time, which can be latched by $\overline{MRAS}$, and A14 at column-address and data-valid times for all cycles. Driving A14 eases interfacing to a BIA ROM. Memory Cycle: 1Q / 2Q / 3Q / 4Q Signal: AX2 / A14 / A14 / A14
MAXPH	35	I/O	Local-memory extended address and parity — high byte. For the first quarter of a memory cycle, MAXPH carries the extended-address bit AX1; for the second quarter of a memory cycle, MAXPH carries the extended-address bit AX0; and for the last half of the memory cycle, MAXPH carries the parity bit for the high data byte. Memory Cycle: 1Q / 2Q / 3Q / 4Q Signal: AX1 / AX0 / Parity / Parity
MAXPL	39	I/O	Local-memory extended address and parity — low byte. For the first quarter of a memory cycle, MAXPL carries the extended-address bit AX3; for the second quarter of a memory cycle, MAXPL carries extended-address bit AX2; and for the last half of the memory cycle, MAXPL carries the parity bit for the low data byte. Memory Cycle: 1Q / 2Q / 3Q / 4Q Signal: AX3 / AX2 / Parity / Parity
MBCLK1 MBCLK2	173 174	O	Local-bus clock 1 and local-bus clock 2. MBCLK1 and MBCLK2 are referenced for all local-bus transfers. MBCLK2 lags MBCLK1 by a quarter of a cycle. MBCLK1 and MBCLK2 operate according to: MBCLK[1:2] / OSCIN / CLKDIV 8 MHz / 64 MHz / H 8 MHz / 32 MHz / L 12 MHz / 48 MHz / L
$\overline{MBEN}$	24	O	Buffer enable. $\overline{MBEN}$ enables the bidirectional buffer outputs on the MADH, MAXPH, MAXPL, and MADL buses during the data phase. $\overline{MBEN}$ is used in conjunction with MDDIR, which selects the buffer-output direction. H = Buffer output disabled L = Buffer output enabled
$\overline{MBGR}$	37	I/O	Reserved; must be left unconnected
$\overline{MBIAEN}$	176	O	Burned-in address enable. $\overline{MBIAEN}$ is an output signal used to provide an output enable for the ROM containing the adapter's BIA. H = $\overline{MBIAEN}$ is driven high for any write accesses to the addresses between >00.0000 and >00.000F, or any accesses (read/write) to any other address. L = $\overline{MBIAEN}$ is driven low for any read from addresses between >00.0000 and >00.000F.

† I = input, O = output, E = provides external-component connection to the internal circuitry for tuning

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O/E†	DESCRIPTION
$\overline{\text{MBRQ}}$	36	I/O	Reserved; must be pulled high (see Note 3)
$\overline{\text{MCAS}}$	18	O	Column-address strobe for DRAMs. The column address is valid for the 3/16 of the memory cycle following the row-address portion of the cycle. $\overline{\text{MCAS}}$ is driven low every memory cycle while the column address is valid on MADL0–MADL7, MAXPH, and MAXPL, except when one of the following conditions occurs: • When the address accessed is in the BIA ROM (>00.0000 – >00.000F) • When the address accessed is in the EPROM memory map (i.e., when the BOOT bit in the SIFACL register is zero and an access is made between >00.0010 and >00.FFFF or >1F.0000 and >1F.FFFF) • When the cycle is a refresh cycle, in which case $\overline{\text{MCAS}}$ is driven low at the start of the cycle before $\overline{\text{MRAS}}$ (for DRAMs that have $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh). For DRAMs that do not support $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, it can be necessary to disable $\overline{\text{MCAS}}$ with MREF during the refresh cycle.
MDDIR	15	I/O	Data direction. MDDIR is used as a direction control for bidirectional bus drivers. MDDIR becomes valid before $\overline{\text{MBEN}}$ becomes active. H = TI380C30 memory-bus write L = TI380C30 memory-bus read
$\overline{\text{MOE}}$	23	O	Memory-output enable. $\overline{\text{MOE}}$ enables the outputs of the DRAM memory during a read cycle. $\overline{\text{MOE}}$ is high for EPROM or BIA ROM read cycles. H = Disable DRAM outputs L = Enable DRAM outputs
$\overline{\text{MRAS}}$	20	O	Row-address strobe for DRAMs. The row address lasts for the first 5/16 of the memory cycle. $\overline{\text{MRAS}}$ is driven low every memory cycle while the row address is valid on MADL0–MADL7, MAXPH, and MAXPL for both RAM and ROM cycles. $\overline{\text{MRAS}}$ is also driven low during refresh cycles when the refresh address is valid on MADL0–MADL7.
MREF	1	O	DRAM refresh cycle in progress. MREF indicates that a DRAM refresh cycle is occurring. It is also used for disabling $\overline{\text{MCAS}}$ to all DRAMs that do not use a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh. H = DRAM refresh cycle in process L = Not a DRAM refresh cycle
$\overline{\text{MRESET}}$	175	O	Memory-bus reset. $\overline{\text{MRESET}}$ is a reset signal generated when either the ARESET bit in the SIFACL register is set or $\overline{\text{SRESET}}$ is asserted. $\overline{\text{MRESET}}$ is used for resetting external local-bus glue logic. H = External logic not reset L = External logic reset
$\overline{\text{MROMEN}}$	4	O	ROM enable. During the first 5/16 of the memory cycle, $\overline{\text{MROMEN}}$ is used to provide a chip select for ROMs when the BOOT bit of the SIFACL is zero (i.e., when code is resident in ROM, not RAM). $\overline{\text{MROMEN}}$ can be latched by $\overline{\text{MAL}}$. $\overline{\text{MROMEN}}$ goes low for any read from addresses >00.0010 – >00.FFFF or >1F.0000 – >1F.FFFF when the BOOT bit in the SIFACL register is zero. $\overline{\text{MROMEN}}$ stays high for writes to these addresses, accesses of other addresses, or accesses of any address when the BOOT bit is 1. During the final three quarters of the memory cycle, $\overline{\text{MROMEN}}$ outputs the A13 address signal for interfacing to a BIA ROM. This means $\overline{\text{MBIAEN}}$, MAX0, $\overline{\text{ROMEN}}$, and MAX2 form a glueless interface for the BIA ROM. H = ROM disabled L = ROM enabled

† I = input, O = output, E = provides external-component connection to the internal circuitry for tuning
NOTE 3: Each pin must be individually tied to V_{DD} with a 1-kΩ pullup resistor.

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O/E†	DESCRIPTION
$\overline{MW}$	19	O	Local-memory write. $\overline{MW}$ is used to specify a write cycle on the local-memory bus. The data on the MADH0–MADH7 and MADL0–MADL7 buses is valid while $\overline{MW}$ is low. DRAMs latch data on the falling edge of $\overline{MW}$, while SRAMs latch data on the rising edge of $\overline{MW}$. H = Not a local-memory write cycle L = Local-memory write cycle
NABL	156	I	Output-enable control. NABL is used in the physical-layer circuitry (see Note 3).
NC	135 166		These pins should be left unconnected.
$\overline{NMI}$	55	I	Nonmaskable interrupt request. $\overline{NMI}$ must be left unconnected.
NSELOUT0 NSELOUT1	58 171	O O	Network selection outputs. NSELOUT0 and NSELOUT1 are controlled by the host through the corresponding bits of the SIFACL register. The value of NSELOUT0 and NSELOUT1 can be changed only while the TI380C30 is reset. NSELOUT0 NSELOUT1 DESCRIPTION L H 16-Mbps token ring H H 4-Mbps token ring
$\overline{NSRT}$	121	O	Insert control. $\overline{NSRT}$ enables the phantom-driver outputs (PHOUTA and PHOUTB) through the watchdog timer for insertion onto the token ring. Static high = Inactive, phantom current removed (due to watchdog timer) Static low = Inactive, phantom current removed (due to watchdog timer) Falling edge = Active, current output on PHOUTA and PHOUTB
OSC32	5	O	Oscillator output . OSC32 provides a 32-MHz clock output and can be used to drive OSCIN and one other TTL load.
OSCIN	6	I	External oscillator input. OSCIN provides the clock frequency to the TI380C30 for a 4-MHz or 6-MHz internal bus (see Notes 5 and 6). CLKDIV OSCIN H 64 MHz for a 4-MHz local bus L 32 MHz for a 4-MHz local bus or 48 MHz for a 6-MHz local bus
OSCOUT	172	O	Oscillator output CLKDIV OSCOUT L OSCIN ÷ 4 (if OSCIN = 32 MHz, OSCOUT = 8 MHz; if OSCIN = 48 MHz, OSCOUT = 12 MHz) H OSCIN ÷ 8 (if OSCIN = 64 MHz, OSCOUT = 8 MHz)
PHOUTA PHOUTB	139 141	O O	Phantom-driver outputs A and B. PHOUTA and PHOUTB cause insertion onto the token ring. PHOUTA and PHOUTB should be connected to the center tap of the transmit transformer secondary winding for phantom-drive generation.
PRTYEN	59	I	Parity enable. The value on PRTYEN is loaded into the PEN bit of the SIFACL register at reset (i.e., when $\overline{SRESET}$ is asserted or the ARESET bit in the SIFACL register is set) to form a default value. PRTYEN enables parity checking for the local memory. H = Local-memory data bus checked for parity (see Note 1). L = Local-memory data bus not checked for parity.
$\overline{PWRDN}$	154	I	Power-down control H = Normal operation L = TI380C30 physical-layer circuitry is placed into a power-down state. All TTL outputs of the physical layer are driven to the high-impedance state.
PXTAL	163	O	Reference-clock output. PXTALIN is synthesized from the 8-MHz crystal oscillator used for XT1 and XT2.

† I = input, O = output, E = provides external-component connection to the internal circuitry for tuning

NOTES: 1. Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).
3. Each pin must be individually tied to V_{DD} with a 1-kΩ pullup resistor.
5. Pin has an expanded input voltage specification.
6. A maximum of two TI380C30 devices can be connected to any one oscillator.

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O/E†	DESCRIPTION
$\overline{\text{RATER}}$	158	O	$\overline{\text{RATER}}$ indicates that there are transitions on the RCV+/RCV– input pair (DRVR+/DRVR– if $\overline{\text{WRAP}}$ is asserted low) but that the transition rate is not consistent with the ring speed selected by the S4/$\overline{16}$ pin.
RCLK	161	O	Recovered clock. RCLK is the clock recovered from the token-ring received data. For 16-Mbps operation, it is a 32-MHz clock. For 4-Mbps operation, it is an 8-MHz clock.
RCV+ RCV–	149 147	I I	Receiver. RCV+ and RCV– are differential inputs that receive the token-ring data via isolation transformers.
RCVR	162	O	Recovered data. RCVR contains the data recovered from the token ring.
$\overline{\text{REDY}}$	124	O	PLL ready. $\overline{\text{REDY}}$ is normally asserted (active) low. It is cleared following the assertion of FRAQ and reasserted after the data recovery PLL has been reinitialized. H = Received data not valid L = Received data valid
RES	137	—	Reserved. Should be left unconnected.
SADH0 SADH1 SADH2 SADH3 SADH4 SADH5 SADH6 SADH7	110 109 108 107 106 105 101 100	I/O	System address/data bus—high byte (see Note 1).These lines make up the most significant byte of each address word (32-bit address bus) and data word (16-bit data bus). The most significant bit is SADH0, and the least significant bit is SADH7. Address multiplexing: Bits 31 – 24 and bits 15 – 8‡ Data multiplexing: Bits 15 – 8‡
SADL0 SADL1 SADL2 SADL3 SADL4 SADL5 SADL6 SADL7	91 90 89 86 85 84 83 82	I/O	System address/data bus—low byte (see Note 1). These lines make up the least significant byte of each address word (32-bit address bus) and data word (16-bit data bus). The most significant bit is SADL0, and the least significant bit is SADL7. Address multiplexing: Bits 23 – 16 and bits 7 – 0‡ Data multiplexing: Bits 7 – 0‡
SALE	80	O	System address-latch enable. SALE is the enable pulse used to externally latch the 16 LSBs of the address from the SADH0 – SADH7 and SADL0 – SADL7 buses at the start of the DMA cycle. Systems that implement address parity can also externally latch the parity bits (SPH and SPL) for the latched address.
$\overline{\text{SBBSY}}$	68	I	System bus busy. The TI380C30 samples the value on $\overline{\text{SBBSY}}$ during arbitration (see Note 1). The sample has one of two values: H = Not busy. The TI380C30 can become bus master if the grant condition is met. L = Busy. The TI380C30 cannot become bus master.
SBCLK	81	I	System bus clock. The TI380C30 requires the external clock to synchronize its bus timings for all DMA transfers. Valid frequencies are 2 MHz–33 MHz.
$\overline{\text{SBHE}}$/SRNW	94	I/O	**Intel Mode:** $\overline{\text{SBHE}}$ is used for system byte high enable. $\overline{\text{SBHE}}$ is a 3-state output driven during DMA; it is an input at all other times. H = System byte high not enabled (see Note 1) L = System byte high enabled
			Motorola Mode: SRNW is used for system read not write. SRNW serves as a control signal to indicate a read or write cycle. H = Read cycle (see Note 1) L = Write cycle

† I = input, O = output, E = provides external-component connection to the internal circuitry for tuning
‡ Typical bit ordering for Intel™ and Motorola processor buses
NOTE 1: Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).

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ADVANCE INFORMATION

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O/E†	DESCRIPTION
$\overline{\text{SBRLS}}$	67	I	System-bus release. $\overline{\text{SBRLS}}$ indicates to the TI380C30 that a higher-priority device requires the system bus. The value on $\overline{\text{SBRLS}}$ is ignored when the TI380C30 is not performing DMA. $\overline{\text{SBRLS}}$ is internally synchronized to SBCLK. H = The TI380C30 can hold onto the system bus (see Note 1). L = The TI380C30 should release the system bus upon completion of current DMA cycle. If the DMA transfer is not yet complete, the SIF rearbitrates for the system bus.
$\overline{\text{SCS}}$	66	I	System-chip select. $\overline{\text{SCS}}$ activates the system interface of the TI380C30 for a DIO read or write. H = Not selected (see Note 1) L = Selected
$\overline{\text{SDBEN}}$	95	O	System data-bus enable. $\overline{\text{SDBEN}}$ signals to the external data buffers to begin driving data. $\overline{\text{SDBEN}}$ is activated during both DIO and DMA. H = Keep external data buffers in the high-impedance state L = Cause external data buffers to begin driving data
SDDIR	75	O	System data direction. SDDIR provides to the external data buffers a signal indicating the direction in which the data is moving. During DIO writes and DMA reads, SDDIR is low (data direction is into the TI380C30). During DIO reads and DMA writes, SDDIR is high (data direction is out from the TI380C30). When the system interface is not involved in a DIO or DMA operation, SDDIR is high by default. SDDIR: H / L DATA DIRECTION: output / input DIO: read / write DMA: write / read
SHLDA/$\overline{\text{SBGR}}$	74	I	Intel Mode: SHLDA is used for system-hold acknowledge. SHLDA indicates that the system DMA-hold request has been acknowledged. SHLDA is internally synchronized to SBCLK (see Note 1). H = Hold request acknowledged L = Hold request not acknowledged
			Motorola Mode: $\overline{\text{SBGR}}$ is used for system bus grant. $\overline{\text{SBGR}}$ is an active-low bus grant, as defined in the standard 68xxx interface, and is internally synchronized to SBCLK (see Note 1). H = System bus not granted L = System bus granted
SHRQ/$\overline{\text{SBRQ}}$	93	O	Intel Mode: SHRQ is used for system-hold request. SHRQ is used to request control of the system bus in preparation for a DMA transfer. SHRQ is internally synchronized to SBCLK. H = System bus requested L = System bus not requested
			Motorola Mode: $\overline{\text{SBRQ}}$ is used for system-bus request. $\overline{\text{SBRQ}}$ is used to request control of the system bus in preparation for a DMA transfer. $\overline{\text{SBRQ}}$ is internally synchronized to SBCLK. H = System bus not requested L = System bus requested
$\overline{\text{SIACK}}$	61	I	System-interrupt acknowledge. SIACK is from the host processor to acknowledge the interrupt request from the TI380C30. H = System interrupt not acknowledged (see Note 1) L = System interrupt acknowledged: The TI380C30 places its interrupt vector onto the system bus.

† I = input, O = output, E = provides external-component connection to the internal circuitry for tuning

NOTE 1: Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O/E†	DESCRIPTION	
SI/$\overline{M}$	72	I	System-Intel/Motorola mode select. The value on SI/$\overline{M}$ specifies the system-interface mode. H = Intel-compatible-interface mode selected. Intel interface can be 8-bit or 16-bit mode (see S8/$\overline{SHALT}$ description and Note 1). L = Motorola-compatible-interface mode selected. Motorola-interface mode is always 16 bits.	
SINTR/$\overline{SIRQ}$	73	O	Intel Mode	SINTR is used for system-interrupt request. TI380C30 activates SINTR to signal an interrupt request to the host processor. H = Interrupt request by TI380C30 L = No interrupt request
			Motorola Mode	$\overline{SIRQ}$ is used for system-interrupt request. TI380C30 activates $\overline{SIRQ}$ to signal an interrupt request to the host processor. H = No interrupt request L = Interrupt request by TI380C30
$\overline{SOWN}$	96	O	System bus owned. $\overline{SOWN}$ indicates to external devices that TI380C30 has control of the system bus. $\overline{SOWN}$ drives the enable signal of the bus-transceiver chips that drive the address and bus-control signals. H = TI380C30 does not have control of the system bus. L = TI380C30 has control of the system bus.	
SPH	99	I/O	System parity high. SPH is the optional odd-parity bit for each address or data byte transmitted over SADH0–SADH7 (see Note 1).	
SPL	92	I/O	System parity low. SPL is the optional odd-parity bit for each address or data byte transmitted over SADL0–SADL7 (see Note 1).	
SRAS/$\overline{SAS}$	76	I/O	Intel Mode	SRAS is used for system memory-address strobe (see Note 7). SRAS is used to latch the $\overline{SCS}$ and SRSX – SRS2 register input signals. In a minimum-chip system, SRAS is tied to the SALE output of the system bus. The latching capability can be defeated since the internal latch for these inputs remains transparent as long as SRAS remains high. This permits SRAS to be pulled high and the signals at $\overline{SCS}$, SRSX – SRS2, and $\overline{SBHE}$ to be applied independently of the SALE strobe from the system bus. During DMA, SRAS remains an input. H = Transparent mode L = Holds latched values of $\overline{SCS}$, SRSX–SRS2, and $\overline{SBHE}$ Falling edge = Latches $\overline{SCS}$, SRSX – SRS2, and $\overline{SBHE}$
			Motorola Mode	$\overline{SAS}$ is used for sytem-memory address strobe (see Note 7). $\overline{SAS}$ is an active-low address strobe that is an input during DIO (although ignored as an address strobe) and an output during DMA. H = Address is not valid. L = Address is valid and a transfer operation is in progress.

† I = input, O = output, E = provides external-component connection to the internal circuitry for tuning

NOTES: 1. Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).
7. Pin should be tied to V_{DD} with a 4.7-kΩ pullup resistor.

ADVANCE INFORMATION

Pin Functions (Continued)

PIN NAME	NO.	I/O/E†		DESCRIPTION
$\overline{SRD}$/$\overline{SUDS}$	98	I/O	Intel Mode	$\overline{SRD}$ is used for system-read strobe (see Note 7). $\overline{SRD}$ is the active-low strobe indicating that a read cycle is performed on the system bus. $\overline{SRD}$ is an input during DIO and an output during DMA. H = Read cycle is not occurring. L = If DMA, host provides data to system bus. If DIO, SIF provides data to system bus.
			Motorola Mode	$\overline{SUDS}$ is used for upper-data strobe (see Note 7). $\overline{SUDS}$ is the active-low upper-data strobe. $\overline{SUDS}$ is an input during DIO and an output during DMA. H = Not valid data on SADH0–SADH7 lines L = Valid data on SADH0–SADH7 lines
$\overline{SRDY}$/$\overline{SDTACK}$	97	I/O	Intel Mode	$\overline{SRDY}$ is used for system bus ready (see Note 7). $\overline{SRDY}$ indicates to the bus master that a data transfer is complete. $\overline{SRDY}$ is asynchronous but during DMA and pseudo-DMA cycles, it is internally synchronized to SBCLK. During DMA cycles, $\overline{SRDY}$ must be asserted before the falling edge of SBCLK in state T2 in order to prevent a wait state. $\overline{SRDY}$ is an output when the TI380C30 is selected for DIO; otherwise, it is an input. H = System bus is not ready. L = Data transfer is complete; system bus is ready.
			Motorola Mode	$\overline{SDTACK}$ is used for system data-transfer acknowledge (see Note 7). The purpose of $\overline{SDTACK}$ is to indicate to the bus master that a data transfer is complete. $\overline{SDTACK}$ is internally synchronized to SBCLK. During DMA cycles, $\overline{SDTACK}$ must be asserted before the falling edge of SBCLK in state T2 in order to prevent a wait state. $\overline{SDTACK}$ is an output when the TI380C30 is selected for DIO; otherwise, it is an input. H = System bus is not ready. L = Data transfer is complete; system bus is ready.
$\overline{SRESET}$	62	I		System reset. $\overline{SRESET}$ is activated to place the TI380C30 into a known initial state. Hardware reset puts most of the TI380C30 outputs into the high-impedance state and places all blocks into the reset state. The Intel-mode DMA bus-width selection (S8) is latched on the rising edge of $\overline{SRESET}$. H = No system reset L = System reset Rising edge = Latch bus width for DMA operations (for Intel-mode applications)
SRSX SRS0 SRS1 SRS2/$\overline{SBERR}$	65 64 63 70	I	Intel Mode	SRSX and SRS0–SRS2 are used for system-register select. These inputs select the word or byte to be transferred during a system DIO access. The most significant bit is SRSX and the least significant bit is SRS2 (see Note 1). MSb LSb Register selected = SRSX SRS0 SRS1 SRS2/$\overline{SBERR}$
			Motorola Mode	SRSX, SRS0 and SRS1 are used for system-register select. These inputs select the word or byte to be transferred during a system DIO access. The most significant bit is SRSX and the least significant bit is SRS1 (see Note 1). MSb LSb Register selected = SRSX SRS0 SRS1 $\overline{SBERR}$ is used for bus error. $\overline{SBERR}$ corresponds to the bus-error signal of the 68xxx microprocessor. It is internally synchronized to SBCLK. $\overline{SBERR}$ is driven low during a DMA cycle to indicate to the TI380C30 that the cycle must be terminated (see Section 3.4.5.3 of the *TMS380 Second-Generation Token-Ring User's Guide* (SPWU005) for more information).

† I = input, O = output, E = provides external-component connection to the internal circuitry for tuning

NOTES: 1. Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).
7. Pin should be tied to V_{DD} with a 4.7-kΩ pullup resistor.

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O/E†	DESCRIPTION	
SWR/SLDS	77	I/O	Intel Mode	SWR is used for system-write strobe (see Note 7). SWR is an active-low write strobe that is an input during DIO and an output during DMA. H = Write cycle is not occurring. L = If DMA, data to be driven from SIF to host bus. If DIO, on the rising edge, the data is latched and written to the selected register.
			Motorola Mode	SLDS is used for lower-data strobe (see Note 7). SLDS is an input during DIO and an output during DMA. H = Not valid data on SADL0–SADL7 lines L = Valid data on SADL0–SADL7 lines
SXAL	79	O	System extended-address latch. SXAL provides the enable pulse used to externally latch the most significant 16 bits of the 32-bit system address during DMA. SXAL is activated prior to the first cycle of each block DMA transfer, and thereafter as necessary (whenever an increment of the DMA address counter causes a carry out of the lower 16 bits). Systems that implement parity on addresses can use SXAL to externally latch the parity bits (available on SPL and SPH) for the DMA address extension.	
SYNCIN	12	I	Reserved. SYNCIN must be left unconnected (see Note 1).	
S4/16	155	I	Speed switch. S4 / 16 specifies the token-ring data rate. H = 4-Mbps data rate L = 16-Mbps data rate	
S8/SHALT	69	I	Intel Mode	S8 is used for system 8-/16-bit bus select. S8 selects the bus width used for communications through the system interface. On the rising edge of SRESET, the TI380C30 latches the DMA bus width; otherwise, the value on S8 dynamically selects the DIO bus width. H = Selects 8-bit mode (see Note 1) L = Selects 16-bit mode
			Motorola Mode	SHALT is used for system halt/bus error retry. If SHALT is asserted along with bus error (SBERR), the adapter retries the last DMA cycle. This is the rerun operation as defined in the 68xxx specification. The BERETRY counter is not decremented by SBERR when SHALT is asserted (see Section 3.4.5.3 of the *TMS380 Second-Generation Token-Ring User's Guide* (SPWU005) for more information).
TCLK TMS TDI TDO	7 8 165 164	I I I O	Test ports used during the production test of the device. Should be left unconnected.	
TEST0 TEST1 TEST2	116 115 114	I I I	Network select inputs. TEST0–TEST2 are used to select the network speed and type to be used by the TI380C30. These inputs should be changed only during adapter reset. Connect TEST2 to V_{DDL}. TEST0 TEST1 TEST2 DESCRIPTION L NC H 16-Mbps token ring H NC H 4-Mbps token ring X X L Reserved	
TEST3 TEST4 TEST5	113 112 111	I I I	Test inputs. TEST3–TEST5 should be left unconnected (see Note 1). Module-in-place test mode is achieved by tying TEST3 and TEST4 to ground. In this mode, all TI380C30 outputs are in the high-impedance state. Internal pullups on all TI380C30 inputs are disabled (except TEST3–TEST5).	
TRST	9	I	Test-port reset. TRST should be tied to ground for normal operation of the TI380C30. H = Reserved L = Test ports forced to an idle state	

† I = input, O = output, E = provides external-component connection to the internal circuitry for tuning

NOTES: 1. Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).
7. Pin should be tied to V_{DD} with a 4.7-kΩ pullup resistor.

ADVANCE INFORMATION

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O/E†	DESCRIPTION
V_{DD}	14 29 45 87 103 119	—	Positive-supply voltage for output buffers. All V_{DD} pins must be attached to the common-system power-supply plane.
V_{DDA1}	148	—	Positive-supply voltage for receiver circuits
V_{DDA2}	129	—	Positive-supply voltage for data recovery PLL
V_{DDA3}	123		Positive-supply voltage for the current-bias generator
V_{DDD}	157	—	Positive-supply voltage for output buffers
V_{DDL}	13 47 71	—	Positive-supply voltage for digital logic. All V_{DDL} pins must be attached to the common-system power-supply plane.
$V_{DDL(1)}$	134 146	—	Positive-supply voltage for digital logic. All V_{DDL} pins must be attached to the common-system power-supply plane.
V_{DDO}	133	—	Positive-supply voltage for XTAL oscillator
V_{DDP}	138	—	Positive-supply voltage for phantom drive
V_{DDX}	145	—	Positive-supply voltage for transmit output
V_{SS}	11 30 38 78 104	—	Ground connections for output buffers. All V_{SS} pins must be attached to system ground plane.
V_{SSA1}	150	—	Ground reference for receiver circuits
V_{SSA2}	127	—	Ground reference for data recovery PLL
V_{SSA3}	125		Ground reference for the current-bias generator
V_{SSC}	10 21 57 102	—	Ground reference for output buffers (clean ground). All V_{SSC} pins must be attached to the common-system ground plane.
$V_{SSC(1)}$	160		Ground reference for output buffers
V_{SSD}	159	—	Ground reference for output buffers
V_{SSL}	22 46 88 120	—	Ground reference for digital logic. All V_{SSL} pins must be attached to the common-system ground plane.
$V_{SSL(1)}$	136, 153	—	Ground reference for internal logic
V_{SSO}	131	—	Ground reference for XTAL oscillator
V_{SSP}	140	—	Ground reference for phantom drive
V_{SSX}	142	—	Ground reference for transmit output
$\overline{WFLT}$	167	O	Phantom-wire fault. $\overline{WFLT}$ provides an indication of the presence of a short or open circuit on PHOUTA or PHOUTB. H = No fault L = Open or short. The DC fault condition is present in the phantom-drive lines.

† I = input, O = output, E = provides external-component connection to the internal circuitry for tuning

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O/E†	DESCRIPTION
$\overline{\text{WRAP}}$	170	O	Internal wrap mode control. $\overline{\text{WRAP}}$ indicates the TI380C30 has placed the physical layer in the loopback-wrap mode for adapter self test. H = Normal ring operation L = Physical-layer wrap mode selected
XFAIL	117	I	External fail-to-match signal. An enhanced address copy option (EACO) device uses XFAIL to indicate to the TI380C30 that it should not copy the frame nor set the ARI/FCI bits in a token-ring frame due to an external address match. The ARI/FCI bits in a token-ring frame can be set due to an internal address-matched frame. If an EACO device is not used, XFAIL must be left unconnected. XFAIL is ignored when CAF mode is enabled [see table in XMATCH description section (see Note 1)]. H = No address match by external address checker L = External address-checker-armed state
XMATCH	118	I	External match signal. An EACO device uses XMATCH to indicate to the TI380C30 to copy the frame and set the ARI/FCI bits in a token-ring frame. If an EACO device is not used, XMATCH must be left unconnected. XMATCH is ignored when CAF mode is enabled (see Note 1). H = Address match recognized by external address checker L = External address-checker-armed state XMATCH / XFAIL / FUNCTION 0 / 0 / Armed (processing frame data) 0 / 1 / Do not externally match the frame (XFAIL takes precedence) 1 / 0 / Copy the frame 1 / 1 / Do not externally match the frame (XFAIL takes precedence) Hi-Z / Hi-Z / Reset state (adapter not initialized)
XMT+ XMT–	143 144	E	Transmit differential outputs XMT+ and XMT– provide a low-impedance differential source for line drive via filtering and transformer isolation.
XT1 XT2	130 132	I E	XTAL connection. An 8-MHz crystal network can be connected here to provide a reference clock for the TI380C30. Alternatively, an 8-MHz TTL clock source can be connected to XT1.

† I = input, O = output, E = provides external-component connection to the internal circuitry for tuning

NOTE 1: Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).

architecture

The major blocks of the TI380C30 include the communications processor (CP), system interface (SIF), memory interface (MIF), protocol handler (PH), clock generator (CG), adapter-support function (ASF), and physical-layer interface. The functionality of each block is described in the following sections.

communications processor (CP)

The CP performs the control and monitoring of the other functional blocks in the TI380C30. The control and monitoring protocols are specified by the software (downloaded or ROM-based) in local memory. Available protocols include:

- Media access control (MAC) software
- Logical link control (LLC) software
- Copy all frames (CAF) software

The CP is a proprietary 16-bit central processing unit (CPU) with data cache and a single prefetch pipe for pipelining of instructions. These features enhance the TI380C30 maximum performance capability to about 8 million instructions per second (MIPS) with an average of about 5 MIPS.

system interface (SIF)

The SIF performs the interfacing of the LAN subsystem to the host system. This interface may require additional logic depending on the application. The system interface can transfer information/data using any of these three methods:

- Direct memory access (DMA)
- Direct input/output (DIO)
- Pseudo-direct memory access (PDMA)

DMA (or PDMA) is used to transfer all data to/from host memory from/to local memory. The main uses of DIO are for loading the software to local memory and for initializing the TI380C30. DIO also allows command/status interrupts to occur to and from the TI380C30.

The system interface can be hardware selected for either of two modes by using SI/$\overline{M}$. The mode selected determines the memory organizations and control signals used. These modes are:

- The Intel mode (80x8x families): 8-, 16-, and 32-bit bus devices
- The Motorola mode (68xxx microprocessor family): 16- and 32-bit bus devices

The system interface supports host-system memory addressing up to 32 bits (32-bit reach into the host system memory). This allows greater flexibility in using/accessing host-system memory. System designers are allowed to customize the system interface to their particular bus by:

- Programmable burst transfers or cycle-steal DMA operations
- Optional parity protection

These features are implemented in hardware to reduce system overhead, facilitate automatic rearbitration of the bus after a burst, or repeat a cycle when errors occur (parity or bus). Bus retries are also supported.

The system-interface hardware also includes features to enhance the integrity of the TI380C30 operation and the data. These features include the following:

- Always internally maintain odd-byte parity regardless of parity being disabled
- Monitor for the presence of a clock failure
- Provide switchable SIF speeds at 2MHz to 33MHz

On every cycle, the system interface compares all the system clocks to a reference clock. If any of the clocks become invalid, the TI380C30 enters the slow-clock mode which prevents latch-up of the TI380C30. If the SBCLK is invalid, any DMA cycle is terminated immediately; otherwise, the DMA cycle is completed and the TI380C30 is placed in slow-clock mode.

system interface (SIF) (continued)

When the TI380C30 enters the slow-clock mode, the clock that failed is replaced by a slow free-running clock, and the device is placed into a low-power reset state. When the failed clock(s) return to valid operation, the TI380C30 must be reinitialized.

For DMA with a 16-MHz clock, a continuous transfer rate of 64 Mbps (8 MBps) can be obtained. For DMA with a 25-MHz clock, a continuous transfer rate of 96 Mbps (12 MBps) can be obtained. For DMA with a 33-MHz clock, a continuous transfer rate of 128 Mbps (16MBps) can be obtained. For 8-bit and 16-bit pseudo-DMA, the following data rates can be obtained:

LOCAL BUS SPEED	8-BIT PDMA	16-BIT PDMA
4 MHz	48 Mbps	64 Mbps
6 MHz	72 Mbps	96 Mbps

Since the main purpose of DIO is for downloading and initialization, the DIO transfer rate is not a significant issue.

memory interface (MIF)

The MIF performs memory management to allow the TI380C30 to address 2 Mbytes in local memory. Hardware in the MIF allows the TI380C30 to be directly connected to DRAMs without additional circuitry. This glueless-DRAM connection includes the DRAM refresh controller. The MIF also handles all internal bus arbitration between these blocks. When required, the MIF arbitrates for the external bus.

The MIF is responsible for the memory mapping of the CPU of a task. The memory map of DRAMs, EPROMs, burned-in addresses (BIA), and external devices are appropriately addressed when required by the system interface, protocol handler when required for a DMA transfer. The memory interface is capable of a 64-Mbps continuous transfer rate when using a 4-MHz local bus (64-MHz device crystal) and a 96-Mbps continuous transfer rate when using a 6-MHz local bus.

protocol handler (PH)

The PH performs the hardware-based real-time protocol functions for a token-ring LAN. Network type is determined by TEST0–TEST2. Token-ring network is determined by software and can be either 16 Mbps or 4 Mbps. These speeds are fixed by the software not by the hardware.

The PH converts the parallel-transmit data to serial-network data of the appropriate coding and converts the received serial data to parallel data. The PH data-management state machines direct the transmission/reception of data to/from local memory through the MIF. The PH buffer-management state machines automatically oversee this process, directly sending/receiving linked lists of frames without CPU intervention.

The PH contains many state machines that provide the following features:

- Transmit and receive frames
- Capture tokens
- Provide token-priority controls
- Manage the TI380C30 buffer memory
- Provide frame-address recognition (group, specific, functional, and multicast)
- Provide internal parity protection
- Control and verify the physical-layer circuitry-interface signals

Integrity of the transmitted and received data is assured by cyclic-redundancy checks (CRC), detection of network-data violations, and parity on internal data paths. All data paths and registers are optionally parity protected to assure functional integrity.

adapter-support function (ASF)

The ASF performs support functions not contained in the other blocks. The features are:

- The TI380C30 base timer
- Identification, management, and service of internal and external interrupts
- Test-pin mode control, including the unit-in-place mode for board testing
- Checks for illegal states, such as illegal opcodes and parity

clock generator (CG)

The CG performs the generation of all internal clocks required by the other functional blocks, including the local memory-bus clocks (MBCLK1, MBCLK2). The CG also generates the reference timer used to sample all input clocks (SBCLK, OSCIN, RCLK, and PXTALIN). If no transition is detected within the period of the reference timer on any input clock signal, the CG places the TI380C30 into slow-clock mode. The frequency of the reference timer is in the range of 10 kHz–100 kHz.

physical-layer interface (PHY)

The major blocks of the TI380C30 PHY include the receiver/equalizer, clock recovery PLL, wrap function, phantom drive with wire-fault detector, and watchdog timer. Figure 2 is the block diagram illustrating these major blocks, and the functionality of each block is described in the following sections.

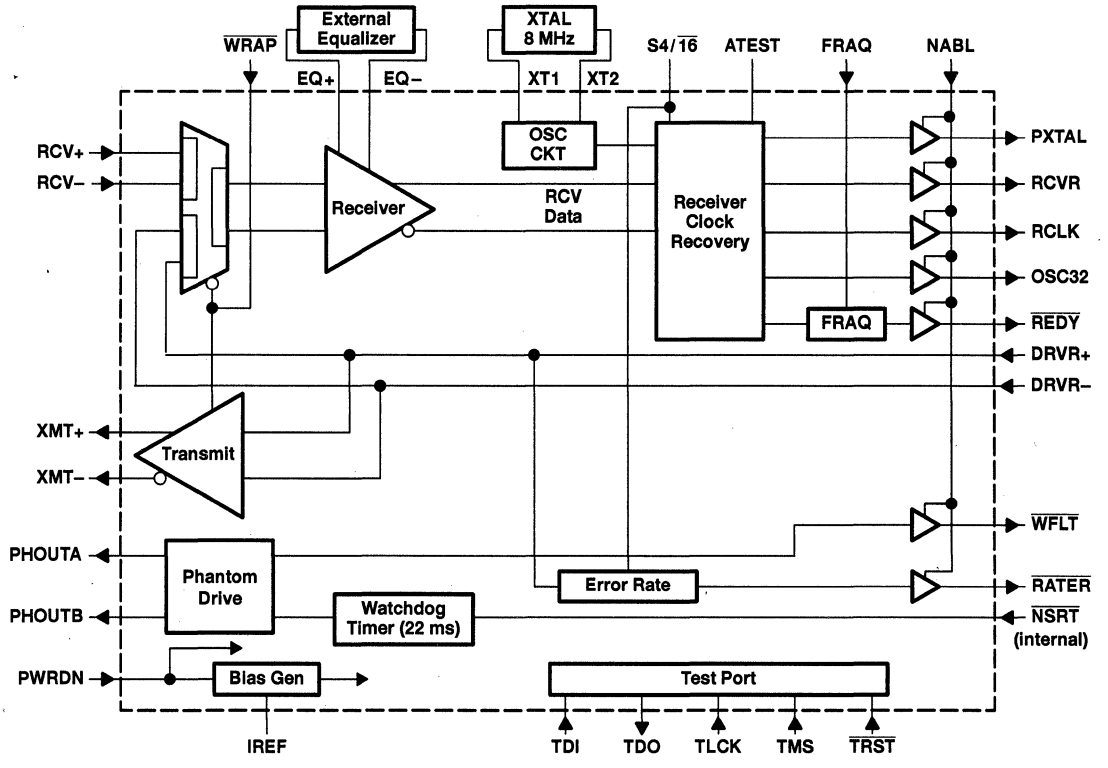


Figure 2. Functional Block Diagram of the PHY

receiver

Figure 3 shows the arrangement of the line-receiver/equalizer circuit. The differential-input pair, RCV+ and RCV–, are designed to be connected to a floating winding of an isolation transformer. Each is equipped with a bias circuit to center the operating point of the differential input at approximately $V_{DD} \div 2$.

The differential-input pair consists of a pair of MOSFETs, each with an identical current source in its source terminal that is set to supply a nominal current of 1.5 mA. At low signal levels, the gain of this pair is inversely proportional to the impedance connected between their sources on EQ– and EQ+. A frequency-equalization network can be connected between EQ+ and EQ– to provide equalization for media-signal distortion.

The internal-wrap mode is provided for self test of the device. When selected by taking $\overline{\text{WRAP}}$ low, the normal input path is disabled by a multiplexer and a path is enabled from the DRVR+/DRVR– input pair. Receiver gain, thresholds, and equalization are unchanged in the internal-wrap mode.

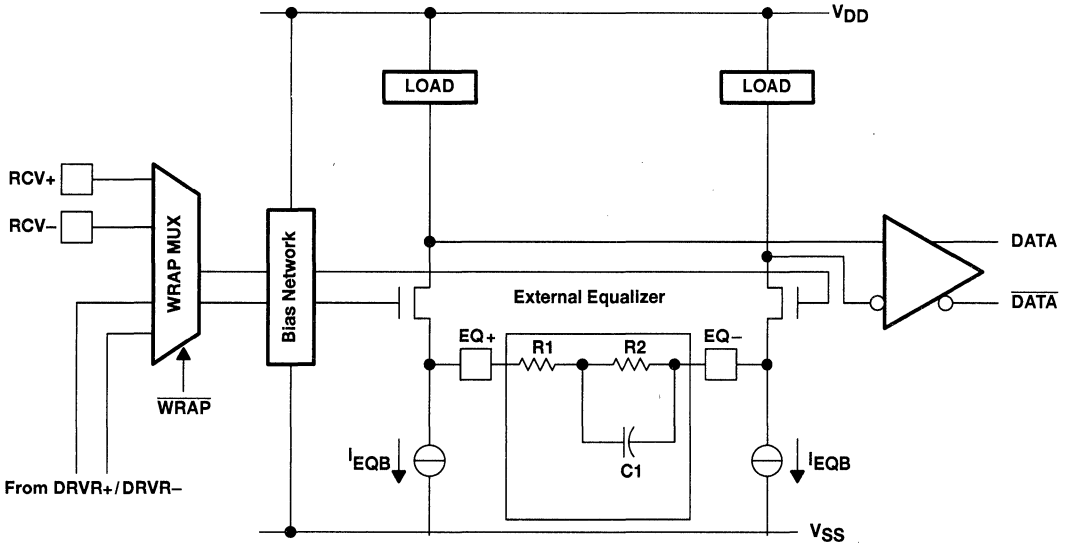


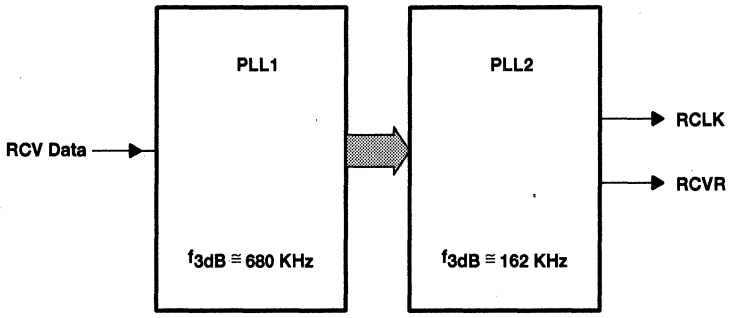
Figure 3. Line Receiver/Equalizer

receiver-clock recovery

The clock and data recovery in TI380C30 is performed by an advanced, digitally controlled phase-locked loop. In contrast to the TMS38054, the PLL of the TI380C30 is digitally controlled and the loop parameters are set by internally programmed digital constants. This results in precise control of loop parameters and requires no external loop-filter components.

The TI380C30 implements an intelligent algorithm to determine the optimum phase position for data sampling and extracted-clock synthesis. The resulting action of the TI380C30 can be modeled as two cascaded PLLs as shown in Figure 4.

receiver-clock recovery (continued)



NOTE: f_{3dB} = 3dB bandwidth of PLL

Figure 4. Dual PLL Arrangement

PLL1 represents the algorithm to recover data from the incoming stream detected by the receiver. It has a relatively high bandwidth to provide good jitter tolerance. Data and embedded-clock-phase information are fed as digital values to PLL2 that generates the extracted clock (RCLK) for the TI380C30 commprocessor. The recovered data is sent to the TI380C30 as the RCVR signal synchronously with RCLK. In addition to sampling the RCVR signal, the TI380C30 uses RCLK to retransmit data in most cases. The lower bandwidth of PLL2 greatly reduces the rate of accumulation of data-correlated phase jitter in a token-ring network and provides very good accumulated-phase-slope (APS) characteristics. In addition to RCLK, the token-ring reference clock (PXTAL) and a fixed-frequency 32-MHz clock (OSC32) are also synthesized from the 8-MHz crystal reference.

line driver and wrap function

The line-drive function of the TI380C30 is performed by XMT+ / XMT–. Unlike the TMS38054, these pins are low-impedance outputs and require external-series resistance to provide line termination. These pins provide buffering of the differential signal from the PH on DRVR+/DRVR– with action to control skew and asymmetry, and with no retiming in the transmit path.

The wrap function is designed to provide a signal path for system self-test diagnostics. When the PH drives $\overline{\text{WRAP}}$ low, the receiver inputs are ignored and the transmit signal is fed to the receiver input circuitry via a multiplexer. In the internal wrap mode, $\overline{\text{WRAP}}$ can be checked by observing the signal amplitude at the equalization pins, EQ+ and EQ–. Equalization is active at this signal level, although the signal does not exhibit the high-frequency attenuation effects for which equalization is intended to compensate. During wrap mode, both XMT+ / XMT– are driven to a low state to prevent any dc current flowing in the isolation transformer.

phantom driver and wire-fault detection

The phantom-drive circuit under control of $\overline{\text{NSRT}}$ generates a dc voltage on both of the phantom-drive outputs, PHOUTA and PHOUTB. In order to maintain the phantom drive, $\overline{\text{NSRT}}$ is toggled by the TI380C30 at least once every 20 ms. A watchdog timer is included in the TI380C30 to remove the phantom drive if $\overline{\text{NSRT}}$ does not have the required transitions.

The watchdog timer is normally not allowed to expire because it is being reinitialized at least every 20 ms. If there is a problem in the TI380C30 or its microcode resulting in failure to toggle $\overline{\text{NSRT}}$, the timer expires in a maximum of 22 ms. If this happens, the phantom drive is deasserted and remains so until the next falling edge of $\overline{\text{NSRT}}$. The watchdog timer requires no external-timing components. When the phantom drive is deasserted, the phantom-drive lines are actively pulled low, reaching a level of 1 V or less within 50 ms.

phantom driver and wire-fault detection (continued)

The dc voltage from PHOUTA and PHOUTB is superimposed on the transmit-signal pair to the trunk-coupling unit (TCU) to request that the station be inserted into the ring. This is achieved by connecting the transmit-signal pair to the center of the secondary winding of the transmit-isolation transformer. Since PHOUTA and PHOUTB are connected to the media side of the isolation transformer, they require extensive protection against line surges. A capacitor is connected between the two phantom lines to provide an ac path for the transmit signal, while PHOUTA and PHOUTB independently drive the dc voltage on each of the transmit lines allowing for independent wire-fault detection on each.

The phantom voltage is detected by the TCU, causing the external wrap path from the transmitter outputs back to the receiver inputs to be broken and the ring to be broken. A signal connection is established from the ring to the receiver inputs and from the transmitter outputs to the ring. The return current from the dc-phantom voltage on the transmit pair is returned to the station via the receive pair. This provides some measure of wire-fault detection on the receive lines. The phantom-drive outputs are current limited to prevent damage if short circuited. They detect either an abnormally high or an abnormally low load current at either output corresponding to a short or an open circuit in the ring or TCU wiring. Either type of fault results in the wire-fault indicator output ($\overline{\text{WFLT}}$) to be driven low. The logic state of $\overline{\text{WFLT}}$ is high when the phantom drive is not active.

frequency acquisition and $\overline{\text{REDY}}$

Unlike its predecessors, the TMS3805x family, the data-recovery PLL of the TI380C30 does not require constant frequency monitoring; neither is it necessary to recenter its frequency via the FRAQ control line. When the TI380C30 PH asserts FRAQ, it initiates a reset of the clock-recovery PLL. The $\overline{\text{REDY}}$ signal is deasserted for the duration of this action and reasserted low when it is complete (a maximum of 3 µs later). This low-going transition of $\overline{\text{REDY}}$ is required by the TI380C30 following the setting of FRAQ high to indicate to the PH that any frequency error that it could have detected has been corrected.

power-down control

The TI380C30 physical-layer interface can be disabled by the $\overline{\text{PWRDN}}$ signal. If $\overline{\text{PWRDN}}$ is taken low, all outputs of the physical-layer interface are in the high-impedance state and all internal logic is powered down, bringing power consumption to a very low level. Upon removing $\overline{\text{PWRDN}}$, the device resets and initializes itself. This process could take up to 2 ms and care should be taken to ensure that the system does not require stable clocks during this period.

user-accessible hardware registers and TI380C30-internal pointers

The following tables show how to access internal data via pointers and how to address the registers in the host interface. The SIFACL register, which directly controls device operation, is described in detail. The adapter-internal pointers table on the following page is defined only after TI380C30 initialization and until the OPEN command is issued. These pointers are defined by the TI380C30 software (microcode), and this table describes the release 2.x software.

Adapter-Internal Pointers for Token Ring†

ADDRESS	DESCRIPTION
>00.FFF8‡	Pointer to software raw microcode level in chapter 0
>00.FFFA‡	Pointer to starting location of copyright notices. Copyright notices are separated by a >0A character and terminated by a >00 character in chapter 0.
>01.0A00	Pointer to burned-in address in chapter 1
>01.0A02	Pointer to software level in chapter 1
>01.0A04	Pointer to TI380C30 addresses in chapter 1: Pointer + 0 node address Pointer + 6 group address Pointer + 10 functional address
>01.0A06	Pointer to TI380C30 parameters in chapter 1: Pointer + 0 physical-drop number Pointer + 4 upstream neighbor address Pointer + 10 upstream physical-drop number Pointer + 14 last ring-poll address Pointer + 20 reserved Pointer + 22 transmit access priority Pointer + 24 source class authorization Pointer + 26 last attention code Pointer + 28 source address of the last received frame Pointer + 34 last beacon type Pointer + 36 last major vector Pointer + 38 ring status Pointer + 40 soft-error timer value Pointer + 42 ring-interface error counter Pointer + 44 local ring number Pointer + 46 monitor error code Pointer + 48 last beacon-transmit type Pointer + 50 last beacon-receive type Pointer + 52 last MAC-frame correlator Pointer + 54 last beaconing-station UNA Pointer + 60 reserved Pointer + 64 last beaconing-station physical-drop number
>01.0A08	Pointer to MAC buffer (a special buffer used by the software to transmit adapter-generated MAC frames) in chapter 1
>01.0A0A	Pointer to LLC counters in chapter 1: Pointer + 0 MAX_SAPs Pointer + 1 open SAPs Pointer + 2 MAX_STATIONs Pointer + 3 open stations Pointer + 4 available stations Pointer + 5 reserved
>01.0A0C	Pointer to 4-/16-Mbps word flag. If zero, the adapter is set to run at 4 Mbps. If nonzero, the adapter is set to run at 16 Mbps.
>01.0A0E	Pointer to total TI380C30 RAM found in 1K bytes in RAM allocation test in chapter 1.

† This table describes the pointers for release 2.x of the TI380C30 software.
‡ This address valid only for microcode release 2.x

User-Access Hardware Registers

80x8x 16-BIT MODE: (SI/$\overline{M}$ = 1, S8/$\overline{SHALT}$ = 0)†

WORD TRANSFERS			NORMAL MODE $\overline{SBHE}$ = 0 SRS2 = 0		PSEUDO-DMA MODE ACTIVE $\overline{SBHE}$ = 0 SRS2 = 0	
BYTE TRANSFERS			$\overline{SBHE}$ = 0 SRS2 = 1	$\overline{SBHE}$ = 1 SRS2 = 0	$\overline{SBHE}$ = 0 SRS2 = 1	$\overline{SBHE}$ = 1 SRS2 = 0
SRSX	SRS0	SRS1				
0	0	0	SIFDAT MSB	SIFDAT LSB	SDMADAT MSB	SDMADAT LSB
0	0	1	SIFDAT/INC MSB	SIFDAT/INC LSB	DMALEN MSB	DMALEN LSB
0	1	0	SIFADR MSB	SIFADR LSB	SDMAADR MSB	SDMAADR LSB
0	1	1	SIFCMD	SIFSTS	SDMAADX MSB	SDMAADX LSB
1	0	0	SIFACL MSB	SIFACL LSB	SIFACL MSB	SIFACL LSB
1	0	1	SIFADR MSB	SIFADR LSB	SIFADR MSB	SIFADR LSB
1	1	0	SIFADX MSB	SIFADX LSB	SIFADX MSB	SIFADX LSB
1	1	1	DMALEN MSB	DMALEN LSB	DMALEN MSB	DMALEN LSB

† $\overline{SBHE}$ = 1 and SRS2 = 1 are not defined

80x8x 8-BIT MODE: (SI/$\overline{M}$ = 1, S8/$\overline{SHALT}$ = 1)

SRSX	SRS0	SRS1	SRS2	NORMAL MODE $\overline{SBHE}$ = X	PSEUDO-DMA MODE ACTIVE $\overline{SBHE}$ = X
0	0	0	0	SIFDAT LSB	SDMADAT LSB
0	0	0	1	SIFDAT MSB	SDMADAT MSB
0	0	1	0	SIFDAT/INC LSB	DMALEN LSB
0	0	1	1	SIFDAT/INC MSB	DMALEN MSB
0	1	0	0	SIFADR LSB	SDMAADR LSB
0	1	0	1	SIFADR MSB	SDMAADR MSB
0	1	1	0	SIFSTS	SDMAADX LSB
0	1	1	1	SIFCMD	SDMAADX MSB
1	0	0	0	SIFACL LSB	SIFACL LSB
1	0	0	1	SIFACL MSB	SIFACL MSB
1	0	1	0	SIFADR LSB	SIFADR LSB
1	0	1	1	SIFADR MSB	SIFADR MSB
1	1	0	0	SIFADX LSB	SIFADX LSB
1	1	0	1	SIFADX MSB	SIFADX MSB
1	1	1	0	DMALEN LSB	DMALEN LSB
1	1	1	1	DMALEN MSB	DMALEN MSB

68xxx MODE: (SI/$\overline{M}$ = 0)‡

WORD TRANSFERS			NORMAL MODE $\overline{SUDS}$ = 0 $\overline{SLDS}$ = 0		PSEUDO-DMA MODE ACTIVE $\overline{SUDS}$ = 0 $\overline{SLDS}$ = 0	
BYTE TRANSFERS			$\overline{SUDS}$ = 0 $\overline{SLDS}$ = 1	$\overline{SUDS}$ = 1 $\overline{SLDS}$ = 0	$\overline{SUDS}$ = 0 $\overline{SLDS}$ = 1	$\overline{SUDS}$ = 1 $\overline{SLDS}$ = 0
SRSX	SRS0	SRS1				
0	0	0	SIFDAT MSB	SIFDAT LSB	SDMADAT MSB	SDMADAT LSB
0	0	1	SIFDAT/INC MSB	SIFDAT/INC LSB	DMALEN MSB	DMALEN LSB
0	1	0	SIFADR MSB	SIFADR LSB	SDMAADR MSB	SDMAADR LSB
0	1	1	SIFCMD	SIFSTS	SDMAADX MSB	SDMAADX LSB
1	0	0	SIFACL MSB	SIFACL LSB	SIFACL MSB	SIFACL LSB
1	0	1	SIFADR MSB	SIFADR LSB	SIFADR MSB	SIFADR LSB
1	1	0	SIFADX MSB	SIFADX LSB	SIFADX MSB	SIFADX LSB
1	1	1	DMALEN MSB	DMALEN LSB	DMALEN MSB	DMALEN LSB

‡ 68xxx mode is always 16 bit.

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SIF adapter-control register (SIFACL)

The SIFACL register allows the host processor to control and to some extent reconfigure the TI380C30 under software control.

SIFACL Register

Bit #	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	TEST0	TEST1	TEST2	—	SWHLDA	SWDDIR	SWHRQ	PSDMAEN	ARESET	CPHALT	BOOT	LBP	SINTEN	PEN	NSEL OUT0	NSEL OUT1
	R	R	R		RP–0	R–u	R–0	RS–0	RW–0	RP–b	RP–b	RW –0	RW–1	RP–p	RP–0	RP–1

Legend:
R = Read
W = Write
P = Write during ARESET = 1 only
S = Set only
–n = Value after reset
b = Value on BTSTRP
p = Value on PRTYEN
u = Indeterminate

Bits 0–2: Value on TEST0 and TEST2 pins

Read only and always reflects the value on the corresponding device pins. This allows the host S/W to determine speed configuration. If the network speed and type are software configurable, these bits can be used to determine which configurations are supported by the network hardware.

TEST0	TEST1	TEST2	Description
L	NC	H	16-Mbps token ring
H	NC	H	4-Mbps token ring
X	X	L	Reserved

Bit 3: **Reserved.** Read data is indeterminate.

Bit 4: SWHLDA — Software-Hold Acknowledge

Allows the function of SHLDA / $\overline{\text{SBGR}}$ to be emulated from software control for pseudo-DMA mode.

PSDMAEN	SWHLDA	SWHRQ	RESULT
0†	X	X	SWHLDA value in the SIFACL register cannot be set to a one.
1†	0	0	No pseudo-DMA request pending
1†	0	1	Indicates a pseudo-DMA request interrupt
1†	1	X	Pseudo-DMA process in progress

† The value on SHLDA / $\overline{\text{SBGR}}$ is ignored.

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Bit 5: **SWDDIR — Current SDDIR-Signal Value**

Contains the current value of the pseudo-DMA direction. This enables the host to easily determine the direction of DMA transfers, which allows system DMA to be controlled by system software.

0 = Pseudo DMA from host system to TI380C30
1 = Pseudo DMA from TI380C30 to host system

Bit 6: **SWHRQ — Current SHRQ-Signal Value**

Contains the current value on SHRQ/$\overline{\text{SBRQ}}$ when in Intel mode and the inverse of the value on SHRQ/$\overline{\text{SBRQ}}$ in Motorola mode. This enables the host to easily determine if a pseudo-DMA transfer is requested.

	INTEL MODE (SI/$\overline{\text{M}}$ = H)	MOTOROLA MODE (SI/$\overline{\text{M}}$ = L)
0 =	System bus not requested	System bus not requested
1 =	System bus requested	System bus requested

Bit 7: **PSDMAEN — Pseudo-System-DMA Enable**

Enables pseudo-DMA operation

0 = Normal bus-master DMA operation is possible.
1 = Pseudo-DMA operation selected. Operation dependent on the values of the SWHLDA and SWHRQ bits in the SIFACL register.

Bit 8: **ARESET — Adapter Reset**

Is a hardware reset of the TI380C30. This bit has the same effect as $\overline{\text{SRESET}}$ except that the DIO interface to the SIFACL register is maintained. This bit is set to 1 if a clock failure is detected (OSCIN, PXTALIN, RCLK, or SBCLK not valid).

0 = The TI380C30 operates normally.
1 = The TI380C30 is held in the reset condition.

Bit 9: **CPHALT — Communications-Processor Halt**

Controls the TI380C30 processor access to the internal TI380C30 buses. This prevents the TI380C30 from executing instructions before the microcode has been downloaded.

0 = The TI380C30 processor can access the internal TI380C30 buses.
1 = The TI380C30 processor is prevented from accessing the internal-adapter buses.

Bit 10: **BOOT — Bootstrap CP Code**

Indicates whether the memory in chapters 0 and 31 of the local-memory space is RAM or ROM/PROM/EPROM. This bit controls the operation of $\overline{\text{MCAS}}$ and $\overline{\text{MROMEN}}$.

0 = ROM/PROM/EPROM memory in chapters 0 and 31
1 = RAM memory in chapters 0 and 31

Bit 11: **LBP — Local-Bus Priority**

Controls the priority levels of devices on the local bus

0 = No external devices (such as TI380FPA) are used with the TI380C30.
1 = An external device (such as TI380FPA) is used with the TI380C30. This allows external bus master to operate at the necessary priority on the local bus

If the system uses the TMS380SRA only, the bit must be set to 0. If the system uses both the TMS380SRA and the TI380FPA, the bit must be set to 1.

Bit 12: **SINTEN — System-Interrupt Enable**

Allows the host processor to enable or disable system-interrupt requests from the TI380C30. The system-interrupt request from the TI380C30 is on SINTR/$\overline{\text{SIRQ}}$. The following equation shows how SINTR/$\overline{\text{SIRQ}}$ is driven. The table also explains the results of the states.

SINTR/$\overline{\text{SIRQ}}$ = (PSDMAEN * SWHRQ * !SWHLDA) + (SINTEN * SYSTEM_INTERRUPT)

PSDMAEN	SWHRQ	SWHLDA	SINTEN	SYSTEM INTERRUPT (SIFSTS REGISTER)	RESULT
1†	1	1	X	X	Pseudo DMA is active.
1†	1	0	X	X	The TI380C30 generated a system interrupt for a pseudo DMA.
1†	0	0	X	X	Not a pseudo-DMA interrupt
X	X	X	1	1	The TI380C30 generates a system interrupt.
0	X	X	1	0	The TI380C30 does not generate a system interrupt.
0	X	X	0	X	The TI380C30 cannot generate a system interrupt.

† The value on SHLDA / $\overline{\text{SBGR}}$ is ignored.

Bit 13: **PEN — Parity Enable**

Determines whether data transfers within the TI380C30 are checked for parity.

0 = Data transfers are not checked for parity.
1 = Data transfers are checked for correct odd parity.

Bit 14 – 15: **NSELOUT0, NSELOUT0 1 — Network-Selection Outputs**

Values control NSELOUT0 and NSELOUT1. These bits can be modified only while the ARESET bit is set.

These bits can be used to software configure a TI380C30: NSELOUT0 should be connected to TEST0 (TEST1 should be left unconnected and TEST2 should be tied high). NSELOUT0 and NSELOUT1 are used to select network speed as shown in the table below:

NSELOUT0	NSELOUT1	SELECTION
0	0	Reserved
0	1	16-Mbps token ring
1	0	Reserved
1	1	4-Mbps token ring

At power up, these bits are set corresponding to 16-Mbps token ring (NSELOUT1 = 1, NSELOUT0 = 0).

SIFACL control for pseudo-DMA operation

Pseudo DMA operation is software controlled by using five bits in the SIFACL register. The logic model for the SIFACL-register control of pseudo-DMA operation is shown in Figure 2.

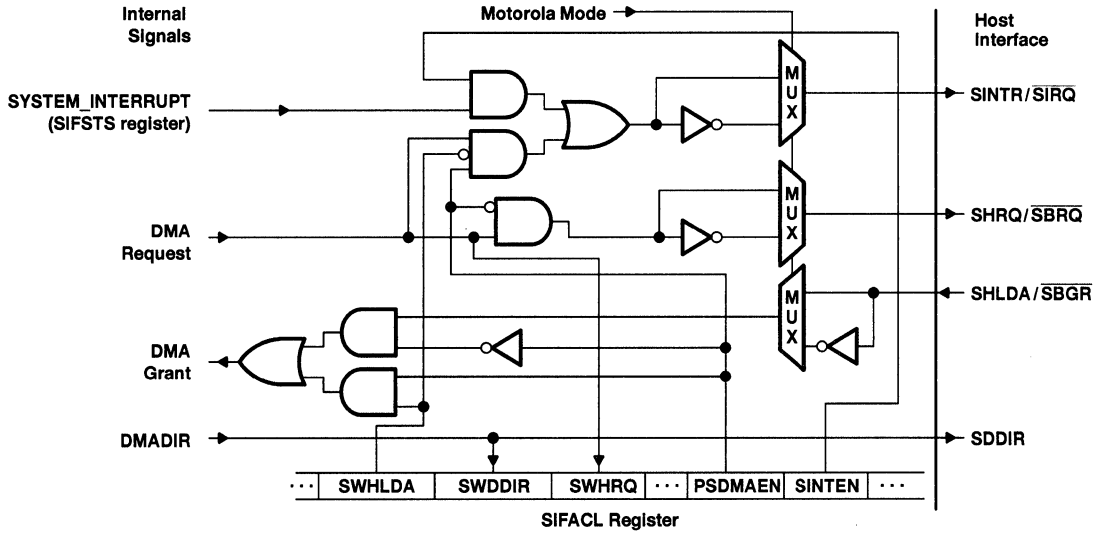

Figure 5. Pseudo-DMA Logic Related to SIFACL Bits

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 8) ..... – 0.5 V to 7 V
Input voltage range (see Note 8) ..... – 0.5 V to 7 V
Output voltage range ..... – 0.5 V to 7 V
Power dissipation ..... 1.25 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 8: Voltage values are with respect to V_{SS}, and all V_{SS} pins should be routed so as to minimize inductance to system ground.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	TTL-level signal	2		V_{DD}+0.3	V
		OSCIN	2.4		V_{DD}+0.3	
		RCLK, PXTALIN, RCVR	2.6		V_{DD}+0.3	
V_{IL}	Low-level input voltage, TTL-level signal (see Note 9)		–0.3		0.8	V
I_{OH}	High-level output current	TTL outputs			–400	µA
I_{OL}	High-level output current (see Note 10)	TTL outputs			2	mA
T_A	Operating free-air temperature		0		70	°C
T_C	Operating case temperature				85	°C

NOTES: 9. The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used for logic-voltage levels only.
10. Output current of 2 mA is sufficient to drive five low-power Schottky TTL loads or ten advanced low-power Schottky TTL loads (worst case).

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS‡		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, TTL-level signal (see Note 11)		V_{DD} = MIN,	I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage, TTL-level signal		V_{DD} = MIN,	I_{OL} = MAX			0.6	V
I_O	High-impedance output current		V_{DD} = MAX,	V_O = 2.4 V			20	µA
			V_{DD} = MAX,	V_O = 0.4 V			–20	
I_I	Input current, any input or input/output		V_I = V_{SS} to V_{DD}				±20	µA
I_{CC}	Supply current	Normal mode	V_{DD} = MAX				160	mA
		Power-down mode	V_{DD} = 5 V			5		
C_i	Input capacitance, any input		f = 1 MHz,	Others at 0 V			15	pF
C_o	Output capacitance, any output or input/output		f = 1 MHz,	Others at 0 V			15	pF

‡ For conditions shown as MIN/MAX, use the appropriate value specified under the recommended operating conditions.

NOTE 11: The following signals require an external pullup resistor: SRAS/$\overline{\text{SAS}}$, $\overline{\text{SRDY}}$/$\overline{\text{SDTACK}}$, $\overline{\text{SRD}}$/$\overline{\text{SUDS}}$, $\overline{\text{SWR}}$/$\overline{\text{SLDS}}$, $\overline{\text{EXTINT0}}$–$\overline{\text{EXTINT3}}$, and $\overline{\text{MBRQ}}$.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

receiver input (RCV+ and RCV–)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_B	Receiver-input bias voltage	See Note 12	$V_{SB}-1$	$V_{SB}+1$	V
V_{T+}	Rising-input threshold voltage	$V_{ICM} = V_{SB}$, $R_{tst} = 330\ \Omega$, See Notes 12, 13, and Figure 6		20	mV
V_{T-}	Falling-input threshold voltage	$V_{ICM} = V_{SB}$, $R_{tst} = 330\ \Omega$, See Notes 12, 13, and Figure 6	–20		mV
V_{AT}	Asymmetry threshold voltage, (V_{T+} + V_{T-})	$V_{ICM} = V_{SB}$, $R_{tst} = 330\ \Omega$, See Notes 12, 13, and Figure 6	–10	10	mV
$V_{r(CM)}$	Rising-input common-mode rejection [V_{T+} (@V_{SB} + 0.5 V) – V_{T+} (@V_{SB} – 0.5 V)]	See Notes 12, 13, and Figure 6	–15	15	mV
$V_{f(CM)}$	Falling-input common-mode rejection [V_{T+} (@V_{SB} + 0.5 V) – V_{T+} (@V_{SB} – 0.5 V)]	See Notes 12, 13, and Figure 6	–15	15	mV
$I_{I(RCVR)}$	Receiver input current	Both inputs at V_{SB}, See Note 12 and Figure 6	–25	25	µA
		Input under test at V_{SB} + 1 V, Other input at V_{SB} – 1 V, See Notes 12 and 13 and Figure 6	300	700	
		$R_{tst} = 330\ \Omega$, Input under test at V_{SB} – 1 V, Other input at V_{SB} + 1 V, See Note 12	–300	–700	
I_{EQB}	Equalizer bias current	EQ+ and EQ– biased at V_{DD} – 3 V RCV+ and RCV– at V_{DD} – 3 V, See Figure 6	1.3	1.7	mA
V_{EQW}	Equalizer wrap voltage	$\overline{WRAP}$ = low, See Figure 6	130	0	mV

NOTES: 12. V_{SB} is the self-bias voltage of the input pair RCV+ and RCV–. It is defined as $V_{SB} = (V_{SB+} + V_{SB-}) \div 2$ (where V_{SB+} is the self-bias voltage of RCV+; V_{SB-} is the self-bias voltage of RCV–). The self-bias voltage of both pins is approximately $V_{DD} \div 2$.
13. V_{ICM} is the common-mode voltage applied to RCV+ and RCV–.

phantom driver (PHOUTA and PHOUTB)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -1$ mA	4.1		V
		$I_{OH} = -2$ mA	3.8		V
I_{OS}	Short-circuit output current	$V_O = 0$ V	–4	–20	mA
I_{OL}	Low-level output current	$V_O = V_{DD}$	–1	–10	mA
I_{OZH}	Off-state output current with high-level voltage applied	$V_O = V_{DD}$	–100	100	µA
I_{OZL}	Off-state output current with low-level voltage applied	$V_O = 0$ V	–100	100	µA

wire fault ($\overline{WFLT}$) (see Notes 14 and 15)

PARAMETER		MIN	MAX	UNIT
R_{LS}	Phantom load resistance detected as short circuit		0.15	kΩ
R_{LO}	Phantom load resistance detected as open circuit	50		kΩ
R_{LN}	Phantom load resistance dectected as normal	2.9	5.5	kΩ

NOTES: 14. The wire-fault circuit recognizes a fault condition for any phantom-drive load resistance to ground of greater than R_{LO} or any load resistance less than R_{LS}. Any resistance in the range specified for R_{LN} is not recognized as a wire fault. A fault condition on either PHOUTA or PHOUTB results in the $\overline{WFLT}$ signal being asserted (low).
15. Resistor (R_{LS}, R_{LO}, R_{LN}) connected from output under test to ground, other output loaded with 4.1 Ω to ground.

ADVANCE INFORMATION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PLL characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{FILT}	Reference PLL operating filter voltage	$t_{c(XT1)}$ = 125 ns	1.8	3.8	V

crystal-oscillator characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{SB(XT1)}$	Input self-bias voltage		1.8	3.8	V
$I_{OH(XT2)}$	Output high-level current	$V_{(XT2)} = V_{SB(XT1)}$ $V_{(XT1)} = V_{SB(XT1)} + 0.5$ V	– 3.5	– 6.5	mA
$I_{OL(XT2)}$	Output low-level current	$V_{(XT2)} = V_{SB(XT1)}$ $V_{(XT1)} = V_{SB(XT1)} - 0.5$ V	0.7	1.3	mA

timing parameters

The timing parameters for the signals of TI380C30 are shown in the following tables and are illustrated in the accompanying figures. The purpose of these figures and tables is to quantify the timing relationships among the various signals. The parameters are numbered for convenience.

static signals

The following table lists signals that are not allowed to change dynamically and therefore have no timing associated with them. They should be strapped high, low, or left unconnected as required.

SIGNAL	FUNCTION
SI/$\overline{M}$	Host-processor select (Intel/Motorola)
CLKDIV	Reserved
BTSTRP	Default-bootstrap mode (RAM/ROM)
PRTYEN	Default-parity select (enabled/disabled)
TEST0	Test pin indicates network type
TEST1	NC
TEST2	Test pin indicates network type
TEST3	Test pin for TI manufacturing test †
TEST4	Test pin for TI manufacturing test †
TEST5	Test pin for TI manufacturing test †

† For unit-in-place test

ADVANCE INFORMATION

timing parameter symbology

Some timing parameter symbols have been created in accordance with JEDEC Standard 100-A. In order to shorten the symbols, some of the signal names and other related terminology have been abbreviated as shown below:

DR	DRVR	RS	$\overline{\text{SRESET}}$
DRN	$\overline{\text{DRVR}}$	VDD	V_{DDL}, V_{DD}
OSC	OSCIN		
SCK	SBCLK		

Lower-case subscripts are defined as follows:

c	cycle time	r	rise time
d	delay time	sk	skew
h	hold time	su	setup time
w	pulse duration (width)	t	transition time

The following additional letters and phrases are defined as follows:

H	High	Z	High impedance
L	Low	Falling edge	No longer high
V	Valid	Rising edge	No longer low

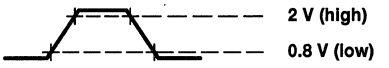
ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

Outputs are driven to a minimum high-logic level of 2.4 V and to a maximum low-logic level of 0.6 V. These levels are compatible with TTL devices.

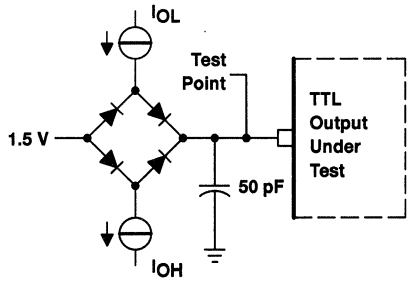
Output transition times are specified as follows: For a high-to-low transition on either an input or output signal, the level at which the signal is said to be no longer high is 2 V and the level at which the signal is said to be low is 0.8 V. For a low-to-high transition, the level at which the signal is said to be no longer low is 0.8 V and the level at which the signal is said to be high is 2 V, as shown below.

The rise and fall times are not specified but are assumed to be those of standard TTL devices, which are typically 1.5 ns.

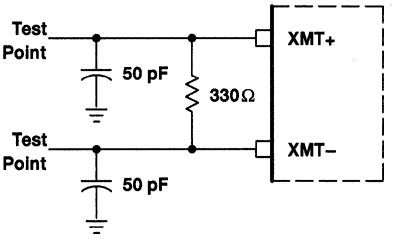


test measurement

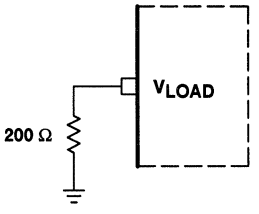
The test-load circuit shown in Figure 6 represents the programmable load of the tester pin electronics that are used to verify timing parameters of TI380C30 output signals.



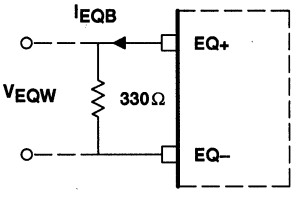
(a) TTL-OUTPUT TEST LOAD



(b) XMT+ and XMT– TEST LOAD



(c) I_{ref} TEST CIRCUIT



(d) EQUALIZER TEST CIRCUIT

Where: I_{OL} = 2 mA, dc-level verification (all outputs)
I_{OH} = 400 μA (all outputs)
V_{LOAD} = 1.5 V, typical dc-level verification or 0.7 V, typical timing verification
C_T = 65 pF, typical load-circuit capacitance

Figure 6. Test and Load Circuits

power up, SBCLK, OSCIN, MBCLK1, MBCLK2, $\overline{\text{SYNCIN}}$, and $\overline{\text{SRESET}}$ timing

NO.				MIN	NOM	MAX	UNIT
100†	$t_{r(VDD)}$	Rise time, 1.2 V to minimum V_{DD}-high level				1	ms
101†‡	$t_{d(VDDH-SCKV)}$	Delay time, minimum V_{DD}-high level to first valid SBCLK no longer high				1	ms
102†‡	$t_{d(VDDH-OSCV)}$	Delay time, minimum V_{DD}-high level to first valid OSCIN high				1	ms
103	$t_{c(SCK)}$	Cycle time, SBCLK (see Note 16)		30.3		500	ns
104	$t_{w(SCKH)}$	Pulse duration, SBCLK high		13		500	ns
105	$t_{w(SCKL)}$	Pulse duration, SBCLK low		13		500	ns
106†	$t_{t(SCK)}$	Transition time, SBCLK				2	ns
107	$t_{c(OSC)}$	Cycle time, OSCIN (see Note 17)			1/OSCIN		ns
108	$t_{w(OSCH)}$	Pulse duration, OSCIN high (see Note 18)	OSCIN = 64 MHz	5.5			ns
			OSCIN = 48 MHz	8			
			OSCIN = 32 MHz	8			
109	$t_{w(OSCL)}$	Pulse duration, OSCIN low (see Note 18)	OSCIN = 64 MHz	5.5			ns
			OSCIN = 48 MHz	8			
			OSCIN = 32 MHz	8			
110†	$t_{t(OSC)}$	Transition time, OSCIN				3	ns
111†	$t_{d(OSCV-CKV)}$	Delay time, OSCIN valid to MBCLK1 and MBCLK2 valid				1	ms
117†	$t_{h(VDDH-RSL)}$	Hold time, $\overline{\text{SRESET}}$ low after V_{DD} reaches minimum high level		5			ms
118†	$t_{w(RSH)}$	Pulse duration, $\overline{\text{SRESET}}$ high		14			µs
119†	$t_{w(RSL)}$	Pulse duration, $\overline{\text{SRESET}}$ low		14			µs
288†	$t_{su(RST)}$	Setup time, DMA size to $\overline{\text{SRESET}}$ high (Intel mode only)		10			ns
289†	$t_{h(RST)}$	Hold time, DMA size from $\overline{\text{SRESET}}$ high (Intel mode only)		10			ns
	t_M	One-eighth of a local-memory cycle	CLKDIV = H	$2t_{c(OSC)}$			ns
			CLKDIV = L	$2t_{c(OSC)}$			

† This specification is provided as an aid to board design. It is not assured during manufacturing testing.

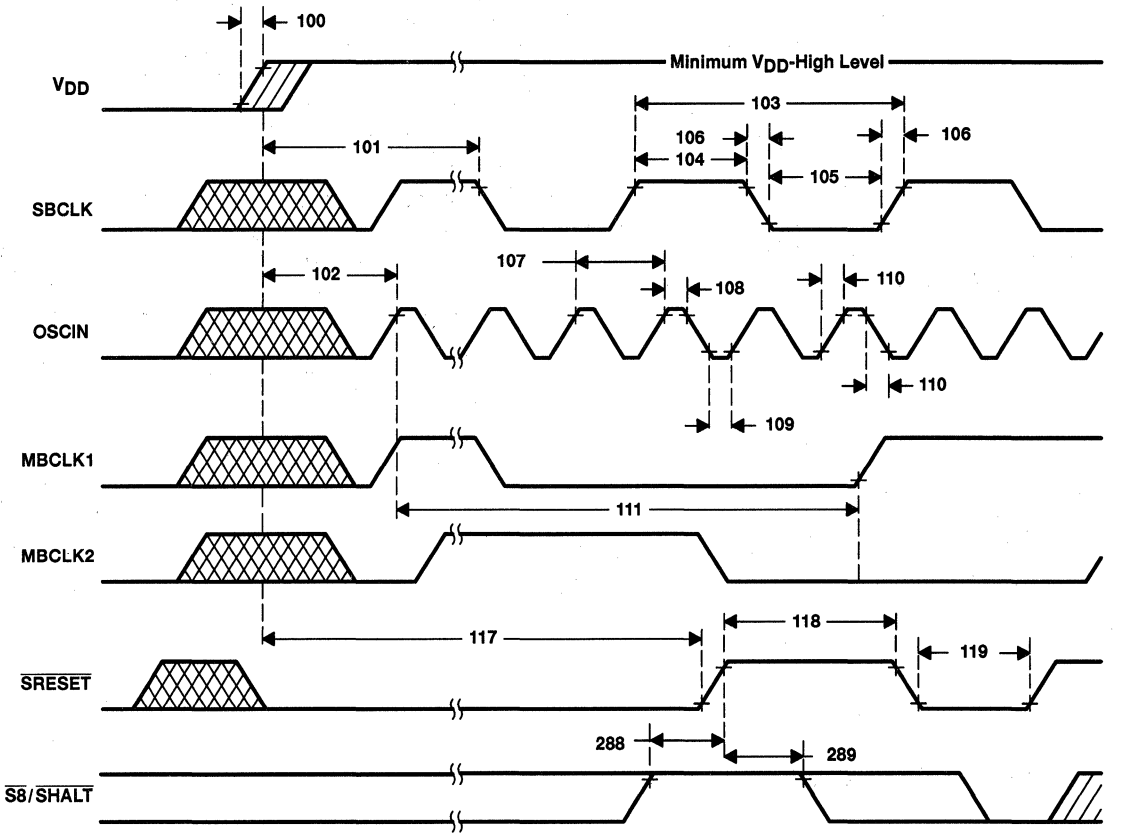
‡ If parameter 101 or 102 cannot be met, parameter 117 must be extended by the larger difference: real value of parameter 101 or 102 minus the max value listed.

NOTES: 16. SBCLK can be any value between 2 MHz and 33 MHz. This data sheet describes the system interface (SIF) timing parameters for the cases of SBCLK at 25 MHz and 33 MHz.

17. The value of OSCIN can be 64 MHz ±1%, 32 MHz ± 1%, or 48 MHz ± 1%. If OSCIN is used to generate PXTALIN, the OSCIN tolerance must be ±0.01%.

18. This is to assure a ± 5% duty-cycle crystal, provided that OSCIN meets the recommended operating conditions for V_{IH} and V_{IL}.

ADVANCE INFORMATION



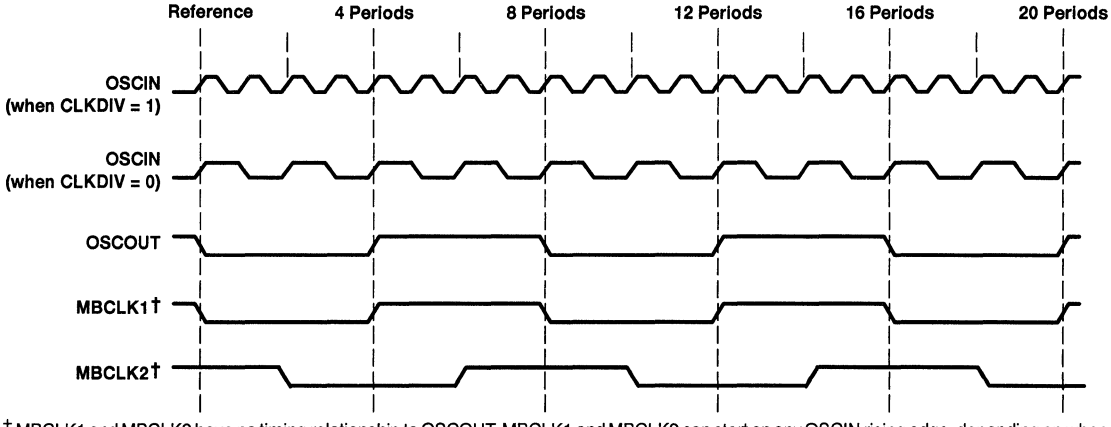
NOTE A: To represent the information in one illustration, nonactual phase and timebase characteristics are shown. Refer to specified parameters for precise information.

Figure 7. Timing for Power Up, System Clocks, $\overline{\text{SYNCIN}}$, and $\overline{\text{SRESET}}$

memory-bus timing: local-memory clocks, $\overline{\text{MAL}}$, $\overline{\text{MROMEN}}$, $\overline{\text{MBIAEN}}$, $\overline{\text{NMI}}$, $\overline{\text{MRESET}}$, and ADDRESS

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

NO.		MIN	MAX	UNIT
1	Period of MBCLK1 and MBCLK2	$4t_M$		ns
2	Pulse duration, clock high	$2t_M-9$		ns
3	Pulse duration, clock low	$2t_M-9$		ns
4	Hold time, MBCLK2 low after MBCLK1 high	t_M-9		ns
5	Hold time, MBCLK1 high after MBCLK2 high	t_M-9		ns
6	Hold time, MBCLK2 high after MBCLK1 low	t_M-9		ns
7	Hold time, MBCLK1 low after MBCLK2 low	t_M-9		ns
8	Setup time, address/enable on MAX0, MAX2, and $\overline{\text{MROMEN}}$ before MBCLK1 no longer high	t_M-9		ns
9	Setup time, row address on MADL0–MADL7, MAXPH, and MAXPL before MBCLK1 no longer high	t_M-14		ns
10	Setup time, address on MADH0–MADH7 before MBCLK1 no longer high	t_M-14		ns
11	Setup time, $\overline{\text{MAL}}$ high before MBCLK1 no longer high	13		ns
12	Setup time, address on MAX0, MAX2, and $\overline{\text{MROMEN}}$ before MBCLK1 no longer low	$0.5t_M-9$		ns
13	Setup time, column address on MADL0–MADL7, MAXPH, and MAXPL before MBCLK1 no longer low	$0.5t_M-9$		ns
14	Setup time, status on MADH0–MADH7 before MBCLK1 no longer low	$0.5t_M-9$		ns
120	Setup time, $\overline{\text{NMI}}$ valid before MBCLK1 low	30		ns
121	Hold time, $\overline{\text{NMI}}$ valid after MBCLK1 low	0		ns
126	Delay time, MBCLK1 no longer low to $\overline{\text{MRESET}}$ valid	0	20	ns
129	Hold time, column address/status after MBCLK1 no longer low	t_M-7		ns



† MBCLK1 and MBCLK2 have no timing relationship to OSCOUT. MBCLK1 and MBCLK2 can start on any OSCIN rising edge, depending on when the memory cycle starts execution.

Figure 8. Clock Waveforms After Clock Stabilization

ADVANCE INFORMATION

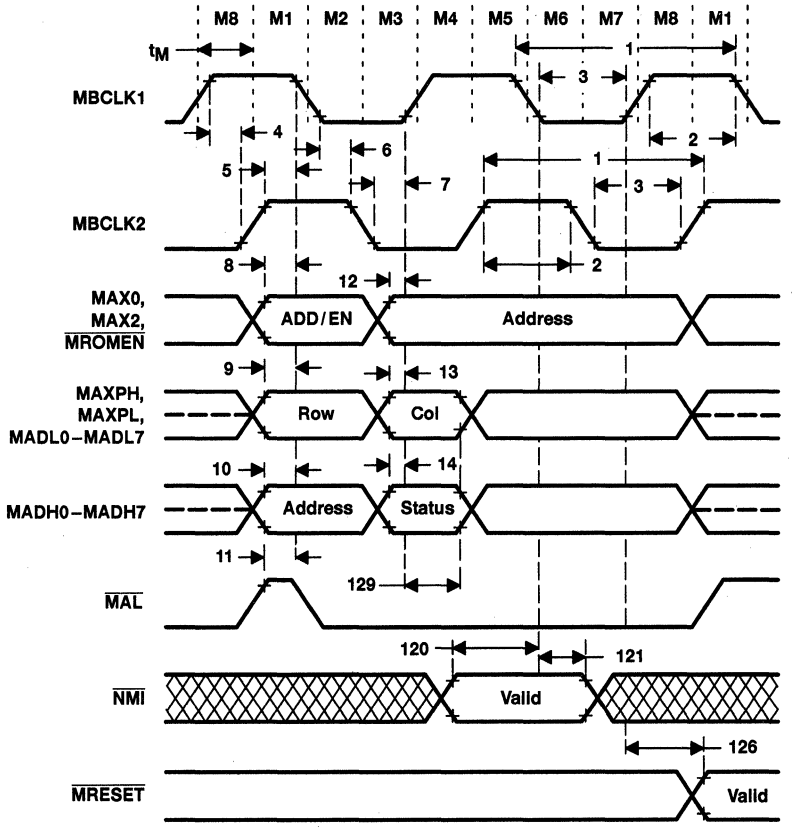


Figure 9. Memory-Bus Timing: Local-Memory Clocks, MAL, MROMEN, MBIAEN, NMI, MRESET, and ADDRESS

memory-bus timing: clocks, $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, and $\overline{\text{MAL}}$ to ADDRESS

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

NO.		MIN MAX	UNIT
15	Setup time, row address on MADL0–MADL7, MAXPH, and MAXPL before $\overline{\text{MRAS}}$ no longer high	$1.5t_M - 11.5$	ns
16	Hold time, row address on MADL0–MADL7, MAXPH, and MAXPL after $\overline{\text{MRAS}}$ no longer high	$t_M - 6.5$	ns
17	Delay time, $\overline{\text{MRAS}}$ no longer high to $\overline{\text{MRAS}}$ no longer high in the next memory cycle	$8t_M$	ns
18	Pulse duration, $\overline{\text{MRAS}}$ low	$4.5t_M - 5$	ns
19	Pulse duration, $\overline{\text{MRAS}}$ high	$3.5t_M - 5$	ns
20	Setup time, column address (MADL0–MADL7, MAXPH, and MAXPL) and status (MADH0–MADH7) before $\overline{\text{MCAS}}$ no longer high	$0.5t_M - 9$	ns
21	Hold time, column address (MADL0–MADL7, MAXPH, and MAXPL) and status (MADH0–MADH7) after $\overline{\text{MCAS}}$ low	$t_M - 5$	ns
22	Hold time, column address (MADL0–MADL7, MAXPH, and MAXPL) and status (MADH0–MADH7) after $\overline{\text{MRAS}}$ no longer high	$2.5t_M - 6.5$	ns
23	Pulse duration, $\overline{\text{MCAS}}$ low	$3t_M - 9$	ns
24	Pulse duration, $\overline{\text{MCAS}}$ high, refresh cycle follows read or write cycle	$2t_M - 9$	ns
25	Hold time, row address on MAXL0–MAXL7, MAXPH, and MAXPL after $\overline{\text{MAL}}$ low	$1.5t_M - 9$	ns
26	Setup time, row address on MAXL0–MAXL7, MAXPH, and MAXPL before $\overline{\text{MAL}}$ no longer high	$t_M - 9$	ns
27	Pulse duration, $\overline{\text{MAL}}$ high	$t_M - 9$	ns
28	Setup time, address/enable on MAX0, MAX2, and $\overline{\text{MROMEN}}$ before $\overline{\text{MAL}}$ no longer high	$t_M - 9$	ns
29	Hold time, address/enable of MAX0, MAX2, and $\overline{\text{MROMEN}}$ after $\overline{\text{MAL}}$ low	$1.5t_M - 9$	ns
30	Setup time, address on MADH0–MADH7 before $\overline{\text{MAL}}$ no longer high	$t_M - 9$	ns
31	Hold time, address on MADH0–MADH7 after $\overline{\text{MAL}}$ low	$1.5t_M - 9$	ns

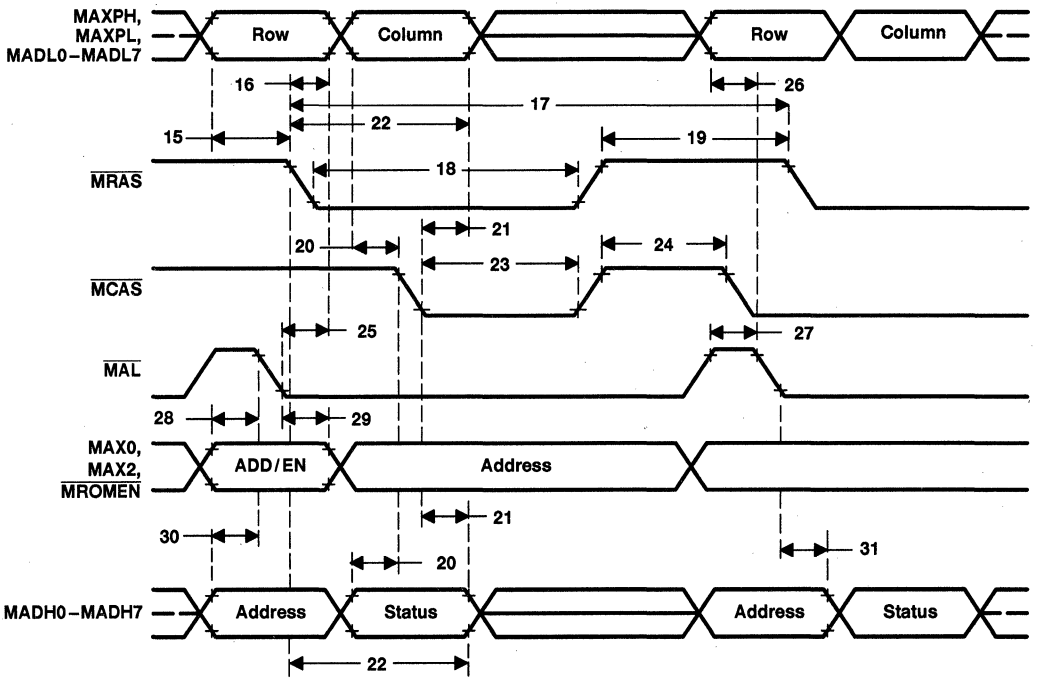


Figure 10. Memory-Bus Timing: Clocks, $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, and $\overline{\text{MAL}}$ to ADDRESS

ADVANCE INFORMATION

memory-bus timing: read cycle

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

NO.		MIN	MAX	UNIT
32	Access time, address/enable valid on MAX0, MAX2, and $\overline{\text{MROMEN}}$ to valid data/parity		$6t_M - 23$	ns
33	Access time, address valid on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 to valid data/parity		$6t_M - 23$	ns
35	Access time, $\overline{\text{MRAS}}$ low to valid data/parity		$4.5t_M - 21.5$	ns
36	Hold time, valid data/parity after $\overline{\text{MRAS}}$ no longer low	0		ns
37†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7 and MADL0–MADL7 after $\overline{\text{MRAS}}$ high (see Note 19)	$2t_M - 10.5$		ns
38	Access time, $\overline{\text{MCAS}}$ low to valid data/parity		$3t_M - 23$	ns
39	Hold time, valid data/parity after $\overline{\text{MCAS}}$ no longer low	0		ns
40†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{\text{MCAS}}$ high (see Note 19)	$2t_M - 13$		ns
41	Delay time, $\overline{\text{MCAS}}$ no longer high to $\overline{\text{MOE}}$ low		$t_M + 13$	ns
42†	Setup time, address / status in the high-impedance state on MAXPH, MAXPL, MADL0–MADL7, and MADH0–MADH7 before $\overline{\text{MOE}}$ no longer high	0		ns
43	Access time, $\overline{\text{MOE}}$ low to valid data/parity		$2t_M - 20$	ns
44	Pulse duration, $\overline{\text{MOE}}$ low	$2t_M - 9$		ns
45	Delay time, $\overline{\text{MCAS}}$ low to $\overline{\text{MOE}}$ no longer low	$3t_M - 9$		ns
46	Hold time, valid data/parity in after $\overline{\text{MOE}}$ no longer low	0		ns
47†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{\text{MOE}}$ high (see Note 19)	$2t_M - 15$		ns
48†	Setup time, address / status in the high-impedance state on MAXPH, MAXPL, MADL0–MADL7, and MADH0–MADH7, before $\overline{\text{MBEN}}$ no longer high	0		ns
48a†	Setup time, address / status in the high-impedance state on MAXPH, MAXPL, MADL0–MADL7, and MADH0–MADH7 and before $\overline{\text{MBIAEN}}$ no longer high	0		ns
49	Access time, $\overline{\text{MBEN}}$ low to valid data/parity		$2t_M - 25$	ns
49a	Access time, $\overline{\text{MBIAEN}}$ low to valid data/parity		$2t_M - 25$	ns
50	Pulse duration, $\overline{\text{MBEN}}$ low	$2t_M - 9$		ns
50a	Pulse duration, $\overline{\text{MBIAEN}}$ low	$2t_M - 9$		ns
51	Hold time, valid data/parity after $\overline{\text{MBEN}}$ no longer low	0		ns
51a	Hold time, valid data/parity after $\overline{\text{MBIAEN}}$ no longer low	0		ns
52†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{\text{MBEN}}$ high (see Note 19)	$2t_M - 15$		ns
52a†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{\text{MBIAEN}}$ high	$2t_M - 15$		ns
53	Hold time, MDDIR high after $\overline{\text{MBEN}}$ high, read follows write cycle	$1.5t_M - 12$		ns
54	Setup time, MDDIR low before $\overline{\text{MBEN}}$ no longer high	$3t_M - 5$		ns
55	Hold time, MDDIR low after $\overline{\text{MBEN}}$ high, write follows read cycle	$3t_M - 12$		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.

NOTE 19: The data/parity that exists on the address lines will most likely reach the high-impedance state sometime later than the rising edge of $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, $\overline{\text{MOE}}$, or $\overline{\text{MBEN}}$ (between MIN and MAX of timing parameter 36) and will be a function of the memory being read. The MIN time given represents the time from the rising edge of $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, $\overline{\text{MOE}}$, or $\overline{\text{MBEN}}$ to the beginning of the next address, and does not represent the actual high-impedance period on the address bus.

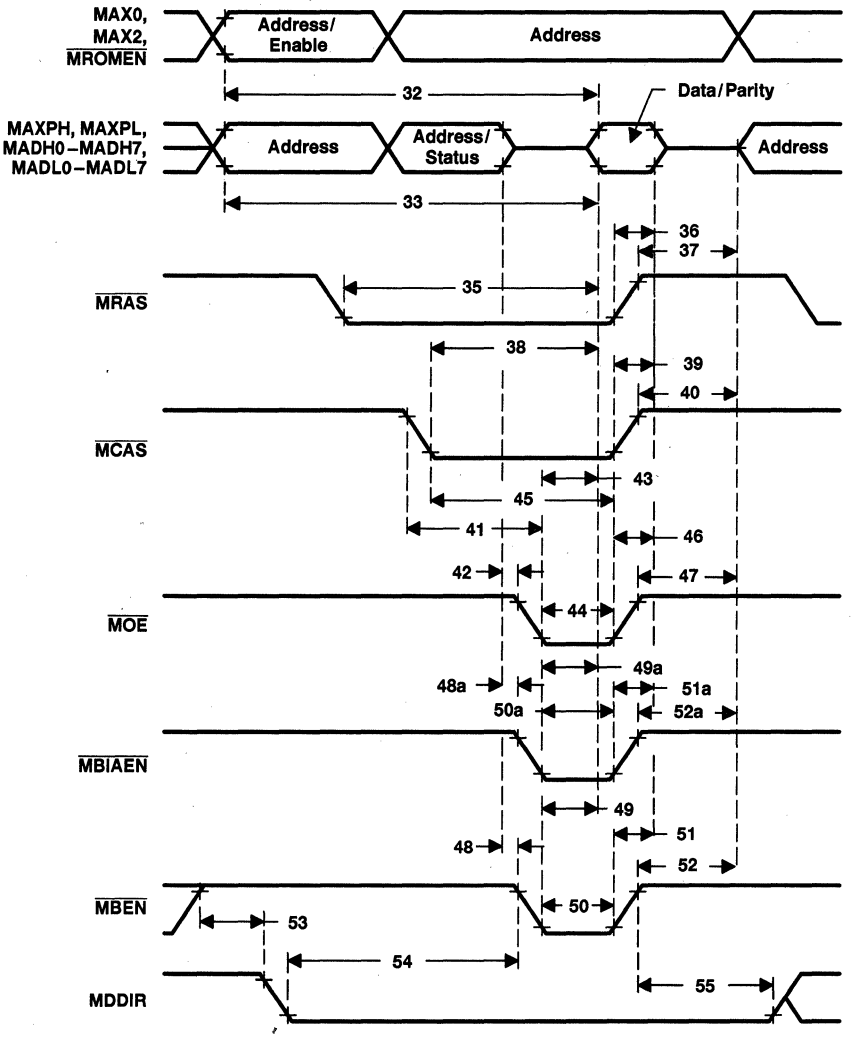


Figure 11. Memory-Bus Timing: Read Cycle

memory-bus timing: write cycle

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

NO.		MIN	MAX	UNIT
58	Setup time, $\overline{MW}$ low before $\overline{MRAS}$ no longer low	t_M		ns
60	Setup time, $\overline{MW}$ low before $\overline{MCAS}$ no longer low	$1.5t_M-6.5$		ns
63	Setup time, valid data/parity before $\overline{MW}$ no longer high	5.1		ns
64	Pulse duration, $\overline{MW}$ low	$2.5t_M-9$		ns
65	Hold time, data/parity out valid after $\overline{MW}$ high	$0.5t_M-10.5$		ns
66	Setup time, address valid on MAX0, MAX2, and $\overline{MROMEN}$ before $\overline{MW}$ no longer low	$7t_M-11.5$		ns
67	Hold time, $\overline{MRAS}$ low to $\overline{MW}$ no longer low	$5.5t_M-9$		ns
69	Hold time, $\overline{MCAS}$ low to $\overline{MW}$ no longer low	$4t_M-11.5$		ns
70	Setup time, $\overline{MBEN}$ low before $\overline{MW}$ no longer high	$1.5t_M-13.5$		ns
71	Hold time, $\overline{MBEN}$ low after $\overline{MW}$ high	$0.5t_M-6.5$		ns
72	Setup time, MDDIR high before $\overline{MBEN}$ no longer high	$2t_M-9$		ns
73	Hold time, MDDIR high after $\overline{MBEN}$ high	$1.5t_M-12$		ns

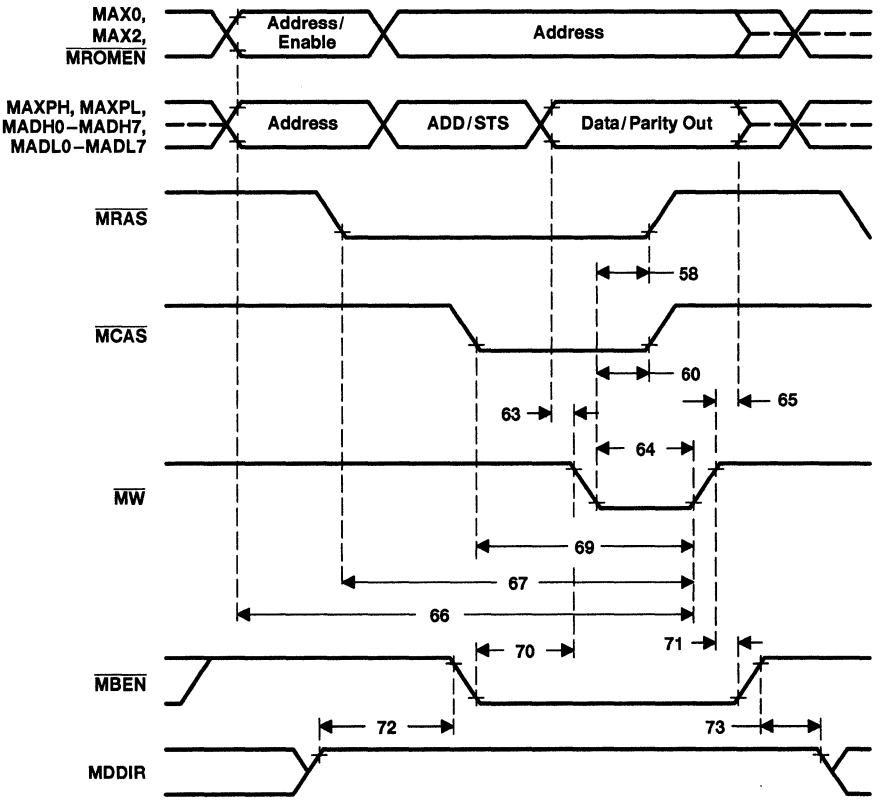


Figure 12. Memory-Bus Timing: Write Cycle

ADVANCE INFORMATION

memory-bus timing: DRAM-refresh timing

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

NO.		MIN	MAX	UNIT
15	Setup time, row address on MADL0–MADL7, MAXPH, and MAXPL before $\overline{MRAS}$ no longer high	$1.5t_M-11.5$		ns
16	Hold time, row address on MADL0–MADL7, MAXPH, and MAXPL after $\overline{MRAS}$ no longer high	$t_M-6.5$		ns
18	Pulse duration, $\overline{MRAS}$ low	$4.5t_M-5$		ns
19	Pulse duration, $\overline{MRAS}$ high	$3.5t_M-5$		ns
73a	Setup time, $\overline{MCAS}$ low before $\overline{MRAS}$ no longer high	$1.5t_M-11.5$		ns
73b	Hold time, $\overline{MCAS}$ low after $\overline{MRAS}$ low	$4.5t_M-6.5$		ns
73c	Setup time, MREF high before $\overline{MCAS}$ no longer high	14		ns
73d	Hold time, MREF high after $\overline{MCAS}$ high	t_M-9		ns

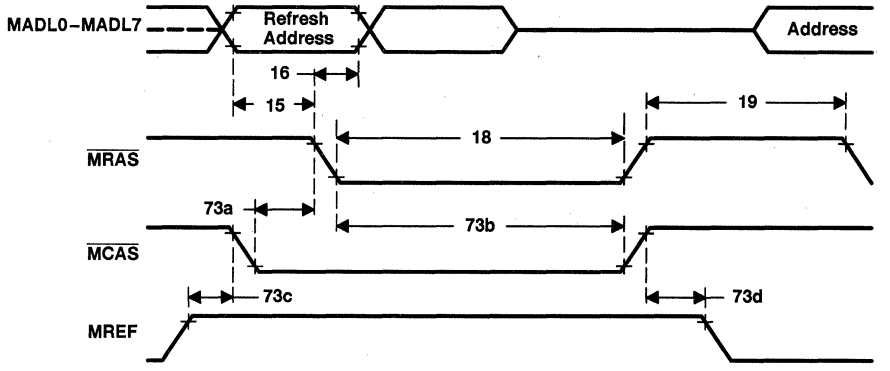


Figure 13. Memory-Bus Timing: DRAM-Refresh Cycle

XMATCH and XFAIL timing

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

NO.		MIN	MAX	UNIT
127	Delay time, status bit 7 high to XMATCH and XFAIL recognized	$7t_M$		ns
128	Pulse duration, XMATCH or XFAIL high	50		ns

Figure 14. XMATCH and XFAIL Timing

token ring: ring-interface timing

NO.			MIN	TYP	MAX	UNIT
153	Period of RCLK (see Note 20)	4 Mbps		125		ns
		16 Mbps		31.25		ns
154L	Pulse duration, RCLK low	4 Mbps nominal: 62.5 ns	46			ns
		16 Mbps nominal: 15.625 ns	15			ns
154H	Pulse duration, RCLK high	4 Mbps nominal: 62.5 ns	35			ns
		16 Mbps nominal: 15.625 ns	8			ns
155	Setup time, RCVR valid before rising edge (1.8 V) of RCLK at 16 Mbps		10			ns
156	Hold time, RCVR valid after rising edge (1.8 V) of RCLK at 16 Mbps		4			ns
158L	Pulse duration, ring-baud clock low	4 Mbps	40			ns
		16 Mbps	8			ns
158H	Pulse duration, ring-baud clock high	4 Mbps	40			ns
		16 Mbps	8			ns
165	Period of OSCOUT and PXTALIN (see Note 20)	4 Mbps		125		ns
		16 Mbps (for PXTALIN only)		31.25		ns
	Tolerance of PXTALIN input frequency (see Note 20)				± 0.01	%

NOTE 20: This parameter is not tested but is required by the IEEE 802.5 specification.

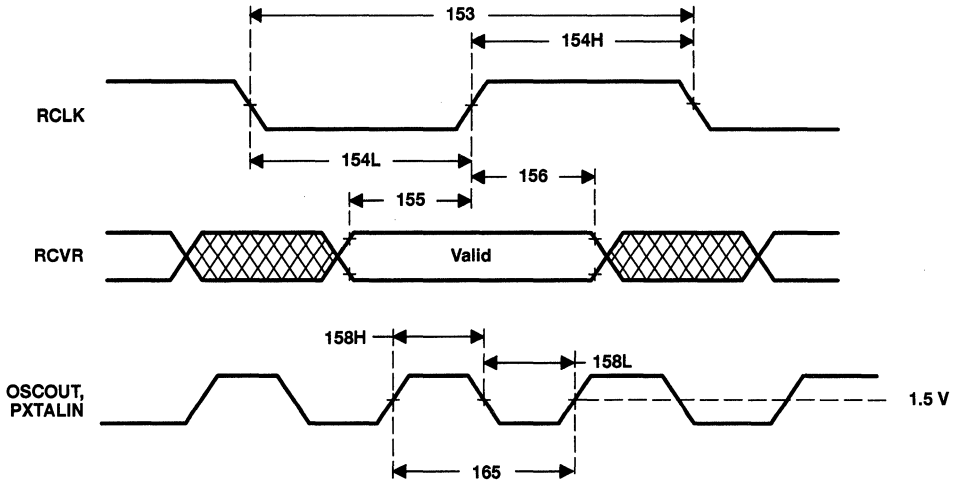


Figure 15. Ring-Interface Timing

ADVANCE INFORMATION

token ring: transmitter timing

NO.			MIN	MAX	UNIT
159	$t_{sk(DR)}$	Delay time, DRVR rising edge (1.8 V) to $\overline{DRVR}$ falling edge (1 V) or DRVR falling edge (1 V) to $\overline{DRVR}$ rising edge (1.8 V)		±2	ns
160	$t_{d(DR)H}$†	Delay time, RCLK (or PXTALIN) falling edge (1 V) to DRVR rising edge (1.8 V)	See Note 21		ns
161	$t_{d(DR)L}$†	Delay time, RCLK (or PXTALIN) falling edge (1 V) to DRVR falling edge (1 V)	See Note 21		ns
162	$t_{d(DRN)H}$†	Delay time, RCLK (or PXTALIN) falling edge (1 V) to $\overline{DRVR}$ falling edge (1 V)	See Note 21		ns
163	$t_{(DRN)L}$†	Delay time, RCLK (or PXTALIN) falling edge (1 V) to $\overline{DRVR}$ rising edge (1.8 V)	See Note 21		ns
164	DRVR / $\overline{DRVR}$ asymmetry	$\frac{t_{d(DR)L} + t_{d(DRN)H}}{2} - \frac{t_{d(DR)H} + t_{d(DRN)L}}{2}$		±1.5	ns

† When in active-monitor mode, the clock source is PXTALIN; otherwise, the clock-source is either RCLK or PXTALIN.
NOTE 21: This parameter is not tested to a minimum or a maximum but is measured and used as a component required for parameter 164.

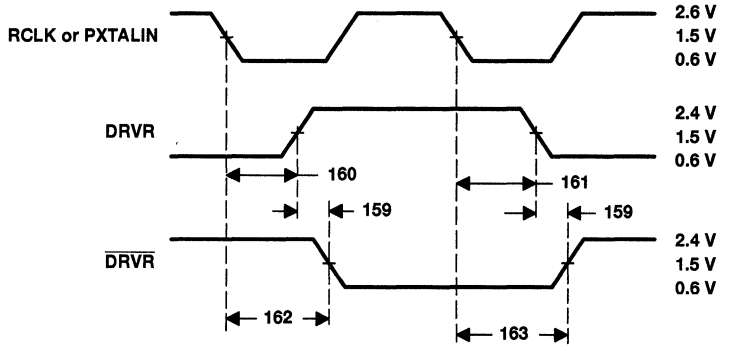


Figure 16. Skew and Asymmetry From RCLK or PXTALIN to DRVR and $\overline{DRVR}$

ADVANCE INFORMATION

80x8x DIO read-cycle timing

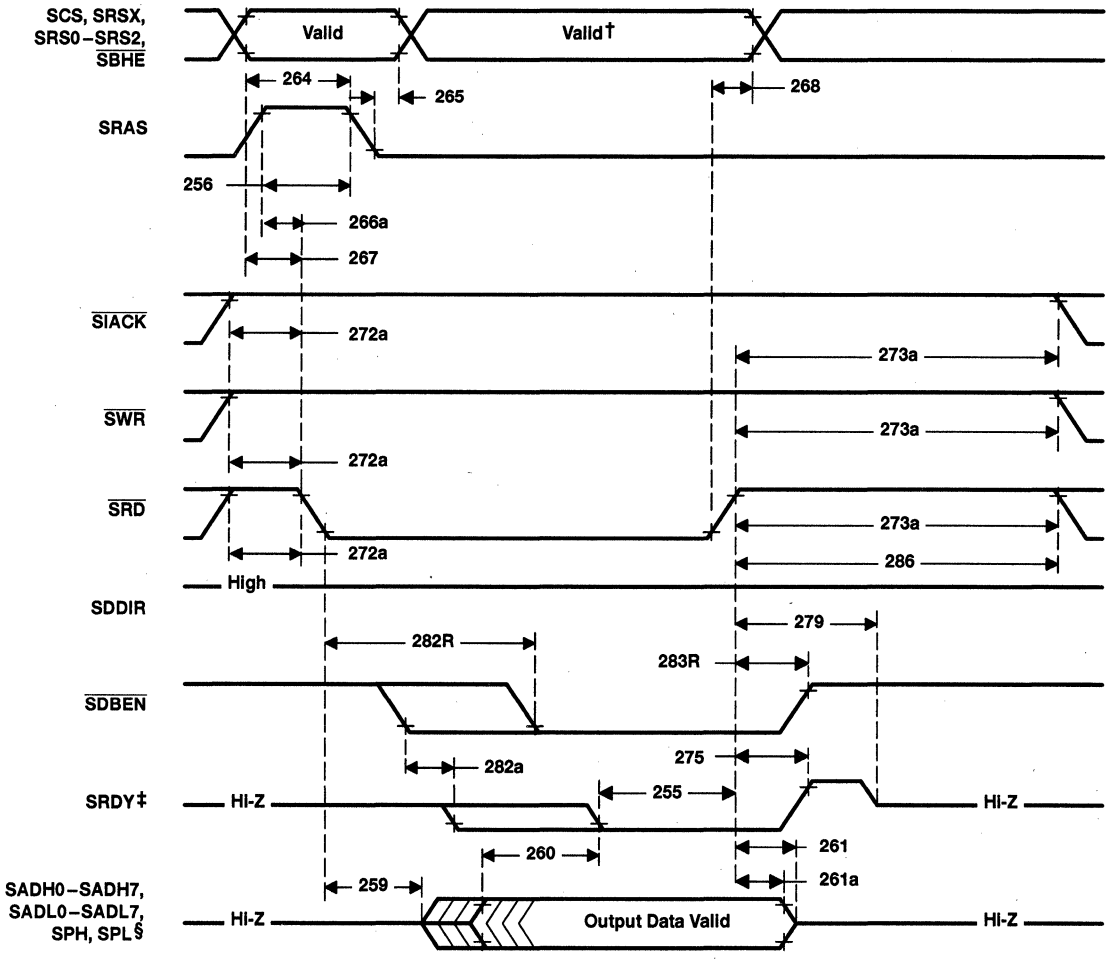
NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
255	Delay time, $\overline{SRDY}$ low to either $\overline{SCS}$ or $\overline{SRD}$ high	15		15		ns
256	Pulse duration, SRAS high	30		30		ns
259†	Hold time, SAD in the high-impedance state after $\overline{SRD}$ low (see Note 22)	0		0		ns
260	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before $\overline{SRDY}$ low	0		0		ns
261†	Delay time, $\overline{SRD}$ or $\overline{SCS}$ high to SAD in the high-impedance state (see Note 22)		35		35	ns
261a	Hold time, output data valid after $\overline{SRD}$ or $\overline{SCS}$ high (see Note 22)	0		0		ns
264	Setup time, SRSX, SRS0–SRS2, $\overline{SCS}$, and $\overline{SBHE}$ valid to SRAS no longer high (see Note 23)	30		30		ns
265	Hold time, SRSX, SRS0–SRS2, $\overline{SCS}$, and $\overline{SBHE}$ valid after SRAS low	10		10		ns
266a	Setup time, SRAS high to $\overline{SRD}$ no longer high (see Note 23)	15		15		ns
267‡	Setup time, SRSX, SRS0–SRS2 valid before $\overline{SRD}$ no longer high (see Note 22)	15		15		ns
268	Hold time, SRSX, SRS0–SRS2 valid after $\overline{SRD}$ no longer low (see Note 23)	0		0		ns
272a	Setup time, $\overline{SRD}$, $\overline{SWR}$, and $\overline{SIACK}$ high from previous cycle to $\overline{SRD}$ no longer high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
273a	Hold time, $\overline{SRD}$, $\overline{SWR}$, and $\overline{SIACK}$ high after $\overline{SRD}$ high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
275	Delay time, $\overline{SRD}$ and $\overline{SWR}$, or $\overline{SCS}$ high to $\overline{SRDY}$ high (see Note 22)	0	25	0	25	ns
279†	Delay time, $\overline{SRD}$ and $\overline{SWR}$, high to $\overline{SRDY}$ in the high-impedance state	0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
282a	Delay time, $\overline{SDBEN}$ low to $\overline{SRDY}$ low in a read cycle	0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
282R	Delay time, $\overline{SRD}$ low to $\overline{SDBEN}$ low (see *TMS380 Second Generation Token-Ring User's Guide*, SPWU005, subsection 3.4.1.1.1), provided previous cycle completed	0	$t_{c(SCK)}+3$	0	$t_{c(SCK)}+3$	ns
283R	Delay time, $\overline{SRD}$ high to $\overline{SDBEN}$ high (see Note 22)	0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
286	Pulse duration, $\overline{SRD}$ high between DIO accesses (see Note 22)	$t_{c(SCK)}$		$t_{c(SCK)}$		ns

† This specification is provided as an aid to board design. It is not assured during manufacturing testing.
‡ It is the later of $\overline{SRD}$ and $\overline{SWR}$ or $\overline{SCS}$ low that indicates the start of the cycle.

NOTES: 22. The inactive chip select is $\overline{SIACK}$ in DIO-read and DIO-write cycles, and $\overline{SCS}$ is the inactive chip select in interrupt-acknowledge cycles.

23. In 80x8x mode, SRAS can be used to strobe the values of $\overline{SBHE}$, SRSX, SRS0 – SRS2, and $\overline{SCS}$. When used to do so, SRAS must meet parameter 266a, and $\overline{SBHE}$, SRS0–SRS2, and $\overline{SCS}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.

ADVANCE INFORMATION



† In 80x8x mode, SRAS can be used to strobe the values of $\overline{\text{SBHE}}$, SRSX, SRS0–SRS2, and $\overline{\text{SCS}}$. When used to do so, SRAS must meet parameter 266a; $\overline{\text{SBHE}}$, SRS0–SRS2, and $\overline{\text{SCS}}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.

‡ When the TMS380C25 begins to drive $\overline{\text{SDBEN}}$ inactive, it has already latched the write data internally. Parameter 263 must be met to the input of the data buffers.

§ In 8-bit 80x8x mode DIO reads, the SADH0–SADH7 contain don't-care data.

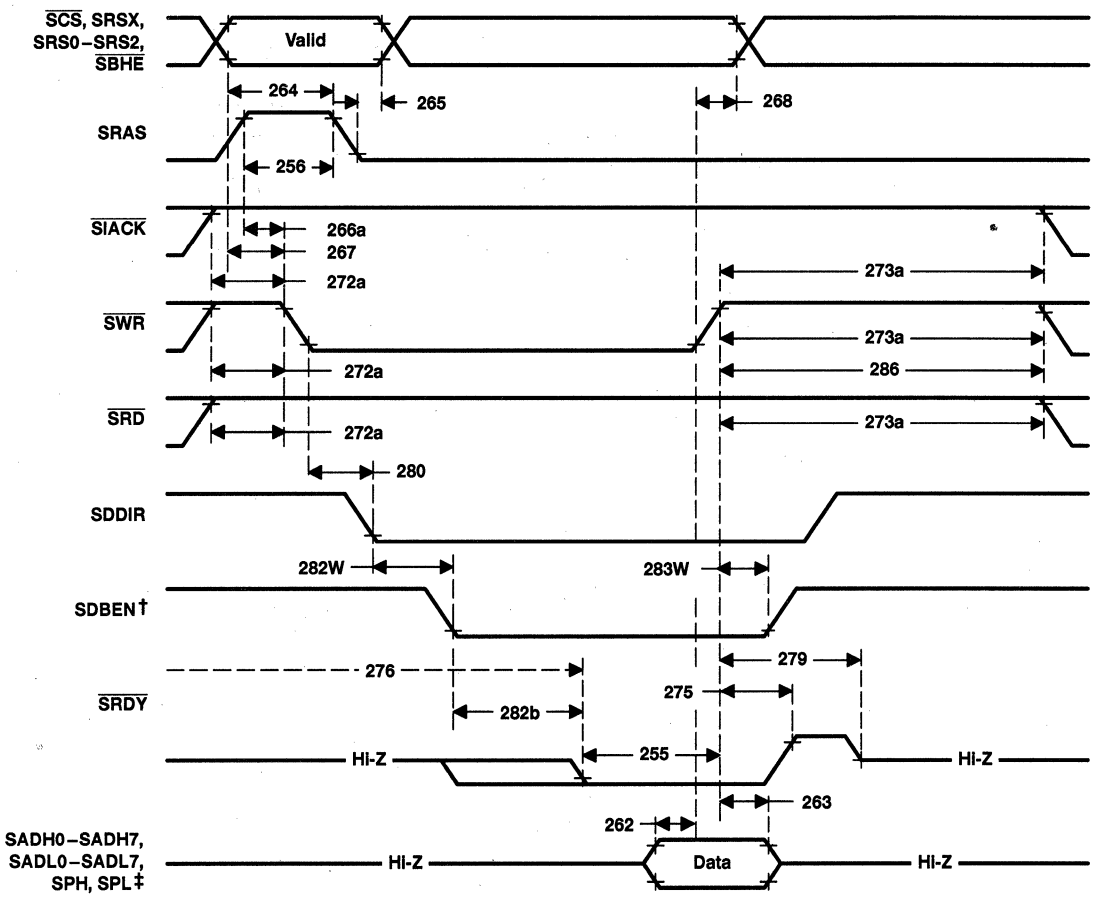
Figure 17. 80x8x DIO Read-Cycle Timing

80x8x DIO write-cycle timing

NO.			25-MHz OPERATION		33-MHz OPERATION		UNIT
			MIN	MAX	MIN	MAX	
255	Delay time, $\overline{SRDY}$ low to either $\overline{SCS}$ or $\overline{SWR}$ high		15		15		ns
256	Pulse duration, SRAS high		30		30		ns
262	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before $\overline{SCS}$ or $\overline{SWR}$ no longer low		15		15		ns
263	Hold time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid after $\overline{SCS}$ or $\overline{SWR}$ high		15		15		ns
264	Setup time, SRSX, SRS0–SRS2, $\overline{SCS}$, and $\overline{SBHE}$ to SRAS no longer high (see Note 23)		30		30		ns
265	Hold time, SRSX, SRS0–SRS2, $\overline{SCS}$, and $\overline{SBHE}$ after SRAS low		10		10		ns
266a	Setup time, SRAS high to $\overline{SWR}$ no longer high (see Note 22)		15		15		ns
267†	Setup time, SRSX, SRS0–SRS2 before $\overline{SWR}$ no longer high (see Note 22)		15		15		ns
268	Hold time, SRSX, SRS0–SRS2 valid after $\overline{SWR}$ no longer low (see Note 23)		0		0		ns
272a	Setup time, $\overline{SRD}$, $\overline{SWR}$, and $\overline{SIACK}$ high from previous cycle to $\overline{SWR}$ no longer high		$t_{c(SCK)}$		$t_{c(SCK)}$		ns
273a	Hold time, $\overline{SRD}$, $\overline{SWR}$, and $\overline{SIACK}$ high after $\overline{SWR}$ high		$t_{c(SCK)}$		$t_{c(SCK)}$		ns
276‡	Delay time, $\overline{SRDY}$ low in the first DIO access to the SIF register to $\overline{SRDY}$ low in the immediately following access to the SIF (see *TMS380 Second-Generation Token-Ring User's Guide*, SPWU005, subsection 3.4.1.1.1)			4000		4000	
275	Delay time, $\overline{SWR}$ or $\overline{SCS}$ high to $\overline{SRDY}$ high (see Note 22)		0	25	0	25	ns
279§	Delay time, $\overline{SWR}$ high to $\overline{SRDY}$ in the high-impedance state		0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
280	Delay time, $\overline{SWR}$ low to SDDIR low (see Note 22)		0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
282b	Delay time, SDBEN low to SRDY low (see *TMS380 Second Generation Token-Ring User's Guide*, SPWU005, subsection 3.4.1.1.1)	If SIF register is ready (no waiting required)	0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
		If SIF register is not ready (waiting required)	0	4000	0	4000	
282W	Delay time, SDDIR low to $\overline{SDBEN}$ low		0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
283W	Delay time, $\overline{SCS}$ or $\overline{SWR}$ high to $\overline{SDBEN}$ no longer low		0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
286	Pulse duration, $\overline{SWR}$ high between DIO accesses (see Note 22)		$t_{c(SCK)}$		$t_{c(SCK)}$		ns

† It is the later of $\overline{SRD}$ and $\overline{SWR}$ or $\overline{SCS}$ low that indicates the start of the cycle.
‡ This specification has been characterized to meet stated value. It is not assured during manufacturing testing.
§ This specification is provided as an aid to board design. It is not assured during manufacturing testing.
NOTES: 22. The inactive chip select is $\overline{SIACK}$ in DIO-read and DIO-write cycles; $\overline{SCS}$ is the inactive chip select in interrupt-acknowledge cycles.
23. In 80x8x mode, SRAS can be used to strobe the values of $\overline{SBHE}$, SRSX, SRS0–SRS2, and $\overline{SCS}$. When used to do so, SRAS must meet parameter 266a; $\overline{SBHE}$, SRS0–SRS2, and $\overline{SCS}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.

ADVANCE INFORMATION



† When the TMS380C25 begins to drive $\overline{\text{SDBEN}}$ inactive, it has already latched the write data internally. Parameter 263 must be met to the input of the data buffers.

‡ In 8-bit 80x8x-mode DIO writes, the value placed on SADH0–SADH7 is a don't care.

Figure 18. 80x8x DIO Write-Cycle Timing

80x8x interrupt-acknowledge-cycle timing: first $\overline{\text{SIACK}}$ pulse

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
286	Pulse duration, $\overline{\text{SIACK}}$ high between DIO accesses (see Note 22)	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
287	Pulse duration, $\overline{\text{SIACK}}$ low on first pulse of two pulses	$t_{c(SCK)}$		$t_{c(SCK)}$		ns

NOTE 22: The inactive chip select is $\overline{\text{SIACK}}$ in DIO-read and DIO-write cycles, and $\overline{\text{SCS}}$ is the inactive chip select in interrupt-acknowledge cycles.

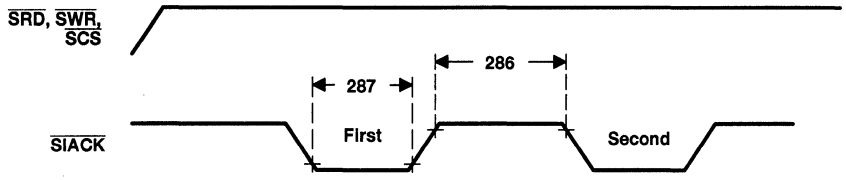
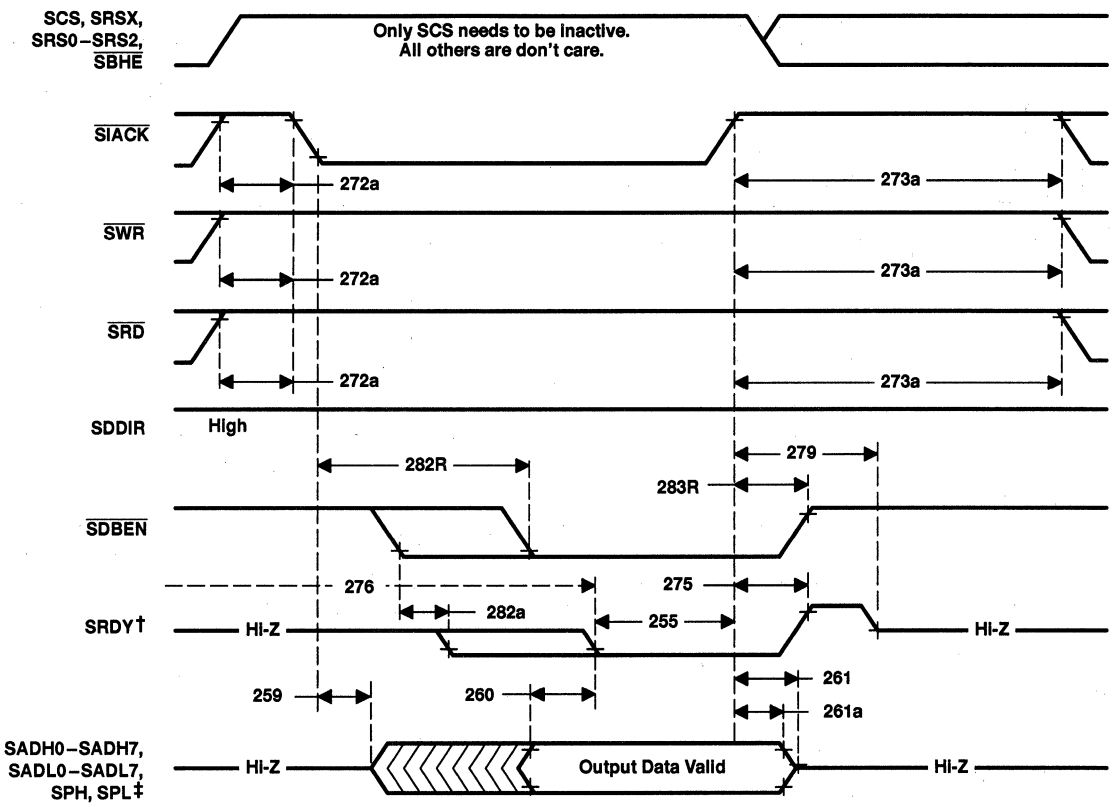


Figure 19. 80x8x Interrupt-Acknowledge-Cycle Timing: First $\overline{\text{SIACK}}$ Pulse

80x8x interrupt-acknowledge-cycle timing: second $\overline{\text{SIACK}}$ pulse

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
255	Delay time, $\overline{\text{SRDY}}$ low to $\overline{\text{SCS}}$ high	15		15		ns
259†	Hold time, SAD in the high-impedance state after $\overline{\text{SIACK}}$ low (see Note 22)	0		0		ns
260	Setup time, output data valid before $\overline{\text{SRDY}}$ low	0		0		ns
261†	Delay time, $\overline{\text{SIACK}}$ high to SAD in the high-impedance state (see Note 22)		35		35	ns
261a	Hold time, output data valid after $\overline{\text{SIACK}}$ high (see Note 22)	0		0		ns
272a	Setup time, inactive data strobe high to $\overline{\text{SIACK}}$ no longer high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
273a	Hold time, inactive data strobe high after $\overline{\text{SIACK}}$ high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
275	Delay time, $\overline{\text{SIACK}}$ high to $\overline{\text{SRDY}}$ high (see Note 22)	0	25	0	25	ns
276‡	Delay time, $\overline{\text{SRDY}}$ low in the first DIO access to the SIF register to $\overline{\text{SRDY}}$ low in the immediately following access to the SIF		4000		4000	ns
279†	Delay time, $\overline{\text{SIACK}}$ high to $\overline{\text{SRDY}}$ in the high-impedance state	0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
282a	Delay time, $\overline{\text{SDBEN}}$ low to $\overline{\text{SRDY}}$ low in a read cycle	0	$t_{c(SCK)} / 2 + 4$	0	$t_{c(SCK)} / 2 + 4$	ns
282R	Delay time, $\overline{\text{SIACK}}$ low to $\overline{\text{SDBEN}}$ low (see *TMS380 Second Generation Token-Ring User's Guide*, SPWU005, subsection 3.4.1.1.1), provided previous cycle completed	0	$t_{c(SCK)} + 3$	0	$t_{c(SCK)} + 3$	ns
283R	Delay time, $\overline{\text{SIACK}}$ high to $\overline{\text{SDBEN}}$ high (see Note 22)	0	$t_{c(SCK)} / 2 + 4$	0	$t_{c(SCK)} / 2 + 4$	ns

† This specification is provided as an aid to board design. It is not assured during manufacturing.
‡ This specification has been characterized to meet stated value. It is not assured during manufacturing.
NOTE 22: The inactive chip select is $\overline{\text{SIACK}}$ in DIO-read and DIO-write cycles; $\overline{\text{SCS}}$ is the inactive chip select in interrupt-acknowledge cycles.



NOTES: A. $\overline{\text{SRDY}}$ is an active-low bus ready signal. It must be asserted before data output.
B. In 8-bit 80x8x-mode DIO writes, the value placed on SADH0–SADH7 is a don't care.

Figure 20. 80x8x Interrupt-Acknowledge-Cycle Timing: Second $\overline{\text{SIACK}}$ Pulse

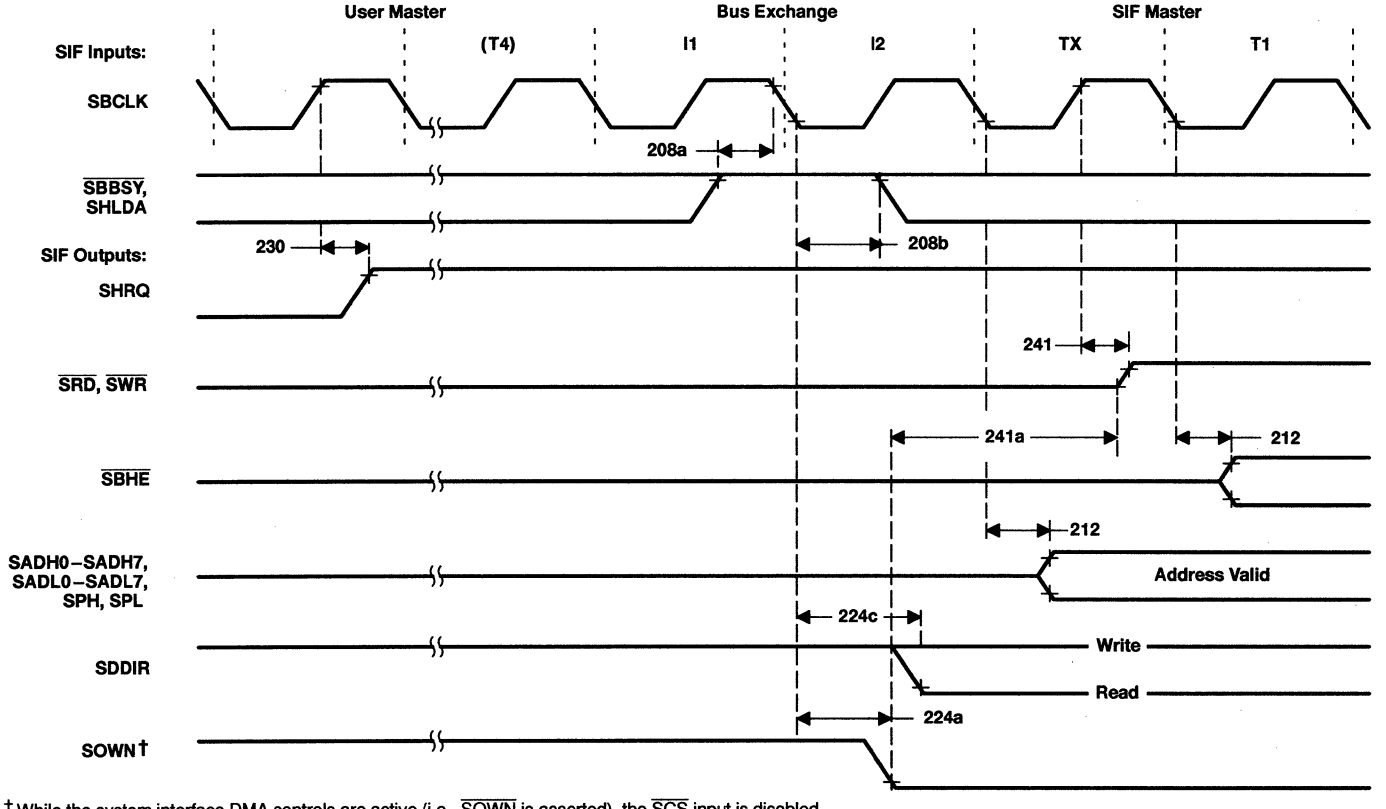
ADVANCE INFORMATION

80x8x-mode bus-arbitration timing, SIF takes control

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous signal $\overline{\text{SBBSY}}$ and SHLDA before SBCLK no longer high to assure recognition on that cycle	10		10		ns
208b	Hold time, asynchronous signal $\overline{\text{SBBSY}}$ and SHLDA after SBCLK low to assure recognition on that cycle	10		10		ns
212	Delay time, SBCLK low to SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid		20		20	ns
224a	Delay time, SBCLK low in cycle I2 to $\overline{\text{SOWN}}$ low	0	20	0	15	ns
224c	Delay time, SBCLK low in cycle I2 to SDDIR low in DMA read		28		23	ns
230	Delay time, SBCLK high to SHRQ high		20		15	ns
241	Delay time, SBCLK high in TX cycle to $\overline{\text{SRD}}$ and $\overline{\text{SWR}}$ high, bus acquisition		25		25	ns
241a†	Hold time, SRD and $\overline{\text{SWR}}$ in the high-impedance state after $\overline{\text{SOWN}}$ low, bus acquisition	$t_{c(SCK)}-15$		$t_{c(SCK)}-15$		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.

ADVANCE INFORMATION



† While the system interface DMA controls are active (i.e., $\overline{\text{SOWN}}$ is asserted), the $\overline{\text{SCS}}$ input is disabled.

Figure 21. 80x8x-Mode Bus-Arbitration Timing, SIF Takes Control

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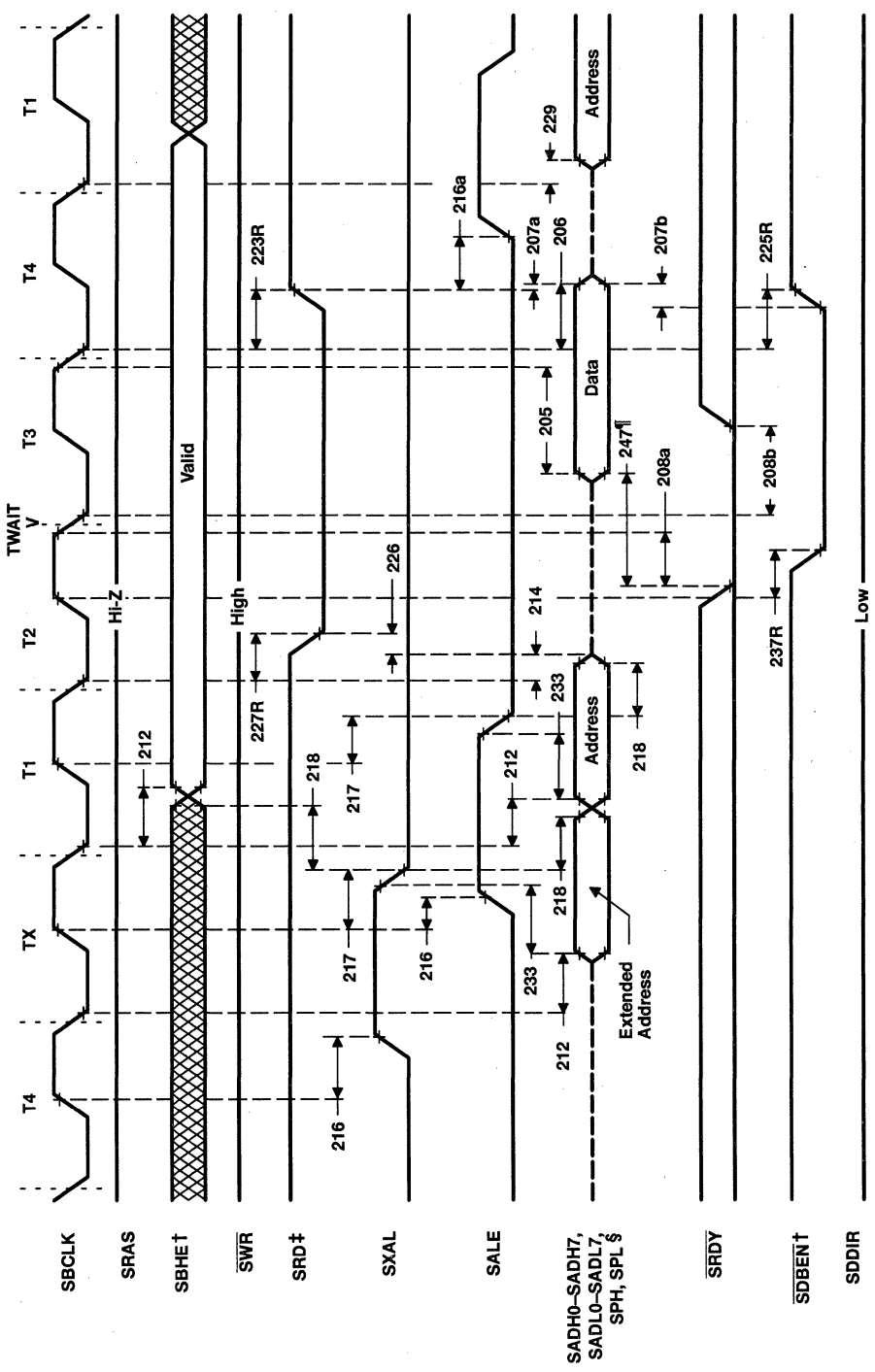
80x8x-mode DMA read-cycle timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
205	Setup time, SADL0–SADL7, SADH0–SADH7, SPH, and SPL valid before SBCLK in T3 cycle no longer high	10		10		ns
206	Hold time, SADL0–SADL7, SADH0–SADH7, SPH, and SPL valid after SBCLK low in T4 cycle if parameters 207a and 207b not met	10		10		ns
207a	Hold time, SADL0–SADL7, SADH0–SADH7, SPH, and SPL valid after $\overline{SRD}$ high	0		0		ns
207b	Hold time, SADL0–SADL7, SADH0–SADH7, SPH, and SPL valid after $\overline{SDBEN}$ no longer low	0		0		ns
208a	Setup time, asynchronous signal $\overline{SRDY}$ before SBCLK no longer high to assure recognition on this cycle	10		10		ns
208b	Hold time, asynchronous signal $\overline{SRDY}$ after SBCLK low to assure recognition on this cycle	10		10		ns
212	Delay time, SBCLK low to address valid		20		20	ns
214†	Delay time, SBCLK low in T1 cycle to SADH0–SADH7, SADL0–SADL7, SPH, and SPL in the high-impedance state		20		15	ns
216	Delay time, SBCLK high to SALE or SXAL high		20		20	ns
216a	Hold time, SALE or SXAL low after $\overline{SRD}$ high	0		0		ns
217	Delay time, SBCLK high to SXAL low in the TX cycle or SALE low in the T1 cycle	0	25	0	25	ns
218	Hold time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid after SALE or SXAL low	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	ns
223R	Delay time, SBCLK low in T4 cycle to $\overline{SRD}$ high (see Note 24)	0	16	0	11	ns
225R	Delay time, SBCLK low in T4 cycle to $\overline{SDBEN}$ high		16		11	ns
226†	Delay time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL in the high-impedance state to $\overline{SRD}$ low	0		0		ns
227R	Delay time, SBCLK low in T2 cycle to $\overline{SRD}$ low	0	15	0	15	ns
229†	Hold time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL in the high-impedance state after SBCLK low in T1 cycle	0		0		ns
231	Pulse duration, $\overline{SRD}$ low	$2t_{c(SCK)}-25$		$2t_{c(SCK)}-25$		ns
233	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before SALE, SXAL no longer high	10		10		ns
237R	Delay time, SBCLK high in the T2 cyle to $\overline{SDBEN}$ low		16		11	ns
247	Setup time, data valid before $\overline{SRDY}$ low if parameter 208a not met	0		0		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.
NOTE 24: While the system-interface DMA controls are active (i.e., $\overline{SOWN}$ is asserted), $\overline{SCS}$ is disabled.

ADVANCE INFORMATION



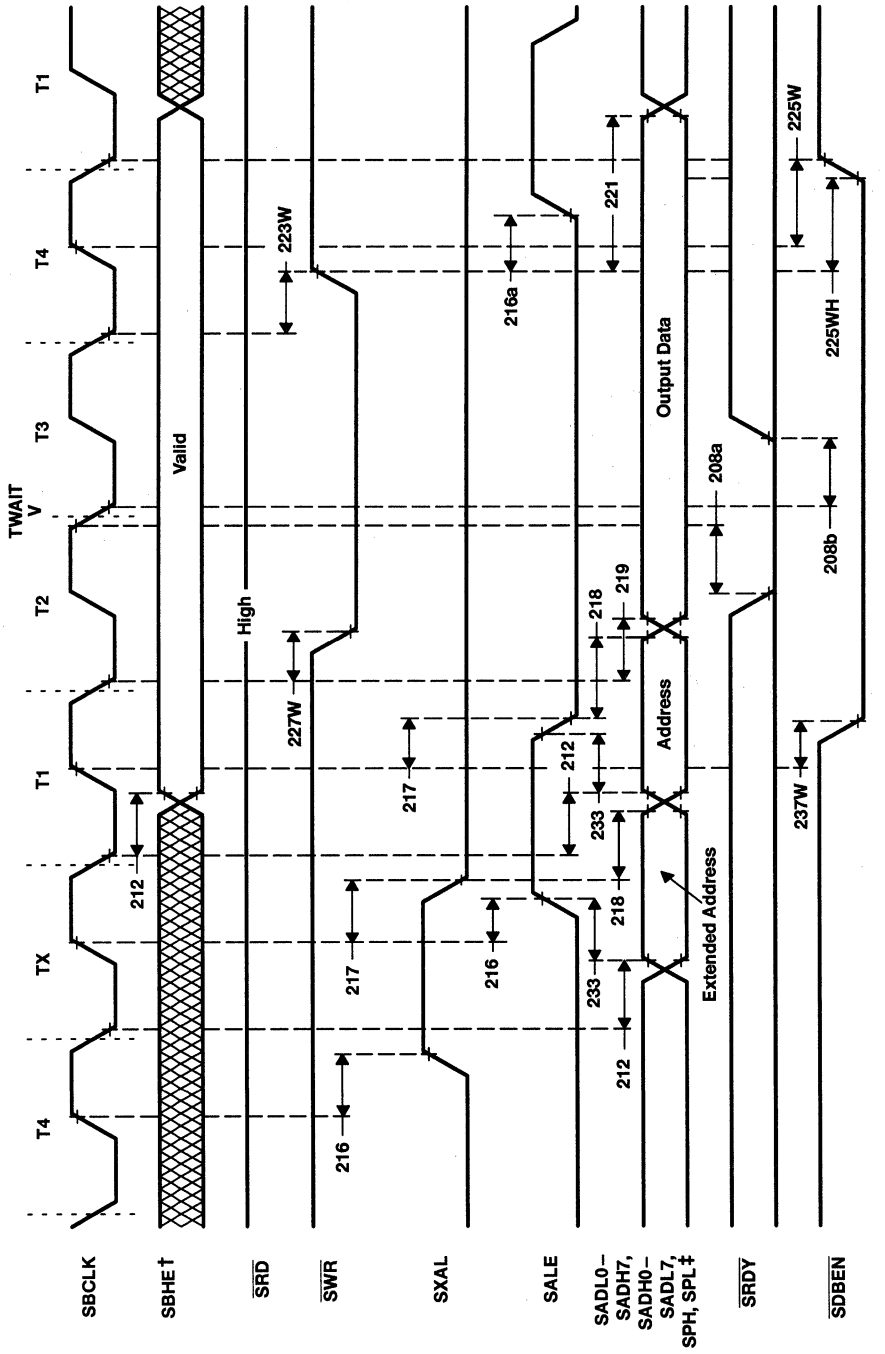
† In 8-bit 80x8x mode, $\overline{SBHE}$/SRNW is a don't care input during DIO and an inactive (high) output during DMA.
‡ Motorola-style bus slaves hold $\overline{SDTACK}$ active until the bus master deasserts $\overline{SAS}$.
§ In 8-bit 80x8x mode, the most significant byte of the address is maintained on SADH for T2, T3, and T4. The address is maintained according to parameter 221; i.e., held after T4 high.
¶ If parameter 208A is not met, then valid data must be present before $\overline{SRDY}$ goes low.

Figure 22. 80x8x-Mode DMA Read-Cycle Timing

80x8x-mode DMA write-cycle timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous signal $\overline{SRDY}$ before SBCLK no longer high to assure recognition on that cycle	10		10		ns
208b	Hold time, asynchronous signal $\overline{SRDY}$ after SBCLK low to assure recognition on that cycle	10		10		ns
212	Delay time, SBCLK low to SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid		20		20	ns
216	Delay time, SBCLK high to SALE or SXAL high		20		20	ns
216a	Hold time, SALE or SXAL low after $\overline{SWR}$ high	0		0		ns
217	Delay time, SBCLK high to SXAL low in the TX cycle or SALE low in the T1 cycle	0	25	0	25	ns
218	Hold time, address valid after SALE, SXAL low	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	ns
219	Delay time, SBCLK low in T2 cycle to output data and parity valid		29		29	ns
221	Hold time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid after $\overline{SWR}$ high	$t_{c(SCK)}-12$		$t_{c(SCK)}-12$		ns
223W	Delay time, SBCLK low to $\overline{SWR}$ high	0	16	0	11	ns
225W	Delay time, SBCLK high in T4 cycle to $\overline{SDBEN}$ high		16		11	ns
225WH	Hold time, $\overline{SDBEN}$ low after $\overline{SWR}$, $\overline{SUDS}$, and $\overline{SLDS}$ high	$t_{c(SCK)}/2-7$		$t_{c(SCK)}/2-7$		ns
227W	Delay time, SBCLK low in T2 cycle to $\overline{SWR}$ low	0	20	0	15	ns
233	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before SALE, SXAL no longer high	10		10		ns
237W	Delay time, SBCLK high in T1 cycle to $\overline{SDBEN}$ low		16		11	ns

ADVANCE INFORMATION



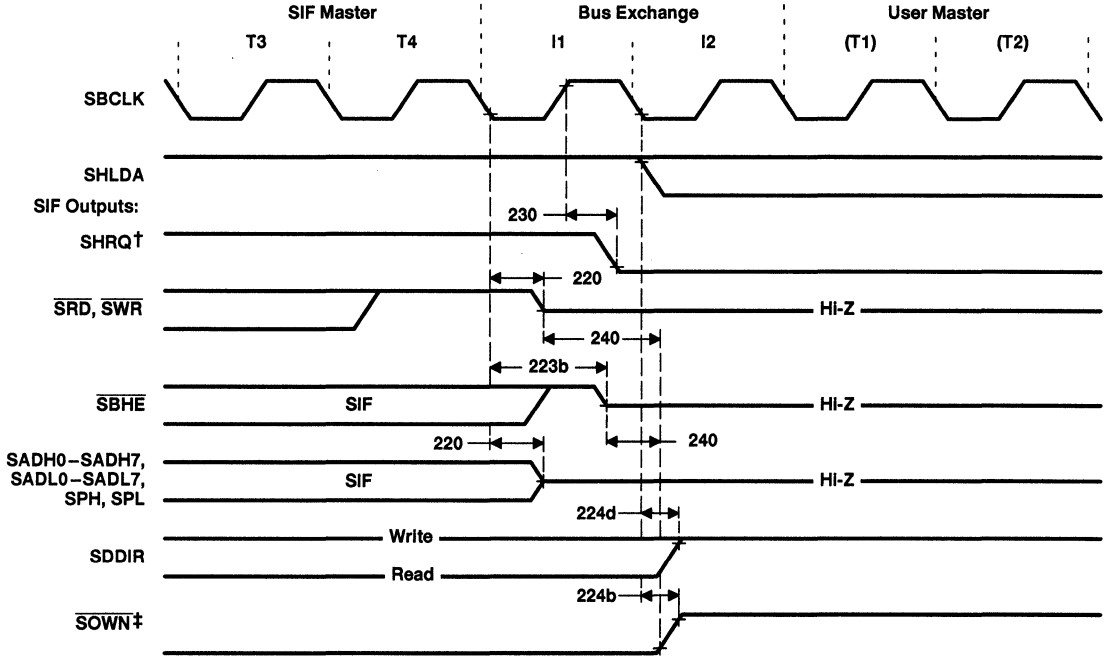
† In 8-bit 80x8x mode, $\overline{SBHE}$/SRNW is a don't care input during DIO and an inactive (high) output during DMA.
‡ In 8-bit 80x8x mode, the most significant byte of the address is maintained on SADH for T2, T3, and T4. The address is maintained according to parameter 221; i.e., held after T4 high.

Figure 23. 80x8x-Mode DMA Write-Cycle Timing

80x8x-mode bus-arbitration timing, SIF returns control

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
220†	Delay time, SBCLK low in I1 cycle to SADH0–SADH7, SADL0–SADL7, SPL, SPH, $\overline{SRD}$, and $\overline{SWR}$ in the high-impedance state		35		35	ns
223b†	Delay time, SBCLK low in I1 cycle to $\overline{SBHE}$ in the high-impedance state		45		45	ns
224b	Delay time, SBCLK low in cycle I2 to $\overline{SOWN}$ high	0	20	0	15	ns
224d	Delay time, SBCLK low in cycle I2 to SDDIR high		27		22	ns
230	Delay time, SBCLK high in cycle I1 to SHRQ low		20		15	ns
240†	Setup time, $\overline{SRD}$, $\overline{SWR}$, and $\overline{SBHE}$ in the high-impedance state before $\overline{SOWN}$ no longer low	0		0		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.



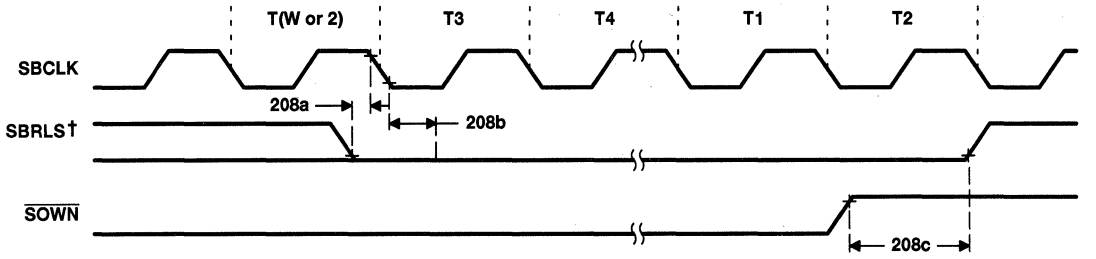
† In 80x8x mode, the system interface deasserts SHRQ on the rising edge of SBCLK following the T4 state of the last system bus transfer it controls. In 68xxx mode, the system interface deasserts $\overline{SBRQ}$ on the rising edge of SBCLK in state T2 of the first system bus-transfer it controls.
‡ While the system-interface DMA controls are active (i.e., $\overline{SOWN}$ is asserted), $\overline{SCS}$ is disabled.

Figure 24. 80x8x-Mode Bus-Arbitration Timing, SIF Returns Control

ADVANCE INFORMATION

80x8x-mode bus-release timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous input $\overline{\text{SBRLS}}$ low before SBCLK no longer high to assure recognition	10		10		ns
208b	Hold time, asynchronous input $\overline{\text{SBRLS}}$ low after SBCLK low to assure recognition	10		10		ns
208c	Hold time, $\overline{\text{SBRLS}}$ low after $\overline{\text{SOWN}}$ high	0		0		ns



† The system interface ignores the assertion of $\overline{\text{SBRLS}}$ if it does not own the system bus. If it does own the bus, when it detects the assertion of $\overline{\text{SBRLS}}$, it completes any internally started DMA cycle and relinquishes control of the bus. If no DMA transfer has started internally, the system interface releases the bus before starting another.

Figure 25. 80x8x-Mode Bus-Release Timing

ADVANCE INFORMATION

68xxx DIO read-cycle timing

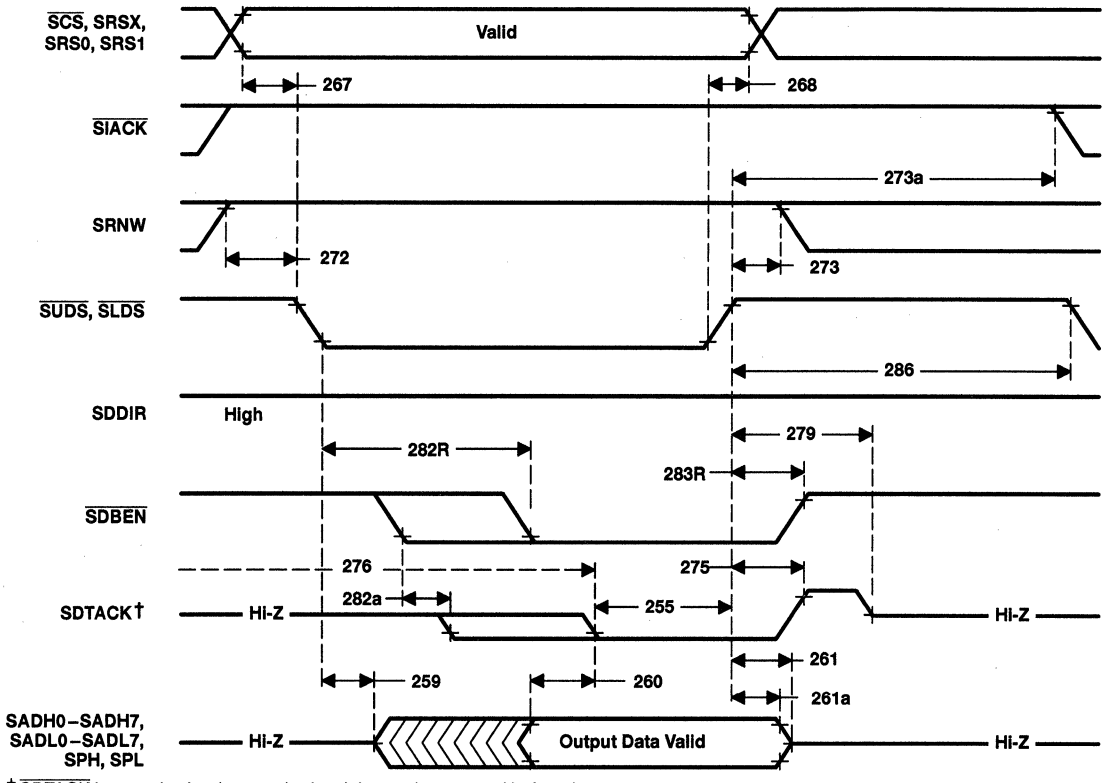
NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
255	Delay time, $\overline{SDTACK}$ low to either $\overline{SCS}$, $\overline{SUDS}$, or $\overline{SLDS}$ high	15		15		ns
259†	Hold time, SAD in the high-impedance state after $\overline{SUDS}$ or $\overline{SLDS}$ low (see Note 22)	0		0		ns
260	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before $\overline{SDTACK}$ low	0		0		ns
261†	Delay time, $\overline{SCS}$, $\overline{SUDS}$, or $\overline{SLDS}$ high to SADH0–SADH7, SADL0–SADL7, SPH, and SPL in the high-impedance state (see Note 22)		35		35	ns
261a	Hold time, output data valid after $\overline{SUDS}$ or $\overline{SLDS}$ no longer low (see Note 22)	0		0		ns
267	Setup time, register address before $\overline{SUDS}$ or $\overline{SLDS}$ no longer high (see Note 22)	15		15		ns
268	Hold time, register address valid after $\overline{SUDS}$ or $\overline{SLDS}$ no longer low (see Note 23)	0		0		ns
272	Setup time, SRNW before $\overline{SUDS}$ or $\overline{SLDS}$ no longer high (see Note 22)	12		12		ns
273	Hold time, SRNW after $\overline{SUDS}$ or $\overline{SLDS}$ high	0		0		ns
273a	Hold time, $\overline{SIACK}$ high after $\overline{SUDS}$ or $\overline{SLDS}$ high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
275	Delay time, $\overline{SCS}$, $\overline{SUDS}$, or $\overline{SLDS}$ high to $\overline{SDTACK}$ high (see Note 22)	0	25	0	25	ns
276‡	Delay time, $\overline{SDTACK}$ low in the first DIO access to the SIF register to $\overline{SDTACK}$ low in the immediately following access to the SIF		4000		4000	ns
279†	Delay time, $\overline{SUDS}$ or $\overline{SLDS}$ high to $\overline{SDTACK}$ in the high-impedance state	0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
282a	Delay time, $\overline{SDBEN}$ low to $\overline{SDTACK}$ low	0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
282R	Delay time, $\overline{SUDS}$ or $\overline{SLDS}$ low to $\overline{SDBEN}$ low (see *TMS380 Second Generation Token-Ring User's Guide,* SPWU005, subsection 3.4.1.1.1), provided the previous cycle completed	0	$t_{c(SCK)}+3$	0	$t_{c(SCK)}+3$	ns
283R	Delay time, $\overline{SUDS}$ or $\overline{SLDS}$ high to $\overline{SDBEN}$ high (see Note 22)	0	$t_{c(SCK)}/2+4$	0	$t_{c(SCK)}/2+4$	ns
286	Pulse duration, $\overline{SUDS}$ or $\overline{SLDS}$ high between DIO accesses (see Note 22)	$t_{c(SCK)}$		$t_{c(SCK)}$		ns

† This specification is provided as an aid to board design. It is not assured during manufacturing testing.
‡ This specification has been characterized to meet stated value. It is not assured during manufacturing testing.

NOTES: 22. The inactive chip select is $\overline{SIACK}$ in DIO-read and DIO-write cycles, and $\overline{SCS}$ is the inactive chip select in interrupt-acknowledge cycles.

23. In 80x8x mode, SRAS can be used to strobe the values of $\overline{SBHE}$, SRSX, SRS0–SRS2, and $\overline{SCS}$. When used to do so, SRAS must meet parameter 266a, and $\overline{SBHE}$, SRS0–SRS2, and $\overline{SCS}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.

ADVANCE INFORMATION



† $\overline{\text{SDTACK}}$ is an active-low bus-ready signal. It must be asserted before data output.

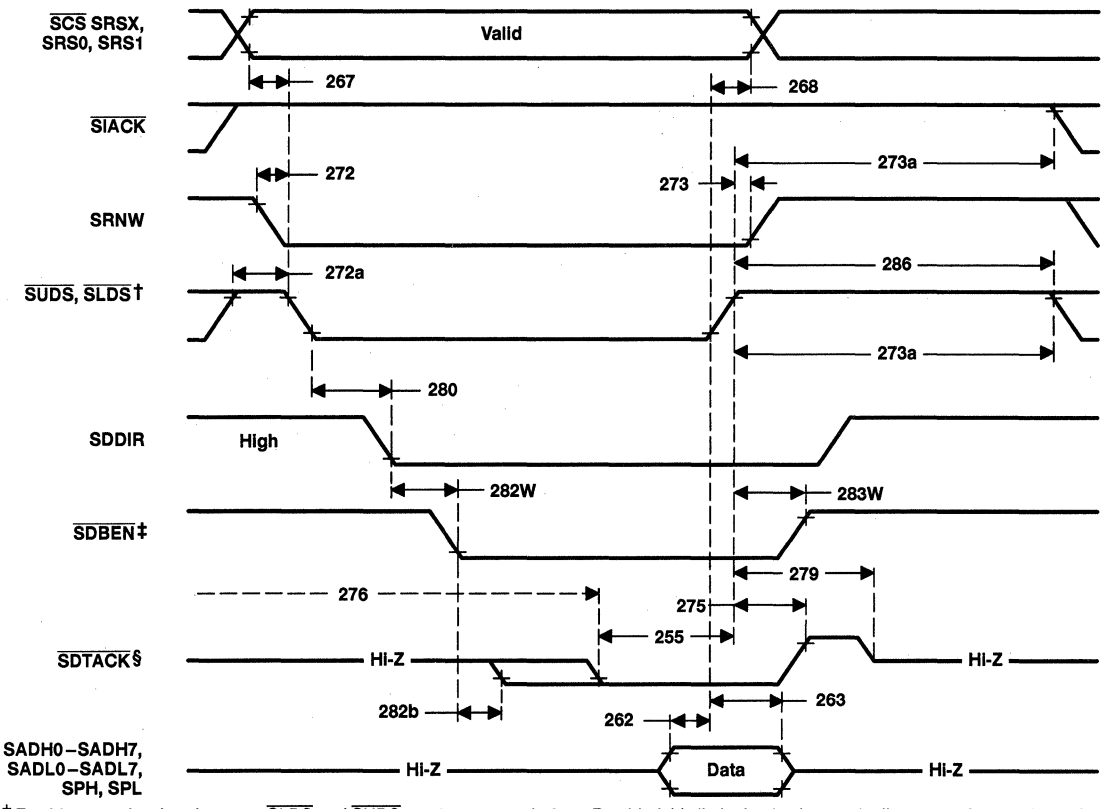
Figure 26. 68xxx DIO Read-Cycle Timing

68xxx DIO write-cycle timing

NO.			25-MHz OPERATION		33-MHz OPERATION		UNIT
			MIN	MAX	MIN	MAX	
255	Delay time, $\overline{SDTACK}$ low to either $\overline{SCS}$, SUDS or $\overline{SLDS}$ high		15		15		ns
262	Setup time, write data valid before $\overline{SUDS}$ or $\overline{SLDS}$ no longer low		15		15		ns
263	Hold time, write data valid after $\overline{SUDS}$ or $\overline{SLDS}$ high		15		15		ns
267†	Setup time, register address before $\overline{SUDS}$ or $\overline{SLDS}$ no longer high (see Note 22)		15		15		ns
268	Hold time, register address valid after $\overline{SUDS}$ or $\overline{SLDS}$ no longer low (see Note 23)		0		0		ns
272	Setup time, SRNW before $\overline{SUDS}$ or $\overline{SLDS}$ no longer high (see Note 22)		12		12		ns
272a	Setup time, inactive $\overline{SUDS}$ or $\overline{SLDS}$ high to active data strobe no longer high		$t_{c(SCK)}$		$t_{c(SCK)}$		ns
273	Hold time, SRNW after $\overline{SUDS}$ or $\overline{SLDS}$ high		0		0		ns
273a	Hold time, inactive $\overline{SUDS}$ or $\overline{SLDS}$ high after active data strobe high		$t_{c(SCK)}$		$t_{c(SCK)}$		ns
275	Delay time, $\overline{SCS}$, $\overline{SUDS}$ or $\overline{SLDS}$ high to $\overline{SDTACK}$ high (see Note 22)		0	25	0	25	ns
276‡	Delay time, $\overline{SDTACK}$ low in the first DIO access to the SIF register to $\overline{SDTACK}$ low in the immediately following access to the SIF			4000		4000	ns
279§	Delay time, $\overline{SUDS}$ or $\overline{SLDS}$ high to $\overline{SDTACK}$ in the high-impedance state		0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
280	Delay time, $\overline{SUDS}$ or $\overline{SLDS}$ low to SDDIR low (see Note 22)		0	$t_{c(SCK)}/2 + 4$	0	$t_{c(SCK)}/2 + 4$	ns
282b	Delay time, SDBEN low to SDTACK low (see *TMS380 Second Generation Token-Ring User's Guide*, SPWU005, subsection 3.4.1.1.1)	If SIF register is ready (no waiting required)	0	$t_{c(SCK)}/2 + 4$	0	$t_{c(SCK)}/2 + 4$	ns
		If SIF register is not ready (waiting required)	0	4000	0	4000	
282W	Delay time, SDDIR low to $\overline{SDBEN}$ low		0	$t_{c(SCK)}/2 + 4$	0	$t_{c(SCK)}/2 + 4$	ns
283W	Delay time, $\overline{SUDS}$ or $\overline{SLDS}$ high to $\overline{SDBEN}$ no longer low		0	$t_{c(SCK)}/2 + 4$	0	$t_{c(SCK)}/2 + 4$	ns
286	Pulse duration, $\overline{SUDS}$ or $\overline{SLDS}$ high between DIO accesses (see Note 22)		$t_{c(SCK)}$		$t_{c(SCK)}$		ns

† It is the later of $\overline{SRD}$ and $\overline{SWR}$ or $\overline{SCS}$ low that indicates the start of the cycle.
‡ This specification has been characterized to meet stated value. It is not assured during manufacturing testing.
§ This specification is provided as an aid to board design. It is not assured during manufacturing testing.
NOTES: 22. The inactive chip select is $\overline{SIACK}$ in DIO-read and DIO-write cycles, and $\overline{SCS}$ is the inactive chip select in interrupt-acknowledge cycles.
23. In 80x8x mode, SRAS can be used to strobe the values of $\overline{SBHE}$, SRSX, SRS0–SRS2, and $\overline{SCS}$. When used to do so, SRAS must meet parameter 266a, and $\overline{SBHE}$, SRS0–SRS2, and $\overline{SCS}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.

ADVANCE INFORMATION



† For 68xxx mode, skew between $\overline{\text{SLDS}}$ and $\overline{\text{SUDS}}$ must not exceed 10 ns. Provided this limitation is observed, all events referenced to a data strobe edge use the later occurring edge. Events defined by two data strobes, edges, such as parameter 286, are measured between latest and earlier edges.

‡ When the TMS380C25 begins to drive $\overline{\text{SDBEN}}$ inactive, it has already latched the write data internally. Parameter 263 must be met to the input of the data buffers.

§ $\overline{\text{SDTACK}}$ is an active-low bus ready signal. It must be asserted before data output.

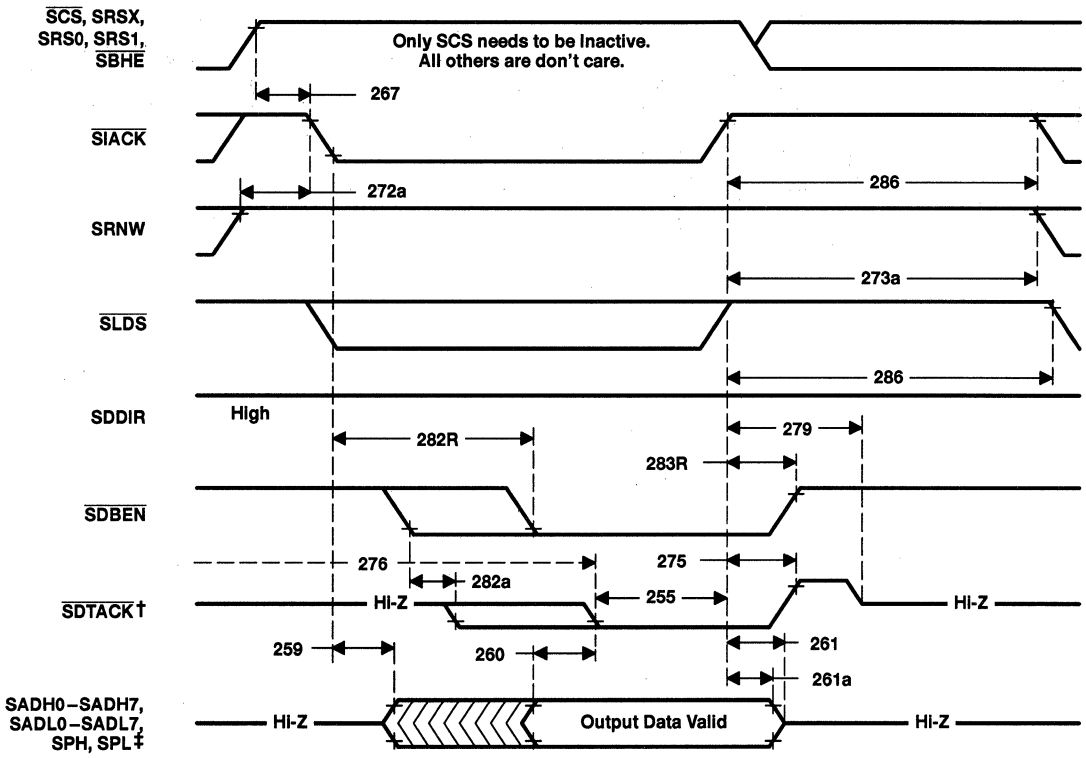
Figure 27. 68xxx DIO Write-Cycle Timing

68xxx interrupt-acknowledge-cycle timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
255	Delay time, $\overline{SDTACK}$ low to either $\overline{SCS}$ or $\overline{SUDS}$, or $\overline{SIACK}$ high	15		15		ns
259†	Hold time, SAD in the high-impedance state after $\overline{SIACK}$ no longer high (see Note 22)	0		0		ns
260	Setup time, output data valid before $\overline{SDTACK}$ no longer high	0		0		ns
261†	Delay time, $\overline{SIACK}$ high to SAD in the high-impedance state (see Note 22)		35		35	ns
261a	Hold time, output data valid after $\overline{SCS}$ or $\overline{SIACK}$ no longer low (see Note 22)	0		0		ns
267§	Setup time, register address before $\overline{SIACK}$ no longer high (see Note 22)	15		15		ns
272a	Setup time, inactive high $\overline{SIACK}$ to active data strobe no longer high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
273a	Hold time, inactive SRNW high after active data strobe high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
275	Delay time, $\overline{SCS}$ or $\overline{SRNW}$ high to $\overline{SDTACK}$ high (see Note 22)	0	25	0	25	ns
276‡	Delay time, $\overline{SDTACK}$ low in the first DIO access to the SIF register to $\overline{SDTACK}$ low in the immediately following access to the SIF	0	4000	0	4000	ns
279†	Delay time, $\overline{SIACK}$ high to $\overline{SDTACK}$ in the high-impedance state	0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
282a	Delay time, $\overline{SDBEN}$ low to $\overline{SDTACK}$ low in a read cycle	0	$t_{c(SCK)}/2 + 4$	0	$t_{c(SCK)}/2 + 4$	ns
282R	Delay time, $\overline{SIACK}$ low to $\overline{SDBEN}$ low (see *TMS380 Second Generation Token-Ring User's Guide,* SPWU005, subsection 3.4.1.1.1), provided the previous cycle completed	0	$t_{c(SCK)} + 3$	0	$t_{c(SCK)} + 3$	ns
283R	Delay time, $\overline{SIACK}$ high to $\overline{SDBEN}$ high (see Note 22)	0	$t_{c(SCK)}/2 + 4$	0	$t_{c(SCK)}/2 + 4$	ns
286	Pulse duration, $\overline{SIACK}$ high between DIO accesses (see Note 22)	$t_{c(SCK)}$		$t_{c(SCK)}$		ns

† This specification is provided as an aid to board design. It is not assured during manufacturing testing.
‡ This specification has been characterized to meet stated value. It is not assured during manufacturing testing.
§ It is the later of $\overline{SRD}$ and $\overline{SRD}$ or $\overline{SCS}$ low that indicates the start of the cycle.
NOTE 22: The inactive chip select is $\overline{SIACK}$ in DIO-read and DIO-write cycles, and $\overline{SCS}$ is the inactive chip select in interrupt-acknowledge cycles.

ADVANCE INFORMATION



† $\overline{\text{SDTACK}}$ is an active-low bus ready signal. It must be asserted before data output.
‡ Internal logic drives $\overline{\text{SDTACK}}$ high and verifies that it has reached a valid-high level before making it a 3-state signal.

Figure 28. 68xxx Interrupt-Acknowledge-Cycle Timing

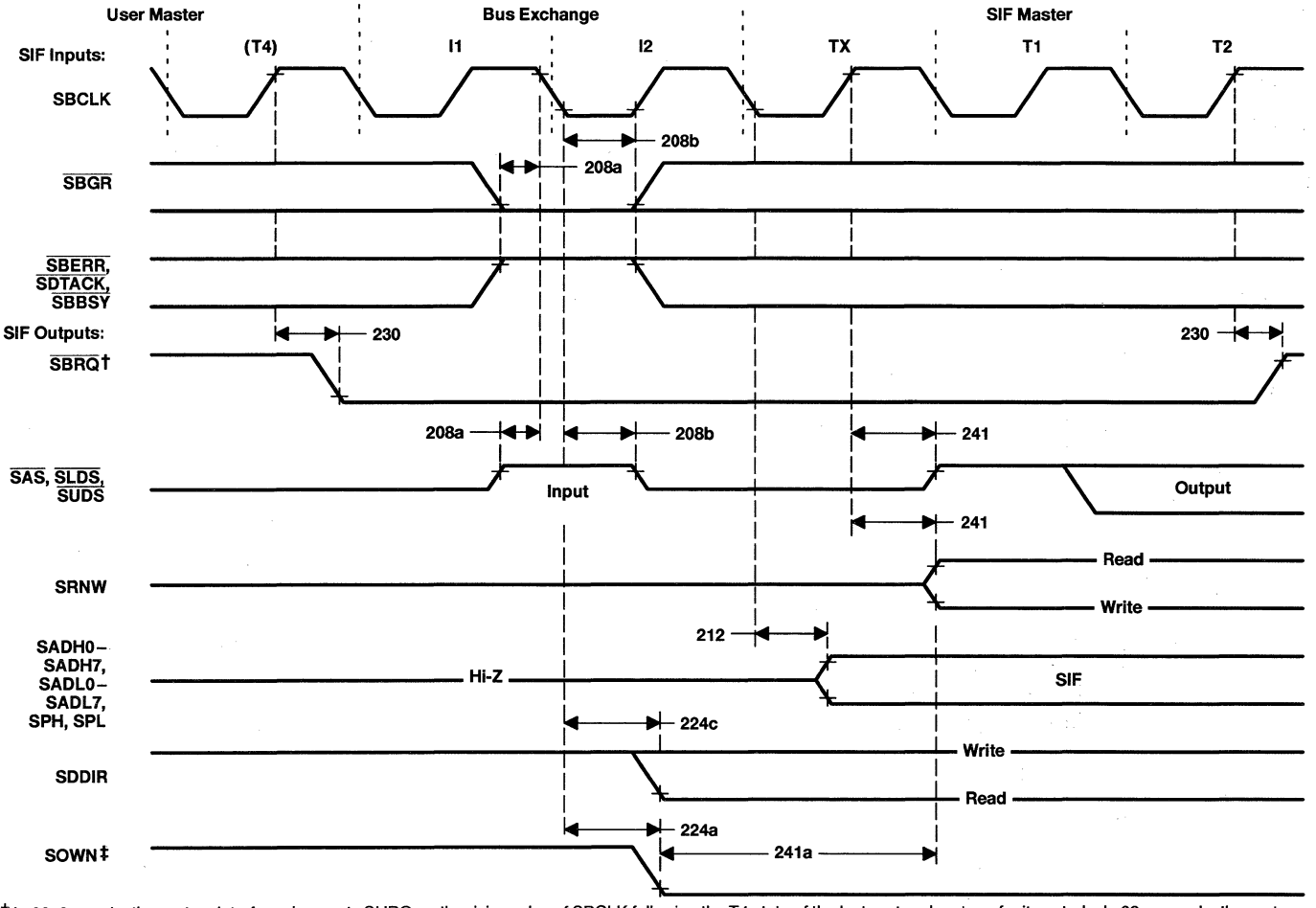
ADVANCE INFORMATION

68xxx-mode bus-arbitration timing, SIF takes control

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous input $\overline{\text{SBGR}}$ before SBCLK no longer high to assure recognition on this cycle	10		10		ns
208b	Hold time, asynchronous input $\overline{\text{SBGR}}$ after SBCLK low to assure recognition on this cycle	10		10		ns
212	Delay time, SBCLK low to address valid	0	20	0	20	ns
224a	Delay time, SBCLK low in cycle I2 to $\overline{\text{SOWN}}$ low (see Note 25)	0	20	0	15	ns
224c	Delay time, SBCLK low in cycle I2 to SDDIR low in DMA read		28		23	ns
230	Delay time, SBCLK high to either SHRQ low or $\overline{\text{SBRQ}}$ high		20		15	ns
241	Delay time, SBCLK high in TX cycle to $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$ high		25		25	ns
241a	Hold time, $\overline{\text{SUDS}}$, $\overline{\text{SLDS}}$, SRNW, and $\overline{\text{SAS}}$ in the high-impedance state after $\overline{\text{SOWN}}$ low, bus aquisition	$t_{c(SCK-15)}$		$t_{c(SCK-15)}$		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.
NOTE 25: Motorola-style bus slaves hold $\overline{\text{SDTACK}}$ active until the bus master deasserts $\overline{\text{SAS}}$.

ADVANCE INFORMATION



† In 80x8x mode, the system interface deasserts SHRQ on the rising edge of SBCLK following the T4 state of the last system-bus transfer it controls. In 68xxx mode, the system interface deasserts $\overline{\text{SBRQ}}$ on the rising edge of SBCLK in state T2 of the first system-bus transfer it controls.
‡ While the system-interface DMA controls are active (i.e., $\overline{\text{SOWN}}$ is asserted), the $\overline{\text{SCS}}$ input is disabled.

Figure 29. 68xxx-Mode Bus-Arbitration Timing, SIF Takes Control

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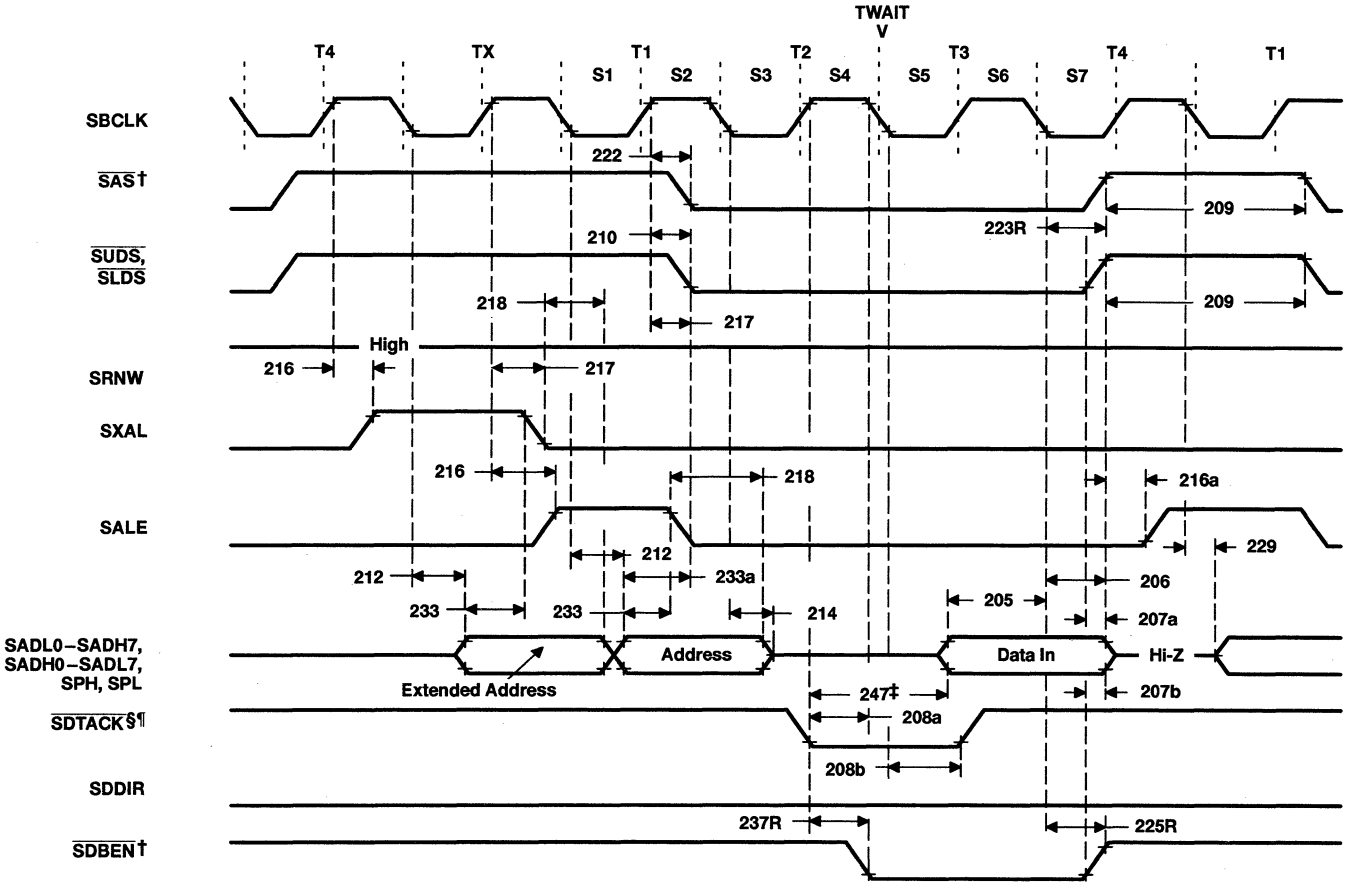
68xxx-mode DMA read-cycle timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
205	Setup time, input data valid before SBCLK in T3 cycle no longer high	10		10		ns
206	Hold time, input data valid after SBCLK low in T4 cycle if parameters 207a and 207b not met	10		10		ns
207a	Hold time, input data valid after data strobe no longer low	0		0		ns
207b	Hold time, input data valid after $\overline{\text{SDBEN}}$ no longer low	0		0		ns
208a	Setup time, asynchronous input $\overline{\text{SDTACK}}$ before SBCLK no longer high to assure recognition on this cycle	10		10		ns
208b	Hold time, asynchronous input $\overline{\text{SDTACK}}$ after SBCLK low to assure recognition on this cycle	10		10		ns
209	Pulse duration, $\overline{\text{SAS}}$, $\overline{\text{SUDS}}$, and $\overline{\text{SLDS}}$ high	$t_{c(SCK)}+t_{w(SCKL)}-18$		$t_{c(SCK)}+t_{w(SCKL)}-18$		ns
210	Delay time, SBCLK high in T2 cycle to $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$ active		16		11	ns
212	Delay time, SBCLK low to address valid		20		20	ns
214†	Delay time, SBCLK low in T2 cycle to SAD high impedance		20		15	ns
216	Delay time, SBCLK high to SALE or SXAL high		20		20	ns
216a	Hold time, SALE or SXAL low after $\overline{\text{SUDS}}$ and $\overline{\text{SAS}}$ high	0		0		ns
217	Delay time, SBCLK high to SXAL low in the TX cycle or SALE low in the T1 cycle	0	25	0	25	ns
218	Hold time, address valid after SALE, SXAL low	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	ns
222	Delay time, SBCLK high to $\overline{\text{SAS}}$ low		20		15	ns
223R	Delay time, SBCLK low in T4 cycle to $\overline{\text{SUDS}}$, $\overline{\text{SLDS}}$, and $\overline{\text{SAS}}$ high (see Note 24)	0	16	0	11	ns
225R	Delay time, SBCLK low in T4 cycle to $\overline{\text{SDBEN}}$ high		16		11	ns
229†	Hold time, SAD in the high-impedance state after SBCLK low in T4 cycle	0		0		ns
233	Setup time, address valid before SALE or SXAL no longer high	10		10		ns
233a	Setup time, address valid before $\overline{\text{SAS}}$ no longer high	$t_{w(SCKL)}-15$		$t_{w(SCKL)}-15$		ns
237R	Delay time, SBCLK high in the T2 cycle to $\overline{\text{SDBEN}}$ low		16		11	ns
247	Setup time, data valid before $\overline{\text{SDTACK}}$ low if parameter 208a not met	0		0		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.
NOTE 24: While the system-interface DMA controls are active (i.e., $\overline{\text{SOWN}}$ is asserted), $\overline{\text{SCS}}$ is disabled.

ADVANCE INFORMATION



† On a read cycle, the read strobe remains active until the internal sample of incoming data is completed. Input data may be removed when either the read strobe or $\overline{\text{SDBEN}}$ becomes no longer active.
‡ If parameter 208a is not met, then valid data must be present before $\overline{\text{SDTACK}}$ goes low.
§ Motorola-style bus slaves hold $\overline{\text{SDTACK}}$ active until the bus master deasserts $\overline{\text{SAS}}$.
¶ All V_{SS} pins should be routed to minimize inductance to system ground.

Figure 30. 68xxx-Mode DMA Read-Cycle Timing

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68xxx-mode DMA write-cycle timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous input $\overline{SDTACK}$ before SBCLK no longer high to assure recognition on this cycle	10		10		ns
208b	Hold time, asynchronous input $\overline{SDTACK}$ after SBCLK low to assure recognition on this cycle	10		10		ns
209	Pulse duration, $\overline{SAS}$, $\overline{SUDS}$, and $\overline{SLDS}$ high	$t_{c(SCK)}+t_{w(SCKL)}-18$		$t_{c(SCK)}+t_{w(SCKL)}-18$		ns
211	Delay time, SBCLK high in T2 cycle to $\overline{SUDS}$ and $\overline{SLDS}$ active		25		25	ns
211a	Delay time, output data valid to $\overline{SUDS}$ and $\overline{SLDS}$ no longer high	$t_{w(SCKL)}-15$		$t_{w(SCKL)}-15$		ns
212	Delay time, SBCLK low to address valid		20		20	ns
216	Delay time, SBCLK high to SALE or SXAL high		20		20	ns
216a	Hold time, SALE or SXAL low after $\overline{SUDS}$ and $\overline{SAS}$ high	0		0		ns
217	Delay time, SBCLK high to SXAL low in the TX cycle or SALE low in the T1 cycle	0	25	0	25	ns
218	Hold time, address valid after SALE, SXAL low	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	ns
219	Delay time, SBCLK low in T2 cycle to output data and parity valid		29		29	ns
221	Hold time, output data, parity valid after $\overline{SUDS}$ and $\overline{SLDS}$ high	$t_{c(SCK)}-12$		$t_{c(SCK)}-12$		ns
222	Delay time, SBCLK high to $\overline{SAS}$ low		20		15	ns
223W	Delay time, SBCLK low to $\overline{SUDS}$, $\overline{SLDS}$, and $\overline{SAS}$ high	0	16	0	11	ns
225W	Delay time, SBCLK high in T4 cycle to $\overline{SDBEN}$ high		16		11	ns
225WH	Hold time, $\overline{SDBEN}$ low after $\overline{SUDS}$ and $\overline{SLDS}$ high	$t_{c(SCK)}/2-7$		$t_{c(SCK)}/2-7$		ns
233	Setup time, address valid before SALE or SXAL no longer high	10		10		ns
233a	Setup time, address valid before $\overline{SAS}$ no longer high	$t_{w(SCKL)}-15$		$t_{w(SCKL)}-15$		ns
237W	Delay time, SBCLK high in T1 cycle to $\overline{SDBEN}$ low		16		11	ns

ADVANCE INFORMATION

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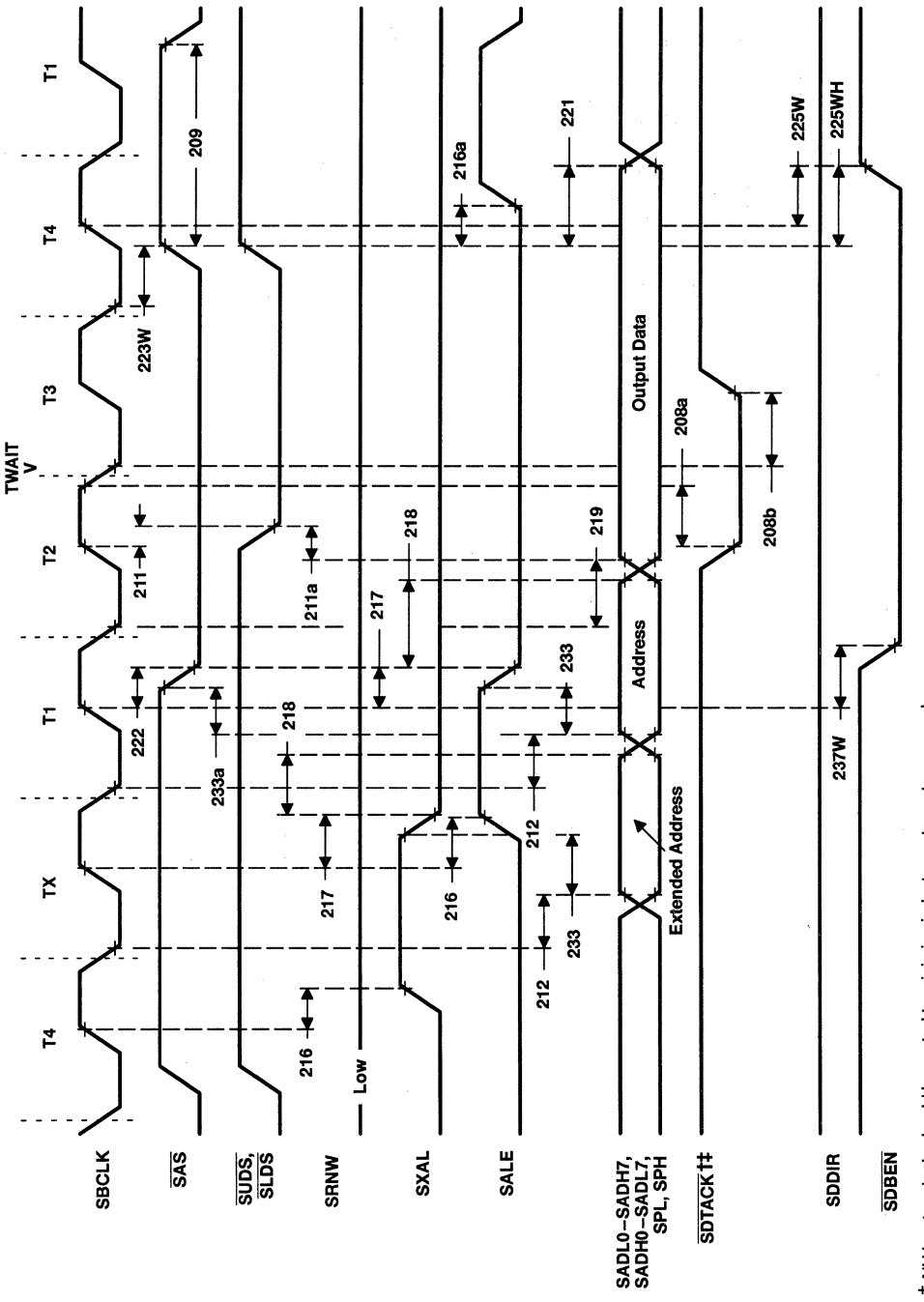


† All V_{SS} terminals should be routed to minimize inductance to system ground.
‡ On a read cycle, the read strobe remains active until the internal sample of incoming data is completed. Input data can be removed when either the read strobe or $\overline{SDBEN}$ becomes no longer active.

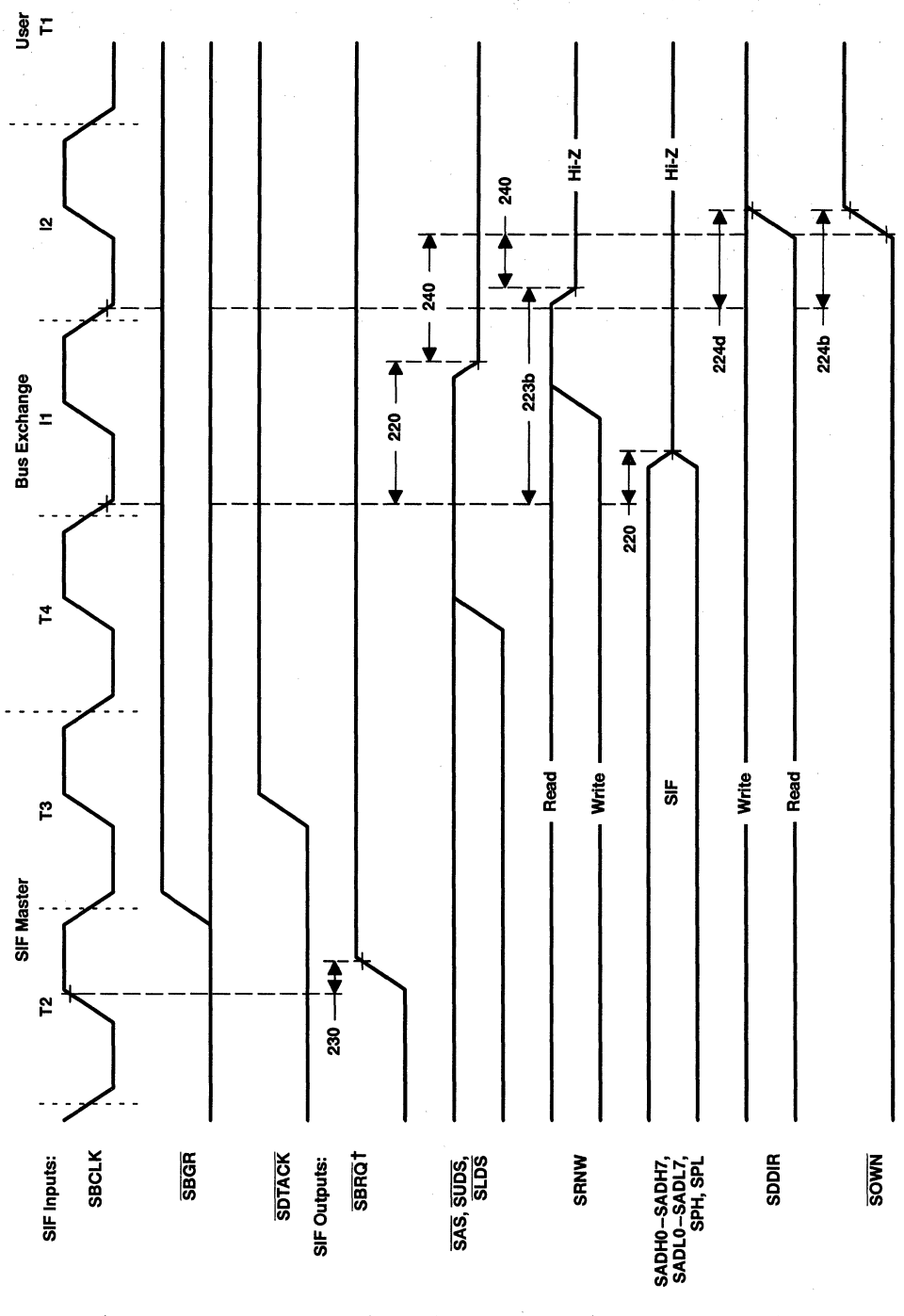
Figure 31. 68xxx-Mode DMA Write-Cycle Timing

68xxx-mode bus-arbitration timing, SIF returns control

NO.		25-MHz OPERATION		25-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
220†	Delay time, SBCLK low in I1 cycle to SAD, SPL, SPH, $\overline{\text{SUDS}}$, and $\overline{\text{SLDS}}$ in the high-impedance state, bus release		35		35	ns
223b†	Delay time, SBCLK low in I1 cycle to $\overline{\text{SBHE}}$/SRNW in the high-impedance state		45		45	ns
224b	Delay time, SBCLK low in cycle I2 to $\overline{\text{SOWN}}$ high	0	20	0	15	ns
224d	Delay time, SBCLK low in cycle I2 to SDDIR high		27		22	ns
230	Delay time, SBCLK high to either SHRQ low or $\overline{\text{SBRQ}}$ high		20		15	ns
240†	Setup from, $\overline{\text{SUDS}}$, $\overline{\text{SLDS}}$, SRNW, and $\overline{\text{SAS}}$ control signals in the high-impedance state before $\overline{\text{SOWN}}$ no longer low	0		0		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.

ADVANCE INFORMATION

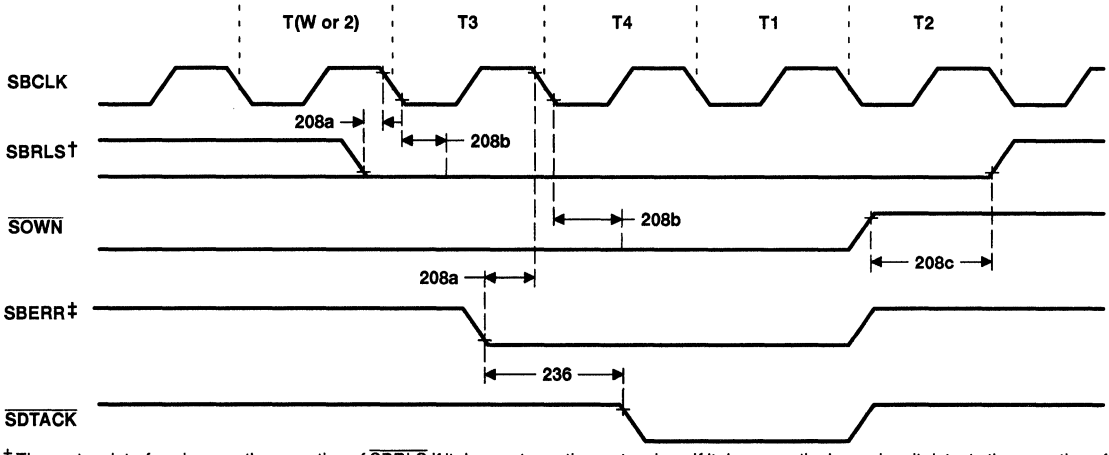


† In 80x8x mode, the system interface deasserts SHRQ on the rising edge of SBCLK following the T4 state of the last system-bus transfer it controls. In 68xxx mode, the system interface deasserts SBRQ on the rising edge of SBCLK in state T2 of the first system-bus transfer it controls.

Figure 32. 68xxx-Mode Bus-Arbitration Timing, SIF Returns Control

68xxx-mode bus-release and error timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous input before SBCLK no longer high to assure recognition	10		10		ns
208b	Hold time, asynchronous input $\overline{\text{SBRLS}}$, $\overline{\text{SOWN}}$, or $\overline{\text{SBERR}}$ after SBCLK low to assure recognition	10		10		ns
208c	Hold time, $\overline{\text{SBRLS}}$ low after $\overline{\text{SOWN}}$ high	0		0		ns
236	Setup time, $\overline{\text{SBERR}}$ low before $\overline{\text{SDTACK}}$ no longer high if parameter 208a not met	30		30		ns



† The system interface ignores the assertion of $\overline{\text{SBRLS}}$ if it does not own the system bus. If it does own the bus, when it detects the assertion of $\overline{\text{SBRLS}}$, it completes any internally-started DMA cycle and relinquishes control of the bus. If no DMA transfer has started internally, the system interface releases the bus before starting another.

‡ If $\overline{\text{SBERR}}$ is asserted when the system interface controls the system bus, the current bus transfer is completed, regardless of the value of $\overline{\text{SDTACK}}$. If the BERETRY register is nonzero, the cycle is retried. If the BERETRY register is zero, the system interface then releases control of the system bus. The system interface ignores the assertion of $\overline{\text{SBERR}}$ if it is not performing a DMA-bus cycle on the system bus. When $\overline{\text{SBERR}}$ is properly asserted and BERETRY is zero, however, the system interface releases the bus upon completion of the current bus transfer and halts all further DMA on the system side. The error is synchronized to the local bus and DMA stops on the local sides. The value of the SDMAADR, SDMADDRX, and SDMALEN registers in the system interface are not defined after a system-bus error.

Figure 33. 68xxx-Mode Bus-Release and Error Timing

ADVANCE INFORMATION

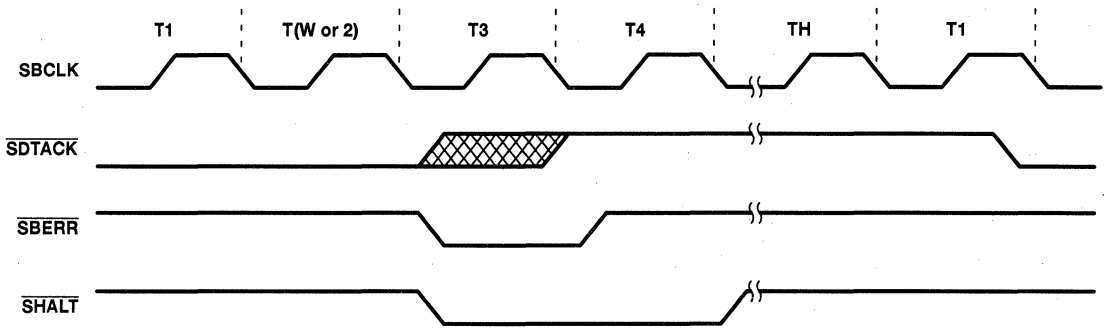


Figure 34. 68xxx-Mode Bus Halt and Retry, Normal Completion With Delayed Start†

† Only the relative placement of the edges to SBCLK falling edge is shown. Actual signal edge placement can vary from waveforms shown.

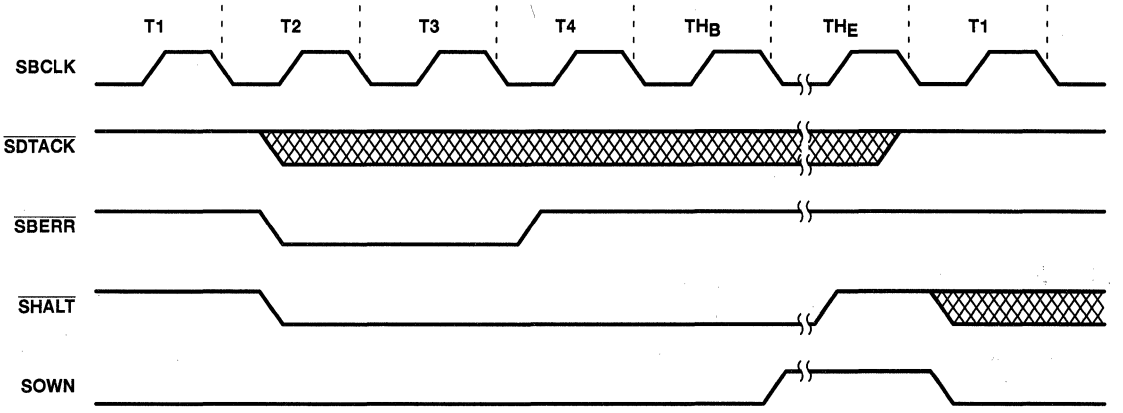
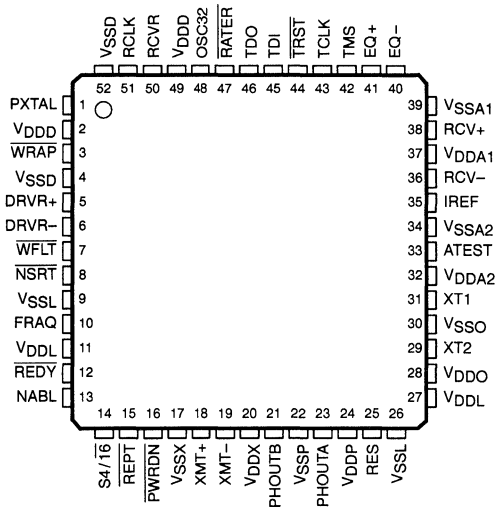


Figure 35. 68xxx-Mode Bus Halt and Retry, Rerun Cycle With Delayed Start†

† Only the relative placement of the edges to SBCLK falling edge is shown. Actual signal edge placement can vary from waveforms shown.

- **Facilitates Connection of the TI380C25, TI380C26, or TI380C27 to Token Ring**
- **Loop Back (Wrap Mode) for Self-Test Diagnostics**
- **Compatible With Electrical Interface of ISO/IEC IEEE Std. 802.5:1992 Token-Ring Access-Method and Physical-Layer Specifications**
- **Glueless Interface to TI380C2x Commprocessor for Token Ring**
- **16- and 4-Mbps Token-Ring Data Rates With No External Switching Circuits**
- **Repeater Application Requires No Additional Active Components**
- **Digital Phase-Locked Loop**
  - **Precise Control of Bandwidths**
  - **Improved Jitter Tolerance**
  - **Minimizes Accumulated Phase Slope**
- **Phantom Drive for Physical Insertion Onto Ring**
- **Differential Line Receiver With Level-Dependent Frequency Equalization**
- **Low-Impedance Differential Line Driver to Ease Transmit-Filter Design**
- **Internal Crystal Oscillator for Reference-Clock Generation**
- **On-Chip Watchdog Timer**
- **Low-Power EPIC™ 0.8-μm CMOS Process**
- **PCMCIA-Compatible 52-Lead 1,0-mm Plastic Quad Flatpack**

PAH PACKAGE
(TOP VIEW)



description

The TI380C60 token-ring interface device is a full-duplex electrical interface compatible with ISO/IEC IEEE Standard 802.5:1992 token-ring access-method and physical-layer specifications. The TI380C60 operates at the IEEE-standard 4- and 16-Mbps data rates. The Manchester-encoded data stream is received and phase aligned using an on-chip phase-locked loop (PLL). Both the recovered clock and data are passed to the protocol-handling circuits of one of the TI380C2x single-chip token-ring commprocessors for serial-to-parallel conversion and data processing. On transmit, the TI380C60 buffers the output of the TI380C2x and drives the media via suitable isolation and waveform-shaping components.

All necessary functions required to interface to an IEEE-802.5 token ring are provided. These include the PLL, the phantom drive to control the relays within a trunk-coupling unit, and wire-fault detection circuits. An internal wrap function is provided for self test, and a watchdog timer is included to provide fail-safe deinsertion from the ring in the event of a station microcode or commprocessor failure.

The TI380C60, when coupled with one of the TI380C2x token-ring commprocessors, forms a highly integrated token-ring LAN adapter compatible with the ISO/IEEE Standard 802.5. The TI380C60 synthesizes the necessary token-ring reference clock for its own use and for the TI380C2x. This removes the need for external components to provide this function.

The TI380C60 can function as a standalone device because the digital PLL is self contained and requires no additional circuits for frequency management. Using the device in this manner in the repeat mode provides a highly integrated token-ring repeater with no additional active components suitable for wiring center applications.

The TI380C60 is available in a 52-lead 1,0-mm plastic quad flatpack and is characterized for operation from 0°C to 70°C with a typical power dissipation of 600 mW.

EPIC is a trademark of Texas Instruments Incorporated.

Pin Functions

PIN NAME	PIN NO.	I/O/E†	TYPE‡	DESCRIPTION
ATEST	33	E	N	Analog test. Should be left unconnected.
DRVR+ DRVR–	5 6	I I	D D	Differential driver data inputs. DRVR+ and DRVR– receive the '380C2x transmit data.
EQ+ EQ–	41 40	E E	N N	Equalization/gain points. Connections to allow frequency tuning of equalization circuit.
FRAQ	10	I	TTL	Frequency acquisition control. FRAQ is driven by the '380C2x or can be tied low for repeater applications. H = Clock recovery PLL is initialized. L = Normal operation
IREF	35	E	N	Internal reference. IREF allows the internal bias current of analog circuitry to be set via an external resistor.
NABL	13	I	TTL	Output-enable control. NABL can be used in token-ring / ethernet applications to disable the token-ring function. H = TI380C60 operates normally L = All outputs are driven to the high-impedance state, except XMT+/XMT– which are driven low. Internal logic continues to operate unless $\overline{\text{PWRDN}}$ is asserted low.
$\overline{\text{NSRT}}$	8	I	TTL	Insert control. $\overline{\text{NSRT}}$ enables the phantom-driver outputs (PHOUTA and PHOUTB) through the watchdog timer for insertion onto the token ring. Static high = Inactive, phantom current removed (due to watchdog timer) Static low = Inactive, phantom current removed (due to watchdog timer) Falling edge = Active, current output on PHOUTA and PHOUTB.
PHOUTA PHOUTB	23 21	O O	N N	Phantom-driver outputs A and B. The outputs that cause insertion onto the token ring. PHOUTA and PHOUTB should be connected to the center tap of the transmit transformer secondary winding for phantom-drive generation.
$\overline{\text{PWRDN}}$	16	I	TTL	Power-down control H = Normal operation L = TI380C60 is placed into a power-down state. All TTL outputs are driven to the high-impedance state.
PXTAL	1	O	TTL	Token-ring reference-clock output. For 16-Mbps operation, PXTAL is a 16-MHz clock, and for 4-Mbps operation, PXTAL is an 8-MHz clock.
OSC32	48	O	TTL	Oscillator output. OSC32 provides a 32-MHz clock output and can be used to drive CLKIN of a TI380C2x.
$\overline{\text{REPT}}$	15	I	TTL	Repeat-mode enable L = Repeat mode selected. The received and sampled data present on RCVR is also driven out on the XMT+/XMT– pair. This function is overridden if $\overline{\text{WRAP}}$ is asserted low. H = TI380C60 operates normally
$\overline{\text{RATER}}$	47	O	TTL	Rate error. $\overline{\text{RATER}}$ indicates that there are transitions on RCV+/RCV– input pair (DRVR+/DRVR– if $\overline{\text{WRAP}}$ is asserted low) but that the transition rate is not consistent with the ring speed selected by S4/$\overline{16}$.
RCLK	51	O	TTL	Recovered clock. RCLK is the clock recovered from the token-ring received data. For 16-Mbps operation, it is a 32-MHz clock. For 4-Mbps operation, it is an 8-MHz clock.
RCV+ RCV–	38 36	I I	D D	Receiver inputs. RCV+ and RCV– receive the token-ring data via isolation transformers.
RCVR	50	O	TTL	Recovered data. RCVR contains the data recovered from the token ring and should be sampled at the rising edge of RCLK.

† I = input, O = output, E = provides external-component connection to the internal circuitry for tuning
‡ TTL = TTL signal, N = non-TTL signal, D = differential drive or data

Pin Functions

PIN NAME	PIN NO.	I/O/E†	TYPE‡	DESCRIPTION
$\overline{\text{REDY}}$	12	O	TTL	PLL ready. $\overline{\text{REDY}}$ is normally asserted (active) low. $\overline{\text{REDY}}$ is cleared following the assertion of FRAQ and reasserted after the data recovery PLL has been reinitialized. H = Received data not valid L = Received data valid
RES	25	—	—	Reserved. Should be left unconnected.
S4/$\overline{16}$	14	I	TTL	Speed switch. S4/$\overline{16}$ specifies the token-ring data rate. H = 4-Mbps data rate L = 16-Mbps data rate
TCLK TMS TDI TDO	43 42 45 46	I I I O	TTL	Test ports used during the production test of the device. Should be left unconnected.
$\overline{\text{TRST}}$	44	I	TTL	Test-port reset. $\overline{\text{TRST}}$ should be tied to ground for normal operation of the TI380C60. H = Reserved L = Test ports forced to an idle state
$\overline{\text{WFLT}}$	7	O	TTL	Phantom-wire fault. $\overline{\text{WFLT}}$ provides an indication of the presence of a short or open circuit on PHOUTA or PHOUTB. H = No fault L = Open or short. The dc fault condition is present in the phantom-drive lines.
$\overline{\text{WRAP}}$	3	I	TTL	Internal wrap-mode control. $\overline{\text{WRAP}}$ allows the TI380C60 to be placed in the loopback-wrap mode for adapter self test. H = Normal ring operation L = Transmit data drives the receive data. RCV+ or RCV– are ignored by the TI380C60 and XMT+ and XMT– are both forced low.
XMT+ XMT–	18 19	E	D	Transmit differential outputs XMT+ and XMT– provide a low-impedance differential source for line drive via filtering and transformer isolation.
XT1 XT2	31 29	E	N/TTL N	XTAL connection. An 8-MHz crystal network can be connected here to provide a reference clock for the TI380C60. Alternatively, an 8-MHz TTL clock source can be connected to XT1.
V_{DDA1}	37	—	—	Positive-supply voltage for receiver circuits
V_{DDD}	2, 49	—	—	Positive-supply voltage for output buffers
V_{DDL}	11, 27	—	—	Positive-supply voltage for internal logic
V_{DDA2}	32	—	—	Positive-supply voltage for data recovery PLL
V_{DDO}	28	—	—	Positive-supply voltage for XTAL oscillator
V_{DDP}	24	—	—	Positive-supply voltage for phantom drive
V_{DDX}	20	—	—	Positive-supply voltage for transmit output
V_{SSA1}	39	—	—	Ground reference for receiver circuits
V_{SSA2}	34	—	—	Ground reference for data recovery PLL
V_{SSD}	4, 52	—	—	Ground reference for output buffers
V_{SSL}	9, 26	—	—	Ground reference for internal logic
V_{SSX}	17	—	—	Ground reference for transmit output
V_{SSO}	30	—	—	Ground reference for XTAL oscillator
V_{SSP}	22	—	—	Ground reference for phantom drive

† I = input, O = output, E = provides external-component connection to the internal circuitry for tuning
‡ TTL = TTL signal, N = non-TTL signal, D = differential drive or data

architecture

The major blocks of the TI380C60 include the receiver/equalizer, clock recovery PLL, wrap function, phantom drive with wire-fault detector, and watchdog timer. Figure 1 is the block diagram illustrating these major blocks, and the functionality of each block is described in the following sections.

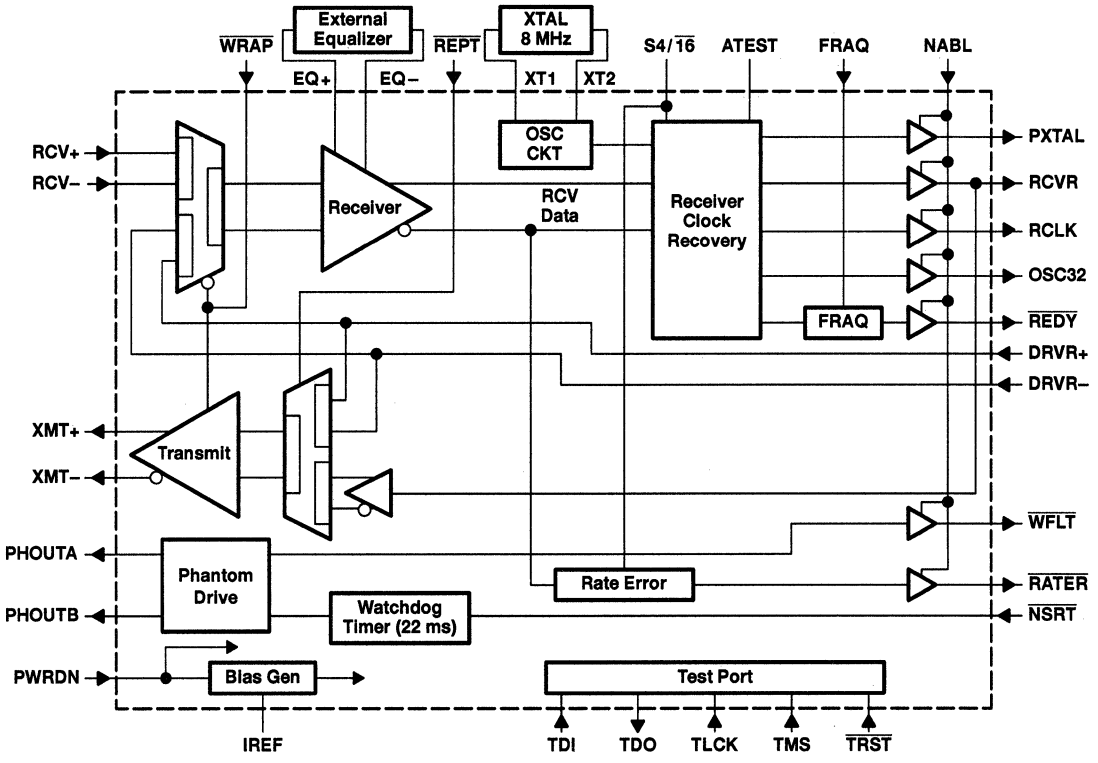


Figure 1. Functional Block Diagram

receiver

Figure 2 shows the arrangement of the line-receiver/equalizer circuit. The differential-input pair, RCV+ and RCV–, are designed to be connected to a floating winding of an isolation transformer. Each is equipped with a bias circuit to center the operating point of the differential input at approximately $V_{DD} \div 2$.

The differential-input pair consists of a pair of MOSFETs, each with an identical current source in its source pin that is set to supply a nominal current of 1.5 mA. At low signal levels, the gain of this pair is inversely proportional to the impedance connected between their sources on EQ– and EQ+. A frequency-equalization network can be connected between EQ+ and EQ– to provide equalization for media signal distortion.

The internal wrap mode is provided for self test of the device. When selected by taking $\overline{\text{WRAP}}$ low, the normal input path is disabled by a multiplexer and a path is enabled from DRVR+/DRVR– pair. Receiver gain, thresholds, and equalization are unchanged in the internal wrap mode.

receiver (continued)

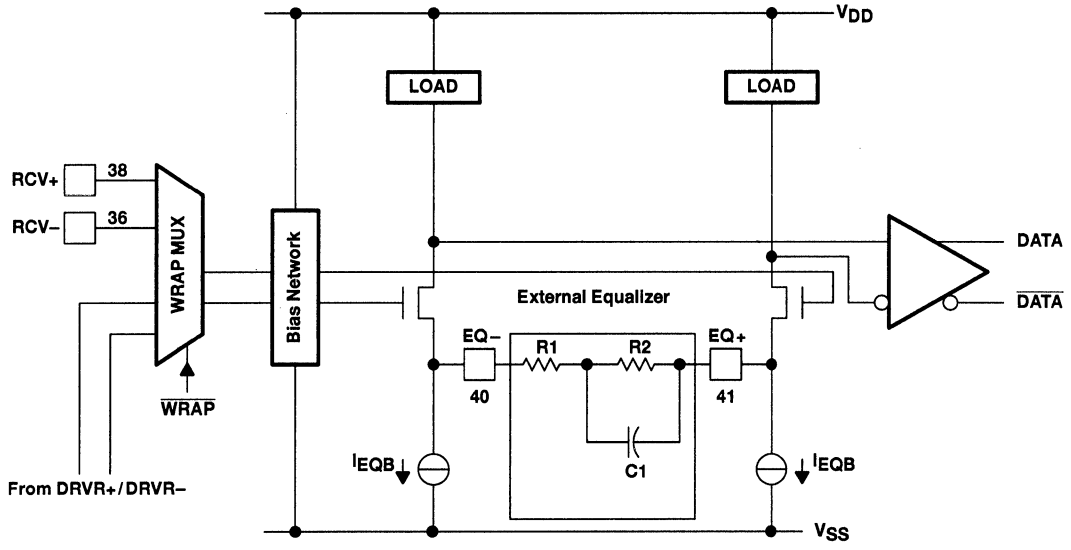
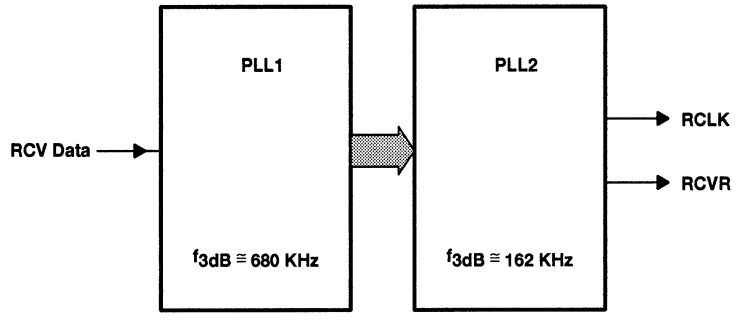


Figure 2. Line Receiver/Equalizer

receiver-clock recovery

The clock and data recovery in TI380C60 is performed by an advanced, digitally controlled phase-locked loop. In contrast to the TMS38054, the PLL of the TI380C60 is digitally controlled and the loop parameters are set by internally programmed digital constants. This results in precise control of loop parameters and requires no external loop-filter components.

The TI380C60 implements an intelligent algorithm to determine the optimum phase position for data sampling and extracted clock synthesis. The resulting action of the TI380C60 can be modeled as two cascaded PLLs as shown in Figure 3.



NOTE: f_{3dB} = –3dB bandwidth of PLL

Figure 3. Dual PLL Arrangement

receiver-clock recovery (continued)

PLL1 represents the algorithm to recover data from the incoming stream detected by the receiver. It has a relatively high bandwidth to provide good jitter tolerance. Data and embedded clock phase information are fed as digital values to PLL2 that generates the extracted clock (RCLK) for the TI380C2x commprocessor. The recovered data is sent to the TI380C2x as the RCVR signal synchronously with RCLK. In addition to sampling the RCVR signal, the TI380C2x uses RCLK to retransmit data in most cases. The lower bandwidth of PLL2 greatly reduces the rate of accumulation of data-correlated phase jitter in a token-ring network and provides very good accumulated-phase-slope (APS) characteristics. In addition to RCLK, the token-ring reference clock (PXTAL) and a fixed-frequency 32-MHz clock (OSC32) are also synthesized from the 8-MHz crystal reference.

line driver, wrap function, and repeat mode

The line-drive function of the TI380C60 is performed by XMT+ and XMT–. Unlike the TMS38054, these pins are low-impedance outputs and require external series resistance to provide line termination. These pins provide buffering of the differential signal from the TI380C2x on DRVR+/DRVR– with action to control skew and asymmetry and with no retiming in the transmit path.

The wrap function is designed to provide a signal path for system self-test diagnostics. When $\overline{\text{WRAP}}$ is taken low, the receiver inputs are ignored and the transmit signal is fed to the receiver input circuitry via a multiplexer. In the internal wrap mode, $\overline{\text{WRAP}}$ can be checked by observing the signal amplitude at the equalization pins, EQ+ and EQ–. Equalization is active at this signal level, although the signal does not exhibit the high-frequency attenuation effects for which equalization is intended to compensate. During internal wrap mode, both XMT+ and XMT– are driven to a low state to prevent any dc current flowing in the isolation transformer.

When the repeat function is selected, the sampled and retimed ring data present on RCVR is also driven out on XMT+ and XMT–. This allows the TI380C60 to operate as a standalone repeater. Both RCVR and RCLK continue to provide valid sampled ring data and extracted clock as normal. The DRVR+/DRVR– inputs are ignored. The repeat function is enabled by taking $\overline{\text{REPT}}$ low while holding $\overline{\text{WRAP}}$ high.

phantom driver and wire-fault detection

The phantom-drive circuit under control of $\overline{\text{NSRT}}$ generates a dc voltage on both of the phantom-drive outputs, PHOUTA and PHOUTB. In order to maintain the phantom drive, $\overline{\text{NSRT}}$ is toggled by the TI380C2x at least once every 20 ms. An internal watchdog timer is included in the TI380C60 to remove the phantom drive if $\overline{\text{NSRT}}$ fails to have the required transitions.

The watchdog timer is normally not allowed to expire because it is being reinitialized at least every 20 ms. If, there is a problem in the TI380C2x or its microcode resulting in failure to toggle $\overline{\text{NSRT}}$, the timer expires in a maximum of 22 ms. If this happens, the phantom drive is deasserted and remains so until the next falling edge of $\overline{\text{NSRT}}$. The watchdog timer requires no external timing components. When the phantom drive is deasserted, the phantom-drive lines are actively pulled low, reaching a level of 1 V or less within 50 ms.

The dc voltage from PHOUTA and PHOUTB is superimposed on the transmit-signal pair to the trunk-coupling unit (TCU) to request that the station be inserted into the ring. This is achieved by connecting them to the center of the secondary winding of the transmit-isolation transformer. Since PHOUTA and PHOUTB are connected to the media side of the isolation transformer, they require extensive protection against line surges. A capacitor is connected between the two phantom lines to provide an ac path for the transmit signal. PHOUTA and PHOUTB independently drive the dc voltage on each of the transmit lines allowing for independent wire-fault detection on each.

The phantom voltage is detected by the TCU, causing the external wrap path from the transmitter outputs back to the receiver inputs to be broken and the ring to be broken. A signal connection is then established from the ring to the receiver inputs and from the transmitter outputs to the ring. The return current from the dc-phantom voltage on the transmit pair is returned to the station via the receive pair. This provides some measure of wire-fault detection on the receive lines. The phantom-drive outputs are current limited to prevent damage if

short circuited. They detect either an abnormally high or an abnormally low load current at either output, corresponding to a short or an open circuit in the ring or TCU wiring. Either fault causes the wire-fault indicator output, $\overline{\text{WFLT}}$, to be driven low. The logic state of $\overline{\text{WFLT}}$ is high when the phantom drive is not active.

frequency acquisition and $\overline{\text{REDY}}$

Unlike its predecessors, the TMS3805x family, the data-recovery PLL of the TI380C60 does not require constant frequency monitoring; neither is it necessary to recenter its frequency via the FRAQ control line. However, it is necessary to provide the interaction with the TI380C2x or other commprocessors that expect to perform this frequency-management task.

When the TI380C2x asserts FRAQ, it initiates a reset of the clock-recovery PLL. The $\overline{\text{REDY}}$ signal is deasserted for the duration of this action and reasserted low when it is complete (a maximum of 3 µs later). This low-going transition of $\overline{\text{REDY}}$ is required by the TI380C2x following the setting of FRAQ high to indicate to the commprocessor that any frequency error that it detected has been corrected. In fact, the TI380C60 will never require FRAQ to be asserted after the PLL has been initialized. This interaction is provided purely for the benefit of the TI380C2x.

rate error ($\overline{\text{RATER}}$) function

$\overline{\text{RATER}}$ provides an indication that incoming data transitions are present on the RCV+/RCV– pair but that the rate of transitions is outside the range that would be expected for the ring speed selected by S4/$\overline{16}$. $\overline{\text{RATER}}$ is not asserted low if no incoming transitions are present. In wrap mode, the rate-error function monitors the transitions on the DRVR+/DRVR– pair.

The rate-error function interprets 16 or more transitions in a 1.5-µs period as valid 16-Mbps data. It interprets 15 or less transitions in a 1.5-µs period as 4-Mbps data. One transition or less in a 1.5-µs period is interpreted as no incoming transitions.

disable and power-down mode

The TI380C60 can be disabled by either NABL or $\overline{\text{PWRDN}}$. If NABL is taken low, the output buffers of the commproccessor interface are placed in the high-impedance state; however, internal logic continues to operate. Phantom drive is disabled, but XMT+ and XMT– are driven to a low value to sustain line termination in token-ring/Ethernet™ 10-base-T applications that share magnetics.

If $\overline{\text{PWRDN}}$ is taken low, all outputs are in the high-impedance state and all internal logic is powered down, bringing power consumption to a very low level. Upon removing $\overline{\text{PWRDN}}$, the device resets and initializes itself. This process can take up to 2 ms and care should be taken to ensure that the system does not require stable clocks during this period. In particular, slow-clock errors can be seen by a TI380C2x commprocessor in a dual-physical-layer application if the TI380C60 is powered down when not in use.

test facilities

A 5-pin test port is included for production-device testing. While the signals are compatible with IEEE-1149.1, this port is not compliant with the standard and the port is not suitable for in-circuit test.

ATEST gives access to the filter of the internal PLL. This pin is also for production test purposes, and no connection should be made to it in an application.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) ..... – 0.5 V to 7 V
Input voltage range (see Notes 1 and 2) ..... – 0.5 V to 7 V
Output voltage range ..... – 0.5 V to 7 V
Power dissipation (see Note 3) ..... 0.75 W
Operating free-air temperature range ..... 0°C to 70°C
Maximum case temperature ..... 95°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to V_{SS} unless otherwise noted.
2. Inputs can be taken to more negative voltages if the current is limited to 20 mA.
3. Maximum power dissipation per package

recommended operating conditions‡

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	All V_{DD}	4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 4)	TTL inputs	2		V_{DD} + 0.3	V
V_{IL}	Low-level input voltage (see Notes 4 and 5)	TTL inputs	– 0.3		0.8	V
V_{IB}	Receiver input bias voltage	See Note 6	V_{SB} – 1		V_{SB} + 1	V
I_{OH}	High-level output current (see Note 4)	TTL outputs			– 0.2	mA
I_{OL}	Low-level output current (see Note 4)	TTL outputs			2	mA
T_A	Operating free-air temperature		0		70	°C

‡ Recommended operating conditions indicate the conditions that must be met to ensure that the device functions as intended and meets the detailed electrical specifications. Unless otherwise noted, all electrical specifications apply for all recommended operating conditions. Voltages are measured with respect to the device V_{SS} pins. Currents into the device are considered to be positive.

NOTES: 4. The TTL input and TTL output pins are the pins listed as commprocessor interface or test port in the pin functions table. This section also identifies them as inputs and outputs.
5. Inputs can be taken to more negative voltages if the I_{DD} current is limited to 20 mA.
6. V_{SB} is the self-bias voltage of the input pair RCV+ and RCV–. It is defined as $V_{SB} = (V_{SB+} + V_{SB-}) \div 2$ (where V_{SB+} is the self-bias voltage of RCV+; V_{SB-} is the self-bias voltage of RCV–). The self-bias voltage of both pins is approximately $V_{DD} \div 2$.

TTL input and output pins (see Note 4)

PARAMETER			TEST CONDITIONS§	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current		$V_I = V_{DD}$	– 20		20	µA
I_{IL}	Low-level input current		$V_I = 0$ V	– 20		20	µA
V_{OH}	High-level output voltage		$I_{OH} = – 0.2$ mA	2.6			V
V_{OL}	Low-level output voltage		$I_{OL} = 2$ mA			0.45	V
I_{OZH}	Off-state output current with high-level voltage applied		$V_O = 2.7$ V	– 20		20	µA
I_{OZL}	Off-state output current with low-level voltage applied		$V_O = 0.4$ V	– 20		20	µA
I_{DD}	Supply current	Normal mode	V_{DD} = MAX		120		mA
		Power-down mode			10		mA

§ For conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

NOTE 4: The TTL input and TTL output pins are the pins listed as commprocessor interface or test port in the pin functions table. This section also identifies them as inputs and outputs.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

receiver input (RCV+ and RCV–)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	$V_{ICM} = V_{SB}$, See Notes 6 and 7, and Figure 6		50	mV
V_{IT-}	Negative-going input threshold voltage	$V_{ICM} = V_{SB}$, See Notes 6 and 7, and Figure 6	– 50		mV
V_{hys}	Hysteresis asymmetry threshold voltage, (V_{T+} + V_{T-})	$V_{ICM} = V_{SB}$, See Notes 6 and 7, and Figure 6	– 20	20	mV
CMRR	Common-mode rejection ratio	See Notes 6 and 7, and Figure 6	– 30	30	mV
$I_{I(RCV)}$	Receiver input current	Both inputs at V_{SB}, See Note 6 and Figure 6	– 10	10	µA
		Input under test at V_{SB} + 1 V, Other input at V_{SB} – 1 V, See Note 6 and Figure 6	15	60	
		Input under test at V_{SB} – 1 V, Other input at V_{SB} + 1 V, See Note 7 and Figure 6	–15	–60	
$I_{IB(EQ)}$	Input bias current, equalizer	EQ+ and EQ– biased at V_{DD} – 3 V RCV+ and RCV– at V_{DD} – 3 V, See Figure 6	1.2	1.8	mA
	Equalizer wrap voltage	$\overline{WRAP}$ = low, See Figure 6	300	700	mV

NOTES: 6. V_{SB} is the self-bias voltage of the input pair RCV+ and RCV–. It is defined as $V_{SB} = (V_{SB+} + V_{SB-}) \div 2$ (where V_{SB+} is the self-bias voltage of RCV+; V_{SB-} is the self-bias voltage of RCV–). The self-bias voltage of both pins is approximately $V_{DD} \div 2$.

7. V_{ICM} is the common-mode voltage applied to RCV+ and RCV–.

phantom driver (PHOUTA and PHOUTB)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -1$ mA	4.1		V
		$I_{OH} = -2$ mA	3.8		V
I_{OS}	Short-circuit output current	$V_O = 0$ V	– 4	– 20	mA
I_{OL}	Low-level output current	$V_O = V_{DD}$	– 1	– 10	mA
I_{OZH}	Off-state output current with high-level voltage applied	$V_O = V_{DD}$	– 100	100	µA
I_{OZL}	Off-state output current with low-level voltage applied	$V_O = 0$ V	– 100	100	µA

wire fault ($\overline{WFLT}$) (see Notes 8 and 9)

PARAMETER		MIN	MAX	UNIT
$R_{L(S)}$	Phantom-drive load resistance detected as short circuit		0.15	kΩ
$R_{L(O)}$	Phantom-drive load resistance detected as open circuit	50		kΩ
$R_{L(N)}$	Phantom-drive load resistance detected as normal	2.9	5.5	kΩ

NOTES: 8. The wire-fault circuit recognizes a fault condition for any phantom-drive load resistance to ground greater than $R_{L(O)}$ or any load resistance less than $R_{L(S)}$. Any resistance in the range specified for $R_{L(N)}$ is not recognized as a wire fault. A fault condition on either PHOUTA or PHOUTB results in $\overline{WFLT}$ being asserted (low).

9. Resistor [$R_{L(S)}$, $R_{L(O)}$, $R_{L(N)}$] connected from output under test to ground, other output loaded with 4.1 Ω to ground.

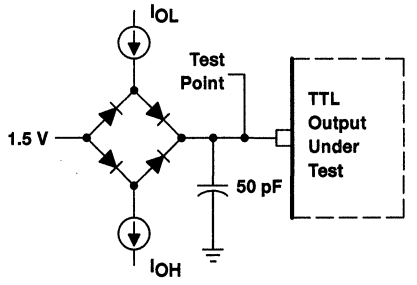
electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PLL characteristics

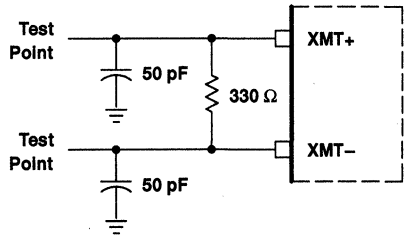
PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Reference PLL operating filter voltage	$t_{c(XT1)}$ = 125 ns	1.8	4	V

crystal-oscillator characteristics

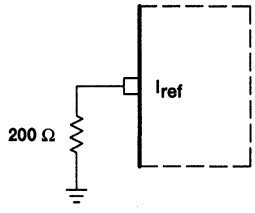
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{IB(XT1)}$	Input self-bias voltage		1.8	4	V
$I_{OH(XT2)}$	High-level output current	$V_{(XT2)} = V_{SB(XT1)}$ $V_{(XT1)} = V_{SB(XT1)} + 0.5$ V	– 2.5	– 6.5	mA
$I_{OL(XT2)}$	Low-level output current	$V_{(XT2)} = V_{SB(XT1)}$ $V_{(XT1)} = V_{SB(XT1)} – 0.5$ V	0.4	1.3	mA



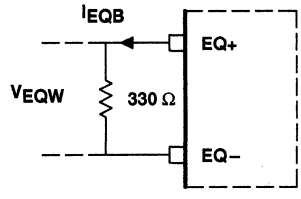
(a) TTL-OUTPUT TEST LOAD



(b) XMT+ and XMT– TEST LOAD



(c) I_{ref} TEST CIRCUIT



(d) EQUALIZER TEST CIRCUIT

Figure 4. Test and Load Circuits

switching characteristics over recommended range of supply voltage (unless otherwise noted)

transmitter-drive characteristics

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{N(PP)}$ XMT+/XMT– peak-to-peak voltage (see Note 10)	V_{DD} = 4.75 V, See Figures 4 and 5	8.2		V
	V_{DD} = 5.25 V, See Figures 4 and 5		10.3	

NOTE 10: $V_{N(PP)}$ is determined by:
$V_{OH(XMT+)} + V_{OH(XMT-)} - V_{OL(XMT+)} - V_{OL(XMT-)}$

transmitter switching characteristics (see Figures 4 and 5)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
XMT+/XMT– skew (see Note 11)	$t_{sk(DRV)}$ = – 1 ns	– 3	+ 3	ns
	$t_{sk(DRV)}$ = + 1 ns	– 3	+ 3	ns
XMT+/XMT– asymmetry (see Note 12)	$t_{sk(DRV)}$ = – 1 ns	– 2	+ 2	ns
	$t_{sk(DRV)}$ = + 1 ns	– 2	+ 2	ns

NOTES: 11. XMT+/XMT– skew is determined by: $t_{d(XMT+\,H)} - t_{d(XMT-\,L)}$ or $t_{d(XMT+\,L)} - t_{d(XMT-\,H)}$

12. XMT+/XMT– asymmetry is determined by:

$$\frac{t_{d(XMT+L)} + t_{d(XMT-H)}}{2} - \frac{t_{d(XMT+H)} + t_{d(XMT-L)}}{2}$$

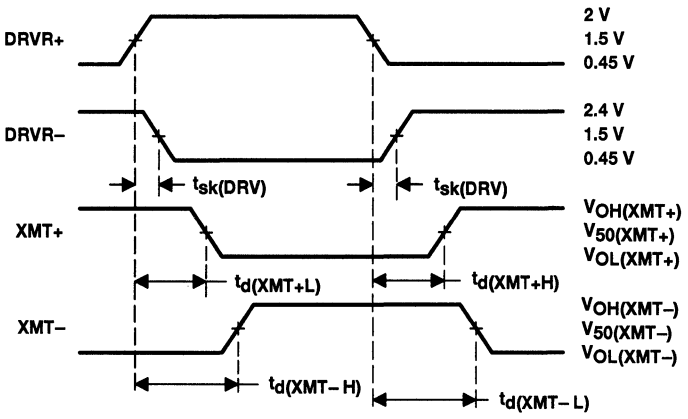


Figure 5. Transmitter Timing

timing requirements over recommended range of supply voltage, $t_{c(XT1)}$ = 125 ns (see Figure 6)

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{c(XT1)}$	Cycle time of clock applied to XT1			125		ns
$t_{w(OSC32H)}$	Pulse duration, OSC32 high		10			ns
$t_{w(OSC32L)}$	Pulse duration, OSC32 low		12			ns
$t_{w(PXTALL)}$	Pulse duration, PXTAL low	16-Mbps mode	12			ns
		4-Mbps mode	46			ns
$t_{w(PXTALH)}$	Pulse duration, PXTAL high	16-Mbps mode	10			ns
		4-Mbps mode	46			ns
$t_{w(RCLKL)}$	Pulse duration, RCLK low	16-Mbps mode	12			ns
		4-Mbps mode	46			ns
$t_{w(RCLKH)}$	Pulse duration, RCLK high	16-Mbps mode	10			ns
		4-Mbps mode	46			ns
$t_{su(RCVR)}$	Setup time, RCVR valid to RCLK rising edge	16-Mbps mode	10			ns
$t_{h(RCVR)}$	Hold time, RCVR valid after RCLK rising edge	16-Mbps mode	1			ns

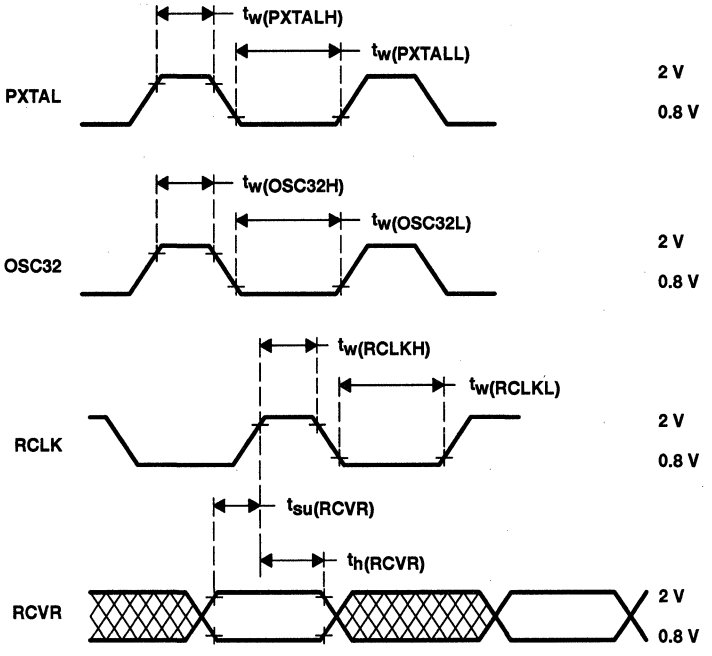


Figure 6. PXTAL, RCLK, and RCVR Timing

- IEEE 802.5 and IBM Token-Ring Network™ Compatible
- IEEE 802.3 and Blue Book Ethernet™ Network Compatible
- Pin and Software Compatible With the TMS380C16
- Configurable Network Type and Speed:
  - Selectable by Host Software Control (Adapter-Control Register)
  - Selectable by Network Front-End
  - Readable from Host (Adapter-Control Register)
- Token-Ring Features
  - 16- or 4-Mbps Data Rates
  - Supports up to 18K-Byte Frame Size (16-Mbps Operation Only)
  - Supports Universal and Local Network Addressing
  - Early Token-Release Option (16-Mbps Operation Only)
  - Compatible With the TMS38054
- Ethernet Features
  - 10-Mbps Data Rate
  - Compatible With Most Ethernet Serial-Network-Interface Devices
  - Full-Duplex Ethernet Operation Allows Network Speed Self-Test Feature
- Expandable Local LAN-Subsystem Memory Space up to 2 Megabytes
- Supports Multicast Addressing of Network Group Addresses Through Hashing
- Glueless Interface to DRAMs
- High-Performance 16-Bit CPU for Communications-Protocol Processing
- Up to 8-Mbps High-Speed Bus Master DMA Interface
- Low-Cost Host-Slave I/O Interface Option
- Up to 32-Bit Host Address Bus
- Selectable Host System-Bus Options
- 80x8x or 68xxx-Type Bus and Memory Organization
  - 8- or 16-Bit Data Bus on 80x8x Buses
  - Optional Parity Checking
- Dual-Port DMA and Direct I/O Transfers to Host Bus
- Specification for External Adapter-Bus Devices (SEADs) Supports External Hardware Interface for User-Defined External Logic
- Enhanced-Address-Copy-Option (EACO) Interface Supports External Address Checking Logic for Bridging or External Custom Applications
- Support for Module High-Impedance In-Circuit Testing
- Built-in Real-Time Error Detection
- Bring-Up and Self-Test Diagnostics With Loopback
- Automatic Frame-Buffer Management
- Slow-Clock Low-Power Mode
- Single 5-V Supply
- 1-μm CMOS Technology
- 250-mA Typical Latch-Up Immunity at 25°C
- ESD Protection Exceeds 2000 V
- 132-Pin Plastic Quad Flat Package (PQ Suffix)
- Operating Temperature Range 0°C to 70 °C

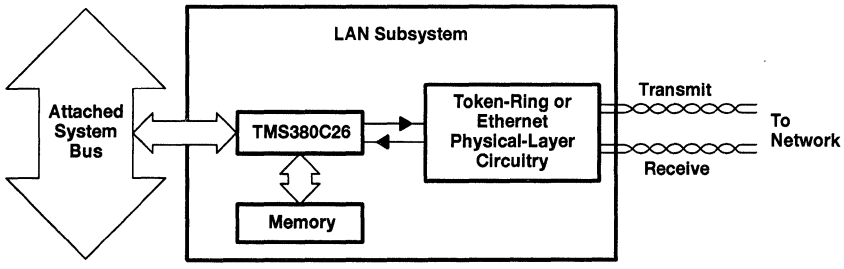


Figure 1. Network-Commprocessor Applications Diagram

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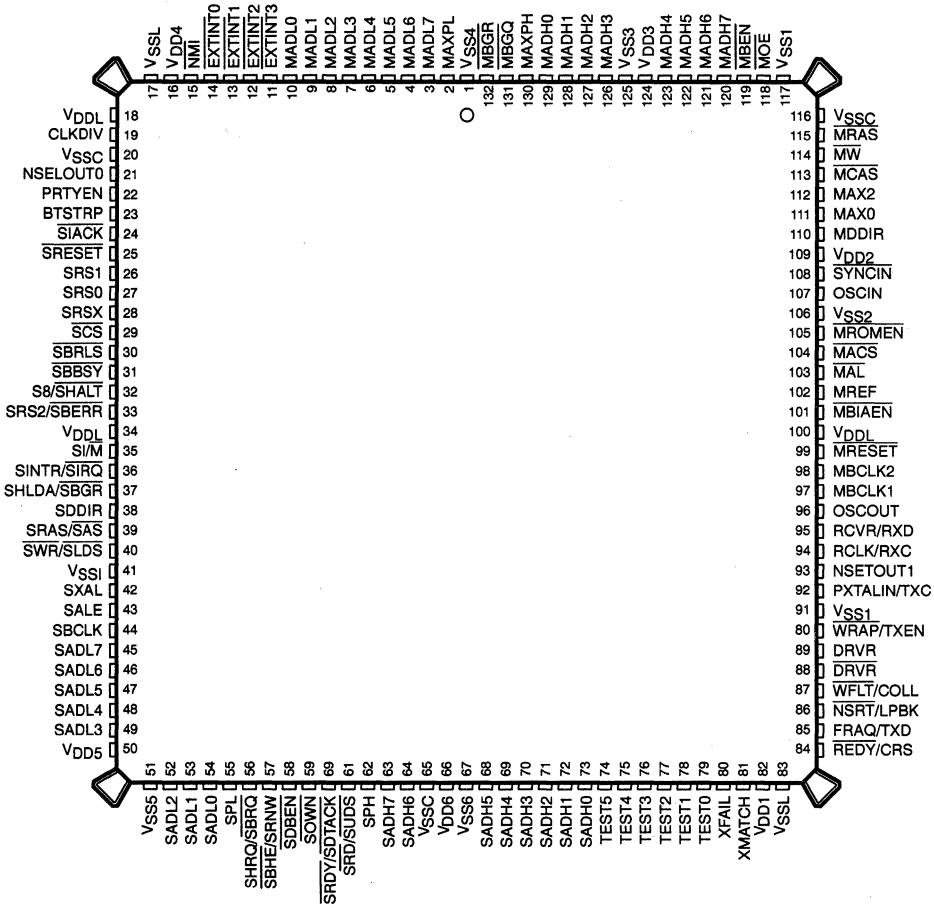
Ethernet is a trademark of Xerox Corporation.

pin assignments

PQ PACKAGE
(TOP VIEW)



description

The TMS380C26 is a single-chip network-communications processor (commprocessor) that supports token-ring or Ethernet local area networks (LANs). Either token ring at data rates of 16 Mbps or 4 Mbps, or Ethernet at a data rate of 10 Mbps, can be selected. A flexible configuration scheme allows network type and speed to be configured by hardware or software. This allows the design of LAN subsystems that support both token-ring and Ethernet networks by electrically or physically switched network front-end circuits.

The TMS380C26 conforms to IEEE 802.5–1989 standards and has been verified to be completely IBM™ Token-Ring compatible. By integrating the essential control building blocks needed on a LAN-subsystem card into one device, the TMS380C26 can ensure that this IBM compatability is maintained in silicon.

The TMS380C26 conforms to ISO/IEC 8802–3 (ANSI/IEEE Std 802.3) CSMA/CD standards and the Ethernet Blue Book standard.

The high degree of integration of the TMS380C26 makes it a virtual LAN subsystem on a single chip. Protocol handling, host-system interfacing, memory interfacing, and communications processing are all provided through the TMS380C26. To complete LAN-subsystem design, only the network-interface hardware, local memory, and minimal additional components such as PALs and crystal oscillators need to be added.

The TMS380C26 provides a 32-bit system-memory address reach with a high-speed bus-master DMA interface that supports rapid communications with the host system. In addition, the TMS380C26 supports direct I/O and a low-cost 8-bit pseudo-DMA interface that requires only a chip select to work directly on an 80x8x 8-bit slave I/O interface. Finally, selectable 80x8x or 68xxx-type host-system bus and memory organization add to design flexibility.

The TMS380C26 supports addressing for up to 2M bytes of local memory. This expanded memory capacity can improve LAN-subsystem performance by minimizing the frequency of host LAN-subsystem communications by allowing larger blocks of information to be transferred at one time. The support of large local memory is important in applications that require large data transfers (such as graphics or data-base transfers) and in heavily loaded networks where the extra memory can provide data buffers to store data until it can be processed by the host.

The proprietary CPU used in the TMS380C26 allows protocol software to be downloaded into RAM or stored in ROM in the local-memory space. By moving protocols (such as LLC) to the LAN-subsystem, overall system performance is increased. This is accomplished due to the the offloading of processing from the host system to the TMS380C26, which can also reduce LAN-subsystem-to-host communications. As other protocol software is developed, greater differentiation of end products with enhanced system performance is possible.

In addition, the TMS380C26 includes hardware counters that provide real-time error detection and automatic frame-buffer management. These counters control system-bus retries, burst size, and track host and LAN-subsystem buffer status. Previously, these counters needed to be maintained in software. By integrating them into hardware, software overhead is removed and LAN-subsystem performance is improved.

The TMS380C26 implements a TI-patented enhanced-address-copy-option (EACO) interface. This interface supports external address-checking devices, such as the TMS380SRA source-routing accelerator. The TMS380C26 has a 128-word external I/O space in its memory map to support external address-checker devices and other hardware extensions to the TMS380 architecture. Hardware designed in conformance with TI's specification for external adapter-bus devices (SEADs) can map registers into this external I/O space and post interrupts to the TMS380C26.

The major blocks of the TMS380C26 include the communications processor (CP), system interface (SIF), memory interface (MIF), protocol handler (PH), clock generator (CG), and the adapter-support function (ASF) as shown in the functional block diagram.

The TMS380C26 is available in a 132-pin plastic quad flat pack and is characterized for operation from 0°C to 70°C.

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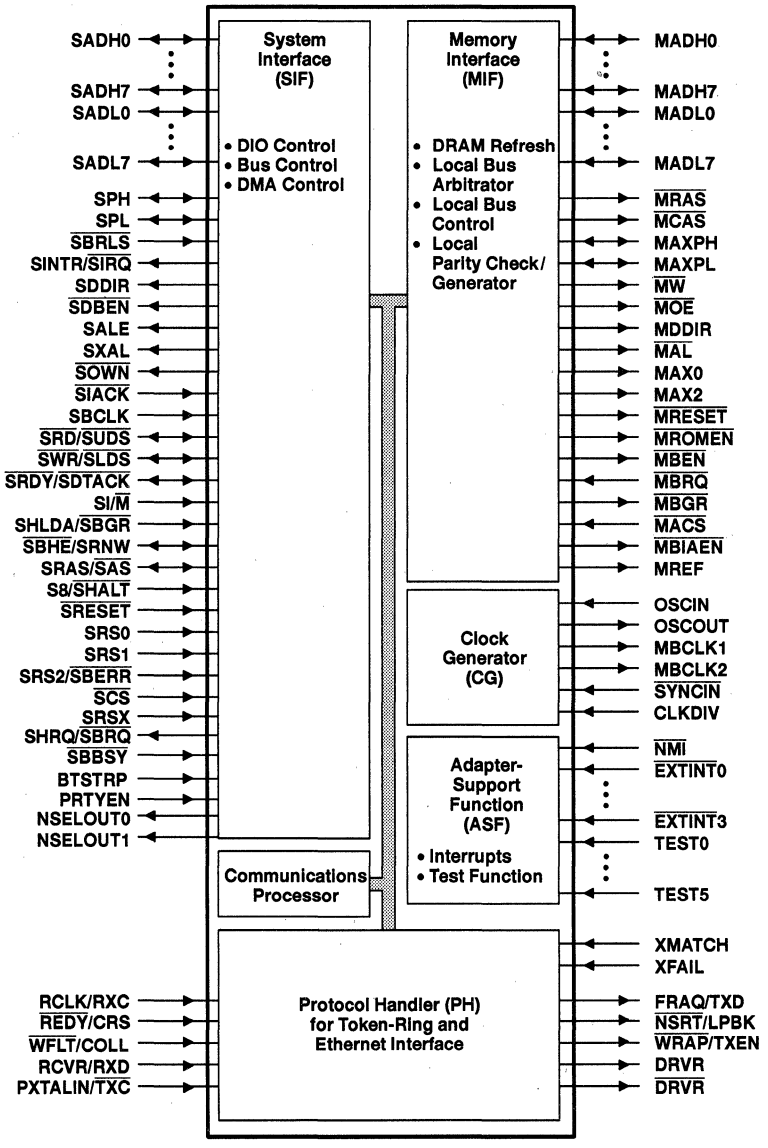
description (continued)

The TMS380C26 has a bus interface to the host system, a bus interface to local memory, and an interface to the physical-layer circuitry. Pin names starting with the letter S attach to the host-system bus and pin names starting with the letter M attach to the local-memory bus. Active-low signals have names with overbars, e.g., $\overline{\text{SCS}}$.

functional block diagram



Pin Functions

PIN NAME	NO.	I/O†	DESCRIPTION
BTSTRP	23	I	Bootstrap. The value on BTSTRP is loaded into the BOOT bit of the SIFACL register at reset (i.e., when $\overline{\text{SRESET}}$ is asserted or the $\overline{\text{ARESET}}$ bit in the SIFACL register is set) to form a default value. BTSTRP indicates whether chapters 0 and 31 of the memory map are RAM or ROM. If these chapters are RAM then the TMS380C26 is denied access to the local-memory bus until the CPHALT bit in the SIFACL register is cleared. H = Chapters 0 and 31 of local memory are RAM based (see Note 1). L = Chapters 0 and 31 of local memory are ROM based.
CLKDIV	19	I	Clock divider select. CLKDIV must be pulled high. H = Indicates 64-MHz OSCIN (see Note 3) L = Reserved
$\overline{\text{EXTINT0}}$ $\overline{\text{EXTINT1}}$ $\overline{\text{EXTINT2}}$ $\overline{\text{EXTINT3}}$	14 13 12 11	I	Reserved; must be pulled high (see Note 4)
$\overline{\text{MACS}}$	104	I	Reserved; must be tied low (see Note 2)
MADH0 MADH1 MADH2 MADH3 MADH4 MADH5 MADH6 MADH7	129 128 127 126 123 122 121 120	I/O	Local-memory address, data and status bus – high byte. For the first quarter of the local-memory cycle these bus lines carry address bits AX4 and A0 to A6; for the second quarter, they carry status bits; and for the third and fourth quarters, they carry data bits 0 to 7. The most significant bit is MADH0 and the least significant bit is MADH7. Memory Cycle 1Q 2Q 3Q 4Q Signal AX4,A0–A6 Status D0–D7 D0–D7
MADL0 MADL1 MADL2 MADL3 MADL4 MADL5 MADL6 MADL7	10 9 8 7 6 5 4 3	I/O	Local-memory address, data and status bus – low byte. For the first quarter of the local-memory cycle, these bus lines carry address bits A7 to A14; for the second quarter, they carry address bits AX4 and A0 to A6; and for the third and fourth quarters, they carry data bits 8 to 15. The most significant bit is MADL0 and the least significant bit is MADL7. Memory Cycle 1Q 2Q 3Q 4Q Signal A7–A14 AX4,A0–A6 D8–D15 D8–D15
$\overline{\text{MAL}}$	103	O	Memory-address latch. $\overline{\text{MAL}}$ is a strobe signal for sampling the address at the start of the memory cycle; it is used by SRAMs and EPROMs. The full 20-bit word address is valid on MAX0, MAXPH, MAX2, MAXPL, MADH0-MADH7, and MADL0-MADL7. Three 8-bit transparent latches can be used to retain a 20-bit static address throughout the cycle. Rising edge = No signal latching Falling edge = Allows the above address signals to be latched
MAX0	111	O	Local-memory-extended address bit. MAX0 drives AX0 at ROW address time and drives A12 at COL address and DATA time for all cycles. This signal can be latched by $\overline{\text{MRAS}}$. Driving A12 eases interfacing to a BIA ROM. Memory Cycle 1Q 2Q 3Q 4Q Signal AX0 A12 A12 A12

† I = input, O = output

NOTES: 1. Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch or loads).
2. Pin should be connected to ground.
3. Pin should be tied to V_{CC} with a 4.7-kΩ pullup resistor.
4. Each pin must be individually tied to V_{CC} with a 1-kΩ pullup resistor.

Pin Functions (Continued)

PIN NAME	NO.	I/O†	DESCRIPTION
MAX2	112	O	Local-memory-extended address bit. MAX2 drives AX2 at ROW address time, which can be latched by $\overline{\text{MRAS}}$, and A14 at COL address, and DATA time for all cycles. Driving A14 eases interfacing to a BIA ROM. Memory Cycle 1Q 2Q 3Q 4Q Signal AX2 A14 A14 A14
MAXPH	130	I/O	Local-memory-extended address and parity – high byte. For the first quarter of a memory cycle, MAXPH carries the extended-address bit (AX1); for the second quarter of a memory cycle, MAXPH carries the extended-address bit (AX0); and for the last half of the memory cycle, MAXPH carries the parity bit for the high-data byte. Memory Cycle 1Q 2Q 3Q 4Q Signal AX1 AX0 Parity Parity
MAXPL	2	I/O	Local-memory-extended address and parity – low byte. For the first quarter of a memory cycle, MAXPL carries the extended-address bit (AX3); for the second quarter of a memory cycle, MAXPL carries extended-address bit (AX2); and for the last half of the memory cycle, MAXPL carries the parity bit for the low-data byte. Memory Cycle 1Q 2Q 3Q 4Q Signal AX3 AX2 Parity Parity
MBCLK1 MBCLK2	97 98	O	Local-bus clock 1 and local-bus clock 2. These signals are referenced for all local-bus transfers. MBCLK2 lags MBCLK1 by a quarter of a cycle. These clocks operate at 8 MHz for a 64-MHz OSCIN and 6 MHz for a 48-MHz OSCIN, which is twice the memory-cycle rate. The MBCLK signals are always a divide-by-8 of the OSCIN frequency.
$\overline{\text{MBEN}}$	119	O	Buffer enable. $\overline{\text{MBEN}}$ enables the bidirectional buffer outputs on the MADH, MAXPH, MAXPL, and MADL buses during the data phase. This signal is used in conjunction with MDDIR, which selects the buffer output direction. H = Buffer output disabled L = Buffer output enabled
$\overline{\text{MBGR}}$	132	O	Reserved; must be left unconnected
$\overline{\text{MBIAEN}}$	101	O	Burned-in address enable. $\overline{\text{MBIAEN}}$ is an output signal used to provide an output enable for the ROM containing the adapter's burned-in address (BIA). H = This signal is driven high for any WRITE accesses to the addresses between >00.0000 and >00.000F, or any accesses (read/write) to any other address. L = This signal is driven low for any READ from addresses between >00.0000 and >00.000F.
$\overline{\text{MBRQ}}$	131	I	Reserved; must be pulled high (see Note 4)
$\overline{\text{MCAS}}$	113	O	Column-address strobe for DRAMs. The column address is valid for the 3/16 of the memory cycle following the row-address portion of the cycle. $\overline{\text{MCAS}}$ is driven low every memory cycle while the column address is valid on MADL0 – MADL7, MAXPH, and MAXPL, except when one of the following conditions occurs: 1) When the address accessed is in the BIA ROM (>00.0000 – >00.000F) 2) When the address accessed is in the EPROM memory map (i.e., when the BOOT bit in the SIFACL register is zero and an access is made between >00.0010 – >00.FFFF) or >1F.0000 – >1F.FFFF) 3) When the cycle is a refresh cycle, in which case $\overline{\text{MCAS}}$ is driven at the start of the cycle before $\overline{\text{MRAS}}$ (for DRAMs that have $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh). For DRAMs that do not support $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, it can be necessary to disable $\overline{\text{MCAS}}$ with MREF during the refresh cycle.

† I = input, O = output

NOTE 4: Each pin must be individually tied to V_{CC} with a 1-kΩ pullup resistor.

Pin Functions (Continued)

PIN NAME	NO.	I/O†	DESCRIPTION
MDDIR	110	O	Data direction. MDDIR is used as a direction control for bidirectional bus drivers. This signal becomes valid before $\overline{\text{MBEN}}$ becomes active. H = TMS380C26 memory-bus write L = TMS380C26 memory-bus read
$\overline{\text{MOE}}$	118	O	Memory output enable. $\overline{\text{MOE}}$ is used to enable the outputs of the DRAM memory during a read cycle. This signal is high for EPROM or BIA ROM read cycles. H = Disable DRAM outputs L = Enable DRAM outputs
$\overline{\text{MRAS}}$	115	O	Row-address strobe for DRAMs. The row address lasts for the first 5/16 of the memory cycle. $\overline{\text{MRAS}}$ is driven low every memory cycle while the row address is valid on MADL0–MADL7, MAXPH, and MAXPL for both RAM and ROM cycles. It is also driven low during refresh cycles when the refresh address is valid on MADL0–MADL7.
MREF	102	O	DRAM refresh cycle in progress. MREF is used to indicate that a DRAM refresh cycle is occurring. It is also used for disabling $\overline{\text{MCAS}}$ to all DRAMs that do not use a $\overline{\text{CAS}}$ before-$\overline{\text{RAS}}$ refresh. H = DRAM refresh cycle in process L = Not a DRAM refresh cycle
$\overline{\text{MRESET}}$	99	O	Memory-bus reset. $\overline{\text{MRESET}}$ is a reset signal generated when either the ARESET bit in the SIFACL register is set or $\overline{\text{SRESET}}$ is asserted. This signal is used for resetting external local-bus glue logic. H = External logic not reset L = External logic reset
$\overline{\text{MROMEN}}$	105	O	ROM enable. During the first 5/16 of the memory cycle, $\overline{\text{MROMEN}}$ is used to provide a chip select for ROMs when the BOOT bit of the SIFACL register is zero (i.e., when code is resident in ROM, not RAM). It can be latched by $\overline{\text{MAL}}$. $\overline{\text{MROMEN}}$ goes low for any read from addresses >00.0010 – >00.FFFF or >1F.0000–>1F.FFFF when the BOOT bit in the SIFACL register is zero. $\overline{\text{MROMEN}}$ stays high for writes to these addresses, accesses of other addresses, or accesses of any address when the BOOT bit is one. During the final three quarters of the memory cycle, $\overline{\text{MROMEN}}$ outputs the A13 address signal for interfacing to a BIA ROM. This means $\overline{\text{MBIAEN}}$, MAX0, $\overline{\text{ROMEN}}$, and MAX2 together form a glueless interface for the BIA ROM. H = ROM disabled L = ROM enabled
$\overline{\text{MW}}$	114	O	Local-memory write. $\overline{\text{MW}}$ is used to specify a write cycle on the local-memory bus. The data on the MADH0 – MADH7 and MADL0 – MADL7 buses is valid while $\overline{\text{MW}}$ is low. DRAMs latch data on the falling edge $\overline{\text{MW}}$, while SRAMs latch data on the rising edge of $\overline{\text{MW}}$. H = Not a local-memory write cycle L = Local-memory write cycle
$\overline{\text{NMI}}$	15	I	Nonmaskable interrupt request. $\overline{\text{NMI}}$ must be left unconnected.
OSCIN	107	I	External oscillator input. OSCIN provides the clock frequency to the TMS380C26 for a 4-MHz internal bus. OSCIN should be 64-MHz signal (see Note 5).
OSCOUT	96	O	Oscillator output. With OSCIN at 64 MHz and CLKDIV pulled high, OSCOUT provides an 8-MHz output that can be used by TMS3054 for 4-Mbps operation without the need for an additional crystal. CLKDIV OSCOUT L Reserved (Reserved) H OSCIN/8 (if OSCIN = 64 MHz, then OSCOUT = 8 MHz)

† I = input, O = output

NOTE 5: Pin has an expanded input voltage specification.

Pin Functions (Continued)

PIN NAME	NO.	I/O†	DESCRIPTION
PRTYEN	22	I	Parity enable. The value on PRTYEN is loaded into the PEN bit of the SIFACL register at reset (i.e., when $\overline{\text{SRESET}}$ is asserted or the ARESET bit in the SIFACL register is set) to form a default value. PRTYEN enables parity checking for the local memory. H = Local-memory data bus checked for parity (see Note 1) L = Local-memory data bus not checked for parity
NSELOUT0 NSELOUT1	21 93	O	Network selection outputs. NSELOUT0 and NSELOUT1 are controlled by the host through the corresponding bits of the SIFACTL register. The value of these bits/signals can only be changed while the TMS380C26 is reset. NSELOUT0 / NSELOUT1 / Description L / L / Reserved L / H / 16-Mbps token ring H / L / Ethernet (802.3/blue book) H / H / 4-Mbps token ring

† I = input, O = output

NOTE 1: Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch or loads).

Pin Functions (Continued)

System Interface – Intel Mode (SI/$\overline{M}$ = H)

PIN NAME	NO.	I/O†	DESCRIPTION
SADH0 SADH1 SADH2 SADH3 SADH4 SADH5 SADH6 SADH7	73 72 71 70 69 68 64 63	I/O	System address/data bus–high byte (see Note 1). SADH0–SADH7 make up the most significant byte of each address word (32-bit address bus) and data word (16-bit data bus). The most significant bit is SADH0, and the least significant bit is SADH7. Address multiplexing‡: Bits 31 – 24 and bits 15 – 8 Data multiplexing‡: Bits 15 – 8
SADL0 SADL1 SADL2 SADL3 SADL4 SADL5 SADL6 SADL7	54 53 52 49 48 47 46 45	I/O	System address/data bus–low byte (see Note 1). SADL0–SADL7 make up the least significant byte of each address word (32-bit address bus) and data word (16-bit data bus). The most significant bit is SADL0, and the least significant bit is SADL7. Address multiplexing‡: Bits 23 – 16 and bits 7 – 0 Data multiplexing‡: Bits 7 – 0
SALE	43	O	System address-latch enable. SALE is the enable pulse used to externally latch the 16 LSBs of the address from the SADH0 – SADH7 and SADL0 – SADL7 buses at the start of the DMA cycle. Systems that implement address parity can also externally latch the parity bits (SPH and SPL) for the latched address.
$\overline{SBBSY}$	31	I	System bus busy. The TMS380C26 samples the value on $\overline{SBBSY}$ during arbitration. The sample has one of (2) two values (see Note 1): H = Not busy. The TMS380C26 can become bus master if the grant condition is met. L = Busy. The TMS380C26 cannot become bus master.
SBCLK	44	I	System bus clock. The TMS380C26 requires SBCLK to synchronize its bus timings for all DMA transfers.
$\overline{SBHE}$/SRNW	57	I/O	System byte high enable. $\overline{SBHE}$/SRNW is a 3-state output that is driven during DMA and an input at all other times. H = System byte high not enabled (see Note 1) L = System byte high enabled
$\overline{SBRLS}$	30	I	System bus release. $\overline{SBRLS}$ indicates to the TMS380C26 that a higher-priority device requires the system bus. The value on $\overline{SBRLS}$ is ignored when the TMS380C26 is not perfoming DMA. $\overline{SBRLS}$ is internally synchronized to SBCLK. H = The TMS380C26 can hold onto the system bus (see Note 1). L = The TMS380C26 should release the system bus upon completion of current DMA cycle. If the DMA transfer is not yet complete, the SIF rearbitrates for the system bus.
$\overline{SCS}$	29	I	System chip select. $\overline{SCS}$ activates the system interface of the TMS380C26 for a DIO read or write. H = Not selected (see Note 1) L = Selected
$\overline{SDBEN}$	58	O	System data-bus enable. $\overline{SDBEN}$ signals to the external data buffers to begin driving data. $\overline{SDBEN}$ is activated during both DIO and DMA. H = Keep external data buffers in the high-impedance state L = Cause external data buffers to begin driving data

† I = input, O = output
‡ Typical bit ordering for Intel and Motorola processor buses
NOTE 1: Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch or loads).

Pin Functions (Continued)

System Interface – Intel Mode (SI/$\overline{M}$ = H)

PIN NAME	NO.	I/O†	DESCRIPTION
SDDIR	38	O	System data direction. SDDIR provides to the external data buffers a signal indicating the direction in which the data is moving. During DIO writes and DMA reads, SDDIR is low (data direction input to the TMS380C26). During DIO reads and DMA writes, SDDIR is high (data direction output from the TMS380C26). When the system interface is not involved in a DIO or DMA operation, then SDDIR is high by default. SDDIR: H = DATA DIRECTION output, DIO read, DMA write SDDIR: L = DATA DIRECTION input, DIO write, DMA read
SHLDA/$\overline{SBGR}$	37	I	System hold acknowledge. **SHLDA**/$\overline{SBGR}$ indicates that the system DMA hold request has been acknowledged. **SHLDA**/$\overline{SBGR}$ is internally synchronized to SBCLK (see Note 1). H = Hold request acknowledged L = Hold request not acknowledged
SHRQ/$\overline{SBRQ}$	56	O	System hold request. **SHRQ**/$\overline{SBRQ}$ is used to request control of the system bus in preparation for a DMA transfer. **SHRQ**/$\overline{SBRQ}$ is internally synchronized to SBCLK. H = System bus requested L = System bus not requested
$\overline{SIACK}$	24	I	System interrupt acknowledge. $\overline{SIACK}$ is from the host processor to acknowledge the interrupt request from the TMS380C26. H = System interrupt not acknowledged (see Note 1) L = System interrupt acknowledged: the TMS380C26 places its interrupt vector onto the system bus.
SI/$\overline{M}$	35	I	System Intel/Motorola mode select. The value on **SI**/$\overline{M}$ specifies the system-interface mode. H = Intel-compatible interface mode selected. Intel interface can be 8-bit or 16-bit mode (see S8/$\overline{SHALT}$ pin description and Note 1). L = Motorola-compatible interface mode selected
SINTR/$\overline{SIRQ}$	36	O	System interrupt request. TMS380C26 activates **SINTR**/$\overline{SIRQ}$ to signal an interrupt request to the host processor. H = Interrupt request by TMS380C26 L = No interrupt request
$\overline{SOWN}$	59	O	System bus owned. $\overline{SOWN}$ indicates to external devices that TMS380C26 has control of the system bus. $\overline{SOWN}$ drives the enable signal of the bus transceiver chips, which drive the address and bus-control signals. H = TMS380C26 does not have control of the system bus. L = TMS380C26 has control of the system bus.
SPH	62	I/O	System parity high. The optional odd-parity bit for each address or data byte transmitted over SADH0 – SADH7 (see Note 1).
SPL	55	I/O	System parity low. The optional odd-parity bit for each address or data byte transmitted over SADL0 – SADL7 (see Note 1).

† I = input, O = output

NOTE 1: Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch or loads).

Pin Functions (Continued)

System Interface – Intel Mode (SI/$\overline{M}$ = H)

PIN NAME	NO.	I/O†	DESCRIPTION
SRAS/$\overline{SAS}$	39	I/O	System memory address strobe (see Note 3). **SRAS**/$\overline{SAS}$ is used to latch the $\overline{SCS}$, SRSX – SRS2 register input signals. In a minimum-chip system, SRAS is tied to SALE of the system bus. The latching capability can be defeated since the internal latch for these inputs remains transparent as long as SRAS remains high. This permits SRAS to be pulled high and the signals at the $\overline{SCS}$, SRSX – SRS2, and $\overline{SBHE}$ to be applied independently of the SALE strobe from the system bus. During DMA, **SRAS**/$\overline{SAS}$ remains an input. High = Transparent mode Low = Holds latched values of $\overline{SCS}$, SRSX–SRS2, and $\overline{SBHE}$ Falling edge = Latches $\overline{SCS}$, SRSX – SRS2, and $\overline{SBHE}$
$\overline{SRD}$/$\overline{SUDS}$	61	I/O	System read strobe (see Note 3). **$\overline{SRD}$**/$\overline{SUDS}$ is the active-low strobe indicating that a read cycle is performed on the system bus. **$\overline{SRD}$**/$\overline{SUDS}$ is an input during DIO and an output during DMA. H = Read cyle is not occurring. L = If DMA, host provides data to system bus. If DIO, SIF provides data to system bus.
$\overline{SRDY}$/$\overline{SDTACK}$	60	I/O	System bus ready (see Note 3).The purpose of **$\overline{SRDY}$**/$\overline{SDTACK}$ is to indicate to the bus master that a data transfer is complete. This signal is asynchonous, but during DMA and pseudo-DMA cycles, it is internally synchronized to SBCLK. During DMA cycles, it must be asserted before the falling edge of SBCLK in state T2 in order to prevent a wait state. This signal is an output when the TMS380C26 is selected for DIO, otherwise, it is an input. H = System bus not ready L = Data transfer is complete; system bus is ready.
$\overline{SRESET}$	25	I	System reset. $\overline{SRESET}$ is activated to place the TMS380C26 into a known initial state. Hardware reset puts most of the TMS380C26 outputs into the high-impedance state and places all blocks into the reset state. DMA bus width selection is latched on the rising edge of $\overline{SRESET}$. H = No system reset L = System reset Rising edge = Latch bus width for DMA operation
SRSX 28 SRS0 27 SRS1 26 SRS2/$\overline{SBERR}$ 33		I	System register select. These inputs select the word or byte to be transferred during a system DIO access. The most significant bit is SRSX and the least significant bit is SRS2 (see Note 1). MSb LSb Registered selected = SRSX SRS0 SRS1 SRS2/$\overline{SBERR}$
$\overline{SWR}$/$\overline{SLDS}$	40	I/O	System write strobe (see Note 3). **$\overline{SWR}$**/$\overline{SLDS}$ serves as an active-low write strobe. **$\overline{SWR}$**/$\overline{SLDS}$ is an input during DIO and an output during DMA. H = Write cycle is not occurring. L = If DMA, data to be driven from SIF to host bus. If DIO, on the rising edge, the data is latched and written to the selected register.
SXAL	42	O	System-extended-address latch. SXAL provides the enable pulse used to externally latch the most significant 16 bits of the 32-bit system address during DMA. SXAL is activated prior to the first cycle of each block DMA transfer, and thereafter as necessary (whenever an increment of the DMA address counter causes a carry-out of the lower 16 bits). Systems that implement parity on addresses can use SXAL to externally latch the parity bits (available on SPL and SPH) for the DMA address extension.

† I = input, O = output

NOTES: 1. Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch or loads).
3. Pin should be tied to V_{CC} with a 4.7-kΩ pullup resistor.

Pin Functions (Continued)

System Interface – Intel Mode (SI/$\overline{M}$ = H)

PIN NAME	NO.	I/O†	DESCRIPTION
$\overline{SYNCIN}$	108	I	Reserved. $\overline{SYNCIN}$ must be left unconnected (see Note 1).
S8/$\overline{SHALT}$	32	I	System 8/16-bit bus select. **S8**/$\overline{SHALT}$ selects the bus width used for communications through the system interface. On the rising edge of $\overline{SRESET}$, the TMS380C26 latches the DMA bus width; otherwise the value on this pin dynamically selects the DIO bus width. H = Selects 8-bit mode (see Note 1) L = Selects 16-bit mode

† I = input, O = output

NOTE 1: Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch or loads).

Pin Functions (Continued)

System Interface – Motorola Mode (SI/$\overline{M}$ = L)

PIN NAME	NO.	I/O†	DESCRIPTION
SADH0 SADH1 SADH2 SADH3 SADH4 SADH5 SADH6 SADH7	73 72 71 70 69 68 64 63	I/O	System address/data bus–high byte (see Note 1). SADH0–SADH7 make up the most significant byte of each address word (32-bit address bus) and data word (16-bit data bus). The most significant bit is SADH0, and the least significant bit is SADH7. Address multiplexing‡: Bits 31 – 24 and bits 15 – 8 Data multiplexing‡: Bits 15 – 8
SADL0 SADL1 SADL2 SADL3 SADL4 SADL5 SADL6 SADL7	54 53 52 49 48 47 46 45	I/O	System address/data bus–low byte (see Note 1). SADL0–SADL7 make up the least significant byte of each address word (32-bit address bus) and data word (16-bit data bus). The most significant bit is SADL0, and the least significant bit is SADL7. Address multiplexing‡: Bits 23 – 16 and bits 7 – 0 Data multiplexing‡: Bits 7 – 0
SALE	43	O	System address-latch enable. SALE is the enable pulse used to externally latch the 16 LSBs of the address from the SADH0 – SADH7 and SADL0 – SADL7 buses at the start of the DMA cycle. Systems that implement address parity can also externally latch the parity bits (SPH and SPL) for the latched address.
$\overline{\text{SBBSY}}$	31	I	System bus busy. The TMS380C26 samples the value on $\overline{\text{SBBSY}}$ during arbitration. The sample has one of (2) two values (see Note 1): H = Not busy. The TMS380C26 can become bus master if the grant condition is met. L = Busy. The TMS380C26 cannot become bus master.
SBCLK	44	I	System bus clock. The TMS380C26 requires SBCLK to synchronize its bus timings for all DMA transfers.
$\overline{\text{SBHE}}$/**SRNW**	57	I/O	System read not write. $\overline{\text{SBHE}}$/**SRNW** serves as a control signal to indicate a read or write cycle. H = Read cycle (see Note 1) L = Write cycle
$\overline{\text{SBRLS}}$	30	I	System bus release. $\overline{\text{SBRLS}}$ indicates to the TMS380C26 that a higher-priority device requires the system bus. The value on $\overline{\text{SBRLS}}$ is ignored when the TMS380C26 is not performing DMA. $\overline{\text{SBRLS}}$ is internally synchronized to SBCLK. H = The TMS380C26 can hold onto the system bus (see Note 1). L = The TMS380C26 should release the system bus upon completion of current DMA cycle. If the DMA transfer is not yet complete, the SIF rearbitrates for the system bus.
$\overline{\text{SCS}}$	29	I	System chip select. $\overline{\text{SCS}}$ activates the system interface of TMS380C26 for a DIO read or write. H = Not selected (see Note 1) L = Selected
$\overline{\text{SDBEN}}$	58	O	System data-bus enable. $\overline{\text{SDBEN}}$ signals to the external data buffers to begin driving data. $\overline{\text{SDBEN}}$ is activated during both DIO and DMA. H = Keep external data buffers in the high-impedance state L = Cause external data buffers to begin driving data

† I = input, O = output
‡ Typical bit ordering for Intel and Motorola processor buses.
NOTE 1: Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch or loads).

Pin Functions (Continued)

System Interface – Motorola Mode (SI/$\overline{M}$ = L)

PIN NAME	NO.	I/O†	DESCRIPTION
SDDIR	38	O	System data direction. SDDIR provides to the external data buffers a signal indicating the direction in which the data is moving. During DIO writes and DMA reads, SDDIR is low (data direction input to the TMS380C26). During DIO reads and DMA writes, SDDIR is high (data direction output from the TMS380C26). When the system interface is not involved in a DIO or DMA operation, SDDIR is high by default. SDDIR: H = DATA DIRECTION output, DIO read, DMA write; L = DATA DIRECTION input, DIO write, DMA read
SHLDA/**$\overline{SBGR}$**	37	I	System bus grant. SHLDA/**$\overline{SBGR}$** serves as an active-low bus grant as defined in the standard 68000 interface and is internally synchronized to SBCLK (see Note 1). H = System bus not granted L = System bus granted
SHRQ/**$\overline{SBRQ}$**	56	O	System bus request. SHRQ/**$\overline{SBRQ}$** is used to request control of the system bus in preparation for a DMA transfer. SHRQ/**$\overline{SBRQ}$** is internally synchronized to SBCLK. H = System bus not requested L = System bus requested
$\overline{SIACK}$	24	I	System interrupt acknowledge. $\overline{SIACK}$ is from the host processor to acknowledge the interrupt request from the TMS380C26. H = System interrupt not acknowledged (see Note 1) L = System interrupt acknowledged: The TMS380C26 places its interrupt vector onto the system bus.
SI/$\overline{M}$	35	I	System Intel/Motorola mode select. The value on SI/$\overline{M}$ specifies the system-interface mode. H = Intel-compatible interface mode selected L = Motorola-compatible interface mode selected. Motorola interface mode is always 16 bits.
SINTR/**$\overline{SIRQ}$**	36	O	System interrupt request. TMS380C26 activates SINTR/**$\overline{SIRQ}$** to signal an interrupt request to the host processor. H = No interrupt request L = Interrupt request by TMS380C26
$\overline{SOWN}$	59	O	System bus owned. $\overline{SOWN}$ indicates to external devices that TMS380C26 has control of the system bus. $\overline{SOWN}$ drives the enable signal of the bus transceiver chips that drive the address and bus-control signals. H = TMS380C26 does not have control of the system bus. L = TMS380C26 has control of the system bus.
SPH	62	I/O	System parity high. The optional odd-parity bit for each address or data byte transmitted over SADH0 – SADH7 (see Note 1).
SPL	55	I/O	System parity low. The optional odd-parity bit for each address or data byte transmitted over SADL0 – SADL7 (see Note 1).
SRAS/**$\overline{SAS}$**	39	I/O	System-memory address strobe (see Note 3). SRAS/**$\overline{SAS}$** is an active-low address strobe that is an input during DIO (although ignored as an address strobe) and an output during DMA. H = Address not valid L = Address is valid and a transfer operation is in progress.

† I = input, O = output

NOTES: 1. Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch or loads).
3. Pin should be tied to V_{CC} with a 4.7-kΩ pullup resistor.

Pin Functions (Continued)

System Interface – Motorola Mode (SI/$\overline{M}$ = L)

PIN NAME	NO.	I/O†	DESCRIPTION
$\overline{SRD}$/**$\overline{SUDS}$**	61	I/O	Upper data strobe (see Note 3). $\overline{SRD}$/**$\overline{SUDS}$** serves as the active-low upper data strobe. $\overline{SRD}$/**$\overline{SUDS}$** is an input during DIO and an output during DMA. H = Not valid data on SADH0 – SADH7 lines L = Valid data on SADH0 – SADH7 lines
$\overline{SRDY}$/**$\overline{SDTACK}$**	60	I/O	System-data-transfer acknowledge (see Note 3). The purpose of $\overline{SRDY}$/**$\overline{SDTACK}$** is to indicate to the bus master that a data transfer is complete. This signal is internally synchronized to SBCLK. During DMA cycles, it must be asserted before the falling edge of SBCLK in state T2 in order to prevent a wait state. This signal is an output when the TMS380C26 is selected for DIO; otherwise it is an input. H = System bus not ready L = Data transfer is complete; system bus is ready.
$\overline{SRESET}$	25	I	System reset. $\overline{SRESET}$ is activated to place the adapter into a known initial state. Hardware reset puts most of the TMS380C26 output pins into the high-impedance state and places all blocks into the reset state. H = No system reset L = System reset
SRSX SRS0 SRS1	28 27 26	I	System register select. SRSX–SRS0 select the word or byte to be transferred during a system DIO access. The most significant bit is SRSX and the least significant bit is SRS1 (see Note 1). MSb LSb Register selected = SRSX SRS0 SRS1
SRS2/**$\overline{SBERR}$**	33	I	Bus error. SRS2/**$\overline{SBERR}$** corresponds to the bus-error signal of the 68000 microprocessor and is internally synchronized to SBCLK. SRS2/**$\overline{SBERR}$** is driven low during a DMA cycle to indicate to the TMS380C26 that the cycle must be terminated [see Section 3.4.5.3 of the *TMS380 Second-Generation Token Ring User's Guide* (SPWU005) for more information (see Note 1)].
$\overline{SWR}$/**$\overline{SLDS}$**	40	I/O	Lower data strobe (see Note 3). $\overline{SWR}$/**$\overline{SLDS}$** is an input during DIO and an output during DMA. $\overline{SWR}$/**$\overline{SLDS}$** serves as the active-low lower data strobe. H = Not valid data on SADL0 – SADL7 lines L = Valid data on SADL0–SADL7 lines
SXAL	42	O	System-extended-address latch. SXAL provides the enable pulse used to externally latch the most significant 16 bits of the 32-bit system address during DMA. SXAL is activated prior to the first cycle of each block DMA transfer, and thereafter as necessary (whenever an increment of the DMA address counter causes a carry-out of the lower 16-bits). Systems that implement parity on addresses can use SXAL to externally latch the parity bits (available on SPL and SPH) for the DMA address extension.
$\overline{SYNCIN}$	108	I	Reserved. $\overline{SYNCIN}$ must be left unconnected (see Note 1).
S8/**$\overline{SHALT}$**	32	I	System halt/bus error retry. If S8/**$\overline{SHALT}$** is asserted along with bus errror ($\overline{SBERR}$), the adapter retries the last DMA cycle. This is the rerun operation as defined in the 68000 specification. The BERETRY counter is not decremented by $\overline{SBERR}$ when $\overline{SHALT}$ is asserted [see Section 3.4.5.3 of the *TMS380 Second-Generation Token Ring User's Guide* (SPWU005) for more information].

† I = input, O = output

NOTES: 1. Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch or loads).
3. Pin should be tied to V_{CC} with a 4.7-kΩ pullup resistor.

Pin Functions (Continued)

Network Media Interface – Token-Ring Mode (TEST1 = H, TEST2 = H)

PIN NAME	NO.	I/O†	DESCRIPTION
DRVR $\overline{\text{DRVR}}$	89 88	O	Differential driver data output. DRVR and $\overline{\text{DRVR}}$ are the differential outputs that send the TMS380C16 transmit data to the TMS38054 for driving onto the ring-transmit-signal pair.
FRAQ/TXD	85	O	Frequency acquisition control. **FRAQ**/TXD determines the use of frequency or phase-acquisition mode in the TMS38054. H = Wide range. Frequency centering to PXTALIN by TMS38054. L = Narrow range. Phase lock onto the incoming data (RCVINA and RCVINB) by the TMS38054.
$\overline{\text{NSRT}}$/LPBK	86	O	Insert control signal to the TMS38054. **$\overline{\text{NSRT}}$**/LPBK enables the phantom-driver outputs (PHOUTA and PHOUTB) of the TMS38054, through the watchdog timer, for insertion onto the token ring. Static high = Inactive, phantom current removed (due to watchdog timer) Static low = Inactive, phantom current removed (due to watchdog timer) $\overline{\text{NSRT}}$ low and pulsed high = Active, current output on PHOUTA and PHOUTB
PXTALIN/$\overline{\text{TXC}}$	92	I	Ring-interface clock-frequency control (see Note 5). At 16-Mbps ring speed, **PXTALIN**/$\overline{\text{TXC}}$ must be supplied a 32-MHz signal. At 4-Mbps ring speed, the **PXTALIN**/$\overline{\text{TXC}}$ must be 8-MHz and can be the output from OSCOUT.
RCLK/RXC	94	I	Ring-interface recovered clock (see Note 5). **RCLK**/RXC is the clock recovered by the TMS38054 from the token-ring received data. For 16-Mbps operation, it is a 32-MHz clock. For 4-Mbps operation, it is an 8-MHz clock.
RCVR/RXD	95	I	Ring-interface received data (see Note 5). **RCVR**/RXD contains the data received by the TMS38054 from the token-ring.
$\overline{\text{REDY}}$/$\overline{\text{CRS}}$	84	I	Ring-interface ready. **$\overline{\text{REDY}}$**/$\overline{\text{CRS}}$ provides an indication of the presence of received data as monitored by the TMS38054 energy-detect capacitor. H = Not ready. Ignore received data. L = Ready. Received data.
$\overline{\text{WFLT}}$/COLL	87	I	Wire-fault detect. **$\overline{\text{WFLT}}$**/COLL is an input to the TMS380C16 driven by the TMS38054 and indicates a current imbalance of the TMS38054 PHOUTA and PHOUTB pins. H = No wire fault detected L = Wire fault detected
$\overline{\text{WRAP}}$/TXEN	90	O	Internal wrap select. **$\overline{\text{WRAP}}$**/TXEN is an output from the TMS380C16 to the ring interface to activate an internal attenuated-feedback path from the transmitted data (DRVR) to receive data (RCVR) signals for bring-up diagnostic testing. When active, the TMS38054 also cuts off the current drive to the transmission pair. H = Normal ring operation L = Transmit data drives receive data (loopback)

† I = input, O = output

NOTE 5: Pin has an expanded input voltage specification.

Pin Functions (Continued)

Network Media Interface – Ethernet Mode (TEST1 = L, TEST2 = H)

PIN NAME	NO.	I/O†	DESCRIPTION
DRVR $\overline{\text{DRVR}}$	89 88	O	DRVR and $\overline{\text{DRVR}}$ have no Ethernet function. In Ethernet mode, these pins are placed in their token-ring reset state of DRVR = high, $\overline{\text{DRVR}}$ = low.
FRAQ/**TXD**	85	O	Ethernet transmit data. FRAQ/**TXD** provides the Ethernet physical-layer circuitry with bit rate from the TMS380C26. Data on this pin is output synchronously to the transmit clock $\overline{\text{TXC}}$. It is normally connected to TXD of an Ethernet serial network interface (SNI) chip.
$\overline{\text{NSRT}}$/**LPBK**	86	O	Loopback. $\overline{\text{NSRT}}$/**LPBK** enables loopback of Ethernet transmit data through the Ethernet SNI device to receive data. H = Wrap through the front end device L = Normal operation
PXTALI/$\overline{\textbf{TXC}}$	92	I	Ethernet transmit clock. PXTALI/$\overline{\textbf{TXC}}$ is a 10-MHz clock input used to synchronize transmit data from the TMS380C26 to the Ethernet physical-layer circuitry. This is a continuously running clock and is normally connected to TXC of an Ethernet SNI chip (see Note 5).
RCLK/**RXC**	94	I	Ethernet receive clock. RCLK/**RXC** is a 10-MHz clock input used to synchronize received data from the Ethernet physical-layer circuitry to the TMS380C26. This clock must be present when CRS is active (although it can be held low for a maximum of 16 clock cycles after the rising edge of CRS). When CRS is inactive it is permissable to hold this clock in a low phase. It is normally connected to RXC of an Ethernet SNI chip. The TMS380C26 requires RCLK/**RXC** to be maintained in the low state when $\overline{\text{CRS}}$ is not asserted (see Note 5).
RCVR/**RXD**	95	I	Ethernet received data. RCVR/**RXD** provides the TMS380C26 with bit-rate network data from the Ethernet front-end device. Data on RCVR/**RXD** must be synchronous with the receive clock RXC and is normally connected to RXD of an Ethernet SNI chip (see Note 5).
$\overline{\text{REDY}}$/$\overline{\textbf{CRS}}$	84	I	Ethernet carrier sense. $\overline{\text{REDY}}$/$\overline{\textbf{CRS}}$ indicates to the TMS380C26 that the Ethernet physical-layer circuitry has network data present on RXD. $\overline{\text{REDY}}$/$\overline{\textbf{CRS}}$ is asserted high when the first bit of the frame is received and is deasserted after the last bit of the frame is received. H = Receiving data L = No data on network
$\overline{\text{WFLT}}$/**COLL**	87	I	Ethernet collision detect. $\overline{\text{WFLT}}$/**COLL** indicates to the TMS380C26 that the Ethernet physical-layer circuitry has detected a network collision. This signal must be present for at least two TXC clock cycles to ensure it is accepted by the TMS380C26 and is normally connected to COLL of an Ethernet SNI chip. $\overline{\text{WFLT}}$/**COLL** can also be an indication of the SQE test signal. H = COLL detected by the SNI device L = Normal operation
$\overline{\text{WRAP}}$/**TXEN**	90	O	Ethernet transmit enable. $\overline{\text{WRAP}}$/**TXEN** indicates to the Ethernet physical-layer circuitry that bit-rate data is present on TXD. $\overline{\text{WRAP}}$/**TXEN** is output synchronously to $\overline{\text{TXC}}$ and is normally connected to TXE of an Ethernet SNI chip. H = Data line currently contains data to be transmitted L = No valid data on TXEN

† I = input, O = output

NOTE 5: Pin has an expanded input voltage specification.

Pin Functions (Continued)

PIN NAME	NO.	I/O†	DESCRIPTION
TEST 0 TEST 1 TEST 2	79 78 77	I	Network select inputs. TEST 0 – TEST2 are used to select the network speed and type to be used by the TMS380C26. These inputs should only be changed during adapter reset. TEST0 TEST1 TEST2 Description L L H Reserved L H H 16-Mbps token ring H L H Ethernet (802.3/blue book) H H H 4-Mbps token ring X X 0 Reserved
TEST3 TEST4 TEST5	76 75 74	I	Test pin inputs. TEST3 – TEST5 should be left unconnected (see Note 1). Module-in-place test mode is achieved by tying TEST 3 and TEST 4 to ground. In this mode, all TMS380C26 output pins are in the high-impedance state. Internal pullups on all TMS380C26 inputs are disabled (except TEST3 – TEST5).
XFAIL	80	I	External fail-to-match signal. An enhanced-address-copy-option (EACO) device uses XFAIL to indicate to the TMS380C26 that it should not copy the frame nor set the ARI/FCI in bits in a token-ring frame due to an external address match.The ARI/FCI bits in a token-ring frame can be set due to an internal address-matched frame. If an EACO device is not used, XFAIL must be left unconnected. XFAIL is ignored when CAF mode is enabled [see table given below in XMATCH description (see Note 1)]. H = No address match by external address checker L = External address-checker-armed state
XMATCH	81	I	External match signal. An EACO device uses XMATCH to indicate to the TMS380C26 to copy the frame and set the ARI/FCI bits in a token-ring frame. If an EACO device is not used, XMATCH must be left unconnected. XMATCH is ignored when CAF mode is enabled (see Note 1). H = Address match recognized by external address checker L = External address-checker-armed state XMATCH XFAIL Function 0 0 Armed (processing frame data) 0 1 Do not externally match the frame (XFAIL takes precedence) 1 0 Copy the frame 1 1 Do not externally match the frame (XFAIL takes precedence) Hi-Z Hi-Z Reset state (adapter not initialized)
V_{DDL}	18 34 100	I	Positive-supply voltage for digital logic. All V_{DD} pins must be attached to the common-system power-supply plane.
V_{DD1} V_{DD2} V_{DD3} V_{DD4} V_{DD5} V_{DD6}	82 109 124 16 50 66	I	Positive-supply voltage for output buffers. All V_{DD} pins must be attached to the common-system power-supply plane.
V_{SSC}	20 65 116	I	Ground reference for output buffers (clean ground). All V_{SS} pins must be attached to the common-system ground plane.
V_{SSI}	41 117	I	Ground reference for input buffers. All V_{SS} pins must be attached to the common-system ground plane.

† I = input, O = output

NOTE 1: Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch or loads).

Pin Functions (Continued)

PIN NAME	NO.	I/O†	DESCRIPTION
V_{SSL}	17 83	I	Ground reference for digital logic. All V_{SS} pins must be attached to the common-system ground plane.
V_{SS1} V_{SS2} V_{SS3} V_{SS4} V_{SS5} V_{SS6}	91 106 125 1 51 67	I	Ground connections for output buffers. All V_{SS} pins must be attached to system-ground plane.

† I = input, O = output

architecture

The major blocks of the TMS380C26 include the communications processor (CP), system interface (SIF), memory interface (MIF), protocol handler (PH), clock generator (CG), and the adapter-support function (ASF). The functionality of each block is described in the following sections.

communications processor (CP)

The CP performs the control and monitoring of the other functional blocks in the TMS380C26. The control and monitoring protocols are specified by the software (downloaded or ROM based) in local memory. Available protocols include:

- Media access control (MAC) software
- Logical link control (LLC) software (token-ring version only)
- Copy all frames (CAF) software

The CP is a proprietary 16-bit central processing unit (CPU) with data cache and a single prefetch pipe for pipelining of instructions. These features enhance the TMS380C26's maximum performance capability to about 4 million instructions per second (MIPS) with an average of about 2.5 MIPS.

system interface (SIF)

The SIF performs the interfacing of the LAN subsystem to the host system. This interface may require additional logic depending on the application. The system interface can transfer information/data using any of these three methods:

- Direct memory access (DMA)
- Direct input/output (DIO)
- Pseudo-direct memory access (PDMA)

DMA (or PDMA) is used to transfer all data to/from host memory from/to local memory. The main uses of DIO are for loading the software to local memory and for initializing the TMS380C26. DIO also allows command/status interrupts to occur to and from the TMS380C26.

The system interface can be hardware selected for either of two modes by use of SI/$\overline{M}$. The mode selected determines the memory organizations and control signals used. These modes are:

- The Intel 80x8x families: 8-, 16-, and 32-bit bus members
- The Motorola 68000 microprocessor family: 16- and 32-bit bus members

The system interface supports host-system memory addressing up to 32 bits (32-bit reach into the host-system memory). This allows greater flexibility in using/accessing host-system memory.

System designers are allowed to customize the system interface to their particular bus by:

- Programmable burst transfers or cycle-steal DMA operations
- Optional parity protection

These features are implemented in hardware to reduce system overhead, facilitate automatic rearbitration of the bus after a burst, or repeat a cycle when errors occur (parity or bus). Bus retries are also supported.

The system-interface hardware also includes features to enhance the integrity of the TMS380C26 and the data. These features include the following:

- Always internally maintain odd-byte parity regardless if parity is disabled
- Monitor for the presence of a clock failure

On every cycle, the system interface compares all the system clocks to a reference clock. If any of the clocks become invalid, the TMS380C26 enters the slow-clock mode, which prevents latch-up of the TMS380C26. If the SBCLK is invalid, any DMA cycle is terminated immediately; otherwise, the DMA cycle is completed and the TMS380C26 is placed in slow-clock mode.

system interface (SIF) (continued)

When the TMS380C26 enters the slow-clock mode, the clock that failed is replaced by a slow free-running clock and the device is placed into a low-power reset state. When the failed clock(s) return to valid operation, the TMS380C26 must be reinitialized.

Using DMA, a continuous transfer rate of 64 Mbits per second (8 MBps) can be obtained. For pseudo-DMA, a continuous transfer rate of 48 Mbps (6 MBps) can be obtained when using a 16-MHz clock. Since the main purpose of DIO is for downloading initialization, the DIO transfer rate is not a significant issue. For comparison, the ISA bus continuous DMA transfer is rated for approximately 23 Mbps.

memory interface (MIF)

The MIF performs the memory management to allow the TMS380C26 to address 2M bytes in local memory. Hardware in the MIF allows the TMS380C26 to be directly connected to DRAMs without additional circuitry. This glueless DRAM connection includes the DRAM refresh controller. The MIF also handles all internal bus arbitration between these blocks. When required, the MIF then arbitrates for the external bus.

The MIF is responsible for the memory mapping of the CPU of a task. The memory map of DRAMs, EPROMs, burned-in addresses (BIA), and external devices are appropriately addressed when required by the system interface (SIF), protocol handler (PH), or for a DMA transfer.

The memory interface is capable of a 64-Mbps continuous transfer rate when using a 4-MHz local bus (64-MHz device crystal).

protocol handler (PH)

The PH performs the hardware-based real-time protocol functions for a token-ring or Ethernet LAN. Network type is determined by TEST0 –TEST2. Token-ring network is determined by software and can be either 16 Mbps or 4 Mbps. These speeds are not fixed by the hardware but by the software.

The PH converts the parallel-transmit data to serial-network data of the appropriate coding and converts the received serial data to parallel data. The PH data-management state machines direct the transmission/reception of data to/from local memory through the MIF. The PH buffer-management state machines automatically oversee this process, directly sending / receiving linked lists of frames without CPU intervention.

The protocol handler contains many state machines which provide the following features:

- Transmit and receive frames
- Capture tokens (token ring)
- Provide token-priority controls (token ring)
- Automatic retry of frame transmissions after collisions (Ethernet)
- Implement the random exponential backoff algorithm (Ethernet)
- Manage the TMS380C26 buffer memory
- Provide frame-address recognition (group, specific, functional, and multicast)
- Provide internal parity protection
- Control and verify the physical-layer circuitry-interface signals

Integrity of the transmitted and received data is assured by cyclic redundancy checks (CRC), detection of network data violations, and parity on internal data paths. All data paths and registers are optionally parity-protected to assure functional integrity.

adapter support function (ASF)

The ASF performs support functions not contained in the other blocks. The features are:

- The TMS380C26 base timer
- Identification, management, and service of internal and external interrupts
- Test-pin mode control, including the unit-in-place mode for board testing
- Checks for illegal states, such as illegal opcodes and parity

clock generator (CG)

The CG performs the generation of all the clocks required by the other functional blocks including the local-memory-bus clocks (MBCLK1, MBCLK2). The CG also generates the reference clock to be sampled by the SIF to determine if the TMS380C26 needs to be placed into slow-clock mode. This reference clock is free floating in the range of 10 kHz–100 kHz.

user-accessible hardware registers and TMS380C26 internal pointers

The following tables show how to access internal data via pointers and how to address the registers in the host interface. The SIFACL register, which directly controls device operation, is described in detail.

NOTE:

The adapter-internal pointers table is defined only after TMS380C26 initialization and until the OPEN command is issued.

These pointers are defined by the TMS380C26 software (microcode), and this table describes the release 1.00 and 2.x software.

Adapter-Internal Pointers for Token Ring†

ADDRESS	DESCRIPTION
>00.FFF8‡	Pointer to software raw microcode level in chapter 0
>00.FFFA‡	Pointer to starting location of copyright notices. Copyright notices are separated by a >0A character and terminated by a >00 character in chapter 0.
>01.0A00	Pointer to burned-in address in chapter 1
>01.0A02	Pointer to software level in chapter 1
>01.0A04	Pointer to TMS380C26 addresses in chapter 1: Pointer + 0 node address Pointer + 6 group address Pointer + 10 functional address
>01.0A06	Pointer to TMS380C26 parameters in chapter 1: Pointer + 0 physical drop number Pointer + 4 upstream neighbor address Pointer + 10 upstream physical-drop number Pointer + 14 last ring-poll address Pointer + 20 reserved Pointer + 22 transmit access priority Pointer + 24 source class authorization Pointer + 26 last attention code Pointer + 28 source address of the last received frame Pointer + 34 last beacon type Pointer + 36 last major vector Pointer + 38 ring status Pointer + 40 soft-error timer value Pointer + 42 ring-interface error counter Pointer + 44 local ring number Pointer + 46 monitor error code Pointer + 48 last beacon-transmit type Pointer + 50 last beacon-receive type Pointer + 52 last MAC frame correlator Pointer + 54 last beaconing-station UNA Pointer + 60 reserved Pointer + 64 last beaconing-station physical drop number
>01.0A08	Pointer to MAC buffer (a special buffer used by the software to transmit adapter generated MAC frames) in chapter 1
>01.0A0A	Pointer to LLC counters in chapter 1: Pointer + 0 MAX_SAPs Pointer + 1 open SAPs Pointer + 2 MAX_STATIONs Pointer + 3 open stations Pointer + 4 available stations Pointer + 5 reserved
>01.0A0C	Pointer to 4-/16-Mbps word flag. If zero, 4 Mbps; if nonzero, the adapter is set to run at 16-Mbps data rate.
>01.0A0E	Pointer to total TMS380C26 RAM found in 1K bytes in RAM allocation test in chapter 1

† This table describes the pointers for release 1.00 and 2.x of the TMS380C26 software.
‡ This address valid only for microcode release 2.x.

Adapter-Internal Pointers for Ethernet†

ADDRESS	DESCRIPTION
>00.FFF8‡	Software raw microcode level in chapter 0
>00.FFFA‡	Pointer to starting location of copyright notices. Copyright notices are separated by a >0A character and terminated by a >00 character in chapter 0.
>01.0A00	Pointer to burned-in address in chapter 1
>01.0A02	Pointer to software level in chapter 1
>01.0A04	Pointer to TMS380C26 addresses in chapter 1: Pointer + 0 node address Pointer + 6 group address Pointer + 10 functional address
>01.0A08	Pointer to MAC buffer (a special buffer used by the software to transmit adapter generated MAC frames) in chapter 1
>01.0A0A	Pointer to LLC counters in chapter 1: Pointer + 0 MAX_SAPs Pointer + 1 open SAPs Pointer + 2 MAX_STATIONs Pointer + 3 open stations Pointer + 4 available stations Pointer + 5 reserved
>01.0A0C	Pointer to 4-/16-Mbps word flag. If zero, 4 Mbps; if nonzero, the adapter is set to run at 16-Mbps data rate.
>01.0A0E	Pointer to total TMS380C26 RAM found in 1K bytes in RAM allocation test in chapter 1

† This table describes the pointers for release 1.00 and 2.x of the TMS380C26 software.
‡ This address valid only for microcode release 2.x.

User-Access Hardware Registers

80x8x 16-BIT MODE: (SI / $\overline{M}$ = 1, S8 / $\overline{SHALT}$ = 0)†

WORD TRANSFERS			NORMAL MODE $\overline{SBHE}$ = 0 SRS2 = 0		PSEUDO-DMA MODE ACTIVE $\overline{SBHE}$ = 0 SRS2 = 0	
BYTE TRANSFERS			$\overline{SBHE}$ = 0 SRS2 = 1	$\overline{SBHE}$ = 1 SRS2 = 0	$\overline{SBHE}$ = 0 SRS2 = 1	$\overline{SBHE}$ = 1 SRS2 = 0
SRSX	SRS0	SRS1				
0	0	0	SIFDAT MSB	SIFDAT LSB	SDMADAT MSB	SDMADAT LSB
0	0	1	SIFDAT / INC MSB	SIFDAT / INC LSB	DMALEN MSB	DMALEN LSB
0	1	0	SIFADR MSB	SIFADR LSB	SDMAADR MSB	SDMAADR LSB
0	1	1	SIFCMD	SIFSTS	SDMAADX MSB	SDMAADX LSB
1	0	0	SIFACL MSB	SIFACL LSB	SIFACL MSB	SIFACL LSB
1	0	1	SIFADR MSB	SIFADR LSB	SIFADR MSB	SIFADR LSB
1	1	0	SIFADX MSB	SIFADX LSB	SIFADX MSB	SIFADX LSB
1	1	1	DMALEN MSB	DMALEN LSB	DMALEN MSB	DMALEN LSB

† $\overline{SBHE}$ = 1 and SRS2 = 1 are not defined

80x8x 8-BIT MODE: (SI / $\overline{M}$ = 1, S8/SHALT = 1)

SRSX	SRS0	SRS1	SRS2	NORMAL MODE $\overline{SBHE}$ = X	PSEUDO-DMA MODE ACTIVE $\overline{SBHE}$ = X
0	0	0	0	SIFDAT LSB	SDMADAT LSB
0	0	0	1	SIFDAT MSB	SDMADAT MSB
0	0	1	0	SIFDAT/INC LSB	DMALEN LSB
0	0	1	1	SIFDAT/INC MSB	DMALEN MSB
0	1	0	0	SIFADR LSB	SDMAADR LSB
0	1	0	1	SIFADR MSB	SDMAADR MSB
0	1	1	0	SIFSTS	SDMAADX LSB
0	1	1	1	SIFCMD	SDMAADX MSB
1	0	0	0	SIFACL LSB	SIFACL LSB
1	0	0	1	SIFACL MSB	SIFACL MSB
1	0	1	0	SIFADR LSB	SIFADR LSB
1	0	1	1	SIFADR MSB	SIFADR MSB
1	1	0	0	SIFADX LSB	SIFADX LSB
1	1	0	1	SIFADX MSB	SIFADX MSB
1	1	1	0	DMALEN LSB	DMALEN LSB
1	1	1	1	DMALEN MSB	DMALEN MSB

68xxx MODE: (SI/$\overline{M}$ = 0)‡

WORD TRANSFERS			NORMAL MODE $\overline{SUDS}$ = 0 $\overline{SLDS}$ = 0		PSEUDO-DMA MODE ACTIVE $\overline{SUDS}$ = 0 $\overline{SLDS}$ = 0	
BYTE TRANSFERS			$\overline{SUDS}$ = 0 $\overline{SLDS}$ = 1	$\overline{SUDS}$ = 1 $\overline{SLDS}$ = 0	$\overline{SUDS}$ = 0 $\overline{SLDS}$ = 1	$\overline{SUDS}$ = 1 $\overline{SLDS}$ = 0
SRSX	SRS0	SRS1				
0	0	0	SIFDAT MSB	SIFDAT LSB	SDMADAT MSB	SDMADAT LSB
0	0	1	SIFDAT/INC MSB	SIFDAT/INC LSB	DMALEN MSB	DMALEN LSB
0	1	0	SIFADR MSB	SIFADR LSB	SDMAADR MSB	SDMAADR LSB
0	1	1	SIFCMD	SIFSTS	SDMAADX MSB	SDMAADX LSB
1	0	0	SIFACL MSB	SIFACL LSB	SIFACL MSB	SIFACL LSB
1	0	1	SIFADR MSB	SIFADR LSB	SIFADR MSB	SIFADR LSB
1	1	0	SIFADX MSB	SIFADX LSB	SIFADX MSB	SIFADX LSB
1	1	1	DMALEN MSB	DMALEN LSB	DMALEN MSB	DMALEN LSB

‡ 68xxx mode is always 16 bit.

SIF adapter-control register (SIFACL)

The SIFACL register allows the host processor to control and to some extent reconfigure the TMS380C26 under software control.

SIFACL Register

Bit #	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	TEST0	TEST1	TEST2	—	SWHLDA	SWDDIR	SWHRQ	PSDMAEN	ARESET	CPHALT	BOOT	RESO	SINTEN	PEN	NSEL OUT0	NSEL OUT1
	R	R	R		RP–0	R–u	R–0	RS–0	RW–0	RP–b	RP–b	R	RW–1	RP–p	RP–0	RP–1

Legend:

R	=	Read
W	=	Write
P	=	Write during ARESET = 1 only
S	=	Set only
–n	=	Value after reset
b	=	Value on BTSTRP
p	=	Value on PRTYEN
u	=	Indeterminate

Bits 0–2: Value on TEST0 and TEST2 pins

These bits are read only and always reflect the value on the corresponding device pins. This allows the host S/W to determine the network type and speed configuration. If the network speed and type are software configurable, these bits can be used to determine which configurations are supported by the network hardware.

TEST0	TEST1	TEST2	Description
L	L	H	Reserved
L	H	H	16-Mbps token ring
H	L	H	Ethernet (802.3/blue book)
H	H	H	4-Mbps token ring
X	X	0	Reserved

Bit 3: **Reserved.** Read data is indeterminate.

Bit 4: SWHLDA — Software Hold Acknowledge

This bit allows the function of SHLDA / $\overline{\text{SBGR}}$ to be emulated from software control for pseudo-DMA mode.

PSDMAEN	SWHLDA	SWHRQ	RESULT
0†	X	X	SWHLDA value in the SIFACL register cannot be set to a one.
1†	0	0	No pseudo-DMA request pending
1†	0	1	Indicates a pseudo-DMA request interrupt
1†	1	X	Pseudo-DMA process in progress

† The value on SHLDA / $\overline{\text{SBGR}}$ is ignored.

Bit 5: **SWDDIR — Current SDDIR Signal Value**

This bit contains the current value of the pseudo-DMA direction. This enables the host to easily determine the direction of DMA transfers, which allows system DMA to be controlled by system software.

0 = Pseudo DMA from host system to TMS380C26
1 = Pseudo DMA from TMS380C26 to host system

Bit 6: **SWHRQ — Current SHRQ Signal Value**

This bit contains the current value on SHRQ/$\overline{\text{SBRQ}}$ when in Intel mode, and the inverse of the value on SHRQ/$\overline{\text{SBRQ}}$ when in Motorola mode. This enables the host to easily determine if a pseudo-DMA transfer is requested.

	INTEL MODE (SI/$\overline{\text{M}}$ = H)	MOTOROLA MODE (SI/$\overline{\text{M}}$ = L)
0 =	System bus not requested	System bus not requested
1 =	System bus requested	System bus requested

Bit 7: **PSDMAEN — Pseudo-System-DMA Enable**

This bit enables pseudo-DMA operation.

0 = Normal bus-master DMA operation is possible.
1 = Pseudo-DMA operation selected. Operation dependent on the values of the SWHLDA and SWHRQ bits in the SIFACL register.

Bit 8: **ARESET — Adapter Reset**

This bit is a hardware reset of the TMS380C26. This bit has the same effect as $\overline{\text{SRESET}}$ except that the DIO interface to the SIFACL register is maintained. This bit is set to 1 if a clock failure is detected (OSCIN, PXTALIN, RCLK, or SBCLK not valid).

0 = The TMS380C26 operates normally.
1 = The TMS380C26 is held in the reset condition.

Bit 9: **CPHALT — Communications-Processor Halt**

This bit controls the TMS380C26 processor access to the internal TMS380C26 buses. This prevents the TMS380C26 from executing instructions before the microcode has been downloaded.

0 = The TMS380C26 processor can access the internal TMS380C26 buses.
1 = The TMS380C26 processor is prevented from accessing the internal adapter buses.

Bit 10: **BOOT — Bootstrap CP Code**

This bit indicates whether the memory in chapters 0 and 31 of the local-memory space is RAM or ROM/PROM/EPROM. This bit controls the operation of $\overline{\text{MCAS}}$ and $\overline{\text{MROMEN}}$.

0 = ROM/PROM/EPROM memory in chapters 0 and 31
1 = RAM memory in chapters 0 and 31

Bit 11: **RES 0 — Reserved.** This bit must be set to 0.

Bit 12: **SINTEN — System-Interrupt Enable**

This bit allows the host processor to enable or disable system-interrupt requests from the TMS380C26. The system-interrupt request from the TMS380C26 is on SINTR/$\overline{\text{SIRQ}}$. The following equation shows how SINTR/$\overline{\text{SIRQ}}$ is driven. The table also explains the results of the states.

SINTR/$\overline{\text{SIRQ}}$ = (PSDMAEN * SWHRQ * !SWHLDA) + (SINTEN * SYSTEM_INTERRUPT)

PSDMAEN	SWHRQ	SWHLDA	SINTEN	SYSTEM INTERRUPT (SIFSTS REGISTER)	RESULT
1†	1	1	X	X	Pseudo DMA is active.
1†	1	0	X	X	The TMS380C26 generated a system interrupt for a pseudo DMA.
1†	0	0	X	X	Not a pseudo-DMA interrupt
X	X	X	1	1	The TMS380C26 generates a system interrupt.
0	X	X	1	0	The TMS380C26 does not generate a system interrupt.
0	X	X	0	X	The TMS380C26 cannot generate a system interrupt.

† The value on SHLDA / $\overline{\text{SBGR}}$ is ignored.

Bit 13: **PEN — Adapter-Parity Enable**

This bit determines whether data transfers within the TMS380C26 are checked for parity.

0 = Data transfers are not checked for parity.
1 = Data transfers are checked for correct odd parity.

Bit 14 – 15: **NSELOUT0, NSELOUT0 1 — Network-Selection Outputs**

The values in these bits control NSELOUT0 and NSELOUT1. These bits can be modified only while the ARESET bit is set.

These bits can be used to software configure a TMS380C26 as follows: NSELOUT0 and NSELOUT1 should be connected to TEST0 and TEST1, respectively (TEST2 should be left unconnected or tied high). NSELOUT0 should be used to select network speed and NSELOUT1 network type, as shown in the following table:

NSELOUT0	NSELOUT1	SELECTION
0	0	Reserved
0	1	16-Mbps token ring
1	0	Ethernet (802.3/blue book)
1	1	4-Mbps token ring

At power up, these bits are set corresponding to 16-Mbps token ring (NSELOUT1 = 1, NSELOUT0 = 0).

SIFACL control for pseudo-DMA operation

Pseudo DMA is software controlled by the use of five bits in the SIFACL register. The logic model for the SIFACL register control of pseudo-DMA operation is shown in Figure 2.

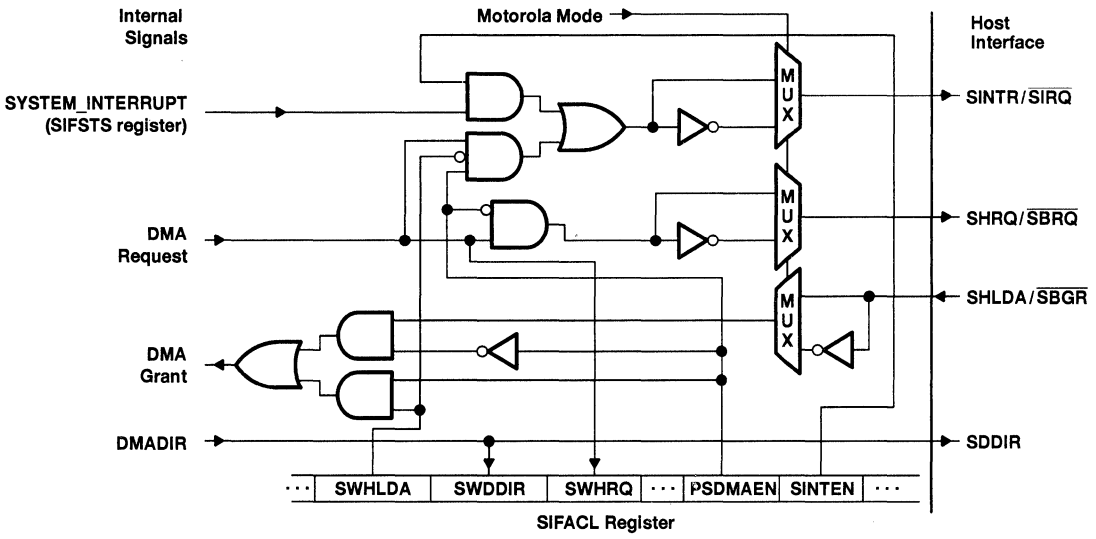


Figure 2. Pseudo-DMA Logic Related to SIFACL Bits

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 6) ..... 7 V
Input voltage range, V_I (see Note 6) ..... – 0.3 V to 20 V
Output voltage range ..... – 2 V to 7 V
Power dissipation ..... 0.9 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 6: Voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.75	5	5.25	V
V_{SS}	Supply voltage (see Note 7)		0	0	0	V
V_{IH}	High-level input voltage	TTL-level signal	2		V_{DD}+0.3	V
		OSCIN‡	2.6		V_{DD}+0.3	
		RCLK, PXTALIN, RCVR	2.6		V_{DD}+0.3	
V_{IL}	Low-level input voltage, TTL-level signal (see Note 8)	OSCIN§	–0.3		0.6	V
		All other	–0.3		0.8	
I_{OH}	High-level output current				–400	µA
I_{OL}	High-level output current (see Note 9)				2	mA
T_A	Operating free-air temperature		0		70	°C

‡ The minimum level specified is a result of the manufacturing test environment. This signal has been characterized to a minimum level of 2.4 V over the full temperature range.

§ The maximum level specified is a result of the manufacturing test environment. This signal has been characterized to a maximum level of 0.8 V over the full temperature range.

NOTES: 7. All V_{SS} pins should be routed to minimize inductance to system ground.
8. The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used for logic-voltage levels only.
9. Output current of 2 mA is sufficient to drive five low-power Schottky TTL loads or ten advanced low-power Schottky TTL loads (worst case).

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS¶		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, TTL-level signal (see Note 10)	V_{DD} = MIN,	I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage, TTL-level signal	V_{DD} = MIN,	I_{OL} = MAX			0.6	V
I_O	High-impedance output current	V_{DD} = MAX,	V_O = 2.4 V			20	µA
		V_{DD} = MAX,	V_O = 0.4 V			–20	
I_I	Input current, any input or input / output	V_I = V_{SS} to V_{DD}				±20	µA
I_{DD}	Supply current	V_{DD} = MAX				160	mA
C_i	Input capacitance, any input	f = 1 MHz,	Others at 0 V			15	pF
C_o	Output capacitance, any output or input/output	f = 1 MHz,	Others at 0 V			15	pF

¶ For conditions shown as MIN/MAX, use the appropriate value specified under the recommended operating conditions.

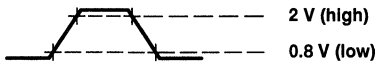
NOTE 10: The following signals require an external pullup resistor: SRAS/$\overline{\text{SAS}}$, $\overline{\text{SRDY}}$/$\overline{\text{SDTACK}}$, $\overline{\text{SRD}}$/$\overline{\text{SUDS}}$, $\overline{\text{SWR}}$/$\overline{\text{SLDS}}$, $\overline{\text{EXTINT0}}$–$\overline{\text{EXTINT3}}$, and $\overline{\text{MBRQ}}$.

PARAMETER MEASUREMENT INFORMATION

Outputs are driven to a minimum high-logic level of 2.4 V and to a maximum low-logic level of 0.6 V. These levels are compatible with TTL devices.

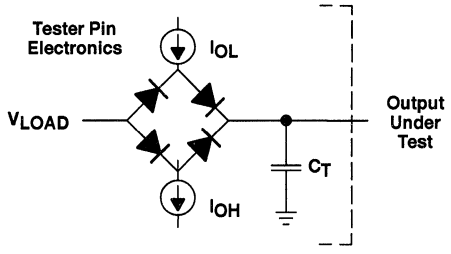
Output transition times are specified as follows: For a high-to-low transition on either an input or output signal, the level at which the signal is said to be no longer high is 2 V and the level at which the signal is said to be low is 0.8 V. For a low-to-high transition, the level at which the signal is said to be no longer low is 0.8 V and the level at which the signal is said to be high is 2 V, as shown below.

The rise and fall times are not specified but are assumed to be those of standard TTL devices, which are typically 1.5 ns.



test measurement

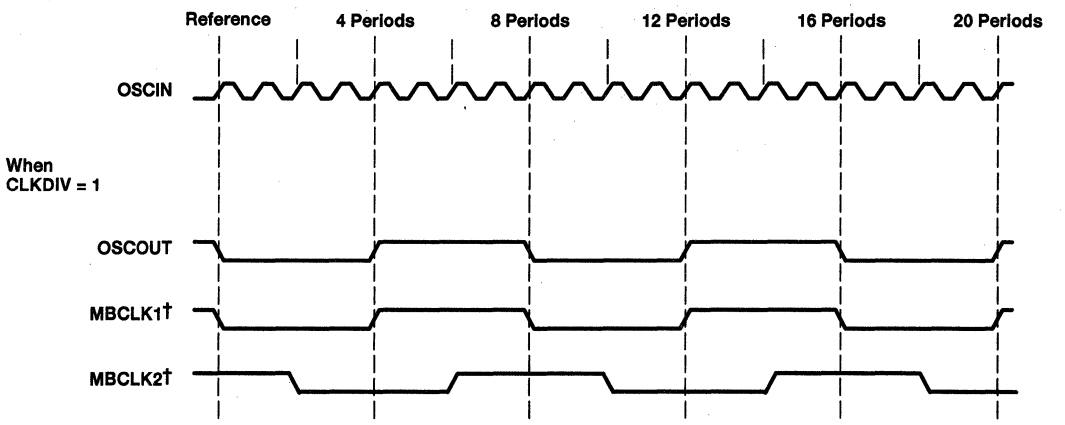
The test-load circuit shown in Figure 3 represents the programmable load of the tester pin electronics that are used to verify timing parameters of TI380C25 output signals.



Where: I_{OL} = 2 mA, dc-level verification (all outputs)
I_{OH} = 400 μA (all outputs)
V_{LOAD} = 1.5 V, typical dc-level verification or 0.7 V, typical timing verification
C_T = 65 pF, typical load-circuit capacitance

Figure 3. Test-Load Circuit

PARAMETER MEASUREMENT INFORMATION



† MBCLK1 and MBCLK2 have no timing relationship to OSCOUT. MBCLK1 and MBCLK2 can start on any OSCIN rising edge, depending on when the memory cycle starts execution.

Figure 4. Clock Waveforms After Clock Stabilization

PARAMETER MEASUREMENT INFORMATION

timing parameters

The timing parameters for all the signals of the TI380C25 are shown in the following tables and are illustrated in the accompanying figures. The purpose of these figures and tables is to quantify the timing relationships among the various signals. The parameters are numbered for convenience.

static signals

The following table lists signals that are not allowed to change dynamically and therefore have no timing associated with them. They should be strapped high or low as required.

SIGNAL	FUNCTION
SI/$\overline{M}$	Host-processor select (Intel/Motorola)
CLKDIV	Reserved
BTSTRP	Default-bootstrap mode (RAM/ROM)
PRTYEN	Default-parity select (enabled/disabled)
TEST0	Test pin indicates network type
TEST1	Test pin, indicator network type
TEST2	Test pin indicates network type
TEST3	Test pin for TI manufacturing test †
TEST4	Test pin for TI manufacturing test †
TEST5	Test pin for TI manufacturing test †

† For unit-in-place test

timing parameter symbology

Some timing parameter symbols have been created in accordance with JEDEC Standard 100-A. In order to shorten the symbols, some of the signal names and other related terminology have been abbreviated as shown below:

DR	DRVR	RS	$\overline{SRESET}$
DRN	$\overline{DRVR}$	VDD	V_{DDL}, V_{DD}
OSC	OSCIN		
SCK	SBCLK		

Lower case subscripts are defined as follows:

c	cycle time	r	rise time
d	delay time	sk	skew
h	hold time	su	setup time
w	pulse duration (width)	t	transition time

The following additional letters and phrases are defined as follows:

H	High	Z	High impedance
L	Low	Falling edge	No longer high
V	Valid	Rising edge	No longer low

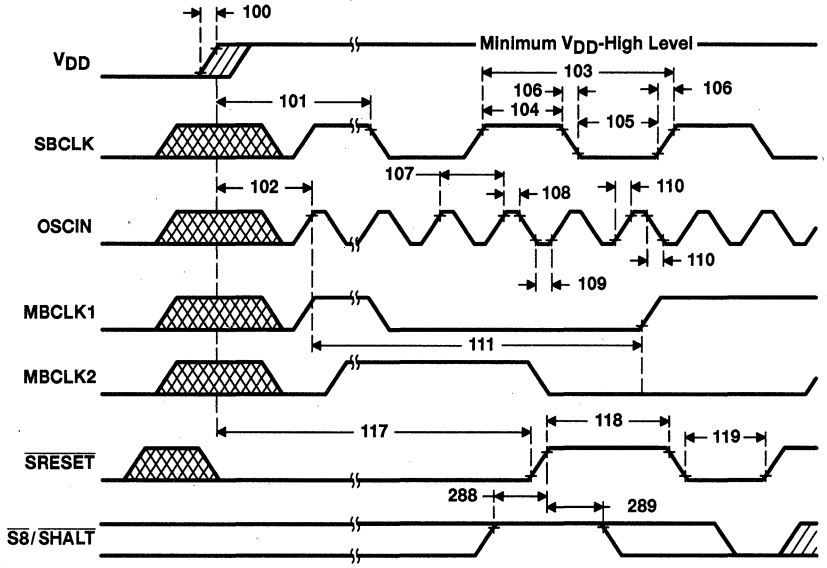
power up, SBCLK, OSCIN, MBCLK1, MBCLK2, $\overline{\text{SYNCIN}}$, and $\overline{\text{SRESET}}$ timing

NO.			MIN	MAX	UNIT
100†	$t_{r(VDD)}$	Rise time, 1.2 V to minimum V_{DD}-high level		1	ms
101†‡	$t_{d(VDDH-SCKV)}$	Delay time, minimum V_{DD}-high level to first valid SBCLK no longer high		1	ms
102†‡	$t_{d(VDDH-OSCV)}$	Delay time, minimum V_{DD}-high level to first valid OSCIN high		1	ms
103	$t_{c(SCK)}$	Cycle time, SBCLK	62.5		ns
104	$t_{w(SCKH)}$	Pulse duration, SBCLK high	26		ns
105	$t_{w(SCKL)}$	Pulse duration, SBCLK low	26		ns
106†	$t_{t(SCK)}$	Transition time, SBCLK		5	ns
107	$t_{c(OSC)}$	Cycle time, OSCIN (see Note 11)	15.6	500	ns
108	$t_{w(OSCH)}$	Pulse duration, OSCIN high	5.5		ns
109	$t_{w(OSCL)}$	Pulse duration, OSCIN low	5.5		ns
110†	$t_{t(OSC)}$	Transition time, OSCIN		3	ns
111†	$t_{d(OSCV-CKV)}$	Delay time, OSCIN valid to MBCLK1 and MBCLK2 valid		1	ms
117†	$t_{h(VDDH-RSL)}$	Hold time, $\overline{\text{SRESET}}$ low after V_{DD} reaches minimum high level	5		ms
118†	$t_{w(RSH)}$	Pulse duration, $\overline{\text{SRESET}}$ high	14		µs
119†	$t_{w(RSL)}$	Pulse duration, $\overline{\text{SRESET}}$ low	14		µs
288†	$t_{su(RST)}$	Setup time, DMA size to $\overline{\text{SRESET}}$ high (Intel mode only)	15		ns
289†	$t_{h(RST)}$	Hold time, DMA size from $\overline{\text{SRESET}}$ high (Intel mode only)	15		ns
	t_M	One-eighth of a local memory cycle	$2t_{c(OSC)}$		

† This specification is provided as an aid to board design.

‡ If parameter 101 or 102 cannot be met, parameter 117 must be extended by the larger difference: real value of parameter 101 or 102 minus the max value listed.

NOTE 11: If OSCIN is used to generate PXTALIN, the specification for the tolerance of OSCIN is equal to ± 0.01%.



NOTE A: In order to represent the information in one illustration, nonactual phase and timebase characteristics are shown. Refer to specified parameters for precise information.

Figure 5. Timing for Power Up, System Clocks, $\overline{\text{SYNCIN}}$, and $\overline{\text{SRESET}}$

memory-bus timing: clocks, $\overline{\text{MAL}}$, $\overline{\text{MROMEN}}$, $\overline{\text{MBIAEN}}$, $\overline{\text{NMI}}$, $\overline{\text{MRESET}}$, and ADDRESS

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum).

NO.		MIN	MAX	UNIT
1	Period of MBCLK1 and MBCLK2	$4t_M$		ns
2	Pulse duration, clock high	$2t_M-9$		ns
3	Pulse duration, clock low	$2t_M-9$		ns
4	Hold time, MBCLK2 low after MBCLK1 high	t_M-9		ns
5	Hold time, MBCLK1 high after MBCLK2 high	t_M-9		ns
6	Hold time, MBCLK2 high after MBCLK1 low	t_M-9		ns
7	Hold time, MBCLK1 low after MBCLK2 low	t_M-9		ns
8	Setup time, address/enable on MAX0, MAX2, and $\overline{\text{MROMEN}}$ before MBCLK1 no longer high	t_M-9		ns
9	Setup time, row address on MADL0–MADL7, MAXPH, and MAXPL before MBCLK1 no longer high	t_M-14		ns
10	Setup time, address on MADH0–MADH7 before MBCLK1 no longer high	t_M-14		ns
11	Setup time, $\overline{\text{MAL}}$ high before MBCLK1 no longer high	t_M-13		ns
12	Setup time, address on MAX0, MAX2, and $\overline{\text{MROMEN}}$ before MBCLK1 no longer low	$0.5t_M-9$		ns
13	Setup time, column address on MADL0–MADL7, MAXPH, and MAXPL before MBCLK1 no longer low	$0.5t_M-9$		ns
14	Setup time, status on MADH0–MADH7 before MBCLK1 no longer low	$0.5t_M-9$		ns
120	Setup time, $\overline{\text{NMI}}$ valid before MBCLK1 low	30		ns
121	Hold time, $\overline{\text{NMI}}$ valid after MBCLK1 low	0		ns
126	Delay time, MBCLK1 no longer low to $\overline{\text{MRESET}}$ valid	0	20	ns
129	Hold time, column address/status after MBCLK1 no longer low	t_M-7		ns

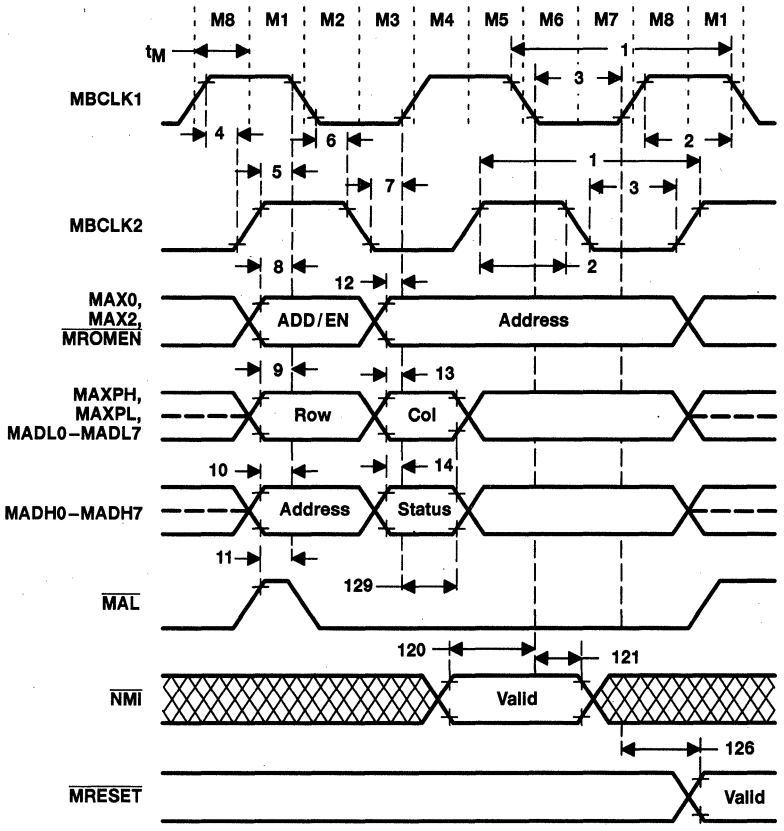


Figure 6. Memory-Bus Timing: Local-Memory Clocks, $\overline{\text{MAL}}$, $\overline{\text{MROMEN}}$, $\overline{\text{MBIAEN}}$, $\overline{\text{NMI}}$, $\overline{\text{MRESET}}$, and ADDRESS

memory-bus timing: clocks, $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, and $\overline{\text{MAL}}$ to ADDRESS

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum).

NO.		MIN	MAX	UNIT
15	Setup time, row address on MADL0–MADL7, MAXPH, and MAXPL before $\overline{\text{MRAS}}$ no longer high	$1.5t_M - 11.5$		ns
16	Hold time, row address on MADL0–MADL7, MAXPH, and MAXPL after $\overline{\text{MRAS}}$ no longer high	$t_M - 6.5$		ns
17	Delay time, $\overline{\text{MRAS}}$ no longer high to $\overline{\text{MRAS}}$ no longer high in the next memory cycle	$8t_M$		ns
18	Pulse duration, $\overline{\text{MRAS}}$ low	$4.5t_M - 9$		ns
19	Pulse duration, $\overline{\text{MRAS}}$ high	$3.5t_M - 9$		ns
20	Setup time, column address (MADL0–MADL7, MAXPH, and MAXPL) and status (MADH0–MADH7) before $\overline{\text{MCAS}}$ no longer high	$0.5t_M - 9$		ns
21	Hold time, column address (MADL0–MADL7, MAXPH, and MAXPL) and status (MADH0–MADH7) after $\overline{\text{MCAS}}$ low	$t_M - 9$		ns
22	Hold time, column address (MADL0–MADL7, MAXPH, and MAXPL) and status (MADH0–MADH7) after $\overline{\text{MRAS}}$ no longer high	$2.5t_M - 6.5$		ns
23	Pulse duration, $\overline{\text{MCAS}}$ low	$3t_M - 9$		ns
24	Pulse duration, $\overline{\text{MCAS}}$ high, refresh cycle follows read or write cycle	$2t_M - 9$		ns
25	Hold time, row address on MAXL0–MAXL7, MAXPH, and MAXPL after $\overline{\text{MAL}}$ low	$1.5t_M - 9$		ns
26	Setup time, row address on MAXL0–MAXL7, MAXPH, and MAXPL before $\overline{\text{MAL}}$ no longer high	$t_M - 9$		ns
27	Pulse duration, $\overline{\text{MAL}}$ high	$t_M - 9$		ns
28	Setup time, address/enable on MAX0, MAX2, and $\overline{\text{MROMEN}}$ before $\overline{\text{MAL}}$ no longer high	$t_M - 9$		ns
29	Hold time, address/enable of MAX0, MAX2, and $\overline{\text{MROMEN}}$ after $\overline{\text{MAL}}$ low	$1.5t_M - 9$		ns
30	Setup time, address on MADH0–MADH7 before $\overline{\text{MAL}}$ no longer high	$t_M - 9$		ns
31	Hold time, address on MADH0–MADH7 after $\overline{\text{MAL}}$ low	$1.5t_M - 9$		ns

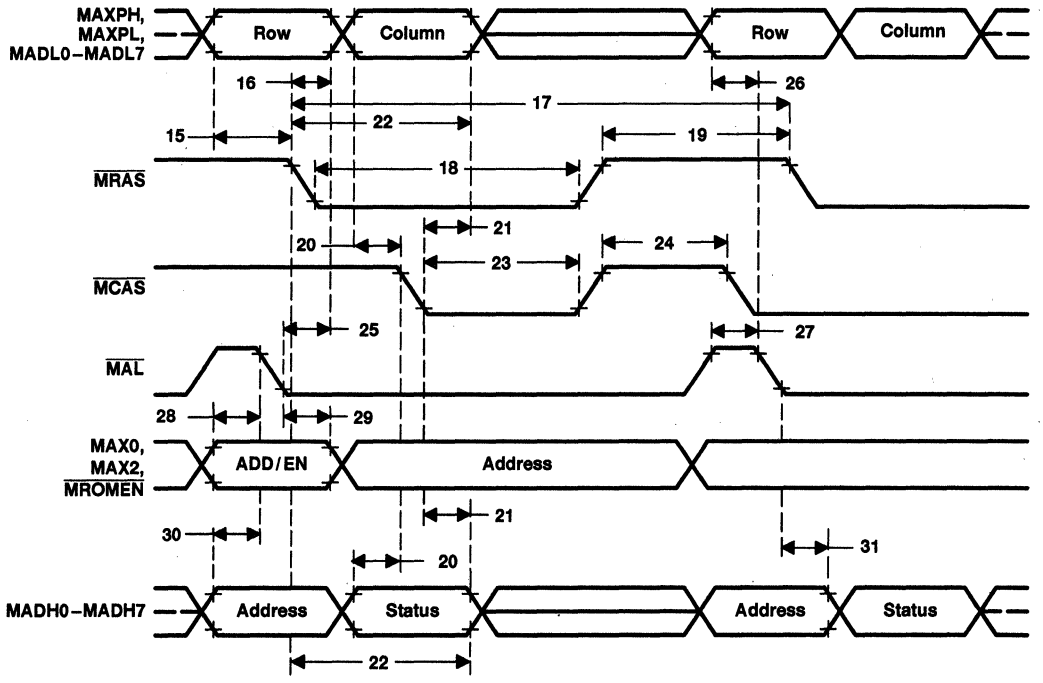


Figure 7. Memory-Bus Timing: Clocks, $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, and $\overline{\text{MAL}}$ to ADDRESS

memory-bus timing: read cycle

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum).

NO.		MIN	MAX	UNIT
32	Access time, address/enable valid on MAX0, MAX2, and $\overline{\text{MROMEN}}$ to valid data/parity		$6t_M - 23$	ns
33	Access time, address valid on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 to valid data/parity		$6t_M - 23$	ns
35	Access time, $\overline{\text{MRAS}}$ low to valid data/parity		$4.5t_M - 21.5$	ns
36	Hold time, valid data/parity after $\overline{\text{MRAS}}$ no longer low	0		ns
37†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7 and MADL0–MADL7 after $\overline{\text{MRAS}}$ high (see Note 12)	$2t_M - 10.5$		ns
38	Access time, $\overline{\text{MCAS}}$ low to valid data/parity		$3t_M - 23$	ns
39	Hold time, valid data/parity after $\overline{\text{MCAS}}$ no longer low	0		ns
40†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{\text{MCAS}}$ high (see Note 12)	$2t_M - 13$		ns
41	Delay time, $\overline{\text{MCAS}}$ no longer high to $\overline{\text{MOE}}$ low		$t_M + 13$	ns
42†	Setup time, address/status in the high-impedance state on MAXPH, MAXPL, MADL0–MADL7, and MADH0–MADH7 before $\overline{\text{MOE}}$ no longer high	0		ns
43	Access time, $\overline{\text{MOE}}$ low to valid data/parity		$2t_M - 25$	ns
44	Pulse duration, $\overline{\text{MOE}}$ low	$2t_M - 9$		ns
45	Delay time, $\overline{\text{MCAS}}$ low to $\overline{\text{MOE}}$ no longer low	$3t_M - 9$		ns
46	Hold time, valid data/parity in after $\overline{\text{MOE}}$ no longer low	0		ns
47†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{\text{MOE}}$ high (see Note 12)	$2t_M - 15$		ns
48†	Setup time, address/status in the high-impedance state on MAXPH, MAXPL, MADL0–MADL7, and MADH0–MADH7, before $\overline{\text{MBEN}}$ no longer high	0		ns
48a†	Setup time, address/status in the high-impedance state on MAXPH, MAXPL, MADL0–MADL7, and MADH0–MADH7 and before $\overline{\text{MBIAEN}}$ no longer high	0		ns
49	Access time, $\overline{\text{MBEN}}$ low to valid data/parity		$2t_M - 25$	ns
49a	Access time, $\overline{\text{MBIAEN}}$ low to valid data/parity		$2t_M - 25$	ns
50	Pulse duration, $\overline{\text{MBEN}}$ low	$2t_M - 9$		ns
50a	Pulse duration, $\overline{\text{MBIAEN}}$ low	$2t_M - 9$		ns
51	Hold time, valid data/parity after $\overline{\text{MBEN}}$ no longer low	0		ns
51a	Hold time, valid data/parity after $\overline{\text{MBIAEN}}$ no longer low	0		ns
52†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{\text{MBEN}}$ high (see Note 12)	$2t_M - 15$		ns
52a†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{\text{MBIAEN}}$ high	$2t_M - 15$		ns
53	Hold time, MDDIR high after $\overline{\text{MBEN}}$ high, read follows write cycle	$1.5t_M - 12$		ns
54	Setup time, MDDIR low before $\overline{\text{MBEN}}$ no longer high	$3t_M - 5$		ns
55	Hold time, MDDIR low after $\overline{\text{MBEN}}$ high, write follows read cycle	$3t_M - 12$		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.

NOTE 12: The data/parity that exists on the address lines most likely reaches the high-impedance state sometime later than the rising edge of $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, $\overline{\text{MOE}}$, or $\overline{\text{MBEN}}$ (between MIN and MAX of timing parameter 36) and is a function of the memory being read. The MIN time given represents the time from the rising edge of $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, $\overline{\text{MOE}}$, or $\overline{\text{MBEN}}$ to the beginning of the next address, and does not represent the actual high-impedance period on the address bus.

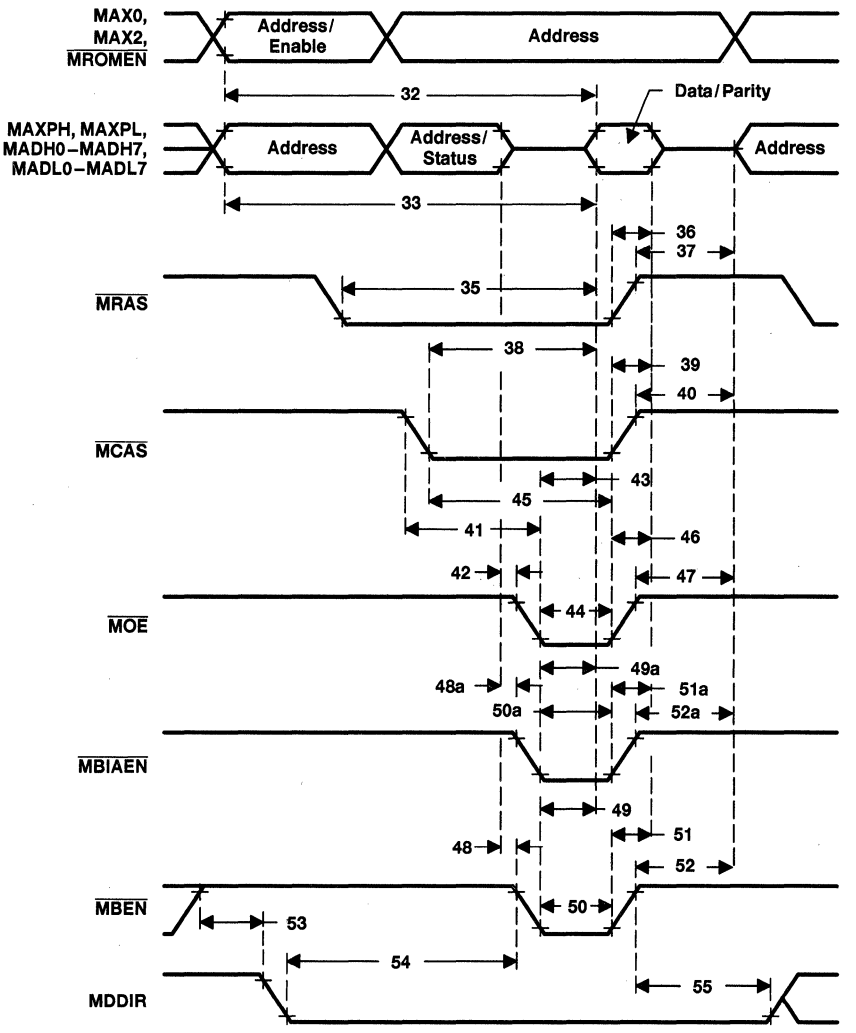


Figure 8. Memory-Bus Timing: Read Cycle

memory-bus timing: write cycle

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum).

NO.		MIN	MAX	UNIT
58	Setup time, $\overline{MW}$ low before $\overline{MRAS}$ no longer low	$1.5t_M - 9$		ns
60	Setup time, $\overline{MW}$ low before $\overline{MCAS}$ no longer low	$1.5t_M - 6.5$		ns
63	Setup time, valid data/parity before $\overline{MW}$ no longer high	$0.5t_M - 11.5$		ns
64	Pulse duration, $\overline{MW}$ low	$2.5t_M - 9$		ns
65	Hold time, data/parity out valid after $\overline{MW}$ high	$0.5t_M - 10.5$		ns
66	Setup time, address valid on MAX0, MAX2, and $\overline{MROMEN}$ before $\overline{MW}$ no longer low	$7t_M - 11.5$		ns
67	Hold time, $\overline{MRAS}$ low to $\overline{MW}$ no longer low	$5.5t_M - 9$		ns
69	Hold time, $\overline{MCAS}$ low to $\overline{MW}$ no longer low	$4t_M - 11.5$		ns
70	Setup time, $\overline{MBEN}$ low before $\overline{MW}$ no longer high	$1.5t_M - 13.5$		ns
71	Hold time, $\overline{MBEN}$ low after $\overline{MW}$ high	$0.5t_M - 6.5$		ns
72	Setup time, MDDIR high before $\overline{MBEN}$ no longer high	$2t_M - 9$		ns
73	Hold time, MDDIR high after $\overline{MBEN}$ high	$1.5t_M - 12$		ns

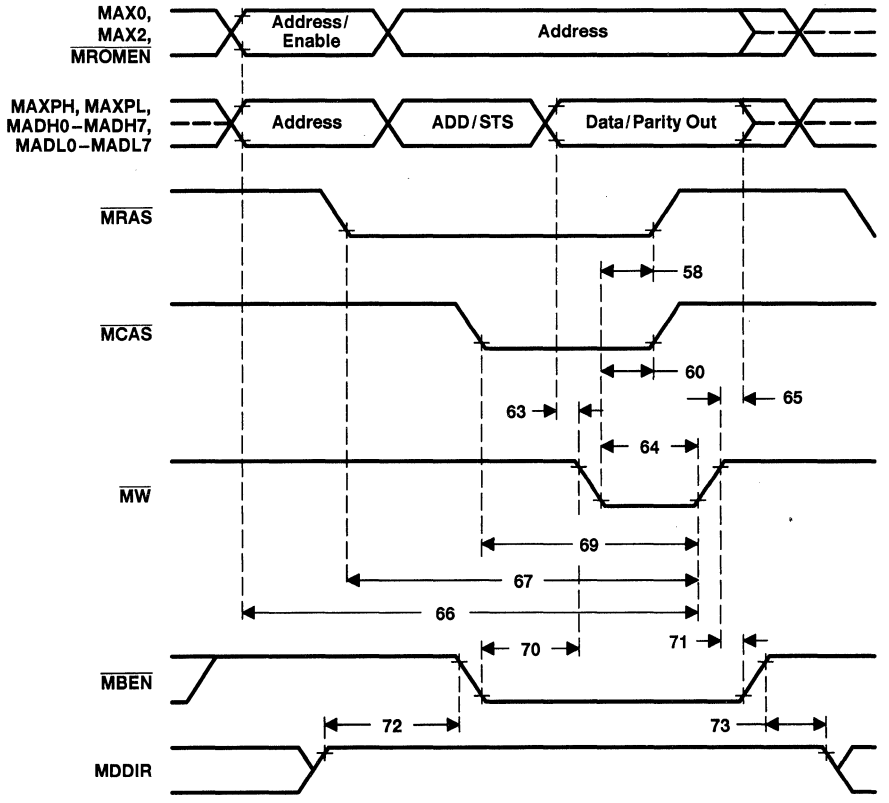


Figure 9. Memory-Bus Timing: Write Cycle

memory-bus timing: TMS380C26 releases control of bus

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum).

NO.		MIN	MAX	UNIT
74	Hold time, MIF after MBCLK1 rising edge, bus release	$0.5t_M - 13$		ns
74a	Hold time, $\overline{\text{MBEN}}$ valid after MBCLK1 rising edge, bus release	$t_M - 13$		ns
75	Delay time, MBCLK1 high to MIF in the high-impedance state, bus release		$0.5t_M$	ns
75a	Delay time, MBCLK1 high to $\overline{\text{MBEN}}$ in the high-impedance state, bus release		t_M	ns
76	Setup time, $\overline{\text{MBRQ}}$ low before MBCLK1 falling edge, bus release	24		ns
77	Hold time, $\overline{\text{MBRQ}}$ low after MBCLK1 low, bus release	0		ns
78	Setup time, $\overline{\text{MBGR}}$ low before MBCLK1 rising edge, bus release	29		ns

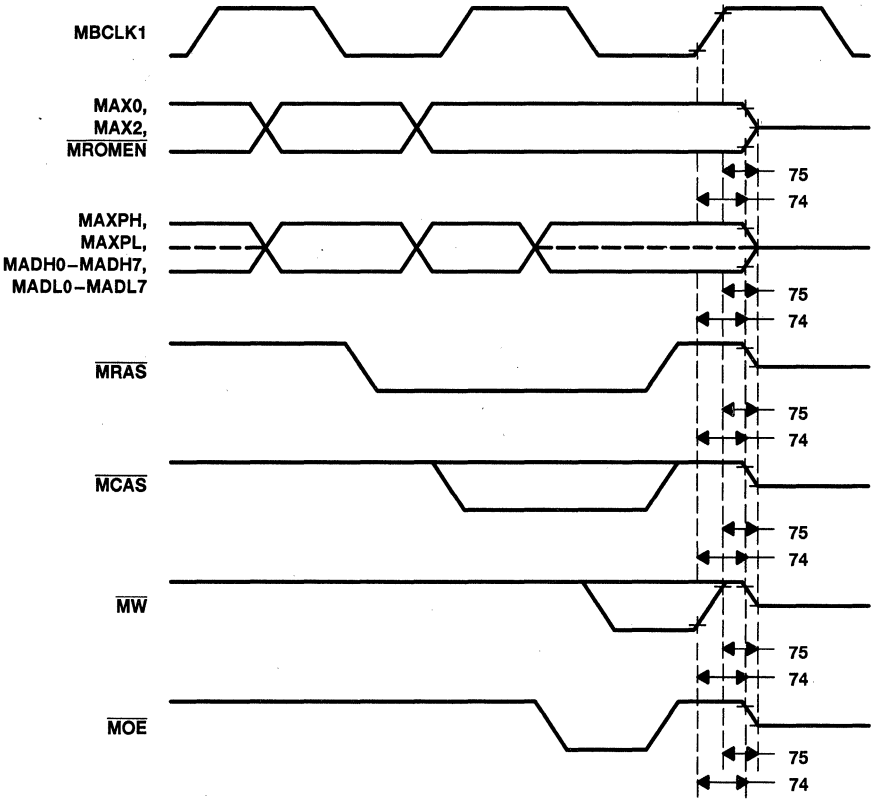


Figure 10. Memory-Bus Timing: TMS380C26 Releases Control of Bus

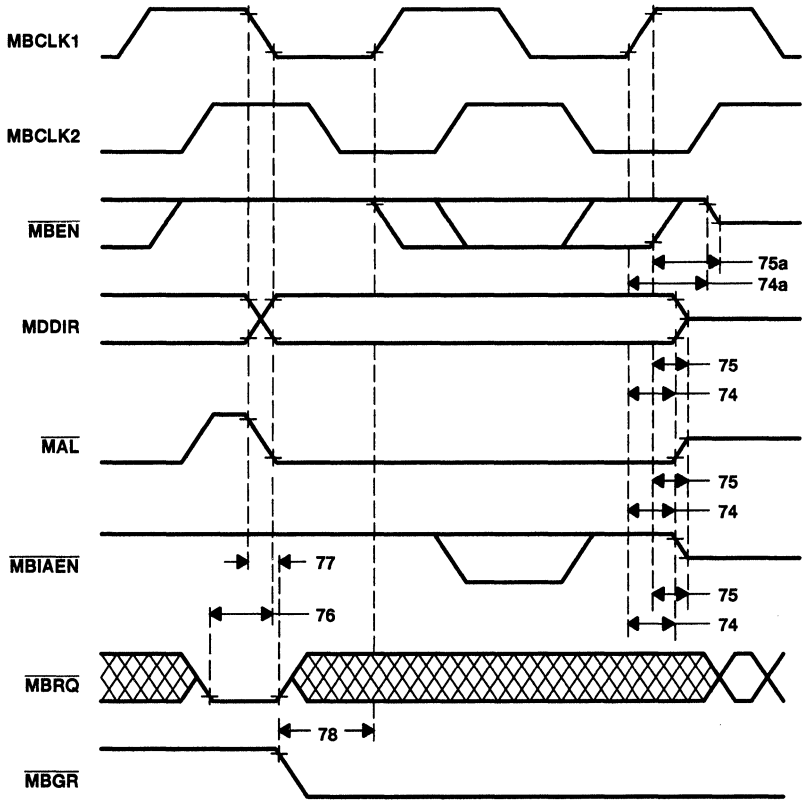


Figure 10. Memory-Bus Timing: TMS380C26 Releases Control of Bus (Continued)

memory-bus timing: TMS380C26 resumes control of bus

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum).

NO.		MIN	MAX	UNIT
79	Hold time, MIF in the high-impedance state after MBCKL1 rising edge, bus resume	$t_M - 13$		ns
80	Delay time, MBCLK1 high to MIF valid, bus resume		$t_M + 9$	ns
91	Setup time, $\overline{\text{MBRQ}}$ valid before MBCLK1 falling edge, bus resume	24		ns
82	Hold time, $\overline{\text{MBRQ}}$ valid after MBCLK1 low, bus resume	0		ns
83	Setup time, $\overline{\text{MBGR}}$ high before MBCLK1 rising edge, bus resume	29		ns

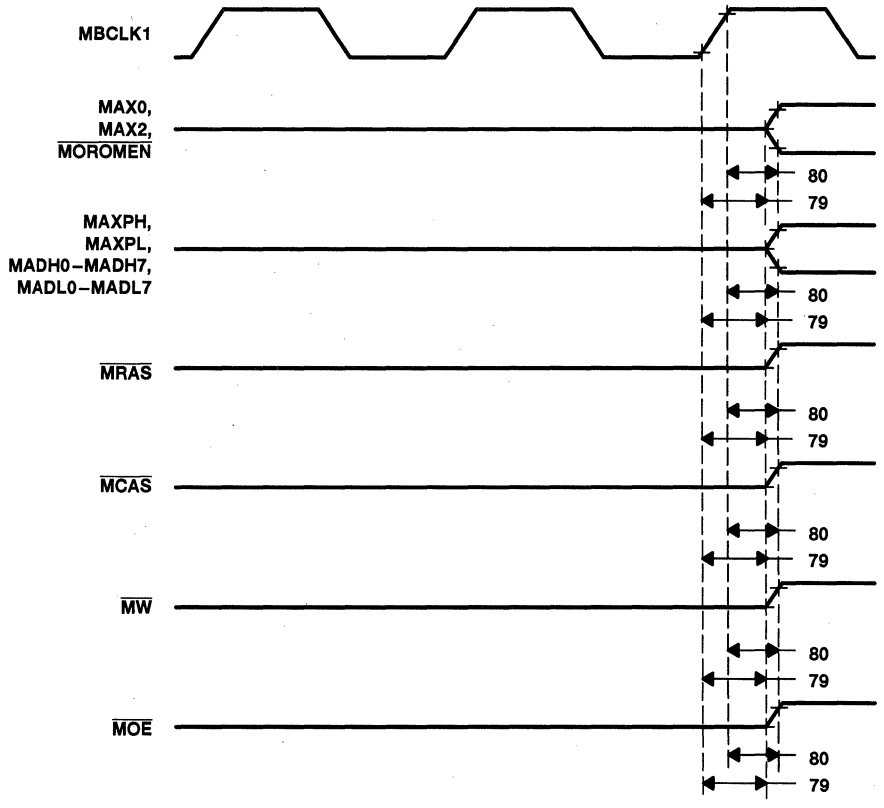


Figure 11. Memory-Bus Timing: TMS380C26 Resumes Control of Bus

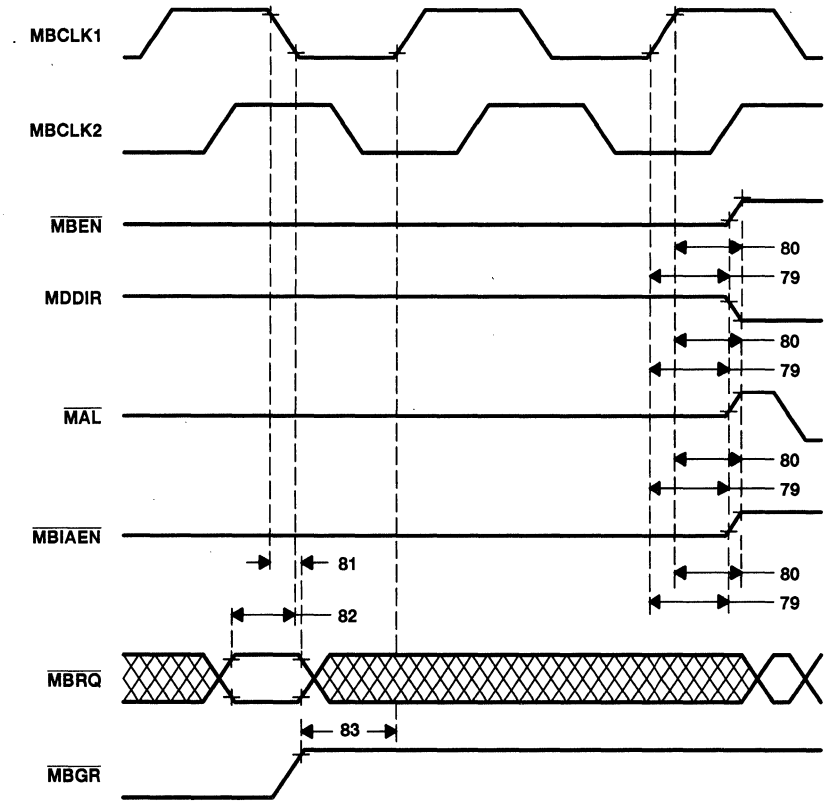


Figure 11. Memory-Bus Timing: TMS380C26 Resumes Control of Bus (Continued)

memory-bus timing: external bus-master read from TMS380C26

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum).

NO.		MIN	MAX	UNIT
84	Setup time, address on MAX0 and MAX2 before MBCLK1 falling edge, external bus-master access	21		ns
85	Hold time, address on MAX0 and MAX2 after MBCLK1 low, external bus-master access	0		ns
86	Setup time, valid address before MBCLK1 falling edge, external bus-master access	21		ns
87	Hold time, valid address after MBCLK1 low, external bus-master access	0		ns
88	Setup time, address in the high-impedance state before MBCLK1 falling edge, external bus-master read	0		ns
89	Setup time, data/parity valid before MBCLK2 falling edge, external bus-master read	$1.5t_M - 17^\dagger$		ns
90	Hold time, valid data/parity after MBCLK2 low, external bus-master read	$t_M - 13$		ns
91	Setup time, data/parity in the high-impedance state before MBCLK2 rising edge, external bus-master read	$t_M - 9$		ns
92	Setup time, MDDIR low before MBCLK2 falling edge, external bus-master read	21		ns
93	Hold time, MDDIR low after MBCLK2 low, external bus-master read	0		ns
94	Setup time, $\overline{\text{MACS}}$ low before MBCLK2 falling edge, external bus-master read	21		ns
95	Hold time, $\overline{\text{MACS}}$ low after MBCLK2 low, external bus-master read	0		ns

† This specification has been characterized to meet stated value.

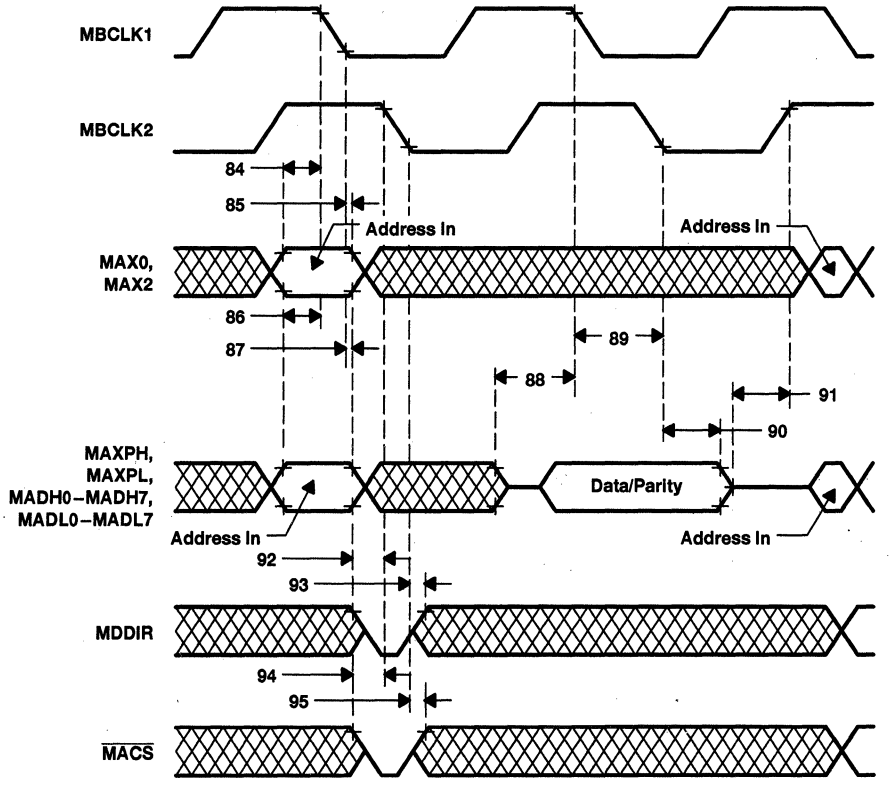


Figure 12. Memory-Bus Timing: External Bus-Master Read From TMS380C26

memory-bus timing: external bus-master write to TMS380C26

NO.		MIN	MAX	UNIT
96	Setup time, valid data/parity before MBCLK2 falling edge, external bus-master write	21		ns
97	Hold time, valid data/parity after MBCLK2 low, external bus-master write	0		ns
98	Setup time, MDDIR high before MBCLK2 falling edge, external bus-master write	21		ns
99	Hold time, MDDIR high after MBCLK2 low, external bus-master write	0		ns

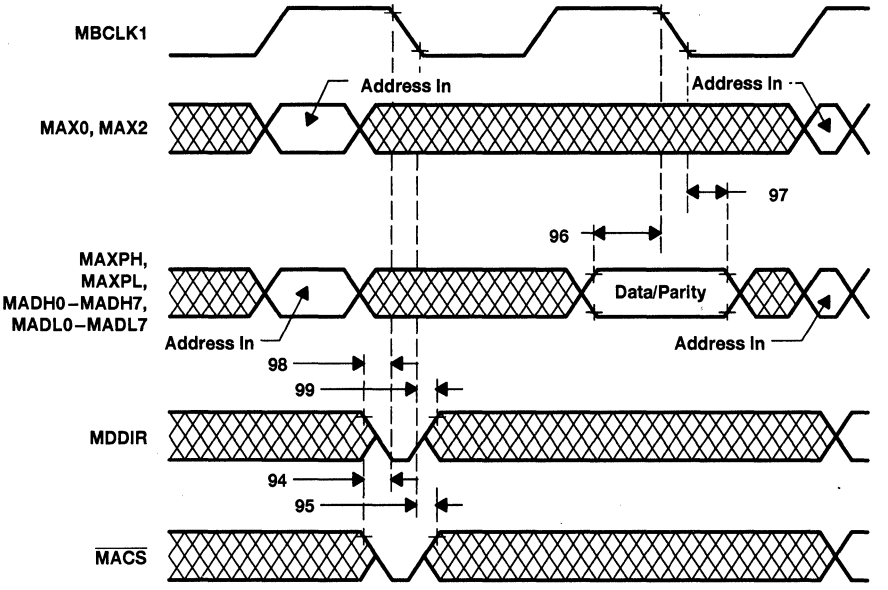


Figure 13. Memory-Bus Timing: External Bus-Master Write to TMS380C26

memory-bus timing: DRAM-refresh timing

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum).

NO.		MIN	MAX	UNIT
15	Setup time, row address on MADL0–MADL7, MAXPH, and MAXPL before $\overline{MRAS}$ no longer high	$1.5t_M-11.5$		ns
16	Hold time, row address on MADL0–MADL7, MAXPH, and MAXPL after $\overline{MRAS}$ no longer high	$t_M-6.5$		ns
18	Pulse duration, $\overline{MRAS}$ low	$4.5t_M-9$		ns
19	Pulse duration, $\overline{MRAS}$ high	$3.5t_M-9$		ns
73a	Setup time, $\overline{MCAS}$ low before $\overline{MRAS}$ no longer high	$1.5t_M-11.5$		ns
73b	Hold time, $\overline{MCAS}$ low after $\overline{MRAS}$ low	$4.5t_M-6.5$		ns
73c	Setup time, MREF high before $\overline{MCAS}$ no longer high	14		ns
73d	Hold time, MREF high after $\overline{MCAS}$ high	t_M-9		ns

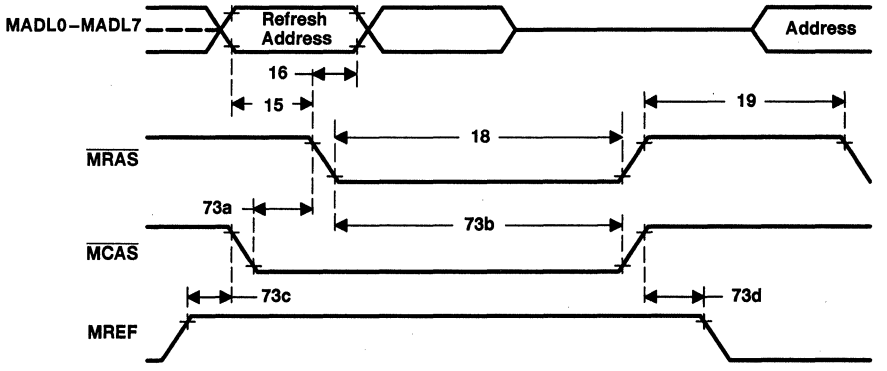


Figure 14. Memory-Bus Timing: DRAM-Refresh Cycle

XMATCH and XFAIL timing

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum).

NO.		MIN	MAX	UNIT
127	Delay time, status bit 7 high to XMATCH and XFAIL recognized	$7t_M$		ns
128	Pulse duration, XMATCH or XFAIL high	50		ns

Figure 15. XMATCH and XFAIL Timing

token ring – ring-interface timing

NO.			MIN	TYP	MAX	UNIT
153	Period of RCLK (see Note 13)	4 Mbps		125		ns
		16 Mbps		31.25		ns
154L	Pulse duration, RCLK low	4 Mbps nominal: 62.5 ns	46			ns
		16 Mbps nominal: 15.625 ns	15			ns
154H	Pulse duration, RCLK high	4 Mbps nominal: 62.5 ns	35			ns
		16 Mbps nominal: 15.625 ns	8			ns
155	Setup time, RCVR valid before rising edge (1.8 V) of RCLK at 16 Mbps		10			ns
156	Hold time, RCVR valid after rising edge (1.8 V) of RCLK at 16 Mbps		4			ns
158L	Pulse duration, ring baud clock low	4 Mbps	40			ns
		16 Mbps	8			ns
158H	Pulse duration, ring baud clock high	4 Mbps	40			ns
		16 Mbps	8			ns
165	Period of OSCOUT and PXTALIN (see Note 13)	4 Mbps		125		ns
		16 Mbps (for PXTALIN only)		31.25		ns
166	Tolerance of PXTALIN input frequency (see Note 13)				± 0.01	%

NOTE 13: This parameter is not tested but is required by the IEEE 802.5 specification.

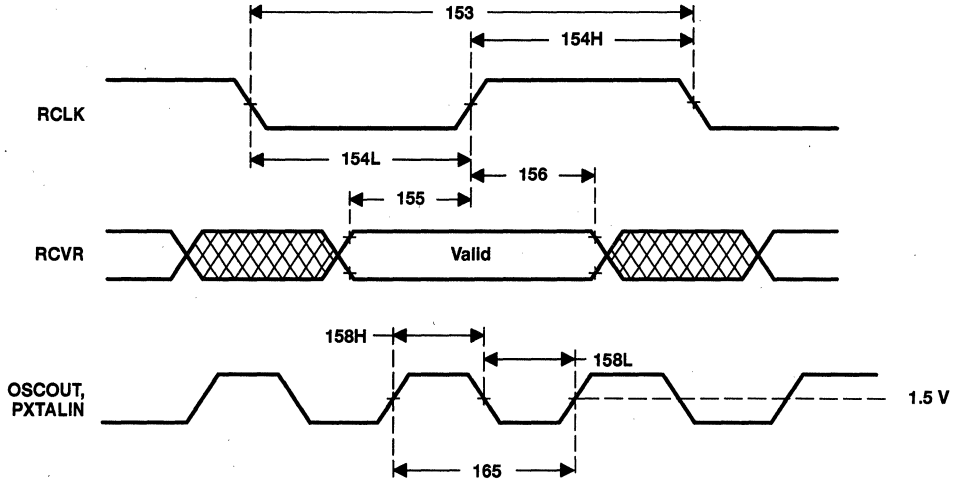


Figure 16. Token Ring – Ring-Interface Timing

token ring – transmitter timing

NO.			MIN	MAX	UNIT
159	$t_{sk(DR)}$	Delay time, DRVR rising edge (1.8 V) to $\overline{DRVR}$ falling edge (1 V) or DRVR falling edge (1 V) to $\overline{DRVR}$ rising edge (1.8 V)		±2	ns
160	$t_{d(DR)H}$†	Delay time, RCLK (or PXTALIN) falling edge (1 V) to DRVR rising edge (1.8 V)	See Note 14		ns
161	$t_{d(DR)L}$†	Delay time, RCLK (or PXTALIN) falling edge (1 V) to DRVR falling edge (1 V)	See Note 14		ns
162	$t_{d(DRN)H}$†	Delay time, RCLK (or PXTALIN) falling edge (1 V) to $\overline{DRVR}$ falling edge (1 V)	See Note 14		ns
163	$t_{(DRN)L}$†	Delay time, RCLK (or PXTALIN) falling edge (1 V) to $\overline{DRVR}$ rising edge (1.8 V)	See Note 14		ns
164	DRVR / $\overline{DRVR}$ asymmetry	$\frac{t_{d(DR)L} + t_{d(DRN)H}}{2} - \frac{t_{d(DR)H} + t_{d(DRN)L}}{2}$		±1.5	ns

† When in active-monitor mode, the clock source is PXTALIN; otherwise, the clock source is either RCLK or PXTALIN.
NOTE 14: This parameter is not tested to a minimum or a maximum but is measured and used as a component required for parameter 164.

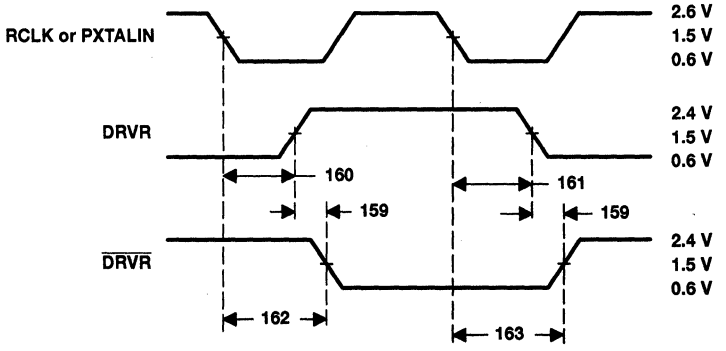


Figure 17. Skew and Asymmetry From RCLK or PXTALIN to DRVR and $\overline{DRVR}$

ethernet timing of clock signals

NO.			MIN	MAX	UNIT
300	CLKPHS	Pulse duration, TXC	45		ns
301	CLKPER	Cycle time, TXC	95	1000	ns

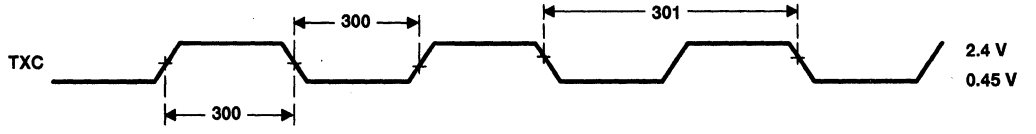


Figure 18. Ethernet Timing of Clock Signals

ethernet timing of XMIT signals

NO.			MIN	MAX	UNIT
305	t_{XDHLD}	Hold time, TXD after TXC high	5		ns
306	t_{XDVLD}	Delay time, TXC high to TXD valid and delay time, TXC high to TXEN high		40	ns

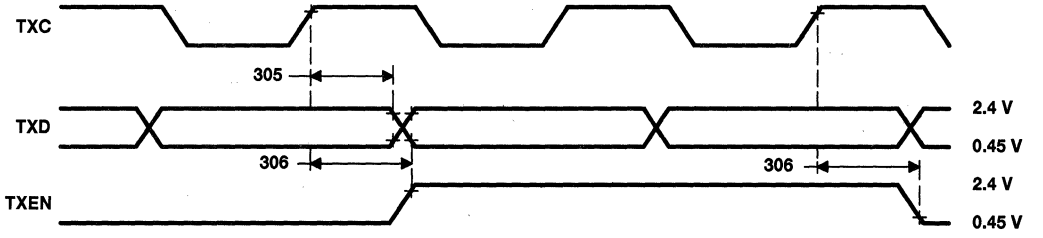


Figure 19. Ethernet Timing of XMIT Signals

ethernet timing of RCV signals – start of frame

NO.			MIN	TYP	MAX	UNIT
310	RXDSET	Setup time, RXD before RXC no longer low	20			ns
311	RXDHLD	Hold time, RXD after RXC high	5			ns
312	CRSSET	Setup time, CRS high before RXC no longer low for first valid data sample	20			ns
313	SAMDLY	Delay time, CRS internally recognized to first valid data sample (see Notes 15 and 16)		3		clk cycles
314	RXCHI	Pulse duration, RXC high	36			ns
315	RXCLO	Pulse duration, RXC low	36			ns

NOTES: 15. For valid frame synchronization one of the following data sequences must be received. Any other pattern delays frame synchronization until after the next CRS rising edge.
a) 0n(10) 11 where n is an integer and n is greater than or equal to 3
b) 10n(10) 11
16. If a previous frame or frame fragment is completed without extra RXC clock cycles (XTRCVC = 0), SAMDLY = 2 clock cycles.

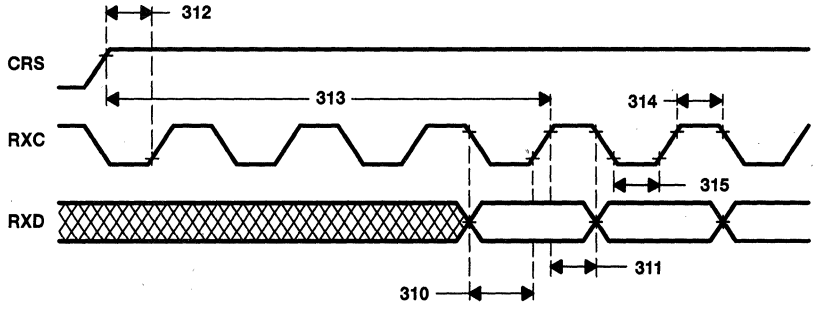


Figure 20. Ethernet Timing of RCV Signals – Start of Frame

ethernet timing of RCV signals – end of frame

NO.			MIN	TYP	MAX	UNIT
320	CRSSET	Setup time, CRS low before RXC no longer low, to determine if last data bit seen on previous RXC no longer low (see Note 17)	20			ns
321	CRSHLD	Hold time, CRS low after RXC no longer low, to determine if last data bit seen on previous RXC no longer low	0			ns
322	XTRCYC	Number of extra RXC clock cycles after last data bit (CRS is low) (see Note 17)	0	5		cycle

NOTE 17: TMS380C26 operates correctly even with no extra RXC clock cycles, provided that CRS does not remain asserted longer than 2 μs (see timing spec NDRXC). Providing no extra clocks affect receive-startup timing, see timing spec SAMDLY.

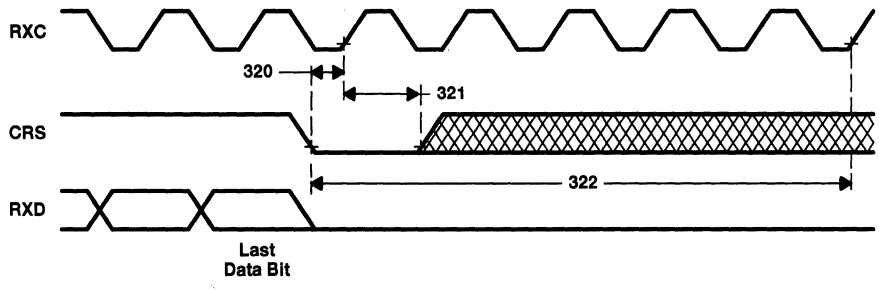


Figure 21. Ethernet Timing of RCV Signals – End of Frame

ethernet timing of RCV signals – no RXC

NO.			MIN	MAX	UNIT
330	NORXC	Time with no clock pulse on RXC, when CRS is high (see Note 18)		2	μs

NOTE 18: If NORXC is exceeded, local-clock-failure circuitry can become activated, resetting the device.

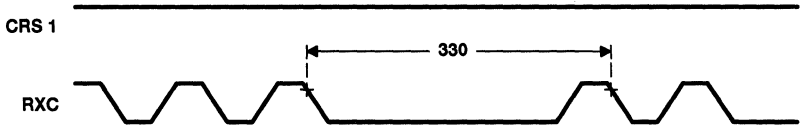


Figure 22. Ethernet Timing of RCV Signals – No RXC

ethernet timing of XMIT signals

NO.			MIN	TYP	MAX	UNIT
340	HBWIN	Delay time, TXC high of the last transmitted data bit (TXEN is high) to COLL sampled high, so not to generate a heart-beat error			47	cycles
341	COLPUL	Minimum pulse duration, COLL high for specified sample		20 ns + 1 cycle		ns
342	COLSET	Setup time, COLL high to TXC high		20		ns

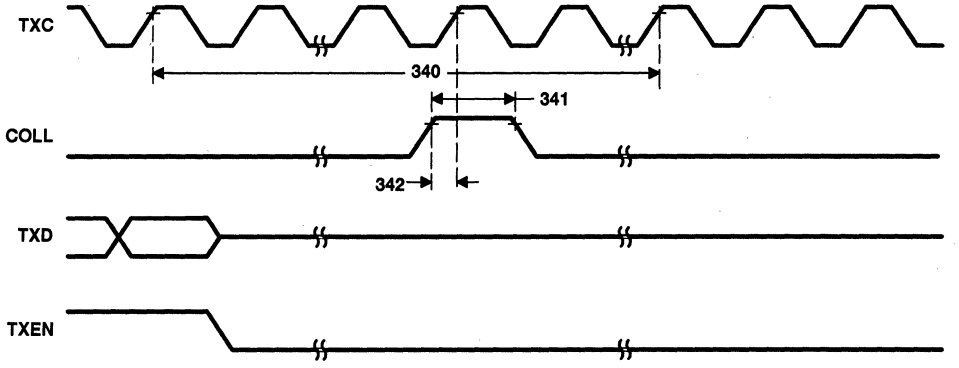


Figure 23. Ethernet Timing of XMIT Signals

ethernet timing of XMIT signals

NO.			MIN	TYP	MAX	UNIT
350	JAMTIM	Time from COLL sampled high (TXC high) to first transmitted JAM bit on TXD (see Note 19)			4	cycles
351	COLSET	Setup time, COLL high before TXC high		20		ns
352	COLPUL	Minimum pulse duration, COLL high for specified sample		20 ns + 1 cycle		ns

NOTE 19: The JAM pattern is delayed until after the completion of the preamble pattern. The TMS380C26 transmits a JAM pattern of all 1s.

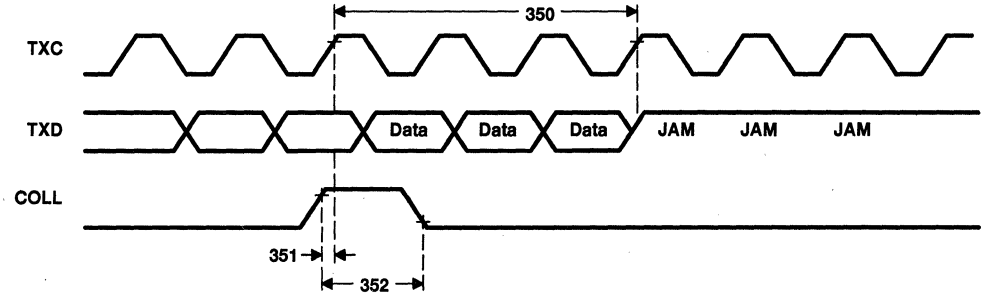


Figure 24. Ethernet Timing of XMIT Signals: JAM

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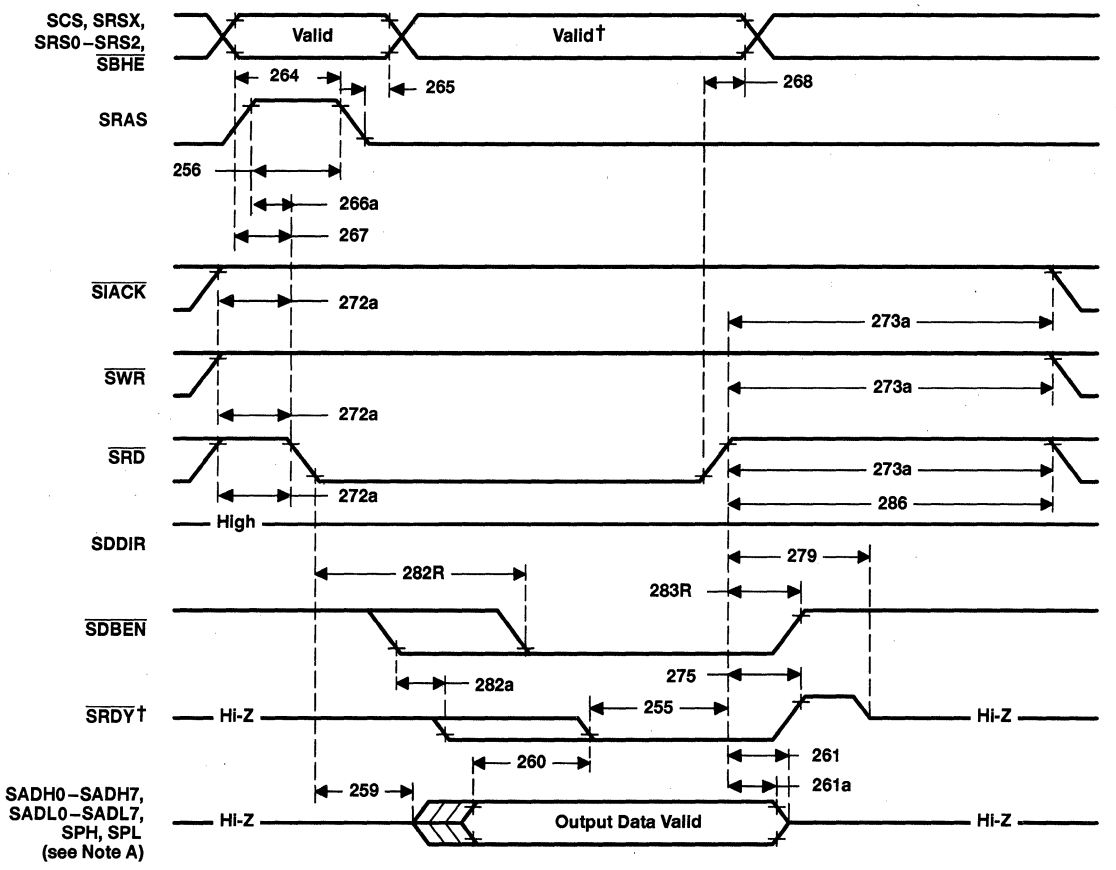
80x8x-DIO read-cycle timing

NO.		MIN	MAX	UNIT
255	Delay time, $\overline{SRDY}$ low to either $\overline{SCS}$ or $\overline{SRD}$ high	15		ns
256	Pulse duration, SRAS high	30		ns
259†	Hold time, SAD in the high-impedance state after $\overline{SRD}$ low (see Note 20)	0		ns
260	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before $\overline{SRDY}$ low	0		ns
261†	Delay time, $\overline{SRD}$ or $\overline{SCS}$ high to SAD in the high-impedance state (see Note 20)	0	35	ns
261a	Hold time, output data valid after $\overline{SRD}$ or $\overline{SCS}$ high (see Note 20)	0		ns
264	Setup time, SRSX, SRS0–SRS2, $\overline{SCS}$, and $\overline{SBHE}$ valid to SRAS no longer high (see Note 21)	30		ns
265	Hold time, SRSX, SRS0–SRS2, $\overline{SCS}$, and $\overline{SBHE}$ valid after SRAS low	10		ns
266a	Setup time, SRAS high to $\overline{SRD}$ no longer high (see Note 21)	15		ns
267‡	Setup time, SRSX, SRS0–SRS2 valid before $\overline{SRD}$ no longer high (see Note 20)	15		ns
268	Hold time, SRSX, SRS0–SRS2 valid after $\overline{SRD}$ no longer low (see Note 21)	0		ns
272a	Setup time, $\overline{SRD}$, $\overline{SWR}$, and $\overline{SIACK}$ high from previous cycle to $\overline{SRD}$ no longer high	55		ns
273a	Hold time, $\overline{SRD}$, $\overline{SWR}$, and $\overline{SIACK}$ high after $\overline{SRD}$ high	55		ns
275	Delay time, $\overline{SRD}$ and $\overline{SWR}$, or $\overline{SCS}$ high to $\overline{SRDY}$ high (see Note 20)	0	35	ns
279†	Delay time, $\overline{SRD}$ and $\overline{SWR}$, high to $\overline{SRDY}$ in the high-impedance state	0	65	ns
282a	Delay time, $\overline{SDBEN}$ low to $\overline{SRDY}$ low in a read cycle	0	35	ns
282R	Delay time, $\overline{SRD}$ low to $\overline{SDBEN}$ low (see *TMS380 Second Generation Token-Ring User's Guide*, SPWU005, subsection 3.4.1.1.1), provided previous cycle completed	0	55	ns
283R	Delay time, $\overline{SRD}$ high to $\overline{SDBEN}$ high (see Note 20)	0	35	ns
286	Pulse duration, $\overline{SRD}$ high between DIO accesses (see Note 20)	55		ns

† This specification is provided as an aid to board design. It is not assured during manufacturing testing.
‡ It is the later of $\overline{SRD}$ and $\overline{SWR}$ or $\overline{SCS}$ low that indicates the start of the cycle.

NOTES: 20. The inactive chip select is $\overline{SIACK}$ in DIO read and DIO write cycles, and $\overline{SCS}$ is the inactive chip select in interrupt-acknowledge cycles.

21. In 80x8x mode, SRAS can be used to strobe the values of $\overline{SBHE}$, SRSX, SRS0 – SRS2, and $\overline{SCS}$. When used to do so, SRAS must meet parameter 266a, and $\overline{SBHE}$, SRS0–SRS2, and $\overline{SCS}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.



† When the TMS380C25 begins to drive $\overline{\text{SDBEN}}$ inactive, it has already latched the write data internally. Parameter 263 must be met to the input of the data buffers.

NOTES: A. In 8-bit 80x8x mode DIO reads, the SADH0–SADH7 contain don't care data.

B. In 80x8x mode, SRAS can be used to strobe the values of $\overline{\text{SBHE}}$, SRSX, SRS0–SRS2, and $\overline{\text{SCS}}$. When used to do so, SRAS must meet parameter 266a, and $\overline{\text{SBHE}}$, SRS0–SRS2, and $\overline{\text{SCS}}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.

Figure 25. 80x8x-DIO Read-Cycle Timing

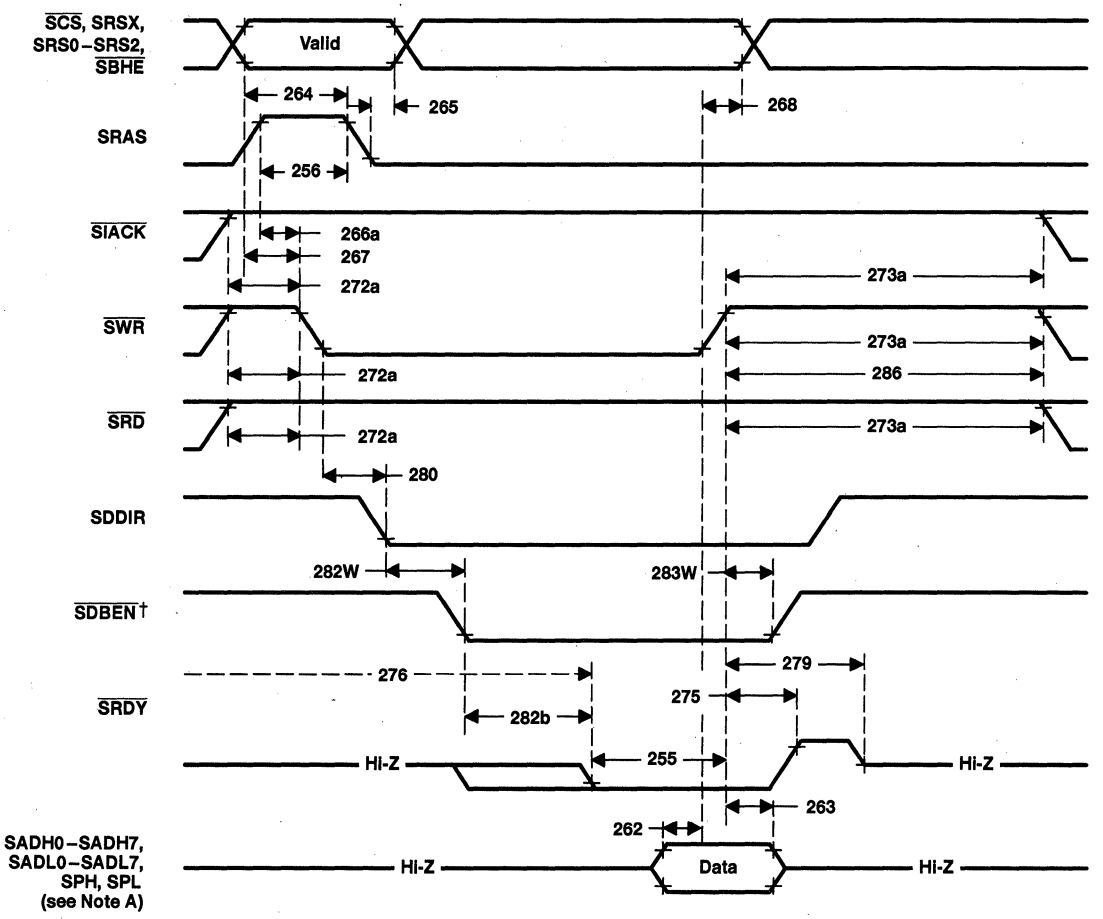
80x8x-DIO write-cycle timing

NO.			MIN	MAX	UNIT
255	Delay time, $\overline{SRDY}$ low to either $\overline{SCS}$ or $\overline{SWR}$ high		15		ns
256	Pulse duration, SRAS high		30		ns
262	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before $\overline{SCS}$ or $\overline{SWR}$ no longer low		25		ns
263	Hold time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid after $\overline{SCS}$ or $\overline{SWR}$ high		25		ns
264	Setup time, SRSX, SRS0–SRS2, $\overline{SCS}$, and $\overline{SBHE}$ to SRAS no longer high (see Note 20)		30		ns
265	Hold time, SRSX, SRS0–SRS2, $\overline{SCS}$, and $\overline{SBHE}$ after SRAS low		15		ns
266a	Setup time, SRAS high to $\overline{SWR}$ no longer high (see Note 21)		25		ns
267†	Setup time, SRSX, SRS0–SRS2 before $\overline{SWR}$ no longer high (see Note 20)		15		ns
268	Hold time, SRSX, SRS0–SRS2 valid after $\overline{SWR}$ no longer low (see Note 21)		0		ns
272a	Setup time, $\overline{SRD}$, $\overline{SWR}$, and $\overline{SIACK}$ high from previous cycle to $\overline{SWR}$ no longer high		55		ns
273a	Hold time, $\overline{SRD}$, $\overline{SWR}$, and $\overline{SIACK}$ high after $\overline{SWR}$ high		55		ns
276‡	Delay time, $\overline{SRDY}$ low in the first DIO access to the SIF register to $\overline{SRDY}$ low in the immediately following access to the SIF (see *TMS380 Second-Generation Token-Ring User's Guide*, SPWU005, subsection 3.4.1.1.1)				ns
275	Delay time, $\overline{SWR}$ or $\overline{SCS}$ high to $\overline{SRDY}$ high (see Note 20)		0	35	ns
279§	Delay time, $\overline{SWR}$ high to $\overline{SRDY}$ in the high-impedance state		0	65	ns
280	Delay time, $\overline{SWR}$ low to SDDIR low (see Note 20)		0	25	ns
281	Delay time, $\overline{SWR}$ high to SDDIR high (see note 20)			55	ns
281a	Hold time, SDDIR low after $\overline{SWR}$ no longer active (see Note 20)		0		ns
282b	Delay time, SDBEN low to SRDY low (see *TMS380 Second Generation Token-Ring User's Guide,* SPWU005, subsection 3.4.1.1.1)	If SIF register is ready (no waiting required)	0	35	ns
		If SIF register is not ready (waiting required)	0	4000	
282W	Delay time, SDDIR low to $\overline{SDBEN}$ low		0	25	ns
283W	Delay time, $\overline{SCS}$ or $\overline{SWR}$ high to $\overline{SDBEN}$ no longer low		0	25	ns
286	Pulse duration, $\overline{SWR}$ high between DIO accesses (see Note 20)		55		ns

† It is the later of $\overline{SRD}$ and $\overline{SWR}$ or $\overline{SCS}$ low that indicates the start of the cycle.
‡ This specification has been characterized to meet stated value. It is not assured during manufacturing testing.
§ This specification is provided as an aid to board design. It is not assured during manufacturing testing.

NOTES: 20. The inactive chip select is $\overline{SIACK}$ in DIO read and DIO write cycles, and $\overline{SCS}$ is the inactive chip select in interrupt-acknowledge cycles.

21. In 80x8x mode, SRAS can be used to strobe the values of $\overline{SBHE}$, SRSX, SRS0–SRS2, and $\overline{SCS}$. When used to do so, SRAS must meet parameter 266a, and $\overline{SBHE}$, SRS0–SRS2, and $\overline{SCS}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.



† When the TMS380C25 begins to drive $\overline{\text{SDBEN}}$ inactive, it has already latched the write data internally. Parameter 263 must be met to the input of the data buffers.

NOTE A: In 8-bit 80x8x-mode DIO writes, the value placed on SADH0–SADH7 is a don't care.

Figure 26. 80x8x-DIO Write-Cycle Timing

80x8x-interrupt-acknowledge-cycle timing: first $\overline{\text{SIACK}}$ pulse

NO.		MIN	MAX	UNIT
286	Pulse duration, $\overline{\text{SIACK}}$ high between DIO accesses (see Note 20)	55		ns
287	Pulse duration, $\overline{\text{SIACK}}$ low on first pulse of two pulses	62.5		ns

NOTE 20: The inactive chip select is $\overline{\text{SIACK}}$ in DIO read and DIO write cycles, and $\overline{\text{SCS}}$ is the inactive chip select in interrupt-acknowledge cycles.

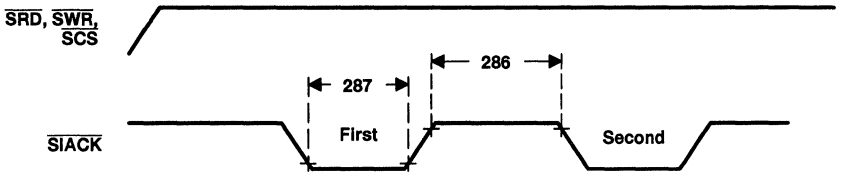
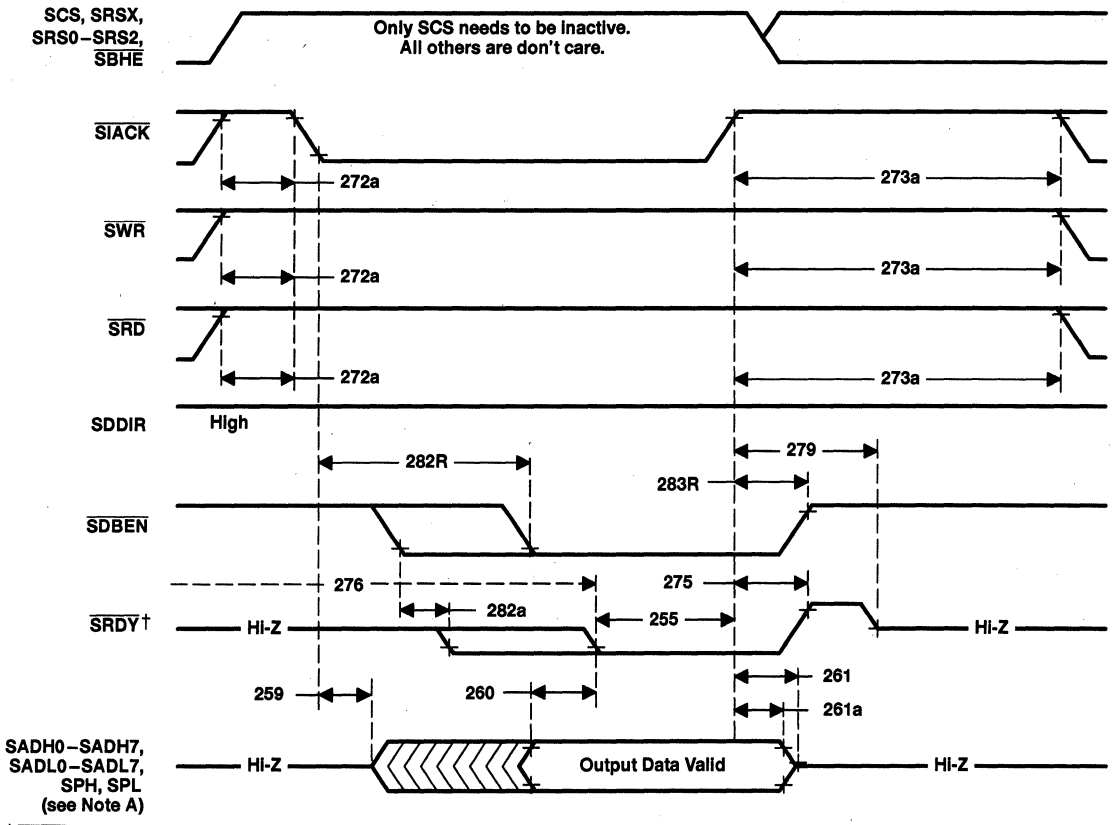


Figure 27. 80x8x-Interrupt-Acknowledge-Cycle Timing: First $\overline{\text{SIACK}}$ Pulse

80x8x-interrupt-acknowledge-cycle timing: second $\overline{\text{SIACK}}$ pulse

NO.		MIN	MAX	UNIT
255	Delay time, $\overline{\text{SRDY}}$ low to $\overline{\text{SCS}}$ high	15		ns
259†	Hold time, SAD in the high-impedance state after $\overline{\text{SIACK}}$ low (see Note 20)	0		ns
260	Setup time, output data valid before $\overline{\text{SRDY}}$ low	0		ns
261†	Delay time, $\overline{\text{SIACK}}$ high to SAD in the high-impedance state (see Note 20)		35	ns
261a	Hold time, output data valid after $\overline{\text{SIACK}}$ high (see Note Note 20)	0		ns
272a	Setup time, inactive data strobe high to $\overline{\text{SIACK}}$ no longer high	55		ns
273a	Hold time, inactive data strobe high after $\overline{\text{SIACK}}$ high	55		ns
275	Delay time, $\overline{\text{SIACK}}$ high to $\overline{\text{SRDY}}$ high (see Note Note 20)	0	35	ns
276‡	Delay time, $\overline{\text{SRDY}}$ low in the first DIO access to the SIF register to $\overline{\text{SRDY}}$ low in the immediately following access to the SIF		4000	ns
279†	Delay time, $\overline{\text{SIACK}}$ high to $\overline{\text{SRDY}}$ in the high-impedance state	0	65	ns
282a	Delay time, $\overline{\text{SDBEN}}$ low to $\overline{\text{SRDY}}$ low in a read cycle	0	35	ns
282R	Delay time, $\overline{\text{SIACK}}$ low to $\overline{\text{SDBEN}}$ low (see *TMS380 Second Generation Token-Ring User's Guide*, SPWU005, subsection 3.4.1.1.1), provided previous cycle completed	0	55	ns
283R	Delay time, $\overline{\text{SIACK}}$ high to $\overline{\text{SDBEN}}$ high (see Note Note 20)	0	35	ns

† This specification is provided as an aid to board design. It is not assured during manufacturing.
‡ This specification has been characterized to meet stated value. It is not assured during manufacturing.
NOTE 20: The inactive chip select is $\overline{\text{SIACK}}$ in DIO read and DIO write cycles, and $\overline{\text{SCS}}$ is the inactive chip select in interrupt-acknowledge cycles.



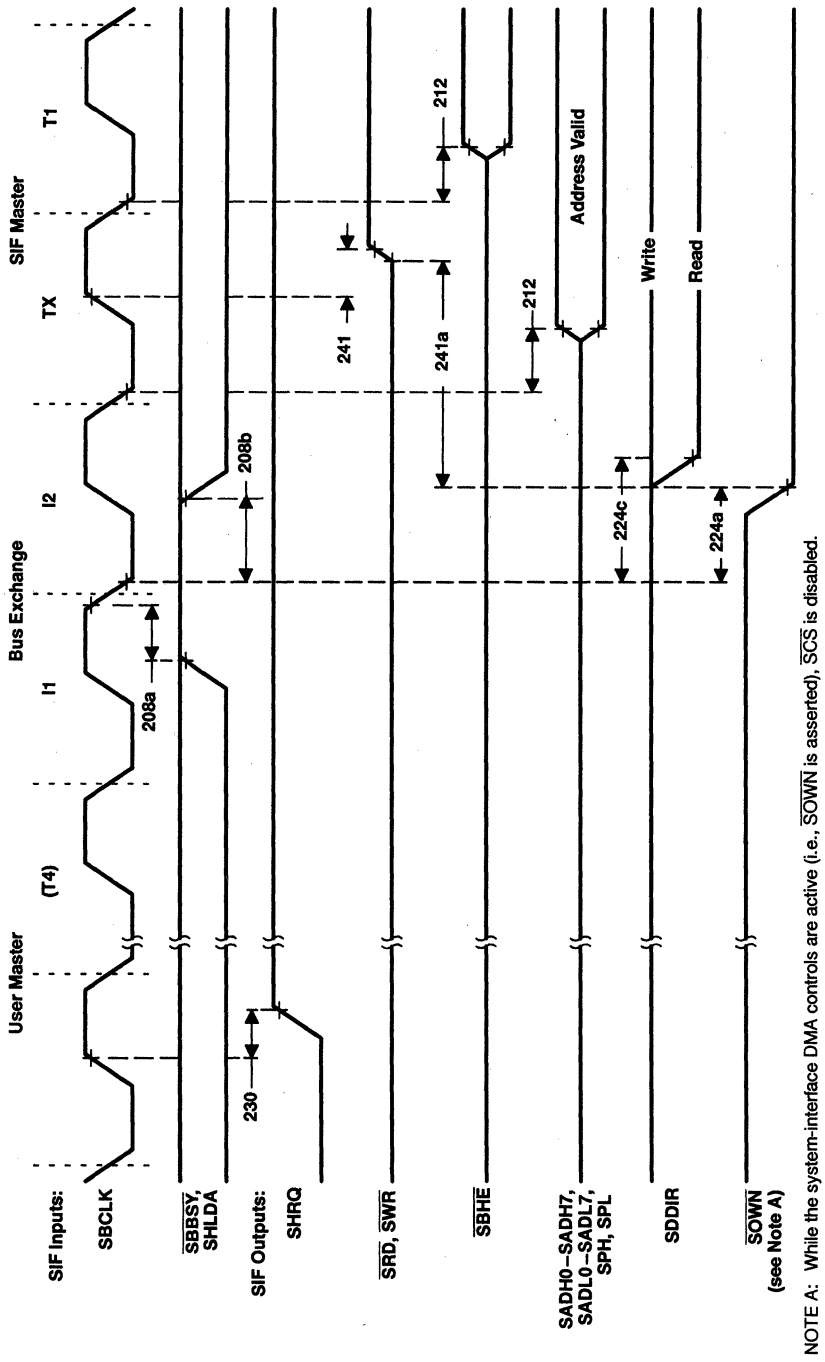
† $\overline{\text{SRDY}}$ is an active-low bus ready signal. It must be asserted before data output.
NOTE A: In 8-bit 80x8x mode DIO writes, the value placed on SADH0–SADH7 is a don't care.

Figure 28. 80x8x-Interrupt-Acknowledge-Cycle Timing: Second $\overline{\text{SIACK}}$ Pulse

80x8x-mode bus-arbitration timing, SIF takes control

NO.		MIN	MAX	UNIT
208a	Setup time, asynchronous signal $\overline{\text{SBBSY}}$ and SHLDA before SBCLK no longer high to assure recognition on that cycle	15		ns
208b	Hold time, asynchronous signal $\overline{\text{SBBSY}}$ and SHLDA after SBCLK low to assure recognition on that cycle	15		ns
212	Delay time, SBCLK low to SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid		25	ns
224a	Delay time, SBCLK low in cycle I2 to $\overline{\text{SOWN}}$ low	0	25	ns
224c	Delay time, SBCLK low in cycle I2 to SDDIR low in DMA read		30	ns
230	Delay time, SBCLK high to SHRQ high		25	ns
241	Delay time, SBCLK high in TX cycle to $\overline{\text{SRD}}$ and $\overline{\text{SWR}}$ high, bus acquisition		25	ns
241a†	Hold time, SRD and $\overline{\text{SWR}}$ in the high-impedance state after $\overline{\text{SOWN}}$ low, bus acquisition	$t_{c(SCK)}-15$		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.



NOTE A: While the system-interface DMA controls are active (i.e., $\overline{SOWN}$ is asserted), $\overline{SCS}$ is disabled.

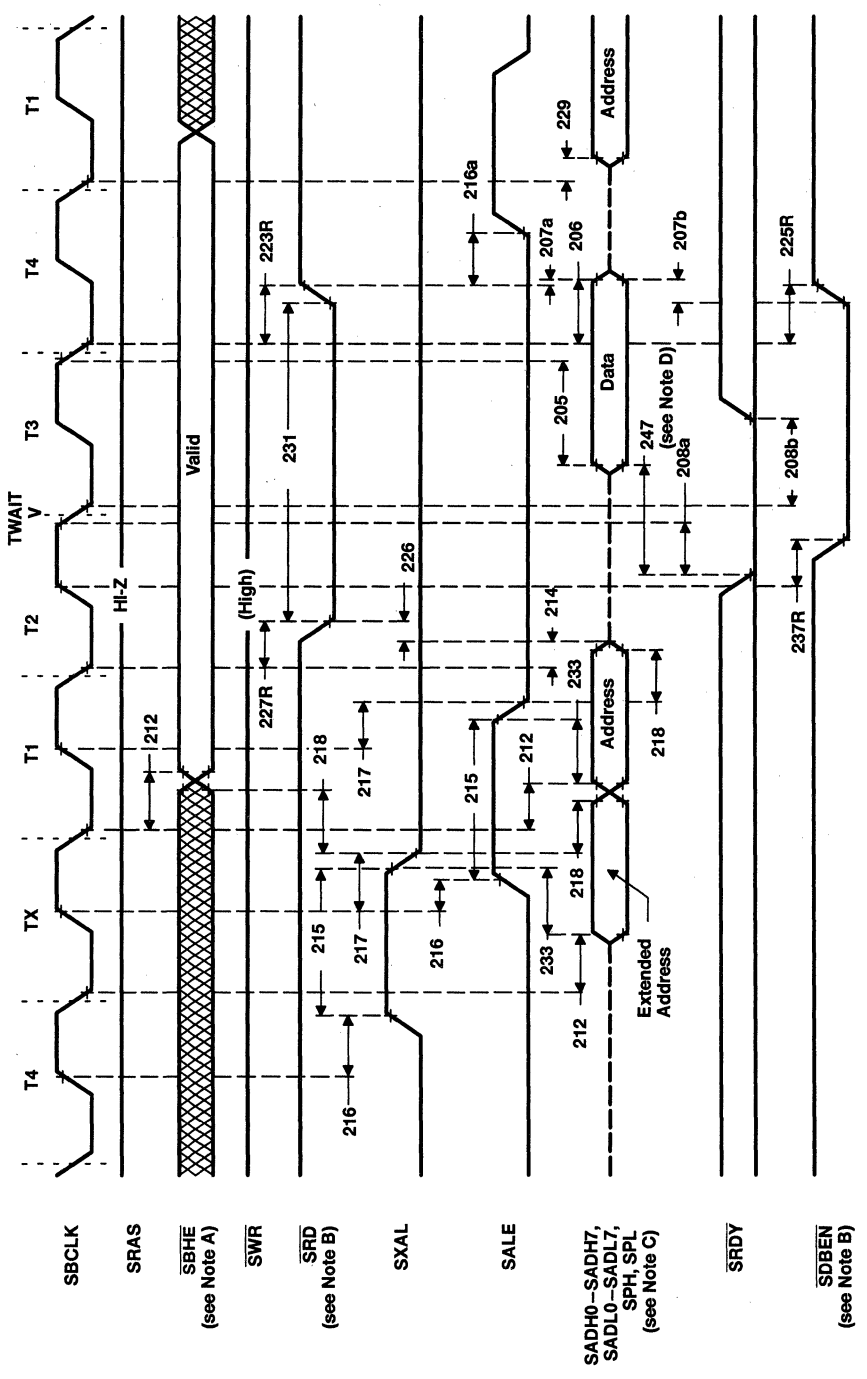
Figure 29. 80x8x-Mode Bus-Arbitration Timing, SIF Takes Control

80x8x-mode DMA read-cycle timing

NO.		MIN	MAX	UNIT
205	Setup time, SADL0–SADL7, SADH0–SADH7, SPH, and SPL valid before SBCLK in T3 cycle no longer high	15		ns
206	Hold time, SADL0–SADL7, SADH0–SADH7, SPH, and SPL valid after SBCLK low in T4 cycle if parameters 207a and 207b not met	15		ns
207a	Hold time, SADL0–SADL7, SADH0–SADH7, SPH, and SPL valid after $\overline{SRD}$ high	0		ns
207b	Hold time, SADL0–SADL7, SADH0–SADH7, SPH, and SPL valid after $\overline{SDBEN}$ no longer low	0		ns
208a	Setup time, asynchronous signal $\overline{SRDY}$ before SBCLK no longer high to assure recognition on this cycle	15		ns
208b	Hold time, asynchronous signal $\overline{SRDY}$ after SBCLK low to assure recognition on this cycle	15		ns
212	Delay time, SBCLK low to address valid		25	ns
214†	Delay time, SBCLK low in T1 cycle to SADH0–SADH7, SADL0–SADL7, SPH, and SPL in the high-impedance state		25	ns
215	Pulse duration, SALE and SXAL high	$t_{c(SCK)}-25$		ns
216	Delay time, SBCLK high to SALE or SXAL high		25	ns
216a	Hold time, SALE or SXAL low after $\overline{SRD}$ high	$t_{w(SCKL)}-15$		ns
217	Delay time, SBCLK high to SXAL low in the TX cycle or SALE low in the T1 cycle		25	ns
218	Hold time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid after SALE or SXAL low	$t_{w(SCKH)}-15$		ns
223R	Delay time, SBCLK low in T4 cycle to $\overline{SRD}$ high (see Note 22)		25	ns
225R	Delay time, SBCLK low in T4 cycle to $\overline{SDBEN}$ high		25	ns
226†	Delay time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL in the high-impedance state to $\overline{SRD}$ low	0		ns
227R	Delay time, SBCLK low in T2 cycle to $\overline{SRD}$ low		25	ns
229†	Hold time,SADH0–SADH7, SADL0–SADL7, SPH, and SPL in the high-impedance state after SBCLK low in T1 cycle	0		ns
231	Pulse duration, $\overline{SRD}$ low	$2t_{c(SCK)}-30$		ns
233	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before SALE, SXAL no longer high	$t_{w(SCKL)}-15$		ns
237R	Delay time, SBCLK high in the T2 cyle to $\overline{SDBEN}$ low		25	ns
247	Setup time, data valid before $\overline{SRDY}$ low if parameter 208a not met	0		ns

† This specification has been characterized to meet stated value.

NOTE 22: While the system-interface DMA controls are active (i.e., $\overline{SOWN}$ is asserted), $\overline{SCS}$ is disabled.



NOTES: A. In 8-bit 80x8x mode, $\overline{SBHE}$/SRNW is a don't care input during DIO and an inactive (high) output during DMA.
B. Motorola-style bus slaves hold SDTACK active until the bus master deasserts SAS.
C. In 8-bit 80x8x mode, the most significant byte of the address is maintained on SADH for T2, T3, and T4. The address is maintained according to parameter 21; i.e., held after T4 high.
D. If parameter 208A is not met, valid data must be present before $\overline{SRDY}$ goes low.

Figure 30. 80x8x-Mode DMA Read-Cycle Timing

80x8x-mode DMA write-cycle timing

NO.		MIN	MAX	UNIT
208a	Setup time, asynchronous signal $\overline{\text{SRDY}}$ before SBCLK no longer high to assure recognition on that cycle	15		ns
208b	Hold time, asynchronous signal $\overline{\text{SRDY}}$ after SBCLK low to assure recognition on that cycle	15		ns
212	Delay time, SBCLK low to SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid		25	ns
215	Pulse duration, SALE and SXAL high	$t_{c(SCK)}-25$		ns
216	Delay time, SBCLK high to SALE or SXAL high		25	ns
216a	Hold time, SALE or SXAL low after $\overline{\text{SWR}}$ high	$t_{w(SCKL)}-15$		ns
217	Delay time, SBCLK high to SXAL low in the TX cycle or SALE low in the T1 cycle		25	ns
218	Hold time, address valid after SALE, SXAL low	$t_{w(SCKH)}-15$		ns
219	Delay time, SBCLK low in T2 cycle to output data and parity valid		39	ns
221	Hold time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid after $\overline{\text{SWR}}$ high	$t_{c(SCK)}-15$		ns
223W	Delay time, SBCLK low to $\overline{\text{SWR}}$ high		25	ns
225W	Delay time, SBCLK high in T4 cycle to $\overline{\text{SDBEN}}$ high		25	ns
225WH	Hold time, $\overline{\text{SDBEN}}$ low after $\overline{\text{SWR}}$, $\overline{\text{SUDS}}$, and $\overline{\text{SLDS}}$ high	$t_{w(SCKL)}-25$		ns
227W	Delay time, SBCLK low in T2 cycle to $\overline{\text{SWR}}$ low		31	ns
232	Pulse duration, $\overline{\text{SWR}}$ low	$2t_{c(SCK)}-30$		ns
233	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before SALE, SXAL no longer high	$t_{w(SCKL)}-15$		ns
237W	Delay time, SBCLK high in T1 cycle to $\overline{\text{SDBEN}}$ low		25	ns

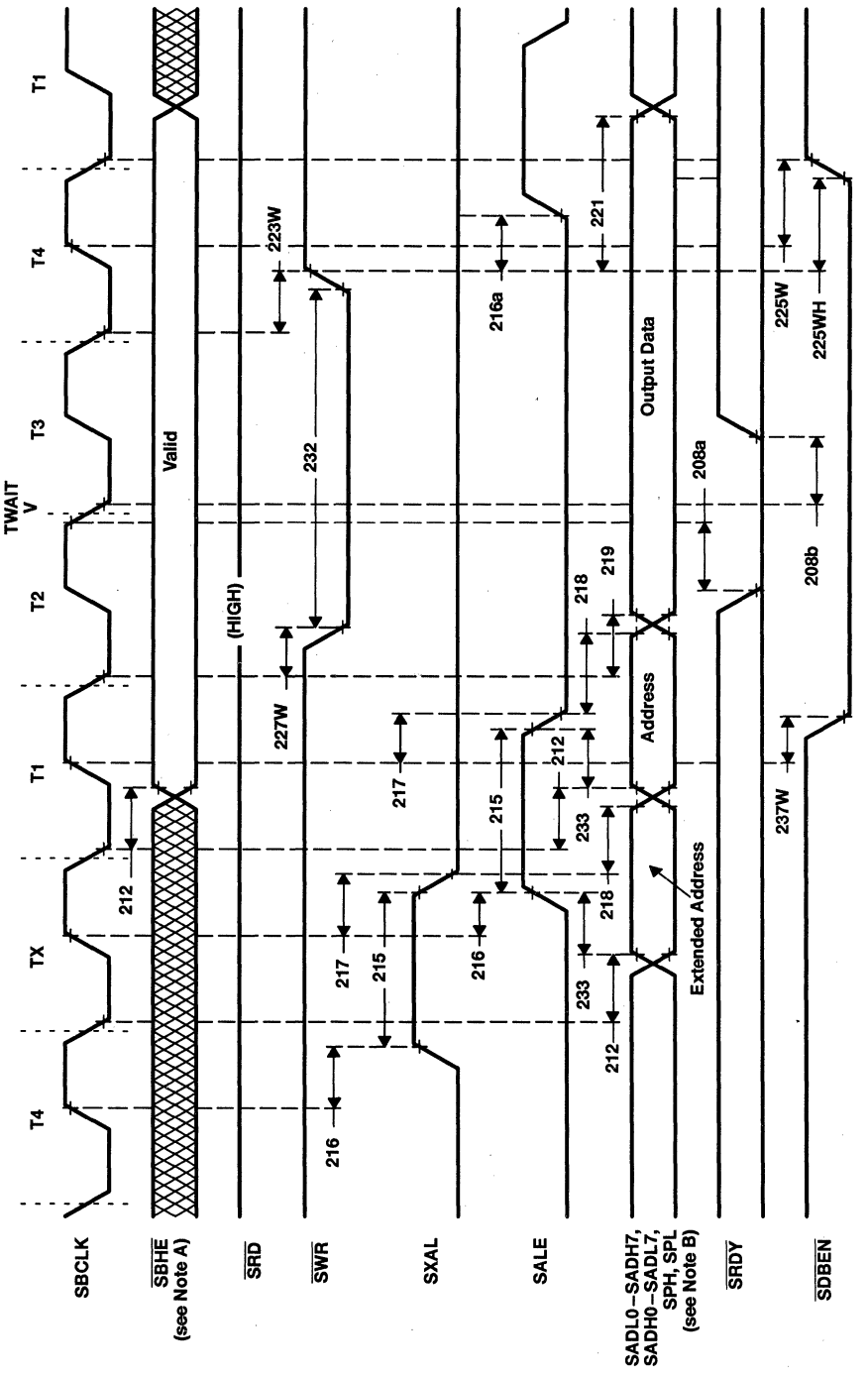


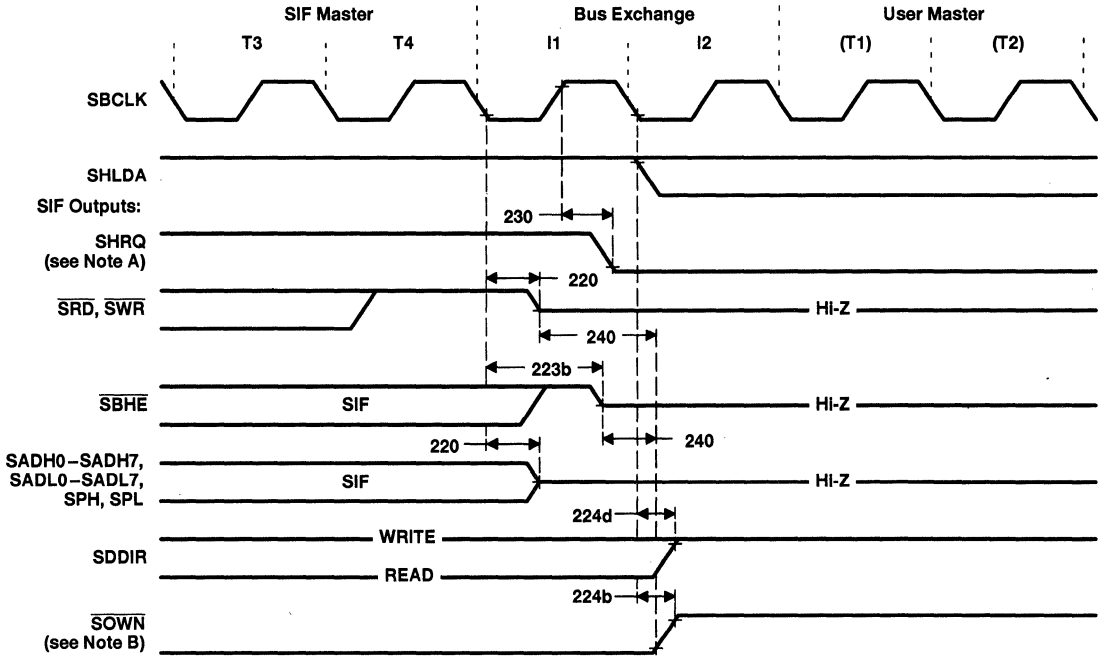
Figure 31. 80x8x-Mode DMA Write-Cycle Timing

NOTES: A. In 8-bit 80x8x mode, $\overline{SBHE}$/SRNW is a don't care input during DIO and an inactive (high) output during DMA.
B. In 8-bit 80x8x mode, the most significant byte of the address is maintained on SADH for T2, T3, and T4. The address is maintained according to parameter 21; i.e., held after T4 high.

80x8x-mode bus-arbitration timing, SIF returns control

NO.		MIN	MAX	UNIT
220†	Delay time, SBCLK low in I1 cycle to SADH0–SADH7, SADL0–SADL7, SPL, SPH, $\overline{SRD}$, and $\overline{SWR}$ in the high-impedance state		35	ns
223b†	Delay time, SBCLK low in I1 cycle to $\overline{SBHE}$ in the high-impedance state		45	ns
224b	Delay time, SBCLK low in cycle I2 to $\overline{SOWN}$ high		25	ns
224d	Delay time, SBCLK low in cycle I2 to SDDIR high		30	ns
230	Delay time, SBCLK high in cycle I1 to SHRQ low		25	ns
240†	Setup time, $\overline{SRD}$, $\overline{SWR}$, and $\overline{SBHE}$ in the high-impedance state before $\overline{SOWN}$ no longer low	0		ns

† This specification has been characterized to meet stated value.



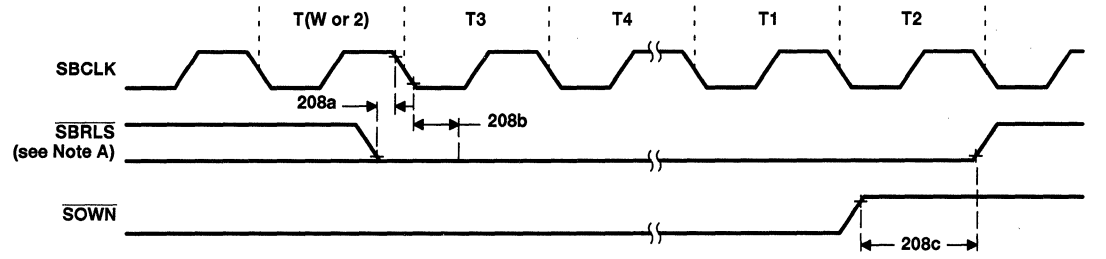
NOTES: A. In 80x8x mode, the system interface deasserts SHRQ on the rising edge of SBCLK following the T4 state of the last system-bus transfer it controls. In 68xxx mode, the system interface deasserts $\overline{SBRQ}$ on the rising edge of SBCLK in state T2 of the first system bus transfer it controls.

B. While the system-interface DMA controls are active (i.e., $\overline{SOWN}$ is asserted), $\overline{SCS}$ is disabled.

Figure 32. 80x8x-Mode Bus-Arbitration Timing, SIF Returns Control

80x8x-mode bus-release timing

NO.		MIN	MAX	UNIT
208a	Setup time, asynchronous input $\overline{\text{SBRLS}}$ low before SBCLK no longer high to assure recognition	15		ns
208b	Hold time, asynchronous input $\overline{\text{SBRLS}}$ low after SBCLK low to assure recognition	15		ns
208c	Hold time, $\overline{\text{SBRLS}}$ low after $\overline{\text{SOWN}}$ high	0		ns



NOTES: A. The system interface ignores the assertion of $\overline{\text{SBRLS}}$ if it does not own the system bus. If it does own the bus when it detects the assertion of $\overline{\text{SBRLS}}$, it completes any internally started DMA cycle and relinquish control of the bus. If no DMA transfer has internally started, the system interface releases the bus before starting another.

B. If $\overline{\text{SBERR}}$ is asserted when the system interface controls the system bus, the current bus transfer is completed regardless of the value of $\overline{\text{SDTACK}}$. If the BERETRY register is nonzero, the cycle is retried. If the BERETRY register is zero, the system interface releases control of the system bus. The system interface ignores the assertion of $\overline{\text{SBERR}}$ if it is not performing a DMA bus cycle on the system bus. When $\overline{\text{SBERR}}$ is properly asserted and BERETRY is zero, however, the system interface releases the bus upon completion of the current bus transfer and halts all further DMA on the system side. The error is synchronized to the local bus and DMA stops on the local sides. The value of the SDMAADR, SDMADDRX, and SDMALEN registers in the system interface are not defined after a system-bus error.

C. In cycle-steal mode, state TX is present on every system-bus transfer. In burst mode, state TX is present on the first bus transfer and whenever the increment of the DMA address register carries beyond the least significant 16 bits.

D. $\overline{\text{SDTACK}}$ is not sampled to verify that it is deasserted.

E. Unless otherwise specified, for all signals specified as a maximum delay from the end of an SBCLK transition to the signal valid, the signal is also specified to hold its previous value (including high impedance) until the start of that SBCLK transition.

Figure 33. 80x8x-Mode Bus-Release Timing

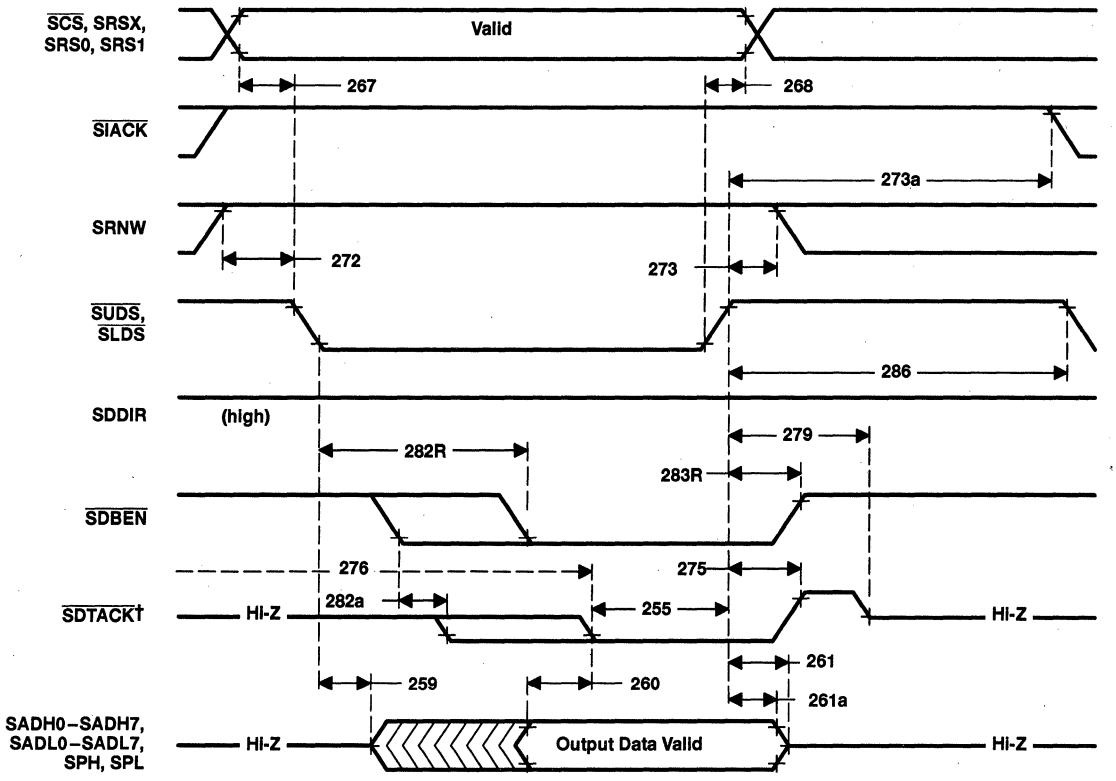
68xxx-DIO read-cycle timing

NO.		MIN	MAX	UNIT
255	Delay time, $\overline{SDTACK}$ low to either $\overline{SCS}$, $\overline{SUDS}$, or $\overline{SLDS}$ high	15		ns
259†	Hold time, SAD in the high-impedance state after $\overline{SUDS}$ or $\overline{SLDS}$ low (see Note 20)	0		ns
260	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before $\overline{SDTACK}$ low	0		ns
261†	Delay time, $\overline{SCS}$, $\overline{SUDS}$, or $\overline{SLDS}$ high to SADH0–SADH7, SADL0–SADL7, SPH, and SPL in the high-impedance state (see Note 20)		35	ns
261a	Hold time, output data valid after $\overline{SUDS}$ or $\overline{SLDS}$ no longer low (see Note 20)	0		ns
267	Setup time, register address before $\overline{SUDS}$ or $\overline{SLDS}$ no longer high (see Note 20)	15		ns
268	Hold time, register address valid after $\overline{SUDS}$ or $\overline{SLDS}$ no longer low (see Note 21)	0		ns
272	Setup time, SRNW before $\overline{SUDS}$ or $\overline{SLDS}$ no longer high (see Note 20)	15		ns
273	Hold time, SRNW after $\overline{SUDS}$ or $\overline{SLDS}$ high	0		ns
273a	Hold time, $\overline{SIACK}$ high after $\overline{SUDS}$ or $\overline{SLDS}$ high	55		ns
275	Delay time, $\overline{SCS}$, $\overline{SUDS}$, or $\overline{SLDS}$ high to $\overline{SDTACK}$ high (see Note 20)		35	ns
276‡	Delay time, $\overline{SDTACK}$ low in the first DIO access to the SIF register to $\overline{SDTACK}$ low in the immediately following access to the SIF		4000	ns
279†	Delay time, $\overline{SUDS}$ or $\overline{SLDS}$ high to $\overline{SDTACK}$ in the high-impedance state		65	ns
282a	Delay time, $\overline{SDBEN}$ low to $\overline{SDTACK}$ low		35	ns
282R	Delay time, $\overline{SUDS}$ or $\overline{SLDS}$ low to $\overline{SDBEN}$ low (see *TMS380 Second Generation Token-Ring User's Guide,* SPWU005, subsection 3.4.1.1.1) provided the previous cycle completed		55	ns
283R	Delay time, $\overline{SUDS}$ or $\overline{SLDS}$ high to $\overline{SDBEN}$ high (see Note 20)		35	ns
286	Pulse duration, $\overline{SUDS}$ or $\overline{SLDS}$ high between DIO accesses (see Note 20)	55		ns

† This specification is provided as an aid to board design.
‡ This specification has been characterized to meet stated value.

NOTES: 20. The inactive chip select is $\overline{SIACK}$ in DIO read and DIO write cycles, and $\overline{SCS}$ is the inactive chip select in interrupt-acknowledge cycles.

21. In 80x8x mode, SRAS can be used to strobe the values of $\overline{SBHE}$, SRSX, SRS0–SRS2, and $\overline{SCS}$. When used to do so, SRAS must meet parameter 266a, and $\overline{SBHE}$, SRS0–SRS2, and $\overline{SCS}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.



† $\overline{\text{SDTACK}}$ is an active-low bus ready signal. It must be asserted before data output.

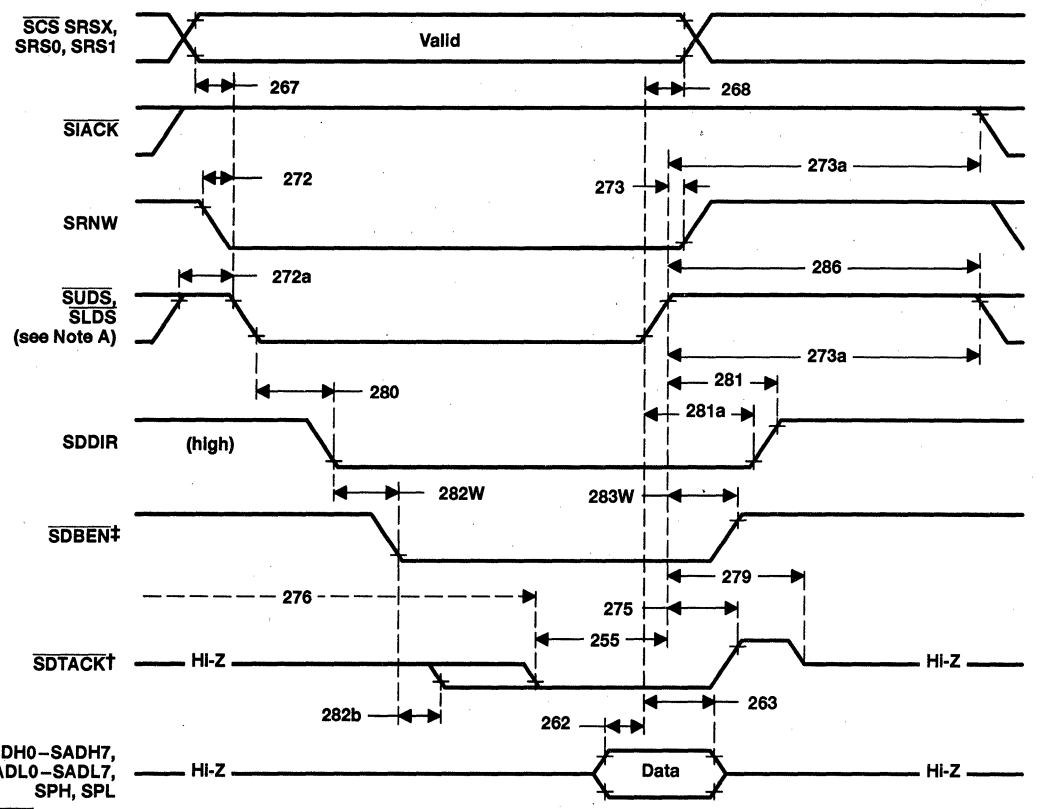
Figure 34. 68xxx-DIO Read-Cycle Timing

68xxx-DIO write-cycle timing

NO.			MIN	MAX	UNIT
255	Delay time, $\overline{SDTACK}$ low to either $\overline{SCS}$, SUDS or $\overline{SLDS}$ high		15		ns
262	Setup time, write data valid before $\overline{SUDS}$ or $\overline{SLDS}$ no longer low		25		ns
263	Hold time, write data valid after $\overline{SUDS}$ or $\overline{SLDS}$ high		25		ns
267†	Setup time, register address before $\overline{SUDS}$ or $\overline{SLDS}$ no longer high (see Note 20)		15		ns
268	Hold time, register address valid after $\overline{SUDS}$ or $\overline{SLDS}$ no longer low (see Note 21)		0		ns
272	Setup time, SRNW before $\overline{SUDS}$ or $\overline{SLDS}$ no longer high (see Note 20)		15		ns
272a	Setup time, inactive $\overline{SUDS}$ or $\overline{SLDS}$ high to active data strobe no longer high		55		ns
273	Hold time, SRNW after $\overline{SUDS}$ or $\overline{SLDS}$ high		0		ns
273a	Hold time, inactive $\overline{SUDS}$ or $\overline{SLDS}$ high after active data strobe high		55		ns
275	Delay time, $\overline{SCS}$, $\overline{SUDS}$ or $\overline{SLDS}$ high to $\overline{SDTACK}$ high (see Note 20)			35	ns
276‡	Delay time, $\overline{SDTACK}$ low in the first DIO access to the SIF register to $\overline{SDTACK}$ low in the immediately following access to the SIF			4000	ns
279§	Delay time, $\overline{SUDS}$ or $\overline{SLDS}$ high to $\overline{SDTACK}$ in the high-impedance state			65	ns
280	Delay time, $\overline{SUDS}$ or $\overline{SLDS}$ low to SDDIR low (see Note 20)			25	ns
281	Delay time, $\overline{SUDS}$ or $\overline{SLDS}$ high to SDDIR high (see Note 20)			55	ns
281a	Hold time, SDDIR low after $\overline{SUDS}$ or $\overline{SLDS}$ no longer active (see Note 20)		0		ns
282b	Delay time, SDBEN low to SDTACK low (see *TMS380 Second Generation Token-Ring User's Guide,* SPWU005, subsection 3.4.1.1.1)	If SIF register is ready (no waiting required)	0	35	ns
		If SIF register is not ready (waiting required)	0	4000	
282W	Delay time, SDDIR low to $\overline{SDBEN}$ low			25	ns
283W	Delay time, $\overline{SUDS}$ or $\overline{SLDS}$ high to $\overline{SDBEN}$ no longer low			25	ns
286	Pulse duration, $\overline{SUDS}$ or $\overline{SLDS}$ high between DIO accesses (see Note 20)		55		ns

† This specification has been characterized to meet stated value.
‡ It is the later of $\overline{SRD}$ and $\overline{SWR}$ or $\overline{SCS}$ low that indicates the start of the cycle.
§ This specification is provided as an aid to board design.

NOTES: 20. The inactive chip select is $\overline{SIACK}$ in DIO read and DIO write cycles, and $\overline{SCS}$ is the inactive chip select in interrupt-acknowledge cycles.
21. In 80x8x mode, SRAS can be used to strobe the values of $\overline{SBHE}$, SRSX, SRS0–SRS2, and $\overline{SCS}$. When used to do so, SRAS must meet parameter 266a, and $\overline{SBHE}$, SRS0–SRS2, and $\overline{SCS}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.



† $\overline{\text{SDTACK}}$ is an active-low bus ready signal. It must be asserted before data output.

‡ When the TMS380C16 begins to drive $\overline{\text{SDBEN}}$ inactive, it has already latched the write date internally. Parameter 263 must be met to the input of the data buffers.

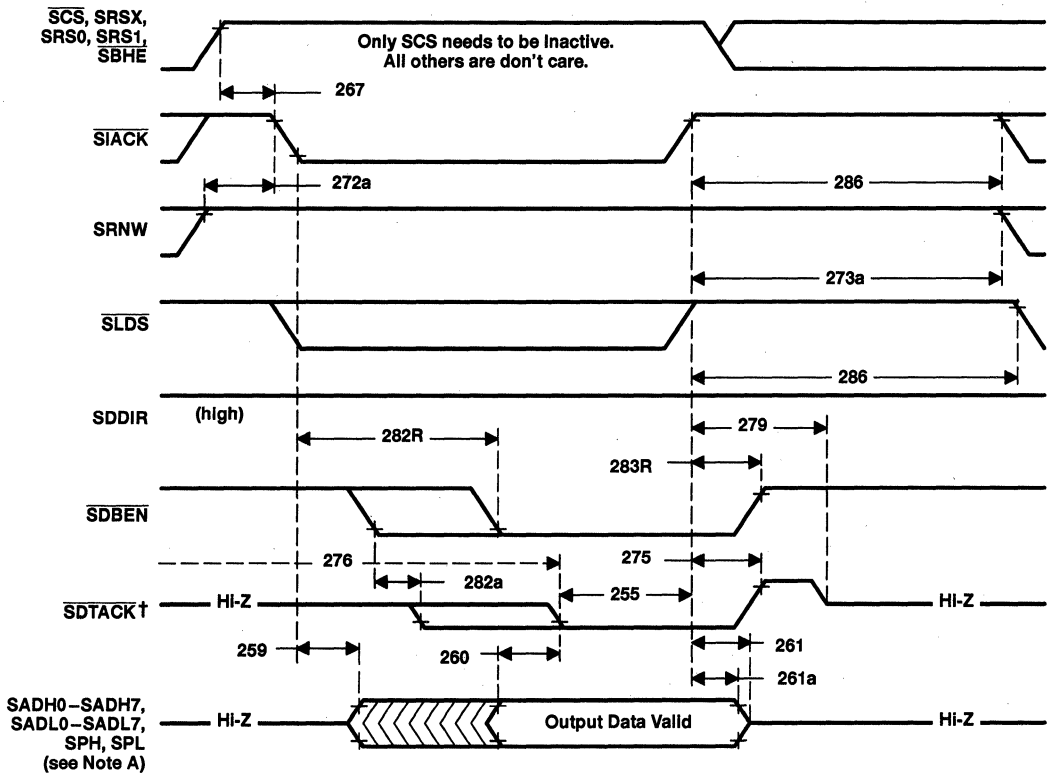
NOTE A: For 68xxx mode, skew between $\overline{\text{SLDS}}$ and $\overline{\text{SUDS}}$ must not exceed 10 ns. Provided this limitation is observed, all events referenced to a data strobe edge use the later occurring edge. Events defined by two data strobes edges, such as parameter 286, are measured between latest and earlier edges.

Figure 35. 68xxx-DIO Write-Cycle Timing

68xxx-interrupt-acknowledge-cycle timing

NO.		MIN	MAX	UNIT
255	Delay time, $\overline{SDTACK}$ low to either $\overline{SCS}$ or $\overline{SUDS}$, or $\overline{SIACK}$ high	15		ns
259†	Hold time, SAD in the high-impedance state after $\overline{SIACK}$ no longer high (see Note 20)	0		ns
260	Setup time, output data valid before $\overline{SDTACK}$ no longer high	0		ns
261†	Delay time, $\overline{SIACK}$ high to SAD in the high-impedance state (see Note 20)		35	ns
261a	Hold time, output data valid after $\overline{SCS}$ or $\overline{SIACK}$ no longer low (see Note 20)	0		ns
267‡	Setup time, register address before $\overline{SIACK}$ no longer high (see Note 20)	15		ns
272a	Setup time, inactive high $\overline{SIACK}$ to active data strobe no longer high	55		ns
273a	Hold time, inactive SRNW high after active data strobe high	55		ns
275	Delay time, $\overline{SCS}$ or $\overline{SRNW}$ high to $\overline{SDTACK}$ high (see Note 20)		35	ns
276§	Delay time, $\overline{SDTACK}$ low in the first DIO access to the SIF register to $\overline{SDTACK}$ low in the immediately following access to the SIF		4000	ns
279†	Delay time, $\overline{SIACK}$ high to $\overline{SDTACK}$ in the high-impedance state		65	ns
282a	Delay time, $\overline{SDBEN}$ low to $\overline{SDTACK}$ low in a read cycle		35	ns
282R	Delay time, $\overline{SIACK}$ low to $\overline{SDBEN}$ low (see *TMS380 Second Generation Token-Ring User's Guide*, SPWU005, subsection 3.4.1.1.1) provided the previous cycle completed		55	ns
283R	Delay time, $\overline{SIACK}$ high to $\overline{SDBEN}$ high (see Note 20)		35	ns
286	Pulse duration, $\overline{SIACK}$ high between DIO accesses (see Note 20)	55		ns

† This specification is provided as an aid to board design.
‡ It is the later of $\overline{SRD}$ and $\overline{SRD}$ or $\overline{SCS}$ low that indicates the start of the cycle.
§ This specification has been characterized to meet stated value.
NOTE 20: The inactive chip select is $\overline{SIACK}$ in DIO read and DIO write cycles, and $\overline{SCS}$ is the inactive chip select in interrupt-acknowledge cycles.



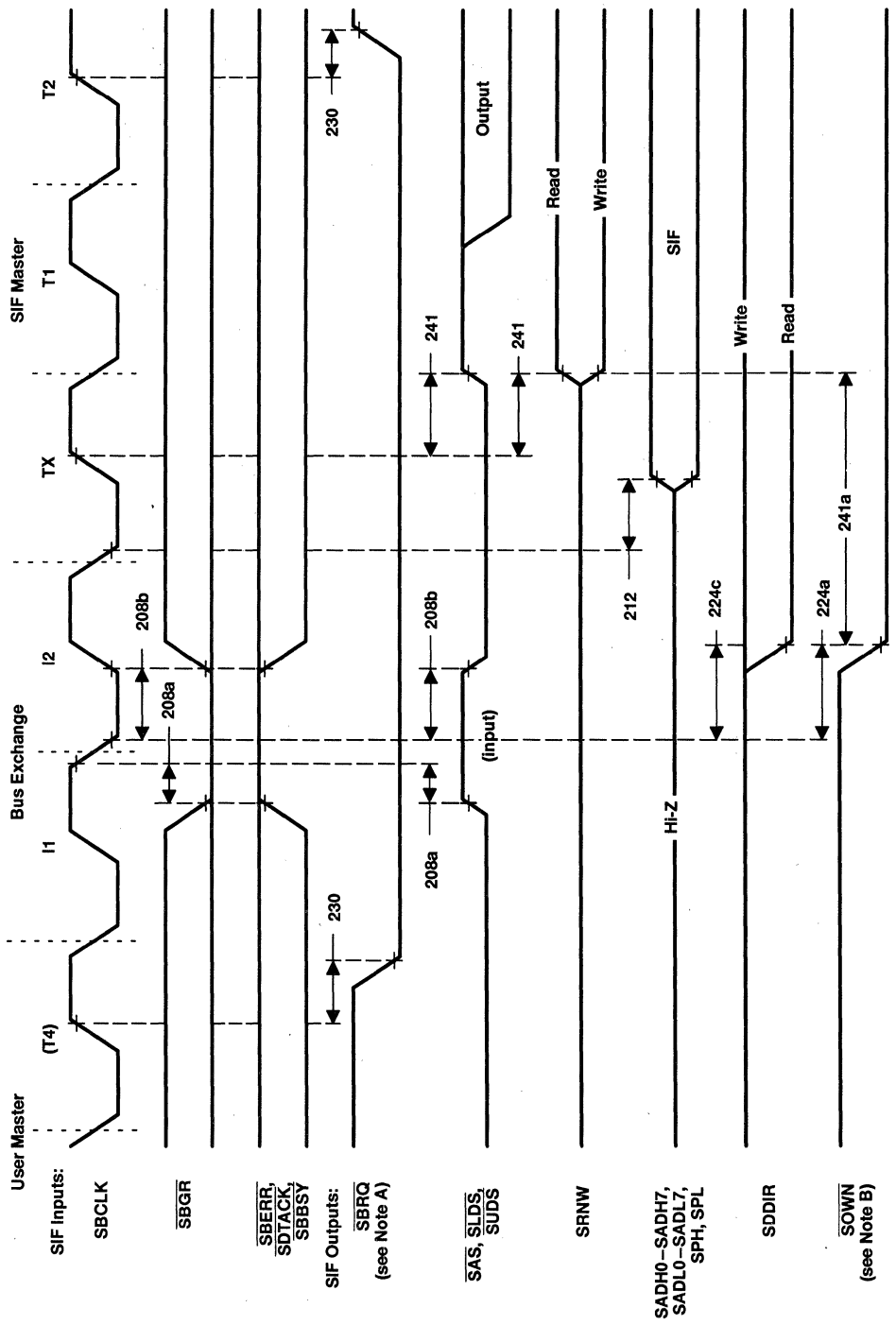
† $\overline{\text{SDTACK}}$ is an active-low bus ready signal. It must be asserted before data output.
NOTE A: Internal logic drives $\overline{\text{SDTACK}}$ high and verifies that it has reached a valid-high level before the signal enters the high-impedance state.

Figure 36. 68xxx-Interrupt-Acknowledge-Cycle Timing

68xxx-mode bus-arbitration timing, SIF takes control

NO.		MIN	MAX	UNIT
208a	Setup time, asynchronous input $\overline{\text{SBGR}}$ before SBCLK no longer high to assure recognition on this cycle	15		ns
208b	Hold time, asynchronous input $\overline{\text{SBGR}}$ after SBCLK low to assure recognition on this cycle	15		ns
212	Delay time, SBCLK low to address valid		25	ns
224a	Delay time, SBCLK low in cycle I2 to $\overline{\text{SOWN}}$ low (see Note 23)		25	ns
224c	Delay time, SBCLK low in cycle I2 to SDDIR low in DMA read		30	ns
230	Delay time, SBCLK high to either SHRQ low or $\overline{\text{SBRQ}}$ high		25	ns
241	Delay time, SBCLK high in TX cycle to $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$ high		25	ns
241a†	Hold time, $\overline{\text{SUDS}}$, $\overline{\text{SLDS}}$, SRNW, and $\overline{\text{SAS}}$ in the high-impedance state after $\overline{\text{SOWN}}$ low, bus acquisition	$t_{c(SCK)}-15$		ns

† This specification has been characterized to meet stated value.
NOTE 23: Motorola-style bus slaves hold $\overline{\text{SDTACK}}$ active until the bus master deasserts $\overline{\text{SAS}}$.



NOTES: A. In 80x8x mode, the system interface deasserts SHRQ on the rising edge of SBCLK following the T4 state of the last system bus transfer it controls. In 68xxx mode, the system interface deasserts SBRQ on the rising edge of SBCLK in state T2 of the first system bus transfer it controls.
B. While the system-interface DMA controls are active (i.e., SOWN is asserted), SCS is disabled.

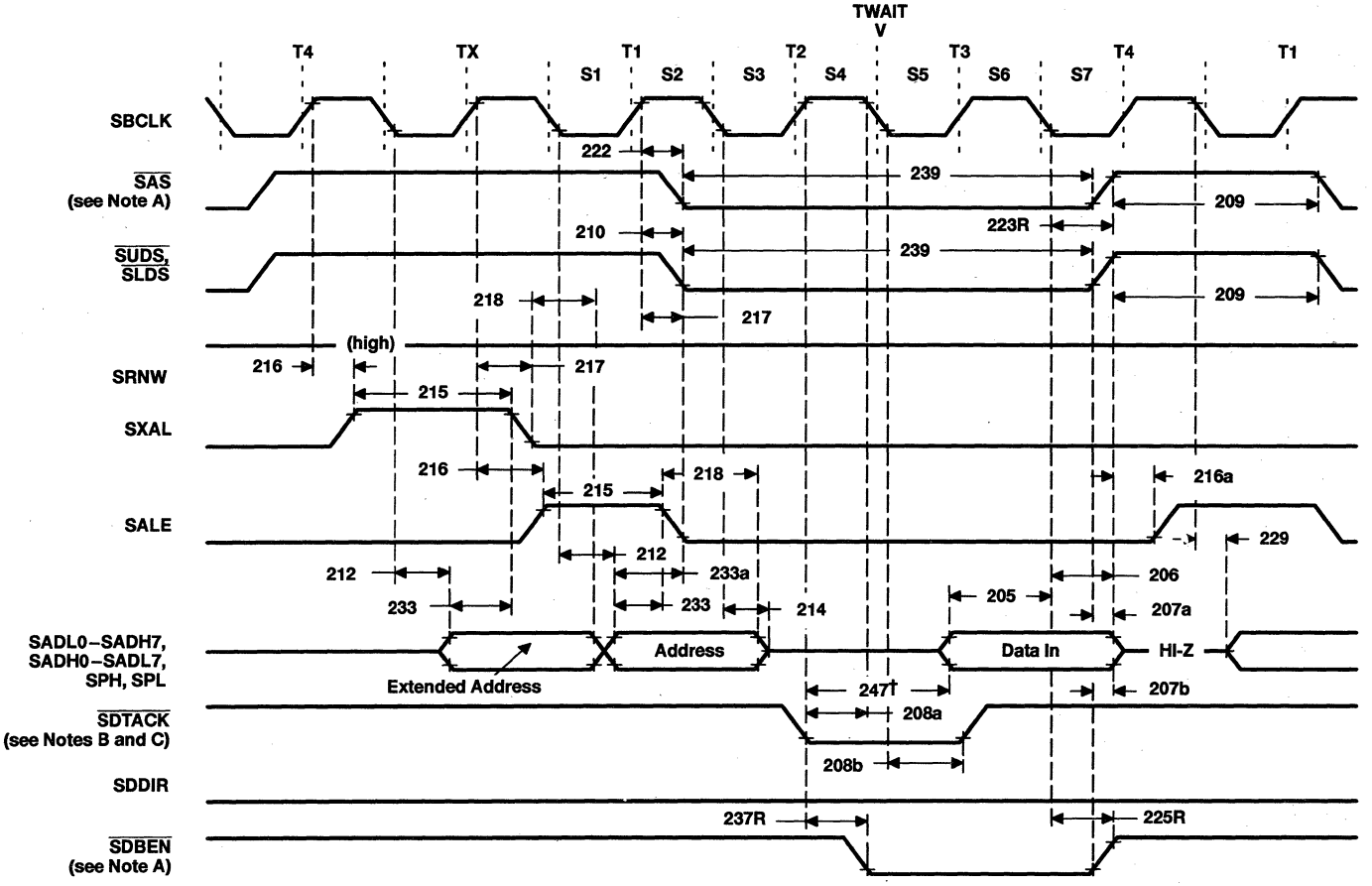
Figure 37. 68xxx-Mode Bus-Arbitration Timing, SIF Takes Control

68xxx-mode DMA-read-cycle timing

NO.		MIN	MAX	UNIT
205	Setup time, input data valid before SBCLK in T3 cycle no longer high	15		ns
206	Hold time, input data valid after SBCLK low in T4 cycle if parameters 207a and 207b not met	15		ns
207a	Hold time, input data valid after data strobe no longer low	0		ns
207b	Hold time, input data valid after $\overline{\text{SDBEN}}$ no longer low	0		ns
208a	Setup time, asynchronous input $\overline{\text{SDTACK}}$ before SBCLK no longer high to assure recognition on this cycle	15		ns
208b	Hold time, asynchronous input $\overline{\text{SDTACK}}$ after SBCLK low to assure recognition on this cycle	15		ns
209	Pulse duration, $\overline{\text{SAS}}$, $\overline{\text{SUDS}}$, and $\overline{\text{SLDS}}$ high	$t_{c(SCK)}+t_{w(SCKL)}-25$		ns
210	Delay time, SBCLK high in T2 cycle to $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$ active		25	ns
212	Delay time, SBCLK low to address valid		25	ns
214†	Delay time, SBCLK low in T2 cycle to SAD in the high-impedance state		25	ns
215	Pulse duration, SALE and SXAL high	$t_{c(SCK)}-25$		ns
216	Delay time, SBCLK high to SALE or SXAL high		25	ns
216a	Hold time, SALE or SXAL low after $\overline{\text{SUDS}}$ and $\overline{\text{SAS}}$ high	$t_{w(SCKL)}-15$		ns
217	Delay time, SBCLK high to SXAL low in the TX cycle or SALE low in the T1 cycle		25	ns
218	Hold time, address valid after SALE, SXAL low	$t_{w(SCKH)}-15$		ns
222	Delay time, SBCLK high to $\overline{\text{SAS}}$ low		25	ns
223R	Delay time, SBCLK low in T4 cycle to $\overline{\text{SUDS}}$, $\overline{\text{SLDS}}$, and $\overline{\text{SAS}}$ high (see Note 22)		25	ns
225R	Delay time, SBCLK low in T4 cycle to $\overline{\text{SDBEN}}$ high		25	ns
229†	Hold time, SAD in the high-impedance state after SBCLK low in T4 cycle	0		ns
233	Setup time, address valid before SALE or SXAL no longer high	$t_{w(SCKL)}-15$		ns
233a	Setup time, address valid before $\overline{\text{SAS}}$ no longer high	$t_{w(SCKL)}-15$		ns
237R	Delay time, SBCLK high in the T2 cycle to $\overline{\text{SDBEN}}$ low		25	ns
239	Pulse duration, $\overline{\text{SAS}}$, $\overline{\text{SUDS}}$, and $\overline{\text{SLDS}}$	$2t_{c(SCK)}+t_{w(SCKH)}-30$		ns
247	Setup time, data valid before $\overline{\text{SDTACK}}$ low if parameter 208a not met	0		ns

† This specification has been characterized to meet stated value.

NOTE 22: While the system-interface DMA controls are active (i.e., $\overline{\text{SOWN}}$ is asserted), $\overline{\text{SCS}}$ is disabled.



† If parameter 208a is not met, valid data must be present before SDTACK goes low.

NOTES: A. Motorola-style bus slaves hold SDTACK active until the bus master deasserts SAS.
B. All V_{SS} pins should be routed to minimize inductance to system ground.
C. On read cycle, read strobe remains active until the internal sample of incoming data is completed. Input data can be removed when either the read strobe or SDBEN becomes no longer active.

Figure 38. 68xxx-Mode DMA-Read-Cycle Timing

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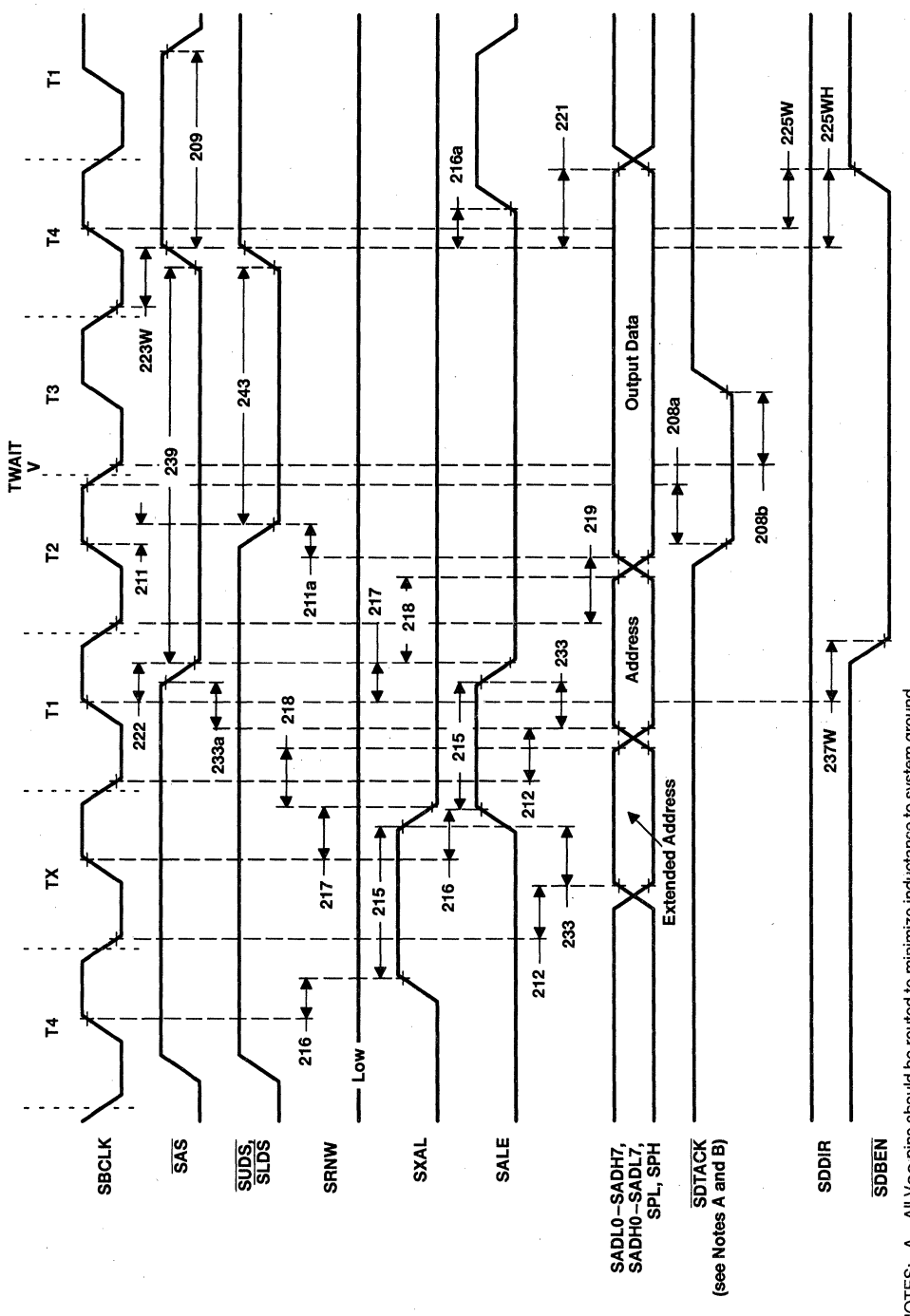
68xxx-mode DMA-write-cycle timing

NO.		MIN	MAX	UNIT
208a	Setup time, asynchronous input $\overline{\text{SDTACK}}$ before SBCLK no longer high to assure recognition on this cycle	15		ns
208b	Hold time, asynchronous input $\overline{\text{SDTACK}}$ after SBCLK low to assure recognition on this cycle	15		ns
209	Pulse duration, $\overline{\text{SAS}}$, $\overline{\text{SUDS}}$, and $\overline{\text{SLDS}}$ high	$t_{c(SCK)}+t_{w(SCKL)}-25$		ns
211	Delay time, SBCLK high in T2 cycle to $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$ active		25	ns
211a	Delay time, output data valid to $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$ no longer high	$t_{w(SCKL)}-15$		ns
212	Delay time, SBCLK low to address valid		25	ns
215	Pulse duration, SALE and SXAL high	$t_{c(SCK)}-25$		ns
216	Delay time, SBCLK high to SALE or SXAL high		25	ns
216a	Hold time, SALE or SXAL low after $\overline{\text{SUDS}}$ and $\overline{\text{SAS}}$ high	$t_{w(SCKL)}-15$		ns
217	Delay time, SBCLK high to SXAL low in the TX cycle or SALE low in the T1 cycle		25	ns
218	Hold time, address valid after SALE, SXAL low	$t_{w(SCKH)}-15$		ns
219	Delay time, SBCLK low in T2 cycle to output data and parity valid		39	ns
221	Hold time, output data, parity valid after $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$ high	$t_{c(SCK)}-15$		ns
222	Delay time, SBCLK high to $\overline{\text{SAS}}$ low		25	ns
223W	Delay time, SBCLK low to $\overline{\text{SUDS}}$, $\overline{\text{SLDS}}$, and $\overline{\text{SAS}}$ high		25	ns
225W	Delay time, SBCLK high in T4 cycle to $\overline{\text{SDBEN}}$ high		25	ns
225WH	Hold time, $\overline{\text{SDBEN}}$ low after $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$ high	$t_{w(SCKL)}-25$		ns
233	Setup time, address valid before SALE or SXAL no longer high	$t_{w(SCKL)}-15$		ns
233a	Setup time, address valid before $\overline{\text{SAS}}$ no longer high	$t_{w(SCKL)}-15$		ns
237W	Delay time, SBCLK high in T1 cycle to $\overline{\text{SDBEN}}$ low		25	ns
239	Pulse duration, $\overline{\text{SAS}}$	$2t_{c(SCK)}+t_{w(SCKH)}-30$		ns
243	Pulse duration, $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$	$t_{c(SCK)}+t_{w(SCKH)}-25$		ns



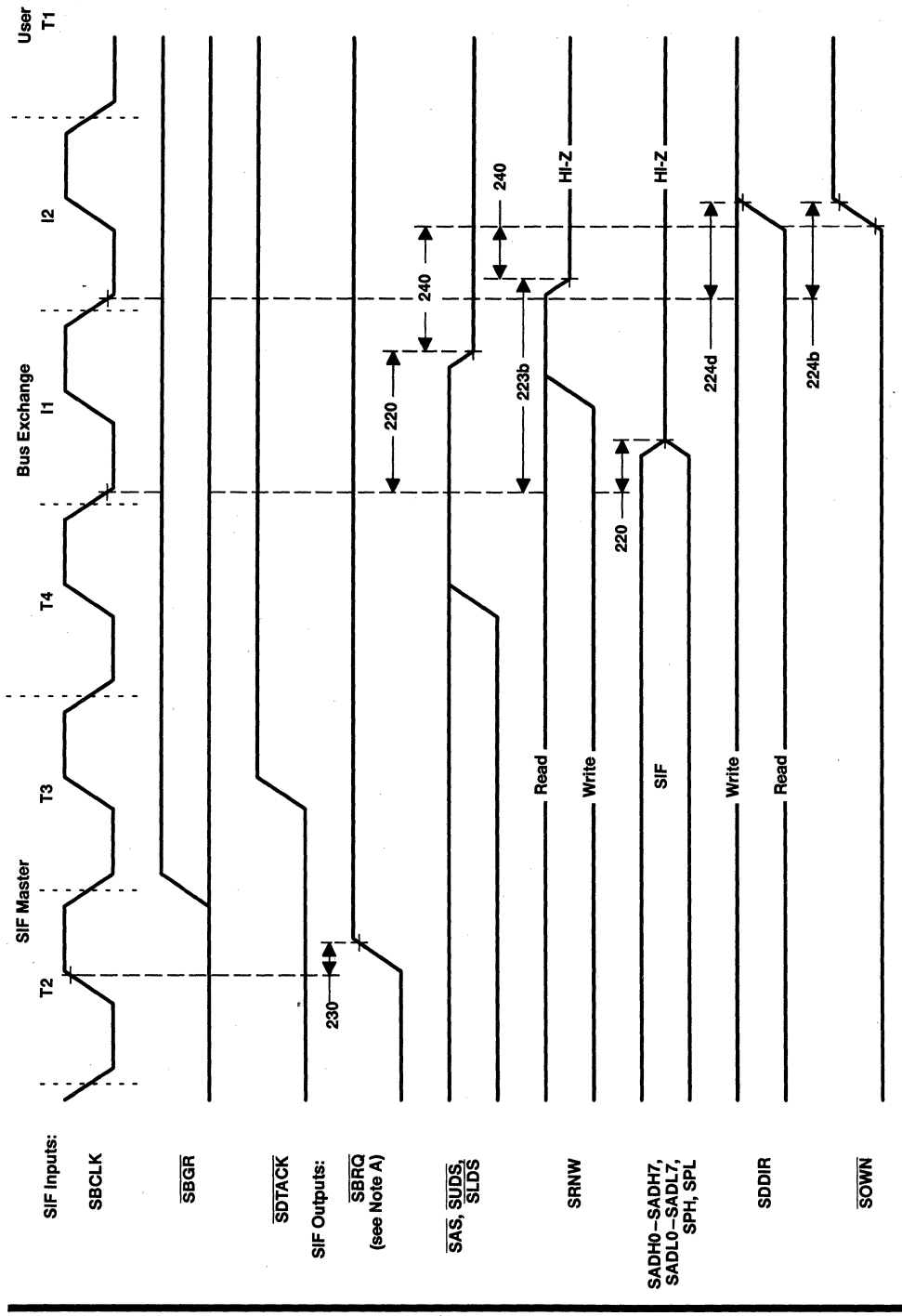
NOTES: A. All V_{SS} pins should be routed to minimize inductance to system ground.
B. On read cycle, read strobe remains active until the internal sample of incoming data is completed. Input data can be removed when either the read strobe or $\overline{SDBEN}$ becomes no longer active.

Figure 39. 68xxx-Mode DMA-Write-Cycle Timing

68xxx-mode bus-arbitration timing, SIF returns control

NO.		MIN	MAX	UNIT
220†	Delay time, SBCLK low in I1 cycle to SAD, SPL, SPH, $\overline{\text{SUDS}}$, and $\overline{\text{SLDS}}$ in the high-impedance state, bus release		35	ns
223b†	Delay time, SBCLK low in I1 cycle to $\overline{\text{SBHE}}$/SRNW in the high-impedance state		45	ns
224b	Delay time, SBCLK low in cycle I2 to $\overline{\text{SOWN}}$ high		25	ns
224d	Delay time, SBCLK low in cycle I2 to SDDIR high		30	ns
230	Delay time, SBCLK high to either SHRQ low or $\overline{\text{SBRQ}}$ high		25	ns
240†	Setup time, $\overline{\text{SUDS}}$, $\overline{\text{SLDS}}$, SRNW, and $\overline{\text{SAS}}$ control signals in the high-impedance state before $\overline{\text{SOWN}}$ no longer low	0		ns

† This specification has been characterized to meet stated value.

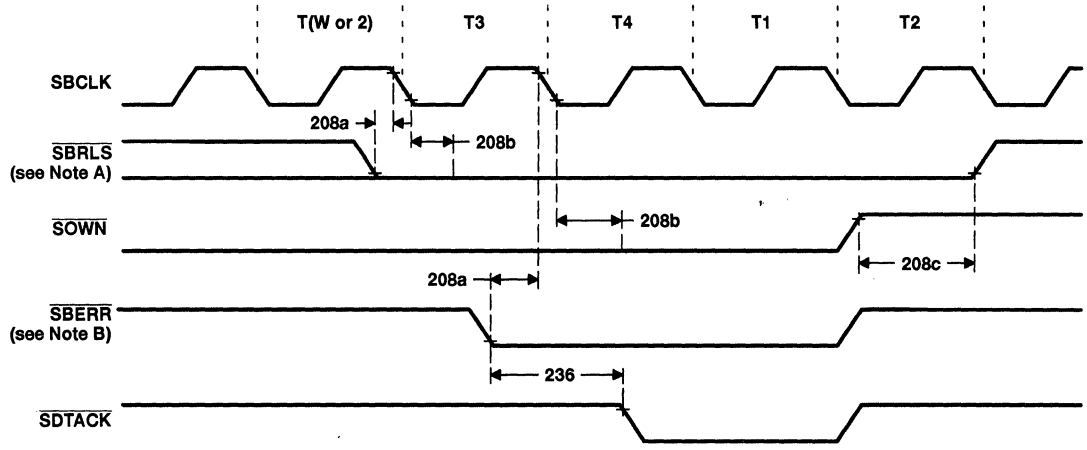


NOTE A: In 80x8x mode, the system-interface deasserts SHRQ on the rising edge of SBCLK following the T4 state of the last system bus transfer it controls. In 68xxx mode, the system-interface deasserts SBRQ on the rising edge of SBCLK in state T2 of the first system bus transfer it controls.

Figure 40. 68xxx-Mode Bus-Arbitration Timing, SIF Returns Control

68xxx-mode bus-release and error timing

NO.		MIN	MAX	UNIT
208a	Setup time, asynchronous input before SBCLK no longer high to assure recognition	15		ns
208b	Hold time, asynchronous input $\overline{\text{SBRLS}}$, $\overline{\text{SOWN}}$, or $\overline{\text{SBERR}}$ after SBCLK low to assure recognition	15		ns
208c	Hold time, $\overline{\text{SBRLS}}$ low after $\overline{\text{SOWN}}$ high	0		ns
236	Setup time, $\overline{\text{SBERR}}$ low before $\overline{\text{SDTACK}}$ no longer high if parameter 208a not met	30		ns



NOTES: A. The system interface ignores the assertion of $\overline{\text{SBRLS}}$ if it does not own the system bus. If it does own the bus when it detects the assertion of $\overline{\text{SBRLS}}$, it completes any internally started DMA cycle and relinquish control of the bus. If no DMA transfer has internally started, the system interface releases the bus before starting another.

B. If $\overline{\text{SBERR}}$ is asserted when the system interface controls the system bus, the current bus transfer is completed regardless of the value of $\overline{\text{SDTACK}}$. If the BERETRY register is nonzero, the cycle is retried. If the BERETRY register is zero, the system interface releases control of the system bus. The system interface ignores the assertion of $\overline{\text{SBERR}}$ if it is not performing a DMA bus cycle on the system bus. When $\overline{\text{SBERR}}$ is properly asserted and BERETRY is zero, however, the system interface releases the bus upon completion of the current bus transfer and halts all further DMA on the system side. The error is synchronized to the local bus and DMA stops on the local sides. The value of the SDMAADR, SDMADDRX, and SDMALEN registers in the system interface are not defined after a system-bus error.

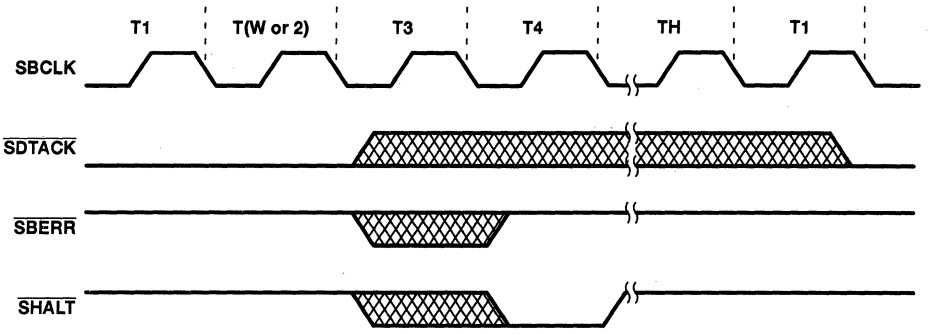
C. In cycle-steal mode, state TX is present on every system-bus transfer. In burst mode, state TX is present on the first bus transfer and whenever the increment of the DMA address register carries beyond the least significant 16 bits.

D. $\overline{\text{SDTACK}}$ is not sampled to verify that it is deasserted.

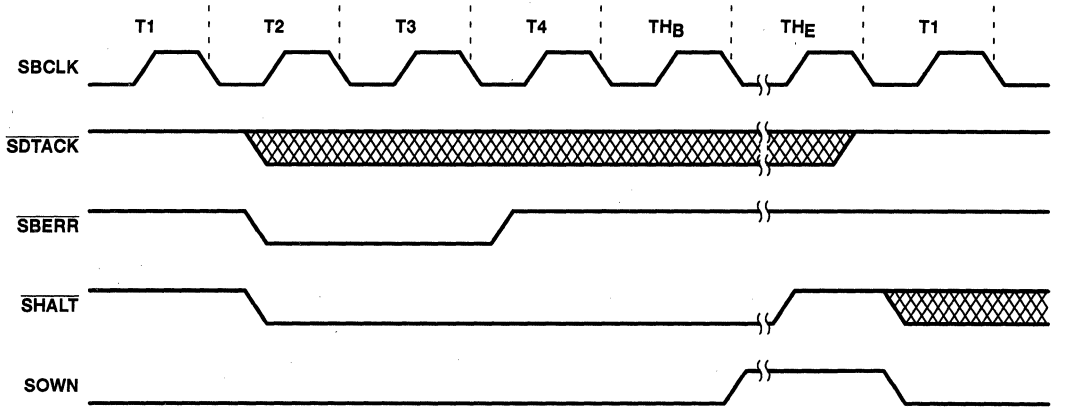
E. Unless otherwise specified, for all signals specified as a maximum delay from the end of an SBCLK transition to the signal valid, the signal is also specified to hold its previous value (including high impedance) until the start of that SBCLK transition.

Figure 41. 68xxx-Mode Bus-Release and Error Timing

normal completion with delayed start†



rerun cycle with delayed start†

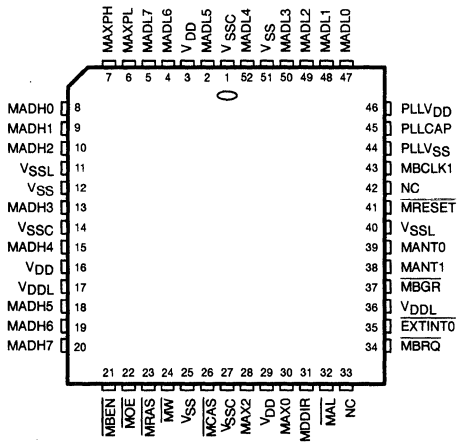


† Only the relative placement of the edges to SBCLK falling edge is shown. Actual signal edge placement may vary from waveforms shown.

Figure 42. 68xxx Bus Halt and Retry Cycle Waveforms

- **Frame-Processing Accelerator for TMS380C2x Adapters**
- **Supports TMS380C2x Token-Ring Adapters**
- **Supports TMS380C2x Ethernet™ Adapters**
- **Interfaces Directly to TMS380C2x Network Commprocessors**
- **Hardware Capture of Network Statistics**
- **Increases Adapter-Frame-Processing Rate Up to 28K Frames per Second**
- **Single 5-V Supply**
- **0.8-μm CMOS Technology**
- **250-mA Typical Latch-Up Immunity at 25°C**
- **ESD Protection Exceeds 2,000 V**
- **52-Pin Plastic Leaded Chip Carrier (FN)**
- **Operating Temperature Range 0°C to 70°C**

FN PACKAGE
(TOP VIEW)



description

The TMS380FPA frame processing accelerator (FPA) provides hardware to accelerate the processing rate of frames by the network communications processor (commprocessor). The CPU of a normal TMS380C2x adapter is responsible for frame transport between network and host, gathering adapter and network statistics, local-network-management protocols, and medium-access-control (MAC) protocols. The TMS380FPA puts the performance bottlenecks of frame transport and statistics gathering into dedicated hardware, leaving the CPU to run MAC and management protocols.

The TMS380FPA is responsible for:

- Management of all commprocessor protocol handler (PH) operations. The FPA manages all receive and transmit frame queues.
- Management of adapter buffers. The FPA manages all adapter memory buffers, allocating them to the appropriate queues as required.
- Management of host DMA by way of the commprocessor system interface (SIF) DMA controller.
- Management of frame transfers to the host. The FPA manages queues of frames to and from the host, manages rx/tx list information, and coordinates the two.
- Gathering adapter and network statistics in dedicated hardware counters.

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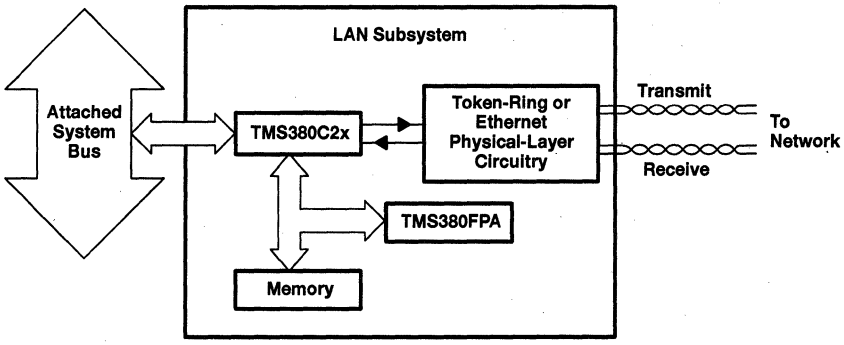

Figure 1. Network-Commprocessor Applications Diagram

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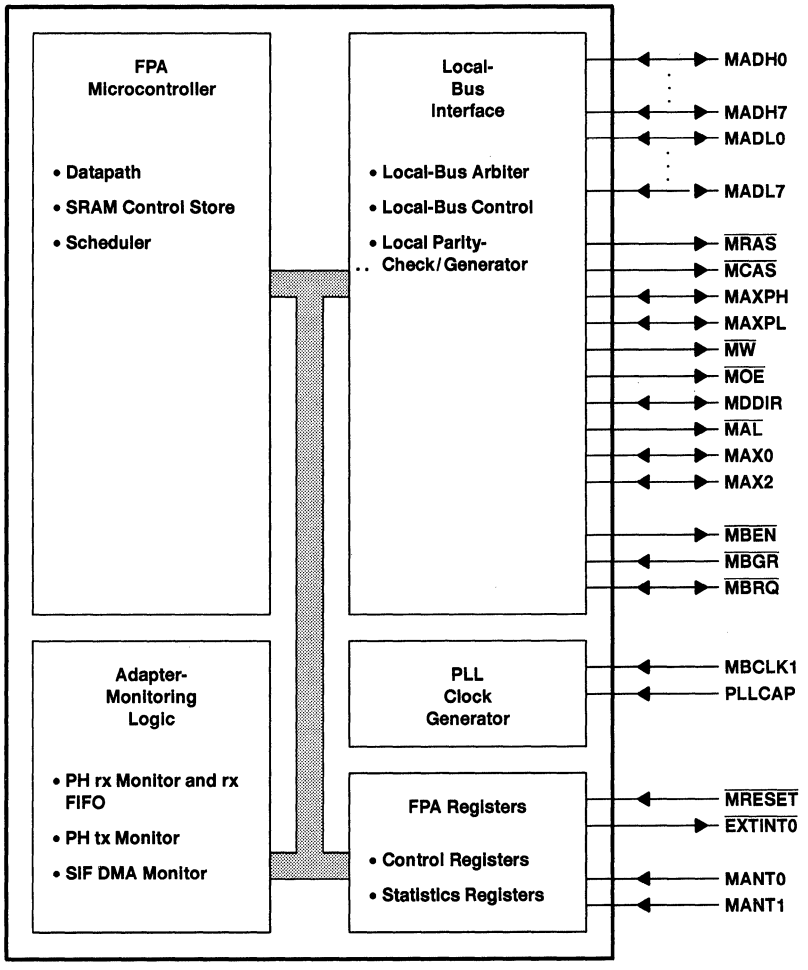
functional block diagram

TMS380FPA attaches directly to the adapter local memory bus of a TMS380C2x COMMprocessor. Generally, FPA pins should be directly connected to like-named pins of the TMS380C2x.



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Pin Functions

PIN NAME	NO.	I/O†	DESCRIPTION
$\overline{\text{EXTINT0}}$	35	O	FPA interrupt request (see Note 1)
MADH0 MADH1 MADH2 MADH3 MADH4 MADH5 MADH6 MADH7	8 9 10 13 15 18 19 20	I/O	Local-memory address, data, and status bus – high byte. For the first quarter of the local-memory cycle, these bus lines carry address bits AX4 and A0 to A6; for the second quarter, they carry status bits; and for the third and fourth quarters, they carry data bits 0 to 7. The most significant bit is MADH0, and the least significant bit is MADH7. Memory Cycle 1Q 2Q 3Q 4Q Signal AX4,A0–A6 Status D0–D7 D0–D7
MADL0 MADL1 MADL2 MADL3 MADL4 MADL5 MADL6 MADL7	47 48 49 50 52 2 4 5	I/O	Local-memory address, data, and status bus – low byte. For the first quarter of the local-memory cycle, these bus lines carry address bits A7 to A14; for the second quarter, they carry address bits AX4 and A0 to A6; and for the third and fourth quarters, they carry data bits 8 to 15. The most significant bit is MADL0, and the least significant bit is MADL7. Memory Cycle 1Q 2Q 3Q 4Q Signal A7–A14 AX4,A0–A6 D8–D15 D8–D15
$\overline{\text{MAL}}$	32	O	Memory-address latch. $\overline{\text{MAL}}$ is a strobe signal for sampling the address at the start of the memory cycle; it is used by SRAMs and EPROMs. The full 20-bit word address is valid on MAX0, MAXPH, MAX2, MAXPL, MADH0–MADH7, and MADL0–MADL7. Three 8-bit transparent latches can be used to retain a 20-bit static address throughout the cycle. Rising edge = No signal latching Falling edge = Allows the above address signals to be latched
MANT0 MANT1	39 38	I	Test pin inputs. MANT0 and MANT1 should be left unconnected (see Note 2). Module-in-place test mode is achieved by tying MANT0 and MANT1 to ground. In this mode, all TMS380FPA output pins are in high-impedance state and internal pullups on all TMS380FPA inputs are disabled (except MANT0 and MANT1).
MAX0	30	I/O	Local-memory-extended address bit. MAX0 drives AX0 at row address time, which can be located by $\overline{\text{MRAS}}$. Normally, MAX0 drives A12 at column address and data time for all cycles. Memory Cycle 1Q 2Q 3Q 4Q Signal AX0 A12 A12 A12
MAX2	28	I/O	Local-memory-extended address bit. MAX2 drives AX2 at row address time, which can be located by $\overline{\text{MRAS}}$. Normally, MAX2 drives A14 at column address and data time for all cycles. Memory Cycle 1Q 2Q 3Q 4Q Signal AX2 A14 A14 A14
MAXPH	7	I/O	Local-memory-extended address and parity–high byte. For the first quarter of a memory cycle, MAXPH carries the extended address bit AX1; for the second quarter of a memory cycle, MAXPH carries the extended address bit AX0; and for the last half of the memory cycle, MAXPH carries the parity bit for the high-data byte. Memory Cycle 1Q 2Q 3Q 4Q Signal AX1 AX0 Parity Parity

† I = input, O = output

NOTES: 1. Pin has an open-collector output. $\overline{\text{EXTINT0}}$ should have an individual 1-kΩ pullup resistor. A 4.7-kΩ resistor can lead to transmit underruns in the adapter system and should not be used. For this reason, a 1-kΩ resistor is specified.

2. Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch or loads). Alternatively, both pins together and pulled high can be tied through a single 4.7-Ω pullup resistor.

Pin Functions (Continued)

PIN NAME	NO.	I/O†	DESCRIPTION
MAXPL	6	I/O	Local-memory-extended address and parity – low byte. For the first quarter of a memory cycle, MAXPL carries the extended address bit AX3; for the second quarter of a memory cycle, MAXPL carries extended address bit AX2; and for the last half of the memory cycle, MAXPL carries the parity bit for the low-data byte. Memory Cycle 1Q 2Q 3Q 4Q Signal AX3 AX2 Parity Parity
$\overline{\text{MBEN}}$	21	O	Buffer enable. $\overline{\text{MBEN}}$ enables the bidirectional buffer outputs on the MADH, MAXPH, MAXPL, and MADL buses during the data phase. $\overline{\text{MBEN}}$ is used in conjunction with MDDIR, which selects the buffer output direction. H = Buffer output disabled L = Buffer output enabled
$\overline{\text{MBGR}}$	37	I	Local bus grant. $\overline{\text{MBGR}}$ indicates that the FPA has been granted access to the adapter local-memory bus.
$\overline{\text{MBRQ}}$	34	I/O	Local bus request. $\overline{\text{MBRQ}}$ is used by the FPA to request bus-master access to the adapter local-memory bus. The FPA also monitors $\overline{\text{MBRQ}}$ to allow it to defer to other higher-priority bus requests (see Note 1).
$\overline{\text{MCAS}}$	26	O	Column-address strobe for DRAMs. The column address is valid for the 3/16 of the memory cycle following the row-address portion of the cycle. $\overline{\text{MCAS}}$ is driven low every memory cycle while the column address is valid on MADL0–MADL7, MAXPH, and MAXPL, except when one of the following conditions occurs: 1) When the address accessed is a TMS380C2x internal register (>01.0100 – >01.01FF). 2) When the address accessed is in the TMS380C2x external device-address range (>01.0200 – >01.02FF). This address range includes the FPA registers. 3) When the FPA ROM bit is set, and the address accessed is in adapter ROM-address range (>00.0000–>00.FFFE or >1F.0000–>1F.FFFE).
MDDIR	31	I/O	Data direction. MDDIR is used as a direction control for bidirectional bus drivers. MDDIR becomes valid before $\overline{\text{MBEN}}$ becomes active. H = TMS380FPA memory bus write L = TMS380FPA memory bus read
$\overline{\text{MOE}}$	22	O	Memory output enable. $\overline{\text{MOE}}$ is used to enable the outputs of the DRAM memory during a read cycle. $\overline{\text{MOE}}$ is high for EPROM or BIA ROM read cycles. 1) When the address read is a TMS380C2x internal register (>01.0100–>01.01FF). 2) When the address read is in the TMS380C2x external device-address range (>01.0200–>01.02FF). This address range includes the FPA registers. 3) When the FPA ROM bit is set, and the address read is in adapter ROM-address range (>00.0000–>00.FFFE or 1F.0000–1F.FFFE). H= Disable DRAM outputs L = Enable DRAM outputs
$\overline{\text{MRAS}}$	23	O	Row-address strobe for DRAMs. The row address lasts for the first 5/16 of the memory cycle. $\overline{\text{MRAS}}$ is driven low every memory cycle while the row address is valid on MADL0–MADL7, MAXPH, and MAXPL for both RAM and register-access cycles.
$\overline{\text{MRESET}}$	41	I	Memory bus reset. $\overline{\text{MRESET}}$ is the reset signal provided by the TMS380C2x and is used to reset and initialize the FPA internal logic. While $\overline{\text{MRESET}}$ is asserted, all FPA output pins are in the high-impedance state.

† I = input, O = output

NOTE 1: Pin has an open-collector output. $\overline{\text{EXTINT0}}$ should have an individual 1-kΩ pullup resistor. A 4.7-kΩ resistor can lead to transmit underruns in the adapter system and should not be used. For this reason, a 1-kΩ resistor is specified.

ADVANCE INFORMATION

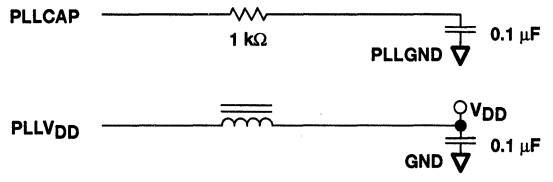
Pin Functions (Continued)

PIN NAME	PIN NO.	I/O†	DESCRIPTION
$\overline{MW}$	24	O	Local-memory write. $\overline{MW}$ is used to specify a write cycle on the local-memory bus. The data on the MADH0–MADH7 and MADL0–MADL7 buses is valid while $\overline{MW}$ is low. DRAMs latch data on the falling edge $\overline{MW}$, while SRAMs latch data on the rising edge of $\overline{MW}$. H = Not a local memory write cycle L = Local memory write cycle
NC	33 42		No connect. Do not connect these pins.
MBCLK1	43	I	Local-bus clock 1. MBCLK1 is referenced for all local-bus transfers.
PLLCAP	45	I	Phase-locked loop (PLL) tuning capacitor (see Note 3).
V_{DDL}	17 36	I	Positive-supply voltage for digital logic. All V_{DDL} pins must be attached to the common-system power-supply plane.
V_{DD}	3 16 29	I	Positive-supply voltage for output buffers. All V_{DDL} pins must be attached to the common-system power-supply plane.
$PLLV_{DD}$	46	I	Positive-supply voltage for phase-locked loop (see Note 4).
V_{SSC}	1 14 27	I	Ground reference for output buffers (clean ground). All V_{SSC} pins must be attached to the common-system-ground plane.
V_{SSL}	11 40	I	Ground reference for digital logic. All V_{SSL} pins must be attached to the common-system-ground plane.
V_{SS}	12 25 51	I	Ground connections for output buffers. All V_{SS} pins must be attached to common-system-ground plane.
$PLLV_{SS}$	44	I	Ground reference for phase-locked loop. Attach to the common-system-ground plane.

† I = input, O = output

NOTES: 3. The PLLCAP requires the following connection: These components must be placed as close as possible to PLLCAP.

4. Isolate $PLLV_{DD}$ to a separate PLL power pad with ferrite bead separation from the common-system power-supply plane. A 0.1-μF decoupling capacitor on $PLLV_{DD}$ is also necessary as shown. These components must be placed as close as possible to $PLLV_{DD}$.



ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 5) ..... – 0.6 to 7 V
Input voltage range (see Note 5) ..... – 0.3 V to 20 V
Output voltage range ..... – 2 V to 7 V
Power dissipation ..... 0.5 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 5: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage (see Note 6)	0	0	0	V
V_{IH}	High-level input voltage	2.0		V_{DD}+0.3	V
V_{IL}	Low-level input voltage, TTL-level signal (see Note 7)	–0.3		0.8	V
I_{OH}	High-level output current			–400	μA
I_{OL}	Low-level output current (see Note 8)			2	mA
T_A	Operating free-air temperature	0		70	°C

NOTES: 6. All V_{SS} pins should be routed to minimize inductance to system ground.
7. The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used for logic-voltage levels only.
8. Output current of 2 mA is sufficient to drive five low-power Schottky TTL loads or ten advanced low-power Schottky TTL loads (worst case).

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS (SEE NOTE 9)		MIN	MAX	UNIT
V_{OH}	High-level output voltage, TTL-level signal (see Note 10)	V_{DD} = MIN,	I_{OH} = MAX	2.4		V
V_{OL}	Low-level output voltage, TTL-level signal	V_{DD} = MIN,	I_{OL} = MAX		0.6	V
I_O	High-impedance output current	V_{DD} = MAX,	V_O = 2.4 V		20	μA
		V_{DD} = MAX,	V_O = 0.4 V		– 20	
I_I	Input current, any input or input/output pin	V_I = V_{SS} to V_{DD}			± 20	μA
I_{DD}	Supply current	V_{DD} = MAX			110	mA
C_i	Input capacitance, any input	f = 1 MHz,	Others at 0 V		15	pF
C_o	Output capacitance, any output or input/output	f = 1 MHz,	Others at 0 V		15	pF

NOTES: 9. For conditions shown as MIN or MAX, use the appropriate value specified under the recommended operating conditions.
10. The following signals require an external pullup resistor: $\overline{\text{EXTINT0}}$ and $\overline{\text{MBRQ}}$.

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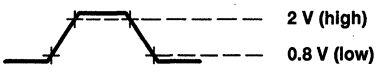
test measurement

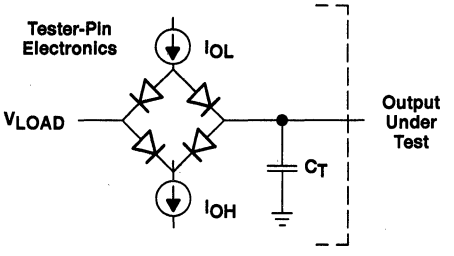
Outputs are driven to a minimum high-logic level of 2.4 V and to a maximum low-logic level of 0.6 V. These levels are compatible with TTL devices.

Output transition times are specified as follows: for a high-to-low transition on either an input or output signal, the level at which the signal is said to be no longer high is 2 V, and the level at which the signal is said to be low is 0.8 V. For a low-to-high transition, the level at which the signal is said to be no longer low is 0.8 V, and the level at which the signal is said to be high is 2 V, as shown below.

The rise and fall times are not specified but are assumed to be those of standard TTL devices, which are typically 1.5 ns.



The test load circuit shown in Figure 3 represents the programmable load of the tester-pin electronics, that are used to verify timing parameters of TMS380FPA output signals.



Where: I_{OL} = 2 mA DC-level verification (all outputs)
I_{OH} = 400 μA (all outputs)
V_{LOAD} = 1.5 V, typical dc-level verification
0.7 V, typical timing verification
C_T = 65 pF, typical load-circuit capacitance

Figure 2. Test-Load Circuit

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timing parameters

The timing parameters for all the pins of TMS380FPA are shown in the following tables and are illustrated in the accompanying figures. The purpose of these figures and tables is to quantify the timing relationships among the various signals. The parameters are numbered for convenience.

static signals

The following table lists signals that are not allowed to change dynamically and have no timing associated with them. They should be strapped high or low as required.

SIGNAL	FUNCTION
MANT0	Test pin for TI manufacturing test†
MANT1	Test pin for TI manufacturing test†

† For unit-in-place test

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as shown below:

DR	DRVR	RS	$\overline{\text{SRESET}}$
DRN	$\overline{\text{DRVR}}$	VDD	V_{DDL}, V_{DDB}
OSC	OSCIN		
SCK	SBCLK		

Lower-case subscripts are defined as follows:

c	cycle time	r	rise time
d	delay time	sk	skew
h	hold time	su	setup time
w	pulse duration (width)	t	transition time

The following additional letters and phrases are defined as follows:

H	High	Z	High impedance
L	Low	Falling edge	No longer high
V	Valid	Rising edge	No longer low

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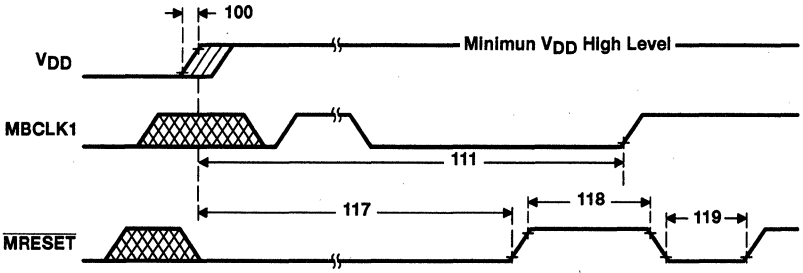
power up, MBCLK1, $\overline{\text{MRESET}}$ timing

NO.			MIN	MAX	UNIT
100†	$t_{r(VDD)}$	Rise time, 1.2 V to minimum V_{DD}-high level		1	ms
111†	$t_{d(CKV)}$	Delay time, minimum V_{DD}-high level to MBCLK1 valid		3	ms
117†	$t_{h(VDDH-RSL)}$	Hold time, $\overline{\text{MRESET}}$ low after V_{DD} reaches minimum high level	5		ms
118†	$t_{w(RSH)}$	Pulse duration, $\overline{\text{MRESET}}$ high	14		µs
119†	$t_{w(RSL)}$	Pulse duration, $\overline{\text{MRESET}}$ low	14		µs

† This specification is provided as an aid to board design. This specification is not tested.



NOTE A: In order to represent the information on one illustration, nonactual phase and timebase characteristics are shown. Refer to specified parameters for precise information.

Figure 3. Power Up, MBCLK1, and $\overline{\text{MRESET}}$ Timing

clock timing: MBCLK1

NO.		MIN	MAX	UNIT
1	Period of MBCLK1	125		ns
2	Pulse duration, MBCLK1 high	53		ns
3	Pulse duration, MBCLK1 low	53		ns
4	Transition time, MBCLK1	5		ns

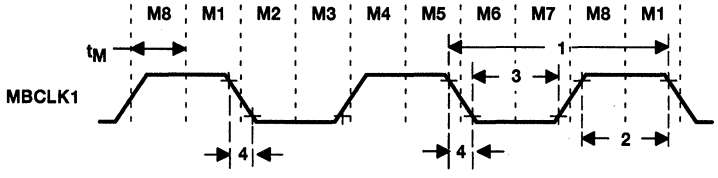


Figure 4. Clock Timing: MBCLK1

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FPA-bus-master timing: $\overline{\text{MAL}}$, $\overline{\text{MRESET}}$, and ADDRESS

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum).

NO.		MIN	MAX	UNIT
8	Setup time, address/enable on MAX0 and MAX2 before MBCLK1 no longer high	t_M-9		ns
9	Setup time, row address on MADL0–MADL7, MAXPH, and MAXPL before MBCLK1 no longer high	t_M-14		ns
10	Setup time, address on MADH0–MADH7 before MBCLK1 no longer high	t_M-14		ns
11	Setup time, $\overline{\text{MAL}}$ high before MBCLK1 no longer high	t_M-13		ns
12	Setup time, address on MAX0 and MAX2 before MBCLK1 no longer low	$0.5t_M-9$		ns
13	Setup time, column address on MADL0–MADL7, MAXPH, and MAXPL before MBCLK1 no longer low	$0.5t_M-9$		ns
14	Setup time, status on MADH0–MADH7 before MBCLK1 no longer low	$0.5t_M-9$		ns
126	Delay time, MBCLK1 no longer low to $\overline{\text{MRESET}}$ valid	0	20	ns
129	Hold time, column address/status after MBCLK1 no longer low	t_M-7		ns

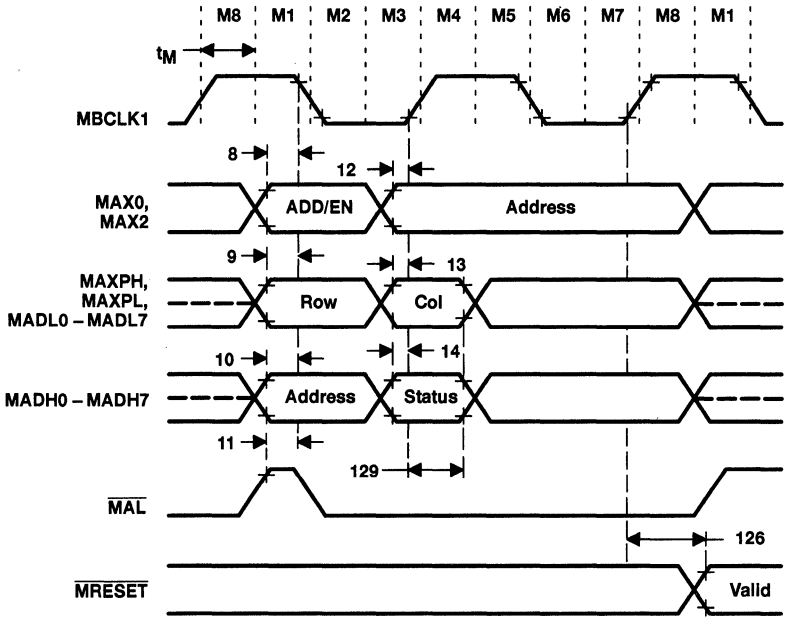

Figure 5. FPA-Bus-Master Timing: $\overline{\text{MAL}}$, $\overline{\text{MRESET}}$, and ADDRESS

ADVANCE INFORMATION

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FPA-bus-master timing: $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, and $\overline{\text{MAL}}$ to ADDRESS

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum).

NO.		MIN	MAX	UNIT
15	Setup time, row address on MADL0–MADL7, MAXPH, and MAXPL before $\overline{\text{MRAS}}$ no longer high	$1.5t_M - 11.5$		ns
16	Hold time, row address on MADL0–MADL7, MAXPH, and MAXPL after $\overline{\text{MRAS}}$ no longer high	$t_M - 6.5$		ns
17	Delay time, $\overline{\text{MRAS}}$ no longer high to $\overline{\text{MRAS}}$ no longer high in the next memory cycle	$8t_M$		ns
18	Pulse duration, $\overline{\text{MRAS}}$ low	$4.5t_M - 9$		ns
19	Pulse duration, $\overline{\text{MRAS}}$ high	$3.5t_M - 9$		ns
20	Setup time, column address (MADL0–MADL7, MAXPH, and MAXPL) and status (MADH0–MADH7) before $\overline{\text{MCAS}}$ no longer high	$0.5t_M - 9$		ns
21	Hold time, column address (MADL0–MADL7, MAXPH, and MAXPL) and status (MADH0–MADH7) after $\overline{\text{MCAS}}$ low	$t_M - 9$		ns
22	Hold time, column address (MADL0–MADL7, MAXPH, and MAXPL) and status (MADH0–MADH7) after $\overline{\text{MRAS}}$ no longer high	$2.5t_M - 6.5$		ns
23	Pulse duration, $\overline{\text{MCAS}}$ low	$3t_M - 9$		ns
24	Pulse duration, $\overline{\text{MCAS}}$ high, refresh cycle follows read or write cycle	$2t_M - 9$		ns
25	Hold time, row address on MADL0–MADL7, MAXPH, and MAXPL after $\overline{\text{MAL}}$ low	$1.5t_M - 9$		ns
26	Setup time, row address on MADL0–MADL7, MAXPH, and MAXPL before $\overline{\text{MAL}}$ no longer high	$t_M - 9$		ns
27	Pulse duration, $\overline{\text{MAL}}$ high	$t_M - 9$		ns
28	Setup time, address/enable on MAX0 and MAX2 before $\overline{\text{MAL}}$ no longer high	$t_M - 9$		ns
29	Hold time, address/enable of MAX0 and MAX2 after $\overline{\text{MAL}}$ low	$1.5t_M - 9$		ns
30	Setup time, address on MADH0–MADH7 before $\overline{\text{MAL}}$ no longer high	$t_M - 9$		ns
31	Hold time, address on MADH0–MADH7 after $\overline{\text{MAL}}$ low	$1.5t_M - 9$		ns

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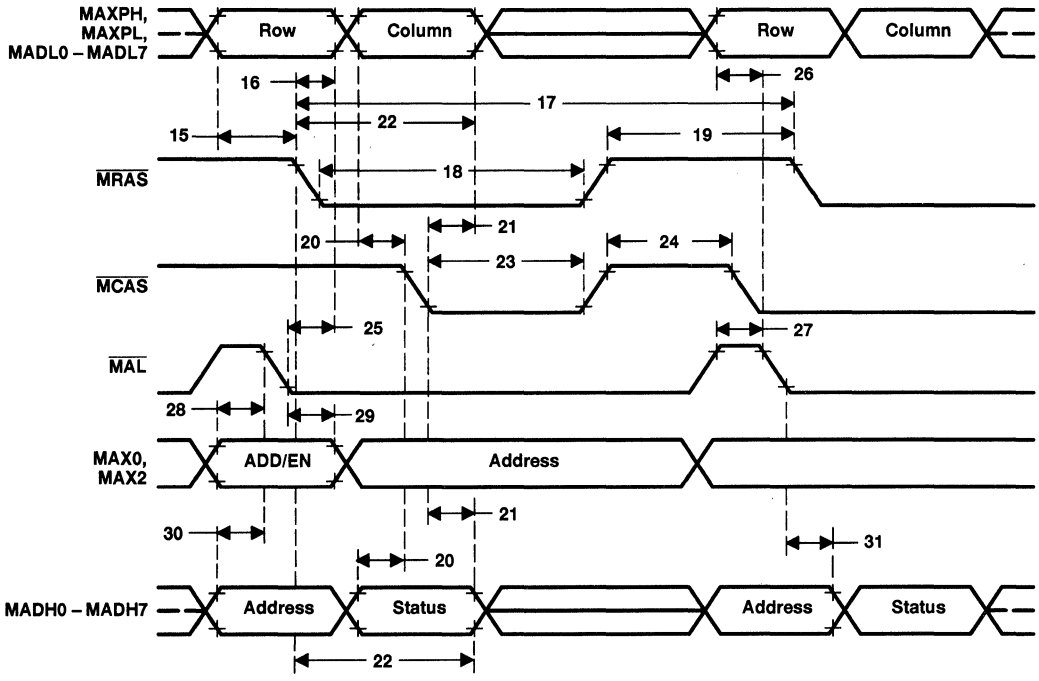

Figure 6. FPA-Bus-Master Timing: $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, and $\overline{\text{MAL}}$ to ADDRESS

ADVANCE INFORMATION

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FPA-bus-master timing: read cycle

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum).

NO.		MIN	MAX	UNIT
32	Access time, address/enable valid on MAX0 and MAX2 to valid data/parity		$6t_M - 23$	ns
33	Access time, address valid on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 to valid data/parity		$6t_M-23$	ns
35	Access time, $\overline{MRAS}$ low to valid data/parity		$4.5t_M-21.5$	ns
36	Hold time, valid data/parity after $\overline{MRAS}$ no longer low	0		ns
37†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7 and MADL0–MADL7 after $\overline{MRAS}$ high (see Note 11)	$2t_M-10.5$		ns
38	Access time, $\overline{MCAS}$ low to valid data/parity		$3t_M-23$	ns
39	Hold time, valid data/parity after $\overline{MCAS}$ no longer low	0		ns
40†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{MCAS}$ high (see Note 11)	$2t_M-13$		ns
41	Delay time, $\overline{MCAS}$ no longer high to $\overline{MOE}$ low		t_M+13	ns
42†	Setup time, address/status in the high-impedance state on MAXPH, MAXPL, MADL0–MADL7, and MADH0–MADH7 before $\overline{MOE}$ no longer high	0		ns
43	Access time, $\overline{MOE}$ low to valid data/parity		$2t_M-25$	ns
44	Pulse duration, $\overline{MOE}$ low	$2t_M-9$		ns
45	Delay time, $\overline{MCAS}$ low to $\overline{MOE}$ no longer low	$3t_M-9$		ns
46	Hold time, valid data/parity in after $\overline{MOE}$ no longer low	0		ns
47†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{MOE}$ high (see Note 11)	$2t_M-15$		ns
48†	Setup time, address/status in the high-impedance state on MAXPH, MAXPL, MADL0–MADL7, and MADH0–MADH7, before $\overline{MBEN}$ no longer high	0		ns
49	Access time, $\overline{MBEN}$ low to valid data/parity		$2t_M-25$	ns
50	Pulse duration, $\overline{MBEN}$ low	$2t_M-9$		ns
51	Hold time, valid data/parity after $\overline{MBEN}$ no longer low	0		ns
52†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{MBEN}$ high (see Note 11)	$2t_M-15$		ns
53	Hold time, MDDIR high after $\overline{MBEN}$ high, read follows write cycle	$1.5t_M-12$		ns
54	Setup time, MDDIR low before $\overline{MBEN}$ no longer high	$3t_M-9$		ns
55	Hold time, MDDIR low after $\overline{MBEN}$ high, write follows read cycle	$3t_M-12$		ns

† This specification has been characterized to meet stated value. This parameter is not tested.

NOTE 11: The data/parity that exists on the address lines will most likely achieve the high-impedance state sometime later than the rising edge of $\overline{MRAS}$, $\overline{MCAS}$, $\overline{MOE}$, or $\overline{MBEN}$ (between MIN and MAX of timing parameter 36) and will be a function of the memory being read. The MIN time given represents the time from the rising edge of $\overline{MRAS}$, $\overline{MCAS}$, $\overline{MOE}$, or $\overline{MBEN}$ to the beginning of the next address and does not represent the actual high-impedance state on the address bus.

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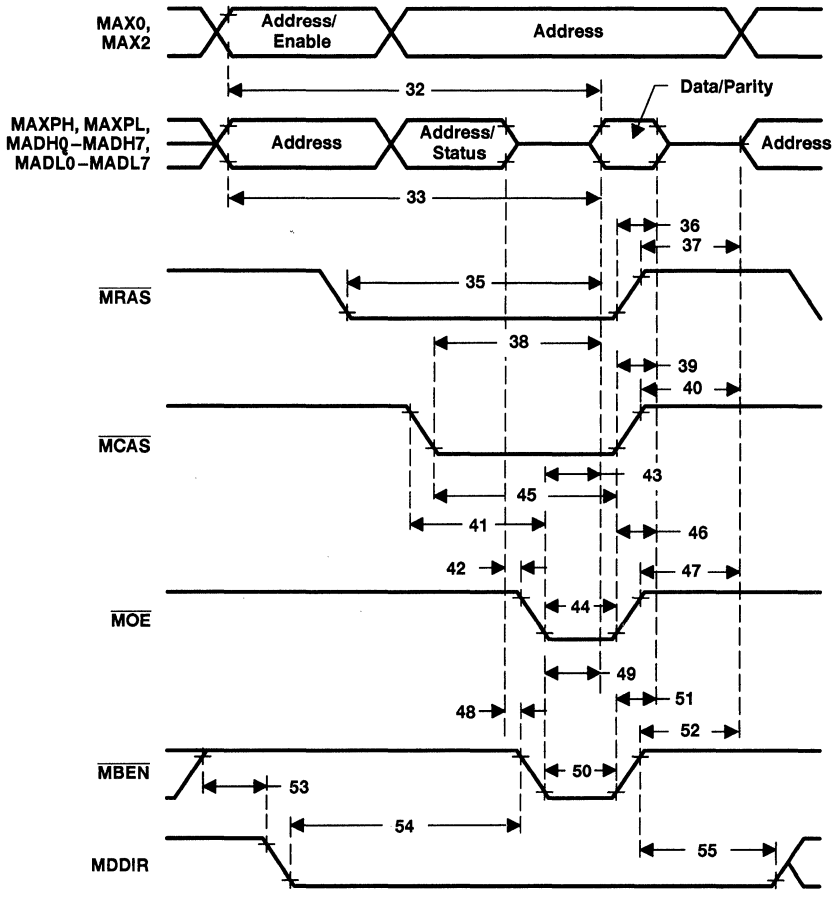

Figure 7. FPA-Bus-Master Timing: Read Cycle

ADVANCE INFORMATION

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FPA-bus-master timing: write cycle

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum).

NO.		MIN	MAX	UNIT
58	Setup time, $\overline{MW}$ low before $\overline{MRAS}$ no longer low	$1.5t_M - 9$		ns
60	Setup time, $\overline{MW}$ low before $\overline{MCAS}$ no longer low	$1.5t_M - 6.5$		ns
63	Setup time, valid data/parity before $\overline{MW}$ no longer high	$0.5t_M - 11.5$		ns
64	Pulse duration, $\overline{MW}$ low	$2.5t_M - 9$		ns
65	Hold time, data/parity out valid after $\overline{MW}$ high	$0.5t_M - 10.5$		ns
66	Setup time, address valid on MAX0 and MAX2 before $\overline{MW}$ no longer low	$7t_M - 11.5$		ns
67	Hold time, $\overline{MRAS}$ low to $\overline{MW}$ no longer low	$5.5t_M - 9$		ns
69	Hold time, $\overline{MCAS}$ low to $\overline{MW}$ no longer low	$4t_M - 11.5$		ns
70	Setup time, $\overline{MBEN}$ low before $\overline{MW}$ no longer high	$1.5t_M - 13.5$		ns
71	Hold time, $\overline{MBEN}$ low after $\overline{MW}$ high	$0.5t_M - 6.5$		ns
72	Setup time, MDDIR high before $\overline{MBEN}$ no longer high	$2t_M - 9$		ns
73	Hold time, MDDIR high after $\overline{MBEN}$ high	$1.5t_M - 12$		ns

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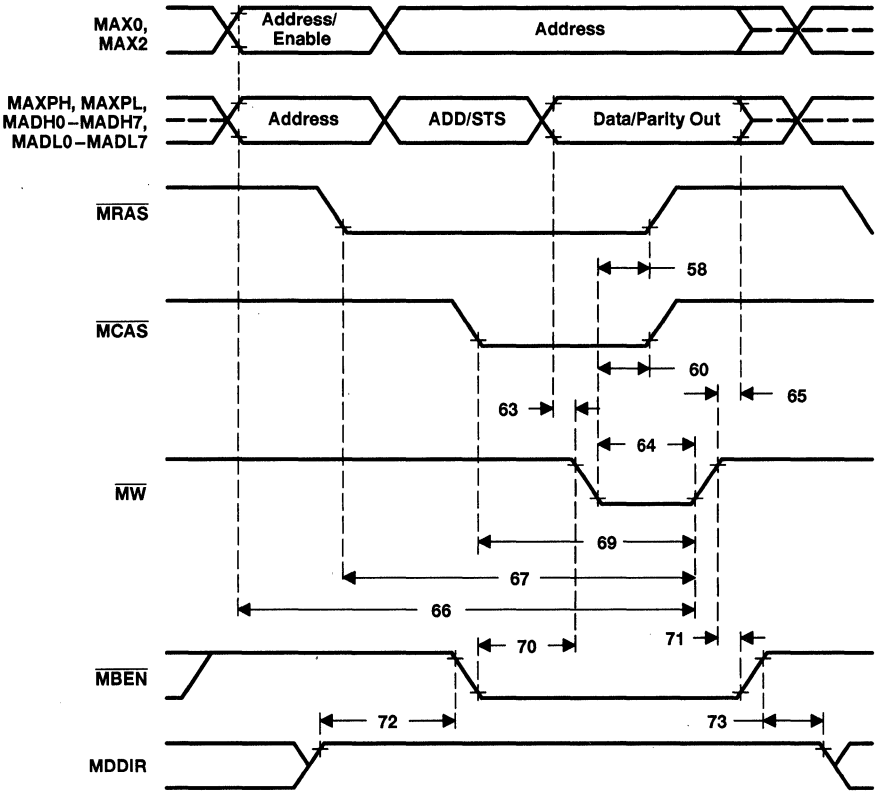

Figure 8. FPA-Bus-Master Timing: Write Cycle

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

FPA-slave timing: read cycle

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum).

NO.		MIN	MAX	UNIT
84	Setup time, address on MAX0, MAX2 before MBCLK1 falling edge, FPA-slave read	10		ns
85	Hold time, address on MAX0, MAX2 after MBCLK1 falling edge, FPA-slave read	0		ns
86	Setup time, valid address before MBCLK1 falling edge, FPA-slave read	10		ns
87	Hold time, valid address after MBCLK1 falling edge, FPA-slave read	0		ns
88	Setup time, address in the high-impedance state before MBCLK1 falling edge, FPA-slave read	0		ns
89	Setup time, data/parity valid after MBCLK1 falling edge, FPA-slave read	$0.5t_M + 10$		ns
90	Hold time, data/parity valid after MBCLK1 falling edge, FPA-slave read	$2t_M$		ns
91	Setup time, data/parity in the high-impedance state after MBCLK1 falling edge, FPA-slave read	$2t_M + 9$		ns
92	Setup time, MDDIR low after MBCLK1 falling edge, FPA-slave read	$t_M - 15$		ns
93	Hold time, MDDIR low after MBCLK1 falling edge, FPA-slave read	t_M		ns

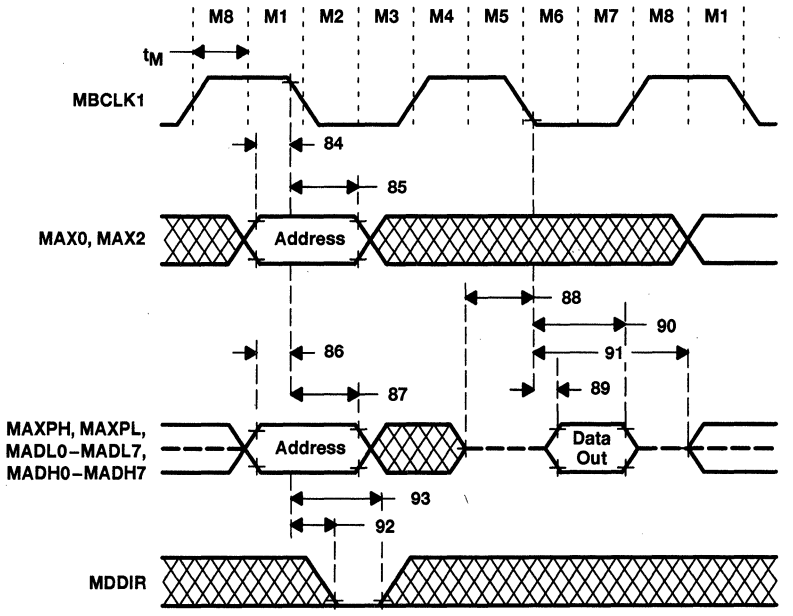

Figure 9. FPA-Slave Timing: Read Cycle

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PARAMETER MEASUREMENT INFORMATION

FPA-slave timing: write cycle

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum).

NO.		MIN	MAX	UNIT
96	Setup time, valid data/parity after MBCLK1 falling edge, FPA-slave write	$t_M - 15$		ns
97	Hold time, valid data/parity after MBCLK1 falling edge, FPA-slave write	t_M		ns
98	Setup time, MDDIR high after MBCLK1 falling edge, FPA-slave write	$t_M - 15$		ns
99	Hold time, MDDIR high after MBCLK1 falling edge, FPA-slave read	t_M		ns

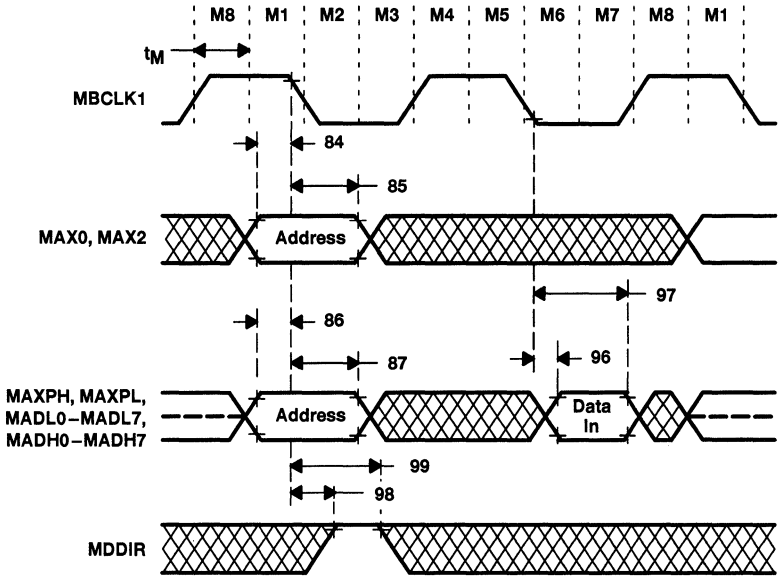

Figure 10. FPA-Slave Timing: Write Cycle

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FPA-slave timing: status monitoring

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum).

NO.		MIN	MAX	UNIT
100	Setup time, valid bus status on MADH0–MADH7 after MBCLK1 falling edge, FPA-slave cycle	$2t_M - 5$		ns
101	Hold time, valid bus status on MADH0–MADH7 after MBCLK1 falling edge, FPA-slave cycle	$2t_M + 10$		ns

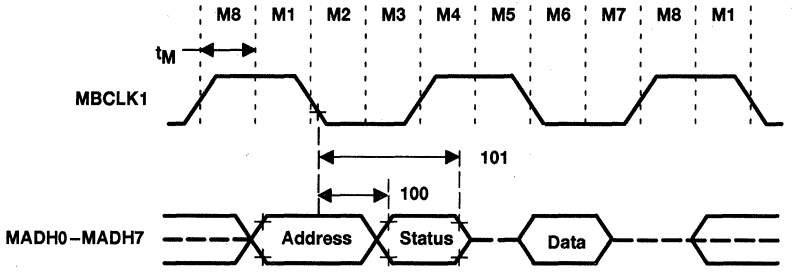


Figure 11. FPA-Slave Timing: Status Monitoring

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

FPA-bus arbitration: arbitration handshake

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum).

NO.		MIN	MAX	UNIT
76	Setup time, $\overline{\text{MBRQ}}$ output low before MBCLK1 falling edge, FPA-bus request	10		ns
77	Hold time, $\overline{\text{MBRQ}}$ output low after MBCLK1 falling edge, FPA-bus request	$3t_M$		ns
78	Delay time, $\overline{\text{MBGR}}$ low after MBCLK1 falling edge, bus granted to FPA	10		ns
81	Setup time, $\overline{\text{MBRQ}}$ input valid before MBCLK1 falling edge, request override	0		ns
82	Hold time, $\overline{\text{MBRQ}}$ input valid before MBCLK1 falling edge, request override	t_M		ns
83	Delay time, $\overline{\text{MBGR}}$ high after MBCLK1 falling edge, bus taken from FPA	0		ns

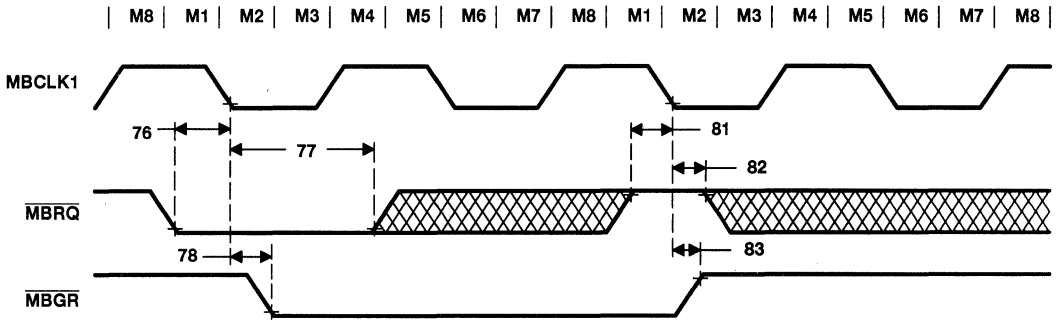


Figure 12. FPA-Bus Arbitration: Arbitration Handshake

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

FPA-bus arbitration: FPA takes control of bus

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum).

NO.		MIN	MAX	UNIT
79	Setup time, FPA in the high-impedance state after MBCLK1 rising edge, bus resume	$2t_M - 13$		ns
80	Delay time, MBCLK1 falling edge to FPA valid, bus resume		$2t_M + 9$	ns

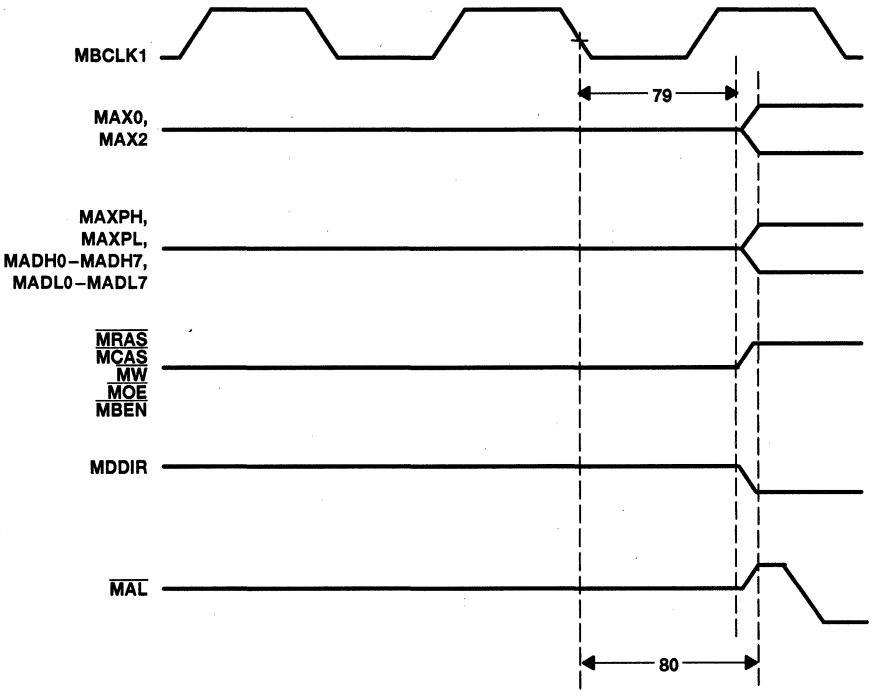


Figure 13. FPA-Bus Arbitration: FPA Takes Control of Bus

PARAMETER MEASUREMENT INFORMATION

FPA-bus arbitration: FPA releases control of bus

t_M is the cycle time of one-eighth of a local-memory cycle (31.25 ns minimum).

NO.		MIN	MAX	UNIT
74	Hold time, FPA after MBCLK1 falling edge, bus release	$2.5t_M - 13$		ns
74a	Hold time, $\overline{\text{MBEN}}$ valid after MBCLK1 falling edge, bus release	$3t_M - 13$		ns
75	Delay time, MBCLK1 falling edge to FPA in the high-impedance state, bus release		$2.5t_M$	ns
75a	Delay time, MBCLK1 falling edge to $\overline{\text{MBEN}}$ in the high-impedance state, bus release		$3t_M$	ns

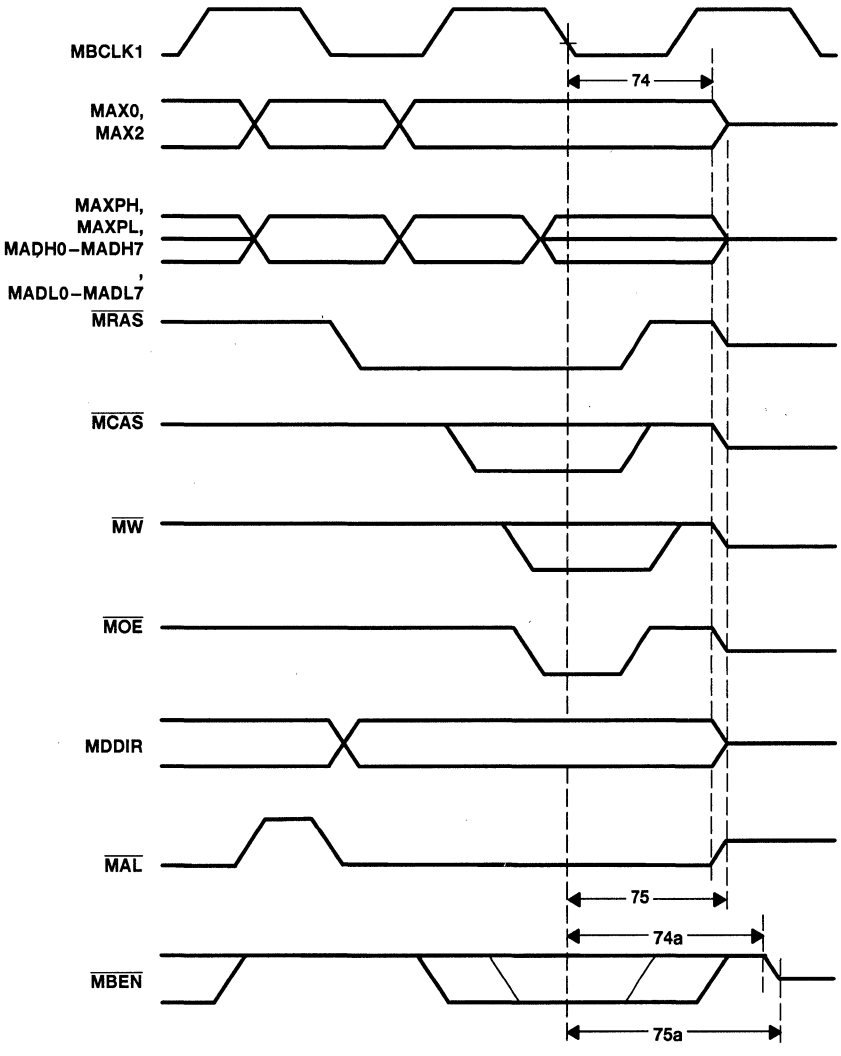
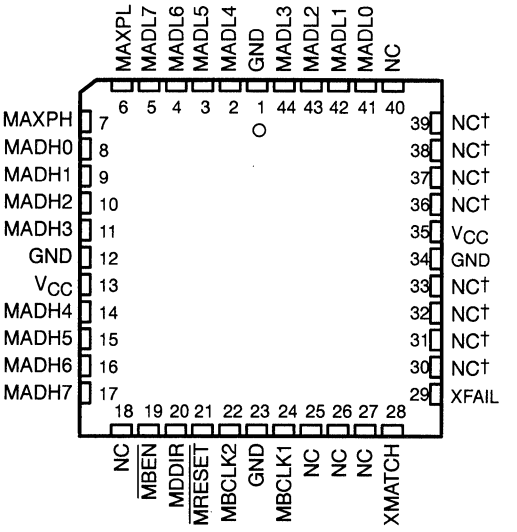


Figure 14. FPA-Bus Arbitration: FPA Releases Control of Bus

ADVANCE INFORMATION

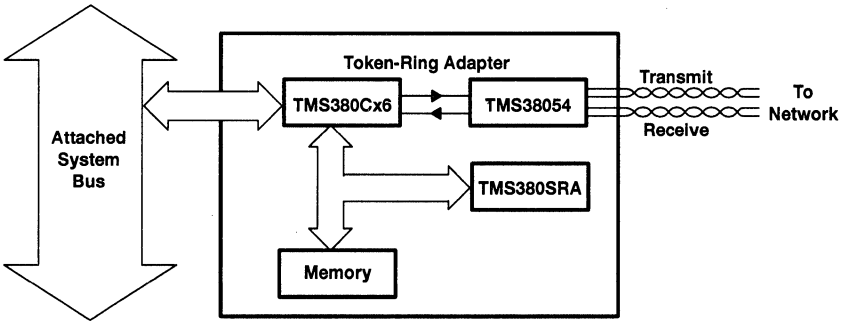
- **Source-Routing Bridge Accelerator for 16-Mbps and 4-Mbps Token-Ring Bridges**
- **Compatible With the IBM Token-Ring Network Architecture**
- **Interfaces Directly to the TMS380Cx6 Second-Generation Network Commprocessor**
- **Provides Automatic Recognition of Source-Routing Field in Token-Ring Frame for Hardware-Accelerated-Frame Copying and High-Performance Bridging**
- **Utilizes TI-Patented Enhanced-Address Copy Option (EACO) Interface of the TMS380Cx6**
- **High-Performance, 1-μm EPIC™ CMOS Technology**
- **44-Pin JEDEC PLCC Surface-Mount Package**

FN PACKAGE
(TOP VIEW)



† These pins must be left externally unconnected.
NC – No internal connection

Token-Ring LAN SRA Applications Diagram



EPIC is a trademark of Texas Instruments Incorporated.

description

The TMS380SRA source-routing accelerator (SRA) device provides the hardware for direct recognition and parsing of the source-routing field in a token-ring frame. The TMS380SRA is designed to interface directly to the TMS380Cx6. The TMS380SRA searches the received frame for frames that need to be forwarded to the adjacent ring by examining the source-routing field. If a frame is to be forwarded, the frame is copied by the adapter and transferred to the attached system through the system interface of the TMS380Cx6. A second adapter with the TMS380SRA can also be included in the attached system (thus forming a bridge) to provide an identical function for the second ring. Transfer of data between the two rings (bridging) occurs under attached system-software control.

A block diagram of the TMS380SRA is shown in Figure 1. The internal registers fall into two categories: registers that can be set by the host software for the specific bridge parameters for this adapter, and dynamic registers that are loaded with the received frames-routing information as read from the adapter bus transfer. The routing information is compared to the specified bridge parameters, which determines the value to be placed on the XMATCH and XFAIL pins. The memory-interface (MIF) address output during memory cycles is shown in Table 1. Status information is provided on the MADH0–MADH7 signals in the second quarter of the memory cycle (shaded area). MADH6 and MADH7 are the bits that can be used by an EACO device. The information provided in these bits during the second quarter of the memory cycle can be decoded as follows:

MADH6	H	=	The TMS380Cx6 PH RX DMA machine is transferring a word of received frame data to memory.
	L	=	At all other times
MADH7	H	=	The TMS380Cx6s PH RX DMA machine is transferring the first word of a new received frame to memory. In a token-ring frame, the first word contains the AC and FC fields.
	L	=	At all other times

The decode of the rest of the status information is shown in Table 2 and Table 3.

The TMS380SRA is available in a 44-lead plastic chip-carrier package (FN suffix) and is characterized for operation from 0°C to 70°C (L suffix). The electrostatic-discharge protection of the TMS380SRA is rated at 500 V human-body model (HBM).

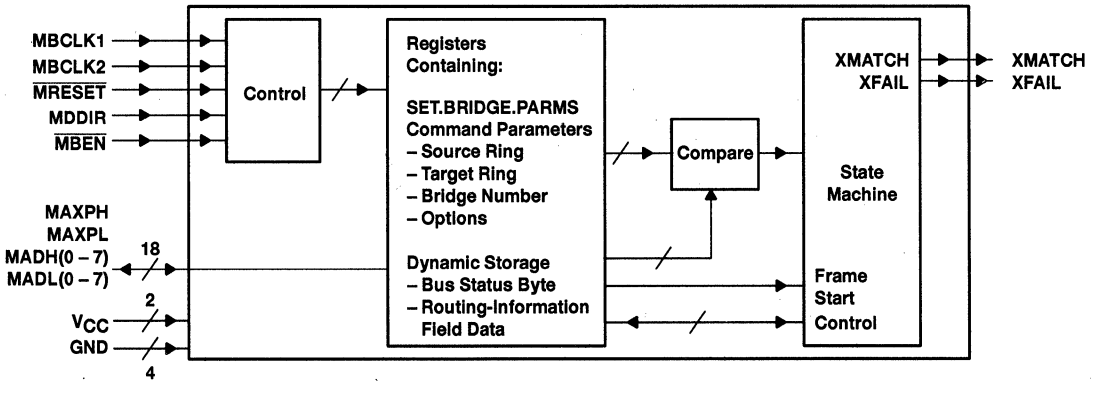


Figure 1. TMS380SRA Block Diagram

Table 1. TMS380Cx6 Address Output During Memory Cycle

PIN	FIRST QUARTER	SECOND QUARTER	REST OF CYCLE
MAX0†	AX0	A12	A12
MAXPH	AX1	AX0	Parity
MAX2†	AX2	A14	A14
MAXPL	AX3	AX2	Parity
MADH0	AX4	Status	Data
MADH1	A0	Status	Data
MADH2	A1	Status	Data
MADH3	A2	Status	Data
MADH4	A3	Status	Data
MADH5	A4	Status	Data
MADH6	A5	Status	Data
MADH7	A6	Status	Data
MADL0	A7	AX4	Data
MADL1	A8	A0	Data
MADL2	A9	A1	Data
MADL3	A10	A2	Data
MADL4	A11	A3	Data
MADL5	A12	A4	Data
MADL6	A13	A5	Data
MADL7	A14	A6	Data
MROMEN†	ROMEN	A13	A13

† These signals do not attach to the TMS380SRA; therefore, there are no corresponding pins.

Table 2. Status Information on MADH0–MADH7

SECOND-QUARTER MEMORY CYCLE	FUNCTION
MADH0	Code/$\overline{\text{data}}$‡
MADH1	Indicates which internal module of the TMS380Cx6 has ownership of the adapter memory bus (see Table 3)‡.
MADH2	
MADH3	
MADH4	
MADH5	SIF DMA active
MADH6	PH RX DMA cycle
MADH7	New RX frame

‡ To the TMS380SRA, these bits are don't care.

Table 3. Decode of Status Information on MADH1–MADH4

MADH1	MADH2	MADH3	MADH4	REPRESENTATION
0	0	0	0	DRAM controller
0	0	0	1	Not assigned
0	0	1	0	PH TX DMA machine
0	0	1	1	PH RX DMA machine
0	1	0	0	PH TX buffer manager
0	1	0	1	PH RX buffer manager
0	1	1	0	SIF DIO machine
0	1	1	1	SIF DMA machine
1	0	0	0	CP (uses bus)
1	0	0	1	CP (does not use bus)
1	0	1	0	Not assigned
1	0	1	1	Not assigned
1	1	0	0	Not assigned
1	1	0	1	Not assigned
1	1	1	0	Program debug controller
1	1	1	1	No memory access

† To the TMS380SRA, these bits are don't care.

Pin Functions

PIN NAME	NO.	I/O/Z‡	DESCRIPTION
MADHO MADH1 MADH2 MADH3 MADH4 MADH5 MADH6 MADH7	8 9 10 11 14 15 16 17	I/O	Adapter-memory address, data and status bus – high byte. For the first quarter of the adapter-memory cycle, these bus lines carry address bits AX4 and A0 to A6; for the second quarter, they carry status bits; and for the third and fourth quarters, they carry data bits 0 to 7. The most significant bit is MADH0 and the least significant bit is MADH7. Memory Cycle Signal: 1Q AX4, A0 – A6; 2Q Status; 3Q D0 – D7; 4Q D0 – D7
MADLO MADL1 MADL2 MADL3 MADL4 MADL5 MADL6 MADL7	41 42 43 44 2 3 4 5	I/O	Adapter-memory address, data and status bus – low byte. For the first quarter of the adapter-memory cycle these bus lines carry address bits A7 to A14; for the second quarter, they carry address bits AX4 and A0 to A6; and for the third and fourth quarters, they carry data bits 8 to 15. The most significant bit is MADL0 and the least significant bit is MADL7. Memory Cycle Signal: 1Q AX7 – A14; 2Q AX4, A0 – A6; 3Q D8 – D15; 4Q D8 – D15
MAXPH	7	I/O	Adapter-memory-extended address and parity – high byte. For the first quarter of a memory cycle, carries the extended address bit (AX1); for the second quarter of a memory cycle, it carries the extended address bit (AX)); and for the last half of the memory cycle, it carries the parity bit for the high data byte. Memory Cycle Signal: 1Q AX1; 2Q AX0; 3Q Parity; 4Q Parity
MAXPL	6	I/O	Adapter-memory-extended address parity – low byte. For the first quarter of the adapter memory cycle, MAXPL carries the extended address bit (AX3), for the second quarter of a memory cycle, it carries extended address bit (AX2); and for the last half of the memory cycle, it carries the parity bit for the low data byte. Memory Cycle Signal: 1Q AX3; 2Q AX2; 3Q Parity; 4Q Parity

‡ Denotes input/output/high-impedance state

Pin Functions (Continued)

PIN NAME	NO.	I/O/Z†	DESCRIPTION
MBCLK1 MBCLK2	24 22	I	Adapter-bus clock 1 and adapter-bus clock 2. MBCLK1 and MBCLK2 are references for all adapter-bus transfers. MBCLK2 lags MBCLK1 by a quarter of a cycle. These clocks operate at 8 MHz for a 64-MHz OSCIN (on the TMS380Cx6) and 6 MHz for a 48-MHz OSCIN (on the TMS380Cx6), which is twice the memory cycle rate. The MBCLK signals are always a divide-by-8 of the OSCIN (on the TMS380Cx6) frequency.
$\overline{\text{MBEN}}$	19	I (see Note 1)	Buffer enable. $\overline{\text{MBEN}}$ enables the bidirectional buffer outputs on the MADH, MAXPH, MAXPL, and MADL buses during the data phase. $\overline{\text{MBEN}}$ is used in conjunction with MDDIR, which selects the buffer output direction. H = Buffer output disabled L = Buffer output enabled
MDDIR	20	I	Data direction. MDDIR is used as a direction control for the bidirectional bus drivers from the TMS380Cx6. MDDIR becomes valid before $\overline{\text{MBEN}}$ becomes active. H = TMS380Cx6 memory-bus write L = TMS380Cx6 memory-bus read
$\overline{\text{MRESET}}$	21	I (see Note 1)	Memory bus reset. $\overline{\text{MRESET}}$ is a reset signal generated when either the ARESET bit in the SIFACL register is set or the $\overline{\text{SRESET}}$ is asserted. This signal is used for resetting external adapter bus glue logic and the TMS380SRA. H = External logic not reset L = External logic reset
XFAIL	29	O	External fail-to-match. The TMS380SRA device uses XFAIL to indicate to the TMS380Cx6 that it should not copy the data frame nor set the ARI/FCI bits due to an external address match. The ARI/FCI bits may still be set by the TMS380Cx6 due to an internal address match (see table in XMATCH description). H = No address match by TMS380SRA L = TMS380SRA armed state
XMATCH	28	O	External match. The TMS380SRA device uses XMATCH to indicate to the TMS380Cx6 to copy the data frame and set the ARI/FCI bits. H = Address match recognized by TMS380SRA L = TMS380SRA armed state XMATCH / XFAIL / Function 0 / 0 / Armed (processing frame data) 0 / 1 / Do *not* externally match the frame 1 / 0 / Copy the frame 1 / 1 / Do *not* externally match the frame Hi-Z / Hi-Z / Reset state (TMS380SRA is in the reset state
V_{CC} (2 pins)	13,35	5-V supply voltage	
GND (4 pins)	1,12,23,34	Ground	
NC (13 pins)		These pins must be unconnected.	

† Denotes input/output/high-impedance state

NOTE 1: Pin has an internal pullup device to maintain a high voltage level when left unconnected (no etch or loads)

operation

The TMS380SRA is designed to be interfaced with the TMS380Cx6 on DRAM-based adapters operating at 4-MHz adapter-bus speed with no external glue logic required. In adapter designs utilizing EPROMs or other devices in addition to DRAMs and a BIA PROM, it may be necessary to buffer the DRAMs in order to reduce the total bus loading below the maximum output load capacitance (50 pF) of the TMS380SRA.

The TMS380SRA control registers are mapped into the TMS380Cx6 memory map at all times, and no external chip-select signal is used. The adapter software controls access to these registers through the SET.BRIDGE.PARMS command (>0010), as described in the TMS380 Second-Generation Token-Ring User's Guide (SPWS005).

operation (continued)

The TMS380SRA is reset by a low-level signal on $\overline{\text{MRESET}}$. The TMS380Cx6 forces a $\overline{\text{MRESET}}$ active during a hardware or software reset of the adapter. In the reset state of the TMS380SRA, XMATCH and XFAIL are in the high-impedance state.

The TMS380SRA is also reset by the SET.BRIDGE.PARMS command before loading the supplied values and conditions for the TMS380SRA to use. If the SET.BRIDGE.PARMS command is supplied with invalid values, the values are not loaded and the device remains in the reset state (disabled).

The TMS380SRA should be placed such that the length of the signal lines between it and the TMS380Cx6 does not exceed 7 cm in length. Figure 2 illustrates the TMS380Cx6 to TMS380SRA interface.

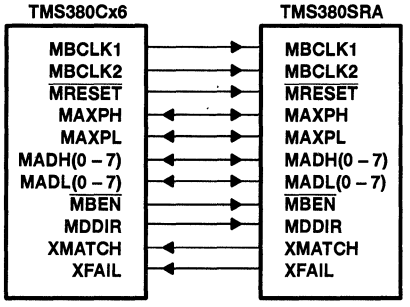


Figure 2. TMS380Cx6 to TMS380SRA Interface

bridging

Bridging is the process of passing information from one physical ring to another and is achieved by having a token-ring adapter attached to each ring but sharing a common attached-system processor. Each adapter monitors frames received on its ring for frames to be forwarded via its colleague to the other ring. When such a frame is detected, the transfer takes place via the attached-system processor. Each of these bridge adapters has a designator composed of its own ring number and its individual bridge number, and each also knows the ring number and bridge number of its colleague. This principle of the bridge is illustrated in Figure 3. Bridge #3 on ring 1 looks for frames to be forwarded to ring 2, and similarly bridge #3 on ring 2 looks for frames to forward to ring 1.

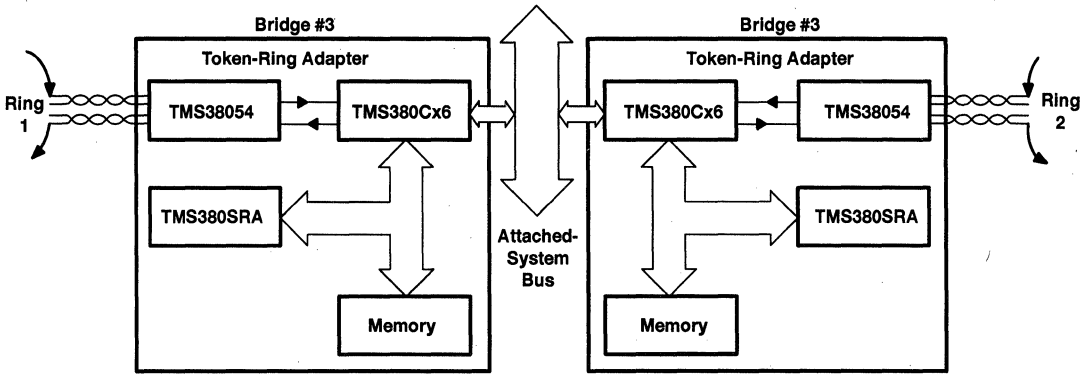


Figure 3. SRA Bridge

bridging (continued)

The TMS380SRA source-routing accelerator provides for high-speed frame copying and forwarding to the attached system. The SRA monitors incoming frames and asserts either XMATCH and XFAIL for each frame to indicate whether the frame should be bridged. Asserting XMATCH enables the TMS380Cx6 commprocessor to copy the frame, set the address recognize indicator (ARI) bits in the frame status (FS) byte, and set frame copied indicator (FCI) bits in the FS if the frame is copied. The attached system provides the appropriate frame building and forwarding services as well as the bridge-control functions described in the IBM token-ring network architecture reference.

The frame format containing the routing information is shown in Figure 4. The most significant bit of the source-address field is transmitted as a one, indicating that the frame contains routing information. If this bit is zero, the TMS380SRA does not copy the frame. The routing-information field immediately follows the source address and contains a 2-byte routing-control field and additional 2-byte route designators. The TMS380SRA supports up to fifteen route designators (see Note). The frame data, CRC field, end deliminator, and frame status follow the routing-information field.

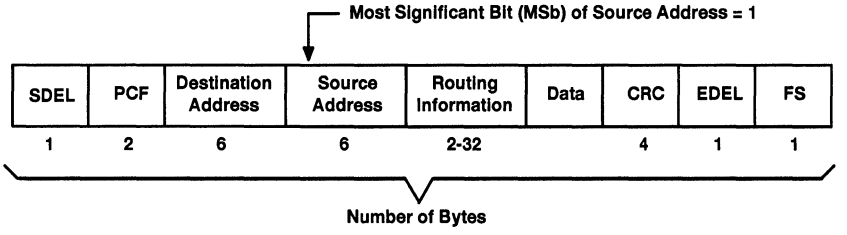


Figure 4. Frame Format Containing Routine Information

NOTE: IBM's current token-ring source-routing architecture supports only an 18-byte routing-information field. Texas Instruments Release 1.00, 2.00 and 2.10 second-generation adapter software will not transmit frames with routing-information fields longer than 18 bytes.

The routing-information field is expanded in Figure 5. If the frame is routed via a particular sequence of bridges (i.e., nonbroadcast), all the required route designators are provided by the token-ring node sourcing the frame. If the frame is a broadcast and meets requirements for forwarding (as determined by the routing-control field), the TMS380SRA copies the frame and the attached system adds the route designator of the next ring to the end of the routing-information field and transmits the frame through the colleague adapter.

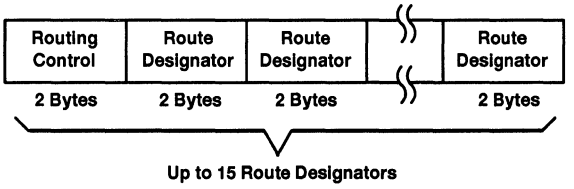


Figure 5. Routing-Information Field

bridging (continued)

The routing-control field contains two bytes of information as shown in Figure 6. Bits 0–2 indicate if the frame is a broadcast, and if so, what type. Bits 3–7 are the length field and indicate the length of the routing-information field, including the routing-control field. Bit 8 is a direction bit that, for nonbroadcast frames, indicates the order in which route designators should be interpreted by bridges routing the frame. Bits 9–11 are the largest frame-indicator bits, which can be modified by the attached system to indicate the maximum frame size that can travel via that bridge. The TMS380SRA ignores bit 2 in the broadcast-indicator field, bits 9–11 in the largest frame size field, and bits 12–15 in the reserved field.

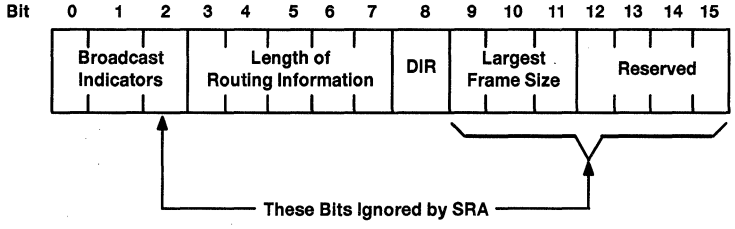


Figure 6. Routing-Control Field

Each ring in a multiple-ring network is assigned a unique ring number, and each bridge is assigned a bridge number, which may or may not be unique. Together the ring and bridge number form a route designator as shown in Figure 7. The two bytes of the route designator are divided into two parts. The least significant K-bits are the individual bridge number, and the most significant K-bits are the ring number. The individual bridge-number portion allows parallel bridges to exist to share traffic between two particular rings. The value of K is set using the PARTITION_LENGTH parameter of the SET.BRIDGE.PARMS command.

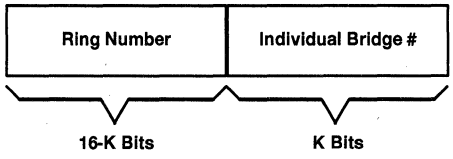


Figure 7. Route-Designator Field

frame-copying algorithm

Frame copying by the TMS380SRA is controlled by register-bit settings in the TMS380SRA and the incoming-frame routing-information field. If a frame is to be copied, the TMS380SRA asserts XMATCH, otherwise XFAIL is asserted. The TMS380SRA copies only frames with the source-routing-indicator bit set in the source address. The major parsing function is controlled by the broadcast bit settings of the incoming frame in the routing-control field [the broadcast indicator bits of the routing-control field (bits 0–2)]. The frame-copy algorithms are as follows:

0xx — Indicates that the routing-information field contains a specific route for the frame to travel through the network (nonbroadcast routing). For direction bit equal zero, the TMS380SRA examines the route designators for two adjacent designators containing its own adapter ring number and bridge number, and its colleague adapter's ring number. For direction bit equal one, the TMS380SRA examines the route designators for two adjacent designators containing its own adapter ring number, and its colleague adapter's ring number and bridge number. If these combinations are detected, the frame is copied. If no such match is found, the TMS380SRA does not enable frame coying. The TMS380SRA uses the direction bit to determine the required

order in which the routing information should be interpreted. This allows a frame to be returned to the sender without having to reorder the designators by changing the direction bit. If the direction bit is zero, the designators are read from left to right; if the direction bit is one, from right to left.

The TMS380SRA does not check that the same ring number appears more than once in the routing information. If rings 1, 2, and 3 are bridged together as a triangle, and a frame contains a sequence of designators 1, 2, 3, 1, it circulates indefinitely. Attached system software should check for this condition before forwarding the frame.

10x — Indicates that the frame is an all-routes broadcast. Every bridge forwards the frame to the next ring if it has not already circulated on that ring or has not already traversed the maximum number of bridges permitted by the protocol. (IBM token-ring network architecture reference limits this count to seven.) If the network is configured so that there are several routes to the destination adapter, then as many copies are received by that adapter as there are routes. The ring number in the final route designator of a broadcast should be the same as the ring number of the token-ring adapter bridge that receives it for forwarding. the TMS380SRA does not copy an all-routes broadcast frame with an incorrect final-route designator.

With broadcast frames, the value in the length field grows as the frame traverses the network. The first bridge to forward a frame adds 4 to the value and appends its designator (ring number and bridge number) and its colleague's ring number to the routing-information field, leaving its colleague's bridge number as all zeros. Subsequent bridges forwarding the frame add 2 to the value of the length field, add their bridge number into the all zeros bridge number part of the received final designator, and append their colleague's designator to the routing-information field, again leaving the colleague's bridge number portion as all zeros.

11x — Indicates that the frame is a single-route broadcast. Only bridges that are set up to transfer single-route broadcast frames consider the frame for forwarding. The TMS380SRA can be configured to copy single-route broadcast frames using the SET.BRIDGE.PARMS command. Frames are copied by the TMS380SRA under the same conditions as for all-route broadcasts. There is nothing inherent in the frame to limit its propagation to just one route. The network manager must select which bridges forward single-route broadcast frames and inform the bridges appropriately.

length-field requirements

The five length bits in the routing-control field indicate, in bytes, the length of the routing-information field. The minimum value is 2, which is how all bridge-broadcast frames originate, and the maximum value supported by the TMS380SRA is 30. All odd values, 0, 4, and values greater than 30 result in frames not being copied by the TMS380SRA. A value of 4 is illegal since this would mean there was only one route designator present. A value of 2 is not copied by the TMS380SRA for nonbroadcast frames.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 2) ..... −0.5 V to 7 V
Input voltage range ..... −0.5 V to 7 V
Output voltage range ..... −0.5 V to 7 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: Voltage values are with respect to GND.

recommended operating conditions

The TMS380SRA is designed to interface directly to the TMS380Cx6 token-ring commprocessor, Refer to the *TMS380 Second-Generation Token Ring User's Guide* (SPWS005) for details on TMS380Cx6 operation.

All inputs to the TMS380SRA have TTL compatible levels. All outputs are CMOS compatible; therefore, like-named pins on the TMS380SRA and TMS380Cx6 should be connected together.

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{CC}	Supply voltage, GND (see Note 3)		0	0	0	V
I_{OH}	High-level output current	Except XMATCH and XFAIL			8	mA
		XMATCH and XFAIL			2	
I_{OL}	Low-level output current (see Note 4)	Except XMATCH and XFAIL			−8	mA
		XMATCH and XFAIL			−2	
T_A	Operating free-air temperature		0		70	°C
C_L	Output load capacitance	MADH, MADL, MAXPH, MAXPL			50	pF
		XFAIL, XMATCH			20	

NOTES: 3. All GND pins should be routed to minimize inductance to system ground.
4. The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating conditions (unless otherwise noted)

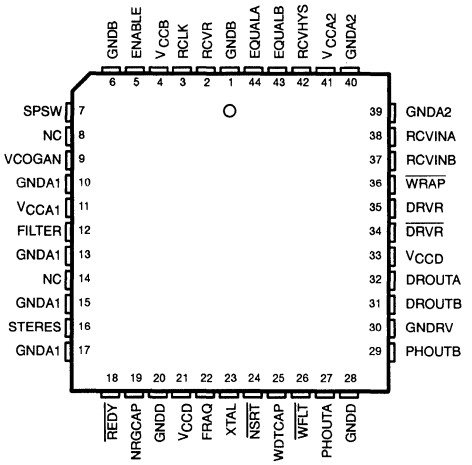
PARAMETER		TEST CONDITIONS (see Note 5)	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	V_{CC} = 5.5 V	2			V
V_{IL}	Low-level input voltage, TTL-level signal	V_{CC} = 4.5 V			0.8	V
V_{OH}	High-level output voltage, TTL-level signal	V_{CC} = MIN, I_{OL} = MAX	3.7			V
V_{OL}	Low-level output voltage, TTL-level signal	V_{CC} = MIN, I_{OL} = MAX			0.5	V
I_{CC}	Supply current	V_{CC} = MAX		60	160	mA
C_i	Input capacitance, any input				15	pF
C_o	Output capacitance, any output or input/output				15	pF

NOTE 5: For conditions shown as MIN or MAX, use the appropriate value specified under the recommended operating conditions.

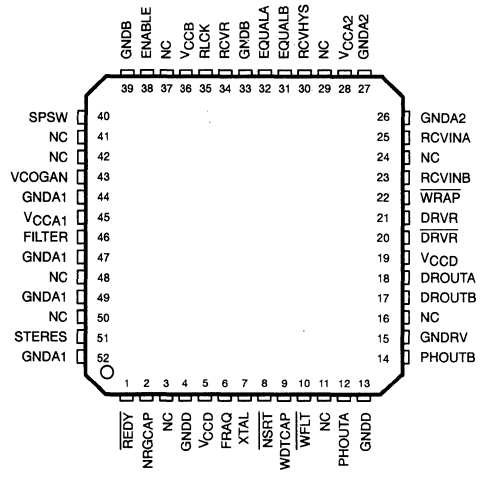
SPWS008B – APRIL 1991 – REVISED MAY 1994

- **Facilitates Connection of the TI380C25, TI380C27, or TMS380C26 to a Token-Ring Network™**
- **Compatible With Electrical Interface of ISO/IEC IEEE Std. 802.5:1992 Token-Ring Access Method and Physical Layer Specifications**
- **Constant-Gain Phase Detector for UTP Applications**
- **Phase-Locked Loop for Clock Generation and Data Signal Recovery**
- **Independent Transmit and Receive Channels**
- **Phantom Drive for Physical Insertion Onto Ring**
- **16- and 4-Mbps Token-Ring Data Rates**
- **Integrated Receiver Frequency Equalization**
- **Loop Back (Wrap Mode) for Self-Test Diagnostics**
- **On-Chip Watchdog Timer**
- **ESD Protection Exceeds 2 kV per MIL-STD-883C, Method 3015**
- **Advanced Low-Power Schottky Technology**
- **44-Lead Plastic Chip-Carrier Package (FN Suffix) or 52-Pin Thin Quad Flatpack (PAH Suffix)**

FN PACKAGE
(TOP VIEW)



PAH PACKAGE
(TOP VIEW)



description

The TMS38054 ring interface device with its associated external passive components form a full-duplex electrical interface to the token ring. Coupling the TMS38054 with one of the TMS380 family of commprocessors forms a highly integrated token-ring LAN adapter compatible with the ISO/IEC IEEE Std. 802.5: 1992 token-ring access method and physical layer specifications.

The TMS38054 operates at the IEEE-standard 16-Mbps and 4-Mbps data rates. The token-ring data stream is received by the TMS38054 and phase aligned using an on-chip phase-locked loop (PLL). Both the recovered clock and data are passed to the TI380C2x single-chip token-ring commprocessor's protocol-handling circuits for serial-to-parallel conversion and data processing. On transmit, the TMS380C2x provides a differential signal that the TMS38054 converts to analog levels for transmission on the media. A watchdog timer is also included to provide fail-safe deinsertion from the ring in the event of a station failure. The phase-detector gain is constant for all valid differential Manchester data that provide increased margin for unshielded twisted-pair applications.

Token-Ring Network is a trademark of International Business Machines Corp.

description (continued)

The TMS38054 is available in a 44-lead plastic chip-carrier package (FN suffix) and a 52-lead plastic quad flatpack (PAH suffix). The TMS38054 is characterized for operation from 0°C to 70°C with case temperature maintained at or below 99°C.

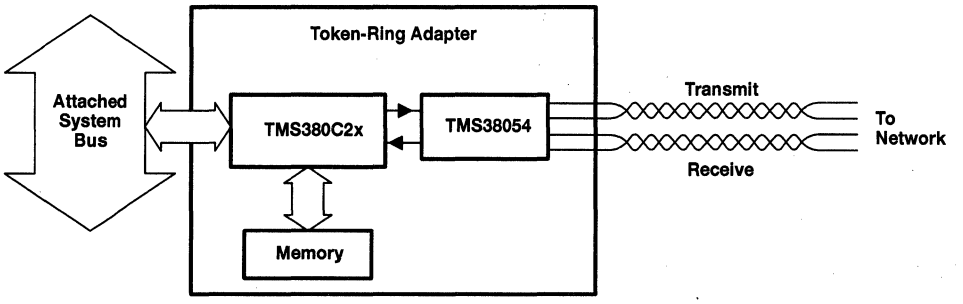


Figure 1. Token-Ring LAN Application Diagram

Pin Functions

PIN NAME	PIN NUMBER		I/O/E†	TYPE‡	DESCRIPTION
	PAH	FN			
DROUTA DROUTB	18 17	32 31	O O	D D	Driver outputs A and B. DROUTA and DROUTB are the differential driver outputs to the token ring via isolation transformers.
DRVR $\overline{\text{DRVR}}$	21 20	35 34	I I	D D	Differential driver data inputs. DRVR and $\overline{\text{DRVR}}$ are the differential inputs that receive the '380C2x transmit data.
ENABLE	38	5	I	T	Output-enable control. ENABLE is the TTL input used to enable a board-test mode. High = TMS38054 operates normally Low = All TTL outputs and phantom drive outputs are driven to the high-impedance state. DROUTA and DROUTB are not affected.
EQUALA EQUALB	32 31	44 43	E E	N N	Equalization/gain points A and B. EQUALA and EQUALB are connections that allow frequency tuning of the equalization circuit.
FILTER	46	12	E	N	Charge pump output/filter buffer input. FILTER allows connection of external components for the PLL filter.
FRAQ	6	22	I	T	Frequency acquisition control. FRAQ determines the use of frequency or phase-acquisition mode. High = Wide range. Frequency centering to XTAL reference. Low = Narrow range. Phase locked onto the incoming data (RCVINA and RCVINB).
GNDA1§¶	44, 47, 49, 52	10,13,1 5,17			Ground reference for VCO and filter input
GNDA2§¶	26, 27	39,40			Ground reference for receiver circuits
GNDB§¶	33, 39	1, 6			Ground reference for input and output buffers
GNDD§	4, 13	20, 28			Ground reference for digital circuits
GNDRV§	15	30			Ground reference for driver output circuits
NC§	3, 11, 16, 24, 29, 37, 41, 42, 48, 50	8, 14			Not internally connected
NRGCAP	2	19	E	N	Energy-detect capacitor. NRGCAP allows connection to an external capacitor for sensing received-data transitions (energy).
$\overline{\text{NSRT}}$	8	24	I	T	Phantom-driver control. $\overline{\text{NSRT}}$ enables PHOUTA and PHOUTB through the watchdog timer for insertion onto the token ring. Static high = Inactive, phantom current removed (due to watchdog timer) Static low = Inactive, phantom current removed (due to watchdog timer) Falling edge = Active, current output on PHOUTA and PHOUTB
PHOUTA PHOUTB	12 14	27 29	O O	N N	Phantom-driver outputs A and B. PHOUTA and PHOUTB cause insertion onto the token ring.
RCLK	35	3	O	T	Recovered clock. RCLK is the clock recovered from the token-ring received data. For 16-Mbps operation, RCLK is a 32-MHz clock. For 4-Mbps operation, RCLK is an 8-MHz clock.
RCVHYS	30	42	E	N	Receiver hysteresis resistor. RCVHYS allows setting of the receiver (hysteresis) threshold.
RCVINA RCVINB	25 23	38 37	I I	D D	Receiver inputs A and B. RCVINA and RCVINB receive the token-ring data via isolation transformers.
RCVR	34	2	O	T	Recovered data. RCVR contains the data recovered from the token ring.

† I = input, O = output, E = provides external component connection to the internal circuitry for tuning
‡ T = TTL signal, N = non-TTL signal, D = differential drive or data
§ These terminals should be connected to a single power or ground plane as appropriate.
¶ GNDA1, GNDA2, and GNDB are internally connected together.

Pin Functions (Continued)

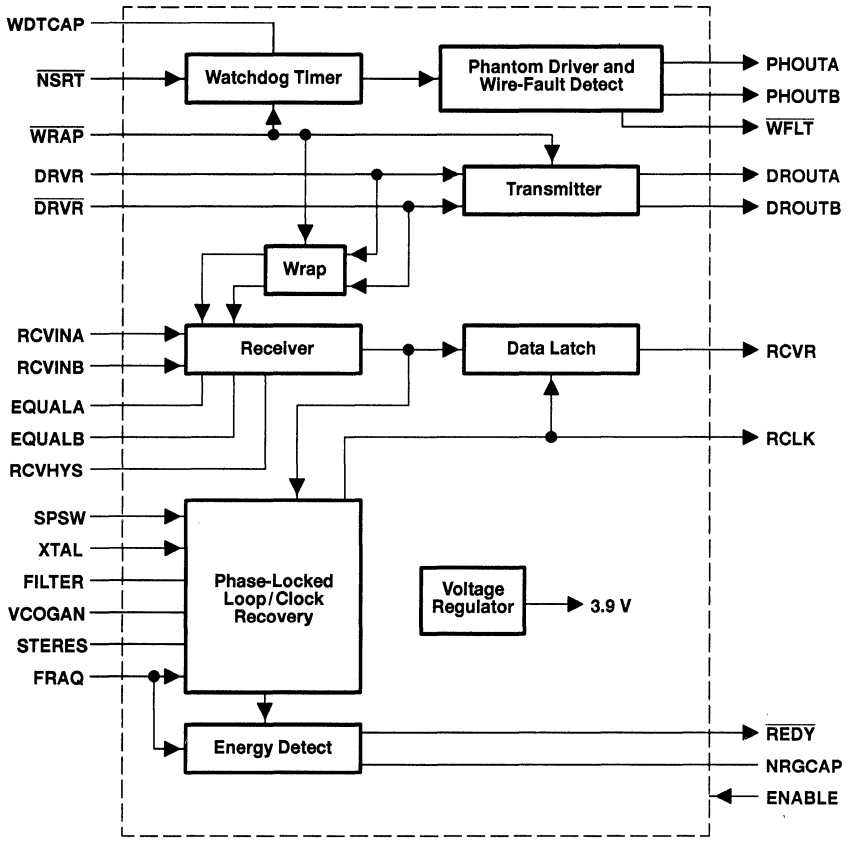
PIN NAME	PIN NUMBER		I/O/E†	TYPE‡	DESCRIPTION
	PAH	FN			
$\overline{\text{REDY}}$	1	18	O	T	Ready. $\overline{\text{REDY}}$ to the '380C2x provides an indication that sufficient time has elapsed since the last transition of FRAQ for the PLL to achieve lock as monitored by the energy-detect capacitor. High = Received data not valid Low = Received data valid
SPSW	40	7	I	T	Speed switch. SPSW specifies the token-ring data rate. High = 4-Mbps data rate Low = 16-Mbps data rate
STERES	51	16	E	N	Static timing error resistor. STERES allows connection to an external resistor for adjusting the static-timing error.
V_{CCA1}§	45	11			Positive supply voltage for VCO and filter input
V_{CCA2}§	28	41			Positive supply voltage for receiver circuits
V_{CCB}§	36	4			Positive supply voltage for input and output buffers
V_{CCD}§	5, 19	21, 33			Positive supply voltage for digital circuits (5 V)
VCOGAN	43	9	E	N	VCO gain resistor. VCOGAN allows connection to an external resistor for setting the VCO gain.
WDTCAP	9	25	E	N	Watchdog timer capacitor. WDTCAP allows connection to an external capacitor, which sets the watchdog-timeout period.
$\overline{\text{WFLT}}$	10	26	O	T	Phantom-wire-fault. $\overline{\text{WFLT}}$ provides an indication of the presence of a short circuit or open on PHOUTA or PHOUTB. High = No fault Low = Open or short
$\overline{\text{WRAP}}$	22	36	I	T	Internal-wrap mode control. $\overline{\text{WRAP}}$ allows the TMS38054 to be placed in the loopback-wrap mode for adapter self test. High = Normal ring operation Low = Transmit data drives the receive data.
XTAL	7	23	I	T	Crystal-oscillator input. XTAL (normally externally gated by FRAQ) is used to synchronize the PLL. XTAL is 32 MHz for 16-Mbps ring, and 8 MHz for 4-Mbps ring.

† I = input, O = output, E = provides external component connection to the internal circuitry for tuning
‡ T = TTL signal, N = non-TTL signal, D = differential drive or data
§ These terminals should be connected to a single power or ground plane as appropriate.

architecture

The major blocks of the TMS38054 include the receiver, data latch, transmitter, wrap, voltage regulator, energy detect, phase-locked loop, watchdog timer, and phantom driver and wire-fault detect (see functional block diagram). The functionality of each block is described in the following sections.

functional block diagram



receiver

The receiver circuit reads incoming data from the ring and performs five other functions:

- Provides dc bias for the differential input
- Provides clamping of large signal swings
- Provides gain and equalization
- Provides definition of thresholds
- Provides hysteresis for data detection

Gain as a function of frequency is set by the equalizer impedance. Equalization characteristics are determined by the external equalization circuit across EQUALA and EQUALB. Equalization is effective at low-signal amplitudes. At larger-signal levels, nonlinear effects reduce the effective equalization. The signal level where saturation occurs is determined by the impedance between EQUALA and EQUALB. The circuit is suitable for differential Manchester-encoded data at 16 or 4 Mbps.

data latch

The output of the receiver drives two internal circuits: the data latch and the phase detector. The latch samples the internal receiver output signal on the rising edge of the internal recovered clock. Data (RCVR) is therefore stable and can be sampled at the rising edge of RCLK. The timing of this edge is set by the phase detector and other loop components so that the received signal is sampled at the optimum time for error-free data recovery. Both the sampled data and the recovered clock signal are buffered and sent to the '380C2x token-ring commprocessor as the RCVR and RCLK signals to provide decoding of the differential Manchester data.

Static-timing error is defined as the amount of error that the rising edge of the recovered clock has from the midpoint of the data signal into the data latch. An error of zero is optimum sampling, as this places the rising edge of the sampling clock in the middle of the data pulse. A positive offset represents early sampling.

transmitter

The transmit driver provides differential current drive at a suitable level for driving the data onto the ring. Both outputs (DROUTA and DROUTB) are open collector and intended to drive a center-tapped transformer with the center tap connected to V_{CC}. The output stage controls a fixed current between the two outputs under the control of the driver data input (DRVR and $\overline{\text{DRVR}}$).

DRVR and $\overline{\text{DRVR}}$ drive a differential transmit circuit that enhances the symmetry of the current switching on DROUTA and DROUTB. The DRVR and $\overline{\text{DRVR}}$ inputs are not retimed within the TMS38054. Consequently, low skew in the input is important in order to avoid degrading the transmitted output waveform. The transmitter-drive outputs are not affected by ENABLE. When DRVR is high and $\overline{\text{DRVR}}$ is low, the output current is directed to DROUTA and, when reversed, to DROUTB.

wrap

The wrap function provides an internal signal path used for system self-test diagnostics. When the internal-wrap mode-control input ($\overline{\text{WRAP}}$) is taken low, the transmitter outputs are disabled and the receiver inputs are ignored. An alternate path is provided from the transmitter output circuitry to the receiver input circuitry through the wrap circuit. This wrap path to RCVR inverts the transmitted signal. In the internal-wrap mode, attenuation is checked by observing the signal amplitude at EQUALA and EQUALB. Equalization is active at this signal level although the signal does not exhibit the high-frequency attenuation effects for which equalization is intended to compensate.

phantom driver and wire-fault detector

The phantom-drive circuit under control of $\overline{\text{NSRT}}$ generates a dc signal on both of the two drive outputs, PHOUTA and PHOUTB. To maintain the dc signal, $\overline{\text{NSRT}}$ must provide a positive (low-to-high) clock edge once every 20 ms. An internal watchdog timer (oneshot) is designed so that the PHOUTA and PHOUTB dc signals are removed if $\overline{\text{NSRT}}$ fails to have the required transitions. The PHOUTA and PHOUTB signals are sent over the transmit-signal pair to the trunk-coupling unit (TCU) to request that the station be inserted into the ring. The signal current is detected by the TCU, causing the external-wrap path from the transmitter outputs back to the receiver inputs to be broken. A connection is established from the ring to the receiver inputs and from the transmitter outputs to the ring. The phantom-drive outputs are short-circuit protected; they detect a short circuit from either output to ground or when there is an abnormally low load current at either output corresponding to an open circuit in the signal or TCU wiring. Either type of fault results in $\overline{\text{WFLT}}$ being driven low. The logic state of $\overline{\text{WFLT}}$ is high when $\overline{\text{NSRT}}$ is high. All three outputs, PHOUTA, PHOUTB, and $\overline{\text{WFLT}}$, are in the high-impedance state when ENABLE is low.

watchdog timer

The watchdog timer provides protection against a failed adapter remaining on the ring. $\overline{\text{NSRT}}$ must be toggled low or the watchdog timer will turn off the phantom drive. The period of the watchdog timer is determined by the value of the external capacitor connected to WDTCAP. The capacitor is chosen to give a period of 21 ms minimum and 50 ms maximum. This assures compatibility with a system that toggles $\overline{\text{NSRT}}$ at a rate faster than once every 20 ms and assures deinsertion from the ring within 50 ms of the last $\overline{\text{NSRT}}$ high-to-low transition.

watchdog timer (continued)

The duty cycle of $\overline{\text{NSRT}}$ is not critical. Phantom drive is turned on following a falling $\overline{\text{NSRT}}$ edge. Deinsertion occurs if $\overline{\text{NSRT}}$ is left high or low or if the internal-wrap mode is selected from $\overline{\text{WRAP}}$. The following describes the operation of the watchdog timer and indicates the priorities of the control signals:

- $\overline{\text{WRAP}}$ is low (internal mode selected):
  - Phantom drive is off. Operation of the watchdog timer is not defined but can continue, and if the timer has not expired, taking $\overline{\text{WRAP}}$ high can result in the phantom drive being turned on.
- $\overline{\text{WRAP}}$ is high:
  - If the timing capacitor is connected and $\overline{\text{NSRT}}$ goes from high to low, the timing capacitor is charged or recharged to a defined level. Phantom drive is on and discharging of the timing capacitor continues.
  - If the timing capacitor is connected and $\overline{\text{NSRT}}$ goes from low to high, there is no effect on the watchdog timer and the discharging of the timing capacitor continues.
  - If the timing capacitor is connected and the capacitor discharges to a defined level, the phantom drive is turned off regardless of the state of $\overline{\text{WRAP}}$.
  - If the timing capacitor is not connected and the timing capacitor pin is held to V_{CC} + 0.5 V, the phantom drive is controlled directly by $\overline{\text{NSRT}}$. This serves to disable the watchdog-timer function.

voltage regulator

The internal voltage regulator is used to make the performance of the TMS38054 less dependent on the supply voltage. The regulator consists of a band-gap reference scaled up to a nominal 3.9 V with a temperature coefficient designed to compensate for coefficients in circuits referenced to the voltage regulator.

phase-locked loop/clock recovery

The TMS38054 contains a phase-locked loop (PLL) for recovering a data clock from the received bit stream. The elements of PLL are: phase and frequency detectors, a charge pump, an external filter (connected to FILTER), a filter buffer, a voltage-to-current converter, and a voltage-controlled oscillator. There are three pins on the TMS38054 that allow connection to external components and tuning of the characteristics of the phase-locked loop. These pins are FILTER, STERES, and VCOGAN. Figure 2 illustrates these blocks. The following paragraphs describe the PLL elements.

phase-locked loop/clock recovery (continued)

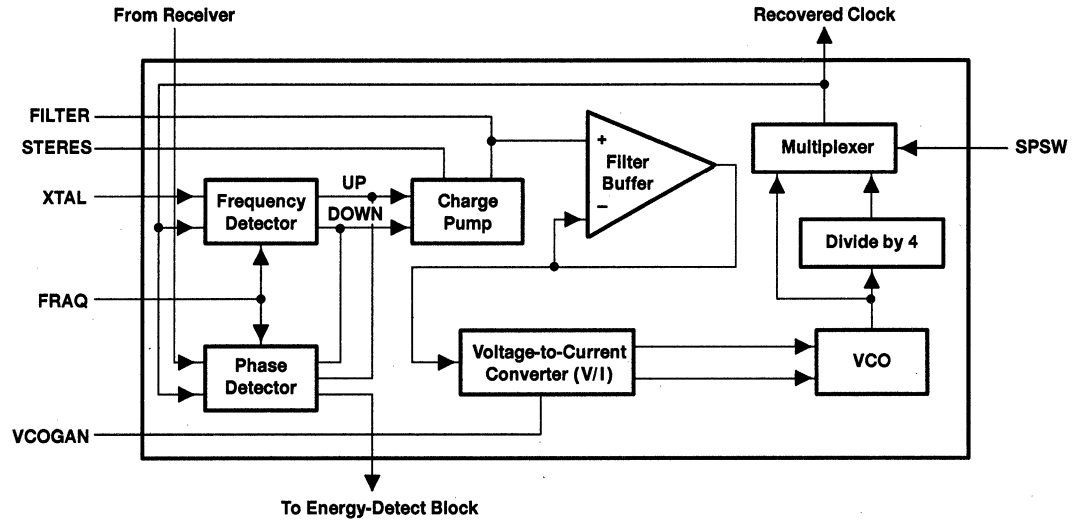


Figure 2. Phase-Locked-Loop Block Diagram

phase and frequency detectors

The phase- and frequency-detector blocks generate control signals suitable for controlling the charge pump. The frequency detector is used to bring the frequency of the voltage-controlled oscillator (VCO) close to the frequency of XTAL. The phase detector is used to provide precise phase alignment of the recovered clock to the incoming data. The circuit is not capable of locking the PLL in cases where the VCO frequency and incoming data frequency differ substantially, hence, the need for frequency centering before phase alignment to incoming data occurs.

The phase detector compares the phase of the received data and the recovered clock, and accordingly generates the charge pump control signals, UP and DOWN. The width of the UP pulse is determined by the phase alignment of the received data and the recovered clock. Each UP pulse is followed by a DOWN pulse of constant width. Phase-detector UP-DOWN sequences are initiated at a 16-MHz rate for all valid differential Manchester data patterns. This rate can drop momentarily during code violations or delimiters, but such deviations are of short duration and the gain of the phase detector can be considered constant.

A multiplexer selects the required detection mode during insertion onto the ring. The frequency-detection mode is selected by taking FRAQ high and the phase-detection mode is selected by taking FRAQ low. The phase or frequency detectors supply the necessary charge (or UP) and discharge (or DOWN) control signals to the charge pump.

charge pump

The charge pump supplies charge to and removes charge from the external filter components.The output of either the phase detector or frequency detector drives the charge pump as selected by FRAQ. The charge pump has two internal inputs, so there are four possible states of the charge pump:

- Pump UP – current into the filter, increasing the voltage
- Pump DOWN – current out of the filter, reducing the voltage
- No pump – in the high-impedance state, holding the voltage on the filter
- Pump UP and pump DOWN – both currents on (not allowed by the detector logic)

The pump UP and pump DOWN currents are approximately equal; the net charge supplied by the charge pump in a given time depends primarily on the relative duration and frequency of UP and DOWN controls from the phase and frequency detectors. If the net current output is positive, the voltage at FILTER rises causing an increase in the VCO clock frequency. If the net output is negative, the FILTER voltage falls slowing the VCO clock.

The charge-pump block has two constant-current circuits operating continuously, one for pump UP and one for pump DOWN. They are designed for stability under all operating conditions. The UP current is fixed and directly affects the magnitude of the loop gain and the bandwidth and damping factor of the loop. Any difference between the UP and DOWN currents creates an offset in the loop, which introduces a static-timing error. Provision for an external resistor at STERES is included to allow slight variation in the DOWN current and allows the static-timing error of the loop to be adjusted to compensate for error introduced by the charge pump and other elements of the PLL. This resistor is not required for normal operation of the TMS38054, but provisions should be made to accommodate this resistor in possible future applications.

external filter

The external filter consists of passive external components connected from FILTER to ground. A system diagram for the PLL circuit is shown in Figure 3. The phase-detector/charge-pump gain, G_d, is given in the electrical specifications as 16 Mbps. This value is true for any valid differential Manchester data pattern. The result is in μA/ns, which can be converted to A/rad by using the equation on the following page. The value, in A/rad, is the same at both 16 Mbps and 4 Mbps.

The VCO gain, G_O, is given in the electrical specifications at 16 Mbps. This value is in MHz/V, which can be converted to rad/volt by using the equation on the following page. The value at 4 Mbps is one-fourth this value because of the ×4 divider on the VCO output at 4 Mbps.

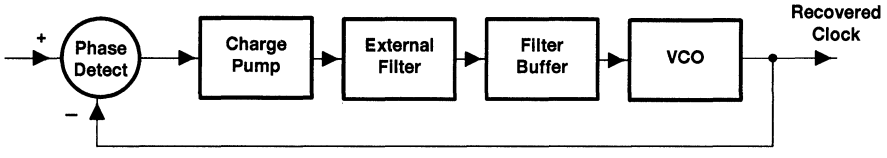


Figure 3. Analytical PLL Diagram

external filter (continued)

A typical external filter circuit is shown in Figure 4. Capacitor C5 limits the filter-buffer ripple but should be chosen to be as small as possible to reduce PLL overshoot. The resistor (R5) sets the effective bandwidth of the PLL closed loop, and capacitor C4 sets the damping factor. The filter buffer is an amplifier with bandwidth of 3–5 MHz.

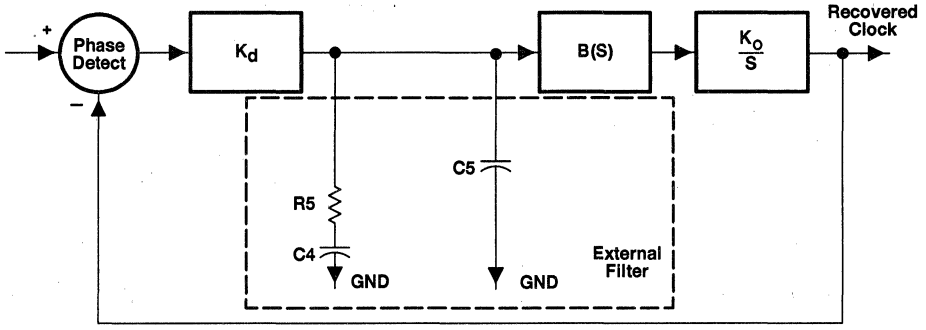


Figure 4. Analytical PLL Model

The simplified equations for the PLL are:

VCO gain	$K_o = (G_o)\ (10^6)\ (2\pi)\ (F)$	rad/(s • V)
Phase-detector gain	$K_d = \frac{(G_d)\ (10^3)\ (31.25)\ (10^{-9})}{2\pi}$	A/rad
PLL-noise-equivalent bandwidth	$B_L = \frac{(K_o)\ (K_d)\ (\text{R5 in ohms})}{4}$	Hz

G_o = the VCO gain measured in MHz/V

G_d = phase-detector gain measured in μA/ns

F = the frequency divider factor; i.e., F = 1 for 16-Mbps operation
F = 0.25 for 4-Mbps operation

These equations are only a guide and the actual bandwidth and PLL-damping characteristics should be obtained through correlation and modeling on specific hardware implementations that take into effect all circuit card parasitics. Both 16-Mbps and 4-Mbps ring operation can be achieved by suitable selection of glue components at each frequency. More information on PLL characteristics are found in:

- Gardner, Floyd, *Phase Lock Techniques*, John Wiley & Sons, 1979.
- *Token Ring Access Method and Physical Layer Specification*, ANSI/IEEE/ISO/IEC Standard 802.5:1992.
- Gardner, Floyd, "Charge-Pump Phase-Locked Loops", *IEEE Transaction Communications*, Vol. COM–28, pp. 1849 – 1858, Nov. 1980.

filter buffer and voltage-to-current converter (V/I)

The filter-buffer amplifier is a unity-gain amplifier used to buffer the voltage present at FILTER with minimal leakage current. The output of the filter buffer drives a voltage-current (V/I) converter that produces equal currents, proportional to the filter voltage, for use in the voltage-controlled oscillator (VCO). The current level or constant of proportionality is set by the external resistor connected to ground connected at VCOGAN. This resistor sets the VCO gain, which is critical to loop gain and damping. The filter voltage range over which the current level tracks the voltage determines the pull-in range of the VCO.

voltage-controlled oscillator (VCO)

The voltage-controlled oscillator (VCO) is an emitter-coupled astable multivibrator. The frequency is set by internal circuit parameters, the currents from the filter buffer, and an internal VCO timing capacitor. Symmetrical circuit design helps ensure symmetry of the VCO output, which has a nominal frequency of 32 MHz. The VCO output is buffered and sent to the divider (for 4-Mbps operation) and multiplexer circuit.

divider and multiplexer

The multiplexer selects the source of the recovered clock, which can be either the direct output of the VCO (nominally a 32-MHz signal) or the divided version of the VCO output (nominally an 8-MHz signal) for 16- or 4-Mbps operation. The output clock of the VCO is fed to a divide-by-4 circuit and to a multiplexer. The divider is enabled when SPSW is high. The recovered clock is passed to frequency and phase detectors, the clock of the data latch, and is buffered at RCLK and passed on to the '380C2x commprocessor for processing of the received data.

energy detect

The energy-detect circuit provides a timing delay on $\overline{\text{REDY}}$. When FRAQ changes state, it indicates to the energy-detect circuit that a change of lock mode has occurred and that time must be allowed before data recovered by the TMS38054 can be considered valid. The energy-detect-timing capacitor is discharged shortly after a low or high going transition of FRAQ, which results in the $\overline{\text{REDY}}$ signal being deasserted.

The time taken for the TMS38054 to acquire phase lock depends on the transition density of the incoming data, so the delay of the energy-detect circuit also changes. Each rising transition of data results in a current pulse of fixed duration being injected into the energy-detect-timing capacitor. The charge time of the capacitor is dependent on incoming-data-transition density and $\overline{\text{REDY}}$ is reasserted after the capacitor reaches an internally set threshold voltage.

A small discharge current is always present on the energy-detect-timing capacitor. When the incoming-data-transition density falls below a certain threshold, the current pulses may not be sufficient to overcome this discharge current and $\overline{\text{REDY}}$ may not be asserted.

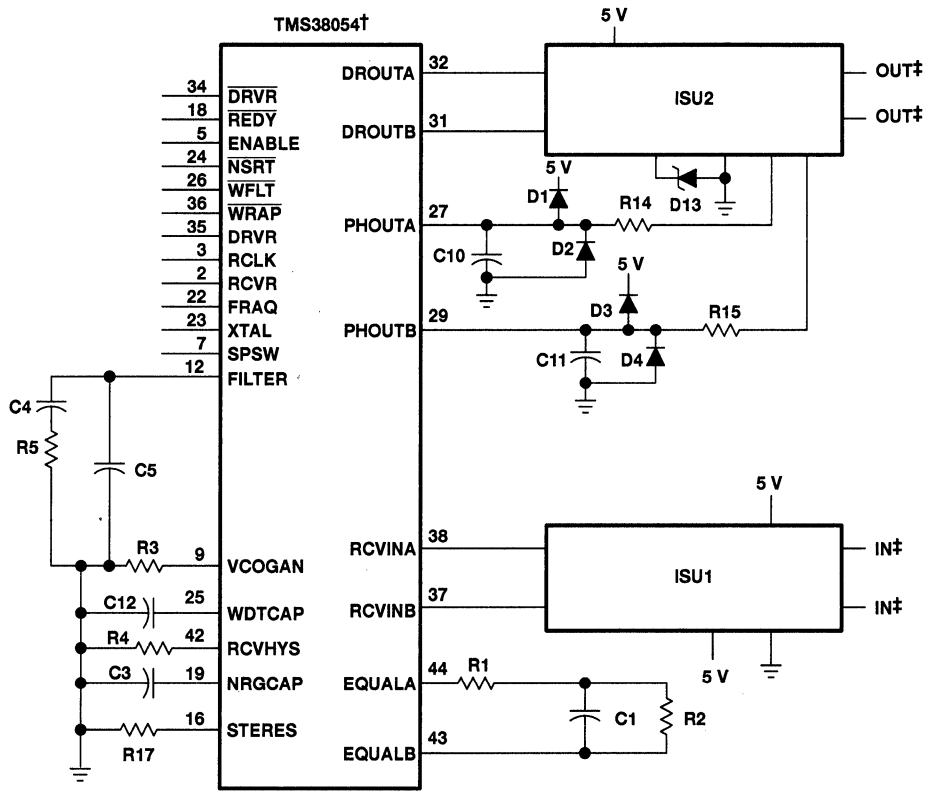
test mode

The TMS38054 features a test mode for board-level testing with the components in the circuits. This facilitates testing by bed-of-nails testers. This test mode is enabled by pulling ENABLE to a low level. DROUTA and DROUTB are not affected by this function. When ENABLE is high, the TMS38054 operates normally. When ENABLE is low, the circuit continues to operate except that PHOUTA, PHOUTB, RCVR, $\overline{\text{WFLT}}$, and RCLK are driven to the high-impedance state and $\overline{\text{REDY}}$ is driven high.

external passive circuitry

Figure 5 shows an arrangement of external components for a typical 16-Mbps or 4-Mbps token-ring interface. The selection of component values is dependent on the objective of the design. The design needs to take into account the importance of layout and component selection (values and tolerances).

The ISU1 and ISU2 blocks represent transformers that couple data from the TMS38054 to the ring. They also represent protection circuitry against large voltage excursions. Information on ISU1 and ISU2 connections can be found in the *TMS38054 Second-Generation Ring Interface Design Note* (revision C). To obtain this design note, contact the TMS380 Technical Support Line at TI380HOT@micro.ti.com.



† Pin numbers shown are for the FN package.
‡ Refer to the *TMS38054 Second-Generation Ring Interface Design Note* (revision C) for further information.

Figure 5. Typical Token-Ring Interface Circuit for 16 Mbps or 4 Mbps

Table 1. Typical Components for Figure 5

SYMBOL(S)	FUNCTION
C1	Equalizer capacitor
C3	Energy-detect capacitor
C4	PLL-filter capacitor
C5	PLL-filter capacitor
C10, C11	Phantom-drive isolation capacitor
C12	Watchdog-timer capacitor
D1-D4	Phantom surge-suppression diodes
D13	Driver surge-suppression zener diode
R1	Equalizer resistor
R2	Equalizer resistor
R3	VCO gain resistor
R4	Receiver-hysteresis resistor
R5	PLL-filter resistor
R14, R15	Phantom-drive resistor
R17	Static-timing-error resistor
ISU 1	Isolation/shaping unit (see previous page)
ISU 2	Isolation/shaping unit (see previous page)

absolute maximum ratings†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... – 0.5 V to 7 V
Output voltage range: Driver outputs ..... – 0.5 V to 8 V
All other outputs (see Note 2) ..... – 0.5 V to 7 V
Power dissipation (see Note 3) ..... 1.25 W
Storage temperature range ..... – 10°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Inputs may be taken to more negative voltages if the current is limited to 20 mA.
2. These outputs may not be taken more than 0.5 V above the V_{CC} pins.
3. Maximum power dissipation per package

recommended operating conditions‡

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	$\overline{WRAP}$, ENABLE, FRAQ, XTAL, $\overline{NSRT}$, SPSW	2			V
V_{IL}	Low-level input voltage	$\overline{WRAP}$, ENABLE, FRAQ, XTAL, $\overline{NSRT}$, SPSW			0.7	V
	Receiver input bias voltage (see Note 4)		V_{SB} – 1		V_{SB} + 1	V
I_{OH}	High-level output current	RCVR, RCLK, $\overline{WFLT}$, $\overline{REDY}$			– 0.1	mA
I_{OL}	Low-level output current	$\overline{REDY}$, RCVR, $\overline{WFLT}$, RCLK			1	mA
T_C	Operating case temperature		0		99	°C

‡ Recommended operating conditions indicate the conditions that must be met to ensure that the device will function as intended and meet the detailed electrical specifications. Unless otherwise noted, all electrical specifications apply for all recommended operating conditions. Voltages are measured with respect to the device ground pins. Currents into the device are considered to be positive.

NOTE 4: V_{SB} is the self-bias voltage of the input pair RCVINA and RCVINB. It is defined as $V_{SB} = (V_{SBA} + V_{SBB})/2$ (where V_{SBA} is the self-bias voltage of RCVINA; V_{SBB} is the self-bias voltage of RCVINB). The self-bias voltage of both pins will be approximately $V_{CC}/2$.

electrical characteristics over recommended range of supply voltage (unless otherwise noted)

TTL input

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
I_{IH}	High-level input current	$\overline{WRAP}$, ENABLE, FRAQ, XTAL, $\overline{NSRT}$, SPSW	V_I = 2.7 V		20	µA
I_{IL}	Low-level input current	$\overline{WRAP}$, ENABLE, FRAQ, XTAL, $\overline{NSRT}$, SPSW	V_I = 0.4 V		– 0.4	mA
I_I	Input current at maximum input voltage	$\overline{WRAP}$, ENABLE, FRAQ, XTAL, $\overline{NSRT}$, SPSW	V_I = 7 V		100	µA
V_{IK}	Input clamp voltage	$\overline{WRAP}$, ENABLE, FRAQ, XTAL, $\overline{NSRT}$, SPSW, DRVR, $\overline{DRVR}$	I_I = – 12 mA		– 1.5	V

TTL output (RCVR, RCLK, $\overline{REDY}$, and $\overline{WFLT}$)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 0.1 mA	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA		0.45	V
I_{OZH}	Off-state output current with high-level voltage applied	V_O = 2.7 V		± 100	µA
I_{OZL}	Off-state output current with low-level voltage applied	V_O = 0.4 V		± 100	µA

electrical characteristics over recommended range of supply voltage (unless otherwise noted) (continued)

receiver input (RCVINA and RCVINB)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Rising input threshold voltage, V_{T+}	$V_{IC} = V_{SB}$, R4 = 2.49 kΩ, R_{tst} = 330 Ω, See Notes 4, 5, and 6		35	mV
Falling input threshold voltage, V_{T-}	$V_{IC} = V_{SB}$, R4 = 2.49 kΩ, R_{tst} = 330 Ω, See Notes 4, 5, and 6	– 35†		mV
Asymmetry threshold voltage, (V_{T+} + V_{T-})	$V_{IC} = V_{SB}$, R4 = 2.49 kΩ, R_{tst} = 330 Ω, See Notes 4, 5, and 6	– 20†	20	mV
Rising input common-mode rejection [V_{T+} (@V_{SB} + 0.5 V) – V_{T+} (@V_{SB} – 0.5 V)]	R_{tst} = 330 Ω, R4 = 2.49 kΩ, See Notes 4, 5, and 6	– 30†	30	mV
Falling input common-mode rejection [V_{T+} (@V_{SB} + 0.5 V) – V_{T+} (@V_{SB} – 0.5 V)]	R_{tst} = 330, R4 = 2.49 kΩ, See Notes 4, 5, and 6	– 30†	30	mV
Receiver input current	R_{tst} = 330 Ω, Both inputs at V_{SB} See Note 4		± 25	µA
	R_{tst} = 330 Ω, Input under test at V_{SB} + 1.0 V, Other input at V_{SB} – 1 V, See Note 4	300	700	µA
	R_{tst} = 330 Ω, Input under test at V_{SB} – 1.0 V, Other input at V_{SB} + 1.V, See Note 4	–300	–700	µA
Equalizer bias current (EQUALA and EQUALB)	RCVINA and RCVINB open, EQUALA and EQUALB at 3 V	1.125	1.875	mA

† The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used in this data sheet for threshold voltages only.

NOTES: 4. V_{SB} is the self-bias voltage of the input pair RCVINA and RCVINB. It is defined as $V_{SB} = (V_{SBA} + V_{SBB})/2$ (where V_{SBA} is the self-bias voltage of RCVINA; V_{SBB} is the self-bias voltage of RCVINB). The self-bias voltage of both pins will be approximately $V_{CC}/2$.
5. R_{tst} is a resistor connected between pins 43 and 44; it replaces R1, R2, and C1 (see Figure 5).
6. V_{IC} is the common-mode voltage applied to RCVINA and RCVINB.

transmitter

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
	Output current, on	DROUTA, DROUTB	$V_O = V_{CC}$, See Note 7	20	35	mA
	Output current, off	DROUTA, DROUTB	V_O = 8 V, See Note 7		100	µA
	Output current, off	DROUTA, DROUTB	$\overline{WRAP} = V_{IL}$, V_O = 8 V		100	µA
I_{IH}	High-level input current	DRVR, $\overline{DRVR}$	Input under test at 2.7 V, Other input at 0.4 V	100	700	µA
I_{IL}	Low-level input current	DRVR, $\overline{DRVR}$	Input under test at 0.4 V, Other input at 2.7 V	–100	–700	µA

NOTE 7: Output not under test is loaded with 75 Ω to V_{CC}.

phantom driver (PHOUTA and PHOUTB)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 1 mA	4.1		V
		I_{OH} = – 2 mA	3.8		V
I_{OS}	Short circuit output current	V_O = 0 V, $\overline{NSRT} = V_{IL}$	– 4	– 20	mA
I_{OH}	High-level output current	$V_O = V_{CC}$, $\overline{NSRT} = V_{IH}$		± 100	µA
I_{OZH}	Off-state output current with high-level voltage applied	$V_O = V_{CC}$, ENABLE = V_{IL}		± 100	µA
I_{OZL}	Off-state output current with low-level voltage applied	V_O = 0 V, ENABLE = V_{IL}		± 100	µA

electrical characteristics over recommended range of supply voltage (unless otherwise noted) (continued)

wire fault ($\overline{\text{WFLT}}$) (see Notes 8 and 9)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Phantom-normal condition	2.9 kΩ < R_{L1} < 5.5 kΩ, 2.9 kΩ < R_{L2} < 5.5 kΩ	2.4		V
Phantom-open condition	R_{L1} > 9.9 kΩ and 2.9 kΩ > R_{L2} < 5.5 kΩ or R_{L2} > 9.9 kΩ and 2.9 kΩ < R_{L1} < 5.5 kΩ		0.45	V
Phantom-short condition	R_{L1} < 0.1 kΩ and 2.9 kΩ < R_{L2} < 5.5 kΩ or R_{L2} < 0.1 kΩ and 2.9 kΩ < R_{L1} < 5.5 kΩ		0.45	V

NOTES: 8. The wire-fault logic recognizes a load condition corresponding to greater than 9.9 kΩ to ground as an open-circuit fault, but it does not recognize a load condition less than 5.5 kΩ to ground as an open. The wire-fault logic recognizes a load condition corresponding to less than 100 Ω to ground as a short-circuit fault, but it does not recognize a load condition corresponding to greater than 2.9 kΩ to ground as a short. Figure 6 illustrates this with R_{L1} connected from PHOUTA to ground and R_{L2} connected from PHOUTB to ground.

9. R_{L1} is connected from PHOUTA to ground; R_{L2} is connected from PHOUTB to ground.

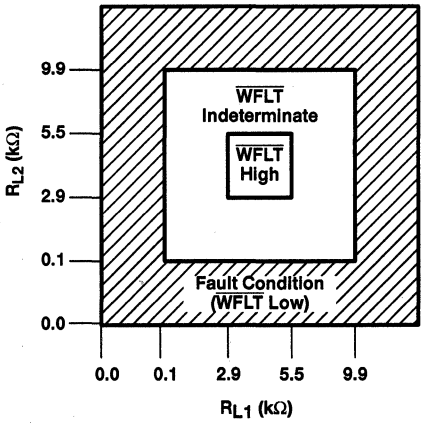


Figure 6. $\overline{\text{WFLT}}$

supply current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5.25 V, See Figure 7		180	200	mA

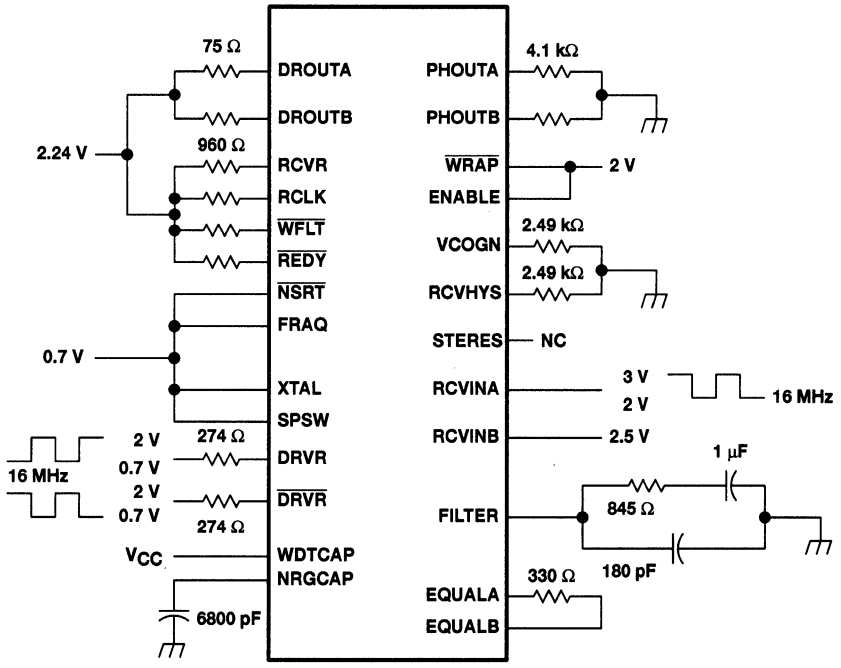


Figure 7. I_{CC} Test Circuit

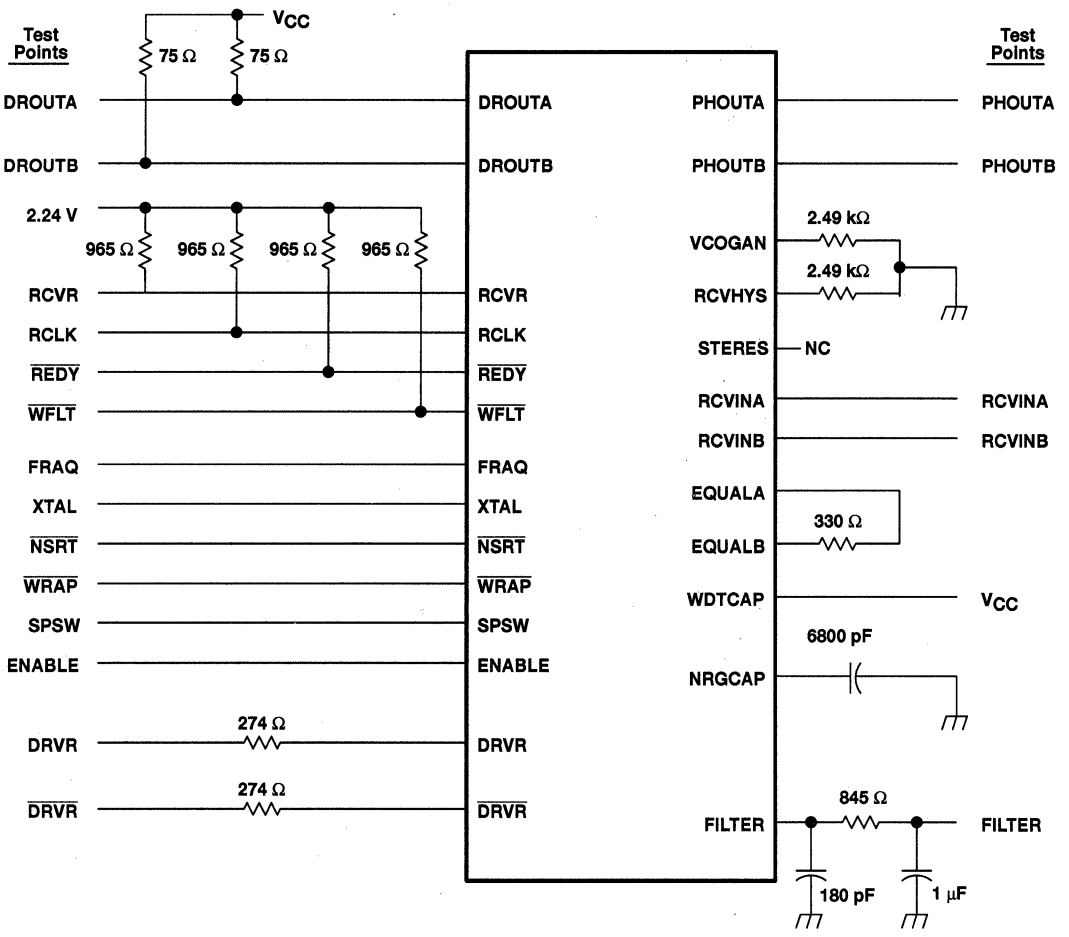


Figure 8. AC Test Circuit

timing requirements over recommended range of supply voltage (unless otherwise noted)

transmitter (see Figures 8 and 9)

NO.			TEST CONDITIONS	MIN	TYP	MAX	UNIT
1	$t_{sk(DRVR)}$	Delay time, DRVR edge (1.5 V) to following $\overline{DRVR}$ edge (1.5 V)		See Note 10			
2	$t_{d(DROUTA)H}$	Delay time, DRVR falling edge (1.5 V) to DROUTA rising edge (midpoint)		See Note 10			
3	$t_{d(DROUTA)L}$	Delay time, DRVR rising edge (1.5 V) to DROUTA falling edge (midpoint)		See Note 10			
4	$t_{d(DROUTB)L}$	Delay time, DRVR falling edge (1.5V) to DROUTB falling edge (midpoint)		See Note 10			
5	$t_{d(DROUTB)H}$	Delay time, DRVR rising edge (1.5 V) to DROUTB rising edge (midpoint)		See Note 10			
6	DROUTA/DROUTB skew	$t_{d(DROUTA)H} - t_{d(DROUTB)L}$	$t_{sk(DRVR)} = -1$ ns			±3	ns
		$t_{d(DROUTA)L} - t_{d(DROUTB)H}$	$t_{sk(DRVR)} = 1$ ns			±3	
7	DROUTA/DROUTB asymmetry	$\frac{t_{d(DROUTA)L} + t_{d(DROUTB)H}}{2} - \frac{t_{d(DROUTA)H} + t_{d(DROUTB)L}}{2}$	$t_{sk(DRVR)} = -1$ ns			±2	ns
			$t_{sk(DRVR)} = 1$ ns			±2	

NOTE 10: This parameter is not tested to a minimum or a maximum but is measured and used as a component required for parameters 6 and 7.

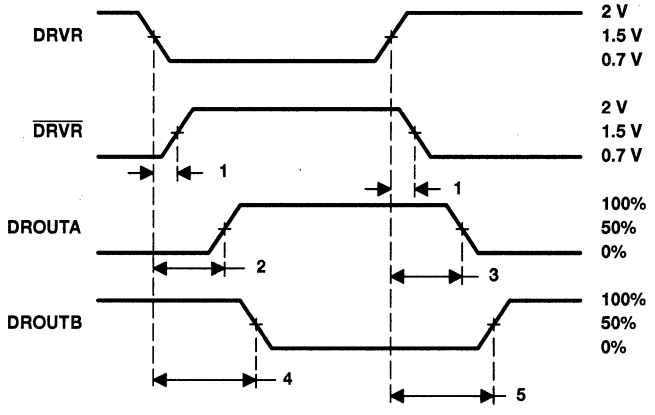


Figure 9. Skew and Asymmetry From DRVR and $\overline{DRVR}$ to DROUTA and DROUTB

timing requirements over recommended range of supply voltage (unless otherwise noted) (continued)

RCLK and RCVR (see Figures 8 and 10)

NO.			TEST CONDITIONS	MIN	TYP	MAX	UNIT
8	$t_{w(RCLK)L}$	Pulse duration, RCLK low	4 Mbps, $t_{c(RCLK)}$ = 115 ns, See Note 11	46			ns
			16 Mbps, $t_{c(RCLK)}$ = 30 ns, See Note 11	10			
9	$t_{w(RCLK)H}$	Pulse duration, RCLK high	4 Mbps, $t_{c(RCLK)}$ = 115 ns, See Note 11	35			ns
			16 Mbps, $t_{c(RCLK)}$ = 30 ns, See Note 11	8			
10	$t_{su(RCVR)}$	Setup time, RCVR valid to RCLK rising edge (1.5-V point)	$t_{c(RCLK)}$ = 31.25 ns	10			ns
11	$t_{h(RCVR)}$	Hold time, RCVR valid after RCLK rising edge (1.5-V point)	$t_{c(RCLK)}$ = 31.25 ns	2			ns
12	$t_{c(RCLK)}$	Cycle time, RCLK (see Note 12)	4 Mbps		125		ns
			16 Mbps		31.25		

NOTES: 11. The pulse duration high and low of RCLK is tested at a frequency in excess of nominal to ensure correct operation during brief periods where lock is lost.
12. This parameter is not tested. The typical value shown is that for the recovered clock from an IEEE 802.5 token ring.

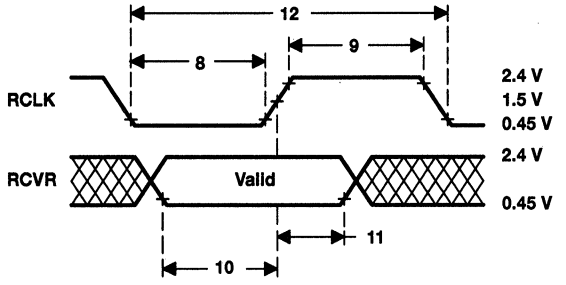


Figure 10. RCLK and RCVR Timing

timing requirements over recommended range of supply voltage (unless otherwise noted)

loop parameters (see Figures 8, 11, and 12)

	TEST CONDITIONS	MIN	MAX	UNIT
Filter voltage, low	f = 30.8 MHz, See Note 13	2		V
Filter voltage, high	f = 33.3 MHz, See Note 13		3	V
VCO gain (G_O)	f1 = 28.6 MHz, f2 = 36.4 MHz, See Note 14	12.75	17.25	MHz/V
Phase-detector gain (G_d)	$I_{(FILTER)1}$ = +50 µA, $I_{(FILTER)2}$ = – 50 µA, f = 32 MHz, See Note 15	5.40	7.20	µA/ns

NOTES: 13. The frequency f is applied to XTAL with FRAQ high as shown in Figure 11. The voltage at FILTER is measured after lock is achieved.

14. A frequency of f1 is applied to the XTAL with FRAQ high. After lock is achieved, the voltage at FILTER is measured (V1). This is repeated using f2 and measuring V2. VCO gain is calculated as (f2 – f1) / (V2 – V1). The result is in Hz / V (see external filter section).

15. The circuit of Figure 8 is used to measure phase-detector gain with $I_{(FILTER)}$ injected at the filter test point. Figure 12 shows the relevant timing. With the TMS38054 in phase lock, the propagation delay (t_p) between RCVINA positive transition and RCLK negative transition is measured. A value t_{p1} is seen when $I_{(FILTER)} = I_{(FILTER)1}$, and a value of t_{p2} is seen when $I_{(FILTER)} = I_{(FILTER)2}$. The phase-detector gain is then calculated as $(I_{(FILTER)2} - I_{(FILTER)1}) \div (t_{p1} - t_{p2})$. The result is in µA/ns (see external filter section).

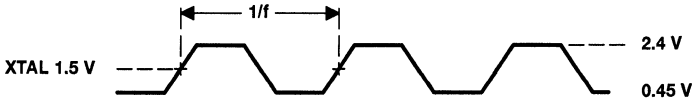


Figure 11. VCO-Gain and Filter-Voltage Test Timing

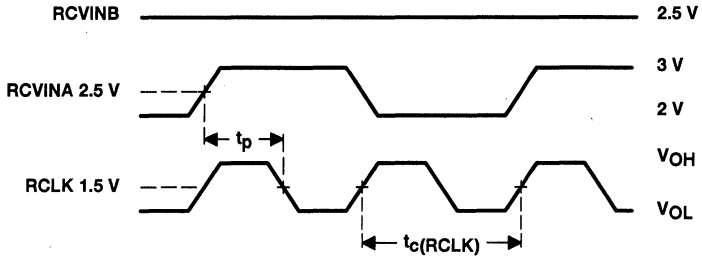


Figure 12. Phase-Detector-Gain Test Timing

timing requirements over recommended range of supply voltage (unless otherwise noted)

data recovery (see Figures 8 and 13 and Note 16)

NO.			TEST CONDITIONS	MIN	MAX	UNIT
13	t_{se}	Static timing error from voltage midpoint of RCVINA edge to midpoint to RCVINA pulse	4 Mbps, f = 8 MHz		±20	ns
			16 Mbps, f = 32 MHz		±3.62	

NOTE 16: The TMS38054 is phase locked to a RCVINA waveform as shown in Figure 13 with RCVINB biased to 2.5 V. RCVR is monitored for proper data being latched. For one pulse, shorten the time at which RCVINA's negative transition occurs. Check RCVR if the short pulse was latched. Restabilize the VCO with normal pulses. Input another short pulse. Continue this routine, while gradually shortening the pulse, until the data is not latched. The time between this negative transition and the midpoint of the original pulse's uptime is t_{se}. Repeat this procedure using all of the RCVINA waveforms shown.

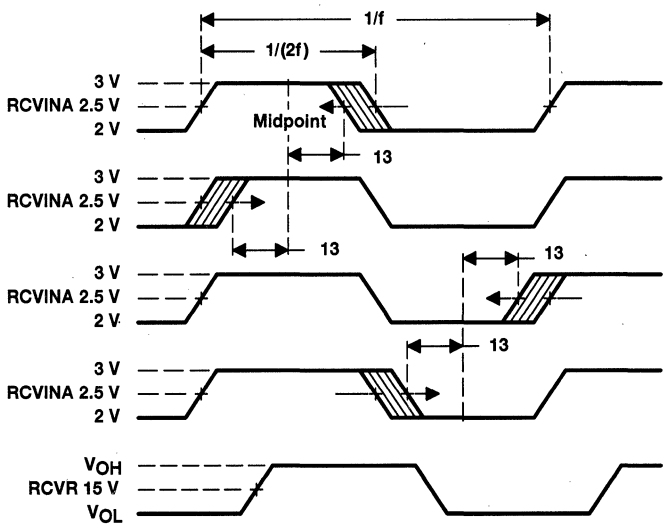


Figure 13. TMS38054 Phase Locked to RCVINA

timing requirements over recommended range of supply voltage (unless otherwise noted) (continued)

energy detect ($\overline{\text{REDY}}$) (see Figure 8 and Note 17)

NO.			TEST CONDITIONS	MIN	MAX	UNIT
14	$t_{d(REDYHL)}$	Delay time, FRAQ transition to REDY low again	Data transition density = 100%, See Figure 14	2		µs
			Data transition density = 33%, See Figure 14	6	100	
15	$t_{d(REDYH)}$	Delay time, data loss to $\overline{\text{REDY}}$ high	Data transition density changes 100% to 2.5%, See Figure 15	20	100	µs

NOTE 17: The transition density of the incoming data is the percentage of transitions of the incoming data as compared to the maximum possible number of transitions. For a string of Manchester-encoded 0 data, 100% transition density is a 16-MHz signal at a 16-Mbps data transmission rate.

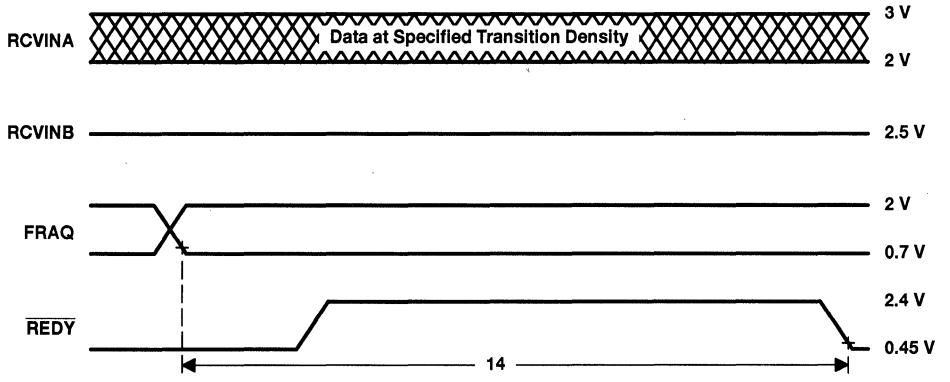


Figure 14. Timing Waveforms for Energy-Detect, FRAQ to $\overline{\text{REDY}}$ Timing

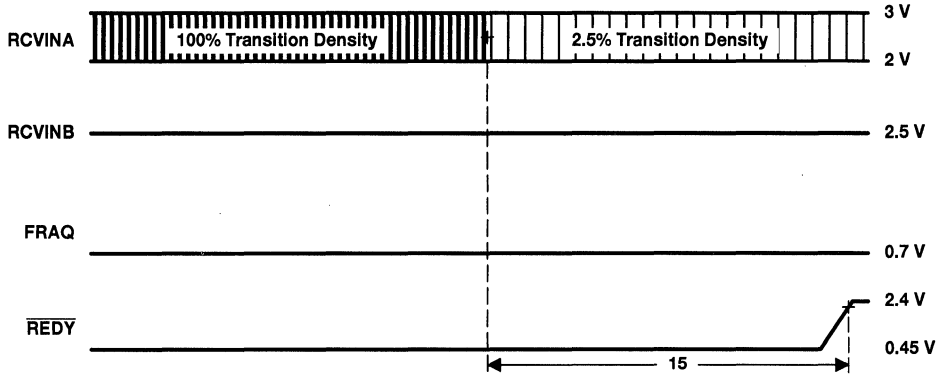


Figure 15. Timing Waveforms for Energy-Detect to Energy-Loss Timing

timing requirements over recommended range of supply voltage (unless otherwise noted) (continued)

watchdog timer (see Figures 16 and Notes 9, 18, 19, 20)

NO.		TEST CONDITIONS	MIN	MAX	UNIT
16	$t_{d(WDT)H}$ Delay time, watchdog-timer expiration	C_{wdt} = 1.5 μF, $R_{L1} = R_{L2}$ = 2.9 kΩ	21	50	ms

NOTES: 9. R_{L1} is connected from PHOUTA to ground; R_{L2} is connected from PHOUTB to ground.
18. To enable the phantom-driver signals, $\overline{NRST}$ must be toggled high with a maximum 20-ms period (50-Hz repetition rate). Phantom-driver signals are assured to be disabled if $\overline{NRST}$ does not toggle for 50 ms. The '380C2x software assures a maximum 20-ms period toggling rate for the insertion condition.
19. Pulse duration high of $\overline{NSRT}$ is not critical, but it is recommended that it be at least 125 ns.
20. C_{wdt} is the capacitor connected from WDTCAP to GND.

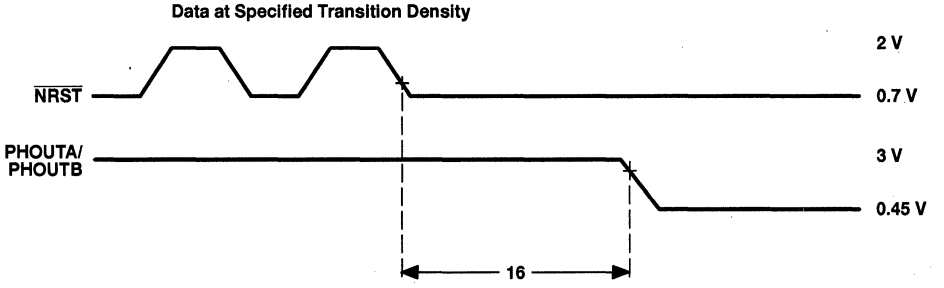


Figure 16. Watchdog-Timer Expiration Waveforms

Contents

SCBS127C – JULY 1992 – REVISED APRIL 1994

- **Free-Running CLKA and CLKB Can Be Asynchronous or Coincident**
- **64 × 36 Clocked FIFO Buffering Data From Port A to Port B**
- **Mailbox Bypass Register In Each Direction**
- **Programmable Almost-Full and Almost-Empty Flags**
- **Microprocessor Interface Control Logic**
- **Full Flag ($\overline{FF}$) and Almost-Full Flag ($\overline{AF}$) Synchronized by CLKA**
- **Empty Flag ($\overline{EF}$) and Almost-Empty Flag ($\overline{AE}$) Synchronized by CLKB**
- **Passive Parity Checking on Each Port**
- **Parity Generation Can Be Selected for Each Port**
- **Low-Power Advanced BiCMOS Technology**
- **Supports Clock Frequencies up to 67 MHz**
- **Fast Access Times of 10 ns**
- **Available in Space-Saving 120-Pin Thin Quad Flat Package (PCB) or 132-Pin Plastic Quad Flat Package (PQ)**

description

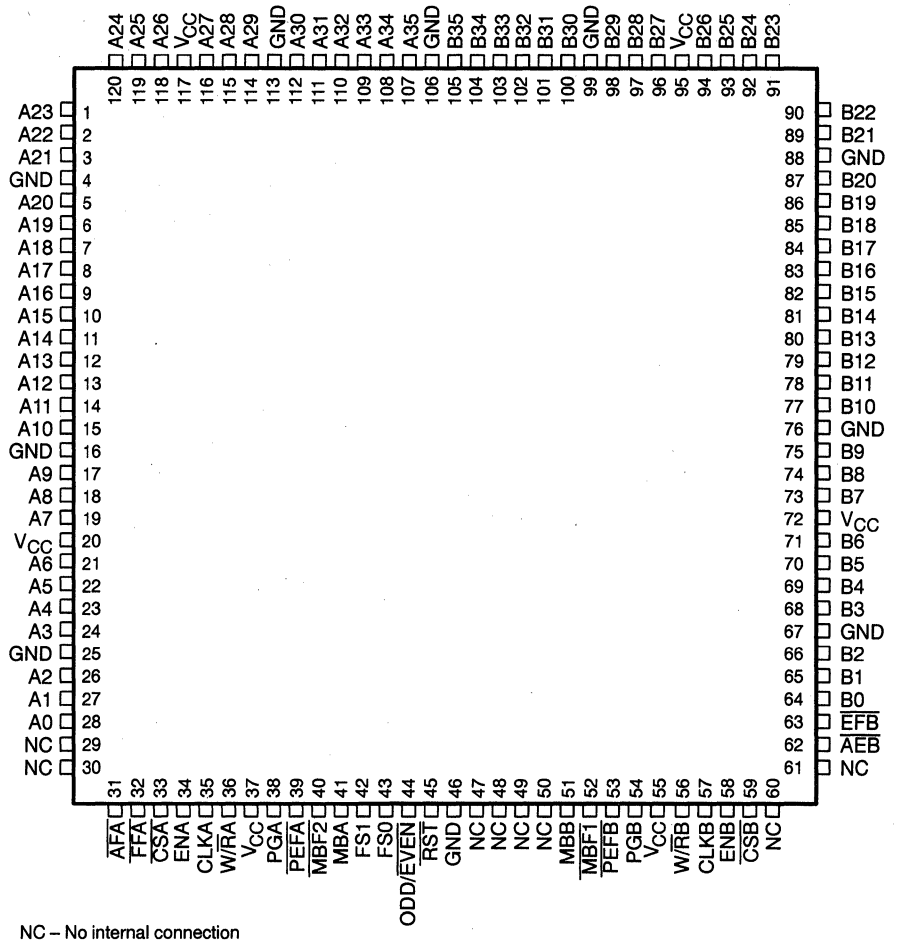
The SN74ABT3611 is a high-speed, low-power BiCMOS clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 10 ns. A 64 × 36 dual-port SRAM FIFO buffers data from port A to port B. The FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words are stored in memory. Communication between each port can take place through two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and can be ignored if not desired. Parity generation can be selected for data read from each port. Two or more devices can be used in parallel to create wider data paths.

The SN74ABT3611 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The full flag ($\overline{FF}$) and almost-full flag ($\overline{AF}$) of the FIFO are two-stage synchronized to the port clock that writes data to its array (CLKA). The empty flag ($\overline{EF}$) and almost-empty ($\overline{AE}$) flag of the FIFO are two-stage synchronized to the port clock that reads data from array (CLKB).

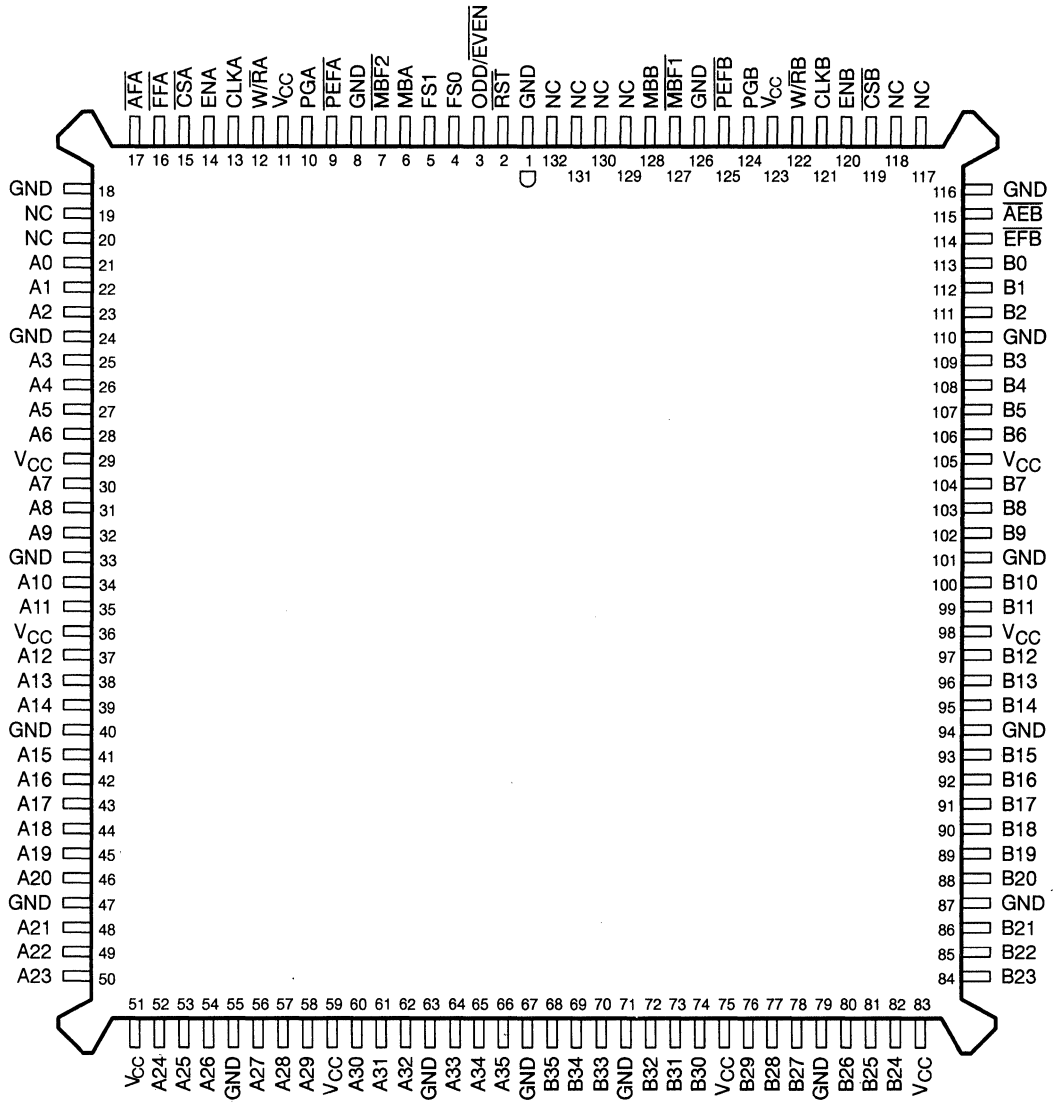
The SN74ABT3611 is characterized for operation from 0°C to 70°C.

PCB PACKAGE
(TOP VIEW)



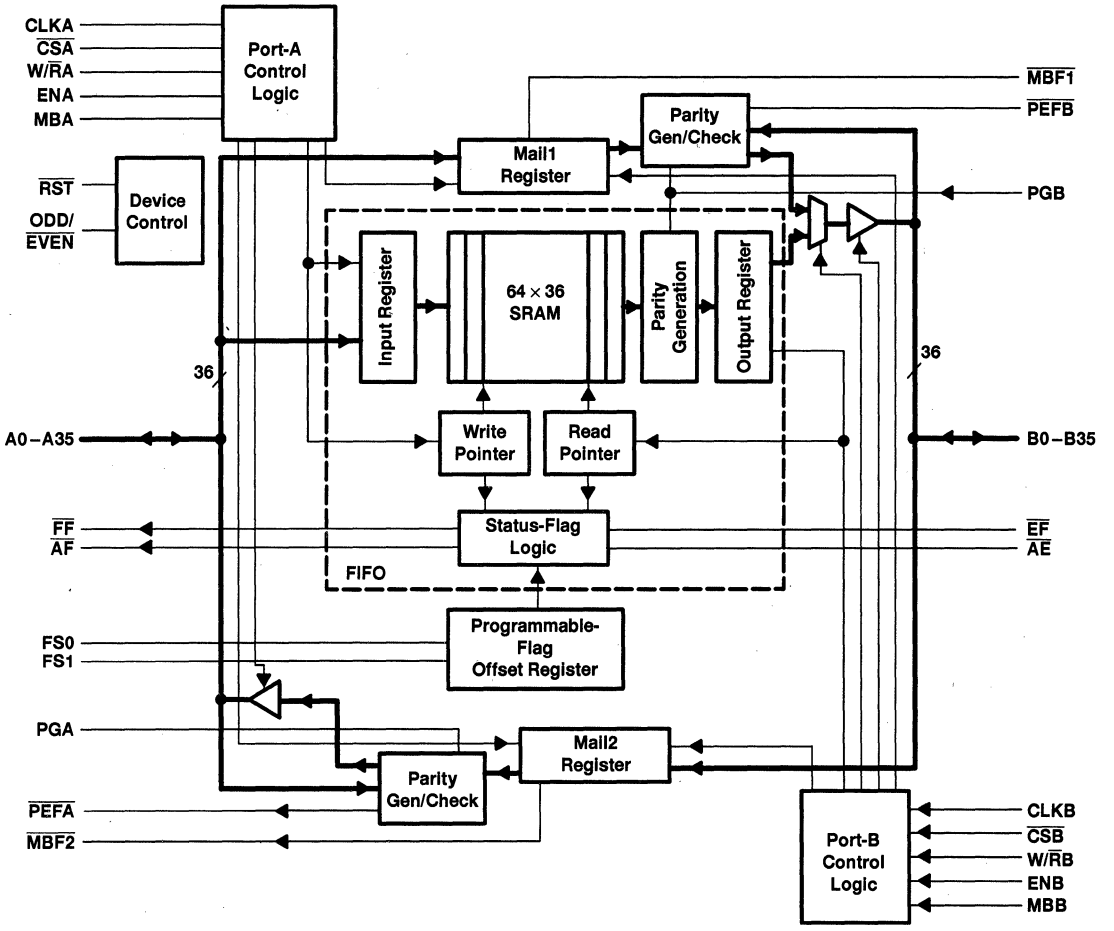
NC – No internal connection

PQ PACKAGE†
(TOP VIEW)



NC – No internal connection
† Uses Yamaichi socket IC51-1324-828

functional block diagram



Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
A0–A35	I/O	Port-A data. The 36-bit bidirectional data port for side A.
$\overline{AE}$	O	Almost-empty flag. Programmable almost-empty flag synchronized to CLKB. $\overline{AE}$ is low when the number of words in the FIFO is less than or equal to the value in the offset register, X.
$\overline{AF}$	O	Almost-full flag. Programmable almost-full flag synchronized to CLKA. $\overline{AF}$ is low when the number of empty locations in the FIFO is less than or equal to the value in the offset register, X.
B0–B35	I/O	Port-B data. The 36-bit bidirectional data port for side B.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. $\overline{FF}$ and $\overline{AF}$ are synchronized to the low-to-high transition of CLKA.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. $\overline{EF}$ and $\overline{AE}$ are synchronized to the low-to-high transition of CLKB.
$\overline{CSA}$	I	Port-A chip select. $\overline{CSA}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{CSA}$ is high.
$\overline{CSB}$	I	Port-B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{CSB}$ is high.
$\overline{EF}$	O	Empty flag. $\overline{EF}$ is synchronized to the low-to-high transition of CLKB. When $\overline{EF}$ is low, the FIFO is empty and reads from its memory are disabled. Data can be read from the FIFO to its output register when $\overline{EF}$ is high. $\overline{EF}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKB after data is loaded into empty FIFO memory.
ENA	I	Port-A enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port-B enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
$\overline{FF}$	O	Full flag. $\overline{FF}$ is synchronized to the low-to-high transition of CLKA. When $\overline{FF}$ is low, the FIFO is full and writes to its memory are disabled. $\overline{FF}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKA after reset.
FS1, FS0	I	Flag-offset selects. The low-to-high transition of $\overline{RST}$ latches the values of FS0 and FS1, which loads one of four preset values into the almost-full and almost-empty offset register (X).
MBA	I	Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation.
MBB	I	Port-B mailbox select. A high level on MBB chooses a mailbox register for a port-B read or write operation. When the B0–B35 outputs are active, a high level on MBB selects data from the mail1 register for output and a low level selects the FIFO output register data for output.
$\overline{MBF1}$	O	Mail1 register flag. $\overline{MBF1}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is low. $\overline{MBF1}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and MBB is high. $\overline{MBF1}$ is set high when the device is reset.
$\overline{MBF2}$	O	Mail2 register flag. $\overline{MBF2}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is low. $\overline{MBF2}$ is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. $\overline{MBF2}$ is set high when the device is reset.
ODD/$\overline{EVEN}$	I	Odd/even parity select. Odd parity is checked on each port when ODD/$\overline{EVEN}$ is high, and even parity is checked when ODD/$\overline{EVEN}$ is low. ODD/$\overline{EVEN}$ also selects the type of parity generated for each port if parity generation is enabled for a read operation.
$\overline{PEFA}$	O (port A)	Port-A parity error flag. When any byte applied to terminals A0–A35 fails parity, $\overline{PEFA}$ is low. Bytes are organized as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/$\overline{EVEN}$ input. The parity trees used to check the A0–A35 inputs are shared by the mail2 register to generate parity if parity generation is selected by PGA. Therefore, if a mail2 read with parity generation is setup by having $\overline{CSA}$ low, ENA high, W/$\overline{RA}$ low, MBA high, and PGA high, the $\overline{PEFA}$ flag is forced high regardless of the state of the A0–A35 inputs.

Terminal Functions (Continued)

TERMINAL NAME	I/O	DESCRIPTION
$\overline{PEFB}$	O (port B)	Port-B parity error flag. When any byte applied to terminals B0–B35 fails parity, $\overline{PEFB}$ is low. Bytes are organized as B0–B8, B9–B17, B18–B26, and B27–B35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/$\overline{EVEN}$ input. The parity trees used to check the B0–B35 inputs are shared by the mail1 register to generate parity if parity generation is selected by PGB. Therefore, if a mail1 read with parity generation is setup by having $\overline{CSB}$ low, ENB high, W/$\overline{RB}$ low, MBB high, and PGB high, the $\overline{PEFB}$ flag is forced high regardless of the state of the B0–B35 inputs.
PGA	I	Port-A parity generation. Parity is generated for mail2 register reads from port A when PGA is high. The type of parity generated is selected by the state of the ODD/$\overline{EVEN}$ input. Bytes are organized as A0–A8, A9–A17, A18–A26, and A27–A35. The generated parity bits are output in the most significant bit of each byte.
PGB	I	Port-B parity generation. Parity is generated for data reads from port B when PGB is high. The type of parity generated is selected by the state of the ODD/$\overline{EVEN}$ input. Bytes are organized as B0–B8, B9–B17, B18–B26, and B27–B35. The generated parity bits are output in the most significant bit of each byte.
$\overline{RST}$	I	Reset. To reset the device, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RST}$ is low. This sets the $\overline{AF}$, $\overline{MBF1}$, and $\overline{MBF2}$ flags high and the $\overline{EF}$, $\overline{AE}$, and $\overline{FF}$ flags low. The low-to-high transition of $\overline{RST}$ latches the status of the FS1 and FS0 inputs to select almost-full and almost-empty flag offset.
W/$\overline{RA}$	I	Port-A write/read select. W/$\overline{RA}$ high selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{RA}$ is high.
W/$\overline{RB}$	I	Port-B write/read select. W/$\overline{RB}$ high selects a write operation and a low selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when W/$\overline{RB}$ is high.

detailed description

reset

The SN74ABT3611 is reset by taking the reset ($\overline{RST}$) input low for at least four port-A clock (CLKA) and four port-B clock (CLKB) low-to-high transitions. The reset input can switch asynchronously to the clocks. A device reset initializes the internal read and write pointers of the FIFO and forces the full flag ($\overline{FF}$) low, the empty flag ($\overline{EF}$) low, the almost-empty flag ($\overline{AE}$) low, and the almost-full flag ($\overline{AF}$) high. A reset also forces the mailbox flags ($\overline{MBF1}$, $\overline{MBF2}$) high. After a reset, $\overline{FF}$ is set high after two low-to-high transitions of CLKA. The device must be reset after power up before data is written to its memory.

A low-to-high transition on the $\overline{RST}$ input loads the almost-full and almost-empty offset register (X) with the value selected by the flag-select (FS0, FS1) inputs. The values that can be loaded into the register are shown in Table 1.

Table 1. Flag Programming

FS1	FS0	$\overline{RST}$	ALMOST-FULL AND ALMOST-EMPTY FLAG OFFSET REGISTER (X)
H	H	↑	16
H	L	↑	12
L	H	↑	8
L	L	↑	4

FIFO write/read operation

The state of the port-A data (A0–A35) outputs is controlled by the port-A chip select ($\overline{CSA}$) and the port-A write/read select (W/$\overline{RA}$). The A0–A35 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is high. The A0–A35 outputs are active when both $\overline{CSA}$ and W/$\overline{RA}$ are low. Data is loaded into the FIFO from the A0–A35 inputs on a low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is high, ENA is high, MBA is low, and $\overline{FF}$ is high (see Table 2).

Table 2. Port-A Enable Function Table

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	A0–A35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, mail2 register	None
L	L	H	L	↑	Active, mail2 register	None
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set $\overline{MBF2}$ high)

The port-B control signals are identical to those of port A. The state of the port-B data (B0–B35) outputs is controlled by the port-B chip select ($\overline{CSB}$) and the port-B write/read select (W/$\overline{RB}$). The B0–B35 outputs are in the high-impedance state when either $\overline{CSB}$ or W/$\overline{RB}$ is high. The B0–B35 outputs are active when both $\overline{CSB}$ and W/$\overline{RB}$ are low. Data is read from the FIFO to the B0–B35 outputs by a low-to-high transition of CLKB when $\overline{CSB}$ is low, W/$\overline{RB}$ is low, ENB is high, MBB is high, and $\overline{EF}$ is high (see Table 3).

Table 3. Port-B Enable Function Table

$\overline{CSB}$	W/$\overline{RB}$	ENB	MBB	CLKB	B0–B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	None
L	H	H	H	↑	In high-impedance state	Mail2 write
L	L	L	L	X	Active, FIFO output register	None
L	L	H	L	↑	Active, FIFO output register	FIFO read
L	L	L	H	X	Active, mail1 register	None
L	L	H	H	↑	Active, mail1 register	Mail1 read (set $\overline{MBF1}$ high)

The setup and hold-time constraints to the port clocks for the port chip selects ($\overline{CSA}$, $\overline{CSB}$) and write/read selects (W/$\overline{RA}$, W/$\overline{RB}$) are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is low during a clock cycle, the port's chip select and write/read select can change states during the setup and hold-time window of the cycle.

synchronized FIFO flags

Each FIFO flag is synchronized to its port clock through two flip-flop stages. This is done to improve flag reliability by reducing the probability of metastable events on their outputs when CLKA and CLKB operate asynchronously to one another (see the application report *Metastability Performance of Clocked FIFOs* in the 1994 *High-Performance FIFO Memories Data Book,* literature #SCAD003B). $\overline{FF}$ and $\overline{AF}$ are synchronized to CLKA. $\overline{EF}$ and $\overline{AE}$ are synchronized to CLKB. Table 4 shows the relationship of the flags to the FIFO.

Table 4. FIFO Flag Operation

NUMBER OF WORDS IN THE FIFO	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA	
	$\overline{EF}$	$\overline{AE}$	$\overline{AF}$	$\overline{FF}$
0	L	L	H	H
1 to X	H	L	H	H
(X + 1) to [64 – (X + 1)]	H	H	H	H
(64 – X) to 63	H	H	L	H
64	H	H	L	L

† X is the value in the almost-empty flag and almost-full flag offset register.

empty flag ($\overline{EF}$)

The FIFO empty flag is synchronized to the port clock that reads data from its array (CLKB). When the empty flag is high, new data can be read to the FIFO output register. When the empty flag is low, the FIFO is empty and attempted FIFO reads are ignored.

The FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an empty flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. A word written to the FIFO can be read to the FIFO output register in a minimum of three port-B clock (CLKB) cycles; therefore, an empty flag is low if a word in memory is the next data to be sent to the FIFO output register and two CLKB cycles have not elapsed since the time the word was written. The empty flag of the FIFO is set high by the second low-to-high transition of CLKB, and the new data word can be read to the FIFO output register in the following cycle.

A low-to-high transition on CLKB begins the first synchronization cycle of a write if the clock transition occurs at time t_{sk1} or greater after the write. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 4).

full flag ($\overline{FF}$)

The FIFO full flag is synchronized to the port clock that writes data to its array (CLKA). When the full flag is high, an SRAM location is free to receive new data. No memory locations are free when the full flag is low and attempted writes to the FIFO are ignored.

Each time a word is written to the FIFO, its write pointer is incremented. The state machine that controls the full flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is full, full–1, or full–2. From the time a word is read from the FIFO, its previous memory location is ready to be written in a minimum of three port-A clock cycles. A full flag is low if less than two CLKA cycles have elapsed since the next memory write location has been read. The second low-to-high transition on CLKA after the read sets the full flag high and data can be written in the following clock cycle.

A low-to-high transition on CLKA begins the first synchronization cycle of a read if the clock transition occurs at time t_{sk1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figure 5).

almost-empty flag ($\overline{AE}$)

The FIFO almost-empty flag is synchronized to the port clock that reads data from its array (CLKB). The state machine that controls the almost-empty flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see *reset*). The almost-empty flag is low when the FIFO contains X or less words in memory and is high when the FIFO contains (X + 1) or more words.

Two low-to-high transitions on the port-B clock (CLKB) are required after a FIFO write for the almost-empty flag to reflect the new level of fill. The almost-empty flag of a FIFO containing (X + 1) or more words remains low if two CLKB cycles have not elapsed since the write that filled the memory to the (X + 1) level. The almost-empty flag is set high by the second CLKB low-to-high transition after the FIFO write that fills memory to the (X + 1) level. A low-to-high transition on CLKB begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the write that fills the FIFO to (X + 1) words. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 6).

almost-full flag ($\overline{AF}$)

The FIFO almost-full flag is synchronized to the port clock that writes data to its array (CLKA). The state machine that controls an almost-full flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is almost full, almost full–1, or almost full–2. The almost-full state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see *reset*). The almost-full flag is low when the FIFO contains (64 – X) or more words in memory and is high when the FIFO contains [64 – (X + 1)] or less words.

Two low-to-high transitions on the port-A clock (CLKA) are required after a FIFO read for the almost-full flag to reflect the new level of fill. The almost-full flag of a FIFO containing [64 – (X + 1)] or less words remains low if two CLKA cycles have not elapsed since the read that reduced the number of words in memory to [64 – (X + 1)]. The almost-full flag is set high by the second CLKA low-to-high transition after the FIFO read that reduces the number of words in memory to [64 – (X + 1)]. A low-to-high transition on CLKA begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the read that reduces the number of words in memory to [64 – (X + 1)]. Otherwise, the subsequent CLKA cycle can be the first synchronization cycle (see Figure 7).

mailbox registers

Two 36-bit bypass registers are on the SN74ABT3611 to pass command and control information between port A and port B. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A low-to-high transition on CLKA writes A0–A35 data to the mail1 register when a port-A write is selected by ($\overline{CSA}$, W/$\overline{RA}$, and ENA) with MBA high. A low-to-high transition on CLKB writes B0–B35 data to the mail2 register when a port-B write is selected by ($\overline{CSB}$, W/$\overline{RB}$, and ENB) with MBB high. Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) low. Attempted writes to a mail register are ignored while its mail flag is low.

When the port-B data (B0–B35) outputs are active, the data on the bus comes from the FIFO output register when the port-B mailbox select (MBB) input is low and from the mail1 register when MBB is high. Mail2 data is always present on the port-A data (A0–A35) outputs when they are active. The mail1 register flag ($\overline{MBF1}$) is set high by a low-to-high transition on CLKB when a port-B read is selected by ($\overline{CSB}$, W/$\overline{RB}$, and ENB) with MBB high. The mail2 register flag ($\overline{MBF2}$) is set high by a low-to-high transition on CLKA when a port-A read is selected by ($\overline{CSA}$, W/$\overline{RA}$, and ENA) with MBA high. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

parity checking

The port-A (A0–A35) inputs and port-B (B0–B35) inputs each have four parity trees to check the parity of incoming (or outgoing) data. A parity failure on one or more bytes of the input bus is reported by a low level on the port parity error flag ($\overline{PEFA}$, $\overline{PEFB}$). Odd or even parity checking can be selected, and the parity error flags can be ignored if this feature is not desired.

parity checking (continued)

Parity status is checked on each input bus according to the level of the odd/even parity (ODD/$\overline{\text{EVEN}}$) select input. A parity error on one or more bytes of a port is reported by a low level on the corresponding port parity error flag ($\overline{\text{PEFA}}$, $\overline{\text{PEFB}}$) output. Port-A bytes are arranged as A0–A8, A9–A17, A18–A26, and A27–A35, and port-B bytes are arranged as B0–B8, B9–B17, B18–B26, and B27–B35. When odd/even parity is selected, a port parity error flag ($\overline{\text{PEFA}}$, $\overline{\text{PEFB}}$) is low if any byte on the port has an odd/even number of low levels applied to its bits.

The four parity trees used to check the A0–A35 inputs are shared by the mail2 register when parity generation is selected for port-A reads (PGA = high). When a port-A read from the mail2 register with parity generation is selected with $\overline{\text{CSA}}$ low, ENA high, W/$\overline{\text{RA}}$ low, MBA high, and PGA high, the port-A parity error flag ($\overline{\text{PEFA}}$) is held high regardless of the levels applied to the A0–A35 inputs. Likewise, the parity trees used to check the B0–B35 inputs are shared by the mail1 register when parity generation is selected for port-B reads (PGB = high). When a port-B read from the mail1 register with parity generation is selected with $\overline{\text{CSB}}$ low, ENB high, W/$\overline{\text{RB}}$ low, MBB high, and PGB high, the port-B parity error flag ($\overline{\text{PEFB}}$) is held high regardless of the levels applied to the B0–B35 inputs.

parity generation

A high level on the port-A parity generate select (PGA) or port-B parity generate select (PGB) enables the SN74ABT3611 to generate parity bits for port reads from a FIFO or mailbox register. Port-A bytes are arranged as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit of each byte used as the parity bit. Port-B bytes are arranged as B0–B8, B9–B17, B18–B26, and B27–B35, with the most significant bit of each byte used as the parity bit. A write to a FIFO or mail register stores the levels applied to all thirty-six inputs regardless of the state of the parity generate select (PGA, PGB) inputs. When data is read from a port with parity generation selected, the lower eight bits of each byte are used to generate a parity bit according to the level on the ODD/$\overline{\text{EVEN}}$ select. The generated parity bits are substituted for the levels originally written to the most significant bits of each byte as the word is read to the data outputs.

Parity bits for FIFO data are generated after the data is read from SRAM and before the data is written to the output register. Therefore, the port-B parity generate select (PGB) and ODD/$\overline{\text{EVEN}}$ have setup and hold-time constraints to the port-B clock (CLKB) for a rising edge of CLKB used to read a new word to the FIFO output register.

The circuit used to generate parity for the mail1 data is shared by the port-B bus (B0–B35) to check parity and the circuit used to generate parity for the mail2 data is shared by the port-A bus (A0–A35) to check parity. The shared parity trees of a port are used to generate parity bits for the data in a mail register when the port write/read select (W/$\overline{\text{RA}}$, W/$\overline{\text{RB}}$) input is low, the port mail select (MBA, MBB) input is high, chip select ($\overline{\text{CSA}}$, $\overline{\text{CSB}}$) is low, enable (ENA, ENB) is high, and port parity generate select (PGA, PGB) is high. Generating parity for mail-register data does not change the contents of the register.

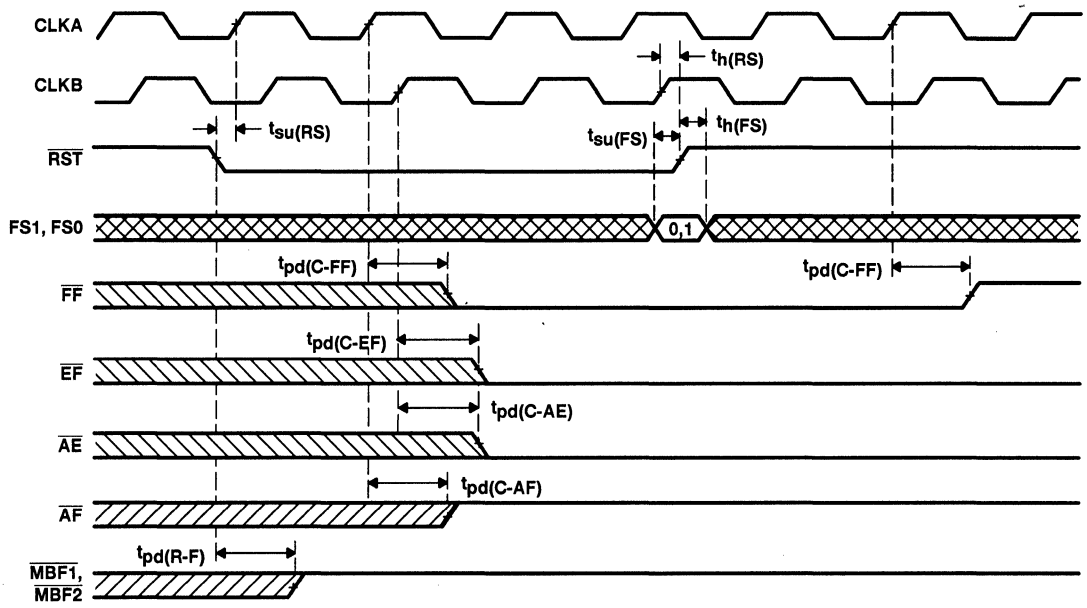


Figure 1. Device Reset Loading the X Register With the Value of Eight

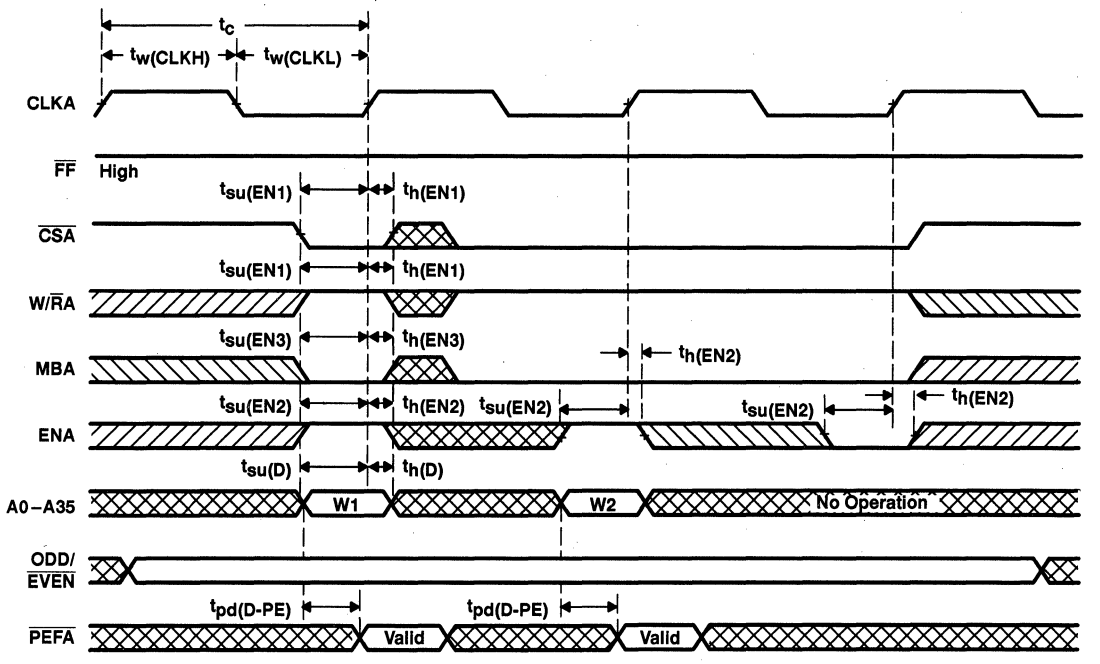


Figure 2. FIFO1-Write-Cycle Timing

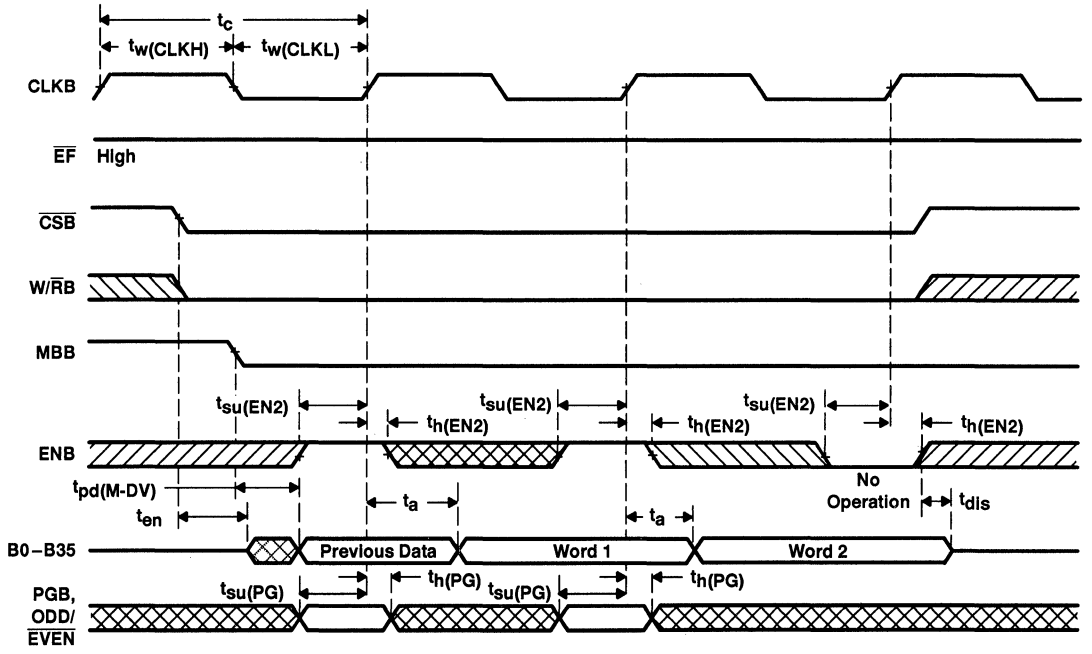
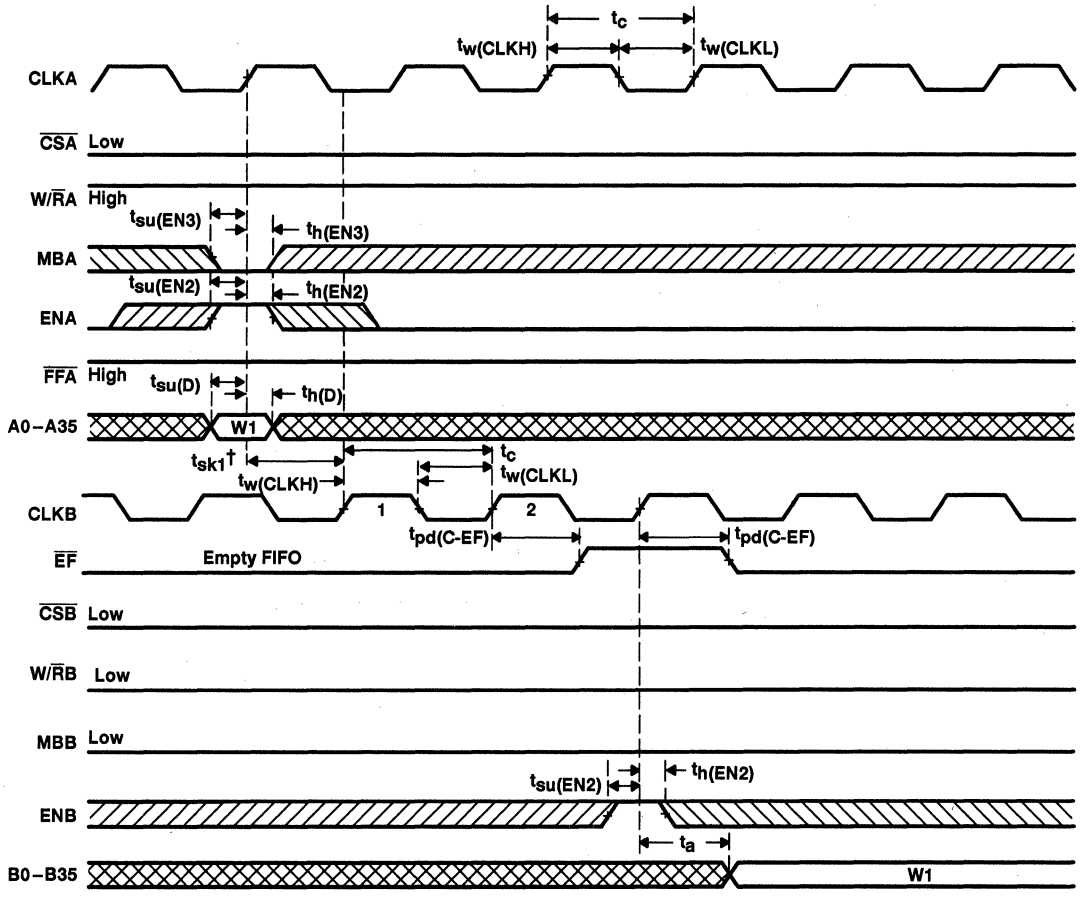
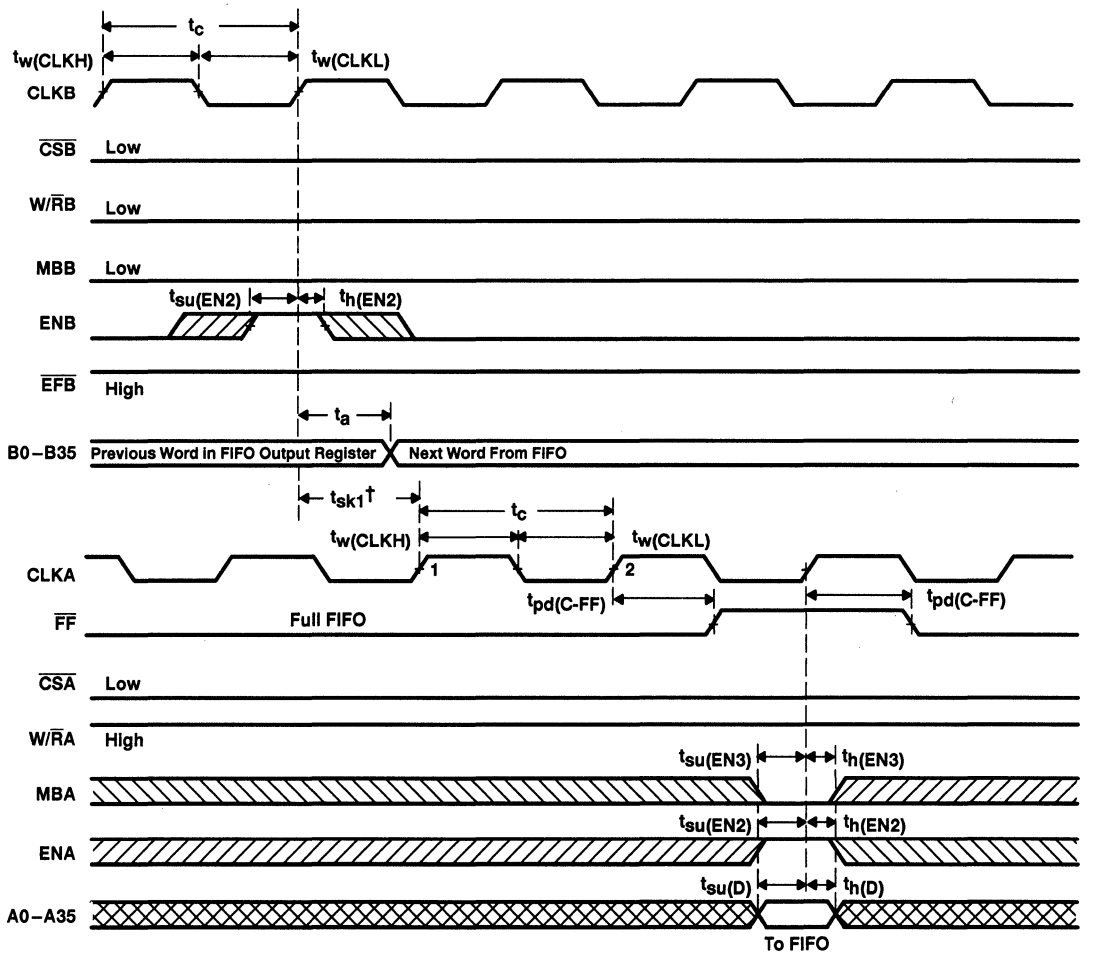


Figure 3. FIFO-Read-Cycle Timing



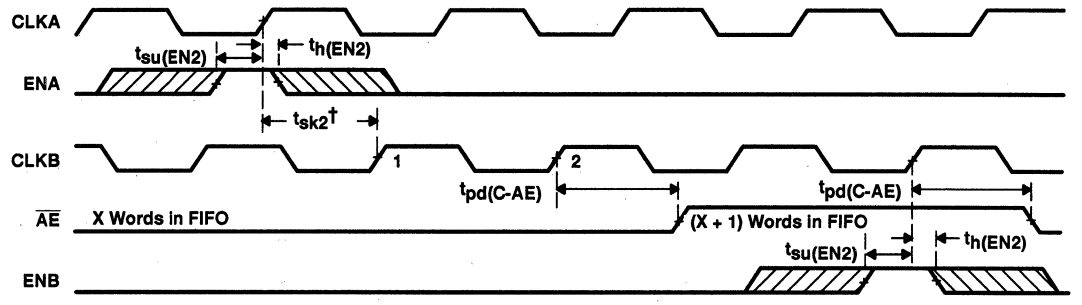
† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EF}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, the transition of $\overline{EF}$ high may occur one CLKB cycle later than shown.

Figure 4. $\overline{EF}$-Flag Timing and First Data Read When the FIFO Is Empty



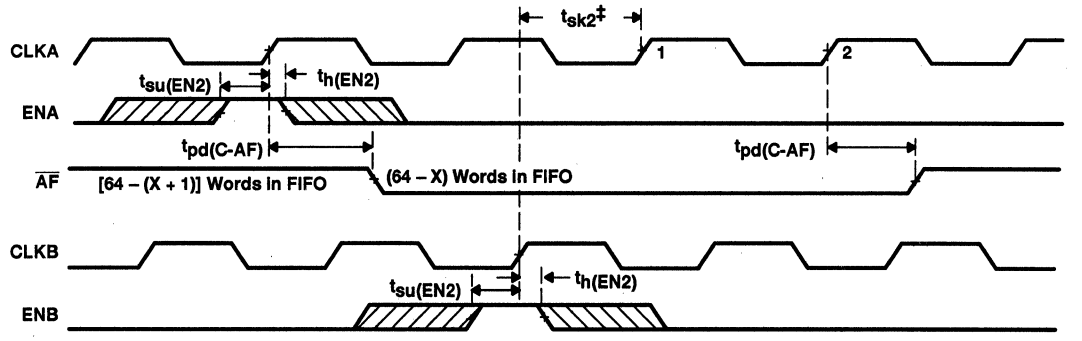
† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{FF}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less t_{sk1}, $\overline{FF}$ may transition high one CLKA cycle later than shown.

Figure 5. $\overline{FF}$-Flag Timing and First Available Write When the FIFO Is Full



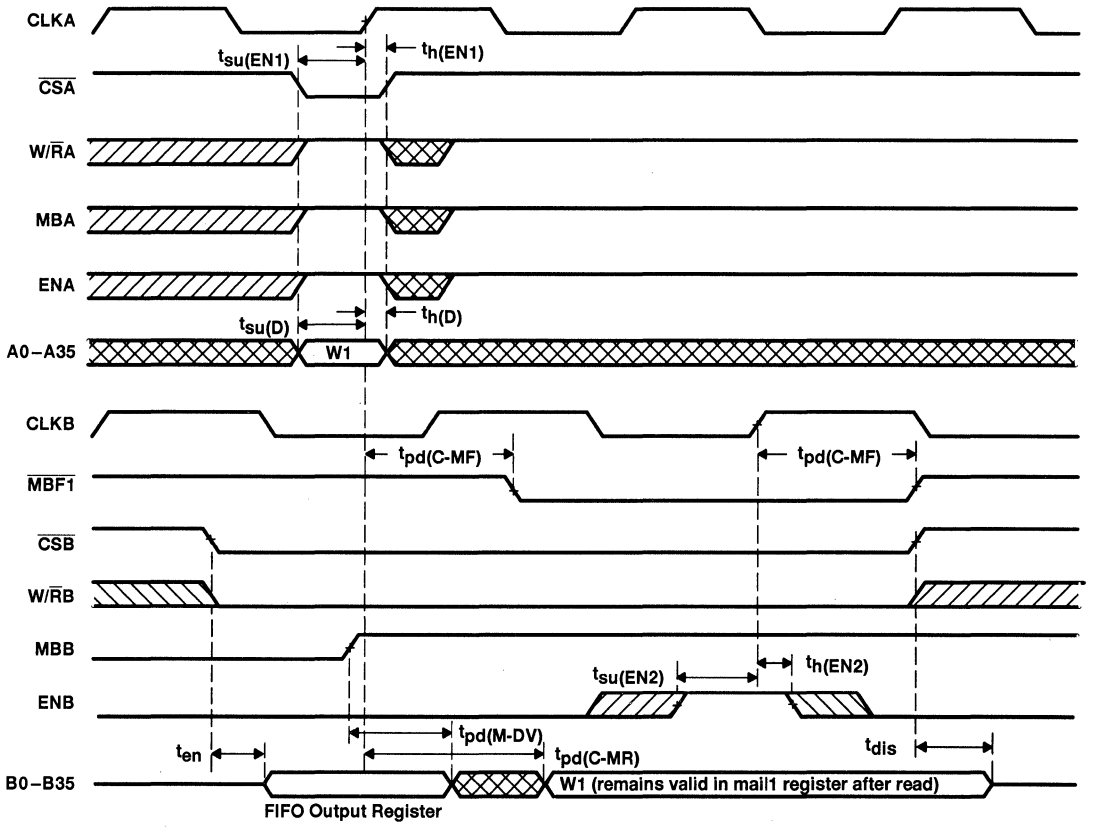
† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AE}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, $\overline{AE}$ may transition high one CLKB cycle later than shown.
NOTE A: FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L).

Figure 6. Timing for $\overline{AE}$ When the FIFO Is Almost Empty



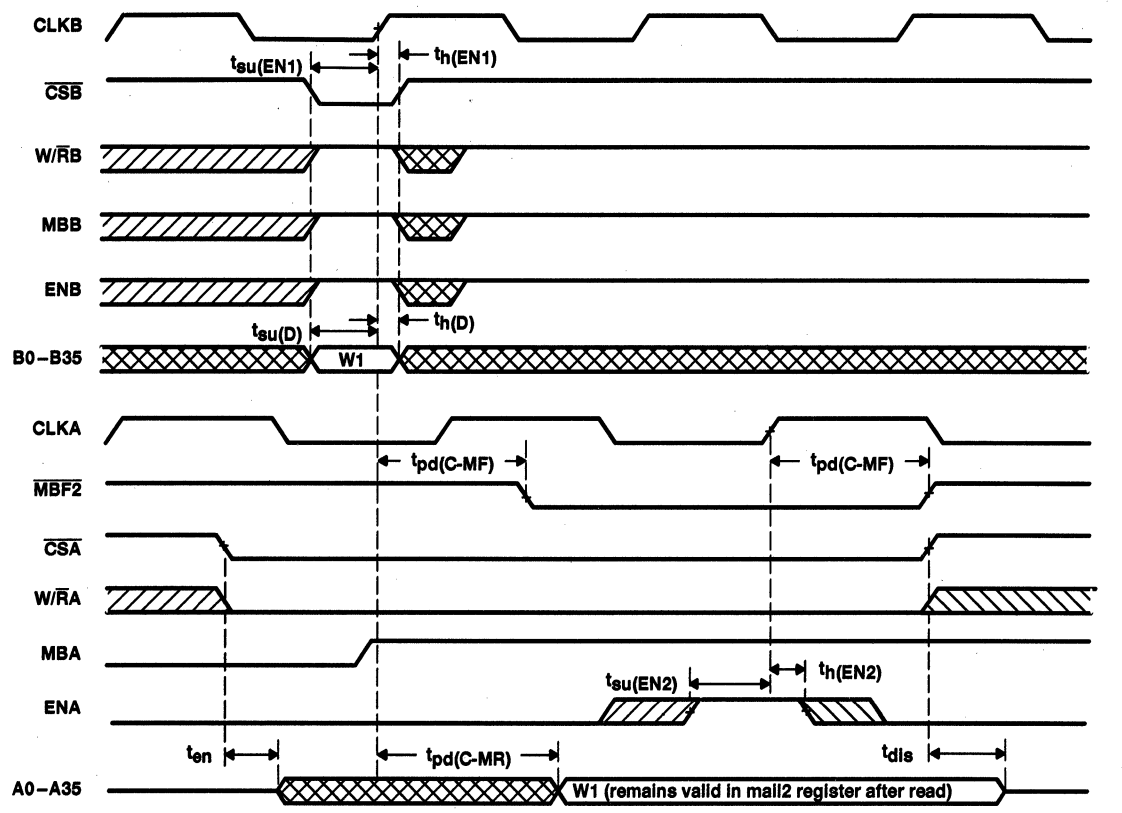
‡ t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AF}$ to transition high in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, $\overline{AF}$ may transition high one CLKB cycle later than shown.
NOTE A: FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L).

Figure 7. Timing for $\overline{AF}$ When the FIFO Is Almost Full



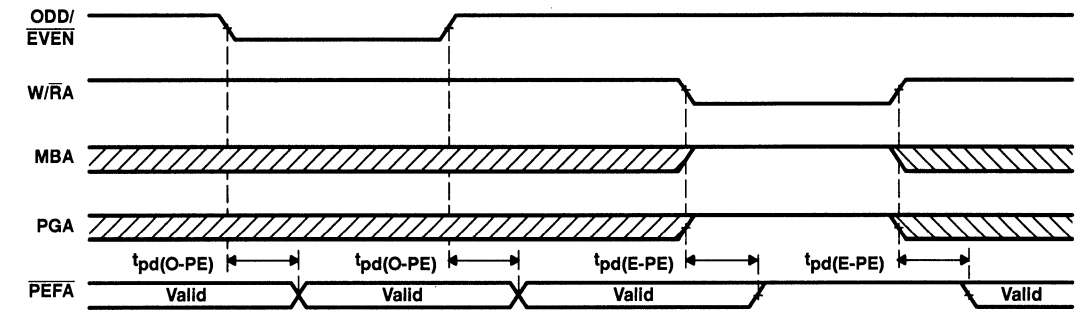
NOTE A: Port-B parity generation off (PGB = L)

Figure 8. Timing for Mail1 Register and $\overline{\text{MBF1}}$ Flag



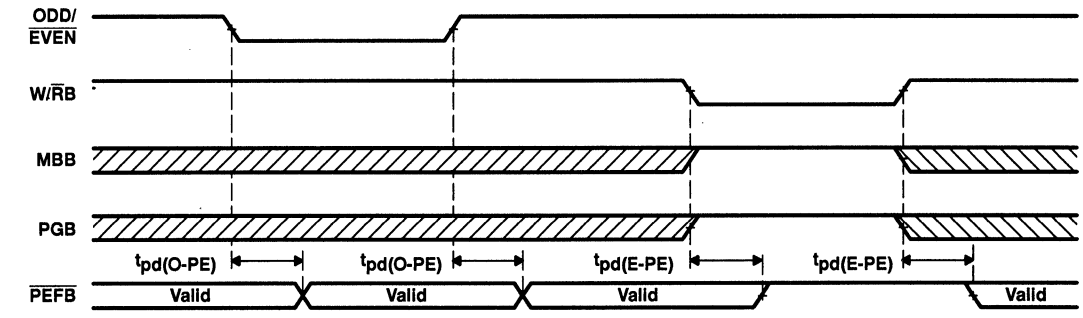
NOTE A: Port-A parity generation off (PGA = L)

Figure 9. Timing for Mail2 Register and $\overline{MBF2}$ Flag



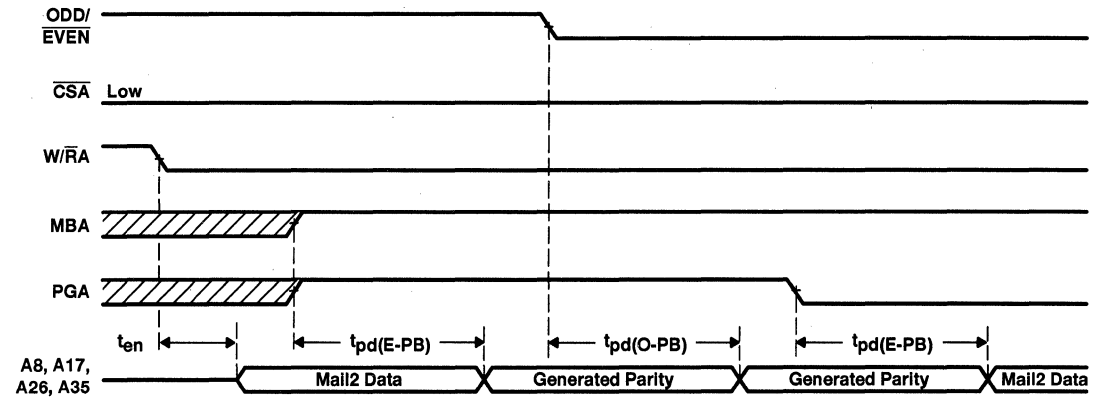
NOTE A: $\overline{CSA}$ = L and ENA = H

Figure 10. ODD/$\overline{EVEN}$, W/$\overline{RA}$, MBA, and PGA to $\overline{PEFA}$ Timing



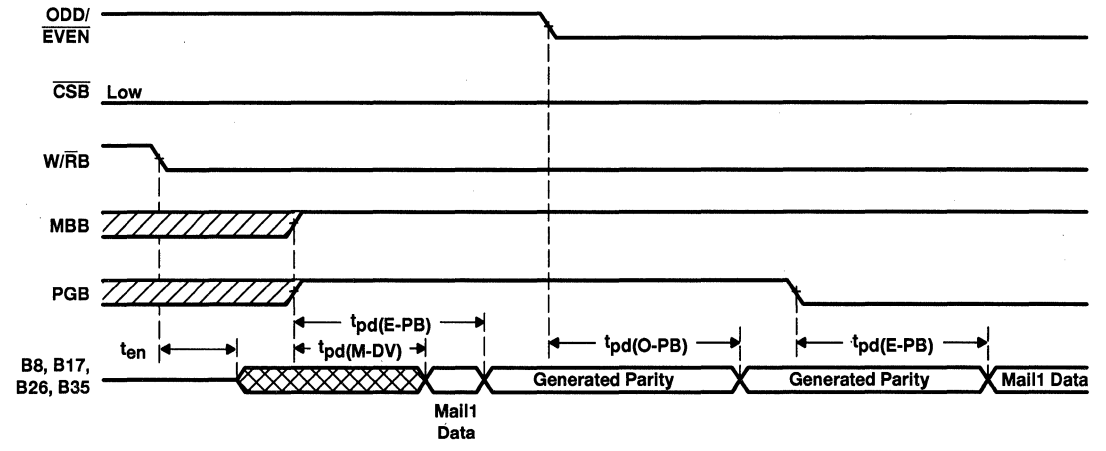
NOTE A: $\overline{CSB}$ = L and ENB = H

Figure 11. ODD/$\overline{EVEN}$, W/$\overline{RB}$, MBB, and PGB to $\overline{PEFB}$ Timing



NOTE A: ENA = H

Figure 12. Parity-Generation Timing When Reading From the Mail2 Register



NOTE A: ENB = H

Figure 13. Parity-Generation Timing When Reading From the Mail1 Register

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±500 mA
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−4	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS				MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −4 mA			2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.5	V
I_I	V_{CC} = 5.5 V,	$V_I = V_{CC}$ or 0					±50	µA
I_{OZ}	V_{CC} = 5.5 V,	$V_O = V_{CC}$ or 0					±50	µA
I_{CC}	V_{CC} = 5.5 V,	I_O = 0 mA,	$V_I = V_{CC}$ or GND	Outputs high			60	mA
				Outputs low			130	
				Outputs disabled			60	
C_i	V_I = 0,	f = 1 MHz				4		pF
C_o	V_O = 0,	f = 1 MHz				8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 13)

		'ABT3611-15		'ABT3611-20		'ABT3611-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_c	Clock cycle time, CLKA or CLKB	15		20		30		MHz
$t_{w(CLKH)}$	Pulse duration, CLKA and CLKB high	6		8		12		ns
$t_{w(CLKL)}$	Pulse duration, CLKA and CLKB low	6		8		12		ns
$t_{su(D)}$	Setup time, A0–A35 before CLKA↑ and B0–B35 before CLKB↑	4		5		6		ns
$t_{su(EN1)}$	Setup time, $\overline{CSA}$, W/$\overline{RA}$ before CLKA↑; $\overline{CSB}$, W/$\overline{RB}$, before CLKB↑	6		6		7		ns
$t_{su(EN2)}$	Setup time, ENA before CLKA↑; ENB before CLKB↑	4		5		6		ns
$t_{su(EN3)}$	Setup time, MBA before CLKA↑; ENB before CLKB↑	4		5		6		ns
$t_{su(PG)}$	Setup time, ODD/$\overline{EVEN}$ and PGB before CLKB↑†	4		5		6		ns
$t_{su(RS)}$	Setup time, $\overline{RST}$ low before CLKA↑ or CLKB↑‡	5		6		7		ns
$t_{su(FS)}$	Setup time, FS0 and FS1 before $\overline{RST}$ high	5		6		7		ns
$t_{h(D)}$	Hold time, A0–A35 after CLKA↑ and B0–B35 after CLKB↑	1		1		1		ns
$t_{h(EN1)}$	Hold time, $\overline{CSA}$, W/$\overline{RA}$ after CLKA↑; $\overline{CSB}$, W/$\overline{RB}$ after CLKB↑	1		1		1		ns
$t_{h(EN2)}$	Hold time, ENA after CLKA↑; ENB after CLKB↑	1		1		1		ns
$t_{h(EN3)}$	Hold time, MBA after CLKA↑; MBB after CLKB↑	1		1		1		ns
$t_{h(PG)}$	Hold time, ODD/$\overline{EVEN}$ and PGB after CLKB↑†	0		0		0		ns
$t_{h(RS)}$	Hold time, $\overline{RST}$ low after CLKA↑ or CLKB↑‡	6		6		7		ns
$t_{h(FS)}$	Hold time, FS0 and FS1 after $\overline{RST}$ high	4		4		4		ns
t_{sk1}§	Skew time between CLKA↑ and CLKB↑ for $\overline{EFA}$, $\overline{EFB}$, $\overline{FFA}$, and $\overline{FFB}$	8		8		10		ns
t_{sk2}§	Skew time between CLKA↑ and CLKB↑ for $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$, and $\overline{AFB}$	9		16		20		ns

† Only applies for a rising edge of CLKB that does a FIFO read

‡ Requirement to count the clock edge as one of at least four needed to reset a FIFO

§ Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Figures 1 through 13)

PARAMETER		'ABT3611-15		'ABT3611-20		'ABT3611-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_a	Access time, CLKB↑ to B0–B35	2	10	2	12	2	15	ns
$t_{pd(C-FF)}$	Propagation delay time, CLKA↑ to $\overline{FF}$	2	10	2	12	2	15	ns
$t_{pd(C-EF)}$	Propagation delay time, CLKB↑ to $\overline{EF}$	2	10	2	12	2	15	ns
$t_{pd(C-AE)}$	Propagation delay time, CLKB↑ to $\overline{AE}$	2	10	2	12	2	15	ns
$t_{pd(C-AF)}$	Propagation delay time, CLKA↑ to $\overline{AF}$	2	10	2	12	2	15	ns
$t_{pd(C-MF)}$	Propagation delay time, CLKA↑ to $\overline{MBF1}$ low or $\overline{MBF2}$ high and CLKB↑ to $\overline{MBF2}$ low or $\overline{MBF1}$ high	1	9	1	12	1	15	ns
$t_{pd(C-MR)}$	Propagation delay time, CLKA↑ to B0–B35† and CLKB↑ to A0–A35‡	3	12	3	14	3	16	ns
$t_{pd(M-DV)}$	Propagation delay time, MBB to B0–B35 valid	1	11	1	11.5	1	12	ns
$t_{pd(D-PE)}$	Propagation delay time, A0–A35 valid to $\overline{PEFA}$ valid; B0–B35 valid to $\overline{PEFB}$ valid	3	12	3	13	3	14	ns
$t_{pd(O-PE)}$	Propagation delay time, ODD/$\overline{EVEN}$ to $\overline{PEFA}$ and $\overline{PEFB}$	3	11	3	12	3	14	ns
$t_{pd(O-PB)}$§	Propagation delay time, ODD/$\overline{EVEN}$ to parity bits (A8, A17, A26, A35) and (B8, B17, B26, B35)	2	12	2	13	2	15	ns
$t_{pd(E-PE)}$	Propagation delay time, $\overline{CSA}$, ENA, W/$\overline{RA}$, MBA, or PGA to $\overline{PEFA}$; $\overline{CSB}$, ENB, W/$\overline{RB}$, MBB, or PGB to $\overline{PEFB}$	1	12	1	13	1	15	ns
$t_{pd(E-PB)}$§	Propagation delay time, $\overline{CSA}$, ENA, W/$\overline{RA}$, MBA, or PGA to parity bits (A8, A17, A26, A35); $\overline{CSB}$, ENB, W/$\overline{RB}$, MBB, or PGB to parity bits (B8, B17, B26, B35)	3	14	3	15	3	16	ns
$t_{pd(R-F)}$	Propagation delay time, $\overline{RST}$ to $\overline{AE}$ low and ($\overline{AF}$, $\overline{MBF1}$, $\overline{MBF2}$) high	1	15	1	20	1	30	ns
t_{en}	Enable time, $\overline{CSA}$ and W/$\overline{RA}$ low to A0–A35 active and $\overline{CSB}$ low and $\overline{W}$/RB high to B0–B35 active	2	10	2	12	2	14	ns
t_{dis}	Disable time, $\overline{CSA}$ or W/$\overline{RA}$ high to A0–A35 at high impedance and $\overline{CSB}$ high or $\overline{W}$/RB low to B0–B35 at high impedance	1	9	1	10	1	11	ns

† Writing data to the mail1 register when the B0–B35 outputs are active and MBB is high.
‡ Writing data to the mail2 register when the A0–A35 outputs are active and MBA is high.
§ Only applies when reading data from a mail register

TYPICAL CHARACTERISTICS

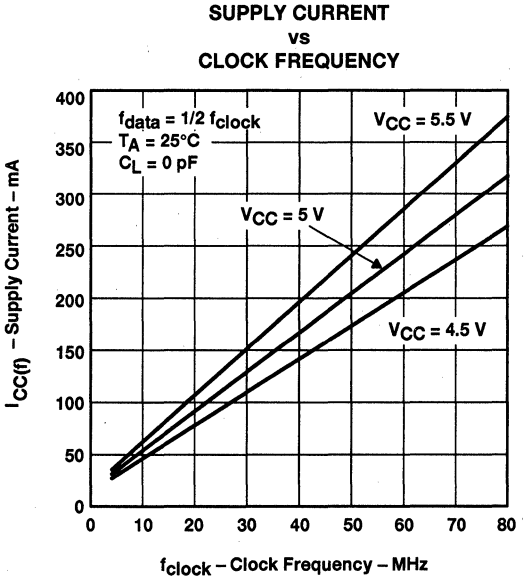


Figure 14

calculating power dissipation

The $I_{CC(f)}$ data for the graph was taken while simultaneously reading and writing the FIFO on the SN74ACT3611 with CLKA and CLKB operating at frequency f_{clock}. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitive load per data-output channel is known, the power dissipation can be calculated with the equation below.

With $I_{CC(f)}$ taken from Figure 14, the maximum power dissipation (P_T) of the SN74ABT3611 can be calculated by:

$$P_T = V_{CC} \times I_{CC(f)} + \Sigma(C_L \times (V_{OH} - V_{OL})^2 \times f_o)$$

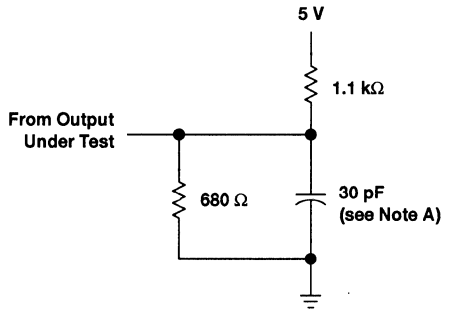
where:

C_L = output capacitive load
f_o = switching frequency of an output
V_{OH} = high-level output voltage
V_{OL} = low-level output voltage

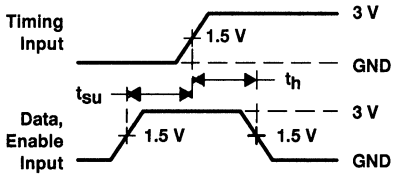
When no reads or writes are occurring on the SN74ABT3611, the power dissipated by a single clock (CLKA or CLKB) input running at frequency f_{clock} is calculated by:

$$P_T = V_{CC} \times f_{clock} \times 0.29 \text{ mA/MHz}$$

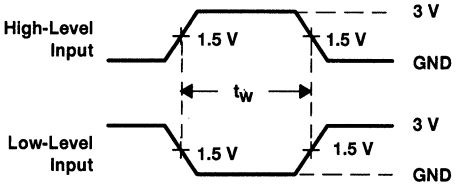
PARAMETER MEASUREMENT INFORMATION



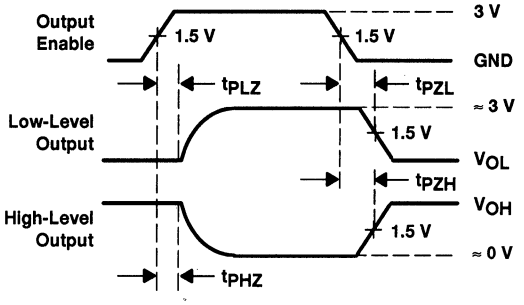
LOAD CIRCUIT



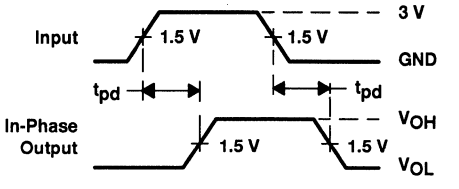
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTE A: Includes probe and jig capacitance

Figure 15. Load Circuit and Voltage Waveforms

SCBS129D – JULY 1992 – REVISED JANUARY 1994

- **Free-Running CLKA and CLKB Can Be Asynchronous or Coincident**
- **Two Independent 64 × 36 Clocked FIFOs Buffering Data in Opposite Directions**
- **Mailbox Bypass Register for Each FIFO**
- **Programmable Almost-Full and Almost-Empty Flags**
- **Microprocessor Interface Control Logic**
- **$\overline{\text{EFA}}$, $\overline{\text{FFA}}$, $\overline{\text{AEA}}$, and $\overline{\text{AFA}}$ Flags Synchronized by CLKA**
- **$\overline{\text{EFB}}$, $\overline{\text{FFB}}$, $\overline{\text{AEB}}$, and $\overline{\text{AFB}}$ Flags Synchronized by CLKB**
- **Passive Parity Checking on Each Port**
- **Parity Generation Can Be Selected for Each Port**
- **Low-Power Advanced BiCMOS Technology**
- **Supports Clock Frequencies up to 67 MHz**
- **Fast Access Times of 10 ns**
- **Available in Space-Saving 120-Pin Thin Quad Flat Package (PCB) or 132-Pin Plastic Quad Flat Package (PQ)**

description

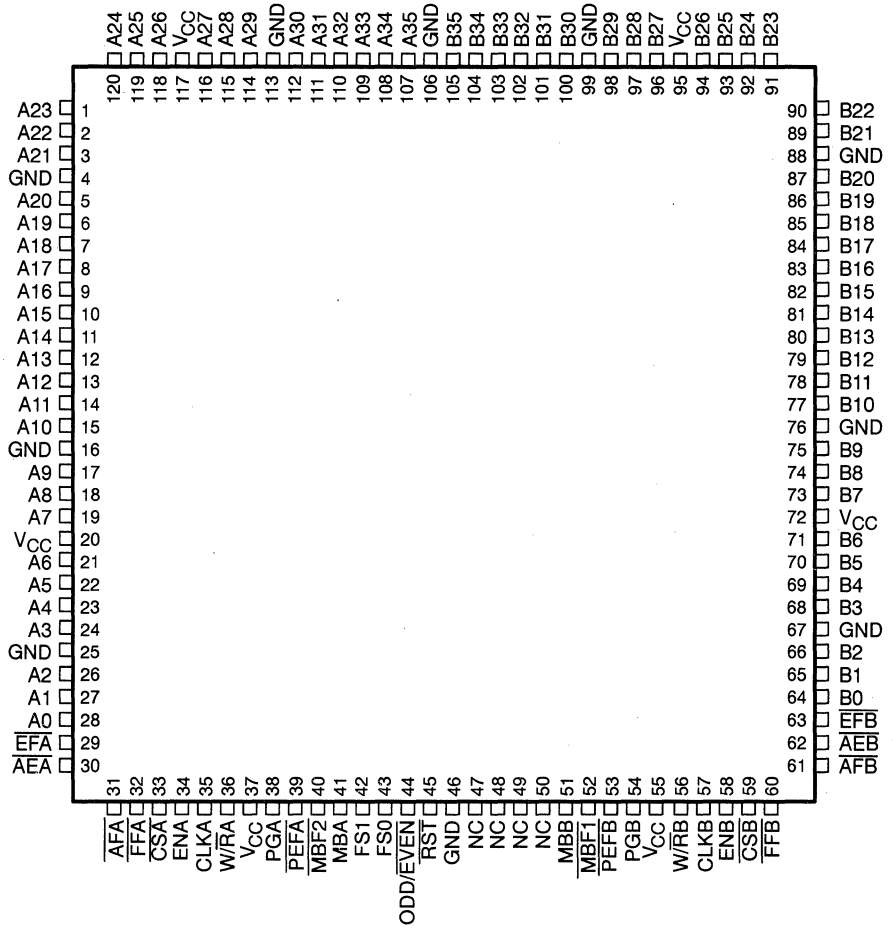
The SN74ABT3612 is a high-speed, low-power BiCMOS bidirectional clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 10 ns. Two independent 64 × 36 dual-port SRAM FIFOs on board the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions and two programmable flags (almost-full and almost-empty) to indicate when a selected number of words is stored in memory. Communication between each port can bypass the FIFOs via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and may be ignored if not desired. Parity generation can be selected for data read from each port. Two or more devices can be used in parallel to create wider data paths.

The SN74ABT3612 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The full flag ($\overline{\text{FFA}}$, $\overline{\text{FFB}}$) and almost-full ($\overline{\text{AFA}}$, $\overline{\text{AFB}}$) flag of a FIFO are two-stage synchronized to the port clock that writes data to its array. The empty flag ($\overline{\text{EFA}}$, $\overline{\text{EFB}}$) and almost-empty ($\overline{\text{AEA}}$, $\overline{\text{AEB}}$) flag of a FIFO are two-stage synchronized to the port clock that reads data from its array.

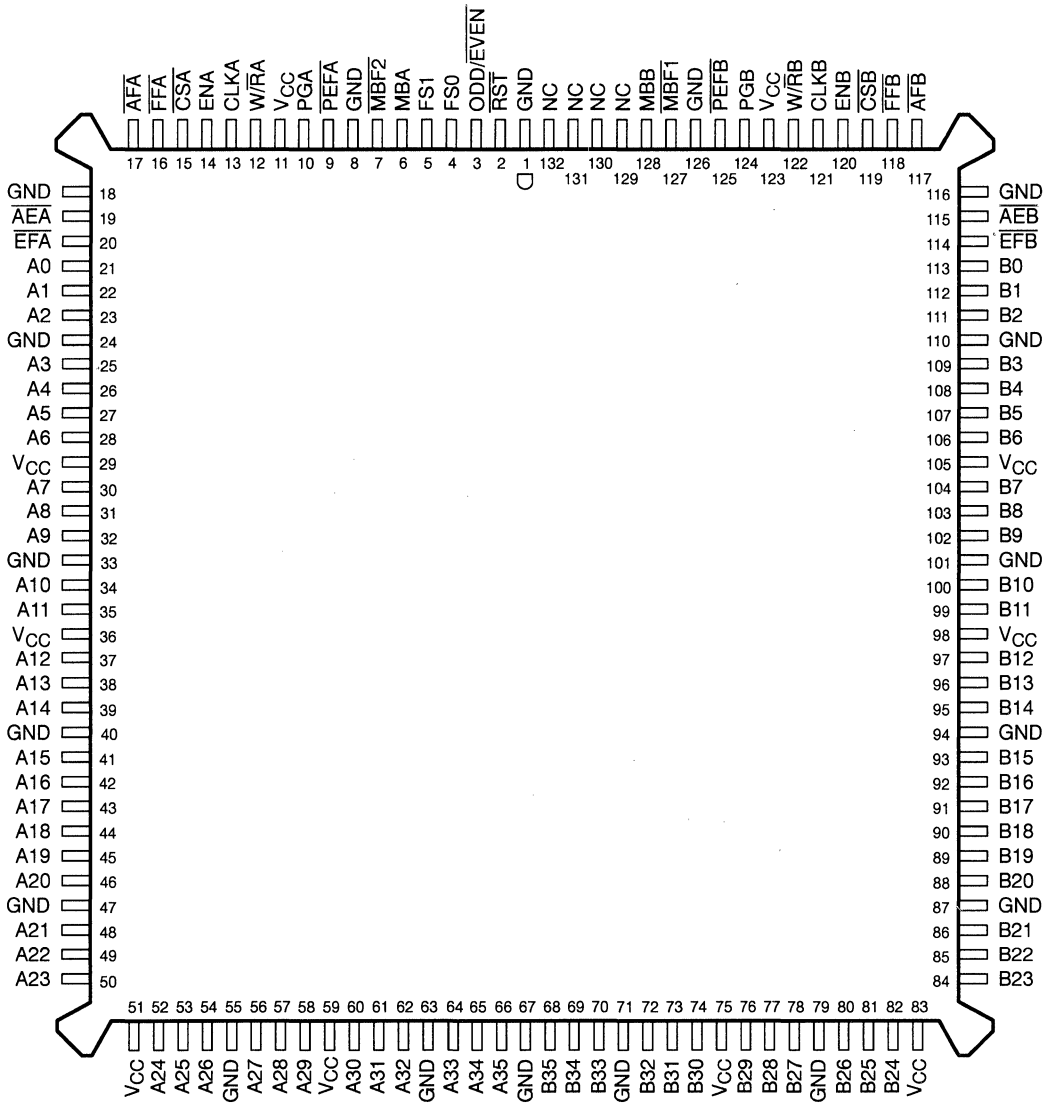
The SN74ABT3612 is characterized for operation from 0°C to 70°C.

PCB PACKAGE
(TOP VIEW)



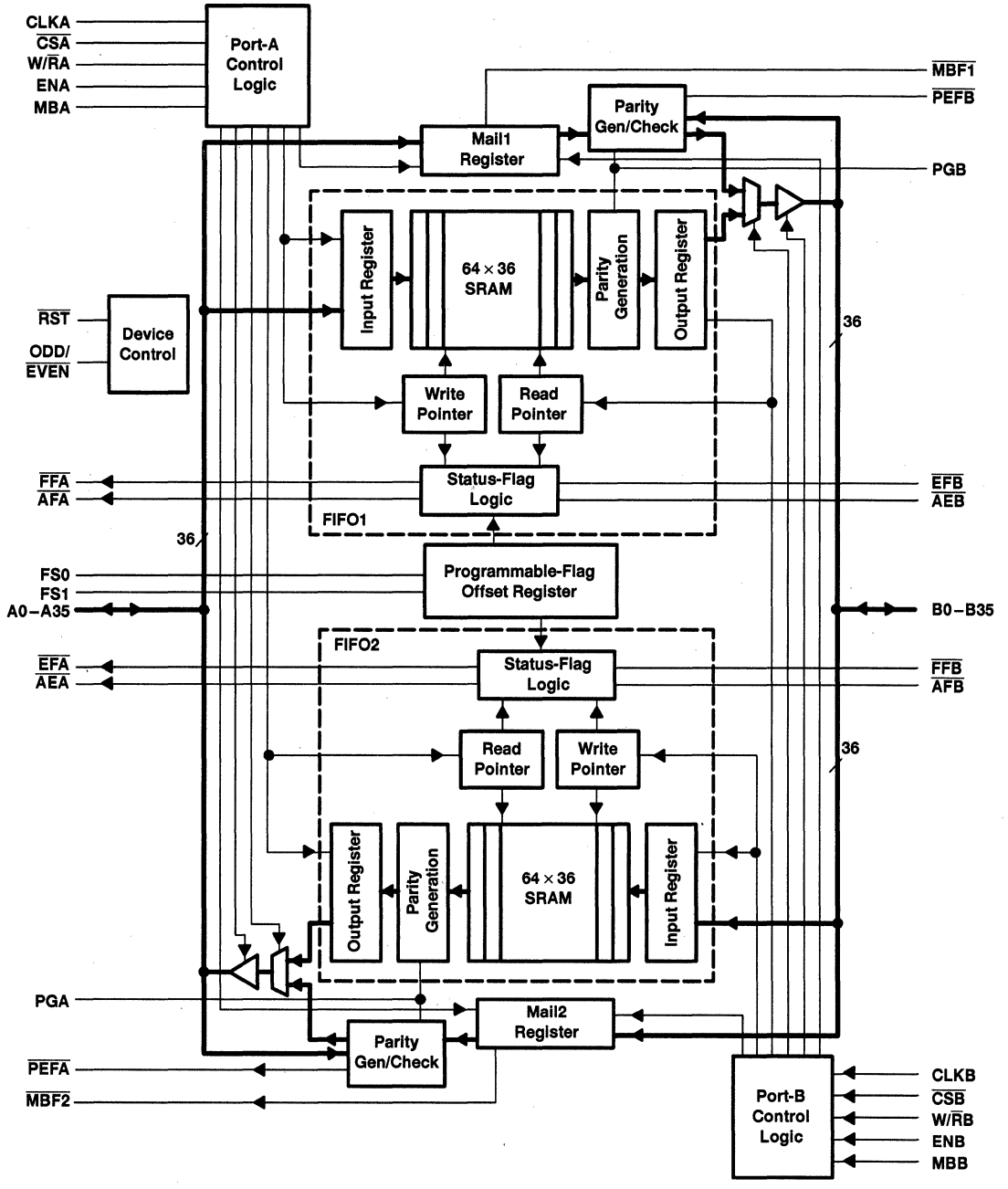
NC – No internal connection

PQ PACKAGE†
(TOP VIEW)



NC – No internal connection
† Uses Yamaichi socket IC51-1324-828

functional block diagram



Terminal Functions

PIN NAME	I/O	DESCRIPTION
A0–A35	I/O	Port-A data. The 36-bit bidirectional data port for side A.
$\overline{AEA}$	O (port A)	Port-A almost-empty flag. Programmable almost-empty flag synchronized to CLKA. $\overline{AEA}$ is low when the number of words in FIFO2 is less than or equal to the value in the offset register, X.
$\overline{AEB}$	O (port B)	Port-B almost-empty flag. Programmable almost-empty flag synchronized to CLKB. $\overline{AEB}$ is low when the number of words in FIFO1 is less than or equal to the value in the offset register, X.
$\overline{AFA}$	O (port A)	Port-A almost-full flag. Programmable almost-full flag synchronized to CLKA. $\overline{AFA}$ is low when the number of empty locations in FIFO1 is less than or equal to the value in the offset register, X.
$\overline{AFB}$	O (port B)	Port-B almost-full flag. Programmable almost-full flag synchronized to CLKB. $\overline{AFB}$ is low when the number of empty locations in FIFO2 is less than or equal to the value in the offset register, X.
B0–B35	I/O	Port-B data. The 36-bit bidirectional data port for side B.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. $\overline{EFA}$, $\overline{FFA}$, $\overline{AFA}$, and $\overline{AEA}$ are synchronized to the low-to-high transition of CLKA.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. $\overline{EFB}$, $\overline{FFB}$, $\overline{AFB}$, and $\overline{AEB}$ are synchronized to the low-to-high transition of CLKB.
$\overline{CSA}$	I	Port-A chip select. $\overline{CSA}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{CSA}$ is high.
$\overline{CSB}$	I	Port-B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{CSB}$ is high.
$\overline{EFA}$	O (port A)	Port-A empty flag. $\overline{EFA}$ is synchronized to the low-to-high transition of CLKA. When $\overline{EFA}$ is low, FIFO2 is empty and reads from its memory are disabled. Data can be read from FIFO2 to the output register when $\overline{EFA}$ is high. $\overline{EFA}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKA after data is loaded into empty FIFO2 memory.
$\overline{EFB}$	O (port B)	Port-B empty flag. $\overline{EFB}$ is synchronized to the low-to-high transition of CLKB. When $\overline{EFB}$ is low, FIFO1 is empty and reads from its memory are disabled. Data can be read from FIFO1 to the output register when $\overline{EFB}$ is high. $\overline{EFB}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKB after data is loaded into empty FIFO1 memory.
ENA	I	Port-A enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port-B enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
$\overline{FFA}$	O (port A)	Port-A full flag. $\overline{FFA}$ is synchronized to the low-to-high transition of CLKA. When $\overline{FFA}$ is low, FIFO1 is full and writes to its memory are disabled. $\overline{FFA}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKA after reset.
$\overline{FFB}$	O (port B)	Port-B full flag. $\overline{FFB}$ is synchronized to the low-to-high transition of CLKB. When $\overline{FFB}$ is low, FIFO2 is full and writes to its memory are disabled. $\overline{FFB}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKB after reset.
FS1, FS0	I	Flag offset selects. The low-to-high transition of $\overline{RST}$ latches the values of FS0 and FS1, which selects one of four preset values for the almost-empty flag and almost-full flag offset.
MBA	I	Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation. When the A0–A35 outputs are active, a high level on MBA selects data from the mail2 register for output and a low level selects FIFO2 output register data for output.
MBB	I	Port-B mailbox select. A high level on MBB chooses a mailbox register for a port-B read or write operation. When the B0–B35 outputs are active, a high level on MBB selects data from the mail1 register for output and a low level selects FIFO1 output register data for output.
$\overline{MBF1}$	O	Mail1 register flag. $\overline{MBF1}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is low. $\overline{MBF1}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and MBB is high. $\overline{MBF1}$ is set high when the device is reset.

Terminal Functions (Continued)

PIN NAME	I/O	DESCRIPTION
$\overline{MBF2}$	O	Mail2 register flag. $\overline{MBF2}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is low. $\overline{MBF2}$ is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. $\overline{MBF2}$ is set high when the device is reset.
ODD/$\overline{EVEN}$	I	Odd/even parity select. Odd parity is checked on each port when ODD/$\overline{EVEN}$ is high, and even parity is checked when ODD/$\overline{EVEN}$ is low. ODD/$\overline{EVEN}$ also selects the type of parity generated for each port if parity generation is enabled for a read operation.
$\overline{PEFA}$	O (port A)	Port-A parity error flag. When any byte applied to terminals A0–A35 fails parity, $\overline{PEFA}$ is low. Bytes are organized as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/$\overline{EVEN}$ input. The parity trees used to check the A0–A35 inputs are shared by the mail2 register to generate parity if parity generation is selected by PGA. Therefore, if a mail2 read with parity generation is setup by having W/$\overline{RA}$ low, MBA high, and PGA high, the $\overline{PEFA}$ flag is forced high regardless of the state of the A0–A35 inputs.
$\overline{PEFB}$	O (port B)	Port-B parity error flag. When any byte applied to terminals B0–B35 fails parity, $\overline{PEFB}$ is low. Bytes are organized as B0–B8, B9–B17, B18–B26, and B27–B35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/$\overline{EVEN}$ input. The parity trees used to check the B0–B35 inputs are shared by the mail1 register to generate parity if parity generation is selected by PGB. Therefore, if a mail1 read with parity generation is setup by having W/$\overline{RB}$ low, MBB high, and PGB high, the $\overline{PEFB}$ flag is forced high regardless of the state of the B0–B35 inputs.
PGA	I	Port-A parity generation. Parity is generated for data reads from port A when PGA is high. The type of parity generated is selected by the state of the ODD/$\overline{EVEN}$ input. Bytes are organized as A0–A8, A9–A17, A18–A26, and A27–A35. The generated parity bits are output in the most significant bit of each byte.
PGB	I	Port-B parity generation. Parity is generated for data reads from port B when PGB is high. The type of parity generated is selected by the state of the ODD/$\overline{EVEN}$ input. Bytes are organized as B0–B8, B9–B17, B18–B26, and B27–B35. The generated parity bits are output in the most significant bit of each byte.
$\overline{RST}$	I	Reset. To reset the device, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RST}$ is low. This sets the $\overline{AFA}$, $\overline{AFB}$, $\overline{MBF1}$, and $\overline{MBF2}$ flags high and the $\overline{EFA}$, $\overline{EFB}$, $\overline{AEA}$, $\overline{AEB}$, $\overline{FFA}$, and $\overline{FFB}$ flags low. The low-to-high transition of $\overline{RST}$ latches the status of the FS1 and FS0 inputs to select almost-full flag and almost-empty flag offset.
W/$\overline{RA}$	I	Port-A write/read select. W/$\overline{RA}$ high selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{RA}$ is high.
W/$\overline{RB}$	I	Port-B write/read select. W/$\overline{RB}$ high selects a write operation and a low selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when W/$\overline{RB}$ is high.

detailed description

reset

The SN74ABT3612 is reset by taking the reset ($\overline{RST}$) input low for at least four port-A clock (CLKA) and four port-B clock (CLKB) low-to-high transitions. The reset input can switch asynchronously to the clocks. A device reset initializes the internal read and write pointers of each FIFO and forces the full flags ($\overline{FFA}$, $\overline{FFB}$) low, the empty flags ($\overline{EFA}$, $\overline{EFB}$) low, the almost-empty flags ($\overline{AEA}$, $\overline{AEB}$) low, and the almost-full flags ($\overline{AFA}$, $\overline{AFB}$) high. A reset also forces the mailbox flags ($\overline{MBF1}$, $\overline{MBF2}$) high. After a reset, $\overline{FFA}$ is set high after two low-to-high transitions of CLKA and $\overline{FFB}$ is set high after two low-to-high transitions of CLKB. The device must be reset after power up before data is written to its memory.

A low-to-high transition on the $\overline{RST}$ input loads the almost-full and almost-empty offset register (X) with the value selected by the flag-select (FS0, FS1) inputs. The values that can be loaded into the register are shown in Table 1.

reset (continued)

Table 1. Flag Programming

FS1	FS0	$\overline{RST}$	ALMOST-FULL AND ALMOST-EMPTY FLAG OFFSET REGISTER (X)
H	H	↑	16
H	L	↑	12
L	H	↑	8
L	L	↑	4

FIFO write/read operation

The state of the port-A data (A0–A35) outputs is controlled by the port-A chip select ($\overline{CSA}$) and the port-A write/read select (W/$\overline{RA}$). The A0–A35 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is high. The A0–A35 outputs are active when both $\overline{CSA}$ and W/$\overline{RA}$ are low. Data is loaded into FIFO1 from the A0–A35 inputs on a low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is high, ENA is high, MBA is low, and $\overline{FFA}$ is high. Data is read from FIFO2 to the A0–A35 outputs by a low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is low, ENA is high, MBA is low, and $\overline{EFA}$ is high (see Table 2).

Table 2. Port-A Enable Function Table

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	A0–A35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO1 write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, FIFO2 output register	None
L	L	H	L	↑	Active, FIFO2 output register	FIFO2 read
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set $\overline{MBF2}$ high)

The port-B control signals are identical to those of port A. The state of the port-B data (B0–B35) outputs is controlled by the port-B chip select ($\overline{CSB}$) and the port-B write/read select (W/$\overline{RB}$). The B0–B35 outputs are in the high-impedance state when either $\overline{CSB}$ or W/$\overline{RB}$ is high. The B0–B35 outputs are active when both $\overline{CSB}$ and W/$\overline{RB}$ are low.

Data is loaded into FIFO2 from the B0–B35 inputs on a low-to-high transition of CLKB when $\overline{CSB}$ is low, W/$\overline{RB}$ is high, ENB is high, MBB is low, and $\overline{FFB}$ is high. Data is read from FIFO1 to the B0–B35 outputs by a low-to-high transition of CLKB when $\overline{CSB}$ is low, W/$\overline{RB}$ is low, ENB is high, MBB is high, and $\overline{EFB}$ is high (see Table 3).

The setup and hold time constraints to the port clocks for the port chip selects ($\overline{CSA}$, $\overline{CSB}$) and write/read selects (W/$\overline{RA}$, W/$\overline{RB}$) are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is low during a clock cycle, the port chip select and write/read select may change states during the setup and hold time window of the cycle.

FIFO write/read operation (continued)

Table 3. Port-B Enable Function Table

$\overline{CSB}$	W/$\overline{RB}$	ENB	MBB	CLKB	B0–B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO2 write
L	H	H	H	↑	In high-impedance state	Mail2 write
L	L	L	L	X	Active, FIFO1 output register	None
L	L	H	L	↑	Active, FIFO1 output register	FIFO1 read
L	L	L	H	X	Active, mail1 register	None
L	L	H	H	↑	Active, mail1 register	Mail1 read (set $\overline{MBF1}$ high)

synchronized FIFO flags

Each FIFO is synchronized to its port clock through two flip-flop stages. This is done to improve flag reliability by reducing the probability of metastable events on the output when CLKA and CLKB operate asynchronously to one another (see the application report *Metastability Performance of Clocked FIFOs* in the 1994 *High-Performance FIFO Memories Data Book*, literature #SCAD003B). $\overline{EFA}$, $\overline{AEA}$, $\overline{FFA}$, and $\overline{AFA}$ are synchronized to CLKA. $\overline{EFB}$, $\overline{AEB}$, $\overline{FFB}$, and $\overline{AFB}$ are synchronized to CLKB. Tables 4 and 5 show the relationship of each port flag to FIFO1 and FIFO2.

Table 4. FIFO1 Flag Operation

NUMBER OF WORDS IN FIFO1†	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA	
	$\overline{EFB}$	$\overline{AEB}$	$\overline{AFA}$	$\overline{FFA}$
0	L	L	H	H
1 to X	H	L	H	H
(X +1) to [64 – (X +1)]	H	H	H	H
(64 – X) to 63	H	H	L	H
64	H	H	L	L

† X is the value in the almost-empty flag and almost-full flag offset register.

Table 5. FIFO2 Flag Operation

NUMBER OF WORDS IN FIFO2†	SYNCHRONIZED TO CLKA		SYNCHRONIZED TO CLKB	
	$\overline{EFA}$	$\overline{AEA}$	$\overline{AFB}$	$\overline{FFB}$
0	L	L	H	H
1 to X	H	L	H	H
(X +1) to [64 – (X +1)]	H	H	H	H
(64 – X) to 63	H	H	L	H
64	H	H	L	L

† X is the value in the almost-empty flag and almost-full flag offset register.

empty flags ($\overline{EFA}$, $\overline{EFB}$)

The empty flag of a FIFO is synchronized to the port clock that reads data from its array. When the empty flag is high, new data can be read to the FIFO output register. When the empty flag is low, the FIFO is empty and attempted FIFO reads are ignored.

The read pointer of a FIFO is incremented each time a new word is clocked to the output register. The state machine that controls an empty flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. A word written to a FIFO can be read to the FIFO output register in a minimum of three cycles of the empty flag synchronizing clock; therefore, an empty flag is low if a word in memory is the next data to be sent to the FIFO output register and two cycles of the port clock that reads data from the FIFO have not elapsed since the time the word was written. The empty flag of the FIFO is set high by the second low-to-high transition of the synchronizing clock, and the new data word can be read to the FIFO output register in the following cycle.

A low-to-high transition on an empty flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{sk1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 6 and 7).

full flags ($\overline{FFA}$, $\overline{FFB}$)

The full flag of a FIFO is synchronized to the port clock that writes data to its array. When the full flag is high, a memory location is free in the SRAM to receive new data. No memory locations are free when the full flag is low and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, the write pointer is incremented. The state machine that controls the full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is full, full–1, or full–2. From the time a word is read from a FIFO, the previous memory location is ready to be written in a minimum of three cycles of the full flag synchronizing clock; therefore, a full flag is low if less than two cycles of the full flag synchronizing clock have elapsed since the next memory write location has been read. The second low-to-high transition on the full flag synchronizing clock after the read sets the full flag high and data can be written in the following clock cycle.

A low-to-high transition on a full flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{sk1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 8 and 9).

almost-empty flags ($\overline{AEA}$, $\overline{AEB}$)

The almost-empty flag of a FIFO is synchronized to the port clock that reads data from its array. The state machine that controls an almost-empty flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see reset). An almost-empty flag is low when the FIFO contains X or less words in memory and is high when the FIFO contains (X + 1) or more words.

Two low-to-high transitions of the almost-empty flag synchronizing clock are required after a FIFO write for the almost-empty flag to reflect the new level of fill; therefore, the almost-empty flag of a FIFO containing (X + 1) or more words remains low if two cycles of the synchronizing clock have not elapsed since the write that filled the memory to the (X + 1) level. An almost-empty flag is set high by the second low-to-high transition of the synchronizing clock after the FIFO write that fills memory to the (X + 1) level. A low-to-high transition of an almost-empty flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the write that fills the FIFO to (X + 1) words. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figures 11 and 12).

almost-full flags ($\overline{AFA}$, $\overline{AFB}$)

The almost-full flag of a FIFO is synchronized to the port clock that writes data to its array. The state machine that controls an almost-full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost full, almost full–1, or almost full–2. The almost-full state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see reset). An almost-full flag is low when the FIFO contains (64 – X) or more words in memory and is high when the FIFO contains [64 – (X + 1)] or less words.

Two low-to-high transitions of the almost-full flag synchronizing clock are required after a FIFO read for the almost-full flag to reflect the new level of fill; therefore, the almost-full flag of a FIFO containing [64 – (X + 1)] or less words remains low if two cycles of the synchronizing clock have not elapsed since the read that reduced the number of words in memory to [64 – (X + 1)]. An almost-full flag is set high by the second low-to-high transition of the synchronizing clock after the FIFO read that reduces the number of words in memory to [64 – (X + 1)]. A low-to-high transition of an almost-full flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the read that reduces the number of words in memory to [64 – (X + 1)]. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figures 13 and 14).

mailbox registers

Each FIFO has a 36-bit bypass register to pass command and control information between port A and port B without putting it in queue. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A low-to-high transition on CLKA writes A0–A35 data to the mail1 register when a port-A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and MBA is high. A low-to-high transition on CLKB writes B0–B35 data to the mail2 register when a port-B write is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB and MBB is high. Writing data to a mail register sets the corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) low. Attempted writes to a mail register are ignored while the mail flag is low.

When a port's data outputs are active, the data on the bus comes from the FIFO output register when the port mailbox-select input (MBA, MBB) is low and from the mail register when the port mailbox-select input is high. The mail1 register flag ($\overline{MBF1}$) is set high by a low-to-high transition on CLKB when a port-B read is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB and MBB is high. The mail2 register flag ($\overline{MBF2}$) is set high by a low-to-high transition on CLKA when a port-A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and MBA is high. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

parity checking

The port-A inputs (A0–A35) and port-B inputs (B0–B35) each have four parity trees to check the parity of incoming (or outgoing) data. A parity failure on one or more bytes of the input bus is reported by a low level on the port parity error flag ($\overline{PEFA}$, $\overline{PEFB}$). Odd or even parity checking can be selected, and the parity error flags can be ignored if this feature is not desired.

Parity status is checked on each input bus according to the level of the odd/even parity (ODD/$\overline{EVEN}$) select input. A parity error on one or more bytes of a port is reported by a low level on the corresponding port parity error flag ($\overline{PEFA}$, $\overline{PEFB}$) output. Port-A bytes are arranged as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit of each byte used as the parity bit. Port-B bytes are arranged as B0–B8, B9–B17, B18–B26, and B27–B35, with the most significant bit of each byte used as the parity bit. When odd/even parity is selected, a port parity error flag ($\overline{PEFA}$, $\overline{PEFB}$) is low if any byte on the port has an odd/even number of low levels applied to the bits.

parity checking (continued)

The four parity trees used to check the A0–A35 inputs are shared by the mail2 register when parity generation is selected for port-A reads (PGA = high). When a port-A read from the mail2 register with parity generation is selected with W/$\overline{R}$A low, $\overline{CSA}$ low, ENA high, MBA high, and PGA high, the port-A parity error flag ($\overline{PEFA}$) is held high regardless of the levels applied to the A0–A35 inputs. Likewise, the parity trees used to check the B0–B35 inputs are shared by the mail1 register when parity generation is selected for port-B reads (PGB = high). When a port-B read from the mail1 register with parity generation is selected with W/$\overline{R}$B low, $\overline{CSB}$ low, ENB high, MBB high, and PGB high, the port-B parity error flag ($\overline{PEFB}$) is held high regardless of the levels applied to the B0–B35 inputs.

parity generation

A high level on the port-A parity generate select (PGA) or port-B parity generate select (PGB) enables the SN74ABT3612 to generate parity bits for port reads from a FIFO or mailbox register. Port-A bytes are arranged as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit of each byte used as the parity bit. Port-B bytes are arranged as B0–B8, B9–B17, B18–B26, and B27–B35, with the most significant bit of each byte used as the parity bit. A write to a FIFO or mail register stores the levels applied to all thirty-six inputs regardless of the state of the parity generate select (PGA, PGB) inputs. When data is read from a port with parity generation selected, the lower eight bits of each byte are used to generate a parity bit according to the level on the ODD/$\overline{EVEN}$ select. The generated parity bits are substituted for the levels originally written to the most significant bits of each byte as the word is read to the data outputs.

Parity bits for FIFO data are generated after the data is read from SRAM and before the data is written to the output register. Therefore, the port-A parity generate select (PGA) and odd/even parity select (ODD/$\overline{EVEN}$) have setup and hold time constraints to the port-A clock (CLKA) and the port-B parity generate select (PGB) and ODD/$\overline{EVEN}$ have setup and hold-time constraints to the port-B clock (CLKB). These timing constraints only apply for a rising clock edge used to read a new word to the FIFO output register.

The circuit used to generate parity for the mail1 data is shared by the port-B bus (B0–B35) to check parity and the circuit used to generate parity for the mail2 data is shared by the port-A bus (A0–A35) to check parity. The shared parity trees of a port are used to generate parity bits for the data in a mail register when the port write/read select (W/$\overline{R}$A, W/$\overline{R}$B) input is low, the port mail select (MBA, MBB) input is high, chip select ($\overline{CSA}$, $\overline{CSB}$) is low, enable (ENA, ENB) is high, and port parity generate select (PGA, PGB) is high. Generating parity for mail-register data does not change the contents of the register.

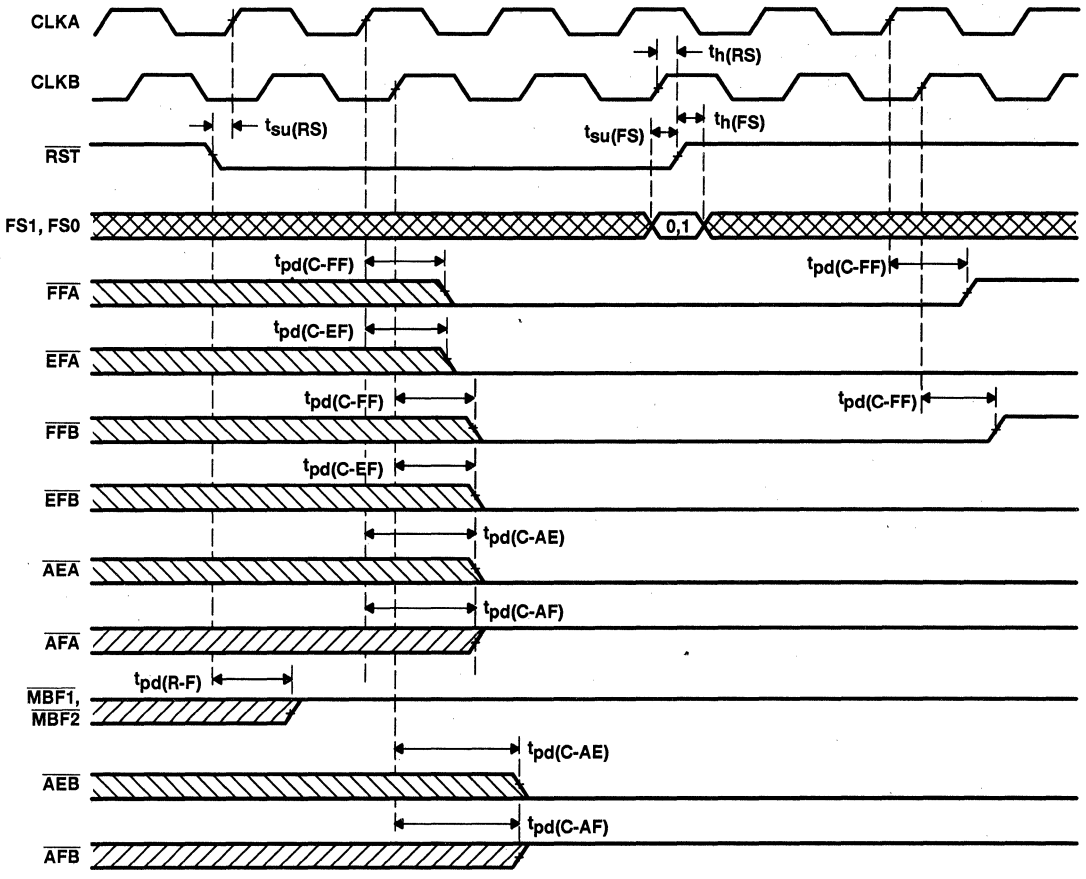
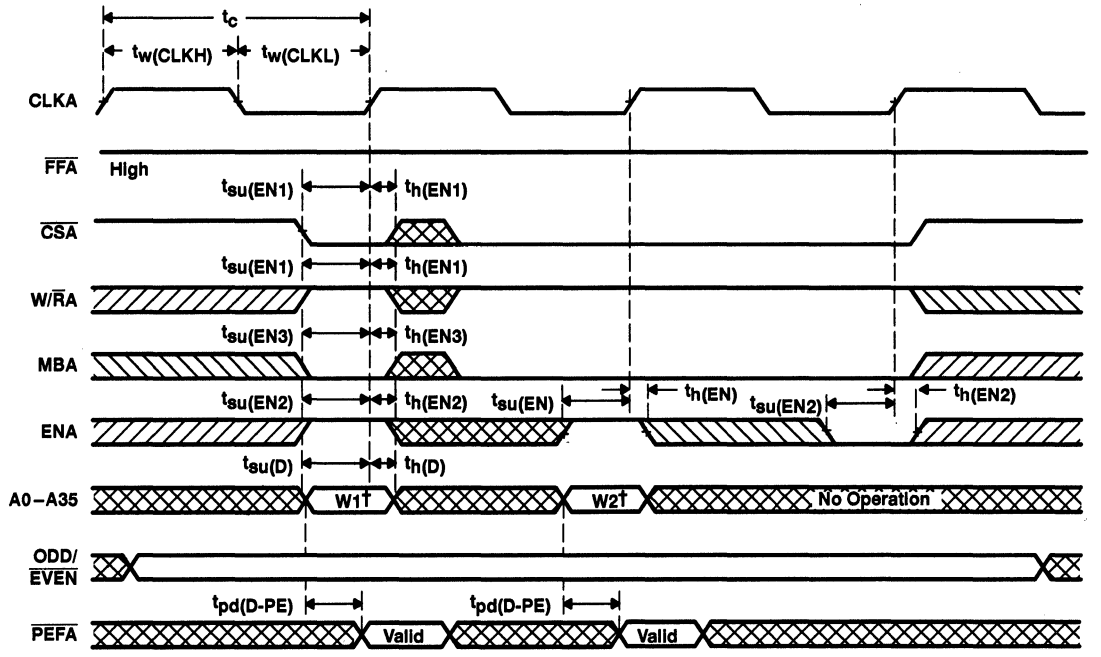
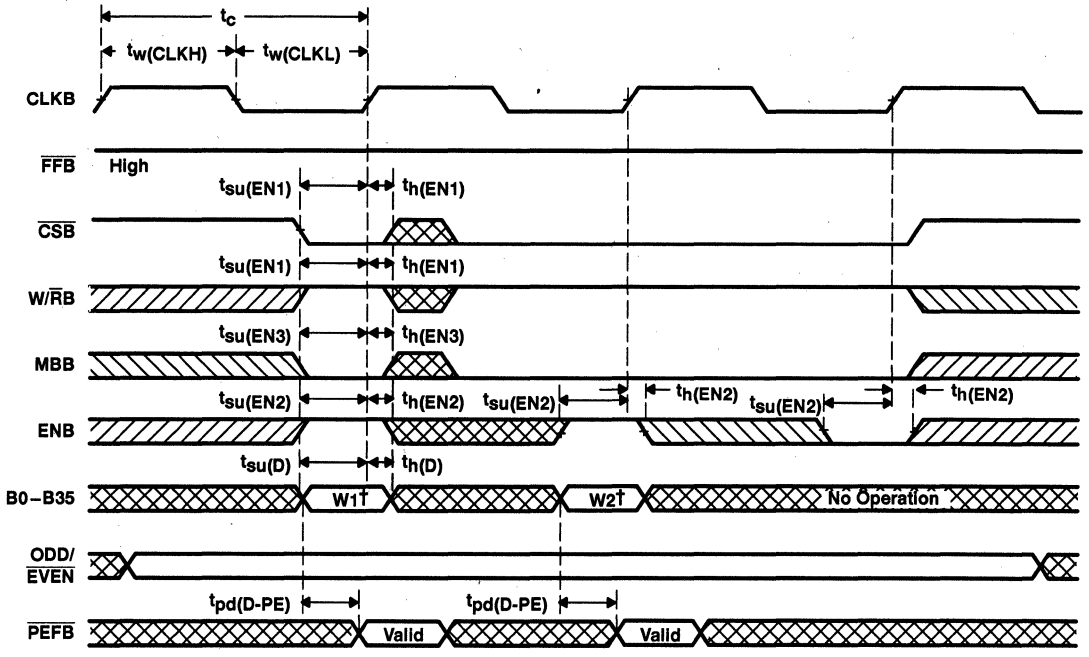


Figure 1. Device Reset Loading the X Register With the Value of Eight



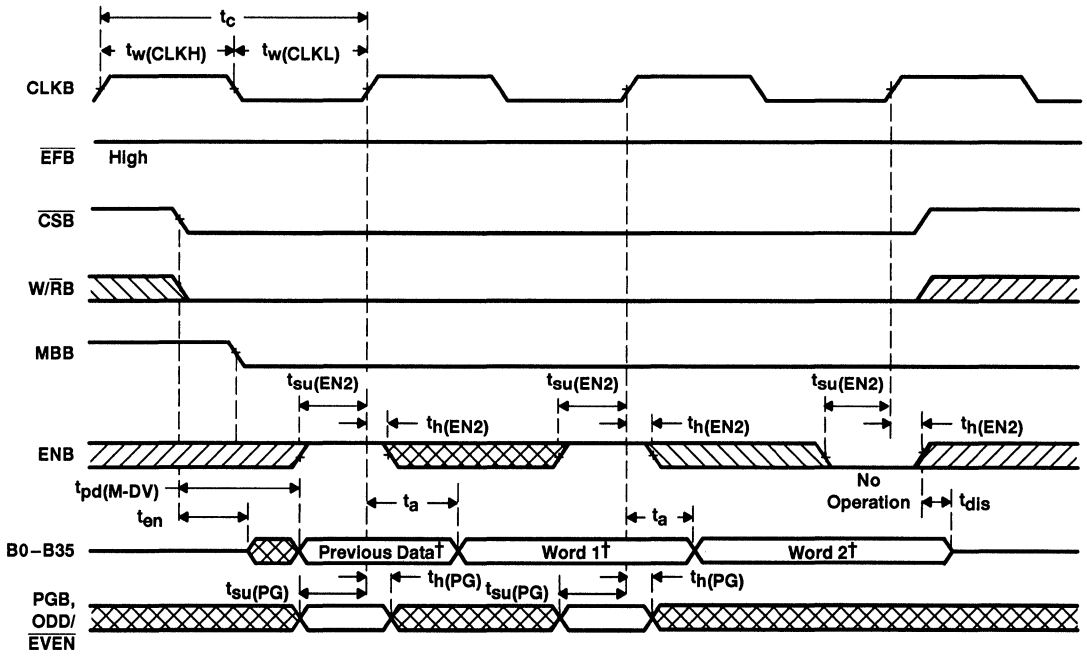
† Written to FIFO1

Figure 2. Port-A Write-Cycle Timing for FIFO1



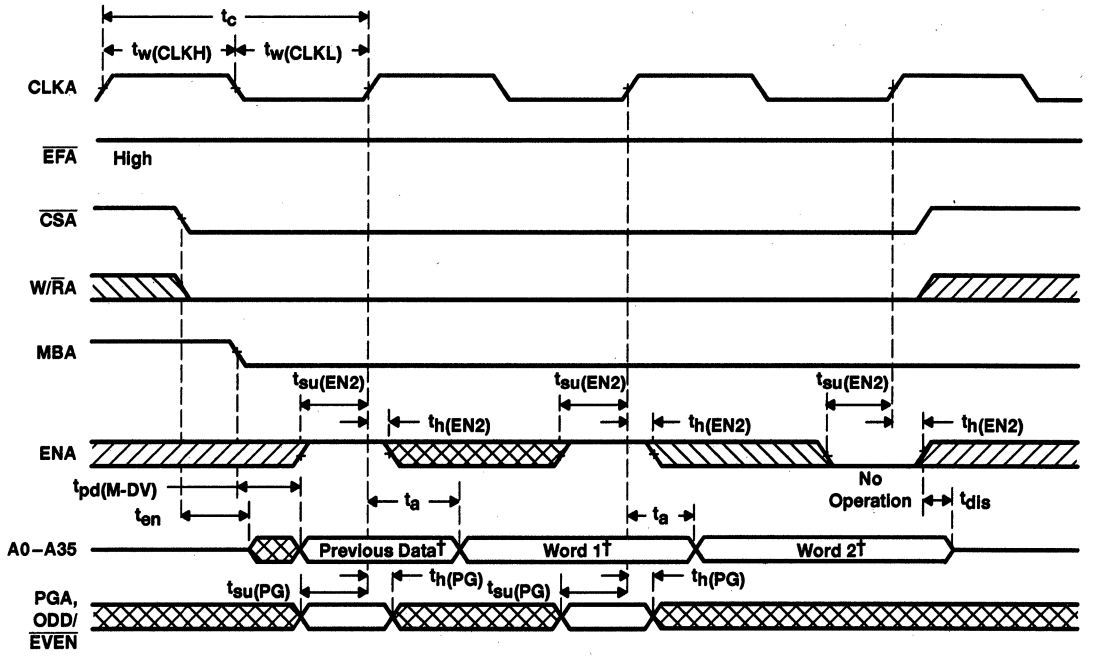
† Written to FIFO2

Figure 3. Port-B Write-Cycle Timing for FIFO2



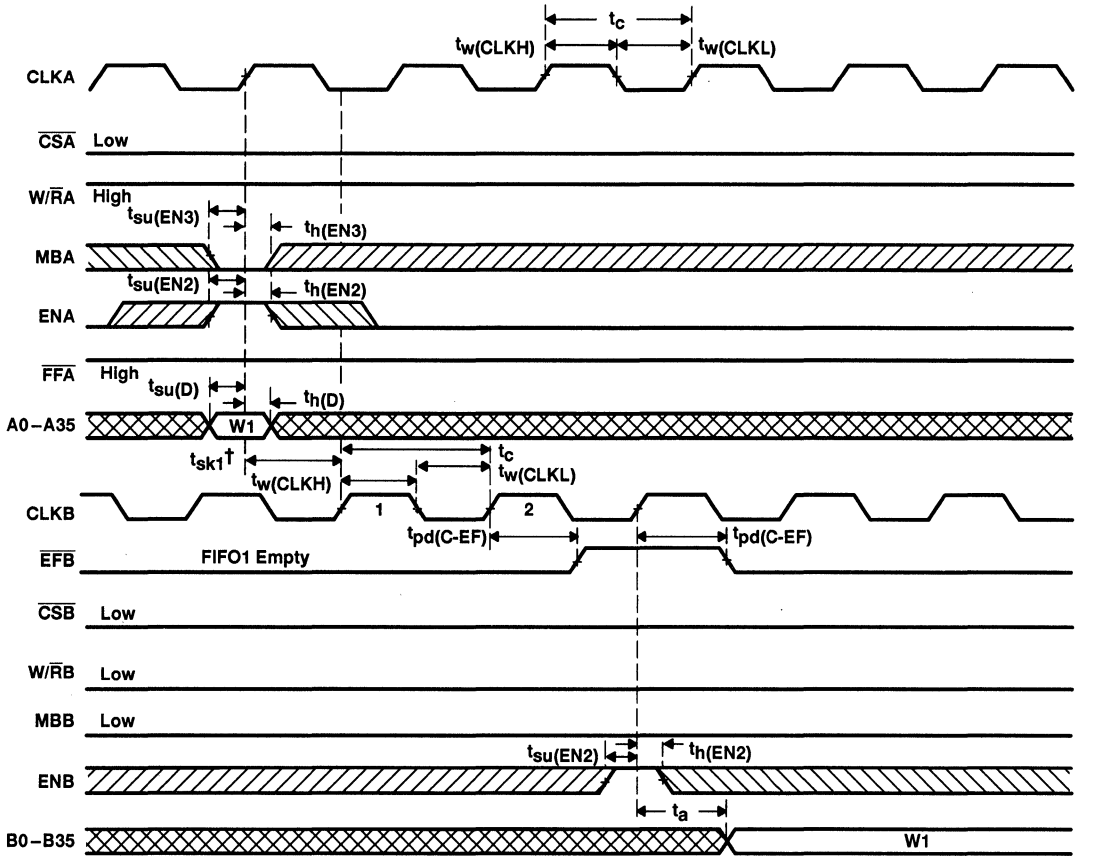
† Read from FIFO1

Figure 4. Port-B Read-Cycle Timing for FIFO1



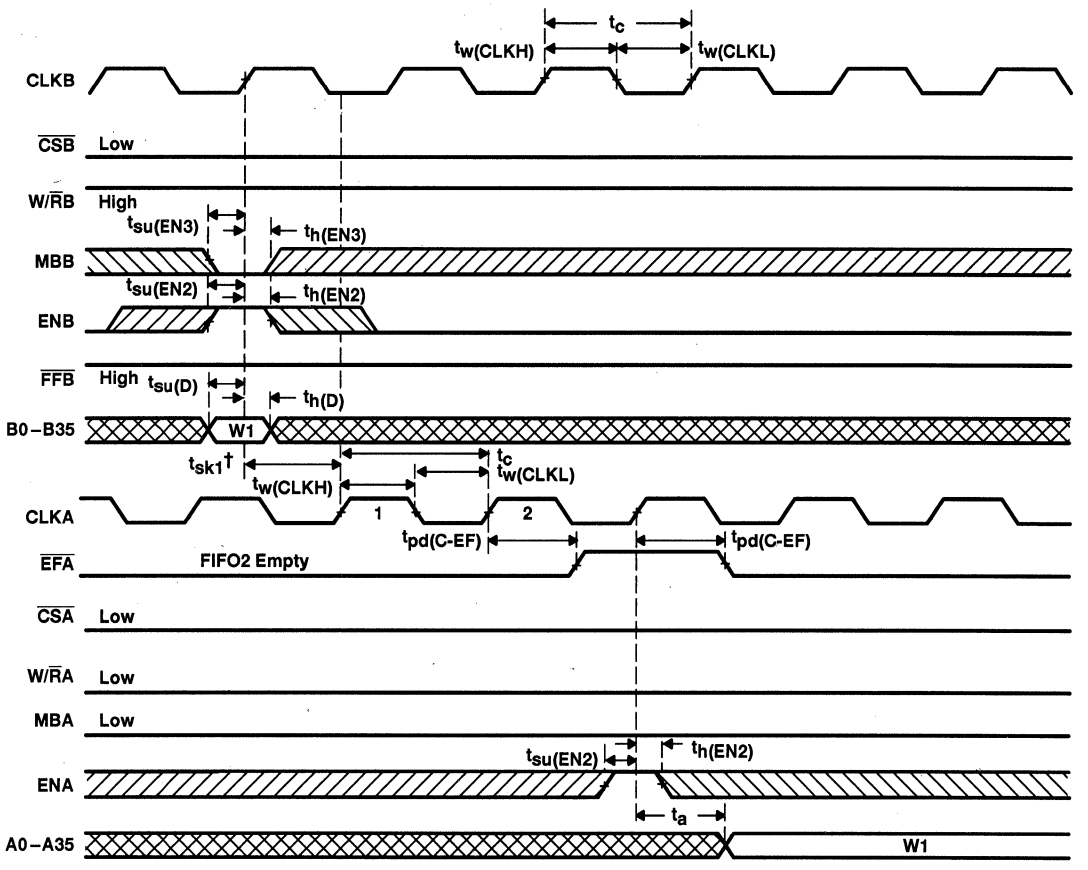
† Read from FIFO2

Figure 5. Port-A Read-Cycle Timing for FIFO2



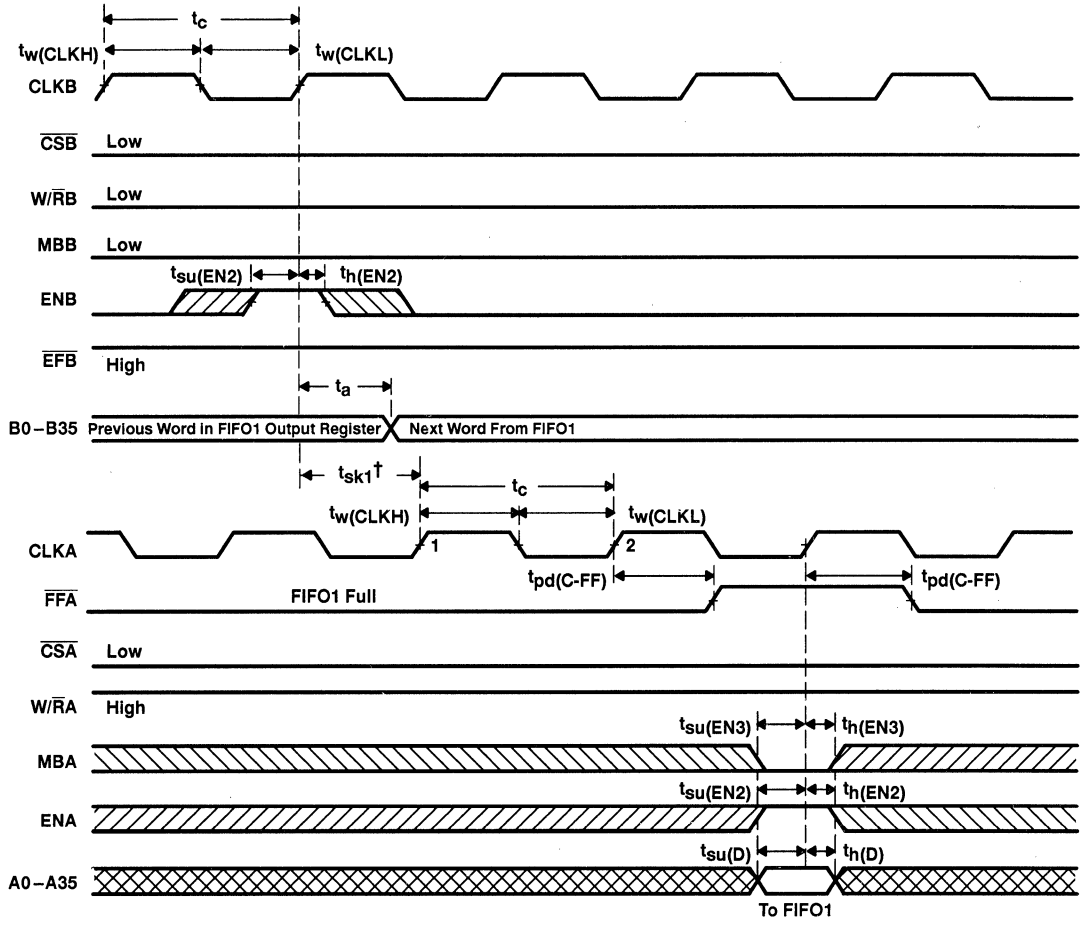
† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EFB}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, the transition of $\overline{EFB}$ high may occur one CLKB cycle later than shown.

Figure 6. $\overline{EFB}$-Flag Timing and First Data Read When FIFO1 Is Empty



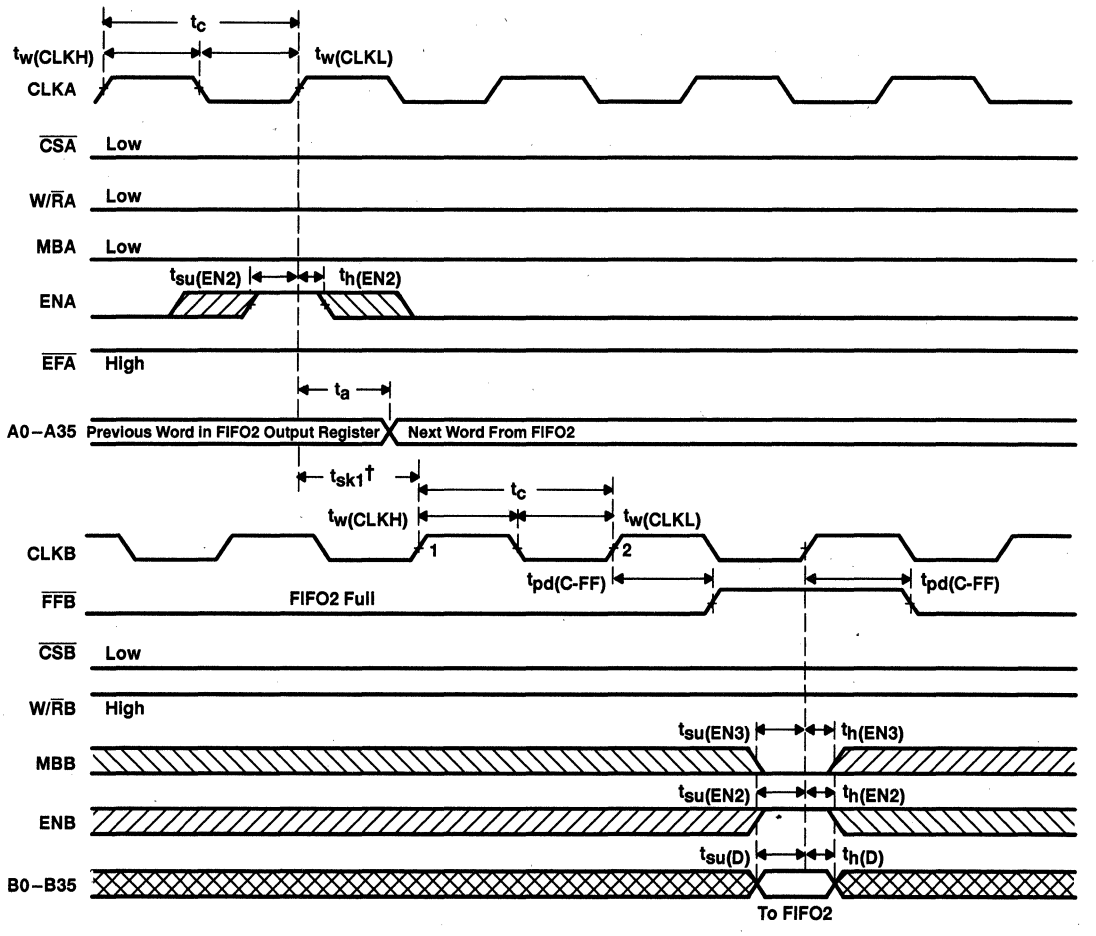
† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{EFA}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, the transition of $\overline{EFA}$ high may occur one CLKA cycle later than shown.

Figure 7. $\overline{EFA}$-Flag Timing and First Data Read When FIFO2 Is Empty



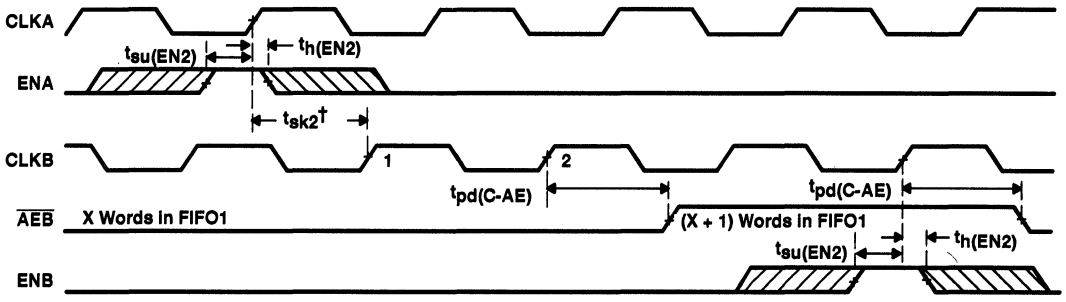
† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{FFA}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, $\overline{FFA}$ may transition high one CLKA cycle later than shown.

Figure 8. $\overline{FFA}$-Flag Timing and First Available Write When FIFO1 Is Full



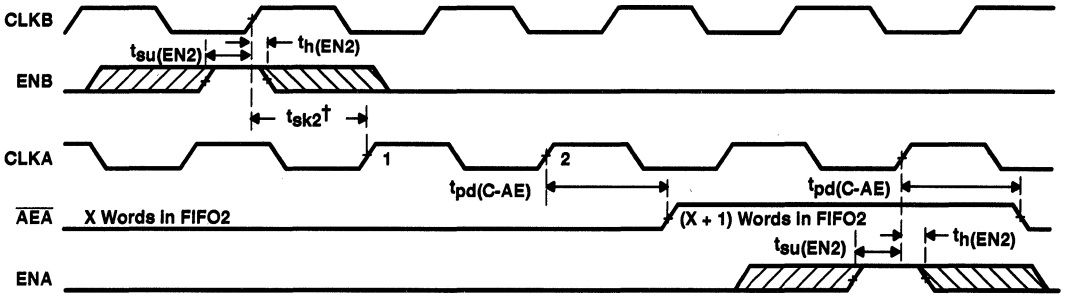
† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{FFB}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, $\overline{FFB}$ may transition high one CLKB cycle later than shown.

Figure 9. $\overline{FFB}$-Flag Timing and First Available Write When FIFO2 Is Full



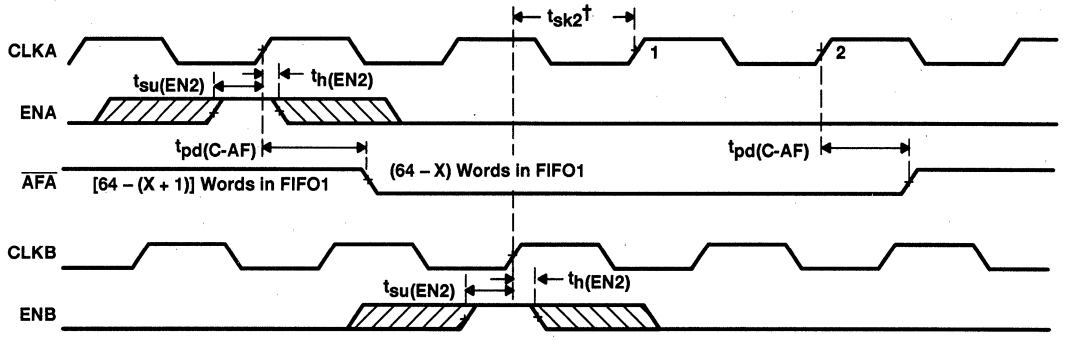
† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AEB}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, $\overline{AEB}$ may transition high one CLKB cycle later than shown.
NOTE A: FIFO1 write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO1 read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L).

Figure 10. Timing for $\overline{AEB}$ When FIFO1 Is Almost Empty



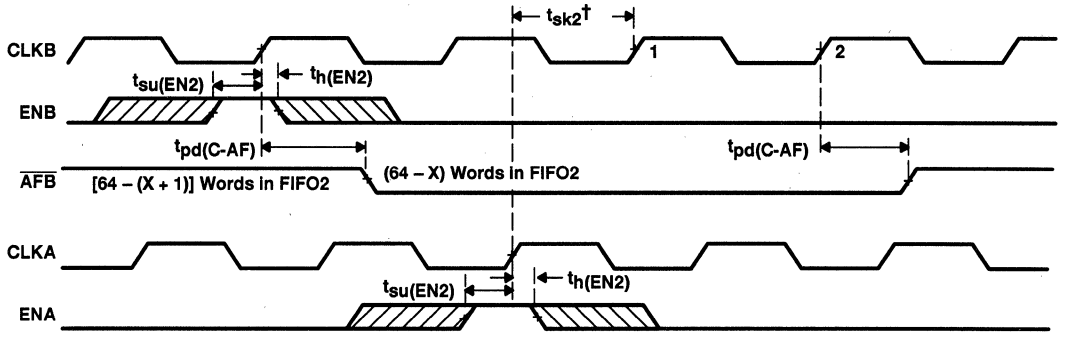
† t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AEA}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, $\overline{AEA}$ may transition high one CLKA cycle later than shown.
NOTE A: FIFO2 write ($\overline{CSB}$ = L, W/$\overline{RB}$ = H, MBB = L), FIFO2 read ($\overline{CSA}$ = L, W/$\overline{RA}$ = L, MBA = L).

Figure 11. Timing for $\overline{AEA}$ When FIFO2 Is Almost Empty



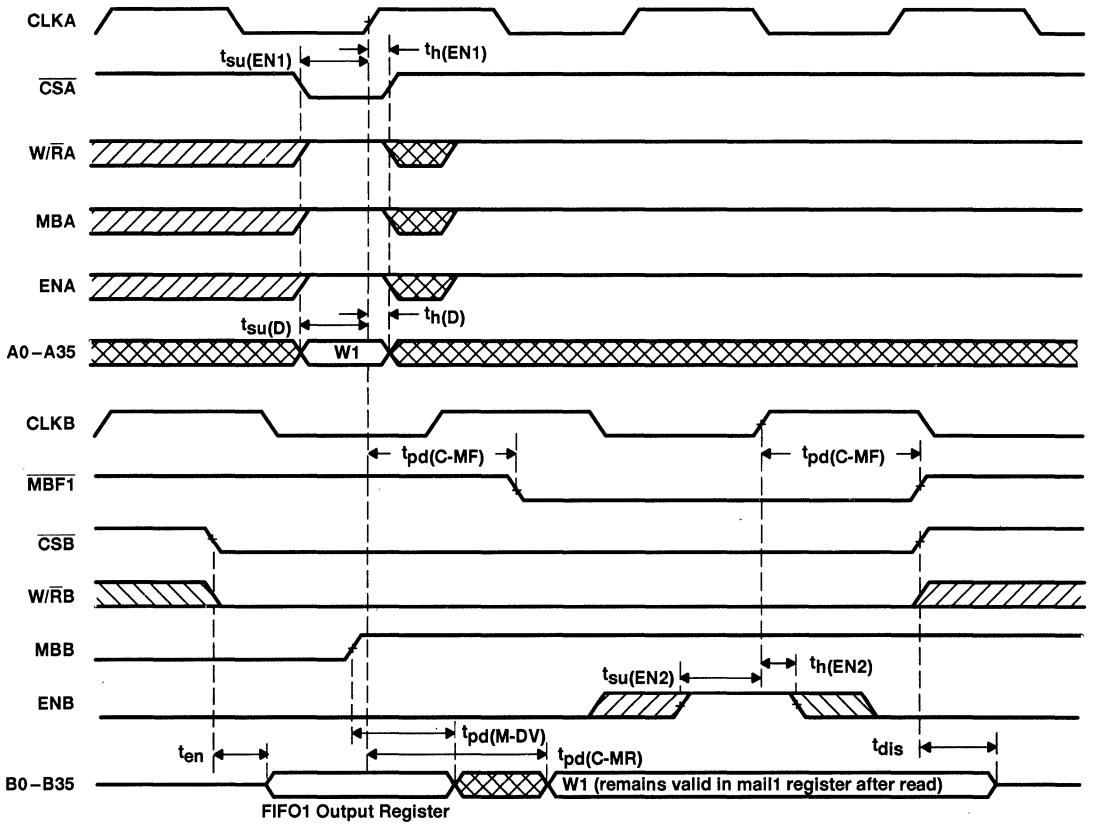
† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AFA}$ to transition high in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, $\overline{AFA}$ may transition high one CLKB cycle later than shown.
NOTE A: FIFO1 write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO1 read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L).

Figure 12. Timing for $\overline{AFA}$ When FIFO1 Is Almost Full



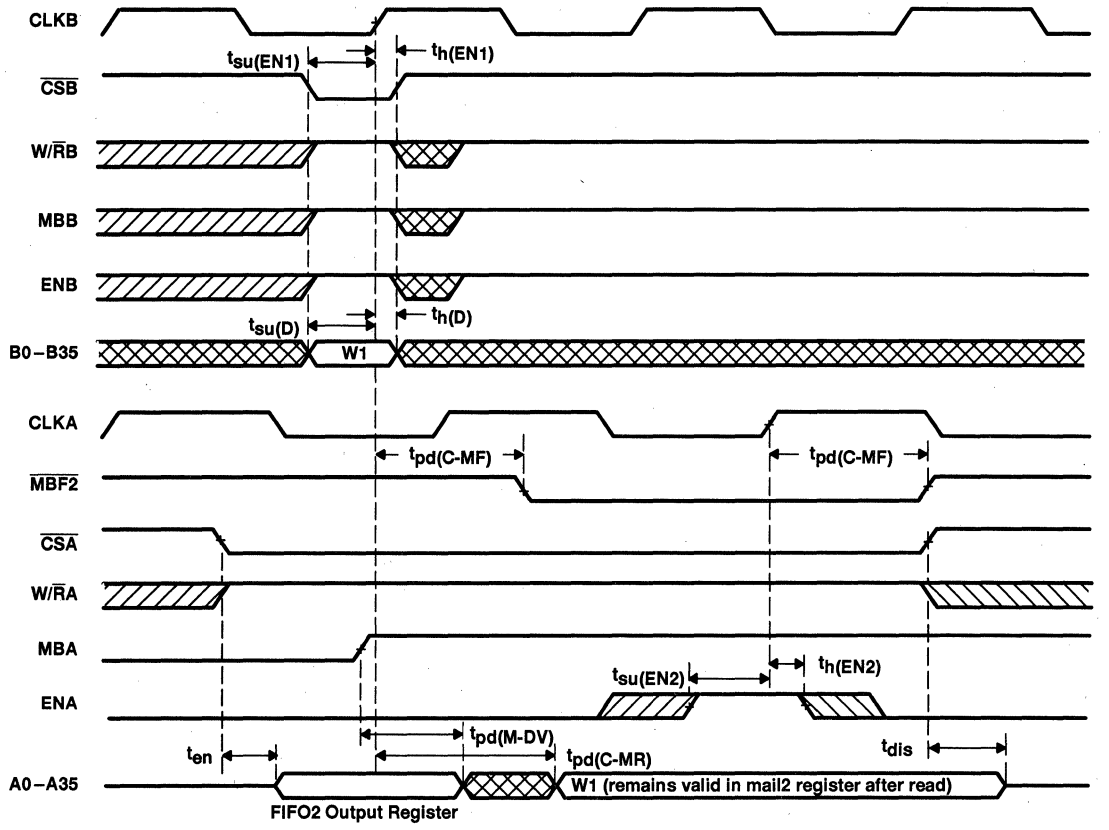
† t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AFB}$ to transition high in the next CLKB cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, $\overline{AFB}$ may transition high one CLKA cycle later than shown.
NOTE A: FIFO2 write ($\overline{CSB}$ = L, W/$\overline{RB}$= H, MBB = L), FIFO2 read ($\overline{CSA}$ = L, W/$\overline{RA}$ = L, MBA = L).

Figure 13. Timing for $\overline{AFB}$ When FIFO2 Is Almost Full



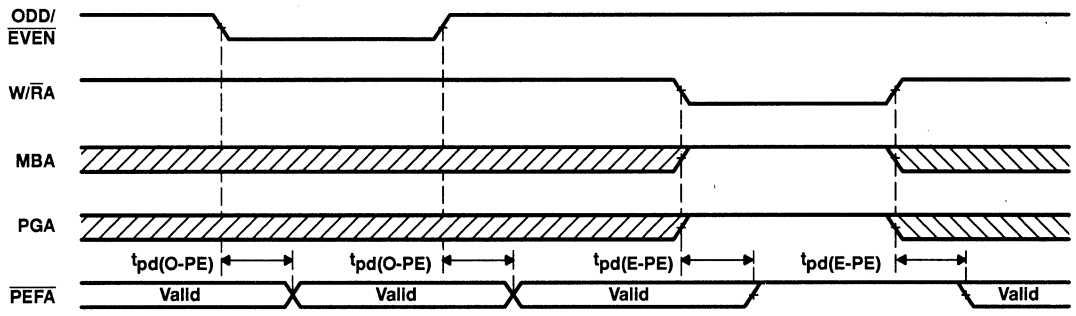
NOTE A: Port-B parity generation off (PGB = L)

Figure 14. Timing for Mail1 Register and $\overline{\text{MBF1}}$ Flag



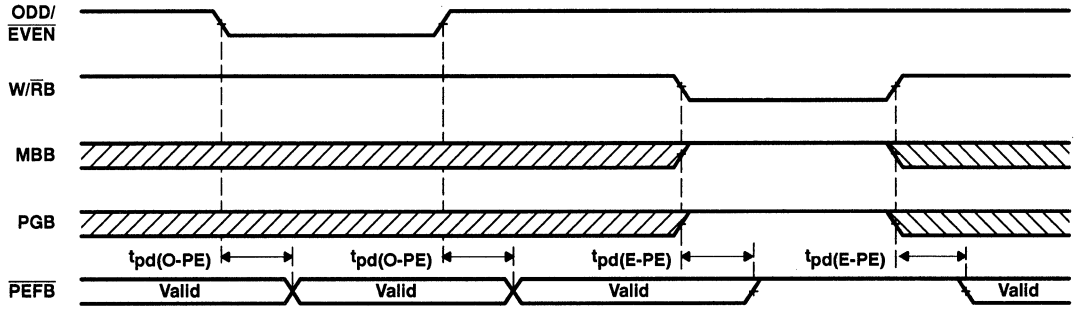
NOTE A: Port-A parity generation off (PGA = L)

Figure 15. Timing for Mail2 Register and $\overline{\text{MBF2}}$ Flag



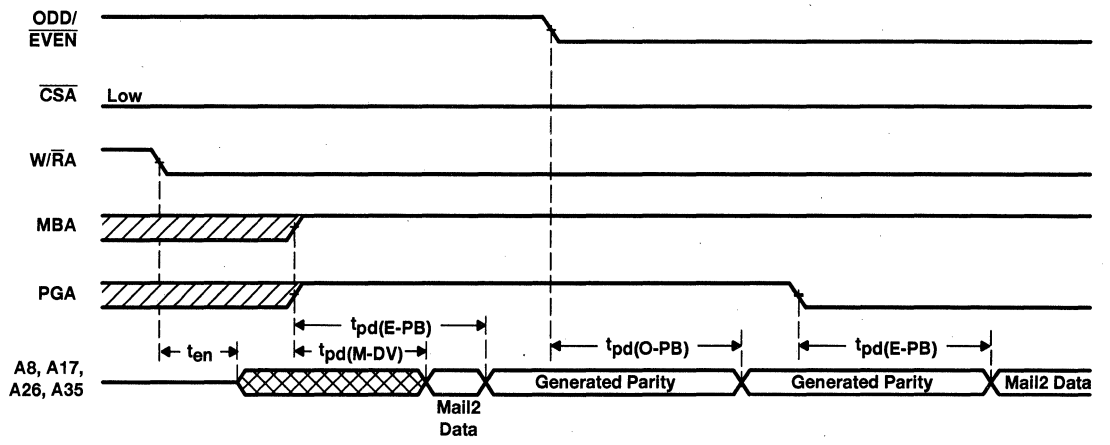
NOTE A: ENA is high and $\overline{CSA}$ is low.

Figure 16. ODD/$\overline{EVEN}$, W/$\overline{RA}$, MBA, and PGA to $\overline{PEFA}$ Timing



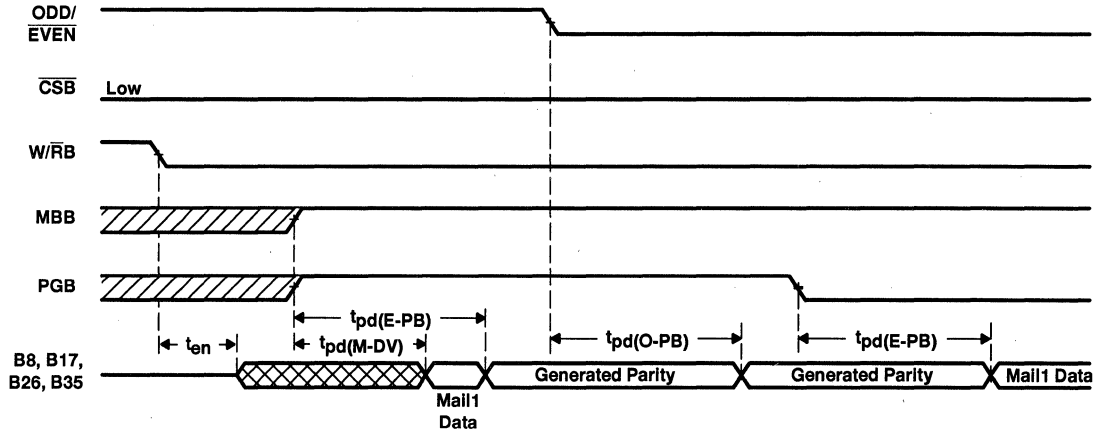
NOTE A: ENB is high and $\overline{CSB}$ is low.

Figure 17. ODD/$\overline{EVEN}$, W/$\overline{RB}$, MBB, and PGB to $\overline{PEFB}$ Timing



NOTE A: ENA is high.

Figure 18. Parity-Generation Timing When Reading From the Mail2 Register



NOTE A: ENB is high.

Figure 19. Parity-Generation Timing When Reading From the Mail1 Register

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±500 mA
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−4	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS				MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −4 mA			2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0					±50	µA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0					±50	µA
I_{CC}	V_{CC} = 5.5 V,	I_O = 0 mA,	V_I = V_{CC} or GND	Outputs high			60	mA
				Outputs low			130	mA
				Outputs disabled			60	mA
C_i	V_I = 0,	f = 1 MHz				4		pF
C_o	V_O = 0,	f = 1 MHz				8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 19)

		'ABT3612-15		'ABT3612-20		'ABT3612-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_c	Clock cycle time, CLKA or CLKB	15		20		30		ns
$t_{w(CLKH)}$	Pulse duration, CLKA and CLKB high	6		8		12		ns
$t_{w(CLKL)}$	Pulse duration, CLKA and CLKB low	6		8		12		ns
$t_{su(D)}$	Setup time, A0–A35 before CLKA↑ and B0–B35 before CLKB↑	4		5		6		ns
$t_{su(EN1)}$	Setup time, $\overline{CSA}$, W/$\overline{RA}$ before CLKA↑; $\overline{CSB}$, W/$\overline{RB}$ before CLKB↑	6		6		7		ns
$t_{su(EN2)}$	Setup time, ENA before CLKA↑; ENB before CLKB↑	4		5		6		ns
$t_{su(EN3)}$	Setup time, MBA before CLKA↑; MBB before CLKB↑	4		5		6		ns
$t_{su(PG)}$	Setup time, ODD/$\overline{EVEN}$ and PGA before CLKA↑; ODD/$\overline{EVEN}$ and PGB before CLKB↑†	4		5		6		ns
$t_{su(RS)}$	Setup time, $\overline{RST}$ low before CLKA↑ or CLKB↑‡	5		6		7		ns
$t_{su(FS)}$	Setup time, FS0 and FS1 before $\overline{RST}$ high	5		6		7		ns
$t_{h(D)}$	Hold time, A0–A35 after CLKA↑ and B0–B35 after CLKB↑	2.5		2.5		2.5		ns
$t_{h(EN1)}$	Hold time, $\overline{CSA}$, W/$\overline{RA}$ after CLKA↑; $\overline{CSB}$, W/$\overline{RB}$ after CLKB↑	2		2		2		ns
$t_{h(EN2)}$	Hold time, ENA after CLKA↑; ENB after CLKB↑	2.5		2.5		2.5		ns
$t_{h(EN3)}$	Hold time, MBA after CLKA↑; MBB after CLKB↑	1		1		1		ns
$t_{h(PG)}$	Hold time, ODD/$\overline{EVEN}$ and PGA after CLKA↑; ODD/$\overline{EVEN}$ and PGB after CLKB↑†	1		1		1		ns
$t_{h(RS)}$	Hold time, $\overline{RST}$ low after CLKA↑ or CLKB↑‡	5		6		7		ns
$t_{h(FS)}$	Hold time, FS0 and FS1 after $\overline{RST}$ high	4		4		4		ns
t_{sk1}§	Skew time, between CLKA↑ and CLKB↑ for $\overline{EFA}$, $\overline{EFB}$, $\overline{FFA}$, and $\overline{FFB}$	8		8		10		ns
t_{sk2}§	Skew time, between CLKA↑ and CLKB↑ for $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$, and $\overline{AFB}$	9		16		20		ns

† Only applies for a clock edge that does a FIFO read

‡ Requirement to count the clock edge as one of at least four needed to reset a FIFO

§ Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Figures 1 through 19)

PARAMETER		'ABT3612-15		'ABT3612-20		'ABT3612-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_a	Access time, CLKA↑ to A0–A35 and CLKB↑ to B0–B35	2	10	2	12	2	15	ns
$t_{pd(C\text{-}FF)}$	Propagation delay time, CLKA↑ to $\overline{FFA}$ and CLKB↑ to $\overline{FFB}$	2	10	2	12	2	15	ns
$t_{pd(C\text{-}EF)}$	Propagation delay time, CLKA↑ to $\overline{EFA}$ and CLKB↑ to $\overline{EFB}$	2	10	2	12	2	15	ns
$t_{pd(C\text{-}AE)}$	Propagation delay time, CLKA↑ to $\overline{AEA}$ and CLKB↑ to $\overline{AEB}$	2	10	2	12	2	15	ns
$t_{pd(C\text{-}AF)}$	Propagation delay time, CLKA↑ to $\overline{AFA}$ and CLKB↑ to $\overline{AFB}$	2	10	2	12	2	15	ns
$t_{pd(C\text{-}MF)}$	Propagation delay time, CLKA↑ to $\overline{MBF1}$ low or $\overline{MBF2}$ high and CLKB↑ to $\overline{MBF2}$ low or $\overline{MBF1}$ high	1	9	1	12	1	15	ns
$t_{pd(C\text{-}MR)}$	Propagation delay time, CLKA↑ to B0–B35† and CLKB↑ to A0–A35‡	3	11	3	13	3	15	ns
$t_{pd(M\text{-}DV)}$	Propagation delay time, MBA to A0–A35 valid and MBB to B0–B35 valid	1	11	1	11.5	1	12	ns
$t_{pd(D\text{-}PE)}$	Propagation delay time, A0-A35 valid to $\overline{PEFA}$ valid; B0-B35 valid to $\overline{PEFB}$ valid	3	10	3	11	3	13	ns
$t_{pd(O\text{-}PE)}$	Propagation delay time, ODD/$\overline{EVEN}$ to $\overline{PEFA}$ and $\overline{PEFB}$	3	11	3	12	3	14	ns
$t_{pd(O\text{-}PB)}$§	Propagation delay time, ODD/$\overline{EVEN}$ to parity bits (A8, A17, A26, A35) and (B8, B17, B26, B35)	2	11	2	12	2	14	ns
$t_{pd(E\text{-}PE)}$	Propagation delay time, W/$\overline{RA}$, $\overline{CSA}$, ENA, MBA, or PGA to $\overline{PEFA}$; W/$\overline{RB}$, $\overline{CSB}$, ENB, MBB, or PGB to $\overline{PEFB}$	1	11	1	12	1	14	ns
$t_{pd(E\text{-}PB)}$§	Propagation delay time, W/$\overline{RA}$, $\overline{CSA}$, ENA, MBA, or PGA to parity bits (A8, A17, A26, A35); W/$\overline{RB}$, $\overline{CSB}$, ENB, MBB, or PGB to parity bits (B8, B17, B26, B35)	3	12	3	13	3	14	ns
$t_{pd(R\text{-}F)}$	Propagation delay time, $\overline{RST}$ to ($\overline{AEA}$, $\overline{AEB}$) low and ($\overline{AFA}$, $\overline{AFB}$, $\overline{MBF1}$, $\overline{MBF2}$) high.	1	15	1	20	1	30	ns
t_{en}	Enable time, $\overline{CSA}$ and W/$\overline{RA}$ low to A0–A35 active and $\overline{CSB}$ low and $\overline{W}$/RB high to B0–B35 active	2	10	2	12	2	14	ns
t_{dis}	Disable time, $\overline{CSA}$ or W/$\overline{RA}$ high to A0–A35 at high impedance and $\overline{CSB}$ high or $\overline{W}$/RB low to B0–B35 at high impedance	1	8	1	9	1	11	ns

† Writing data to the mail1 register when the B0–B35 outputs are active and MBB is high.
‡ Writing data to the mail2 register when the A0–A35 outputs are active and MBA is high.
§ Only applies when reading data from a mail register

TYPICAL CHARACTERISTICS

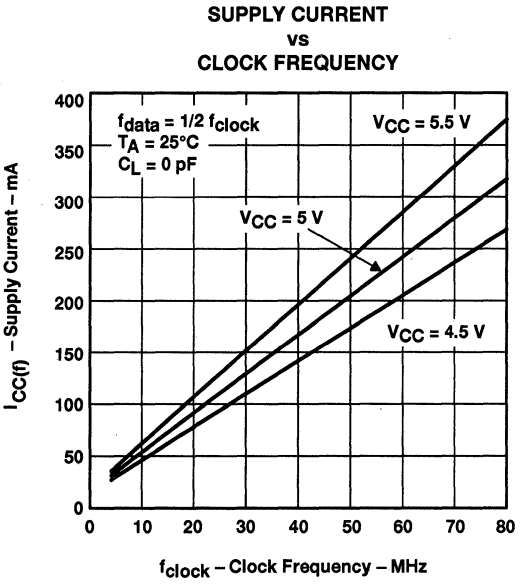


Figure 20

calculating power dissipation

The $I_{CC(f)}$ current for the graph in Figure 20 was taken while simultaneously reading and writing the FIFO on the SN74ACT3612 with CLKA and CLKB set to f_{clock}. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitive load per data-output channel is known, the power dissipation can be calculated with the equation below.

With $I_{CC(f)}$ taken from Figure 20, the maximum dynamic power dissipation (P_D) of the SN74ABT3612 can be calculated by:

$$P_D = V_{CC} \times I_{CC(f)} + \Sigma(C_L \times V_{CC} \times (V_{OH} - V_{OL}) \times f_o)$$

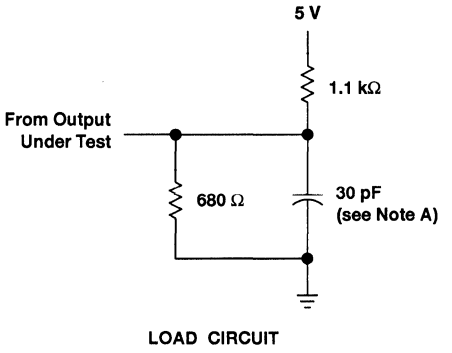
where:

C_L = output capacitive load
f_o = switching frequency of an output
V_{OH} = high-level output voltage
V_{OL} = low-level output voltage

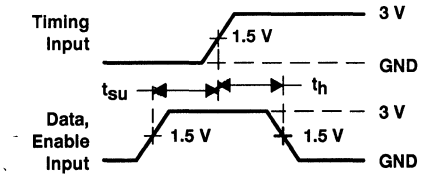
When no reads or writes are occurring on the SN74ABT3612, the power dissipated by a single clock (CLKA or CLKB) input running at frequency f_{clock} is calculated by:

$$P_T = V_{CC} \times f_{clock} \times 0.29 \text{ mA/MHz}$$

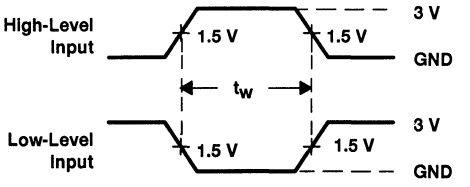
PARAMETER MEASUREMENT INFORMATION



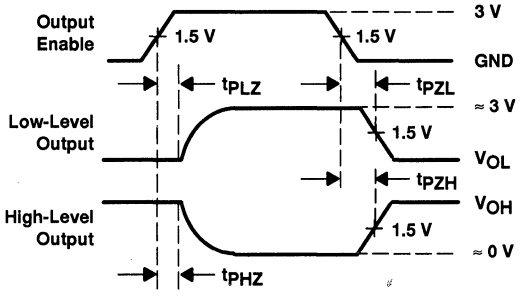
LOAD CIRCUIT



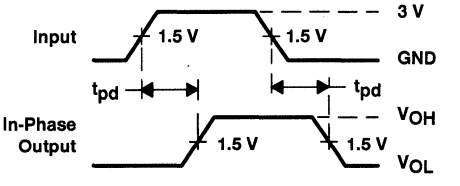
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTE A: Includes probe and jig capacitance

Figure 21. Load Circuit and Voltage Waveforms

- **Free-Running CLKA and CLKB Can Be Asynchronous or Coincident**
- **64 × 36 FIFO Buffering Data From Port A to Port B**
- **Mailbox Bypass Registers in Each Direction**
- **Dynamic Port-B Bus Sizing of 36 Bits (Long Word), 18 Bits (Word), and 9 Bits (Byte)**
- **Selection of Big- or Little-Endian Format for Word and Byte Bus Sizes**
- **Three Modes of Byte-Order Swapping on Port B**
- **Programmable Almost-Full and Almost-Empty Flags**
- **Microprocessor Interface Control Logic**
- **$\overline{FF}$ and $\overline{AF}$ Flags Synchronized by CLKA**
- **$\overline{EF}$ and $\overline{AE}$ Flags Synchronized by CLKB**
- **Passive Parity Checking on Each Port**
- **Parity Generation Can Be Selected for Each Port**
- **Low-Power Advanced BiCMOS Technology**
- **Supports Clock Frequencies up to 67 MHz**
- **Fast Access Times of 10 ns**
- **Available in Space-Saving 120-Pin Thin Quad Flat Package (PCB) or 132-Pin Quad Flat Package (PQ)**

description

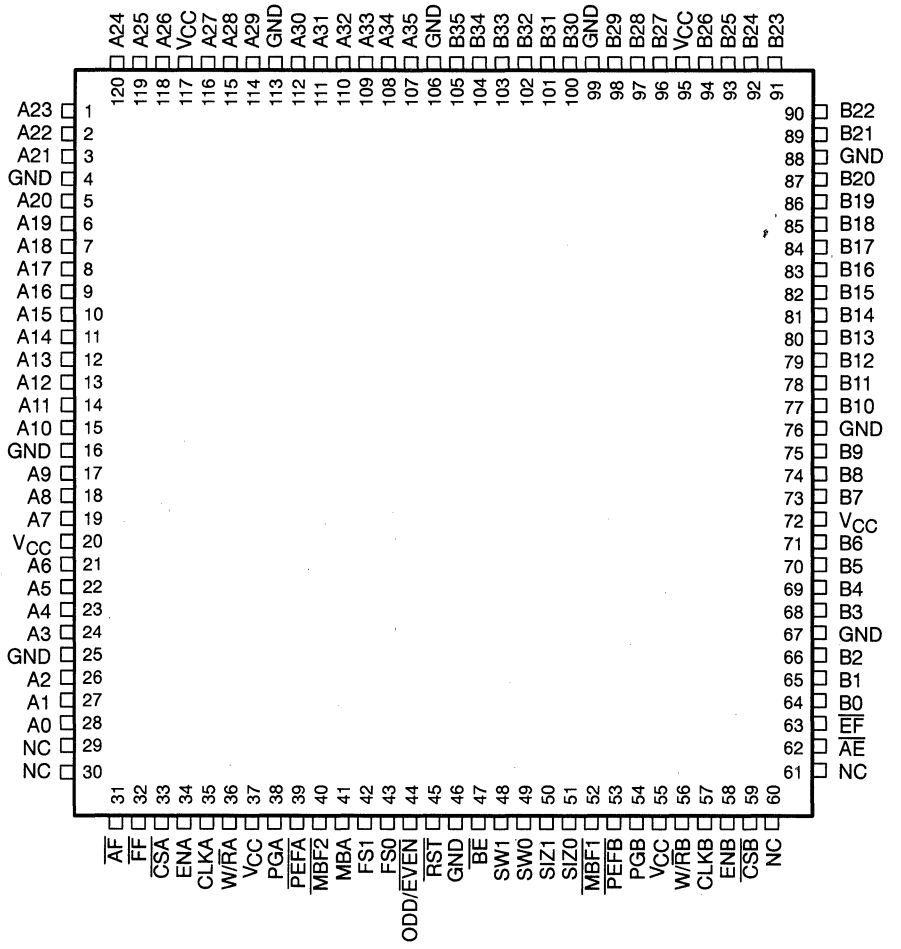
The SN74ABT3613 is a high-speed, low-power BiCMOS clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read-access times as fast as 10 ns. A 64 × 36 dual-port SRAM FIFO on board the chip buffers data from port A to port B. The FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words is stored in memory. FIFO data on port B can be output in 36-bit, 18-bit, and 9-bit formats with a choice of big- or little-endian configurations. Three modes of byte-order swapping are possible with any bus-size selection. Communication between each port can bypass the FIFO via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and can be ignored if not desired. Parity generation can be selected for data read from each port.

The SN74ABT3613 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple interface between microprocessors and/or buses controlled by a synchronous interface.

The full flag and almost-full flag of a FIFO are two-stage synchronized to the port clock that writes data to its array. The empty flag and almost-empty flag of a FIFO are two-stage synchronized to the port clock that reads data from its array.

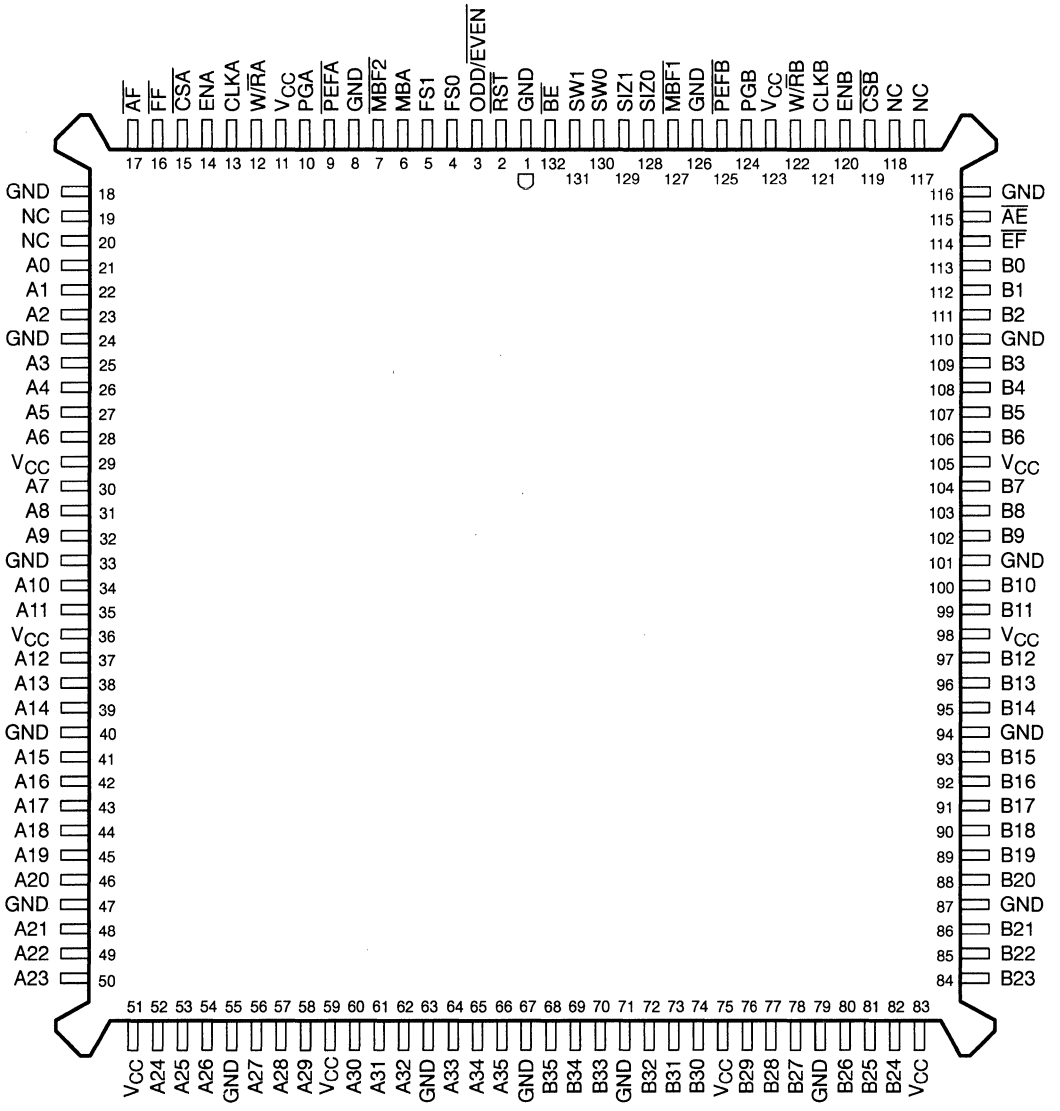
The SN74ABT3613 is characterized for operation from 0°C to 70°C.

PCB PACKAGE
(TOP VIEW)



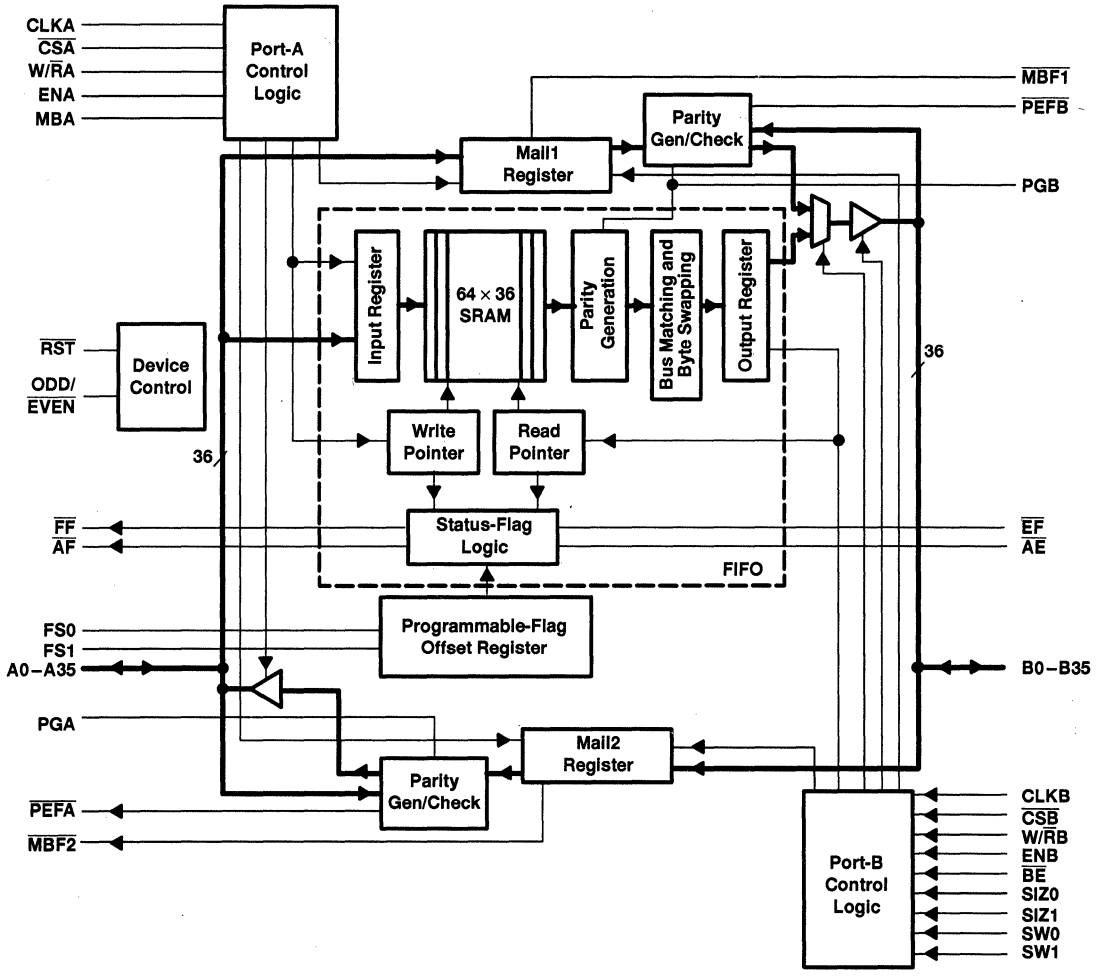
NC – No internal connection

PQ PACKAGE†
(TOP VIEW)



NC – No internal connection
† Uses Yamaichi socket IC51-1324-828

functional block diagram



Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
A0–A35	I/O	Port-A data. The 36-bit bidirectional data port for side A.
$\overline{AE}$	O (port B)	Almost-empty flag. Programmable almost-empty flag synchronized to CLKB. $\overline{AE}$ is low when the number of 36-bit words in the FIFO is less than or equal to the value in the offset register, X.
$\overline{AF}$	O (port A)	Almost-full flag. Programmable almost-full flag synchronized to CLKA. $\overline{AF}$ is low when the number of 36-bit empty locations in the FIFO is less than or equal to the value in the offset register, X.
B0–B35	I/O	Port-B data. The 36-bit bidirectional data port for side B.
$\overline{BE}$	I	Big-endian select. Selects the bytes on port B used during byte or word FIFO reads. A low on $\overline{BE}$ selects the most significant bytes on B0–B35 for use, and a high selects the least significant bytes.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. $\overline{FF}$ and $\overline{AF}$ are synchronized to the low-to-high transition of CLKA.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. Port-B byte swapping and data port sizing operations are also synchronous to the low-to-high transition of CLKB. $\overline{EF}$ and $\overline{AE}$ are synchronized to the low-to-high transition of CLKB.
$\overline{CSA}$	I	Port-A chip select. $\overline{CSA}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{CSA}$ is high.
$\overline{CSB}$	I	Port-B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{CSB}$ is high.
$\overline{EF}$	O (port B)	Empty flag. $\overline{EF}$ is synchronized to the low-to-high transition of CLKB. When $\overline{EF}$ is low, the FIFO is empty and reads from its memory are disabled. Data can be read from the FIFO to the output register when $\overline{EF}$ is high. $\overline{EF}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKB after data is loaded into empty FIFO memory.
ENA	I	Port-A enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port-B enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
$\overline{FF}$	O (port A)	Full flag. $\overline{FF}$ is synchronized to the low-to-high transition of CLKA. When $\overline{FF}$ is low, the FIFO is full and writes to its memory are disabled. $\overline{FF}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKA after reset.
FS1, FS0	I	Flag offset selects. The low-to-high transition of $\overline{RST}$ latches the values of FS0 and FS1, which selects one of four preset values for the almost-empty flag and almost-full flag offset.
MBA	I	Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation. When the A0–A35 outputs are active, mail2 register data is output.
$\overline{MBF1}$	O	Mail1 register flag. $\overline{MBF1}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is low. $\overline{MBF1}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and both SIZ1 and SIZ0 are high. $\overline{MBF1}$ is set high when the device is reset.
$\overline{MBF2}$	O	Mail2 register flag. $\overline{MBF2}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is low. $\overline{MBF2}$ is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. $\overline{MBF2}$ is set high when the device is reset.
ODD/$\overline{EVEN}$	I	Odd/even parity select. Odd parity is checked on each port when ODD/$\overline{EVEN}$ is high, and even parity is checked when ODD/$\overline{EVEN}$ is low. ODD/$\overline{EVEN}$ also selects the type of parity generated for each port if parity generation is enabled for a read operation.
$\overline{PEFA}$	O (port A)	Port-A parity error flag. When any byte applied to terminals A0–A35 fails parity, $\overline{PEFA}$ is low. Bytes are organized as A0–A8, A9–A17, A18–A26, and A27–A35 with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/$\overline{EVEN}$ input. The parity trees used to check the A0–A35 inputs are shared by the mail2 register to generate parity if parity generation is selected by PGA; therefore, if a mail2 read with parity generation is set up by having $\overline{CSA}$ low, ENA high, W/$\overline{RA}$ low, MBA high, and PGA high, the $\overline{PEFA}$ flag is forced high regardless of the state of the A0–A35 inputs.

Terminal Functions (Continued)

TERMINAL NAME	I/O	DESCRIPTION
$\overline{PEFB}$	O (port B)	Port-B parity error flag. When any valid byte applied to terminals B0–B35 fails parity, $\overline{PEFB}$ is low. Bytes are organized as B0–B8, B9–B17, B18–B26, and B27–B35 with the most significant bit of each byte serving as the parity bit. A byte is valid when it is used by the bus size selected for port B. The type of parity checked is determined by the state of the ODD/$\overline{EVEN}$ input. The parity trees used to check the B0–B35 inputs are shared by the mail1 register to generate parity if parity generation is selected by PGB; therefore, if a mail1 read with parity generation is set up by having $\overline{CSB}$ low, ENB high, W/$\overline{RB}$ low, SIZ1 and SIZ0 high, and PGB high, the $\overline{PEFB}$ flag is forced high regardless of the state of the B0–B35 inputs.
PGA	I	Port-A parity generation. Parity is generated for data reads from the mail2 register when PGA is high. The type of parity generated is selected by the state of the ODD/$\overline{EVEN}$ input. Bytes are organized as A0–A8, A9–A17, A18–A26, and A27–A35. The generated parity bits are output in the most significant bit of each byte.
PGB	I	Port-B parity generation. Parity is generated for data reads from port B when PGB is high. The type of parity generated is selected by the state of the ODD/$\overline{EVEN}$ input. Bytes are organized as B0–B8, B9–B17, B18–B26, and B27–B35. The generated parity bits are output in the most significant bit of each byte.
$\overline{RST}$	I	Reset. To reset the device, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RST}$ is low. This sets the $\overline{AF}$, $\overline{MBF1}$, and $\overline{MBF2}$ flags high and the $\overline{EF}$, $\overline{AE}$, and $\overline{FF}$ flags low. The low-to-high transition of $\overline{RST}$ latches the status of the FS1 and FS0 inputs to select almost-full flag and almost-empty flag offset.
SIZ0, SIZ1	I (port B)	Port-B bus size selects. The low-to-high transition of CLKB latches the states of SIZ0, SIZ1, and $\overline{BE}$, and the following low-to-high transition of CLKB implements the latched states as a port-B bus size. Port-B bus sizes can be long word, word, or byte. A high on both SIZ0 and SIZ1 accesses the mailbox registers for a port-B 36-bit write or read.
SW0, SW1	I (port B)	Port-B byte swap selects. At the beginning of each long word FIFO read, one of four modes of byte-order swapping is selected by SW0 and SW1. The four modes are no swap, byte swap, word swap, and byte-word swap. Byte-order swapping is possible with any bus-size selection.
W/$\overline{RA}$	I	Port-A write/read select. W/$\overline{RA}$ high selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{RA}$ is high.
W/$\overline{RB}$	I	Port-B write/read select. W/$\overline{RB}$ high selects a write operation and a low selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when W/$\overline{RB}$ is high.

detailed description

reset

The SN74ABT3613 is reset by taking the reset ($\overline{RST}$) input low for at least four port-A clock (CLKA) and four port-B clock (CLKB) low-to-high transitions. The reset input can switch asynchronously to the clocks. A device reset initializes the internal read and write pointers of each FIFO and forces the full flag ($\overline{FF}$) low, the empty flag ($\overline{EF}$) low, the almost-empty flag ($\overline{AE}$) low, and the almost-full flag ($\overline{AF}$) high. A reset also forces the mailbox flags ($\overline{MBF1}$, $\overline{MBF2}$) high. After a reset, $\overline{FF}$ is set high after two low-to-high transitions of CLKA. The device must be reset after power up before data is written to its memory.

A low-to-high transition on the $\overline{RST}$ input loads the almost-full and almost-empty offset register (X) with the value selected by the flag-select (FS0, FS1) inputs. The values that can be loaded into the register are shown in Table 1.

Table 1. Flag Programming

FS1	FS0	$\overline{RST}$	ALMOST-FULL AND ALMOST-EMPTY FLAG OFFSET REGISTER (X)
H	H	↑	16
H	L	↑	12
L	H	↑	8
L	L	↑	4

FIFO write/read operation

The state of the port-A data (A0–A35) outputs is controlled by the port-A chip select ($\overline{CSA}$) and the port-A write/read select (W/$\overline{RA}$). The A0–A35 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is high. The A0–A35 outputs are active when both $\overline{CSA}$ and W/$\overline{RA}$ are low. Data is loaded into the FIFO from the A0–A35 inputs on a low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is high, ENA is high, MBA is low, and $\overline{FFA}$ is high (see Table 2).

Table 2. Port-A Enable Function Table

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	A0–A35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, mail2 register	None
L	L	H	L	↑	Active, mail2 register	None
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set $\overline{MBF2}$ high)

The state of the port-B data (B0–B35) outputs is controlled by the port-B chip select ($\overline{CSB}$) and the port-B write/read select (W/$\overline{RB}$). The B0–B35 outputs are in the high-impedance state when either $\overline{CSB}$ or W/$\overline{RB}$ is high. The B0–B35 outputs are active when both $\overline{CSB}$ and W/$\overline{RB}$ are low. Data is read from the FIFO to the B0–B35 outputs by a low-to-high transition of CLKB when $\overline{CSB}$ is low, W/$\overline{RB}$ is low, ENB is high, $\overline{EFB}$ is high, and either SIZ0 or SIZ1 is low (see Table 3).

Table 3. Port-B Enable Function Table

$\overline{CSB}$	W/$\overline{RB}$	ENB	SIZ1, SIZ0	CLKB	B0–B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	One, both low	↑	In high-impedance state	None
L	H	H	Both high	↑	In high-impedance state	Mail2 write
L	L	L	One, both low	X	Active, FIFO output register	None
L	L	H	One, both low	↑	Active, FIFO output register	FIFO read
L	L	L	Both high	X	Active, mail1 register	None
L	L	H	Both high	↑	Active, mail1 register	Mail1 read (set $\overline{MBF1}$ high)

The setup and hold time constraints to the port clocks for the port chip selects ($\overline{CSA}$, $\overline{CSB}$) and write/read selects (W/$\overline{RA}$, W/$\overline{RB}$) are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is low during a clock cycle, the port chip select and write/read select can change states during the setup and hold time window of the cycle.

synchronized FIFO flags

Each FIFO flag is synchronized to its port clock through two flip-flop stages. This is done to improve flag reliability by reducing the probability of metastable events on the output when CLKA and CLKB operate asynchronously to one another (see the application report *Metastability Performance of Clocked FIFOs* in the 1994 *High-Performance FIFO Memories Data Book*, literature #SCAD003B). $\overline{FF}$ and $\overline{AF}$ are synchronized to CLKA. $\overline{EF}$ and $\overline{AE}$ are synchronized to CLKB. Table 4 shows the relationship of each port flag to the level of FIFO fill.

Table 4. FIFO Flag Operation

NUMBER OF 36-BIT WORDS IN THE FIFO†	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA	
	$\overline{EF}$	$\overline{AE}$	$\overline{AF}$	$\overline{FF}$
0	L	L	H	H
1 to X	H	L	H	H
(X + 1) to [64 – (X + 1)]	H	H	H	H
(64 – X) to 63	H	H	L	H
64	H	H	L	L

† X is the value in the almost-empty flag and almost-full flag offset register.

empty flag ($\overline{EF}$)

The FIFO empty flag is synchronized to the port clock that reads data from its array (CLKB). When the empty flag is high, new data can be read to the FIFO output register. When the empty flag is low, the FIFO is empty and attempted FIFO reads are ignored. When reading the FIFO with a byte or word size on port B, $\overline{EF}$ is set low when the fourth byte or second word of the last long word is read.

The FIFO read pointer is incremented each time a new word is clocked to the output register. The state machine that controls the empty flag monitors a write-pointer and a read-pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. A word written to the FIFO can be read to the FIFO output register in a minimum of three port-B clock (CLKB) cycles. An empty flag is low if a word in memory is the next data to be sent to the FIFO output register and two cycles of the port clock that reads data from the FIFO have not elapsed since the time the word was written. The empty flag of the FIFO is set high by the second low-to-high transition of CLKB, and the new data word can be read to the FIFO output register in the following cycle.

A low-to-high transition on CLKB begins the first synchronization cycle of a write if the clock transition occurs at time t_{sk1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figure 9).

full flag ($\overline{FF}$)

The FIFO full flag is synchronized to the port clock that writes data to its array (CLKA). When the full flag is high, a memory location is free in the SRAM to receive new data. No memory locations are free when the full flag is low and attempted writes to the FIFO are ignored.

Each time a word is written to the FIFO, the write pointer is incremented. The state machine that controls a full flag monitors a write-pointer and a read-pointer comparator that indicates when the FIFO SRAM status is full, full–1, or full–2. From the time a word is read from the FIFO, the previous memory location is ready to be written in a minimum of three CLKA cycles. A full flag is low if less than two CLKA cycles have elapsed since the next memory write location has been read. The second low-to-high transition on the full-flag synchronizing clock after the read sets the full flag high and data can be written in the following clock cycle.

A low-to-high transition on CLKA begins the first synchronization cycle of a read if the clock transition occurs at time t_{sk1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figure 10).

almost-empty flag ($\overline{AE}$)

The FIFO almost-empty flag is synchronized to the port clock that reads data from its array (CLKB). The state machine that controls an almost-empty flag monitors a write-pointer and a read-pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see reset). An almost-empty flag is low when the FIFO contains X or less long words in memory and is high when the FIFO contains (X + 1) or more long words.

Two low-to-high transitions of CLKB are required after a FIFO write for the almost-empty flag to reflect the new level of fill; therefore, the almost-empty flag of a FIFO containing (X + 1) or more long words remains low if two CLKB cycles have not elapsed since the write that filled the memory to the (X + 1) level. An almost-empty flag is set high by the second low-to-high transition of CLKB after the FIFO write that fills memory to the (X + 1) level. A low-to-high transition of CLKB begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the write that fills the FIFO to (X + 1) long words. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 11).

almost-full flag ($\overline{AF}$)

The FIFO almost-full flag is synchronized to the port clock that writes data to its array (CLKA). The state machine that controls an almost-full flag monitors a write-pointer and a read-pointer comparator that indicates when the FIFO SRAM status is almost full, almost full–1, or almost full–2. The almost-full state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see reset above). An almost-full flag is low when the FIFO contains (64 – X) or more long words in memory and is high when the FIFO contains [64 – (X + 1)] or less long words.

Two low-to-high transitions of CLKA are required after a FIFO read for the almost-full flag to reflect the new level of fill; therefore, the almost-full flag of a FIFO containing [64 – (X + 1)] or less words remains low if two CLKA cycles have not elapsed since the read that reduced the number of long words in memory to [64 – (X + 1)]. An almost-full flag is set high by the second low-to-high transition of CLKA after the FIFO read that reduces the number of long words in memory to [64 – (X + 1)]. A low-to-high transition of CLKA begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the read that reduces the number of long words in memory to [64 – (X + 1)]. Otherwise, the subsequent CLKA cycle can be the first synchronization cycle (see Figure 12).

mailbox registers

Two 36-bit bypass registers (mail1, mail2) are on board the SN74ABT3613 to pass command and control information between port A and port B without putting it in queue. A low-to-high transition on CLKA writes A0–A35 data to the mail1 register when a port-A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA, and MBA is high. A low-to-high transition on CLKB writes B0–B35 data to the mail2 register when a port-B write is selected by ($\overline{CSB}$, W/$\overline{RB}$, and ENB) and both SIZ0 and SIZ1 are high. Writing data to a mail register sets the corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) low. Attempted writes to a mail register are ignored while the mail flag is low.

When the port-B data outputs (B0–B35) are active, the data on the bus comes from the FIFO output register when either one or both SIZ1 and SIZ0 are low and from the mail1 register when both SIZ1 and SIZ0 are high. The mail1 register flag ($\overline{MBF1}$) is set high by a rising CLKB edge when a port-B read is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB, and both SIZ1 and SIZ0 are high. The mail2 register flag ($\overline{MBF2}$) is set high by a rising CLKA edge when a port-A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and MBA is high. The data in the mail register remains intact after it is read and changes only when new data is written to the register.

dynamic bus sizing

The port-B bus can be configured in a 36-bit long word, 18-bit word, or 9-bit byte format for data read from the FIFO. Word- and byte-size bus selections can utilize the most significant bytes of the bus (big endian) or least significant bytes of the bus (little endian). Port-B bus-size can be changed dynamically and synchronous to CLKB to communicate with peripherals of various bus widths.

The levels applied to the port-B bus size select (SIZ0, SIZ1) inputs and the big-endian select ($\overline{BE}$) input are stored on each CLKB low-to-high transition. The stored port-B bus-size selection is implemented by the next rising edge on CLKB according to Figure 1.

Only 36-bit long-word data is written to or read from the FIFO memory on the SN74ABT3613. Bus-matching operations are done after data is read from the FIFO RAM. Port-B bus sizing does not apply to mail-register operations.

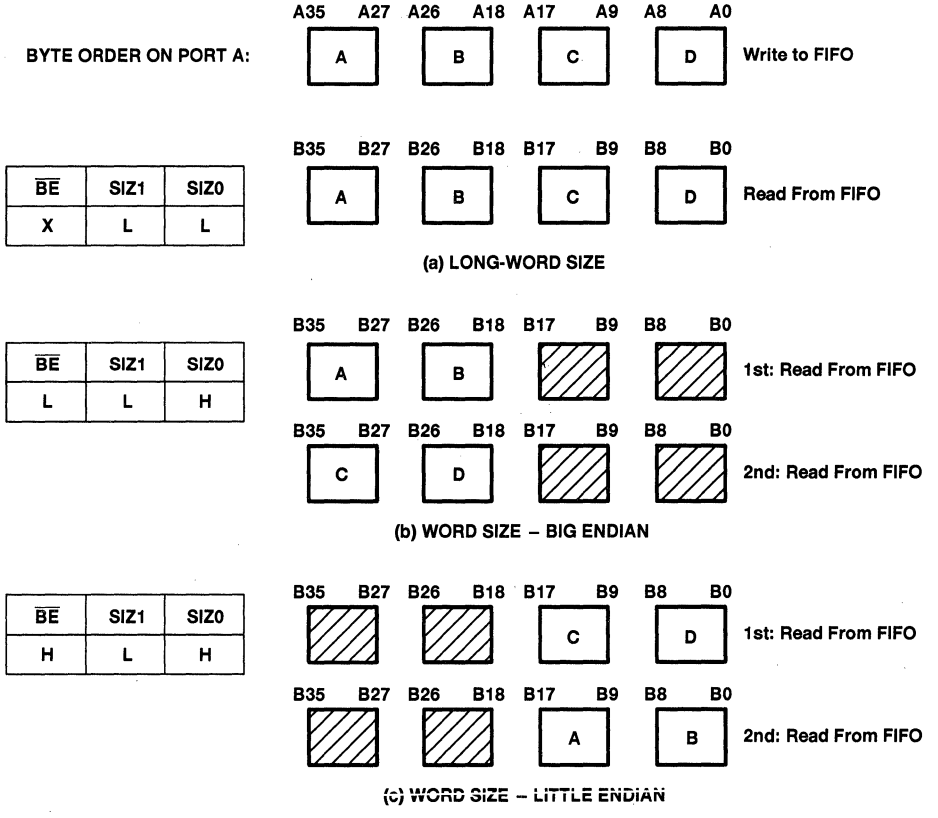
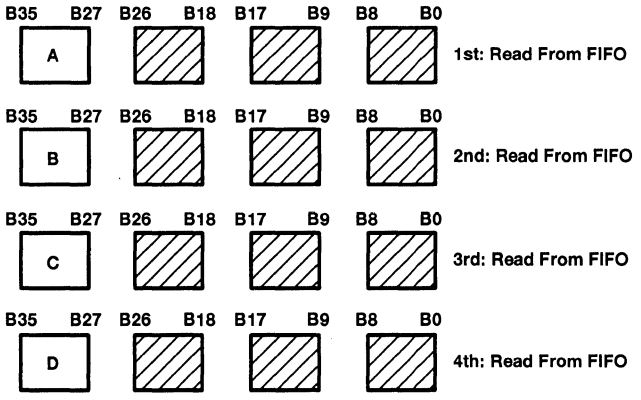


Figure 1. Dynamic Bus Sizing

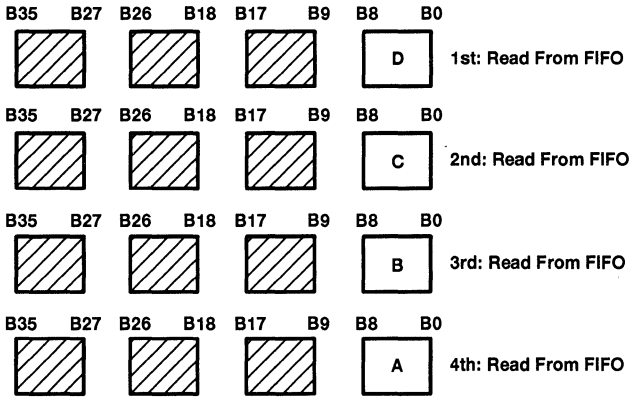
dynamic bus sizing (continued)

$\overline{BE}$	SIZ1	SIZ0
L	H	L



(d) BYTE SIZE – BIG ENDIAN

$\overline{BE}$	SIZ1	SIZ0
H	H	L



(e) BYTE SIZE – LITTLE ENDIAN

Figure 1. Dynamic Bus Sizing (continued)

bus-matching FIFO reads

Data is read from the FIFO RAM in 36-bit long-word increments. If a long-word bus size is implemented, the entire long word immediately shifts to the FIFO output register upon a read. If byte or word size is implemented on port B, only the first one or two bytes appear on the selected portion of the FIFO output register with the rest of the long word stored in auxiliary registers. In this case, subsequent FIFO reads with the same bus-size implementation output the rest of the long word to the FIFO output register in the order shown by Figure 1.

Each FIFO read with a new bus-size implementation automatically unloads data from the FIFO RAM to its output register and auxiliary registers. Implementing a new port-B bus size and performing a FIFO read before all bytes or words stored in the auxiliary registers have been read results in a loss of the unread data in these registers.

When reading data from FIFO in byte or word format, the unused B0–B35 outputs remain inactive but static, with the unused FIFO output register bits holding the last data value to decrease power consumption.

port-B mail register access

In addition to selecting port-B bus sizes for FIFO reads, the port-B bus size select (SIZ0, SIZ1) inputs also access the mail registers. When both SIZ0 and SIZ1 are high, the mail1 register is accessed for a port-B long-word read and the mail2 register is accessed for a port-B long-word write. The mail register is accessed immediately and any bus-sizing operation that can be underway is unaffected by the the mail-register access. After the mail-register access is complete, the previous FIFO access can resume in the next CLKB cycle. The logic diagram in Figure 2 shows the previous bus-size selection is preserved when the mail registers are accessed from port B. A port-B bus size is implemented on each rising CLKB edge according to the states of SIZ0_Q, SIZ1_Q, and $\overline{BE}$_Q.

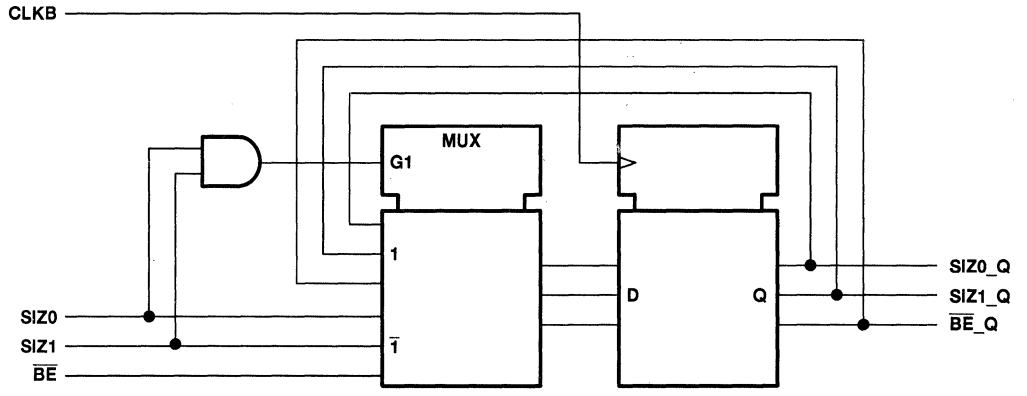


Figure 2. Logic Diagram for SIZ0, SIZ1, and $\overline{BE}$ Register

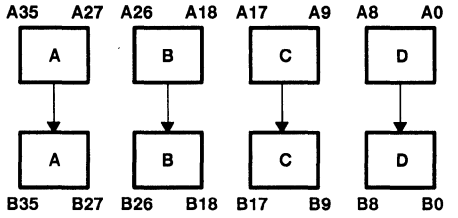
byte swapping

The byte-order arrangement of data read from the FIFO can be changed synchronous to the rising edge of CLKB. Byte-order swapping is not available for mail-register data. Four modes of byte-order swapping (including no swap) can be done with any data port-size selection. The order of the bytes are rearranged within the long word, but the bit order within the bytes remains constant.

Byte arrangement is chosen by the port-B swap select (SW0, SW1) inputs on a CLKB rising edge that reads a new long word from the FIFO. The byte order chosen on the first byte or first word of a new long word read from the FIFO is maintained until the entire long word is transferred, regardless of the SW0 and SW1 states during subsequent reads. Figure 3 is an example of the byte-order swapping available for long word reads. Performing a byte swap and bus size simultaneously for a FIFO read first rearranges the bytes as shown in Figure 3, then outputs the bytes as shown in Figure 1.

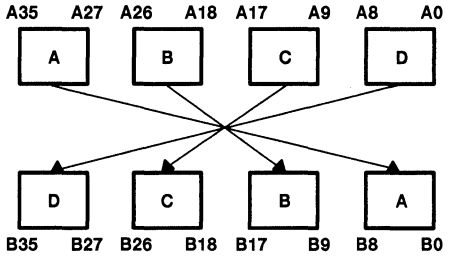
byte swapping (continued)

SW1	SW0
L	L



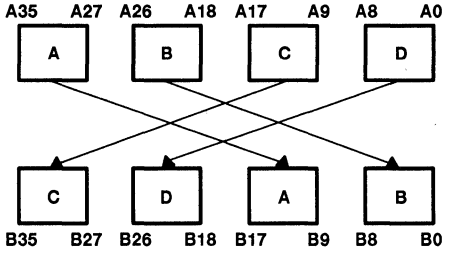
(a) NO SWAP

SW1	SW0
L	H



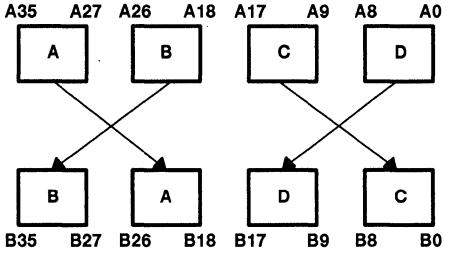
(b) BYTE SWAP

SW1	SW0
H	L



(c) WORD SWAP

SW1	SW0
H	H



(d) BYTE-WORD SWAP

Figure 3. Byte Swapping for FIFO Reads (Long-Word Size Example)

parity checking

The port-A data inputs (A0–A35) and port-B data inputs (B0–B35) each have four parity trees to check the parity of incoming (or outgoing) data. A parity failure on one or more bytes of the port-A data bus is reported by a low level on the port-A parity error flag ($\overline{\text{PEFA}}$). A parity failure on one or more bytes of the port-B data inputs that are valid for the bus-size implementation is reported by a low level on the port-B parity error flag ($\overline{\text{PEFB}}$). Odd or even parity checking can be selected, and the parity error flags can be ignored if this feature is not desired.

Parity status is checked on each input bus according to the level of the odd/even parity (ODD/$\overline{\text{EVEN}}$) select input. A parity error on one or more valid bytes of a port is reported by a low level on the corresponding port-parity-error flag ($\overline{\text{PEFA}}$, $\overline{\text{PEFB}}$) output. Port-A bytes are arranged as A0–A8, A9–A17, A18–A26, and A27–A35. Port-B bytes are arranged as B0–B8, B9–B17, B18–B26, and B27–B35, and its valid bytes are those used in a port-B bus-size implementation. When odd/even parity is selected, a port-parity-error flag ($\overline{\text{PEFA}}$, $\overline{\text{PEFB}}$) is low if any valid byte on the port has an odd/even number of low levels applied to the bits.

The four parity trees used to check the A0–A35 inputs are shared by the mail2 register when parity generation is selected for port-A reads (PGA = high). When a port-A read from the mail2 register with parity generation is selected with $\overline{\text{CSA}}$ low, ENA high, W/$\overline{\text{RA}}$ low, MBA high, and PGA high, the port-A parity error flag ($\overline{\text{PEFA}}$) is held high regardless of the levels applied to the A0–A35 inputs. Likewise, the parity trees used to check the B0–B35 inputs are shared by the mail1 register when parity generation is selected for port-B reads (PGB = high). When a port-B read from the mail1 register with parity generation is selected with $\overline{\text{CSB}}$ low, ENB high, W/$\overline{\text{RB}}$ low, both SIZ0 and SIZ1 high, and PGB high, the port-B parity error flag ($\overline{\text{PEFB}}$) is held high regardless of the levels applied to the B0–B35 inputs.

parity generation

A high level on the port-A parity generate select (PGA) or port-B parity generate select (PGB) enables the SN74ABT3613 to generate parity bits for port reads from a FIFO or mailbox register. Port-A bytes are arranged as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit of each byte used as the parity bit. Port-B bytes are arranged as B0–B8, B9–B17, B18–B26, and B27–B35 with the most significant bit of each byte used as the parity bit. A write to a FIFO or mail register stores the levels applied to all nine inputs of a byte regardless of the state of the parity generate select (PGA, PGB) inputs. When data is read from a port with parity generation selected, the lower eight bits of each byte are used to generate a parity bit according to the level on the ODD/$\overline{\text{EVEN}}$ select. The generated parity bits are substituted for the levels orignially written to the most significant bits of each byte as the word is read to the data outputs.

Parity bits for FIFO data are generated after the data is read from SRAM and before the data is written to the output register. The port-A parity generate select (PGA) and odd/even parity select (ODD/$\overline{\text{EVEN}}$) have setup and hold time constraints to the port-A clock (CLKA) and the port-B parity generate select (PGB) and ODD/$\overline{\text{EVEN}}$ select have setup and hold-time constraints to the port-B clock (CLKB). These timing constraints only apply for a rising clock edge used to read a new long word to the FIFO output register.

The circuit used to generate parity for the mail1 data is shared by the port-B bus (B0–B35) to check parity and the circuit used to generate parity for the mail2 data is shared by the port-A bus (A0–A35) to check parity. The shared parity trees of a port are used to generate parity bits for the data in a mail register when the port chip select ($\overline{\text{CSA}}$, $\overline{\text{CSB}}$) is low, enable (ENA, ENB) is high, and write/read select (W/$\overline{\text{RA}}$, W/$\overline{\text{RB}}$) input is low, the mail register is selected (MBA is high for port A; both SIZ0 and SIZ1 are high for port B), and port parity generate select (PGA, PGB) is high. Generating parity for mail-register data does not change the contents of the register.

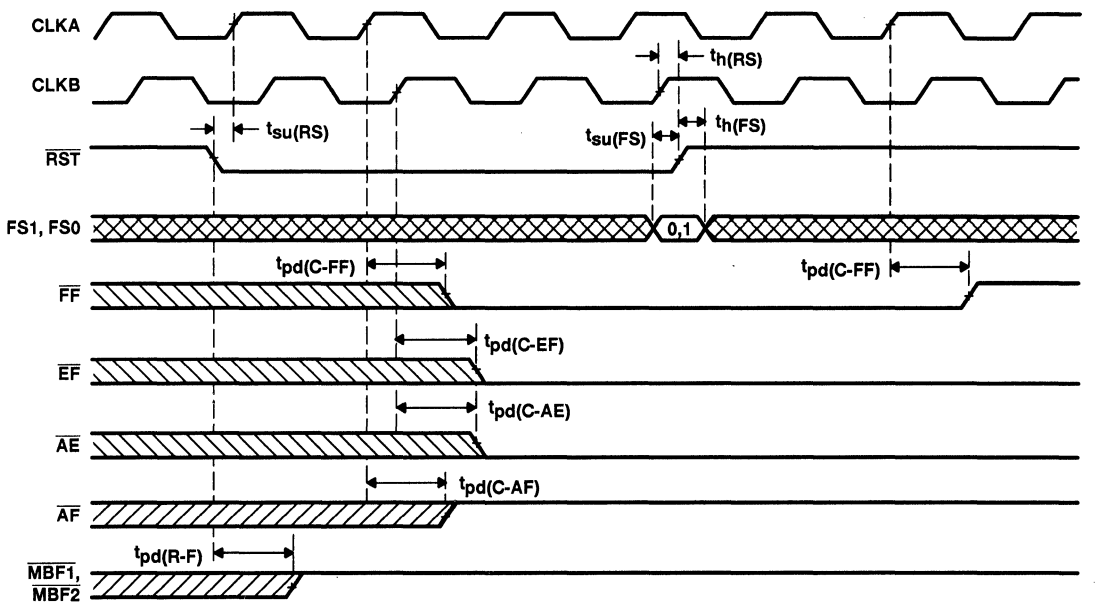
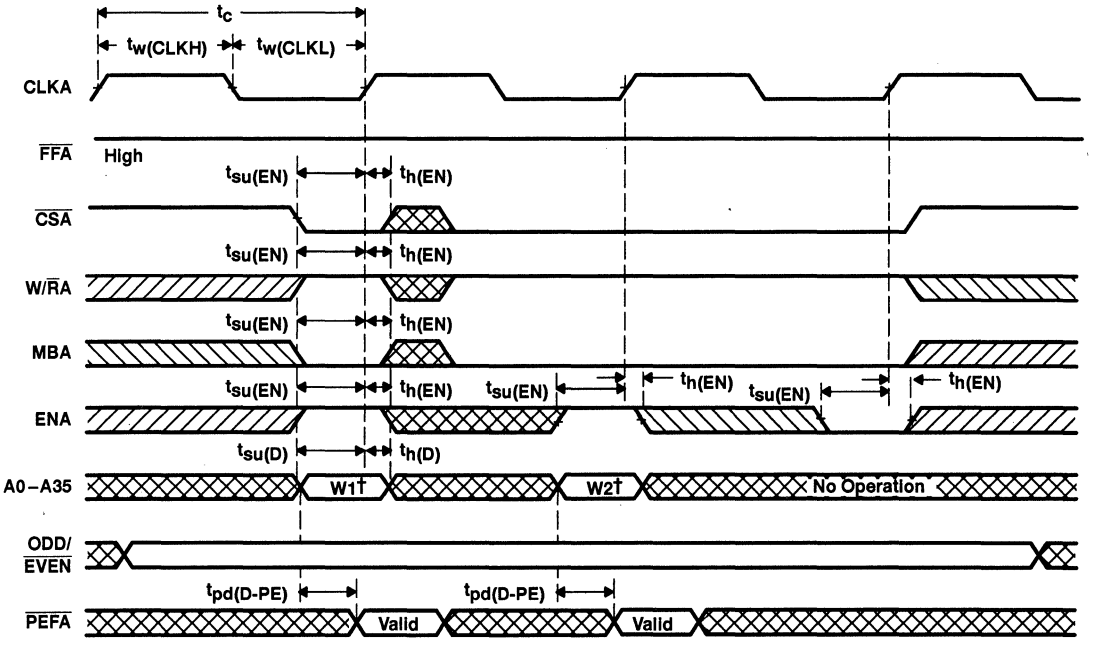
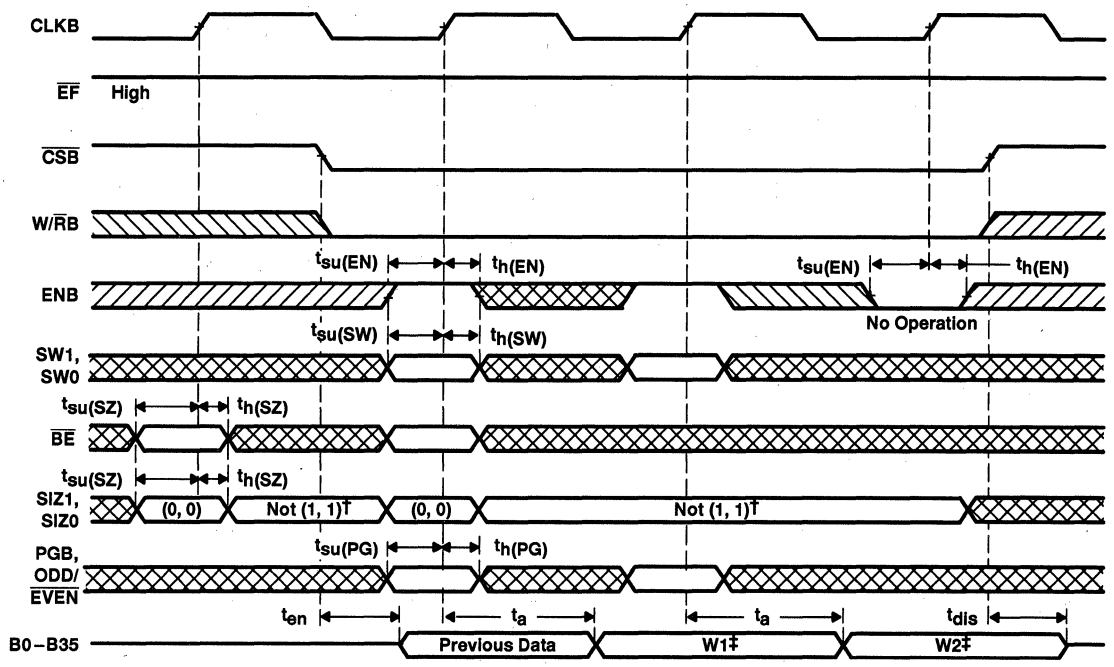


Figure 4. Device Reset Loading the X Register With the Value of Eight



† Written to the FIFO

Figure 5. FIFO-Write-Cycle Timing

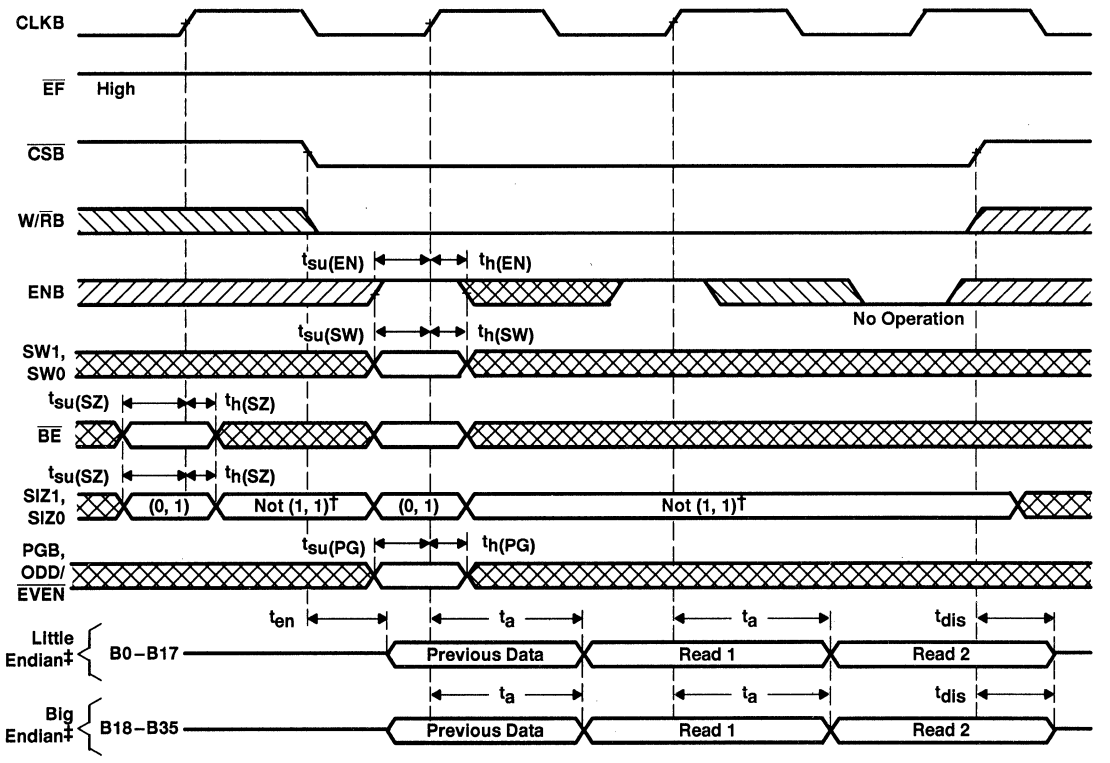


† SIZ0 = H and SIZ1 = H selects the mail1 register for output on B0–B35.
‡ Data read from the FIFO

DATA SWAP TABLE FOR FIFO LONG-WORD READS

FIFO-DATA WRITE				SWAP MODE		FIFO-DATA READ			
A35–A27	A26–A18	A17–A9	A8–A0	SW1	SW0	B35–B27	B26–B18	B17–B9	B8–B0
A	B	C	D	L	L	A	B	C	D
A	B	C	D	L	H	D	C	B	A
A	B	C	D	H	L	C	D	A	B
A	B	C	D	H	H	B	A	D	C

Figure 6. FIFO Long-Word Read-Cycle Timing

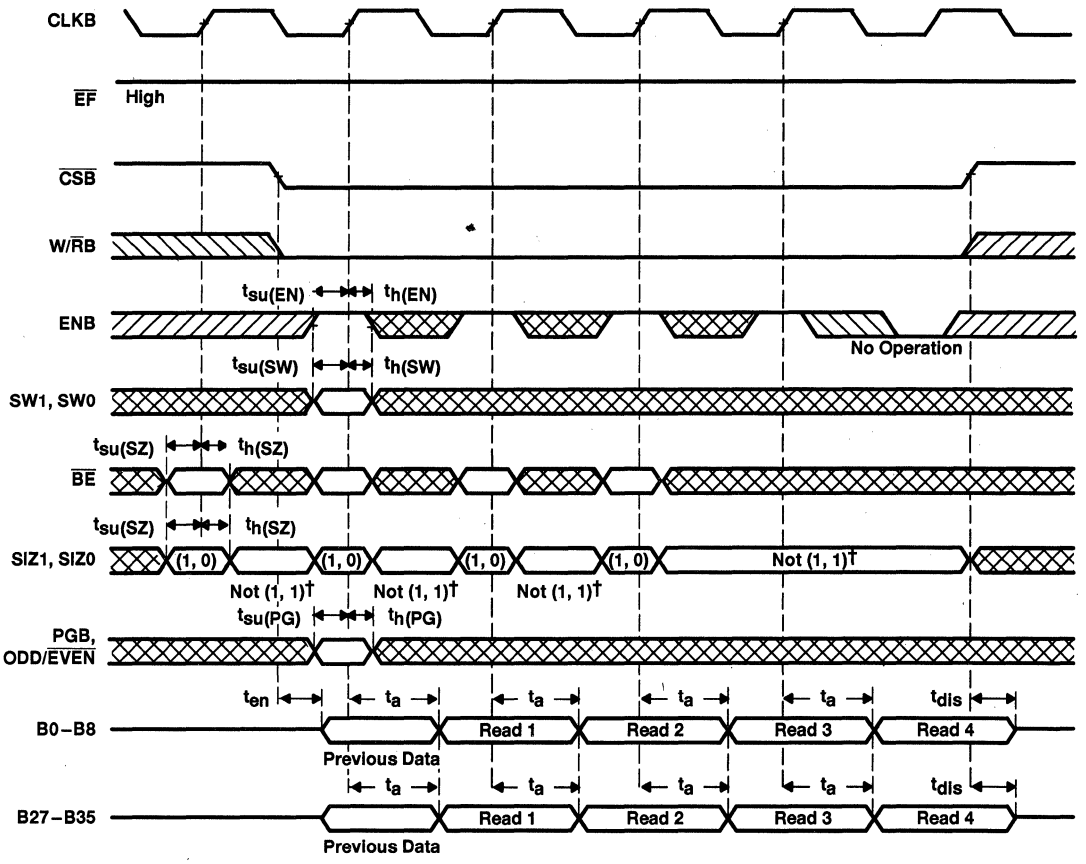


† SIZ0 = H and SIZ1 = H selects the mail1 register for output on B0–B35.
‡ Unused word B0–B17 or B18–B35 holds last FIFO output register data for word-size reads.

DATA SWAP TABLE FOR FIFO-WORD READS

FIFO-DATA WRITE				SWAP MODE		READ NO.	FIFO-DATA READ			
							BIG ENDIAN		LITTLE ENDIAN	
A35–A27	A26–A18	A17–A9	A8–A0	SW1	SW0		B35–B27	B26–B18	B17–B9	B8–B0
A	B	C	D	L	L	1	A	B	C	D
						2	C	D	A	B
A	B	C	D	L	H	1	D	C	B	A
						2	B	A	D	C
A	B	C	D	H	L	1	C	D	A	B
						2	A	B	C	D
A	B	C	D	H	H	1	B	A	D	C
						2	D	C	B	A

Figure 7. FIFO-Word Read-Cycle Timing



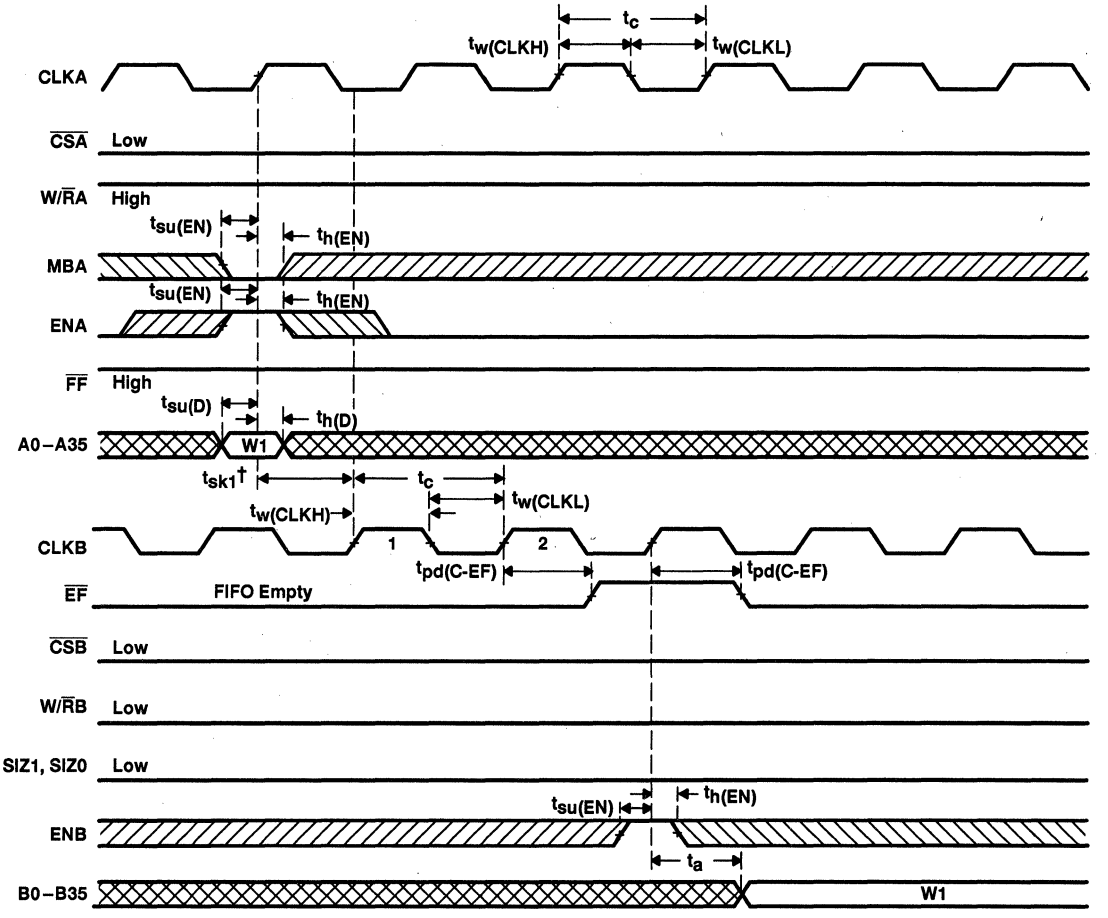
† SIZ0 = H and SIZ1 = H selects the mail1 register for output on B0–B35.
NOTE A: Unused bytes hold last FIFO output register data for byte-size reads.

Figure 8. FIFO-Byte Read-Cycle Timing

DATA SWAP TABLE FOR FIFO-BYTE READS

FIFO-DATA WRITE				SWAP MODE		READ NO.	FIFO-DATA READ	
							BIG ENDIAN	LITTLE ENDIAN
A35–A27	A26–A18	A17–A9	A8–A0	SW1	SW0		B35–B27	B8–B0
A	B	C	D	L	L	1 2 3 4	A B C D	D C B A
A	B	C	D	L	H	1 2 3 4	D C B A	A B C D
A	B	C	D	H	L	1 2 3 4	C D A B	B A D C
A	B	C	D	H	H	1 2 3 4	B A D C	C D A B

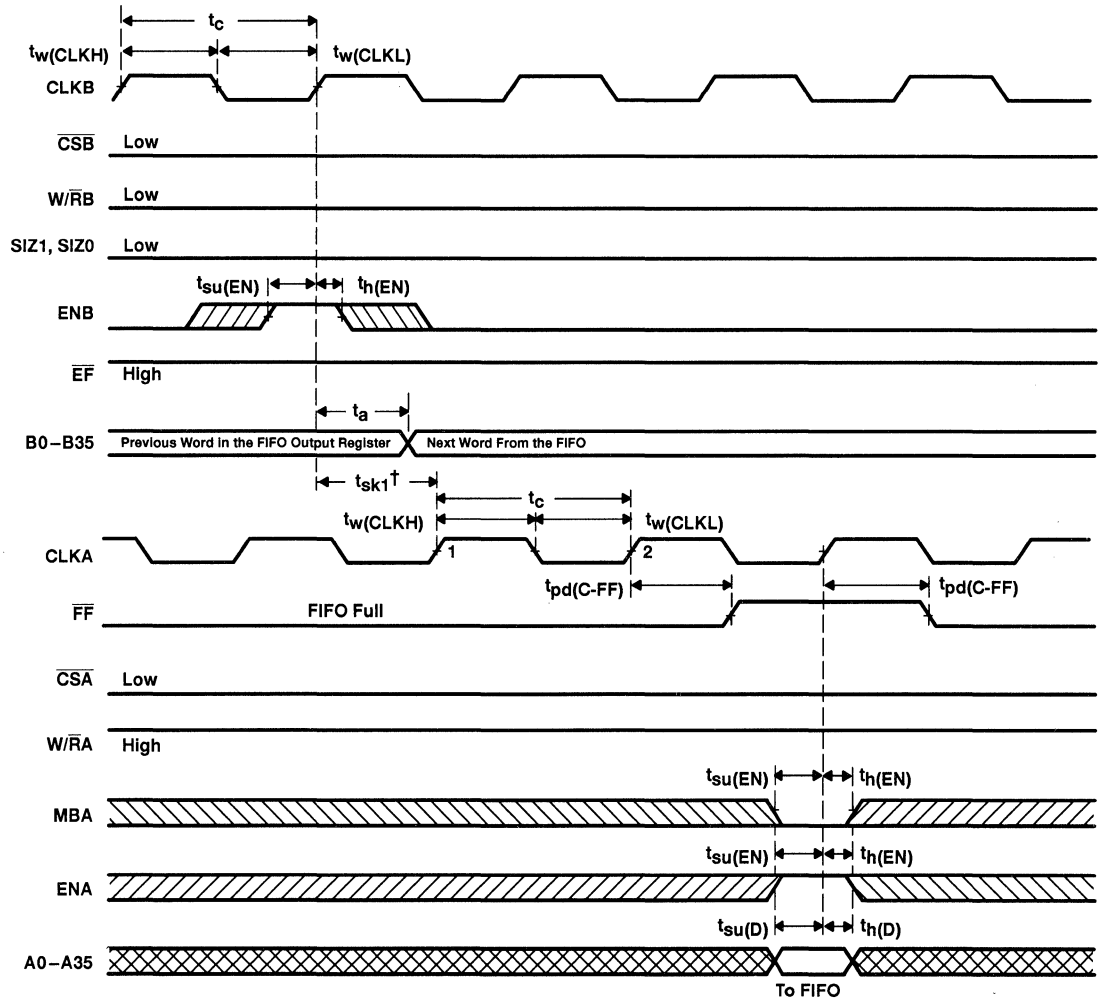
Figure 8. FIFO-Byte Read-Cycle Timing (continued)



† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EF}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, the transition of $\overline{EF}$ high may occur one CLKB cycle later than shown.

NOTE A: Port-B size of long word is selected for the FIFO read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, $\overline{EF}$ is set low by the last word or byte read from the FIFO, respectively.

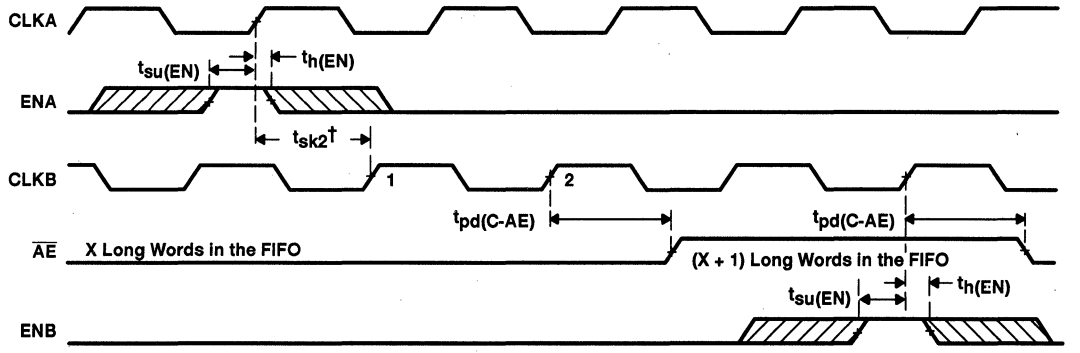
Figure 9. $\overline{EF}$-Flag Timing and First Data Read When the FIFO Is Empty



† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{FF}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, $\overline{FF}$ may transition high one CLKA cycle later than shown.

NOTE A: Port-B size of long word is selected for the FIFO read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, t_{sk1} is referenced from the rising CLKB edge that reads the first word or byte of the long word, respectively.

Figure 10. $\overline{FF}$-Flag Timing and First Available Write When the FIFO Is Full

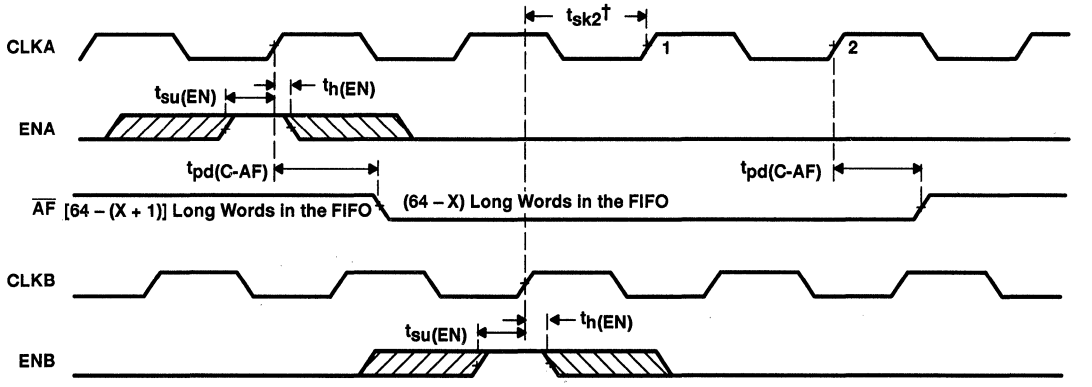


† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AE}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, $\overline{AE}$ may transition high one CLKB cycle later than shown.

NOTES: A. FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L)

B. Port-B size of long word is selected for FIFO read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, t_{sk2} is referenced to the first word or byte read of the long word, respectively.

Figure 11. Timing for $\overline{AE}$ When the FIFO Is Almost Empty

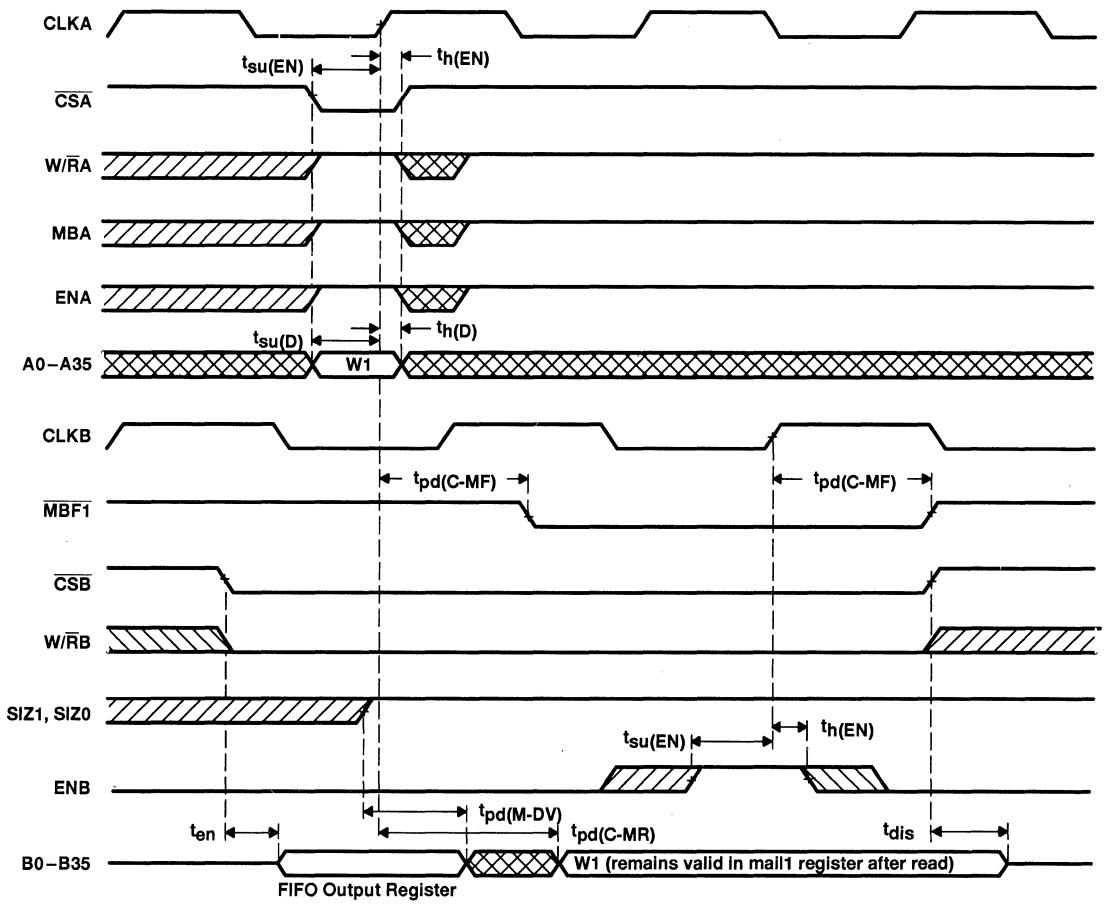


† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AF}$ to transition high in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, $\overline{AF}$ may transition high one CLKB cycle later than shown.

NOTES: A. FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L)

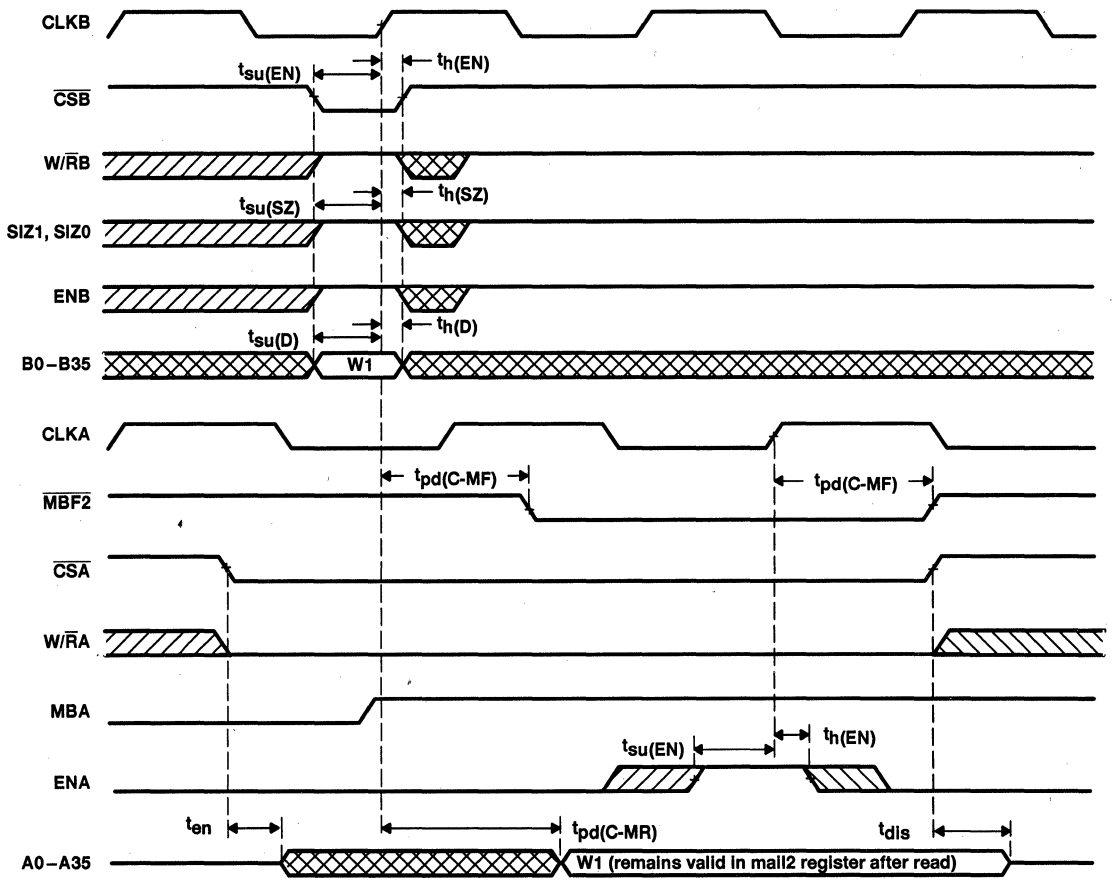
B. Port-B size of long word is selected for FIFO read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, t_{sk2} is referenced from the first word or byte read of the long word, respectively.

Figure 12. Timing for $\overline{AF}$ When the FIFO Is Almost Full



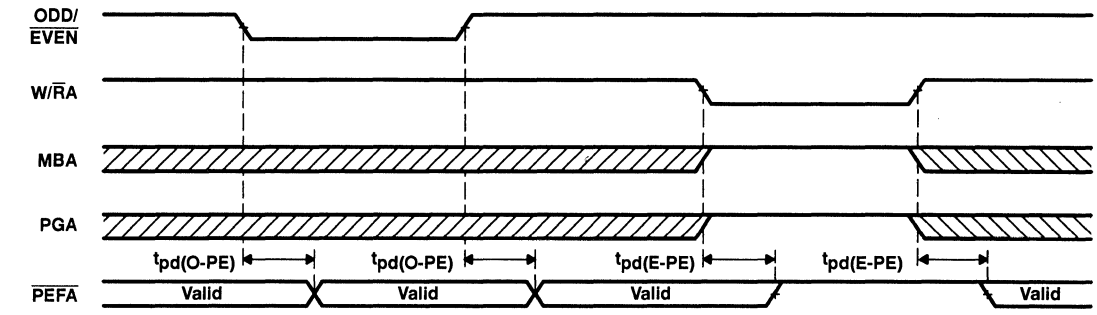
NOTE A: Port-B parity generation off (PGB = L)

Figure 13. Timing for Mail1 Register and $\overline{\text{MBF1}}$ Flag



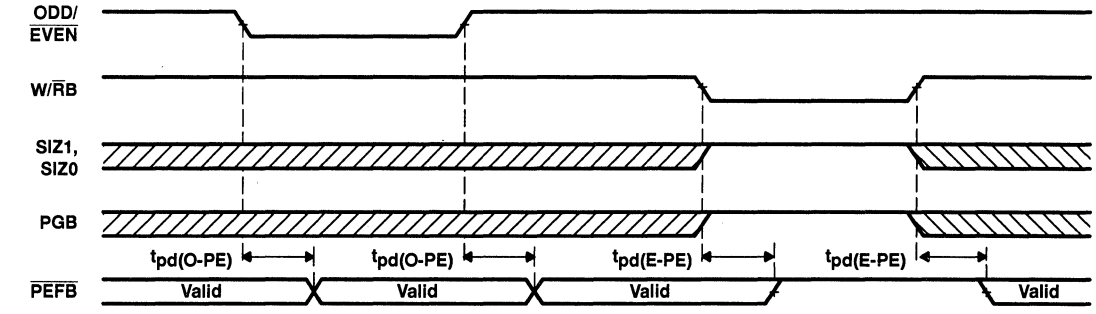
NOTE A: Port-A parity generation off (PGA = L)

Figure 14. Timing for Mail2 Register and $\overline{\text{MBF2}}$ Flag



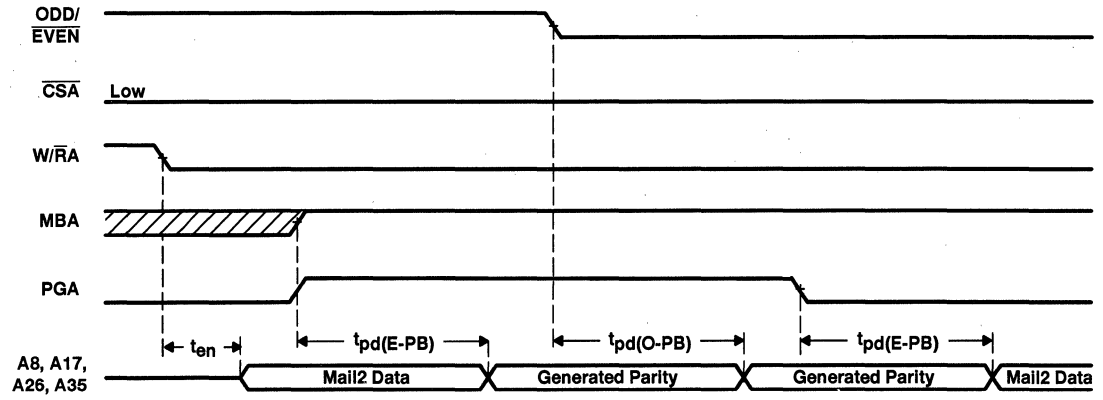
NOTE A: $\overline{CSA}$ = L and ENA = H

Figure 15. ODD/$\overline{EVEN}$, W/$\overline{RA}$, MBA, and PGA to $\overline{PEFA}$ Timing



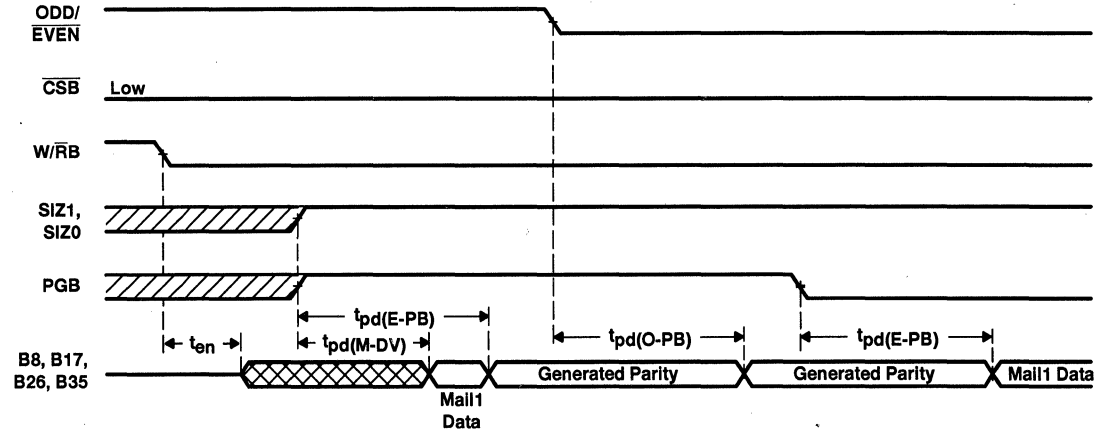
NOTE A: $\overline{CSB}$ = L and ENB = H

Figure 16. ODD/$\overline{EVEN}$, W/$\overline{RB}$, SIZ1, SIZ0, and PGB to $\overline{PEFB}$ Timing



NOTE A: ENA = H

Figure 17. Parity-Generation Timing When Reading From the Mail2 Register



NOTE A: ENB = H

Figure 18. Parity-Generation Timing When Reading From the Mail1 Register

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±500 mA
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−4	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS				MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −4 mA			2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0					±50	µA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0					±50	µA
I_{CC}	V_{CC} = 5.5 V,	I_O = 0 mA,	V_I = V_{CC} or GND	Outputs high			60	mA
				Outputs low			130	
				Outputs disabled			60	
C_i	V_I = 0,	f = 1 MHz				4		pF
C_o	V_O = 0,	f = 1 MHz				8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 4 through 18)

		'ABT3613-15		'ABT3613-20		'ABT3613-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_c	Clock cycle time, CLKA or CLKB	15		20		30		ns
$t_{w(CLKH)}$	Pulse duration, CLKA and CLKB high	6		8		12		ns
$t_{w(CLKL)}$	Pulse duration, CLKA and CLKB low	6		8		12		ns
$t_{su(D)}$	Setup time, A0–A35 before CLKA↑ and B0–B35 before CLKB↑	4		5		6		ns
$t_{su(EN)}$	Setup time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA before CLKA↑; $\overline{CSB}$, W/$\overline{RB}$, and ENB before CLKB↑	5		5		6		ns
$t_{su(SZ)}$	Setup time, SIZ0, SIZ1, and $\overline{BE}$ before CLKB↑	4		5		6		ns
$t_{su(SW)}$	Setup time, SW0 and SW1 before CLKB↑	5		7		8		ns
$t_{su(PG)}$	Setup time, ODD/$\overline{EVEN}$ and PGB before CLKB↑†	4		5		6		ns
$t_{su(RS)}$	Setup time, $\overline{RST}$ low before CLKA↑ or CLKB↑‡	5		6		7		ns
$t_{su(FS)}$	Setup time, FS0 and FS1 before $\overline{RST}$ high	5		6		7		ns
$t_{h(D)}$	Hold time, A0–A35 after CLKA↑ and B0–B35 after CLKB↑	1		1		1		ns
$t_{h(EN)}$	Hold time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA after CLKA↑; $\overline{CSB}$, W/$\overline{RB}$, and ENB after CLKB↑	1		1		1		ns
$t_{h(SZ)}$	Hold time, SIZ0, SIZ1, and $\overline{BE}$ after CLKB↑	2		2		2		ns
$t_{h(SW)}$	Hold time, SW0 and SW1 after CLKB↑	0		0		0		ns
$t_{h(PG)}$	Hold time, ODD/$\overline{EVEN}$ and PGB after CLKB↑†	0		0		0		ns
$t_{h(RS)}$	Hold time, $\overline{RST}$ low after CLKA↑ or CLKB↑‡	5		6		7		ns
$t_{h(FS)}$	Hold time, FS0 and FS1 after $\overline{RST}$ high	4		4		4		ns
t_{sk1}§	Skew time between CLKA↑ and CLKB↑ for $\overline{EF}$ and $\overline{FF}$	8		8		10		ns
t_{sk2}§	Skew time between CLKA↑ and CLKB↑ for $\overline{AE}$ and $\overline{AF}$	9		16		20		ns

† Only applies for a clock edge that does a FIFO read
‡ Requirement to count the clock edge as one of at least four needed to reset a FIFO
§ Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Figures 4 through 18)

PARAMETER		'ABT3613-15		'ABT3613-20		'ABT3613-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_a	Access time, CLKA↑ to A0–A35 and CLKB↑ to B0–B35	2	10	2	12	2	15	ns
$t_{pd(C-FF)}$	Propagation delay time, CLKA↑ to $\overline{FF}$	2	10	2	12	2	15	ns
$t_{pd(C-EF)}$	Propagation delay time, CLKB↑ to $\overline{EF}$	2	10	2	12	2	15	ns
$t_{pd(C-AE)}$	Propagation delay time, CLKB↑ to $\overline{AE}$	2	10	2	12	2	15	ns
$t_{pd(C-AF)}$	Propagation delay time, CLKA↑ to $\overline{AF}$	2	10	2	12	2	15	ns
$t_{pd(C-MF)}$	Propagation delay time, CLKA↑ to $\overline{MBF1}$ low or $\overline{MBF2}$ high and CLKB↑ to $\overline{MBF2}$ low or $\overline{MBF1}$ high	1	9	1	12	1	15	ns
$t_{pd(C-MR)}$	Propagation delay time, CLKA↑ to B0–B35† and CLKB↑ to A0–A35‡	3	11	3	12	3	15	ns
$t_{pd(C-PE)}$§	Propagation delay time, CLKB↑ to $\overline{PEFB}$	2	11	2	12	2	13	ns
$t_{pd(M-DV)}$	Propagation delay time, SIZ1, SIZ0 to B0–B35 valid	1	11	1	11.5	1	12	ns
$t_{pd(D-PE)}$	Propagation delay time, A0-A35 valid to $\overline{PEFA}$ valid; B0–B35 valid to $\overline{PEFB}$ valid	3	10	3	11	3	13	ns
$t_{pd(O-PE)}$	Propagation delay time, ODD/$\overline{EVEN}$ to $\overline{PEFA}$ and $\overline{PEFB}$	3	11	3	12	3	14	ns
$t_{pd(O-PB)}$¶	Propagation delay time, ODD/$\overline{EVEN}$ to parity bits (A8, A17, A26, A35) and (B8, B17, B26, B35)	2	12	2	13	2	15	ns
$t_{pd(E-PE)}$	Propagation delay time, $\overline{CSA}$, ENA, W/$\overline{RA}$, MBA, or PGA to $\overline{PEFA}$; $\overline{CSB}$, ENB, W/$\overline{RB}$, SIZ1, SIZ0, or PGB to $\overline{PEFB}$	1	11	1	12	1	14	ns
$t_{pd(E-PB)}$¶	Propagation delay time, $\overline{CSA}$, ENA, W/$\overline{RA}$, MBA, or PGA to parity bits (A8, A17, A26, A35); $\overline{CSB}$, ENB, W/$\overline{RB}$, SIZ1, SIZ0, or PGB to parity bits (B8, B17, B26, B35)	3	12	3	13	3	14	ns
$t_{pd(R-F)}$	Propagation delay time, $\overline{RST}$ to $\overline{AE}$, $\overline{EF}$ low and $\overline{AF}$, $\overline{MBF1}$, $\overline{MBF2}$ high.	1	15	1	20	1	25	ns
t_{en}	Enable time, $\overline{CSA}$ and W/$\overline{RA}$ low to A0–A35 active and $\overline{CSB}$ low and W/$\overline{RB}$ high to B0–B35 active	2	10	2	12	2	14	ns
t_{dis}	Disable time, $\overline{CSA}$ or W/$\overline{RA}$ high to A0–A35 at high impedance and $\overline{CSB}$ high or W/$\overline{RB}$ low to B0–B35 at high impedance	1	8	1	9	1	11	ns

† Writing data to the mail1 register when the B0–B35 outputs are active and SIZ1 and SIZ0 are high.
‡ Writing data to the mail2 register when the A0–A35 outputs are active and MBA is high.
§ Only applies when a new port-B bus size is implemented by the rising CLKB edge.
¶ Only applies when reading data from a mail register

TYPICAL CHARACTERISTICS

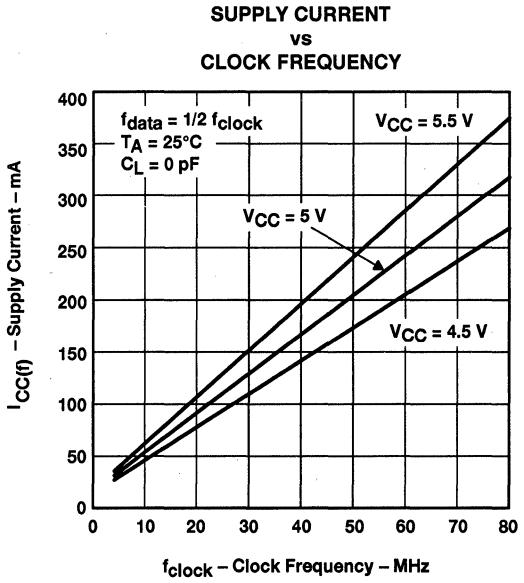


Figure 19

calculating power dissipation

The $I_{CC(f)}$ current for the graph in Figure 19 was taken while simultaneously reading and writing the FIFO on the SN74ACT3613 with CLKA and CLKB set to f_{clock}. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitive load per data-output channel is known, the power dissipation can be calculated with the equation below.

With $I_{CC(f)}$ taken from Figure 19, the maximum power dissipation (P_T) of the SN74ABT3613 can be calculated by:

$$P_T = V_{CC} \times I_{CC(f)} + \Sigma[C_L \times (V_{OH} - V_{OL})^2 \times f_o]$$

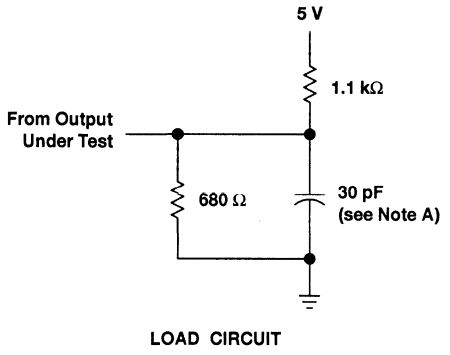
where:

C_L = output capacitive load
f_o = switching frequency of an output
V_{OH} = high-level output voltage
V_{OL} = low-level output voltage

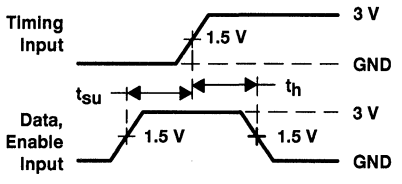
When no reads or writes are occurring on the SN74ABT3613, the power dissipated by a single clock (CLKA or CLKB) input running at frequency f_{clock} is calculated by:

$$P_T = V_{CC} \times f_{clock} \times 0.29 \text{ mA/MHz}$$

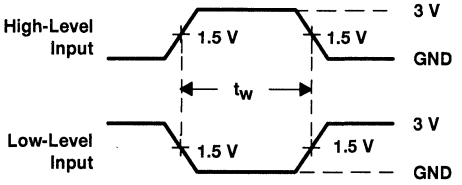
PARAMETER MEASUREMENT INFORMATION



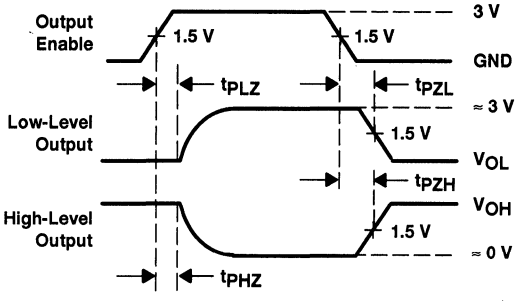
LOAD CIRCUIT



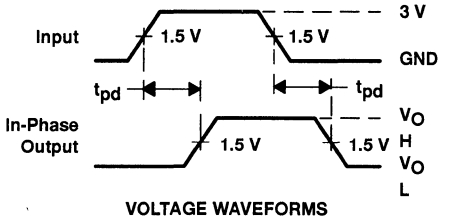
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTE A: Includes probe and jig capacitance

Figure 20. Load Circuit and Voltage Waveforms

- **Free-Running CLKA and CLKB Can Be Asynchronous or Coincident**
- **Two Independent 64 × 36 Clocked FIFOs Buffering Data in Opposite Directions**
- **Mailbox Bypass Register for Each FIFO**
- **Dynamic Port-B Bus Sizing of 36 Bits (Long Word), 18 Bits (Word), and 9 Bits (Byte)**
- **Selection of Big- or Little-Endian Format for Word and Byte Bus Sizes**
- **Three Modes of Byte-Order Swapping on Port B**
- **Almost-Full and Almost-Empty Flags**
- **Microprocessor Interface Control Logic**
- **$\overline{\text{EFA}}$, $\overline{\text{FFA}}$, $\overline{\text{AEA}}$, and $\overline{\text{AFA}}$ Flags Synchronized by CLKA**
- **$\overline{\text{EFB}}$, $\overline{\text{FFB}}$, $\overline{\text{AEB}}$, and $\overline{\text{AFB}}$ Flags Synchronized by CLKB**
- **Passive Parity Checking on Each Port**
- **Parity Generation Can Be Selected for Each Port**
- **Low-Power Advanced BiCMOS Technology**
- **Supports Clock Frequencies up to 67 MHz**
- **Fast Access Times of 10 ns**
- **Available in Space-Saving 120-Pin Thin Quad Flat Package (PCB) or 132-Pin Quad Flat Package (PQ)**

description

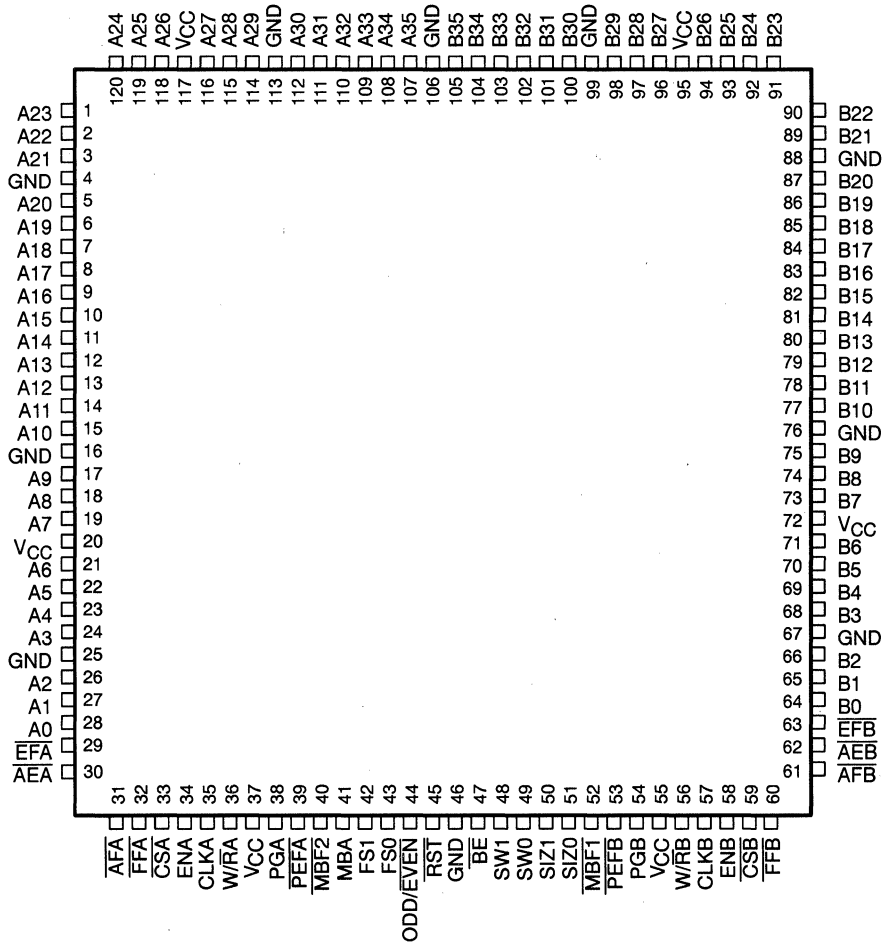
The SN74ABT3614 is a high-speed, low-power BiCMOS bidirectional clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read-access times as fast as 10 ns. Two independent 64 × 36 dual-port SRAM FIFOs on board the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words is stored in memory. FIFO data on port B can be input and output in 36-bit, 18-bit, and 9-bit formats with a choice of big- or little-endian configurations. Three modes of byte-order swapping are possible with any bus size selection. Communication between each port can bypass the FIFOs via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and can be ignored if not desired. Parity generation can be selected for data read from each port.

The SN74ABT3614 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses controlled by a synchronous interface.

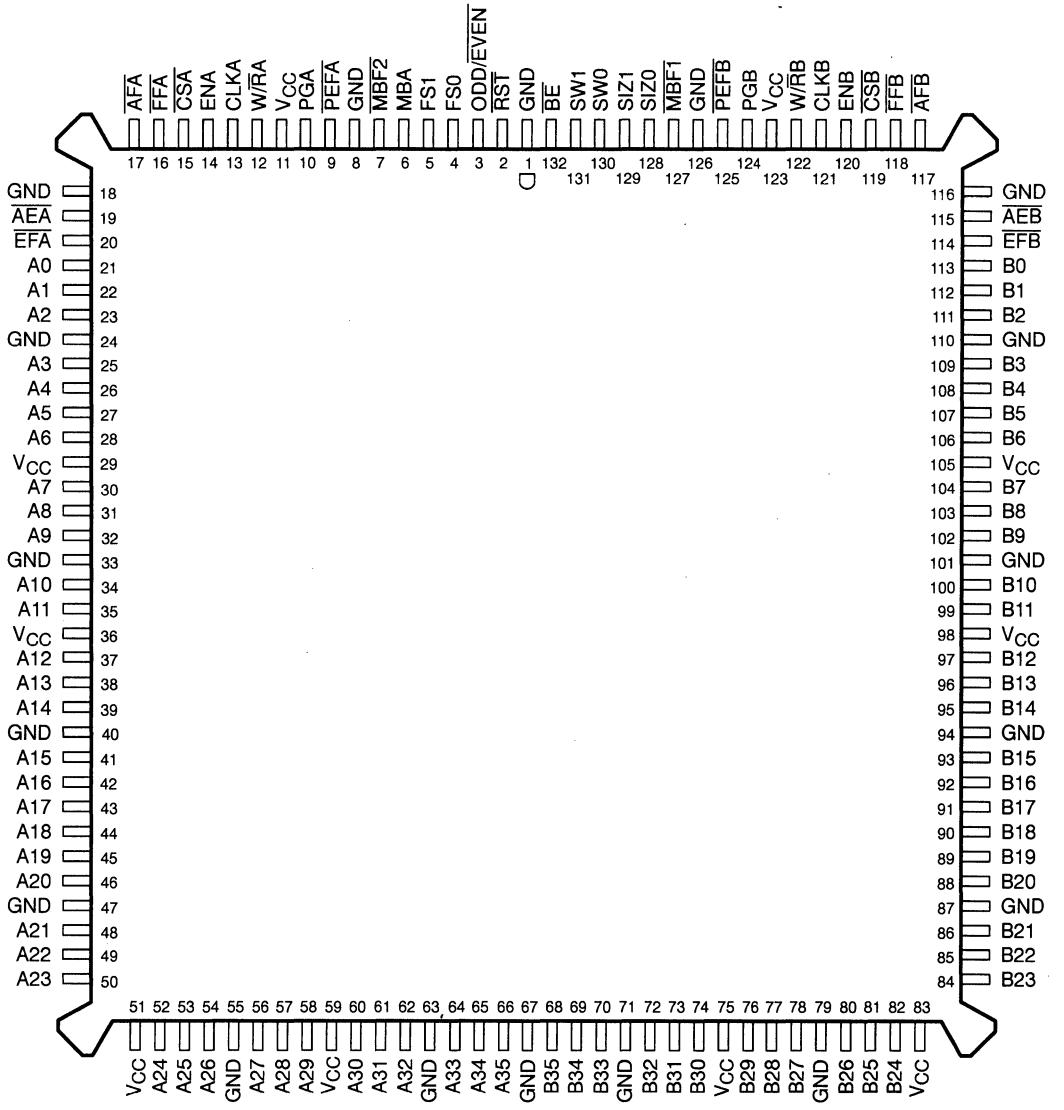
The full flag and almost-full flag of a FIFO are two-stage synchronized to the port clock that writes data to its array. The empty flag and almost-empty flag of a FIFO are two-stage synchronized to the port clock that reads data from its array.

The SN74ABT3614 is characterized for operation from 0°C to 70°C.

PCB PACKAGE
(TOP VIEW)

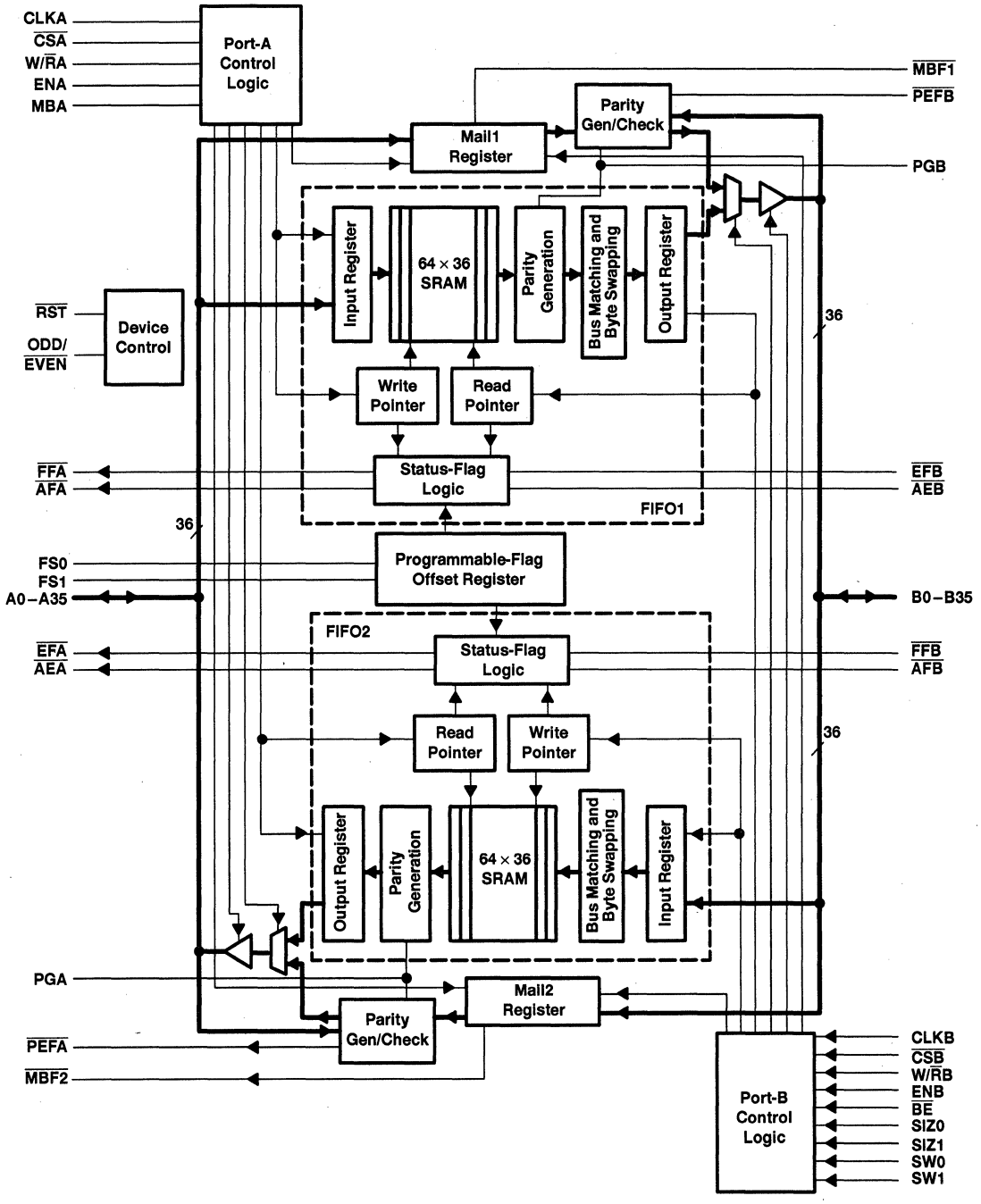


PQ PACKAGE†
(TOP VIEW)



NC – No internal connection
† Uses Yamaichi socket IC51-1324-828

functional block diagram



Terminal Functions

PIN NAME	I/O	DESCRIPTION
A0–A35	I/O	Port-A data. The 36-bit bidirectional data port for side A.
$\overline{AEA}$	O (port A)	Port-A almost-empty flag. Programmable almost-empty flag synchronized to CLKA. $\overline{AEA}$ is low when the number of 36-bit words in FIFO2 is less than or equal to the value in the offset register, X.
$\overline{AEB}$	O (port B)	Port-B almost-empty flag. Programmable almost-empty flag synchronized to CLKB. $\overline{AEB}$ is low when the number of 36-bit words in FIFO1 is less than or equal to the value in the offset register, X.
$\overline{AFA}$	O (port A)	Port-A almost-full flag. Programmable almost-full flag synchronized to CLKA. $\overline{AFA}$ is low when the number of 36-bit empty locations in FIFO1 is less than or equal to the value in the offset register, X.
$\overline{AFB}$	O (port B)	Port-B almost-full flag. Programmable almost-full flag synchronized to CLKB. $\overline{AFB}$ is low when the number of 36-bit empty locations in FIFO2 is less than or equal to the value in the offset register, X.
B0–B35	I/O	Port-B data. The 36-bit bidirectional data port for side B.
$\overline{BE}$	I	Big-endian select. Selects the bytes on port B used during byte or word data transfer. A low on $\overline{BE}$ selects the most significant bytes on B0–B35 for use, and a high selects the least significant bytes.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. $\overline{EFA}$, $\overline{FFA}$, $\overline{AFA}$, and $\overline{AEA}$ are synchronized to the low-to-high transition of CLKA.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. Port-B byte swapping and data port sizing operations are also synchronous to the low-to-high transition of CLKB. $\overline{EFB}$, $\overline{FFB}$, $\overline{AFB}$, and $\overline{AEB}$ are synchronized to the low-to-high transition of CLKB.
$\overline{CSA}$	I	Port-A chip select. $\overline{CSA}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{CSA}$ is high.
$\overline{CSB}$	I	Port-B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{CSB}$ is high.
$\overline{EFA}$	O (port A)	Port-A empty flag. $\overline{EFA}$ is synchronized to the low-to-high transition of CLKA. When $\overline{EFA}$ is low, FIFO2 is empty and reads from its memory are disabled. Data can be read from FIFO2 to the output register when $\overline{EFA}$ is high. $\overline{EFA}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKA after data is loaded into empty FIFO2 memory.
$\overline{EFB}$	O (port B)	Port-B empty flag. $\overline{EFB}$ is synchronized to the low-to-high transition of CLKB. When $\overline{EFB}$ is low, FIFO1 is empty and reads from its memory are disabled. Data can be read from FIFO1 to the output register when $\overline{EFB}$ is high. $\overline{EFB}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKB after data is loaded into empty FIFO1 memory.
ENA	I	Port-A enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port-B enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
$\overline{FFA}$	O (port A)	Port-A full flag. $\overline{FFA}$ is synchronized to the low-to-high transition of CLKA. When $\overline{FFA}$ is low, FIFO1 is full and writes to its memory are disabled. $\overline{FFA}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKA after reset.
$\overline{FFB}$	O (port B)	Port-B full flag. $\overline{FFB}$ is synchronized to the low-to-high transition of CLKB. When $\overline{FFB}$ is low, FIFO2 is full and writes to its memory are disabled. $\overline{FFB}$ is forced low when the device is reset and is set high by the second low-to-high transition of CLKB after reset.
FS1, FS0	I	Flag offset selects. The low-to-high transition of $\overline{RST}$ latches the values of FS0 and FS1, which selects one of four preset values for the almost-empty flag and almost-full flag offset.
MBA	I	Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation. When the A0–A35 outputs are active, a high level on MBA selects data from the mail2 register for output and a low level selects FIFO2 output register data for output.
$\overline{MBF1}$	O	Mail1 register flag. $\overline{MBF1}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is low. $\overline{MBF1}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and both SIZ1 and SIZ0 are high. $\overline{MBF1}$ is set high when the device is reset.
$\overline{MBF2}$	O	Mail2 register flag. $\overline{MBF2}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is low. $\overline{MBF2}$ is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. $\overline{MBF2}$ is set high when the device is reset.

Terminal Functions (Continued)

PIN NAME	I/O	DESCRIPTION
ODD/$\overline{\text{EVEN}}$	I	Odd/even parity select. Odd parity is checked on each port when ODD/$\overline{\text{EVEN}}$ is high, and even parity is checked when ODD/$\overline{\text{EVEN}}$ is low. ODD/$\overline{\text{EVEN}}$ also selects the type of parity generated for each port if parity generation is enabled for a read operation.
$\overline{\text{PEFA}}$	O (port A)	Port-A parity error flag. When any byte applied to terminals A0–A35 fails parity, $\overline{\text{PEFA}}$ is low. Bytes are organized as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/$\overline{\text{EVEN}}$ input. The parity trees used to check the A0–A35 inputs are shared by the mail2 register to generate parity if parity generation is selected by PGA. Therefore, if a mail2 read with parity generation is setup by having W/$\overline{\text{RA}}$ low, MBA high, and PGA high, the $\overline{\text{PEFA}}$ flag is forced high regardless of the state of the A0–A35 inputs.
$\overline{\text{PEFB}}$	O (port B)	Port-B parity error flag. When any valid byte applied to terminals B0–B35 fails parity, $\overline{\text{PEFB}}$ is low. Bytes are organized as B0–B8, B9–B17, B18–B26, and B27–B35, with the most significant bit of each byte serving as the parity bit. A byte is valid when it is used by the bus size selected for port B. The type of parity checked is determined by the state of the ODD/$\overline{\text{EVEN}}$ input. The parity trees used to check the B0–B35 inputs are shared by the mail1 register to generate parity if parity generation is selected by PGB. Therefore, if a mail1 read with parity generation is setup by having W/$\overline{\text{RB}}$ low, SIZ1 and SIZ0 high, and PGB high, the $\overline{\text{PEFB}}$ flag is forced high regardless of the state of the B0–B35 inputs.
PGA	I	Port-A parity generation. Parity is generated for data reads from port A when PGA is high. The type of parity generated is selected by the state of the ODD/$\overline{\text{EVEN}}$ input. Bytes are organized as A0–A8, A9–A17, A18–A26, and A27–A35. The generated parity bits are output in the most significant bit of each byte.
PGB	I	Port-B parity generation. Parity is generated for data reads from port B when PGB is high. The type of parity generated is selected by the state of the ODD/$\overline{\text{EVEN}}$ input. Bytes are organized as B0–B8, B9–B17, B18–B26, and B27–B35. The generated parity bits are output in the most significant bit of each byte.
$\overline{\text{RST}}$	I	Reset. To reset the device, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{\text{RST}}$ is low. This sets the $\overline{\text{AFA}}$, $\overline{\text{AFB}}$, $\overline{\text{MBF1}}$, and $\overline{\text{MBF2}}$ flags high and the $\overline{\text{EFA}}$, $\overline{\text{EFB}}$, $\overline{\text{AEA}}$, $\overline{\text{AEB}}$, $\overline{\text{FFA}}$, and $\overline{\text{FFB}}$ flags low. The low-to-high transition of $\overline{\text{RST}}$ latches the status of the FS1 and FS0 inputs to select almost-full flag and almost-empty flag offset.
SIZ0, SIZ1	I (port B)	Port-B bus size selects. The low-to-high transition of CLKB latches the states of SIZ0, SIZ1, and $\overline{\text{BE}}$, and the following low-to-high transition of CLKB implements the latched states as a port-B bus size. Port-B bus sizes can be long word, word, or byte. A high on both SIZ0 and SIZ1 accesses the mailbox registers for a port-B 36-bit write or read.
SW0, SW1	I (port B)	Port-B byte swap selects. At the beginning of each long word transfer, one of four modes of byte-order swapping is selected by SW0 and SW1. The four modes are no swap, byte swap, word swap, and byte-word swap. Byte-order swapping is possible with any bus-size selection.
W/$\overline{\text{RA}}$	I	Port-A write/read select. W/$\overline{\text{RA}}$ high selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{\text{RA}}$ is high.
W/$\overline{\text{RB}}$	I	Port-B write/read select. W/$\overline{\text{RB}}$ high selects a write operation and a low selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when W/$\overline{\text{RB}}$ is high.

detailed description

reset

The SN74ABT3614 is reset by taking the reset ($\overline{\text{RST}}$) input low for at least four port-A clock (CLKA) and four port-B clock (CLKB) low-to-high transitions. The reset input can switch asynchronously to the clocks. A device reset initializes the internal read and write pointers of each FIFO and forces the full flags ($\overline{\text{FFA}}$, $\overline{\text{FFB}}$) low, the empty flags ($\overline{\text{EFA}}$, $\overline{\text{EFB}}$) low, the almost-empty flags ($\overline{\text{AEA}}$, $\overline{\text{AEB}}$) low, and the almost-full flags ($\overline{\text{AFA}}$, $\overline{\text{AFB}}$) high. A reset also forces the mailbox flags ($\overline{\text{MBF1}}$, $\overline{\text{MBF2}}$) high. After a reset, $\overline{\text{FFA}}$ is set high after two low-to-high transitions of CLKA and $\overline{\text{FFB}}$ is set high after two low-to-high transitions of CLKB. The device must be reset after power up before data is written to its memory.

A low-to-high transition on the $\overline{\text{RST}}$ input loads the almost-full and almost-empty offset register (X) with the value selected by the flag-select (FS0, FS1) inputs. The values that can be loaded into the register are shown in Table 1.

reset (continued)

Table 1. Flag Programming

FS1	FS0	$\overline{RST}$	ALMOST-FULL AND ALMOST-EMPTY FLAG OFFSET REGISTER (X)
H	H	↑	16
H	L	↑	12
L	H	↑	8
L	L	↑	4

FIFO write/read operation

The state of the port-A data (A0–A35) outputs is controlled by the port-A chip select ($\overline{CSA}$) and the port-A write/read select (W/$\overline{RA}$). The A0–A35 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is high. The A0–A35 outputs are active when both $\overline{CSA}$ and W/$\overline{RA}$ are low. Data is loaded into FIFO1 from the A0–A35 inputs on a low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is high, ENA is high, MBA is low, and $\overline{FFA}$ is high. Data is read from FIFO2 to the A0–A35 outputs by a low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is low, ENA is high, MBA is low, and $\overline{EFA}$ is high (see Table 2).

Table 2. Port-A Enable Function Table

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	A0–A35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO1 write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, FIFO2 output register	None
L	L	H	L	↑	Active, FIFO2 output register	FIFO2 read
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set $\overline{MBF2}$ high)

The state of the port-B data (B0–B35) outputs is controlled by the port-B chip select ($\overline{CSB}$) and the port-B write/read select (W/$\overline{RB}$). The B0–B35 outputs are in the high-impedance state when either $\overline{CSB}$ or W/$\overline{RB}$ is high. The B0–B35 outputs are active when both $\overline{CSB}$ and W/$\overline{RB}$ are low. Data is loaded into FIFO2 from the B0–B35 inputs on a low-to-high transition of CLKB when $\overline{CSB}$ is low, W/$\overline{RB}$ is high, ENB is high, $\overline{FFB}$ is high, and either SIZ0 or SIZ1 is low. Data is read from FIFO1 to the B0–B35 outputs by a low-to-high transition of CLKB when $\overline{CSB}$ is low, W/$\overline{RB}$ is low, ENB is high, $\overline{EFB}$ is high, and either SIZ0 or SIZ1 is low (see Table 3).

The setup and hold time constraints to the port clocks for the port chip selects ($\overline{CSA}$, $\overline{CSB}$) and write/read selects (W/$\overline{RA}$, W/$\overline{RB}$) are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is low during a clock cycle, the port chip select and write/read select can change states during the setup and hold time window of the cycle.

FIFO writer/read operation (continued)

Table 3. Port-B Enable Function Table

$\overline{CSB}$	W/$\overline{RB}$	ENB	SIZ1, SIZ0	CLKB	B0–B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	One, both low	↑	In high-impedance state	FIFO2 write
L	H	H	Both high	↑	In high-impedance state	Mail2 write
L	L	L	One, both low	X	Active, FIFO1 output register	None
L	L	H	One, both low	↑	Active, FIFO1 output register	FIFO1 read
L	L	L	Both high	X	Active, mail1 register	None
L	L	H	Both high	↑	Active, mail1 register	Mail1 read (set $\overline{MBF1}$ high)

synchronized FIFO flags

Each FIFO flag is synchronized to its port clock through two flip-flop stages. This is done to improve flag reliability by reducing the probability of metastable events on the output when CLKA and CLKB operate asynchronously to one another (see the application report *Metastability Performance of Clocked FIFOs* in the 1994 *High-Performance FIFO Memories Data Book*, literature #SCAD003B). $\overline{EFA}$, $\overline{AEA}$, $\overline{FFA}$, and $\overline{AFA}$ are synchronized to CLKA. $\overline{EFB}$, $\overline{AEB}$, $\overline{FFB}$, and $\overline{AFB}$ are synchronized to CLKB. Tables 4 and 5 show the relationship of each port flag to FIFO1 and FIFO2.

Table 4. FIFO1 Flag Operation

NUMBER OF 36-BIT WORDS IN FIFO1†	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA	
	$\overline{EFB}$	$\overline{AEB}$	$\overline{AFA}$	$\overline{FFA}$
0	L	L	H	H
1 to X	H	L	H	H
(X + 1) to [64 – (X + 1)]	H	H	H	H
(64 – X) to 63	H	H	L	H
64	H	H	L	L

Table 5. FIFO2 Flag Operation

NUMBER OF 36-BIT WORDS IN FIFO2†	SYNCHRONIZED TO CLKA		SYNCHRONIZED TO CLKB	
	$\overline{EFA}$	$\overline{AEA}$	$\overline{AFB}$	$\overline{FFB}$
0	L	L	H	H
1 to X	H	L	H	H
(X + 1) to [64 – (X + 1)]	H	H	H	H
(64 – X) to 63	H	H	L	H
64	H	H	L	L

† X is the value in the almost-empty flag and almost-full flag offset register.

empty flags ($\overline{EFA}$, $\overline{EFB}$)

The empty flag of a FIFO is synchronized to the port clock that reads data from its array. When the empty flag is high, new data can be read to the FIFO output register. When the empty flag is low, the FIFO is empty and attempted FIFO reads are ignored. When reading FIFO1 with a byte or word size on port B, $\overline{EFB}$ is set low when the fourth byte or second word of the last long word is read.

The read pointer of a FIFO is incremented each time a new word is clocked to the output register. The state machine that controls an empty flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. A word written to a FIFO can be read to the FIFO output register in a minimum of three cycles of the empty flag synchronizing clock; therefore, an empty flag is low if a word in memory is the next data to be sent to the FIFO output register and two cycles of the port clock that reads data from the FIFO have not elapsed since the time the word was written. The empty flag of the FIFO is set high by the second low-to-high transition of the synchronizing clock, and the new data word can be read to the FIFO output register in the following cycle.

A low-to-high transition on an empty flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{sk1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 13 and 14).

full flags ($\overline{FFA}$, $\overline{FFB}$)

The full flag of a FIFO is synchronized to the port clock that writes data to its array. When the full flag is high, a memory location is free in the SRAM to receive new data. No memory locations are free when the full flag is low and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, the write pointer is incremented. The state machine that controls a full flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is full, full–1, or full–2. From the time a word is read from a FIFO, the previous memory location is ready to be written in a minimum of three cycles of the full flag synchronizing clock. Therefore, a full flag is low if less than two cycles of the full flag synchronizing clock have elapsed since the next memory write location has been read. The second low-to-high transition on the full flag synchronizing clock after the read sets the full flag high and data can be written in the following clock cycle.

A low-to-high transition on a full flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{sk1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 15 and 16).

almost-empty flags ($\overline{AEA}$, $\overline{AEB}$)

The almost-empty flag of a FIFO is synchronized to the port clock that reads data from its array. The state machine that controls an almost-empty flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see reset above). An almost-empty flag is low when the FIFO contains X or less long words in memory and is high when the FIFO contains (X + 1) or more long words.

Two low-to-high transitions of the almost-empty flag synchronizing clock are required after a FIFO write for the almost-empty flag to reflect the new level of fill; therefore, the almost-empty flag of a FIFO containing (X + 1) or more long words remains low if two cycles of the synchronizing clock have not elapsed since the write that filled the memory to the (X + 1) level. An almost-empty flag is set high by the second low-to-high transition of the synchronizing clock after the FIFO write that fills memory to the (X + 1) level. A low-to-high transition of an almost-empty flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the write that fills the FIFO to (X + 1) long words. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figures 17 and 18).

almost-full flags ($\overline{AFA}$, $\overline{AFB}$)

The almost-full flag of a FIFO is synchronized to the port clock that writes data to its array. The state machine that controls an almost-full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost full, almost full–1, or almost full–2. The almost-full state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see reset above). An almost-full flag is low when the FIFO contains (64 – X) or more long words in memory and is high when the FIFO contains [64 – (X + 1)] or less long words.

Two low-to-high transitions of the almost-full flag synchronizing clock are required after a FIFO read for the almost-full flag to reflect the new level of fill; therefore, the almost-full flag of a FIFO containing [64 – (X + 1)] or less words remains low if two cycles of the synchronizing clock have not elapsed since the read that reduced the number of long words in memory to [64 – (X + 1)]. An almost-full flag is set high by the second low-to-high transition of the synchronizing clock after the FIFO read that reduces the number of long words in memory to [64 – (X + 1)]. A low-to-high transition of an almost-full flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the read that reduces the number of long words in memory to [64 – (X + 1)]. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figures 19 and 20).

mailbox registers

Each FIFO has a 36-bit bypass register to pass command and control information between port A and port B without putting it in queue. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A low-to-high transition on CLKA writes A0–A35 data to the mail1 register when a port-A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA, and MBA is high. A low-to-high transition on CLKB writes B0–B35 data to the mail2 register when a port-B write is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB and both SIZ0 and SIZ1 are high. Writing data to a mail register sets the corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) low. Attempted writes to a mail register are ignored while the mail flag is low.

When the port-A data outputs (A0–A35) are active, the data on the bus comes from the FIFO2 output register when MBA is low and from the mail2 register when MBA is high. When the port-B data outputs (B0–B35) are active, the data on the bus comes from the FIFO1 output register when either one or both SIZ1 and SIZ0 are low and from the mail2 register when both SIZ1 and SIZ0 are high. The mail1 register flag ($\overline{MBF1}$) is set high by a rising CLKB edge when a port-B read is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB and both SIZ1 and SIZ0 are high. The mail2 register flag ($\overline{MBF2}$) is set high by a rising CLKA edge when a port-A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and MBA is high. The data in the mail register remains intact after it is read and changes only when new data is written to the register.

dynamic bus sizing

The port-B bus can be configured in a 36-bit long word, 18-bit word, or 9-bit byte format for data read from FIFO1 or written to FIFO2. Word- and byte-size bus selections can utilize the most significant bytes of the bus (big endian) or least significant bytes of the bus (little endian). Port-B bus size can be changed dynamically and synchronous to CLKB to communicate with peripherals of various bus widths.

The levels applied to the port-B bus size select (SIZ0, SIZ1) inputs and the big-endian select ($\overline{BE}$) input are stored on each CLKB low-to-high transition. The stored port-B bus size selection is implemented by the next rising edge on CLKB according to Figure 1.

Only 36-bit long-word data is written to or read from the two FIFO memories on the SN74ABT3614. Bus-matching operations are done after data is read from the FIFO1 RAM and before data is written to the FIFO2 RAM. Port-B bus sizing does not apply to mail-register operations.

dynamic bus sizing (continued)

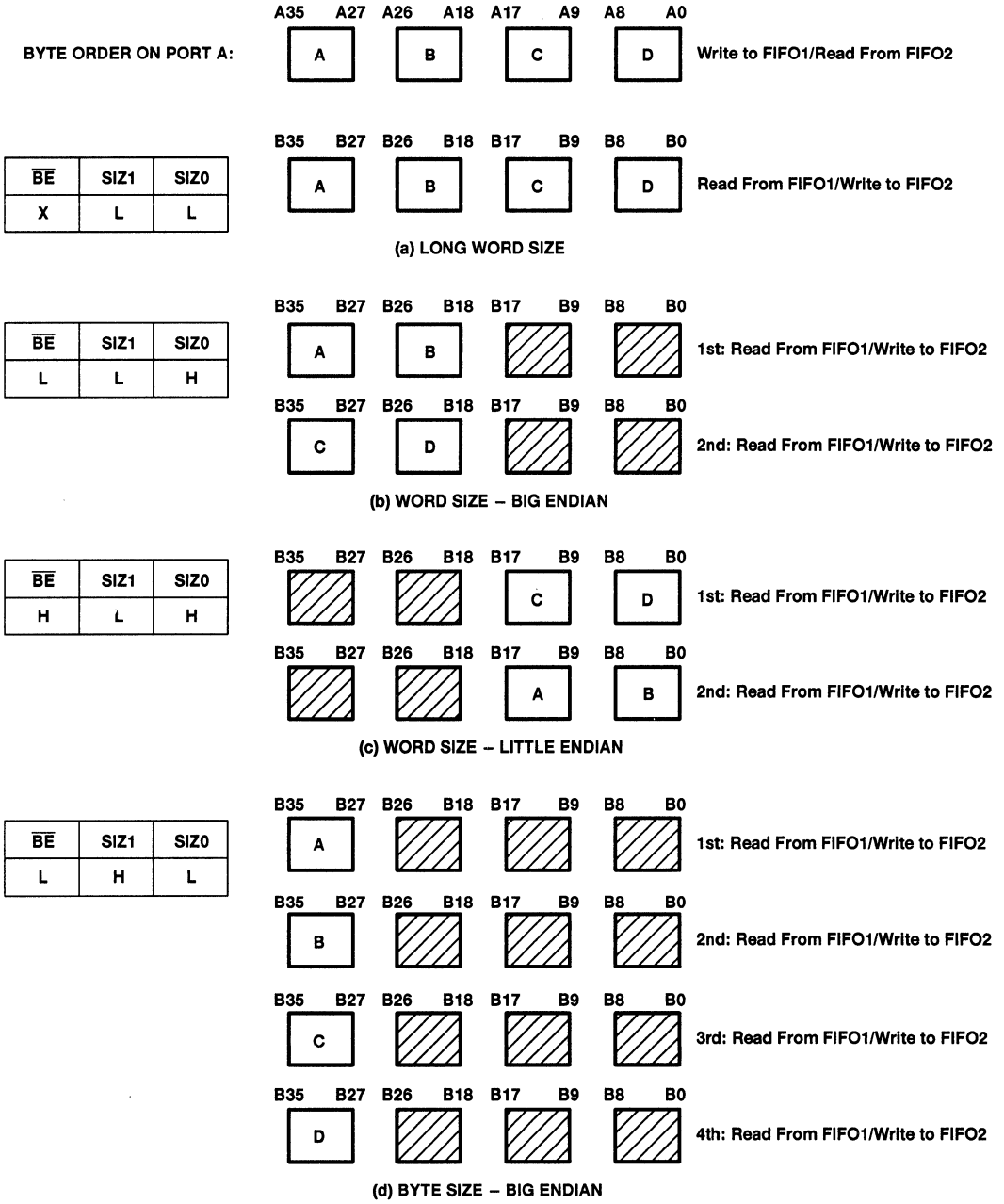
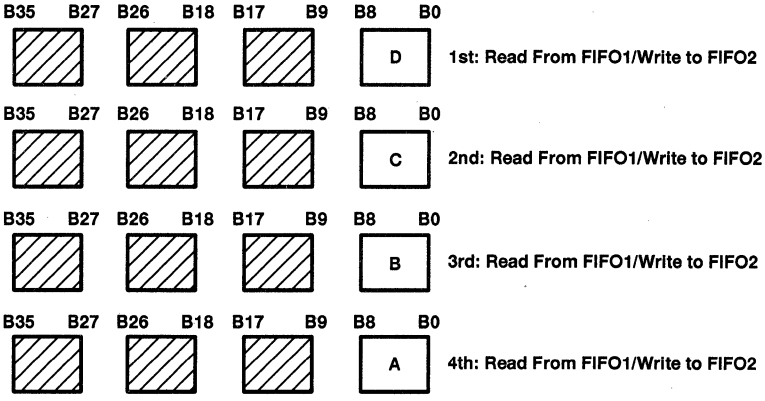


Figure 1. Dynamic Bus Sizing

dynamic bus sizing (continued)

$\overline{BE}$	SIZ1	SIZ0
H	H	L



(e) BYTE SIZE – LITTLE ENDIAN

Figure 1. Dynamic Bus Sizing (continued)

bus-matching FIFO1 reads

Data is read from the FIFO1 RAM in 36-bit long-word increments. If a long-word bus size is implemented, the entire long word immediately shifts to the FIFO1 output register. If byte or word size is implemented on port B, only the first one or two bytes appear on the selected portion of the FIFO1 output register with the rest of the long word stored in auxiliary registers. In this case, subsequent FIFO1 reads with the same bus-size implementation output the rest of the long word to the FIFO1 output register in the order shown by Figure 1.

Each FIFO1 read with a new bus-size implementation automatically unloads data from the FIFO1 RAM to its output register and auxiliary registers. Therefore, implementing a new port-B bus size and performing a FIFO1 read before all bytes or words stored in the auxiliary registers have been read results in a loss of the unread long-word data.

When reading data from FIFO1 in byte or word format, the unused B0–B35 outputs remain inactive but static with the unused FIFO1 output register bits holding the last data value to decrease power consumption.

bus-matching FIFO2 writes

Data is written to the FIFO2 RAM in 36-bit long-word increments. FIFO2 writes, with a long-word bus size, immediately store each long word in FIFO2 RAM. Data written to FIFO2 with a byte or word bus size stores the initial bytes or words in auxiliary registers. The CLKB rising edge that writes the fourth byte or the second word of long word to FIFO2 also stores the entire long word in FIFO2 RAM. The bytes are arranged in the manner shown in Figure 1.

Each FIFO2 write with a new bus-size implementation resets the state machine that controls the data flow from the auxiliary registers to the FIFO2 RAM. Therefore, implementing a new bus size and performing a FIFO2 write before bytes or words stored in the auxiliary registers have been loaded to FIFO2 RAM results in a loss of data.

port-B mail register access

In addition to selecting port-B bus sizes for FIFO reads and writes, the port-B bus size select (SIZ0, SIZ1) inputs also access the mail registers. When both SIZ0 and SIZ1 are high, the mail1 register is accessed for a port-B long-word read and the mail2 register is accessed for a port-B long-word write. The mail register is accessed immediately and any bus-sizing operation that can be underway is unaffected by the the mail register access. After the mail register access is complete, the previous FIFO access can resume in the next CLKB cycle. The logic diagram in Figure 2 shows the previous bus-size selection is preserved when the mail registers are accessed from port B. A port-B bus size is implemented on each rising CLKB edge according to the states of SIZ0_Q, SIZ1_Q, and $\overline{BE}$_Q.

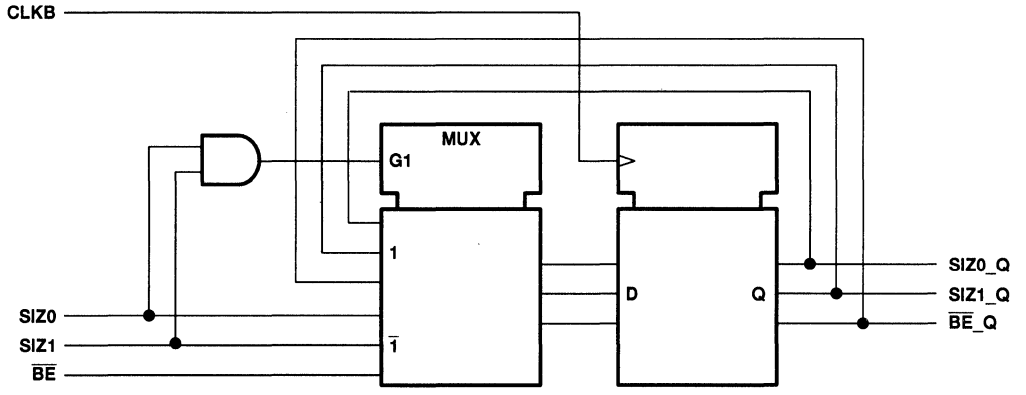


Figure 2. Logic Diagram for SIZ0, SIZ1, and $\overline{BE}$ Register

byte swapping

The byte-order arrangement of data read from FIFO1 or data written to FIFO2 can be changed synchronous to the rising edge of CLKB. Byte-order swapping is not available for mail register data. Four modes of byte-order swapping (including no swap) can be done with any data port size selection. The order of the bytes are rearranged within the long word, but the bit order within the bytes remains constant.

Byte arrangement is chosen by the port-B swap select (SW0, SW1) inputs on a CLKB rising edge that reads a new long word from FIFO1 or writes a new long word to FIFO2. The byte order chosen on the first byte or first word of a new long word read from FIFO1 or written to FIFO2 is maintained until the entire long word is transferred, regardless of the SW0 and SW1 states during subsequent writes or reads. Figure 3 is an example of the byte-order swapping available for long words. Performing a byte swap and bus size simultaneously for a FIFO1 read first rearranges the bytes as shown in Figure 3, then outputs the bytes as shown in Figure 1. Simultaneous bus-sizing and byte-swapping operations for FIFO2 writes, first loads the data according to Figure 1, then swaps the bytes as shown in Figure 3 when the long word is loaded to FIFO2 RAM.

byte swapping (continued)

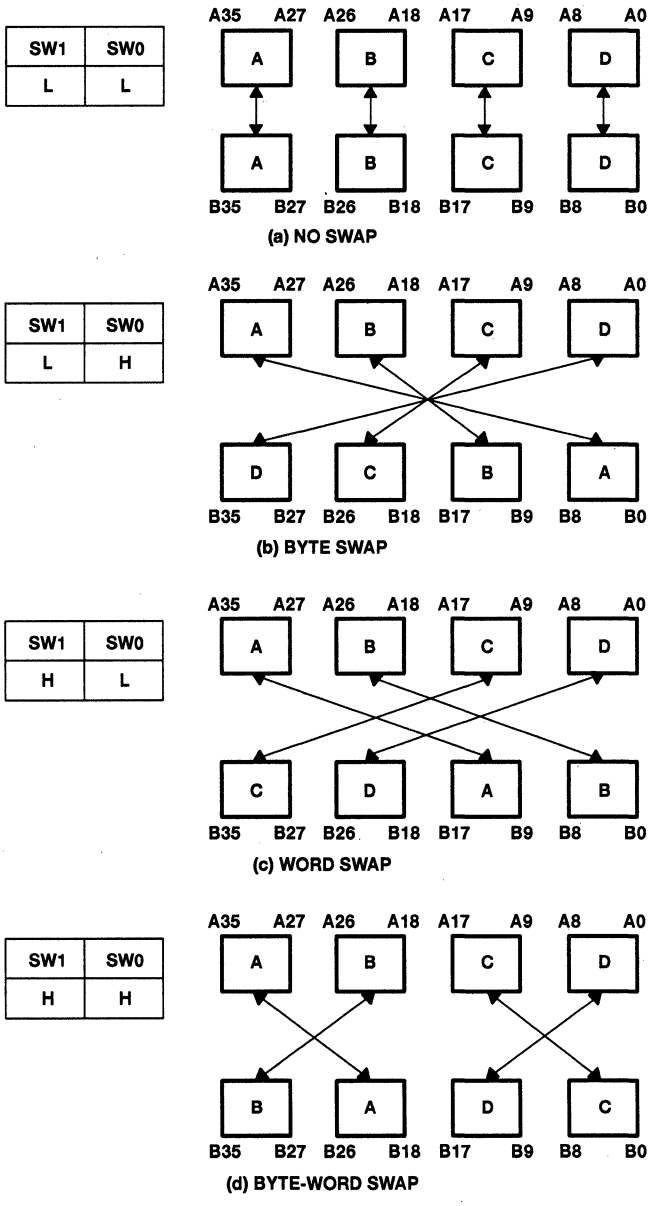


Figure 3. Byte Swapping (Long-Word Size Example)

parity checking

The port-A data inputs (A0–A35) and port-B data inputs (B0–B35) each have four parity trees to check the parity of incoming (or outgoing) data. A parity failure on one or more bytes of the port-A data bus is reported by a low level on the port-A parity error flag ($\overline{\text{PEFA}}$). A parity failure on one or more bytes of the port-B data inputs that are valid for the bus-size implementation is reported by a low level on the port-B parity error flag ($\overline{\text{PEFB}}$). Odd or even parity checking can be selected, and the parity error flags can be ignored if this feature is not desired.

Parity status is checked on each input bus according to the level of the odd/even parity (ODD/$\overline{\text{EVEN}}$) select input. A parity error on one or more valid bytes of a port is reported by a low level on the corresponding port parity error flag ($\overline{\text{PEFA}}$, $\overline{\text{PEFB}}$) output. Port-A bytes are arranged as A0–A8, A9–A17, A18–A26, and A27–A35. Port-B bytes are arranged as B0–B8, B9–B17, B18–B26, and B27–B35, and its valid bytes are those used in a port-B bus-size implementation. When odd/even parity is selected, a port parity error flag ($\overline{\text{PEFA}}$, $\overline{\text{PEFB}}$) is low if any valid byte on the port has an odd/even number of low levels applied to the bits.

The four parity trees used to check the A0–A35 inputs are shared by the mail2 register when parity generation is selected for port-A reads (PGA = high). When a port-A read from the mail2 register with parity generation is selected with $\overline{\text{CSA}}$ low, ENA high, W/$\overline{\text{RA}}$ low, MBA high, and PGA high, the port-A parity error flag ($\overline{\text{PEFA}}$) is held high regardless of the levels applied to the A0–A35 inputs. Likewise, the parity trees used to check the B0–B35 inputs are shared by the mail1 register when parity generation is selected for port-B reads (PGB = high). When a port-B read from the mail1 register with parity generation is selected with $\overline{\text{CSB}}$ low, ENB high, and W/$\overline{\text{RB}}$ low, both SIZ0 and SIZ1 high, and PGB high, the port-B parity error flag ($\overline{\text{PEFB}}$) is held high regardless of the levels applied to the B0–B35 inputs.

parity generation

A high level on the port-A parity generate select (PGA) or port-B parity generate select (PGB) enables the SN74ABT3614 to generate parity bits for port reads from a FIFO or mailbox register. Port-A bytes are arranged as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit of each byte used as the parity bit. Port-B bytes are arranged as B0–B8, B9–B17, B18–B26, and B27–B35, with the most significant bit of each byte used as the parity bit. A write to a FIFO or mail register stores the levels applied to all nine inputs of a byte regardless of the state of the parity generate select (PGA, PGB) inputs. When data is read from a port with parity generation selected, the lower eight bits of each byte are used to generate a parity bit according to the level on the ODD/$\overline{\text{EVEN}}$ select. The generated parity bits are substituted for the levels orginally written to the most significant bits of each byte as the word is read to the data outputs.

Parity bits for FIFO data are generated after the data is read from SRAM and before the data is written to the output register. Therefore, the port-A parity generate select (PGA) and odd/even parity select (ODD/$\overline{\text{EVEN}}$) have setup and hold time constraints to the port-A clock (CLKA) and the port-B parity generate select (PGB) and ODD/$\overline{\text{EVEN}}$ have setup and hold-time constraints to the port-B clock (CLKB). These timing constraints only apply for a rising clock edge used to read a new long word to the FIFO output register.

The circuit used to generate parity for the mail1 data is shared by the port-B bus (B0–B35) to check parity and the circuit used to generate parity for the mail2 data is shared by the port-A bus (A0–A35) to check parity. The shared parity trees of a port are used to generate parity bits for the data in a mail register when the port chip select ($\overline{\text{CSA}}$, $\overline{\text{CSB}}$) is low, enable (ENA, ENB) is high, write/read select (W/$\overline{\text{RA}}$, W/$\overline{\text{RB}}$) input is low, the mail register is selected (MBA is high for port A; both SIZ0 and SIZ1 are high for port B), and port parity generate select (PGA, PGB) is high. Generating parity for mail register data does not change the contents of the register.

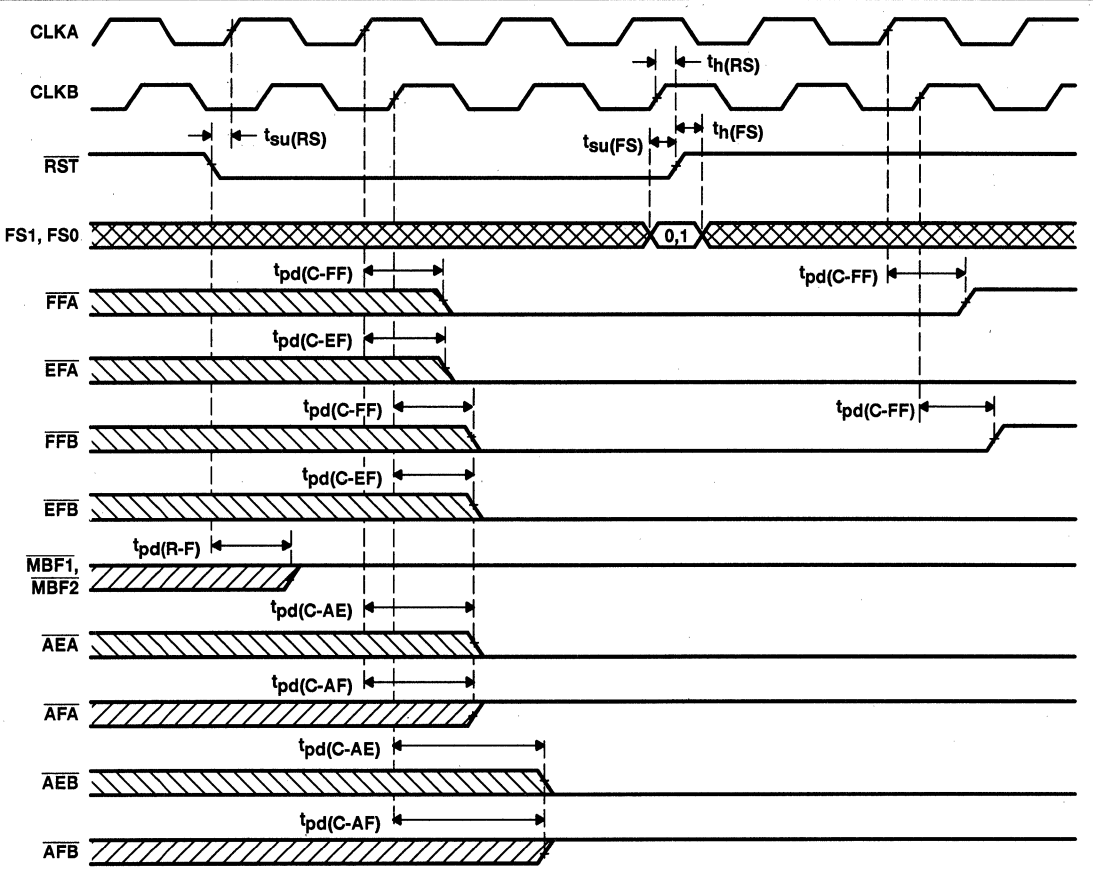
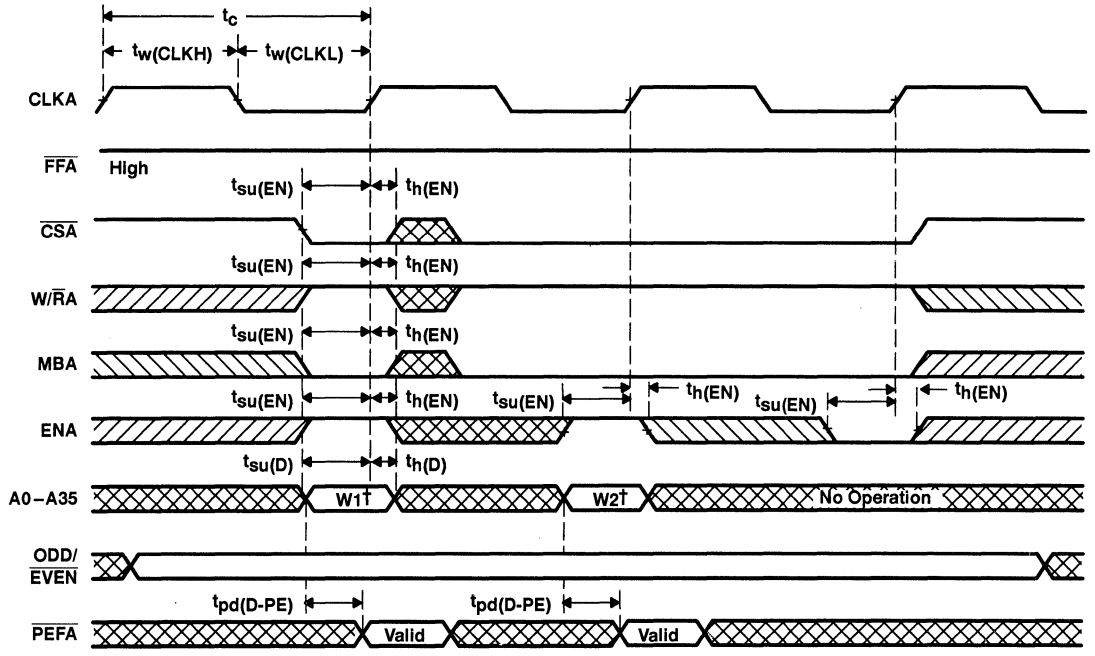
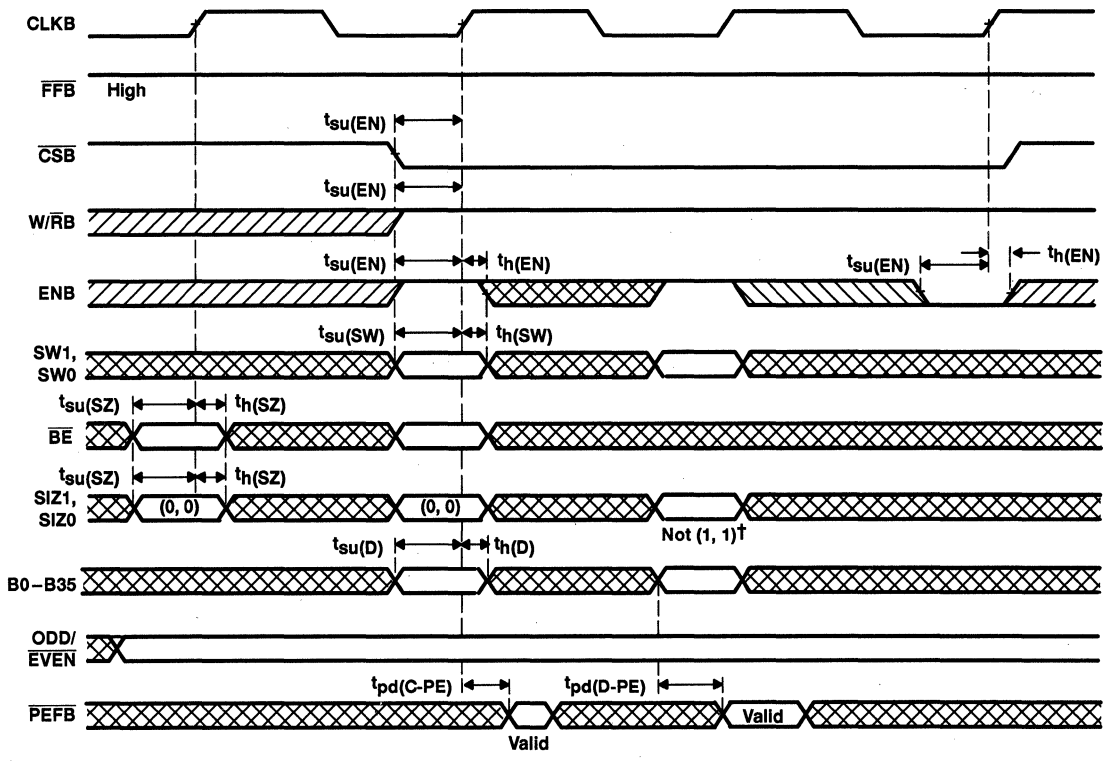


Figure 4. Device Reset Loading the X Register With the Value of Eight



† Written to FIFO1

Figure 5. Port-A Write-Cycle Timing for FIFO1

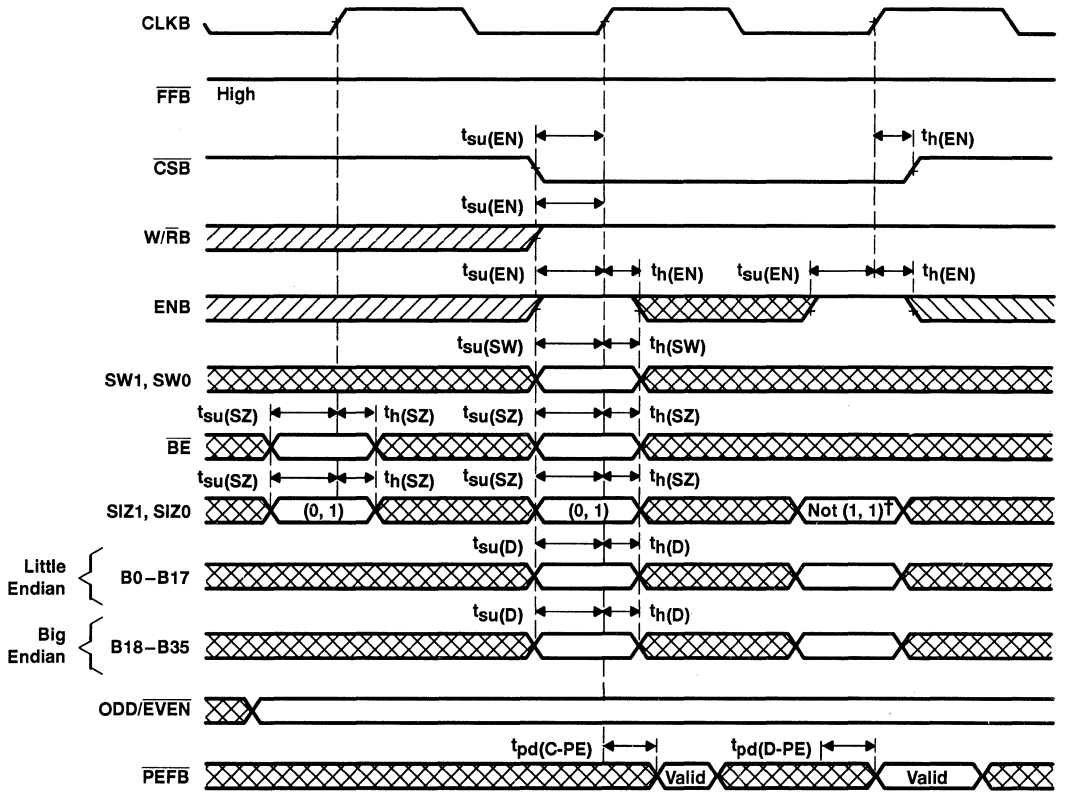


† SIZ0 = H and SIZ1 = H writes data to the mail2 register.

DATA SWAP TABLE FOR LONG-WORD WRITES TO FIFO2

SWAP MODE		DATA WRITTEN TO FIFO2				DATA READ FROM FIFO2			
SW1	SW0	B35–B27	B26–B18	B17–B9	B8–B0	A35–A27	A26–A18	A17–A9	A8–A0
L	L	A	B	C	D	A	B	C	D
L	H	D	C	B	A	A	B	C	D
H	L	C	D	A	B	A	B	C	D
H	H	B	A	D	C	A	B	C	D

Figure 6. Port-B Long-Word Write-Cycle Timing for FIFO2



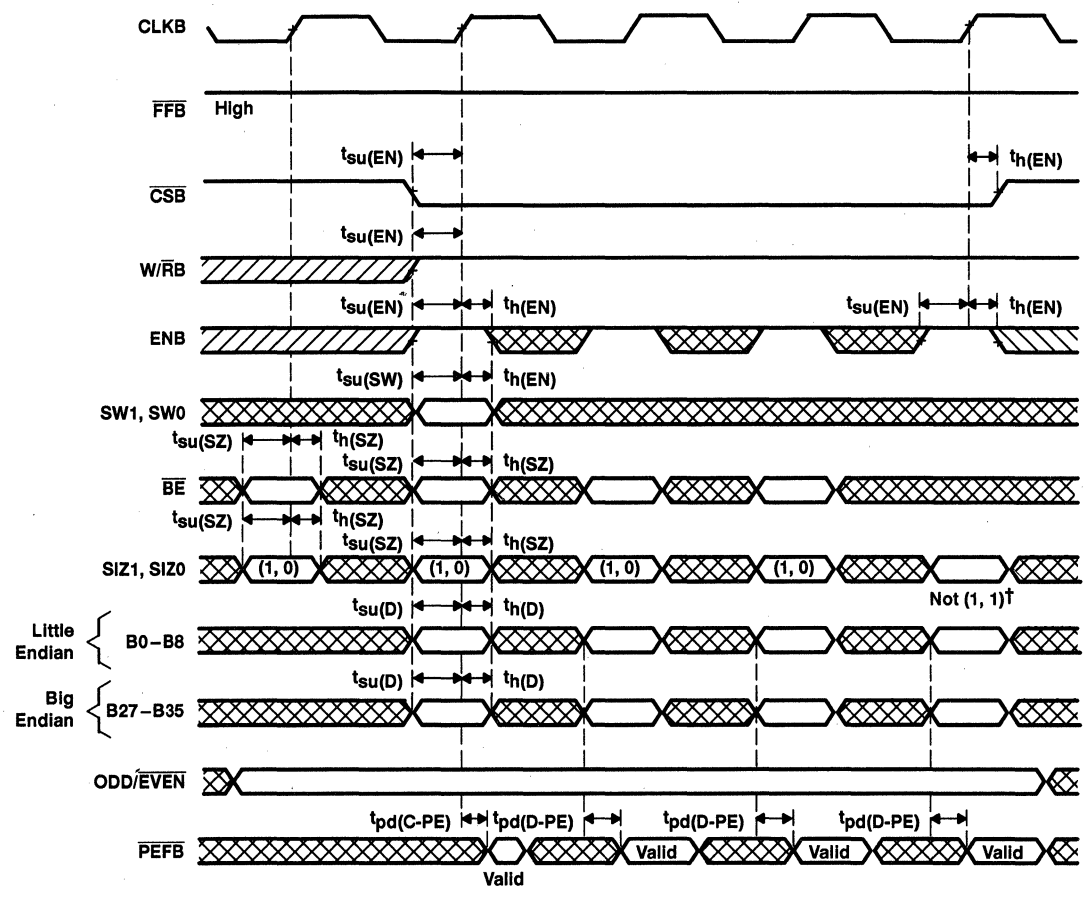
† SIZ0 = H and SIZ1 = H writes data to the mail2 register.

NOTE A: $\overline{PEFB}$ indicates parity error for the following bytes: B35–B27 and B26–B18 for big-endian bus, and B17–B9 and B8–B0 for little-endian bus.

DATA SWAP TABLE FOR WORD WRITES TO FIFO2

SWAP MODE		WRITE NO.	DATA WRITTEN TO FIFO2				DATA READ FROM FIFO2			
			BIG ENDIAN		LITTLE ENDIAN					
SW1	SW0		B35–B27	B26–B18	B17–B9	B8–B0	A35–A27	A26–A18	A17–A9	A8–A0
L	L	1	A	B	C	D	A	B	C	D
		2	C	D	A	B				
L	H	1	D	C	B	A	A	B	C	D
		2	B	A	D	C				
H	L	1	C	D	A	B	A	B	C	D
		2	A	B	C	D				
H	H	1	B	A	D	C	A	B	C	D
		2	D	C	B	A				

Figure 7. Port-B Word Write-Cycle Timing for FIFO2



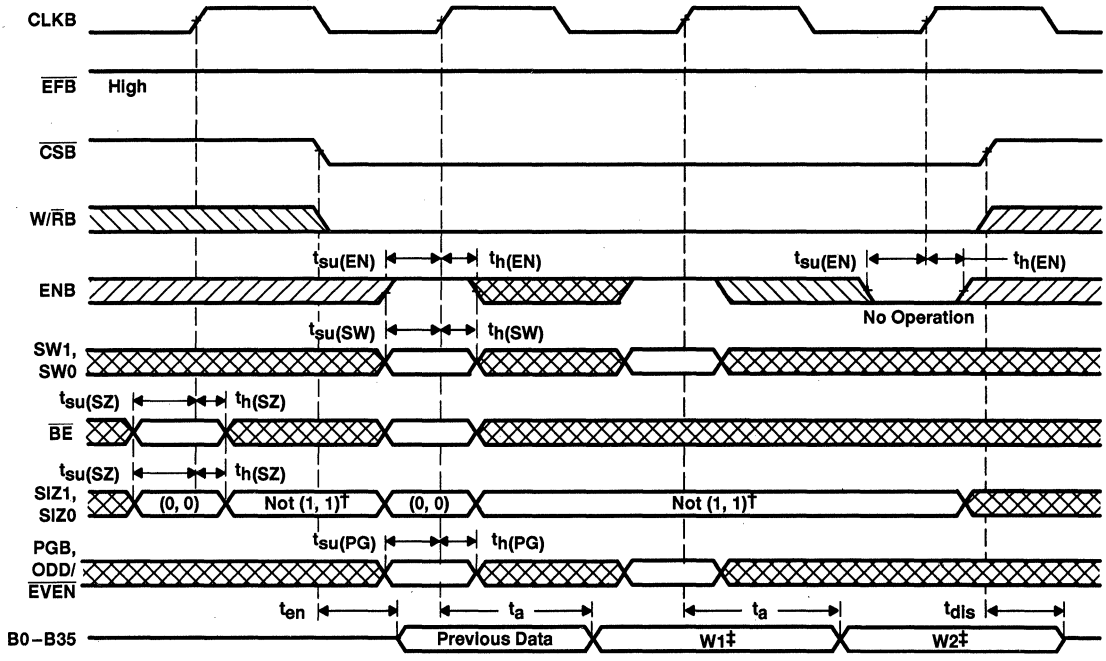
† SIZ0 = H and SIZ1 = H writes data to the mail2 register.
NOTE A: $\overline{PEFB}$ indicates parity error for the following bytes: B35–B27 for big-endian bus and B17–B9 for little-endian bus.

Figure 8. Port-B Byte Write-Cycle Timing for FIFO2

DATA SWAP TABLE FOR BYTE WRITES TO FIFO2

SWAP MODE		WRITE NO.	DATA WRITTEN TO FIFO2		DATA READ FROM FIFO2			
			BIG ENDIAN	LITTLE ENDIAN				
SW1	SW0		B35–B27	B8–B0	A35–A27	A26–A18	A17–A9	A8–A0
L	L	1	A	D	A	B	C	D
		2	B	C				
		3	C	B				
		4	D	A				
L	H	1	D	A	A	B	C	D
		2	C	B				
		3	B	C				
		4	A	D				
H	L	1	C	B	A	B	C	D
		2	D	A				
		3	A	D				
		4	B	C				
H	H	1	B	C	A	B	C	D
		2	A	D				
		3	D	A				
		4	C	B				

Figure 8. Port-B Byte Write-Cycle Timing for FIFO2 (continued)

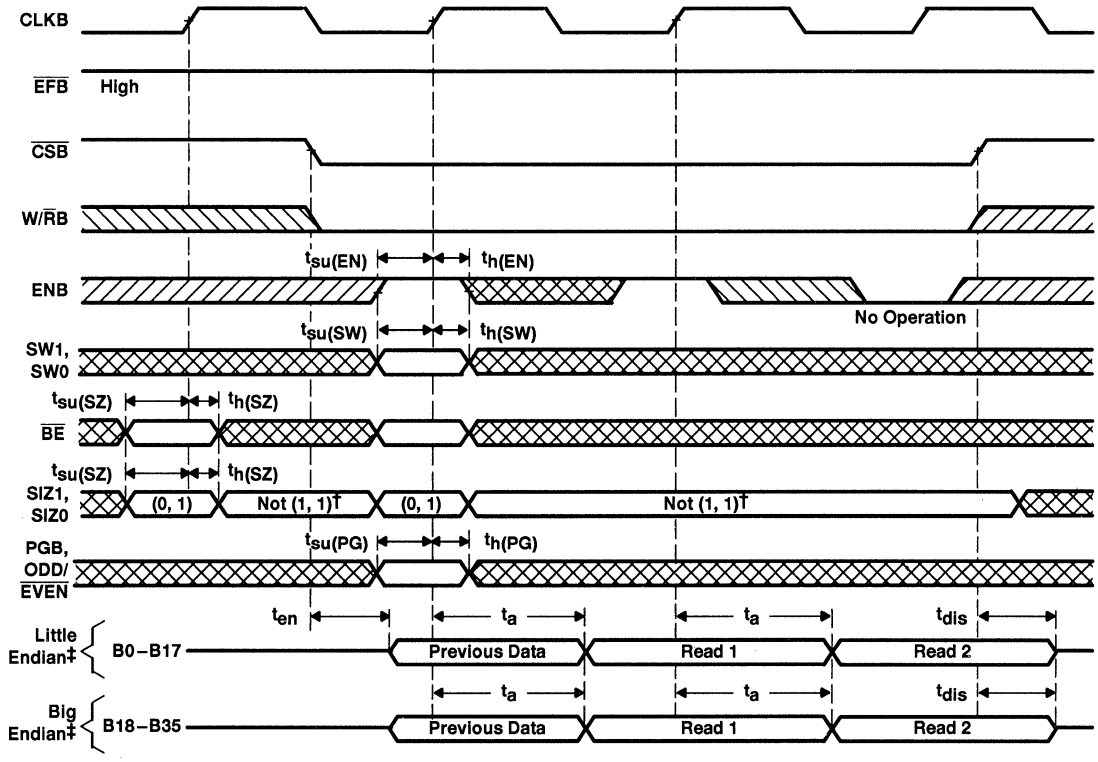


† SIZ0 = H and SIZ1 = H selects the mail1 register for output on B0–B35.
‡ Data read from FIFO1

DATA SWAP TABLE FOR LONG-WORD READS FROM FIFO1

DATA WRITTEN TO FIFO1				SWAP MODE		DATA READ FROM FIFO1			
A35–A27	A26–A18	A17–A9	A8–A0	SW1	SW0	B35–B27	B26–B18	B17–B9	B8–B0
A	B	C	D	L	L	A	B	C	D
A	B	C	D	L	H	D	C	B	A
A	B	C	D	H	L	C	D	A	B
A	B	C	D	H	H	B	A	D	C

Figure 9. Port-B Long-Word Read-Cycle Timing for FIFO1

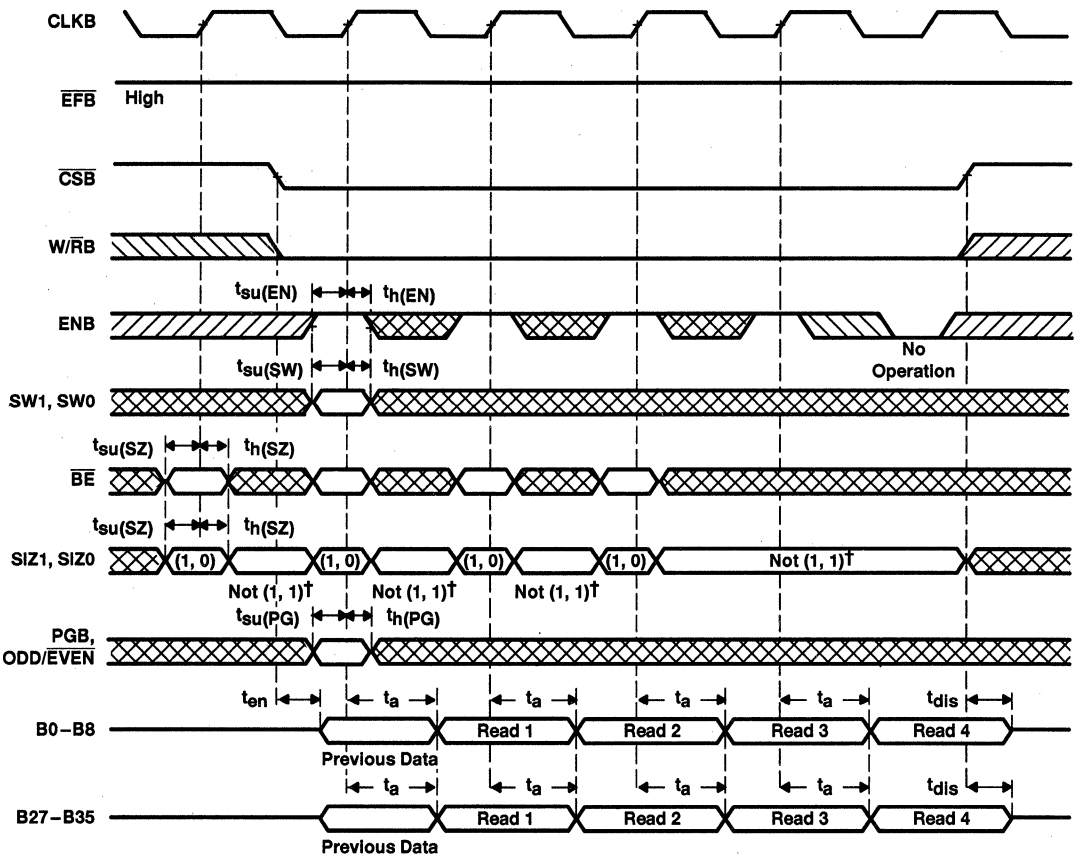


† SIZ0 = H and SIZ1 = H selects the mail1 register for output on B0–B35.
‡ Unused word B0–B17 or B18–B35 holds last FIFO1 output register data for word-size reads.

DATA SWAP TABLE FOR WORD READS FROM FIFO1

DATA WRITTEN TO FIFO1				SWAP MODE		READ NO.	DATA READ FROM FIFO1			
							BIG ENDIAN		LITTLE ENDIAN	
A35–A27	A26–A18	A17–A9	A8–A0	SW1	SW0		B35–B27	B26–B18	B17–B9	B8–B0
A	B	C	D	L	L	1 2	A C	B D	C A	D B
A	B	C	D	L	H	1 2	D B	C A	B D	A C
A	B	C	D	H	L	1 2	C A	D B	A C	B D
A	B	C	D	H	H	1 2	B D	A C	D B	C A

Figure 10. Port-B Word Read-Cycle Timing for FIFO1



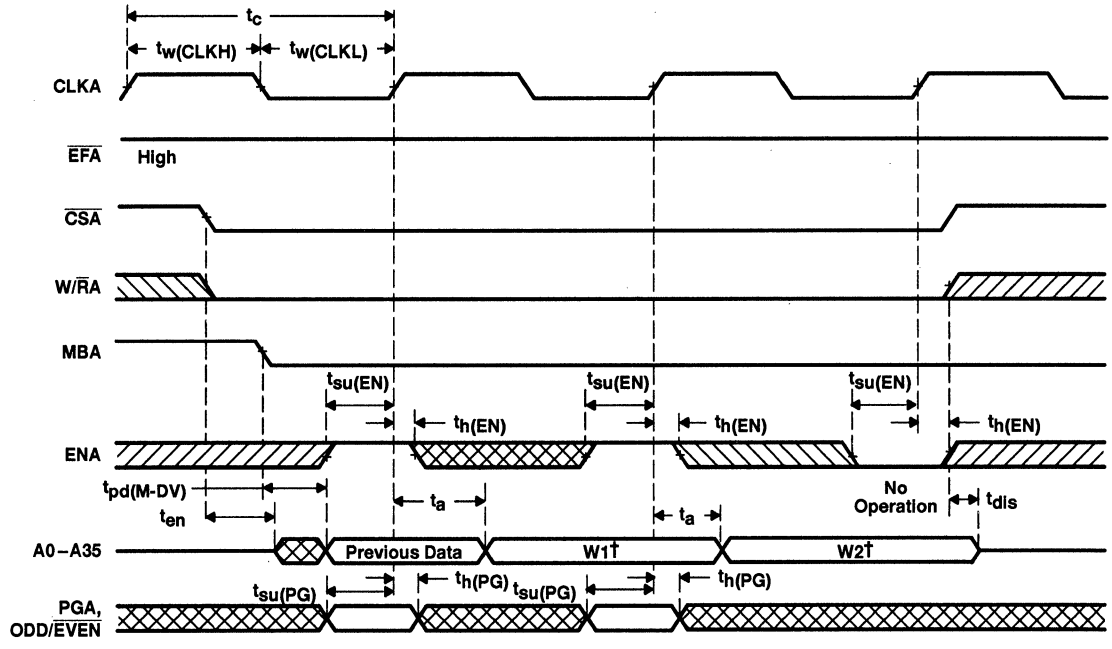
† SIZ0 = H and SIZ1 = H selects the mail1 register for output on B0–B35.
NOTE A: Unused bytes hold last FIFO1 output register data for byte-size reads.

Figure 11. Port-B Byte Read-Cycle Timing for FIFO1

DATA SWAP TABLE FOR BYTE READS FROM FIFO1

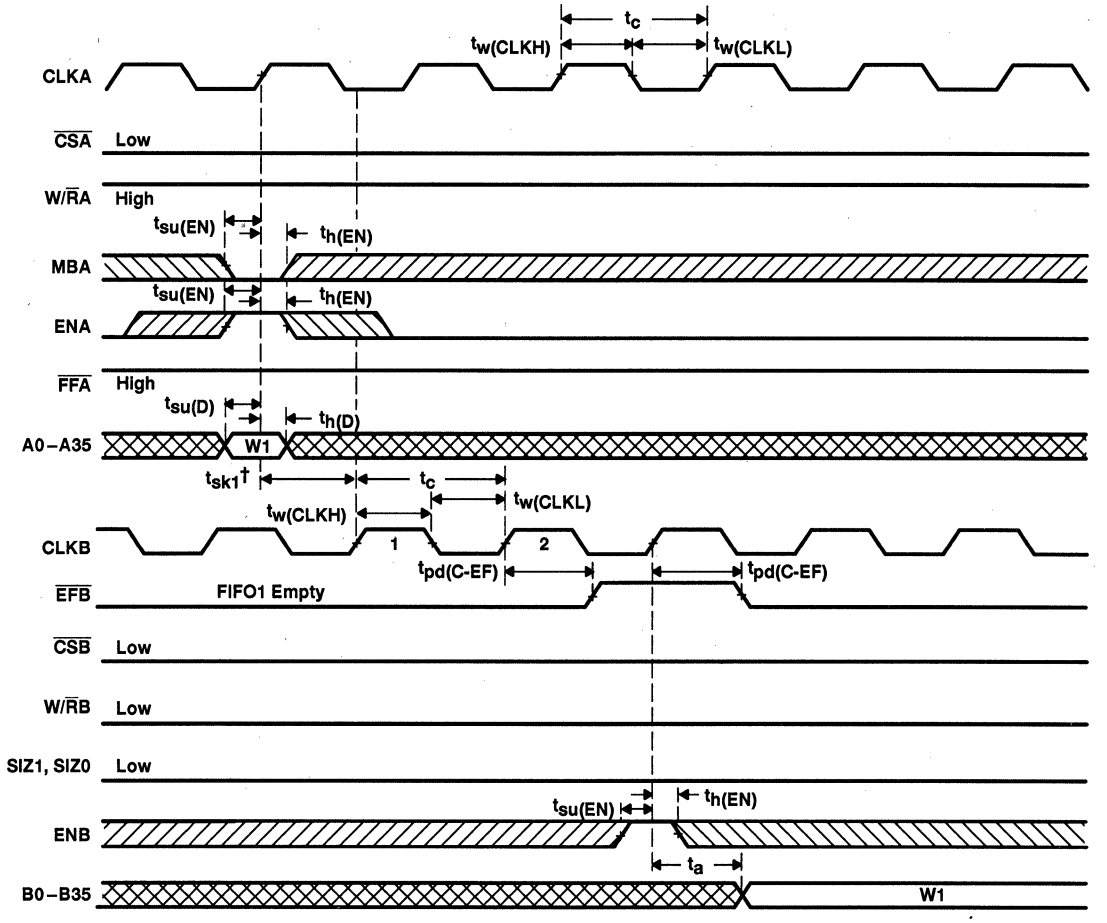
DATA WRITTEN TO FIFO1				SWAP MODE		READ NO.	DATA READ FROM FIFO1	
							BIG ENDIAN	LITTLE ENDIAN
A35–A27	A26–A18	A17–A9	A8–A0	SW1	SW0		B35–B27	B8–B0
A	B	C	D	L	L	1 2 3 4	A B C D	D C B A
A	B	C	D	L	H	1 2 3 4	D C B A	A B C D
A	B	C	D	H	L	1 2 3 4	C D A B	B A D C
A	B	C	D	H	H	1 2 3 4	B A D C	C D A B

Figure 11. Port-B Byte Read-Cycle Timing for FIFO1 (continued)



† Read from FIFO2

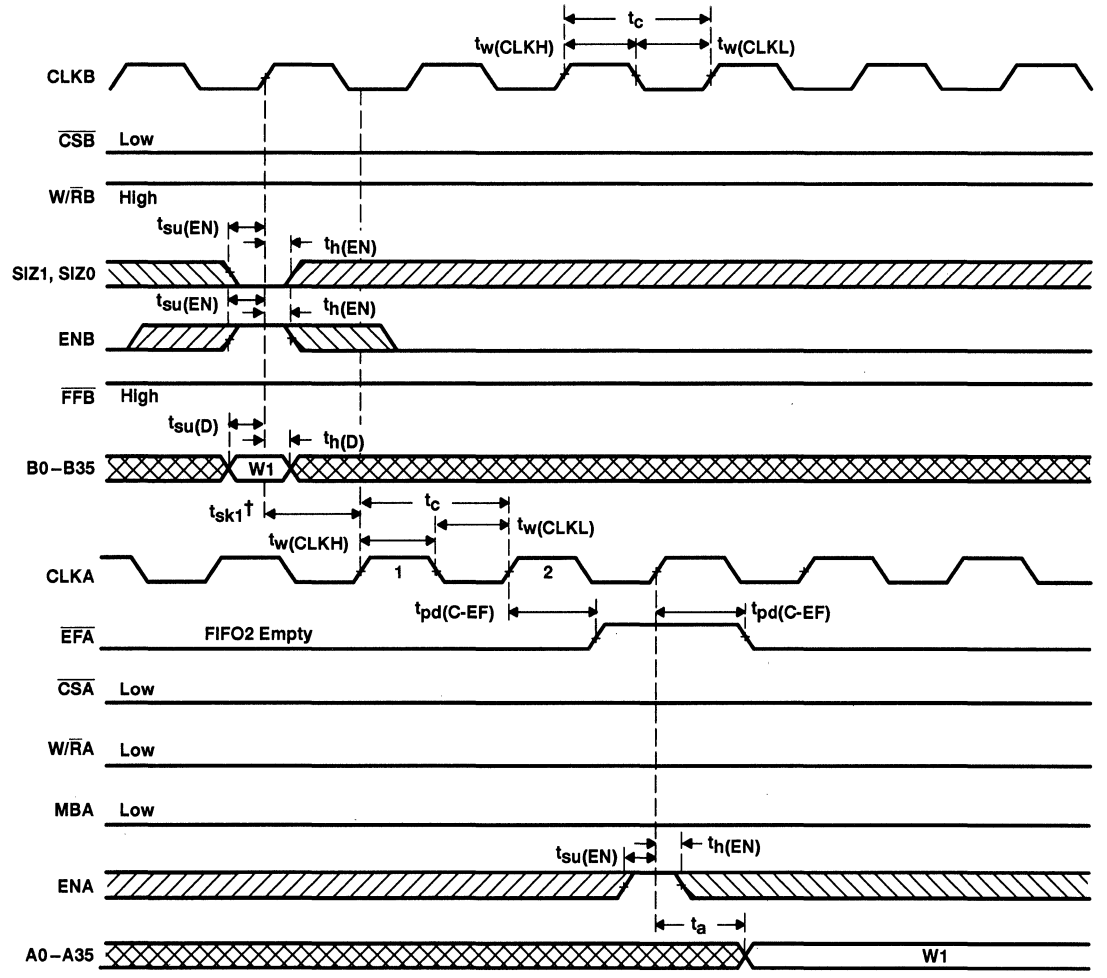
Figure 12. Port-A Read-Cycle Timing for FIFO2



† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EFB}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, the transition of $\overline{EFB}$ high may occur one CLKB cycle later than shown.

NOTE A: Port-B size of long word is selected for FIFO1 read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, $\overline{EFB}$ is set low by the last word or byte read from FIFO1, respectively.

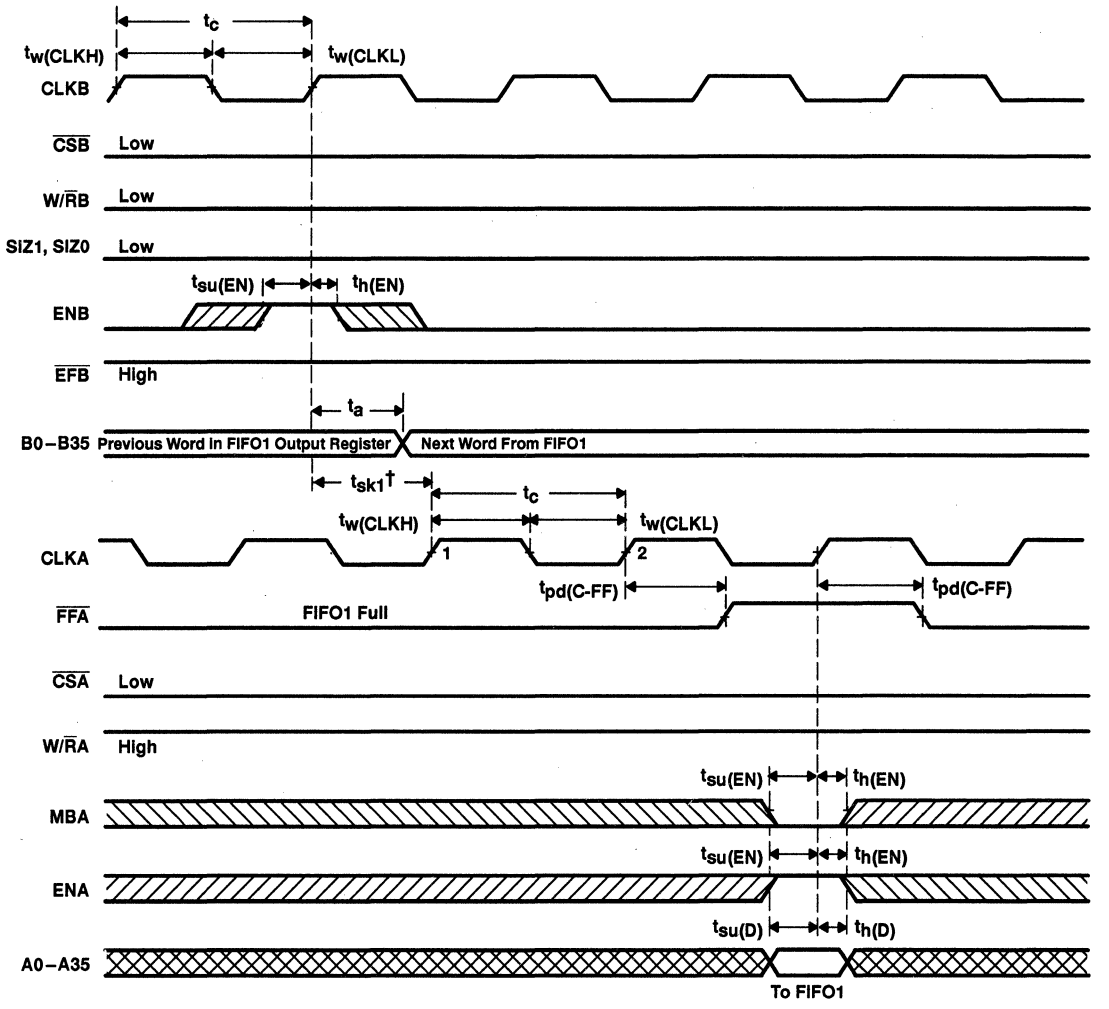
Figure 13. $\overline{EFB}$-Flag Timing and First Data Read When FIFO1 Is Empty



† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{EFA}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, the transition of $\overline{EFA}$ high may occur one CLKA cycle later than shown.

NOTE A: Port-B size of long word is selected for FIFO2 write by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, t_{sk1} is referenced to the rising CLKB edge that writes the last word or byte of the long word, respectively.

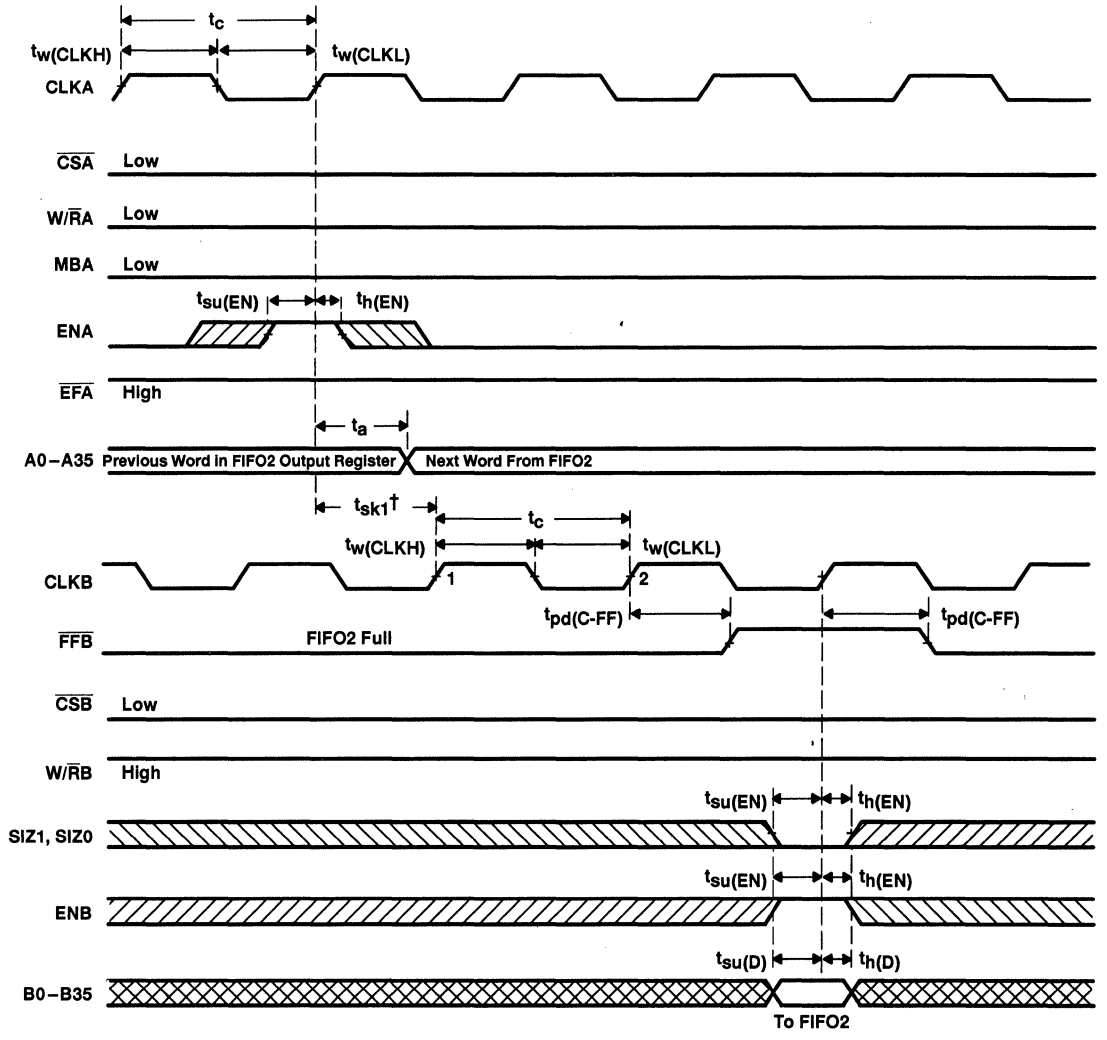
Figure 14. $\overline{EFA}$-Flag Timing and First Data Read When FIFO2 Is Empty



† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{FFA}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, $\overline{FFA}$ may transition high one CLKA cycle later than shown.

NOTE A: Port-B size of long word is selected for the FIFO1 read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, t_{sk1} is referenced from the rising CLKB edge that reads the first word or byte of the long word, respectively.

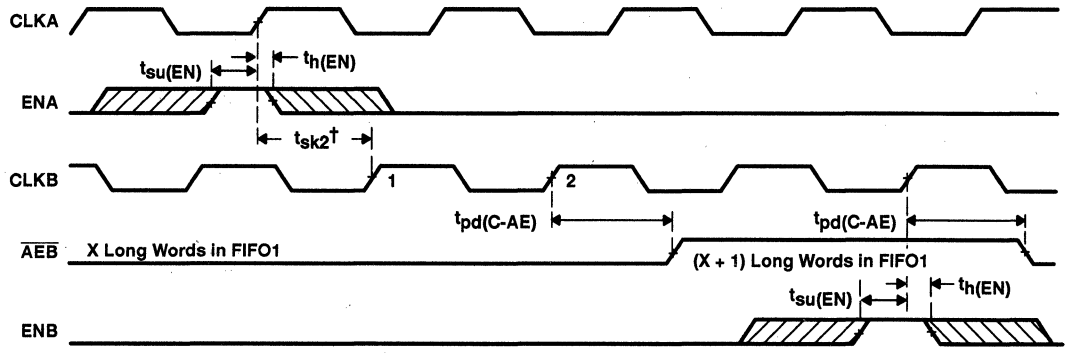
Figure 15. $\overline{FFA}$-Flag Timing and First Available Write When FIFO1 Is Full



† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{FFB}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, $\overline{FFB}$ may transition high one CLKB cycle later than shown.

NOTE A: Port-B size of long word is selected for FIFO2 write by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, $\overline{FFB}$ is set low by the last word or byte write of the long word, respectively.

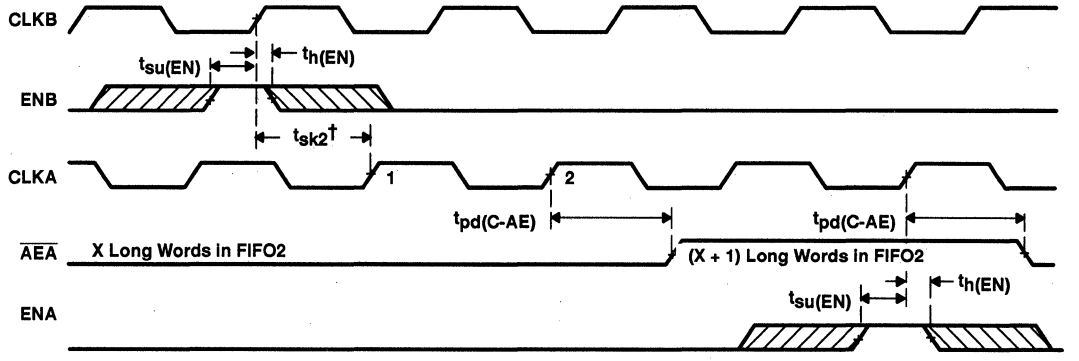
Figure 16. $\overline{FFB}$-Flag Timing and First Available Write When FIFO2 Is Full



† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AEB}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, $\overline{AEB}$ may transition high one CLKB cycle later than shown.

NOTES: A. FIFO1 write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO1 read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L).
B. Port-B size of long word is selected for FIFO1 read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, $\overline{AEB}$ is set low by the first word or byte read of the long word, respectively.

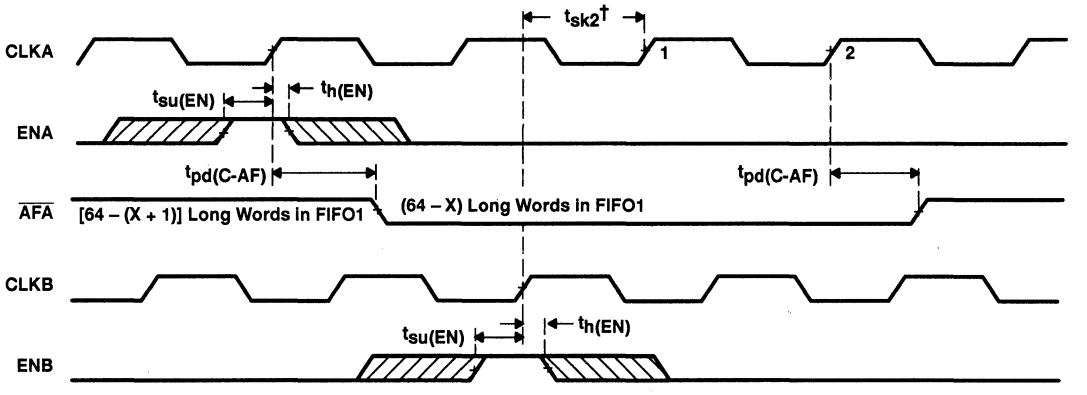
Figure 17. Timing for $\overline{AEB}$ When FIFO1 Is Almost Empty



† t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AEA}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, $\overline{AEA}$ may transition high one CLKA cycle later than shown.

NOTES: A. FIFO2 write ($\overline{CSB}$ = L, W/$\overline{RB}$ = H, MBB = L), FIFO2 read ($\overline{CSA}$ = L, W/$\overline{RA}$ = L, MBA = L).
B. Port-B size of long word is selected for FIFO2 write by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, t_{sk2} is referenced from the rising CLKB edge that writes the last word or byte of the long word, respectively.

Figure 18. Timing for $\overline{AEA}$ When FIFO2 Is Almost Empty

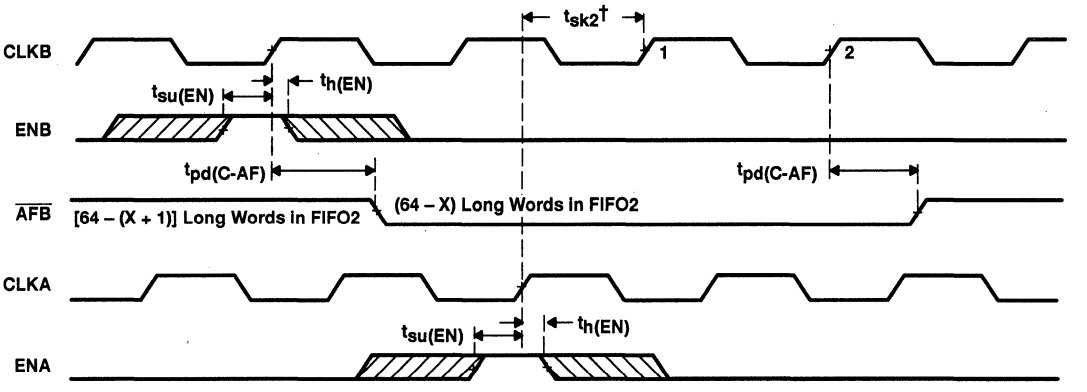


† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AFA}$ to transition high in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, $\overline{AFA}$ may transition high one CLKA cycle later than shown.

NOTES: A. FIFO1 write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO1 read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L).

B. Port-B size of long word is selected for FIFO1 read by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, t_{sk2} is referenced from the first word or byte read of the long word, respectively.

Figure 19. Timing for $\overline{AFA}$ When FIFO1 Is Almost Full

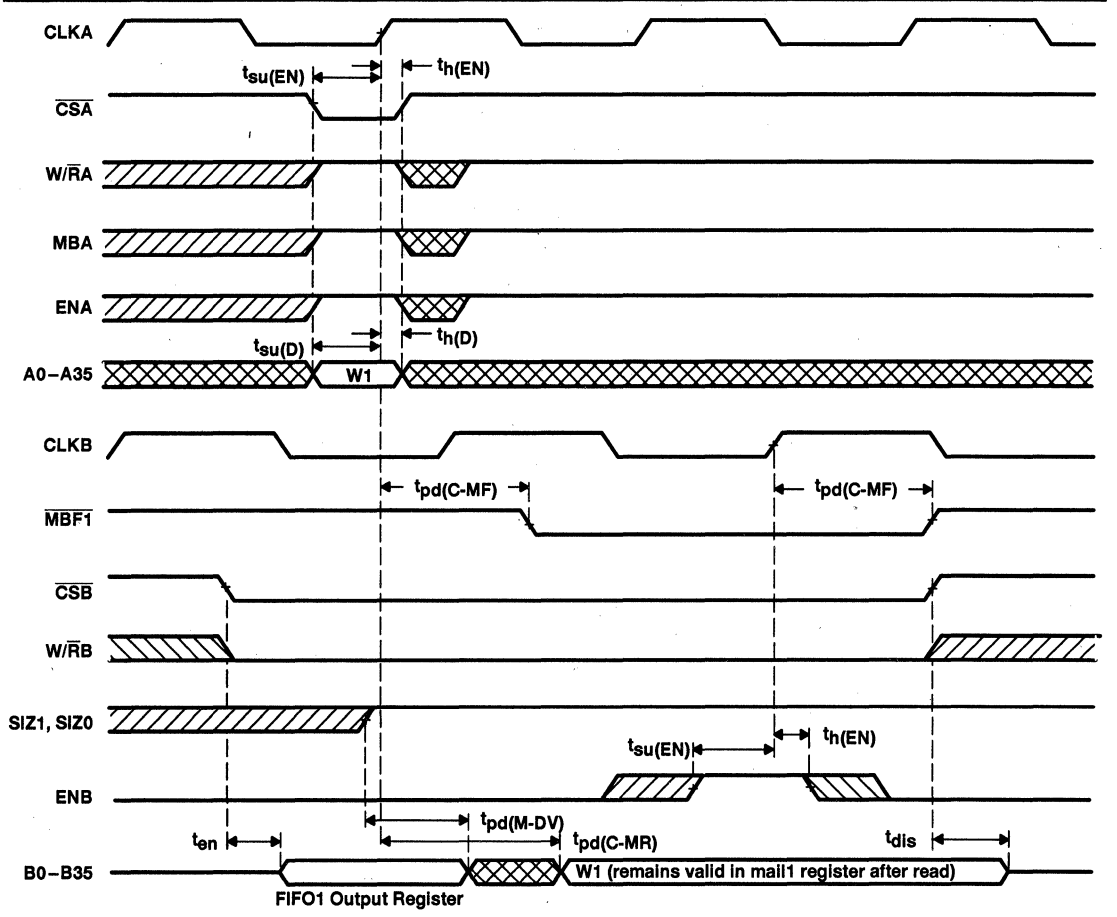


† t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AFB}$ to transition high in the next CLKB cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, $\overline{AFB}$ may transition high one CLKA cycle later than shown.

NOTES: A. FIFO2 write ($\overline{CSB}$ = L, W/$\overline{RB}$= H, MBB = L), FIFO2 read ($\overline{CSA}$ = L, W/$\overline{RA}$ = L, MBA = L).

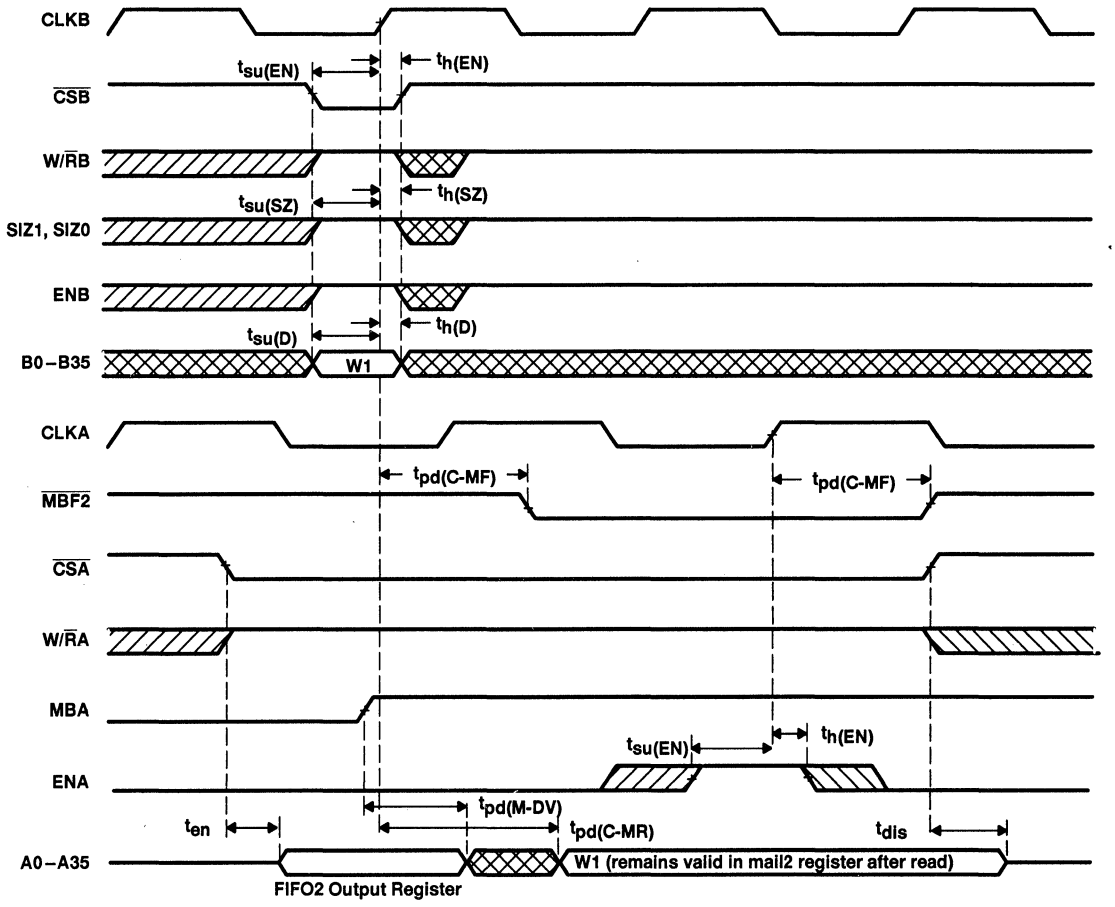
B. Port-B size of long word is selected for FIFO2 write by SIZ1 = L, SIZ0 = L. If port-B size is word or byte, $\overline{AFB}$ is set low by the last word or byte write of the long word, respectively.

Figure 20. Timing for $\overline{AFB}$ When FIFO2 Is Almost Full



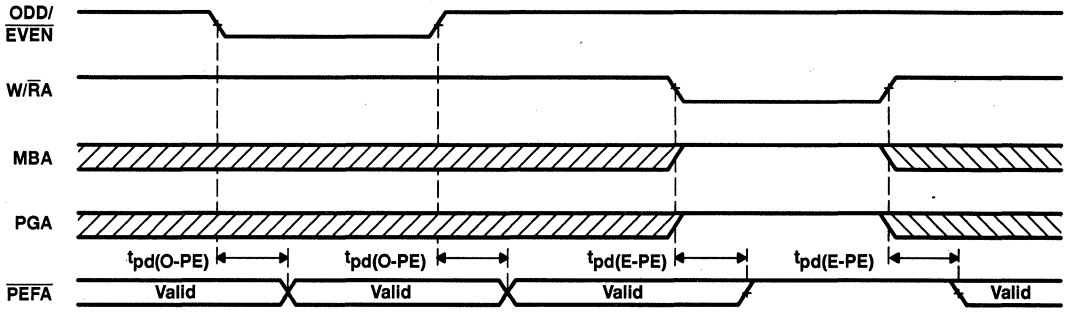
NOTE A: Port-B parity generation off (PGB = L)

Figure 21. Timing for Mail1 Register and $\overline{\text{MBF1}}$ Flag



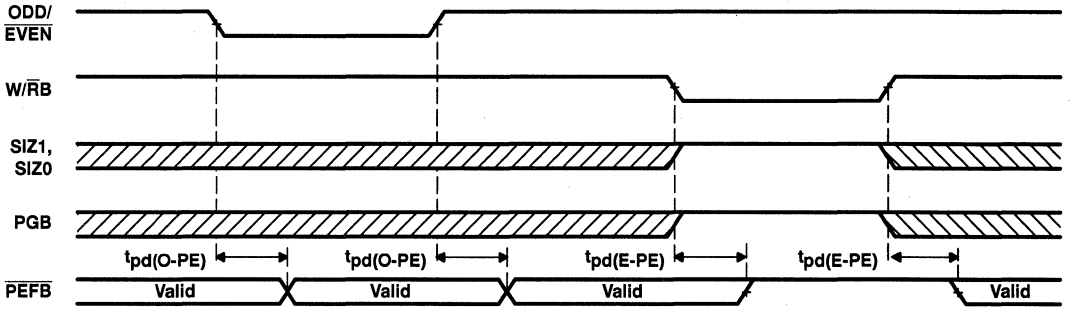
NOTE A: Port-A parity generation off (PGA = L)

Figure 22. Timing for Mail2 Register and $\overline{\text{MBF2}}$ Flag



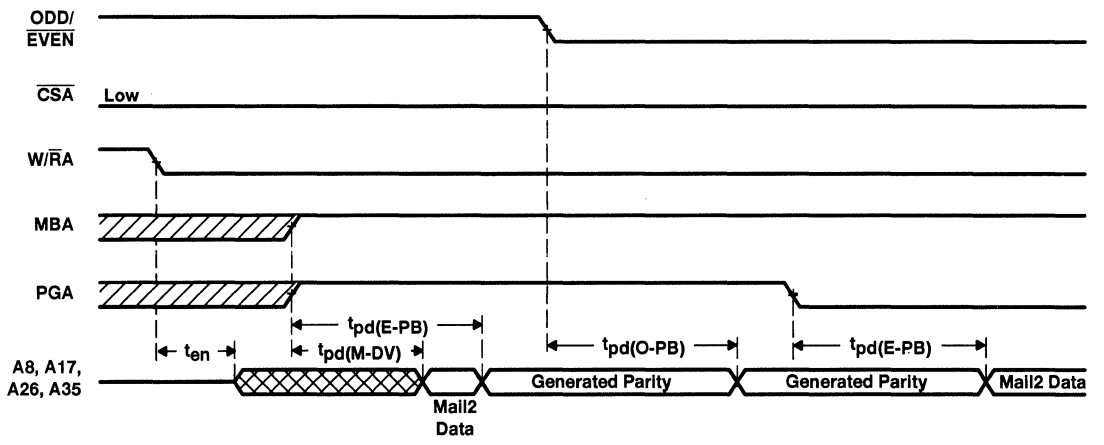
NOTE A: ENA is high and $\overline{CSA}$ is low.

Figure 23. ODD/$\overline{EVEN}$, W/$\overline{RA}$, MBA, and PGA to $\overline{PEFA}$ Timing



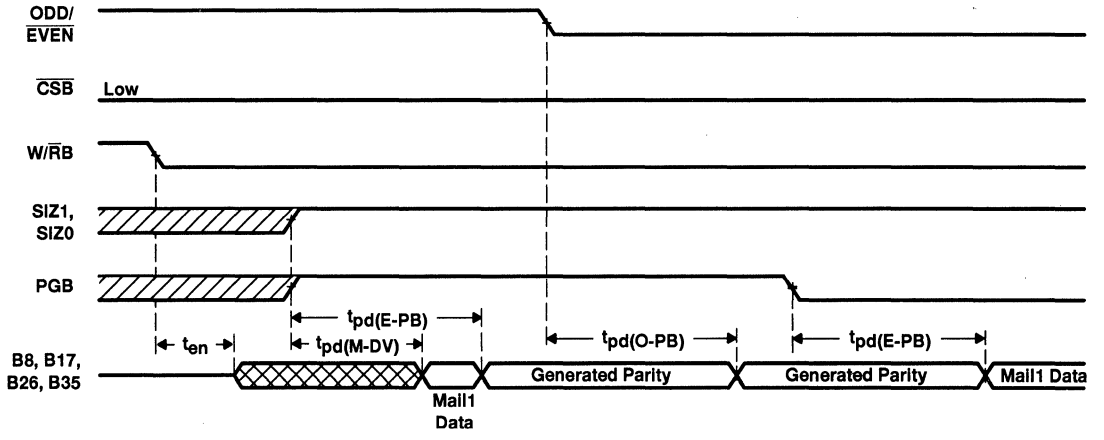
NOTE A: ENB is high and $\overline{CSB}$ is low.

Figure 24. ODD/$\overline{EVEN}$, W/$\overline{RB}$, SIZ1, SIZ0, and PGB to $\overline{PEFB}$ Timing



NOTE A: ENA is high.

Figure 25. Parity-Generation Timing When Reading From the Mail2 Register



NOTE A: ENB is high.

Figure 26. Parity-Generation Timing When Reading From the Mail1 Register

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±500 mA
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−4	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS				MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −4 mA			2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.5	V
I_I	V_{CC} = 5.5 V,	$V_I = V_{CC}$ or 0					±50	µA
I_{OZ}	V_{CC} = 5.5 V,	$V_O = V_{CC}$ or 0					±50	µA
I_{CC}	V_{CC} = 5.5 V,	I_O = 0 mA,	$V_I = V_{CC}$ or GND	Outputs high			30	mA
				Outputs low			130	
				Outputs disabled			30	
C_i	V_I = 0,	f = 1 MHz				4		pF
C_o	V_O = 0,	f = 1 MHz				8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 4 through 26)

		'ABT3614-15		'ABT3614-20		'ABT3614-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_c	Clock cycle time, CLKA or CLKB	15		20		30		ns
$t_{w(CLKH)}$	Pulse duration, CLKA and CLKB high	6		8		12		ns
$t_{w(CLKL)}$	Pulse duration, CLKA and CLKB low	6		8		12		ns
$t_{su(D)}$	Setup time, A0–A35 before CLKA↑ and B0–B35 before CLKB↑	4		5		6		ns
$t_{su(EN)}$	Setup time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA before CLKA↑; $\overline{CSB}$, W/$\overline{RB}$, and ENB before CLKB↑	5		5		6		ns
$t_{su(SZ)}$	Setup time, SIZ0, SIZ1, and $\overline{BE}$ before CLKB↑	4		5		6		ns
$t_{su(SW)}$	Setup time, SW0 and SW1 before CLKB↑	5		7		8		ns
$t_{su(PG)}$	Setup time, ODD/$\overline{EVEN}$ and PGA before CLKA↑; ODD/$\overline{EVEN}$ and PGB before CLKB↑†	4		5		6		ns
$t_{su(RS)}$	Setup time, $\overline{RST}$ low before CLKA↑ or CLKB↑‡	5		6		7		ns
$t_{su(FS)}$	Setup time, FS0 and FS1 before $\overline{RST}$ high	5		6		7		ns
$t_{h(D)}$	Hold time, A0–A35 after CLKA↑ and B0–B35 after CLKB↑	1		1		1		ns
$t_{h(EN)}$	Hold time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA after CLKA↑; $\overline{CSB}$, W/$\overline{RB}$, and ENB after CLKB↑	1		1		1		ns
$t_{h(SZ)}$	Hold time, SIZ0, SIZ1, and $\overline{BE}$ after CLKB↑	2		2		2		ns
$t_{h(SW)}$	Hold time, SW0 and SW1 after CLKB↑	0		0		0		ns
$t_{h(PG)}$	Hold time, ODD/$\overline{EVEN}$ and PGA after CLKA↑; ODD/$\overline{EVEN}$ and PGB after CLKB↑†	0		0		0		ns
$t_{h(RS)}$	Hold time, $\overline{RST}$ low after CLKA↑ or CLKB↑‡	5		6		7		ns
$t_{h(FS)}$	Hold time, FS0 and FS1 after $\overline{RST}$ high	4		4		4		ns
t_{sk1}§	Skew time between CLKA↑ and CLKB↑ for $\overline{EFA}$, $\overline{EFB}$, $\overline{FFA}$, and $\overline{FFB}$	8		8		10		ns
t_{sk2}§	Skew time between CLKA↑ and CLKB↑ for $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$, and $\overline{AFB}$	9		16		20		ns

† Only applies for a clock edge that does a FIFO read
‡ Requirement to count the clock edge as one of at least four needed to reset a FIFO
§ Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Figures 4 through 26)

PARAMETER		'ABT3614-15		'ABT3614-20		'ABT3614-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_a	Access time, CLKA↑ to A0–A35 and CLKB↑ to B0–B35	2	10	2	12	2	15	ns
$t_{pd(C-FF)}$	Propagation delay time, CLKA↑ to $\overline{FFA}$ and CLKB↑ to $\overline{FFB}$	2	10	2	12	2	15	ns
$t_{pd(C-EF)}$	Propagation delay time, CLKA↑ to $\overline{EFA}$ and CLKB↑ to $\overline{EFB}$	2	10	2	12	2	15	ns
$t_{pd(C-AE)}$	Propagation delay time, CLKA↑ to $\overline{AEA}$ and CLKB↑ to $\overline{AEB}$	2	10	2	12	2	15	ns
$t_{pd(C-AF)}$	Propagation delay time, CLKA↑ to $\overline{AFA}$ and CLKB↑ to $\overline{AFB}$	2	10	2	12	2	15	ns
$t_{pd(C-MF)}$	Propagation delay time, CLKA↑ to $\overline{MBF1}$ low or $\overline{MBF2}$ high and CLKB↑ to $\overline{MBF2}$ low or $\overline{MBF1}$ high	1	9	1	12	1	15	ns
$t_{pd(C-MR)}$	Propagation delay time, CLKA↑ to B0–B35† and CLKB↑ to A0–A35‡	3	11	3	13	3	15	ns
$t_{pd(C-PE)}$§	Propagation delay time, CLKB↑ to $\overline{PEFB}$	2	11	2	12	2	13	ns
$t_{pd(M-DV)}$	Propagation delay time, MBA to A0–A35 valid and SIZ1, SIZ0 to B0–B35 valid	1	11	1	11.5	1	12	ns
$t_{pd(D-PE)}$	Propagation delay time, A0-A35 valid to $\overline{PEFA}$ valid; B0-B35 valid to $\overline{PEFB}$ valid	3	10	3	11	3	13	ns
$t_{pd(O-PE)}$	Propagation delay time, ODD/$\overline{EVEN}$ to $\overline{PEFA}$ and $\overline{PEFB}$	3	11	3	12	3	14	ns
$t_{pd(O-PB)}$¶	Propagation delay time, ODD/$\overline{EVEN}$ to parity bits (A8, A17, A26, A35) and (B8, B17, B26, B35)	2	11	2	12	2	14	ns
$t_{pd(E-PE)}$	Propagation delay time, $\overline{CSA}$, ENA, W/$\overline{RA}$, MBA, or PGA to $\overline{PEFA}$; $\overline{CSB}$, ENB, W/$\overline{RB}$, SIZ1, SIZ0, or PGB to $\overline{PEFB}$	1	11	1	12	1	14	ns
$t_{pd(E-PB)}$¶	Propagation delay time, $\overline{CSA}$, ENA, W/$\overline{RA}$, MBA, or PGA to parity bits (A8, A17, A26, A35); $\overline{CSB}$, ENB, W/$\overline{RB}$, SIZ1, SIZ0, or PGB to parity bits (B8, B17, B26, B35)	3	12	3	13	3	14	ns
$t_{pd(R-F)}$	Propagation delay time, $\overline{RST}$ to ($\overline{MBF1}$, $\overline{MBF2}$) high.	1	15	1	20	1	30	ns
t_{en}	Enable time, $\overline{CSA}$ and W/$\overline{RA}$ low to A0–A35 active and $\overline{CSB}$ low and W/$\overline{RB}$ high to B0–B35 active	2	10	2	12	2	14	ns
t_{dis}	Disable time, $\overline{CSA}$ or W/$\overline{RA}$ high to A0–A35 at high impedance and $\overline{CSB}$ high or W/$\overline{RB}$ low to B0–B35 at high impedance	1	8	1	9	1	11	ns

† Writing data to the mail1 register when the B0–B35 outputs are active and SIZ1, SIZ0 are high.
‡ Writing data to the mail2 register when the A0–A35 outputs are active and MBA is high.
§ Only applies when a new port-B bus size is implemented by the rising CLKB edge.
¶ Only applies when reading data from a mail register

TYPICAL CHARACTERISTICS

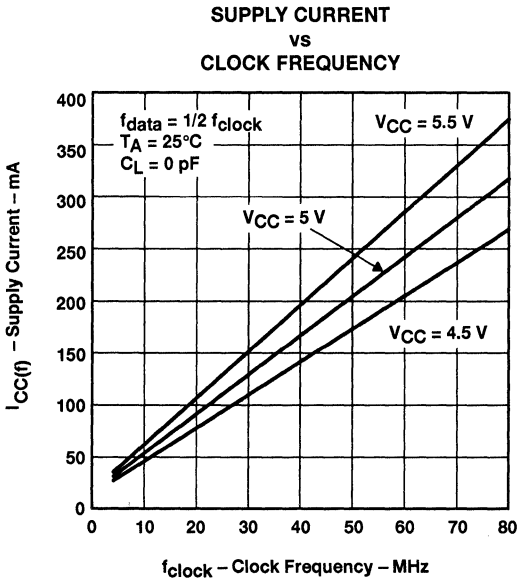


Figure 27

calculating power dissipation

The $I_{CC(f)}$ current for the graph in Figure 28 was taken while simultaneously reading and writing the FIFO on the SN74ACT3614 with CLKA and CLKB set to f_{clock}.All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitive load per data-output channel is known, the power dissipation can be calculated with the equation below.

With $I_{CC(f)}$ taken from Figure 28, the maximum power dissipation (P_T) of the SN74ABT3614 can be calculated by:

$$P_T = V_{CC} \times I_{CC(f)} + \Sigma(C_L \times V_{OH}^2 \times f_o)$$

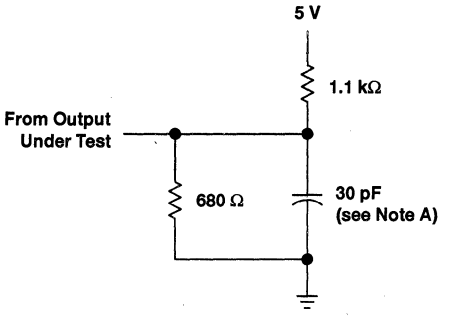
where:

C_L = output capacitive load
f_o = switching frequency of an output
V_{OH} = high-level output voltage

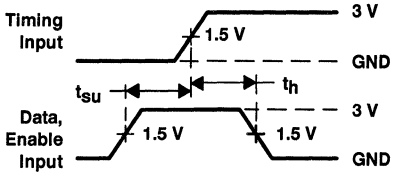
When no reads or writes are occurring on the SN74ABT3614, the power dissipated by a single clock (CLKA or CLKB) input running at frequency f_{clock} is calculated by:

$$P_T = V_{CC} \times f_{clock} \times 0.29 \text{ mA/MHz}$$

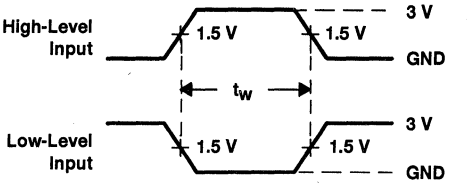
PARAMETER MEASUREMENT INFORMATION



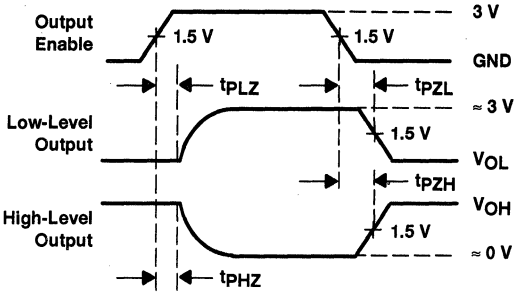
LOAD CIRCUIT



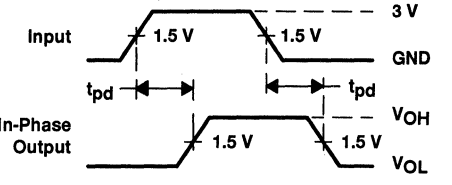
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

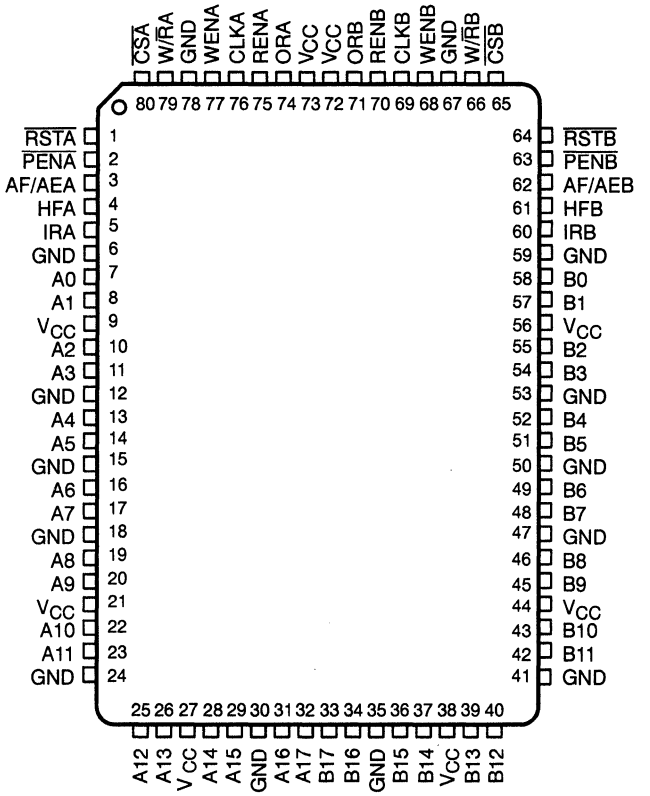
NOTE A: Includes probe and jig capacitance

Figure 28. Load Circuit and Voltage Waveforms

SCBS125B – JULY 1992 – REVISED AUGUST 1994

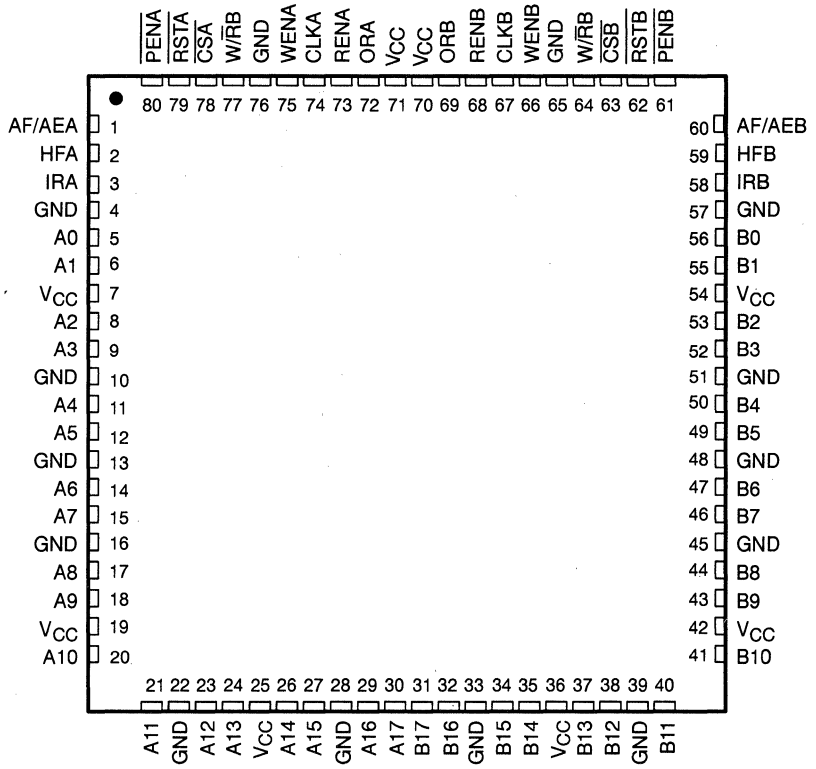
- Member of the Texas Instruments Widebus™ Family
- Free-Running CLKA and CLKB Can Be Asynchronous or Coincident
- Read and Write Operations Synchronized to Independent System Clocks
- Two Separate 512 × 18 Clocked FIFOs Buffering Data in Opposite Directions
- IRA and ORA Synchronized to CLKA
- IRB and ORB Synchronized to CLKB
- Microprocessor Interface Control Logic
- Programmable Almost-Full/Almost-Empty Flags
- Fast Access Times of 9 ns With a 50-pF Load and Simultaneous Switching Data Outputs
- Data Rates up to 80 MHz
- Advanced BiCMOS Technology
- Available in 80-Pin Quad Flat Package (PH) and Space-Saving 80-Pin Thin Quad Flat Package (PN)

PH PACKAGE
(TOP VIEW)



Widebus is a trademark of Texas Instruments Incorporated.

PN PACKAGE
(TOP VIEW)



description

A FIFO memory is a storage device that allows data to be read from its array in the same order it is written. The SN74ABT7819 is a high-speed, low-power BiCMOS bidirectional clocked FIFO memory. Two independent 512 × 18 dual-port SRAM FIFOs on board the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions, a half-full flag, and a programmable almost-full/almost-empty flag.

The SN74ABT7819 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The state of the A0–A17 outputs is controlled by $\overline{CSA}$ and W/$\overline{RA}$. When both $\overline{CSA}$ and W/$\overline{RA}$ are low, the outputs are active. The A0–A17 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is high. Data is written to FIFOA–B from port A on the low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is high, WENA is high, and the IRA flag is high. Data is read from FIFOB–A to the A0–A17 outputs on the low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is low, RENA is high, and the ORA flag is high.

description (continued)

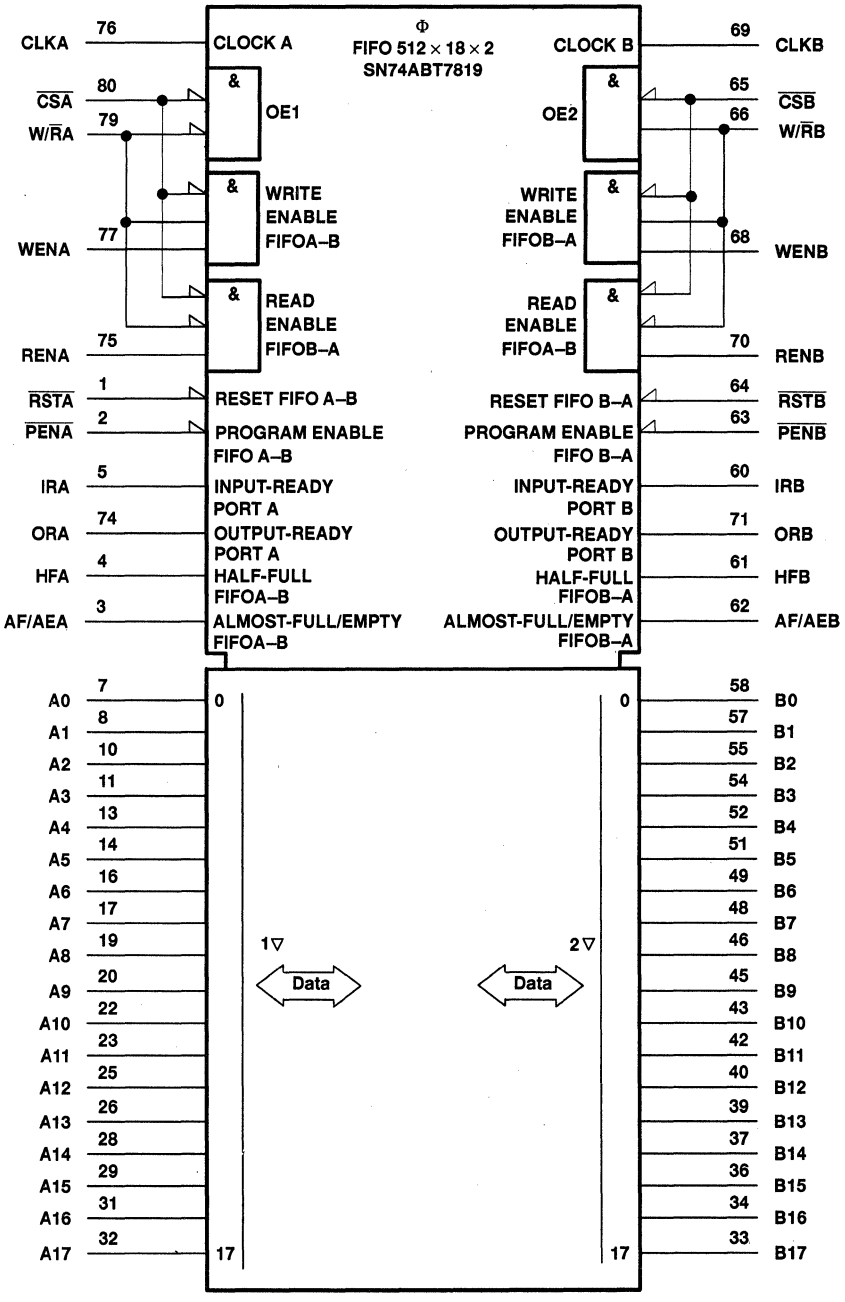
The state of the B0–B17 outputs is controlled by $\overline{CSB}$ and W/$\overline{RB}$. When both $\overline{CSB}$ and W/$\overline{RB}$ are low, the outputs are active. The B0–B17 outputs are in the high-impedance state when either $\overline{CSB}$ or W/$\overline{RB}$ is high. Data is written to FIFOB–A from port B on the low-to-high transition of CLKB when $\overline{CSB}$ is low, W/$\overline{RB}$ is high, WENB is high, and the $\overline{IRB}$ flag is high. Data is read from FIFOA–B to the B0–B17 outputs on the low-to-high transition of CLKB when $\overline{CSB}$ is low, W/$\overline{RB}$ is low, RENB is high, and the ORB flag is high.

The setup and hold-time constraints for the chip selects ($\overline{CSA}$, $\overline{CSB}$) and write/read selects (W/$\overline{RA}$, W/$\overline{RB}$) are for enabling write and read operations on memory and are not related to the high-impedance control of the data outputs. If a port's read enable (RENA or RENB) and write enable (WENA or WENB) are set low during a clock cycle, the chip select and write/read select can switch at any time during the cycle to change the state of the data outputs.

The input-ready and output-ready flags of a FIFO are two-stage synchronized to the port clocks for use as reliable control signals. CLKA synchronizes the status of the input-ready flag of FIFOA–B (IRA) and the output-ready flag of FIFOB–A (ORA). CLKB synchronizes the status of the input-ready flag of FIFOB–A (IRB) and the output-ready flag of FIFOA–B (ORB). When the input-ready flag of a port is low, the FIFO receiving input from the port is full and writes are disabled to its array. When the output-ready flag of a port is low, the FIFO that outputs data to the port is empty and reads from its memory are disabled. The first word loaded to an empty memory is sent to the FIFO output register at the same time its output-ready flag is asserted (high). When the memory is read empty and the output-ready flag is forced low, the last valid data remains on the FIFO outputs until the output-ready flag is asserted (high) again. In this way, a high on the output-ready flag indicates new data is present on the FIFO outputs.

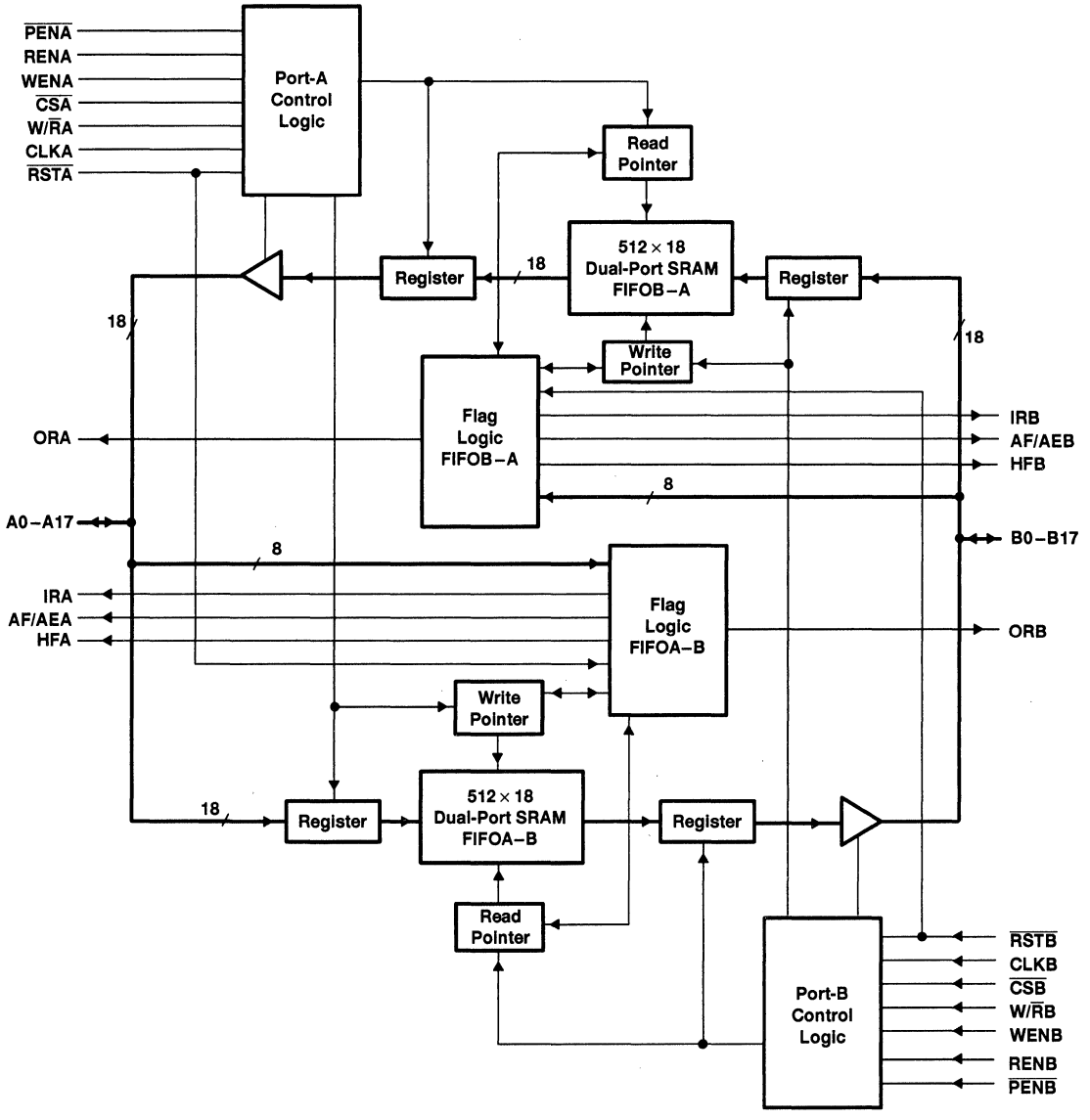
The SN74ABT7819 is characterized for operation from 0°C to 70°C.

logic symbol†

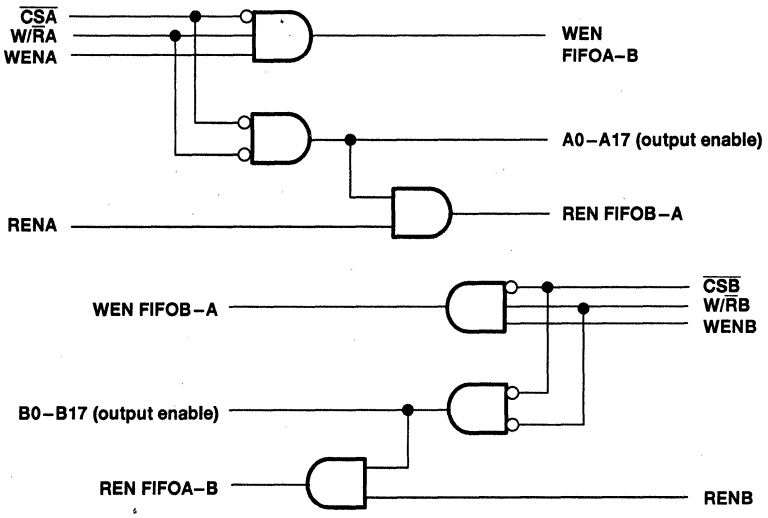


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the PH package.

functional block diagram



enable logic diagram (positive logic)



FUNCTION TABLES

SELECT INPUTS					A0–A17	PORT-A OPERATION
CLKA	$\overline{CSA}$	W/$\overline{RA}$	WENA	RENA		
X	H	X	X	X	High Z	None
↑	L	H	H	X	High Z	Write A0–A17 to FIFOA–B
↑	L	L	X	H	Active	Read FIFOB–A to A0–A17

SELECT INPUTS					B0–B17	PORT-B OPERATION
CLKB	$\overline{CSB}$	W/$\overline{RB}$	WENB	RENB		
X	H	X	X	X	High Z	None
↑	L	H	H	X	High Z	Write B0 –B17 to FIFOB–A
↑	L	L	X	H	Active	Read FIFOA–B to B0–B17

Terminal Functions

PIN NAME	I/O	DESCRIPTION
A0–A17	I/O	Port-A data. The 18-bit bidirectional data port for side A.
AF/AEA	O	FIFOA–B almost-full/almost-empty flag. Depth offsets can be programmed for AF/AEA or the default value of 128 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AEA is high when X or less words or (512 – Y) or more words are stored in FIFOA–B. AF/AEA is forced high when FIFOA–B is reset.
AF/AEB	O	FIFOB–A almost-full/almost-empty flag. Depth offsets can be programmed for AF/AEB or the default value of 128 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AEB is high when X or less words or (512 – Y) or more words are stored in FIFOB –A. AF/AEB is forced high when FIFOB –A is reset.
B0–B17	I/O	Port-B data. The 18-bit bidirectional data port for side B.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A to its low-to-high transition and can be asynchronous or coincident to CLKB.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B to its low-to-high transition and can be asynchronous or coincident to CLKA.
$\overline{CSA}$	I	Port-A chip select. $\overline{CSA}$ must be low to enable a low-to-high transition of CLKA to either write data from A0–A17 to FIFOA–B or read data from FIFOB–A to A0–A17. The A0–A17 outputs are in the high-impedance state when $\overline{CSA}$ is high.
$\overline{CSB}$	I	Port-B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to either write data from B0–B17 to FIFOB–A or read data from FIFOA–B to B0–B17. The B0–B17 outputs are in the high-impedance state when $\overline{CSB}$ is high.
HFA	O	FIFOA–B half-full flag. HFA is high when FIFOA–B contains 256 or more words and is low when FIFOA–B contains 255 or less words. HFA is set low after FIFOA–B is reset.
HFB	O	FIFOB –A half-full flag. HFB is high when FIFOB–A contains 256 or more words and is low when FIFOB–A contains 255 or less words. HFB is set low after FIFOB –A is reset.
IRA	O	Port-A input-ready flag. IRA is synchronized to the low-to-high transition of CLKA. When IRA is low, FIFOA–B is full and writes to its array are disabled. IRA is set low during a FIFOA–B reset and is set high on the second low-to-high transition of CLKA after reset.
IRB	O	Port-B input-ready flag. IRB is synchronized to the low-to-high transition of CLKB. When IRB is low, FIFOB–A is full and writes to its array are disabled. IRB is set low during a FIFOB –A reset and is set high on the second low-to-high transition of CLKB after reset.
ORA	O	Port-A output-ready flag. ORA is synchronized to the low-to-high transition of CLKA. When ORA is low, FIFOB–A is empty and reads from its array are disabled. The last valid word remains on the FIFOB–A outputs when ORA is low. Ready data is present for the A0–A17 outputs when ORA is high. ORA is set low during a FIFOB–A reset and goes high on the third low-to-high transition of CLKA after the first word is loaded to an empty FIFOB –A.
ORB	O	Port-B output-ready flag. ORB is synchronized to the low-to-high transition of CLKB. When ORB is low, FIFOA–B is empty and reads from its array are disabled. The last valid word remains on the FIFOA–B outputs when ORB is low. Ready data is present for the B0–B17 outputs when ORB is high. ORB is set low during a FIFOA–B reset and goes high on the third low-to-high transition of CLKB after the first word is loaded to an empty FIFOA–B.
$\overline{PENA}$	I	AF/AEA program enable. After FIFOA–B is reset and before a word is written to its array, the binary value on A0–A7 is latched as an AF/AEA offset when $\overline{PENA}$ is low and CLKA is high.
$\overline{PENB}$	I	AF/AEB program enable. After FIFOB –A is reset and before a word is written to its array, the binary value on B0–B7 is latched as an AF/AEB offset when $\overline{PENB}$ is low and CLKB is high.
RENA	I	Port-A read enable. A high level on RENA enables data to be read from FIFOB–A on the low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is low, and ORA is high.
RENB	I	Port-B read enable. A high level on RENB enables data to be read from FIFOA–B on the low-to-high transition of CLKB when $\overline{CSB}$ is low, W/$\overline{RB}$ is low, and ORB is high.
$\overline{RSTA}$	I	FIFOA–B reset. To reset FIFOA–B, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RSTA}$ is low. This sets HFA low, IRA low, ORB low, and AF/AEA high.
$\overline{RSTB}$	I	FIFOB –A reset. To reset FIFOB –A, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RSTB}$ is low. This sets HFB low, IRB low, ORA low, and AF/AEB high.
WENA	I	Port-A write enable. A high level on WENA enables data on A0–A17 to be written into FIFOA–B on the low-to-high transition of CLKA when W/$\overline{RA}$ is high, $\overline{CSA}$ is low, and IRA is high.

Terminal Functions (Continued)

PIN NAME	I/O	DESCRIPTION
WENB	I	Port-B write enable. A high level on WENB enables data on B0–B17 to be written into FIFOB–A on the low-to-high transition of CLKB when W/$\overline{R}$B is high, $\overline{CSB}$ is low, and IRB is high.
W/$\overline{R}$A	I	Port-A write/$\overline{read}$ select. A high on W/$\overline{R}$A enables A0–A17 data to be written to FIFOA–B on a low-to-high transition of CLKA when WENA is high, $\overline{CSA}$ is low, and IRA is high. A low on W/$\overline{R}$A enables data to be read from FIFOB–A on a low-to-high transition of CLKA when RENA is high, $\overline{CSA}$ is low, and ORA is high. The A0–A17 outputs are in the high-impedance state when W/$\overline{R}$A is high.
W/$\overline{R}$B	I	Port-B write/read select. A high on W/$\overline{R}$B enables B0–B17 data to be written to FIFOB–A on a low-to-high transition of CLKB when WENB is high, $\overline{CSB}$ is low, and IRB is high. A low on W/$\overline{R}$B enables data to be read from FIFOA–B on a low-to-high transition of CLKB when RENB is high, $\overline{CSB}$ is low, and ORB is high. The B0–B17 outputs are in the high-impedance state when W/$\overline{R}$B is high.

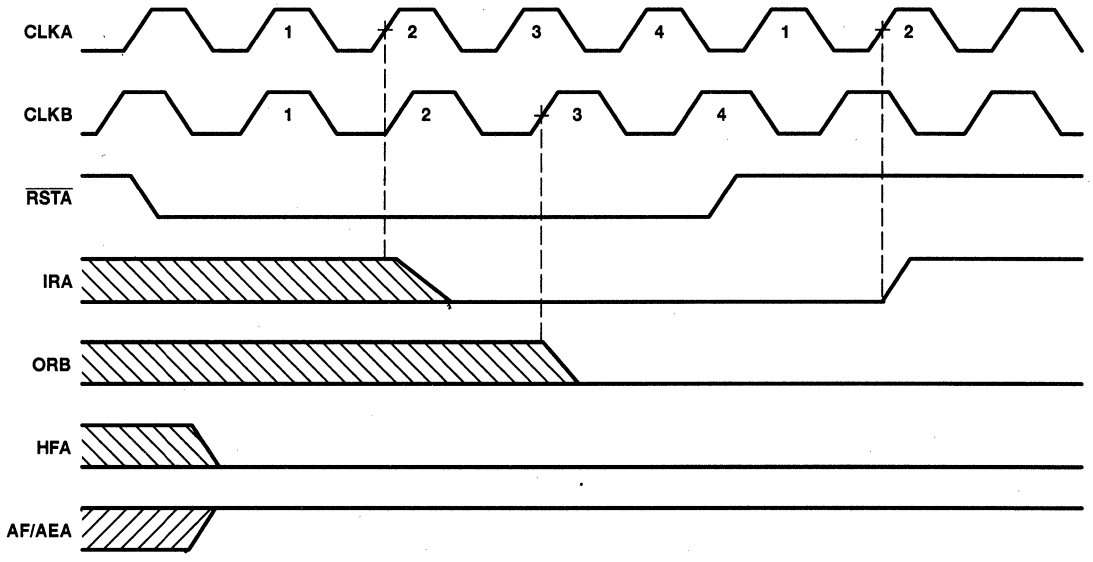
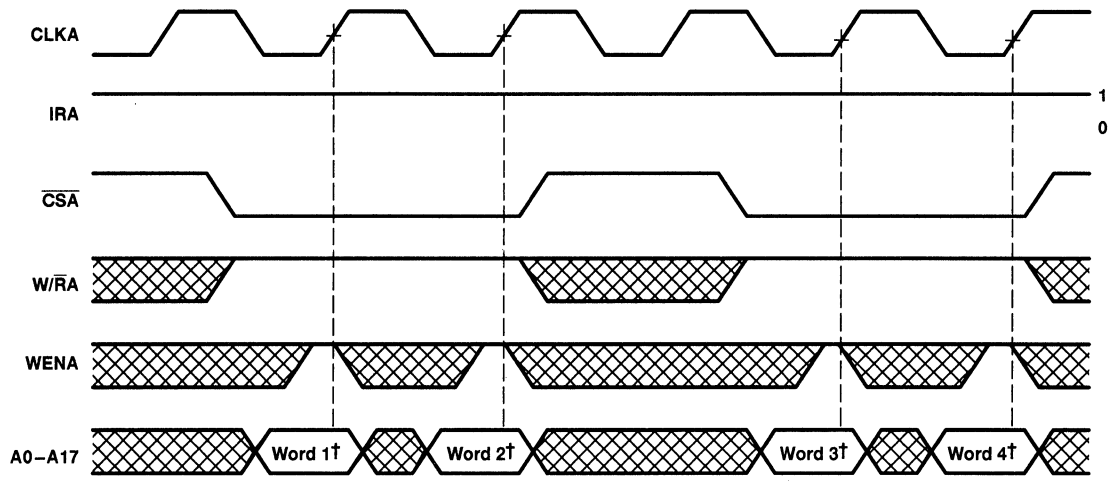


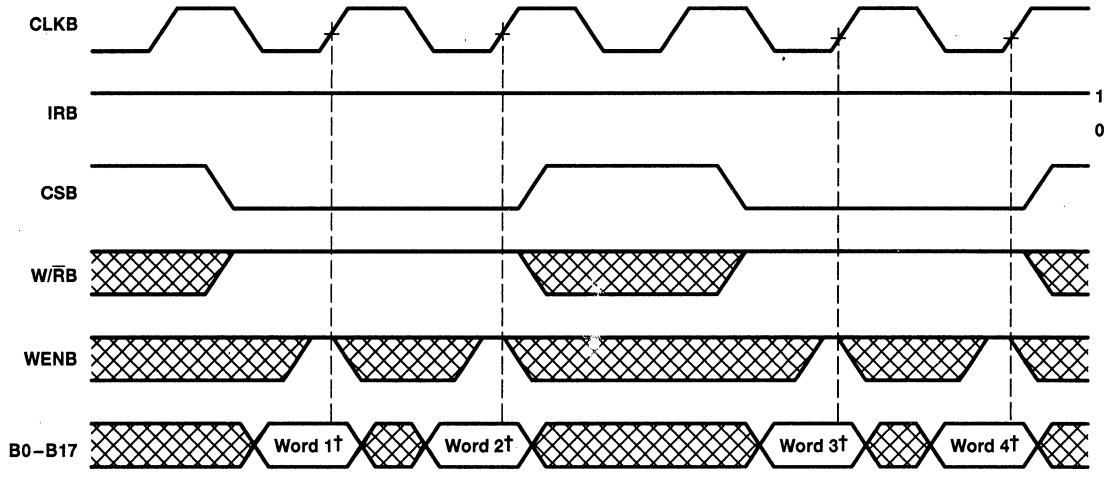
Figure 1. Reset Cycle for FIFOA–B†

† FIFOB–A is reset in the same manner.



† Written to FIFOA–B

Figure 2. Write Timing – Port A



† Written to FIFOB–A

Figure 3. Write Timing – Port B

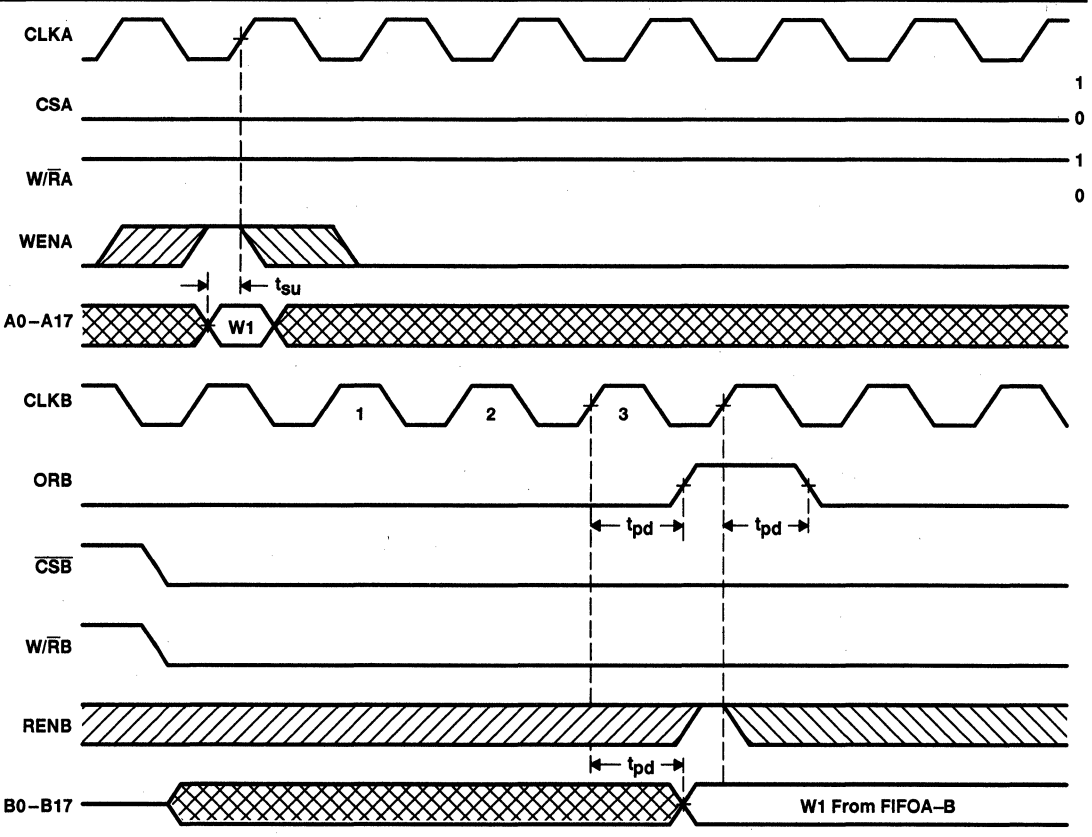


Figure 4. ORB-Flag Timing and First Data Word Fallthrough When FIFOA–B Is Empty†

† Operation of FIFOB–A is identical to that of FIFOA–B.

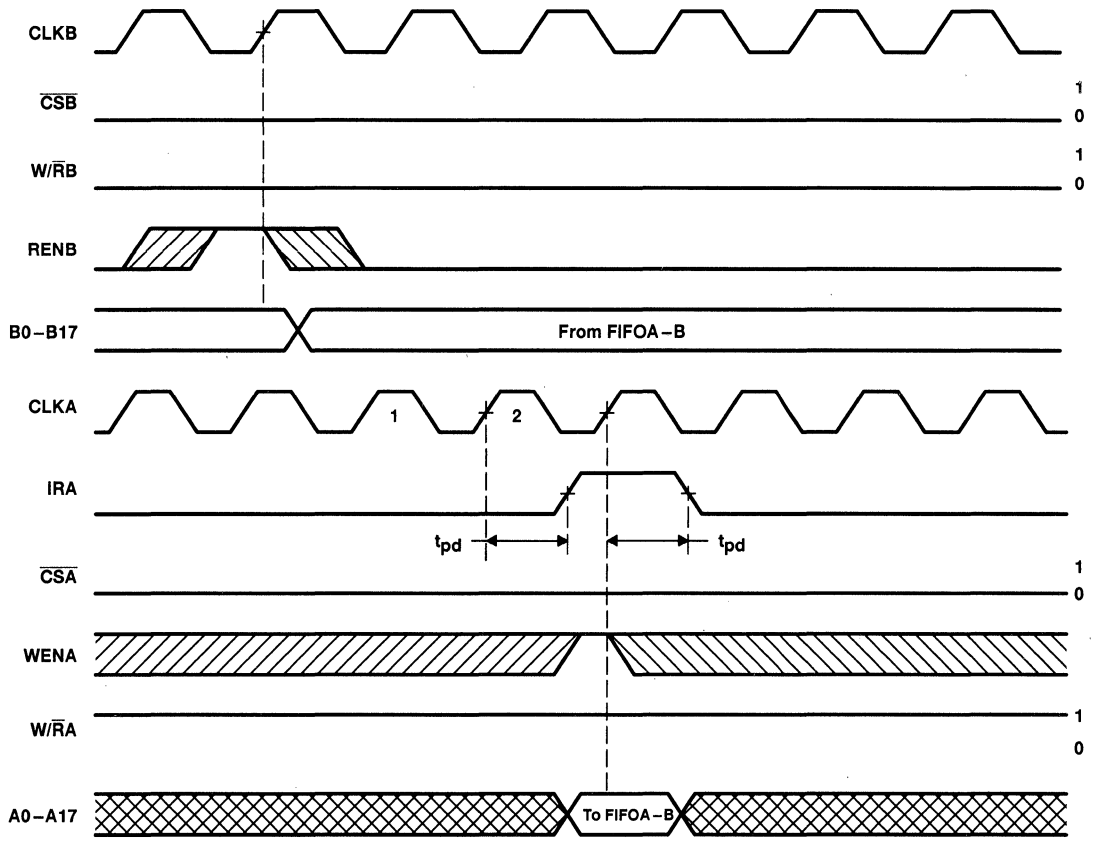
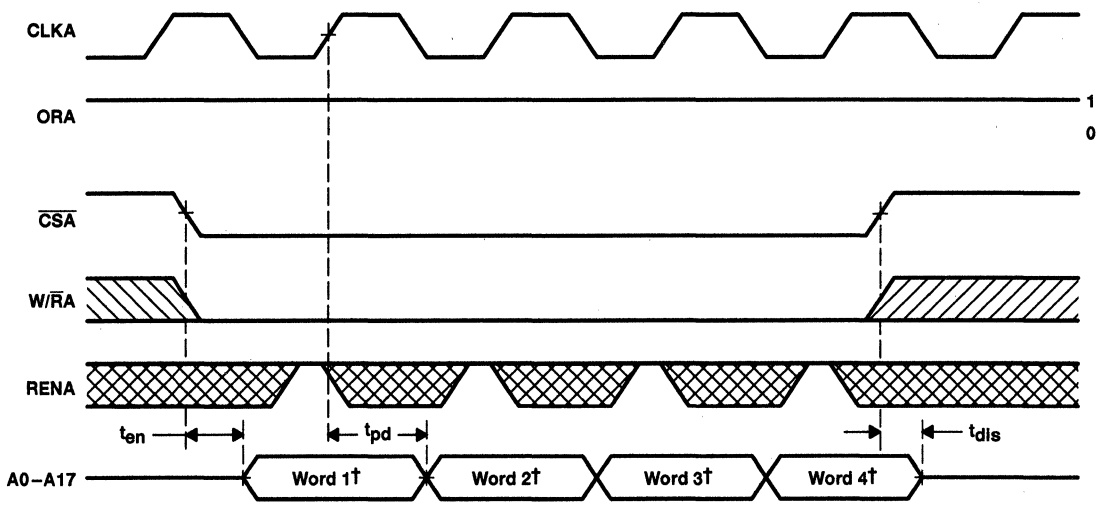


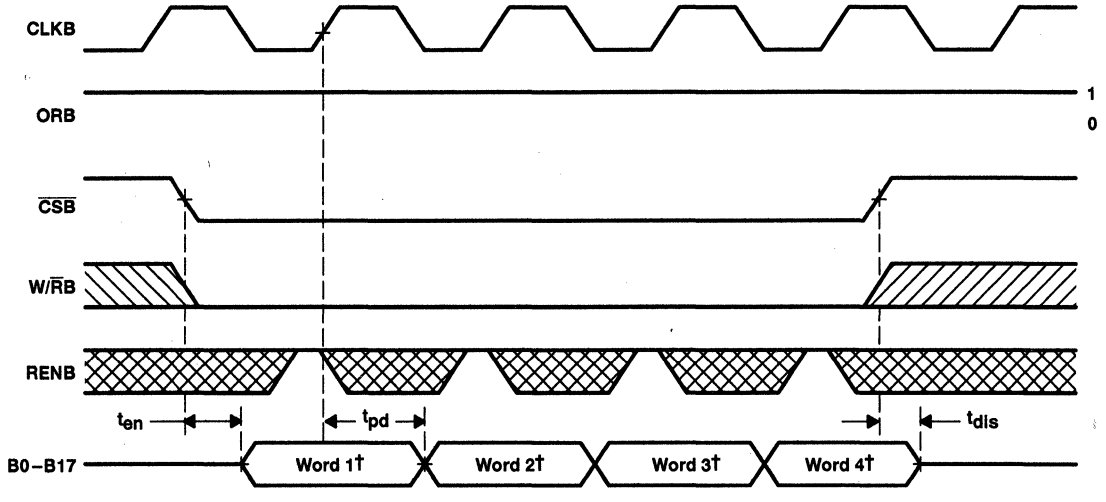
Figure 5. Write-Cycle and IRA-Flag Timing When FIFOA–B Is Full†

† Operation of FIFOB–A is identical to that of FIFOA–B.



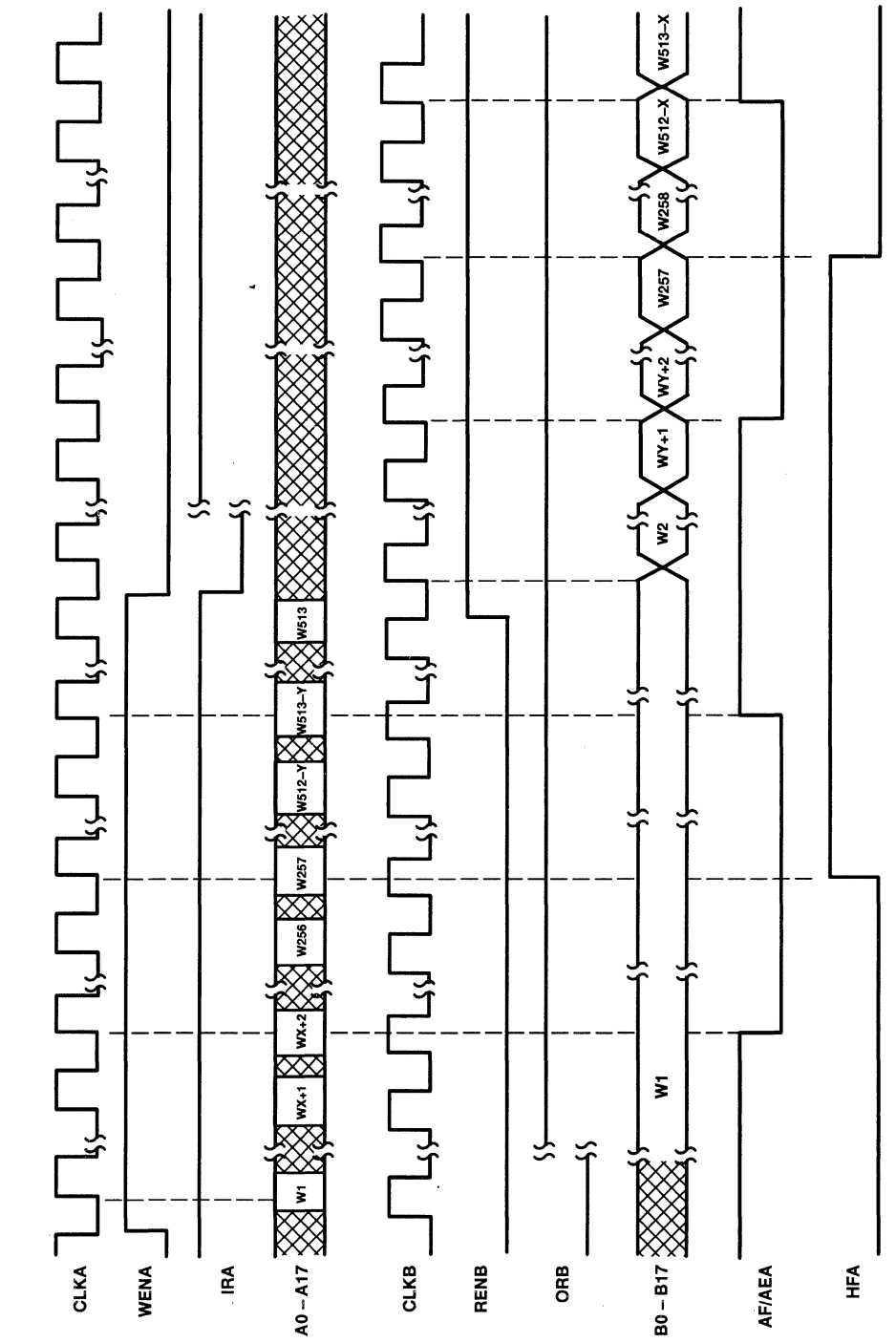
† Read from FIFOB–A

Figure 6. Read Timing – Port A



† Read from FIFOA–B

Figure 7. Read Timing – Port B



NOTES: $\overline{CSA}$, $\overline{CSB}$ = 0, W/$\overline{RA}$ = 1, W/$\overline{RB}$ = 0
X is the almost-empty offset and Y is the almost-full offset for AF/AEA.
HFB and AF/AEB function in the same manner for FIFO B–A.

Figure 8. FIFOA – B (HFA, AF/AEA) Asynchronous Flag Timing

offset values for AF/AE

The almost-full/almost-empty flag of each FIFO has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed from the input of the FIFO after it is reset and before a word is written to its memory. An AF/AE flag is high when its FIFO contains X or less words or (512 – Y) or more words.

To program the offset values for AF/AEA, $\overline{\text{PENA}}$ is brought low after FIFOA–B is reset and only when CLKA is low. On the following low-to-high transition of CLKA, the binary value on A0–A7 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{\text{PENA}}$ low for another low-to-high transition of CLKA reprograms Y to the binary value on A0–A7 at the time of the second CLKA low-to-high transition.

During the first two CLKA cycles used for offset programming, $\overline{\text{PENA}}$ can be brought high only when CLKA is low. $\overline{\text{PENA}}$ can be brought high at any time after the second CLKA pulse used for offset programming returns low. A maximum value of 255 can be programmed for either X or Y (see Figure 9). To use the default values of X = Y = 128, $\overline{\text{PENA}}$ must be tied high. No data is stored in FIFOA–B while the AF/AEA offsets are programmed. The AF/AEB flag is programmed in the same manner with $\overline{\text{PENB}}$ enabling CLKB to program the offset values taken from B0–B7.

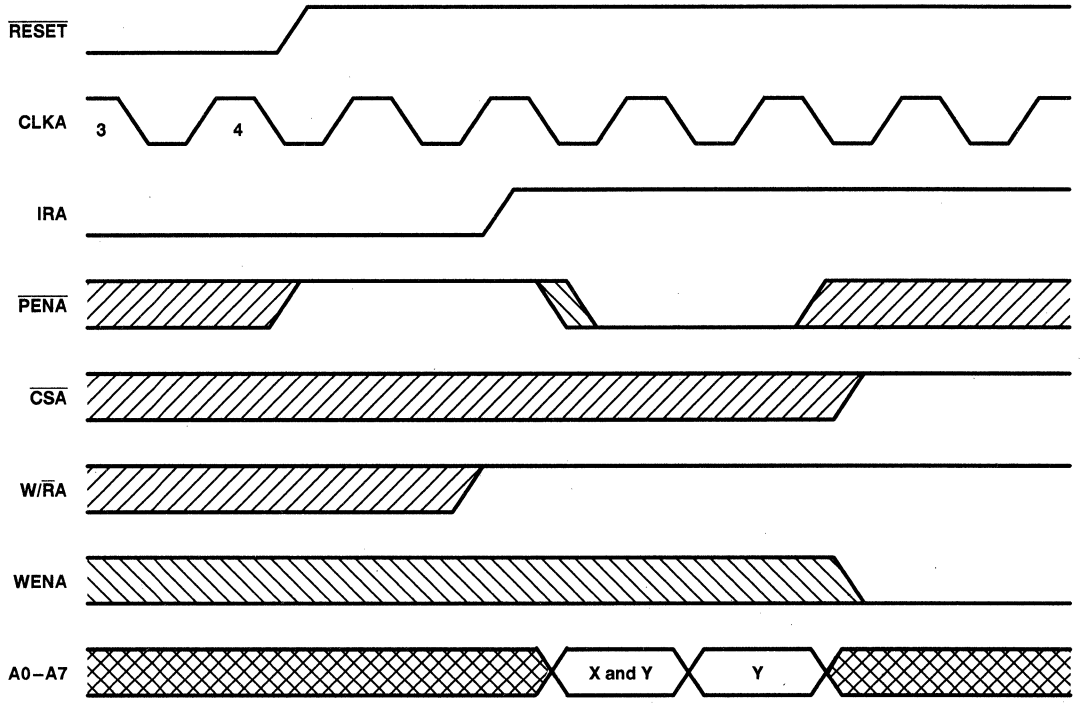


Figure 9. Programming X and Y Separately for AF/AEA

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 48 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
I_{OH}	High-level output current			−12	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate			5	ns/V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA					−1.2	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −3 mA			2.5			V
		V_{CC} = 5 V, I_{OH} = −3 mA			3			
		V_{CC} = 4.5 V, I_{OH} = −12 mA			2			
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 24 mA				0.5		V
I_I		V_{CC} = 5.5 V, V_I = V_{CC} or GND					±1	µA
I_{OZH}§		V_{CC} = 5.5 V, V_O = 2.7 V					50	µA
I_{OZL}§		V_{CC} = 5.5 V, V_O = 0.5 V					−50	µA
I_O¶		V_{CC} = 5.5 V, V_O = 2.5 V			−40	−100	−180	mA
I_{CC}		V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND		Outputs high			15	mA
				Outputs low			95	
				Outputs disabled			15	
C_i	Control inputs	V_I = 2.5 V or 0.5 V				6		pF
C_o	Flags	V_O = 2.5 V or 0.5 V				4		pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V				8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ The parameters I_{OZH} and I_{OZL} include the input leakage current.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 8)

			'ABT7819-12		'ABT7819-15		'ABT7819-20		'ABT7819-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			80		67		50		33.3	MHz
t_w	Pulse duration	CLKA, CLKB high or low	4.5		6		8		11		ns
t_{su}	Setup time	A0–A17 before CLKA↑ and B0–B17 before CLKB↑	3		4		5		5		ns
		$\overline{CSA}$ before CLKA↑ and $\overline{CSB}$ before CLKB↑	6		6		7		7		
		W/$\overline{RA}$ before CLKA↑ and W/$\overline{RB}$ before CLKB↑	6		6		7		7		
		WENA before CLKA↑ and WENB before CLKB↑	4		4		5		5		
		RENA before CLKA↑ and RENB before CLKB↑	5		5		5		6		
		$\overline{PENA}$ before CLKA↑ and $\overline{PENB}$ before CLKB↑	3		4		5		5		
		$\overline{RSTA}$ or $\overline{RSTB}$ low before first CLKA↑ and CLKB↑ †	3		4		5		5		
t_h	Hold time	A0–A17 after CLKA↑ and B0–B17 after CLKB↑	0		0		0		0		ns
		$\overline{CSA}$ after CLKA↑ and $\overline{CSB}$ after CLKB↑	0		0		0		0		
		W/$\overline{RA}$ after CLKA↑ and W/$\overline{RB}$ after CLKB↑	0		0		0		0		
		WENA after CLKA↑ and WENB after CLKB↑	0		0		0		0		
		RENA after CLKA↑ and RENB after CLKB↑	0		0		0		0		
		PENA after CLKA low and PENB after CLKB low	2		2		2		2		
		$\overline{RSTA}$ or $\overline{RSTB}$ low after fourth CLKA↑ and CLKB↑ †	3		3		4		4		

† To permit the clock pulse to be utilized for reset purposes

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 10 and 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ABT7819-12			'ABT7819-15		'ABT7819-20		'ABT7819-30		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKA or CLKB		80			67		50		33.3		MHz
t_{pd}	CLKA↑	A0–A17	4	7	9	4	10	4	12	4	14	ns
	CLKB↑	B0–B17	4	7	9	4	10	4	12	4	14	
t_{pd}‡	CLKA↑	A0–A17		6								ns
	CLKB↑	B0–B17		6								
t_{pd}	CLKA↑	IRA	4		9	4	10	4	12	4	14	ns
	CLKB↑	IRB	4		9	4	10	4	12	4	14	
t_{pd}	CLKA↑	ORA	3.5		9	3.5	10	3.5	12	3.5	14	ns
	CLKB↑	ORB	3.5		9	3.5	10	3.5	12	3.5	14	
t_{pd}	CLKA↑	AF/AEA	8		17	8	17	8	18	8	20	ns
	CLKB↑		8		17	8	17	8	18	8	20	
t_{PLH}	$\overline{RSTA}$	AF/AEA	4		12	4	14	4	15	4	16	ns
t_{pd}	CLKA↑	AF/AEB	8		17	8	17	8	18	8	20	ns
	CLKB↑		8		17	8	17	8	18	8	20	
t_{PLH}	$\overline{RSTB}$	AF/AEB	4		12	4	14	4	15	4	16	ns
	CLKA↑	HFA	8		17	8	17	8	18	8	20	
t_{PHL}	CLKB↑	HFA	8		17	8	17	8	18	8	20	ns
	$\overline{RSTA}$		4		12	4	14	4	15	4	16	
t_{PHL}	CLKA↑	HFB	8		17	8	17	8	18	8	20	ns
t_{PLH}	CLKB↑	HFB	8		17	8	17	8	18	8	20	ns
t_{PHL}	$\overline{RSTB}$		4		12	4	14	4	15	4	16	
t_{en}	$\overline{CSA}$	A0–A17	2.5		8	2.5	9	2.5	10	2.5	11	ns
	W/$\overline{RA}$		2.5		8	2.5	9	2.5	10	2.5	11	
t_{en}	$\overline{CSB}$	B0–B17	2.5		8	2.5	9	2.5	10	2.5	11	ns
	W/$\overline{RB}$		2.5		8	2.5	9	2.5	10	2.5	11	
t_{dis}	$\overline{CSA}$	A0–A17	2.5		8	2.5	9	2.5	10	2.5	11	ns
	W/$\overline{RA}$		2.5		8	2.5	9	2.5	10	2.5	11	
t_{dis}	$\overline{CSB}$	B0–B17	2.5		8	2.5	9	2.5	10	2.5	11	ns
	W/$\overline{RB}$		2.5		8	2.5	9	2.5	10	2.5	11	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This parameter is measured with a 30-pF load (see Figure 10).

TYPICAL CHARACTERISTICS

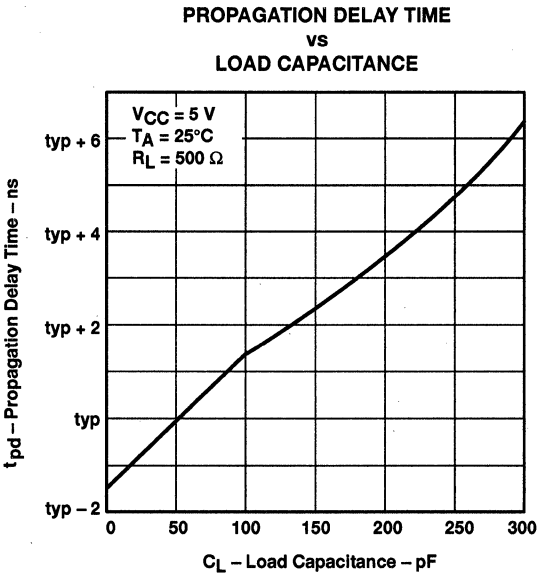


Figure 10

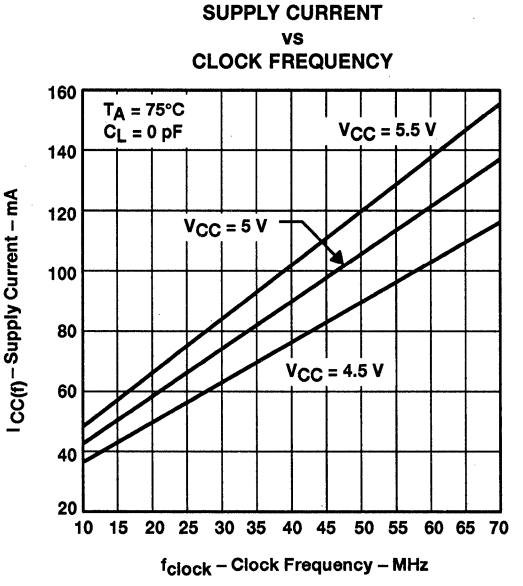


Figure 11

TYPICAL CHARACTERISTICS

calculating power dissipation

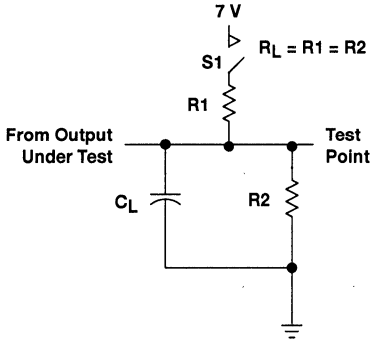
With $I_{CC(f)}$ taken from Figure 11, the maximum power dissipation (P_T) based on all outputs changing states on each read can be calculated using:

$$P_T = V_{CC} \times I_{CC(f)} + \Sigma(C_L \times V_{OH}^2 \times f_o)$$

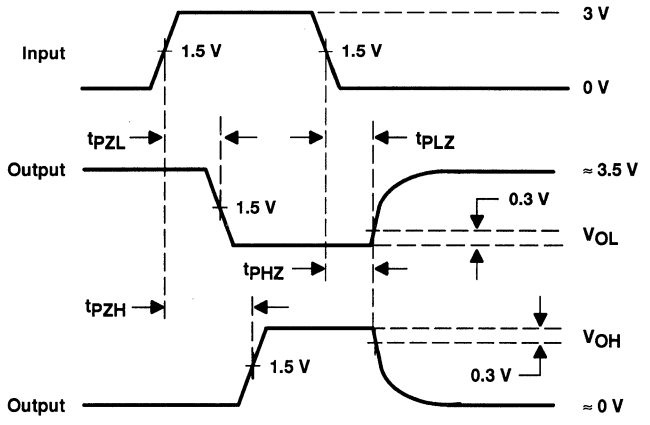
where:

$I_{CC(f)}$ = maximum I_{CC} per clock frequency
C_L = output capacitive load
f_o = data output frequency
V_{OH} = high-level output voltage

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

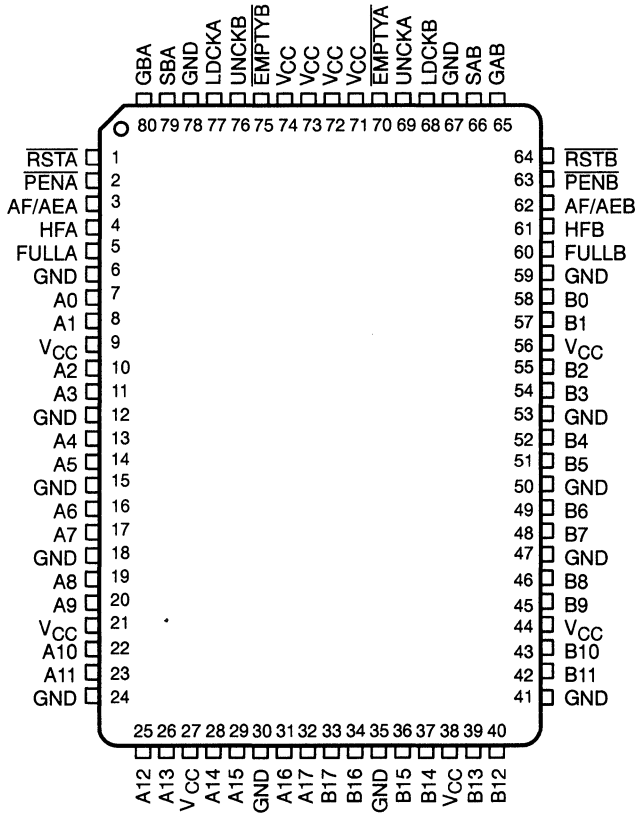
PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test-fixture capacitance

Figure 12. Load Circuit and Voltage Waveforms

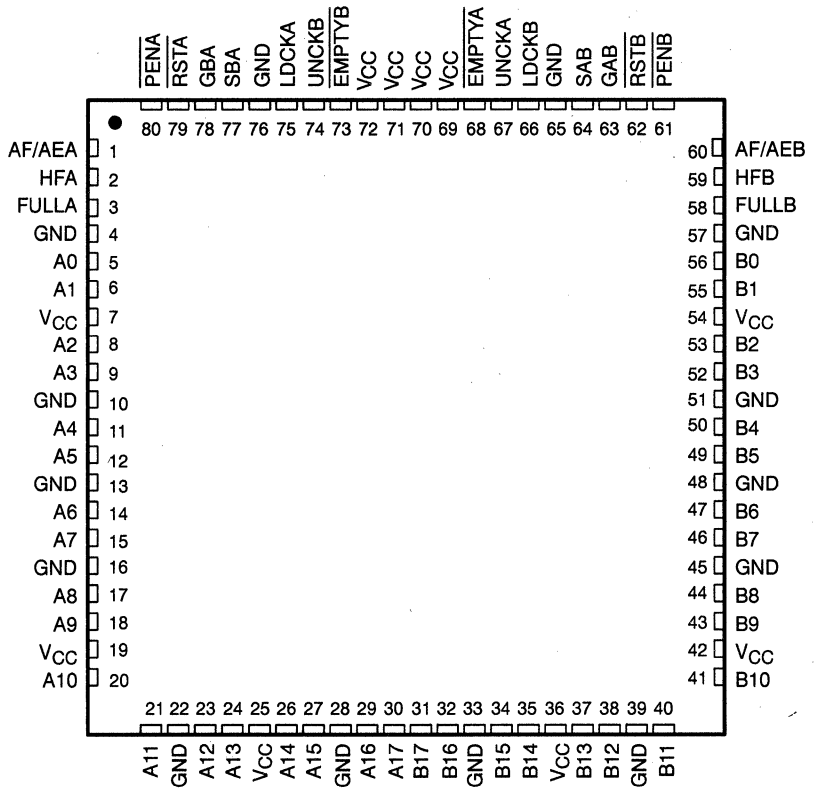
- Member of the Texas Instruments Widebus™ Family
- Independent Asynchronous Inputs and Outputs
- Produced in Advanced BiCMOS Technology
- Two Separate 512 × 18 FIFOs Buffering Data in Opposite Directions
- Programmable Almost-Full/Almost-Empty Flags
- Empty, Full, and Half-Full Flags
- Fast Access Times of 12 ns With a 50-pF Load and Simultaneous Switching Data Outputs
- Supports Clock Rates up to 67 MHz
- Available in 80-Pin Quad Flat Package (PH) and Space-Saving 80-Pin Thin Quad Flat Package (PN)

PH PACKAGE
(TOP VIEW)



Widebus is a trademark of Texas Instruments Incorporated.

PN PACKAGE
(TOP VIEW)



description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ABT7820 is arranged as two 512 by 18-bit FIFOs for high speed and fast access times. It processes data at rates from 0 to 67 MHz with access times of 12 ns in a bit-parallel format.

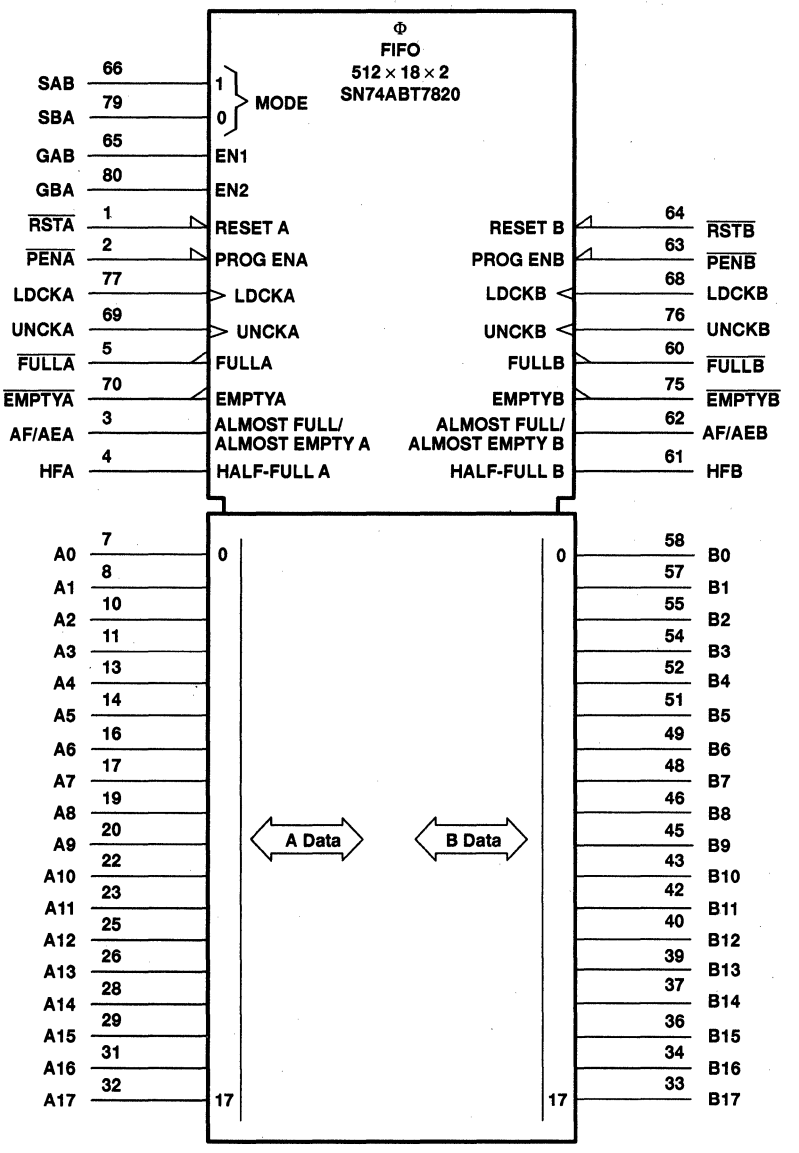
The SN74ABT7820 consists of bus transceiver circuits, two 512 × 18 FIFOs, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal FIFO memories. Enable inputs GAB and GBA control the transceiver functions. The SAB and SBA control inputs select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the eight fundamental bus-management functions that can be performed with the SN74ABT7820.

The SN74ABT7820 is characterized for operation from 0°C to 70°C.

Terminal Functions

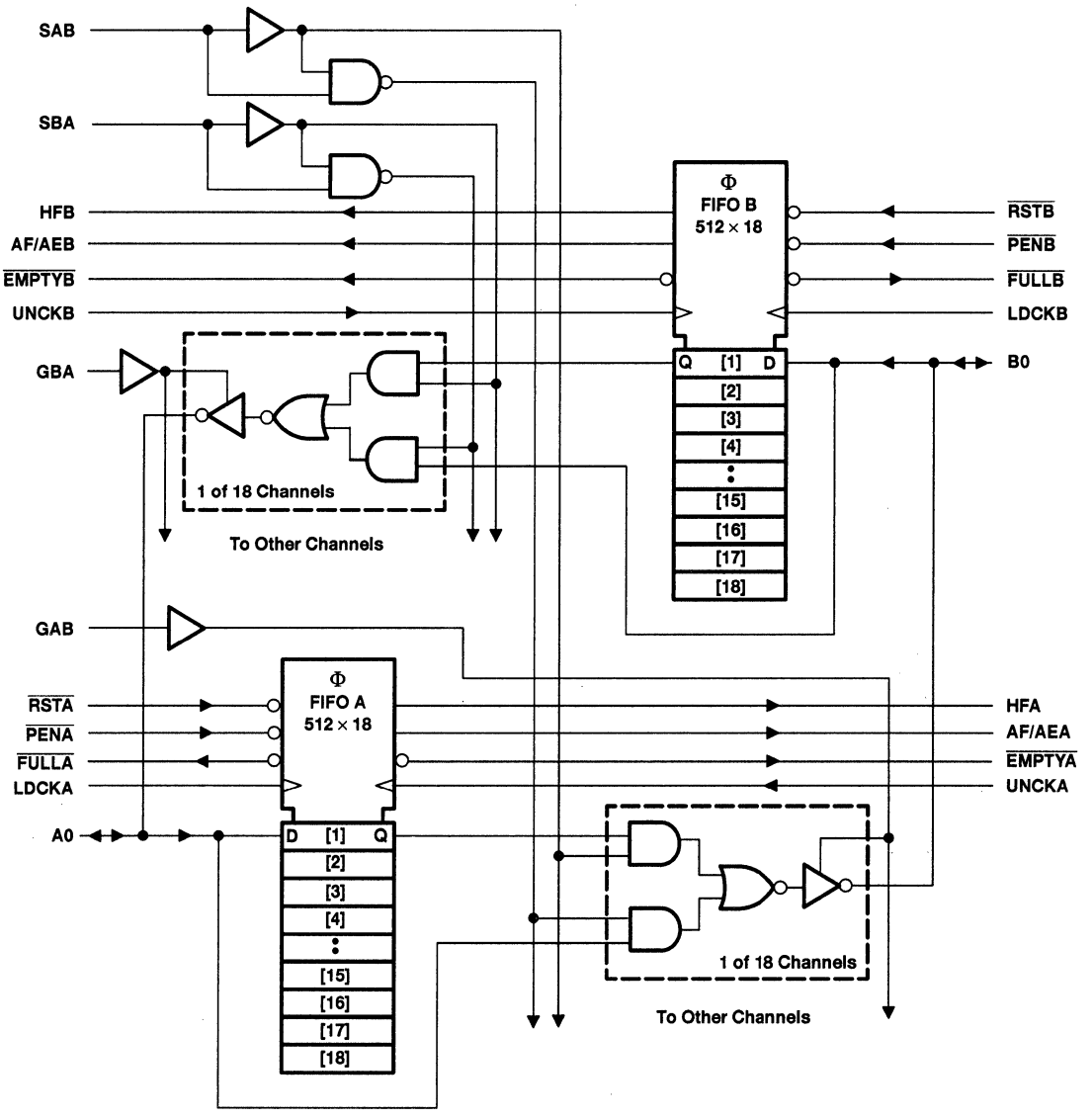
TERMINAL	I/O	DESCRIPTION
A0–A17	I/O	Port-A data. The 18-bit bidirectional data port for side A.
AF/AEA	O	FIFO A almost-full/almost-empty flag. Depth offset values can be programmed for AF/AEA or the default value of 128 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AEA is high when FIFO A contains X or less words or (512 – Y) or more words. AF/AEA is set high after FIFO A is reset.
AF/AEB	O	FIFO B almost-full/almost-empty flag. Depth offset values can be programmed for AF/AEB or the default value of 128 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AEB is high when FIFO B contains X or less words or (512 – Y) or more words. AF/AEB is set high after FIFO B is reset.
B0–B17	I/O	Port-B data. The 18-bit bidirectional data port for side B.
$\overline{\text{EMPTYA}}$	O	FIFO A empty flag. $\overline{\text{EMPTYA}}$ is low when FIFO A is empty and high when FIFO A is not empty. $\overline{\text{EMPTYA}}$ is set low after FIFO A is reset.
$\overline{\text{EMPTYB}}$	O	FIFO B empty flag. $\overline{\text{EMPTYB}}$ is low when FIFO B is empty and high when FIFO B is not empty. $\overline{\text{EMPTYB}}$ is set low after FIFO B is reset.
$\overline{\text{FULLA}}$	O	FIFO A full flag. $\overline{\text{FULLA}}$ is low when FIFO A is full and high when FIFO A is not full. $\overline{\text{FULLA}}$ is set high after FIFO A is reset.
$\overline{\text{FULLB}}$	O	FIFO B full flag. $\overline{\text{FULLB}}$ is low when FIFO B is full and high when FIFO B is not full. $\overline{\text{FULLB}}$ is set high after FIFO B is reset.
GAB	I	Port-B output enable. B0–B17 outputs are active when GAB is high and in the high-impedance state when GAB is low.
GBA	I	Port-A output enable. A0–A17 outputs are active when GBA is high and in the high-impedance state when GBA is low.
HFA	O	FIFO A half-full flag. HFA is high when FIFO A contains 256 or more words and is low when FIFO A contains 255 or less words. HFA is set low after FIFO A is reset.
HFB	O	FIFO B half-full flag. HFB is high when FIFO B contains 256 or more words and is low when FIFO B contains 255 or less words. HFB is set low after FIFO B is reset.
LDCKA	I	FIFO A load clock. Data is written into FIFO A on a low-to-high transition of LDCKA when $\overline{\text{FULLA}}$ is high. The first word written into an empty FIFO A is sent directly to the FIFO A data outputs.
LDCKB	I	FIFO B load clock. Data is written into FIFO B on a low-to-high transition of LDCKB when $\overline{\text{FULLB}}$ is high. The first word written into an empty FIFO B is sent directly to the FIFO B data outputs.
$\overline{\text{PENA}}$	I	FIFO A program enable. After reset and before a word is written into FIFO A, the binary value on A0–A7 is latched as an AF/AEA offset value when $\overline{\text{PENA}}$ is low and LDCKA is high.
$\overline{\text{PENB}}$	I	FIFO B program enable. After reset and before a word is written into FIFO B, the binary value on B0–B7 is latched as an AF/AEB offset value when $\overline{\text{PENB}}$ is low and LDCKB is high.
$\overline{\text{RSTA}}$	I	FIFO A reset. A low level on $\overline{\text{RSTA}}$ resets FIFO A forcing $\overline{\text{EMPTYA}}$ low, HFA low, $\overline{\text{FULLA}}$ high, and AF/AEA high.
$\overline{\text{RSTB}}$	I	FIFO B reset. A low level on $\overline{\text{RSTB}}$ resets FIFO B forcing $\overline{\text{EMPTYB}}$ low, HFB low, $\overline{\text{FULLB}}$ high, and AF/AEB high.
SAB	I	Port-B read select. SAB selects the source of B0–B17 read data. A low level selects real-time data from A0–A17. A high level selects the FIFO A output.
SBA	I	Port-A read select. SBA selects the source of A0–A17 read data. A low level selects real-time data from B0 – B17. A high level selects the FIFO B output.
UNCKA	I	FIFO A unload clock. Data is read from FIFO A on a low-to-high transition of UNCKA when $\overline{\text{EMPTYA}}$ is high.
UNCKB	I	FIFO B unload clock. Data is read from FIFO B on a low-to-high transition of UNCKB when $\overline{\text{EMPTYB}}$ is high.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the PH package.

logic diagram (positive logic)



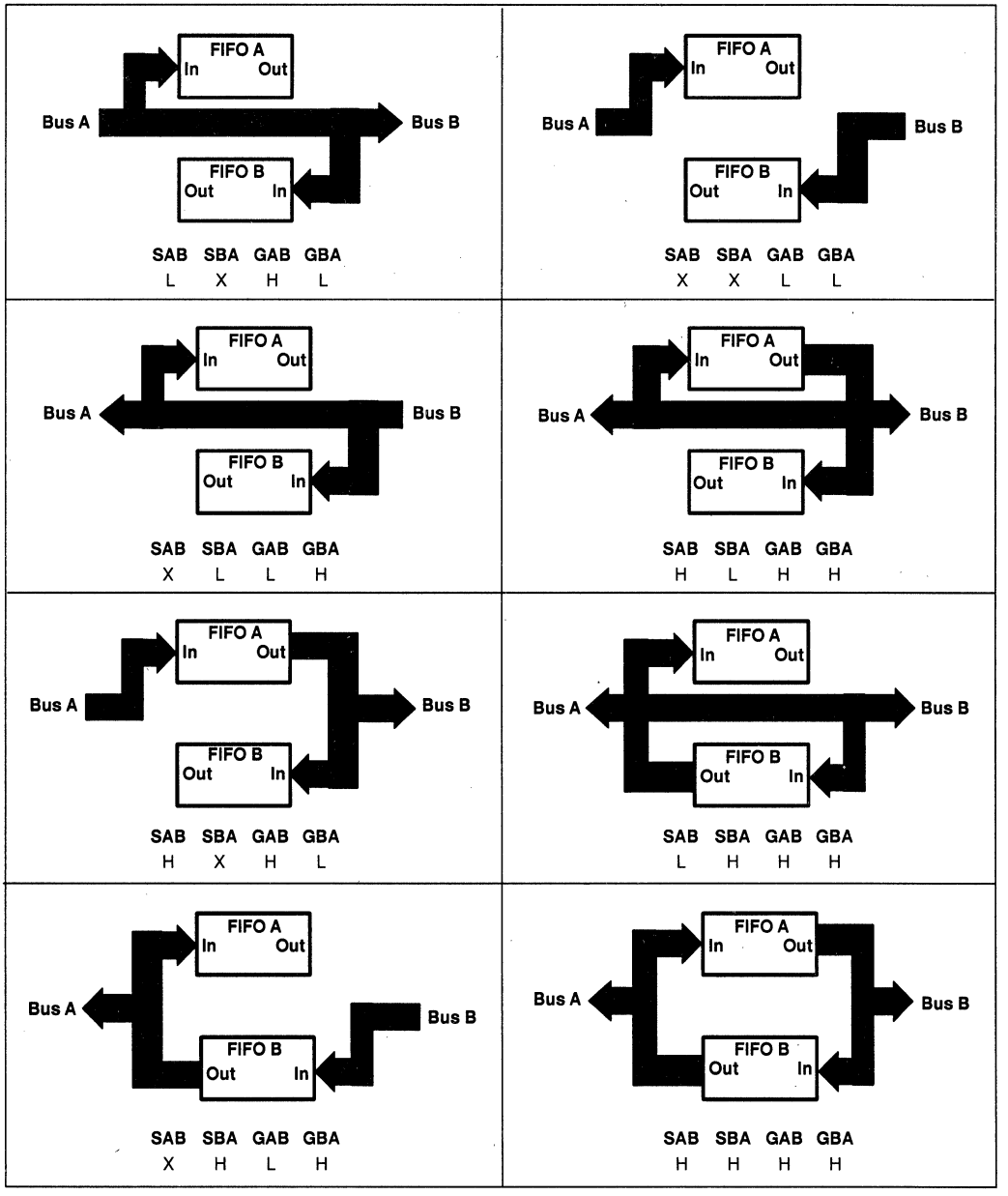


Figure 1. Bus-Management Functions

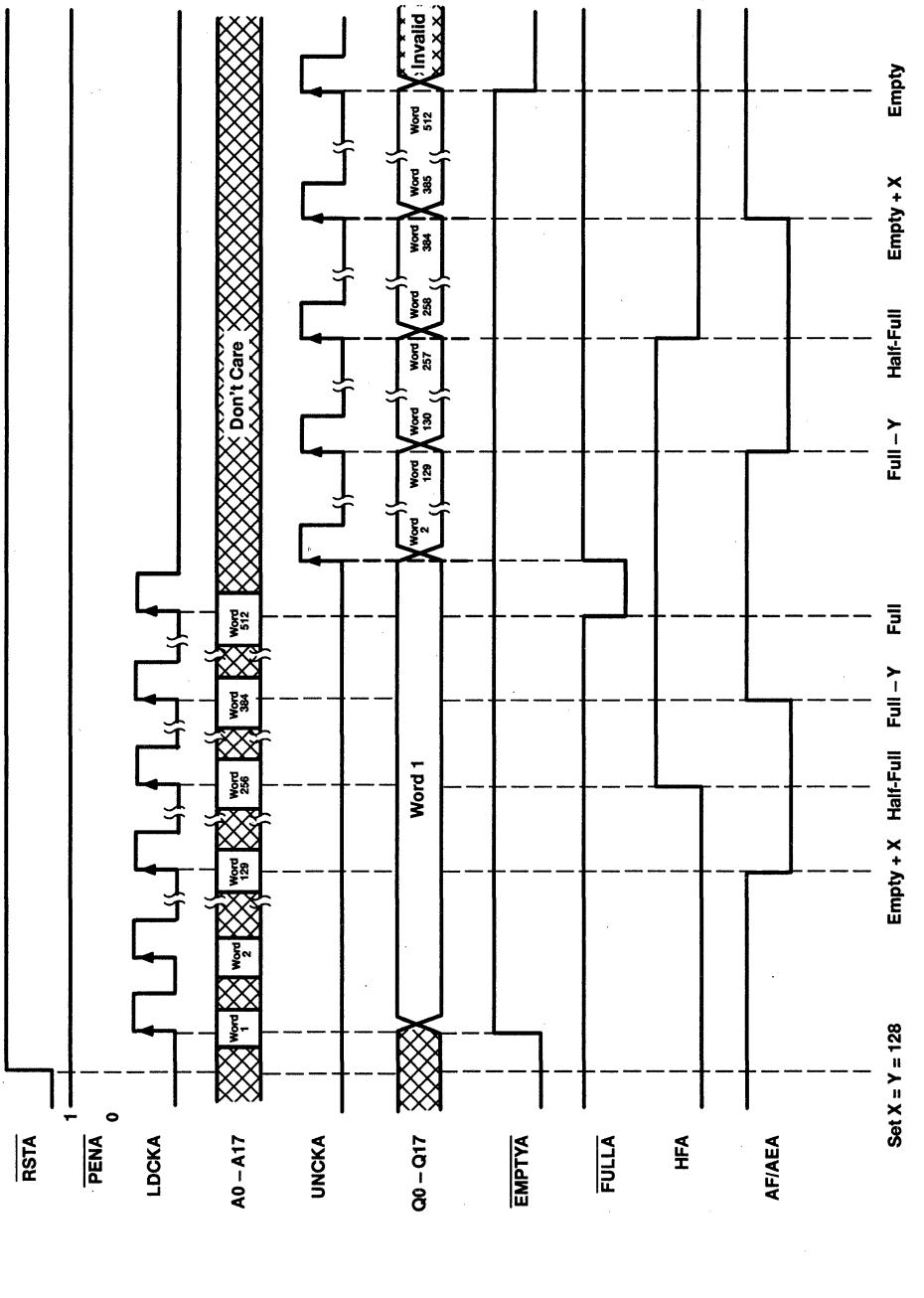
SELECT-MODE CONTROL TABLE

CONTROL		OPERATION	
SBA	SAB	A BUS	B BUS
L	L	Real-time B to A bus	Real-time A to B bus
H	L	FIFO B to A bus	Real-time A to B bus
L	H	Real-time B to A bus	FIFO A to B bus
H	H	FIFO B to A bus	FIFO A to B bus

OUTPUT-ENABLE CONTROL TABLE

CONTROL		OPERATION	
GBA	GAB	A BUS	B BUS
L	L	Isolation/input to A bus	Isolation/input to B bus
H	L	A bus enabled	Isolation/input to B bus
L	H	Isolation/input to A bus	B bus enabled
H	H	A bus enabled	B bus enabled

timing diagram for FIFO A†



† SAB = GAB = H, GBA = L
Operation of FIFO B is identical to that of FIFO A.

offset values for AF/AE

The almost-full/almost-empty flag of each FIFO has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). The offsets of a flag can be programmed from the input of its FIFO after it is reset and before any data is written to its memory. An AF/AE flag is high when its FIFO contains X or less words or (512 – Y) or more words.

To program the offset values for AF/AEA, $\overline{\text{PENA}}$ can be brought low after FIFO A is reset and only when LDCKA is low. On the following low-to-high transition of LDCKA, the binary value on A0–A7 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{\text{PENA}}$ low for another low-to-high transition of LDCKA reprograms Y to the binary value on A0–A7 at the time of the second LDCKA low-to-high transition.

$\overline{\text{PENA}}$ can be brought back high only when LDCKA is low during the first two LDCKA cycles. $\overline{\text{PENA}}$ can be brought high at any time after the second LDCKA pulse returns low. A maximum value of 255 can be programmed for either X or Y (see Figure 2). To use the default values of X = Y = 128 for AF/AEA, $\overline{\text{PENA}}$ must be tied high. No data is stored in the FIFO when its AF/AE offsets are programmed. The AF/AEB flag is programmed in the same manner. $\overline{\text{PENB}}$ enables LDCKB to program the AF/AEB offset values taken from B0–B7.

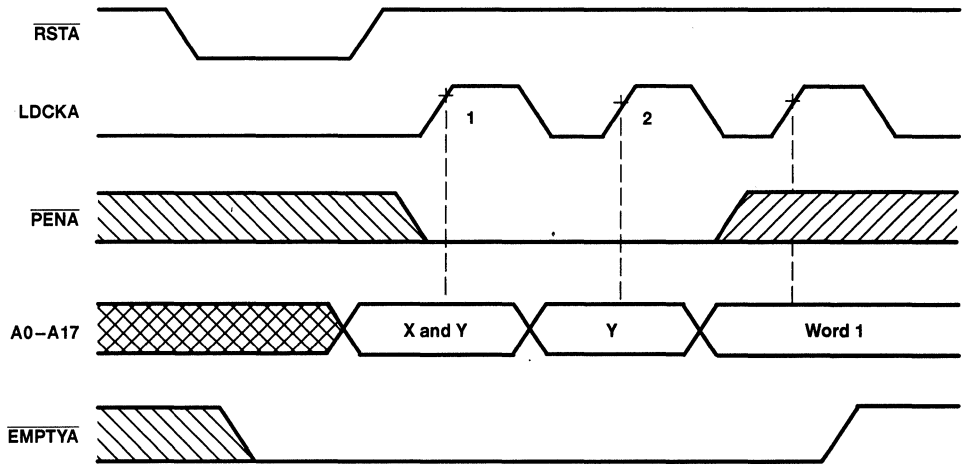


Figure 2. Programming X and Y Separately for AF/AEA

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 48 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	4.5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
I_{OH}	High-level output current			−12	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate			5	ns/V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = − 18 mA				− 1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = − 3 mA		2.5			V
		V_{CC} = 5 V,	I_{OH} = − 3 mA		3			
		V_{CC} = 4.5 V,	I_{OH} = − 12 mA		2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 24 mA				0.55	V
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±5	µA
I_{OZH}§		V_{CC} = 5.5 V,	V_O = 2.7 V				50	µA
I_{OZL}§		V_{CC} = 5.5 V,	V_O = 0.5 V				− 50	µA
I_O¶		V_{CC} = 5.5 V,	V_O = 2.5 V		− 40	− 100	− 180	mA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	Outputs high			15	mA
			V_I = V_{CC} or GND	Outputs low			95	
				Outputs disabled			15	
C_i	Control inputs	V_I = 2.5 V or 0.5 V				6		pF
C_o	Flags	V_O = 2.5 V or 0.5 V				4		pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V				8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ The parameters I_{OZH} and I_{OZL} include the input leakage current.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			'ABT7820-15		'ABT7820-20		'ABT7820-25		'ABT7820-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		67		50		40		33		MHz
t_w	Pulse duration	LDCKA, LDCKB high	4		6		9		11		ns
		LDCKA, LDCKB low	4		6		9		11		
		UNCKA, UNCKB high	4		6		9		11		
		UNCKA, UNCKB low	4		6		9		11		
		$\overline{RSTA}$, $\overline{RSTB}$ low	6		8		10		12		
t_{su}	Setup time	A0–A17 before LDCKA↑ and B0–B17 before LDCKB↑	3		4		4		4		ns
		$\overline{PENA}$ before LDCKA↑ and $\overline{PENB}$ before LDCKB↑	5		5		5		5		
		LDCKA inactive before $\overline{RSTA}$ high and LDCKB inactive before $\overline{RSTB}$ high	3		3		4		4		
t_h	Hold time	A0–A17 after LDCKA↑ and B0–B17 after LDCKB↑	0		0		0		0		ns
		$\overline{PENA}$ after LDCKA low and $\overline{PENB}$ after LDCKB low	2		2		2		2		
		LDCKA inactive after $\overline{RSTA}$ high and LDCKB inactive after $\overline{RSTB}$ high	3		3		4		4		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7820-15			'ACT7820-20		'ACT7820-25		'ACT7820-30		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK, UNCK				67		50		40		33.3	MHz
t_{pd}	LDCKA↑, LDCKB↑	B/A	4		14	4	15	4	18	4	20	ns
	UNCKA↑, UNCKB↑		4	9	12	4	13.5	4	15	4	17	
t_{pd}‡	UNCKA↑, UNCKB↑	B/A		8								ns
t_{PLH}	LDCKA↑, LDCKB↑	$\overline{EMPTYA}$, $\overline{EMPTYB}$	4		14	4	15	4	17	4	19	ns
t_{PHL}	UNCKA↑, UNCKB↑		4		13	4	14	4	16	4	18	
t_{PHL}	$\overline{RSTA}$ low, $\overline{RSTB}$ low	$\overline{EMPTYA}$, $\overline{EMPTYB}$	6		16	6	16	6	18	6	20	ns
t_{PHL}	LDCKA↑, LDCKB↑	$\overline{FULLA}$, $\overline{FULLB}$	6		13	6	14	6	16	6	18	ns
t_{PLH}	UNCKA↑, UNCKB↑	$\overline{FULLA}$, $\overline{FULLB}$	6		15	6	15	6	17	6	19	ns
	$\overline{RSTA}$ low, $\overline{RSTB}$ low		8		20	8	20	8	22	8	22	
t_{pd}	LDCKA↑, LDCKB↑	AF/AEA, AF/AEB	8		16	8	17	8	18	8	20	ns
	UNCKA↑, UNCKB↑		8		16	8	17	8	18	8	20	
t_{PLH}	$\overline{RSTA}$ low, $\overline{RSTB}$ low	AF/AEA, AF/AEB	2		12	2	14	2	16	2	18	ns
t_{PLH}	LDCKA↑, LDCKB↑	HFA, HFB	8		15	8	15	8	17	8	19	ns
t_{PHL}	UNCKA, UNCKB	HFA, HFB	8		15	8	15	8	17	8	19	ns
	$\overline{RSTA}$ low, $\overline{RSTB}$ low		2		12	2	14	2	16	2	18	
t_{pd}	SAB/SBA§	B/A	2		10	2	11	2	12	2	14	ns
	A/B		2		9	2	10	2	11	2	13	
t_{en}	GBA/GAB	A/B	2		6.5	2	8	2	10	2	12	ns
t_{dis}	GBA/GAB	A/B	2		11	2	12	2	13	2	14	ns

† All typical values are at 5 V, T_A = 25°C.
‡ This parameter is measured with a 30-pF load (see Figure 3).
§ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

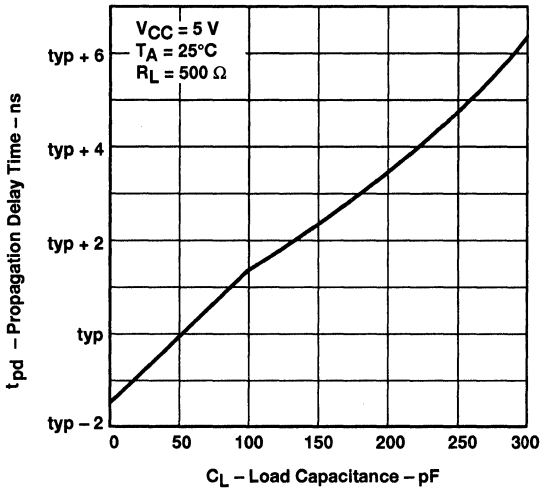


Figure 3

SUPPLY CURRENT
vs
CLOCK FREQUENCY

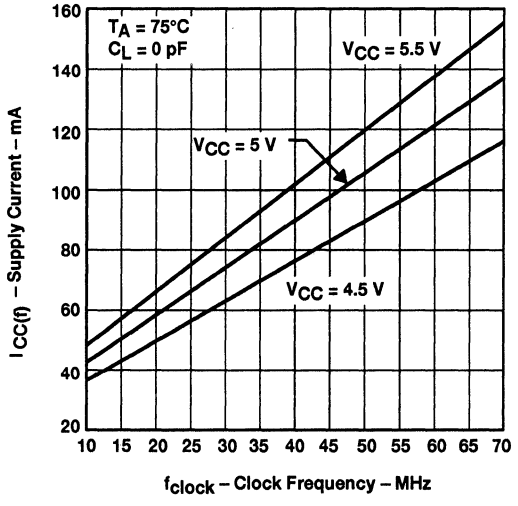


Figure 4

TYPICAL CHARACTERISTICS

calculating power dissipation

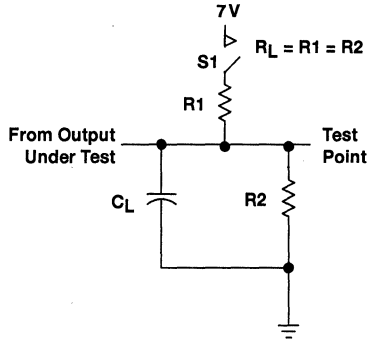
With $I_{CC(f)}$ taken from Figure 4, the maximum power dissipation (P_T) based on all outputs changing states on each read can be calculated using:

$$P_T = V_{CC} \times I_{CC(f)} + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

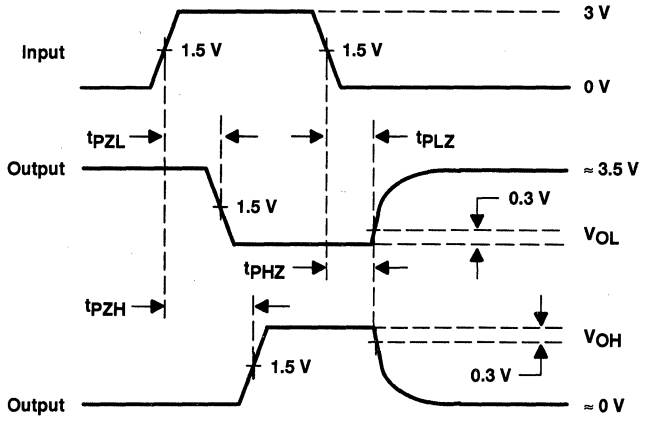
where:

$I_{CC(f)}$ = maximum I_{CC} per clock frequency
C_L = output capacitive load
f_o = data output frequency

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

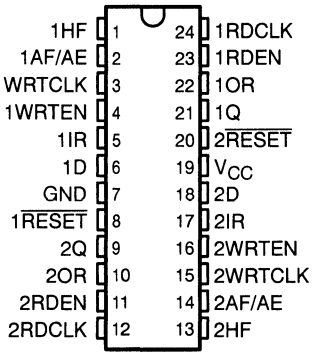
PARAMETER		R1, R2	CL†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test-fixture capacitance

Figure 5. Load Circuit and Voltage Waveforms

- **Dual Independent FIFOs Organized as:**
  64 Words by 1 Bit Each – SN74ACT2226
  256 Words by 1 Bit Each – SN74ACT2228
- **Free-Running Read and Write Clocks Can Be Asynchronous or Coincident on Each FIFO**
- **Input-Ready Flags Synchronized to Write Clocks**
- **Output-Ready Flags Synchronized to Read Clocks**
- **Half-Full and Almost-Full/Almost-Empty Flags**
- **Support Clock Frequencies up to 22 MHz**
- **Characterized for Operation Over the Industrial Temperature Range (–40°C to 85°C)**
- **Access Times of 20 ns**
- **Low-Power Advanced CMOS Technology**
- **Available in 24-Pin SOIC (DW) Package**

DW PACKAGE
(TOP VIEW)



description

The SN74ACT2226 and SN74ACT2228 are dual FIFOs suited for a wide range of serial data buffering applications including elastic stores for frequencies up to T2 telecommunication rates. Each FIFO on the chip is arranged as 64 × 1 (SN74ACT2226) or 256 × 1 (SN74ACT2228) and has control signals and status flags for independent operation. Output flags per FIFO include input ready (1IR or 2IR), output ready (1OR or 2OR), half full (1HF or 2HF), and almost full/almost empty (1AF/AE or 2AF/AE).

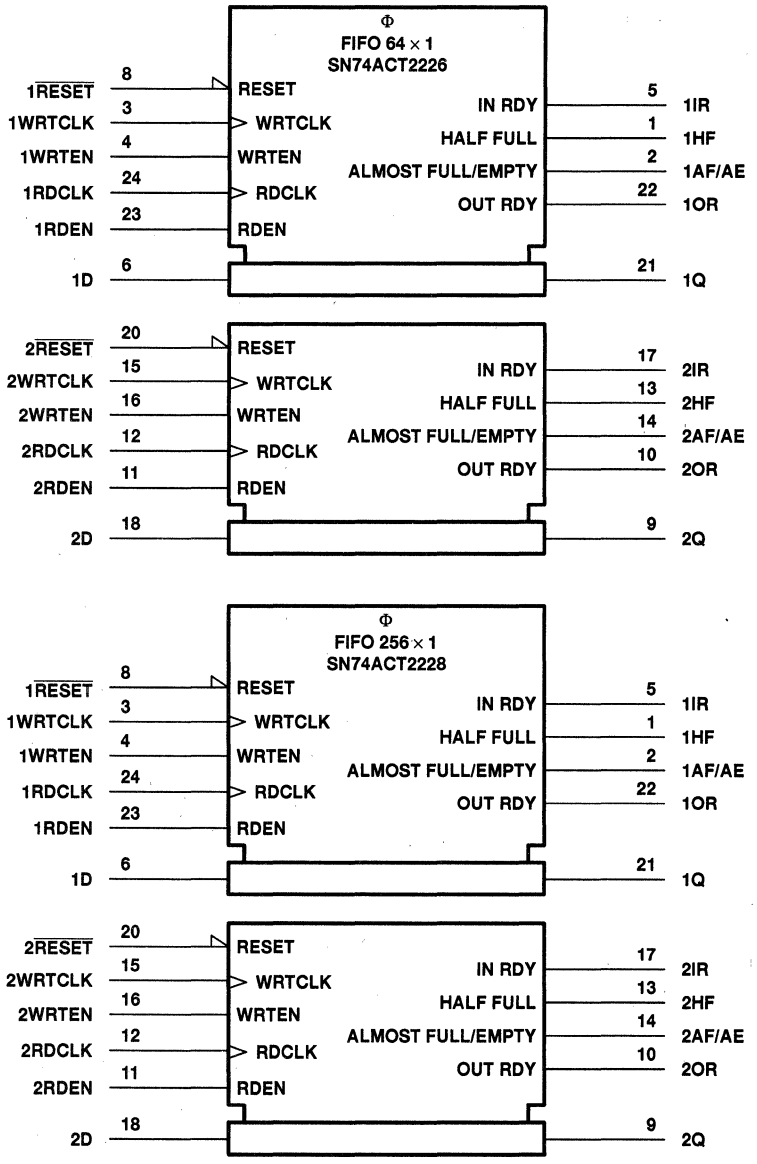
Serial data is written into a FIFO on the low-to-high transition of the write-clock (1WRTCLK or 2WRTCLK) input when the write-enable (1WRTEN or 2WRTEN) input and input-ready flag (1IR or 2IR) output are both high. Serial data is read from a FIFO on the low-to-high transition of the read-clock (1RDCLK or 2RDCLK) input when the read-enable (1RDEN or 2RDEN) input and output-ready flag (1OR or 2OR) output are both high. The read and write clocks of a FIFO can be asynchronous to one another.

Each input-ready flag (1IR or 2IR) is synchronized by two flip-flop stages to its write clock (1WRTCLK or 2WRTCLK), and each output-ready flag (1OR or 2OR) is synchronized by three flip-flop stages to its read clock (1RDCLK or 2RDCLK). This multistage synchronization ensures reliable flag-output states when data is written and read asynchronously.

A half-full flag (1HF or 2HF) is high when the number of bits stored in its FIFO is greater than or equal to half the depth of the FIFO. An almost-full/almost-empty flag (1AF/AE or 2AF/AE) is high when eight or less bits are stored in its FIFO and when eight or fewer empty locations are left in the FIFO. A bit present on the data output is not stored in the FIFO.

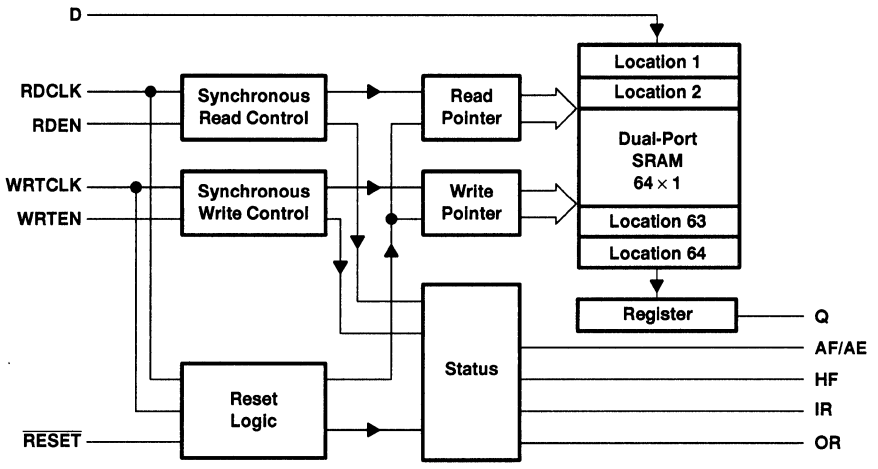
The SN74ACT2226 and SN74ACT2228 are characterized for operation from –40°C to 85°C.

logic symbols†

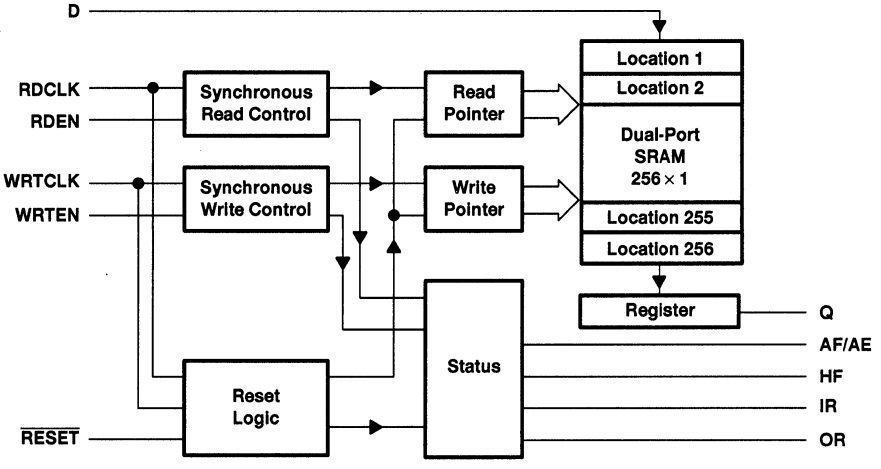


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ACT2226 functional block diagram (each FIFO)



SN74ACT2228 functional block diagram (each FIFO)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
1AF/AE 2AF/AE	2 14	O	Almost-full/almost-empty flag. AF/AE is high when the memory is eight locations or less from a full or empty state. AF/AE is set high after reset.
1D 2D	6 18	I	Data input
GND	7		Ground
1HF 2HF	1 15	O	Half-full flag. HF is high when the number of bits stored in memory is greater than or equal to half the FIFO depth. HF is set low after reset.
1IR 2IR	5 17	O	Input-ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is set low during reset and is set high on the second low-to-high transition of WRTCLK after reset.
1OR 2OR	22 10	O	Output-ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on the data output when OR is high. OR is set low during reset and set high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory.
1Q 2Q	21 9	O	Data outputs. After the first valid write to empty memory, the first bit is output on the third rising edge of RDCLK. OR for the FIFO is asserted high to indicate ready data.
1RDCLK 2RDCLK	24 12	I	Read clock. RDCLK is a continuous clock and can be independent of any other clock on the device. A low-to-high transition of RDCLK reads data from memory when the FIFO RDEN and OR are high. OR is synchronous with the low-to-high transition of RDCLK.
1RDEN 2RDEN	23 11	I	Read enable. When the RDEN and OR of a FIFO are high, data is read from the FIFO on the low-to-high transition of RDCLK.
1$\overline{\text{RESET}}$ 2$\overline{\text{RESET}}$	8 20	I	Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{\text{RESET}}$ is low. This sets HF, IR, and OR low and AF/AE high. Before it is used, a FIFO must be reset after power up.
V_{CC}	19		Supply voltage
1WRTCLK 2WRTCLK	3 15	I	Write clock. WRTCLK is a continuous clock and can be independent of any other clock on the device. A low-to-high transition of WRTCLK writes data to memory when WRTEN and IR are high. IR is synchronous with the low-to-high transition of WRTCLK.
1WRTEN 2WRTEN	4 16	I	Write enable. When WRTEN and IR are high, data is written to the FIFO on a low-to-high transition of WRTCLK.

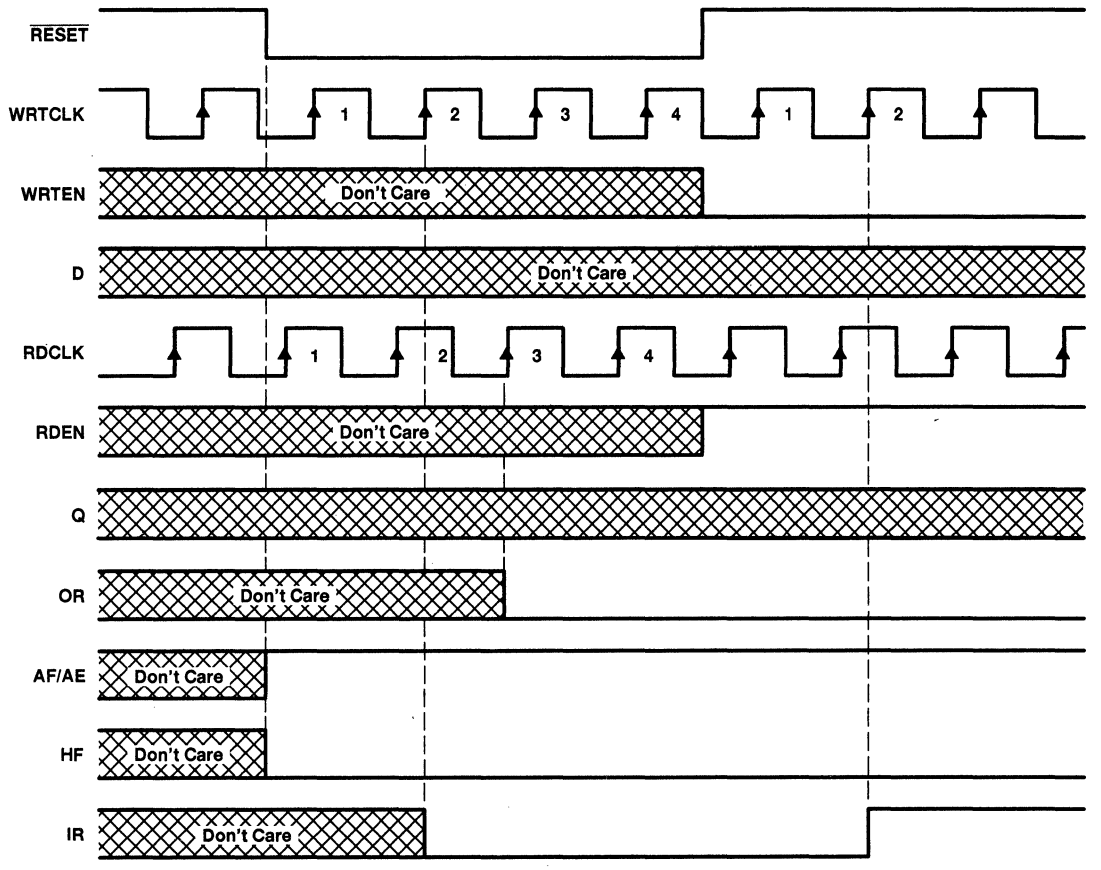
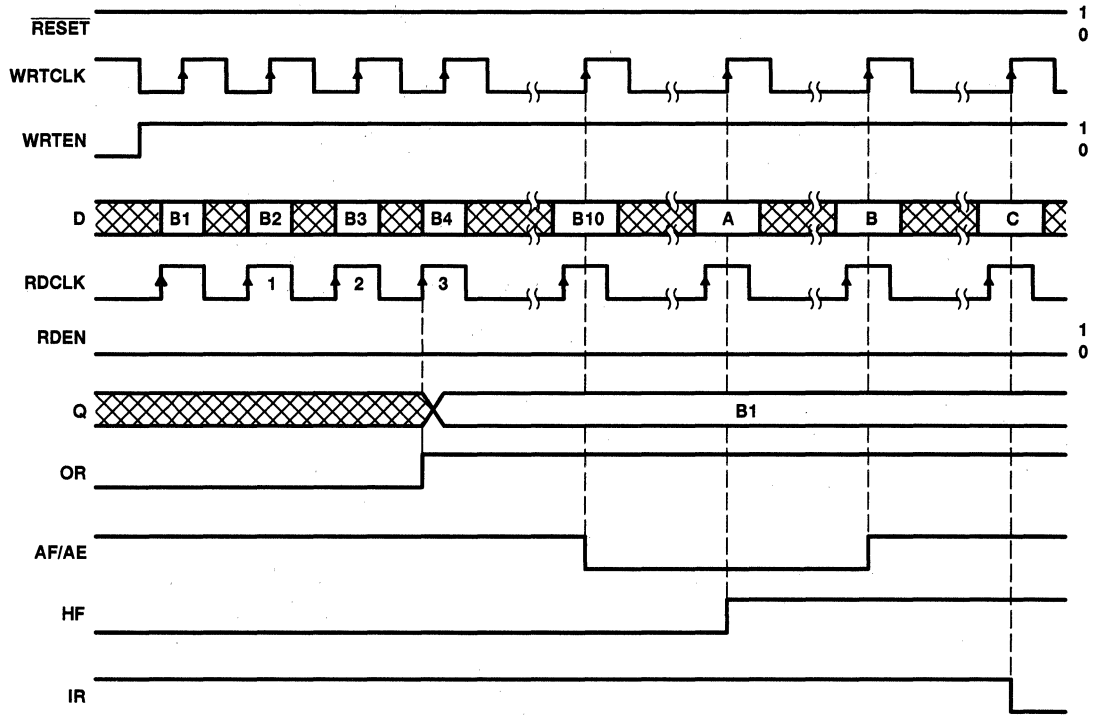


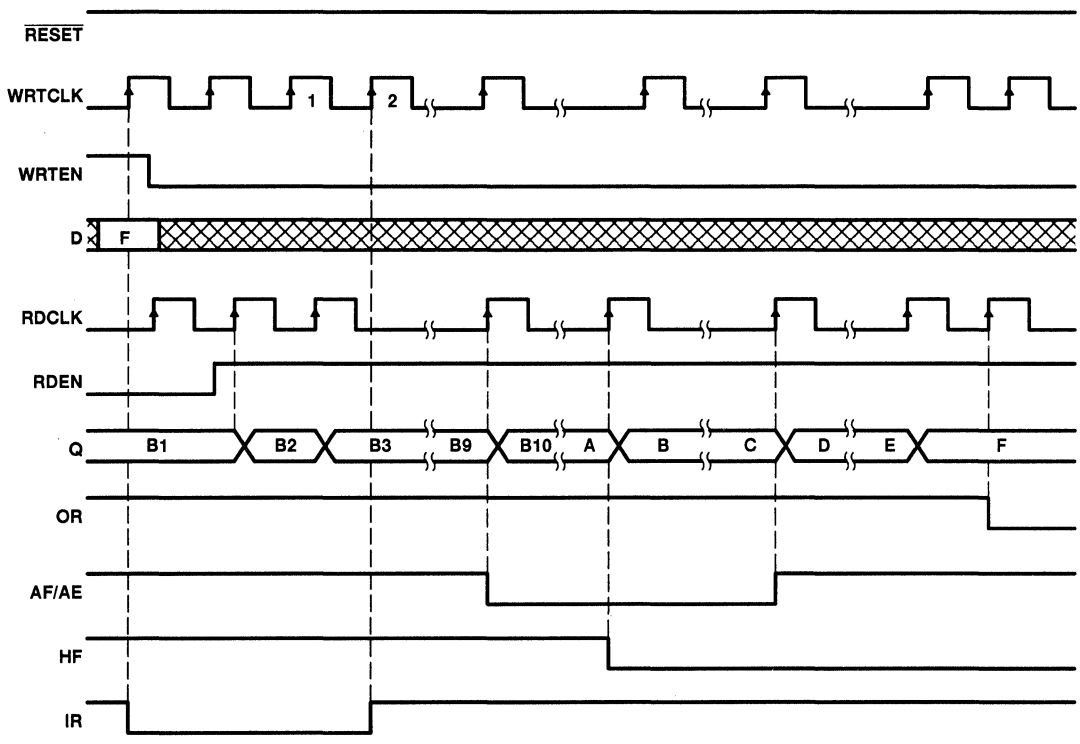
Figure 1. FIFO Reset



DATA BIT NUMBER BASED ON FIFO DEPTH

DEVICE	DATA BIT		
	A	B	C
SN74ACT2226	B33	B57	B65
SN74ACT2228	B129	B249	B257

Figure 2. FIFO Write



DATA BIT NUMBER BASED ON FIFO DEPTH

DEVICE	DATA BIT					
	A	B	C	D	E	F
SN74ACT2226	B33	B34	B56	B57	B64	B65
SN74ACT2228	B129	B130	B248	B249	B256	B257

Figure 3. FIFO Read

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±200 mA
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided that the input and output current ratings are observed.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	Q outputs, Flags		−8	mA
I_{OL}	Low-level output current	Q outputs		16	mA
		Flags		8	
T_A	Operating free-air temperature		−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = − 8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	µA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	µA
I_{CC}		V_I = V_{CC} − 0.2 V or 0					400	µA
ΔI_{CC}‡		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 1 through 3)

			MIN	MAX	UNIT
f_{clock}	Clock frequency			22	MHz
t_w	Pulse duration	1WRTCLK, 2WRTCLK high or low	15		ns
		1RDCLK, 2RDCLK high or low	15		
t_{su}	Setup time	1D before 1WRTCLK↑ and 2D before 2WRTCLK↑	6		ns
		1WRTEN before 1WRTCLK↑ and 2WRTEN before 2WRTCLK↑	6		
		1RDEN before 1RDCLK↑ and 2RDEN before 2RDCLK↑	6		
		1$\overline{\text{RESET}}$ low before 1WRTCLK↑ and 2$\overline{\text{RESET}}$ low before 2WRTCLK↑§	6		
		1$\overline{\text{RESET}}$ low before 1RDCLK↑ and 2$\overline{\text{RESET}}$ low before 2RDCLK↑§	6		
t_h	Hold time	1D after 1WRTCLK↑ and 2D after 2WRTCLK↑	0		ns
		1WRTEN after 1WRTCLK↑ and 2WRTEN after 2WRTCLK↑	0		
		1RDEN after 1RDCLK↑ and 2RDEN after 2RDCLK↑	0		
		1$\overline{\text{RESET}}$ low after 1WRTCLK↑ and 2$\overline{\text{RESET}}$ low after 2WRTCLK↑§	6		
		1$\overline{\text{RESET}}$ low after 1RDCLK↑ and 2$\overline{\text{RESET}}$ low after 2RDCLK↑§	6		

§ Requirement to count the clock edge as one of at least four needed to reset a FIFO

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}	1WRTCLK, 2WRTCLK, or 1RDCLK, 2RDCLK		22		MHz
t_{pd}	1RDCLK↑, 2RDCLK↑	1Q, 2Q	2	20	ns
t_{pd}	1WRTCLK↑, 2WRTCLK↑	1IR, 2IR	1	20	ns
t_{pd}	1RDCLK↑, 2RDCLK↑	1OR, 2OR	1	20	ns
t_{pd}	1WRTCLK↑, 2WRTCLK↑	1AF/AE, 2AF/AE	3	20	ns
	1RDCLK↑, 2RDCLK↑		3	20	
t_{PLH}	1WRTCLK↑, 2WRTCLK↑	1HF, 2HF	2	20	ns
t_{PHL}	1RDCLK↑, 2RDCLK↑		3	20	
t_{PLH}	$\overline{1RESET}$, $\overline{2RESET}$ low	1AF/AE, 2AF/AE	1	20	ns
t_{PHL}		1HF, 2HF	1	20	

PARAMETER MEASUREMENT INFORMATION

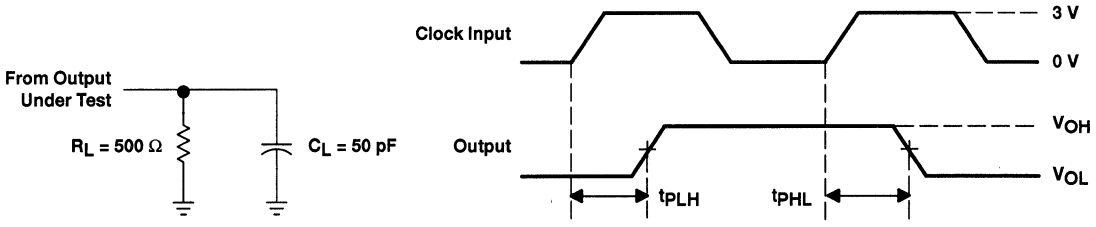


Figure 4. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

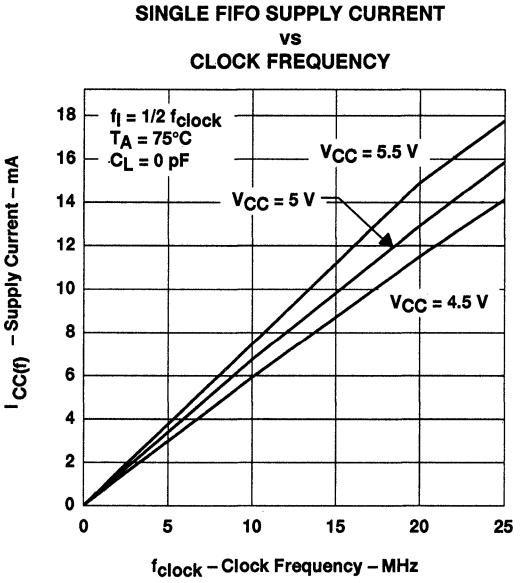


Figure 5

calculating power dissipation

Data for Figure 5 is taken with one FIFO active and one FIFO idle on the device. The active FIFO has both writes and reads enabled with its read clock (RDCLK) and write clock (WRTCLK) operating at the rate specified by f_{clock}. The data input rate and data output rate are half the f_{clock} rate, and the data output is disconnected. A close approximation to the total device power can be found by using Figure 5, determining the capacitive load on the data output and determining the number of SN74ACT2226/2228 inputs driven by TTL high levels.

With $I_{CC(f)}$ taken from Figure 5, the maximum power dissipation (P_T) of one FIFO on the SN74ACT2226 or SN74ACT2228 can be calculated by:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + (C_L \times V_{CC}^2 \times f_o)$$

where:

N	=	number of inputs driven by TTL levels
ΔI_{CC}	=	increase in power supply current for each input at a TTL high level
dc	=	duty cycle of inputs at a TTL high level of 3.4 V
C_L	=	output capacitive load
f_o	=	switching frequency of an output

APPLICATION INFORMATION

An example of concentrating two independent serial data signals into a single composite data signal with the use of an SN74ACT2226 or SN74ACT2228 device is shown in Figure 6. The input data to the FIFOs share the same average (mean) frequency, and the mean frequency of the SYS_CLOCK is greater than or equal to the sum of the individual mean input rates. A single-bit FIFO is needed for each additional input data signal that is time-division multiplexed into the composite signal.

The FIFO memories provide a buffer to absorb clock jitter generated by the transmission systems of incoming signals and synchronize the phase-independent inputs to one another. FIFO half-full (HF) flags are used to signal the multiplexer to start fetching data from the buffers. The state of the flags can also be used to indicate when a FIFO read should be suppressed to regulate the output flow (pulse-stuffing control). The FIFO almost-full/almost-empty flags (AF/AE) can be used in place of the half-full flags to reduce transmission delay.

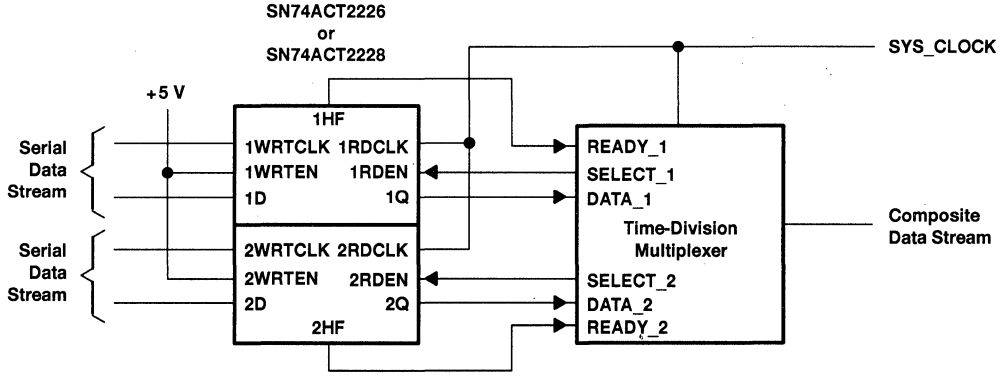
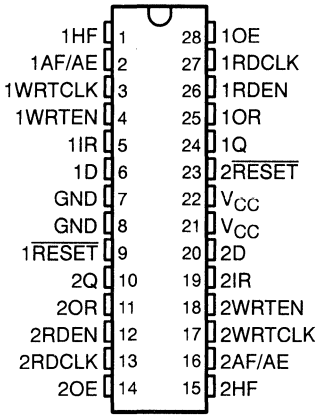


Figure 6. Time-Division Multiplexing Using the SN74ACT2226 or SN74ACT2228

- **Dual Independent FIFOs Organized as:**
  64 Words by 1 Bit Each – SN74ACT2227
  256 Words by 1 Bit Each – SN74ACT2229
- **Free-Running Read and Write Clocks Can Be Asynchronous or Coincident on Each FIFO**
- **Input-Ready Flags Synchronized to Write Clocks**
- **Output-Ready Flags Synchronized to Read Clocks**
- **Half-Full and Almost-Full/Almost-Empty Flags**
- **Characterized for Operation Over the Industrial Temperature Range (–40°C to 85°C)**
- **Support Clock Frequencies up to 60 MHz**
- **Access Times of 9 ns**
- **3-State Data Outputs**
- **Low-Power Advanced CMOS Technology**
- **Available in 28-Pin SOIC (DW) Package**

DW PACKAGE
(TOP VIEW)



description

The SN74ACT2227 and SN74ACT2229 are dual FIFOs suited for a wide range of serial data buffering applications including elastic stores for frequencies up to OC-1 telecommunication rates. Each FIFO on the chip is arranged as 64 × 1 (SN74ACT2227) or 256 × 1 (SN74ACT2229) and has control signals and status flags for independent operation. Output flags per FIFO include input ready (1IR or 2IR), output ready (1OR or 2OR), half full (1HF or 2HF), and almost full/almost empty (1AF/AE or 2AF/AE).

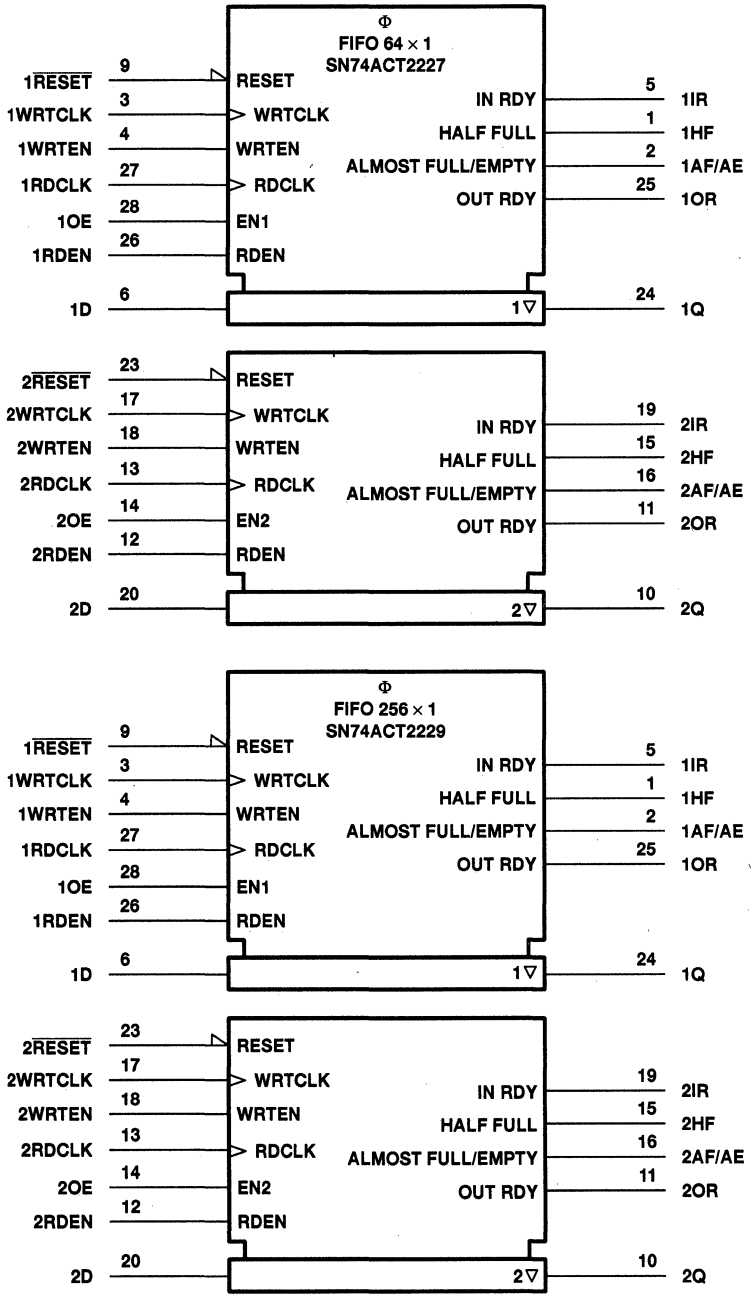
Serial data is written into a FIFO on the low-to-high transition of the write-clock (1WRTCLK or 2WRTCLK) input when the write-enable (1WRTEN or 2WRTEN) input and input-ready flag (1IR or 2IR) output are both high. Serial data is read from a FIFO on the low-to-high transition of the read-clock (1RDCLK or 2RDCLK) input when the read-enable (1RDEN or 2RDEN) input and output-ready flag (1OR or 2OR) output are both high. The read and write clocks of a FIFO can be asynchronous to one another. A FIFO data output (1Q or 2Q) is in the high-impedance state when its output-enable (1OE or 2OE) input is low.

Each input-ready flag (1IR or 2IR) is synchronized by two flip-flop stages to its write clock (1WRTCLK or 2WRTCLK), and each output-ready flag (1OR or 2OR) is synchronized by three flip-flop stages to its read clock (1RDCLK or 2RDCLK). This multistage synchronization ensures reliable flag-output states when data is written and read asynchronously.

A half-full flag (1HF or 2HF) is high when the number of bits stored in its FIFO is greater than or equal to half the depth of the FIFO. An almost-full/almost-empty flag (1AF/AE or 2AF/AE) is high when eight or less bits are stored in its FIFO and when eight or fewer empty locations are left in the FIFO. A bit present on the data output is not stored in the FIFO.

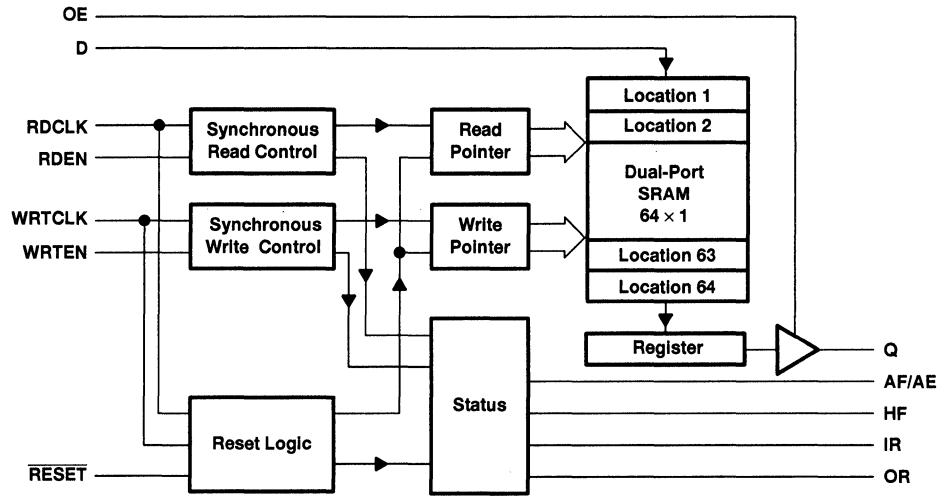
The SN74ACT2227 and SN74ACT2229 are characterized for operation from –40°C to 85°C.

logic symbols†

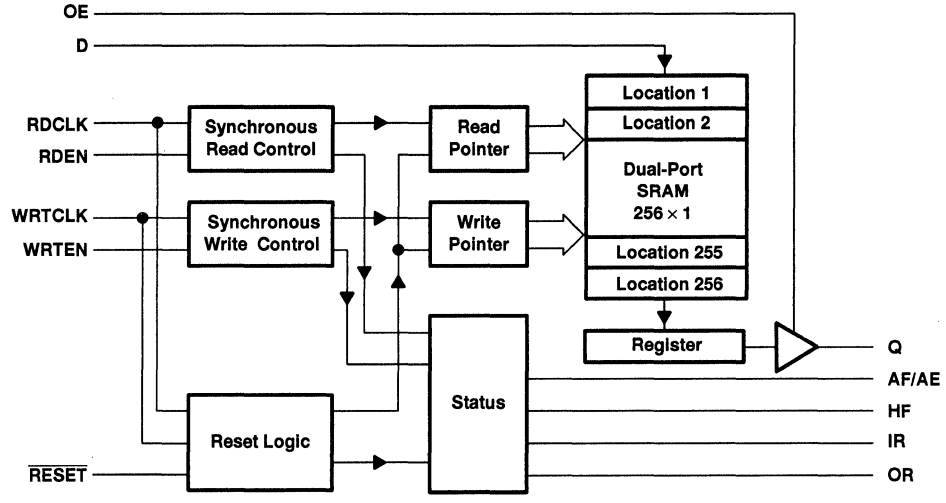


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ACT2227 functional block diagram (each FIFO)



SN74ACT2229 functional block diagram (each FIFO)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
1AF/AE 2AF/AE	2 16	O	Almost-full/almost-empty flag. AF/AE is high when the memory is eight locations or less from a full or empty state. AF/AE is set high after reset.
1D 2D	6 20	I	Data input
GND	7, 8		Ground
1HF 2HF	1 15	O	Half-full flag. HF is high when the number of bits stored in memory is greater than or equal to half the FIFO depth. HF is set low after reset.
1IR 2IR	5 19	O	Input-ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is set low during reset and is set high on the second low-to-high transition of WRTCLK after reset.
1OE 2OE	28 14	I	Output enable. The data output of a FIFO is active when OE is high and in the high-impedance state when OE is low.
1OR 2OR	25 11	O	Output-ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on the data output when OR is high. OR is set low during reset and set high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory.
1Q 2Q	24 10	O	Data outputs. After the first valid write to empty memory, the first bit is output on the third rising edge of RDCLK. OR for the FIFO is asserted high to indicate ready data.
1RDCLK 2RDCLK	27 13	I	Read clock. RDCLK is a continuous clock and can be independent of any other clock on the device. A low-to-high transition of RDCLK reads data from memory when the FIFO RDEN and OR are high. OR is synchronous with the low-to-high transition of RDCLK.
1RDEN 2RDEN	26 12	I	Read enable. When the RDEN and OR of a FIFO are high, data is read from the FIFO on the low-to-high transition of RDCLK.
1$\overline{\text{RESET}}$ 2$\overline{\text{RESET}}$	9 23	I	Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{\text{RESET}}$ is low. This sets HF, IR, and OR low and AF/AE high. Before it is used, a FIFO must be reset after power up.
V_{CC}	21, 22		Supply voltage
1WRTCLK 2WRTCLK	3 17	I	Write clock. WRTCLK is a continuous clock and can be independent of any other clock on the device. A low-to-high transition of WRTCLK writes data to memory when WRTEN and IR are high. IR is synchronous with the low-to-high transition of WRTCLK.
1WRTEN 2WRTEN	4 18	I	Write enable. When WRTEN and IR are high, data is written to the FIFO on a low-to-high transition of WRTCLK.

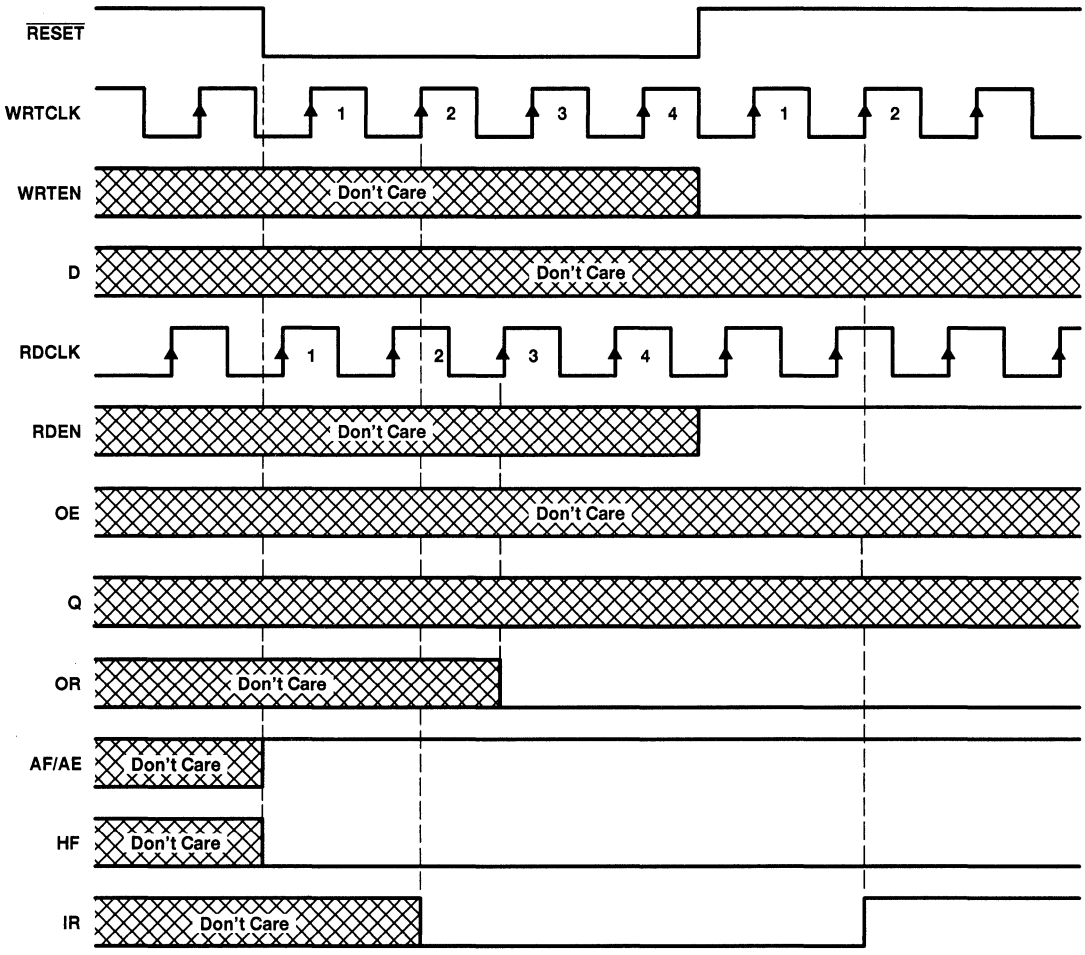
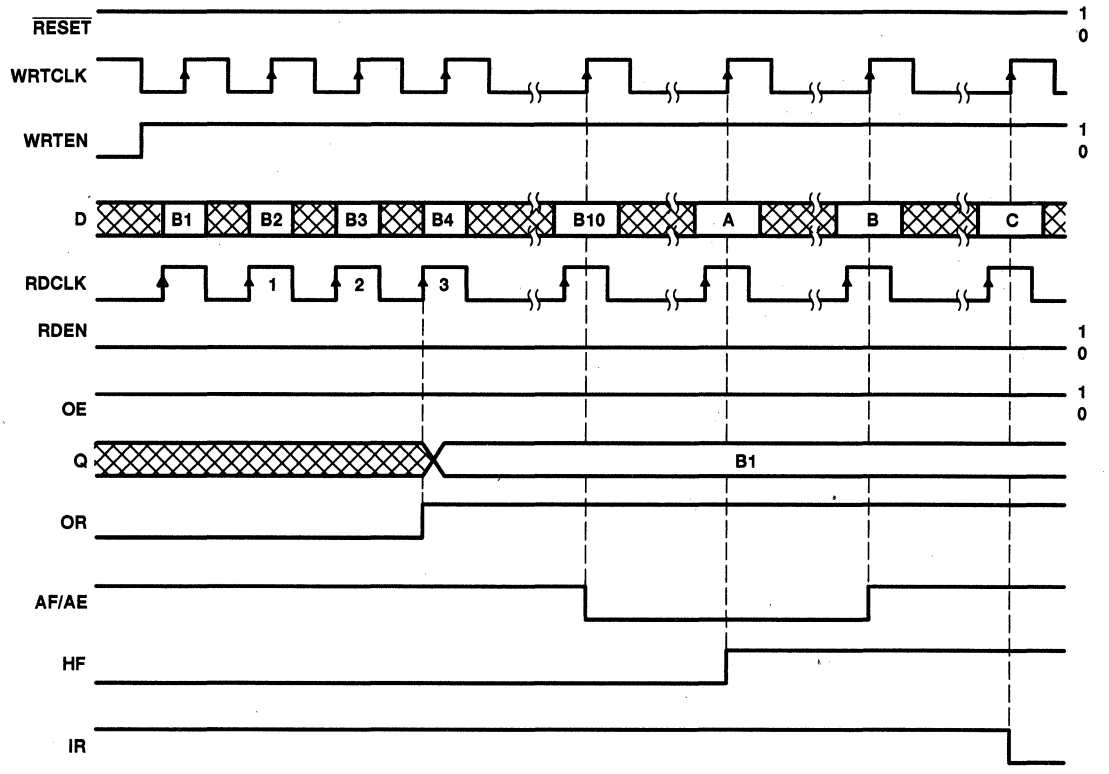


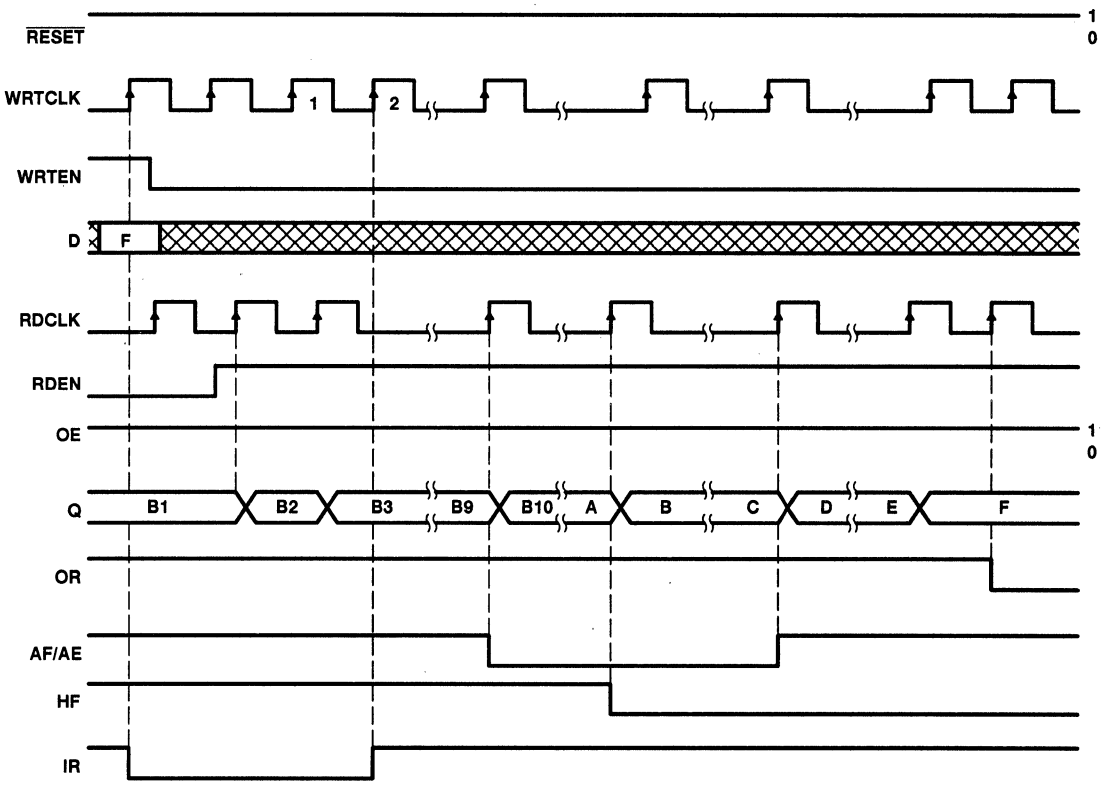
Figure 1. FIFO Reset



DATA BIT NUMBER BASED ON FIFO DEPTH

DEVICE	DATA BIT		
	A	B	C
SN74ACT2227	B33	B57	B65
SN74ACT2229	B129	B249	B257

Figure 2. FIFO Write



DATA BIT NUMBER BASED ON FIFO DEPTH

DEVICE	DATA BIT					
	A	B	C	D	E	F
SN74ACT2227	B33	B34	B56	B57	B64	B65
SN74ACT2229	B129	B130	B248	B249	B256	B257

Figure 3. FIFO Read

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±200 mA
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided that the input and output current ratings are observed.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	Q outputs, Flags		−8	mA
I_{OL}	Low-level output current	Q outputs		16	mA
		Flags		8	
T_A	Operating free-air temperature		−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = − 8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	$V_I = V_{CC}$ or 0				±5	µA
I_{OZ}		V_{CC} = 5.5 V,	$V_O = V_{CC}$ or 0				±5	µA
I_{CC}		$V_I = V_{CC}$ − 0.2 V or 0					400	µA
ΔI_{CC}§		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 1 through 3)

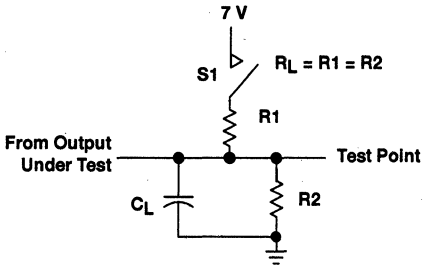
			MIN	MAX	UNIT
f_{clock}	Clock frequency			60	MHz
t_w	Pulse duration	1WRTCLK, 2WRTCLK high or low	5		ns
		1RDCLK, 2RDCLK high or low	5		
t_{su}	Setup time	1D before 1WRTCLK↑ and 2D before 2WRTCLK↑	4.5		ns
		1WRTEN before 1WRTCLK↑ and 2WRTEN before 2WRTCLK↑	4.5		
		1RDEN before 1RDCLK↑ and 2RDEN before 2RDCLK↑	4		
		1$\overline{\text{RESET}}$ low before 1WRTCLK↑ and 2$\overline{\text{RESET}}$ low before 2WRTCLK↑†	6		
		1$\overline{\text{RESET}}$ low before 1RDCLK↑ and 2$\overline{\text{RESET}}$ low before 2RDCLK↑†	6		
t_h	Hold time	1D after 1WRTCLK↑ and 2D after 2WRTCLK↑	0		ns
		1WRTEN after 1WRTCLK↑ and 2WRTEN after 2WRTCLK↑	0		
		1RDEN after 1RDCLK↑ and 2RDEN after 2RDCLK↑	0		
		1$\overline{\text{RESET}}$ low after 1WRTCLK↑ and 2$\overline{\text{RESET}}$ low after 2WRTCLK↑†	6		
		1$\overline{\text{RESET}}$ low after 1RDCLK↑ and 2$\overline{\text{RESET}}$ low after 2RDCLK↑†	6		

† Requirement to count the clock edge as one of at least four needed to reset a FIFO

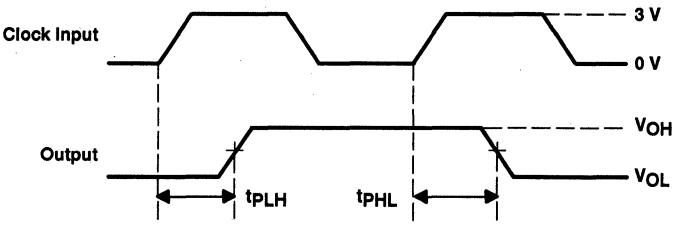
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}	1WRTCLK, 2WRTCLK, or 1RDCLK, 2RDCLK		60		MHz
t_{pd}	1RDCLK↑, 2RDCLK↑	1Q, 2Q	2	9	ns
t_{pd}	1WRTCLK↑, 2WRTCLK↑	1IR, 2IR	1	8	ns
t_{pd}	1RDCLK↑, 2RDCLK↑	1OR, 2OR	1	8	ns
t_{pd}	1WRTCLK↑, 2WRTCLK↑	1AF/AE, 2AF/AE	3	14	ns
	1RDCLK↑, 2RDCLK↑		3	14	
t_{PLH}	1WRTCLK↑, 2WRTCLK↑	1HF, 2HF	2	12	ns
t_{PHL}	1RDCLK↑, 2RDCLK↑		3	14	
t_{PLH}	1$\overline{\text{RESET}}$, 2$\overline{\text{RESET}}$ low	1AF/AE, 2AF/AE	1	17	ns
t_{PHL}		1HF, 2HF	1	18	
t_{en}	1OE, 2OE	1Q, 2Q	0	8	ns
t_{dis}			0	8	

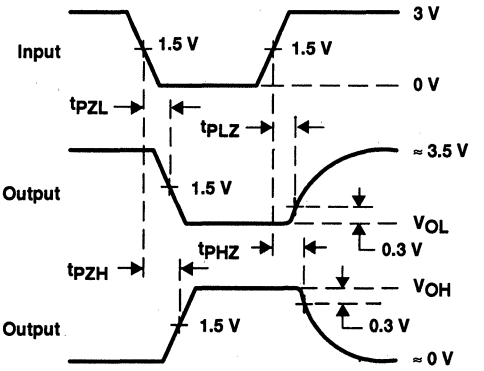
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test-fixture capacitance

Figure 4. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

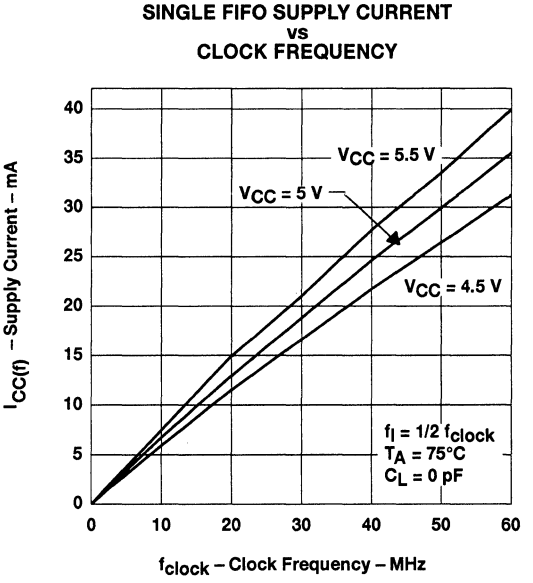


Figure 5

calculating power dissipation

Data for Figure 5 is taken with one FIFO active and one FIFO idle on the device. The active FIFO has both writes and reads enabled with its read clock (RDCLK) and write clock (WRTCLK) operating at the rate specified by f_{clock}. The data input rate and data output rate are half the f_{clock} rate, and the data output is disconnected. A close approximation to the total device power can be found by Figure 5, determining the capacitive load on the data output, and determining the number of SN74ACT2227/2229 inputs driven by TTL high levels.

With $I_{CC(f)}$ taken from Figure 5, the maximum power dissipation (P_T) of one FIFO on the SN74ACT2227 or SN74ACT2229 can be calculated by:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + (C_L \times V_{CC}^2 \times f_o)$$

where:

N	=	number of inputs driven by TTL levels
ΔI_{CC}	=	increase in power supply current for each input at a TTL high level
dc	=	duty cycle of inputs at a TTL high level of 3.4 V
C_L	=	output capacitive load
f_o	=	switching frequency of an output

APPLICATION INFORMATION

An example of concentrating two independent serial data signals into a single composite data signal with the use of an SN74ACT2227 or SN74ACT2229 device is shown in Figure 6. The input data to the FIFOs share the same average (mean) frequency, and the mean frequency of the SYS_CLOCK is greater than or equal to the sum of the individual mean input rates. A single-bit FIFO is needed for each additional input data signal that is time-division multiplexed into the composite signal.

The FIFO memories provide a buffer to absorb clock jitter generated by the transmission systems of incoming signals and synchronize the phase-independent inputs to one another. FIFO half-full (HF) flags are used to signal the multiplexer to start fetching data from the buffers. The state of the flags can also be used to indicate when a FIFO read should be suppressed to regulate the output flow (pulse-stuffing control). The FIFO almost-full/almost-empty flags (AF/AE) can be used in place of the half-full flags to reduce transmission delay.

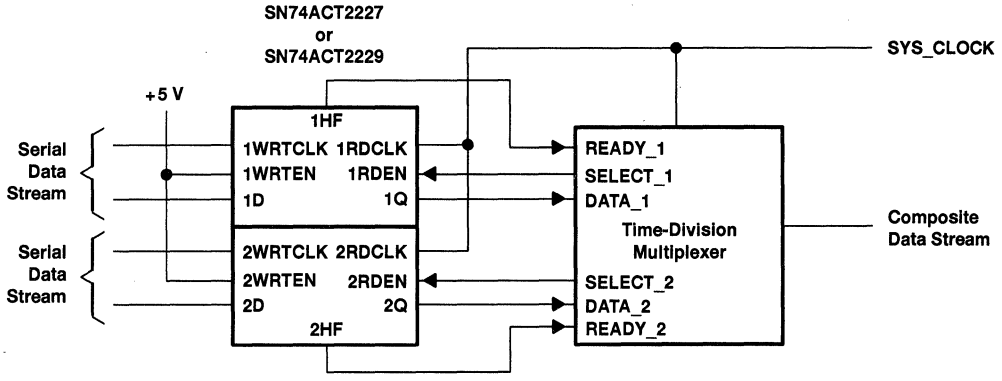
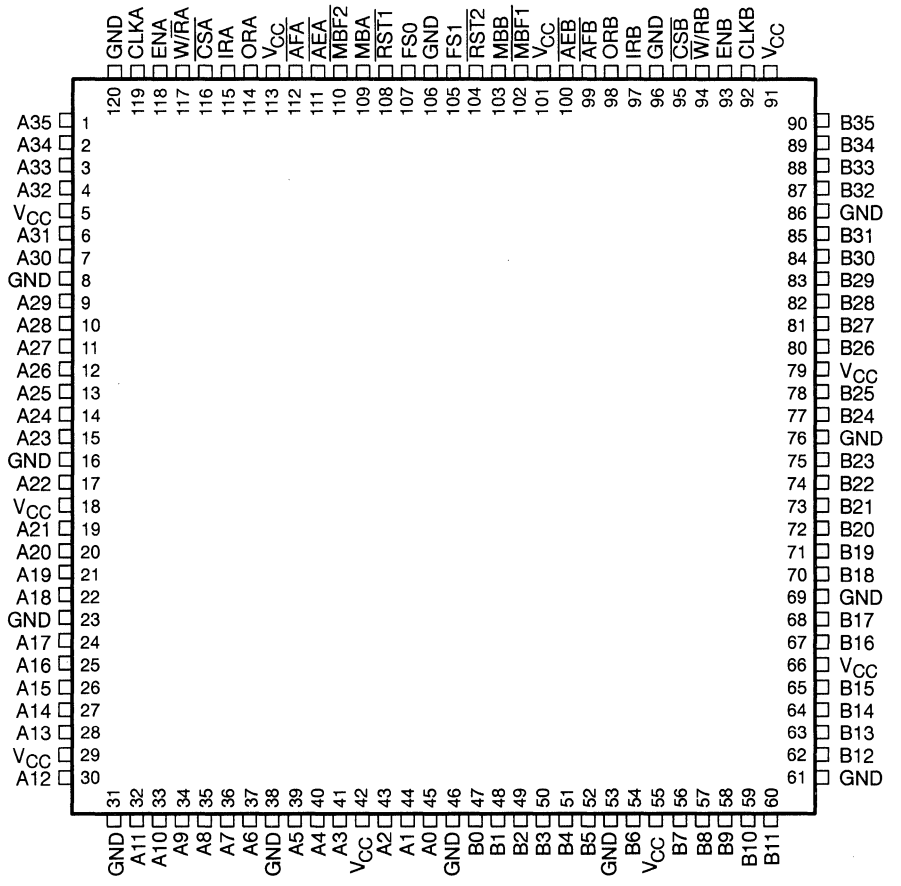


Figure 6. Time-Division Multiplexing Using the SN74ACT2227 or SN74ACT2229

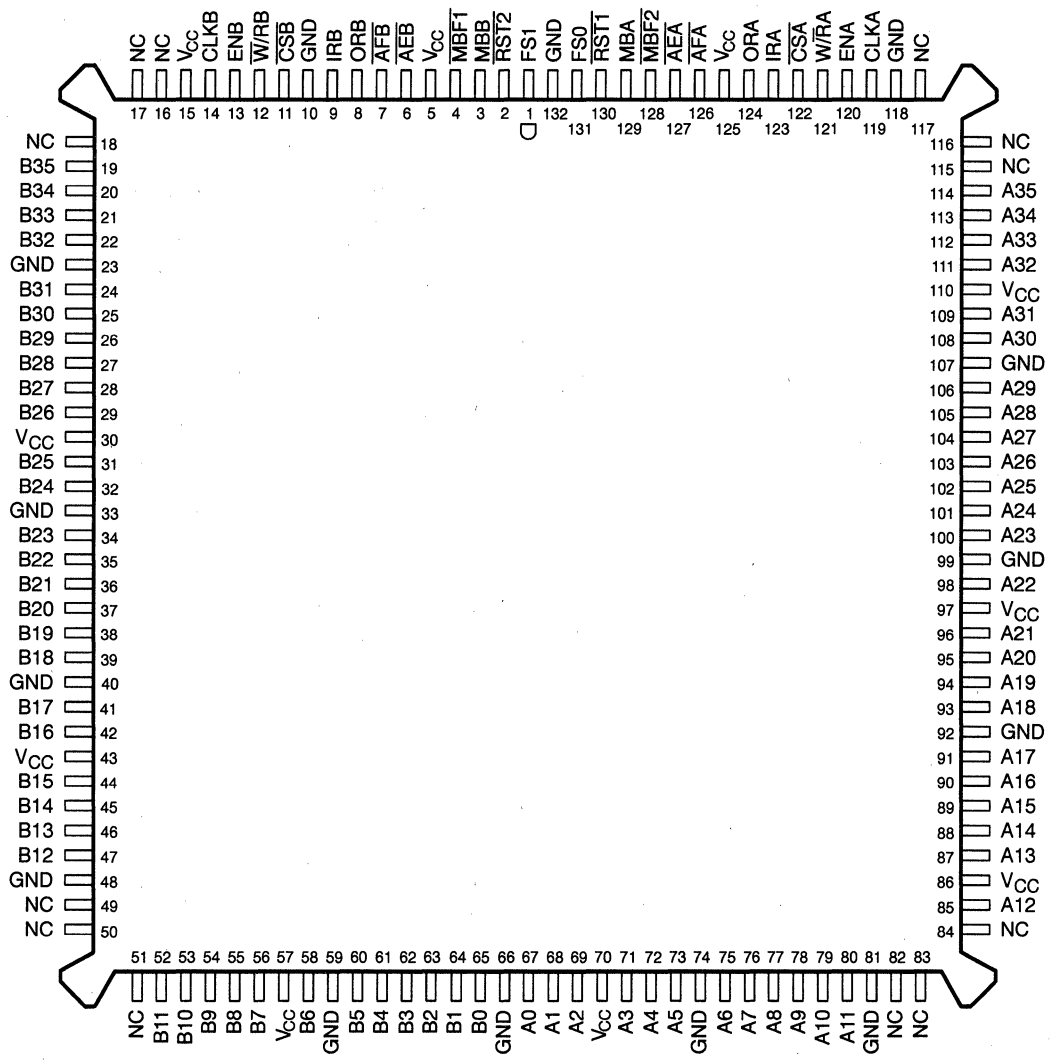
SCAS224B – JUNE 1992 – REVISED SEPTEMBER 1994

- Free-Running CLKA and CLKB Can Be Asynchronous or Coincident
- Two Independent 512 × 36 Clocked FIFOs Buffering Data in Opposite Directions
- Mailbox Bypass Register for Each FIFO
- Programmable Almost-Full and Almost-Empty Flags
- Microprocessor Interface Control Logic
- IRA, ORA, $\overline{AEA}$, and $\overline{AFA}$ Flags Synchronized by CLKA
- IRB, ORB, $\overline{AEB}$, and $\overline{AFB}$ Flags Synchronized by CLKB
- Low-Power 0.8-Micron Advanced CMOS Technology
- Supports Clock Frequencies up to 67 MHz
- Fast Access Times of 11 ns
- Pin-to-Pin Compatible With the SN74ACT3622 and SN74ACT3642
- Available in Space-Saving 120-Pin Thin Quad Flat Package (PCB) or 132-Pin Plastic Quad Flat Package (PQ)

PCB PACKAGE
(TOP VIEW)



PQ PACKAGE†
(TOP VIEW)



NC – No internal connection
† Uses Yamaichi socket IC51-1324-828

description

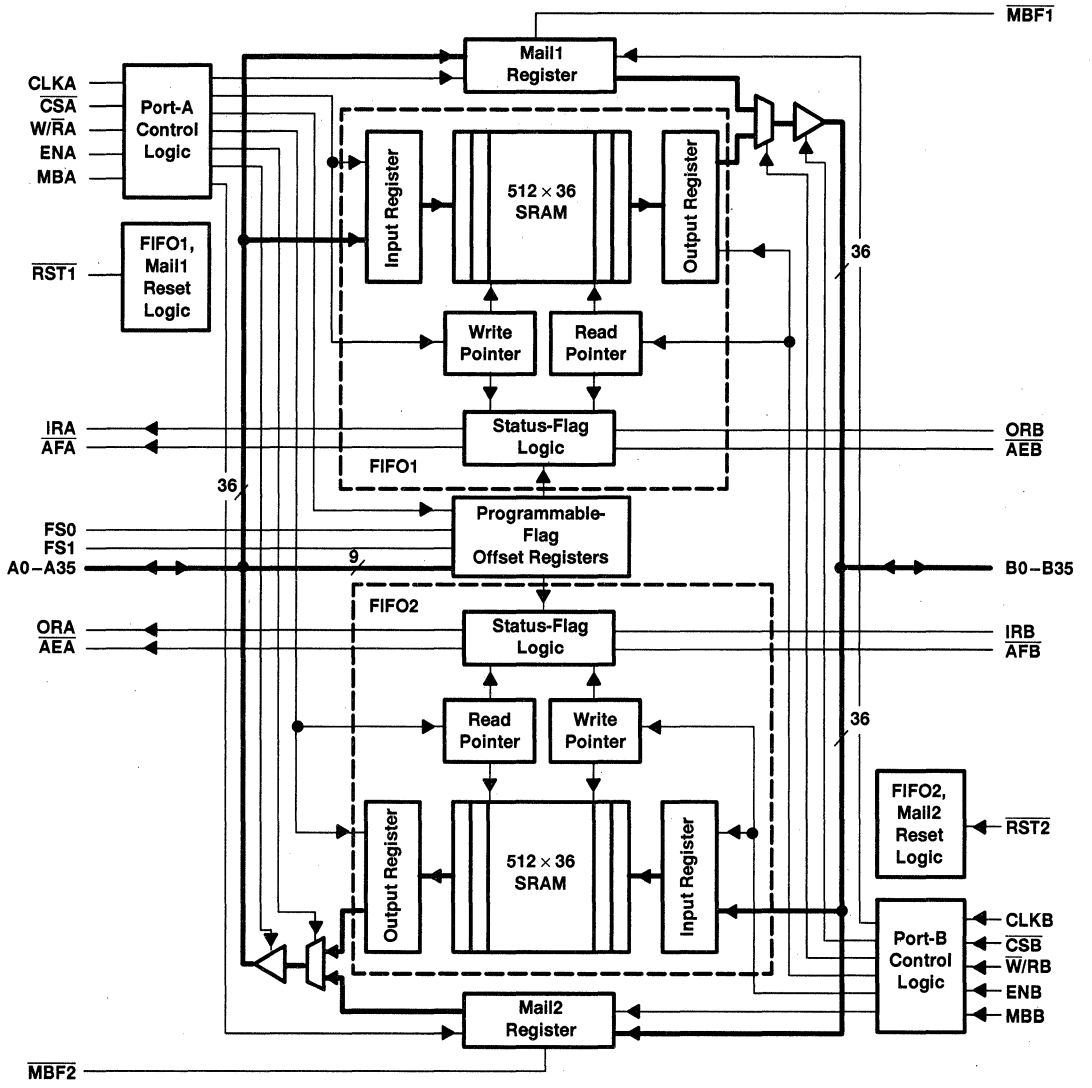
The SN74ACT3632 is a high-speed, low-power CMOS bidirectional clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 11 ns. Two independent 512 × 36 dual-port SRAM FIFOs on board the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words are stored in memory. Communication between each port can bypass the FIFOs via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Two or more devices can be used in parallel to create wider data paths.

The SN74ACT3632 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The input-ready (IRA, IRB) flag and almost-full ($\overline{AFA}$, $\overline{AFB}$) flag of a FIFO are two-stage synchronized to the port clock that writes data to its array. The output-ready (ORA, ORB) flag and almost-empty ($\overline{AEA}$, $\overline{AEB}$) flag of a FIFO are two-stage synchronized to the port clock that reads data from its array. Offset values for the almost-full and almost-empty flags of both FIFOs can be programmed from port A.

The SN74ACT3632 is characterized for operation from 0°C to 70°C.

functional block diagram



Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
A0–A35	I/O	Port-A data. The 36-bit bidirectional data port for side A.
$\overline{AEA}$	O (port A)	Port-A almost-empty flag. Programmable almost-empty flag synchronized to CLKA. $\overline{AEA}$ is low when the number of words in FIFO2 is less than or equal to the value in the almost-empty A offset register, X2.
$\overline{AEB}$	O (port B)	Port-B almost-empty flag. Programmable almost-empty flag synchronized to CLKB. $\overline{AEB}$ is low when the number of words in FIFO1 is less than or equal to the value in the almost-empty B offset register, X1.
$\overline{AFA}$	O (port A)	Port-A almost-full flag. Programmable almost-full flag synchronized to CLKA. $\overline{AFA}$ is low when the number of empty locations in FIFO1 is less than or equal to the value in the almost-full A offset register, Y1.
$\overline{AFB}$	O (port B)	Port-B almost-full flag. Programmable almost-full flag synchronized to CLKB. $\overline{AFB}$ is low when the number of empty locations in FIFO2 is less than or equal to the value in the almost-full B offset register, Y2.
B0–B35	I/O	Port-B data. The 36-bit bidirectional data port for side B.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. IRA, ORA, $\overline{AFA}$, and $\overline{AEA}$ are all synchronized to the low-to-high transition of CLKA.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. IRB, ORB, $\overline{AFB}$, and $\overline{AEB}$ are synchronized to the low-to-high transition of CLKB.
$\overline{CSA}$	I	Port-A chip select. $\overline{CSA}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{CSA}$ is high.
$\overline{CSB}$	I	Port-B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{CSB}$ is high.
ENA	I	Port-A enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port-B enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
FS1, FS0	I	Flag offset selects. The low-to-high transition of a FIFO reset input latches the values of FS0 and FS1. If either FS0 or FS1 is high when a reset input goes high, one of three preset values is selected as the offset for the FIFO almost-full and almost-empty flags. If both FIFOs are reset simultaneously and both FS0 and FS1 are low when $\overline{RST1}$ and $\overline{RST2}$ go high, the first four writes to FIFO1 program the almost-full and almost-empty offsets for both FIFOs.
IRA	O (port A)	Input-ready flag. IRA is synchronized to the low-to-high transition of CLKA. When IRA is low, FIFO1 is full and writes to its array are disabled. IRA is set low when FIFO1 is reset and is set high on the second low-to-high transition of CLKA after reset.
IRB	O (port B)	Input-ready flag. IRB is synchronized to the low-to-high transition of CLKB. When IRB is low, FIFO2 is full and writes to its array are disabled. IRB is set low when FIFO2 is reset and is set high on the second low-to-high transition of CLKB after reset.
MBA	I	Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation. When the A0–A35 outputs are active, a high level on MBA selects data from the mail2 register for output and a low level selects FIFO2 output-register data for output.
MBB	I	Port-B mailbox select. A high level on MBB chooses a mailbox register for a port-B read or write operation. When the B0–B35 outputs are active, a high level on MBB selects data from the mail1 register for output and a low level selects FIFO1 output-register data for output.
$\overline{MBF1}$	O	Mail1 register flag. $\overline{MBF1}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is low. $\overline{MBF1}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and MBB is high. $\overline{MBF1}$ is set high when FIFO1 is reset.
$\overline{MBF2}$	O	Mail2 register flag. $\overline{MBF2}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is low. $\overline{MBF2}$ is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. $\overline{MBF2}$ is also set high when FIFO2 is reset.
ORA	O (port A)	Output-ready flag. ORA is synchronized to the low-to-high transition of CLKA. When ORA is low, FIFO2 is empty and reads from its memory are disabled. Ready data is present on the output register of FIFO2 when ORA is high. ORA is forced low when FIFO2 is reset and goes high on the third low-to-high transition of CLKA after a word is loaded to empty memory.

Terminal Functions (Continued)

TERMINAL NAME	I/O	DESCRIPTION
ORB	O (port B)	Output-ready flag. ORB is synchronized to the low-to-high transition of CLKB. When ORB is low, FIFO1 is empty and reads from its memory are disabled. Ready data is present on the output register of FIFO1 when ORB is high. ORB is forced low when FIFO1 is reset and goes high on the third low-to-high transition of CLKB after a word is loaded to empty memory.
$\overline{RST1}$	I	FIFO1 reset. To reset FIFO1, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RST1}$ is low. The low-to-high transition of $\overline{RST1}$ latches the status of FS0 and FS1 for $\overline{AFA}$ and $\overline{AEB}$ offset selection. FIFO1 must be reset upon power up before data is written to its RAM.
$\overline{RST2}$	I	FIFO2 reset. To reset FIFO2, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RST2}$ is low. The low-to-high transition of $\overline{RST2}$ latches the status of FS0 and FS1 for $\overline{AFB}$ and $\overline{AEA}$ offset selection. FIFO2 must be reset upon power up before data is written to its RAM.
W/$\overline{RA}$	I	Port-A write/read select. A high on W/$\overline{RA}$ selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{RA}$ is high.
$\overline{W}$/RB	I	Port-B write/read select. A low on $\overline{W}$/RB selects a write operation and a high selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when $\overline{W}$/RB is low.

detailed description

reset

The FIFO memories of the SN74ACT3632 are reset separately by taking their reset ($\overline{RST1}$, $\overline{RST2}$) inputs low for at least four port-A clock (CLKA) and four port-B clock (CLKB) low-to-high transitions. The reset inputs can switch asynchronously to the clocks. A FIFO reset initializes the internal read and write pointers and forces the input-ready flag (IRA, IRB) low, the output-ready flag (ORA, ORB) low, the almost-empty flag ($\overline{AEA}$, $\overline{AEB}$) low, and the almost-full flag ($\overline{AFA}$, $\overline{AFB}$) high. Resetting a FIFO also forces the mailbox flag ($\overline{MBF1}$, $\overline{MBF2}$) of the parallel mailbox register high. After a FIFO is reset, its input-ready flag is set high after two clock cycles to begin normal operation. A FIFO must be reset after power up before data is written to its memory.

A low-to-high transition on a FIFO reset ($\overline{RST1}$, $\overline{RST2}$) input latches the value of the flag-select (FS0, FS1) inputs for choosing the almost-full and almost-empty offset programming method.

almost-empty flag and almost-full flag offset programming

Four registers in the SN74ACT3632 are used to hold the offset values for the almost-empty and almost-full flags. The port-B almost-empty flag ($\overline{AEB}$) offset register is labeled X1 and the port-A almost-empty flag ($\overline{AEA}$) offset register is labeled X2. The port-A almost-full flag ($\overline{AFA}$) offset register is labeled Y1 and the port-B almost-full flag ($\overline{AFB}$) offset register is labeled Y2. The index of each register name corresponds to its FIFO number. The offset registers can be loaded with preset values during the reset of a FIFO or they can be programmed from port A (see Table 1).

Table 1. Flag Programming

FS1	FS0	$\overline{RST1}$	$\overline{RST2}$	X1 AND Y1 REGISTERS†	X2 AND Y2 REGISTERS‡
H	H	↑	X	64	X
H	H	X	↑	X	64
H	L	↑	X	16	X
H	L	X	↑	X	16
L	H	↑	X	8	X
L	H	X	↑	X	8
L	L	↑	↑	Programmed from port A	Programmed from port A

† X1 register holds the offset for $\overline{AEB}$; Y1 register holds the offset for $\overline{AFA}$.
‡ X2 register holds the offset for $\overline{AEA}$; Y2 register holds the offset for $\overline{AFB}$.

almost-empty flag and almost-full flag offset programming (continued)

To load the almost-empty flag and almost-full flag offset registers of a FIFO with one of the three preset values listed in Table 1, at least one of the flag-select inputs must be high during the low-to-high transition of its reset input. For example, to load the preset value of 64 into X1 and Y1, FS0 and FS1 must be high when FIFO1 reset ($\overline{RST1}$) returns high. Flag-offset registers associated with FIFO2 are loaded with one of the preset values in the same way with FIFO2 reset ($\overline{RST2}$). When using one of the preset values for the flag offsets, the FIFOs can be reset simultaneously or at different times.

To program the X1, X2, Y1, and Y2 registers from port A, both FIFOs should be reset simultaneously with FS0 and FS1 low during the low-to-high transition of the reset inputs. After this reset is complete, the first four writes to FIFO1 do not store data in RAM but load the offset registers in the order Y1, X1, Y2, X2. Each offset register uses port-A (A8–A0) inputs, with A8 as the most significant bit. Each register value can be programmed from 1 to 508. After all the offset registers are programmed from port A, the port-B input-ready flag (IRB) is set high and both FIFOs begin normal operation.

FIFO write/read operation

The state of the port-A data (A0–A35) outputs is controlled by the port-A chip select ($\overline{CSA}$) and the port-A write/read select (W/$\overline{RA}$). The A0–A35 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is high. The A0–A35 outputs are active when both $\overline{CSA}$ and W/$\overline{RA}$ are low.

Data is loaded into FIFO1 from the A0–A35 inputs on a low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is high, ENA is high, MBA is low, and IRA is high. Data is read from FIFO2 to the A0–A35 outputs by a low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is low, ENA is high, MBA is low, and ORA is high (see Table 2). FIFO reads and writes on port A are independent of any concurrent port-B operation.

Table 2. Port-A Enable Function Table

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	A0–A35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO1 write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, FIFO2 output register	None
L	L	H	L	↑	Active, FIFO2 output register	FIFO2 read
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set $\overline{MBF2}$ high)

The port-B control signals are identical to those of port A with the exception that the port-B write/read select ($\overline{W}$/RB) is the inverse of the port-A write/read select (W/$\overline{RA}$). The state of the port-B data (B0–B35) outputs is controlled by the port-B chip select ($\overline{CSB}$) and the port-B write/read select ($\overline{W}$/RB). The B0–B35 outputs are in the high-impedance state when either $\overline{CSB}$ is high or $\overline{W}$/RB is low. The B0–B35 outputs are active when $\overline{CSB}$ is low and $\overline{W}$/RB is high.

Data is loaded into FIFO2 from the B0–B35 inputs on a low-to-high transition of CLKB when $\overline{CSB}$ is low, $\overline{W}$/RB is low, ENB is high, MBB is low, and IRB is high. Data is read from FIFO1 to the B0–B35 outputs by a low-to-high transition of CLKB when $\overline{CSB}$ is low, $\overline{W}$/RB is high, ENB is high, MBB is low, and ORB is high (see Table 3). FIFO reads and writes on port B are independent of any concurrent port-A operation.

FIFO write/read operation (continued)

Table 3. Port-B Enable Function Table

$\overline{CSB}$	W/$\overline{RB}$	ENB	MBB	CLKB	B0–B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	L	L	X	X	In high-impedance state	None
L	L	H	L	↑	In high-impedance state	FIFO2 write
L	L	H	H	↑	In high-impedance state	Mail2 write
L	H	L	L	X	Active, FIFO1 output register	None
L	H	H	L	↑	Active, FIFO1 output register	FIFO1 read
L	H	L	H	X	Active, mail1 register	None
L	H	H	H	↑	Active, mail1 register	Mail1 read (set $\overline{MBF1}$ high)

The setup and hold time constraints to the port clocks for the port chip selects and write/read selects are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is low during a clock cycle, the port's chip select and write/read select may change states during the setup and hold time window of the cycle.

When a FIFO output-ready flag is low, the next data word is sent to the FIFO output register automatically by the low-to-high transition of the port clock that sets the output-ready flag high. When the output-ready flag is high, an available data word is clocked to the FIFO output register only when a FIFO read is selected by the port's chip select, write/read select, enable, and mailbox select.

synchronized FIFO flags

Each FIFO is synchronized to its port clock through at least two flip-flop stages. This is done to improve flag-signal reliability by reducing the probability of metastable events when CLKA and CLKB operate asynchronously to one another (see the application report *Metastability Performance of Clocked FIFOs* in the 1994 *High-Performance FIFO Memories Data Book*, literature #SCAD003B). ORA, $\overline{AEA}$, IRA, and $\overline{AFA}$ are synchronized to CLKA. ORB, $\overline{AEB}$, IRB, and $\overline{AFB}$ are synchronized to CLKB. Tables 4 and 5 show the relationship of each port flag to FIFO1 and FIFO2.

Table 4. FIFO1 Flag Operation

NUMBER OF WORDS IN FIFO1†‡	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA	
	ORB	$\overline{AEB}$	$\overline{AFA}$	IRA
0	L	L	H	H
1 to X1	H	L	H	H
(X1 + 1) to [512 – (Y1 + 1)]	H	H	H	H
(512 – Y1) to 511	H	H	L	H
512	H	H	L	L

† X1 is the almost-empty offset for FIFO1 used by $\overline{AEB}$. Y1 is the almost-full offset for FIFO1 used by $\overline{AFA}$. Both X1 and Y1 are selected during a reset of FIFO1 or programmed from port A.

‡ When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.

synchronized FIFO flags (continued)

Table 5. FIFO2 Flag Operation

NUMBER OF WORDS IN FIFO2†‡	SYNCHRONIZED TO CLKA		SYNCHRONIZED TO CLKB	
	ORA	$\overline{AEA}$	$\overline{AFB}$	IRB
0	L	L	H	H
1 to X2	H	L	H	H
(X2 + 1) to [512 – (Y2 + 1)]	H	H	H	H
(512 – Y2) to 511	H	H	L	H
512	H	H	L	L

† X2 is the almost-empty offset for FIFO2 used by $\overline{AEA}$. Y2 is the almost-full offset for FIFO2 used by $\overline{AFB}$. Both X2 and Y2 are selected during a reset of FIFO2 or programmed from port A.

‡ When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.

output-ready flags (ORA, ORB)

The output-ready flag of a FIFO is synchronized to the port clock that reads data from its array. When the output-ready flag is high, new data is present in the FIFO output register. When the output-ready flag is low, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

A FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an output-ready flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. From the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of the output-ready flag synchronizing clock; therefore, an output-ready flag is low if a word in memory is the next data to be sent to the FIFO output register and three cycles of the port clock that reads data from the FIFO have not elapsed since the time the word was written. The output-ready flag of the FIFO remains low until the third low-to-high transition of the synchronizing clock occurs, simultaneously forcing the output-ready flag high and shifting the word to the FIFO output register.

A low-to-high transition on an output-ready flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{sk1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 7 and 8).

input-ready flags (IRA, IRB)

The input-ready flag of a FIFO is synchronized to the port clock that writes data to its array. When the input-ready flag is high, a memory location is free in the SRAM to receive new data. No memory locations are free when the input-ready flag is low and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, its write pointer is incremented. The state machine that controls an input-ready flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is full, full–1, or full–2. From the time a word is read from a FIFO, its previous memory location is ready to be written in a minimum of two cycles of the input-ready flag synchronizing clock; therefore, an input-ready flag is low if less than two cycles of the input-ready flag synchronizing clock have elapsed since the next memory write location has been read. The second low-to-high transition on the input-ready flag synchronizing clock after the read sets the input-ready flag high.

A low-to-high transition on an input-ready flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{sk1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 9 and 10).

almost-empty flags ($\overline{AEA}$, $\overline{AEB}$)

The almost-empty flag of a FIFO is synchronized to the port clock that reads data from its array. The state machine that controls an almost-empty flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the contents of register X1 for $\overline{AEB}$ and register X2 for $\overline{AEA}$. These registers are loaded with preset values during a FIFO reset or programmed from port A (see *almost-empty flag and almost-full flag offset programming*). An almost-empty flag is low when its FIFO contains X or less words and is high when its FIFO contains (X + 1) or more words. A data word present in the FIFO output register has been read from memory.

Two low-to-high transitions of the almost-empty flag synchronizing clock are required after a FIFO write for its almost-empty flag to reflect the new level of fill. Therefore, the almost-empty flag of a FIFO containing (X + 1) or more words remains low if two cycles of its synchronizing clock have not elapsed since the write that filled the memory to the (X + 1) level. An almost-empty flag is set high by the second low-to-high transition of its synchronizing clock after the FIFO write that fills memory to the (X + 1) level. A low-to-high transition of an almost-empty flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the write that fills the FIFO to (X + 1) words. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figures 11 and 12).

almost-full flags ($\overline{AFA}$, $\overline{AFB}$)

The almost-full flag of a FIFO is synchronized to the port clock that writes data to its array. The state machine that controls an almost-full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost full, almost full–1, or almost full–2. The almost-full state is defined by the contents of register Y1 for $\overline{AFA}$ and register Y2 for $\overline{AFB}$. These registers are loaded with preset values during a FIFO reset or programmed from port A (see *almost-empty flag and almost-full flag offset programming*). An almost-full flag is low when its FIFO contains (512 – Y) or more words and is high when its FIFO contains [512 – (Y + 1)] or less words. A data word is present in the FIFO output register has been read from memory.

Two low-to-high transitions of the almost-full flag synchronizing clock are required after a FIFO read for its almost-full flag to reflect the new level of fill. Therefore, the almost-full flag of a FIFO containing [512 – (Y + 1)] or less words remains low if two cycles of its synchronizing clock have not elapsed since the read that reduced the number of words in memory to [512 – (Y + 1)]. An almost-full flag is set high by the second low-to-high transition of its synchronizing clock after the FIFO read that reduces the number of words in memory to [512 – (Y + 1)]. A low-to-high transition of an almost-full flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{sk2} or greater after the read that reduces the number of words in memory to [512 – (Y + 1)]. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figures 13 and 14).

mailbox registers

Each FIFO has a 36-bit bypass register to pass command and control information between port A and port B without putting it in queue. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A low-to-high transition on CLKA writes A0–A35 data to the mail1 register when a port-A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and with MBA high. A low-to-high transition on CLKB writes B0–B35 data to the mail2 register when a port-B write is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB and with MBB high. Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) low. Attempted writes to a mail register are ignored while the mail flag is low.

When data outputs of a port are active, the data on the bus comes from the FIFO output register when the port mailbox select input is low and from the mail register when the port-mailbox select input is high. The mail1 register flag ($\overline{MBF1}$) is set high by a low-to-high transition on CLKB when a port-B read is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB and with MBB high. The mail2 register flag ($\overline{MBF2}$) is set high by a low-to-high transition on CLKA when a port-A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and with MBA high. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

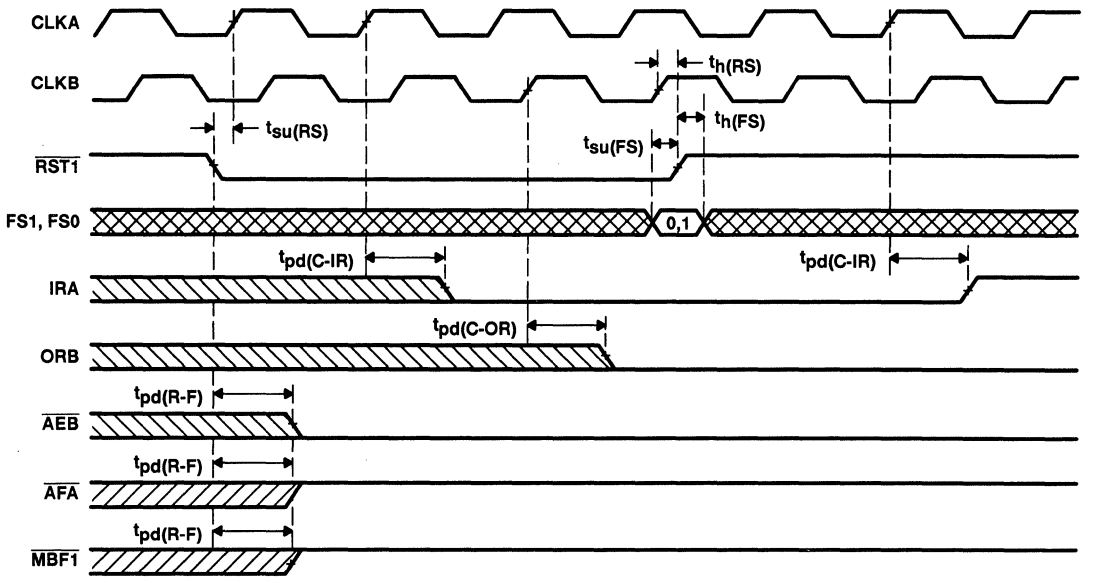
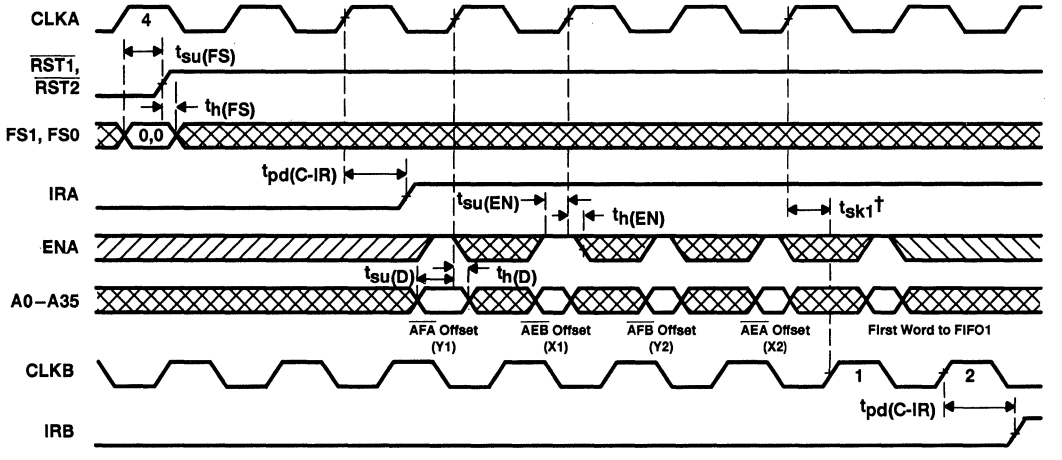


Figure 1. FIFO1 Reset Loading X1 and Y1 With a Preset Value of Eight†

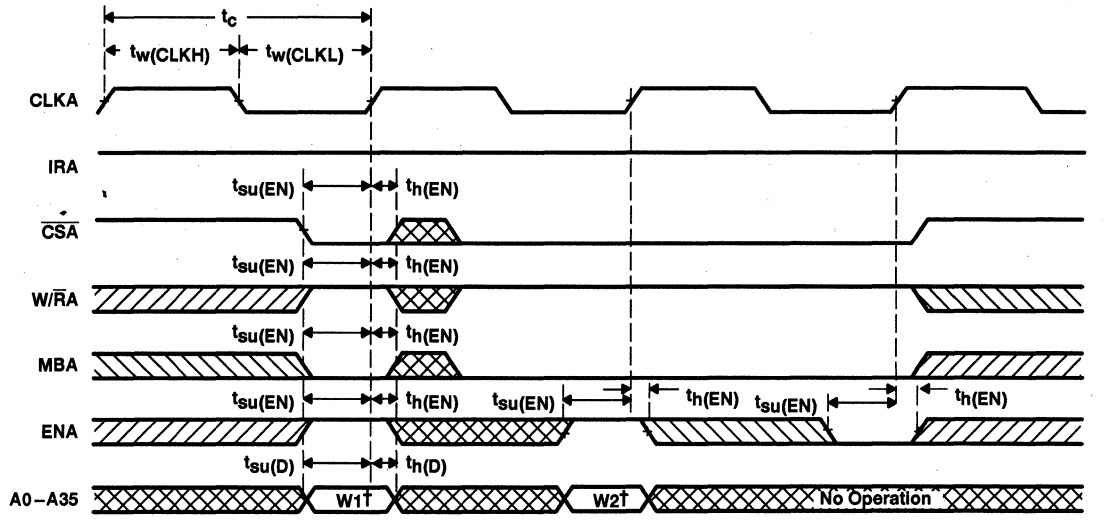
† FIFO2 is reset in the same manner to load X2 and Y2 with a preset value.



† t_{sk1} is the minimum time between the rising CLKA edge and a rising CLKB edge for IRB to transition high in the next cycle. If the time between the rising edge of CLKA and rising edge of CLKB is less than t_{sk1}, IRB may transition high one cycle later than shown.

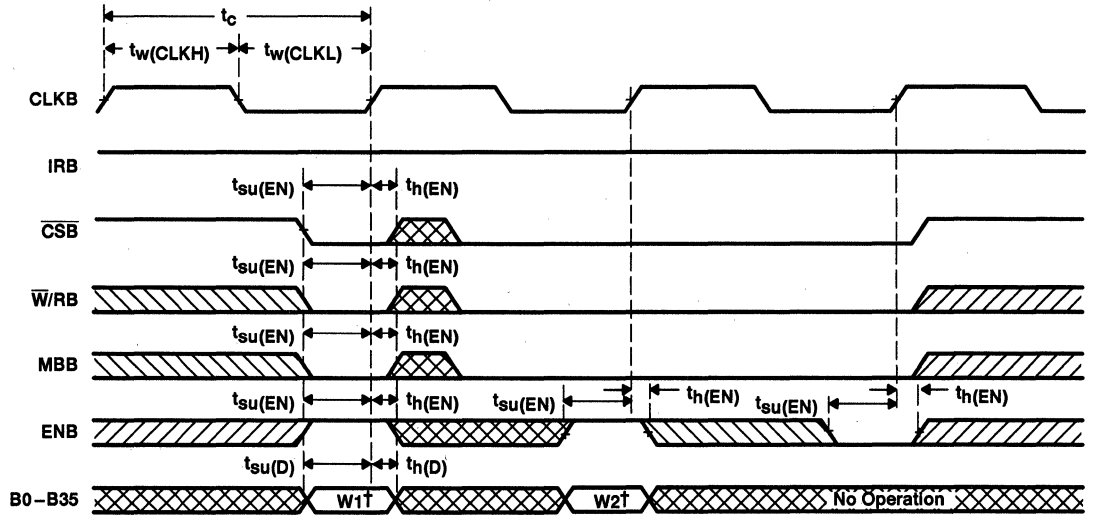
NOTE A: $\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L. It is not necessary to program offset register on consecutive clock cycles.

Figure 2. Programming the Almost-Full Flag and Almost-Empty Flag Offset Values After Reset



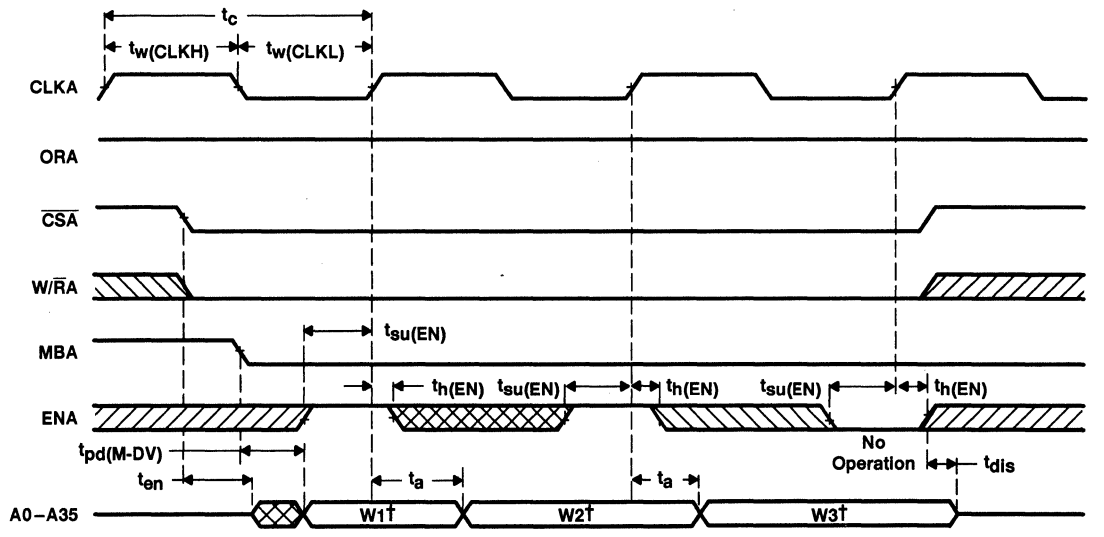
† Written to FIFO1

Figure 3. Port-A Write-Cycle Timing for FIFO1



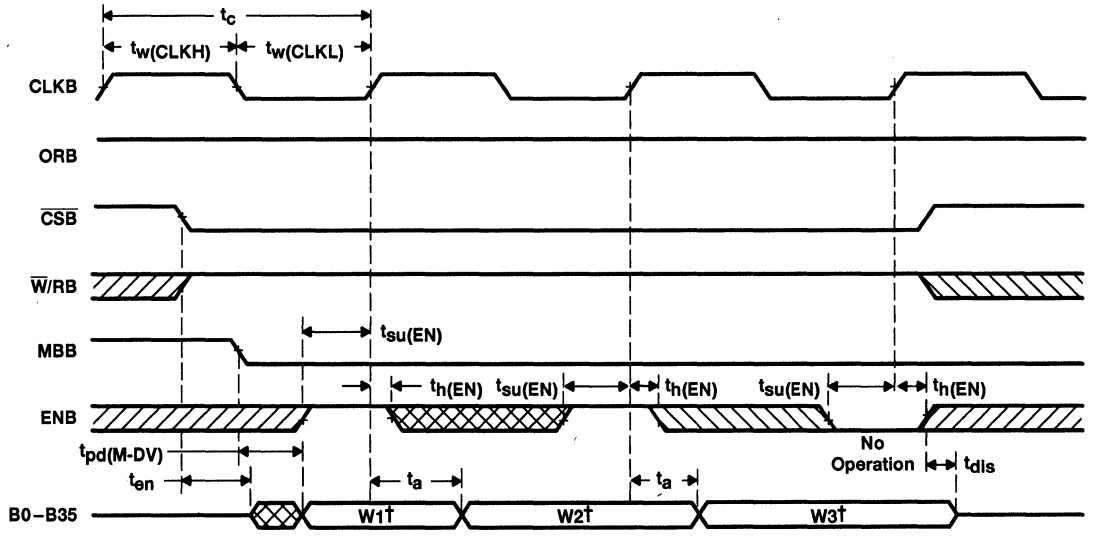
† Written to FIFO2

Figure 4. Port-B Write-Cycle Timing for FIFO2



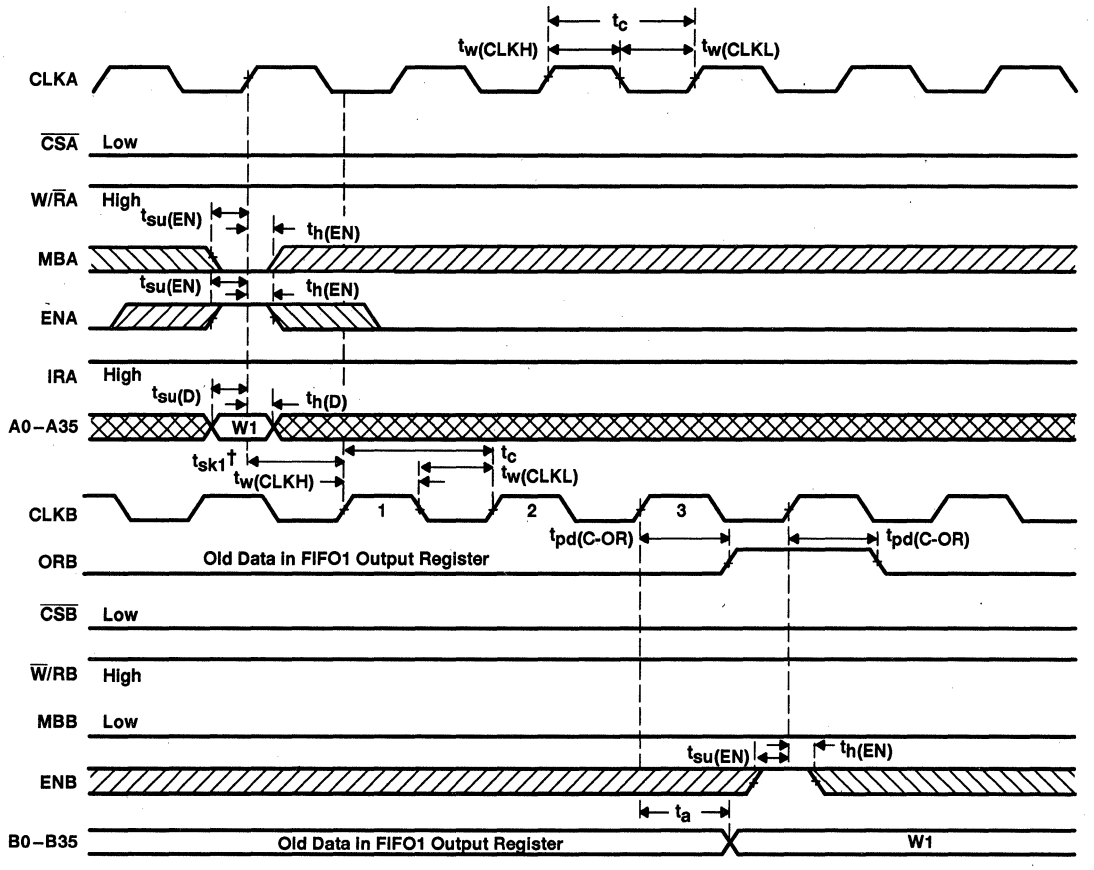
† Read from FIFO2

Figure 5. Port-A Read-Cycle Timing for FIFO2



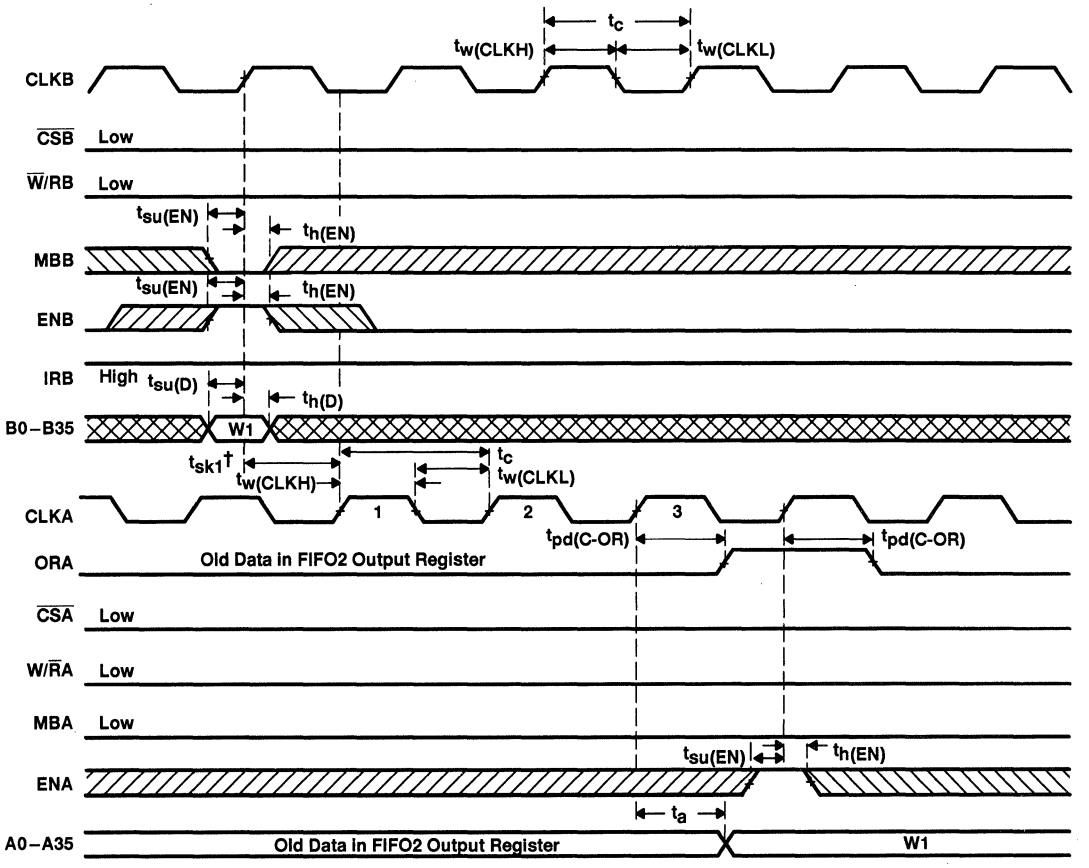
† Read from FIFO1

Figure 6. Port-B Read-Cycle Timing for FIFO1



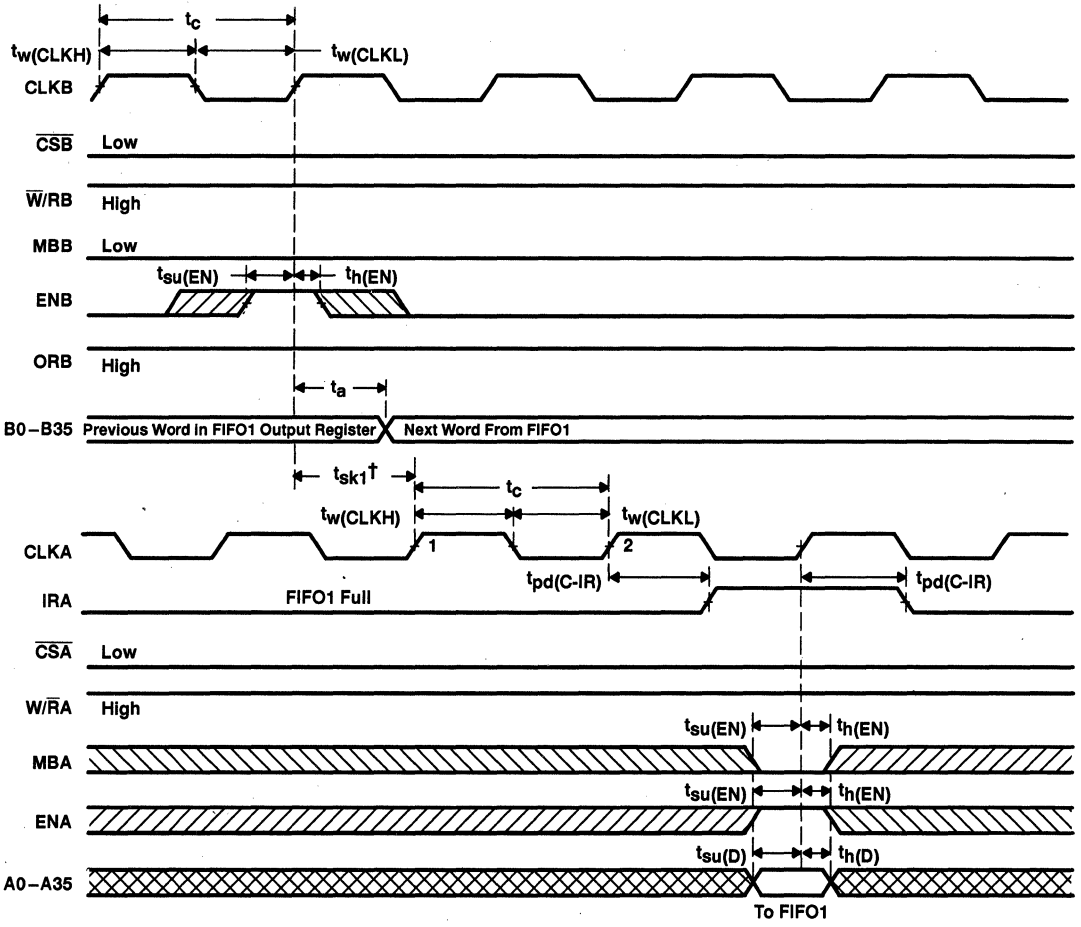
† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for ORB to transition high and to clock the next word to the FIFO1 output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, the transition of ORB high and load of the first word to the output register may occur one CLKB cycle later than shown.

Figure 7. ORB-Flag Timing and First-Data-Word Fallthrough When FIFO1 Is Empty



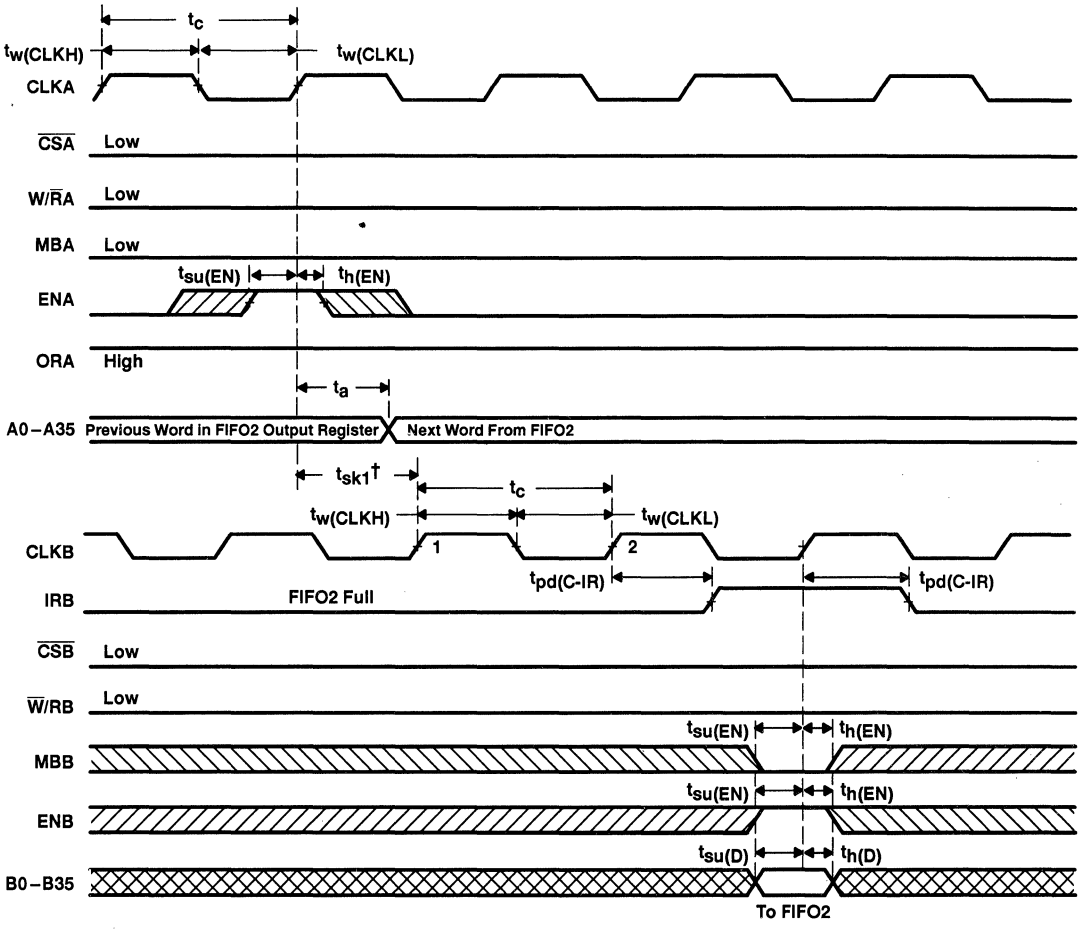
† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for ORA to transition high and to clock the next word to the FIFO2 output register in three CLKA cycles. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, the transition of ORA high and load of the first word to the output register may occur one CLKA cycle later than shown.

Figure 8. ORA-Flag Timing and First-Data-Word Fallthrough When FIFO2 Is Empty



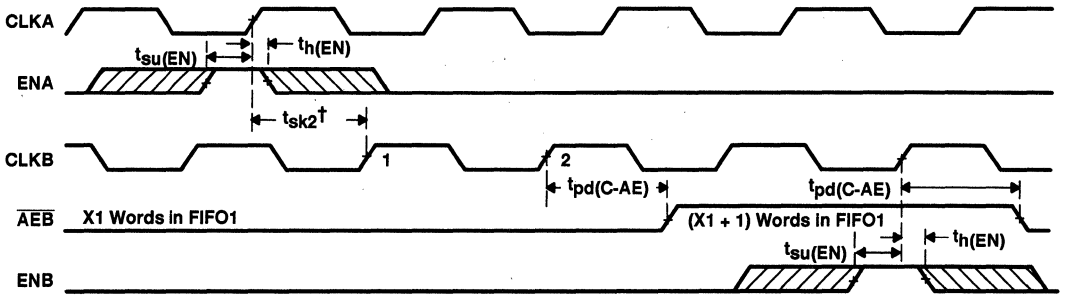
† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for IRA to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, IRA may transition high one CLKA cycle later than shown.

Figure 9. IRA-Flag Timing and First Available Write When FIFO1 Is Full



† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for IRB to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, IRB may transition high one CLKB cycle later than shown.

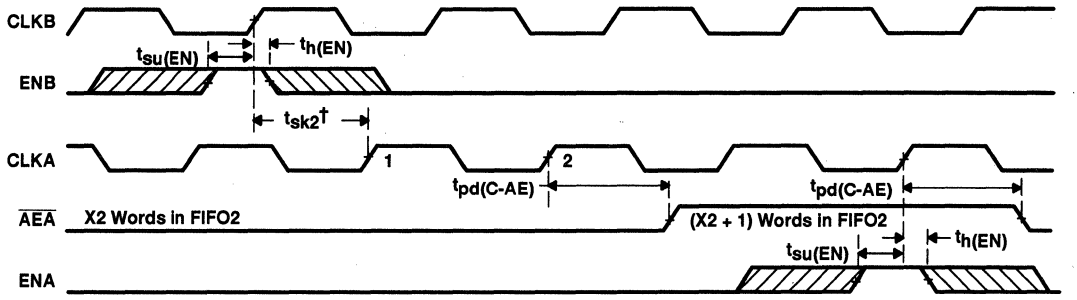
Figure 10. IRB-Flag Timing and First Available Write When FIFO2 Is Full



† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AEB}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, $\overline{AEB}$ may transition high one CLKB cycle later than shown.

NOTE A: FIFO1 write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO1 read ($\overline{CSB}$ = L, W/$\overline{RB}$ = H, MBB = L). Data in the FIFO1 output register has been read from the FIFO.

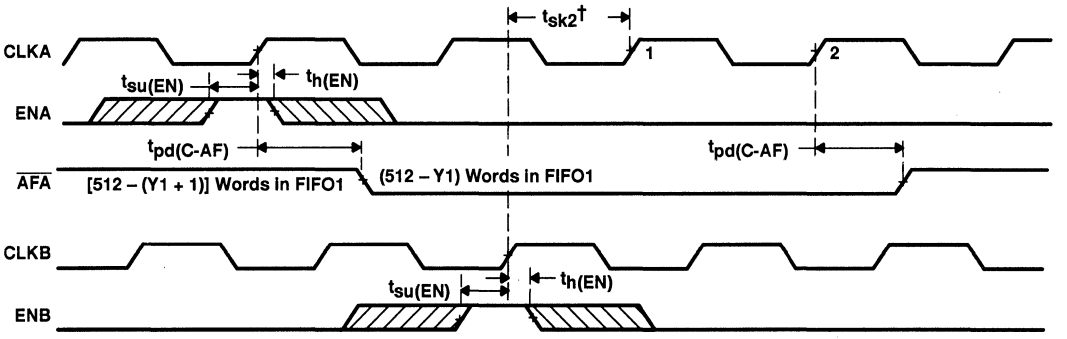
Figure 11. Timing for $\overline{AEB}$ When FIFO1 Is Almost Empty



† t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AEA}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, $\overline{AEA}$ may transition high one CLKA cycle later than shown.

NOTE A: FIFO2 write ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L), FIFO2 read ($\overline{CSA}$ = L, W/$\overline{RA}$ = L, MBA = L). Data in the FIFO2 output register has been read from the FIFO.

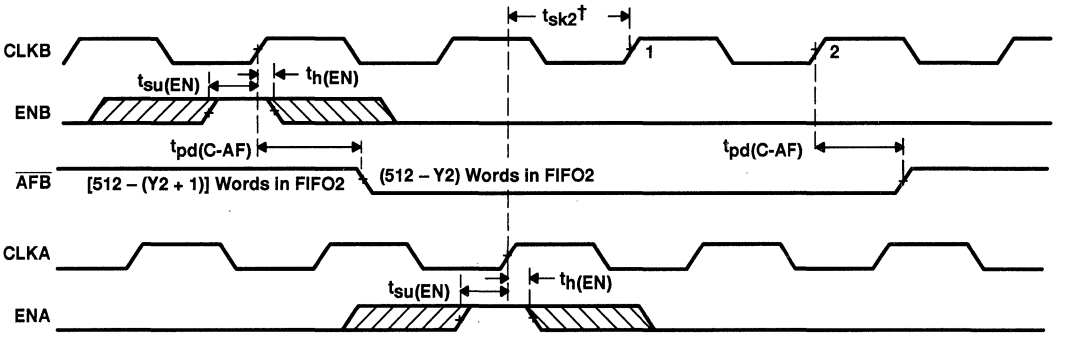
Figure 12. Timing for $\overline{AEA}$ When FIFO2 Is Almost Empty



† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AFA}$ to transition high in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, $\overline{AFA}$ may transition high one CLKB cycle later than shown.

NOTE A: FIFO1 write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO1 read ($\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L). Data in the FIFO1 output register has been read from the FIFO.

Figure 13. Timing for $\overline{AFA}$ When FIFO1 Is Almost Full



† t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AFB}$ to transition high in the next CLKB cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, $\overline{AFB}$ may transition high one CLKA cycle later than shown.

NOTE A: FIFO2 write ($\overline{CSB}$ = L, $\overline{W}$/RB= L, MBB = L), FIFO2 read ($\overline{CSA}$ = L, W/$\overline{RA}$ = L, MBA = L). Data in the FIFO2 output register has been read from the FIFO.

Figure 14. Timing for $\overline{AFB}$ When FIFO2 Is Almost Full

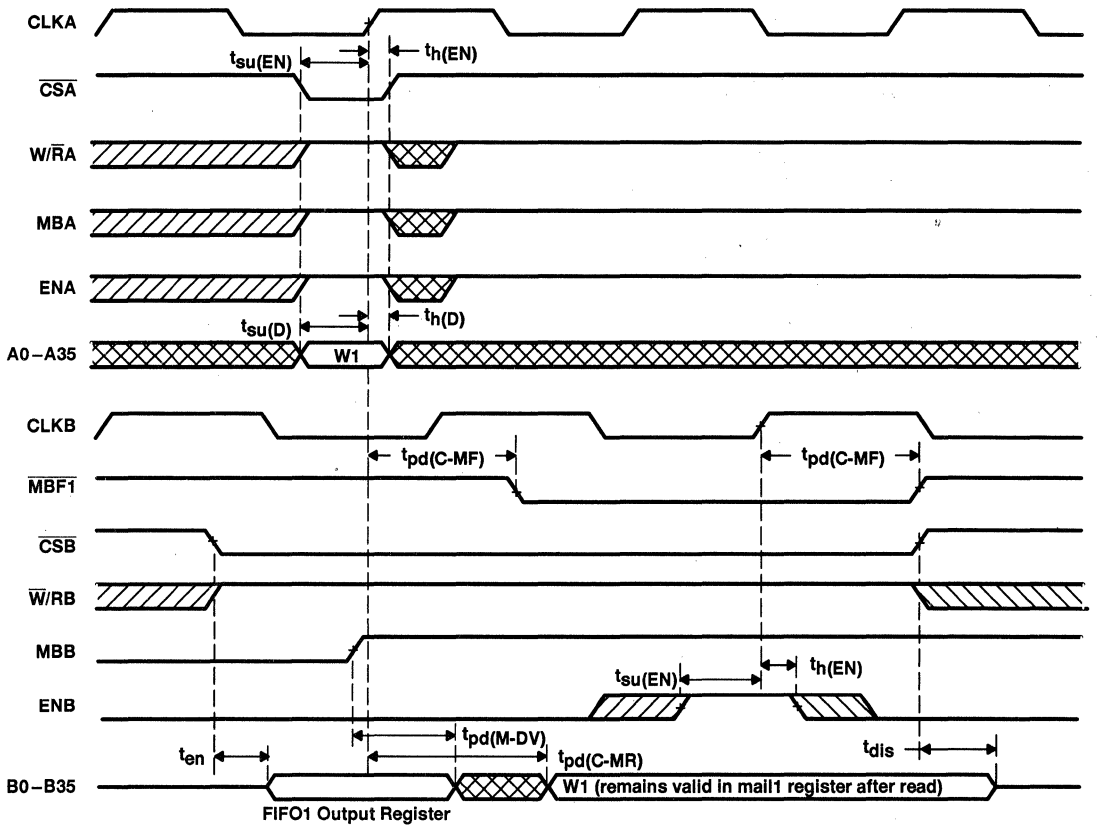


Figure 15. Timing for Mail1 Register and $\overline{\text{MBF1}}$ Flag

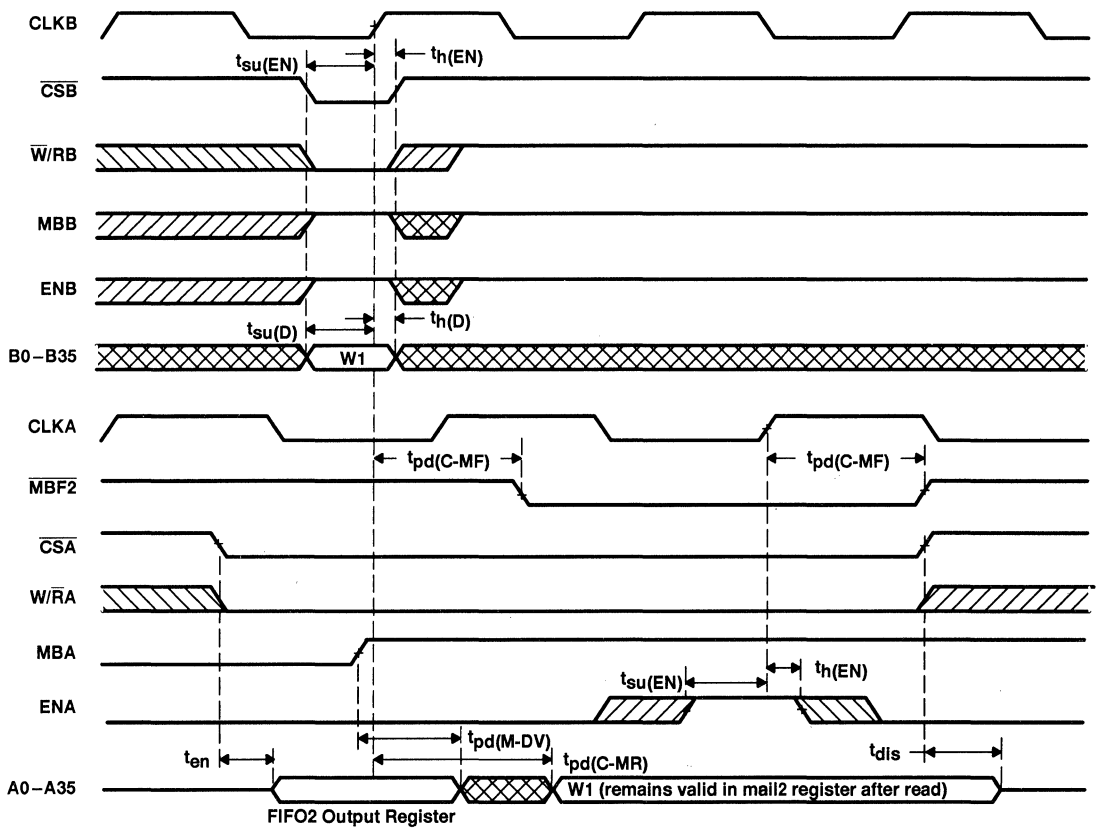


Figure 16. Timing for Mail2 Register and $\overline{MBF2}$ Flag

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−4	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −4 mA			2.4			V
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA					0.5	V
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or 0					±5	μA
I_{OZ}	V_{CC} = 5.5 V, V_O = V_{CC} or 0					±5	μA
I_{CC}	V_{CC} = 5.5 V, V_I = V_{CC} − 0.2 V or 0					400	μA
ΔI_{CC}‡	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	$\overline{CSA}$ = V_{IH}	A0–A35		0		mA
		$\overline{CSB}$ = V_{IH}	B0–B35		0		
		$\overline{CSA}$ = V_{IL}	A0–A35			1	
		$\overline{CSB}$ = V_{IL}	B0–B35			1	
		All other inputs				1	
C_i	V_I = 0, f = 1 MHz				4		pF
C_o	V_O = 0, f = 1 MHz				8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 16)

		'ACT3632-15		'ACT3632-20		'ACT3632-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_c	Clock cycle time, CLKA or CLKB	15		20		30		ns
$t_{w(CLKH)}$	Pulse duration, CLKA and CLKB high	6		8		10		ns
$t_{w(CLKL)}$	Pulse duration, CLKA and CLKB low	6		8		10		ns
$t_{su(D)}$	Setup time, A0–A35 before CLKA↑ and B0–B35 before CLKB↑	4		5		6		ns
$t_{su(EN)}$	Setup time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA before CLKA↑; $\overline{CSB}$, W/$\overline{RB}$, ENB, and MBB before CLKB↑	4.5		5		6		ns
$t_{su(RS)}$	Setup time, $\overline{RST1}$ or $\overline{RST2}$ low before CLKA↑ or CLKB↑§	5		6		7		ns
$t_{su(FS)}$	Setup time, FS0 and FS1 before $\overline{RST1}$ and $\overline{RST2}$ high	7.5		8.5		9.5		ns
$t_{h(D)}$	Hold time, A0–A35 after CLKA↑ and B0–B35 after CLKB↑	1		1		1		ns
$t_{h(EN)}$	Hold time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA after CLKA↑; $\overline{CSB}$, W/$\overline{RB}$, ENB, and MBB after CLKB↑	1		1		1		ns
$t_{h(RS)}$	Hold time, $\overline{RST1}$ or $\overline{RST2}$ low after CLKA↑ or CLKB↑§	4		4		5		ns
$t_{h(FS)}$	Hold time, FS0 and FS1 after $\overline{RST1}$ and $\overline{RST2}$ high	2		3		3		ns
t_{sk1}¶	Skew time between CLKA↑ and CLKB↑ for ORA, ORB, IRA, and IRB	7.5		9		11		ns
t_{sk2}¶	Skew time between CLKA↑ and CLKB↑ for $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$, and $\overline{AFB}$	12		16		20		ns

§ Requirement to count the clock edge as one of at least four needed to reset a FIFO
¶ Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Figures 1 through 16)

PARAMETER		'ACT3632-15		'ACT3632-20		'ACT3632-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_a	Access time, CLKA↑ to A0–A35 and CLKB↑ to B0–B35	3	11	3	13	3	15	ns
$t_{pd(C\text{-}IR)}$	Propagation delay time, CLKA↑ to IRA and CLKB↑ to IRB	2	8	2	10	2	12	ns
$t_{pd(C\text{-}OR)}$	Propagation delay time, CLKA↑ to ORA and CLKB↑ to ORB	1	8	1	10	1	12	ns
$t_{pd(C\text{-}AE)}$	Propagation delay time, CLKA↑ to $\overline{AEA}$ and CLKB↑ to $\overline{AEB}$	1	8	1	10	1	12	ns
$t_{pd(C\text{-}AF)}$	Propagation delay time, CLKA↑ to $\overline{AFA}$ and CLKB↑ to $\overline{AFB}$	1	8	1	10	1	12	ns
$t_{pd(C\text{-}MF)}$	Propagation delay time, CLKA↑ to $\overline{MBF1}$ low or $\overline{MBF2}$ high and CLKB↑ to $\overline{MBF2}$ low or $\overline{MBF1}$ high	0	8	0	10	0	12	ns
$t_{pd(C\text{-}MR)}$	Propagation delay time, CLKA↑ to B0–B35† and CLKB↑ to A0–A35‡	3	13.5	3	15	3	17	ns
$t_{pd(M\text{-}DV)}$	Propagation delay time, MBA to A0–A35 valid and MBB to B0–B35 valid	3	11	3	13	3	15	ns
$t_{pd(R\text{-}F)}$	Propagation delay time, $\overline{RST1}$ low to $\overline{AEB}$ low, $\overline{AFA}$ high, and $\overline{MBF1}$ high, and $\overline{RST2}$ low to $\overline{AEA}$ low, $\overline{AFB}$ high, and $\overline{MBF2}$ high	1	15	1	20	1	30	ns
t_{en}	Enable time, $\overline{CSA}$ and W/$\overline{RA}$ low to A0–A35 active and $\overline{CSB}$ low and $\overline{W}$/RB high to B0–B35 active	2	12	2	13	2	14	ns
t_{dis}	Disable time, $\overline{CSA}$ or W/$\overline{RA}$ high to A0–A35 at high impedance and $\overline{CSB}$ high or $\overline{W}$/RB low to B0–B35 at high impedance	1	8	1	12	1	11	ns

† Writing data to the mail1 register when the B0–B35 outputs are active and MBB is high.
‡ Writing data to the mail2 register when the A0–A35 outputs are active and MBA is high.

TYPICAL CHARACTERISTICS

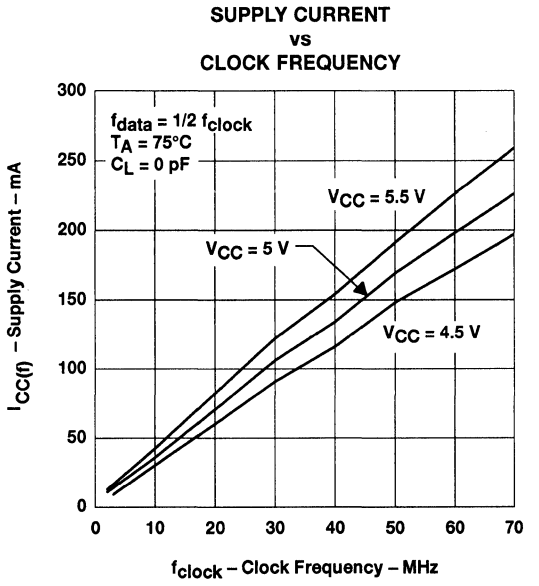


Figure 17

calculating power dissipation

The $I_{CC(f)}$ current for the graph in Figure 17 was taken while simultaneously reading and writing a FIFO on the SN74ACT3632 with CLKA and CLKB set to f_{clock}. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitive load per data-output channel and the number of SN74ACT3632 inputs driven by TTL high levels are known, the power dissipation can be calculated with the equation below.

With $I_{CC(f)}$ taken from Figure 17, the maximum power dissipation (P_T) of the SN74ACT3632 can be calculated by:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

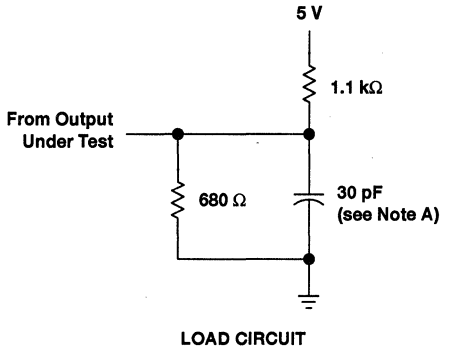
where:

N	=	number of inputs driven by TTL levels
ΔI_{CC}	=	increase in power supply current for each input at a TTL high level
dc	=	duty cycle of inputs at a TTL high level of 3.4 V
C_L	=	output capacitive load
f_o	=	switching frequency of an output

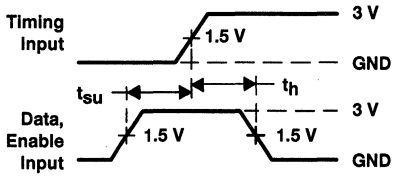
When no reads or writes are occurring on the SN74ACT3632, the power dissipated by a single clock (CLKA or CLKB) input running at frequency f_{clock} is calculated by:

$$P_T = V_{CC} \times f_{clock} \times 0.184 \text{ mA/MHz}$$

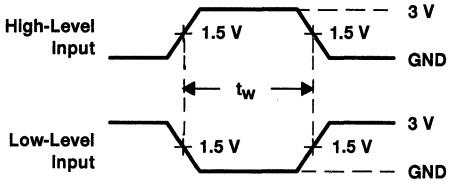
PARAMETER MEASUREMENT INFORMATION



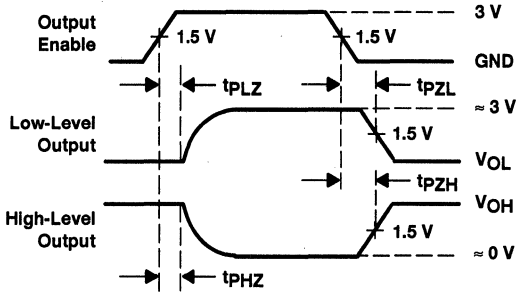
LOAD CIRCUIT



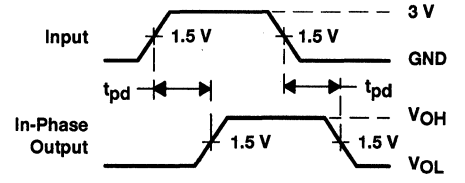
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

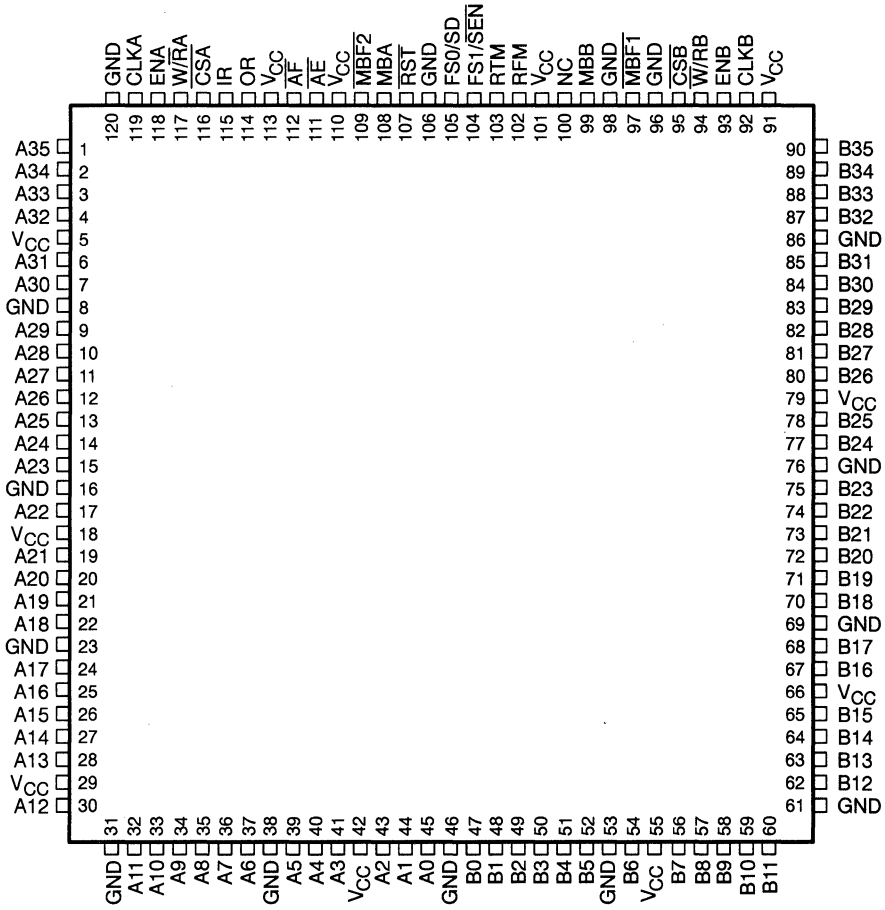
NOTE A: Includes probe and jig capacitance

Figure 18. Load Circuit and Voltage Waveforms

SCAS338A – JANUARY 1994 – REVISED JUNE 1994

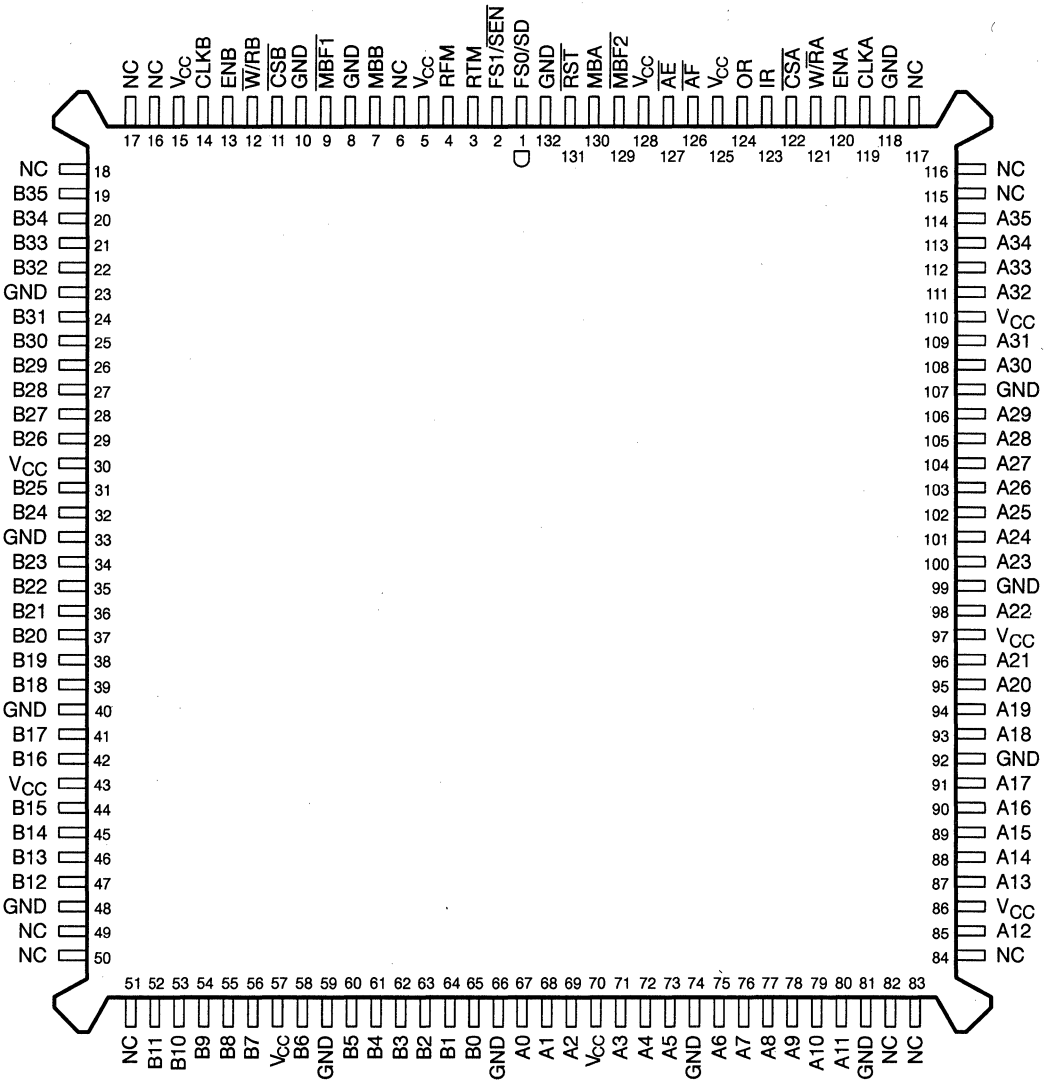
- Free-Running CLKA and CLKB Can Be Asynchronous or Coincident
- Clocked FIFO Buffering Data From Port A to Port B
- Memory Size: 1024 × 36
- Synchronous Read Retransmit Capability
- Mailbox Register in Each Direction
- Programmable Almost-Full and Almost-Empty Flags
- Microprocessor Interface Control Logic
- Input-Ready (IR) and Almost-Full ($\overline{AF}$) Flags Synchronized by CLKA
- Output-Ready (OR) and Almost-Empty ($\overline{AE}$) Flags Synchronized by CLKB
- Low-Power 0.8-Micron Advanced CMOS Technology
- Supports Clock Frequencies up to 67 MHz
- Fast Access Times of 11 ns
- Pin-to-Pin Compatible With the SN74ACT3631, and SN74ACT3651
- Available in Space-Saving 120-Pin Thin Quad Flat Package (PCB) or 132-Pin Plastic Quad Flat Package (PQ)

PCB PACKAGE
(TOP VIEW)



NC – No internal connection

PQ PACKAGE†
(TOP VIEW)



NC – No internal connection
† Uses Yamaichi socket IC51-1324-828

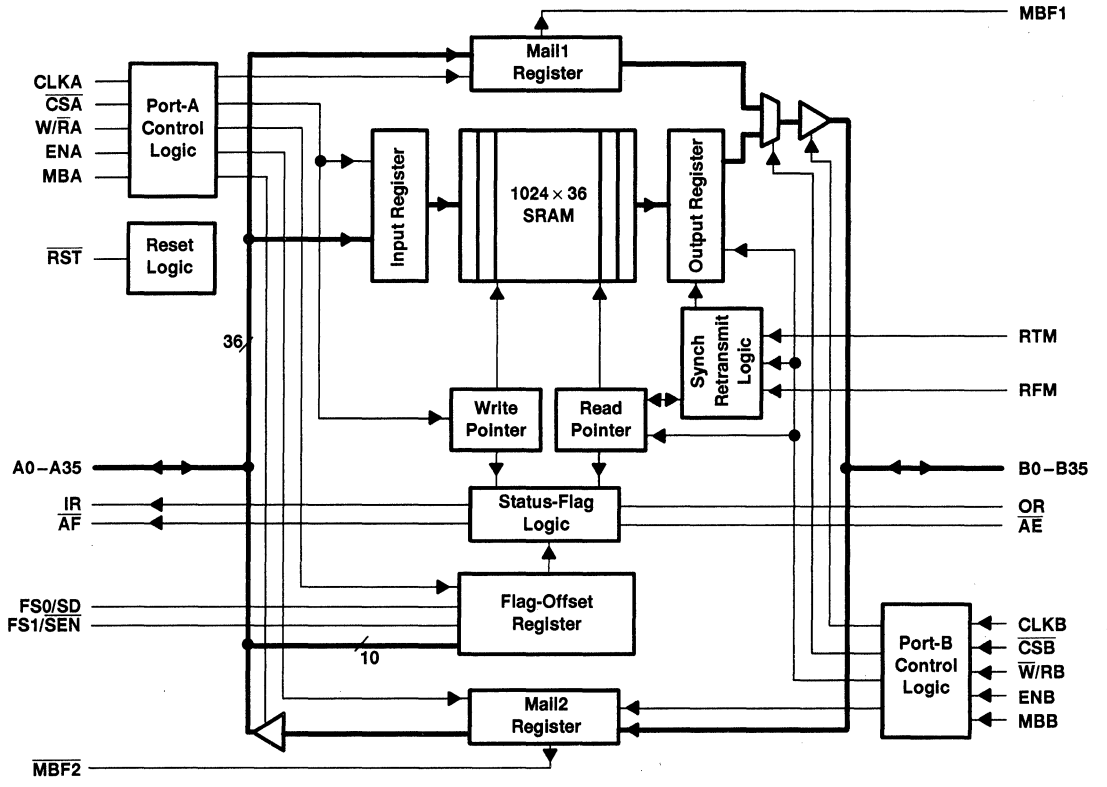
description

The SN74ACT3641 is a high-speed, low-power, CMOS clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 12 ns. The 1024 × 36 dual-port SRAM FIFO buffers data from port A to port B. The FIFO memory has retransmit capability, which allows previously read data to be accessed again. The FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words is stored in memory. Communication between each port can take place with two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Two or more devices can be used in parallel to create wider data paths. Expansion is also possible in word depth.

The SN74ACT3641 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple interface between microprocessors and/or buses with synchronous control.

The input-ready (IR) flag and almost-full ($\overline{AF}$) flag of the FIFO are two-stage synchronized to CLKA. The output-ready (OR) flag and almost-empty ($\overline{AE}$) flag of the FIFO are two-stage synchronized to CLKB. Offset values for the almost-full and almost-empty flags of the FIFO can be programmed from port A or through a serial input.

functional block diagram



Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
A0–A35	I/O	Port-A data. The 36-bit bidirectional data port for side A.
$\overline{AE}$	O	Almost-empty flag. Programmable flag synchronized to CLKB. $\overline{AE}$ is low when the number of words in the FIFO is less than or equal to the value in the almost-empty offset register (X).
$\overline{AF}$	O	Almost-full flag. Programmable flag synchronized to CLKA. $\overline{AF}$ is low when the number of empty locations in the FIFO is less than or equal to the value in the almost-full offset register (Y).
B0–B35	I/O	Port-B data. The 36-bit bidirectional data port for side B.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. IR and $\overline{AF}$ are synchronous to the low-to-high transition of CLKA.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. OR and $\overline{AE}$ are synchronous to the low-to-high transition of CLKB.
$\overline{CSA}$	I	Port-A chip select. $\overline{CSA}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{CSA}$ is high.
$\overline{CSB}$	I	Port-B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{CSB}$ is high.
ENA	I	Port-A master enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port-B master enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
FS1/$\overline{SEN}$, FS0/SD	I	Flag offset select 1/serial enable, flag offset select 0/serial data. FS1/$\overline{SEN}$ and FS0/SD are dual-purpose inputs used for flag offset register programming. During a device reset, FS1/$\overline{SEN}$ and FS0/SD select the flag offset programming method. Three offset register programming methods are available: automatically load one of two preset values, parallel load from port A, and serial load. When serial load is selected for flag offset register programming, FS1/$\overline{SEN}$ is used as an enable synchronous to the low-to-high transition of CLKA. When FS1/$\overline{SEN}$ is low, a rising edge on CLKA loads the bit present on FS0/SD into the X and Y offset registers. The number of bit writes required to program the offset registers is 20. The first bit write stores the Y-register MSB and the last bit write stores the X-register LSB.
IR	O	Input-ready flag. IR is synchronized to the low-to-high transition of CLKA. When IR is low, the FIFO is full and writes to its array are disabled. When the FIFO is in retransmit mode, IR indicates when the memory has been filled to the point of the retransmit data and prevents further writes. IR is set low during reset and is set high after reset.
MBA	I	Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation.
MBB	I	Port-B mailbox select. A high level on MBB chooses a mailbox register for a port-B read or write operation. When the B0–B35 outputs are active, a high level on MBB selects data from the mail1 register for output and a low level selects FIFO data for output.
$\overline{MBF1}$	O	Mail1 register flag. $\overline{MBF1}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. $\overline{MBF1}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and MBB is high. $\overline{MBF1}$ is set high by a reset.
$\overline{MBF2}$	O	Mail2 register flag. $\overline{MBF2}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. $\overline{MBF2}$ is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. $\overline{MBF2}$ is set high by a reset.
OR	O	Output-ready flag. OR is synchronized to the low-to-high transition of CLKB. When OR is low, the FIFO is empty and reads are disabled. Ready data is present in the output register of the FIFO when OR is high. OR is forced low during the reset and goes high on the third low-to-high transition of CLKB after a word is loaded to empty memory.
RFM	I	Read from mark. When the FIFO is in retransmit mode, a high on RFM enables a low-to-high transition of CLKB to reset the read pointer to the beginning retransmit location and output the first selected retransmit data.
$\overline{RST}$	I	Reset. To reset the device, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RST}$ is low. The low-to-high transition of $\overline{RST}$ latches the status of FS0 and FS1 for $\overline{AF}$ and $\overline{AE}$ offset selection.
RTM	I	Retransmit mode. When RTM is high and valid data is present in the FIFO output register (OR is high), a low-to-high transition of CLKB selects the data for the beginning of a retransmit and puts the FIFO in retransmit mode. The selected word remains the initial retransmit point until a low-to-high transition of CLKB occurs while RTM is low, taking the FIFO out of retransmit mode.

Terminal Functions (Continued)

TERMINAL NAME	I/O	DESCRIPTION
W/$\overline{R}$A	I	Port-A write/read select. A high on W/$\overline{R}$A selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{R}$A is high.
$\overline{W}$/RB	I	Port-B write/read select. A low on $\overline{W}$/RB selects a write operation and a high selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when $\overline{W}$/RB is low.

detailed description

reset

The SN74ACT3641 is reset by taking the reset ($\overline{RST}$) input low for at least four port-A clock (CLKA) and four port-B clock (CLKB) low-to-high transitions. The reset input can switch asynchronously to the clocks. A reset initializes the memory read and write pointers and forces the input-ready (IR) flag low, the output-ready (OR) flag low, the almost-empty ($\overline{AE}$) flag low, and the almost-full ($\overline{AF}$) flag high. Resetting the device also forces the mailbox flags ($\overline{MBF1}$, $\overline{MBF2}$) high. After a FIFO is reset, its input-ready flag is set high after at least two clock cycles to begin normal operation. A FIFO must be reset after power up before data is written to its memory.

almost-empty flag and almost-full flag offset programming

Two registers in the SN74ACT3641 are used to hold the offset values for the almost-empty and almost-full flags. The almost-empty ($\overline{AE}$) flag offset register is labeled X, and the almost-full ($\overline{AF}$) flag offset register is labeled Y. The offset registers can be loaded with a value in three ways: one of two preset values are loaded into the offset registers, parallel load from port A, or serial load. The offset register programming mode is chosen by the flag select (FS1, FS0) inputs during a low-to-high transition on the $\overline{RST}$ input (see Table 1).

Table 1. Flag Programming

FS1	FS0	$\overline{RST}$	X AND Y REGISTERS†
H	H	↑	Serial load
H	L	↑	64
L	H	↑	8
L	L	↑	Parallel load from port A

† X register holds the offset for $\overline{AE}$; Y register holds the offset for $\overline{AF}$.

preset values

If a preset value of 8 or 64 is chosen by the FS1 and FS0 inputs at the time of a $\overline{RST}$ low-to-high transition according to Table 1, the preset value is automatically loaded into the X and Y registers. No other device initialization is necessary to begin normal operation, and the IR flag is set high after two low-to-high transitions on CLKA.

parallel load from port A

To program the X and Y registers from port A, the device is reset with FS0 and FS1 low during the low-to-high transition of $\overline{RST}$. After this reset is complete, the IR flag is set high after two low-to-high transitions on CLKA. The first two writes to the FIFO do not store data in its memory but load the offset registers in the order Y, X. Each offset register of the SN74ACT3641 uses port-A inputs (A9–A0). Data input A9 is used as the most significant bit of the binary number. Each register value can be programmed from 1 to 1020. After both offset registers are programmed from port A, subsequent FIFO writes store data in the SRAM.

serial load

To program the X and Y registers serially, the device is reset with FS0/SD and FS1/$\overline{SEN}$ high during the low-to-high transition of $\overline{RST}$. After this reset is complete, the X and Y register values are loaded bitwise through the FS0/SD input on each low-to-high transition of CLKA that the FS1/$\overline{SEN}$ input is low. 20-bit writes are needed to complete the programming for the SN74ACT3641. The first-bit write stores the most significant bit of the Y register, and the last-bit write stores the least significant bit of the the X register. Each register value can be programmed from 1 to 1020.

When the option to program the offset registers serially is chosen, the input-ready (IR) flag remains low until all 20 bits are written. The IR flag is set high by the low-to-high transition of CLKA after the last bit is loaded to allow normal FIFO operation.

FIFO write/read operation

The state of the port-A data (A0–A35) outputs is controlled by the port-A chip select ($\overline{CSA}$) and the port-A write/read select (W/$\overline{RA}$). The A0–A35 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is high. The A0–A35 outputs are active when both $\overline{CSA}$ and W/$\overline{RA}$ are low.

Data is loaded into the FIFO from the A0–A35 inputs on a low-to-high transition of CLKA when $\overline{CSA}$ and the port-A mailbox select (MBA) are low, W/$\overline{RA}$, the port-A enable (ENA), and the input-ready (IR) flag are high (see Table 2). Writes to the FIFO are independent of any concurrent FIFO reads.

Table 2. Port-A Enable Function Table

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	A0–A35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, mail2 register	None
L	L	H	L	↑	Active, mail2 register	None
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set $\overline{MBF2}$ high)

The port-B control signals are identical to those of port A with the exception that the port-B write/read select ($\overline{W}$/RB) is the inverse of the port-A write/read select (W/$\overline{RA}$). The state of the port-B data (B0–B35) outputs is controlled by the port-B chip select ($\overline{CSB}$) and the port-B write/read select ($\overline{W}$/RB). The B0–B35 outputs are in the high-impedance state when either $\overline{CSB}$ is high or $\overline{W}$/RB is low. The B0–B35 outputs are active when $\overline{CSB}$ is low and $\overline{W}$/RB is high.

Data is read from the FIFO to its output register on a low-to-high transition of CLKB when $\overline{CSB}$ and the port-B mailbox select (MBB) are low, $\overline{W}$/RB, the port-B enable (ENB), and the output-ready (OR) flag are high (see Table 3). Reads from the FIFO are independent of any concurrent FIFO writes.

FIFO write/read operation (continued)

Table 3. Port-B Enable Function Table

$\overline{CSB}$	W/$\overline{RB}$	ENB	MBB	CLKB	B0–B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	L	L	X	X	In high-impedance state	None
L	L	H	L	↑	In high-impedance state	None
L	L	H	H	↑	In high-impedance state	Mail2 write
L	H	L	L	X	Active, FIFO output register	None
L	H	H	L	↑	Active, FIFO output register	FIFO read
L	H	L	H	X	Active, mail1 register	None
L	H	H	H	↑	Active, mail1 register	Mail1 read (set $\overline{MBF1}$ high)

The setup- and hold-time constraints to the port clocks for the port-chip selects and write/read selects are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is low during a clock cycle, the port chip select and write/read select can change states during the setup- and hold-time window of the cycle.

When the output-ready (OR) flag is low, the next data word is sent to the FIFO output register automatically by the CLKB low-to-high transition that sets the output-ready flag high. When OR is high, an available data word is clocked to the FIFO output register only when a FIFO read is selected by the port-B chip select ($\overline{CSB}$), write/read select (W/$\overline{RB}$), enable (ENB), and mailbox select (MBB).

synchronized FIFO flags

Each FIFO is synchronized to its port clock through at least two flip-flop stages. This is done to improve the flags' reliability by reducing the probability of metastable events on their outputs when CLKA and CLKB operate asynchronously to one another (see the application report *Metastability Performance of Clocked FIFOs* in the 1994 *High-Performance FIFO Memories Data Book*, literature #SCAD003B). OR and $\overline{AE}$ are synchronized to CLKB. IR and $\overline{AF}$ are synchronized to CLKA. Table 4 shows the relationship of each flag to the number of words stored in memory.

Table 4. FIFO Flag Operation

NUMBER OF WORDS IN FIFO†‡	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA	
	OR	$\overline{AE}$	$\overline{AF}$	IR
0	L	L	H	H
1 to X	H	L	H	H
(X + 1) to [1024 – (Y + 1)]	H	H	H	H
(1024 – Y) to 1023	H	H	L	H
1024	H	H	L	L

† X is the almost-empty offset for $\overline{AE}$. Y is the almost-full offset for $\overline{AF}$.
‡ When a word is present in the FIFO output register, its previous memory location is free.

output-ready flag (OR)

The output-ready flag of a FIFO is synchronized to the port clock that reads data from its array (CLKB). When the output-ready flag is high, new data is present in the FIFO output register. When the output-ready flag is low, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

A FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an output-ready flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. From the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of CLKB; therefore, an output-ready flag is low if a word in memory is the next data to be sent to the FIFO output register and three CLKB cycles have not elapsed since the time the word was written. The output-ready flag of the FIFO remains low until the third low-to-high transition of CLKB occurs, simultaneously forcing the output-ready flag high and shifting the word to the FIFO output register.

A low-to-high transition on CLKB begins the first synchronization cycle of a write if the clock transition occurs at time $t_{sk(1)}$ or greater after the write. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 6).

input-ready flag (IR)

The input-ready flag of a FIFO is synchronized to the port clock that writes data to its array (CLKA). When the input-ready flag is high, a memory location is free in the SRAM to write new data. No memory locations are free when the input-ready flag is low and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, its write pointer is incremented. The state machine that controls an input-ready flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is full, full–1, or full–2. From the time a word is read from a FIFO, its previous memory location is ready to be written in a minimum of three cycles of CLKA; therefore, an input-ready flag is low if less than two cycles of CLKA have elapsed since the next memory write location has been read. The second low-to-high transition on CLKA after the read sets the input-ready flag high, and data can be written in the following cycle.

A low-to-high transition on CLKA begins the first synchronization cycle of a read if the clock transition occurs at time $t_{sk(1)}$ or greater after the read. Otherwise, the subsequent CLKA cycle can be the first synchronization cycle (see Figure 7).

almost-empty flag ($\overline{AE}$)

The almost-empty flag of a FIFO is synchronized to the port clock that reads data from its array (CLKB). The state machine that controls an almost-empty flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the contents of register X. This register is loaded with a preset value during a FIFO reset, programmed from port A, or programmed serially (see *almost-empty flag and almost-full flag offset programming*). The almost-empty flag is low when the FIFO contains X or less words and is high when the FIFO contains (X + 1) or more words. A data word present in the FIFO output register has been read from memory.

Two low-to-high transitions of CLKB are required after a FIFO write for the almost-empty flag to reflect the new level of fill; therefore, the almost-empty flag of a FIFO containing (X + 1) or more words remains low if two cycles of CLKB have not elapsed since the write that filled the memory to the (X + 1) level. An almost-empty flag is set high by the second low-to-high transition of CLKB after the FIFO write that fills memory to the (X + 1) level. A low-to-high transition of CLKB begins the first synchronization cycle if it occurs at time $t_{sk(2)}$ or greater after the write that fills the FIFO to (X + 1) words. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 8).

almost-full flag ($\overline{AF}$)

The almost-full flag of a FIFO is synchronized to the port clock that writes data to its array (CLKA). The state machine that controls an almost-full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost full, almost full–1, or almost full–2. The almost-full state is defined by the contents of register Y. This register is loaded with a preset value during a FIFO reset, programmed from port A, or programmed serially (see *almost-empty flag and almost-full flag offset programming*). The almost-full flag is low when the number of words in the FIFO is greater than or equal to (1024 – Y). The almost-full flag is high when the number of words in the FIFO is less than or equal to [1024 – (Y + 1)]. A data word present in the FIFO output register has been read from memory.

Two low-to-high transitions of CLKA are required after a FIFO read for its almost-full flag to reflect the new level of fill. Therefore, the almost-full flag of a FIFO containing [1024 – (Y + 1)] or less words remains low if two cycles of CLKA have not elapsed since the read that reduced the number of words in memory to [1024 – (Y + 1)]. An almost-full flag is set high by the second low-to-high transition of CLKA after the FIFO read that reduces the number of words in memory to [1024 – (Y + 1)]. A low-to-high transition of CLKA begins the first synchronization cycle if it occurs at time $t_{sk(2)}$ or greater after the read that reduces the number of words in memory to [1024 – (Y + 1)]. Otherwise, the subsequent CLKA cycle can be the first synchronization cycle (see Figure 9).

synchronous retransmit

The synchronous retransmit feature of the SN74ACT3641 allows FIFO data to be read repeatedly starting at a user-selected position. The FIFO is first put into retransmit mode to select a beginning word and prevent on-going FIFO write operations from destroying retransmit data. Data vectors with a minimum length of three words can retransmit repeatedly starting at the selected word. The FIFO can be taken out of retransmit mode at any time and allow normal device operation.

The FIFO is put in retransmit mode by a low-to-high transition on CLKB when the retransmit mode (RTM) input is high and OR is high. This rising CLKB edge marks the data present in the FIFO output register as the first retransmit data. The FIFO remains in retransmit mode until a low-to-high transition occurs while RTM is low.

When two or more reads have been done past the initial retransmit word, a retransmit is initiated by a low-to-high transition on CLKB when the read-from-mark (RFM) input is high. This rising CLKB edge shifts the first retransmit word to the FIFO output register and subsequent reads can begin immediately. Retransmit loops can be done endlessly while the FIFO is in retransmit mode. RFM must be low during the CLKB rising edge that takes the FIFO out of retransmit mode.

When the FIFO is put into retransmit mode, it operates with two read pointers. The current read pointer operates normally, incrementing each time a new word is shifted to the FIFO output register and used by the OR and $\overline{AE}$ flags. The shadow read pointer stores the SRAM location at the time the device is put into retransmit mode and does not change until the device is taken out of retransmit mode. The shadow read pointer is used by the IR and $\overline{AF}$ flags. Data writes can proceed while the FIFO is in retransmit mode, but $\overline{AF}$ is set low by the write that stores (1024 – Y) words after the first retransmit word. The IR flag is set low by the 1024th write after the first retransmit word.

When the FIFO is in retransmit mode and RFM is high, a rising CLKB edge loads the current read pointer with the shadow read-pointer value and the OR flag reflects the new level of fill immediately. If the retransmit changes the FIFO status out of the almost-empty range, up to two CLKB rising edges after the retransmit cycle are needed to switch $\overline{AE}$ high (see Figure 11). The rising CLKB edge that takes the FIFO out of retransmit mode shifts the read pointer used by the IR and $\overline{AF}$ flags from the shadow to the current read pointer. If the change of read pointer used by IR and $\overline{AF}$ should cause one or both flags to transition high, at least two CLKA synchronizing cycles are needed before the flags reflect the change. A rising CLKA edge after the FIFO is taken out of retransmit mode is the first synchronizing cycle of IR if it occurs at time $t_{sk(1)}$ or greater after the rising CLKB edge (see Figure 12). A rising CLKA edge after the FIFO is taken out of retransmit mode is the first synchronizing cycle of $\overline{AF}$ if it occurs at time $t_{sk(2)}$ or greater after the rising CLKB edge (see Figure 14).

mailbox registers

Two 36-bit bypass registers are on the SN74ACT3641 to pass command and control information between port A and port B. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A low-to-high transition on CLKA writes A0–A35 data to the mail1 register when a port A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA with MBA high. A low-to-high transition on CLKB writes B0–B35 data to the mail2 register when a port-B write is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB with MBB high. Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) low. Attempted writes to a mail register are ignored while its mail flag is low.

When the port-B data (B0–B35) outputs are active, the data on the bus comes from the FIFO output register when the port-B mailbox select (MBB) input is low and from the mail1 register when MBB is high. Mail2 data is always present on the port-A data (A0–A35) outputs when they are active. The mail1 register flag ($\overline{MBF1}$) is set high by a low-to-high transition on CLKB when a port-B read is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB with MBB high. The mail2 register flag ($\overline{MBF2}$) is set high by a low-to-high transition on CLKA when a port-A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA with MBA high. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

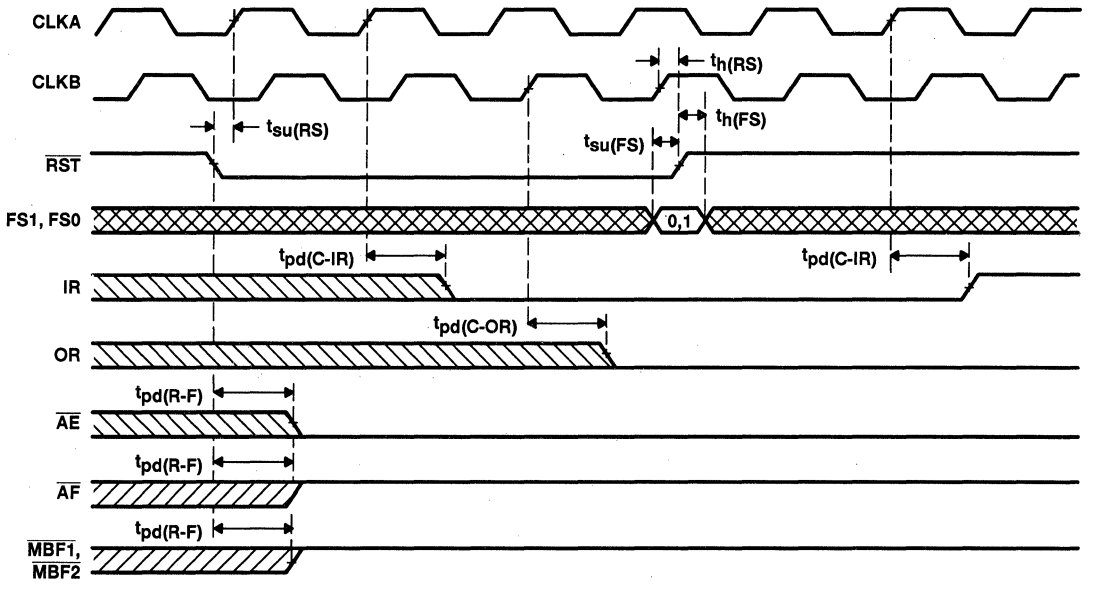
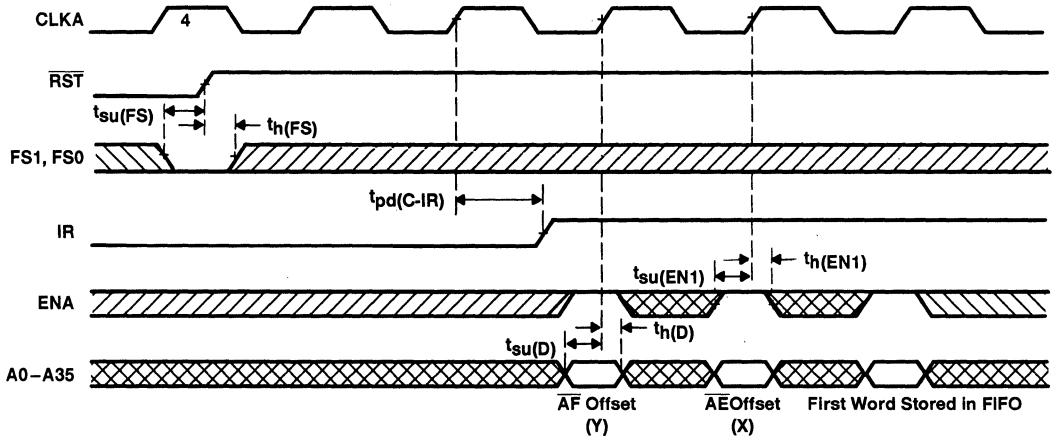
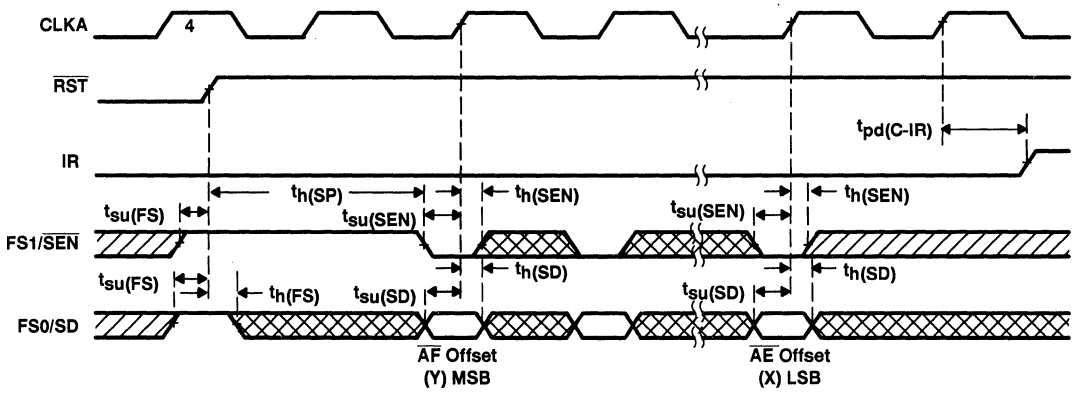


Figure 1. FIFO Reset Loading X and Y With a Preset Value of Eight



NOTE A: $\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L. It is not necessary to program offset register on consecutive clock cycles.

Figure 2. Programming the Almost-Full Flag and Almost-Empty Flag Offset Values From Port A



NOTE A: It is not necessary to program offset register bits on consecutive clock cycles. FIFO write attempts are ignored until IR is set high.

Figure 3. Programming the Almost-Full Flag and Almost-Empty Flag Offset Values Serially

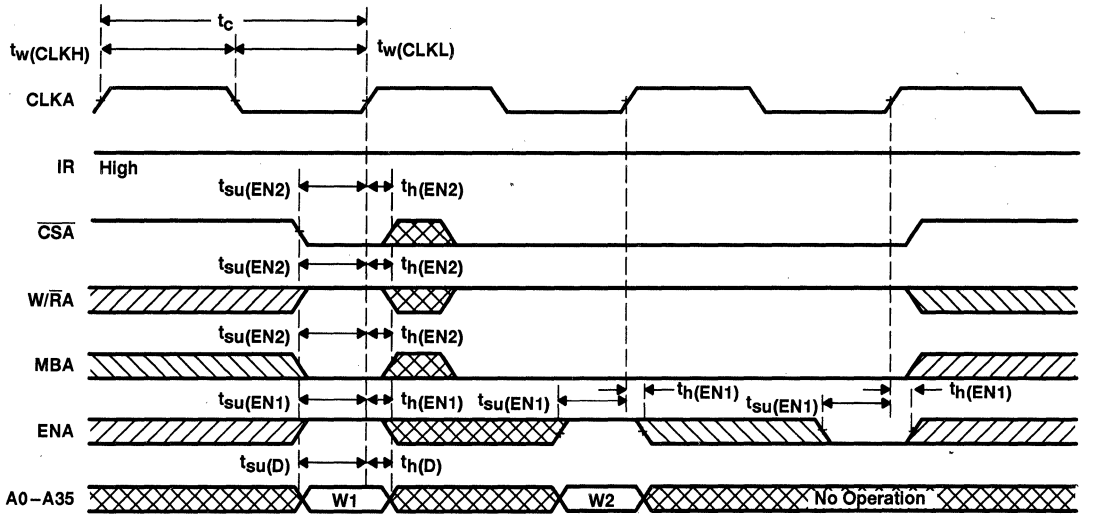


Figure 4. FIFO Write-Cycle Timing

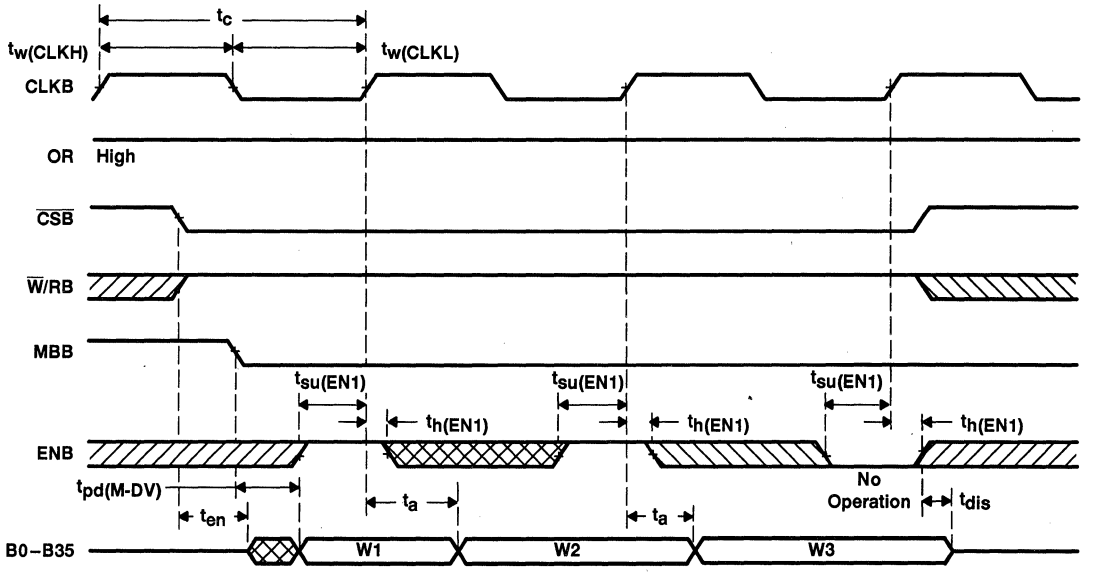
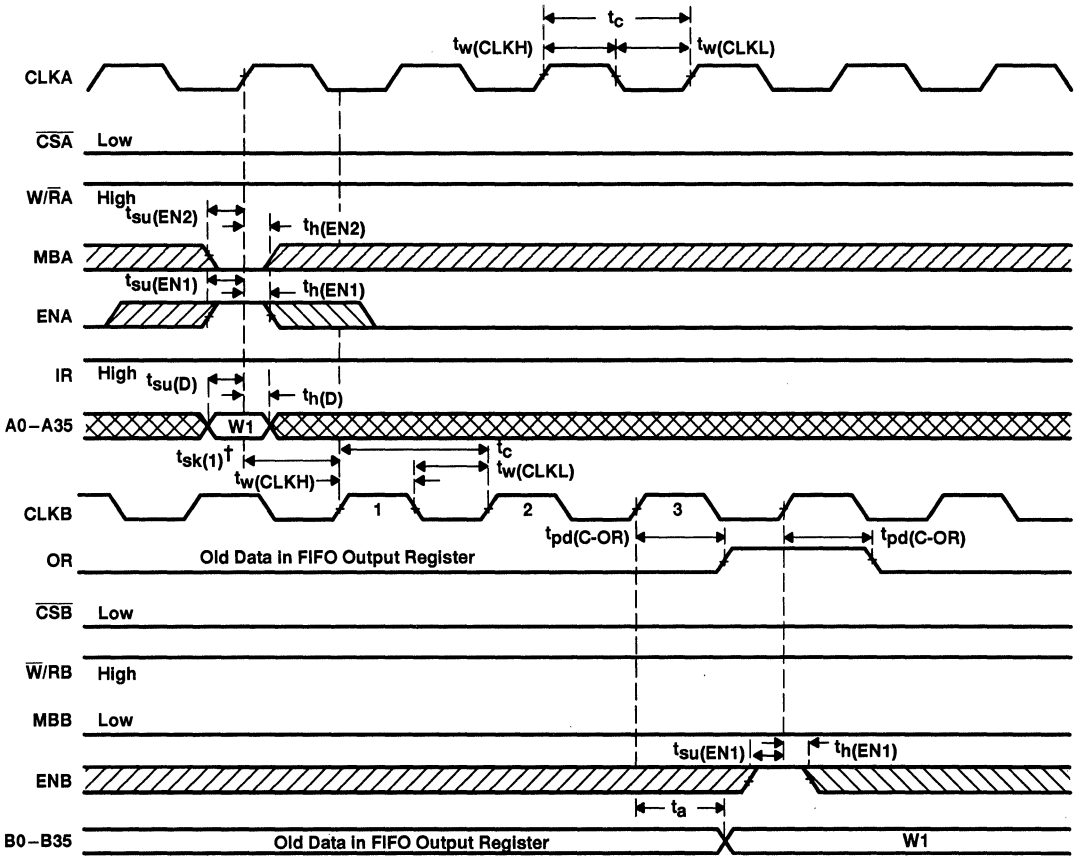
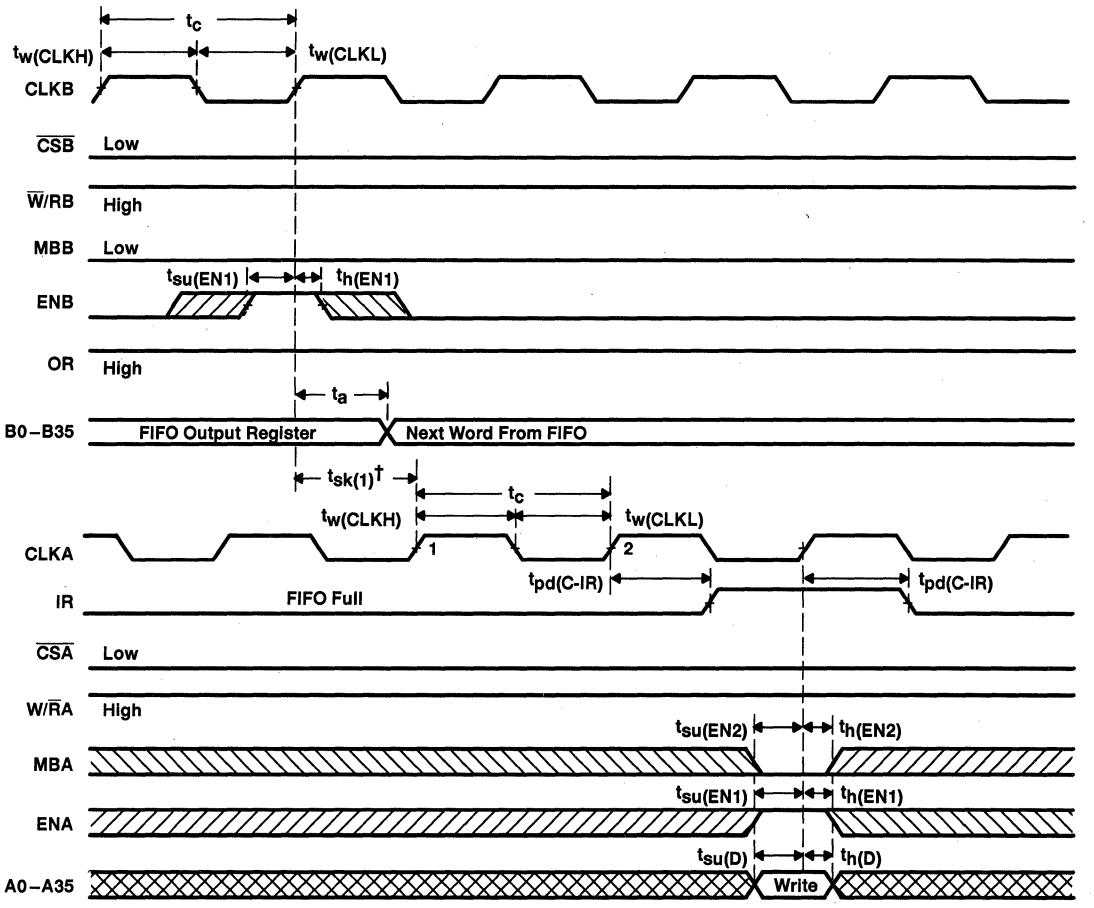


Figure 5. FIFO Read-Cycle Timing



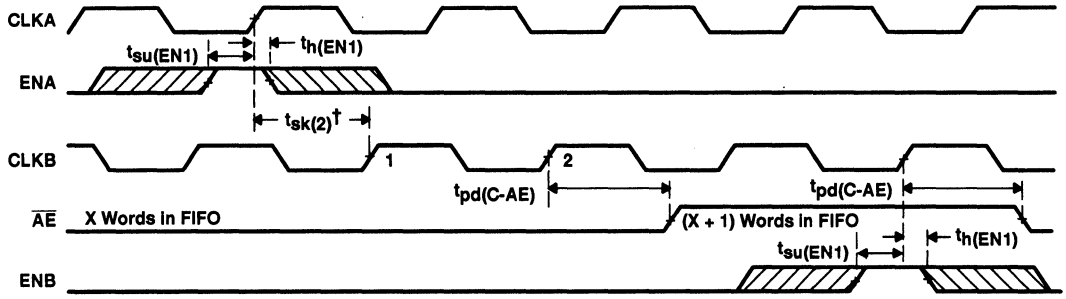
† $t_{sk(1)}$ is the minimum time between a rising CLKA edge and a rising CLKB edge for OR to transition high and to clock the next word to the FIFO output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than $t_{sk(1)}$, the transition of OR high and the first word load to the output register can occur one CLKB cycle later than shown.

Figure 6. OR-Flag Timing and First-Data-Word Fallthrough When the FIFO Is Empty



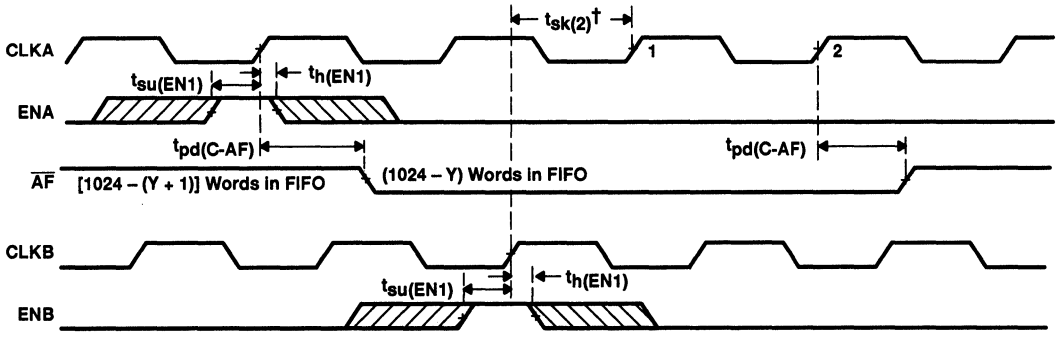
† $t_{sk(1)}$ is the minimum time between a rising CLKB edge and a rising CLKA edge for IR to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than $t_{sk(1)}$, IR can transition high one CLKA cycle later than shown.

Figure 7. IR-Flag Timing and First Available Write When the FIFO Is Full



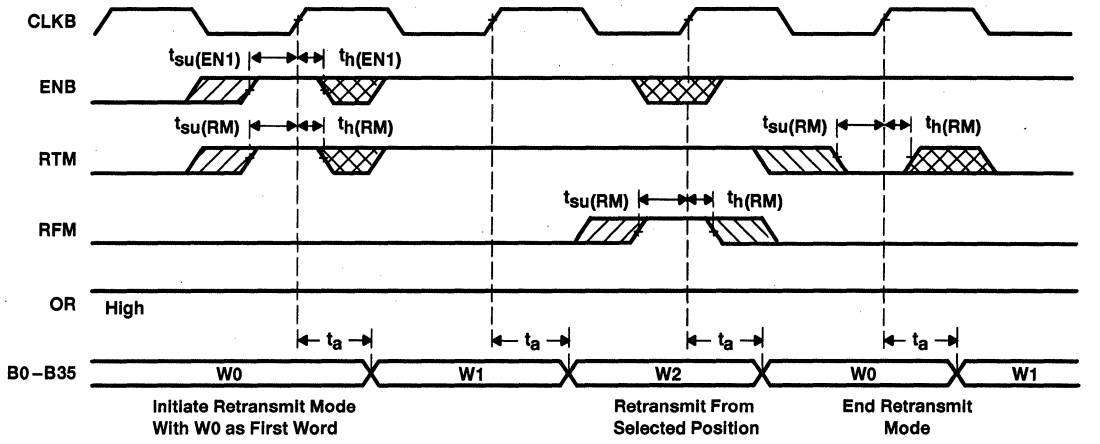
† $t_{sk(2)}$ is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AE}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than $t_{sk(2)}$, $\overline{AE}$ can transition high one CLKB cycle later than shown.
NOTE A: FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO read ($\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L)

Figure 8. Timing for $\overline{AE}$ When FIFO Is Almost Empty



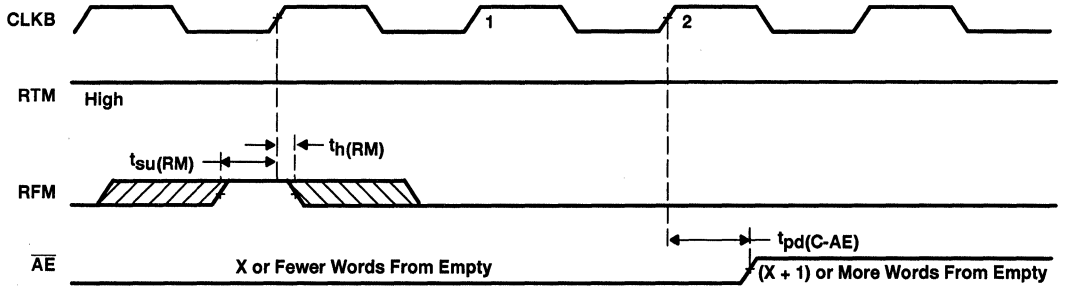
† $t_{sk(2)}$ is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AF}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than $t_{sk(2)}$, $\overline{AF}$ can transition high one CLKA cycle later than shown.
NOTE A: FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO read ($\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L)

Figure 9. Timing for $\overline{AF}$ When FIFO Is Almost Full



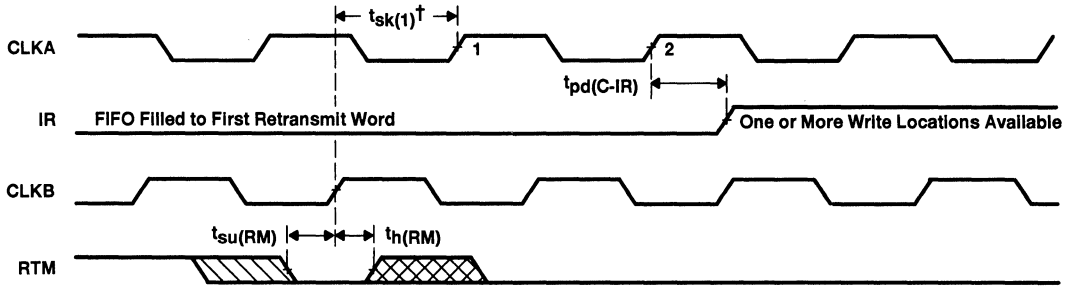
NOTE A: $\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L. No input enables other than RTM and RFM are needed to control retransmit mode or begin a retransmit. Other enables are shown only to relate retransmit operations to the FIFO output register.

Figure 10. Retransmit Timing Showing Minimum Retransmit Length



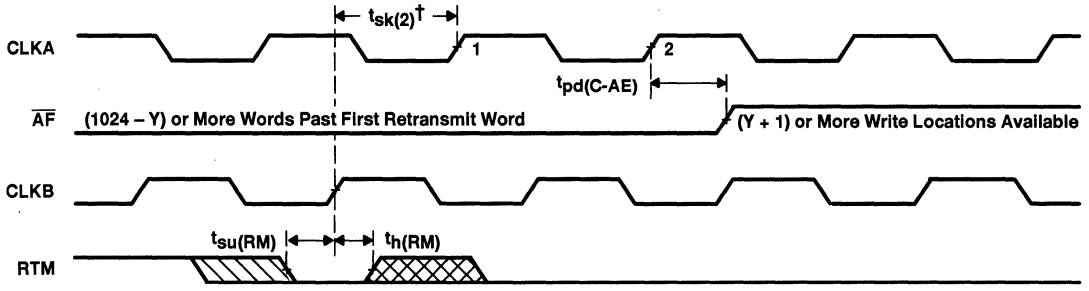
NOTE A: X is the value loaded in the almost-empty flag offset register.

Figure 11. $\overline{AE}$ Maximum Latency When Retransmit Increases the Number of Stored Words Above X



† $t_{sk(1)}$ is the minimum time between a rising CLKB edge and a rising CLKA edge for IR to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than $t_{sk(1)}$, IR can transition high one CLKA cycle later than shown.

Figure 12. IR Timing From the End of Retransmit Mode When One or More Write Locations Are Available



† $t_{sk(2)}$ is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AF}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than $t_{sk(2)}$, $\overline{AF}$ can transition high one CLKA cycle later than shown.
NOTE A: Y is the value loaded in the almost-full flag offset register.

Figure 13. $\overline{AF}$ Timing From the End of Retransmit Mode When (Y + 1) or More Write Locations Are Available

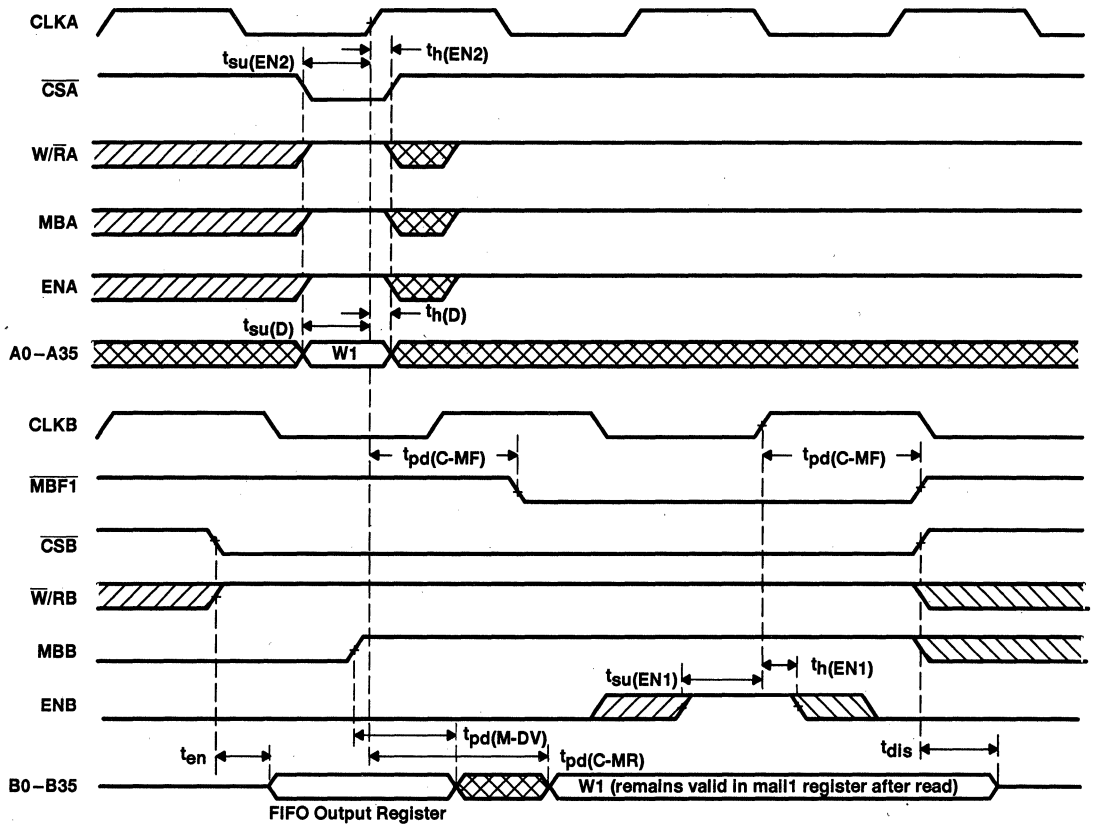


Figure 14. Timing for Mail1 Register and $\overline{\text{MBF1}}$ Flag

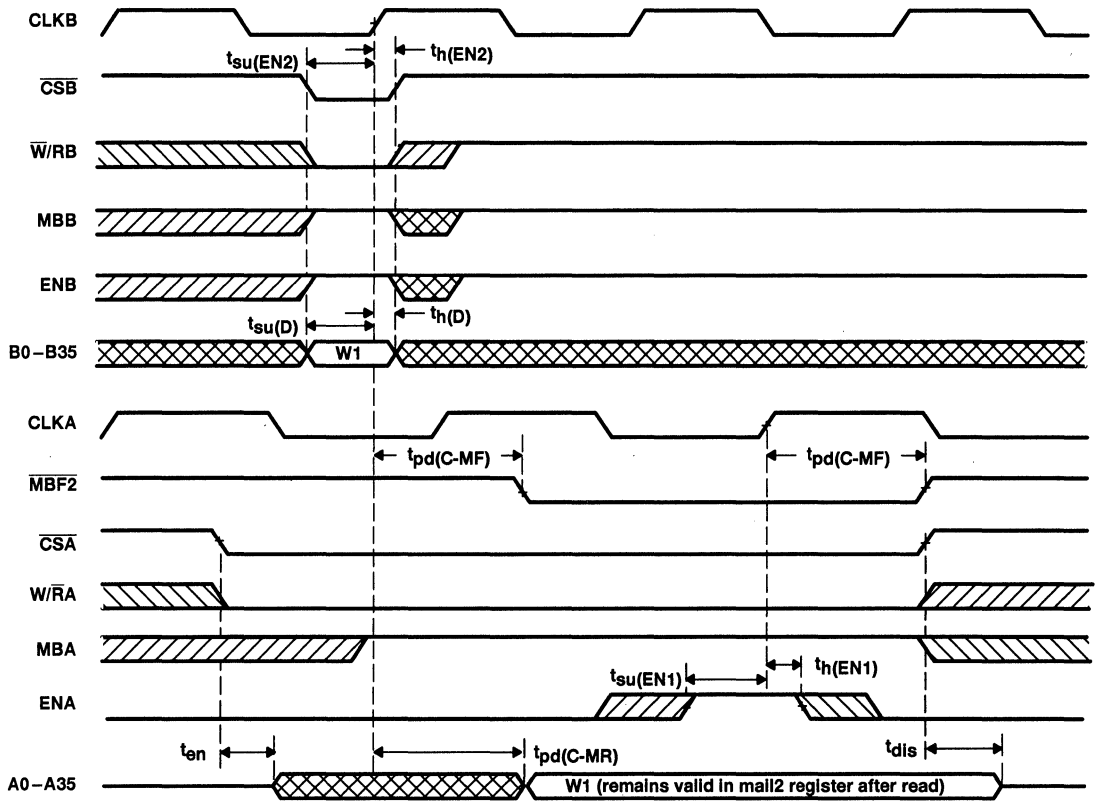


Figure 15. Timing for Mail2 Register and $\overline{\text{MBF2}}$ Flag

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−4	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS				MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −4 mA			2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0					±5	µA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0					±5	µA
I_{CC}	V_{CC} = 5.5 V,	V_I = V_{CC} − 0.2 V or 0					400	µA
ΔI_{CC}§	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,	$\overline{CSA}$ = V_{IH}	A0–A35		0		mA
			$\overline{CSB}$ = V_{IH}	B0–B35		0		
			$\overline{CSA}$ = V_{IL}	A0–A35			1	
			$\overline{CSB}$ = V_{IL}	B0–B35			1	
			All other inputs				1	
C_i	V_I = 0,	f = 1 MHz				4		pF
C_o	V_O = 0,	f = 1 MHz				8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 15)

		'ACT3641-15		'ACT3641-20		'ACT3641-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_c	Clock cycle time, CLKA or CLKB	15		20		30		ns
$t_{w(CH)}$	Pulse duration, CLKA and CLKB high	6		8		12		ns
$t_{w(CL)}$	Pulse duration, CLKA and CLKB low	6		8		12		ns
$t_{su(D)}$	Setup time, A0–A35 before CLKA↑ and B0–B35 before CLKB↑	5		6		7		ns
$t_{su(EN1)}$	Setup time, ENA to CLKA↑; ENB to CLKB↑	5		6		7		ns
$t_{su(EN2)}$	Setup time, $\overline{CSA}$, W/$\overline{R}$A, and MBA to CLKA↑; $\overline{CSB}$, W/$\overline{R}$B, and MBB to CLKB↑	7		7.5		8		ns
$t_{su(RM)}$	Setup time, RTM and RFM to CLKB↑	6		6.5		7		ns
$t_{su(RS)}$	Setup time, $\overline{RST}$ low before CLKA↑ or CLKB↑†	5		6		7		ns
$t_{su(FS)}$	Setup time, FS0 and FS1 before $\overline{RST}$ high	9		10		11		ns
$t_{su(SD)}$‡	Setup time, FS0/SD before CLKA↑	5		6		7		ns
$t_{su(SEN)}$‡	Setup time, FS1/$\overline{SEN}$ before CLKA↑	5		6		7		ns
$t_{h(D)}$	Hold time, A0–A35 after CLKA↑ and B0–B35 after CLKB↑	0		0		0		ns
$t_{h(EN1)}$	Hold time, ENA after CLKA↑; ENB after CLKB↑	0		0		0		ns
$t_{h(EN2)}$	Hold time, $\overline{CSA}$, W/$\overline{R}$A, and MBA after CLKA↑; $\overline{CSB}$, W/$\overline{R}$B, and MBB after CLKB↑	0		0		0		ns
$t_{h(RM)}$	Hold time, RTM and RFM after CLKB↑	0		0		0		ns
$t_{h(RS)}$	Hold time, $\overline{RST}$ low after CLKA↑ or CLKB↑ †	5		6		7		ns
$t_{h(FS)}$	Hold time, FS0 and FS1 after $\overline{RST}$ high	0		0		0		ns
$t_{h(SP)}$‡	Hold time, FS1/$\overline{SEN}$ high after $\overline{RST}$ high	0		0		0		ns
$t_{h(SD)}$‡	Hold time, FS0/SD after CLKA↑	0		0		0		ns
$t_{h(SEN)}$‡	Hold time, FS1/$\overline{SEN}$ after CLKA↑	0		0		0		ns
$t_{sk(1)}$§	Skew time between CLKA↑ and CLKB↑ for OR and IR	9		11		13		ns
$t_{sk(2)}$§	Skew time between CLKA↑ and CLKB↑ for $\overline{AE}$ and $\overline{AF}$	12		16		20		ns

† Requirement to count the clock edge as one of at least four needed to reset a FIFO

‡ Only applies when serial load method is used to program flag offset registers

§ Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Figures 1 through 15)

PARAMETER		'ACT3641-15		'ACT3641-20		'ACT3641-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_a	Access time, CLKB↑ to B0–B35	3	11	3	13	3	15	ns
$t_{pd(C-IR)}$	Propagation delay time, CLKA↑ to IR	1	8	1	10	1	12	ns
$t_{pd(C-OR)}$	Propagation delay time, CLKB↑ to OR	1	8	1	10	1	12	ns
$t_{pd(C-AE)}$	Propagation delay time, CLKB↑ to $\overline{AE}$	1	8	1	10	1	12	ns
$t_{pd(C-AF)}$	Propagation delay time, CLKA↑ to $\overline{AF}$	1	8	1	10	1	12	ns
$t_{pd(C-MF)}$	Propagation delay time, CLKA↑ to $\overline{MBF1}$ low or $\overline{MBF2}$ high and CLKB↑ to $\overline{MBF2}$ low or $\overline{MBF1}$ high	0	8	0	10	0	12	ns
$t_{pd(C-MR)}$	Propagation delay time, CLKA↑ to B0–B35† and CLKB↑ to A0–A35‡	3	13.5	3	15	3	17	ns
$t_{pd(M-DV)}$	Propagation delay time, MBB to B0–B35 valid	3	13	3	15	3	17	ns
$t_{pd(R-F)}$	Propagation delay time, $\overline{RST}$ low to $\overline{AE}$ low and $\overline{AF}$ high	1	15	1	20	1	30	ns
t_{en}	Enable time, $\overline{CSA}$ and W/$\overline{RA}$ low to A0–A35 active and $\overline{CSB}$ low and $\overline{W}$/RB high to B0–B35 active	2	12	2	13	2	14	ns
t_{dis}	Disable time, $\overline{CSA}$ or W/$\overline{RA}$ high to A0–A35 at high impedance and $\overline{CSB}$ high or $\overline{W}$/RB low to B0–B35 at high impedance	1	8	1	10	1	11	ns

† Writing data to the mail1 register when the B0–B35 outputs are active and MBB is high.
‡ Writing data to the mail2 register when the A0–A35 outputs are active and MBA is high.

TYPICAL CHARACTERISTICS

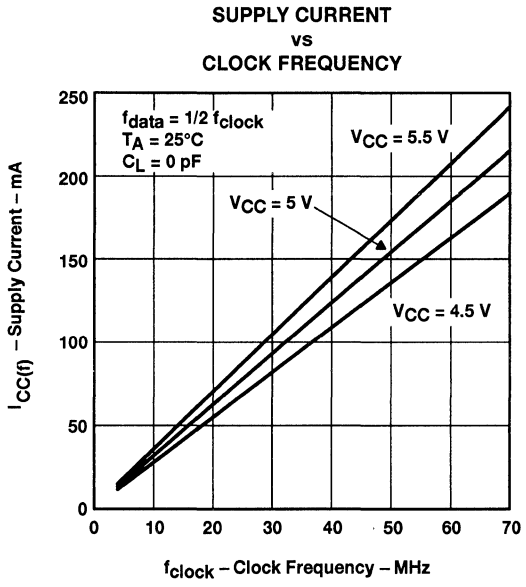


Figure 16

calculating power dissipation

The $I_{CC(f)}$ current in Figure 16 was taken while simultaneously reading and writing the FIFO on the SN74ACT3641 with CLKA and CLKB set to f_{clock}. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs are disconnected to normalize the graph to a zero-capacitance load. Once the capacitive load per data-output channel and the number of SN74ACT3641 inputs driven by TTL high levels are known, the power dissipation can be calculated with the equation below.

With $I_{CC(f)}$ taken from Figure 16, the maximum power dissipation (P_T) of the SN74ACT3641 can be calculated by:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

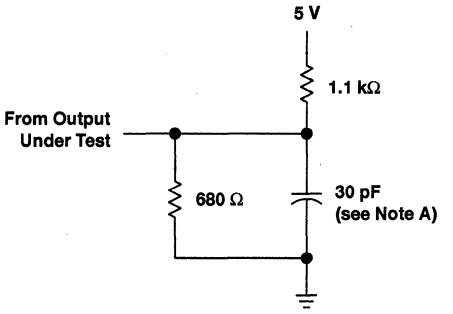
where:

- N = number of inputs driven by TTL levels
- ΔI_{CC} = increase in power supply current for each input at a TTL high level
- dc = duty cycle of inputs at a TTL high level of 3.4 V
- C_L = output capacitive load
- f_o = switching frequency of an output

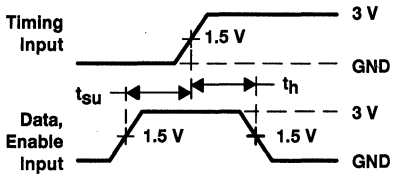
When no reads or writes are occurring on the SN74ACT3632, the power dissipated by a single clock (CLKA or CLKB) input running at frequency f_{clock} is calculated by:

$$P_T = V_{CC} \times f_{clock} \times 0.29 \text{ mA/MHz}$$

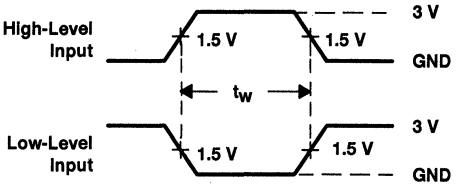
PARAMETER MEASUREMENT INFORMATION



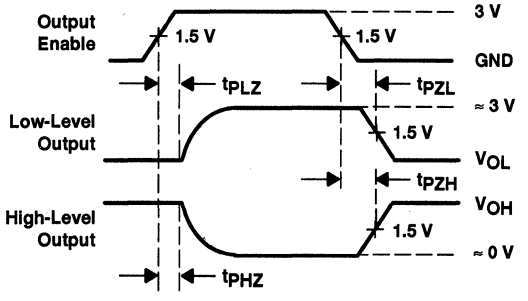
LOAD CIRCUIT



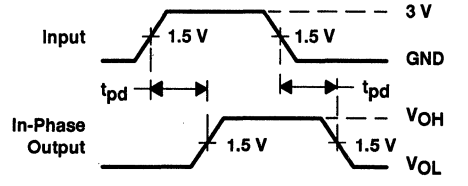
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

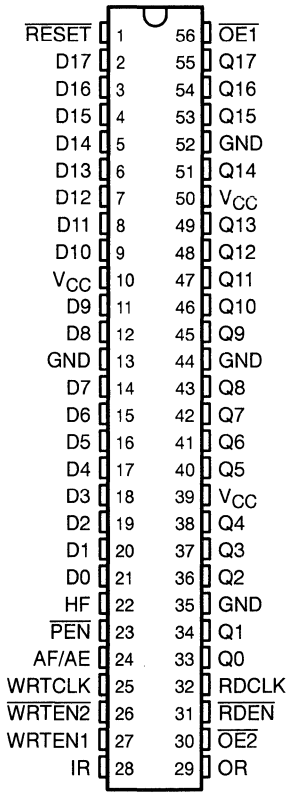
NOTE A: Includes probe and jig capacitance

Figure 17. Load Circuit and Voltage Waveforms

SCAS191 – MARCH 1991 – REVISED MARCH 1992

- **Member of the Texas Instruments Widebus™ Family**
- **Free-Running Read and Write Clocks Can Be Asynchronous or Coincident**
- **Read and Write Operations Synchronized to Independent System Clocks**
- **Input-Ready Flag Synchronized to Write Clock**
- **Output-Ready Flag Synchronized to Read Clock**
- **512 Words by 18 Bits**
- **Low-Power Advanced CMOS Technology**
- **Half-Full Flag and Programmable Almost-Full/Almost-Empty Flag**
- **Bidirectional Configuration and Width Expansion Without Additional Logic**
- **Fast Access Times of 12 ns With a 50-pF Load and All Data Outputs Switching Simultaneously**
- **Data Rates From 0 to 67 MHz**
- **Pin Compatible With SN74ACT7805 and SN74ACT7813**
- **Packaged in Shrink Small-Outline 300-mil Package (DL) Using 25-mil Center-to-Center Spacing**

DL PACKAGE
(TOP VIEW)



description

The SN74ACT7803 is a 512-word × 18-bit FIFO suited for buffering asynchronous data paths at 67-MHz clock rates and 12-ns access times. Its 56-pin shrink small-outline package (DL) offers greatly reduced board space over DIP, PLCC, and conventional SOIC packages. Two devices can be configured for bidirectional data buffering without additional logic. Multiple distributed V_{CC} and GND pins along with TI's patented output edge control (OEC™) circuit dampen simultaneous switching noise.

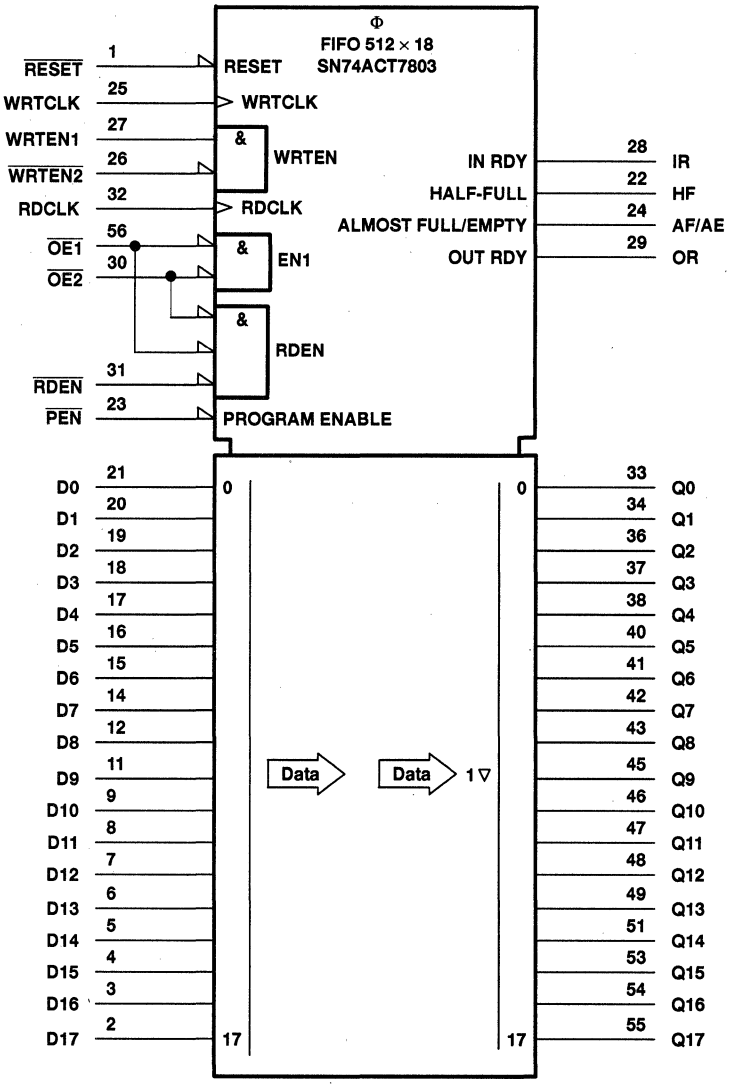
The write clock (WRTCLK) and read clock (RDCLK) should be free running and can be asynchronous or coincident. Data is written to memory on the rising edge of WRTCLK when WRTEN1 is high, $\overline{\text{WRTEN2}}$ is low, and IR is high. Data is read from memory on the rising edge of RDCLK when $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ are low and OR is high. The first word written to memory is clocked through to the output buffer regardless of the $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ levels. The OR flag indicates that valid data is present on the output buffer.

The FIFO can be reset asynchronously to WRTCLK and RDCLK. $\overline{\text{RESET}}$ must be asserted while at least four WRTCLK and four RDCLK rising edges occur to clear the synchronizing registers. Resetting the FIFO initializes the IR, OR, and HF flags low and the AF/AE flag high. The FIFO must be reset upon power up.

The SN74ACT7803 is characterized for operation from 0°C to 70°C.

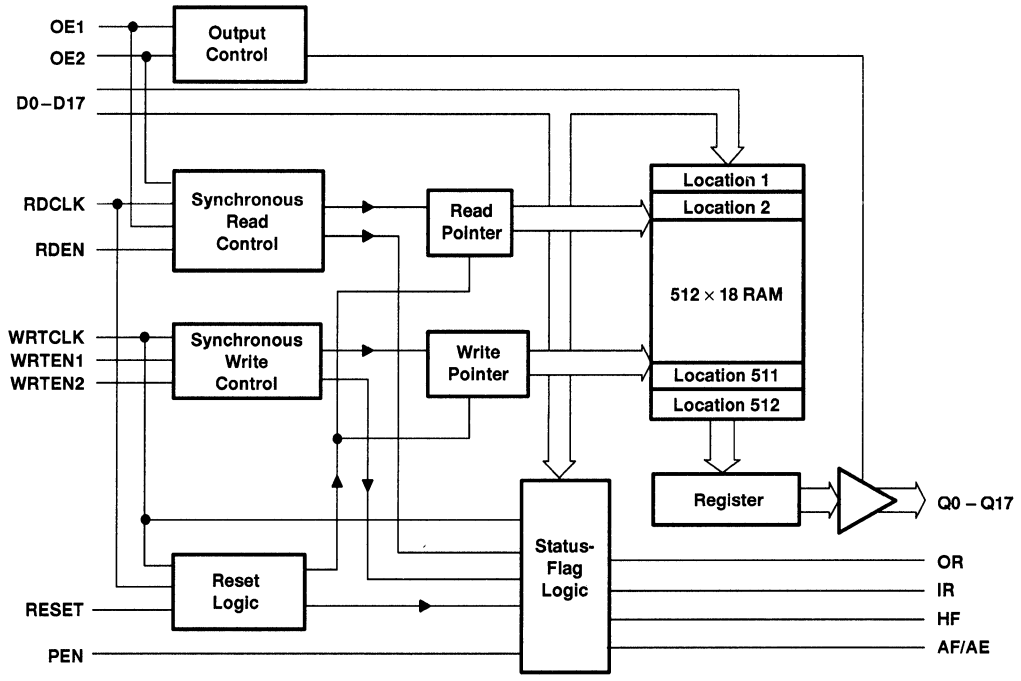
Widebus and OEC are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AE	24	O	Almost-full/almost-empty flag. Depth offset values can be programmed for AF/AE, or the default value of 64 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or less words or (512 – Y) or more words. AF/AE is high after reset.
D0–D17	21–14, 12–11, 9–2	I	The 18-bit data input port
HF	22	O	Half-full flag. HF is high when the FIFO memory contains 256 or more words. HF is low after reset.
IR	28	O	Input-ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is low during reset and goes high on the second low-to-high transition of WRTCLK after reset.
$\overline{OE1}$, $\overline{OE2}$	56, 30	I	Output enables. When $\overline{OE1}$, $\overline{OE2}$, and $\overline{RDEN}$ are low and OR is high, data is read from the FIFO on a low-to-high transition of RDCLK. When either $\overline{OE1}$ or $\overline{OE2}$ is high, reads are disabled and the data outputs are in the high-impedance state.
OR	29	O	Output-ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on Q0–Q17 when OR is high. OR is low during reset and goes high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory.
$\overline{PEN}$	23	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D7 is latched as an AF/AE offset value when $\overline{PEN}$ is low and WRTCLK is high.
Q0–Q17	33–34, 36–38, 40–43, 45–49, 51, 53–55	O	The 18-bit data output port. After the first valid write to empty memory, the first word is output on Q0–Q17 on the third rising edge of RDCLK. OR is also asserted high at this time to indicate ready data. When OR is low, the last word read from the FIFO is present on Q0–Q17.
RDCLK	32	I	Read clock. RDCLK is a continuous clock and can be asynchronous or coincident to WRTCLK. A low-to-high transition of RDCLK reads data from memory when $\overline{OE1}$, $\overline{OE2}$, and $\overline{RDEN}$ are low and OR is high. OR is synchronous to the low-to-high transition of RDCLK.
$\overline{RDEN}$	31	I	Read enable. When $\overline{RDEN}$, $\overline{OE1}$, and $\overline{OE2}$ are low and OR is high, data is read from the FIFO on the low-to-high transition of RDCLK.
$\overline{RESET}$	1	I	Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{RESET}$ is low. This sets HF, IR, and OR low and AF/AE high.
WRTCLK	25	I	Write clock. WRTCLK is a continuous clock and can be asynchronous or coincident to RDCLK. A low-to-high transition of WRTCLK writes data to memory when $\overline{WRTEN2}$ is low, WRTEN1 is high, and IR is high. IR is synchronous to the low-to-high transition of WRTCLK.
WRTEN1, $\overline{WRTEN2}$	27, 26	I	Write enables. When WRTEN1 is high, $\overline{WRTEN2}$ is low, and IR is high, data is written to the FIFO on a low-to-high transition of WRTCLK.

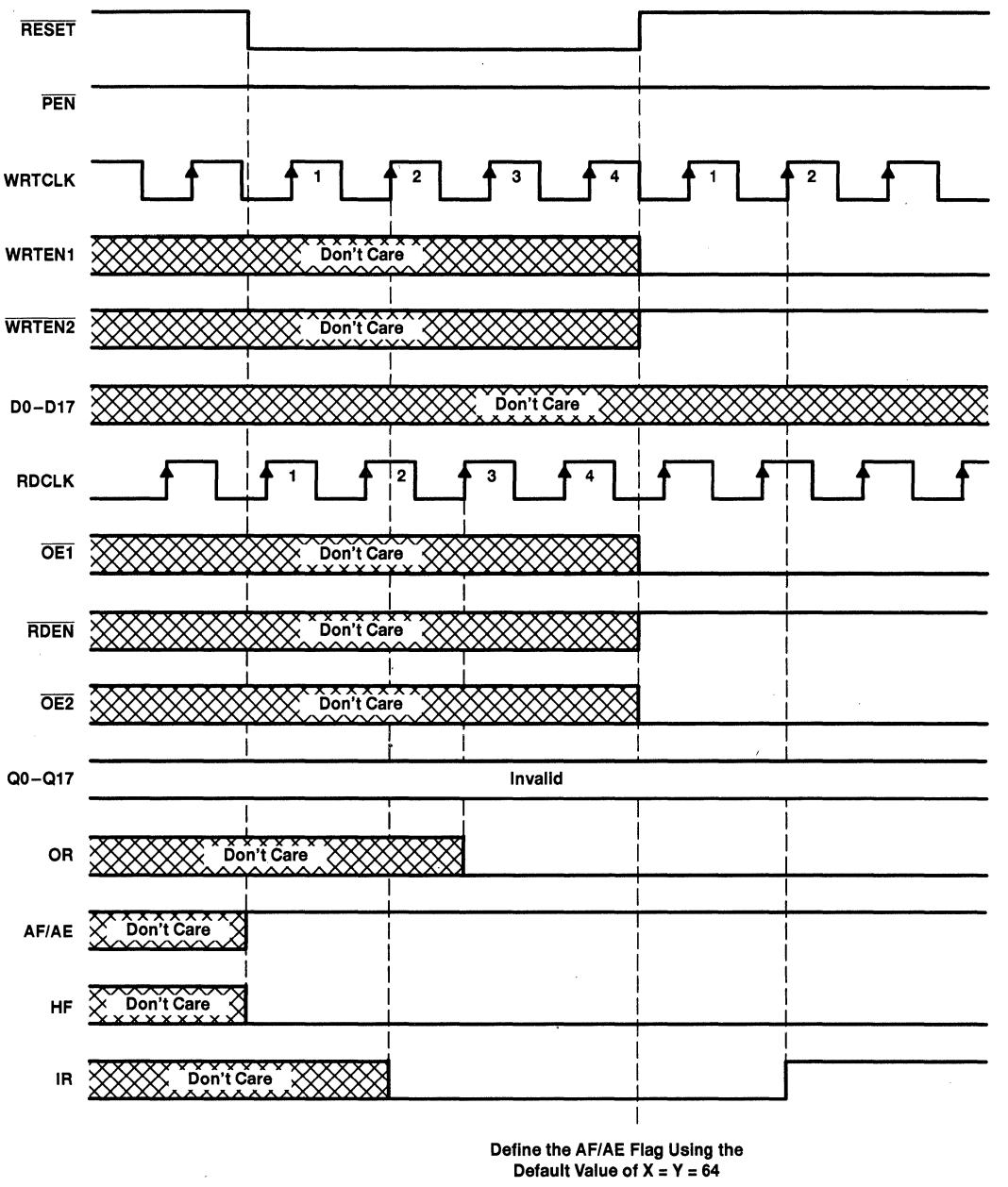


Figure 1. Reset Cycle

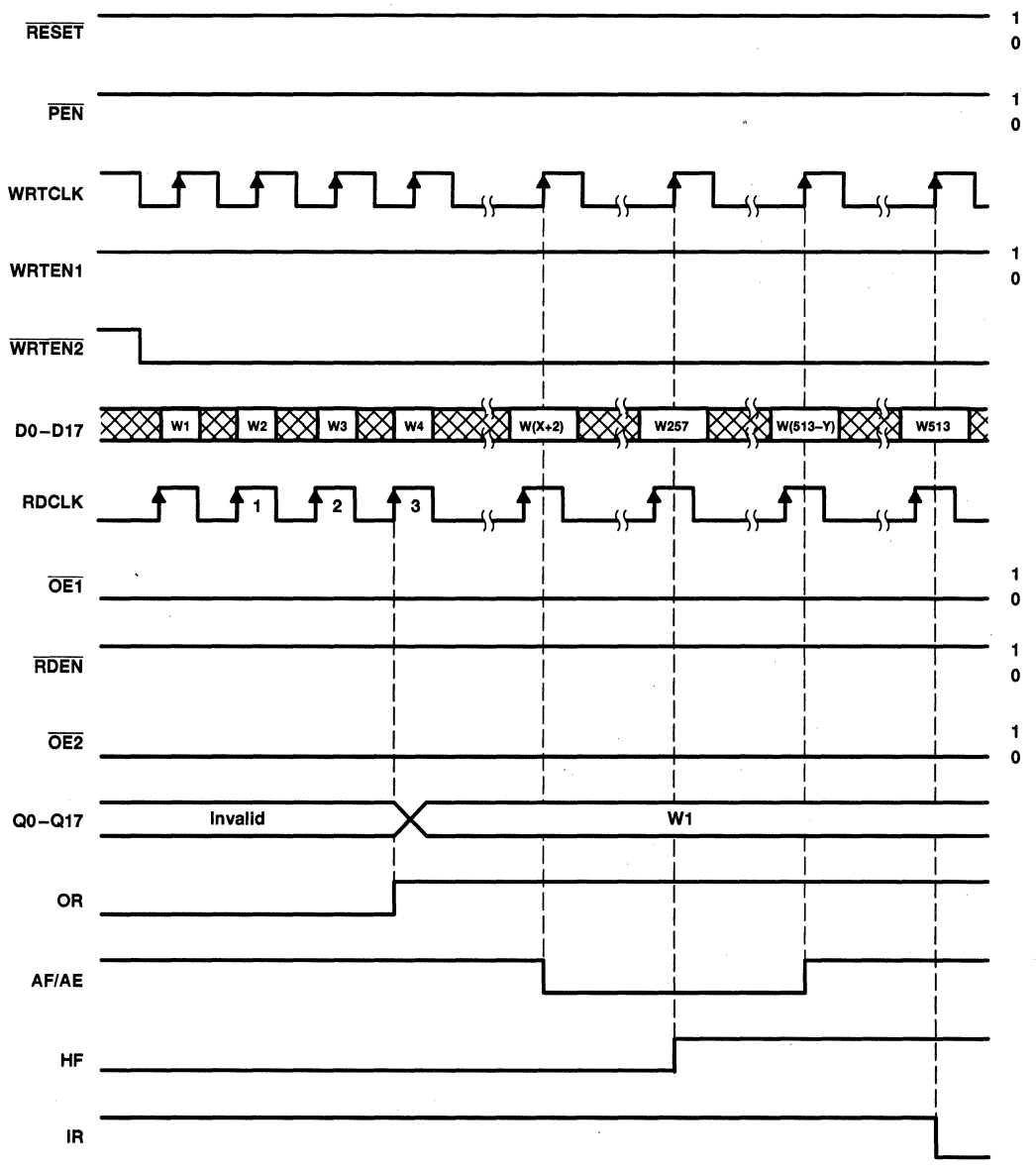


Figure 2. Write Cycle

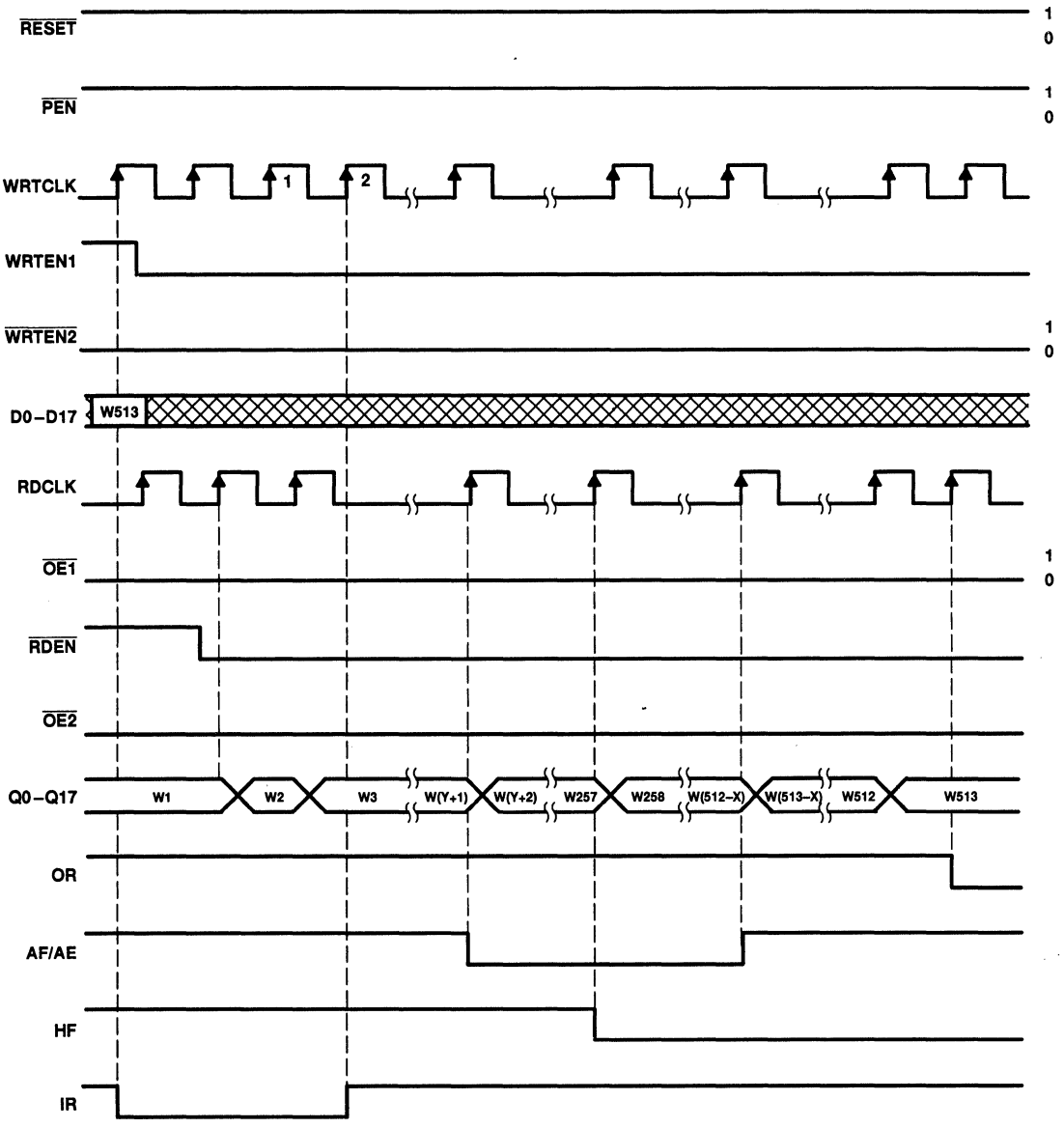


Figure 3. Read Cycle

offset values for AF/AE

The almost-full/almost-empty flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of X = Y = 64 are used. The AF/AE flag is high when the FIFO contains X or less words or (512 – Y) or more words.

Program enable ($\overline{PEN}$) should be held high throughout the reset cycle. $\overline{PEN}$ can be brought low only when IR is high and WRTCLK is low. On the following low-to-high transition of WRTCLK, the binary value on D0–D7 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{PEN}$ low for another low-to-high transition of WRTCLK reprograms Y to the binary value on D0–D7 at the time of the second WRTCLK low-to-high transition. When the offsets are being programmed, writes to the FIFO memory are disabled regardless of the state of the write enables (WRTEN1, $\overline{WRTEN2}$). A maximum value of 255 can be programmed for either X or Y (see Figure 4). To use the default values of X = Y = 64, $\overline{PEN}$ must be held high.

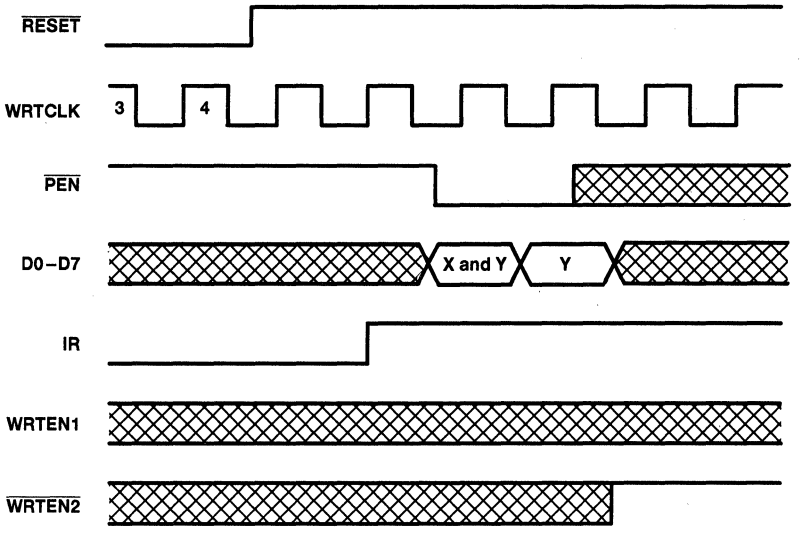


Figure 4. Programming X and Y Separately

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage, V_I ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			'ACT7803-15		'ACT7803-20		'ACT7803-25		'ACT7803-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8		0.8		0.8	V
I_{OH}	High-level output current	Q outputs, Flags		−8		−8		−8		−8	mA
I_{OL}	Low-level output current	Q outputs		16		16		16		16	mA
		Flags		8		8		8		8	
f_{clock}	Clock frequency			67		50		40		25	MHz
t_w	Pulse duration	WRTCLK high or low	6		7		8		12		ns
		RDCLK high or low	6		7		8		12		
		$\overline{PEN}$ low	8		9		9		12		
t_{su}	Setup time	D0–D17 before WRTCLK↑	4		5		5		5		ns
		WRTEN1, $\overline{WRTEN2}$ before WRTCLK↑	4		5		5		5		
		$\overline{OE1}$, $\overline{OE2}$ before RDCLK↑	5		5		6		6		
		$\overline{RDEN}$ before RDCLK↑	4		5		5		5		
		Reset: $\overline{RESET}$ low before first WRTCLK↑ and RDCLK↑†	5		6		6		6		
		$\overline{PEN}$ before WRTCLK↑	5		6		6		6		
t_h	Hold time	D0–D17 after WRTCLK↑	0		0		0		0		ns
		WRTEN1, $\overline{WRTEN2}$ after WRTCLK↑	0		0		0		0		
		$\overline{OE1}$, $\overline{OE2}$, $\overline{RDEN}$ after RDCLK↑	0		0		0		0		
		Reset: $\overline{RESET}$ low after fourth WRTCLK↑ and RDCLK↑†	2		2		2		2		
		$\overline{PEN}$ high after WRTCLK↓	0		0		0		0		
		$\overline{PEN}$ low after WRTCLK↑	2		2		2		2		
T_A	Operating free-air temperature		0	70	0	70	0	70	0	70	°C

† To permit the clock pulse to be utilized for reset purposes

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = – 8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	μA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	μA
I_{CC}		V_I = V_{CC} – 0.2 V or 0					400	μA
ΔI_{CC}‡		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 9 and 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7803-15			'ACT7803-20		'ACT7803-25		'ACT7803-40		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	WRTCLK or RDCLK		67			50		40		25		MHz
t_{pd}	RDCLK↑	Any Q	4	9.5	12	4	13	4	15	4	20	ns
t_{pd}§				8.5								
t_{pd}	WRTCLK↑	IR	3		8.5	3	11	3	13	3	15	ns
t_{pd}	RDCLK↑	OR	3		8.5	3	11	3	13	3	15	ns
t_{pd}	WRTCLK↑	AF/AE	7		16.5	7	19	7	21	7	23	ns
t_{pd}	RDCLK↑	AF/AE	7		17	7	19	7	21	7	23	ns
t_{PLH}	WRTCLK↑	HF	7		15	7	17	7	19	7	21	ns
t_{PHL}	RDCLK↑		7		15.5	7	18	7	20	7	22	
t_{PLH}	$\overline{RESET}$ low	AF/AE	2		9	2	11	2	13	2	15	ns
t_{PHL}		HF	2		10	2	12	2	14	2	16	
t_{en}	$\overline{OE1}$, $\overline{OE2}$	Any Q	2		8.5	2	11	2	11	2	11	ns
t_{dis}			2		9.5	2	11	2	14	2	14	

§ This parameter is measured with a 30-pF load (see Figure 5).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF,	f = 5 MHz	53	pF

TYPICAL CHARACTERISTICS

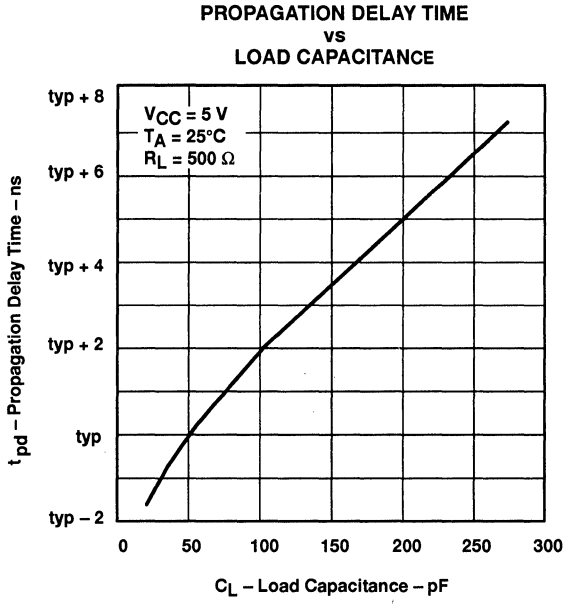


Figure 5

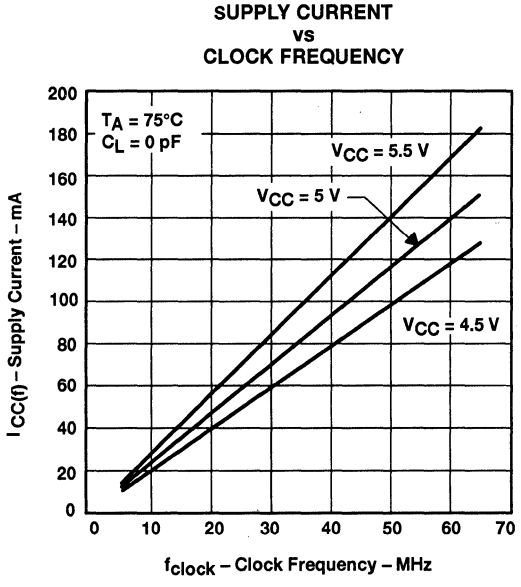


Figure 6

TYPICAL CHARACTERISTICS

calculating power dissipation

With $I_{CC(f)}$ taken from Figure 6, the maximum power dissipation (P_T) based on all data outputs changing states on each read can be calculated using:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC}	=	power-down I_{CC} maximum
N	=	number of inputs driven by a TTL device
ΔI_{CC}	=	increase in supply current
dc	=	duty cycle of inputs at a TTL high level of 3.4 V
C_{pd}	=	power dissipation capacitance
C_L	=	output capacitive load
f_i	=	data input frequency
f_o	=	data output frequency

APPLICATION INFORMATION

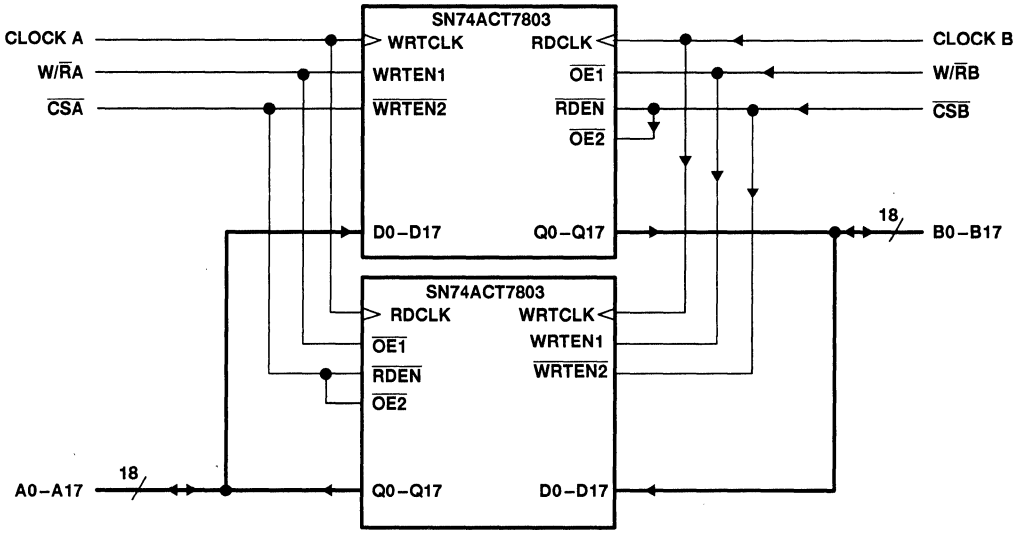


Figure 7. Bidirectional Configuration

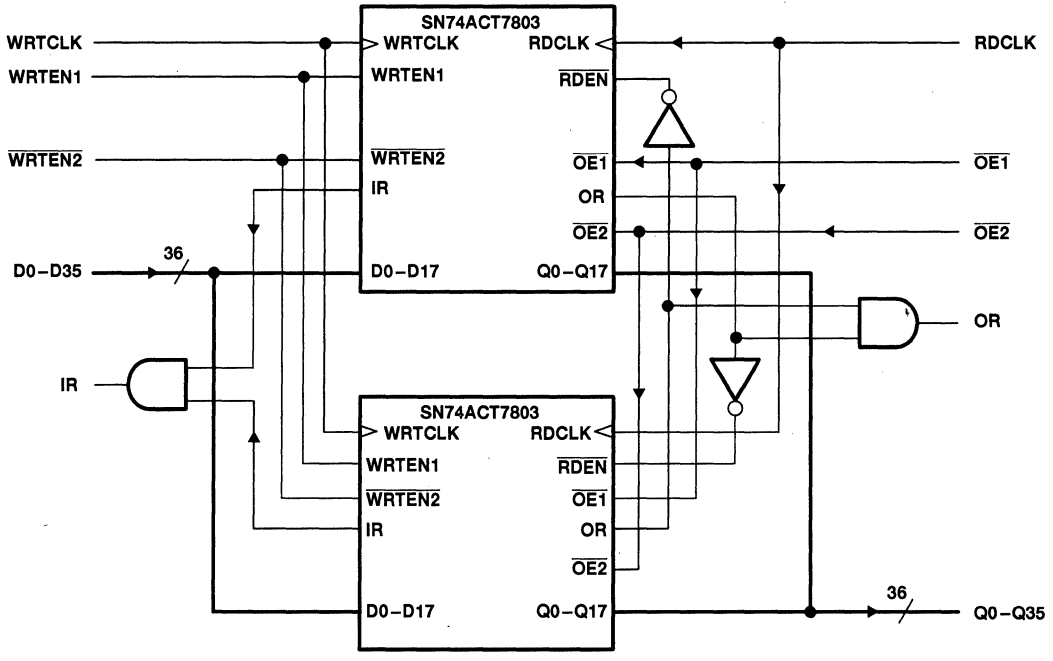


Figure 8. Word-Width Expansion: 512 × 36 Bits

PARAMETER MEASUREMENT INFORMATION

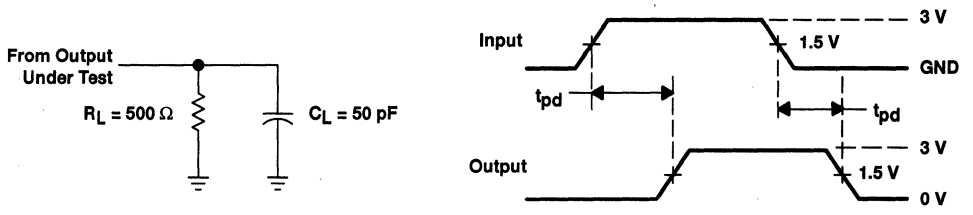
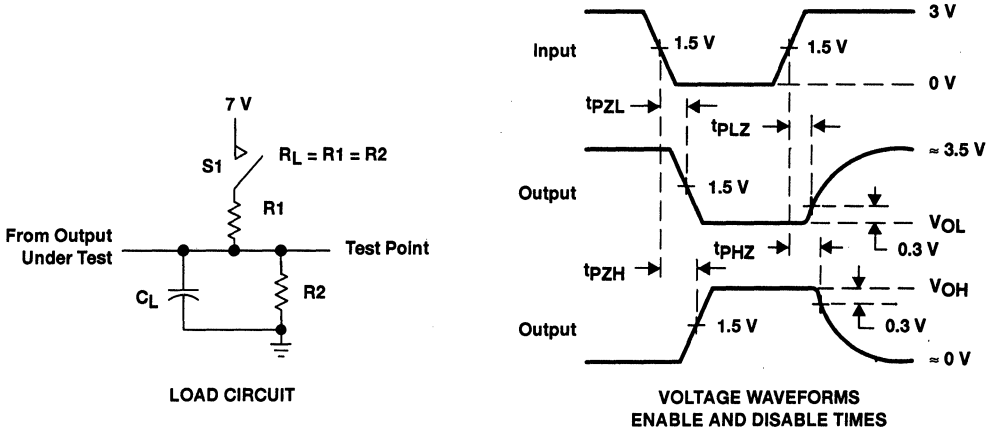


Figure 9. Standard CMOS Outputs (IR, OR, HF, AF/AE)



PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test-fixture capacitance

Figure 10. 3-State Outputs (Any Q)

- **Free-Running Read and Write Clocks Can Be Asynchronous or Coincident**
- **Read and Write Operations Synchronized to Independent System Clocks**
- **Input-Ready Flag Synchronized to Write Clock**
- **Output-Ready Flag Synchronized to Read Clock**
- **2048 Words by 9 Bits**
- **Low-Power Advanced CMOS Technology**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Input-Ready, Output-Ready, and Half-Full Flags**
- **Cascadable in Word Width and/or Word Depth**
- **Fast Access Times of 12 ns With a 50-pF Load**
- **Data Rates From 0 to 67 MHz**
- **3-State Outputs**
- **Available in 44-Pin PLCC (FN), Space-Saving 64-Pin Thin Quad Flat Packages (PM), or Reduced-Height 64-Pin Thin Quad Flat Package (PAG)**

description

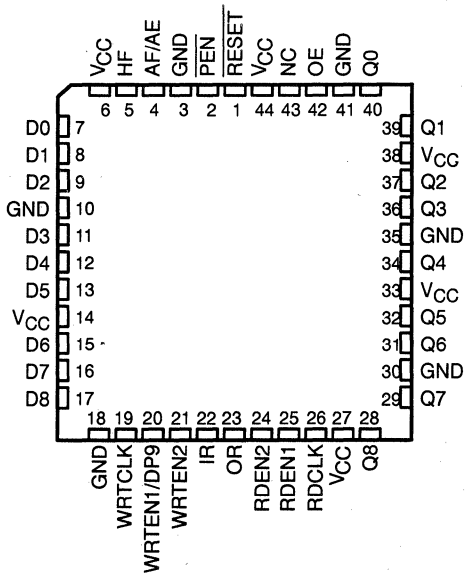
The SN74ACT7807 is a 2048-word by 9-bit FIFO with high speed and fast access times. It processes data at rates up to 67 MHz and access times of 12 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is easily accomplished in both word width and word depth.

The write clock (WRTCLK) and read clock (RDCLK) inputs should be free running and can be asynchronous or coincident. Data is written to memory on the rising edge of WRTCLK when the write-enable (WRTEN1/DP9, WRTEN2) inputs are high and the input-ready (IR) flag output is high. Data is read from memory on the rising edge of RDCLK when the read-enable (RDEN1, RDEN2) and output-enable (OE) inputs are high and the output-ready (OR) flag output is high. The first word written to memory is clocked through to the output buffer regardless of the levels on RDEN1, RDEN2, and OE. The OR flag indicates that valid data is present on the output buffer.

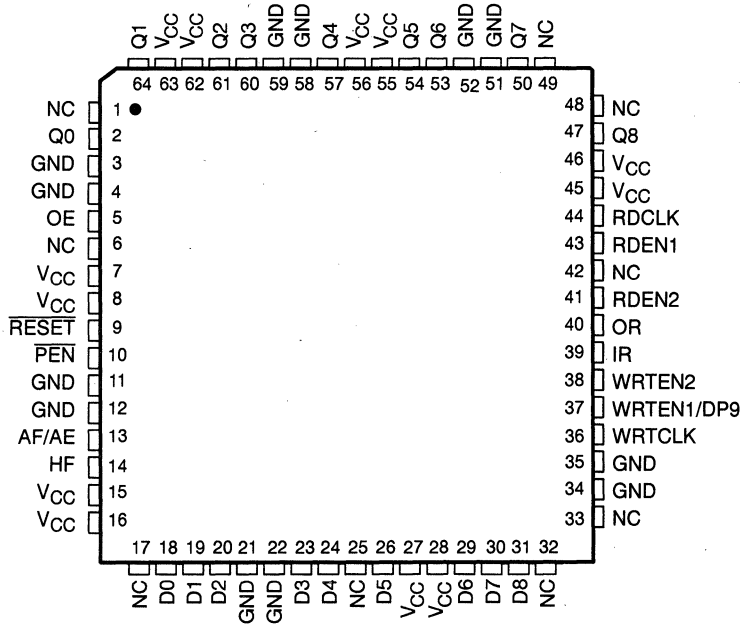
The FIFO can be reset asynchronous to WRTCLK and RDCLK. $\overline{\text{RESET}}$ must be asserted while at least four WRTCLK and four RDCLK cycles occur to clear the synchronizing registers. Resetting the FIFO initializes the IR, OR, and HF flags low and the AF/AE flag high. The FIFO must be reset upon power up.

The SN74ACT7807 is characterized for operation from 0°C to 70°C.

FN PACKAGE
(TOP VIEW)

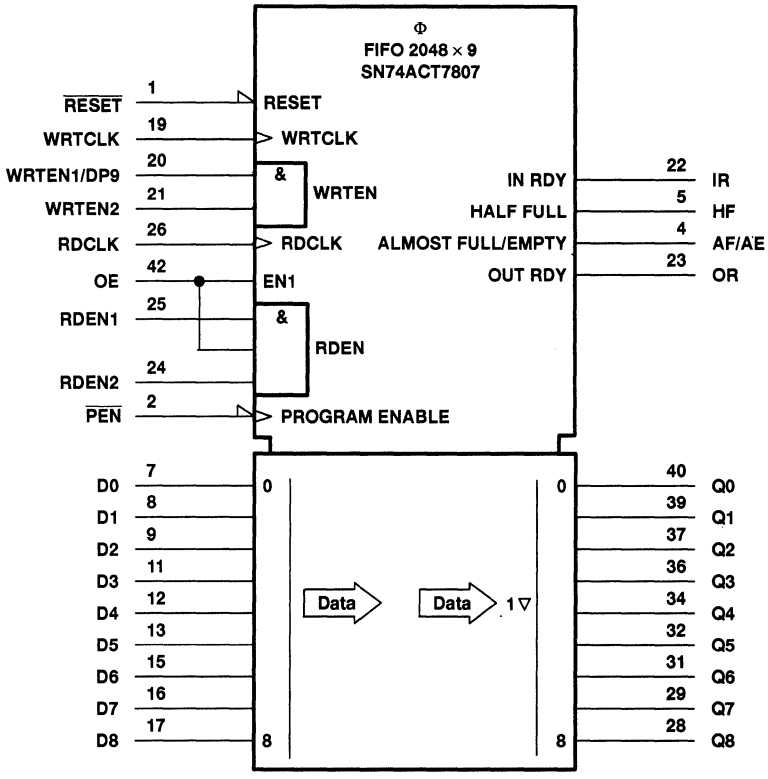


PAG OR PM PACKAGE
(TOP VIEW)



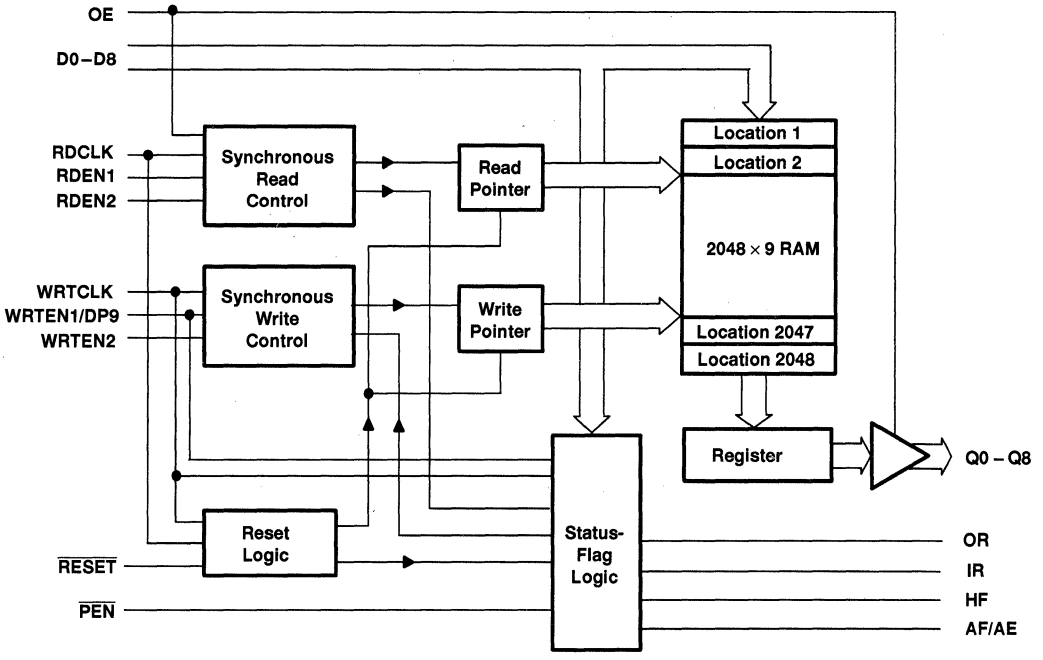
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

functional block diagram



Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
AF/AE	O	Almost-full/almost-empty flag. Depth offset values can be programmed for AF/AE or the default value of 256 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or less words or (2048 – Y) or more words. AF/AE is high after reset.
D0–D8	I	Nine-bit data input port
HF	O	Half-full flag. HF is high when the FIFO memory contains 1024 or more words. HF is low after reset.
IR	O	Input-ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is low during reset and goes high on the second low-to-high transition of WRTCLK after reset.
OE	I	Output enable. When OE, RDEN1, RDEN2 and OR are high, data is read from the FIFO on a low-to-high transition of RDCLK. When OE is low, reads are disabled and the data outputs are in the high-impedance state.
OR	O	Output-ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on Q0–Q17 when OR is high. OR is low during reset and goes high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory.
$\overline{\text{PEN}}$	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D8 and DP9 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and WRTCLK is high.
Q0–Q8	O	Nine-bit data output port. After the first valid write to empty memory, the first word is output on Q0–Q8 on the third rising edge of RDCLK. OR is also asserted high at this time to indicate ready data. When OR is low, the last word read from the FIFO is present on Q0–Q8.
RDCLK	I	Read clock. RDCLK is a continuous clock and can be asynchronous or coincident to WRTCLK. A low-to-high transition of RDCLK reads data from memory when RDEN1, RDEN2, OE, and OR are high. OR is synchronous to the low-to-high transition or RDCLK.
RDEN1, RDEN2	I	Read enables. When RDEN1, RDEN2, OE, and OR are high, data is read from the FIFO on the low-to-high transition of RDCLK.
$\overline{\text{RESET}}$	I	Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{\text{RESET}}$ is low. This sets HF, IR, and OR low and AF/AE high.
WRTCLK	I	Write clock. WRTCLK is a continuous clock and can be asynchronous or coincident to RDCLK. A low-to-high transition of WRTCLK writes data to memory when WRTEN1/DP9, WRTEN2, and IR are high. IR is synchronous to the low-to-high transition of WRTCLK.
WRTEN1/DP9	I	Write enable/data pin 9. When WRTEN1/DP9, WRTEN2, and IR are high, data is written to the FIFO on a low-to-high transition of WRTCLK. When programming an AF/AE offset value, WRTEN1/DP9 is used as the most significant data bit.
WRTEN2	I	Write enable. When WRTEN1/DP9, WRTEN2, and IR are high, data is written to the FIFO on a low-to-high transition of WRTCLK.

offset values for AF/AE

The almost-full/almost-empty flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of X = Y = 256 are used. The AF/AE flag is high when the FIFO contains X or less words or (2048 – Y) or more words.

Program enable ($\overline{PEN}$) should be held high throughout the reset cycle. $\overline{PEN}$ can be brought low only when IR is high and WRTCLK is low. On the following low-to-high transition of WRTCLK, the binary value on D0–D8 and WRTEN1/DP9 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{PEN}$ low for another low-to-high transition of WRTCLK reprograms Y to the binary value on D0–D8 and WRTEN1/DP9 at the time of the second WRTCLK low-to-high transition. While the offsets are programmed, data is not written to the FIFO memory regardless of the state of the write enables (WRTEN1/DP9, WRTEN2). A maximum value of 1023 can be programmed for either X or Y (see Figure 1). To use the default values of X = Y = 256, $\overline{PEN}$ must be held high.

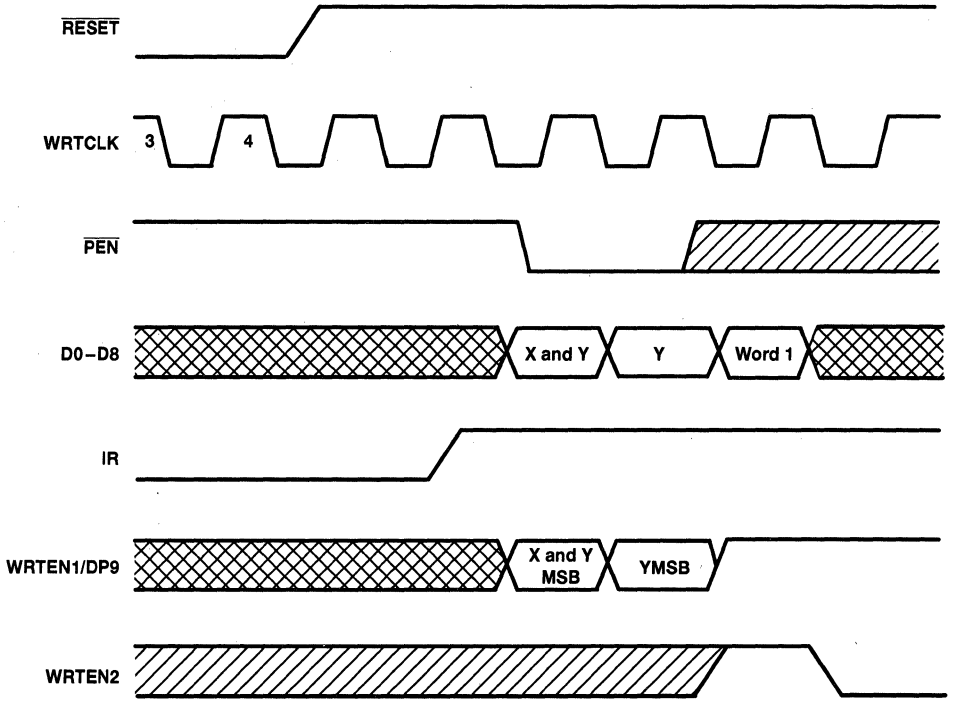


Figure 1. Programming X and Y Separately

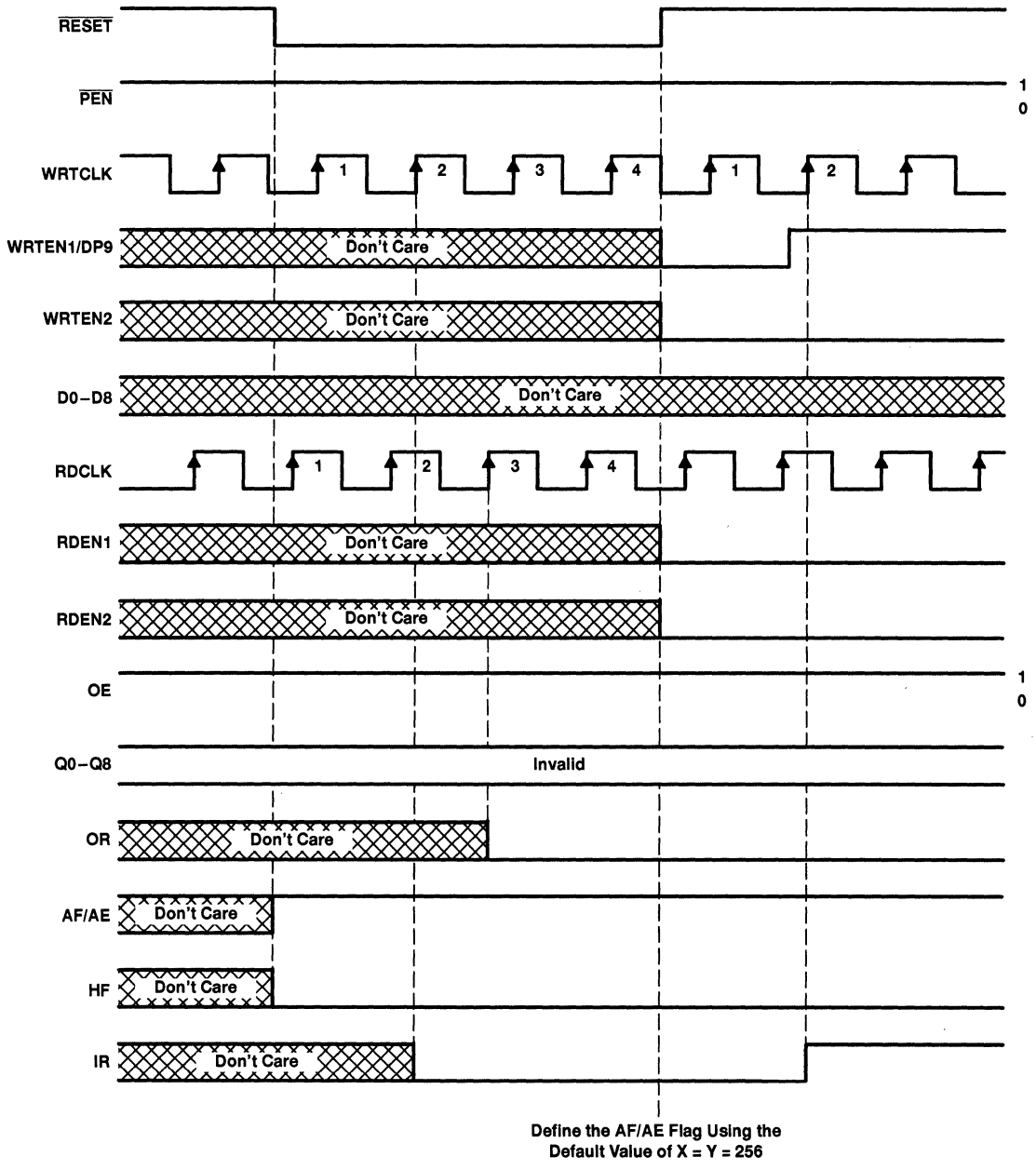


Figure 2. Reset Cycle

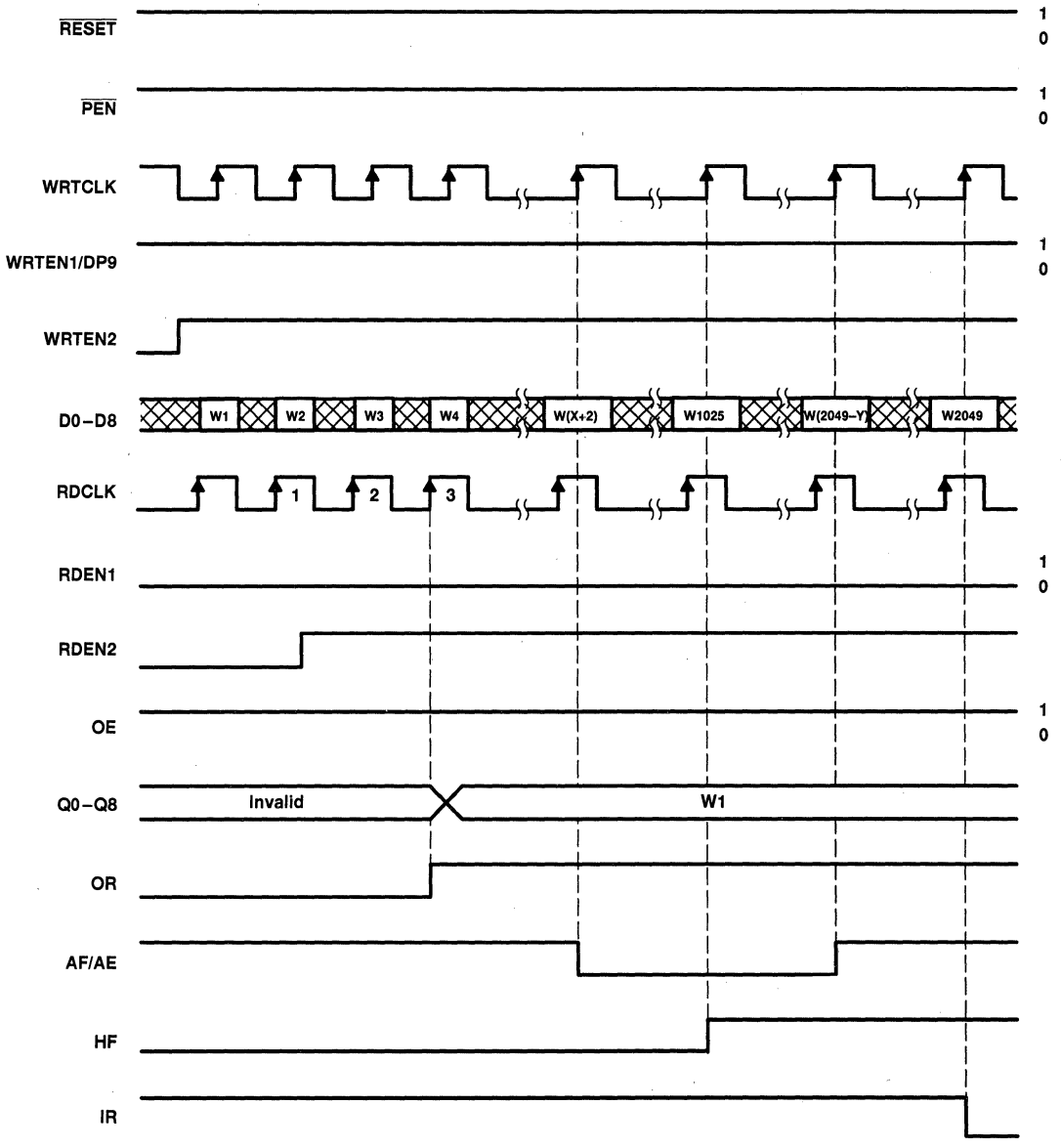


Figure 3. Write Cycle

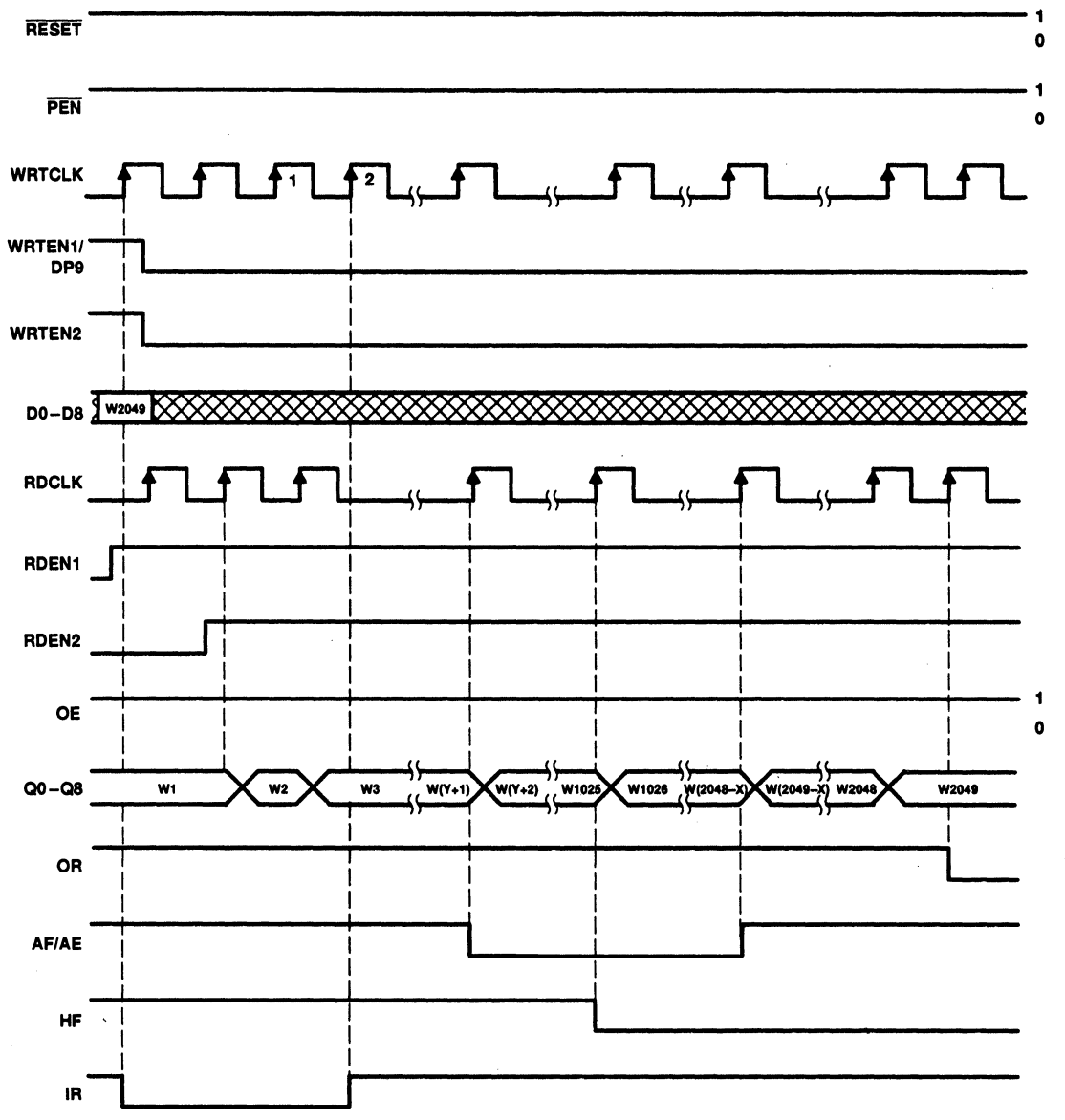


Figure 4. Read Cycle

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage, V_I ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			'ACT7807-15		'ACT7807-20		'ACT7807-25		'ACT7807-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8		0.8		0.8	V
I_{OH}	High-level output current	Q outputs, Flags		−8		−8		−8		−8	mA
I_{OL}	Low-level output current	Q outputs		16		16		16		16	mA
		Flags		8		8		8		8	
f_{clock}	Clock frequency			67		50		40		25	MHz
t_w	Pulse duration	WRTCLK high or low	6		8		9		13		ns
		RDCLK high or low	6		8		9		13		
		$\overline{PEN}$ low	6		9		9		13		
t_{su}	Setup time	D0–D8 before WRTCLK↑	4		5		5		5		ns
		WRTEN1, WRTEN2 before WRTCLK↑	4		5		5		5		
		OE, RDEN1, RDEN2 before RDCLK↑	5		6		6		6.5		
		Reset: $\overline{RESET}$ low before first WRTCLK↑ and RDCLK↑‡	7		8		8		8		
		$\overline{PEN}$ before WRTCLK↑	4		5		5		5		
t_h	Hold time	D0–D8 after WRTCLK↑	0		0		0		0		ns
		WRTEN1, WRTEN2 after WRTCLK↑	0		0		0		0		
		OE, RDEN1, RDEN2 after RDCLK↑	0		0		0		0		
		Reset: $\overline{RESET}$ low after fourth WRTCLK↑ and RDCLK↑‡	5		5		5		5		
		$\overline{PEN}$ high after WRTCLK↓	0		0		0		0		
		$\overline{PEN}$ low after WRTCLK↑	3		3		3		3		
T_A	Operating free-air temperature		0	70	0	70	0	70	0	70	°C

‡ To permit the clock pulse to be utilized for reset purposes

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = – 8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	μA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	μA
I_{CC}		V_{CC} = 5.5 V,	V_I = V_{CC} – 0.2 V or 0				400	μA
ΔI_{CC}‡	WRTEN1/DP9	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2	mA
	Other inputs						1	
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 9 and 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7807-15			'ACT7807-20		'ACT7807-25		'ACT7807-40		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	WRTCLK or RDCLK		67			50		40		25		MHz
t_{pd}	RDCLK↑	Any Q	3	9	12	3	13	3	18	3	25	ns
t_{pd}§				8								
t_{pd}	WRTCLK↑	IR	1		9	1	12	1	14	1	16	ns
t_{pd}	RDCLK↑	OR	1		9	2	12	2	14	2	16	ns
t_{pd}	WRTCLK↑	AF/AE	2		16	2	20	2	25	2	30	ns
	RDCLK↑		2		17	2	20	2	25	2	30	
t_{PLH}	WRTCLK↑	HF	2		19	2	21	2	23	2	25	ns
t_{PHL}	RDCLK↑		2		16	2	18	2	20	2	22	
t_{PLH}	$\overline{\text{RESET}}$ low	AF/AE	1		12	1	18	1	22	1	24	ns
t_{PHL}		HF	2		12	2	18	2	22	2	24	
t_{en}	OE	Any Q	2		10	2	13	2	15	2	18	ns
t_{dis}			1		11	1	13	1	15	1	18	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the supply current for each input that is at one of the specified TTL voltage levels rather 0 V or V_{CC}.
§ This parameter is measured with C_L = 30 pF (see Figure 5).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per FIFO channel	Outputs enabled	C_L = 50 pF, f = 5 MHz	91	pF

TYPICAL CHARACTERISTICS

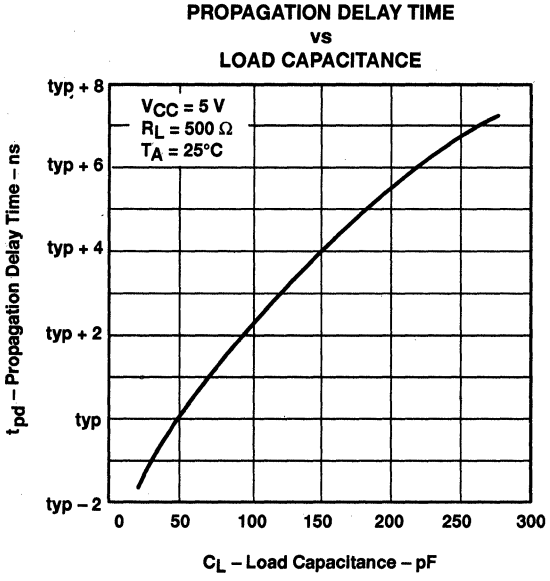


Figure 5

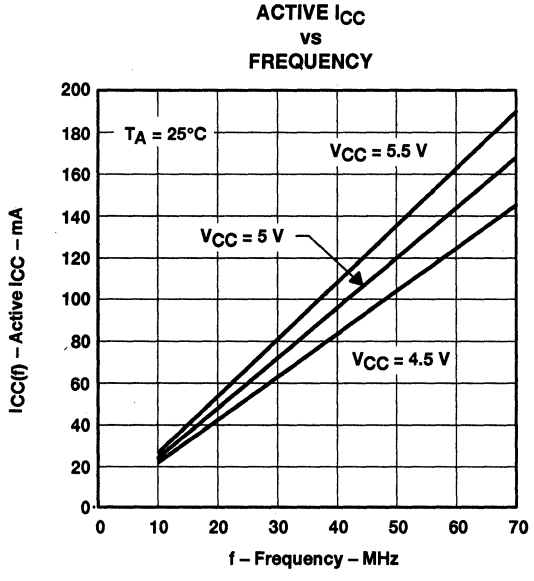


Figure 6

TYPICAL CHARACTERISTICS

calculating power dissipation

With $I_{CC(f)}$ taken from Figure 6, the maximum power dissipation (P_T) of the SN74ACT7807 can be calculated using:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_L \times V_{CC}^2 \times f_o)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma (C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC} = power-down I_{CC} maximum
N = number of inputs driven by a TTL device
ΔI_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitive load
f_i = data input frequency
f_o = data output frequency

APPLICATION INFORMATION

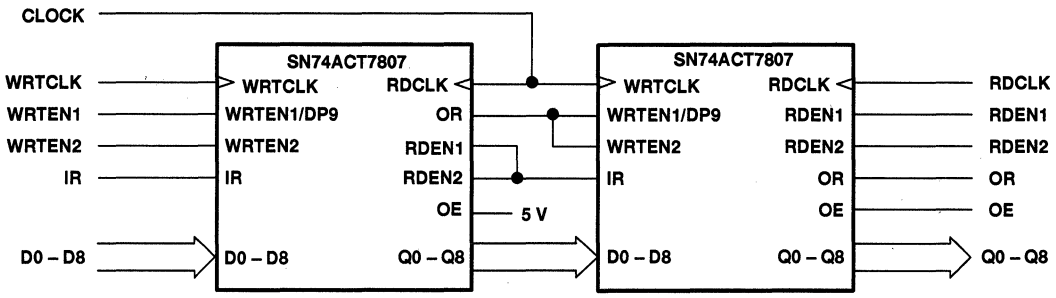


Figure 7. Word-Depth Expansion: 4096 Words by 9 Bits

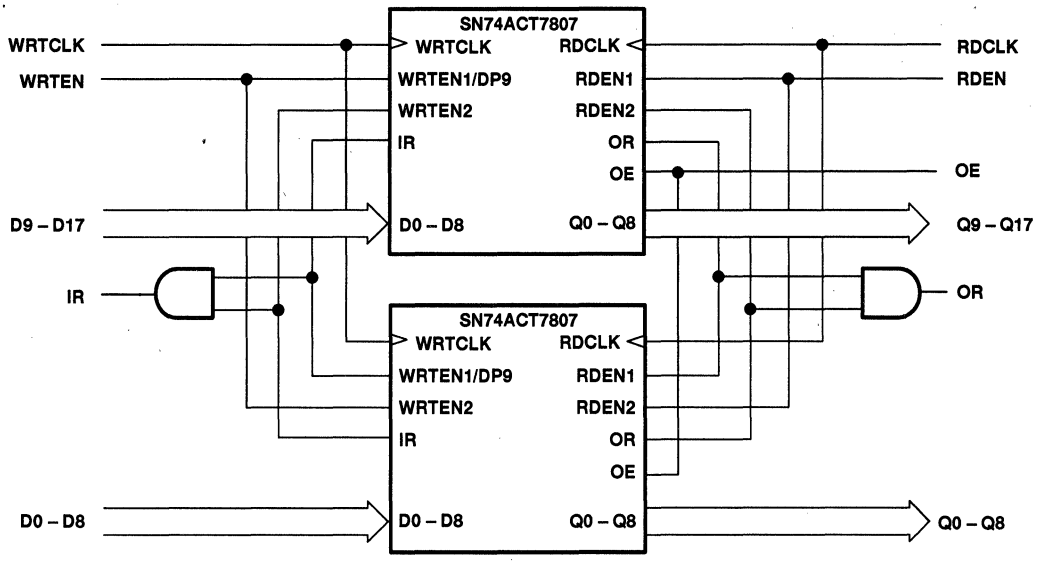


Figure 8. Word-Width Expansion: 2048 Words by 18 Bits

PARAMETER MEASUREMENT INFORMATION

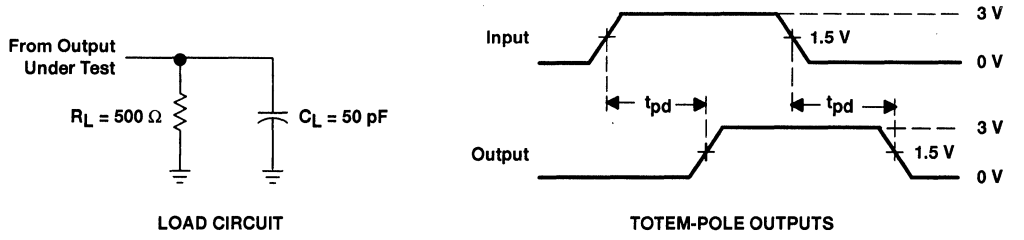
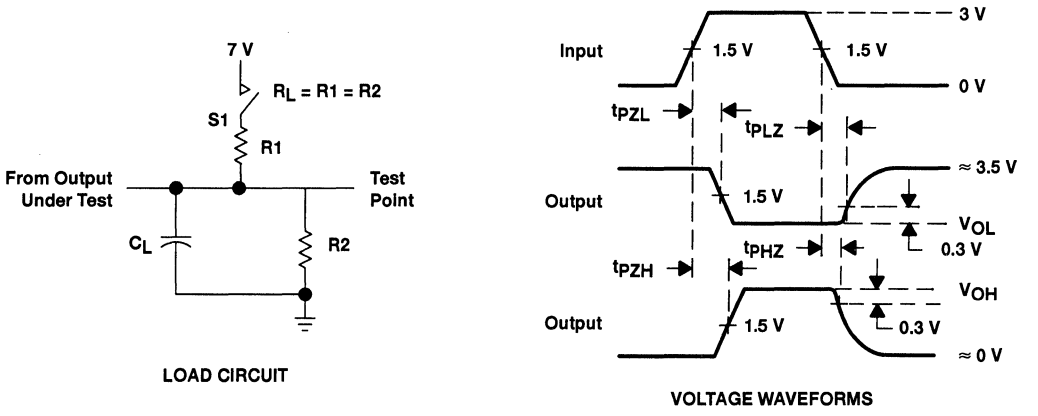


Figure 9. Standard CMOS Outputs (IR, OR, HF, AF/AE)



PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test fixture capacitance

Figure 10. 3-State Outputs (Any Q)

SCAS205A – FEBRUARY 1991 – REVISED AUGUST 1994

- **Load Clocks and Unload Clocks Can Be Asynchronous or Coincident**
- **2048 Words by 9 Bits**
- **Low-Power Advanced CMOS Technology**
- **Fast Access Times of 15 ns With a 50-pF Load**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Expansion Logic for Depth Cascading**
- **Empty, Full, and Half-Full Flags**
- **Fall-Through Time of 20 ns Typ**
- **Data Rates From 0 to 50 MHz**
- **3-State Outputs**
- **Available in 44-Pin PLCC (FN), Space-Saving 64-Pin Thin Quad Flat Packages (PM), or Reduced-Height 64-Pin Quad Flat Package (PAG)**

description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7808 is a 2048-word by 9-bit FIFO designed for high speed and fast access times. It processes data at rates up to 50 MHz and access times of 15 ns in a bit-parallel format.

Data is written into memory on a low-to-high transition at the load clock (LDCK) input and is read out on a low-to-high transition at the unload clock (UNCK) input. The memory is full when the number of words clocked in exceeds the number of words clocked out by 2048. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the full ($\overline{\text{FULL}}$), empty ($\overline{\text{EMPTY}}$), half-full (HF), and almost-full/almost-empty (AF/AE) flags. The $\overline{\text{FULL}}$ output is low when the memory is full and high when the memory is not full. The $\overline{\text{EMPTY}}$ output is low when the memory is empty and high when it is not empty. The HF output is high whenever the FIFO contains 1024 or more words and is low when it contains 1023 or less words. The AF/AE status flag is a programmable flag. The first one or two low-to-high transitions of LDCK after reset can be used to program the almost-empty offset value (X) and the almost-full offset value (Y) if program enable ($\overline{\text{PEN}}$) is low. The AF/AE flag is high when the FIFO contains X or less words or (2048 – Y) or more words. The AF/AE flag is low when the FIFO contains between (X + 1) and (2047 – Y) words.

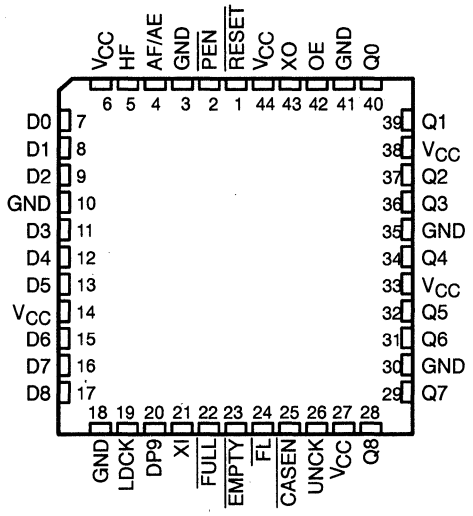
A low level on the reset ($\overline{\text{RESET}}$) input resets the internal stack pointers and sets $\overline{\text{FULL}}$ high, AF/AE high, HF low, and $\overline{\text{EMPTY}}$ low. The Q outputs are not reset to any specific logic level. The FIFO must be reset upon power up.

The first word loaded into empty memory causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are in the high-impedance state when the output-enable (OE) input is low. OE does not affect the output flags.

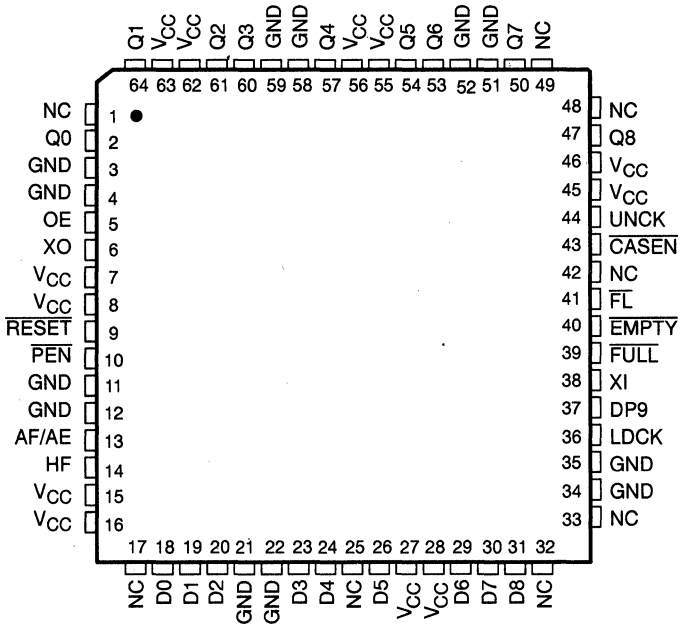
Cascading is easily accomplished in the word-width and word-depth directions. When not using the FIFO in depth expansion, cascade enable ($\overline{\text{CASEN}}$) must be tied high.

The SN74ACT7808 is characterized for operation from 0°C to 70°C.

FN PACKAGE
(TOP VIEW)

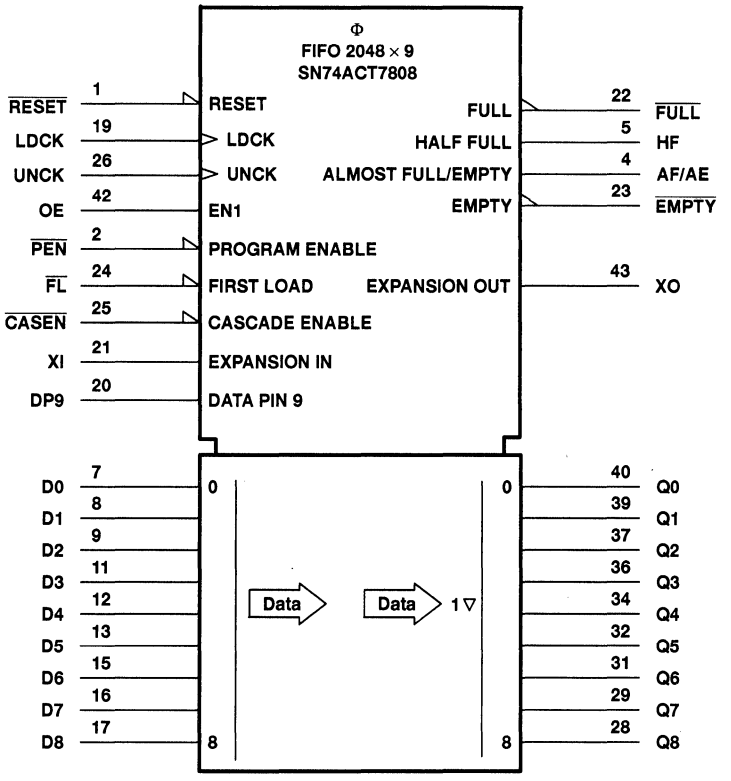


PAG OR PM PACKAGE
(TOP VIEW)



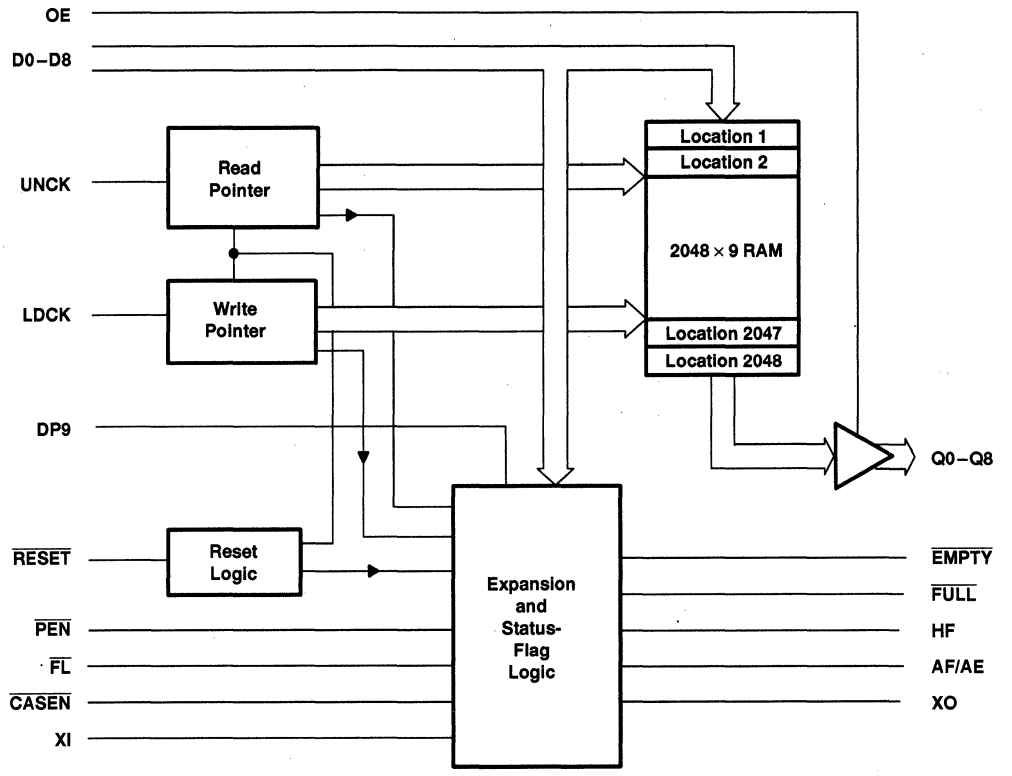
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

functional block diagram



Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
AF/AE	O	Almost-full/almost-empty flag. Depth offset values can be programmed for this AF/AE or the default value of 256 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or less words or (2048 – Y) or more words. AF/AE is high after reset.
$\overline{\text{CASEN}}$†	I	Cascade enable. When multiple SN74ACT7808 devices are depth cascaded, every device must have $\overline{\text{CASEN}}$ tied low. $\overline{\text{CASEN}}$ must be tied high when a device is not used in depth expansion.
D0–D8	I	Nine-bit data input port
DP9	I	DP9 is used as the most significant bit when programming the AF/AE offset values.
$\overline{\text{EMPTY}}$	O	Empty flag. $\overline{\text{EMPTY}}$ is low when the FIFO memory is empty. A FIFO reset also causes $\overline{\text{EMPTY}}$ to go low.
$\overline{\text{FL}}$†	I	When multiple SN74ACT7808 devices are depth cascaded, the first device in the chain must have its $\overline{\text{FL}}$ input tied low and all other devices must have their $\overline{\text{FL}}$ inputs tied high.
$\overline{\text{FULL}}$	O	Full flag. $\overline{\text{FULL}}$ is low when the FIFO is full. A FIFO reset causes $\overline{\text{FULL}}$ to go high.
HF	O	Half-full flag. HF is high when the FIFO memory contains 1024 or more words. HF is low after reset.
LDCK	I	Load clock. Data is written to the FIFO on the rising edge of LDCK when $\overline{\text{FULL}}$ is high.
OE	I	Output enable. When OE is low, D0–D8 are in the high-impedance state.
$\overline{\text{PEN}}$	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D8 and DP9 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and LDCK is high.
Q0–Q8	O	Nine-bit data output port
$\overline{\text{RESET}}$	I	Reset. A low level on $\overline{\text{RESET}}$ resets the FIFO and drives $\overline{\text{FULL}}$ and AF/AE high and HF and $\overline{\text{EMPTY}}$ low.
UNCK	I	Unload clock. Data is read from the FIFO on the rising edge of UNCK when $\overline{\text{EMPTY}}$ is high.
XI†	I	Expansion input (XI) and expansion output (XO). When multiple SN74ACT7808 devices are depth cascaded, the XO of one device must be connected to the XI of the next device in the chain. The XO of the last device in the chain is connected to the XI of the first device in the chain.
XO†	O	

† See Figures 4 and 5 for application information on FIFO word-width and word-depth expansions, respectively.

offset values for AF/AE

The almost-full/almost-empty flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of X = Y = 256 are used. The AF/AE flag is high when the FIFO contains X or less words or (2048 – Y) or more words.

To program the offset values, $\overline{PEN}$ can be brought low after reset only when LDCK is low. On the following low-to-high transition of LDCK, the binary value on D0–D8 and DP9 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{PEN}$ low for another low-to-high transition of LDCK reprograms Y to the binary value on D0–D8 and DP9 at the time of the second LDCK low-to-high transition. Writes to the FIFO memory are disabled while the offsets are programmed. A maximum value of 1023 can be programmed for either X or Y (see Figure 1). To use the default values of X = Y = 256, $\overline{PEN}$ must be held high.

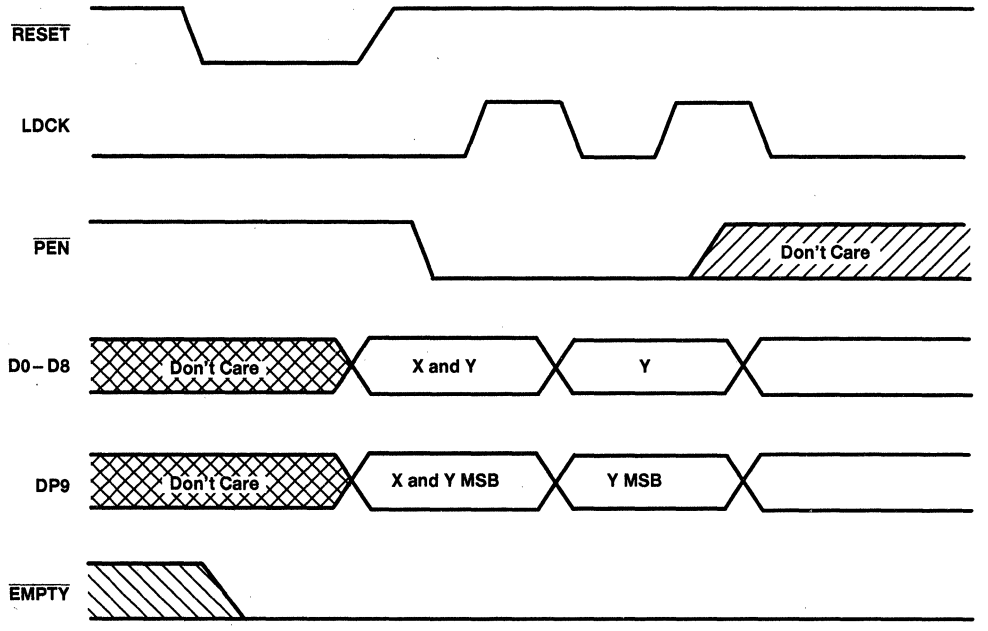


Figure 1. Programming X and Y Separately

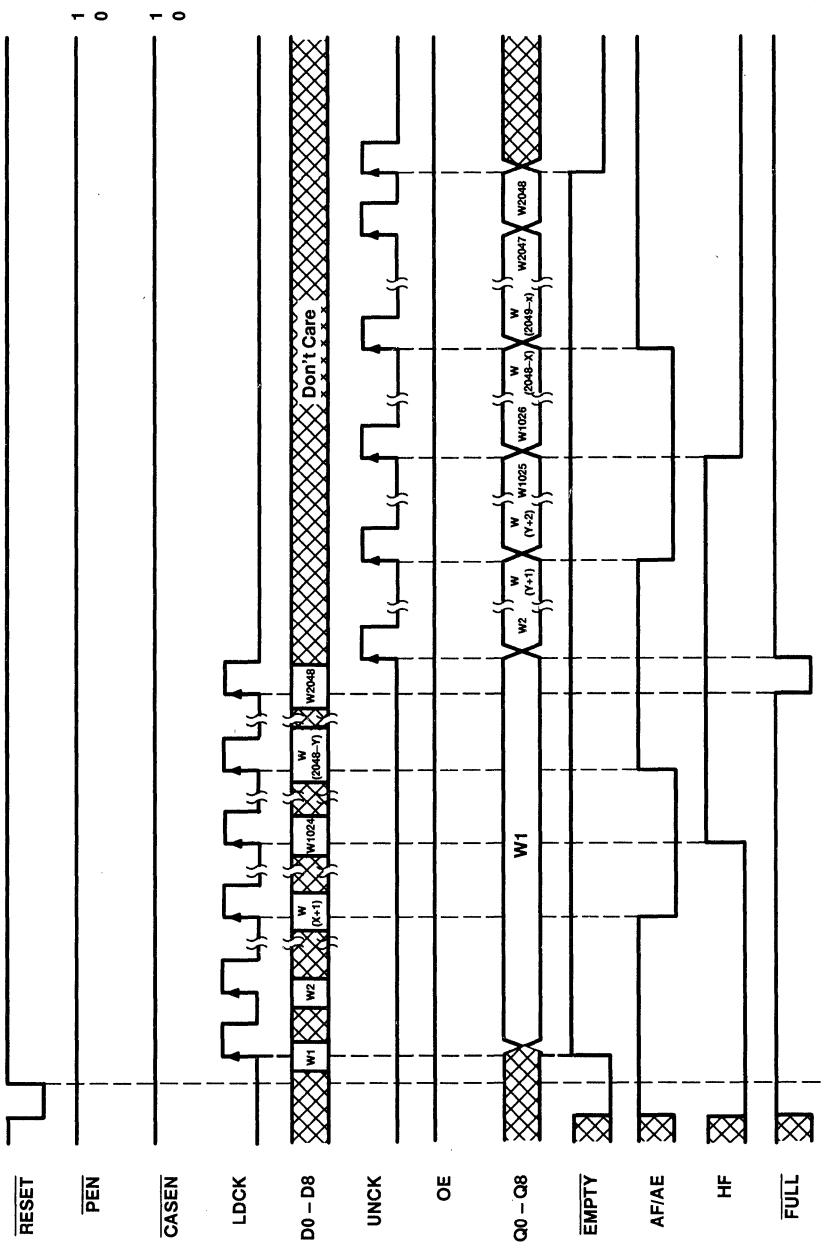


Figure 2. Read

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage, V_I ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			'ACT7808-20		'ACT7808-25		'ACT7808-30		'ACT7808-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	XI	3.85		3.85		3.85		3.85		V
		Other inputs	2		2		2		2		
V_{IL}	Low-level input voltage			0.8		0.8		0.8		0.8	V
I_{OH}	High-level output current			−8		−8		−8		−8	mA
I_{OL}	Low-level output current	Q outputs		16		16		16		16	mA
		Flags		8		8		8		8	
f_{clock}	Clock frequency			50		40		33.3		25	MHz
t_w	Pulse duration	LDCK high or low	8		9		11		13		ns
		UNCK high or low	8		9		11		13		
		$\overline{PEN}$ low	9		9		11		13		
		$\overline{RESET}$ low	10		13		16		19		
t_{su}	Setup time	D0 – D8, DP9 before LDCK↑	5		5		5		5		ns
		LDCK inactive before $\overline{RESET}$ high	5		5		5		5		
		$\overline{PEN}$ before LDCK↑	5		5		5		5		
t_h	Hold time	D0–D8, DP9 after LDCK↑	0		0		0		0		ns
		LDCK inactive after $\overline{RESET}$ high	5		5		5		5		
		$\overline{PEN}$ low after LDCK↑	4		4		4		4		
		$\overline{PEN}$ high after LDCK low	0		0		0		0		
T_A	Operating free-air temperature		0	70	0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = – 8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	µA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	µA
I_{CC}		V_{CC} = 5.5 V,	V_I = V_{CC} – 0.2 V or 0				400	µA
ΔI_{CC}‡		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 7 and 8)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7808-20			'ACT7808-25		'ACT7808-30		'ACT7808-40		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK or UNCK		50			40		33.3		25		MHz
t_{pd}	LDCK↑	Any Q	5		20	5	22	5	25	5	28	ns
	UNCK↑		4.5	11	15	4.5	18	4.5	20	4.5	22	
t_{pd}§				10								
t_{PLH}	LDCK↑	$\overline{EMPTY}$	4		15	4	17	4	19	4	21	ns
t_{PHL}	UNCK↑		2		15	2	17	2	19	2	21	
	$\overline{RESET}$ low		2		16	2	18	2	20	2	22	
t_{PHL}	LDCK↑	$\overline{FULL}$	4		15	4	17	4	19	4	21	ns
t_{PLH}	UNCK↑		4		14	4	16	4	18	4	20	
	$\overline{RESET}$ low		2		18	2	20	2	22	2	24	
t_{pd}	LDCK↑	AF/AE	2		16	2	18	2	20	2	22	ns
	UNCK↑		2		16	2	18	2	20	2	22	
t_{PLH}	$\overline{RESET}$ low		0		10	0	12	0	14	0	16	
t_{PLH}	LDCK↑	HF	2		19	2	21	2	23	2	25	ns
t_{PHL}	UNCK↑		2		16	2	18	2	20	2	22	
	$\overline{RESET}$ low		2		12	2	14	2	16	2	18	
t_{PLH}	UNCK↑	XO	2		11	2	13	2	15	2	17	ns
t_{PHL}	LDCK↑		2		11	2	13	2	15	2	17	
t_{en}	OE	Any Q	1		10	1	12	1	14	1	16	ns
t_{dis}			1		9	1	11	1	13	1	15	
t_{en}	XI high	Any Q	3		13	3	15	3	17	3	19	ns
t_{dis}	XO high				4		4		4		4	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input, excluding XI, that is at one of the specified TTL voltage levels rather 0 V or V_{CC}.
§ This parameter is measured with C_L = 30 pF (see Figure 3).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per FIFO channel	Outputs enabled	C_L = 50 pF, f = 5 MHz	91	pF

TYPICAL CHARACTERISTICS

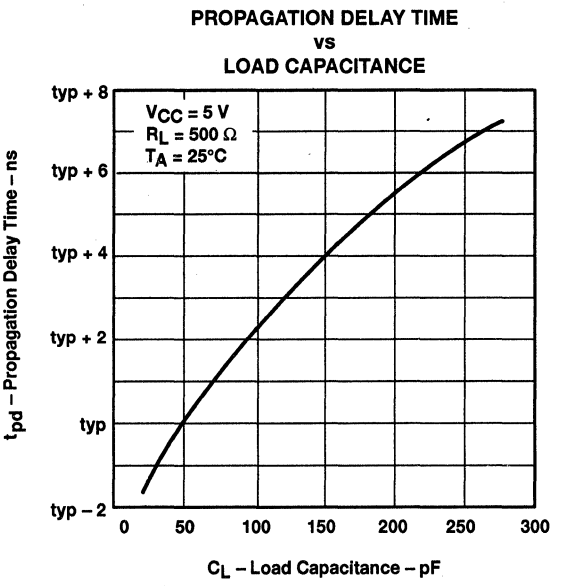


Figure 3

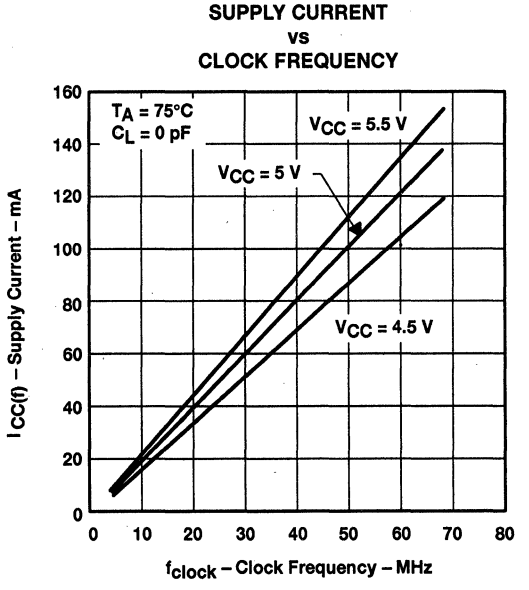


Figure 4

TYPICAL CHARACTERISTICS

calculating power dissipation

With $I_{CC(f)}$ taken from Figure 4, the maximum power dissipation (P_T) of the SN74ACT7808 can be calculated using:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_L \times V_{CC}^2 \times f_o)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma (C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC} = power-down I_{CC} maximum
N = number of inputs driven by a TTL device
ΔI_{CC} = increase in supply current
dc = duty cycle of inputs at a TTL high level of 3.4 V
C_{pd} = power dissipation capacitance
C_L = output capacitive load
f_i = data input frequency
f_o = data output frequency

APPLICATION INFORMATION

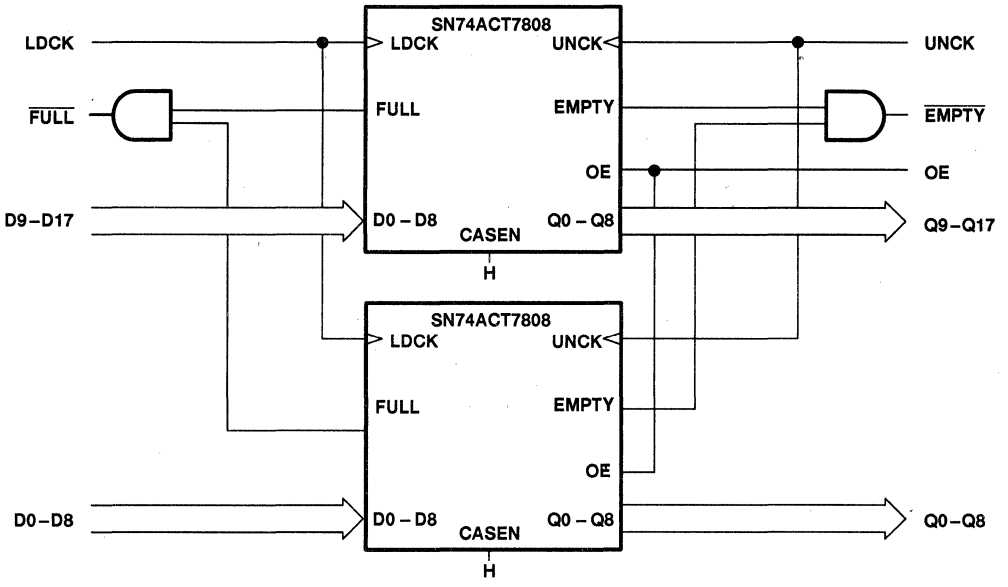


Figure 5. Word-Width Expansion: 2048 Words by 18 Bits

depth cascading (see Figure 6)

The SN74ACT7808 provides expansion logic necessary for cascading an unlimited number of the FIFOs in depth. $\overline{\text{CASEN}}$ must be low on all FIFOs used in depth expansion. $\overline{\text{FL}}$ must be tied low on the first FIFO in the chain; all others must have $\overline{\text{FL}}$ tied high. The expansion-out (XO) output of a FIFO must be tied to the expansion-in (XI) input of the next FIFO in the chain. The XO output of the last FIFO is tied to the XI input of the first FIFO to complete the loop. Data buses are common to each FIFO in the chain. A composite $\overline{\text{EMPTY}}$ and $\overline{\text{FULL}}$ signal must be generated to indicate boundary conditions.

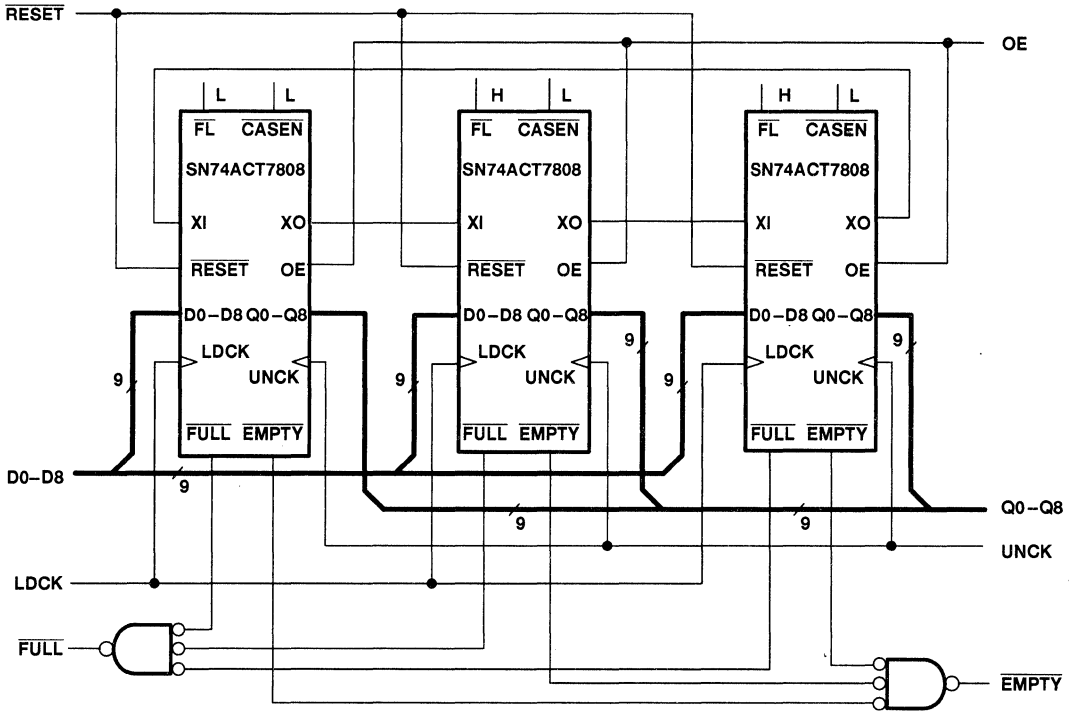


Figure 6. Depth Cascading to Form a 6K × 9 FIFO

PARAMETER MEASUREMENT INFORMATION

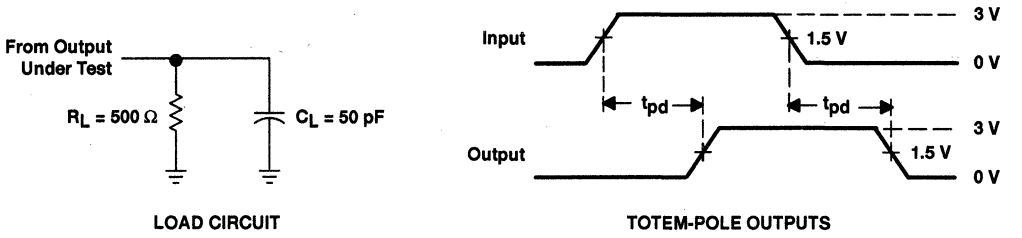
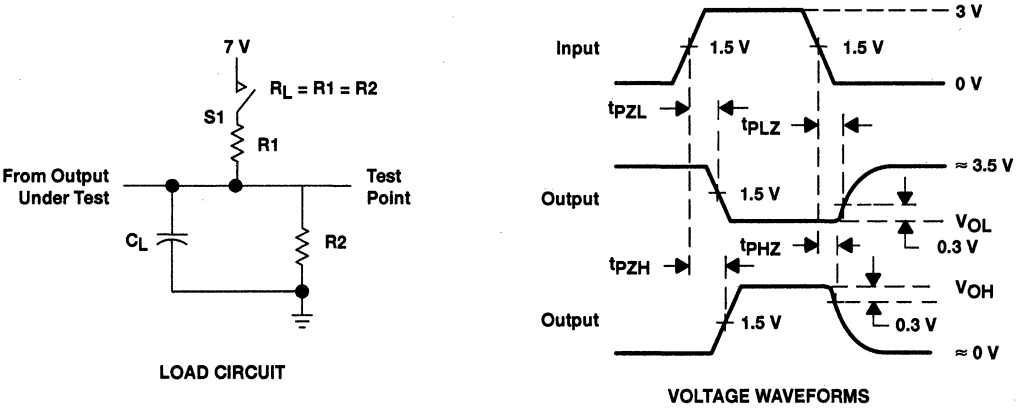


Figure 7. Standard CMOS Outputs (XO, $\overline{\text{EMPTY}}$, $\overline{\text{FULL}}$, AF/AE, HF)



PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

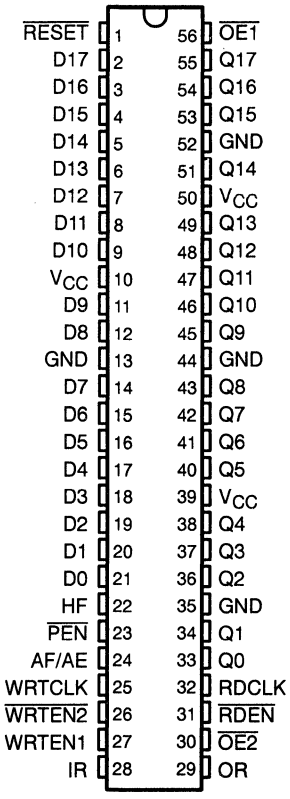
† Includes probe and test fixture capacitance

Figure 8. 3-State Outputs (Any Q)

SCAS199 – JANUARY 1991 – REVISED APRIL 1992

- **Member of the Texas Instruments Widebus™ Family**
- **Free-Running Read and Write Clocks Can Be Asynchronous or Coincident**
- **Read and Write Operations Synchronized to Independent System Clocks**
- **Input-Ready Flag Synchronized to Write Clock**
- **Output-Ready Flag Synchronized to Read Clock**
- **64 Words by 18 Bits**
- **Low-Power Advanced CMOS Technology**
- **Half-Full Flag and Programmable Almost-Full/Almost-Empty Flag**
- **Bidirectional Configuration and Width Expansion Without Additional Logic**
- **Fast Access Times of 12 ns With a 50-pF Load and All Data Outputs Switching Simultaneously**
- **Data Rates From 0 to 67 MHz**
- **Pin Compatible With SN74ACT7803 and SN74ACT7805**
- **Packaged in Shrink Small-Outline 300-mil Package (DL) Using 25-mil Center-to-Center Spacing**

DL PACKAGE
(TOP VIEW)



description

The SN74ACT7813 is a 64-word × 18-bit FIFO suited for buffering asynchronous data paths at 67-MHz clock rates and 12-ns access times. Its 56-pin shrink small-outline package (DL) offers greatly reduced board space over DIP, PLCC, and conventional SOIC packages. Two devices can be configured for bidirectional data buffering without additional logic. Multiple distributed V_{CC} and GND pins along with TI's patented output edge control (OEC™) circuit dampen simultaneous switching noise.

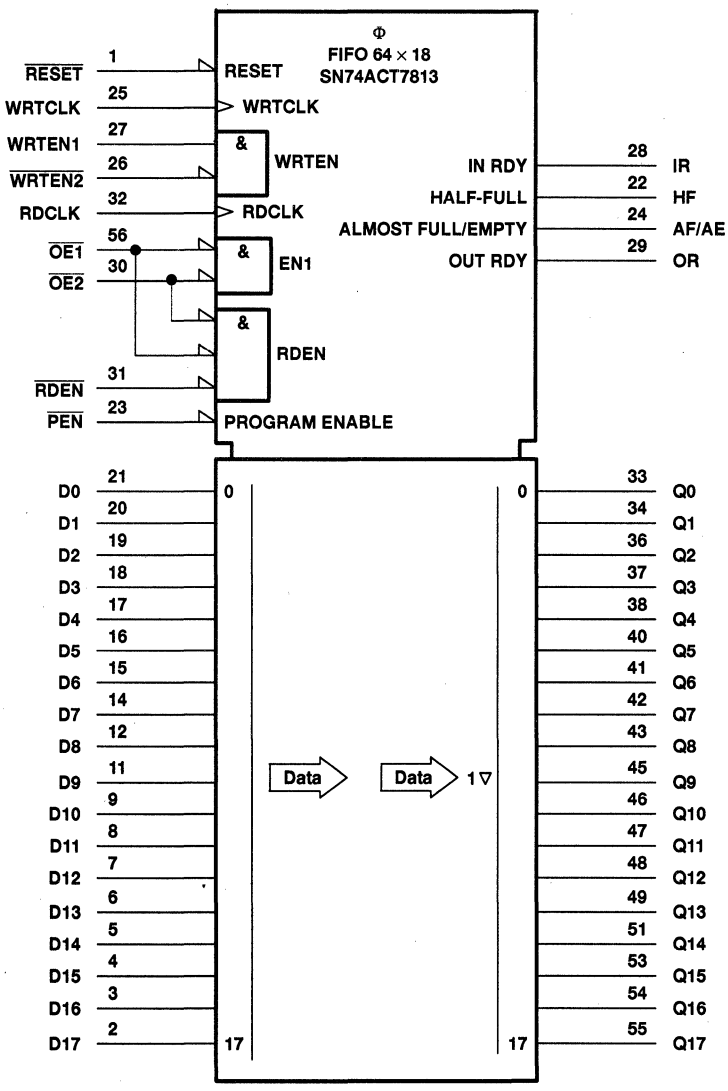
The write clock (WRTCLK) and read clock (RDCLK) should be free running and can be asynchronous or coincident. Data is written to memory on the rising edge of WRTCLK when $\overline{\text{WRTEN1}}$ is high, $\overline{\text{WRTEN2}}$ is low, and IR is high. Data is read from memory on the rising edge of RDCLK when $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ are low and $\overline{\text{OR}}$ is high. The first word written to memory is clocked through to the output buffer regardless of the $\overline{\text{RDEN}}$, $\overline{\text{OE1}}$, and $\overline{\text{OE2}}$ levels. The $\overline{\text{OR}}$ flag indicates that valid data is present on the output buffer.

The FIFO can be reset asynchronously to WRTCLK and RDCLK. $\overline{\text{RESET}}$ must be asserted while at least four WRTCLK and four RDCLK rising edges occur to clear the synchronizing registers. Resetting the FIFO initializes the IR, $\overline{\text{OR}}$, and HF flags low and the AF/AE flag high. The FIFO must be reset upon power up.

The SN74ACT7813 is characterized for operation from 0°C to 70°C.

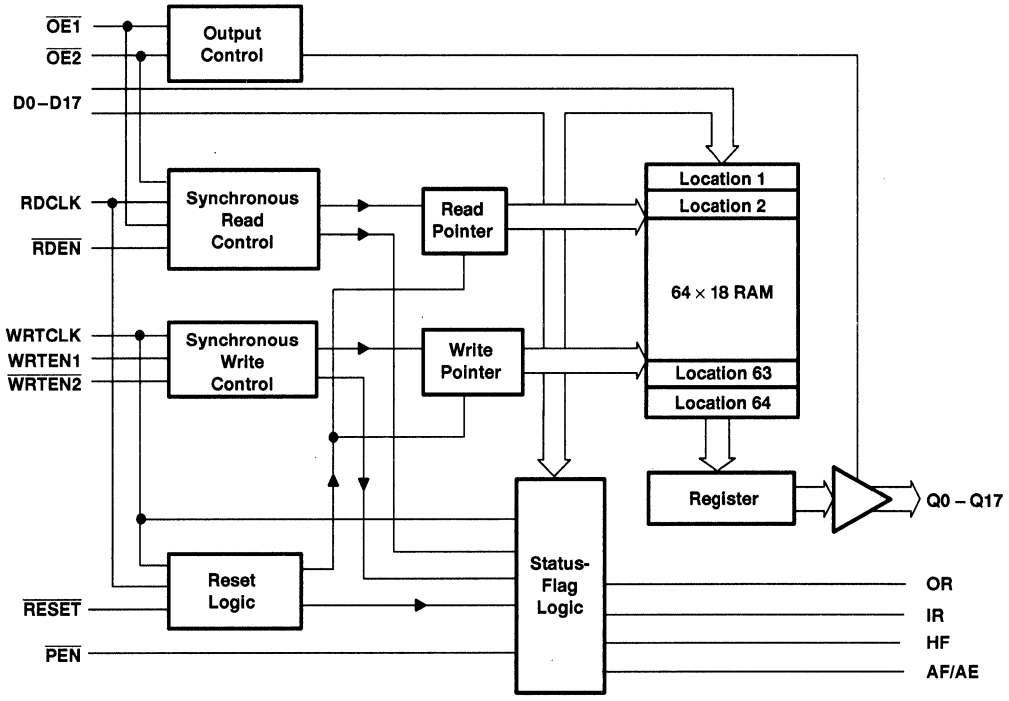
Widebus and OEC are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AE	24	O	Almost-full/almost-empty flag. Depth offset values can be programmed for AF/AE, or the default value of 8 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or less words or (64 – Y) or more words. AF/AE is high after reset.
D0–D17	21–14, 12–11, 9–2	I	The 18-bit data input port
HF	22	O	Half-full flag. HF is high when the FIFO memory contains 32 or more words. HF is low after reset.
IR	28	O	Input-ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is low during reset and goes high on the second low-to-high transition of WRTCLK after reset.
$\overline{OE1}$, $\overline{OE2}$	56, 30	I	Output enables. When $\overline{OE1}$, $\overline{OE2}$, and $\overline{RDEN}$ are low and OR is high, data is read from the FIFO on a low-to-high transition of RDCLK. When either $\overline{OE1}$ or $\overline{OE2}$ is high, reads are disabled and the data outputs are in the high-impedance state.
OR	29	O	Output-ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on Q0–Q17 when OR is high. OR is low during reset and goes high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory.
$\overline{PEN}$	23	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D4 is latched as an AF/AE offset value when $\overline{PEN}$ is low and WRTCLK is high.
Q0–Q17	33–34, 36–38, 40–43, 45–49, 51, 53–55	O	The 18-bit data output port. After the first valid write to empty memory, the first word is output on Q0–Q17 on the third rising edge of RDCLK. OR is also asserted high at this time to indicate ready data. When OR is low, the last word read from the FIFO is present on Q0–Q17.
RDCLK	32	I	Read clock. RDCLK is a continuous clock and can be asynchronous or coincident to WRTCLK. A low-to-high transition of RDCLK reads data from memory when $\overline{OE1}$, $\overline{OE2}$, and $\overline{RDEN}$ are low and OR is high. OR is synchronous to the low-to-high transition or RDCLK.
$\overline{RDEN}$	31	I	Read enable. When $\overline{RDEN}$, $\overline{OE1}$, and $\overline{OE2}$ are low and OR is high, data is read from the FIFO on the low-to-high transition of RDCLK.
$\overline{RESET}$	1	I	Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while $\overline{RESET}$ is low. This sets HF, IR, and OR low and AF/AE high.
WRTCLK	25	I	Write clock. WRTCLK is a continuous clock and can be asynchronous or coincident to RDCLK. A low-to-high transition of WRTCLK writes data to memory when $\overline{WRTEN2}$ is low, WRTEN1 is high, and IR is high. IR is synchronous to the low-to-high transition of WRTCLK.
WRTEN1, $\overline{WRTEN2}$	27, 26	I	Write enables. When WRTEN1 is high, $\overline{WRTEN2}$ is low, and IR is high, data is written to the FIFO on a low-to-high transition of WRTCLK.

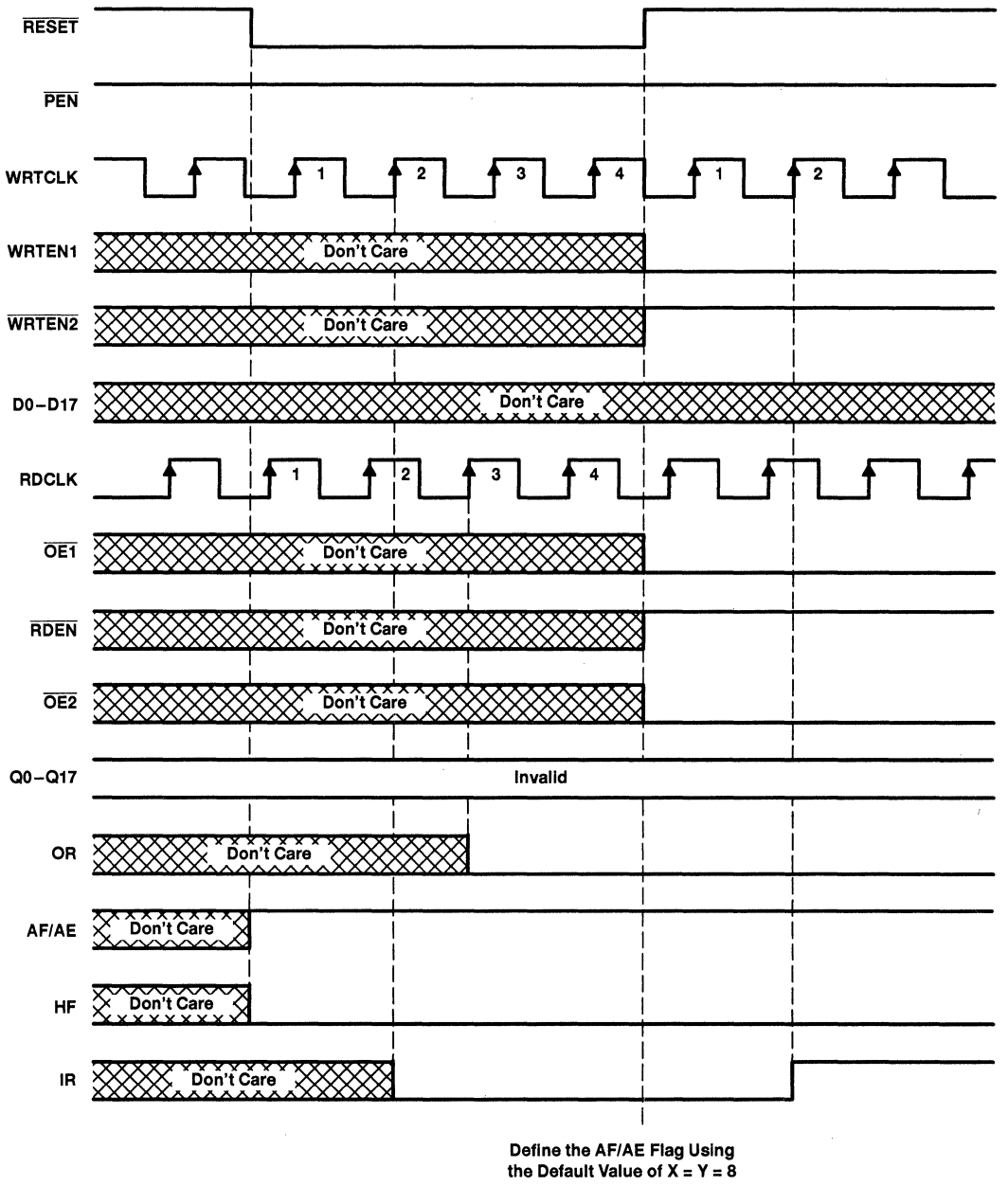


Figure 1. Reset Cycle

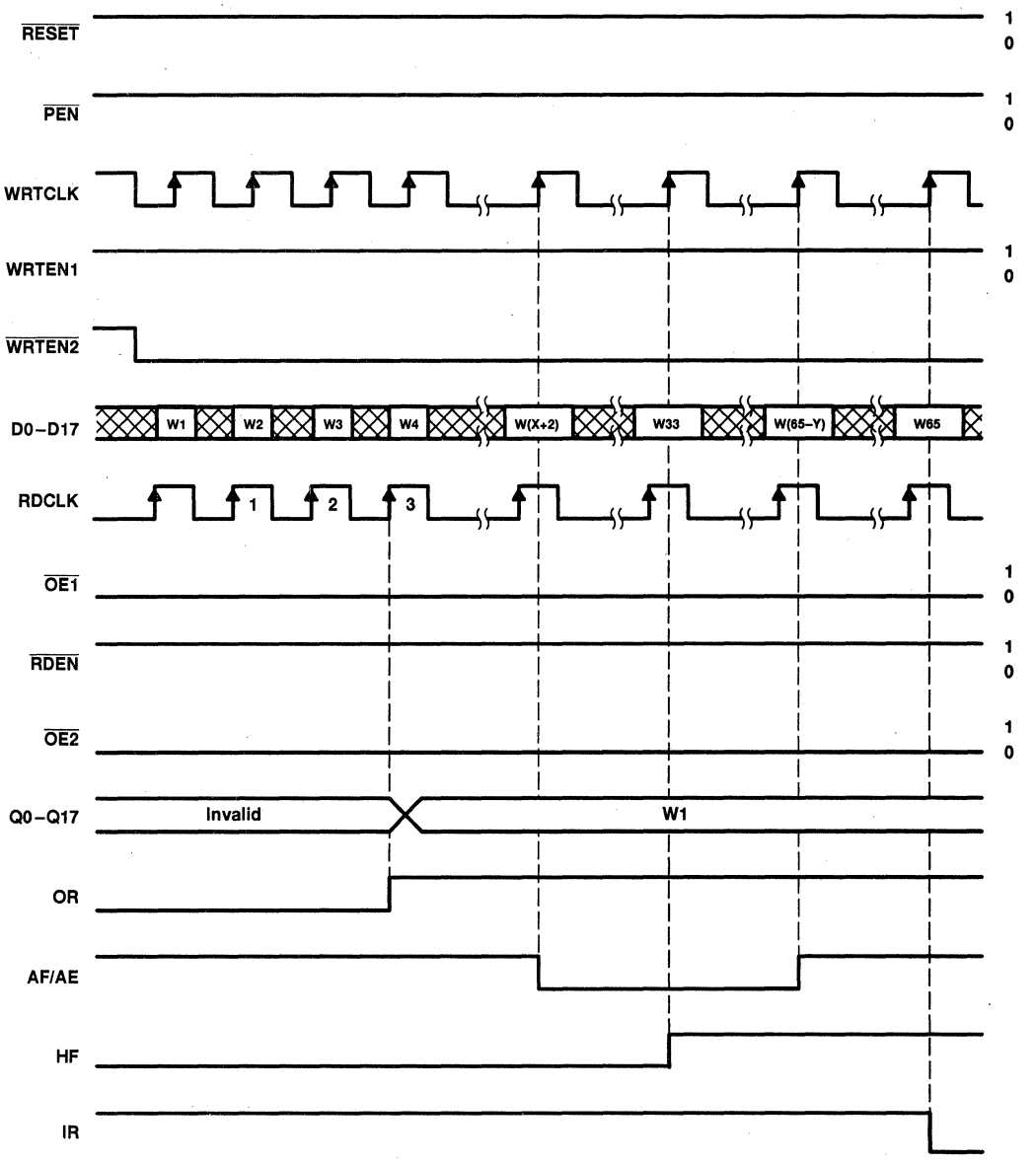


Figure 2. Write Cycle

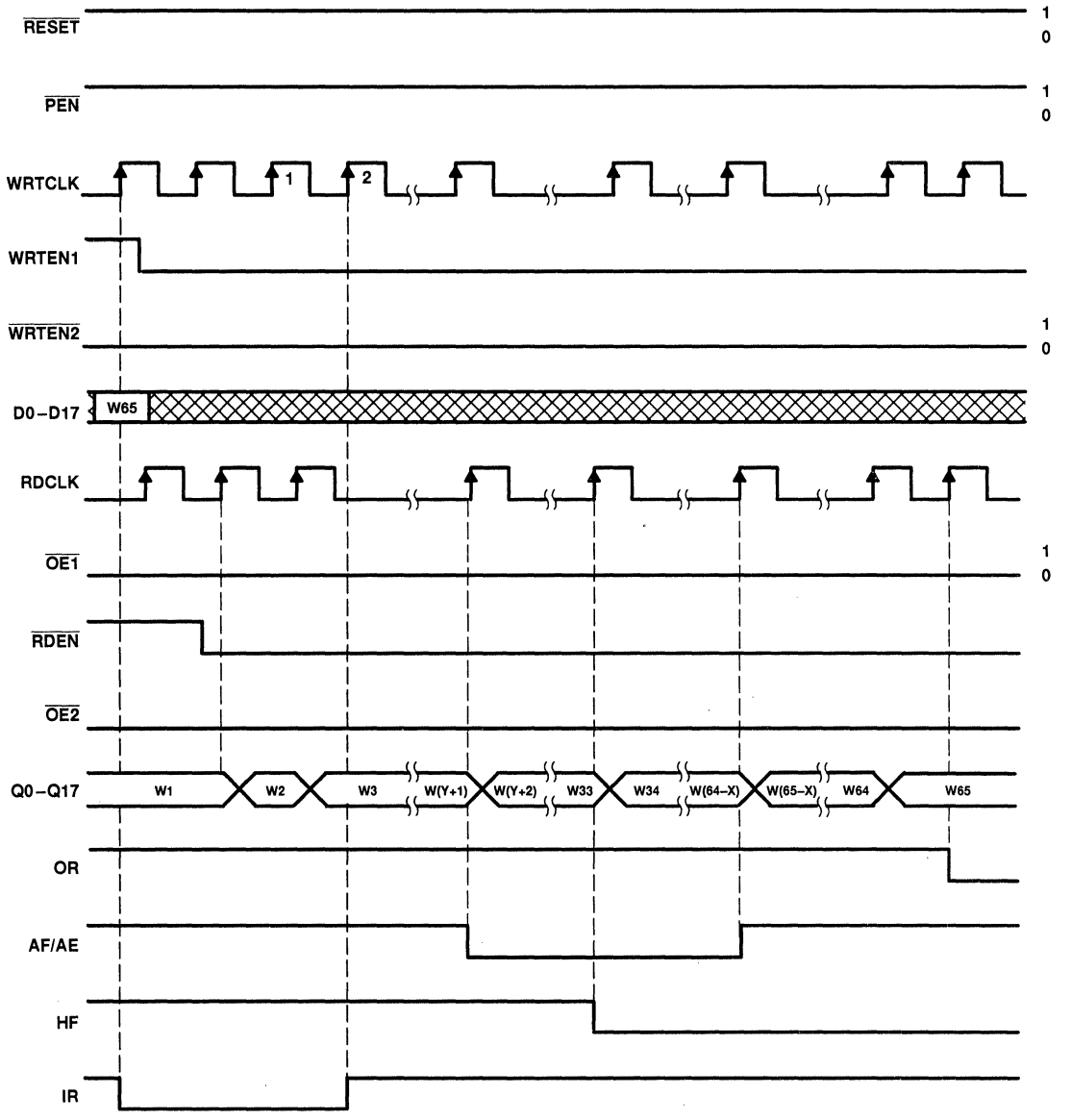


Figure 3. Read Cycle

offset values for AF/AE

The almost-full/almost-empty flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of X = Y = 8 are used. The AF/AE flag is high when the FIFO contains X or less words or (64 – Y) or more words.

Program enable ($\overline{PEN}$) should be held high throughout the reset cycle. $\overline{PEN}$ can be brought low only when IR is high and WRTCLK is low. On the following low-to-high transition of WRTCLK, the binary value on D0–D4 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{PEN}$ low for another low-to-high transition of WRTCLK reprograms Y to the binary value on D0–D4 at the time of the second WRTCLK low-to-high transition. When the offsets are being programmed, writes to the FIFO memory are disabled regardless of the state of the write enables (WRTEN1, $\overline{WRTEN2}$). A maximum value of 31 can be programmed for either X or Y (see Figure 4). To use the default values of X = Y = 8, $\overline{PEN}$ must be held high.

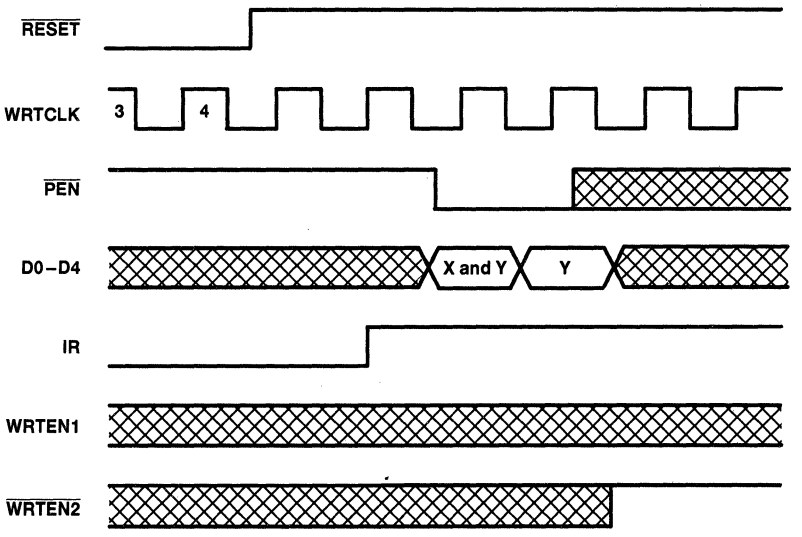


Figure 4. Programming X and Y Separately

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage, V_I ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			'ACT7813-15		'ACT7813-20		'ACT7813-25		'ACT7813-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8		0.8		0.8	V
I_{OH}	High-level output current	Q outputs, Flags		−8		−8		−8		−8	mA
I_{OL}	Low-level output current	Q outputs		16		16		16		16	mA
		Flags		8		8		8		8	
f_{clock}	Clock frequency			67		50		40		25	MHz
t_w	Pulse duration	WRTCLK high or low	6		7		8		12		ns
		RDCLK high or low	6		7		8		12		
		$\overline{PEN}$ low	8		9		9		12		
t_{su}	Setup time	D0–D17 before WRTCLK↑	4		5		5		5		ns
		WRTEN1, $\overline{WRTEN2}$ before WRTCLK↑	4		5		5		5		
		$\overline{OE1}$, $\overline{OE2}$ before RDCLK↑	5		5		6		6		
		$\overline{RDEN}$ before RDCLK↑	4		5		5		5		
		Reset: $\overline{RESET}$ low before first WRTCLK↑ and RDCLK↑†	5		6		6		6		
		$\overline{PEN}$ before WRTCLK↑	5		6		6		6		
t_h	Hold time	D0–D17 after WRTCLK↑	0		0		0		0		ns
		WRTEN1, $\overline{WRTEN2}$ after WRTCLK↑	0		0		0		0		
		$\overline{OE1}$, $\overline{OE2}$, $\overline{RDEN}$ after RDCLK↑	0		0		0		0		
		Reset: $\overline{RESET}$ low after fourth WRTCLK↑ and RDCLK↑†	2		2		2		2		
		$\overline{PEN}$ high after WRTCLK↓	0		0		0		0		
		$\overline{PEN}$ low after WRTCLK↑	2		2		2		2		
T_A	Operating free-air temperature		0	70	0	70	0	70	0	70	°C

† To permit the clock pulse to be utilized for reset purposes

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = – 8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	µA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	µA
I_{CC}		V_I = V_{CC} – 0.2 V or 0					400	µA
ΔI_{CC}‡		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (see Figures 9 and 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7813-15			'ACT7813-20		'ACT7813-25		'ACT7813-40		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	WRTCLK or RDCLK		67			50		40		25		MHz
t_{pd}	RDCLK↑	Any Q	4	9.5	12	4	13	4	15	4	20	ns
t_{pd}§				8.5								
t_{pd}	WRTCLK↑	IR	3		8.5	3	11	3	13	3	15	ns
t_{pd}	RDCLK↑	OR	3		8.5	3	11	3	13	3	15	ns
t_{pd}	WRTCLK↑	AF/AE	7		16.5	7	19	7	21	7	23	ns
	RDCLK↑		7		17	7	19	7	21	7	23	
t_{PLH}	WRTCLK↑	HF	7		15	7	17	7	19	7	21	ns
t_{PHL}	RDCLK↑		7		15.5	7	18	7	20	7	22	
t_{PLH}	$\overline{RESET}$ low	AF/AE	2		9	2	11	2	13	2	15	ns
t_{PHL}		HF	2		10	2	12	2	14	2	16	
t_{en}	$\overline{OE1}$, $\overline{OE2}$	Any Q	2		8.5	2	11	2	11	2	11	ns
t_{dis}			2		9.5	2	11	2	14	2	14	

§ This parameter is measured with a 30-pF load (see Figure 5).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 5 MHz	53	pF

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

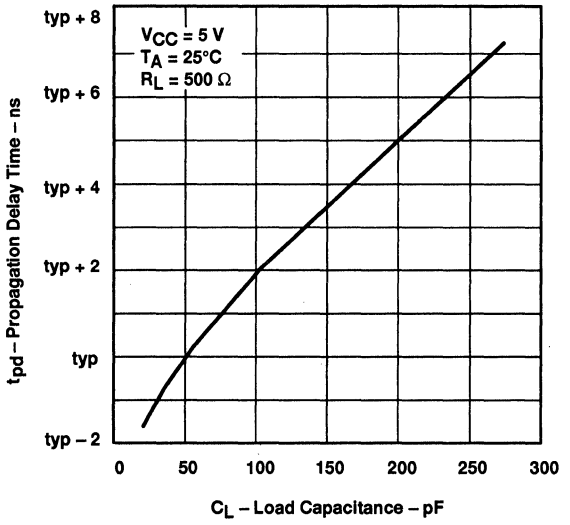


Figure 5

SUPPLY CURRENT
vs
CLOCK FREQUENCY

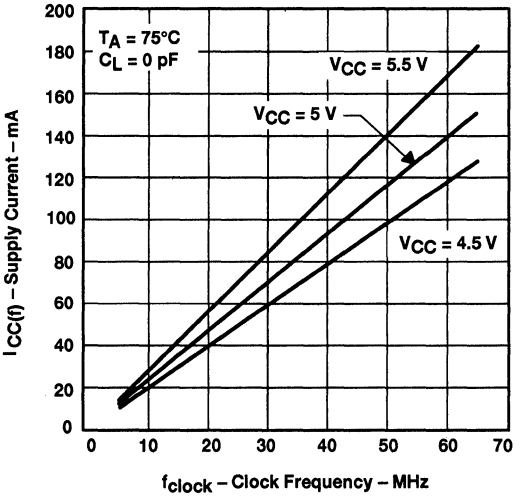


Figure 6

TYPICAL CHARACTERISTICS

calculating power dissipation

With $I_{CC(f)}$ taken from Figure 6, the maximum power dissipation (P_T) based on all data outputs changing states on each read can be calculated using:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC}	=	power-down I_{CC} maximum
N	=	number of inputs driven by a TTL device
ΔI_{CC}	=	increase in supply current
dc	=	duty cycle of inputs at a TTL high level of 3.4 V
C_{pd}	=	power dissipation capacitance
C_L	=	output capacitive load
f_i	=	data input frequency
f_o	=	data output frequency

APPLICATION INFORMATION

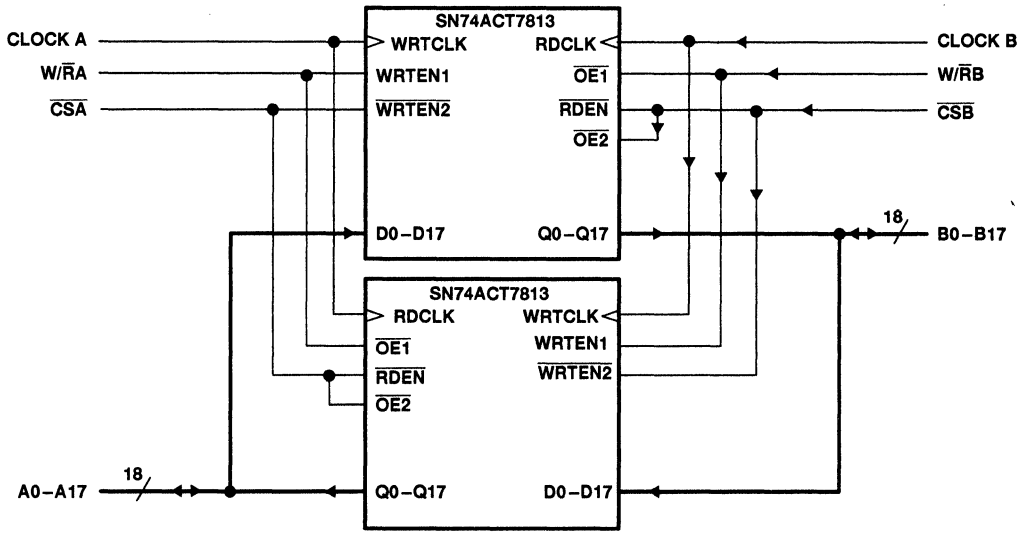


Figure 7. Bidirectional Configuration

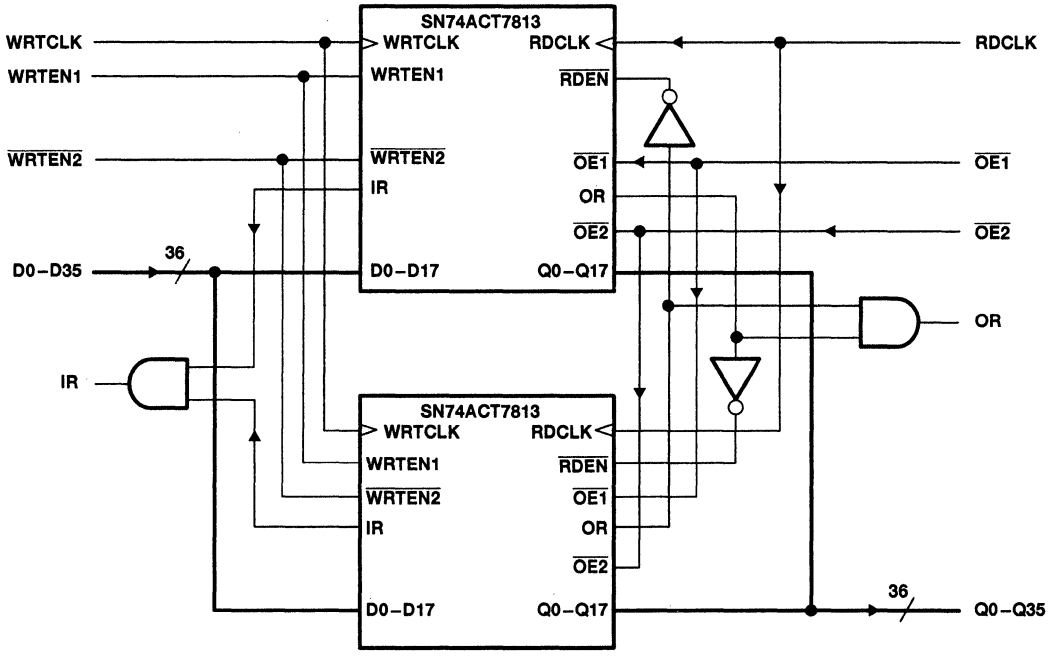


Figure 8. Word-Width Expansion: 64 × 36 Bits

PARAMETER MEASUREMENT INFORMATION

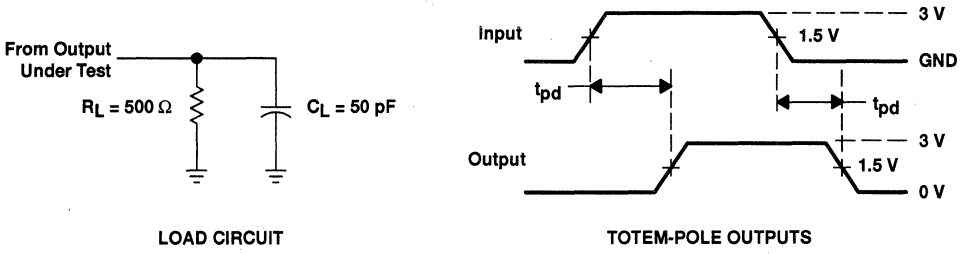
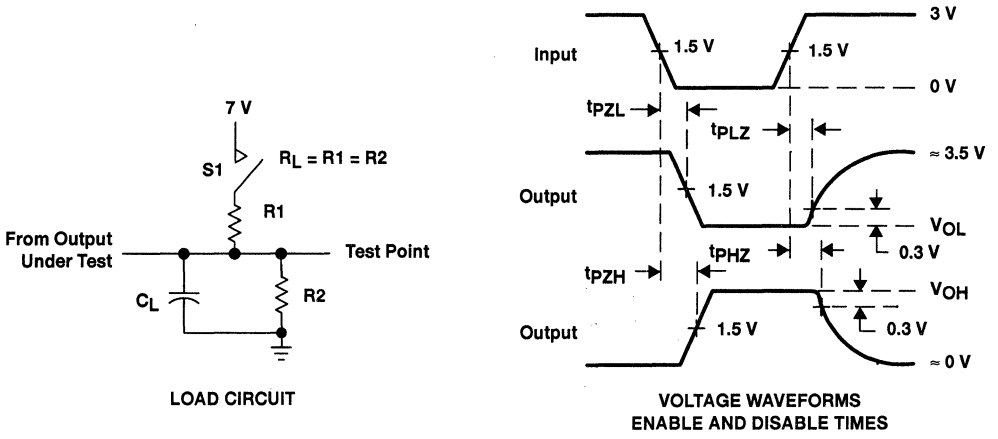


Figure 9. Standard CMOS Outputs (IR, OR, HF, AF/AE)



PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

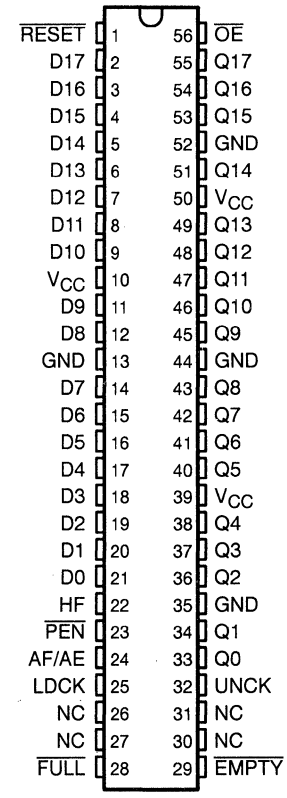
† Includes probe and test-fixture capacitance

Figure 10. 3-State Outputs (Any Q)

SCAS209 – APRIL 1992

- **Member of the Texas Instruments Widebus™ Family**
- **Load Clock and Unload Clock Can Be Asynchronous or Coincident**
- **64 Words by 18 Bits**
- **Low-Power Advanced CMOS Technology**
- **Full, Empty, and Half-Full Flags**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Fast Access Times of 15 ns With a 50-pF Load and All Data Outputs Switching Simultaneously**
- **Data Rates From 0 to 50 MHz**
- **3-State Outputs**
- **Pin Compatible With SN74ACT7804 and SN74ACT7806**
- **Packaged in Shrink Small-Outline 300-mil Package (DL) Using 25-mil Center-to-Center Spacing**

DL PACKAGE
(TOP VIEW)



description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7814 is a 64-word by 18-bit FIFO for high speed and fast access times. It processes data at rates up to 50 MHz and access times of 15 ns in a bit-parallel format.

Data is written into memory on a low-to-high transition at the load clock (LDCK) input and is read out on a low-to-high transition at the unload clock (UNCK) input. The memory is full when the number of words clocked in exceeds the number of words clocked out by 64. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

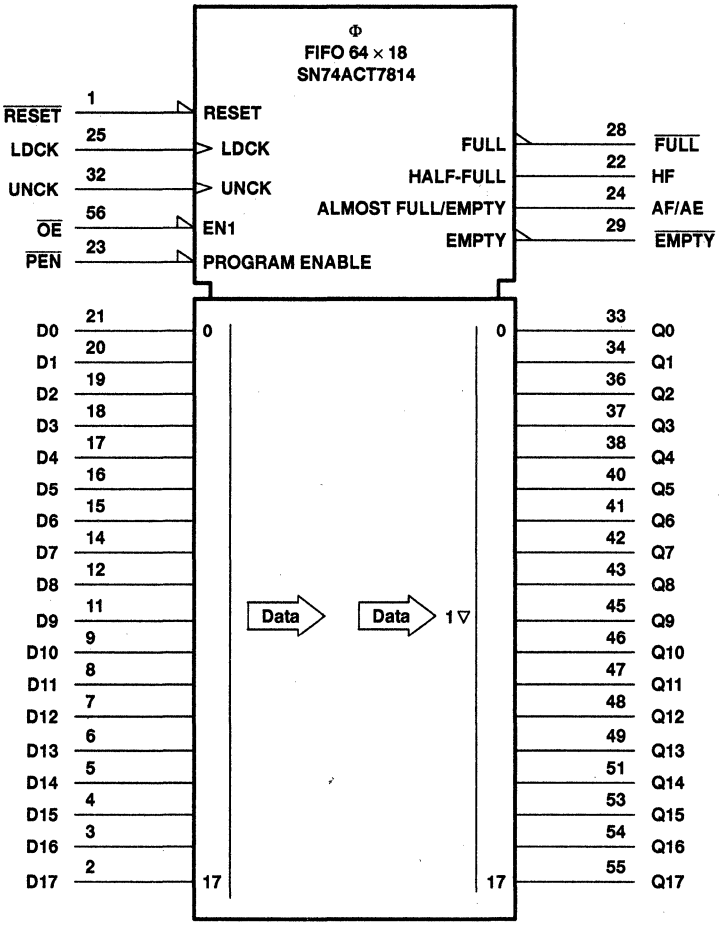
Status of the FIFO memory is monitored by the full ($\overline{FULL}$), empty ($\overline{EMPTY}$), half-full (HF), and almost-full/almost-empty (AF/AE) flags. The $\overline{FULL}$ output is low when the memory is full and high when the memory is not full. The $\overline{EMPTY}$ output is low when the memory is empty and high when it is not empty. The HF output is high when the FIFO contains 32 or more words and is low when it contains 31 or less words. The AF/AE status flag is a programmable flag. The first one or two low-to-high transitions of LDCK after reset are used to program the almost-empty offset value (X) and the almost-full offset value (Y) if program enable ($\overline{PEN}$) is low. The AF/AE flag is high when the FIFO contains X or less words or (64 – Y) or more words. The AF/AE flag is low when the FIFO contains between (X + 1) and (63 – Y) words.

A low level on the reset ($\overline{RESET}$) input resets the internal stack pointers and sets $\overline{FULL}$ high, HF low, and $\overline{EMPTY}$ low. The Q outputs are not reset to any specific logic level. The FIFO must be reset upon power up. The first word loaded into empty memory causes $\overline{EMPTY}$ to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. The data outputs are noninverting with respect to the data inputs and are in the high-impedance state when the output-enable ($\overline{OE}$) input is high.

The SN74ACT7814 is characterized for operation from 0°C to 70°C.

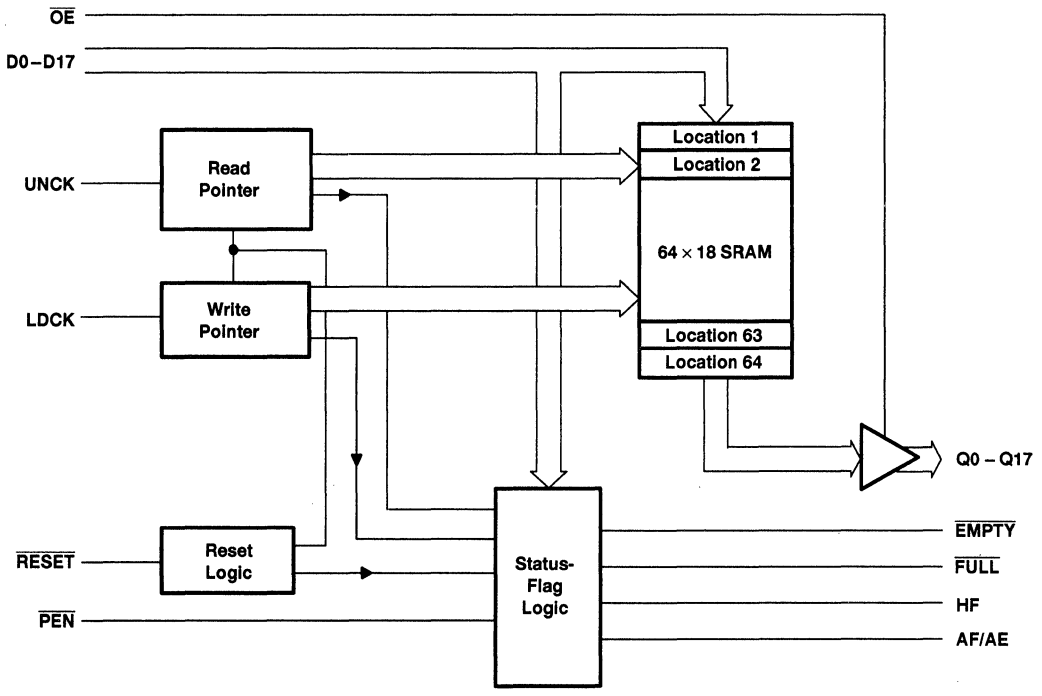
Widebus is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AE	24	O	Almost-full/almost-empty flag. Depth offset values can be programmed for AF/AE, or the default value of 8 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or less words or (64 – Y) or more words. AF/AE is high after reset.
D0–D17	21–14, 12–11, 9–2	I	The 18-bit data input port
$\overline{\text{EMPTY}}$	29	O	Empty flag. $\overline{\text{EMPTY}}$ is high when the FIFO memory is not empty; $\overline{\text{EMPTY}}$ is low when the FIFO memory is empty or upon assertion of $\overline{\text{RESET}}$.
$\overline{\text{FULL}}$	28	O	Full flag. $\overline{\text{FULL}}$ is high when the FIFO memory is not full or upon assertion of $\overline{\text{RESET}}$; $\overline{\text{FULL}}$ is low when the FIFO memory is full.
HF	22	O	Half-full flag. HF is high when the FIFO memory contains 32 or more words. HF is low after reset.
LDCK	25	I	Load clock. Data is written to the FIFO on the rising edge of LDCK when $\overline{\text{FULL}}$ is high.
$\overline{\text{OE}}$	56	I	Output enable. When $\overline{\text{OE}}$ is high, the data outputs are in the high-impedance state.
$\overline{\text{PEN}}$	23	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D4 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and WRTCLK is high.
Q0–Q17	33–34, 36–38, 40–43, 45–49, 51, 53–55	O	The 18-bit data output port
$\overline{\text{RESET}}$	1	I	Reset. A low level on $\overline{\text{RESET}}$ resets the FIFO and drives $\overline{\text{FULL}}$ high and HF and $\overline{\text{EMPTY}}$ low.
UNCK	32	I	Unload clock. Data is read from the FIFO on the rising edge of UNCK when $\overline{\text{EMPTY}}$ is high.

offset values for AF/AE

The almost-full/almost-empty flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. The AF/AE flag will be high when the FIFO contains X or less words or (64 – Y) or more words.

To program the offset values, $\overline{PEN}$ can be brought low after reset only when LDCK is low. On the following low-to-high transition of LDCK, the binary value on D0–D4 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{PEN}$ low for another low-to-high transition of LDCK reprograms Y to the binary value on D0–D4 at the time of the second LDCK low-to-high transition. Writes to the FIFO memory are disabled while the offsets are programmed. A maximum value of 31 can be programmed for either X or Y (see Figure 1). To use the default values of X = Y = 8, $\overline{PEN}$ must be held high.

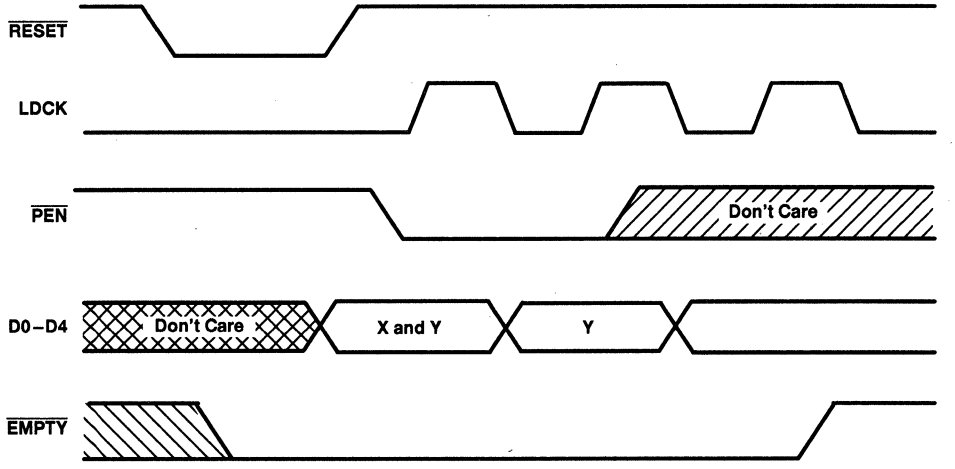


Figure 1. Programming X and Y Separately

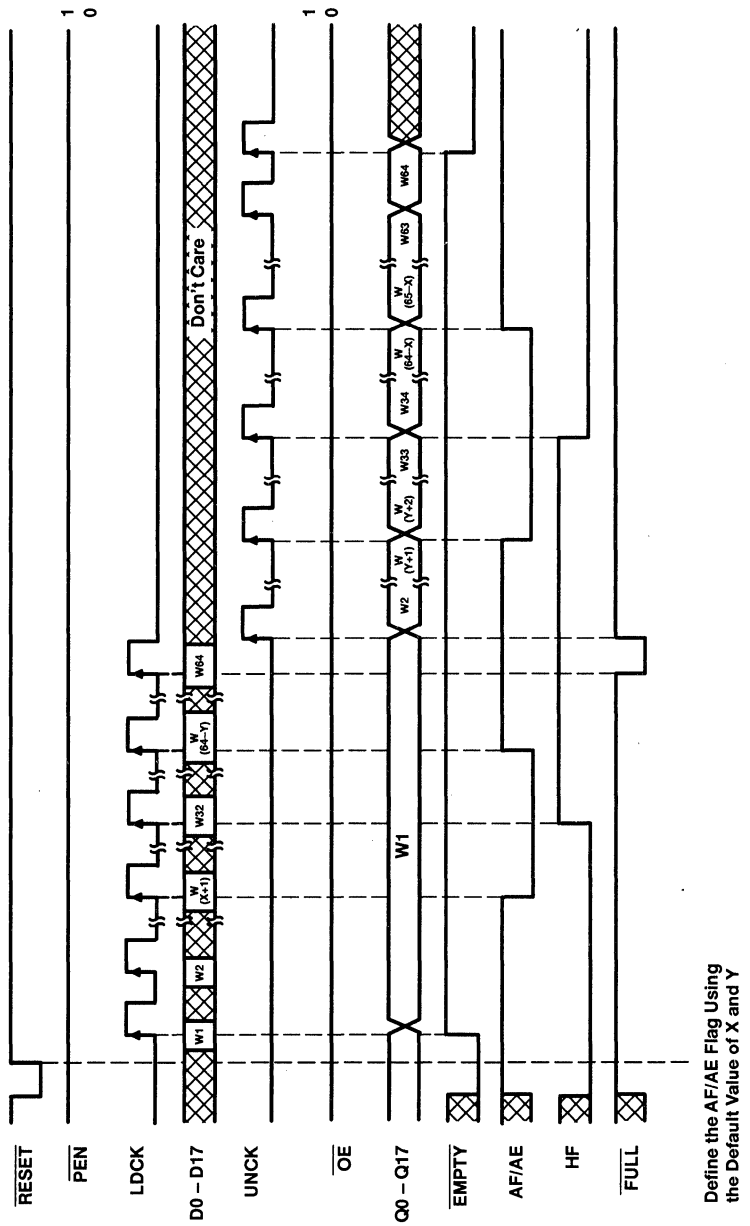


Figure 2. Write, Read, and Flag Timing Reference

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage, V_I ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			'ACT7814-20		'ACT7814-25		'ACT7814-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8		0.8	V
I_{OH}	High-level output current	Q outputs, Flags		−8		−8		−8	mA
I_{OL}	Low-level output current	Q outputs		16		16		16	mA
		Flags		8		8		8	
f_{clock}	Clock frequency			50		40		25	MHz
t_w	Pulse duration	LDCK high or low	7		8		12		ns
		UNCK high or low	7		8		12		
		$\overline{PEN}$ low	7		8		12		
		$\overline{RESET}$ low	10		10		12		
t_{su}	Setup time	D0–D17 before LDCK↑	5		5		5		ns
		$\overline{PEN}$ before LDCK↑	5		5		5		
		LDCK inactive before $\overline{RESET}$ high	5		6		6		
t_h	Hold time	D0–D17 after LDCK↑	0		0		0		ns
		LDCK inactive after $\overline{RESET}$ high	5		6		6		
		$\overline{PEN}$ low after LDCK↑	3		3		3		
		$\overline{PEN}$ high after LDCK↓	0		0		0		
T_A	Operating free-air temperature		0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = − 8 mA		2.4			V
V_{OL}	Flags	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
	Q outputs	V_{CC} = 4.5 V,	I_{OL} = 16 mA				0.5	
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±5	µA
I_{OZ}		V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±5	µA
I_{CC}		V_I = V_{CC} − 0.2 V or 0					400	µA
ΔI_{CC}§		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i		V_I = 0,	f = 1 MHz			4		pF
C_o		V_O = 0,	f = 1 MHz			8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the supply current for each input that is at one of the specified TTL voltage levels rather 0 V or V_{CC}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 5 and 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7814-20			'ACT7814-25		'ACT7814-40		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
f_{max}	LDCK or UNCK		50			40		25		MHz
t_{pd}	LDCK↑	Any Q	9		20	9	22	9	24	ns
	UNCK↑		6	11.5	15	6	18	6	20	
t_{pd}‡	UNCK↑			10.5						
t_{PLH}	LDCK↑	$\overline{EMPTY}$	6		15	6	17	6	19	ns
t_{PHL}	UNCK↑		6		15	6	17	6	19	
	$\overline{RESET}$ low		4		16	4	18	4	20	
t_{PHL}	LDCK↑	$\overline{FULL}$	6		15	6	17	6	19	ns
t_{PLH}	UNCK↑		6		15	6	17	6	19	
	$\overline{RESET}$ low		4		18	4	20	4	22	
t_{pd}	LDCK↑	AF/AE	7		18	7	20	7	22	ns
	UNCK↑		7		18	7	20	7	22	
t_{PLH}	$\overline{RESET}$ low		2		10	2	12	2	14	
t_{PLH}	LDCK↑	HF	5		18	5	20	5	22	ns
t_{PHL}	UNCK↑		7		18	7	20	7	22	
	$\overline{RESET}$ low		3		12	3	14	3	16	
t_{en}	$\overline{OE}$	Any Q	2		9	2	10	2	11	ns
t_{dis}			2		10	2	11	2	12	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This parameter is measured at C_L = 30 pF (see Figure 3).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per FIFO channel	Outputs enabled	C_L = 50 pF, f = 5 MHz	53	pF

TYPICAL CHARACTERISTICS

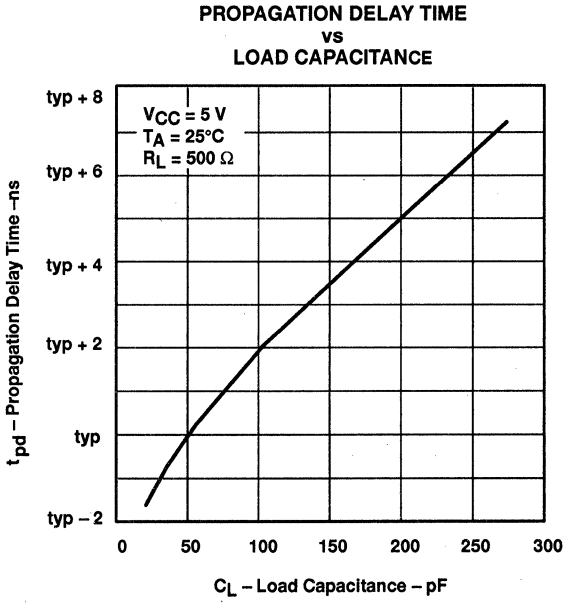


Figure 3

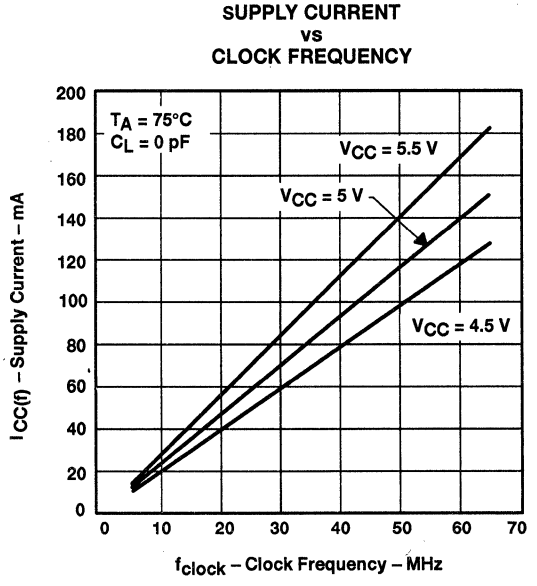


Figure 4

TYPICAL CHARACTERISTICS

calculating power dissipation

With $I_{CC(f)}$ taken from Figure 4, the maximum power dissipation (P_T) based on all data outputs changing states on each read can be calculated using:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

A more accurate power calculation based on device use and average number of data outputs switching can be found using:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC}	=	power-down I_{CC} maximum
N	=	number of inputs driven by a TTL device
ΔI_{CC}	=	increase in supply current
dc	=	duty cycle of inputs at a TTL high level of 3.4 V
C_{pd}	=	power dissipation capacitance
C_L	=	output capacitive load
f_i	=	data input frequency
f_o	=	data output frequency

APPLICATION INFORMATION

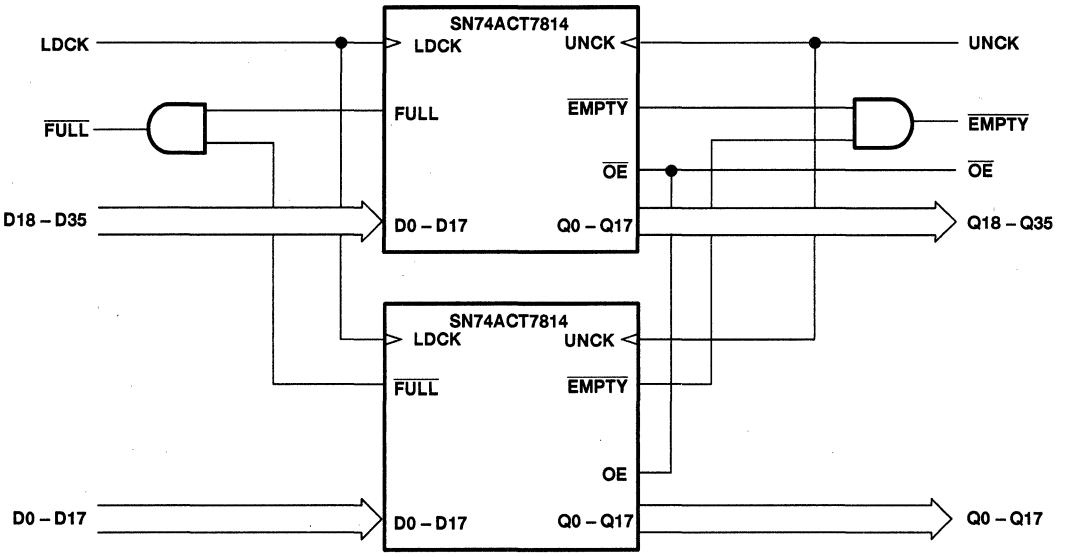


Figure 5. Word-Width Expansion: 64 Words by 36 Bits

PARAMETER MEASUREMENT INFORMATION

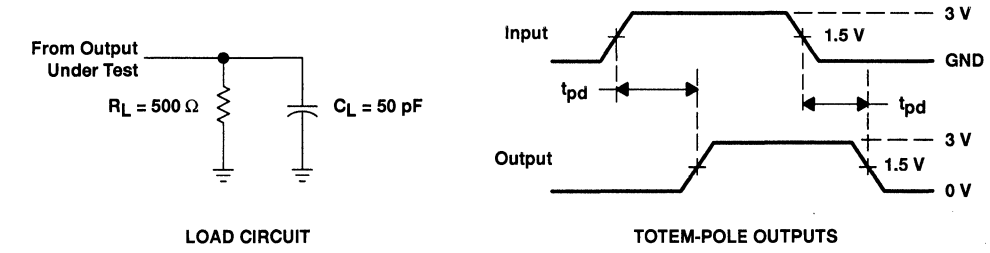
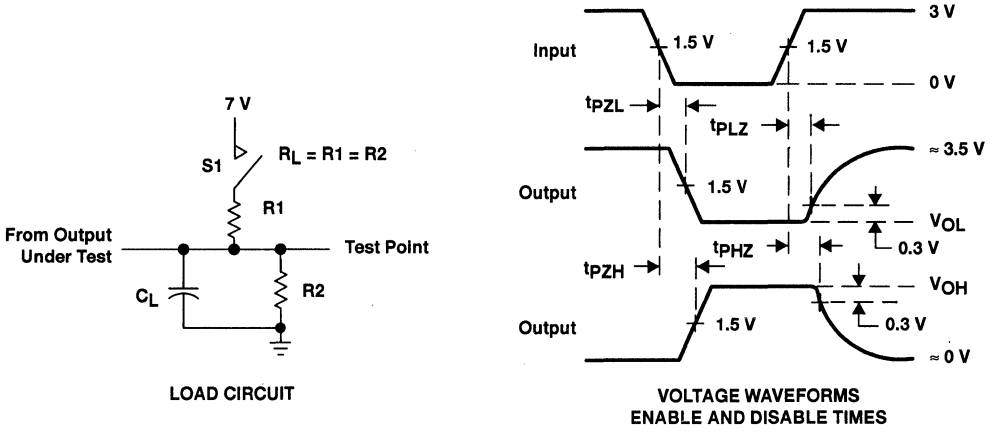


Figure 6. Standard CMOS Outputs ($\overline{FULL}$, $\overline{EMPTY}$, HF, AF/AE)



PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

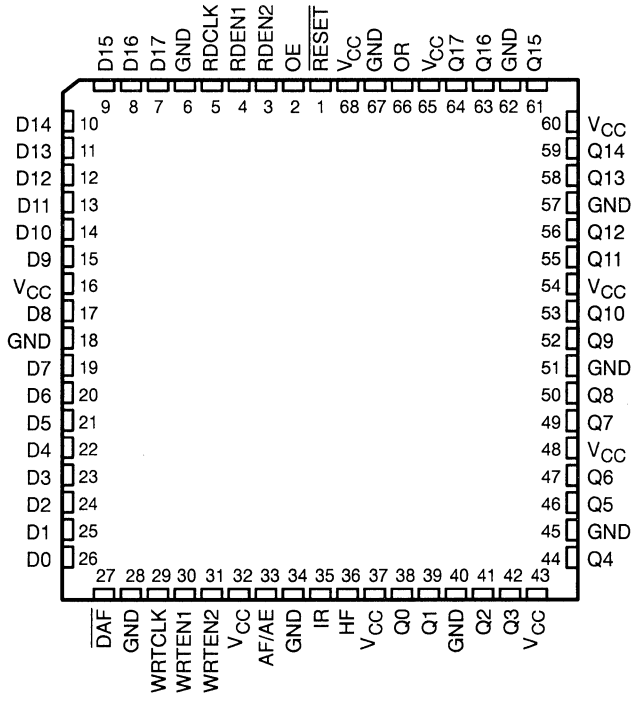
† Includes probe and test-fixture capacitance

Figure 7. 3-State Outputs (Any Q)

SCAS227B – FEBRUARY 1993 – REVISED OCTOBER 1994

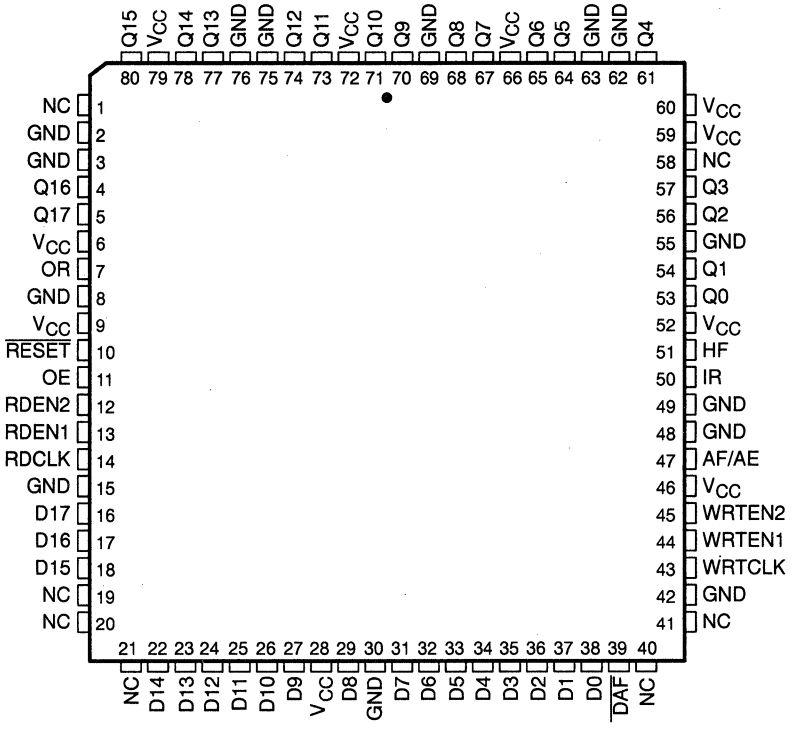
- Member of the Texas Instruments Widebus™ Family
- Independent Asynchronous Inputs and Outputs
- Read and Write Operations Can Be Synchronized to Independent System Clocks
- Programmable Almost-Full/Almost-Empty Flag
- Pin-to-Pin Compatible With SN74ACT7882, SN74ACT7884, and SN74ACT7811
- Input-Ready, Output-Ready, and Half-Full Flags
- Expandable in Word Width and/or Word Depth
- Fast Access Times of 11 ns With a 50-pF Load
- High Output Drive for Direct Bus Interface
- Available in 68-Pin PLCC (FN) or Space-Saving 80-Pin Shrink Quad Flat (PN) Packages

FN PACKAGE
(TOP VIEW)



Widebus is a trademark of Texas Instruments Incorporated.

PN PACKAGE
(TOP VIEW)



NC – No internal connection

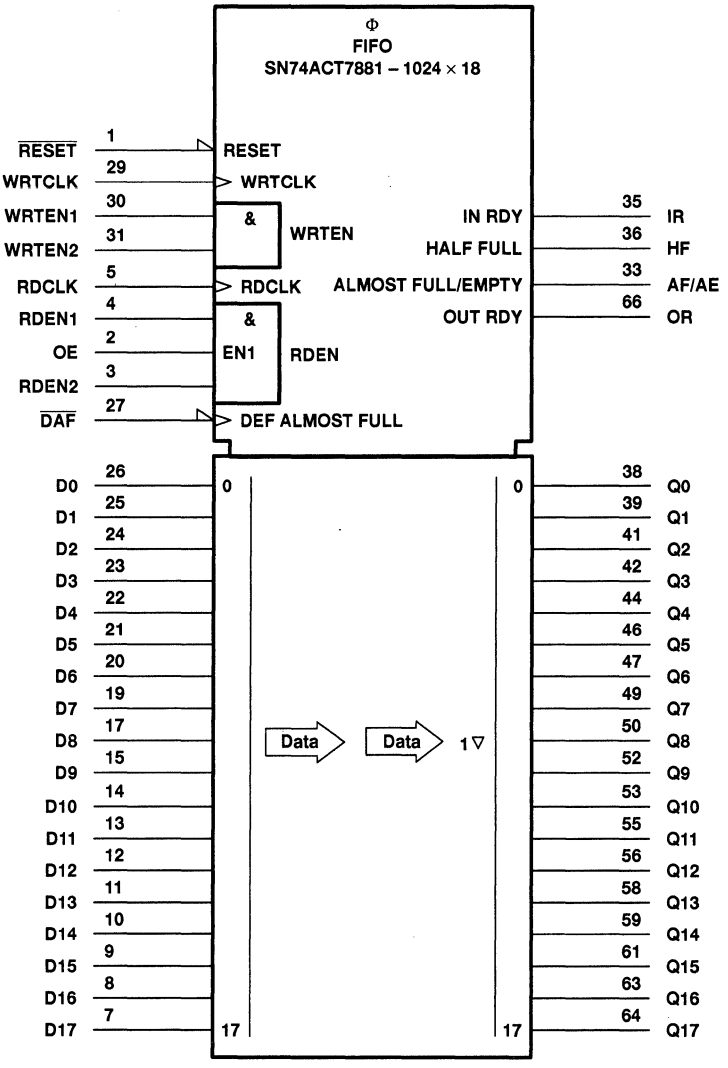
description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7881 is organized as 1024 × 18 bits. The SN74ACT7881 processes data at rates up to 67 MHz and access times of 11 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is easily accomplished in both word width and word depth.

The SN74ACT7881 has normal input-bus-to-output-bus asynchronous operation. The special enable circuitry adds the ability to synchronize independent reads and writes to their respective system clocks.

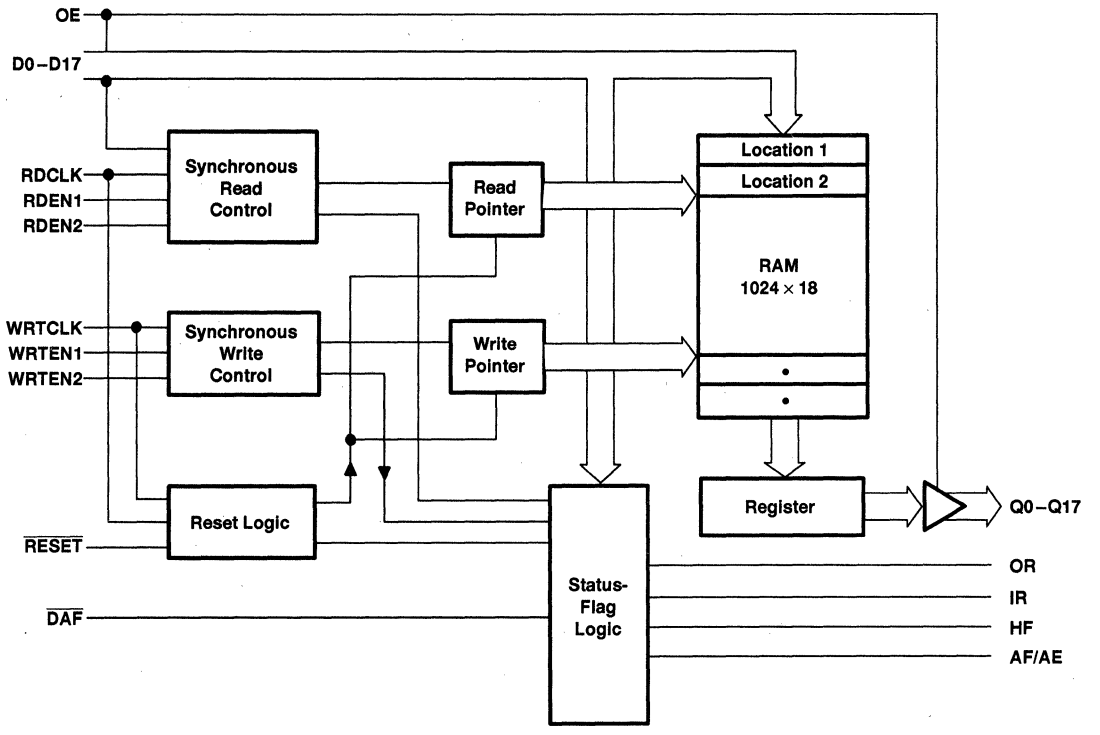
The SN74ACT7881 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FN package.

functional block diagram

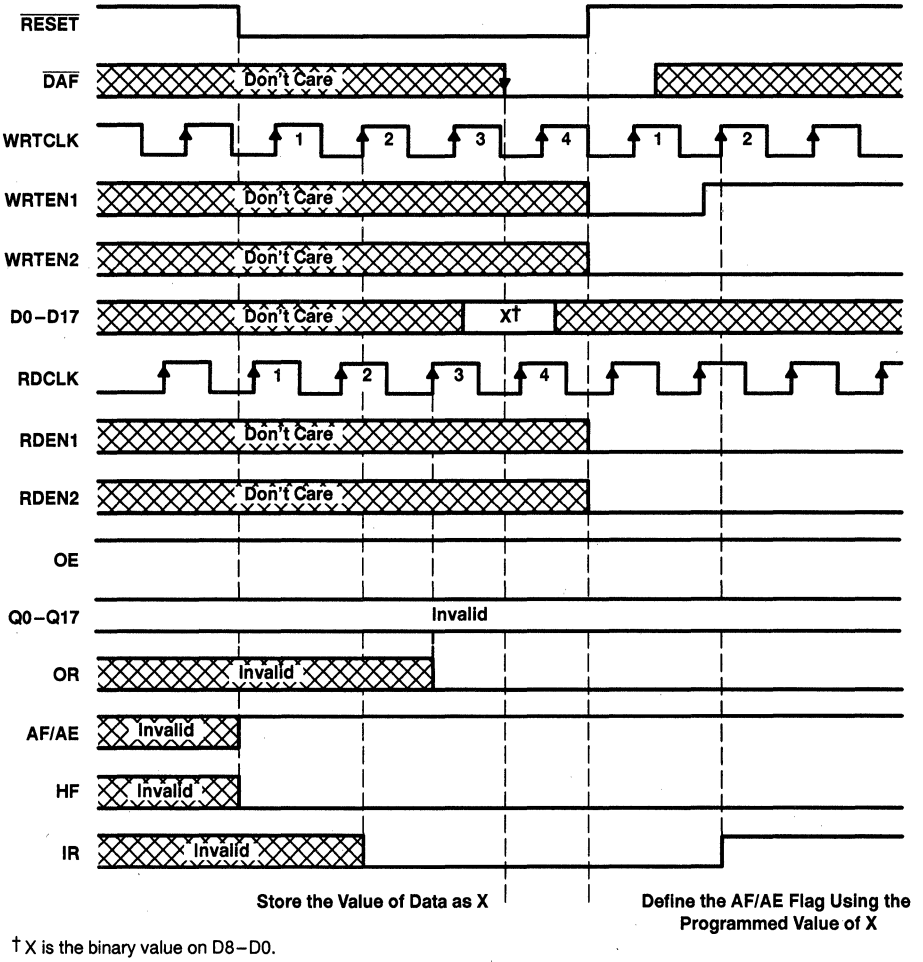


Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AE	33	O	Almost-full/almost-empty flag. The AF/AE boundary is defined by the almost-full/almost-empty offset value (X). This value can be programmed during reset, or the default value of 256 can be used. AF/AE is high when the FIFO contains (X + 1) or less words or (1025 – X) or more words. AF/AE is low when the FIFO contains between (X +2) and (1024 - X) words. Programming procedure for AF/AE – The almost-full/almost-empty flag is programmed during each reset cycle. The almost-full/almost-empty offset value (X) is either a user-defined value or the default of X = 256. Instructions to program AF/AE using both methods are as follows: User-defined X Step 1: Take $\overline{DAF}$ from high to low. Step 2: If $\overline{RESET}$ is not already low, take $\overline{RESET}$ low. Step 3: With $\overline{DAF}$ held low, take $\overline{RESET}$ high. This defines the AF/AE using X. Step 4: To retain the current offset for the next reset, keep $\overline{DAF}$ low. Default X To redefine AF/AE using the default value of X = 256, hold $\overline{DAF}$ high during the reset cycle.
$\overline{DAF}$	27	I	Define-almost-full. The high-to-low transition of $\overline{DAF}$ stores the binary value of data inputs as the almost-full/almost-empty offset value (X). With $\overline{DAF}$ held low, a low pulse on $\overline{RESET}$ defines the almost-full/almost-empty (AF/AE) flag using X.
D0–D17	26–19, 17, 15–7	I	Data inputs for 18-bit-wide data to be stored in the memory. A high-to-low transition of $\overline{DAF}$ captures data for the almost-empty/almost-full offset (X) from D8–D0.
HF	36	O	Half-full flag. HF is high when the FIFO contains 512 or more words and is low when the number of words in memory is less than half the depth of the FIFO.
IR	35	O	Input-ready flag. IR is high when the FIFO is not full and low when the device is full. During reset, IR is driven low on the rising edge of the second WRTCLK pulse. IR is then driven high on the rising edge of the second WRTCLK pulse after $\overline{RESET}$ goes high. After the FIFO is filled and IR is driven low, IR is driven high on the second WRTCLK pulse after the first valid read.
OE	2	I	Output enable. The Q0–Q17 outputs are in the high-impedance state when OE is low. OE must be high before the rising edge of RDCLK to read a word from memory.
OR	66	O	Output-ready flag. OR is high when the FIFO is not empty and low when the FIFO is empty. During reset, OR is set low on the rising edge of the third RDCLK pulse. OR is set high on the rising edge of the third RDCLK pulse to occur after the first word is written into the FIFO. OR is set low on the rising edge of the first RDCLK pulse after the last word is read.
Q0–Q17	38–39, 41–42, 44, 46–47, 49–50, 52–53, 55–56, 58–59, 61, 63–64	O	Data outputs. The first data word to be loaded into the FIFO is moved to Q0–Q17 on the rising edge of the third RDCLK pulse to occur after the first valid write. RDEN1 and RDEN2 do not affect this operation. Following data is unloaded on the rising edge of RDCLK when RDEN1, RDEN2, OE, and OR are high.
RDCLK	5	I	Read clock. Data is read out of memory on the low-to-high transition of RDCLK if OR, OE, RDEN1, and RDEN2 are high. RDCLK is a free-running clock and functions as the synchronizing clock for all data transfers out of the FIFO. OR is also driven synchronously with respect to the RDCLK signal.
RDEN1, RDEN2	4 3	I	Read enable. RDEN1 and RDEN2 must be high before a rising edge on RDCLK to read a word out of memory. RDEN1 and RDEN2 are not used to read the first word stored in memory.
$\overline{RESET}$	1	I	Reset. A reset is accomplished by taking $\overline{RESET}$ low and generating a minimum of four RDCLK and WRTCLK cycles. This ensures that the internal read and write pointers are reset and that OR, HF, and IR are low, and AF/AE is high. The FIFO must be reset upon power up. With $\overline{DAF}$ at a low level, a low pulse on $\overline{RESET}$ defines AF/AE using the almost-full/almost-empty offset value (X), where X is the value previously stored. With $\overline{DAF}$ at a high level, a low-level pulse on $\overline{RESET}$ defines the AF/AE flag using the default value of X = 256.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
WRTCLK	29	I	Write clock. Data is written into memory on a low-to-high transition of WRTCLK if IR, WRTEN1, and WRTEN2 are high. WRTCLK is a free-running clock and functions as the synchronizing clock for all data transfers into the FIFO. IR is also driven synchronously with respect to WRTCLK.
WRTEN1, WRTEN2	30 31	I	Write enable. WRTEN1 and WRTEN2 must be high before a rising edge on WRTCLK for a word to be written into memory. WRTEN1 and WRTEN2 do not affect the storage of the almost-full/almost-empty offset value (X).



† X is the binary value on D8–D0.

Figure 1. Reset Cycle: Define AF/AE Flag Using a Programmed Value of X

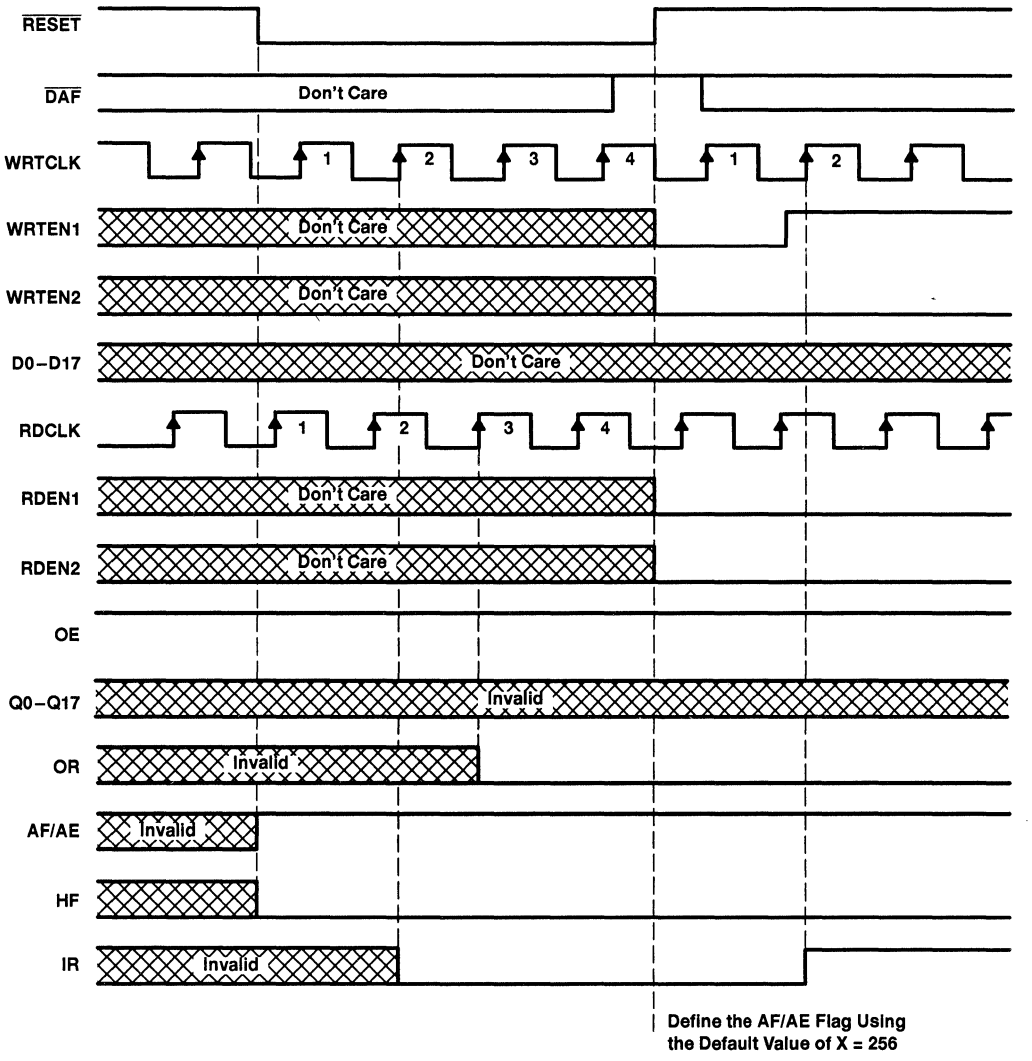
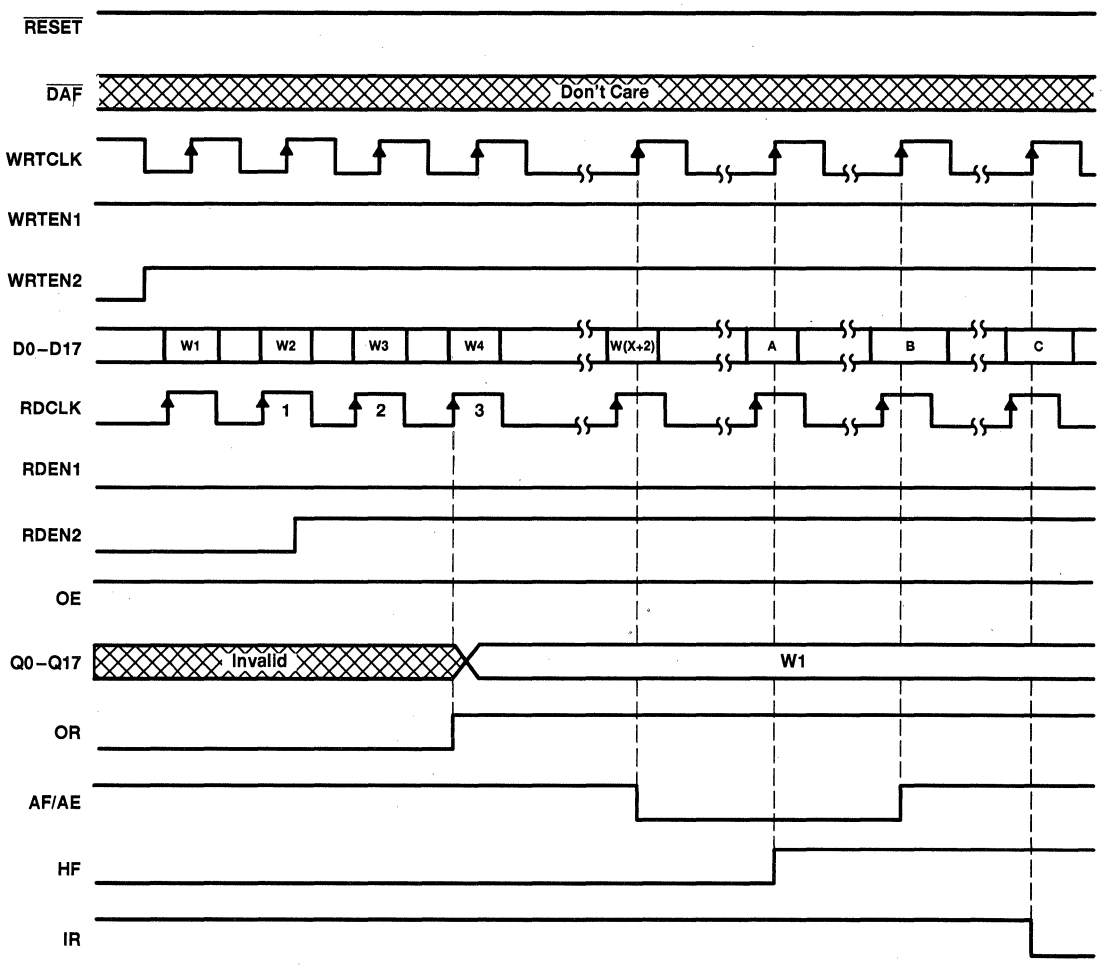


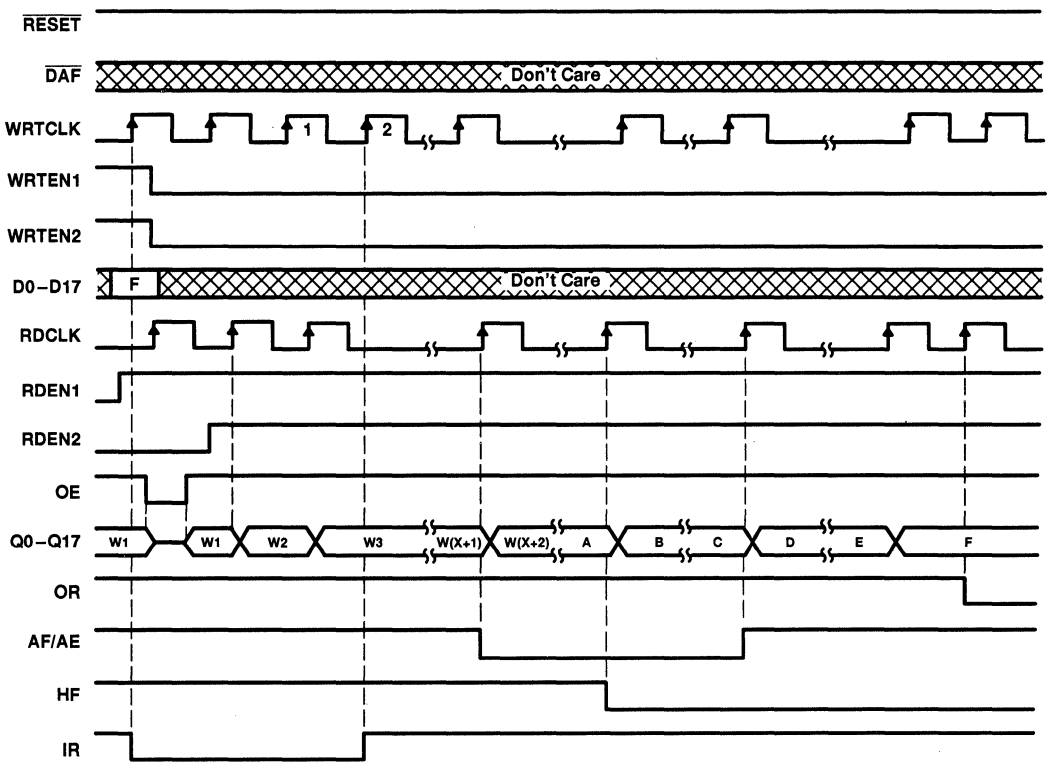
Figure 2. Reset Cycle: Define AF/AE Flag Using the Default Value fo X = 256



DATA WORD NUMBERS FOR FLAG TRANSITIONS

TRANSITION WORD		
A	B	C
W513	W(1025 – X)	W1025

Figure 3. Write Cycle



DATA WORD NUMBERS FOR FLAG TRANSITIONS

TRANSITION WORD					
A	B	C	D	E	F
W513	W514	W(1024 – X)	W(1025 – X)	W1024	W1025

Figure 4. Read Cycle

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage, V_I ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		16	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = − 8 mA	2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 16 mA			0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0			±5	µA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0			±5	µA
I_{CC}§	V_I = V_{CC} − 0.2 V or 0				400	µA
	One input at 3.4 V,	Other inputs at V_{CC} or GND			1.2	mA
C_i	V_I = 0,	f = 1 MHz		4		pF
C_o	V_O = 0,	f = 1 MHz		8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ I_{CC} tested with outputs open.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 4)

			'ACT7881-15		'ACT7881-20		'ACT7881-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		67		50		33.4		MHz
t_w	Pulse duration	WRTCLK high	5		7		8.5		ns
		WRTCLK low	7		7		11		
		RDCLK high	5		7		8.5		
		RDCLK low	7		7		11		
		$\overline{DAF}$ high	7		7		10		
t_{su}	Setup time	D0–D17 before WRTCLK↑	5		5		5		ns
		WRTEN1, WRTEN2 high before WRTCLK↑	4		5		5		
		OE, RDEN1, RDEN2 high before RDCLK↑	4		5		5		
		Reset: $\overline{RESET}$ low before first WRTCLK↑ and RDCLK↑†	5		6		7		
		Define AF/AE: D0–D8 before $\overline{DAF}$↓	3		5		5		
		Define AF/AE: $\overline{DAF}$↓ before $\overline{RESET}$↑	3		6		7		
		Define AF/AE (default): $\overline{DAF}$ high before $\overline{RESET}$↑	4		5		5		
t_h	Hold time	D0–D17 after WRTCLK↑	0		0		0		ns
		WRTEN1, WRTEN2 high after WRTCLK↑	0		0		0		
		OE, RDEN1, RDEN2 high after RDCLK↑	0		0		0		
		Reset: $\overline{RESET}$ low after fourth WRTCLK↑ and RDCLK↑†	0		0		0		
		Define AF/AE: D0–D8 after $\overline{DAF}$↓	0		0		0		
		Define AF/AE: $\overline{DAF}$ low after $\overline{RESET}$↑	0		0		0		
		Define AF/AE (default): $\overline{DAF}$ high after $\overline{RESET}$↑	0		0		0		

† To permit the clock pulse to be utilized for reset purposes

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 7 and 8)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7881-15		'ACT7881-20		'ACT7881-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	WRTCLK or RDCLK		67		50		33.4		MHz
t_{pd}	RDCLK↑	Any Q	3	12	3	13	3	18	ns
t_{pd}‡									
t_{pd}	WRTCLK↑	IR	2	8	2	9.5	2	12	ns
t_{pd}	RDCLK↑	OR	2	8	2	9.5	2	12	
t_{pd}	WRTCLK↑	AF/AE	6	17	6	19	6	22	ns
	RDCLK↑		6	17	6	19	6	22	
t_{PLH}	WRTCLK↑	HF	6	14	6	17	6	21	ns
t_{PHL}	RDCLK↑		6	14	6	17	6	21	
t_{PLH}	$\overline{RESET}$↓	AF/AE	3	12	3	17	3	21	ns
t_{PHL}		HF	3	14	3	19	3	23	
t_{en}	OE	Any Q	2	9	2	11	2	11	ns
t_{dis}			2	10	2	14	2	14	

‡ This parameter is measured with C_L = 30 pF (see Figure 5).

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per 1K bits	C_L = 50 pF, f = 5 MHz	65	pF

TYPICAL CHARACTERISTICS

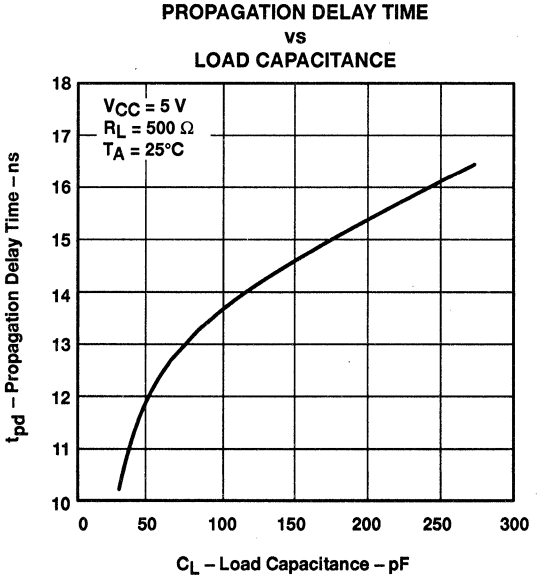


Figure 5

TYPICAL CHARACTERISTICS

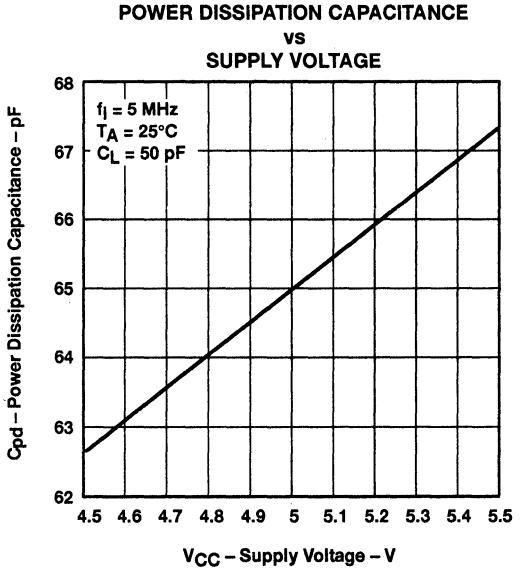


Figure 6

calculating power dissipation

The maximum power dissipation (P_T) of the SN74ACT7881 can be calculated using:

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

where:

I_{CC}	=	power-down I_{CC} maximum
N	=	number of inputs driven by a TTL device
ΔI_{CC}	=	increase in supply current
dc	=	duty cycle of inputs at a TTL high level of 3.4 V
C_{pd}	=	power dissipation capacitance
C_L	=	output capacitive load
f_i	=	data input frequency
f_o	=	data output frequency

PARAMETER MEASUREMENT INFORMATION

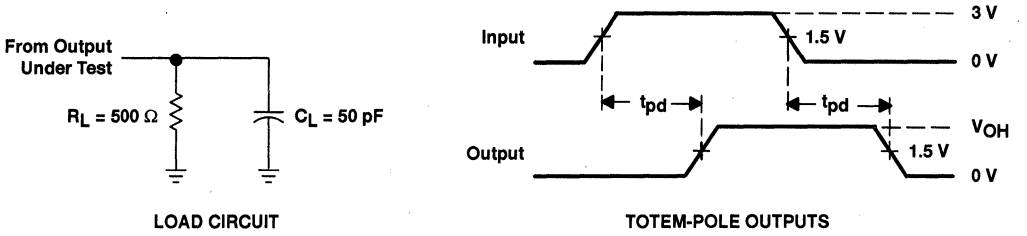
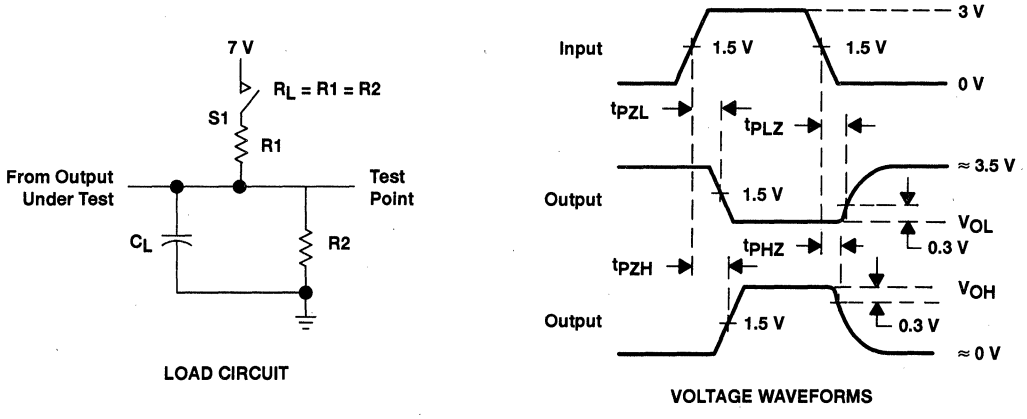


Figure 7. Standard CMOS Outputs



PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test fixture capacitance

Figure 8. 3-State Outputs (Any Q)

APPLICATION INFORMATION

expanding the SN74ACT7881

The SN74ACT7881 is expandable in both word width and word depth. Word-depth expansion is accomplished by connecting the devices in series such that data flows through each device in the chain. Figure 9 shows two SN74ACT7881 devices configured for word-depth expansion. The common clock between the devices can be tied to either the write clock (WRTCLK) of the first device or the read clock (RDCLK) of the last device. The output-ready flag (OR) of the previous device and the input-ready flag (IR) of the next device maintain data flow to the last device in the chain whenever space is available.

Figure 10 shows two SN74ACT7881 devices in word-width expansion. Word-width expansion is accomplished by simply connecting all common control signals between the devices and creating composite input-ready (IR) and output-ready (OR) signals. The almost-full/almost-empty flag (AF/AE) and half-full flag (HF) can be sampled from any one device. Word-Depth expansion and word-width expansion can be used together.

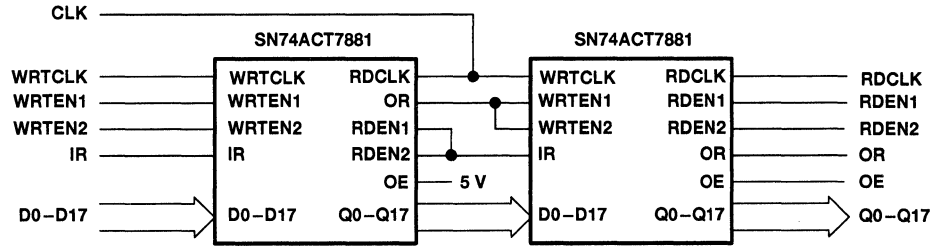


Figure 9. Word-Depth Expansion: 2048/4096/8192 Words × 18 Bits, N = 2

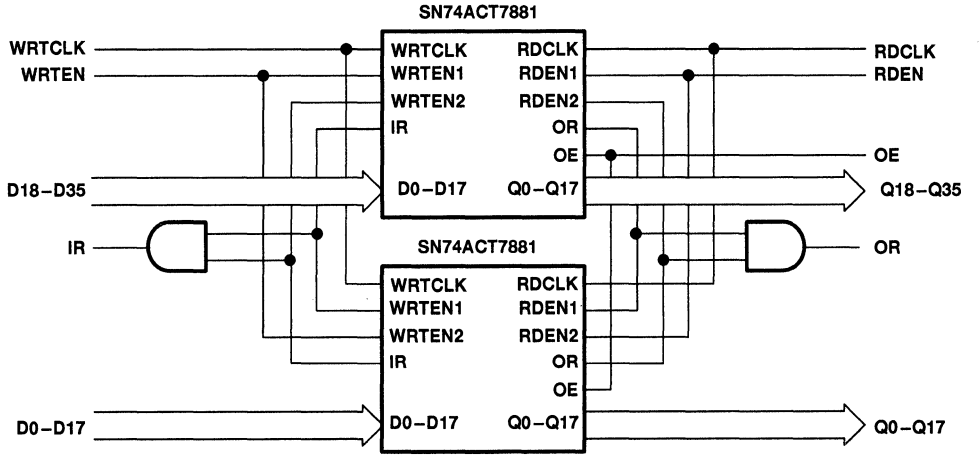
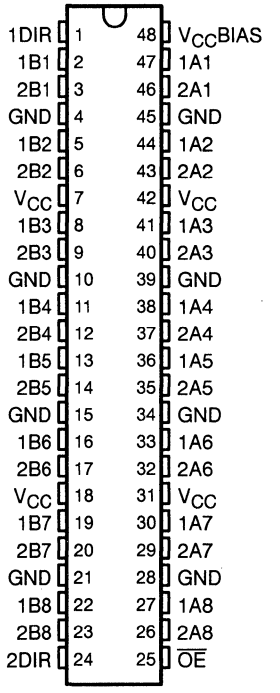


Figure 10. Word-Width Expansion: 1024 Words × 36 Bits

Contents

- **Supports the VME64 ETL Specification**
- **Reduced, TTL-Compatible, Input Threshold Range**
- **High-Drive Outputs (I_{OH} = –60 mA, I_{OL} = 90 mA) Support 25-Ω Incident-Wave Switching**
- **V_{CC}BIAS Pin Minimizes Signal Distortion During Live Insertion**
- **Internal Pullup Resistor on $\overline{OE}$ Keeps Outputs in High-Impedance State During Power Up or Power Down**
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **25-Ω Series Dampening Resistor on B Port**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-Mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABTE16245 . . . WD PACKAGE
SN74ABTE16245 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'ABTE16245 are 16-bit (dual-octal) noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements. These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

The B port has a 25-Ω series output resistor to reduce ringing. Active bus-hold inputs are also found on the B port to hold unused or floating inputs at a valid logic level.

The A port provides for the precharging of the outputs via V_{CC}BIAS, which establishes a voltage between 1.3 V and 1.7 V when V_{CC} is not connected.

The SN74ABTE16245 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABTE16245 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABTE16245 is characterized for operation from –40°C to 85°C.

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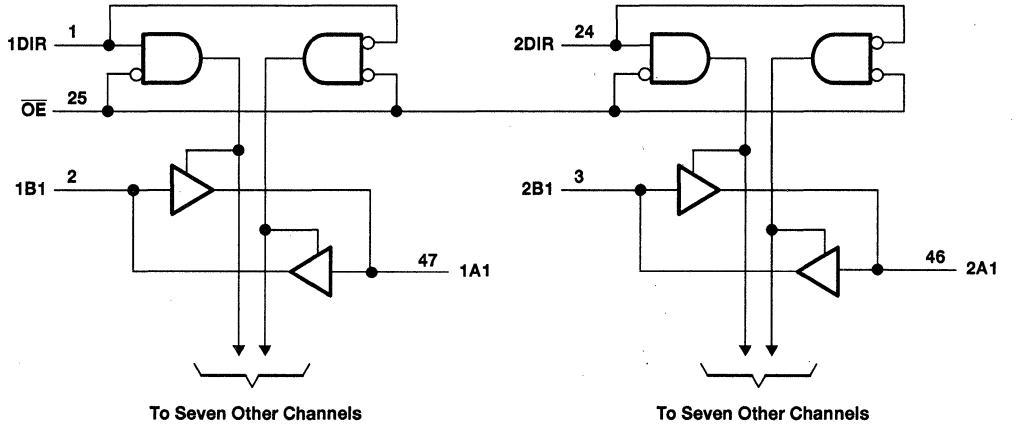
FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	A data to B bus
L	H	B data to A bus
H	X	Isolation

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

			SN54ABTE16245			SN74ABTE16245			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{OE}$	2			2			V
		Except $\overline{OE}$	1.6			1.6			
V_{IL}	Low-level input voltage	$\overline{OE}$			0.8			0.8	V
		Except $\overline{OE}$			1.4			1.4	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	B bus			−12			−12	mA
		A bus			−24			−60	
I_{OL}	Low-level output current	B bus			12			12	mA
		A bus			64			90	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10			10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 3: Unused or floating pins (input or A-bus I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54ABTE16245			SN74ABTE16245			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	B port	V_{CC} = 5.5 V,	I_{OH} = – 100 µA				V_{CC}–0.2			V_{CC}–0.2	V
		V_{CC} = 4.5 V	I_{OH} = – 1 mA		2.4			2.4			
			I_{OH} = – 12 mA		2			2			
	A port	V_{CC} = 5.5 V,	I_{OH} = – 1 mA				4.5			4.5	
		V_{CC} = 4.5 V	I_{OH} = – 32 mA		2.4			2.4			
			I_{OH} = – 64 mA					2			
V_{OL}	B port	V_{CC} = 4.5 V	I_{OL} = 1 mA				0.4			0.4	V
			I_{OL} = 12 mA							0.8	
	A port	V_{CC} = 4.5 V	I_{OL} = 64 mA				0.55			0.55	
			I_{OL} = 90 mA							0.9	
$I_{I(hold)}$	B port	V_{CC} = 4.5 V	V_I = 0.8 V		100			100			µA
			V_I = 2 V		–100			–100			
		V_{CC} = 5.5 V,	V_I = 0 to 5.5 V				±500			±500	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1			±1	µA
	A or B ports	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±20			±20	
I_{OZH}‡	A port	V_{CC} = 5.5 V,	V_O = 2.7 V				10			10	µA
I_{OZL}‡	A port	V_{CC} = 5.5 V,	V_O = 0.5 V				–10			–10	µA
I_O	A port	V_{CC} = 5.5 V,	V_O = 0		–50	–120	–180	–50		–180	µA
	B port				–25	–52	–90	–25		–90	
I_{off}		V_{CC} = 0, V_{CC}BIAS = 0	V_I or V_O ≤ 4.5 V,				±100			±100	µA
I_{CC}	A or B ports	V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		28	36		28	36	mA
				Outputs low		38	48		38	48	
				Outputs disabled		20	32		20	32	
I_{CCD}	A or B ports	V_{CC} = 5 V,	C_L = 50 pF	$\overline{OE}$ high		0.02			0.02		mA/ MHz
				$\overline{OE}$ low		0.33			0.33		
C_i	Control inputs	V_I = 2.5 V or 0.5 V				2.5	4		2.5	4	pF
C_{io}	I/O ports	V_O = 2.5 V or 0.5 V				4.5	8		4.5	8	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	SN54ABTE16245			SN74ABTE16245			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{CC} (V_{CC}BIAS)		V_{CC} = 0 to 4.5 V, V_{CC}BIAS = 4.5 V to 5.5 V, $I_{O(DC)}$ = 0		250	700		250	700	µA
		V_{CC} = 4.5 V to 5.5 V‡, V_{CC}BIAS = 4.5 V to 5.5 V, $I_{O(DC)}$ = 0			20			20	
V_O	A port	V_{CC} = 0, V_{CC}BIAS = 4.5 V to 5.5 V	1.1	1.5	1.9	1.1	1.5	1.9	V
		V_{CC} = 0, V_{CC}BIAS = 4.75 V to 5.25 V	1.3	1.5	1.7	1.3	1.5	1.7	
I_O	A port	V_{CC} = 0, V_O = 0, V_{CC}BIAS = 4.5 V	−20		−100	−20		−100	µA
		V_{CC} = 0, V_O = 3 V, V_{CC}BIAS = 4.5 V	20		100	20		100	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{CC} – 0.5 V < V_{CC}BIAS

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABTE16245		SN74ABTE16245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.5	3.3	4.2	1.5	5.4	1.5	5.2	ns
t_{PHL}			1.5	3.8	4.6	1.5	5.4	1.5	5.2	
t_{PLH}	B	A	1.5	3	3.8	1.5	4.7	1.5	4.5	ns
t_{PHL}			1.5	3.1	4	1.5	4.7	1.5	4.5	
t_{PZH}	$\overline{OE}$	A	2	3.9	5.3	2	6.4	2	6.2	ns
t_{PZL}			2	4.4	5.9	2	7	2	6.8	
t_{PZH}	$\overline{OE}$	B	2	4.5	6	2	7.3	2	7.1	ns
t_{PZL}			2	5	6.4	2	7.5	2	7.3	
t_{PHZ}	$\overline{OE}$	A	2	4.9	5.9	2	7	2	6.7	ns
t_{PLZ}			2	3.7	4.6	2	5.4	2	5.1	
t_{PHZ}	$\overline{OE}$	B	2	5.2	6.2	2	7.2	2	7	ns
t_{PLZ}			2	4	5	2	5.8	2	5.5	

extended switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 4 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD	V_{CC} = 5 V, T_A = 25°C			SN54ABTE16245		SN74ABTE16245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	B	A	R_X = 13 Ω	1.5	3.2	4	1.5	5	1.5	4.8	ns
t_{PHL}				1.5	3.8	4.7	1.5	5.8	1.5	5.6	
t_{PLH}	B	A	R_X = 26 Ω	1.5	3.1	4	1.5	4.8	1.5	4.6	ns
t_{PHL}				1.5	3.5	4.4	1.5	5.2	1.5	4.9	
t_{PLH}	B	A	R_X = 56 Ω	1.5	3	3.8	1.5	4.7	1.5	4.5	ns
t_{PHL}				1.5	3.3	4.2	1.5	5.1	1.5	4.7	
$t_{sk(p)}$	B	A	R_X = Open		0.1	0.6		2		2	ns
	A	B			0.4	0.8		2		2	
	B	A	R_X = 26 Ω		0.3	0.8		2		2	
$t_{sk(o)}$	B	A	R_X = Open		0.3	0.7		1.3		1.3	ns
	A	B			0.7	1.1		1.3		1.3	
	B	A	R_X = 26 Ω		0.5	1		1.3		1.3	
t_t†	B	A	R_X = 26 Ω	0.5	0.8	1.5	0.5	1.5	0.5	1.5	ns
t_t‡	A	B	Rise or fall time 10%–90%	3.5	5.5	7.3	3.5	8.1	3.5	7.9	ns

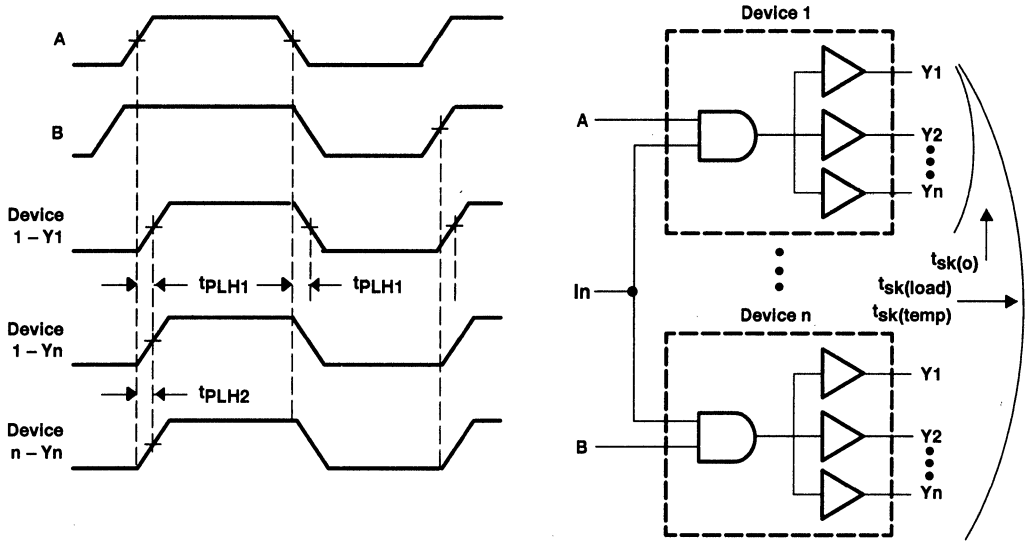
† t_r/t_f between V_O = 1 V/2 V
‡ t_r/t_f between 10% and 90% of output waveform
NOTE 4: Limits are specified but not tested.

extended output characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (see Note 4 and Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LOAD	SN54ABTE16245		SN74ABTE16245		UNIT
					MIN	MAX	MIN	MAX	
$t_{sk(temp)}$	A	B	V_{CC} = Constant, ΔT_A = 20°C			3		2.5	ns
	B	A		R_X = 56 Ω		4.5		4	
$t_{sk(load)}$	B	B	V_{CC} = Constant, Temperature = Constant	R_X = 13, 26, or 56 Ω		4.5		4	ns

NOTE 4: Limits are specified but not tested.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Pulse skew, $t_{sk(p)}$, is defined as the difference in propagation delay times t_{PLH1} and t_{PHL1} on the same terminal at identical operating conditions.

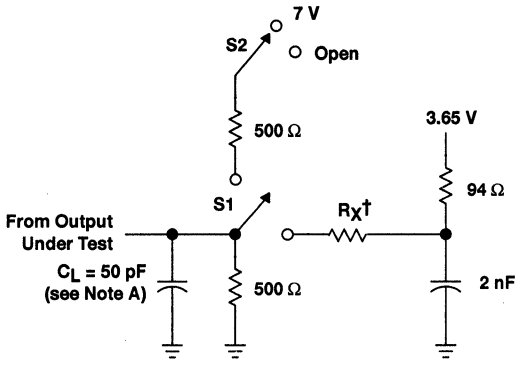
B. Output skew, $t_{sk(o)}$, is defined as the difference in propagation delay of the fastest and slowest paths on a single device that originate at either a single input or multiple simultaneously switched inputs, (e.g., $|t_{PLH1} - t_{PLH2}|$).

C. Temperature skew, $t_{sk(temp)}$, is the output skew of two devices, both having the same value of V_{CC} ± 1% and with package temperature differences of 20°C from each other.

D. Load skew, $t_{sk(load)}$, is measured with R_X in Figure 2 at 13 Ω for one unit and 56 Ω for the other unit.

Figure 1. Voltage Waveforms for Extended Characteristics

PARAMETER MEASUREMENT INFORMATION

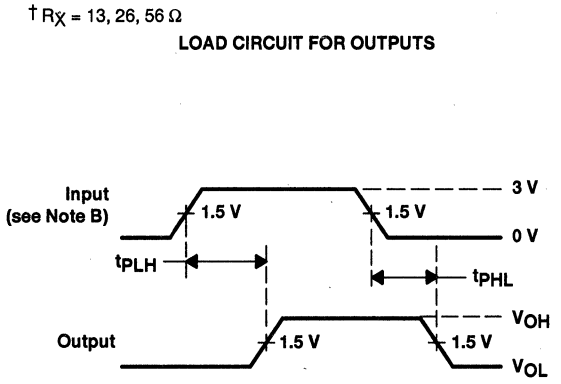


† RX = 13, 26, 56 Ω

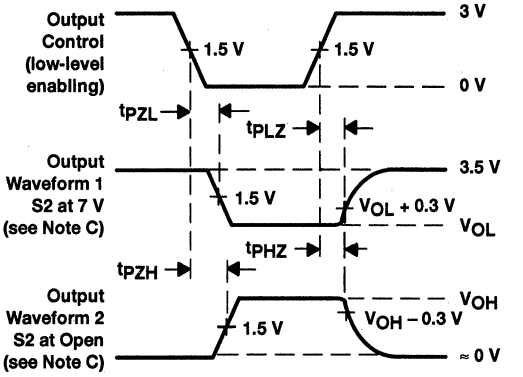
LOAD CIRCUIT FOR OUTPUTS

SWITCHING TABLE LOADS	S1	S2
t_{PLH}/t_{PHL} (A and B port)	Up	Open
t_{PLZ}/t_{PZL}	Up	7 V
t_{PHZ}/t_{PZH}	Up	Open

EXTENDED SWITCHING TABLE LOADS	S1	S2
$t_{PLH}/t_{PHL}/t_{sk}$ (A port)	Down	X
$t_{PLH}/t_{PHL}/t_{sk}$ (B port)	Up	Open
t_t (A port) (see Note E)	Down	X
t_t (B port) (see Note F)	Up	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



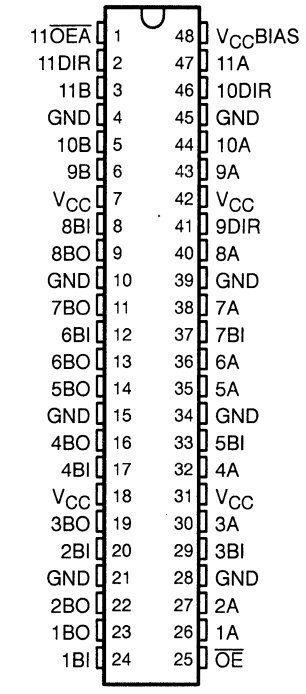
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.
E. t_t is measured at 1 V to 2 V.
F. t_t is measured at 10% to 90%.

Figure 2. Load Circuit and Voltage Waveforms

- **Supports the VME64 ETL Specification**
- **Reduced, TTL-Compatible, Input Threshold Range**
- **High-Drive Outputs (I_{OH} = –60 mA, I_{OL} = 90 mA) Support 25-Ω Incident-Wave Switching**
- **V_{CC}BIAS Pin Minimizes Signal Distortion During Live Insertion**
- **Internal Pullup Resistor on $\overline{OE}$ Keeps Outputs in High-Impedance State During Power Up or Power Down**
- **Members of the Texas Instruments *Widebus*™ Family**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **25-Ω Series Dampening Resistor on B Port**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-Mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABTE16246 . . . WD PACKAGE
SN74ABTE16246 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'ABTE16246 are 11-bit noninverting transceivers designed for synchronous two-way communication between buses. These devices consist of open-collector and 3-state outputs. They allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated. When $\overline{OE}$ is low, the device is active.

The B port has a 25-Ω series output resistor to reduce ringing. Active bus-hold inputs are also found on the B port to hold unused or floating inputs at a valid logic level.

The A port provides for the precharging of the outputs via V_{CC}BIAS, which establishes a voltage between 1.3 V and 1.7 V when V_{CC} is not connected.

The SN74ABTE16246 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABTE16246 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABTE16246 is characterized for operation from –40°C to 85°C.

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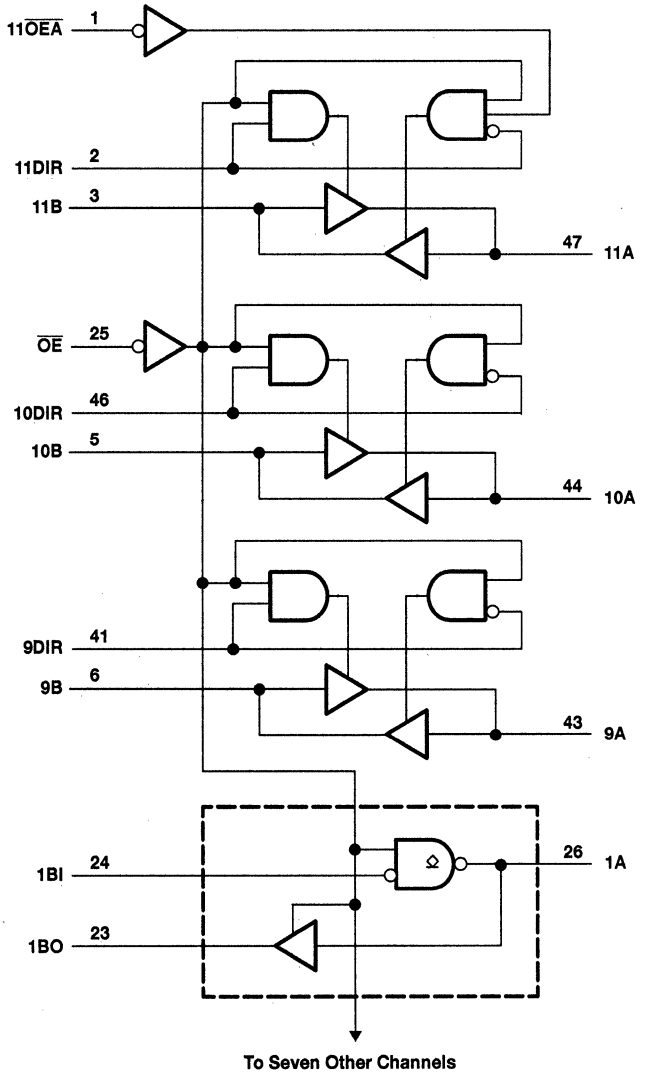
FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	A data to B bus
L	H	B data to A bus
H	X	Isolation

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −18 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

			SN54ABTE16246			SN74ABTE16246			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{OE}$	2			2			V
		Except $\overline{OE}$	1.6			1.6			
V_{IL}	Low-level input voltage	$\overline{OE}$			0.8			0.8	V
		Except $\overline{OE}$			1.4			1.4	
V_{OH}	High-level output voltage	1A–8A			5.5	0		5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	B bus			−12			−12	mA
		9A–11A			−24			−64	
I_{OL}	Low-level output current	B bus			12			12	mA
		A bus			64			90	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10			10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 3: Unused or floating pins (input or A-bus I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54ABTE16246			SN74ABTE16246			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	B port	V_{CC} = 5.5 V,	I_{OH} = − 100 µA				V_{CC}−0.2			V_{CC}−0.2	V
		V_{CC} = 4.5 V	I_{OH} = − 1 mA		2.4			2.4			
			I_{OH} = − 12 mA		2			2			
	9A–11A	V_{CC} = 5.5 V,	I_{OH} = − 1 mA				4.5			4.5	
		V_{CC} = 4.5 V	I_{OH} = − 32 mA		2.4			2.4			
			I_{OH} = − 64 mA					2			
I_{OH}	1A–8A	V_{CC} = 4.5 V,	V_{OH} = 5.5 V				20			20	µA
V_{OL}	B port	V_{CC} = 4.5 V	I_{OL} = 1 mA				0.4			0.4	V
			I_{OL} = 12 mA							0.8	
	A port	V_{CC} = 4.5 V	I_{OL} = 64 mA				0.55			0.55	
			I_{OL} = 90 mA							0.9	
$I_{I(hold)}$	B port	V_{CC} = 4.5 V	V_I = 0.8 V		100			100			µA
			V_I = 2 V		−100			−100			
		V_{CC} = 5.5 V,	V_I = 0 to 5.5 V				±500			±500	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1			±1	µA
	A or B ports						±20			±20	
I_{OZH}‡	9A–11A	V_{CC} = 5.5 V,	V_O = 2.7 V				10			10	µA
I_{OZL}‡	9A–11A	V_{CC} = 5.5 V,	V_O = 0.5 V				−10			−10	µA
I_O	A port	V_{CC} = 5.5 V,	V_O = 0		−50	−120	−180	−50		−180	µA
	B port				−25	−52	−90	−25		−90	
I_{off}		V_{CC} = 0, V_{CC}BIAS = 0	V_I or V_O ≤ 4.5 V,				±100			±100	µA
I_{CC}	A or B ports	V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		28	36		28	36	mA
				Outputs low		38	48		38	48	
				Outputs disabled		20	32		20	32	
I_{CCD}	A or B ports	V_{CC} = 5 V,	C_L = 50 pF	$\overline{OE}$ high		0.02			0.02		mA/ MHz
				$\overline{OE}$ low		0.33			0.33		
C_i	Control inputs	V_I = 2.5 V or 0.5 V				2.5	4		2.5	4	pF
C_{io}	I/O ports	V_O = 2.5 V or 0.5 V				4.5	8		4.5	8	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54ABTE16246			SN74ABTE16246			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{CC} (V_{CC}BIAS)		V_{CC} = 0 to 4.5 V, $I_{O(DC)}$ = 0	V_{CC}BIAS = 4.5 V to 5.5 V,		250	700		250	700	µA
		V_{CC} = 4.5 V to 5.5 V‡, $I_{O(DC)}$ = 0	V_{CC}BIAS = 4.5 V to 5.5 V,			20			20	
V_O	A port	V_{CC} = 0,	V_{CC}BIAS = 4.5 V to 5.5 V	1.1	1.5	1.9	1.1	1.5	1.9	V
		V_{CC} = 0,	V_{CC}BIAS = 4.75 V to 5.25 V	1.3	1.5	1.7	1.3	1.5	1.7	
I_O	A port	V_{CC} = 0, V_O = 0,	V_{CC}BIAS = 4.5 V	−20		−100	−20		−100	µA
		V_{CC} = 0, V_O = 3 V,	V_{CC}BIAS = 4.5 V	20		100	20		100	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{CC} – 0.5 V < V_{CC}BIAS

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABTE16246		SN74ABTE16246		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.5	3.1	4.2	1.5	5.4	1.5	5.2	ns
t_{PHL}			1.5	3.5	4.6	1.5	5.4	1.5	5.2	
t_{PLH}	9B–11B	9A–11A	1.5	3	3.8	1.5	4.7	1.5	4.5	ns
t_{PHL}			1.5	3.2	4	1.5	4.7	1.5	4.5	
t_{PLH}§	1B–8B	1A–8A	1.5	3.2	4	1.5	4.7	1.5	4.5	ns
t_{PLH}¶			7.5	8.9	9.7	7.5	10.6	7.5	10.3	ns
t_{PHL}			1.5	3.2	4	1.5	4.7	1.5	4.5	ns
t_{PZH}	$\overline{OE}$	9A–11A	2	4.3	5.3	2	6.4	2	6.2	ns
t_{PZL}		1A–11A	2	4.4	5.4	2	7	2	6.8	
t_{PZH}	$\overline{OE}$	B	2	4.3	6	2	7.3	2	7.1	ns
t_{PZL}			2	4.5	6.4	2	7.5	2	7.3	
t_{PHZ}	$\overline{OE}$	9A–11A	2	4.2	5.9	2	7	2	6.7	ns
t_{PLZ}		1A–11A	2	3.5	4.6	2	5.4	2	5.1	
t_{PHZ}	$\overline{OE}$	B	2.5	4.3	6.2	2.5	7.2	2.5	7	ns
t_{PLZ}			2	3.6	5	2	5.8	2	5.5	

§ Measurement point is V_{OL} + 0.3 V.
¶ Measurement point is V_{OL} + 1.5 V.

extended switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 4 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD	V_{CC} = 5 V, T_A = 25°C			SN54ABTE16246		SN74ABTE16246		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	9B–11B	9A–11A	R_X = 13 Ω	1.5	3.2	4	1.5	5	1.5	4.8	ns
t_{PHL}				1.5	3.8	4.7	1.5	5.8	1.5	5.6	
t_{PHL}	1B–8B	1A–8A	R_X = 13 Ω	1.5	3.3	4.2	1.5	5	1.5	4.8	ns
t_{PLH}	9B–11B	9A–11A	R_X = 26 Ω	1.5	3.1	4	1.5	4.8	1.5	4.6	ns
t_{PHL}				1.5	3.5	4.4	1.5	5.2	1.5	4.9	
t_{PHL}	1B–8B	1A–8A	R_X = 26 Ω	1.5	3.1	4	1.5	4.6	1.5	4.4	ns
t_{PLH}	9B–11B	1A–8A	R_X = 56 Ω	1.5	3	3.8	1.5	4.7	1.5	4.5	ns
t_{PHL}				1.5	3.3	4.2	1.5	5.1	1.5	4.7	
t_{PHL}	1B–8B	1A–8A	R_X = 56 Ω	1.5	3	4	1.5	4.6	1.5	4.4	ns
$t_{sk(p)}$	B	A	R_X = Open		0.1	0.6		2		2	ns
	A	B			0.4	0.8		2		2	
	B	A	R_X = 26 Ω		0.3	0.8		2		2	
$t_{sk(o)}$	B	A	R_X = Open		0.3	0.7		1.3		1.3	ns
	A	B			0.7	1.1		1.3		1.3	
	B	A	R_X = 26 Ω		0.5	1		1.3		1.3	
t_t†	B	A	R_X = 26 Ω	0.5	0.8	1.5	0.5	1.5	0.5	1.5	ns
t_t‡	A	B	Rise or fall time 10%–90%	3.5	5.5	7.3	3.5	8.1	3.5	7.9	ns

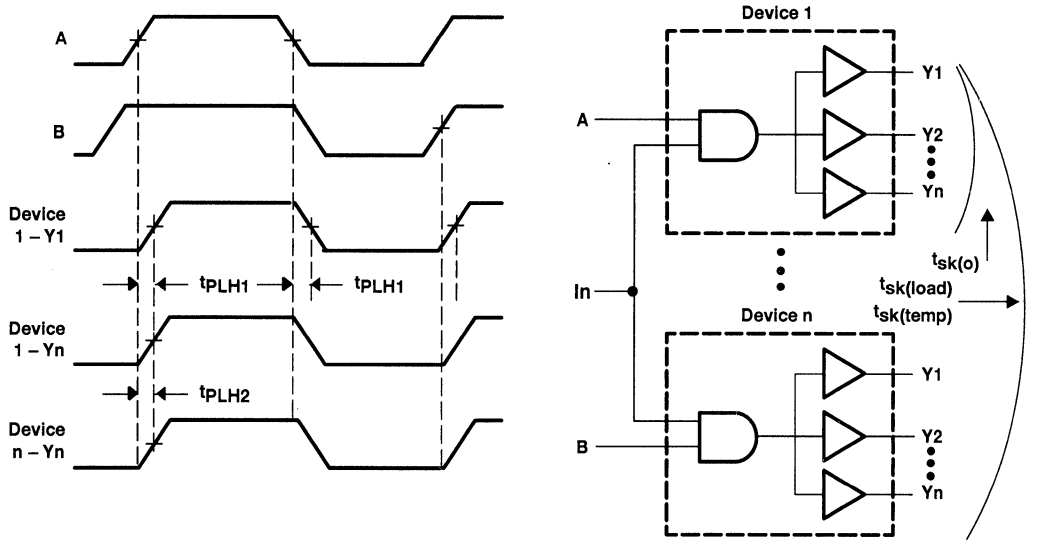
† t_r/t_f between V_O = 1 V/2 V.
‡ t_r/t_f between 10% and 90% of output waveform
NOTE 4: Limits are specified but not tested.

extended output characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (see Note 4 and Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LOAD	SN54ABTE16246		SN74ABTE16246		UNIT
					MIN	MAX	MIN	MAX	
$t_{sk(temp)}$	A	B	V_{CC} = Constant, ΔT_A = 20°C			3		2.5	ns
	B	A		R_X = 56 Ω		4.5		4	
$t_{sk(load)}$	B	A	V_{CC} = Constant, Temperature = Constant	R_X = 13, 26, or 56 Ω		4.5		4	ns

NOTE 4: Limits are specified but not tested.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Pulse skew, $t_{sk(p)}$, is defined as the difference in propagation delay times t_{PLH1} and t_{PHL1} on the same terminal at identical operating conditions.

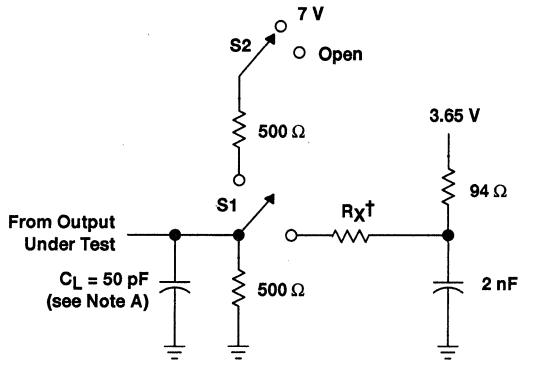
B. Output skew, $t_{sk(o)}$, is defined as the difference in propagation delay of the fastest and slowest paths on a single device that originate at either a single input or multiple simultaneously switched inputs, (e.g., $|t_{PLH1} - t_{PLH2}|$).

C. Temperature skew, $t_{sk(temp)}$, is the output skew of two devices, both having the same value of V_{CC} ±1% and with package temperature differences of 20°C from each other.

D. Load skew, $t_{sk(load)}$, is measured with R_X in Figure 2 at 13 Ω for one unit and 56 Ω for the other unit.

Figure 1. Voltage Waveforms for Extended Characteristics

PARAMETER MEASUREMENT INFORMATION

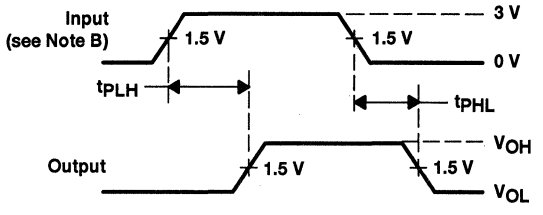


† R_X = 13, 26, 56 Ω

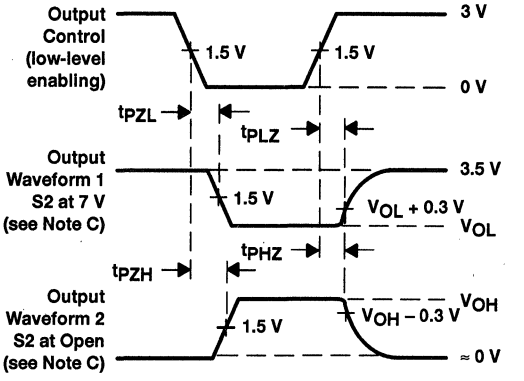
LOAD CIRCUIT FOR OUTPUTS

SWITCHING TABLE LOADS	S1	S2
t_{PLH}/t_{PHL} (9A – 11A and B port)	Up	Open
t_{PLH}/t_{PHL} (1A – 8A)	Up	7 V
t_{PLZ}/t_{PZL}	Up	7 V
t_{PHZ}/t_{PZH} (except 1A – 8A)	Up	Open

EXTENDED SWITCHING TABLE LOADS	S1	S2
$t_{PLH}/t_{PHL}/t_{sk}$ (A port)	Down	X
$t_{PLH}/t_{PHL}/t_{sk}$ (B port)	Up	Open
t_t (A port) (see Note E)	Down	X
t_t (B port) (see Note F)	Up	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



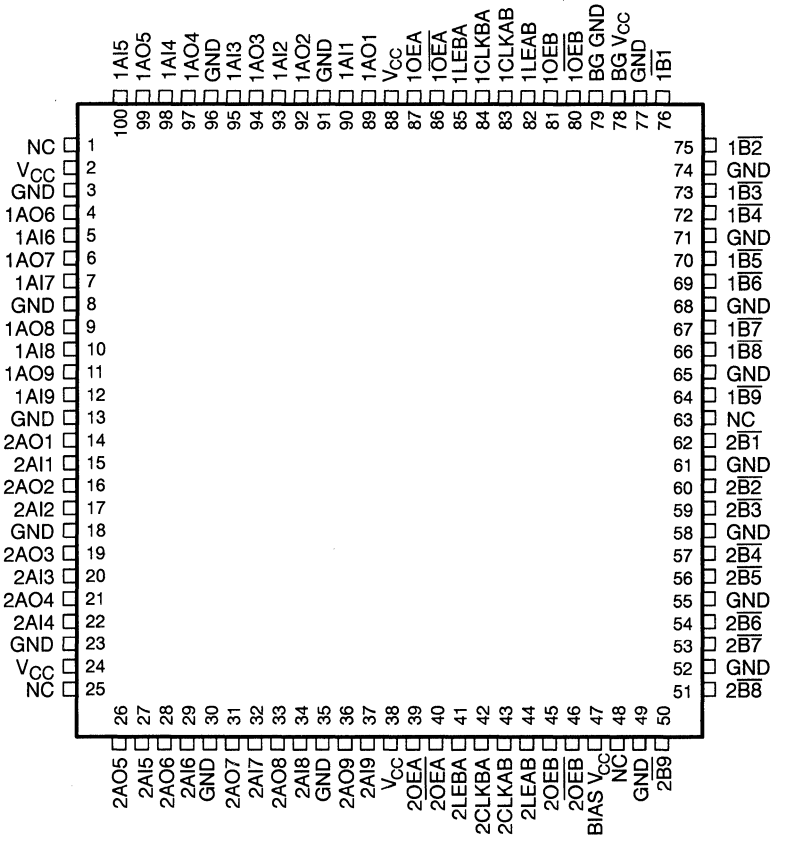
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.
E. t_t is measured at 1 V to 2 V.
F. t_t is measured at 10% to 90%.

Figure 2. Load Circuit and Voltage Waveforms

- **Compatible With IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) Standards**
- **TTL A Port, Backplane Transceiver Logic $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **Isolated Logic-Ground and Bus-Ground Pins Reduce Noise**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage**
- **TTL Input Structures Incorporate Active Clamping and Bus-Hold Networks**
- **Package Options Include High-Power Shrink Quad Flat (PCA) Package With 0.5-mm Pin Pitch and Ceramic Quad Flat (HQA) Package**

SN54FB1650 . . . HQA PACKAGE
SN74FB1650 . . . PCA PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

description

The 'FB1650 contains two 9-bit transceivers designed to translate signals between TTL and backplane transceiver logic (BTL) environments. They are specifically designed to be compatible with IEEE 1194.1-1 (BTL) and IEEE 896.2-1991 (Futurebus+) standards.

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA. Two output enables, OEB and $\overline{OEB}$, are provided for the $\overline{B}$ outputs. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is typically less than 2.5 V, the $\overline{B}$ port is turned off.

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable, OEA, is high. When OEA is low or when V_{CC} is typically less than 2.5 V, the A outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating TTL inputs at a valid logic state.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

BG V_{CC} and BG GND are the supply inputs for the bias generator.

The SN54FB1650 is characterized for operation over the full military temperature range of –55°C to 125°C.The SN74FB1650 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

Function Tables

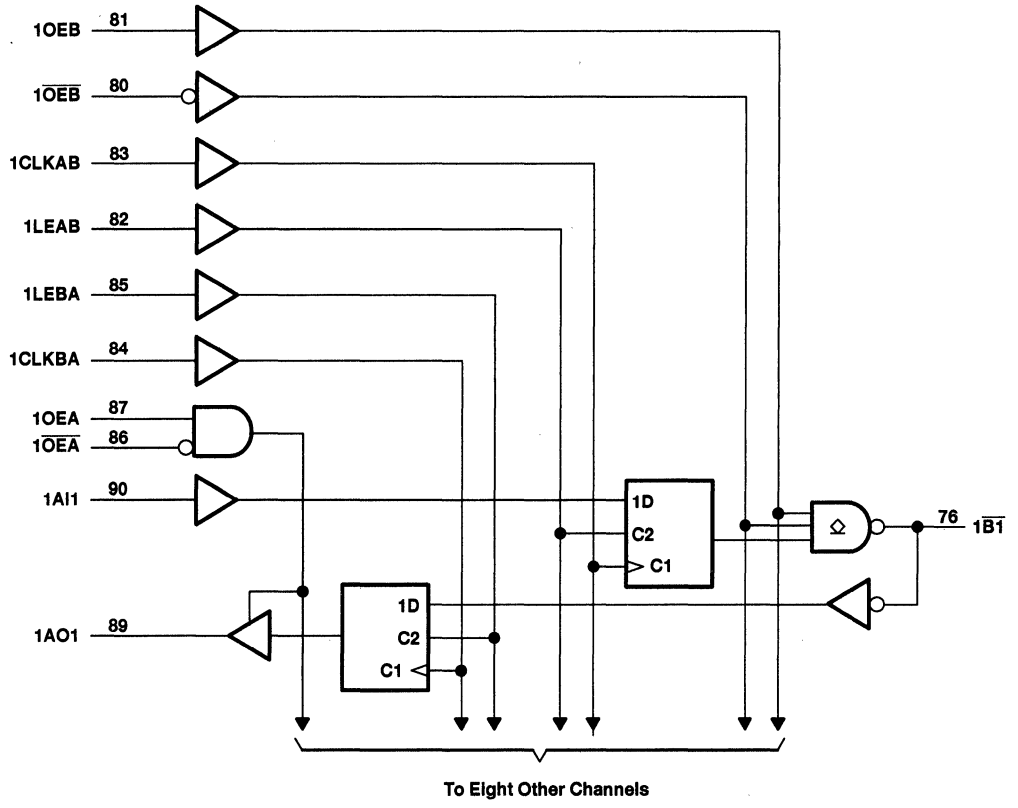
TRANSCEIVER

INPUTS				FUNCTION
$\overline{OEA}$	OEA	OEB	$\overline{OEB}$	
X	X	H	L	$\overline{A}$ data to B bus
L	H	X	X	$\overline{B}$ data to A bus
L	H	H	L	$\overline{A}$ data to B bus, $\overline{B}$ data to A bus
X	X	L	X	B-bus isolation
X	X	X	H	
H	X	X	X	A-bus isolation
X	L	X	X	

STORAGE MODE

INPUTS		FUNCTION
LE	CLK	
H	X	Transparent
L	↑	Store data
L	L	Storage

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}, BIAS V_{CC}, BG V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I: except $\overline{B}$ port ..... −1.2 V to 7 V
$\overline{B}$ port ..... −1.2 V to 3.5 V
Input current range (except $\overline{B}$ port) ..... −40 mA to 5 mA
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to V_{CC}
Current applied to any single output in the low state: A port ..... 48 mA
$\overline{B}$ port ..... 200 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 1): PCA package ..... 1.8 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

PRODUCT PREVIEW

recommended operating conditions (see Note 2)

			SN54FB1650			SN74FB1650			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}, BG V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
BIAS V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62		2.3	1.62		2.3	V
		Except $\overline{B}$ port	2			2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47	0.75		1.47	V
		Except $\overline{B}$ port			0.8			0.8	
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	A port			−3			−3	mA
I_{OL}	Low-level output current	A port			24			24	mA
		$\overline{B}$ port			100			100	
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54FB1650			SN74FB1650			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	AO port	V_{CC} = 4.5 V	I_{OH} = −1 mA							V
			I_{OH} = −3 mA	2.5	3.3		2.5	3.3		
V_{OL}	AO port	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5		0.35	0.5	V
	$\overline{B}$ port	V_{CC} = 4.5 V	I_{OL} = 80 mA	0.75		1.1	0.75		1.1	
			I_{OL} = 100 mA			1.15			1.15	
I_I	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 5.5 V			50			50	µA
I_{IH}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 2.7 V			50			50	µA
I_{IL}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.5 V			−50			−50	µA
	$\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.75 V			−100			−100	
I_{OZH}	AO port	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}	AO port	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	µA
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V			100			100	µA
I_{OS}§	A port	V_{CC} = 5.5 V,	V_O = 0	−30		−150	−30		−150	mA
I_{CC}	A port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0		25			25		mA
	$\overline{B}$ port to A port				60			60		
	Outputs disabled									
C_i		V_I = V_{CC} or GND				5			5	pF
C_o	A port	V_O = V_{CC} or GND								pF
C_{io}	$\overline{B}$ port per P1194.0	V_{CC} = 0 to 4.5 V				6			6	pF
		V_{CC} = 4.5 V to 5.5 V				5			5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

PRODUCT PREVIEW

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54FB1650		SN74FB1650		UNIT
				MIN	MAX	MIN	MAX	
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		450		450	μA
		V_{CC} = 4.5 V to 5.5 V			10		10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	1.62	2.1	1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0, V_B = 1 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	–1		–1		μA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V		100		100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V		100		100	

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54FB1650		SN74FB1650		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency						MHz
t_w	Pulse duration	LE high					ns
		CLK high or low					
t_{su}	Setup time	AI or $\overline{B}$ before LE		2		2	ns
		AI or $\overline{B}$ before CLK↑		2		2	
t_h	Hold time	AI or $\overline{B}$ after LE		1		1	ns
		AI or $\overline{B}$ after CLK↑		1		1	

PRODUCT PREVIEW

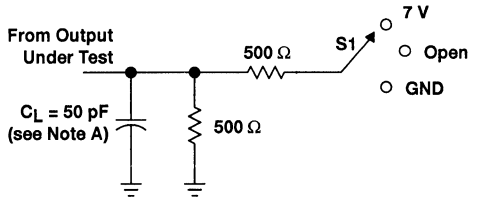
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54FB1650			SN74FB1650			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	AI	$\overline{B}$			5			5	ns
t_{PHL}					5			5	
t_{PLH}	LEAB	$\overline{B}$			6			6	ns
t_{PHL}					6			6	
t_{PLH}	CLKAB	$\overline{B}$			6			6	ns
t_{PHL}					6			6	
t_{PLH}	LEBA	AO			6			6	ns
t_{PHL}					6			6	
t_{PLH}	CLKBA	AO			6			6	ns
t_{PHL}					6			6	
t_{PLH}	$\overline{B}$	AO			5			5	ns
t_{PHL}					5			5	
t_{PLH}	OEB or $\overline{OEB}$	$\overline{B}$			5			5	ns
t_{PHL}					5			5	
t_{PZH}	OEA or $\overline{OEA}$	AO			5			5	ns
t_{PZL}					5			5	
t_{PHZ}	OEA or $\overline{OEA}$	AO			5			5	ns
t_{PLZ}					5			5	
$t_{sk(p)}$‡	Skew for any single channel $\lvert t_{PHL} - t_{PLH} \rvert$	AI to $\overline{B}$ or $\overline{B}$ to AO		0.5			0.5		ns
$t_{sk(o)}$‡	Skew between drivers in the same package	AI to $\overline{B}$ or $\overline{B}$ to AO		1			1		ns
t_t	Transition time, $\overline{B}$ outputs (1.3 V to 1.8 V)		1	2	3	1	2	3	ns
	Transition time, AO outputs (10% to 90%)								
t_{PR}	$\overline{B}$-port input pulse rejection			1			1		ns

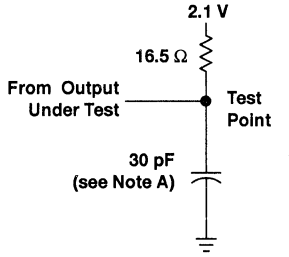
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Skew values are applicable for through mode only.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

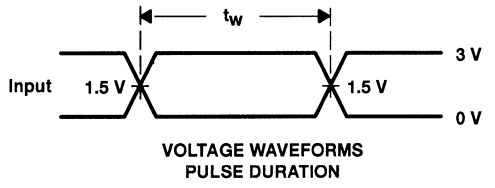


LOAD CIRCUIT FOR A OUTPUTS

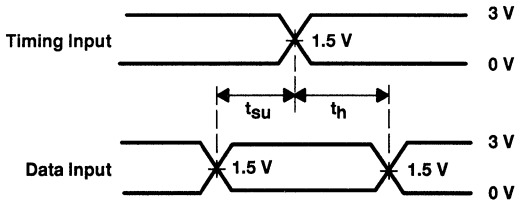


LOAD CIRCUIT FOR B OUTPUTS

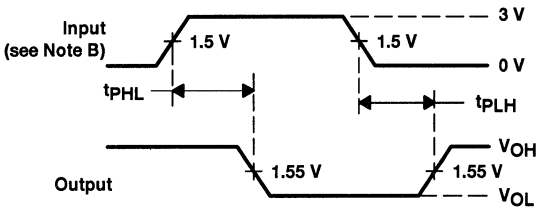
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



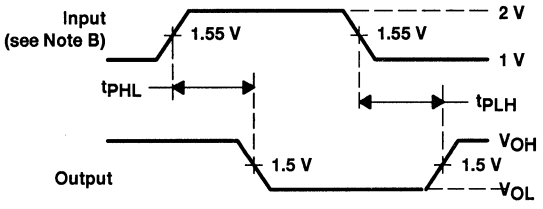
VOLTAGE WAVEFORMS
PULSE DURATION



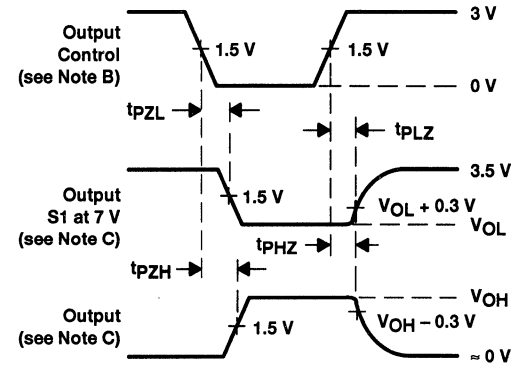
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)

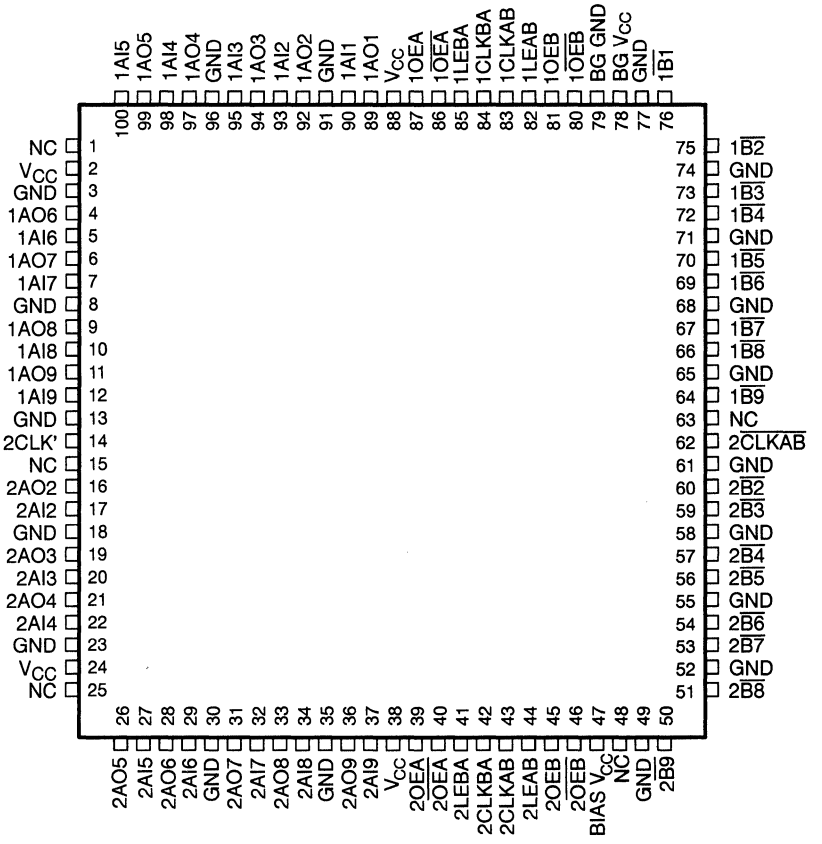
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: TTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns. BTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PRODUCT PREVIEW

- Compatible With IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) Standards
- TTL A Port, Backplane Transceiver Logic $\overline{B}$ Port
- Open-Collector $\overline{B}$-Port Outputs Sink 100 mA
- Isolated Logic-Ground and Bus-Ground Pins Reduce Noise
- $\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage
- TTL-Input Structures Incorporate Active Clamping and Bus-Hold Networks
- Package Options Include High-Power Shrink Quad Flat (PCA) Package With 0.5-mm Pin Pitch and Ceramic Quad Flat (HQA) Package

SN54FB1651 . . . HQA PACKAGE
SN74FB1651 . . . PCA PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

description

The 'FB1651 contains an 8-bit and a 9-bit transceiver with a buffered clock. The clock and the transceivers are designed to translate signals between TTL and backplane transceiver logic (BTL) environments. They are specifically designed to be compatible with IEEE 1194.1-1 (BTL) and IEEE 896.2-1991 (Futurebus+) standards.

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA. Two output enables, OEB and $\overline{OEB}$, are provided for the $\overline{B}$ outputs. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is typically less than 2.5 V, the $\overline{B}$ port is turned off.

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable, OEA, is high. When OEA is low or when V_{CC} is typically less than 2.5 V, the A outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating TTL inputs at a valid logic state.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

BG V_{CC} and BG GND are the supply inputs for the bias generator.

The SN54FB1651 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74FB1651 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

Function Tables

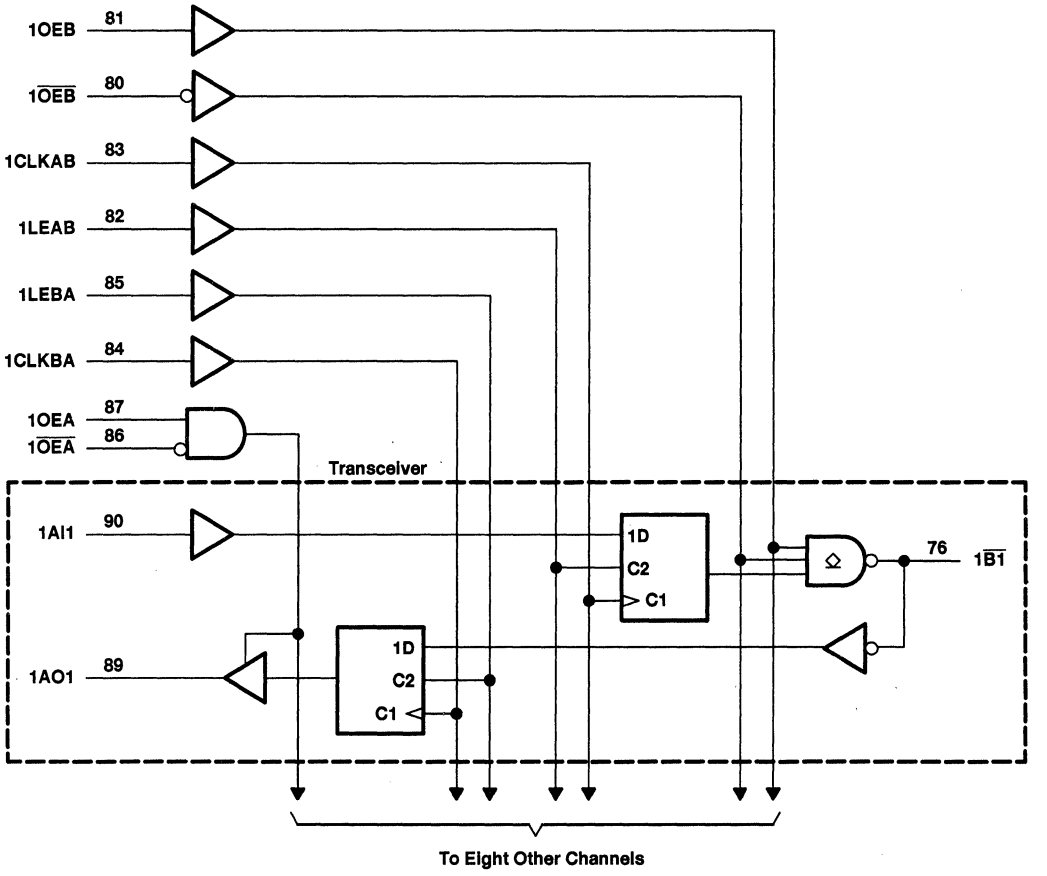
TRANSCEIVER

INPUTS				FUNCTION
$\overline{OEA}$	OEA	OEB	$\overline{OEB}$	
X	X	H	L	$\overline{A}$ data to B bus
L	H	X	X	$\overline{B}$ data to A bus
L	H	H	L	$\overline{A}$ data to B bus, $\overline{B}$ data to A bus
X	X	L	X	B-bus isolation
X	X	X	H	
H	X	X	X	A-bus isolation
X	L	X	X	

STORAGE MODE

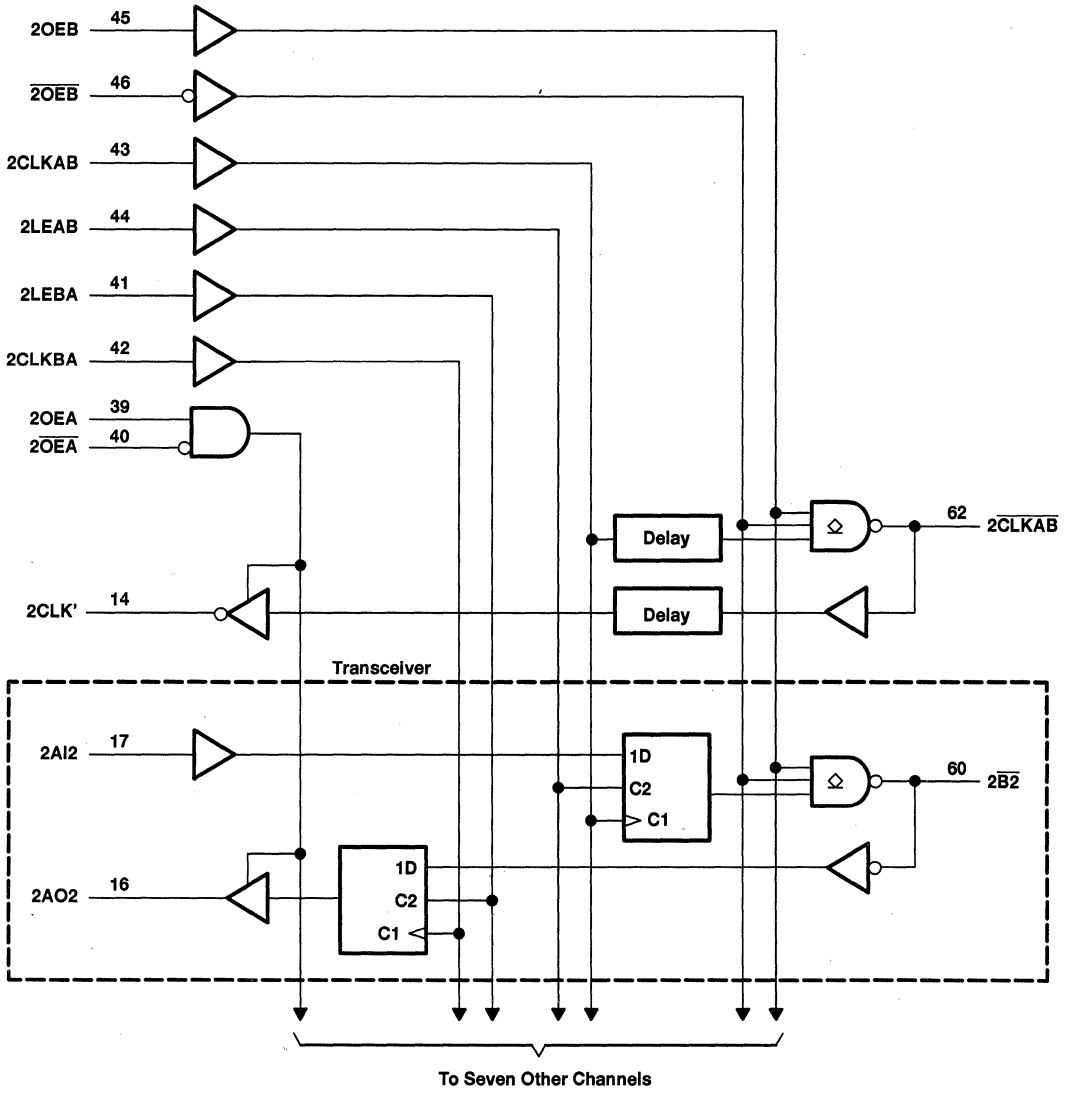
INPUTS		FUNCTION
LE	CLK	
H	X	Transparent
L	↑	Store data
L	L	Storage

functional block diagram



PRODUCT PREVIEW

functional block diagram (continued)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}, BIAS V_{CC}, BG V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I: except $\overline{B}$ port ..... −1.2 V to 7 V
$\overline{B}$ port ..... −1.2 V to 3.5 V
Input current range (except $\overline{B}$ port) ..... −40 mA to 5 mA
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to V_{CC}
Current applied to any single output in the low state: A port ..... 48 mA
$\overline{B}$ port ..... 200 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 1): PCA package ..... 1.8 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 2)

			SN54FB1651			SN74FB1651			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}, BG V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
BIAS V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62		2.3	1.62		2.3	V
		Except $\overline{B}$ port	2			2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47	0.75		1.47	V
		Except $\overline{B}$ port			0.8			0.8	
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	A port			−3			−3	mA
I_{OL}	Low-level output current	A port			24			24	mA
		$\overline{B}$ port			100			100	
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54FB1651			SN74FB1651			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	AO port	V_{CC} = 4.5 V	I_{OH} = –1 mA							V
			I_{OH} = –3 mA	2.5	3.3		2.5	3.3		
V_{OL}	AO port	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5		0.35	0.5	V
	$\overline{B}$ port	V_{CC} = 4.5 V	I_{OL} = 80 mA	0.75		1.1	0.75		1.1	
			I_{OL} = 100 mA			1.15			1.15	
I_I	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 5.5 V			50			50	µA
I_{IH}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 2.7 V			50			50	µA
I_{IL}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.5 V			–50			–50	µA
	$\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.75 V			–100			–100	
I_{OZH}	AO port	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}	AO port	V_{CC} = 5.5 V,	V_O = 0.5 V			–50			–50	µA
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V			100			100	µA
I_{OS}§	A port	V_{CC} = 5.5 V,	V_O = 0	–30		–150	–30		–150	mA
I_{CC}	A port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0		25			25		mA
	$\overline{B}$ port to A port				60			60		
	Outputs disabled									
C_i		V_I = V_{CC} or GND				5			5	pF
C_o	A port	V_O = V_{CC} or GND								pF
C_{io}	$\overline{B}$ port per P1194.0	V_{CC} = 0 to 4.5 V				6			6	pF
		V_{CC} = 4.5 V to 5.5 V				5			5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54FB1651		SN74FB1651		UNIT
				MIN	MAX	MIN	MAX	
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V,	V_B = 0 to 2 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		450		450	µA
		V_{CC} = 4.5 V to 5.5 V			10		10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	1.62	2.1	1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0,	V_B = 1 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	–1		–1		µA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V		100		100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V		100		100	

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54FB1651		SN74FB1651		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency						MHz
t_w	Pulse duration	LE high					ns
		CLK high or low					
t_{su}	Setup time	AI or $\overline{B}$ before LE		2		2	ns
		AI or $\overline{B}$ before CLK↑		2		2	
t_h	Hold time	AI or $\overline{B}$ after LE		1		1	ns
		AI or $\overline{B}$ after CLK↑		1		1	

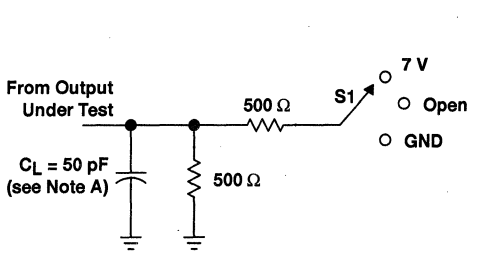
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54FB1651			SN74FB1651			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	AI	$\overline{B}$			5			5	ns
t_{PHL}					5			5	
t_{PLH}	LEAB	$\overline{B}$			6			6	ns
t_{PHL}					6			6	
t_{PLH}	CLKAB	$\overline{B}$	2.4		6.5	2.4		6.5	ns
t_{PHL}			2.2		6.5	2.2		6.5	
t_{PLH}	2CLKAB	$2\overline{CLKAB}$	3.9		10.2	3.9		10.2	ns
t_{PHL}			3.8		10.1	3.8		10.1	
t_{PLH}	LEBA	AO			6			6	ns
t_{PHL}					6			6	
t_{PLH}	CLKBA	AO			6			6	ns
t_{PHL}					6			6	
t_{PLH}	$\overline{B}$	AO			5			5	ns
t_{PHL}					5			5	
t_{PLH}	2CLKAB	2CLK'	4.3		12.7	4.3		12.7	ns
t_{PHL}			4.5		12.4	4.5		12.4	
t_{PLH}	OEB or $\overline{OEB}$	$\overline{B}$			5			5	ns
t_{PHL}					5			5	
t_{PZH}	OEA or $\overline{OEA}$	AO			5			5	ns
t_{PZL}					5			5	
t_{PHZ}	OEA or $\overline{OEA}$	AO			5			5	ns
t_{PLZ}					5			5	
$t_{sk(p)}$‡	Skew for any single channel $\lvert t_{PHL} - t_{PLH} \rvert$	AI to $\overline{B}$ or $\overline{B}$ to AO		0.5			0.5		ns
$t_{sk(o)}$‡	Skew between drivers in the same package	AI to $\overline{B}$ or $\overline{B}$ to AO		1			1		ns
t_t	Transition time, $\overline{B}$ outputs (1.3 V to 1.8 V)		1	2	3	1	2	3	ns
	Transition time, AO outputs (10% to 90%)								
t_{PR}	$\overline{B}$-port input pulse rejection			1			1		ns

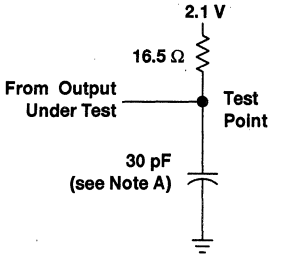
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Skew values are applicable for through mode only.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

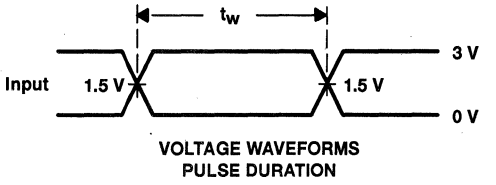


LOAD CIRCUIT FOR A OUTPUTS

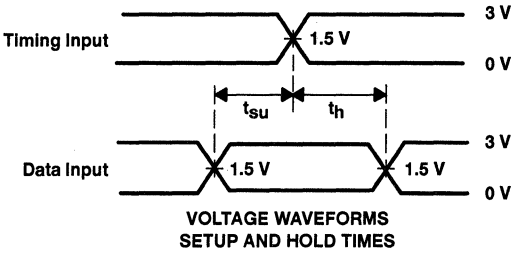


LOAD CIRCUIT FOR B OUTPUTS

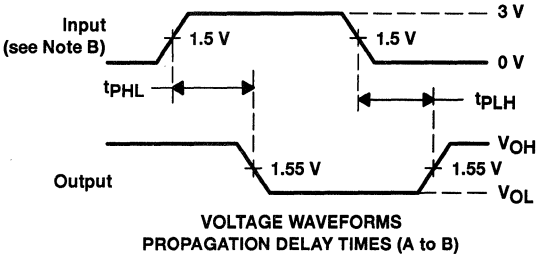
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



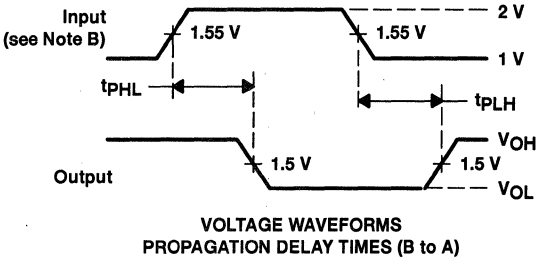
VOLTAGE WAVEFORMS
PULSE DURATION



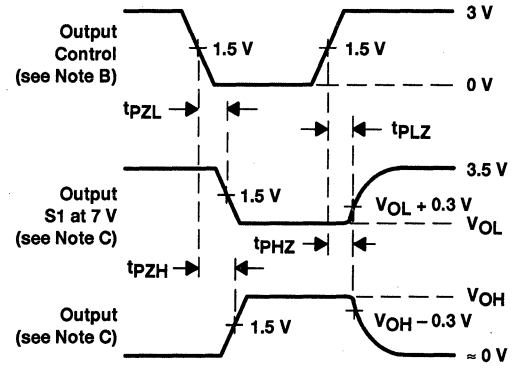
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)



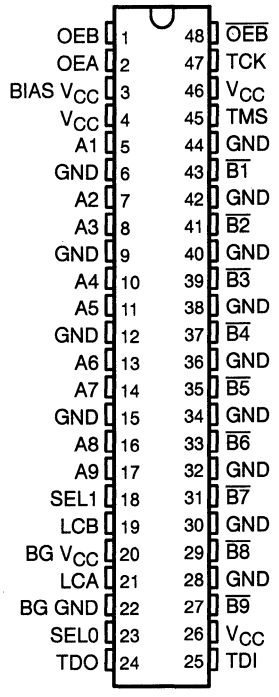
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: TTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns. BTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

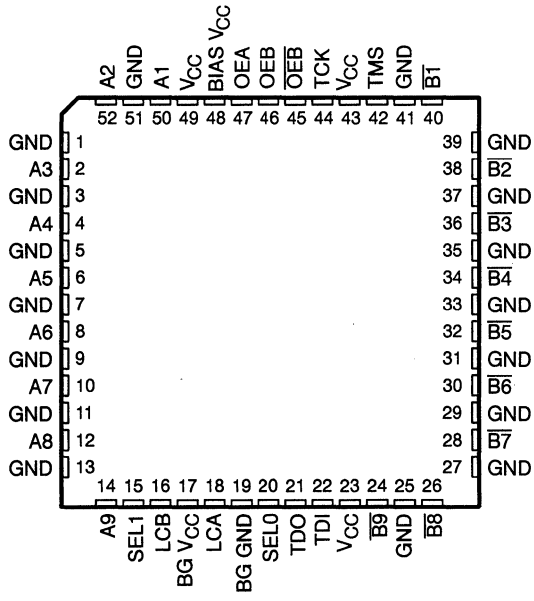
Figure 1. Load Circuits and Voltage Waveforms

- **Compatible With IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) Standards**
- **TTL A Port, Backplane Transceiver Logic $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **Minimum $\overline{B}$-Port Edge Rate = 2 ns**
- **Isolated Logic-Ground and Bus-Ground Pins Reduce Noise**
- **BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion/Withdrawal**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage**
- **TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination**
- **Package Options Include Plastic Quad Flat (RC) Package and Ceramic Flat (WD) Package**

SN54FB2031 . . . WD PACKAGE
(TOP VIEW)



SN74FB2031 . . . RC PACKAGE
(TOP VIEW)



description

The 'FB2031 are 9-bit transceivers designed to translate signals between TTL and backplane transceiver logic (BTL) environments. They are specifically designed to be compatible with IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) standards.

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA and have minimum output edge rates of 2 ns. Two output enables, OEB and $\overline{OEB}$, are provided for the $\overline{B}$ outputs. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is typically less than 2.5 V, the $\overline{B}$ port is turned off.

description (continued)

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable, OEA, is high. When OEA is low or V_{CC} is typically less than 2.5 V, the A outputs are in the high-impedance state.

Pins are allocated for the four-wire IEEE 1149.1 (JTAG) test bus, which will be implemented in a future version of the 'FB2031. Currently, TMS and TCK are not connected and TDI is shorted to TDO.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

BG V_{CC} and BG GND are the supply inputs for the bias generator.

The SN54FB2031 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74FB2031 is characterized for operation from 0°C to 70°C.

Function Tables

TRANSCEIVER

INPUTS			FUNCTION
OEA	OEB	$\overline{OEB}$	
L	H	L	$\overline{A}$ data to B bus
H	L	X	$\overline{B}$ data to A bus
H	X	H	
H	H	L	$\overline{A}$ data to B bus, $\overline{B}$ data to A bus
L	L	X	Isolation
L	X	H	

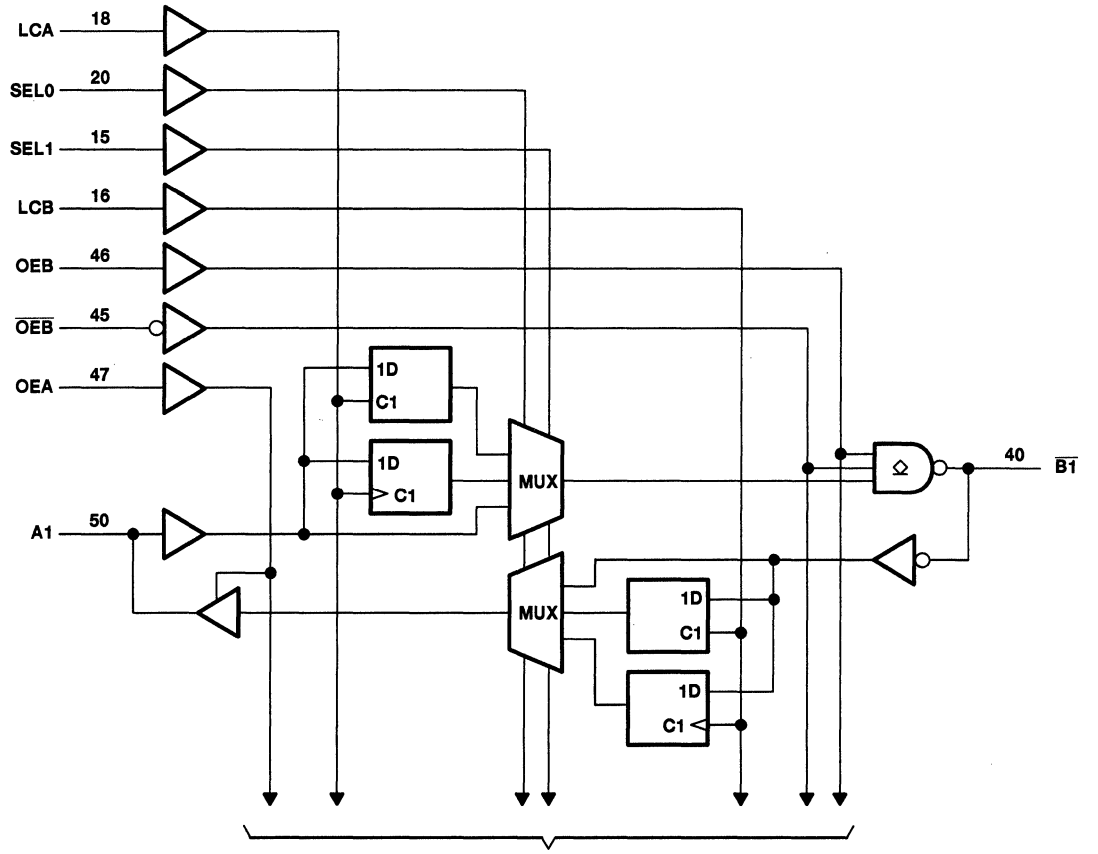
STORAGE MODE

LCA, LCB	RESULT
0	Transparent
1	Latches latched
↑	Flip-flops triggered

SELECT

SEL1	SEL0	MUX A→B	MUX B→A
0	0	Latch	Latch
0	1	Thru	Thru
1	0	Flip-flop	Flip-flop
1	1	Flip-flop	Latch

functional block diagram



Pin numbers shown are for the RC package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I: except $\overline{B}$ port ..... −1.2 V to 7 V
$\overline{B}$ port ..... −1.2 V to 3.5 V
Input current range (except $\overline{B}$ port) ..... −40 mA to 5 mA
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to V_{CC}
Current applied to any single output in the low state: A port ..... 48 mA
$\overline{B}$ port ..... 200 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 1): RC package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 2)

			SN54FB2031			SN74FB2031			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}, BIAS V_{CC}, BG V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62*		2.3	1.62		2.3	V
		Except $\overline{B}$ port	2			2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47*	0.75		1.47	V
		Except $\overline{B}$ port			0.8			0.8	
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	A port			−3			−3	mA
I_{OL}	Low-level output current	A port			24			24	mA
		$\overline{B}$ port			100			100	
T_A	Operating free-air temperature		−55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not tested.

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54FB2031			SN74FB2031			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$\overline{B}$ port	V_{CC} = 4.5 V	I_I = −18 mA			−1.2			−1.2	V
	Except $\overline{B}$ port		I_I = −40 mA			−0.5			−0.5	
V_{OH}	A port	V_{CC} = 4.5 V	I_{OH} = −1 mA		3.2					V
			I_{OH} = −3 mA	2.5	3.3		2.5	3.3		
V_{OL}	A port	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.31					V
			I_{OL} = 24 mA		0.35	0.5		0.35	0.5	
	$\overline{B}$ port	V_{CC} = 4.5 V	I_{OL} = 80 mA	0.75		1.1	0.75		1.1	
			I_{OL} = 100 mA			1.15			1.15	
I_I	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 5.5 V			50			50	µA
I_{IH}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 2.7 V			50			50	µA
I_{IL}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.5 V			−50			−50	µA
	$\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.75 V			−100			−100	
I_{OZH}	A port	V_{CC} = 2.1 V to 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}	A port	V_{CC} = 2.1 V to 5.5 V,	V_O = 0.5 V			−50			−50	µA
I_{OZPU}	A port	V_{CC} = 0 to 2.1 V,	V_O = 0.5 V to 2.7 V			50			50	µA
I_{OZPD}	A port	V_{CC} = 2.1 V to 0,	V_O = 0.5 V to 2.7 V			−50			−50	µA
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V			100			100	µA
I_{OS}§	A port	V_{CC} = 5.5 V,	V_O = 0	−30		−150	−30		−150	mA
I_{CC}	A port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0			78			78	mA
	$\overline{B}$ port to A port					78			78	
C_i		V_I = 0.5 V or 2.5 V			4.5			4.5		pF
C_{io}¶	A port	V_O = 0.5 V or 2.5 V			8.5			8.5		pF
	$\overline{B}$ port per P1194.0	V_{CC} = 0 to 5.5 V				6			6	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
¶ Parameter is based on characterization but is not tested.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54FB2031		SN74FB2031		UNIT
				MIN	MAX	MIN	MAX	
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		450		450	µA
		V_{CC} = 4.5 V to 5.5 V			10		10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 5 V	1.62	2.1	1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0,	V_B = 1 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	−30		−1		µA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V		100		100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V		100		100	

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

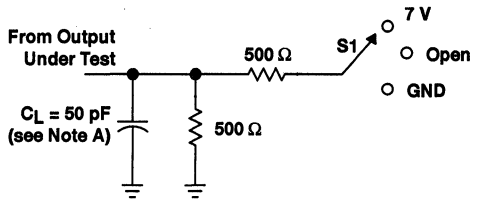
		SN54FB2031		SN74FB2031		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0		0	150	MHz
t_w	Pulse duration, LCA or LCB	3.3		3.3		ns
t_{su}	Setup time , data before LCA↑ (clock mode)	1.5		1.4		ns
	Setup time , data before LCB↑ (clock mode)	2.8		2.8		
	Setup time , data before LCA↑ (latch mode)	1.1		1.1		
	Setup time , data before LCB↑ (latch mode)	2.4		2.4		
t_h	Hold time , data before LCA↑ (clock mode)	0.6		0.6		ns
	Hold time , data before LCB↑ (clock mode)	0		0		
	Hold time , data before LCA↑ (latch mode)	0.9		0.9		
	Hold time , data before LCB↑ (latch mode)	0		0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

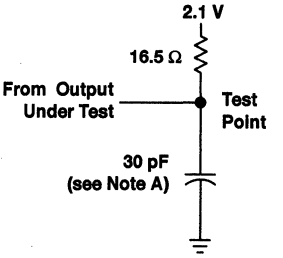
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54FB2031		SN74FB2031		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
f_{max}					150		150		150	MHz
t_{PLH}	A (thru mode)	$\overline{B}$	3.7	4.5	5.9	3.2	8	3.2	6.6	ns
t_{PHL}			2.9	4	5.7	2.6	7.8	2.6	5.9	
t_{PLH}	A (transparent)	$\overline{B}$	4.1	5	6.5	3.6	8.6	3.6	7.3	ns
t_{PHL}			3.3	4.5	6.1	3	8.3	3	6.5	
t_{PLH}	LCA	$\overline{B}$	4.5	5.4	7	3.9	9.1	3.9	7.8	ns
t_{PHL}			4	5.1	6.7	3.4	9	3.4	7.4	
t_{PLH}	LCB	A	2.8	3.7	4.7	1.9	7.9	1.9	6	ns
t_{PHL}			2.5	3.4	4.9	1.8	7.4	1.8	5.5	
t_{PLH}	SEL1 or SEL0	A	2.5	3.8	5.3	1.9	7.9	1.9	6.3	ns
t_{PHL}			2.2	3.5	5.1	1.6	7.1	1.6	5.6	
t_{PLH}	SEL1 or SEL0	$\overline{B}$	4.1	5.3	6.9	3.7	9.3	3.7	7.8	ns
t_{PHL}			3.7	5.2	6.9	3.3	9.2	3.3	7.7	
t_{PLH}	$\overline{B}$ (thru mode)	A	3.1	4	5.6	2.2	8.6	2.2	7.1	ns
t_{PHL}			2.6	3.4	4.9	1.4	7.6	1.4	5.7	
t_{PLH}	$\overline{B}$ (transparent)	A	3.3	4.2	5.9	2.4	9	2.4	7.6	ns
t_{PHL}			2.8	3.9	5.5	1.8	8.2	1.8	6.3	
t_{PLH}	OEB or $\overline{OEB}$	$\overline{B}$	3.7	4.6	6.1	3.2	8.4	3.2	6.7	ns
t_{PHL}			2.9	4.3	5.8	2.5	8.2	2.5	6.4	
t_{PZH}	OEA	A	2.3	3.1	4.5	0.3	7.3	1.6	5	ns
t_{PZL}			1.9	2.7	4.1	0.3	7	1.6	4.4	
t_{PHZ}	OEA	A	2.2	3.1	4.5	1.5	7.1	1.5	5.2	ns
t_{PLZ}			2.5	3.3	4.9	2	7.2	2	5.2	
$t_{sk(p)}$	Skew for any single channel $\lvert t_{PHL} - t_{PLH} \rvert$	A to $\overline{B}$		0.5						ns
		$\overline{B}$ to A		0.3						
$t_{sk(o)}$	Skew between drivers in the same package	A to $\overline{B}$		0.2						ns
		$\overline{B}$ to A		0.3						
t_t	Transition time, $\overline{B}$ outputs (1.3 V to 1.8 V)		0.6	2	2.8	0.3	3.3	0.4	2.9	ns
	Transition time, A outputs (10% to 90%)		0.5	3.5	4.7	0	6.4	0	5.4	
t_{PR}	$\overline{B}$-port input pulse rejection		1			1		1		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

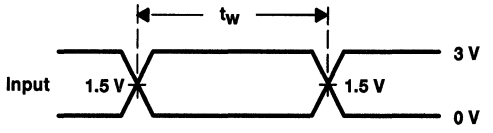


LOAD CIRCUIT FOR A OUTPUTS

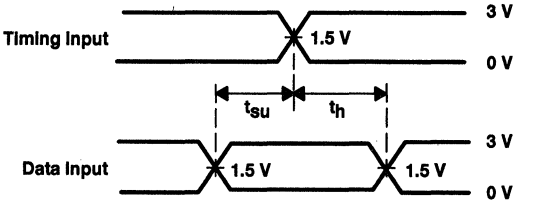


LOAD CIRCUIT FOR B OUTPUTS

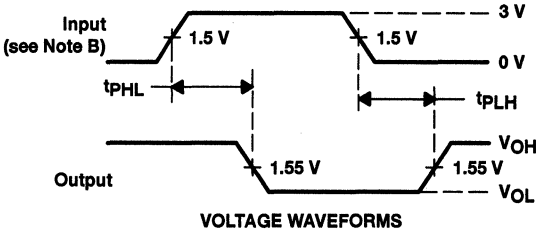
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



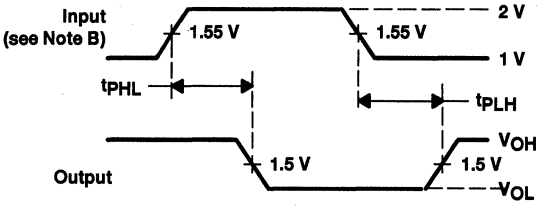
VOLTAGE WAVEFORMS
PULSE DURATION



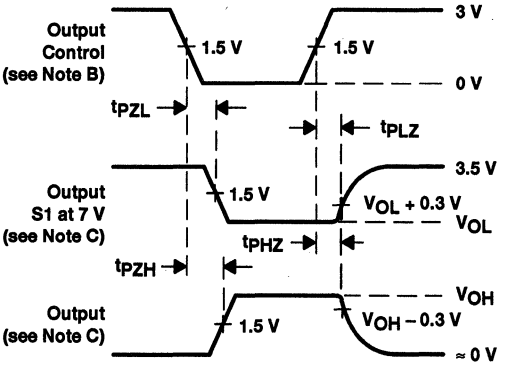
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)



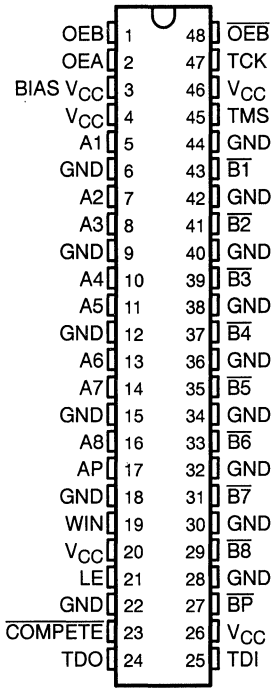
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: TTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns. BTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

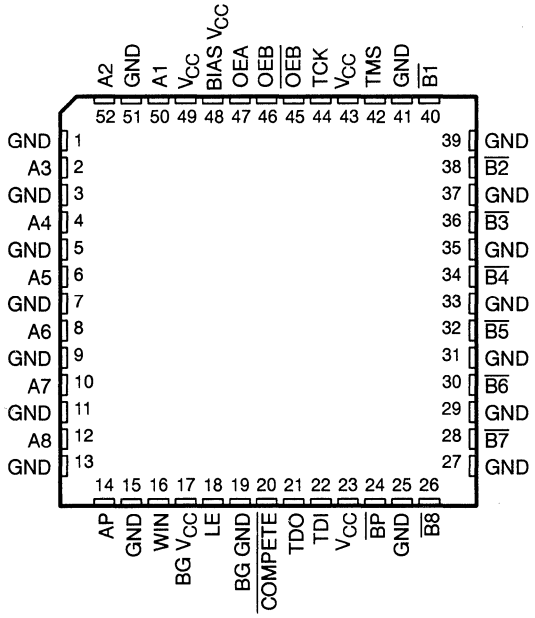
Figure 1. Load Circuits and Voltage Waveforms

- **Compatible With IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) Standards**
- **TTL A Port, Backplane Transceiver Logic $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **Minimum $\overline{B}$-Port Edge Rate = 2 ns**
- **Isolated Logic-Ground and Bus-Ground Pins Reduce Noise**
- **BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion/Withdrawal**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage**
- **TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination**
- **Package Options Include Plastic Quad Flat (RC) Package and Ceramic Flat (WD) Package**

SN54FB2032 . . . WD PACKAGE
(TOP VIEW)



SN74FB2032 . . . RC PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The 'FB2032 are 9-bit transceivers designed to translate signals between TTL and backplane transceiver logic (BTL) environments and to perform bus arbitration. They are specifically designed to be compatible with IEEE 1194.1-1991 (BTL) and IEEE 896.2-1991 (Futurebus+) standards.

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA and have minimum output edge rates of 2 ns. Two output enables, OEB and $\overline{OEB}$, are provided for the $\overline{B}$ outputs. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is typically less than 2.5 V, the $\overline{B}$ port is turned off.

description (continued)

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable, OEA, is high. When OEA is low or when V_{CC} is typically less than 2.5 V, the A outputs are in the high-impedance state.

The A-port data can be latched by taking the latch enable (LE) high. When LE is low, the latches are transparent.

The Futurebus+ protocol logic can be activated by taking $\overline{COMPETE}$ low. The module (device) then compares its A data (arbitration number) against the A data of another identical module also connected to the $\overline{B}$ arbitration bus, and sets WIN high if the A data is greater than the A data of the other module (i.e., has higher priority). A8 and $\overline{B8}$ are the most significant bits, and A1 and $\overline{B1}$ are the least significant bits. If OEB is high and $\overline{OEB}$ is low during this operation and the A bus of the first module wins priority, the A bus asserts its arbitration number on the $\overline{B}$-arbitration bus.

AP and $\overline{BP}$ are the bus-parity bits. The winning module may assert $\overline{BP}$ low if its parity bit (AP) is high.

In a typical operating sequence, a Futurebus+ arbitration controller latches its arbitration number into the A port and waits for the results of a competition. When the competition is complete, and if the controller's arbitration number did not win, the controller reads back the current value of the $\overline{B}$ bus (by taking OEA high) and determines the winning arbitration number. This allows the module to change its arbitration number for the next competition cycle, if desired.

Pins are allocated for the four-wire IEEE 1149.1 (JTAG) test bus, which will be implemented in a future version of the 'FB2032. Currently, TMS and TCK are not connected and TDI is shorted to TDO.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

BG V_{CC} and BG GND are the supply inputs for the bias generator.

The SN54FB2032 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74FB2032 is characterized for operation from 0°C to 70°C.

PRODUCT PREVIEW

Function Tables

TRANSCEIVER

INPUTS			FUNCTION
OEA	OEB	$\overline{OEB}$	
L	H	L	$\overline{A}$ data to B bus
H	L	X	$\overline{B}$ data to A bus
H	X	H	
H	H	L	$\overline{A}$ data to B bus, $\overline{B}$ data to A bus
L	L	X	Isolation
L	X	H	

WIN

INPUTS				WIN
OEB	$\overline{OEB}$	$\overline{COMPETE}$	DATA A1, A2†	
H	H	X	X	L
H	L	H	X	L
H	L	L	A1 < A2	L
H	L	L	A2 ≤ A1	H

† A1 refers to the A data of Module 1 and A2 refers to the A data of Module 2. If LE = L, A = current A data. If LE = H, A = the value of A8-A1 prior to the most recent low-to-high transition of LE.

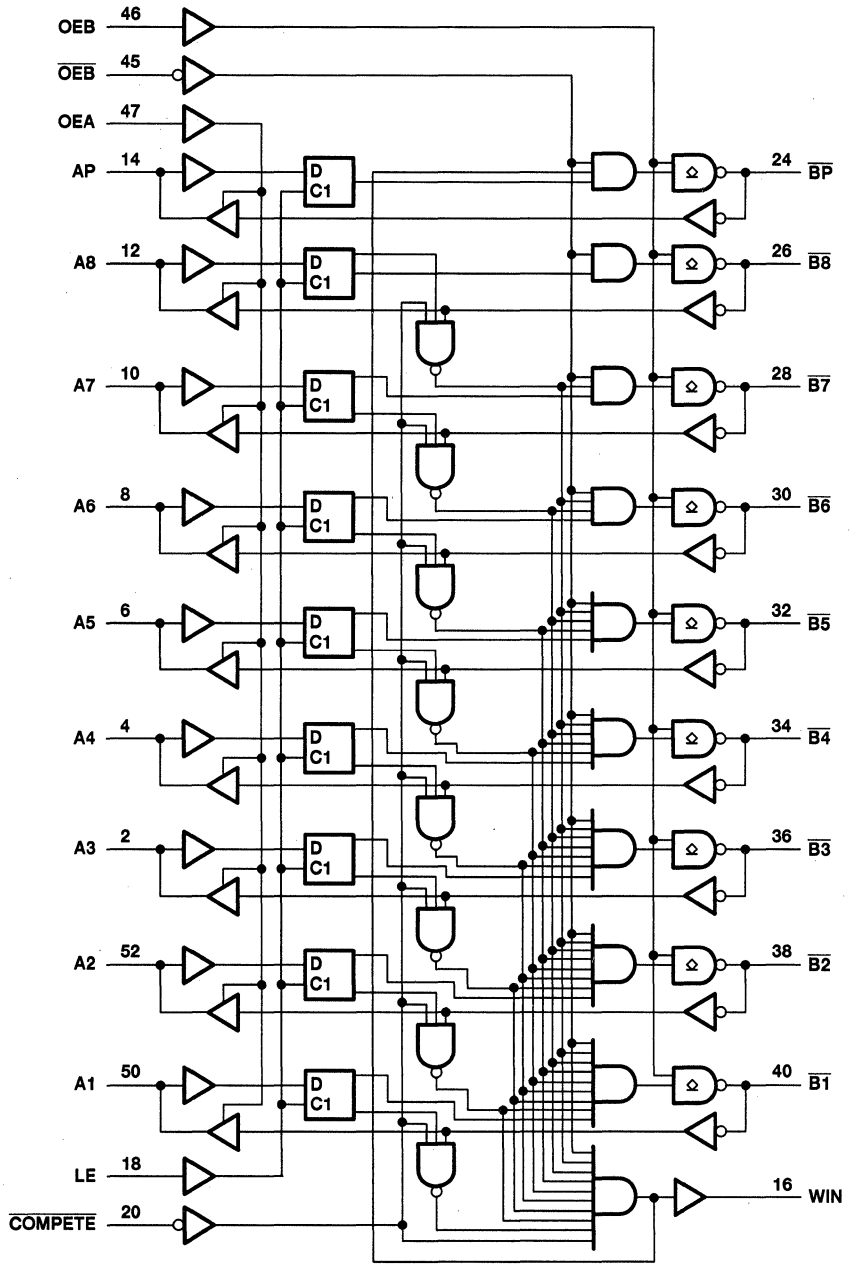
$\overline{BP}$

INPUTS				BP
OEB	$\overline{OEB}$	WIN	AP‡	
L	X	X	X	H
X	H	X	X	H
H	L	L	X	H
H	L	H	L	H
H	L	H	H	L

‡ If LE = L, AP = current AP data, if LE = H, AP = the level of AP prior to the most recent low-to-high transition of LE.

PRODUCT PREVIEW

functional block diagram



Pin numbers shown are for the RC package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I: except $\overline{BP}$, $\overline{B}$ port ..... −1.2 V to 7 V
$\overline{BP}$, $\overline{B}$ port ..... −1.2 V to 3.5 V
Input current range (except $\overline{B}$ port) ..... −40 mA to 5 mA
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to V_{CC}
Current applied to any single output in the low state: A port ..... 48 mA
$\overline{B}$ port ..... 200 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 1): RC package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 2)

			SN54FB2032			SN74FB2032			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}, BIAS V_{CC}, BG V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{BP}$, $\overline{B}$ port	1.62		2.3	1.62		2.3	V
		Except $\overline{B}$ port	2			2			
V_{IL}	Low-level input voltage	$\overline{BP}$, $\overline{B}$ port	0.75		1.47	0.75		1.47	V
		Except $\overline{B}$ port			0.8			0.8	
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	AP, WIN, A port						−3	mA
I_{OL}	Low-level output current	AP, WIN, A port						24	mA
		$\overline{BP}$, $\overline{B}$ port			100			100	
T_A	Operating free-air temperature		−55		125	0		70	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54FB2032			SN74FB2032			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$\overline{BP}$, $\overline{B}$ port	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
	Except $\overline{BP}$, $\overline{B}$ port	V_{CC} = 4.5 V,	I_I = –40 mA			–0.5			–0.5	
V_{OH}	AP, WIN, A port	V_{CC} = 4.5 V,	I_{OH} = –3 mA	2.5	3.3		2.5	3.3		V
V_{OL}	AP, WIN, A port	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5		0.35	0.5	V
	$\overline{BP}$, $\overline{B}$ port	V_{CC} = 4.5 V,	I_{OL} = 80 mA	0.75		1.1	0.75		1.1	
I_I	Except $\overline{BP}$, $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 5.5 V			50			50	µA
I_{IH}‡	Except $\overline{BP}$, $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 2.7 V			50			50	µA
I_{IL}‡	Except $\overline{BP}$, $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.5 V			–50			–50	µA
	$\overline{BP}$, $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.75 V			–100			–100	
I_{OH}	$\overline{BP}$, $\overline{B}$ port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V			100			100	µA
I_{OS}§	AP, WIN, A port	V_{CC} = 5.5 V,	V_O = 0	– 30		–150	– 30		–150	mA
I_{CC}	A port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0		25			25		mA
	$\overline{B}$ port to A port				60			60		
C_i		V_I = V_{CC} or GND				5			5	pF
C_o	A port	V_O = V_{CC} or GND								pF
C_{io}	$\overline{B}$ port per P1194.0	V_{CC} = 0 to 4.5 V				6			6	pF
		V_{CC} = 4.5 V to 5.5 V				5			5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54FB2032		SN74FB2032		UNIT
				MIN	MAX	MIN	MAX	
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		450		450	µA
		V_{CC} = 4.5 V to 5.5 V			10		10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	1.62	2.1	1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0 ,	V_B = 1 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	–1		–1		µA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V		100		100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V		100		100	

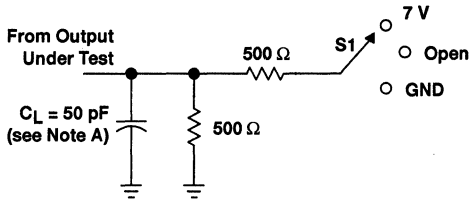
PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

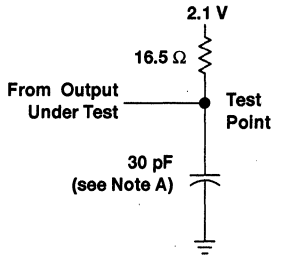
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C		SN54FB2032		SN74FB2032		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or AP	$\overline{B}$ or $\overline{BP}$				8		8	ns
t_{PHL}						8		8	
t_{PLH}	A	$\overline{B}_{n-1}$				9		9	ns
t_{PHL}						9		9	
t_{PLH}	A	$\overline{BP}$				10		10	ns
t_{PHL}						10		10	
t_{PLH}	$\overline{B}$	$\overline{B}_{n-1}$				9		9	ns
t_{PHL}						9		9	
t_{PLH}	LE	$\overline{B}$				7.5		7.5	ns
t_{PHL}						7.5		7.5	
t_{PLH}	LE	$\overline{BP}$				7.5		7.5	ns
t_{PHL}						7.5		7.5	
t_{PLH}	$\overline{B}$ or $\overline{BP}$	A or AP				7.5		7.5	ns
t_{PHL}						7.5		7.5	
t_{PLH}	$\overline{B}$	WIN				8.5		8.5	ns
t_{PHL}						8.5		8.5	
t_{PLH}	A	WIN				7.6		7.6	ns
t_{PHL}						7.6		7.6	
t_{PLH}	LE	WIN				7		7	ns
t_{PHL}						7		7	
t_{PLH}	$\overline{COMPETE}$	WIN				5.5		5.5	ns
t_{PHL}						5.5		5.5	
t_{PLH}	$\overline{OEB}$	WIN				6		6	ns
t_{PHL}						6		6	
t_{PLH}	$\overline{COMPETE}$	$\overline{B}$				7.5		7.5	ns
t_{PHL}						7.5		7.5	
t_{PLH}	$\overline{COMPETE}$	$\overline{BP}$				6.5		6.5	ns
t_{PHL}						6.5		6.5	
t_{PLH}	OEB	$\overline{B}$				6.5		6.5	ns
t_{PHL}						6.5		6.5	
t_{PLH}	$\overline{OEB}$	$\overline{B}$				6.5		6.5	ns
t_{PHL}						6.5		6.5	
t_{PZH}	OEA	A				5.5		5.5	ns
t_{PZL}						5.5		5.5	
t_{PHZ}	OEA	A				7		7	ns
t_{PLZ}						7		7	
t_t	Transition time, $\overline{B}$ outputs (1.3 V to 1.8 V)		2		1	3	1	3	ns
t_{PR}	$\overline{B}$-port input pulse rejection					1		1	ns

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

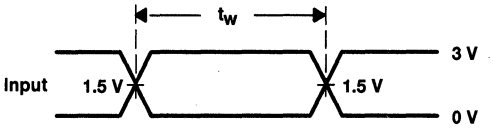


LOAD CIRCUIT FOR A OUTPUTS

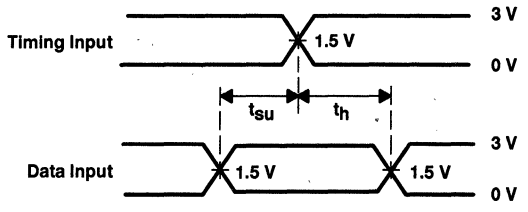


LOAD CIRCUIT FOR B OUTPUTS

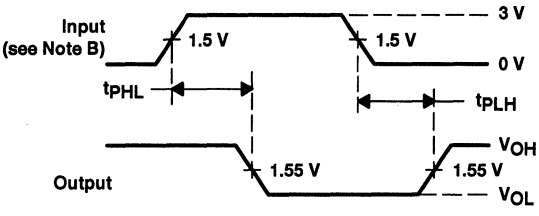
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



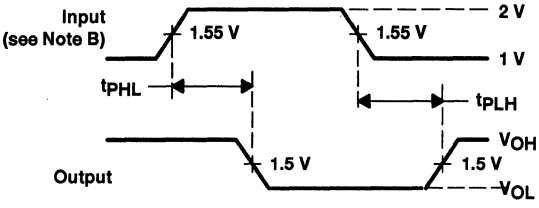
VOLTAGE WAVEFORMS
PULSE DURATION



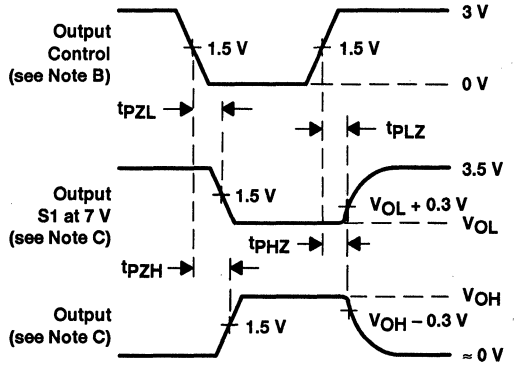
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)

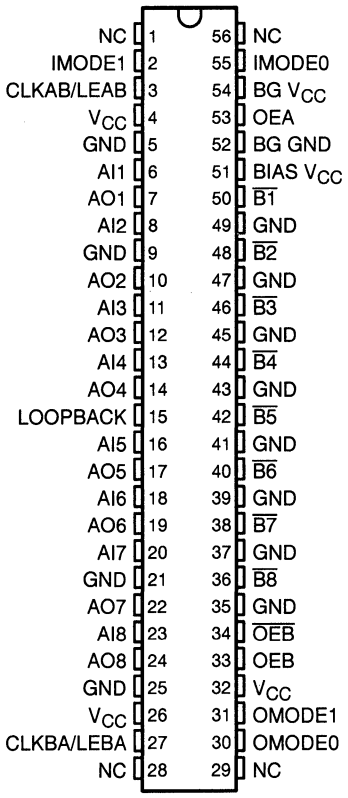
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: TTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns. BTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PRODUCT PREVIEW

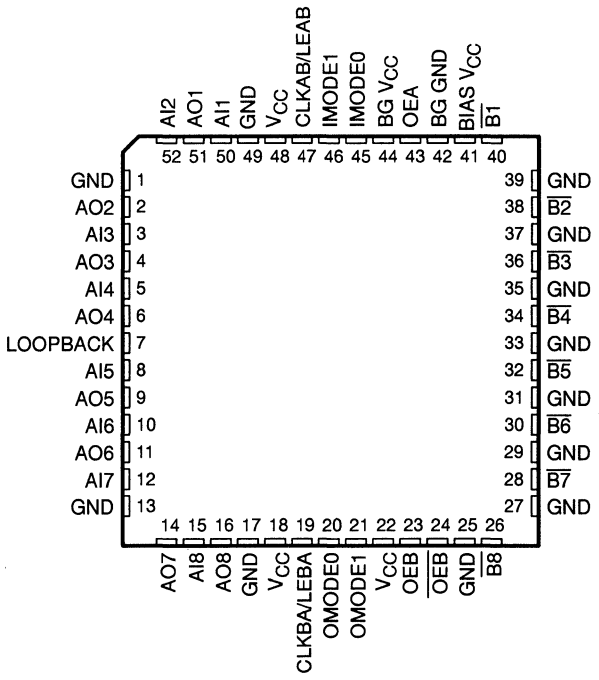
- **TTL A Port, Backplane Transceiver Logic (BTL) $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **Isolated Logic-Ground and Bus-Ground Pins Reduce Noise**
- **BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion/Withdrawal**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage**
- **TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination**
- **Package Options Include Plastic Quad Flat (RC) Package and Ceramic Flat (WD) Package**

SN54FB2033 . . . WD PACKAGE
(TOP VIEW)



NC – No internal connection

SN74FB2033A . . . RC PACKAGE
(TOP VIEW)



description

The SN54FB2033 and SN74FB2033A are 8-bit transceivers featuring a split input (AI) and output (AO) bus on the TTL-level A port. The common-I/O, open-collector $\overline{B}$ port operates at backplane transceiver logic (BTL) signal levels.

The logic element for data flow in each direction is configured by two mode inputs (IMODE1 and IMODE0 for B-to-A, OMODE1 and OMODE0 for A-to-B) as a buffer, a D-type flip-flop, or a D-type latch. When configured in the buffer mode, the inverted input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock input (CLKAB/LEAB or CLKBA/LEBA). In the latch mode, the clock pins serve as active-high transparent latch enables.

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the LOOPBACK input. When LOOPBACK is low, $\overline{B}$-port data is the B-to-A input. When LOOPBACK is high, the output of the selected A-to-B logic element (prior to inversion) is the B-to-A input.

The AO port-enable/-disable control is provided by OEA. When OEA is low or when V_{CC} is less than 2.5 V, the AO port is in the high-impedance state. When OEA is high, the AO port is active (high or low logic levels).

The $\overline{B}$ port is controlled by OEB and $\overline{OEB}$. If OEB is low, $\overline{OEB}$ is high, or V_{CC} is less than 2.5 V, the $\overline{B}$ port is inactive. If OEB is high and $\overline{OEB}$ is low, the B port is active.

BG V_{CC} and BG GND are the bias-generator reference inputs.

The A-to-B and B-to-A logic elements are active regardless of the state of their associated outputs. The logic elements can enter new data (in flip-flop and latch modes) or retain previously stored data while the associated outputs are in the high-impedance (AO port) or inactive ($\overline{B}$ port) states.

Output clamps are provided on the BTL outputs to reduce switching noise. One clamp reduces inductive ringing effects on V_{OH} during a low-to-high transition. The other clamps out ringing below the BTL V_{OL} voltage of 0.75 V. Both these clamps are active only during AC switching and do not affect the BTL outputs during steady-state conditions.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

The SN54FB2033 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74FB2033A is characterized for operation from 0°C to 70°C.

Function Tables

FUNCTION/MODE TABLE

INPUTS								FUNCTION/MODE
OEA	OEB	$\overline{OEB}$	OMODE1	OMODE0	IMODE1	IMODE0	LOOPBACK	
L	L	X	X	X	X	X	X	Isolation
L	X	H	X	X	X	X	X	
X	H	L	L	L	X	X	X	AI to $\overline{B}$, buffer mode
X	H	L	L	H	X	X	X	AI to $\overline{B}$, flip-flop mode
X	H	L	H	X	X	X	X	AI to $\overline{B}$, latch mode
H	L	X	X	X	L	L	L	$\overline{B}$ to AO, buffer mode
H	X	H	X	X	L	L	L	
H	L	X	X	X	L	H	L	$\overline{B}$ to AO, flip-flop mode
H	X	H	X	X	L	H	L	
H	L	X	X	X	H	X	L	$\overline{B}$ to AO, latch mode
H	X	H	X	X	H	X	L	
H	L	X	X	X	L	L	H	AI to AO, buffer mode
H	X	H	X	X	L	L	H	
H	L	X	X	X	L	H	H	AI to AO, flip-flop mode
H	X	H	X	X	L	H	H	
H	L	X	X	X	H	X	H	AI to AO, latch mode
H	X	H	X	X	H	X	H	
H	H	L	X	X	X	X	L	AI to $\overline{B}$, $\overline{B}$ to AO

Function Tables (Continued)

ENABLE/DISABLE

INPUTS			OUTPUTS	
OEA	OEB	$\overline{OEB}$	AO	$\overline{B}$
L	X	X	Hi Z	
H	X	X	Active	
X	L	L		Inactive (H)
X	L	H		Inactive (H)
X	H	L		Active
X	H	H		Inactive (H)

BUFFER

INPUT	OUTPUT
L	H
H	L

LATCH

INPUTS		OUTPUT
CLK/LE	DATA	
H	L	H
H	H	L
L	X	Q_0

LOOPBACK

LOOPBACK	Q†
L	$\overline{B}$ port
H	Point P‡

† Q is the input to the B-to-A logic element.
‡ P is the output of the A-to-B logic element (see functional block diagram).

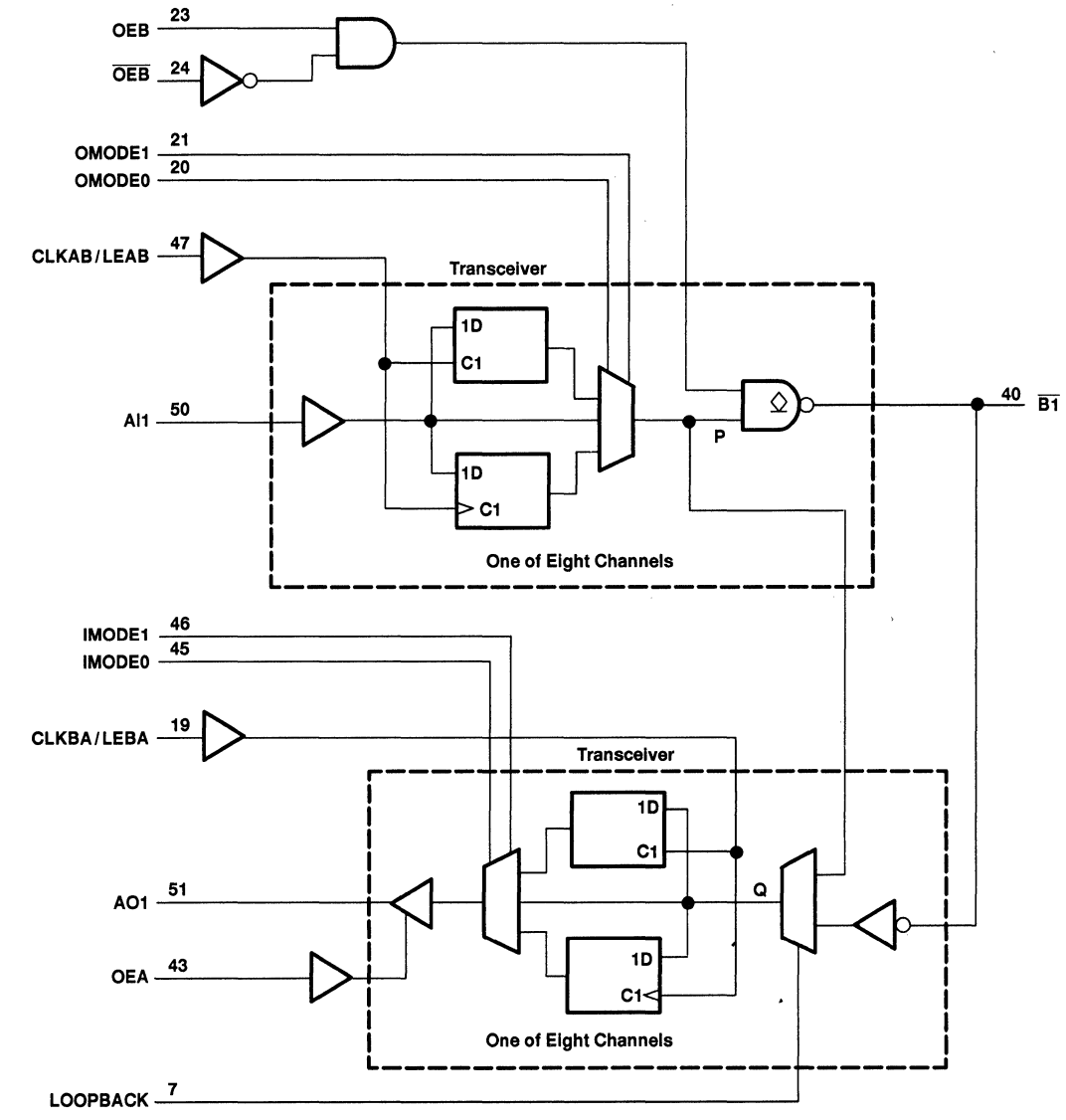
SELECT

INPUTS		SELECTED LOGIC ELEMENT
MODE1	MODE0	
L	L	Buffer
L	H	Flip-flop
H	X	Latch

FLIP-FLOP

INPUTS		OUTPUT
CLK/LE	DATA	
L	X	Q_0
↑	L	H
↑	H	L

functional block diagram



Pin numbers shown are for the RC package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I: except $\overline{B}$ port ..... −1.2 V to 7 V
$\overline{B}$ port ..... −1.2 V to 3.5 V
Input current range, (except $\overline{B}$ port) ..... −40 mA to 5 mA
Voltage range applied to any B output in the disabled or power-off state ..... −0.5 V to 3.5 V
Voltage range applied to any output in the high state: A port ..... −0.5 V to V_{CC}
Current applied to any single output in the low state: A port ..... 48 mA
$\overline{B}$ port ..... 200 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 1): RC package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 2)

			SN54FB2033			SN74FB2033A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}, BG V_{CC}	Supply voltage		4.75	5	5.25	4.75	5	5.25	V
BIAS V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62*		2.3	1.62		2.3	V
		Except $\overline{B}$ port	2			2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47*	0.75		1.47	V
		Except $\overline{B}$ port			0.8			0.8	
I_{OH}	High-level output current	AO port			−3			−3	mA
I_{OL}	Low-level output current	AO port			24			24	mA
		$\overline{B}$ port			100			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Except $\overline{B}$ port			10			10	ns/V
T_A	Operating free-air temperature		−55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not tested.

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54FB2033			SN74FB2033A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	AO port	V_{CC} = 4.75 V to 5.25 V,	I_{OH} = −10 μA			V_{CC}−1			V_{CC}−1.1	V
		V_{CC} = 4.75 V	I_{OH} = −3 mA	2.5	2.85	3.4	2.5	2.85	3.4	
			I_{OH} = −32 mA	2			2			
V_{OL}	AO port	V_{CC} = 4.75 V	I_{OL} = 20 mA		0.33	0.5		0.33	0.5	V
			I_{OL} = 55 mA			0.8			0.8	
	$\overline{B}$ port	V_{CC} = 4.75 V	I_{OL} = 100 mA	0.75		1.1	0.75		1.1	
			I_{OL} = 4 mA	0.5			0.5			
I_I	Except $\overline{B}$ port	V_{CC} = 0,	V_I = 5.25 V			100			100	μA
I_{IH}	Except $\overline{B}$ port	V_{CC} = 5.25 V,	V_I = 2.7 V			50			50	μA
	$\overline{B}$ port‡	V_{CC} = 0 to 5.25 V,	V_I = 2.1 V			100			100	
I_{IL}	Except $\overline{B}$ port	V_{CC} = 5.25 V,	V_I = 0.5 V			−50			−50	μA
	$\overline{B}$ port‡	V_{CC} = 5.25 V,	V_I = 0.75 V			−100			−100	
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.25 V,	V_O = 2.1 V			100			100	μA
I_{OZH}	AO port	V_{CC} = 5.25 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	AO port	V_{CC} = 5.25 V,	V_O = 0.5 V			−50			−50	μA
I_{OS}§	AO port	V_{CC} = 5.25 V,	V_O = 0	−40	−80	−150	−40	−80	−150	mA
I_{CC}	All outputs on	V_{CC} = 5.25 V,	I_O = 0		45	90		45	70	mA
C_i	AI port and control inputs	V_I = V_{CC} or GND			5			5		pF
C_o	AO port	V_O = V_{CC} or GND			5			5		pF
C_{io}¶	$\overline{B}$ port per P1194.0	V_{CC} = 0 to 4.75 V				8			6	pF
		V_{CC} = 4.75 V to 5.25 V				8			6	

† All typical values are at V_{CC} = 5 V.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
¶ Parameter is based on characterization data but is not tested.

live-insertion characteristics over recommended operating free-air temperature range (see Note 3)

PARAMETER		TEST CONDITIONS		SN54FB2033		SN74FB2033A		UNIT
				MIN	MAX	MIN	MAX	
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		400		400	μA
		V_{CC} = 4.5 V to 5.5 V			10		10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	1.62	2.1	1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0,	V_B = 1 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	−30		−1		μA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V		170		100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V		100		100	

NOTE 3: Power-up sequence is as follows: GND, BIASV_{CC}, V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

		SN54FB2033				SN74FB2033A				UNIT
		V_{CC} = 5 V, T_A = 25°C		MIN	MAX	V_{CC} = 5 V, T_A = 25°C		MIN	MAX	
		MIN	MAX			MIN	MAX			
f_{clock}	Clock frequency	0	150	0	150	0	150	0	150	MHz
t_w	Pulse duration, CLKAB/LEAB or CLKBA/LEBA	3.9		4.3		3.3		3.3		ns
t_{su}	Setup time, data before CLKAB/LEAB or CLKBA/LEBA↑	2.9		3.3		2.7		2.7		ns
t_h	Hold time, data after CLKAB/LEAB or CLKBA/LEBA↑	1		1.3		0.7		0.7		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54FB2033					SN74FB2033A					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			MIN	TYP	MAX			
f_{max}			150			150		150			150		MHz
t_{PLH}	AI (thru mode)	$\overline{B}$	1.7	3.8	4.6	1.2	7.5	2.3	3.6	4.6	2.3	5.6	ns
t_{PHL}			1.3	2.6	4.3	1	5.5	1.9	3	4.2	1.9	4.5	
t_{PLH}	$\overline{B}$ (thru mode)	AO	2.5	3.9	5.9	1.4	7.6	2.5	4.2	5.5	2.5	6.1	ns
t_{PHL}			2.7	5.2	5.7	1.6	7.8	3	4.2	5.6	3	5.7	
t_{PLH}	AI (transparent)	$\overline{B}$	1.7	5	4.6	1.2	8.7	2.3	3.6	4.6	2.3	5.6	ns
t_{PHL}			1.3	3.6	4.3	1	5.9	1.9	3	4.1	1.9	4.5	
t_{PLH}	$\overline{B}$ (transparent)	AO	2.5	4.3	5.8	1.5	7.8	2.5	4.2	5.5	2.5	6.1	ns
t_{PHL}			2.7	5.6	5.7	1.6	8	3	4.2	5.6	3	5.7	
t_{PLH}	OEB	$\overline{B}$	1.6	3.7	4.7	1.1	6.6	2.4	3.7	4.7	2.4	5.8	ns
t_{PHL}			1.2	2.6	4.1	0.4	5.4	1.8	3	4.1	1.8	4.4	
t_{PLH}	$\overline{OEB}$	$\overline{B}$	1.3	3.8	4.3	1.2	6.6	2	3.4	4.3	2	5.2	ns
t_{PHL}			1.2	2.9	4.4	0.8	5.5	2	3.3	4.4	2	4.8	
t_{PZH}	OEA	AO	2	3.5	5.1	1.2	6.6	2	3.5	4.6	2	5.1	ns
t_{PZL}			2.7	4.3	6.1	1.3	7.7	2.7	4.2	5.1	2.7	5.4	
t_{PHZ}	OEA	AO	2.1	3.5	5.8	1.1	6.9	2.1	4	5	2.1	5.5	ns
t_{PLZ}			1.6	2.7	4.7	1	6	1.6	2.8	3.9	1.6	4.3	
t_{PLH}	CLKAB/LEAB	$\overline{B}$	2.1	5	5.8	1.6	8.7	3	4.7	5.8	3	6.9	ns
t_{PHL}			2	3.6	5.6	1.1	6.6	2.8	4.3	5.6	2.8	6.1	
t_{PLH}	CLKBA/LEBA	AO	2	3.8	5.4	1.4	6.7	2	3.6	4.9	2	5.4	ns
t_{PHL}			2.2	4.1	5.6	1.5	6.5	2.2	3.5	4.7	2.2	5.1	
t_{PLH}	OMODE	$\overline{B}$	2.3	4.8	6.1	1.6	8.1	2.4	5	6.1	2.4	7.2	ns
t_{PHL}			1.4	3.5	6	1	6.5	2.4	4.5	6	2.4	6.7	
t_{PLH}	IMODE	AO	1.8	3.6	5.9	1.3	7.3	1.8	4	5.3	1.8	5.9	ns
t_{PHL}			2.3	4.1	5.4	1.4	6.4	2.3	4.1	5.2	2.3	5.4	
t_{PLH}	LOOPBACK	AO	2.4	4.6	7.1	1.6	8.3	2.4	5	7	2.4	8	ns
t_{PHL}			3.1	4.8	6.9	1.8	7.5	3.1	4.6	5.7	3.1	5.9	
t_{PLH}	AI	AO	1.9	3.7	5.7	1.4	7.1	1.9	3.7	5.5	1.9	6.1	ns
t_{PHL}			2.6	4.3	5.8	1.6	7.3	2.6	4.2	5.6	2.6	5.8	
t_t	Rise time, 1.3 V to 1.8 V	$\overline{B}$	0.5	1.5	2.1	0.4	3.2	0.5	1.2	2.1	0.5	3	ns
	Fall time, 1.8 V to 1.3 V		0.4	1.5	2.3	0.4	3.4	0.5	1.4	2.3	0.5	3	
	Rise time, 10% to 90%	AO	2	3.5	4.2	1.8	5.4	2	3.3	4.2	2	5	
	Fall time, 90% to 10%		1	2.5	3.4	0.8	5.1	1	2.5	3.4	1	5	
t_{PR}	$\overline{B}$-port input pulse rejection					1*					1		ns

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not tested.

output-voltage characteristics

PARAMETER			TEST CONDITIONS	SN54FB2033		SN74FB2033A		UNIT
				MIN	MAX	MIN	MAX	
V_{OHP}†	Peak output voltage during turnoff of 100 mA into 40 nH	$\overline{B}$ port	See Figure 1		4		4.5	V
V_{OHV}†	Minimum output voltage during turnoff of 100 mA into 40 nH			1.62		1.62		V
V_{OLV}	Minimum output voltage during high-to-low switch		I_{OL} = −50 mA	0.3		0.3		V

† Parameter is based on characterization data but not tested.

PARAMETER MEASUREMENT INFORMATION

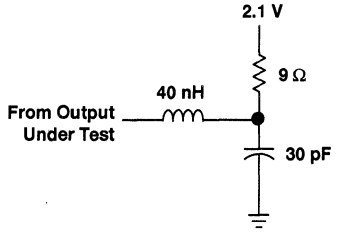
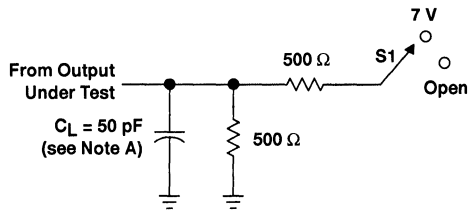
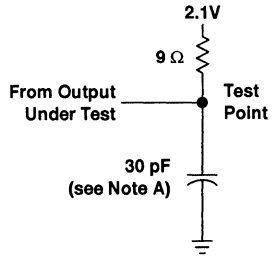


Figure 1. Load Circuit for V_{OHP}, V_{OHV}

PARAMETER MEASUREMENT INFORMATION

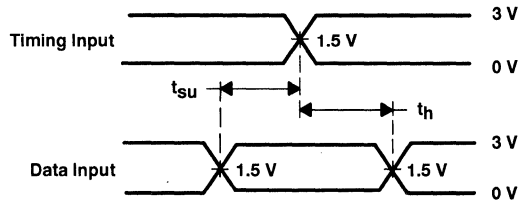


LOAD CIRCUIT FOR A OUTPUTS

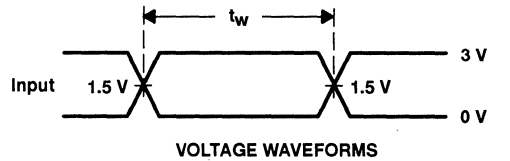


LOAD CIRCUIT FOR B OUTPUTS

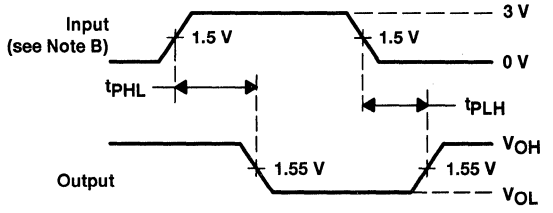
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



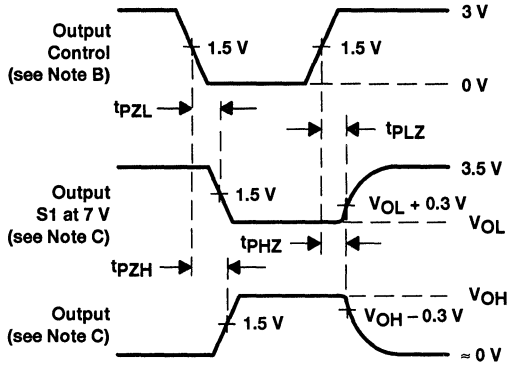
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



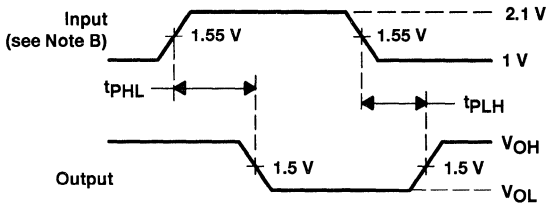
VOLTAGE WAVEFORMS
PULSE DURATION



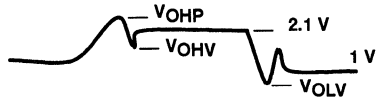
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)



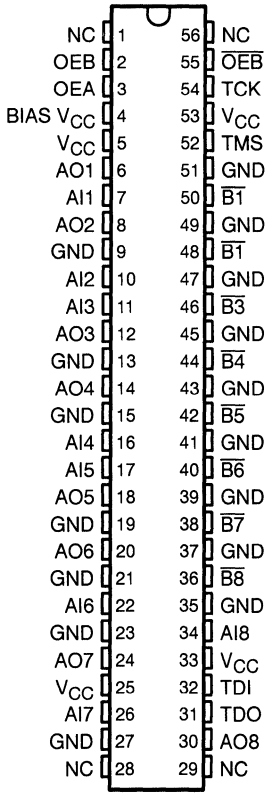
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: TTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns, BTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

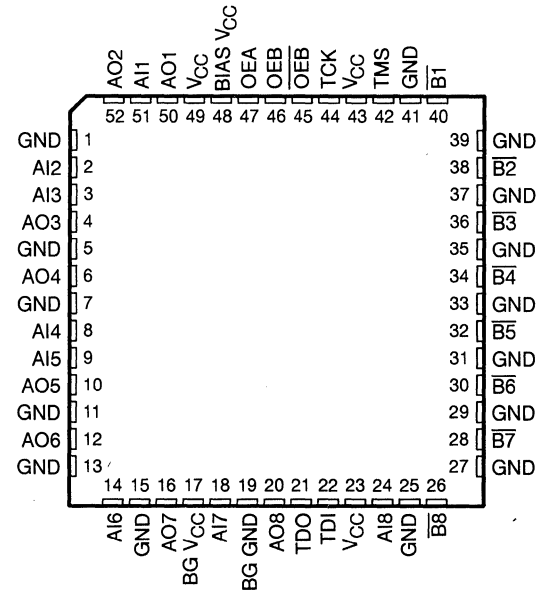
- **Compatible With IEEE 1194.1-1991 (BTL) Standard**
- **TTL A Port, Backplane Transceiver Logic $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **Isolated Logic-Ground and Bus-Ground Reduces Noise**
- **BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion/Withdrawal**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage**
- **Package Options Include Plastic Quad Flat (RC) Package and Ceramic Flat (WD) Package**

SN54FB2040 . . . WD PACKAGE
(TOP VIEW)



NC – No internal connection

SN74FB2040 . . . RC PACKAGE
(TOP VIEW)



description

The 'FB2040 are 8-bit transceivers designed to translate signals between TTL and backplane transceiver logic (BTL) environments.

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA. Two output enables, OEB and $\overline{OEB}$, are provided for the $\overline{B}$ outputs. When OEB is high and $\overline{OEB}$ is low, the $\overline{B}$ port is active and reflects the inverse of the data present at the A-input pins. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is typically less than 2.5 V, the $\overline{B}$ port is turned off.

description (continued)

The A port operates at TTL-signal levels and has split input and output pins. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable, OEA, is high. When OEA is low or when V_{CC} is typically less than 2.5 V, the A outputs are in the high-impedance state.

Pins are allocated for the four-wire IEEE 1149.1 (JTAG) test bus. Currently, TMS and TCK are not connected and TDI is shorted to TDO.

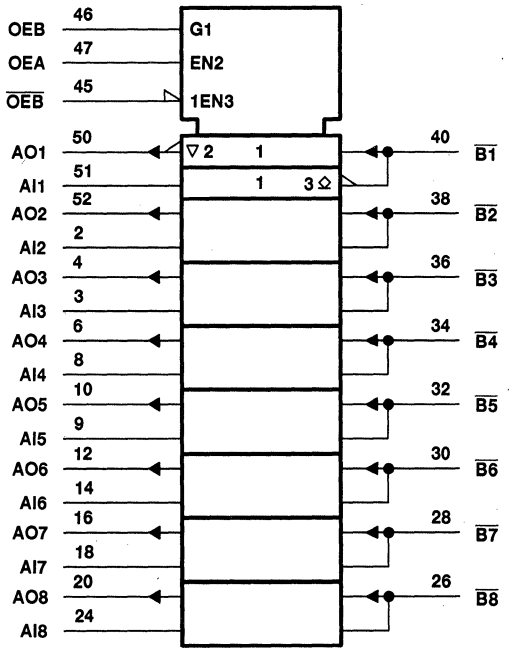
BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

The SN54FB2040 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74FB2040 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

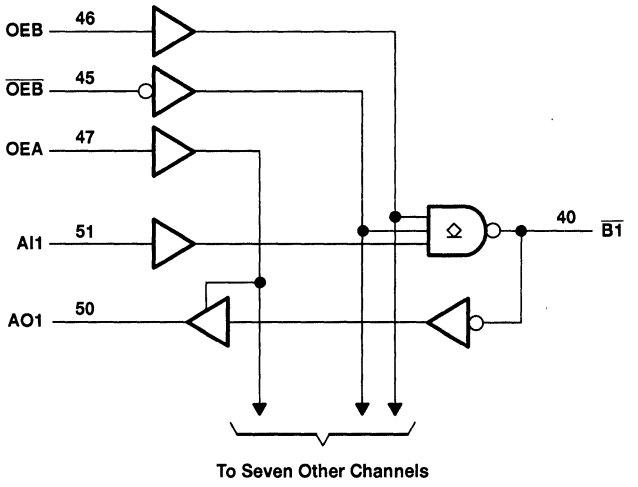
INPUTS			FUNCTION
OEB	$\overline{OEB}$	OEA	
L	X	L	Isolation
X	H	L	
L	X	H	$\overline{B}$ data to AO bus
X	H	H	
H	L	L	$\overline{AI}$ data to B bus
H	L	H	$\overline{AI}$ data to B bus, $\overline{B}$ data to AO bus

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the RC package.

functional block diagram



Pin numbers shown are for the RC package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I: except $\overline{B}$ port ..... −1.2 V to 7 V
$\overline{B}$ port ..... −1.2 V to 3.5 V
Input current range (except $\overline{B}$ port) ..... −40 mA to 5 mA
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to V_{CC}
Current applied to any single output in the low state: A port ..... 48 mA
$\overline{B}$ port ..... 200 mA
Operating free-air temperature range, T_A: SN54FB2040 ..... −55°C to 125°C
SN74FB2040 ..... 0°C to 70°C
Maximum power dissipation at T_A = 55°C (in still air) (see Note 1): RC package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 2)

			SN54FB2040			SN74FB2040			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}, BIAS V_{CC}, BG V_{CC}	Supply voltage		4.75	5	5.25	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port*	1.62		2.3	1.62		2.3	V
		Except $\overline{B}$ port	2			2			
V_{IL}	Low-level input voltage	$\overline{B}$ port*	0.75		1.47	0.75		1.47	V
		Except $\overline{B}$ port			0.8			0.8	
I_{IK}	Input clamp current				–18			–18	mA
I_{OH}	High-level output current	AO port						–3	mA
I_{OL}	Low-level output current	AO port						24	mA
		$\overline{B}$ port			100			100	
T_A	Operating free-air temperature		–55		125	0		70	°C

* On products compliant to MIL-STD-833, Class B, this parameter is based on characterization data but is not tested.
NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54FB2040			SN74FB2040			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$\overline{B}$ port	V_{CC} = 4.5 V	I_I = –18 mA			–1.2			–1.2	V
	Except $\overline{B}$ port		I_I = –40 mA			–1.2			–0.5	
V_{OH}	AO port	V_{CC} = 4.5 V	I_{OH} = –1 mA		3.2					V
			I_{OH} = –3 mA	2.5	3.3		2.5	3.3		
V_{OL}	AO port	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.09					V
			I_{OL} = 24 mA		0.35	0.5		0.35	0.5	
	$\overline{B}$ port	V_{CC} = 4.5 V	I_{OL} = 80 mA	0.75		1.1	0.75		1.1	
			I_{OL} = 100 mA			1.2			1.15	
I_I	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 5.5 V			50			50	µA
I_{IH}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 2.7 V			50			50	µA
I_{IL}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V	V_I = 0.5 V			–50			–50	µA
	$\overline{B}$ port		V_I = 0.75 V			–100			–100	
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V			100			100	µA
I_{OZH}	AO port	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}	AO port	V_{CC} = 5.5 V,	V_O = 0.5 V			–50			–50	µA
I_{OS}§	AO port	V_{CC} = 5.5 V,	V_O = 0	–30		–170	–30		–180	mA
I_{CC}	AI port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0		25	40		40		mA
	$\overline{B}$ port to AO port				60	70		70		
C_i	AI port*	V_I = V_{CC} or GND			25	70		3.5		pF
	Control inputs*					9.9		3		
C_o	AO port*	V_O = V_{CC} or GND				14.7		6		pF
C_{io}	$\overline{B}$ port per P1194.0*	V_{CC} = 0 to 4.5 V				8			5	pF
		V_{CC} = 4.5 V to 5.5 V				9			5	

* On products compliant to MIL-STD-833, Class B, this parameter is based on characterization data but is not tested.
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

live-insertion specifications over recommended operating free-air temperature range

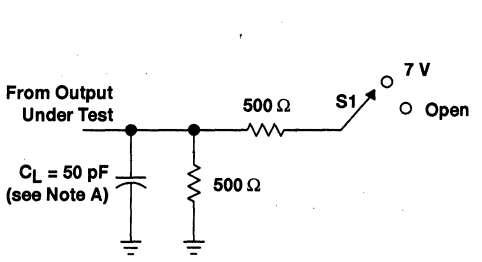
PARAMETER		TEST CONDITIONS		SN54FB2040		SN74FB2040		UNIT
				MIN	MAX	MIN	MAX	
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		450		450	μA
		V_{CC} = 4.5 to 5.5 V			10		10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	1.62	2.1	1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0,	V_B = 1 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	–30		–1		μA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V		100		100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V		100		100	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

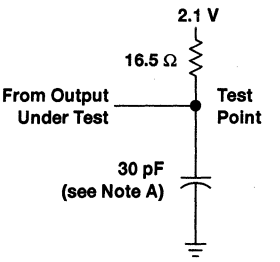
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54FB2040		SN74FB2040		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	AI	$\overline{B}$	3.2	4.5	6	0.5	8.5	2.4	6.5	ns
t_{PHL}			2.8	4.2	5.6	0.4	8.5	2.7	5.8	
t_{PLH}	$\overline{B}$	AO	2.3	3.8	5.7	0.4	8	1.9	6.2	ns
t_{PHL}			2.3	4.2	5.9	0.8	14.9	2	8.2	
t_{PLH}	OEB	$\overline{B}$	3.7	5.1	6.7	0.5	9.9	3	7	ns
t_{PHL}			3.1	4.6	5.9	0.4	9.5	3	6.1	
t_{PLH}	$\overline{OEB}$	$\overline{B}$	3.6	5.2	6.8	1.3	9.5	3.3	7	ns
t_{PHL}			2.9	4.4	5.9	0.2	9.8	2.6	6.1	
t_{PZH}	OEA	AO	2.5	4	5.5	1.2	8	2.1	5.8	ns
t_{PZL}			2.1	3.6	4.8	0.8	7.5	2	5	
t_{PHZ}	OEA	AO	2.3	4.1	5.9	1	8.2	1.9	6.5	ns
t_{PLZ}			1.6	3.1	4.5	0.4	7.2	1.4	4.7	
$t_{sk(p)}$*	Skew for any single channel $\lvert t_{PHL} - t_{PLH} \rvert$	AI to $\overline{B}$ or $\overline{B}$ to AO		0.5						ns
$t_{sk(o)}$*	Skew between drivers in the same package	AI to $\overline{B}$ or $\overline{B}$ to AO		0.4			2			ns
t_t	Rise time, 1.3 V to 1.8 V	$\overline{B}$	2	2.8	3.8	0.2	4.5	1.7		
	Fall time, 1.8 V to 1.3 V		1	1.9	3	0.9	4.0	1	4.2	
t_{PR}*	$\overline{B}$-port input pulse rejection							1	3.4	ns

* On products compliant to MIL-STD-833, Class B, this parameter is based on characterization data but is not tested.

PARAMETER MEASUREMENT INFORMATION

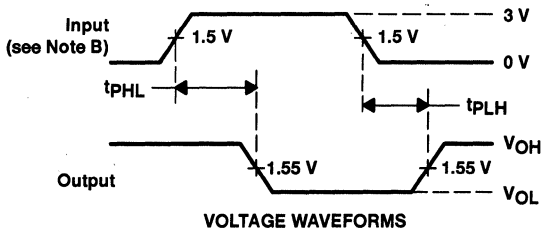


LOAD CIRCUIT FOR A OUTPUTS

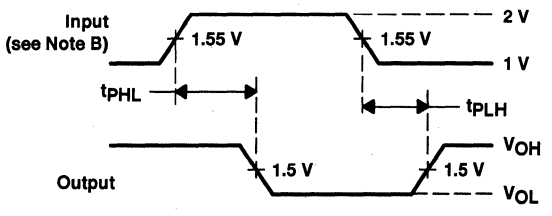


LOAD CIRCUIT FOR B OUTPUTS

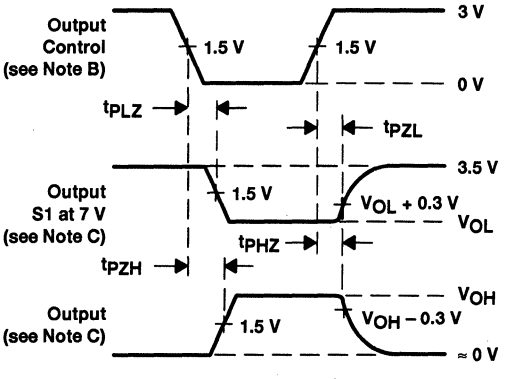
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)



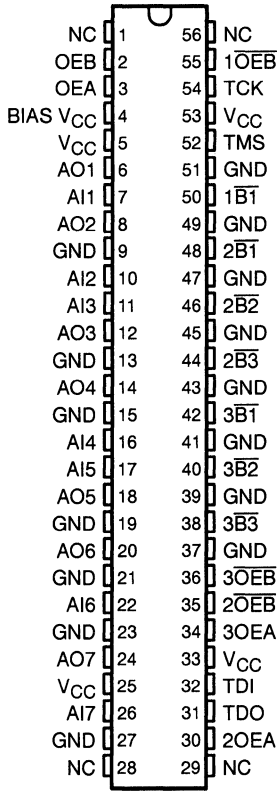
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: TTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns. BTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

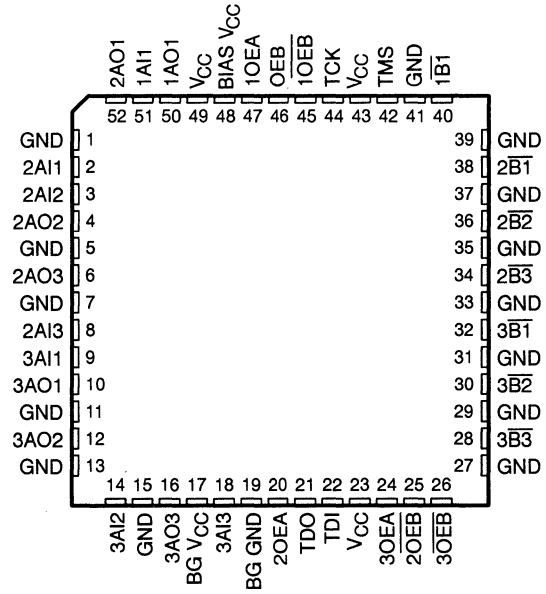
- **Compatible With IEEE 1194.1-1991 (BTL) Standard**
- **TTL A Port, Backplane Transceiver Logic $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **Isolated Logic-Ground and Bus-Ground Reduces Noise**
- **BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion/Withdrawal**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the Backplane Transceiver Logic High-Level Voltage**
- **Package Options Include Plastic Quad Flat (RC) Package and Ceramic Flat (WD) Package**

SN54FB2041 . . . WD PACKAGE
(TOP VIEW)



NC – No internal connection

SN74FB2041 . . . RC PACKAGE
(TOP VIEW)



description

The 'FB2041 are 7-bit transceivers designed to translate signals between TTL and backplane transceiver logic (BTL) environments.

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA. Two output enables, OEB and $\overline{OEB}$, are provided for the $\overline{B}$ outputs. When OEB is high and $\overline{OEB}$ is low, the $\overline{B}$ port is active and reflects the inverse of the data present at the A-input pins. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is typically less than 2.5 V, the $\overline{B}$ port is turned off. The enable/disable logic partitions the device as two 3-bit sections and one 1-bit section.

description (continued)

The A port operates at TTL-signal levels and has split input and output pins. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable, OEA, is high. When OEA is low or when V_{CC} is typically less than 2.5 V, the A outputs are in the high-impedance state.

Pins are allocated for the four-wire IEEE 1149.1 (JTAG) test bus. Currently, TMS and TCK are not connected and TDI is shorted to TDO.

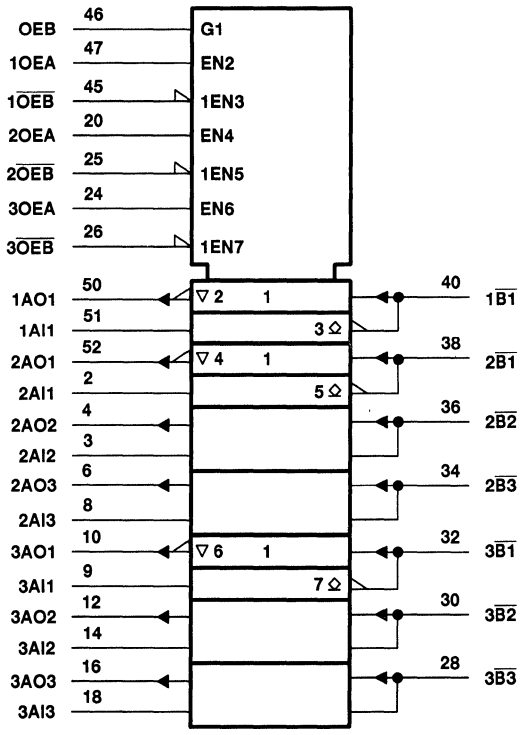
BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

The SN54FB2041 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74FB2041 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

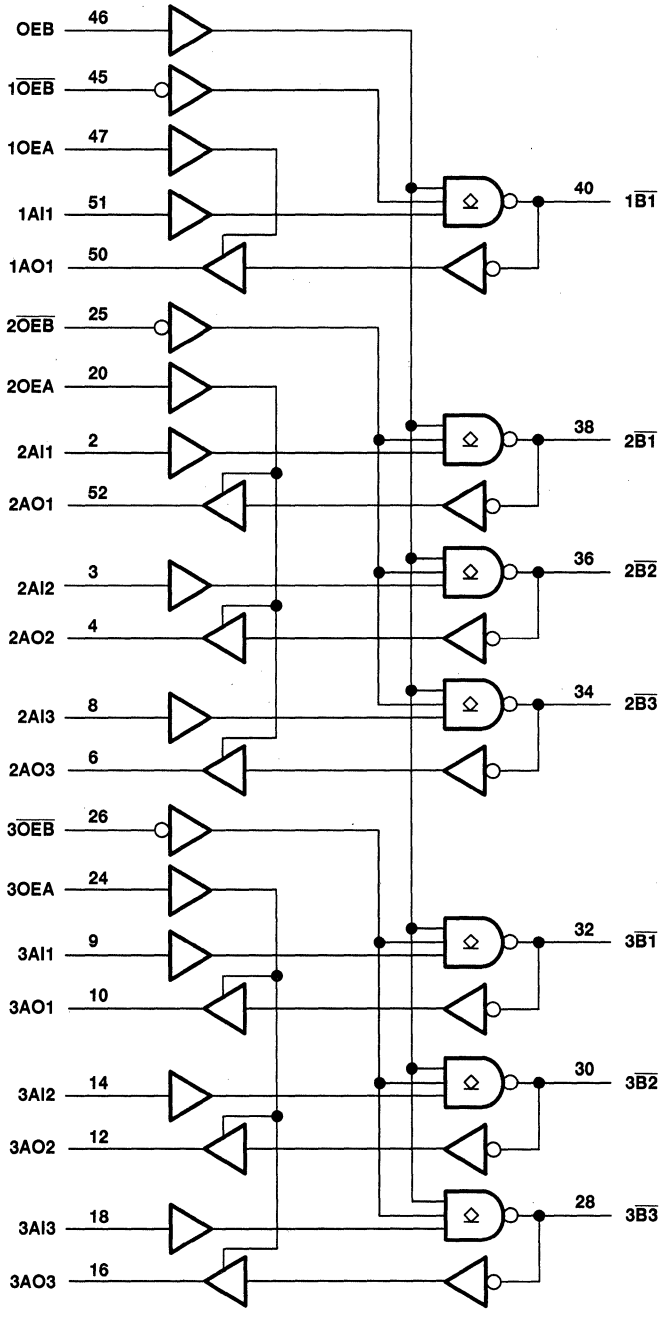
INPUTS			FUNCTION
OEB	$\overline{OEB}$	OEA	
L	X	L	Isolation
X	H	L	
L	X	H	$\overline{B}$ data to AO bus
X	H	H	
H	L	L	$\overline{AI}$ data to B bus
H	L	H	$\overline{AI}$ data to B bus, $\overline{B}$ data to AO bus

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the RC package.

functional block diagram



Pin numbers shown are for the RC package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I: except $\overline{B}$ port ..... −1.2 V to 7 V
$\overline{B}$ port ..... −1.2 V to 3.5 V
Input current range (except $\overline{B}$ port) ..... −40 mA to 5 mA
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ..... −0.5 V to V_{CC}
Current applied to any single output in the low state: A port ..... 48 mA
$\overline{B}$ port ..... 200 mA
Operating free-air temperature range, T_A: SN54FB2041 ..... −55°C to 125°C
SN74FB2041 ..... 0°C to 70°C
Maximum power dissipation at T_A = 55°C (in still air) (see Note 1): RC package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 2)

			SN54FB2041			SN74FB2041			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}, BIAS V_{CC}, BG V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62		2.3	1.62		2.3	V
		Except $\overline{B}$ port	2			2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47	0.75		1.47	V
		Except $\overline{B}$ port			0.8			0.8	
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	AO port			−3			−3	mA
I_{OL}	Low-level output current	AO port			24			24	mA
		$\overline{B}$ port			100			100	
T_A	Operating free-air temperature		−55		125	0		70	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54FB2041			SN74FB2041			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$\overline{B}$ port	V_{CC} = 4.5 V	I_I = −18 mA			−1.2			−1.2	V
	Except $\overline{B}$ port		I_I = −40 mA			−0.5			−0.5	
V_{OH}	AO port	V_{CC} = 4.5 V	I_{OH} = −1 mA							V
			I_{OH} = −3 mA	2.5	3.3		2.5	3.3		
V_{OL}	AO port	V_{CC} = 4.5 V	I_{OL} = 20 mA							V
			I_{OL} = 24 mA		0.35	0.5		0.35	0.5	
	$\overline{B}$ port	V_{CC} = 4.5 V	I_{OL} = 80 mA	0.75		1.1	0.75		1.1	
			I_{OL} = 100 mA			1.15			1.15	
I_I	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 5.5 V			50			50	µA
I_{IH}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 2.7 V			50			50	µA
I_{IL}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V	V_I = 0.5 V			−50			−50	µA
	$\overline{B}$ port		V_I = 0.75 V			−100			−100	
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V			100			100	µA
I_{OZH}	AO port	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}	AO port	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	µA
I_{OS}§	AO port	V_{CC} = 5.5 V,	V_O = 0	−30		−150	−30		−180	mA
I_{CC}	AI port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0		25			40		mA
	$\overline{B}$ port to AO port				65			65		
C_i	AI port	V_I = V_{CC} or GND						3.5		pF
	Control inputs							3		
C_o	AO port	V_O = V_{CC} or GND						6		pF
C_{io}	$\overline{B}$ port per P1194.0	V_{CC} = 0 to 4.5 V				6			5	pF
		V_{CC} = 4.5 V to 5.5 V				5			5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

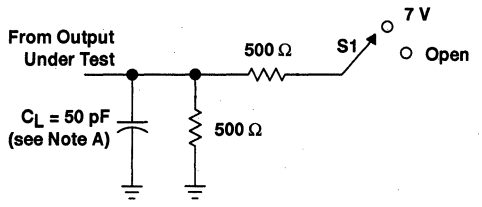
live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		SN54FB2041		SN74FB2041		UNIT
				MIN	MAX	MIN	MAX	
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		450		450	µA
		V_{CC} = 4.5 V to 5.5 V			10		10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	1.62	2.1	1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	V_B = 1 V,	−1		−1		µA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V		100		100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V		100		100	

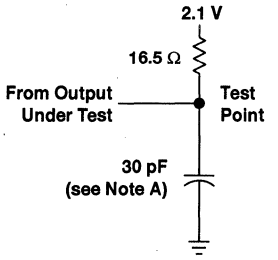
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54FB2041		SN74FB2041		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	AI	$\overline{B}$	3	4.6	6			2.7	6.5	ns
t_{PHL}			2.7	4.2	5.6			2.5	5.8	
t_{PLH}	$\overline{B}$	AO	2.2	3.7	5.5			1.8	6	ns
t_{PHL}			2.6	4.1	5.9			2.2	7.9	
t_{PLH}	OEB	$\overline{B}$	3.8	5.3	7.1			3.3	7.4	ns
t_{PHL}			3.4	4.9	6.5			3.2	6.7	
t_{PLH}	OEB	$\overline{B}$	3.7	5.1	6.8			3.4	7	ns
t_{PHL}			2.9	4.4	6.2			2.4	6.4	
t_{PZH}	OEA	AO	1.8	3.3	5.1			1.5	5.6	ns
t_{PZL}			1.7	3.1	4.7			1.6	5	
t_{PHZ}	OEA	AO	1.9	3.3	5			1.3	5.3	ns
t_{PLZ}			1.1	2.6	4.3			0.9	4.7	
$t_{sk(p)}$	Skew for any single channel $\lvert t_{PHL} - t_{PLH} \rvert$	AI to $\overline{B}$ or $\overline{B}$ to AO		0.5						ns
$t_{sk(o)}$	Skew between drivers in the same package	AI to $\overline{B}$ or $\overline{B}$ to AO		0.4						ns
t_t	Rise time, 1.3 V to 1.8 V	$\overline{B}$	2.4	3.5	4.6			2.2	5.2	
	Fall time, 1.8 V to 1.3 V		1	2	3			1	3.4	
t_{PR}	$\overline{B}$-port input pulse rejection					1		1		ns

PARAMETER MEASUREMENT INFORMATION

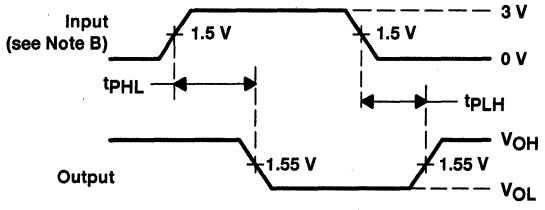


LOAD CIRCUIT FOR A OUTPUTS

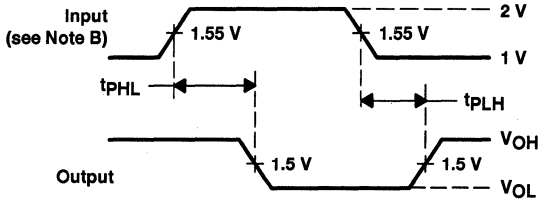


LOAD CIRCUIT FOR B OUTPUTS

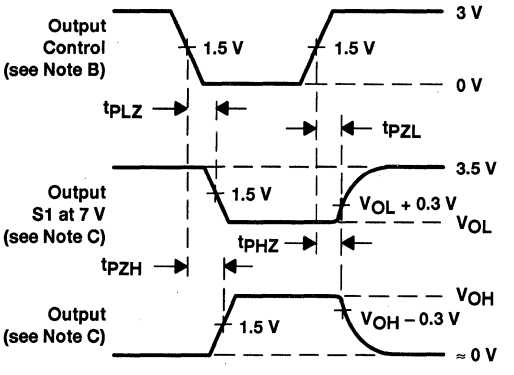
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: TTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns. BTL inputs – PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

- **Translates Between GTL Logic Levels and LVTTL or 5-V TTL Logic Levels**
- **Members of the Texas Instruments *Widebus*™ Family**
- **Support Mixed-Mode Signal Operation on A Port**
- **Universal Bus Transceiver (*UBT*™) Combines D-Type Latches and D-Type Flip-Flops With Qualified Storage Enable**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors on A Port**
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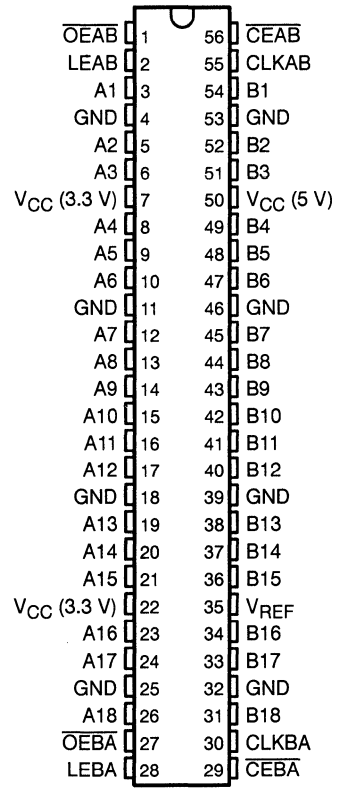
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Ceramic Flat (WD) Packages**

SN54GTL16612 . . . WD PACKAGE
SN74GTL16612 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

These 18-bit bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

The B port operates at GTL levels while the A port and control pins are compatible with LVTTL or 5-V TTL logic levels.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock or latch-enable can be controlled by the clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ is also low. $\overline{OEAB}$ is active low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that for A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54GTL16612 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74GTL16612 is characterized for operation from −40°C to 85°C.

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FUNCTION TABLE†

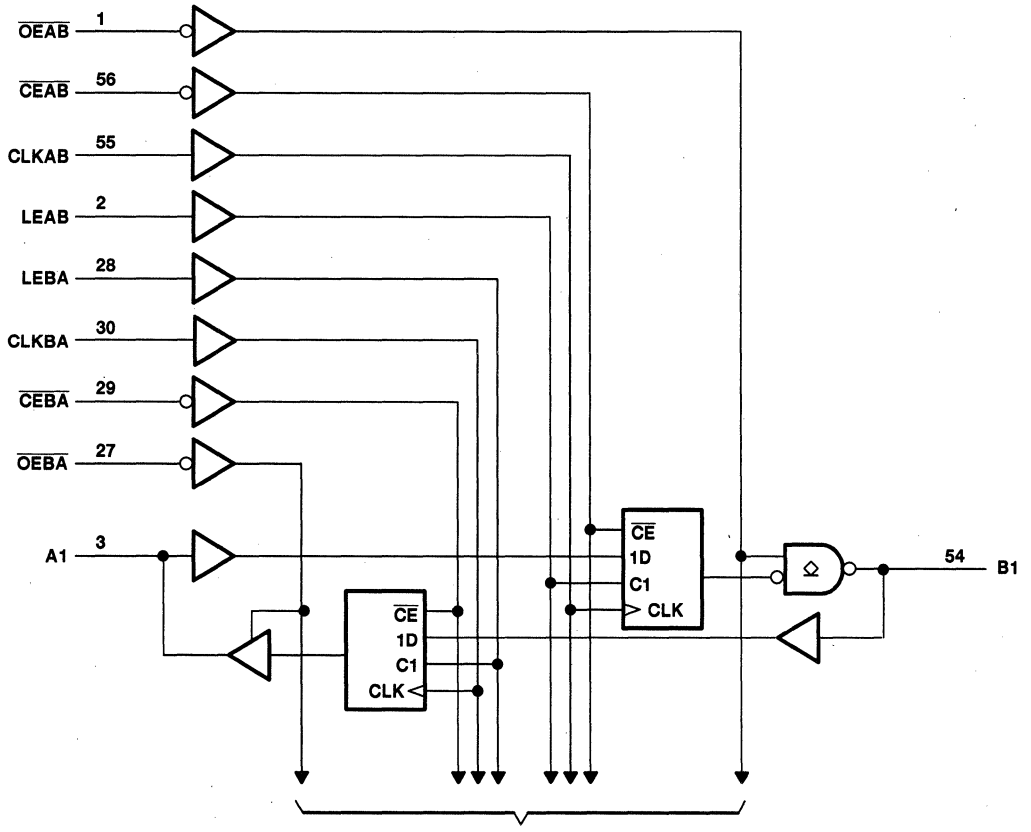
INPUTS					OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Latched storage of A data
L	L	L	H	X	B_0‡	
L	L	L	L	X	B_0§	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0§	Clock inhibit

† A-to-B data flow is shown: B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

§ Output level before the indicated steady-state input conditions were established.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}: 3.3 V ..... −0.5 V to 4.6 V
5 V ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1): A port ..... −0.5 V to 7 V
B port ..... −0.5 V to 4.6 V
Voltage range applied to any output in the high or power-off state, V_O (see Note 1): A port ..... −0.5 V to 7 V
B port ..... −0.5 V to 4.6 V
Current into any A-port output in the low state, I_O ..... 128 mA
Current into any B-port output in the low state, I_O ..... 80 mA
Current into any A-port output in the high state, I_O (see Note 2) ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Operating free-air temperature range, T_A: SN54GTL16612 ..... −55°C to 125°C
SN74GTL16612 ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54GTL16612			SN74GTL16612			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage, 3.3 V		3.15	3.3	3.45	3.15	3.3	3.45	V
	Supply voltage, 5 V		4.75	5	5.25	4.75	5	5.25	
V_{REF}	Supply voltage			0.8			0.8		V
V_I	Input voltage	B port			V_{CC} (3.3 V)			V_{CC} (3.3 V)	V
		Except B port			5.5			5.5	
V_{IH}	High-level input voltage	B port	V_{REF} + 50 mV			V_{REF} + 50 mV			V
		Except B port	2			2			
V_{IL}	Low-level input voltage	B port			V_{REF} − 50 mV			V_{REF} − 50 mV	V
		Except B port			0.8			0.8	
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	A port			−32			−32	mA
I_{OL}	Low-level output current	A port			64			64	mA
		B port			40			40	
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range, V_{REF} = 0.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54GTL16612			SN74GTL16612			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	A port	V_{CC} = MIN to MAX‡,	I_{OH} = −100 μA	V_{CC} − 0.2			V_{CC} − 0.2			V
		V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_{OH} = −8 mA	2.4			2.4			
			I_{OH} = −32 mA	2			2			
V_{OL}	A port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_{OL} = 100 μA			0.2			0.2	V
			I_{OL} = 16 mA			0.4			0.4	
			I_{OL} = 32 mA			0.5			0.5	
			I_{OL} = 64 mA			0.55			0.55	
	B port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_{OL} = 40 mA			0.4			0.4	
I_I	Control inputs	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10			10	μA
	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_I = 5.5 V			20			20	
			V_I = V_{CC}			1			1	
			V_I = 0			−30			−30	
	B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_I = V_{CC} (3.3 V)			5			5	
			V_I = 0			−5			−5	
I_{off}	A port	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V			100			100	μA
$I_{I(hold)}$	A port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	V_I = 0.8 V	75			75			μA
			V_I = 2 V	−75			−75			
I_{OZH}	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_O = 3 V			1			1	μA
	B port		V_O = 1.2 V			10			10	
I_{OZL}	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_O = 0.5 V			−1			−1	μA
	B port		V_O = 0.4 V			−10			−10	
I_{CC} (3.3 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (3.3 V) or GND	Outputs high			1			1	mA
			Outputs low			5			5	
			Outputs disabled			1			1	
I_{CC} (5 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (5 V) or GND	Outputs high			120			120	mA
			Outputs low			120			120	
			Outputs disabled			120			120	
ΔI_{CC}§		V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, A or control inputs at V_{CC} (3.3 V) or GND, One input at 2.7 V				1			1	mA
C_i	Control inputs	V_I = 3.15 V or 0			3.5			3.5		pF
C_{io}	A port	V_O = 3.15 V or 0			12			12		pF
	B port	Per IEEE Standard 1149.0-1991				5			5	

† All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (unless otherwise noted)

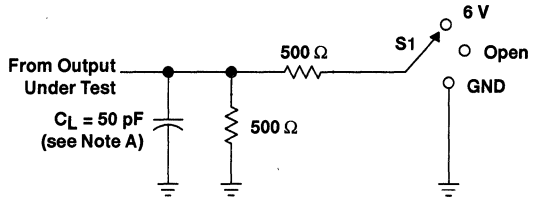
			SN54GTL16612		SN74GTL16612		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	95	0	95	MHz
t_w	Pulse duration	LEAB or LEBA high	3.3		3.3		ns
		CLKAB or CLKBA high or low	5.6		5.6		
t_{su}	Setup time	A before CLKAB↑	0.9		0		ns
		B before CLKBA↑	3.4		2.5		
		A before LEAB↓	1.2		0.4		
		B before LEBA↓	1		0.9		
		$\overline{CEAB}$ before CLKAB↑	2.1		1		
		$\overline{CEBA}$ before CLKBA↑	2.6		2.1		
t_h	Hold time	A after CLKAB↑	2.9		2.7		ns
		B after CLKBA↑	4.1		0.4		
		A after LEAB↓	4.5		3.4		
		B after LEBA↓	4.3		3.3		
		$\overline{CEAB}$ after CLKAB↑	2		1.5		
		$\overline{CEBA}$ after CLKBA↑	0.5		0.4		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (see Figure 1)

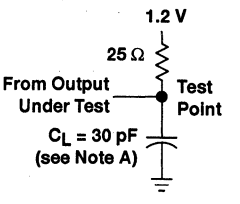
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54GTL16612			SN74GTL16612			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			95			95			MHz
t_{PLH}	A	B	1	2.6	3.8	1	2.6	3.8	ns
t_{PHL}			1	2.2	4	1	2.2	4	
t_{PLH}	LEAB	B	1.8	3.6	5.4	1.8	3.6	5.4	ns
t_{PHL}			1.5	3.3	5.5	1.5	3.3	5.5	
t_{PLH}	CLKAB	B	1.8	3.7	5.3	1.8	3.7	5.3	ns
t_{PHL}			1.5	3.3	5.5	1.5	3.3	5.5	
t_{PLH}	$\overline{OEAB}$	B	1.6	3.3	4.7	1.6	3.3	4.7	ns
t_{PHL}			1.3	3.2	5.5	1.3	3.2	5.5	
t_r	Transition time, B outputs (0.5 V to 1 V)			1.3			1.3		ns
t_f	Transition time, B outputs (1 V to 0.5 V)			0.5			0.5		ns
t_{PLH}	B	A	2	4.8	6.9	2	4.8	6.9	ns
t_{PHL}			1.4	3.6	5.1	1.4	3.6	5.1	
t_{PLH}	LEBA	A	2.1	4.3	6.1	2.1	4.3	6.1	ns
t_{PHL}			1.9	3.6	5.1	1.9	3.6	5.1	
t_{PLH}	CLKBA	A	2.3	4.5	6.4	2.3	4.5	6.4	ns
t_{PHL}			2.2	4	5.6	2.2	4	5.6	
t_{en}	$\overline{OEBA}$	A	1.9	4.7	7.2	1.9	4.7	7.2	ns
t_{dis}			2.5	4.6	6.9	2.5	4.6	6.9	

† All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

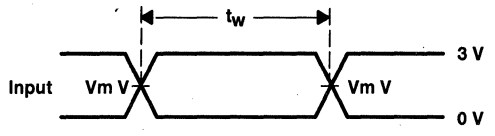


TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6 V GND

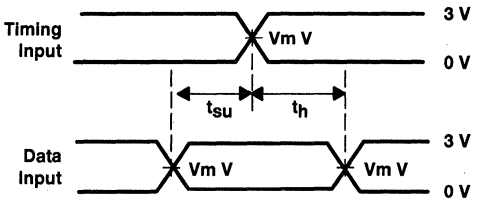


LOAD CIRCUIT FOR A OUTPUTS

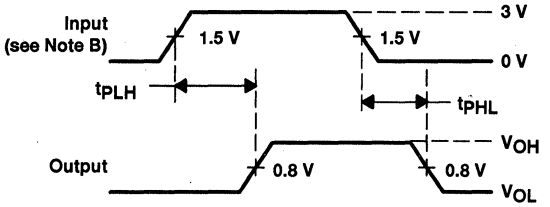
LOAD CIRCUIT FOR B OUTPUTS



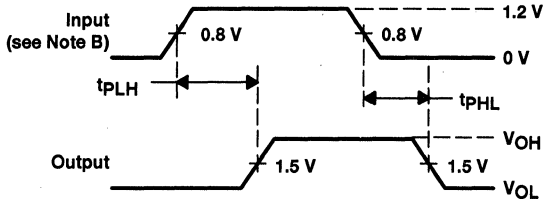
VOLTAGE WAVEFORMS
PULSE DURATION
(Vm = 1.5 V for A port and 0.8 V for B port)



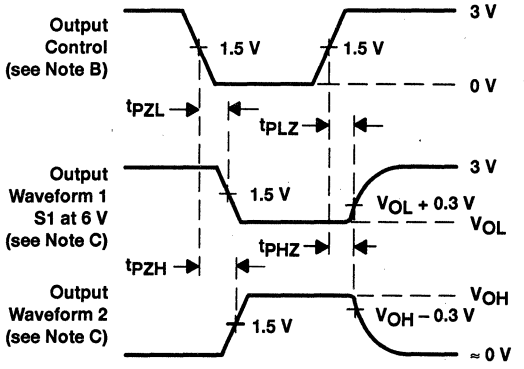
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(Vm = 1.5 V for A port and 0.8 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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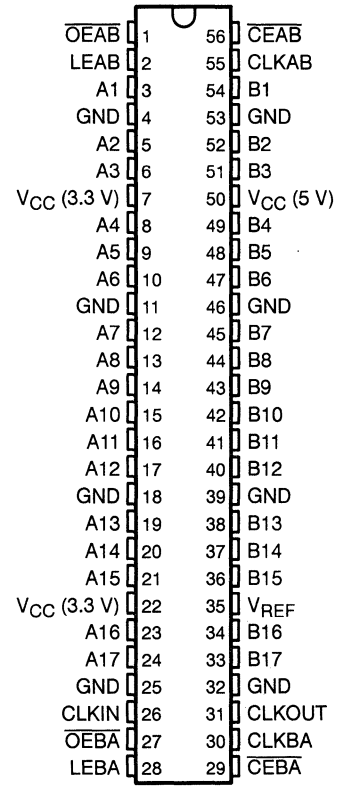
SN54GTL16616 . . . WD PACKAGE
SN74GTL16616 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

These 17-bit registered bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes. The 'GTL16616 provides for a copy of CLKAB at GTL logic levels (CLKOUT) and also provides a conversion of the GTL clock to a TTL environment (CLKIN).

The B port operates at GTL levels while the A port and control pins are compatible with LVCMOS, LVTTL, or 5-V TTL logic levels.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock or latch-enable can be controlled by the clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ is also low. $\overline{OEAB}$ is active low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74GTL16616 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54GTL16616 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74GTL16616 is characterized for operation from −40°C to 85°C.

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FUNCTION TABLE†

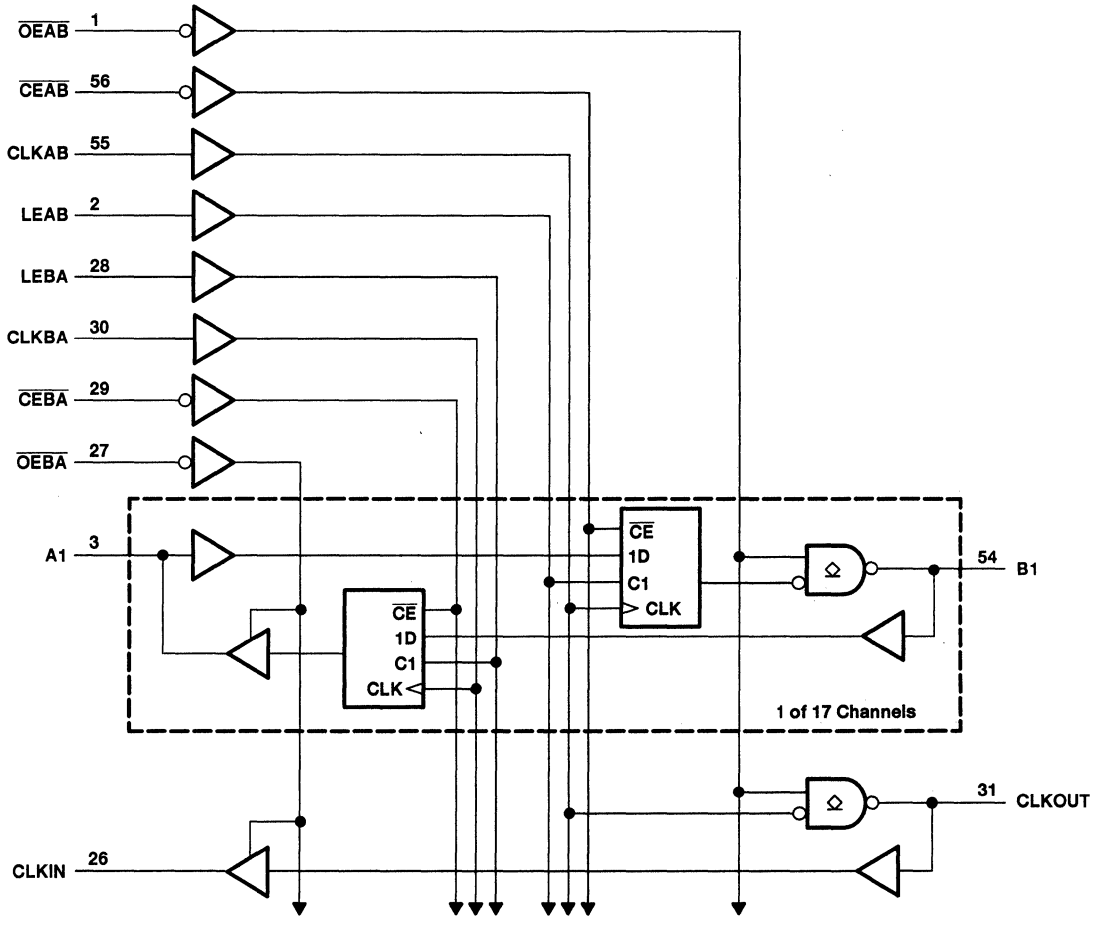
INPUTS					OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Latched storage of A data
L	L	L	H or L	X	B_0‡	
L	L	L	H or L	X	B_0§	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0§	Clock inhibit

† A-to-B data flow is shown: B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, $\overline{CLKBA}$, and $\overline{CEBA}$.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

§ Output level before the indicated steady-state input conditions were established.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}: 3.3 V ..... −0.5 V to 4.6 V
5 V ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1): A port ..... −0.5 V to 7 V
B port ..... −0.5 V to 4.6 V
Voltage range applied to any output in the high or power-off state, V_O (see Note 1): A port ..... −0.5 V to 7 V
B port ..... −0.5 V to 4.6 V
Current into any A-port output in the low state, I_O ..... 128 mA
Current into any B-port output in the low state, I_O ..... 80 mA
Current into any A-port output in the high state, I_O (see Note 2) ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will flow only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54GTL16616			SN74GTL16616			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage, 3.3 V		3.15	3.3	3.45	3.15	3.3	3.45	V
	Supply voltage, 5 V		4.75	5	5.25	4.75	5	5.25	
V_{REF}	Supply voltage			0.8			0.8		V
V_I	Input voltage	B port			V_{CC} (3.3 V)			V_{CC} (3.3 V)	V
		Except B port			5.5			5.5	
V_{IH}	High-level input voltage	B port	V_{REF} +50 mV			V_{REF} +50 mV			V
		Except B port	2			2			
V_{IL}	Low-level input voltage	B port			V_{REF} −50 mV			V_{REF} −50 mV	V
		Except B port			0.8			0.8	
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	A port			−32			−32	mA
I_{OL}	Low-level output current	A port			64			64	mA
		B port			40			40	
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range, V_{REF} = 0.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54GTL16616			SN74GTL16616			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	A port	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA	V_{CC} − 0.2			V_{CC} − 0.2			V
		V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_{OH} = − 8 mA	2.4			2.4			
			I_{OH} = − 32 mA	2			2			
V_{OL}	A port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_{OL} = 100 µA			0.2			0.2	V
			I_{OL} = 16 mA			0.4			0.4	
			I_{OL} = 32 mA			0.5			0.5	
			I_{OL} = 64 mA			0.55			0.55	
	B port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_{OL} = 40 mA			0.4			0.4	
I_I	Control inputs	V_{CC} = 0 or MAX‡,	V_I = 5.5 V			10			10	µA
	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_I = 5.5 V			20			20	
			V_I = V_{CC}			1			1	
			V_I = 0			−30			−30	
	B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_I = V_{CC} (3.3 V)			5			5	
			V_I = 0			−5			−5	
I_{off}	A port	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V			100			100	µA
$I_{I(hold)}$	A port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	V_I = 0.8 V	75			75			µA
			V_I = 2 V	−75			−75			
I_{OZH}	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_O = 3 V			1			1	µA
	B port		V_O = 1.2 V			10			10	
I_{OZL}	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_O = 0.5 V			−1			−1	µA
	B port		V_O = 0.4 V			−10			−10	
I_{CC} (3.3 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (3.3 V) or GND	Outputs high			1			1	mA
			Outputs low			5			5	
			Outputs disabled			1			1	
I_{CC} (5 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (5 V) or GND	Outputs high			120			120	mA
			Outputs low			120			120	
			Outputs disabled			120			120	
ΔI_{CC}§		V_{CC} (3.3 V) = 3.45 V, A or control inputs at V_{CC} (3.3 V) or GND, One input at 2.7 V	V_{CC} (5 V) = 5.25 V,			1			1	mA
C_i	Control inputs	V_I = 3.15 V or 0			3.5			3.5		pF
C_{io}	A port	V_O = 3.15 V or 0			12			12		pF
	B port	Per IEEE 1194.0-1991				5			5	

† All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (unless otherwise noted)

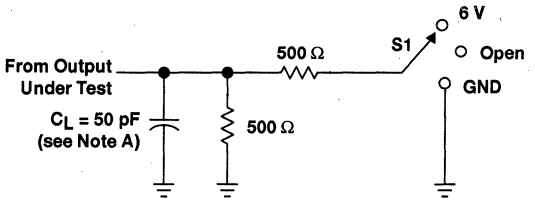
			SN54GTL16616		SN74GTL16616		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	95	0	95	MHz
t_w	Pulse duration	LEAB or LEBA high	3.3		3.3		ns
		CLKAB or CLKBA high or low	5.5		5.5		
t_{su}	Setup time	A before CLKAB↑	1.1		1.1		ns
		B before CLKBA↑	2.6		2.6		
		A before LEAB↓	0		0		
		B before LEBA↓	1		1		
		$\overline{CEAB}$ before CLKAB↑	1.8		1.8		
		$\overline{CEBA}$ before CLKBA↑	2.1		2.1		
t_h	Hold time	A after CLKAB↑	1.6		1.6		ns
		B after CLKBA↑	0.2		0.2		
		A after LEAB↓	4.3		4.3		
		B after LEBA↓	2.8		2.8		
		$\overline{CEAB}$ after CLKAB↑	0.8		0.8		
		$\overline{CEBA}$ after CLKBA↑	0.7		0.7		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54GTL16616			SN74GTL16616			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			95			95			MHz
t_{PLH}	A	B	1	2.5	3.8	1	2.5	3.8	ns
t_{PHL}			1	2	3.8	1	2	3.8	
t_{PLH}	LEAB	B	1.5	3.4	5.1	1.5	3.4	5.1	ns
t_{PHL}			1.4	3.2	5.1	1.4	3.2	5.1	
t_{PLH}	CLKAB	B	1.5	3.6	5	1.5	3.6	5	ns
t_{PHL}			1.4	4.1	5	1.4	4.1	5	
t_{PLH}	CLKAB	CLKOUT	3.4	6	7.7	3.4	6	7.7	ns
t_{PHL}			4.3	7.4	10.4	4.3	7.4	10.4	
t_{PLH}	$\overline{OEAB}$	B	1.3	3.2	5	1.3	3.2	5	ns
t_{PHL}			1.1	3.1	5	1.1	3.1	5	
t_r	Transition time, B outputs (0.5 V to 1 V)			1.2			1.2		ns
t_f	Transition time, B outputs (1 V to 0.5 V)			0.7			0.7		ns
t_{PLH}	B	A	2.1	4.4	6.5	2.1	4.4	6.5	ns
t_{PHL}			1.3	3.3	4.8	1.3	3.3	4.8	
t_{PLH}	LEBA	A	1.7	3.9	6	1.7	3.9	6	ns
t_{PHL}			1.3	3.3	4.6	1.3	3.3	4.6	
t_{PLH}	CLKBA	A	1.7	4.1	6.3	1.7	4.1	6.3	ns
t_{PHL}			1.4	3.6	5.3	1.4	3.6	5.3	
t_{PLH}	CLKOUT	CLKIN	6.5	10.5	14.3	6.5	10.5	14.3	ns
t_{PHL}			5.1	8.8	11.8	5.1	8.8	11.8	
t_{en}	$\overline{OEBA}$	A	1.8	4.7	6.9	1.8	4.7	6.9	ns
t_{dis}			2	4.7	6.7	2	4.7	6.7	

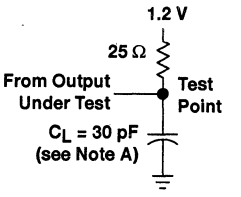
† All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

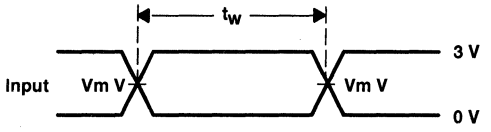


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

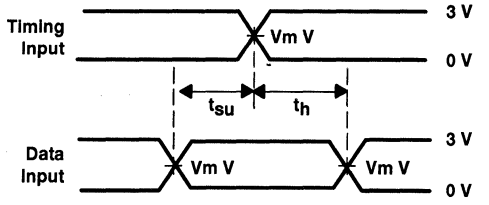
LOAD CIRCUIT FOR A OUTPUTS



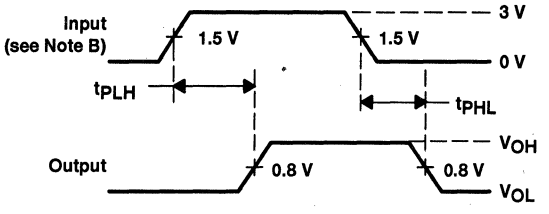
LOAD CIRCUIT FOR B OUTPUTS



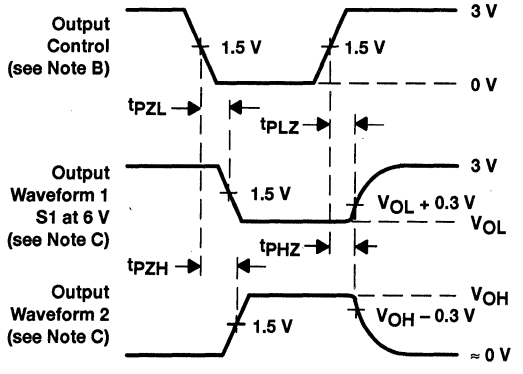
VOLTAGE WAVEFORMS
PULSE DURATION
(Vm = 1.5 V for A port and 0.8 V for B port)



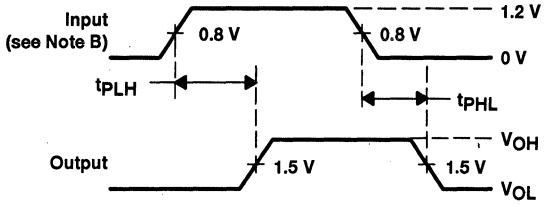
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(Vm = 1.5 V for A port and 0.8 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

7 Application Report

TNETS2020A/TNETS2021A Advanced STS-1/DS-3 Receiver/Transmitter

TEXAS INSTRUMENTS

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Contents

List of Illustrations

Introduction

This application report provides information on the operation and use of the Texas Instruments TNETS2020A and TNETS2021A advanced STS-1/DS-3 receiver/transmitter devices. These devices provide a single-chip solution for interfacing DS-3 or STS-1 signals to DSX or STX cross-connect frames. This report is intended to supplement existing information and serve as a reference in the design and integration of systems utilizing these products. Additional assistance is available through sources listed under references at the end of this report.

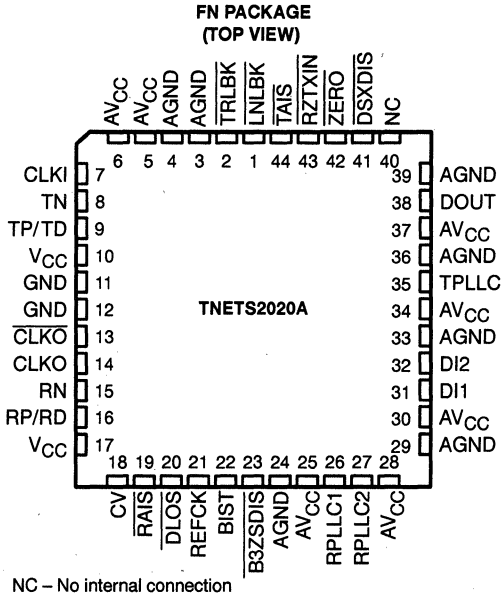
The TNETS2020A and TNETS2021A are members of a line of products that provide broadband solutions for both local- and wide-area networks. Each device can be operated from a single 5-V power supply to provide the functions necessary to interface DS-3 (44.736 Mbit/s) or STS-1 (51.840 Mbit/s) signals to DSX or STX cross-connect frames. Each device can receive and transmit data simultaneously.

During receive operations (receiving DS-3/STS-1 data), each device provides automatic-gain control (AGC) and adaptive equalization to recover a pulse transmitted over coaxial cable up to 450 feet in length. Depending on the setup, the DS-3/STS-1 input signal is decoded (from B3ZS) and converted to a CMOS signal of nonreturn-to-zero (NRZ) or P-data and N-data formats (a high in the P data represents a bipolar + 1, and a high in the N data represents a bipolar – 1). An on-chip phase-locked loop (PLL) is utilized in the clock-recovery circuit to obtain a CMOS-level clock from the incoming data stream.

For transmit operations (transmitting DS-3/STS-1 data), each device can accept CMOS-level inputs in NRZ data or P- and N-data formats. Prior to input into the TNETS2020A or TNETS2021A, P and N data are encoded to meet B3ZS line-code requirements for DS-3 or STS-1 signals. B3ZS encoding can be performed in the TNETS2020A and TNETS2021A if NRZ data is used as the input. Before transmission, signals are processed to meet pulse-mask requirements for DS-3 or STS-1 communications. On-chip line drivers allow direct interface with a 75-Ω coaxial output cable (AT&T 728A/734A or equivalent).

The TNETS2020A and TNETS2021A provide all functions required to interface to DS-3 or STS-1 communication channels. The TNETS2021A has all the terminals and features of the TNETS2020A, as well as additional capabilities for monitoring, testing, and configuring the device. Details on the additional features of the TNETS2021A are provided in this report.

Both devices are available in cost-effective plastic packages. Due to its increased capabilities, the TNETS2021A comes in a 68-terminal plastic leaded chip carrier; the TNETS2020A is available in a 44-terminal plastic leaded chip carrier (see Figure 1).



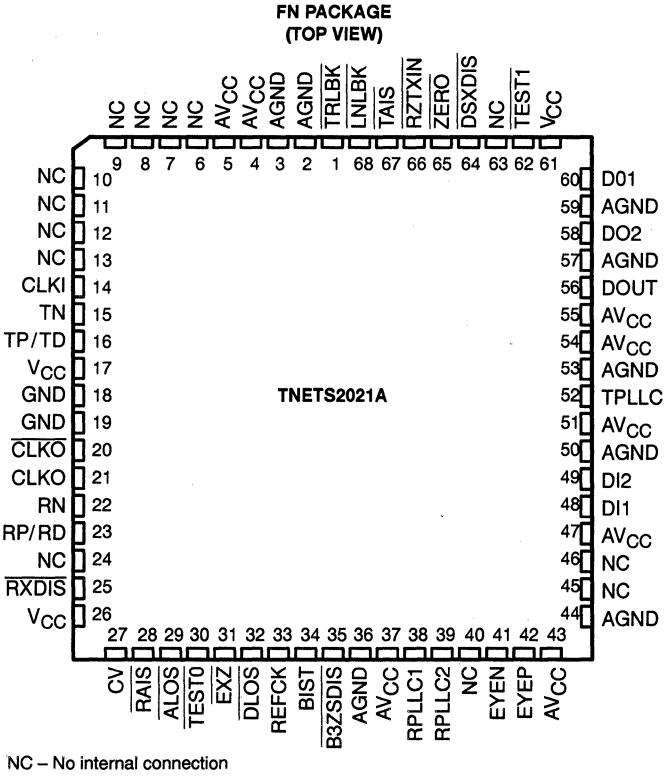


Figure 1. TNETS2020A/TNETS2021A Terminal Layouts

Application Information

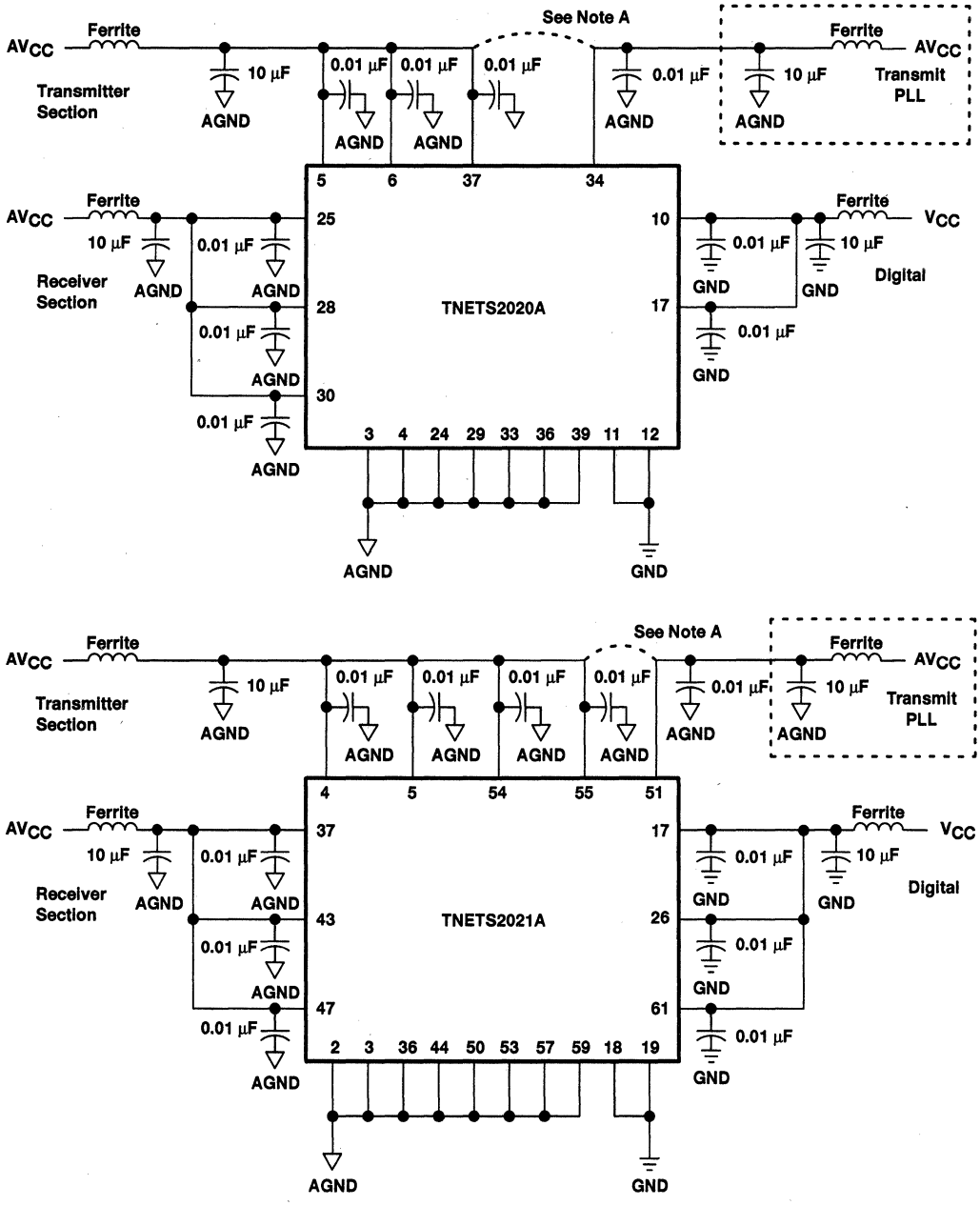
The TNETS2020A and TNETS2021A devices can be used in a variety of applications. The following paragraphs provide insight into the operation and application of the devices with answers to commonly asked questions.

Power Connections

Terminal layouts of the TNETS2020A and TNETS2021A identify separate analog and digital power connections. To provide common references, the analog and digital power connections are tied together on the chip with a single, thin, metal via. This via connects the analog and digital power signals. The nature of the thin connection provides some degree of noise immunity between the power signals. For example, eddy currents are reduced with this layout technique and on-chip noise is reduced due to lower chip inductance.

The TNETS2020A and TNETS2021A function properly with a single power supply. In this case, it is recommended that nodes for analog and digital power be split as far from the TNETS2020A/TNETS2021A as possible to provide independent traces to the chip. This ensures optimal noise immunity for the device. To reduce high-frequency noise, decoupling measures should be taken. It is also recommended that each node be decoupled through a series ferrite-bead inductor (e.g., FairRite part no. 2743002111) and a single 10-μF (6.3-V) capacitor connected to that node's ground (GND or AGND). The ferrite bead serves as a series inductance to attenuate high-frequency noise induced on the power terminals and to prevent noise from passing to other nodes and devices. In addition to the 10-μF capacitor, it is recommended that each V_{CC} and AV_{CC} terminal be decoupled through a 0.01-μF capacitor placed as close to the power terminal as reasonably possible. Figure 2 shows the recommended power connections for the TNETS2020A and TNETS2021A devices.

To allow for reduced power requirements in receive-only or transmit-only applications, analog power connections for each mode of operation are provided through separate terminals. Figure 2 shows the separate power connections for each device. To reduce power consumption in receive-only applications, terminals 5, 6, and 37 (TNETS2020A) or terminals 4, 5, 54, and 55 (TNETS2021A) should be connected to analog ground (AGND). Tests performed on initial versions of the devices indicate that this action results in a power-supply current reduction of approximately 15 mA. Similarly, in transmit-only applications, terminals 25, 28, and 30 (TNETS2020A) or terminals 37, 43, and 47 (TNETS2021A) should be connected to AGND for a power-supply current reduction of approximately 70 mA. Initial tests, in both the transmit-only and receive-only modes, resulted in only a slight reduction (less than 0.01-UI peak-to-peak) in jitter in the enabled data path.



NOTE A: The transmit-PLL ferrite bead and 10-µF capacitor (enclosed by dotted line) can be eliminated by connecting the transmit-PLL 0.01-µF capacitor node to the transmitter-section node (if in a transmit-only mode), as shown by the dotted line, or by connecting the 0.01-µF capacitor to the receiver-section node (if in a receive-only or transmit and receive mode).

Figure 2. TNETS2020A/TNETS2021A Recommended Power Connections

Data-Line External Components

Due to the high frequencies involved, care should be taken when terminating data lines. The following paragraphs provide recommendations for these and other external (passive) components.

Receive-Data Line

During receive operations, DS-3 or STS-1 signals are provided across TNETS2020A/TNETS2021A terminals DI1 and DI2. The recommended procedure is to direct the signal through an external transformer (e.g., Micro-Circuits Laboratory MCL part T1-1). This transformer is not required if the input signal is ac coupled through a capacitor. With differential operation, a step-down transformer can be used to ensure that the maximum ac voltage level (1-V differential) is not exceeded.

Whether or not a transformer is used, the transmission line carrying the DS-3 or STS-1 data must be properly terminated. The recommended method is to connect two equal-value resistors in series between DI1 and DI2 on the device side of the transformer or the ac-coupling capacitor. The resistance of each component should be one-half of the transmission line's characteristic impedance (real part only). A 0.01-µF capacitor should be connected from analog ground (AGND) to the node between the two equal-value resistors. Figure 3 shows the recommended component values and connections for a 75-Ω coaxial transmission-line input. If single-ended operation is desired, the input is connected to DI1 or DI2. In this case, the unused input is connected to analog ground through a capacitor. Figure 4 shows typical components used for signal-ended inputs with and without a transformer.

The TNETS2020A/TNETS2021A outputs for the receive-data channel (RP/RD, RN, CLKO, $\overline{\text{CLKO}}$) are CMOS-level signals and are handled accordingly.

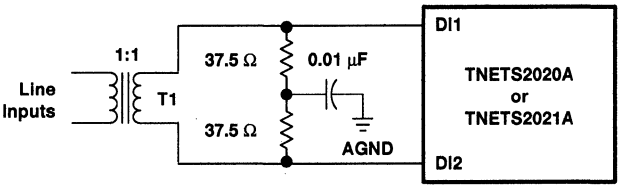
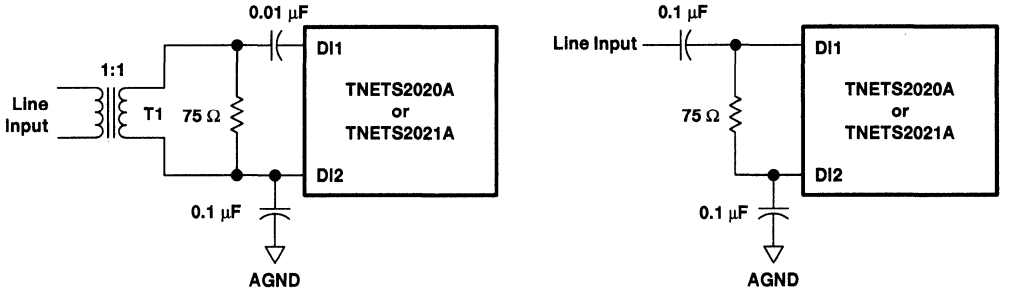


Figure 3. TNETS2020A/TNETS2021A Differential-Input Line Components



(a) INPUT WITH TRANSFORMER

(b) INPUT WITHOUT TRANSFORMER

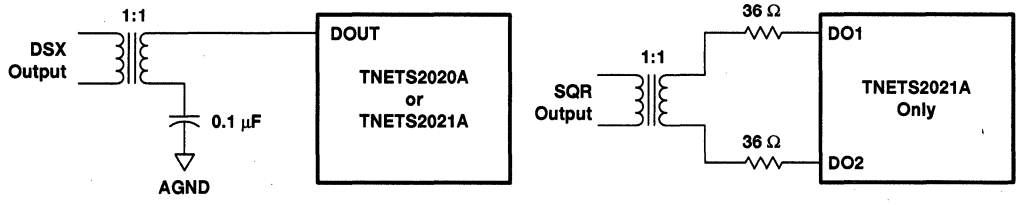
Figure 4. TNETS2020A/TNETS2021A Single-Ended-Input Line Components

Transmit-Data Line

During transmit operations using the TNETS2020A or TNETS2021A, digital inputs are converted to DS-3 or STS-1 formats for transmission on coaxial cable. The digital inputs are either NRZ or P and N data. The data (TP/TD, TN) and the associated clock (CLKI) are provided at CMOS levels.

The DSX line-side output (DOUT) carries signals of DS-3 or STS-1 format and is designed to drive a line transformer directly. DOUT is single ended and is connected to the line transformer. The other side of the transformer is connected to the analog ground (AGND) through a 0.1-μF capacitor. A capacitor for ac coupling can be used in place of the line transformer when the signal satisfies the DS-3 or STS-1 requirements [see Figure 5 (a)].

The TNETS2021A device can provide rectangular pulses that represent level-translated versions of the P-/N-data digital signals. These pulses are output across DO1 and DO2. It is recommended that DO1 be connected through a 36-Ω resistor to one side of a line transformer and DO2 be connected through a separate 36-Ω resistor to the other side of the line transformer [see Figure 5(b)].



(a) RECOMMENDED DOUT OUTPUT CONNECTIONS

(b) TYPICAL DO1/DO2 OUTPUT CONNECTIONS

Figure 5. TNETS2020A/TNETS2021A Output Line Components

Phase-Locked Loop Capacitors

External connections for additional control of the transmit and receive PLLs are provided in both the TNETS2020A and TNETS2021A. No external connections are required for the receive PLL control terminals (RPLLC1 and RPLLC2). A 0.01-μF calibration capacitor is required for the transmit PLL. This capacitor should be connected between TPLLC and AGND.

Eye-Pattern Monitor Resistors

The TNETS2021A provides terminals for monitoring the DS-3/STS-1 signals in the receive chain after they are equalized and gain controlled but before clock recovery and decoding. These eye-pattern monitor terminals (EYEP and EYEN) should be connected to AGND through a 1-kΩ resistor. This resistor is necessary for monitoring purposes only, but not for device operation. If monitoring is not required, the EYEP and EYEN terminals are left open (no connection).

Data-Type Selection and Processing

The TNETS2020A/TNETS2021A devices convert DS-3 or STS-1 data to/from NRZ or P and N data. A CMOS-level clock must be provided to the device at the REFCK terminal for the device to operate. Generally, REFCK should be supplied by the local oscillator on the board where the TNETS2020A/TNETS2021A is installed. The frequency of REFCK is 51.840 MHz for STS-1 applications and 44.736 MHz for DS-3 applications. The tolerance is ±200 ppm (±20 ppm if a valid DS-3 AIS pattern is required). Figure 6 and Figure 7 are functional block diagrams of the devices.

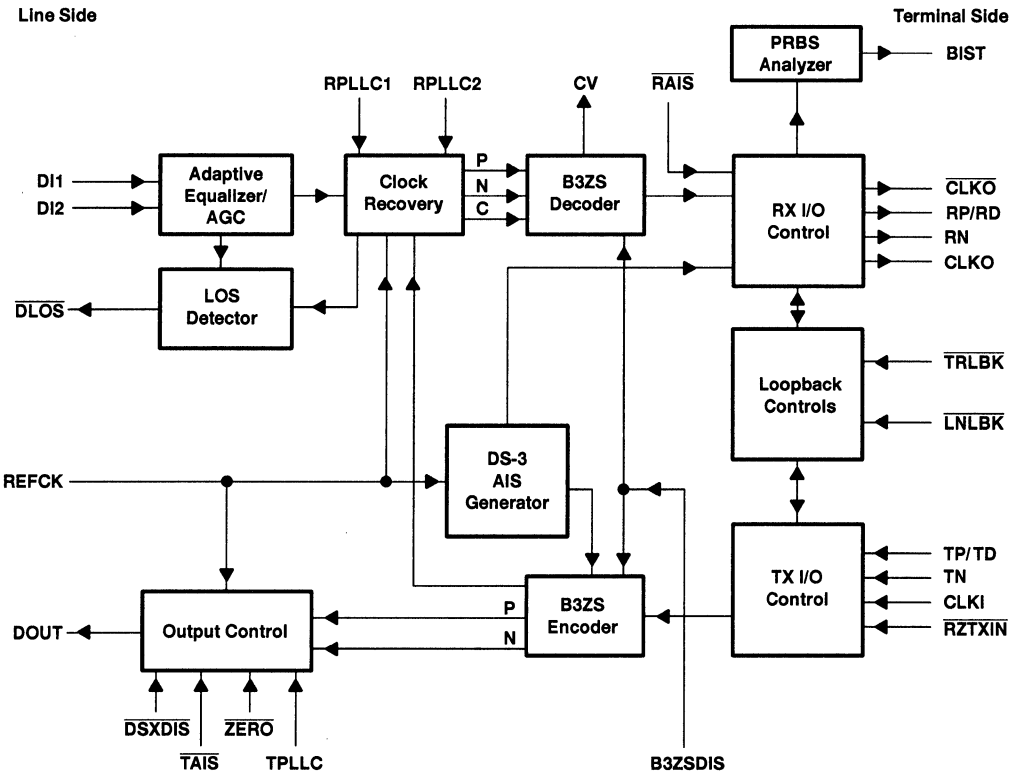


Figure 6. TNETS2020A Functional Block Diagram

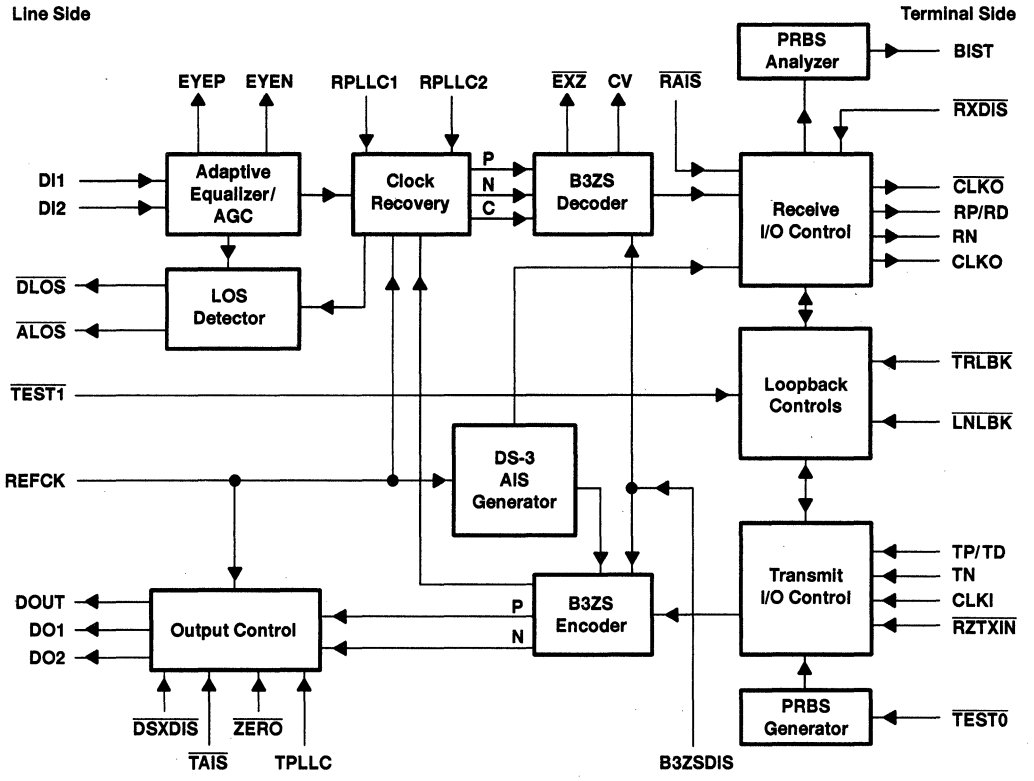


Figure 7. TNETS2021A Functional Block Diagram

Receive Path

The data-reception operations of the TNETS2020A/TNETS2021A involve the conversion of DS-3 or STS-1 data to NRZ or P and N data. The following paragraphs describe the associated control and monitoring of these operations.

Data Input

For receive operations, the TNETS2020A and TNETS2021A accept either DS-3 or STS-1 signals across DI1 and DI2. No external control is required to select between the two signal formats (DS-3/STS-1). For optimum performance, a differential input across DI1 and DI2 should be used. A single-ended input can be used if noise immunity is less critical or if use of a line transformer is not feasible. In any case, the input must be ac coupled to the device and a stepdown transformer or resistive-attenuation circuit should be used to maintain a maximum differential input voltage below 1-V peak.

Equalization/AGC

The devices include automatic gain control (AGC) and adaptive equalization to recover DS-3 or STS-1 signals transmitted on coaxial cable up to 450 feet long. AT&T 728A / 734A (or equivalent) is the preferred coaxial cable for the DS-3/STS-1 interface. To use the device in applications where signals are attenuated beyond the standard pulse mask, the AGC circuit has a 29-dB dynamic range, which makes it capable of recovering signals from 35 mV to 1 V. The TNETS2021A provides eye-pattern monitoring terminals (EYEP and EYEN) to examine the respective noninverted and inverted equalized and gain-controlled signals.

Clock Recovery/LOS

The TNETS2020A and TNETS2021A provide clock recovery and loss-of-signal (LOS) detection. The clock recovery utilizes a PLL to obtain a CMOS-level clock signal from the equalized and gain-controlled data stream. Each device also monitors the data stream and provides an output terminal to indicate when the data stream has a string of 175 ±75 consecutive zeroes. When this condition occurs, $\overline{\text{DLOS}}$ transitions to a low state. $\overline{\text{DLOS}}$ remains low until the pulse density (the number of logical ones in the data stream) exceeds 33% (nominal) for 175 ±75 pulses.

The TNETS2021A also provides an analog loss-of-signal terminal ($\overline{\text{ALOS}}$). $\overline{\text{ALOS}}$ is specified low when the pulse density is below 28% for 175 ±75 pulses and is cleared when the pulse density exceeds 33% for 175 ±75 pulses. $\overline{\text{ALOS}}$ can toggle between active and inactive when the pulse density is between 28% and 33% for 175 ±75 pulses.

B3ZS Decoding

The B3ZS decoding function is enabled when $\overline{\text{B3ZSDIS}}$ is high. When enabled, the incoming B3ZS data is decoded and B3ZS coding errors (TNETS2020A and TNETS2021A) and excessive zeroes (TNETS2021A only) are monitored. The coding-violation output (CV) goes high when incoming data violates B3ZS encoding requirements for excess zeroes or bipolar transitions. CV goes low when a valid data sequence is detected. The TNETS2021A also has an excessive-zeroes output ($\overline{\text{EXZ}}$), which goes low when a string of at least three zeroes is encountered. This signal remains low until a one is detected. B3ZS decoder functions are disabled when $\overline{\text{B3ZSDIS}}$ is low.

Receiver Output

During normal TNETS2020A/TNETS2021A receive operations, two types of data can be output at CMOS levels on RP/RD and RN. If $\overline{\text{B3ZSDIS}}$ is high, decoded NRZ data is available on the RP/RD output and RN is held low. If $\overline{\text{B3ZSDIS}}$ is low, encoded P (positive pulse) and N (negative pulse) data are available on the RP/RD and RN outputs, respectively. The RP/RD terminal contains positive-rail data and the RN terminal contains negative-rail data. This latter condition is desirable when an external device (e.g., a framer) is used to perform the B3ZS decoding functions. In either mode, the recovered clock (CLKO) and its complement ($\overline{\text{CLKO}}$) are available at the receiver output. The TNETS2021A has a receiver-output disable function. If $\overline{\text{RXDIS}}$ is low, RP/RD and RN are forced and held low. If $\overline{\text{RXDIS}}$ is high, receiver outputs are enabled and take on values as previously described.

The TNETS2020A and TNETS2021A have receiver output controls for generating DS-3 alarm-indication signals (AIS) on the receiver output. If $\overline{\text{RAIS}}$ is low, the generation of DS-3 AIS (compliant with TR191) on the receiver output lines is enabled. If $\overline{\text{RAIS}}$ is high, normal receiver outputs are enabled. The AIS generation is valid only for DS-3 operations; therefore, input data must include the correct overhead for path sectionalizing if STS-1 operation is implemented.

The TNETS2020A and TNETS2021A can operate in a terminal-side loopback mode where transmit-side inputs (TP/TD, TN, and CLKI) are directly routed to the receiver outputs (RP/RD, RN, and CLKO). This loopback path is activated when $\overline{\text{TRLBK}}$ is low and is deactivated when $\overline{\text{TRLBK}}$ is high. The terminal-side loopback function can be operated independently of the line-side loopback function. Terminal-side loopback is not available when in a receive-AIS mode (the $\overline{\text{TRLBK}}$ terminal is disabled when $\overline{\text{RAIS}}$ is low).

Transmit Path

Data-transmission operations of the TNETS2020A and TNETS2021A involve the conversion of NRZ or P and N data to DS-3 or STS-1 data. The following paragraphs describe the associated control and monitoring of these operations.

Data Input

For transmit operations, the TNETS2020A and TNETS2021A can accept data in any of the following formats on the TP/TD and TN terminals:

- Unencoded NRZ data
- B3ZS-encoded NRZ data
- B3ZS-encoded P and N data

To accept unencoded NRZ data at the transmit input, $\overline{\text{B3ZSDIS}}$ and $\overline{\text{RZTXIN}}$ are both connected high. A high $\overline{\text{B3ZSDIS}}$ enables the B3ZS encoder and decoder and a high $\overline{\text{RZTXIN}}$ indicates that the input data is NRZ. Valid NRZ data is input into TP/TD. TN must be low. The data input clock is provided on CLKI. The receive-side B3ZS decoder and the transmit-side B3ZS encoder are enabled and disabled by the same terminal ($\overline{\text{B3ZSDIS}}$). Consequently, the device cannot simultaneously encode transmit data without decoding receive data and vice versa.

To input B3ZS-encoded NRZ data, $\overline{\text{B3ZSDIS}}$ is low (to disable the encoder) and $\overline{\text{RZTXIN}}$ is high (to indicate that NRZ data is being used). In this mode, positive data is processed on the TP/TD input and negative data is processed on the TN input. CLKI is the input clock signal.

To input B3ZS-encoded P and N data (RZ data), $\overline{\text{RZTXIN}}$ is low. This indicates that RZ data is present at the transmit-side input. TP/TD contains positive data and TN contains negative data. Because B3ZS encoding is not performed on RZ data (P and N data), $\overline{\text{B3ZSDIS}}$ must always be low when $\overline{\text{RZTXIN}}$ is low. CLKI is ignored in this mode and is held low. Controls for the various transmit data formats are summarized as follows:

INPUT FORMAT	$\overline{\text{B3ZSDIS}}$	$\overline{\text{RZTXIN}}$
Unencoded NRZ data	H	H
B3ZS-encoded NRZ data	L	H
B3ZS-encoded P- and N-data	L	L

B3ZS Encoding

When unencoded NRZ data is input into the transmit-side input, B3ZS encoding (compliant with ANSI TI.102A) can be performed on the device. This mode is enabled when $\overline{\text{B3ZSDIS}}$ and $\overline{\text{RZTXIN}}$ are high.

Transmitter Output

During normal TNETS2020A and TNETS2021A transmit operations, data is provided (single ended) on DOUT. The output-control circuitry transforms the B3ZS-encoded signal into pulses that meet the templates required for DS-3 and STS-1 lines. An internal line driver allows the devices to directly drive a coaxial-output cable or line transformer. DOUT is disabled (low) when $\overline{\text{DSXDIS}}$ is low.

The TNETS2021A has additional outputs, DO1 and DO2, that are rectangular pulses representing B3ZS encoded P- and N-data without the effects of DS-3/STS-1 pulse shaping. These outputs are enabled when $\overline{\text{DSXDIS}}$ is low. DO1 is a positive-pulse output and DO2 is a negative-pulse output.

If DOUT is to be transmitted on a short cable (less than 50 feet), the DOUT pulse shape is improved by asserting $\overline{\text{ZERO}}$ (connect the $\overline{\text{ZERO}}$ terminal low). This effectively negates some of the pulse shaping performed for transmission on long (up to 450 feet) coaxial cables.

As mentioned previously, TPLLC is provided for tuning the internal transmit PLL filter. It is recommended that a 0.01-μF capacitor be connected between this terminal and AGND.

The TNETS2020A and TNETS2021A provide an input ($\overline{\text{TAIS}}$) to enable the generation of a DS-3 AIS. When $\overline{\text{TAIS}}$ is low, AIS format signals are generated and available on the transmitter output (when $\overline{\text{TAIS}}$ is low, the AIS signal is transmitted on DOUT if $\overline{\text{DSXDIS}}$ is high). As only DS-3 format AIS is generated, inputs must include the correct overhead for path sectionalization when utilizing STS-1 operation.

The TNETS2020A and TNETS2021A can be operated in a line-side loopback mode. In this mode, receive-side DS-3/STS-1 inputs (DI1 and DI2) are routed through the receive channel and fed back (on the device) to the transmit-channel input function (where normal transmit-channel processing begins). In this mode, the data is ultimately made available at the transmit output (DOUT), if enabled, or DO1 and DO2 (TNETS2021A only). This loopback mode is enabled when $\overline{\text{LNLBK}}$ is low and can be operated independently of the terminal-side loopback function (controlled by $\overline{\text{TRLBK}}$).

Testability

The TNETS2020A and TNETS2021A have a 15-bit pseudorandom bit-sequence (PRBS) generator and analyzer and a built-in self-test (BIST) output that is high if a proper 2^{15}-bit pattern is detected near the receive-channel output. Only the TNETS2021A provides external control of the PRBS generator. The built-in self-test function of the TNETS2020A can only be used if a valid PRBS is externally input into the device and routed by the normal receive-channel controls to the receive output. In general, the TNETS2020A self-test function is used only as a manufacturing test (e.g., to screen the die).

In the TNETS2021A, a PRBS is driven into the transmitter input path when $\overline{\text{TEST0}}$ is low. This PRBS proceeds through the normal transmit path, including the B3ZS encoding function, to DOUT (if $\overline{\text{DSXDIS}}$ is high). From DOUT, the signal

can be looped back to the receiver (DI1 or DI2) via an external capacitor, where it can be passed through normal receiver functions to the output (RP/RD and RN). BIST goes low if an invalid bit pattern is detected near the receive-channel output.

The TNETS2021A also provides an alternative terminal-side loopback mode that tests many device functions without the need for the external capacitor. When $\overline{\text{TEST1}}$ is low, transmitter-input signals (TP/TD and TN) are routed to receive outputs RP/RD and RN by the way of the transmit input, transmit B3ZS encoding, receive-clock recovery, receive B3ZS decoding, and receive-output functions. This loopback mode provides increased testability over the normal terminal-side loopback. Because this loopback mode can be exercised with or without the PRBS self test, it is not independent of the normal line-side and terminal-side loopback methods. When $\overline{\text{TEST1}}$ is low (enabling this loopback path), it is recommended that both $\overline{\text{TRLBK}}$ and $\overline{\text{LNLBK}}$ be held high.

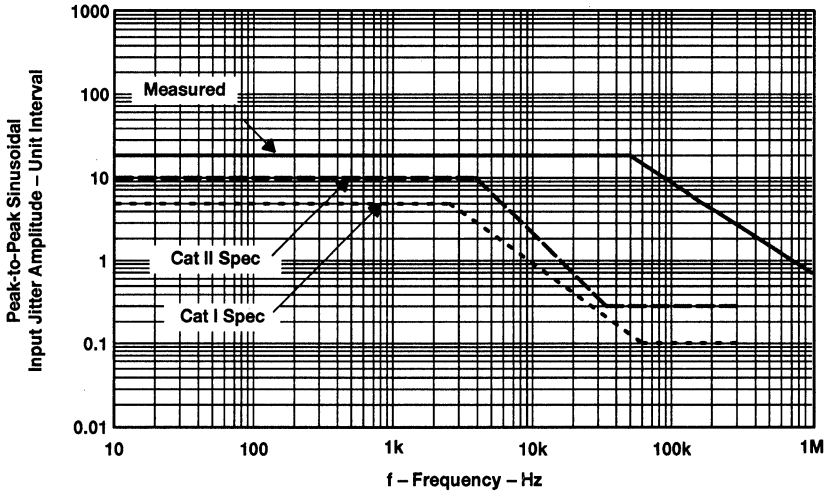
Summary of Experimental Data

Jitter Performance

Preliminary tests on the TNETS2021A have allowed jitter performance to be qualitatively characterized. Typical data from such tests follows. This information is for reference only and is not intended to be used as precise performance parameters for these devices. Although the data was taken on the TNETS2021A, results are also applicable to the TNETS2020A.

Receiver-Jitter Tolerance

Receiver-jitter tolerance data is shown in Figures 8 and 9. The device meets DS-3 jitter-tolerance requirements (as specified in Bellcore TR-TSY-000499) for both Category I and Category II equipment (see Figure 8). The flat tolerance from 10 Hz to 40 kHz results from an overrange condition in the test equipment. Actual jitter tolerance in this range exceeded 20-UI peak-to-peak. For STS-1, jitter-tolerance requirements (as specified in Bellcore TR-NWT-000253) are exceeded (see Figure 9).



Test setup:					
Instrument:	HP3784A	Transmit interface:	XCON 75 B3ZS	Receive interface:	Binary TTL
Temperature:	Room	Transmit clock:	Standard rate DS-3 + 0 ppm	Receive clock:	DS-3
Supply:	5 V	Transmit pattern:	PRBS 15 zero substitution 000	Receive pattern:	As per transmit
Filtering:	None			Receive hit threshold:	0.500 UIP

Figure 8. DS-3 Receive-Jitter Tolerance Measurement

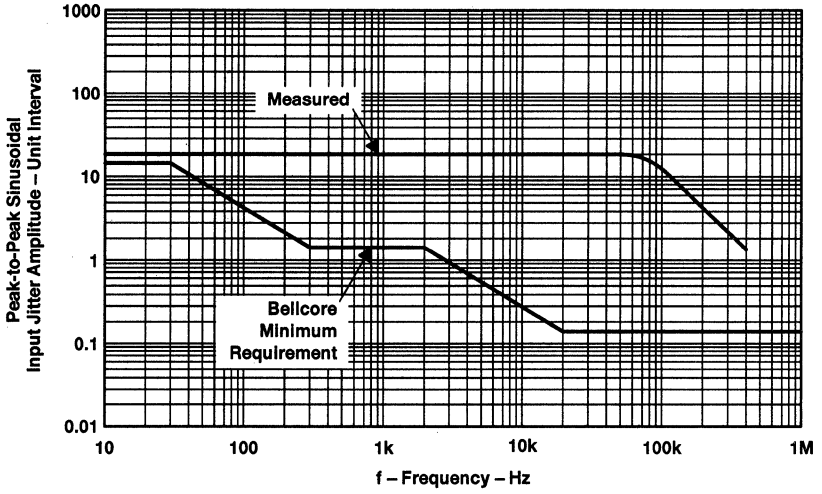
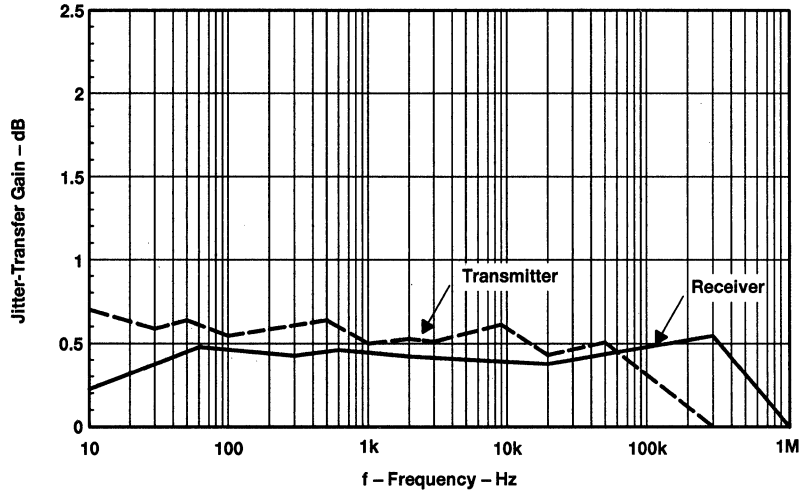


Figure 9. STS-1 Receive-Jitter Tolerance Measurement

Jitter Transfer

DS-3 jitter-transfer data for the receiver and transmitter sections of the TNETS2021A is shown in Figure 10. The device did not (and was not designed to) meet the TR-TSY-000499 jitter-transfer requirements (< 0.1 dB) for Category II equipment (regenerators). TR-TSY-000499 does not impose requirements for Category I equipment of this type. Such requirements are application dependent.



Test setup (receive-jitter testing; transmit-jitter testing is similar):

Instrument:	HP3784A	Jitter input:	0.75-UI peak to peak	Receive interface:	Binary TTL
Temperature:	Room	Transmit interface:	XCON 75 B3ZS	Receive clock:	DS-3
Supply:	5 V	Transmit clock:	Standard rate DS-3 + 0 ppm	Receive pattern:	As per transmit
Filtering:	10-Hz HP	Transmit pattern:	PRBS 15 zero substitution 000	Receive hit threshold:	0.500 UIP

Figure 10. Jitter-Transfer Measurement

Jitter Generation

No plots of jitter generation are currently available. Initial DS-3 tests have found receiver-jitter generation to be approximately 0.1-UI peak to peak. This value was measured in tests that exercised the normal receive-data path as well as tests that looped data from receiver inputs to transmitter outputs. These tests were performed under the following conditions:

- Room temperature
- 5-V power supply
- 2^{15} PRBS
- HP3784A analyzer (with a 10-Hz high-pass filter)

Similar testing found transmitter jitter to be approximately 0.05-UI peak to peak. This value was measured in tests that exercised the normal transmit-data path as well as tests that looped data from transmitter inputs to receiver outputs.

References

The following sources provide additional information regarding the operation of the TNETS2020A and TNETS2021A.

Data Sheets

The following data sheets provide detailed information on the TNETS2020A and TNETS2021A and are available through Texas Instruments contacts listed below. In the event of a conflict between the information in the following data sheets and the information presented in this application report, the data sheets take precedence.

TNETS2020A	Advanced STS-1/DS-3 Receiver/Transmitter Product Preview SDNS006C – Revised December 1994
TNETS2021A	Advanced STS-1/DS-3 Receiver/Transmitter Product Preview SDNS018B – Revised December 1994

Standards

The following standards are pertinent to the operation of these devices.

ANSI T1.102-1989	Digital Hierarchy – Electrical Interfaces 1989
TR-TSY-000191	Alarm Indication Signal Requirements and Objectives, Issue 1, May 1986
TR-TSY-000499	Transport Systems Generic Requirements, Issue 3, December 1989
TR-NWT-000253	SONET Transport Systems: Common Generic Criteria, Issue 6, September 1990
CCITT Rec G.703	Physical/Electrical Characteristics of Hierarchical Digital Interfaces, 1985

Contacts

ASL hotline	(214) 997-5202
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SONET / ATM data sheets:	
Chris Taylor	(214) 997-5211
SONET / ATM technical:	
Rick Curtis	(903) 868-5628
Kurt Himmelreich†	(903) 868-5665
Anders Oldeback	(903) 868-7971
Carlos Valdivia	(903) 868-5716

† Primary TNETS2020A/TNETS2021A contacts

Contents

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

TNET Ordering Instructions

The networking capability of Texas Instruments ATM, SONET/SDH, and Ethernet™ devices has made it necessary to change the device prefix from TDC to TNET in the standard four-part type number used for factory orders. The following examples illustrate the use of the new prefix used in this data book. Factory orders for the devices should include a four-part type number.

The historical TMS380 and TI380 products are not affected including the C16/C24/C26/C27/C30/C60/SRA/FPA and TMS38054 products. All other products adhere to the following four-part type number.

Examples are:

TNETA1500PCM replaces TDC1500PCM
TNETS2302CFN replaces TDC2302CFN
TNETA1555DW replaces TDC1555DW
TNETE100 replaces TI380C100

EXAMPLE: TNETA 1500 PCM R

Prefix

MUST CONTAIN TWO TO FIVE LETTERS

TNET = TI Networking devices

- TNETA = ATM/SONET/SDH devices
- TNETE = ThunderLAN devices and derivatives
- TNETS = SONET/SDH devices
- XTNET = Prototype devices

Unique Circuit Description

MUST CONTAIN FOUR TO ELEVEN CHARACTERS

Examples: 1500
2020A

Package

MUST CONTAIN ONE TO THREE LETTERS

- DW = plastic small-outline package
- FN = plastic J-leaded chip carrier
- PGC, PCM = plastic quad flat package

(from pin-connection diagram on individual data sheet)

Tape and Reel Packaging

Valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

MUST CONTAIN ONE OR TWO LETTERS

- LE = Left embossed tape and reel (required for DB and PW packages)
- R = Standard tape and reel (optional for DW package)

TNET Wafer-Lot Trace Code

The standard-lot trace-code formats are shown below for different wafer packages.

20/24/28 DW AND DL PACKAGES

Symbolization

All QFP/PLCC/MQUAD/BGA PACKAGES

Symbolization

where:

ymlllls = standard-lot trace-code format. Use yymm format if lot trace code is not available (INDY, ASIC assembly, etc.)

fffffff = 7- digit wafer fabrication lot number

r = alphabetic die revision

ww = 2-digit wafer number (implies that each wafer is built on a separate SWR) or use XX when the wafer number does not apply

t = material type:
- N – nominal material
- L – Low material
- H – high material
- X – don't care

– x = prototype designation (only for prototype)

Some examples:

TNETA1630: TNETA1630DW
ymlllls
4294883X21H (lot #4294883, no-revision die, wafer 21, high material)

SABRE: TNETA1500PCM
ymlllls
4342996H03L (lot #4342996, H-revision die, wafer 03, low material)

Factory orders for circuits other than TNET described in this data book should include a four-part type number as explained in the following example.

EXAMPLES: SN 74ACT7808 FN
SN 74ABT7819 PH R

Prefix

MUST CONTAIN TWO TO THREE LETTERS

SN = Standard prefix
SNJ =
MIL-STD-883 processed and
screened per JEDEC Standard 101

Unique Circuit Description

MUST CONTAIN EIGHT TO ELEVEN CHARACTERS

Examples: 74GTL16612
74FB1650
74ABT7819
74ABTE16245

Package

MUST CONTAIN ONE TO THREE LETTERS

DW	=	plastic small-outline package
DL	=	plastic shrink small-outline package
DGG	=	plastic thin shrink small-outline package
FN	=	plastic J-leaded chip carrier
HQA	=	ceramic quad flat package
PH	=	JEDEC metric plastic quad flat package
PQ	=	JEDEC plastic quad flat package
PM, PN, PAG PAH, PCA, PCB, PGE, PGF	=	plastic thin quad flat package
PCM, PGC, RC	=	plastic quad flat package
WD	=	ceramic flat package

(from pin-connection diagram on individual data sheet)

Tape and Reel Packaging

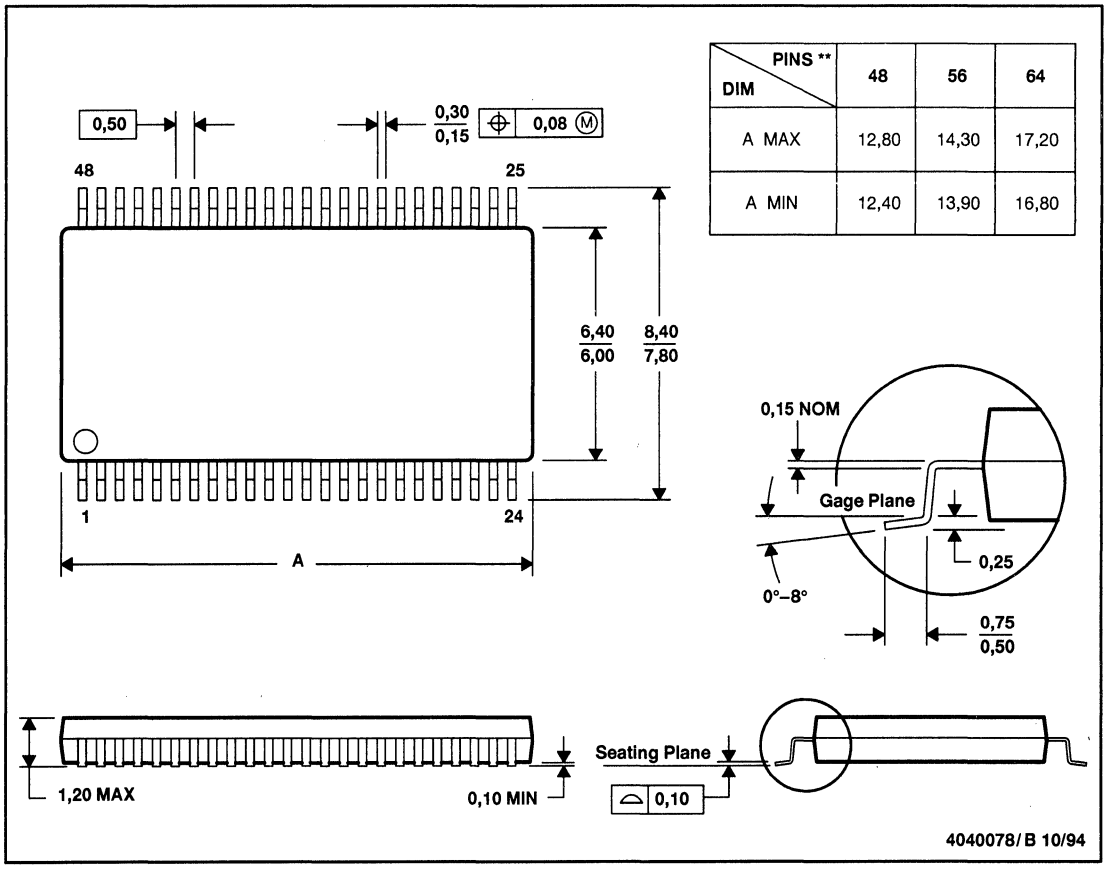
Valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

MUST CONTAIN ONE OR TWO LETTERS

LE = Left embossed tape and reel (required for DB and PW packages)
R = Standard tape and reel (optional for DW package)

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PIN SHOWN

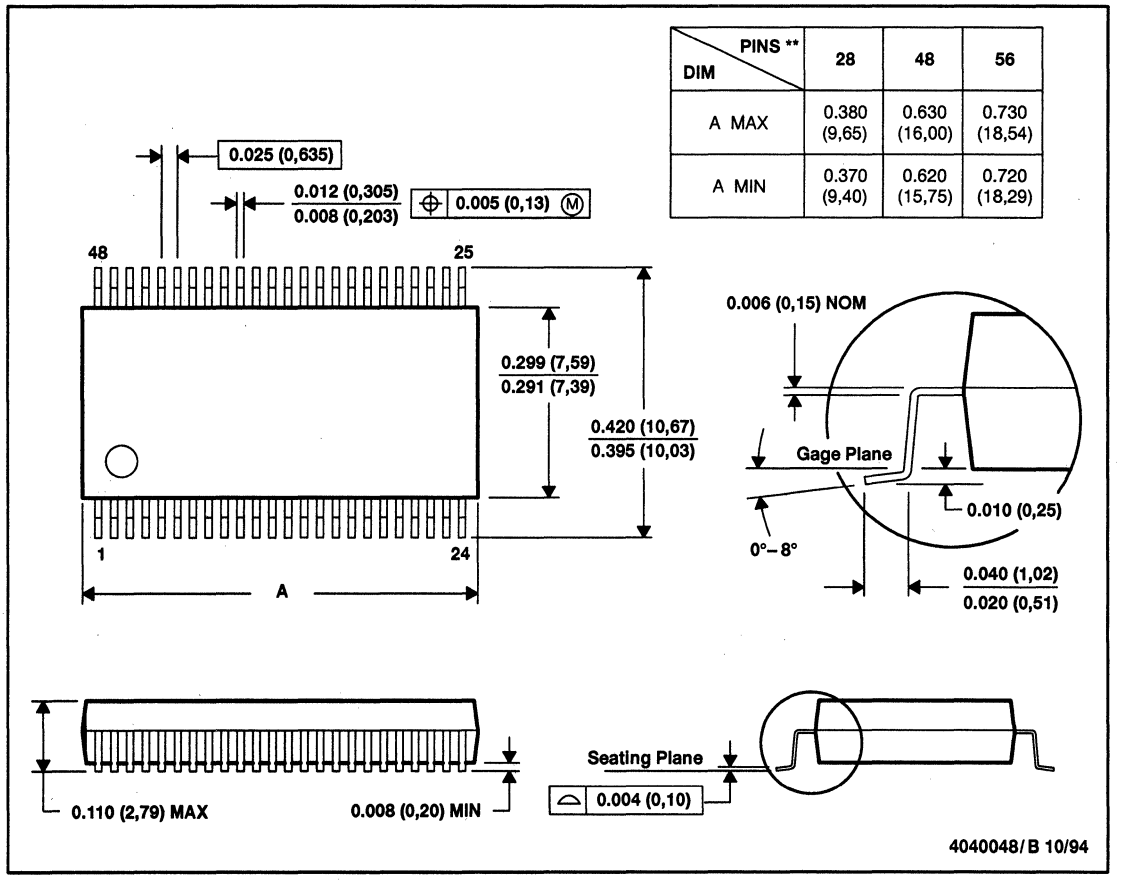


DIM \ PINS **	48	56	64
A MAX	12,80	14,30	17,20
A MIN	12,40	13,90	16,80

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PIN SHOWN

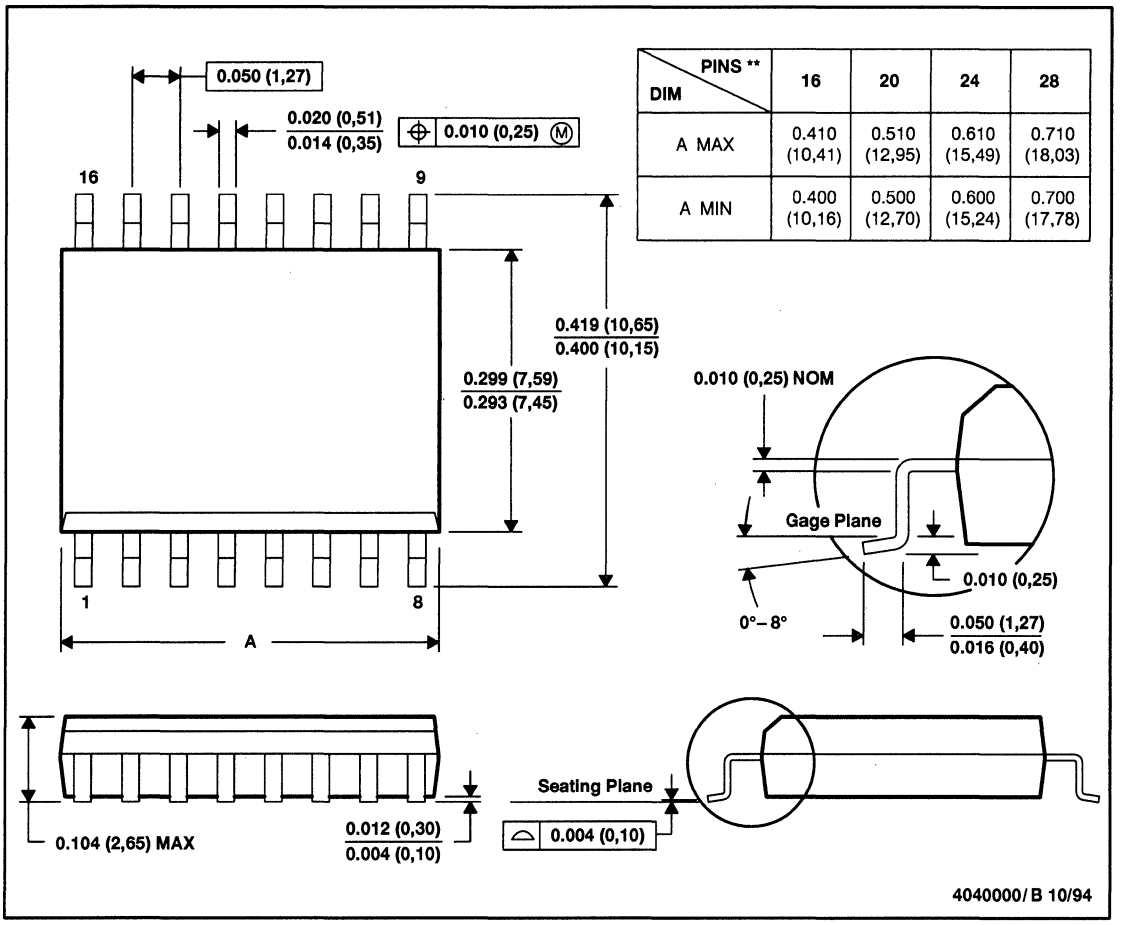


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PIN SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

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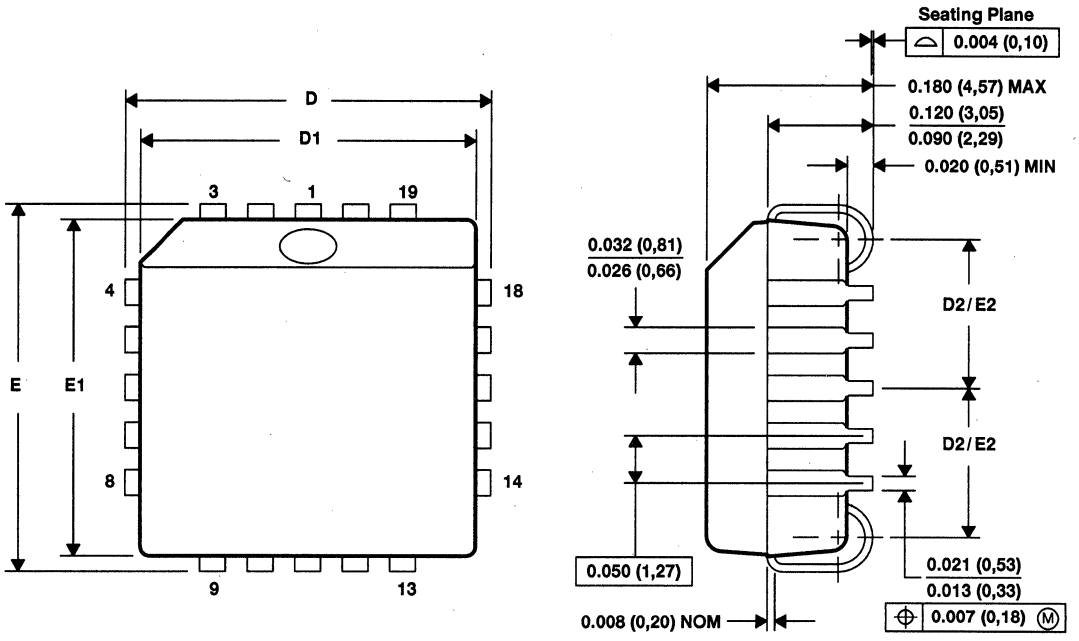
FN (S-PQCC-J)** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN



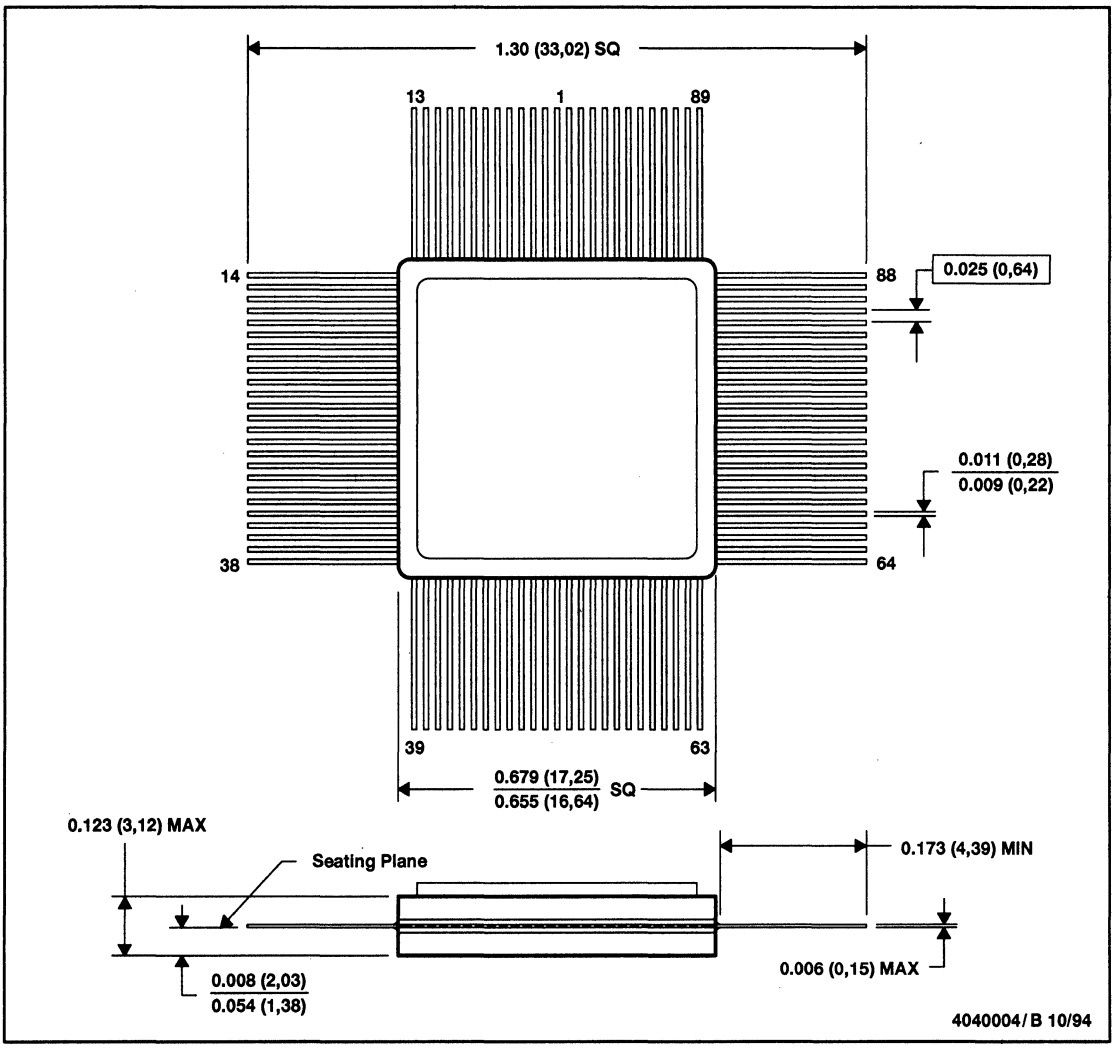
NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

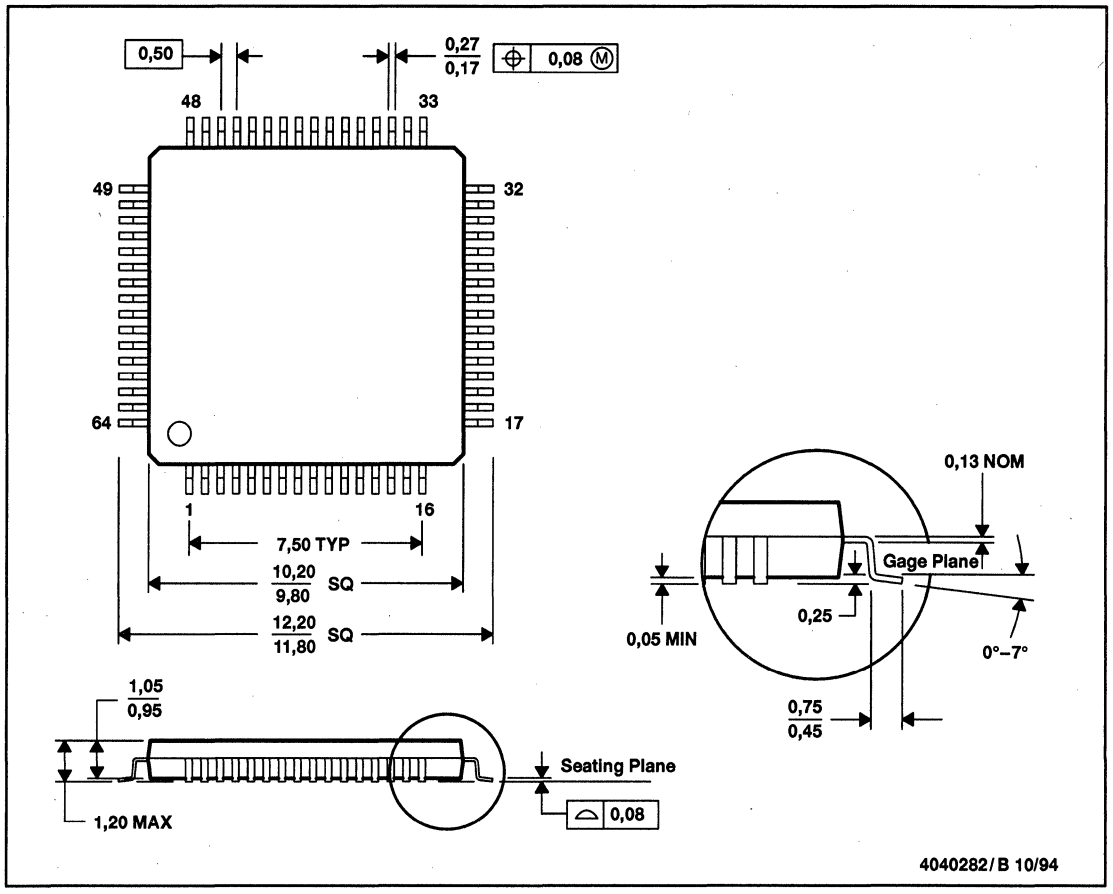
OCTOBER 1994

HQA (S-GQFP-F100) **CERAMIC QUAD FLATPACK**



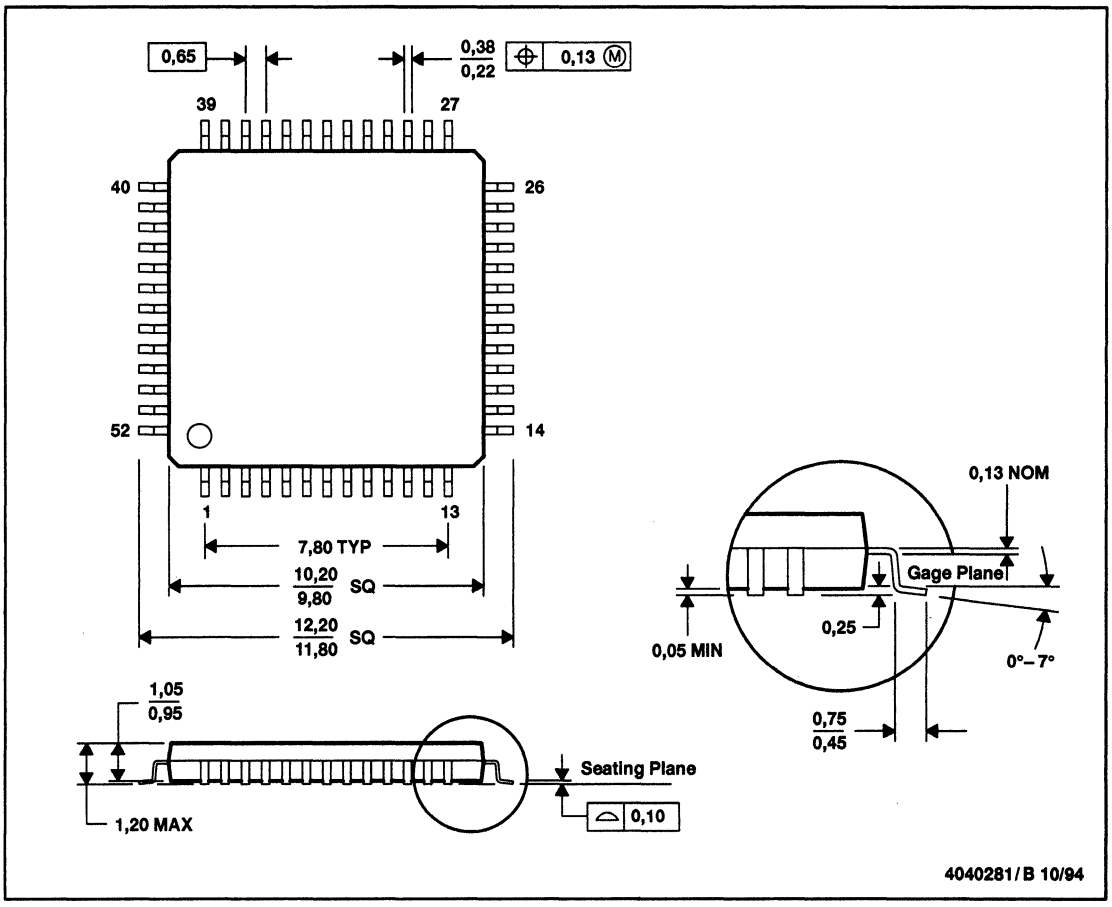
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The 0.05-inch lead spacing configured with straight leads for surface-mounting capability.

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

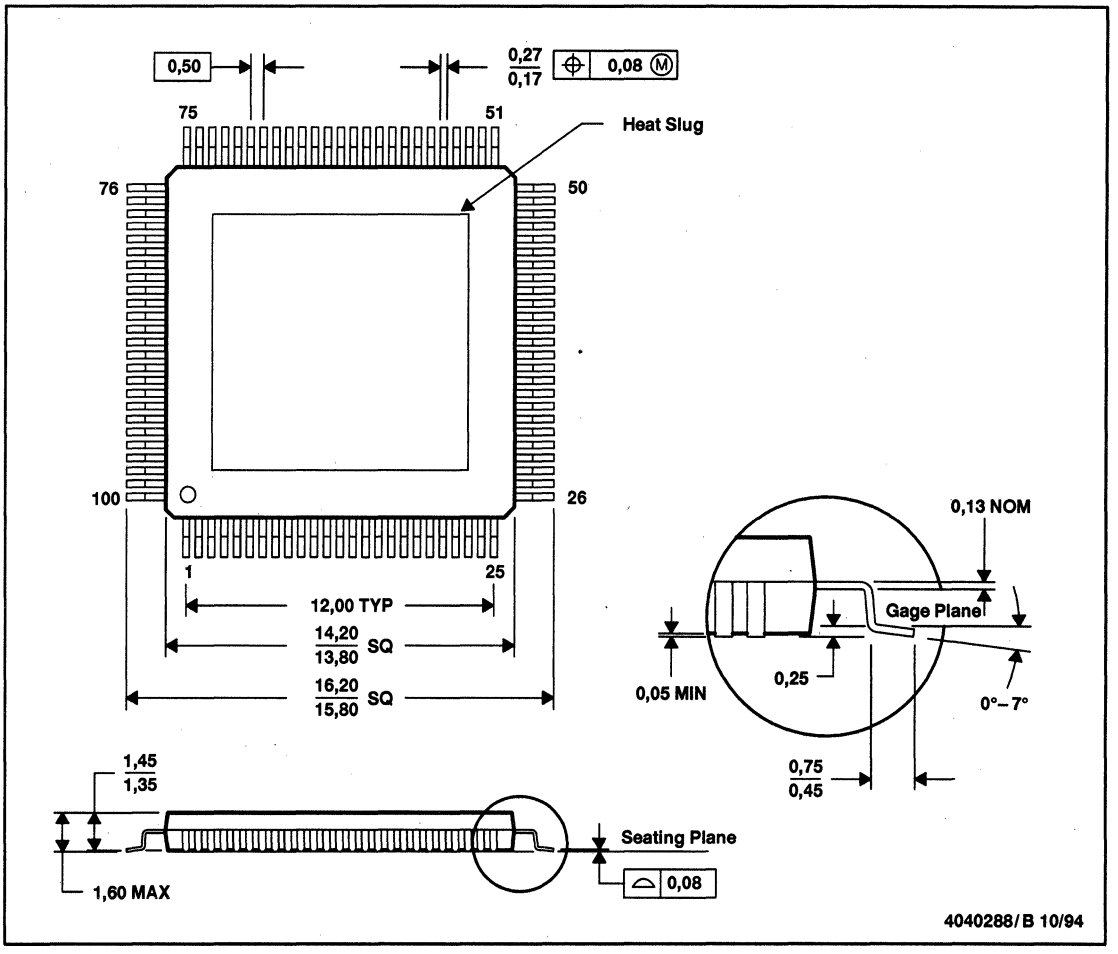
PAH (S-PQFP-G52) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

OCTOBER 1994

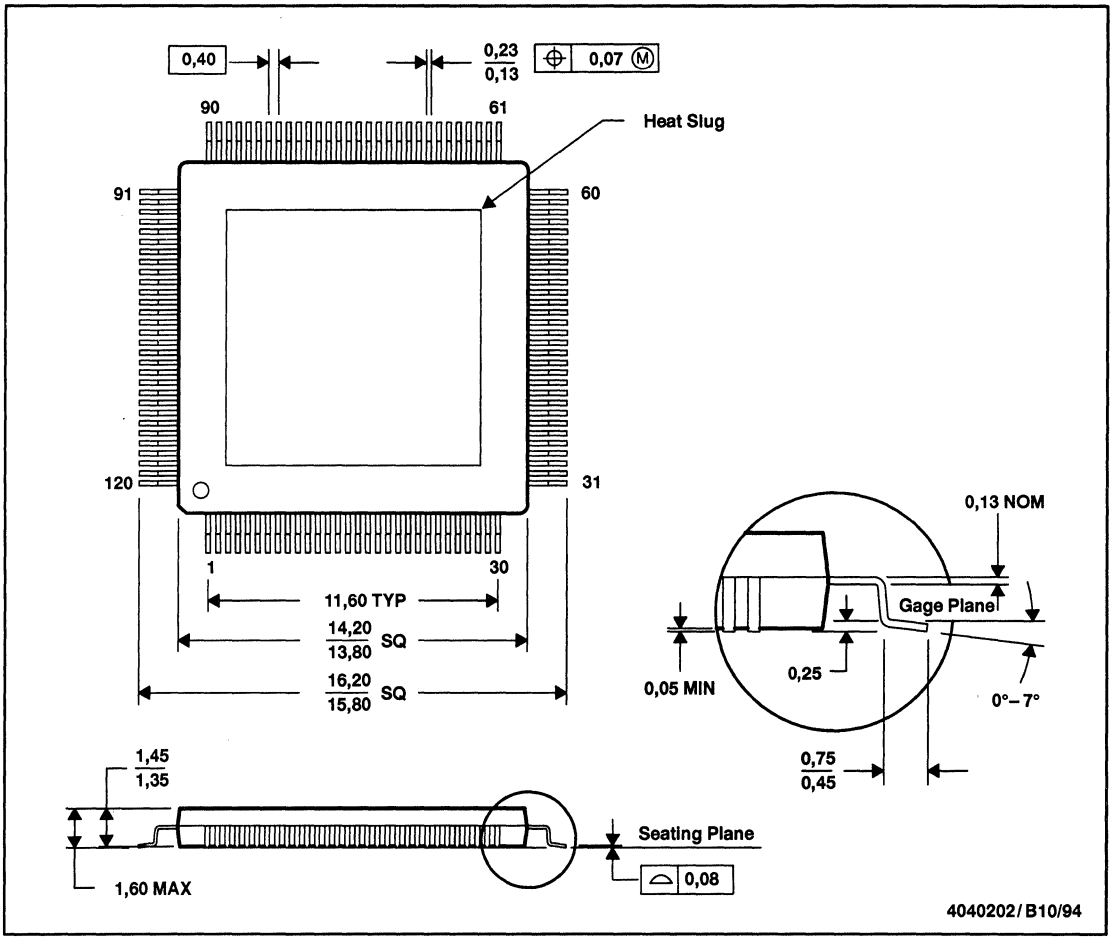
PCA (S-PQFP-G100) **PLASTIC QUAD FLATPACK (DIE-DOWN)**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Thermally enhanced molded plastic package with a heat slug (HSL)
D. Falls within JEDEC MO-136

OCTOBER 1994

PCB (S-PQFP-G120) **PLASTIC QUAD FLATPACK**



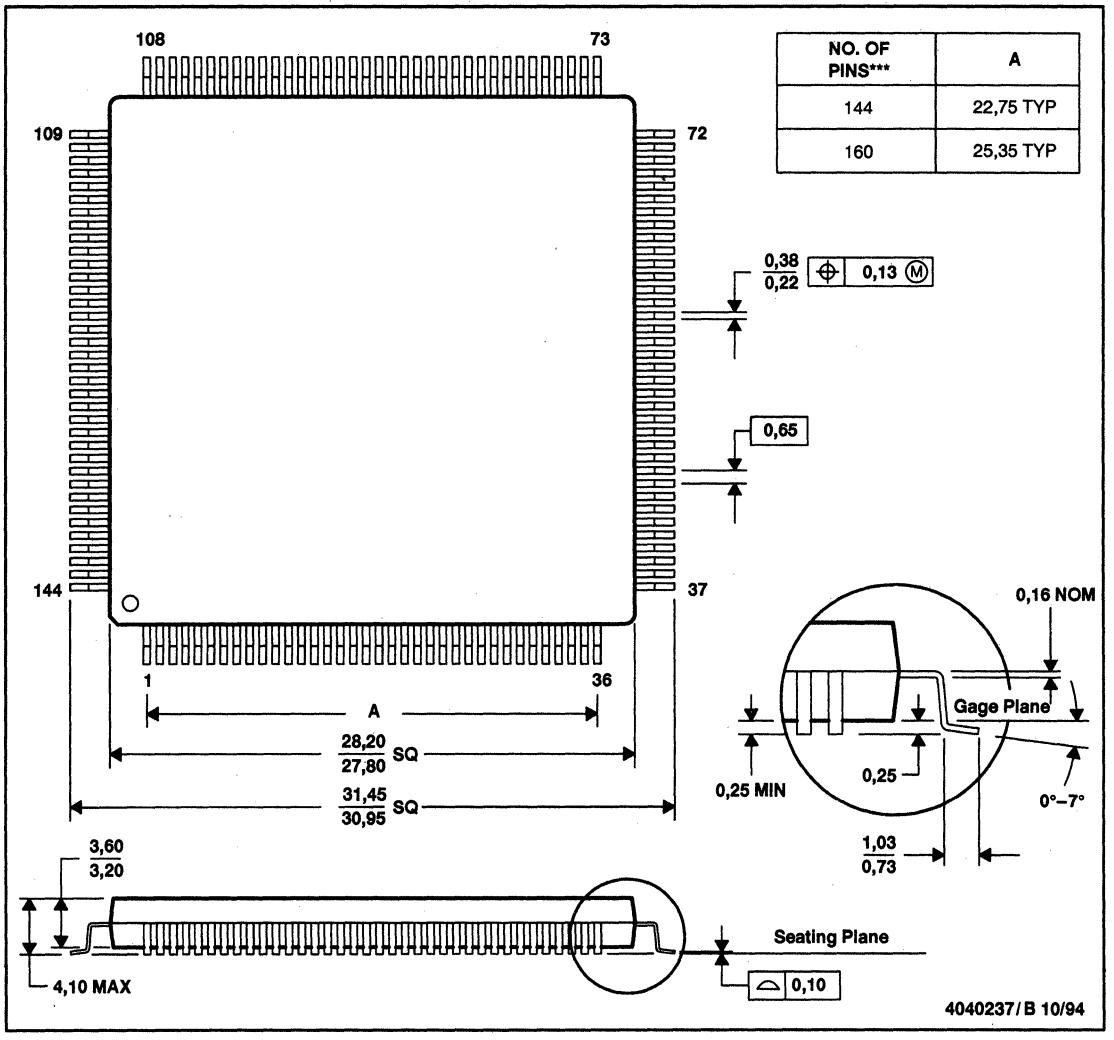
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136
D. Thermally enhanced molded plastic package with a heat slug (HSL)

OCTOBER 1994

PCE (S-PQFP-G***)

PLASTIC QUAD FLATPACK

144 PIN SHOWN

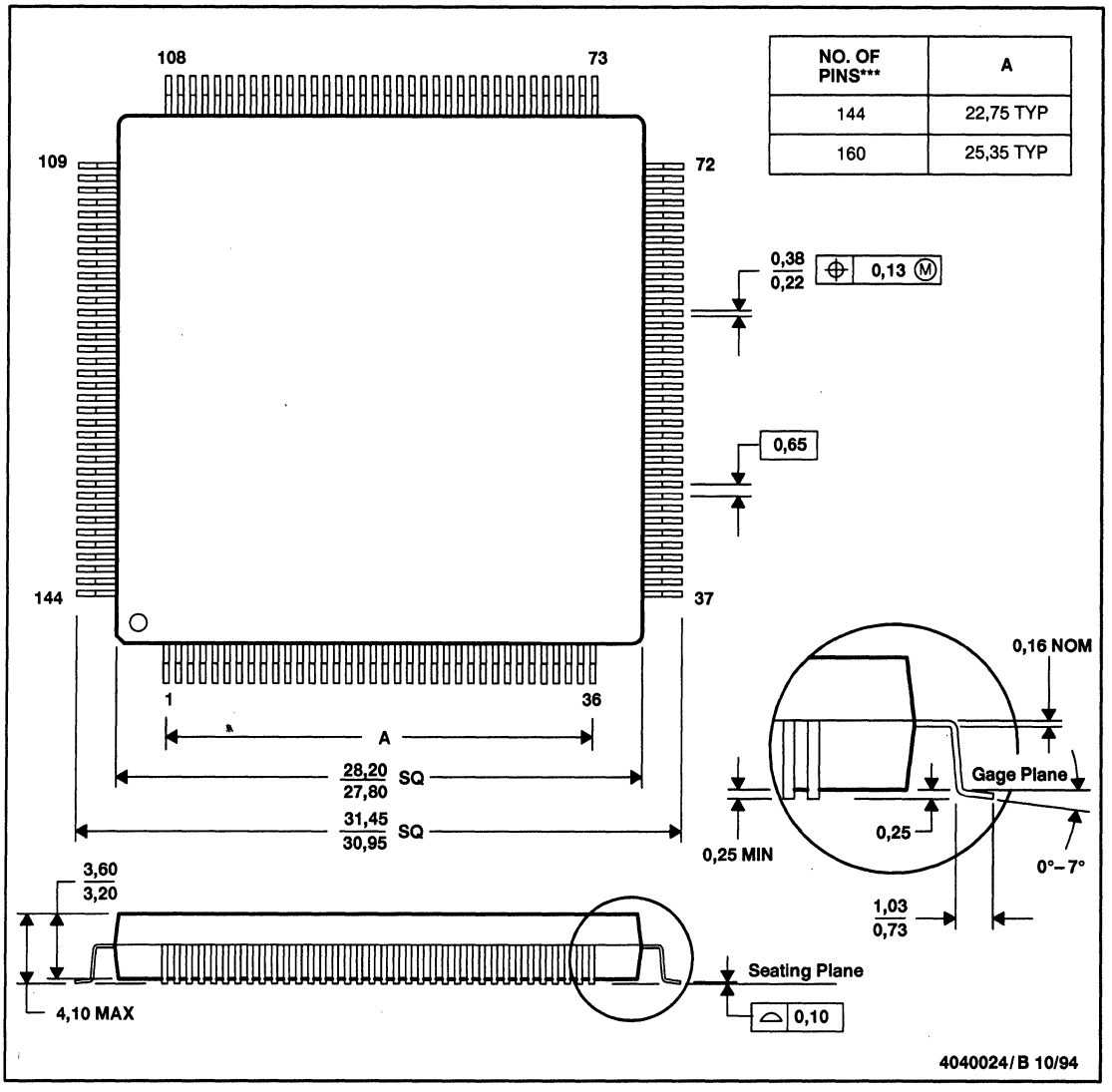


NO. OF PINS***	A
144	22,75 TYP
160	25,35 TYP

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Thermally enhanced molded plastic package with a heat spreader (HSP)
D. Falls within JEDEC MS-022
E. The 144 PCE is identical to the 160 PCE except that four leads per corner are removed.

PCM (S-PQFP-G*)** **PLASTIC QUAD FLATPACK**

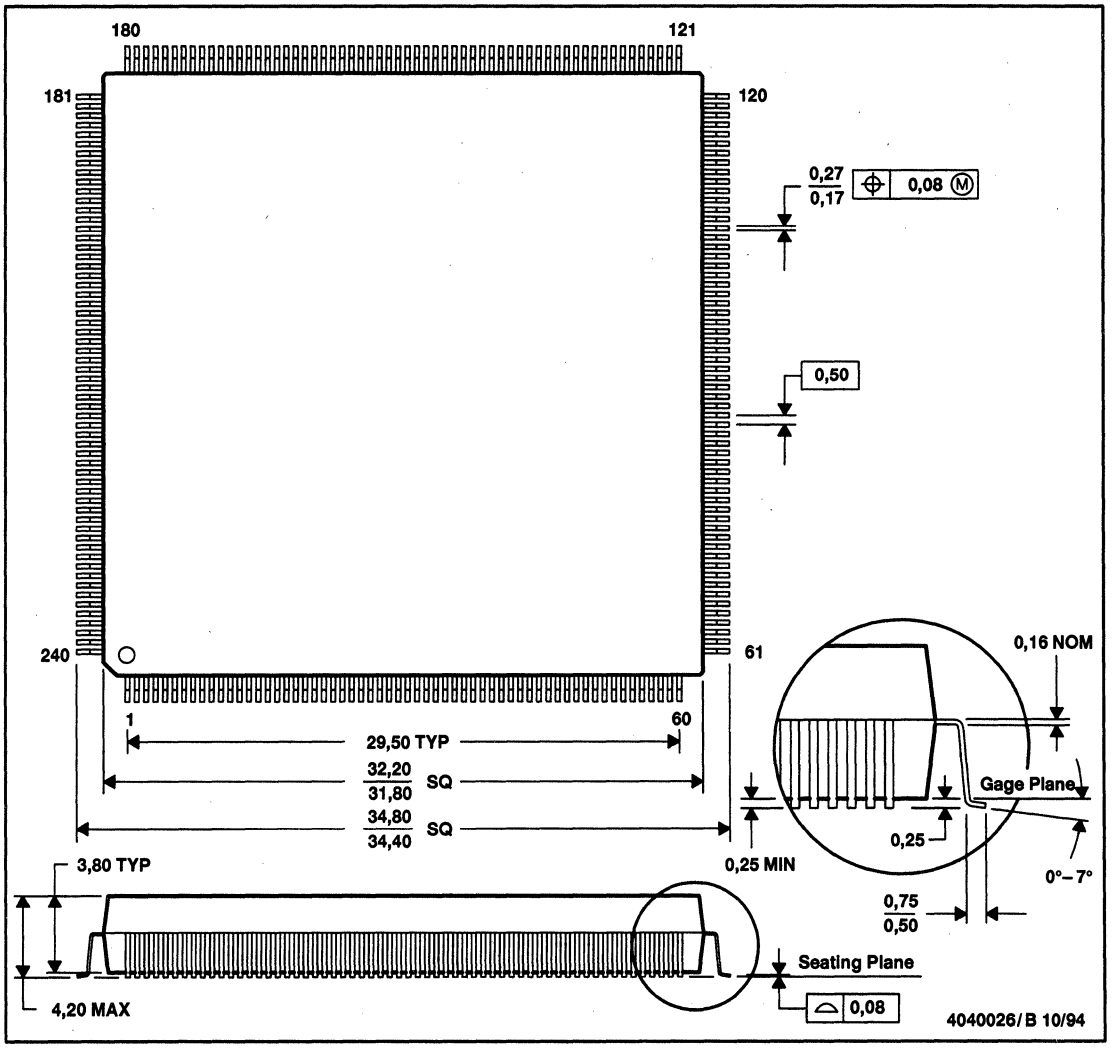
144 PIN SHOWN



NO. OF PINS***	A
144	22,75 TYP
160	25,35 TYP

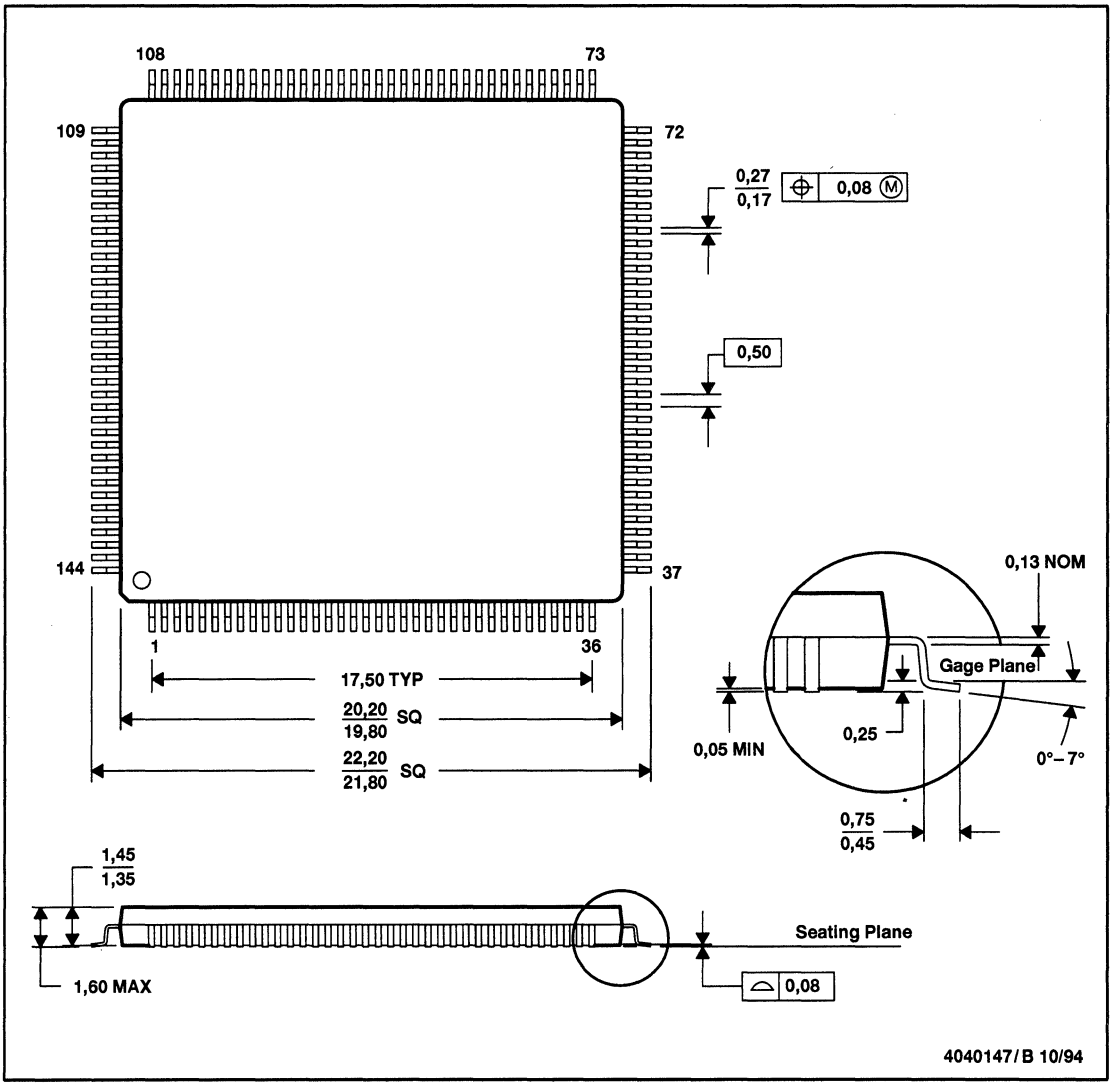
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-022
D. The 144 PCM is identical to the 160 PCM except that four leads per corner are removed.

PGC (S-PQFP-G240) **PLASTIC QUAD FLATPACK**



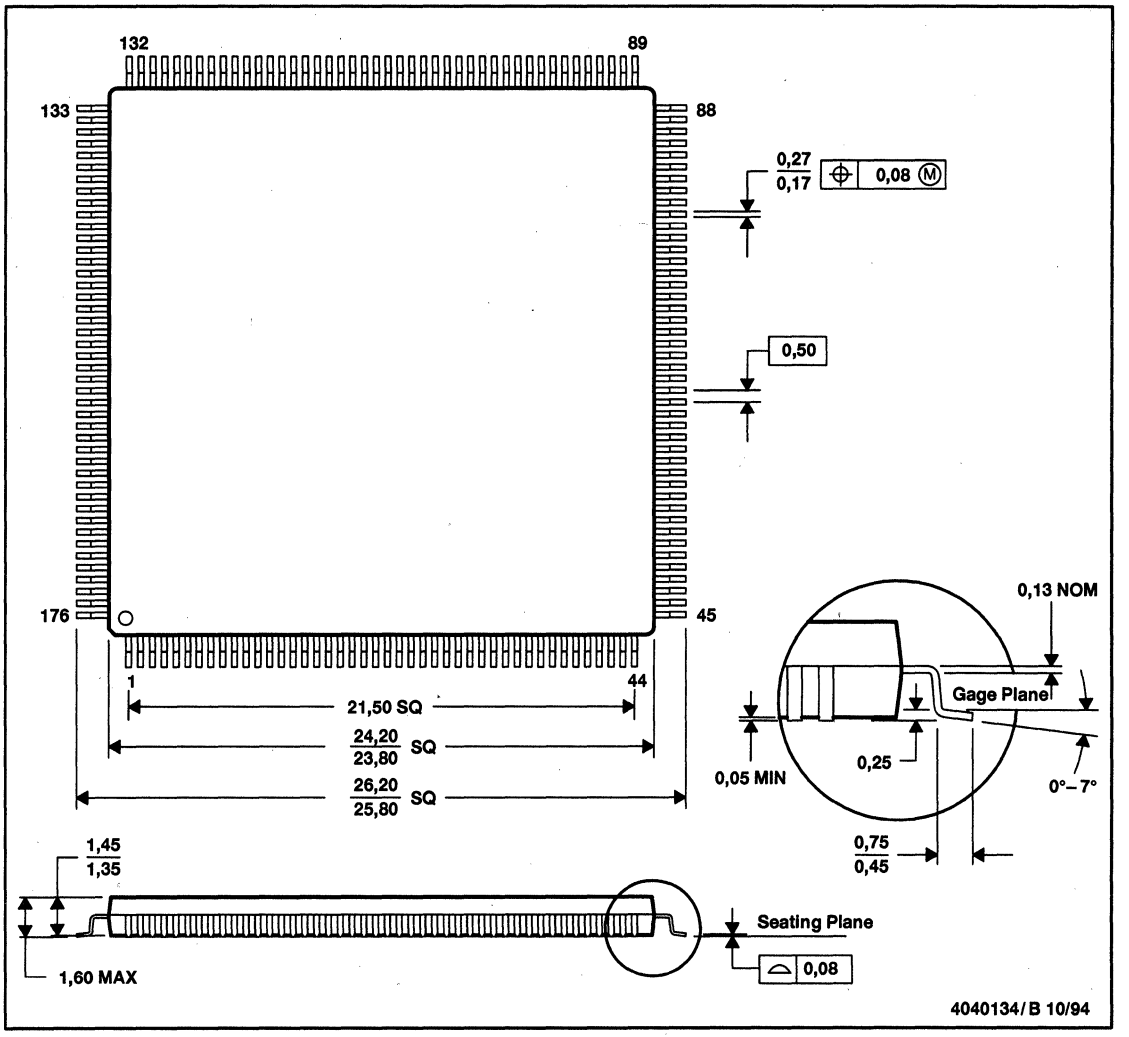
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

PGE (S-PQFP-G144) **PLASTIC QUAD FLATPACK**



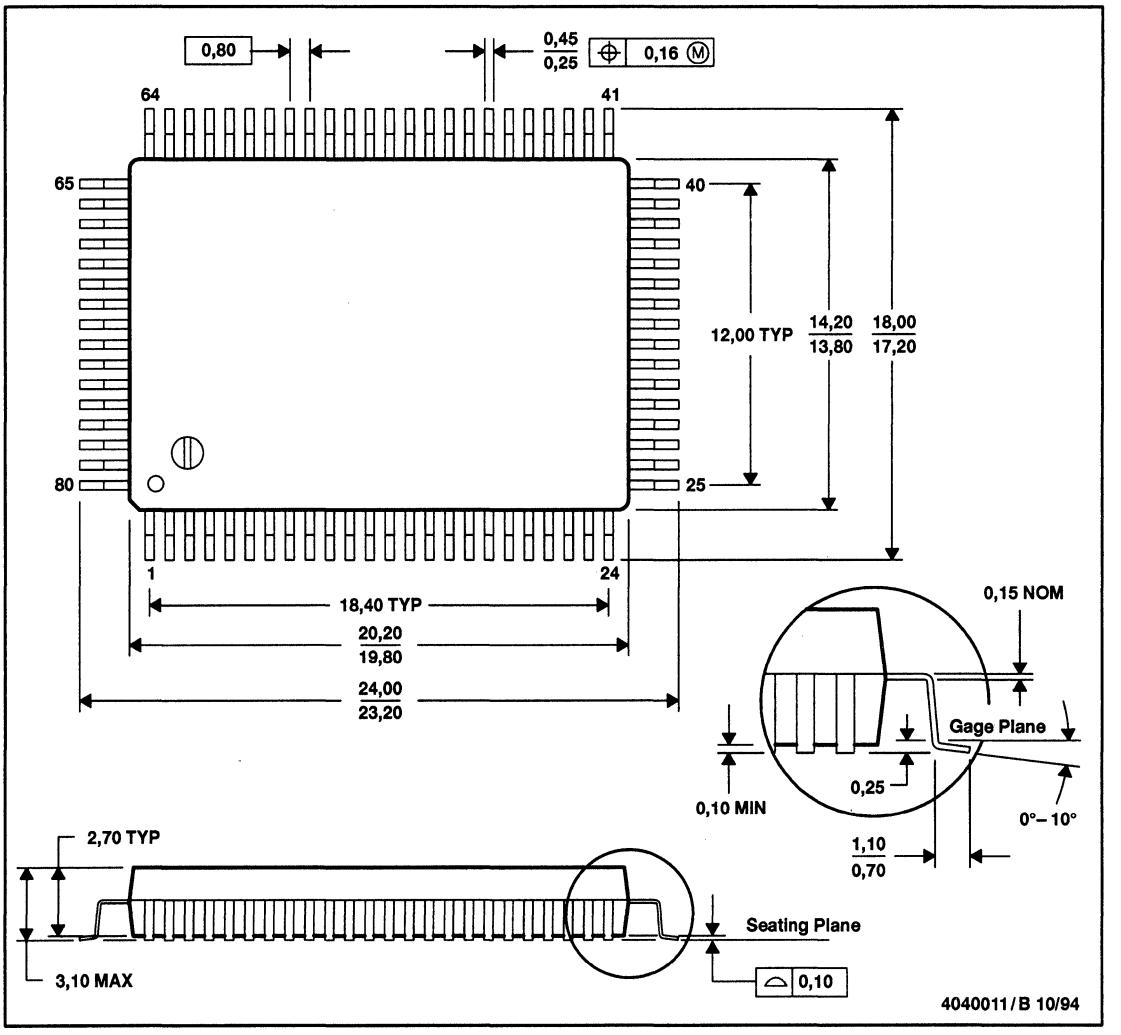
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

PGF (S-PQFP-G176) **PLASTIC QUAD FLATPACK**



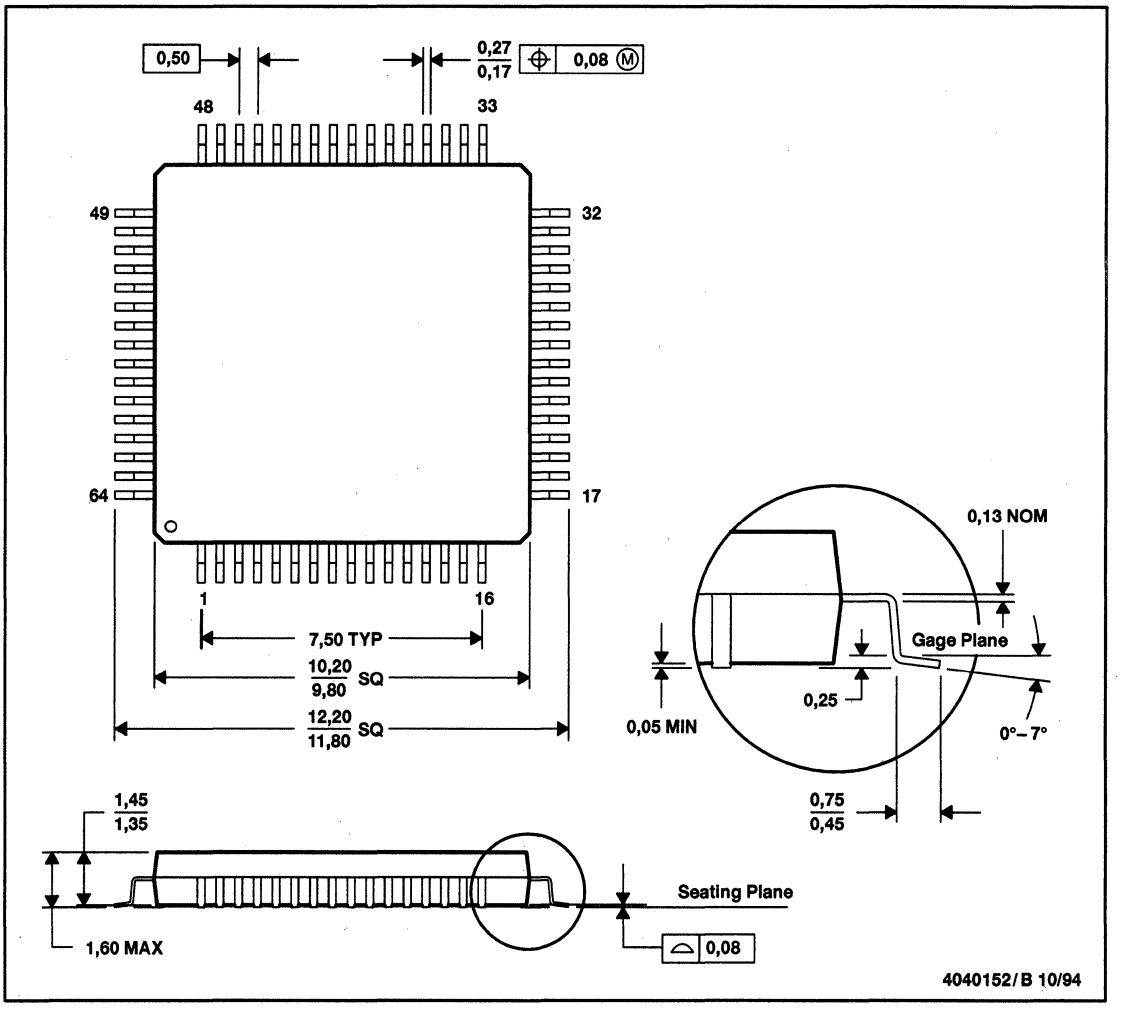
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

PH (R-PQFP-G80) **PLASTIC QUAD FLATPACK**



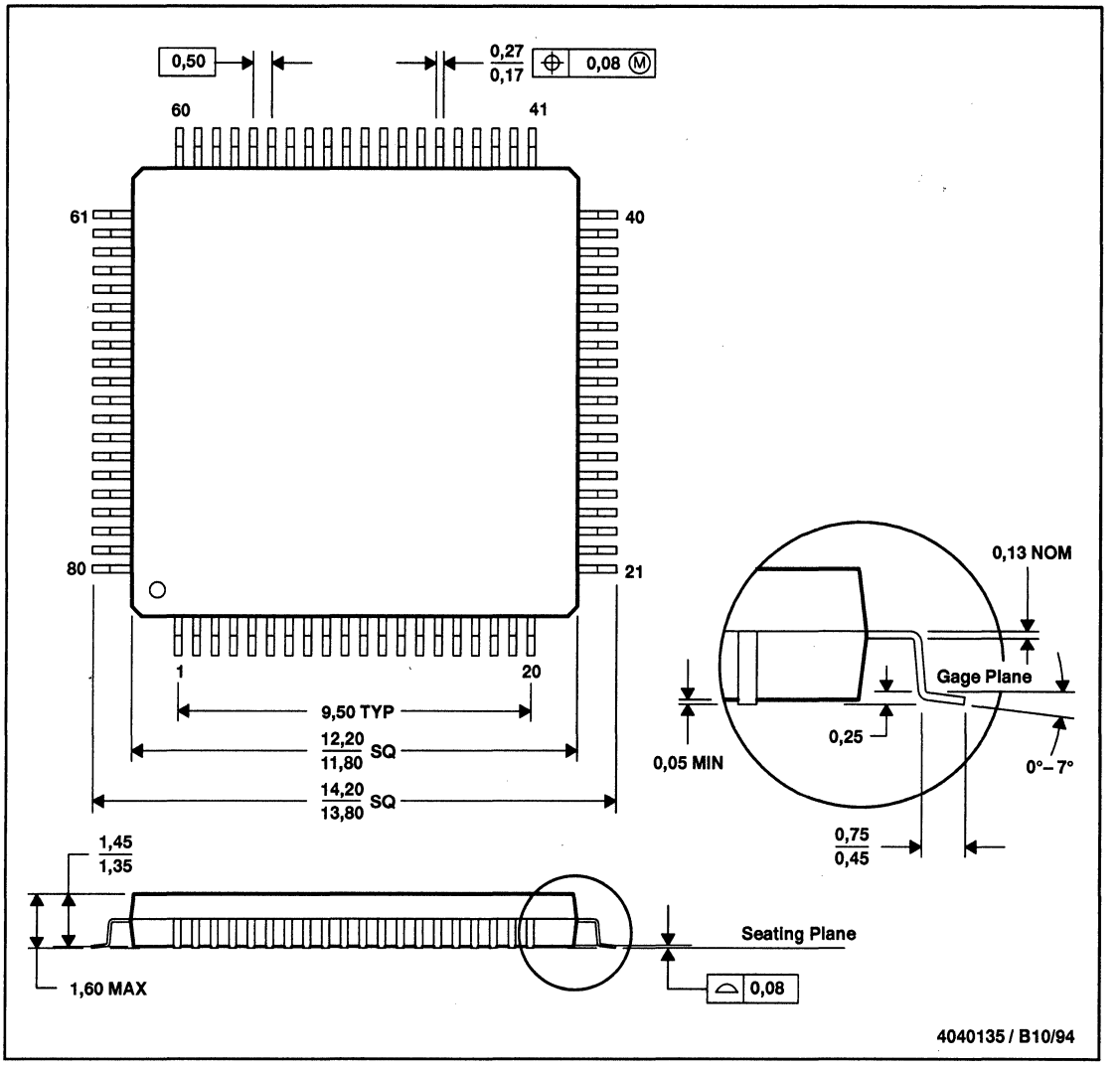
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

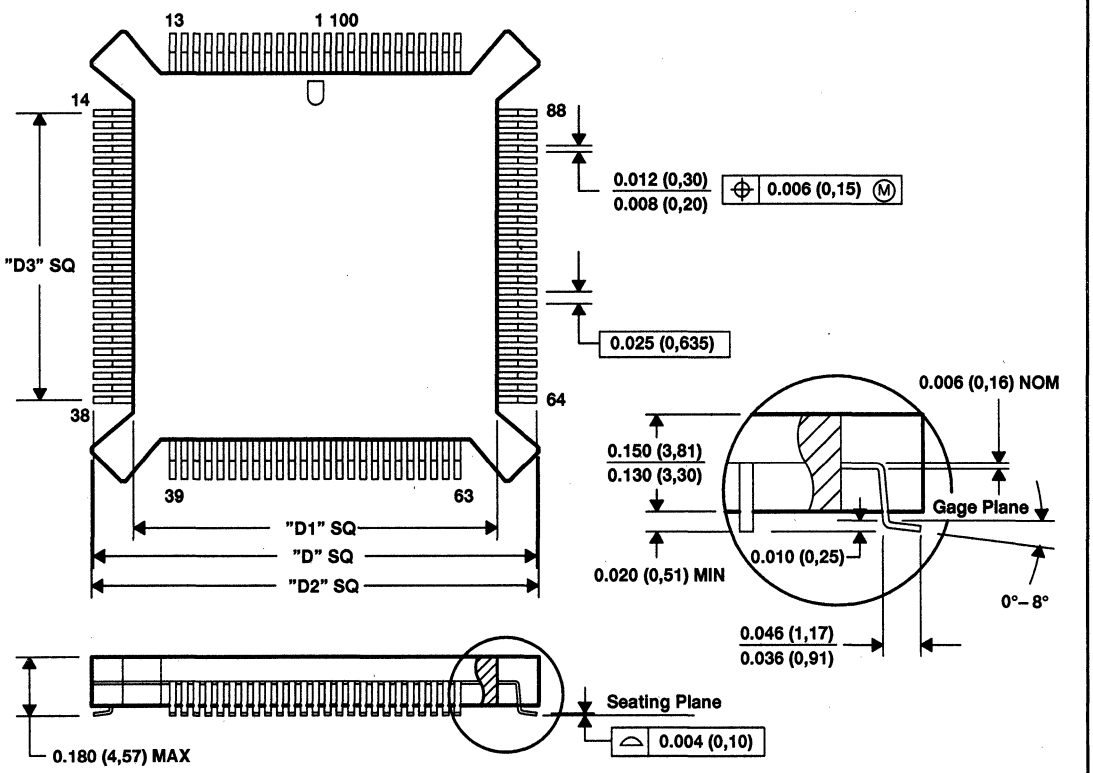
PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

PQ (S-PQFP-G*)** **PLASTIC QUAD FLATPACK**

100 LEAD SHOWN

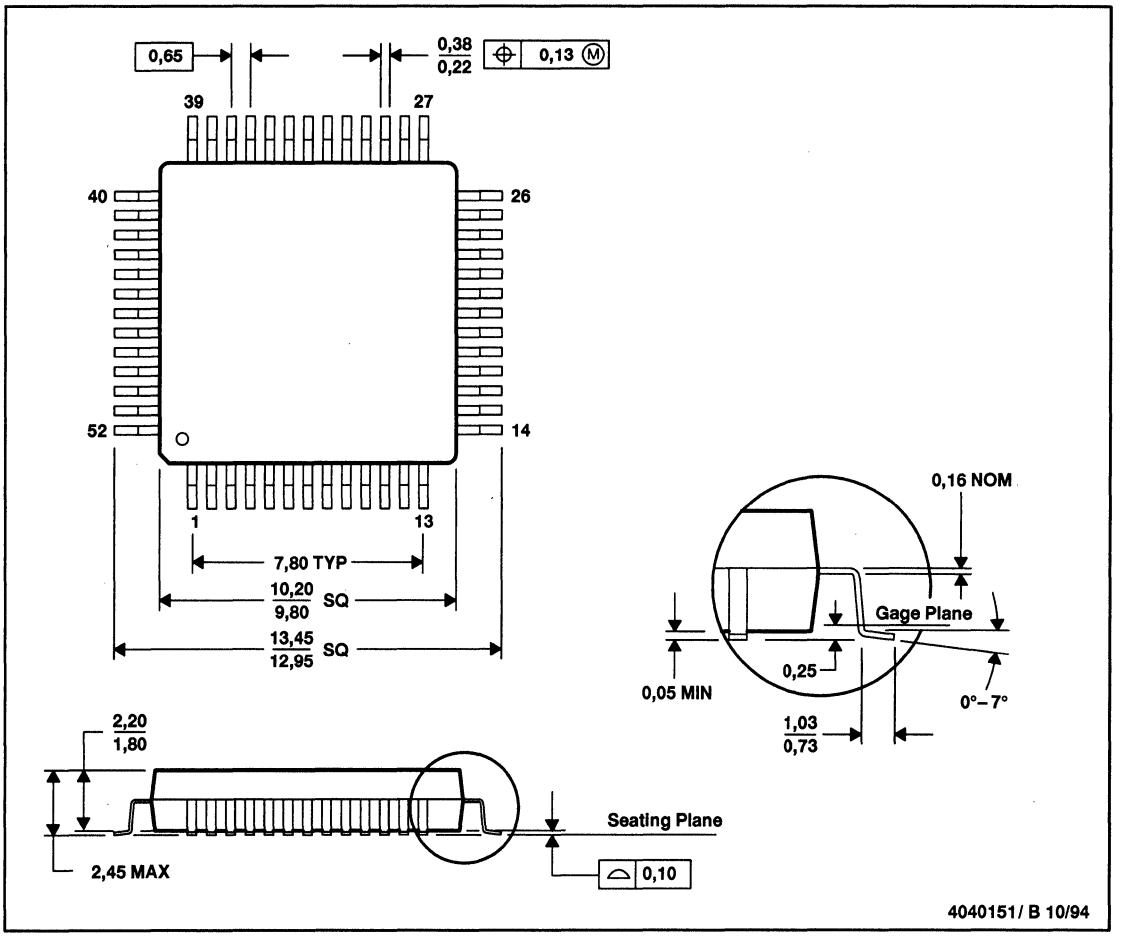


DIM \ LEADS ***		100 PQ	132 PQ
"D"	MAX	0.890 (22,61)	1.090 (27,69)
	MIN	0.870 (22,10)	1.070 (27,18)
"D1"	MAX	0.766 (19,46)	0.966 (24,54)
	MIN	0.734 (18,64)	0.934 (23,72)
"D2"	MAX	0.912 (23,16)	1.112 (28,25)
	MIN	0.888 (22,56)	1.088 (27,64)
"D3"	NOM	0.600 (15,24)	0.800 (20,32)

4040045/B 10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-069

RC (S-PQFP-G52) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-022

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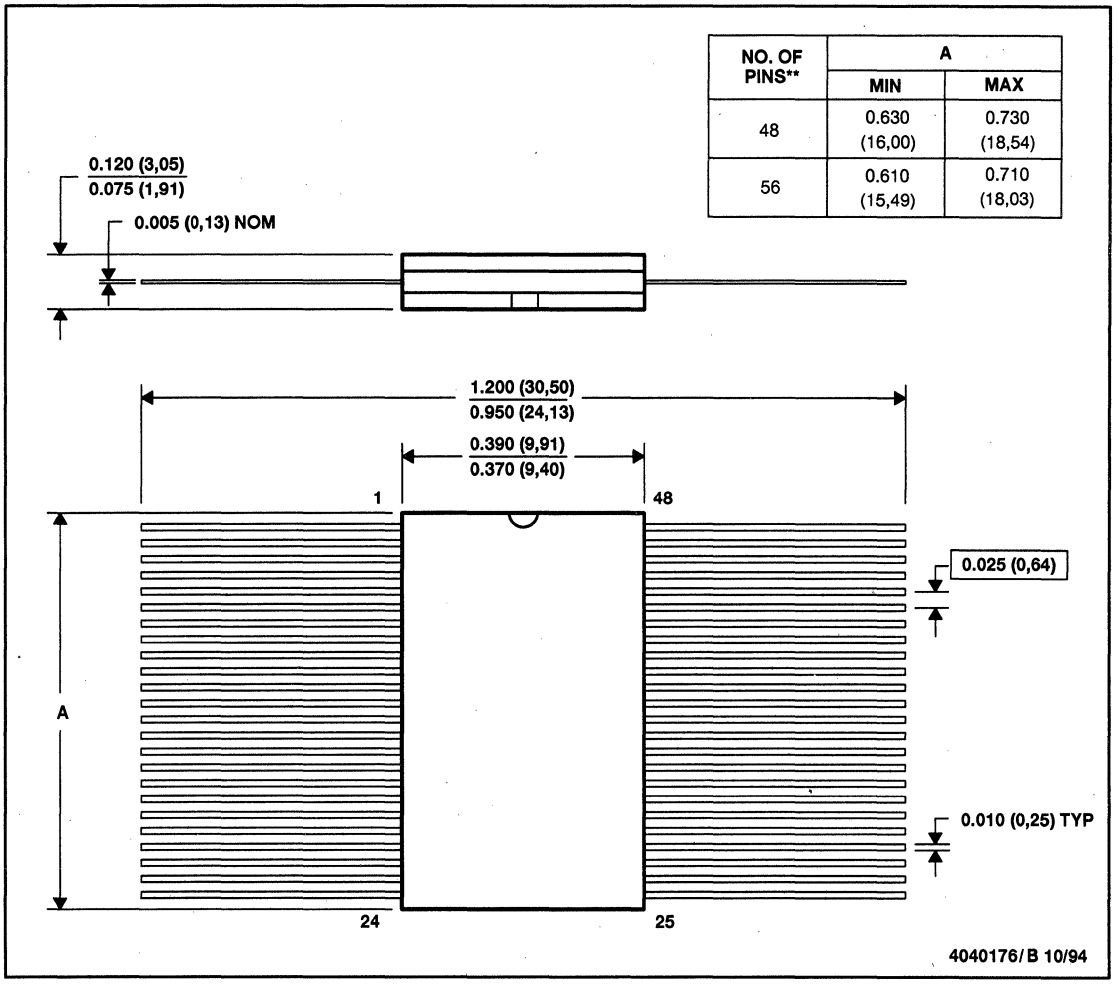
WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

48 PIN SHOWN



NO. OF PINS**	A	
	MIN	MAX
48	0.630 (16,00)	0.730 (18,54)
56	0.610 (15,49)	0.710 (18,03)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for pin identification only.
E. Falls within MIL-STD-1835: GDFP1-F48 and JEDEC MO-146AA
GDFP1-F56 and JEDEC MO-146AB

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