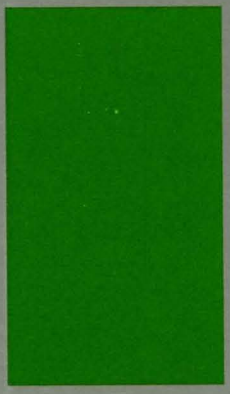
TOSHIBA AMERICA, INC.

MICROPROCESSORS

VOL. 1–8 BIT MPUs & MCUs



MICROPROCESSORS

VOL. 1—8 BIT MPUs & MCUs

January 1987

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TLCS-85 Family LSI

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Application Specific Standard Products

TLCS-Z80 Family

TMPZ84C00AP, TMPZ84C00AP-6, TMPZ84C00AP-8, TMPZ84C00AF, TMPZ84C00AF-6
TLCS-Z80 CPU: 8-BIT MICROPROCESSOR

1. GENERAL DESCRIPTION AND FEATURES

THE TMPZ84C00A (from here on referred to as Z80 or CPU) is CMOS version of Z80 CPU which provides low power operation and high performance.
Built into the CMOS Z80 microprocessor are all bus control, memory control, and timing signals in addition to eight general purpose 16-bit registers and an arithmetic-and-logic unit. The CMOS Z80 is fabricated using Toshiba's CMOS Silicon Gate Technology.

1.1 FEATURES

- Software Compatible with the Zilog Z80 CPU
- DC to 4MHz Operation (TMPZ84C00AP/AF)
- DC to 6MHz Operation (TMPZ84C00AP-6/AF-6)
- DC to 8MHz Operation (TMPZ84C00AP-8)
- Single 5V Power Supply : 5V $\pm$ 10%
- Powerful Set of 158 Instructions
- Duplicate Sets of Both General-purpose and Flag Registers
- Two Interrupt Inputs
  - Non-maskable Interrupt ($\overline{NMI}$)
  - 3 Modes of Maskable Interrupt ($\overline{INT}$)
    - 8080 Compatible (Non-Z80 Peripheral Device) (Mode 0)
    - Restart (Mode 1)
    - Z80 Family Peripheral with Daisy Chain (Model 2)
- Low Power Consumption
  9mA Typ. @4MHz@5V (TMPZ84C00AP/AF)
  15mA Typ. @6MHz@5V (TMPZ84C00AP-6/AF-6)
  20mA Typ. @8MHz@5V (TMPZ84C00AP-8)
  Less than 10uA @5V (Stand-by)
- Extended Operating Temperature
  -40°C to 85°C
- Two Indexed Registers
- IO Addressing Modes
- On-chip Dynamic Memory Refresh Counter
- 40 pin DIP package, 44 pin Mini Flat package.

Z80 is a trademark of Zilog Inc.

2. PIN CONNECTIONS AND PIN FUNCTIONS

2.1 PIN CONNECTIONS (TOP VIEW)

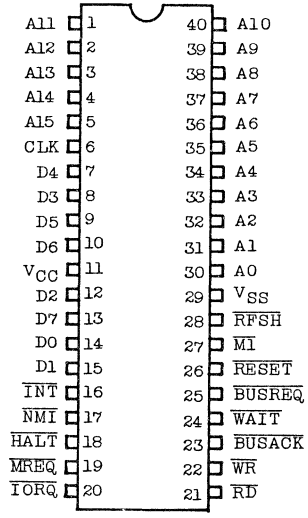
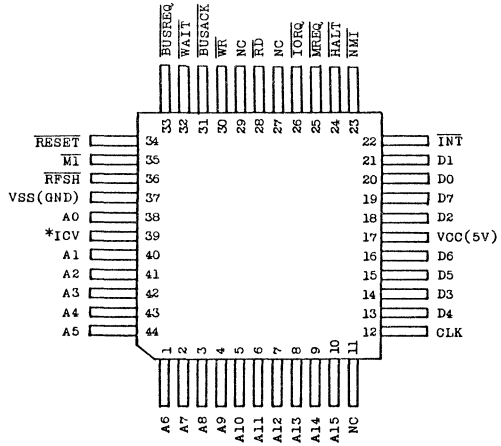


Fig. 2.1 DIP Pin Connections



(Note) Connect Pin 39 and Pin 17 externally.
* ICV must be used at open condition or connected with VCC.

Fig. 2.2 MFP Pin Connections

2.2 PIN NAMES AND PIN DESCRIPTION

(1) A0-A15. Address Bus (output, active High, 3-state)
A0-A15 form a 16-bit address bus. The Address Bus provides the address for memory data bus exchanges (up to 64K bytes) and for I/O device exchanges.

(2) $\overline{\text{BUSACK}}$. Bus Acknowledge (output, active Low)
Bus Acknowledge indicates to the requesting device that the CPU address bus, data bus, and control signals MREQ, IORQ, RD, and WR have entered their high impedance states. The external circuitry can now control these lines.

(3) $\overline{\text{BUSREQ}}$. Bus Request (input, active Low)
Bus Request has a higher priority than NMI and is always recognized at the end of the current machine cycle. BUSREQ forces the CPU address bus, data, and control signals MREQ, IORQ, RD, and WR to go to a high-impedance state so that other devices can control these lines. BUSREQ is normally wire-ORed and requires an external pullup for these applications. Extended BUSREQ periods due to extensive DMA operations can prevent the CPU from properly refreshing dynamic RAMs.

(4) D0-D7. Data Bus (input/output, active High, 3-state)
D0-D7 constitute an 8-bit bidirectional data bus, used for data exchange with memory and I/O.

(5) $\overline{\text{HALT}}$. Halt State (output, active Low)
HALT indicates that the CPU has executed a Hal instruction and is awaiting either a non-maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOPs to maintain memory refresh.

(6) $\overline{\text{INT}}$. Interrupt Request (input, active Low)
Interrupt Request is generated by I/O devices. The CPU honors a request at the end of the current instruction if the internal software-controlled interrupt enable flip-flop (IFF) is enabled. INT is normally wire-ORed and requires an external pull-up for these applications.

(7) $\overline{\text{IORQ}}$. Input/Output Request (output, active Low, 3-state)
IORQ indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. IORQ is also generated concurrently with M1 during an interrupt acknowledge cycle to indicate that an interrupt response vector can be placed on the data bus.

(8) $\overline{\text{M1}}$. Machine Cycle One (output, active Low)
M1, together with MREQ, indicates that the current machine cycle is the opcode fetch cycle of an instruction execution. Note that during execution of 2-byte op-codes always begin with CBH, DDH, EDH or FDH. M1 also occurs with IORQ to indicate an interrupt acknowledge cycle.

(9) $\overline{\text{MREQ}}$. Memory Request (output, active Low, 3-state)
MREQ indicates that the address bus holds a valid address for a memory read or memory write operation.

(10) $\overline{\text{NMI}}$. Non-Maskable Interrupt (input, active Low)
NMI has higher priority than INT. NMI is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop, and automatically forces the CPU to restart at location 0066H.

(11) $\overline{\text{RD}}$. Memory Read (output, active Low, 3-state)
RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

(12) $\overline{\text{RESET}}$. Reset (input, active Low)
RESET initializes the CPU as follows: it resets the interrupt enable flip-flop, clears the PC and Registers I and R, and sets the interrupt status to Mode 0. During reset time, the address and data bus go to a high-impedance state, and all control output signals go to the inactive state. Note that RESET must be active for a minimum of three full clock cycles before the reset operation is complete.

(13) $\overline{\text{RFSH}}$. Refresh (output, active Low)
RFSH together with MREQ, indicates that the lower seven bits of the system's address bus can be used as a refresh address to the system's dynamic memories.

(14) $\overline{\text{WAIT}}$. Wait (input, active Low)
WAIT indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter a Wait state as long as this signal is active. Extended WAIT periods can prevent the CPU from refreshing dynamic memory properly.

(15) $\overline{\text{WR}}$. Memory Write (output, active Low, 3-state)
WR indicates that the CPU data bus holds valid data to be stored at the addressed memory or I/O location.

(16) CLK. clock (input)
Single phase system clock input. When CLK is a DC state (either a high or low level), CPU stops its operation and maintains resisters and control signals.

(17) VCC. Power Supply
+5V

(18) VSS. Power Supply
Ground refernece (0V).

3. FUNCTIONAL DESCRIPTION

3.1 BLOCK DIAGRAM

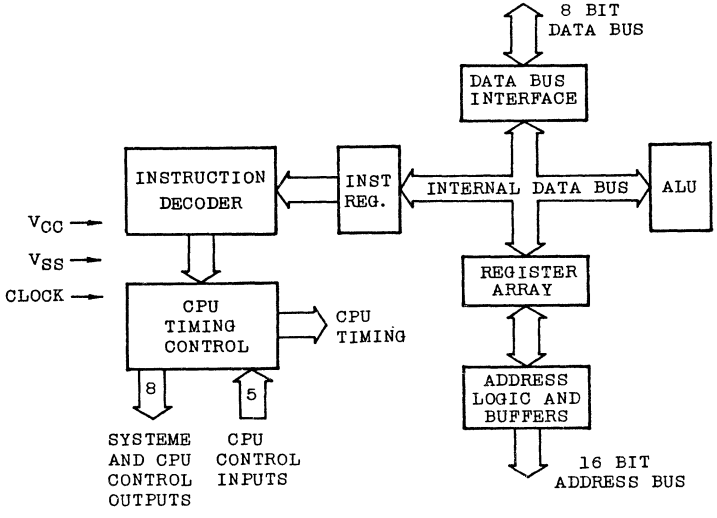


Fig. 3.1 BLOCK DIAGRAM

3.2 CPU REGISTERS

The internal registers contain 208 bits of read/write memory that are accessible to the programmer. These registers include two sets of six general-purpose registers which may be used individually as either 8-bit registers or as 16-bit register pairs. In addition, there arfe two sets of accumulator and flag registers. A group of "Exchange" instructions makes either set of main or alternate registers accessbile to the programmer. The alternate set allows operation in foregound-background mode or it may be reserved for very fast interrupt response.

The Z80 also contains a Stack Pointer, Program Counter, two index registers, a Refresh register (counter), and an Interrupt register.

Figure 3 shows the registers within the Z80 CPU.

Table 1 provides further information on these resisters.

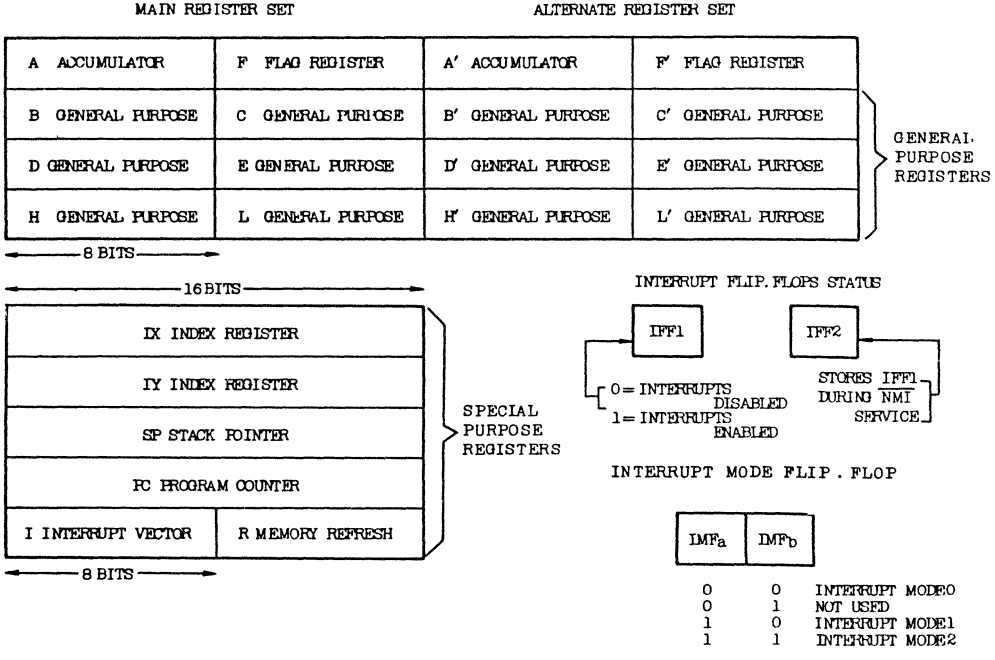


FIGURE 3. CPU REGISTERS

Register		Size (Bits)	Remarks
A, A'	Accumulator	8	Stores an operand or the results of an operation.
F, F'	Flags	8	See Instruction Set.
B, B'	General Purpose	8	Can be used separately or as a 16-bit register with C.
C, C'	General Purpose	8	See B, above.
D, D'	General Purpose	8	Can be used separately or as a 16-bit register with E.
E, E'	General Purpose	8	See D, above.
H, H'	General Purpose	8	Can be used separately or as a 16-bit register with L.
L, L'	General Purpose	8	See H, above. Note: The (B,C), (D,E), and (H,L) sets are combined as follows: B - High byte C - Low byte D - High byte E - Low byte H - High byte L - Low byte
I	Interrupt Register	8	Stores upper eight bits of memory address for vectored interrupt processing.
R	Refresh Register	8	Provides user transparent dynamic memory refresh. Automatically incremented and placed on the address bus during each instruction fetch cycle.
IX	Index Register	16	Used for indexed addressing.
IY	Index Register	16	Same as IX, above.
SP	Stack Pointer	16	Stores addresses or data temporarily. See Push or Pop in instruction set.
PC	Program Counter	16	Holds address of next instruction.
IFF_1-IFF_2	Interrupt Enable	Flip-Flops	Set or reset to indicate interrupt status (see Figure 3).
IMFa-IMFb	Interrupt Mode	Flip-Flops	Reflect Interrupt mode (see Figure 3).

TABLE 1. Z80 CPU REGISTERS

(1) Special Purpose Registers

• Program Counter (PC)

The program counter is 16-bit counter and holds the 16-bit address of the current instruction being fetched from memory. The PC is automatically incremented after its contents have been transferred to the address lines. When a program jump occurs the new valve is automatically placed in the PC, overriding the incrementer.

• Stack Pointer (SP)

The stack pointer holds the 16-bit address of the current top of a stack located anywhere in external system RAM memory. The external stack memory is organized as a last-in first-out (LIFO) file. Data can be pushed onto the stack from specific CPU registers or popped off of the stack into specific CPU registers through the execution of PUSH and POP instructions. The data popped from the stack is always the last data pushed onto it. The stack allows simple implementation of multiple level interrupts, unlimited subroutine nesting and simplification of many types of data manipulation.

• Two Index Registers (IX & IY)

The two independent index registers hold a 16-bit base address that is used in indexed addressing modes. In this mode, an index register is used as a base to point to a region in memory from which data is to be stored or retrieved. An additional byte is included in indexed instructions to specify a displacement from this base. This displacement is specified as a two's

complement signed integer. This mode of addressing greatly simplifies many types of programs, especially where tables of data are used.

- Interrupt Page Address Register (I)

The Z80CPU can be operated in a mode where an indirect call to any memory location can be achieved in response to an interrupt. The I Register is used for this purpose to store the high order 8-bits of the indirect address while the interrupting device provides the lower 8-bits of the address. This feature allows interrup routines to be dynamically located anywhere in memory with absolute minimal access time to the routine.

- Memory Refresh Register (R)

The Z80CPU contains a memory refresh counter to enable dynamic memories to be used with the same ease as static memories. Seven bits of this 8-bit register are automatically incremented after each instruction fetch. The eighth bit will remain as programmed as the result of an LD R, A instruction. The data in the refresh counter is sent out on the lower portion of the address bus along with a refresh control signal while the CPU is decoding and executing the fetched instruction. This mode of refresh is totally transparent to the programmer and does not slow down the CPU operation. The programmer can load the R register for testing purposes, but this register is normally not used by the programmer. During refresh, the contents of the I register are placed on the upper 8 bits of the address bus.

(2) Accumulator and Flag Registers

The CPU includes two independent 8-bit accumulators and associated 8-bit flag registers. The accumulator holds the results of 8-bit arithmetic or logical operations while the flag register indicates specific conditions for 8 or 16-bit operations, such as indicating whether or not the result of an operation is equal to zero. The programmer selects the accumulator and flag pair that he wishes to work with a single exchange instruction so that he may easily work with either pair.

(3) General Purpose Registers

There are two matched sets of general purpose registers, each set containing six 8-bit registers that may be used individually as 8-bit registers or as 16-bit register pairs by the programmer. One set is called BC, DE and HL while the complementary set is called BC', DE' and HL'. At any one time the programmer can select either set of registers to work with through a single exchange command for the entire set. In systems where fast interrupt response is required, one set of general purpose registers and an accumulator-flag register may be reserved for handling this very fast routine. Only a simple exchange commands need be executed to go between the routines. This greatly reduces interrupt service time by eliminating the requirement for saving and retrieving register contents in the external stack during interrupt or subroutine processing. These general purpose registers are used for a wide range of applications by the programmer. They also simplify programming, especially in ROM based systems where little external read/write memory is available.

ARITHMETIC & LOGIC UNIT (ALU)

The 8-bit arithmetic and logical instructions of the CPU are executed in the ALU. Internally the ALU communicates with the registers and the external data bus on the internal data bus.

The type of functions performed by the ALU include:

Add	Left or right shifts or rotates (arithmetic and logical)
Subtract	Increment
Logical AND	Decrement
Logical OR	Set bit
Logical Exclusive OR	Reset bit
Compare	Test bit

INSTRUCTION REGISTER AND CPU CONTROL

As each instruction is fetched from memory, it is placed in the instruction register and decoded. The control section performs this function and then generates and supplies all of the control signals necessary to read or write data from or to the registers, controls the ALU and provides all required external control signals.

FLAGS

Each of the two Z80 CPU Flag registers contains six bits of information which are set or reset by various CPU instructions. Four of these bits are testable; that is, they are used as conditions for jump, call or return instructions. The four testable flag bits are:

1) Carry Flag (C) - This flag is the carry from the highest order bit of the accumulator. For example, the carry flag will be set during an add instruction where a carry from the highest bit of the accumulator is generated. This flag is also set if a borrow is generated during a subtraction instruction. The shift and rotate instructions also affect this bit.

2) Zero Flag (Z) - This flag is set if the result of the operation loaded a zero into the accumulator. Otherwise it is reset.

3) Sign Flag (S) - This flag is intended to be used with signed numbers and it is set if the result of the operation was negative. Since bit 7 (MSB) represents the sign of the number (A negative number has a 1 in bit 7), this flag stores the state of bit 7 in the accumulator.

4) Parity/Overflow Flag (P/V) - This dual purpose flag indicates the parity of the result in the accumulator when logical operations are performed (such as AND A, B) and it represents overflow when signed two's complement arithmetic operations are perfomed. The Z80 overflow

flag indicates that the two's complement number in the accumulator is in error since it has exceeded the maximum possible (+127) or is less than the minimum possible (-128) number that can be represented two's complement notation.

There are also two non-testable bits in the flag register. Both of these are used for BCD arithmetic.

1) Half carry (H) = This is the BCD carry or borrow result from the least significant four bits of operation. When using the DAA (Decimal Adjust Instruction) this flag is used to correct the result of a previous packed decimal add or subtract.

2) Add/Subtract Flag (N) - Since the agorithim for correcting BCD operations is different for addition or subtraction, this flag is used to specify what type of instruction was executed last so that the DAA operation will be correct for either addition or subtraction.

The Flag register can be accessed by the programmer and its format is as follows:

D7	D6	D5	D4	D3	D2	D1	D0
S	Z	X	H	X	P/V	N	C

X means flag is indeterminate.

The Table 2 lists how each flag is affected by various CPU instructions.

- '_' indicates that the instruction does not change the flag.
- 'X' means that the flag goes to an indeterminate state.
- 'R' means that it is reset.
- 'S' means that it is set.
- 'O' indicates that it is set or reset according to the previous discussion.

Note) Any instruction not appearing in the table 2 does not affect any of the flags.

Table 2 includes a few special cases that must be described for clarity. Notice that the block search instruction sets the Z flag if the last compare operation indicated a match between the source and the accumulator data. Also, the parity flag is set if the byte counter (register pair BC) is not equal to zero. This same use of the parity flag is made with the block move instructions. Another special case is during block input or output instructions, here the Z flag is used to indicate the state of register B which is used as a byte counter. Notice that when the I/O block transfer is complete, the zero flag will be reset to a zero (i.e. B=0) while in the case of a block move command the parity flag is reset when the operation is complete. A final case is when the refresh or I register is loaded into the accumulator, the interrupt enable flip flop is loaded into the parity flag so that the complete state of the CPU can be saved at any time.

Instruction	D7 S	D6 Z	D5	D4 H	D3	D2 P/V	D1 N	D0 C	Comments
ADD A,s;ADC A,s	o	o	x	o	x	V	R	o	8-bit add or add with carry
SUB s; SBC A,s; CP s; NEG	o	o	x	o	x	V	S	o	8-bit subtract, subtract with carry, compare and negate accumulator
AND s	o	o	x	S	x	P	R	R	Logical operations
OR s; XOR s	o	o	x	R	x	P	R	R	Logical operations
INC s	o	o	x	o	x	V	R	-	8-bit increment
DEC s	o	o	x	o	x	V	S	-	8-bit decrement
ADD DD, SS	-	-	x	x	x	-	R	o	16-bit add
ADC HL, SS	o	o	x	x	x	V	R	o	16-bit add with carry
SBC HL, SS	o	o	x	x	x	V	S	o	16-bit subtract with carry
RLA; RLCA; RRA; RRCA	-	-	x	R	x	-	R	o	Rotate accumulator
RL s; RLC s; RR s; RRC s; SLA s; SRA s; SRL s	o	o	x	R	x	P	R	o	Rotate and shift locations
RLD; RRD	o	o	x	R	x	P	R	-	Rotate digit left and right
DAA	o	o	x	o	x	P	-	o	Decimal adjust accumulator
CPL	-	-	x	S	x	-	S	-	Complement accumulator
SCF	-	-	x	R	x	-	R	S	Set carry
CCF	-	-	x	x	x	-	R	o	Complement carry
IN r, (C)	o	o	x	R	x	P	R	-	Input register indirect
INI; IND; OUTI; OUTD	x	o	x	x	x	x	S	x	Block input and output
INIR; INDR; OTIR; OTDR	x	S	x	x	x	x	S	x	Z=0 if B≠0 otherwise Z=1
LDI; LDD	x	x	x	R	x	o	R	-	Block transfer instructions
LDIR; LDDR	x	x	x	R	x	R	R	-	P/V=1 if BC≠0, otherwise P/V=0

Instruction	D7 S	D6 Z	D5	D4 H	D3	D2 P/V	D1 N	D0 C	Comments
CPI; CPIR; CPD; CPDR	o	o	x	o	x	o	S	-	Block search instructions Z=1 if A=(HL), otherwise Z=0 P/V=1 if BC≠0, otherwise P/V=0
LD A, I; LD A, R	o	o	x	R	x	IFF	R	-	The content of the interrupt enable flip-flop (IFF) is copied into the P/V flag.
BIT b, s	x	o	x	S	x	x	R	-	The state of bit b of location s is copied into the Z flag

TABLE 2. SUMMARY OF FLAG OPERATION

The following notation is used in this table:

SYMBOL	OPERATION
C	Carry/link flag. C=1 if the operation produced a carry from the MSB of the operand or result.
Z	Zero flag. Z=1 if the result of the operation is zero.
S	Sign flag. S=1 if the MSB of the result is one.
P/V	Parity or overflow flag. Parity (P) and overflow (V) share the same flag. Logical operations affect this flag with the parity of the result while arithmetic operations affect this flag with the overflow of the result. If P/V holds parity, P/V=1 if the result of the operation is even, P/V=0 if result is odd. If P/V holds overflow, P/V=1 if the result of the operation produced an overflow.
H	Half-carry flag. H=1 if the add or subtract operation produced a carry into or borrow from bit 4 of the accumulator.

SYMBOL	OPERATION
N	Add/Subtract flag. N=1 if the previous operation was a subtract. H and N flags are used in conjunction with the decimal adjust instruction (DAA) to properly correct the result into packed BCD format following addition or subtraction using operands with packed BCD format. The flag is affected according to the result of the operation.
-	The flag is unchanged by the operation.
R	The flag is reset by the operation.
S	The flag is set by the operation.
o	The flag is affected according to the result of the operation.
x	The flag is a "don't care".
V	P/V flag affected according to the overflow result of the operation.
P	P/V flag affected according to the parity result of the operation.
r	Any one of the CPU registers A, B, C, D, E, H, L.
s	Any 8-bit location for all the addressing modes allowed for the particular instruction.
ss	Any 16-bit location for all the addressing modes allowed for that instruction.
I	I resister
R	Refresh counter.
n	8-bit value in range <0, 255>
nn	16-bit value in range <0, 65535>

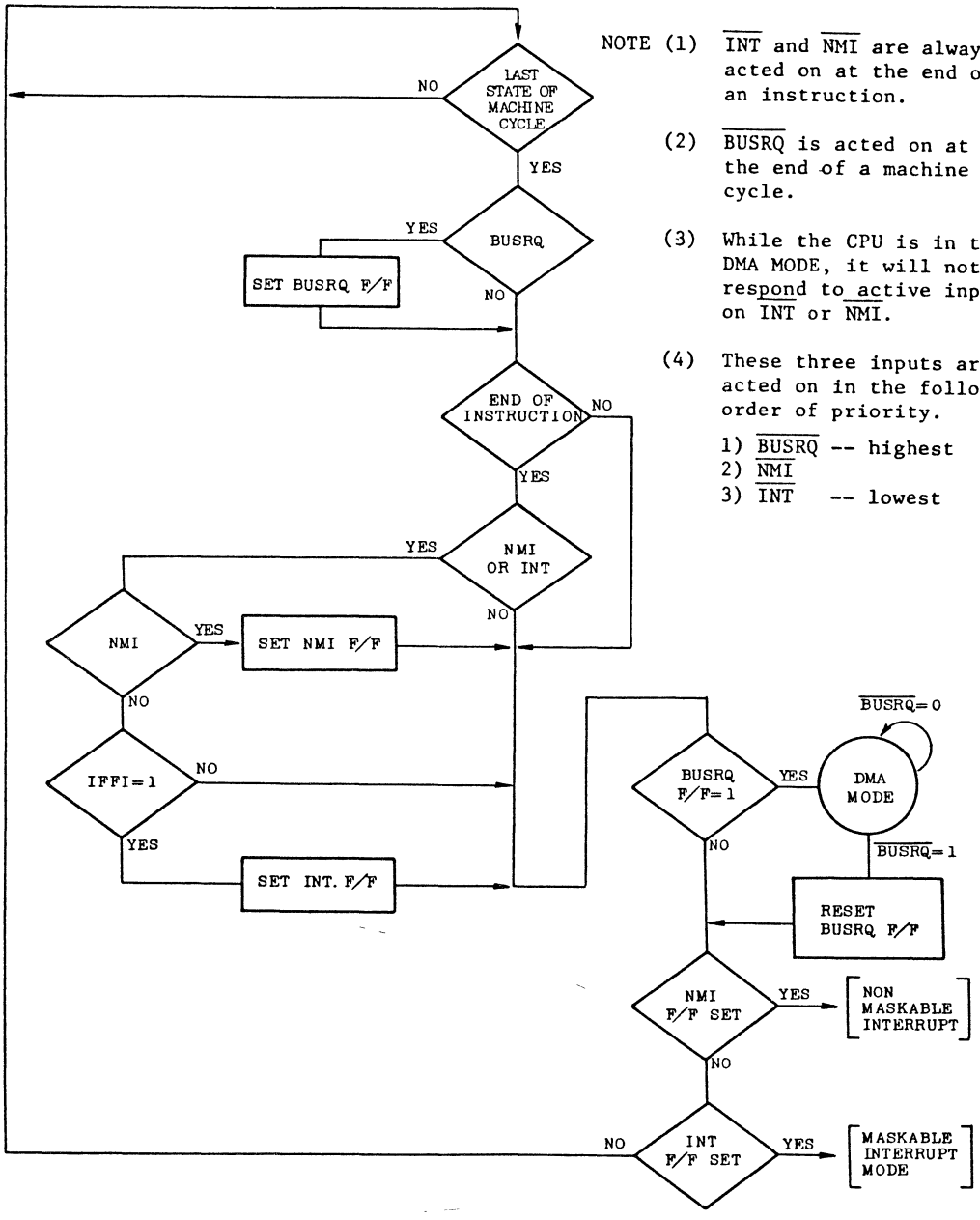
INTERRUPT

The CPU accepts two interrupt input signals: $\overline{NMI}$ and $\overline{INT}$. The $\overline{NMI}$ is a non-maskable interrupt and has the highest priority. $\overline{INT}$ is a lower priority interrupt since it requires that interrupts be enabled in software in order to operate. Either $\overline{NMI}$ or $\overline{INT}$ can be connected to multiple peripheral devices in a wired-OR configuration.

The Z80 has a single response mode for interrupt service for the non-maskable interrupt. The maskable interrupt, $\overline{INT}$, has three programmable response modes available.
These are:

- Mode 0 — compatible with the 8080 microprocessor.
- Mode 1 — Peripheral Interrupt service, for use with non-8080/Z80 systems.
- Mode 2 — a vectored interrupt scheme, usually daisy-chained, for use with Z80 family and compatible peripheral devices.

Both the $\overline{INT}$ and $\overline{NMI}$ inputs are sampled by the CPU on the rising edge of CLK in the last T state of the last Machine (M) cycle of any instruction. However, if $\overline{BUSRQ}$ is active at the same time, it will be processed before any interrupts. Figure 4 illustrates the Z80 interrupt service sequence.



NOTE (1) $\overline{INT}$ and $\overline{NMI}$ are always acted on at the end of an instruction.

(2) $\overline{BUSRQ}$ is acted on at the end of a machine cycle.

(3) While the CPU is in the DMA MODE, it will not respond to active inputs on $\overline{INT}$ or $\overline{NMI}$.

(4) These three inputs are acted on in the following order of priority.

1) $\overline{BUSRQ}$ -- highest
2) $\overline{NMI}$
3) $\overline{INT}$ -- lowest

FIGURE 4. Z80 CPU INTERRUPT SEQUENCE

(1) Non-Maskable Interrupt ($\overline{NMI}$)

The non-maskable interrupt cannot be disabled by program control and therefore will be accepted at all times by the CPU. $\overline{NMI}$ is usually reserved for servicing only the highest priority type interrupts, such as that for orderly shutdown after power failure has been detected. After recognition of the $\overline{NMI}$ signal (providing $\overline{BUSREQ}$ is not active), the CPU jumps to restart location 0066H. Normally, software starting at this address contains the interrupt service routine.

(2) Maskable Interrupt ($\overline{INT}$)

Regardless of the interrupt mode set by the user, the Z80 CPU response to a maskable interrupt input follows a common timing cycle. After the interrupt has been detected by the CPU (provided that interrupts are enabled and $\overline{BUSREQ}$ is not active) a special interrupt processing cycle begins. This is a special fetch ($\overline{M1}$) cycle in which $\overline{IORQ}$ becomes active rather than $\overline{MREQ}$, as in a normal $\overline{M1}$ cycle. In addition, this special $\overline{M1}$ cycle is automatically extended by two $\overline{WAIT}$ states, to allow for the time required to acknowledge the interrupt request and to place the interrupt vector on the bus.

- Mode 0 Interrupt Operation

This mode is compatible with the 8080 microprocessor interrupt service procedures. The interrupting device places an instruction on the data bus.

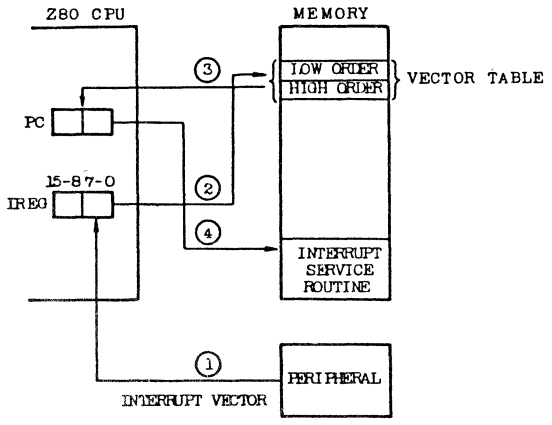
This is normally a Restart Instruction, which will initiate an unconditional jump to the selected one of eight restart locations in page zero of memory.

- Mode 1 Interrupt Operation

Mode 1 operation is very similar to that for the $\overline{NMI}$. The principal difference is that the Mode 1 interrupt has a vector address of 0038H only.

- Mode 2 Interrupt Operation

This interrupt mode has been designed to utilize most effectively the capabilities of the Z80 microprocessor and its associated peripheral family. The interrupting peripheral device selects the starting address of the interrupt service routine. It does this by placing an 8-bit address vector on the data bus during the interrupt acknolwedge cycle. The high-order byte of the interrupt service routine address is supplied by the I (Interrupt) register. This flexibility in selecting the interrupt service routine address allows the peripheral device to use several different types of service routines.
These routines may be located at any available location in memory. Since the interrupting device supplies the low-order byte of the 2-byte vector, bit 0 (A_0) must be a zero.
Figure 5 illustrates the vector processing sequence.



NOTES:

1) Interrupt vector generated by peripheral is read by CPU during interrupt acknowledge cycle.

2) Vector combined with I register contents form 16-bit memory address pointing to vector table.

3) Two bytes are read sequentially from vector table. These 2 bytes are read into PC.

4) Processor control is transferred to interrupt service routine and execution continues.

FIGURE 5. VECTOR PROCESSING SEQUENCE

(3) Interrupt Priority (Daisy Chaining and Nested Interrupts).

The interrupt priority of each peripheral device is determined by its physical location within a daisy-chain configuration. Each device in the chain has an interrupt enable input line (IEI) and an interrupt enable output line (IEO), which is fed to the next lower priority device. The first device in the daisy chain has its IEI input hardwired to a High level. The first device has highest priority, while each succeeding device has a corresponding lower priority. This arrangement permits the CPU to select the highest priority interrupt from several simultaneously interrupting peripherals.

The interrupting device disables its IEO line to the next lower priority peripheral until it has been serviced. After servicing, its IEO line is raised, allowing lower priority peripherals to demand interrupt servicing.

The Z80 CPU will nest (queue) any pending interrupts or interrupts received while a selected peripheral is being serviced.

(4) Interrupt Enable/Disable Operation.

In the Z80-CPU there is an enable flip flop (called IFF) that is set or reset by the programmer using the Enable Interrupt (EI) and Disable Interrupt (DI) instructions. When the IFF is reset, an interrupt (except $\overline{NMI}$) cannot be accepted by the CPU.

Actually, there are two enable flip flops, called IFF_1 and IFF_2.

IFF_1	IFF_2
Actually disables interrupts from being accepted.	Temporary storage location for IFF_1.

A reset to the CPU will force both IFF_1 and IFF_2 to the reset state so that interrupts are disabled. They can then be enabled by an EI instruction at any time by the programmer. When an EI instruction is executed, any pending interrupt request will not be accepted until after the instruction following EI has been executed. This single instruction delay is necessary for cases when the following instruction is a return instruction and interrupts must not be allowed until the return has been completed. Both IFF_1 and IFF_2 can be enabled by execution of the EI instruction. When an interrupt is accepted by the CPU, both IFF_1 and IFF_2 are automatically reset, inhibiting further interrupts until a new EI instruction is executed. Note that for all of the previous cases, IFF_1 and IFF_2 are always equal.

The purpose of IFF_2 is to save the status of IFF_1 when a non-maskable interrupt occurs. When a non-maskable interrupt is accepted, IFF_1 is reset to prevent further interrupts until reenable by the programmer. Thus, after a non-maskable interrupt has been accepted maskable interrupts are disabled but the previous state of IFF_1 has been saved so that the complete state of the CPU just prior to the non-maskable interrupt can be restored at any time. When a Load Register A with Register I (LD A, I) instruction or a Load Register A with Register R (LD A, R) instruction is executed, the state of IFF_2 is

copied into the parity flag where it can be tested or stored.

A second method of restoring the status of IFF_1 is thru the execution of a Return From Non-Maskable Interrupt (RETN) instruction. Since this instruction indicates that the non maskable interrupt service routine is complete, the contents of IFF_2 are now copied back into IFF_1, so that the status of IFF_1 just prior to the acceptance of the non-maskable interrupt will be restored automatically.

Operation of the two flip-flops is described in Table 3.

Action	IFF_1	IFF_2	Comments
CPU Reset	0	0	Maskable interrupt $\overline{INT}$ disabled
DI instruction execution	0	0	Maskable interrupt $\overline{INT}$ disabled
EI instruction execution	1	1	Maskable interrupt $\overline{INT}$ enabled
LD A,I instruction execution	-	-	IFF_2 → Parity flag
LD A,R instruction execution	-	-	IFF_2 → Parity flag
Accept $\overline{NMI}$	0	IFF_1	IFF_1 → IFF_2 (Maskable interrupt $\overline{INT}$ disabled)
RETN instruction execution	IFF_2	-	IFF_2 → IFF_1 at completion of an $\overline{NMI}$ service routine.
Accept $\overline{INT}$	0	0	
RETI	-	-	

Note) "-" indicates no change.

TABLE 3. STATE OF FLIP-FLOPS

CPU TIMING

The Z80 CPU executes instructions by proceeding through a specific sequence of operations. These include:

Memory read or write

I/O device read or write

Interrupt acknowledge

All instructions are merely a series of these basic operations. Each of these basic operations can take from three to six clock periods to complete or they can be lengthened to synchronize the CPU to the speed of external devices. The basic clock periods are referred to as T states and the basic operations are referred to as M (for machine) cycles. Figure 6 illustrates how a typical instruction will be merely a series of specific M and T cycles. Notice that this instruction consists of three machine cycles (M1, M2 and M3). The first machine cycle of any instruction is a fetch cycle which is four, five or six T states long (unless lengthened by the wait signal). The fetch cycle (M1) is used to fetch the OP code of the next instruction to be executed. Subsequent machine cycles move data between the CPU and memory or I/O devices and they may have anywhere from three to five T cycles (again they may be lengthened by wait states to synchronize the external devices to the CPU). The following paragraphs describe the timing which occurs within any of the basic machine cycles.

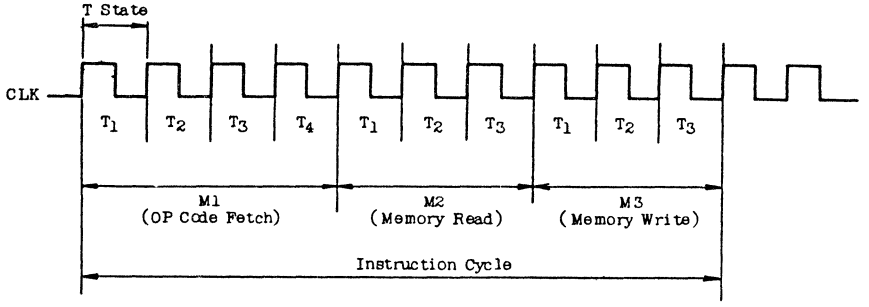


FIGURE 6. BASIC CPU TIMING EXAMPLE

All CPU timing can be broken down into some very simple timing diagrams as shown in Figure 7 through 14. These diagrams show the following basic operations with and without wait states (wait states are added to synchronize the CPU to slow memory or I/O devices).

Fig. 7 Instruction OP code fetch (M1 cycle)

Fig. 8 Memory data read or write cycles

Fig. 9 I/O read or write cycles

Fig. 10 Bus Request/Acknowledge Cycle

Fig. 11 Interrupt Request/Acknowledge Cycle

Fig. 12 Non maskable Interrupt Request/Acknowledge Cycle

Fig. 13 Exit from a HALT instruction

Fig. 14 Reset Cycle

(1) Instruction fetch

Figure 7-0 shows the timing during an M1 cycle (OP code fetch). Notice that the PC is placed on the address bus at the beginning of the M1 cycle. One halt clock time later the $\overline{MREQ}$ signal goes active. At this time the address to the memory has had time to stabilize so that the falling edge of $\overline{MREQ}$ can be used directly as a chip enable clock to dynamic memories. The $\overline{RD}$ line also goes active to indicate that the memory read data should be enabled onto the CPU data bus. The CPU samples the data from the memory on the data bus with the rising edge of the clock of state T3 and this same edge is used by the CPU to turn off the $\overline{RD}$ and $\overline{MREQ}$ signals. Thus the data has already been sampled by the CPU before the $\overline{RD}$ signal becomes inactive. Clock state T3 and T4 of a fetch cycle are used to refresh dynamic memories. (The CPU uses this time to decode and execute the fetched instruction so that no other operation could be performed at this time). During T3 and T4 the lower 7-bits of the address bus contain a memory refresh address and the $\overline{RFSH}$ signal becomes active to indicate that a refresh read of all dynamic memories should be accomplished. Notice that a $\overline{RD}$ signal is not generated during refresh time to prevent data from different memory segments from being gated onto the data bus. The $\overline{MREQ}$ signal during refresh time should be used to perform a refresh read of all memory elements. The refresh signal cannot be used by itself since the refresh address is only guaranteed to be stable during $\overline{MREQ}$ time.

Figure 7-1 illustrates how the fetch cycle is delayed if the memory activates the $\overline{WAIT}$ line. During T2 and every subsequent Tw, the CPU samples the $\overline{WAIT}$ line with the falling edge of CLK. If the $\overline{WAIT}$ line is active at this time, another wait state will be entered during the following cycle. Using this technique the read cycle can be lengthened to match the access time of any type of memory device.

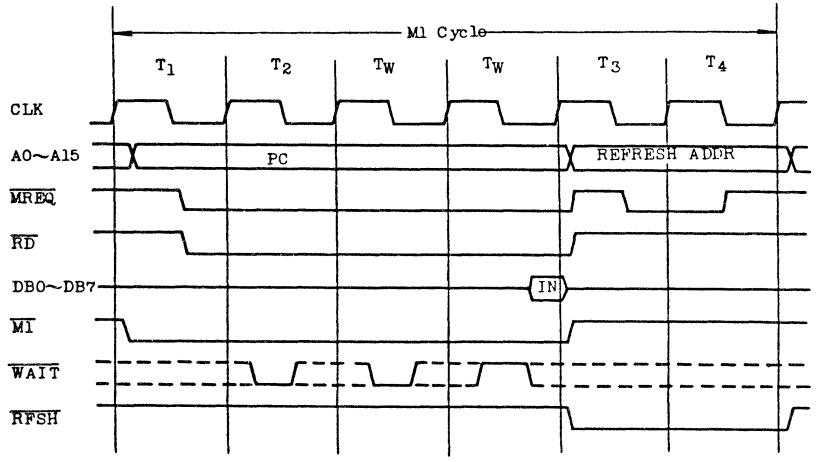


FIGURE 7-1. INSTRUCTION OP CODE FETCH WITH WAIT STATES

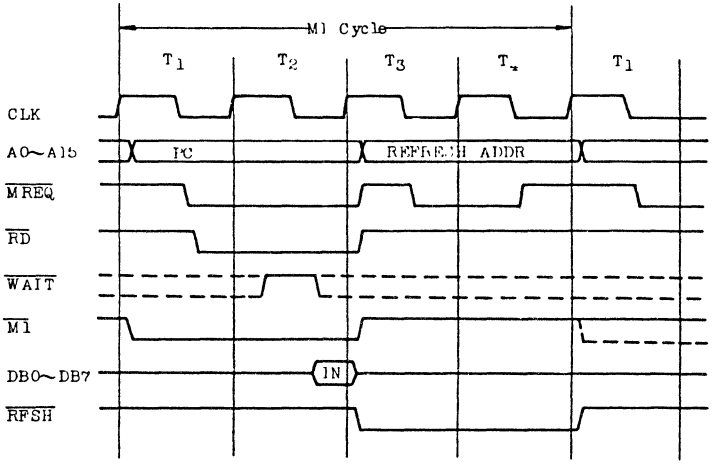


FIGURE 7-0. INSTRUCTION OP CODE FETCH

(2) Memory read or write

Figure 8-0 illustrates the timing of memory read or write cycles other than an OP code fetch (M1 cycle). These cycles are generally three clock periods long unless wait states are requested by the memory via the $\overline{WAIT}$ signal. The $\overline{MREQ}$ signal and the $\overline{RD}$ signal are used the same as in the fetch cycle. In the case of a memory write cycle, the $\overline{MREQ}$ also becomes active when the address bus is stable so that it can be used directly as a chip enable for dynamic memories. The $\overline{WR}$ line is active when data on the data bus is stable so that it can be used directly as a R/W pulse to virtually any type of semiconductor memory.

Furthermore the $\overline{WR}$ signal goes inactive one halt T state before the address and data bus contents are changed so that the overlap requirements for virtually any type of semiconductor memory type will be met.

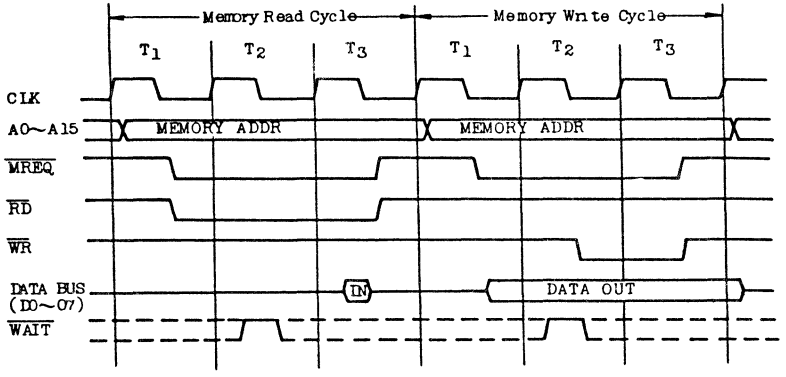


FIGURE 8-0. MEMORY READ OR WRITE CYCLES

Figure 8-1 illustrates how a $\overline{WAIT}$ request signal will lengthen any memory read or write operation. This operation is identical to that previously described for a fetch cycle. Notice in this figure that a separate read and a separate write cycle are shown in the same figure although read and write cycles can never occur simultaneously.

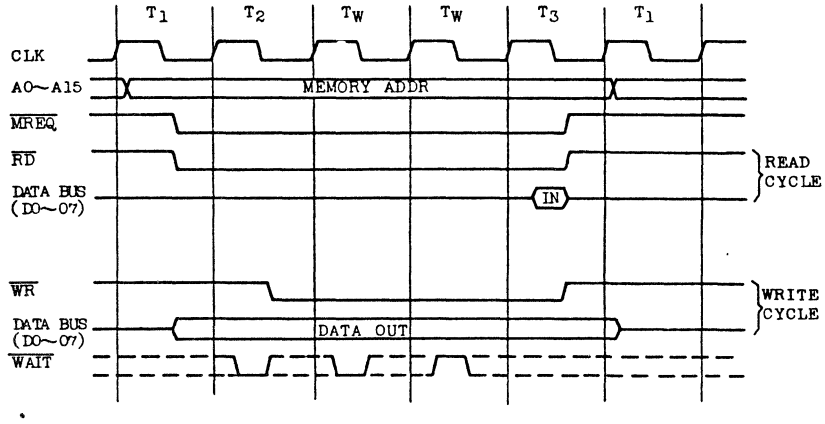


FIGURE 8-1. MEMORY READ OR WRITE CYCLES WITH WAIT STATES

(3) Input or output cycles

Figure 9-0 illustrates an I/O read or I/O write operation. Notice that during I/O operations a single wait state is automatically inserted. The reason for this is that during I/O operations, the time from when the $\overline{IORQ}$ signal goes active until the CPU must sample the $\overline{WAIT}$ line is very short and without this extra state sufficient time does not exist for an I/O port to decode its address and activate the $\overline{WAIT}$ line if a wait is required. Also, without this wait state it is difficult to design MOS I/O devices that can operate at full CPU speed. During this wait state time the $\overline{WAIT}$ request signal is sampled. During a read I/O operation, the RD line is used to enable the addressed port onto the data bus just as in the case of a memory read. For I/O write operations, the $\overline{WR}$ line is used as a clock to the I/O port, again with sufficient overlap timing automatically provided so that the rising edge may be used as a data clock.

Figure 9-1 illustrates how additional wait states may be added with the $\overline{WAIT}$ line. The operation is identical to that previously described.

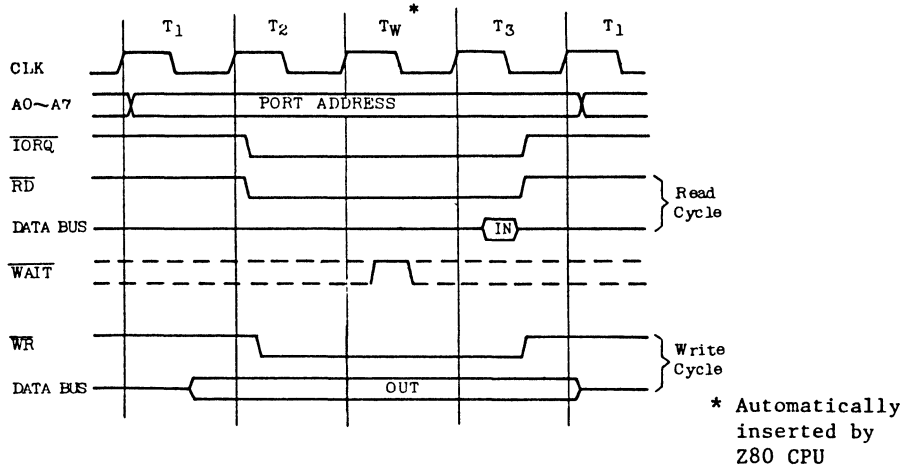


FIGURE 9-0. INPUT OR OUTPUT CYCLES

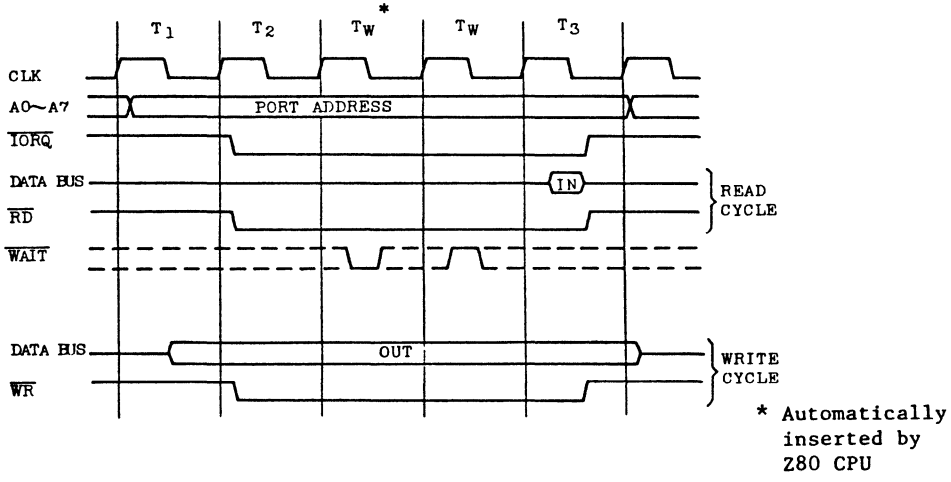


FIGURE 9-1. INPUT OR OUTPUT CYCLES WITH WAIT STATES

(4) Bus request/acknowledge cycle

Figure 10 illustrates the timing for a Bus Request/Acknowledge cycle. The $\overline{BUSRQ}$ signal is sampled by the CPU with the rising edge of the last clock period of any machine cycle. If the $\overline{BUSRQ}$ signal is active, the CPU will set its address, data and tri-state control signals to the high impedance state with the rising edge of the next clock pulse. At that time any external device can control the buses to transfer data between memory and I/O devices. (This is generally known as Direct Memory Access [DMA] using cycle stealing).

The maxunyn time for the CPU to respond to a bus request is the length of a machine cycle and the external controller can maintain control of the bus for as many clock cycles as is desired.
Note, however, that if very long DMA cycles are used, and dynamic memories are being used, the external controller must also perform the refresh function. This situation only occurs if very large blocks of data are transferred under DMA control. Also note that during a bus request cycle, the CPU cannot be interrupted by either a $\overline{NMI}$ or an $\overline{INT}$ signal.

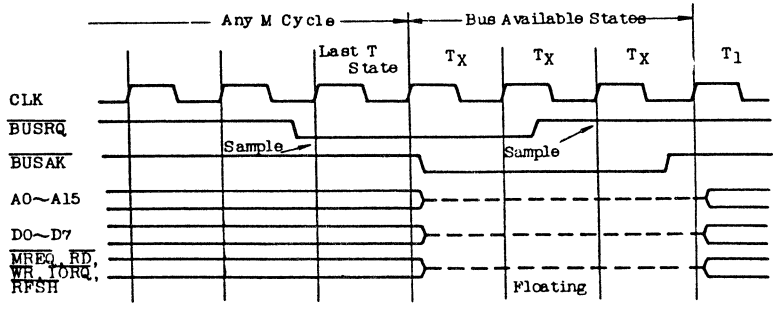


FIGURE 10. BUS REQUEST/ACKNOWLEDGE CYCLE

(5) Interrupt request/acknowledge cycle

Figure 11-0 illustrates the timing associated with an interrupt cycle. The interrupt signal ($\overline{INT}$) is sampled by the CPU with the rising edge of the last clock at the end of any instruction. The signal will not be accepted if the internal CPU software controlled interrupt enable flip-flop is not set or if the $\overline{BUSRQ}$ signal is active. When the signal is accepted a special M1 cycle is generated. During this special M1 cycle the $\overline{IORQ}$ signal becomes active (instead of the normal $\overline{MREQ}$) to indicate that the interrupting device can place an 8-bit vector on the data bus. Notice that two wait states are automatically added to this cycle. These states are added so that a ripple priority interrupt scheme can be easily implemented. The two wait states allow sufficient time for the ripple signals to stabilize and identify which I/O device must insert the response vector.

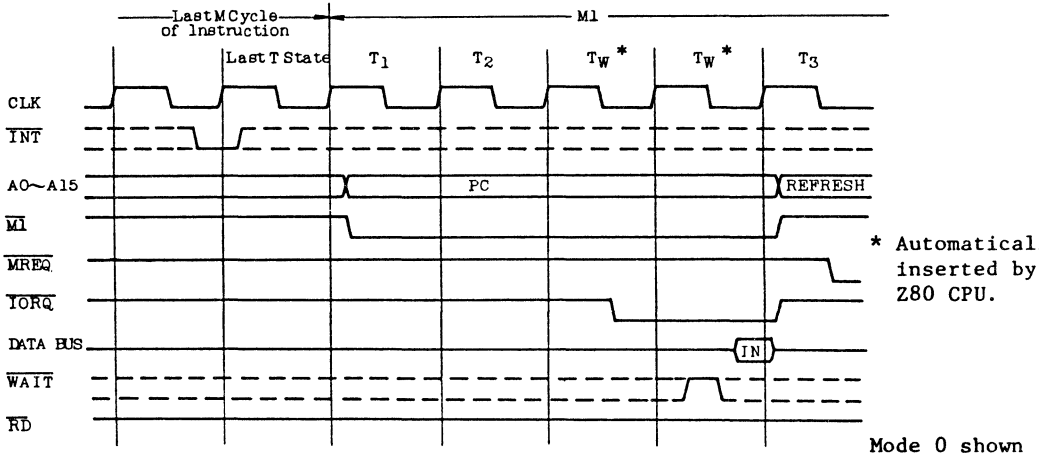


FIGURE 11-0. INTERRUPT REQUEST/ACKNOWLEDGE CYCLE

Figure 11-1 illustrates how additional wait states can be added to the interrupt response cycle. Again the operation is identical to that previously described.

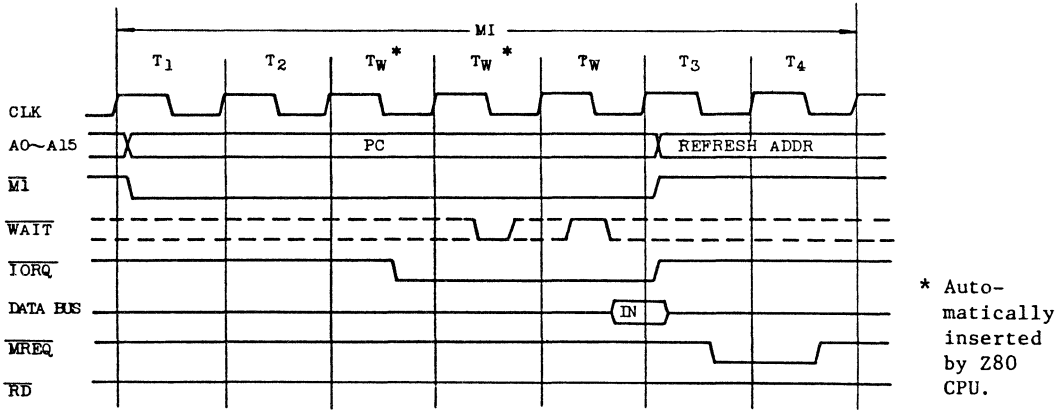


FIGURE 11-1. INTERRUPT REQUEST/ACKNOWLEDGE WITH WAIT STATES

(6) Non maskable interrupt response

Figure 12 illustrates the request/acknowledge cycle for the non-maskable interrupt. A pulse on the $\overline{NMI}$ input sets an internal NMI latch which is tested by the CPU at the end of every instruction. This NMI latch is sampled at the same time as the interrupt line, but this line has priority over the normal interrupt and it cannot be disabled under software control. Its usual function is to provide immediate response to important signals such as an impending power failure. The CPU response to a non maskable interrupt is similar to a normal memory read operation. The only difference being that the content of the data bus is ignored while the processor automatically stores the PC in the external stack and jumps to location 0066H. The service routine for the non maskable interrupt must begin at this location if this interrupt is used.

(7) Halt acknowledge cycle and exit

Whenever a software halt instruction is executed the CPU begins executing NOP's until an interrupt is received (either a non-maskable or a maskable interrupt while the interrupt flip flop is enabled). The two interrupt lines are sampled with the rising clock edge during each T4 state as shown in Figure 13. If a non-maskable interrupt has been received or a maskable interrupt has been received and the interrupt enable flip-flop is set, then the halt state will be exited on the next rising clock edge. The following cycle will then be an interrupt acknowledge cycle corresponding to the type of interrupt that was received. If both are received at this time, then the

non maskable one will be acknowledged since it was highest priority. The purpose of executing NOP instructions while in the halt state is to keep the memory refresh signals active. Each cycle in the halt state is a normal M1 (fetch) cycle except that the data received from the memory is ignored and a NOP instruction is forced internally to the CPU. The halt acknowledge signal is active during this time to indicate that the processor is in the halt state.

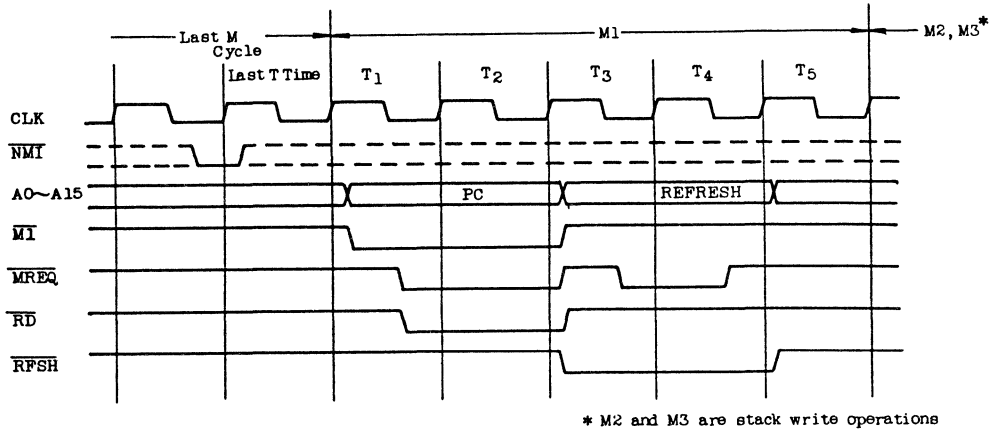


FIGURE 12. NON MASKABLE INTERRUPT RESPONSE

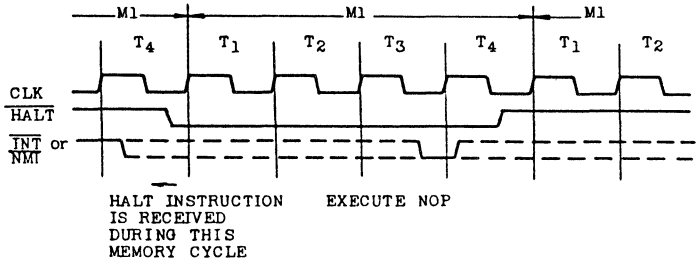


FIGURE 13. HALT ACKNOWLEDGE CYCLE AND EXIT

(8) Reset cycle

$\overline{\text{RESET}}$ must be active for at least three clock cycles for the CPU to properly accept it. As long as $\overline{\text{RESET}}$ remains active, the address and data buses float, and the control outputs are inactive.

Once $\overline{\text{RESET}}$ goes inactive, two internal T cycles are consumed before the CPU resumes normal processing operation. $\overline{\text{RESET}}$ clears the PC (program counter), so the first OPcode fetch will be to location 0000_H.

(See Figure 14.)

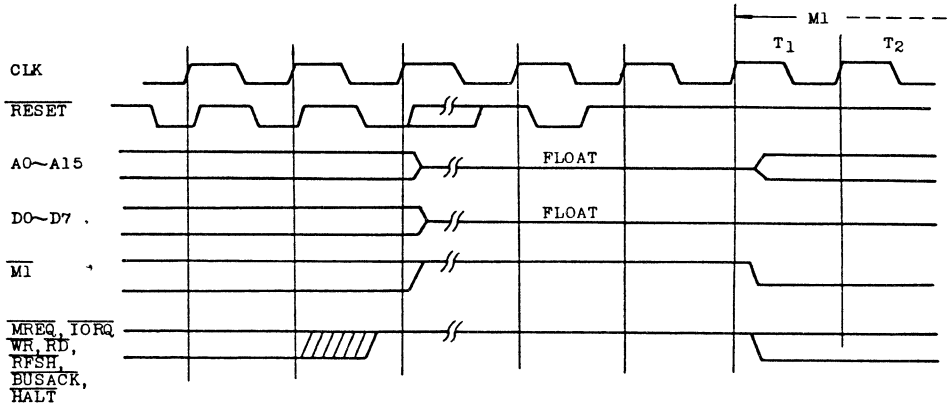


FIGURE 14. RESET CYCLE

POWER DOWN FUNCTION

When system clock to Z80 CPU is stopped at either a high or low level, Z80 CPU stops its operation and maintains registers and control signals.

However I_{CC2} Stand-by Supply Current is guaranteed only when the supplied system clock is stopped at a low level during T4 state of the following machine cycle (actually that is M1 cycle and executes NOP instruction) next to OPcode fetch cycle of HALT instruction. The timing diagram when POWER DOWN FUNCTION is implemented by HALT instruction is shown as figure 15.

This function can be easily realized when T6497 clock generator controller is connected with Z80 CPU.

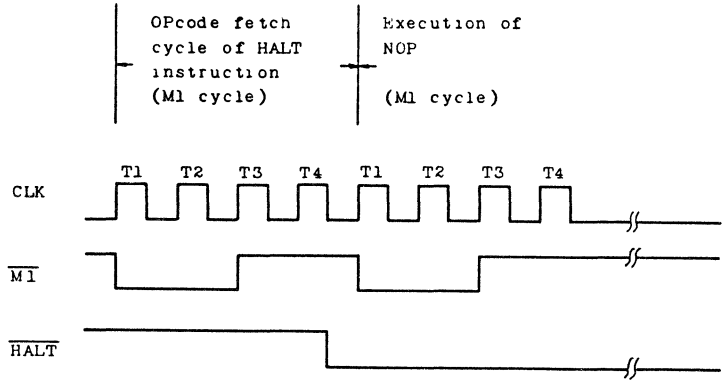


FIGURE 15. TIMING DIAGRAM OF POWER DOWN FUNCTION BY HALT INSTRUCTION

RELEASE FROM POWER DOWN STATE

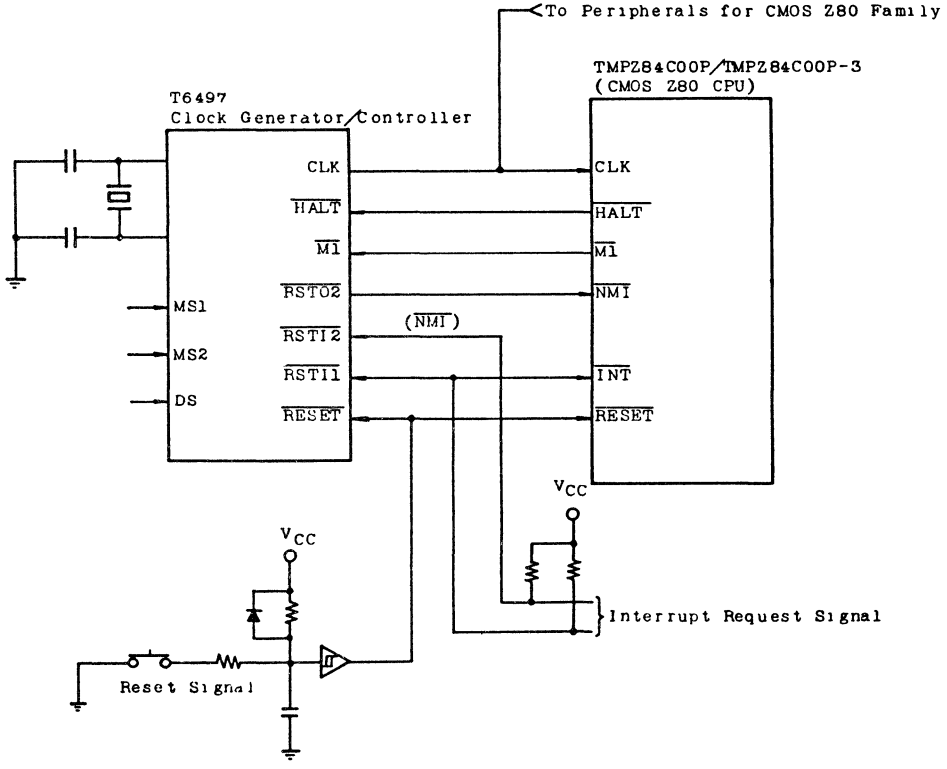
The system clock must be supplied to Z80 CPU to release power down state. When the system clock is supplied to CLK terminal of Z80 CPU, CPU restarts operation continuously from the state when power down function has been implemented.

Note the followings when release from power down state.

(1) When external oscillator has been stopped to enter power down state, some warming-up time may be required to obtain precious and stable system clock for release from power down state.

(2) When HALT instruction is executed to enter power down state, Z80 CPU will enter HALT state. An interrupt signal ($\overline{NMI}$ or $\overline{INT}$) or $\overline{RESET}$ signal must be generated to Z80 CPU after the system clock is supplied to release power down state. Otherwise Z80 CPU is still in HALT state even if the system clock is supplied.

Figure 16 shows an example to connect with T6497 clock generator/controller.



INSTRUCTION SET

The Z80 microprocessor has one of the most powerful and versatile instruction sets available in any 8-bit microprocessor.
It includes such unique operations as a block move for fast, efficient data transfers within memory or between memory and I/O. It also allows operations on any bit in any location in memory.

The Z80 CPU can execute 158 different instruction types including all 78 of the 8080A CPU.

The instructions are devided into the following categories:

- 8-bit loads
- 16-bit loads
- Exchanges, block transfers, and searches
- 8-bit arithmetic and logic operations
- General-purpose arithmetic and CPU control
- 16-bit arithmetic operations
- Rotates and shifts
- Bit set, reset, and test operations
- Jumps
- Calls, returns, and restarts
- Input and output operations

A variety of addressing modes are implemented to permit efficient and data transfer between various registers, memory locations, and input/output devices. These addressing modes are as follows:

- Immediate
- Immediate extended
- Modified page zero
- Relative
- Extended
- Indexed
- Resister
- Resister indirect
- Implied
- Bit

8-BIT LOAD GROUP

Mnemonic	Instruction $D_7D_6D_5D_4D_3D_2D_1D_0$	Code Hex	Operation	Flags S	Z	H	P/V	N	C	No. of Bytes	No. of M Cycles	No. of T States	Comments
LDr,r	0 1 ← r → ← r' →		r ← r'	–	–	–	–	–	–	1	1	4	r,r Reg.
LDr,n	0 0 ← r → 1 1 0 ← n →		r ← n	–	–	–	–	–	–	2	2	7	000 B 001 C
LDr,(HL)	0 1 ← r → 1 1 0		r ← (HL)	–	–	–	–	–	–	1	2	7	010 D
LDr,(IX+d)	1 1 0 1 1 1 0 1 0 1 ← r → 1 1 0 ← d →	DD	r ← (IX+d)	–	–	–	–	–	–	3	5	19	011 E 100 H 101 L
LDr,(IY+d)	1 1 1 1 1 1 0 1 0 1 ← r → 1 1 0 ← d →	FD	r ← (IY+d)	–	–	–	–	–	–	3	5	19	111 A
LD(HL),r	0 1 1 1 0 ← r →		(HL) ← r	–	–	–	–	–	–	1	2	7	
LD(IX+d),r	1 1 0 1 1 1 0 1 0 1 1 1 0 ← r → ← d →	DD	(IX+d) ← r	–	–	–	–	–	–	3	5	19	
LD(IY+d),r	1 1 1 1 1 1 0 1 0 1 1 1 0 ← r → ← d →	FD	(IY+d) ← r	–	–	–	–	–	–	3	5	19	
LD(HL),n	0 0 1 1 0 1 1 0 ← n →	36	(HL) ← n	–	–	–	–	–	–	2	3	10	
LD(IX+d),n	1 1 0 1 1 1 0 1 0 0 1 1 0 1 1 0 ← d → ← n →	DD	(IX+d) ← n	–	–	–	–	–	–	4	5	19	
LD(IY+d),n	1 1 1 1 1 1 0 1 0 0 1 1 0 1 1 0 ← d → ← n →	FD 36	(IY+d) ← n	–	–	–	–	–	–	4	5	19	
LD A, (BC)	0 0 0 0 1 0 1 0	0A	A ← (BC)	–	–	–	–	–	–	1	2	7	
LD A, (DE)	0 0 0 1 1 0 1 0	1A	A ← (DE)	–	–	–	–	–	–	1	2	7	
LD A, (nn)	0 0 1 1 1 0 1 0 ← n → ← n →	3A	A ← (nn)	–	–	–	–	–	–	3	4	13	
LD(BC),A	0 0 0 0 0 0 1 0	02	(BC) ← A	–	–	–	–	–	–	1	2	7	
LD(DE),A	0 0 0 1 0 0 1 0	12	(DE) ← A	–	–	–	–	–	–	1	2	7	
LD(nn),A	0 0 1 1 0 0 1 0 ← n → ← n →	32	(nn) ← A	–	–	–	–	–	–	3	4	13	
LD A, I	1 1 1 0 1 1 0 1 0 1 0 1 0 1 1 1	ED 57	A ← I	0	0	R	IFF	R	–	2	2	9	
LD A, R	1 1 1 0 1 1 0 1 0 1 0 1 1 1 1 1	ED 5F	A ← R	0	0	R	IFF	R	–	2	2	9	
LDI,A	1 1 1 0 1 1 0 1 0 1 0 0 0 1 1 1	ED 47	I ← A	–	–	–	–	–	–	2	2	9	
LD R, A	1 1 1 0 1 1 0 1 0 1 0 0 1 1 1 1	ED 4F	R ← A	–	–	–	–	–	–	2	2	9	

Notes: r,r' means any of the registers A, B, C, D, E, H, L
IFF the content of the interrupt enable flip-flop (IFF) is copied into the P/V flag
Flag Notation: – = flag not affected, R = flag reset, S = flag set.
0 = flag is affected according to the result of the operation.

16-BIT LOAD GROUP

Mnemonic	Instruction Code $D_7D_6D_5D_4D_3D_2D_1D_0$	Hex	Operation	Flags S	Z	H	P/V	N	C	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD dd,nn	0 0 d d 0 0 0 1 ← n → ← n →		dd ← nn	–	–	–	–	–	–	3	3	10	dd Pair 00 BC 01 DE 10 HL 11 SP
LDIX,nn	1 1 0 1 1 1 0 1 0 0 1 0 0 0 0 1 ← n → ← n →	DD 21	IX ← nn	–	–	–	–	–	–	4	4	14	
LDIY,nn	1 1 1 1 1 1 0 1 0 0 1 0 0 0 0 1 ← n → ← n →	FD 21	IY ← nn	–	–	–	–	–	–	4	4	14	
LD HL, (nn)	0 0 1 0 1 0 1 0 ← n → ← n →	2A	H ← (nn+1) L (nn)	–	–	–	–	–	–	3	5	16	
LDdd, (nn)	1 1 1 0 1 1 0 1 0 1 d d 1 0 1 1 ← n → ← n →	ED	dd_H ← (nn+1) dd_L ← (nn)	–	–	–	–	–	–	4	6	20	
LDIX, (nn)	1 1 0 1 1 1 0 1 0 0 1 0 1 0 1 0 ← n → ← n →	DD 2A	IX_H ← (nn+1) IX_L ← (nn)	–	–	–	–	–	–	4	6	20	
LDIY, (nn)	1 1 1 1 1 1 0 1 0 0 1 0 1 0 1 0 ← n → ← n →	FD 2A	IY_H ← (nn+1) IY_L ← (nn)	–	–	–	–	–	–	4	6	20	
LD(nn),HL	0 0 1 0 0 0 1 0 ← n → ← n →	22	(nn+1) ← H (nn) ← L	–	–	–	–	–	–	3	5	16	
LD(nn),dd	1 1 1 0 1 1 0 1 0 1 d d 0 0 1 1 ← n → ← n →	ED	(nn+1) ← dd_H (nn) ← dd_L	–	–	–	–	–	–	4	6	20	
LD(nn),IX	1 1 0 1 1 1 0 1 0 0 1 0 0 0 1 0 ← n → ← n →	DD 22	(nn+1) ← IX_H (nn) ← IX_L	–	–	–	–	–	–	4	6	20	
LD(nn),IY	1 1 1 1 1 1 0 1 0 0 1 0 0 0 1 0 ← n → ← n →	FD 22	(nn+1) ← IY_H (nn) ← IY_L	–	–	–	–	–	–	4	6	20	
LD SP,HL	1 1 1 1 1 0 0 1	F9	SP ← HL	–	–	–	–	–	–	1	1	6	
LD SP, IX	1 1 0 1 1 1 0 1 1 1 1 1 1 0 0 1	DD F9	SP ← IX	–	–	–	–	–	–	2	2	10	
LD SP, IY	1 1 1 1 1 1 0 1 1 1 1 1 1 0 0 1	FD F9	SP ← IY	–	–	–	–	–	–	2	2	10	

Mnemonic	Instruction Code		Operation	Flags						No. of Bytes	No. of M Cycles	No. of T States	Comments
	$D_7D_6D_5D_4D_3D_2D_1D_0$	Hex		S	Z	H	P/V	N	C				
PUSHqq	1 1 q q 0 1 0 1		(SP-2)←qq$_L$ (SP-1)←qq$_H$ SP→SP-2	-	-	-	-	-	-	1	3	11	qq Pair 00 BC 01 DE 10 HL 11 AF
PUSH IX	1 1 0 1 1 1 0 1 1 1 1 0 0 1 0 1	DD E5	(SP-2)←IX$_L$ (SP-1)←IX$_H$ SP→SP-2	-	-	-	-	-	-	2	4	15	
PUSH IY	1 1 1 1 1 1 0 1 1 1 1 0 0 1 0 1	FD E5	(SP-2)←IYL (SP-2)←IY$_H$ SP→SP-2	-	-	-	-	-	-	2	4	15	
POPqq	1 1 q q 0 0 0 1		qq$_H$←(SP+1) qq$_L$←(SP) SP→SP+2	-	-	-	-	-	-	1	3	10	
POPIX	1 1 0 1 1 1 0 1 1 1 1 0 0 0 0 1	DD E1	IX$_H$←(SP+1) IX$_L$←(SP) SP→SP+2	-	-	-	-	-	-	2	4	14	
POPIY	1 1 1 1 1 1 0 1 1 1 1 0 0 0 0 1	FD E1	IY$_H$←(SP+1) IY$_L$←(SP) SP→SP+2	-	-	-	-	-	-	2	4	14	

Notes: dd is any of the register pairs BC, DE, HL, SP
qq is any of the register pairs AF, BC, DE, HL
$(PAIR)_H$, $(PAIR)_L$ refer to high order and low order eight bits of the register pair respectively. e.g. BC_L=C, AF_H=A

Flag Notation: - = flag not affected, R = flag reset, S = flag set,
O=flag is affected according to the result of the operation.

EXCHANGE GROUP AND BLOCK TRANSFER AND SEARCH GROUP

Mnemonic	Instruction Code $D_7D_6D_5D_4D_3D_2D_1D_0$	Hex	Operation	Flags S	Z	H	P/V	N	C	No. of Bytes	No. of M Cycles	No. of T States	Comments
EX DE, HL	1 1 1 0 1 0 1 1	EB	DE↔HL	-	-	-	-	-	-	1	1	4	
EX AF, AF'	0 0 0 0 1 0 0 0	08	AF↔AF'	-	-	-	-	-	-	1	1	4	(Exx) Register bank and auxiliary register bank exchange
EXX	1 1 0 1 1 0 0 1	D9	(BC↔BC' DE↔DE' HL↔HL')	-	-	-	-	-	-	1	1	4	
EX(SP),HL	1 1 1 0 0 0 1 1	E3	H↔(SP+1) L↔(SP)	-	-	-	-	-	-	1	5	19	
EX(SP),IX	1 1 0 1 1 1 0 1 1 1 1 0 0 0 1 1	DD E3	IX_H↔(SP+1) IX_L↔(SP)	-	-	-	-	-	-	2	6	23	
EX(SP),IY	1 1 1 1 1 1 0 1 1 1 1 0 0 0 1 1	FD E3	IY_H↔(SP+1) IY_L↔(SP)	-	-	-	-	-	-	2	6	23	
LDI	1 1 1 0 1 1 0 1 1 0 1 0 0 0 0 0	ED A0	(DE)←(HL) DE←DE+1 HL←HL+1 BC←BC-1	-	-	R	①	R	-	2	4	16	*1
LDIR	1 1 1 0 1 1 0 1 1 0 1 1 0 0 0 0	ED B0	(DE)←(HL) DE←DE+1 HL←HL+1 BC←BC-1 Repeat until BC=0	-	-	R	R	R	-	2 2	5 4	21 16	If BC≠0 If BC=0
LDD	1 1 1 0 1 1 0 1 1 0 1 0 1 0 0 0	ED A8	(DE)←(HL) DE←DE-1 HL←HL-1 BC←BC-1	-	-	R	①	R	-	2	4	16	
LDDR	1 1 1 0 1 1 0 1 1 0 1 1 1 0 0 0	ED B8	(DE)←(HL) DE←DE-1 HL←HL-1 BC←BC-1 Repeat until BC=0	-	-	R	R	R	-	2 2	5 4	21 16	If BC≠0 If BC=0
CPI	1 1 1 0 1 1 0 1 1 0 1 0 0 0 0 1	ED A1	A-(HL) HL←HL+1 BC←BC-1	○	②	○	①	S	-	2	4	16	
CPIR	1 1 1 0 1 1 0 1 1 0 1 1 0 0 0 1	ED B1	A-(HL) HL←HL+1 BC←BC-1 Repeat until A=(HL) or BC=0	○	②	○	①	S	-	2 2	5 4	21 16	*2 *3
CPD	1 1 1 0 1 1 0 1 1 0 1 0 1 0 0 1	ED A9	A-(HL) HL←HL-1 BC←BC-1	○	②	○	①	S	-	2	4	16	

Nmenomic	Instruction Code		Operation	Flags						No. of Bytes	No. of M Cycles	No. of T States	Comments
	$D_7D_6D_5D_4D_3D_2D_1D_0$	Hex		S	Z	H	P/V	N	C				
CPDR	1 1 1 0 1 1 0 1 1 0 1 1 1 0 0 1	ED B9	A-(HL) HL←HL-1 BC←BC-1 Repeat until A=(HL)or BC=0	0	②	0	①	S	-	2 2	5 4	21 16	*2 *3

Notes: ① P/V flag is 0 if the result of BC-1,=0, otherwise P/V=1
② Z flag is 1 if A=(HL), otherwise Z=0.

Flag Notation: - = flag not affected, R = flag reset, S = flag set.
0 = flag is affected according to the result of the operation.

*1 LDI: Load (HL) into (DE), increment the pointers and decrement the byte counter (BC).

*2 : If BC≠0 and A≠(HL)

*3 : If BC=0 or A=(HL)

8-BIT ARITHMETIC AND LOGICAL GROUP

Mnemonic	Instruction Code $D_7D_6D_5D_4D_3D_2D_1D_0$	Hex	Operation	Flags S	Z	H	P/V	N	C	No. of Bytes	No. of M Cycles	No. of T States	Comments
ADD A,r	1 0 [0 0 0] ← r →		A←A+r	0	0	0	V	R	0	1	1	4	r Reg. 000 B 001 C 010 D 011 E 100 H 101 L 111 A
ADD A,n	1 1 [0 0 0] 1 1 0 ← n →		A←A+n	0	0	0	V	R	0	2	2	7	
ADD A,(HL)	1 0 [0 0 0] 1 1 0		A←A+(HL)	0	0	0	V	R	0	1	2	7	
ADD A,(IX+d)	1 1 0 1 1 1 0 1 1 0 [0 0 0] 1 1 0 ← d →	DD	A←A+(IX+d)	0	0	0	V	R	0	3	5	19	
ADD A,(IY+d)	1 1 1 1 1 1 0 1 1 0 [0 0 0] 1 1 0 ← d →	FD	A←A+(IY+d)	0	0	0	V	R	0	3	5	19	
ADCA,s	[0 0 1]		A←A+s+CY	0	0	0	V	R	0				s is any of r, n, (HL),(IX+d), (IY+d)as shown for ADD instruction.
SUBs	[0 1 0]		A←A-s	0	0	0	V	S	0				
SBCA,s	[0 1 1]		A←A-s-CY	0	0	0	V	S	0				
ANDs	[1 0 0]		A←A ∧ s	0	0	S	P	R	R				
ORs	[1 1 0]		A←A ∨ s	0	0	R	P	R	R				
XORs	[1 0 1]		A←A ⊕ s	0	0	R	P	R	R				
CPs	[1 1 1]		A-s	0	0	0	V	S	0				
INCr	0 0 ← r → [1 0 0]		r←r+1	0	0	0	V	R	-	1	1	4	The indicated bits replace the [000] in the ADD set above.
INC(HL)	0 0 1 1 0 [1 0 0]		(HL)←(HL)+1	0	0	0	V	R	-	1	3	11	
INC(IX+d)	1 1 0 1 1 1 0 1 0 0 1 1 0 [1 0 0] ← d →	DD	(IX+d)← (IX+d)+1	0	0	0	V	R	-	3	6	23	
INC(IY+d)	1 1 1 1 1 1 0 1 0 0 1 1 0 [1 0 0] ← d →	FD	(IY+d)← (IY+d)+1	0	0	0	V	R	-	3	6	23	
DECs	[1 0 1]		s←s-1	0	0	0	V	S	-				s is any of r,(HL), (IX+d),(IY +d) as shown for INC. DEC same format and states as INC. Replace [100] with [101] in OP Code.

Notes: The V symbol in the P/V flag column indicates that the P/V flag contains the overflow of the result of the operation. Similarly the P symbol indicates parity. V=1 means overflow, V=0 means not overflow, P=1 means parity of the result is even, P=0 means parity of the result is odd.

Flag Notation: - = flag not affected, R = flag reset, S = flag set,
O = flag is affected according to the result of the operation.

GENERAL PURPOSE ARITHMETIC AND CPU CONTROL GROUPS

Mnemonic	Instruction Code $D_7D_6D_5D_4D_3D_2D_1D_0$	Hex	Operation	Flags S	Z	H	$P/\overline{V}$	N	C	No. of Bytes	No. of M Cycles	No. of T States	Comments
DAA	0 0 1 0 0 1 1 1	27	Converts acc, content into packed BCD following add or subtract with packed BCD operands	0	0	0	P	-	0	1	1	4	Decimal adjust accumulator
CPL	0 0 1 0 1 1 1 1	2F	$A \leftarrow \overline{A}$	-	-	S	-	S	-	1	1	4	
NEG	1 1 1 0 1 1 0 1 0 1 0 0 0 1 0 0	ED 44	$A \leftarrow \overline{A}+1$	0	0	0	V	S	0	2	2	8	
CCF	0 0 1 1 1 1 1 1	3F	$CY \leftarrow \overline{CY}$	-	-	X	-	R	0	1	1	4	
SCF	0 0 1 1 0 1 1 1	37	CY←1	-	-	R	-	R	S	1	1	4	
NOP	0 0 0 0 0 0 0 0	00	No operation	-	-	-	-	-	-	1	1	4	
HALT	0 1 1 1 0 1 1 0	76	CPU halted	-	-	-	-	-	-	1	1	4	
DI*	1 1 1 1 0 0 1 1	F3	IFF←0	-	-	-	-	-	-	1	1	4	
EI*	1 1 1 1 1 0 1 1	FB	IFF←1	-	-	-	-	-	-	1	1	4	
IM 0	1 1 1 0 1 1 0 1 0 1 0 0 0 1 1 0	ED 46	Set interrupt mode 0	-	-	-	-	-	-	2	2	8	
IM 1	1 1 1 0 1 1 0 1 0 1 0 1 0 1 1 0	ED 56	Set interrupt mode 1	-	-	-	-	-	-	2	2	8	
IM 2	1 1 1 0 1 1 0 1 0 1 0 1 1 1 1 0	ED 5E	Set interrupt mode 2	-	-	-	-	-	-	2	2	8	

Notes: IFF indicates the interrupt enable flip-flop
CY indicates the carry flip-flop.

Flag Notation: - = flag not affected, R = flag reset, S = flag set, X = flag is unknown,
O = flag is affected according to the result of the operation.

* Interrupts are not sampled at the end of EI or DI

16-BIT ARITHMETIC GROUP

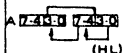
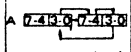
Mnemonic	Instruction Code $D_7D_6D_5D_4D_3D_2D_1D_0$	Hex	Operation	Flags S	Z	H	P/V	N	C	No. of Bytes	No. of M Cycles	No. of T States	Comments
ADD HL,ss	0 0 s s 1 0 0 1		HL←HL+ss	-	-	X	-	R	C	1	3	11	ss Reg.
ADC HL,ss	1 1 1 0 1 1 0 1 0 1 s s 1 0 1 0	ED	HL←HL+ss+CY	O	O	X	V	R	O	2	4	15	00 BC 01 DE
SBC HL,ss	1 1 1 0 1 1 0 1 0 1 s s 0 0 1 0	ED	HL←HL-ss-CY	O	O	X	V	S	O	2	4	15	10 HL 11 SP
ADDIX,pp	1 1 0 1 1 1 0 1 1 1 p p 1 0 0 1	DD	IX←IX+pp	-	-	X	-	R	O	2	4	15	pp Reg. 00 BC 01 DE 10 IX 11 SP
ADDIY,rr	1 1 1 1 1 1 0 1 0 0 r r 1 0 0 1	FD	IY←IY+rr	-	-	X	-	R	O	2	4	15	rr Reg. 00 BC 01 DE 10 IY 11 SP
INCss	0 0 s s 0 0 1 1		ss←ss+1	-	-	-	-	-	-	1	1	6	
INCIX	1 1 0 1 1 1 0 1 0 0 1 0 0 0 1 1	DD 23	IX←IX+1	-	-	-	-	-	-	2	2	10	
INCIY	1 1 1 1 1 1 0 1 0 0 1 0 0 0 1 1	FD 23	IY←IY+1	-	-	-	-	-	-	2	2	10	
DECss	0 0 s s 1 0 1 1		ss←ss-1	-	-	-	-	-	-	2	2	6	
DECIX	1 1 0 1 1 1 0 1 0 0 1 0 1 0 1 1	DD 2B	IX←IX-1	-	-	-	-	-	-	2	2	10	
DECIY	1 1 1 1 1 1 0 1 0 0 1 0 1 0 1 1	FD 2B	IY←IY-1	-	-	-	-	-	-	2	2	10	

Notes: ss is any of the register pairs BC, DE, HL, SP
pp is any of the register pairs BC, DE, IX, SP
rr is any of the register pairs BC, DE, IY, SP.

Flag Notation: - = flag not affected, R = flag reset, S = flag set, X = flag is unknown.
O = flag is affected according to the result of the operation.

ROTATE AND SHIFT GROUP

Mnemonic	Instruction Code $D_7D_6D_5D_4D_3D_2D_1D_0$	Hex	Operation	Flags S	Z	H	P/V	N	C	No. of Bytes	No. of M Cycles	No. of T States	Comments
RLCA	0 0 0 0 0 1 1 1	07	CY ← 7 ← 0 ← A	-	-	R	-	R	0	1	1	4	•Rotate left circular accumulator •Rotate left accumulator •Rotate right circular accumulator •Rotate right accumulator •Rotate left circular register r r Reg. 000 B 001 C 010 D 011 E 100 H 101 L 111 A
RLA	0 0 0 1 0 1 1 1	17	CY ← 7 ← 0 ← A	-	-	R	-	R	0	1	1	4	
RRCA	0 0 0 0 1 1 1 1	0F	7 → 0 → CY, A	-	-	R	-	R	0	1	1	4	
RRA	0 0 0 1 1 1 1 1	1F	7 → 0 → CY ← A	-	-	R	-	R	0	1	1	4	
RLCr	1 1 0 0 1 0 1 1 0 0 0 0 0 — r —	CB	CY ← 7 ← 0 r, (HL), (IX+d), (IY+d)	0	0	R	P	R	0	2	2	8	
RLC(HL)	1 1 0 0 1 0 1 1 0 0 0 0 0 1 1 0	CB		0	0	R	P	R	0	2	4	15	
RLC(IX+d)	1 1 0 1 1 1 0 1 1 1 0 0 1 0 1 1 — d — 0 0 0 0 0 1 1 0	DD CB		0	0	R	P	R	0	4	6	23	
RLC(IY+d)	1 1 1 1 1 1 0 1 1 1 0 0 1 0 1 1 — d — 0 0 0 0 0 0 0 0	FD CB		0	0	R	P	R	0	4	6	23	
RLs	0 1 0		CY ← 7 ← 0 s≡r, (HL), (IX+d), (IY+d)	0	0	R	P	R	0				Instruction format and states are as shown for RLC's. To form new Op-Code replace 000 of RLC's with shown code.
RRCs	0 0 1		7 → 0 → CY s≡r, (HL), (IX+d), (IY+d)	0	0	R	P	R	0				
RRs	0 1 1		7 → 0 → CY s≡r, (HL), (IX+d), (IY+d)	0	0	R	P	R	0				
SLAs	1 0 0		CY ← 7 ← 0 ← 0 s≡r, (HL), (IX+D), (IY+d)	0	0	R	P	R	0				
SRAs	1 0 1		7 → 0 → CY s≡r, (HL), (IX+D), (IY+d)	0	0	R	P	R	0				
SRLs	1 1 1		0 → 7 → 0 → CY s≡r, (HL), (IX+d), (IY+d)	0	0	R	P	R	0				

Mnemonic	Instruction Code $D_7D_6D_5D_4D_3D_2D_1D_0$	Hex	Operation	Flags S	Z	H	$P_{/V}$	N	C	No. of Bytes	No. of M Cycles	No. of T States	Comments
RLD	1 1 1 0 1 1 0 1 0 1 1 0 1 1 1 1	ED 6F		0	0	R	P	R	-	2	5	18	Rotate digit left & right between the accumulator and location (HL). The content of the upper half of the accumulator is unaffected.
RRD	1 1 1 0 1 1 0 1 0 1 1 0 0 1 1 1	ED 67		0	0	R	P	R	-	2	5	18	

Flag Notation: - = flag not affected, R = flag reset, S = flag set,
O = flag is affected according to the result of the operation.

BIT SET, RESET AND TEST GROUP

Mnemonic	Instruction Code $D_7D_6D_5D_4D_3D_2D_1D_0$	Hex	Operation	Flags S	Z	H	P/V	N	C	No. of Bytes	No. of M Cycles	No. of T States	Comments
BIT b,r	1 1 0 0 1 0 1 1 0 1 ←b→ ←r→	CB	$Z \leftarrow \overline{rb}$	X	O	S	X	R	-	2	2	8	r | Reg. 000 | B 001 | C 010 | D 011 | E 100 | H 101 | L 111 | A b | Bit Tested 000 | 0 001 | 1 010 | 2 011 | 3 100 | 4 101 | 5 110 | 6 111 | 7
BIT b,(HL)	1 1 0 0 1 0 1 1 0 1 ←b→ 1 1 0	CB	$Z \leftarrow \overline{(HL)_b}$	X	O	S	X	R	-	2	3	12	
BIT b,(IX+d)b	1 1 0 1 1 1 0 1 1 1 0 0 1 0 1 1 ←d→ 0 1 ←b→ 1 1 0	DD CB	$Z \leftarrow \overline{(IX+d)_b}$	X	O	S	X	R	-	4	5	20	
BIT b,(IY+d)b	1 1 1 1 1 1 0 1 1 1 0 0 1 0 1 1 ←d→ 0 1 ←b→ 1 1 0	FD CB	$Z \leftarrow \overline{(IY+d)_b}$	X	O	S	X	R	-	4	5	20	
SET b,r	1 1 0 0 1 0 1 1 1 1 ←b→ ←r→	CB	$r_b \leftarrow 1$	-	-	-	-	-	-	2	2	8	
SET b,(HL)	1 1 0 0 1 0 1 1 1 1 ←b→ 1 1 0	CB	$(HL)_b \leftarrow 1$	-	-	-	-	-	-	2	4	15	
SET b,(IX+d)	1 1 0 1 1 1 0 1 1 1 0 0 1 0 1 1 ←d→ 1 1 ←b→ 1 1 0	DD CB	$(IX+d)_b \leftarrow 1$	-	-	-	-	-	-	4	6	23	
SET b,(IY+d)	1 1 1 1 1 1 0 1 1 1 0 0 1 0 1 1 ←d→ 1 1 ←b→ 1 1 0	FD CB	$(IY+d)_b \leftarrow 1$	-	-	-	-	-	-	4	6	23	
RES b,s	1 0		$s_b \leftarrow 0$ s≡r (HL), (IX+d), (IY+d)	-	-	-	-	-	-				To form new Op Code replace 11 of SET b,s with 10. Flags and time states for SET instruction

Notes: The notation s_b indicates bit b (0 to 7) or location s.

Flag Notation: - = flag not affected, R = flag reset, S = flag set, X = flag is unknown,
O = flag is affected according to the result of the operation.

JUMP GROUP

Mnemonic	Instruction Code $D_7D_6D_5D_4D_3D_2D_1D_0$	Hex	Operation	Flags S	Z	H	P/V	N	C	No. of Bytes	No. of M Cycles	No. of T States	Comments
JPnn	1 1 0 0 0 0 1 1 ←——n——→ ←——n——→	C3	PC←nn	-	-	-	-	-	-	3	3	10	
JPcc,nn	1 1 C C 0 1 0 ←——n——→ ←——n——→		If condition cc is true PC←nn, otherwise continue	-	-	-	-	-	-	3	3	10	cc: 000 NZ non zero; 001 Z zero; 010 NC non carry; 011 C carry; 100 PO parity odd; 101 PE parity even; 110 P sign positive; 111 M sign negative
JRe	0 0 0 1 1 0 0 0 ←——e-2——→	18	PC←PC+e	-	-	-	-	-	-	2	3	12	
JR C,e	0 0 1 1 1 0 0 0 ←——e-2——→	38	If C=0, continue If C=1, PC←PC+e	-	-	-	-	-	-	2 2	2 3	7 12	If condition not met If condition is met
JR NC,e	0 0 1 1 0 0 0 0 ←——e-2——→	30	If C=1, continue If C=0, PC←PC+e	-	-	-	-	-	-	2 2	2 3	7 12	If condition not met If condition is met
JR Z,e	0 0 1 0 1 0 0 0 ←——e-2——→	38	If Z=0, continue If Z=1, PC←PC+e	-	-	-	-	-	-	2 2	2 3	7 12	If condition not met If condition is met
JR NZ,e	0 0 1 0 0 0 0 0 ←——e-2——→	20	If Z=1, continue If Z=0, PC←PC+e	-	-	-	-	-	-	2 2	2 3	7 12	If condition not met If condition is met
JP(HL)	1 1 1 0 1 0 0 1	E9	PC←HL	-	-	-	-	-	-	1	1	4	
JP(IX)	1 1 0 1 1 1 0 1 1 1 1 0 1 0 0 1	DD E9	PC←IX	-	-	-	-	-	-	2	2	8	
JP(IY)	1 1 1 1 1 1 0 1 1 1 1 0 1 0 0 1	FD E9	PC←IY	-	-	-	-	-	-	2	2	8	
DJNZ,e	0 0 0 1 0 0 0 0 ←——e-2——→	10	B←B-1 If B=0, continue If B≠0, PC←PC+e	-	-	-	-	-	-	2 2	2 3	8 13	If B=0 If B≠0

Notes: e represents the extension in the relative addressing mode. e is a signed two's complement number in the range <-126,129>. e-2 in the op-code provides an effective address of pc+e as PC is incremented by 2 prior to the addition of e.

Flag Notation: - = flag not affected, R = flag reset, S = flag set,
0 = flag is affected according to the result of the operation.

CALL AND RETURN GROUP

Mnemonic	Instruction Code $D_7D_6D_5D_4D_3D_2D_1D_0$	Hex	Operation	Flags S	Z	H	P/V	N	C	No. of Bytes	No. of M Cycles	No. of T States	Comments
CALLnn	1 1 0 0 1 1 0 1 ← n → ← n →	CD	(SP-1)←PC_H (SP-2)←PC_L PC←nn	-	-	-	-	-	-	3	5	17	
CALLcc,nn	1 1 c c 1 0 0 ← n → ← n →		If condition cc is false continue, otherwise same is CALLnn	-	-	-	-	-	-	3 3	3 5	10 17	If cc is false If cc is true
RET	1 1 0 0 1 0 0 1	C9	PC_L←(SP) PC_H←(SP+1)	-	-	-	-	-	-	1	3	10	
RETcc	1 1 c c 0 0 0		If condition cc is false continue, otherwise same as RET	-	-	-	-	-	-	1 1	1 3	5 11	If cc is false If cc is true
RETI	1 1 0 1 1 0 1 0 1 0 0 1 1 0 1	ED 4D	Return from interrupt	-	-	-	-	-	-	2	4	14	
RETN*	1 1 1 0 1 1 0 1 0 1 0 0 0 1 0 1	ED 45	Return from non maskable interrupt	-	-	-	-	-	-	2	4	14	
RSTp	1 1 ← t → 1 1 1		(SP-1)←PC_H (SP-2)←PC_L PC_H←0 PC_L←p	-	-	-	-	-	-	1	3	11	

cc	Condition
000	NZ non zero
001	Z zero
010	NC non carry
011	C carry
100	PO parity odd
101	PE parity even
110	P sign positive
111	M sign negative

t	p
000	00H
001	08H
010	10H
011	18H
100	20H
101	28H
110	30H
111	38H

* RETN loads $IFF_2 \rightarrow IFF_1$

Flag Notation: - = flag not affected, R = flag reset, S = flag set,
0 = flag is affected according to the result of the operation.

INPUT AND OUTPUT GROUP

Mnemonic	Instruction Code $D_7D_6D_5D_4D_3D_2D_1D_0$	Hex	Operation	Flags S	Z	H	P/V	N	C	No. of Bytes	No. of M Cycles	No. of T States	Comments
IN A,(n)	1 1 0 1 1 0 1 1 n	DB	A←(n)	-	-	-	-	-	-	2	3	11	n to $A_0 \sim A_7$ Acc to $A_8 \sim A_{15}$
INr,(C)	1 1 1 0 1 1 0 1 0 1 r 0 0 0	ED	r←(C) If r=110 only the flags will be affected	0	0	0	P	R	-	2	3	12	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
INI	1 1 1 0 1 1 0 1 1 0 1 0 0 0 1 0	ED A2	(HL)←(C) B←B-1 HL←HL+1	X	①	X	X	S	X	2	4	16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
INIR	1 1 1 0 1 1 0 1 1 0 1 1 0 0 1 0	ED B2	(HL)←(C) B←B-1 HL←HL+1 Repeat until B=0	X	1	X	X	S	X	2 2	5 (If B≠0) 4 (If B=0)	21 16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
IND	1 1 1 0 1 1 0 1 1 0 1 0 1 0 1 0	ED AA	(HL)←(C) B←B-1 HL←HL-1	X	①	X	X	S	X	2	4	16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
INDR	1 1 1 0 1 1 0 1 1 0 1 1 1 0 1 0	ED BA	(HL)←(C) B←B-1 HL←HL-1 Repeat until B=0	X	1	X	X	S	X	2 2	5 (If B≠0) 4 (If B=0)	21 16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
OUT(n),A	1 1 0 1 0 0 1 1	D3	(n)←A	-	-	-	-	-	-	2	3	11	n to $A_0 \sim A_7$ Acc to $A_8 \sim A_{15}$
OUT(C),r	1 1 1 0 1 1 0 1 0 1 r 0 0 1	ED	(C)←r	-	-	-	-	-	-	2	3	12	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
OUTI	1 1 1 0 1 1 0 1 1 0 1 0 0 0 1 1	ED A3	B←B-1 (C)←(HL) HL←HL+1	-	①	-	-	S	X	2	4	16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
OTIR	1 1 1 0 1 1 0 1 1 0 1 1 0 0 1 1	ED B3	B←B-1 (C)←(HL) HL←HL+1 Repeat until B=0	X	1	X	X	S	X	2 2	5 (If B≠0) 4 (If B=0)	21 16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
OUTD	1 1 1 0 1 1 0 1 1 0 1 0 1 0 1 1	ED AB	(C)←(HL) B←B-1 HL←HL-1	X	①	X	X	S	X	2	4	16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$
OTDR	1 1 1 0 1 1 0 1 1 0 1 1 1 0 1 1	ED BB	(C)←(HL) B←B-1 HL←HL-1 Repeat until B=0	X	1	X	X	S	X	2 2	5 (If B≠0) 4 (If B=0)	21 16	C to $A_0 \sim A_7$ B to $A_8 \sim A_{15}$

Notes: ① If the result of B-1 is zero the Z flag is set, otherwise it is reset.

Flag Notation: - = flag not affected, R = flag reset, S = flag set, X = flag is unknown,
0 = flag is affected according to the result of the operation.

4. ELECTRICAL CARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
VCC	Vcc Supply Voltage with respect to Vss	-0.5V to 7V
VIN	Input Voltage	-0.5V to VCC + 0.5V
PD	Power Dissipation (TA=85°C)	250mW
TSOLDER	Soldering Temperature (Soldering Time 10 sec)	260°C
TSTG	Storage Temperature	-65°C to 150°C
TOPR	Operating Temperature	-40°C to 85°C

4.2 DC CHARACTERISTICS

TA=-40°C to 85°C, VCC=5V±10%, VSS=0V

SYMBOL	PAREMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
VILC	Clock Input Low Voltage			-0.3	-	0.6	V
VIHC	Clock Input High Voltage			VCC-0.6	-	VCC+0.3	V
VIL	Input Low Voltage (except CLK)			-0.5	-	0.8	V
VIH	Input High Voltage (except CLK)			2.2	-	VCC	V
VOL	Output Low Voltage	IOL=2.0mA		-	-	0.4	V
VOH1	Output High Voltage 1	IOH=-1.6mA		2.4	-	-	V
VOH2	Output High Voltage 2	IOH=-250uA		VCC-0.8	-	-	V
ILI	Input Leakage Current	Vss≦VIN≦Vcc		-	-	±10	uA
ILO	3-state Output Leakage Current in Float	Vss+0.4≦Vout ≦VCC		-	-	±10	uA
ICC1	Power Supply Current	Vcc=5V, fCLK=(1) VIH=VCC-0.2V VIL=0.2V	AP/AF	-	9	15	mA
			AP-6 /AF-6	-	15	22	
			AP-8	-	20	25	
ICC2 (2)	Stand-by Supply Current	VCC=5V, CLK=(2) VIL=VCC-0.2V VIH=0.2V			0.5	10	uA

Note (1) fCLK = 1/TcC (MIN)

(2) IcC2 Stand-by Supply Current is guaranteed only when the supplied clock is stopped at a low level during T4 state of the following machine Cycle (M1) next to OP code fetch Cycle of HALT instruction.

4.3 AC CHARCTERISTICS

TA=-40°C to 85°C, VCC = 5VV±10%, Vss = 0V, Unless otherwise noted. (1)

NO.	SYMBOL	PARAMETER	4MHz 00AP/AF		6MHz AP-6/AF-6		8MHz AP-8		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
1	TcC	Clock Cycle Time	250	DC	165	DC	125	DC	ns
2	TwCh	Clock Pulse Width (HIGH)	110	DC	65	DC	55	DC	ns
3	TwCl	Clock Pulse Width (LOW)	110	DC	65	DC	55	DC	ns
4	TfC	Clock Fall Time	-	30	-	20	-	10	ns
5	TrC	Clock Rise Time	-	30	-	20	-	10	ns
6	TdCr(A)	Clock to Address Valid Delay	-	110	-	90	-	80	ns
7	TdA (MREQf)	Address Valid to MREQ Delay	65	-	35	-	20	-	ns
8	TdCf (MREQf)	Clock to MREQ Delay	-	85	-	70	-	60	ns
9	TdCr (MREQf)	Clock to MREQ Delay	-	85	-	70	-	60	ns
10	TwMREQh	MREQ Pulse Width (High)	110	-	65	-	45	-	ns
11	TwMREQl	MREQ Pulse Width (Low)	220	-	135	-	100	-	ns
12	TdCf (MREQr)	Clock to MREQ Delay	-	85	-	70	-	60	ns
13	TdCf(RDf)	Clock to RD Delay	-	95	-	80	-	70	ns
14	TdCr(RDr)	Clock to RD Delay	-	85	-	70	-	60	ns
15	TsD(Cr)	Data Setup Time to Clock	35	-	30	-	30	-	ns
16	ThD(RDr)	Data Hold Time to RD	0	-	0	-	0	-	ns
17	TsWAIT (Cf)	WAIT Setup Time to Clock	70	-	60	-	50	-	ns
*18	ThWAIT (Cf)	WAIT Hold Time after Clock	10	-	10	-	10	-	ns
19	TdCr(M1f)	Clock to M1 Delay	-	100	-	80	-	70	ns
20	TdCr(M1r)	Clock to M1 Delay	-	100	-	80	-	70	ns
21	TdCr (RFSHf)	Clock to RFSH Delay	-	130	-	110	-	95	ns
22	TdCr (RFSHr)	Clock to RFSH Delay	-	120	-	100	-	85	ns
23	TdCf(RDr)	Clock to RD Delay	-	85	-	70	-	60	ns
24	TdCf(RDf)	Clock to RD Delay	-	85	-	70	-	60	ns
25	TsD(Cf)	Data Setup to Clock during M2,M3,M4, or M5 Cycles	50	-	40	-	30	-	ns
26	TdA (IORQf)	Address Stable prior IORQ	180	-	110	-	75	-	ns
27	TdCr (IORQf)	Clock to IORQ Delay	-	75	-	65	-	55	ns
28	TdCf (IORQr)	Clock to IORQ Delay	-	85	-	70	-	60	ns
29	TdD(WRf)	Data Stable prior to WR	80	-	25	-	5	-	ns
30	TdDf(WRf)	Clock to WR Delay	-	80	-	70	-	60	ns
31	TwWR	WR Pulse Width	220	-	135	-	100	-	ns
32	TdCf(WRr)	Clock to WR Delay	-	80	-	70	-	60	ns

NO.	SYMBOL	PARAMETER	4NHz 00AP/AF		6MHz AP-6/AF-6		8MHz AP-8		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
33	TdD(WRf)	Data Stable prior to WR ↓	-10	-	-55	-	-55	-	ns
34	TdCr(WRf)	Clock ↑ to WR ↓ Delay	-	65	-	60	-	55	ns
35	TdWRr(D)	Data Stable from WR ↑	60	-	30	-	15	-	ns
36	TdCf (HALT)	Clock ↓ to HALT ↑ or ↓	-	300	-	260	-	225	ns
37	TwNMI	NMI Pulse Width	80	-	70	-	60	-	ns
38	TsBUSREQ (Cr)	BUSREQ Setup Time to Clock ↑	50	-	50	-	40	-	ns
*39	ThBUSREQ (Cr)	BUSREQ Hold Time after Clock ↑	10	-	10	-	10	-	ns
40	TdCr (BUSACKf)	Clock ↑ to BUSACK ↓ Delay Clock	-	100	-	90	-	80	ns
41	TdCf (BUSACKr)	Clock ↓ to BUSACK ↑ Delay Clock	-	100	-	90	-	80	ns
42	TdCr(Dz)	Clock ↑ to Data Float Delay	-	90	-	80	-	70	ns
43	TdCf(CTz)	Clock ↑ to Control Outputs Float Delay (MREQ,RD,and WR)	-	80	-	70	-	60	ns
44	TdCr(Az)	Clock ↑ to Data Float Delay	-	90	-	80	-	70	ns
45	TdCTr(A)	MREQ ↑ ,IORQ ↑ ,RD ↑ , and WR ↑ to Address Hold Time	80	-	35	-	20	-	ns
46	TsRESET (Cr)	RESET to Clock ↑ Setup Time	60	-	60	-	45	-	ns
*47	ThRESET (Cr)	RESET to Clock ↑ Hold Time	10	-	10	-	10	-	ns
48	TsINTf (Cr)	INT to Clock ↑ Setup Time	80	-	70	-	55	-	ns
*49	ThINTr (Cr)	INT to Clock ↑ Hold Time	10	-	10	-	10	-	ns
50	TdM1f (IORQf)	M1 ↓ to IORQ ↓ Delay	565	-	365	-	270	-	ns
51	TdCf (IORQf)	Clock ↓ to IORQ ↑ Delay	-	85	-	70	-	60	ns
52	TdCf (IORQr)	Clock ↑ to IORQ ↑ Delay	-	85	-	70	-	60	ns
53	TdCf(D)	Clock ↓ to Data Valid Delay	-	150	-	130	-	115	ns

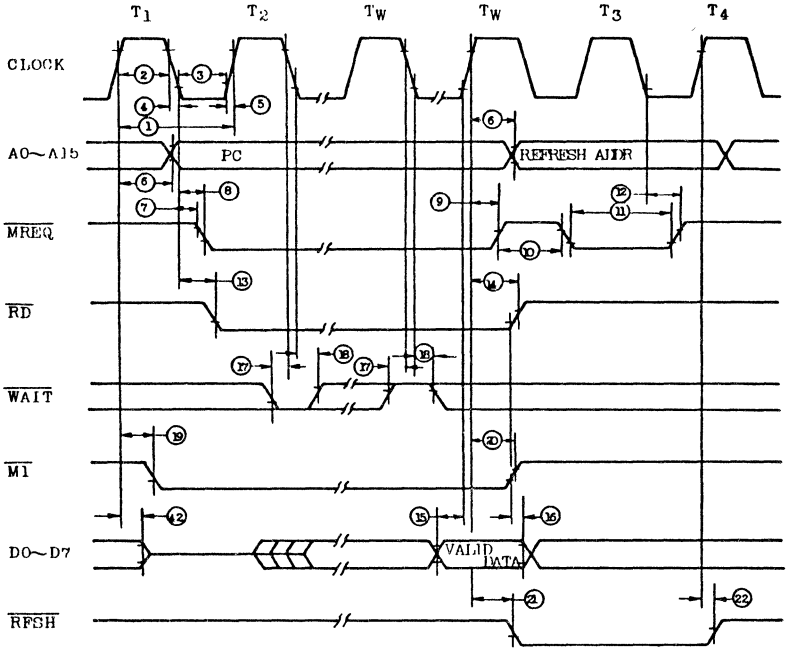
NOTE 1) Timing Measurements are made at the following voltage.
Input VIH=2.4V, VIL=0.4V, VIHC=VCC-0.6V, VILC=0.6V
Output VOH=2.2V, VOL=0.8V
CL=100pF

NOTE 2) The items attached * mark are not compatible with NMOS Z80 SPECS.

4.4 CAPACITANCE

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CCLOCK	Clock Input Capacitance	f=1MHz All terminals except that to be measured be earthed.	–	–	8	PF
CIN	Input Capacitance		–	–	6	
COUT	Output Capacitance		–	–	10	

4.5 TIMING WAVEFORMS



NOTE: TW-Wait cycle added when necessary for slow ancilliary devices.

FIGURE 17. INSTRUCTION OPCODE FETCH

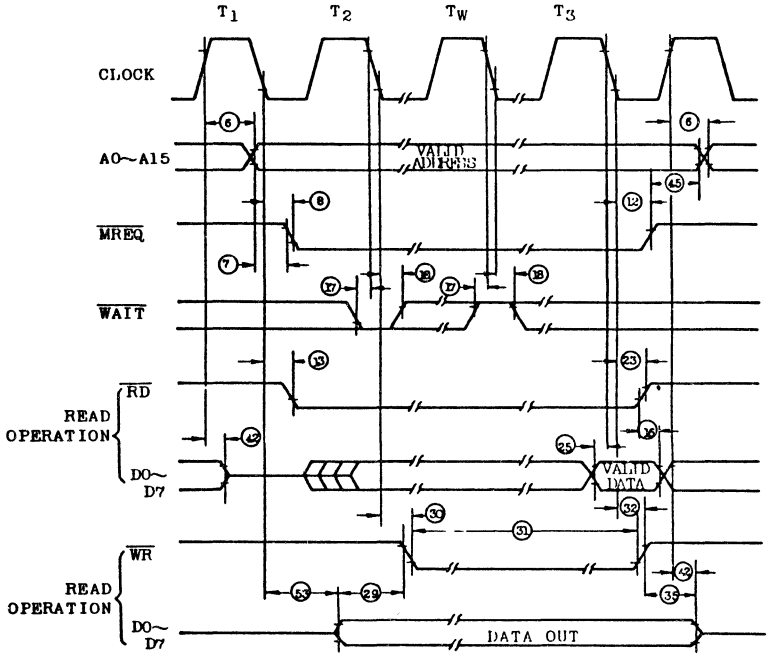
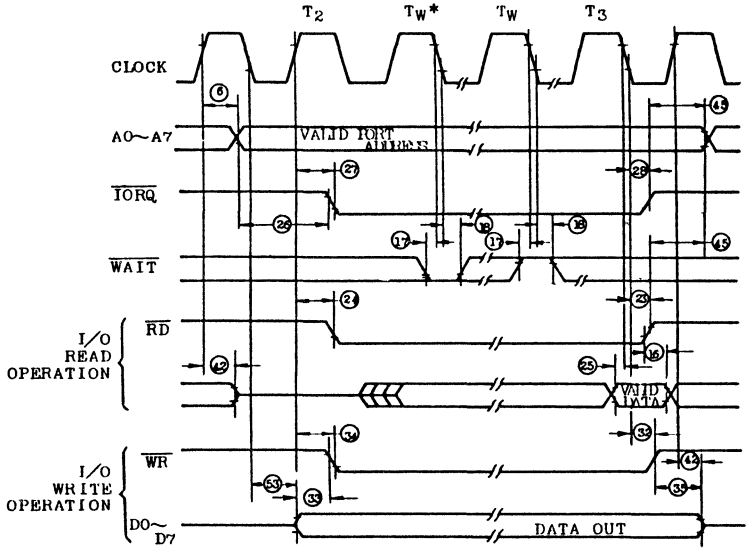
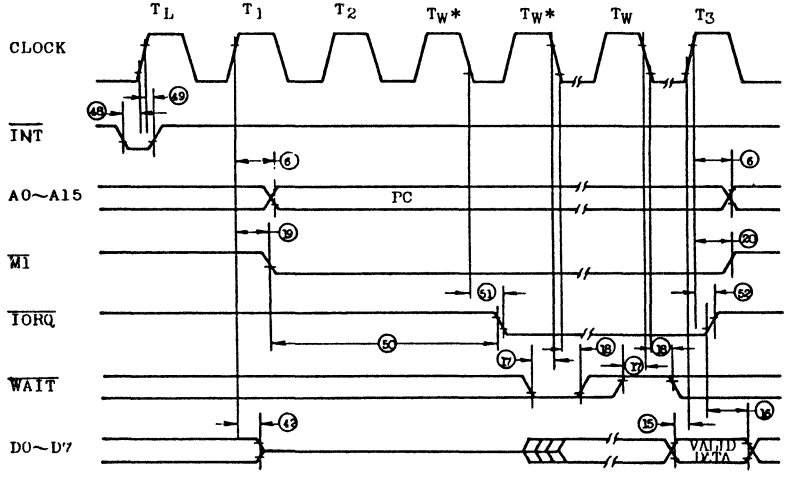


FIGURE 18. MEORY READ OR WRITE CYCLES



NOTE: TW = One Wait cycle automatically inserted by CPU.

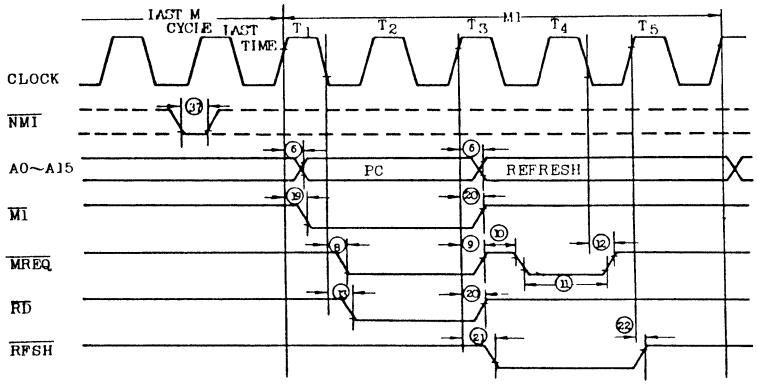
FIGURE 19. INPUT OR OUTPUT CYCLES



NOTE: 1) TL=Last state of previous instruction.

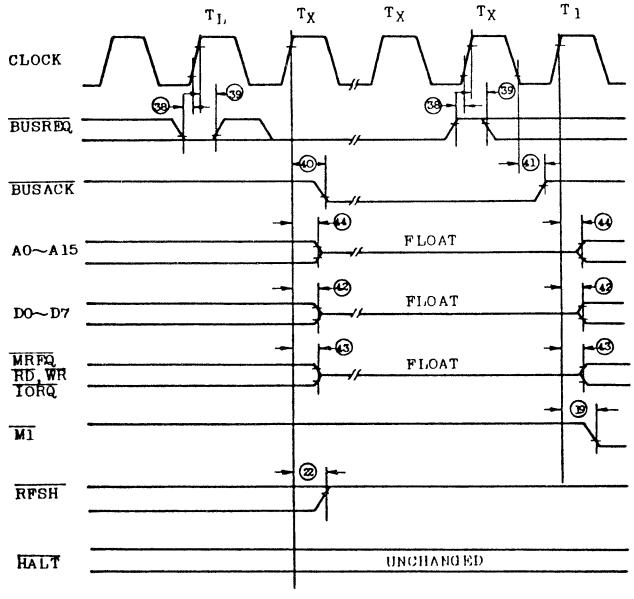
2) Two Wait cycles automatically inserted by CPU(*)

FIGURE 20. INTERRUPT REQUEST/ACKNOWLEDGE CYCLE



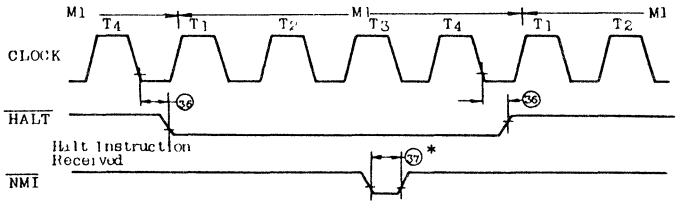
* Although NMI is an asychronous input, to guarantee its being recognized on the following machine cycle, NMI's falling edge must occur no later tha the rising edge of the clock cycle preceding TLAST.

FIGURE 21. NON-MASKABLE INTERRUPT REQUEST OPRATION



NOTE: TL=Last state of nay M cycle. TX=An arbitrary clock cycle used by requesting device.

FIGURE 22. BUS REQUEST/ACKNOWLEDGE CYCLE



NOTE: $\overline{INT}$ will also force a Halt exit.

* See note, Figure 19.

FIGURE 23. HALT ACKNOWLEDGE CYCLE

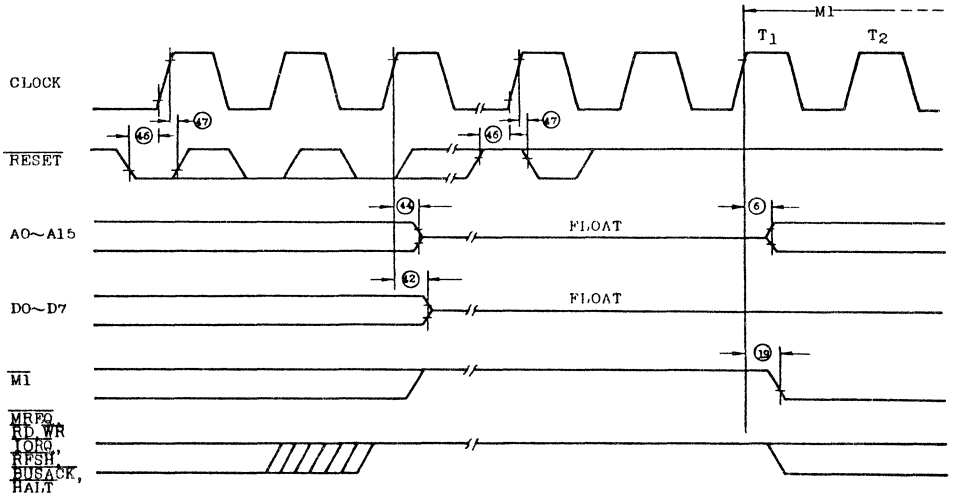
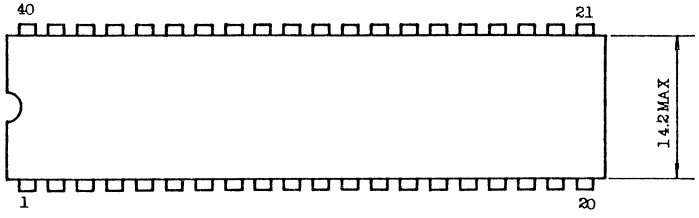
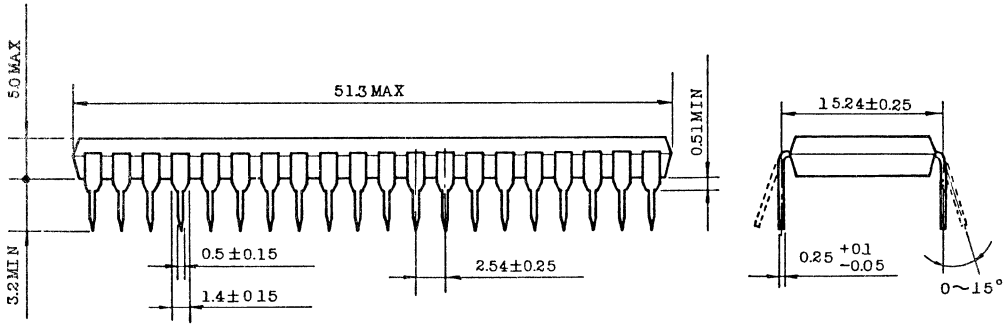


FIGURE 24. RESET CYCLE

5. OUTLINE DRAWING

5.1 Plastic Package



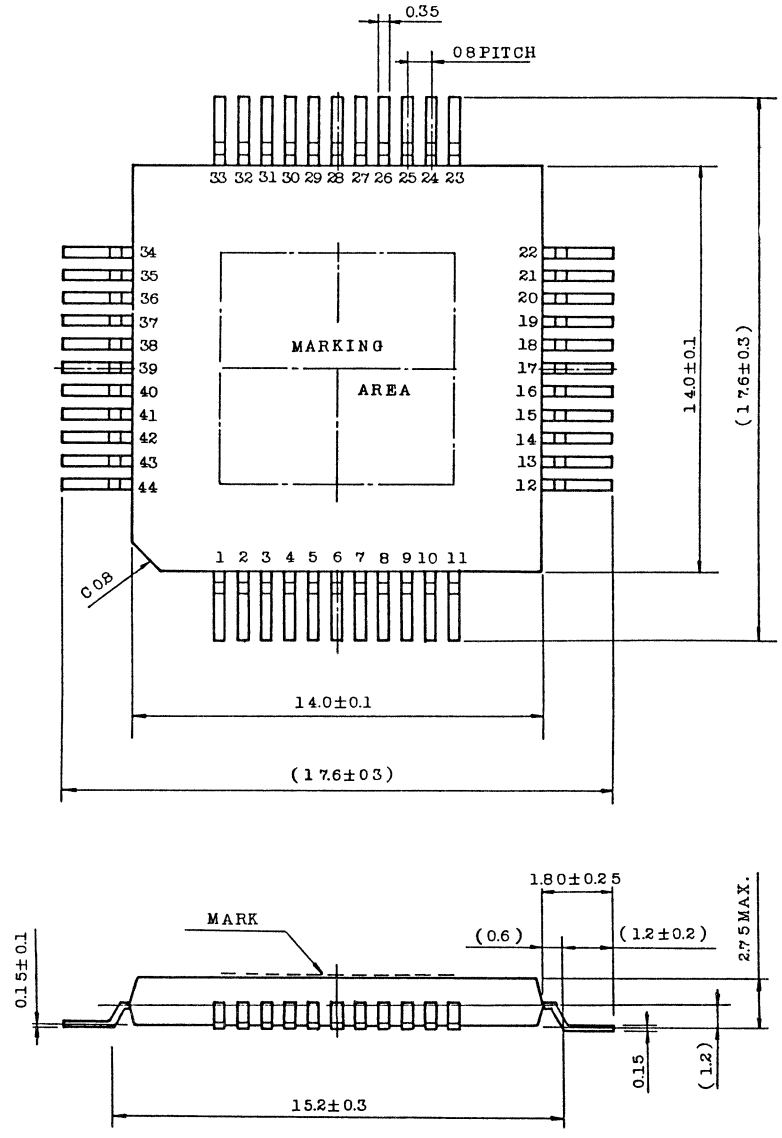


Note 1. This dimension is measured at the center of bending point of leads.

Note 2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoretical positions with respect to No.1 and No.40 leads.

5.2 Flat Package

Unit in mm



CMOS Z80 8-BIT MICROPROCESSOR

1. General Description and Features

The TMPZ84C01F if an 8-bit microprocessor (hereinafter referred to as MPU) with a built-in clock generator/controller, which provides low power operation and high performance.
Built into the TMPZ84C01F are a control function and clock generator for the standby function in addition to paired 6 general purpose registers, accumulator, flag registers, an arithmetic-and-logic unit, bus control, memory control and timing control circuits.
The TMPZ84C01F is fabricated using Toshiba's CMOS Silicon Gate Technology and molded in a 44-pin mini-flat package.

The principal functions and features of the TMPZ84C01F are as follows.

(1) Commands compatible with the Zilog Z80 MPU.
(2) Low power consumption
  15mA Typ (5V, 4MHz under RUN mode)
  1mA Typ (5V, 4MHz under IDLE1 mode)
  3mA Typ (5V, 4MHz under IDLE2 mode)
  0.5μA Typ (5V under STOP mode)
(3) DC to 4MHz operation (at 5V±10%)
(4) Single 5V power supply (at 5V±10%)
(5) Operating temperature (-40°C to 85°C)
(6) On-chip clock generator
(7) In the HALT state, the following 4 modes are selectable:
  - o RUN mode
  - o IDLE 1 mode
  - o IDLE 2 mode
  - o STOP mode

In the following explanation for the same content, IDLE1 Mode and IDLE2 Mode are referred to as IDLE1/2.

(8) Powerful set of 158 instructions available
(9) Powerful interrupt function
  (a) Non-maskable interrupt terminal ($\overline{NMI}$)
  (b) Maskable interrupt terminal ($\overline{INT}$)
  The following 3 modes are selectable:
  - o 8080 compatible interrupt mode (interrupt by Non-Z80 family peripheral LSI) (Mode 0)
  - o Restart interrupt (Mode 1)
  - o Daisy chain structure interrupt using Z-80 family peripheral LSI (Mode 2)

(10) An auxiliary register provided to each of general purpose registers.
(11) Two index registers
(12) 10 addressing modes
(13) Built-in refresh circuit for dynamic memory.
(14) Molded in 44-pin mini flat package

Further, in the following text and explanations for charts and tables, hexadecimal numbers are directly used without giving an identification to explanation of address, etc. to the extent not to cause confusions.

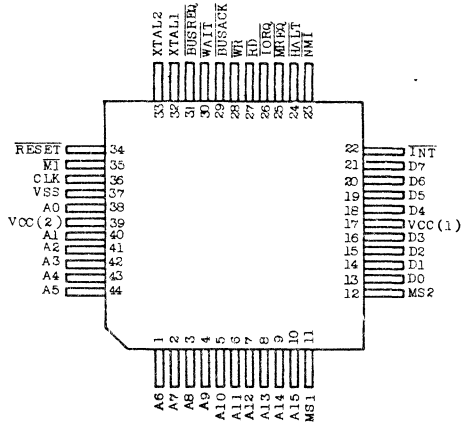
(Note) Z80(R) is a registered trademark of Zilog Inc., U.S.A.

2. Pin Connections and Pin Functions

The pin connections and I/O pin names and brief functions of the TMPZ84C01F are shown below.

2.1 Pin connections

The pin connections of the TMPZ84C01F are as shown in Fig. 2.1.



(Note) Connect Pin 39 and Pin 17 externally.

Fig. 2.1 Pin Connections (Top View)

2.2 Pin names and functions

I/O pin names and functions are as shown in Table 2.1.

Table 2.1 Pin Names and Functions

Pin Name	Number of Pin	Input/Output 3-state	Function
A0 - A15	16	Output 3-state	16-bit address bus. Specify addresses of memories and I/O to be accessed. During the refresh period, addresses for refreshing are output.
MS1, MS2	2	Input	Mode selection input. One of 4 modes (RUN, IDLE1/2, STOP) is selected according to the state of these 2 pins
D0 - D7	8	I/O 3-state	8-bit bidirectional data bus.
$\overline{INT}$	1	Input	Maskable interrupt request signal. Interrupt is generated by peripheral LSI. This signal is accepted if the interrupt enable flip-flop (IFF) is set at "1". $\overline{INT}$ is normally used on Wired-OR. In this case, a pull-up resistor is externally connected.

Pin Name	Number of Pin	Input/Output 3-state	Function
$\overline{NMI}$	1	Input	Non-maskable interrupt request signal. This interrupt request has the higher priority than the maskable interrupt request and does not rely upon the state of the interrupt enable flip-flop (IFF).
$\overline{HALT}$	1	Output	Halt signal. MPU execute HALT instruction and when the halt state is resulted, "0" is output.
$\overline{MREQ}$	1	Output 3-state	Memory request signal. When an effective address for memory access is on the address bus, "0" is output.
$\overline{IORQ}$	1	Output 3-state	I/O request signal. When addresses for I/O are on the lower 8 bits (A0 - A7) of the address bus in the I/O operation, "0" is output. In addition, $\overline{IORQ}$ signal is output together with $\overline{M1}$ signal at time of interrupt acknowledge cycle to inform peripheral LSI of the state that the interrupt response vector may be put on the data bus.
$\overline{RD}$	1	Output 3-state	Read signal "0" signal is output for a period when MPU can receive data from a memory or peripheral LSI. It is possible to put data from a specified peripheral LSI or mamory on the MPU data bus after gating by this signal.
$\overline{WR}$	1	Output 3-state	Write signal. This signal is output when data to be stored in a specified memory or peripheral LSI is on the MPU data bus.
$\overline{BUSACK}$	1	Output	Bus acknowledge signal. In response to $\overline{BUSREQ}$ signal, this signal informs a peripheral LSI of the fact that the address bus, data bus, $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$ signals have been placed in the high impedance state.
$\overline{WAIT}$	1	Input	Wait signal. $\overline{WAIT}$ signal is a signal to inform MPU of specified memory or peripheral LSI which is not ready for data transfer. As long as $\overline{WAIT}$ signal as at "0" level, MPU is continuously kept in the wait state.
$\overline{BUSREQ}$	1	Input	Bus request signal. $\overline{BUSREQ}$ signal is a signal requesting placement of the address bus, data bus, $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$ signals in the high impedance state. $\overline{BUSREQ}$ signal is normally used on wired-OR. In this case, a pull-up resistor is externally connected.

Pin Name	Number of Pin	Input/Output 3-state	Function
$\overline{\text{RESET}}$	1	Input	$\overline{\text{Reset}}$ signal. $\overline{\text{RESET}}$ signal is used for initialization MPU and must be kept in active state ("0") for a period of at least 3 clocks.
$\overline{\text{M1}}$	1	Output	Signal showing machine cycle 1. "0" is output together with $\overline{\text{MREQ}}$ signal in the operation code fetch sycle. This signal is output for every opcode fetch when 2 byte opcode is executed. In the maskable interrupt acknowledge cycle, this signal is output together with $\overline{\text{IORQ}}$ signal.
XTAL 1 (XIN) XTAL 2 (XOUT)	2	Input Output	Crystal oscillator connecting terminal
CLK	1	Output	Single-phase clock output. When the HALT instruction in STOP Mode is executed, MPU stops its operation and holds clock output at "0" level.
VCC (1), (2)	2	Power supply	+5V Connect 39 pin and 17 pin externally.
VSS	1	Power supply	0V

3. Functional Description

The system configuration, functions and basic operation of the TMPZ84C01F are described here.

3.1 Block diagram

The block diagram of the internal configuration is shown in Fig. 3.1.

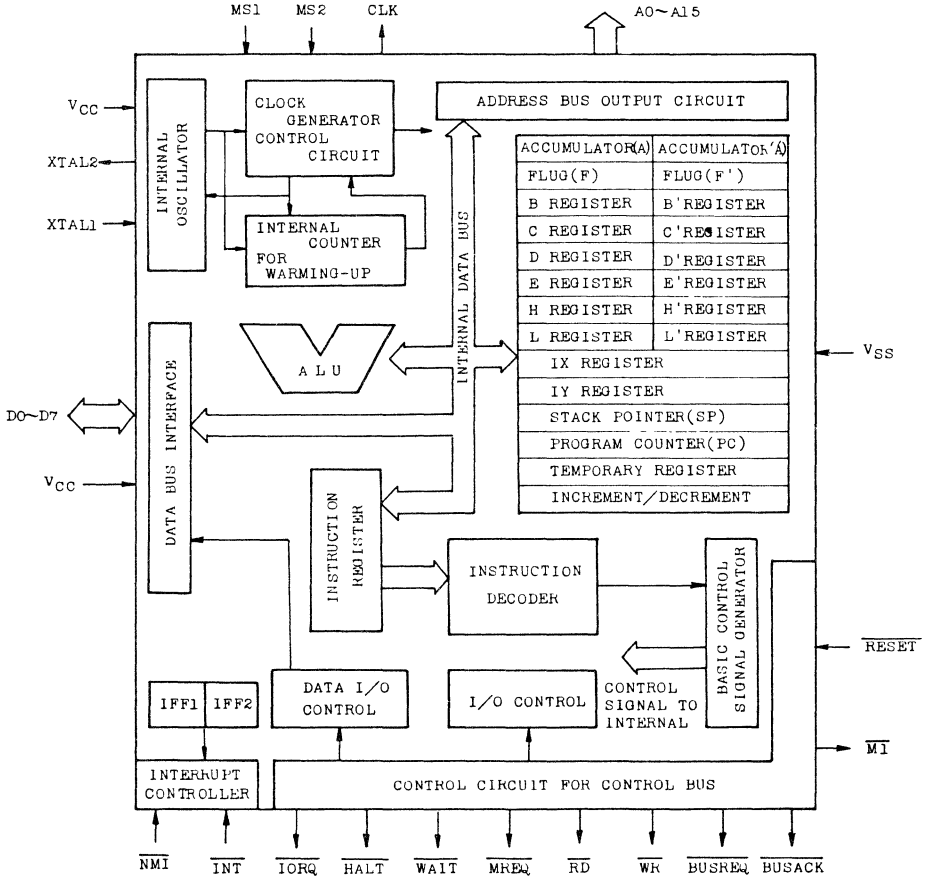


Fig. 3.1 Block Diagram

3.2 System configuration

The TMPZ84C01F has a built-in system clock generator for CMOS Z80 in addition to the standard functions of the TMPZ84C00P CMOS Z80 MPU.

The explanation is provided here with emphasis placed on the halt function relative to the clock generator, which is an additional function. The internal register group, reset and interrupt function are identical to those of the TMP84C00P. For details please refer to the data sheet for the TMPZ84C00P.

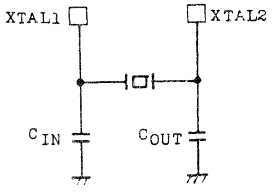
In this section, the following principal compoments and functions will be described.

(1) Generation of clock
(2) Operation mode
(3) Warming-up time at time of restart

3.2.1 Generating the system clock

The TMPZ84C01F has a built-in oscillation circuit and required clock can be easily generated by connecting an oscillator to the external terminals (XTAL1, XTAL2). Clock in the same frequency as input oscillation frequency is generated.

Examples of oscillator connection are shown in Fig. 3.2.



C_{IN}	C_{OUT}
22 pF	33 pF

Fig. 3.2 Examples of Oscillator Connection and Constant

3.2.2 Operation modes

There are 4 kinds of operations modes available for the TMPZ48C01F in connection with generation of clock; RUN Mode, IDLE1/2 Modes and STOP Mode. One of these modes is selected by the mode select inputs (MS1, MS2).

The operation mode is effective when the halt instruction is executed and when the halt instruction is not executed, clock is supplied continuously. Restart of MPU from the stopped state under IDLE1/2 Mode or STOP Mode is effected by inputting either RESET signal or interrupt signal (INT or NMI).

Operations of these modes in the halt state are shown in Table 3.1.

Table 3.1 Clock Generating Operation Modes

Operation Mode	MS1	MS2	Description at HALT State
RUN Mode	1	1	MPU continues the operation and supplies clock to the outside continuously.
IDLE1 Mode	0	0	The internal oscillator's operation only is continued and clock (CLK) output as well as internal operation are stopped at "0" level of T4 state in the halt instruction operation code fetch cycle.
IDLE2 Mode	0	1	The internal oscillator's operation and clock (CLK) output are continued but the internal operation are stopped at "0" level of T4 state in the halt instruction operation code fetch cycle.
STOP Mode	1	0	All operations of the internal oscillator, clock (CLK) output, and internal operation are stopped at "0" level of T4 state in the halt instruction operation code fetch cycle.

3.2.3 Warming-up time at time of restart (STOP Mode)

When MPU is released from the halt state by accpeting an interrupt request, MPU, then, will execute an interrupt service routine. Therefore, when an interruption request is accepted, MPU starts generation of internal system clock and clock output after a warming-up time by the internal counter (2**14+2.5) TcC (TcC: Clock Cycle) to obtain a stabilized oscillation for MPU operation.

Further, in case of the restart by $\overline{\text{RESET}}$ signal, the internal counter does not operate for a quick operation at time of power ON.

3.3 Status change flowchart and basic timing

In this section, the status change and basic timing when the TMPZ84C01F is operating are explained.

3.3.1 Status change flowchart

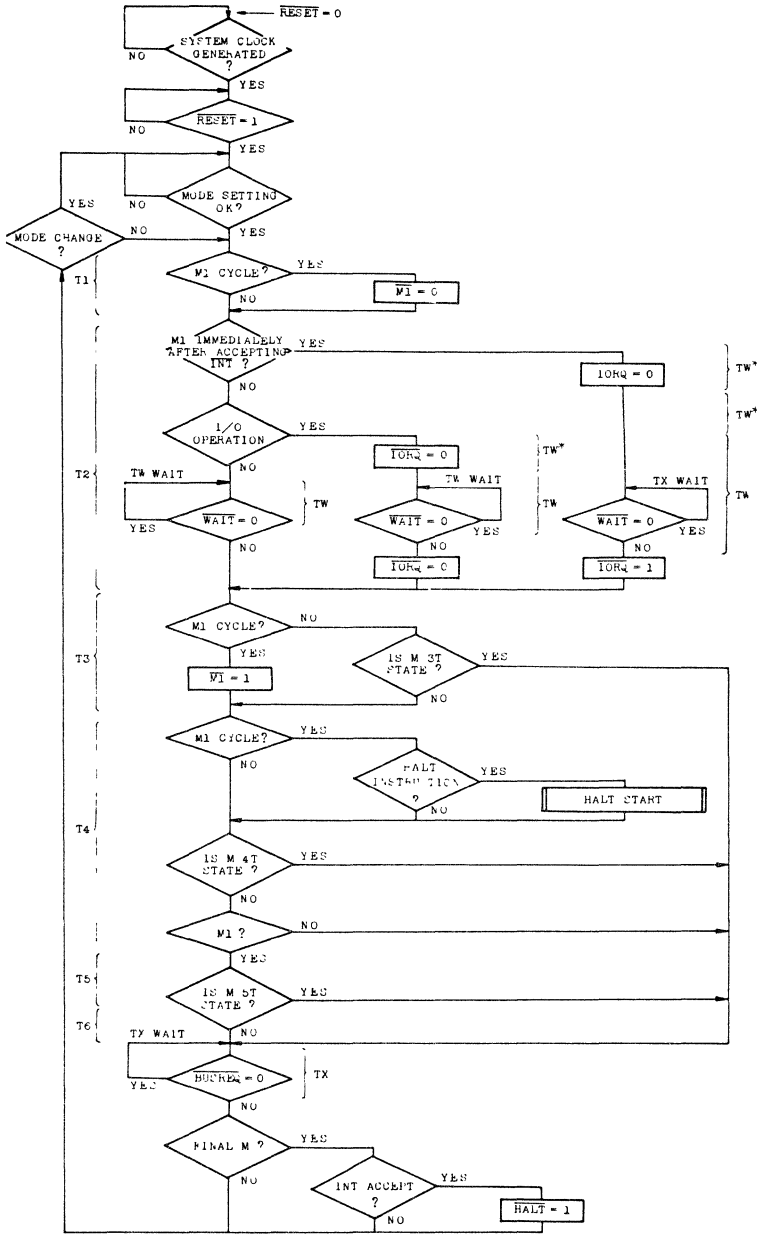


Fig. 3.3 (a) Status Change Flowchart

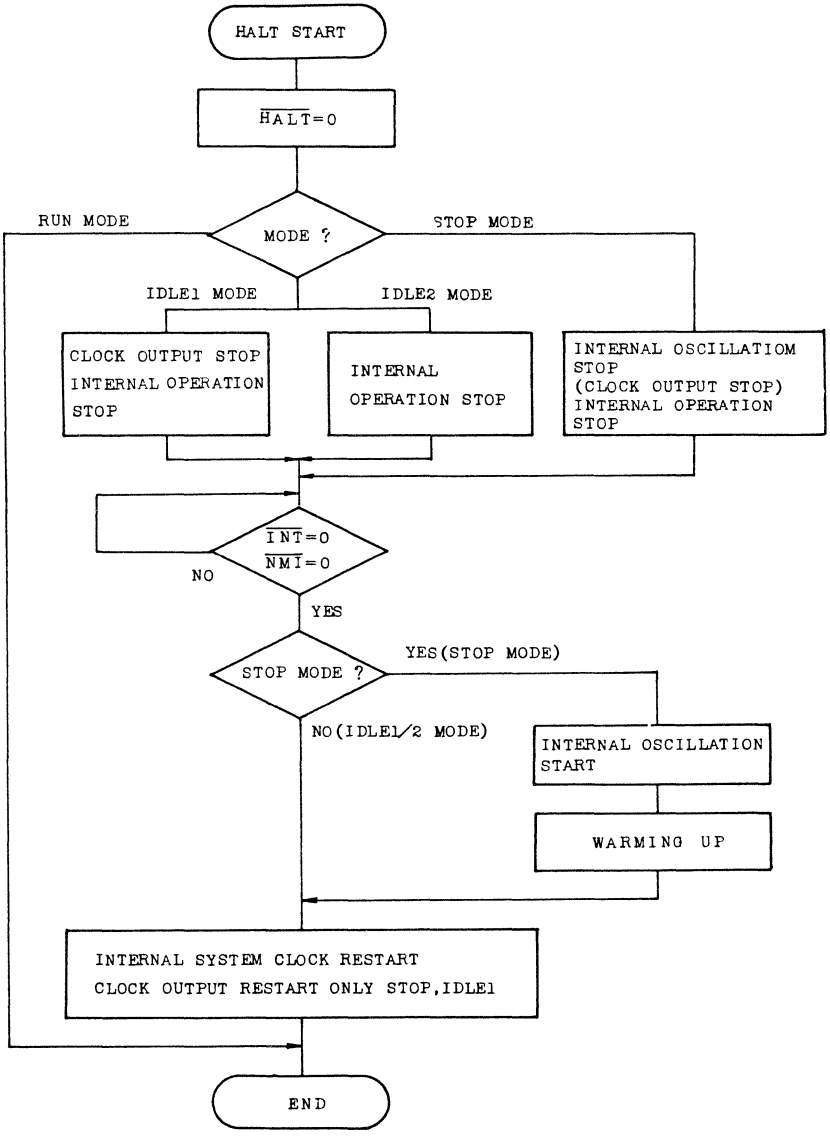


Fig. 3.3 (b) Status Change Flowchart

3.3.2 Basic timing

The basic timing is explained here with emphasis placed on the halt function relative to the clock generator. Except $\overline{RFSH}$ signal output, the following items are idnetical to those for the TMPZ84C00P. Refer to the data sheet for the TMPZ84C00P.

- o Operation code fetch cycle
- o Memory read/write operation
- o Input/output operation
- o Bus request/acknowledge operation
- o Maskable interrupt request accepting operation
- o Non-maskable interrupt request accepting operation
- o Reset operation

Note that the TMPZ84C01F does not have the refresh terminal ($\overline{RFSM}$) but refresh address is output on the address bus in the operation code fetch cycle ($\overline{M1}$) as in the TMPZ84C00P since the on-chip refresh control circuit is available.

(1) Operation when $\overline{HALT}$ instruction is execution

When MPU fetches a halt instruction in the operation code fetch cycle, $\overline{HALT}$ signal goes active (low level) in synchronous with falling edge of T4 state for the peripheral LSI and MPU stops the operation. The system clock generating operation after this differs depending upon the operation mode (RUN Mode, IDLE1/2 Mode or STOP Mode). If the internal system clock is running, MPU continues to execute NOP instruction even in the halt state.

(a) RUN Mode (MS1=1, MS2=1)

Shown in Fig. 3.4 is the basic timing when the halt instruction is executed in RUM Mode.

In RUN Mode, system clock (ϕ) in MPU and clock output (CLK) to the outside of MPU are not stopped even after the halt instruction is executed. Therefore,until the halt stae is released by the interrupt signal ($\overline{MNI}$ OR $\overline{INT}$) or $\overline{RESET}$ signal, MPU continues to execute NOP instruction.

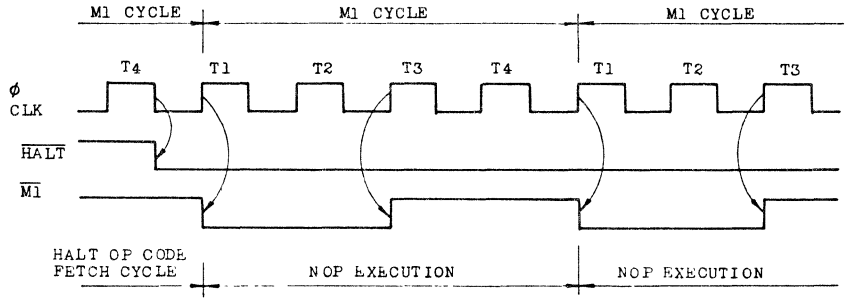


Fig. 3.4 Timing of RUN Mode (at Halt Command Execution)

(b) IDLE1 Mode (MS1=0, MS2=0)
Shown in Fig. 3.5 is the basic timing when the halt instruction is executed in IDLE1 Mode.
In IDLE1 Mode, system clock (ϕ) in MPU and clock output (CLK) to the outside of MPU are stopped and MPU stops its operation after the halt instruction is exeduted.
However, the internal oscillator continues to operate.

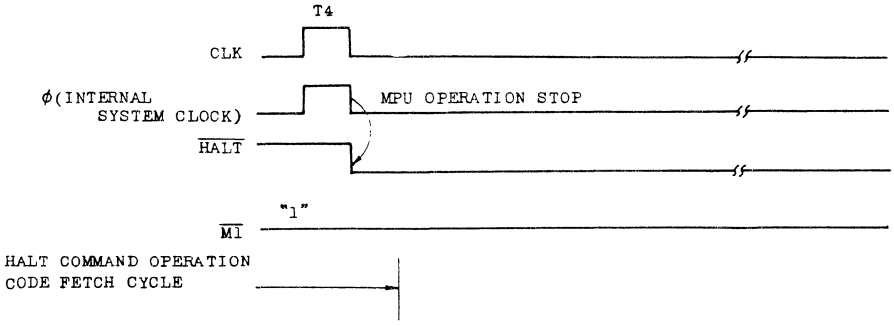


Fig. 3.5 IDLE1 Mode Timing (at Halt Instruction Execution)

(c) IDLE2 Mode (MS1=0, MS2=1)
Shown in Fig. 3.6 is the basic timing when the halt instruction is executed in IDLE2 Mode.
In IDLE2 Mode, system clock (ϕ) in MPU is stopped and MPU stops its operation after the halt instruction is executed.
However, the internal oscillator and clock output (CLK) to the outside of MPU continues to operate.

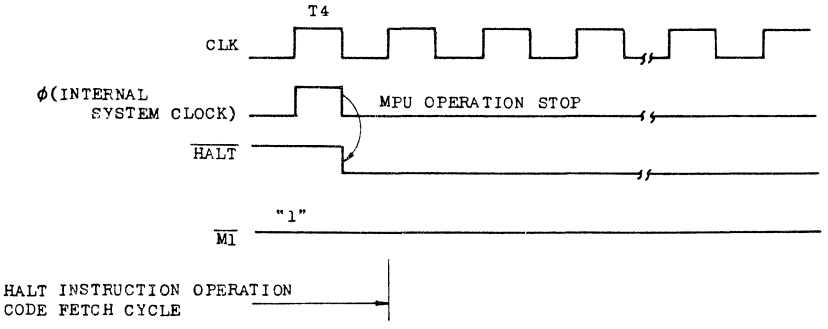


Fig. 3.6 IDLE2 Mode Timing (at Halt Instruction Execution)

(d) STOP Mode (MS1=1, MS2=0)
Shown in Fig. 3.7 is the basic timing when the halt instruction is executed in STOP Mode.
In STOP Mode, internal operation and internal oscillator are stopped after the halt instruction is executed. Therefore, system clock (ϕ) in MPU and clock output (CLK) to the outside of MPU are stopped.

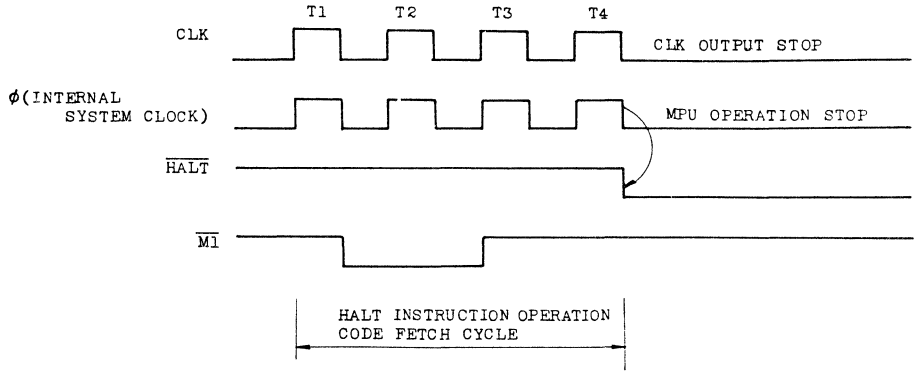


Fig. 3.7 STOP Mode Timing (at Halt Instruction Execution)

(2) Release from halt state
The halt state of MPU is released when "0" is input to $\overline{\text{RESET}}$ signal and MPU is reset or an interrupt request is accepted. An interrupt request signal is sampled at the leading edge of the last clock cycle (T4 state) of NOP instruction. In case of the maskable interrupt, interrupt will be accepted by an active $\overline{\text{INT}}$ signal ("0" level). In case of the non-maskable interrupt, if the internal $\overline{\text{NMI}}$ F/F which is set at the leading edge of $\overline{\text{NMI}}$ signal is set to "1", the interrupt is accepted. However, in case of the maskable interrupt, the interrupt enable flip-flop must have been set to "1". The accepted interrupt process is started from next cycle.

Further, when the internal system clock is stopped (IDLE1/2 Mode, STOP Mode), it is necessary first to restart the internal system clock. The internal system clock is restarted when $\overline{\text{RESET}}$ or interrupt signal ($\overline{\text{NMI}}$ or $\overline{\text{INT}}$) is input.

(a) RUM Mode (MS1, MS2=1)
The halt release operation by acceptance of interrupt request in RUN Mode is shown in Fig. 3.8.
In RUN Mode the internal system clock is not stopped and therefore, if the interruption signal is recognized at the rise of T4 state of the continued NOP instruction, MPU will executes the interrupt process from next cycle.

The halt release operation by resetting MPU in RUN Mode is shown in Fig. 3.9. After reset, MPU will execute an instruction starting from address 0000H. However, in order to reset MPU it is necessary to keep $\overline{RESET}$ signal at "0" for at least 3 clocks. In addtion, if $\overline{RESET}$ signal becomes "1", after the dummy cycle for at least 2T states, MPU executes an instruction from address 0000H.

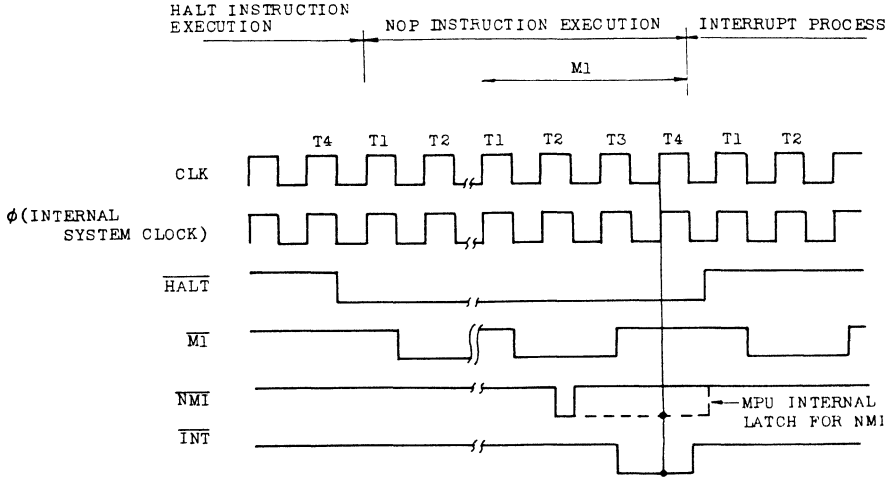


Fig. 3.8 Halt Release Operation Timing by Interrupt Request Signal in RUN Mode

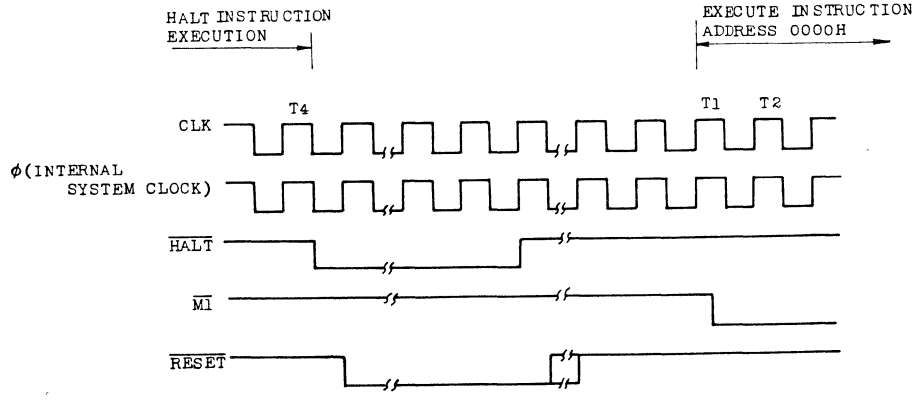


Fig. 3.9 Halt Release Operation Timing by Reset in RUN Mode

(b) IDLE1 Mode (MS1=0, MS2=0), IDLE2 Mode (MS1=0, MS2=1)

The halt release operation by interrupt signal in IDLE1 Mode is shown in Fig. 3.10 (a) and in IDLE 2 Mode in Fig. 3.10 (b).
When receiving $\overline{NMI}$ or $\overline{INT}$ signal, MPU starts the internal system clock operation. In IDLE1 Mode, MPU starts clock output to the outside at the same time. The operation stop of MPU in IDLE1/2 Mode is taken place at "0" level during T4 state in the halt instruction operation code fetch cycle. Therefore, after restarted by the interruption signal, MPU executes one NOP instruction and samples an interrupt signal at the rise of T4 state during the execution of this NOP instruction, and executes the interrupt process from nect cycle.

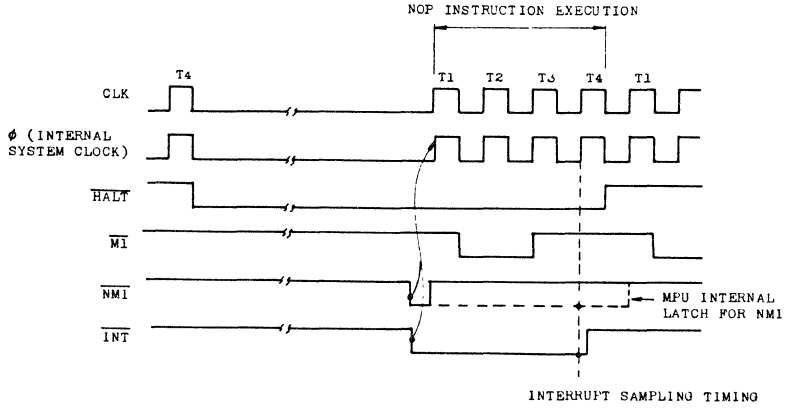


Fig. 3.10 (a) IDLE1 Mode

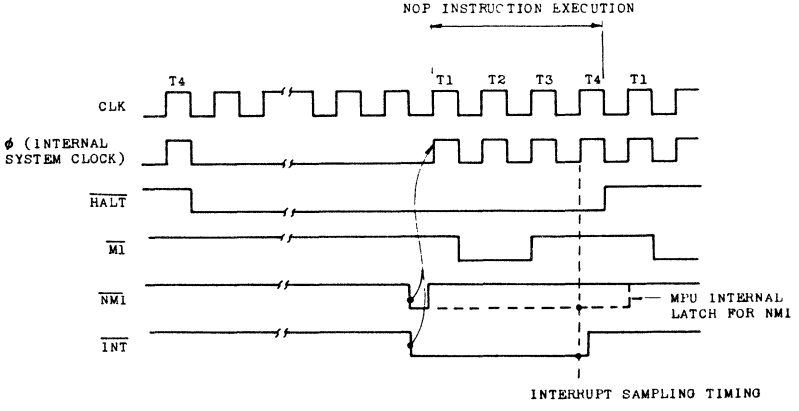


Fig. 3.10 (b) IDLE2 Mode

Fig. 3.10 Halt Release Operation Timing by Interrupt Request Signal in IDLE1/2 Mode

If no interrupt signal is accepted during the execution of the first NOP instruction after the internal system clock is restarted, MPU is not released from the halt state and is placed in IDLE1/2 Mode again at "0" level during T4 state of the NOP instruction, stopping the internal system clock. If $\overline{INT}$ signal is not at "0" level at the rise of T4 state, no interrupt request is accepted.

The halt release operation by resetting MPU in IDLE1 Mode is shown in Fig. 3.11 (a) and that in IDLE2 Mode in Fig. 3.11 (b).
When $\overline{RESET}$ signal at "0" level is input into MPU, the internal system clock is restarted and MPU will execute an instruction stored in address 0000H.
At time of $\overline{RESET}$ signal input, it is necessary to take the same care as that in resetting MPU in RUN Mode.

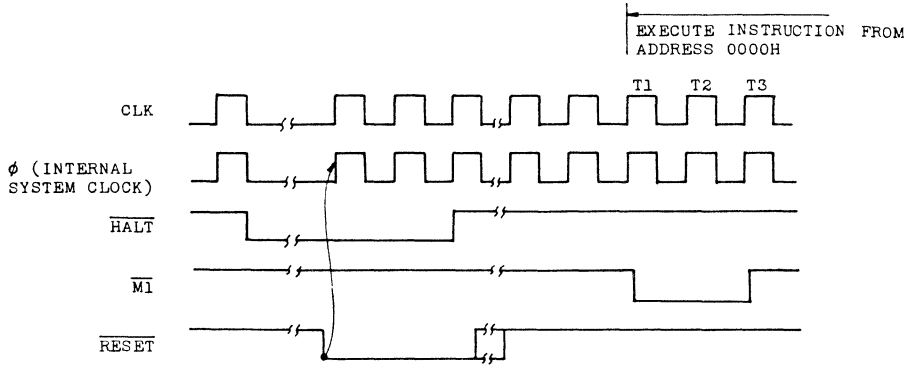


Fig. 3.11 (a) IDLE1 Mode

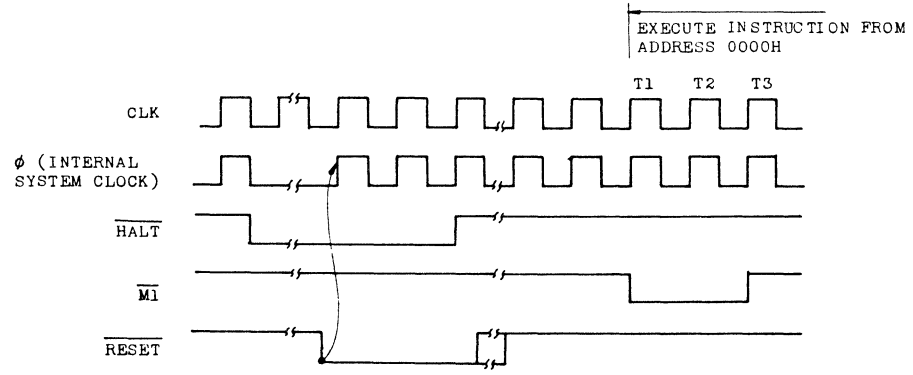


Fig. 3.11 (b) IDLE2 Mode

Fig. 3.11 Halt Release Operation Timing by Reset in IDLE1/2 Mode

(c) STOP Mode (MS1=1, MS2=0)

The halt release operation by interrupt signal in STOP mode is shown in Fig. 3.12.

When MPU received an interrupt signal, the internal oscillator is restarted. In order to obtain stabillized oscillation, the internal system clock and clock output to the outside are started after a warming-up time of (2**14+2.5) TcC (TcC: Clock Cycle) by the internal counter passed.

MPU executes one NOP instruction after the internal system clock is restarted and at the same time, sampling an interrupt signal at the rise of T4 state during the execution of this NOP instruction. If the interrupt signal is accepted, MPU executes the interrupt process operation from next cycle.

At time of interrupt signal input, it is necessary to take the same care as that in the interrupt signal input in IDLE1/2 Mode. The halt release operation by MPU resetting in STOP Mode is shown in Fig. 3.13.

When $\overline{\text{RESET}}$ signal at "0" level is input into MPU, the internal oscillator is restarted. However, since it performs a quick operation at time of power ON, the internal counter does not operate. Therefore, the operation may not be carried out properly due to unstable clock immediately after the internal oscillator is restarted. To restart the clock by $\overline{\text{RESET}}$ signal in STOP Mode, it is necessary to hold $\overline{\text{RESET}}$ signal at "0" level for sufficient time. When $\overline{\text{RESET}}$ signal becomes "1", after the dummy cycle for at least 2T states, MPU starts to execute an execution from address 0000H.

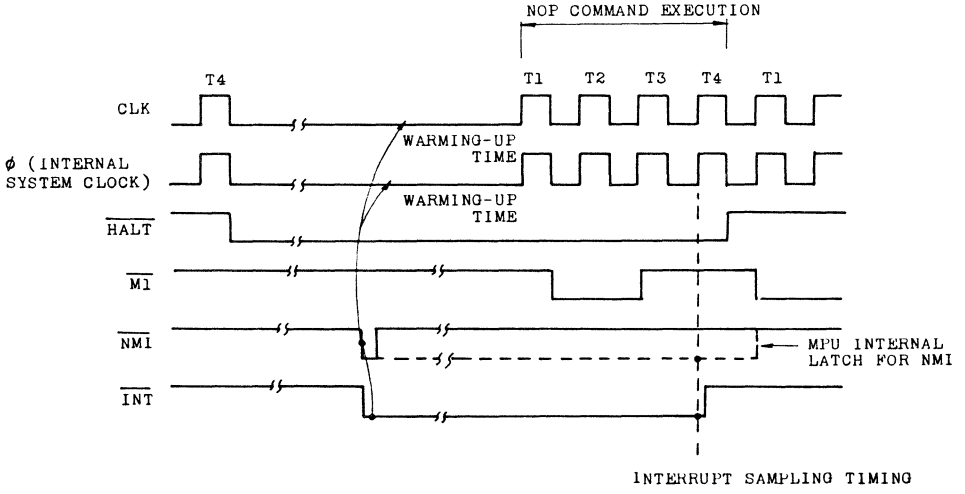


Fig. 3.12 Halt Release Operation Timing by Interrupt Request Signal in STOP Mode

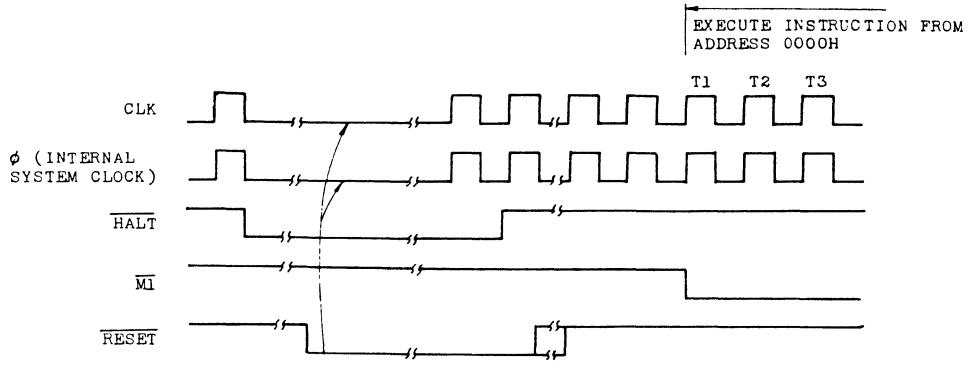


Fig. 3.13 Halt Release Operation Timing by Reset in STOP Mode

3.4 Instruction set

Instruction set of the TMPZ84C01F are the same as those for the TMPZ84C00P. For details refer to the data sheet for the TMPZ84C00P.

3.5 Method of use

A connecting example of the TMPZ84C01F with the TLCS-Z80 family peripheral LSI's is shown in Fig. 3.4. For the explanation and precautions for connection, refer to Section 3.5 Method of use of the data sheet for the TMPZ8400P.

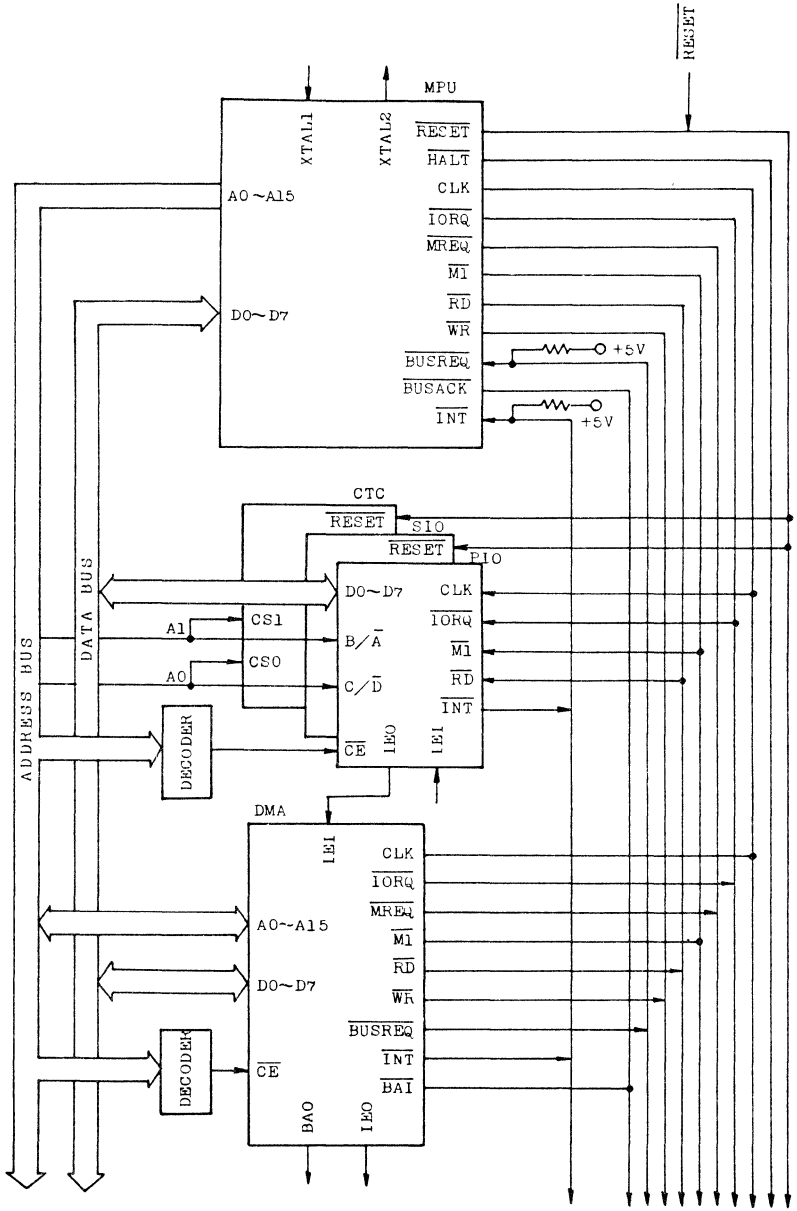


Fig. 3.14 Example Connection with Z80 family peripheral LSI

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Symbol	Item	Rating	Unit
VCC	Supply Voltage	-0.5 to +7	V
VIN	Input Voltage	-0.5 to Vcc + 0.5	V
PD	Power Dissipation (TA=85°C)	250	mW
TSOLDER	Soldering Temperature (10 sec)	260	°C
TSTG	Storage Temperature	-55 to 125	°C
TOPR	Operating Temperature	-40 to 85	°C

4.2 DC Electrical Characteristics

DC Characteristics (I)

TA = -40°C to 80°C, VCC = 5V ± 10%, VSS = 0V

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VOLC	Low Level Clock Output Voltage	IOL = 2.0mA	-	-	0.4	V
VOHC	High Level Clock Output Voltage	IOH =-2.0mA	VCC-0.6	-	-	V
VIL	Input Low Voltage		-0.5	-	0.8	V
VIH	Input High Voltage		2.2	-	VCC	V
VIHR	Input High Voltage ($\overline{\text{RESET}}$)		VCC-0.6	-	VCC	V
VILR	Input Low Voltage ($\overline{\text{RESET}}$)		-0.5	-	0.45	V
VOL	Output Low Voltage (Except Clock)	IOL = 2.0mA	-	-	0.4	V
VOH1	Output High Voltage (I) (Except Clock)	IOH = -1.6mA	2.4	-	-	V
VOH2	Output High Voltage (II)(Except Clock)	IOH = -250uA	VCC-0.8	-	-	V
ILI	Input Leak Current	VSS≦ VIN≦ VCC	-	-	±10	µA
ILO	3 State Output Current in Floating	VSS + 0.4≦ VOUT≦ VCC	-	-	±10	µA
ICC1	Supply Current (@ RUN Mode)	VCC=5V,CLK=4MHz VIHC=VIH=VCC-0.2V,VILC=VIL =0.2V	-	15	20	mA
(Note) ICC2	Supply Current (@ STOP Mode)	VCC=5V,CLK=Note VIHC=VIH=VCC-0.2V,VILC=VIL =0.2V	-	0.5	10	µA
ICC3	Supply Current (@ IDLE1 Mode)	VCC=5V,CLK=4MHz VIHC=VIH=VCC-0.2V,VILC=VIL =0.2V	-	1.0	2.0	mA

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
ICC4	Supply Current (@ IDLE2 Mode)	VCC=5V,CLK=4MHz VIHC=VIH=VCC-0.2V,VILC=VIL=0.2V	-	3.0	6.0	mA

(Note) At T4 "LOW" state of the halt instruction fetch cycle.

4.3 AC Electrical Charactreistics

TA = -40°C to 85°C, VCC = 5V ± 10%, VSS = 0V (*): TEST CONDITION

NO.	SYMBOL	ITEM	(*)	MIN.	TYP.	MAX.	UNIT
1	TcC	Clock frequency		250	-	DC	ns
2	TwCh	High clock pulse width		110	-	DC	ns
3	TwCl	Low clock pulse width		110	-	DC	ns
4	TfC	Clock falling time		-	-	30	ns
5	TrC	Clock rising time		-	-	30	ns
6	TdCr(A)	Effective address output delay from clock rise		-	-	110	ns
7	TdA(MREQf)	Address output definite time prior to $\overline{MREQ}$		65	-	-	ns
8	TdCf(MREQf)	Delay from clock fall to $\overline{MREQ}$="L"		-	-	85	ns
9	TdCf(MREQr)	Delay from clock rise to $\overline{MREQ}$="H"		-	-	85	ns
10	TwMREQh	$\overline{MREQ}$ high level pulse width		110	-	-	ns
11	TwMREQl	$\overline{MREQ}$ low level pulse width	CL=	220	-	-	ns
12	TdCf(MREQr)	Delay from clock fall to $\overline{MREQ}$="H"	100pF	-	-	85	ns
13	TdCf(RDf)	Delay from clock fall to $\overline{RD}$="L"		-	-	95	ns
14	TdCr(RDr)	Delay from clock rise to $\overline{RD}$="H"		-	-	85	ns
15	TsD(Cr)	Data set-up time for clock rise		35	-	-	ns
16	ThD(RDr)	Data hold time for $\overline{RD}$ rise		0	-	-	ns
17	TsWAIT(Cf)	$\overline{WAIT}$ signal set-up time for clock fall		70	-	-	ns
18 *	ThWAIT(Cf)	$\overline{WAIT}$ hold time after clock fall		10	-	-	ns
19	TdCr(M1f)	Delay from clock rise to $\overline{M1}$="L"		-	-	100	ns
20	TdCr(M1r)	Delay from clock rise to $\overline{M1}$="H"		-	-	100	ns

NO.	SYMBOL	ITEM	(*)	MIN.	TYP.	MAX.	UNIT
21	TdCf(RDr)	Delay from clock fall to $\overline{RD}$="H"		-	-	85	ns
22	TdCr(RDf)	Delay from clock rise to $\overline{RD}$="L"		-	-	85	ns
23	TsD(Cf)	Data set-up time for clock fall (at time of M2, M3, M4, M5 cycle)		50	-	-	ns
24	TdA(IORQf)	Address definite time prior to $\overline{IORQ}$ fall		180	-	-	ns
25	TdCr(IORQf)	Delay from clock rise to $\overline{IORQ}$="L"		-	-	75	ns
26	TdCf(IORQr)	Delay from clock fall to $\overline{IORQ}$="H"		-	-	85	ns
27	TdD(WRf)	Data definit time prior to $\overline{WR}$ fall		80	-	-	ns
28	TdCf(WRf)	Delay from clock fall to $\overline{WR}$="L"		-	-	80	ns
29	TwWR	$\overline{WR}$ pulse width		220	-	-	ns
30	TdCf(WRr)	Delay from clock fall to $\overline{WR}$="H"		-	-	80	ns
31	TdD(WRf)	Data definite time prior to $\overline{WR}$ fall		-10	-	-	ns
32	TdCr(WRf)	Delay from clock rise to $\overline{WR}$="L"	CL=	-	-	65	ns
33	TdWRr(D)	Output data holding after $\overline{WR}$="H"	100pF	60	-	-	ns
34	TdCf(HALT)	Delay from clock fall to HALT="L" or "H"		-	-	300	ns
35	TwNMI	$\overline{NMI}$ pulse width		80	-	-	ns
36	TsBUSREQ(Cr)	Set-up time for clock rise		50	-	-	ns
37 *	ThBUSREQ(Cr)	$\overline{BUSREQ}$ hold time after clock rise		10	-	-	ns
38	TdCr(BUSACKf)	Time from clock rise to $\overline{BUSACK}$="L"		-	-	100	ns
39	TdCf(BUSACKr)	Time from clock fall to $\overline{BUSACK}$="H"		-	-	100	ns
40	TdCr(Dz)	Delay from clock rise to data bus float state		-	-	90	ns
41	TdCr(CTz)	Delay from clock rise to control output float state ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, $\overline{WR}$)		-	-	80	ns
42	TdCr(Az)	Delay from clock rise to address bus float state		-	-	90	ns
43	TdCr(A)	Address holding time from $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$		80	-	-	ns

NO.	SYMBOL	ITEM	(*)	MIN.	TYP.	MAX.	UNIT
44	TsRESET(Cr)	$\overline{RESET}$ set-up time for clock rise		60	-	-	ns
45 *	ThRESET(Cr)	$\overline{RESET}$ hold time from clock rise		10	-	-	ns
46	TsINTf(Cr))	$\overline{INT}$ set-up time for clock rise		80	-	-	ns
47 *	TsINTr(Cr)	$\overline{INT}$ hold time after clock rise		10	-	-	ns
48	TdM1F(IORQf)	$\overline{M1}$ output ("L") definite time prior to $\overline{IORQ}$ fall	CL= 100pF	565	-	-	ns
49	TdCf(IORQf)	Delay from clock fall to $\overline{IORQ}$="L"		-	-	85	ns
50	TdCr(IORQr)	Delay from clock rise to $\overline{IORQ}$="H"		-	-	85	ns
51	TdCf(D)	Delay from clock fall to data output		-	-	150	ns
52	TRST1S	Clock (CLK) restart time by $\overline{INT}$ (STOP mode)		-	(2**14+2.5)xTcC	-	ns
53	TRST2S	Clock (CLK) restart time by $\overline{NMI}$ (STOP mode)		-	(2**14+2.5)xTcC	-	ns
54	TRST1I	Clock (CLK) restart time by $\overline{INT}$ (IDLE1/2 mode)		-	2.5TcC	-	ns
55	TRST2I	Clock (CLK) restart time by $\overline{NMI}$ (IDLE1/2 mode)		-	2.5TcC	-	ns

Note 1. Test conditions
VIH = 2.4V, VIL = 0.4V, VIHC = VCC - 0.6V, VILC = 0.6V
VOH = 2.2V, VOL = 0.8V
Note 2. Items with an asterisk (*) are non-compatible with NMOS Z80.

4.4 Capacitance
The capacity of TMPZ84C01F is alike with that of the TMPZ84C00P. For details refer to the relative part of the TMPPZ84C00P.

4.5 Timing diagram
Figs. 4.1 to 4.10 show the basic timings of respective operations. Numbers shown in the figures correspond with those in the AC Electrical Characteristics Table in 4.3.

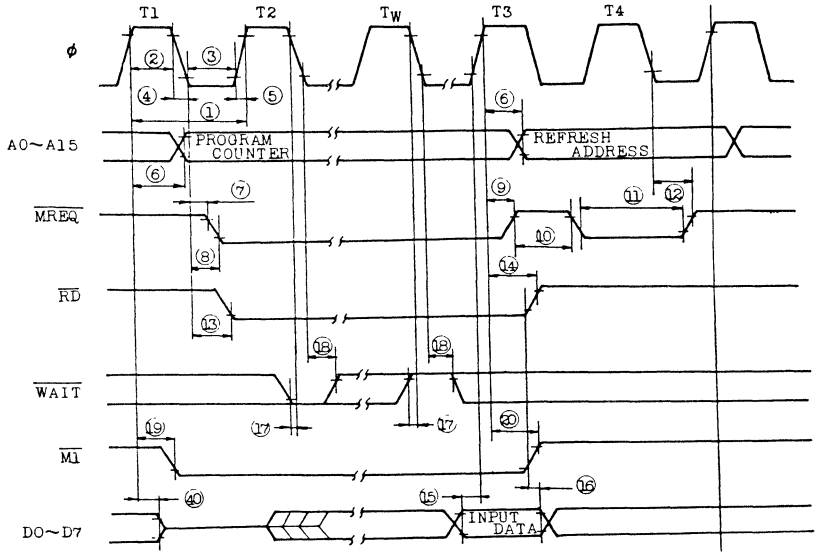


Fig. 4.1 Operation Code Fetch Cycle

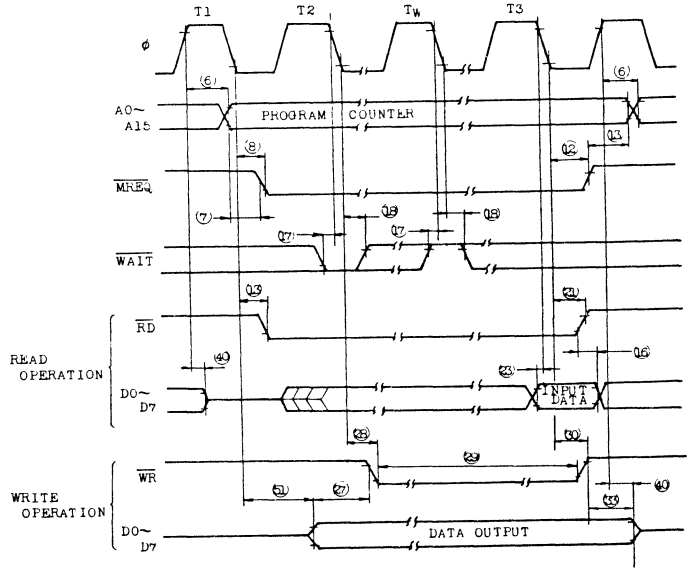
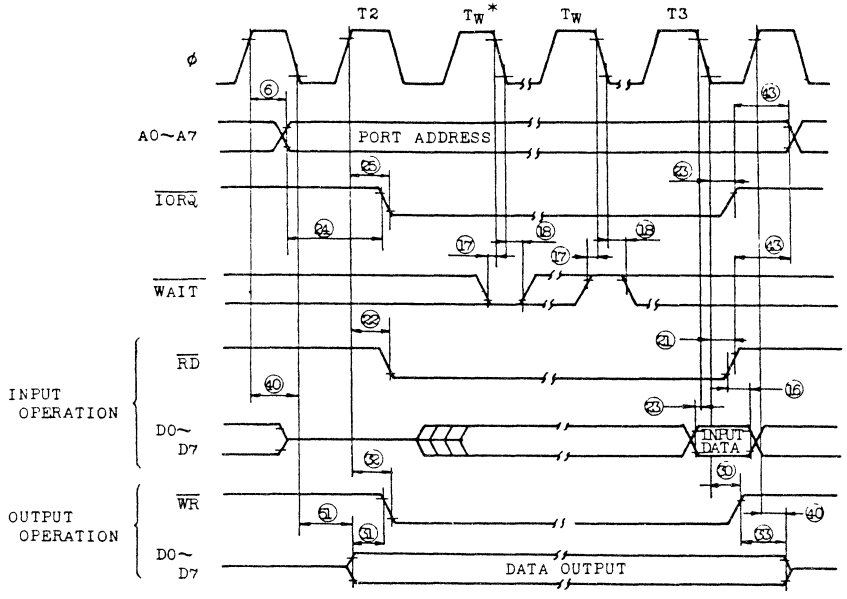
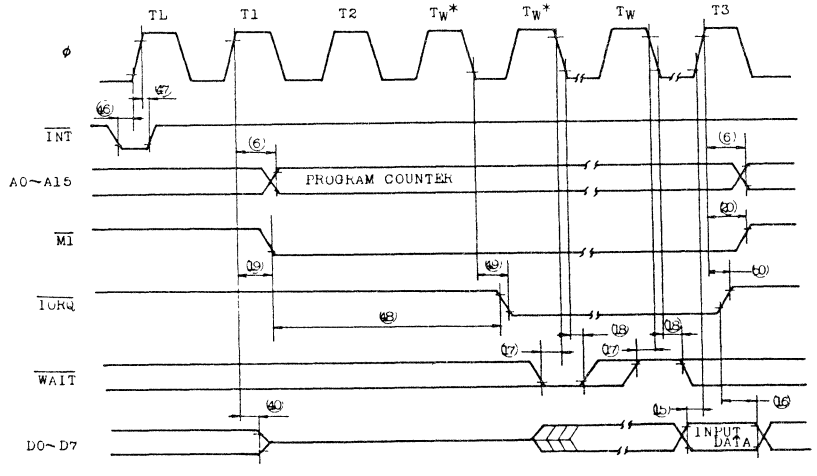


Fig. 4.2 Memory Read/Write Cycle



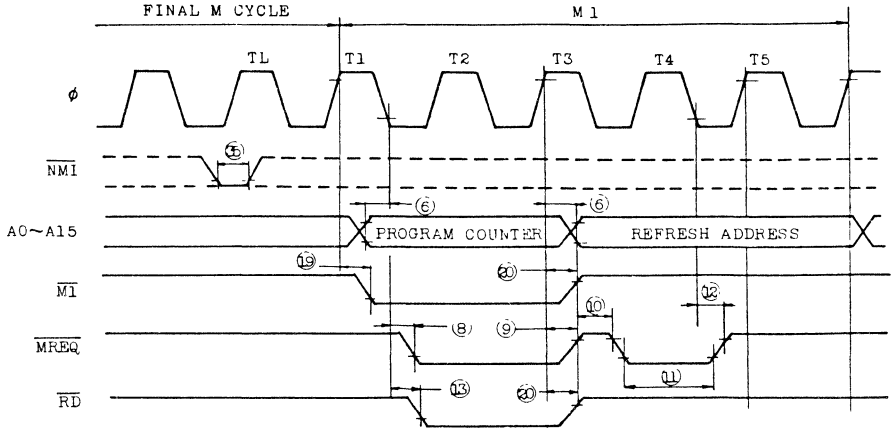
(Note) 1 wait state (TW*) is inserted automatically by MPU.

Fig. 4.3 Input/Output Cycle



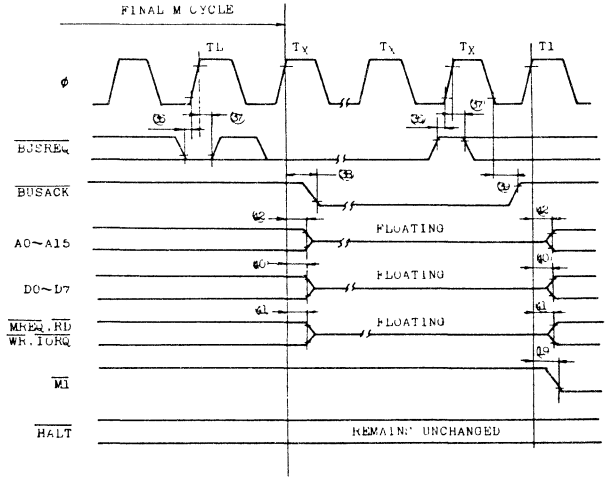
Note 1 TL is the final state of the preceding instruction.
Note 2 2 wait state (TW*) is inserted automatically by MPU.

Fig. 4.4 Interrupt Request/Acknowledge Cycle



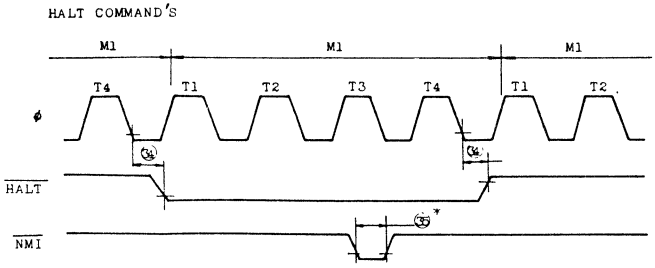
(Note) $\overline{NMI}$ is asynchronous input but in order to assure the positive response in the following cycle, $\overline{NMI}$ trailing edge signal must be generated keeping abreast of the leading edge of the preceding TL state.

Fig. 4.5 Non-maskable Interrupt Request Cycle



Note 1 TL is the final state of any machine cycle.
Note 2 Tx is optional clock used by requested peripheral LSI.

Fig. 4.6 Bus Request/Acknowledge Cycle



(Note) $\overline{INT}$ signal is also used for releasing from the halt state.

Fig. 4.7 Halt Asknowlege Cycle

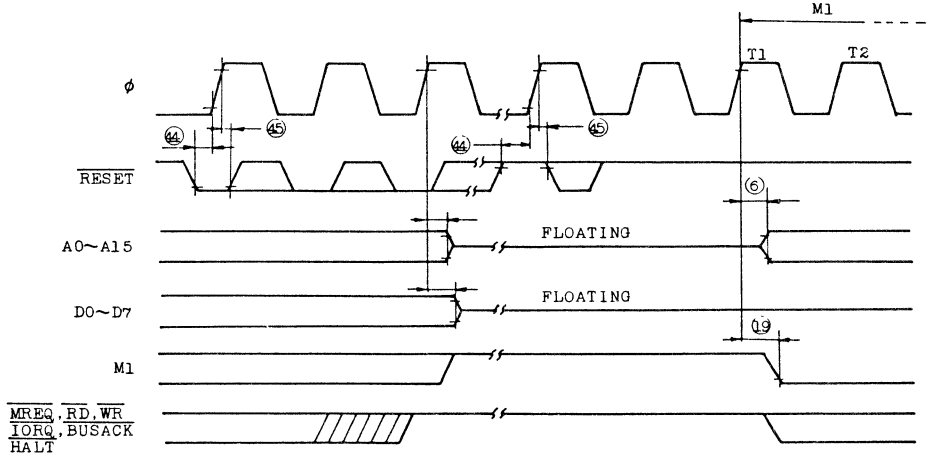


Fig. 4.8 Reset Cycle

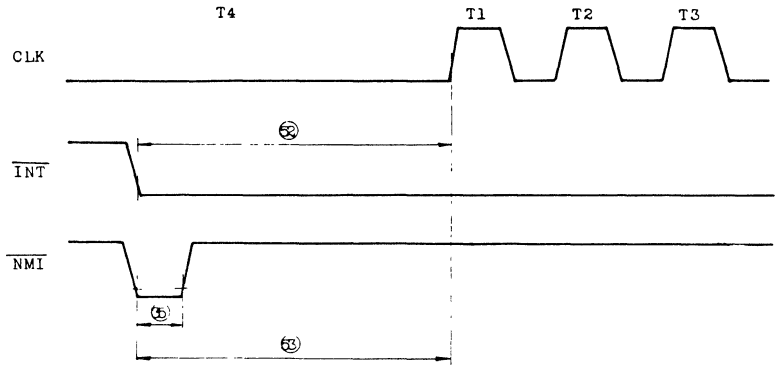


Fig. 4.9 Clock Restart Timing (STOP Mode)

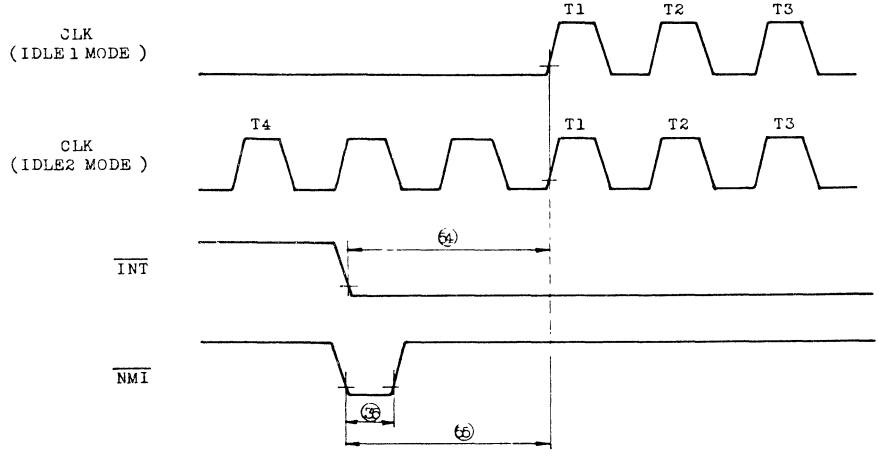
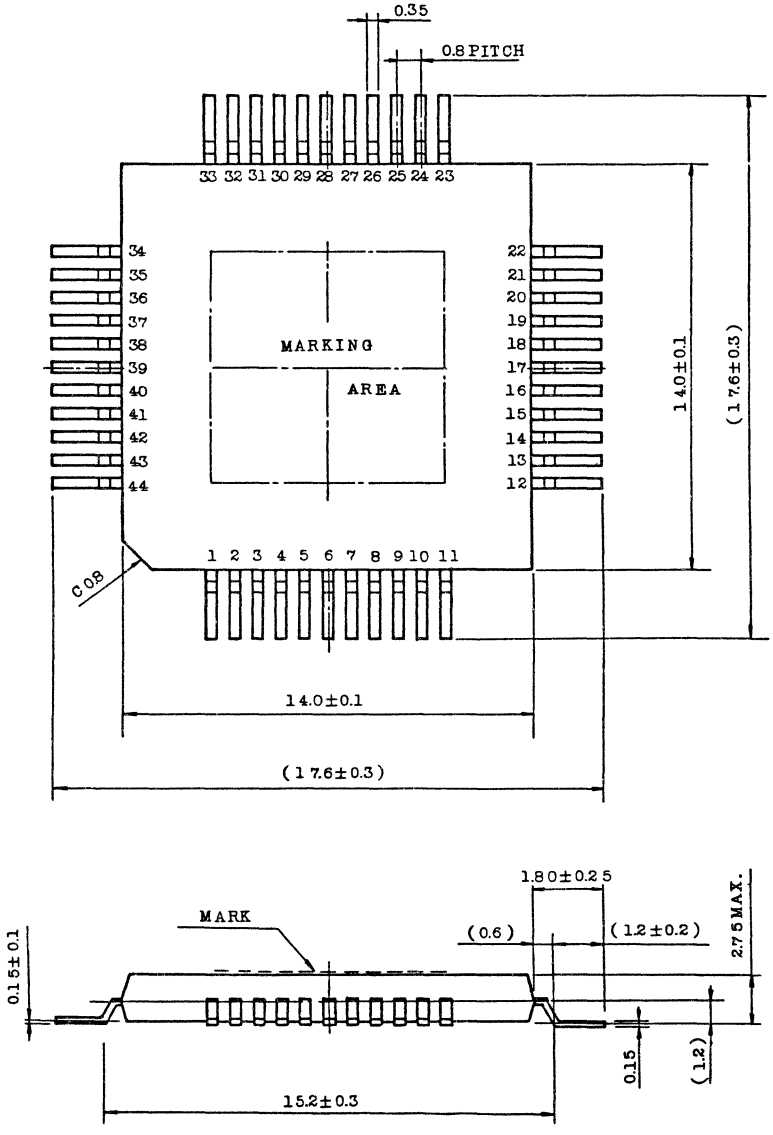


Fig. 4.10 Clock Restart Timing (IDLE1/2 Mode)

5. Outline Drawing

Unit in mm



6. Precautions

(1) To reset MPU, it is necessary to hold $\overline{\text{RESET}}$ signal input at "0" level for at least 3 clocks.
In particular, to release the HALT state by $\overline{\text{RESET}}$ signal in STOP Mode, hold $\overline{\text{RESET}}$ signal at "0" level for sufficient time in order to stabilize output from the internal oscillator.

(2) In releasing MPU from the HALT state by interrupt signal in IDLE1/2 Mode and STOP Mode, MPU will not be released from the HALT state and the internal system clock will stop again unless an interrupt signal is accepted during the execution of NOP instruction even when the internal system clock is restarted by the interrupt signal input. In particular, care must be taken when $\overline{\text{INT}}$ is used.

Other precautions are identical to those for the TMPZ84C00P except those for $\overline{\text{RFSH}}$ termial. Refer to the data sheet for the TMPZ84C00P.

TMPZ84C10AP, *TMPZ84C10AP-6, TMPZ84C10AF, *TMPZ84C10AF-6

CMOS Z80 DMA: Direct Memory Access Controller

1. General Description and Features

The TMPZ84C10A (hereinafter referred to as DMA) is CMOS version of Z80 DMA (Direct Memory Access Controller) which provides low power consuming but powerful and versatile operations.
This DMA is designed to improve system performance by allowing the system memory and peripheral LSI's to directly transfer data between them. Memory-to-memory and I/O-to-I/O (I/O devices as peripheral LSI or I/O devices such as printer, etc.) data transfer capability is also provided.

The DMA is fabricated using Toshiba's CMOS Silicon Gate Technology.
The principal functions and features of the DMA are as follows.

(1) Compatible with the Zilog Z80 DMA.
(2) DC to 4MHz operation (TMPZ84C10AP/TMPZ84C10AF)
DC to 6MHz operation (TMPZ84C10AP-6/TMPZ84C10AF-6)
(3) Single 5V power supply: 5V±10%
(4) Data transfer rate 2M bytes/sec. (at 4MHz), 3M bytes/sec. (at 6MHz)
(5) Data transfer in max. 64K byte block length.
(6) Address generation with incrementing, decrementing, or fixed address by source and destination.
(7) Built-in daisy chain structure interrupt circuit.
(8) Low power consumption
5mA Typ. (5V,4MHz)
6mA Typ. (5V,6MHz)
10uA MAX. (5V, stand-by)
(9) Extended operating temperature
-40°C to 85°C
(10) Transfer, search, or transfer/search operations can be specified.
(11) Byte, burst or continuous modes can be specified.
(12) Bit maskable byte searching function.
(13) Available in standard 40-pin dual-in-line package and 44-pin mini flat package.

Further, in the following text and explanations for charts and tables, hexadecimal numbers are directly used without giving an identification to explanation of address, etc. to the extent not to cause confusions.

* Under development.

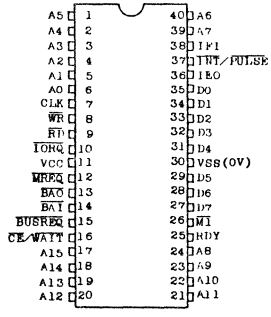
(Note) Z80(R) is a registered trademark of Zilog Inc., U.S.A.

2. Pin Connections and Pin Functions

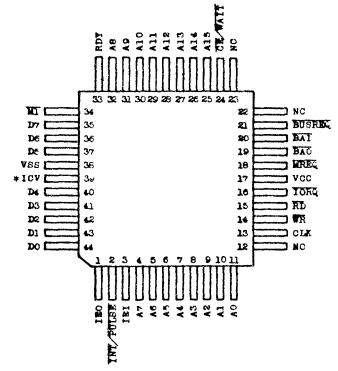
The pin connections and I/O pin names and brief functions of the TMPZ84C10A are shown below.

2.1 Pin connections

The pin connections of the TMPZ80C10A are as shown in Fig. 2.1.



(a) TMPZ84C10AP/AP-6



(Note) NC must be used at open condition.
*ICV must be used at open
Condition or Connected with Vcc.

(b) MFP Pin Connection

(b) TMPZ84C10AF/AF-6

Fig. 2.1 Pin Connections (Top View)

2.2 Pin names and functions

Table 2.1 Pin Names and Functions

Pin Name	Number of Pin	Input/Output 3-state	Function
A0 - A15	16	Output 3-state	16-bit address bus. DMA output address bus to source port and destination port.
CLK	1	Input	Single phase clock signal. Clock input to DMA. The same clock as that for MPU can be used.
$\overline{WR}$	1	I/O 3-state	Write signal. When used as input, MPU writes to DMA control register. When used as output, DMA controls write to the memory or I/O port address.
$\overline{RD}$	1	I/O 3-state	Read signal. When used as input, MPU reads out of DMA status register. When used as output, DMA controls read from the memory or I/O port address.

Pin Name	Number of Pin	Input/Output 3-state	Function
$\overline{IORQ}$	1	I/O 3-state	I/O request signal. When I/O data is read or written, DMA controls read/write.
$\overline{MREQ}$	1	Output 3-state	Memory request signal. When memory data is read or written, DMA controls read/write.
$\overline{BAO}$		Output	Bus line enable output signal. In the several DMA configuration, controls priority for the bus using right.
$\overline{BAI}$		Input	Bus line enable input signal. Indicates that the system bus using right is released for DMA control.
$\overline{BUSREQ}$	1	I/O	Bus line enable input signal. Indicates that the system bus control are sent to MPU. Open drain.
$\overline{CE}/\overline{WAIT}$	1	Input	Chip enable/wait signal. Normally, operates as $\overline{CE}$ but it is possible to program to operate as $\overline{WAIT}$ at time of data transfer.
RDY	1	Input	Ready signal. Monitored by DMA to determine effective polarity. Effective polarity is programmable.
$\overline{M1}$	1	Input	Signal showing machine cycle 1. Indicates that MPU is in the operation code fetch cycle or interruption acknowledge.
D0-D7	8	I/O 3-state	8-bit bidirectional data bus. Control byte from MPU, status byte from DMA and data from the memory or I/O are transferred through these terminals.
IEO	1	Output	Interrupt enable output signal. Using jointly with IEI, forms the daisy chain structure for interrupt priority when several peripheral LSI' are connected.
IEI	1	Input	Interrupt enable input signal. Using jointly with IEO, forms the daisy chain structure for interrupt priority when several peripheral LSI' are connected.
$\overline{INT}/\overline{PULSE}$	1	Output	Interrupt request signal For interrupt request and pulse generation. Open drain.
VCC	1	Power supply	+5V
VSS	1	Power supply	0V

3. Description of Operation

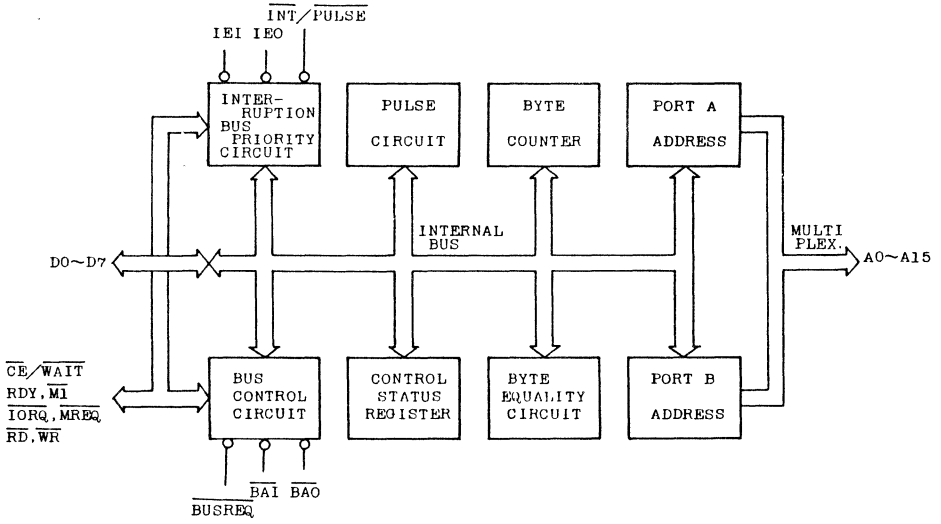


Fig. 3.1 Block Diagram

3.2 System configuration

The architecture (system configuration and functions) which must be known in using DMA will be described here.

Components

(1) Control & status register groups
(2) Bus control circuit
(3) Pulse circuit
(4) Byte couter
(5) Byte equality circuit
(6) Port A address
(7) Port B address
(8) Interruption pirority circuit

3.2.1 Control & status register groups

The DMA is provided with 21 writable regiser control register group and 7 readable register status register group. Registers are all in 8 bits but 2 byte data is held in optional 2 continued registers. The Z80 Microprocessor (hereinafter referred to as MPU) is capable of setting and monitoring values in respective registers.

The control register group is classified into 7 groups of WR0 to WR7 (Fig. 3.2), each of which is consisting of the basic register and related registers. The operation of DMA is controlled by programming in the control register group.

The status register group consists of RR0 to RR6 (Fig. 3.3) and are used to know state of execution or end of DMA operation.
Further, these registers are described in detail in 3.4 Commands.

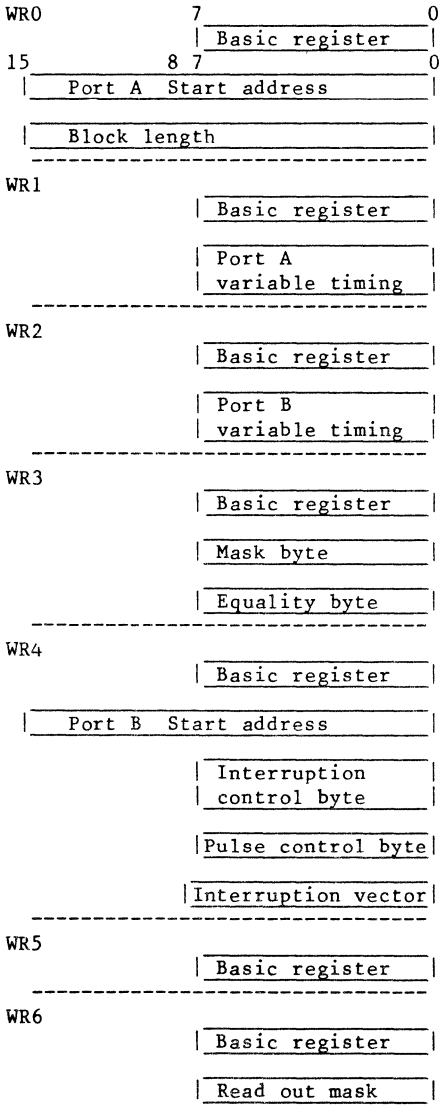


Fig. 3.2 Control Register

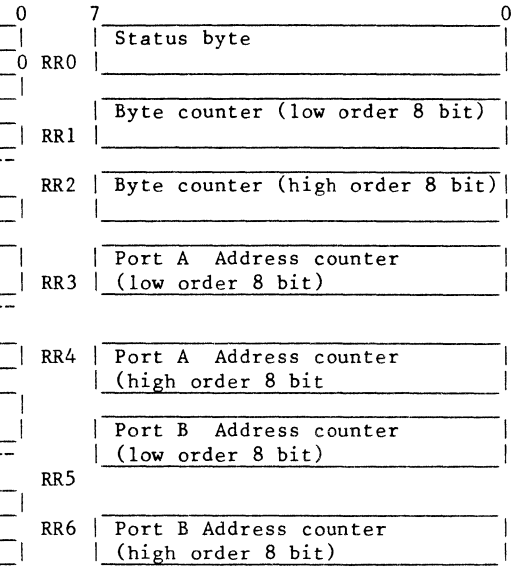


Fig. 3.3 Status Register

3.2.2 Bus control circuit

The bus control circuit controls bus direction between DMA and system bus at time of programming, while controls the control bus at time to data transfer according to the data transfer direction between the memory and I/O devices. In addition, it controls updating of required address counter and byte counter.

(1) Bus direction control

- o At time of programming, the bus master is MPU and the control bus and data bus (when data is written into the control regsiter) are in the direction from the system bus to DMA. Further, when data (status, etc.) is read from the control register, the direction will be from DMA to the sytem bus. At this time, the address bus buffer is deisabled.
- o At time data transfer, the bus master is DMA. The control bus buffer and address bus buffer are enabled, and the bus direction will become from DMA to the system bus.
- o When data is read out of the memory or I/O deivce, the data bus direction is from the system bus to DMA but it becomes in the direction from DMA to the system bus at time of data write.

(2) Bus request

If DMA requeseted MPU to transfer the bus control right and received it, MPU cannot fetch commands from the memory and is placed in the completely idle state.

For DMA to request the bus control right to MPU, following 2 enable conditions are required:

(a) Enable command from MPU
(b) Active RDY condition

3.2.3 Pulse circuit

The pulse circuit generates pulse signals on the INT line for every 256 bytes of 0 to 255 when data transfer is started. The details are described in 3.3.2 (2) (k).

3.2.4 Byte counter

The byte counter is cleared when data is transferred and is incremented by one whenever data is transferred for every 1 byte. A value of this counter is always compared with block length of WR0 and when they agree with each other, the DMA operation ends.

3.2.5 Byte equality circuit

DMA always monitors data being transferred during the data transfer and when equality is detected, generation of interruption becomes possible.

3.2.6 Port A address, Port B address

Data transfer is performed between Port A and Port B. Either port is specified by the source and destination specified by WR0.

3.2.7 Interrupt priority circuit

The Z80 system used the daisy chain structure to control interrupt among peripheral LSI's and the bus priority among multiple DMA's.
Further, for the interrupt timing, refer to 3.2.2 (2) (j).

(1) Interrupt daisy chain

When the interrupt priority is connected in the daisy chain structure, connect IEI and IEO. When the interrupt is acknowledged, the interrupt configuration of MPU is disabled. In order to allow other peripheral LSI to make the interrupt into MPU, it is necessary to enable the MPU's interrupt configuration by the interrupt enable command. The interrupt enable command is normally executed in the service routine. When the interrupt enable command is executed in the early part of the service routine, a peripheral LSI with higher priority can make the interrupt even when MPU is executing the service routine. (Interrupt in the nest structure is authorized.)

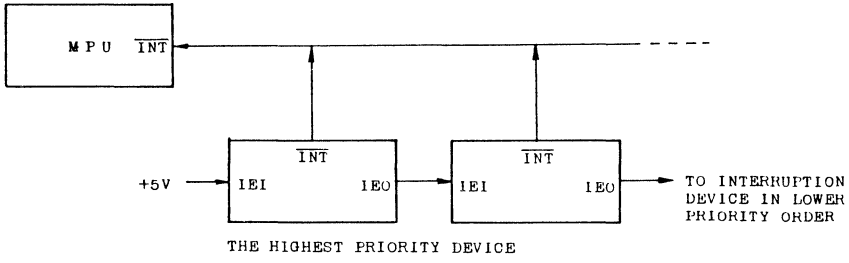


Fig 3.4 Interruption Daisy Chain

(2) Bus request daisy chain

When multiple DMA's are used, priority can be controlled by the daisy chain structure connection. Since BUSREQ signal of each DMA is bidirectional type, each DMA in the daisy chain is able to know bus requests as an input and until a DMA having the bus completes its operation, the bus requests of other DMA's are kept in wait state. Untile completion of the operation, any DMA is not able to release the bus in operation by force. Further, the bus request daisy chain has no nesting function but is able to hold the bus until its process is completed.

The priority among DMA's in the daisy chain is in order from high order to low order corresponding to distances from MPU. Priority is so decided that low order DMA will not receive BUSACK signal through BA1/BA0 chain of DMA when multiple DMA's made the bus request in the same clock cycle period.

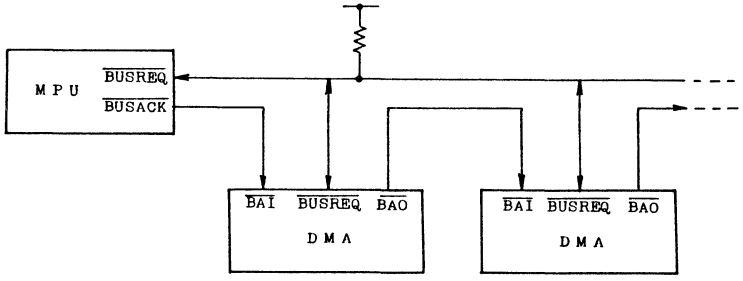


Fig. 3.5 Bus Request Daisy Chain

3.2.8 Basic functions

DMA is provided with the following basic functions:

(1) Data transfer paths
   1] Transfer between memory and I/O
   2] Transfer between memories
   3] Transfer between I/O and I/O
   4] Memory search
   5] I/O search
(2) Operating classes
(3) Operation modes
   1] Byte mode
   2] Burst mode
   3] Continuous mode
(4) Transfer speed
(5) Operating conditions
(6) Automatic restart
(7) Variable cycle
(8) Pulse generation

3.8.1 Data transfer paths

The data transfer paths of DMA are as shown in Fig. 3.6.

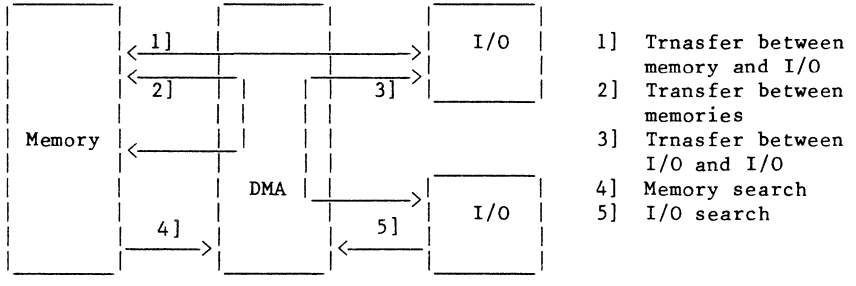


Fig. 3.6 Transfer paths of DMA

(1) Transfer between memory and I/O

This is the most ordinary method of data transfer and data transfer with the high speed serial interfaces (Z80SIO, etc.) is possible.

(2) Transfer between memories

This method of transfer is used for relocation of the memory content and high speed transfer of voluminous data between memories. In addition, this method is used to support memory mapped I/O. It is possible to program to make RDY conditions active for this type of data transfer.
The same function as that of LDIR command (block transfer command) of the Z80 MPU is provided. Number of clocks required by MPU for transfer of data of single byte is 21 clocks in case of the LDIR command while it can be processed in 4 clocks when DMA is used (in case of 2 cycle variable timing). Further, when DMA is used, approx. 420 clocks are required for initialization but in transfering data of 25 bytes or above, DMA becomes advantageous.

(3) Transfer between I/O and I/O
This method of transfer can be used in such applications as acquisition of real time data requiring temporary storage of input data. For instance, in transfering data from a diskette to a line printer, a program only starts the DMA operation and data is tranferred from I/O to I/O. However, if I/O error occurred, its recovery becomes necessary. Further, when there is a byte equality, it is possible to branch into various operations by the search function.

(4) Memory search
This memory search is used to search a large quantity of data at high speed. The same function as that of CPIR command (sarch command) of the Z80 MPU is provided. Number of clocks required by MPU for single byte memory search is 21 clocks when the CPTR command is used while the search is possible in 2 clocks (in case of 2 cycle variable timing) when DMA is used. Further, approx. 376 clocks are required for initialization when DMA is used and therefore, DMA is advantageous for memory search of more than 19 bytes. In addition, the search of special bytes in the end of block and character check block is also possible.

(5) I/O Search
This is used for search of special bytes in the end of block and character check block. For instance, this is used for search of a file mark showning a file delimiter on a magnetic tape.

3.2.8.2 Operating classes
There are 3 kinds of basic operation classes for DMA. 2 out of these 3 kinds are further divided into 2 classes. In addition, the ports referred to here denote the data source and destination.

(1) Data transfer between 2 ports
1] Transfer
Data transfer path in the flow of readout cycle followed by write cycle. This is executed without external logic circuit between DMA and MPU.
2] Simultaneous transfer
Data transfer path for simultaneous read and write of data tranferred between ports by generating required control signal through use of an external logic circuit. 2 times of efficiency of the transfer only class is obtained.

(2) Search of special bit pattern in byte at one port
1] Search
This is a method to search special bit pattern by comaparing data read from the source port with a matched byte. The matched byte is masked by another byte and can be compared with a special bit pattern (a certain bit in bytes).

(3) Data transfer between 2 ports and search
1] Transfer/search
Data transfer is performed in the same transfer method as that of the only transfer class and at the same time, the same search as that for the search only class is performed.

2] Simultaneous transfer/search
Data transfer is performed in the same transfer method as that of the simultaneous transfer class and at the same time, the same search as that for the search only class is performed.
In this case, an external logic circuit is required.

3.2.8.3 Operation modes

In the transfer methods for various operation classes, DMA can select the following modes:

- o Byte mode
- o Burst mode
- o Continuous mode

The single byte transfer/search is shown in Fig. 3.7 (commonly applicable to all modes).

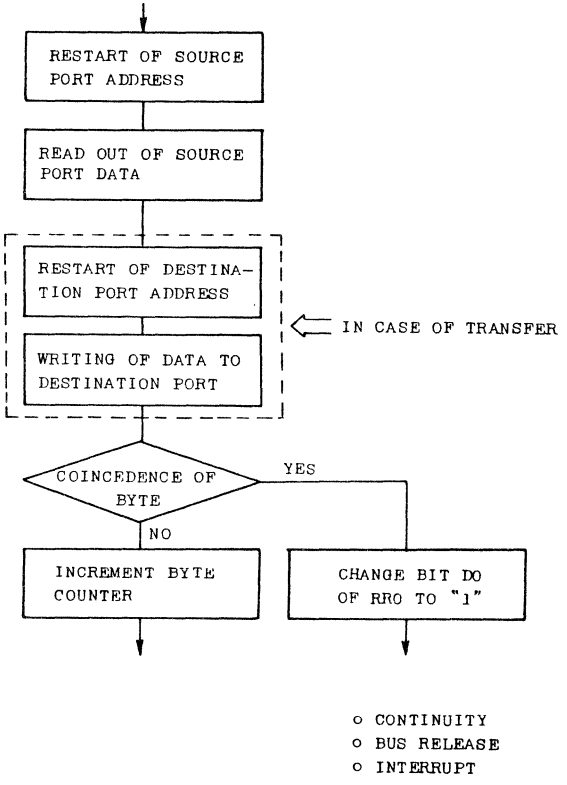


Fig. 3.7 Single Byte Transfer/Search

The data transfer is started at the point of time when DMA is enabled. In the first single byte operation in any mode, RDY signal is first checked to determine if it is active.

Then, the bus request is made and single byte transfer/search is performed when DMA becomes the bus master. The same operation is continued until the end of block judgement is made. If it is not the end of block, however, a different operation is carried out after judgement of RDY signal. The operations in respective modes are as shown in Fig. 3.8, 3.9 and 3.10.

(1) Byte mode

In the data transfer operation of DMA, the system bus control right is released whenever 1 byte is transferred at a time and the system bus control right is returned to MPU for at least one machine cycle period. If RDY signal of DMA is active when one machine cycle passes after the system bus control right is returned to MPU, the bus request is made again to MPU and next one byte data transfer is performed. Further, when RDY signal is non-active, the system bus control right is retained by MPU. This operation is shown in Fig. 3.8.

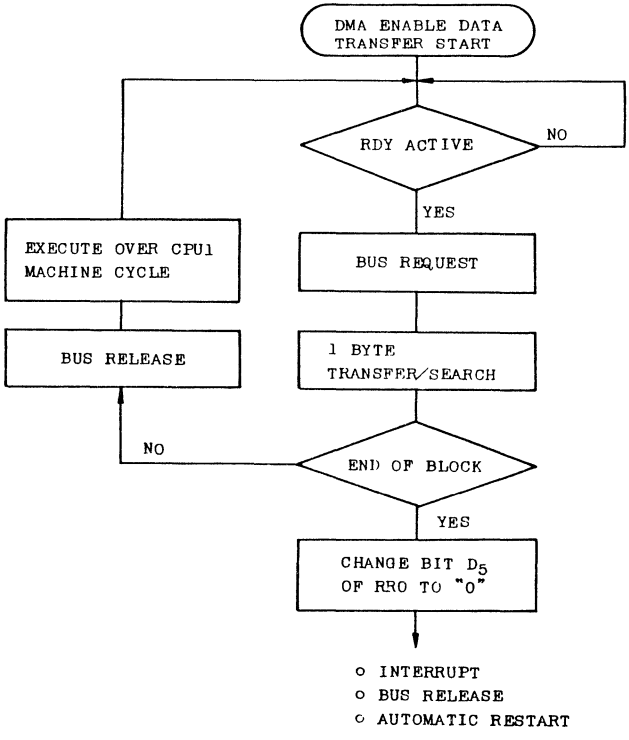


Fig. 3.8 Byte Mode

(2) Burst mode

In the burst mode, after one byte data is transferred, RDY signal is checked to determine if it is active whithout abandoning the system bus control right. If RDY signal is active, data transfer is continued until RDY signal becomes non-active and after the data transfer is completed, DMA stops to operate. Since MPU is ready to operate during the period in which I/O device does not transfer data (when RDY signal is non-active), data transfer rate and bus using efficiency are effective.
This operation is shown in Fig. 3.9.

Fig. 3.9 Burst Mode

(3) Continuous mode

When the data transfer is commenced, DMA retains the system bus control right until the transfer of last byte of a data block is completed or the stop condition of RDY signal becomes non-active during the operation, DMA is simply put in the idle state and still retains the system bus control right while waiting that RDY signal becomes active again. What must be taken care of ls that if number of data bytes is smaller than that set in the byte counter, DMA cannot end the block transfer forever and the system is impeded to operate properly.

This operation is shown in Fig. 3.10.

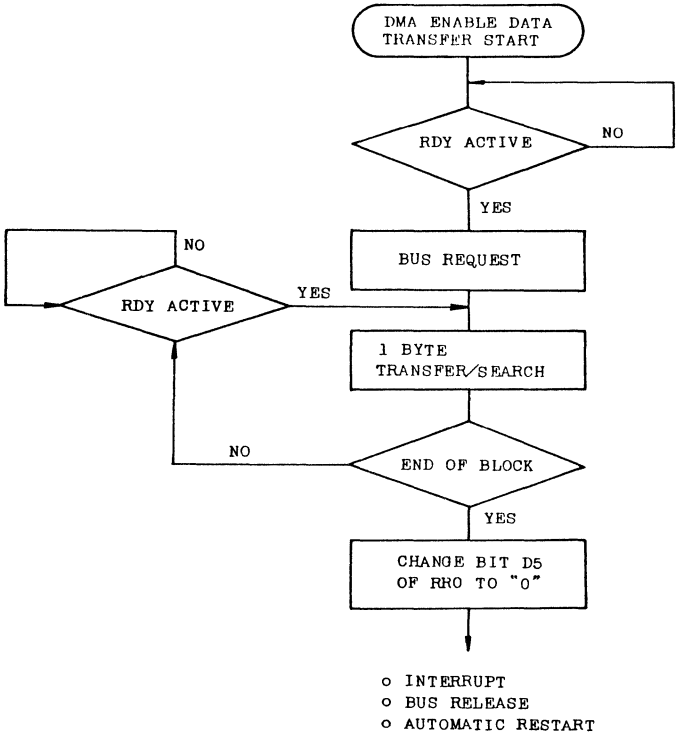


Fig. 3.10 Continuous Mode

3.2.8.4 Transfer speed

Shown in Table 3.1 are the comparison of max. transfer rates in 5 transfer classes of DMA operation and that of max. transfer rates in block transfer command of MPU. The max. speed transfer rate is accomplished in the simultaneous transfer operation of DMA and at least one external logic circuit is required. DMA transfers shown in the table are based on the assumption that interruption is not involved in the burst or continuous mode, and that the read and write cycle is 2 cycles.

Table 3.1 Transfer and Search Max. Speed (Burst and continuous modes)

Operation	Z-80 (4.0 MHz)	Z-80 (6.0 MHz)
Simultaneous transfer of DMA DMA search only Simultaneous transfer/ search	2M byte/S	3M byte/S
DMA transfer DMA transfer/search	1M byte/S	1.5M byte/S
Block transfer command of MPU	0.200M byte/S	0.300M byte/S

Shown in Table 3.2 is the comparison of the Z80 throughput reduction rate (per transfer K baud) in the byte mode of data transfer by DMA with the throughput reduction rate in the byte transfer using the interrupt service routine by six commands (actual minimum) by MPU. The DMA transfer in this data is based on the assumption that read and write cycle timing is longer than 2 cycles (min.). Therefore, MPU throughput reduction rate in the 2 cycle simultaneous tranfer is further reduced.

Table 3.2 Z-80 MPU throughput reduction per DMA transfer K baud (byte mode)

Operation	Z-80 (4.0 MHz)	Z-80 (6.0 MHz)
DMA transfer DMA transfer/search	0.041%	0.027%
MPU transfer by interrupt	0.213%	0.142%

3.2.8.5 Operating conditions

Programmable conditions to get DMA perform certain operations and these operations are shown in Table 3.3 (a) and (b). The conditions referred to here are those conditions for the internal registers of DMA, signals from peripheral LSI's and commands to DMA on the data bus. For details refer to Table 3.3 (a) and (b).

Table 3.3 (a) Operating Conditions

Conditions	Operations that can be caused under conditions at left hand
End of block	a. Bus release b. MPU interruption c. Automatic restart

Table 3.3 (b) Operating Conditions

Conditions	Operations that can be caused under conditions at left hand
Coincidence of byte	a. Bus release b. MPU interruption c. Continuation
Pulse control byte coincided with low order byte of byte counter	a. Pulse generation
RDY signal is active	a. Bus request b. MPU interruption
RDY signal is non-active	a. Bus release b. Breaking (in case of continuous mode)
RETI command (interruption return command from MPU)	a. Bus request

3.2.8.6 Automatic restart

In DMA data transfer, it is possible to automatically clear the byte counter, load the content of the start address register on the address counter again and restart the data transfer at the end of block.

The automatic restart function can reduce a burden of software on MPU in the CRT refresh or repeating operation. In addition, it is possible to write a different start address into the buffer register during the data transfer (when RDY signal is non-active and the bus is released during the data transfer in the byte mode or burst mode). At this time, it becomes possible to commence the automatic restart of data transfer from a new start address.

3.2.8.7 Variable cycle

DMA is capable of changing readout and write cycle lengths through programming. This function is effective in increasing data transfer rate and reducing a burden on a software, and an external logic circuit may be omitted. Refer to 3.3.2 (2) (i) where this function is described.

3.2.8.8 Pulse generation

DMA generates pulse signal on the INT line for every 256 bytes for data transfer. This is described in detail in 3.3.2 (2) (k).

3.2.9 Interrupt

DMA is able to make an interrupt request to MPU under the following conditions:

- o After DMA's RDY signal becomes active and before DMA makes a bus request (BUSREQ = "0").
- o When the content of the byte counter coincides with that of the block length register and the end of block is detected.
- o When the content of the coincided byte masked by the mask byte coincides with data in the transfer or search period when the byte coincidence is formed.

To make an interrupt request to MPU, it is necessary for DMA to release the bus. If DMA is the bus master, signal on the INT line generates periodic pulses to the peripheral LSI's, which are not sensed by MPU. Therefore, at the end of block or after stop by byte coincidence, DMA releases the bus before interrupting MPU.

If interrupt at the end of block and automatic restart at the end of block are set for DMA by programming, an interrupt is taken place at each end of block (at this point of time, it is acknowledged for the continuous operation). If the automatic restart is programmed in this case, the status flag at the end of block is not set. In this case, the interrupt vector cannot determine a factor for that interrupt.

On the Z80 system, interrupt is controlled through the daisy chain system. For the interrupt daisy chain, refer to 3.2.7 Interrupt/ Priority Circuit. In addition, for the interrupt timing, refer to 3.3.2 (2) (j).

3.3 Status change flowchart and basic timing

The status change flowchart and the basic data transfer timing by DMA are shown here. The status change flowchart is shown in 3.3.1 and the basic timing in 3.3.2.

3.3.1 Status change flowchart

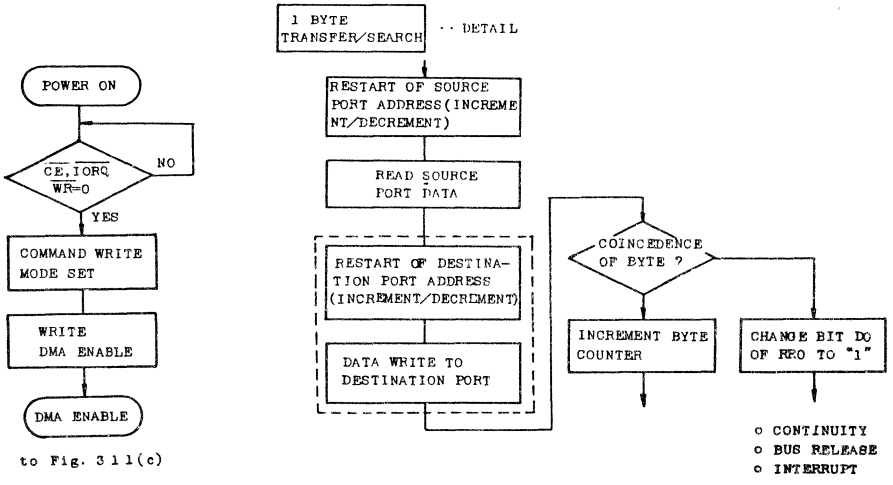
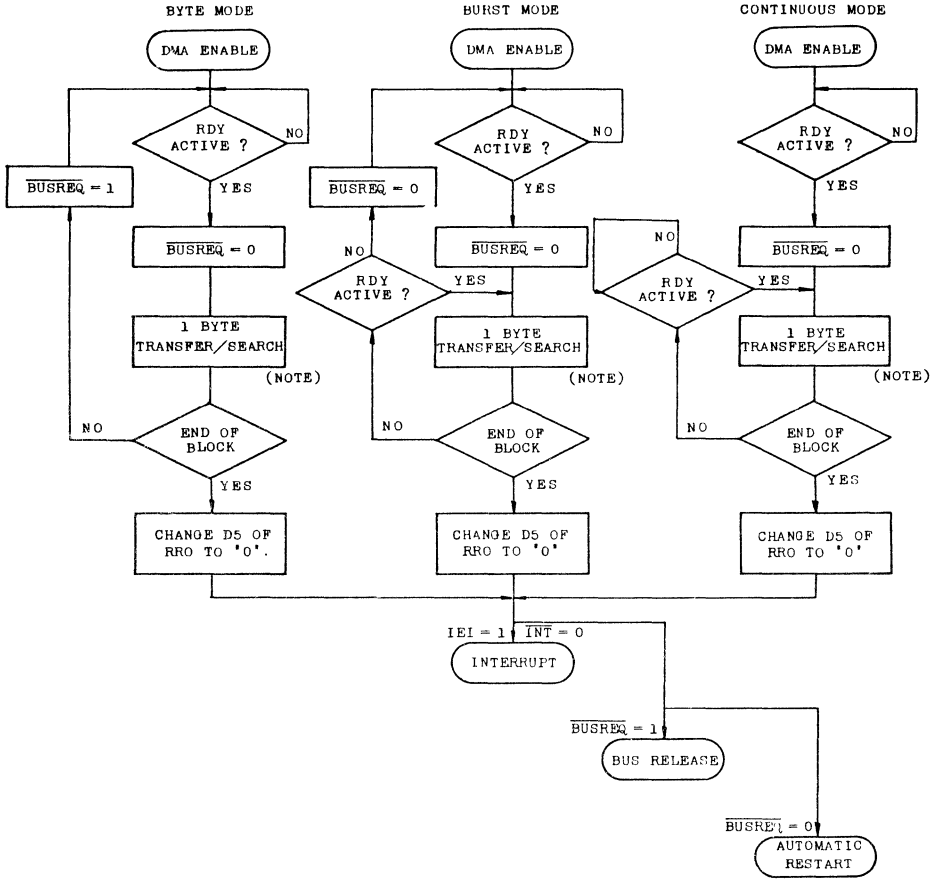


Fig. 3.11(a) Status Change Flowchart Fig. 3.11(b) Status Change Flowchart



(Note) The details for single byte transfer/search is shown in Fig. 3.11(b) Status Change Flowchart.

Fig. 3.11 (c) Status Change Flowchart

3.3.2 Basic timing

When DMA receives a command from MPU or reads the readout register, MPU has the system bus control right, BUSACK = "1", and MPU is called the bus master. When DMA operation is data transfer by DMA proper, BUSACK = "0", and DMA gets the system bus control right and becomes the bus master.

(1) When the bus master is MPU:

(a) Write timing into the write register

To write data into the write register, it is necessary for 3 signals of CE, IORQ and WR to become "0" simultaneously at the rising edge of clock. At this leading edge, DMA latches these 3 signals. After latched, CE, IORQ and WR signals may change to the invalid level after certain hold time. Further, DMA writes the status of the data bus (D0 to D7) into necessary write registers at the rising edge of next clock.

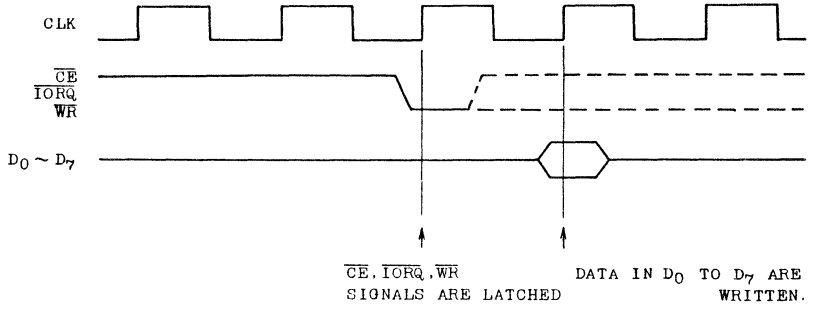


Fig. 3.12 Write Timing into the Write Register of DMA

(b) Readout timing from the readout register

To readout the readout register it is necessary that 3 signals of CE, IORQ and RD are at "0" and stable for more than 2 clocks. At the rising edges of 2 clocks, the status data is on the data bus and kept as long as CE, IORQ and WR signals are active.

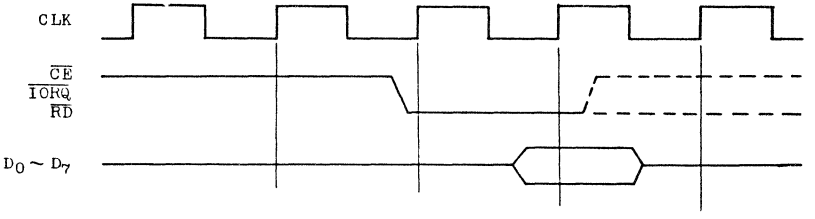


Fig. 3.13 Readout Timing from the Readout Register of DMA

(2) When DMA is the bus master:

(a) Transfer

Transfer and transfer/search operations are performed at the same timing.

Data is latched at the rising edge of RD signal (in case of the standard timing, the falling edge of T3 state) and held on the data bus during next write cycle. After RD signal becomes "1", the data bus buffer of DMA is enabled.

The standard timing is 3 clock cycles for the memory operation while it is 4 clock cycles for the I/O operation. In addition, in the I/O operation, the timing is 4 clock cycles including TW* which is automatically inserted between T2 and T3 state.

When CE/WAIT signal is programmed as "Multiplex" in the write regiser WR5, DMA samples the status of this signal at the falling edge of T2 in case of the memory readout and at the falling edge of TW* in case of the I/O write. If WAIT signal is at "0" level at this time, DMA inserts one clock cycle (Tw) and if it is at "1" level, proceeds to next cycle. Further, when Tw is inserted, WAIT signal is sampled again during this period and the same processing is performed.

o Memory to I/O

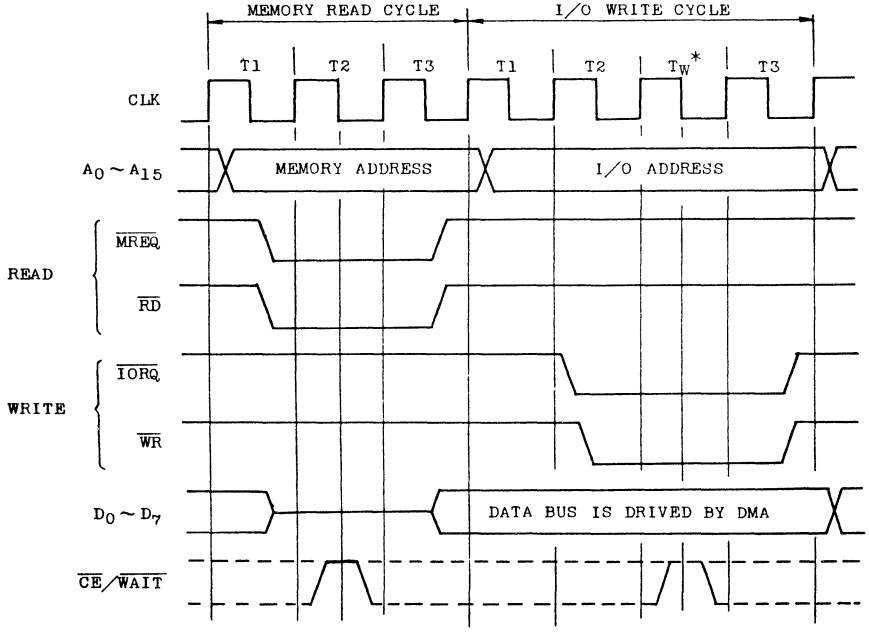


Fig. 3.14 Transfer Standard Timing of Memory to I/O

In the memory readout, DMA put the memory address on the memory bus (A0 to A5) in the period of T1 rise and bring MREQ and RD signals to "0" level at the falling edge of T1 state. The memory data is read out at this point of time, put on the data bus (D0 to D7), latched by DMA at the falling edge of T3 immediately before the rise of RD signal, and when RD signal becomes "1" level, DMA data bus buffer is enabled and the latched data is output on the data bus.

In the I/O write cyle, DMA put I/O address on the address bus in the T1 rise operiod, makes IORQ signal and WR signal to "0" level in the T2 rise period, and writes the data on the data bus (data readout from the memory) into I/O.

o I/O to memory

In the I/O readout cycle, DMA put I/O address on the address bus in the T1 rise period and makes IORQ signal and RD signal to "0" in the T2 fall period. I/O data is read out and placed on the data bus at this time, and is latched by DMA at the trailing edge of T3 immediately before the rise of RD signal. When RD signal becomes "1" level, DMA data bus buffer is enabled and the latched data is output on the data bus.

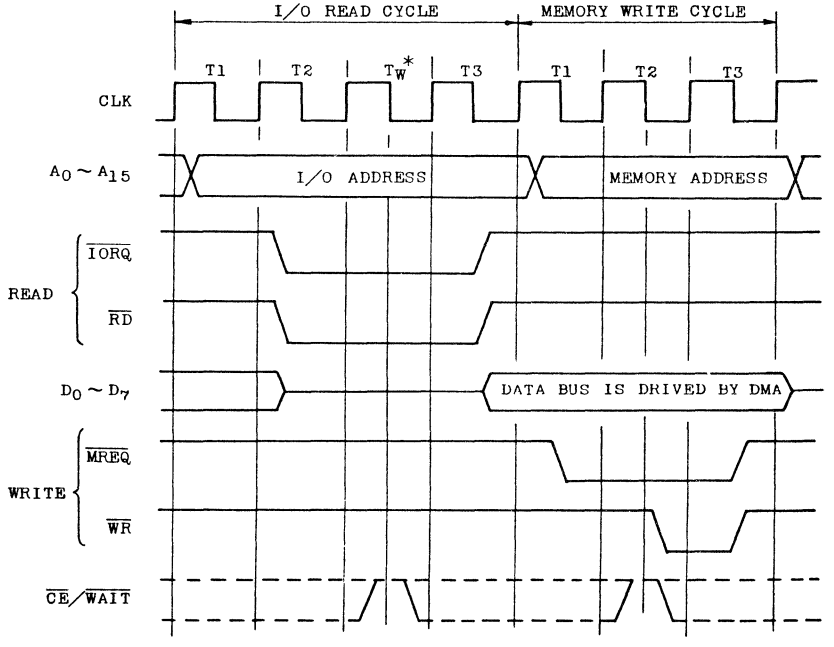


Fig. 3.15 Transfer Standard Timing of I/O to Memory

In the memory write cycle, DMA places memory address on the address bus in the T1 fall period, makes MREQ signal to "0" level at the falling edge of T1 and WR signal to "0" level in the T2 rise period, and write data on the data bus (data readout from I/O) into the memory.

o Memory to memory
This operation is a combined operation of the memory read cycle and memory write cycle.

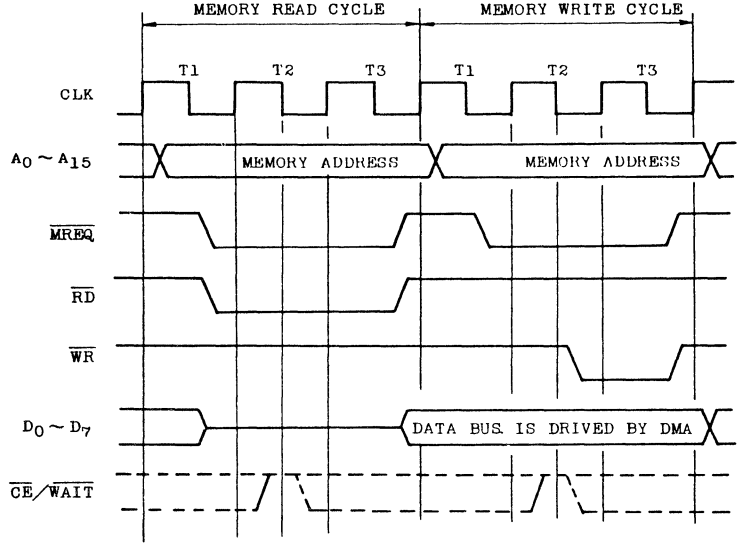


Fig. 3.16 Transfer Timing of Memory to Memory

o I/O to I/O
This operation is a combined operation of the I/O read cycle and I/O write cycle.

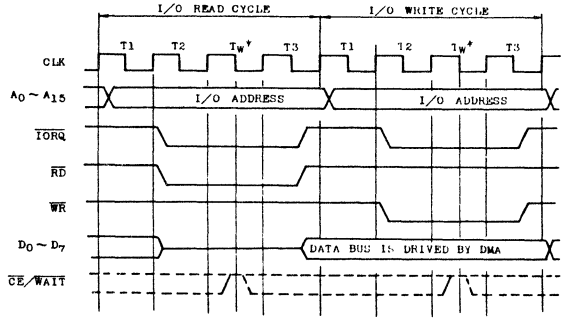


Fig. 3.17 Transfer Timing of I/O to I/O

(b) Search timing
The search operation is identical to the readout only operation and data is only read into DMA register for comparison with coincided byte. The timing of search operation is identical to that of memory to I/O transfer shown in Fig. 3.14 and that of I/O to memory transfer in Fig. 3.15.

(c) Simultaneous transfer
The simultaneous transfer operation and the simultaneous transfer/search operation are performed in the same timing.
When DMA is programmed in the search only mode, the read and write cycles are generated in one read cycle (source port readout period). Since only one address is generated on the address bus, the memory or I/O control signal is generated using an external logic circuit and DMA operation is performed according to this control signal. In addition, I/O ports are selected by hardware during the operation. Signals with (EXT) shown in Fig. 3.18 through Fig. 3.21 are those generated by an external logic circuit.

o Memory to I/O (Memory search cycle)
In this data transfer, the memory search mode is programmed and the memory readout and I/O write are performed in one read cycle by generating IORQ signal and WR signal in the memory readout cycle using an external logic circuit. The hardware performs the memory readout by MREQ signal and RD signal that are output by DMA and the I/O write by IORQ signal and WD signal that are generated using an external logic circuit.

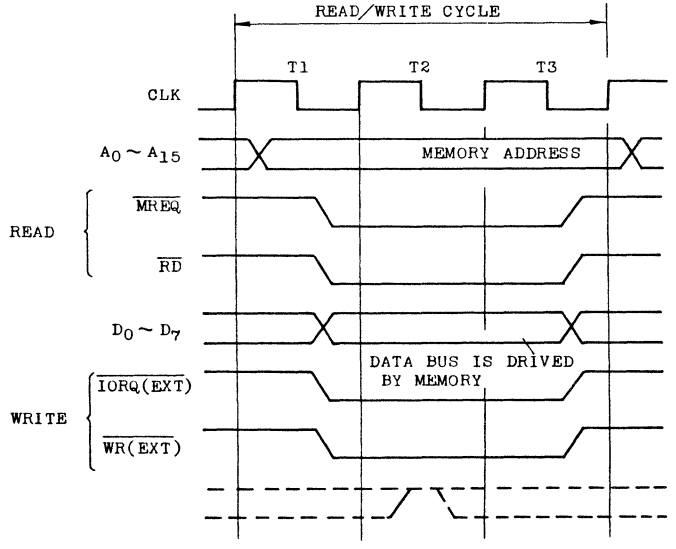


Fig. 3.18 Simultaneous Transfer Timing of Memory to I/O (Memory research timing)

o I/O to memory (Memory search cycle)
In this data transfer, the memory search mode is programmed and the I/O read and memory write operations are performed in one readout cycle by generating IORQ signal and WR signal in the memory readout cycle using an external logic circuit. The hardwaer performs the I/O readout using RD signal output by DMA and IORQ signal generated by an external logic circuit and the memory write using MREQ signal generated by DMA and WR signal produced by an external logic circuit.

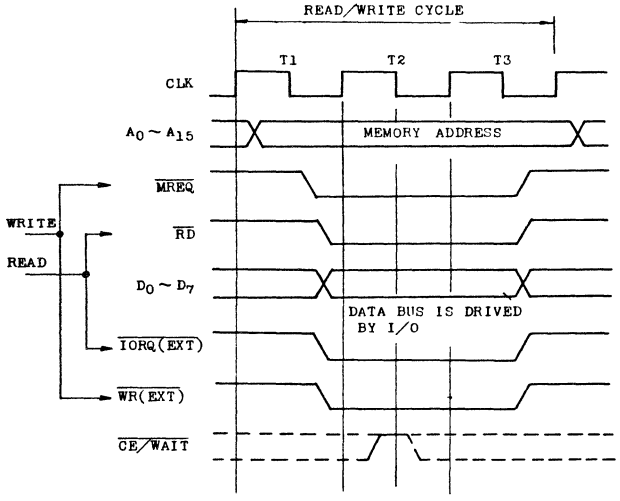
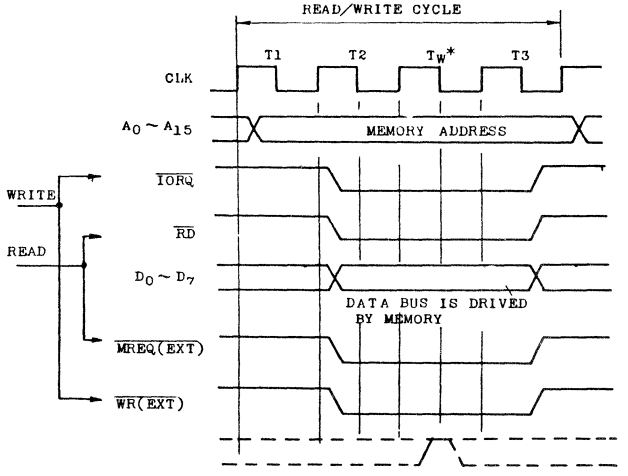


Fig. 3.19 Simultaneous Transfer Timing of I/O to Memory (Memory research timing)

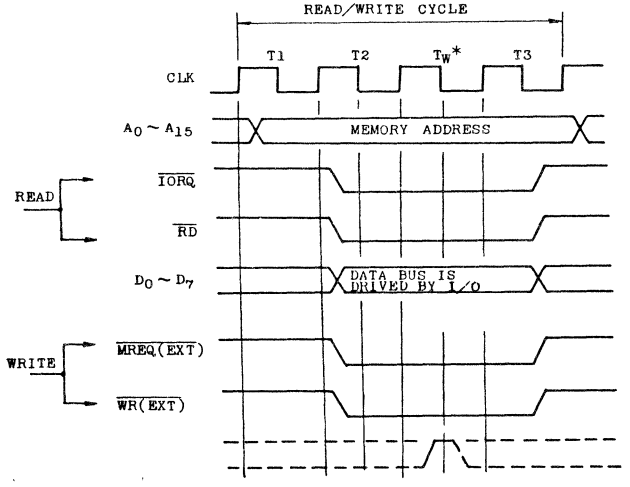
o Memory to I/O (I/O search cycle)
In this data transfer, the I/O search mode is programmed and the memory read and I/O write operations are performed in one readout cycle by generating MREQ signal and WR signal in the I/O readout cycle using an external logic circuit. The hardwaer performs the memory readout using RD signal output by DMA and MREQ signal generated by an external logic circuit and the I/O write using IORQ signal generated by DMA and WR signal produced by an external logic circuit.

o I/O to memory (I/O search cycle)
In this data transfer, the I/O search mode is programmed and the I/O read and memory write operations are performed in one readout cycle by generating MREQ signal and WR signal in the I/O readout cycle using an external logic circuit. The hardwaer performs the I/O readout using IORQ and RD signals output by DMA and the memory write using MREQ signal and WR signal produced by an external logic circuit.



(Note) Although addresses on A0 - A15 are originally I/O addresses, they are handled as memory addresses.

Fig. 3.20 Simultaneous Transfer Timing of Memory to I/O (I/O search timing)



(Note) Although addresses on A0 - A15 are originally I/O addresses, they are handled as memory addresses.

Fig. 3.21 Simultaneous Transfer Timing of Memory to I/O (I/O search timing)

(d) Bus request timing

When RDY signal becomes active, DMA samples RDY signal at the rising edge of the clock and if the bus is not full (BUSREQ = "1") DMA makes BUSREQ signal to "0" level at the rising edge of next clock and request MPU to hand over the system bus control right.
MPU samples BUSREQ signal at the rising edge of the last state clock of the machine cycle which MPU is executing at that point of time and if it is "0", makes BUSACK signal to "0" level at the rising edge of next clock.

Therefore, maximum value of a time required for MPU to hand over the bus control right to DMA (BUSACK = "0") after DMA detected that RDY signal becomes active is the sum of one machine cycle (variable) and one clock period of MPU.
When detecting that BAI (BUSACK) signal is at "0" level for 2 clock period, DMA start the DMA action. There is the delay time of max. One machine cycle + 3 clock period after RDY signal becomes active till the DMA action is actually started.

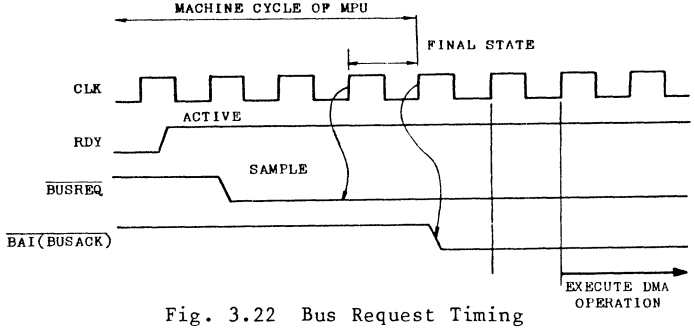


Fig. 3.22 Bus Request Timing

(e) Bus release timing - byte mode

In the byte mode, DMA makes BUSREQ signal to "1" level at the rising edge of the clock immediately before end of each data transfer cycle (the end of readout cycle in the search operation and the end of write cycle in the transfer and transfer/searach operation.)
Although BUSREQ signal becomes "1" before the end of DMA cycle by one clock, MPU resumes the operation one clock after BUSREQ signal becomes "1" level and therefore, there will be no trouble.
After the bus is released, next bus request is made at the leading edge of the clock immediately after both BUSREQ signal and BAI signal becomes "1" level. RDY signal being active is the conditions for this.

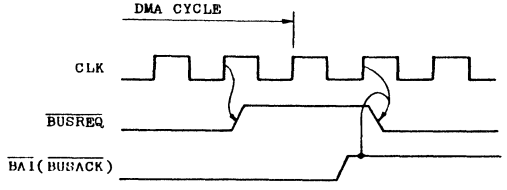


Fig. 3.23 Bus Release Timing - Byte Mode

(f) Bus release at the end of block in the busrst mode or continuous mode
When it is programmed to stop DMA at the end of block in the burst mode or continuous mode, BUSREQ signal is set to "1" level at the rising edge of the clock at the end of last data transfer. This last data is transferred even when RDY signal becomes non-active.

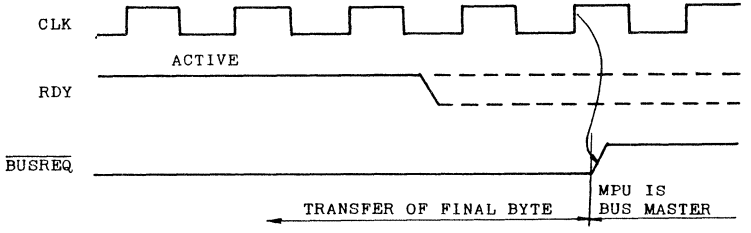


Fig. 3.24 Bus Request Timing - at End of Block

(g) Bus release when coincidence is detected in the burst mode or continuous mode
When DMA is set in the burst mode or continuous mode and programmed to stop its operation at byte coincidence, DMA stops to operated when the byte coincidence is detected.
Since DMA operation is pipelined and the advance reading is performed, a check to determine if the n th data coincides with the coincidenced byte is carried out at the same time when the n + 1 st data is transferred. Therefore, data of N + 1 byte is transferred and BUSREQ signal is set to "1" level at the leading edge of the clock when this transfer ended.

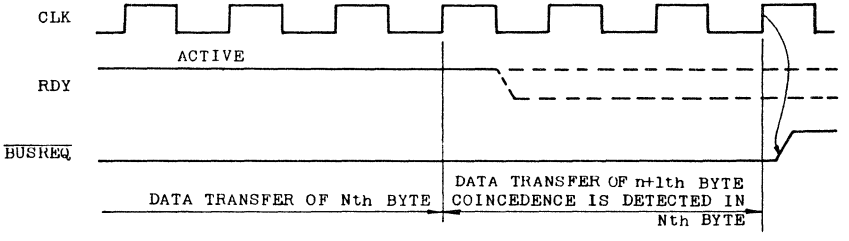


Fig. 3.25 Bus Release Timing - Byte Mode

(h) Bus release when RDY signal is non-active
If RDY signal becomes non-active in the burst mode, BUSREQ signal is set to "1" level at the rising edge of next clock after end of the byte operation that is under execution at the time. For instance, this is done when the read of the search only or simultaneous transfer/search operation ended or when the write of the transfer/search operation ended. Therefore, the action for BUSREQ signal is slightly behind the action for RDY signal.

DMA always does not release the bus until the byte action at the time is completed.

In contrast with this, in the continuous mode BUSREQ signal is kept at "0" level even when RDY signal becomes non-active.
In addition, after the byte action at the time ended DMA is put in the idle state until RDY signal becomes active again.
This figure is shown in Fig. 3.26.

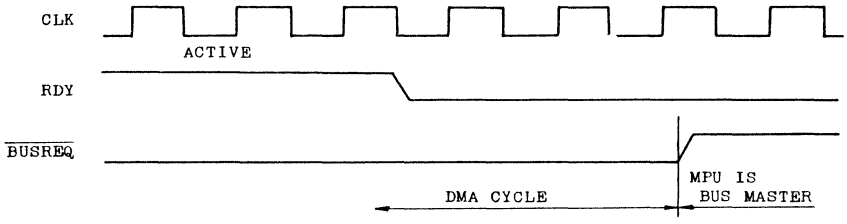


Fig. 3.26 Bus Release Timing when RDY Signal becomes Non-active

Timing of RDY signal with other signals are shown in Figs. 3.27, 3.28 and 3.29. In these figures the memory search only operation by the Z80 standard timing by mode is assumed. In each of the operation modes, RDY signal is sampled at the rising edge of the last clock of the read or write cycle to determine its level.

RDY signal can become non-active before completion of the last byte operation without affecting its operation. In the byte or burst mode, BUSREQ signal and BAI signal are set to "1" at the end of byte operation of RDY signal. In the byte or burst mode, the bus control signals (MREQ, IORQ, RD, WR) are also kept at "1" level as long as RDY signal is non-active. Further, the address bus and data bus are kept in 3 state.

The continuous mode differs from other modes in that the address bus holds an address which is incremented in advance against next byte during the period when RDY signal is non-active. This address can be used immediately after RDY signal becomes active again.

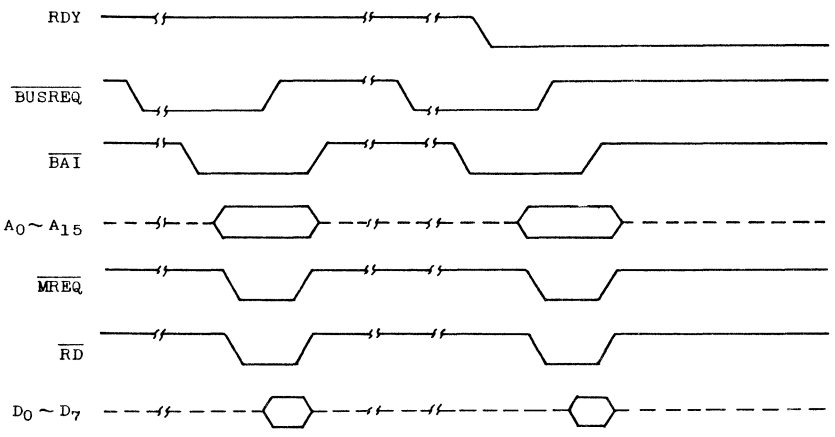


Fig. 3.27 Timings of RDY signal with other signals

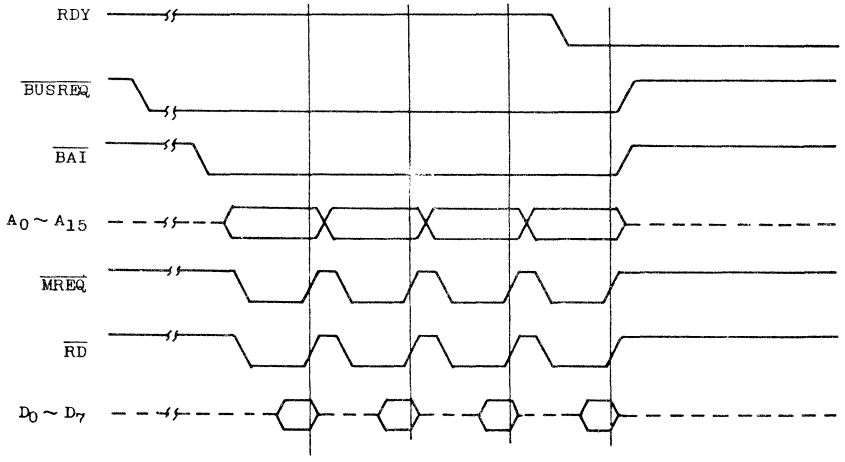


Fig. 3.28 Timings of RDY signal with other signals (Bus mode)

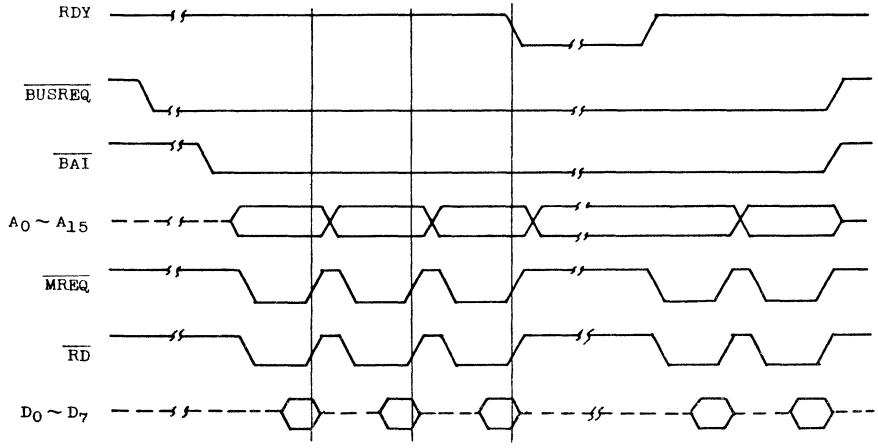


Fig. 3.29 Timings of RDY signal with other signals (Continuous mode)

(i) Variable cycle

When programmed, DMA is capable of changing read and write cycle lengths. Source and destination can be programmed independently by the write register WR1 (designation of Port A) and WR2 (designation of Port B). This variable cycle function allows the read or write in 2, 3 or 4 clock cycles (more clock cycles if Tw is inserted) and further, can increase or decrease pulse widths of all signals generated by DMA. Four signals relative to the data transfer; MREQ, IORQ, RD and WR signals have the function to end the rising edge timing earlier by 1/2 clock independently.

Differing from the standard timing, in the variable cycle mode IORQ signal becomes active earlier than MREQ, RD and WR signals by 1/2 clock. Further, CE/WAIT signal can be used in the extension of 3 or 4 clock cycle variable memory cycle and 4 clock cycle variable I/O cycle only. In the 3 or 4 clock cycle memory operation, CE/WAIT signal is sampled at the T2 falling edge while it is sampled at the T3 falling edge in the 4 clock cycle I/O operation. In the 2 clock cycle operation it is not sampled. Use of this variable cycle is effective in increasing data transfer rate and reducing software burden and further, can eliminate an external logic circuit. In addition, this function provides more faster memory read/write speed than normal speed.

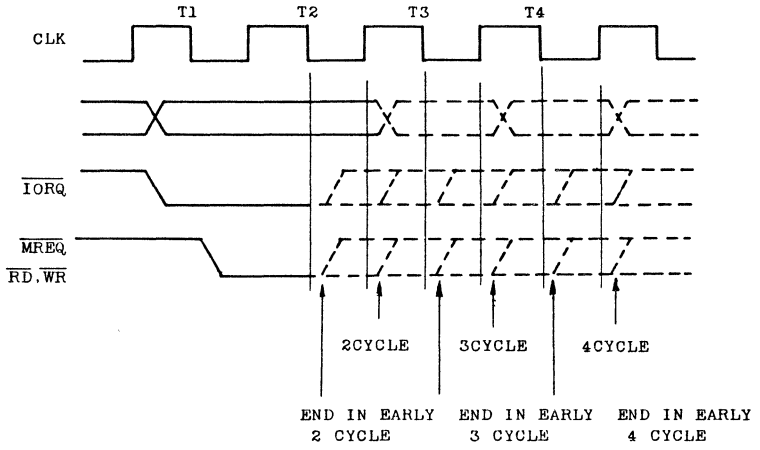


Fig. 30 Variable Cycle

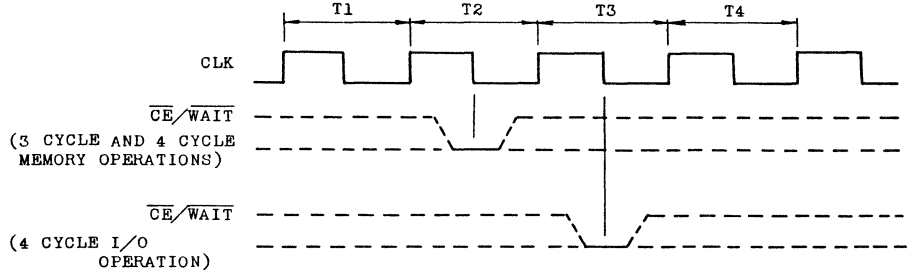


Fig. 31 $\overline{\text{WAIT}}$ Sample in Variable Timing

(j) Interrupt

The timing for the interrupt acknowledge or return from interrupt is identical to that of other Z80 peripheral LSI's. INT signal is sampled by MPU at the rising edge of the last clock of all commands. If the interrupt enable is not set by the internal MPU software or when BUSREQ signal is active, this INT signal is not accepted. When INT signal is accpeted, IORQ signal also becomes active at the same time (normally, MREQ signal) in the period of its M1 cycle, indicating that the interrupting LSI can load its 8-bit vector on the data bus. At the same time, two wait status are automatically inserted into this cycle. This is to facilitate execution of the priority interrupt mechanism and the wait status of 2T gives a stabilizing time to IE1 and IEO signals and thus, it becomes possible to identify which peripheral LIS will react.

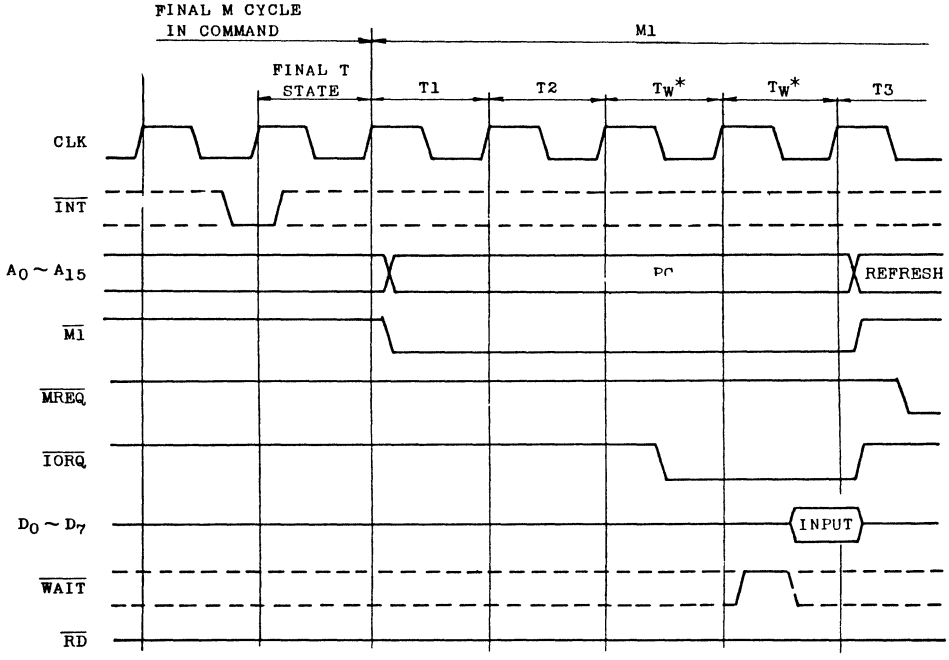


Fig. 3.32 Interrupt Acknowledge

Interrupt on RDY signal (interrupt before the bus request) does not directly affect BUSREQ signal. The process in this case is carried out by giving following commands to the write register WR6 in the interrupt service routine.

- o Enable after interrupt return (B7H)
- o DMA enable (87H)
- o Execution of RETI command to reset IUS latch during the interrupt service in the Z80 DMA (ED4DH)

(k) Pulse generation

In the pulse generation, INT signal is set to "0" level (pulses are generated on the INT line) every 256 bytes after offset value is loaded to the write registger WR4 by the program.
INT signal is put to "0" level during the DMA cycle in which pulse control bytes coincide with low order bytes of the byte counter and kept at "0" level in the full period of transfer cycle. Here, the transfer cycle means the read cycle (the search only or simultaneous transfer operation) or read/write cycle and lengths of the read and write cycles can be set independently by variable cycle.

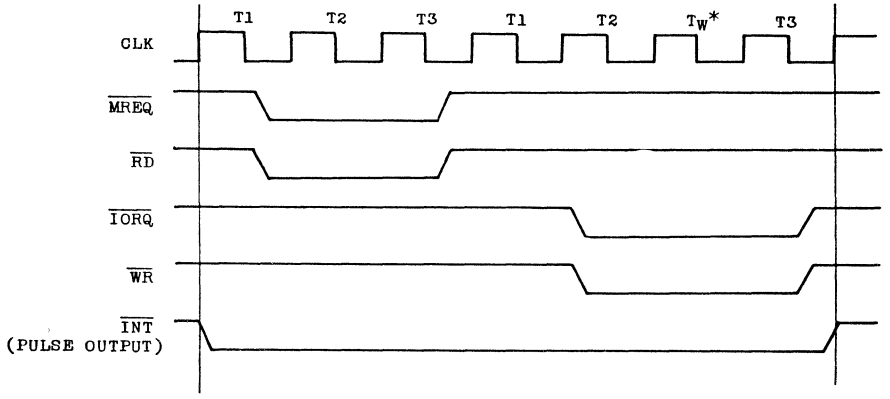


Fig. 3.33 (a) Pulse Output (Standard timing at the time of transfer)

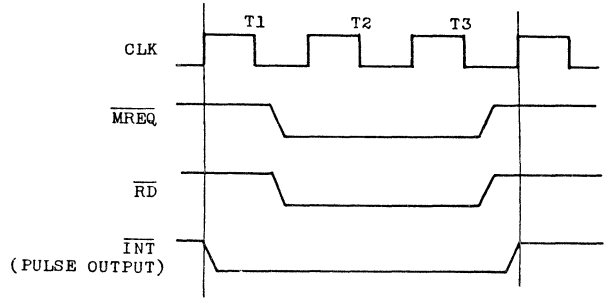


Fig. 3.33 (b) Pulse Output (Standard timing at the time of memory search)

(1) Precautions

1] Transfer timing

Although the DMA transfer timing is basically identical to the read/write timing of the Z80 MPU, care is required when variable cycle is used or in case of simultaneous transfer.

In the case of simultaneous transfer, all addresses which are output by DMA are interpreted to be memory addresses and I/O are selected by the hardware using an external logic circuit. It is normally programmed that I/O addresses are fixed and memory addresses are updated during the DMA operation. At this time, DMA controls memory addresses and outputs I/O select signal using an external logic circuit.

2] Memory refresh
Since DMA has no refresh signal output function, the refresh of a dynamic RAM is performed normally using RFSH signal of MPU. If the transfer period becomes long in the DMA operation using the burst mode or continuous mode, another refresh method must be used.

3] Pulse generation
When the pulse generating function is used for transfer in the byte mode, pulse output is generated in two times. This is to avoid BAI signal from becoming non-active and MPU from being put in HALT state. Further, when offset value and low order 8 bits of the block length are equal other, pulse is once generated and after DMA operation is completed, pulse is generated during the read cycle of the 1st byte when the DMA operation is performed again without changing the offset value.

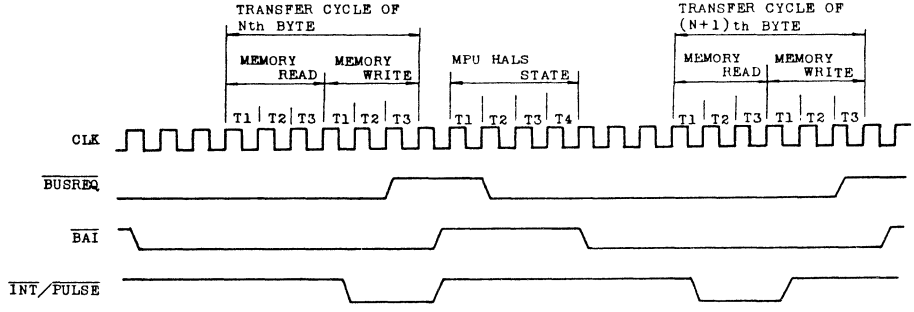


Fig. 3.34 Pulse Generation Timing (at Byte mode)

3.4 Peripheral commands
To operate DMA, specify its operations by writing into the control register group through programming. In addition, the status of DMA can be known by reading the contents of the status register group.
To give effect to this on a program, write the operation into the write register by OTIR or OUT command to MPU and read out by INIR or IN command. In both cases, output of the I/O address decoder to DMA becomes "0" level. This output is connected to the CE/WAIT pin.
The configurations of the control register group and status register group are as follows:

(1) Control register group
1] Write register WR0
2] Write register WR1
3] Write register WR2
4] Write register WR3
5] Write register WR4
6] Write register WR5
7] Write register WR6

(2) Status register group
1] Readout register RR0
2] Readout register RR1
3] Readout register RR2
4] Readout register RR3
5] Readout register RR4
6] Readout register RR5
7] Readout register RR6

3.4.1 Control register group

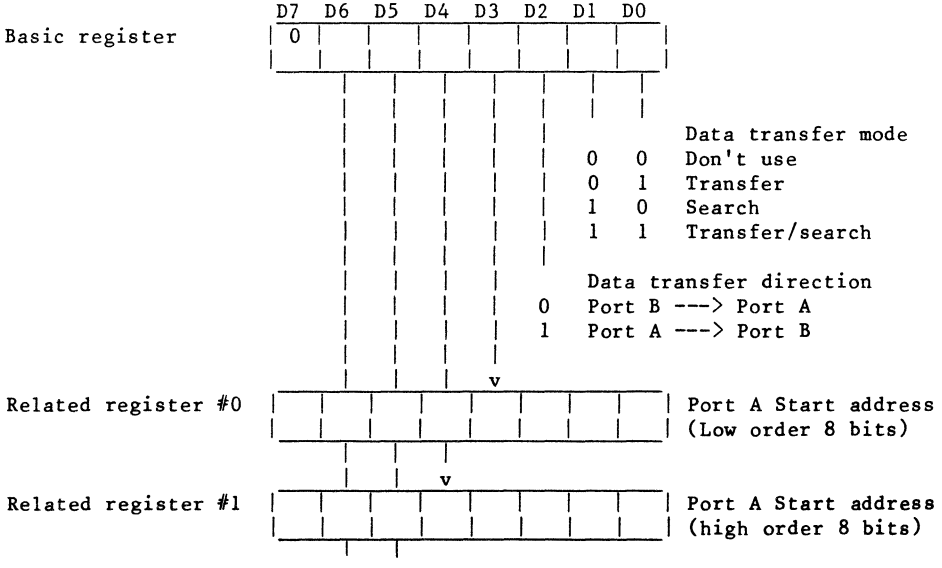
The control registers consist of 7 groups of WR0 to WR6, each of which consists of a basic register and related registers. If the pointer bit of the basic register is "1", related registers are accessed by turns. The basic registers WR0 to WR6 are identified by the combination of bits 0, 1, 2, 6 and 7. There may be pointer bits for related registers. BBH (followed by the readout mask) command of WR6 has no pointer bit but data that follows this command is limited to the readout mask.

(1) Write register WR0

WR0 is idnetified by the condition that Bit 7 of the basic register is "0" and Bit 1, 0 are other than both "0".
WR0 has 4 pointer bits, each of which has related registers, respectively.

(a) Basic register bit 0, 1 (Designation of operating class)

Bit 0 and 1 designate the operating class; transfer, search only, and transfer/search operaitons. In addition, simultaneous transfer or transfer/search is obtained by selecting search and generating a proper bus control signal for complete transfer through external hardware.



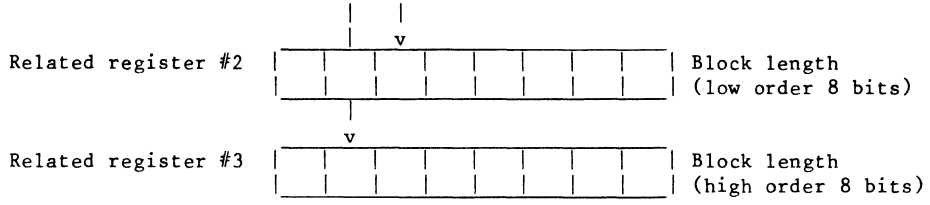


Fig. 3.35 Write Register WR0

(b) Basic register bit 2 (Designation of data transfer direction)
Data transfer direction is designated when the source port and destination port at time of the transfer only operaiton by Bit 2. In the search only operation, the source port only is designated and in the simultaenous transfer or transfer/search operation, the destination port is decided by external wiring.

(c) Basic register bit 3 - 6 (Pointer bits)
Bit 3 - 6 are the pointer bits which are used to designate four related registers following respective bits.

(d) Related register #0, #1 (Port A start address)
These registers are accessed by Bit 3 and 4 of the basic register byte. When Port A is used as a source or destination, it is necessary to write the start address. Low order bytes are written into #0 and high order bytes in #1.

(e) Related register #2, #3 (Block length)
These registers are designated by Bit 5 and 6 of the basic register. Max. 64K bytes can be designated by writing low order bytes of block length into #2 and high order bytes into #3. However, as data read is pipe line type, number of bytes actually searched or transferred is more than that entered here by 1 or 2. In addition, if "zero" is set for these registers, the transfer or search of 2**16+1 bytes is carried out.

(2) Write register WR1
WR1 is idnetified by the condition that all of Bits 0, 1 and 7 of the basic register are "0" and Bit 2 is "1".

(a) Basic register bit 3 (Port A designation)
A memory is designated by Port A when "0" is written for Bit 3, while I/O is designated when "1" is written. This designation makes the control signal (MREQ or IORQ) active against the cycle including this port.

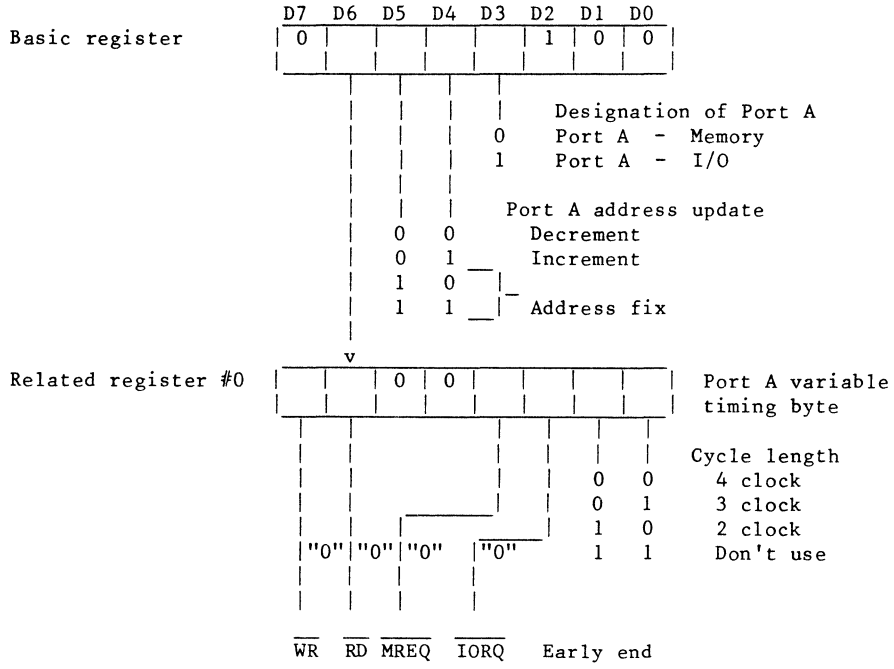


Fig. 3.36 Write Register WR1

(b) Basic register Bit 4, 5 (Fixed or variable address designation)
Fixed or variable Port A address is designated by Bit 4 and Bit 5 for each transfer or search byte.

(c) Basic register Bit 6 (Pointer bit)
When Bit 6 is set to "1", next related register is accessed. In addition, when Bit 6 is set to "0", DMA's variable cycle is not used.

(d) Related register #0 (Port A variable timing byte)
. By setting values for this register, Port A cycle length and control signal timing can be designated.
- o Bit 0, 1 (Cycle length)
  Length of data transfer cycle (memory read/write, I/O read/write) relative to Port A is designated. Timing can be changed in a range of 2 - 4 clocks.
- o Bit 2, 3, 6, 7 (Early end)
  The timing of the control signal IORQ, MREQ, RD and WR can be advanced by 1/2 clock.

(3) Write register WR2
WR2 is idnetified by the condition that all of Bits 0, 1, 2 and 7 of the basic register are "0"

(a) Basic register bit 3 (Port B designation)
A memory is designated by Port B when "0" is written for Bit 3, while I/O is designated when "1" is written. This designation makes the control signal (MREQ or IORQ) active against the cycle including this port.

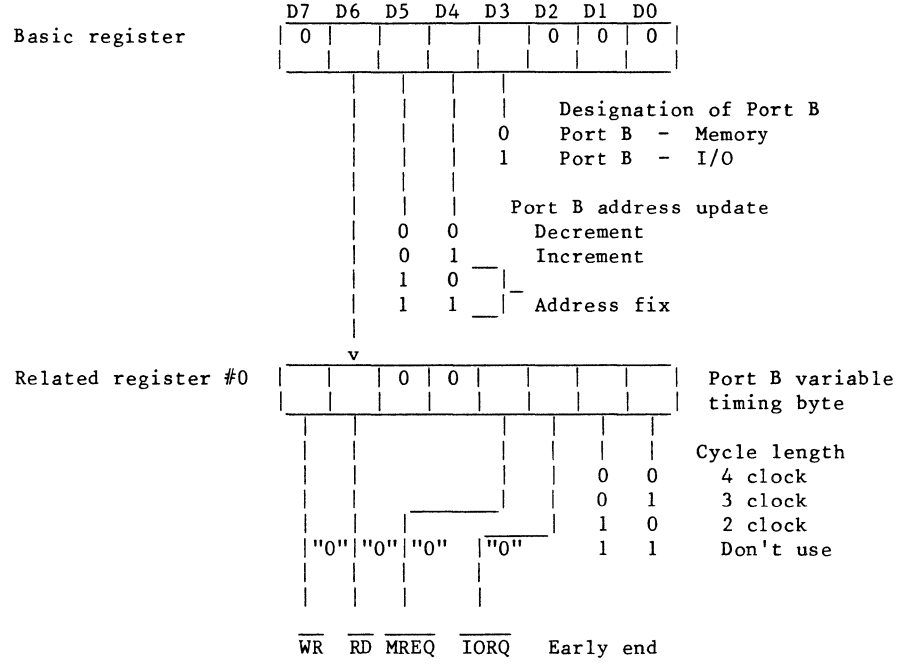


Fig. 3.37 Write Register WR2

(b) Basic register Bit 4, 5 (Fixed or variable address designation)
Fixed or variable Port B address is designated by Bit 4 and Bit 5 for each transfer or search byte.

(c) Basic register Bit 6 (Pointer bit)
When Bit 6 is set to "1", next related register is accessed. In addition, when Bit 6 is set to "0", DMA's variable cycle is not used.

(d) Related register #0 (Port B variable timing byte)
By setting values for this register, Port B cycle length and control signal timing can be designated.

- o Bit 0, 1 (Cycle length)
  Length of data transfer cycle (memory read/write, I/O read/write) relative to Port B is designated. Timing can be changed in a range of 2 - 4 clocks.
- o Bit 2, 3, 6, 7 (Early end)
  The timing of the control signal IORQ, MREQ, RD and WR can be advanced by 1/2 clock.

(4) Write register WR3
WR3 is identified by the condition that both Bit 0 and Bit 1 of the basic register are "0" and Bit 7 is "1".

(a) Basic register Bit 2 (Stop on match)
This bit is used for the search or transfer/search operation. When this bit is "1" and transferred data matches the match byte, the data transfer is stopped and the bus is released. When this bit is "0" and transferred data matches the match byte (if DMA is not stopped even when they matched), the status flag is set on the status byte to allow interrupt resulting from byte match.

(b) Basic register Bit 3 (Pointer bit)
When this bit is set at "1", the mask byte follows the basic register.

(c) Basic register Bit 4 (Pointer bit)
When this bit is set at "1", a match byte follows the basic register. This bit designates a match byte used for comparison with all data to be searched.

(d) Basic register Bit 5 (Interrupt enabled)
When this bit is set at "1", DMA interrupt is enabled.

(e) Basic register Bit 6 (DMA enable)
When this bit is set at "1", DMA operation is enabled and a bus request can be made to MPU.

(f) Related register #0 (Mask byte)
This register is accessed by basic register Bit 3. It is possible to write a mask byte required for the search operation. The mask byte is capable of masking the match byte (data to be compared) during the search operation to extract bits to be compared.
When all bits of the mask byte are at "0", the comparison is made and when they are at "1", the masking is made. In addition, if no masking is required and all bits are compared, write 00H mask byte.

(g) Related register #1 (matche byte)
This register is accessed by basic register Bit 4. The match byte is used as data to be comapred when the data transfer mode is search or transfer/search. The match byte is masked by the mask byte of related register #0.

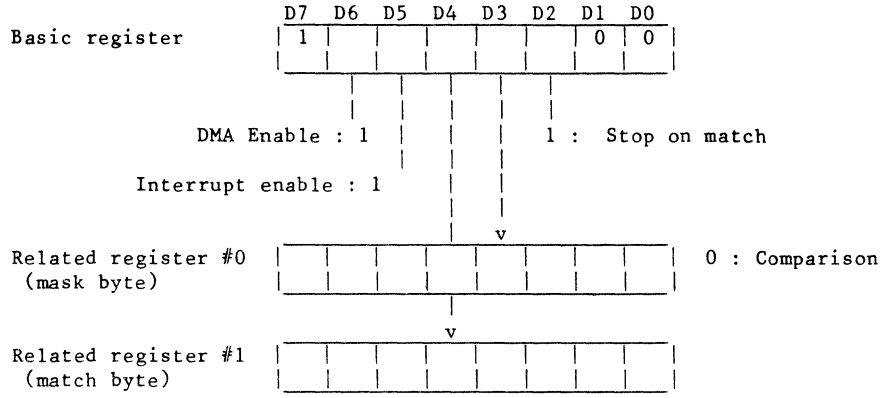


Fig. 3.38 Write Register WR3

(5) Write register WR4
WR4 is identified by the condition that both Bit 0 and Bit 7 of the basic register are "1" and Bit 1 is "0".

(a) Basic register Bit 2 - 4 (Pointer bit)
When these bits are set at "1", the related registers #0 to #2 are accessed after the basic register.

(b) Basic register Bit 5, 6 (Operation mode designation)
Operation mode selected values can be set for Bit 5 and Bit 6. For values to be set, refer to Fig. 3.39.

(c) Related register #0, #1 (Port B start address)
These registers are accessed by basic register Bit 2 and Bit 3. Related register #0 designates low order byte of Port B start address while related register #1 designated high order byte of Port B. Further, if low order 8 bits are sufficient for Port B start address, the loading to related register #1 is not required.

(d) Related register #2 (Interrupt control byte)
This register control DMA interrupt or pulse generation. By setting Bit 3 and Bit 4, related registers #3 and #4 can be accessed.
- o Bit 0 (Interrupt on match)
  When Bit 0 is set at "1", DMA generates interrupt if transferred data matches the match byte in the search or transfer/search operation.
- o Bit 1 (Interrupt on end of block)
  When Bit 1 is set at "1", DMA generates interrupt if a value of the byte counter becomes "0" in DMA operation.
- o Bit 2 (Pulse generation)
  When Bit 2 is set at "1", pulse is generated on the INT line whenever data in number of bytes set on the pulse control byte is transferred.

- Bit 3, 4 (Pointer bits)
  When Bit 3 is set at "1", pulse control byte is accessed after interrupt control byte.
  When Bit 4 is set at "1", the interrupt vector is accessed.
- Bit 5 (Vector value change by status)
  When this bit is set at "1", interrupt vector value changes according to cause for generating interrupt. However, if the automatic restart or interrupt at the end of block was already set, this mode cannot be used.
- Bit 6 (Interrupt on RDY)
  When this bit is set at "1", DMA generates interrupt prior to the bus request if it detects that RDY signal has become active. Therefore, the interrupt enable command becomes necessary and when RETI command is executed after the interrupt enable of WR6 (B7H) is sent out, the bus request is started.

(e) Related register #3 (Pulse control byte)
When Bit 3 of the interrupt control byte is set at "1", the pulse control byte is accessed after the interrupt control byte. The pulse control byte gives offset values to pulse that are first generated (Number of bytes shown by this control byte). The pulse control byte compares low order 8 bits of the byte counter and if both coincide each other, pulses are output on the $\overline{INT}$ line.

(f) Related register #4 (Interrupt vector)
When Bit 4 of the interrupt control byte is set at "1", the interrupt vector is accessed after the interrupt control byte. The interrupt vector is loaded on the data bus at time of the interrupt acknowledge by MPU ($\overline{IORQ}$ = "0", $\overline{M1}$ = "0"). If Bit 5 of the interrupt control byte is set at "1", Bit 1 and Bit 2 of the interrupt vector change according to the interrupt factor. However, when the automatic restart and interrupt on the end of block has been already programmed, the interrupt vector sent out at the end of block does not change and therefore, the mode for vector value change by status cannot be used.

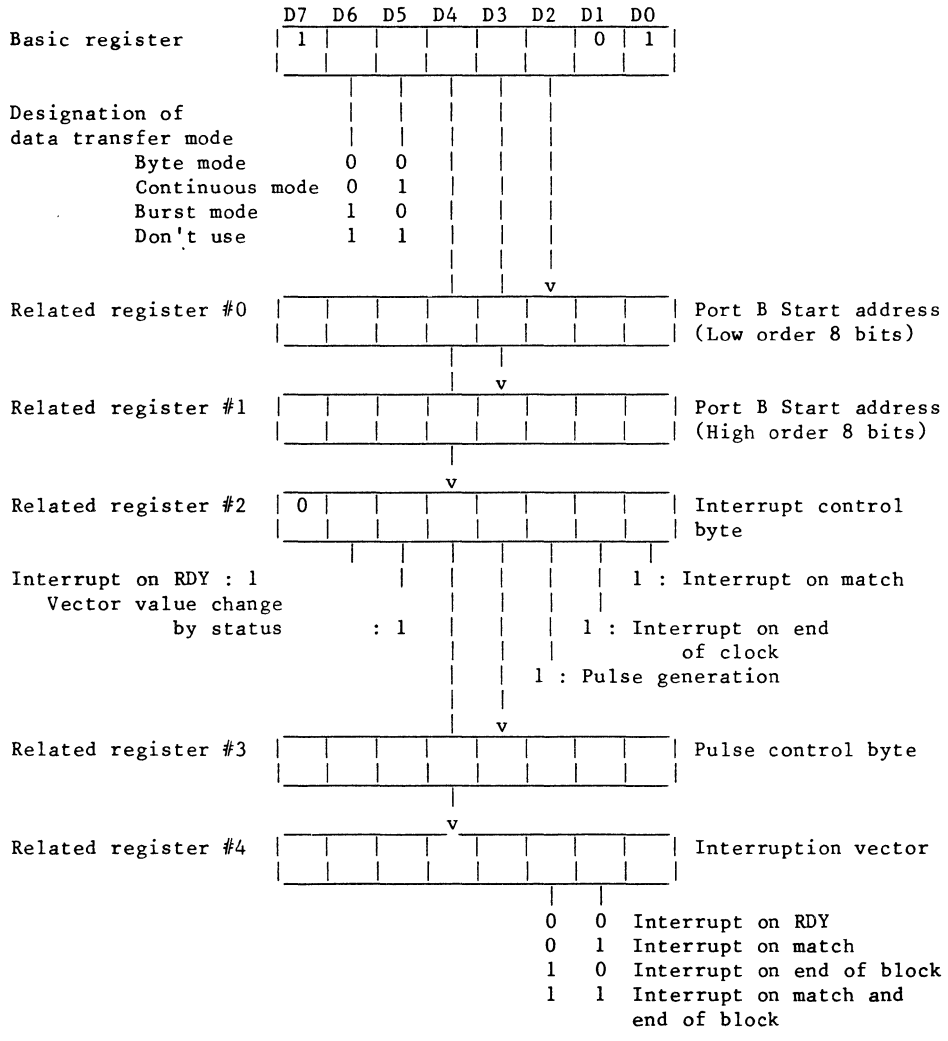


Fig. 3.39 Write Register WR4

(6) Write register WR5

WR5 is identified by the condition that Bit 1 and 7 of the basic register are "1" and Bit 0, 2 and 6 are "0". WR5 has no related register.

o Bit 3 (Effective polarity of RDY signal)

When this bit is set at "0", RDY signal becomes "0" and active, and when it is set at "1", RDY signal becomes "1" and active.

o Bit 4 (Use of CE/WAIT pin)
When this bit is set at "0", CE function only is available. When it is set at "1", both CE and WAIT functions become available. When BUSREQ signal is at "1", CE function is available, while if BUSREQ signal is at "1" level, WAIT function is available.

o Bit 5 (Automatic register)
When this bit is set at "0" level, DMA operation is stopped at time of the end of block (Byte counter = "Zero"). When it is at "1" level, the contents of the address register and byte counter are automatically loaded on the address counter and byte counter, and DMA operation is continued.

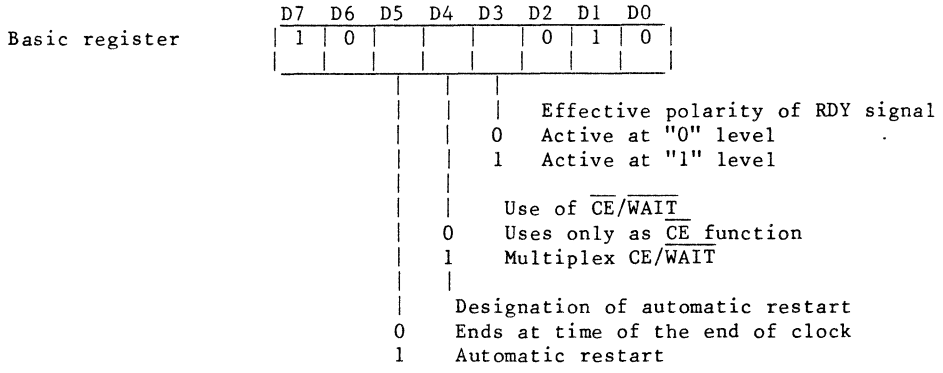


Fig. 3.40 Write Register WR5

(7) Write register WR6
WR6 is idnetified by the condition that Bit 0, 1 and 7 of the basic register are at "1" level. In the case of WR6, the functions (commands) are divided by the combination of Bits 2 to 6.

(a) Reset (C3H)
This command is used to reset DMA. By executing this command, DMA performs the followings;
- o Disables the interrupt control circuit and bus request control circuit.
- o Releases the interrupt latch.
- o Releases the forced RDY condition.
- o Releases the automatic restart condition.
- o Releases CE/WAIT function (Bit 4 WR5) and retians CE function only.
- o Returns the timings of both Port A and B to the Z80 standard timing.

After turning power to DMA ON, and performing the programming, it is necessary to execute the reset command once. In addition, if the DMA operation is interrupted during its execution, it is necessary to execute the reset command 6 times successively (this is because there are 5 related registers that are capable of directing in WR4).

Further, DMA is not always reset completely by this reset command. The read sequence is reset only by the read sequence reset command.

(b) Port A timing reset (C7H)
This command resets Port A variable timing byte and returns Port A timing to the Z80 standard timing.

(c) Port B timing reset (CBH)
This command resets Port B variable timing byte and returns Port B timing to the Z80 standard timing.

(d) Load (CFH)
When this command is excuted, the content of the address register is loaded on the address counter and the byte counter is cleared. In addition, the internal forced RDY condition is also released.
Further, an address counter to which the loading can be made immedaitely is the source port address counter only. The loading to the destination port address counter is made when a value of this counter is initially updated (incremented/decremented) but if "address if fixed", the loading is not performed. However, the loading by the "fixed address destination port programming" technique is possible.
If DMA becomes non-active when the load command is written, another DMA control byte is written before the load command.

(e) Continue (D3H)
Although this command clears the byte counter to "zero", both port address counters do not change. This command is used in transferring several data blocks to continued positions in the many buffer if it is desirable to know a break of every block, and continues DMA operation which has been interrupted by detection of match at the end of block or search. In order to execute this command, interrupt at the end of each blocks is needed and new block length shall be entered in WR0 with the continue command.
In transferring data blocks, interrupt becomes necessary whenever transfer of each data block ended. In transferring next data block after the interrupt, this continuity command is used instead of the load command.

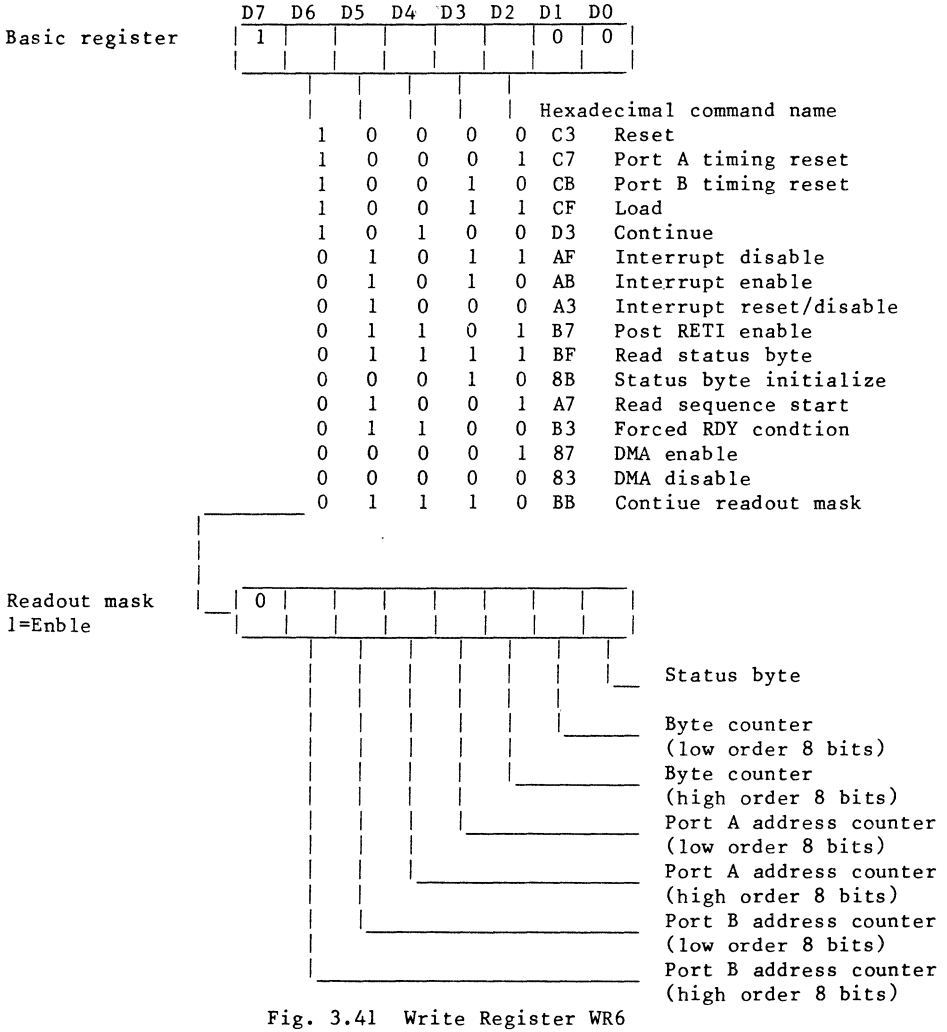


Fig. 3.41 Write Register WR6

(f) Interrupts disable (AFH)

This command is used to simulate the Z80 MPU's interrupt acknowledge when DMA is operated in a system other than the Z80 MPU. When DMA sends the interrupt signal into any MPU other than the Z80 MPU, if the interrupt disable command is written into the beginning of the service routine, INT signal returns to "1" level but next interrut signal of DMA cannot be sent during the service routine is continuously carried out. Generation of next interrupt signal becomes possible when the interrupt enable command is written into the end of the service routine.

(g) Interrupts enable (ABH)
This is a command used on the Z80 system to enable the interrupt when the power source is ON. This command enables the interrupt control circuit of DMA. When the interrupt disable command is not used, if the interrupt enable command is once written, next interrupt is enabled automatically when RETI command is executed at the final stage of the interrupt service routine. However, if the interrupt disable command is used, it becomes necessary to write the interrupt enable command at the final stage of the interrupt service routine.

(h) Interrupt reset and disable (A3H)
This command is used on such systems as 8080 and 8085 to interface DMA and MPU which is povided with the interrupt acknowledge function but has no RETI command. This command, when executed, performs the followings:

- o Reset of the in-interrupt service routine (IUS) latch
- o Reset of the interrupt pending (IP) latch
- o Release of the internal forced RDY signal conditions
- o Succeeding interrupt disable by DMA (same as the interrupt disable command)

(i) Enable after RTEI (B7H)
This command is used only when "interrupt on RDY signal" is programmed on WR4. DMA, when detecting that RDY signal becomes active, does not make the bus request but generates the interrupt signal. After the interrupt return, this command enables DMA to make the bus request again. This command is always used to make the bus request after the interrupt to RDY signal on the Z80 MPU system. This command also can be used on other MPU's, for instance, 8080.
The interrupt latch (IOR) to RDY signal is set during its interrupt cycle. This latch makes RDY signal active and DMA is not allowed to make the bus request until this latch is reset by post-RETI enable command.
The execution sequence of the Z80 MPU service routine is as follows and the bus request is mode after RETI command is executed:

```
      :
      :
  Post RETI Enable
  DMA Enable
      :
      :
  RETI Command
```

(j) Read status byte (BFH)
This command indicates that next read command is the status byte access.

(k) Status command initialization (80H)
This command indicates the reinitialization of bit 4 and 5 of the status byte.

The reinitialization of the interrupt pending status (Bit 3) of the status byte can be effected by the interrupt acknoweledge, interrupt process, interrupt reset and disable command writing. The reinitialization of DMA operation status (Bit 0) can be efected by the load command.

(l) Read mask continue (BBH)
This command denotes that next control byte which is to be written into DMA follows the read mask register. The read mask register is used for setting a new read sequence of RR0 to RR6 and is normally a part of the initial state setting when the power source for DMA is turned ON.
The read mask can be programmed by setting the related pointer bit of register to be read out "1" level. The read sequence start command is used for initialization.

(m) Read sequence initiote (A7H)
This command is used to initiate the read sequence pointer command as a measures to access the first (in low order) read register that is designated to be readable by the read mask for initialization of DMA by next MPU read command. Normally, this command is output to reset the read sequence immediately after loading of the read mask.

(n) Forced RDY (B3H)
In the burst mode or continuous mode, this command is used to make the internal RDY conditions active for the active RDY signal by an external logic circuit. This command is used for memory-to-memory transfer or memory search where RDY signal is not required. It is not necessary to consider the effective polarity of RDY signal. Use of this command can eliminate an external logic circuit.

The forced RDY conditions are released by the following commands/ conditions:

- o Reset command
- o Load command
- o Interrupt reset and disable command
- o Ending by end-of-block
- o Ending by byte match
- o Bus release by DMA

(o) DMA enable (87H)
This command is used to enable the bus control circuit of DMA. The interrupt circuit is not affected nor the function and latch are reset. This bus request enable function is identical to that of Bit 6 of WR3. In the interrupt service routine, DMA enable command is the last command to DMA before MPU executes RETI command.

(p) DMA disable (83H)
This command inhibits the bus request by DMA. This command is used to stop DMA operation by external events, end-of-block or match by bytes and when reinitialization of the status byte is required.

3.4.2 Status register group

There are 7 read registers RR0 to RR6 available for DMA to know the operation execution or end status.

The readout of MPU is made according to the method to access DMA as the peripheral I/O using I/O command. Commands to be written into DMA are as follows:

1] Read status byte (BFH)
2] Read sequence initiate (A7H)
3] Status byte rinitialize (8BH)
4] Read mask continue (BBH)

The above commands are those which are shown for WR6.

(1) Read register RR0 - Status byte

(a) Bit 0 (DMA operation)
This bit indicates if DMA made the bus request after the last LOAD command. "1" indicates that DMA made the bus request while "0" indicates no bus request made.

(b) Bit 1 (RDY signal active)
"0" of this bit indicates that RDY signal is active. "1" indicates RDY signal being non-active.

(c) Bit 2 (Don't care)

(d) Bit 3 (Interrupt pending)
This bit indicates the interrupt pending (IP) latch status. "0" indicates the interrupt pending.

(e) Bit 4 (Match detection)
When this bit is "0", it indicates the match after the last status byte reset or reinitialization command.

(f) Bit 5 (End-of-block detection)
When this bit is "0", it indicates the end-of-block reached after the last status byte reset, load, continuity or reinitialization.

(g) Bit 6, 7 (Don't care)

(2) Read register RR1, RR2 - Byte counter
The 16-bit counter consisting of two register RR1 and RR2 are cleared to zero by the load, continuity or reset command. When DMA starts the transfer or search, the byte counter is incremented by one at the end of each read cycle and judges the end-of-block by comparing with the program content of the block length register (WR0), when match is detected, DMA operation is stopped. If the pulse generation is used at this time, the content of the WR4 pulse control byte is, after transferred, compared with low order4 byte (RR1) of the byte counter.

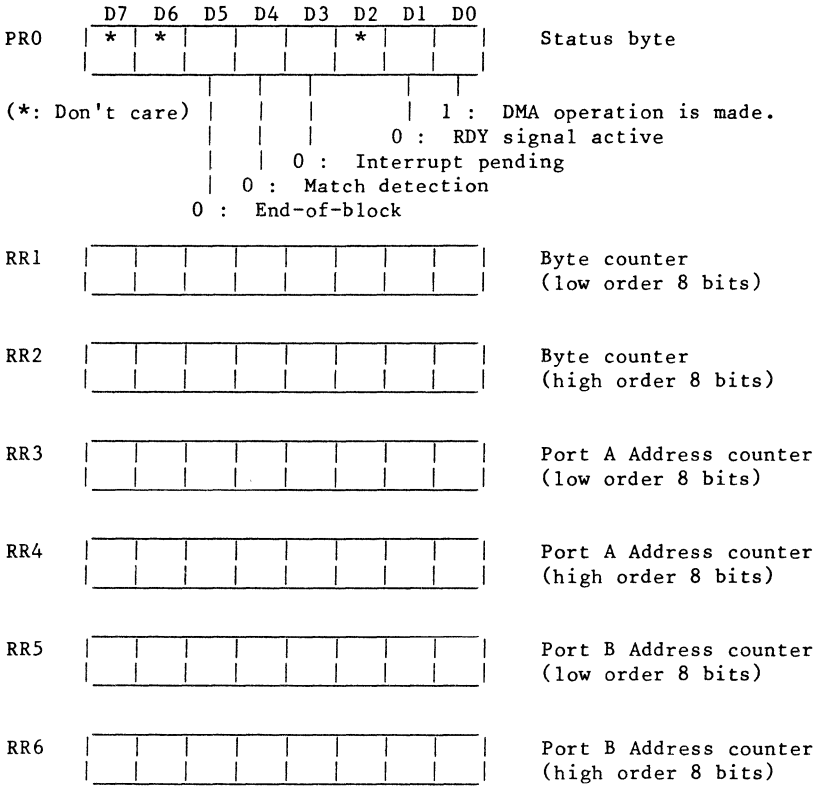


Fig. 3.42 Read Register

(3) Read register RR3, RR4 - Port A address counter
Write into the 16-bit counter consisting of two read registers RR3 and Rr4 is made from WR0 port A start address register by the load command. Whenever one byte of DMA operation is carried out according to the designated content of WR0, this counter is updated (incremented or decremented) by one.

(4) Read register RR5, RR6 - Port B address counter
The 16-bit counter consisting of two read registers RR5 and RR6 indicates Port B address when DMA operation ended. Values in the port B address register (WR4) are loaded into this counter by the load command and the coutner is updated by one every time when DMA operation is carried out by one byte. However, if address fix (Bit 4 and 5 of WR2) is programmed, the counter does not change. If Port A or Port B is a fixed address destination port, in order to properly function the port it is necessary to program as described for the fixed address destination port.

3.4.3 Address counter and byte counter values when DMA operation ended.

Values of these counters when DMA operation ended are shown in Table 3.4 (a) and Table 3.4 (b).

Table 3.4(a) Values of those counters when DMA operation ended

Data format	Data tansfer mode	Value of block length register	Number of byte to be trans-ferred	Value of byte counter	Address counter value of source port	Address counter value of destina-tion port
Transfer	Byte	N	N + 1	N	As ± (N + 1)	As ± (N)
	Burst	N	N + 1	N	As ± (N + 1)	As ± (N)
	Conti-nuity	N	N + 1	N	As ± (N + 1)	As ± (N)
Search	Byte	N	N + 1	N	As ± (N + 1)	_
	Burst	N	N + 1	N	As ± (N + 1)	_
			N + 2*	N + 1*	As ± (N + 2)*	_
	Conti-nuity	N	N + 1	N	As ± (N + 1)	_
			N + 2*	N + 1*	As ± (N + 2)*	_

AS: Start address *: The values when N+1 byte data is transferred and RDY signal is active using 2-cycle variable timing.

Table 3.4(b) Values of those counters when DMA operation ended

Data format	Data tansfer mode	Byte no. to be detected	Number of byte to be trans-ferred	Value of byte counter	Address counter value of source port	Address counter value of destina-tion port
Transfer	Byte	M	M	M - 1	As ± (M)	As ± (W-1)
	Burst	M	M	M - 1	As ± (M)	As ± (W-1)
	Conti-nuity	M	M	M - 1	As ± (M)	As ± (W-1)
Search	Byte	M	M	M - 1	As ± (M)	_
	Burst	M	M + 1	M	As ± (M + 1)	_
			M*	M - 1*	As ± (M)*	_
	Conti-nuity	M	M + 1	M	As ± (M + 1)	_
			M*	M - 1*	As ± (M)*	_

AS: Start address *: The values when match is detected and RDY signal is active.

3.4.4 List of command

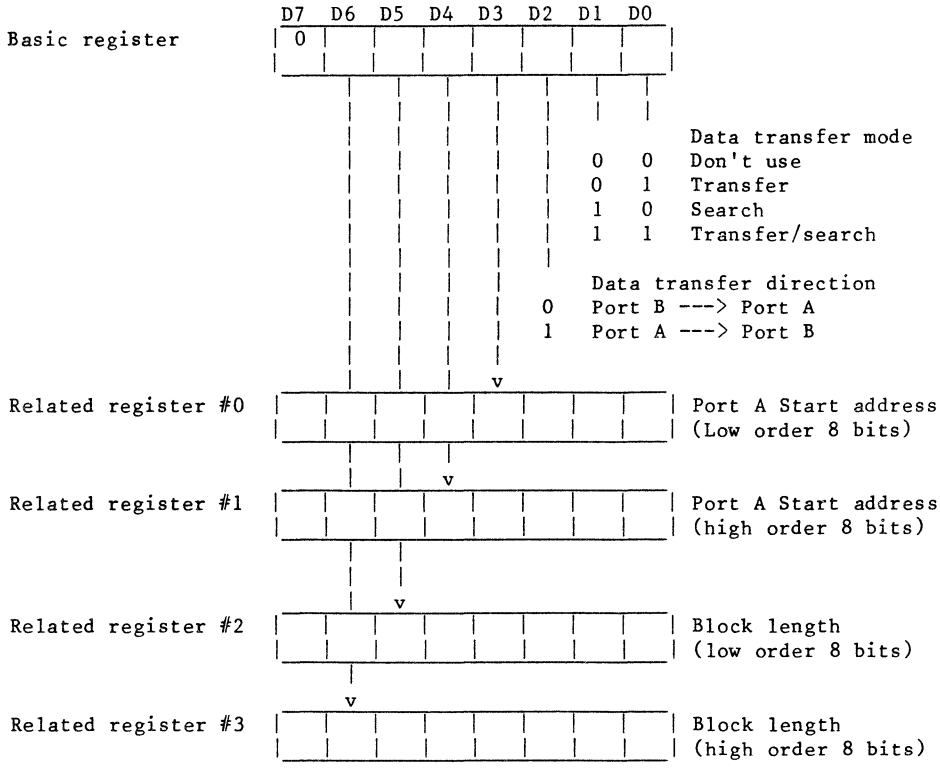


Fig. 3.35 Write Register WR0

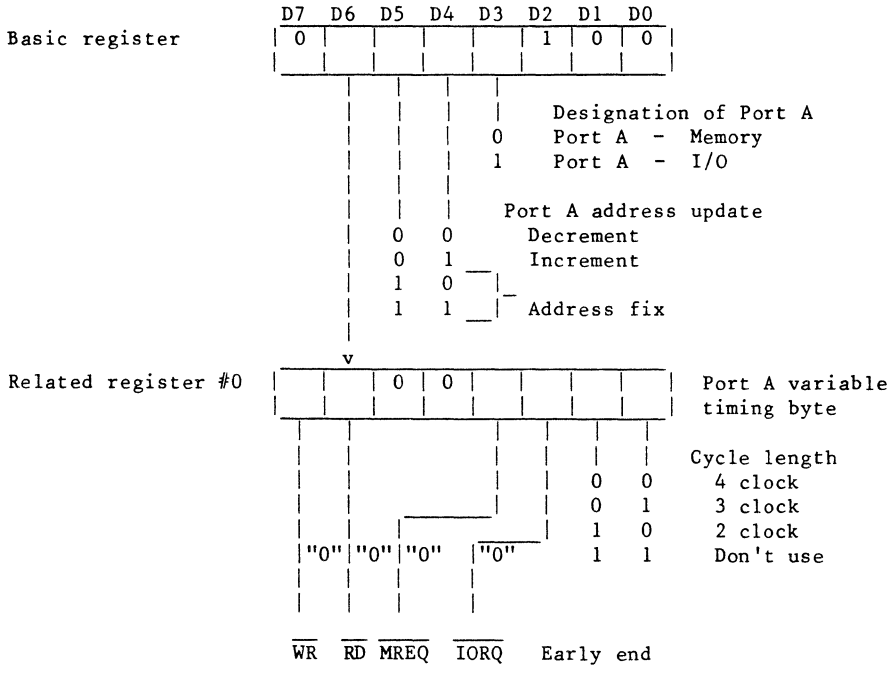


Fig. 3.36 Write Register WR1

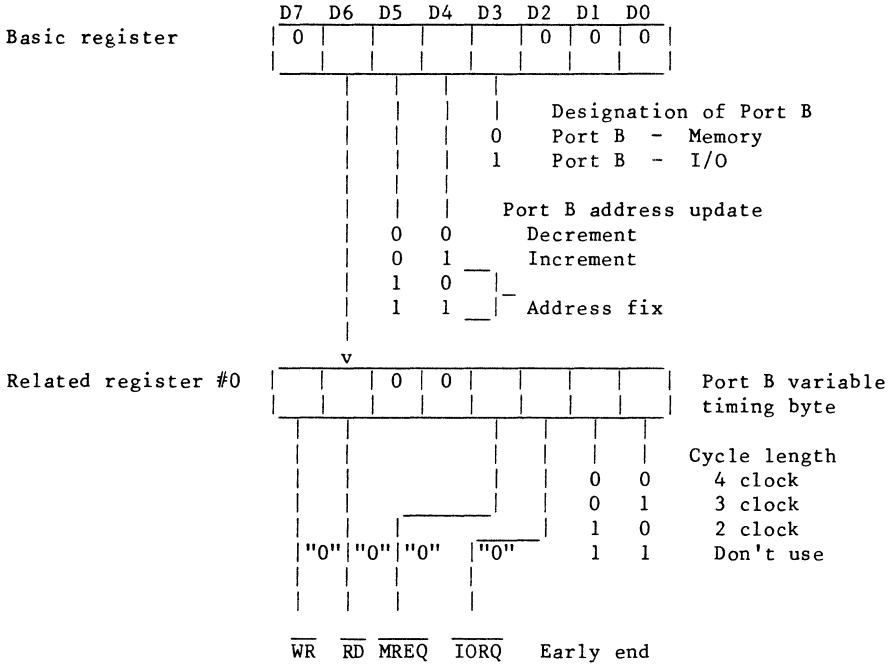


Fig. 3.37 Write Register WR2

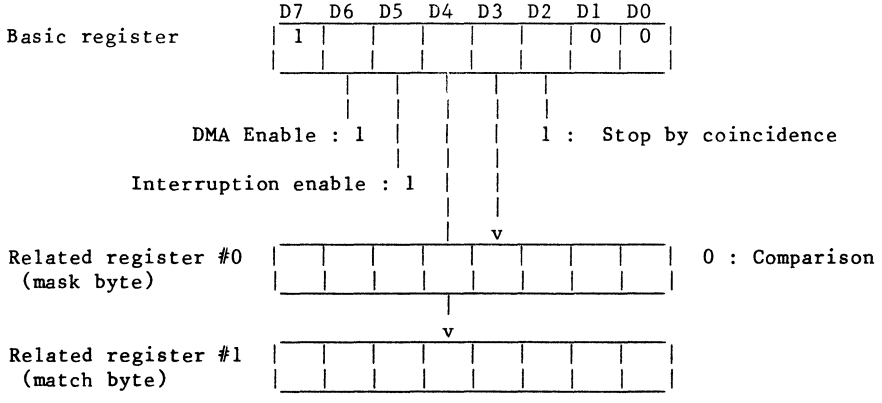


Fig. 3.38 Write Register WR3

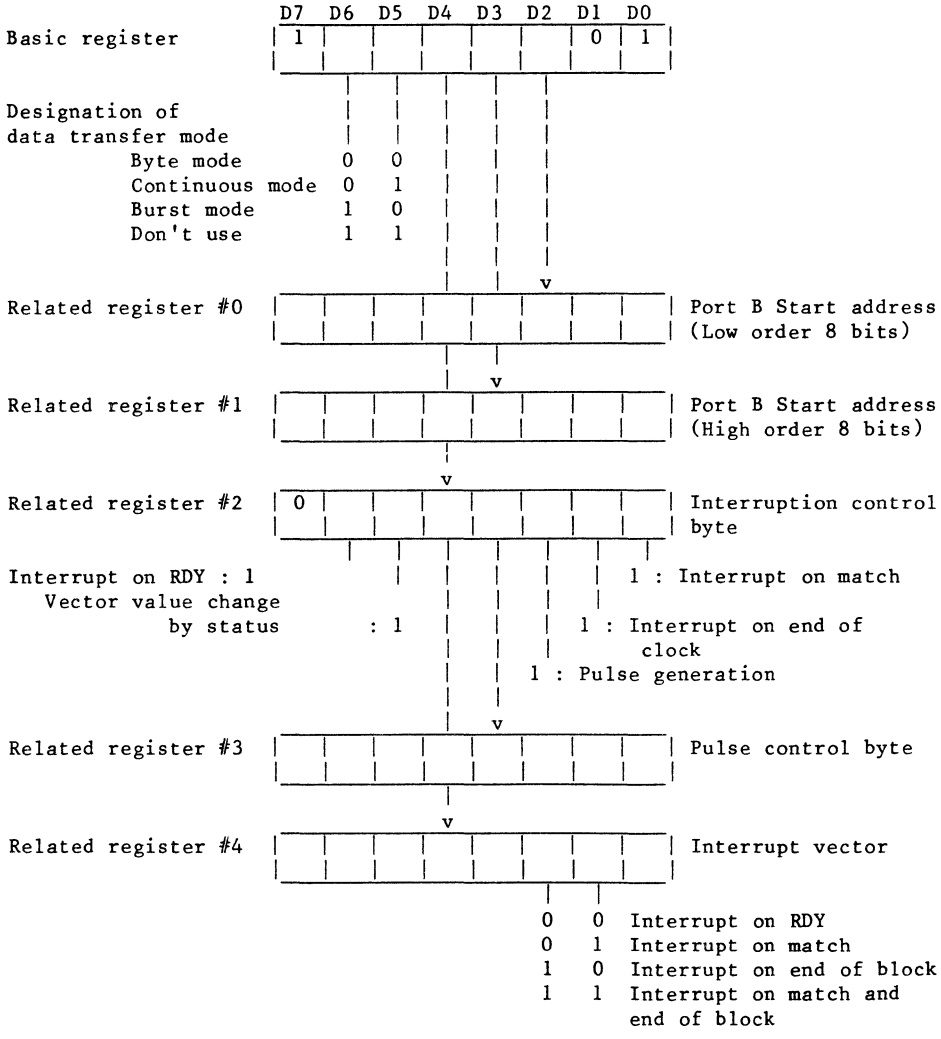


Fig. 3.39 Write Register WR4

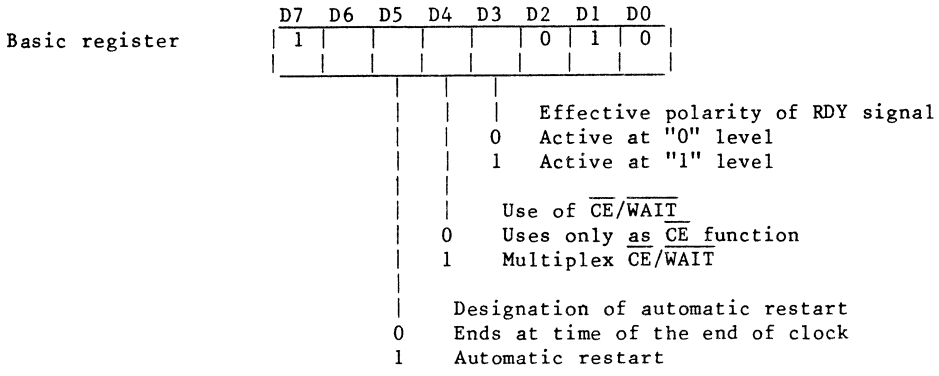


Fig. 3.40 Write Register WR5

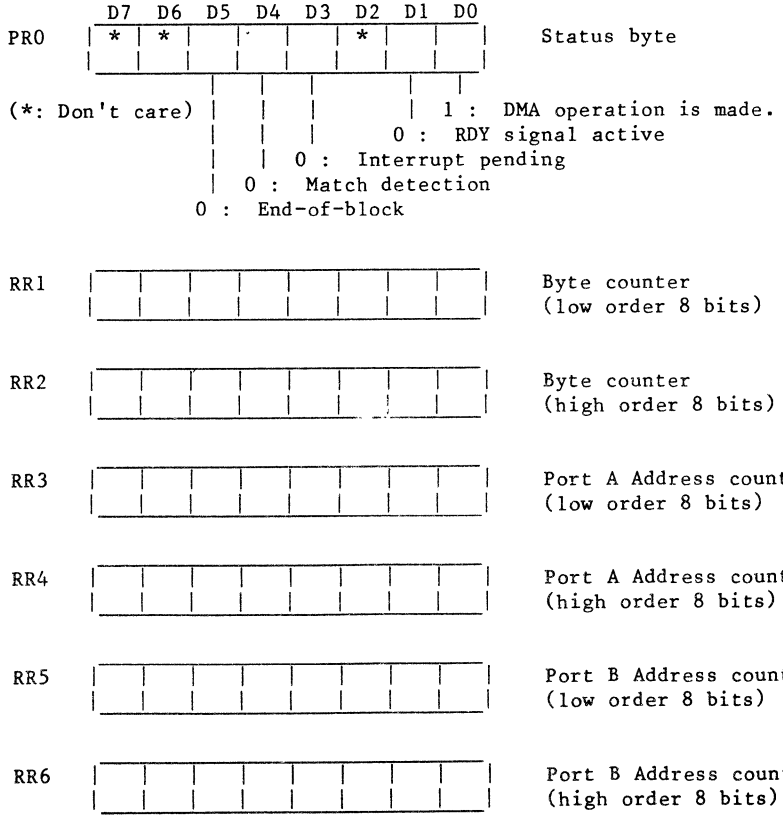


Fig. 3.42 Read Register

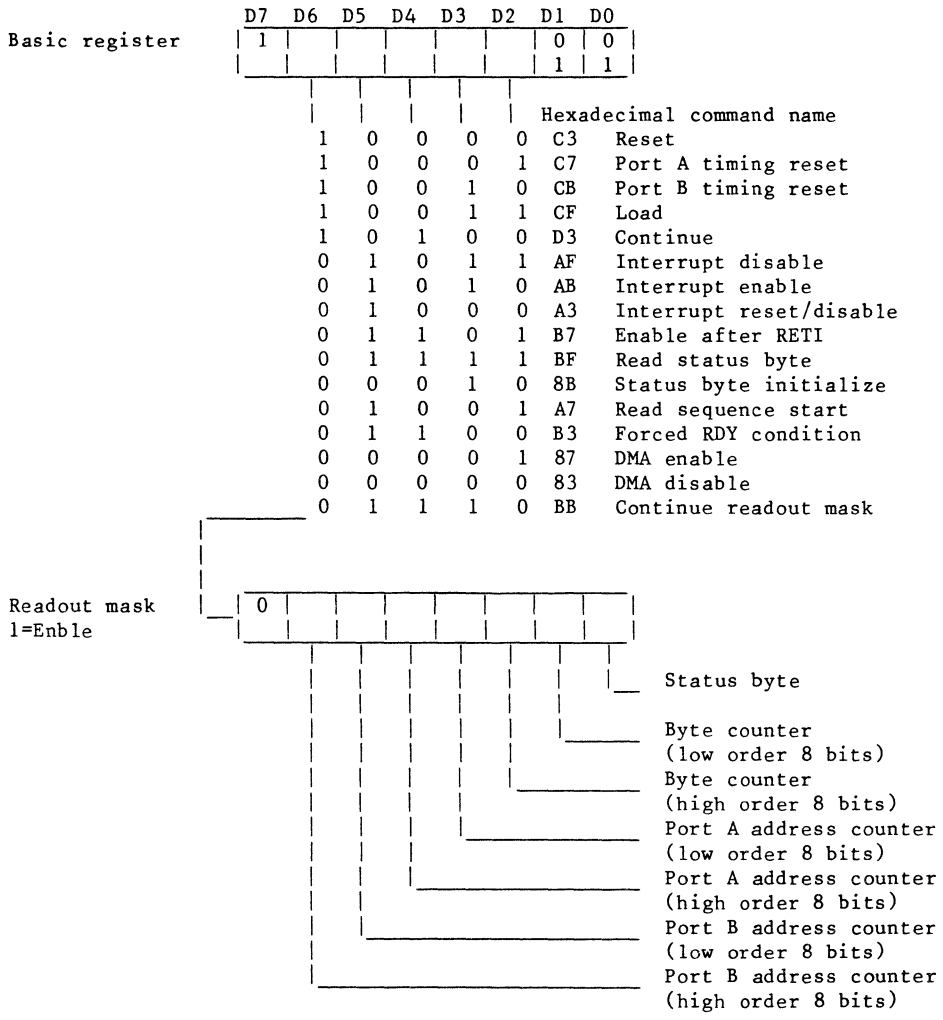


Fig. 3.41 Write Register WR6

3.5 Method of use

(1) Example of interface

As the method of use of DMA using the Z80 family, a simple example of the Z80 system interface is shown below. Fig. 3.43 shows the connection employing the Z80MPU, Z80DMA, Z80PIO, and MEMORY.

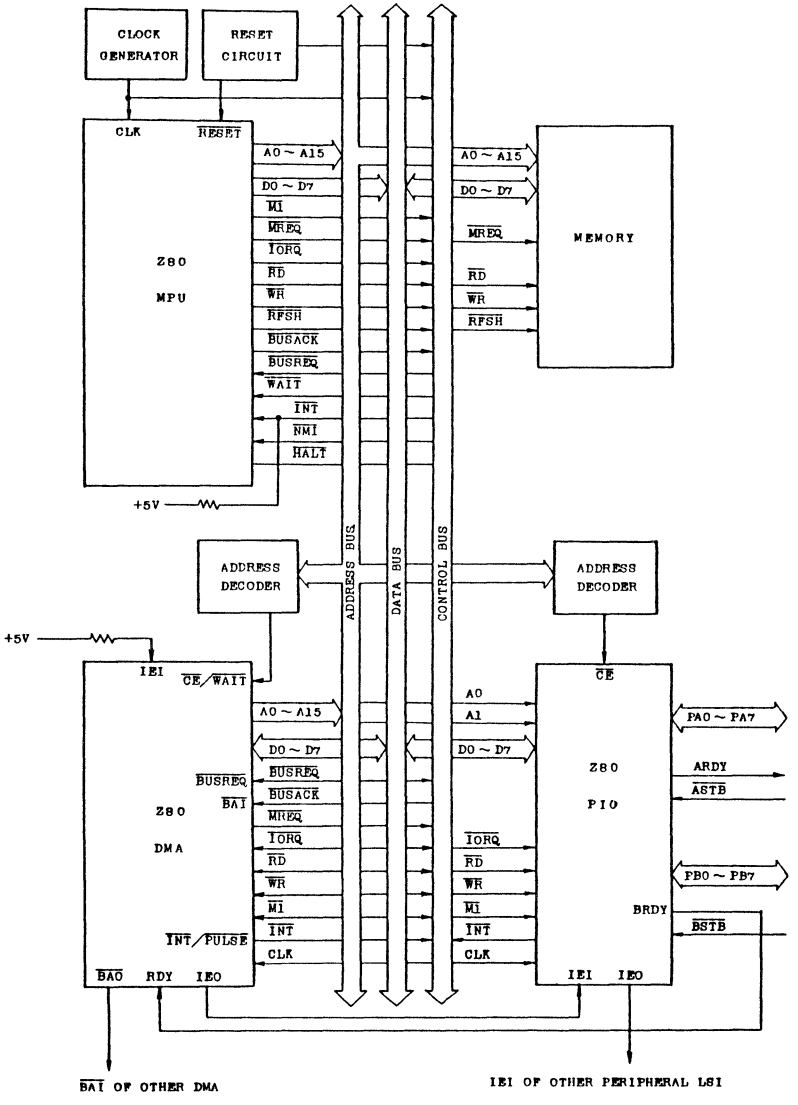


Fig. 3.43 Example of Z80 System Interface

On the Z80 system, signal lines of MPU and peripheral devices are conneced almost directly. In Fig. 3.43, priority is in the order of DMA and PIO. This is becuase the connection is made according to the daisy chanin method which is peculiar to the Z80 system. In the case of DMA, especially, in order to operate as a bus controller, BUSACK signal, which is the output of MPU, is input to BAI of DMA by the bus request daisy chain. When several units of DMA are used, BAO is connect to BAI of DMA which has the next higher priority. Hardware can be easily connected as shown in Fig. 3.43. In addition, memory mapped I/O also can be connected to DMA.

(2) Program example

As a program exmaple of DMA operation, an example of transfer from I/O to memory using PIO is shown.

```
                        .Z80
                ;       Z80 DMA DATA TRANSFER
                ;       I/O TO MEMORY
                ;       (PIO PORT B)
0020            DPIOB   EQU     20H             ;DATA PIO CHANNEL B
0021            DPIOB   EQU   +)DPIOB+1         ;CONTROL PIO CHANNEL B
0030            DMA     EQU     30H             ;DMA ADDRESS
2000            DSTN    EQU     2000H           ;DESTINATION
0100            LENGTH  EQU     256             ;BLOCK LENGTH

                        ORG     1000H
1000'  F3       STRT:   DI
1001'  3E 10            LD      A,10
1003'  ED 47            LD      1,A
1005'  ED 5E            IM      2               ;INTERRUPT MODE 2
                ;
                ;   PIO  B INITIALIZATION
1007'  3E 4F            LD      A,4FH           ;MODE 1
1009'  D3 21            OUT     (CPIOB),A
100B'  3E 07            LD      A,07H
100D'  D3 21            OUT     (CPIOB),A
                ;
                ;   DMA RESET
100F'  3E C3            LD      A,0C3H
1011'  06 06            LD      B,06H
1013'  D3 30    DMRT:   OUT     (DMA),A
1015'  10 FC            DJNZ    DMRT
                ;
                ;   DMA INITIALIZATION
1017'  06 12            LD      B,DMAFIN-DMACTA
1019'  0E 30            LD      B,DMA
101B'  21 104E'         LD      HL,DMACTA
101E'  ED B3            OTIR
1020'  FB               EI
1021'  C9               RET
```

```
                        ;
                        ;     INTERRUPT ON READY
1022'   76              IOR:    HALT
                        ;
                        ;     INTERRUPT ON MATCH
1023'   76              IOM:    HALT
                        ;
                        ;     INTERRUPT ON END OF BLOCK
1024'   CD 1037'        IOE:    CALL    SAV
1027'   3E 8B                  LD      A,8BH
1029'   32 0030                LD      (DMA),A
102C'   06 04                  LD      B,DMAFIN-DMACTB
102E'   0E 30                  LD      C,DMA
1030'   21 105C'              LD      HL,DMACTB
1033'   ED B3                  OTIR
1035'   C9                      RET
                        ;
                        ;     INTERRUPT ON MATCH, END OF BLOCK
1036'   76              IME:    HALT
                        ;
                        ;     REGISTER SAVE
1037'   E3              SAV:    EX      (SP),HL
1038'   D5                      PUSH    DE
1039'   C5                      PUSH    BC
103A'   F5                      PUSH    AF
103B'   DD E5                   PUSH    IX
103D'   FD E5                   PUSH    IY
103F'   CD 104D'                CALL    RUN
1042'   FD E1                   POP     IY
1044'   DD E1                   POP     IX
1046'   F1                      POP     AF
1047'   C1                      POP     BC
1048'   D1                      POP     DE
1049'   E1                      POP     HL
104A'   FB                      EI
104B'   ED 4D                   RETI
                        ;
104D'   E9              RUN:    JP      (HL)
                        ;
                        ;    DMA COMMAND TABLE
                        ;      PORT A - MEMORY
                        ;      PORT B - PIO CHANNEL B
104E'                   DMACTA  EQU     $
104E'   C3                      DEFB    0C3H        :WR6  RESET COMMNAD
104F'   7D                      DEFB    7DH         :WR0  PORT A TO PORT B(TEMP)
1050'   2000                    DEFW    DSTN        :     DESTINATION ADDRESS
1052'   00FF                    DEFW    LNGTH-1     :     BLOCK LENGTH
1054'   14                      DEFB    14H         :WR1  PORT A - "INCREMENT"
                                                          ADDRESS
1055'   28                      DEFB    28H         :WR2  PORT B - "FIXED"
                                                          ADDRESS
```

```
1056'  A0              DEFB    0A0H        :WR3  ENABLE INTERRUPT
1057'  95              DEFB    95H         :WR4  BYTE MODE TRANSFER
1058'  20              DEFB    DPIOB       :     PORT B ADDRESS(L)
1059'  32              DEFB    32H         :     IOE,STATUS AFFECTS
                                                  VECTOR
105A'  FF              DEFB    INTV-STRT   :INTV INTERRUPT VECTOR
105B'  82              DEFB    82H         :WR5  RDY ACTIVE "LOW",CE/
                                                  ONLY
105C'          DMACTB  EQU     $
105C'  CF              DEFB    0CFH        :WR6  LOAD ADDRESS TO PORT A
105D'  01              DEFB    01H         :WR0  PORT B TO PORT A
105E'  CF              DEFB    0CFH        :WR6  LOAD ADDRESS TO PORT B
105F'  87              DEFB    87H         :WR6  ENABLE DMA
1060'          DMAFIN  EQU     $
               ;
                       ORG     STRT+0FFH
10FF'  1022'   INTV:   DEFW    IOR
1101'  1023'           DEFW    IOM
1103'  1024'           DEFW    IOE
1105'  1036'           DEFW    IME
                       END
```

4. ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
VCC	Supply Voltage	-0.5 to +7	V
VIN	Input Voltage	-0.5 to Vcc + 0.5	V
PD	Power Dissipation (TA=85°C)	250	mW
TSOLDER	Soldering Temperature (10 sec)	260	°C
Tstg	Storage Temperature	-65 to 150	°C
Topr	Operating Temperature	-40 to 85	°C

4.2 DC ELECTRICAL CHARACTERISTICS

TA = -40°C to 85°C, VCC = 5V ± 10%, VSS = 0V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
VILC	Low Clock Input Voltage			-0.3	-	0.6	V
VIHC	High Clock Input Voltage			VCC-0.6	-	VCC+0.3	V
VIL	Low Input Voltage (Except CLK)			-0.5	-	0.8	V
VIH	High Input Voltage (Except CLK)			2.2	-	VCC	V
VOL	Output Low Voltage	IOL = 2.0mA BUSREQ only 3.2mA		-	-	0.4	V
VOH1	Output High Voltage (I)	IOH = -1.6mA		2.4	-	-	V
VOH2	Output High Voltage (II)	IOH = -250uA		VCC-0.8	-	-	V
ILI	Input Leak Current	VSS ≦ VIN ≦ VCC		-	-	±10	uA
ILO	Output Leak Current	VSS + 0.4 ≦ VIN ≦ VCC		-	-	±10	uA
ICC1	Power Supply Current	VCC=5V, fCLK=(1) VIHC=VIH= VCC-0.2V VILC=VIL= 0.2V	AP/AF	-	5	7	mA
			AP-6 /AF-6	-	(2) 6	(2) 10	
ICC2	Standby Supply Current	VCC=5V VIHC =VIH=VCC-0.2V VILC=VIL=0.2V		-	-	10	uA

Note (1) fCLK=1/TcC(MIN.) (2) Preliminary

4.3 AC ELECTRICAL CHARACTERISTICS

4.3.1 A.C. Characteristics (I)

When operate as peripheral devices (inactive state)

TA = -40°C to 85°C, VCC = 5V ± 10%, VSS = 0V

NO.	SYMBOL	PARAMETER	4 MHz AP/AF		Preliminary 6 MHz AP-6/AF-6		UNIT
			MIN.	MAX.	MIN.	MAX.	
1	TcC	Clock cycle time	250	DC	165	DC	ns
2	TwCh	High clock pulse width	110	DC	65	DC	ns
3	TwCl	Low clock pulse width	110	DC	65	DC	ns
4	TrC	Clock rise time	-	30	-	20	ns
5	TfC	Clock fall time	-	30	-	20	ns
6	Th	Hold time	0	-	0	-	ns
7	TsC(Cr)	$\overline{IORQ}$, $\overline{WR}$ and $\overline{CE}$ signals set-up time for clock rise	145	-	60	-	ns
8	TdDO(RDf)	Delay from $\overline{RD}$ rise to data output	-	380	-	300	ns
9	TsWM(Cr)	Data input set-up time for clock rise (write and $\overline{M1}$ cycle)	50	-	30	-	ns
10	TsCf(DO)	Delay from $\overline{IORQ}$ fall to data output (INTA cycle)	-	160	-	100	ns
11	TsRD(DZ)	Delay from $\overline{RD}$ rise to data bus float state	-	110	-	70	ns
12	TsIEI(IORQ)	IEI set-up time for $\overline{IORQ}$ fall (INTA cycle)	140	-	100	-	ns
13	TdIEOr(IEIr)	Delay from IEI rise to IEO rise	-	160	-	70	ns
14	TdIEOf(IEIf)	Delay from IEI fall to IEO fall	-	130	-	70	ns
15	TdM1(IEO)	Delay from $\overline{M1}$ fall to IEO fall (When interrupt is generated immediately before $\overline{M1}$ cycle.)	-	190	-	100	ns
16	TsM1f(Cr)	$\overline{M1}$ signal set-up time for clock rise	90	-	70	-	ns
17	TsM1r(Cf)	$\overline{M1}$ signal set-up time for clock fall	-10	-	-10	-	ns

NO.	SYMBOL	PARAMETER	4 MHz AP/AF MIN.	4 MHz AP/AF MAX.	Preliminary 6 MHz AP-6/AF-6 MIN.	Preliminary 6 MHz AP-6/AF-6 MAX.	UNIT
18	TsRD(Cr))	$\overline{RD}$ signal set-up time for clock rise (M1 cycle)	115	-	60	-	ns
19	TdI(INT)	Delay from interruption generation to $\overline{INI}$ fall (at inactive state)	-	500	-	450	ns
20	TdBAIr(BAOr)	Delay from $\overline{BAI}$ rise to $\overline{BAO}$ rise	-	150	-	100	ns
21	TdBAIf(BAOf)	Delay from $\overline{BAI}$ fall to $\overline{BAO}$ fall	-	150	-	100	ns
22	TsRDY(Cr)	RDY signal set-up time for clock rise	100	-	50	-	ns

4.3.2 A.C. Characteristics (II)
When operate as bus controller (active state)
TA = -40°C to 85°C, VCC = 5V ± 10%, VSS = 0V

NO.	SYMBOL	PARAMETER	4 MHz AP/AF MIN.	4 MHz AP/AF MAX.	Preliminary 6 MHz AP-6/AF-6 MIN.	Preliminary 6 MHz AP-6/AF-6 MAX.	UNIT
1	TcC	Clock cycle time	250	DC	165	DC	ns
2	TwCh	High clock pulse width	110	DC	65	DC	ns
3	TwCl	Low clock pulse width	110	DC	65	DC	ns
4	TrC	Clock rise time	-	30	-	20	ns
5	TfC	Clock fall time	-	30	-	20	ns
6	TdA	Delay of address output	-	110	-	90	ns
7	TdC(AZ)	Delay from clock rise to address bus float state		90	-	80	ns
8	TsA(MREQ)	Address set-up time for $\overline{MREQ}$ rise (memory cycle)	65	-	35	-	ns
9	TsA(IRW)	Address set-up time for $\overline{IORQ}$, $\overline{RD}$, $\overline{WR}$ fall (I/O cycle)	180	-	110	-	ns
10	TdRW(A)	Address hold time from $\overline{RD}$, $\overline{WR}$ rise	90	-	35	-	ns
11	TdRW(Az)	Address hold time from $\overline{RD}$, $\overline{WR}$ rise (at float state)	95	-	65	-	ns
12	TdCf(DO)	Delay from clock fall to data output	-	150	-	130	ns

NO.	SYMBOL	PARAMETER	4 MHz AP/AF MIN.	4 MHz AP/AF MAX.	Preliminary 6 MHz AP-6/AF-6 MIN.	Preliminary 6 MHz AP-6/AF-6 MAX.	UNIT
13	TdCr(DZ)	Delay from clock rise to data bus float state (write cycle)	-	90	-	70	ns
14	TsDI(Cr)	Data input set-up time up to clock rise (read cycle in which $\overline{RD}$ ended at clock rise)	35	-	30	-	ns
15	TsDI(Cf)	Data input set-up time up to clock fall (read cycle in which RD ended at clock fall)	50	-	40	-	ns
16	TsDO(WfM)	Data output set-up time up to $\overline{WR}$ fall (memory cycle)	80	-	25	-	ns
17	TsDO(WfI)	Data output set-up time up to $\overline{WR}$ fall (I/O cycle)	100	-	55	-	ns
18	TsWr(DO)	Data hold time from WR rise	70	-	30	-	ns
19	Th	Hold time	0	-	0	-	ns
20	TdCr(Mf)	Delay from clock rise to $\overline{MREQ}$ fall	-	85	-	70	ns
21	TdCf(Mf)	Delay from clock fall to $\overline{MREQ}$ fall	-	85	-	70	ns
22	TdCr(Mr)	Delay from clock rise to $\overline{MREQ}$ rise	-	85	-	70	ns
23	TdCf(Mr)	Delay from clock fall to $\overline{MREQ}$ rise	-	85	-	70	ns
24	TwMl	Low $\overline{MREQ}$ pulse width	220	-	135	-	ns
25	TwMh	High $\overline{MREQ}$ pulse width	120	-	65	-	ns
26	TdCf(If)	Delay from clock fall to $\overline{IORQ}$ fall	-	85	-	70	ns
27	TdCr(If)	Delay from clock rise to $\overline{IORQ}$ fall	-	75	-	65	ns
28	TdCr(Ir)	Delay from clock rise to $\overline{IORQ}$ rise	-	85	-	70	ns
29	TdCf(Ir)	Delay from clock fall to $\overline{IORQ}$ rise	-	85	-	70	ns
30	TdCr(Rf)	Delay from clock rise to $\overline{RD}$ fall	-	85	-	70	ns
31	TdCf(Rf)	Delay from clock fall to $\overline{RD}$ fall	-	95	-	80	ns
32	TdCr(Rr)	Delay from clock rise to $\overline{RD}$ rise	-	85	-	70	ns
33	TdCf(Rr)	Delay from clock fall to $\overline{RD}$ rise	-	85	-	70	ns

NO.	SYMBOL	PARAMETER	4 MHz AP/AF MIN.	4 MHz AP/AF MAX.	Preliminary 6 MHz AP-6/AF-6 MIN.	Preliminary 6 MHz AP-6/AF-6 MAX.	UNIT
34	TdCr(Wf)	Delay from clock rise to $\overline{WR}$ fall	-	65	-	60	ns
35	TdCf(Wf)	Delay from clock fall to $\overline{WR}$ fall	-	80	-	60	ns
36	TdCr(Wr)	Delay from clock rise to $\overline{WR}$ rise	-	80	-	70	ns
37	TdCf(Wr)	Delay from clock fall to $\overline{WR}$ rise	-	80	-	70	ns
38	TwWl	Low $\overline{WR}$ pulse width	220	-	135	-	ns
39	TsWA(Cf)	$\overline{WAIT}$ signal set-up time for clock fall	70	-	60	-	ns
40	TdCr(B)	Delay from clock rise up to $\overline{BUSREQ}$ signal	-	100	-	90	ns
41	TdCr(Iz)	Delay from clock rise to $\overline{IORQ}$, $\overline{MREQ}$, $\overline{RD}$, $\overline{WR}$ signal float state	-	80	-	70	ns

A.C Test conditions

VIH = 2.4V, VIL = 0.4V, VIHC = VCC - 0.6V, VILC = 0.6V

VOH = 2.2V, VOL = 0.8V

CL=100pF

4.4 Capacitance

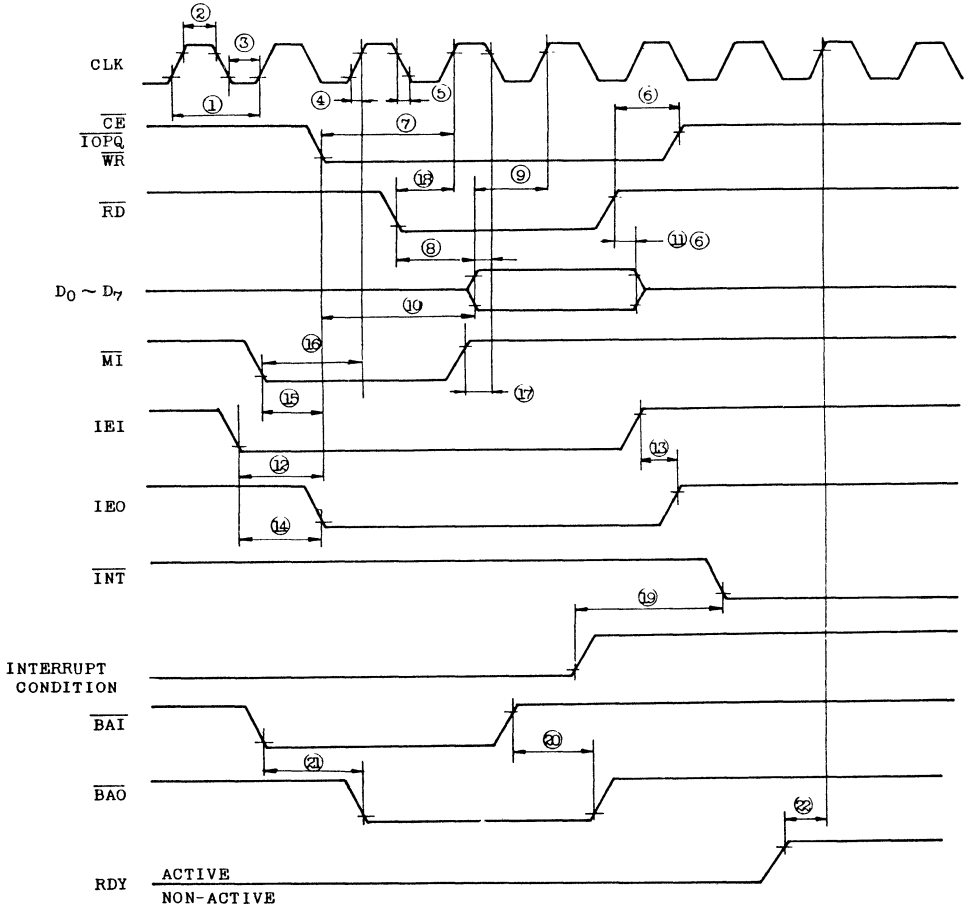
TA = 25°C

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CCLOCK	Clock Input Capacitance	f=1MHz All terminals except that to be measured should be earthed.	-	-	5	pF
CIN	Input Capacitance		-	-	5	pF
COUT	Output Capacitance		-	-	5	pF

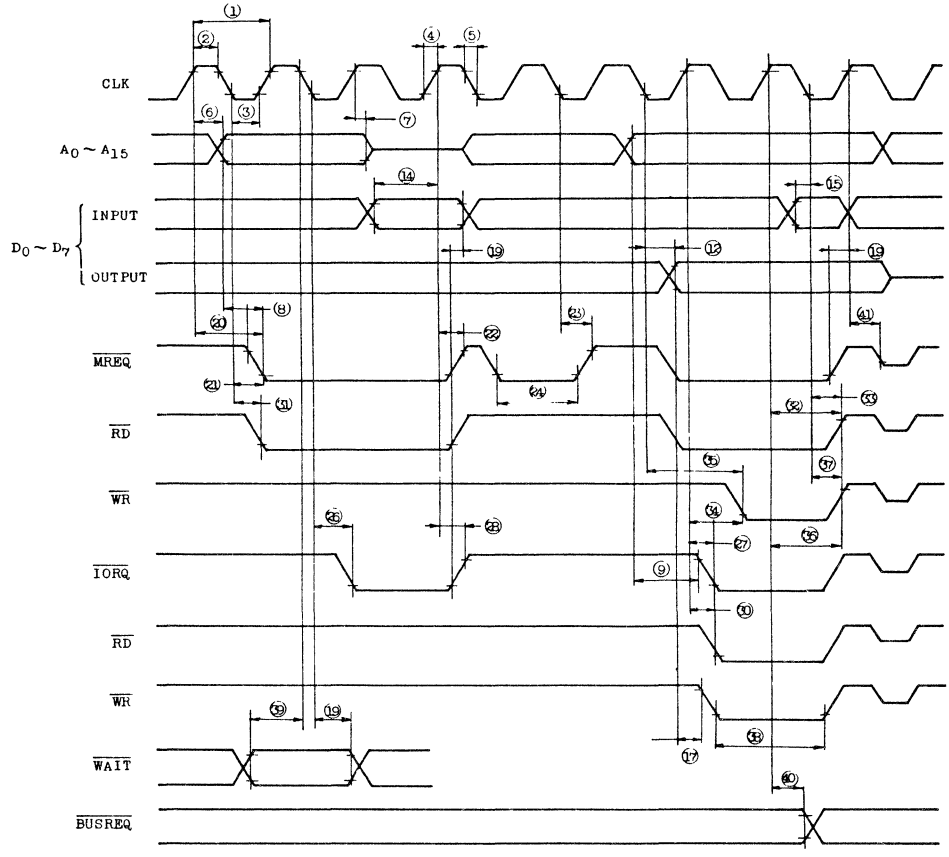
4.5 Timing diagram

Numbers shown in the following figures correspond with those in the 4.3 A.C. Electrical Characteristics Table.

(1) When operate as peripheral devices (inactive state)



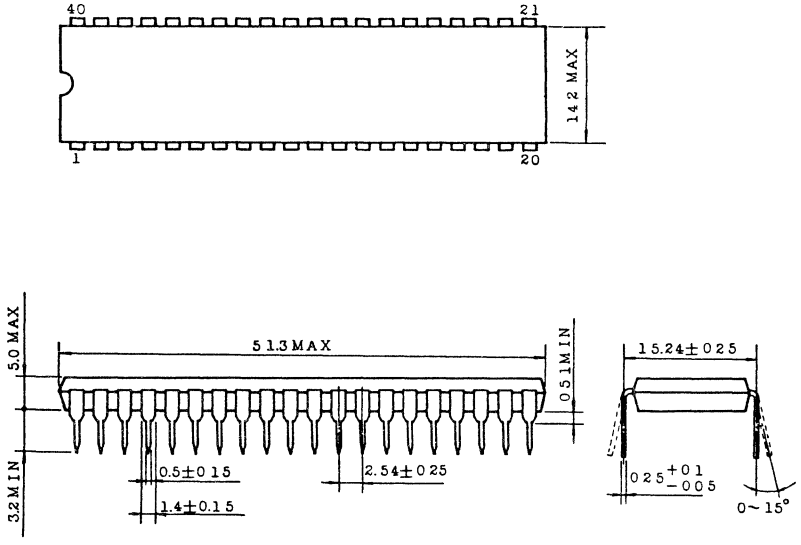
(2) When operate as bus controller (active state)



5. External Dimension View

Unit in mm

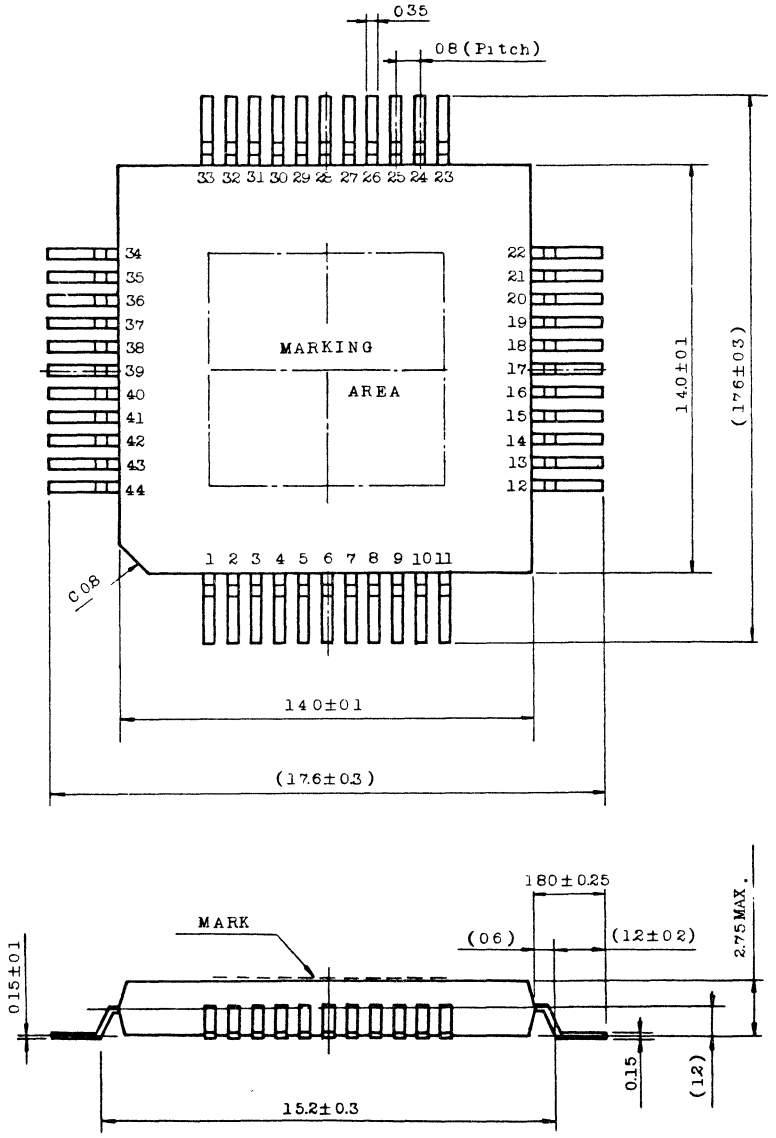
5.1 DIP package



Note 1. This dimension is measured at the center of bending point of leads.
Note 2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25 mm from their theoretical positions with respect to No.1 and No.40 leads.

5.2 44-Pin mini-flat Package

Unit in mm



6. Precautions

For the basic timings, please refer to the precautions in 3.3.2 (1).
For the commands, care shall be taken to the programming as there are many registers and setup is considerably complictated.
As the precaution for the programming, the "fixed address destination port programming" is briefly described. When Port A is assumed to be the "fixed address destination port", address can be loaded in the following steps:

(1) Write Port A address into WR0.
(2) Designate Port A as the source port. (set up temporarily)
(3) Load Port A address on the address counter. (Load command CFH)
(4) Write Port B start address into WR4.
(5) Convert Port A into the destination port.
(6) Load Port B start address on the address counter. (source port address)

TMPZ84C20P, TMPZ84C20AP, TMPZ84C20AP-6, TMPZ84C20F, TMPZ84C20AF, TMPZ84C20AF-6
TLCS-Z80 PIO: PARALLEL INPUT/OUTPUT CONTROLLER

1. General Description and Features

The TMPZ84C20 (hereinafter referred to as PIO) is CMOS version of Z80 PIO and has been designed to provide low power operation.
The PIO is a general purpose parallel input/output port device with two programmable independent 8-bit ports, which provides a direct interface between the Z80 microprocessor (hereinafter referred to as MPU) and peripheral devices.
This PIO provides excellent data transfer processing by the interrupt and allows the interrupt in Mode 2 of MPU.
The TMPZ84C20 is fabricated using Toshiba's CMOS Silicon Gate Technology.

The principal functions and features of the TMP84C20 are as follows.

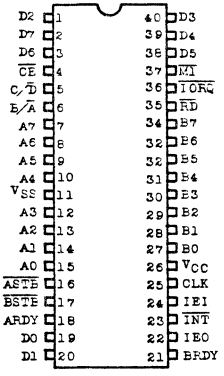
(1) Compatible with the functions and pin connections of Zilog Z80 PIO.
(2) Low power consumption
  2mA Typ. (@5V @4MHz) ... TMPZ84C20P/F, TMPZ84C20AP/AF
  3mA Typ. (@5V @6MHz) ... TMPZ84C20AP-6/AF-6
  10uA Max. (@5V, Stand-by)
(3) Operating temperature
  -40 C to 85 C
(4) DC to 4MHz operation ... TMPZ84C20P/AP
  DC to 6MHz operation ... TMPZ84C20AP-6/AF-6
(5) 2 programmable independent 8-bit input/output ports with handshake function.
(6) 4 operation modes for each port:
  Mode 0 (Byte Output Mode)
  Mode 1 (Byte Input Mode)
  Mode 2 (Byte Input/Output Mode) ..... Port A only.
  Mode 3 (Bit Mode)
(7) Built-in interrupt priority control circuit in daisy chain structure
(8) Port B outputs capable of driving Darlington transistors
(9) All input/output lines are TTL compatible.
(10) Single 5V power supply. Single-phase clock
(11) 40 pin DIP package, 44 pin Mini Flat Package.

(Note) Z80(R) is a registered trademark of Zilog Inc., U.S.A.

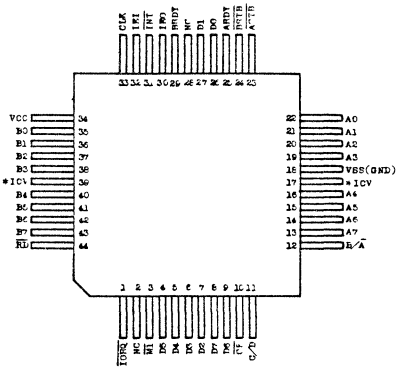
2. Pin Connections and Pin Functions

2.1 Pin connections

The pin connections of the TMPZ84C20P are as shown in Fig. 2.1.



(a) DIP Pin Connection



(b) MFP Pin Connection

(Note) NC must be used at open condition.
*ICV must be used at open
Condition or Connected with Vcc.

Fig. 2.1 Pin Connections (Top View)

2.2 Pin names and functions

I/O pin names and functions are as shown in Table 2.1.

Table 2.1 Pin Names and Functions

Pin Name	Number of Pin	Input/Output 3-state	Function
D0 - D7	8	I/O 3-state	8-bit bidirectional data bus. Data transfer between MPU and PIO
$\overline{CE}$	1	Input	Chip enable. Used for accessing MPU and PIO. When MPU selects this PIO, this terminal becomes L level (Refer to 3.4 Basic timing.) Normally, this terminal is connected to the address decoder output.
C/$\overline{D}$	1	Input	Control/data select. Indicates if signal on the data bus is control signal or data. Selects data at L level and command at H level. Normally, connected to address bit A1 of MPU.
B/$\overline{A}$	1	Input	Port A/port B select. Selects Port A at L level and Port B at H level. Normally, connected to address bit A0 of MPU.

Pin Name	Number of Pin	Input/Output 3-state	Function
A0 - A7	8	I/O 3-state	Port A bus. Data transfer between Port A of PIO and external device.
$\overline{ASTB}$	1	Input	Port A strobe input Handshake signal from the external device. Signal meaning differs depending upon operatiom mode. (Refer to 3.4 Basic timing.)
$\overline{BSTB}$	1	Input	Port B strobe input Handshake signal from the external device. Signal meaning is the same as ASTB but differs if Port A is in Mode 2. (Refer to 3.4 Basic timing.) Register A ready.
ARDY	1	Output	Port A ready. Handshake signal to the external device. Signal meaning differs depending upon operation mode. (Refer to 3.4 Basic timing.)
$\overline{M1}$	1	Input	Machine cycle 1. When both $\overline{M1}$ and $\overline{IORQ}$ are at L level, indicates that MPU is executing the interrupt acknowledge cycle. (Refer to 3.4 Basic timing.) Normally, connected to $\overline{M1}$ of MPU.
$\overline{IORQ}$	1	Input	I/O request. Used to access between MPU and PIO. This terminal becomes L level when I/O addresses are on the address in the write cycle and read cycle. Further, when $\overline{IORQ}$ and $\overline{M1}$ are both at L level, it indicates that MPU is executing the interrupt acknoledge cycle. (Refer to 3.4 Basic timing.) Normally, connected to $\overline{IORQ}$ of MPU.
$\overline{RD}$	1	Input	Read signal. Used to access between MPU and PIO. Controls the transfer direction. (Refer to 3.4 Basic timing) Normally, connected to $\overline{RD}$ of MPU.
B0 - B7	8	I/O 3-state	Port B bus. Data transfer between Port B of PIO and external device. Capable of driving -1.5mA (@VoH=1.5V) Darlington transistors.
CLK	1	Input	System clock. Single-phase clock input. In DC state (either at H or L level), PIO is in a stand-by state and power consumption becomes extermely less.

Pin Name	Number of Pin	Input/Output 3-state	Function
IEI	1	Input	Interrupt enable input. Together with IEO and $\overline{INT}$, forms daisy chain interrupt control signal. Connected to IEO of high priority peripheral LSI. However, to give higher priority than other peripheral LSI's to this PIO, connect this terminal to the +5V power. (Refer to 3.3.2 Interruption.)
$\overline{INT}$	1	Output	Interrupt request. Interrupt request signal for MPU. Connect to $\overline{INT}$ of MPU. (Open drain)
IEO	1	Output	Interrupt enable output. Together with IEI and $\overline{INT}$, forms daisy chain interrupt control signal. Connected to IEI of low priority peripheral LSI. However, if this PIO has the lowest priority than any other peripheral LSI's, this IEO is not used. (Refer to 3.3.2 Interruption)
BRDY	1	Output	PORT B ready Handshake signal to the external device. Signal meaning is the same as that of ARDY. However, it differs when Port A is in Mode 2. (Refer to 3.4 Basic timing.)
VCC	1	Power supply	+5V
VSS	1	Power supply	0V

3. Functional Description

3.1 Block diagram
The block diagram of PIO is shown in Fig. 3.1.

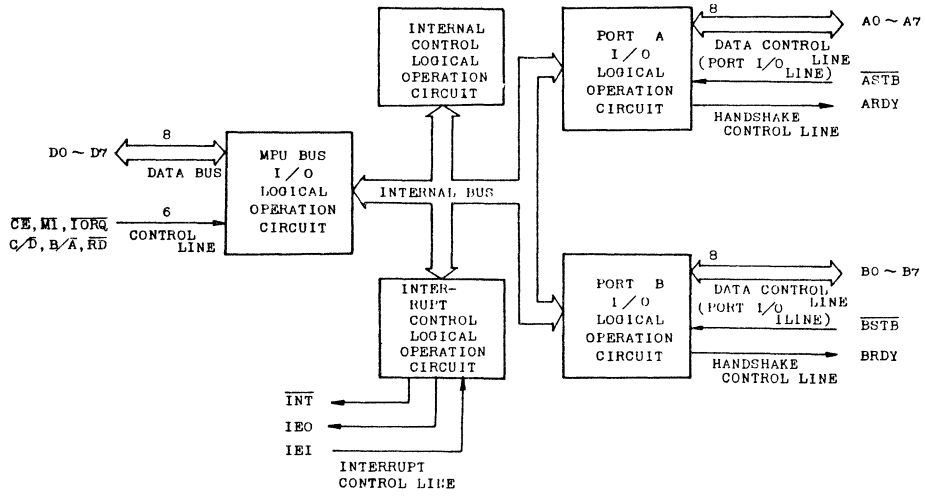


Fig. 3.1 Block Diagram

3.2 System cinfiguration (Architecture)
The system configuration of PIO consists of four logical operation circuits as below.
(1) MPU Bus Input/Output Logical Operation Circuit
(2) Internal Control Logical Operation Circuit
(3) Interrupt Control Logical Operation Circuit
(4) Port Input/Output Logical Operation Circuit

3.2.1 MPU bus input/output logical operaton circuit
This is a circuit for connecting PIO to MPU. This circuit connects PIO directly to MPU without using other external circuit. However, if a system becomes large, it becomes necessary to provide an address decoder and a line buffer.

3.2.2 Internal control logical operation circuit
This is a circuit to synchronize the MPU data bus with PIO Port A and Port B.

3.2.3 Interrupt control logical operation circuit

This is a circuit to perform processing concerning interrupt of MPU such as decision of priority.

3.2.4 Port input/output logical operation circuit

This is a circuit to connect PIO to external devices. This ciruit consists of 7 registers and one flip-flop circuit shown below. Data write to the registers is performed by MPU according to program. Shown in parentheses is number of bits. The internal port configuration is shown in Fig. 3.2.

- o Data input register (8 bits)
- o Data output register (8 bits)
- o Mode control register (2 bits)
- o Interrupt vector register (8 bits)
- o Interrupt control register (2 bits)
- o Mask control register (8 bits)
- o Data input/output control register (8 bits)

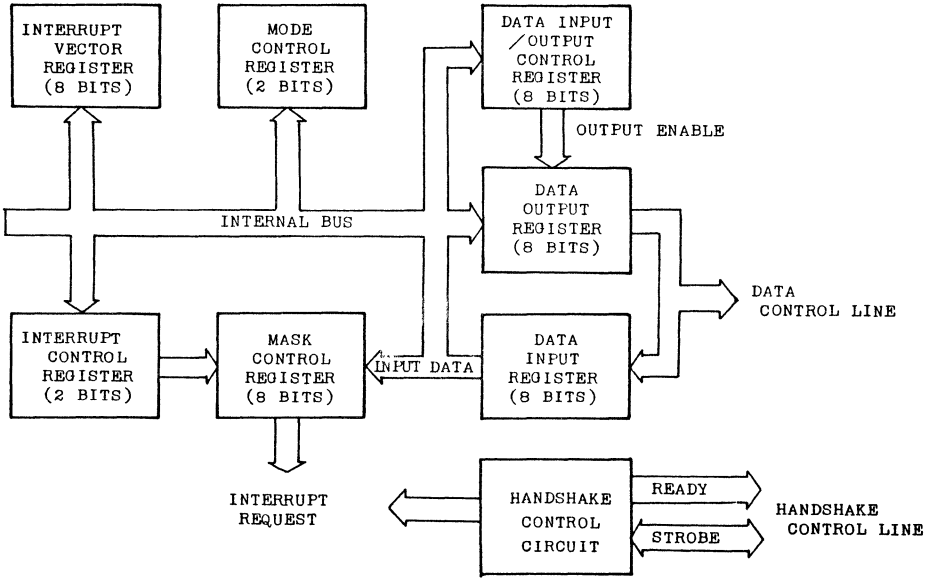


Fig. 3.2 Internal Port Configuration

(1) Data output register

This register holds data to be transferred from MPU to external devices. Output data from MPU are transferred through this register.

(2) Data input register
This register latches data being transferred to MPU from external devices. All input data to MPU are read into MPU through this register.
(3) Mode control register
This register is used to designate operation modes. Operation modes are set up through control by MPU.
(4) Interrupt vector register
This register holds vector address of a table that stores atart address of an interrupt routine. This register is used only when the interrupt process is performed.
(5) Interrupt control register
This register designates condtions for monitoring the input ports. This register is used only in Mode 3 of PIO.
(6) Mask control register
This register designates which bits of the input port is enable for the interrupt request. This register is used only in Mode 3 of PIO.
(7) Data input/output control register
This register designates each of the terminals for output/input use. This register is used only in Mode 3 of PIO.
(8) Handshake control circuit
This circuit controls data transfer with external devices connected to 8 bit input/output ports.

3.3 Basic operation

3.3.1 Reset

PIO has the following two reset functions:
(1) Power ON reset
PIO has a built-in automatic power ON reset circuit.
(2) Reset by external signal
When RD and IORQ termiansl are set at H level and M1 terminal kept at L level for 2 system clocks, PIO is reset immediately after the rise of M1 terminal.

Reset status
(1) Both ports are set in Mode 1.
(2) Interrupt is disabled.
(3) All bits of the data input/output registers of both ports are reset.
(4) All bits of the mask control registers for both ports are reset and the completely masked state is resulted.
(5) The port input/output lines of both ports are placed in high impedance state.
(6) RDY signals for both ports become L level.

The reset status is held until control characters are input. For the control characters refer to "3.5 Operating procedures".

3.3.2 Interrupt

PIO is capable of generating interrupt when MPU is operating in Mode 2. The interrupt request signal (INT) from PIO is accepted when MPU is in the enabled state (after execution of EI instruction). When accepted INT, MPU latches the interrupt vector (8 bit data) from PIO.

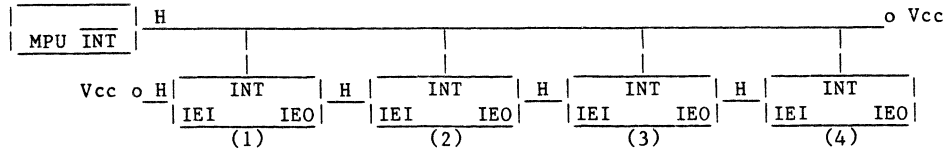
Based on this data, MPU designates the start address of the interrupt routine and by calling this routine, starts the interrupt processing. Since the start address of the interrupt routine can be thus designated by the interrupt vector from PIO, it is possible for user to call any address by changing a value of this vector.
The interrupt ends when MPU executes RETI instruction. PIO has the RETI instruction decoding circuit and is capable of knowing end of the interrupt by constantly monitoring the data bus.
The interrupt priority of peripheral LSI's is decided by the daisy chain structure. When peripheral LSI's are connected in series as shown in Fig. 3.3, peripheral LSI's which are physically closer to MPU will have higher interrupt priority. Further, in the inside of PIO, Port A has the higher priority than Port B.

Z80 Peripheral LSI has IEO and IEI terminal. The IEO terminal of a higher priority peripheral LSI is connected to the IEI terminal of a lower priority peripheral LSI by this signal line. However, the IEI terminal of a peripheral LSI having the highest priority is connected to the +5V power supply and the IEO terminal of a peripheral LSI having the lowest priority is not used. Generation of interrupt is in accordance with the following rules:

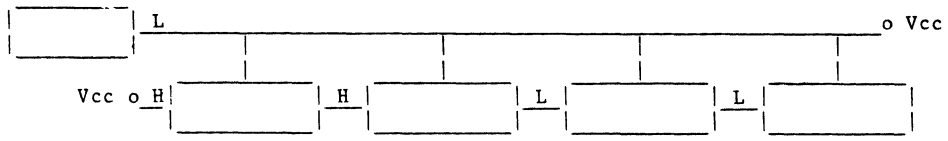
- o When the IEI and IEO terminals are both at H level, no interrupt in progress. At this time, the INT terminal is at H level. In this state, the interrupt can be requested.
- o When PIO outputs the interrupt request signal (INT), the IEO terminal is made to L level by this PIO. When an interrupt request is accepted by MPU, the INT terminal returns to H level.
- o When the IEI terminal becomes L level, the IEO terminal also becomes L level.
- o When the IEI terminal is at L level, no interrupt request can be made.
- o If the IEI terminal becomes L level while interrupt is generated, the interruption process is kept suspended.

The connection in daisy chain structure allows connection of up to 4 PIO's without providing an external circuit. This is maximum quantity not to exceed the limit of IEO signal propagation time (time from the fall of MI signal to the fall of IORQ signal in the interrupt acknowledge cycle). Connecting of more than 5 PIO's requires a simple external circuit.

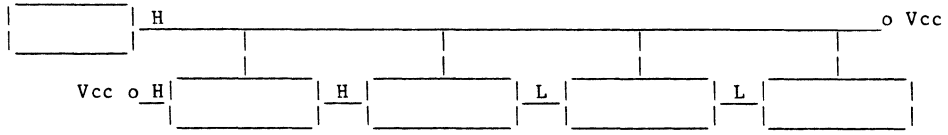
(1) Before generation of interrupt



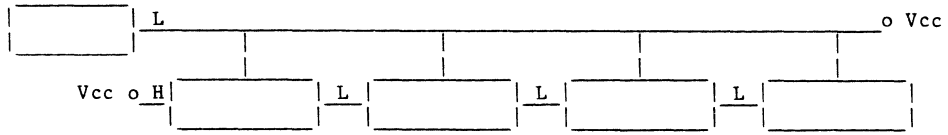
(2) Interrupt request from peripheral (2) to MPU



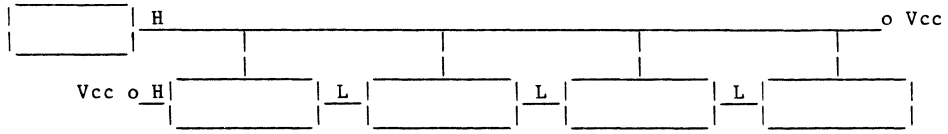
(3) Response by MPU to interrupt request ..... Execute the interrupt routine of peripheral (2)



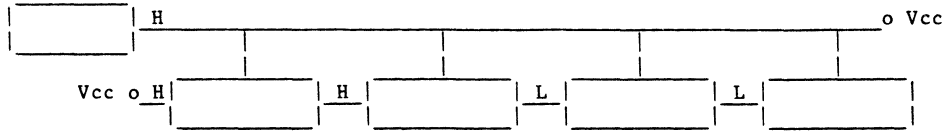
(4) Interrupt request from peripheral (1) to MPU ..... Suspends the interrupt routine of peripheral (2)



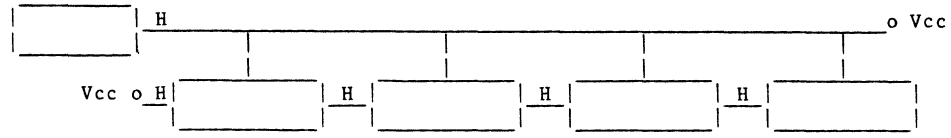
(5) Response by MPU to interrupt request ..... Execute the interrupt routine of peripheral (1)



(6) The interrupt routine of peripheral (1) ends (execution of RETI command) ..... Restarts interrupt routine of peripheral (2)



(7) The interrupt routine of peripheral (2) ends (execution of RETI command)



The interrupt priority of peripheral LSI (1) > (2) > (3) > (4)

Fig. 3.3 Operation of Daisy Chain

3.3.3 Operation mode

PIO is operated in one of the following 4 operation modes. These modes are selected by writing mode control characters.

- o Mode 0 (Byte output mode)
- o Mode 1 (Byte input mode)
- o Mode 2 (Byte input/output mode)
- o Mode 3 (Bit mode)

(1) Mode 0 (Byte output mode)

In Mode 0, PIO sends out data received from MPU to external devices through the port data output register.
The content of the data output register can be written using an output command. In addition, it remains unchanged till next output command even when data on the data bus changed.
Executing an output command by MPU generates a write signal in PIO in the write cycle. Data on the data bus can be latched in the data output register by this write signal.

(2) Mode 1 (Byte input mode)

In Mode 1, PIO sends out data received from external device to MPU through the port data input register.

(3) Mode 2 (Byte input/output mode)

Mode 2 is an operation mode which combined Mode 0 and Mode 1. Mode 2 is used at Port A only.
In this mode, all of 4 handshake control lines are used. The handshake control line of Port A is used for data output, and that of Port B for data input. Port A is used for data transfer and Port B is set in Mode 3 (Bit mode) under which the handshake control line is not used. Interrupt timing generation is nearly the same in both Mode 0 and Mode 1. In case of the input operation, the handshake control line of Port B is used and therefore, the interrupt vector written into Port B is transferred. It is therefore possible to control interrupt of input and output operation by different vectors.

(4) Mode 3 (Bit mode)

Mode 3 is an operation mode which each bit of 8-bit port can be handled as an input or output. Since the handshake control line is not used, normal read/write can be performed.

In case of write, data sent from MPU to PIO is latched in the data output register corresponding to bits which are set for output at the same timing as in Mode 0.
Interrupt is generated under the enabled state and when the condition specified in interrupt control register is satisfied for the bits which is set as an input. However, if Port A is operating in Mode 2, Port B cannot generate interrupt in the bit mode. Further, when the interrupt is used, the interrupt of a bit which is set for output is inhibited, a mask control register bit corresponding to that bit is set to 1.

3.4 Status change flowchart and basic timing

3.4.1 Status change flowchart

The status change flowchart of PIO is shown in Fig. 3.4 .

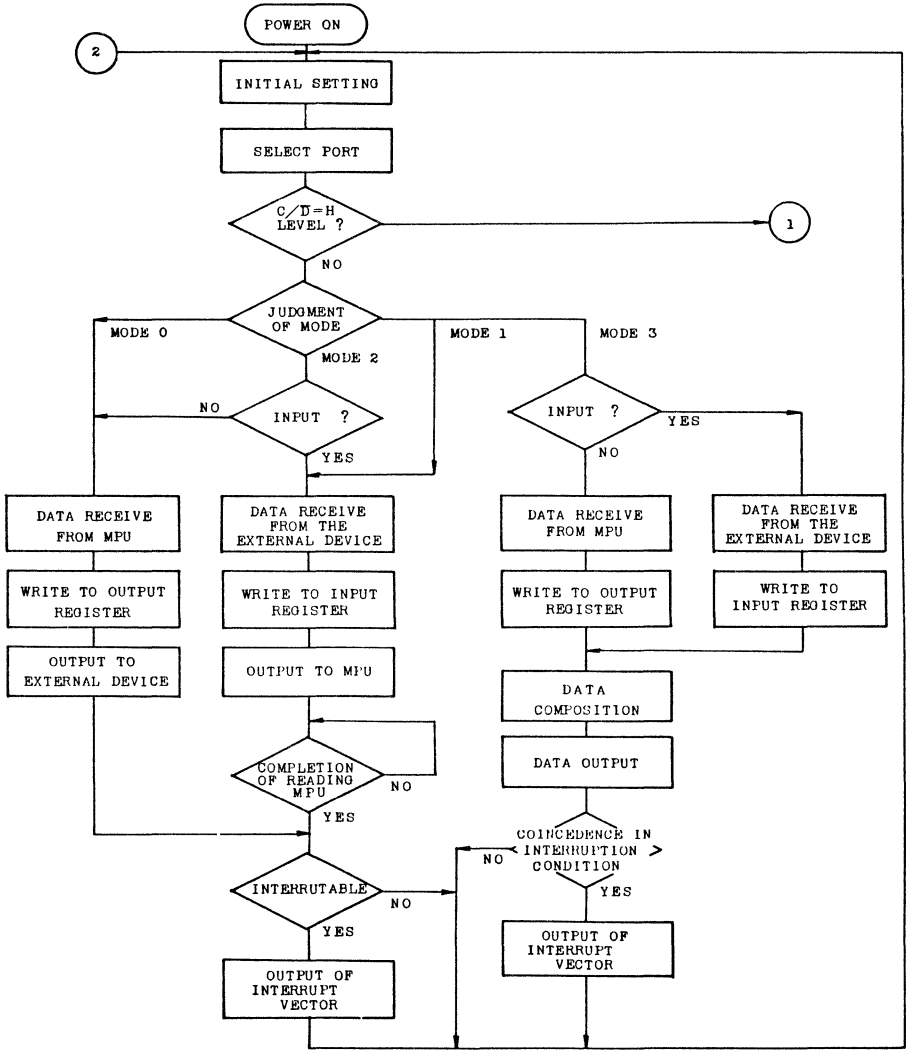


Fig. 3.4 (a) Status Change Flowchart of PIO

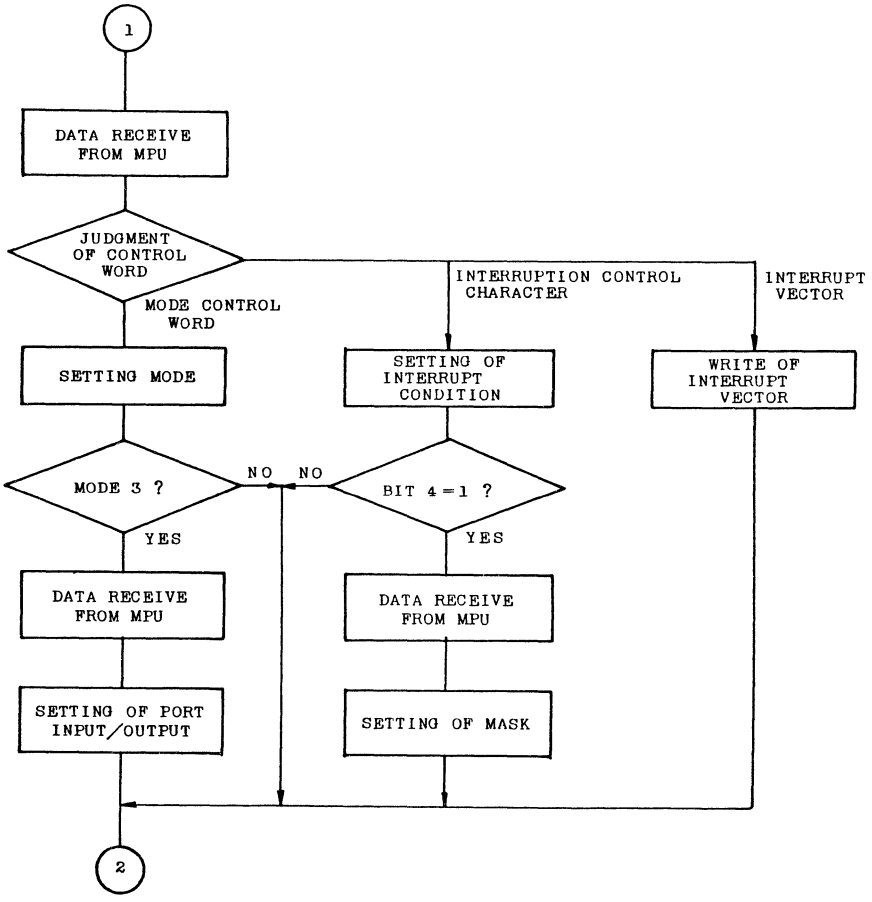
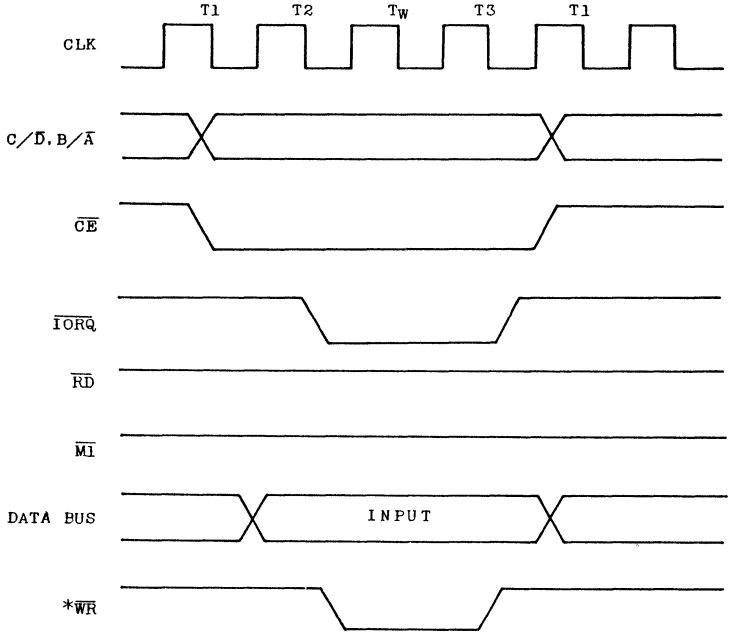


Fig. 3.4 (b) Status Change Flowchart of PIO

3.4.2 Write cycle

Write signal (*WR) is produced in the PIO by IORQ, RD, C/D and CE signals. At the system clock T2 state, MPU changes the IORQ terminal to L level and starts the write cycle. At this time, in order to show the write eycle. M1 terminal needs to be H level. Furhter, signals are sent from MPU to the B/A terminal and C/D terminal of PIO, respectively, to designate selection of port, control signal or data. Thus, the data output register for the selected port of PIO can latch data at the system clock T3 state. TW is the waiting state that is automatically added by MPU.



$*\overline{WR} = C/\overline{D} \cdot \overline{CE} \cdot \overline{IORQ}$

Fig. 3.5 Write Cycle Timing

3.4.3 Readout cycle

At the system clock T2 state, MPU sets the RD, CE and IORQ terminals of the PIO at L level and starts the read cycle. At this time, in order to show the read cycle it is necessary to set the M1 terminal at H level. The PIO output data by CE, IORQ or RD signal. TW is the waiting state that is automatically added by MPU

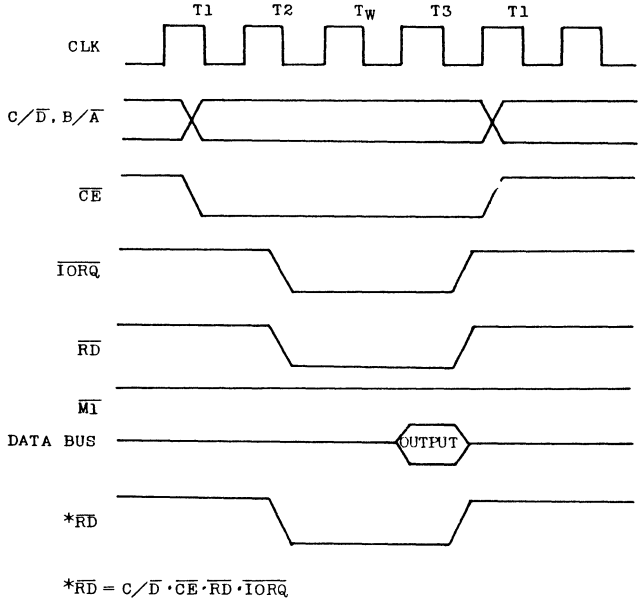


Fig. 3.6 Readout Cycle Timing

3.4.4 Mode 0 (Byte output mode)

The output cycle in Mode 0 starts when MPU executes an output command. When MPU executes the output command, a write signal (*WR) is produced in the PIO in the write cycle. Data on the data bus is latched by this signal in the data output register of the selected port. The RDY terminal becomes H level at the first fall of the system clock after the rise of the write signal (*WR). This indicates that data from the data output register is already on the port I/O terminal.

The external device sets the RDY terminal to L level at the fall of the first system clock after the rise of the STB terminal through which information of receipt of this data is input to the PIO, and waits next output command.

If it is the interrupt enabled state at this time, the INT terminal is set to L level at the rise of the STB terminal and the interrupt request signal is output to MPU. The timing chart of Mode 0 is shown in Fig. 3.7.

3.4.5 Mode 1 (Byte input mode)

The input cycle is started when MPU completed the preceding data read. The external device sets the STB terminal of the PIO to L level and loads data on the port I/O line.

The RDY terminal becomes L level at the first fall of the system clock after the rise of the STB terminal to inhibit the external device to send out next data.
If it is the interrupt enabled state at this time, the INT terminal is set to L level at the rise of the STB terminal and the interrupt is requested to MPU.

When MPU executes the input command by the interrupt routine, the read signal (*RD) is produced in the PIO in the read cycle. This signal outputs data from the selected port data input register to the data bus, and MPU receives this data. The RDY terminal becomes H level at the first fall of the system clock after the rise of the read signal (*RD) and next input is waited. The timing chart of Mode 1 is shown in Fig. 3.8.

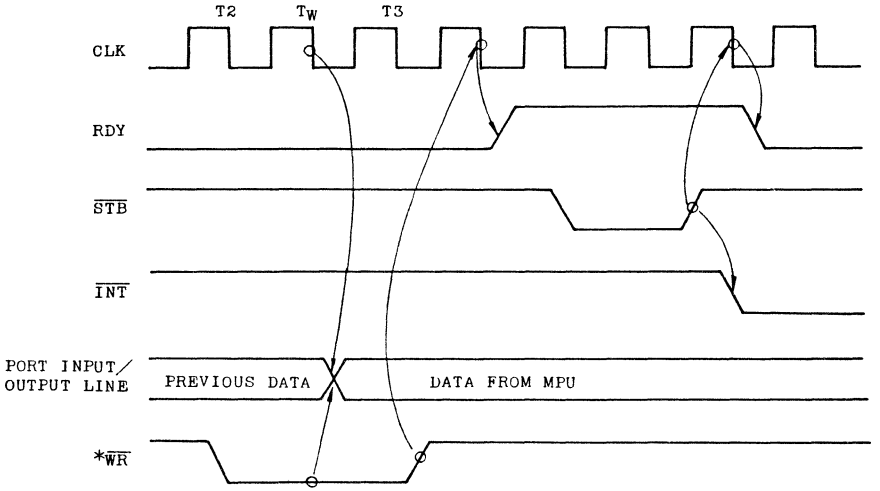


Fig. 3.7 Mode 0 Timing

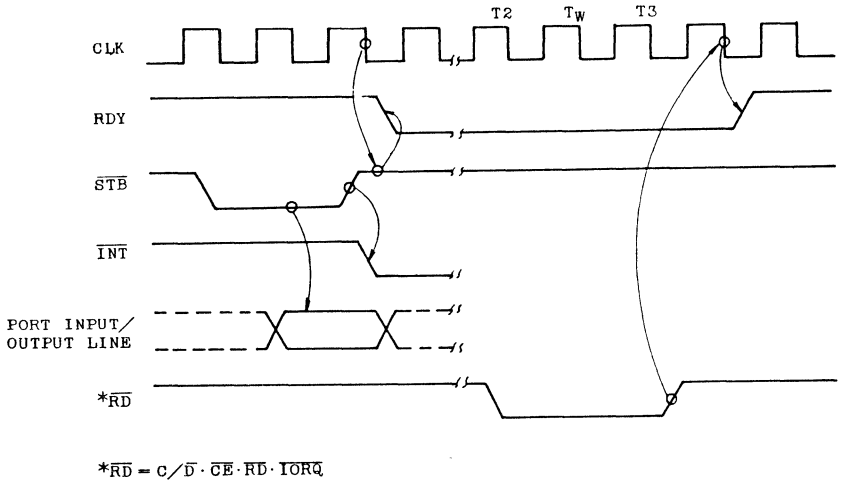
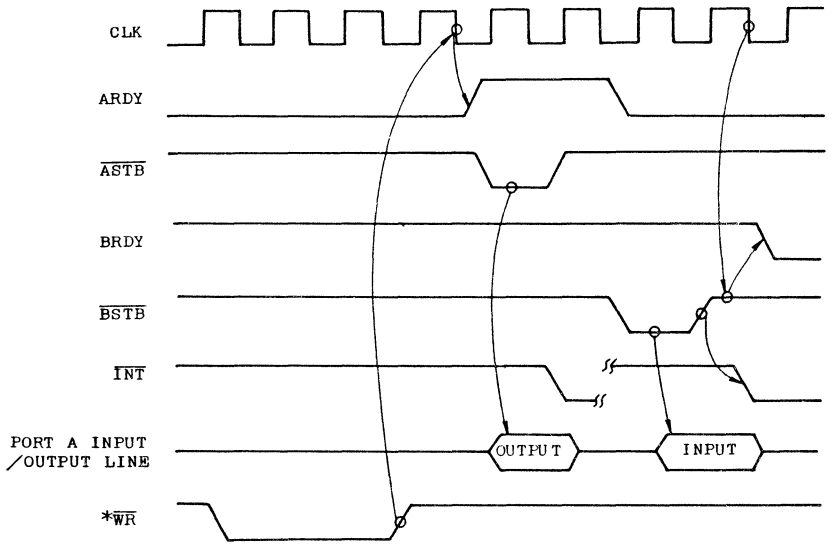


Fig. 3.8 Mode 1 Timing

3.4.6 Mode 2 (Byte input/output mode)

Mode 2 is an operation mode combining Mode 0 and Mode 1.
The timing of output operation is almost identical to that of Mode 0. However, in Mode 2 data is output only when the ASTB terminal is at L level while in Mode 0, data is always output to the port input/output line. External devices can receive data at the rise of the ASTB signal using it as a latch signal.
The timing of input operation is identical to that of Mode 1.
The handshake line of Port A is used for output control and the handshake line of Port B for input control.
Further, the interrupt vector produced by the BSTB signal when Port A is in input operation and that produced when Port B is used in Mode 3 will become the same value. For this reason Port B masks all bits by setting the mask control words so that the interrupt function is not used.



$*\overline{WR} = C/\overline{D} \cdot \overline{CE} \cdot \overline{IORQ}$

Fig. 3.9 Mode 2 Timing

3.4.7 Mode 3 (Bit mode)

In this mode, the handshake line is not used. Therefore, the normal port read/write can be performed and read and write of the port is possible any time. Write from MPU is latched in the data output register corresponding to a bit which is set for output at the same timing as that of Mode 0. Except when Port A is used in Mode 2, the RDY terminal of a port operating in Mode 3 is fixed at L level and data being transferred is composed of two data of the data output register and data input register. That is, data in bits that are set for output and data in bits set for input are composed into one data.

Interrupt is generated when the interrupt is enabled and bits that are set for input satisfy conditions specified by the mask control register and interrupt control register. However, when Port A operates in Mode 2, Port B is not capable of producing any interrupt in Bit Mode. Further, when the interrupt is used, in order to inhibit interrupt of a bit that is set for output, a mask register bit corresponding to that bit is set to 1.

An interrupt request is generated at the point of time when the logical condition becomes true. In addition, when the logical condition becomes true immediately before the M1 terminal becomes L level or the M1

terminal is at L level, an interrupt is generated at the rise of the M1 terminal.

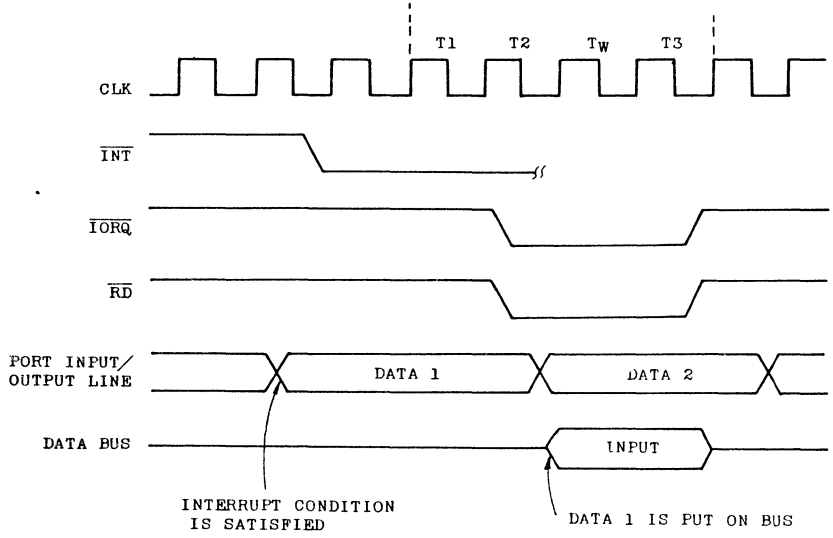


Fig. 3.10 Mode 3 Timing

3.4.8 Interrupt acknowledge cycle

At the same time INT signal set to L level, the PIO sets the IEO terminal at L level to inhibit interrupt request from lower priority order LSI.
When receiving the interrupt request signal (INT) from the PIO, MPU sets the M1 and IORQ terminals of the PIO at L level as the interrupt acknowledge signal. The IORQ terminal becomes L level later than the M1 terminal by 2.5 system clocks. In order to stabilize the daisy chain connected signal lines, IEI and IEO signals, the ports and peripheral LSI cannot change interrupt requests during interrupt acknowledge cycle.
The RD terminal is kept at H level to distinguish the interrupt acknowledge cycle from the command fetch cycle. If the IORQ terminal becomes L level when the IEI terminal is at H level, interrupt vector is output to the data bus from the port requesting the interrupt
At this time, 2 system clocks are automatically inserted by MPU as the waiting state to keep stability of the daisy chain connect.

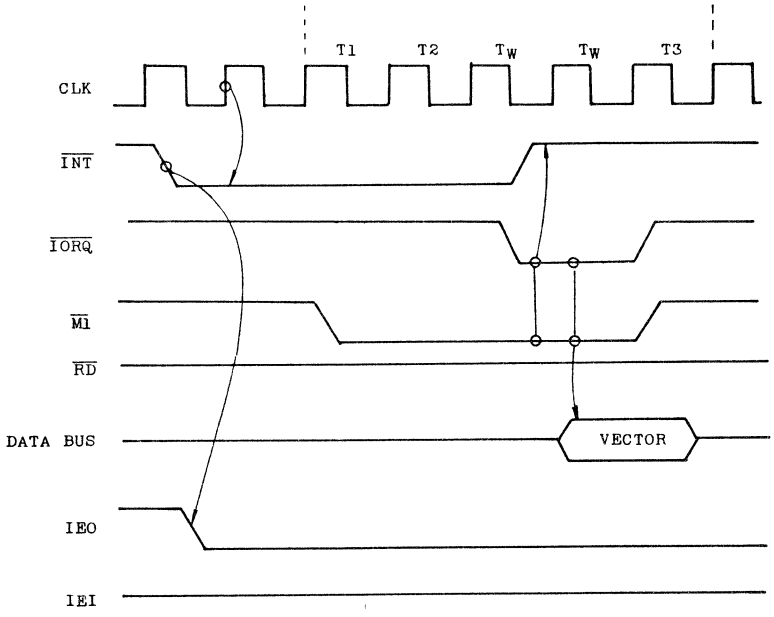


Fig. 3.11 Interrupt Acknowledge Cycle Timing

3.4.9 Return from the interrupt cycle

Return from the interrupt is effected when MPU executes RETI command. This RETI command must be used at the last instruction of the interrupt routine. The execution of this RETI command by MPU returns the IEI and IEO terminals of the PIO to the state before interrupt.

RETI command is a two byte command and its code is EDH and 4DH. The PIO decodes the codes of RETI command and desides a port which makes next interruption request. In the daisy chain structure, at the point of time when the command code EDH is decoded, the IEI terminal of a peripheral LSI making the interrupt is kept at H level and the IEO terminal at L level. If the code following EDH is 4DH, an LSI that transmitted the interrupt immediately before the decoding, that is, only the LSI with IEI terminal at H level and IEO terminal at L level is returned from the interrupt. As a result, the interrupt process of a lower priority peripheral LSI was suspended.

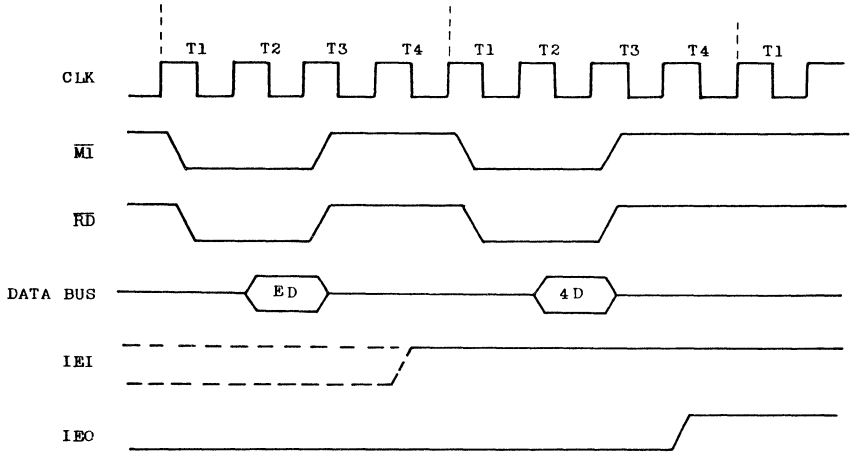


Fig. 3.12 Return Timing from Interrupt Cycle

3.5 Operating procedures

To operate the PIO it is necessary to write several control registers into the PIO for initialization.

On a system with the C/D terminal connected to the Address A0 and B/A terminal connected to Address A1, the write is performed separated for Port A and B.

B/$\overline{A}$ (A1)	C/$\overline{D}$ (A0)	$\overline{CE}$	Register Select
0	0	0	PORTA DATA REGISTER.
0	1	0	PORTA CONTROL REGISTERS
1	0	0	PORTB DATA REGISTER.
1	1	0	PORTB CONTROL REGISTERS
x	x	1	-

(1) Interrupt vector register

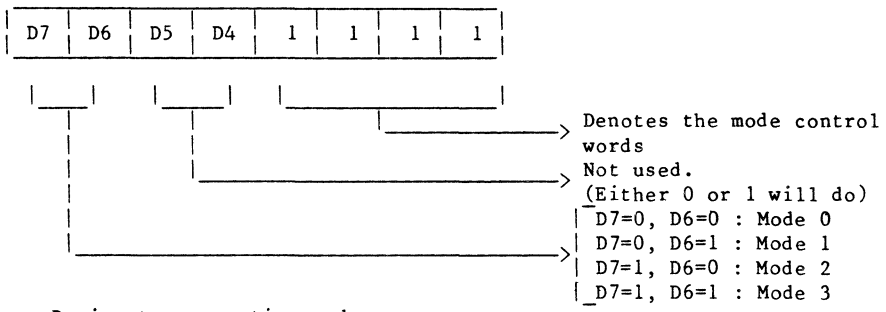
D7	D6	D5	D4	D3	D2	D1	0

Denotes the interrupt vector words

Interrupt vectors given by user

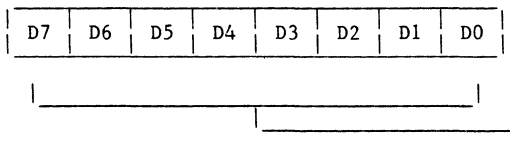
- o MPU generates the start address of the interrupt processing routine by this vector and the content of address shown by the control of I register of MPU.
- o D1 to D7 are written into the interrupt vector register.
- o If no interrupt is used, the interrupt vector words are not required.

(2) Mode control register



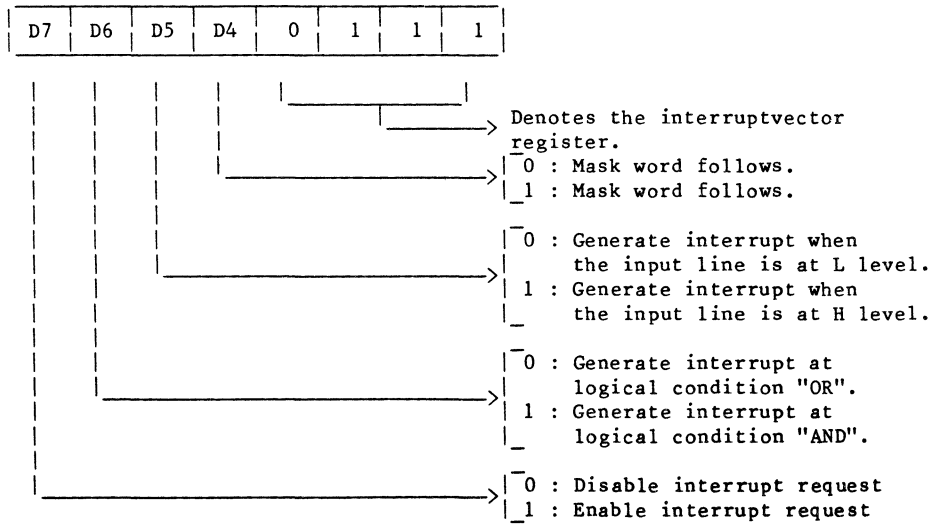
- o Designates operation modes.
- o D7 and D6 are written into the mode control register.

(3) Data input/output control register



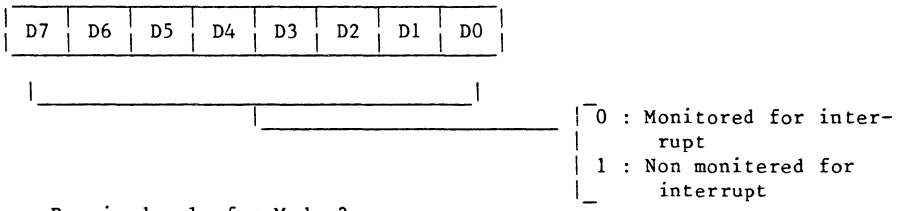
- o Required only for Mode 3
- o When Mode 3 is designated by mode control register, write following a mode control register.
- o Designates each termnal of the port for output or input.
- o D0 to D7 are written into the data input/output register.

(4) Interrupt control register



- Set the interrupt generating conditions.
- D4, D5 and D6 are used only in Mode 3.
- If D6 is set at 0 (D6=0), interrupt is generated when any one bit that is not masked (monitored) by the mask control register become active.
- If D6 is set at 1 (D6=1), interrupt is generated when all bits that are not masked (monitored) by the mask control register become active.
- If D4=1, all bits which are pending will be reset in any operation mode.
- D5 and D6 are written into the interruption control register.

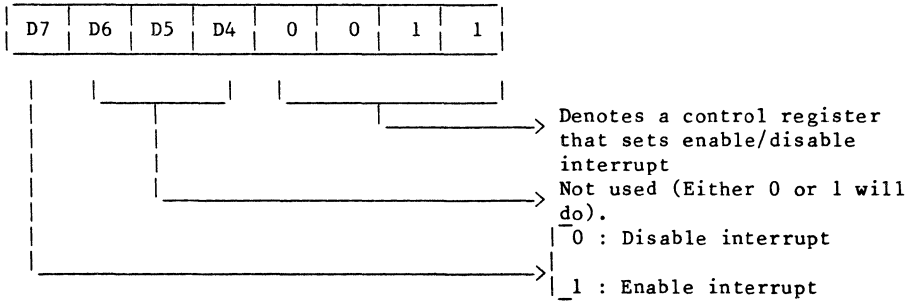
(5) Mask control register



- Required only for Mode 3
- If D4 is set at 1 (D4=1) by the interrupt control register, the mask control word is written following the interrupt control register.
- If a bit is set at 0, the corresponding input line is monitored.
- If a bit is set at 1, the corresponding input line is not monitored.
- The PIO checks only the input line which has 0 data and requests interrupt if the interrupt generation condition is satisfied.
- D0 to D7 are written into the mask control register.

Since four handshake control lines are all used in setting Port A in Mode 2, it is necessary to set Port B in Mode 3 in which the handshake control line is not used. In this case, all bits should be masked by the mask control register (all bits are set at 1).

(Note) It is possible to set only generation of interrupt by the control register shown below.



4. ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
VCC	Supply Voltage	-0.5 to +7	V
VIN	Input Voltage	-0.5 to Vcc + 0.3	V
PD	Power Dissipation	250	mW
TSOLDER	Soldering Temperature (10 sec)	260	°C
Tstg	Storage Temperature	-65 to 150	°C
Topr	Operating Temperature	-40 to 85	°C

4.2 DC ELECTRICAL CHARACTERISTICS

TA = -40°C to 85°C, VCC = 5V ± 10%, VSS = 0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VILC	Low Clock Input Voltage		-0.3	-	0.6	V
VIHC	High Clock Input Voltage		VCC-0.6	-	VCC+0.3	V
VIL	Low Input Voltage (Except CLK)		-0.5	-	0.8	V
VIH	High Input Voltage (Except CLK)		2.2	-	VCC	V
VOL	Output Low Voltage	IOL = 2.0mA	-	-	0.4	V
VOH1	Output High Voltage (I)	IOH = -1.6mA	2.4	-	-	V
VOH2	Output High Voltage (II)	IOH = -250uA	VCC-0.8	-	-	V
IL1	Input Leakage Current	VSS ≦ VIN ≦ VCC	-	-	±10	uA
ILO	3-state Output Leakage Current in Float	VSS + 0.4 ≦ VOUT ≦ VCC	-	-	±10	uA
ICC1	Power Supply Current	VCC=5V, fCLK=(1), VILC=VIL=0.2V, VIHC=CIH=VCC-0.2V	P/F AP/AF -	2	5	mA
			AP-6 /AF-6 -	3	8	mA
ICC2	Standly Supply Current	VILC=VIL=0.2 VIHC=VIH =VCC-0.2V	-	0.5	10	uA
IOHD*	Darlington Drive Current,(2)	VOH=1.5V REXT = 1.1K	-1.5	-	-5.0	mA

Note (1) fCLK=1/tcC(MIN.)
(2) Port B only

4.3 AC ELECTRICAL CHARACTERISTICS

TA = -40°C to 85°C, VCC = 5V ± 10%, VSS = 0V

NO.	SYMBOL	PARAMETAER	4MHz P/AP/AF		6MHz AP-6/AF-6		UNIT
			MIN.	MAX.	MIN.	MAX.	
1	TcC	Clock cycle time	250	DC	165	DC	ns
2	TwCh	High clock pulse width	105	DC	65	DC	ns
3	TwCl	Low clock pulse width	105	DC	65	DC	ns
4	TfC	Clock falling time	-	30	-	20	ns
5	TrC	Clock rising time	-	30	-	20	ns
6	TsCS(RI)	$\overline{CE}$, B/$\overline{A}$ and C/$\overline{D}$ Set-up time for $\overline{RD}$, IORQ	50	-	50	-	ns
*7	Th	Hold time	40	-	40	-	ns
8	TsRI(C)	$\overline{RD}$, $\overline{IORQ}$ set-up time for clock rise	115	-	70	-	ns
9	TdRI(DO)	Delay from $\overline{RD}$, $\overline{IORQ}$ fall to data output	-	380	-	300	ns
10	TdRI(DOs)	Delay from $\overline{RD}$, $\overline{IORQ}$ rise to data float	-	110	-	70	ns
11	TsDI(C)	Data set-up time for clock rise	50	-	40	-	ns
12	TdIO(DOI)	Delay from $\overline{IORQ}$ fall of INTA cycle to data output	-	160	-	120	ns
13	TsMl(Cr)	$\overline{M1}$=L set-up time for clock rise	90	-	70	-	ns
14	TsMl(Cf)	$\overline{M1}$=H set-up time for clock fall ($\overline{M1}$ cycle)	0	-	0	-	ns
15	TdMl(IEO)	Delay from $\overline{M1}$ fall to IEO fall	-	190 (1)	-	100	ns
16	TsIEI(IO)	IEI set-up time for $\overline{IORQ}$ fall (INTA cycle)	140	-	100	-	ns
17	TdIEI(IEOf)	Delay from IEI fall to IEO rise	-	130	-	120	ns
18	TdIEI(IEOr)	Delay from IEI rise to IEO fall	-	160	-	150	ns
19	TcIO(C)	$\overline{IORQ}$=H set-up time for clock fall	200	-	170	-	ns
20	TdC(RDYr)	Delay from clock fall to READY rise	-	190	-	170	ns
21	TdC(RDYf)	Delay from clock fall to READY fall	-	140	-	120	ns
22	TwSTB(C))	STROBE pulse width	150 (2)		120 -	-	ns

NO.	SYMBOL	PARAMETAER	4MHz P/AP/AF MIN.	4MHz P/AP/AF MAX.	6MHz AP-6/AF-6 MIN.	6MHz AP-6/AF-6 MAX.	UNIT
23	TsSTB(C)	Set-up time of $\overline{\text{STROBE}}$ rise for clock fall (in case of making READY to active by next cycle)	220	-	150	-	ns
24	TdIO(PD)	Delay from $\overline{\text{IORQ}}$ rise to port data stable (Mode 0)	-	180	-	160	ns
25	TsPD(STB)	Data set-up time for $\overline{\text{STROBE}}$ rise (Mode 1)	230	-	190	-	ns
26	TdSTB(PD)	Output data delay time from $\overline{\text{STROBE}}$ fall (Mode 2)	-	210	-	180	ns
27	TdSTB(PDr)	Delay from $\overline{\text{STROBE}}$ rise to data float (Mode 2)	-	180	-	160	ns
28	TdPD(INT)	Delay from port data match to $\overline{\text{INT}}$ fall (Mode 3)	-	490	-	430	ns
29	TdSTB(INT)	Delay from $\overline{\text{STROBE}}$ rise to $\overline{\text{INT}}$ fall (Mode 2)	-	440	-	350	ns

Note 1 Item with * mark (No.7) is not compatible with NMOS Z80 PIO.

Note 2 (1) If the daisy chain is at N stage,
2.5 TcC>(N-2)TdIEI(IEOf)+(TdMl(IEO)+TsIEI(IO)+TTL buffer delay must be satisfied.

(2) In Mode 2, TwSTB>TsPD(STB) must be satified.

(3) AC test condition : Input - VIH=2,4V, VIHC=VCC-0.6V, VIL=0.4V, VILC=0.6V
Output - VOH=2.2V, VOL=0.8V
CL=100pF

4.4 Capacitance

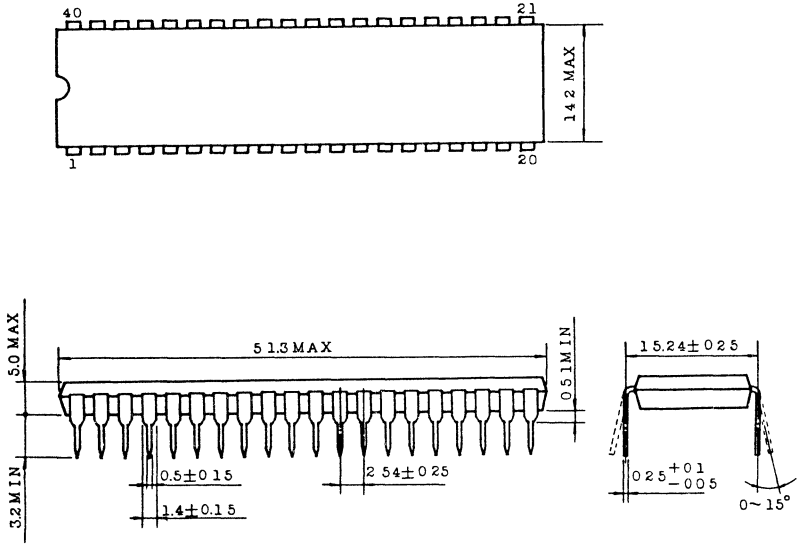
TA = 25°C

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{CLOCK}	Clock Input Capacitance	f=1MHz All terminals except that to be measured should be earthed.	-	-	5	pF
CIN	Input Capacitance		-	-	5	pF
COUT	Output Capacitance		-	-	10	pF

5. Package Dimension

Unit in mm

5.1 Plastic Package

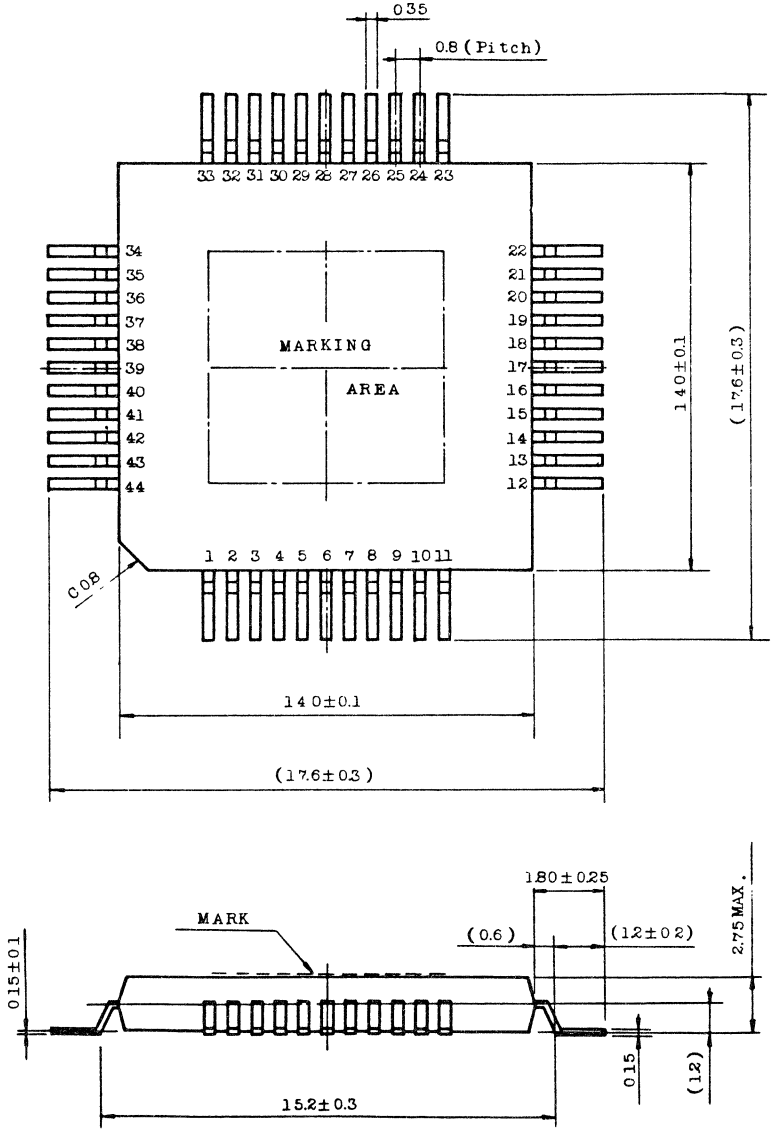


Note 1. This dimension is measured at the center of bending point of leads.

Note 2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoretical positions with respect to No.1 and No.40 leads.

Unit in mm

5.2 44-pin mini-flat package



TMPZ84C30P, TMPZ84C30AP, TMPZ84C30AP-6, TMPZ84C30F, TMPZ84C30AF, TMPZ84C30AF-6
TLCS-Z80 CTC: COUNTER TIMER CIRCUIT

1. General Description and Features

The TMPZ84C30P (hereinafter referred to as CTC) is CMOS version of Z80 CTC and has been designed to provide low power operation.
The TMPZ84C30P is fabricated using Toshiba's CMOS Silicon Gate Technology.

The principal functions and features of the CTCs are as follows.

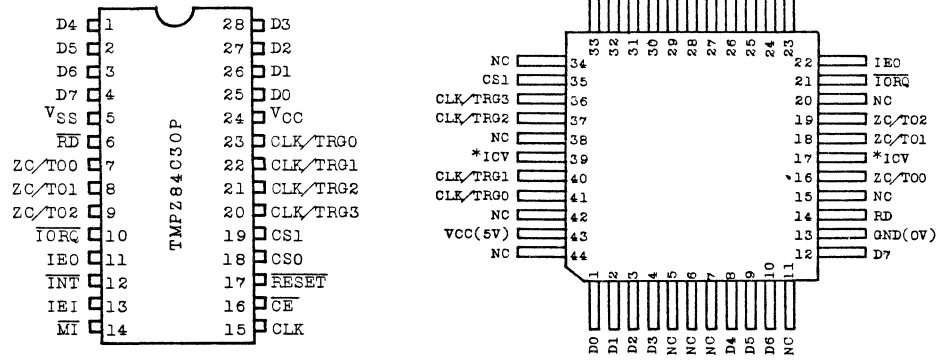
(1) Compatible with the Zilog Z80 CTC.
(2) Low power consumption
  3mA Typ. (@5V @4MHz) ... TMPZ84C30P/F
  2.5mA Typ. (@5V @4MHz) ... TMPZ84C30AP/AF
  4mA Typ. (@5V @4MHz) ... TMPZ84C30AP-6/AF-6
  10uA Max. (@5V, Stand-by)
(3) DC to 4MHz operation ... TMPZ84C20P/F, TMPZ84C20AP/AF
  DC to 6MHz operation ... TMPZ84C20AP-6/AF-6
(4) Signle 5V power supply and single-phase clock. 5V $\pm$ 10%
(5) Capable of driving Darlington transistors.
(6) Four independent countor/timer channels each of which is capable of independently selecting Timer Mode and Counter Mode.
(7) Each channel is provided with a prescaler to divide system clock into 16 or 256.
(8) Built-in interrupt control logical operation circuit allows priority processing of interrupt in Daisy-chain structrure and automatic loading of 8 bit interrupt vector on the system bus.
(9) Four channels occupy 4 successive positions in the Daisy-chain structure. Most significant channel is Channel 0 and least significant channel is Channel 3.
(10) In both modes, at the zero count, the content of the time constant register is automatically loaded on the down counter.
(11) In either Counter Moder or Timer Mode, the content of the down counter is readable by the microporcessor (hereinafter referred to as MPU).
(12) Interrupt function available in Z80 MPU Mode 2.
(13) In Timer Mode, the timer operation is selectable at the rise or fall of the starting trigger. In addition, in Counter Mode the decrement (-1) of the content of the down counter either at the rise or fall of external clock is selectable.
(14) Programming to generate interrupt by zero count by the down counter in each channel is possible.
(15) 40 pin DIP package, 44 pin Mini Flat package.

(Note) Z80(R) is a registered trademark of Zilog Inc., U.S.A

2. Pin Connections and Pin Functions

2.1 Pin connections (Top View)

The pin connections of the CTC are as shown in Fig. 2.1.



(Note) NC must be used at open condition.
*ICV must be used at open
Condition or Connected with Vcc.

(a) DIP Pin Connection (b) MFP Pin Connection

Fig. 2.1 DIP Pin Connections

2.2 Pin names and functions

I/O pin names and functions are as shown in Table 2.1.

Table 2.1 Pin Names and Functions

Pin Name	Number of Pin	Input/Output 3-state	Function
D0 - D7	8	I/O 3-state	8-bit bidirectional data bus. Data transfer between MPU and PIO
$\overline{RD}$	1	Input	Read signal. This signal is used in combination with $\overline{IORQ}$ and $\overline{CE}$/P signals for transfer of data and channel control words between MPU and CTC.
ZC/T00 : ZC/T02	1	Output	In both counter and timer modes the output is an active high pulse when the down-counter decrements to zero.

Pin Name	Number of Pin	Input/Output 3-state	Function
$\overline{IORQ}$	1	Input	I/O request signal. This signal is used in combine with $\overline{RD}$ and $\overline{CE}$ signals for transfer of data and channel control words between MPU and CTC.
IEO	1	Output	Interruption enable output. Controls interruptions by subordinate peripheral LSI's in the Daisy-chain structure. This terminal becomes H level only when the IEI terminal is at H level and MPU is not providing the interruption service to channels in CTC.
$\overline{INT}$	1	Output	Interruption request. This terminal becomes L level if a downcounter for any channel in CTC counts zero when the IEI terminal is at H level and interruption is authorized by a program.
IEI	1	Input	Interruption enable input. This terminal indicates presence of interruption by a host peripheral LSI.
$\overline{MI}$	1	Input	Machine cycle 1. Informs the machine cycle from MPU. In combination with the $\overline{ROD}$ signal, indicates that MPU fetches commands from the memory, and in combination with the $\overline{IORQ}$ signal, indicates that MPU is in the interruption acknowledge cycle. This terminal is used, in combination with the $\overline{IORQ}$ signal, to send the interruption vector to MPU.
CLK	1	Input	Single-phase clock input. Single-phase Z80 standard system clock is inputted to this terminal. When this CLK terminal is in the DC state (high or low level), the CTC is placed in the stationary state.
$\overline{CE}$	1	Input	Chip enable. Used to write MPU-CTC channel control word, interruption vector, and time constant or to read the content of a downcounter for each channel in combination with the $\overline{IORQ}$ and $\overline{RD}$ terminals.
$\overline{RESET}$	1	Input	Reset signal. When the reset signal is inputted to this terminal, all channels stop to operate and interruption enable bits in all channel control registers are reset. This $\overline{RESET}$ terminal must be kept at L level for at least 3 system clocks.
CS0 - CS1	1	Input	Channel selection. Any one of four channels of the CTC is selected by 2-bit code at time of read/write.

Pin Name	Number of Pin	Input/Output 3-state	Function
CLK/TRG0 : CLK/TRG3	4	Input	External clock/timer trigger. There are 4 CLK/TRG terminals correresponding to 4 channels. At the leading or trailing edge of active signals which are inputted through these terminals, the content of down counter is decremented (-1) in Counter Mode, while the timer operation is started in Timer Mode. Active leading edge or trailing edge is selectable.
Vcc	1	Power Supply	+5V
Vss	1	Power Supply	0V

3. Functional Description

3.1 Block diagram
The block diagram of CTC is shown in Fig. 3.1.

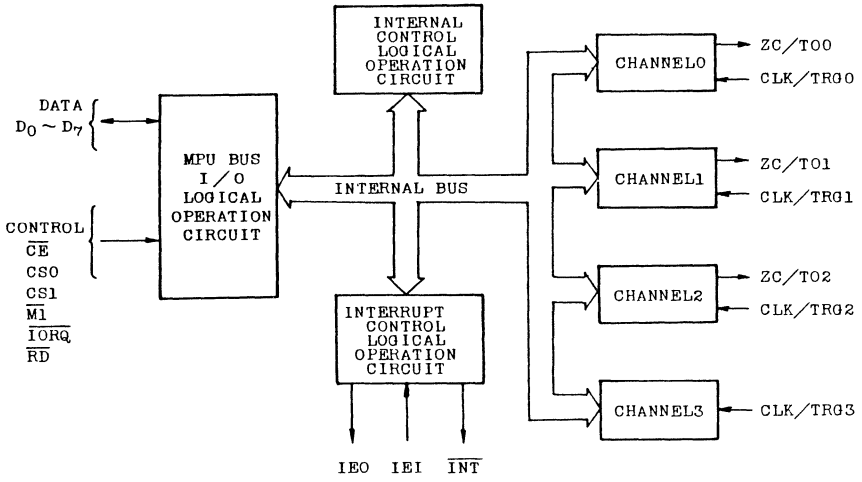


Fig. 3.1 Block Diagram

3.2 System cinfiguration
The system configuration of CTC consists of four logical operation circuits as below.
(1) MPU Bus Input/Output Logical Operation Circuit
(2) Channel Control Logic
(3) Interruption Control Logical Operation Circuit
(4) 4 Independent Counter/Timer Channel Logical Circuit

3.2.1 MPU bus input/output logical operaton circuit
This is a circuit for connecting CTC to MPU. This circuit connects CTC directly to MPU without using other external circuit. However, if a system becomes large, it becomes necessary to provided an address decoder and a line buffer.

3.2.2 Internal control logical operation circuit
This circuit controls the overall chip operation function like the chip enable, reset and read/write circuit.

3.2.3 Interruption control logical operation circuit

This circuit performs processes of MPU relative to interruption such as decision of priority, etc.
Priority of peripheral LSI's is decided according to their physical locations in the Daisy-chain connection.

3.2.4 Counter/timer channel logical operation circuit

This counter/timer channel logical operation circuit consists of the following two registers and two counters. The figures shown in parentheses is number of bits. The configuration of this counter/timer channel logical operation circuit is shown in Fig. 3.2.

- o Time constant register (8-bit)
- o Channel control register (8-bit)
- o Downcounter (8-bit)
- o Prescaler (8-bit)

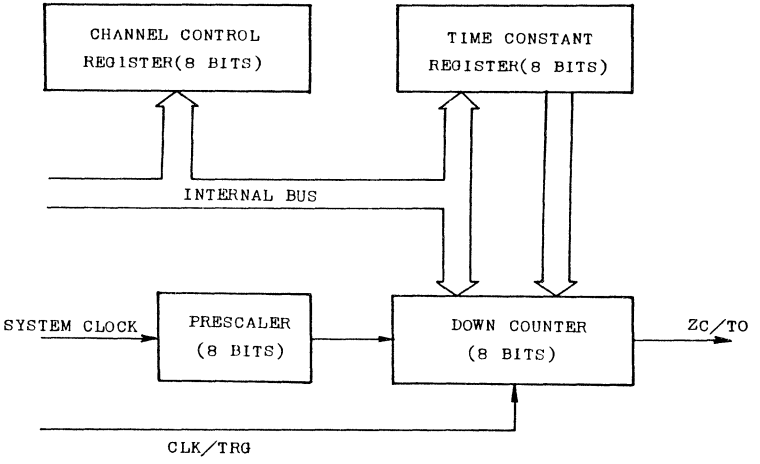


Fig. 3.2 Counter/Timer Channel Logical Circuit

(1) Timer constant register

This register retains time constants that are written into the down-counter. When the CTC is initialized or the downcounter counts zero, time constants are loaded on the downcounter. Time constants are set immediately after MPU writes channel control word into the channel control register. Time constants that can be set are integers ranging from 1 to 256.

(2) Channel control register

This register selects channel modes and conditions by the channel control word provided from MPU.

(3) Downcounter

The content of the time constant register is loaded on this downcounter and its content is decremented (-1) at every edge of external clock in case of Counter Mode and for every clock output of the prescaler in case of Timer Mode. The content of the time constant registger is loaded at time of initialization and when the downcounter counts zero.
The content of the downcounter can be read out anytime. In addition, it is also possible to program so as to generate an interruption request every time when the downcounter counts zero.

(4) Prescaler
The prescaler is used only in Timer Mode and divides the system clock into 1/16 or 1/256. Whether the system clock is to be divided into 16 or 256 is programmed by the channel control word. Further, output of the prescaler becomes clock input to the downcounter.

3.3 Basic operation

3.3.1 Reset
After power ON, the CTC is in the unstable state. To stabilize the CTC, apply a signal of L level to the RESET terminal. Before starting any channel in Counter Mode or Timer Mode, it is necessary to write the channel control word and time constant data into the registers for the channel to be started. In addition, to make a programming to enable interruption, it is necessary to write the interruption vector words into the interruption control circuit. When these data are written into the CTC, it becomes ready to start.

3.3.2 Interruption
The CTC is capable of producing the interruption while MPU is operating in Mode 2.
The interruption by the CTC can be programmed for each channel and the interruption request signal (INT) is output every time when the downcounter of each channel counts zero. When MPU accepts the interruption request from the CTC, the CTC outputs the interruption vector. Based on this interruption vector, MPU designates the top address of the interruption processing routine and MPU starts the interruption process by calling this interruption processing routine.

Since MPU designates the top address of the interruption processing routine by the interruption vector received from the CTC, users can call optional address by changeing this vector value.
The interruption process is ended when MPU executes RETI command. The CTC is provided with the RETI command decoding circuit and is therefore able to know end of the interruption process by constantly monitoring the data bus.
Interruption priority among peripheral LSIs is decided by their connection in the Daisy-chain structure. Peripheral LSIs are connected in series and higher priority is given to peripheral LSIs which are located physically more closer to MPU. Further, as to the priority of channel in the CTC, the highest priority is given to channel 0 and priority beocmes lower in order of Channel 1, 2 and 3.

Peripheral LSI's have the signal lines for the IEO and IEI terminals, and the IEO terminal of a host peripheral LSI is connected to the IEI terminal of a subordinate peripheral LSI. However, the IEI terminal of a peripheral LSI with the highest priority is connected to the +5V power terminal and the IEO terminal of a lowest priority peripheral LSI is not used. Interruption under this condition is generated according to the following rules:

- o When the IEO and IEI terminals are both at H level, no interruption is generated. At this time, the INT terminal is at H level. In this state, the interruption request can be available.
- o When the CTC output the interruption request signal (INT), this CTC resets the IEO terminal to L level. When the interruption is accepted by MPU, the INT terminal returns to H level.
- o When the IEI terminal becomes L level, the IEO terminal also becomes L level.
- o When the IEI terminal is at L level, no interruption request can be available.
- o If the IEI terminal is turned to L level while the interruption is generating, the interruption process is kept suspended.

3.3.3 Operation Modes

The CTC is operated in the following alternative operation modes. Selection of these modes is performed by writing the channel control word.

- o Counter Mode
- o Timer Mode

(1) Counter mode

In counter mode, number of input edges at the CLK/TRG terminal is counted and after inputting pulses. The content of the downcounter is decremented by -1 synchronizing with the rise of next system clock. Pulse edge to be counted can be designated either at the leading or trailing edge by the channel control word.

When the content of the downcounter becomes zero, time constant data that are written into the time constant register are automatically loaded into the downcounter. To load new time constant data into the downcounter, new time constant data is written into the time constant register. These new data will be loaded after the present counting operation is ended.

(2) Timer mode

In timer mode, a time interval of integral number times of the system clock cycle is generated. The time interval is measured on the basis of the system clock, and system clock is supplied to the prescaler. The prescaler divides this system clock into 1/16 or 1/156. Further, output of the prescaler is used as the clock to decrement (-1) the downcounter. Time constant data is automatically loaded onto the downcounter every time when the downcounter counts zero in the same manner as in Counter Mode.

When the content of the downcounter is reduced to zero, pulse in the fixed cycle is output from the ZC/TO terminal.

This pulse is given by the following formula:

tc * P * TC

tc : System clock cycle
P : Prescaler value (16 or 256)
TC : Time constant data (256 at 00H)

Whether the starting of the timer operation is automatically mode or performed at the edge of the CLK/TRG terminal and case of the CLK/TRG terminal, whether it is performed at the leading edge or trailing edge is designated by the channel control word.

3.4 Status change flowchart and basic timing

3.4.1 Status change flowchart

The status change flowchart of CTC is shown in Fig. 3.3

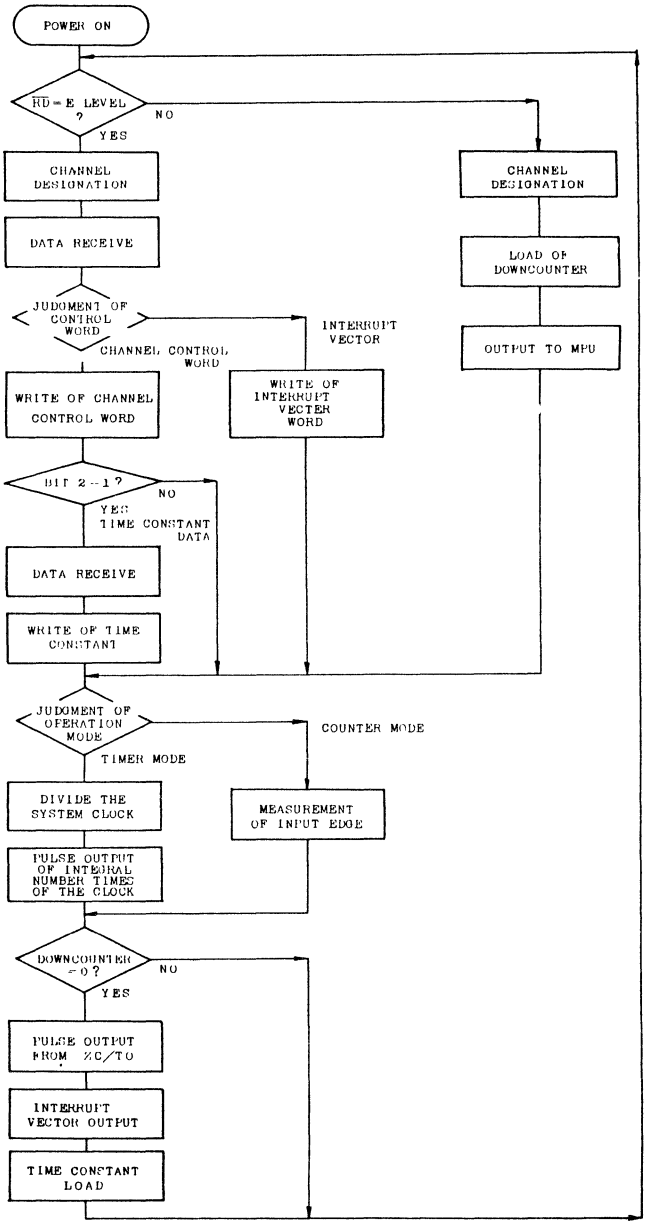


Fig. 3.4 (a) Status Change Flowchart of CTC

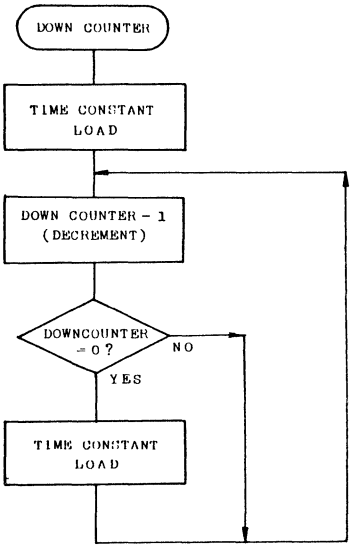


Fig. 3.4 (b) Status Change Flowchart of PIO

3.4.2 Write cycle

The write cycle is used for writing channel control word, interruption vector and time constant.

In the next system clock T2, MPU changes the IORQ terminal of CTC to L level and starts the write cycle. At time of starting the write cycle, a 2-bit code is added to the CS1 and CS0 terminals of the CTC to designate a channel. The CTC internal registers are ready to secure data at the system clock T3. Tw is in the waiting state which is automatically added by MPU.

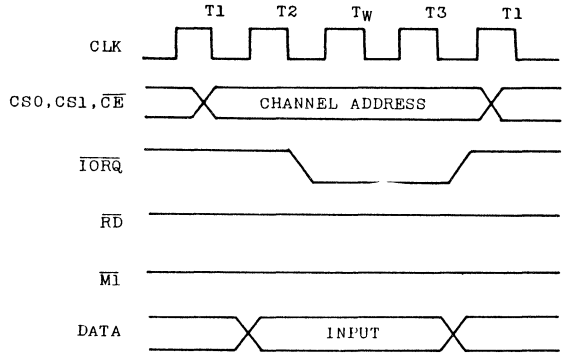


Fig. 3.5 Write Cycle Timing

3.4.3 Readout cycle

The read cycle is used to read out the content of the downcounter. At the system clock T2, MPU sets the RD and IORQ terminals of the CTC at L level and starts the read cycle. At time of starting the read cycle, a 2-bit code is added to the CS1 and CS0 terminals of the CTC to designate a channel. The content of the downcounter at time of the rise of T2 is output to the data bus at the rise of the system clock Tw. Tw is the waiting state which is automatically added by MPU.

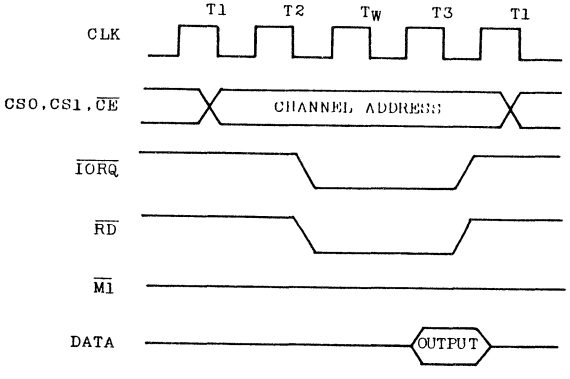


Fig. 3.5 Read Timing

3.4.4 Counter mode

In counter mode, the content of the downcounter is decremented (-1) synchronizing with the system clock by the edge of pulse added from the external circuit connected to the CLK/TRG terminal. Cycle of the pulse added to the CLK/TRG terminal must be larger by two times or more than the system clock. In addition, a setup time becomes necessary between the active edge of the CLK/TRG terminal and the rise of next system clock. If a setup time between the active edge of the CLK/TRG terminal and the rise of next system clock is short. The downcounter decrements its content by one (-1) one cycle behind the system clock.
When the content of the downcounter becomes zero, H level pulse will be output from the ZC/TO terminal.

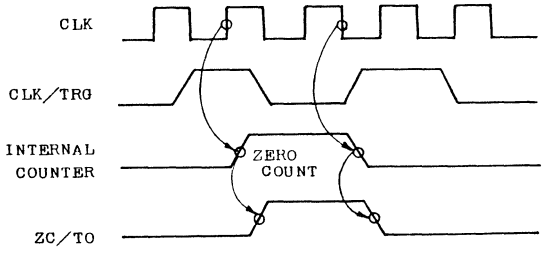


Fig. 3.6 Counter Mode Timing

3.4.5 Timer mode

The timer operation is started by the second rise of system clock at the edge of pulse added from the external circuit conneced to the CLK/TRG terminal. Cycle of the pulse added to the CLK/TRG terminal. Cycle of the pulse added to the CLK/TRG terminal must be larger by two times or more than the system clock. In addition, a setup time becomes necessary between the active edge of the CLK/TRG terminal and the rise of next system clock. If a setup time between the active edge of the CLK/TRG terminal and the rise of next system clock is short. The timer starts one cycle behind the system clock.

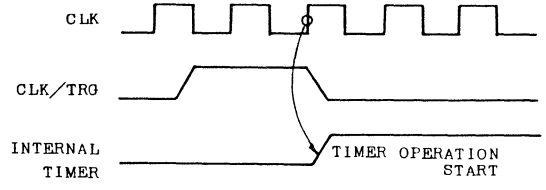


Fig. 3.7 Timer Mode Timing

3.4.6 Interruption acknowledge cycle

After transmitting the interruption reqeust signal (INT), the PIO sets the IEO terminal at L level to inhibit interruption request by low order LSI.

Receiving the interruption request signal (INT) from the CTC, MPU sets the M1 and IORQ terminals of the CTC at L level as the interruption acknowledge signal. The IORQ terminal becomes L level later than the M1 terminal by 2.5 system clocks. In order to stabilize the daisy chain connected signal lines, IEI and IEO signals, each channel cannot change interruption requests.
The RD terminal is kept at H level to distinguish the command fetch cycle from the interruption acknowledge cycle. During this period, the interruption control logical operation circuit in the CTC decide the most high order channel requesting the interruption. If the IORQ terminal becomes L level when the IEI terminal is at H level, interruption vector is output to the data bus from the most high order channel requesting the interruption
At this time, 2 system clocks are automatically inserted by MPU as the waiting state to keep stability of the daisy chain connection.

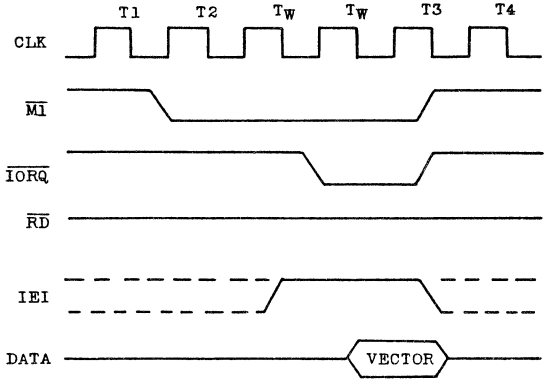


Fig. 3.8 Interruption Acknowledge Timing

3.4.7 Return from the interruption cycle

Return from the interruption is effected when MPU executes RETI command. This RETI command must be used at the last stage of the interruption processing routine. The execution of this RETI command by MPU returns the IEI and IEO terminals of the CTC to the state before interruption.

RETI command is a two byte command and its code is EDH and 4DH. The CTC decodes the codes of RETI command and decides a port which makes next interruption request. In the daisy chain structure, at the point of time when the command code EDH is decoded, the IEI terminal of a peripheral LSI making the interruption is kept at H level and the IEO terminal at L level. If the code following EDH is 4DH, an LSI that transmitted the interruption immediately before the decoding, that is, only the LSI with IEI terminal at H level and IEO terminal at L level is returned from the interruption. As a result, the interruption process of a low order peripheral LSI of which interruption process was suspended.

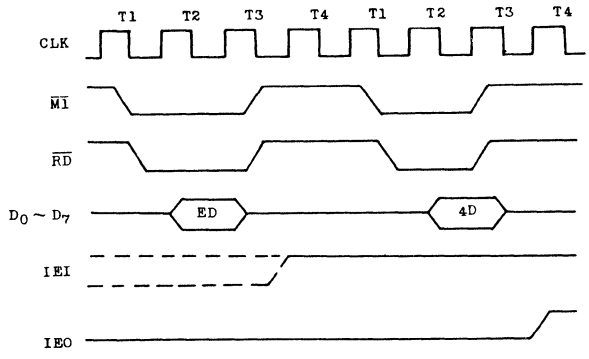


Fig. 3.9 Interruption Return Timing

3.5 Operating procedures

In order to operate the CTC in Counter Mode or Timer Mode, a channel control word and time constant data must be written into the CTC. To authorize any interruption by a channel control word, the interruption vector must be written into the CTC.

(1) Channel control word

To write a channel control word into the CTC, designate a channel by inputting a 2-bit code into the LSI terminal and the LSI terminal. Codes for respective channels are shown in Table 3.1.

Table 3.1 Channel Codes

		Input Terminal	
		CS1	CS0
Chan-	0	0	0
	1	0	0
	2	1	0
Chan-	3	1	1

The channel control word is written into the CTC is 8 bits. The system data bus D0 to D7 correspond to bit 0 - 7.
The meaning of each bit is outlined in Fig. 3.10. The function of each bit is shown in Table 3.2.

D7	D6	D5	D4	D3	D2	D1	D0
Inter-ruption	Counter timer	Pres-caler	Edge	Trigger	Time constant	Reset	1

Fig. 3.10 Channel Control Words

In case of the channel control word, D0 must always be 1 (D0=1).

Table 3.2 Meanings and Functions of Channel Control Words

Bit	Meaning and Functon	
	0	1
Bit 7 (D7)	Channel interruption is inhibited.	Authorizes channel interruption. In either counter mode or timer mode, this bit requests the interruption to MPU whenever the content of the downcounter becomes zero. If this bit is set at 1, the interruption vector must be written into the CTC before starting the downcounter. Further, if the channel control word with this bit set to 1 it is written into the CTC. The interruption is generated when the content of the downcounter becomes zero first after a new channel control word is written.
Bit 6 (D6)	A channel is mode in timer mode. System clock is input into the prescaler divided and output to the downcounter.	A channel is made in counter mode. The content of the downcounter is decremented by 1 (-1) at every edge of each trigger that is input into the CLK/TRG terminal. The prescaler is not used in counter mode.
Bit 7 (D7)	Used only in timer mode. The prescaler is set so as to divide the system clock into 1/16.	Used only in timer mode. The prescaler is set so as to divide the system clock into 1/256.
Bit 4 (d4)	In timer mode, the timer operation is started at the trailing edge of the trigger pulse (CLK/TRG). In counter mode, the content of the downcounter is decremented by one (-1) at the trailing edge of the external clock pulse (CLK/TRG).	In timer mode, the timer operation is started at the leading edge of the trigger pulse (CLK/TRG). In counter mode, the content of the downcounter is decremented by one (-1) at the trailing edge of the external clock pulse.
Bit 3 (D3)	Used only in timer mode. The timer operation is started at the leading edge of the trigger pulse clocks after a time constant is loaded onto the downtimer.	Used only in timer mode. The timer operation is started at the leading edge of the external trigger pulse that is input 2 system clocks after a time constant is loaded onto the downcounter. When a time lag between the system clock and trigger pulse satisfies a setup time, the prescaler starts to operate from the second leading edge of the trigger pulse. If a time flag between the system clock and trigger pulse does not satisfy the setup time. The prescaler

Bit	Meaning and Functon	
	0	1
Bit 3 (D3)		starts to operate at the leading edge of the trigger pulse after 3 system clocks. If the trigger pulse is inputted before leading of a time constant, the operation is the same as that when Bit 3 = 0.
Bit 2 (D2)	This bit (0) indicates that there is no time constant written after a channel con trol word. However, the chan-nel is in the reset state and this bit cannot be changed to "0" in the channel control word which is given first after the channel reset. To change other state without changing a time constant, input a channel control word with this bit changed to 0.	This bit (1) indicates that there is a time constant written immediately after a channel control word. If a time constant is written while the downcounter is operating, a new time constant is set in the time constant register. The counting which is in progress is carried out continuously and only after the content of the downcounter becomes zero, a new time constant is loaded onto the down-counter.
Bit 1 (D1)	The present channel operation is continued.	The downcounter operation is stop-ped. When this bit is set to 1, the channel operation is stopped but all bits in the channel control register remain unchanged. When Bit 2=1 and Bit 1=1, the chan-nel stops to operate until a new time constant is written. After a new time constant is programmed, the preparation for reopening the chan-nel is performed and the channel is reopened according to a value set for Bit 3. When Bit 2=0 and bit 1= 1, the channel operation is not started until a new channel control word is written.

(2) Time constant data

In timer mode or counter mode it is necessary to write time constant data into the time constant register.

When the channel control word Bit 2 (D2) is 1, time constants are written into the time constant register immediately after the channel control word is written. Time constant data are integers in the range from 1 to 256. When 8 bits of this data are all 0, it is regarded as 256.

The bit configuration of time constant data is shown in Fig. 3.11.

D7	D6	D5	D4	D3	D2	D1	D0
TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0

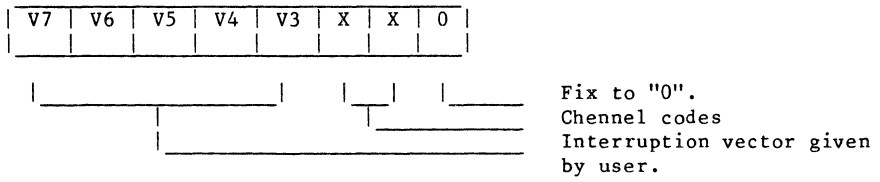
Fig. 3.11 Time Constant Data

(3) Interruption vector

In the interruption when MPU is in Mode 2, it is necessary for the channel requesting the interruption to give the interruption vector to MPU. The interruption vector is written into the interruption vector register for Channel 0 with Bit 0 (D)) set to 0. The write method is the same as that to write the channel control word into Channel 0. However, bit 0 (D0) must be always zero. Bit 7 (D7) to Bit 3 (D3) are values given by user. Bit 2 (D2) and Bit 1 (D1) are values given automatically by the CTC and a code of a channel with the highest priority among channels requesting the interruption is used. The channel codes are shown in Table 3.3 and the bit configuration of interruption vector in Fig. 3.12.

Table 3.3 Channel Codes

Bit 2 (D2)	Bit 1 (D1)	Channel No.	
0	0	0	^ High
0	1	1	Prior-
1	0	2	Low ity
1	1	3	v



Fi.g 3.12 Interruption Vector

3.6 Method of use

(1) Counter mode

A program when the interruption disabled is set using Channel 0 is explained.

(a) The programming step is shown in fig. 3.13.

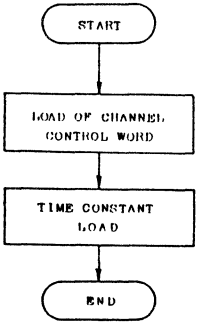


Fig. 3.13 Counter Programming Step

(b) The block diagram to change 100 KHz to 10 KHz is shown in Fig. 3.14.

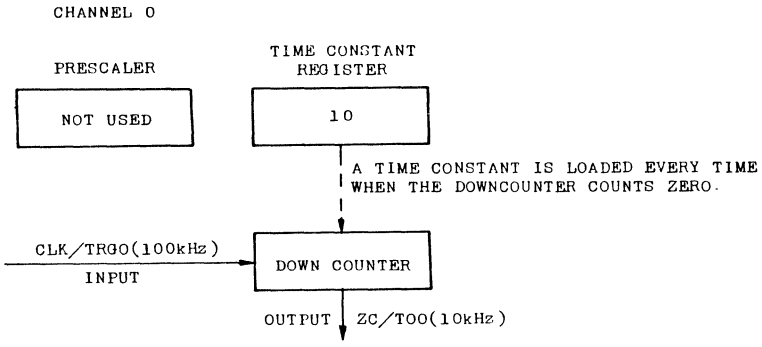


Fig. 3.14 Counter Block Diagram

(c) Channel control words are shown in Fig. 3.15.

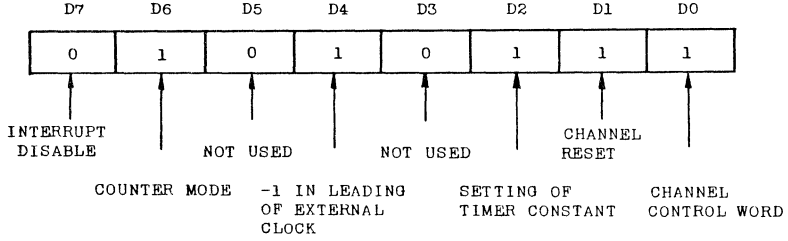


Fig. 3.15 Channel Control Words

(2) Timer mode

(a) A programming step when the interruption disabled is set using Channel 1 is shown in Fig. 3.26.

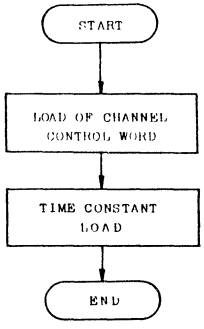


Fig. 3.16 Timer Programming Step

(b) The block diagram to change the system clock of 4 MHz to 1 KHz is shown in fig. 3.17.

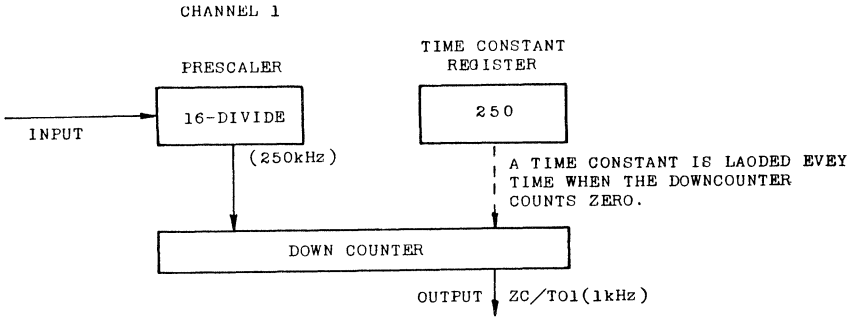


Fig. 3.17 Timer Block Diagram

(c) Channel control words are shown in Fig. 3.18.

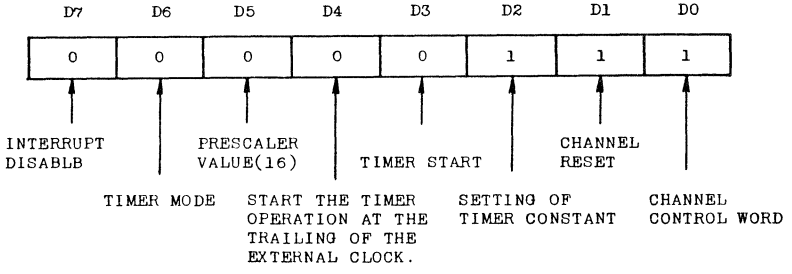


Fig. 3.18 Channel Control Words

4. ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
VCC	Supply Voltage	-0.5 to +7	V
VIN	Input Voltage	-0.5 to Vcc + 0.5	V
PD	Power Dissipation (TA=85°C)	250	mW
TSOLDER	Soldering Temperature (10 sec)	260	°C
TSTG	Storage Temperature	-65 to 150	°C
TOPR	Operating Temperature	-40 to 85	°C

4.2 DC ELECTRICAL CHARACTERISTICS

TA = -40°C to 85°C, VCC = 5V ± 10%, VSS = 0V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
VILC	Low Clock Input Voltage			-0.3	-	0.6	V
VIHC	High Clock Input Voltage			VCC-0.6	-	VCC+0.3	V
VIL	Low Input Voltage (Except CLK)			-0.5	-	0.8	V
VIH	High Input Voltage (Except CLK)			2.2	-	VCC	V
VOL	Output Low Voltage	IOL = 2.0mA		-	-	0.4	V
VOH1	Output High Voltage (I)	IOH = -1.6mA		2.4	-	-	V
VOH2	Output High Voltage (II)	IOH = -250uA		VCC-0.8	-	-	V
IL1	Input Leak Current	VSS ≦ VIN ≦ VCC		-	-	±10	uA
ILO	3-state Output Leakage Current in Float	VSS + 0.4 < VOUT ≦ VCC		-	-	±10	uA
ICC1	Power Supply Current	VCC=5V fCLK=(1) VIH=VIHC =VCC-0.2V VIL=VILC =0.2V	P/F	-	3	7	mA
			AP/AF	-	2	5	
			AP-6 /AF-6	-	4	7	
ICC2	Standly Supply Current	VCC=5VIL=0.2 VIH=VIHC=Vcc-0.2 V VIL=VILC=0.2V		-	0.5	10	uA
IOHD*	Darlington Drive Current,(2)	VOH=1.5V,REXT= 1.1K ohm.Applied to ZC/TO0-ZC/TO2		-1.5	-	-5.0	mA

Note (1) fCLK=1/tcC(MIN.)

(2) Applied to ZC/TO0, ZC/TO1 and ZC/TO2.

4.3 AC ELECTRICAL CHARACTERISTICS

TOPR = -40°C to 85°C, VCC = 5V ± 10%, VSS = 0V

NO.	SYMBOL	PARAMETER	4MHz P/AP/AF		6MHz AP-6/AF-6		UNIT
			MIN.	MAX.	MIN.	MAX.	
1	TcC	Clock cycle time	250	DC	165	DC	ns
2	TwCh	High clock pulse width	105	DC	65	DC	ns
3	TwCl	Low clock pulse width	105	DC	65	DC	ns
4	TfC	Clock falling time	-	30	-	20	ns
5	TrC	Clock rising time	-	30	-	20	ns
6	Th	Hold time	0	-	0	-	ns
7	TsCS(C)	$\overline{CS}$ set-up time for clock rise	160	-	100	-	ns
8	TsCE(C)	$\overline{CE}$ set-up time for clock fall	150	-	100	-	ns
9	TsIO(C)	Set-up time up to $\overline{IORQ}$ fall for clock rise	115	-	100	-	ns
10	TsRD(C)	Set-up time up to $\overline{RD}$ fall for clock rise	115	-	70	-	ns
11	TdC(DO)	Delay from clock rise to data output	-	200	-	130	ns
12	TdC(DOZ)	Delay from $\overline{IORQ}$, $\overline{RD}$ rise to data float	-	110	-	90	ns
13	TsDI(C)	Data input set-up time for clock rise	50	-	40	-	ns
14	TsMI(C)	$\overline{M1}$ set-up time for clock rise	90	-	70	-	ns
15	TdMI(IEO)	Delay from $\overline{M1}$ fall to IEO fall (in case of generating only interruption immediately before M1 cycle)	-	190	-	130	ns
16	TdIO(DOI)	Delay from $\overline{IORQ}$ fall to data output (INTA cycle)	-	160	-	110	ns
17	TdIEI(IDOf)	Delay from IEI fall to IEO fall	-	130	-	100	ns
18	TdIEI(IDOr)	Delay from IEI rise to IEO rise (after ED decode)	-	160	-	110	ns
19	TdC(INT)	Delay from clock rise to $\overline{INT}$ fall	-	(1)+ 140	-	(1)+ 120	ns

NO.	SYMBOL	PARAMETER	4MHz P/AP/AF MIN.	4MHz P/AP/AF MAX.	6MHz AP-6/AF-6 MIN.	6MHz AP-6/AF-6 MAX.	UNIT
20	TdCLK(INT)	Delay from CLK/TRG rise to INT fall (Counter mode)					
		tsCTR(C) Satisfied	-	(19)+(26)	-	(19)+(26)	ns
		tsCTR(C) not Satisfied	-	(1)+(19)+(26)	-	(1)+(19)(26)	ns
21	TcCTR	CLK/TRG Frequency	2x(1)	-	-	40	ns
21	TcCTR	(COUNT MODE)					
22	TcCTR	CLK/TRG rising time	-	50	-	40	ns
23	TfCTR	CLK/TRG falling time	-	50	-	40	ns
24	TwCTRl	Low CLK/TRG pulse width	200	-	120	-	ns
25	TwCTRh	High CLK/TRG pulse width	200	-	120	-	ns
26	TsCTR(Cs)	Set-up time up to CLK/TRG rise for clock rise requiring immediate count (counter mode)	210	-	150	-	ns
27	TsCTR(Ct)	Set-up time up to CLK/TRG rise for clock rise requiring immediate start of prescaler (timer mode)	210	-	150	-	ns
28	TdC(ZC/TOr)	Delay from clock rise to ZC/TO rise	-	190	-	140	ns
29	TdC(ZC/TOf)	Delay from clock fall to ZC/TO fall	-	190	-	140	ns

Note 1. AC test condition
VIH=2.4V, VIHC=VCC-0.6V, VIL=0.4V,
VOH=2.2V, VOL=0.8V CL=100pF

Note 2 If the daisy chain is at N stage,
2.5 TcC>(N-2)TdIEI(IEOf)+(TdMl(IEO)+TsIEI+TTL buffer delay must be satisfied.

Note 3 (1):Tcc, (19):Tdc(INT), (26):TsCTR(Cs)

4.4 Capacitance

TA = 25°C

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CCLOCK	Clock Input Capacitance	f=1MHz All terminals except that to be measured should be earthed.	-	-	5	pF
CIN	Input Capacitance		-	-	5	pF
COUT	Output Capacitance		-	-	10	pF

4.5 Timing diagram

Numbers shown in the following figures correspond with those in the 4.3 A.C. Electrical Characteristics Table.

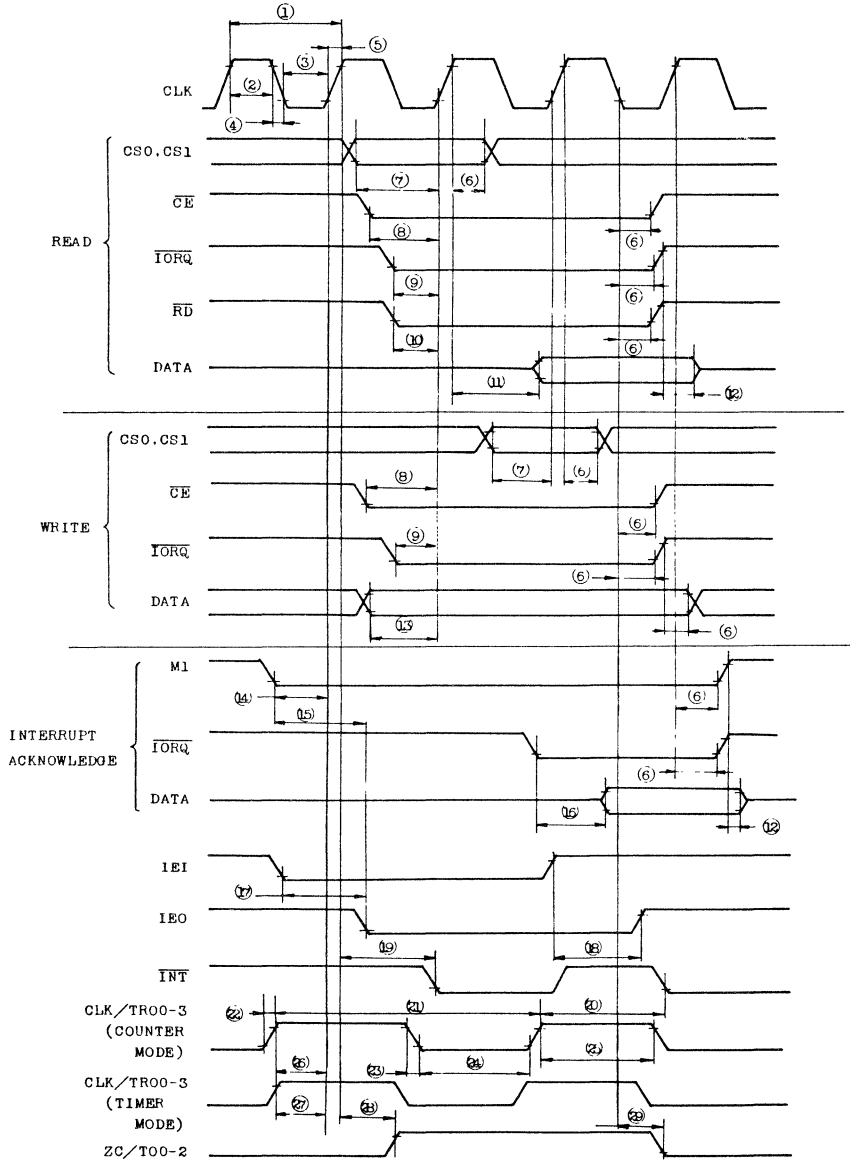
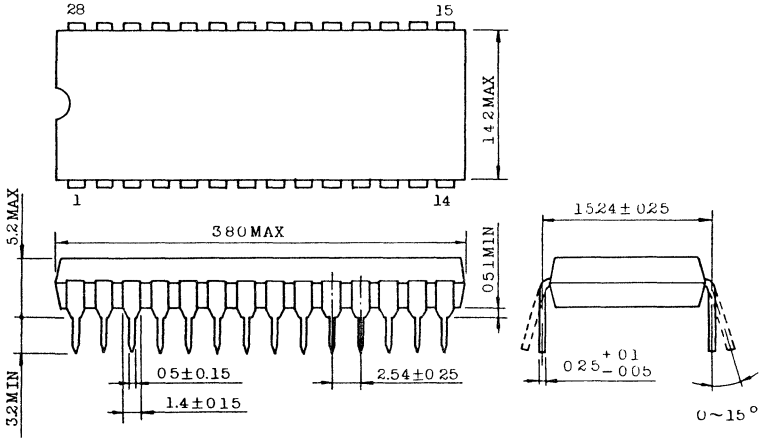


Fig. 4.1 Timing Diagram

5. Package Dimension

Unit in mm

5.1 DIP Package



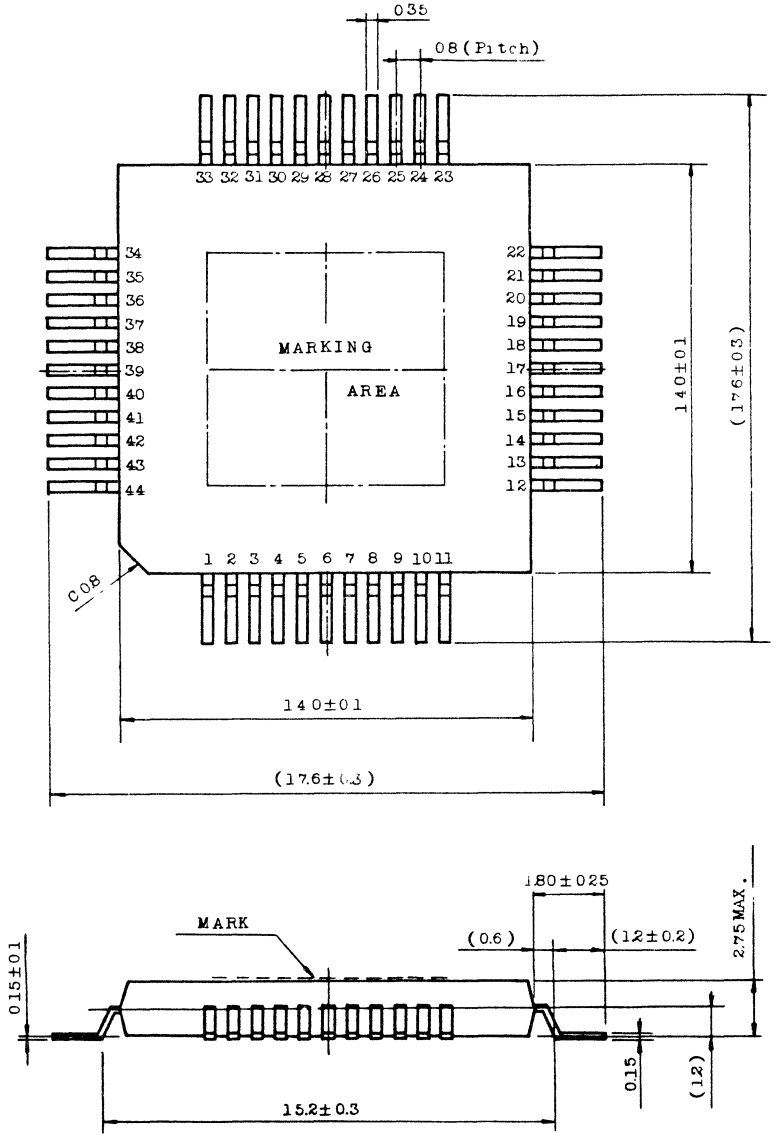
Note 1. This dimension is measured at the center of bending point of leads.

Note 2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoretical positions with respect to No.1 and No.28 leads.

Fig. 5.1 Package Dimension

Unit in mm

5.2 44-pin mini-flat package



TMPZ84C40P/41P/42P/43F TMPZ84C40AP/41AP/42AP/43AF TMPZ84C40AP-6/42AP-6/43AF-6
TLCS-Z80 SIO: SERIAL INPUT/OUTPUT CONTROLLER

1. General Description and Features

The TMPZ84C40(SIO/0), TMPZ84C41(SIO/1), TMPZ84C42(SIO/2) (hereinafter referred to as SIO) are CMOS version of Z80 SIO and have been designed to provide low power operation.
SIOs are designed for the adaptation to the various serial data communications which are needed to the microcomputer system.
SIOs are able to handle the asynchronous signal, the synchronous byte unit protocol and the synchronous bit unit protocol like HDLC and SDLC.
SIOs are fabricated using Toshiba's CMOS Silicon Gate Technology.

The principal functions and features of the SIOs are as follows.

(1) Compatible with the Zilog Z80 SIO.
(2) Compatible with the CCITT-X.25.
(3) Compatible with the HDLC/SDLC.
(4) Data transfer rate up to 800K bit/Sec
(5) 2 independent full-duplex channels can be used.
(6) Built-in CRC generation and checking function.
(7) On chip daisy-chain structure interrupt circuit.
(8) Low power consumption
mA Typ. (@5V @4MHz) ... TMPZ84C40/41/42P, TMPZ84C43F
2.5mA Typ. (@5V @4MHz) ... TMPZ84C40/41/42AP, TMPZ84C43AF
4 mA Typ. (@5V @4MHz) ... TMPZ84C40/41/42AP-6, TMPZ84C43AF-6
(9) Single power supply: 5V $\pm$ 10%
(10) Extended operating temperature: -40°C to 85°C
(11) 40 pin DIP package, 44 pin Mini Flat package.

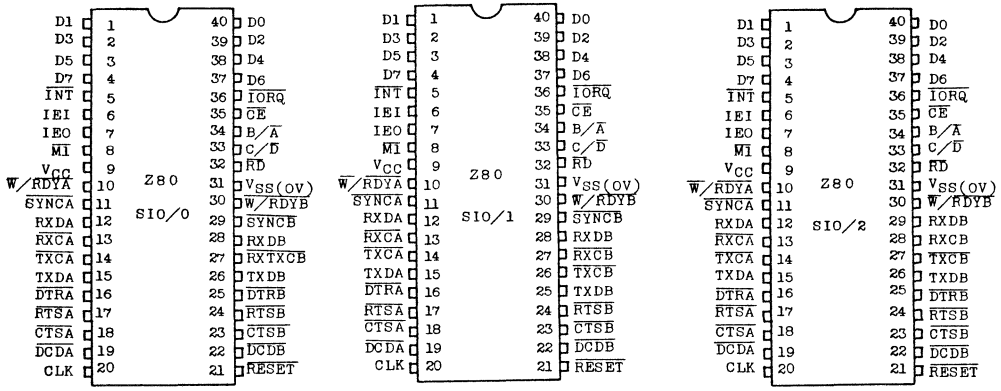
(Note) Z80(R) is a registered trademark of Zilog Inc., U.S.A.

2. Pin Connections and Pin Functions

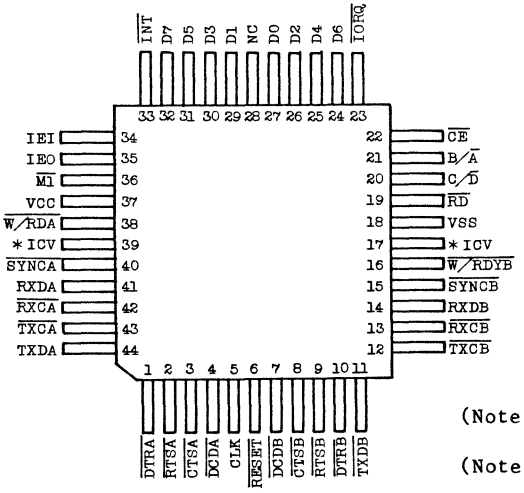
The pin connections, pin functions and functions of SIOs are described in this chapter.

2.1 Pin connections

The pin connections of the SIOs are as shown in Fig. 2.1.



(TMPZ84C40) (TMPZ84C41) (TMPZ84C42)



(Note 1) NC must be used at open condition.

(Note 2) *ICV must be used at open condition or connected with VCC.

(TMPZ84C43)

Fig. 2.1 Pin Connections (Top View)

However, it is necessary to choose the terminals in accordance with the purposes, because they are limited in number. The differences in SIO/0, SIO/1 and SIO/2 are shown in Fig. 2.2(a) SIOs version diagram.

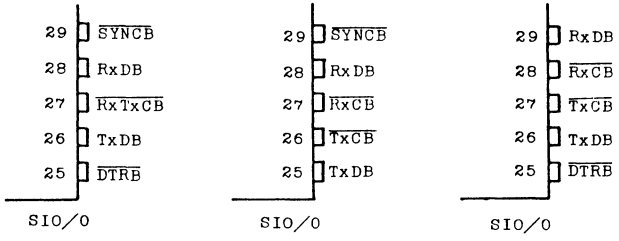


Fig. 2.2(a) SIOs Version (40-pin DIP)

2.2 How to use TMPZ84C43 as SIO/0 or SIO/1 SIO/2.
The Figure 2.2(b) shows six terminals to define TMPZ84C43 as SIO/0 or SIO/1 or SIO/2.

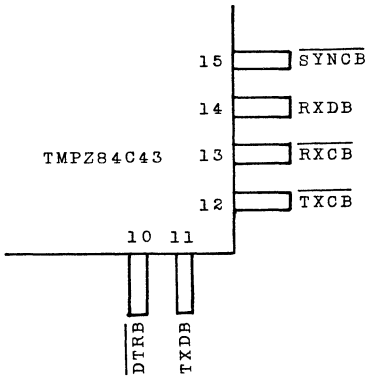


Fig. 2.2(b) Pinout of TMPZ84C43 "B" Channel

The following table shows five terminals (No.25 through 29) of SIO in 40-pin DIP corresponding to these of TMPZ84C43.

Table 2.1 SIOs Version by TMPZ84C43

Terminal No. of SIO in 40 pin DIP	TMPZ84C43 as SIO/0			as SIO/1			as SIO/2		
	A1	B	C	A2	B	C	A3	B	C
25	$\overline{\text{DTRB}}$	10	Output	TxDB	11	Output	$\overline{\text{DTRB}}$	10	Output
26	TxDB	11	Output	$\overline{\text{TxCB}}$	12	Input	TxDB	11	Output
27	$\overline{\text{RxTxCB}}$	* Note 1	Input	$\overline{\text{RxCB}}$	13	Input	$\overline{\text{TxCB}}$	12	Input
28	RxDB	14	Input	RxDB	14	Input	$\overline{\text{RxCB}}$	13	Input
29	$\overline{\text{SYNCB}}$	15	** Note 2	$\overline{\text{SYNCB}}$	15	** Note 2	RxDB	14	Input
				(Note) DTRB (terminal number 10) will not be used. The terminal may be open.			(Note) $\overline{\text{SYNCB}}$ (terminal number 15) will not be used. The terminal is pulled-up internally, so it may be open.		

A1: Signal Name of SIO/0 A2: Signal Name of SIO/1 A3: Signal Name of SIO/2
B: Terminal No. of TMPZ84C43 C: In/out

*Note 1) The terminal No.12 ($\overline{\text{TxCB}}$) and No.13 ($\overline{\text{RxCB}}$) must be connected externally when TMPZ84C43 will be used as SIO/0.

**Note 2) Bi-directional

2.2 Pin Names and Functions

Table 2.2 Pin Names and Functions

Pin Name	Number of Pin	Input/Output 3-state	Function
D0 - D7	8	I/O 3-state	8-bit bidirectional data bus.
$\overline{INT}$	1	Output	Interrupt request signal. This is used, in case SIOs request MPU the interrupt. Wired OR connection is possible (becuase of the open drain).
IEI	1	Input	Interrupt enable input signal.
IEO	1	Output	Interrupt enable output signal. IEI and IEO are used for the daisy-chain structure. When IEI terminal is "1" and IEO terminal is "0" the SIO is being serviced by a MPU interrupt service routine.
$\overline{M1}$	1	Input	Machine cycle 1. When the both of M1 and IORQ are "0", the SIO is requesting the interrupt.
$\overline{W/RDYA}$ $\overline{W/RDYB}$	2	Output	Wait/ready signal A, wait/ready signal B. These can be used as wait signal or ready signal according to SIOs-programming. SIO becomes active on "0", when pins are programmed as "WAIT" and are not ready to receive the data for MPU. SIO become active on "0", when pins are programmed as "READY" and ready to receive the data character for DMA.
$\overline{SYNCA}$ *$\overline{SYNCB}$	*2	I/O	Synchronous signal. In case of the asynchronous receive mode, These pins become the same input terminals as CTS and DCD. In case of the external synchronous mode, pins become the input terminals and in case of the internal synchronous mode, become the output terminals.
RxDA RxDB	2	Input	Serial receive data
$\overline{RxCA}$ *$\overline{RxCB}$	*2	Input	Receive clock signal. In asynchronous mode, pins can choose the receive clocks which are 1, 16, 32 and 64 times as large as the data transfer rate according to the program.
TxDA TxDB	2	Output	Serial transmit data
$\overline{DTRA}$ *$\overline{DTRB}$	2	Output	Data terminal ready signal. These pins output the possibility or impossibility of the serial data receive.

Pin Name	Number of Pin	Input/Output 3-state	Function
$\overline{RTSA}$ $\overline{RTSB}$	2	Output	Transmit request signal. In serial data transmit, become "0".
$\overline{CTSA}$ $\overline{CTSB}$	2	Output	Transmittable signal. When terminals are "0", SIOs can receive the serial data transmit of the modem which has sent these signals.
DCDA	2	Input	Data carrier detect signal. When terminals are "0", SIOs can enable the serial data transmit.
CLK	1	Input	Single-phase clock input. Inputs Z80 standard system clock of single-phase. When CLK terminal is DC state ("1" or "0"), SIOs are in stationary sate.
$\overline{IORQ}$	1	Input	I/O request signal In case both of $\overline{IORQ}$ and $\overline{CE}$ are "0", the data or command are transferred between MPU and SIO by the combination of B/$\overline{A}$ and C/$\overline{D}$.
$\overline{CE}$	1	Input	Chip enable signal When input becomes "0", SIOs are enabled.
B/$\overline{A}$	1	Input	Channel select signal Selects the channel (A/B).
C/$\overline{D}$	1	Input	Command/data select signal Selects the command and data.
$\overline{RD}$	1	Input	Read signal. In case both of $\overline{CE}$ and $\overline{IORQ}$ are "0", if RD is "0", this pin performs the read operation and if $\overline{RD}$ is "1", this pin performs the write operation.
$\overline{RESET}$	1	Input	Reset signal. If RESET is turned into "0", the receiver and transmitter become disabled and the serial data become the mark state.
*$\overline{RxTxCB}$	*1	Input	Bonding terminal of $\overline{TxCB}$ and $\overline{RxCB}$.
Vcc	1	Power Supply	+5V
Vss	1	Power Supply	0V

The asterisk (*) mark is difference in accordance with the three versions (SIO/0, SIO/1, SIO/2).

3. Functional Description

3.1 Block diagram

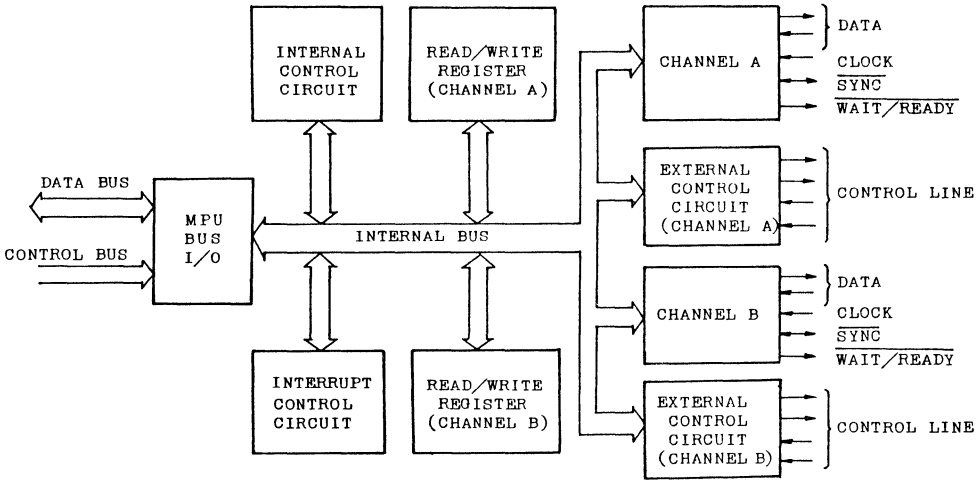


Fig. 3.1 Block Diagram

3.2 System configuration

3.2.1 Architecture

As shown in Fig 3.1, the SIO is composed of MPU bus interface, the internal control circuit, the interrupt control circuit and two full-duplex channels which operate independently. Each channel has the read register, the write register and the external control circuit which is conneced to the peripheral LSI or the external device.

Table 3.1 shows the registers in the SIO and their functions. Each channel has eight write registers and three read registers. Refer to 3.4 SIO programming for details.

(1) Communication data path

Fig. 3.2 shows the communication path of the transmit/receive data of each channel.

1] Receiving

The receiver has 8-bit receive shift register and 3-stage 8-bit buffer register in FIFO configuration. Therefore, it is possible to get the sufficient time at the high speed data block transfer. Moreover, the receiver has the receive error FIFO for the purpose of holding the parity error, the framing error and the other status information.

The receive data take the different paths according to the oepration mode and the character length as shown in Fig. 3.2.

Table 3.1 (a) Write Register

Register	Function
Write register 0(WR0)	CRC reset. This is used for the setting of the register-pointer and command.
Write register 1(WR1)	This is used for the setting of the interruption mode.
Write register 2(WR2)	Register for the setting of the vector which is sent out at interruption (Channel B only)
Write register 3(WR3)	Register having the parameter for the control of receiver
Write register 4(WR4)	Register having the parameter for the control of receiver and transmitter
Write register 5(WR5)	Register controlling the transmitter
Write register 6(WR6)	Register for the setting of the synchronous character and the address field of SDLC
Write register 7(WR7)	Register for the setting of the synchronous and the flag of SDLC

(a) Write Register

Register	Function
Write register 0(WR0)	Indicates the state of transmit/receive and the state of terminals.
Write register 1(WR1)	Indicates the error status and terminals number code.
Write register 2(WR2)	Indicates the content of the interruption vector. (Channel B only)

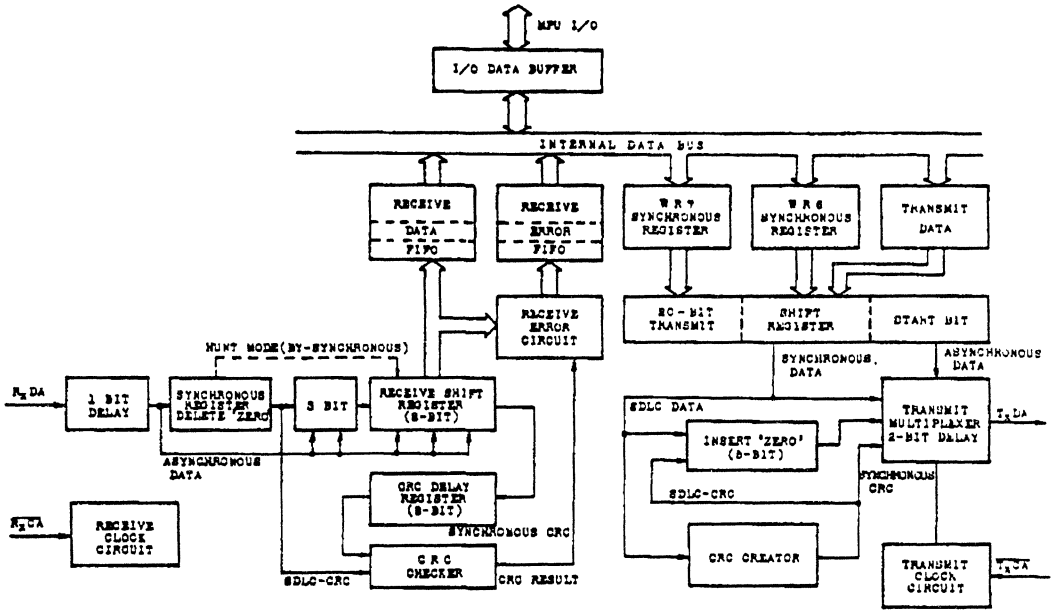


Fig. 3.2 Transmit/Receive Data Path (Channel)

- Asynchronous mode
  In the asynchronous mode, when the character length is 7 or 8 bit, the receive data enter into 3-bit buffer and when it is 5 or 6 bit, data enter into 8-bit receive shift régister jumping 3-bit buffer.

- Synchronous mode
  In the synchronous mode, the data path changes according to the then receive processing steps. The receive operaiton begins at the hunt phase. In this mode, the receiver seeks the bit pattern which coincides with the synchronous charcter which has been programmed within the receive data. When SIO is programmed in the mono-synchronous mode, the receiver seeks the bit pattern which coincides with the synchronous character which is set in WR 7. And when SIO is programmed in the bi-synchronous mode, the receiver seeks the bit pattern which coincides with the two successive synchronous characters which are set in WR 6 and WR7.
  When the synchronization is once settled, the subsequent data do not pass the synchronous register and so enter into 3-bit buffer.

- SDLC mode
  In SDLC mode, the synchronous register always monitors the receive data and the zero elimination is carried out if necessary.
  When the synchronous register detects the successive five "1" within the receive data and the next bit is "0", this register eliminates the "0". Moreover, if the next bit is "1", this register monitors the second next bit.

If this bit is "0", it must be recognized as the flag and if it is "1", it must be recognized as the abort sequence (the successive seven "1"). The reformatting data enter into the receive shift register through 3-bit buffer. When the synchronization is once settled, the subsequent data take the same path regardless of the character length.

2] Transmitting

The transmitter has 8-bit transmit data register and 20-bit transmit shift register. 20-bit transmit shift register reads the data from WR 6, WR 7 and the transmit data register.

o Asynchronous mode

In the asynchronous mode, the data in 20-bit transmit shift register are sent to the transmit multiplexer with the start bit and the stop bit.

o Synchronous mode

In the synchronous mode, WR 6 and WR 7 hold the synchronous character. Furthermore, these contents are sent into 20-bit transmit register as the synchronous character at the time of the data block transmit. If the transmitter underrun state occurs during the trasnsmission of the data block, the contents sent into 20-bit transmit register as the idle synchronous character.

o SDLC mode

In SDLC mode, WR 6 holds the station address and WR 7 holds the flag. The flag (WR 7) is sent into 20-bit transmit shift register at the beginning and end of the frame. With regard to all other field in the data, one "0" is inserted after the successive five "1".

(2) I/O function

When the transmit/receive of the informations are carried out with MPU, one of the polling mode, interrupt mode or block transfer mode is chosen as SIO mode.

o Polling

In order to operate SIO in the form of polling mode, every interrupt modes must be inhibited. In this mode, MPU reads the status bit D0 and D2 within each channel RR 0 and so checks the possibility of transmit/receive.

o Interrupt

SIO interrupts are composed of the transmit interrupt, receive interrupt and external/status interrupt. Enabling and disabling the interrupt are executed by using the program. The receive interruption is further divided into the following three modes.

- o Interrupt in the first receive character
- o Interrupt in the full receive character
- o Interrupt in the special receive condition

The priority order of the interrupt of the channel A is higher than that of the channel B. The order in the same channel is the receive-, transmit- and external/status interrupt.

The SIO has as well as the other peripheral LSI the daisy-chain sturcture interruption priority order control function and the interrupton vector generation function. Furthermore, SIOs have "Status affect vector" function. This status affect vector is the function which can output the four kinds of vectors according to the interruption factors.

o Block transfer
SIOs have the block transfer mode and so can adapt the mode to MPU block transfer and DMA controller.
W/RDY line is used for the block transfer. This line is used as WAIT line for MPU block transfer and is used as READY line for DMA block transfer. The ready output of SIOs can transmit the data to DMA controller. Further, the wait output of SIOs can not ready to transmit the data and so request the delay of the output cycle.

3.2.2 Operation

(1) Asynchronous mode
In asynchronous mode, in order to transmit/receive of data, it is necessary to program the character length, clock rate, interruption mode, etc. All these parameters are written into the write register, but only WR 4 should be programmed prior to other registers.
In data transmit, it is not started until transmit enable bit has been set, but when auto-enable bit is set, SIOs start to transmit immediately after CTS terminal has become "0", so a programmer can transmit messages to SIO, needless to wait for CTS.
The data format of the asynchronous mode is shown in fig. 3.3.

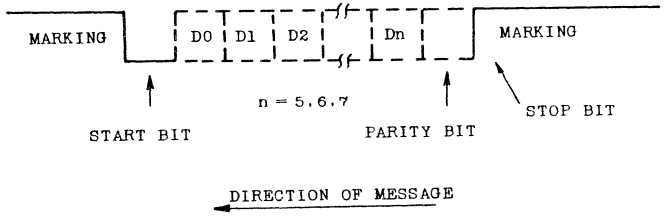


Fig. 3.3 Data Format of Asynchronous Mode

1] Transmitting
Serial data are output from TxD terminal, whereby the transmitting clock rate can be programmed at any of 1, 1/16, 1/32 or 1/64 of the clock rate furnished to transmit clock input (TxC). In addition, these data are output at leading edge of TxC.

2] Receiving
Receiving operation of asynchronous mode starts when receiving enable bit (D0 of WR 3) is set. When receiving data input RxD is set at "0" for at least 1/2 bit time, SIOs take it a start bit and sample out the input data at the middle of bit time. In addition, the sampling is carried out at the trailing edge of Rxc.

When a receiver receives the data of the other character length than 8 bit, it converts them into such data as composed with necessary bit, parity bit, and by making free bit as "1".

(Example) The case of 6-bit character |1|P|D5|D4|D3|D2|D1|D0|

When external/status interruption is enabled, if it detects break state during receiving data, it generates interrupt, and then break/abort status bit (D7 of RR 0) is set, while SIOs wait the release of break state, monitoring the transmit data. Further, when no-active state of DCD terminal lasts longer than the time of a specified pulse width, interrupt is generated and DCD status bit is set at "1".
In the polling mode, MPU must read out the data, detecting significant bit (D0 of RR 0) of receiving character. This bit is automatically reset, whenever it reads out a receiving buffer. In this mode, caution is requested to prevent double writing, by checking the status of transmit buffer prior to writing into a transmitter.

(2) Synchronous mode

In the synchronous mode, though there are three kinds of character synchronization which are monosynchronization, bisynchronization and external synchronization, the clock of xl is used both for transmit/receive. Receiving data is sampled at the trailing edge of receive clock input (RxC), while tranmsitting data varies at the leading edge of transmit clock input.
The data format of synchronous mode is shown in Fig. 3.4

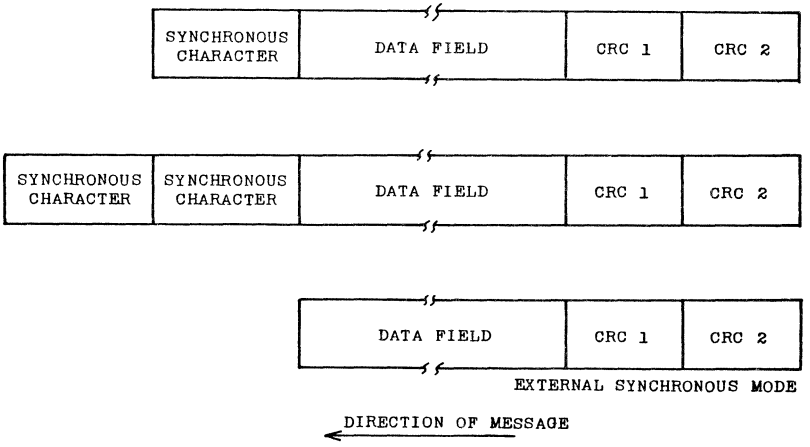


Fig. 3.4 Data Format of Synchronous Mode

1] Monosynchronous

In this mode, when coincidence with synchronous character (8 bit) programmed in WR 7 is realized, synchronization is generated, thereby the data transmit becomes possible.

2] Bisynchronous
In this mode, when coincidence with two successive synchronous characters programmed in WR 6 and WR 7 is attained, the synchronization is generated, thereby data transmit becomes possible. Further, in these mono- and bi-synchronous modes, SYNC becomes active during the receive clock which detects the synchronous character.

3] External synchronous
In this mode, the synchronization is carried out externally. When the synchronization is attained, it is informed by SYNC terminal. In addition, SYNC input should be kept at "0", until the character synchronization is released. The character configuration begins at RxC rising after SYNC falling.
After resetting, SIO enter into the hunt phase, searching the synchronous character. If the synchronization becomes incomplete, it is possible to enter again into the hunt phase by set the enter-hunt phase bit (D4 of WR 3) at "1".

o Transmitting

a. Data transfer using interruption
If transmit interrupt is enabled, interrupt is carried out when the transmit buffer becomes empty. As for the interruption procedure, the other data are written in the transmitter. In such case, the transmit underrun state occure if the data is not yet prepared by some reason.

b. Bi-synchronous transmitting
In the bisynchronous mode, if data run out in a transmitter during the transmitting, replacing character is to be sent in order to keep the synchronization. There are two ways for that; one is to insert a synchronous character, and another is to feed CRC characters which are till then generated, and then to feed the synchronous character. The selection of the way is controlled by reset transmit underrun/EOM command in WR 0.

c. End of transmission
Break is carried out by setting D4 of WR 5. At this time, a in both the transmit buffer and the shift register will go out.
When external/status interruption is enabled, SIO generates interrupt and transmit vector according to the state of the transmitter.
This mode can be used for the block transfer.

o Receiving

a. Interrupt on first received character
This mode is usually used for the block transfer. In addition, in this mode, SIO generates interrupt only for the first character, but thereafter do not generate interrupt except under the special receive conditions.
For the purpose of the initialization, it is required to set command 4 of WR 0 (enable at next receive interrupt).

b. Interrupt on all received character
In this mode, interrupt is generated for all characters entering into receive buffer. When status affect vector is set, special vector is generated by special receive condition.

c. Special receiving conditional interrupt
This interrupt can be generated regardless of the selection of the above two ways of interrupt. Although as for the special receive conditions, there are parity error, receive overrun error, framing error, and end of frame (SDLC), the reset is necessary after read out, since these error status bits are latched.
These error status bits can be reset by the command 6 of the WR0.

(3) SDLC mode
Though SIO can use both protocols of SDLC and HDLC, since both are very much similar, here explanation is made only for SDLC mode.
Fig. 3.5 shows the data format of SDLC mode.
In SDLC mode, one data block is called "frame", and these messages are held between two flags, called open flag and close flag. Address field includes the address of secondary station, and SIO receive or disregard this frame according to the address.

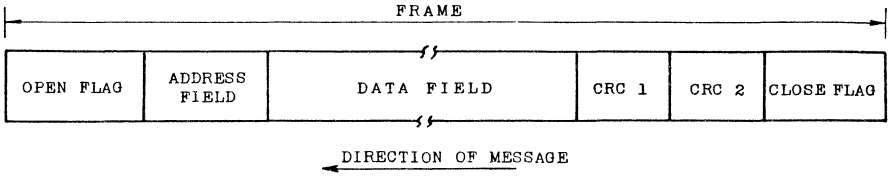


Fig. 3.5 Data Format of SDLC Mode

o Transmitting
a. Data transfer using interrupt
If transmit interrupt is set, whenever transmit buffer becomes empty, interrupt is generated. In SDLC mode, data are transferred to SIOs, by the use of this interrupt.
b. Data transfer using wait/ready
In wait/ready function, WAIT is for lengthening the output cycle of MPU when SIO transfer buffer is not empty, while READY notifies DMA that SIO transfer buffer is empty and so ready for receiving data.
If data is written in transfer shift register prior to the transmitting, SIO enter into the underrun state.
Using this function, it is possible to transmit data to SIOs.
c. Transmitting underrun/EOM
SIO, when there is no data to be transmitted in transfer data buffer, automatically terminate SDLC frame. In order to carry out this, after data run out, SIO at first transmit CRC of 2-byte and then transmit one or more flags.
After resetting, status bits of transmit underrun/EOM are set and prevent CRC character from inserting when transfer data run out.
Using this operation, the frame transmission is started. At this time, transmit underrun/ EOM reset command must be set between the time of transmit of the first data and the end of data.
By doing this, reset state is generated at the end of message, so CRC characters are automatically transmitted.

d. CRC generation
When CRC calculation is carried out, CRC generator must have been reset (D6 and D7 of WR 0) piror to the start of transmit. Calculation of CRC is started at the time (WR 6) when address field is written into SIOs.
Further, transmit CRC enable bit (D0 of WR 5) must be set prior to address field writing.

e. End of transmit
While transmitting, if the transmitter is made to be disabled, though the data under transmitting at that time are transmitted without any change, the transmitter enters into the marking state thereafter.
Even if a transmitter is disabled, characters in the buffer remain, but when abort command is written in command register, abort sequence becomes significant and then all data go away.

o Receiving
In receiving mode, the initial setting of several parameters is necessary. Address field is written in WR 6, and flag character in WR 7.
When a receiver receives open flag, it compares the content of address field following the flag with the address set in WR6 and global address ("1111 1111). If address field in frame coincides with either one of the above two, SlOs start receive.

a. Interrupt on first received character
This mode is used for the block transfer, which usually uses WAIT/READY function. In this mode, SIOs generate interruption only to the first character.
Further, since status flag of this interruption is latched, it is necessary to set command 4 (enable at next receiving character) of WR 0 beforehand, in order to initialize again.
When external/status interruption is set, interruption is generated at every change of DCD. In addition, interruption is generated under special receive conditions.

b. Interrupt on all received character
In this mode, SIO generate interrupt to all characters received. In additioon, when status affect vector has been set, special vector is generated to interruption under special receive conditions.

c. Special receive condition interrupt
When special receive conditions are used, it is necessary to select beforehand either of interrupt by first received character or interrupt by all received characters. Among interrupt under special receive conditions, status of receive overrun is latched. Reset of status bit is carried out by error reset command (command of WR 0).

d. CRC check
The CRC checker is reset when it receives the leading open flag of frame, and carries out CRC calculation of the following characters, continuing to close flag.
In SDLC mode, as transmitting CRC is inverted, special check sequence is used. Check must be ended with "0001 1101 0000 1111".
Since SIO processes CRC characters as data, MPU must discard them after reading.

e. End of receive
When SIO receives close flag, end of frame bit is set and this fact indicates that the close flag has been received. Further, if the status affect vector is set at this time, interrupt under special receiving conditions is generated and the vector is transmitted. At any frame, abort can be carried out by abort transmit. Further, if external/status interrupt has been set at this time, interrupt is generated and break/abort bit in RR0 is set.

3.3 Status flowchart and basic timing

3.3.1 Status flowchart

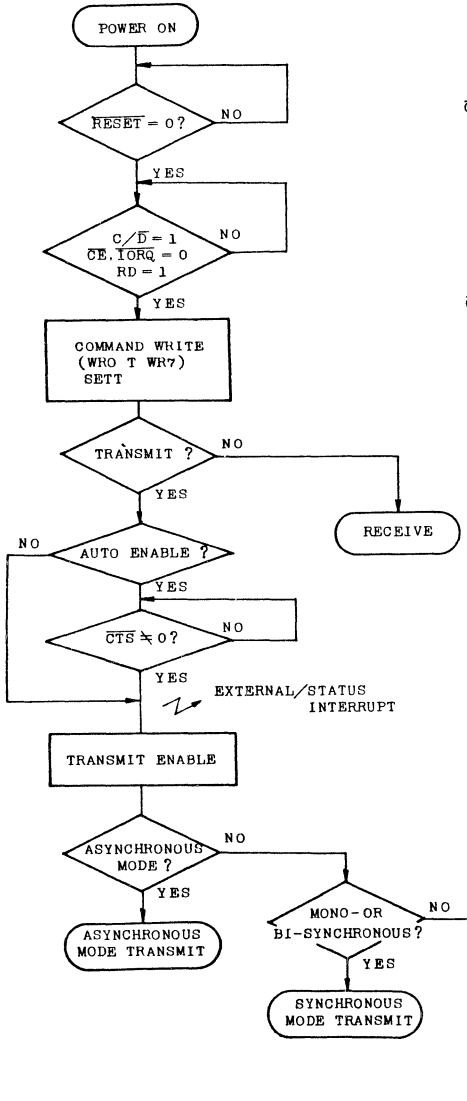


Fig. 3.6 (a) Status Flowchart

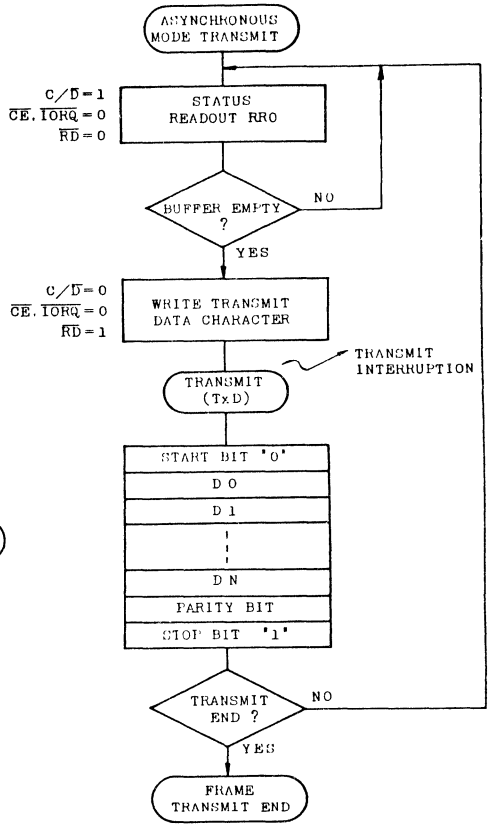


Fig. 3.6 (b) Status Flowchart

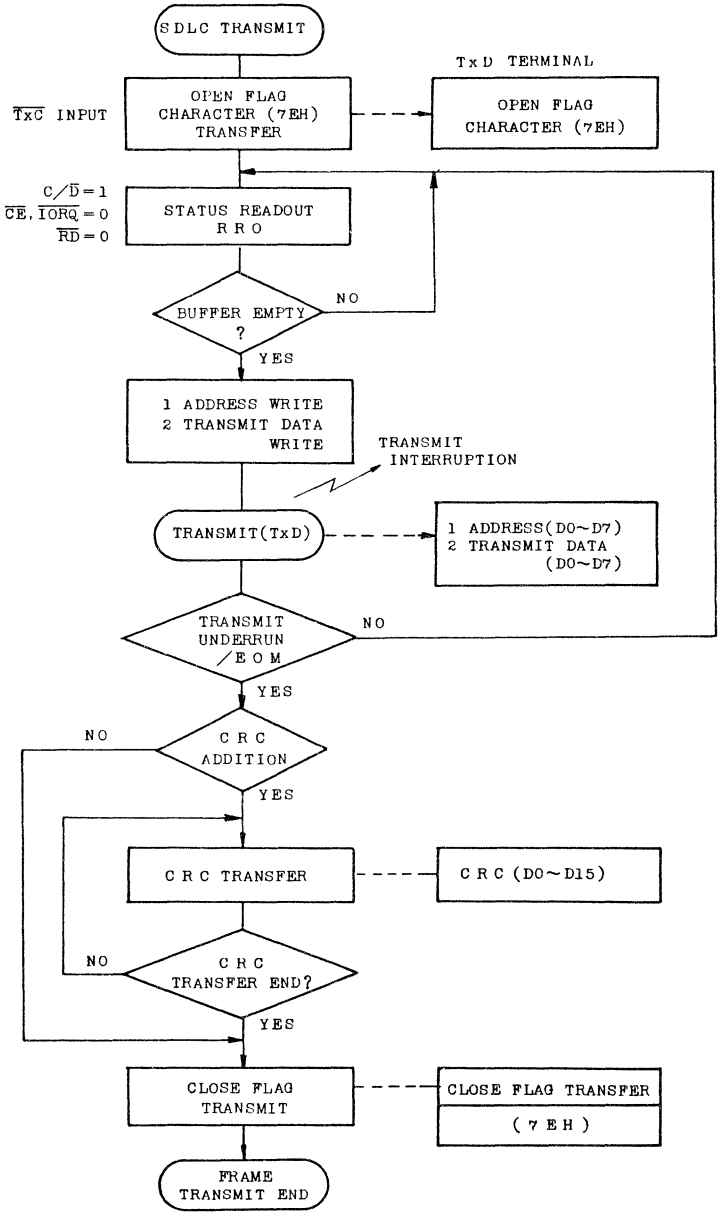


Fig. 3.6 (c) Status Change Flowchart

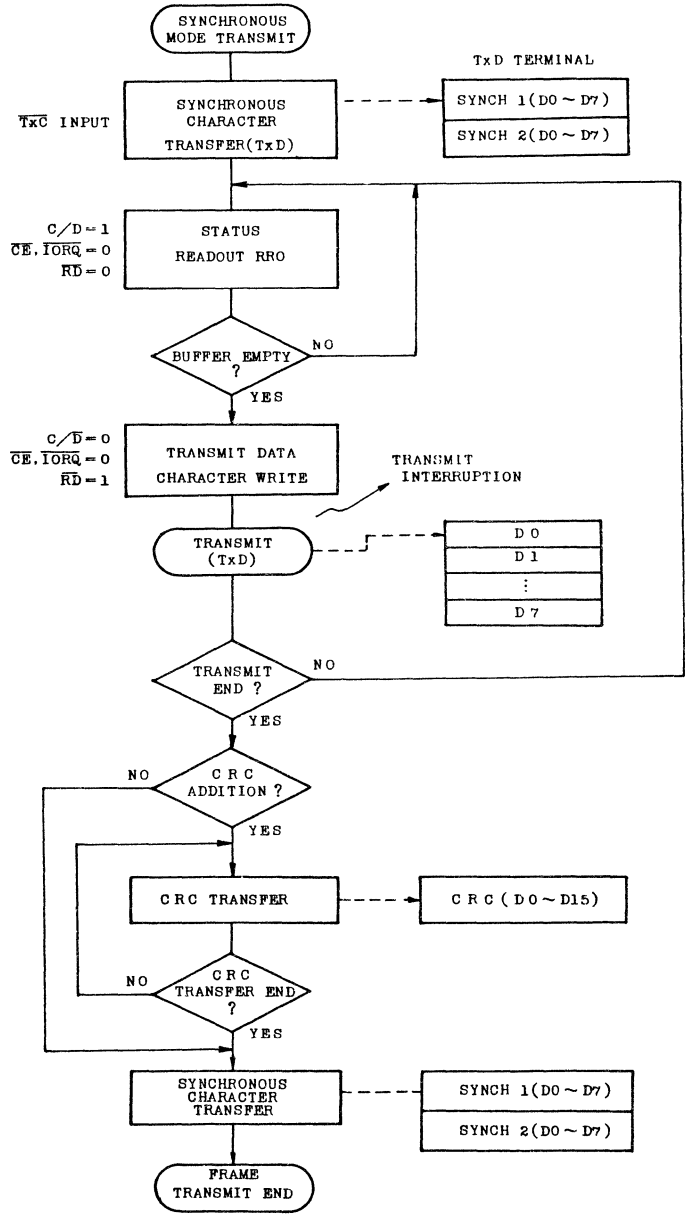


Fig. 3.6 (d) Status Change Flowchart

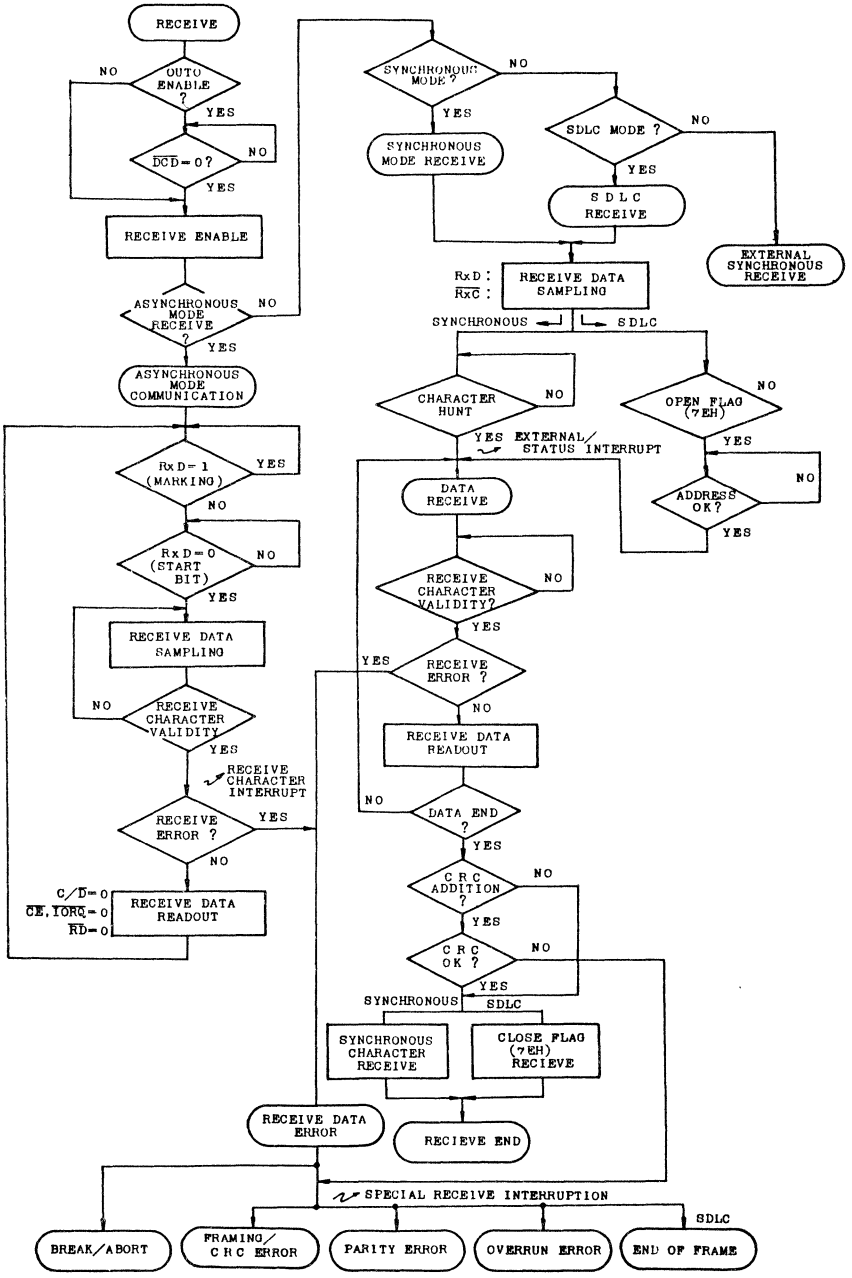


Fig. 3.6 (e) Status Flowchart

3.3.2 Basic timing

Fig. 3.7 is the timing diagram when data or command are written into SIO from MPU.
Fig. 3.8 is the timing diagram when MPU reads data from SIO.
Fig. 3.9 shows that when MPU accepts an interrupt request of SIO, as the acknowledge signal, IORQ terminal is made "0" within a couple of clocks after M1 terminal is made "0".
In order to hold the state under interruption service at daisy-chain, the state of interruption request cannot be changed as long as M1 remains active.
Figure 3.10 is the timing diagram of returning from interruption.
Figure 3.11 shows the state of daisy-chain.
At first, the period during interruption service of SIO is considered.
After M1 becomes active, by interruption request of PIO immediately before the deconding of "EDH" in the first byte of RETI instruction, "IEO" of PIO becomes "0". However, interruption request of PIO is not acknowledged, because "EDH" is decoded. Therefore, "IEO" of PIO returns to "1".
By decoding "4DH" at the 2nd byte, "IEO" of SIO returns to "1". Therefore, "IEI" and "IEO" of peripheral LSI at this time become "1", and so they enter into the state under no interruption service. PIO keeps INT terminal at "0" until this state is realized. Under this state, interruption starts from the peripheral LSI of higher interruption priority order.

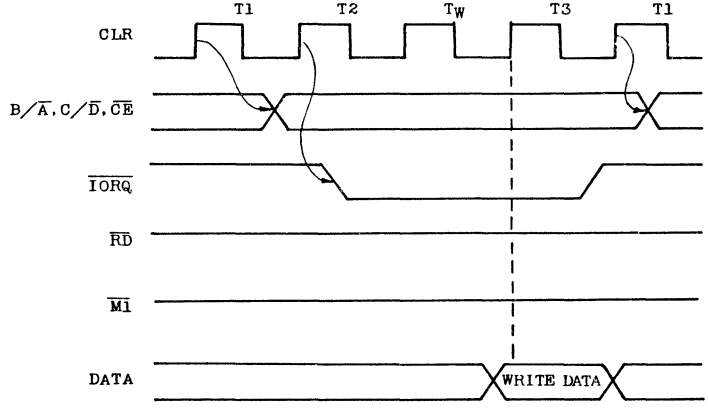


Fig. 3.7 Data Write Cycle from MPU to SIO

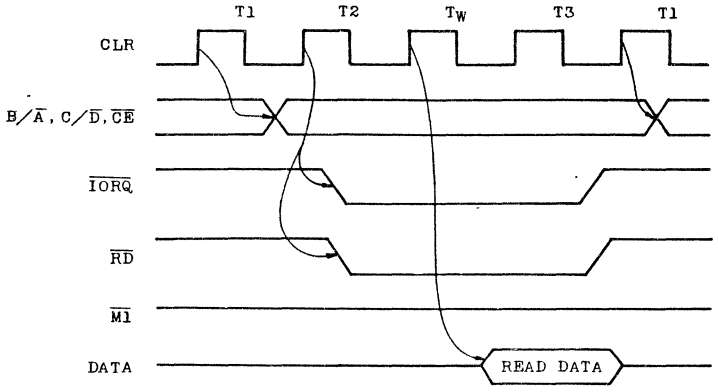


Fig. 3.8 Data Readout Cycle from MPU to SIO

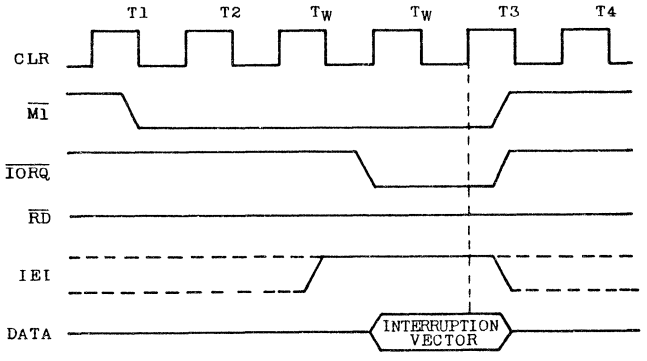


Fig. 3.9 Interrupt Acknowledge Cycle

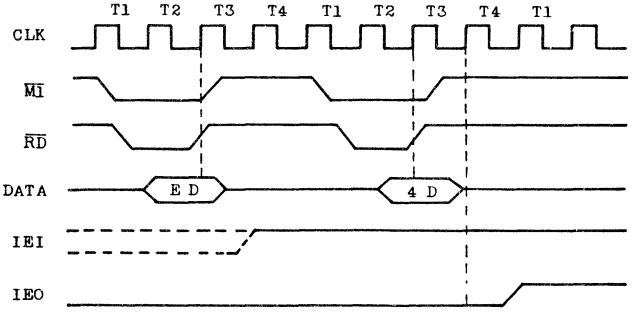
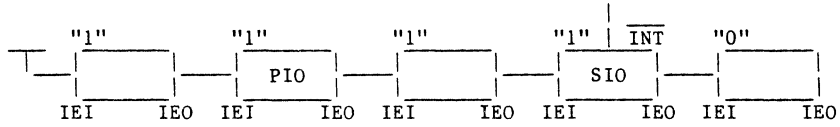
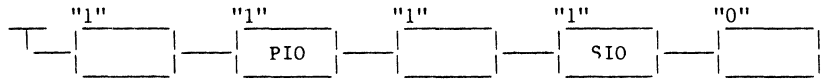


Fig. 3.10 Return Cycle from Interruption

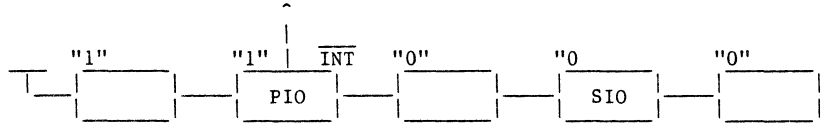
[1] Status where SIOs request interruption



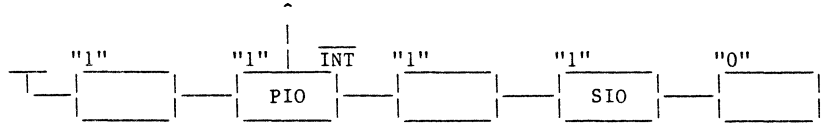
[2] SIOs are under interruption service



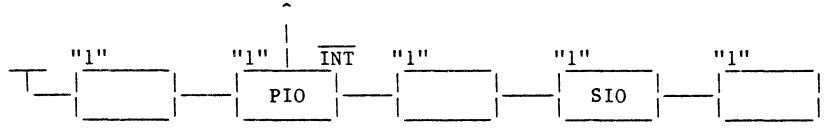
[3] Status where PIO has requested interruption immediately before SIOs decode "ED".
By the request of PIO for interruption IEO of PIO becomes "0".



[4] As "EDH" has been decoded, the interruption request of PIO is not acknowledged. Therefore, IEO of PIO returns to "1".



[5] As "4DH" has been decoded, IEO of SIOs becomes "1".



[6] Interruption request by PIO is acknowledged, and the IEO of PIO becomes "0".

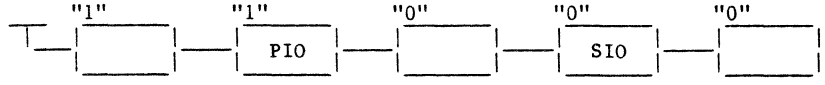


Fig. 3.11 Daisy-chain at RETI nstruction

3.4 SIO programming

Here, the meanings of each write register and read register are specifically explained with regard to each bit. It should be noted that parameter of write register (WR 4) must have been set prior to other parameters.

In addition, there are such registers that are used for only single channel.

WR 0: Write register 0

Table 3.2 Composition of Write Register 0

D7	D6	D5	D4	D3	D2	D1	D0
CRC Reset code		Basic command bit			Register pointer bit		

D0 - D2: Register pointer bit

These bits specify the registers to be written in or read out at the next byte. When write or read have ended, the register pointer specifies WR 0.

D3 - D5: Basic command bit

Command 0 (=000) : No operation

This command is for setting register pointer without operating SIO. This is used for reserving the space, in case there is any possibility of invalidating some command among the command chain to SIO or inserting command at some part of the command chain.

Command 1 (=001) : Abort generation

This command is used in order to generate abort sequence (sequence of successive "1" of more than 7).

This command is used for SDLC only.

Command 2 (=010) : External/status interruption reset

Once external interrupt or status interrupt occurs, status bits of RR0 are latched. This command enables status bits of RR0 for permitting the interrupt again.

Command 3 (=011) : Channel reset

This command operates same as reset signal is given at "RESET" terminal. The difference between them is that this command resets single channel only. Further, command to channel A also reset interruption priority circuit.

Command 4 (=100) : Enabling the interruption at the time of next character receive

This command is used, when the end of block in data block is detected and next data block is received and interruption generation is desired.

Command 5 (=101) : Transmitter interruption hold reset

In transmitter interruption enable mode, when transmit buffer becomes empty, interruption is generated. But, if there is no data to be sent, this command is used in order to suppress the transmitter interruption generation.

Command 6 (=110) : Error reset
Errors committed during block transmit (parity error and overrun error) are latched at D4 and D5 of RR 1. This command is used to clear them.
Command 7 (=111) : Return from interruption
This command operates same as it executes RETI instruction on SIO data bus. Therefore, even in MPU other than Z80 MPU (systems not using RETI interruption), daisy-chain in SIO can be used. This command is for channel A only.

D6 - D7: CRC reset code
These two bits are able to select one of receive CRC checker reset, tranbsmitter CRC generator reset and transmitter underrun/EOM reset.

Table 3.3 Reset Command Code

Reset command	D7	D6
No operation	0	0
Reset the receiving CRC checker.	0	1
Reset the transmitter CRC generator	1	0
Reset the transmitter underrun/EOM	1	1

WR1: Write register 1

Table 3.4 Composition of Write Register 1

D7	D6	D5	D4	D3	D2	D1	D0
Wait/ready Enable	Function selection	Receiving transmitting selection	Receiving interruption mode		Status affect vector	Transmitter interruption enable	External status interruption enable

D0: External/status interrupt enable
When this bit is set, interrupt can be generated at the time of synchronous character transmitter start even in such case as break/abort has been detected and finished, DCD, CTS or SYNC signals have changed, or transmitter underrun/EOM latch has been set.
D1: Transmit interrupt enable
If this bit is set, transmit interrupt is generaetd when transmit buffer becomes empty.
D2: Status affect vector
When this bit is set, D1 - D3 (V1-V3) of WR 2 varies according to interrupt conditions.
When this bit is not set, interrupt vector is sent with the same content as in WR 2. This bit can be used for channel B only.
D3-D4: Receive interrupt mode
This bit can select receiving interrupt mode.

D5-D7: Wait/ready function selection (D5-D7)

By these three bits, the selection of function of W/RDY terminal at SIO is carried out.

Wait/ready function is not used at the same time, since it is selected according to the program.

The semantics of each of these three bits are:

- o When D5 is set, they mean receive, whereas reset means tranmmit.
- o When D6 is set, this means READY terminals, and while reset, this means WAIT terminal.
- o When D7 is set, Wait/ready function becomes enable, while reset, becomes disable.

This means, for example, when D7, D6 and D5 are 110 and transmitter buffer is full, READY output becomes "1", and when tramsmitter buffer is empty, READY terminal becomes "0".

The above (D3-D4 and D5-D7) is summarized in the table below.

Table 3.5 Receiving Interruption Mode Codes

Receiving interrupt mode	D4	D3
Receiving interrupt disable	0	0
Interrupt in first character receiving or *special receiving condition	0	1
Interrupt in character receiving or special receiving condition	1	0
Interrupt in character receiving or special receiving condition (However, except parity error)	1	1

* The special receiving conditions are as follows:

- o End of frame (SDLC mode only)
- o Receiving overrun error
- o Parity error
- o Framing error

Table 3.6 Selection of Wait Ready Functions (D5 - D7)

Function	WAIT/REA' H/L Level	Terminal Condition	D7	D6	D5
WAIT	At floating active	-	0	0	-
READY	Low	-		1	
WAIT	High	Transmitter buffer is full and SIO data port have been selected.	1	0	0
READY	Floating	Tranmsitter buffer is empty.		1	0
WAIT	High	Transmitter buffer is full.		0	1
READY	Low	Transmitter buffer is empty.		1	
	Floating	Receiving buffer is full.			
	Low	Receiving buffer is empty and SIO data port have been selected.			
	Low	Receiving buffer is full.			
	High	Receiving bugger is empty.			

WR2: Write register 2

Table 3.7 Composition of Write Register 2

D7	D6	D5	D4	D3	D2	D1	D0

Interruption Vector

V7	V6	V5	V4	V3	V2	V1	V0

When the status affect vector bit is set, V3 to V1 change according to the interruption condition.

This write register is an interruption vector register. When D2 of WR 1 is not set, interruption vector is sent. When D2 of WR 1 is set, D1-D3 (V1-V3) varies according to interruption generate conditions. In this case, the content of WR 2 remains unchanged.
Further, since WR 2 exists in channel B only, programming of WR 2 of channel B is necessary even if only channel A of SIO is used.
The following Table (3.8) shows the V3 to V1 of an interrupt vector when the status affect vector bit is set.

Table 3.8 Codes according to interruption generate conditions of each channel

Channel	Interruption generate condition	V3	V2	V1
B	In case transmitter buffer is empty.	0	0	0
	In case external/status change	0	0	1
	In case of receiving character is effective.	0	1	0
	* In case of special receiving condition	0	1	1
A	In case transmitter buffer is empty.	1	0	0
	In case external/status change	1	0	1
	In case of receiving character is effective.	1	1	0
	* In case of special receiving condition	1	1	1

* The special receiving conditions are as follows:
- o End of frame (SDLC mode only)
- o Receiving overrun error
- o Parity error
- o Framing error

W3: Write register 3

Table 3.9 Composition of Write Register 3

D7	D6	D5	D4	D3	D2	D1	D0
Receiving bit/character		Auto enable	Enter hunt phase	Receiving CRC enable	Address search mode	Synchronous character load inhibition	Receiving enable

D0: Receiving enable
When this bit is set, receiving operation starts.
This bit is used for starting receiving operaiton, so it must be set after all receiving program are complete.

D1: Synchronous character load inhibition
In synchronous mode, if this bit has been set, synchronous character is not loaded on transmitter buffer.

D2: Address search mode
When SDLC mode is selected and this bit is set, any message having programmed address in WR 6 or other address than global address (FFH) is not received. Therefore, receive interruption does not occur until the addresses coincide.

D3: Receiving CRC enable
When this bit is set, CRC calculation starts at the time of the start of transmitter of the last data to the receiving buffer from the receiving shift register.

D4: Enter hunt phase
When synchronization settling is needed, SIO enter into hunt phase by setting this bit. In addition, once synchronization is settled, the hunt phase is released automatically.

D5: Auto enable
If this bit is set, transmitter is enabled when CTS terminal is "0". Further, when DCD terminal is "0", receiver is enabled.

D6-D7: Receiving character length
These bits specify the receiving bit number which composes one character. The table below shows the bit numbers per one character.

Table 3.10 Codes according to receiving character length

Bit number/Character	D7	D6
5	0	0
6	0	1
7	1	0
8	1	1

WR 4: Write register 4

Table 3.11 Composition of Write Register 4

D7	D6	D5	D4	D3	D2	D1	D0
Clock mode		Synchronous mode		Stop bit		Parity Even/ odd	Enable

D0: Parity selection
When this bit is set, 1 bit transmitter data is added to the bit numbers which are specified in D6-D7 of WR 3 and then this added bit number is received.
Further, if the selected character length is other than 8 bits, the added parity bit is set at MSB side of data bit and then will be transferred to receiving data FIFO.
When 8 bits of character length is selected, the parity bit will not be transferred to receiving data FIFO.

D1: Parity polarity
When parity is selected by this bit, it must be determined whether transmittance and check are carried out at even number or odd number. (even number = 1, odd number = 0)

D2-D3: Stop bit length
Stop bit length at asynchronous mode is selected by these bits. Both of D2 and D3 are set at "0" in synchronous mode.

Table 3.12 Codes according to Stop Bit Length

Stop bit	D3	D2
Synchronous mode	0	0
1 stop bit/character	0	1
1.5 stop bit/character	1	0
2 stop bit/character	1	1

D4-D5: Synchronous mode
Synchronous mode is selected by these bits.

Table 3.12 Codes according to Synchronous Mode

Synchronous mode	D3	D2
8 bits synchronous mode	0	0
16 bits synchronous mode (bisynch mode)	0	1
SDLC mode (Flag character:7FH)	1	0
External synchronous mode	1	1

D6-D7: Clock mode

Scale factor between transmitter/receiving clock and data transfer rate is selected by these bits. Besides, xl clock mode must be used in shynchronous mode. But, in asynchronous mode, the same scale factor is used at transmitter and receiving area.

Table 3.14 Codes according to Clock Mode

Clock Mode (Data Transfer Rate)	D7	D6
x 1 data transfer rate	0	0
x 16 data transfer rate	0	1
x 32 data transfer rate	1	0
x 64 data transfer rate	1	1

WR 5: Write register 5

Table 3.15 Composition of Write Register 5

D7	D6	D5	D4	D3	D2	D1	D0
DTR	Transmitter /character		Trans-mitter break	Trans-mitter enable	CRC-16 /SDLC	RTS	Trans-mitter CRC enable

D0: Transmitter CRC enable

When transmitter data are loaded from transmitter data buffer into transmitter shit register, if this bit is set, CRC calculation for these data is carried out. In synchronous mode or SDLC mode, if this bit is not set, CRC calculation and transmission of the transmitter underrun state are not carried out.

D1: Transmitter request

When this bit is set, RTS terminal becomes "0". If not, RTS terminal becomes "1".

In asynchronous mode, when tranmsitter buffer becomes empty, RTS terminal becomes "1". In synchronous mode and SDLC mode, RTS terminal state follows this bit state.

D2: CRC-16/SDLC

When this bit is set, CRC-16 multiple term expression (X**16+X**15+X**2+1) is selected. When this bit is reset, CRC-CCITT multiple term expression (X**16+X**12+X**5+1) is selected.

D3: Transmitter enable

If this bit is set, the transmitter is enabled.

Moreover, even if this bit is reset after data transmitter start, all of synchronous character and data in progreses of transmit.

D4: Transmitter break

If this bit is set, whatever data are transmitted, transmitter data line (TxD terminal) is forced to become the space state.

If this bit is reset, TxD becomes the marking state.

D5-D6: Transmitter character length

These bits indicate the transmitter data character length.

Table 3.10 Codes according to Transmitter Character Length

Bit number/Character	D6	D5
Max. 5	0	0
7 bits	0	1
6 bits	1	0
8 bits	1	1

As shown in Table 3.16, when bits below than 5 (4 bits, 3 bits etc.) per 1 character are transmitted, D5 and D6 are expressed as "0", but it is impossible to understand how many bits do data have. Therefore, data character should be treated according to the aftermentioned format. Now, D means the data.

Table 3.17 Transfer Format in case of max. 5 bits transmitter data

Transmitter bits/Character	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	0	0	0	D
2	1	1	1	0	0	0	D	D
3	1	1	0	0	0	D	D	D
4	1	0	0	0	D	D	D	D
5	0	0	0	0	D	D	D	D

D7: Data terminal ready
This bit indicates the state of DTR terminal.
When this bit is set, the state of DTR terminal becomes "0", when reset, it becomes "1".

WR 6: Write register 6

Table 3.18 Composition of Write Register 6

D7	D6	D5	D4	D3	D2	D1	D0
		S	Y	N	C		
7	6	5	4	3	2	1	0

This register is programmed in accordance with the following state:
- o External syncrhronous mode ..... Transmitter synchronous character
- o Mono-syncrhronous mode ..... Transmitter synchronous character
- o Bi-syncrhronous mode ..... First synchronous character
- o SDLC mode ..... Slave station address

WR 7: Write register 7

Table 3.19 Composition of Write Register 7

D7	D6	D5	D4	D3	D2	D1	D0
		S	Y	N	C		
15 (7)	14 (6)	13 (5)	12 (4)	11 (3)	10 (2)	9 (1)	8 (0)

This register is programmed in accordance with the following state:
- o Mono-syncrhronous mode ..... Receiving synchronous character
- o Bi-syncrhronous mode ..... Second synchronous character
- o SDLC mode ..... Flag character (7EH)

This register is not used in the external synchronous mode.

WR 0: Readout register 0

Table 3.15 Composition of Readout Register 0

D7	D6	D5	D4	D3	D2	D1	D0
Break /abort	Transmitter under run/ EOM	CTS	SYNC /Hunt	DCD	Transmitter buffer empty	Interruption pending	Receiving character effective

These registers are used for the external/status interruption mode.

D0: Receiving character effective
When there is any character of more than 1 byte in the receiving burrer, this bit is set. When the receiving buffer has become empty, this bit is reset.

D1: Interruption pending
When the interruption has occurred within SIO regardless of the kinds of the interruption conditions, this bit is reset. Moreover, this bit is effective for the channel A only.

D2: Transmitter buffer empty
When the tramsmitter data buffer is empty or SIO is reset, this bit is set. However, only when CRC character is sent in the synchronous mode and in SDLC mode, this bit is reset.

D3: Data carrier detect
This bit indicates the $\overline{DCD}$ terminal input status. if the external/status interruption is generated, the value of this bit is latched.

D4: Sync/hunt
The meaning of this bit differs according to the operation mode.

i) Asynchronous mode
In this mode, the $\overline{SYNC}$ terminal status of the SIO is shown. The external/status interruption is generated by the $\overline{SYNC}$ terminal status change.

ii) External synchronous mode
If synchronized through the detection of external synchronization, the bit must be changed to "0" at the trailing edge of the second $\overline{RxC}$ from the trailing edge of $\overline{RxC}$ which recevied the last bit of that synchronous character. That is, to make "$\overline{SYNC}$" input to "0" in the external circuit after detection of the synchronization, it is necessary to wait completely 2 receiving clock cycles. When "$\overline{SYNC}$" input becomes "0", the sync/hunt bit is set. If the synchronization is lost or end of message is detected, the enter hunt phase bit is set.

iii) Internal synchronous mode
In Monosynchronous and Bisynchronous modes, this bit is first set at "1" by the enter hunt phase command (D4 of WR3). After the SIO detected the synchronous character, this bit is reset.

iv) SDLC mode
This bit is set when the receiver is disabled or by the enter hunt phase command. Thereafter, when the open flag of the frame is detected, this bit is reset.

D5: CTS (clear to send)
This bit indicates the status opposite to the $\overline{CTC}$ terminal input status.

D6: Transmitter under Run/EOM
When SIO is reset (including channel reset), this bit is set. This bit can be reset only by the reset transmitter under run/EOM latch command (D7, D6 of WR 0=11).
When the transmitter under run status is caused, the external/status interruption is also generated.
This bit is also used for controlling transmission in the synchronous and SDLC modes.

D7: Break abort
In the receiving in asynchronous mode, tihs bit has a meaning of the break status detection. Detection of the break status sets this bit, generating the external/status interruption, while the external/status interruption reset command resets this bit.
After the break ended, the external/status interruption is again generated.
In case of the SDLC mode, detection of the abort sequence sets this bit, generating the external/status interruption.

RR 1: Read register 1

Table 3.21 Composition of Readout Register 1

D7	D6	D5	D4	D3	D2	D1	D0
End of frame	CRC/ framing error	Receiving overrun error	Parity error	Fraction			All character transmission

D0: All character transmission
In the asynchronous mode, when all characters are sent out of the tramsmitter or when there is no transmitted data in the SIO, this bit is set. Furhter, in the synchronouss mode this bit is always kept set.

D1 - D3: Fraction codes
Since I Field is normally integer times of character length, if not integer times, these codes show last fragmentary bits. These codes are significant only for transfer in which end-of-frame bit is set in the SDLC mode.

Example) Two cases that [1] number of bits of one character at the end of I Field is 8 (0) bits and [2] 4 bits are shown in Fig. 3.12.

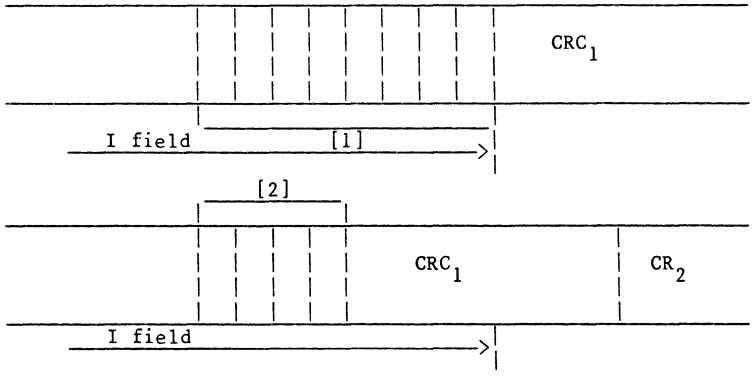


Fig. 3.12 I Field Fractions

Further, the fragmentary codes for receiving characters in length of 8 bits/character are as follows:

Table 3.22 (a) Bit pattern according to last fragmentary bits in I field

Last fraction bits in I fiedd		D3	D2	D1
1 byte before	2 byte before			
0	3	1	0	0
0	4	0	1	0
0	5	1	1	0
0	6	0	0	1
0	7	1	0	1
0	8	0	1	1
1	8	1	1	1
2	8	0	0	0

Even when length of I field receiving characters is other than 8 bits, a similar table can be composed for each character length.

Table 3.22 (b) Bit pattern according to data bits per I character (In case of no fraction)

bit/character	D3	D2	DO
5-bit/character	0	0	1
6-bit/character	0	1	0
7-bit/character	0	0	0
8-bit/character	0	1	1

D4: Parity error
When the parity selecting bit (Do of WR4) is set, if parity error is detected in receiving data, this bit is latched. The latch can be released by the error reset command (D5, D4, D3 of WR 0=110).

D5: Receive overrun error
Receiving data FIFO is set up to 3 characters. If there is no read by MPU and more characters are received, these characters are set as the receiving FIFO.
When these characters are read out by MPU, this receive overrun error is set. Once set, this bit latches its status. This bit is also reset if the error reset command (WR0 D3 - D5 commands) is written.

D6: CRC/framing error
In the asynchronous mode, if a framing error is detected in received characters, this bit is set. Since not latched, this bit is always updated.
In the synchronous mode and the SDLC mode, this bit shows the sent CRC check result. This bit is reset when the error reset command (command 6 of WR0 D3 - D5) is written.

D7: End of frame
When the end of flag is detected during receiving data and no CRC error and fragmentary code is normal, this bit is set. bit is reset by the error reset command (command 6 of WR0 D3 - D5).
Further, this bit is used only in the SDLC mode and is updated when the first character of next frame is received.

RR 2: Readout register 2

Table 2.23 Composition of Readout Register 2

D7	D6	D5	D4	D3	D2	D1	D0

Interruption Vector

V7	V6	V5	V4	V3	V2	V1	V0

When the status affect vector bit is set, V3 to V1 change according to the interruption condition.

When the status affect vector bit (D2 of WR1), is set, V3 to V1 change according to the interruption condition at the time. Vector that is read out is decided by the interrupt condition with the highest priority at the time of readout.
Further, when the status affect vector bit is reset, the content becomes equal to that of WR2.

3.5 How to use SIO

Two examples of systems using the SIO are introduced here.
Shown in Fig. 3.13 is an inter-processor communication system.
In this example, MPU at the left side transmits/receives data to/from other modules at the right side. Shown in Fig. 3.13 (a) is also a communication system as in Fig. 3.13 (b).
As shown in these examples, the SIO is used for data communication with external devices. In addition, the most great advantage of the SIO is that it requires less data lines than parallel communication as shown in this figure.

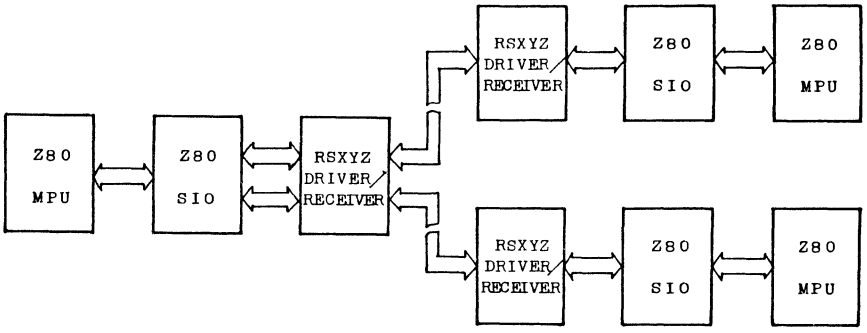


Fig. 3.13 (a) Inter-processor Communication System

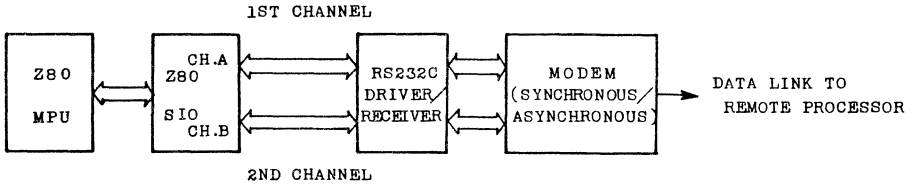


Fig. 3.13 (b) Inter-processor Communication System

4. ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
VCC	Supply Voltage	-0.5 to +7.0	V
VIN	Input Voltage	-0.5 to Vcc + 0.5	V
PD	Power Dissipation (TA = 85°C)	250	mW
TSOLDER	Soldering Temperature (10 sec)	260	°C
TSTG	Storage Temperature	-65 to 150	°C
TOPR	Operating Temperature	-40 to 85	°C

4.2 DC ELECTRICAL CHARACTERISTICS

TA = -40°C to 85°C, VCC = 5V ± 10%, VSS = 0V

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VILC	Low Clock Input Voltage		-0.3	-	0.6	V
VIHC	High Clock Input Voltage		VCC-0.6	-	VCC+0.3	V
VIL	Input Low Voltage (Except CLK)		-0.5	-	0.8	V
VIH	Input High Voltage (Except CLK)		2.2	-	VCC	V
VOL	Output Low Voltage	IOL = 2.0mA	-	-	0.4	V
VOH1	Output High Voltage (I)	IOH = -1.6mA	2.4	-	-	V
VOH2	Output High Voltage (II)	IOH = -250uA	VCC-0.8	-	-	V
IL1	Input Leakage Current	VSS ≦ VIN ≦ VCC	-	-	±10	uA
ILO	Output Leakage Current	VSS + 0.4 < VIN ≦ VCC	-	-	±10	uA
IL(SY)	$\overline{\text{SYNC}}$ Pin Leakage Current	VSS + 0.4 ≦ VIN ≦ VCC	-40	-	10	uA
ICC1	Power Supply Current	VCC=5V, fCLOK=(1), VIH=VIHC =VCC-0.2V, VIL=VILC =0.2V — P/F	-	4	10	mA
		AP/AF	-	2.5	6	
		AP-6/AF-6	-	4	10	
ICC2	Standby Supply Current Except SYNC at "L" output	VCC=5V, VIH=VIHC =Vcc-0.2V, VIL=VILC=0.2V	-	-	10	uA

Note (1) fCLK=1/TcC(MIN.)

4.3 AC ELECTRICAL CHARACTERISTICS

TA = -40°C to 85°C, VCC = 5V ± 10%, VSS = 0V

NO.	SYMBOL	PARAMETER	4MHz PF, AP/AF MIN.	4MHz PF, AP/AF MAX.	6MHz AP-6/AF-6 MIN.	6MHz AP-6/AF-6 MAX.	UNIT
1	TcC	Clock cycle time	250	DC	165	DC	ns
2	TwCh	Clock pulse width (High)	105	DC	70	DC	ns
3	TfC	Clock fall time	-	30	-	15	ns
4	TrC	Clock rise time	-	30	-	15	ns
5	TwCl	Clock pulse width (Low)	105	DC	70	DC	ns
6	TsCS(C)	Control signal to clock↓ setup time ($\overline{CE}$, C/$\overline{D}$, B/$\overline{A}$)	145	-	60	-	ns
7	TsRD(C)	$\overline{IORQ}$, $\overline{RD}$ to clock↓ setup time	115	-	60	-	ns
						-	ns
8	TdC(DO)	Clock↓ to data out delay	-	220	-	150	ns
9	TsDI(C)	Data in to clock setup (Write or $\overline{M1}$ cycle)	50	-	30	-	ns
10	TdRD(DOZ)	$\overline{RD}$↓ to data out float delay	-	110	-	90	ns
11	TdIO(DOI)	$\overline{IORQ}$↓ to data out delay (INTACK cycle)	-	160	-	120	ns
12	TsM1(C)	$\overline{M1}$ to clock↓ setup time	90	-	75	-	ns
13	TsIEI(IO)	IEI to $\overline{IORQ}$↓ setup time (INTACK cycle)	140	-	120	-	ns
14	TdM1(IEO)	M1↓ to IEO↓ delay (interrupt before $\overline{M1}$)	-	190	-	160	ns
15	TdIEI(IEOr)	IEI↑ to IEO delay (after ED decode)	160	-	-	110	ns
16	TdIEI(IEOf)	IEI↓ to IEO↓ delay	-	100	-	70	ns
17	TdC(INT)	Clock↓ to $\overline{INT}$↓ delay	-	200	-	150	ns
18	TdIO(W/RWf)	$\overline{IORQ}$↓ or $\overline{CE}$↓ to $\overline{W/RDY}$↓ delay (Wait mode)	-	210	-	175	ns
19	TdC(W/RRf)	Clock↓ to $\overline{W/RDY}$↓ delay (Ready mode)	-	120	-	100	ns
20	TdC(W/RWZ)	Clock↓ to $\overline{W/RDY}$ float delay (Wait mode)	-	130	-	110	ns
21	Th, Th (CS)	Any unspecified hold when setup is specified	0	-	0		ns
22	TwPh	Pulse width (High)	200	-	200		ns
23	TwPl	Pulse width (Low)	200	-	200	-	ns
24	TcTxC	$\overline{TxC}$ cycle time	400	-	330	-	ns

NO.	SYMBOL	PARAMETER	4MHz PF, AP/AF MIN.	4MHz PF, AP/AF MAX.	6MHz AP-6/AF-6 MIN.	6MHz AP-6/AF-6 MAX.	UNIT
25	TwTxCl	$\overline{TxC}$ width (Low)	180	∞	100	∞	ns
26	TwTxCh	$\overline{TxC}$ width (High)	180	∞	100	∞	ns
27	TdTxC(TxD)	$\overline{TxC}$ ↓ to TxD delay (x1 mode)	-	300	-	220	ns
28	TdTxC(W/RRf)	$\overline{TxC}$ ↓ to $\overline{W/RDY}$ ↓ delay (Ready mode)	5	9	5	9	CLK Periods*
29	TdTxC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ ↓ delay	5	9	5	9	CLK Periods*
30	TcRxC	$\overline{RxC}$ cycle time	400	∞	330	∞	ns
31	TwRxCl	$\overline{RxC}$ width (Low)	180	∞	100	∞	ns
32	TwRxCh	RxC width (High)	180	∞	100	∞	ns
33	TsRxD(RxC)	RxD to $\overline{RxC}$ ↑ setup time (x1 mode)	0	-	0	-	ns
34	ThRxD(RxC)	$\overline{RxC}$ ↑ to RxD hold time (x1 mode)	140	-	100	-	ns
35	TdRxC(W/RRf)	$\overline{RxC}$ ↓ to $\overline{W/RDY}$ ↓ delay (Ready mode)	10	13	10	13	CLK Periods*
36	TdRxC(INT)	$\overline{RxC}$ ↓ to $\overline{INT}$ ↓ delay	10	13	10	13	CLK Periods*
37	TdRxC(SYNC)	$\overline{RxC}$ ↓ to $\overline{SYNC}$ ↓ delay (Output modes)	4	7	4	7	CLK ods*
38	TsSYNC(RxC)	$\overline{SYNC}$ ↓ to $\overline{RxC}$ ↓ setup (External sync modes)	-100	-	-100	-	ns

(note) AC test condition
VIH=2.4V, VIHC=VCC-0.6V, VIL=0.4V, VILC=0.6V
VOH=2.2V, VOL=0.8V
CL=100pF

* System Clock
In all modes, the System Clock rate must be at least five times the maximum data rate. Restart must be active a minimum of one complete Clock cycle.

4.4 Capacitance

TA = 25°C

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C CLOCK	Clock Input Capacitance	f=1MHz All terminals except that to be measured should be earthed.	-	-	7	pF
CIN	Input Capacitance		-	-	5	pF
COUT	Output Capacitance		-	-	10	pF

4.5 Timing diagram

Numbers shown in the following figures correspond with those in the 4.3 A.C. Electrical Characteristics Table.

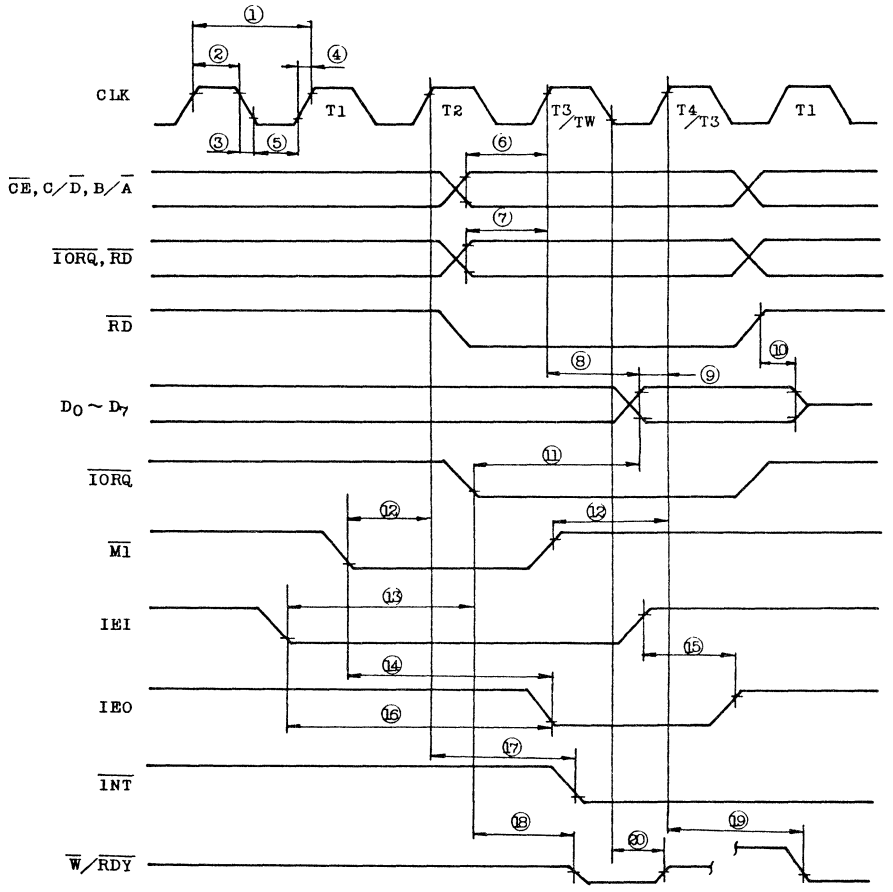


Fig. 4.1 (a) Timing Diagram

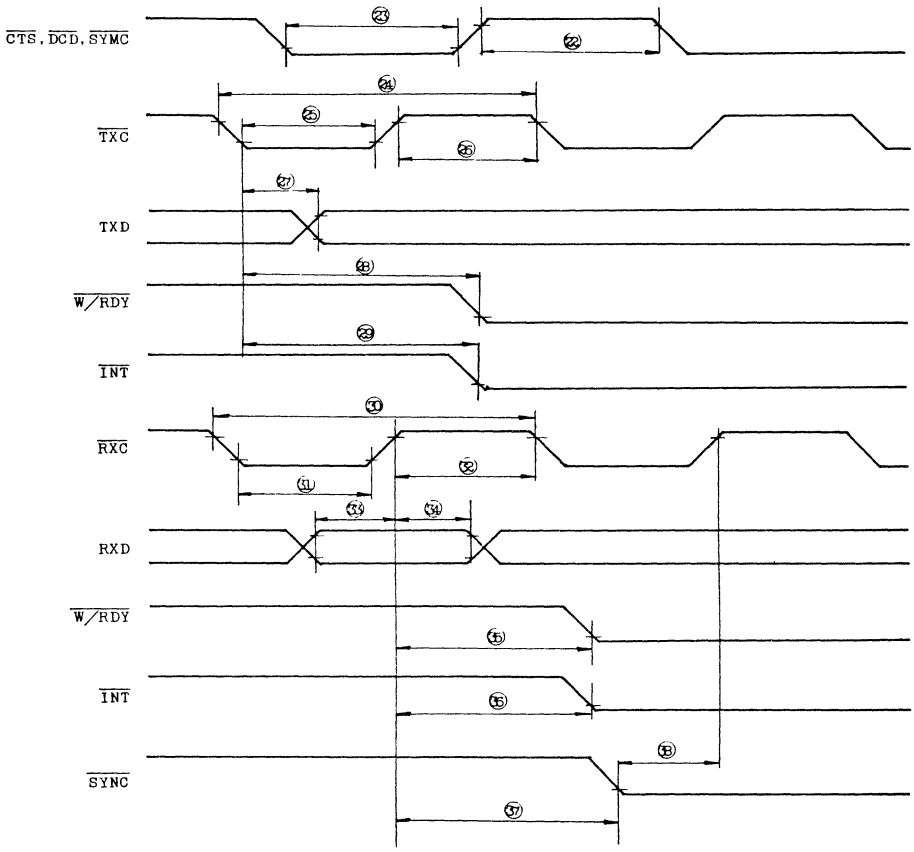
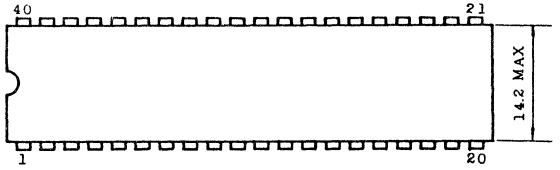
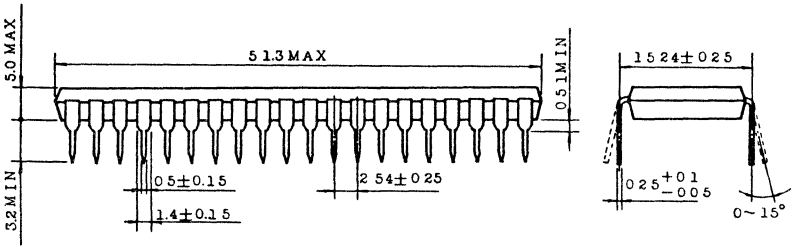


Fig. 4.1 (b) Timing Diagram

5. Package Dimension

Unit : mm





Note 1. This dimension is measured at the center of bending point of leads.

Note 2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoretical positions with respect to No.1 and No.40 leads.

5. Outline Drawing

Unit in mm

44-pin mini-flat package

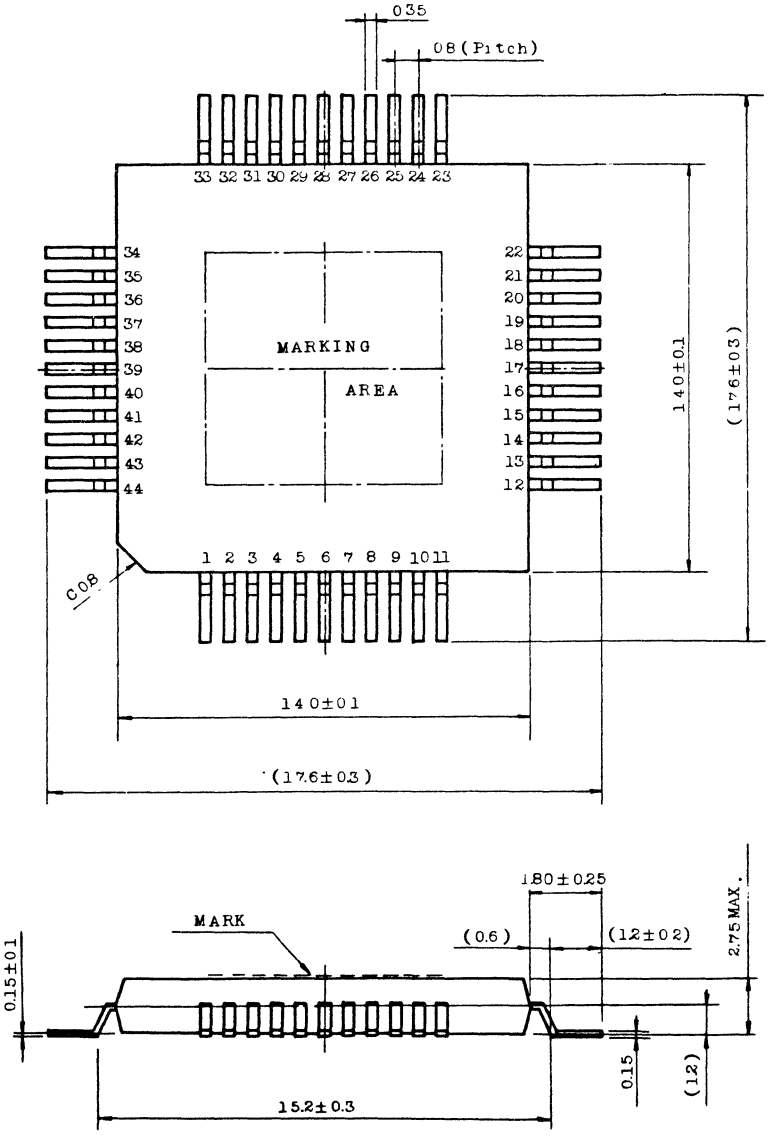


Fig. 5.1 Outline Drawing

6. Precautions

In the programming using the SIO, it can be used only for single channel according to registers and bits.

TMPZ84C60P
CMOS Z80 Clock Generator/Controller

1. General Description and Features

The TMPZ84C60P is a clock generator/controller for the TLCS-Z80 (CMOS) Family (Microprocessor (MPU) and its peripheral LSI's) fabricated with Toshiba's CMOS Silicon Gate Technology. The TMPZ84C60P is provided with two input terminals which are capable of selecting one of the following 3 modes when the TLCS-Z80 MPU execute the HALT instruction.

(1) RUN Mode
The clock (CLK) output operation of the TMPZ84C60P is continued. The TLCS-Z80 MPU is in the HALT state at this time and continues to execute the NOP instruction.

(2) IDLE Mode
The clock (CLK) output by the TMPZ84C60P is stopped. However, the internal oscillator only continues to run.

(3) STOP Mode
The operation of the TMPZ84C60P is completely stopped.
In STOP Mode, the operation of the microcomputer system is completely stopped. Therefore, it becomes possible to keep the system at low power consumption.
The TMPZ84C60P is molded in Toshiba's 16 pin standard DIP Package.

The principal functions and features of the TMPZ84C60P are as follows.

(1) Compatible with Toshiba CMOS Z80 (TLCS-Z80)
(2) Low power consumption
2mA Typ (@5V, 4MHz operation)
500uA Typ (@5V 4MHz) (IDLE Mode)
10uA Less (@5V stationary) (STOP Mode)
(3) Single 5V power supply (5V±10%)
(4) Extended operating temperature (-40°C to 85°C)
(5) The following 3 modes are selectable:
- RUN Mode
- IDLE Mode
- STOP Mode

(Note) Z80(R) is a registered trademark of Zilog Inc., U.S.A.

2. Pin Connections and Pin Functions

The pin connections and I/O pin names and brief functions of the TMPZ84C60P are shown below.

2.1 Pin connections

The pin connections of the TMPZ84C60P are as shown in Fig. 2.1.

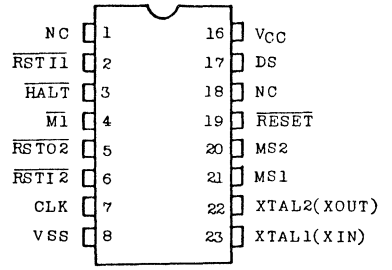


Fig. 2.1 Pin Connections

2.2 Pin names and functions

I/O pin names and functions of the TMPZ84C60P are as shown in Table 2.1.

Table 2.1 Pin Names and Functions

Pin Name	Number of Pin	Input/Output 3-state	Function
$\overline{\text{RSTI1}}$	1	Input	Restart signal from clock (CLK) stop state (Level trigger input)
$\overline{\text{HALT}}$	1	Input	Halt signal ($\overline{\text{HALT}}$) input
$\overline{\text{M1}}$	1	Input	Machine cycle 1 ($\overline{\text{M1}}$) signal input
$\overline{\text{RSTO2}}$	1	Output	Restart signal $\overline{\text{RSTI2}}$ output
$\overline{\text{RSTI2}}$	1	Input	Restart signal from clock (CLK) stop state (Edge trigger input)
CLK	1	Output	Single-phase clock output. When the HALT instruction in STOP Mode is executed, the TMPZ84C60P stops its operation and holds clock output at "0" level.
DS	1	Input	Counter output stage selecting input. Input to set up a warming-up time at time of restart from the clock stop state in stop mode.

Pin Name	Number of Pin	Input/Output 3-state	Function
$\overline{\text{RESET}}$	1	Output	Reset signal. Restart signal from clock (CLK) stop state (Level trigger input)
MS1, MS2	2	Input	Mode selection input. One of 3 modes (RUN, IDLE, STOP) is selected according to the state of these 2 pins
XTAL 1 (XIN) XTAL 2 (XOUT)	2	Input Output	Crystal oscillator connecting terminal
NC	1		Use in the open state
VCC	1	Power supply	+5V
VSS	1	Power supply	0V

3. Description of Operation

The system configuration, functions and basic operation of the TMPZ84C60P Clock Generator are described here.

3.1 Block diagram

The block diagram of the internal cinfiguration is shown in Fig. 3.1.

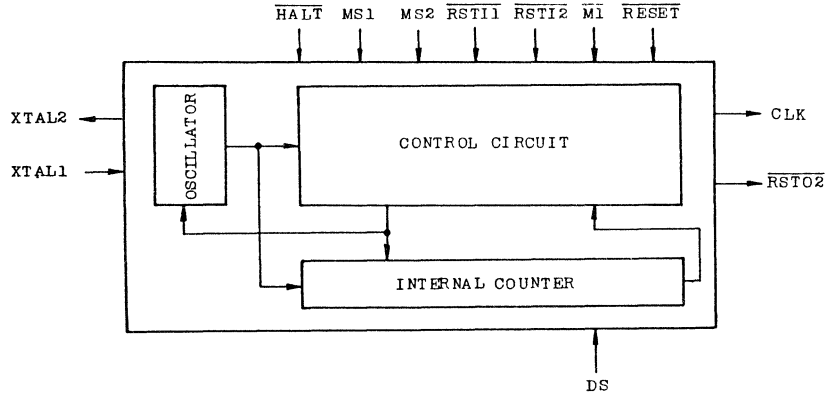


Fig. 3.1 Block Diagram

3.2 System cinfiguration

The internal cinfiguration of TMPZ84C60P is as shown in Fig. 3.1.
The waveform that is input by the external oscillator is converted into the square-wave for clock by the internal oscillator. Clock is controlled by the control circuit and the counter, and output to the outside.
In this section, the following principal compoments and functions which must be known in using the T6497 will be described.

(1) Generation of clock
(2) Operation mode
(3) Warming-up time at time of restart

3.2.1 Generation of clock

The T6497 has a built-in oscillation circuit and required clock can be easily output from CLK terminal by connecting an oscillator to the external terminals (XTAL1, XTAL2). Clock in the same frequency as input oscillation frequency is output.
Examples of oscillator connection are shown in Fig. 3.2.
Quartz crystal unit characteristics are required following.

(1) fosc = 4MHz (CIN=COUT=30pF)
Rs $\leqq$ 50 ohm
Cs $\leqq$ 40 pF
(ex. TOKYO DENPA COMP. LTD. "MR4000-C20")

(2) fosc = 2.5MHz (CIN=COUT=36pF)
Rs $\leqq$ 300 ohm
Cs $\leqq$ 4 pF
(ex. TOKYO DENPA COMP. LTD. "MR2500-C20")

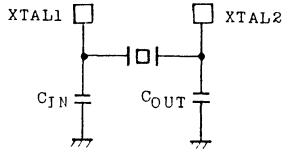


Fig. 3.2 Examples of Oscillator Connection

3.2.2 Operation modes

There are 3 kinds of operations modes; Run mode, IDLE mode, and STOP mode available for the T6497. One of these modes can be selected by the mode select input (MS1, MS2). These operation modes are effective when the TLCS-Z80 MPU is executing the HALT instruction. When fetching the HALT instruction, MPU outputs "0" on the $\overline{HALT}$ terminal to indicate that MPU enters into the HALT state. After executing the HALT instruction, the T6497 performs the operation in one of these mode by this signal.
The operations of these modes in the HALT state are shown in Table 3.1.

Table 3.1 T6497 Operation Modes

MS2	MS2	Operation Mode	Content of Operation at HALT State
1	1	RUN Mode	Continues to supply clock to the outside.
0	* Note)	IDLE Mode	The internal oscillator only operates and supply of clock to the outside is stopped. Clock output (CLK) is held at "0" level.
1	1	STOP Mode	The internal operations are all stopped. Clock output (CLK) is held at "0" level.

Note) MS2 can be used for any modes.

Clock is continuously supplied in any mode except the HALT state. MPU is restarted from the clock stop state in IDLE mode and STOP mode by inputting one of $\overline{RSTI1}$, $\overline{RSTI2}$ or $\overline{RESET}$ signal.
MPU is released from the HALT state by the input of RESET signal or acceptance of maskable ($\overline{INT}$ signal) or non-maskable ($\overline{NMI}$ signal) interrupt request. Tehrefore, these signals are normally connected to MPU as follows:

- $\overline{RESET}$ signal is commonly used with MPU.
- $\overline{INI}$ signal (maskable interrupt input) and RSTI1 signal (restart input) are commonly used.
- $\overline{RETO2}$ signal (output of restart input signal RSTI2) is connected to $\overline{NMI}$ signal (non-maskable interrupt input).

3.2.3 Warming-up time at restart (STOP mode)

When released from the HALT state by acceptance of interrupt request, MPU will execute the interrupt routine. Therefore, to restart the clock by $\overline{RSTI1}$ or $\overline{RSTI2}$ restart signal in STOP mode it is necessary to supply clock to the outside after the oscillation is sufficiently stabilized. The TMPZ84C60P provides a sufficient warming-up time enough to reach stabilized frequency by operating the internal counter. The warming-up is completed and clock output is started at the trailing edge of the internal counter output which is divided oscillation frequency. There is the DS input terminal provided for setting this warming-up time, and a time of 2**17 (DS=0) or 2**14 (DS=1) division of the externally connected oscillator is provided.

The block diagram of the internal counter unit is shown in Fig. 3.3 and the relationship bedtween the logic of the DS terminal and warming-up time is shown in Table 3.2.
Further, in case of the restart by $\overline{RESET}$ signal, the internal counter does not operate for a quick operation at time of power ON.

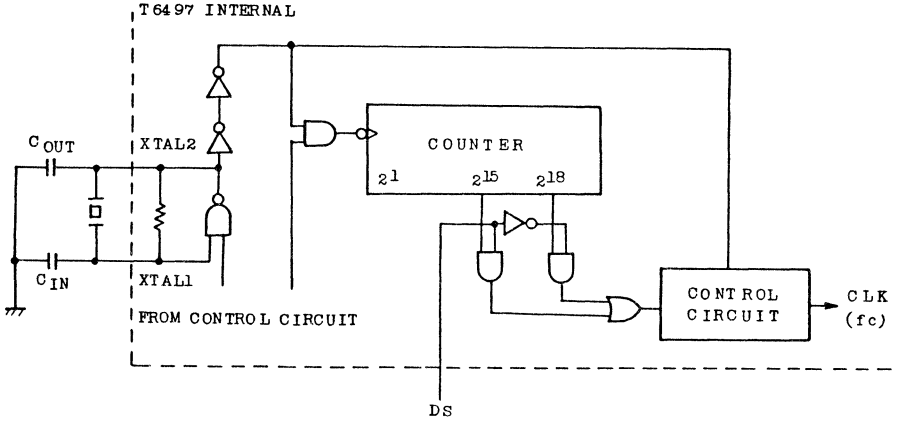


Fig. 3.3 Block Diagram of Internal Counter

Table 3.2 Warming-up Time

DS	Counter Output	Warming-up Time			
			fXTAL=4MHz	fXTAL=2.5MHz	fXTAL=400kHz
0	2**18	2**17/fXTAL	=32.8ms	=52.4ms	=328ms
1	2**15	2**14/fXTAL	= 4 ms	= 6.6ms	= 40ms

3.3 Status change flowchart and basic timing

In this section, the status change and basic timing when the TMPZ84C60P is operating are explained.

3.3.1 Status change flowchart

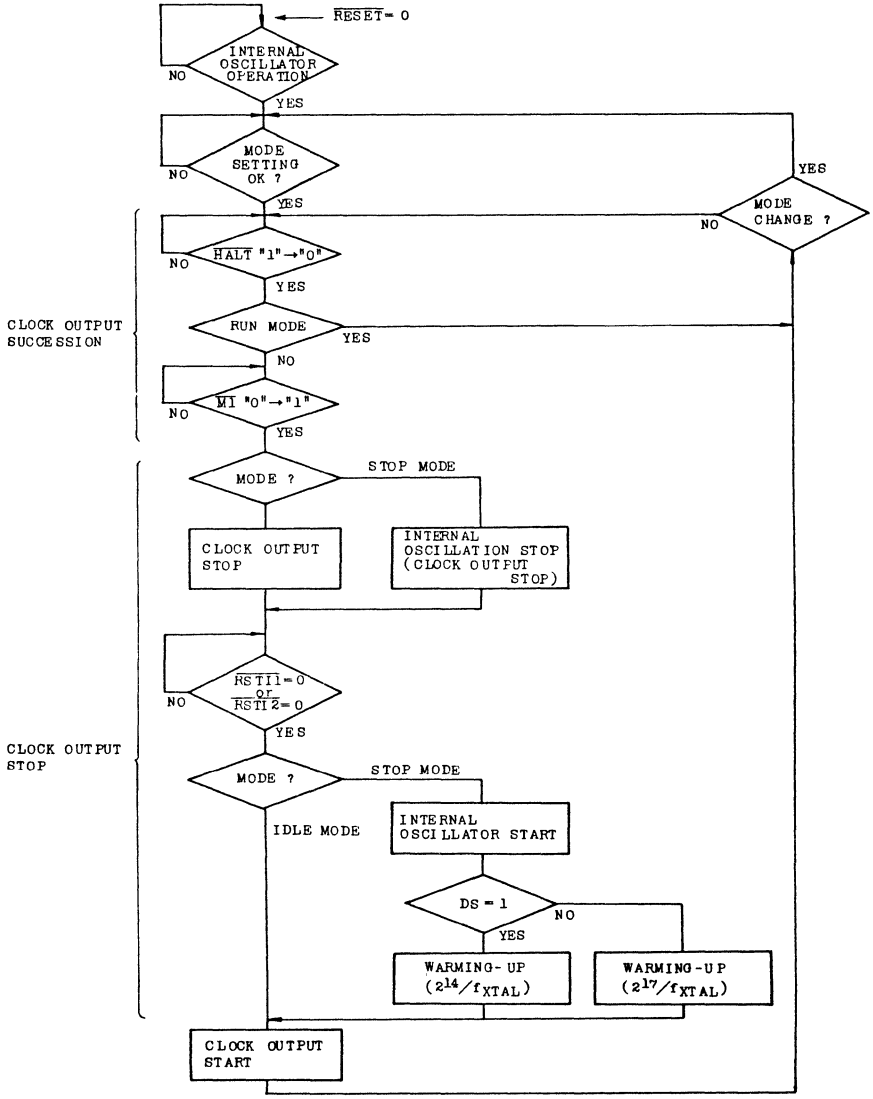


FIG. 3.4 Status Change Flowchart

3.2.2 Basic timing

(1) Operation when HALT instruction is executed
The basic timing of each mode when the TLCS-Z80 MPU executes the HALT instruction is explained.
In synchronous with the fall of T4 state of the $\overline{HALT}$ instruction operation code fetch cycle (M1), MPU makes the $\overline{HALT}$ signal to "0" level. By this signal, the TMPZ84C60P detects that MPU is going to enter into the HALT state.

(a) RUN mode (MS=1, MS2=1)
The basic timing of RUN mode is shown in Fig. 3.5.
In the RUM mode, clock is continuously supplied to the outside even when MPU is in the HALT state. This mode is used on a system requiring the memory address refresh.

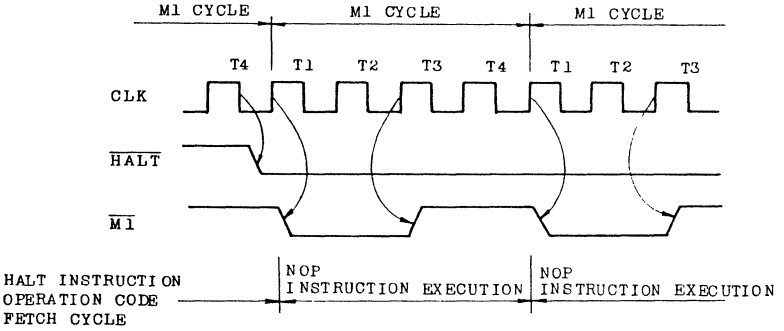


Fig. 3.5 RUM Mode Timing

(b) IDLE mode (MS1=0) and STOP mode (MS1=1, MS2=0)
The basic timing in the IDLE and STOP modes is shown in Fig. 3.6.
In these modes, clock output is stopped at the "0" level during T4 state by the $\overline{HALT}$ signal and $\overline{M1}$ signal following the HALT instruction. However, in case of the stop mode the internal oscillator of the TMPZ84C60P is also stopped.

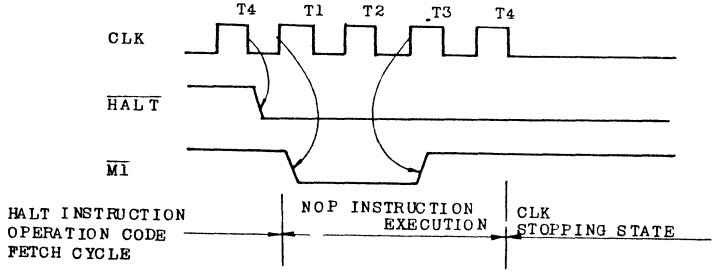


Fig. 3.6 IDLE/STOP Mode Timing

(2) Restart from clock stop
The clock is restarted from the stopped state in the IDLE or STOP mode when "0" is input to any one of the following signals:

- o $\overline{\text{RSTI1}}$ (level trigger input)
- o $\overline{\text{RSTI2}}$ (edge trigger input)
- o $\overline{\text{RESET}}$ (level trigger input)

(a) Restart in IDLE mode

The restart sequence from the clock output stop state in the IDLE mode is shown in Fig. 3.7. In the restart in the IDLE mode, the clock output is restarted in a relatively short delay time as the internal oscillator is in operation even during the clock output is kept stopped.

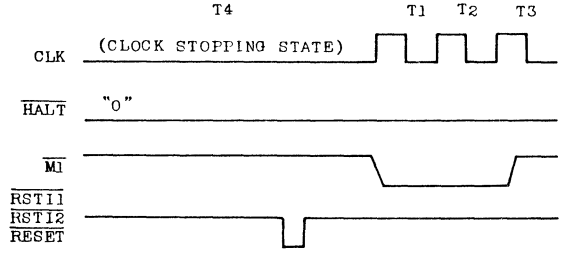


Fig. 3.7 Restart Sequence Timing from Clock Stop State (IDLE mode)

(b) Restart in STOP mode

The restart sequence from the clock output stopped state in the STOP mode is shown in Fig. 3.8. In restarting the clock output by inputting "0" into $\overline{\text{RSTI1}}$ or $\overline{\text{RSTI2}}$ signal, a warming-up time is automatically provided by the internal counter.

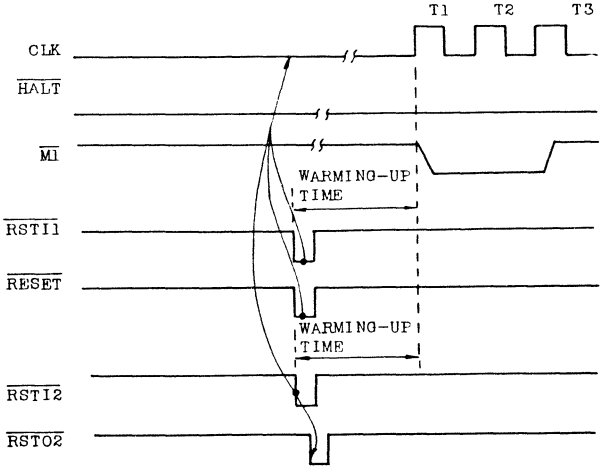


Fig. 3.8 Restart Sequence Timing from Clock Stop State (STOP mode)

3.4 Method of use

Connection of the TMPZ84C60P with MPU is explained here on the $\overline{HALT}$ release operation.

3.4.1 Common use of $\overline{RESET}$ signal

Shown in Fig. 3.9 are examples of restart timing in the STOP mode when the TLCS-Z80 MPU and TMPZ84C60P use RESET signal commonly.
To reset the TLCS-Z80 MPU, RESET signal must be kept at "0" level for at least 3 clocks. Further, when RESET signal becomes "1" level, MPU is released from the HALT state after the dummy cycle for at least 2T states and executes an instruction starting from address 0000H.

In restarting the clock output in the STOP mode by $\overline{RESET}$ signal, the internal counter for determining the warming-up time does not operate. Note that MPU may not be restarted properly due to unstable clock output immediately after the internal oscillator is restarted. Therefore, RESET signal should be kept at "0" level for a sufficient period of time enough to firmly reset MPU by taking stability of crystal oscillation at time of power ON.

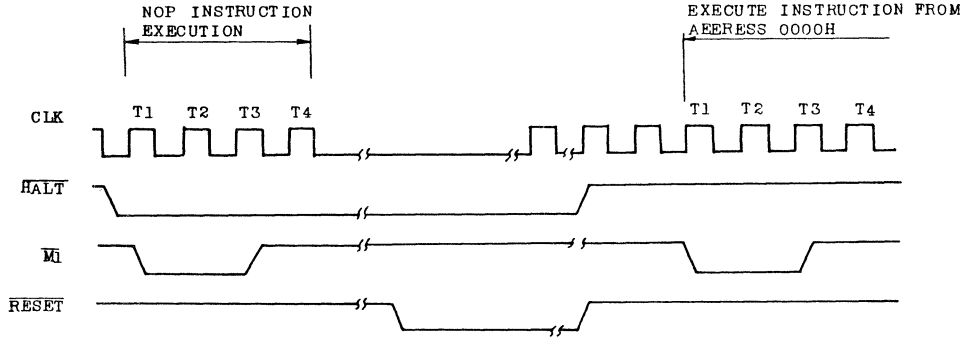


Fig. 3.9 Example of Clock Restart Timing by RESET Signal

3.4.2 HALT release by interrupt signal

When the TMPZ84C60P is in the IDLE or STOP mode, the clock output is restarted by RSTI1 or RSTI2 signal input and MPU starts to run according to that clock input. However, after the clock output, MPU is still in the HALT state and executes the NOP instruction. To release MPU from the HALT state, it is necessary to input the interrupt signal ($\overline{INT}$ or $\overline{NMI}$). MPU samples the interrupt signal at the leading edge of the last clock of each instruction (NOP instruction for the HALT state).

(1) When non-maskable interrupt ($\overline{NMI}$) is used:

The non-maskable interrupt is the edge trigger input, and there is a flip-flop (F/F) in MPU. The state of this internal NMI F/F is sampled at the leading edge of the last clock of an instruction. Therefore, if a short low active ("0") pulse has been input before the interrupt signal sampling timing, this interrupt request is accepted.

RSTI2 input of the TMPZ84C60P is output to RSTO2 through the internal circuit. It is therefore recommended that the restart signal is generated to the RSTI2 input terminal and RSTO2 signal is output into the NMI terminal of MPU.

(2) When maskable interrupt (INT) is used:
For maskable interrupt, the interrupt enable flip-flop (IFF) must be set to "1" before "0" of $\overline{INT}$ input signal is recognized. In the connection of MPU and TMPZ84C60P, this interrupt signal $\overline{INT}$ is jointly used with the restart signal $\overline{RSTI1}$ of the TMPZ84C60P. Shown in Fig. 3.10 are examples of the timing when $\overline{RSTO2}$ output signal of the TMPZ84C60P is input to $\overline{NMI}$ of MPU and $\overline{RSTI1}$ signal of the TMPZ84C60P is jointly used with $\overline{INT}$ signal of MPU.

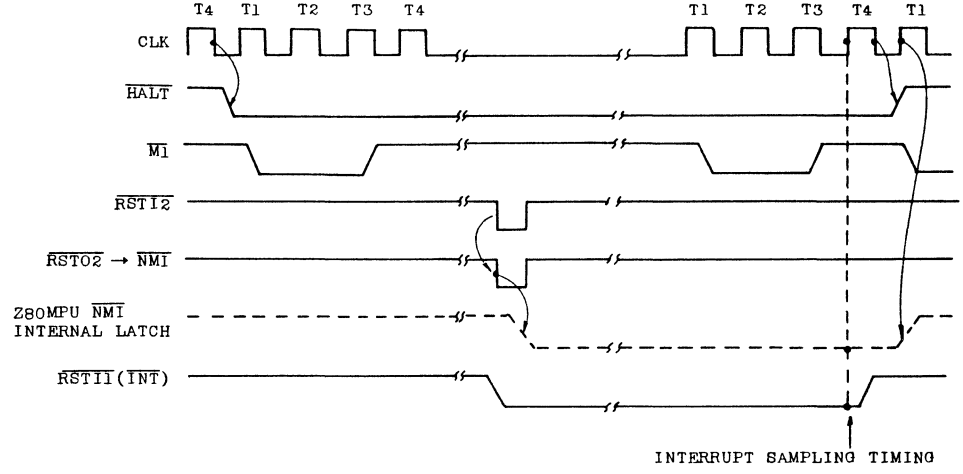


Fig. 3.10 Example of Clock Restart Timing by $\overline{RSTI1}$ or $\overline{RSTI2}$ Signals

3.4.3 Example of connection
A connecting example of the TMPZ84C60P and MPU is shown in fig. 3.11. This figure shows an example when $\overline{RSTO2}$ output signal of the TMPZ84C60P is input into $\overline{NMI}$ of MPU by jointly using RESET signal with MPU and $\overline{RESI1}$ signal of the TMPZ84C60P and $\overline{INT}$ signal of MPU are joinly used.

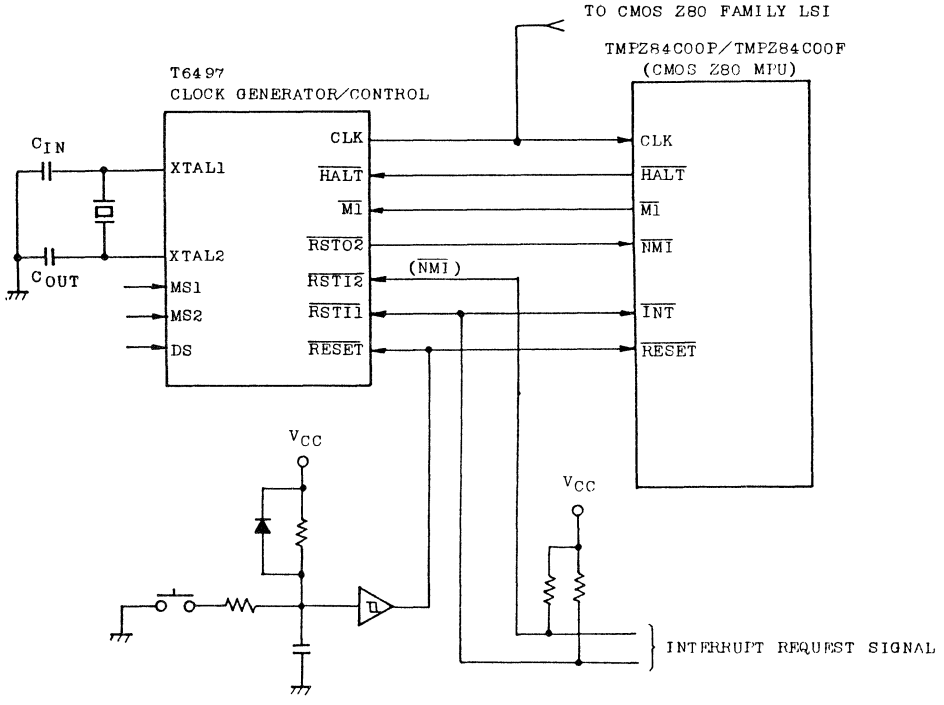


Fig. 3.11 Connecting Example of the TMPZ84C60P and CMOS Z80 MPU

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Symbol	Item	Rating	Unit
VCC	Supply Voltage	-0.5 to +7	V
VIN	Input Voltage	-0.5 to Vcc + 0.5	V
PD	Power Dissipation (TA=85°C)	250	mW
TSOLDER	Soldering Temperature (10 sec)	260	°C
Tstg	Storage Temperature	-65 to 150	°C
Topr	Operating Temperature	-40 to 85	°C

4.2 DC Electrical Characteristics

TA = -40°C to 85°C, VCC = 5V ± 10%, VSS = 0V

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage (Except XTAL 1, 2)		-0.5	-	0.8	V
VIH	Input High Voltage (Except XTAL 1, 2)		2.2	-	VCC	V
VOLC	Output Low Voltage (CLK)	IOL = 2.0mA	-	-	0.4	V
VOL	Output Low Voltage (Except CLK)	IOL = 2.0mA	-	-	0.4	V
VOHC	Output High Voltage (CLK)	IOH = -250μA	VCC-0.6	-	-	V
VOH1	Output High Voltage (Except CLK)	IOH = -1.6mA	2.4	-	-	V
VOH2	Output High Voltage (Except CLK)	IOH = -250μA	VCC-0.8	-	-	V
ILI	Input Leak Current	VSS≦ VIN≦ VCC	-	-	ç1	μA
ICC1	Supply Current (Operation) (RUM Mode)	VCC=5V, fXTAL=4MHz VIHC=VIH=VCC-0.2, VILC=VIL=0.2	-	2	4	mA
ICC2	Supply Current (STOP Mode)	VCC=5V, VIHC=VIH=VCC-0.2, VILC=VIL=0.2	-	0.3	10	μA
ICC3	Supply Current (IDLE Mode)	VCC=5V, fXTAL=4MHz VIHC=VIH=VCC-0.2, VILC=VIL=0.2	-	0.5	1	mA

4.3 AC Electrical Characteristics

TA = -40°C to 85°C, VCC = 5V ± 10%, VSS = 0V (*): TEST CONDITION

NO.	SYMBOL	ITEM		(*)	MIN.	TYP.	MAX.	UNIT
1	TcC	CLK frequency			250	-	-	ns
2	TwCh	High CLK width			110	-	-	ns
3	TwCl	Low CLK width			110	-	-	ns
4	TrC	CLK rising time			-	-	15	ns
5	TfC	CLK falling time			-	-	15	ns
6	TsHALT(Mlr)	$\overline{\text{HALT}}$ set-up time			10	-	-	ns
7	TwRSTI1	Low $\overline{\text{RSTI1}}$ width			80	-	-	ns
8	TwRSTI2	Low $\overline{\text{RSTI2}}$ width			200	-	-	ns
9	TdRST02 (RSTI2f)	$\overline{\text{RST02}}$ delay time			-	-	100	ns
10	TwRST02	Low $\overline{\text{RST02}}$ width			80	-	-	ns
11	TwRESET	Low $\overline{\text{RESET}}$ width			80	-	-	ns
12	TRST1S	CLK restart time by RSTI1 (STOP Mode)	DS=0		-	(2**17+2.5)TcC	-	ns
			DS=1		-	(2**14+2.5)TcC	-	ns
13	TRST2S	CLK restart time by RSTI2 (STOP Mode)	DS=0		-	(2**17+2.5)TcC	-	ns
			DS=1		-	(2**14+2.5)TcC	-	ns
14	TRST1I	CLK restart time by $\overline{\text{RSTI1}}$ (IDLE Mode)			-	2.5TcC	-	ns
15	TRST2I	CLK restart time by $\overline{\text{RSTI2}}$ (IDLE Mode)			-	2.5TcC	-	ns
16	TRESETI	CLK restart time by $\overline{\text{RESET}}$ (IDLE Mode)			-	1TcC	-	ns

(Note) Test conditions
1) Input high voltage VIH = 2.4V, Input low voltage VIL = 0.4V
2) Testing point
a VOH = 2.2V, VOL = 0.8V (however, except CLK output)
b CLK Output: VOH = VCC-0.6V, VOL = 0.4V

4.4 Capacitance

TA = 25°C

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CCLOCK	Clock Input Capacitance	f=1MHz All terminals except that to be measured should be earthed.	-	-	15	pF
CIN	Input Capacitance		-	-	5	pF
COUT	Output Capacitance		-	-	6	pF

4.5 Timing diagram

Figs. 4.1 to 4.4 show the basic timings of respective operations. Numbers shown in the figures correspond with those in the AC Electrical Characteristics Table in 4.3.

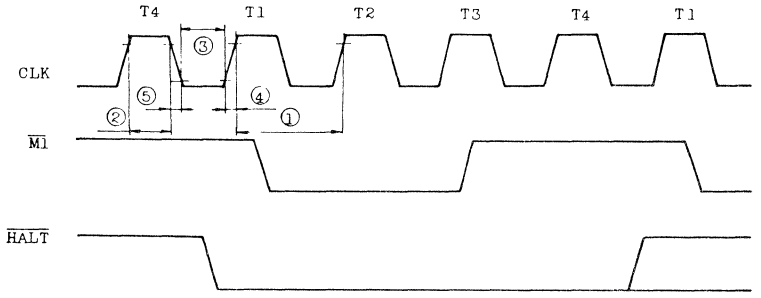


Fig. 4.1 Clock Timing

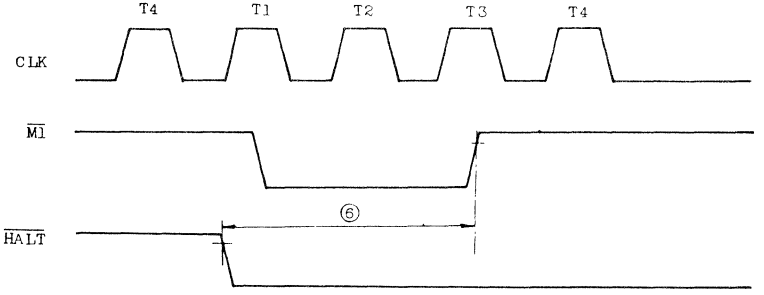


Fig. 4.2 Clock Stop Timing (IDLE/STOP Mode)

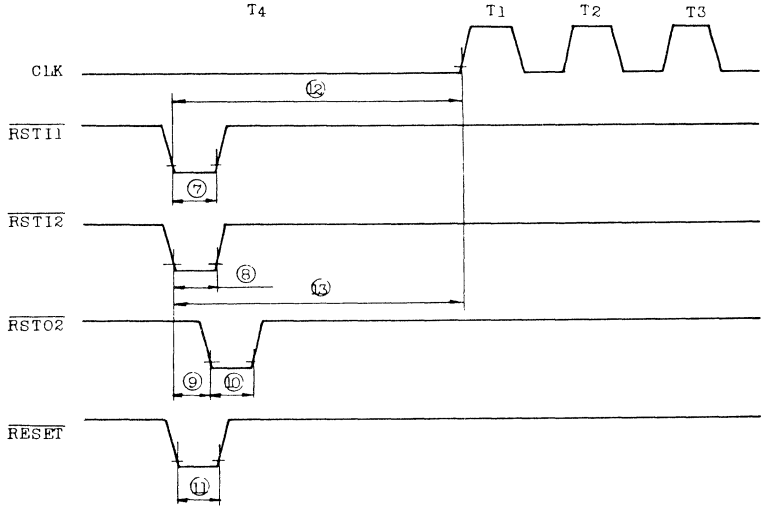


Fig. 4.3 Clock Restart Timing (STOP Mode)

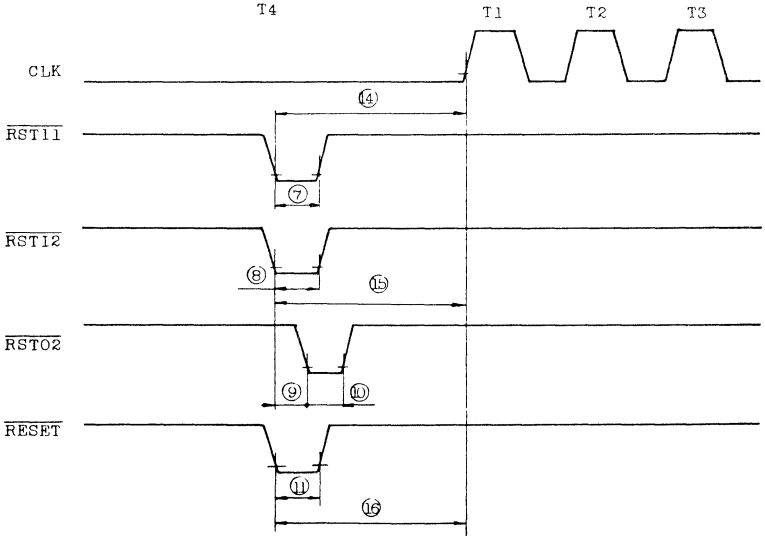
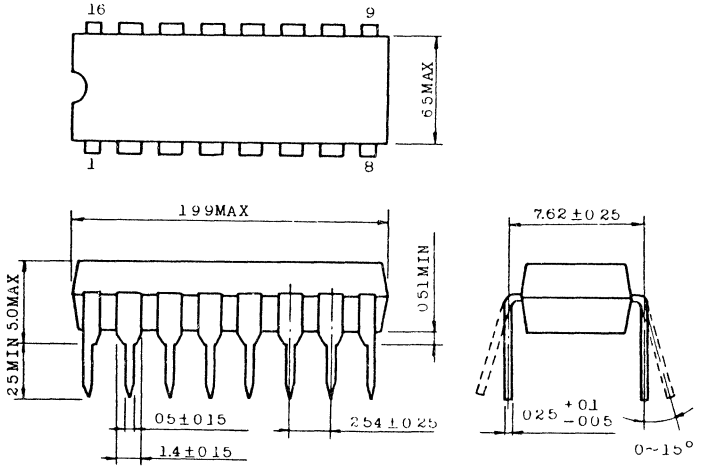


Fig. 4.4 Clock Restart Timing (IDLE Mode)

5. Outline Drawing

Unit in mm



Note 1. This dimension is measured at the center of bending point of leads.
Note 2. Each lead pitch is 2.54mm, and all the leads are located within ¢0.25 mm from their theoretical positions with respect to No.1 and No.16 leads.

6. Precautions

When the TMPZ84C60P is used, care should be taken to the following points.

(1) In using $\overline{\text{RESET}}$ signal commonly with MPU, hold $\overline{\text{RESET}}$ signal at "0" for a sufficient period of time enough to positively reset MPU. Especially, in case of the restart in the STOP mode using $\overline{\text{RESET}}$ signal, be careful as output of the internal oscillator is not stable.

(2) MPU is not released from the HALT state simply when the clock input is resumed. To release MPU, it is necessary to reset MPU or accept an interrupt request.

(3) Since $\overline{\text{RSTI2}}$ signal of the TMPZ84C60P and $\overline{\text{NMI}}$ signal of MPU are both trailing edge trigger inputs, if both signals are jointly used, $\overline{\text{RSTI2}}$ signal only may be detected and $\overline{\text{NMI}}$ signal may not be detected in some cases. This trouble can be solved by using $\overline{\text{RSTO2}}$ signal, which is the output signal of $\overline{\text{RSTI2}}$ input signal, as the input signal to $\overline{\text{NMI}}$ in order to a sufficient pulse for the detection.

TLCS-85 Family LSI

8-BIT SINGLE CHIP MICROPROCESSOR

GENERAL DESCRIPTION

The TMP8085AP, from here on referred to as the TMP8085A, is a new generation, complete 8 bit parallel central processing unit (CPU). Its high level of system integration allows a minimum system of there IC's : TMP8085A (CPU), TMP8155P/TMP8156P (RAM/IO) and TMP8355P (ROM/IO). The TMP8085A uses a multiplexed data bus. The address is plit between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of TMP8155P/TMP8156P/TMP8355P memory products allow a direct interface with TMP8085P.

FEATURES

- 0.8μSec Instruction Cycle (TMP8085AP-2 : CLK Cycle Period @200nSec)
- Single +5V Power Supply
- On-Chip Clock Generator (with External Crystal or RC Network)
- On-Chip System Controller; Advanced Cycle status information available for Large System Control
- 4 Vectored Interrupts (One is Non-Maskable)
- Decimal, Binary and Double Precision Arithmetic
- Serial In/Serial Out Port
- Direct Addressing Capability to 64K Bytes of Memory
- Compatible with Intel's 8085A

PIN CONNECTION
(TOP VIEW)

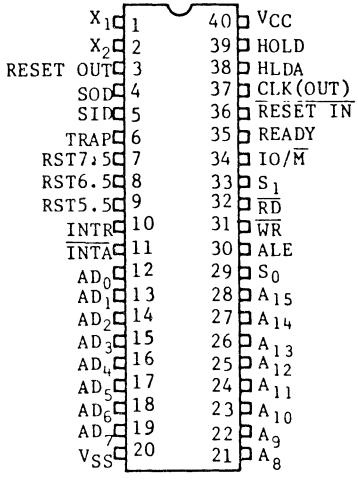


FIGURE 2. TMP8085A PINOUT DIAGRAM

BLOCK DIAGRAM

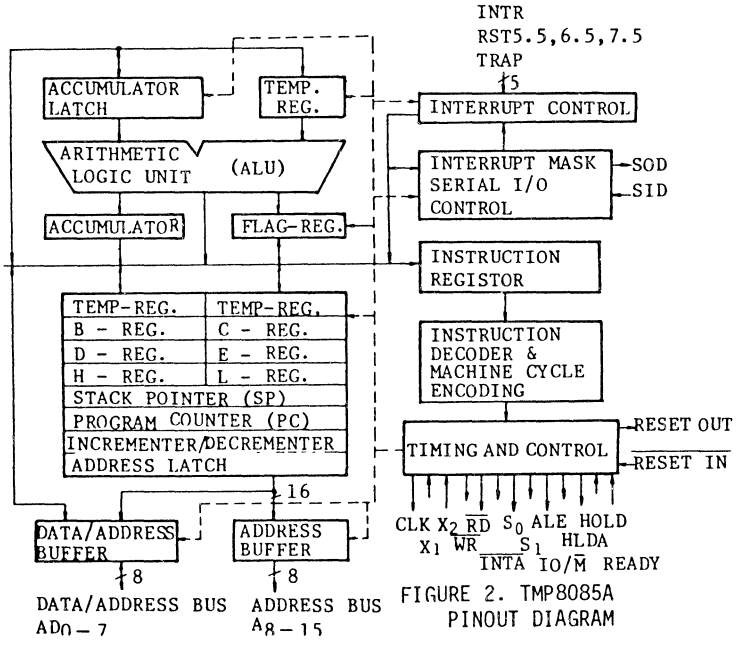


FIGURE 2. TMP8085A PINOUT DIAGRAM

PIN NAME AND PIN DESCRIPTION

X_1, X_2 (Input)

Crystal, LC, or RC network are connected to X_1 and X_2 to drive the internal clock generator. X_1 and X_2 can also be driven from an externally derived frequency source. The input frequency is devided by 2 to give the processor's internal operating frequency.

CLK (Output)

Clock Output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.

$\overline{\text{RESET IN}}$ (Input)

The RESET Input initialize the processor by clearing the program counter, instruction register, SOD latch, Interrupt Enable flip-flop and HLDA flip-flop. The address and data buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{\text{RESET IN}}$ is a Schmitt-triggered input, allowing connection to an RC network for power on RESET delay. The TMP8085A is held in the reset condition as long as $\overline{\text{RESET IN}}$ is applied.

RESET OUT (OUTPUT)

The RESET OUT signal indicates that the TMP8085A is being reset. It can be used as a system reset. It is synchronized to the processor clock and lasts an integral number of clock periods.

SOD (Output)

Serial output data line. The output SOD is set or reset as specified by the SIM instruction.

SID (Input)

Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.

INTR (Input)

INTERRUPT REQUEST signal provides a mechanism for external devices to modify the instruction flow of the program in progress. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is recognized, the processor will complete the execution of the current instruction, and then the Program Counter (PC) will be inhibited from incrementing and an $\overline{\text{INTA}}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by RESET and immediately after an interrupt is accepted.

$\overline{INTA}$ (Output)

INTERRUPT ACKNOWLEDGE: Occurs in response to an Interrupt input and indicates that the processor will be ready for an interrupt instruction on the data bus. It is used instead of (and has the same timing as) $\overline{RD}$ during the instruction cycle after an INTR is accepted.

RST 5.5
RST 6.5 } (Inputs)
RST 7.5

RESTART INTERRUPTS: These three inputs have the same timing as INTR exept they cause an internal RESTART to be automatically inserted. These interrupts have a higher priority than INTR. The priority of these interrupts is ordered as shown Table 1. They may be individually masked out using the SIM instruction.

TRAP (Input)

Trap interrupt is a nonmaskable RESTART interrupt. It is sampled at the same timing as INTR or RST 5.5 - 7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt.

AD_0 - AD_7 (Input/Output, 3-state)

Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T_1 state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.

A_8 - A_{15}(Output, 3-state)

The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.

S_0, S_1, and $IO/\overline{M}$ (Output)
Machine cycle status:

$IO/\overline{M}$	S_1	S_0	Status
0	1	1	Opcode fetch
0	1	0	Memory read
0	0	1	Memory write
1	1	0	I/O read
1	0	1	I/O write
1	1	1	Interrupt Acknowledge
TS	0	0	Halt
TS	X	X	Hold
TS	X	X	Reset

Note: TS = 3-state (high impedance)
X = unspecified

ALE (Output)

Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE can be used to strobe the status information. ALE is never 3-stated.

$\overline{WR}$ (Output, 3-state)

WRITE control: A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. It is 3-stated during Hold and Halt modes and during RESET.

$\overline{RD}$ (Output, 3-state)

READ control: A low level on $\overline{RD}$ indicates the selected memory or I/O device to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.

READY(Input)

When READY is absent (low), indicating the external operation is not complete, the processor will enter the Wait state. It will wait an integral number of clock cycles for READY to go high before completing the read or write cycle.

HOLD (Input)

The Hold input allows an external signal to cause the processor to relinquish control over the address bus and the data bus. When Hold goes active, the processor completes its current operation, activates the HLDA output, and puts the Address, Data, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines into their high-impedance state. Internal processing can continue. The Holding device can then utilize the address and data buses without interference. The processor can regain the bus only after the Hold is removed.

HLDA (Output)

The Hold Acknowledge output signal is a response to a Hold input. It indicates that the processor has received the HOLD request and it will relinquish the bus in the next cycle. HLDA goes low after the Hold request is moved. The processor takes the bus one half clock cycle after HDLA goes low.

V_{CC}
+5 volt supply

V_{SS}
Ground Reference

FUNCTIONAL DESCRIPTION

The TMP8085A is a complete 8-bit parallel central processor. Its basic clock speed is 3 MHz. Also it is designed to fit into a minimum system of three IC's: The CPU (TMP8085A), a RAM I/O (TMP8155P or TMP8156P), and a ROM or EPROM I/O chip (TMP8355P or TMP8755AC).

The TMP8085A is provided with internal 8-bit registers and 16-bit registers. The TMP8085A has eight addressable 8-bit registers. Six of them can be used either as 8-bit registers or as 16-bit register pairs. In addition to the register pairs, the TMP8085A contains two more 16-bit registers. The TMP8085A register set is as follows:

- The accumulator (A Register) is the focus of all of the accumulator instructions, which include arithmetic, logic, load and store, and I/O instructions.
- The program counter (PC) always points to the memory location of the next instruction to be executed.
- General - purpose registers BC, DE, and HL may be used as 8-bit registers or as three 16-bit registers, interchangeably, depending on the instruction being performed.
- The stack pointer (sp) is a special data pointer that always points to the stack top (next available stack address).
- The flag register contains five one-bit flags, each of which records processor status information and may also control processor operation.

The five flags in the TMP8085A CPU are shown below:

(MSB)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S	Z		AC		P		C

- The carry flag (C) is set and reset by arithmetic operations. An addition operation that resutls in an overflow out of the high-order bit of the accumulator sets the carry flag. The carry flag also acts as a "borrow" flag for subtract instruction.
- The auxiliary carry flag (AC) indicates overflow out of bit 3 of the accumulator in the same way that C flag indicates overflow out of bit 7. This flag is commonly used in BCD arithmetic.
- The sign flag (S) is set to the condition of the most significant (MSB) bit of the accumulator following the execution of arithmetic or logic instructions.
- The zero flag (Z) is set if the result generated by certain instructions is zero. The zero flag is cleared if the result is not zero.
- The parity flag (P) is set to 1 if the parity (number of 1-bits) of the accumulator is even. If odd, it is cleared.

In the TMP8085A microprocessor are contained the functions of clock generation, system bus control, and interrupt priority selection, in addition to execution of the instruction set. The TMP8085A uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (T_1 clock cycle) of a machine cycle the lower order address is sent out on the Address/Data Bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

INTERRUPT AND SERIAL I/O

The TMP8085A has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to 9080A INT. Each of three RESTART inputs 5.5, 6.5, 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three RESTART interrupts cause the internal execution of RESTART if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes internal execution independent of the state of the interrupt enable or masks.

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are high levelsensitive like INTR and are recognized with the same timing as INTR.RST 7.5 is rising edge-sensitive.

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the interrupt request. The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{\text{RESET IN}}$ to the TMP8085A. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending : TRAP-highest priority. RST 7.5, RST 6.5, RST 5.5, INTR - lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt a RST 7.5 routine if the interrupts were reenabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic errors such as power failure or bus error. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive. The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches.

TABLE 1. INTERRUPT PRIORITY, RESTART ADDRESS, AND SENSITIVITY

Name	Priority	Address Branched to When Interrupt Occurs	Type Trigger
TRAP	1	24 (Hex.)	Rising edge and high level until sampled.
RST 7.5	2	3C (Hex.)	Rising edge (latched).
RST 6.5	3	34 (Hex)	High level until sampled.
RST 5.5	4	2C (Hex.)	High level until sampled.
INTR	5	See Note (2)	High level until sampled.

Notes: (1) The processor pushes the PC on the stack before branching to the indicated address.

(2) The address branched to depends on the instruction provided to the TMP8085A when the interrupt is acknowledged.

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instruction provide current interrupt enable status. Performing a RIM instruction following INTR, or RST 5.5 - 7.5 will provide current interrupt enable status, revealing that interrupts are disabled.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD date.

BASIC TIMING

The execution of each instruction by the TMP8085A consists of a sequence of from one to five machine cycles, and cach machine cycle consists of a minimum of from three to six clock cycles. Most machine cycles consist of three T states, (cycles of the CLK output) with the exception of opecode fetch, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of $\overline{READY}$ or HOLD inputs). Any T state must be one of ten possible states, shown in Table 3.
At the beginning of every machine cycle, the TMP8085A sends out three status signals ($IO/\overline{M}$, S_1, S_0) that define what type of machine cycle is about to take place. The TMP8085A also sends out a 16-bit address at the beginning of every machine cycle to identify the particular memory location or I/O port that the machine cycle applies to.

The special timing signal, ADDRESS LATCH ENABLE (ALE), is used a strobe to sample the lower 8-bits of address on the $AD_0 - AD_7$ lines. ALE is present during T_1 of every machine cycle. Control lines $\overline{RD}$ ($\overline{INTA}$) and $\overline{WR}$ become active later, at the time when the transfer of data is to take plece.
Figure 3 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction).

TABLE 2. TMP8085A MACHINE CYCLE CHART

MACHINE CYCLE	IO/$\overline{M}$	S_1	SO	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
OPCODE FETCH	0	1	1	0	1	1
MEMORY READ	0	1	0	0	1	1
MEMORY WRITE	0	0	1	1	0	1
I/O READ	1	1	0	0	1	1
I/O WRITE	1	0	1	1	0	1
ACKNOWLEDGE OF INTR	1	1	1	1	1	0
BUS IDLE : DAD	0	1	0	1	1	1
ACK. OF RST, TRAP	1	1	1	1	1	1
HALT	TS	0	0	TS	TS	1

NOTE: 0 = Logic "0", 1 = Logic "1", TS = High Impedance

TABLE 3. TMP8085A MACHINE STATE CHART

MACHINE STATE	S_1, S_0	IO/$\overline{M}$	A_8-A_{15}	AD_0-AD_7	$\overline{RD}, \overline{WR}$	$\overline{INTA}$	ALE
T_1	X	X	X	X	1	1	1°
T_2	X	X	X	X	X	X	0
T_{WAIT}	X	X	X	X	X	X	0
T_3	X	X	X	X	X	X	0
T_4	1	0†	X	TS	1	1	0
T_5	1	0†	X	TS	1	1	0
T_6	1	0†	X	TS	1	1	0
T_{RESET}	X	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	1	0
T_{HOLD}	X	TS	TS	TS	TS	1	0

NOTES: (1) 0 = Logic "0", 1 = Logic "1", TS = High Impedance, X = Unspecified

(2) °ALE not generated during 2nd and 3rd machine cycles of DAD instruction

(3) † IO/$\overline{M}$ = 1 during T_4 - T_6 of INA machine cycle

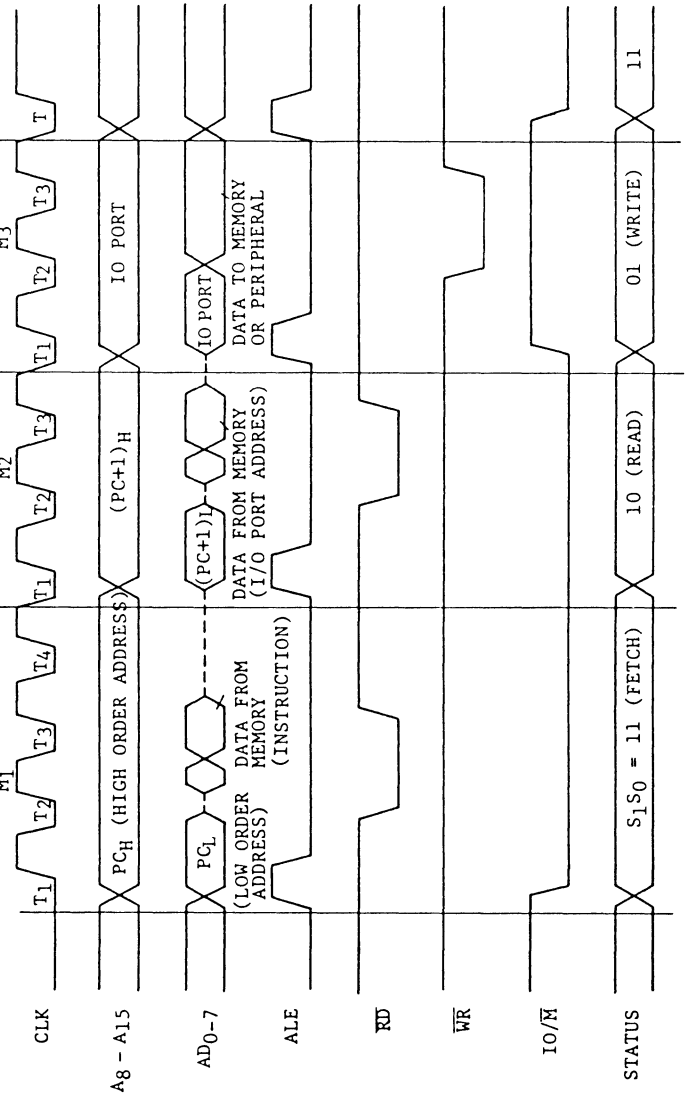


FIGURE 3. TMP8085A BASIC SYSTEM TIMING

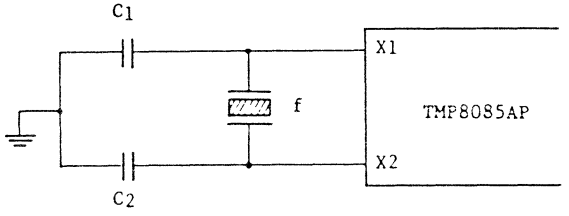
DRIVING THE X1 AND X2 INPUTS

You may drive the clock inputs of the TMP8085A with a crystal, an LC tuned circuit, an RC network or an external clock source. The driving frequency must be at least 1 MHz, and must be twice the desired internal clock frequency.

A. Quartz Crystal Clock Driver

If a crystal used, it must have the following characteristics.

- Parallel resonance at twice the clock frequency desired
- C_S (shunt capacitance) $\leq$ 7 PF
- R_S (equivalent shunt resistance) $\leq$ 75 Ohms



Note a value of the external capacitors C_1 and C_2 between X1, X2 and ground.

We recommended the following.

1MHz $\leq$ f < 4MHz: C_1=20pF, C_2=20pF

4MHz $\leq$ f $\leq$ 8MHz: C_1=10pF, C_2=10pF

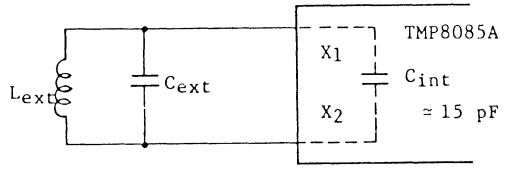
8MHz < f $\leq$ 10MHz: C_1=0, C_2=0

B. LC Turned Circuit Clock Driver

A parallel-resonant LC circuit may be used as the frequency-determining network for the TMP8085A, providing that its frequency tolerance of approximately 10% is acceptable. The components are chosen from the formula.

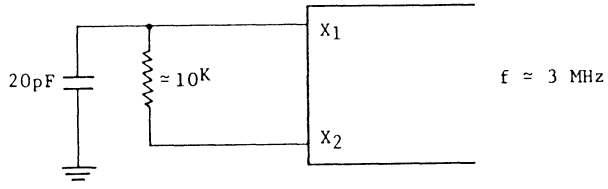
$$f = \frac{1}{2\pi \sqrt{L\ (C_{ext} + C_{int})}}$$

The use of an LC circuit is not recommended for frequencies higher than approximately 5 MHz.

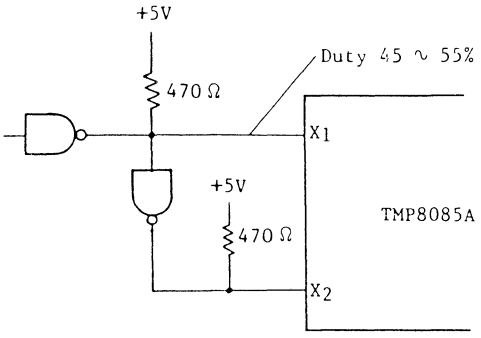


C. RC Circuit Clock Driver

An RC circuit may be used as the frequency - determining network for the TMP 8085A if maintaining a precise clock frequency is of no importance. Variations in the on-chip timing generation can cause a wide variation in frequency when using RC circuit. The driving frequency generated by the circuit shown is approximately 3 MHz. It is not recommended that frequencies greatly higher or lower than this be attempted.



D. External clock Driver Circuit



POWER ON AND $\overline{\text{RESET IN}}$

The TMP 8085A is not guaranteed to work until 10 ms after V_{CC} reaches 4.75 V. It is suggested that $\overline{\text{RESET IN}}$ be kept low during this period. Note that the 10 ms period does not include the time it takes for the power supply to reach its 4.75 V level.

INSTRUCTION SET

Symbols and Abbreviations

SYMBOLS	DEFINITION
ddd,sss	The bit pattern designating one of the registers A,B,C,D,E,H,L (ddd=destination, sss=source):

ddd or sss	REGISTER NAME
111	A
000	B
001	C
010	D
011	E
100	H
101	L
110	M (Memory)

r,r1,r2	One of the registers A,B,C,D,E,H,L
d8	8-bit data quantity
d16	16-bit data quantity
addr8	8-bit address of an I/O device
addr	16-bit address quantity
RP	The bit pattern designating one of the register pairs B,D,H,SP:

RP	rp	REGISTER PAIR (rpH)(rpL)
00	B	B-C
01	D	D-E
10	H	H-L
11	SP	SP

B_2	The second byte of the instruction
B_3	The third byte of the instruction
0	Affected
S	Set
R	Reset
-	Not affected

Data Transfer

Mnemonic	Instruction Code								Operation	Bytes	States	Flag				
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				C	Z	S	P	AC
MOV r1, r2	0	1	d	d	d	S	S	S	(r1) ← (r2)	1	4	-	-	-	-	-
MOV M, r	0	1	1	1	0	S	S	S	[(H)(L)] ← (r)	1	7	-	-	-	-	-
MOV r, M	0	1	d	d	d	1	1	0	(r) ← [(H)(L)]	1	7	-	-	-	-	-
MVI r, d8	0	0	d	d	d	1	1	0	(r) ← (B_2)	2	7	-	-	-	-	-
					B_2											
MVI M, d8	0	0	1	1	0	1	1	0	[(H)(L)] ← (B_2)	2	10	-	-	-	-	-
					B_2											
LDA addr	0	0	1	1	1	0	1	0	(A) ← [(B_3)(B_2)]	3	13	-	-	-	-	-
					B_2											
					B_3											
LDAX B	0	0	0	0	1	0	1	0	(A) ← [(B)(C)]	1	7	-	-	-	-	-
LDAX D	0	0	0	1	1	0	1	0	(A) ← [(D)(E)]	1	7	-	-	-	-	-
LHLD addr	0	0	1	0	1	0	1	0	(L) ← [(B_3)(B_2)]	3	16	-	-	-	-	-
					B_2				(H) ← [(B_3)(B_2)+1]							
					B_3											
LXI H, d16	0	0	1	0	0	0	0	1	(H) ← (B_3)	3	10	-	-	-	-	-
					B_2				(L) ← (B_2)							
					B_3											
LXI D, d16	0	0	0	1	0	0	0	1	(D) ← (B_3)	3	10	-	-	-	-	-
					B_2				(E) ← (B_2)							
					B_3											
LXI B, d16	0	0	0	0	0	0	0	1	(B) ← (B_3)	3	10	-	-	-	-	-
					B_2				(C) ← (B_2)							
					B_3											
LXI SP, d16	0	0	1	1	0	0	0	1	$(SP)_H$ ← (B_3)	3	10	-	-	-	-	-
					B_2				$(SP)_L$ ← (B_2)							
					B_3											
SHLD addr	0	0	1	0	0	0	1	0	[(B_3)(B_2)] ← (L)	3	16	-	-	-	-	-
					B_2				[(B_3)(B_2)+1] ← (H)							
					B_3											
STA addr	0	0	1	1	0	0	1	0	[(B_3)(B_2)] ← (A)	3	13	-	-	-	-	-
					B_2											
					B_3											

Mnemonic	Instruction Code								Operation	Bytes	States	Flag				
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				C	Z	S	P	AC
STAX B	0	0	0	0	0	0	1	0	[(B)(C)] ← (A)	1	7	-	-	-	-	-
STAX D	0	0	0	1	0	0	1	0	[(D)(E)] ← (A)	1	7	-	-	-	-	-
SPHL	1	1	1	1	1	0	0	1	(SP) ← (H)(L)	1	6	-	-	-	-	-
XCHG	1	1	1	0	1	0	1	1	(H) ↔ (D) (L) ↔ (E)	1	4	-	-	-	-	-
XTHL	1	1	1	0	0	0	1	1	(L) ↔ [(SP)] (H) ↔ [(SP)+1]	1	16	-	-	-	-	-
IN addr8	1	1	0	1	1	0	1	1	(A) ← (data)	2	10	-	-	-	-	-
					B_2											
OUT addr8	1	1	0	1	0	0	1	1	(data) ← (A)	2	10	-	-	-	-	-
					B_2											

Branch

Mnemonic	Instruction Code								Operation	Bytes	States	Flag				
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				C	Z	S	P	AC
JMP addr	1	1	0	0	0	0	1	1	(PC) ← (B_3)(B_2)	3	10	-	-	-	-	-
					B_2											
					B_3											
JNZ addr	1	1	0	0	0	0	1	0	If Z = 0 (PC) ← (B_3)(B_2), If Z = 1 (PC) ← (PC) + 3	3	7/10	-	-	-	-	-
					B_2											
					B_3											
JZ addr	1	1	0	0	1	0	1	0	If Z = 1 (PC) ← (B_3)(B_2), If Z = 0 (PC) ← (PC) + 3	3	7/10	-	-	-	-	-
					B_2											
					B_3											
JNC addr	1	1	0	1	0	0	1	0	If C = 0 (PC) ← (B_3)(B_2), If C = 1 (PC) ← (PC) + 3	3	7/10	-	-	-	-	-
					B_2											
					B_3											
JC addr	1	1	0	1	1	0	1	0	If C = 1 (PC) ← (B_3)(B_2), If C = 0 (PC) ← (PC) + 3	3	7/10	-	-	-	-	-
					B_2											
					B_3											

Mnemonic	Instruction Code								Operation	Bytes	States	Flag				
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				C	Z	S	P	AC
JPO addr	1	1	1	0	0	0	1	0	If P = 0	3	7/10	-	-	-	-	-
					B_2				(PC) ← (B_3)(B_2),							
					B_3				If P = 1							
									(PC) ← (PC) + 3							
JPE addr	1	1	1	0	1	0	1	0	If P = 1	3	7/10	-	-	-	-	-
					B_2				(PC) ← (B_3)(B_2),							
					B_3				If P = 0							
									(PC) ← (PC) + 3							
JP addr	1	1	1	1	0	0	1	0	If S = 0	3	7/10	-	-	-	-	-
					B_2				(PC) ← (B_3)(B_2),							
					B_3				If S = 1							
									(PC) ← (PC) + 3							
JM addr	1	1	1	1	1	0	1	0	If S = 1	3	7/10	-	-	-	-	-
					B_2				(PC) ← (B_3)(B_2),							
					B_3				If S = 0							
									(PC) ← (PC) +3							
CALL addr	1	1	0	0	1	1	0	1	[(SP)-1] ← (PCH)	3	18	-	-	-	-	-
					B_2				[(SP)-2] ← (PCL)							
					B_3				(SP) ← (SP) - 2							
									(PC) ← (B_3)(B_2)							
CNZ addr	1	1	0	0	0	1	0	0	If Z = 0, the actions specified in the CALL instruction are performed.	3	9/18	-	-	-	-	-
					B_2											
					B_3											
									If Z = 1							
									(PC) ← (PC) + 3							
CZ addr	1	1	0	0	1	1	0	0	If Z = 1, the actions specified in the CALL instruction are performed.	3	9/18	-	-	-	-	-
					B_2											
					B_3											
									If Z = 0,							
									(PC) ← (PC) + 3							

Mnemonic	Instruction Code								Operation	Bytes	States	Flag				
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				C	Z	S	P	AC
CNC addr	1	1	0	1	0	1	0	0	If C = 0, the actions specified in the CALL instruction are performed. If C = 1 (PC) ← (PC) + 3	3	9/18	-	-	-	-	-
				B_2												
				B_3												
CC addr	1	1	0	1	1	1	0	0	If C = 1, the actions specified in the CALL instruction are performed. If C = 0 (PC) ← (PC) + 3	3	9/18	-	-	-	-	-
				B_2												
				B_3												
CPO addr	1	1	1	0	0	1	0	0	If P = 0, the actions specified in the CALL instruction are performed. If P = 1 (PC) ← (PC) + 3	3	9/18	-	-	-	-	-
				B_2												
				B_3												
CPE addr	1	1	1	0	1	1	0	0	If P = 1, the actions specified in the CALL instruction are performed. If P = 0 (PC) ← (PC) + 3	3	9/18	-	-	-	-	-
				B_2												
				B_3												
CP addr	1	1	1	1	0	1	0	0	If S = 0, the actions specified in the CALL instruction are performed. If S = 1 (PC) ← (PC) + 3	3	9/18	-	-	-	-	-
				B_2												
				B_3												

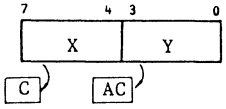
Mnemonic	Instruction Code								Operation	Bytes	States	Flag				
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				C	Z	S	P	AC
CM addr	1	1	1	1	1	1	0	0	If S = 1, the actions specified in the CALL instruction are performed.	3	9/18	-	-	-	-	-
				B_2					If S = 0							
				B_3					(PC) ← (PC) + 3							
RET	1	1	0	0	1	0	0	1	(PCL) ← [(SP)]	1	10	-	-	-	-	-
									(PCH) ← [(SP)+1]							
									(SP) ← (SP) + 2							
RNZ	1	1	0	0	0	0	0	0	If Z = 0, the actions specified in the RET instruction are performed.	1	6/12	-	-	-	-	-
									If Z = 1							
									(PC) ← (PC) + 1							
RZ	1	1	0	0	1	0	0	0	If Z = 1, the actions specified in the RET instruction are performed.	1	6/12	-	-	-	-	-
									If Z = 0							
									(PC) ← (PC) + 1							
RNC	1	1	0	1	0	0	0	0	If C = 0, the actions specified in the RET instruction are performed.	1	6/12	-	-	-	-	-
									If C = 1							
									(PC) ← (PC) + 1							

Mnemonic	Instruction Code								Operation	Bytes	States	Flag				
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				C	Z	S	P	AC
RC	1	1	0	1	1	0	0	0	If C = 1, the actions specified in the RET instruction are performed. If C = 0 (PC) ← (PC) + 1	1	6/12	-	-	-	-	-
RPO	1	1	1	0	0	0	0	0	If P = 0, the actions specified in the RET instruction are performed. If P = 1 (PC) ← (PC) + 1	1	6/12	-	-	-	-	-
RPE	1	1	1	0	1	0	0	0	If P = 1, the actions specified in the RET instruction are performed. If P = 0 (PC) ← (PC) + 1	1	6/12	-	-	-	-	-
RP	1	1	1	1	0	0	0	0	If S = 0, the actions specified in the RET instruction are performed. If S = 1 (PC) ← (PC) + 1	1	6/12	-	-	-	-	-
RM	1	1	1	1	1	0	0	0	If S = 1, the actions specified in the RET instruction are performed. If S = 0 (PC) ← (PC) + 1	1	6/12	-	-	-	-	-

Mnemonic	Instruction Code								Operation	Bytes	States	Flag				
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				C	Z	S	P	AC
PCHL	1	1	1	0	1	0	0	1	(PCH) ← (H) (PCL) ← (L)	1	6	-	-	-	-	-
RST	1	1	A	A	A	1	1	1	[(SP)-1] ← (PCH) [(SP)-2] ← (PCL) (SP) ← (SP) - 2 (PC) ← (00000000 00AAA000)	1	12	-	-	-	-	-

Arithmetic

Mnemonic	Instruction Code								Operation	Bytes	States	Flag				
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				C	Z	S	P	AC
ADD r	1	0	0	0	0	S	S	S	(A) ← (A) + (r)	1	4	0	0	0	0	0
ADC r	1	0	0	0	1	S	S	S	(A) ← (A) + (r) + (C)	1	4	0	0	0	0	0
ADD M	1	0	0	0	0	1	1	0	(A) ← (A)+[(H)(L)]	1	7	0	0	0	0	0
ADC M	1	0	0	0	1	1	1	0	(A)←(A)+[(H)(L)]+(C)	1	7	0	0	0	0	0
ADI d8	1	1	0	0	0	1	1	0 B_2	(A) ← (A) + (B_2)	2	7	0	0	0	0	0
ACI d8	1	1	0	0	1	1	1	0 B_2	(A) ← (A)+(B_2)+(C)	2	7	0	0	0	0	0
DAD rp	0	0	R	P	1	0	0	1	(H)(L) ← (H)(L) + (rH)(rL)	1	10	0	-	-	-	-
SUB r	1	0	0	1	0	S	S	S	(A) ← (A) - (r)	1	4	0	0	0	0	0
SBB r	1	0	0	1	1	S	S	S	(A) ← (A) - (r) - (C)	1	4	0	0	0	0	0
SUB M	1	0	0	1	0	1	1	0	(A) ← (A)-[(H)(L)]	1	7	0	0	0	0	0
SBB M	1	0	0	1	1	1	1	0	(A)←(A)-[(H)(L)]-(C)	1	7	0	0	0	0	0
SUI d8	1	1	0	1	0	1	1	0 B_2	(A) ← (A) - (B_2)	2	7	0	0	0	0	0
SBI d8	1	1	0	1	1	1	1	0 B_2	(A) ← (A) - (B_2) - (C)	2	7	0	0	0	0	0

Mnemonic	Instruction Code								Operation	Bytes	States	Flag				
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				C	Z	S	P	AC
DAA	0	0	1	0	0	1	1	1	The 8-bit number in the accumulator is adjusted to form two 4-bit BCD digits by the following process. Accumulator  1. If $Y \geq 10$ or AC=1, $(A) \leftarrow (A) + 6$ 2. If $X \geq 10$ or C=1, $(A)_{4-7} \leftarrow (A)_{4-7} + 6$	1	4	0	0	0	0	0

Logical Instruction

Mnemonic	Instruction Code								Operation	Bytes	States	Flag				
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				C	Z	S	P	AC
ANA r	1	0	1	0	0	S	S	S	(A) ← (A) ∧ (r)	1	4	R	0	0	0	S
ANA M	1	0	1	0	0	1	1	0	(A) ← (A) ∧ [(H)(L)]	1	7	R	0	0	0	S
ANI d8	1	1	1	0	0	1	1	0	(A) ← (A) ∧ (B_2)	2	7	R	0	0	0	S
					B_2											
XRA r	1	0	1	0	1	S	S	S	(A) ← (A) ∀ (r)	1	4	R	0	0	0	R
XRA M	1	0	1	0	1	1	1	0	(A) ← (A) ∀ [(H)(L)]	1	7	R	0	0	0	R
XRI d8	1	1	1	0	1	1	1	0	(A) ← (A) ∀ (B_2)	2	7	R	0	0	0	R
					B_2											
ORA r	1	0	1	1	0	S	S	S	(A) ← (A) ∨ (r)	1	4	R	0	0	0	R
ORA M	1	0	1	1	0	1	1	0	(A) ← (A) ∨ [(H)(L)]	1	7	R	0	0	0	R
ORI d8	1	1	1	1	0	1	1	0	(A) ← (A) ∨ (B_2)	2	7	R	0	0	0	R
					B_2											
CMP r	1	0	1	1	1	S	S	S	(A) - (r)	1	4	0	0	0	0	0
CMP M	1	0	1	1	1	1	1	0	(A) - [(H)(L)]	1	7	0	0	0	0	0
CPI d8	1	1	1	1	1	1	1	0	(A) - (B_2)	2	7	0	0	0	0	0
					B_2											
CMA	0	0	1	0	1	1	1	1	(A) ← $\overline{(A)}$	1	4	-	-	-	-	-
RLC	0	0	0	0	0	1	1	1	(A_{n+1}) ← (An) (A_0) ← (A_7) (C) ← (A_7)	1	4	0	-	-	-	-
RRC	0	0	0	0	1	1	1	1	(An) ← (A_{n+1}) (A_7) ← (A_0) (C) ← (A_0)	1	4	0	-	-	-	-
RAL	0	0	0	1	0	1	1	1	(A_{n+1}) ← (An) (C) ← (A_7) (A_0) ← (C)	1	4	0	-	-	-	-
RAR	0	0	0	1	1	1	1	1	(An) ← (A_{n+1}) (C) ← (A_0) (A_7) ← (C)	1	4	0	-	-	-	-

Increment and Decrement

Mnemonic	Instruction Code								Operation	Bytes	States	Flag				
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				C	Z	S	P	AC
INR r	0	0	d	d	d	1	0	0	(r) ← (r) + 1	1	4	-	0	0	0	0
INR M	0	0	1	1	0	1	0	0	[(H)(L)] ← [(H)(L)] + 1	1	10	-	0	0	0	0
INX rp	0	0	R	P	0	0	1	1	(rH)(rL) ← (rH)(rL) + 1	1	6	-	-	-	-	-
DCR r	0	0	d	d	d	1	0	1	(r) ← (r) - 1	1	4	-	0	0	0	0
DCR M	0	0	1	1	0	1	0	1	[(H)(L)] ← [(H)(L)] - 1	1	10	-	0	0	0	0
DCX rp	0	0	R	P	1	0	1	1	(rH)(rL) ← (rH)(rL) - 1	1	6	-	-	-	-	-

Stack

Mnemonic	Instruction Code								Operation	Bytes	States	Flag				
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				C	Z	S	P	AC
PUSH rp	1	1	R	P	0	1	0	1	[(SP)-1] ← (rH) [(SP)-2] ← (rL) (SP) → (SP) - 2 Note: Register pair rp=SP may not be specified.	1	12	-	-	-	-	-
PUSH PSW	1	1	1	1	0	1	0	1	[(SP)-1] ← (A) [(SP)-2] ← $D_7D_6D_5D_4D_3D_2D_1D_0$ S Z X AC X P X C MSB (SP) ← (SP) - 2	1	12	-	-	-	-	-
POP rp	1	1	R	P	0	0	0	1	(rL) ← [(SP)] (rH) ← [(SP)+1] (SP) ← (SP)+2	1	10	-	-	-	-	-
POP PSW	1	1	1	1	0	0	0	1	(C) ← [(SP)]$_0$ (P) ← [(SP)]$_2$ (AC) ← [(SP)]$_4$ (Z) ← [(SP)]$_6$ (S) ← [(SP)]$_7$ (A) ← [(SP)+1] (SP) ← (SP) + 2	1	10	0	0	0	0	0

Control

Mnemonic	Instruction Code								Operation	Bytes	States	Flag				
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				C	Z	S	P	AC
HLT	0	1	1	1	0	1	1	0	Halt	1	5	-	-	-	-	-
STC	0	0	1	1	0	1	1	1	(C) ← 1	1	4	0	-	-	-	-
CMC	0	0	1	1	1	1	1	1	(C) ← $(\overline{C})$	1	4	0	-	-	-	-
EI	1	1	1	1	1	0	1	1	Enable interrupts Note: Interrupts are not recognized during the EI instruction.	1	4	-	-	-	-	-
DI	1	1	1	1	0	0	1	1	Disable interrupts Note: Interrupts are not recognized during the DI instruction.	1	4	-	-	-	-	-
NOP	0	0	0	0	0	0	0	0	No operation is performed.	1	4	-	-	-	-	-
RIM	0	0	1	0	0	0	0	0	(A) ← d_7 = SID d_6 = I7 d_5 = I6 d_4 = I5 d_3 = IE d_2 = M7 d_1 = M6 d_0 = M5	1	4	-	-	-	-	-
SIM	0	0	1	1	0	0	0	0	IF$(A)_6$ = 1; SOD ← $(A)_7$,IF$(A)_3$ = 1; M7 ← $(A)_2$ M6 ← $(A)_1$ M5 ← $(A)_0$,IF$(A)_4$ = 1; RST7.5 RESET	1	4	-	-	-	-	-

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Ratings	Units
V_{CC}	Vcc Supply Voltage	-0.5～+7.0	V
V_{IN}	Input Voltage With Respect to V_{SS}	-0.5～+7.0	V
V_{out}	Output Voltage With Respect to V_{SS}	-0.5～+7.0	V
P_D	Power Dissipation	1.5	W
T_{solder}	Soldering Temperature (Soldering Time 10 sec.)	260(10sec)	℃
T_{stg}	Soldering Temperature	-55～150	℃
T_{opr}	Operating Temperature	0～70	℃

DC CHARACTERISTICS

TA=0℃ to 70℃, Vcc=5V±5%

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{IL}	Input Low Voltage		-0.5	0/8	V
V_{IH}	Input High Voltage		2.0	VCC+0.5	V
V_{OL}	Output Low Voltage	IOL=2mA	2		mA
V_{OH}	Output High Voltage	IOH=-400uA		-0.4	mA
I_{CC}	Power Supply Current			170	mA
I_{IL}	Input Leakage	0≦VIN ≦VCC		±10	uA
I_{LO}	Output Leakage	0.45 ≦VOUT≦VCC		±10	uA
V_{ILR}	Input Low Level (RESET)		-0.5	0.8	V
V_{IHR}	Input High Level (RESET)		2.4	VCC+0.5	V
V_{HY}	Hysteresis (RESET)		0.25		V

AC CHARACTERISTICS

TA=0℃ to 70℃, Vcc=5V±5%, Vss=0V, Unless Otherwise Noted.

Symbol	Parameter	TMP8085AP		TMP8085AP-2		Units
		Min.	Max.	Min.	Max.	
t_{CYC}	CLK Cycle Period	320	2000	200	2000	ns
t_L	CLK Low Time - Standard 150pF Loading	80		40		ns
	- Lightly Loaded[2]	100		50		ns
t_H	CLK High Time - Standard 150pF Loding	120		70		ns
	- Lightly Loaded[2]	150		80		ns
$t_{r,tf}$	CLK Rise and Fall Time	30		30		ns
t_{XKR}	X1 Rising to CLK Rising	30	120	30	100	ns
t_{XKF}	X1 Rising to CLK Falling	30	150	30	110	ns
t_{AC}	A8-15 Valid to Leading Edge of Control[1]	270		115		ns
t_{ACL}	A0-7 Valid to Leading of Control	240		115		ns
t_{AD}	A0-15 Valid to Valid Data In		575		350	ns
t_{AFR}	Address Float after Leading Edge of READ (INT)		0		0	ns
t_{AL}	A8-15 Valid before Trailing Edge of ALE[1]	115		50		ns
t_{ALL}	A0-7 Valid before Trailing Edge of ALE	90		50		ns
t_{ARY}	READY Valid from Address Valid		220		100	ns
t_{CA}	Address (A8-15) Valid after Control	120		60		ns
t_{CC}	Width of Control Low(RD, WR, INTA) Edge of ALE	400		230		ns
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	50		25		ns
t_{DW}	Data Valid to trailing Edge of WRITE	420		230		ns
t_{HABE}	HLDA to Bus Enable		210		150	ns
t_{HABF}	Bus Float after HLDA		210		150	ns
t_{HACK}	HLDA Valid to Trailing Edge of CLK	110		40		ns
t_{HDH}	HOLD Hold Time	0		0		ns
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		120		ns
t_{INH}	INTR Hold Time	0		0		ns

Symbol	Parameter	TMP8085AP		TMP8085AP-2		Units
		Min.	Max.	Min.	Max	
t_{INS}	INTR, RST and TRAP Setup Time to Falling Edge of CLK	160		150		ns
t_{LA}	Address Hold Time after ALE	100		50		ns
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	130		60		ns
t_{LCK}	ALE low during CLK High	100		50		ns
t_{LDR}	ALE to Valid Data during Read		460		270	ns
t_{LDW}	ALE to Valid Data during Write	200	120			ns
t_{LL}	ALE Width	140		80		ns
t_{LRY}	ALE to READY Stable		110		30	ns
t_{RAE}	Trailing Edge of READ to Re-Enabling of Address	150		90		ns
t_{RD}	READ (or INTA)to Valid Data		300		150	ns
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	400		220		ns
t_{RDH}	Data Hold Time After READ INTA	0		0		ns
t_{RYH}	READY Hold Time	0		0		ns
t_{RYS}	READY Setup Time to Leading Edge of CLK	110		100		ns
t_{WD}	Data Valid After Trailing Edge of WRITE	100		60		ns
t_{WDI}	LEADING Edge of WRITE to Data Valid		40		20	ns

Test conditions. CL=150p

TMP8085AP : tcYc=320ms

TMP8085AP-2 : tcYc=200ms

Notes: 1. A8-15 address specs apply to IO/M, S0 and S1 except A8-15 are undifined duringT4 - T6 of 0F Cycle whereas IO/M, S0, and S1 are stable.

2. Loading equivalent to 50 pF + 1 TTL input.

3. All timings are measured at output voltage VL = 0 8 V, VH = 2 0V>

4 To calculate timing specifications at other value of t_{CYC} use Table 4.

TABLE 4. BUS TIMING SPECIFICATION AS A T_{CYC} DEPENDENT

t_{AL}	(1/2) T - 45	MIN
t_{LA}	(1/2) T - 60	MIN
t_{LL}	(1/2) T - 20	MIN
t_{LCK}	(1/2) T - 60	MIN
t_{LC}	(1/2) T - 30	MIN
t_{AD}	(5/2 + N) T - 225	MAX
t_{RD}	(3/2 + N) T - 180	MAX
t_{RAE}	(1/2) T - 10	MIN
t_{CA}	(1/2) T - 40	MIN
t_{DW}	(3/2 + N) T - 60	MIN
t_{WD}	(1/2) T - 60	MIN
t_{CC}	(3/2 + N) T - 80	MIN
t_{CL}	(1/2) T - 110	MIN
t_{ARY}	(3/2) T - 260	MAX
t_{HACK}	(1/2) T - 50	MIN
t_{HABF}	(1/2) T + 50	MAX
t_{HABE}	(1/2) T + 50	MAX
t_{AC}	(2/2) T - 50	MIN
t_{L}	(1/2) T - 80	MIN
t_{H}	(1/2) T - 40	MIN
t_{RV}	(3/2) T - 80	MIN
t_{LDR}	(4/2) T - 180	MAX

Note: N is equal to the total WAIT states.

$T = t_{CYC}$

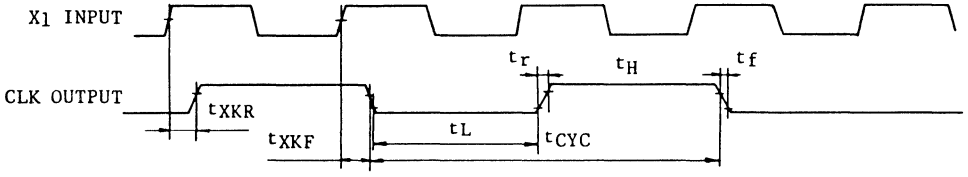


FIGURE 4. CLOCK TIMING WAVEFORM

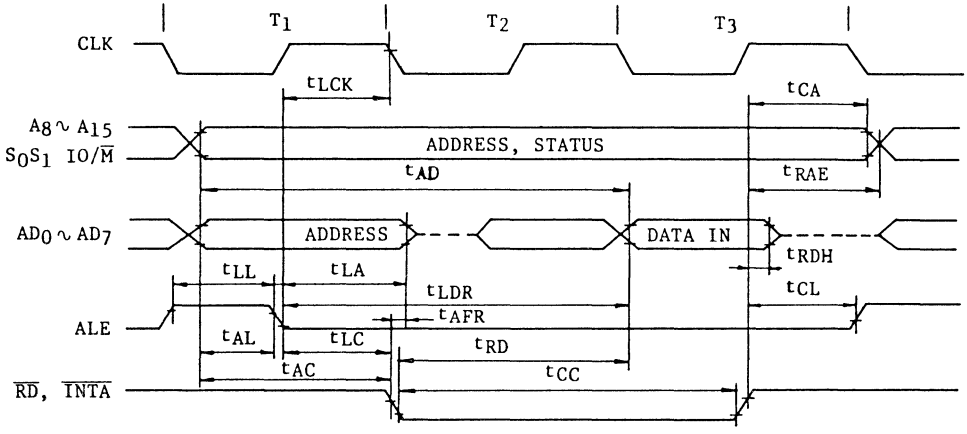


FIGURE 5. READ OPERATION

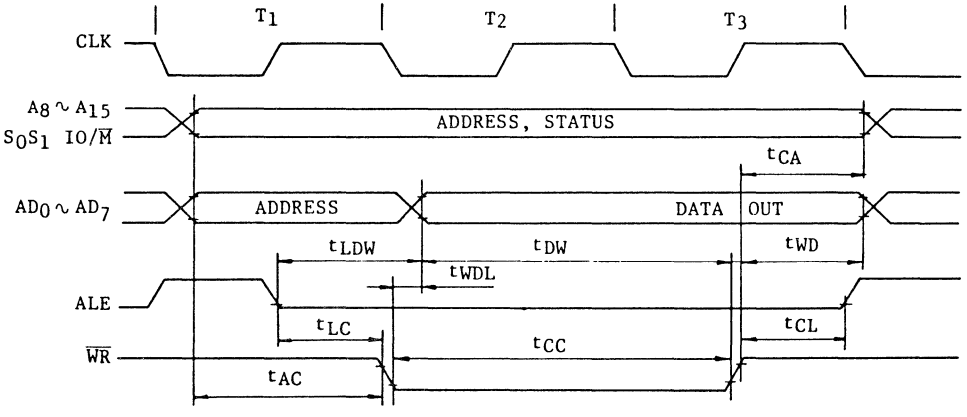


FIGURE 6. WRITE OPERATION

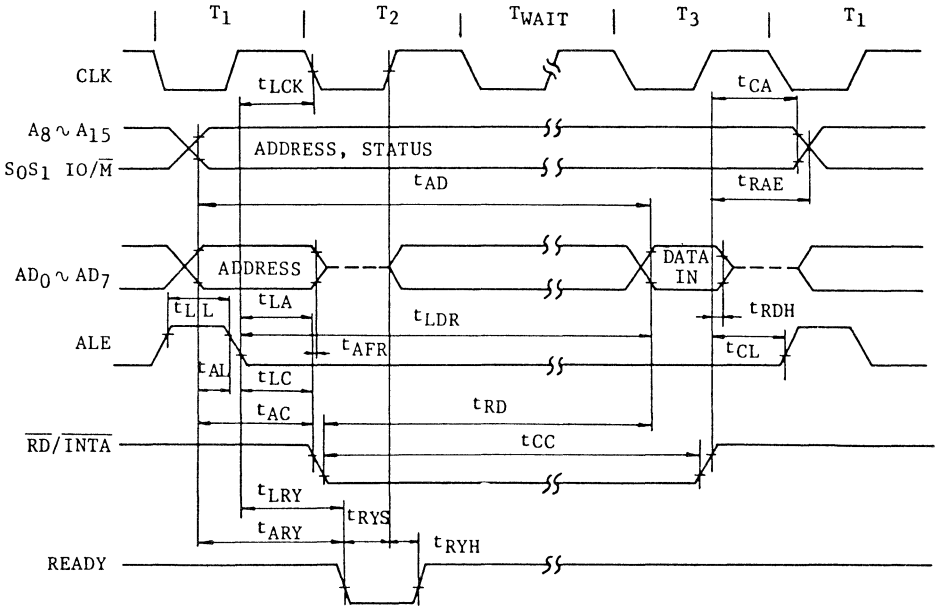


FIGURE 7. READ OPERATION WITH WAIT CYCLE (TYPICAL)
- SAME READY TIMING APPLIES TO WRITE OPERATION

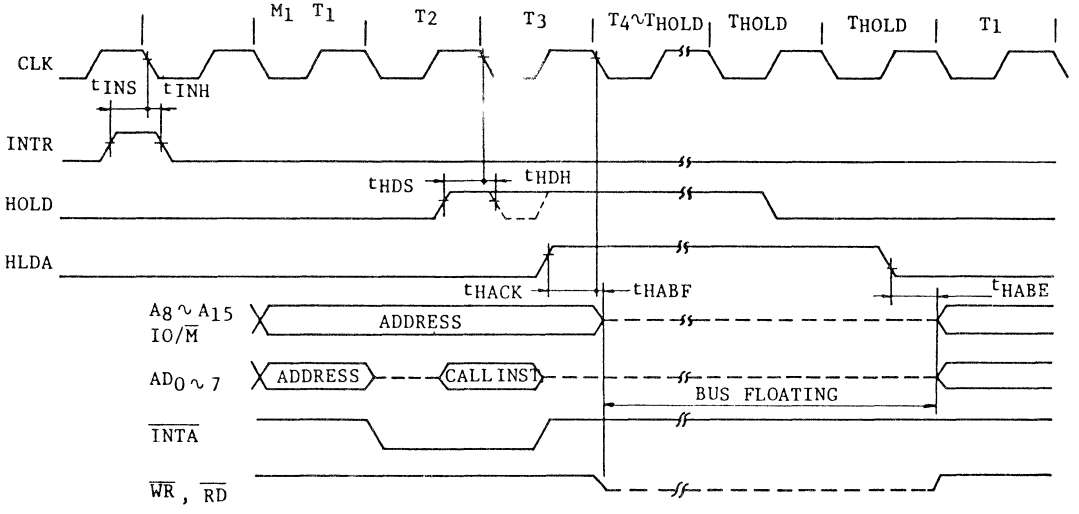
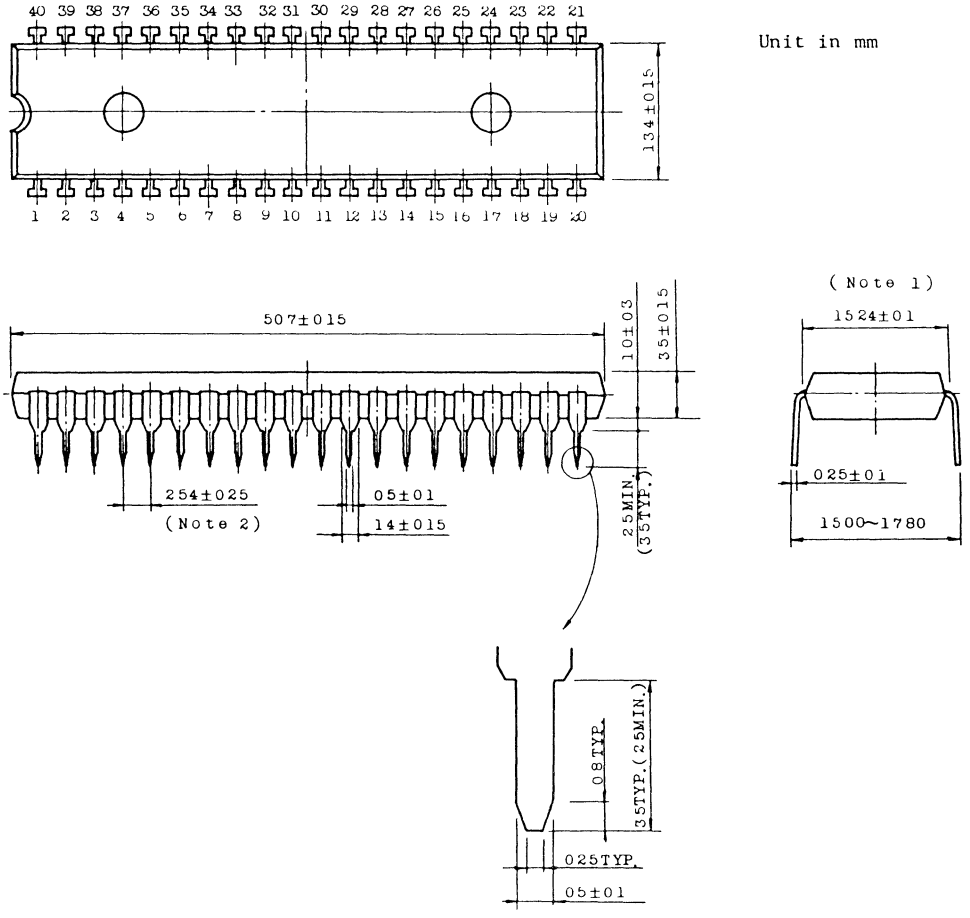


FIGURE 8. INTERRUPT AND HOLD TIMING

OUTLINE DRAWING

Unit in mm



Note: 1. This dimension is measured at the center of bending point of leads.

2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoritical positions with respect to No.1 and No.40 leads.

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT
N-CHANNEL SILICON GATE MOS

8-BIT SINGLE CHIP MICROPROCESSOR

GENERAL DESCRIPTION

The TMP8085AHP/AHP-2, from here on referred to as the TMP8085A, is world standard, complete 8 bit parallel central processing unit (CPU). Its high level of system integration allows a minimum system of there IC's : TMP8085A (CPU), TMP8155P/TMP8156P (RAM/IO) and TMP8355P (ROM/IO). The TMP8085A uses a multiplexed data bus. The address is plit between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of TMP8155P/TMP8156P/TMP8355P memory products allow a direct interface with TMP8085A.

FEATURES

- 0.8uSec Instruction Cycle (TMP8085AHP-2 : CLK Cycle Period @200nSec)
- Single +5V Power Supply (5V±10%)
- On-Chip Clock Generator (with External Crystal or RC Network)
- On-Chip System Controller; Advanced Cycle status information available for Large System Control
- 4 Vectored Interrupts (One is Non-Maskable)
- Decimal, Binary and Double Precision Arithmetic
- Serial In/Serial Out Port
- Direct Addressing Capability to 64K Bytes of Memory
- Low Power Consumption (Icc max = 135mA)

PIN CONNECTION
(TOP VIEW)

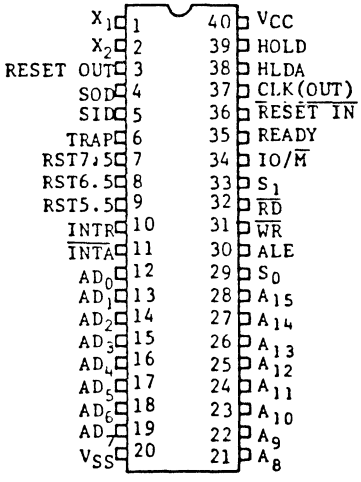


FIGURE 2. TMP8085A PINOUT DIAGRAM

BLOCK DIAGRAM

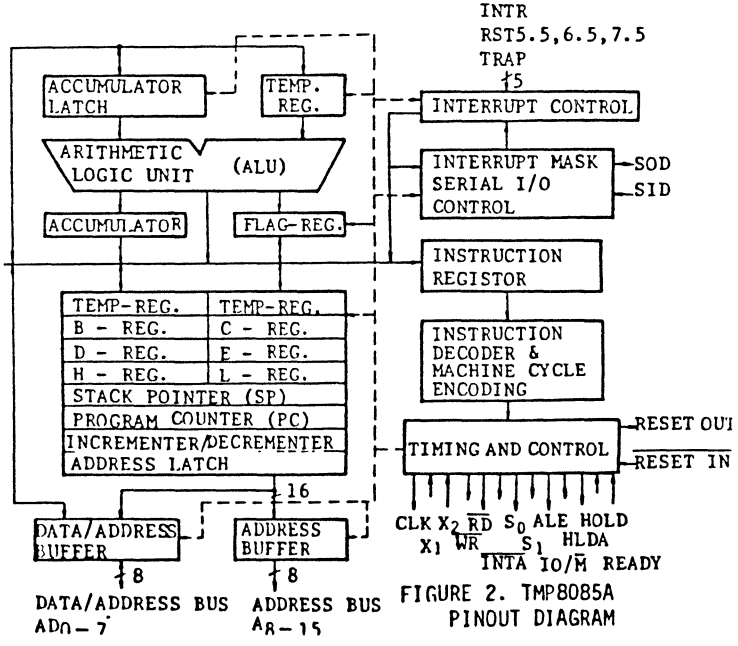


FIGURE 2. TMP8085A PINOUT DIAGRAM

DRIVING THE X1 and X2 INPUTS

You may drive the clock inputs of the TMP8085A with a crystal, an LC turned circuit, an RC network or an external clock source. The driving frequency must be at least 1 MHz, and must be twice the desired internal clock frequency.

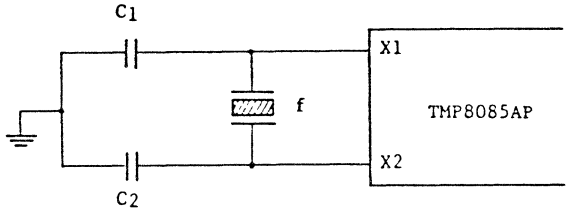
A. Quartz Crystal Clock Driver

If a crystal used, it must have the following characteristics.

. Parallel resonance at twice the clock frequency desired.

. C_S (shunt capacitance) $\leq$ 7 PF

. R_S (equivalent shunt resistance) $\leq$ 75 ohms



Note a value of the external capacitance C1 and C2 between X1, X2 and ground.

We recommended the following.

1MHz $\leq$ f < 4MHz: C_1=20pF, C_2=20pF

4MHz $\leq$ f $\leq$ 8MHz: C_1=10pF, C_2=10pF

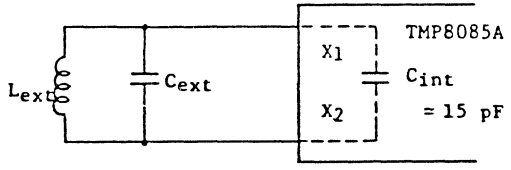
8MHz $\leq$ f < 10MHz: C_1=0, C_2=0

B LC Turned Circuit Clock Driver

A parallel-resonant LC circuit may be used as the frequency-determining network for the TMP8085A, providing that its frequency tolerance of aproximately 10% is acceptable. The components are chosen from the formula.

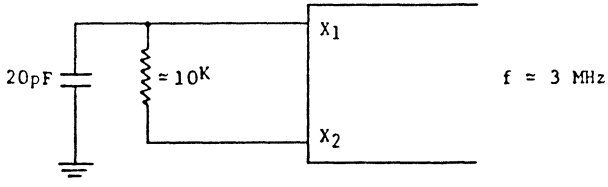
$$f = \frac{1}{2\pi \sqrt{L\,(C_{ext} + C_{int})}}$$

The use of an LC circuit is not recommended for frequencies higher than approximately 5 MHz.

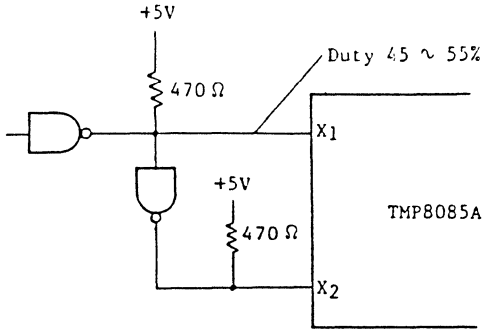


C. RC Circuit Clock Driver

An RC circuit may be used as the frequency - determining network for the TMP8085A if maintaining a precise clock frequency is of no importance. Variations in the on-chip timing generation can cause a wide variation in frequency when using RC circuit. The driving frequency generated by the circuit shown is approximately 3 MHz. It is not recommended that frequencies greatly higher or lower than this be attempted.



D. External Clock Driver Circuit



POWER ON AND $\overline{\text{RESET IN}}$

The TMP8085A is not guaranteed to work until 10 ms after VCC reaches 4.50V. It is suggested that $\overline{\text{RESET IN}}$ be kept low during this period. Note that the 10 ms period does not include the time it takes for the power supply to reach its 4.50V level.

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Ratings	Units
VCC	VCC Supply voltage	-0.5 to +7.0	V
VIN	Input Voltage with Respect to VSS	-0.5 to +7.0	V
Vout	Output Voltage with Respect to VSS	-0.5 to +7.0	V
PD	Power Dissipation	1.5	W
Tsolder	Soldering Temperature	260 (10 sec)	C
Tstg	Storage Temperature	-65 to 150	C
Topr	Operating Temperature	0 to 70	C

DC CHARACTERISTICS

T_A=0°C to 70°C, VCC=5V±10%

Symbol	Parameter	Test Conditions	Min.	Max.	Units
VIL	Input Low Voltage		-0.5	0/8	V
VIH	Input High Voltage		2.0	VCC+0.5	V
VOL	Output Low Voltage	IOL=2mA		0.45	V
VOH	Output High Voltage	IOH=-400uA	2.4		V
ICC	Power Supply Current			135	mA
IIL	Input Leakage	$0 \leqq VIN \leqq VCC$		±10	uA
ILO	Output Leakage	$0.45 \leqq VOUT \leqq VCC$		±10	uA
VILR	Input Low Level (RESET)		-0.5	0.8	V
VIHR	Input High Level(RESET)		2.4	VCC+0.5	V
VHY	Hysteresis (RESET)		0.25		V

AC CHARACTERISTICS

T_A=0°C to 70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted.

Symbol	Parameter	TMP8085AHP		TMP8085AHP-2		Units
		Min.	Max.	Min.	Max.	
tCYC	CLK Cycle Period	320	2000	200	2000	ns
tL	CLK Low Time - Standard 150pF Loading	80		40		ns
	- Lightly Loaded [2]	100		50		ns
tH	CLK High Time- Standard 150pF Loading	120		70		ns
	- Lightly Loaded [2]	150		80		ns
tr,tf	CLK Rise and Fall Time		30		30	ns
tXKR	X1 Rising to CLK Rising	30	120	30	100	ns
tXKF	X1 Rising to CLK Falling	30	150	30	110	ns
tAC	A8-15 Valid to Leading Edge of Control [1]	270		115		ns
tACL	A0-7 Valid to Leading of Control	240		115		ns
tAD	A0-15 Valid to Valid Data In		575		350	ns
tAFR	Address Float after Leading Edge of READ (INT)		0		0	ns
tAL	A8-15 Valid before Trailing Edge of ALE[1]	115		50		ns
tALL	A0-7 Valid before Trailing Edge of ALE	90		50		ns
tARY	READY Valid from Address Valid		220		100	ns
tCA	Address (A8-15) Valid after Control	120		60		ns
tCC	Width of Control Low (RD,WR,INTA)	400		230		ns
	Edge of ALE					
tCL	Trailing Edge of Control to Leading	50		25		ns
	Edge of ALE					
tDW	Data Valid to Trailing Edge of WRITE	420		230		ns
tHABF	HLDA to Bus Enable		210		150	ns
tHABF	Bus Float after HLDA		210		150	ns
tHACK	HLDA Valid to Trailing Edge of CLK	110		40		ns
tHDH	HOLD Hold Time	0		0		ns
tHDS	HOLD Setup Time to Trailing Edge of	170		120		ns
	CLK					
tINH	INTR Hold Time	0		0		ns
tINS	INTR, RST and TRAP Setup Time to	160		150		ns
	Falling					
	Edge of CLK					
tLA	Address Hold Time after ALE	100		50		ns
tLC	Trailing Edge of ALE to Leading Edge	130		60		ns
	of Control					
tLCK	ALE Low during CLK High	100		50		ns
tLDR	ALE to Valid Data during Read		460		270	ns
tLDW	ALE to Valid Data during Write		200		120	ns
tLL	ALE Width	140		80		ns
tLRY	ALE to READY Stable		110		30	ns
tRAE	Trailing Edge of READ to Re-Enabling	150		90		ns
	of Address					
tRD	READ (or INTA) to Valid Data		300		150	ns

Symbol	Parameter	TMP8085AHP		TMP8085AHP-2		Units
		Min.	Max.	Min.	Max.	
tRV	Control Trailing Edge of Leading Edge of Next Control	400		220		ns
tRDH	Data Hold Time After READ INTA	0		0		ns
tRYH	READY Hold Time	0		0		ns
tRYS	READY Setup Time to Leading Edge of CLK	110		100		ns
tWD	Data Valid After Trailing Edge of WRITE	100		60		ns
tWDL	LEADING Edge of WRITE to Data Valid		40		20	ns

Test conditions CL=150pF

TMP8085AP : tCYC = 320ns
TMP8085AP-2 : tCYC = 200ns

Notes: 1. A8-15 address specs apply to IO/M, S0 and S1 except A8-15 are undifiend during T4 - T6 of Cycle whereas IO/M, S0, and S1 are stable.

2. Loading equivalent to 50pF + 1 TTL input.

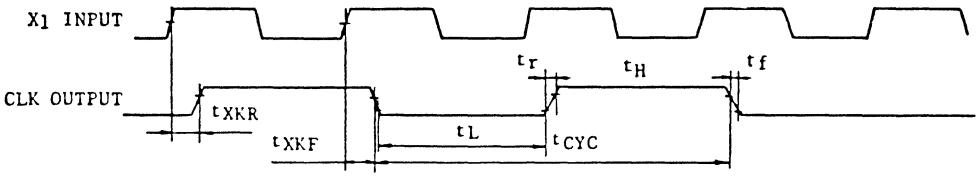
3. All timings are measured at output voltage VL=0.8V, VH=2.0V

4. To calculate timing specifications at other value of tCYC use Table 4.

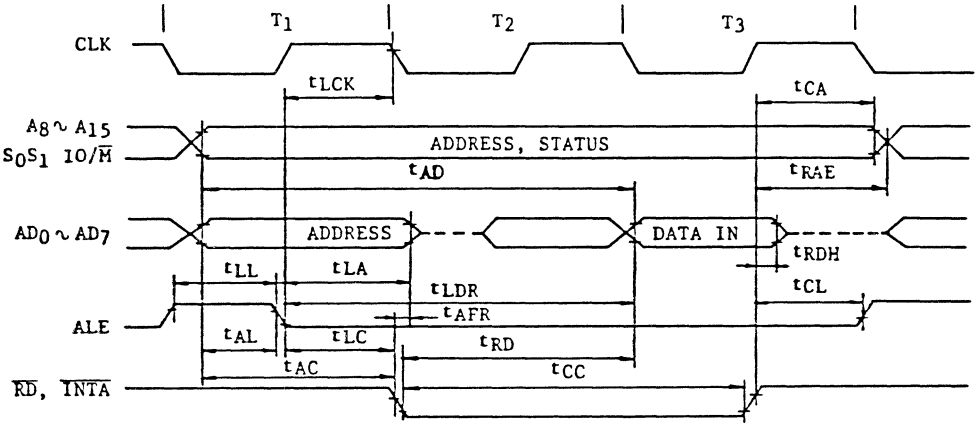
Table 4. Bus Timing Specification as a TCYC Dependent

tAL	(1/2) T-45	MIN
tLA	(1/2) T-60	MIN
tLL	(1/2) T-20	MIN
tLCK	(1/2) T-60	MIN
tLC	(1/2) T-30	MIN
tAD	(5/2+N) T-225	MAX
tRD	(3/2+N) T-180	MAX
tRAE	(1/2) T-10	MIN
tCA	(1/2) T-40	MIN
tDW	(3/2+N) T-60	MIN
tWD	(1/2) T-60	MIN
tCC	(3/2+N) T-80	MIN
tCL	(1/2) T-110	MIN
tARY	(3/2) T-260	MAX
tHACK	(1/2) T-50	MIN
tHABF	(1/2) T+50	MAX
tHABE	(1/2) T+50	MAX
tAC	(2/2) T-50	MIN
tL	(1/2) T-80	MIN
tH	(1/2) T-40	MIN
tRV	(3/2) T-80	MIN
tLDR	(4/2) T-180	MAX

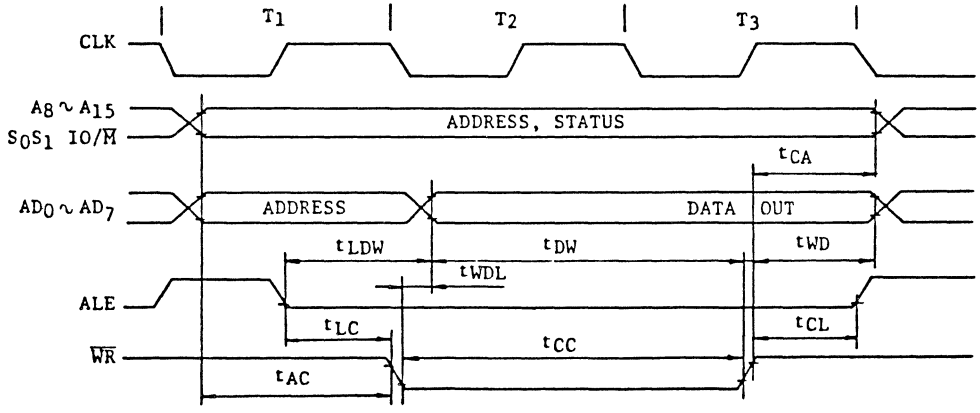
Note: N is equal to the total WAIT states.
T=tCYC



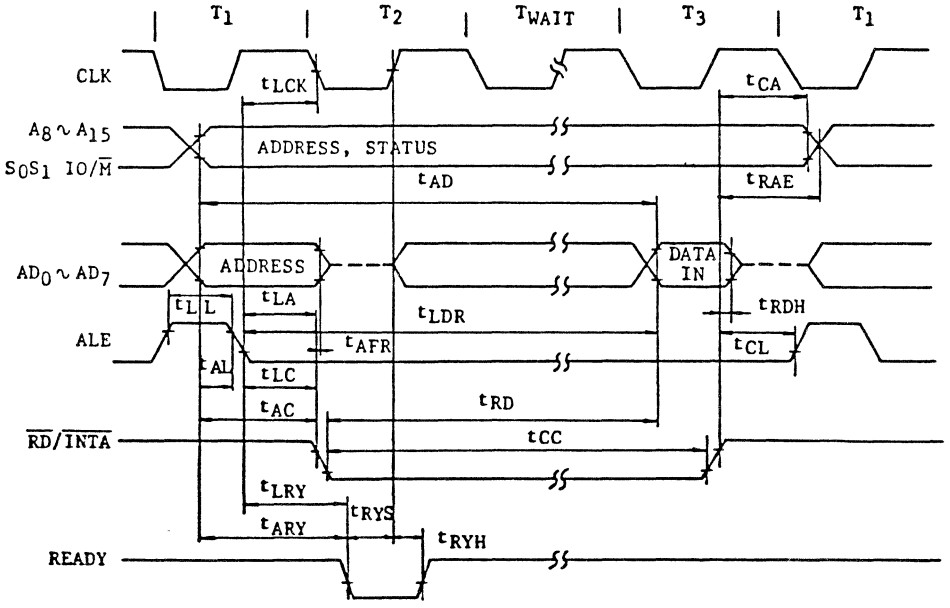
CLOCK TIMING WAVEFORM



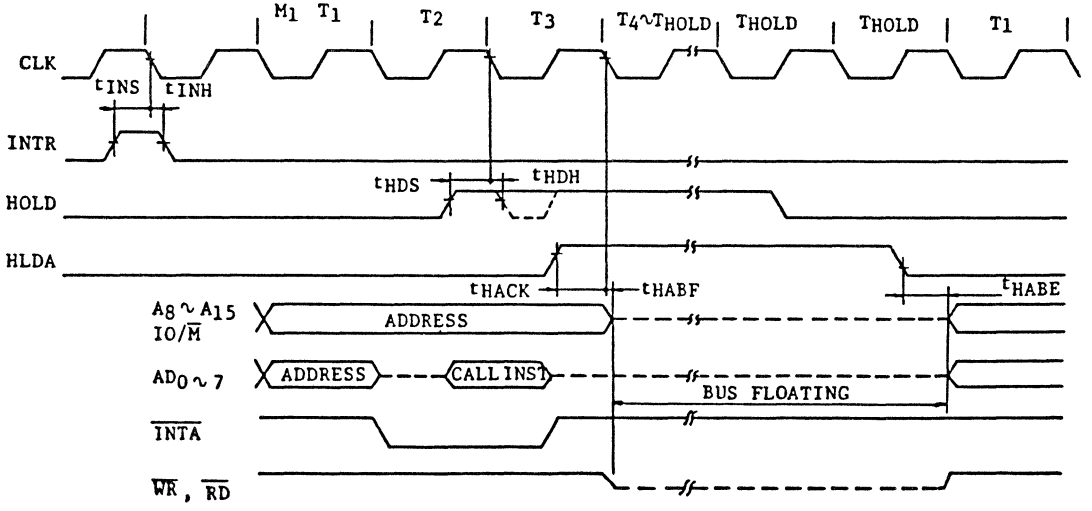
READ OPERATION



WRITE OPERATION

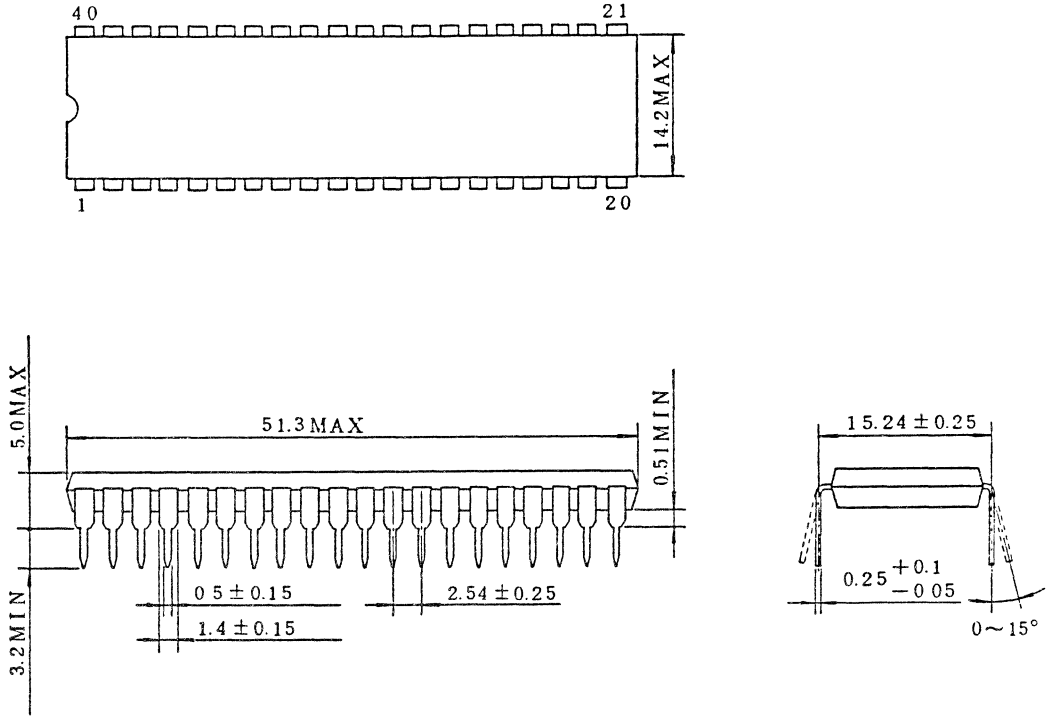


READ OPERATION WITH WAIT CYCLE (TYPICAL)
- SAME READY TIMING APPLIES TO WRITE OPERATION



INTERRUPT AND HOLD TIMING

単位 mm



Note: Each lead pitch is 2.54mm, and all the leads are located within ±0.25 mm from their theoretical positions with respect to No.1 and No.40 leads.

2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

GENERAL DESCRIPTION

The TMP 8155P/8156P are RAM including I/O ports and counter/timer on the chip for using in the TLCS-85A microcomputer system. The RAM portion is designed with 2K bit static cells organized as 256 x 8. The 14 bit programmable counter/timer is the down counter. It provides either a square wave or terminal count pulse for the cpu system depending on timer mode.

The I/O portion is consists of 2 programmable 8 bit I/O ports and 1 programmable 6 bit I/O port. The programmable I/O ports can be operated by BASIC MODE and STROBE MODE.

FEATURES

- Single +5V Power Supply
- Access Time: 330 ns (TMP8155-2/TMP8156-2)
- Internal Address Latch
- 2 Programmable 8 Bit I/O Ports and 1 Programmable 6 Bit I/O Port.
- 256 Ward x 8 Bits RAM
- Programmable 14 Bit Binary Counter/Timer
- Multiplexed Address and Data Bus
- Chip Enable Active High (TMP8156P) or Low (TMP8155P)
- 40 pin DIP

PIN CONNECTION (TOP VIEW)

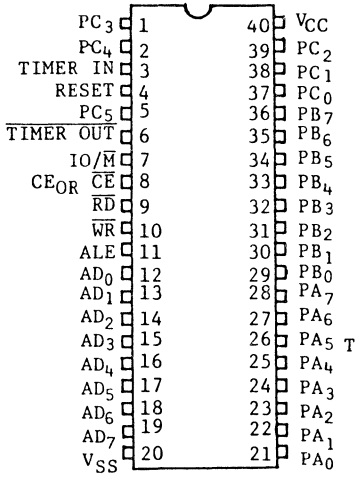


FIGURE 1 TMP8155P/8156P PINOUT DIAGRAM

BLOCK DIAGRAM

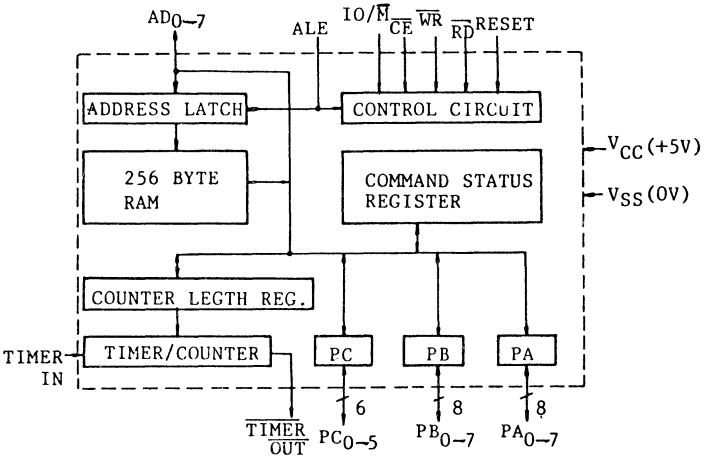


FIGURE 2 TMP8155P/8156P FUNCTIONAL BLOCK DIAGRAM

PIN NAMES AND PIN DESCRIPTION

RESET (INPUT)

The Reset signal is a pulse provided by the TMP8085A to initialize the system. Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two TMP8085A clock cycle times.

$AD_{0\sim7}$ (INPUT / OUTPUT, 3-STATE)

These are 3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latche on the falling edge of the ALE. The address can be applied to the memory section or the I/O section depending on the polarity of the IO/$\overline{M}$ input signal. The 8-bit data is either written into the chip or read from the chip depending on the status of $\overline{WR}$ or $\overline{RD}$ input signal.

CE OR $\overline{CE}$ (INPUT)

Chip Enable: On the TMP8155P, this pin is $\overline{CE}$ and is ACTIVE LOW.
On the TMP8156P, this pin is CE and is ACTIVE HIGH.

$\overline{RD}$ (INPUT)

Input low on this line with the Chip Enable active enables the $AD_{0\sim7}$ buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status register will be read to the AD bus.

$\overline{WR}$ (INPUT)

Input low on this line with the Chip Enable active causes the data on the AD lines to be written to the RAM or I/O ports and command/status register depending on the polarity of IO/$\overline{M}$.

ALE (INPUT)

Address Latch Enable: This control signal latches both the address on the $AD_{0\sim7}$ lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.

IO/$\overline{M}$ (INPUT)

IO/$\overline{\text{Memory}}$ Select: This line selects the memory if low and selects the I/O and command/status register if high.

$PA_{0\sim7}$ (INPUT/OUTPUT, 3-STATE)

These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command Register.

PB0~7 (INPUT/OUTPUT, 3-STATE)

These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command Register.

PC0~5 (INPUT/OUTPUT, 3-STATE)

These 6 pins can function as either input port, output port, or as control signal for PA and PB. Programming is done through the Command Register.

When $PC_{0\sim5}$ are used as control signals, they are defined the following:

PC_0 - A INTR (Port A Interrupt)

PC_1 - A BF (Port A Buffer Full)

PC_2 - A $\overline{STB}$ (Port A Strobe)

PC_3 - B INTR (Port B Interrupt)

PC_4 - B BF (Port B Buffer Full)

PC_5 - B $\overline{STB}$ (Port B Strobe)

TIMER IN (INPUT)

This is the input to the counter-timer.

$\overline{\text{TIMER OUT}}$ (OUTPUT)

This pin is the timer output. This output can be either a square wave or a pulse depending on the timer mode.

V_{CC} (Power)
+5 volt supply

V_{SS} (Power)
Ground Reference

FUNCTIONAL DESCRIPTION

PROGRAMMING OF THE COMMAND REGISTER

The command register consists of eitht latches. Four bits (0-3) define the mode of the ports, two bits (4-5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6-7) are for the timer.

The command register contents can be altered at any time by using the I/O address XXXX000 during a WRITE operation. The function of each bit of the command byte is defined in FUGURE 3.

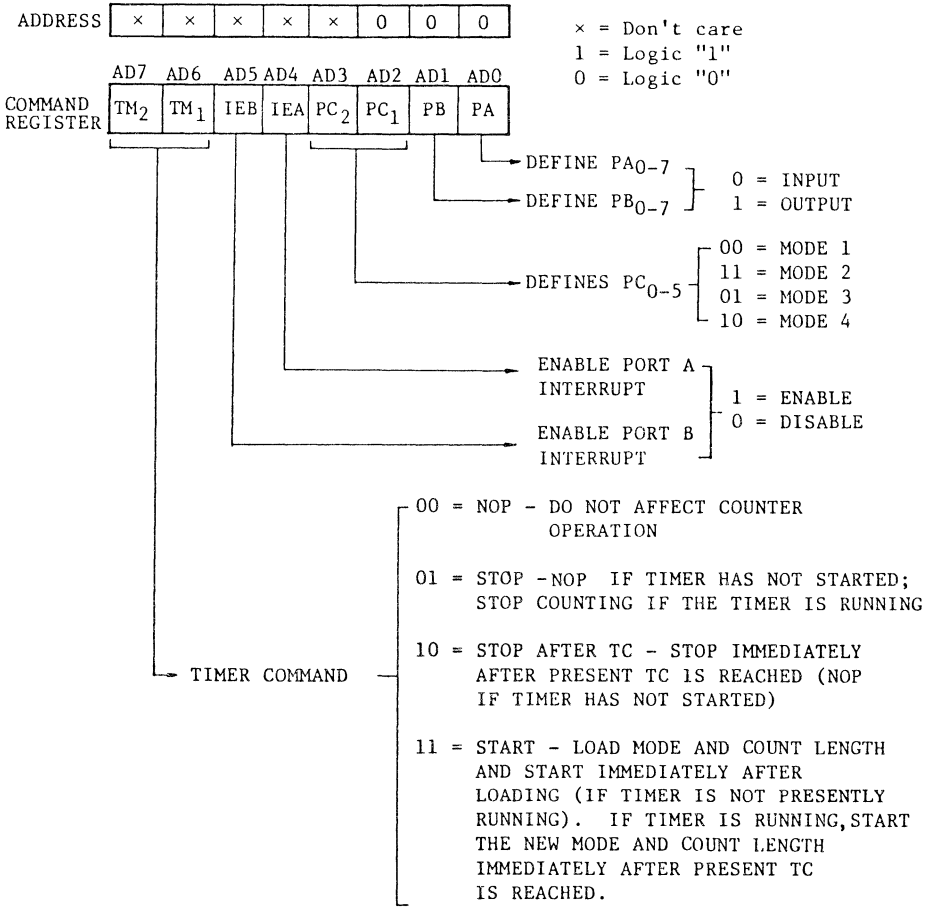


FIGURE 3 COMMAND REGISTER BIT ASSIGNMENT

READING THE STATUS REGISTER

The status register consists of seven latches, one for each bit; six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the Status Register (Address XXXXX000). Status word format is shown in FIGURE 4.

Note that you may never write to the status register since the command register shares the same I/O address and the command register is selected when a write to that address is issued.

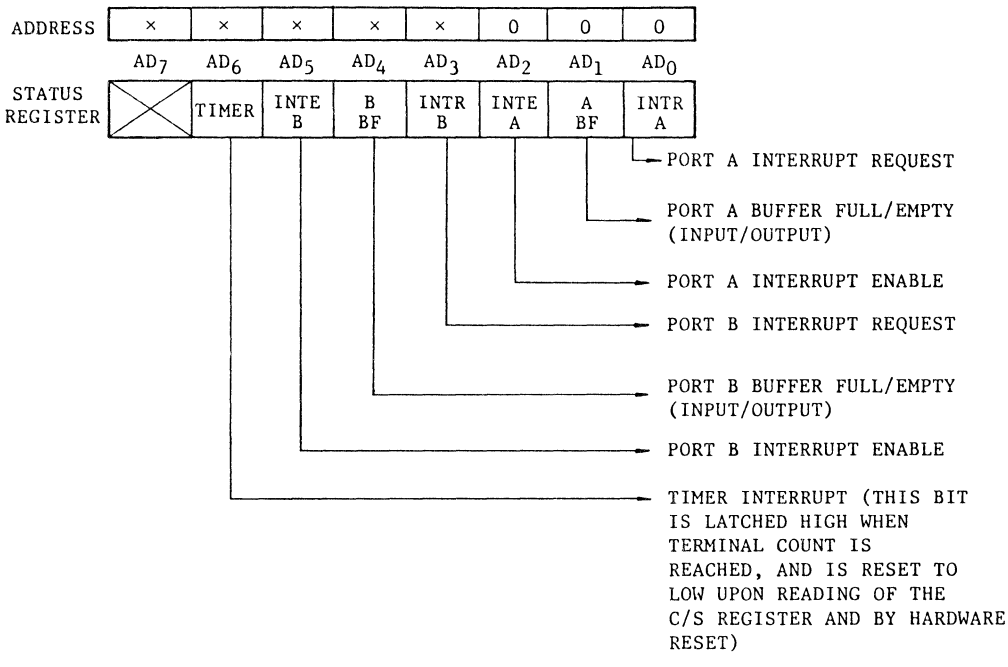


FIGURE 4 STATUS REGISTER BIT ASSIGNMENT

INPUT/OUTPUT SECTION

COMMAND/STATUS REGISTER (C/S)

Both register have the common address ×××××000. When the C/S registers are selected during WRITE operation, a command is written into the C/S register. The contents of this register are not accessible through the pins. When the C/S is selected during a READ operation, the status information of the I/O ports and the timer becomes available on the AD_{0-7} lines.

- PA Register — This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register. Also depending on the command, this port can operate in either the basic mode or the strobed mode (See timing diagram). The I/O pins assigned in relation to this register are PA_{0-7}. The address of this register is XXXXX001.

- PB Register — This register functions the same as PA Register. The I/O pins assigned are PB_{0-7}. The address of this register is XXXXX010.

- PC Register — This register has the address XXXXX011 and contains only 6-bits. The 6-bits can be programmed to be either input ports, output ports or as control signals for PA and PB by properly programming the AD_2 and AD_3 bits of the C/S register.

When PC_{0-5} is used as a control port, 3-bits are assigned for Port A and 3 for Port B. The first bit is an interrupt that the TMP8155P/8156P issues.

The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. See Table 2.

When the port C is programmed to either MODE 3 or MODE 4, the control signals for PA and PB are initialized as follows:

MODE \ CONTROL	BF	INTR	$\overline{STB}$
INPUT MODE	Low	Low	Input Control
OUTPUT MODE	Low	High	Input Control

To summarize, the register's assignments are shown TABLE 1.

TABLE 1 I/O PORT ADDRESSING SCHEME

I/O ADDRESS								PINOUTS	SELECTION	NO. OF BITS
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0			
X	X	X	X	X	0	0	0	Internal	Command/Status Register	8
X	X	X	X	X	0	0	1	PA_{0-7}	General Purpose I/O Port A	8
X	X	X	X	X	0	1	0	PB_{0-7}	General Purpose I/O Port B	8
X	X	X	X	X	0	1	1	PC_{0-7}	General Purpose I/O Port or Control	6
X	X	X	X	X	1	0	0		Low-Order 8 bits of Timer Count	
X	X	X	X	X	1	0	1		High 6 bits/2 bits of Timer Count	

TABLE 2 TABLE OF PORT CONTROL ASSIGNMENT

Pin	MODE 1	MODE 2	MODE 3	MODE 4
PC0	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A $\overline{STB}$ (Port A strobe)	A $\overline{STB}$ (Port A Strobe)
PC3	Input Port	Output Port	Output Port	B INTR (Port B Interrupt)
PC4	Input Port	Output Port	Output Port	B BF (Port B Buffer Full)
PC5	Input Port	Output Port	Output Port	B $\overline{STB}$ (Port B Strobe)

TIMER SECTION

The timer is a 14-bit down-counter that counts the 'timer input' pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register.

To program the timer, the COUNT LENGTH REGISTER is loaded first, one byte at a time, by selecting the timer addresses. Bits 0-13 will specify the length of the next count and bits 14-15 will specify the timer output mode. The value loaded into the count length register can have any value from 2_H through $3FFF_H$ in bits 0-13.

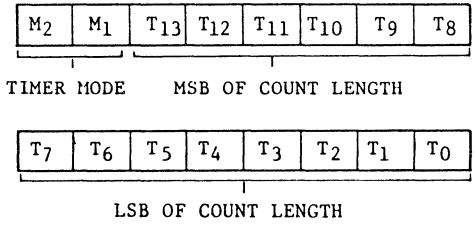


FIGURE 5 TIMER FROMAT

There are four timer modes which are defined by M2 and M1.

M2	M1	
0	0	——— Put out low during second half of count.
0	1	——— Continuous square wave; The period of the square-wave equals the count length programmed with automatic reload at terminal count.
1	0	——— Single pulse upon TC being reached.
1	1	——— Continuous pulses.

Note: In case of an odd-numbered count, the first half-cycle of the square-wave output, which is high, is one count longer than the second (low) half-cycle as shown in FIGURE 6.

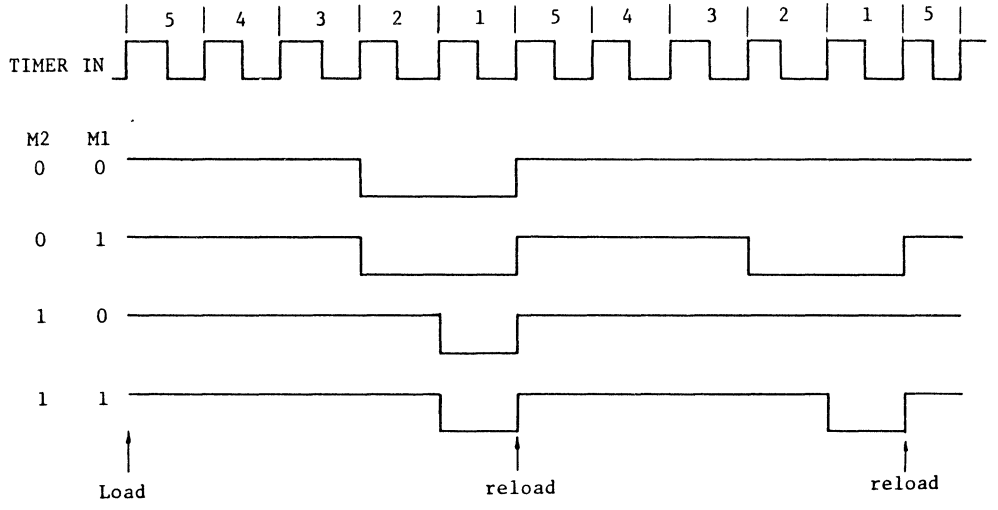


FIGURE 6 ASYMMETRICAL SQUARE-WAVE OUTPUT RESULTING FROM COUNT OF 5

Bits 6-7 (TM2 and TM1) of command register contents are used to start and stop the counter. There are four commands to choose from;

TM2	TM1	
0	0	NOP: Do not affect counter operation.
0	1	STOP: NOP if timer has not started; stop counting if the timer is running.
1	0	STOP AFTER TC: Stop immediately after present TC is reached. (NOP if timer has not started)
1	1	START: Load mode and count length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and count length immediately after present TC is reached.

Note that while the counter is counting, you may load a new count and mode into the count length registers. Before the new count and mode will be used by the counter, you must issue a START command to the counter. This applies even though you may only want to change the count and use the previous mode.

The counter in the TMP8155P/8156P is not initialized to any particular mode or count when hardware RESET occurs, but RESET does stop the counting. Therefore you must issue a START command via the C/S register, because counting cannot begin following RESET.

Please note that the timer circuit on the TMP8155P/8156P chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by twos twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. You cannot load an initial value of 1 into the count register and cause the timer to operate, as its terminal count value is 10 (binary). After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses required to complete the timer cycle if desired. To obtain the remaining count, perform the following operations in order:

1. Stop the count.
2. Read in the 16-bit value from the count length registers.
3. Reset the upper two mode bits.
4. Reset the carry and rotate right one position all 16 bits through carry.
5. If carry is set, add 1/2 of the full original count (1/2 full count-1 if full count is odd.)

Note: If you started with an odd count and you read the count length register before the third count pulse occurs, you will not be able to discern whether one or two counts has occurred. Regardless of this, the TMP8155P/8156P always counts out the right number of pulses in generating the $\overline{\text{TIMER OUT}}$ waveforms.

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating
V_{CC}	V_{CC} Supply Voltage with Respect to V_{SS}	-0.5V to +7.0V
V_{IN}	Input Voltage with Respect to V_{SS}	-0.5V to +7.0V
V_{OUT}	Output Voltage with Respect to V_{SS}	-0.5V to +7.0V
P_D	Power Dissipation	1.5W
T_{SOLDER}	Soldering Temperature (Soldering Time 10 sec.)	260°C
T_{STG}	Storage Temperature	-55°C to +150°C
T_{OPR}	Operating Temperature	0°C to +70°C

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}+0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -400μA	2.4			V
I_{IL}	Input Leakage	V_{IN} = V_{CC} to 0V			±10	μA
I_{LO}	Output Leakage Current	0.45V ≤ V_{OUT} ≤ V_{CC}			±10	μA
I_{CC}	V_{CC} Supply Current				180	mA
$I_{IL(CE)}$	Chip Enable Leakage 8155 8156	V_{IN} = V_{CC} to 0V.			 +100 -100	 μA μA

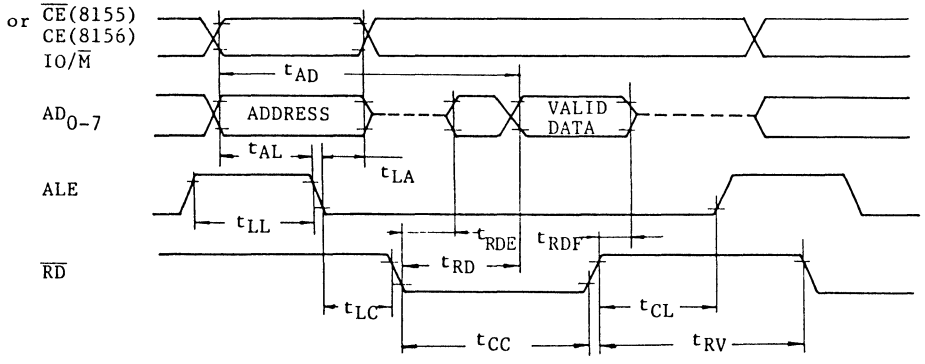
A.C. CHARACTERISTICS

T_A=0°C to +70°C, V_{CC}=+5V±5%

Symbol	Parameters	Test Condition	TMP8155P/56P		TMP8155P-2/56P-2		Units
			Min.	Max.	Min.	Max.	
t_{AL}	Address to Latch Setup Time	150pF Load	50		30		ns
t_{LA}	Address Hold Time after Latch		80		30		ns
t_{LC}	Latch to READ/WRITE Control		100		40		ns
t_{RD}	Valid Data out Delay from READ Control			170		140	ns
t_{AD}	Address Stable to Data Out Valid			400		330	ns
t_{LL}	Latch Enable Width		100		70		ns
t_{RDF}	Data Bus Float after READ		0	100	0	80	ns
t_{CL}	READ/WRITE Control Latch Enable		20		10		ns
t_{CC}	READ/WRITE Control Width		250		200		ns
t_{DW}	Data In to WRITE Setup Time		150		100		ns
t_{WD}	Data in Hold Time After WRITE		0		25		ns
t_{RV}	Recovery Time Between Controls		300		200		ns
t_{WP}	WRITE to Port Output			400		300	ns
t_{PR}	Port Input Setup Time		70		50		ns
t_{RP}	Port Input Hold Time		50		10		ns
t_{SBF}	Strobe to Buffer Full			400		300	ns
t_{SS}	Strobe Width		200		150		ns
t_{RBE}	READ to Buffer Empty			400		300	ns
t_{SI}	Strobe to INTR On			400		300	ns
t_{RDI}	READ to INTR Off			400		300	ns
t_{PSS}	Port Setup Time to Strobe		50		20		ns
t_{PHS}	Port Hold Time After Strobe		120		100		ns
t_{SBE}	Strobe to Buffer Empty			400		300	ns
t_{WBF}	WRITE to Buffer Full			400		300	ns
t_{WI}	WRITE to INTR Off			400		300	ns
t_{TL}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low			400		300	ns
t_{TH}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ High			400		300	ns
t_{RDE}	Data Bus Enable from READ Control		10		10		ns
t_L	TIMER-IN Low Time		80		40		ns
t_H	TIMER-IN High Time		120		70		ns

TIMING WAVEFORMS

A. READ CYCLE



B. WRITE CYCLE

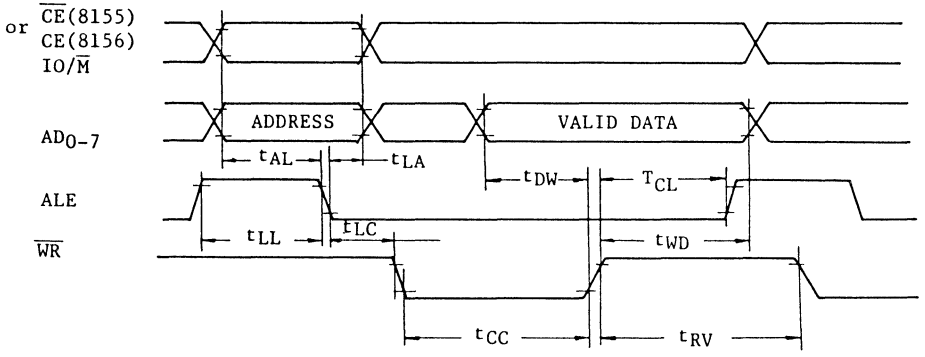
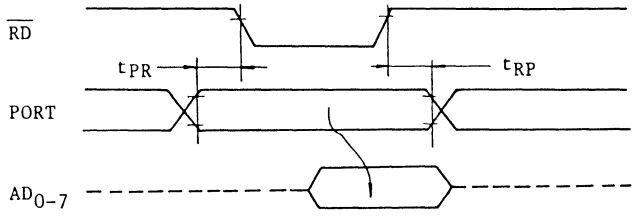


FIGURE 7 READ/WRITE TIMING DIAGRAMS

A. BASIC INPUT MODE



B. BASIC OUTPUT MODE

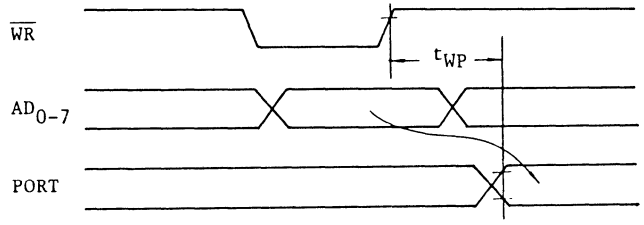
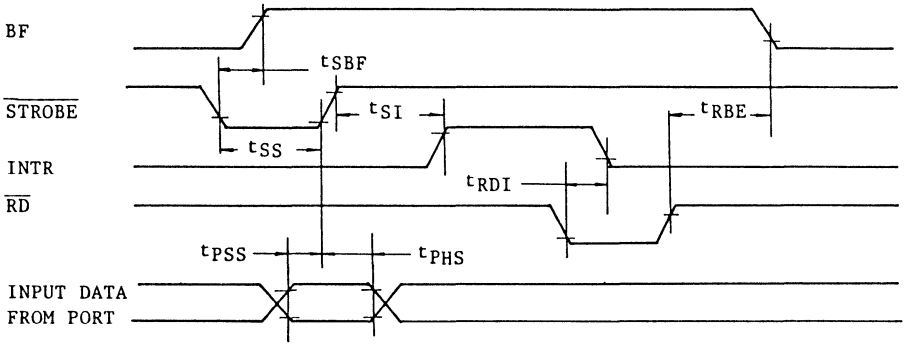


FIGURE 8 BASIC I/O TIMING WAVEFORM

A. STROBED INPUT MODE



B. STROBED OUTPUT MODE

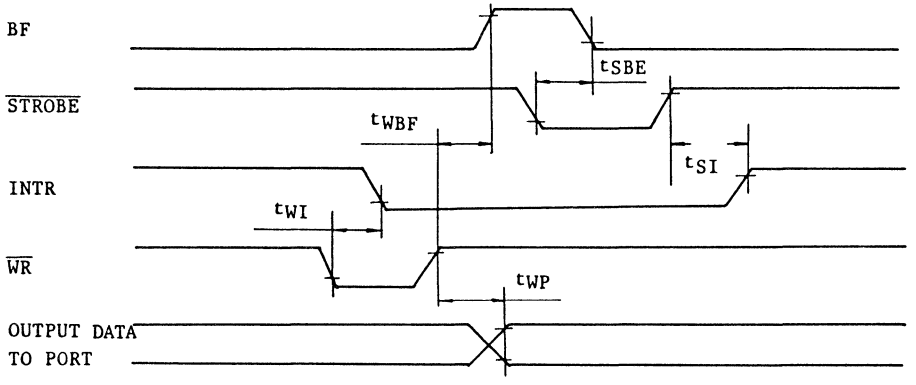
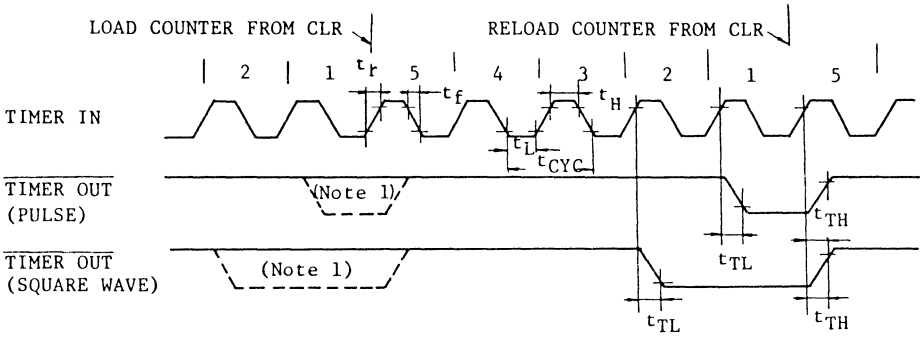


FIGURE 9 STROBED I/O TIMING WAVEFORM

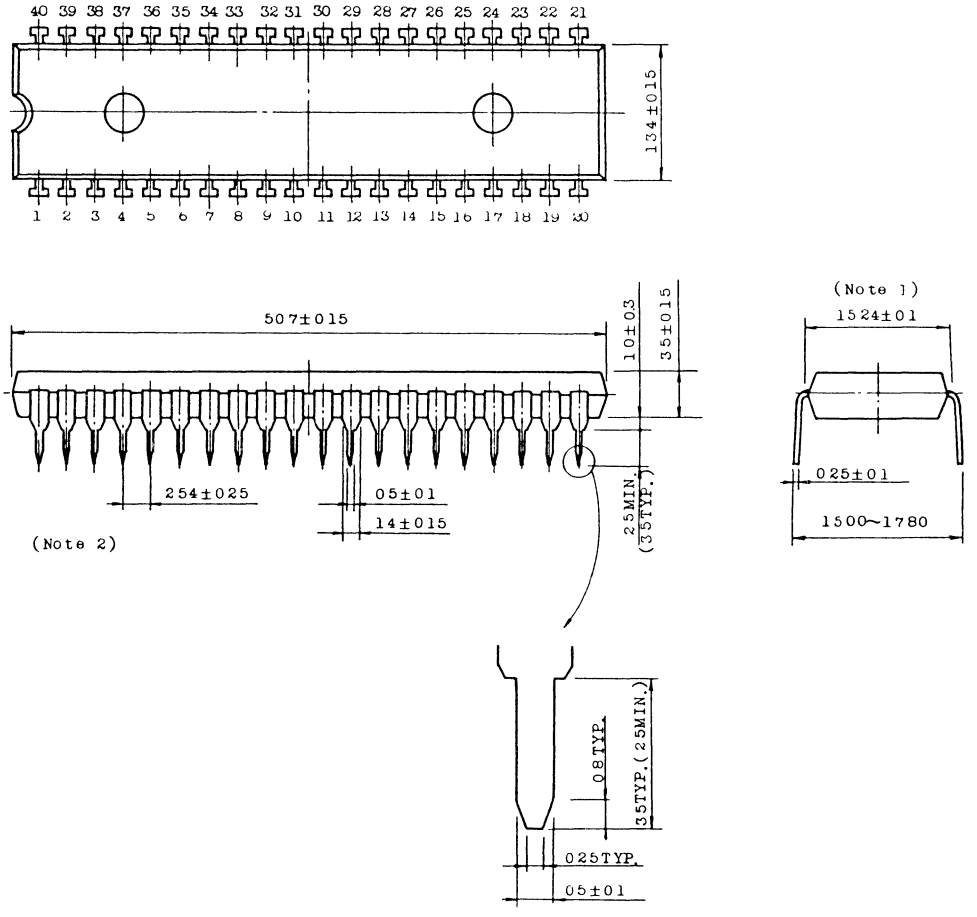


Note 1: The timer output is periodic if in an automatic reload mode (M_1 Mode Bit = 1)

FIGURE 10 TIMER OUTPUT WAVEFORM COUNTDOWN FROM 5 TO 1

OUTLINE DRAWING

Unit in mm



Note: 1. This dimension is measured at the center of bending point of leads.

2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoritical positions with respect to No.1 and No.40 leads.

16,384 BIT ROM WITH I/O PORTS

GENERAL DESCRIPTION

The TMP8355P is a ROM and I/O chip to be used in the TLCS-85A microcomputer system. The ROM portion is organized as 2,048 words by 8 bits.
The I/O portion consists of 2 general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is individually programmable as input or output.

FEATURES

- 2048 words x 8 bits ROM
- Single + 5V Power Supply
- Internal Address Latch
- 2 General Purpose 8-Bit I/O Ports
- Access Time : 400 ns (MAX.)
- Each I/O Port Line Individually Programmable as Input or Output
- Multiplexed Address and Data Bus
- 40 pin DIP
- Compatible with Inptel's 8355

PIN CONNECTIONS (TOP VIEW)

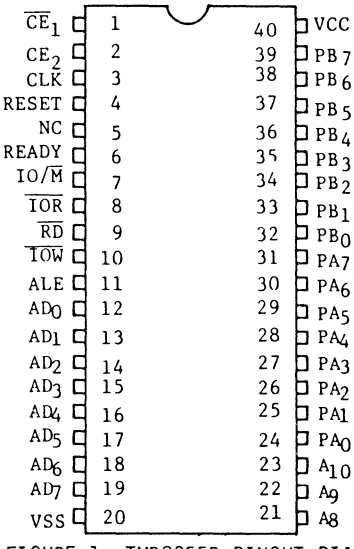


FIGURE 1 TMP8355P PINOUT DIAGRAM

BLOCK DIAGRAM

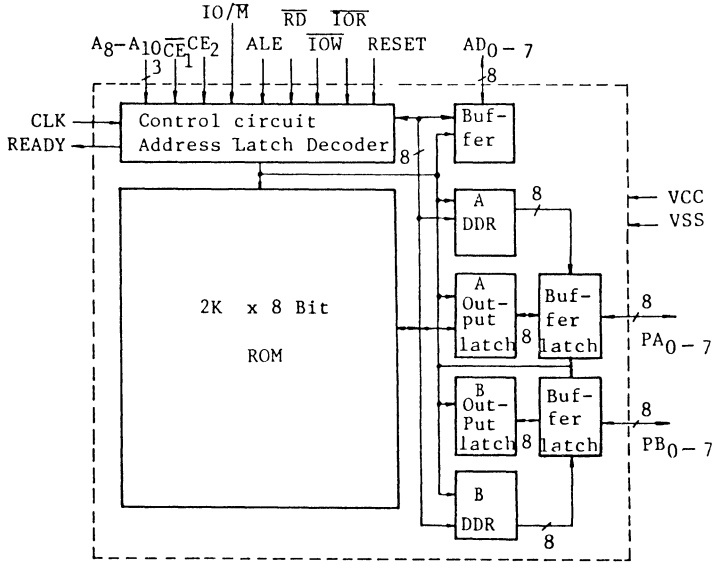


FIGURE 2 TMP8355P FUNCTIONAL BLOCK DIAGRAM

PIN NAMES AND PIN DESCRIPTION

ALE (INPUT)

When Address Latch Enable goes high, AD_{0-7}, IO/$\overline{M}$, A_{8-10}, CE_2, and $\overline{CE_1}$, enter the address latches. The signals (AD_{0-7}, IO/$\overline{M}$, A_{8-10}, CE_2, $\overline{CE_1}$) are latched in at the trailing edge of ALE.

AD_{0-7} (INPUT/OUTPUT, 3-STATE)

Bi-directional Address/Data bus. The lower 8-bits of the ROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle, Port A or B are selected based on the latched value of AD_0. If $\overline{RD}$ or $\overline{IOR}$ is low when the latched Chip Enables are active, the output buffers present data on the bus.

A_{8-10} (INPUT)

These are the high order bits of the ROM address. They do not affect I/O operations.

$\overline{CE1}$, CE2 (INPUT)

CHIP ENABLE INPUTS: $\overline{CE_1}$ is active low and CE_2 is active high. Both chip enables must be active to permit accessing the ROM.

IO/$\overline{M}$ (INPUT)

If the latched IO/$\overline{M}$ is high when $\overline{RD}$ is low, the output data comes from an I/O port. If it is low the output data comes from the ROM.

$\overline{RD}$ (INPUT)

If the latched Chip Enables are active when $\overline{RD}$ goes low, the AD_{0-7} output buffers are enabled and output either the selected ROM location or I/O port.
When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD_{0-7} output buffers are 3-stated.

$\overline{IOW}$ (INPUT)

If the latched Chip Enables are active, a low on $\overline{IOW}$ causes the output port pointed to by the latched value of AD_0 to be written with the data on AD_{0-7}.
The state of IO/$\overline{M}$ is ignored.

CLK (INPUT)

The CLK is used to force the READY into its high state after it has been forced low by $\overline{CE_1}$ lOW, CE_2 high, and ALE high.

READY (OUTPUT, 3-STATE)

READY is a 3-state output controlled by $\overline{CE}_1$, CE_2, ALE and CLK.
READY is forced low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK.

PA_0 - PA_7 (INPUT/OUTPUT, 3-STATE)

These are general purpose I/O pins. Their input/output direction is determined by the contents of Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active, and $\overline{IOW}$ is low and a 0 was previously latched from AD_0.
Read operation is selected by either $\overline{IOR}$ low, active Chip Enables and AD_0 low, or IO/$\overline{M}$ high, $\overline{RD}$ low, active Chip Enables, and AD_0 low.

PB_0 - PB_7 (INPUT/OUTPUT, 3-STATE)

This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD_0.

RESET (INPUT)

In normal operation, an input high on RESET causes all pins in Ports A and B to assume input mode (clear DDR register).

$\overline{IOR}$ (INPUT)

When the Chip Enables are active, a low on $\overline{IOR}$ will output the selected I/O port onto the AD bus. $\overline{IOR}$ low performs the same function as the combination of IO/$\overline{M}$ high and $\overline{RD}$ low. When $\overline{IOR}$ is not used in a system, $\overline{IOR}$ should be tied to V_{CC} "1".

V_{CC} (POWER)

+5 volt supply.

V_{SS} (POWER)

Ground Reference

FUNCTIONAL DESCRIPTION

ROM SECTION

The TMP8355P contains an 8-bit address latch which allows it to interface circectly to TLCS-85A microcomputer system without additional hardware.
The ROM portion of the chip is addressed by the 11-bit address (A8-10, AD_{0-7}) and CE. The address, IO/$\overline{M}$, CE_2 and $\overline{CE_1}$ are latched into the address latches on falling edge of ALE. If the Chip Enables (CE_2 and $\overline{CE_1}$) are active and IO/$\overline{M}$ is low when $\overline{RD}$ goes low, the contents of the ROM location addressed by the latched address are put out on the AD_{0-7} lines.

I/O SECTION

The I/O port portion consits of two 8-bit I/O ports and two 8-bit Data Direction Registers (DDR). The I/O portion of the chip is addressed by the latched value of AD_0 and AD_1. Contents of Port A and Port B can be read and written, but the contents of DDR's cannot be read. The contents of the selected I/O port can be read out when the latched Chip Enable are active and either $\overline{RD}$ goes low with IO/$\overline{M}$ high, or $\overline{IOR}$ goes low.
The two 8-bit DDR's (DDRA and DDRB) are used to determine the input/output status of each pin in the corresponding port.
A '0' specifies an input mode and a '1' specifies an output mode.
The two 8-bit DDR's are cleared by RESET signal. The table 1 summarize Port and DDR designation.

TABLE 1, SELECTION OF PORT AND DDR DESIGNATION

AD_1	AD_0	Selection
0	0	Port A
0	1	Port B
1	0	Port A Data Direction Register (DDR A)
1	1	Port B Data Direction Register (DDR B)

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating
V_{CC}	V_{CC} Supply Voltage with Respect to V_{SS}	-0.5V to 7.0V
V_{IN}	Input Voltage with Respect to V_{SS}	-0.5V to 7.0V
V_{OUT}	Output Voltage with Respect to V_{SS}	-0.5V to 7.0V
P_D	Power Dissipation	1.5W
T_{SOLDER}	Soldering Temperature (Soldering Time 10sec.)	260°C
T_{STG}	Storage Temperature	-55°C to+150°C
T_{OPR}	Operating Temperature	0°C to+70°C

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}+0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -400μA	2.4			V
I_{IL}	Input Leakage Current	V_{IN} = V_{CC} to 0V			± 10	μA
I_{LO}	Output Leakage Current	0.45 ≤ Vout ≤ V_{CC}			± 10	μA
I_{CC}	V_{CC} Supply Current				180	mA

A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
t_{CYC}	Clock Cycle Time		320			ns
t_L	CLK Low Width		80			ns
t_H	CLK High Width		120			ns
t_r, t_f	CLK Rise and Fall Time				30	ns
t_{AL}	Address to Latch Set Up Time		50			ns
t_{LA}	Address Hold Time after Latch		80			ns
t_{LC}	Latch to READ/WRITE Control		100			ns
t_{RD}	Valid Data Out Delay from READ Control	150pF			170	ns
t_{AD}	Address Stable to Data Out Valid	Load			400	ns
t_{LL}	Latch Enable Width		100			ns
t_{RDF}	Data Bus Float after READ		0		100	ns
t_{CL}	READ/WRITE Control to Latch Enable		20			ns
t_{CC}	READ/WRITE Control Width		250			ns
t_{DW}	Data In to WRITE Set Up Time		150			ns
t_{WD}	Data In Hold Time after WRITE		10			ns
t_{WP}	WRITE to Port Output				400	ns
t_{PR}	Port Input Set Up Time		50			ns
t_{RP}	Port Input Hold Time		50			ns
t_{RYH}	READY Hold Time		0		160	ns
t_{ARY}	ADDRESS (CE) to READY				160	ns
t_{RV}	Recovery Time between Controls		300			ns
t_{RDE}	Data Out Delay from READ Controls		10			ns
t_{LCK}	ALE Low during CLK High		100			ns

TIMING WAVEFORMS

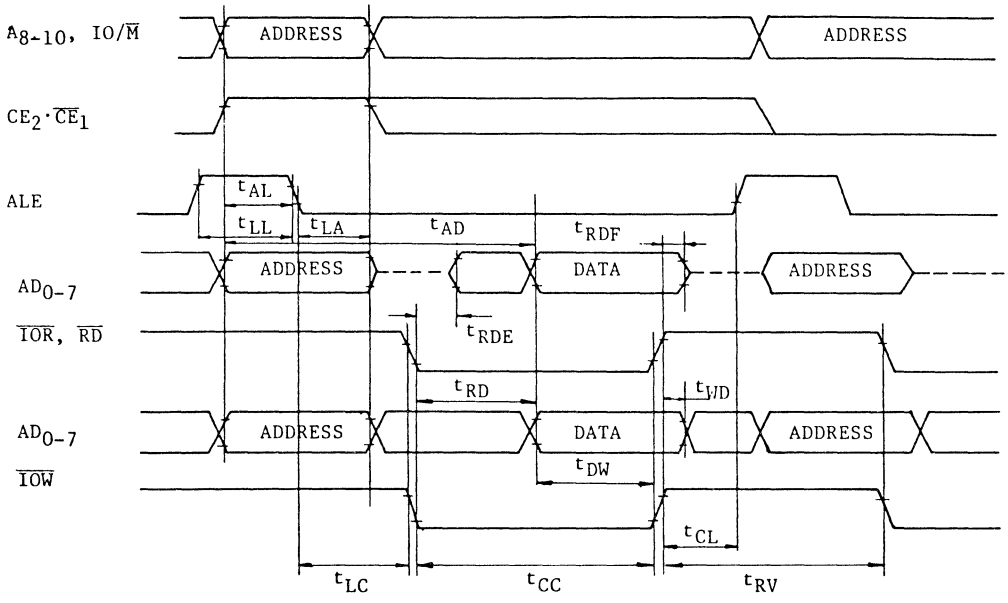


FIGURE 3 PROM READ, I/O READ, AND WRITE TIMING

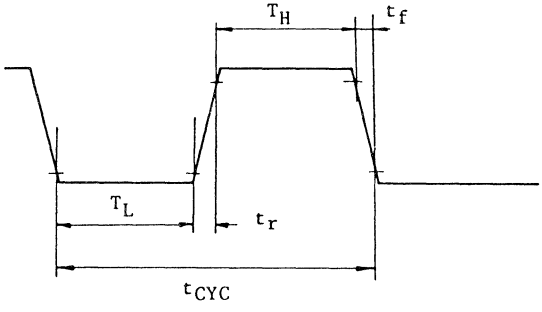


FIGURE 4 CLOCK SPECIFICATION FOR TMP8355P

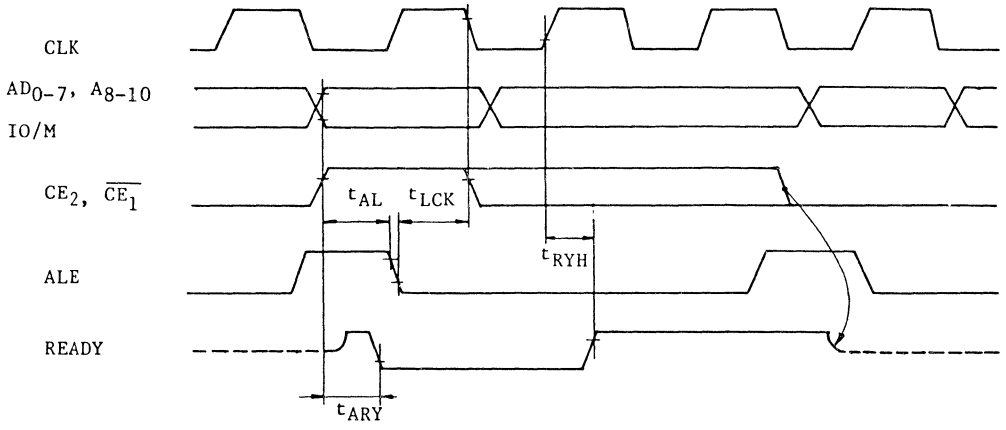
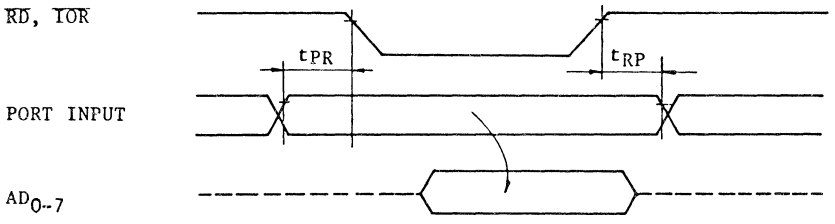


FIGURE 5 WAIT STATE TIMING (READY = 0)

A. INPUT MODE



B. OUTPUT MODE

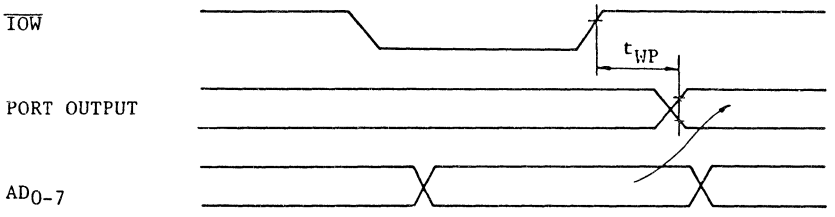
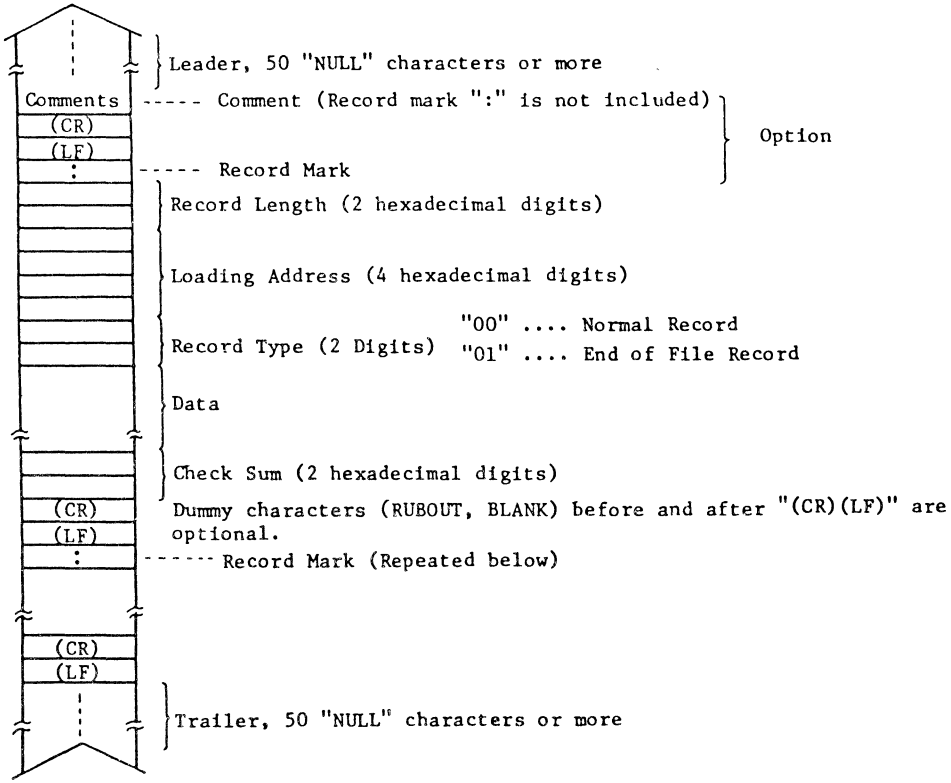


FIGURE 6 I/O PORT TIMING

PROGRAM TAPE FORMAT

TMP8355P programs are delivered in the form of punched paper tape or the 8755A from which to copy. In case of the 8755A, Toshiba needs two pieces.

(1) Tape Format

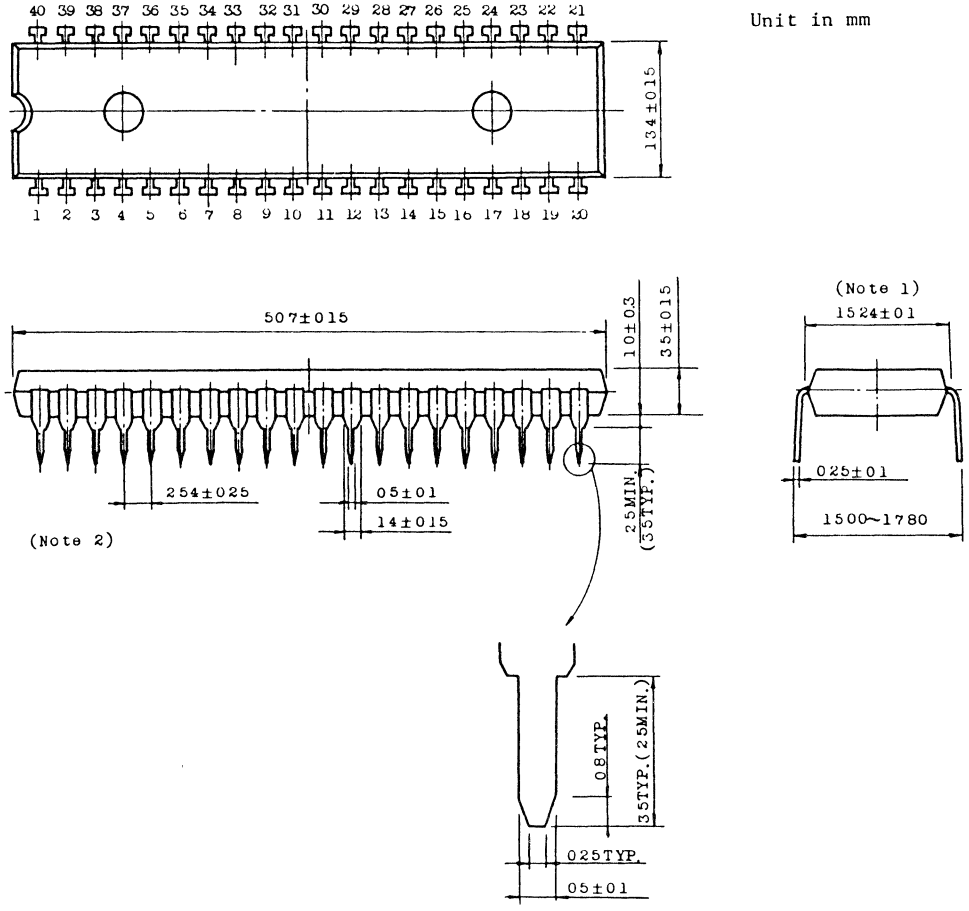


(2) Example of Tape List

```
TOSHIBA MICRO COMPUTER TLCS-84
:100000000665C7D79CF50F3F951FED55A8FF16E570
:1000100088884DDE67D31F5D8ABA6DF292F113F5C1
:100020004FF1FB5DFFDAA96A99CF7DF94A346B7C09
:10003000197352F729F12F79AA9C057C5B851EED77
                    :
                    :
                    :
                    :
                    :
:1003C0005DFDB5E556A67277F61A51C631CF9F0E80
:1003D000BD2F6F20E8BB1977E3FB5AD1F41FDAA7E2
:1003E000B53D42E0EC32546025B7308CDD52063D1D
:1003F000B4BE9E9E345B6138060B20VC372BF60BD6
:00000001FF
```

OUTLINE DRAWING

Unit in mm



Note: 1. This dimension is measured at the center of bending point of leads.

2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoritical positions with respect to No.1 and No.40 leads.

PROGRAMMABLE COMMUNICATION INTERFACE

TMP82C51AP-2/TMP82C51AF-2
TMP82C51AP-8/TMP82C51AF-8

GENERAL DESCRIPTION

The TMP82C51A is the industry standard Universal Synchronous/Asynchronous Receiver/Transmitter (USART) that is fabricated using C-MOS silicon gate technology.
The 82C51A is mainly used for 8-bit microcomputer extension system, which require serial data communications.

The TMP82C51AP-2/TMP82C51AP-2 is packaged in the 28 pin standard Dual Inline Package.
The TMP82C51AF-2/TMP82C51AF-8 is packaged in the 44 pin Flat Package.

FEATURES

. Synchronous and Asynchronous Operation

  - Synchronous:
    5-8 Bit Characters
    Internal or External Character Synchronization
    Single or Double Character Synchronization (Internal)
    Automatic Sync Insertion

  - Asynchronous:
    5-8 Bit Characters
    Clock Rate - 1, 16 or 64 Times Baud Rate
    Break Character Generation
    1, 1.5 or 2 stop Bits
    False Start Bit Detection
    Automatic Break Detect and Handling

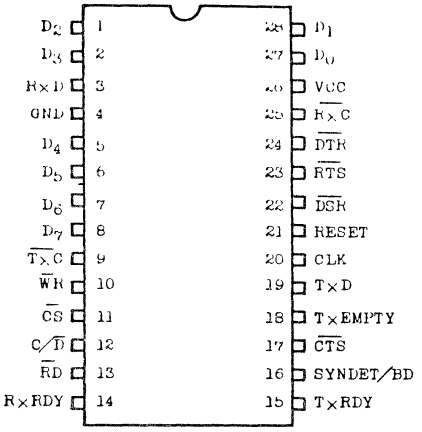
. Baud Rate TMP82C51AP-2 TMP82C51AP-8
DC-104K Baud DC-240k Baud

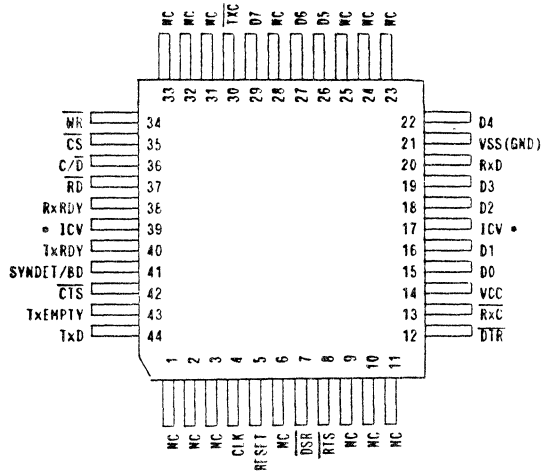
. Full-Duplex, Double-Buffered, Transmitter and Receiver

. Error Detection-Parity, Overrun and Framing

. Single +5V Supply : 5V + 10%

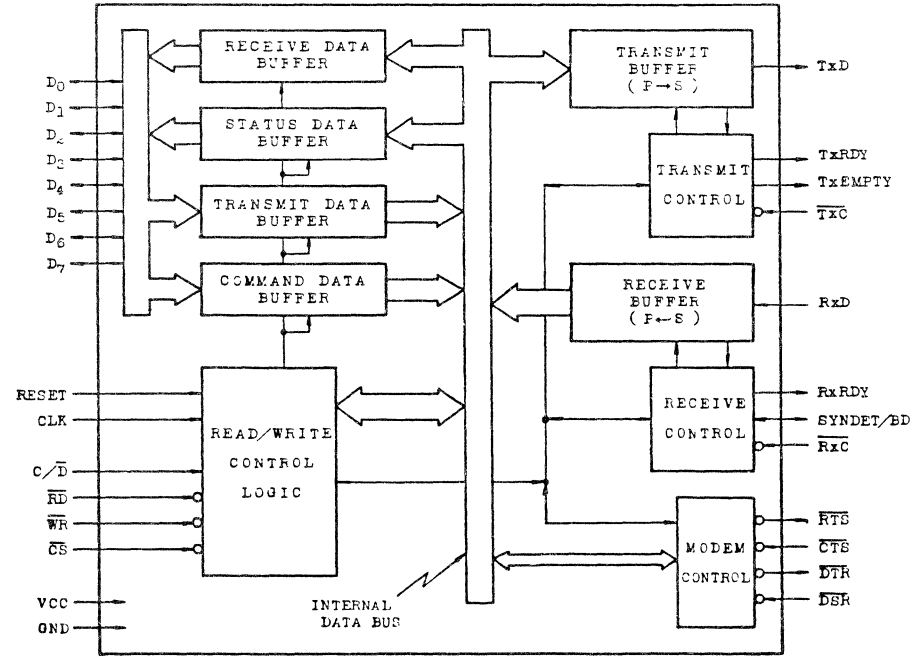
PIN CONNECTIONS (TOP View)





* Pin 17 and Pin 39 must be connected to Vcc or must be open.
NC: No connection

BLOCK DIAGRAM



PIN NAMES AND PIN DESCRIPTIONS

. Interface Signals to CPU (Main System)

D0 - D7 (Input/Output)

This 3-state, bidirectional, 8-bit buffer is used to interface the 82C51A to the system Data Bus. Data is transmitted or received through the buffer upon execution of Input or Output Instructions of the CPU. Control Words, Command Words and Status Information are also transferred through the Data Bus Buffer.

$\overline{WR}$ (Input)

A "low" level signal on this input informs the 82C51A that the CPU is Writing Data or Control Words to the 82C51A.

$\overline{RD}$ (Input)

A "low" level signal on this input informs the 82C51A that the CPU is Reading Data or Status Information from the 82C51A.

$\overline{CS}$ (Input)

A "low" level signal on this input selects the 82C51A. No reading or writing operation will occur unless the device is selected. When $\overline{CS}$ is "high" the Data Bus is in the floating state and $\overline{RD}$ and $\overline{WR}$ have no effect on the chip.

C/$\overline{D}$ (Input)

This input signal, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the 82C51A that the word on the Data Bus is either a Data Character, Control Word or Status Information. A "high" level signal means Control or Status, a "low" level signal means Data.

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	82C51A Receive DATA Buffer --> DATA Bus
0	1	0	0	82C51A Transmit DATA Buffer <-- DATA Bus
1	0	1	0	82C51A Status DATA Buffer --> DATA Bus
x	1	1	0	DATA Bus is in floating state.
x	x	x	1	DATA Bus is in floating state.

CLK (Input)

The CLK input is used to generate internal device timing. No external input or output is referenced to CLK, but the frequency of CLK must be greater than 30 times the Receiver or Transmitter Data Bit Rates ($\overline{RxC}$ or $\overline{TxC}$) in Synchronous Operation, and greater than 4.5 times the Receiver Data Bit Rates ($\overline{RxC}$ or Transmitter, $\overline{TxC}$) in Asynchronous operation.

RESET (Input)

A "high" level signal on this input forces the 82C51A into an "Idle" mode. The device will remain at "Idle" until a new set of Control Words is written into the 82C51A to program its functional definition. Minimum RESET pulse width is 6 tcy.

. MODEM Control Signals

$\overline{\text{DSR}}$ (Input)

The $\overline{\text{DSR}}$ input signal is a general purpose, 1-bit inverting input port. Its condition can be tested by the CPU using a Status Read Operation. The $\overline{\text{DSR}}$ input is normally used to test MODEM conditions such as Data Set Ready signal.

$\overline{\text{DTR}}$ (Output)

The $\overline{\text{DTR}}$ output signal is a general purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction Word. The $\overline{\text{DTR}}$ output signal is normally used for MODEM control such as Data Terminal Ready or Rate Select signal.

$\overline{\text{RTS}}$ (Output)

The $\overline{\text{RTS}}$ output signal is a general purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction Word. The $\overline{\text{RTS}}$ output signal is normally used for MODEM control such as Request to Send signal.

$\overline{\text{CTS}}$ (Input)

A "low" level signal on this input enables the 82C51A to transmit serial data, if the Tx Enable Bit in the Command Byte is set to a "one" (TxEN=1). If either a Tx Enable off (TxEN=0) or $\overline{\text{CTS}}$ off (CTS=1) condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART, written prior to Tx Disable Command before shutting down.

. Transmit Control Signals

$\overline{\text{TxC}}$ (Input)

The transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous Transmission Mode, the Baud Rate (1x) is equal to the $\overline{\text{TxC}}$ frequency. In Asynchronous Transmission Mode the baud rate is a fraction of the actual $\overline{\text{TxC}}$ frequency. A portion of the Mode Instruction selects this factor; it can be 1, 1/16 or 1/64 the $\overline{\text{TxC}}$.

For Example:
If Baud Rate equals 110 Baud,
$\overline{\text{TxC}}$ = 110 Hz (1x)
$\overline{\text{TxC}}$ = 1.76 kHz (16x)
$\overline{\text{TxC}}$ = 7.04 Hz (64x)

The falling edge of $\overline{TxC}$ shifts the serial data out of the 82C51A.

TxD (Output)

This line is used to transmit the serial data. Serial output data on TxD is changed from parallel data to serial data in accordance with the TxD line will be held in the marking state ('1' level) immediately on one of the followings.

- Master Reset
- CTS signal is high ($\overline{CTS}$=1)
- Tx Disable (TxEN=0)
- TxEMPTY signal is high (TxEMPTY=1)

TxRDY (Output)

This output informs the CPU that the transmitter is ready to accept a Data Character. The TxRDY output pin can be used as an interrupt to the system, since it is masked by Tx Disable (TxEN=0), or, for polled Operation, the CPU can check TxRDY using a Sttus Read Operation, TxRDY is automatically reset by the trailing edge of $\overline{WR}$ when a Data Character is loaded from the CPU. The TxRDY pin output status (TxRDY (pin)) is different from the TxRDY status bit status register (TxRDY (status bit)) as follows.

TxRDY (status bit) = (Transmit Data Buffer Empty)
TxRDY (pin) = (Transmit Data Buffer Empty) AND ($\overline{CTS}$=0) AND (TxEN=1)

TxEMPTY (Output)

The TxEMPTY output will go "high" when the 82C51A has no characters to send. It resets upon receiving a character from the CPU if the transmitter is enabled.

In Synchronous Mode, a "high" level signal on this output indicates that a Character has not been loaded and the SYNC Character or Characters are about to be or are being transmitted automatically as "fillers". TxEMPTY does not go "low" when the SYNC characters are being shifted out.

. Receive Control Signals

$\overline{RxC}$ (Input)

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the Baud Rate (1x) is equal to the actual frequency of $\overline{RxC}$. In Asynchronous Mode, the Baud Rate is a fraction of the actual $\overline{RxC}$ frequency. A portion of the Mode Instruction selects this factor; 1, 1/16 or 1/64 the RxC.

For Example:
if Baud Rate equals 2400 Baud,
$\overline{RxC}$ = 2.4 kHz (1x)
$\overline{RxC}$ = 38.4 kHz (16x)
$\overline{RxC}$ = 153.6kHz (64x)

Data is sampled into the 82C51A on the rising edge of $\overline{RxC}$.

RxD (Input)

This line is used to receive the serial data. Serial input data on this line is changed to parallel data in accordance with the format specified by the Control Words, and then transfered to the Receive Data Buffer.

RxRDY (Output)

This output indicates that the 82C51A contains a Data Character that is ready to be input to the CPU. RxRDY can be connected to the interrupt structure of the CPU, or, for Polled Operation, the CPU can check the condition of RxRDY using a Status Read Operation.
Rx Enable off both masks and holds RxRDY in the Reset Condition.

SYNDET/BD (Input/Output)

This pin is used for SYNDET in Synchronous Mode and may be used as either input or output, programmable through the Control Word. It is reset to output mode "low" upon RESET. When used as an Output (Internal Sync Mode), the SYNDET pin will go "high" to indicate that the 82C51A has located the SYNC Character in the Receive Mode. If the 82C51A is programmed to use Double Sync Characters then SYDET will go "high" in the middle of the last bit of the second SYNC Character. SYNDET is automatically reset upon a Status Read Operation. When used as an Input (External Sync Mode), a positive going signal will cause the 82C51A to start assembling Data Characters on the rising edge of the next $\overline{RxC}$.

In Asynchronous Mode this pin is used for BD.
This output will go "high" whenever the receiver remains "low" through two consecutive Stop Bit Sequences (including the Start Bits, Data Bits, and parity bits). Break Detect may also be read as a Status Bit.
It is reset only upon a Master Chip Reset or Rx Data returning to a "one" state.

. Power Supply

  . VCC (power)
    +5 Volt supply

  . GND (Power)
    0 Volt supply

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating
VCC	Power Supply Voltage (with respect to GND)	-0.5V to 7.0V
VIN	Input Voltage (with respect to GND)	-0.5V to VCC+0.5
VOUT	IOutput Voltage (with respect to GND)	-0.5V to VCC+0.5
PD	Power Dissipation (Ta=70°C)	250mW
TSOLDER	Soldering Temperature (10 sec)	260°C
TSTG.	Storage Temperature	-65°C to 150°C
TOPR.	Operating Temperature	-40°C to 85°C

D.C CHARACTERS

Topr = -40°C to +85°C, VCC = +5V ± 10%, GND=0V, Unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
VIL	Input Low Voltage		-0.5	-	0.8	V
VIH	Input High Voltage		2.2	-	VCC+0.5	V
VOL	Output Low Voltage	IOL=2.2mA	-	-	0.45	V
VOH1	Output High Voltage	IOH=-400uA	2.4	-	-	V
VOH2	Output High Voltage	IOH=-100uA	Vcc-0.8	-	-	V
VOFL	Output Leak Current	0.45V≦VOUT≦VCC	-	-	±10	uA
IIL	Input Leak Current	0.45V≦VOUT≦VCC	-	-	±10	uA
ICC1	Power Supply Current (AP-2/AF-2,5MHz)	tcyc=200ns Vin=4.8V/0.2V	-	1.2	5.0	mA
	Power Supply Current (AP-8/AF-8,8MHz)	tcyc=125ns Vin=4.8V/0.2V	-	2.0	8.0	mA
ICC2	Power Supply Current (Standby Mode)	Stop All Clocks VCC=5V,$\overline{CS}$=1 Vin=4.8V/0.2V				uA

A.C. CHARACTERISTICS
Topr= -40°C to +80°C, VCC= 5V ± 10%, GND=0V, Unless otherwise noted.

BUS READ CYCLE TIMING Note 1)

Symbol	Parameter	Test Conditions	AP-2/AF-2 Min.	AP-2/AF-2 Max.	AP-8/AF-8 Min.	AP-8/AF-8 Max.	Units
tAR	$\overline{CS}$, C/$\overline{D}$ Set-Up Time for $\overline{RD}$		10	-	10	-	nS
tRA	$\overline{CS}$, C/$\overline{D}$ Hold Time for $\overline{RD}$		0	-	0	-	nS
tRR	$\overline{RD}$ Pulse Width		150	-	150	-	nS
tRD	Data Delay Time for $\overline{RD}$ Note 2)	CL=150pF Note 3)	-	140	-	140	nS
tDF	Data Hold Time for $\overline{RD}$		10	80	10	50	nS

BUS WRITE CYCLE TIMING Note 1)

Symbol	Parameter	Test Conditions	TMP82C51AP-2		TMP82C51AP-8		Units
			Min.	Max.	Min.	Max.	
tAW	$\overline{CS}$, C/$\overline{D}$ Set-Up Time for $\overline{WR}$		0	-	0	-	nS
tWA	$\overline{CS}$, C/$\overline{D}$ Hold Time for $\overline{WR}$		0	-	0	-	nS
tWW	$\overline{RD}$ Pulse Width		150	-	150	-	nS
tDW	Data Set-Up Time for $\overline{WR}$		100	-	80	-	nS
tWD	Data Hold Time for $\overline{WR}$		10	-	10	-	nS
tRV	Recovery Time Between Write	Note 4)	6	-	6	-	tcyc

OTHER TIMINGS

Symbol	Parameter	Test Conditions	TMP82C51AP-2		TMP82C51AP-8		Units
			Min.	Max.	Min.	Max.	
tcyc	Clock Period Note 5),6)		200	-	125	-	nS
tH	Clock High Level Wdith		80	-	50	-	nS
tL	Clock Low Level Width		50	-	35	-	nS
tR,tF	Clock Rise, Fall Time		-	20	-	20	nS
tDTx	TxD Delay Time from Falling Edge of TxC		-	1	-	0.5	us
fTx	Transmitter Input Clock Frequency	1xBaud Rate	DC	104	DC	240	kHz
		16xBaud Rate	DC	528	DC	1536	
		64xBaud Rate	DC	832	DC	1536	
tTPH	Transmitter Input Clock Low Level Width	1xBaud Rate	12	-	12	-	tcyc
		16x, 64x, Baud Rate	1	-	1	-	
tTPL	Transmitter Input Clock High Level Width	1xBaud Rate	15	-	15	-	tcyc
		16x, 64x, Baud Rate	3	-	3	-	
fRx	Receiver Input Clock Frequency	1xBaud Rate	DC	104	DC	240	kHz
		16xBaud Rate	DC	528	DC	1536	
		64xBaud Rate	DC	832	DC	1536	
tRPH	Receiver Input Clock High Level Width	1xBaud Rate	12	-	12	-	tcyc
		16x, 64x, Baud Rate	1	-	1	-	
tRPH	Receiver Input Clock Low Level Width	1xBaud Rate	15	-	15	-	tcyc
		16x, 64x, Baud Rate	3	-	3	-	
tTxRDY	TxRDY Pin Delay Time from Center of Last Bit		-	14	-	14	tcyc
tTxRDY CLEAR	TxRDY Clear Delay Time from Leading Edge of $\overline{WR}$		-	400	-	200	ns

Symbol	Parameter	Test Conditions	TMP82C51AP-2		TMP82C51AP-8		Units
			Min.	Max.	Min.	Max.	
tRxRDY	TxRDY Pin Delay Time from Center of Last Bit		-	26	-	26	tcyc
tRxRDY CLEAR	RxRDY Clear Delay Time from Leading Edge of $\overline{RD}$		-	400	-	200	ns
tIS	Internal SYNDET Delay Time from Rising Edge of RxC		-	26	-	26	tcyc
tES	External SYNDET Set-Up Time for Falling Edge of RxC		-	18	-	18	tcyc
tTx EMPTY	TxEMPTY Delay Time from Center of Last Bit		-	20	-	20	tcyc
tWC	Control Delay Time from Rising Edge of $\overline{WR}$ (TxEN, $\overline{DTR}$, $\overline{RTS}$)		-	8	-	8	tcyc
tCR	$\overline{DSR}$, $\overline{CTS}$ Set-Up Time for $\overline{RD}$		20	-	20	-	tcyc

Notes:

1) AC Test Conditions: Output measuring point VOH=2.0V, VOL=0.8V
   Input supply level VIH=2.4V, VIL=0.45V

2) Assumes that Address is valid before the falling edge of $\overline{RD}$.

3) CL means load capacitance.

4) This recovery time is defined only for Mode Initialization.
   Write Data is allowed only when TxRDY=1. Recovery Time between Writes for Asynchronous Mode is 8 tcyc and for Synchronous Mode is 16 tcyc.

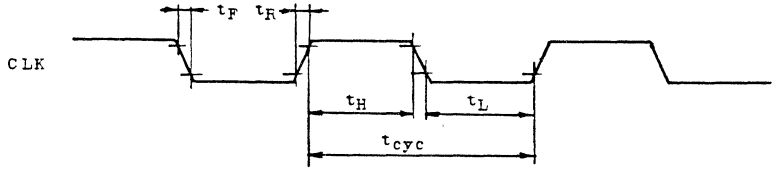
5) The $\overline{TxC}$ and $\overline{RxC}$ frequencies have the following limitations with respect to CLK:
   For 1x Baud Rate, fTx or fRx<1(30 tcyc)
   For 16x and 64x Baud Rate, ftX or fRx≤1(4.5 tcyc)

6) Minimum Reset Pulse Width is 6 tcyc. System Clock must running during Reset.

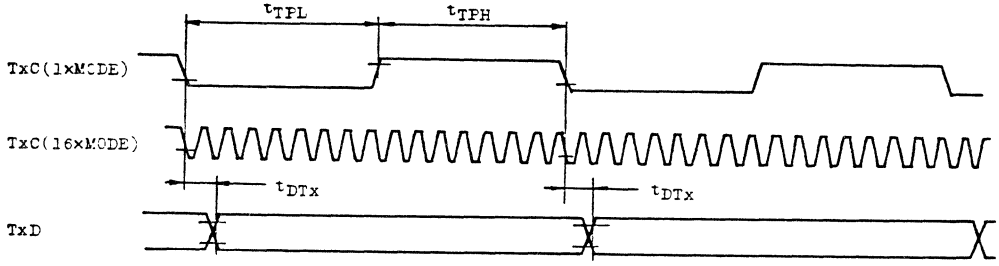
7) Status up data can have a maximum delay of 28 clock periods from the event affecting the status.

TIMING WAVEFORMS

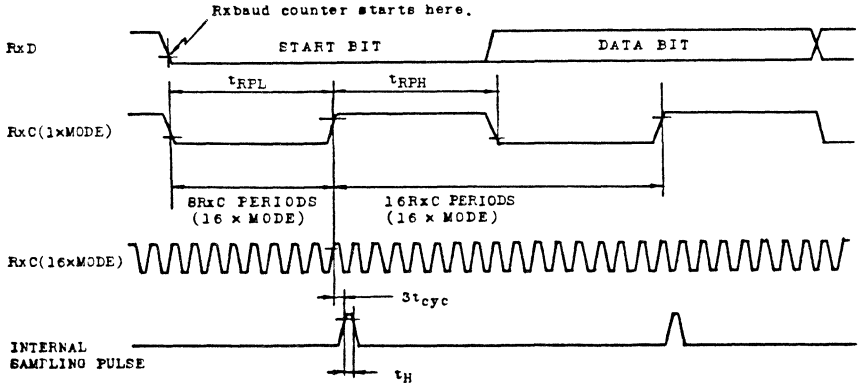
SYSTEM CLOCK INPUT



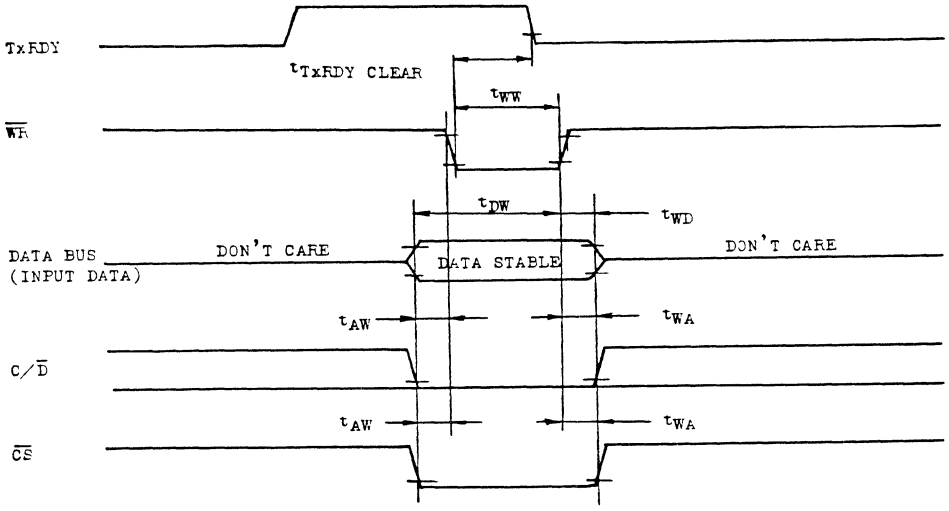
TRANSMITTER CLOCK AND DATA



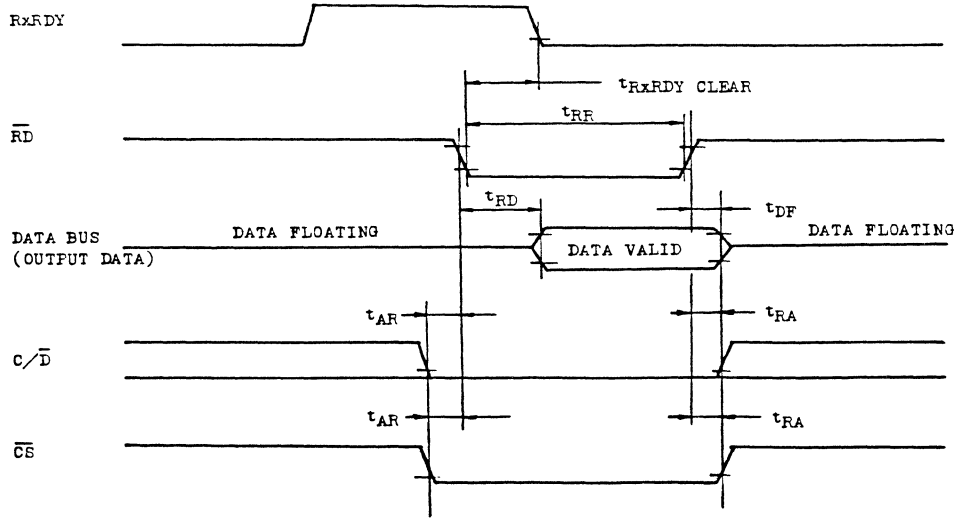
RECEIVER CLOCK AND DATA



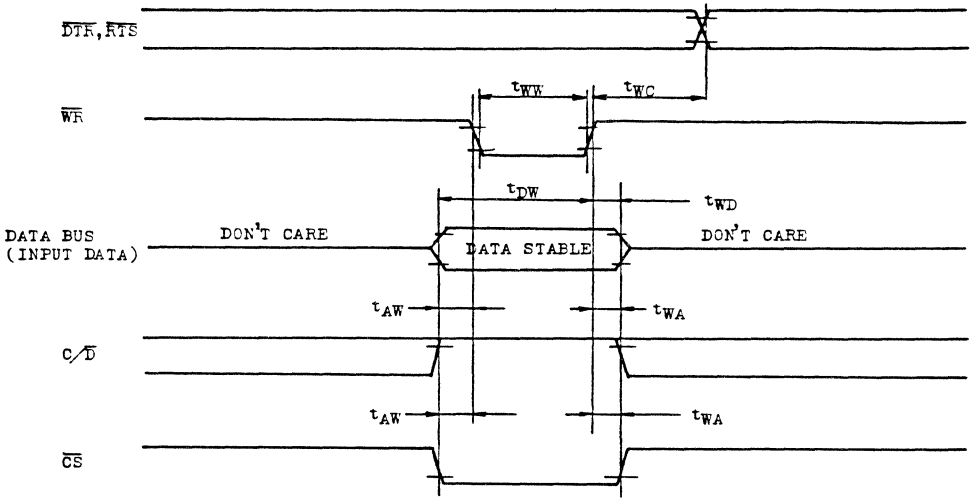
WRITE DATA CYCLE (CPU --> 82C51A)



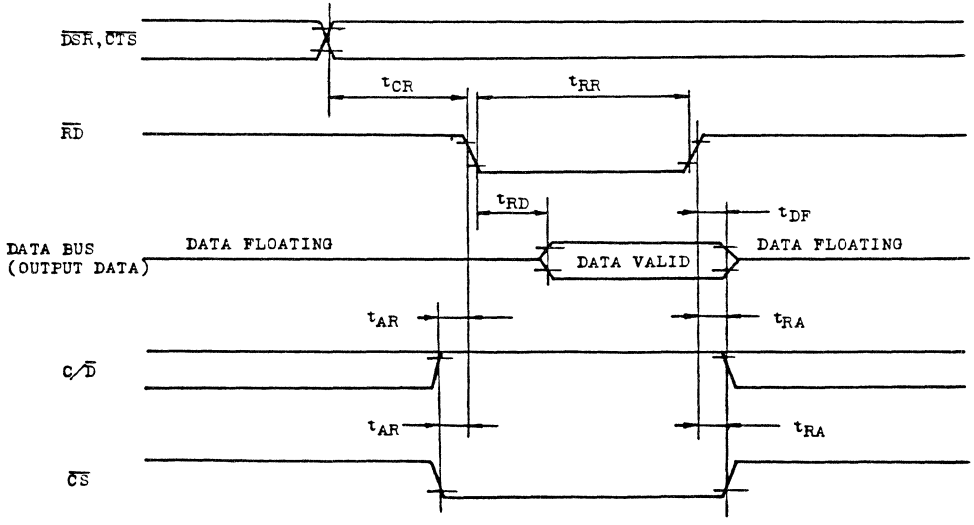
READ DATA CYCLE (82C51A --> CPU)



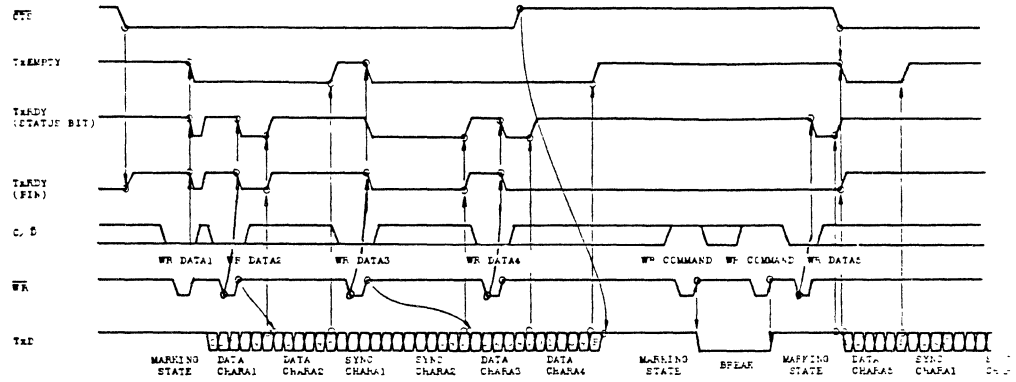
WRITE CONTROL OR OUTPUT PORT CYCLE (CPU --> 82C51A)



READ CONTROL OR INPUT PORT CYCLE (82C51A --> CPU)

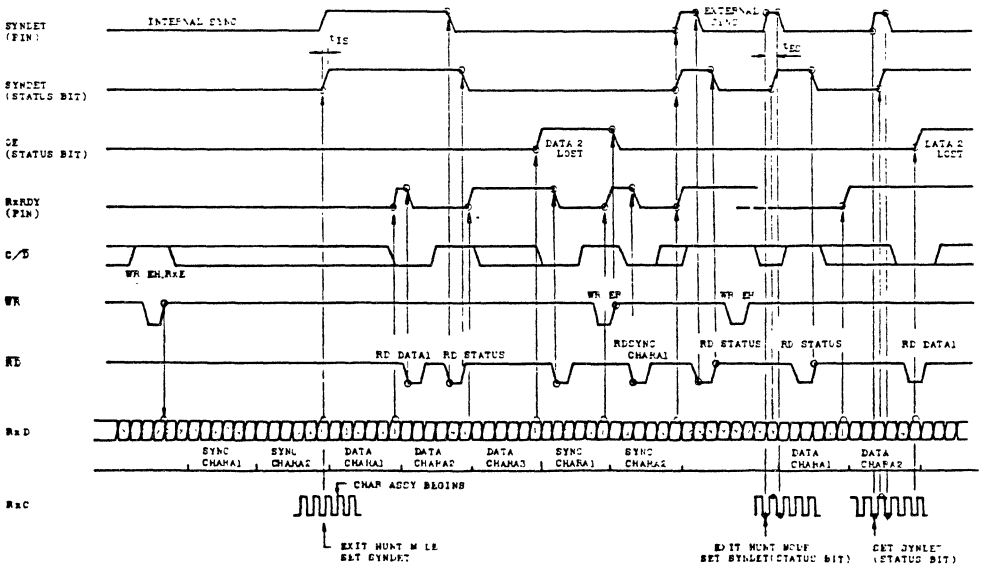


TRANSMITTER CONTROL AND FLAG TIMING (SYNC MODE)



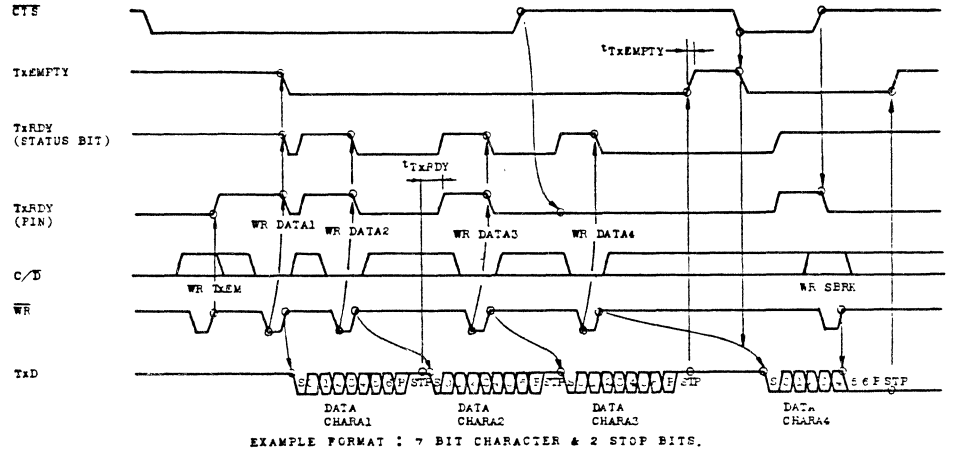
EXAMPLE FORMAT : 5 BIT CHARACTER WITH PARITY 2 SYNC CHARACTERS.

RECEIVER CONTROL AND FLAG TIMING (SYNC MODE)



EXAMPLE FORMAT : 8 BIT CHARACTER WITH PARITY 2 SYNC CHARACTERS.

TRANSMITTER CONTROL AND FLAG TIMING (ASYNC MODE)

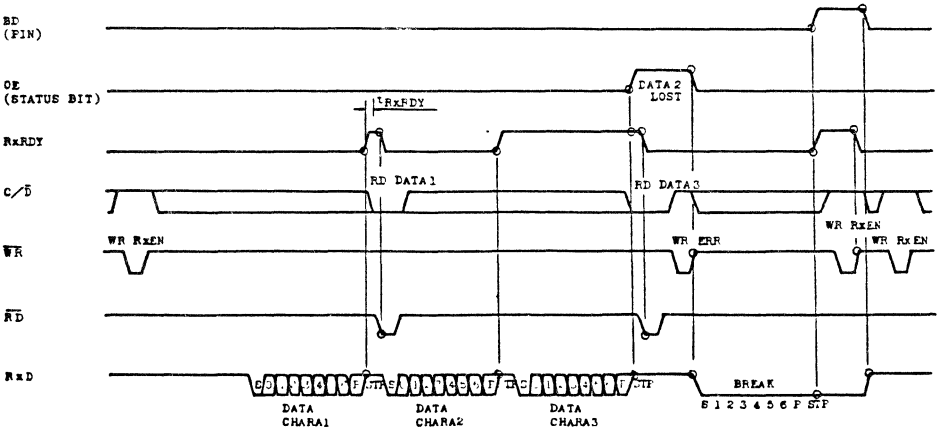


EXAMPLE FORMAT : 7 BIT CHARACTER & 2 STOP BITS.

Note : TxRDY(PIN) = (Transmit Data Buffer is empty) · (TxEN=1) · (CTS=0)
TxRDY(STATUS BIT) = (Transmit Data Buffer is empty)

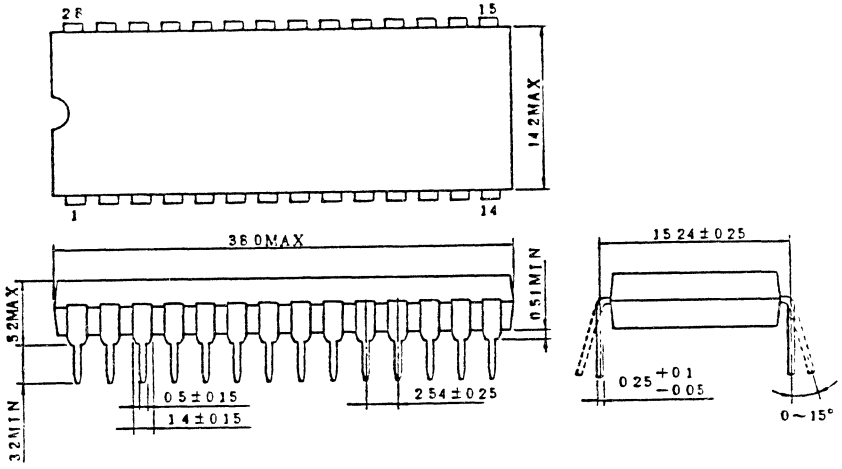
RECEIVER CONTROL AND FLAG TIMING (ASYNC MODE)

RECEIVER CONTROL AND FLAG TIMING (ASYNC MODE)



EXAMPLE FORMAT : 7 BIT CHARACTER WITH PARITY & 2 STOP BITS.

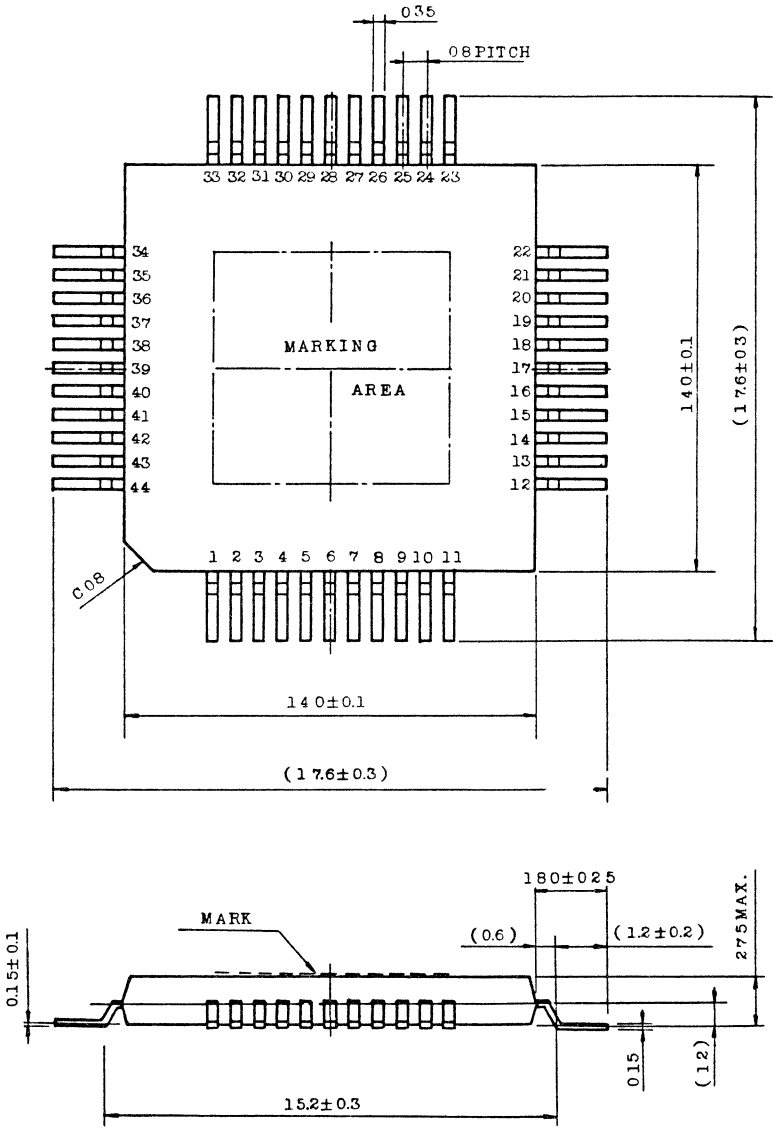
OUTLINE DRAWING (Dual Inline Package) Unit in mm



Note: Lead pitch is 2.54mm and to lerance is ±0.25mm against theoretical center of each lead that is obtained on the basis of NO.1 and NO.28 leads.

OUTLINE DRAWING (FLAT PACKAGE)

Unit in mm



PROGRAMMABLE COMMUNICATION INTERFACE

GENERAL DESCRIPTION

The TMP8251AP is the industry standard Universal Synchronous/Asynchronous Receiver/Transmitter (USART) that is fabricated using N-channel silicon gate MOS technology.

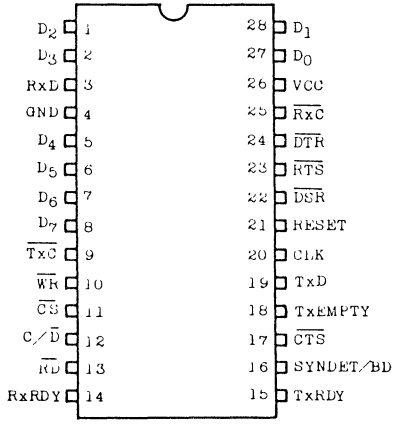
The TMP8251A is mainly used for 8-bit microcomputer extension systems, which require serial data communications.

FEATURES

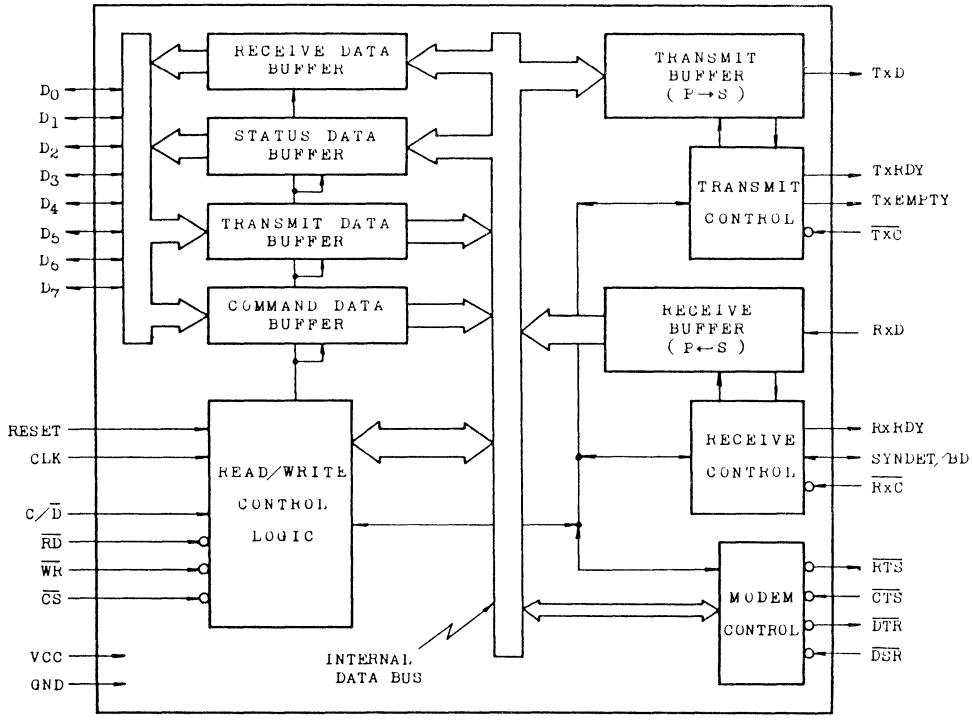
- Synchronous and Asynchronous Operation
  - Synchronous:
    - 5-8 Bit Characters
    - Internal or External Character Synchronization
    - Single or Double Character Synchronization (Internal)
    - Automatic Sync Insertion
  - Asynchronous:
    - 5-8 Bit Characters
    - Clock Rate - 1,16 or 64 Times Baud Rate
    - Break Character Generation
    - 1, 1 1/2, or 2 Stop Bits
    - False Start Bit Detection
    - Automatic Break Detect and Handling
- Baud Rate DC to 64K Baud (Synchronous)

  DC to 19.6K Baud (Asynchronous)
- Full-Duplex, Double-Buffered, Transmitter and Receiver
- Error Detection-Parity, Overrun and Framing
- Single +5V Supply
- Compatible with Intel's 8251A/S2657

PIN CONNECTIONS (Top View)



BLOCK DIAGRAM



PIN NAMES AND PIN DESCRIPTIONS

• Interface Signals to CPU (Main System)

$D_0 \sim D_7$ (Input/Output)

This 3-state, bidirectional, 8-bit buffer is used to interface the 8251A to the system Data Bus. Data is transmitted or received through the buffer upon execution of Input or Output Instructions of the CPU. Control Words, Command Words and Status Information are also transferred through the Data Bus Buffer.

$\overline{WR}$ (Input)

A "low" level signal on this input informs the 8251A that the CPU is Writing Data or Control Words to the 8251A.

$\overline{RD}$ (Input)

A "low" level signal on this input informs the 8251A that the CPU is Reading Data or Status Information from the 8251A.

$\overline{CS}$ (Input)

A "low" level signal on this input selects the 8251A. No reading or writing operation will occur unless the device is selected. When $\overline{CS}$ is "high" the Data Bus is in the floating state and $\overline{RD}$ and $\overline{WR}$ have no effect on the chip.

C/$\overline{D}$ (Input)

This input signal, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, imforms the 8251A that the word on the Data Bus is either a Data Character, Control Word or Status Infromation. A "high" level signal means Control or Status, a "low" level signal means Data.

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	8251A Receive DATA Buffer → DATA Bus
0	1	0	0	8251A Transmit DATA Buffer ← DATA Bus
1	0	1	0	8251A Status DATA Buffer → DATA Bus
1	1	0	0	8251A Command DATA Buffer ← DATA Bus
×	1	1	0	DATA Bus is in floating state.
×	×	×	1	"

CLK (Input)

The CLK input is used to generate internal device timing. No external input or output is referenced to CLK, but the frequency of CLK must be greater than 30 times the Receiver or Transmitter Data Bit Rates ($\overline{RxC}$ or $\overline{TxC}$) in Synchronous Operation, and greater than 4.5 times the Receiver Data Bit Rates ($\overline{RxC}$) in Asynchronous Operation.

RESET (Input)

A "high" level signal on this input forces the 8251A into an "Idle" mode. The device will remain at "Idle" untill a new set of Control Words is written into the 8251A to program its functional definition. Minimum RESET pulse width is 6 tcy.

- MODEM Control Signals

$\overline{DSR}$ (Input)

The $\overline{DSR}$ input signal is a general purpose, 1-bit inverting input port. Its condition can be tested by the CPU using a Status Read Operation. The $\overline{DSR}$ input is normally used to test MODEM conditions such as Data Set Ready signal.

$\overline{DTR}$ (Output)

The $\overline{DTR}$ output signal is a general purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction Word. The $\overline{DTR}$ output signal is normally used for MODEM control such as Data Terminal Ready or Rate Select signal.

$\overline{RTS}$ (Output)

The $\overline{RTS}$ output signal is a general purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction Word. The $\overline{RTS}$ output signal is normally used for MODEM control such as Request to Send signal.

$\overline{CTS}$ (Input)

A "low" level signal on this input enables the 8251A to transmit serial data, if the Tx Enable Bit in the Command Byte is set to a "one" (TxEN=1). If either a Tx Enable off (TxEN=0) or CTS off ($\overline{CTS}$=1) condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART, written prior to Tx Disable Command before shutting down.

• Transmit Control Signals

$\overline{TxC}$ (Input)

The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous Transmission Mode, the Baud Rate (1x) is equal to the $\overline{TxC}$ frequency. In Asynchronous Transmission Mode the baud rate is a fraction of the actual $\overline{TxC}$ frequency. A portion of the Mode Instruction selects this factor; it can be 1, 1/16 or 1/64 the $\overline{TxC}$.

For Example:

If Baud Rate equals 110 Baud,

$\overline{TxC}$ = 110 Hz (1x)

$\overline{TxC}$ = 1.76 KHz (16x)

$\overline{TxC}$ = 7.04 KHz (64x)

The falling edge of $\overline{TxC}$ shifts the serial data out of the 8251A.

TxD (Output)

This line is used to transmit the serial data. Serial output data on TxD is changed from parallel data to serial data in accordance with the format specified by the Control Words.
TxD line will be held in the marking state ('1' level) immediately on one of the followings.

- Master Reset
- Tx Disable (TxEN=0)
- CTS signal is high ($\overline{CTS}$=1)
- TxEMPTY signal is high (TxEMPTY=1)

TxRDY (Output)

This output informs the CPU that the transmitter is ready to accept a Data Character. The TxRDY output pin can be used as an interrupt to the system, since it is masked by Tx Disable(TxEN=0), or, for polled Operation, the CPU can check TxRDY using a Status Read Operation. TxRDY is automatically reset by the trailing edge of $\overline{WR}$ when a Data Character is loaded from the CPU.
The TxRDY pin output status (TxRDY (pin)) is different from the TxRDY status bit status (TxRDY (status bit)) as follows.

TxRDY (status bit) = (Transmit Data Buffer Empty)

TxRDY (pin) = (Transmit Data Buffer Empty)·(CTS=0)·(TxEN=1)

TxEMPTY (Output)

The TxEMPTY output will go "high" when the 8251A has no characters to send. It resets upon receiving a character from the CPU if the transmitter is enabled.

In Synchronous Mode, a "high" level signal on this output indicates that a Character has not been loaded and the SYNC Character or Characters are about to be or are being transmitted automatically as "fillers". TxEMPTY does not go "low" when the SYNC characters are being shifted out.

- Receive Control Signals

$\overline{RxC}$ (Input)

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the Baud Rate (1x) is equal to the actual frequency of $\overline{RxC}$. In Asynchronous Mode, the Baud Rate is a fraction of the actual $\overline{RxC}$ frequency. A portion of the Mode Instruction selects this factor; 1, 1/16 or 1/64 the $\overline{RxC}$.

For Example:

if Baud Rate equals 2400 Baud,

$\overline{RxC}$ = 2.4 KHz (1x)

$\overline{RxC}$ = 38.4 KHz (16x)

$\overline{RxC}$ = 153.6 KHz (64x)

Data is sampled into the 8251A on the rising edge of $\overline{RxC}$.

RxD (Input)

This line is used to receive the serial data. Serial input data on this line is changed to parallel data in accordance with the format specified by the Control Words, and then transfered to the Recive Data Buffer.

RxRDY (Output)

This output indicates that the 8251A contains a Data Character that is ready to be input to the CPU. RxRDY can be connected to the interrupt structure of the CPU, or, for Polled Operation, the CPU can check the condition of RxRDY using a Status Read Operation.
Rx Enable off both masks and holds RxRDY in the Reset Condition.

SYNDET/BD (Input/Output)

This pin is used for SYNDET in Synchronous Mode and may be used as either input or output, programmable through the Control Word. It is reset to output mode "low" upon RESET. When used as an Output (Internal Sync Mode), the SYNDET pin will go "high" to indicate that the 8251A has located the SYNC Characte in the Receive Mode. If the 8251A is programmed to use Double Sync Characters then SYNDET will go "high" in the middle of the last bit of the second SYNC Character. SYNDET is automatically reset upon a Status Read Operation. When used as an Input (External Sync Mode), a positive going signal will cause the 8251A to start assembling Data Characters on the rising edge of the next $\overline{RxC}$.

In Asynchronous Mode this pin is used for BD.
This output will go "high" whenever the receiver remains "low" through two consecutive Stop Bit Sequences (including the Start Bits, Data Bits, and Parity Bits). Break Detect may also be read as a Status Bit.
It is reset only upon a Master Chip Reset or Rx Data returning to a "one" state.
But, if the Rx Data returns to a "one" State during the last bit of the next character after the Break, Break Detect does not always reset.

- Power Supply
  - V_{CC} (Power)
    +5 Volt supply
  - GND (Power)
    0 Volt supply

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{CC}	Power Supply Voltage (with respect to GND)	-0.5V to 7.0V
V_{IN}	Input Voltage (with respect to GND)	-0.5V to 7.0V
V_{OUT}	Output Voltage (with respect to GND)	-0.5V to 7.0V
P_D	Power Dissipation (Ta=70°C)	1W
T_{solder}	Soldering Temperature (10 sec)	260°C
$T_{stg.}$	Storage Temperature	-55°C to 150°C
$T_{opr.}$	Operating Temperature	0°C to 70°C

D.C. CHARACTERISTICS T_{opr}=0°C to 70°C, V_{CC}=5V ±5%, GND=0V, Unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IL}	Input Low Voltage		-0.5	-	0.8	V
V_{IH}	Input High Voltage		2.2	-	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL}=2.2mA	-	-	0.45	V
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OFL}	Output Leak Current	$0.45V \leq V_{OUT} \leq V_{CC}$	-	-	±10	μA
I_{IL}	Input Leak Current	$0.45V \leq V_{IN} \leq V_{CC}$	-	-	±10	μA
I_{CC}	Power Supply Current	All Outputs="High"	-	-	100	mA

A.C. CHARACTERISTICS T_{opr}=0°C to 70°C, V_{CC}=5V±5%, GND=0V, Unless otherwise noted.

BUS READ CYCLE TIMING Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{AR}	$\overline{CS}$, C/$\overline{D}$ Set-up Time for $\overline{RD}$		50	-	-	ns
t_{RA}	$\overline{CS}$, C/$\overline{D}$ Hold Time for $\overline{RD}$		50	-	-	ns
t_{RR}	$\overline{RD}$ Pulse Width		250	-	-	ns
t_{RD}	Data Delay Time for $\overline{RD}$ Note 2)	C_L=150pF Note 3)	-	-	250	ns
t_{DF}	Data Hold Time for $\overline{RD}$		10	-	100	ns

BUS WRITE CYCLE TIMING Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{AW}	$\overline{CS}$, C/$\overline{D}$ Set-up Time for $\overline{WR}$		50	-	-	ns
t_{WA}	$\overline{CS}$, C/$\overline{D}$ Hold Time for $\overline{WR}$		50	-	-	ns
t_{WW}	$\overline{WR}$ Pulse Width		250	-	-	ns
t_{DW}	Data Set Up Time for $\overline{WR}$		150	-	-	ns
t_{WD}	Data Hold Time for $\overline{WR}$		50	-	-	ns
t_{RV}	Recovery Time Between WRITES	Note 4)	6	-	-	t_{cyc}

OTHER TIMING

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT	
t_{cyc}	Clock Period Note 5), 6)		320	-	1350	ns	
t_H	Clock High Level Width		140	-	t_{cyc}-90	ns	
t_L	Clcok Low Level Width		90	-	-	ns	
t_R, t_F	Clock Rise and Fall Time		-	-	20	ns	
t_{DTx}	TxD Delay Time from Falling Edge of $\overline{TxC}$		-	-	1	μs	
f_{Tx}	Transmitter Input Clock Frequency	1x Baud Rate	DC	-	64	kHz	
		16x Baud Rate	DC	-	310		
		64x Baud Rate	DC	-	615		
t_{TPH}	Transmitter Input Clock High Level Width	1x Baud Rate	12	-	-	t_{cyc}	
		16x,64x Baud Rate	1	-	-		
t_{TPL}	Transmitter Input Clock Low Level Width	1x Baud Rate	15	-	-	t_{cyc}	
		16x,64x Baud Rate	3	-	-		
f_{Rx}	Receiver Input Clock Frequency	1x Baud Rate	DC	-	64	kHz	
		16x Baud Rate	DC	-	310		
		64x Baud Rate	DC	-	615		
t_{RPH}	Receiver Input Clock High Level Width	1x Baud Rate	12	-	-	t_{cyc}	
		16x,64x Baud Rate	1	-	-		
t_{RPL}	Receiver Input Clock Low Level Width	1x Baud Rate	15	-	-	t_{cyc}	
		16x,64x Baud Rate	3	-	-		
t_{TxRDY}	TxRDY Pin Delay Time from Center of Last Bit		-	-	8	t_{cyc}	Note 7
$t_{TxRDY\ CLEAR}$	TxRDY Clear Delay Time from Trailing Edge of $\overline{WR}$		-	-	6	t_{cyc}	Note 7
t_{RxRDY}	RxRDY Pin Delay Time from Center of Last Bit		-	-	24	t_{cyc}	Note 7
$t_{RxRDY\ CLEAR}$	RxRDY Clear Delay Time from Leading Edge of $\overline{RD}$		-	-	6	t_{cyc}	Note 7
t_{IS}	Internal SYNDET Delay Time from Rising Edge of $\overline{RxC}$		-	-	24	t_{cyc}	Note 7
t_{ES}	External SYNDET Set-Up Time fore Falling Edge of $\overline{RxC}$		16	-	-	t_{cyc}	Note 7
$t_{TxEMPTY}$	TxEMPTY Delay Time from Center of Last Bit		20	-	-	t_{cyc}	Note 7
t_{WC}	Control Delay Time from Rising Edge of $\overline{WR}$ (TxEN, $\overline{DTR}$, $\overline{RTS}$)		8	-	-	t_{cyc}	Note 7
t_{CR}	$\overline{DSR}$, $\overline{CTS}$ Set-Up Time for $\overline{RD}$		20	-	-	t_{cyc}	Note 7

Notes:

1) AC Test Conditions: Output measuring point V_{OH}=2.0V, V_{OL}=0.8V
Input supply level V_{IH}=2.4V, V_{IL}=0.45V

2) Assumes that Address is valid before the falling edge of $\overline{RD}$.

3) C_L means load capacitance.

4) This recovery time is defined only for Mode Initialization. Write Data is allowed only when TxRDY=1. Recovery Time between Writes for Asynchronous Mode is 8 tcy and for Synchronous Mode is 16 tcy.

5) The TxC and RxC frequencies have the following limitations with respect to CLK:

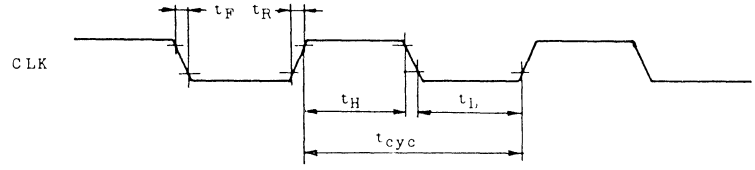
For 1x Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(30tcy)$
For 16x and 64x Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(4.5tcy)$

6) Minimum Reset Pulse Width is 6 tcy. System Clock must be running during Reset.

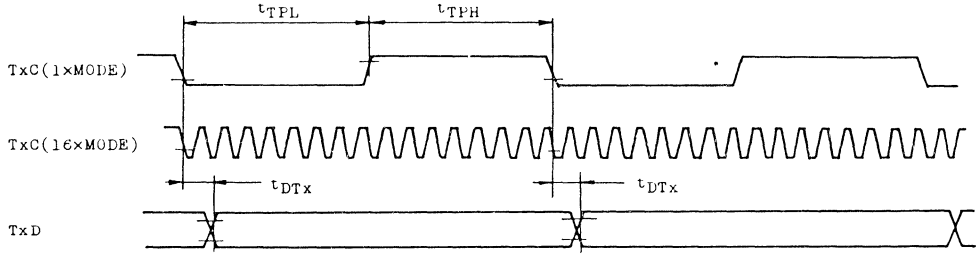
7) Status up data can have a maximum delay of 28 clock periods from the event affecting the status.

TIMING WAVEFORMS

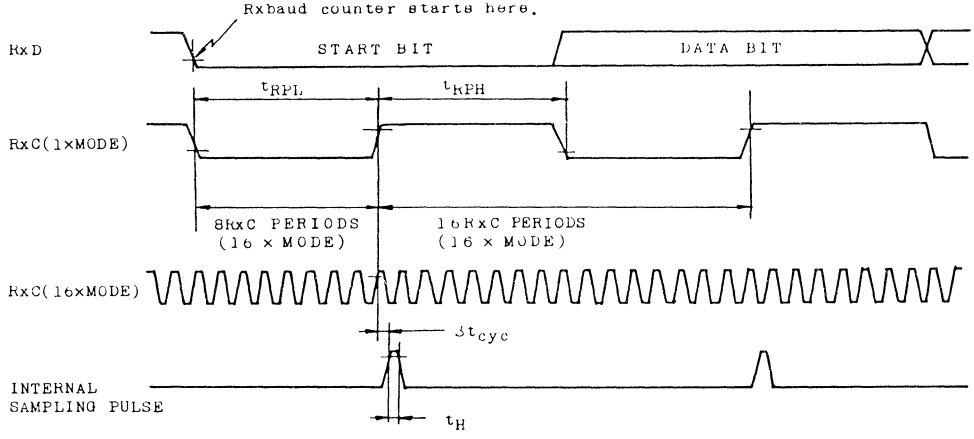
SYSTEM CLOCK INPUT



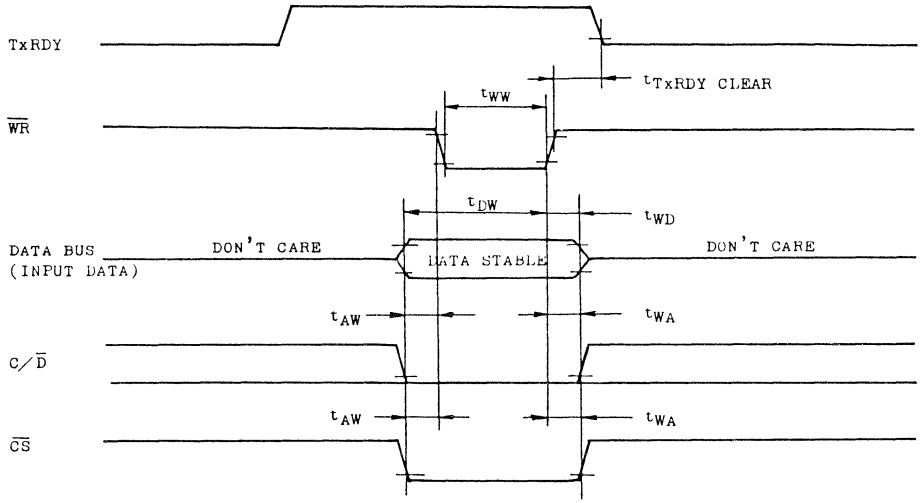
TRANSMITTER CLOCK AND DATA



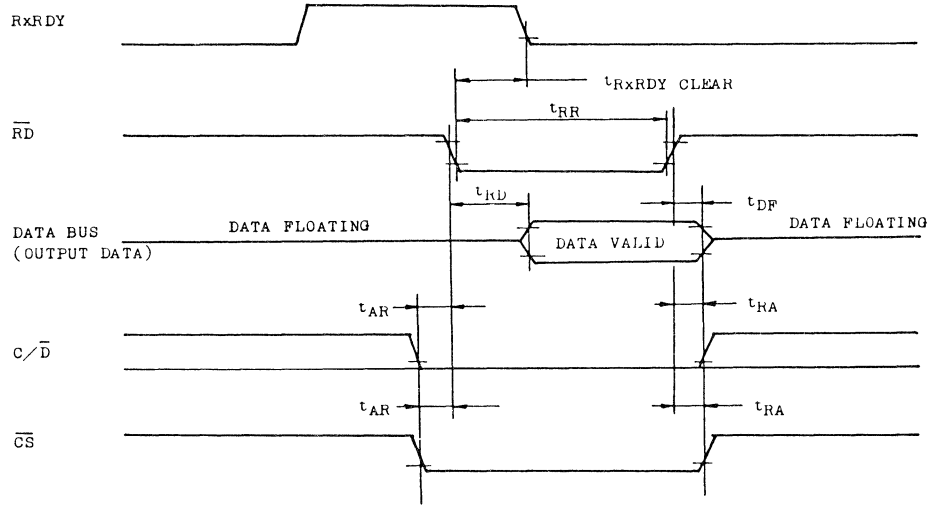
RECEIVER CLOCK AND DATA



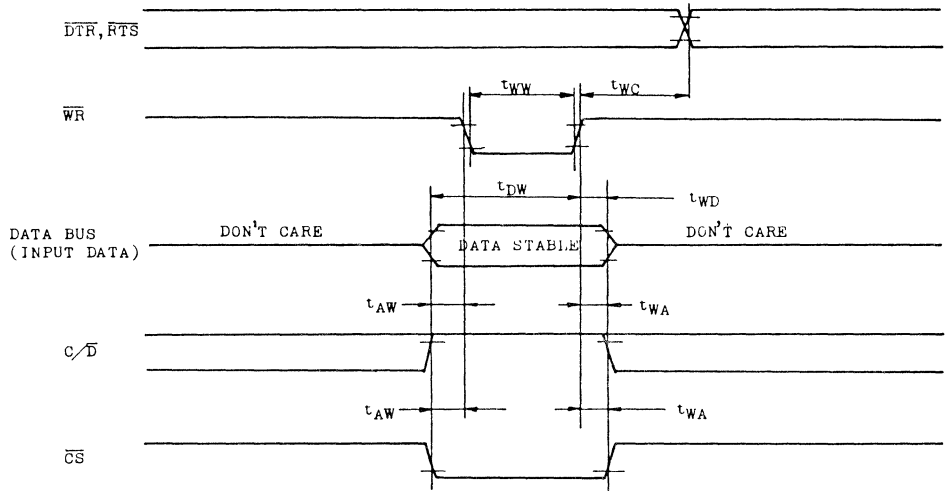
WRITE DATA CYCLE (CPU → 8251A)



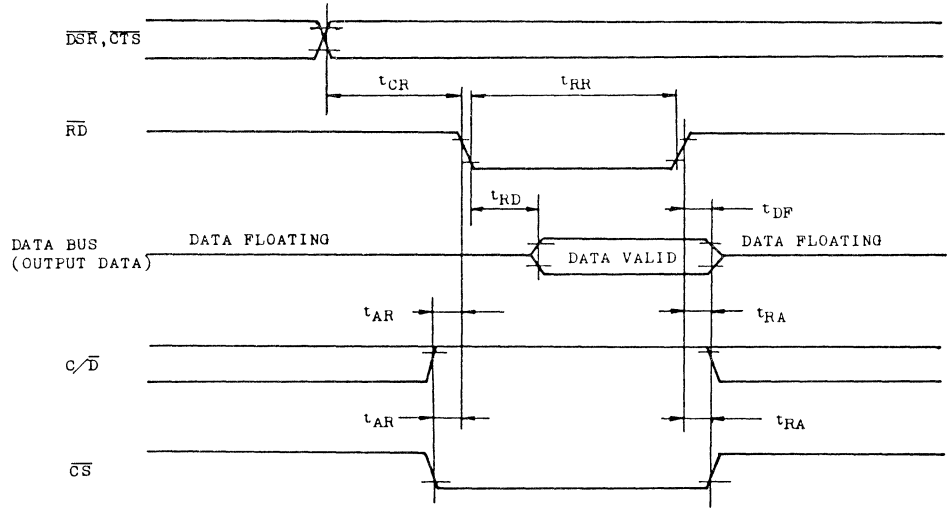
READ DATA CYCLE (8251A → CPU)



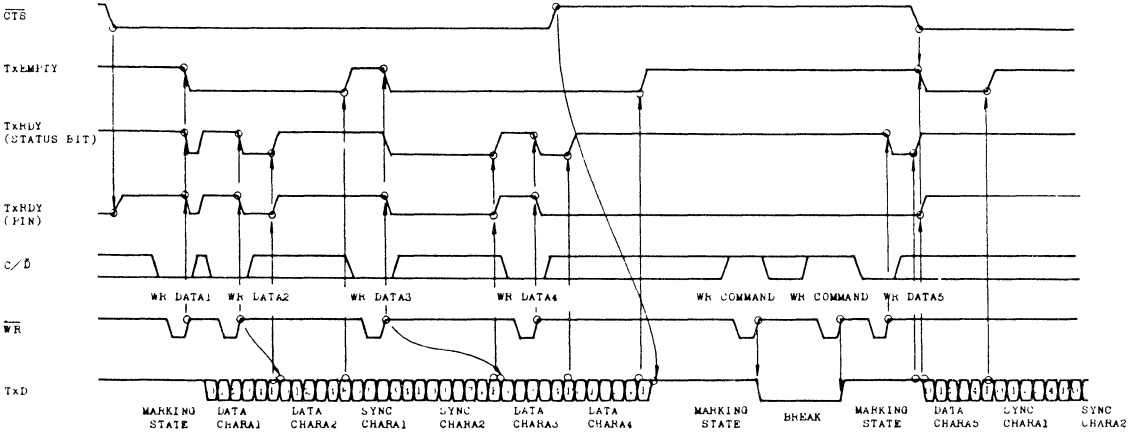
WRITE CONTROL OR OUTPUT PORT CYCLE (CPU → 8251A)



READ CONTROL OR INPUT PORT CYCLE (8251A → CPU)

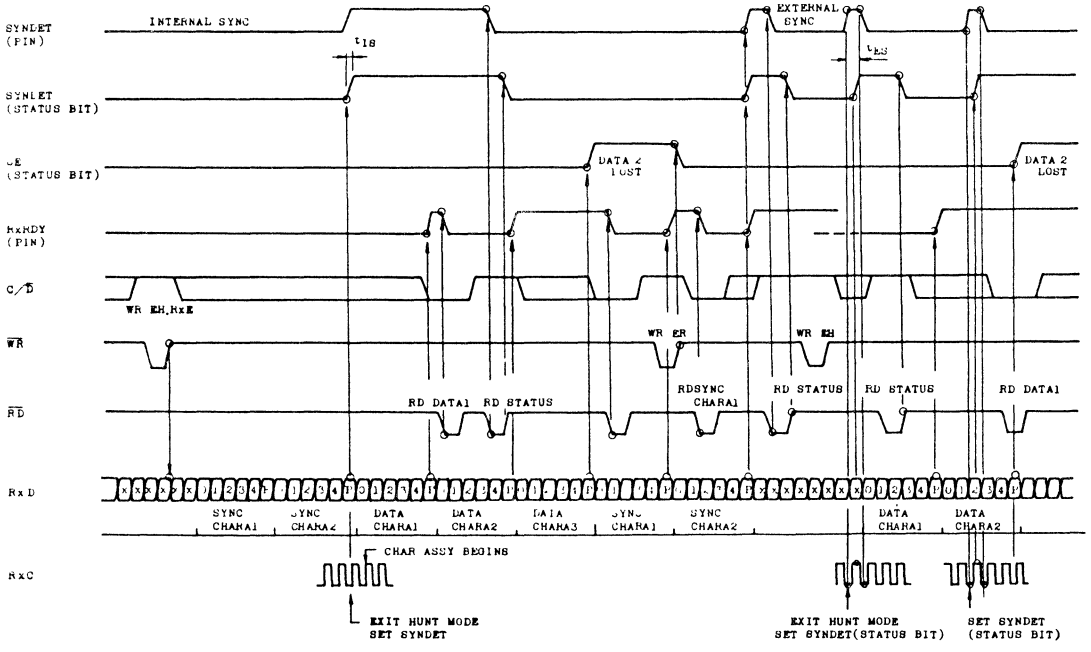


TRANSMITTER CONTROL AND FLAG TIMING (SYNC MODE)



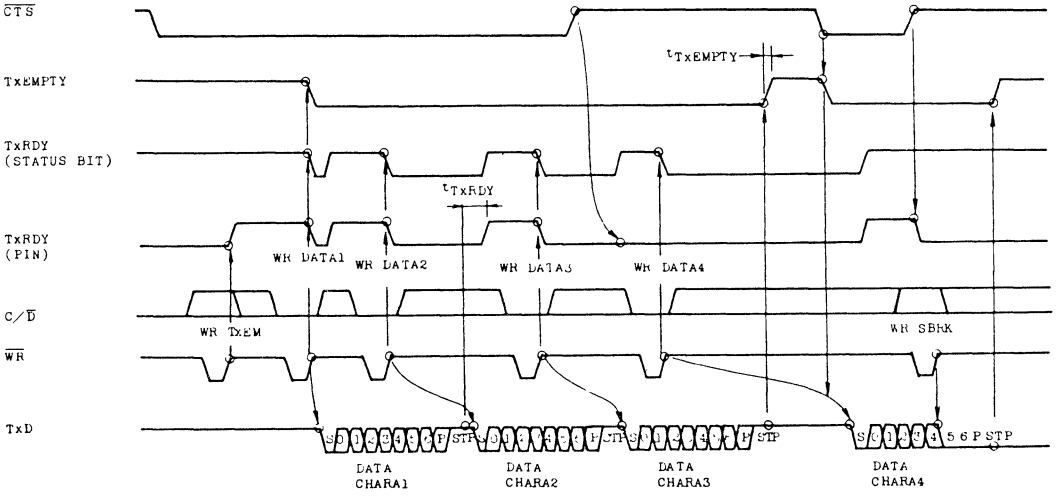
EXAMPLE FORMAT : 5 BIT CHARACTER WITH PARITY 2 SYNC CHARACTERS.

RECEIVER CONTROL AND FLAG TIMING (SYNC MODE)



EXAMPLE FORMAT : 5 BIT CHARACTER WITH PARITY 2 SYNC CHARACTERS.

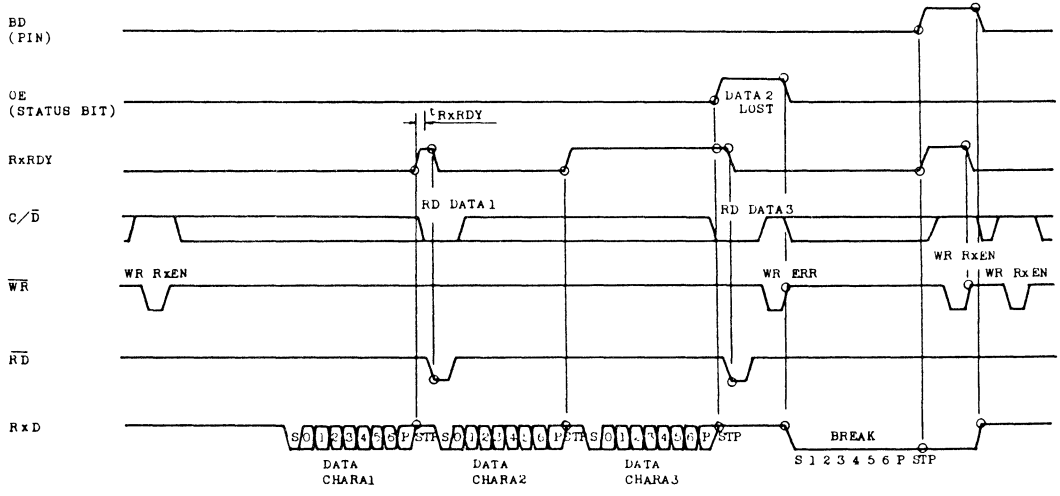
TRANSMITTER CONTROL AND FLAG TIMING (ASYNC MODE)



EXAMPLE FORMAT : 7 BIT CHARACTER & 2 STOP BITS.

Note : TxRDY(PIN) = (Transmit Data Buffer is empty) · (TxEN=1) · (CTS=0)
TxRDY(STATUS BIT) = (Transmit Data Buffer is empty)

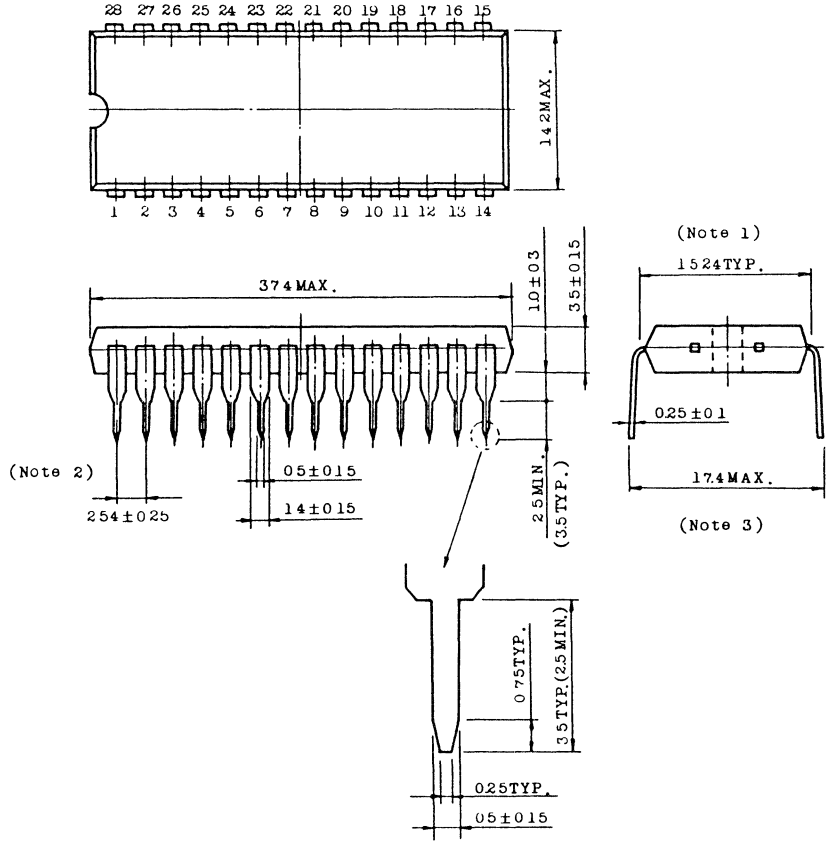
RECEIVER CONTROL AND FLAG TIMING (ASYNC MODE)



EXAMPLE FORMAT : 7 BIT CHARACTER WITH PARITY & 2 STOP BITS.

OUTLINE DRAWING

Unit in mm



Note: 1. This dimension is measured at the center of bending point of leads.

2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoritical positions with respect to No.1 and No.28 leads.

3. This dimension is to outside of leads.

TOSHIBA MOS TYPE DIGITAL INTEGRATED CIRCUIT
TMP82C53P-2/TMP82C53F-2
SILICON MONOLITHIC CMOS SILICON GATE

PROGRAMMABLE INTERVAL TIMER

GENERAL DESCRIPTION

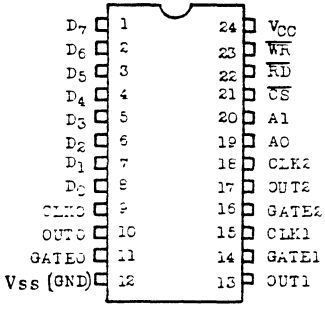
The TMP82C53P-2/F-2(hereinafter referred to as TMP82C53) is a programmable counter/timer. It is organized as 3 independent 16 bit counters, each operates with a count rate of up to 5MHz. All modes of operation are software programmable.

FEATURES

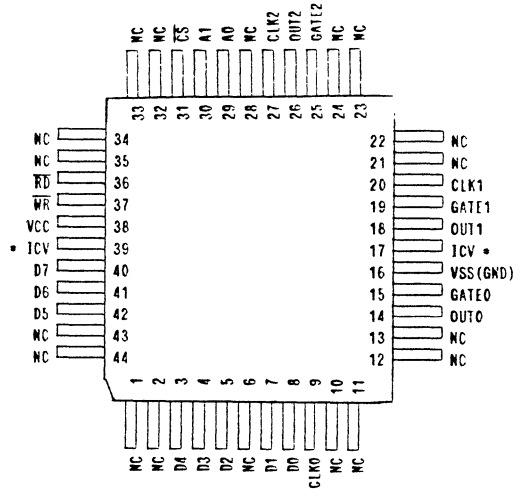
- o Count Binary or BCD
- o 3 Independent 16 Bit Counters
- o Single +5V Supply
- o Count rate DC to 5MHz
- o 6 programmable Counter Mode
- o Low Power Consumption 2mA TYP. @5MHz
- o Extended Operating Temperature $-40^{\circ}C$ to $85^{\circ}C$

PIN CONNECTIONS

TMP82C53P-2



TMP82C53F-2



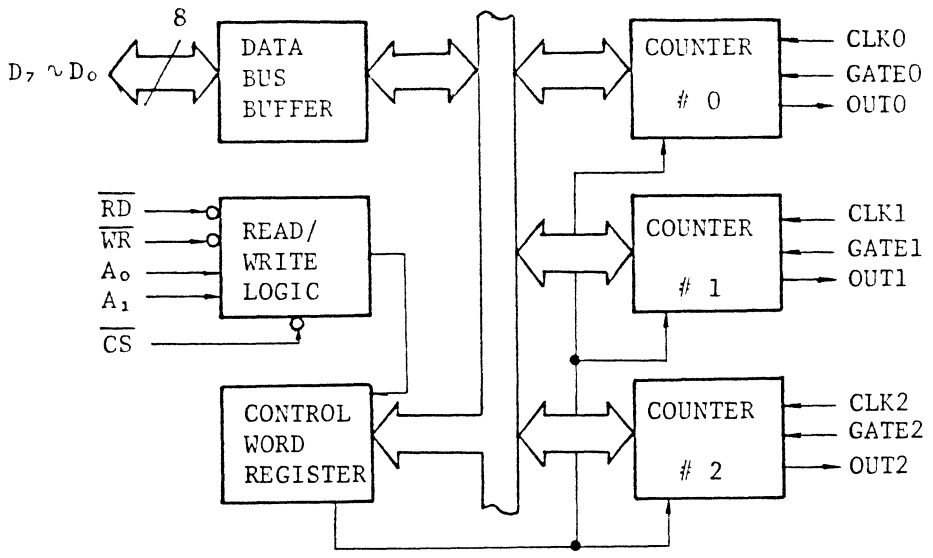
PIN NAMES

D7 - D0	Data Bus (8 bit)
CLK N	Counter Clock Input
GATE N	Counter Gate Input
OUT N	Counter Output
$\overline{RD}$	Read Counter
$\overline{WR}$	Write Counter
$\overline{CS}$	Chip Select
A0 - A1	Counter Select
VCC	+5V
Vss	Ground (0V)

*) ICV (Pin17 and Pin39) must be connected with Vcc or must be OPEN

NC : No Connection

BLOCK DIAGRAM



PIN NAMES AND PIN DESCRIPTION

Vss(GND) (Power Supply)
Ground.

VCC (Power Supply)
+5V during operation.

$\overline{CS}$ (Input)
A low on this pin enables read and write communication between the CPU and the TMP82C53. The $\overline{CS}$ input has no effect upon the actual operation of the counters.

A0, A1 (Input)
These inputs acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. This pin is used to select one of the three counters to be operated on and to address the control word register for mode selection.

$\overline{WR}$ (Input)
A low on this pin when $\overline{CS}$ is low enables the TMP82C53 to accept mode information or loading counters from the CPU.

$\overline{RD}$ (Input)
A low on this pin when $\overline{CS}$ is low enables the TMP82C53 to release a counter value onto the data bus for the CPU.

D0 - D7 (Input/Output)
Bidirectional 8bit Data Bus. Mode information and the count values are transferred via this data bus.

CLK0 - CLK2 (Input)
Clock inputs to counters. Falling edge on this pin enable the counter to count down.

GATE0 - GATE2 (Input)
Gate inputs to counters. The function of this pin differs by the mode selection of counter operation.

Out0 - Out2 (Output)
Outputs from the counters. The output signal from this pin differs by the mode selection of counter operation.

FUNCTIONAL DESCRIPTION

[Block Description]

Data Bus Buffer
This is 3-state, bidiractional, 8 bit buffer used for interfacing the TMP82C53 to the system data bus. The Data Bus Buffer has three functions as follows. Programming the MODEs of the TMP82C53, Loading the count registers, and Reading the count values.

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and in turn generates control signals for overall device operation.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	
0	1	0	0	0	Load Counter #0
0	1	0	0	1	Load Counter #1
0	1	0	1	0	Load Counter #2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter #0
0	0	1	0	1	Read Counter #1
0	0	1	1	0	Read Counter #2
0	0	1	1	1	Data Bus is in High-impedance state
1	x	x	x	x	
0	1	1	x	x	

Control Word Register

The Control Word Register is selected when A0, A1 are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operational MODE of each counter, selection of binary or BCD counting and the loading of each count register. No reading of the contents of the control Word Register is available.

Counter #0, Counter #1, Counter #2

These three blocks are identical so only a single counter will be described. Each counter consists of a signle, 16 bit, presettable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of MODES (Six MODES: MODE 0 to MODE 5) stored in the Control Word Register. Also the control word handles the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications. Special commands and logic are included in the TMP82C53 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

[MODE Definition]

Mode 0: Interrupt on Terminal Count.

The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached the output will go high and remain high until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count has been reached.

Rewriting a counter register during counting results in the following:

(1) Write 1st byte stops the current counting.
(2) Write 2nd byte starts the new count.

MODE 1: Programmable One Shot.

The output will go low on the count following the rising edge of the gate input.

The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

MODE 2: Rate Generator

Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The gate input, when low, will force the output high. When the gate input goes high, the count will start from the initial count. Thus, the gate input can be used to synchronize the counter.

When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

MODE 3: Square Wave Rate Generator

Similar to MODE 2 except that the output will remain high until one half the count has been completed (for even numbers) and go low for the other half of the count.

This is accomplished by decrementing the counter by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the clock by 2. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by 2 until timeout. Then the whole process is repeated. In this way, if the count is odd, the output will be high for (N + 1)/2 counts and low for (N - 1)/2 counts.

MODE 4: Software Triggered Strobe

After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

If the count register is reloaded between output pulses, counting will continue from the new value. The count will be inhibited while the gate input is low. Reloading the counter register will restart counting beginning with the new number.

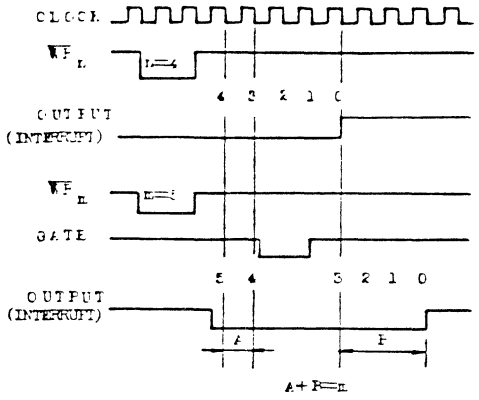
MODE 5: Hardware Triggered Strobe

The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

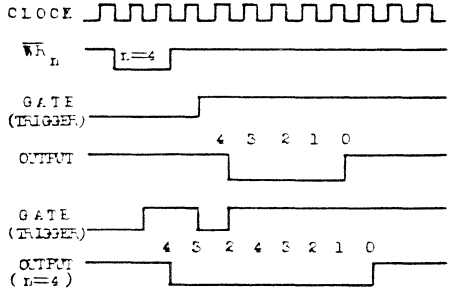
Status / Modes	Low or Going Low	Rising	High
0	Disables counting	-	Enable counting
1	-	(1) Initiates counting (2) Resets output after next clock	-
2	(1) Disables counting (2) Sets output immediately High	(1) Reloads counter (2) Initiates counting	Enable counting
3	(1) Disables counting (2) Sets output immediately High	Initiates counting	Enable counting
4	Disables counting	-	Enable counting
5	-	Initiates counting	-

Figure 1. Gate Pin Operations

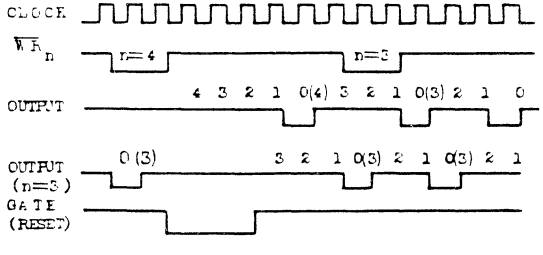
MODE 0: Interrupt on Terminal Count



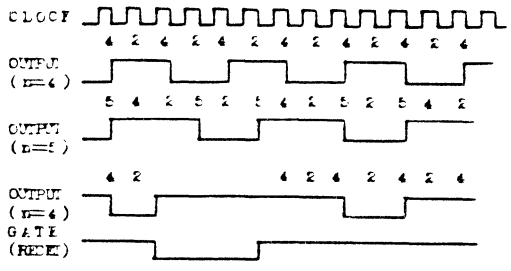
MODE 1: Programmable One-Shot



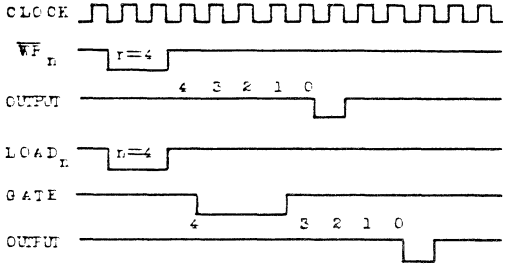
MODE 2: Rate Generator



MODE 3: Square Wave Generator



MODE 4: Software-Triggered Strobe



MODE 5: Hardware-Triggered Strobe

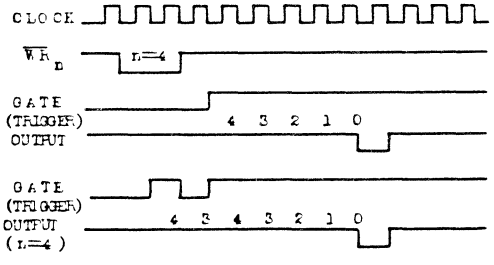


Figure 2. TMP82C53 Timing Diagrams

PROGRAMMING the TMP82C53

All of the MODEs for each counter are programmed by the systems software by simple I/O operations.

Each counter of the TMP82C53 is individually programmed by writing a control word into the Control Word Register. (CS=0, A0=A1=1, WR=0)

	D7	D6	D5	D4	D3	D2	D1	D0	
	SC1	SC0	RL1	RL0	M2	M1	M0	BCD	
Select Counter 0	0	0						0	Binary Counter (16-bits)
Select Counter 1	0	1							
Select Counter 2	1	0						1	BCD Counter (4 Decades)
Illegal	1	1							

Counter Latching Operation	0	0	0	0	0	MODE 0
Read/Load least significant byte only	0	1	0	0	1	MODE 1
			x	1	0	MODE 2
Read/Load most significant byte only	1	0	x	1	1	MODE 3
			1	0	0	MODE 4
Read/Load least significant byte first then most significant byte	1	1	1	0	1	MODE 5

Note. SC: Select Counter, RL: Read/Load, M: Mode, BCD: Binary Coded Decimal.

Figure 3. Control Word Format

The programmer must write out to the TMP82C53 a MODE Control Word and the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

The actual order of the programming is quite flexible. Writing out of the MODE Control Word can be in any sequence of counter selection.

The loading of the Count Register with actual count value, however, must be done in exactly the sequence programmed in the MODE Control Word (RL0, RL1).

Counter Loading

The count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits), followed by a rising edge and a falling edge of the clock.

The count register must be loaded with the number of bytes programmed in the MODE Control Word. The one or two bytes to be loaded in the count register do not have to follow the associated MODE Control Word. They can be programmed at any time following the MODE Control Word loading as long as the correct number of bytes is loaded in order.

All counters are down counters. Loading all zeros will result in the maximum count (2^{16} for Binary or 10^4 for BCD). In MODE 0 and MODE 4, the new count will not restart until the load has been completed.

Read Operations

The TMP82C53 contains logic that will allow the programmer to easily read the contents of any of the three counters without distrubing the actual count in progress.

There are two methods that the programmer can use to read the value of the counters. The first method involves the use of simple I/O read operations. By controlling the A0, A1 inputs to the TMP82C53, the programmer can select the counter to be read. The only requirement with this method is that in order to assure a stable count reading the actual operation of the selected counter must be inhibited either by controlling the Gate input or by external logic that inhibits the clock input.

The contents of the counter selected must be read in the sequence programmed in the MODE Control Word (RL0, RL1). When RL0, RL1 is 11. First I/O Read contains the least significant byte (LSB), second I/O Read contains the most significant byte (MSB), and the two bytes must be read before any loading WR command can be sent to the same counter.

The second method allows the programmer to read the contents of any counter without effecting or distrubing the counting operation. When the programmer wishes to read the contents of a selected counter "On the fly", he loads the MODE register with a special code which latches the present count value into a storage register so that its contents contain an accurate, stable quantity. The programmer then issues a normal read command to the selected counter. The contents of the latched register must be read in the sequence programmed in the MODE Control Word (RL0, RL1). This commands has no effect on the counters mode.

Program Example

```
Set up sequence      MVI  A, 00110000B ...  #0, LSB-MSB, MODE 0, Binary
for counter #0       OUT  CWAD          ...  The address of Control Word
                                             Register
                     MVI  A, 53H        ...  LSB for counter #0
                     OUT  CNTO          ...  The address of counter #0
                     MVI  A, 82H        ...  MSB for counter #0
                     OUT  CNTO          ...  The address of counter #0
                      :
                      :
READ the contents    MVI  A, 0000XXXXB
of counter #0        OUT  CWAD          ...  Latching count
                     IN   CNTO          ...  Read LSB of counter #0
                     MOV  L, A
                     IN   CNTO          ...  Read MSB of counter #0
                     MOV  H, A
                      :
                      :
RELOAD to            MVI  A, 28H
counter #0           OUT  CNTO          ...  Load LSB for counter #0
                     MVI  A, 53H
                     OUT  CNTO          ...  Load MSB for counter #0
```

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
VCC	Vcc Supply Voltage (with respect to Vss[GND])	-0.5V to +7.0V
VIN	Input Voltage (with respect to Vss [GND])	-0.5V to Vcc+0.5V
VOUT	Output Voltage (with respect to Vss [GND])	-0.5V to Vcc+0.5V
PD	Power Dissipation	250 mW
Tsol	Soldering Temperature (Soldering Time 10 sec)	260 °C
Tstg	Storage Temperature	-65°C to +150°C
Topr	Operating Temperature	-40°C to 85°C

DC CHARACTERISTICS (Ta = -40 to + 85°C, Vcc = 5V ± 10%, Vss(GND)=0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage		-0.5		0.8	V
VIH	Input High Voltage		2.2		Vcc +0.5	V
VOL	Output Low Voltage	IOL=2.2 mA			0.45	V
VOH1	Output High Voltage	IOH=-400 uA	2.4			V
VOH2	Output High Voltage	IOH=-100 uA	Vcc -0.8			V
IIL	Input Leak Current	0V≦VIN≦Vcc			±10	uA
IOFL	Output Leak Current	0.45V≦VOUT≦Vcc			±10	uA
ICC1	Operating Supply Current	CLK=5MHz VIH=Vcc-0.2V VIL=0.2V		2	5	mA
ICC2	Stand-by Supply Current	CLK=DC VIH=Vcc-0.2V VIL=0.2V			10	uA

AC CHARACTERISTICS
(Ta = -40°C to +85°C, Vcc = 5.0V±10%, Vss(GND)=0V

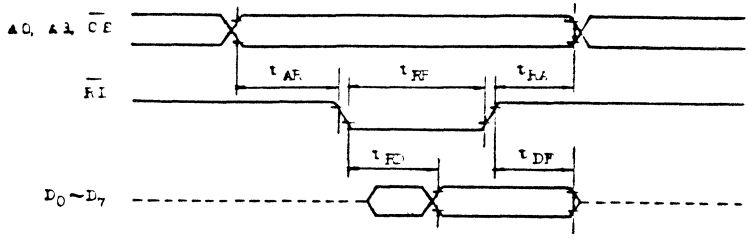
ABBR.	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
tAR	Address Set-up Time ($\overline{RD}$)		30			ns
tRA	Address Hold Time ($\overline{RD}$)		0			ns
tRR	$\overline{RD}$ Pulse Width		180			ns
tRD	Valid Data ($\overline{RD}$)	CL = 150 pF			140	ns
tDF	Data Floating ($\overline{RD}$)		10		85	ns
tRV	Recovery Time		250			us
tAW	Address Set-up Time ($\overline{WR}$)		0			ns
tWA	Address Hold Time ($\overline{WR}$)		30			ns
tWW	$\overline{WR}$ Pulse Width		150			ns
tDW	Data Set-up time ($\overline{WR}$)		100			ns
tWD	Data Hold Time ($\overline{WR}$)		30			ns
tCLK	Clock Period		200		DC	ns
tPWH	CLK High Pulse Width		80			ns
tPWL	CLK Low Pulse Width		65			ns
tGW	GATE Width High		50			ns
tGL	CATE Width Low		50			ns
tGS	GATE Set-up Time (CLK)		70			ns
tGH	GATE Hold Time (CLK)		50			ns
tOD	Output Delay From(CLK)	CL = 150 pF			200	ns
tODG	Output Delay From(GATE)	CL = 150 pF			200	ns

Note: AC timings measurements are referenced to VIL=0.45V, VIH=2.4V, VOL=0.8V, VOH=2.2V.

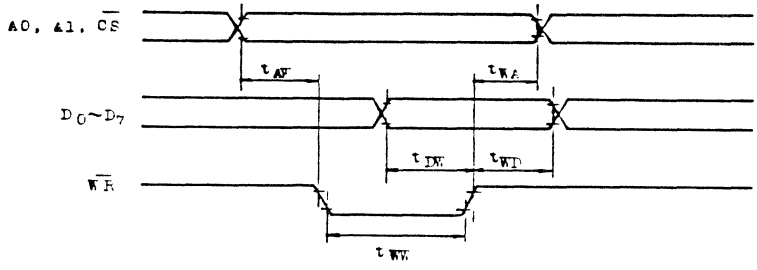
INPUT CAPACITANCE (Ta=25°C, Vcc=Vss(GND)=0V)

SYMNOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CI	Input Capacitance	fC = 1 MHz Unmeasured pins, 0V			10	pF
CI/O	Input/Output Capacitance				20	

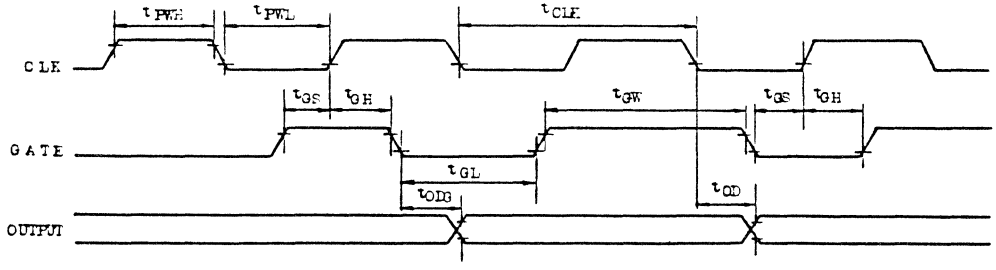
READ TIMING



WRITE TIMING



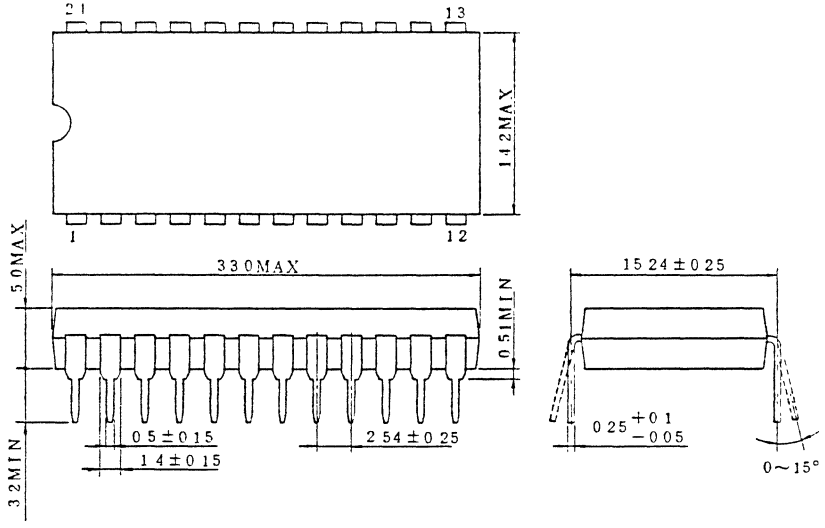
CLOCK & GATE TIMING



EXTERNAL DIMENSION VIEW

24 Pins PRASTIC DIP

Unit in mm

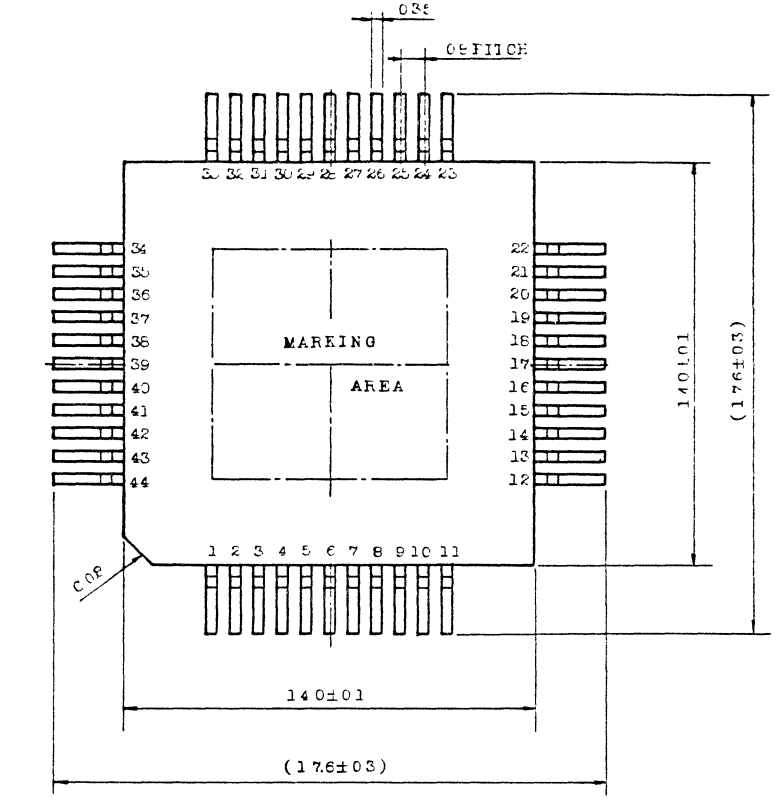


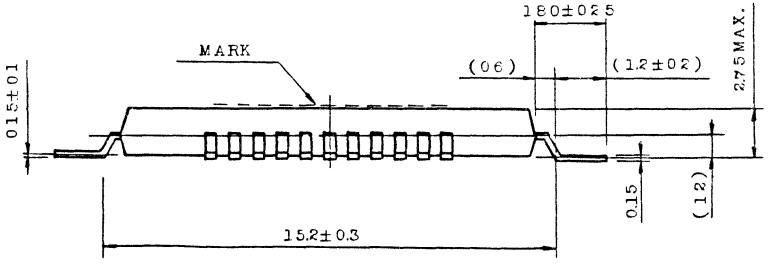
Note) Lead pitch is 2.54mm and tolerance is ±0.25mm against theoretical center of each lead that is obtained on the basis of No.1 and No.24 leads.

EXTERNAL DIMENSION VIEW

44 Pins MINI FULATPACKAGE

Unit in mm





PROGRAMMABLE INTERVAL TIMER

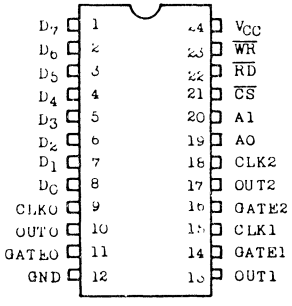
GENERAL DESCRIPTION

The TMP8253-5 is a programmable counter/timer chip designed for use as the TLCS-85A microcomputer peripheral. It is organized as 3 independent 16 bit counters, each operates with a count rate of up to 2.5MHz. All modes of operation are software programmable.

FEATURES

- Count Binary or BCD
- 3 Independent 16 Bit Counters
- Single +5V Supply
- Count rate DC to 2.5MHz
- 6 programmable Counter Modes
- Compatible with Intel's 8253-5

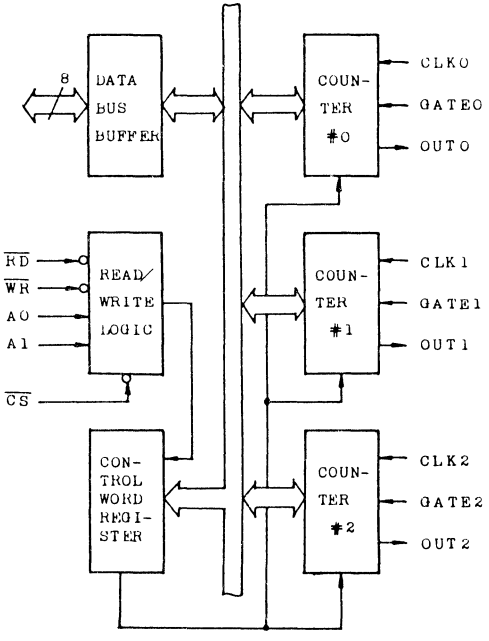
PIN CONNECTIONS



PIN NAMES

$D_7 \sim D_0$	Data Bus (8 bit)
CLK N	Counter Clock Input
GATE N	Counter Gate Input
OUT N	Counter Output
$\overline{RD}$	Read Counter
$\overline{WR}$	Write Counter
$\overline{CS}$	Chip Select
$A_0 \sim A_1$	Counter Select
VCC	+5V
GND	Ground (0V)

BLOCK DIAGRAM



PIN NAMES AND PIN DESCRIPTION

GND (Power Supply)

Ground.

V_{CC} (Power Supply)

+5V during operation.

$\overline{CS}$ (Input)

A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the TMP8253-5. The $\overline{CS}$ input has no effect upon the actual operation of the counters.

A0, A1 (Input)

These inputs acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. This pin is used to select one of the three counters to be operated on and to address the control word register for mode selection.

$\overline{WR}$ (Input)

A low on this pin when $\overline{CS}$ is low enables the TMP8253-5 to accept mode information or loading counters from the CPU.

$\overline{RD}$ (Input)

A low on this pin when $\overline{CS}$ is low enables the TMP8253-5 to release a counter value onto the data bus for the CPU.

D0 ∿ D7 (Input/Output)

Bidirectional Data Bus. Mode information, the information loading counter or the count values are transfered via this data bus.

CLK0 ∿ CLK2 (Input)

Clock inputs to counters. Falling edge on this pin enables the counter to count down.

GATE0 ∿ GATE2 (Input)

Gate inputs to counters. The function of this pin differs by the mode selection of counter operation.

Out0 ∿ Out2 (Output)

Outputs from the counters. The output signal from this pin differs by the mode selection of counter operation.

FUNCTIONAL DESCRIPTION

[Block Description]

Data Bus Buffer

This is 3-state, bi-directional, 8 bit buffer used for interfacing the TMP8253-5 to the system data bus. The Data Bus Buffer has three functions as follows. Programming the MODEs of the TMP8253-5, Loading the count registers, and Reading the count values.

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and in turn generates control signals for overall device operation.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Load Counter #0
0	1	0	0	1	Load Counter #1
0	1	0	1	0	Load Counter #2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter #0
0	0	1	0	1	Read Counter #1
0	0	1	1	0	Read Counter #2
0	0	1	1	1	Data Bus is in High-impedance state
1	x	x	x	x	
0	1	1	x	x	

Control Word Register

The Control Word Register is selected when A0, A1 are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operational MODE of each counter, selection of binary or BCD counting and the loading of each count register. No reading of the contents of the Control Word Register is available.

Counter #0, Counter #1, Counter #2

These three blocks are identical so only a single counter will be described. Each counter consists of a single, 16 bit, presettable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of MODES (Six MODES: MODE 0 to MODE 5) stored in the Control Word Register. Also the control word handles the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications. Special commands and logic are included in the TMP8253-5 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

[MODE Definition]

MODE 0: Interrupt on Terminal Count.

The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached the output will go high and remain high until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count has been reached.

Rewriting a counter register during counting results in the following:

(1) Write 1st byte stops the current counting.

(2) Write 2nd byte starts the new count.

MODE 1: Programmable One Shot.

The output will go low on the count following the rising edge of the gate input.

The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

MODE 2: Rate Generater

Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Thus, the gate input can be used to synchronize the counter.

When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

MODE 3: Square Wave Rate Generator.

Similar to MODE 2 except that the output will remain high until one half the count has been completed (for even numbers) and go low for the other half of the count.

This is accomplished by decrementing the counter by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the clock by 2. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by 2 until timeout. Then the whole process is repeated. In this way, if the count is odd, the output will be high for $(N + 1)/2$ counts and low for $(N - 1)/2$ counts.

MODE 4: Software Triggered Strobe.

After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

If the count register is reloaded between output pulses, counting will continue from the new value. The count will be inhibited while the gate input is low. Reloading the counter register will restart counting beginning with the new number.

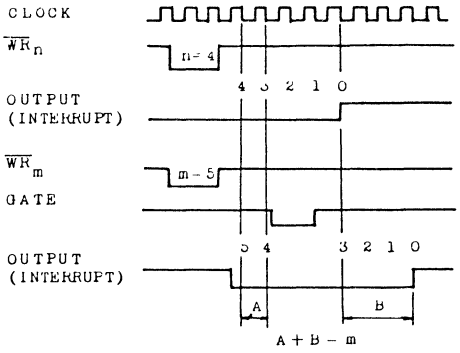
MODE 5: Hardware Triggered Strobe.

The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

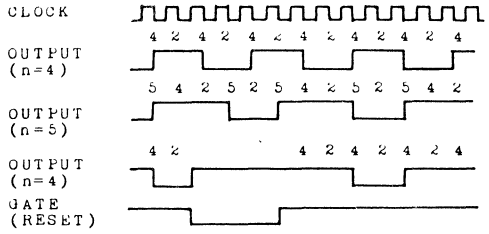
Status / Modes	Low or Going Low	Rising	High
0	Disables counting	-	Enables counting
1	-	(1) Initiates counting (2) Resets output after next clock	-
2	(1) Disables counting (2) Sets output immediately High	(1) Reloads counter (2) Initiates counting	Enables counting
3	(1) Disables counting (2) Sets output immediately High	Initiates counting	Enables counting
4	Disables counting	-	Enables counting
5	-	Initiates counting	-

Figure 1. Gate Pin Operations

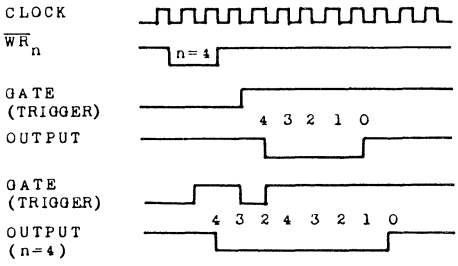
MODE 0: Interrupt on Terminal Count



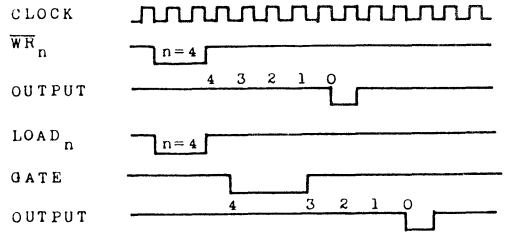
MODE 3: Square Wave Generator



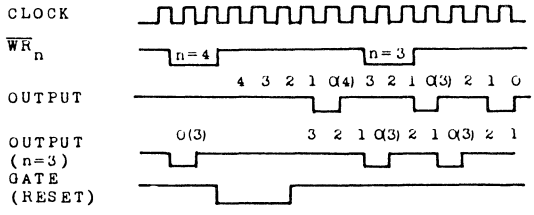
MODE 1: Programmable One-Short



MODE 4: Software-Triggered Strobe



MODE 2: Rate Generator



MODE 5: Hardware-Triggered Strobe

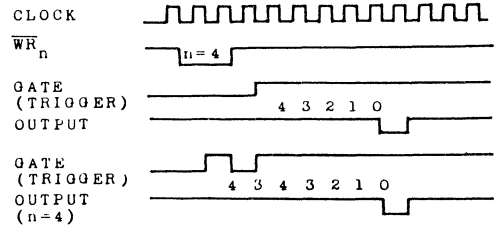
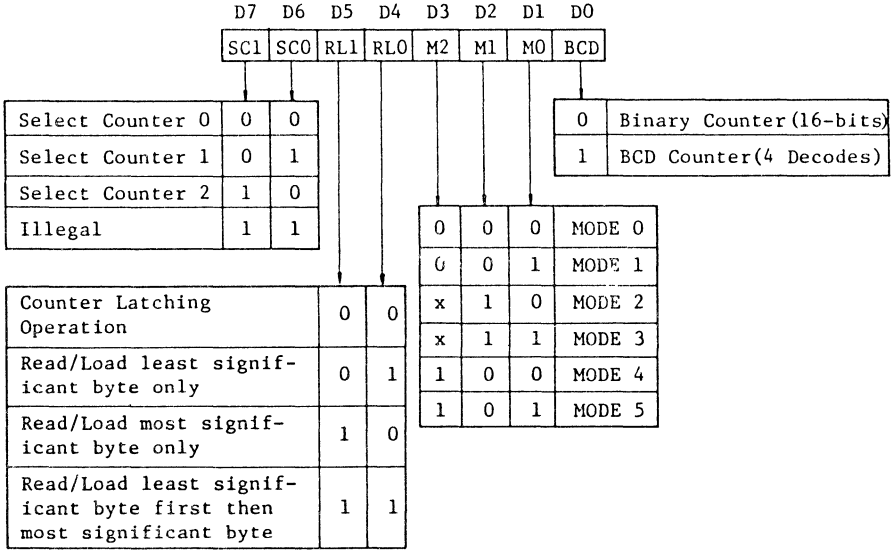


Figure 2. TMP8253-5 Timing Diagrams

PROGRAMMING the TMP8253-5

All of the MODEs for each counter are programmed by the systems software by simple I/O operations.

Each counter of the TMP8253-5 is individually programmed by writing a control word into the Control Word Register. ($\overline{CS}$=0, A0=A1=1, $\overline{WR}$=0)



NOTE. SC: Select Counter, RL: Read/Load, M: Mode,
BCD: Binary Coded Decimal.

Figure 3. Control Word Format

The programmer must write out to the TMP8253-5 a MODE Control Word and the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

The actual order of the programming is quite flexible. Writing out of the MODE Control Word can be in any sequence of counter selection.

The loading of the Count Register with actual count value, however, must be done in exactly the sequence programmed in the MODE Control Word (RL0, RL1)

Counter Loading

The count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits), followed by a rising edge and a falling edge of the clock.

The count register must be loaded with the number of bytes programmed in the MODE Control Word. The one or two bytes to be loaded in the count register do not have to follow the associated MODE Control Word. They can be programmed at any time following the MODE Control Word loading as long as the correct number of bytes is loaded in order.

All counters are down counters. Loading all zeros will result in the maximum count (2^{16} for Binary or 10^4 for BCD). In MODE 0 and MODE 4, the new count will not restart until the load has been completed.

Read Operations

The TMP8253-5 contains logic that will allow the programmer to easily read the contents of any of the three counters without disturbing the actual count in progress.

There are two methods that the programmer can use to read the value of the counters. The first method involves the use of simple I/O read operations. By controlling the A0, A1 inputs to the TMP8253-5, the programmer can select the counter to be read. The only requirement with this method is that in order to assure a stable count reading the actual operation of the selected counter must be inhibited either by controlling the Gate input or by external logic that inhibits the clock input.

The contents of the counter selected must be read in the sequence programmed in the MODE Control Word (RL0, RL1). When RL0, RL1 is 11. First I/O Read contains the least significant byte (LSB), second I/O Read contains the most significant byte (MSB), and the two bytes must be read before any loading WR command can be sent to the same counter.

The second method allows the programmer to read the contents of any counter without effecting or disturbing the counting operation. When the programmer wishes to read the contents of a selected counter "On the fly", he loads the MODE register with a special code which latches the present

count value into a storage register so that its contents contain an accurate, stable quantity. The programmer then issues a normal read command to the selected counter. The contents of the latched register must be read in the sequence programmed in the MODE Control Word (RL0, RL1). This commands has no effect on the counters mode.

Program Example

```
Set up sequence for counter #0
    MVI  A, 0011000B ... #0, LSB-MSB, MODE 0, Binary
    OUT  CWAD        ... The address of Control Word Register
    MVI  A, 53H      ... LSB for counter #0
    OUT  CNTO        ... The address of counter #0
    MVI  A, 82H      ... MSB for counter #0
    OUT  CNTO        ... The address of counter #0
     ⋮
READ the contents of counter #0
    MVI  A, 0000XXXXB
    OUT  CWAD        ... Latching count
    IN   CNTO        ... Read LSB of counter #0
    MOV  L, A
    IN   CNTO        ... Read MSB of counter #0
    MOV  H, A
     ⋮
RELOAD to counter #0
    MVI  A, 82H      ...
    OUT  CNTO        ... Load LSB for counter #0
    MVI  A, 53H      ...
    OUT  CNTO        ... Load MSB for counter #0
```

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{CC}	V_{CC} Supply Voltage (with respect to GND (V_{SS}))	-0.5V to +7.0V
V_{IN}	Input Voltage (with respect to GND (V_{SS}))	-0.5V to +7.0V
V_{OUT}	Output Voltage (with respect to GND (V_{SS}))	-0.5V to +7.0V
P_D	Power Dissipation	1W
Tsol	Soldering Temperature (Soldering Time 10 sec)	260°C
Tstg	Storage Temperature	-55°C to +150°C
Topr	Operating Temperature	0°C to 70°C

DC CHARACTERISTICS (Topr=0°C to 70°C, V_{CC}=5.0V±5%, GND=0V)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		2.2		V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL}=2.2 mA			0.45	V
V_{OH}	Output High Voltage	I_{OH}=-400 μA	2.4			V
I_{IL}	Input Leak Current	$0 \leq V_{IN} \leq V_{CC}$			±10	μA
I_{OFL}	Output Leak Current	$0 \leq V_{OUT} \leq V_{CC}$			±10	μA
I_{CC}	V_{CC} Supply Current				140	mA

INPUT CAPACITANCE (Ta=25°C, V_{CC}=GND=0V)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	INPUT CAPACITANCE	f_C=1 MHz			10	pF
$C_{I/O}$	INPUT/OUTPUT CAPACITANCE	Unmeasured pins, 0V			20	pF

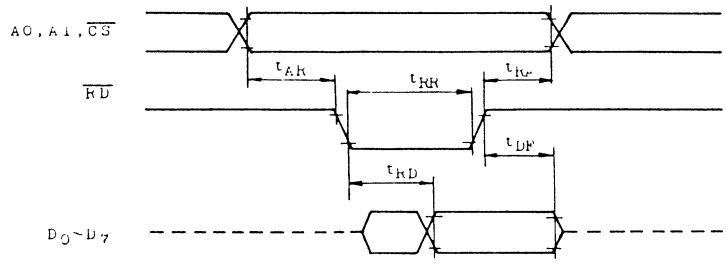
AC CHARACTERISTICS

(Topr=0°C to 70°C, V_{CC}=5.0V±5%, GND=0V)

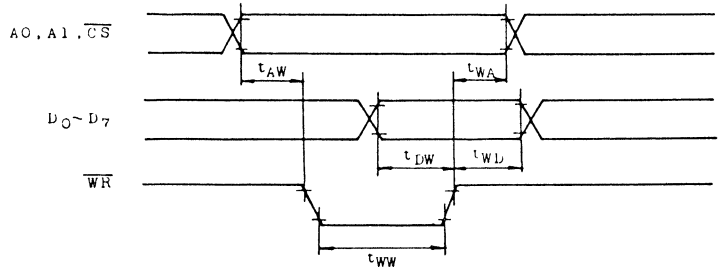
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{AR}	Address Set up Time ($\overline{RD}\downarrow$)		30			ns
t_{RA}	Address Hold Time ($\overline{RD}\uparrow$)		5			ns
t_{RR}	$\overline{RD}$ Pulse Width		300			ns
t_{RD}	Valid Data ($\overline{RD}\downarrow$)	C_L=150 pF			200	ns
t_{DF}	Data Floating ($\overline{RD}\uparrow$)		25		100	ns
t_{RV}	Recovery Time		1			μs
t_{AW}	Address Set up Time ($\overline{WR}\downarrow$)		30			ns
t_{WA}	Address Hold Time ($\overline{WR}\uparrow$)		30			ns
t_{WW}	$\overline{WR}$ Pulse Width		300			ns
t_{DW}	Data Set up Time ($\overline{WR}\uparrow$)		250			ns
t_{WD}	Data Hold Time ($\overline{WR}\uparrow$)		30			ns
t_{CLK}	Clock Period		380		DC	ns
t_{PWH}	CLK High Pulse Width		230			ns
t_{PWL}	CLK Low Pulse Width		150			ns
t_{GW}	GATE Width High		150			ns
t_{GL}	GATE Width Low		100			ns
t_{GS}	GATE Set up Time (CLK↑)		100			ns
t_{GH}	GATE Hold Time(CLK↑)		50			ns
t_{OD}	Output Delay From (CLK↓)	C_L=150 pF			400	ns
t_{ODG}	Output Delay From (GATE↓)	C_L=150 pF			300	ns

NOTE: AC timings measured at V_{OH}=2.2V, V_{OL}=0.8V

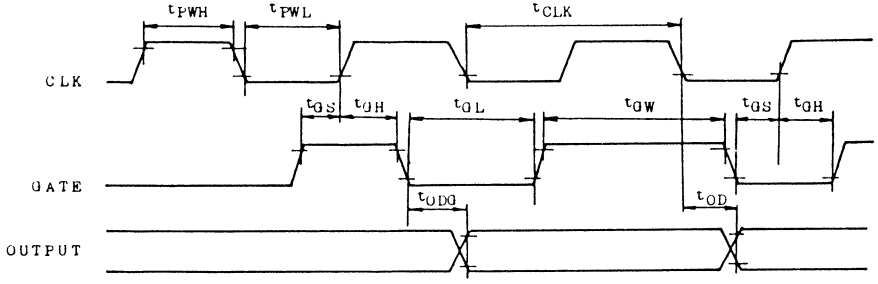
READ TIMING



WRITE TIMING



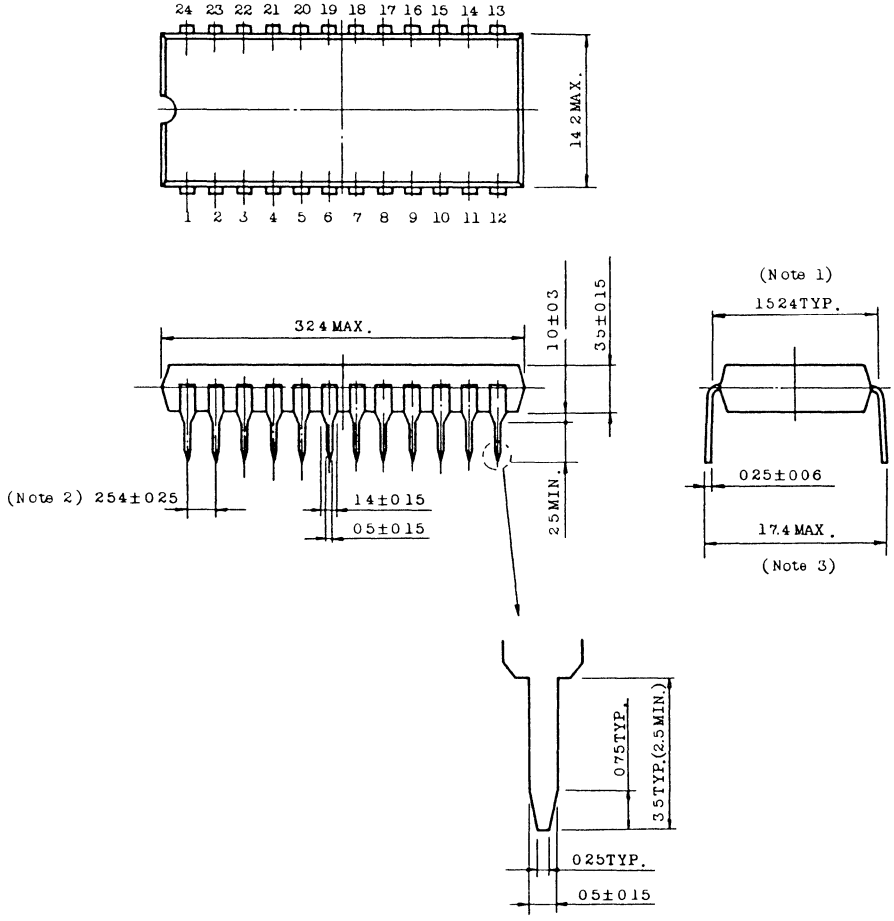
CLOCK & GATE TIMING



OUTLINE DRAWING

PLASTIC PACKAGE

Unit in mm



Note: 1. This dimension is measured at the center of bending point of leads.

2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoritical positions with respect to No.1 and No.24 leads.

3. This dimension is to outside of leads.

CMOS PROGRAMMABLE PERIPHERAL INTEFACE
TMP82C55AP-5/TMP82C55AF-5
TMP82C55AP-2/TMP82C55AF-2
TMP82C55AP-10/TMP82C55AF-10

1. General Description and Features

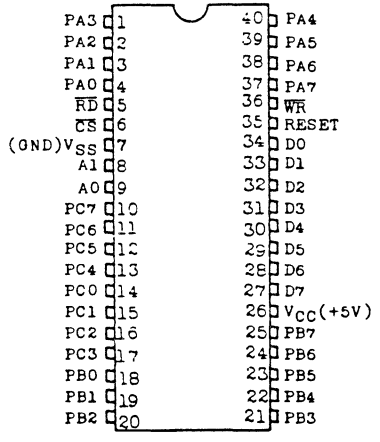
The TMP82C55AP/AF (hereinafter referred to as PPI) is a CMOS high Speed programmable input/output interface with three 8-bit I/O ports. 24 I/O terminals are divided into two groups (Port A and Port B) which are programmable independently by control words provided by CPU. The PPI has three operation modes (Mode 0, 1 and 2) and is capable of versatile interface between CPU and peripheral devices.

The TMP82C55AP/AF is fabricated using Toshiba's CMOS Silicon Gate Technology.

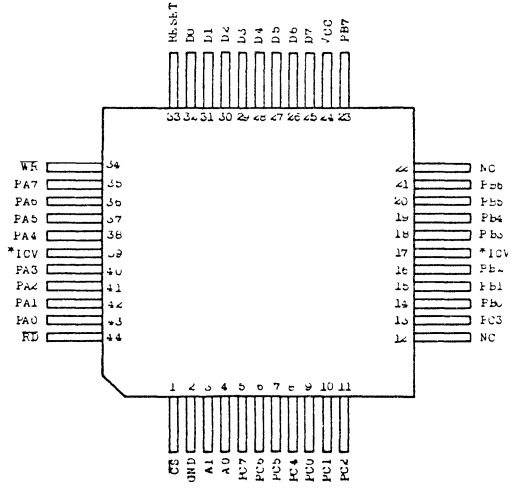
(1) High Speed Version (TRD=100ns MAX: TMP82C55AP-10/AF-10)
(2) Low power consumption
  2mA Typ.
  10μA Max. (@5V, Stand-by)
(3) 5V ± 10% Single power supply
(4) 24 programmable I/O terminals
(5) Three operation modes (Mode 1, Mode 2, Mode 3)
(6) Bit set/reset capability
(7) Any 8 bits outputs of port B and C are capable of driving darlington transistors (Min. -1.0mA @ VOH=1.5V)
(8) Extended operating temperature: -40°C to + 85°C
(9) Available 40pin Standard DIP and 44pin Mini Flat Package

Pin Connections (Top View)

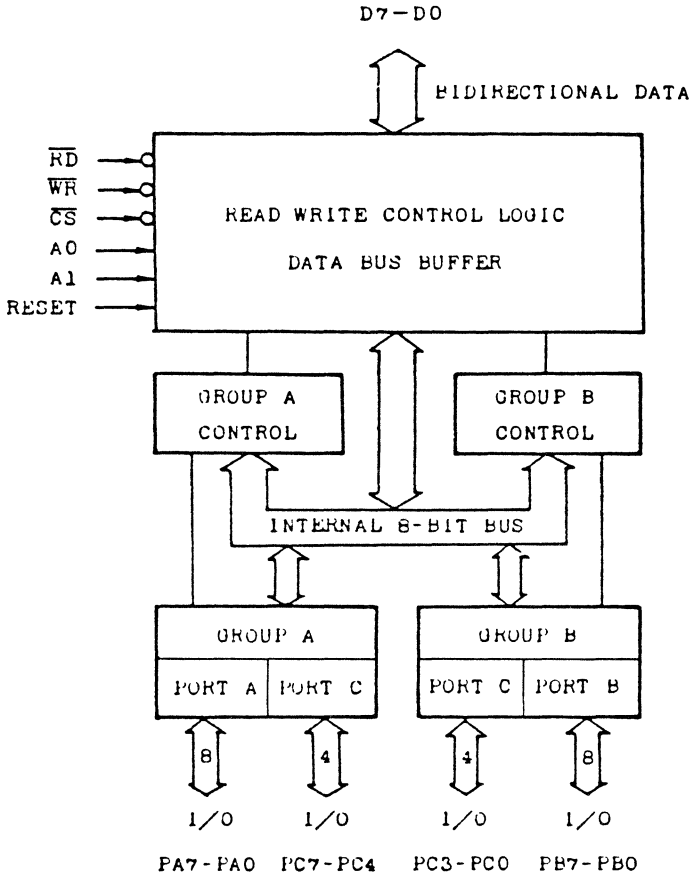
TMP82C55AP-5/AP-2/AP-10



TMP82C55AF-5/AF-2/AF-10



*ICV (Pin 17 and Pin 39) must be connected to VCC (Pin24) or must be open.
NC: No Connection


D7-D0
BIDIRECTIONAL DATA
RD
WR
CS
A0
A1
RESET
READ WRITE CONTROL LOGIC
DATA BUS BUFFER
GROUP A CONTROL
GROUP B CONTROL
INTERNAL 8-BIT BUS
GROUP A
PORT A
PORT C
GROUP B
PORT C
PORT B
8
4
4
8
I/O
I/O
I/O
I/O
PA7-PA0
PC7-PC4
PC3-PC0
PB7-PB0

2. Pin names and pin functions

Pin Name	Number of Pin	Input/Output 3-state	Function
D7 - D0	8	I/O 3-state	3-state bidirectional 8-bit data bus. Used for data transfer with CPU. Also, used for transfer of control words to PPI and status information from PPI.
PA7-PA0	8	I/O 3-state	3-state 8-bit I/O Port A. Operation mode and input/output configuration are defined by software. Port A contains the output latch buffer and input latch.
PB7-PB0	8	I/O 3-state	3-state 8-bit I/O Port B. Opepration mode and input/output configuration are defined by software. Port B contains the output latch buffer and input latch.
PC7-PC0	8	I/O 3-state	3-state 8-bit I/O Port C. Operation mode and input/output configuration are defined by software. Port C can be divided into two 4-bit ports by the mode control and also, used as the control signal for Port A and Port B. In this case, 3 bits of PC0 to PC2 are used for Port B and 5 bits of PC3 to PC7 for Port A.
$\overline{CS}$	1	Input	Chip select input. When this terminal is at "L" level, data transfer PPI and CPU becomes possible. At "H" level, the data bus is placed in the high impedance state and control from the processor is ignored.
$\overline{RD}$	1	Input	Read signal. When this terminal is at "L" level, data that is input into the port is transferred to CPU.
$\overline{WR}$	1	Input	Write signal. When this terminal is at "L" level, data or control word is written into PPI from CPU.
A0, A1	2	Input	Used for selecting Port A, B, C and the control registers. Normally, this terminal is connected to low order 2 bits of the address bus.
RESET	1	Input	When this terminals is at "H" level, all internal registers including the control register are cleared. In addition, all ports (Port A, B, C) are placed in the input mode (high impedance) of mode 0.
VCC	1	Power Supply	5V
VSS	1	Power Supply	GND

3. Functional Description

The PPI is a programmable peripheral interface with three 8-bit ports (Port A, B and C) and two control registers. 24 I/O terminals are divided into 12-bit group A and group B. Group A consists of Port A and high order 4 bits of Port C, while Group B consists of Port B and low order 4 bits of Port C. Each group is independently programmable by control words provided from CPU. There are three operation modes available for the PPI. In mode 0, two 8-bit I/O ports and two 4-bit I/O ports can be programmed as input or output ports, respectively. In mode 1, 24 I/O terminals are divided into Group A and Group B. 8 bits of each group are used as input or outpt port and of the remaining 4 bits, 3 bits are used as handshaking and interrupt control signal. Mode 2 is applicable only to group A and the terminals are used as a bidirectional 8-bit data bus and 5-bit control signal. In case of Port C being used as the output, any bits of Port C can be set/reset.

There are two control registers; one is used for mode setting and the other for bit set/reset control. The control registers can only be written into. Further, when the reset input (RESET) becomes "1", the control registers are reset and all I/O terminals are placed in input mode (high impedance status).

					Function
A1	A0	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	
0	0	0	0	1	Data bus <—— Port A
0	1	0	0	1	Data bus <—— Port B
1	0	0	0	1	Data bus <—— Port C
0	0	0	1	0	Port A ——> Data bus
0	1	0	1	0	Port B ——> Data bus
1	0	0	1	0	Port C ——> Data bus
1	1	0	1	0	Control register <---- Data bus
x	x	1	x	x	Data bus ——> 3-state
x	x	0	1	1	Data bus ——> 3-state
1	1	0	0	1	inhibition of combination

Table 3.1 Basic Operation of TMP82C55A

3.1. Mode Selection

There are three basic modes of operation that can be selected by control words.

Mode 0 - Basic I/O (Group A, Group B)
Mode 1 - Strobe input/Strobe output (Group A, Group B)
Mode 2 - Two-way bus (Port A only)

Operation modes for Group A and Group B can be independently defined by the control word from the CPU. If DB7 is set to "1" in writing a control word into the PPI, on operation mode is selected, while of DB7="0", the set/reset function for Port C is selected.

3.1.1 Control word to define operation mode

Fig. 5.1 shows the control words to define operation mode of the TMP82C55A.

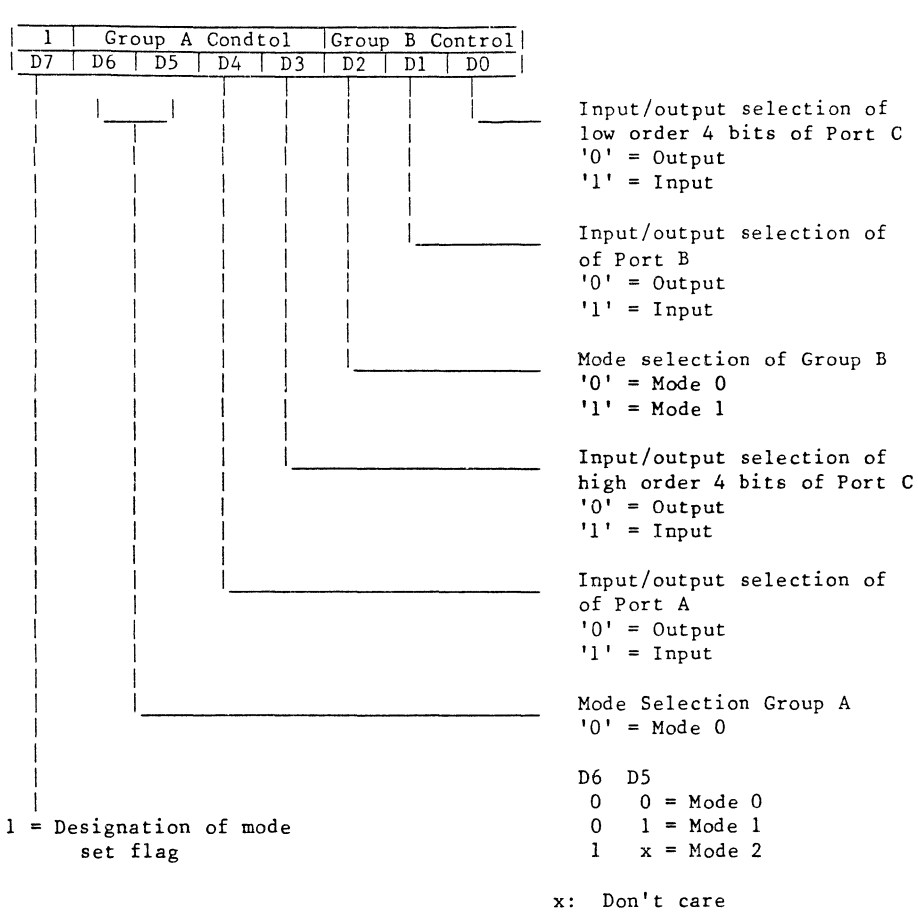


Fig. 3.1 Control Word for Mode Selection

3.1.2 Port C bit set/reset control word

Any bit of 8 bits of Port C can be set/reset by Port C bit set/reset control word. Fig. 3.2 shows the Port C bit set/reset control word.

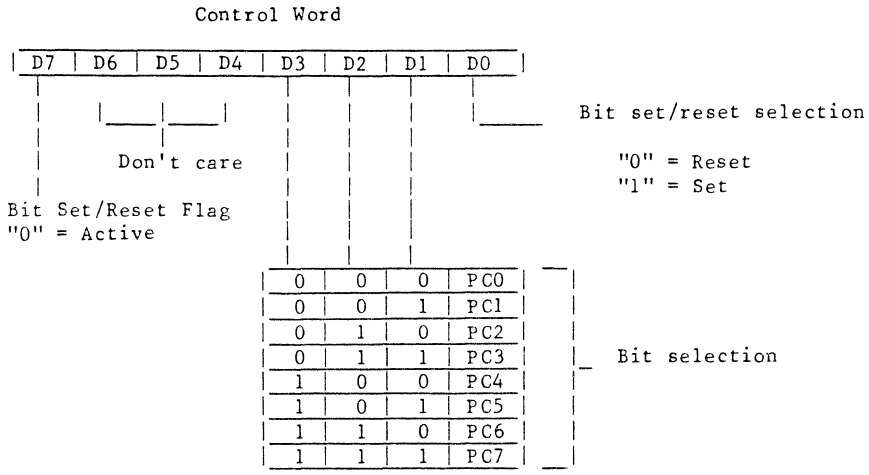


Fig. 3.2 Control Word for Bit Set/Reset

3.2 Operation Modes

3.2.1 Mode 0 (Basic I/O)

This functional configuration is used for simple input or output operations. No 'handshaking' is required and data is simply written to or read from a specified part. Output data to the ports from CPU are latched out but input data from the ports are not latched.

In Mode 0, 24 I/O terminals are divided into four groups of Port A (8 bits), Port B (8 bits), high order 4 bits of Port C and low order 4 bits of Port C. Each port can be programmed to be input or output. The configuration of each port are determined according to the contents of Bit 4 (D4), 3(D3), 1(D1) and 0(D0) of the control word for mode selection.
The I/O configuration of each port in Mode 0 are shown in Table 3.2.

Node Setting Control Word				Port A	Port C	Port B	Port C
D4	D3	D1	D0		(PC7-PC4)		(PC3-PC0)
0	0	0	0	Out	Out	Out	Out
0	0	0	1	Out	Out	Out	In
0	0	1	0	Out	Out	In	Out
0	0	1	1	Out	Out	In	In
0	1	0	0	Out	In	Out	Out
0	1	0	1	Out	In	Out	In
0	1	1	0	Out	In	In	Out
0	1	1	1	Out	In	In	In
1	0	0	0	In	Out	Out	Out
1	0	0	0	In	Out	Out	In
1	0	1	0	In	Out	In	Out
1	0	1	1	In	Out	In	In
1	1	0	0	In	In	Out	Out
1	1	0	1	In	In	Out	In
1	1	1	0	In	In	In	Out
1	1	1	1	In	In	In	In

Table 3.2 Port definition in Mode 0

3.2.2 Mode 1 (Strobe I/O)

In Mode 1, input/output of port data is performed in conjunction with the strobe signals or 'handshaking' signals. Port C is used to control Port A or Port B.

The basic operatings in Mode 1 are as follows:

- o Mode 1 can be set for two groups of Group A and Group B.
- o Each group consist of 8-bit data port and 4-bit control/data port.
- o The 8-bit data port can be set as input or output port.
- o The control/data port is used as control or status of the 8-bit data port.

(1) When used as the input port in Mode 1:

- o STB (Strobe Input)
  At "0", input data is loaded in the internal input latch in the port. In this case, a control signal from CPU is not concerned and data is input from the port any time. This data is not read out on the data bus unless CPU executes an input instruction.

- o IBF (Input Buffer Full F/F Output)
  When data is loaded in the internal input latch from the port, this output is set to "1". IBF is set ("1") by STB input being reset and is reset ("0") by the rising edge of RD input.

- o INTR (Interrupt Request Output)
  Used for the interrupt process of data loaded in the internal input latch. When STB input is at "0" if INTE (INTE flag) in the PPI is in the enabled state ("1"), IBF is set to "1". INTR is set to "1" immediately after the rising edge of this STB input and reset to "0" by the falling edge of RD input.
  The INTE flags of Group A and Group B are controlled as follows:

INTEA - Control by bit set/reset of PC4
INTEB - Control by bit set/reset of PC2

(2) When used as the output port in Mode 1:

o $\overline{OBF}$ (Output Buffer Full F/F Output)
This is a flag which shows that CPU has written data into a specified port. OBF is set to becomes "0" at the rising edge of WR signal and is set to "1" at the falling edge of ACK (Acknowledge input) signal.

o $\overline{ACK}$ (Acknowledge Input)
ACK signal is sent to the PPI as a response from a peripheral device that received data from the port.

o INTR (Interrupt Request Output)
When a peripheral device received data from CPU, INTR is set to "1" and the interrupt is requested to CPU. If ACK signal is received when INTE flag is in the enable state, OBF is set to "1" and INTR signal becomes "1" immediately after the rising edge of ACK signal. Further, INTR is reset at the falling edge of WR signal when data is written into the PPI by CPU.
The INTE flags of Group A and Group B are controlled as follows:

INTEA - Control by bit set/reset of PC6
INTEB - Control by bit set/reset of PC2

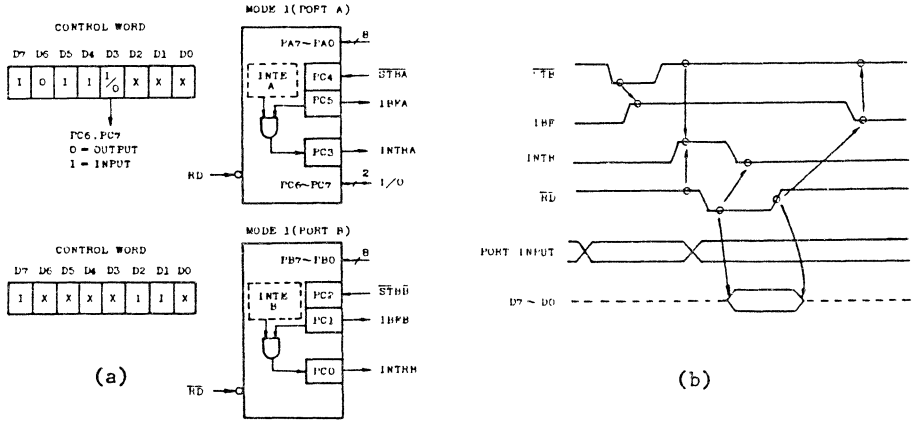


Fig. 3.3 Example of Strobe Input in Mode 1

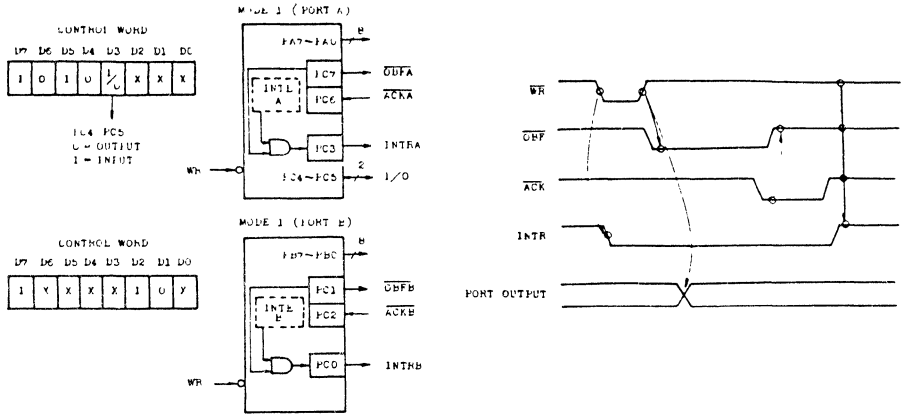


Fig. 3.4 Example of Strobe Output in Mode 1

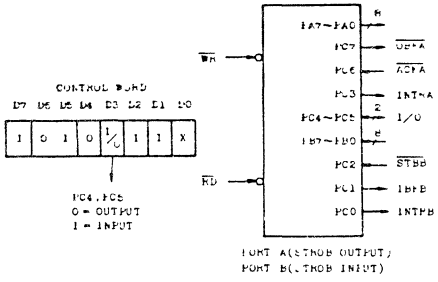


Fig. 3.5 Example of Port A Output, Port B Input in Mode 1

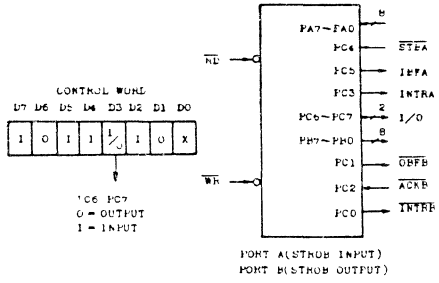


Fig. 3.6 Examaple of Port A Input, Port B Output in Mode 1

3.2.3 Mode 2 (Strobed Bidirectional Bus I/O)

In this mode, Port A is used as 8 bits bidirectional bus for data transfer with a peripheral device. This mode is applicable only to Group A, which consists of an 8-bit bidirectional bus (Port A 8-bit) and 5-bit control signals (high order 5 bits of Port C). The bidirectional bus (Port A) has both the internal input and output registers. When group A is set in Mode 2, Group B can be set independently. There are 5 control signals as follows when Group A is used in Mode 2.

o OBF (Output buffer Full F/F Output)
When CPU writes data into of Port A, OBF is set to "0" to inform a peripheral device that the PPI is ready to output data. However, Port A is kept in the floating (high impedance) state until ACK input signal is received.

o ACK (Acknowledge Input)
When ACK signal is set to "0", the data of the 3-state output buffer of Port A is send out. If ACK signal is at "1", Port A is in the high impedance state.

o STB (Strobe Input)
When STB input is set to "0", the data from peripheral devices are held in the input latch. When the active RD signal is input into the PPI, the latched input data are output on the system data bus (D7 - D0).

o IBF (Input Buffer Full F/F Output)
When data from peripheral devices are held in the input latch, IBF is set to "1".

o INTR (Interrupt Request Output)
INTR is the output to request the interrupt to CPU and its function is the same as that in Mode 1. There are two interrupt enable flip-flop (INTE), INTE1 corresponds to INTEA in Mode 1 output and INTE2 to INTEA in Mode 1 input.

INTE 1 - Used to generate INTR signal in conjunction with OBF and ACK signals, and is controlled by PC6 bit set/reset.
INTE 2 - Used to generate INTR signal in conjunction with IBF and STB signals, and is controlled by PC4 bit set/reset.

Fig. 3.7 shows the operating example and the timing diagram in Mode 2.

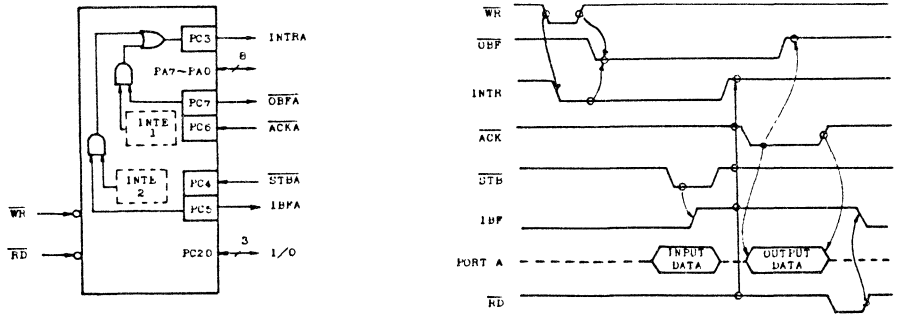


Fig. 3.7 Operating example in Mode 1

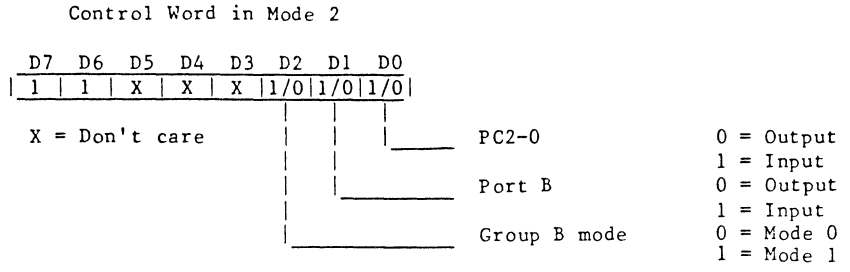


Fig. 3.8 Control Word and Configuration in Mode 2

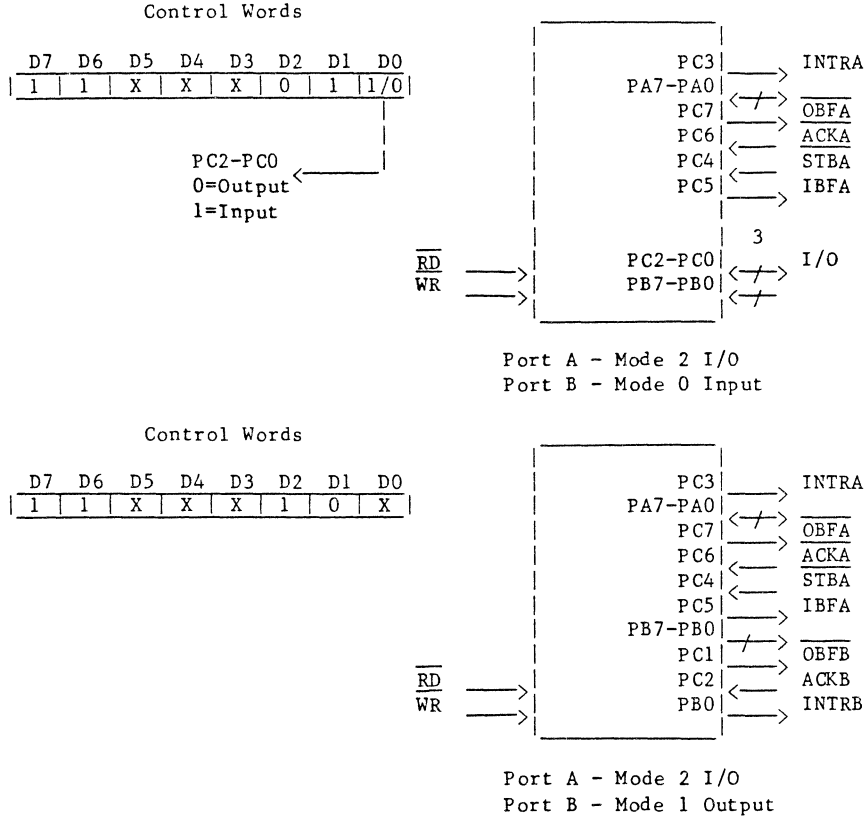


Fig. 3.9 Examples in Combination with Mode 2 and Other Mode

3.2.4 Precautions for use in Mode 1 and 2

When used in Mode 1 and 2, bits which are not used as control or status in Port C can be used as follow.

If programmed as the input, they are accessed by normal Port C read.

If programmed as the output, high order bits of Port C (PC - PC4) are accessed using the bit set/reset function. As to low order bits of Port C (PC3 - PC0), in additions ot access by the bit set/reset function, 3 bits only can be accessed by normal writing.

3.3. Reading Port C Status

When Port C is used as the control port, that is, when Port C is used in Mode 1 or Mode 2, the status information of the control word can be read out by a normal read operation of Port C.

Data Mode	D7	D6	D5	D4	D3	D2	D1	D0
Mode 1 Input	I/O	I/O	IBFA	INTEA	INTRA	INTEB	IBFB	INTRB
Mode 1 Output	$\overline{\text{OBFA}}$	INTEA	I/O	I/O	INTRA	INTEB	$\overline{\text{OBFB}}$	INTRB
Mode 2	$\overline{\text{OBFA}}$	INTE1	IBFA	INTE2	INTRA	By Group B Mode		

Table 3.3 Status Word Format of Port C

6. Absolute Maximum Ratings

Symbol	Item	Rating	Unit
VCC	Supply Voltage	-0.5 to 7.0	V
VIN	Input Voltage	-0.5 to Vcc + 0.5	V
PD	Power Dissipation	250	mW
TSOLDER	Soldering Temperature (10 sec)	260	°C
TSTG	Storage Temperature	-65 to 150	°C
TOPR	Operating Temperature	-40 to 85	°C

7. DC Electrical Characteristics

TA = -40°C to 85°C, VCC = 5V ± 10%, VSS = 0V

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage		-0.3	-	0.8	V
VIH	Input High Voltage		2.2	-	VCC +0.5	V
VOL	Output Low Voltage	IOL = 2.5mA	-	-	0.45	V
VOH1	Output High Voltage	IOH = -400μA	2.4	-	-	V
VOH2	Output High Voltage	IOH = -100μA	VCC-0.8	-	-	V
IL1	Input Leak Current	$0 \leqq VIN \leqq VCC$	-	-	±10	μA
ILO	Output Leak Current (High Impedance State)	$0 \leqq VOUT \leqq VCC$	-	-	±10	μA
(Note1) IDAR	Darlington Drive Current	VEXT = 1.5V REXT = 1.1kΩ	-1.0	-	-5.0	mA
ICC1	Operating Supply Current	I/O cycle Time 1 usec	-	2.0	5.0	mA
(Note2) ICC2	Stand-by Supply Current	VIH > VCC-0.2V VIL < 0.2V $\overline{CS}$ > VCC-0.2V	-	-	10	μA

(Note1) Applied for optional 8 I/O terminals in Port B and Port C.
(Note2) Icc2 is not specified for TMP82C55AP-2/AF-2/AP-10/AF-10.

8. Capacitance

TA = 25°C, VCC=VSS=0V

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CIN	Input Capacitance	f = 1MHz	-	-	10	pF
COUT	Output Capacitance	(*)	-	-	20	pF

(*): All terminals except that to be measured should be earthed.

4.4 AC Electrical Charactreistics

TA =-40°C to 85°C, VCC = 5V±10%, VSS=0V

SYMBOL	PARAMETER	AP-5/AF-5		AP-2/AF-2		AP,AF-10		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tAR	Address set-up time for $\overline{RD}$ fall	0	-	0	-	0	-	ns
tRA	Address hold time for $\overline{RD}$ rise	0	-	0	-	0	-	ns
tRR	$\overline{RD}$ pulse width	300	-	160	-	150	-	ns
tRD	Delay from $\overline{RD}$ fall to decided data output	-	200	-	140	-	100	ns
tDF	Time from $\overline{RD}$ rise to data bus floating	10	100	0	40	0	40	ns
tRV	Time from $\overline{RD}$ or $\overline{WR}$ rise to next $\overline{RD}$ or $\overline{WR}$ fall	850	-	200	-	150	-	ns
tAW	Address set-up time for $\overline{WR}$ fall	0	-	0	-	0	-	ns
tWA	Address holding time for $\overline{WR}$ rise	20	-	20	-	20	-	ns
tWW	$\overline{WR}$ pulse width	300	-	120	-	120	-	ns
tDW	Bus data set-up time for $\overline{WR}$ rise	100	-	100	-	100	-	ns
tWD	Bus data holding time for $\overline{WR}$ rise	30	-	30	-	30	-	ns
tWB	Delay from $\overline{WR}$ rise to decided data output	-	350	-	350	-	350	ns
tIR	Port data set-up time for $\overline{RD}$ fall	0	-	0	-	0	-	ns
tHR	Port data holding time for $\overline{RD}$ rise	0	-	0	-	0	-	ns
tAK	$\overline{ACK}$ pulse width	300	-	300	-	300	-	ns
tST	$\overline{STB}$ pulse width	500	-	350	-	350	-	ns
tPS	Port data set-up time for $\overline{STB}$ rise	0	-	0	-	0	-	ns
tPH	Port data holding time for $\overline{STB}$ rise	180	-	150	-	150	-	ns

T_A=-40°C to 85°C, V_{CC}=5V±10%, V_{SS}=0V

SYMBOL	PARAMETER	AP-5/AF-5		AP-2/AF-2		AP,AF-10		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tAD	Delay from $\overline{ACK}$ fall to decided data output	-	300	-	300	-	300	ns
tKD	Time from $\overline{ACK}$ rise up to port (Port A in Mode 2) floating	20	250	20	250	20	250	ns
tWOB	Delay from $\overline{WR}$ rise to $\overline{OBF}$ fall	-	650	-	300	-	300	ns
tSIB	Delay from $\overline{ACK}$ fall to $\overline{OBF}$ rise	-	350	-	350	-	350	ns
tRIB	Delay from $\overline{STB}$ fall to $\overline{IBF}$ rise	-	300	-	300	-	300	ns
tRIT	Delay from $\overline{RD}$ fall to INTR fall	-	400	-	400	-	400	ns
tSIT	Delay from $\overline{ACK}$ rise to INTR rise	-	300	-	300	-	300	ns
tAIT	Delay from $\overline{ACK}$ rise to INTR rise	-	350	-	350	-	350	ns
tWIT	Delay from $\overline{WR}$ rise to INTR fall	-	450	-	450	-	450	ns

Note 1. When the power supply is turned ON, reset pulse duration must be active for at least 500 ns or more.

2. AC Measuring Point Input Voltage VIH=2.4V, VIL=0.45V
Output Voltage VOH=2.2V, VOL=0.8V
CL=150pF.

4.5 Timing diagram

Mode 0

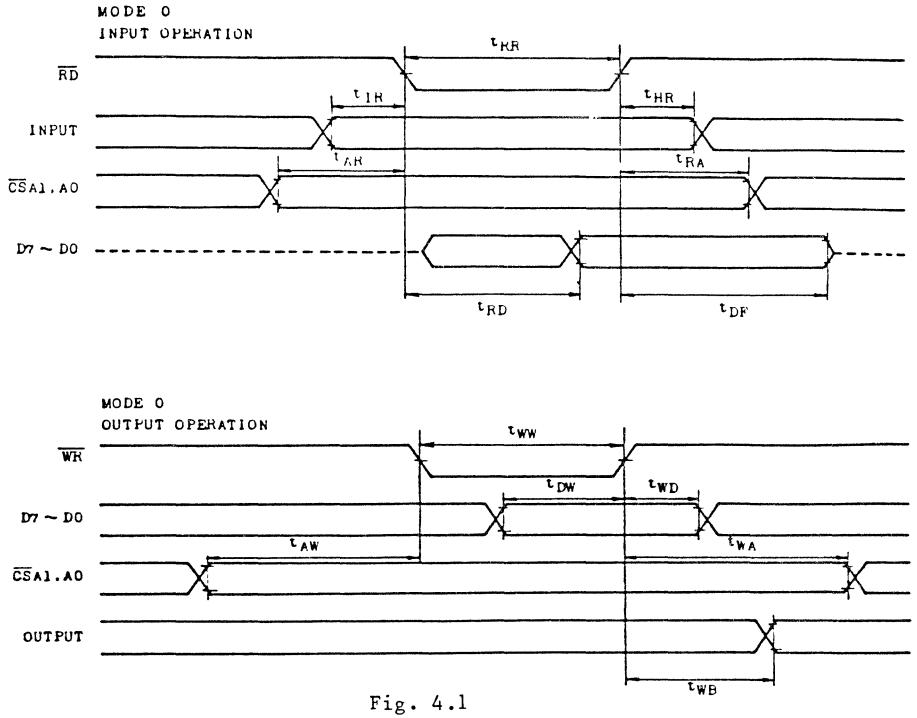
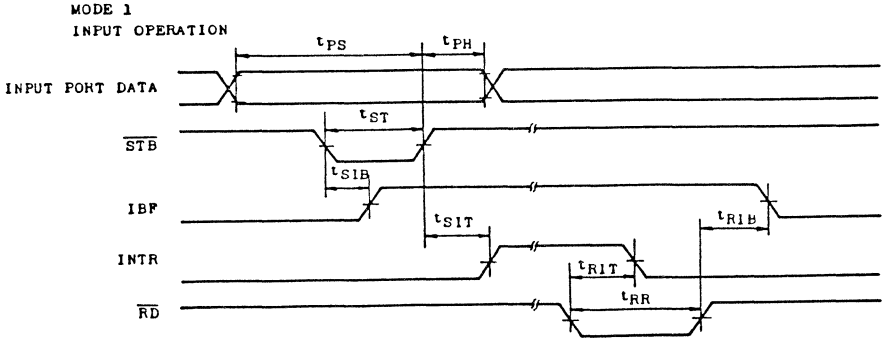


Fig. 4.1

Mode 1



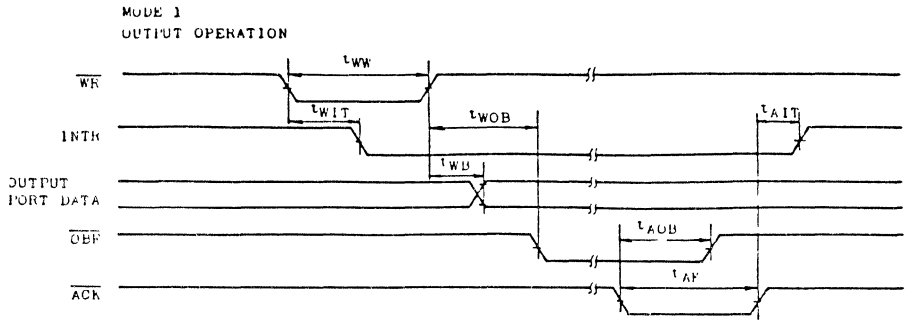


Fig. 4.2

Mode 2

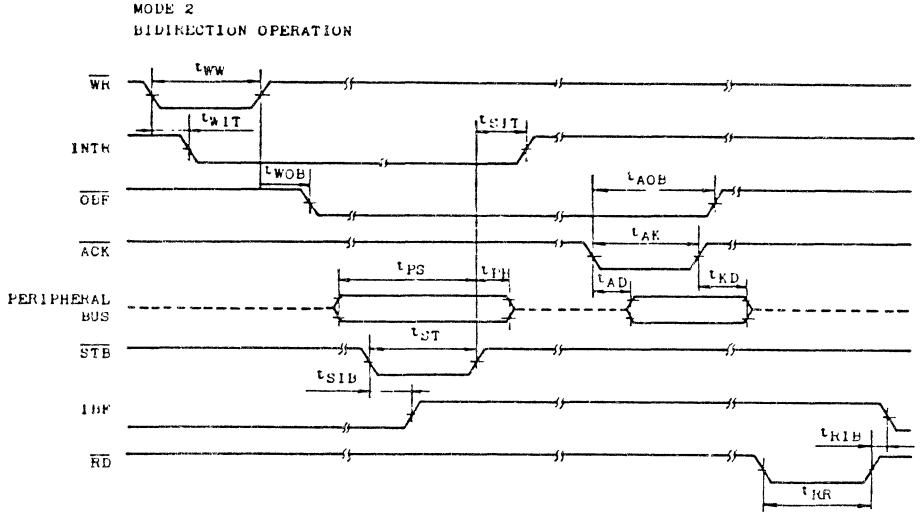
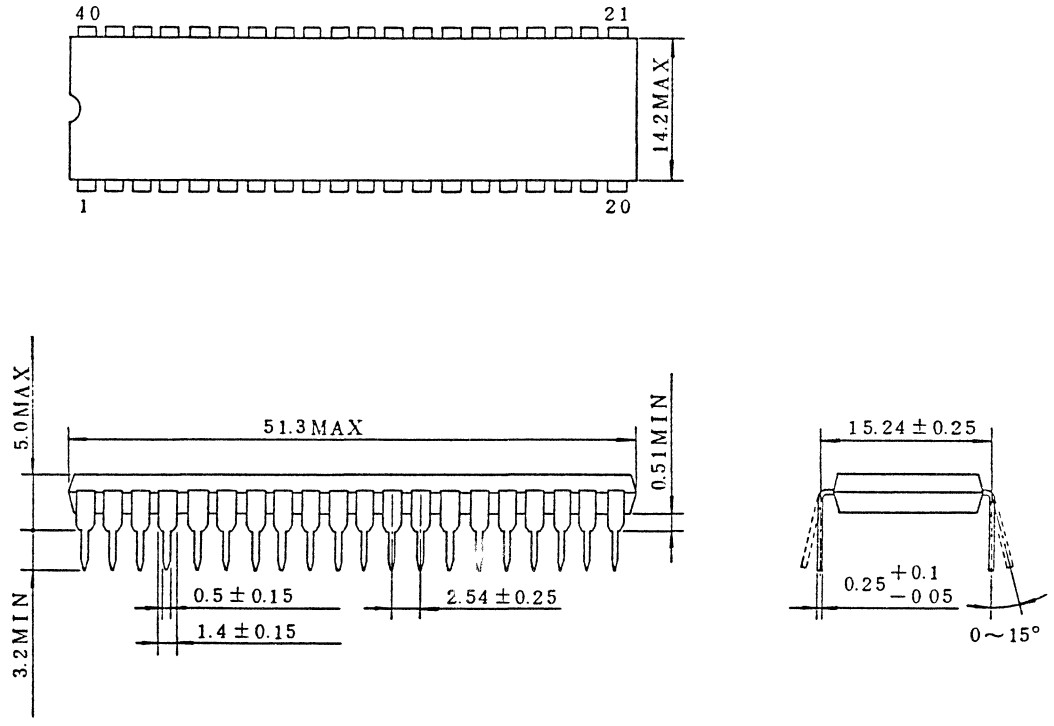


Fig. 4.3

5. Package Dimension
Plastic Packge

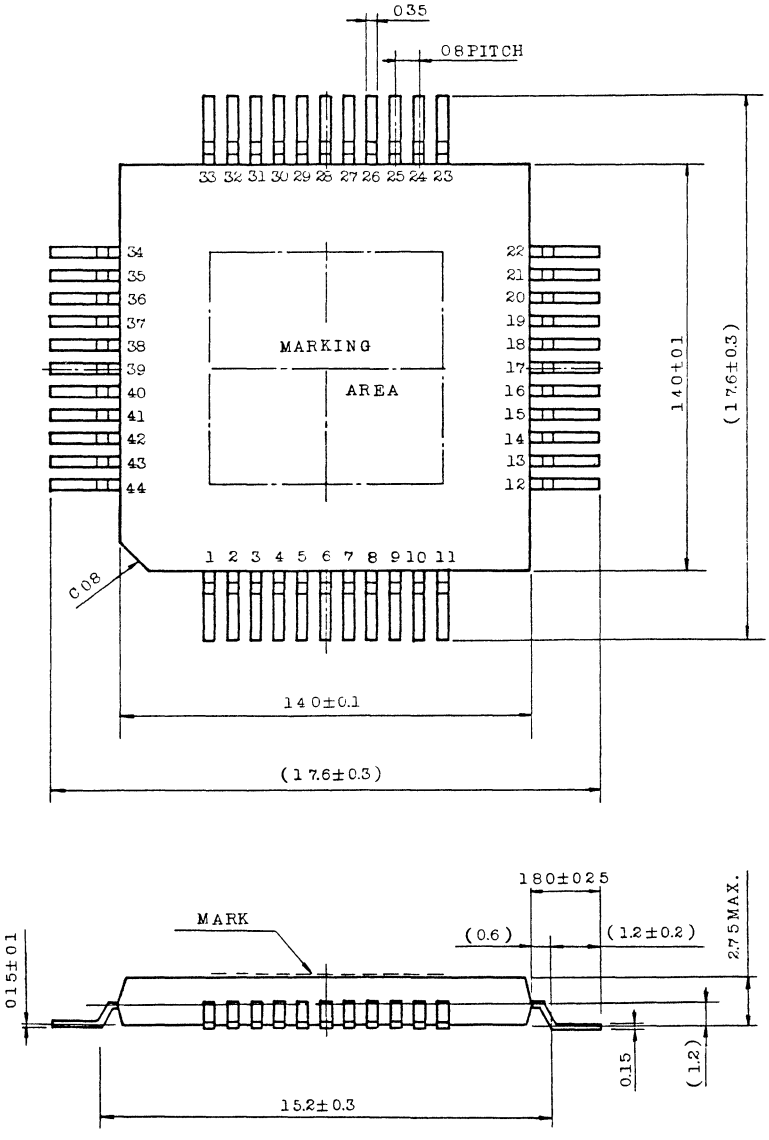
Unit : mm



Note Each lead pitch is 2.54mm, and all the leads are located within ±0.25 mm from their theoretical positions with respect to No.1 and No.4 leads.

EXTERNAL DIMENSION VIEW (Mini Flat Package)

Unit in mm



PROGRAMMABLE PERIPHERAL INTERFACE (PPI)

GENERAL DESCRIPTION

TMP8255AP-5 is the high speed programmable peripheral interface LSI, capable of controlling parallel input/output data. This LSI is programmable in several operation modes and is capable of supplying a simple interface between micro-processors and peripherals equipment.

24 input/output pins are divided into three 8-bit ports and used either for input or output by programs.

All signal levels are TTL compatible.

Data transfer between the processor and TMP8255AP-5 is possible by using Chip Select Input ($\overline{CS}$) and Port Address A_0, A_1.

Data write/read operation to/from a specified port is possible by using Write Input ($\overline{WR}$) or Read Input ($\overline{RD}$).

FEATURES

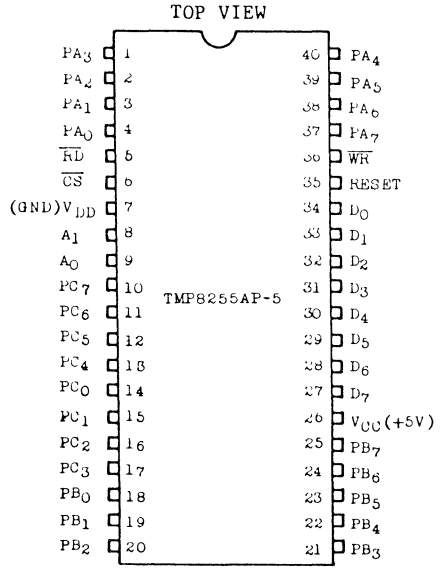
- Compatible with INTEL's 8255A-5
- 24 Programmable Input/Output Pins
- Programmable Operation Modes
- Direct Bit Set/Reset Capability
- Single +5V Power Supply

PIN NAMES

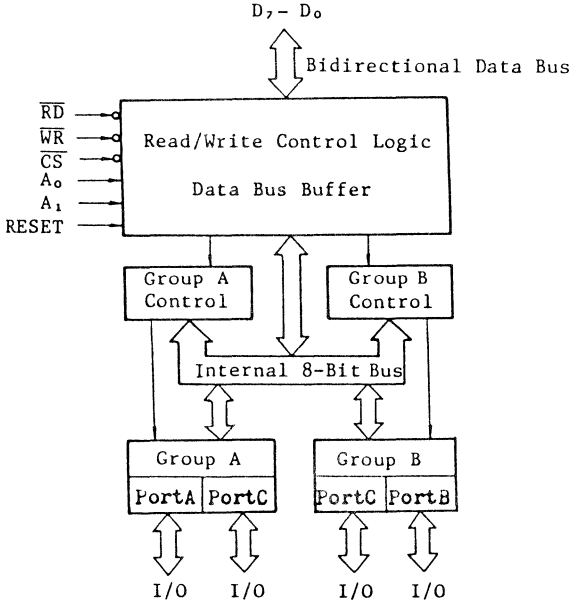
$PA_0 \sim PA_7$	Port A
$PB_0 \sim PB_7$	Port B
$PC_0 \sim PC_7$	Port C
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Signal
$\overline{WR}$	Write Signal
A_0 - A_1	Port Address
RESET	Reset
V_{CC} . V_{SS}	Power Supply

PIN CONNECTION

TOP VIEW



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

I/O SIGNALS

TMP8255A-5 uses a 8-bit bidirectional data bus for data transfer to/from the processor. Data can be transfered between the data bus and control registers or between 2 output port groups (Group A and Group B), in the inside of TMP8255AP-5. There are 2 control registers.
Group A consists of high-order 4 bits of Port C and Port A. Group B consists of low-order 4 bits of Port C and Port B.

Port A 8 data bits are used for input latch/buffer, output latch/buffer, or bidirectional bus, respectively.

Port B 8 data bits are used for input buffer or output latch/buffer.

Port C 8 data bits are used for input buffer, output latch/buffer, or two 4-bit control ports in combination with Port A and B.

Operation of each port is controlled by programs.

When two inputs of Port Addresses A_0 and A_1 are used together with Read Input, Write Input and Chip Select, it is possible to select a specific port or control register.

Port A selection	$A_1 = 0$	$A_0 = 0$
Port B selection	$A_1 = 0$	$A_0 = 1$
Port C selection	$A_1 = 1$	$A_0 = 0$
Control register selection	$A_1 = 1$	$A_0 = 1$

(Note: Readout operation from a control register is impossible.)

Read ($\overline{RD}$)	Data read operation from TMP8255AP-5 to the data bus is controlled by $\overline{RD}$ signal (low active).
Write ($\overline{WR}$)	Data write operation from the data bus to TMP8255AP-5 is controlled by $\overline{WR}$ signal (low active).
Chip Select ($\overline{CS}$)	TMP8255AP-5 is selected by $\overline{CS}$ signal (low active). When $\overline{CS}$="1", the data bus driver is in the high impedance state.
Reset (RESET)	When RESET="1", all internal registers are cleared and all ports are in high impedance input mode.
Data Bus ($D_7 - D_0$)	The 8-bit data bus is used for transferring data and program information between the processor and TMP8255AP-5.

PROGRAMMING

To program the operations of TMP8255AP-5, first select the internal control function to be programmed by the processor. To do this, execute the write operation under the programming mode ($A_1 = A_0 = \overline{RD}$ = "1", $\overline{CS} = \overline{WR}$ = "0"). As a result, data bus information is written into one of two control registers. Input/Output of respective ports and operation mode of each group (Mode 0, 1 and 2 are available) can be selected by one of these control registers. Another control register is used for controlling set/reset of Port C bits. One of these two control registers is selected by Bit 7 of the data bus. When Bit 7 is "1", an operation mode is selected, while the set/reset function is selected when it is "0".

Bit 0 through 6 have different meanings depending upon a selected control mode.

(a) Operation Mode Control (DB7 = "1")

1	Control of Group A				Control of Group B		
DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0

- Control of Group A (DB_6 - DB_3)

  The operation mode is defined by Bit 6 and 5, and the port function (input or output) is selected by Bit 4 and 3.

- Control of Group B (Bit 2, 1 and 0)

  The operation mode is defined by Bit 2, and the port function (input or output) is selected by Bit 1 and 0.

The detail of operation modes and port input/output selection are described in the next item.

Relationship between operation modes and control bit are shown in the following table.

Operation Mode	Control Bit		
	Group A		Group B
	6	5	2
0	0	0	0
1	0	1	1
2	1	X	

Bit 6 and 5 define Group A modes and Bit 2 defines Group B modes.

Note: X mark shows that either 0 or 1 is acceptable.

(b) Bit Set/Reset Control (DB_7 = "0")

0	X	X	X	Bit Select			I/O
DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0

Bit Select

Bit 3, 2 and 1 select Port C bit to be set/reset.

Port C Bit Selection	Control Bit		
	3	2	1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Set/Reset

When Bit 0 is "1", selected bit of Port C is set and when it is "0", selected bit of Port C is reset. In this case, Bit 6, 5 and 4 are not used. Therefore, either "0" or "1" is acceptable.

OPERATION MODES

TMP8255AP-5 is designed for various programs which control for interfacing with various peripherals.
For this purpose, there are 3 basic modes.

Mode 0

24 input/output pins of 3 ports are devided into 4 groups of Port A (8 bits), Port B (8 bits), Port C (high order 4 bits) and Port C (low order 4 bits).

Data is latched in the output port, but is not latched in the input port. In the data input operation, input data is placed on the data bus at $\overline{RD}$ = 0. The combination of input/output of these 4 groups is available in 16 ways. This combination is selected by the operation mode register of TMP8255AP-5 using Bit 0, 1, 3 and 4 of the data bus.

Programming under Mode 0

In the case $\overline{CS}$ = $\overline{WR}$ = "0", A_1 = A_0 = $\overline{RD}$ = "1", DB_7 = "1" and DB_6 = DB_5 = DB_2 = "0", the programming is shown in the following table.

Data Bus Bit				Port A	Port C (PC_7-PC_4)	Port B	Port C (PC_3-PC_0)
4	3	1	0				
0	0	0	0	Out	Out	Out	Out
0	0	0	1	Out	Out	Out	In
0	0	1	0	Out	Out	In	Out
0	0	1	1	Out	Out	In	In
0	1	0	0	Out	In	Out	Out
0	1	0	1	Out	In	Out	In
0	1	1	0	Out	In	In	Out
0	1	1	1	Out	In	In	In
1	0	0	0	In	Out	Out	Out
1	0	0	1	In	Out	Out	In
1	0	1	0	In	Out	In	Out
1	0	1	1	In	Out	In	In
1	1	0	0	In	In	Out	Out
1	1	0	1	In	In	Out	In
1	1	1	0	In	In	In	Out
1	1	1	1	In	In	In	In

Mode 1

Under Mode 1, Port A and high order 5 bits of Port C are correlated to Group A, and Port B and low order 3 bits of Port B are correlated to Group B, respectively.

Port C is used for a control signal to control input/output data of Port A or Port B.

The internal enable/disable flip-flop (INTE) can be controlled by setting/resetting Bit 4 and 2 of Port C when Ports A and B are used as the input ports using the bit set/reset function, and by setting/resetting Bit 6 and 2 when they are used as the output ports.

When bit set/reset is "1", the flip-flop is placed in the enable state, and when bit set/reset is "0", it is placed in the disable state.

Data transfer between the ports and peripherals is controlled by 3 control signals for input operation, and is also controlled by 3 control signals for output operation. Functions of individual bits of Port C are specified as shown in the following table.

	Control Functions	Related Port	
		A	B
Input	$\overline{STB}$	PC_4	PC_2
	IBF	PC_5	PC_1
	INTR	PC_3	PC_0
Output	$\overline{OBF}$	PC_7	PC_1
	$\overline{ACK}$	PC_6	PC_2
	INTR	PC_3	PC_0

Out of above stated control functions, those related to input are as follows.

- Strobe Input ($\overline{STB}$): When $\overline{STB}$ = "0", data is loaded into the input latch

- Input Buffer Full (IBF): This signal shows that data has been already loaded. IBF is set by $\overline{STB}$ = "0" and is reset at the rising edge of $\overline{RD}$.

- Interrupt Request (INTR): If INTE flag is in the enable state and IBF = "1", INTR signal becomes "1" at $\overline{STB}$ = "1"

  INTR signal can be directly connected to INT input of the processor, and when data is loaded on a port, an interrupt signal is generated. INTR is reset when $\overline{RD}$ signal from the processor is received into the port.

On the other hand, control functions related to output are as follows.

- Output Buffer Full (OBF): This is a flag showing that the processor has loaded data on a specific port ($\overline{OBF}$ = 0). $\overline{OBF}$ becomes "0" at the rising edge of $\overline{WR}$ signal and becomes "1" at the falling edge of $\overline{ACK}$ signal from peripherals.

- Acknowledge ($\overline{ACK}$): When data has been received from a TMP8255AP-5 port, a peripheral responds to TMP8255AP-5 by transmitting an acknowledge signal $\overline{ACK}$ (low active).

- Interrupt Request (INTR): This output can be used to interrupt the processor when a peripheral has accepted data transmitted by the processor. If INTE flag is in the enable state and $\overline{OBF}$ = "1", INTR signal is set by $\overline{ACK}$ = "1" and is reset by $\overline{WR}$ = "0".

Mode 2

Under mode 2, Port A is used as a bidirectional bus. Both input and output of Port A are latched under this mode.

5 bits of Port C are used for control between peripherals and TMP8255AP-5. Signals used for this control are as follows:

$\overline{STB}$, IBF, $\overline{OBF}$ and INTR: The functions of these signals are identical in Mode 1.

$\overline{ACK}$: When this signal becomes active (low), 3-state output buffer of Port A is enabled to transfer data to peripheral equipment. During other periods, the output buffer is in high impedance.

For the selection enable/disable of INTE flip-flop, Bit 6 is used for output operation, and Bit 4 is used for input operation. Data transfer between the ports and peripherals is executed by designating pins of Port C same as in operations under Mode 1.

Under Mode 1 and 2, Port C status and control bits can be tested when Port C contents are read out. All bits of Port C are not used for control and status functions, unspecified bits can be programmed for input or output as described below.

In the case Port C has been programmed as output, Pins (PC_7 - PC_4) of Group A operate Port C by using the bit set/reset function. Pins (PC_3 - PC_0) of Group B controls write operation into Port C or read operation by using the bit set/reset function.

ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	RATING
T_{stg}	Storage Temperature	-65°C to 150°C
T_{opr}	Operating Temperature	0°C to 70°C
V_{CC}	Supply Voltage	-0.5V to 7.0V
V_{OUT}	Output Voltage	-0.5V to 7.0V
V_{IN}	Input Voltage	-0.5V to 7.0V
P_W	Power Dissipation	1.0W

D.C CHARACTERISTICS (Ta = 0°C to 70°C, V_{CC}=5V±5%, V_{SS}=0V)

SYMBOL	PARAMETER		TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V_{IL}	Input Low Voltage			-0.5		0.8	V
V_{IH}	Input High Voltage			2.0		V_{CC}	V
V_{OL}	Output Low Voltage	(DB)	I_{OL} = 2.5 mA			0.45	V
		(PER)	I_{OL} = 1.7 mA			0.45	V
V_{OH}	Output High Voltage	(DB)	I_{OH} = -400 μA	2.4			V
		(PER)	I_{OH} = -200 μA	2.4			V
I_{DAR} (Note 1)	Darlington Drive Current		V_{EXT} = 1.5V, R_{EXT} = 750Ω	-1.0		-4.0	mA
I_{IL}	Input Leak Current		0V ≤ V_{IN} ≤ V_{CC}			±10	μA
I_{OFL}	Output Leak Current (High Impedance State)		0V ≤ V_{OUT} ≤ V_{CC}			±10	μA
I_{CC}	Supply Current					120	mA

CAPACITANCE (Ta=25°C, V_{CC}=V_{SS}=0V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacity	fc = 1 MHz			10	pF
$C_{I/O}$	I/O Capacity				20	pF

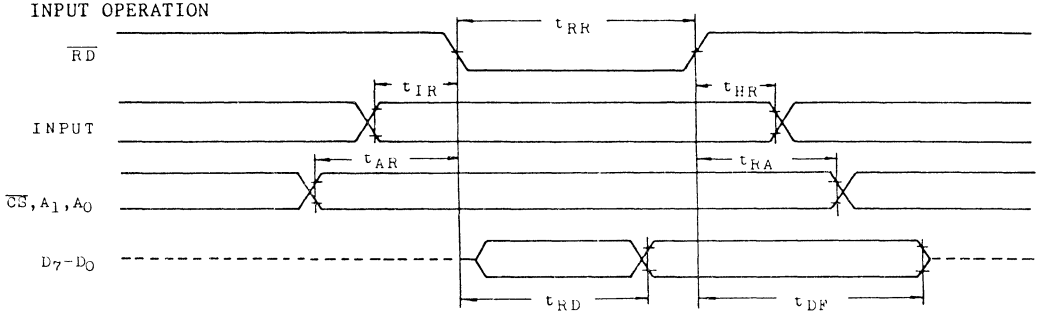
A.C. CHARACTERISTICS (Ta=0°C to 70°C, V_{CC}=5V±5%, V_{SS}=0V)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{AR}	Address Stable before $\overline{RD}$	0			ns
t_{RA}	Address Stable after $\overline{RD}$	0			ns
t_{RR}	$\overline{RD}$ Pulse Width	300			ns
t_{RD}	Data Valid from $\overline{RD}$ (Note 2)			200	ns
t_{DF}	Data Float after $\overline{RD}$	10		100	ns
t_{RV}	Time between READs and/or WRITEs	850			ns
t_{AW}	Address Stable before $\overline{WR}$	0			ns
t_{WA}	Address Stable after $\overline{WR}$	20			ns
t_{WW}	$\overline{WR}$ Pulse Width	300			ns
t_{DW}	Data Valid to $\overline{WR}$	100			ns
t_{WD}	Data Valid after $\overline{WR}$	30			ns
t_{WB}	$\overline{WR}$ = 1 to Output Delay (Note 2)			350	ns
t_{IR}	Peripheral Data before $\overline{RD}$	0			ns
t_{HR}	Peripheral Data after $\overline{RD}$	0			ns
t_{AK}	$\overline{ACK}$ Pulse Width	300			ns
t_{ST}	$\overline{STB}$ Pulse Width	500			ns
t_{PS}	Peripheral Data before Rising Edge of $\overline{STB}$	0			ns
t_{PH}	Peripheral Data after Rising Edge of $\overline{STB}$	180			ns
t_{AD}	$\overline{ACK}$ = 0 to Output (Note 2)			300	ns
t_{KD}	$\overline{ACK}$ = 1 to Output Float	20		250	ns
t_{WOB}	$\overline{WR}$ = 1 to $\overline{OBF}$ = 0 (Note 2)			650	ns
t_{AOB}	$\overline{ACK}$ = 0 to $\overline{OBF}$ = 1 (Note 2)			350	ns
t_{SIB}	$\overline{STB}$ = 0 to IBF = 1 (Note 2)			300	ns
t_{RIB}	$\overline{RD}$ = 1 to IBF = 0 (Note 2)			300	ns
t_{RIT}	$\overline{RD}$ = 0 to INTR = 0 (Note 2)			400	ns
t_{SIT}	$\overline{STB}$ = 1 to INTR = 1 (Note 2)			300	ns
t_{AIT}	$\overline{ACK}$ = 1 to INTR = 1 (Note 2)			350	ns
t_{WIT}	$\overline{WR}$ = 0 to INTR = 0 (Note 2)			850	ns

TIMING WAVEFORMS

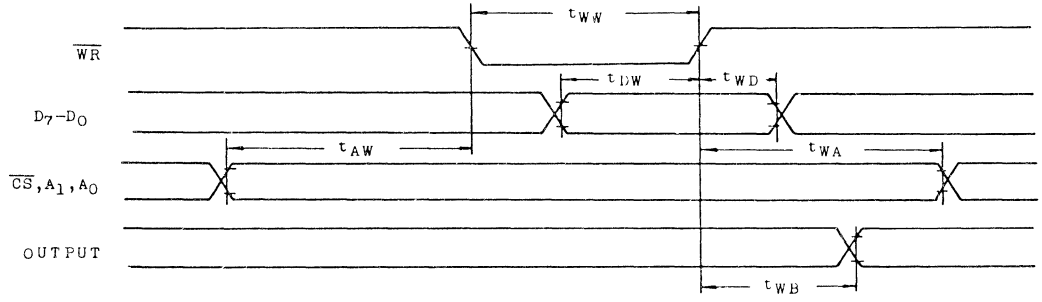
MODE 0

INPUT OPERATION



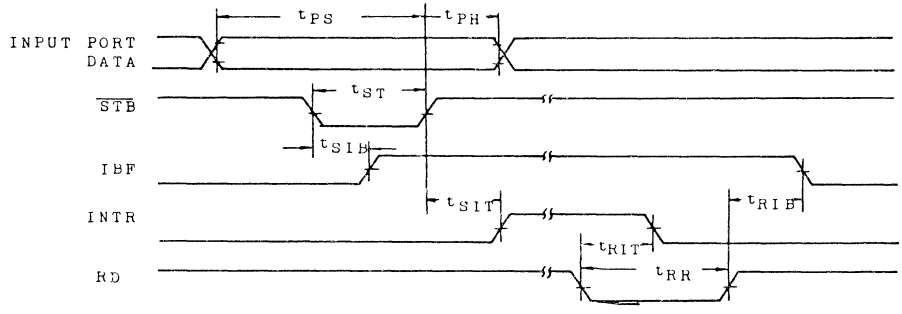
MODE 0

OUTPUT OPERATION



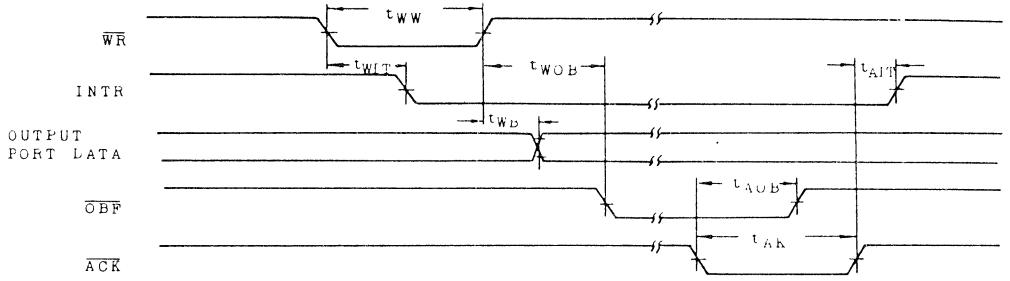
MODE 1

INPUT OPERATION



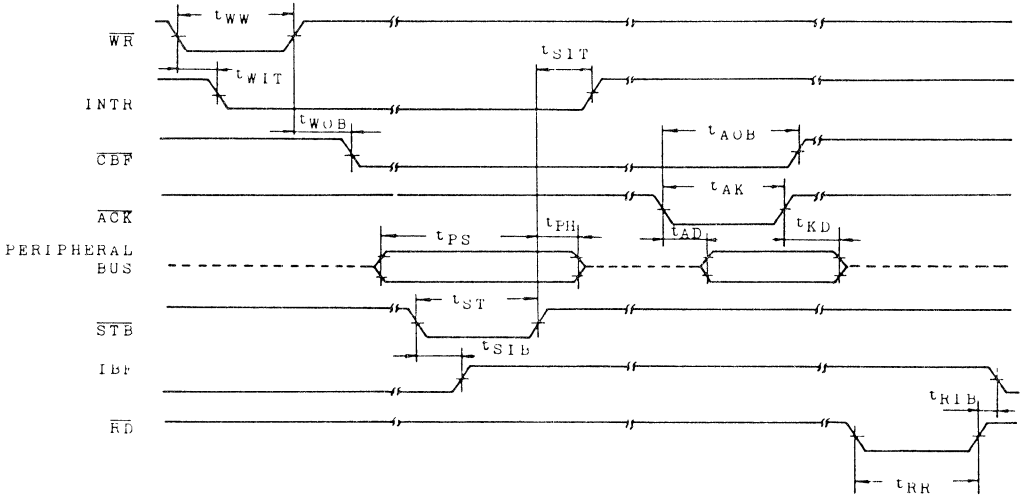
MODE 1

OUTPUT OPERATION



MODE 2

BIDIRECTIONAL OPERATION



Note 1. Available on any 8 pins of Port B and Port C.

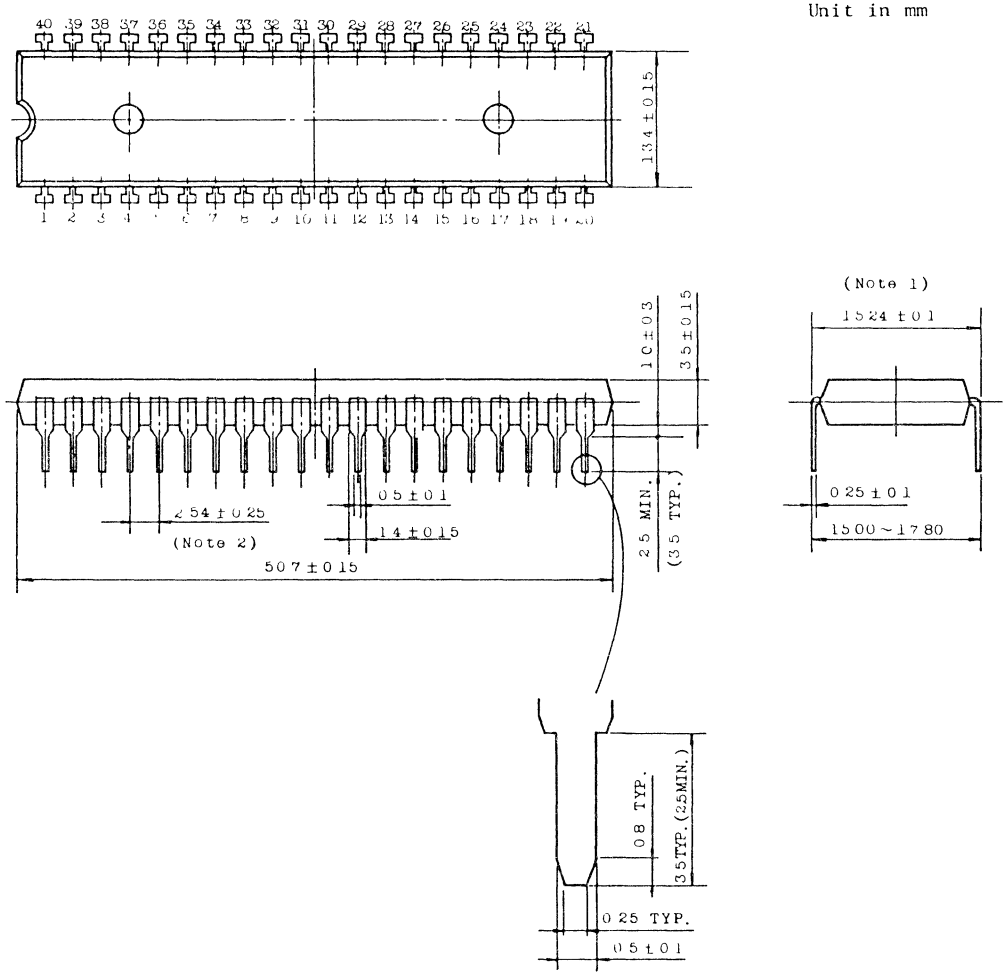
2. Test conditions; C_L = 150pF

3. Period of Reset pulse should be at least 50μs during or after power on. Subsequent Reset pulse can be 500ns min.

4. Timing measuring levels are as follows: high level = 2V
low level = 0.8V

OUTLINE DRAWING

Unit in mm



Note: 1. This dimension is measured at the center of bending point of leads.

2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoritical positions with respect to No.1 and No.40 leads.

TOSHIBA MOS TYPE DEGITAL
INTEGRATED CIRCUIT
Silicon Monolithic CMOS Silicon Gate

TMP82C59AP-2/TMP82C59AF-2

PROGRAMMABLE INTERRUPT CONTROLLER

GENERAL DESCRIPTION

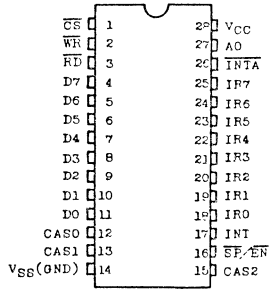
The TMP82C59AP-2/AF-2 (hereinafter referred to as TMP82C59A) is a programmable interrupt controller. It handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry.

FEATURES

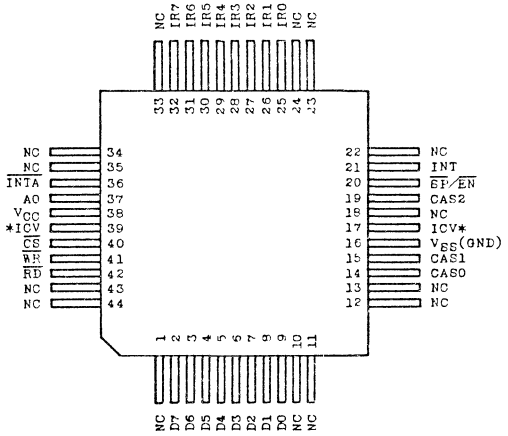
- o Eight Level Priority Controller.
- o Expandable to 64 Level.
- o Interrupt Modes, Interrupt Mask, Vectored Address Programmable.
- o Single +5V Power Supply.
- o 8085A, 8086 Microcomputer System Compatible.

PIN CONNECTIONS (TOP VIEW)

TMP82C59AP-2



TMP82C59AF-2



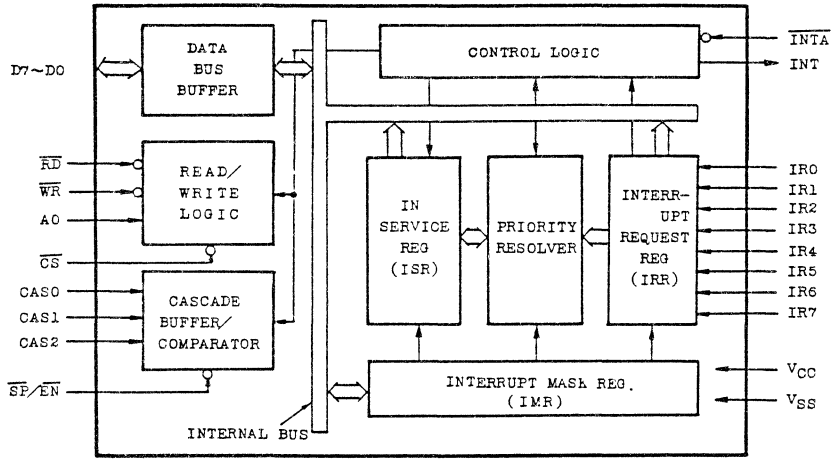
*) ICV (Pin17 and Pin39) must be connected with Vcc or must be OPEN
NC : No Connection.

PIN NAMES AND PIN DESCRIPTION

Pin Name	Input/Output	Function
$\overline{CS}$	Input	Chip Select Input. A low on this pin enables RD and WR communication between the CPU and the 82C59A. INTA functions are independent of CS.
$\overline{WR}$	Input	Write Control Input. A low on this pin when $\overline{CS}$ is low enables the 82C59A to accept command words from CPU.
$\overline{RD}$	Input	Read Control Input. A low on this pin when $\overline{CS}$ is low enables the 82C59A to release status onto the data bus for the CPU.
D0 to D7	Input/Output	Bidirectional Data Bus. Command status and interrupt-vector information is transferred via this bus.
CAS0 to CAS2	Input/Output	Cascade Lines. The CAS lines form a private 82C59A bus to control a multiple 82C59A structure. These pins are outputs for a master 82C59A and inputs for a slave 82C59A.
$\overline{SP}/\overline{EN}$	Input/Output	Slave Program/Enable Buffer. This is a dual function pin. When in the buffered mode it can be used as an Output to control buffer transceivers ($\overline{EN}$). When not in the buffered mode it is used as an input to designate a master 82C59A ($\overline{SP}$=1) or a slave ($\overline{SP}$=0).
INT	Output	Interrupt Request Output. This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU. It is conected to CPU's interrupt pin.
IR0 to IR7	Input	Interrupt Request Inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on a IR input (Level Triggered Mode).
$\overline{INTA}$	Input	Interrupt Acknowledge Input. This pin is used to enable 82C59A interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.

Pin Name	Input/Output	Function
A0	Input	A0 Address Line. This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the 82C59A to decipher various command words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line.
VCC		+5V Power Supply
VSS		Ground

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The TMP82C59A is connected to the system bus as shown in Fig. 1. and operates as an interrupt controller.

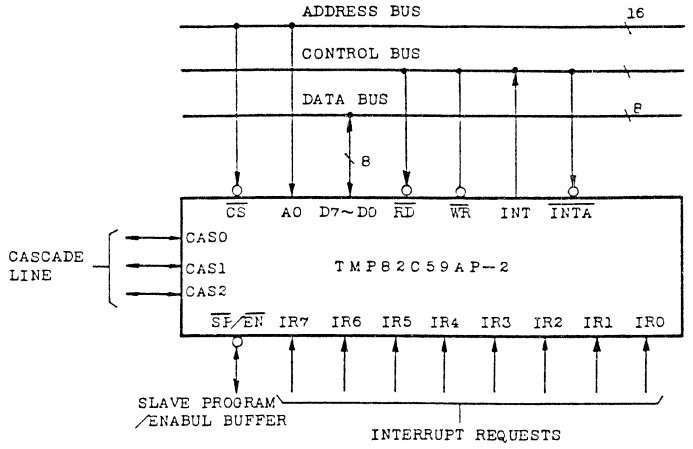


Fig. 1 Interface to System Bus

Whenever interrupt request is accepted at the 8 level interrupt request input, the TMP82C59A, judging its mask status and priority, output interrupt signal to CPU for requesting interrupt. Then, according to response signal ($\overline{\text{INTA}}$ signal) from CPU or the system controller, the TMP82C59A outputs CALL command code and vectored address data on the data bus. CPU starts the interrupt service routine and the TMP82C59A stores which interrupt request has been serviced. At the end of the service routine, CPU resets it and informs the TMP82C59A of its end.

A0	D4	D3	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{CS}}$	
						READ OPERATION
0			0	1	0	IRR, ISR or Interrupt request level → Data bus
1			0	1	0	IMR → Data bus
						WRITE OPERATION
0	0	0	1	0	0	Data bus → OCW2
0	0	1	1	0	0	Data bus → OCW3
0	1	x	1	0	0	Data bus → ICW1
1	x	x	1	0	0	Data bus → OCW1, ICW2, ICW3 or ICW4
						HIGH IMPEDANCE
x	x	x	1	1	0	Data bus (D7 to D0) High impedance
x	x	x	x	x	1	Data bus (D7 to D0) High impedance

Table 1 Basic Operation

[SYSTEM CONFIGURATION]

The TMP82C59A consists of the following components.

(1) Interrupt Request Register (IRR) and Inservice Register (ISR)
(2) Priority Resolver
(3) Interrupt Mask Register (IMR)
(4) Data Bus Buffer
(5) Read/Write Logic
(6) Cascade Buffer/Comparator

(1) Interrupt Request Register (IRR) and Inservice Register (ISR)
Interrupt requests to the interrupt request input are processed by 2 registers IRR and ISR. IRR holds interrupt request to the interrupt request input while ISR holds all interrupt levels that are being serviced by CPU. Contents of IRR and ISR can be read out.

(2) Priority Resolver
The priority resolver is the block that decides interrupt request to be sent to CPU by judging priority. If the interrupt mask register (IMR) cooresponding to the interrupt request terminal does not sent the mask request, IRR sends interrupt requests to the priority resolver. Normally, when the interrupt reqeust level having the highest priority among these interrrupt request is higher than the content of ISR, that is, the priority of the interrupt request being serviceed by CPU, the TMP82C59A sends INT signal to CPU. When $\overline{INTA}$ signal is input as a response from CPU, the TMP82C59A sends CALL command and vectored address corresponding to an interrupt request of the highest priority to CPU, and resetting IRR bit corresponding to the interrupt request, sets ISR bits. CPU processes the interrupt service, sends a command to TMP82C59A to accept interrupt requests of lower priority at the end of the interrupt service, and resets the corresponding ISR bits. The priority resolver has a register to assign the interrupt request input of lowest priority.

(3) Interrupt Mask Register (IMR)
The interrupt mask register normally acts only on IRR, and disables interrupt requests of the masked interrupt request input. The mask for high priority interrupt request input does not affect lower priority interrupt request. In the special mask mode, this register also acts on ISR and enables acceptance of lower level interrupt requests than the interrupt request being serviced. The content of IMR can be read out.

(4) Data Bus Buffer
This data bus buffer consists of 8 bit 3 state bidirectional bus buffer and acts as the interface with the system bus. Command word to and status information and CALL command vectored address readout from the TMP82C59A are transfered via this bus buffer.

(5) Read/Write Logic
This circuit controls the functions for decoding and accepting command words from CPU and for feeding status information to the data bus.

In addition, this circuit controls operations including ICW (Initialization Command Word) register and OCW (Operation Set Command Word) register.

$\overline{CS}$ Low level input to $\overline{CS}$ input enables $\overline{RD}$ or $\overline{WR}$ input operation.

$\overline{WR}$ When WR input is made to low level together with $\overline{CS}$ input, command write to the TMP82C59A is enabled.

$\overline{RD}$ When $\overline{RD}$ is made to low level together with $\overline{CS}$ input, readout of the contents of ISR, IRR and IMR and interrupt level in the poll mode on the data bus is enabled.

A0 A0 is used together with $\overline{WR}$ and $\overline{RD}$ signals for command write or status readout. It acts as a read select signal for one of command word discrimination information or status information. It is normally connected to one of the address lines.

(6) Cascade Buffer/Comparator
This block stores the identification code as the slave and during the programming as the slave, compares the identification code with data on the 3 bit cascade line (CAS0-2). When both agree, the slave interpretes that the slave itself is selected. In the case of the master, an identification signal corresponding to the accepted interrupt request inputs are output for a period from the input of initial $\overline{INTA}$ signal to the final $\overline{INTA}$ signal (second or third signal).

[INTERRUPT SEQUENCE]

(1) When the TMP8085A is used as CPU

(a) When one or more interrupt request become high level, IRR bits corresponding to that input are set.
(b) The TMP82C59A judges the mask status and priority of these interrupt and outputs INT signal to CPU as necessary.
(c) CPU outputs $\overline{INTA}$ signal in response to INT signal.
(d) Upon receipt of $\overline{INTA}$ signal, the TMP82C59A outputs CALL command on the data bus.
(e) As CALL command is a 3 byte command, two $\overline{INTA}$ signals are consecutively sent from CPU.
(f) Upon receipt of these two $\overline{INTA}$ signals, the TMP82C59A outputs the preprogrammed vector address corresponding to the highest priority interrupt request at time of (d) on the data bus. The TMP82C59A outputs the low-order address and then, the high-order address in response to the first and next $\overline{INTA}$ signals, respectively.
Furthermore, the TMP82C59A sets ISR bit corresponding to the interrupt request and resets IRR bit.
(g) The above operations complete CALL command and vector address output and CPU executes the interrupt service. In AEOI mode, ISR bits are automatically reset after CALL command is output. Otherwise, ISR bits are kept in the set status till EOI command is input.

(2) When the 8086 is used as CPU

(a) to (c) Same as (a) to (c) for the TMP8085A.

(d) Even when $\overline{INTA}$ signal is received, the TMP82C59A keeps the data bus in high impedance state.

(e) Another $\overline{INTA}$ signal is further sent from CPU. The TMP82C59A outputs 8 bit pointer on the data bus, and sets corresponding ISR bit and resets IRR bit.

(f) The above operations complete the interrupt cycle. In AEOI mode, ISR bit are automatically reset after the final $\overline{INTA}$ signal is received. Otherwise, ISR bits kept in the set status till EOI command is input.

Further, if there is not interrupt request at time of step (d) of the above interrupt sequence, (i.e., the request was too short in duration), the TMP82C59A performs the same operations as those when interrupt request are generated at IR7, but ISR bits are not set.

[INTERRUPT SEQUENCE OUTPUT]

(1) When the TMP8085A is used as CPU
CALL command code is output on the data bus upon receipt of the first INTA signal and the low-order vectored address and the high-order vectored address on the data bus upon receipt of the second and third INTA signals, respectively.
The vectored address A5 to A15 on Table 2 must be programmed in advance on the TMP82C59A. The remaining bits of the vectored addresses are produced by the TMP82C59A corresponding to interrupt request.

(2) When the 8086 is uses as CPU
When the first INTA signal is received, the data bus is placed in the high impedance state. When the second INTA signals is received, 8 bit pointer is output on the data bus.
The 8 bit pointers T7 to T3 shown on Table 3 must be programmed in advance on the TMP82C59A. The remaining bits are automatically produced by the TMP82C59A corresponding to interrupts.

[PROGRAMMING TMP82C59A]

The TMP82C59A accepts the following 2 types of command words.

For First $\overline{INTA}$

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	1	1	0	1

For Second $\overline{INTA}$

IR	INTERVAL=4							
	D7	D6	D5	D4	D3	D2	D1	D0
IR7	A7	A6	A5	1	1	1	0	0
IR6	A7	A6	A5	1	1	0	0	0
IR5	A7	A6	A5	1	0	1	0	0
IR4	A7	A6	A5	1	0	0	0	0
IR3	A7	A6	A5	0	1	1	0	0
IR2	A7	A6	A5	0	1	0	0	0
IR1	A7	A6	A5	0	0	1	0	0
IR0	A7	A6	A5	0	0	0	0	0

IR	INTERVAL=8							
	D7	D6	D5	D4	D3	D2	D1	D0
IR7	A7	A6	1	1	1	0	0	0
IR6	A7	A6	1	1	0	0	0	0
IR5	A7	A6	1	0	1	0	0	0
IR4	A7	A6	1	0	0	0	0	0
IR3	A7	A6	0	1	1	0	0	0
IR2	A7	A6	0	1	0	0	0	0
IR1	A7	A6	0	0	1	0	0	0
IR0	A7	A6	0	0	0	0	0	0

For Third $\overline{INTA}$

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

Table 2 Interrupt Sequence Output (8085A Mode)

(1) Initialization Command Words (ICW)
Prior to operating the TMP82C59A it is necessary to program this command.

(2) Operation Command Words (OCW)
This command is for operating the TMP82C59A in various operating modes and is programmable anytime during the TMP82C59A is in operation.

(1) ICW
There are 4 kinds of commands; ICW1, ICW2, ICW3 and ICW4.
Each of these command is not programmable independently. The initialization is made according to the initialization command sequence shown in Fig. 2. ICW3 is used for cascade connection and ICW4 is for setting a special mode.

ICW1

When A0 = 0 and D4 = 1, the initialization is interpreted as ICW1 and the initialization of following 5 items is made independently of content of the command:

[1] The interrupt mask register (IMR) is cleared.
[2] The interrupt request input IR7 becomes the lowest priority.
[3] The special mask mode is cleared and IRR is assigned as the register for reading status information.
[4] When IC4 = 0, all function bits of ICW4 are set at "0".
[5] The edge detection circuit of the interrupt request terminal is cleared.

The format of ICW1 is shown in Fig. 3.
ICW1 makes the assignment of vector addresses A7 to A5, assignment as to whether the interrupt request input is to be made in the edge trigger mode or the level trigger mode (LTIM), assignment of CALL address intervals when the TMP8085A is used as CPU (refer to Table 2) (ADI), assignement as to whether the cascade connection to be made (SNGL) and assignment as to whether ICW4 is needed (IC4).

For First $\overline{INTA}$

High Impedance

Second $\overline{INTA}$

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

Table 3 Interrupt Sequence Output (8086 Mode)

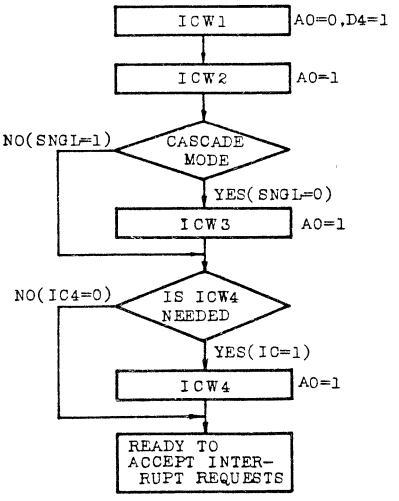
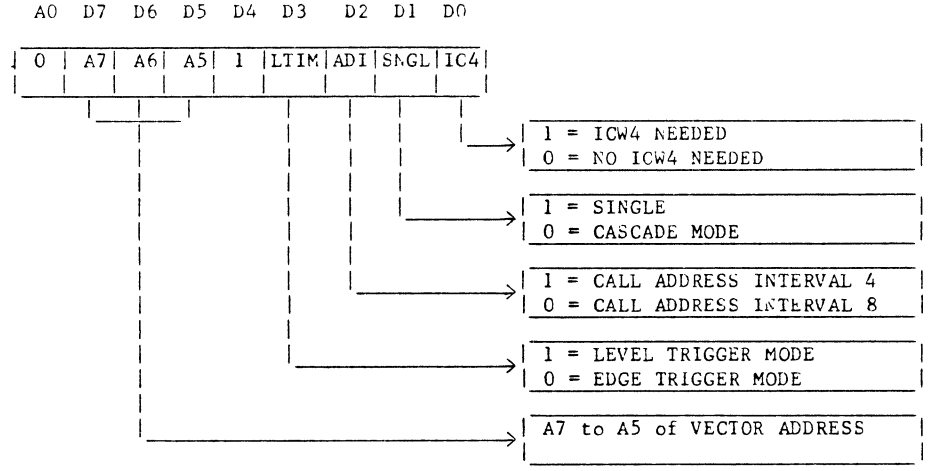


Fig.2 Initialization Command Sequence

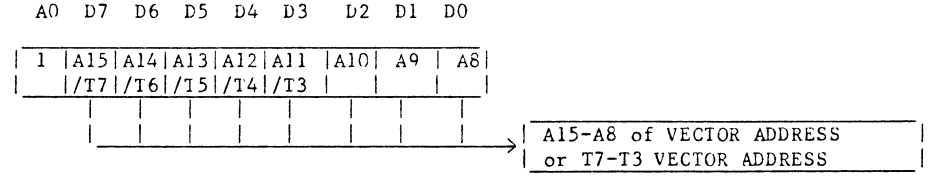
ICW2

ICW2 assigns high-order vector addresses A6 to A15 when the 8085A is used as CPU or 5-bit pointers T3 to T7 when the 8086 is used as CPU. The TMP82C59A interpretes a command written with A0 input made to "H" level after ICW1 written as ICW2. The format of ICW2 is shown in Fig. 3.

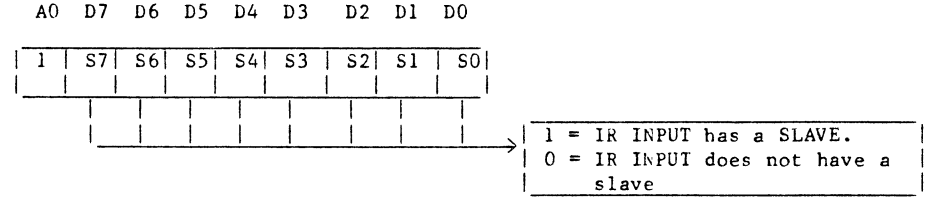
ICW1



ICW2



ICW3



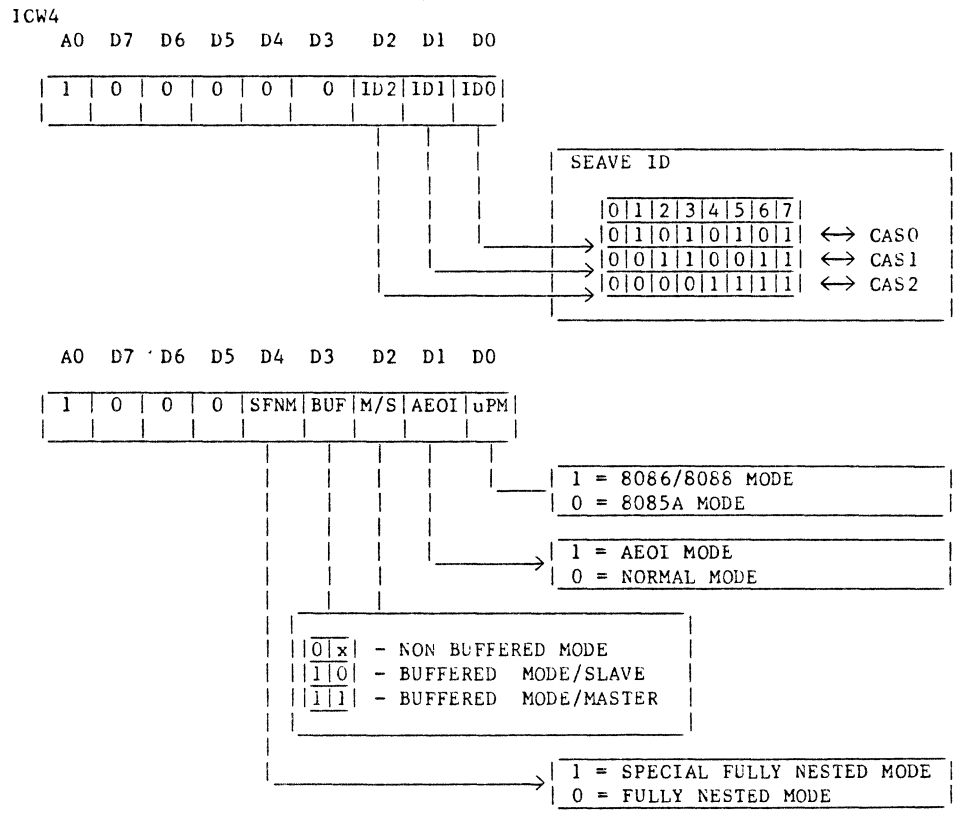


Fig. 3 ICW Format

ICW3

This is a command required for cascade connection of plural number of TMP82C59As. When SNGL = 0 in ICW1, the TMP82C59A interpretes a command written with A0 input made at "H" level after ICW2 as ICW3.

[1] Master Mode

In the master mode, the TMP82C59A specifies individually as to whether a slave device is added to each interrupt request input.

If the TMP8085A is used as CPU when addition of a slave device is specified, the master device outputs CALL command code on the data bus upon receipt of the first $\overline{\text{INTA}}$ signal and simultaneously outputs the slave identification code to the cascade line.

The master device becomes high impedance at the second and third $\overline{\text{INTA}}$ signals, and the slave device selected by the identification code outputs vector address on the data bus. When the 8086 is used as CPU, both the master and slave devices become high impedance at the first INTA signal. Simulataneously, the master device outputs the slave identification code to the cascade line. The master device also

becomes high impedance at the second $\overline{INTA}$ signal and the selected slave device outputs a pointer on the data bus.
When it is specified that no slave device is added, the master device outputs both CALL command code and vector address as a response to $\overline{INTA}$ signal and simultaneously outputs "L" signal to 3 cascade lines. This is the same as the identification code of the slave device connected to IR0 and therefore, in the case of the interrupt request input without the slave device, added, no slave device can be added to IR0.
Further, to specify the master slave, the $\overline{SP}/\overline{EN}$ terminal must be set at "H" level or BUF must be set at 1 and M/S at 1 by ICW4.

[2] Slave Mode
In the slave mode, the TMP82C59A specifies the slave identification code.
The slave device compares its identification code with the identification code sent from the master device via the cascade line and if they agree, outputs vector addresses on the data bus upon receipt of the second and third $\overline{INTA}$ signals.
Further, to specify the slave mode, the $\overline{SP}/\overline{EN}$ terminal must be set at "L" level or BUF at 1 and M/S at 1 by ICW4. The format of ICW3 is shown in Fig. 3.

ICW4

ICW4 is effective only when IC4 = 1 in ICW1.
Although ICW4 is effective for assignment of the special fully nested mode (SFNM), assignment of the buffer mode (BUF) and in the buffer mode, this command makes the assignment of the master/slave (M/S), automatic EOI (AEOI) and CPU mode. When IC4 = 0 in ICW1, all function bits of ICW4 are set at "0". The format of ICW4 is shown in Fig. 3.

(2) OCW
There are 3 kinds of commands: OCW1, OCW2 and OCW3. Any time after ICW is programmed, these command can be programmed to set the TMP82C59A in various operation modes.

OCW1
After ICW is set, the TMP82C59A interpretes the operation set command to be OCW1 when A0 = 1. This command is used for setting the content of the interrupt mask register (IMR). The OCW1 format is shown in Fig. 4.

OCW2
The TMP82C59A interpretes the operation set command to be OCW2 when A0 = 0, D4 = 0 and D3 = 0. This command is used for outputting EOI L2 to L0 are effective only in the case of specific EOI and specific rotation. The OCW2 format is shown in Fig. 4.

OCW3
The TMP82C59A interpretes the operation set command to be OCW3 when A0 = 0, D4 = 0 and D3 = 1. This command is used for assigning the special mask mode, the poll mode and register for status information readout, that is, assigning IRR or ISR. The OCW3 format is shown in Fig. 4.

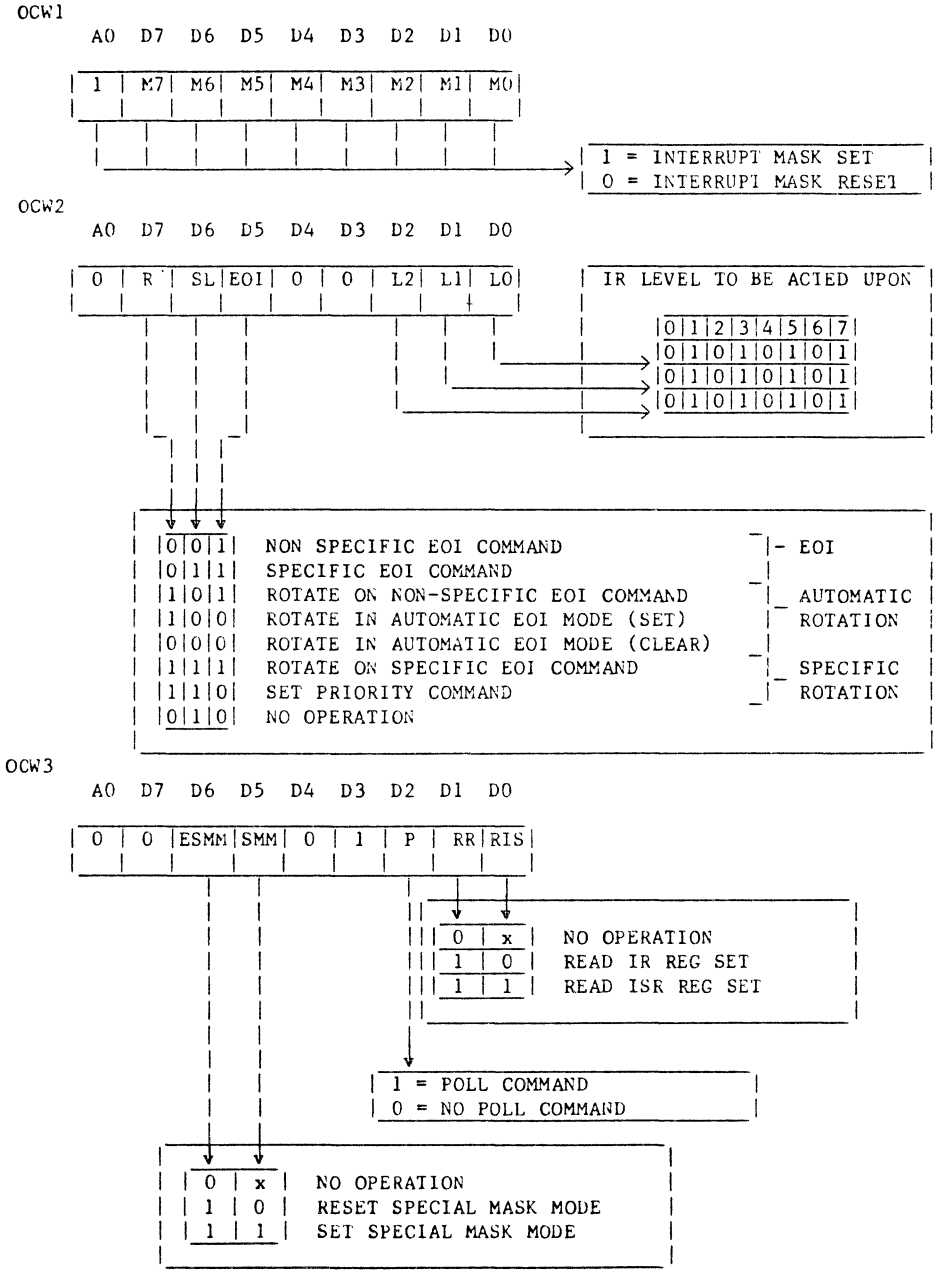


Fig. 4 OCW Format

[EXPLANATION OF MODES AND COMMANDS]

(1) FULLY NESTED MODE

Unless other modes are specified, the TMP82C59A operates in this mode. Under this mode, priority of the interrupt request inputs is most high at IR0 and becomes low in order toward IR7.

When $\overline{INTA}$ signal is input, vector address corresponding to an interrupt and request having the highest priority at the time is output together with CALL command code on the data bus and furthermore, corresponding ISR bits are kept set till EOI command is input to the TMP82C59A before CPU returns from the service routine or to the final leading edge of $\overline{INTA}$ pulse in AEOI mode. As long as these ISR bits are kept set, low priority interrupt requests are ignored. Priority can be changed by OCW2.

(2) EOI (END OF INTERRUPT)

EOI command is used to reset ISR bits. It is necessary for CPU to output EOI command before returning from the service routine.

When AEOI is set in ICW4, ISR bit are automatically reset at the leading edge of the final $\overline{INTA}$ pulse and it is therefore not necessary to output EOI command. As ISR bits are set in both the master and slave devices when cascade connected, it is necessary to output EOI command to to both master device and the slave device corresponding to the master device.

EOI command is available in 2 kinds: non-specific EOI and specific EOI commands.

When non-specific EOI command is output to the TMP82C59A, ISR bit having the highest priority among ISR bit is reset. However, in the special mask mode it is not possible to reset ISR bit that are masked by IMR by the non-specific EOI command, and ISR bit having the highest priority among the unmasked ISR bits is reset. On the other hand, it is possible to specify ISR bit to be reset by the specific EOI command by a program. EIO command is executed by OCW2.

(3) AEOI (AUTOMATIC EOI) MODE

In this mode, the non-specific EOI operation is automatcally executed at the leading edge of the final $\overline{INTA}$ signal.

Therefore, this mode cannot be used for multiple interruptions. In addition, this mode also cannot be used in the slave TMP82C59A. The TMP82C59A can be set in AEOI mode by setting AEOI bit in ICW4 to 1.

(4) AUTOMATIC ROTATION

This mode is effective in the application to give equal priority to the interrupt devices.

In this mode, whenever the interrupt service ends, priority of each interrupt request is updated so that the serviced interrupt request is set at the lowest priority. Priority of interrupt request input IRn (n=0 to 7) that has been serviced becomes the lowest priority level 7 and becomes high in order toward IR0 and then, IR7 and next IRn+1 become the highest priority level 0. (Rotation Priority)

For instance, when the interrupt request IR4 is serviced as shown in the figure at the right hand, priority of each interrupt request input is updated.

This mode specifies R = 1, SL = 0 and EOI = 1 by OCW2 at the end of service. Further, in case of AEOI mode, when R = 1, SL = 0 and EOI = 0 are specified by OCW2, the internal flip-flop is set and the TMP82C59A operates in this mode. If R = 0, SL = 0 and EOI = 0 are specified by OCW2, this mode is cleared.

Before ROTATION (highest pririty interrupt request IR4 is being serviced.)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
ISR	0	1	0	1	0	0	0	0
Priority	7	6	5	4	3	2	1	0

Lowest priority — Highest priority

After ROTATION (Interrupt request IR4 is being servied.)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
ISR	0	1	0	0	0	0	0	0
Priority	2	1	0	7	6	5	4	3

Highest priority — Lowest priority

(5) SPECIFIC ROTATION

In the automatic rotation mode, priority of each interrupt request input is updated whenever interrupt requests are serviced. Under this mode it is possible to change priority by specifying an interrupt request input to be set at the lowest priority by a program. Priority is determined according to the rotation priority. In this mode, R and SL are set at 1 by OCW2 and interrupt request input that is to be set at lowest priority at L2 to L0 is specified. Priority can be changed simultaneously with EOI command or independently regardless of EOI command.

(6) INTERRUPT MASK

Each interrupt request input can be masked individually by the interrupt mask register (IMR). Content of IMR can be specified by OCW1.

(7) SPECIAL MASK MODE

Normally when an interrupt service routine is being executed, lower priority interrupt requests than the interrupt request being serviced are ignored unless ISR bits are reset by EOI command. This special mode is used for an application in which an interrupt request of lower priority is approved during the service. In this mode IMR also acts as the mask for ISR. That is , the TMP82C59A processes an interrupt request by assuming that ISR bit and IRR bit corresponding to IMR bit set at "1" have not been set. This mode is set by setting ESSM = 1 and SMM = 1 by OCW3. Further, when ESSM = 1 and SMM = 0 are assigned by OCW3, this mode is cleared to the normal mode. The IMR programming is made by OCW1.

(8) POLL COMMAND

This mode is used in a state where the internal interrupt enable flip-flop of CPU is disabled and no interrupt is authorized. The service to the device is made by using the poll command. The poll command specifies P=1 in OCW3. The mode becomes now the poll mode. When the read operation ($\overline{RD}$=0, $\overline{CS}$=0) is made on the TMP82C59A, the following output is made on the data bus:

	D7	D6	D5	D4	D3	D2	D1	D0
	I	-	-	-	-	W2	W1	W0

W0 - W2 : Binary code of highest priority interrupt request among interrupt requests to the interrupt request inputs.

I : There is an interrupt request to CPU when I = 1.

The TMP82C59A interpretes $\overline{RD}$ signal as the interrupt acknowledge and when D7 = 1 is output, sets corresponding ISR bit. This poll mode is valid for a period from $\overline{WR}$ (P = 1 in OCW3) to next $\overline{RD}$ ($\overline{CS}$ = 0). Further, an interrupt request to be serviced is determined at the time when the mode is made to the poll mode and even when a new or high priority interrupt request is sent between $\overline{WR}$ and $\overline{RD}$, it is not accepted.

(9) READING STATUS

CPU is capable of reading the contents of 3 registers (IRR, ISR, IMR). When the reading operation is made at A0 = 0, the content of IRR or ISR can be read out. Selection of IRR and ISR is made by OCW3. When RR is set at 1 and RIS at 0, IRR is assigned and when RR and RIS are set at 1, ISR is assigned.

This assignement is kept stored without necessity for performing at every reading operation. IMR is read when A0 = 1. If the poll mode is specified before the reading operation, the poll command has priority.

(10) EDGE TRIGGERD MODE/LEVEL TRIGGERD MODE

This mode is selected by LTIM of ICW1.

When LTIM is 0, the edge triggered mode is selected and interrupt request is triggered at the leading edge of the interrupt request signal and kept continued by holding "H" level. When LTIM is 1, the level triggered mode is selected and interrupt request is recognized by "H" level of the interrupt request signal. For both modes it is necessary to hold the interrupt request input at "H" level by triggering it till the fast $\overline{INTA}$ signal is output from CPU. If the interrupt request input is at "L" level when $\overline{INTA}$ signal is output from CPU, the same operations as those when interrupt requests are generated at IR7 are performed but ISR bits are not set.

(11) SPECIAL FULLY NESTED MODE

This mode is used to give priority to the interrupt request input for the slave devices when they are cascade connected.
This mode is assigned to the master TMP82C59A when SFNM is 1 in ICW4.
With the exception of the following 2 points, this mode is identical to the fully nested mode.

[1] Even when an interrupt request from a slave device is being serviced, the master device accepts a higher priority interrupt request from the same slave device without ignoring it. (In the fully nested mode, a higher priority interrupt request from the slave device that is now being serviced is ignored and interrupt requests from a higher priority slave device only are accpeted.)

[2] When an interrupt request from a slave device is being serviced, it is necessary to check by a software as to whether the interrupt request is only one interrupt request from that slave device.
When the service ended, after the non-specific EOI is output to that slave device, CPU has to check whether all ISR bits of that slave device are "0". If they are all "0", that slave has no interrupt request being serviced and therefore, the non-specific EOI is output to the master device to allow acceptance of interrupt request from the lower priority slave devices.
Otherwise, the non-specific EOI must not be output to the master device.

(12) BUFFERED MODE

This mode is to output an enable signal to a data bus buffer from the $\overline{SP}/\overline{EN}$ terminal when the data bus buffer is needed for the data bus on a large system. Under this mode, "L" level signal is output to the $\overline{SP}/\overline{EN}$ terminal whenever the data bus output of the TMP82C59A is enabled. The assingment of this mode is made by ICW4 simultaneously with the assingment of the master/slave devices.

(13) CASCADE MODE

The TMP82C59A is able to process interrupt requests up to 64 levels by one master and 8 slave devices.
The cascading is shown in Fig. 5. The master TMP82C59A selects the slave devices by identification codes using 3 cascade lines. INT output of each slave device is connected to the interrupt request inputs of the master device. Further, the identification codes corresponding to respective connections are assigned for the slave devices by ICW3.

When interrupt request are generated at the interrupt request inputs of the slave devices and accepted, the master device outputs the identification code to the slave device at the first $\overline{INTA}$ signal trailing edge to output vector address or pointer. This identification code is kept maintained to the leading edge of the final $\overline{INTA}$ signal. Normally, the master device outputs "L" level signal to all cascade line. EOI command must be output twice; to the master and second, to the slave corresponding to the interrupt service. Further, an address decoder is required to activate to the $\overline{CS}$ input of each TMP82C59A.

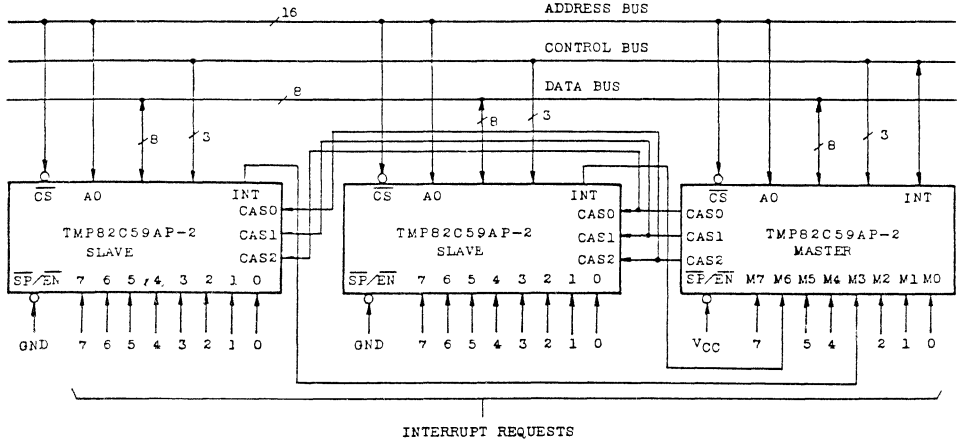


Fig. 5 CASCADING

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
VCC	VCC Supply Voltage (with respect to VSS (GND)	-0.5 to +7V
VIN	Input Voltage	-0.5to+Vcc+0.5
PD	Power Dissipation	250 mW
Tsol	Soldering Tmeperature (Soldering Time 10 sec)	260°C
Tstg	Storage Temperature	-65°C to+150°C
Topr	Operating Tempertature	-40°C to 85°C

DC CHARACTERISTICS Ta=-40 to +85°C,VCC=5V±10%,Vss(GND)=0V,
Unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage		-0.5	-	0.8	V
VIH	Input High Voltage		2.2	-	VCC+0.5	V
VOL	Output Low Voltage	IOL = 2.2mA	-	-	0.45	V
VOH1	Output High Voltage	IOH = -400uA	2.4	-	-	V
VOH2	Output High Voltage	IOH = -100uA	VCC -0.8	-	-	V
ILI	Input Leak Current	0V≤VIN≤VCC	-	-	±10	uA
ILOL	Output Leak Current	0.45V<VIN<VCC	-	-	±10	uA
ILIR	Input Current (IR)	VIN = 0V	-	-	-300	uA
		VIN = VCC	-	-	10	uA
ICC1	Operating Supply Current	I/O CYCLE=1uS VIH=VCC-0.2V VIL = 0.2V			5	mA
ICC2	Stand-by Supply Current	VIH=VCC-0.2V VIL=0.2V			10	uA

INPUT CAPACITANCE (Ta=25°c, V_{CC}=V_{SS}(GND)=0V)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
CI	INPUT CAPACITANCE	f_C=1 MHz Unmeasured pins, 0V			10	pF
$C_{I/O}$	INPUT/OUTPUT CAPACITANCE				20	pF

AC CHARACTERISTICS
Ta=-40°C to +85°C,VCC=5V±10%,VSS(GND)=0V,Unless otherwise noted.

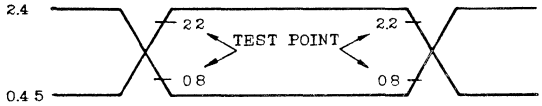
TIMING REQUIREMENTS

SYMBOL	PAREMETER	MIN.	MAX.	UNIT
TAHRL	A0/$\overline{CS}$ Setup Time ($\overline{RD}$)	0	-	ns
TRHAX	A0/$\overline{CS}$ Hold Time ($\overline{RD}$)	0	-	ns
TRLRH	$\overline{RD}$ Pulse Width	160	-	ns
TAHWL	A0/$\overline{CS}$ Setup Time ($\overline{WR}$)	0	-	ns
TWHAX	A0/$\overline{CS}$ Hold Time ($\overline{WR}$)	0	-	ns
TWLWH	$\overline{WR}$ Pulse Width	120	-	ns
TDVWH	D0 to D7 Setup Time ($\overline{WR}$)	120	-	ns
TWHDX	D0 to D7 Hold Time ($\overline{WR}$)	0	-	ns
TJLJH	Interrupt Request Pulse Width (LOW)	100	-	ns
TCVIAL	Cascade Setup Time (Second or Third $\overline{INTA}$)	40	-	ns
TRHRL	$\overline{RD}$ to Next Command	160	-	ns
TWHWL	$\overline{WR}$ to Next Command	190	-	ns
TCHCL	End of Command to next Command (Not Same) End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence	250		ns

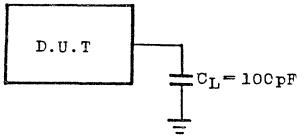
RESPONSE CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
TRLDV	Valid Data Delay ($\overline{RD}/\overline{INTA}$)		-	-	120	ns
TRHDZ	Data Floating ($\overline{RD}/\overline{INTA}$)	D0 to D7	10	-	85	ns
TJHIH	Interrupt Output Delay (IR)	CL=100pF	-	-	300	ns
TIALCV	Valid Cascade Delay ($\overline{INTA}$)	INT	-	-	360	ns
TRLEL	Enable Active ($\overline{RD}/\overline{INTA}$)	CL=100pF	-	-	100	ns
TRHEH	Enable Inactive ($\overline{RD}/\overline{INTA}$)	CAS0 to CAS2	-	-	150	ns
TAHDV	Valid Data Delay (A0/$\overline{CS}$)	CL=100pF	-	-	200	ns
TCVDV	Valid Data Delay (CAS0 to CAS2)		-	-	200	ns

AC Testing I/O Waveform

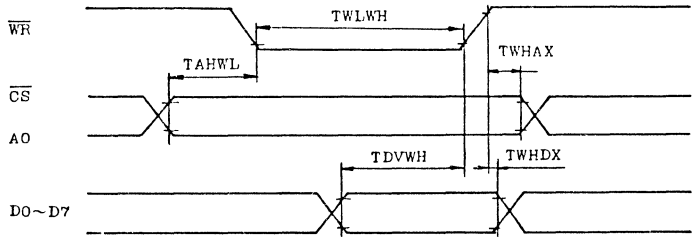


AC Testing Load Circuit

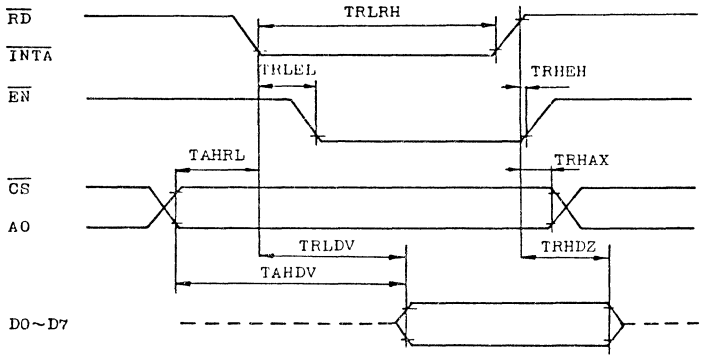


TIMING WAVEFORMS

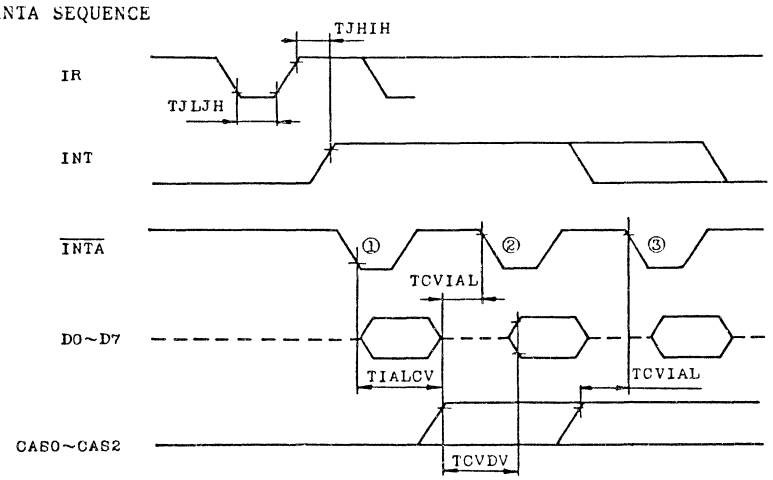
WRITE OPERATOIN



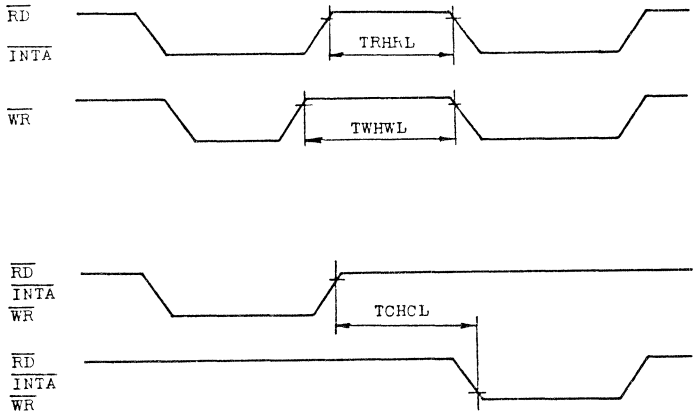
READ AND INTA OPERATION



INTA SEQUENCE



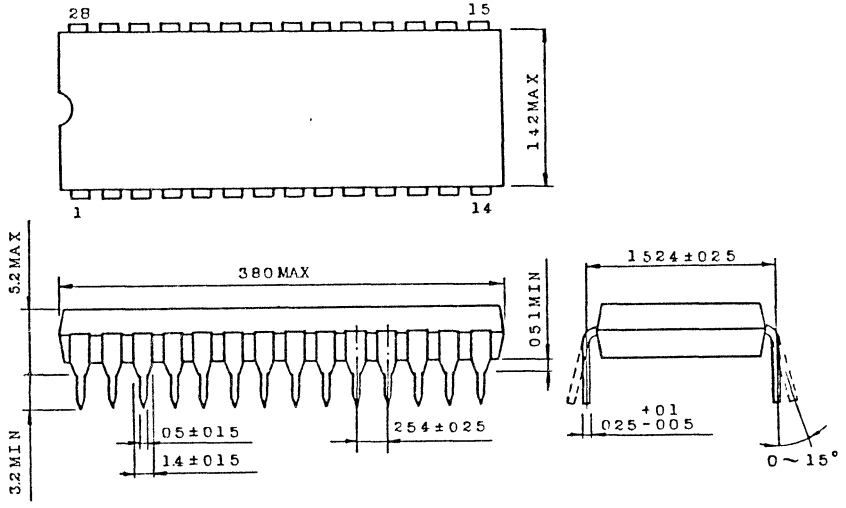
OTHER TIMING



EXTERNAL DIMENSION VIEW

28 pins PRASTIC DIP

Unit in mm

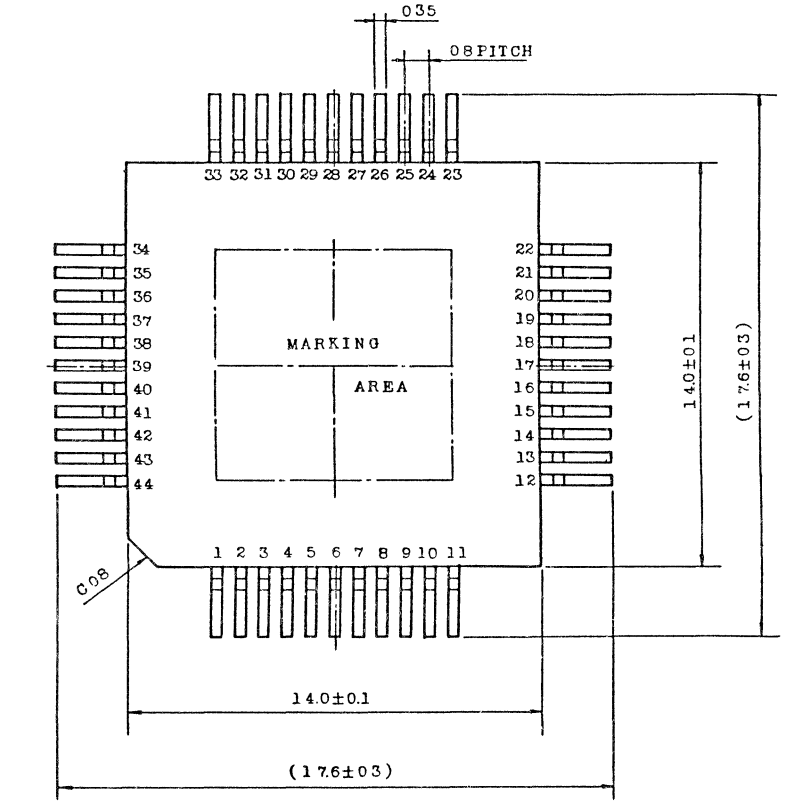


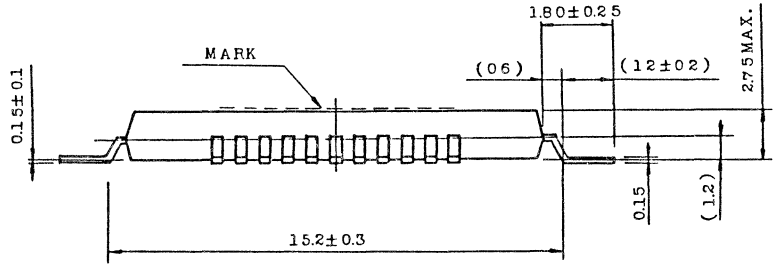
Note) Each lead pitch is 2.54mm, and all the leads are located within +0.25mm from their theoretical position with respect to No.1 and No.28 leads.

EXTERNAL DIMENSION VIEW

44 pins MINI FLATPACKAGE

Unit in mm





TOSHIBA MOS TYPE DEGITAL
INTEGRATED CIRCUIT
Silicon Monolithic N-Channel Silicon Gate MOS

TMP8259AP

PROGRAMMABLE INTERRUPT CONTROLLER

GENERAL DESCRIPTION

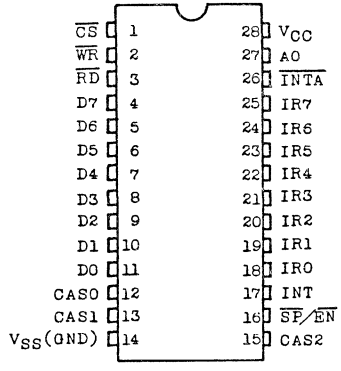
The TMP8259AP is a programmable interrupt controller. It handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry.

FEATURES

- o Eight Level Priority Controller.
- o Expandable to 64 Level.
- o Interrupt Modes, Interrupt Mask, Vectored Address Programmable.
- o Single +5V Power Supply.
- o 8085A, 8086 Microcomputer System Compatible.

PIN CONNECTIONS (TOP VIEW)

TMP8259AP

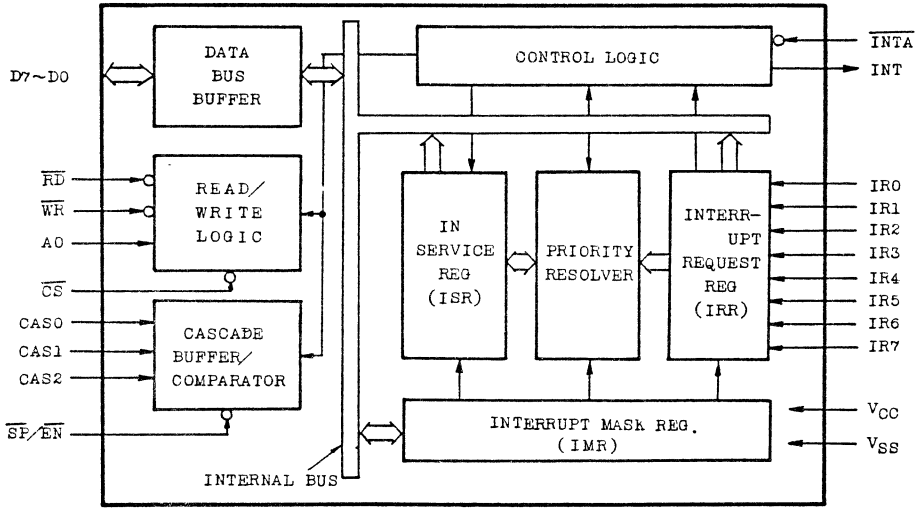


PIN NAMES AND PIN DESCRIPTION

Pin Name	Input/Output	Function
$\overline{CS}$	Input	Chip Select Input. A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the 8259AP. $\overline{INTA}$ functions are independent of $\overline{CS}$.
$\overline{WR}$	Input	Write Control Input. A low on this pin when $\overline{CS}$ is low enables the 8259AP to accept command words from CPU.
$\overline{RD}$	Input	Read Control Input. A low on this pin when $\overline{CS}$ is low enables the 8259AP to release status onto the data bus for the CPU.
D0 to D7	Input/Output	Bidirectional Data Bus. Command status and interrupt-vector information is transferred via this bus.
CAS0 to CAS2	Input/Output	Cascade Lines. The CAS lines form a private 8259AP bus to control a multiple 8259AP structure. These pins are outputs for a master 8259AP and inputs for a slave 8259AP.
$\overline{SP}/\overline{EN}$	Input/Output	Slave Program/Enable Buffer. This is a dual function pin. When in the buffered mode it can be used as an Output to control buffer transceivers ($\overline{EN}$). When not in the buffered mode it is used as an input to designate a master 8259AP ($\overline{SP}$=1) or a slave ($\overline{SP}$=0).
INT	Output	Interrupt Request Output. This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU. It is conected to CPU's interrupt pin.
IR0 to IR7	Input	Interrupt Request Inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on a IR input (Level Triggered Mode).
$\overline{INTA}$	Input	Interrupt Acknowledge Input. This pin is used to enable 8259AP interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.

Pin Name	Input/Output	Function
A0	Input	A0 Address Line. This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the 8259AP to decipher various command words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line.
VCC		+5V Power Supply
VSS		Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
VCC	VCC Supply Voltage (with respect to VSS (GND)	-0.5 to +7V
VIN	Input Voltage	-0.5 to +7V
PD	Power Dissipation	1 W
Tsol	Soldering Tmeperature (Soldering Time 10 sec)	260°C
Tstg	Storage Temperature	-65°C to+150°C
Topr	Operating Tempertature	0°C to 70°C

DC CHARACTERISTICS Ta=0 to +70°C,Vcc=5V±10%,Vss=0V,
Unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage		-0.5	-	0.8	V
VIH	Input High Voltage		2.0	-	VCC+0.5	V
VOL	Output Low Voltage	IOL = 2.2mA	-	-	0.45	V
VOH	Output High Voltage	IOH = -400uA	2.4	-	-	V
VOH (INT)	Output High Voltage (INT)	IOH = -100uA	3.5	-	-	V
		IOH = -400uA	2.4	-	-	V
ILI	Input Leak Current	0V≦VIN≦Vcc	-	-	±10	uA
ILOL	Output Leak Current	0.45V≦VIN≦Vcc	-	-	±10	uA
ILIR	Input Current (IR)	VIN = 0V	-	-	-300	uA
		VIN = VCC	-	-	10	uA
ICC	Operating Supply Current				85	mA

INPUT CAPACITANCE ($Ta=25^{o}C$, $Vcc=Vss=0V$)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_I	INPUT CAPACITANCE	f_C=1 MHz Unmeasured pins, 0V			10	pF
$C_{I/O}$	INPUT/OUTPUT CAPACITANCE				20	pF

AC CHARACTERISTICS

$Ta=0^{o}C$ to $+70^{o}C$, $Vcc=5V\pm10\%$, $Vss=0V$, Unless otherwise noted.

TIMING REQUIREMENTS

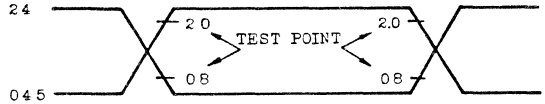
SYMBOL	PAREMETER	MIN.	MAX.	UNIT
TAHRL	A0/$\overline{CS}$ Setup Time ($\overline{RD}$)	0	-	ns
TRHAX	A0/$\overline{CS}$ Hold Time ($\overline{RD}$)	0	-	ns
TRLRH	$\overline{RD}$ Pulse Width	235	-	ns
TAHWL	A0/$\overline{CS}$ Setup Time ($\overline{WR}$)	0	-	ns
TWHAX	A0/$\overline{CS}$ Hold Time ($\overline{WR}$)	0	-	ns
TWLWH	$\overline{WR}$ Pulse Width	290	-	ns
TDVWH	D0 to D7 Setup Time ($\overline{WR}$)	240	-	ns
TWHDX	D0 to D7 Hold Time ($\overline{WR}$)	0	-	ns
TJLJH	Interrupt Request Pulse Width (LOW)	100	-	ns
TCVIAL	Cascade Setup Time (Second or Third $\overline{INTA}$)	55	-	ns
TRHRL	$\overline{RD}$ to Next Command	160	-	ns
TWHWL	$\overline{WR}$ to Next Command	190	-	ns
*TCHCL	End of Command to next Command (Not Same) End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence	500		ns

*Worst case timing for TCHCL in an actual microprocessor system is typically much greater than 500 ns (i.e. 8085A = 1.6us, 8085A-2 = 1us, 8086 = 1us, 8086-2 = 625 ns)

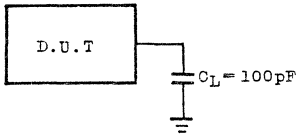
RESPONSE CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
TRLDV	Valid Data Delay ($\overline{RD}/\overline{INTA}$)		-	-	200	ns
TRHDZ	Data Floating ($\overline{RD}/\overline{INTA}$)	D0 to D7	10	-	100	ns
TJHIH	Interrupt Output Delay (IR)	CL=100pF	-	-	350	ns
TIALCV	Valid Cascade Delay ($\overline{INTA}$)	INT	-	-	565	ns
TRLEL	Enable Active ($\overline{RD}/\overline{INTA}$)	CL=100pF	-	-	125	ns
TRHEH	Enable Inactive ($\overline{RD}/\overline{INTA}$)	CAS0 to CAS2	-	-	150	ns
TAHDV	Valid Data Delay (A0/$\overline{CS}$)	CL=100pF	-	-	200	ns
TCVDV	Valid Data Delay (CAS0 to CAS2)		-	-	300	ns

AC Testing I/O Waveform

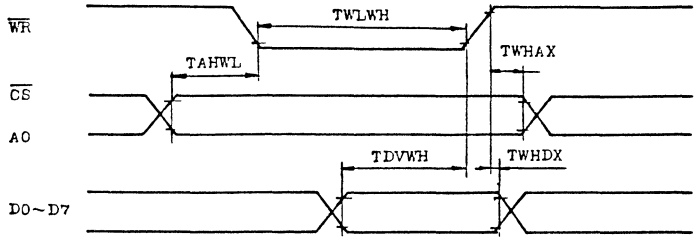


AC Testing Load Circuit

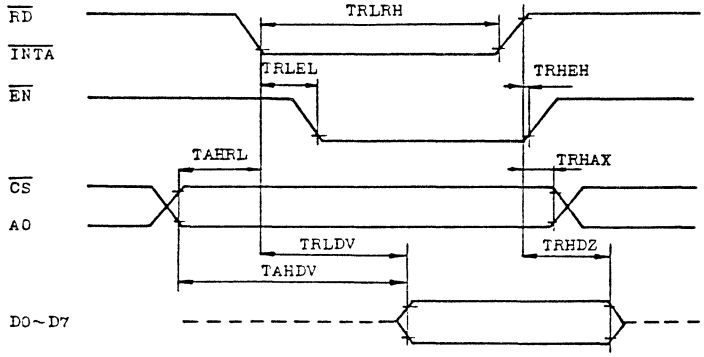


TIMING WAVEFORMS

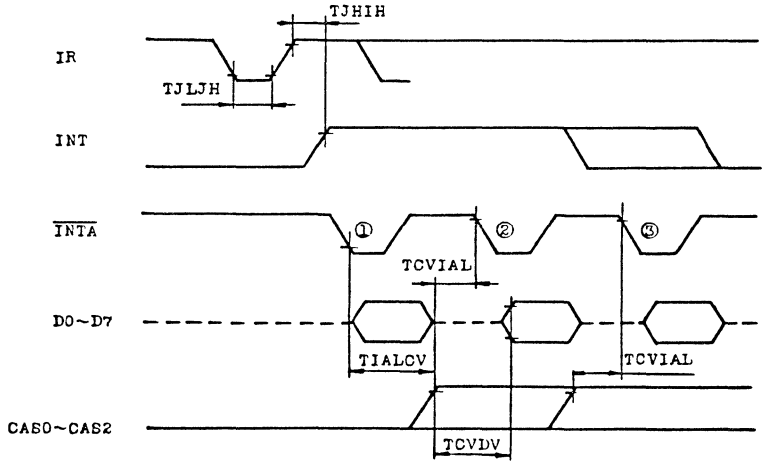
WRITE OPERATION



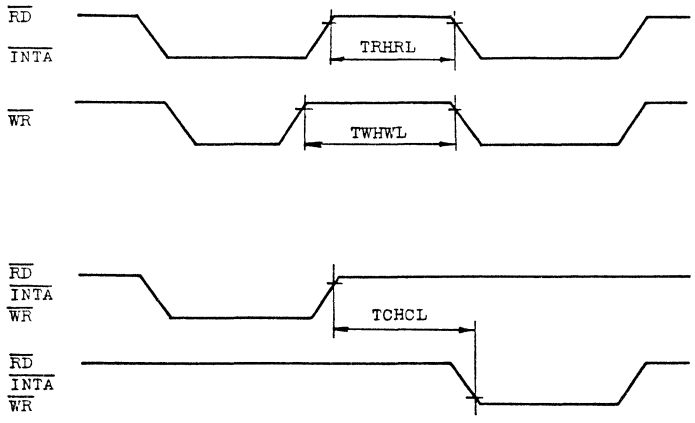
READ AND INTA OPERATION



INTA SEQUENCE



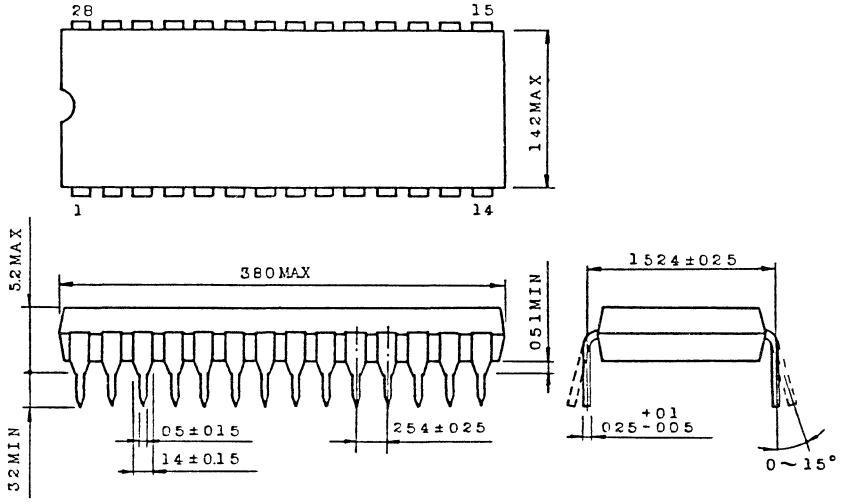
OTHER TIMING



EXTERNAL DIMENSION VIEW

28 pins PRASTIC DIP

Unit in mm



Note) Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoretical position with respect to No.1 and No.28 leads.

TOSHIBA MOS TYPE DIGITAL INTEGRATED CIRCUIT
TMP82C37AP-5/TMP82C37AF-5
SILICON MONOLITHIC CMOS SILICON GATE

MULTIMODE DMA CONTROLLER

GENERAL DESCRIPTION

The TMP82C37AP-5/AF-5 (hereinafter referred to as TMP82C37A) is a multimode direct memory access (DMA) controller. The TMP82C37A improves the system function by directly transferring information between the system memory and external devices. Memory-to-Memory data transfer capability is also provided.

The TMP82C37A is provided with versatile programmable control functions in order to improve data throughput.

The TMP82C37A is used with an 8-bit address register connected externally. The TMP82C37A has four built-in independent channels and it is possible to expand channels through cascade connection.

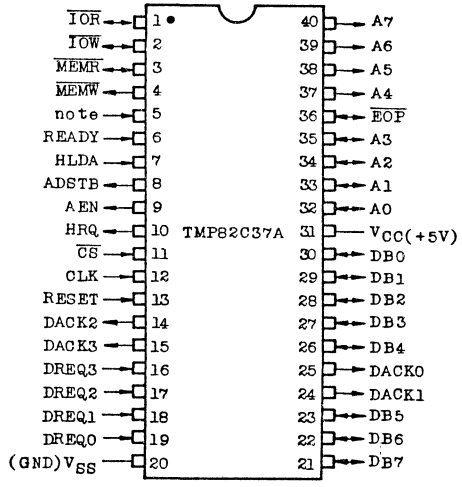
There are three basic data transfer modes which are programmable by the user. Each channel is programmable individually and autoinitialization is possible by End of Process ($\overline{EOP}$) signal.

Each channel has the maximum 64K capability for both address and word count. EOP signal is capable of terminating data transfer between DMA and memories. EOP signal is useful for block search or verify or for terminating erroneous service.

FEATURES

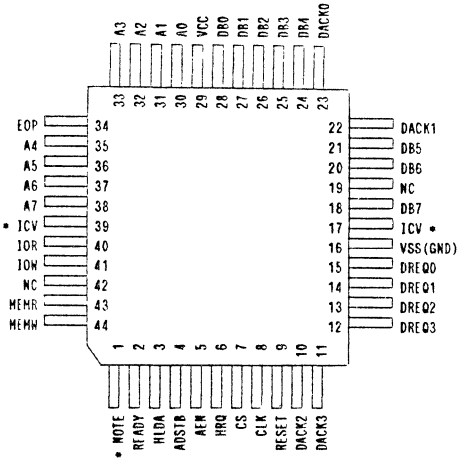
- o Four independent DMA channels available
- o Three transfer modes available; block, demand, and single transfer modes
- o Independent auto initialize function provided to each of all channels
- o Memory-to-Memory transfer
- o Address increment or decrement
- o All DMA request disabled by disabling the master system
- o Individual DMA request enable/disable control
- o Unrestricted channel expansion by cascade connection
- o End of Process ($\overline{EOP}$) input for terminating transfer
- o Software DMA Request
- o Polarity control provided for DREQ signal and DACK signal
- o Option for increasing transfer speed up to 2.5M word/sec
- o Single +5V power supply
- o Low power consumption 5 mA TYP. @5MHz
- o Extend operating temperature $-40^{\circ}C$ to $+85^{\circ}C$

PIN CONNECTIONS (TOP VIEW)
TMP82C37AP-5 (DIP)

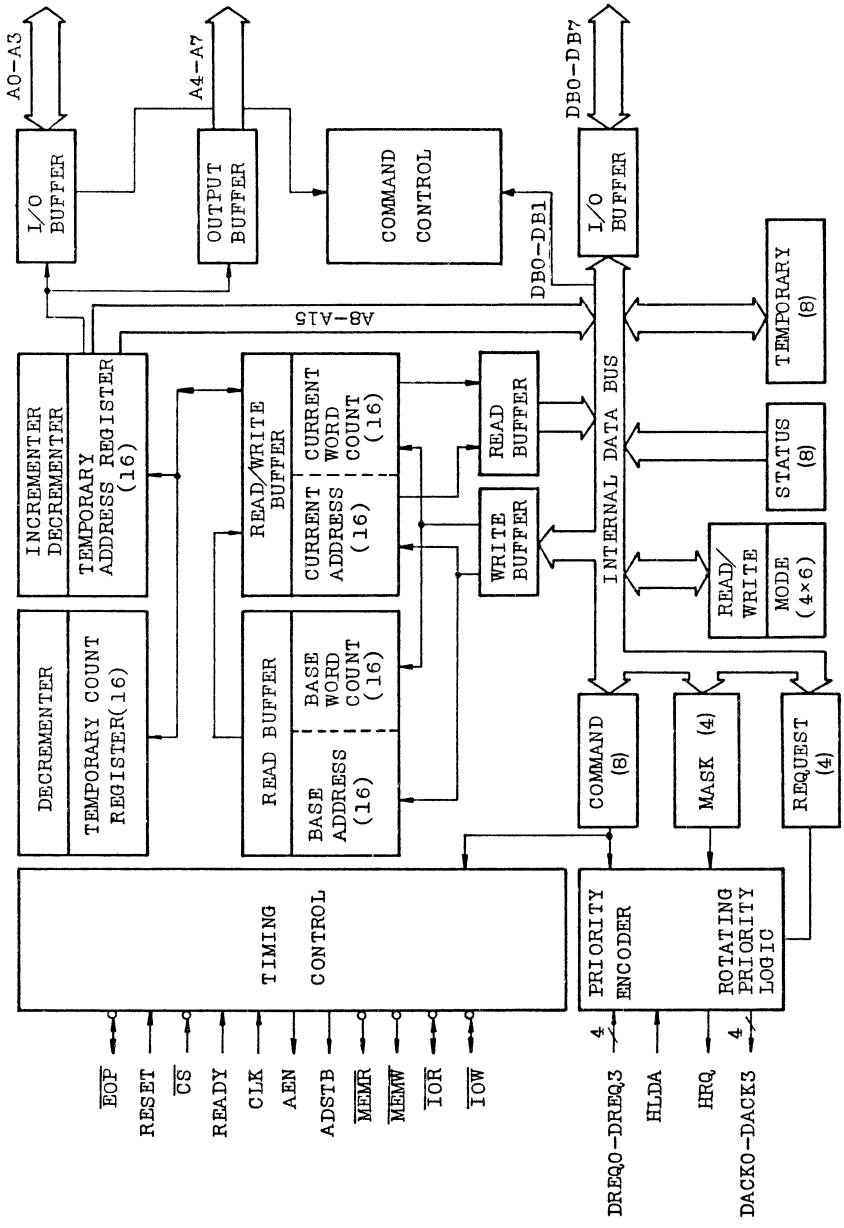


Note) PIN 5 connected +5V or OPEN state

PIN CONNECTIONS (TOP VIEW)
TMP82C37AF-5(MFP)



*) ICV and NOTE (Pin 1, Pin 17 and Pin 39) must be connected with Vcc or must be OPEN
NC: No Connection



Block Diagram of TMP82C37A

PIN NAME & FUNCTION

- VCC
  +5V power supply

- VSS
  Ground

- CLK (Clock, Input)
  This input controls the internal operation and data transfer rate of the TMP82C37A.

- $\overline{CS}$ (Chip Select, Input)
  This input is low active and used to select the TMP82C37A as an I/O device during an I/O read or I/O write by the host CPU. If $\overline{IOR}$ or $\overline{IOW}$ is toggled following each transfer when a host CPU and the TMP82C37A are transferring data mutually, $\overline{CS}$ may be kept at LOW.

- RESET (Reset, Input)
  This input is asynchronous input to clear the command, status, request and temporary registers. In addition, this input is used to clear First/Last flip-flops and set the mask register. Following the reset, the TMP82C37A is placed in the idle cycle.

- READY (Ready, Input)
  This input is used to extend the memory read and write pulses from the TMP82C37A in order to adapt to a slow memories or I/O peripheral devices.

- HLDA (Hold Acknowledge, Input)
  By this signal, the TMP82C37A knows that the system bus control is turned over from CPU.

- $DREQ_0$ - $DREQ_3$ (DMA Request, Input)
  DMA request signals are input from peripheral circuits. If priority is fixed, the highest priority is given to $DREQ_0$ and the lowest priority to $DREQ_3$. Polarity of DREQ is programmable. DREQ becomes high active by RESET.

- DB_0 - DB_7 (Data Bus, Input/Output)
  The Data Bus lines are bidirectional three-state signals connected to the system data bus. During CPU is in I/O read state, output is enabled and contents of the registers (address, status, temporary and word count) are output to CPU. During CPU is in I/O write state, the data bus serves as input and it becomes possible to program the control register of the TMP82C37A.

  During the DMA cycle, the most significant 8 bits of address are output on the data bus and latched by ADSTB signal externally. During the Memory-to-Memory transfer, the data of the source memory location are loaded into the temporary register of the TMP82C37A by the read operation and the contents of the temporary register are output to the destination memory location by the write operation.

- $\overline{IOR}$ (I/O Read, Input/Output)
  I/O read is a bidirectional, low active and 3-state signal. During the idle cycle, this signal serves as an input control signal used by CPU to read the control registers of the TMP82C37A. During the active cycle, this signal serves as an output control signal used by the TMP82C37A to access data from the peripheral circuit during the DMA read and transfer.
- $\overline{IOW}$ (I/O Write, Input/Output)
  I/O write is a bidirectional, low active, 3-state signal. During the idle cycle, this signal serves as an input control signal used by CPU to load the information to the TMP82C37A. During the active cycle, this signal served as an output control signal used by TMP82C37A to load the data to the peripheral. For write to the TMP82C37A by CPU, the leading edge of the write signal ($\overline{IOW}$) is required for every data transfer. It is not possible to write more than two data by toggling $\overline{CS}$ while holding the $\overline{IOW}$ pin at low level.

- $\overline{EOP}$ (End of Process, Input/Output)
  $\overline{EOP}$ (End of Process) is a signal relative to end of DMA service, and is a low active, bidirectional and open drain signal. When the channel word count reaches zero, the TMP82C37A outputs low pulse of $\overline{EOP}$ to peripheral devices as the end signal.
  In addition, it is also possible to pull $\overline{EOP}$ to the low level by peripheral device in order to cause the end of process.
  When $\overline{EOP}$ is received (internally or externally), the channel which is presently active terminates the service, sets that TC bit of the status register and resets that request bit.
  If that channel is programmed for auto initialization, that current register is updated from the base register. In all other cases, mask bit is set and the content of that register remains unchanged.
  During the Memory-to-Memory transfer, $\overline{EOP}$ is output when TC of channel 1 is produced. $\overline{EOP}$ is always used for channels with active DACK and external $\overline{EOP}$ has no connection when $DACK_0$ - $DACK_3$ are all inactive.
  $\overline{EOP}$ is an open drain signal and therefore, requires an external pull-up resistor.

- A_0 - A_3 (Address, Input/Output)
  The four least significant address lines are the bidirectional 3-state signals. In the idle cycle, these lines serve as the input signals and used by CPU for write/read of the control register. In the active cycle, they serve as the output signals and become low order 4 bits of output address.

- A_4 - A_7 (Address, Output)
  The four most significant address lines are 3-state output signals. These lines are enabled for the period of DMA service only.

- HRQ (Hold Request, Output)
  This is the hold request signal to CPU, and is used to request the system bus control. HRQ is output by the TMP82C37A according to a software request or unmasked DREQ.

- $DACK_0$ - $DACK_3$ (DMA Acknowledge, Output)
  The DMA acknowledge lines indicate that channels are active. On ordinary systems, these are used for selecting peripheral devices. Only one DACK becomes active but it does not become active unless DMA is controlling the system bus. Porarily of these lines are programmable. When reset, they become low active.

- AEN (Address Enable, Output)
  Address Enable is a high active signal and used to enable output of the external latch which holds high order byte of address and to disable the system bus during the DMA cycle.
  During the DMA transfer, HLDA and AEN are used to disable all I/O except programmed I/O. The TMP82C37A disables $\overline{CS}$ input for DMA transfer to prevent itself from being selected automatically.

- ADSTB (Address Strobe, Output)
  This signal is a strobe output to an external latch circuit and is used to latch high order 8-bit address from DB_0 - DB_7.

- $\overline{MEMR}$ (Memory Read, Output)
  This is a low active 3-state output used for transferring data from a memory to a peripheral device or for data accessing from a selected memory during the Memory-to-Memory transfer.

- $\overline{MEMW}$ (Memory Write, Output)
  This is a low active 3-state output used for transferring data from a peripheral device to a memory or for writing data into a selected memory during the Memory-to-Memory transfer.

OPERATIONAL DESCRIPTION

- DMA Operation
  The TMP82C37A has two operations; idle cycle and active cycle. Each of these cycles consists of several states.
  On the TMP82C37A, it is possible to consider 7 states each of which consists of one clock cycle. State I (SI) is an idle state. This is such a state as there is no valid DMA request pending. SI is a program condition state which is programmable by CPU.
  State 0 (S0) is the first DMA service state. This is a state that the TMP82C37A made a hold request to CPU but not yet received the acknowledge signal from CPU. When the acknowledge signal is recieved from CPU, the transfer is started.
  S1, S2, S3 and S4 are the DMA service state. If more time is required by the transfer, it is possible to insert the wait state (SW) before S4 by READY input to the TMP82C37A.
  In the Memory-to-Memory transfer, in order to assure complete transfer, read from the memory and write to the memory are required. 8 states are necessary for one transfer. The first four states (S11, S12, S13 and S14) are read from the memory and the latter four state (S21, S22, S23 and S24) are write to the memory.
  The temporary data register is used as an intermediate storage area of memory bytes.

o Idle cycle

When DMA service is not requested by channels, the TMP82C37A enters into the idle cycle and is placed in SI state. In order to check if the channels request DMA service, the TMP82C37A samples DREQ for every clock.

The TMP82C37A also samples $\overline{CS}$ to check if CPU is requesting read or write of internal registers. When $\overline{CS}$ is low and HLDA is also low, the TMP82C37A is placed in the program condition.

At this time, CPU is able to change or check the content of any internal register through read or write from that register.

Address lines A_0 - A_3 are input signals and used for selecting a register being read or written. $\overline{IOR}$ and $\overline{IOW}$ are used for selecting read or write and decide read/write timing.

The internal flip-flop is used for generating address extension bits according to number and size of internal registers. (First/Last Flip-flop) This bit is used for deciding high or low order byte of 16-bit address and word count register.

The flip-flop is reset by the master clear or reset. In addition, this flip-flop also can be reset by an independent software command. On a special software command, the execution in the TMP82C37A program condition is possible. These commands are decoded as in the address setting when both $\overline{CS}$ and $\overline{IOW}$ are active.

The data bus is not used for this command. This command is available in two types; clear First/Last flip-flop and master clear.

o Active cycle

When the TMP82C37A is in the idle cycle and the channels are requesting DMA service, the TMP82C37A outputs HRQ to CPU and goes into the active cycle. In this cycle, the DMA service for any one of 4 modes is executed.

Single Transfer Mode:

In this mode, the TMP82C37A performs a single byte transfer during each HRQ/HLDA handshake. When DREQ becomes active, HRQ becomes active. After CPU responds by driving HLDA active, a single byte transfer will take place. After the transfer HRQ becomes inactive, its word count is decreased, and address is increased or decireased. When word count becomes zero, a terminal signal is generated and if the channels are programmed, the auto initialization is made.

To execute the single byte transfer, it is necessary to hold DREQ until DACK corresponding each DREQ becomes active. If DREQ is continuously active, HRQ becomes inactive following each transfer and then, becomes active again, and the new single byte is executed following the leading edge of HLDA.

On the 8085 system, one machine cycle can be executed during the DMA transfer.

Block Transfer Mode:

In this mode the TMP82C37A continues the transfer until terminal count (TC) is generated or an external End of Process signal ($\overline{EOP}$) is encountered. Here, TC is produced when the word count becomes zero.

What is required for DREQ is to hold it in active state until DACK becomes active. Auto initialization (if so programmed) is taken place at the end of DMA service.

Demand Transfer Mode:

In this mode the TMP82C37A continues the transfer when TC is produced or $\overline{EOP}$ is input or until DREQ becomes inactive. Thus, it is possible for a device, which is requesting the DMA service, to suspend the transfer by making DREQ inactive. The service is resumed when DREQ is made active again. It is possible to read an intermediate value of address and word count from the current address and current word count register of the TMP82C37A while the system bus is returned to CPU during execution of the DMA service.

The auto initialization is taken place following TC or $\overline{EOP}$ at the end of DMA service. In order to perform a new DMA service following the auto initialization, the active edge of DREQ is necessary.

Cascade Mode:

This mode is used when the TMP82C37A is cascade connected for a simple system expansion. HRQ and HLDA of the additional TMP82C37A are connected to DREQ and DACK of the first TMP82C37A. DMA request to the TMP82C37A which is added for the purpose of system expansion is authorized by the priority circuit of the first TMP82C37A.

If the priority is already decided, the additional device must wait till the acknowledge request. The cascade channel of the first TMP82C37A is used only for deciding priority of the additional TMP82C37A and therefore, the channel itself does not output address nor control signal. This is to prevent the added device from colliding with output of the cascade channel. On the TMP82C37A, DACK respond to DREQ. However all other outputs except HRQ are disabled.

The state of cascade connection is shown in Fig. 2. In Fig. 2, two levels of DMA are formed. To further expand the TMP82C37A, it is possible to add it to the second level using the remaining channel of the first TMP82C37A. To further add another TMP82C37A, the third level can be formed by cascade connecting it to the second level.

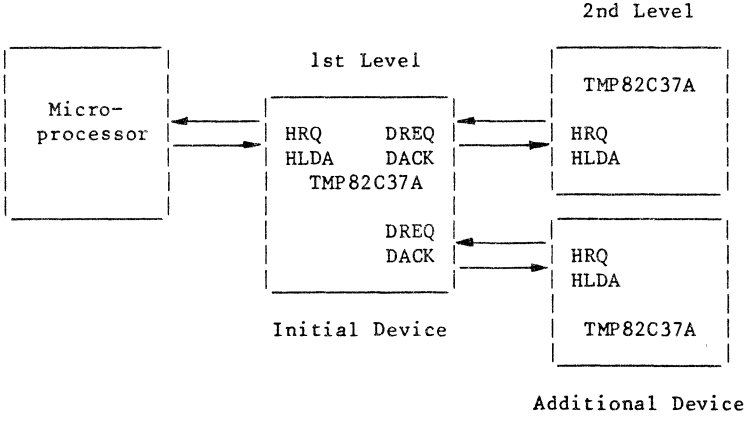


Fig. 2 Example of Cascade Connection of TMP82C37A

o Transfer format

3 different transfer format are available for 3 active transfer modes. They are read, write and verify. In the write transfer, data is transferred from I/O dvice to memory by MEMW and IOR. In the read transfer, data is transferred from memory to I/O device by MEMR and IOW.

The verify transfer is a pseudo transfer. The TMP82C37A perform such operations as address generation for read or write transfer, answer to EOP, etc. However, memory or I/O control line does not become active.

Memory-to-Memory Transfer:

The TMP82C37A has the ability of block movement and is capable of transferring data block from one memory address location to another location. When Bit 0 of the command register is programmed at Logic 1, Channel 0 and 1 operate as the Memory-to-Memory transfer channels. Channel 0 serves as a source address and Channel 1 as a destination address, and the word count of Channel 1 is used. The Memory-to-Memory transfer is executed when software DMA request is set for Channel 0.

The Memory-to-Memory transfer must use the block transfer mode.

When Channel 0 is programmed as a fixed source address, it is possible to write single source words into a memory block.

When the TMP82C37A is programmed for the Memory-to-Memory transfer, Channel 0 and Channel 1 must be masked. The same value as that is set for Channel 1 must be set for the word count of Channel 0. During the Memory-to-Memory transfer, DACK does not become active.

During the Memory-to-Memory transfer, the TMP82C37A respond to external EOP signal. In the block search, the data comparator uses this (EOP) input to terminate the DMA serive when match is found. The Memory-to-Memory transfer is shown in Timing Diagram 4. (P.23)

Auto Initialization:

When Bit 4 of the mode register is set to 1, the channels are set up for the auto initialization. During the auto initialization, data are loaded into the current address and current word count registers from the base address and base word count registers, respectively, following EOP. The base registers are loaded by CPU simultaneously with the current registers and remain unchanged during the DMA service.

When the channels are under the auto initialization, mask bit is not set by EOP.

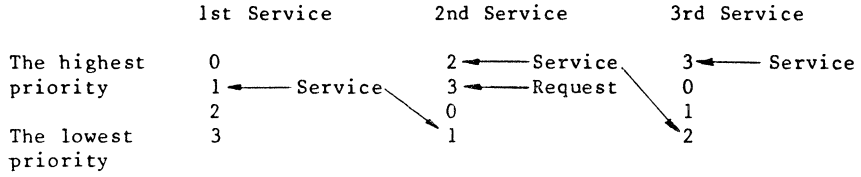
Following the auto initialization, that channel is prepared to execute the service without interposition of CPU.

Priority:

The TMP82C37A has two types of priority which can be selected by software. The first type is the fixed priority. Channel priority is fixed by channel number. The lowest priority is channel 3, followed by 2, 1, and the highest priority is channel 0.

The second type is the rotating priority. In this type, an accepted channels is then given with the lowest priority (See the following next page diagram.).

On the rotating priority in the single chip DMA system, highest priority of any one channel comes after no more than three higher priority services have occurred. This rotating priority prevent one channel to occupy the system all the time.



The priority judging circuit selects a channel with the highest priority requesting the DMA service for every active edge of HLDA

Once the channel starts the service, that operation will not be suspended even when the service is demanded by another channel with higher priority. A channel with higher priority can get the control right only after a channel with lower priority relinquished HRQ. Whenever the control is transferred from a channel to another channel, CPU gets the system bus control right. This assures the leading edge of HLDA which is used for selecting a channel with the highest priority.

Compressed Transfer Timing:

In order to accomplish greater throughput allowed by system characteristics, the TMP82C37A is capable of compressing the transfer time to 2 clock cycles. As can be seen from Timing Diagram 3 (P.22), State S3 is used to extend readout pulse access time. When State S3 is removed, readout pulse width becomes equal to write pulse width. Then, the transfer will consist of State S2 for changing address and State S4 for executing read/write. State S1 is produced when A_8 to A_{15} are updated (refer to Address Generation). Compressed transfer timing is shown in Timing Diagram 5 (P.23).

Address Generation:

To reduce number of pins, the TMP82C37A has high order 8 bits multiplexed with the data bus. State S1 is used to output high order address bits to the external latch. The trailing edge of ADSTB is used to load address bits from the data line on the external latch circuit. AEN is used to enable latch outputs from 3 states. Low order address bits are ditectly output by the TMP82C37A.

A_0 to A_7 are connected to address bus. Timing Diagram 3 (P.22) show the relationship among CLK, AEN, ADSTB, DB_0 to DB_7 and A_0 to A_7.

Addresses produced during the block and demand transfers are sequential. For many transfer the same address data will be held in the external address latch. This address data changes only when carry or borrow from A_7 to A_8 is produced in the normal sequence. To save time and speed, on the TMP82C37A, S1 state is executed only for update of A_8 to A_{15} requiring the latch.

Description of Registers

Register Name	Size	Number
Base address register	16-bit	4
Base word count register	16-bit	4
Current address register	16-bit	4
Current word count register	16-bit	4
Temporary address register	16-bit	1
Temporary word count register	16-bit	1
Status register	8-bit	1
Command register	8-bit	1
Temporary register	8-bit	1
Mode register	6-bit	4
Mask register	4-bit	1
Request register	4-bit	1

Fig. 3 Internal Registers

Current Address Register:

Each channel has a 16-bit current address register. This register holds addresses that are used during the DMA transfer. After each transfer, this register is automatically incremented or decremented, and intermediate address values are stored in the current address register during the transfer. Write or read of this register is made by CPU. An original value is initialized again by the auto initialization.

The auto initialization is taken place only after $\overline{EOP}$.

Current Word Count Register:

Each channel has a 16-bit current word count register. For this register, number of words that is one less than that to be tranferred must be programmed. The word counter is decremented after each transfer. Intermediate values of word count are stored in this register during the transfer. When the register value goes from zero to FFFFH, TC is produced.

When this register is in the program condition, load or read is made by CPU. Following the end of DMA service, this register is initialized to original values again by the auto initialization.

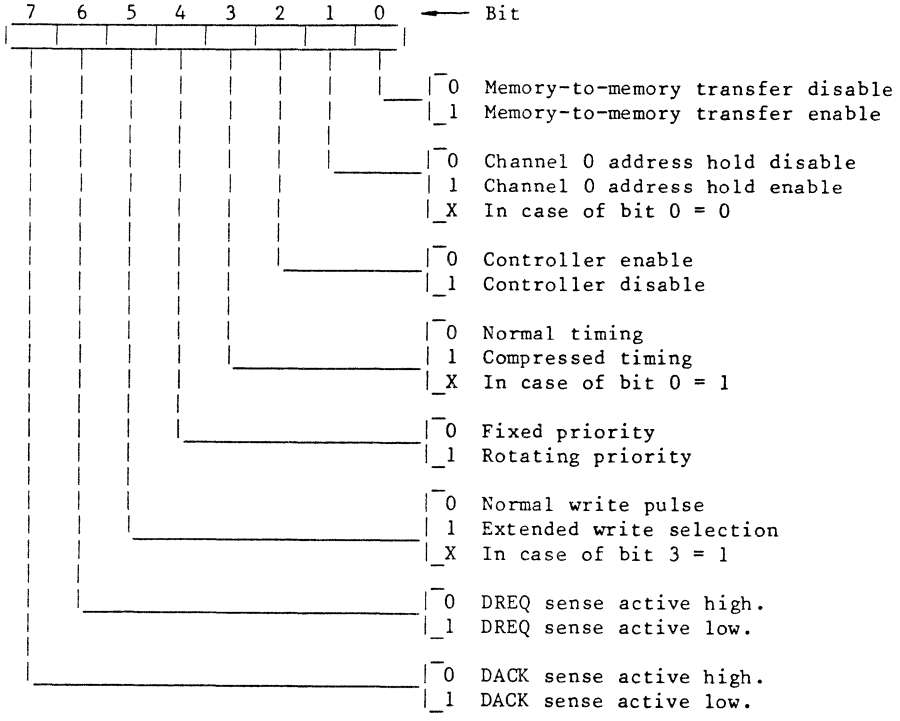
The auto initialization is taken place only when $\overline{EOP}$ is produced. Be careful that the content of the word count register becomes FFFFH following internally produced $\overline{EOP}$.

Base Address Register, Base Word Count Register:

Each channel has a pair of registers; the base address register and base word count register. These 16-bit registers store original values of related current registers. These registers are used to store original values of current registers at time of the auto initialization. Write to the base register is made at the same time of write into equivalent current registers during the programming by CPU. Therefore, write into the current registers which store intermediate values are made over these intermediate values. The base register cannot be read out by CPU.

Command Register:

This 8-bit register controls the operation of TMP82C37A. This command register is programmed (clear or reset) by CPU when it is in the program condition. The charts presented below show the functions of command bits. For address codes, refer to Fig. 4 (P.15).

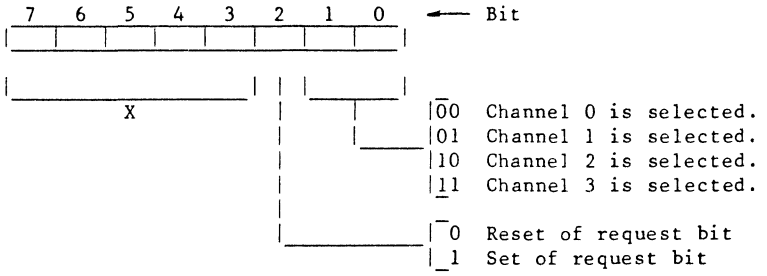


Request Register:

The TMP82C37A is capable of responding to DMA service request by software similar to DREQ. Each channel has a single bit request register which cannot be masked. Further, priority is given by the priority encode circuit.

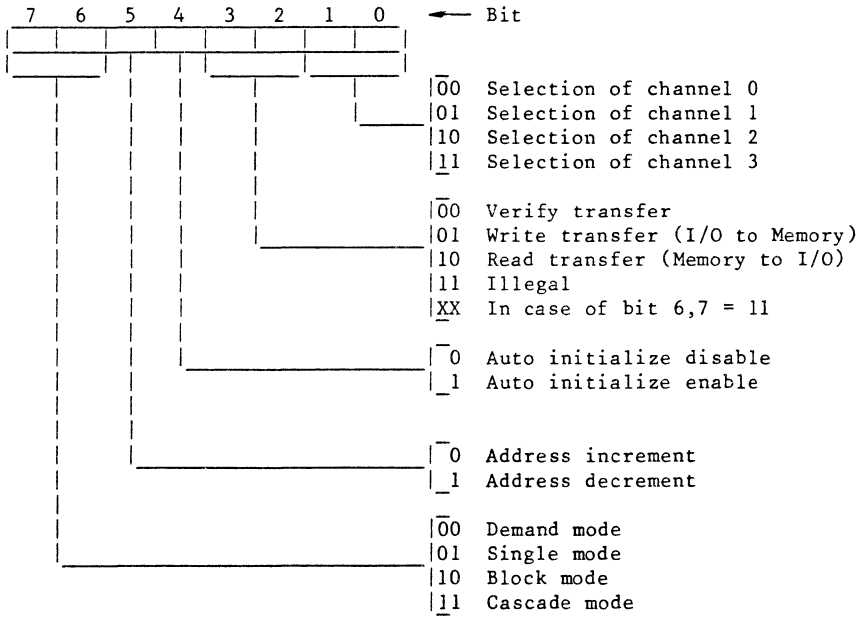
Bit of each register is set or cleared by software and further, cleared by generation of TC or external $\overline{EOP}$. All registers are cleared by reset. In order to set or reset bit, a proper form of data word is loaded by software.

Address codes are shown in Fig. 4 (P.15). DMA service request by software is accepted only when the channels are in the block mode. In the Memory-to-Memory transfer, DMA service request by the software command to Channel 0 only becomes valid.



Mode Register:

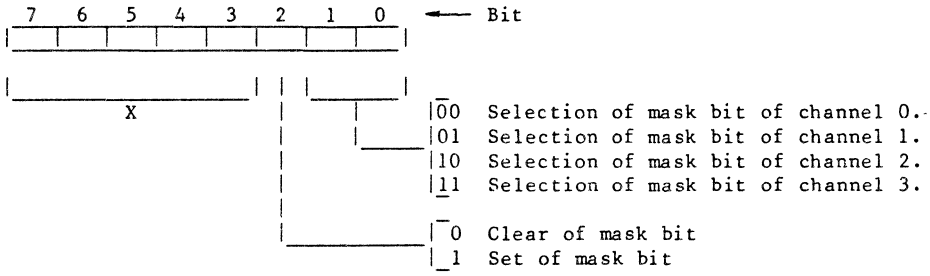
All channels have a 6-bit mode register, respectively. This mode register is written by CPU when it is in the program condition, and Bit 0 and 1 decide which channel's mode register is to be written.



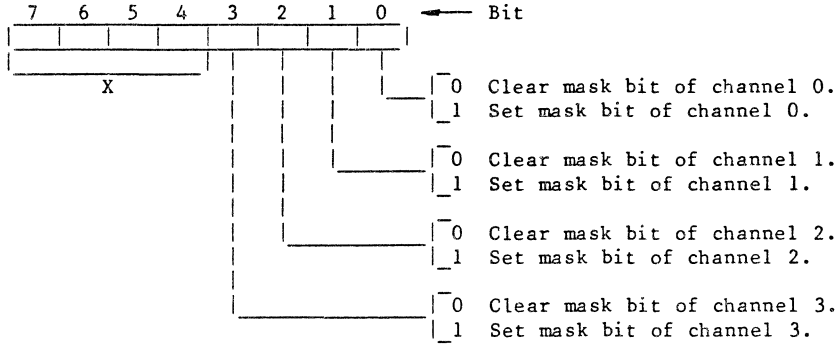
Mask Register:

For each channel, mask bit are allocated to the mask register to disable DREQ input. If the auto initialization has not been programmed for the channels, the channel corresponding to a mask bit is set when $\overline{EOP}$ is produced. Each bit of the 4-bit mask register is also set or cleared by the software command. All bits are also set by reset. This will disable all DMA requests until the clear mask register command is enabled.

Command addressing is shown in Fig. 4 (P.16).



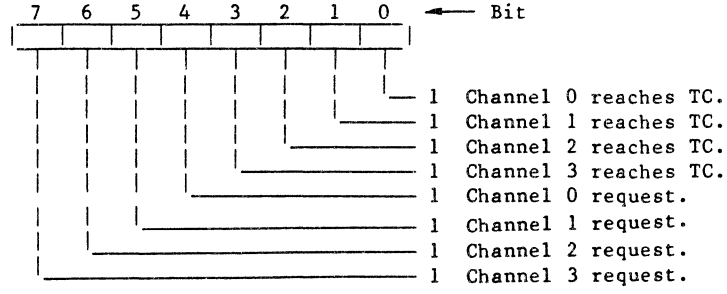
All four bits of the mask register can be written also by a single command.



Status Register

This register is read out by CPU through the TMP82C37A. Status information of the TMP82C37A at time of readout is included. Information as to which channel reaches the terminal count (TC) and which channel is pending the DMA request are included in this information. Bits 0 to 3 are set every time when a channel reaches TC including the auto initialization.

These bits are cleared by reset or when each status is read out. bits 4 to 7 are always set when corresponding channels are requesting the DMA service



Temporary Register:

This register is used for holding data during the Memory-to-Memory transfer. A last word transferred following the end of tranfer is read out by CPU that is in the program condition. Unless cleared by reset, this register contains the last word transferred during the preceding Memory-to-Memory transfer.

Software Commands:

These commands are special software commands which are executed in the program condition and do not depend upon the specified bit pattern on the data bus. These commands are available in following two commands:

Clear First/Last flip-flop

This command is executed prior to write or read of address information or word count information of the TMP82C37A. Furthermore, this command is used when low order or high order 8 bits of register are accessed.

Master Clear

This software command has the same effect as the hardware reset. The command, status, request, temporary, and internal First/Last flip-flop registers are all cleared by this command, and the mask register is set.

The TMP82C37A enters into the idle cycle.

Clear Mask Register

This command clears all mask bits of four channels, enabling acceptance of the DMA service requests.

Address codes of the software commands are shown in Fig. 4.

Signal						Operation
A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$	
1	0	0	0	0	1	Read of status register
1	0	0	0	1	0	Write to command register
1	0	0	1	0	1	-
1	0	0	1	1	0	Write to request register
1	0	1	0	0	1	-
1	0	1	0	1	0	Bit set, reset of mask register
1	0	1	1	1	0	-
1	0	1	1	1	0	Write to mode register
1	1	0	0	0	1	-
1	1	0	0	1	0	Clear First/Last flip-flop
1	1	0	1	0	1	Read of temporary register
1	1	0	1	1	0	Master clear
1	1	1	0	0	1	-
1	1	1	0	1	0	Clear mask register
1	1	1	1	0	1	-
1	1	1	1	1	0	All bit write of mask register

Note) The oblique lined codes denote illegal codes.

Fig. 4 Register and Function Addressing

(*): Internal F/L,F/F

Channel	Register	Operation	Signal							(*)	Data Bus
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		DB0-DB7
0	Base & Current Address	Write	0	1	0	0	0	0	0	0	A0 - A 7
			0	1	0	0	0	0	0	1	A8 - A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0 - A 7
			0	0	1	0	0	0	0	1	A8 - A15
	Base & Current Address	Write	0	1	0	0	0	0	1	0	W0 - W 7
			0	1	0	0	0	0	1	1	W8 - W15
	Current Address	Read	0	0	1	0	0	0	1	0	W0 - W 7
			0	0	1	0	0	0	1	1	W8 - W15
1	Base & Current Address	Write	0	1	0	0	0	1	0	0	A0 - A 7
			0	1	0	0	0	1	0	1	A8 - A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0 - A 7
			0	0	1	0	0	1	0	1	A8 - A15
	Base & Current Address	Write	0	1	0	0	0	1	1	0	W0 - W 7
			0	1	0	0	0	1	1	1	W8 - W15
	Current Address	Read	0	0	1	0	0	1	1	0	W0 - W 7
			0	0	1	0	0	1	1	1	W8 - W15
2	Base & Current Address	Write	0	1	0	0	1	0	0	0	A0 - A 7
			0	1	0	0	1	0	0	1	A8 - A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0 - A 7
			0	0	1	0	1	0	0	1	A8 - A15
	Base & Current Address	Write	0	1	0	0	1	0	1	0	W0 - W 7
			0	1	0	0	1	0	1	1	W8 - W15
	Current Address	Read	0	0	1	0	1	0	1	0	W0 - W 7
			0	0	1	0	1	0	1	1	W8 - W15
3	Base & Current Address	Write	0	1	0	0	1	1	0	0	A0 - A 7
			0	1	0	0	1	1	0	1	A8 - A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0 - A 7
			0	0	1	0	1	1	0	1	A8 - A15
	Base & Current Address	Write	0	1	0	0	1	1	1	0	W0 - W 7
			0	1	0	0	1	1	1	1	W8 - W15
	Current Address	Read	0	0	1	0	1	1	1	0	W0 - W 7
			0	0	1	0	1	1	1	1	W8 - W15

Fig. 5 Word Count, Address Registers

Programming

If HLDA of CPU is inactive it is possible to program the TMP82C37A by CPU even when HRQ is active.

However, it is necessary for CPU to take care that programming of the TMP82C37A and answer of HLDA are taken place simultaneously.

It requires care when the DMA service is requested to an unmasked channel during the programming of the TMP82C37A.

It is considered that an embarrassing trouble may be caused in this case.

For instance, if CPU is going to rewrite the address register of channel 2 and in addition, the TMP82C37A is enabled and channel 2 is not masked when channel 2 received a DMA request. The DMA service will be started after one byte of the address register is written. Such a problem as exampled above can be taken place.

To avoid such problems as this, it is better to disable the controller or mask unmasked channels before reprogramming any register.

It is better to enable the controller or clear the masking when the programming is completed.

Example of Program Set (CH2)

```
DI                    :  Interrupt disable
OUT    MCLR           :  Master clear
MVI    A, xxxxxxxxB
OUT    CMND           :  Command register set-up
MVI    A, xxxxxx10B
OUT    MODE           :  Mode register set-up
MVI    A, 37H
OUT    ADR2           :  CH2 Address Reg. (low order)
MVI    A, 82H
OUT    ADR2           :  CH2 Address Reg. (high order)
MVI    A, 17H
OUT    WCNT2          :  CH2 Word count register (low order)
MVI    A, 95H
OUT    WCNT2          :  CH2 Word count register (high order)
MVI    A, 00000010B
OUT    MSKB2          :  CH2 Mask clear (single bit)
EI                    :  Interrupt enable
```

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEMS	TEST CONDITION	RATING	UNIT
VCC	Supply Voltage	With Respect To GND.	-0.5 to 7.0	V
VIN	Input Voltage		-0.5 to VCC +0.5	V
VOUT	Output Voltage		-0.5 to VCC +0.5	V
PD	Power Dissipation		250	mW
Tsol	Solder Temperature		260 (10 sec)	°C
Tstg	Strage Temperature		-65 to +150	°C
Topr	Operating Temperature		-40 to +85	°C

DC CHARACTERISTICS

[Ta = -40°C to 85°C, VCC = 5V ± 10%, VSS (GND) = 0V]

SYMBOL	ITEMS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage		-0.5		0.8	V
VIH	Input High Voltage		2.2		VCC+0.5	V
VOL	Output Low Voltage	IOL = 3.2mA			0.45	V
VOH1	Output High Voltage	IOH1 = -400uA	2.4			V
VOH2	Output High Voltage	IOH2 = -100uA	VCC-0.8			V
IIL	Input Leakage Current	0V ≦ VIN ≦ VCC			±10	uA
IOFL	Output Leakage Current	0.45V≦VOUT≦VCC			±10	uA
ICC1	Operating Supply Current	CLK = 5 MHz VIH=VCC-0.2V VIL = 0.2V		5	10	mA
ICC2	Stand-by Supply Current	CLK = DC VIH=VCC-0.2V VIL = 0.2V			10	uA

AC CHARACTERISTICS

Active Cycle (Notes: 2 and 9) [Ta=-40°C to 85°C, VCC=5V±10%, VSS(GND)=0V.]

SYMBOL	ITEMS.	MIN.	MAX.	UNIT
TAEL	AEN HIGH from CLK LOW (S1) Delay time		200	ns
TAET	AEN LOW from CLK HIGH (SI) Delay time		130	ns
TAFAB	ADR Active to Float Delay from CLK HIGH		90	ns
TAFC	READ or WRITE Float Delay from CLK HIGH		120	ns
TAFDB	DB Active to Float Delay from CLK HIGH		170	ns
TAHR	ADR from READ HIGH Hold Time	TCY-100		ns
TAHS	DB from ADSTB LOW Hold Time	30		ns
TAHW	ADR from WRITE HIGH Hold time	TCY-50		ns
TAK	DACK Valid from CLK Low Delay Time		170	ns
	EOP HIGH from CLK HIGH Delay Time		170	ns
	EOP LOW to CLK HIGH Delay Time		170	ns
TASM	ADR Stable from CLK HIGH		170	ns
TASS	DB to ADSTB LOW Setup Time	100		ns
*TCH	Clock HIGH Level Time	68		ns
*TCL	Clock LOW Level Time	100		ns
TCY	Clock Cycle Time	200		ns
TDCL	(NOTE 3) CLK HIGH to READ or WRITE LOW Delay Time		190	ns
TDCTR	(NOTE 3) READ HIGH from CLK HIGH (S4) Delay Time		190	ns
TDCTW	(NOTE 3) WRITE HIGH from CLK HIGH (S4) Delay Time		130	ns
TDQ1	(NOTE 4)		120	ns
*TDQ2	HRQ Valid from CLK HIGH Delay Time		140	ns
TEPS	EOP LOW from CLK LOW Setup Time	40		ns
TEPW	EOP pulse width	220		ns
TFAAB	ADR Float to Active Delay from CLK HIGH		170	ns
TFAC	READ or WRITE Active from CLK HIGH		150	ns
TFADB	DB Float to Active Delay from CLK HIGH		200	ns
THS	HLDA Valid to CLK HIGH Setup Time	75		ns
TIDH	Input Data from MEMR HIGH Hold Time	0		ns
TIDS	Input Data to MEMR HIGH Setup Time	170		ns
TODH	Output Data from MEMW HIGH Hold Time	10		ns
TODV	Output Data Valid to MEMW HIGH	125		ns
*TQS	DREQ to CLK LOW (SI, S4) Setup Time	30		ns
TRH	CLK to READY LOW Hold Time	20		ns
TRS	READY to CLK LOW Setup Time	60		ns
TSTL	ADSTB HIGH from CLK HIGH Delay Time		130	ns
TSTT	ADSTB LOW from CLK HIGH Delay Time		90	ns

NOTE 1 : TCL and TDQ2.
The following AC specification can be also guaranteed under the conditions : Ta =-40°C to 50°C
Vcc=5V+5%
Vss= 0V
1 TCL = 80ns (MIN)
2 TDQ2=120ns (MAX)

NOTE 2 : Value with * Mark is different from AC specification of N-MOS part.

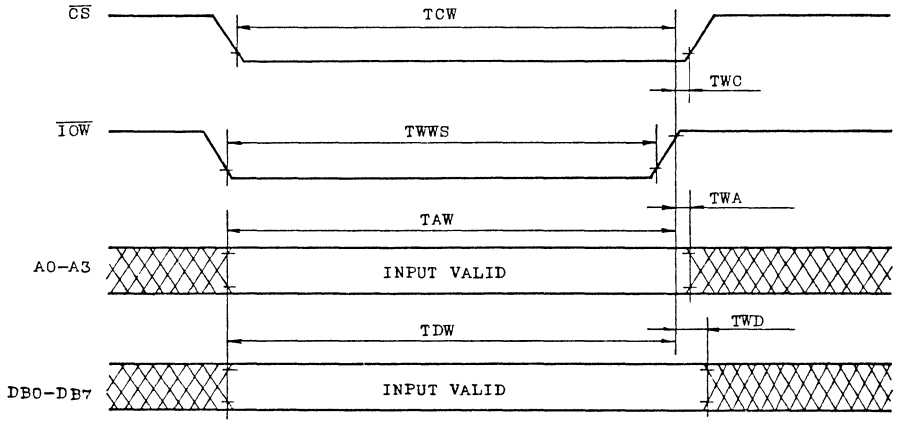
Program Condition (Idle Cycle) (Notes: 2, 8 and 9)
[Ta=-40°C to 85°C, VCC=5V±10%, VSS(GND)=0V]

SYMBOL	ITEMS.	MIN.	MAX.	UNIT
TAR	ADR Valid or $\overline{CS}$ LOW to $\overline{READ}$ LOW	50		ns
TAW	ADR Valid to $\overline{WRITE}$ HIGH Setup Time	130		ns
TCW	$\overline{CS}$ LOW to $\overline{WRITE}$ HIGH Setup Time	130		ns
TDW	Data Valid to $\overline{WRITE}$ HIGH Setup Time	130		ns
TRA	ADR or $\overline{CS}$ Hold from $\overline{READ}$ HIGH	0		ns
TRDE	Data Access from $\overline{READ}$ LOW (Note 7)		140	ns
TRDF	Data Bus Float Delay from $\overline{READ}$ HIGH	0	70	ns
TRSTD	Power Supply HIGH to RESET LOW Setup Time	500		ns
TRSTS	RESET to First $\overline{IOWR}$	2TCY		ns
TRSTW	RESET Pulse Width	300		ns
TRW	$\overline{READ}$ Pulse Width	200		ns
TWA	ADR from $\overline{WRITE}$ HIGH Hold Time	20		ns
TWC	$\overline{CS}$ HIGH from $\overline{WRITE}$ HIGH Hold Time	20		ns
TWD	Data from $\overline{WRITE}$ HIGH Hold Time	30		ns
TWWS	$\overline{WRITE}$ pulse Width	160		ns

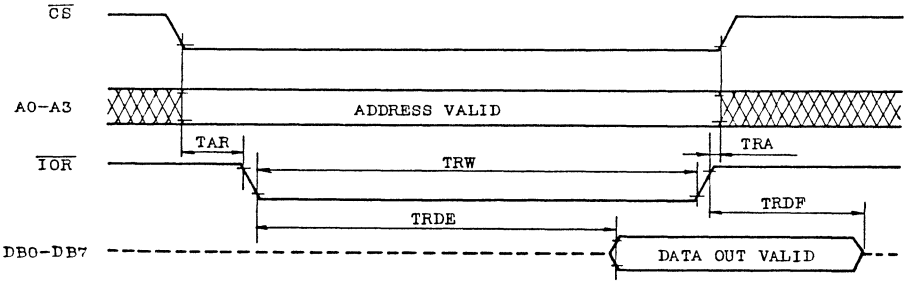
Capacity (Ta=25°C, VCC=GND=0V)

SYMNOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CI	Input Capacitance	fc = 1.0 MHz, Input = 0V			8	pF
CO	Output Capacitance				15	
CIO	I/O Capacitance				20	

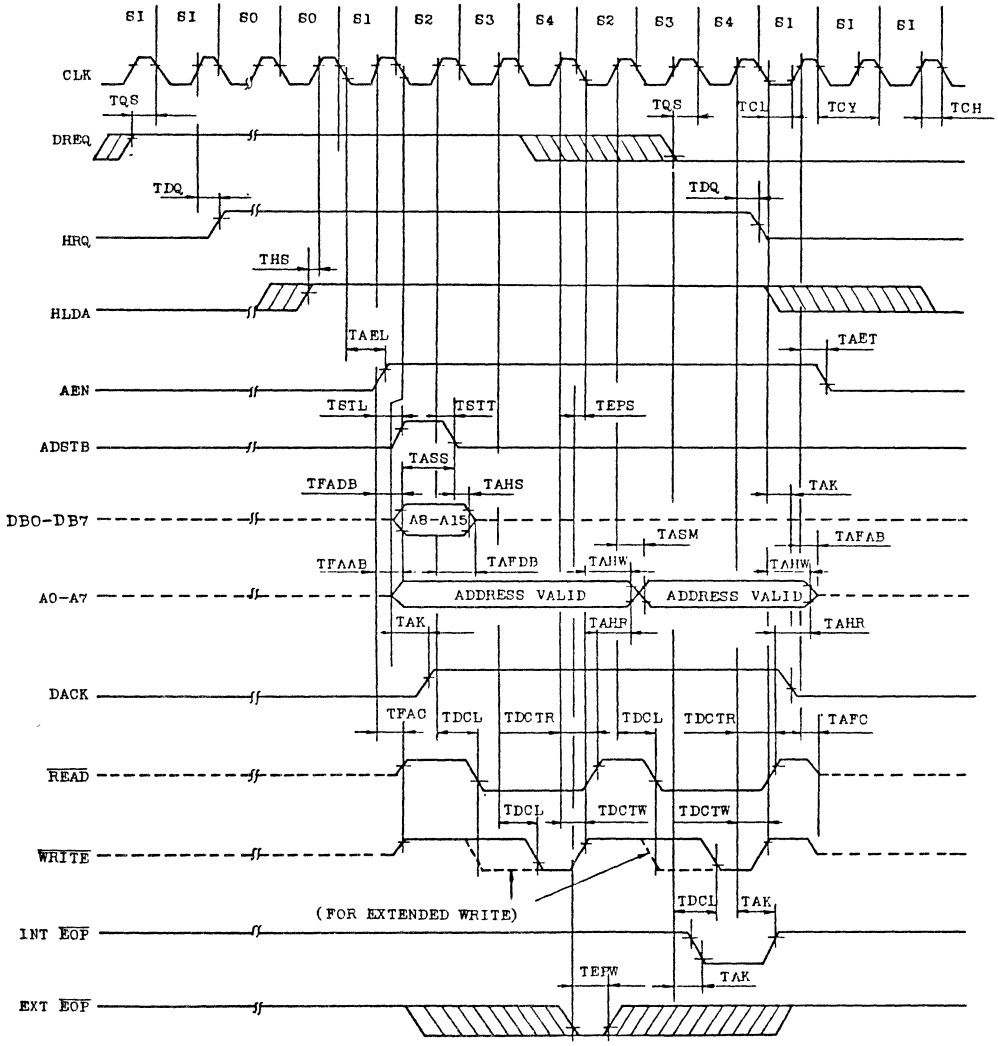
Timing Diagram



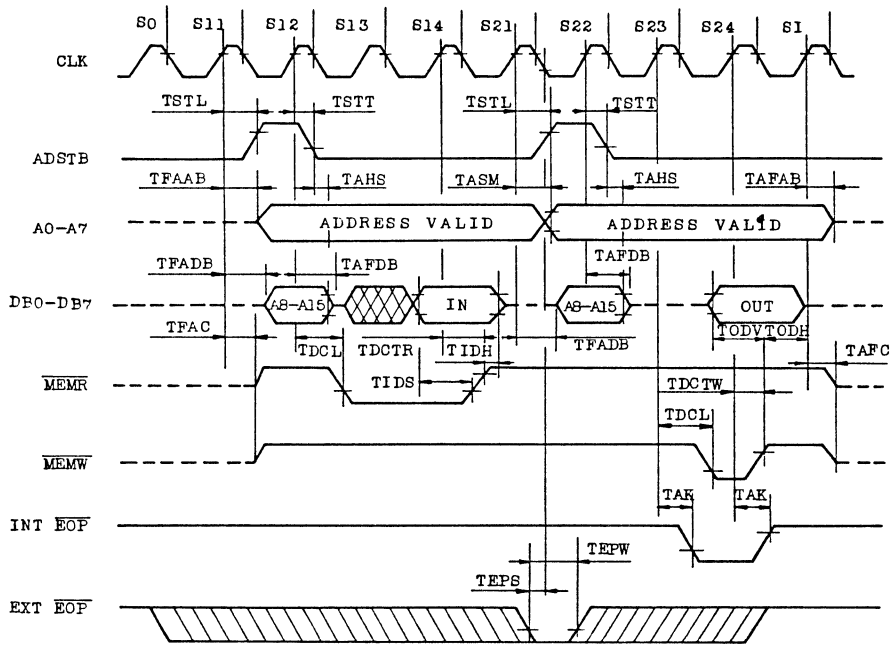
Timing Diagram 1 Program Condition Write Timing



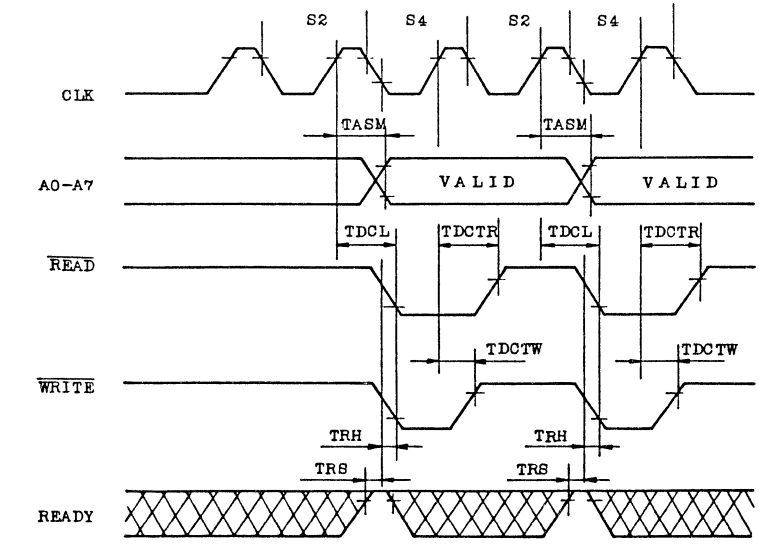
Timing Diagram 2 Program Condition Read Cycle



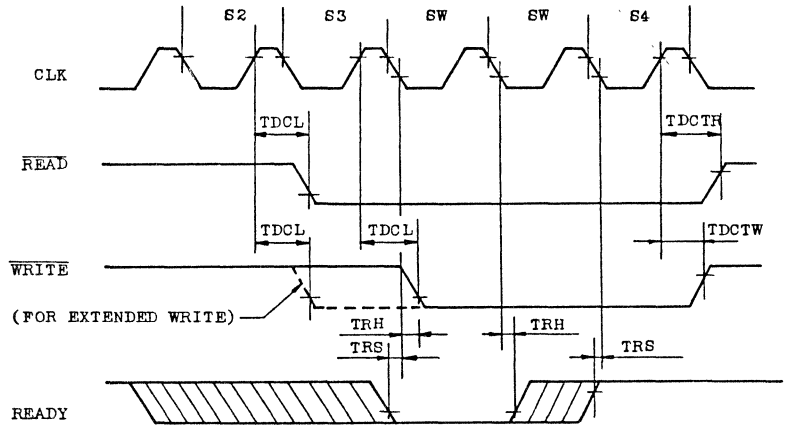
Timing Diagram 3 Active Cycle



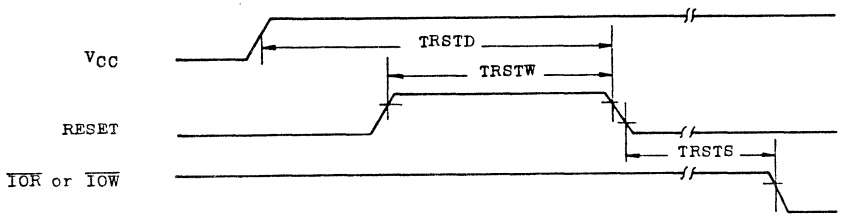
Timing Diagram 4 Memory-to-Memory Transfer



Timing Diagram 5 Compressed Transfer



Timing Diagram 6 Ready Timing



Timing Diagram 7 Reset Timing

Note 1. TYP. value is that when rated voltage is applied at Ta = 25°C.

Note 2. Test conditions; a) Unless otherwise specified, timing defining signal voltages are;
Input High level = 2.4V, Low level = 0.45V
Output High level = 2.2V, Low level = 0.8V
b) Input rising and falling times are below 20 ns.
c) Unless otherwise specified, 1 x TTL gate and 150 pF load are provided to output.

Note 3. Normal write pulse width is TCY-100 ns. Extension write pulse width is 2TCY-100 ns. Read pulse width is 2TCY-50 ns, and compressed read pulse width is TCY-50 ns.

Note 4. TDQ is measured at two different high levels.
TDQ1 = 2.2V, TDQ2 = 3.3V

Note 5. It is necessary to keep DREQ active until DACK is received.

Note 6. Both low active and high active level are available for DREQ and DACK.

Note 7. Output load of the data bus are provided with 1 x TTL gate and 15 pF as the minimum value, and 1 x TTL gate and 150 pF as the maximum value.

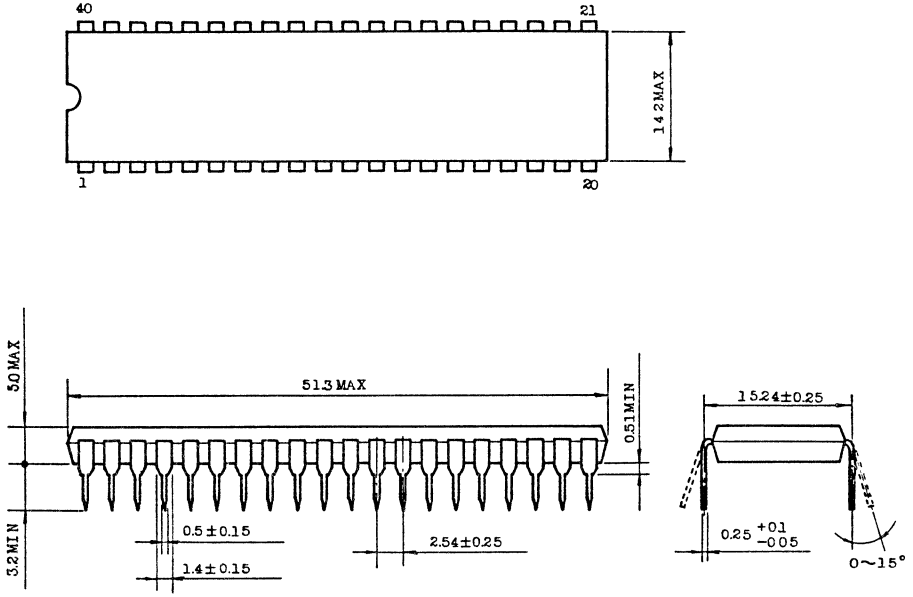
Note 8. 400 ns are required for active read or write pulse recovery time at time of program condition.

Note 9. Signal $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$ are $\overline{\text{IOR}}$ and $\overline{\text{MEMR}}$ for the DMA operations from peripheral devices to the memory. In the DMA operations from the memory to peripheral devices, they are $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$.

Note 10. When N state wait is added at time of write to memory in the latter half of memory-to-memory transfer, this parameter increases by N (TCY) at a time.

EXTERNAL DIMENSION VIEW (Plastic Package)

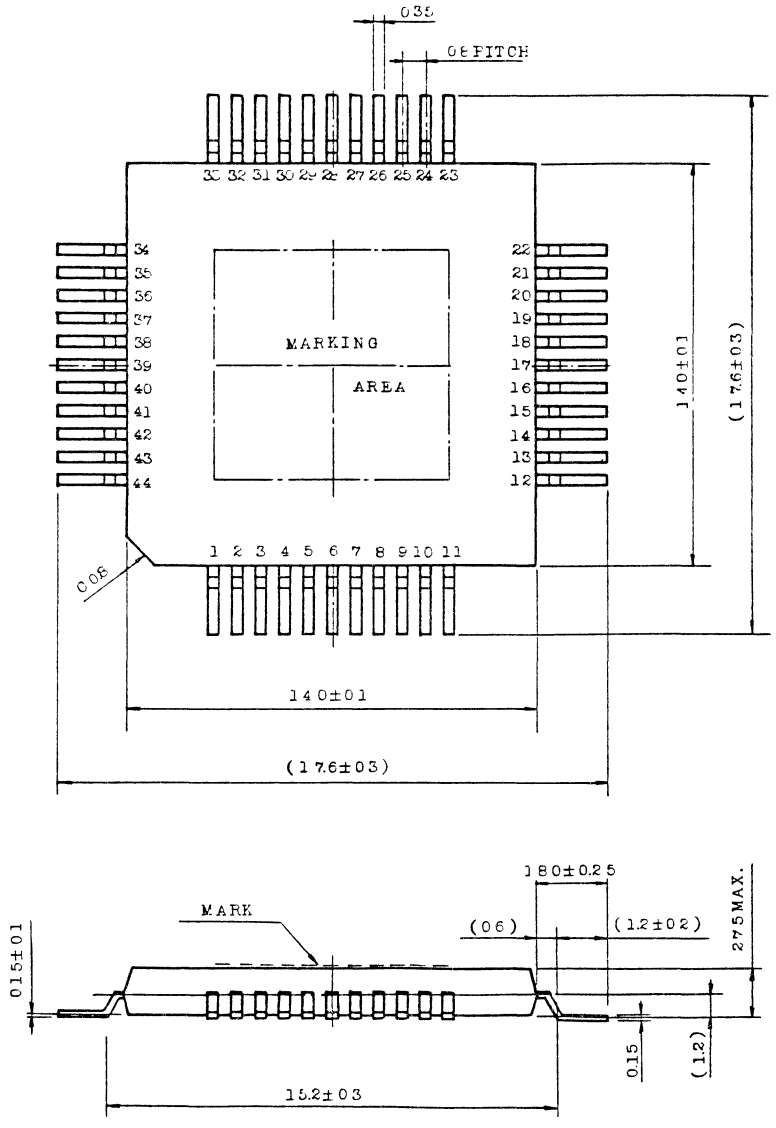
Unit in mm



Note Each pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoretical positions with respect to No. 1 and No. 40 leads.

EXTERNAL DIMENSION VIEW (Mini Flat Package)

Unit in mm



Example of Application Circuit

The connecting method of the TMP82C37A and CPU is shown in Fig. 7.

The multimode DMA controller outputs a hold request whenever valid DMA request is produced from peripheral device. When CPU answers by the hold acknowledge signal, the TMP82C37A receives the control right of the address bus, data bus, and control bus. In the first transfer, address (the least significant 8 bits of the address bits and the most significant 8 bits on the data bus) is output.

The content of the data bus is latched by the 8-bit latch (TC74HC373P) to make the address bus complete. After execution of the first transfer, that latched data is updated only when carry or borrow is produced on the least significant address byte.

When one TMP82C37A is used, four DMA channels are provided.

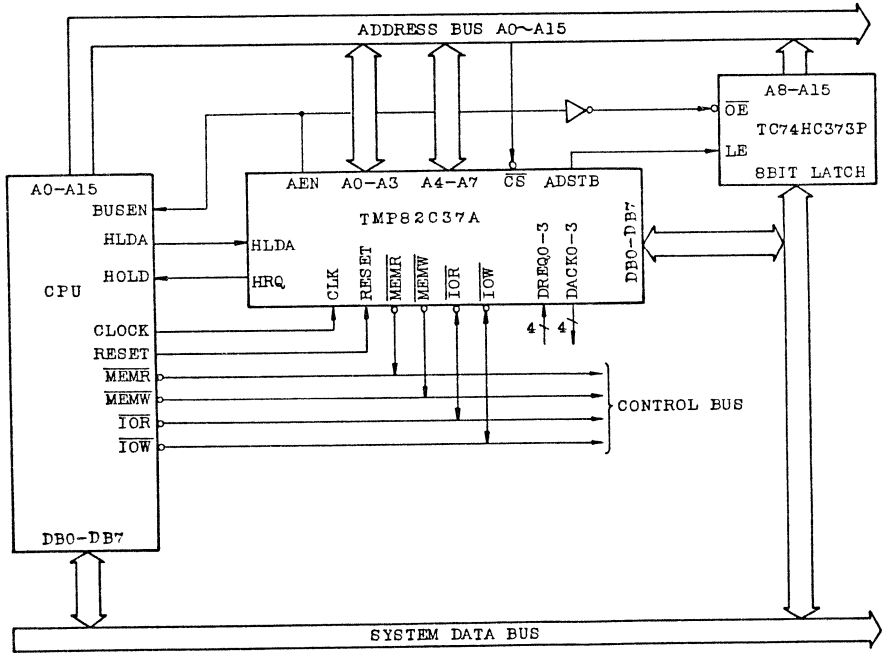


Fig. 7 Basic System Connection Diagram

Fig. 8 shows the expansion method for number of DMA channels. It is possible to realize net 7 DMA channels by connecting the second TMP82C37A to one of the DMA channels of the first TMP82C37A.

Two DMA chips commonly use the same 8-bit latch. Thus, any channel is used for expansion.

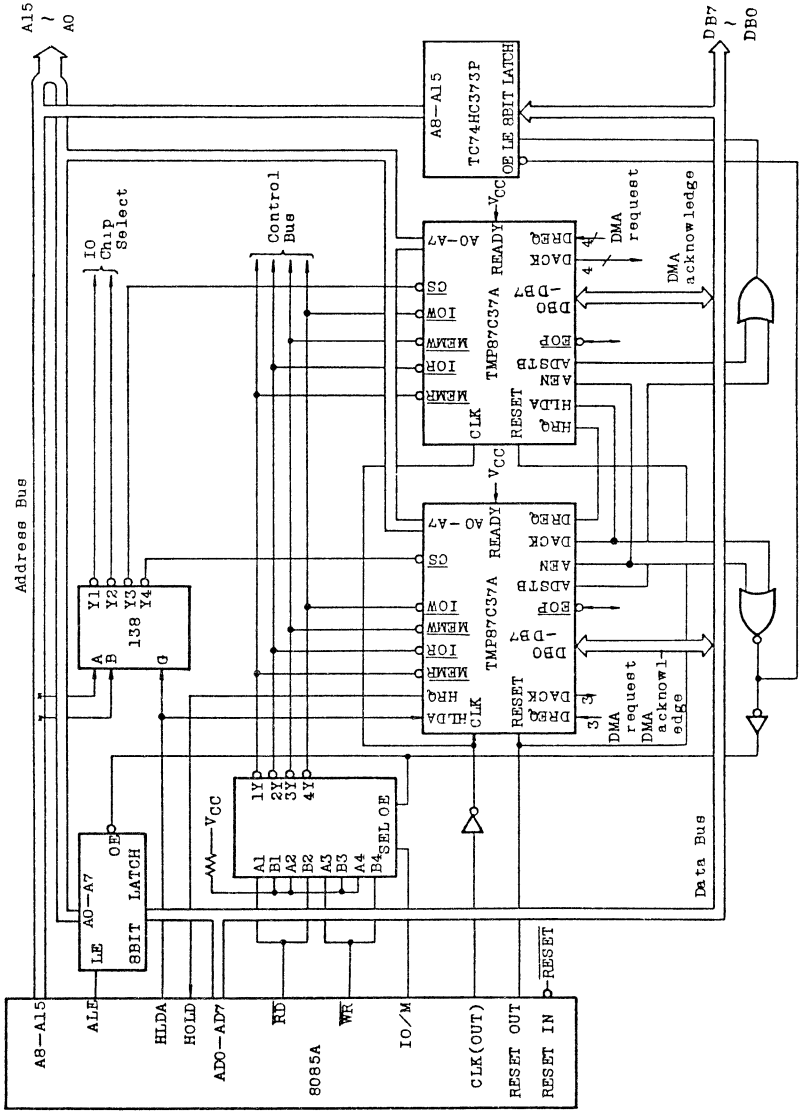


Fig. 8 Expansion of TMP82C37A

TOSHIBA MOS TYPE DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC TMP8237AP

MULTI MODE DMA CONTROLLER

GENERAL DESCRIPTION

The TMP8237AP (hereinafter referred to as TMP8237A) is a multi-mode direct memory access (DMA) controller. The TMP8237A improves the system function by directly transferring information between the system memory and external devices. Memory-to-memory data transfer is also possible.

The TMP8237A is provided with versatile programmable control functions in order to improve data throughput.

The TMP8237A is used with an 8-bit address register connected externally. The TMP8237A has four built-in independent channels and it is possible to extend channels through cascade connection.

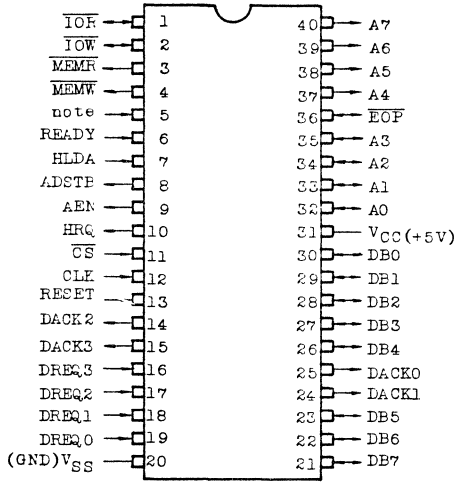
There are three basic data transfer modes which are programmable by the user. Each channel is programmable individually and auto initialization is possible by End of Process ($\overline{EOP}$) signal.

Each channel has the maximum 64K capability for both address and word count. $\overline{EOP}$ signal is capable of terminating data transfer between DMAs and memories. $\overline{EOP}$ signal is useful for block search or verify or for terminating erroneous servies.

FEATURES

- o Four independent DMA channels available, each of which has the following registers; mode countrol, current address, base address, current word count, and base word count registers.
- o Four transfer modes available; block, demand, single word, and cascade modes.
- o Independent auto initialize function provided to each of all channels.
- o Memory-to-memory transfer
- o Address increment or decrement
- o All DMA request disabled by disabling the master system
- o Individual DMA request eanble/disable control
- o Unrestricted channel extension by cascade connection
- o End of Process ($\overline{EOP}$) input terminal for terminating transfer.
- o DMA request by software
- o Polarity control provided for DREQ signal and DACK signal
- o Option for increasing transfer speed up to 1.5M word/sec.
- o Single +5V power supply

Pin Connections

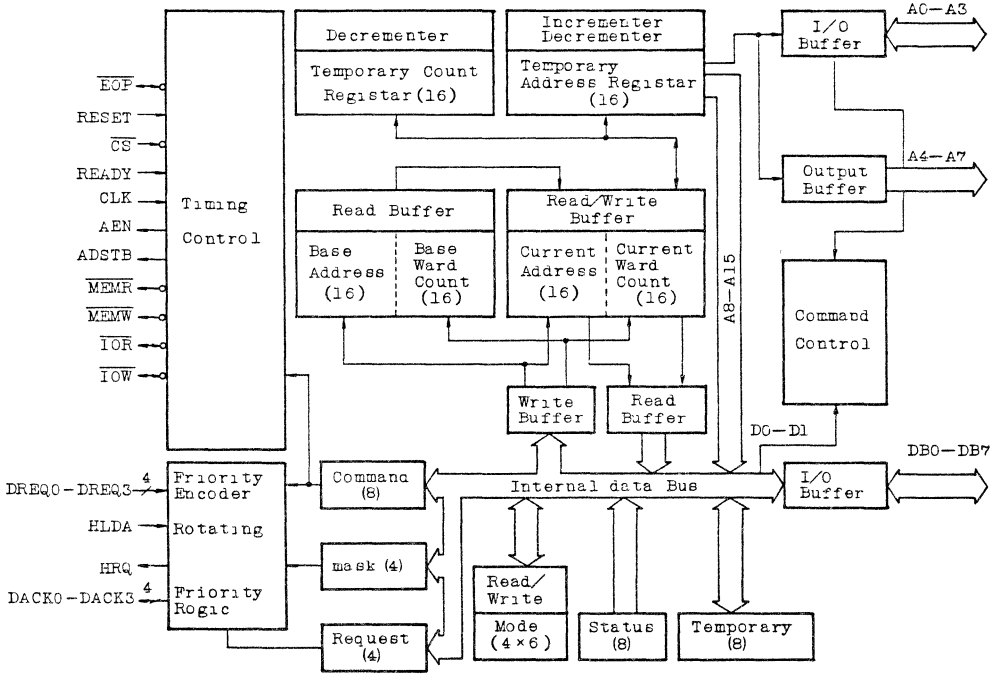


Pin Names

$A_0 \sim A_7$	Address Bus
$DB_0 \sim DB_7$	Data Bus
$DREQ_0 \sim DREQ_3$	DMA Request
$DACK_0 \sim DACK_3$	DMA Acknowledge
$\overline{CS}$	Chip Select
$\overline{IOR}$	I/O Read
$\overline{IOW}$	I/O Write
$\overline{MEMR}$	Memory Read
$\overline{MEMW}$	Memory Write
READY	Ready
HLDA	Hold Acknowledge
ADSTB	Address Strobe
AEN	Address Enable
HRQ	Hold Request
CLK	Clock
RESET	Reset
$\overline{EOP}$	End of Process
V_{CC}, V_{SS}	+5V, GND

Note) +5V connection or open state is available.

Block Diagram



OPERATIONAL DESCRIPTION

Description of I/O signals

- VCC
  +5V power supply

- VSS
  Ground

- CLK (Clock, Input)
  This input controls the internal operation and data transfer rate of the TMP8237A.

- $\overline{CS}$ (Chip Select, Input)
  This input is low active and used to select the TMP8237A as an I/O device during an I/O read or I/O write by the host CPU. If $\overline{IOR}$ or $\overline{IOW}$ is toggeled following each transfer when a host CPU and the TMP8237A are transferring data mutually, $\overline{CS}$ may be kept at LOW.

- RESET (Reset, Input)
  This input is asynchronous input to clear the command, status, request and temporary registers. In addition, this input is used to clear First/Last flip-flops and set the mask register. Following the reset, the TMP8237A is placed in the idle cycle.

- READY (Ready, Input)
  This input is used to extend the memory read and write pulses from the TMP8237A in order to adapt to a slow memories or I/O peripheral devices.

- HLDA (Hold Acknowledge, Input)
  By this signal, the TMP8237A knows that the system bus control is turned over from CPU.

- $DREQ_0$ - $DREQ_3$ (DMA Request, Input)
  DMA request signals are input from peripheral circuits. If priority is fixed, the highest priority is given to $DREQ_0$ and the lowest priority to $DREQ_3$. Polarity of DREQ is programmable. DREQ becomes high active by RESET.

- DB0 - DB7 (Data Bus, Input/Output)
  The Data Bus lines are bidirectional three-state signals connected to the system data bus. When CPU is in I/O read state, output is enabled and contents of the registers (address, status, temporary and word count) are output to CPU. When CPU is in I/O write state, the data bus serves as input and it becomes possible to program the control register of the TMP8237A.

  During the DMA cycle, high order 8 bits of address are output on the data bus and latched by ADSTB signal externally. During the memory-to-memory transfer, the data of the source memory location are loaded into the temporary register of the TMP8237A by the read operation and the contents of the temporary register are output to the destination memory location by the write operation.

- $\overline{IOR}$ (I/O Read, Input/Output)
  I/O read is a bidirectional, low active and 3-state signal. During the idle cycle, this signal serves as an input control signal used by CPU to read the control registers of the TMP8237A. During the active cycle, this signal serves as an output control signal used by the TMP8237A to access data from the peripheral circuit during the DMA read and transfer.
- $\overline{IOW}$ (I/O Write, Input/Output)
  I/O write is a bidirectional low active, 3-state signal. During the idle cycle, this signal serves as an input control signal used by CPU to load the information to the TMP8237A. During the active cycle, this signal served as an output control signal used by TMP8237A to load the data to the peripheral. For write to the TMP8237A by CPU, the leading edge of the write signal ($\overline{IOW}$) is required for every data transfer. It is not possible to write more than two data by toggling $\overline{CS}$ while holding the $\overline{IOW}$ pin at low level.

- $\overline{EOP}$ (End of Process, Input/Output)
  $\overline{EOP}$ (End of Process) is a signal relative to end of DMA service, and is a low active, bidirectional and open drain signal. When the channel word count reaches zero, the TMP8237A outputs low pulse of $\overline{EOP}$ to peripheral deives as the end signal.
  In addition, it is also possible to pull $\overline{EOP}$ to the low level by peripheral device in order to cause the end of process.
  When $\overline{EOP}$ is received (internally or externally), the channel which is presently active terminates the service, sets that TC bit of the status register and resets that request bit.
  If that channel is programmed for auto initialization, that current register is updated from the base register. In all other cases, mask bit is set and the content of that register remains unchanged.
  During the memory-to-memory transfer, $\overline{EOP}$ is output when TC of channel 1 is produced. $\overline{EOP}$ is always used for channels with active DACK and external EOP has no connection when $DACK_0$ - $DACK_3$ are all inactive.
  $\overline{EOP}$ is an open drain signal and therefore, requires an external pull-up resistor.

- A0 to A3 (Address, Input/Output)
  The low order 4 address lines are the bidirectional 3-state terminals. In the idle cycle, these terminals serve as the input terminals and used by CPU for write/read of the control register. In the active cycle, they serve as the output terminals and become low order 4 bits of output address.

- A_4 - A_7 (Address, Output)
  The high order address lines are 3-state output terminals. These terminals are enabled for the period of DMA service only.

- HRQ (Hold Request, Output)
  This is the hold request signal to CPU, and is used to request the system bus control. HRQ is output by the TMP8237A according to a software request or unmasked DREQ.

- $DACK_0$ - $DACK_3$ (DMA Acknowledge, Output)
  The DMA acknowledge lines indicate that channels are active. On ordinary systems, these are used for selecting peripherl devices. Only one DACK becomes active but it does not become active unless DMA is controlling the system bus. Porarily of these lines is programmable. When reset, they become low active.

- AEN (Address Enable, Output)
  Address Enable is a high active signal and used to enable output of the external latch which holds high order bytes of address and to disable the system bus during the DMA cycle.
  During the DMA transfer, HLDA and AEN are used to disable all I/O except programmed I/O. The TMP8237A disables CS input for DMA transfer to prevent itself from being selected automatically.

- ADSTB (Address Strobe, Output)
  This signal is a strobe output to an external latch circuit and is used to latch high order 8-bit address from DB_0 - DB_7.

- $\overline{MEMR}$ (Memory Read, Output)
  This is a low active 3-state output used for transferring data from a memory to a peripheral device or for data accessing from a selected memory during the memory-to-memory transfer.

- $\overline{MEMW}$ (Memory Write, Output)
  This is a low active 3-state output used for transferring data from a peripheral device to a memory or for writing data into a selected memory during the memory-to-memory transfer.

FUNCTIONAL DESCRIPTION

- DMA Operation
  The TMP8237A has two operations; idle cycle and active cycle. Each of these cycles consists of several states.
  On the TMP8237A, it is possible to consider 7 states each of which consists of one clock cycle. State I (SI) is an idle state. This is such a state as there is no valid DMA request pending. SI is a program condition state which is programmable by CPU.
  State 0 (S0) is the first DMA service state. This is a state that the TMP8237A made a hold request to CPU but not yet received the acknowledge signal from CPU. When the acknowledge signal is recieved from CPU, the transfer is started.
  S1, S2, S3 and S4 are the DMA service state. If much time is required by the transfer, it is possible to insert the wait state (SW) before S4 by READY input to the TMP8237A.
  In the memory-to-memory transfer, in order to assure complete transfer, read from the memory and write to the memory are required. 8 states are necessary for one transfer. The first four states (S11, S12, S13 and S14) are read from the memory and the latter four state (S21, S22, S23 and S24) are write to the memory.
  The temporary data register is used as an intermediate storage area of memory bytes.

o Idle cycle

When DMA service is not requested by channels, the TMP8237A enters into the idle cycle and is placed in SI state. In order to check if the channels request DMA service, the TMP8237A samples DREQ for every clock.

The TMP8237A also samples $\overline{CS}$ to check if CPU is requesting read or write of internal registers. When $\overline{CS}$ is low and HLDA is also low, the TMP8237A is placed in the program condition.

At this time, CPU is able to change or check the content of any internal register through read or write from that register.

Address lines A0 - A3 are input signals and used for selecting a register being read or written. $\overline{IOR}$ and $\overline{IOW}$ are used for selecting read or write and decide read/write timing.

The internal flip-flop is used for generating address extension bits according to number and size of internal registers. (First/Last Flip-flop) This bit is used for deciding high or low order bytes of 16-bit address and word counter register.

The flip-flop is reset by the master clear or reset. In addition, this flip-flop also can be reset by an independent software command. On a special software command, the execution in the TMP8237A program condition is possible. These commands are decoded as in the address setting when both $\overline{CS}$ and $\overline{IOW}$ are active.

The data bus is not used for this command. This command is available in two types; clear First/Last flip-flop and master clear.

o Active cycle

When the TMP8237A is in the idle cycle and the channels are requesting DMA service, the TMP8237A outputs HREQ to CPU and goes into the active cycle. In this cycle, the DMA service for any one of 4 modes is executed.

Single Transfer Mode:

In this mode, the TMP8237A performs a single byte transfer during each HRQ/HLDA handshake. When DREQ becomes active, HRQ becomes active. After CPU responds by driving HLDA active, a single byte transfer will take place. After the transfer HRQ becomes inactive, its word count is decreased, and address is increased or decireased. When word count becomes zero, a terminal signal is generated and if the channels are programmed, the auto initialization is made.

To execute the single byte transfer, it is necessary to hold DREQ until DACK corresponding each DREQ becomes active. If DREQ is continuously active, HRQ becomes inactive following each transfer and then, becomes active again, and the new single byte is executed following the leading edge of HLDA.

On the 8085 system, one machine cycle can be executed during the DMA transfer.

Block Transfer Mode:

In this mode the TMP8237A continues the transfer until terminal count (TC) is generated or End of Process signal ($\overline{EOP}$) is externally input. Here, TC is produced when the word count becomes zero.

What is required for DREQ is to hold it in active state until DACK becomes active. Auto initialization (if so programmed) is taken place at the end of DMA service.

Demand Transfer Mode:

In this mode the TMP8237A continues the transfer when TC is produced or EOP is input or until DREQ becomes inactive. Thus, it is possible for a device, which is requesting the DMA service, to suspend the transfer by making DREQ inactive. The service is resumed when DREQ is made active again. It is possible to read an intermediate value of address and word count from the current address and current word count register of the TMP 8237A while the system bus is returned to CPU during execution of the DMA service.

The auto initialization is taken place following TC or $\overline{EOP}$ at the end of DMA service. In order to perform a new DMA service following the auto initialization, the active edge of DREQ is necessary.

Cascade Mode:

This mode is used when the TMP8237A is cascade connected for a simple system extension. HRQ and HLDA of the additional TMP8237A are connected to DREQ and DACK of the first TMP8237A. DMA request to the TMP8237A which is added for the purpose of system extension is authorized by the priority circuit of the first TMP8237A.

If the priority is already decided, the DMA request of additional device must wait till the DMA acknowledge of first TMP8237A. The cascade channel of the first TMP8237A is used only for deciding priority of the additional TMP8237A and therefore, the channel itself does not output address nor control signal. This is to prevent the added device from colliding with output of the cascade channel. On the TMP8237A, DACK answers DREQ. However all other outputs except HRQ are disabled.

The state of cascade connection is shown in Fig. 2. In Fig. 2, two levels of DMA are formed. To further extend the TMP8237A, it is possible to add it to the second level using the remaining channel of the first TMP8237A. To further add another TMP8237A, the third level can be formed by cascade connecting it to the second level.

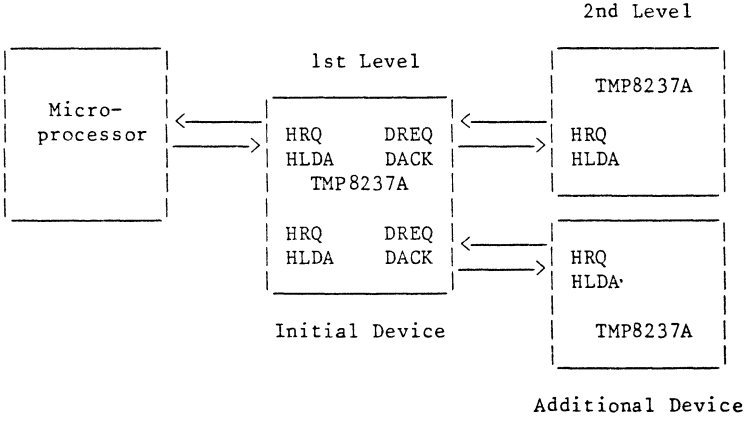


Fig. 2 Example of Cascade Connection of TMP8237A

o Transfer format

3 different transfer format are available for 3 active transfer modes. They are read, write and verify. In the write transfer, data is transferred from I/O dvice to memory by $\overline{MEMW}$ and $\overline{IOR}$. In the read transfer, data is transferred from memory to I/O device by $\overline{MEMR}$ and $\overline{IOW}$.

The verify transfer is a temporary transfer. The TMP8237A perform such operations as address generation for read or write transfer, answer to $\overline{EOP}$, etc. However, memory or I/O control line does not become active.

Memory-to-Memory Transfer:

The TMP8237A has the ability of block movement and is capable of transferring data block from one memory address location to another location. When Bit C0 of the command register is programmed at Logic 1, Channel 0 and 1 operate as the memory-to-memory transfer channels. Channel 0 serves as a source address and Channel 1 as a destination address, and the word count of Channel 1 is used. The memory-to-memory transfer is executed when software DMA requrest is set for Channel 0.

The memory-to-memory transfer must use the block transfer mode.

When Channel 0 is programmed as a fixed source address, it is possible to write single source words into a memory block.

When the TMP8237A is programmed for the memory-to-memory transfer, Channel 0 and Channel 1 must be masked. The same value as that is set for Channel 1 must be set for the word count of Channel 0. During the memory-to-memory transfer, DACK does not become active.

During the memory-to-memory transfer, the TMP8237A answers external $\overline{EOP}$ signal. In the block search, the data comparator uses this ($\overline{EOP}$) input to terminate the DMA serive when match is found. The memory-to-memory transfer is shown in Timing Diagram 4.

Auto Initialization:

When Bit 4 of the mode register is set to 1, the channels are set up for the auto initialization. During the auto initialization, data are loaded into the current address and current word count registers from the base address and base word count registers, respectively, following EOP. The base registers are loaded by CPU simultaneously with the current registers and remain unchanged during the DMA service.

When the channels are under the auto initialization, mask bit is not set by $\overline{EOP}$.

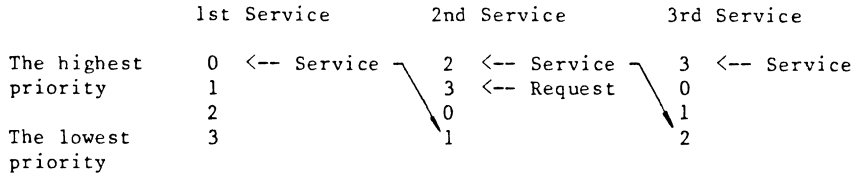
Following the auto initialization, that channel is prepared to execute the service without interposition of CPU.

Priority:

The TMP8237A has two types of priority as an option, which can be selected by software. The first type is the fixed priority. Channel priority is fixed by channel number. The lowest priority is 3, followed by 2, 1, and the highest priority is 0.

The second type is the rotating type priority. In this type, an accepted channels is then given with the lowest priority (See the following diagram.).

On the rotating priority in the single chip DMA system, highest priority of any one channel comes after no more than three higher priority services have occurred. This rotating priority preclued one channel to occupy the system all the time.



The priority judging circuit selects a channel with the highest priority requesting the DMA service for every active edge of HLDA

Once the channel starts the service, that operation will not be suspended even when the service is demanded by another channel with higher priority. A channel with higher priority can get the control right only after a channel with lower priority relinquished HRQ. Whenever the control is transferred from a channel to another channel, CPU gets the system bus control right. This assures the leading edge of HLDA which is used for selecting a channel with the highest priority.

Shortening of Transfer Time:

In order to accomplish larger throughput allowed by system characteristics, the TMP8237A is capable of shortening the transfer time to 2 clock cycles. As can be seen from Timing Diagram 3, State S3 is used to extend readout pulse access time. When State S3 is removed, readout pulse width becomes equal to write pulse width. Then, the transfer will consist of State S2 for changing address and State S4 for executing read/write. State S1 is produced when A8 to A15 are updated (refer to Address Generation). Shortening of transfer time is shown in Timing Diagram 5.

Address Generation:

To reduce number of pins, the TMP8237A has high order 8 bits multiplexed with the data bus. State S1 is used to output high order address bits to the external latch. The trailing edge of ADSTB is used to load address bits from the data line on the external latch circuit. AEN is used to enable latch outputs from high impedance states. Low order address bits are ditectly output by the TMP8237A.

A0 to A7 are connected to address buses. Timing Diagram 3 show the relationship among CLK, AEN, ADSTB, DB0 to DB7 and A0 to A7.

Addresses produced during the block and demand transfers are continuous. In the transfer of much blocks and demands, the same external address latch is left. This address data changes only when carry or borrow from A7 to A8 is produced in the normal sequence. To save time and speed, on the TMP8237A, S1 state is executed only for update of A8 to A15 rquiring the latch.

Description of Registers

Register Name	No. of Bit	Quantity
Base address register	16-bit	4
Base word count register	16-bit	4
Current address register	16-bit	4
Current word count register	16-bit	4
Temporary address register	16-bit	1
Temporary word count register	16-bit	1
Status register	8-bit	1
Command register	8-bit	1
Temporary register	8-bit	1
Mode register	6-bit	4
Mask register	4-bit	1
Request register	4-bit	1

Fig. 3 Internal Register

Current Address Register:

Each channel has a 16-bit current address register. This register holds addresses that are used during the DMA transfer. After each transfer, this register is automatically incremented or decremented, and intermediate address values are stored in the current address register during the transfer. Write or read of this register is made by CPU. An original value is initialized again by the auto initialization.

The auto initialization is taken place only after $\overline{EOP}$.

Current Word Count Register:

Each channel has a 16-bit current word count register. For this register, number of words that is one less than that to be tranferred must be programmed. The word counter is decremented after each transfer. Intermediate values of word count are stored in this register during the transfer. When the register value becomes zero, TC is produced.

When this register is in the program condition, load or read is made by CPU. Following the end of DMA service, this register is initialized to original values again by the auto initialization.

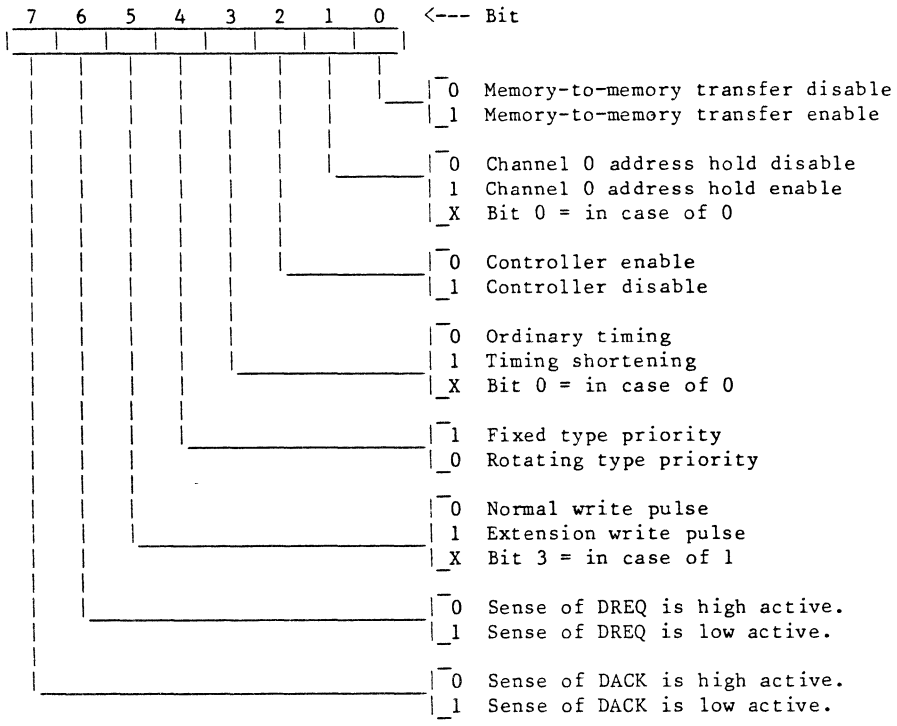
The auto initialization is taken place only when $\overline{EOP}$ is produced. Be careful that the content of the word count register becomes FFFFH following internally produced $\overline{EOP}$.

Base Address Register, Base Word Count Register:

Each channel has a pair of registers; the base address register and base word count register. These 16-bit registers store original values of related current registers. These registers are used to store original values of current registers at time of the auto initialization. Write to the base register is made at the same time of write into 8-bit byte equivalent current registers during the programming by CPU. Therefore, write into the current registers which store intermediate values are made over these intermediate values. The base register cannot be read out by CPU.

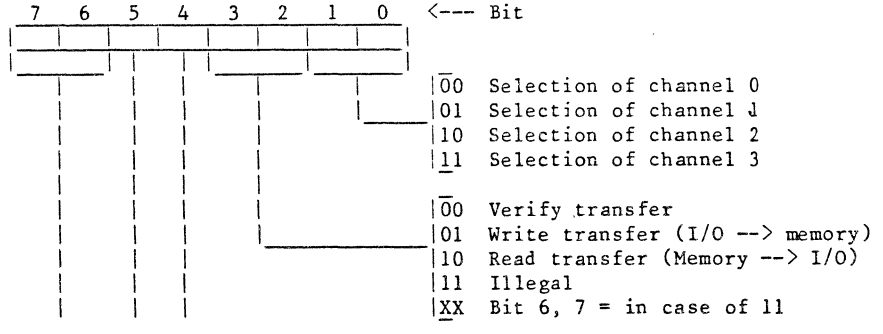
Command Register:

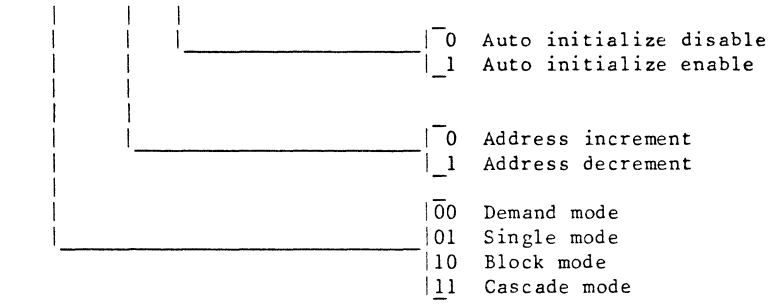
This 8-bit register controls the operation of TMP8237A. This command register is programmed (clear or reset) by CPU when it is in the program condition. The charts presented below show the functions of command bits. For address codes, refer to Fig. 4.



Mode Register:

All channels have a 6-bit mode register, respectively. This mode register is written by CPU when it is in the program condition, and Bit 0 and 1 decide which channel's mode register is to be written.



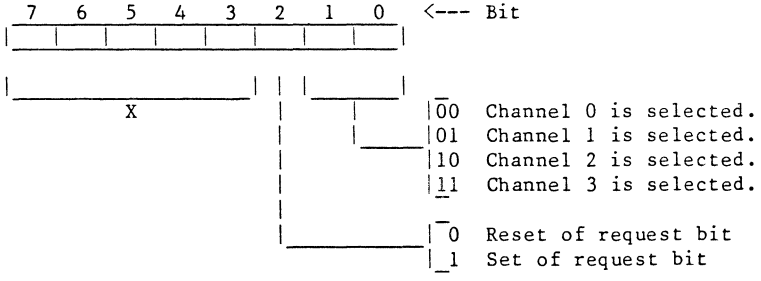


Request Register:

The TMP8237A is capable of answering DMA service request by software similar to DREQ. Each channel has a single bit request register which cannot be masked. Further, priority is given by the priority encode circuit.

Bit of each register is set or cleared by software and further, cleared by generation of TC or external EOP. All registers are cleared by reset. In order to set or reset bit, a proper form of data word is loaded by software.

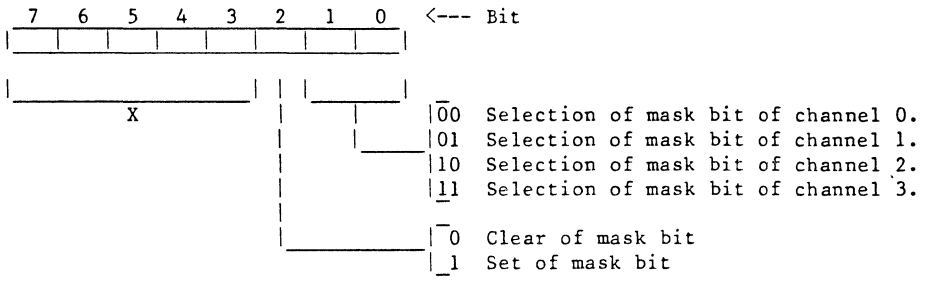
Address codes are shown in Fig. 4. DMA service request by software is accepted only when the channels are in the block mode. In the memory-to-memory transfer, DMA service request by the software command to Channel 0 only becomes valid.



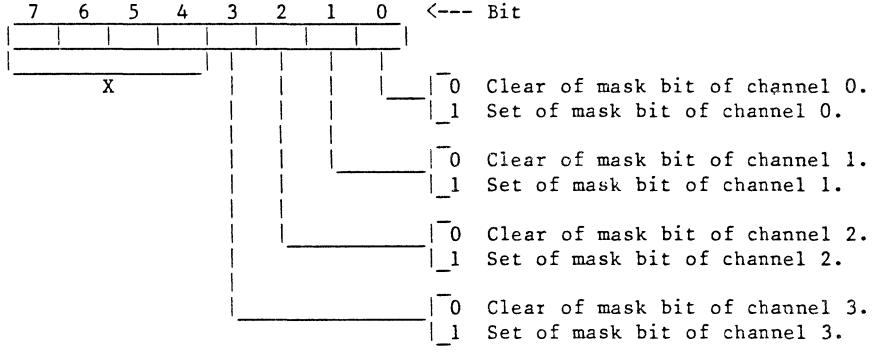
Mask Register:

For each channel, mask bits are allocated to the mask register to disable DREQ input. If the auto initialization has not been programmed for the channels, the channel corresponding to a mask bit is set when EOP is produced. Each bit of the 4-bit mask register is also set or cleared by the software command. All bits are also set by reset. This will disable all DMA requests until the clear mask register command is enabled.

Command addressing is shown in Fig. 4.



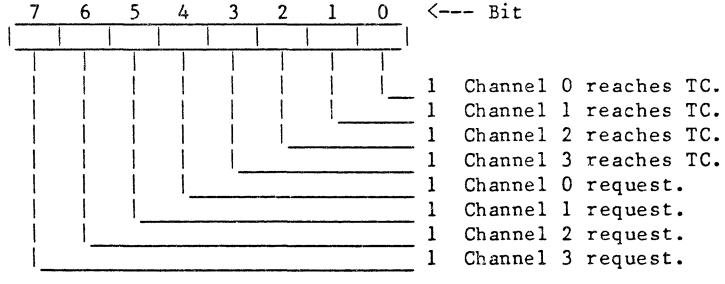
All four bits of the mask register can be written also by a single command.



Status Register

This register is read out by CPU through the TMP8237A. Status information of the TMP8237A at time of readout is included. Information as to which channel reaches the terminal count (TC) and which channel is pending the DMA request are included in this information. Bits 0 to 3 are set every time when a channel reaches TC including the auto initialization.

These bits are cleared by reset or when each status is read out. bits 4 to 7 are always set when corresponding channels are requesting the DMA service



Temporary Register:

This register is used for holding data during the memory-to-memory transfer. A last word transferred following the end of tranfer is read out by CPU that is in the program condition. Unless cleared by reset, this register contains the last word transferred during the preceding memory-to-memory transfer.

Software Commands:

These commands are special software commands which are executed in the program condition and do not depend upon the specified bit pattern on the data bus. These commands are available in following two commands:

Clear First/Last flip-flop

This command is executed prior to write or read of address information or word count information of the TMP8237A. Furthermore, this command is used when low order or high order 8 bits of register are accessed.

Master Clear

This software command has the same effect as the hardware reset. The command, status, request, temporary, and internal First/Last flip-flop registers are all cleared by this command, and the mask register is set.

The TMP8237A enters into the idle cycle.

Clear Mask Register

This command clears all mask bits of four channels, enabling acceptance of the DMA service requests.

Address codes of the software commands are shown in Fig. 4.

Signal						Operation
A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$	
1	0	0	0	0	1	Read of status register
1	0	0	0	1	0	Write to command register
1	0	0	1	0	1	-
1	0	0	1	1	0	Write to request register
1	0	1	0	0	1	-
1	0	1	0	1	0	Bit set, reset of mask register
1	0	1	1	1	0	-
1	0	1	1	1	0	Write to mode register
1	1	0	0	0	1	-
1	1	0	0	1	0	Clear First/Last flip-flop
1	1	0	1	0	1	Read of temporary register
1	1	0	1	1	0	Master clear
1	1	1	0	0	1	-
1	1	1	0	1	0	Clear mask register
1	1	1	1	0	1	-
1	1	1	1	1	0	All bit write of mask register

Note) The oblique lined codes denote illegal codes.

Fig. 4 Register and Function Addressing

(*): Internal F/L,F/F

Channel	Register	Operation	Signal							(*)	Data Bus
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		DB0-DB7
0	Base & Current Address	Write	0	1	0	0	0	0	0	0	A0 - A 7
			0	1	0	0	0	0	0	0	A8 - A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0 - A 7
			0	0	1	0	0	0	0	1	A8 - A15
	Base & Current Address	Write	0	1	0	0	0	0	1	0	W0 - W 7
			0	1	0	0	0	0	1	1	W8 - W15
	Current Address	Read	0	0	1	0	0	0	1	0	W0 - W 7
			0	0	1	0	0	0	1	1	W8 - W15
1	Base & Current Address	Write	0	1	0	0	0	1	0	0	A0 - A 7
			0	1	0	0	0	1	0	0	A8 - A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0 - A 7
			0	0	1	0	0	1	0	1	A8 - A15
	Base & Current Address	Write	0	1	0	0	0	1	1	0	W0 - W 7
			0	1	0	0	0	1	1	1	W8 - W15
	Current Address	Read	0	0	1	0	0	1	1	0	W0 - W 7
			0	0	1	0	0	1	1	1	W8 - W15
2	Base & Current Address	Write	0	1	0	0	1	0	0	0	A0 - A 7
			0	1	0	0	1	0	0	0	A8 - A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0 - A 7
			0	0	1	0	1	0	0	1	A8 - A15
	Base & Current Address	Write	0	1	0	0	1	0	1	0	W0 - W 7
			0	1	0	0	1	0	1	1	W8 - W15
	Current Address	Read	0	0	1	0	1	0	1	0	W0 - W 7
			0	0	1	0	1	0	1	1	W8 - W15
3	Base & Current Address	Write	0	1	0	0	1	1	0	0	A0 - A 7
			0	1	0	0	1	1	0	0	A8 - A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0 - A 7
			0	0	1	0	1	1	0	1	A8 - A15
	Base & Current Address	Write	0	1	0	0	1	1	1	0	W0 - W 7
			0	1	0	0	1	1	1	1	W8 - W15
	Current Address	Read	0	0	1	0	1	1	1	0	W0 - W 7
			0	0	1	0	1	1	1	1	W8 - W15

Fig. 5 Word Count, Address Registers

Programming

If HLDA of CPU is inactive it is possible to program the TMP8237A by CPU even when HRQ is active.

However, it is necessary for CPU to take care that programming of the TMP8237A and answer of HLDA are taken place simultaneously.

If requires care when the DMA service is requested to an unmasked channel during the programming of the TMP8237A.

It is considered that an embarrassing trouble may be caused in this case.

For instance, if CPU is going to rewrite the address register of channel 2 and in addition, the TMP8237A is enabled and channel 2 is not masked when channel 2 received a DMA request. The DMA service will be started after one byte of the address register is written. Such a problem as exampled above can be taken place.

To avoid such problems as this, it is better to disable the controller or mask unmasked channels before reprogramming any register.

It is better to enable the controller or clear the masking when the programming is completed.

Example of Program Set (CH2)

```
DI                  :  Interrupt disable
OUT    MCLR         :  Master clear
MVI    A, xxxxxxxxB
OUT    CMND         :  Command register set-up
MVI    A, xxxxxx10B
OUT    MODE         :  Mode register set-up
MVI    A, 37H
OUT    ADR2         :  CH2 Address Reg. (low order)
MVI    A, 82H
OUT    ADR2         :  CH2 Address Reg. (high order)
MVI    A, 17H
OUT    WCNT2        :  CH2 Word count register (low order)
MVI    A, 95H
OUT    WCNT2        :  CH2 Word count register (high order)
MVI    A, 00000010B
OUT    MSKB2        :  CH2 Mask clear (single bit)
EI                  :  Interrupt enable
```

ABSOLUTE MAXIMUM RATINGS

SIGNAL	ITEM	RATING	UNIT
Tstg	Storage Temperature	-65 to 150	°C
Topr	Operating Temperature	0 to 70	°C
VCC	Supply Voltage	-0.5 to 7.0	V
VIN	Input Voltage	-0.5 to 7.0	V
PW	Power Dissipation	1.5	W

DC CHARACTERISTICS

(Ta = 0°C to 70°C, VCC = 5V ± 5%, VSS = 0V)

SYMBOL	PARAMETER	CONDTION	MIN.	TYP.	MAX.	UNIT
VOH	Output High Voltage	IOH = -200 A	2.4			V
		IOH = -100 A (HRQ only)	3.3			
VOL	Output Low Voltage	IOL = 3.2mA			0.45	V
VIH	Input High Voltage		2.2		VCC+0.5	V
VIL	Input Low Voltage		-0.5		0.8	V
IIX	Input Load Current	VSS<VI<VCC			±10	A
IOZ	Output leak Current	0.5V<VO<VCC			±10	A
ICC	Supply Current				150	mA

AC CHARACTERISTICS

Active Cycle (Notes: 2 and 9) [Ta=0°C to 70°C, VCC=5V±5%, VSS=0V]

ABBR.	PARAMETER	MIN.	MAX.	UNIT
TAEL	CLK = 0(SI) --> AEN = 1 Delay time		300	ns
TAET	CLK = 1(SI) --> AEN = 0 Delay time		200	ns
TAFAB	CLK = 1 --> ADR floating		150	ns
TAFC	CLK = 1 --> $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ floating		150	ns
TAFDB	CLK = 1 --> DB floating		250	ns
TAHR	$\overline{\text{READ}}$ = 1 --> ADR hold time	TCY-100		ns
TAHS	ADSTB = 0 --> DB hold time	30		ns
TAHW	$\overline{\text{WRITE}}$ = 1 --> ADR hold time	TCY-50		ns
TAK	CLK=0 --> Delay time up to DACK effective		250	ns
	CLK=1 --> Delay time up to $\overline{\text{EOP}}$=1		250	ns
	CLK=1 --> Delay time up to $\overline{\text{EOP}}$=0		250	ns
TASM	CLK=1 --> ADR stable time		250	ns
TASS	DB stability --> ADSTB = 0 Set-up time	100		ns
TCH	Clock High Level Time (Transition time : below 10 ns)	120		ns
TCL	Clock Low Level Time (Transition time : below 10 ns)	150		ns
TCY	Clock Cycle Time	320		ns
TDCL	CLK = 1 --> $\overline{\text{READ}}$ = 0 or $\overline{\text{WRITE}}$ = 0 (Note 3)		270	ns
TDCTR	CLK = 1 --> Delay time up to $\overline{\text{READ}}$ = 1 (Note 3)		270	ns
TDCTW	CLK = 1 --> Delay time up to $\overline{\text{WRITE}}$ = 1 (Note 3)		200	ns
TDQ1	(Note 4)		160	ns
TDQ2	CLK = 1 --> HRQ=1 or 0 Delay time		250	ns
TEPS	$\overline{\text{EOP}}$ = 0 --> CLK = 0 set-up time	60		ns
TEPW	$\overline{\text{EOP}}$ pulse width	300		ns
TFAAB	CLK = 1 --> ADR enable		250	ns
TFAC	CLK = 1 --> $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ enable		200	ns
TFADB	CLK = 1 --> DB enable		300	ns
THS	HLDA = 1 --> CLK = 1 set-up time	100		ns
TIDH	$\overline{\text{MEMR}}$ = 1 --> Input data hold time	0		ns
TIDS	Input data --> $\overline{\text{MEMR}}$ = 1 set-up time	250		ns
TODH	$\overline{\text{MEMW}}$ = 1 --> Output data hold time	20		ns
TODV	Output data stability --> $\overline{\text{MEMW}}$ = 1 (Note 10)	200		ns
TQS	DREQ=Active --> CLK=0 (S1,S4) set-up time	0		ns
TRH	CLK = 0 --> READY = 0 hold time	20		ns

ABBR.	PARAMETER	MIN.	MAX.	UNIT
TRS	READY = 0 --> CLK = 0 set-up time	100		ns
TSTL	CLK = 1 --> ADSTB = 1 Delay time		200	ns
TSTT	CLK = 1 --> ADSTB = 0 Delay time		140	ns

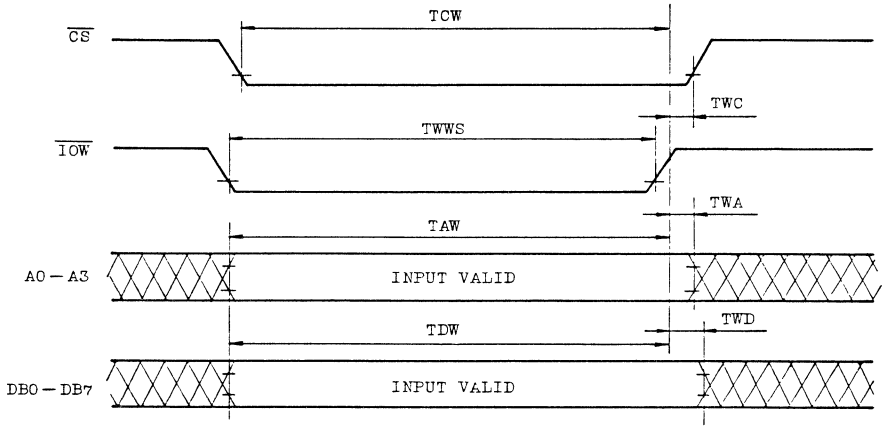
Program Condition (Idle Cycle) (Notes: 2, 8 and 9)
[Ta=0°C to 70°C, VCC=5V±5%, VSS=0V]

ABBR.	PARAMETER	MMIN.	MAX.	UNIT
TAR	ADR Stability or $\overline{CS}$ = 0 --> $\overline{READ}$ = 0	50		ns
TAW	ADR Stability --> $\overline{WRITE}$ = 1 set-up time	200		ns
TCW	$\overline{CS}$ = 0 --> $\overline{WRITE}$ = 1 set-up time	200		ns
TDW	Data stability -> $\overline{WRITE}$ = 1 set-up time	200		ns
TRA	$\overline{READ}$ = 1 --> ADR or $\overline{CS}$ hold time	0		ns
TRDE	$\overline{READ}$ = 0 --> Data stability (Note 7)		200	ns
TRDF	$\overline{READ}$ = 1 --> DB floating	20	100	ns
TRSTD	POWER ON --> Reset = 0 set-up time	500		ns
TRSTS	Reset --> First $\overline{IOWR}$ = 0	2TCY		ns
TRSTW	Reset pulse width	300		ns
TRW	$\overline{READ}$ pulse width	300		ns
TWA	$\overline{WRITE}$ = 1 --> ADR hold time	20		ns
TWC	$\overline{WRITE}$ = 1 --> $\overline{CS}$ = 1 hold time	20		ns
TWD	$\overline{WRITE}$ = 1 --> Data hold time	30		ns
TWWS	$\overline{WRITE}$ pulse width	200		ns
TAD	$\overline{CS}$ = 0, address stability --> Data stability access time		300	ns

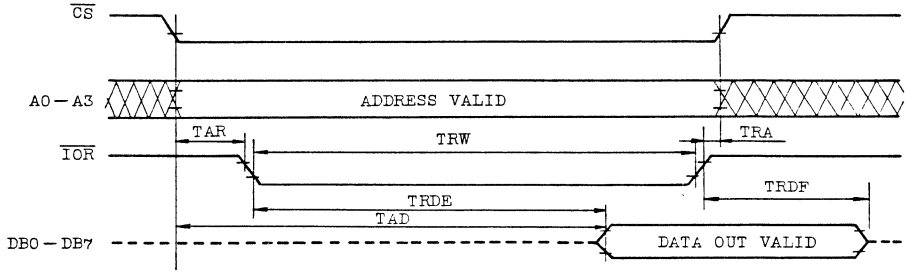
Capacity (Ta=25°C, VCC=GND=0V)

SYMNOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CO	Output Capacitance	fc = 1.0 MHz, Input = 0V			8	pF
CI	Input Capacitance				15	
CIO	I/O Capacitance				20	

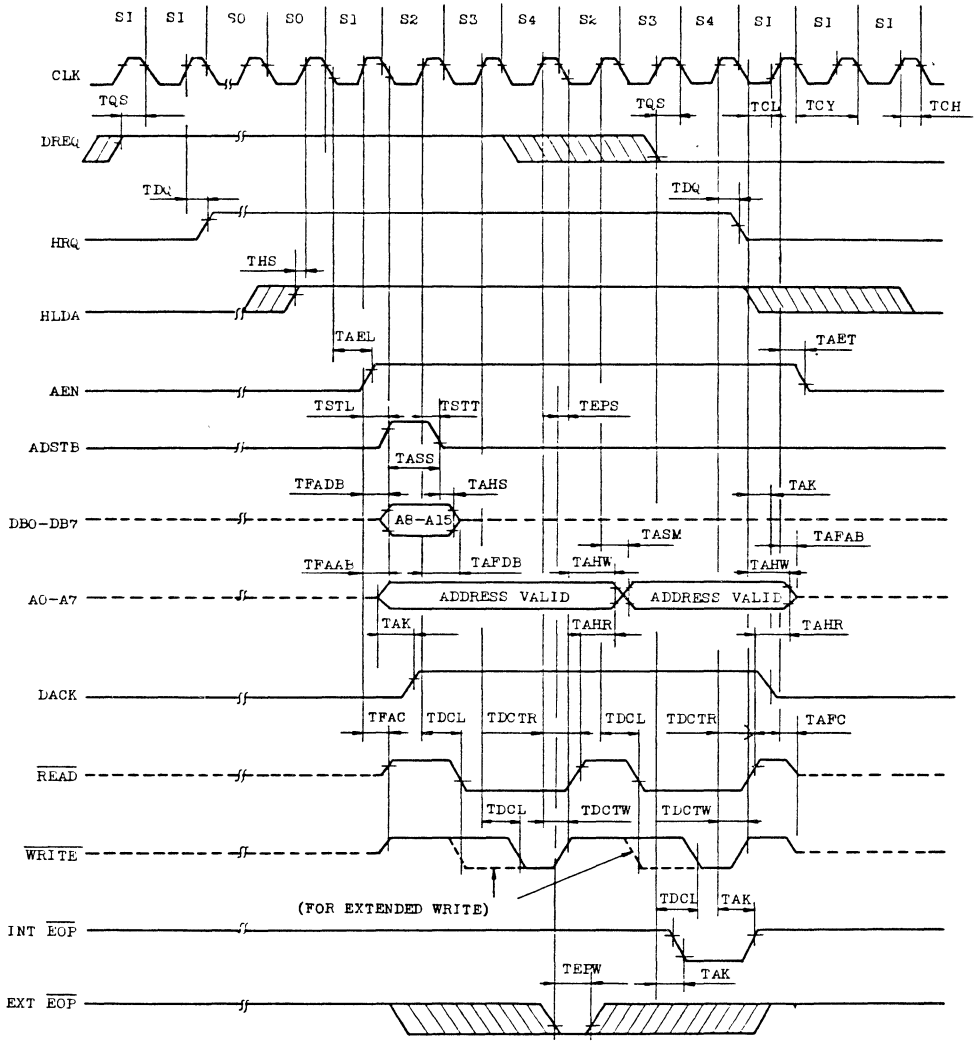
Timing Diagram



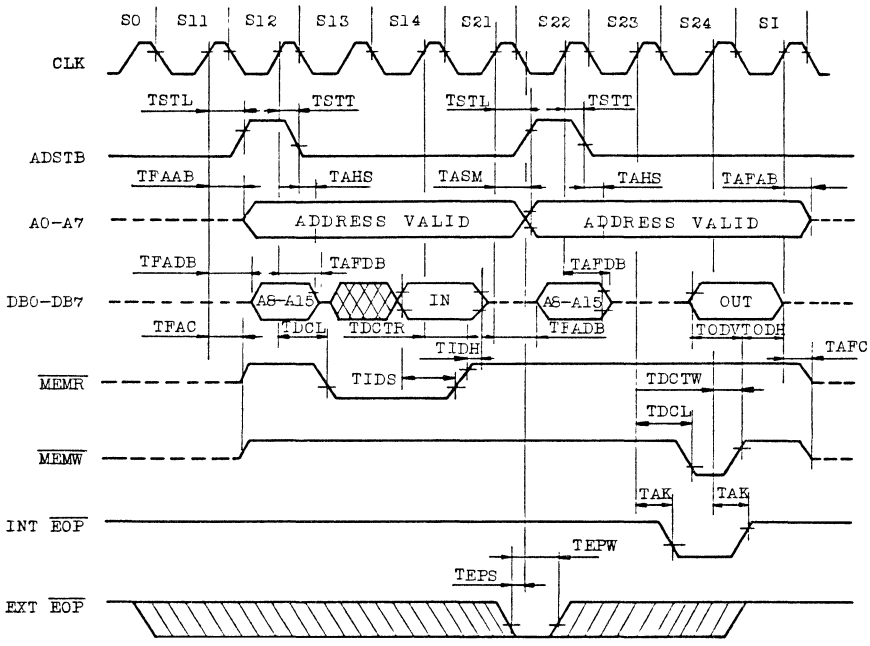
Timing Diagram 1 Program Condition Write Timing



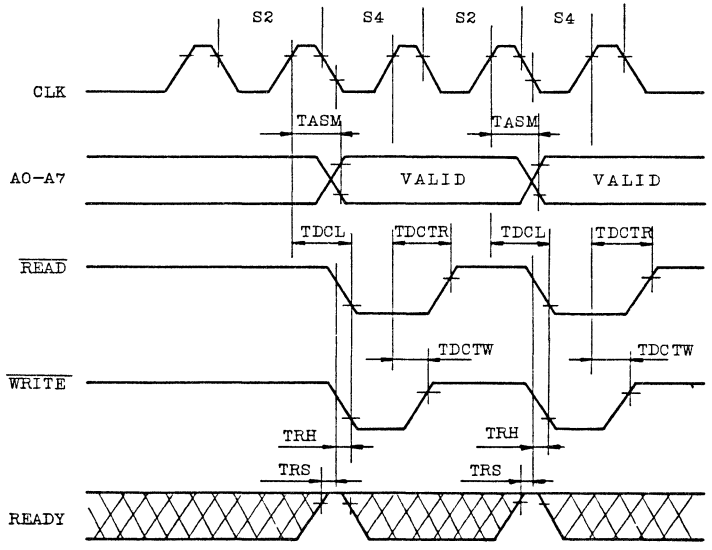
Timing Diagram 2 Program Condition Read Cycle



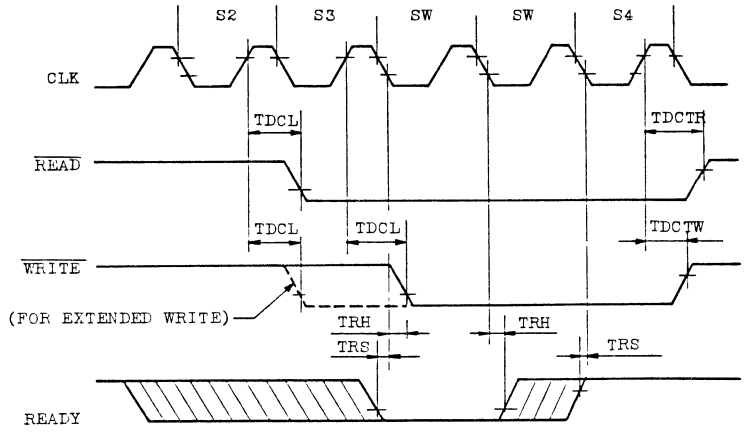
Tining Diagram 3 Active Cycle



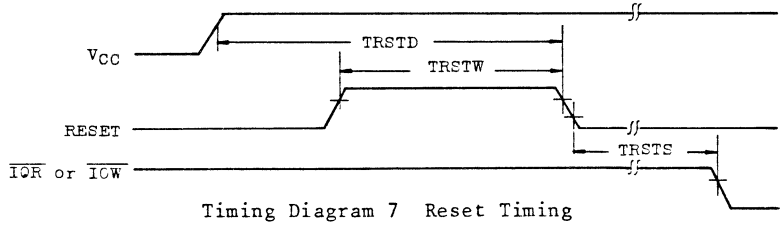
Timing Diagram 4 Memory-to-Memory Transfer



Timing Diagram 5 Short Timing of Transfer Time



Timing Diagram 6 Ready Timing



Timing Diagram 7 Reset Timing

Note 1. TYP value is that when rated voltage is applied at Ta = 25 °C.

Note 2. Test conditions; a) Unless otherwise specified, timing defining signal voltages are;
Input High level = 2.4V, Low level = 0.45V
Output High level = 2.0V, Low level = 0.8V
b) Input rising and falling times are below 20 ns.
c) Unless otherwise specified, 1 x TTL gate and 150 pF load are provided to output.

Note 3. Normal write pulse width is TCY-100 ns. Extension write pulse width is 2TCY-100 ns. Read pulse width is 2TCY-50 ns, and shorted read pulse width is TCY-50 ns.

Note 4. TDQ is measured at two different high levels.
TDQ1 = 2.0V, TDQ2 = 3.3V

Note 5. It is necessary to keep DREQ active until DACK is received.

Note 6. Both low active and high active level are available for DREQ and DACK.

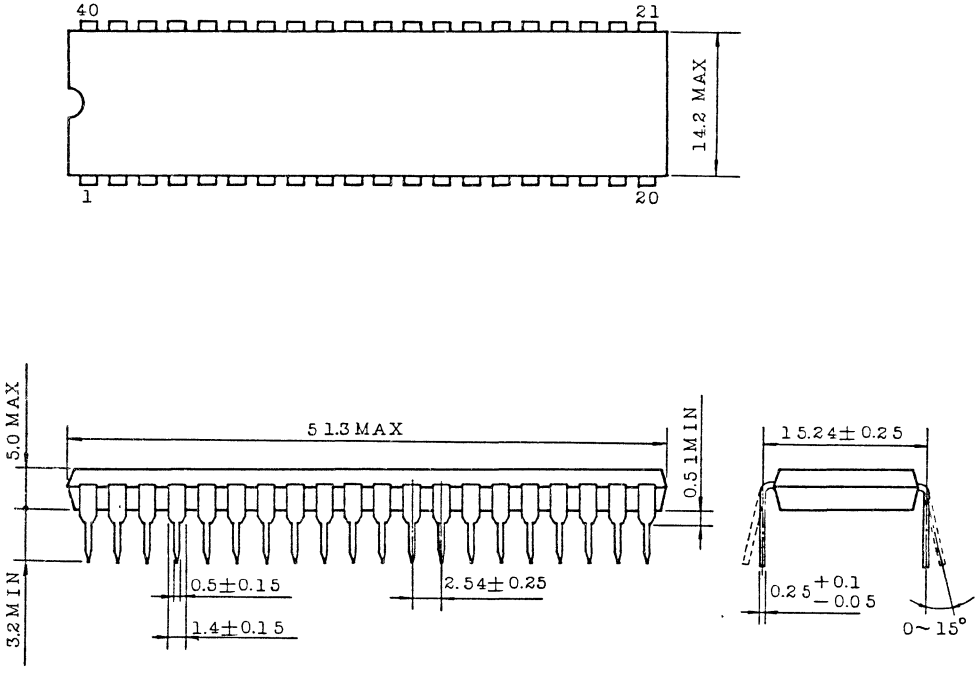
Note 7. Output load of the data bus are provided with 1 x TTL gate and 15 pF as the minimum value, and 1 x TTL gate and 150 pF as the maximum value.

Note 8. 600 ns are required for active read or write pulse recovery time at time of program condition.

Note 9. Signal $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$ are $\overline{\text{IOR}}$ and $\overline{\text{MEMR}}$ for the DMA operations from peripheral devices to the memory. In the DMA operations from memory to peripheral devices, they are $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$.

Note 10. When N state wait is added at time of write to memory in the latter half of memory-to-memory transfer, this parameter increases by N (TCY) at a time.

EXTERNAL DIMENSION VIEW (Plastic Package)



Note Each pitch is 2.54mm, and all the leads are located within +0.25mm from their theoretical positions with respect to No. 1 and No. 40 leads.

Example of Application Circuit

The connecting method of the TMP8237A and CPU is shown in Fig. 7

The multi-mode DMA controller outputs a hold request whenever valid DMA request is produced from peripheral device. When CPU answers by the hold acknowledge signal, the TMP8237A receives the control right of the address bus, data bus, and control bus. In the first transfer, address (low order 8 bits of the address bits and high order 8 bits on the data bus) is output.

The content of the data bus is latched by the 8-bit latch (TC74HC373P) to make the address bus complete. After execution of the first transfer, that latched data is updated only when carry or borrow is produced on the low order address byte.

When one TMP8237A is used, four DMA channels are provided.

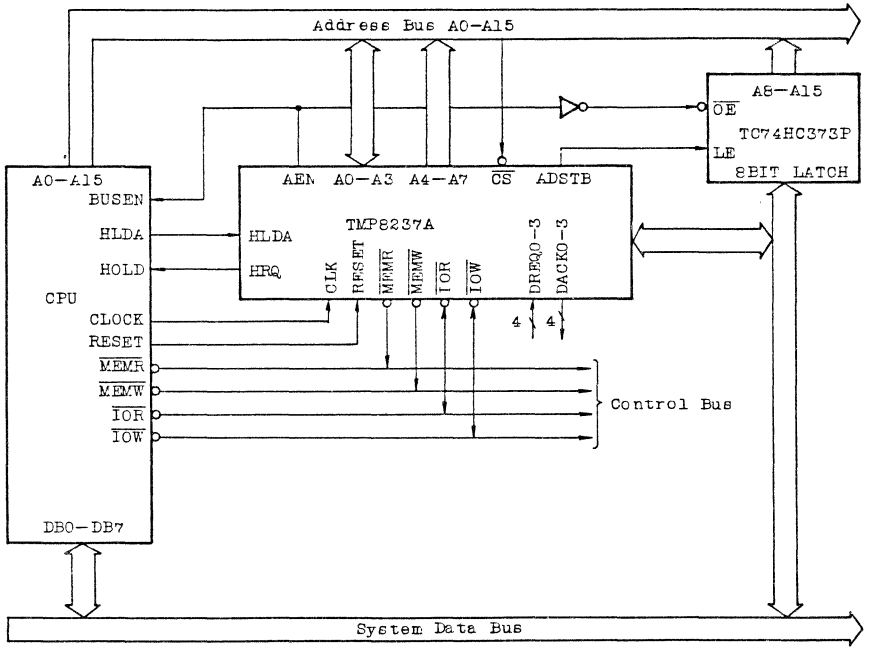


Fig. 7 Basic System Connection Diagram

Fig. 8 shows the extension method for number of DMA channels. It is possible to realize net 7 DMA channels by connecting the second TMP8237A to one of the DMA channels of the first TMP8237A.

Two DMA chips commonly use the same 8-bit latch. Thus, any channel is used for extension.

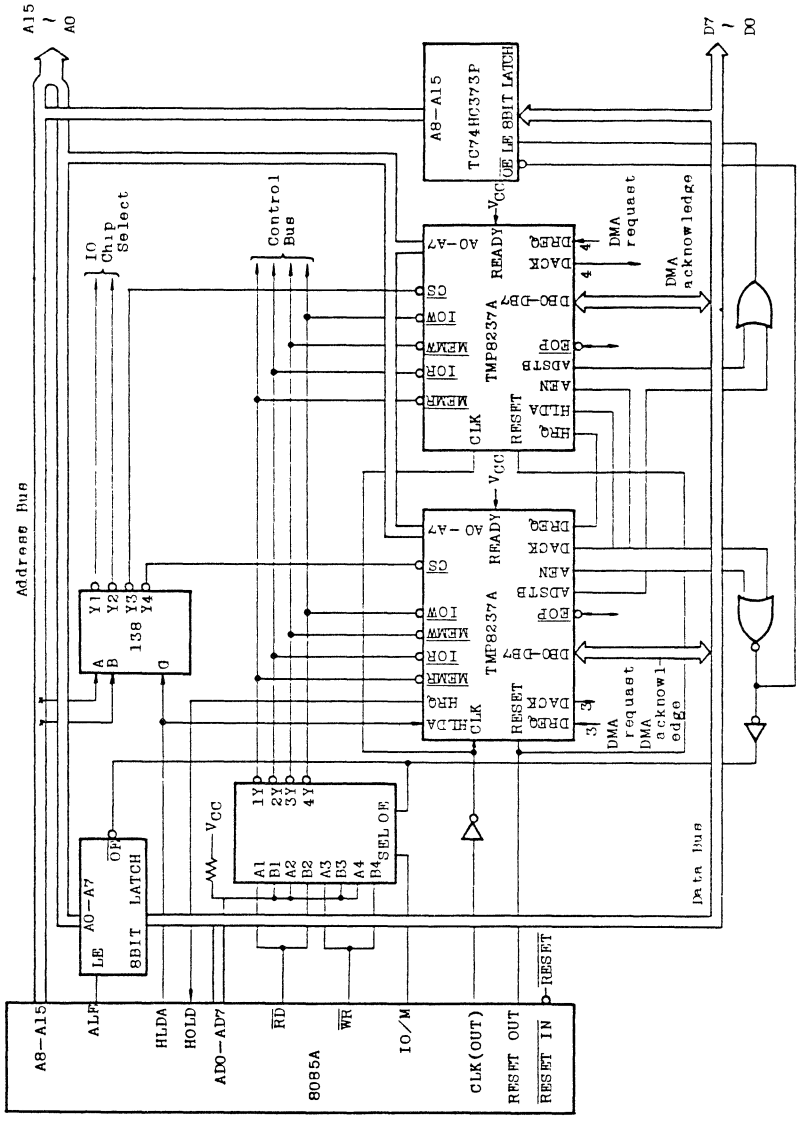


Fig. 8 Extension of TMP8237A

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT
TMP82C79P-2/TMP82C79F-2
SILICON MONOLITHIC CMOS SILICON GATE

PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

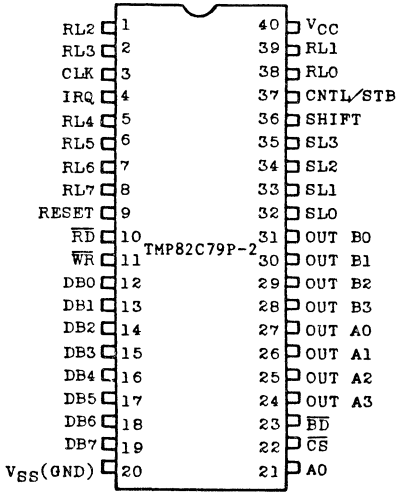
GENERAL DESCRIPTION

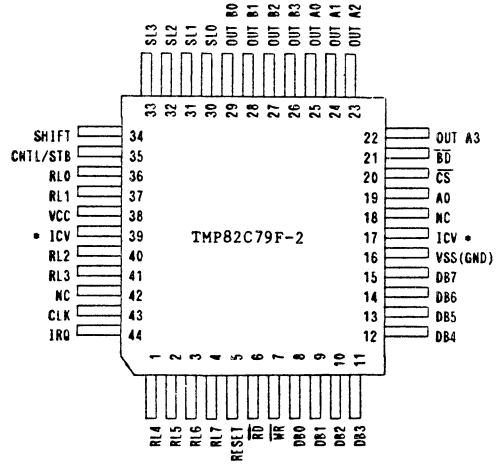
The TMP82C79P-2/F-2 (hereinafter referred to as TMP82C79) is a programmable keyboard/display interface chip. The keyboard portion can provide a scanned interface to a 64-contact key matrix. Also, the keyboard portion will interface to an array of sensors or a strobed interface keyboard. Key depressions can be 2-key lockout or N-key rollover. The display portion has 16 x 8 bits display RAM which can be organized into dual 16 x 4 bits. Both right entry and left entry display formats are possible.

FEATURES

- o Simultaneous Keyboard Display operation is possible.
- o Scanned Keyboard mode.
- o Scanned Sensor matrix mode.
- o Strobed Input Entry mode.
- o 8-Character FIFO is built in.
- o 2 Key Lockout or N-key Rollover with contact De-bounce is programmable.
- o 16 x 8 bit Display RAM is built in.
- o Scan timing is programmable.
- o Extend operating temperature $-40^{\circ}C$ to $+85^{\circ}C$.

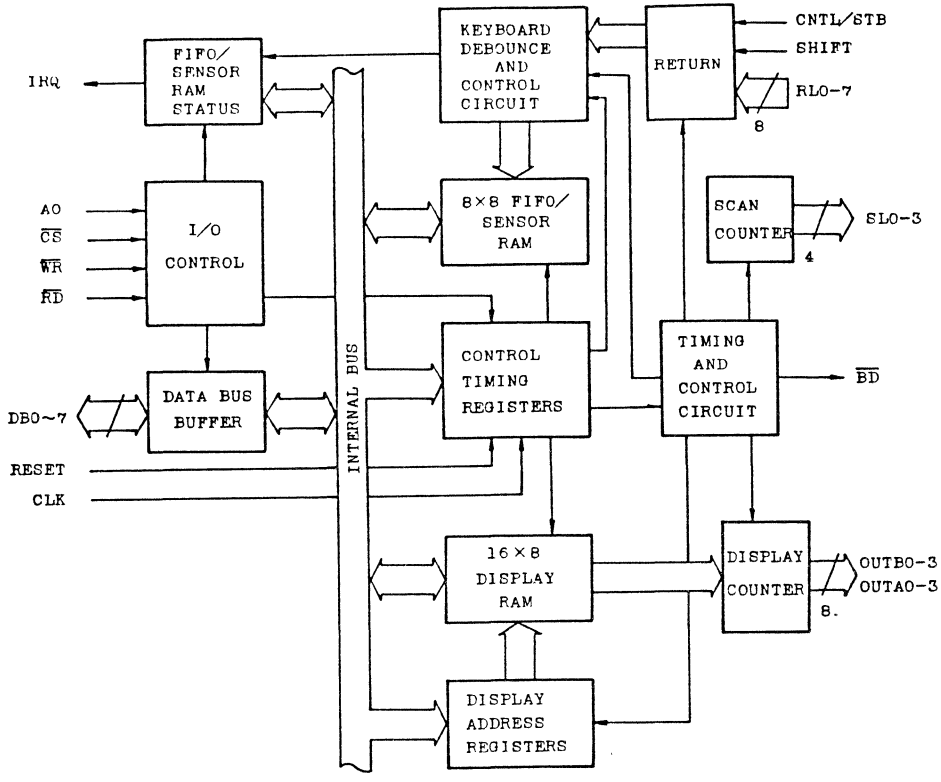
PIN CONNECTION





* Pin 17 and Pin 39 must be connected to Vcc or must be open.
NC: No connection

BLOCK DIAGRAM



PIN NAMES AND PIN DESCRIPTION

VSS (Power Supply)
Gound

VCC (Power Supply)
+5V during operation

DB0 - DB7 (Input/Output)
Bidirectional Data Bus. All data and commands are transferred via this data Bus.

CLK (Input)
CLOCK from system used to generate internal timing.

RESET (Input)
A high signal on this pin resets the TMP82C79. After being reset the TMP82C79 is placed in the following state.

(1) 16 x 8 bit character display, left entry.
(2) Encode scan keyboard, 2 key lockout, clock pre-scale value is set to 31H.

$\overline{CS}$ (Input)
A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the TMP82C79.

A0 (Input)
This input acts in conjunction with the $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ pins. a high on this pin indicates the signals on data bus are interpreted as command or status. A low indicates they are Data.

$\overline{WR}$ (Input)
A low on this pin when $\overline{CS}$ is low enables the TMP82C79 to accept command or data from the CPU.

$\overline{RD}$ (Input)
A low on this pin when $\overline{CS}$ is low enables the TMP82C79 to send data to data Bus.

IRQ (Output)
Interrupt request output. In a keyboard mode, the interrupt line is high when there is data in the FIFO/Sensor RAM. The interrupt line goes low with each FIFO/Sensor RAM read and returns high if there is still information in the RAM. In a sensor mode, interrupt line goes high whenever a change in a sensor is detected.

SL0 - SL3 (Output)
Scan lines which are used to scan the key switch or sensor matrix and the display digits. These lines can be either encoded (1 of 16) or decoded (1 of 4).

RL0 - RL7 (Input)
Return lines which are connected to the scan lines through the key or sensor switches. They have internal pullups to keep them high until a switch closure pulls one low. They also serve as an 8-bit input in the Strobed Input mode.

SHIFT (Input)
This input status is stored along with the key position on key closure in the Scanned key board modes. It has internal pullup to keep it high until a switch closure pulls it low.

CNTL/STB (Input)
For Keyboard modes this line is used as a control input and stored like status on a key closure. The line is also the strobe line that enters the data into FIFO in the Strobed Input mode (Rising Edge). It has an internal pullup to keep it high until a switch closure pulls it low.

OUTA0 - OUTA3 (Output)
OUTB0 - OUTB3 (Output)
These two ports are the outputs for the 16 x 4 display refresh registers. The data from these outputs is synchronized to the scan lines (SL0 - SL3) for multiplexed digit displays. The two 4 bit ports may be blanked independently. These two ports may also be considered as one 8-bit port.

$\overline{BD}$ (Output)
This output is used to blank the display during digit switching or by a display blanking command.

FUNCTIONAL DESCRIPTION
[BLOCK DESCRIPTION]

I/O Control and Data Bus Buffer

The I/O control section uses the $\overline{CS}$, $\overline{A0}$, $\overline{RD}$ and WR lines and controls the flow of data to and from various internal registers and buffers. $\overline{CS}$ input enables the all data flow to and from the TMP82C79. The character of the information given by the CPU, is identified by A0.

$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	Functions
0	0	0	1	Read Data
0	0	1	0	Write Data
0	1	0	1	Read Status word
0	1	1	0	Write Command word
1	X	X	X	High-impedance state

$\overline{RD}$ and $\overline{WR}$ decide the direction of data flow through the data bus buffer. The data bus buffer is bidirectional buffer which is used for connecting the internal bus and a system bus. When $\overline{CS}$ is high, the buffer is in a high impedance state.

Control Register, Timing Register and Timing Control Circuit

The keyboard and display modes and other operating conditions are programmed by the CPU. These modes are latched at the rising edge of $\overline{WR}$ when A0 is high. The timing control contains the basic counter chains. The first counter is the 1/N prescaler that can be programmed to yield an basic internal frequncy. In case of 100kHz basic internal frequency, it gives a 5.1 mS keyboard scan time and a 10.3 mS debounce time. The other counters divide down the basic internal frequency to provide the proper key scan, row scan, keyboard matrix scan and display scan times.

Scan Counter

Two modes are available for the scan counter. In the encode mode, the counter provides a binary count that must be externally decoded to provide the scan lines for the key board and display. In the decode mode, the scan counter decodes the least significant 2 bits internally and provides a decoded 1 of 4 scan. It is necessary to pay attention on the fact that only first 4 characters in the Display RAM are displayed.

Return Buffer and Keyboard Devounce Control circuit

The 8 return lines are latched by the return buffer. In the Keyboard mode, these lines are scanned to look for key closures in a row. If the debounce circuit detects a closed switch, it waits about 10 mS, and checks if the switch remains closed. If it does so, address of the switch in the matrix is transferred to the FIFO along with the status of SHIFT and CNTL lines.
In the scanned Sensor Matrix Modes, the contents of the return lines are directly transferred to the corresponding row of the sensor RAM (FIFO) each scan time.
In the Strobed Input Mode, the contents of the return lines are transferred to the FIFO on the rising edge of the CNTL/STB line pulse.

FIFO/Sensor RAM and FIFO/Senser RAM Status

The FIFO/Sensor RAM is a dual function RAM. In the keyboard mode or In the Strobe Input mode, this FIFO/Sensor RAM serves as a FIFO. The FIFO status shows whether the FIFO is empty or full and keeps track of the number of characters in the FIFO. In addition, there is a flag to show an error in the case where too many reads or writes is recognized. The FIFO status can be read at CS = RD = 0, A0 = 1. The FIFO status logic provides an IRQ signal when the FIFO is not empty. In the scanned sensor matrix mode, the memory serves as a sensor RAM. IRQ becomes high when a change in the sensor is detected.

Display Address Registers and Display RAM

The display address registers hold the address of the word currently being written or read by the CPU and the two 4 bit nibbles being displayed. The Display RAM stores data for display outputs. The read/write addresses are programmed by the CPU command. They also can be programmed to auto-increment after read or write. The Display RAM can be directry read out by the CPU after mode and address is set. The A and B nibbles of the Display RAM are outputted to the Display Outputs A and B synchronously with scan signals (SL0 - SL3). The A and B nibbles can be entered independently or as one word by the CPU command.

[COMMAND DESCRIPTION]

Keyboard/Display Mode Set

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	D	D	K	K	K

Display Mode

0 0	8 x 8 bit character display - Left entry
* 0 1	16 x 8 bit character display - Left entry
1 0	8 x 8 bit character display - Right entry
1 1	16 x 8 bit character display - Right entry

* Default after Reset

* 0 0 0	Encoded Scan Keyboard - 2-Key Lockout
0 0 1	Decoded Scan Keyboard - 2-Key Lockout
0 1 0	Encoded Scan Keyboard - N-Key Rollover
0 1 1	Decoded Scan Keyboard - N-Key Rollover
1 0 0	Encoded Scan Sensor Matrix
1 0 1	Decoded Scan Sensor Matrix
1 1 0	Strobed Input, Encoded Display Scan
1 1 1	Strobed Input, Decoded Display Scan

Program Clock

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	P	P	P	P	P

The TMP82C79 generates all timing and multiplexing signals by means of the internal prescaler. The prescaler generates internal reference clocks by dividing an external clock by a programmable value PPPPP. Any number of ranging from 2 to 31 can be set as a prescaler value. When this value is set to 0 or 1, it is interpreted to be 2. If the internal reference clock is set to 100 kHz, it is possible to obtain 5.1mS keyboard scan time and 10.3mS debounce time. The value PPPPP is set to 31 after reset, but cannot be changed by the Clear command.

Read FIFO/Sensor RAM

D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	AI	X	A	A	A	X=don't care

If this command is written, the subsequent data reads are set up for the FIFO/Sensor RAM. Auto-increment flag (AI) and the RAM address bits AAA are valid only in Senser Matrix Mode. The address bits AAA select one of the 8 rows of the Sensor RAM. If AI = 1, the RAM address is incremented after each successive read. The Auto-incremented flag does not affect the auto-increment of the Display RAM.

Read Display RAM

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	AI	A	A	A	A

If this command is written, the subsequent data reads are set up for the Display RAM. The address bits AAAA select one of the 16 rows of the Display RAM. If AI = 1, the address is incremented after each read or write to the Display RAM. Since the same counter is used for both reading and writing, this command sets the next read or write address and the sense of the Auto-increment for both operation.

Write Display RAM

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	AI	A	A	A	A

If this command is written, the subsequent data writes are set up for the Display RAM. Note that writing this command does not switch the source of the subsequent data reads. The address register of the Display RAM is same for read/write operations. The addressing and Auto-increment function are identical to those for the Read Dispaly RAM.

Display Write Inhibit/Blanking

D7	D6	D5	D4	D3	D2	D1	D0	
1	0	1	X	IWA	IWB	BLA	BLB	X=don't care

The IWA or IWB bit can be used to mask A nibble or B nibble for entering the Display data independently. The BLA or BLB flag is available for the nibble A or B to blank the display. In the case where the Display Outputs are used as separate 4-bit display ports, the IWA or IWB bit is useful so as not to affect the other display port when the CPU writes a word to the display RAM. The BLA or BLB bit is used for blanking the display independently without giving any affect to the other 4-bit display port. The blank code is determined by the last Clear command that has been programmed after reset. If the Display Output is used as an 8-bit port, it is necessary to set both BLA and BLB bits for blnaking the display. Then BD signal becomes low.

D7	D5	D5	D4	D3	D2	D1	D0
A3	A2	A1	A0	B3	B2	B1	B0

: Correspondence between Display Output and Data Bus

Clear

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	CD	CD	CD	CF	CA

The CD bits are used to clear all rows of the Display RAM to the following code shown below.

(D4) CD	(D3) CD	(D2) CD		
1	0	X	---	All Zeros (X = Don't Care)
1	1	0	---	All Hex 20H (0010 0000)
1	1	1	---	All Ones
0	X	X	---	not clear display if CA = 0
|				Enable clear display when CD = 1 (or by CA = 1)

While the Display RAM is being cleared, it may not write to the Display RAM. The MSB bit of the FIFO status word is set during this time. If the CF bit is set to "1", the FIFO status is cleared and the interrupt request output (IRQ) is reset. Also, the Senser RAM pointer is set to the row 0.

The CA bit has the combined effect of the CD bit and CF bit. It enables clear display code to the Display RAM and also clears the FIFO status. Furthermore, it re-synchronizes the internal timing chains.

END Interrupt/Error Mode Set

D7	D6	D5	D4	D3	D2	D1	D0	
1	1	1	E	X	X	X	X	X: don't care

In the Sensor Matrix mode, this command loweres the IRQ line and enables writing to the sensor RAM. This means that a write to the Sensor RAM is inhibited when IRQ line is high. If the E bit is set to "1", the S/E bit of the FIFO status becomes "1" when any one of the sensor switches is closed. If E = 0, the S/E bit is always "0". In the N-Key Rollover mode, if the E bit is programmed to "1", the Special Error mode will be resulted.

FIFO status

D7	D6	D5	D4	D3	D2	D1	D0	
Du	S/E	O	U	F	N	N	N	X: don't care

Number of characters in FIFO
FIFO Full
Error-Underrun
Error-Overrun
Sensor Closure/Error Flag for Multiple Closures
Display unavailable

Du : indicates that the Display RAM was unavailable because a Clear Display or Clear All command has not completed its clearing operation.

S/E : In a Sensor Matrix mode, if the E bit of END Interrupt/Error Mode Set is programmed to "0", this S/E bit is set to indicate that at least one sensor closure indication is contained in the Sensor RAM.
In Special Error Mode, this S/E bit is showing the error flag and serves as an indication to whether a simultaneous multiple closure error has occurred.

O : indicates that the entry of another character into a full FIFO was attempted.

U : indicates that the CPU tried to read an empty FIFO.

F : indicates that the FIFO is full of the eight characters.

NNN : indicates number of characters in the FIFO when in the Keyboard Mode or in the Strobe Input Mode.

[INTERFACE WITH KEYBOARD]

Scanned Keyboard, 2-key LOCKOUT

In this mode, if one key only is kept depressed during one debounce cycle (2 times of the key scan cycle), the key is recognized. When a key is depressed, the debounce logic is set and the other depressed keys are checked during the next two scan cycle. If none are encountered, it is a single key depression and the key position is entered into the FIFO along with the status of CNTL and SHIFT lines. If another depressed key are encountered, operates as follows.

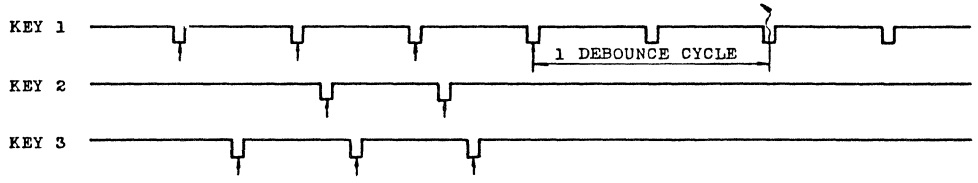


Fig. 1 Example of a case where a first depressed key is continuously kept to the last

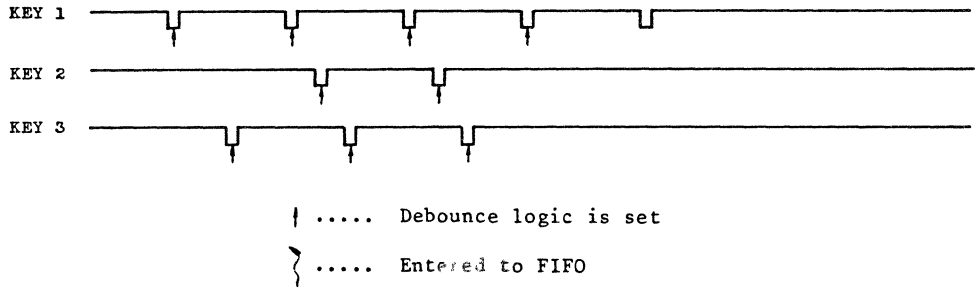


Fig. 2 Example of a case where all depressed keys are ignored

As shown in Fig. 1, if all other keys are released before the first depressed key, the first depressed key is recognized. As shown in Fig. 2, if the first depressed key is released within one debounce cycle after the other keys was released, then all keys are ignored.

Scanned Keyboard, N-key Rollover

In this mode, each key depression is independently treated from all others. In the 2-key lockout mode, if a key is depressed, the debounce logic is set. If other keys are depressed within one debounce cycle after it, the debounce logic is set again. The first depressed key is ignored. In the N-key Rollover mode, if a key is depressed waits one debounce cycle and then checks if the key is still down. If it is, the key is entered into the FIFO even if other keys are depressed.

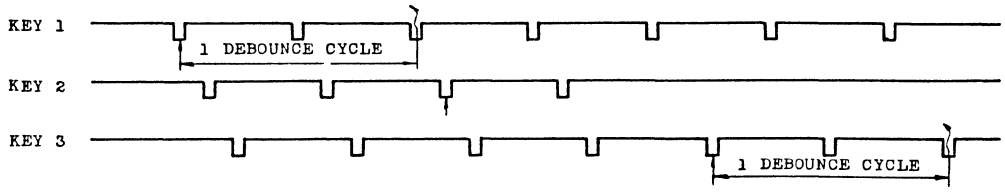


Fig. 3 Example of 3 keys being pushed simultaneously

In the example as shown in Fig. 3, the debounce circuit starts by Key 1, and checks if the key is still down after one debounce cycle. If it is, Key 1 is recognized and Key 2 is ignored not to be depressed for one debounce cycle.

Special Error Mode (N - Key Rollover)

This mode is set if the E bit of the End interrupt/error Mode Set command is programmed to "1". In the normal N-Key Rollover Mode, the key information is entered to the FIFO according to the key scan timing even if a simultaneous multiple depressin occures during one debounce cycle. In the Special Error Mode, if a simultaneous multiple depression occurs during one debounce cycle, sets the error flag (the S/E bit of the FIFO status word) to "1". This flag prevents any further writing into the FIFO and will set interrupt request (IRQ). The S/E bit is cleared if the normal Clear command is written with CF = 1.

Sensor Matrix Mode

In Sensor Matrix Mode, the debounce circuit does not operate. The status of the sensor switch is inputted directly to the Sensor RAM. The CPU can only know a validated closure in the keyboard mode, however this mode has such advantage that the CPU knows how long the senror was closed and when it was released. If there is any change in the sensor value at the end of the sensor matrix scan, the IRQ line goes high. The IRQ line is cleared by the first data read if the Auto-increment flag is "0" or by the End Interrupt/Error Mode Set command if AI = 1.

Strobe Input Mode

In Strobe Input Mode, the debounce circuit does not operate. The data is inputted into the FIFO from the return lines at the rising edge of CNTL/STB Signal. When the data is entered into the FIFO, the IRQ line goes high. The functions of the FIFO and the FIFO status in this mode are same as those in the keyboard mode.

[DATA FORMAT]

Keyborad Mode

D7	D6	D5	D4	D3	D2	D1	D0
CNTL	SHIFT	SCAN			RETURN		

In this mode, the Data Format of the character entered into the FIFO is as follows. The MSB is the status of CNTL/STB line and the next MSB shows the status of SHIFT line. The next three bits are from the scan counter and indicate the row the key was found in. The last three bits are from the column counter and indicate to which return line the key was connected.

Sensor Matrix Mode

D7	D6	D5	D4	D3	D2	D1	D0
RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0

In this mode, the data on return lines is inputted in the row of the Sensor RAM in order according to the scan. The data is entered even if there is no change in the status of the sensor matrix switches. Each switch position maps to a Sensor RAM position. CNTL and SHIFT signals are ignored.

Strobe Input Mode

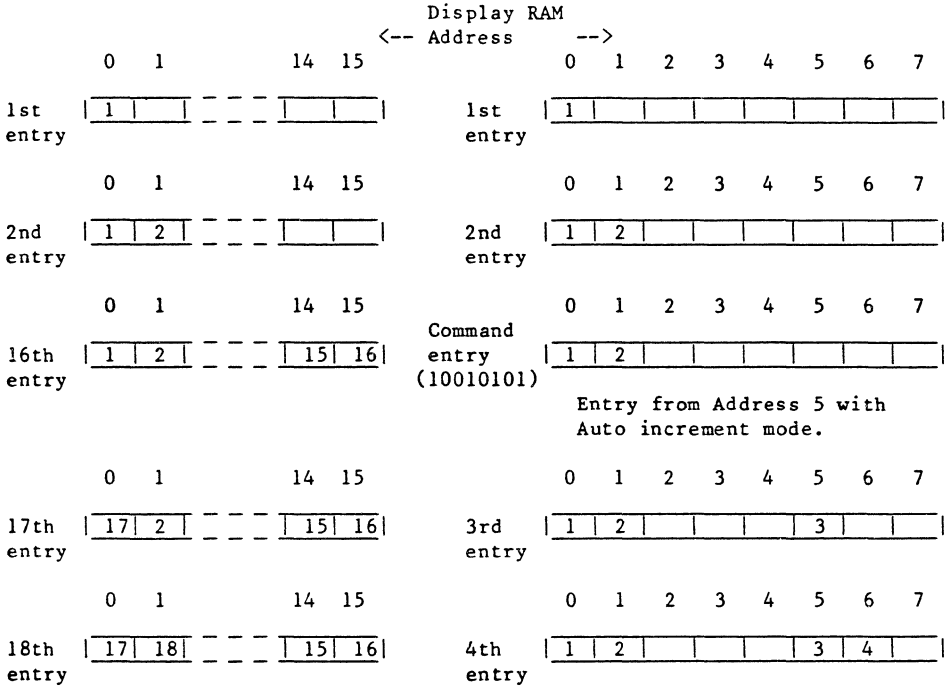
D7	D6	D5	D4	D3	D2	D1	D0
RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0

In this mode, the data on return lines is entered into the FIFO at the rising edge of CNTL/STB signal.

[INTERFACE WITH DISPLAY]

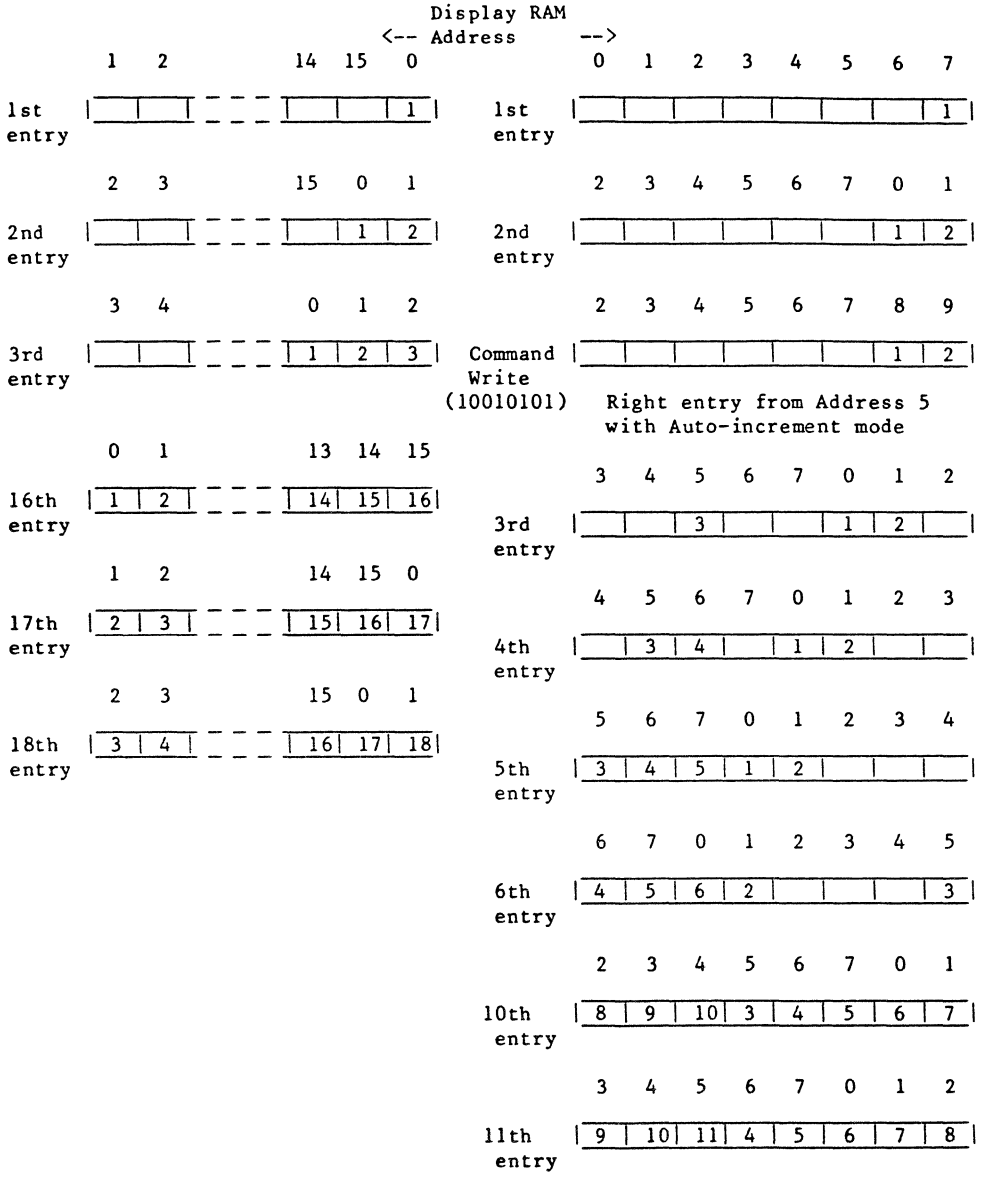
Left Entry

In Left Entry mode, address 0 of the Display RAM is the left-most side of the display and address 15 (address 7 in the case of 8-character display) is the right-most side. when characters are inputted on to the display RAM with the auto increment mode from address 0 of the display RAM, Characters are filled from the left-most position of the display. The 17th (or 9th) character is placed in the left-most position again. Address of the display RAM corresponds directly to each display positon of the display, and so its position does not change every entry.



Right Entry

In Right Entry, the first entry is from the right-most position. Address of the Display RAM does not correspond to the display position.


Display RAM
<-- Address
-->
1st entry
2nd entry
3rd entry
16th entry
17th entry
18th entry
Command Write (10010101)
Right entry from Address 5 with Auto-increment mode
3rd entry
4th entry
5th entry
6th entry
10th entry
11th entry

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
VCC	VCC Supply Voltage (with respect to VSS(GND)	-0.5V to +7.0V
VIN	Input Voltage (with respect to VSS (GND)	-0.5V to VCC +0.5V
VOUT	Output Voltage (with respect to VSS (GND)	-0.5V to VCC +0.5V
PD	Power Dissipation	250 mW
Tsol	Soldering Temperature(soldering time 10 sec)	260°C
Tstg	Storage Temperature	-65°C to +150°C
Topr	Operating Temperature	-40°C to +85°C

D.C. ELECTRICAL CHARACTERISTICS (Ta=-40 to +85°C, VCC=VSS (GND)=0V)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
VIL1	Input Low Voltage (RL0 - RL7)		-0.5		1.4	V
VIL2	Input Low Voltage (Others)		-0.5		0.8	V
VIH1	Input High Voltage (RL0 - RL7)		2.2		VCC+0.5	V
VIH2	Input High Voltage (Others)		2.2		VCC+0.5	V
VOL	Output Low Voltage	IOL=2.2mA			0.45	V
VOH1	Output High Voltage	IOH=-400uA	2.4			V
VOH2	Output High Voltage	IOH=-100uA	VCC -0.8			V
IIL1	Input lLeak Current (SHIFT, CNTL, RL0 - RL7)	VIN=VCC			+10	uA
		VIN=2.4V	-10	-30		
		VIN=0V			-100	
IIL2	Input Leak Current (Others)	0V<VIN<VCC			±10	uA
IOFL	Output Leak Current	0.45<VOUT =<VCC			±10	uA
ICC	Supply Current Operating Supply Current	VIH=VCC-0.2 V,VIL=0.2V fc=5MHz			5	mA

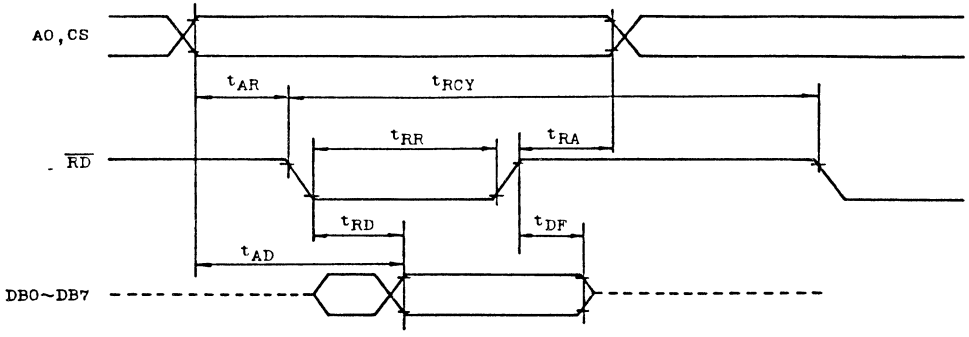
INPUT CAPACITY

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
CIN	Input Capcity	fc=1MHz Unmeasured Pins returned to VSS.		5	10	pF
COUT	Output Capacity			10	20	pF

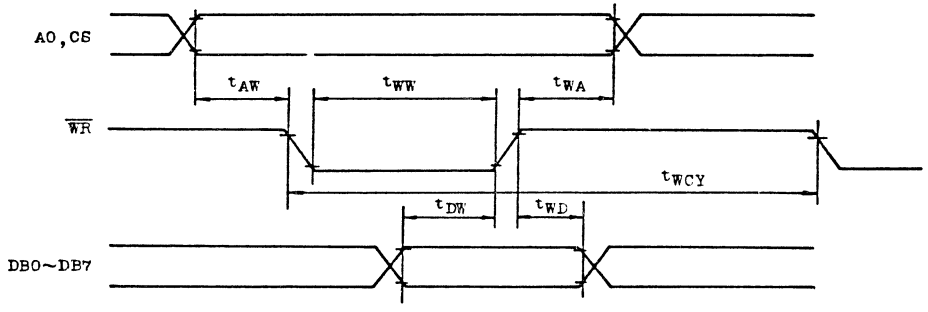
A.C. ELECTTRICAL CHARACTERISTICS (Ta=-40 to +85°C, VCC=5.0V±10%, VSS(GND)=0V)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
tAR	Address Set up Time ($\overline{RD}$)	10			ns
tRA	Address Hold Time ($\overline{RD}$)	10			ns
tRR	RD Pulse Width	160			ns
*tRD	Valid Data ($\overline{RD}$)			120	ns
*tAD	Address to Valid Data			185	ns
tDF	Data Floating ($\overline{RD}$)	10		85	ns
tRCY	Read cycle Time	200			us
tAW	Address Set up Time ($\overline{WR}$)	0			ns
tWA	Address Hold Time ($\overline{WR}$)	0			ns
tWW	WR Pulse Width	140			ns
tDW	Data Set up Time ($\overline{WR}$)	120			ns
tWD	Data Hold Time ($\overline{WR}$)	10			ns
tWCY	Write Cycle Time	200			ns
toWH	CLK Pulse Width of High Level	80			ns
toWL	CLK Pulse Width of Low Level	50			ns
tCY	Clock Period	200			ns

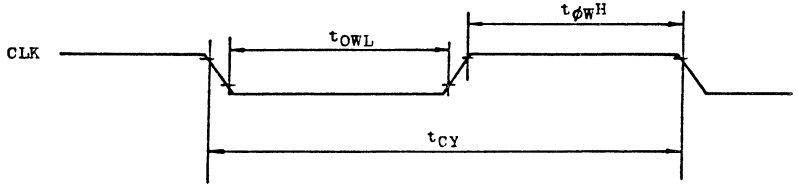
* TEST CONDITION CL = 150pF



Read-operation



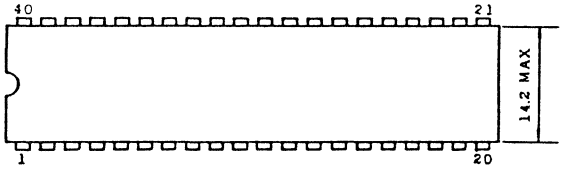
Write-operation

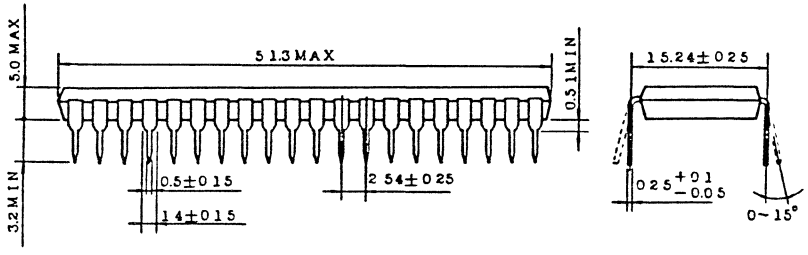


Clock input

OUTLINE DRAWING (40Pins Plastic Package)

Unit in mm

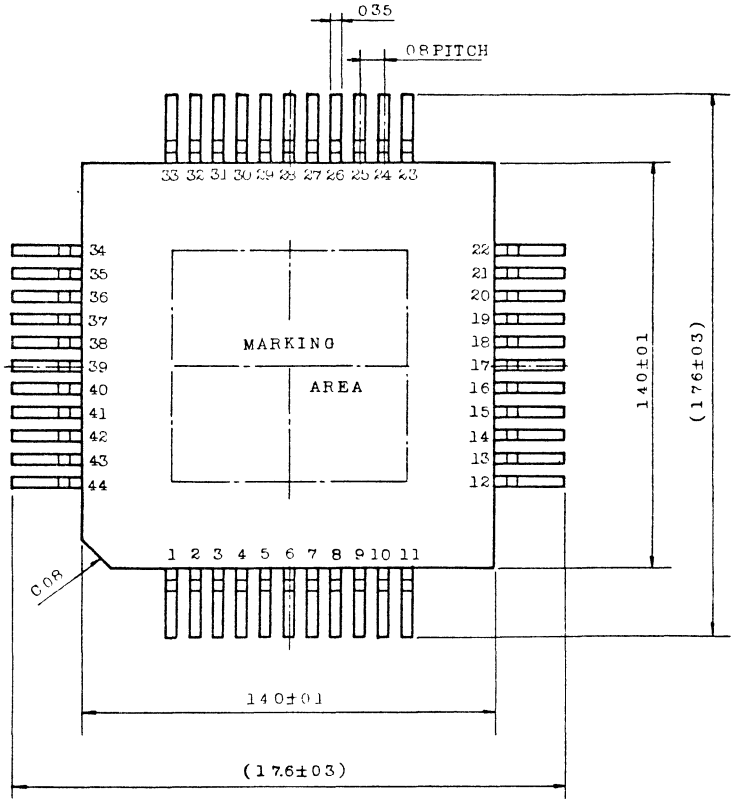


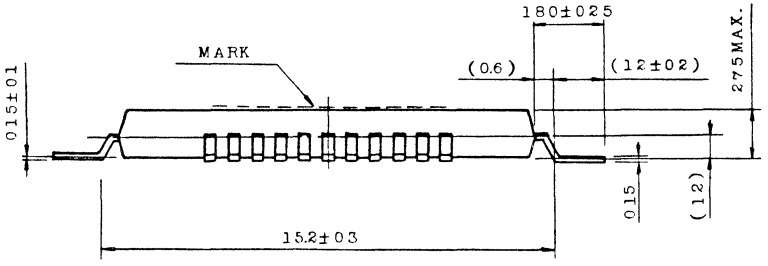


Note Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoritical positions with respect to No.1 and No.40 leads.

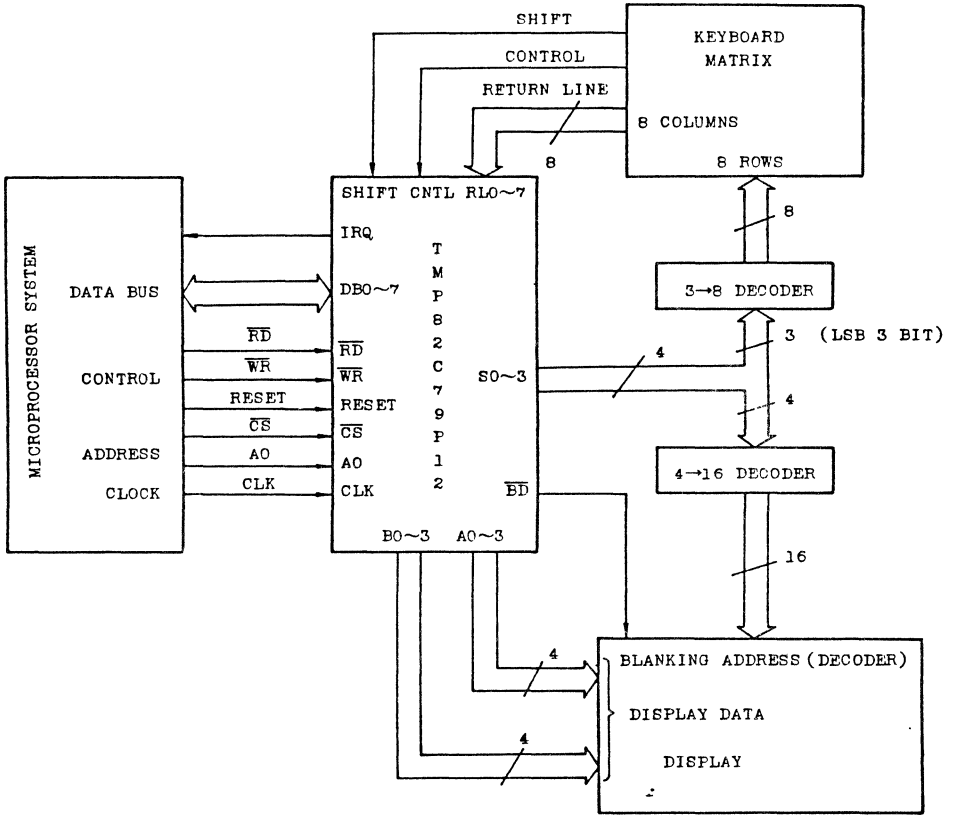
OUTLINE DRAWING (44Pins Mini Flat Package)

Unit in mm





EXAMPLE OF APPLICATION CIRCUIT



PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

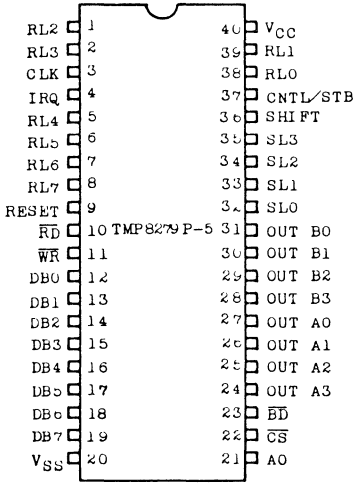
GENERAL DESCRIPTION

The TMP8279-5 is a progammable keyboard/display interface chip designed for use as the TLCS-85A microcomputer peripheral. The keyboard portion can provide a scanned interface to a 64-contact key matrix. Also, the keyboard portion will interface to an array of sensors or a strobed interface keyboard. Key depressions can be 2-key lockout or N-key rollover. The display portion has 16 × 8 bits display RAM which can be organized into dual 16 × 4 bits. Both right entry and left entry display formats are possible.

FEATURES

- Sumulataneous Keyboard Display operation is possible.
- Scanned Keyboard mode.
- Scanned Sensor Matrix mode.
- Strobed Input Entry mode.
- 8-Character FIFO is built in.
- 2 Key Lockout or N-key Rollover with contact De-bounce is programmable.
- 16 × 8 bit Display RAM is built in.
- Scan timing is programmable.
- Compatible with INTEL 8279-5.

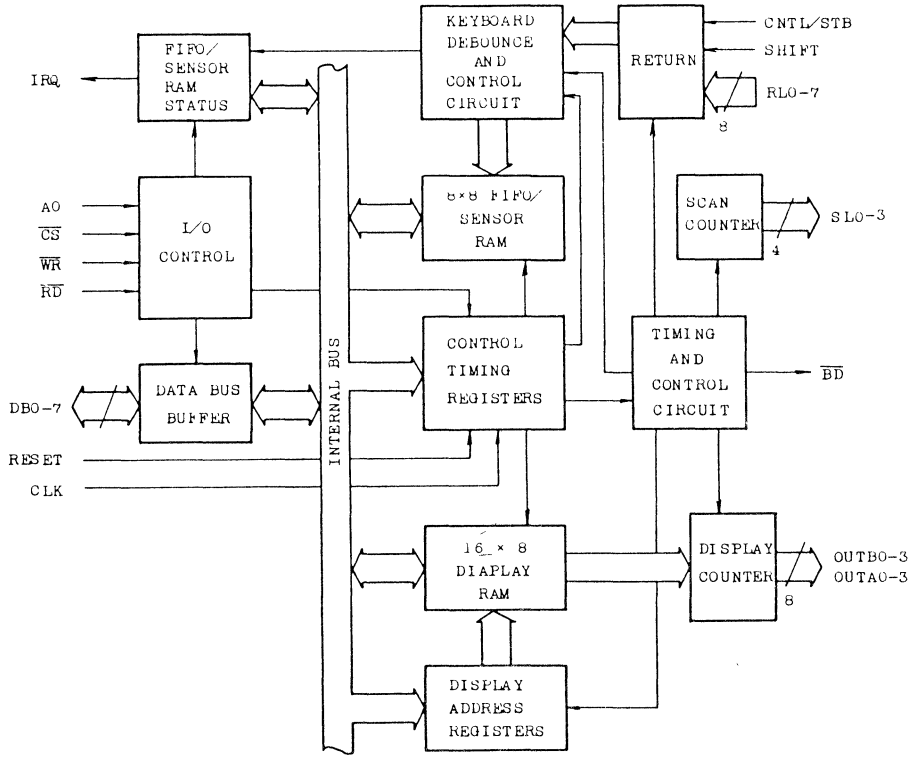
PIN CONNECTION



PIN NAME

DB0 - DB7	8-bit Bidirectional data bus
CLK	Clock input
RESET	Reset input
$\overline{CS}$	Chip select input
$\overline{RD}$	Read input
$\overline{WR}$	Write input
A0	Command/data control input
IRQ	Interrupt request output
SL0 - SL3	Scan lines
RL0 - RL7	Return lines
SHIFT	Shift input
CNTL/STB	Control/strobe input
OUTA0 - A3	Display (A) outputs
OUTB0 - B3	Display (B) outputs
$\overline{BD}$	Blanking display output
V_{CC}	+5V
V_{SS}	Ground

BLOCK DIAGRAM



PIN NAMES AND PIN DESCRIPTION

V_{SS} (Power Supply)

Ground

V_{CC} (Power Supply)

+5V during operation

DB_0 - DB_7 (Input/Output)

Bidirectional Data Bus. All data and commands are transfered via this data Bus.

CLK (Input)

CLOCK from system used to generate internal timing.

RESET (Input)

A high signal on this pin resets the TMP8279 . After being reset the TMP8279 is placed in the following state.

(1) 16 × 8 bit character display, left entry.
(2) Encode scan keyboard, 2 key lockout, clock pre-scale value is set to 31H.

$\overline{CS}$ (Input)

A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the TMP8279-5.

A0 (Input)

This inputs acts in conjunction with the $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ pins. A high on this pin indicates the signals on data bus are interpreted as command or status. A low indicates they are Data.

$\overline{WR}$ (Input)

A low on this pin when $\overline{CS}$ is low enables the TMP8279 to accept command or data from the CPU.

$\overline{RD}$ (Input)

A low on this pin when $\overline{CS}$ is low enables the TMP8279 to send data to data Bus.

IRQ (Output)

Interrupt request output.. In a keyboard mode, the interrupt line is high when there is data in the FIFO/Sensor RAM. The interrupt line goes low with each FIFO/Sensor RAM read and returns high if there is still information in the RAM. In a sensor mode, the interrupt line goes high whenever a change in a sensor is detected.

SL_0 - SL_3 (Output)

Scan lines which are used to scan the key switch or sensor matrix and the display digits. These lines can be either encoded (1 of 16) or decoded (1 of 4).

RL_0 - RL_7 (Input)

Return lines which are connected to the scan lines through the keys or sensor switches. They have internal pullups to keep them high until a switch closure pulls one low. They also serve as an 8-bit input in the Strobed Input mode.

SHIFT (Input)

This input status is stored along with the key position on key closure in the Scanned key board modes. It has a internal pullup to keep it high until a switch closure pulls it low.

CNTL/STB (Input)

For Keyboard modes this line is used as a control input and stored like status on a key closure. The line is also the strobe line that enters the data into FIFO in the Strobed Input mode (Rising Edge). It has an internal pullup to keep it high until a switch closure pulls it low.

$OUTA_0$ - $OUTA_3$ (Output)

$OUTB_0$ - $OUTB_3$ (Output)

These two ports are the outputs for the 16 × 4 display refresh registers. The data from these outputs is synchronized to the scan lines (SL_0 - SL_3) for multiplexed digit displays. The two 4 bit ports may be blanked independently. These two ports may also be considered as one 8-bit port.

$\overline{BD}$ (Output)

This output is used to blank the display during digit switching or by a display blanking command.

FUNCTIONAL DESCRIPTION
[BLOCK DESCRIPTION]

I/O Control and Data Bus Buffer

The I/O control section uses the $\overline{CS}$, A0, $\overline{RD}$ and $\overline{WR}$ lines and controls the flow of data to and from various internal registers and buffers. $\overline{CS}$ input enables the all data flow to and from the TMP8279. The character of the information given by the CPU, is identified by A_0. $\overline{RD}$ and $\overline{WR}$ decide the direction of data flow through the data bus buffer. The data bus buffer is bidirectional buffer which is used for connecting the internal bus and a system bus. When $\overline{CS}$ is high, the buffer is in a high impedance state.

$\overline{CS}$	A_0	$\overline{RD}$	$\overline{WR}$	Functions
0	0	0	1	Read Data
0	0	1	0	Write Data
0	1	0	1	Read Status word
0	1	1	0	Write Command word
1	X	X	X	High-impedance state

Control Register, Timing Register and Timing Control Circuit

The keyboard and display modes or other operating conditions are programmed by the CPU. These modes are latched at the rising edge of $\overline{WR}$ when A_0 is high. The timing control contains the basic counter chains. The first counter is the 1/N prescaler that can be programmed to yield an basic internal frequency which gives a 5.1 mS keyboard scan time and a 10.3 mS debounce time. The other counters divide down the basic internal frequency to provide the proper keyboard matrix scan and display scan times.

Scan Counter

Two modes are available for the scan counter. In the encode mode, the counter provides a binary count that must be externally decoded to provide the scan lines for the key board and display. In the decode mode, the scan counter decodes the least significant 2 bits internally and provides a decoded 1 of 4 scan. It is necessary to pay attention on the fact that only first 4 characters in the Display RAM are displayed.

Return Buffer and Keyboard Devounce Control circuit

The 8 return lines are latched by the return buffer. In the Keyboard mode, these lines are scanned to look for key closures in a row. If the debounce circuit detects a closed switch, it waits about 10 mS, and checks if the switch remains closed. If it does so, address of the switch in the matrix is transferred to the FIFO along with the status of SHIFT and CNTL lines.

FIFO/Sensor RAM and FIFO/Senser RAM Status

The FIFO/Sensor RAM is a dual function RAM. In the keyboard mode or In the Strobe lnput mode, this FIFO/Sensor RAM serves as a FIFO. The FIFO status shows whether the FIFO is empty or full and keeps track of the number of characters in the FIFO. In addition, there is a flag to show an error in the case where too many reads or writes is recognized. The FIFO status can be read at $\overline{CS} = \overline{RD} = 0$, $A_0 = 1$. The FIFO status logic provides an IRQ signal when the FIFO is not empty. In the scanned sensor matrix mode, the memory serves as a sensor RAM. IRQ becomes high when a change in the sensor is detected.

Display Address Registers and Display RAM

The display address registers hold the address of the word currently being written or read by the CPU and the two 4 bit nibbles being displayed. The Display RAM stores data for display outputs. The read/write addresses are programmed by the CPU command. They also can be programmed to auto-increment after read or write. The Display RAM can be directry read out by the CPU after mode and address is set. The A and B nibbles of the Display RAM are outputted to the Display Outputs A and B syncronously with scan signals (SL_0 - SL_3). The A and B nibbles can be entered independently or as one word by the CPU command.

[COMMAND DESCRIPTION]

Keyboard/Display Mode Set

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	D	D	K	K	K

Display Mode

	0	0	8 × 8 bit character display - Left entry
*	0	1	16 × 8 bit character display - Left entry
	1	0	8 × 8 bit character display - Right entry
	1	1	16 × 8 bit character display - Right entry

* Default after reset.

Keyboard Mode

*	0	0	0	Encoded Scan Keyboard - 2-Key Lockout
	0	0	1	Decoded Scan Keyboard - 2-Key Lockout
	0	1	0	Encoded Scan Keyboard - N-Key Rollover
	0	1	1	Decoded Scan Keyboard - N-Key Rollover
	1	0	0	Encoded Scan Sensor Matrix
	1	0	1	Decoded Scan Sensor Matrix
	1	1	0	Strobed Input, Encoded Display Scan
	1	1	1	Strobed Input, Decoded Display Scan

Program Clock

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	P	P	P	P	P

The TMP8279 generates all timing and multiplexing signals by means of the internal prescaler. The prescaler generates internal reference clocks by dividing an external clock by a programmable value PPPPP. Any number of ranging from 2 to 31 can be set as a prescaler value. When this value is set to 0 or 1, it is interpreted to be 2. If the internal reference clock is set to 100kHz, it is possible to obtain 5.1mS keyboard scan time and 10.3mS debounce time. The value PPPPP is set to 31 after reset, but cannot be changed by the Clear command.

Read FIFO/Sensor RAM

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	AI	X	A	A	A

X=don't care

If this command is written, the subsequent data reads are set up for the FIFO/Senser RAM. Auto-increment flag (AI) and the RAM address bits AAA are valid only in Senser Matrix Mode. The address bits AAA select one of the 8 rows of the Sensor RAM. If AI = 1, the RAM address is incremented after each successive read. The Auto-incremented flag does not affect the auto-increment of the Display RAM.

Read Display RAM

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	AI	A	A	A	A

If this command is written, the subsequent data reads are set up for the Display RAM. The address bits AAAA select one of the 16 rows of the Display RAM. If AI = 1, the address is incremented after each read or write to the Display RAM. This command sets the next read or write address and the sense of the Auto-increment.

Write Display RAM

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	AI	A	A	A	A

If this command is written, the subsequent data writes are set up for the Display RAM. Note that writing this command does not switch the source of the subsequent data reads. The address register of the Display RAM is same for read/write operations. The addressing and Auto-increment function are identical to those for the Read Display RAM.

Display Write Inhibit/Blanking

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	X	IWA	IWB	BLA	BLB

X=don't care

The IWA or IWB bit can be used to mask A nibble or B nibble for entering the Display data independently. The BLA or BLB flag is available for the nibble A or B to blank the display. In the case where the Display Outputs are used as separate 4-bit display ports, the IWA or IWB bit is useful so as not to affect the other display port when the CPU writes a word to the Display RAM. The BLA or BLB bit is used for blanking the display independently without giving any affect to the other 4-bit display port. The blank code is determined by the last Clear command that has been programmed after reset. If the Display Output is used as an 8-bit port, it is necessary to set both BLA and BLB bits for blanking the display. Then $\overline{BD}$ signal becomes low.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
↕	↕	↕	↕	↕	↕	↕	↕
A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0

: Correspondence between Display Output and Data Bus

Clear

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	C_D	C_D	C_D	C_F	C_A

The C_D bits are used to clear all rows of the Display RAM to the following code shown below.

(D_4) (D_3) (D_2)

C_D C_D C_D

1 0 X --- All Zeros (X = Don't Care)
1 1 0 --- All Hex 20H (0010 0000)
1 1 1 --- All Ones
0 X X --- not clear display if C_A = 0

↑ Enable clear display when C_D = 1 (or by C_A = 1)

While the Display RAM is being cleared, it may not write to the Display RAM. The MSB bit of the FIFO status word is set during this time. If the C_F bit is set to "1", the FIFO status is cleared and the interrupt request output (IRQ) is reset. Also, the Senser RAM pointer is set to the row 0.

The C_A bit has the combined effect of the C_D bit and C_F bit. It enables clear display code to the Display RAM and also clears the FIFO status. Furthermore, it re-synchronizes the internal timing chains.

END Interrupt/Error Mode Set

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	E	X	X	X	X

X: don't care

In the Sensor Matrix mode, this command loweres the IRQ line and enables writing to the Sensor RAM. This means that a write to the Sensor RAM is inhibited when IRQ line is high. If the E bit is set to "1", the S/E bit of the FIFO status becomes "1" when any one of the sensor switches is closed. If E =0, the S/E bit is always "0". In the N-Key Rollorer, if the E bit is programmed to "1", the Special Error mode will be resulted.

FIFO status

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Du	S/E	O	U	F	N	N	N

Number of characters in FIFO
FIFO Full
Error-Underrun
Error-Overrun
Sensor Closure/Error Flag for Multiple Closures
Display unavailable

Du : indicates that the Display RAM is unavailable because a Clear Display or Clear All command has not completed its clearing operation.

S/E : In a Sensor Matrix mode, if the E bit of END Interrupt/Error Mode Set is programmed to "1", this S/E bit is set to indicate that at least one sensor closure indication is contained in the Sensor RAM.
In Special Error Mode, this S/E bit is showing the error flag and serves as an indication to whether a simulataneous multiple closure error has occurred.

O : indicates that the entry of another character into a full FIFO was attempted.

U : indicates that the CPU tried to read an empty FIFO.

F : indicates that the FIFO is full of the eight characters.

NNN : indicate number of characters in the FIFO when in the Keyboard Mode or in the Strobe Input Mode.

[INTERFACE WITH KEYBOARD]

Scanned Keyboard, 2-key LOCKOUT

In this mode, if one key only is kept depressed during one debounce cycle (2 times of the key scan cycle), the key is recognized. When a key is depressed, the debounce logic is set and the other depressed keys are checked during the next two scan cycle. If none are encountered, it is a single key depression and the key position is entered into the FIFO along with the status of CNTL and SHIFT lines. If another depressed key are encountered, operates as follows.

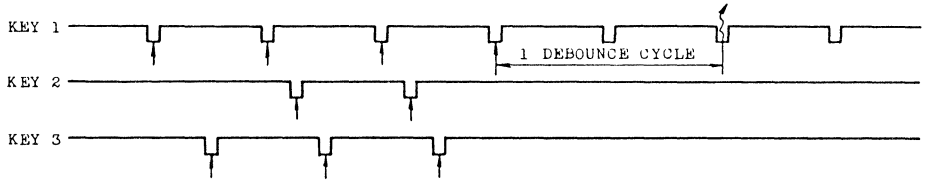
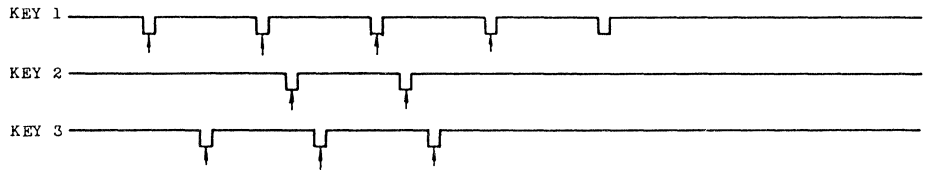


Fig. 1 Example of a case where a first depressed key is continuously kept to the last



↑ ..... Debounce logic is set

↓ ..... Entered to FIFO

Fig. 2 Example of a case where all depressed keys are ignored

As shown in Fig. 1, if all other keys are released before the first depressed key, the first depressed key is recognized. As shown in Fig. 2, if the first depressed key is released within one debounce cycle after the other keys was released, then all keys are ignored.

Scanned Keyboard, N-key Rollover

In this mode, each key depression is independently treated from all others. In the 2-Key lockout mode, if a key is depressed, the debounce logic is set. If other keys are depressed within one debounce cycle after it, the debounce logic is set again. The first depressed key is ignored. In the N-key Rollover mode, if a key is depressed waits one debounce cycle and then checks if the key is still down. If it is, the key is entered into the FIFO even if other keys are depressed.

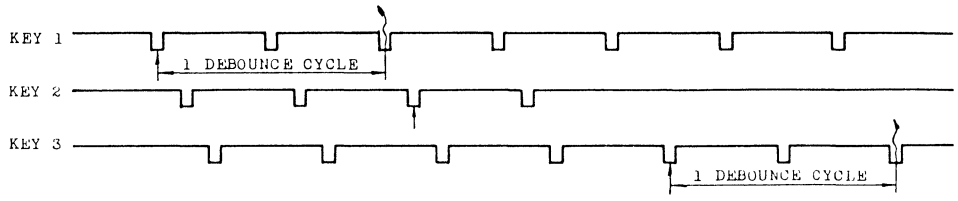


Fig. 3 Example of 3 keys being pushed simultaneously

In the example as shown in Fig. 3, the debounce circuit starts by Key 1, and checks if the key is still down after one debounce cycle. If it is, Key 1 is recognized and Key 2 is ignored not to be depressed for one debounce cycle.

Special Error Mode (N - Key Rollover)

This mode is set if the E bit of the End Interrupt/error Mode Set command is programmed to "1". In the normal N-Key Rollover Mode, the key information is entered to the FIFO according to the key scan timing even if a simulataneous multiple depression occures during one debounce cycle. In the Special Error Mode, if a simulataneous multiple depression occurs during one debounce cycle, sets the error flag (the S/E bit of the FIFO status word) to "1". This flag prevents any further writing into the FIFO and will set interrupt request (IRQ). The S/E bit is cleared if the normal Clear command is written with $C_F = 1$.

Senser Matrix Mode

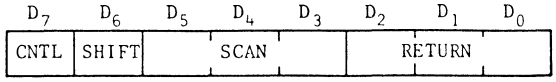
In Sensor Matrix Mode, the debounce circuit does not operate. The status of the senser switch is inputted directly to the Senser RAM. The CPU can know a validated closure in the keyboard, however this mode has such advantage that the CPU knows how long the sensor was closed and when it was released. If there is any change in the sensor value at the end of the sensor matrix scan, the IRQ line goes high. The IRQ line is cleared by the first data read if the Auto-increment flag is "0" or by the End Interrupt/Error Mode Set command if $A_I = 1$.

Strobe Input Mode

In Strobe Input Mode, the debounce circuit does not operate. The data is inputted into the FIFO from the return lines at the rising edge of CNTL/STB Signal. When the data is entered into the FIFO, the IRQ line goes high. The functions of the FIFO and the FIFO status in this mode are same as those in the keyboard mode.

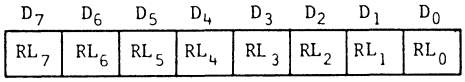
[DATA FORMAT]

Keyboard Mode



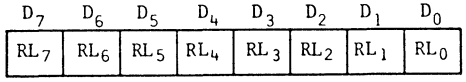
In this mode, the Data Format of the character entered into the FIFO is as follows. The MSB is the status of CNTL/STB line and the next MSB shows the status of SHIFT line. The next three bits are from the scan counter and indicate the row the key was found in. The last three bits are from the column counter and indicate to whitch return line the key was connected.

Sensor Matrix Mode



In this mode, the data on return lines is inputted in the row of the Senser RAM in order according to the scan. The data is entered even if there is no change in the status of the senser matrix switches. Each switch position maps to a Senser RAM position. CNTL and SHIFT signals are ignored.

Strobe Input Mode

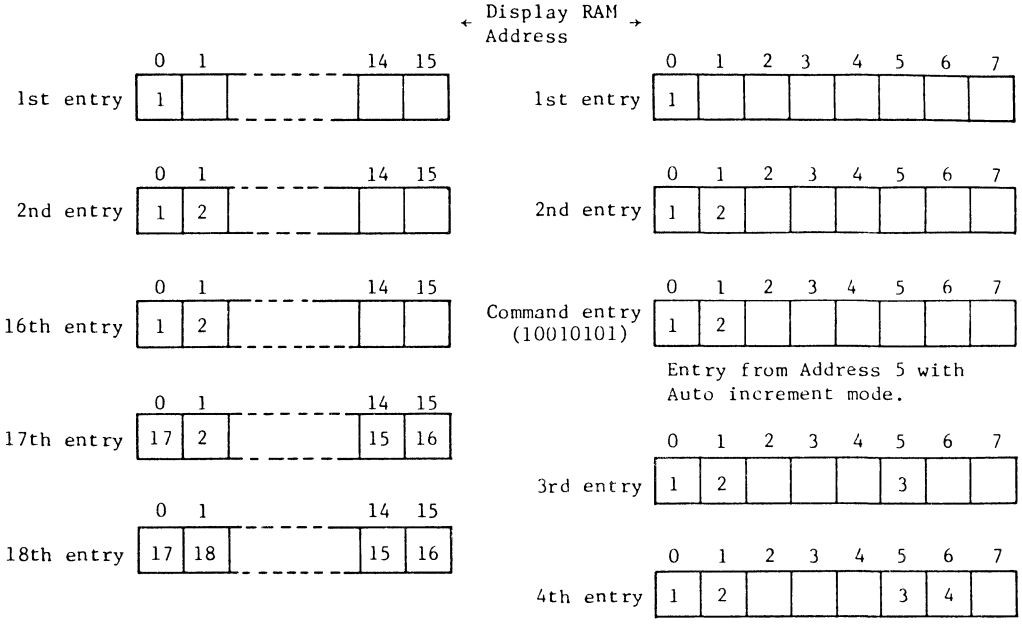


In this mode, the data on the return line is entered into the FIFO at the rising edge of CNTL/STB signal.

[INTERFACE WITH DISPLAY]

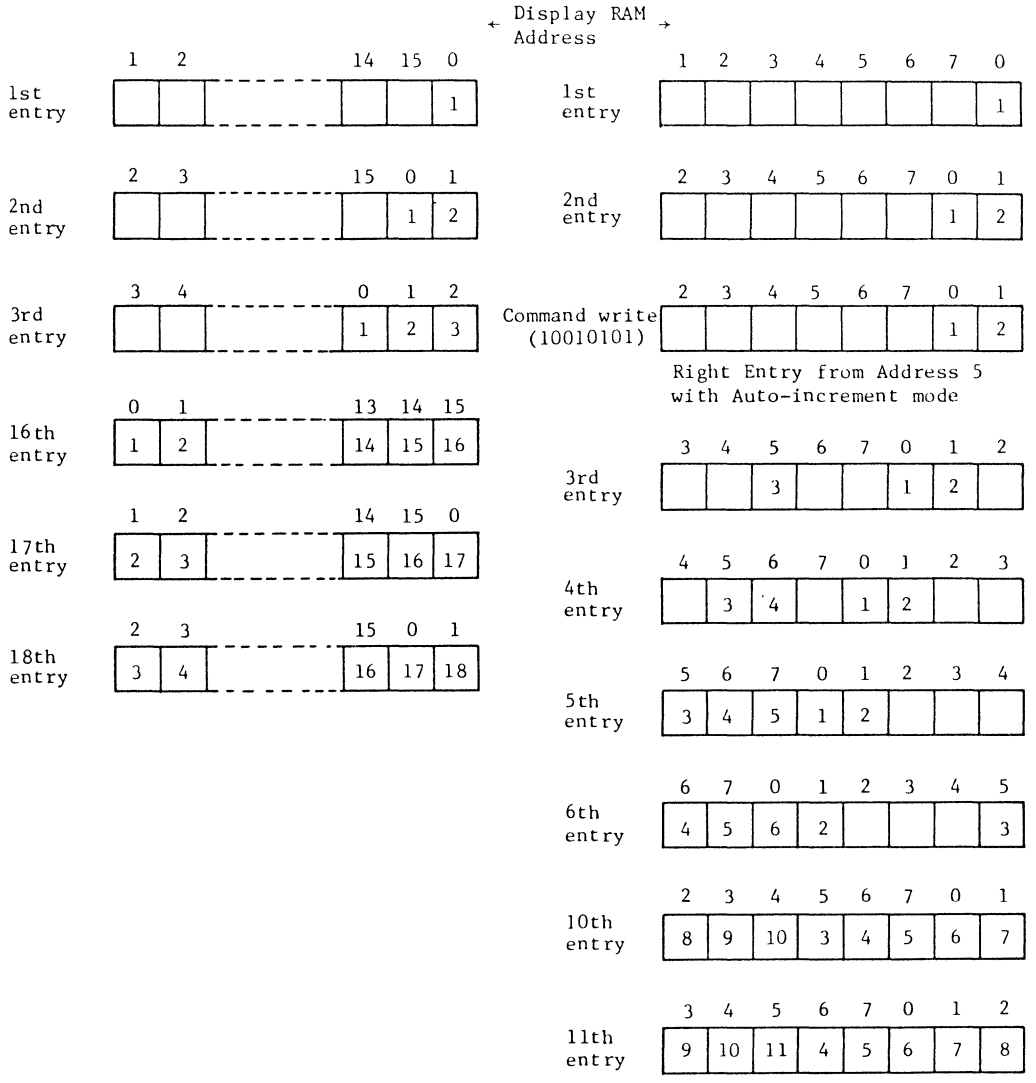
Left Entry

In Left Entry mode, address 0 of the Display RAM is the left-most side of the display and address 15 (address 7 in the case of 8-character display) is the right-most side. When characters are inputted onto the Display RAM with the auto-increment mode from address 0 of the display RAM, Characters are filled from the left-most position of the display. The 17th (or 9th) character is placed in the left-most position again. Address of the display RAM corresponds directry to each display position of the display, and so its position does not change every entry.



Right Entry

In Right Entry, the first entry is from the right-most position. Address of the Display RAM does not correspond to the display position.


← Display RAM Address →
1st entry
2nd entry
3rd entry
16th entry
17th entry
18th entry
Command write (10010101)
Right Entry from Address 5 with Auto-increment mode
4th entry
5th entry
6th entry
10th entry
11th entry

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{CC}	V_{CC} Supply Voltage (with respect to GND (V_{SS}))	-0.5V to +7.0V
V_{IN}	Input Voltage (with respect to GND (V_{SS}))	-0.5V to +7.0V
V_{OUT}	Output Voltage (with respect to GND (V_{SS}))	-0.5V to +7.0V
P_D	Power Dissipation	1W
T_{sol}	Soldering Temperature (soldering time 10 sec)	260°C
T_{stg}	Storage Temperature	-55°C to +150°C
T_{opr}	Operating Temperature	0°C to 70°C

D.C. ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C, V_{CC}=5V±10%, V_{SS}=0V)

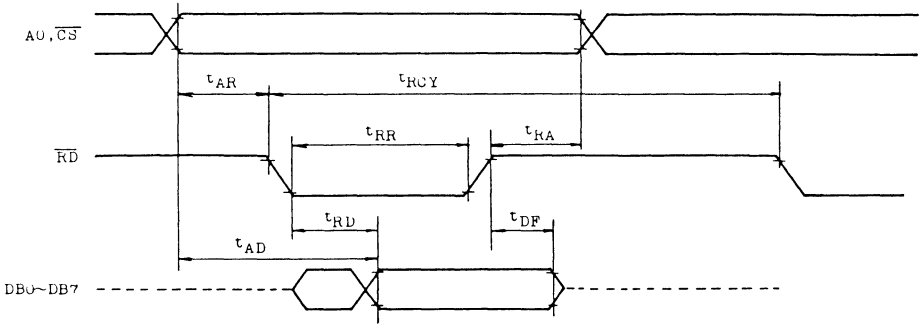
SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{IL1}	Input Low Voltage (RL_0 ~ RL_7)		-0.5		1.4	V
V_{IL2}	Input Low Voltage (Others)		-0.5		0.8	V
V_{IH1}	Input HIgh Voltage (RL_0 ~ RL_7)		2.2			V
V_{IH2}	Input High Voltage (Others)		2.0			V
V_{OL}	Output Low Voltage	I_{OL}=2.2mA			0.45	V
V_{OH1}	Output High Voltage (IRQ)	I_{OH}=-100μA	3.5			V
V_{OH2}	Output High Voltage (Others)	I_{OH}=-400μA	2.4			V
I_{IL1}	Input Leak Current (SHIFT, CNTL, RL_0 ~ RL_7)	V_{IN}=V_{CC}			+10	μA
		V_{IN}=0V			-100	
I_{IL2}	Input Leak Current (Others)	0V ≦ V_{IN} ≦ V_{CC}			±10	μA
I_{OFL}	Output Leak Current	0.45V≦V_{OUT}≦V_{CC}			±10	μA
I_{CC}	Supply Current				120	mA

INPUT CAPACITY

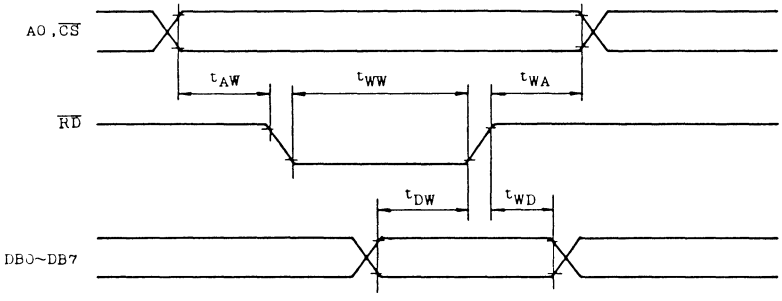
SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacity	f_C=1MHz Unmeasured Pins returned to V_{SS}.		5	10	pF
C_{OUT}	Output Capacity			10	20	pF

A.C. ELECTRICAL CHARACTERISITCS ($Ta=0 \sim 70°C$, $V_{CC}=5.0V \pm 10\%$, $V_{SS}=0V$)

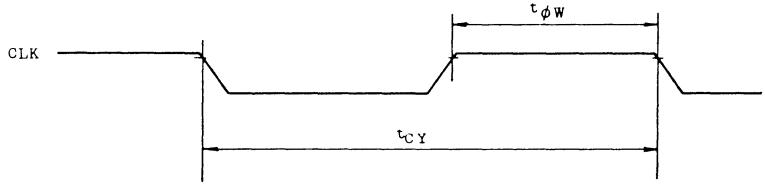
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AR}	Address Set up Time ($\overline{RD}\downarrow$)		0			nS
t_{RA}	Address Hold Time ($\overline{RD}\uparrow$)		0			nS
t_{RR}	$\overline{RD}$ Pulse Width		250			nS
t_{RD}	Valid Data ($\overline{RD}\uparrow$)	$C_L=150pF$			150	nS
t_{AD}	Address to Valid Data	$C_L=150pF$			250	nS
t_{DF}	Data Floating ($\overline{RD}\uparrow$)		10		100	nS
t_{RCY}	Read Cycle Time		1			μS
t_{AW}	Address Set up Time ($\overline{WR}\downarrow$)		0			nS
t_{WA}	Address Hold Time ($\overline{WR}\uparrow$)		0			nS
t_{WW}	$\overline{WR}$ Pulse Width		250			nS
t_{DW}	Data Set up Time ($\overline{WR}\uparrow$)		150			nS
t_{WD}	Data Hold Time ($\overline{WR}\uparrow$)		0			nS
$t_{\phi W}$	CLK Pulse Width		120			nS
t_{CY}	Clock period		320			nS



Read-operation



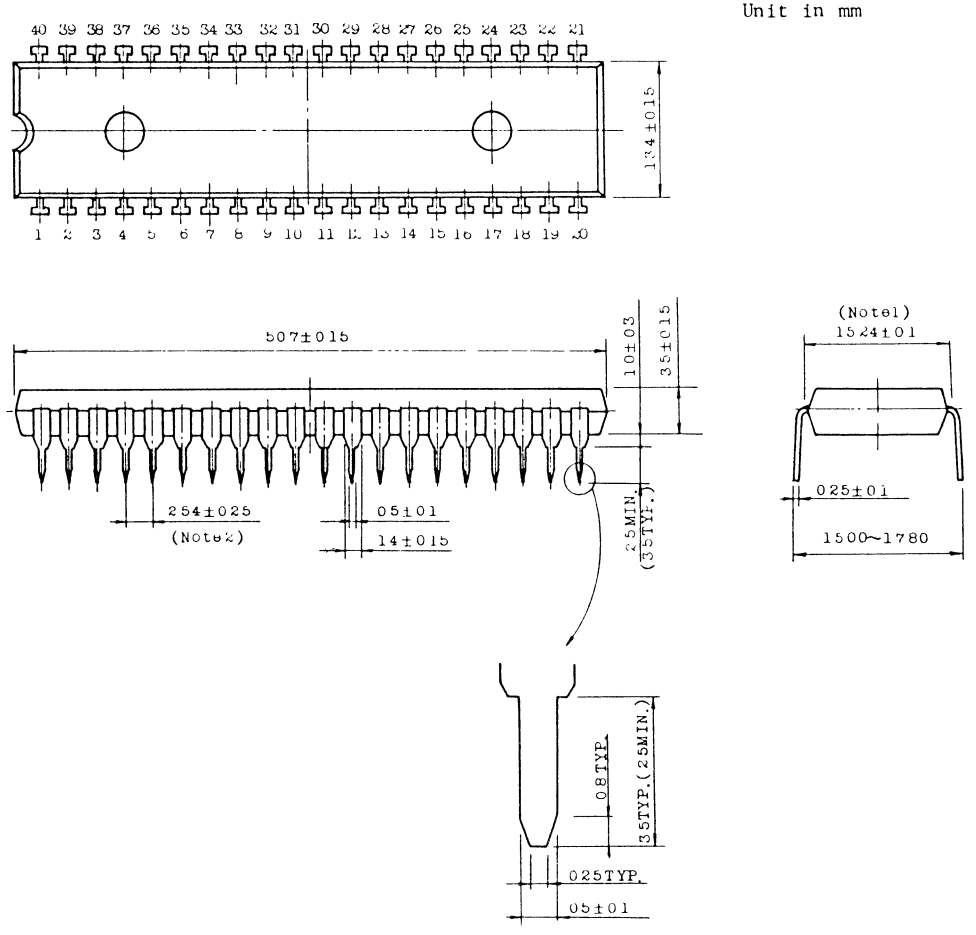
Write-operation



Clock input

OUTLINE DRAWING

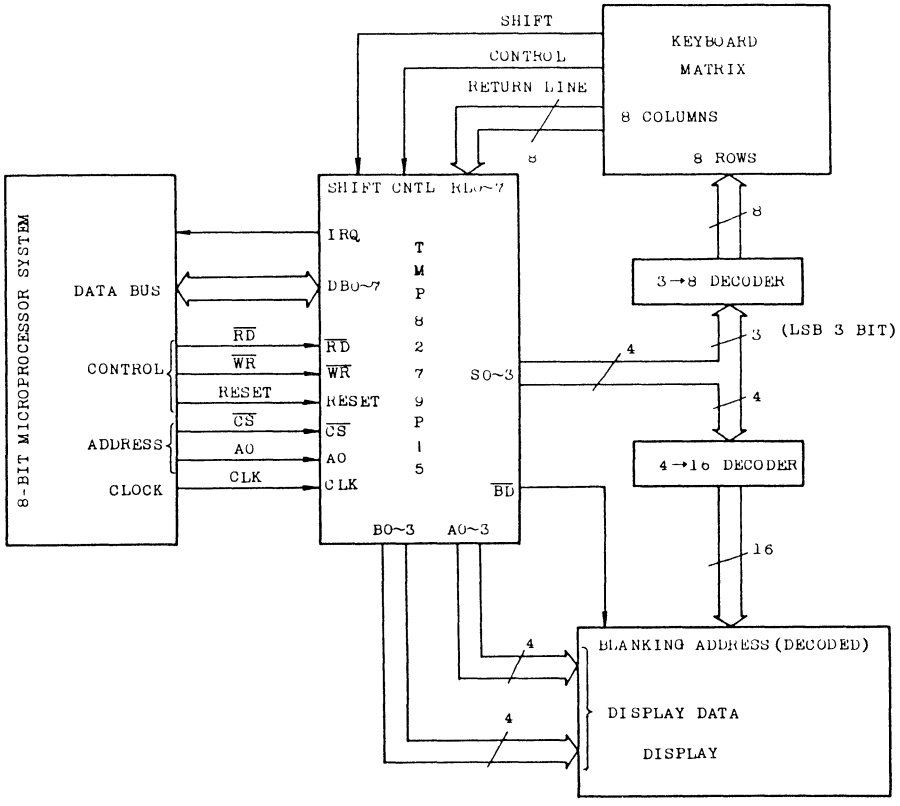
Unit in mm



Note: 1. This dimension is measured at the center of bening point of leads.

2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoritical positions with respect to No.1 and No.40 leads.

EXAMPLE OF APPLICATION CIRCUIT



8 Bit Microcontroller TLCS-48 Family

NMOS 8-BIT MICROCONTROLLER (TLCS-48)

TMP8048AP/TMP8035AP
TMP8049AP/TMP8039AP
TMP8048AT/TMP8035AT
TMP8049AT/TMP8039AT

GENERAL DESCRIPTION

The TMP8048AP/TMP8049AP, from here on referred to as the TMP8048A except in case of no need to specify each parts, is a single chip microcontroller internal 8-bit parallel architecture.

The following basic architectural functions of a computer have been included in a single chip; an 8-bit CPU, RAM data memory, ROM program memory, 27 I/O lines and an 8-bit timer/event counter.

The TMP8048A is particularly efficient as a controller. It has extensive bit handing capability as well as facilities for both binary and BCD arithmetic.

The TMP8035A/TMP8039A is the equivalent of a TMP8048A/TMP8049A without ROM program memory on chip. By using this device with external EPROM or RAM, software debugging becomes easy.

The TMP8048AP/TMP8035AP, TMP8049AP/TMP8039AP are packaged in a standard 40 pin Dual Inline Plastic Package.

The TMP8048AT/TMP8035AT, TMP8049AT/TMP8039AT are packaged in the JEDEC standard type 44pin PLCC (Plastic Leaded Chip Carrier).

FEATURES

- 1.36 us Instruction Cycle
- All instruction 1 or 2 cycles
- Over 90 instructions; 70% single byte
- Easy expandable memory and I/O
- 27 I/O lines
- Interval Time/Event Counter
- Single level interrupt
- Single 5V supply

Parts Number	Program Memory (ROM)	Data Memory (RAM)
TMP8048A	1 k Byte	64 Byte
TMP8049A	2 k Byte	128 Byte
TMP8035A	-	64 Byte
TMP8039A	-	128 Byte

PIN NAMES AND PIN DESCRIPTION

VSS (Power Supply)
Circuit GND potential

VDD (Power Supply)
+5V during operation Low power standby pin for TMP8048A RAM

VCC (Main Power Supply)
+5V during operation

PROG (Output)
Output strobe for the TMP8243P I/O exapnder

P10-P17 (Input/Output) Port 1
8-bit quasi-bidirectional port (Internal Pullup = 50 kohm).

P20-P27 (Input/Output) Port 2
8-bit quasi-bidrectional port (Internal Pullup = 50 kohm).
P20-P23 Contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for the TMP8243P.

DB0-DB7 (Input/Output, 3 State)
True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$ and $\overline{WR}$.

T0 (Input/Output)
Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.

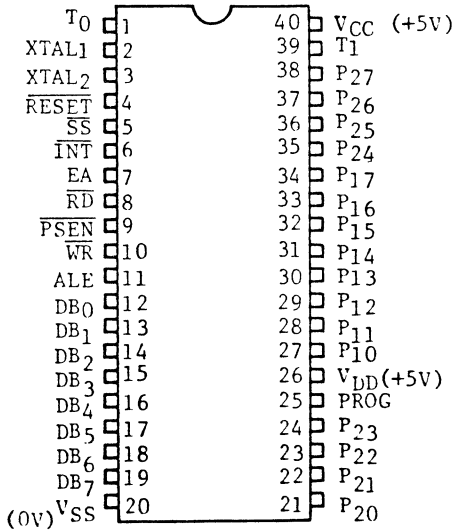
T1 (Input)
Input pin testable using the JT1 and JNT1 instruction. Can be designated the event counter input using the timer/STRT CNT instruction.

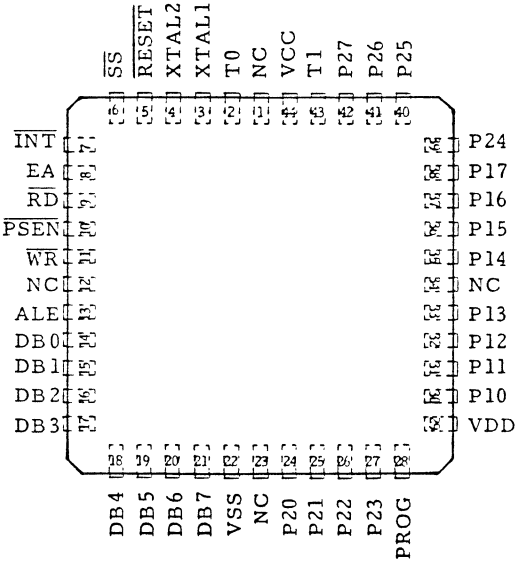
$\overline{INT}$ (Input)
External interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active Low)

$\overline{RD}$ (Output)
Output strobe activated during a Bus read. Can be used to enable data onto the Bus from an external device. Used as a Read Strobe to External Data Memory (Active Low).

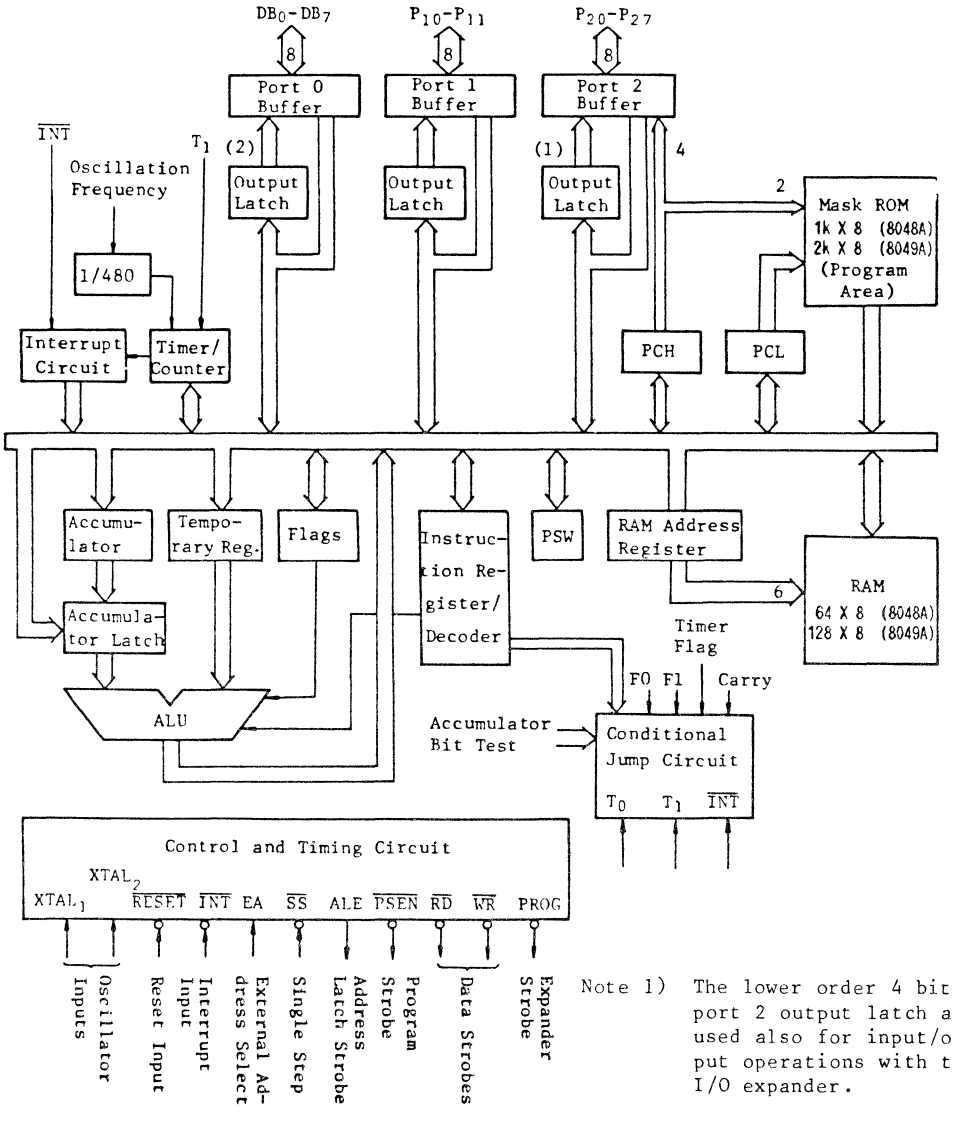
$\overline{WR}$ (Output)
Output strobe during a Bus write (Active Low). Used as a Write Strobe to External Data Memory.

PIN CONNECTIONS (Top View)





BLOCK DIAGRAM



Note 1) The lower order 4 bits of port 2 output latch are used also for input/output operations with the I/O expander.

Note 2) The output latch of port 0 is also used for address output.

$\overline{\text{RESET}}$ (Input)
Active Low signal which is used to initialize the Processor. Also used during Power down.

ALE (Output)
Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.

$\overline{\text{PSEN}}$ (Output)
Program Store Enable. This output occurs only during a fetch to external program memory (Active Low).

$\overline{\text{SS}}$ (Input)
Single Step input can be used in conjunction with ALE to "single step" processor through each instruction when $\overline{\text{SS}}$ is low the CPU is placed into a wait state after it has completed the instruction being excuted.

EA (Input)
External Access input which forces all program memory fetchs to reference external memory. Useful for emulation and debug and essential for testing and program verification. (Active High).

XTAL 1 (Input)
One side of crystal input for internal oscillator. Also input for external source.

XTAL 2 (Input)
Other side of crystal input.

FUNCTIONAL DESCRIPTION

1. System Configuration

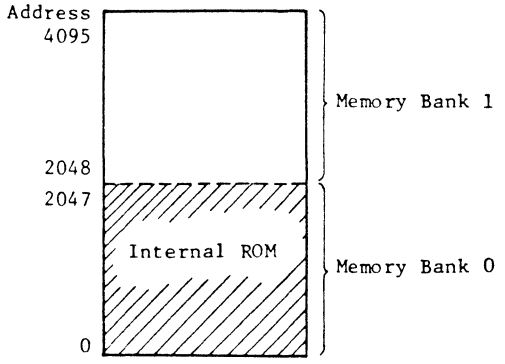
. The following system functions of the TMP8048A are described in detail.

(1)	Program Memory	(6)	Stack (Stack Pointer)
(2)	Data Memory	(7)	Flag 0, Flag 1
(3)	I/O Port	(8)	Program Status Word (PSW)
(4)	Timer/Counter	(9)	Reset
(5)	Interrupt Control Circuit	(10)	Oscillator Circuit

(1) Program Memory

. The maximum memory that can be directly addressed by the TMP8048A is 4096 bytes. The first 1024 bytes from location 0 through 1023 (TMP8048A) or the first 2048 bytes from location 0 to 2047 (TMP8049A) can be internal resident mask ROM. The rest of the 3072 bytes or the 2048 bytes of addressable memory are external to the chip. The TMP8035A and TMP8039A have has no internal resident memory; all memory must be external.

There are three locations in Program Memory of special importance.



Program Memory Area

. Location 0
Activating the Reset line of the processor causes the first instruction to be fetched from Location 0.

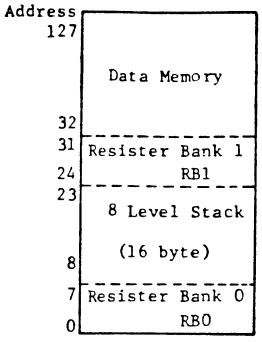
. Location 3
Activating the interrupt line of the processor (if interrupt enabled) causes a jump to subroutine defined by address held in Location 3.

. Location 7
A timer/counter interrupt resulting from a timer/counter overflow (if enabled) causes a jump to a subroutine defined by address held in Location 7.

. Program address 0-2047 and 2048-4095 are called memory banks 0 and 1 respectively switching of memory banks is achieved by changing the most significant bit of the program counter (PC) during execution of an uncoditional jump instruction or call instruction executed after using SEL MB0 or SEL MB1.
Reset operation automatically selects Bank 0.

(2) Data Memory

. Resident Data Memory (volatile RAM) is organized as 64 words (TMP8048A) or 128 words (TMP8049A) by 8-bits wide.
. The first 8 locations (0 - 7) of the memory array are designed as working registers and are directly addressable by several instructions. By executing a Register Bank switch instruction (SEL RB1) locations 24 - 31 are designated as the working registers in palce of 0 - 7.



Internal Data Memory Area

. RAM locations 8 - 23 serve a dual role in that they contain the program counter stack which is a stack 2 bytes wide by 8 levels deep. These locations store returning addresses from subroutines. If the level of subroutine nesting is less than the permitted 8, you free up 2 bytes of RAM for general use for every level of nesting not utilized.

. All 64 (TMP8048A) or 128 (TMP8049A) locations are indirectly addressable through either of two RAM Pointer Registers which reside at R0 and R1 of the Register array.

. The TMP8048A architecture allows extension of the Data Memory to 256 words.

(3) Input/Output Ports

. The TMP8048A has 27 I/O lines which can be used for either input or output. These I/O lines are grouped into 3 ports each having 8 bidirectional lines and 3 "test" inputs which can after program sequences when tested by conditional jump instructions.

. Ports 1 and 2 are each 8-bits wide and have identical characteristics. Data written to these ports is statically latched and remains unchanged until rewritten. As input ports these lines are non-latching, i.e., inputs must be present until read by an input instruction.

. All lines of Ports 1 and 2 are called quasi-bidirectional because of a special output circuit structure (illustrated in Figure 1). Each line is continuously pulled to a +5V level through a high impedance resistive device (50kohm) which is sufficient to provide the source current for a TTL high level yet can be pulled low by a standard TTL gate thus allowing the same pin to be used for both input and output. In order to speed up the "0" to "1" transition a low impedance device (5kohm) is switched in momentarily whenever a "1" is written to line. When "0" is written to line a low impedance device overecomes the pullup and provides TTL current sinking capability.

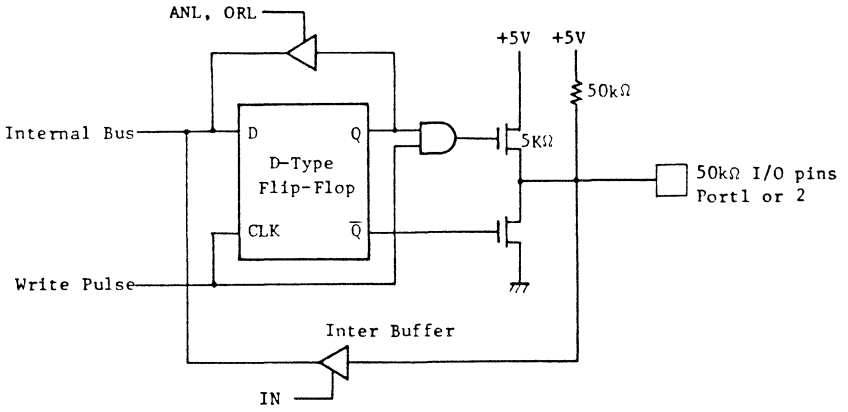


Fig.1 Input/Output Circuit of Port 1, Port 2

. Reset initializes all lines to a high impedance "1" state.

. When external data memory area is not addressed during execution of an internal program, Port 0 (DB0 - DB7) becomes a true bidirectional port (bus) with associated input and output strobes. If bidirectional feature not needed Bus can serve as either a statically latched output port or a non-latched input port. However, I/O lines of this port cannot be intermixed.

. As a static port data is written and latched using the OUTL instruction and inputted using the INS instruction these two commands generate pulses on the corresponding $\overline{RD}$ and $\overline{WR}$ strobe lines.

. As a bidirectional port the MOVX instructions are used to read and write the port which generate the $\overline{RD}$ and $\overline{WR}$ strobes.

. When not being written or read, the Bus lines are in a high impedance state.

(4) Timer/Event Counter

. The 8-bit binary up counter can use either of the following frequency inputs

(1) Internal clock (1/480 of OSC frequency)
..... Timer mode

(2) External input clock form T1 terminal
(minimum cycle time 3 x ALE cycle)
..... Event Counter mode

The counter is presettable and readable with two MOV instructions which transfer the content of the accumulator to the counter and vice versa. The counter content is not affected by a Reset and is initialized solely by the MOVT, A instruction. The counter is stopped by a Reset or STOP TCNT instruction and remains stopped until started by STRT T instruction or as an event counter by a STRT CNT. One started the counter will increment to its maximum count (FF) and overflow to Zero continuing its count until stopped by a STOP TCNT instruction or RESET.

The increment from maximum count to Zero (overflow) results in the setting of an overflow flag and the generation of an interrupt request. When interrupt acknowledged a subroutine call to Location 7 will be initiated. Location 7 should store the starting address of the timer or counter service routine. The state of the overflow flag is testable with the conditional Jump (JTF). The flag is reset by excuting a JTF or by RESET.

Figure 2 illustrates the concept of the timer circuit.

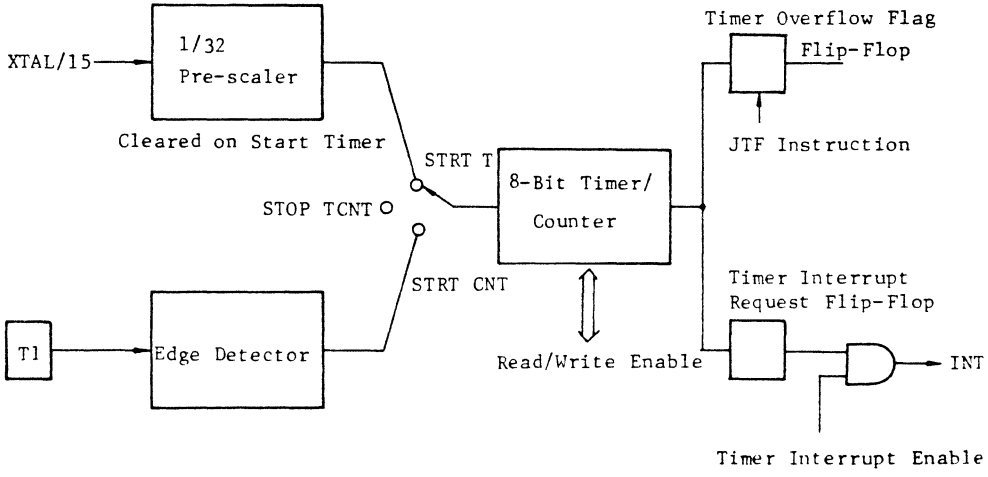


Fig. 2 Concept of Timer Circuit

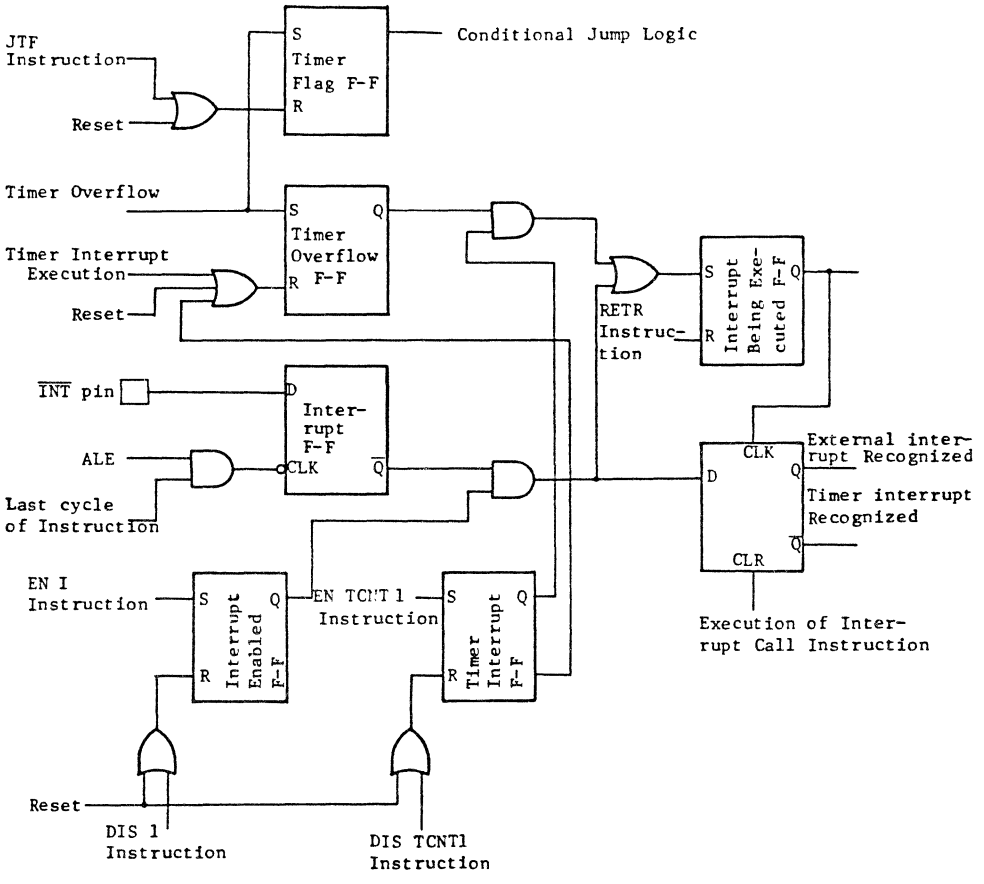


Fig. 3 Concept of Interrupt Control Circuit

(5) Interrupt Control Circuit

. There are two distinct types of Interrupts in the TMP8048A.

(1) External Interrupt from the $\overline{\text{INT}}$ terminal

(2) Timer Interrupt caused by timer overflow

. The interrupt system is single level in that once an interrupt is detected all further interrupt requests are ignored until execution of an RETR (which should occur at the end of an interrupt service routine) reenables the interrupt logic.

. An interrupt sequence is initiated by applying a low level "0" to the $\overline{INT}$ pin. $\overline{INT}$ is level triggered and active low which allows "Wire Oring" of several interrupt sources. The interrupt level is sampled every machine cycle during ALE and when detected causes a "jump to subroutine" at Location 3. As in any call to subroutine, the Program Counter and Program Status Word are saved in the stack.

. When an overflow occurs in the internal timer/event counter an interrupt request is generated which is reserviced as outlined in previous paragraph except that a jump to Location 7 is used instead of 3. If $\overline{INT}$ and times overflow occur simultaneously then external request $\overline{INT}$ takes precedence.

. If an extra external interrupt is needed in addition to $\overline{INT}$ this can be achieved by enabling the counter interrupt, loading FFH in the counter (one less than the terminal count), and enabling the event counter mode. A "1" to "0" transition on T1 will cause an interrupt vector to Location 7.

. The interrupt service routine pointed to be addresses in Location 3 or 7 must reside in memory between 0 and 2047, i.e., Bank 0.

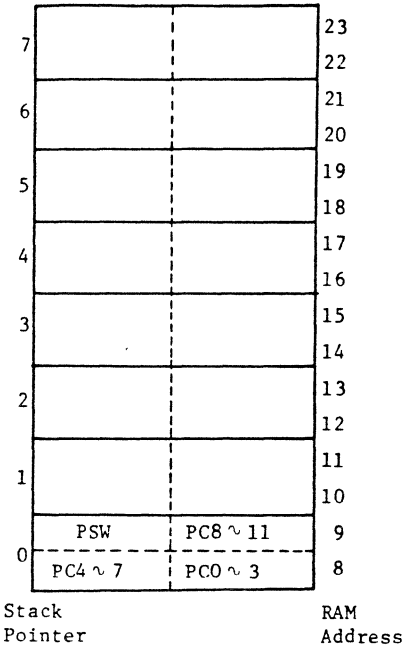
Figure 3 illustrates the concept of the interrupt control circuit.

(6) Stack (Stack Pointer)

. An interrupt or Call to subroutine causes the contents of the program counter to be stored in one of the 8 register pairs of the Program Counter Stack. The pair to be used is determined by a 3-bit stack pointer which is part of the Program Status Words (PSW explained in section (8)). Data RAM locations, 8 through 23 are available as stack registers and are used to store the program counter and 4-bits of PSW as shown in the figure.

. The stack pointer when initialized points to RAM location 8 and 9. The first subroutine jump or interrupt results in the program counter contents being transferred to Locations 8 and 9. Then the stack pointer is incremented by one to point to Locations 10 and 11. Eight levels of subroutine are obviously possible.

. At the end of a subroutine signalled by a RET or RETR causes the stack pointer to be decremented by one and the contents of the resulting pair to be transferred to the Program Counter.



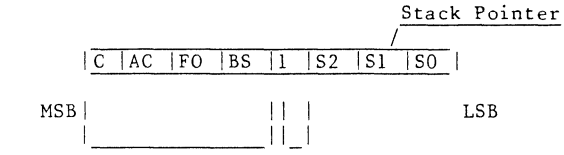
(7) Flag 0, Flag 1 (F0, F1)

. The TMP8048A has two flags F0 and F1 which are used for conditional jump. These flags can be set, reset and tested with the conditional jump instruction JF0.

. F0 is a part of the program status word (PSW) and is saved in the stack area when a subroutine is called.

(8) Program Status Word (PSW)

. An 8-bit status word which can be loaded to and from the accumulator exists called the Program Status Word (PSW). The PSW is read by a MOV A, PWS and written to by a MOV PSW, A. The information available in the PSW is shown in the diagram below.



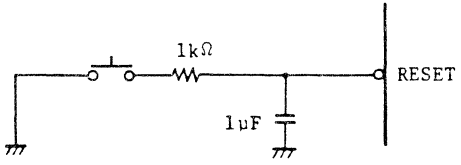
Bits 0 - 2 : Stack Pointer Bits (S0, S1, S2)
Bit 3 : Not used ("1" level when read.)
Bit 4 : Working Register Bank Switch Bit (BS)

0 = Bank 0
1 = Bank 1

Bit 5 : Flag 0 (F0)
Bit 6 : Auxiliary Carry (AC) carry bit generated by an ADD instruction and used by the decimal adjust instruction DA, A (AC)
Bit 7 : Carry (C) flag which indicates that the previous operation has resulted in the accumulator. (C)

(9) Reset

. The reset input provides a means for initialization of the processor. This Schmitt trigger input has an internal pullup register which in combination with an external 1uF capacitor provides an internal reset pulse sufficient length to guarantee that all internal logic is initialized.



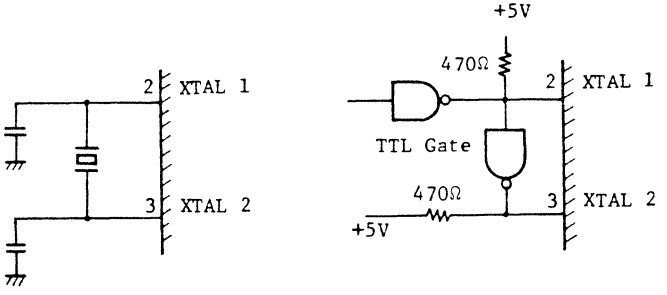
If the pulse is generated externally the reset pin must be held at ground ($\leqq$0.8V) for at least 10mS after the power supply is within tolerance.

. Reset performs the following functions within the chip:

(i) Sets PC to Zero.
(ii) Sets Stack Pointer to Zero.
(iii) Selects Register Bank 0.
(iv) Selects Memory Bank 0.
(v) Sets BUS (DB0 - DB7) to high impedance state. (Except when EA=5V)
(vi) Sets Ports 1 and 2 to input mode.
(vii) Disables interrupts (timer and external).
(viii) Stops Timer.
(ix) Clears Timer Flag.
(x) Clears F0 and F1.
(xi) Disables clock output from T0.

(10) Oscillator Circuit

. TMP8048A can be operated by the external clock input in addition to crystal oscillator as shown below.



(a) Crystal Parameters and External Capacitance

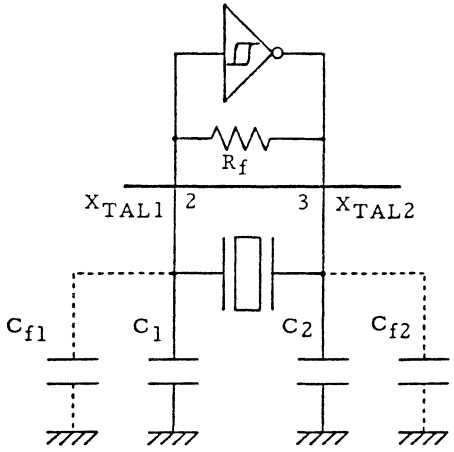
The frequency of the oscillator will be calculated from the following formula.

$$f = (1+C0/2(CL+C))/2\pi\sqrt{L \times C0}$$

Load Capacitance DL
CL=(C1+Cf1)(C2+Cf2)/((C1+Cf1)+(C2+Cf2))
Cf1 : Input Capacitance (4pF Typ.)+Stray Capacitance (less than 5pF)
Cf2 : Output Capacitance(6pF Typ.)+Stray Capacitance (less than 5pF)

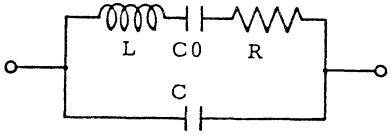
However the recommended value in the following table will be used better by the reason of the start of the oscillation will depend on the Equivalent Series Resistance Rl and the External Capacitances Cl+Cfl, C2+Cf2.

Frequency f(MHz)	Equivalent Series Res. R(ohm)	External Capacitance Cl=C2(pF) Recommended Value	Typical Allowance
11	25 Max.	10	5 to 17
11	30 Max.	10	5 to 15
10	25 Max.	10	5 to 20
10	30 Max.	10	5 to 17
8	30 Max.	15	5 to 25
8	40 Max.	10	5 to 20
6	40 Max.	20	5 to 35
6	80 Max.	10	5 to 17
5	50 Max.	20	5 to 40
5	80 Max.	15	5 to 25
4	100 Max.	15	5 to 30
4	150 Max.	10	5 to 20
3	100 Max.	20	5 to 40
3	200 Max.	15	5 to 25
2	400 Max.	25	5 to 40
2	500 Max.	15	5 to 25
1	800 Max.	25	10 to 40



(b) Ceramic Resonator and External Capacitance

Frequency f(MHz)	External Capacitance Recommended Value Cl=C2 (pF)
3 to 11	33
1 to 3	100



2. Basic Operation and Timing

The following basic operations and timing are explained

(1) Instruction Cycle
(2) External Memory Access Timing
(3) Interface with I/O Expander TMP8243P
(4) Internal Program Verify (Read) Timing
(5) Single Step Operation Timing
(6) Low Power Stand-by Mode

(1) Instruction Cycle

. The instruction of TMP8048A are executed in one or two machine cycles, and one machine cycle contents of five states.

. Fig. 4 illustrates its relationship with the clock input to CPU.

. $\phi 2$ clock shown in Fig. 4 is derived to outside by ENTO CLK instruction.

. ALE can be also used as the clock to indicate the machine cycle as well as giving the external address latch timing.

(2) External Memory Access Timing

(i) Program Memory Access

. TMP8048A programs are executed in the following three modes.

(1) Execution of internal program only.
(2) Execution of both external and internal programs.
(3) Execution of external program only.

The external program memory is accessed (instructions are fetched) automatically when the internal ROM address is exceeded in mode (2) and from initial start address 0 in mode (3).

. In the external program memory access operation, the following will occur
  . The contents of the 12-bit program counter will be output on BUS(DB0 - DB7) and the lower 4-bits of Port 2.
  . Address Latch Enable (ALE) will indicate the time at which address is valid. The trailing edge of ALE is used to latch the address externally.
  . Program Store Enable ($\overline{\text{PSEN}}$) indicates that an external instruction fetch is in progress and serves to enable the external memory device.
  . Bus (DB0 - DB7) reverts to Input mode and the processor accepts its 8-bit contents as an Instruction Word.

. Figure 5 illustrates the timing.

(ii) Access of External Data Memory

. In the extended data memory access operation during READ/WRITE cycle the following occurs
  . The contents of R0 R1 is output onto BUS (DB0 - DB7).
  . ALE indicates address is valid. The trailing edge of ALE is used to latch the address externally.
  . A read $\overline{\text{RD}}$ or write $\overline{\text{WR}}$ pulse on the corresponding output pins indicates the type of data memory access in progress. Output data valid at trailing edge of $\overline{\text{WR}}$ and input data must be valid at trailing edge of $\overline{\text{RD}}$.
  . Data (8-bits) is transferred over BUS.

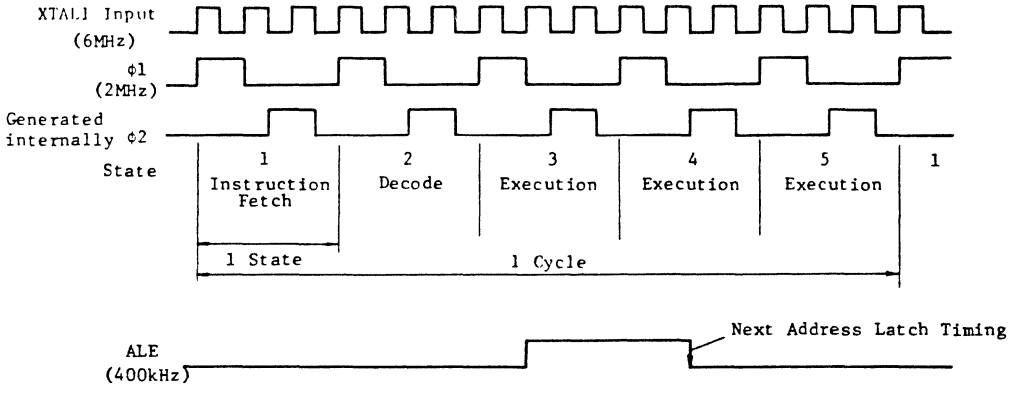


Fig. 4 Instruction Cycle Timing

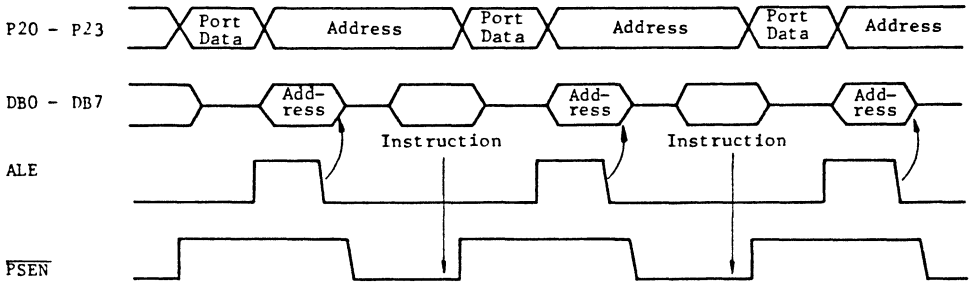
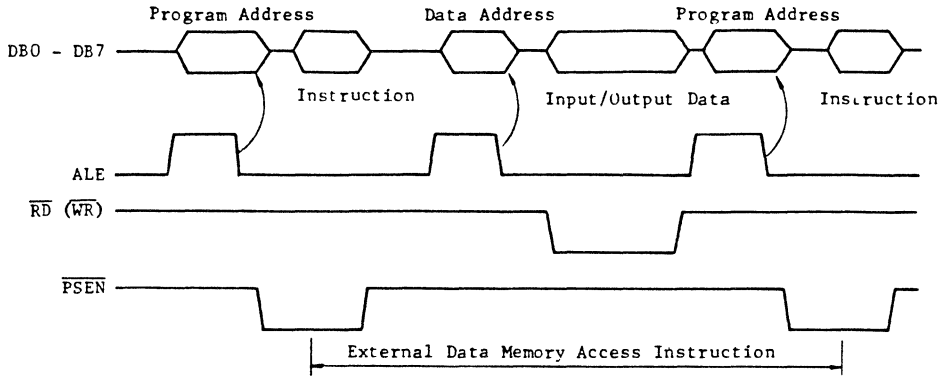


Fig. 5 Timing of External Program Memory Access



Suggest we have two diagrams

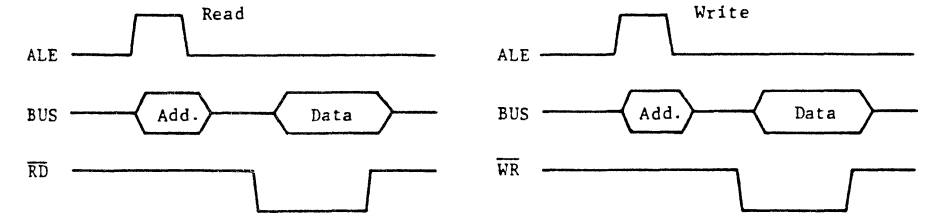


Fig. 6 Timing of Accessing External Data Memory

. Figure 6 illustrates the timing of accessing the external data memory during execution of external program.

(3) Interface with I/O Expander (TMP8243P)

. The TMP8048A I/O can be easily expanded using the TMP8243 I/O Expander. This device uses only the lower half 4-bits of Port 2 for communication with the TMP8048A. The TMP8243 contains for 4-bit I/O ports which serve as extensions of one chip I/O and are addressed as Ports (4-7). All communication takes place over the lower half of port 2 (P20 - P23) with timing provided by an output pulse on the PROG pin. Each transfer consists of two 4-bit nibbles the first containing the "OP Code" and port address and second containing the actual 4-bits of data.

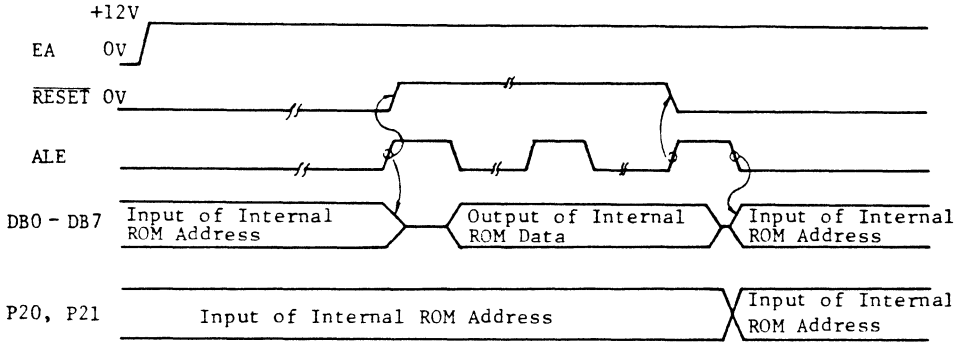


Fig. 7 Timing of Reading Internal Program Memory

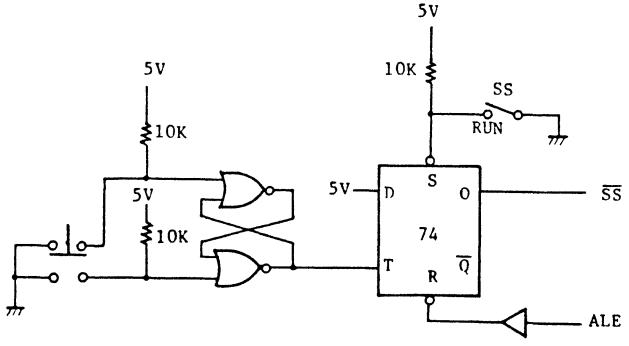


Fig. 8(a) Single Step Circuit

Reading of Internal Program Memory

. The processor is placed in the READ mode by applying +12V to the EA pin and 0V to the RESET pin. The address of the location to be read is then applied to BUS and the low order 2 or 3 bits of Port 2. The address is latched by a 0 to 1 transition on RESET and the high level causes the contents of program memory location addressed to appear on the eight lines of BUS.

. Figure 7 illustrates the timing diagram for this operation.

(5) Single Step Operation.

. A single step feature useful for debug can be implemented by utilizing a circuit shown in Figure 8 (a) combined with the $\overline{SS}$ pin and ALE pin.

. A D-type flip flop with set and reset is used to generate SS. In the run mode $\overline{SS}$ is held high by keeping the flip flop set. To enter single step, set is removed allowing ALE to bring $\overline{SS}$ low via reset input. The next instruction is started by clocking a "1" into the FF which will not appear on $\overline{SS}$ unless ALE is high removing reset. In response to SS going high the processor begins an instruction fetch which brings ALE low resetting FF and causing the processor to again enter the stopped state.

. The timing diagram in this case is as shown in Figure 8 (b). (EA=5V)

(6) Lower Power Stand-by Mode

. The Lower TMP8048A has been organized to allow power to be removed from all but the volatile, 64 x 8 or 128 x 8 data RAM array. In power down mode the contents of data RAM can be maintained while drawing typically 10 - 15% of normal operating power requirements.

. VCC serves as the 5V supply for the bulk of the TMP8048A while the VDD supplies only the RAM array. In standby mode VCC is reduced to 0V but VDD is kept at 5V. Applying a low level to reset inhibits any access to the RAM by the processor and guarantees that RAM cannot be inadvertently altered as power is removed from VCC.

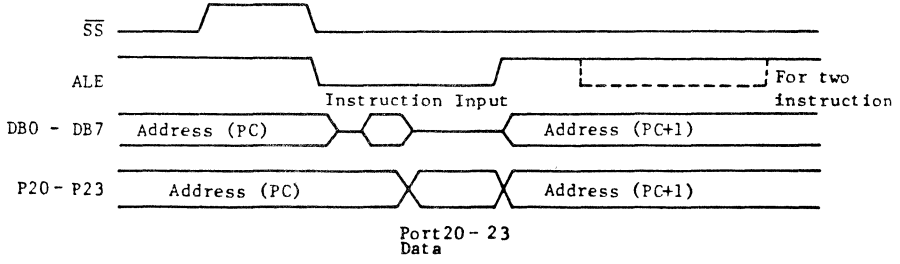


Fig. 8(b) Single Step Operation Timing

INSTRUCTION

ACCUMULATOR INSTRUCTION

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
ADD A,Rr	0	1	1	0	1	r	r	r	(A)<-(A)+(Rr) r = 0 - 7	1	1	o	o
ADD A,@Rr	0	1	1	0	0	0	0	r	(A)<-(A)+((Rr)) r = 0,1	1	1	o	o
ADD A,#Data	0 d7	0 d6	0 d5	0 d4	0 d3	0 d2	1 d1	1 d0	(A)<-(A)+Data	2	2	o	o
ADDC A,Rr	0	1	1	1	1	r	r	r	(A)<-(A)+(Rr)+(C) r = 0 - 7	1	1	o	o
ADDC A,@Rr	0	1	1	1	0	0	0	r	(A)<-(A)+((Rr)) +(C) r = 0,1	1	1	o	o
ADDC A,#Data	0 d7	0 d6	0 d5	1 d4	0 d3	0 d2	1 d1	1 d0	(A)<-(A)+Data+(C)	2	2	o	o
ANL A,Rr	0	1	0	1	1	r	r	r	(A)<-(A)and(Rr) r = 0 - 7	1	1	-	-
ANL A,@Rr	0	1	0	1	0	0	0	r	(A)<-(A)and((Rr)) r = 0,1	1	1	-	-
ANL A,#Data	0 d7	1 d6	0 d5	1 d4	0 d3	0 d2	1 d1	1 d0	(A)<-(A)and Data	2	2	-	-
ORL A,Rr	0	1	0	0	1	r	r	r	(A)<-(A)or(Rr) r = 0 - 7	1	1	-	-
ORL A,@Rr	0	1	0	0	0	0	0	r	(A)<-(A)or((Rr)) r = 0,1	1	1	-	-
ORL A,#Data	0 d7	1 d6	0 d5	0 d4	0 d3	0 d2	1 d1	1 d0	(A)<-(A)or Data	2	2	-	-
XRL A, Rr	1	1	0	1	1	r	r	r	(A)<-(A)Eor(Rr) r = 0 - 7	1	1	-	-
XRL A,@Rr	1	1	0	1	0	0	0	r	(A)<-(A)Eor((Rr)) r = 0,1	1	1	-	-
XRL A,#Data	0 d7	1 d6	0 d5	0 d4	0 d3	0 d2	1 d1	1 d0	(A)<-(A)Eor Data	2	2	-	-
INC A	0	0	0	1	0	1	1	1	(A)<-(A)+1	1	1	-	-
DEC A	0	0	0	0	0	1	1	1	(A)<-(A)-1	1	1	-	-
CLR A	0	0	1	0	0	1	1	1	(A)<-0	1	1	-	-
CPL A	0	0	1	1	0	1	1	1	(A)<-NOT (A)	1	1	-	-
DA A	0	1	0	1	0	1	1	1	Decimal Adjust Accumulator	1	1	o	-
SWAP A	0	1	0	0	0	1	1	1	(A4-7)->(A0-3) <-	1	1	-	-

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
RL A	1	1	1	0	0	1	1	1	(An+1)<-(An) n = 0 - 6	1	1	-	-
RLC A	1	1	1	1	0	1	1	1	(An+1)<-(An) n = 0 - 6 (C)<-(A7) (A0)<-(C)	1	1	-	-
RR A	0	1	1	1	0	1	1	1	(An)<-(An+1) n = 0 - 6 (A7)<-(A0)	1	1	-	-
RRC A	0	1	1	0	0	1	1	1	(An)<-(An+1) n = 0 - 6 (C)<-(A0) (A7)<-(C)	1	1	-	-

Input/Output Instruction

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
IN A,Pp	0	0	0	0	1	0	P	P	(A)<-(Pp) p = 1, 2	1	2	-	-
OUTL Pp,A	0	0	1	1	1	0	P	P	(Pp)<-(A) p = 1, 2	1	2	-	-
ANL Pp,#Data	1	0	0	1	1	0	P	P	(Pp)<-(Pp)and Data p = 1, 2	2	2	-	-
	d7	d6	d5	d4	d3	d2	d1	d0					
ORL Pp,#Data	1	0	0	0	1	0	P	P	(Pp)<-(Pp)or Data p = 1, 2	2	2	-	-
	d7	d6	d5	d4	d3	d2	d1	d0					
INS A,BUS	0	0	0	0	1	0	0	0	(A)<-(BUS)	1	2	-	-
OUTL BUS,A	0	0	0	0	0	0	1	0	(BUS)<-(A)	1	2	-	-
ANL BUS,#Data	1	0	0	1	1	0	0	0	(BUS)<-	2	2	-	-
	d7	d6	d5	d4	d3	d2	d1	d0	(BUS)and Data				
ORL BUS,#Data	1	0	0	0	1	0	0	0	(BUS)<-	2	2	-	-
	d7	d6	d5	d4	d3	d2	d1	d0	(BUS) or Data				
MOVD A,Pp	0	0	0	0	1	1	P	P	(A0-3)<-(Pp) (A4-7)<- 0 p = 4 - 7	1	2	-	-
MOVD Pp,A	0	0	1	1	1	1	P	P	(Pp)<-(A0-3) p = 4 - 7	1	2	-	-
ANLD Pp,A	1	0	0	1	1	1	P	P	(Pp)<- (Pp)and(A0-3) p = 4 - 7	1	2	-	-
ORLD Pp,A	1	0	0	0	1	1	P	P	(Pp)<- (Pp)or (A0-3) P = 4 - 7	1	2	-	-

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
INC Rr	0	0	0	1	1	r	r	r	(Rr)<--(Rr)+1	1	1	-	-
									r = 0 - 7				
INC @Rr	0	0	0	1	0	0	0	r	((Rr))<-((Rr))+1	1	1	-	-
									r = 0, 1				
DEC Rr	1	1	0	0	1	r	r	r	(Rr)<--(Rr)-1	1	1	-	-
									r = 0 - 7				

Branch Instruction

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
JMP Address	a10	a9	a8	0	0	1	0	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	(PC8-10)<--(a8-10				
									(PC11)<--DBF				
JMPP @A	1	0	1	1	0	0	1	1	(PC0-7)<--((A))	1	2	-	-
DJNZ Rr	1	1	1	0	1	r	r	r	(Rr)<--(Rr)-1	2	2	-	-
Address	a7	a6	a5	a4	a3	a2	a1	a0	if Rr not 0				
									(PC0-7)<--(a0-7)				
JC Address	1	1	1	1	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if C = 1				
									(PC)<--(PC)+2				
									if C = 0				
JNC Address	1	1	1	0	0	1	1	0	(PC0-7)<-(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if C = 0				
									(PC)<--(PC)+2				
									if C = 1				
JZ Address	1	1	0	0	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if (A) = 0				
									(PC)<--(PC)+2				
									if (A).NEQ.0				
JNZ Adress	1	0	0	1	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if (A).NEQ.0				
									(PC)<--(PC)+2				
									if (A) = 0				
JT0 Adress	0	0	1	1	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if T0 = 1				
									(PC)<--(PC)+2				
									if T0 = 0				
JNT0 Address	0	0	1	0	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if T0 = 0				
									(PC)<--(PC)+2				
									if T0 = 1				
JT1 Address	0	1	0	1	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if T1 = 1				
									(PC)<--(PC)+2				
									if T1 = 0				
JNT1 Address	0	1	0	0	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if T1 = 0				
									(PC)<--(PC)+2				
									if T1 = 1				

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
JF0 Address	1	0	1	1	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if F0 = 1				
									(PC)<--(PC)+2				
									if F0 = 0				
JF1 Address	0	1	1	1	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if F1 = 1				
									(PC)<--(PC)+2				
									if F1 = 0				
JTF Address	0	0	0	1	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if TF = 1				
									(PC)<--(PC)+2				
									if TF = 0				
JNI Address	1	0	0	0	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if INT = 0				
									(PC)<--(PC)+2				
									if INT = 1				
JBb Address	b2	b1	b0	1	0	0	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if (Bb) = 1				
									(PC)<--(PC)+2				
									if (Bb) = 0				
									(b = 0 - 7)				
CALL Address	a10	a9	a8	1	0	1	0	0	((SP))<--	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	(PC),(PSW4-7)				
									(SP)<--(SP)+1				
									(PC8-10)<--(a8-10)				
									(PC0-7)<--(a0-7)				
									(PC11)<--DBF				
RET	1	0	0	0	0	0	1	1	(SP)<--(SP)-1	1	2		
									(PC)<--((SP))				
RETR	1	0	0	1	0	0	1	1	(SP)<--(SP)-1	1	2		
									(PC)<--((SP))				
									(PSW4-7)<--((SP))				

Flag Manipulation Instruction

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
CLR C	1	0	0	1	0	1	1	1	(C)<-- 0	1	1	0	-
CPL C	1	0	1	0	0	1	1	1	(C)<--NOT(C)	1	1	0	-
CLR F0	1	0	0	0	0	1	0	1	(F0)<-- 0	1	1	-	-
CPL F0	1	0	0	1	0	1	0	1	(F0)<--NOT(F0)	1	1	-	-
CLR F1	1	0	1	0	0	1	0	1	(F1)<-- 0	1	1	-	-
CPL F1	1	0	1	1	0	1	0	1	(F1)<--NOT(F1)	1	1	-	-

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
MOV A, Rr	1	1	1	1	1	r	r	r	(A)<-- (Rr) r = 0 - 7	1	1	-	-
MOV A, @Rr	1	1	1	1	0	0	0	r	(A)<-- ((Rr)) r = 0, 1	1	1	-	-
MOV A, #Data	0	0	1	0	0	0	1	1	(A)<-- Data	2	2	-	-
	d7	d6	d5	d4	d3	d2	d1	d0					
MOV Rr, A	1	0	1	0	1	r	r	r	(Rr)<--(A) r = 0 - 7	1	1	-	-
MOV@Rr,A	1	0	1	0	0	0	0	r	((Rr))<-(A) r = 0, 1	1	1	-	-
MOV Rr,#Data	1	0	1	1	1	r	r	r	(Rr)<--Data	2	2	-	-
	d7	d6	d5	d4	d3	d2	d1	d0	r = 0 - 7				
MOV@Rr,#Data	1	0	1	1	0	0	0	r	((Rr))<--Data	2	2	-	-
	d7	d6	d5	d4	d3	d2	d1	d0	r = 0, 1				
MOV A,PSW	1	1	0	0	0	1	1	1	(A)<-- (PSW)	1	1	-	-
MOV PSW, A	1	1	0	1	0	1	1	1	(PSW)<--(A)	1	1	-	-
XCH A, Rr	0	0	1	0	1	r	r	r	(A)-->(Rr) <-- r = 0 - 7	1	1	-	-
XCH A,@Rr	0	0	1	0	0	0	0	r	(A)-->((Rr)) <-- r = 0, 1	1	1	-	-
XCHD A,@Rr	0	0	1	1	0	0	0	r	(A0-3)-->((Rr0-3)) <-- r = 0, 1	1	1	-	-
MOVX A,@Rr	1	0	0	0	0	0	0	r	(A)<--((Rr)) r = 0, 1	1	2	-	-
MOVX @Rr,A	1	0	0	1	0	0	0	r	((Rr))<--(A) r = 0, 1	1	2	-	-
MOVP A,@A	1	0	1	0	0	0	1	1	(PC0-7)<--(A) (A)<--((PC))	1	2	-	-
MOVP3 A,@A	1	1	1	0	0	0	1	1	(PC0-7)<--(A) (PC8-11)<--0011 (A)<--((PC))	1	2	-	-

Timer/Counter Instruction

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
MOV A,T	0	1	0	0	0	0	1	0	(A)<--(T)	1	1	-	-
MOV T,A	0	1	1	0	0	0	1	0	(T)<--(A)	1	1	-	-
STRT T	0	1	0	1	0	1	0	1	Counting is started in the timer mode	1	1	-	-
STRT CNT	0	1	0	0	0	1	0	1	Counting is started in the event counter mode	1	1	-	-
STOP TCNT	0	1	1	0	0	1	0	1	Stop both time accumulation and event counting	1	1	-	-
EN TCNTI	0	0	1	0	0	1	0	1	Timer interrupt is enabled	1	1	-	-
DIS TCNTI	0	0	1	1	0	1	0	1	Timer interrupt is disabled	1	1	-	-

Control Instruction

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
EN I	0	0	0	0	0	1	0	1	External interrupt is enabled	1	1	-	-
DIS I	0	0	0	1	0	1	0	1	External interrupt is disabled	1	1	-	-
SEL RB0	1	1	0	0	0	1	0	1	(BS)<-- 0	1	1	-	-
SEL RB1	1	1	0	1	0	1	0	1	(BS)<-- 1	1	1	-	-
SEL MB0	1	1	1	0	0	1	0	1	(DBF)<-- 0	1	1	-	-
SEL MB1	1	1	1	1	0	1	0	1	(DBF)<-- 1	1	1	-	-
ENTO CLK	0	1	1	1	0	1	0	1	T0 is enabled to act as the clock output	1	1	-	-
NOP	0	0	0	0	0	0	0	0	No operation	1	1	-	-

SYMBOL	ITEM	RATTING
VDD	VDD Supply Voltage (with respect to GND (VSS))	-0.5V to +7V
VCC	VCC Supply Voltage (with respect to GND (VSS))	-0.5V to +7V
VINA	Input Voltage (Except EA)	-0.5V to +7V
VINB	Input Voltage (Only EA)	-0.5V to +13V
PD	Power Dissipation (Ta = 70°C)	1.5W
TSOLDER	Soldering Temperature (Soldering Time 10 sec)	260°C
TSTG	Storage Temperature	-55°C to 150°C
TOPR	Operating Temperature	0°C to 70°C

DC CHARACTERISTICS

T_A=0°C to 70°C, VCC=VDD=+5V±10%, VSS=0V, Unless Otherwise Noted.

SYMBOL		TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage		-0.5	-	0.8	V
VIH	Input High Voltage (Except XTAL1,XTAL2,$\overline{\text{RESET}}$)		2.0	-	VCC	V
VIH1	Input High Voltage ($\overline{\text{XTAL1}}$,XTAL2,$\overline{\text{RESET}}$)		3.8	-	VCC	V
$\overline{\text{VOL}}$	Output Low Voltage (BUS)	IOL=2.0mA	-	-	0.45	V
$\overline{\text{VOL1}}$	Output Low Voltage ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, ALE)	IOL=1.8mA	-	-	0.45	V
VOL2	Output Low Voltage (PROG)	IOL=1.0mA	-	-	0.45	V
VOL3	Output Low Voltage (For other output pins)	IOL=1.6mA	-	-	0.45	V
VOH	Output High Voltage (BUS)	IOH=-400uA	2.4	-	-	V
VOH1	Output High Voltage ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, ALE)	IOH=-100uA	2.4	-	-	V
VOH2	Output High Voltage (For other output pins)	IOL=-40uA	2.4	-	-	V
ILI	Input Leak Current (T1, $\overline{\text{INT}}$)	VSS $\leqq$ VIN $\leqq$ VCC	-	-	±10	uA
ILI1	Input Leak Current ($\overline{\text{P10-17}}$, P20-27, EA, $\overline{\text{SS}}$)	VSS+0.45$\leqq$VIN$\leqq$ VCC			-500	uA
ILO	Output Leak Current (BUS, T0) (High impedance condition	VSS+0.45$\leqq$VIN$\leqq$ VCC			±10	uA

DC CHARACTERISTICS

T_A=0°C to 70°C, VCC=VDD=+5V±10%, VSS=0V, Unless Otherwise Noted.

SYMBOL	PARAMETER	TMP8048A/ TMP8035A			TMP8049A/ TMP8039A			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
IDD	VDD Supply Current	-	10	15	-	15	20	mA
ICC+IDD	Total Supply Current	-	65	90	-	85	120	mA

AC CHARACTERISTICS

T_A=0°C to 70°C, V_{CC}=V_{DD}=+5V±10%, V_{SS}=0V, Unless Otherwise Noted.

SYMBOL	PARAMETER	TEST CONDITION	f (t)	11 MHz		UNIT
				MIN.	MAX.	
t	Clock Cycle Time		1/xtal f	90	1000	ns
tLL	ALE Pulse Width		3.5t-170	150	-	ns
tAL	Address Setup Time (ALE)		2t-110	70	-	ns
tLA	Address Hold Time (ALE)	CL=20pF	t-40	50	-	ns
tCC1	Control Pulse Width ($\overline{RD}$,$\overline{WR}$)		7.5t-200	480	-	ns
tCC2	Control Pulse Width ($\overline{PSEN}$)		6t-200	350	-	ns
tDW	Data Setup Time ($\overline{WR}$)		6.5t-200	390	-	ns
tWD	Data Hold Time ($\overline{WR}$)	CL=20pF	t-50	40	-	ns
tDR	Data Hold Time ($\overline{PSEN}$,$\overline{RD}$)	CL=20pF	1.5t-30	0	110	ns
tRD1	Data Input Read Time ($\overline{RD}$)		6t-170	-	375	ns
tRD2	Data Input Read Time ($\overline{PSEN}$)		4.5t-170	-	240	ns
tAW	Address Setup Time ($\overline{WR}$)		5t-150	300	-	ns
tAD1	Address Setup Time ($\overline{RD}$)		10.5t-220	-	730	ns
tAD2	Address Setup Time ($\overline{PSEN}$)		7.5t-200	-	460	ns
tAFC1	Address Float Time ($\overline{RD}$)	CL=20pF	2t-40	140	-	ns
tAFC2	Address Float Time ($\overline{PSEN}$)	CL=20pF	0.5t-40	10	-	ns
tLAFC1	ALE to Control Time ($\overline{RD}$,$\overline{WR}$)		3t-75	200	-	ns
tLAFC2	ALE to Control Time ($\overline{PSEN}$)		1.5t-75	60	-	ns
tCA1	Control to ALE Time ($\overline{RD}$,$\overline{WR}$,PROG)		t-65	25	-	ns
tCA2	Control to ALE Time ($\overline{PSEN}$)		4t-70	290	-	ns
tCY	Cycle Time		15t	1.36	15.0	us
tCP	Port Control Setup Time (PROG)		1.5t-80	50	-	ns
tPC	Port Control Hold Time (PROG)		4t-260	100	-	ns
tPR	Port 2 Input Data Set Time (PROG)		8.5t-120	-	650	ns

SYMBOL	PARAMETER	TEST CONDITION	f (t)	11 MHz		UNIT
				MIN.	MAX.	
tDP	Port2 Output Data Setup Time (PROG)		6t-290	250	-	ns
tPD	Port2 Output Data Hold Time (PROG)		1.5t-90	40	-	ns
tPF	Port 2 Input Data Hold Time (PROG)		1.5t	0	140	ns
tPP	PROG Pulse Width		10.5t-250	700	-	ns
tPL	Port2 I/O Data Setup Time(ALE)		4t-200	160	-	ns
tLP	Port2 I/O Data Hold Time (ALE)		0.5t-30	15	-	ns
tPV	Port Output Delay Time (ALE)		4.5t+100	-	510	ns
tOPRR	Output Clock Cycle Time (TO)		3t	270	-	ns

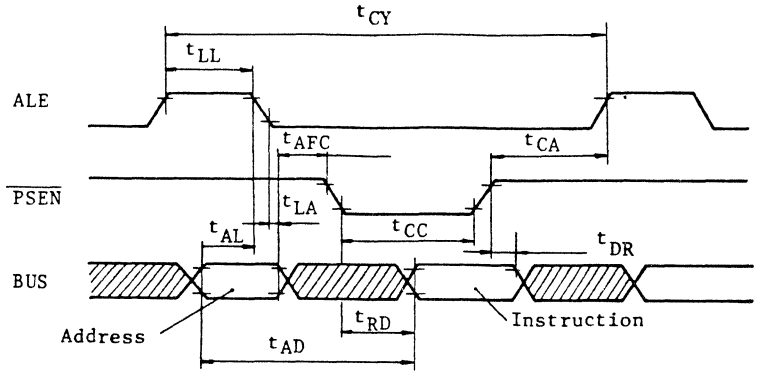
1. Control Outputs : CL=80pF, BUS Output : CL=150pF.

2. Address Float Time: BUS Hi-Impedance, CL=20pF

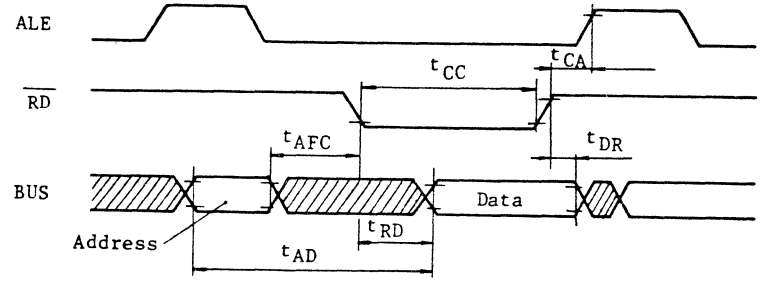
3. f(t): Assume the 50% duty clock is inputed to X1, X2.

TIMING WAVEFORM

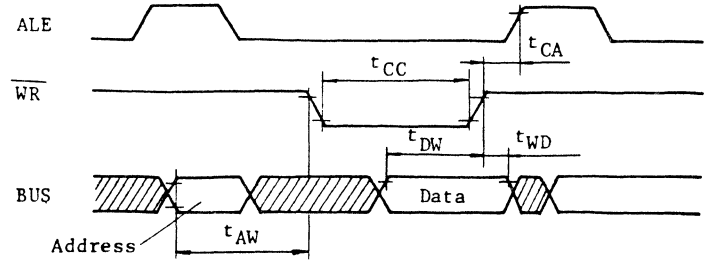
A. Instruction Fetch from External Program Memory



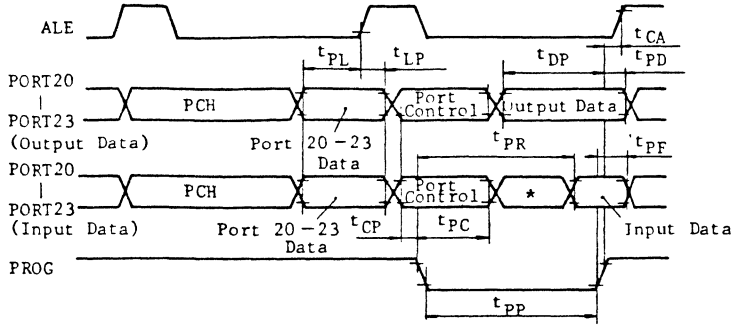
B. Read from External Data Memory



C. Write into External Data Memory

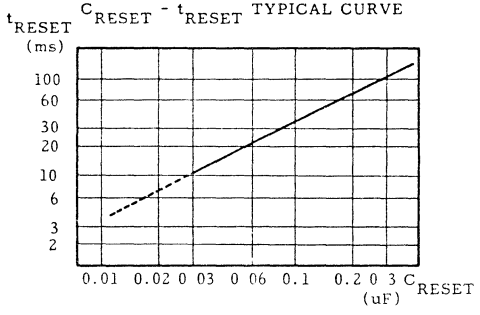


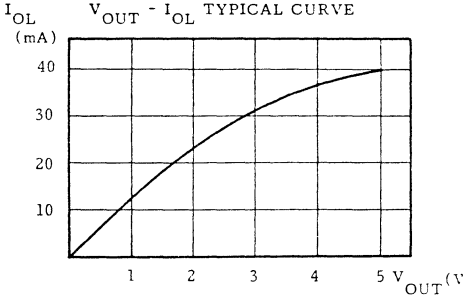
D. Timing of Port 2 during Expander Instruction Execution

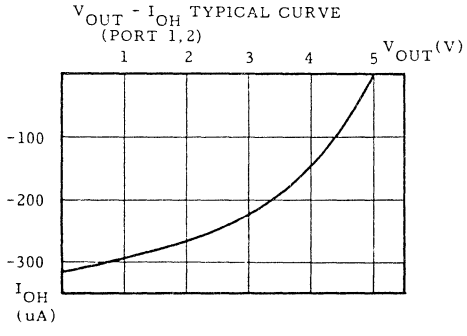


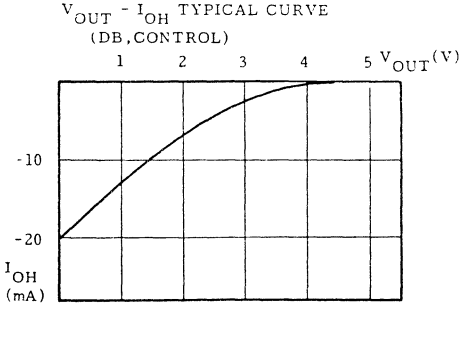
* Input Enabled State

TYPICAL CHARACTERISTICS





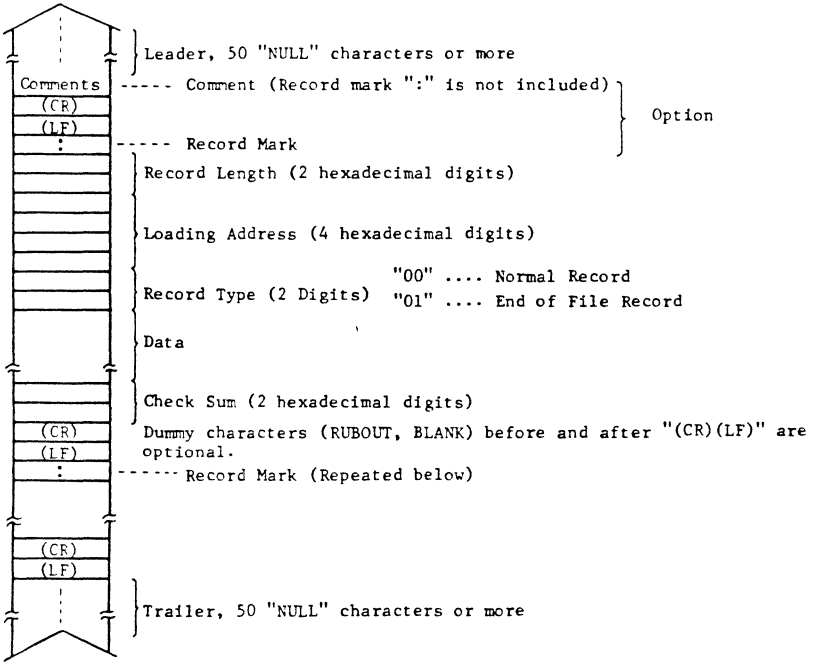




PROGRAM TAPE FORMAT

TMP8048A programs are delivered in the form of paper tape with the following format and it required to attach the tape list. The format of paper tape is same as the Intel type object tape (hexadecimal tape output by Intel MDS system, PROMPT 48 Development Tool, etc.)

(1) Tape Format



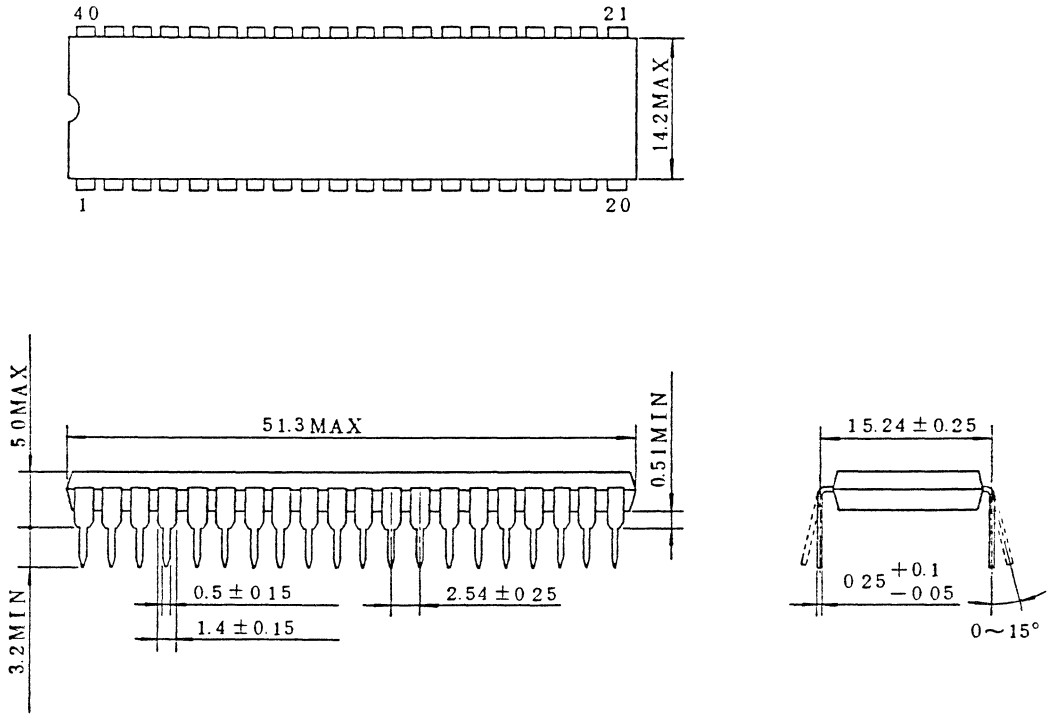
(2) Example of Tape List (TMP8048AP)

```
TOSHIBA MICRO COMPUTER TLCS-48
:100000000665C7D79CF50F3F951FED55A8FF16E570
:1000100088884DDE67D31F5D8ABA6DF292F113F5C1
:100020004FF1FB5DFFDAA96A99CF7DF94A346B7C09
:10003000197352F729F12F79AA9C057C5B851EED77
                    :
                    :
                    :
                    :
:1003C0005DFDB5E556A67277F61A51C631CF9F0E80
:1003D000BD2F6F20E8BB1977E3FB5AD1F41FDAA7E2
:1003E000B53D42E0EC32546025B7308CDD52063D1D
:1003F000B4BE9E9E345B6138060B20VC372BF60BD6
:00000001FF
```

OUTLINE DRAWING

TMP 8048AP / TMP 8035AP , TMP 8049AP / TMP 8039AP

Unit in mm



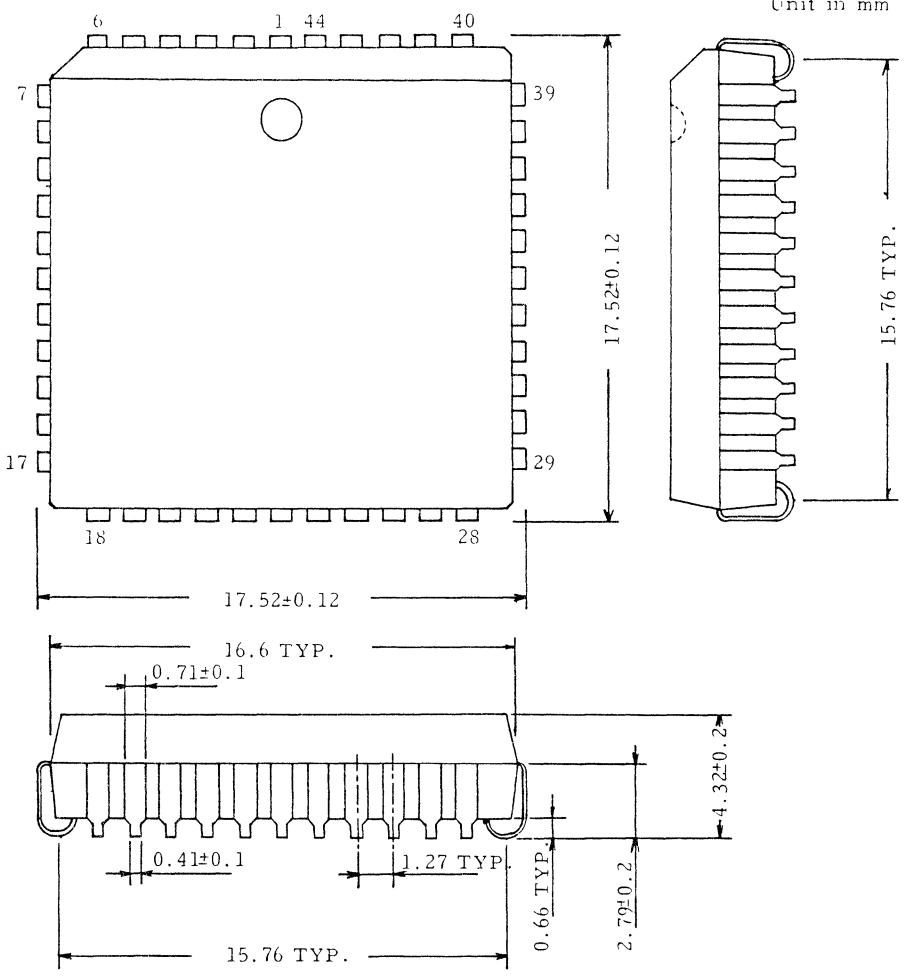
Note: 1. This dimension is measured at the center of bending point of leads.
2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoritical positions with respect to No.1 and No.40 leads.

OUTLINE DRAWING

TMP8048AT/TMP8035AT, TMP8049AT/TMP8039AT

PRELIMINARY

Unit in mm



8-BIT SINGLE-CHIP MICROCOMPUTER

TMP80C48AP/TMP80C48AP-6
TMP80C35AP/TMP80C35AP-6
TMP80C48AF/TMP80C48AF-6

GENERAL DESCRIPTION

The TMP80C48A is a single chip microcomputer fabricated in Silicon Gate CMOS technology which provides internal 8-bit parallel architecture.

The following basic architectural functions of a computer have been included in a single chip; an 8-bit CPU, 64 x 8 RAM data memory, 1K x 8 ROM program memory, 27 I/O lines and an 8-bit timer/event counter.

The TMP80C48A is particularly efficient as a controller. It has extensive bit handling capability as well as facilities for both binary and BCD arithmetic.

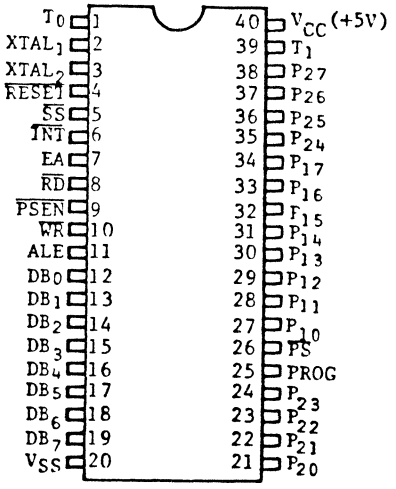
The TMP80C35AP/-6 is the equivalent of a TMP80C48AP/-6 without ROM program memory on chip. By using this device with external EPROM or RAM, software debugging becomes easy.

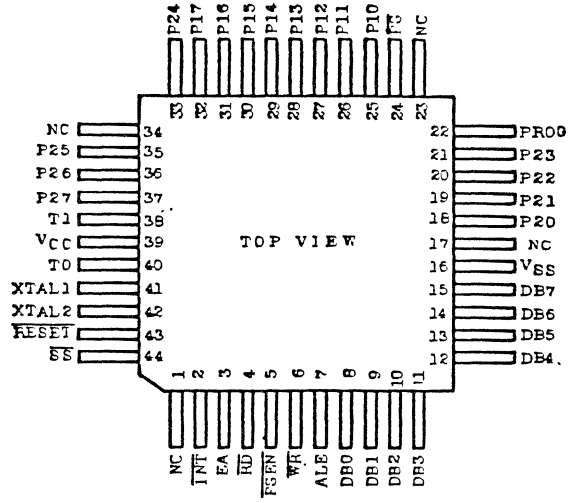
The TMP80C48AP/-6 and TMP80C35AP/-6 are in a standard Dual Inline Package.
The TMP80C48AF/-6 is in a 44-pin Flat Package.

FEATURES

.TMP80C48AP/TMP80C35AP/TMP80C48AF
  1.36μs Instruction Cycle Time
  0°C to 70°C, 5V ±10%
. TMP80C48AP-6/TMP80C35AP-6/TMP80C48AF-6
  2.5 μs Instruction Cycle Time
  -40°C to 85°C, 5V ±20%
. Software Upward Compatible with
  TMP8048A /INTEL's 8048
. HALT Instruction (Additional Instruction)
. 1K x 8 masked ROM
. 64 x 8 RAM
. 27 I/O lines
. Interval Timer/Event Counter
. Low Power
  10mA MAX. in Normal Operation
  (VCC=5V, fXTAL=6MHz)
  10μA Max. in Power Down Mode
  (VCC=5V, fXTAL : DC)
. Single Power Supply
. Power Down Mode (Stand-by Mode)
. Halt Mode (Idle Mode)

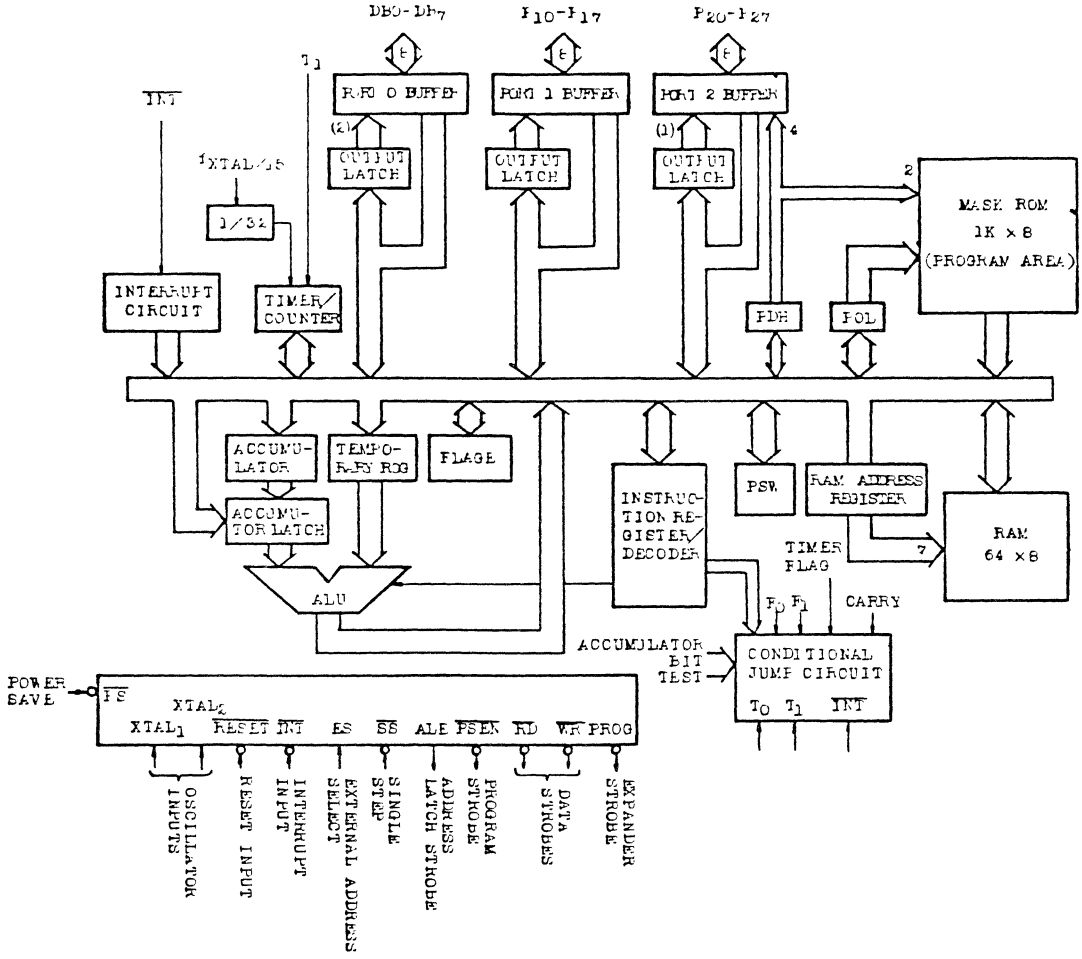
PIN CONNECTIONS (TOP VIEW)





NC: No Connection

BLOCK DIAGRAM



Note 1) The lower order 4 bit of port 2 output latch are used also for input/output operations with the I/O expander.

Note 2) The output latch of port 0 is also used for address output.

PIN NAMES AND PIN DESCRIPTION

VSS (Power Supply)
Circuit GND potential

VCC (Power Supply)
+5V during operation

$\overline{PS}$ (Input)
The control signal for the power saving at the power down mode (Active Low)

PROG (Output)
Output strobe for the TMP82C43P I/O expander.

P10 - P17 (Input/Output) Port 1
8-bit quasi-bidirectional port (Internal Pullup = 50KΩ).

P20 - P27 (Input/Output) Port 2
8-bit quasi-bidirectional port (Internal Pullup = 50KΩ).

P20 - P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for the TMP8243P.

DB0 - DB7 (Input/Output, Tri-State)
True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.

T0 (Input/Output)
Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.

T1 (Input)
Input pin testable using the JT1 and JNT1 instruction. Can be designated the event counter input using the timer/STRT CNT instruction.

$\overline{INT}$ (Input)
External interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)

$\overline{RD}$ (Output)
Output strobe activated during a Bus read. Can be used to enable data onto the Bus from an external device. Used as a Read Strobe to External Data Memory (Active Low).

$\overline{WR}$ (Output)
Output strobe during a Bus write (Active Low). Used as a Write Strobe to External Data Memory.

$\overline{\text{RESET}}$ (Input)
Active Low signal which is used to initialize the Processor. Also used during the power down mode.

ALE (Oupput)
Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.

$\overline{\text{PSEN}}$ (Output)
Program Store Enable. This output occurs only during a fetch to external program memory (Active Low).

$\overline{\text{SS}}$ (Input)
Single step input can be used in conjunction with ALE to "single step" processor through each instruction when $\overline{\text{SS}}$ is low the CPU is placed into a wait state after it has completed the instruction being executed. Also used during the power down mode.

EA (Input)
External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug and essential for testing and program verification. (Active High)

XTAL 1 (Input)
One side of crystal input for internal oscillator. Also input for external source.

XTAL 2 (Input)
Other side of crystal input.

TLCS-48 LIST OF INSTRUCTIONS (1/4)

Class	Assembler Mnemonic		Object Code (1st) (2nd) Bin.	Hex.	Function		Flag C, AC	Cycle
Accumulator Instruction	ADD	A, Rr	01101rrr	68+r	(A)←(A)+(Rr)	r=0~7	↕ ↕	1
	ADD	A, @Rr	0110000r	60+r	(A)←(A)+[(Rr)]	r=0,1	↕ ↕	1
	ADD	A, #i	00000011	03	(A)←(A)+i		↕ ↕	2
			iiiiiiii	ii				
	ADDC	A, Rr	01111rrr	78+r	(A)←(A)+(Rr)+(C)	r=0~7	↕ ↕	1
	ADDC	A, @Rr	0111000r	70+r	(A)←(A)+[(Rr)]+(C)	r=0,1	↕ ↕	1
	ADDC	A, #i	00010011	13	(A)←(A)+i+(C)		↕ ↕	2
			iiiiiiii	ii				
	ANL	A, Rr	01011rrr	58+r	(A)←(A) ∧(Rr)	r=0~7		1
	ANL	A, @Rr	0101000r	50+r	(A)←(A) ∧[(Rr)]	r=0,1		1
	ANL	A, #i	01010011	53	(A)←(A) ∧i			2
			iiiiiiii	ii				
	ORL	A, Rr	01001rrr	48+r	(A)←(A) ∨(Rr)	r=0~7		1
	ORL	A, @Rr	0100000r	40+r	(A)←(A) ∨[(Rr)]	r=0,1		1
	ORL	A, #i	01000011	43	(A)←(A) ∨i			2
			iiiiiiii	ii				
	XRL	A, Rr	11011rrr	D8+r	(A)←(A) ∀(Rr)	r=0~7		1
	XRL	A, @Rr	1101000r	D0+r	(A)←(A) ∀[(Rr)]	r=0,1		1
	XRL	A, #i	11010011	D3	(A)←(A) ∀i			2
			iiiiiiii	ii				
	INC	A	00010111	17	(A)←(A)+1			1
	DEC	A	00000111	07	(A)←(A)-1			1
	CLR	A	00100111	27	(A)←0			1
	CPL	A	00110111	37	(A)←NOT(A)			1
	DA	A	01010111	57	(A)←(A)BCD		↕	1
	SWAP	A	01000111	47	(A)<7:4> ↔(A)<3:0>			1
	RL	A	11100111	E7	(A)<n+1> ←(A)<n>			1
					(A)<0> ←(A)<7>	n=0~6		
	RLC	A	11110111	F7	(A)<n+1> ←(A)<n>		↕	1
					(C)←(A)<7>			
					(A)<0> ←(C)	n=0~6		
	RR	A	01110111	77	(A)<n> ←(A)<n+1>	n=0~6		1
					(A)<7> ←(A)<0>			
	RRC	A	01100111	67	(A)<n> ←(A)<n+1>		↕	1
					(C)←(A)<0>			
					(A)<7> ←(C)	n=0~6		
I/O Instruction	IN	A, Pd	000010pp	08+p	(A)←(Pp)	P=1,2		2

TLCS-48 LIST OF INSTRUCTIONS (2/4)

Class	Assembler Mnemonic		Object Code (1st) (2nd) Bin.	Hex.	Function		Flag C, AC	Cycle
INPUT/OUTPUT Instruction	OUTL	Pp, A	001110pp	38+p	(Pp) ←(A)	P=1,2		2
	ANL	Pp, #i	100110pp	98+p	(Pp) ←(Pp)∧i	P=1,2		2
			iiiiiiii	ii				
	ORL	Pp, #i	100010pp	88+p	(Pp) ←(Pp)∨i	P=1,2		2
			iiiiiiii	ii				
	INS	A, BUS	00001000	08	(A)←(BUS)			2
	OUTL	BUS, A	00000010	02	(BUS)←(AC)			2
	ANL	BUS, #i	10011000	98	(BUS)←(BUS) ∧i			2
			iiiiiiii	ii				
	ORL	BUS, #i	10001000	88	(BUS)←(BUS) ∨i			2
			iiiiiiii	ii				
	MOVD	A, Pp	000011pp	0C+p	(A)<3:0> ←(Pp)	p=4~7		2
					(A)<7:4> ←0			
	MOVD	Pp, A	001111pp	3C+p	(Pp) ←(A)<3:0>	p=4~7		2
	ANLD	Pp, A	100111pp	9C+p	(Pp) ←(Pp)∧(A)<3:0>	p=4~7		2
	ORLD	Pp, A	100011pp	8C+p	(Pp) ←(Pp)∨(A)<3:0>	p=4~7		2
(1)	INC	Rr	00011rrr	18+r	(Rr) ←(Rr)+1	r=0~7		1
	INC	@Rr	0001000r	10+r	[(Rr)] ←[(Rr)]+1	r=0,1		1
	DEC	Rr	11001rrr	C8+r	(Rr) ←(Rr)-1	r=0~7		1
Branch Instruction	JMP	a	aH00100 aHL	aH+4	(PC)<10:0> ←a (PC)<11> ←(DBF).			2
	JMPP	@A	10110011	B3	(PC)<7:0>←PRO[(PC)<11:8>・(A)]			2
	DJNZ	Rr, a	11101rrr aHL	E8+r	(Rr) ←(Rr)-1 if(Rr) ≠0then(PC)<7:0>←aHL else no operation	r=0~7		2
	JC	a	11110110 aHL	F6	if(C)=1 then(PC)<7:0>←aHL else no operation			2
	JNC	a	11100110 aHL	E6	if(C)=0 then(PC)<7:0>←aHL else no operation			2
	JZ	a	11000110 aHL	C6	if(A)=0 then(PC)<7:0>←aHL else no operation			2
	JNZ	a	10010110 aHL	96	if(A)≠0 then(PC)<7:0> ←aHL else no operation			2
	JTO	a	00110110 aHL	36	if TO=1 then(PC)<7:0>←aHL else no operation			2

(1) ····· Register Instruction

TLCS-48 LIST OF INSTRUCTIONS (3/4)

Clas	Assembler Mnemonic		Object Code (1st) (2nd) Bin	Hex	Function	Flag C,AC	Cycle
Branch Instruction	JNTO	a	00100110 aML	26	if T0=0 then(PC)<7:0>←aML else no operation		2
	JT1	a	01010110 aML	56	if T1=1 then(PC)<7:0>←aML else no operation		2
	JNT1	a	01000110 aML	46	if T1=0 then(PC)<7:0>←aML else no operation		2
	JF0	a	10110110 aML	B6	if F0=1 then(PC)<7:0>←aML else no operation		2
	JF1	a	01110110 aML	76	if F1=1 then(PC)<7:0>←aML else no operation		2
	JTF	a	00010110 aML	16	if TF=1 then(PC)<7:0>←aML else no operation		2
	JNI	a	10000110 aML	86	if INT =0 then(PC)<7:0>←aML else no operation		2
	JBb	a	bbb10010 aML	b*12	if (A)<b>=1 then (PC)<7:0>←aML else no operation b=0~7		2
(2)	CALL	a	aH10100 aML	aH*14	[(SP)] ←(PSW)<7:4>・(PC) (SP) ←(SP)+1 (PC)<10:0> ←a (PC)<11> ←(DBF)		2
	RET		10000011	83	(SP) ←(SP)-1 (PC) ←[(SP)]<11:0>		2
	RETR		10010011	93	(SP) ←(SP)-1 (PC) ←[(SP)]<11:0> (PSW)<7:4> ←[(SP)]<15:12>	↕↕	2
(3)	CLR	C	10010111	97	(C)←0		1
	CPL	C	10100111	A7	(C)←NOT(C)		1
	CLR	F0	10000101	85	(F0) ←0		1
	CPL	F0	10010101	95	(F0) ←NOT(F0)		1
	CLR	F1	10100101	A5	(F1) ←0		1
	CPL	F1	10110101	B5	(F1) ←NOT(F1)		1
(4)	MOV	A , Rr	11111rrr	F8+r	(A)←(Rr) r=0~7		1
	MOV	A ,@Rr	1111000r	F0+r	(A)←[(Rr)] r=0,1		1
	MOV	A ,#i	00100011 iiiiiiii	23 ii	(A) ←i		2
	MOV	Rr, A	10101rrr	A8+r	(Rr)←(A) r=0~7		1
	MOV	@Rr, A	1010000r	A0+r	[(Rr)]←(A) r=0,1		1

(2) ····· Subroutine Instruction (3) ····· Flag Instruction
(4) ····· Move Instruction

TLCS-48 LIST OF INSTRUCTIONS (4/4)

Class	Assembler Mnemonic		Object Code (1st) (2nd) Bin.	Hex.	Function	Flag C,AC	Cycle
Move Instruction	MOV	Rr,#i	10111rrr iiiiiiii	B8+r ii	(Rr)←i r=0~7		2
	MOV	@Rr,#i	1011000r iiiiiiii	B0+r ii	[(Rr)]←i r=0,1		2
	MOV	A,PSW	11000111	C7	(A) ←(PSW)		1
	MOV	PSW,A	11010111	D7	(PSW) ←(A)		1
	XCH	A,Rr	00101rrr	28+r	(A) ↔(Rr) r=0~7		1
	XCH	A,@Rr	0010000r	20+r	(A) ↔[(Rr)] r=0,1		1
	XCHD	A,@Rr	0011000r	30+r	(A)<3:0>↔[(Rr)<3:0>] r=0,1		1
	MOVX	@Rr,A	1001000r	90+r	[XT[(Rr)] ←(A) r=0,1		1
	MOVX	A,@Rr	1000000r	80+r	(A) ←EXT[(Rr)] r=0,1		1
	MOVP	A,@A	10100011	A3	(A) ←PRO[(PC)<11:8>・(A)]		1
	MOVP3	A,@A	11100011	E3	(A) ←PR0[(PC)<11>・011・(A)]		1
TC io mu en rt o r	MOV	A,T	01000010	42	(A) ←(TR)		1
	MOV	T,A	01100010	62	(TR)←(A)		1
	STRT	T	01010101	55	Start Timer		1
	STRT	CNT	01000101	45	Start counter		1
	STOP	TCNT	01100101	65	Stop Timer/Counter		1
	EN	TCNTI	00100101	25	Enable Timer/Counter Interrupt		1
	DIS	TCNTI	00110101	35	Disable Timer/Counter Interrupt		1
(5)							
Control Instruction	EN	I	00000101	05	Enable External Interrupt		1
	DIS	I	00010101	15	Disable External Interrupt		1
	SEL	RB0	11000101	C5	(BS)← 0		1
	SEL	RB1	11010101	D5	(BS)← 1		1
	SEL	MB0	11100101	E5	(DBF) ← 0		1
	SEL	MB1	11110101	F5	(DBF) ← 1		1
	ENTO	CLK	01110101	75	Enable Clock Output on T0		1
	HALT		00000001	01	Halt		1
(6)	NOP		00000000	00	no opration		1

(5) ····· A/D Converter Instruction (6) ····· Other

TMP80C48AP/TMP80C35AP/TMP80C48AF ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
VCC	VCC Supply Voltage (with respect to GND (VSS))	-0.5V to +7V
VINA	Input Voltage (Except EA)	-0.5V to VCC+0.5V
VINB	Input Voltage (Only EA)	-0.5V to 13V
PD	Power Dissipation (Ta=70°C)	250mW
TSOLDER	Soldering Temperature (Soldering Timer 10 sec)	260°C
TSTG	Storage Temperature	-65°C to 150°C
TOPR	Operating Temperature	0°C to 70°C

DC CHARACTERISTICS

TOPR=0°C to 70°C, VCC=+5V±10%, VSS=0V, unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage (Except XTAL1, XTAL2, RESET)			-0.5	-	0.8	V
VIL1	Input Low Voltage (XTAL1, XTAL2, RESET)			-0.5	-	0.6	V
VIH	Input High Voltage (Except XTAL1, XTAL2, RESET, PS)			2.2	-	VCC	V
VIH1	Input High Voltage (Except XTAL1, XTAL2, RESET, PS)			0.7 x VCC	-	VCC	V
VOL	Output Low Voltage (Except P10-P17, P20-P27)		IOL=1.6mA	-	-	0.45	V
VOL1	Output Low Voltage (P10-P17, P20-P27)		IOL=1.2mA	-	-	0.45	V
VOH11	Output High Voltage (Except P10-P17, P20-P27)		IOH=-1.6mA	2.4	-	-	V
VOH12	Output High Voltage (Except P10-P17, P20-P27)		IOH=-400μA	VCC-0.8	-	-	V
VOH21	Output High Voltage (P10-P17, P20-P27)		IOH=-50μA	2.4	-	-	V
VOH22	Output High Voltage (P10-P17, P20-P27)		IOH=-25μA	VCC-0.8	-	-	V
ILI	Input Leak Current (T1, INT, EA, PS)		VSS≦VIN≦VCC	-	-	±10	μA
ILI1	Input Leak Current (SS, RESET)		VSS≦VIN≦VCC	-	-	-50	μA
ILI2	Input Leak Current (P10-P17, P20-P27)		VSS+0.45V≦VIN≦VCC	-	-	-500	μA
ILO	Output Leak Current (BUS, TO) (High impedance condition)		VSS+0.45V≦VIN≦VCC	-	-	±10	μA
ICC1	VCC Supply Current	Normal operation	VCC=5V, fXTAL=6MHz VIH=VCC-0.2V	-	-	10	mA
ICCH1		HALT Mode	VIL=0.2V	-	-	2.5	
ICC2	VCC Supply Current	Normal operation	VCC=5V, fXTAL=11MHz	-	-	15	mA
ICCH2		HALT Mode	VIH=VCC-0.2V VIL=0.2V	-	-	4.0	

TMP80C48AP/TMP80C35AP/TMP80C48AF

AC CHARACTRISTICS

TOPR=0°C to 70°C, VCC=+5V±10%, VSS=0V, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITION	f(t)	11 MHz		UNIT
				MIN.	MAX.	
t	Clock Period	Note 2	1/xtal f	90.9	1000	ns
tLL	ALE Pulse Width		3.5t-170	150	-	ns
tAL	Address Setup Time (ALE)		2t-110	70	-	ns
tLA	Address Hold Time (ALE)	CL=20pF	t-40	50	-	ns
tCC1	Control Pulse Width ($\overline{RD}$, $\overline{WR}$)		7.5t-200	480	-	ns
tCC2	Control Pulse Width ($\overline{PSEN}$)		6t-200	350	-	ns
tDW	Data Setup Time ($\overline{WR}$)		6.5t-200	390	-	ns
tWD	Data Hold Time ($\overline{WR}$)	CL=20pF	t-50	40	-	ns
tDR	Data Hold Time ($\overline{RD}$, $\overline{PSEN}$)	CL=20pF	1.5t-30	0	110	ns
tRD1	Data Input Read Time ($\overline{RD}$)		6t-170	-	375	ns
tRD2	Data Input Read Time ($\overline{PSEN}$)		4.5t-170	-	240	ns
tAW	Address Setup Time ($\overline{WR}$)		5t-150	300	-	ns
tAD1	Address Setup Time ($\overline{RD}$)		10.5t-220	-	730	ns
tAD2	Address Setup Time ($\overline{PSEN}$)		7.5t-200	-	460	ns
tAFC1	Address Float Time ($\overline{RD}$, $\overline{WR}$)	CL=20pF	2t-40	140	-	ns
tAFC2	Address Float Time ($\overline{PSEN}$)	CL=20pF	0.5t-40	10	-	ns
tLAFC1	ALE to Control Time ($\overline{RD}$, $\overline{WR}$)		3t-75	200	-	ns
tLAFC2	ALE to Control Time ($\overline{PSEN}$)		1.5t-75	60	-	ns
tCA1	Control to ALE Time ($\overline{RD}$, $\overline{WR}$, PROG)		t-65	25	-	ns
tCA2	Control to ALE Time ($\overline{PSEN}$)		4t-70	290	-	ns
tCP	Port Control Setup Time (PROG)		1.5t-80	50	-	ns
tPC	Port Control Hold Time (PROG)		4t-260	100	-	ns
tPR	Port 2 Input Data Setup Time (PROG)		8.5t-120	-	650	ns
tPF	Port 2 Input Data Hold Time (PROG)		1.5t	0	140	ns
tDP	Port 2 Output Data Setup Time (PROG)		6t-290	250	-	ns
tPD	Port 2 Output Data Hold Time (PROG)		1.5t-90	40	-	ns

TMP80C48AP/TMP80C35AP/TMP80C48AF

AC CHARACTRISTICS (CONTINUE)
TOPR=0°C to 70°C, VCC=+5V±10%, VSS=0V, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITION	f(t)	11 MHz		UNIT
				MIN.	MAX.	
tPP	PROG Pulse Width		10.5t-250	700	-	ns
tPL	Port 2 I/O Data Setup Time(ALE)		4t-200	160	-	ns
tLP	Port 2 I/O Data Hold Time (ALE)		1.5t-120	15	-	ns
tPV	Poer Output Delay Time (ALE)		4.5t+100	-	510	ns
tOPRR	TO Clock Period		3t	270	-	ns
tCY	Cycle Time		15t	1.36	15.0	μs

Note : 1. Control Output CL=80pF. BUS Output CL=150pF.
2. The f(t) assumes 50% duty cycle on XTAL1 and XTAL2.
The Max. Clock frequency is 11MHz. and the Min. Clock frequency is 1MHz.

TMP80C48AP-6/TMP80C35AP-6/TMP80C48AF-6 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
VCC	VCC Supply Voltage (with respect to GND (VSS))	-0.5V to +7V
VINA	Input Voltage (Except EA)	-0.5V to VCC+0.5V
VINB	Input Voltage (Only EA)	-0.5V to 13V
PD	Power Dissipation (Ta=85°C)	250mW
TSOLDER	Soldering Temperature (Soldering Timer 10 sec)	260°C
TSTG	Storage Temperature	-65°C to 150°C
TOPR	Operating Temperature	-40°C to 85°C

DC CHARACTERISTICS (I)

TOPR = -40°C to 85°C, VCC=+5V±10%, VSS=0V, unless otherwise noted

SYMBOL	PARAMETER		TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage			-0.5	-	0.8	V
VIH	Input High Voltage (Except XTAL1, XTAL2, $\overline{RESET}$, $\overline{PS}$)			2.2	-	VCC	V
VIH1	Input High Voltage ($\overline{XTAL1}$, XTAL2, $\overline{RESET}$, $\overline{PS}$)			0.7 x VCC	-	VCC	V
VOL	Output Low Voltage (Except P10-P17, P20-P27)		IOL=1.6mA	-	-	0.45	V
VOL1	Output Low Voltage (P10-P17, P20-P27)		IOL=1.2mA	-	-	0.45	V
VOH11	Output High Voltage (Except P10-P17, P20-P27)		IOH=-1.6mA	2.4	-	-	V
VOH12	Output High Voltage (Except P10-P17, P20-P27)		IOH=-400μA	VCC-0.8	-	-	V
VOH21	Output High Voltage (P10-P17, P20-P27)		IOH=-50μA	2.4	-	-	V
VOH22	Output High Voltage (P10-P17, P20-P27)		IOH=-25μA	VCC-0.8	-	-	V
ILI	Input Leak Current ($\overline{T1}$, $\overline{INT}$, $\overline{EA}$, $\overline{PS}$)		VSS≦VIN≦VCC	-	-	±10	μA
ILI1	Input Leak Current ($\overline{SS}$, $\overline{RESET}$)		VSS≦VIN≦VCC	-	-	-50	μA
ILI2	Input Leak Current (P10-P17, P20-P27)		VSS+0.45V≦VIN≦VCC	-	-	-500	μA
ILO	Output Leak Current (BUS, TO) (High impedance condition)		VSS+0.45V≦VIN≦VCC	-	-	±10	μA
ICC1	VCC Supply Current	Normal operation	VCC=5V, fXTAL=6MHz VIH=VCC-0.2V	-	-	10	mA
ICCH1		HALT Mode	VIL=0.2V	-	-	2.5	

TMP80C48AP-6/TMP80C35AP-6/TMP80C48AF-6 ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (II)

TOPR=-40°C to 85°C, VCC=+5V±20%, VSS=0V, unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage			-0.5	-	0.15 x VCC	V
VIH	Input High Voltage (Except XTAL1, XTAL2, RESET, PS)			0.5 x VCC	-	VCC	V
VIH1	Input High Voltage (XTAL1, XTAL2, RESET, PS)			0.7 x VCC	-	VCC	V
VOL	Output Low Voltage (Except P10-P17, P20-P27)		IOL=1.6mA	-	-	0.45	V
VOL1	Output Low Voltage (P10-P17, P20-P27)		IOL=1.2mA	-	-	0.45	V
VOH12	Output High Voltage (Except P10-P17, P20-P27)		IOH=-400μA	VCC-0.8	-	-	V
VOH22	Output High Voltage (P10-P17, P20-P27)		IOH=-25μA	VCC-0.8	-	-	V
ILI	Input Leak Current (T1, INT, EA, PS)		VSS≦VIN≦VCC	-	-	±10	μA
ILI1	Input Leak Current (SS, RESET)		VSS≦VIN≦VCC	-	-	-VCC/0.1	μA
ILI2	Input Leak Current (P10-P17, P20-P27)		VSS+0.45V≦VIN≦VCC	-	-	-VCC/0.01	μA
ILO	Output Leak Current (BUS, TO) (High impedance condition)		VSS+0.45V≦VIN≦VCC	-	-	±10	μA
ICC1	VCC Supply Current	Normal Operation	VCC=5V, fXTAL=6MHz VIH=VCC-0.2V, VIH=0.2V	-	-	10	mA
ICCH1		HALT Mode		-	-	2.5	

TMP80C48AP-6/TMP80C35AP-6/TMP80C48AF-6

AC CHARACTRISTICS

TOPR=-40°C to 85°C, VCC=+5V±20%, VSS=0V, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITION	f(t)	6 MHz		UNIT
				MIN.	MAX.	
t	Clock Period	Note 2	1/xtal f	166.6	1000	ns
tLL	ALE Pulse Width		3.5t-170	410	-	ns
tAL	Address Setup Time (ALE)		2t-110	220	-	ns
tLA	Address Hold Time (ALE)	CL=20pF	t-40	120	-	ns
tCC1	Control Pulse Width ($\overline{RD}$, $\overline{WR}$)		7.5t-200	1050	-	ns
tCC2	Control Pulse Width ($\overline{PSEN}$)		6t-200	800	-	ns
tDW	Data Setup Time ($\overline{WR}$)		6.5t-200	880	-	ns
tWD	Data Hold Time ($\overline{WR}$)	CL=20pF	t-50	120	-	ns
tDR	Data Hold Time ($\overline{RD}$, $\overline{PSEN}$)	CL=20pF	1.5t-30	0	220	ns
tRD1	Data Input Read Time ($\overline{RD}$)		6t-170	-	830	ns
tRD2	Data Input Read Time ($\overline{PSEN}$)		4.5t-170	-	580	ns
tAW	Address Setup Time ($\overline{WR}$)		5t-150	680	-	ns
tAD1	Address Setup Time ($\overline{RD}$)		10.5t-220	-	1530	ns
tAD2	Address Setup Time ($\overline{PSEN}$)		7.5t-200	-	1050	ns
tAFC1	Address Float Time ($\overline{RD}$, $\overline{WR}$)	CL=20pF	2t-40	290	-	ns
tAFC2	Address Float Time ($\overline{PSEN}$)	CL=20pF	0.5t-40	40	-	ns
tLAFC1	ALE to Control Time ($\overline{RD}$, $\overline{WR}$)		3t-75	420	-	ns
tLAFC2	ALE to Control Time ($\overline{PSEN}$)		1.5t-75	175	-	ns
tCA1	Control to ALE Time ($\overline{RD}$, $\overline{WR}$, PROG)		t-65	100	-	ns
tCA2	Control to ALE Time ($\overline{PSEN}$)		4t-70	590	-	ns
tCP	Port Control Setup Time (PROG)		1.5t-80	170	-	ns
tPC	Port Control Hold Time (PROG)		4t-260	400	-	ns
tPR	Port 2 Input Data Setup Time (PROG)		8.5t-120	-	1290	ns
tPF	Port 2 Input Data Hold Time (PROG)		1.5t	0	250	ns
tDP	Port 2 Output Data Setup Time (PROG)		6t-290	710	-	ns
tPD	Port 2 Output Data Hold Time (PROG)		1.5t-90	160	-	ns

TMP80C48AP-6/TMP80C35AP-6/TMP80C48AF-6

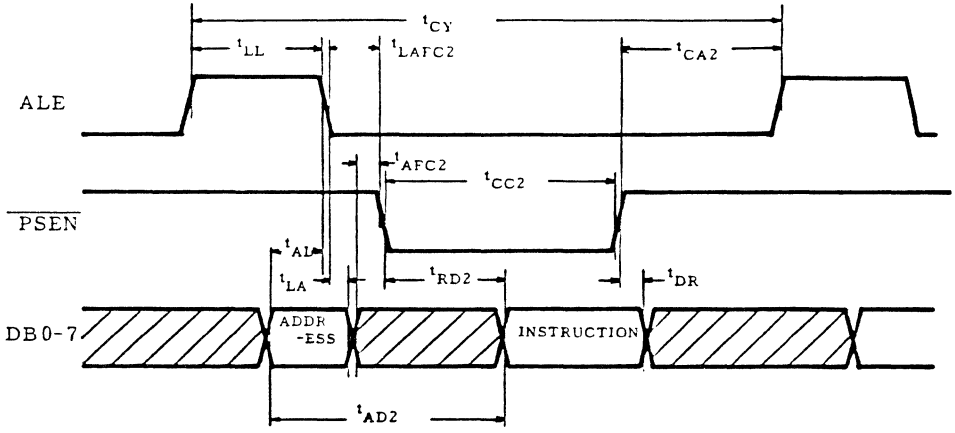
AC CHARACTRISTICS (CONTINUE)
TOPR=-40°C to 85°C, VCC=+5V±20%, VSS=0V, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITION	f(t)	6 MHz		UNIT
				MIN.	MAX.	
tPP	PROG Pulse Width		10.5t-250	1500	-	ns
tPL	Port 2 I/O Data Setup Time(ALE)		4t-200	460	-	ns
tLP	Port 2 I/O Data Hold Time (ALE)		0.5t-30	130	-	ns
tPV	Port Output Delay Time (ALE)		4.5t+100	-	850	ns
tOPRR	TO Clock Period		3t	500	-	ns
tCY	Cycle Time		15t	2.5	15.0	μs

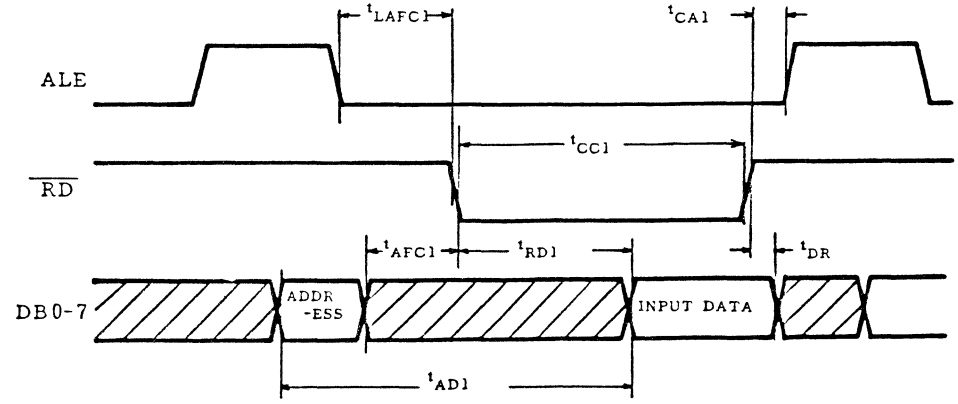
Note : 1. Control Output CL=80pF. BUS Output CL=150pF.
2. The f(t) assumes 50% duty cycle on XTAL1 and XTAL2.
The Max. Clock frequency is 6MHz. and the Min. Clock frequency is 1MHz.

TIMING WAVEFORM

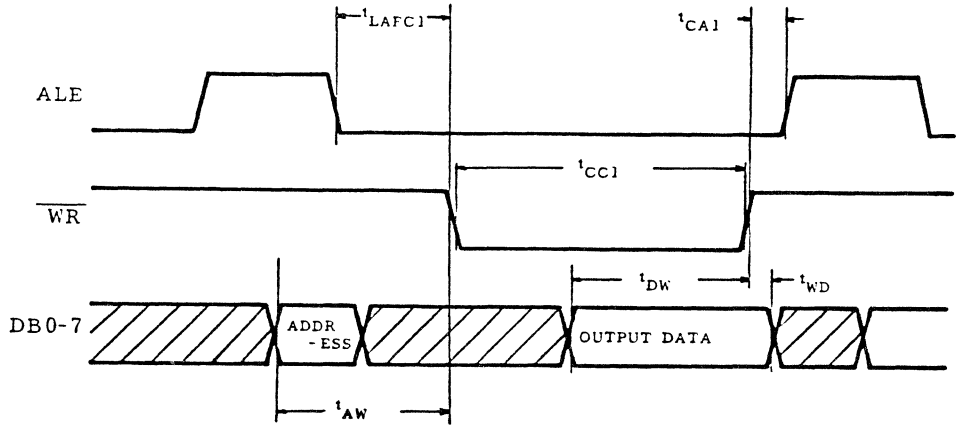
A. Instruction Fetch from External Program Memory



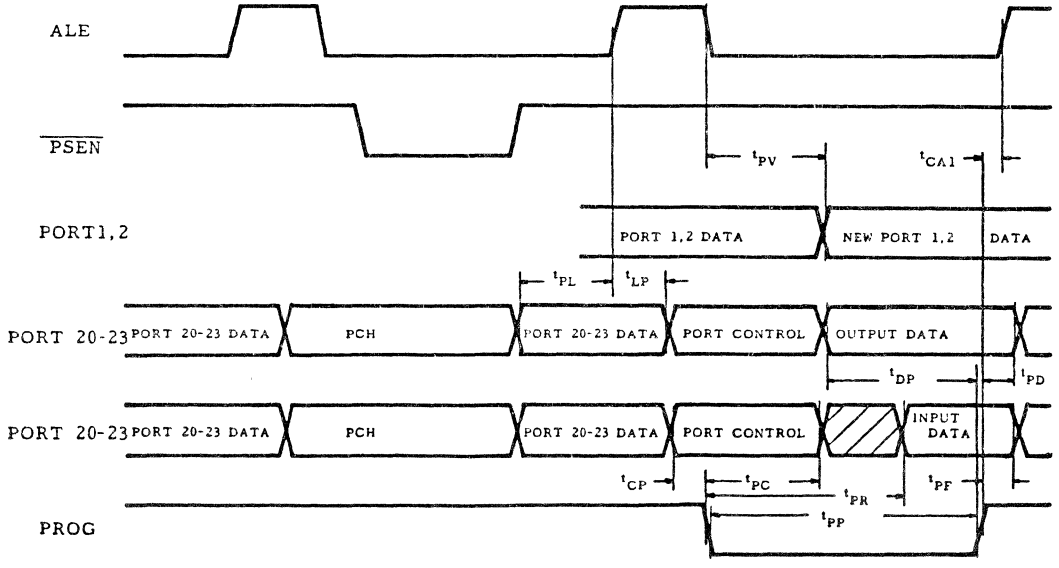
B. Read from External Data Memory



C. Write into External Data Memory



D. Timing of Port 2 during Expander Instruction Execution



POWER DOWN MODE (I) ..... Data Hold Mode in RAM

The operation of oscillation circuit is suspended by setting $\overline{PS}$ terminal to low level after $\overline{RESET}$ terminal has been set to low level. Consequently, all the data in RAM area can be held in low power consumption.

The minimum hold voltage of VCC in this mode is 2V.

$\overline{PS}$ terminal is set to high level to resume oscillation after VCC has been reset to 5V, and then $\overline{RESET}$ terminal is set to high level, thus, the normal mode is restarted from the initialize operation (address 0).

DC CHARACTERISTICS

TMP80C48AP/TMP80C35AP/TMP80C48AF : TOPR=0°C to 70°C, VSS=0V
TMP80C48AP-6/TMP80C35AP-6/TMP80C48AF-6 : TOPR=-40°C to 85°C, VSS=0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VSB1	Standby Voltage(1)		2.0	-	6.0	V
ISB1	Standby Current(1)	VCC=5V, VIH=VCC-0.2V, VIL=0.2V	-	0.5	10	μA

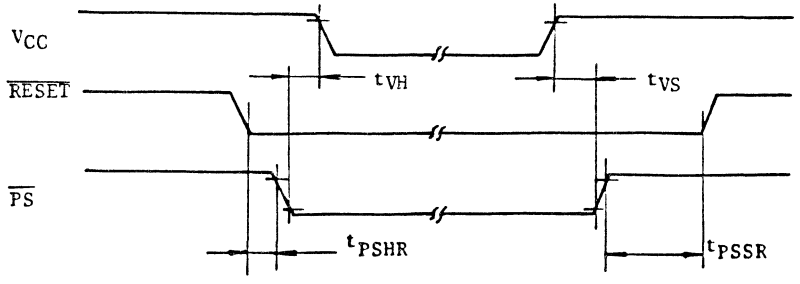
DC CHARACTERISTICS

TMP80C48AP/TMP80C35AP/TMP80C48AF : TOPR= 0°C to 70°C, VCC=5V±10%, VSS=0V
TMP80C48AP-6/TMP80C35AP-6/TMP80C48AF-6 : TOPR=-40°C to 85°C, VCC=5V±20%, VSS=0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
tPSHR	Power Save Hold Time ($\overline{RESET}$)		10	-	-	μS
tPSSR	Power Save Setup Time ($\overline{RESET}$)		10	-	-	mS
tVH	VCC Hold Time ($\overline{PS}$)		5	-	-	μS
tVS	VCC Setup Time ($\overline{PS}$)		5	-	-	μS

Note: tCY=2.5μS (fXTAL=6MHz)

TIMING WAVEFORM



POWER DOWN MODE (II) ..... ALL Data Hold Mode

The operation of oscillation circuit is suspended by setting $\overline{PS}$ terminal to low level after $\overline{SS}$ terminal has been set to low level. Consequently, all data can be held in low power consumption.

The minimum hold voltage of VCC in this mode is 3V.

$\overline{PS}$ terminal is set to high level to resume oscillation after VCC has been reset to 5V, and then $\overline{SS}$ terminal is set to high level, thus, the normal mode is restarted continuously from the state just before the power down mode (II).

DC CHARACTERISTICS

TMP80C48AP/TMP80C35AP/TMP80C48AF : TOPR=0°C to 70°C, VSS=0V
TMP80C48AP-6/TMP80C35AP-6/TMP80C48AF-6 : TOPR=-40°C to 85°C, VSS=0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VSB2	Standby Voltage(2)		3.0	-	6.0	V
ISB2	Standby Current(2)	VCC=5V, VIH=VCC-0.2V, VIL=0.2V	-	0.5	10	μA

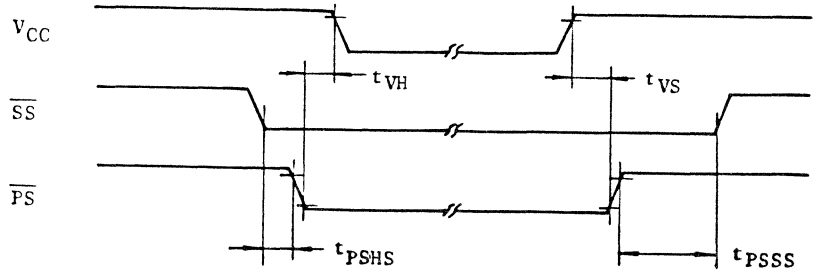
AC CHARACTERISTICS

TMP80C48AP/TMP80C35AP/TMP80C48AF : TOPR= 0°C to 70°C, VSS=5V±10%, VSS=0V
TMP80C48AP-6/TMP80C35AP-6/TMP80C48AF-6 : TOPR=-40°C to 85°C, VCC=5V±20%, VSS=0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
tPSHS	Power Save Hold Time ($\overline{SS}$)		10	-	-	μS
tPSSS	Power Save Setup Time ($\overline{SS}$)		10	-	-	mS
tVH	VCC Hold Time ($\overline{PS}$)		5	-	-	μS
tVS	VCC Setup Time ($\overline{PS}$)		5	-	-	μS

Note: tCY=2.5μS (fXTAL=6MHz)

TIMING WAVEFORM



HALT MODE

. 1 HALT INSTRUCTION

OP code is "01H". HALT INSTRUCTION is an additional instruction to the standard 8048/8049 instruction set.

. 2 Entry to HALT MODE

On the execution of HALT INSTRUCTION, TMP80C48A/TMP80C35A enter HALT MODE.

. 3 Status in HALT MODE

The oscillator continues its operation, however, the internal clocks and internal logic values just prior to the execution of HALT INSTRUCTION are maintained. Power consumption in HALT MODE is less than 50% of normal operation. The status of each pins are described in the following table.

. 4 Release from HALT MODE

HALT MODE is released by either of two signals ($\overline{\text{RESET}}$, $\overline{\text{INT}}$).

(1) $\overline{\text{RESET}}$ Release Mode : An active $\overline{\text{RESET}}$ input signal causes the normal reset function. TMP80C48A/TMP80C35A start the program at address "000 H".

(2) $\overline{\text{INT}}$ Release Mode : An active $\overline{\text{INT}}$ input signal causes the normal operation.

In case of interrupt enable mode (EI MODE), TMP80C48A/TMP80C35A execute the interrupt service routine, after the execution of one instruction which is located at the next address after HALT INSTRUCTION.

In case of interrupt disable mode (DI MODE), TMP80C48A/TMP80C35A execute normal operation from the next address after HALT INSTRUCTION.

. 5 Supply Voltage Range in HALT MODE

The operating supply voltage range and the operating temperature range are same as in normal operation.

PIN STATUS IN POWER DOWN MODE (I) (II)

PIN NAME	STATUS
DB0 - DB7 P10 - P17 P20 - P27	High impedance Input disabled
T0	High impedance, input disabled
T1	Input disabled
XTAL1	High impedance
XTAL2	Output "High" Level
$\overline{\text{RESET}}$, $\overline{\text{SS}}$	Input disabled when oscillator is stopped. Pull-up transistors turn off.
$\overline{\text{INT}}$, EA	Input disabled when oscilltor is stopped.
$\overline{\text{RD}}$, $\overline{\text{WR}}$, ALE PROG, PSEN	High impedance

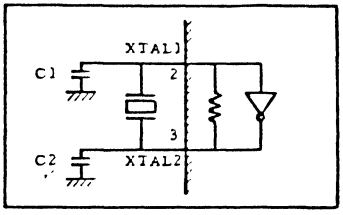
PIN STATUS IN HALT MODE

PIN NAME	STATUS
DB0 - DB7 P10 - P17 P20 - P27	Values prior to the execution of HALT INSTRUCTION are maintained.
T0	Status prior to the execution of HALT INSTRUCTION is maintained.
T1	Input disabled
XTAL1, XTAL2	Continue oscillation
$\overline{\text{RESET}}$, $\overline{\text{INT}}$	Input enabled
$\overline{\text{SS}}$, $\overline{\text{EA}}$	Input disabled
$\overline{\text{RD}}$, $\overline{\text{WR}}$, PROG, PSEN	Output "High" level
ALE	Output "Low" level

OSCILATOR

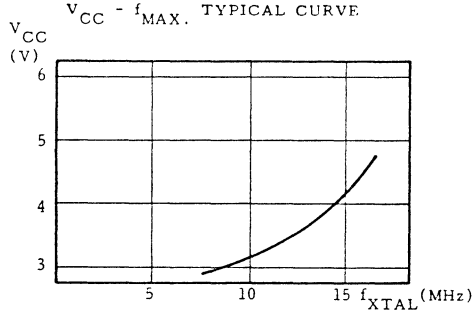
QUARTZ CRYSTAL
f = 1MHz to 4MHz : C1 = C2 = 30pF
f = 4MHz to 11MHz : C1 = C2 = 20pF

CERAMIC RESONATOR
f = 1MHz to 3MHz : C1 = C2 = 100pF
f = 3MHz to 11MHz : C1 = C2 = 30pF

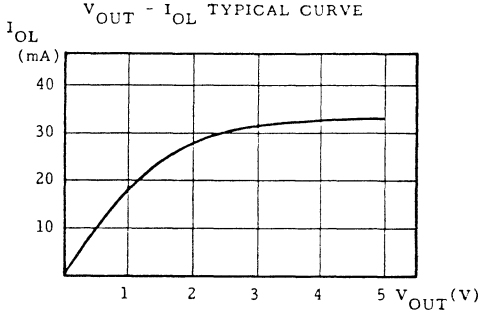


TYPICAL CHARACTARISTICS: Vcc = 5V, Ta = 25°C, unless otherwise noted.

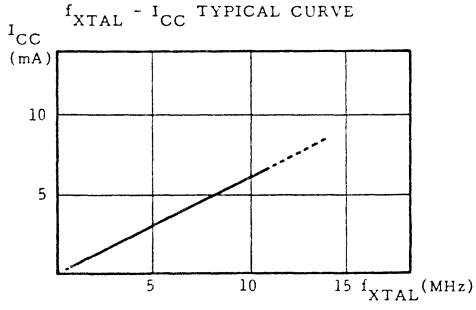
V_{CC} - $f_{MAX.}$ TYPICAL CURVE



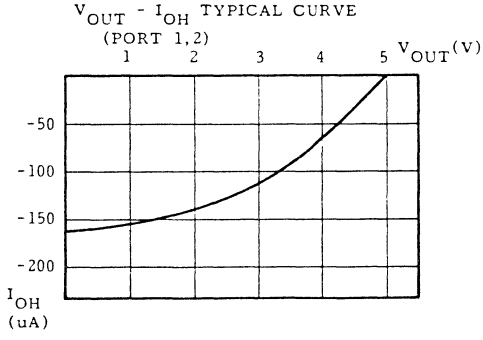
V_{OUT} - I_{OL} TYPICAL CURVE



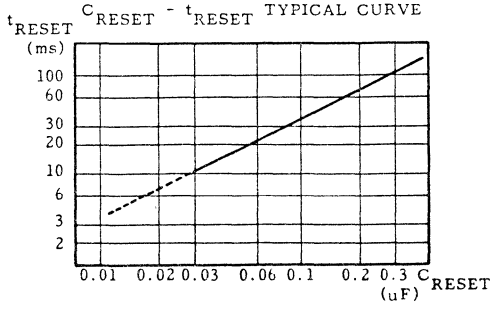
f_{XTAL} - I_{CC} TYPICAL CURVE



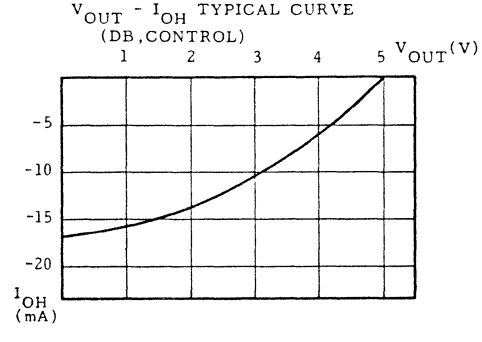
V_{OUT} - I_{OH} TYPICAL CURVE
(PORT 1,2)



t_{RESET} C_{RESET} - t_{RESET} TYPICAL CURVE

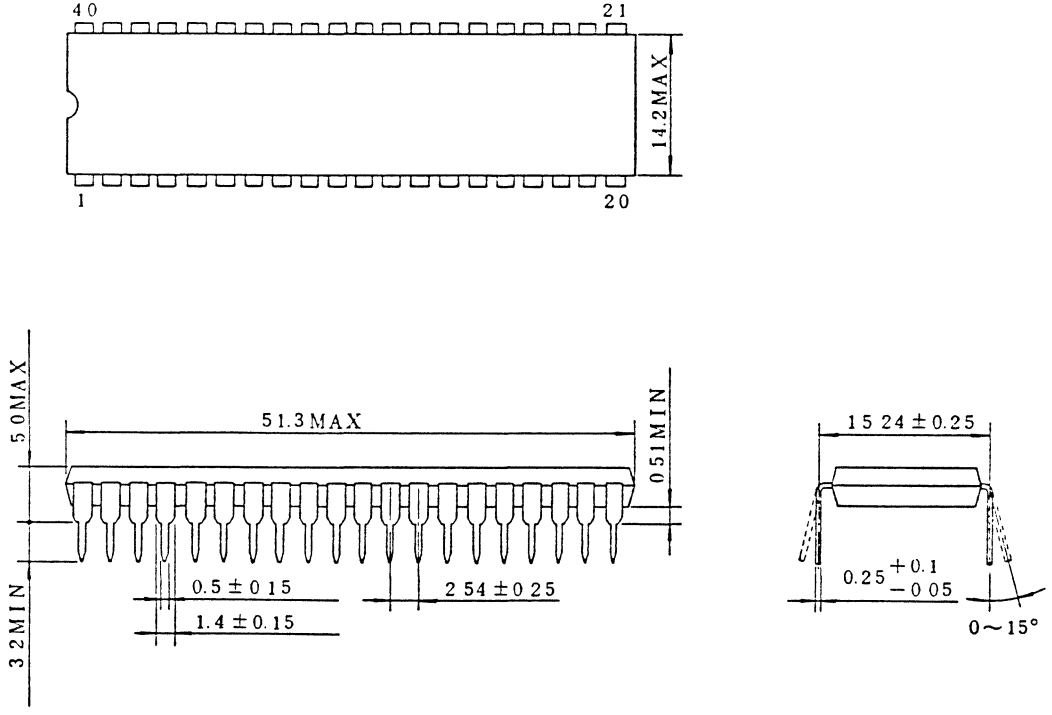


V_{OUT} - I_{OH} TYPICAL CURVE
(DB,CONTROL)



OUTLINE DRAWING (DUAL INLINE PACKAGE)

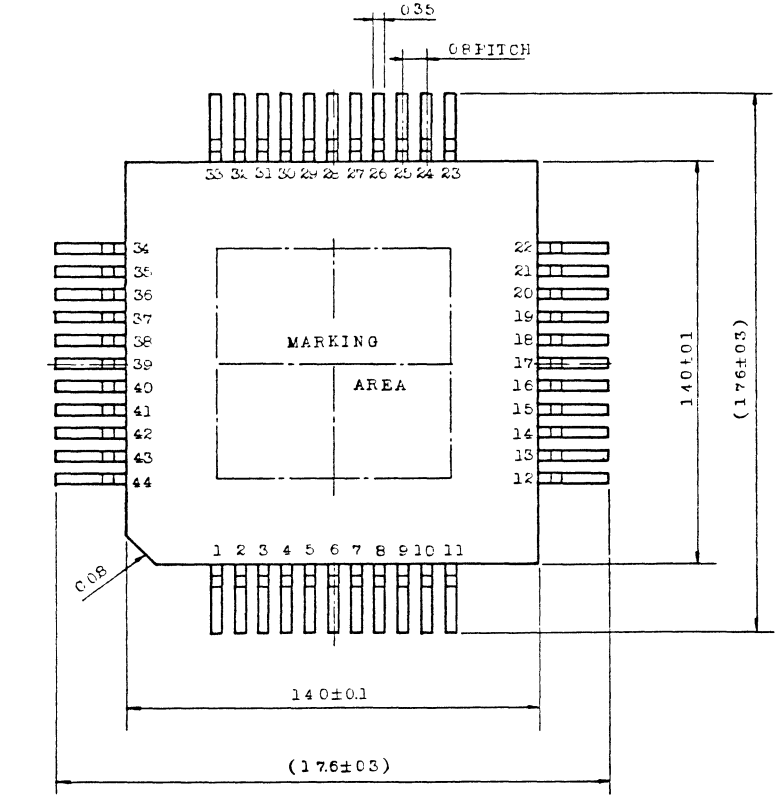
Unit in mm

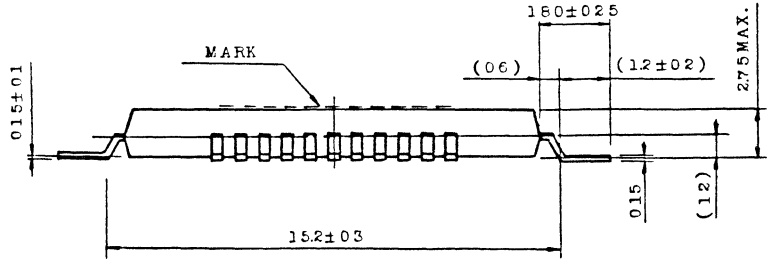


Note: 1. This dimension is measured at the center of bending point of leads.
2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoritical positions with respect to No.1 and No.40 leads.

OUTLINE DRAWING (FLAT PACKAGE)

Unit in mm





8-BIT SINGLE-CHIP MICROCOMPUTER

TMP80C49AP/TMP80C49AP-6
TMP80C49AP/TMP80C39AP-6
TMP80C49AF/TMP80C49AF-6

GENERAL DESCRIPTION

The TMP80C49A is a single chip microcomputer fabricated in Silicon Gate CMOS technology which provides internal 8-bit parallel architecture.

The following basic architectural functions of a computer have been included in a single chip; an 8-bit CPU, 128 x 8 RAM data memory, 2K x 8 ROM program memory, 27 I/O lines and an 8-bit timer/event counter.

The TMP80C49A is particularly efficient as a controller. It has extensive bit handling capability as well as facilities for both binary and BCD arithmetic.

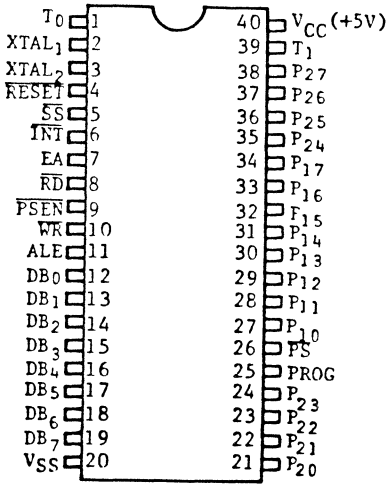
The TMP80C39AP/-6 is the equivalent of a TMP80C49AP/-6 without ROM program memory on chip. By using this device with external EPROM or RAM, software debugging becomes easy.

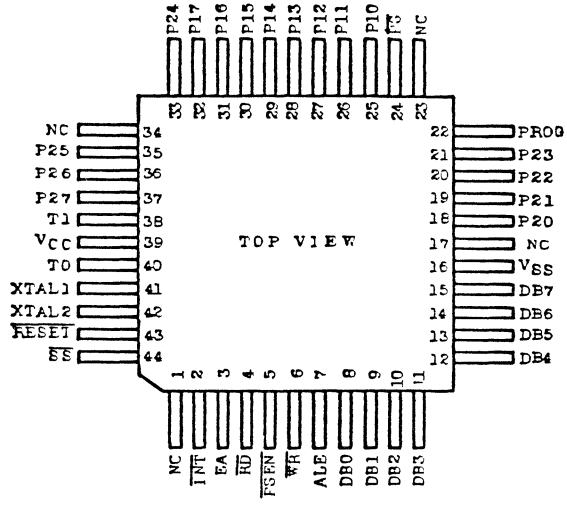
The TMP80C49AP/-6 and TMP80C39AP/-6 are in a standard Dual Inline Package. The TMP80C49AF/-6 is in a 44-pin Flat Package.

FEATURES

- TMP80C49AP/TMP80C39AP/TMP80C49AF
  1.36μs Instruction Cycle Time
  0°C to 70°C, 5V ±10%
- TMP80C49AP-6/TMP80C39AP-6/TMP80C49AF-6
  2.5 μs Instruction Cycle Time
  -40°C to 85°C, 5V ±20%
- Software Upward Compatible with
  TMP8049AP/TMP80C49P-6/INTEL's 8049
- HALT Instruction (Additional Instruction)
- 2K x 8 masked ROM
- 128 x 8 RAM
- 27 I/O lines
- Interval Timer/Event Counter
- Low Power
  10mA MAX. in Normal Operation
  (VCC=5V, fXTAL=6MHz)
  10μA Max. in Power Down Mode
  (VCC=5V, fXTAL : DC)
- Single Power Supply
- Power Down Mode (Stand-by Mode)
- Halt Mode (Idle Mode)

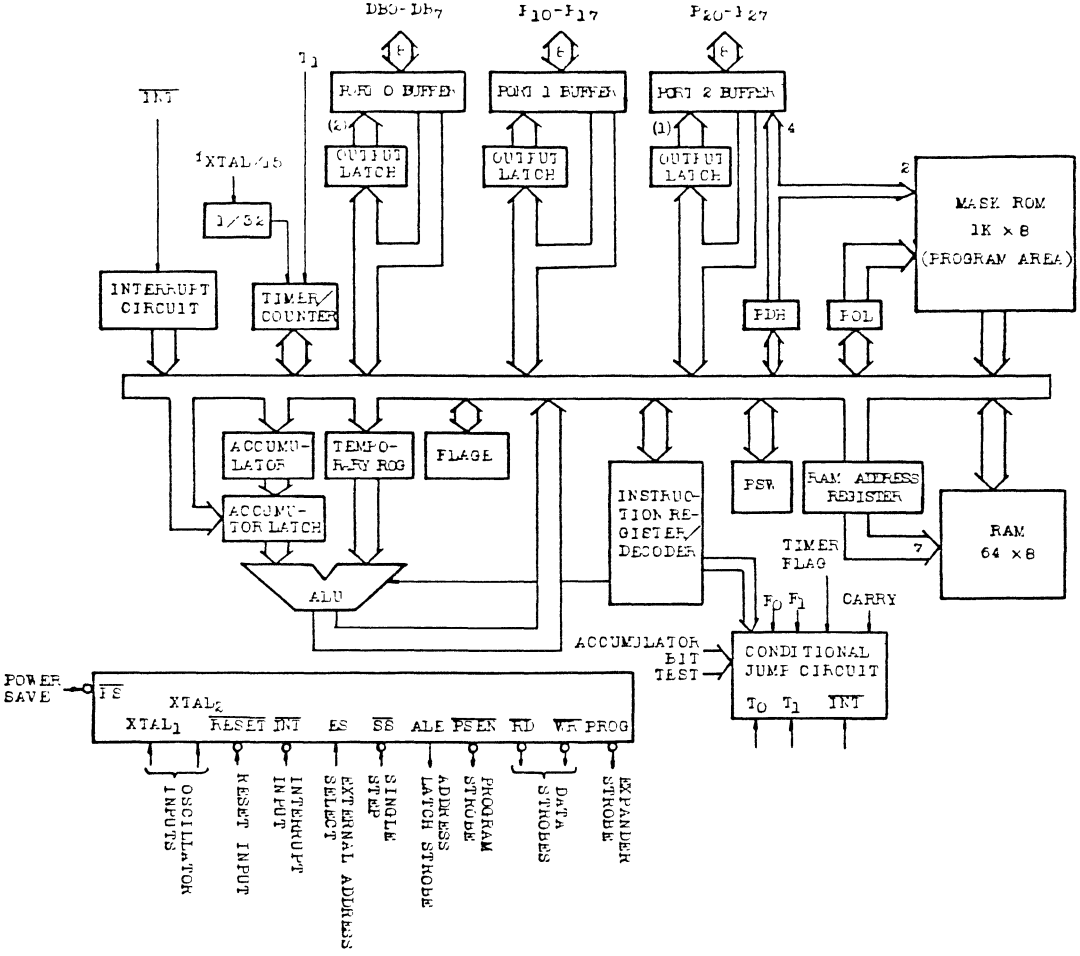
PIN CONNECTIONS (TOP VIEW)





NC: No Connection

BLOCK DIAGRAM



Note 1) The lower order 4 bit of port 2 output latch are used also for input/output operations with the I/O expander.

Note 2) The output latch of port 0 is also used for address output.

PIN NAMES AND PIN DESCRIPTION

VSS (Power Supply)
Circuit GND potential

VCC (Power Supply)
+5V during operation

$\overline{PS}$ (Input)
The control signal for the power saving at the power down mode (Active Low)

PROG (Output)
Output strobe for the TMP82C43P I/O expander.

P10 - P17 (Input/Output) Port 1
8-bit quasi-bidirectional port (Internal Pullup = 50KΩ).

P20 - P27 (Input/Output) Port 2
8-bit quasi-bidirectional port (Internal Pullup = 50KΩ).

P20 - P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for the TMP8243P.

DB0 - DB7 (Input/Output, Tri-State)
True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.

T0 (Input/Output)
Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.

T1 (Input)
Input pin testable using the JT1 and JNT1 instruction. Can be designated the event counter input using the timer/STRT CNT instruction.

$\overline{INT}$ (Input)
External interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)

$\overline{RD}$ (Output)
Output strobe activated during a Bus read. Can be used to enable data onto the Bus from an external device. Used as a Read Strobe to External Data Memory (Active Low).

$\overline{WR}$ (Output)
Output strobe during a Bus write (Active Low). Used as a Write Strobe to External Data Memory.

$\overline{\text{RESET}}$ (Input)
Active Low signal which is used to initialize the Processor. Also used during the power down mode.

ALE (Oupput)
Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.

$\overline{\text{PSEN}}$ (Output)
Program Store Enable. This output occurs only during a fetch to external program memory (Active Low).

$\overline{\text{SS}}$ (Input)
Single step input can be used in conjunction with ALE to "single step" processor through each instruction when $\overline{\text{SS}}$ is low the CPU is placed into a wait state after it has completed the instruction being executed. Also used during the power down mode.

EA (Input)
External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug and essential for testing and program verification. (Active High)

XTAL 1 (Input)
One side of crystal input for internal oscillator. Also input for external source.

XTAL 2 (Input)
Other side of crystal input.

TLCS-48 LIST OF INSTRUCTIONS (1/4)

Clas	Assembler Mnemonic		Object Code (1st) Bin.	Object Code (2nd) Hex.	Function		Flag C, AC	Cycle
Accumulator Instruction	ADD	A, Rr	01101rrr	68+r	(A)←(A)+(Rr)	r=0~7	↕ ↕	1
	ADD	A, @Rr	0110000r	60+r	(A)←(A)+[(Rr)]	r=0,1	↕ ↕	1
	ADD	A, #i	00000011	03	(A)←(A)+i		↕ ↕	2
			iiiiiiii	ii				
	ADDC	A, Rr	01111rrr	78+r	(A)←(A)+(Rr)+(C)	r=0~7	↕ ↕	1
	ADDC	A, @Rr	0111000r	70+r	(A)←(A)+[(Rr)]+(C)	r=0,1	↕ ↕	1
	ADDC	A, #i	00010011	13	(A)←(A)+i+(C)		↕ ↕	2
			iiiiiiii	ii				
	ANL	A, Rr	01011rrr	58+r	(A)←(A) ∧(Rr)	r=0~7		1
	ANL	A, @Rr	0101000r	50+r	(A)←(A) ∧[(Rr)]	r=0,1		1
	ANL	A, #i	01010011	53	(A)←(A) ∧i			2
			iiiiiiii	ii				
	ORL	A, Rr	01001rrr	48+r	(A)←(A) ∨(Rr)	r=0~7		1
	ORL	A, @Rr	0100000r	40+r	(A)←(A) ∨[(Rr)]	r=0,1		1
	ORL	A, #i	01000011	43	(A)←(A) ∨i			2
			iiiiiiii	ii				
	XRL	A, Rr	11011rrr	D8+r	(A)←(A) ∀(Rr)	r=0~7		1
	XRL	A, @Rr	1101000r	D0+r	(A)←(A) ∀[(Rr)]	r=0,1		1
	XRL	A, #i	11010011	D3	(A)←(A) ∀i			2
			iiiiiiii	ii				
	INC	A	00010111	17	(A)←(A)+1			1
	DEC	A	00000111	07	(A)←(A)-1			1
	CLR	A	00100111	27	(A)←0			1
	CPL	A	00110111	37	(A)←NOT(A)			1
	DA	A	01010111	57	(A)←(A)BCD		↕	1
	SWAP	A	01000111	47	(A)<7:4> ↔(A)<3:0>			1
	RL	A	11100111	E7	(A)<n+1> ←(A)<n>			1
					(A)<0> ←(A)<7>	n=0~6		
	RLC	A	11110111	F7	(A)<n+1> ←(A)<n>		↕	1
					(C)←(A)<7>			
					(A)<0> ←(C)	n=0~6		
	RR	A	01110111	77	(A)<n> ←(A)<n+1>	n=0~6		1
					(A)<7> ←(A)<0>			
	RRC	A	01100111	67	(A)<n> ←(A)<n+1>		↕	1
					(C)←(A)<0>			
					(A)<7> ←(C)	n=0~6		
I/O	IN	A, Pp	00001Opp	08+p	(A)←(Pp)	P=1,2		2

TLCS-48 LIST OF INSTRUCTIONS (2/4)

Class	Assembler Mnemonic		Object Code (1st) Bin.	Object Code (2nd) Hex.	Function		Flag C, AC	Cycle
	OUTL	Pp, A	00111Opp	38+p	(Pp) ←(A)	P=1,2		2
INPUT/OUTPUT Instruction	ANL	Pp, #i	10011Opp	98+p	(Pp) ←(Pp)∧i	P=1,2		2
			iiiiiiii	ii				
	ORL	Pp, #i	10001Opp	88+p	(Pp) ←(Pp)∨i	P=1,2		2
			iiiiiiii	ii				
	INS	A, BUS	00001000	08	(A)←(BUS)			2
	OUTL	BUS, A	00000010	02	(BUS)←(AC)			2
	ANL	BUS, #i	10011000	98	(BUS)←(BUS) ∧i			2
			iiiiiiii	ii				
	ORL	BUS, #i	10001000	88	(BUS)←(BUS) ∨i			2
			iiiiiiii	ii				
	MOVD	A, Pp	000011pp	0C+p	(A)<3:0> ←(Pp)	p=4~7		2
					(A)<7:4> ←0			
	MOVD	Pp, A	001111pp	3C+p	(Pp) ←(A)<3:0>	p=4~7		2
	ANLD	Pp, A	100111pp	9C+p	(Pp) ←(Pp)∧(A)<3:0>	p=4~7		2
	ORLD	Pp, A	100011pp	8C+p	(Pp) ←(Pp)∨(A)<3:0>	p=4~7		2
(1)	INC	Rr	00011rrr	18+r	(Rr) ←(Rr)+1	r=0~7		1
(1)	INC	@Rr	0001000r	10+r	[(Rr)] ←[(Rr)]+1	r=0,1		1
(1)	DEC	Rr	11001rrr	C8+r	(Rr) ←(Rr)-1	r=0~7		1
Branch Instruction	JMP	a	aH00100 aHL	aH+4	(PC)<10:0> ←a (PC)<11> ←(DBF)			2
	JMPP	@A	10110011	B3	(PC)<7:0>←PROM[(PC)<11:8>・(A)]			2
	DJNZ	Rr, a	11101rrr aHL	E8+r	(Rr) ←(Rr)-1 if(Rr) ≠0then(PC)<7:0>←aHL else no operation	r=0~7		2
	JC	a	11110110 aHL	F6	if(C)=1 then(PC)<7:0>←aHL else no operation			2
	JNC	a	11100110 aHL	E6	if(C)=0 then(PC)<7:0>←aHL else no operation			2
	JZ	a	11000110 aHL	C6	if(A)=0 then(PC)<7:0>←aHL else no operation			2
	JNZ	a	10010110 aHL	96	if(A)≠0 then(PC)<7:0> ←aHL else no operation			2
	JTO	a	00110110 aHL	36	if TO=1 then(PC)<7:0>←aHL else no operation			2

(1) ····· Register Instruction

TLCS-48 LIST OF INSTRUCTIONS (3/4)

Instructions	Assembler Mnemonic		Object Code (1st) (2nd) Bin	Hex.	Function	Flag C, AC	Cycle
Branch Instruction	JNTO	a	00100110 aHL	26	if T0=0 then(PC)<7 0>←aHL else no operation		2
	JT1	a	01010110 aHL	56	if T1=1 then(PC)<7 0>←aHL else no operation		2
	JNT1	a	01000110 aHL	46	if T1=0 then(PC)<7:0>←aHL else no operation		2
	JF0	a	10110110 aHL	B6	if F0=1 then(PC)<7 0>←aHL else no operation		2
	JF1	a	01110110 aHL	76	if F1=1 then(PC)<7.0>←aHL else no operation		2
	JTF	a	00010110 aHL	16	if TF=1 then(PC)<7:0>←aHL else no operation		2
	JNI	a	10000110 aHL	86	if INT =0 then(PC)<7:0>←aHL else no operation		2
	JBb	a	bbb10010 aHL	b+12	if (A)<b>=1 then (PC)<7:0>←aHL else no operation b=0~7		2
(2)	CALL	a	aH10100 aHL	aH+14	[(SP)] ←(PSW)<7:4> • (PC) (SP) ←(SP)+1 (PC)<10:0> ←a (PC)<11> ←(DBF)		2
	RET		10000011	83	(SP) ←(SP)-1 (PC) ←[(SP)]<11:0>		2
	RETR		10010011	93	(SP) ←(SP)-1 (PC) ←[(SP)]<11:0> (PSW)<7·4> ←[(SP)]<15·12>	↕ ↕	2
(3)	CLR	C	10010111	97	(C)←0		1
	CPL	C	10100111	A7	(C)←NOT(C)		1
	CLR	F0	10000101	85	(F0) ←0		1
	CPL	F0	10010101	95	(F0) ←NOT(F0)		1
	CLR	F1	10100101	A5	(F1) ←0		1
	CPL	F1	10110101	B5	(F1) ←NOT(F1)		1
(4)	MOV	A , Rr	11111rrr	F8+r	(A)←(Rr) r=0~7		1
	MOV	A ,@Rr	1111000r	F0+r	(A)←[(Rr)] r=0,1		1
	MOV	A ,#i	00100011 iiiiiiii	23 ii	(A) ←i		2
	MOV	Rr, A	10101rrr	A8+r	(Rr)←(A) r=0~7		1
	MOV	@Rr, A	1010000r	A0+r	[(Rr)]←(A) r=0,1		1

(2) ····· Subroutine Instruction (3) ····· Flag Instruction
(4) ····· Move Instruction

TLCS-48 LIST OF INSTRUCTIONS (4/4)

Instructions	Assembler Mnemonic		Object Code (1st) (2nd) Bin.	Hex	Function	Flag C AC	Cycle
Move Instruction	MOV	Rr,#i	10111rrr iiiiiiii	B8+r ii	(Rr)←i r=0~7		2
	MOV	@Rr,#i	1011000r iiiiiiii	B0+r ii	[(Rr)]←i r=0,1		2
	MOV	A,PSW	11000111	C7	(A) ←(PSW)		1
	MOV	PSW,A	11010111	D7	(PSW) ←(A)		1
	XCH	A Rr	00101rrr	28+r	(A) ↔(Rr) r=0~7		1
	XCH	A,@Rr	0010000r	20+r	(A) ↔[(Rr)] r=0,1		1
	XCHD	A,@Rr	0011000r	30+r	(A)<3 0>↔[(Rr)<3 0>] r=0,1		1
	MOVX	@Rr,A	1001000r	90+r	EXT[(Rr)] ←(A) r=0 1		1
	MOVX	A @Rr	1000000r	80+r	(A) ←EXT[(Rr)] r=0 1		1
	MOVP	A,@A	10100011	A3	(A) ←PR0[(PC)<11 8> • (A)]		1
	MOVP3	A,@A	11100011	E3	(A) ←PR0[(PC)<11> • 011 • (A)]		1
(5)	MOV	A,T	01000010	42	(A) ←(TR)		1
	MOV	T,A	01100010	62	(TR)←(A)		1
	STRT	T	01010101	55	Start Timer		1
	STRT	CNT	01000101	45	Start counter		1
	STOP	TCNT	01100101	65	Stop Timer/Counter		1
	EN	TCNTI	00100101	25	Enable Timer/Counter Interrupt		1
	DIS	TCNTI	00110101	35	Disable Timer/Counter Interrupt		1
Control	EN	I	00000101	05	Enable External Interrupt		1
	DIS	I	00010101	15	Disable External Interrupt		1
	SEL	RB0	11000101	C5	(BS)← 0		1
	SEL	RB1	11010101	D5	(BS)← 1		1
	SEL	MB0	11100101	E5	(DBF) ← 0		1
	SEL	MB1	11110101	F5	(DBF) ← 1		1
	ENTO	CLK	01110101	75	Enable Clock Output on T0		1
	HALT		00000001	01	Halt		1
(6)	NOP		00000000	00	no opration		1

(5) ····· A/D Converter Instruction (6) ····· Other

TMP80C49AP/TMP80C39AP/TMP80C49AF ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
VCC	VCC Supply Voltage (with respect to GND (VSS))	-0.5V to +7V
VINA	Input Voltage (Except EA)	-0.5V to VCC+0.5V
VINB	Input Voltage (Only EA)	-0.5V to 13V
PD	Power Dissipation (Ta=70°C)	250mW
TSOLDER	Soldering Temperature (Soldering Timer 10 sec)	260°C
TSTG	Storage Temperature	-65°C to 150°C
TOPR	Operating Temperature	0°C to 70°C

DC CHARACTERISTICS

TOPR=0°C to 70°C, VCC=+5V±10%, VSS=0V, unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage (Except XTAL1, XTAL2, RESET)			-0.5	-	0.8	V
VIL1	Input Low Voltage (XTAL1, XTAL2, RESET)			-0.5	-	0.6	V
VIH	Input High Voltage (Except XTAL1, XTAL2, RESET, PS)			2.2	-	VCC	V
VIH1	Input High Voltage(Except XTAL1, XTAL2, RESET, PS)			0.7 x VCC	-	VCC	V
VOL	Output Low Voltage (Except P10-P17, P20-P27)		IOL=1.6mA	-	-	0.45	V
VOL1	Output Low Voltage (P10-P17, P20-P27)		IOL=1.2mA	-	-	0.45	V
VOH11	Output High Voltage (Except P10-P17, P20-P27)		IOH=-1.6mA	2.4	-	-	V
VOH12	Output High Voltage (Except P10-P17, P20-P27)		IOH=-400μA	VCC-0.8	-	-	V
VOH21	Output High Voltage (P10-P17, P20-P27)		IOH=-50μA	2.4	-	-	V
VOH22	Output High Voltage (P10-P17, P20-P27)		IOH=-25μA	VCC-0.8	-	-	V
ILI	Input Leak Current (T1, INT, EA, PS)		VSS≦VIN≦VCC	-	-	±10	μA
ILI1	Input Leak Current (SS, RESET)		VSS≦VIN≦VCC	-	-	-50	μA
ILI2	Input Leak Current (P10-P17, P20-P27)		VSS+0.45V≦VIN≦VCC	-	-	-500	μA
ILO	Output Leak Current (BUS, TO) (High impedance condition)		VSS+0.45V≦VIN≦VCC	-	-	±10	μA
ICC1	VCC Supply Current	Normal operation	VCC=5V, fXTAL=6MHz VIH=VCC-0.2V	-	-	10	mA
ICCH1		HALT Mode	VIL=0.2V	-	-	2.5	
ICC2	VCC Supply Current	Normal operation	VCC=5V, fXTAL=11MHz	-	-	15	mA
ICCH2		HALT Mode	VIH=VCC-0.2V VIL=0.2V	-	-	4.0	

TMP80C49AP/TMP80C39AP/TMP80C49AF

AC CHARACTRISTICS

TOPR=0°C to 70°C, VCC=+5V±10%, VSS=0V, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITION	f(t)	11 MHz		UNIT
				MIN.	MAX.	
t	Clock Period	Note 2	1/xtal f	90.9	1000	ns
tLL	ALE Pulse Width		3.5t-170	150	-	ns
tAL	Address Setup Time (ALE)		2t-110	70	-	ns
tLA	Address Hold Time (ALE)	CL=20pF	t-40	50	-	ns
tCC1	Control Pulse Width ($\overline{RD}$, $\overline{WR}$)		7.5t-200	480	-	ns
tCC2	Control Pulse Width ($\overline{PSEN}$)		6t-200	350	-	ns
tDW	Data Setup Time ($\overline{WR}$)		6.5t-200	390	-	ns
tWD	Data Hold Time ($\overline{WR}$)	CL=20pF	t-50	40	-	ns
tDR	Data Hold Time ($\overline{RD}$, $\overline{PSEN}$)	CL=20pF	1.5t-30	0	110	ns
tRD1	Data Input Read Time ($\overline{RD}$)		6t-170	-	375	ns
tRD2	Data Input Read Time ($\overline{PSEN}$)		4.5t-170	-	240	ns
tAW	Address Setup Time ($\overline{WR}$)		5t-150	300	-	ns
tAD1	Address Setup Time ($\overline{RD}$)		10.5t-220	-	730	ns
tAD2	Address Setup Time ($\overline{PSEN}$)		7.5t-200	-	460	ns
tAFC1	Address Float Time ($\overline{RD}$, $\overline{WR}$)	CL=20pF	2t-40	140	-	ns
tAFC2	Address Float Time ($\overline{PSEN}$)	CL=20pF	0.5t-40	10	-	ns
tLAFC1	ALE to Control Time ($\overline{RD}$, $\overline{WR}$)		3t-75	200	-	ns
tLAFC2	ALE to Control Time ($\overline{PSEN}$)		1.5t-75	60	-	ns
tCA1	Control to ALE Time ($\overline{RD}$, $\overline{WR}$, PROG)		t-65	25	-	ns
tCA2	Control to ALE Time ($\overline{PSEN}$)		4t-70	290	-	ns
tCP	Port Control Setup Time (PROG)		1.5t-80	50	-	ns
tPC	Port Control Hold Time (PROG)		4t-260	100	-	ns
tPR	Port 2 Input Data Setup Time (PROG)		8.5t-120	-	650	ns
tPF	Port 2 Input Data Hold Time (PROG)		1.5t	0	140	ns
tDP	Port 2 Output Data Setup Time (PROG)		6t-290	250	-	ns
tPD	Port 2 Output Data Hold Time (PROG)		1.5t-90	40	-	ns

TMP80C49AP/TMP80C39AP/TMP80C49AF

AC CHARACTRISTICS (CONTINUE)
TOPR=0°C to 70°C, VCC=+5V±10%, VSS=0V, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITION	f(t)	11 MHz		UNIT
				MIN.	MAX.	
tPP	PROG Pulse Width		10.5t-250	700	-	ns
tPL	Port 2 I/O Data Setup Time(ALE)		4t-200	160	-	ns
tLP	Port 2 I/O Data Hold Time (ALE)		1.5t-120	15	-	ns
tPV	Poer Output Delay Time (ALE)		4.5t+100	-	510	ns
t0PRR	T0 Clock Period		3t	270	-	ns
tCY	Cycle Time		15t	1.36	15.0	μs

Note : 1. Control Output CL=80pF. BUS Output CL=150pF.
2. The f(t) assumes 50% duty cycle on XTAL1 and XTAL2.
The Max. Clock frequency is 11MHz. and the Min. Clock frequency is 1MHz.

TMP80C49AP-6/TMP80C39AP-6/TMP80C49AF-6 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
VCC	VCC Supply Voltage (with respect to GND (VSS))	-0.5V to +7V
VINA	Input Voltage (Except EA)	-0.5V to VCC+0.5V
VINB	Input Voltage (Only EA)	-0.5V to 13V
PD	Power Dissipation (Ta=85°C)	250mW
TSOLDER	Soldering Temperature (Soldering Timer 10 sec)	260°C
TSTG	Storage Temperature	-65°C to 150°C
TOPR	Operating Temperature	-40°C to 85°C

DC CHARACTERISTICS (I)

TOPR = -40°C to 85°C, VCC=+5V±10%, VSS=0V, unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage			-0.5	-	0.8	V
VIH	Input High Voltage (Except XTAL1, XTAL2, $\overline{RESET}$, $\overline{PS}$)			2.2	-	VCC	V
VIH1	Input High Voltage ($\overline{XTAL1}$, XTAL2, $\overline{RESET}$, $\overline{PS}$)			0.7 x VCC	-	VCC	V
VOL	Output Low Voltage (Except P10-P17, P20-P27)		IOL=1.6mA	-	-	0.45	V
VOL1	Output Low Voltage (P10-P17, P20-P27)		IOL=1.2mA	-	-	0.45	V
VOH11	Output High Voltage (Except P10-P17, P20-P27)		IOH=-1.6mA	2.4	-	-	V
VOH12	Output High Voltage (Except P10-P17, P20-P27)		IOH=-400μA	VCC-0.8	-	-	V
VOH21	Output High Voltage (P10-P17, P20-P27)		IOH=-50μA	2.4	-	-	V
VOH22	Output High Voltage (P10-P17, P20-P27)		IOH=-25μA	VCC-0.8	-	-	V
ILI	Input Leak Current ($\overline{T1}$, $\overline{INT}$, $\overline{EA}$, $\overline{PS}$)		VSS≦VIN≦VCC	-	-	±10	μA
ILI1	Input Leak Current ($\overline{SS}$, $\overline{RESET}$)		VSS≦VIN≦VCC	-	-	-50	μA
ILI2	Input Leak Current (P10-P17, P20-P27)		VSS+0.45V≦VIN≦VCC	-	-	-500	μA
ILO	Output Leak Current (BUS, $\overline{TO}$) (High impedance condition)		VSS+0.45V≦VIN≦VCC	-	-	±10	μA
ICC1	VCC Supply Current	Normal operation	VCC=5V, fXTAL=6MHz VIH=VCC-0.2V	-	-	10	mA
ICCH1		HALT Mode	VIL=0.2V	-	-	2.5	

TMP80C49AP-6/TMP80C39AP-6/TMP80C49AF-6 ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (II)

TOPR=-40°C to 85°C, VCC=+5V±20%, VSS=0V, unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage			-0.5	-	0.15 x VCC	V
VIH	Input High Voltage (Except XTAL1, XTAL2, RESET, PS)			0.5 x VCC	-	VCC	V
VIH1	Input High Voltage (XTAL1, XTAL2, RESET, PS)			0.7 x VCC	-	VCC	V
VOL	Output Low Voltage (Except P10-P17, P20-P27)		IOL=1.6mA	-	-	0.45	V
VOL1	Output Low Voltage (P10-P17, P20-P27)		IOL=1.2mA	-	-	0.45	V
VOH12	Output High Voltage (Except P10-P17, P20-P27)		IOH=-400μA	VCC-0.8	-	-	V
VOH22	Output High Voltage (P10-P17, P20-P27)		IOH=-25μA	VCC-0.8	-	-	V
ILI	Input Leak Current (T1, INT, EA, PS)		VSS≦VIN≦VCC	-	-	±10	μA
ILI1	Input Leak Current (SS, RESET)		VSS≦VIN≦VCC	-	-	-VCC/0.1	μA
ILI2	Input Leak Current (P10-P17, P20-P27)		VSS+0.45V≦VIN≦VCC	-	-	-VCC/0.01	μA
ILO	Output Leak Current (BUS, TO) (High impedance condition)		VSS+0.45V≦VIN≦VCC	-	-	±10	μA
ICC1	VCC Supply Current	Normal Operation	VCC=5V, fXTAL=6MHz VIH=VCC-0.2V, VIH=0.2V	-	-	10	mA
ICCH1		HALT Mode		-	-	2.5	

TMP80C49AP-6/TMP80C39AP-6/TMP80C49AF-6

AC CHARACTRISTICS
TOPR=-40°C to 85°C, VCC=+5V±20%, VSS=0V, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITION	f(t)	6 MHz		UNIT
				MIN.	MAX.	
t	Clock Period	Note 2	1/xtal f	166.6	1000	ns
tLL	ALE Pulse Width		3.5t-170	410	-	ns
tAL	Address Setup Time (ALE)		2t-110	220	-	ns
tLA	Address Hold Time (ALE)	CL=20pF	t-40	120	-	ns
tCC1	Control Pulse Width ($\overline{RD}$, $\overline{WR}$)		7.5t-200	1050	-	ns
tCC2	Control Pulse Width ($\overline{PSEN}$)		6t-200	800	-	ns
tDW	Data Setup Time ($\overline{WR}$)		6.5t-200	880	-	ns
tWD	Data Hold Time ($\overline{WR}$)	CL=20pF	t-50	120	-	ns
tDR	Data Hold Time ($\overline{RD}$, $\overline{PSEN}$)	CL=20pF	1.5t-30	0	220	ns
tRD1	Data Input Read Time ($\overline{RD}$)		6t-170	-	830	ns
tRD2	Data Input Read Time ($\overline{PSEN}$)		4.5t-170	-	580	ns
tAW	Address Setup Time ($\overline{WR}$)		5t-150	680	-	ns
tAD1	Address Setup Time ($\overline{RD}$)		10.5t-220	-	1530	ns
tAD2	Address Setup Time ($\overline{PSEN}$)		7.5t-200	-	1050	ns
tAFC1	Address Float Time ($\overline{RD}$, $\overline{WR}$)	CL=20pF	2t-40	290	-	ns
tAFC2	Address Float Time ($\overline{PSEN}$)	CL=20pF	0.5t-40	40	-	ns
tLAFC1	ALE to Control Time ($\overline{RD}$, $\overline{WR}$)		3t-75	420	-	ns
tLAFC2	ALE to Control Time ($\overline{PSEN}$)		1.5t-75	175	-	ns
tCA1	Control to ALE Time ($\overline{RD}$, $\overline{WR}$, PROG)		t-65	100	-	ns
tCA2	Control to ALE Time ($\overline{PSEN}$)		4t-70	590	-	ns
tCP	Port Control Setup Time (PROG)		1.5t-80	170	-	ns
tPC	Port Control Hold Time (PROG)		4t-260	400	-	ns
tPR	Port 2 Input Data Setup Time (PROG)		8.5t-120	-	1290	ns
tPF	Port 2 Input Data Hold Time (PROG)		1.5t	0	250	ns
tDP	Port 2 Output Data Setup Time (PROG)		6t-290	710	-	ns
tPD	Port 2 Output Data Hold Time (PROG)		1.5t-90	160	-	ns

TMP80C49AP-6/TMP80C39AP-6/TMP80C49AF-6

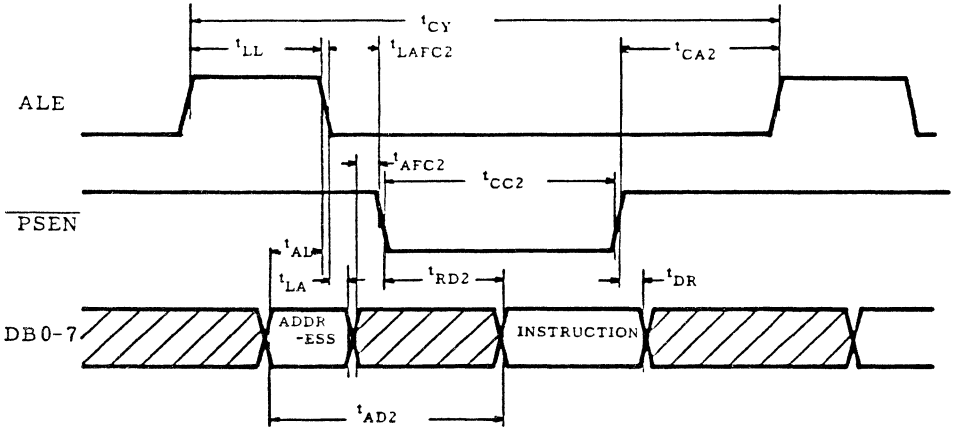
AC CHARACTRISTICS (CONTINUE)
TOPR=-40°C to 85°C, VCC=+5V±20%, VSS=0V, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITION	f(t)	6 MHz		UNIT
				MIN.	MAX.	
tPP	PROG Pulse Width		10.5t-250	1500	-	ns
tPL	Port 2 I/O Data Setup Time(ALE)		4t-200	460	-	ns
tLP	Port 2 I/O Data Hold Time (ALE)		0.5t-30	130	-	ns
tPV	Port Output Delay Time (ALE)		4.5t+100	-	850	ns
t0PRR	T0 Clock Period		3t	500	-	ns
tCY	Cycle Time		15t	2.5	15.0	μs

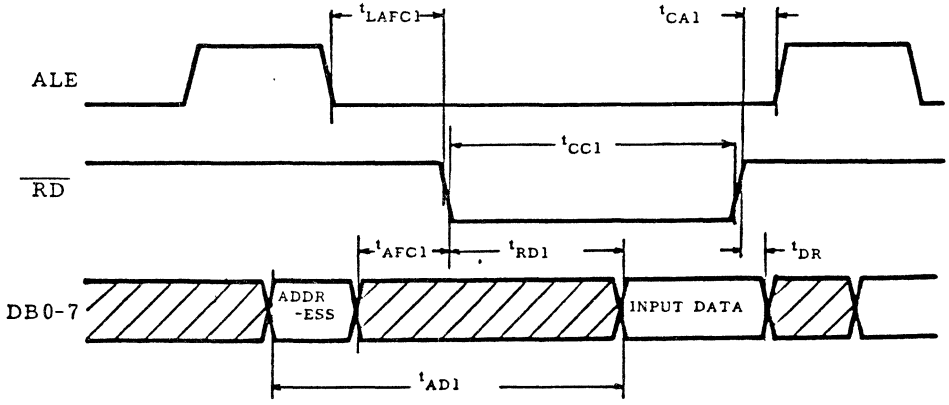
Note : 1. Control Output CL=80pF. BUS Output CL=150pF.
2. The f(t) assumes 50% duty cycle on XTAL1 and XTAL2.
The Max. Clock frequency is 6MHz. and the Min. Clock frequency is 1MHz.

TIMING WAVEFORM

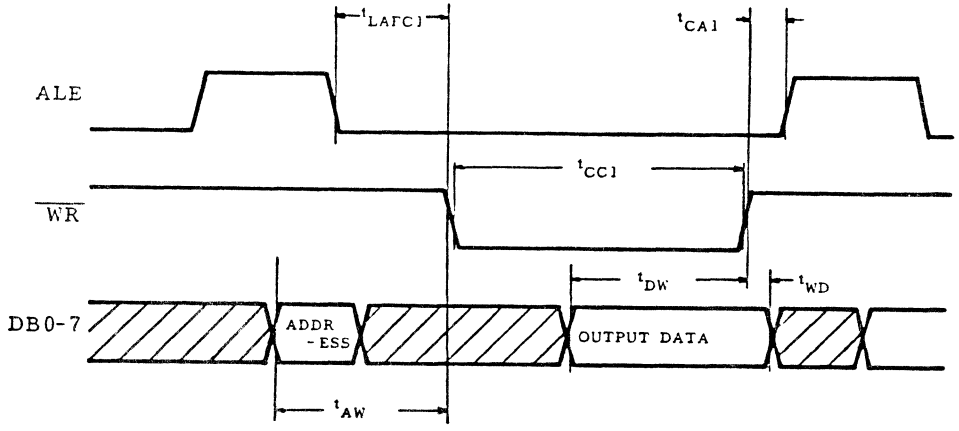
A. Instruction Fetch from External Program Memory



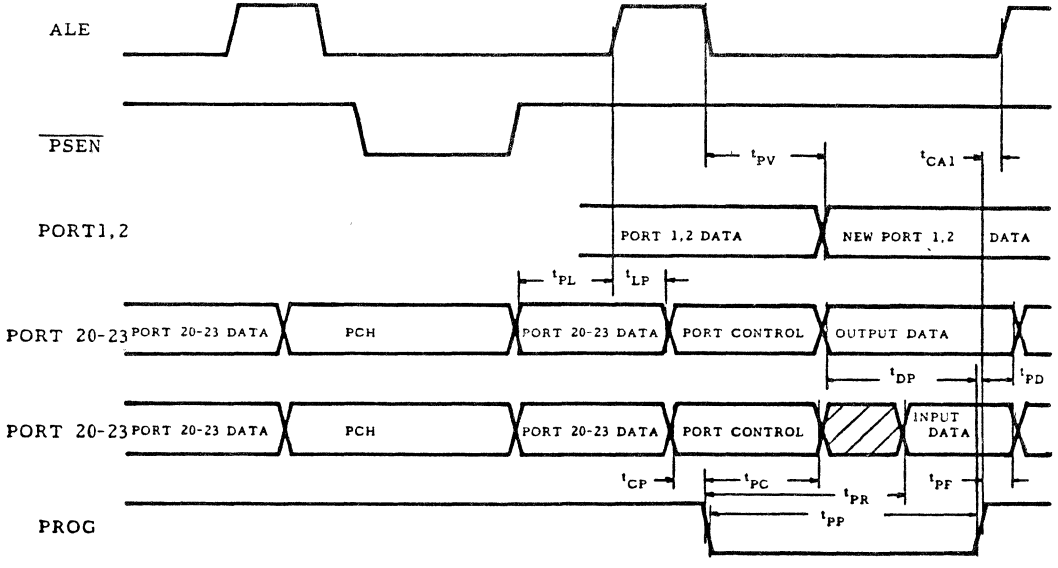
B. Read from External Data Memory



C. Write into External Data Memory



D. Timing of Port 2 during Expander Instruction Execution



POWER DOWN MODE (I) ..... Data Hold Mode in RAM

The operation of oscillation circuit is suspended by setting $\overline{PS}$ terminal to low level after $\overline{RESET}$ terminal has been set to low level. Consequently, all the data in RAM area can be held in low power consumption.

The minimum hold voltage of VCC in this mode is 2V.

$\overline{PS}$ terminal is set to high level to resume oscillation after VCC has been reset to 5V, and then $\overline{RESET}$ terminal is set to high level, thus, the normal mode is restarted from the initialize operation (address 0).

DC CHARACTERISTICS

TMP80C49AP/TMP80C39AP/TMP80C49AF : TOPR=0°C to 70°C, VSS=0V
TMP80C49AP-6/TMP80C39AP-6/TMP80C49AF-6 : TOPR=-40°C to 85°C, VSS=0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VSB1	Standby Voltage(1)		2.0	-	6.0	V
ISB1	Standby Current(1)	VCC=5V, VIH=VCC-0.2V, VIL=0.2V	-	0.5	10	μA

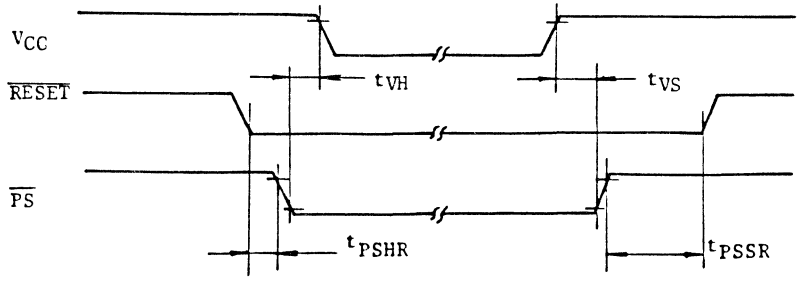
DC CHARACTERISTICS

TMP80C49AP/TMP80C39AP/TMP80C49AF : TOPR= 0°C to 70°C, VCC=5V±10%, VSS=0V
TMP80C49AP-6/TMP80C39AP-6/TMP80C49AF-6 : TOPR=-40°C to 85°C, VCC=5V±20%, VSS=0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
tPSHR	Power Save Hold Time ($\overline{RESET}$)		10	-	-	μS
tPSSR	Power Save Setup Time ($\overline{RESET}$)		10	-	-	mS
tVH	VCC Hold Time ($\overline{PS}$)		5	-	-	μS
tVS	VCC Setup Time ($\overline{PS}$)		5	-	-	μS

Note: tCY=2.5μS (fXTAL=6MHz)

TIMING WAVEFORM



POWER DOWN MODE (II) ..... ALL Data Hold Mode

The operation of oscillation circuit is suspended by setting $\overline{PS}$ terminal to low level after $\overline{SS}$ terminal has been set to low level. Consequently, all data can be held in low power consumption.

The minimum hold voltage of VCC in this mode is 3V.

$\overline{PS}$ terminal is set to high level to resume oscillation after VCC has been reset to 5V, and then $\overline{SS}$ terminal is set to high level, thus, the normal mode is restarted continuously from the state just before the power down mode (II).

DC CHARACTERISTICS

TMP80C49AP/TMP80C39AP/TMP80C49AF : TOPR=0°C to 70°C, VSS=0V
TMP80C49AP-6/TMP80C39AP-6/TMP80C49AF-6 : TOPR=-40°C to 85°C, VSS=0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VSB2	Standby Voltage(2)		3.0	-	6.0	V
ISB2	Standby Current(2)	VCC=5V, VIH=VCC-0.2V, VIL=0.2V	-	0.5	10	μA

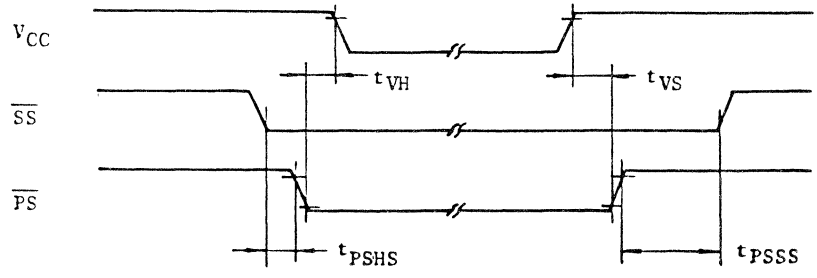
AC CHARACTERISTICS

TMP80C49AP/TMP80C39AP/TMP80C49AF : TOPR= 0°C to 70°C, VSS=5V±10%, VSS=0V
TMP80C49AP-6/TMP80C39AP-6/TMP80C49AF-6 : TOPR=-40°C to 85°C, VCC=5V±20%, VSS=0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
tPSHS	Power Save Hold Time ($\overline{SS}$)		10	-	-	μS
tPSSS	Power Save Setup Time ($\overline{SS}$)		10	-	-	mS
tVH	VCC Hold Time ($\overline{PS}$)		5	-	-	μS
tVS	VCC Setup Time ($\overline{PS}$)		5	-	-	μS

Note: tCY=2.5μS (fXTAL=6MHz)

TIMING WAVEFORM



HALT MODE

. 1 HALT INSTRUCTION

OP code is "01H". HALT INSTRUCTION is an additional instruction to the standard 8048/8049 instruction set.

. 2 Entry to HALT MODE

On the execution of HALT INSTRUCTION, TMP80C49A/TMP80C39A enter HALT MODE.

. 3 Status in HALT MODE

The oscillator continues its operation, however, the internal clocks and internal logic values just prior to the execution of HALT INSTRUCTION are maintained. Power consumption in HALT MODE is less than 50% of normal operation. The status of each pins are described in the following table.

. 4 Release from HALT MODE

HALT MODE is released by either of two signals ($\overline{\text{RESET}}$, $\overline{\text{INT}}$).

(1) $\overline{\text{RESET}}$ Release Mode : An active $\overline{\text{RESET}}$ input signal causes the normal reset function. TMP80C49A/TMP80C39A start the program at address "000 H".

(2) $\overline{\text{INT}}$ Release Mode : An active $\overline{\text{INT}}$ input signal causes the normal operation.

In case of interrupt enable mode (EI MODE), TMP80C49A/TMP80C39A execute the interrupt service routine, after the execution of one instruction which is located at the next address after HALT INSTRUCTION.

In case of interrupt disable mode (DI MODE), TMP80C49A/TMP80C39A execute normal operation from the next address after HALT INSTRUCTION.

. 5 Supply Voltage Range in HALT MODE

The operating supply voltage range and the operating temperature range are same as in normal operation.

PIN STATUS IN POWER DOWN MODE (I) (II)

PIN NAME	STATUS
DB0 - DB7 P10 - P17 P20 - P27	High impedance Input disabled
T0	High impedance, input disabled
T1	Input disabled
XTAL1	High impedance
XTAL2	Output "High" Level
$\overline{\text{RESET}}$, $\overline{\text{SS}}$	Input disabled when oscillator is stopped. Pull-up transistors turn off.
$\overline{\text{INT}}$, EA	Input disabled when oscilltor is stopped.
$\overline{\text{RD}}$, $\overline{\text{WR}}$, ALE PROG, $\overline{\text{PSEN}}$	High impedance

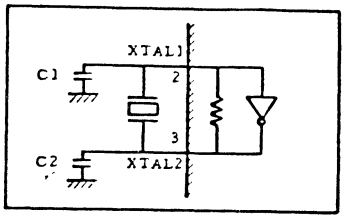
PIN STATUS IN HALT MODE

PIN NAME	STATUS
DB0 - DB7 P10 - P17 P20 - P27	Values prior to the execution of HALT INSTRUCTION are maintained.
T0	Status prior to the execution of HALT INSTRUCTION is maintained.
T1	Input disabled
XTAL1, XTAL2	Continue oscillation
$\overline{\text{RESET}}$, $\overline{\text{INT}}$	Input enabled
$\overline{\text{SS}}$, $\overline{\text{EA}}$	Input disabled
$\overline{\text{RD}}$, $\overline{\text{WR}}$, PROG, $\overline{\text{PSEN}}$	Output "High" level
ALE	Output "Low" level

OSCILATOR

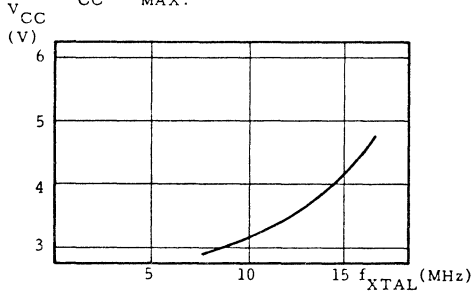
QUARTZ CRYSTAL
f = 1MHz to 4MHz : C1 = C2 = 30pF
f = 4MHz to 11MHz : C1 = C2 = 20pF

CERAMIC RESONATOR
f = 1MHz to 3MHz : C1 = C2 = 100pF
f = 3MHz to 11MHz : C1 = C2 = 30pF

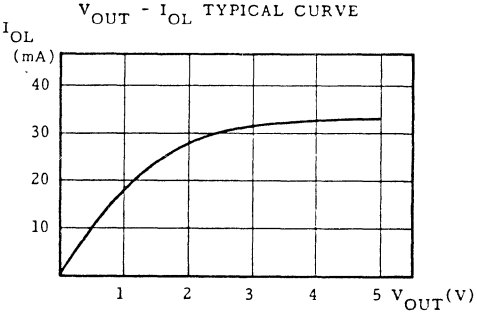


TYPICAL CHARACTARISTICS : Vcc = 5V, Ta = 25°C, unless Otherwise noted.

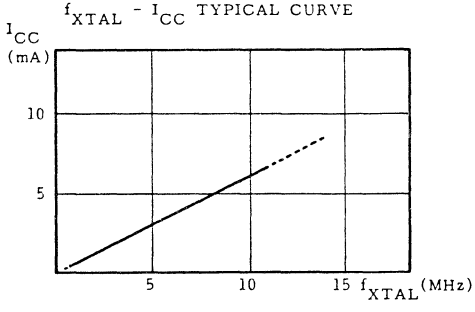
V_{CC} - $f_{MAX.}$ TYPICAL CURVE



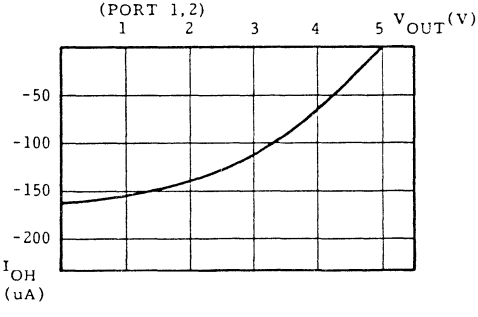
V_{OUT} - I_{OL} TYPICAL CURVE



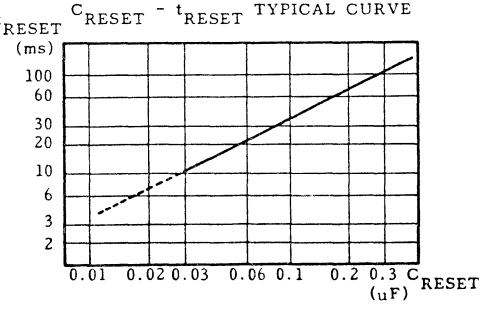
f_{XTAL} - I_{CC} TYPICAL CURVE



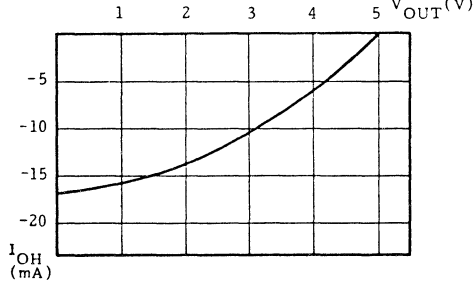
V_{OUT} - I_{OH} TYPICAL CURVE
(PORT 1,2)



t_{RESET} C_{RESET} - t_{RESET} TYPICAL CURVE

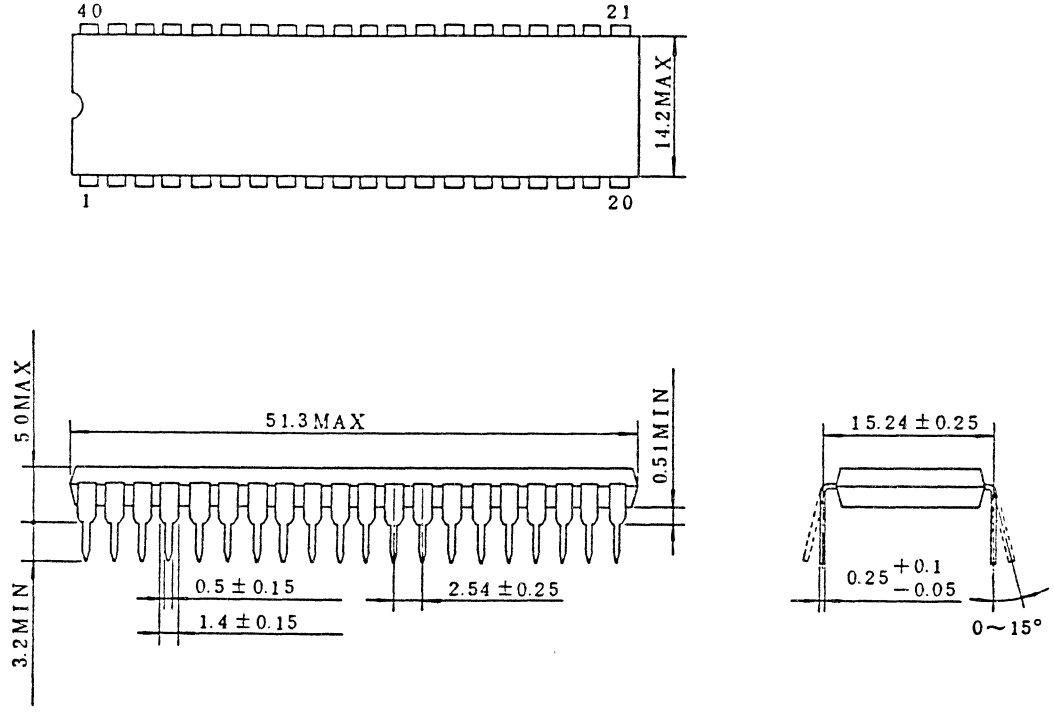


V_{OUT} - I_{OH} TYPICAL CURVE
(DB,CONTROL)



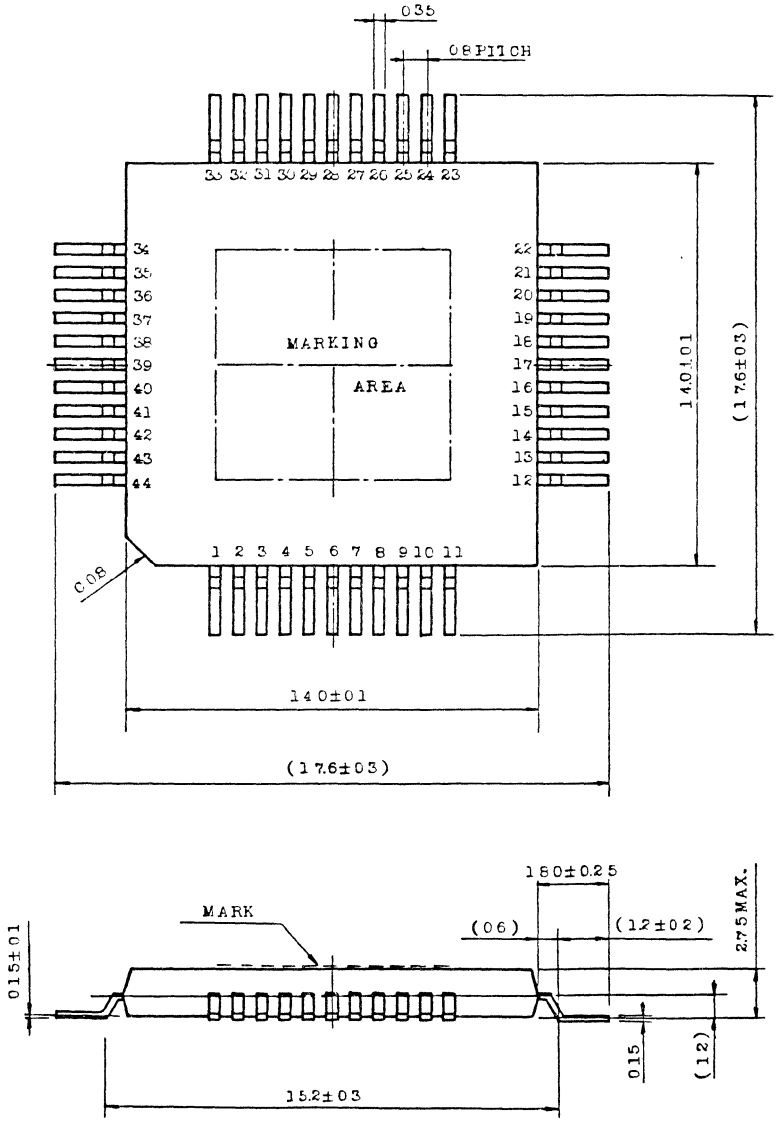
OUTLINE DRAWING (DUAL INLINE PACKAGE)

Unit in mm



Note: 1. This dimension is measured at the center of bending point of leads.
2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoritical positions with respect to No.1 and No.40 leads.

OUTLINE DRAWING (FLAT PACKAGE)



8-BIT SINGLE-CHIP MICROCOMPUTER

TMP80C50AP/TMP80C50AP-6
TMP80C40AP/TMP80C40AP-6
TMP80C50AF/TMP80C50AF-6

GENERAL DESCRIPTION

The TMP80C50A is a single chip microcomputer fabricated in Silicon Gate CMOS technology which provides internal 8-bit parallel architecture.

The following basic architectural functions of a computer have been included in a single chip; an 8-bit CPU, 256 x 8 RAM data memory, 4K x 8 ROM program memory, 27 I/O lines and an 8-bit timer/event counter.

The TMP80C50A is particularly efficient as a controller. It has extensive bit handling capability as well as facilities for both binary and BCD arithmetic.

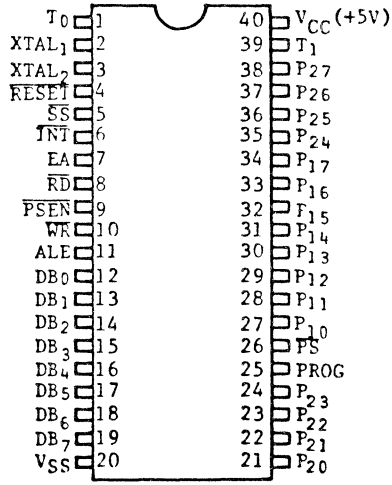
The TMP80C40AP/-6 is the equivalent of a TMP80C50AP/-6 without ROM program memory on chip. By using this device with external EPROM or RAM, software debugging becomes easy.

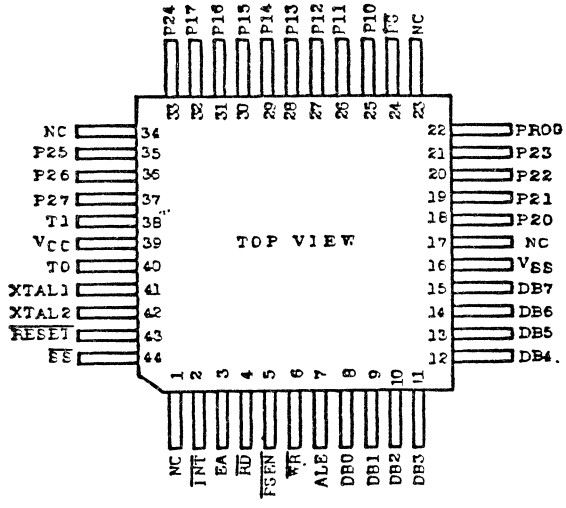
The TMP80C50AP/-6 and TMP80C40AP/-6 are in a standerd Dual Inline Pakage.
The TMP80C50AF/-6 is in a 44-pin Flat Package.

FEATURES

- TMP80C50AP/TMP80C40AP/TMP80C50AF
  1.36μs Instruction Cycle Time
  0°C to 70°C, 5V±10%
- TMP80C50AP-6/TMP80C40AP-6/TMP80C50AF-6
  2.5μs Instruction Cycle Time
  -40°C to 85°C, 5V±20%
- Software Upward Compatible with
  TMP80C49AP/TMP80C49AP-6/INTEL's 8049
- HALT Instruction (Additional Instruction)
- 4K x 8 masked ROM
- 256 x 8 RAM
- 27 I/O lines
- Interval Timer/Event Counter
- Low Power
  10mA MAX. in Normal Operation
  (VCC=5V, fXTAL=6MHz)
  10μAMax. in Power Down Mode
  (VCC=5V, fXTAL: DC)
- Single Power Supply
- Power Down Mode (Stand-by Mode)
- Halt Mode (Idle Mode)

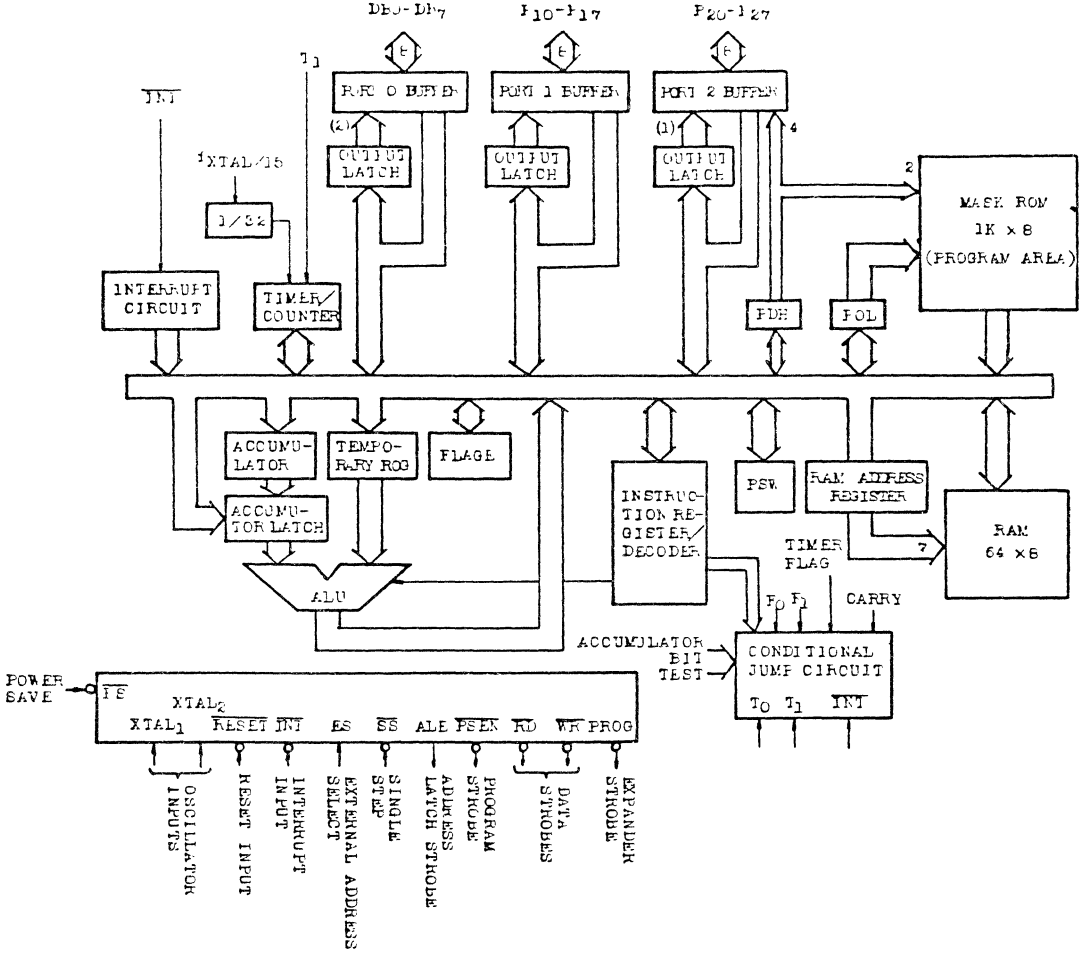
PIN CONNECTIONS (TOP VIEW)





NC: No Connection

BLOCK DIAGRAM



Note 1) The lower order 4 bit of port 2 output latch are used also for input/output operations with the I/O expander.

Note 2) The output latch of port 0 is also used for address output.

PIN NAMES AND PIN DESCRIPTION

VSS (Power Supply)
Circuit GND potential

VCC (Power Supply)
+5V during operation

$\overline{PS}$ (Input)
The control signal for the power saving at the power down mode (Active Low)

PROG (Output)
Output strobe for the TMP82C43P I/O expander.

P10-P17 (Input/Output) Port 1
8-bit quasi-bidirectional port (Internal Pullup = 50KΩ).

P20-P27 (Input/Output) Port 2
8-bit quasi-bidirectional port (Internal Pullup = 50KΩ).

P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for the TMP8243P.

DB0-DB7 (Input/Output, Tri-State)
True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.

T0 (Input/Output)
Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.
(Input)
Input pin testable using the JT1 and JNT1 instruction. Can be designated the event counter input using the timer/STRT CNT instruction.

$\overline{INT}$ (Input)
External interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active Low)

$\overline{RD}$ (Output)
Output strobe activated during a Bus read. Can be used to enable data onto the Bus from an external device. Used as a Read Strobe to External Data Memory (Active Low)

$\overline{WR}$ (Output)
Output strobe during a Bus write (Active Low). Used as a Write Strobe to External Data Memory.

$\overline{\text{RESET}}$ (Input)
Active Low signal which is used to initialize the Processor. Also used during the power down mode.

ALE (Oupput)
Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.

$\overline{\text{PSEN}}$ (Output)
Program Store Enable. This output occurs only during a fetch to external program memory (Active Low).

$\overline{\text{SS}}$ (Input)
Single step input can be used in conjunction with ALE to "single step" processor through each instruction when $\overline{\text{SS}}$ is low the CPU is placed into a wait state after it has completed the instruction being executed. Also used during the power down mode.

EA (Input)
External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug and essential for testing and program verification. (Active High)

XTAL 1 (Input)
One side of crystal input for internal oscillator. Also input for external source.

XTAL 2 (Input)
Other side of crystal input.

TLCS-48 LIST OF INSTRUCTIONS (1/4)

Class	Mnemonic	Object Code (1st) Bin.	(2nd) Hex.	Function		Flag C,AC	Cycle
Accumulator Instruction	ADD A, Rr	01101rrr	68+r	(A)←(A)+(Rr)	r=0~7	↕ ↕	1
	ADD A, @Rr	0110000r	60+r	(A)←(A)+[(Rr)]	r=0,1	↕ ↕	1
	ADD A, #i	00000011	03	(A)←(A)+i		↕ ↕	2
		iiiiiiii	ii				
	ADDC A, Rr	01111rrr	78+r	(A)←(A)+(Rr)+(C)	r=0~7	↕ ↕	1
	ADDC A, @Rr	0111000r	70+r	(A)←(A)+[(Rr)]+(C)	r=0,1	↕ ↕	1
	ADDC A, #i	00010011	13	(A)←(A)+i+(C)		↕ ↕	2
		iiiiiiii	ii				
	ANL A, Rr	01011rrr	58+r	(A)←(A) ∧(Rr)	r=0~7		1
	ANL A, @Rr	0101000r	50+r	(A)←(A) ∧[(Rr)]	r=0,1		1
	ANL A, #i	01010011	53	(A)←(A) ∧i			2
		iiiiiiii	ii				
	ORL A, Rr	01001rrr	48+r	(A)←(A) ∨(Rr)	r=0~7		1
	ORL A, @Rr	0100000r	40+r	(A)←(A) ∨[(Rr)]	r=0,1		1
	ORL A, #i	01000011	43	(A)←(A) ∨i			2
		iiiiiiii	ii				
	XRL A, Rr	11011rrr	D8+r	(A)←(A) ∀(Rr)	r=0~7		1
	XRL A, @Rr	1101000r	D0+r	(A)←(A) ∀[(Rr)]	r=0,1		1
	XRL A, #i	11010011	D3	(A)←(A) ∀i			2
		iiiiiiii	ii				
	INC A	00010111	17	(A)←(A)+1			1
	DEC A	00000111	07	(A)←(A)-1			1
	CLR A	00100111	27	(A)←0			1
	CPL A	00110111	37	(A)←NOT(A)			1
	DA A	01010111	57	(A)←(A)BCD		↕	1
	SWAP A	01000111	47	(A)<7:4> ↔(A)<3:0>			1
	RL A	11100111	E7	(A)<n+1> ←(A)<n>			1
				(A)<0> ←(A)<7>	n=0~6		
	RLC A	11110111	F7	(A)<n+1> ←(A)<n>		↕	1
				(C)←(A)<7>			
				(A)<0> ←(C)	n=0~6		
	RR A	01110111	77	(A)<n> ←(A)<n+1>	n=0~6		1
				(A)<7> ←(A)<0>			
	RRC A	01100111	67	(A)<n> ←(A)<n+1>		↕	1
				(C)←(A)<0>			
				(A)<7> ←(C)	n=0~6		
I/O	IN A, Pp	000010pp	08+p	(A)←(Pp)	P=1,2		2

TLCS-48 LIST OF INSTRUCTIONS (2/4)

Class	Mnemonic	Object Code (1st) Bin.	(2nd) Hex.	Function		Flag C,AC	Cycle
	OUTL Pp, A	001110pp	38+p	(Pp) ←(A)	P=1,2		2
	ANL Pp, #i	100110pp	98+p	(Pp) ←(Pp)∧i	P=1,2		2
		iiiiiiii	ii				
	ORL Pp, #i	100010pp	88+p	(Pp) ←(Pp)∨i	P=1 2		2
		iiiiiiii	ii				
	INS A, BUS	00001000	08	(A)←(BUS)			2
	OUTL BUS, A	00000010	02	(BUS)←(AC)			2
	ANL BUS, #i	10011000	98	(BUS)←(BUS) ∧i			2
		iiiiiiii	ii				
	ORL BUS, #i	10001000	88	(BUS)←(BUS) ∨i			2
		iiiiiiii	ii				
	MOVD A, Pp	000011pp	0C+p	(A)<3 0> ←(Pp)	p=4~7		2
				(A)<7·4> ←0			
	MOVD Pp, A	001111pp	3C+p	(Pp) ←(A)<3 0>	p=4~7		2
	ANLD Pp, A	100111pp	9C+p	(Pp) ←(Pp)∧(A)<3 0>	p=4~7		2
	ORLD Pp, A	100011pp	8C+p	(Pp) ←(Pp)∨(A)<3 0>	p=4~7		2
	INC Rr	00011rrr	18+r	(Rr) ←(Rr)+1	r=0~7		1
(1)	INC @Rr	0001000r	10+r	[(Rr)] ←[(Rr)]+1	r=0,1		1
	DEC Rr	11001rrr	C8+r	(Rr) ←(Rr)-1	r=0~7		1
	JMP a	aH00100	aH+4	(PC)<10·0> ←a			2
		aML		(PC)<11> ←(DBF)			
	JMPP @A	10110011	B3	(PC)<7:0>←PRO[(PC)<11.8>・(A)]			2
	DJNZ Rr, a	11101rrr	E8+r	(Rr) ←(Rr)-1	r=0~7		2
		aHL		if(Rr) ≠0then(PC)<7:0>←aHL			
				else no operation			
	JC a	11110110	F6	if(C)=1 then(PC)<7.0>←aML			2
		aML		else no operation			
	JNC a	11100110	E6	if(C)=0 then(PC)<7·0>←aML			2
		aML		else no operation			
	JZ a	11000110	C6	if(A)=0 then(PC)<7.0>←aML			2
		aML		else no operation			
	JNZ a	10010110	96	if(A)≠0 then(PC)<7·0> ←aML			2
		aML		else no operation			
	JTO a	00110110	36	if T0=1 then(PC)<7.0>←aML			2
		aML		else no operation			

(1) ····· Register Instruction

TLCS-48 LIST OF INSTRUCTIONS (3/4)

Instructions	Assembler Mnemonic		Object Code (1st) (2nd) Bin	Hex.	Function	Flag C,AC	Cycle
Branch Instruction	JNTO	a	00100110 aHL	26	if T0=0 then(PC)<7:0>←aHL else no operation		2
	JT1	a	01010110 aHL	56	if T1=1 then(PC)<7:0>←aHL else no operation		2
	JNT1	a	01000110 aHL	46	if T1=0 then(PC)<7:0>←aHL else no operation		2
	JF0	a	10110110 aHL	B6	if F0=1 then(PC)<7:0>←aHL else no operation		2
	JF1	a	01110110 aHL	76	if F1=1 then(PC)<7:0>←aHL else no operation		2
	JTF	a	00010110 aHL	16	if TF=1 then(PC)<7:0>←aHL else no operation		2
	JNI	a	10000110 aHL	86	if INT =0 then(PC)<7:0>←aHL else no operation		2
	JBb	a	bbb10010 aHL	b*12	if (A)<b>=1 then (PC)<7:0>←aHL else no operation b=0~7		2
(2)	CALL	a	aH10100 aHL	aH*14	[(SP)] ←(PSW)<7:4> • (PC) (SP) ←(SP)+1 (PC)<10:0> ←a (PC)<11> ←(DBF)		2
	RET		10000011	83	(SP) ←(SP)-1 (PC) ←[(SP)]<11:0>		2
	RETR		10010011	93	(SP) ←(SP)-1 (PC) ←[(SP)]<11:0> (PSW)<7:4> ←[(SP)]<15:12>	↕↕	2
(3)	CLR	C	10010111	97	(C)←0		1
	CPL	C	10100111	A7	(C)←NOT(C)		1
	CLR	F0	10000101	85	(F0) ←0		1
	CPL	F0	10010101	95	(F0) ←NOT(F0)		1
	CLR	F1	10100101	A5	(F1) ←0		1
	CPL	F1	10110101	B5	(F1) ←NOT(F1)		1
(4)	MOV	A , Rr	11111rrr	F8+r	(A)←(Rr) r=0~7		1
	MOV	A ,@Rr	1111000r	F0+r	(A)←[(Rr)] r=0,1		1
	MOV	A ,#i	00100011 iiiiiiii	23 ii	(A) ←i		2
	MOV	Rr, A	10101rrr	A8+r	(Rr)←(A) r=0~7		1
	MOV	@Rr, A	1010000r	A0+r	[(Rr)]←(A) r=0,1		1

(2) ····· Subroutine Instruction (3) ····· Flag Instruction
(4) ····· Move Instruction

TLCS-48 LIST OF INSTRUCTIONS (4/4)

Instructions	Assembler Mnemonic		Object Code (1st) (2nd) Bin.	Hex.	Function	Flag C AC	Cycle
Move Instruction	MOV	Rr,#i	10111rrr iiiiiiii	B8+r ii	(Rr)←i r=0~7		2
	MOV	@Rr,#i	1011000r iiiiiiii	B0+r ii	[(Rr)]←i r=0,1		2
	MOV	A,PSW	11000111	C7	(A) ←(PSW)		1
	MOV	PSW,A	11010111	D7	(PSW) ←(A)		1
	XCH	A,Rr	00101rrr	28+r	(A) ↔(Rr) r=0~7		1
	XCH	A,@Rr	0010000r	20+r	(A) ↔[(Rr)] r=0,1		1
	XCHD	A,@Rr	0011000r	30+r	(A)<3:0>↔[(Rr)<3:0>] r=0,1		1
	MOVX	@Rr,A	1001000r	90+r	EXT[(Rr)] ←(A) r=0,1		1
	MOVX	A,@Rr	1000000r	80+r	(A) ←EXT[(Rr)] r=0,1		1
	MOVP	A,@A	10100011	A3	(A) ←PRO[(PC)<11:8>・(A)]		1
	MOVP3	A,@A	11100011	E3	(A) ←PRO[(PC)<11>・011・(A)]		1
TC Instructions	MOV	A,T	01000010	42	(A) ←(TR)		1
	MOV	T,A	01100010	62	(TR)←(A)		1
	STRT	T	01010101	55	Start Timer		1
	STRT	CNT	01000101	45	Start counter		1
	STOP	TCNT	01100101	65	Stop Timer/Counter		1
	EN	TCNTI	00100101	25	Enable Timer/Counter Interrupt		1
	DIS	TCNTI	00110101	35	Disable Timer/Counter Interrupt		1
(5)							
Control Instructions	EN	I	00000101	05	Enable External Interrupt		1
	DIS	I	00010101	15	Disable External Interrupt		1
	SEL	RB0	11000101	C5	(BS)← 0		1
	SEL	RB1	11010101	D5	(BS)← 1		1
	SEL	MB0	11100101	E5	(DBF) ← 0		1
	SEL	MB1	11110101	F5	(DBF) ← 1		1
	ENTO	CLK	01110101	75	Enable Clock Output on T0		1
	HALT		00000001	01	Halt		1
(6)	NOP		00000000	00	no opration		1

(5) ····· A/D Converter Instruction (6) ····· Other

TMP80C50AP/TMP80C40AP/TMP80C50AF ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
VCC	VCC Supply Voltage (with respect to GND (VSS))	-0.5V to +7V
VINA	Input Voltage (Except EA)	-0.5V to VCC+0.5V
VINB	Input Voltage (Only EA)	-0.5V to 13V
PD	Power Dissipation (Ta=70°C)	250mW
TSOLDER	Soldering Temperature (Soldering Time 10 sec)	260°C
TSTG	Storage Temperature	-65°C to 150°C
TOPR	Operating Temperature	0°C to 70°C

DC CHARACTERISTICS

TOPR=0°C to 70°C, VCC=+5V±10%, VSS=0V, unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage (Except XTAL1, XTAL2, $\overline{RESET}$)			-0.5	-	0.8	V
VIL1	Input Low Voltage (XTAL1, XTAL2, $\overline{RESET}$)			-0.5	-	0.6	V
VIH	Input High Voltage (Except XTAL1, XTAL2, $\overline{RESET}$, $\overline{PS}$)			2.2	-	VCC	V
VIH1	Input High Voltage (XTAL1, XTAL2, $\overline{RESET}$, $\overline{PS}$)			0.7 x VCC	-	VCC	V
VOL	Output Low Voltage (Except P10-P17, P20-P27)		IOL=1.6mA	-	-	0.45	V
VOL1	Output Low Voltage (P10-P17, P20-P27)		IOL=1.2mA	-	-	0.45	V
VOH11	Output High Voltage (Except P10-P17, P20-P27)		IOH=-1.6mA	2.4	-	-	V
VOH12	Output High Voltage (Except P10-P17, P20-P27)		IOH=-400μA	VCC-0.8	-	-	V
VOH21	Output High Voltage (P10-P17, P20-P27)		IOH=-50μA	2.4	-	-	V
VOH22	Output High Voltage (P10-P17, P20-P27)		IOH=-25μA	VCC-0.8	-	-	V
ILI	Input Leak Current (T1, $\overline{INT}$, EA, $\overline{PS}$)		VSS≦VIN≦VCC	-	-	±10	μA
ILI1	Input Leak Current ($\overline{SS}$, $\overline{RESET}$)		VSS≦VIN≦VCC	-	-	-50	μA
ILI2	Input Leak Current (P10-P17, P20-P27)		VSS+0.45V≦VIN≦VCC	-	-	-500	μA
ILO	Output Leak Current (BUS, TO) (High impedance condition)		VSS+0.45V≦VIN≦VCC	-	-	±10	μA
ICC1	VCC Supply Current	Normal operation	VCC=5V, fXTAL=6MHz VIH=VCC-0.2V	-	-	10	mA
ICCH1		HALT Mode	VIL=0.2V	-	-	2.5	
ICC2	VCC Supply Current	Normal operation	VCC=5V, fXTAL=11MHz VIH=VCC-0.2V VIL=0.2V	-	-	15	μA
ICCH2		HALT Mode		-	-	4.0	

TMP80C50AP/TMP80C40AP/TMP80C50AF

AC CHARACTRISTICS

TOPR=0°C to 70°C, VCC=+5V±10%, VSS=0V, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITION	f(t)	11 MHz		UNIT
				MIN.	MAX.	
t	Clock Period	Note 2	1/xtal f	90.9	1000	ns
tLL	ALE Pulse Width		3.5t-170	150	-	ns
tAL	Address Setup Time (ALE)		2t-110	70	-	ns
tLA	Address Hold Time (ALE)	CL=20pF	t-40	50	-	ns
tCC1	Control Pulse Width ($\overline{RD}$, $\overline{WR}$)		7.5t-200	480	-	ns
tCC2	Control Pulse Width ($\overline{PSEN}$)		6t-200	350	-	ns
tDW	Data Setup Time ($\overline{WR}$)		6.5t-200	390	-	ns
tWD	Data Hold Time ($\overline{WR}$)	CL=20pF	t-50	40	-	ns
tDR	Data Hold Time ($\overline{RD}$, $\overline{PSEN}$)	CL=20pF	1.5t-30	0	110	ns
tRD1	Data Input Read Time ($\overline{RD}$)		6t-170	-	375	ns
tRD2	Data Input Read Time ($\overline{PSEN}$)		4.5t-170	-	240	ns
tAW	Address Setup Time ($\overline{WR}$)		5t-150	300	-	ns
tAD1	Address Setup Time ($\overline{RD}$)		10.5t-220	-	730	ns
tAD2	Address Setup Time ($\overline{PSEN}$)		7.5t-200	-	460	ns
tAFC1	Address Float Time ($\overline{RD}$, $\overline{WR}$)	CL=20pF	2t-40	140	-	ns
tAFC2	Address Float Time ($\overline{PSEN}$)	CL=20pF	0.5t-40	10	-	ns
tLAFC1	ALE to Control Time ($\overline{RD}$, $\overline{WR}$)		3t-75	200	-	ns
tLAFC2	ALE to Control Time ($\overline{PSEN}$)		1.5t-75	60	-	ns
tCA1	Control to ALE Time ($\overline{RD}$, $\overline{WR}$, PROG)		t-65	25	-	ns
tCA2	Control to ALE Time ($\overline{PSEN}$)		4t-70	290	-	ns
tCP	Port Control Setup Time (PROG)		1.5t-80	50	-	ns
tPC	Port Control Hold Time (PROG)		4t-260	100	-	ns
tPR	Port 2 Input Data Setup Time (PROG)		8.5t-120	-	650	ns
tPF	Port 2 Input Data Hold Time (PROG)		1.5t	0	140	ns
tDP	Port 2 Output Data Setup Time (PROG)		6t-290	250	-	ns
tPD	Port 2 Output Data Hold Time (PROG)		1.5t-90	40	-	ns

TMP 80 C50 AP / TMP 80 C40 AP / TMP 80 C50 AF

AC CHARACTRISTICS (CONTINUE)
TOPR=0°C to 70°C, VCC=+5V±10%, VSS=0V, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITION	f(t)	11 MHz		UNIT
				MIN.	MAX.	
tPP	PROG Pulse Width		10.5t-250	700	-	ns
tPL	Port 2 I/O Data Setup Time(ALE)		4t-200	160	-	ns
tLP	Port 2 I/O Data Hold Time (ALE)		1.5t-120	15	-	ns
tPV	Poer Output Delay Time (ALE)		4.5t+100	-	510	ns
tOPRR	TO Clock Period		3t	270	-	ns
tCY	Cycle Time		15t	1.36	15.0	μs

Note : 1. Control Output CL=80pF. BUS Output CL=150pF.
2. The f(t) assumes 50% duty cycle on XTAL1 and XTAL2.
The Max. Clock frequency is 11MHz. and the Min. Clock frequency is 1MHz.

TMP80C50AP-6/TMP80C40AP-6/TMP80C50AF-6 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
VCC	VCC Supply Voltage (with respect to GND (VSS))	-0.5V to +7V
VINA	Input Voltage (Except EA)	-0.5V to VCC+0.5V
VINB	Input Voltage (Only EA)	-0.5V to 13V
PD	Power Dissipation (Ta=85°C)	250mW
TSOLDER	Soldering Temperature (Soldering Timer 10 sec)	260°C
TSTG	Storage Temperature	-65°C to 150°C
TOPR	Operating Temperature	-40°C to 85°C

DC CHARACTERISTICS (I)

TOPR = -40°C to 85°C, VCC=+5V±10%, VSS=0V, unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage			-0.5	-	0.8	V
VIH	Input High Voltage (Except XTAL1, XTAL2, RESET, PS)			2.2	-	VCC	V
VIH1	Input High Voltage (XTAL1, XTAL2, RESET, PS)			0.7 x VCC	-	VCC	V
VOL	Output Low Voltage (Except P10-P17, P20-P27)		IOL=1.6mA	-	-	0.45	V
VOL1	Output Low Voltage (P10-P17, P20-P27)		IOL=1.2mA	-	-	0.45	V
VOH11	Output High Voltage (Except P10-P17, P20-P27)		IOH=-1.6mA	2.4	-	-	V
VOH12	Output High Voltage (Except P10-P17, P20-P27)		IOH=-400μA	VCC-0.8	-	-	V
VOH21	Output High Voltage (P10-P17, P20-P27)		IOH=-50μA	2.4	-	-	V
VOH22	Output High Voltage (P10-P17, P20-P27)		IOH=-25μA	VCC-0.8	-	-	V
ILI	Input Leak Current (T1, INT, EA, PS)		VSS≦VIN≦VCC	-	-	±10	μA
ILI1	Input Leak Current (SS, RESET)		VSS≦VIN≦VCC	-	-	-50	μA
ILI2	Input Leak Current (P10-P17, P20-P27)		VSS+0.45V≦VIN≦VCC	-	-	-500	μA
ILO	Output Leak Current (BUS, TO) (High impedance condition)		VSS+0.45V≦VIN≦VCC	-	-	±10	μA
ICC1	VCC Supply Current	Normal operation	VCC=5V, fXTAL=6MHz VIH=VCC-0.2V	-	-	10	mA
ICCH1		HALT Mode	VIL=0.2V	-	-	2.5	

TMP80C50AP-6/TMP80C40AP-6/TMP80C50AF-6 ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (II)

TOPR=-40°C to 85°C, VCC=+5V±20%, VSS=0V, unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage			-0.5	-	0.15 x VCC	V
VIH	Input High Voltage (Except XTAL1, XTAL2, RESET, PS)			0.5 x VCC	-	VCC	V
VIH1	Input High Voltage (XTAL1, XTAL2, RESET, PS)			0.7 x VCC	-	VCC	V
VOL	Output Low Voltage (Except P10-P17, P20-P27)		IOL=1.6mA	-	-	0.45	V
VOL1	Output Low Voltage (P10-P17, P20-P27)		IOL=1.2mA	-	-	0.45	V
VOH12	Output High Voltage (Except P10-P17, P20-P27)		IOH=-400μA	VCC-0.8	-	-	V
VOH22	Output High Voltage (P10-P17, P20-P27)		IOH=-25μA	VCC-0.8	-	-	V
ILI	Input Leak Current (T1, INT, EA, PS)		VSS≦VIN≦VCC	-	-	±10	μA
ILI1	Input Leak Current (SS, RESET)		VSS≦VIN≦VCC	-	-	-VCC/0.1	μA
ILI2	Input Leak Current (P10-P17, P20-P27)		VSS+0.45V≦VIN≦VCC	-	-	-VCC/0.01	μA
ILO	Output Leak Current (BUS, TO) (High impedance condition)		VSS+0.45V≦VIN≦VCC	-	-	±10	μA
ICC1	VCC Supply Current	Normal Operation	VCC=5V, fXTAL=6MHz VIH=VCC-0.2V, VIH=0.2V	-	-	10	mA
ICCH1		HALT Mode		-	-	2.5	

TMP80C50AP-6/TMP80C40AP-6/TMP80C50AF-6

AC CHARACTRISTICS

TOPR=-40°C to 85°C, VCC=+5V±20%, VSS=0V, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITION	f(t)	6 MHz		UNIT
				MIN.	MAX.	
t	Clock Period	Note 2	1/xtal f	166.6	1000	ns
tLL	ALE Pulse Width		3.5t-170	410	-	ns
tAL	Address Setup Time (ALE)		2t-110	220	-	ns
tLA	Address Hold Time (ALE)	CL=20pF	t-40	120	-	ns
tCC1	Control Pulse Width ($\overline{RD}$, $\overline{WR}$)		7.5t-200	1050	-	ns
tCC2	Control Pulse Width ($\overline{PSEN}$)		6t-200	800	-	ns
tDW	Data Setup Time ($\overline{WR}$)		6.5t-200	880	-	ns
tWD	Data Hold Time ($\overline{WR}$)	CL=20pF	t-50	120	-	ns
tDR	Data Hold Time ($\overline{RD}$, $\overline{PSEN}$)	CL=20pF	1.5t-30	0	220	ns
tRD1	Data Input Read Time ($\overline{RD}$)		6t-170	-	830	ns
tRD2	Data Input Read Time ($\overline{PSEN}$)		4.5t-170	-	580	ns
tAW	Address Setup Time ($\overline{WR}$)		5t-150	680	-	ns
tAD1	Address Setup Time ($\overline{RD}$)		10.5t-220	-	1530	ns
tAD2	Address Setup Time ($\overline{PSEN}$)		7.5t-200	-	1050	ns
tAFC1	Address Float Time ($\overline{RD}$, $\overline{WR}$)	CL=20pF	2t-40	290	-	ns
tAFC2	Address Float Time ($\overline{PSEN}$)	CL=20pF	0.5t-40	40	-	ns
tLAFC1	ALE to Control Time ($\overline{RD}$, $\overline{WR}$)		3t-75	420	-	ns
tLAFC2	ALE to Control Time ($\overline{PSEN}$)		1.5t-75	175	-	ns
tCA1	Control to ALE Time ($\overline{RD}$, $\overline{WR}$, PROG)		t-65	100	-	ns
tCA2	Control to ALE Time ($\overline{PSEN}$)		4t-70	590	-	ns
tCP	Port Control Setup Time (PROG)		1.5t-80	170	-	ns
tPC	Port Control Hold Time (PROG)		4t-260	400	-	ns
tPR	Port 2 Input Data Setup Time (PROG)		8.5t-120	-	1290	ns
tPF	Port 2 Input Data Hold Time (PROG)		1.5t	0	250	ns
tDP	Port 2 Output Data Setup Time (PROG)		6t-290	710	-	ns
tPD	Port 2 Output Data Hold Time (PROG)		1.5t-90	160	-	ns

TMP80C50AP-6/TMP80C40AP-6/TMP80C50AF-6

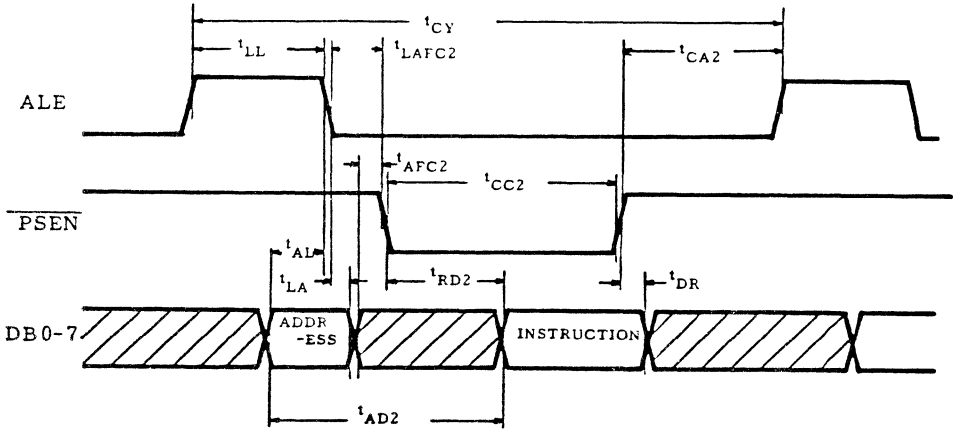
AC CHARACTRISTICS (CONTINUE)
TOPR=-40°C to 85°C, VCC=+5V±20%, VSS=0V, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITION	f(t)	6 MHz		UNIT
				MIN.	MAX.	
tPP	PROG Pulse Width		10.5t-250	1500	-	ns
tPL	Port 2 I/O Data Setup Time(ALE)		4t-200	460	-	ns
tLP	Port 2 I/O Data Hold Time (ALE)		0.5t-30	130	-	ns
tPV	Port Output Delay Time (ALE)		4.5t+100	-	850	ns
tOPRR	TO Clock Period		3t	500	-	ns
tCY	Cycle Time		15t	2.5	15.0	μs

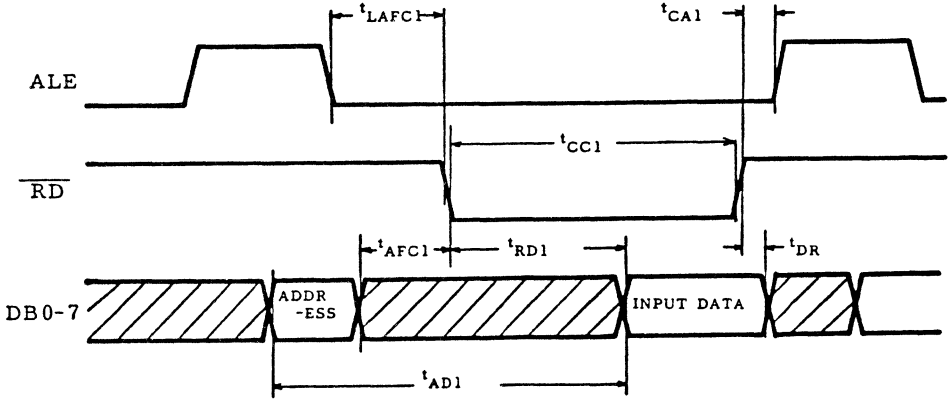
Note : 1. Control Output CL=80pF. BUS Output CL=150pF.
2. The f(t) assumes 50% duty cycle on XTAL1 and XTAL2.
The Max. Clock frequency is 6MHz. and the Min. Clock frequency is 1MHz.

TIMING WAVEFORM

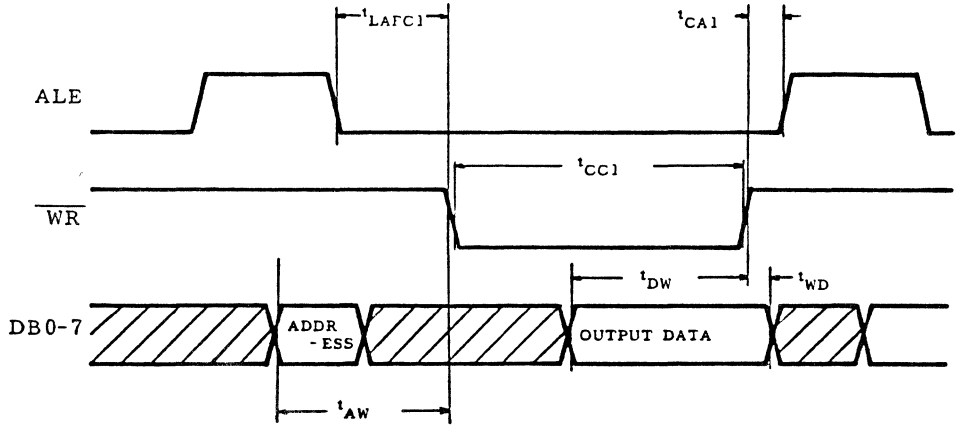
A. Instruction Fetch from External Program Memory



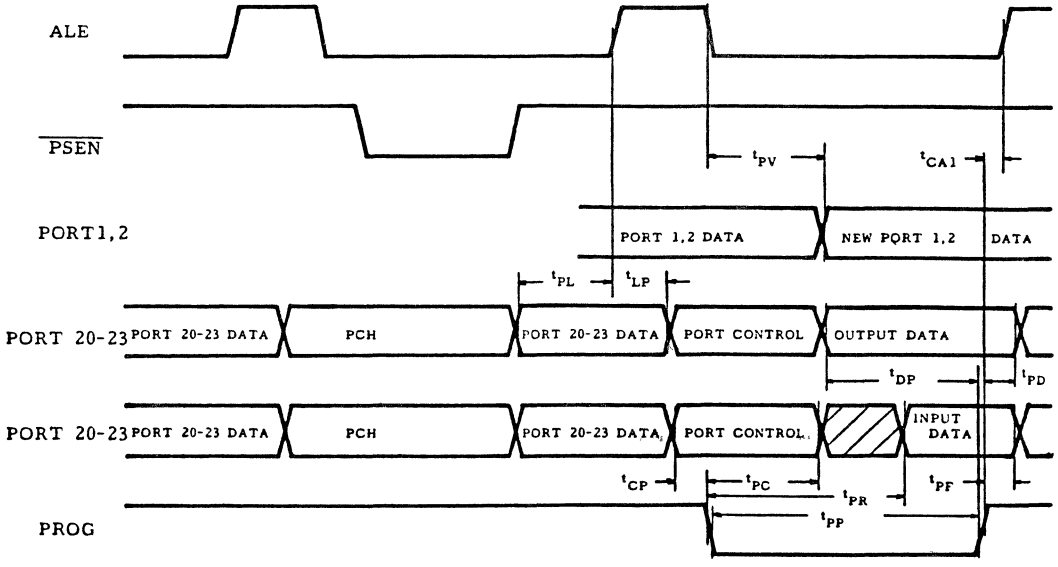
B. Read from External Data Memory



C. Write into External Data Memory



D. Timing of Port 2 during Expander Instruction Execution



POWER DOWN MODE (I) ..... Data Hold Mode in RAM

The operation of oscillation circuit is suspended by setting $\overline{PS}$ terminal to low level after $\overline{RESET}$ terminal has been set to low level. Consequently, all the data in RAM area can be held in low power consumption.

The minimum hold voltage of VCC in this mode is 2V.

$\overline{PS}$ terminal is set to high level to resume oscillation after VCC has been reset to 5V, and then $\overline{RESET}$ terminal is set to high level, thus, the normal mode is restarted from the initialize operation (address 0).

DC CHARACTERISTICS

TMP80C50AP/TMP80C40AP : TOPR=0°C to 70°C, VSS=0V
TMP80C50AP-6/TMP80C40AP-6 : TOPR=-40°C to 85°C, VSS=0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VSB1	Standby Voltage(1)		2.0	-	6.0	V
ISB1	Standby Current(1)	VCC=5V, VIH=VCC-0.2V, VIL=0.2V	-	0.5	10	μA

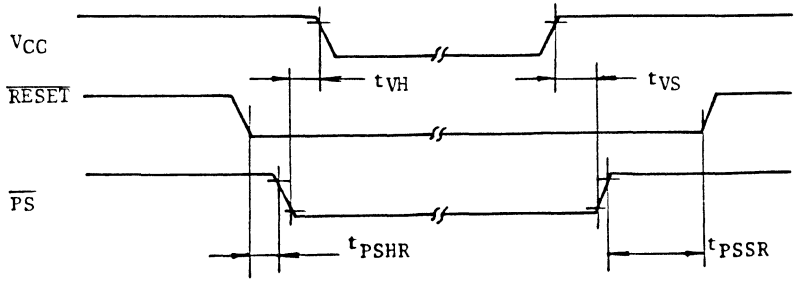
DC CHARACTERISTICS

TMP80C50AP/TMP80C40AP : TOPR=0°C to 70°C, VCC=5V±10%, VSS=0V
TMP80C50AP-6/TMP80C40AP-6 : TOPR=-40°C to 70°C, VCC=5V±20%, VSS=0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
tPSHR	Power Save Hold Time ($\overline{RESET}$)		10	-	-	μS
tPSSR	Power Save Setup Time ($\overline{RESET}$)		10	-	-	mS
tVH	VCC Hold Time ($\overline{PS}$)		5	-	-	μS
tVS	VCC Setup Time ($\overline{PS}$)		5	-	-	μS

Note: tCY=2.5μS (fXTAL=6MHz)

TIMING WAVEFORM



POWER DOWN MODE (II) ..... ALL Data Hold Mode

The operation of oscillation circuit is suspended by setting $\overline{PS}$ terminal to low level after $\overline{SS}$ terminal has been set to low level. Consequently, all data can be held in low power consumption.

The minimum hold voltage of VCC in this mode is 3V.

$\overline{PS}$ terminal is set to high level to resume oscillation after VCC has been reset to 5V, and then $\overline{SS}$ terminal is set to high level, thus, the normal mode is restarted continuously from the state just before the power down mode (II).

DC CHARACTERISTICS

TMP80C50AP/TMP80C40AP/TMP80C50AF: TOPR=0°C to 70°C, VSS=0V
TMP80C50AP-6/TMP80C40AP-6/TMP80C50AF-6: TOPR=-40°C to 85°C, VSS=0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VSB2	Standby Voltage(2)		3.0	-	6.0	V
ISB2	Standby Current(2)	VCC=5V, VIH=VCC-0.2V, VIL=0.2V	-	0.5	10	μA

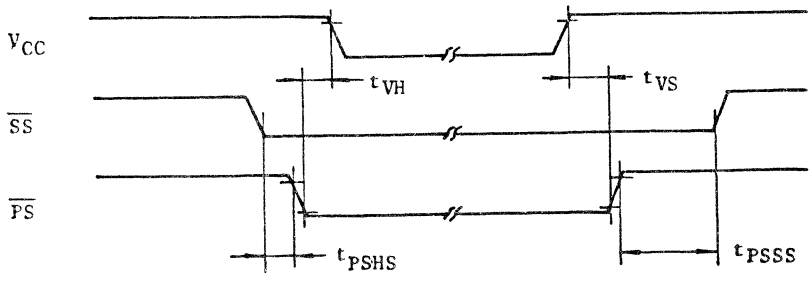
AC CHARACTERISTICS

TMP80C50AP/TMP80C40AP/TMP80C50AF: TOPR=0°C to 70°C, VCC=5V±10%, VSS=0V
TMP80C50AP-6/TMP80C40AP-6/TMP80C50AF-6: TOPR=-40°C to 85°C, VCC=5V±20%, VCC=0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
tPSHS	Power Save Hold Time ($\overline{SS}$)		10	-	-	μS
tPSSS	Power Save Setup Time ($\overline{SS}$)		10	-	-	mS
tVH	VCC Hold Time ($\overline{PS}$)		5	-	-	μS
tVS	VCC Setup Time ($\overline{PS}$)		5	-	-	μS

Note: tCY=2.5μS (fXTAL=6MHz)

TIMING WAVEFORM



HALT MODE

. 1 HALT INSTRUCTION

OP code is "01H". HALT INSTRUCTION is an additional instruction to the standard 8048/8049 instruction set.

. 2 Entry to HALT MODE

On the execution of HALT INSTRUCTION, TMP80C50A/TMP80C40A enter HALT MODE.

. 3 Status in HALT MODE

The oscillator continues its operation, however, the internal clocks and internal logic values just prior to the execution of HALT INSTRUCTION are maintained. Power consumption in HALT MODE is less than 50% of normal operation. The status of each pins are described in the following table.

. 4 Release from HALT MODE

HALT MODE is released by either of two signals ($\overline{\text{RESET}}$, $\overline{\text{INT}}$).

(1) $\overline{\text{RESET}}$ Release Mode : An active $\overline{\text{RESET}}$ input signal causes the normal reset function. TMP80C50A/TMP80C40A start the program at address "000 H".

(2) $\overline{\text{INT}}$ Release Mode : An active $\overline{\text{INT}}$ input signal causes the normal operation.

In case of interrupt enable mode (EI MODE), TMP80C50A/TMP80C40A execute the interrupt service routine, after the execution of one instruction which is located at the next address after HALT INSTRUCTION.

In case of interrupt disable mode (DI MODE), TMP80C50A/TMP80C40A execute normal operation from the next address after HALT INSTRUCTION.

. 5 Supply Voltage Range in HALT MODE

The operating supply voltage range and the operating temperature range are same as in normal operation.

PIN STATUS IN POWER DOWN MODE (I) (II)

PIN NAME	STATUS
DB0 - DB7 P10 - P17 P20 - P27	High impedance Input disabled
T0	High impedance, input disabled
T1	Input disabled
XTAL1	High impedance
XTAL2	Output "High" Level
$\overline{\text{RESET}}$, $\overline{\text{SS}}$	Input disabled when oscillator is stopped. Pull-up transistors turn off.
$\overline{\text{INT}}$, EA	Input disabled when oscilltor is stopped.
$\overline{\text{RD}}$, $\overline{\text{WR}}$, ALE PROG, $\overline{\text{PSEN}}$	High impedance

PIN STATUS IN HALT MODE

PIN NAME	STATUS
DB0 - DB7 P10 - P17 P20 - P27	Values prior to the execution of HALT INSTRUCTION are maintained.
T0	Status prior to the execution of HALT INSTRUCTION is maintained.
T1	Input disabled
XTAL1, XTAL2	Continue oscillation
$\overline{\text{RESET}}$, $\overline{\text{INT}}$	Input enabled
$\overline{\text{SS}}$, $\overline{\text{EA}}$	Input disabled
$\overline{\text{RD}}$, $\overline{\text{WR}}$, PROG, $\overline{\text{PSEN}}$	Output "High" level
ALE	Output "Low" level

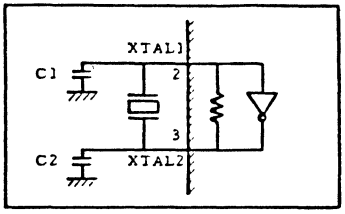
OSCILATOR

QUARTZ CRYSTAL

f = 1MHz to 4MHz : C1 = C2 = 30pF
f = 4MHz to 11MHz : C1 = C2 = 20pF

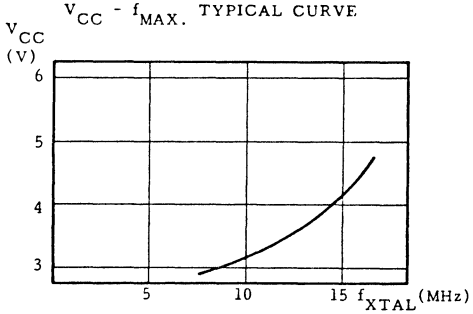
CERAMIC RESONATOR

f = 1MHz to 3MHz : C1 = C2 = 100pF
f = 3MHz to 11MHz : C1 = C2 = 30PF

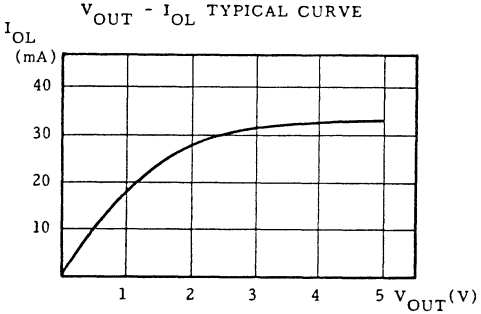


TYPICAL CHARACTARISTICS: Vcc = 5V, Ta = 25°C, unless otherwise noted.

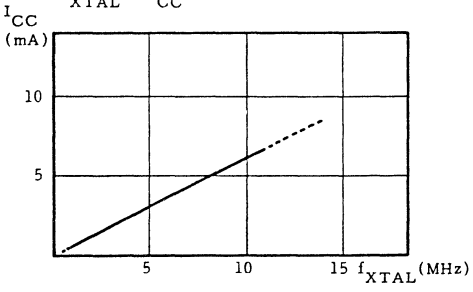
V_{CC} - $f_{MAX.}$ TYPICAL CURVE



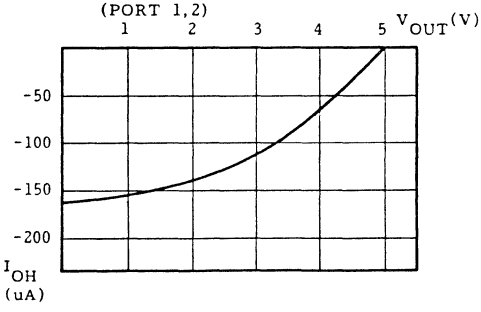
V_{OUT} - I_{OL} TYPICAL CURVE



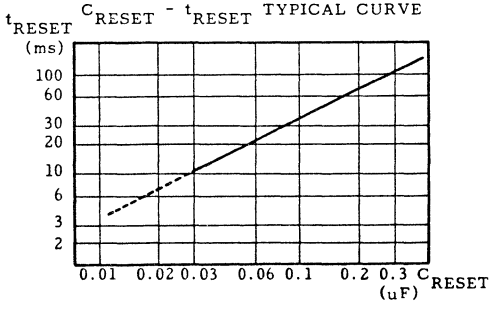
f_{XTAL} - I_{CC} TYPICAL CURVE



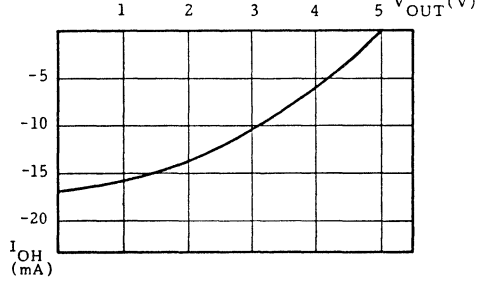
V_{OUT} - I_{OH} TYPICAL CURVE
(PORT 1,2)



t_{RESET} C_{RESET} - t_{RESET} TYPICAL CURVE

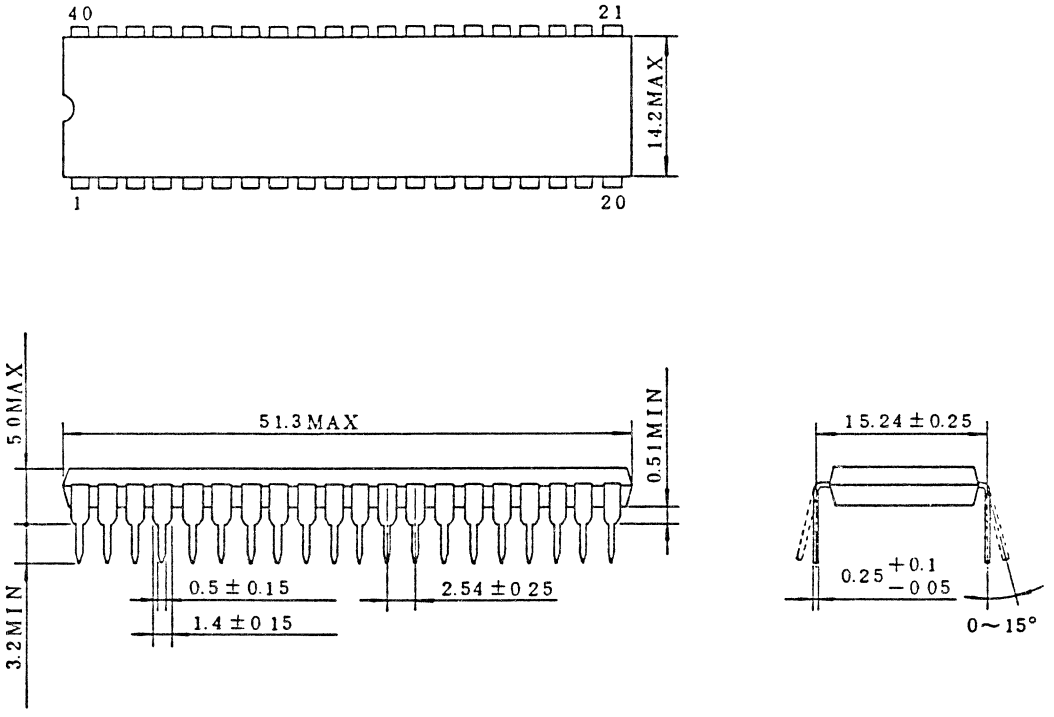


V_{OUT} - I_{OH} TYPICAL CURVE
(DB,CONTROL)



OUTLINE DRAWING

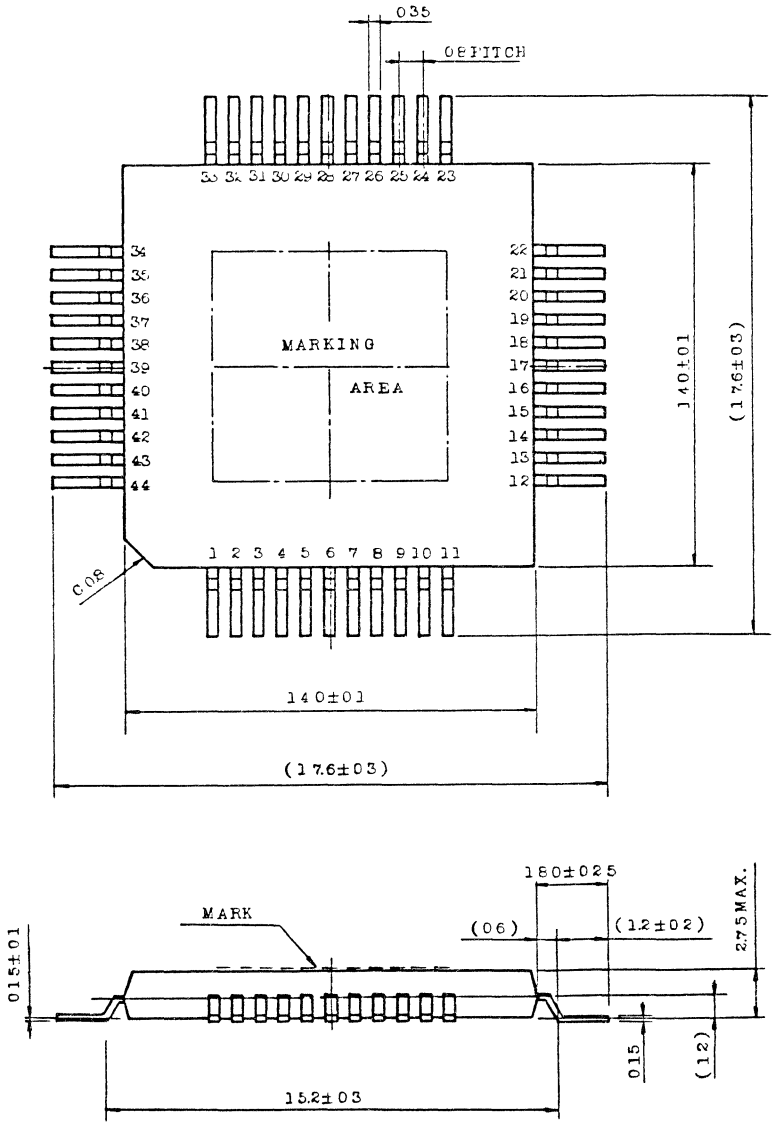
Unit in mm



Note: 1. This dimension is measured at the center of bending point of leads.
2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoritical positions with respect to No.1 and No.40 leads.

OUTLINE DRAWING (FLAT PACKAGE)

Unit in mm



8-BIT SINGLE-CHIP MICROCOMPUTER

GENERAL DESCRIPTION

The TMP8048PI, from here on referred to as the TMP8048, is a single chip microcomputer fabricated in N-channel Silicon Gate MOS technology which provides internal 8-bit parallel architecture.

The following basic architectural functions of a computer have been included in a single chip; an 8-bit CPU, 64 x 8 RAM data memory, 1K x 8 ROM program memory, 27 I/O lines and an 8-bit timer/event counter.

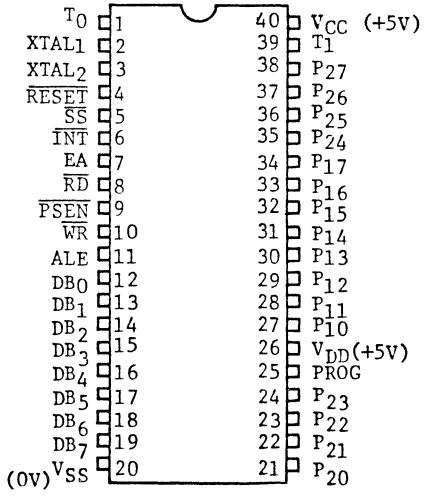
The TMP8048 is particularly efficient as a controller. It has extensive bit handing capability as well as facilities for both binary and BCD arithmetic.

The TMP8035PI is the equivalent of a TMP8048 without ROM program memory on chip. By using this device with external EPROM or RAM, software debugging becomes easy.

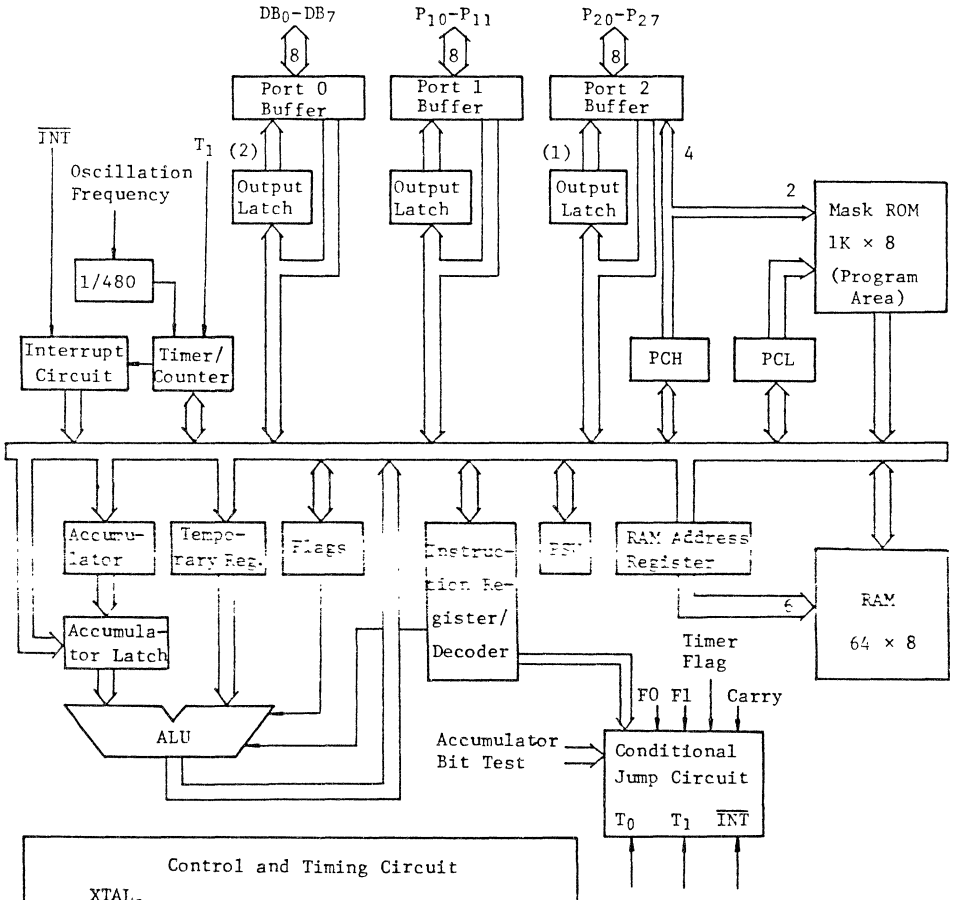
FEATURES

- 2.5 μS Instruction Cycle
- All instruction 1 or 2 cycles
- Over 90 instructions: 70% single byte
- Easy expandable memory and I/O
- 1K x 8 masked ROM
- 64 x 8 RAM
- 27 I/O lines
- Interval Timer Event Counter
- Single level interrupt
- Single 5V supply
  -40°C to +85°C Operation

PIN CONNECTIONS (Top View)



BLOCK DIAGRAM



Note 1) The lower order 4 bits of port 2 output latch are used also for input/output operations with the I/O expander.

Note 2) The output latch of port 0 is also used for address output.

PIN NAMES AND PIN DESCRIPTION

VSS (Power Supply)
Circuit GND potential

VDD (Power Supply)
+5V during operation Low power standby pin for TMP8048 RAM

VCC (Main Power Supply)
+5V during operation

PROG(Output)
Output strobe for the TMP8243P I/O expander

P10-P17 (Input/Output) Port 1
8-bit quasi -bidirectional port (Internal Pullup=50kΩ).

P20-P27 (Input/Output) Port 2
8-bit quasi-bidirectional port (Internal Pullup=50kΩ).
P20-P23 Contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for the TMP8243P.

DB0-DB7 (Input/Output, 3 State)
True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.

T0 (Input/Output)
Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.

T1 (Input)
Input pin testable using the JT1 and JNT1 instruction. Can be designated the event counter input using the timer/STRT CNT instruction.

$\overline{INT}$ (Input)
External interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active Low)

$\overline{RD}$ (Output)
Output strobe activated during a Bus read. Can be used to enable data onto the Bus from an external device. Used as a Read Strobe to External Data Memory (Active Low).

$\overline{WR}$ (Output)
Output strobe during a Bus write (Active Low) Used as a Write Strobe to External Data Memory.

RESET (Input)
Active Low signal which is used to initialize the Processor. Also used during Power down.

ALE (Output)
Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.

$\overline{\text{PSEN}}$ (Output)
Program Store Enable. This output occurs only during a fetch to external program memory (Active Low).

$\overline{\text{SS}}$ (Input)
Single step input can be used in conjunction with ALE to "single step" processor through each instruction when $\overline{\text{SS}}$ is low the CPU is placed into a wait state after it has completed the instruction being excuted.

EA (Input)
External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug and essential for testing and program verification. (Active High).

XTAL 1 (Input)
One side of crystal input for internal oscillator. Also input for external source.

XTAL 2 (Input)
Other side of crystal input.

FUNCTIONAL DESCRIPTION

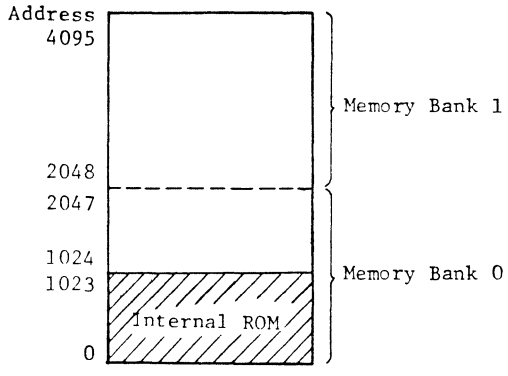
1. System Configuration

The following system functions of the TMP8048 are described in detail.

(1)	Program Memory	(6)	Stack (Stack Pointer)
(2)	Data Memory	(7)	Flag 0, Flag 1
(3)	I/O Port	(8)	Program Status Word (PSW)
(4)	Timer/Counter	(9)	Reset
(5)	Interrupt Control Circuit	(10)	Oscillator Circuit

(1) Program Memory
. The maximum memory that can be directly addressed by the TMP8048 is 4096 bytes. The first 1024 bytes from location 0 through 1023 can be internal resident mask ROM. The rest of the 3072 bytes of addressable memory are external to the chip. The TMP8035 has no internal resident memory; all memory must be external.

There are three locations in Program Memory of special importance.



Program Memory Area

. Location 0
Activating the Reset line of the processor causes the first instruction to be fetched from Location 0.

. Location 3
Activating the interrupt line of the processor (if interrupt enabled) causes a jump to subroutine defined by address held in Location 3.

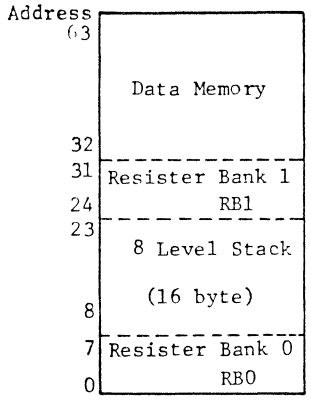
. Location 7
A timer/counter interrupt resulting from a timer/counter overflow (if enabled) causes a jump to a subroutine defined by address held in Location 7.

. Program address 0-2047 and 2048-4095 are called memory banks 0 and 1 respectively switching of memory banks is achieved by changing the most significant bit of the program counter (PC) during execution of an unconditional jump instruction or call instruction executed after using SEL MB0 or SEL MB1.

Reset operation automatically selects Bank 0.

(2) Data Memory

. Resident Data Memory (volatile RAM) is organized as 64 words by 8-bits wide.
. The first 8 locations (0 -7) of the memory array are designated as working registers and are directly addressable by several instructions. By executing a Register Bank switch instruction (SEL RB1) locations 24 - 31 are designated as the working registers in place of 0 - 7.



Internal Data Memory Area

. RAM locations 8 - 23 serve a dual role in that they contain the program counter stack which is a stack 2 bytes wide by 8 levels deep. These locations store returning addresses from subroutines. If the level of subroutine nesting is less than the permitted 8, you free up 2 bytes of RAM for general use for every level of nesting not utilized.

. All 64 locations are indirectly addressable through either of two RAM Pointer Registers which reside at R0 and R1 of the Register array.

. The TMP8048 architecture allows extension of the Data Memory to 256 words.

(3)Input/Output Ports

. The TMP8048 has 27 I/O lines which can be used for either input or output. These I/O lines are grouped into 3 ports each having 8 bidirectional lines and 3 "test" inputs which can alter program sequences when tested by conditional jump instructions.

. Ports 1 and 2 are each 8-bits wide and have identical characteristics. Data written to these ports is statically latched and remains unchanged until rewritten. As input ports these lines are non-latching, i.e., inputs must be present until read by an input instruction.

. All lines of Ports 1 and 2 are called quasi-bidirectional because of a special output circuit structure (illustrated in Figure 1). Each line is continously pulled to a +5V level through a high impedance resistive device (50kΩ) which is sufficient to provide the source current for a TTL high level yet can be pulled low by a standard TTL gate thus allowing the same pin to be used for both input and output. In order to speed up the "0" to "1" transition a low impedance device (5kΩ) is switched in momentarily whenever a "1" is written to line. When a "0" is written to line a low impedance device overcomes the pullup and provides TTL current sinking capability.

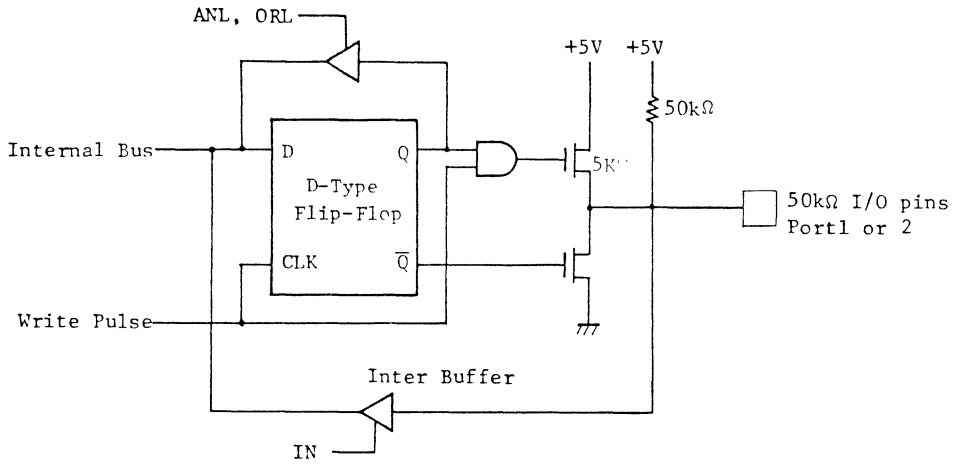


Fig.1 Input/Output Circuit of Port 1, Port 2

. Reset initializes all lines to a high impedance "1" state.

. When external data memory area is not addressed during excution of an internal program. Port 0 (DB0 - DB7) becomes a true bidirectional port bus with associated input and output strobes. If bidirectional feature not needed Bus can serve as either a statically latched output port or a non-latched input port. However, I/O lines of this port cannot be intermixed.

. As a static port data is written and latched using the OUTL instruction and inputted using the INS instruction these two commands generate pulses on the corresponding $\overline{RD}$ and $\overline{WR}$ strobe lines.

. As a bidirectional port the MOVX instructions are used to read and write the port which generate the $\overline{RD}$ and $\overline{WR}$ strobes.

. When not being written or read, the Bus lines are in a high impedance state.

(4)Timer/Event Counter

. The 8-bit binary up counter can use either of the following frequency inputs

(1) Internal clock (1/480 of OSC frequency)
..... Timer mode

(2) External input clock form T1 terminal
(minimum cycle time 3 x ALE cycle)
..... Event Counter mode

The counter is presettable and readable with two MOV instructions which transfer the content of the accumulator to the counter and vice versa. The counter content is not affected by a Reset and is initialized solely by the MOVT, A instruction. The counter is stopped by a Reset or STOP TCNT instruction and remains stopped until started by START T instruction or as an event counter by a START CNT. Once started the counter will increment to its maximum count (FF) and overflow to Zero continuing its count until stopped by a STOP TCNT instruction or RESET.

The increment from maximum count to Zero (overflow) results in the setting of an overflow flag and the generation of an interrupt request. When interrupt acknowledged a subroutine call to Location 7 will be initiated. Location 7 should store the starting address of the timer or counter service routine. The state of the overflow flag is testable with the conditional JUMP (JTF). The flag is reset by excuting a JTF or by RESET. Figure 2 illustrates the concept of the timer circuit.

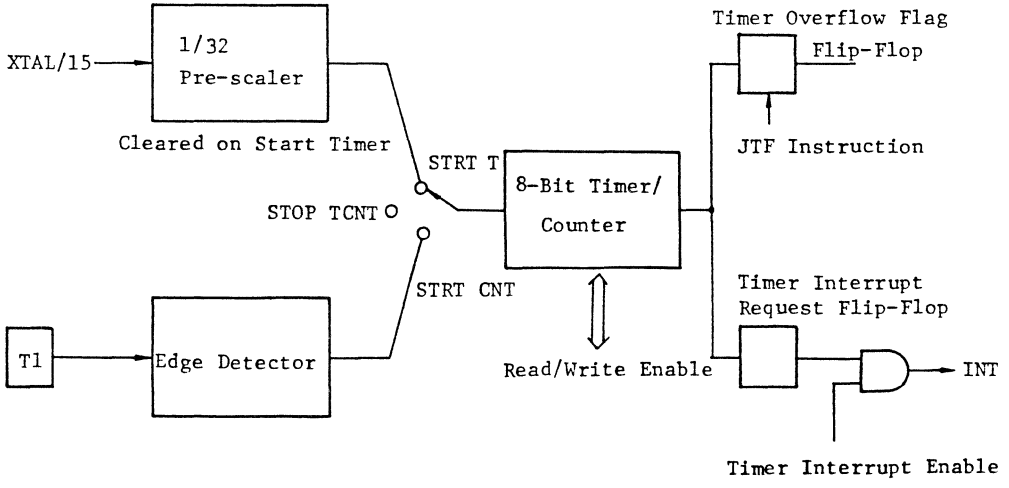


Fig.2 Concept of Timer Circuit

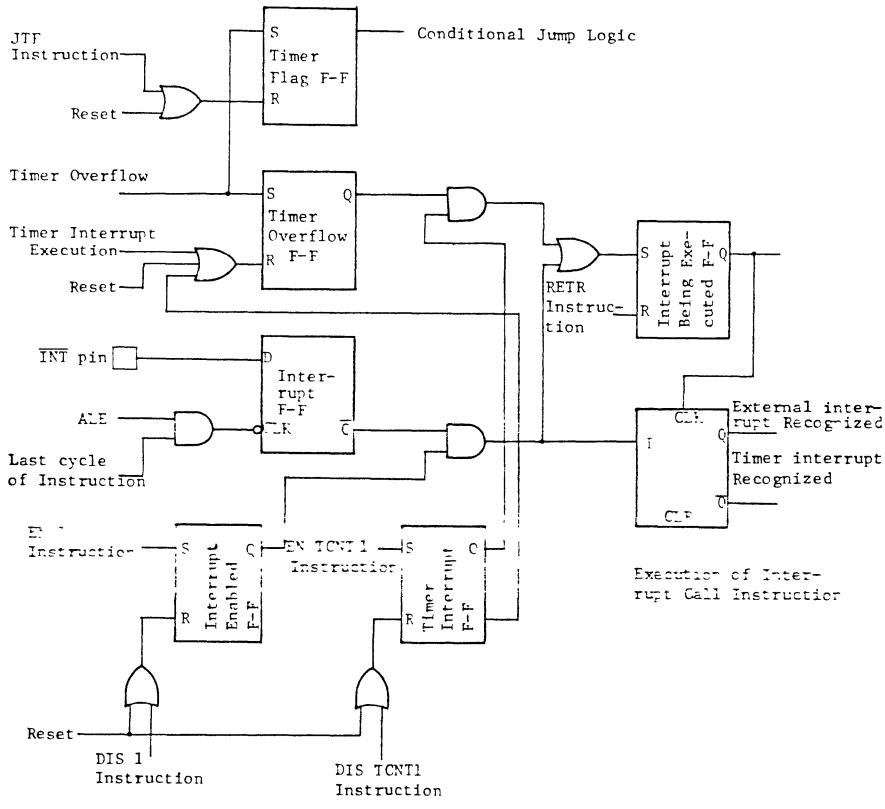


Fig.3 Concept of Interrupt Control Circuit

(5) Interrupt Control Circuit

. There are two distinct types of Interrupts in the TMP8048.

(1) External Interrupt from the $\overline{\text{INT}}$ terminal

(2) Timer Interrupt caused by timer overflow

The interrupt system is single level in that once an interrupt is detected all further interrupt requests are ignored until execution of an RETR (which should occur at the end of an interrupt service routine) reenables the interrupt input logic.

- An interrupt sequence is initiated by applying a low level "0" to the $\overline{INT}$ pin. $\overline{INT}$ is level triggered and active low which allows "Wire Oring" of several interrupt sources. The interrupt level is sampled every machine cycle during ALE and when detected causes a "jump to subroutine" at Location 3. As in any call to subroutine, the Program Counter and Program Status Word are saved in the stack.

- When an overflow occurs in the internal timer/event counter an interrupt request is generated which is reserviced as outlined in previous paragraph except that a jump to Location 7 is used instead of 3. If $\overline{INT}$ and times overflow occur simultaneously then external request $\overline{INT}$ takes precedence.

- If an extra external interrupt is needed in addition to $\overline{INT}$ this can be achieved by enabling the counter interrupt, loading FFH in the counter (one less than the terminal count), and enabling the event counter mode. A "1" to "0" transition on T1 will cause an interrupt vector to Location 7.

- The interrupt service routine pointed to be addresses in Location 3 or 7 must reside in memory between 0 and 2047, i.e., Bank 0.

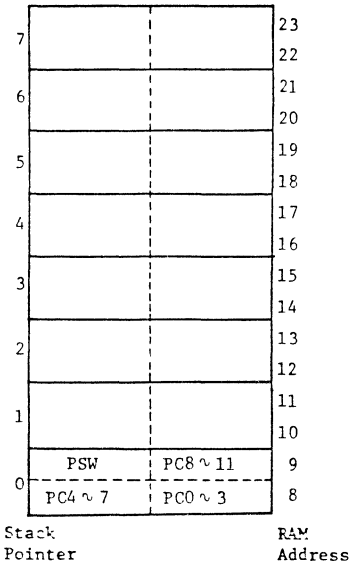
Figure 3 illustrates the concept of the interrupt control circuit.

(6) Stack (stack Pointer)

- An interrupt or Call to subroutine causes the contents of the program counter to be stored in one of the 8 register pairs of the Program Counter Stack. The pair to be used is determined by a 3-bit stack pointer which is part of the Program Status Words (PSW explained in section (8)). Data RAM locations, 8 through 23 are available as stack registers and are used to store the program counter and 4-bits of PSW as shown in the figure.

- The stack pointer when initialized points to RAM location 8 and 9. The first subroutine jump or interrupt results in the program counter contents being transferred to Locations 8 and 9. Then the stack pointer is incremented by one to point to Locations 10 and 11. Eight levels of subroutine are obviously possible.

- At the end of a subroutine signalled by a RET or RETR causes the stack pointer to be decremented by one and the contents of the resulting pair to be transferred to the Program Counter.



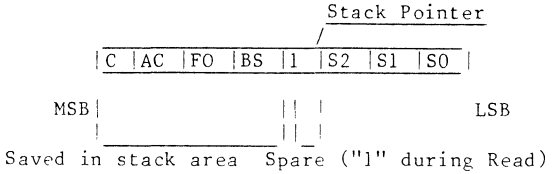
(7) Flag 0, Flag 1, (F0, F1)

. The TMP8048 has two flags F0 and F1 which are used for conditional jump. These flags can be set, reset and tested with the conditional jump instruction JF0.

. F0 is a part of the program status word (PSW) and is saved in the stack area when a subroutine is called.

(8) Program Status Word (PSW)

. An 8-bit status word which can be loaded to and from the accumlator exists called the Program Status Word (PSW). The PSW is read by a MOV A, PSW and written to by a MOV PSW, A. The information available in the PSW is shown in the diagram below.



Bits 0 - 2 : Stack Pointer Bits(S0, S1, S2)
Bit 3 : Not used ("1" level when read.)
Bit 4 : Working Register Bank Switch Bit (BS)

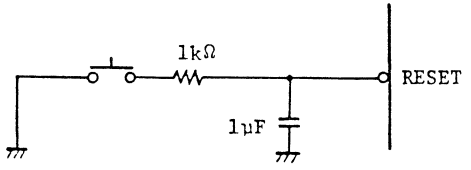
0 = Bank 0
1 = Bank 1

Bit 5 : Flag 0 (F0)
Bit 6 : Auxiliary Carry (AC) carry bit generated by an ADD instruction and used by the decimal adjust instruction DA, A (AC

Bit 7 : Carry (C) flag which indicates that the previous operation has resulted in the accumulator. (C)

(9) Reset

. The reset input provides a means for initialization of the processor. This Schmitt trigger input has an internal pullup registor which in combination with an external 1μF capacitor provides an internal reset pulse sufficient length to guarantee that all internal logic is initialized.



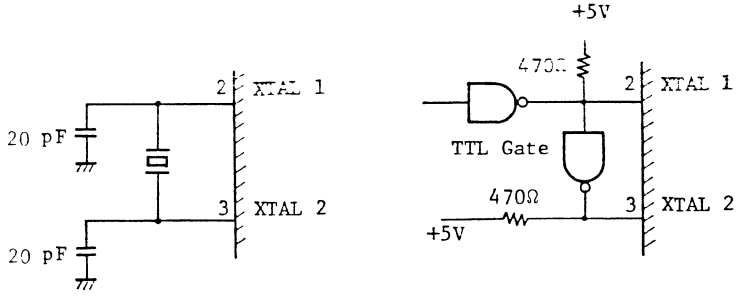
If the pulse is generated externally the reset pin must be held at ground ($\leq$0.5V) for at least 50mS after the power supply is within tolerance.

. Reset performs the following functions within the chip:

(i) Sets PC to Zero.
(ii) Sets Stack Pointer to Zero.
(iii) Selects Register Bank 0.
(iv) Selects Memory Bank 0.
(v) Sets BUS (DB0 - DB 7) to high impedance state. (Except when EA = 5V)
(vi) Sets Ports 1 and 2 to input mode.
(vii) Disables interrupts (timer and external).
(viii) Stops Timer.
(ix) Clears Timer Flag.
(x) Clears F0 and F1.
(xi) Disables clock output from T0.

(10) Oscillator Circuit

. TMP8048 can be operated by the external clock input in addition to crystal oscillator as shown below.



2. Basic Operation and Timing

The following basic operations and timing are explained
(1) Instruction Cycle
(2) External Memory Access Timing
(3) Interface with I/O Expander TMP8243P
(4) Internal Program Verify (Read) Timing
(5) Single Step Operation Timing
(6) Low Power Stand-by Mode

(1) Instruction Cycle

. The instructions of TMP8048 are executed in one or two machine cycles, and one machine cycle contents of five states.

. Fig.4 illustrates its relationship with the clock input to CPU.

. ϕ2 clock shown in Fig.4 is derived to outside by ENTO CLK instruction.

. ALE can be also used as the clock to indicate the machine cycle as well as giving the external address latch timing.

(2) External Memory Access Timing

(i) Program Memory Access

. TMP8048 programs are excuted in the following three modes.

(1) Execution of internal program only.
(2) Execution of both external and internal programs.
(3) Execution of external program only.

The external program memory is accessed (instructions are fetched) automatically when the internal ROM address is exceeded in mode (2) and from initial start address 0 in mode (3).

. In the external program memory access operation, the following will occur

. The contents of the 12-bit program counter will be output on BUS(DB0 - DB7) and the lower 4-bits of Port 2.
. Address Latch Enable (ALE) will indicate the time at which address is valid. The trailing edge of ALE is used to latch the address externally.
. Program Store Enable (PSEN) indicates that an external instruction fetch is in progress and serves to enable the external memory device.
. BUS (DB0 - DB7) reverts to Input mode and the processor accepts its 8-bit contents as an Instruction Word.

. Figure 5 illustrates the timing.

(ii) Access of External Data Memory

. In the extended data memory access operation during READ/WRITE cycle the following occurs
. The contents of R0 R1 is output onto BUS (DB0 - DB7).
. ALE indciates address is valid. The trailing edge of ALE is used to latch the address externally.
. A read $\overline{RD}$ or write $\overline{WR}$ pulse on the corresponding output pins indicates the type of data memory access in progress. Output data valid at trailing edge of $\overline{WR}$ and input data must be valid at trailing edge of $\overline{RD}$.
. Data (8-bits) is transferred over BUS.

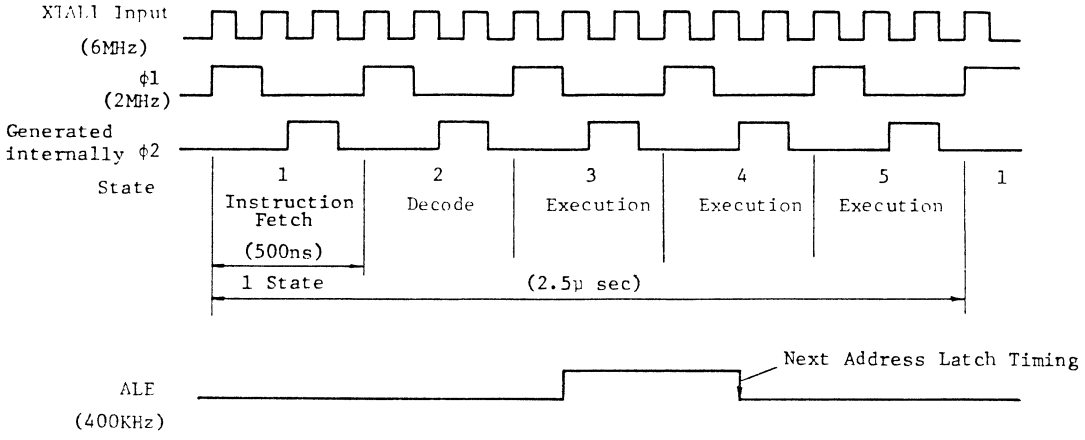


Fig.4 Instruction Cycle Timing

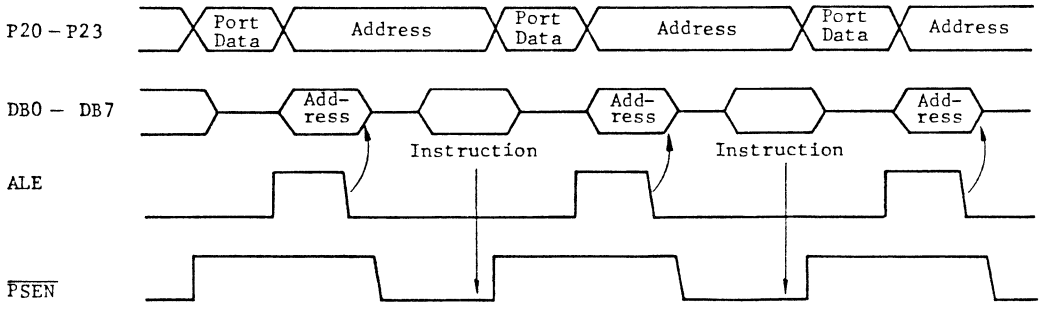
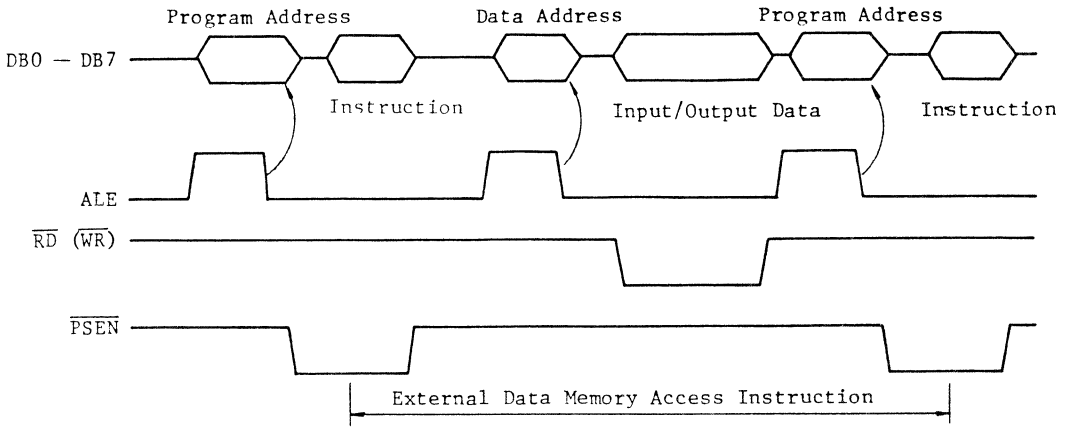


Fig. 5 Timing of External Program Memory Access



Suggest we have diagrams

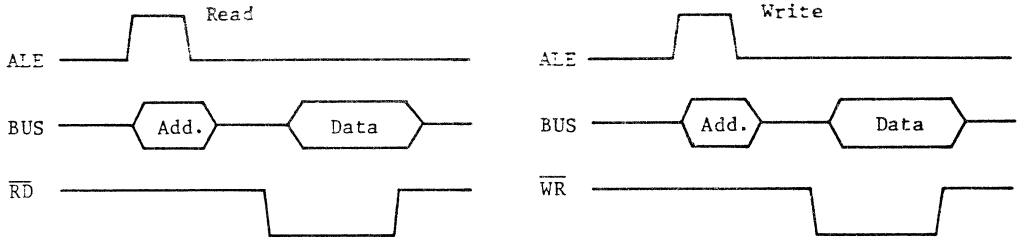


Fig.6 Timing of Accessing External Data Memory

Figure 6 illustrates the timing of accessing the external data memory during execution of external program.

(3) Interface with I/O Expander (TMP8243P)

The TMP8048 I/O can be easily expanded using the TMP8243 I/O Expander. THis device uses only the lower half 4-bits of Port 2 for commuication with the TMP8048. The TMP8243 contains four 4-bit I/O ports which serve as extensions of one chip I/O and are addressed as Ports (4-7). All communication takes place over the lower half of port 2 (P20 - P23) with timing provided by an output pulse on the PROG pin. Each transfer consists of two 4-bit nibbles the first containing the "OP Code" and port address and the second containing the actual 4-bits of data.

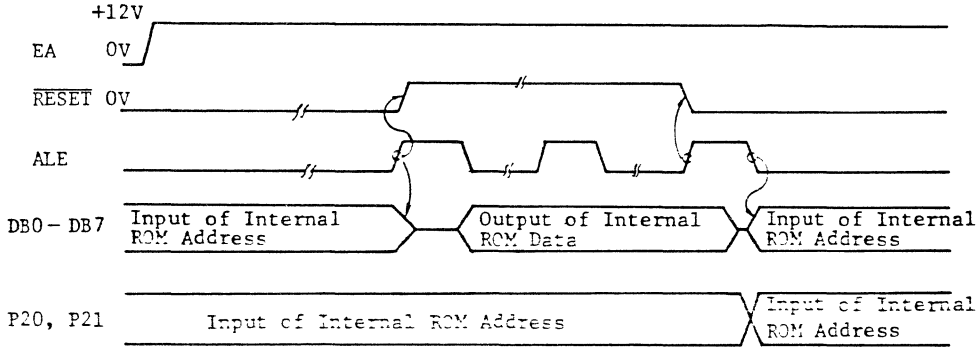


Fig.7 Timing of Reading Internal Program Memory

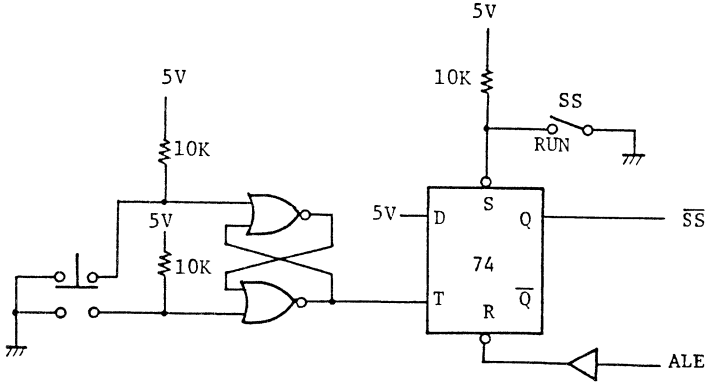


Fig.8 (a) Single Step Circuit

Reading of Internal Program Memory

- The processor is placed in the READ mode by applying +12V to the EA pin and 0V to the RESET pin. The address of the location to be read is then applied to BUS and the low order 2-bits of Port 2. The address is latched by a 0 to 1 transition on RESET and the high level causes the contents of program memory location addressed to appear on the eight lines of BUS.

- Figure 7 illustrates the timing diagram for this operation.

(5) Single Step Operation.

- A single step feature useful for debug can be implemented by utilizing a circuit shown in Figure 8 (a) combined with the $\overline{SS}$ pin and ALE pin.

- A D-type flip flop with set and reset is used to generate $\overline{SS}$. In the run mode $\overline{SS}$ is held high by keeping the flip flop set. To enter single step, set is removed allowing ALE to bring $\overline{SS}$ low via reset input. The next instruction is started by clocking a "1" into the FF which will not appear on $\overline{SS}$ unless ALE is high removing reset. In response to $\overline{SS}$ going high the processor begins an instruction fetch which brings ALE low resetting FF and causing the processor to again enter the stopped state.

- The timing diagram in this case is as shown in Figure 8 (b). (EA = 5V).

(6) Lower Power Stand-by Mode

- The Lower TMP8048 has been organized to allow power to be removed from all but the volatile, 64 x 8 data RAM array. In power down mode the contents of data RAM can be maintained while drawing typically 10 - 15% of normal operating power requirements.

- VCC serves as the 5V supply for the bulk of the TMP8048 while the VDD supplies only the RAM array. In standby mode VCC is reduced to 0V but VDD is kept at 5V. Applying a low level to reset inhibits any access to the RAM by the processor and guarantees that RAM cannot be inadvertently altered as power is removed from VCC.

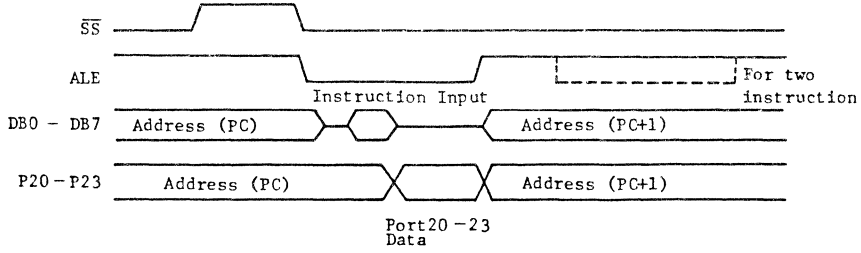


Fig.8(b) Single Step Operation Timing

INSTRUCTION

ACCUMULATOR INSTRUCTION

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
ADD A,Rr	0	1	1	0	1	r	r	r	(A)<-(A)+(Rr) r = 0 - 7	1	1	o	o
ADD A,@Rr	0	1	1	0	0	0	0	r	(A)<-(A)+((Rr)) r = 0, 1	1	1	o	o
ADD A,#Data	0	0	0	0	0	0	1	1	(A)<-(A)+Data	2	2	o	o
	d7	d6	d5	d4	d3	d2	d1	d0					
ADDC A,Rr	0	1	1	1	1	r	r	r	(A)<-(A)+(Rr)+(C) r = 0 - 7	1	1	o	o
ADDC A,@Rr	0	1	1	1	0	0	0	r	(A)<-(A)+((Rr))+(C) r = 0, 1	1	1	o	o
ADDC A,#Data	0	0	0	1	0	0	1	1	(A)<-(A)+Data+(C)	2	2	o	o
	d7	d6	d5	d4	d3	d2	d1	d0					
ANL A,Rr	0	1	0	1	1	r	r	r	(A)<-(A) and (Rr) r = 0 - 7	1	1	-	-
ANL A,@Rr	0	1	0	1	0	0	0	r	(A)<-(A)and ((Rr)) r = 0, 1	1	1	-	-
ANL A,#Data	0	1	0	1	0	0	1	1	(A)<-(A) and Data	2	2	-	-
	d7	d6	d5	d4	d3	d2	d1	d0					
ORL A,Rr	0	1	0	0	1	r	r	r	(A)<-(A) or (Rr) r = 0 - 7	1	1	-	-
ORL A,@Rr	0	1	0	0	0	0	0	r	(A)<-(A) or ((Rr)) r = 0, 1	1	1	-	-
ORL A,#Data	0	1	0	0	0	0	1	1	(A)<-(A) or Data	2	2	-	-
	d7	d6	d5	d4	d3	d2	d1	d0					
XRL A,Rr	1	1	0	1	1	r	r	r	(A)<-(A) EOR (Rr) r = 0 - 7	1	1	-	-
XRL A,@Rr	1	1	0	1	0	0	0	r	(A)<-(A) EOR((Rr)) r = 0, 1	1	1	-	-
XRL A,#Data	1	1	0	1	0	0	1	1	(A)<-(A) EOR Data	2	2	-	-
	d7	d6	d5	d4	d3	d2	d1	d0					
INC A	0	0	0	1	0	1	1	1	(A)<-(A)+1	1	1	-	-
DEC A	0	0	0	0	0	1	1	1	(A)<-(A)-1	1	1	-	-
CLR A	0	0	1	0	0	1	1	1	(A)<-0	1	1	-	-
CPL A	0	0	1	1	0	1	1	1	(A)<-NOT (A)	1	1	-	-
DA A	0	1	0	1	0	1	1	1	Decimal Adjust Accumulator	1	1	o	-
SWAP A	0	1	0	0	0	1	1	1	(A4-7)->(A0-3) <-	1	1	-	-

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
RL A	1	1	1	0	0	1	1	1	(An+1)<-(An)	1	1	-	-
									n = 0 - 6				
									(A0)<-(A7)				
RLC A	1	1	1	1	0	1	1	1	(An+1)<-(An)	1	1	-	-
									n = 0 - 6				
									(C)<-(A7)				
									(A0)<-(C)				
RR A	0	1	1	1	0	1	1	1	(An)<-(An+1)	1	1	-	-
									n = 0 - 6				
									(A7)<-(A0)				
RRC A	0	1	1	0	0	1	1	1	(An)<-(An+1)	1	1	-	-
									n = 0 - 6				
									(C)<-(A0)				
									(A7)<-(C)				

Input/Output Instruction

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
IN A,Pp	0	0	0	0	1	0	P	P	(A)<-(Pp)	1	2	-	-
									P = 1, 2				
OUTL Pp,A	0	0	1	1	1	0	P	P	(Pp)<-(A)	1	2	-	-
									P = 1, 2				
ANL Pp,#Data	1	0	0	1	1	0	P	P	Pp<-Pp and Data	2	2	-	-
	d7	d6	d5	d4	d3	d2	d1	d0	P = 1, 2				
ORL Pp,#Data	1	0	0	0	1	0	P	P	(Pp)<-(Pp)or Data	2	2	-	-
	d7	d6	d5	d4	d3	d2	d1	d0	P = 1, 2				
INS A,BUS	0	0	0	0	1	0	0	0	(A)<-(BUS)	1	2	-	-
OUTL BUS,A	0	0	0	0	0	0	1	0	(BUS)<-(A)	1	2	-	-
ANL BUS,#Data	1	0	0	1	1	0	0	0	(BUS)<-(BUS) and	2	2	-	-
	d7	d6	d5	d4	d3	d2	d1	d0	Data				
ORL BUS,#Data	1	0	0	0	1	0	0	0	(BUS)<-(BUS) or	2	2	-	-
	d7	d6	d5	d4	d3	d2	d1	d0	Data				
MOVD A,Pp	0	0	0	0	1	1	P	P	(A0-3)<-(Pp)	1	2	-	-
									(A4-7)<-0				
									P = 4 - 7				
MOVD Pp,A	0	0	1	1	1	1	P	P	(Pp)<-(A0-3)	1	2	-	-
									P = 4 - 7				
ANLD Pp,A	1	0	0	1	1	1	P	P	(Pp)<-(Pp)and	1	2	-	-
									(A0-3)				
									P = 4 - 7				
ORLD Pp,A	1	0	0	0	1	1	P	P	(Pp)<-(Pp)or(A0-3)	1	2	-	-
									P = 4 - 7				

Register Instruction

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
INC Rr	0	0	0	1	1	r	r	r	(Rr)<--(Rr)+1 r = 0 - 7	1	1	-	-
INC @Rr	0	0	0	1	0	0	0	r	((Rr))<-((Rr))+1 r = 0, 1	1	1	-	-
DEC Rr	1	1	0	0	1	r	r	r	(Rr)<--(Rr)-1 r = 0 - 7	1	1	-	-

Branch Instruction

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
JMP Address	a10	a9	a8	0	0	1	0	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	(PC8-10)<--(a8-10) (PC11)<--DBF				
JMPP @A	1	0	1	1	0	0	1	1	(PC0-7)<--((A))	1	2	-	-
DJNZ Rr,	1	1	1	0	1	r	r	r	(Rr)<--(Rr)-1	2	2	-	-
Address	a7	a6	a5	a4	a3	a2	a1	a0	if Rr not 0 (PC0-7)<--(a0-7)				
JC Address	1	1	1	1	0	1	1	0	(PC0-7)<--(a0-7) if C = 1	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	(PC) = (PC)+2 if C = 0				
JNC Address	1	1	1	0	0	1	1	0	(PC0-7)<-(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if C = 1 (PC)<-- (PC)+2 if C = 1				
JZ Address	1	1	0	0	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if (A) = 0 (PC)<--(PC)+2 if (A) .NEQ.0				
JNZ Address	1	0	0	1	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if (A) .NEQ.0 (PC)<--(PC)+2 if (A) = 0				
JTO Address	0	0	1	1	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if TO = 1 (PC)<--(PC)+2 if TO = 0				
JNTO Address	0	0	1	0	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if TO = 0 (PC)<--(PC)+2 if TO = 1				
JT1 Address	0	1	0	1	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if T1 = 1 (PC)<--(PC)+2 if T1 = 0				
JNT1 Address	0	1	0	0	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if T1 = 0 (PC)<--(PC)+2 if T1 = 1				

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
JF0 Address	1	0	1	1	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if F0 = 1				
									(PC)<--(PC)+2				
									if F0 = 0				
JF1 Address	0	1	1	1	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if F1 = 1				
									(PC)<--(PC)+2				
									if F1 = 0				
JTF Address	0	0	0	1	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if TF = 1				
									(PC)<--(PC)+2				
									if TF = 0				
JNI Address	1	0	0	0	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if INT = 0				
									(PC)<--(PC)+2				
									if INT = 1				
JBb Address	b2	b1	b0	1	0	0	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if Bb = 1				
									(PC)<-(PC)+2				
									if Bb = 0				
									(b = 0 - 7)				
CALL Address	a10	a9	a8	1	0	1	0	0	((SP))<--	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	(PC),(PSW4-7)				
									(SP)<--(SP)+1				
									(PC8-10)<--(a8-10)				
									(PC0-7)<--a0-7				
									(PC11)<--DBF				
RET	1	0	0	0	0	0	1	1	(SP)<--(SP)-1	1	2		
									(PC)<--((SP))				
RETR	1	0	0	1	0	0	1	1	(SP)<--(SP)-1	1	2		
									(PC)<--((SP))				
									(PSW4-7)<--((SP))				

Flag Manipulation Instruction

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
CLR C	1	0	0	1	0	1	1	1	(C)<-- 0	1	1	0	-
CPL C	1	0	1	0	0	1	1	1	(C)<--NOT(C)	1	1	0	-
CLR F0	1	0	0	0	0	1	0	1	(F0)<-- 0	1	1	-	-
CPL F0	1	0	0	1	0	1	0	1	(F0)<--NOT(F0)	1	1	-	-
CLR F1	1	0	1	0	0	1	0	1	(F1)<-- 0	1	1	-	-
CPL F1	1	0	1	1	0	1	0	1	(F1)<--NOT(F1)	1	1	-	-

Data Transfer Instruction

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
MOV A, Rr	1	1	1	1	1	r	r	r	(A)<-- (Rr) r = 0 - 7	1	1	-	-
MOV A, @Rr	1	1	1	1	0	0	0	r	(A)<-- ((Rr)) r = 0, 1	1	1	-	-
MOV A, #Data	0 d7	0 d6	1 d5	0 d4	0 d3	0 d2	1 d1	1 d0	(A)<--Data	2	2	-	-
MOV Rr, A	1	0	1	0	1	r	r	r	(Rr)<--(A) r = 0 - 7	1	1	-	-
MOV@Rr,A	1	0	1	0	0	0	0	r	((Rr))<-(A) r = 0, 1	1	1	-	-
MOV Rr,#Data	1 d7	0 d6	1 d5	1 d4	1 d3	r d2	r d1	r d0	(Rr)<--Data r = 0 - 7	2	2	-	-
MOV@Rr,#Data	1 a7	0 a6	1 a5	1 a4	0 a3	0 a2	0 a1	r a0	((Rr))<--Data r = 0, 1	2	2	-	-
MOV A,PSW	1	1	0	0	0	1	1	1	(A)<-- (PSW)	1	1	-	-
MOV PSW, A	1	1	0	1	0	1	1	1	(PSW)<--(A)	1	1	-	-
XCH A, Rr	0	0	1	0	1	r	r	r	(A)-->(Rr) <-- r = 0 - 7	1	1	-	-
XCH A,@Rr	0	0	1	0	0	0	0	r	(A)-->((Rr)) <-- r = 0, 1	1	1	-	-
XCHD A,@Rr	0	0	1	1	0	0	0	r	(A0-3)--((Rr)0-3) -- r = 0, 1	1	1	-	-
MOVX A,@Rr	1	0	0	0	0	0	0	r	(A)<--((Rr)) r = 0, 1	1	2	-	-
MOVX @Rr,A	1	0	0	1	0	0	0	r	((Rr))<--(A) r = 0, 1	1	2	-	-
MOVP A, @A	1	0	1	0	0	0	1	1	(PC0-7)<--(A) (A)<--((PC))	1	2	-	-
MOVP3 A,@A	1	1	1	1	0	0	0	1	(PC0-7)<--(A) (PC8-11)<--0011 (A)<--((PC))	1	2	-	-

Timer/Counter Instruction

Mnemonic	Instruction Code									Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
MOV A,T	0	1	0	0	0	0	1	0	(A)<--(T)	1	1	-	-
MOV T,A	0	1	1	0	0	0	1	0	(T)<--(A)	1	1	-	-
STRT T	0	1	0	1	0	1	0	1	Counting is started in the timer mode	1	1	-	-
STRT CNT	0	1	0	0	0	1	0	1	Counting is started in the event counter mode	1	1	-	-
STOP TCNT	0	1	1	0	0	1	0	1	Stop both time accumulation and event counting	1	1	-	-
EN TCNTI	0	0	1	0	0	1	0	1	Timer interrupt is enabled	1	1	-	-
DIS TCNTI	0	0	1	1	0	1	0	1	Timer interrupt is disabled	1	1	-	-

Control Instruction

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
EN I	0	0	0	0	0	1	0	1	External interrupt is enabled	1	1	-	-
DIS I	0	0	0	1	0	1	0	1	External interrupt is disabled	1	1	-	-
SEL RB0	1	1	0	0	0	1	0	1	(BS)<-- 0	1	1	-	-
SEL RB1	1	1	0	1	0	1	0	1	(BS)<-- 1	1	1	-	-
SEL MB0	1	1	1	0	0	1	0	1	(DBF)<-- 0	1	1	-	-
SEL MB1	1	1	1	1	0	1	0	1	(DBF)<-- 1	1	1	-	-
ENTO CLK	0	1	1	1	0	1	0	1	TO is enabled to act as the clock output	1	1	-	-
NOP	0	0	0	0	0	0	0	0	No operation	1	1	-	-

TMP8048PI/8035PI: INDUSTRIAL SPECIFICATION

ABSOLUTE MAXIMUM RATTINGS

SYMBOL	ITEM	RATTING
VDD	VDD Supply Voltage (with respect to GND (VSS))	-0.5V to + 7V
VCC	VCC Supply Voltage (with respect to GND (VSS))	-0.5V to + 7V
VINA	Input Voltage (Except EA)	-0.5V to + 7V
VINB	Input Voltage (Only EA)	-0.5V to + 13V
PD	Power Dissipation (Ta = 70°C)	1.5W
TSOLDER	Soldering Temperature (Soldering Time 10 sec)	260°C
TSTG	Storage Temperature	-55°C to 150°C
TOPR	Operating Temperature	-40°C to 85°C

DC CHARACTERISTICS

TA=-40°C to 85°C, VCC=VDD=+5V±10%, VSS=0V, Unless Otherwise Noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage (Except XTAL1,XTAL2,$\overline{\text{RESET}}$)		-0.5	-	0.7	V
VIL1	Input Low Voltage (XTAL1,XTAL2,$\overline{\text{RESET}}$)		-0.5	-	0.6	V
VIH	Input High Voltage (Except XTAL1,XTAL2,$\overline{\text{RESET}}$)		2.2	-	VCC	V
VIH1	Input High Voltage (XTAL1,XTAL2,$\overline{\text{RESET}}$)		3.8	-	VCC	V
VOL	Output Low Voltage (BUS)	IOL = 1.6 mA	-	-	0.45	V
VOL1	Output Low Voltage ($\overline{\text{RD}}$, $\overline{\text{WR}}$, PSEN, ALE)	IOL = 1.6 mA	-	-	0.45	V
VOL2	Output Low Voltage (PROG)	IOL = 0.8 mA	-	-	0.45	V
VOL3	Output Low Voltage (For other output pins)	IOL = 1.2 mA	-	-	0.45	V
VOH	Output High Voltage (BUS)	IOH =-280μA	2.4	-	-	V
VOH1	Output High Voltage ($\overline{\text{RD}}$, $\overline{\text{WR}}$, PSEN, ALE)	IOH =-80μA	2.4	-	-	V
VOH2	Output High Voltage (For other output pins)	IOH =-30μA	2.4	-	-	V
ILI	Input Leak Current (T1, $\overline{\text{INT}}$)	VSS $\leqq$ VIN $\leqq$ VCC	-	-	±10	μA
ILI1	Input Leak Current (P10-17, P20-P27, EA, $\overline{\text{SS}}$)	VSS+0.45$\leqq$VIN$\leqq$VCC	-	-	-700	μA
ILO	Output Leak Current (BUS, TO) (High impedance condition)	VSS+0.45$\leqq$VIN$\leqq$VCC	-	-	±10	μA
IDD	VDD Supply Current		-	-	20	mA
IDD+ICC	Total Supply Current		-	-	145	mA

AC CHARACTERISTICS

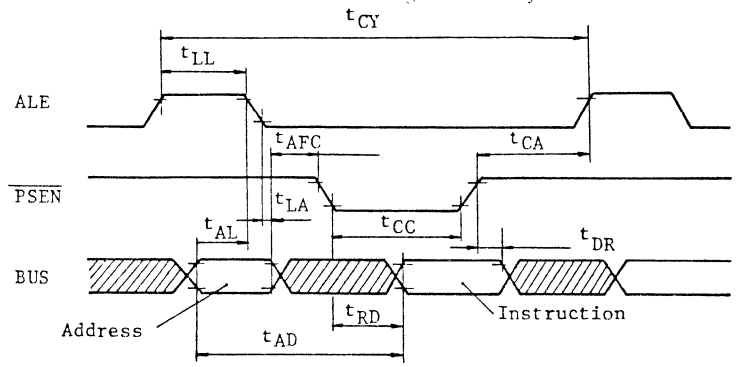
T_A=-40°C to 85°C, VCC=VDD=+5V±10%, VSS=0V, Unless Otherwise Noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
tLL	ALE Pulse Width		200	-	-	ns
tAL	Address Setup Time (ALE)		120	-	-	ns
tLA	Address Hold time (ALE)		80	-	-	ns
tCC	Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)		400	-	-	ns
tDW	Data Setup Time ($\overline{WR}$)		420	-	-	ns
tWD	Data Hold Time ($\overline{WR}$)		80	-	-	ns
tCY	Cycle Time		2.5	-	15.0	μs
tDR	Data Hold Time ($\overline{PSEN}$, $\overline{RD}$)	CL = 20 pF	0	-	200	ns
tRD	Data Input Read Time ($\overline{PSEN}$, $\overline{RD}$)		-	-	400	ns
tAW	Address Setup Time ($\overline{WR}$)		230	-	-	ns
tAD	Address Setup Time (Data Input)		-	-	600	ns
tAFC	Address Float Time ($\overline{RD}$, $\overline{PSEN}$)		-40	-	-	ns
tCA	Internal between Control Pulse and ALE		10	-	-	ns
tCP	Port Control Setup Time (PROG)		115	-	-	ns
tPC	Port Control Hold Time (PROG)		65	-	-	ns
tPR	Port 2 Input Data Set Time (PROG)		-	-	860	ns
tDP	Output Data Setup Time (PROG)		230	-	-	ns
tPD	Output Data Hold Time (PROG)		25	-	-	ns
tPF	Port 2 Input Data Hold Time (PROG)		0	-	160	ns
tPP	PROG Pulse Width		920	-	-	ns
tPL	Port 2 I/O Data Setup Time		300	-	-	ns
tLP	Port 2 I/O Data Hold Time		120	-	-	ns

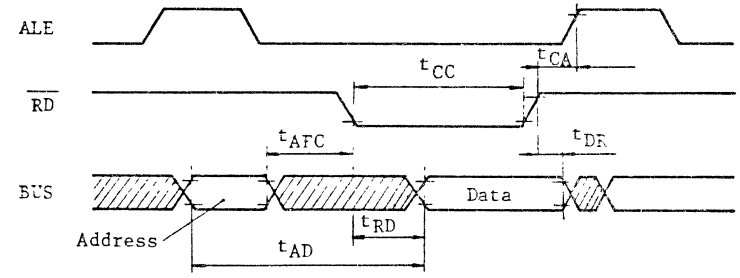
Note : t_{CY}=2.5μs, Control Output: CL=80pF, BUS Output: CL=150pF, PORT20-23: CL=80pF.

TIMING WAVEFORM

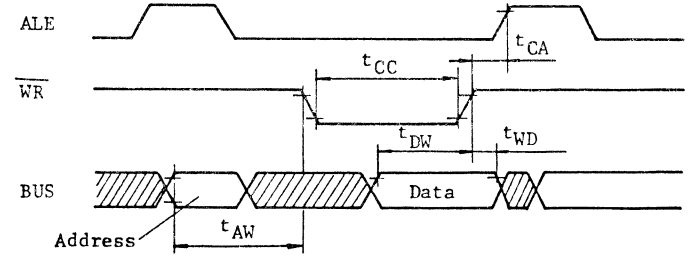
A. Instruction Fetch from External Program Memory



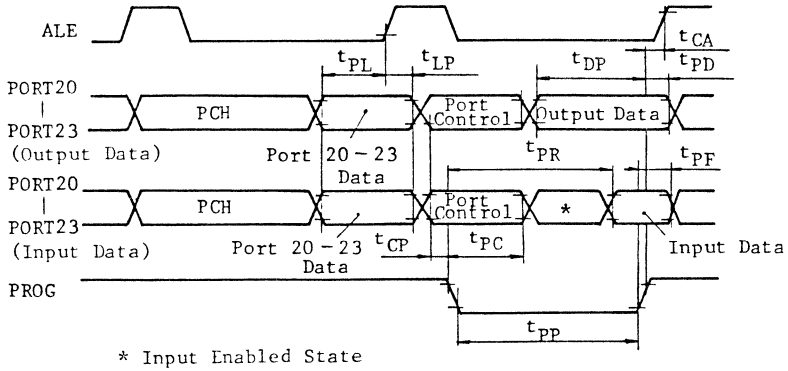
B. Read from External Data Memory



C. Write into External Data Memory



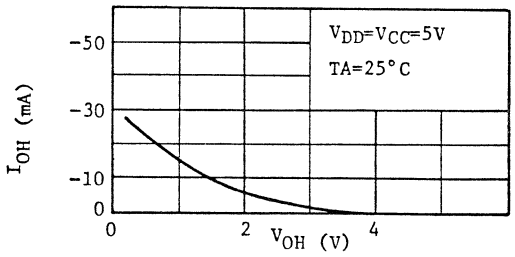
D. Timing of Port 2 during Expander Instruction Execution



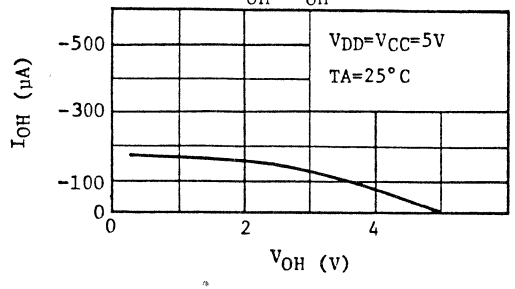
* Input Enabled State

TYPICAL CHARACTERISTICS

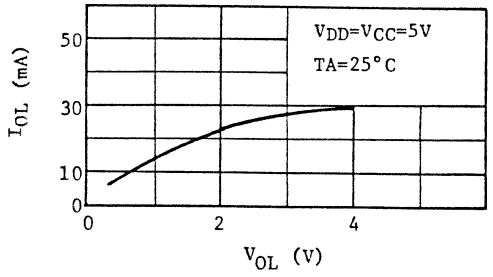
1) BUS: I_{OH} - V_{OH}



2) P1, P2: I_{OH} - V_{OH}



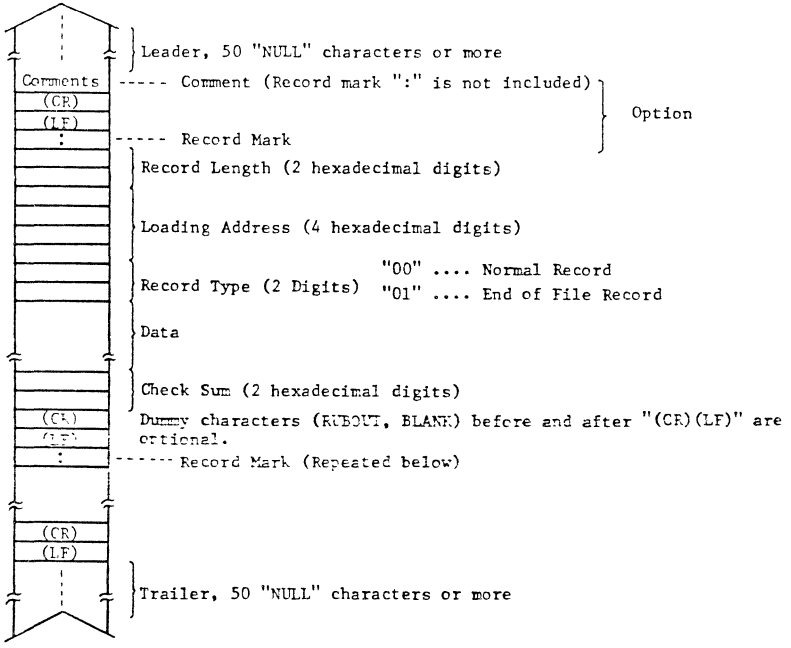
3) BUS, P1, P2: I_{OL} - V_{OL}



PROGRAM TAPE FORMAT

TMP8048 programs are delivered in the form of paper tape with the following format and it is required to attach the tape list. The format of paper tape is same as the Intel type object tape (hexadecimal tape output by Intel MDS system, PROMPT 48 Development Tool, etc.)

(1) Tape Format

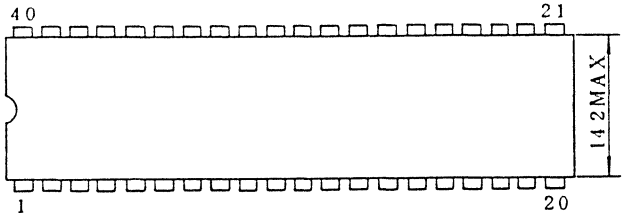


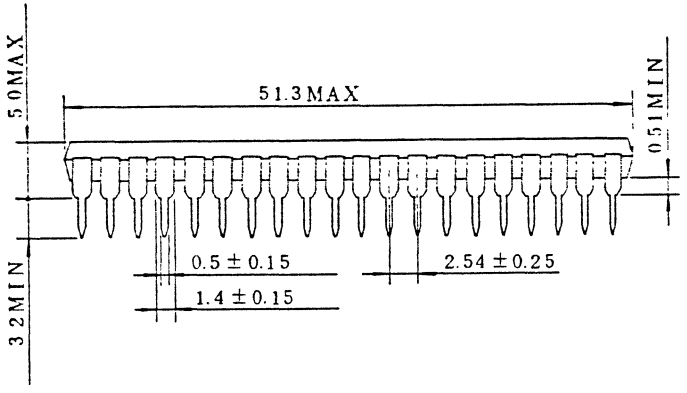
(2) Example of Tape List

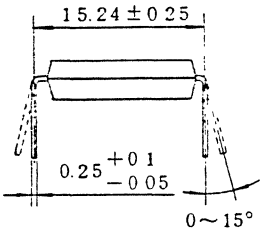
```
TOSHIBA MICRO COMPUTER TLCS-48
:100000000665C7D79CF50F3F951FED55A8FF16E570
:1000100088884DDE67D31F5D8ABA6DF292F113F5C1
:100020004FF1FB5DFFDAA96A99CF7DF94A346B7C09
:10003000197352F729F12F79AA9C057C5B851EED77
                    :
                    :
                    :
                    :
:1003C0005DFDB5E556A67277F61A51C631CF9F0E80
:1003D000BD2F6F20E8BB1977E3FB5AD1F41FDAA7E2
:1003E000B53D42E0EC32546025B7308CDD52063D1D
:1003F000B4BE9E9E345B6138060B20VC372BF60BD6
:00000001FF
```

OUTLINE DRAWING

Unit in mm







Note: 1. This dimension is measured at the center of bending point of leads.
2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoritical positions with respect to No.1 and No.40 leads.

8-BIT SINGLE-CHIP MICROCOMPUTER

GENERAL DESCRIPTION

The TMP8049PI-6, from here on referred to as the TMP8049, is a single chip microcomputer fabricated in N-channel Silicon Gate MOS technology which provides internal 8-bit parallel architecture.

The following basic architectural functions of a computer have been included in a single chip; an 8-bit CPU, 128 x 8 RAM data memory, 2K x 8 ROM program memory, 27 I/O lines and an 8-bit timer/event counter.

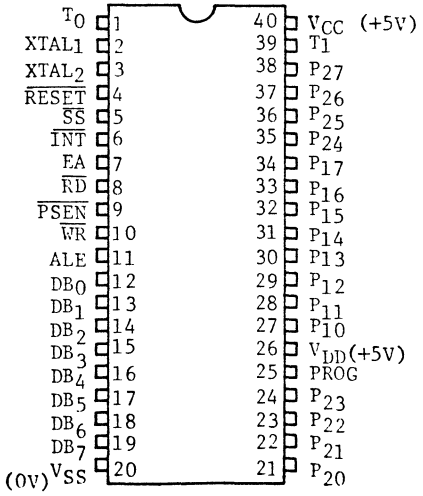
The TMP8049 is particularly efficient as a controller. It has extensive bit handing capability as well as facilities for both binary and BCD arithmetic.

The TMP8039PI is the equivalent of a TMP8049 without ROM program memory on chip. By using this device with external EPROM or RAM, software debugging becomes easy.

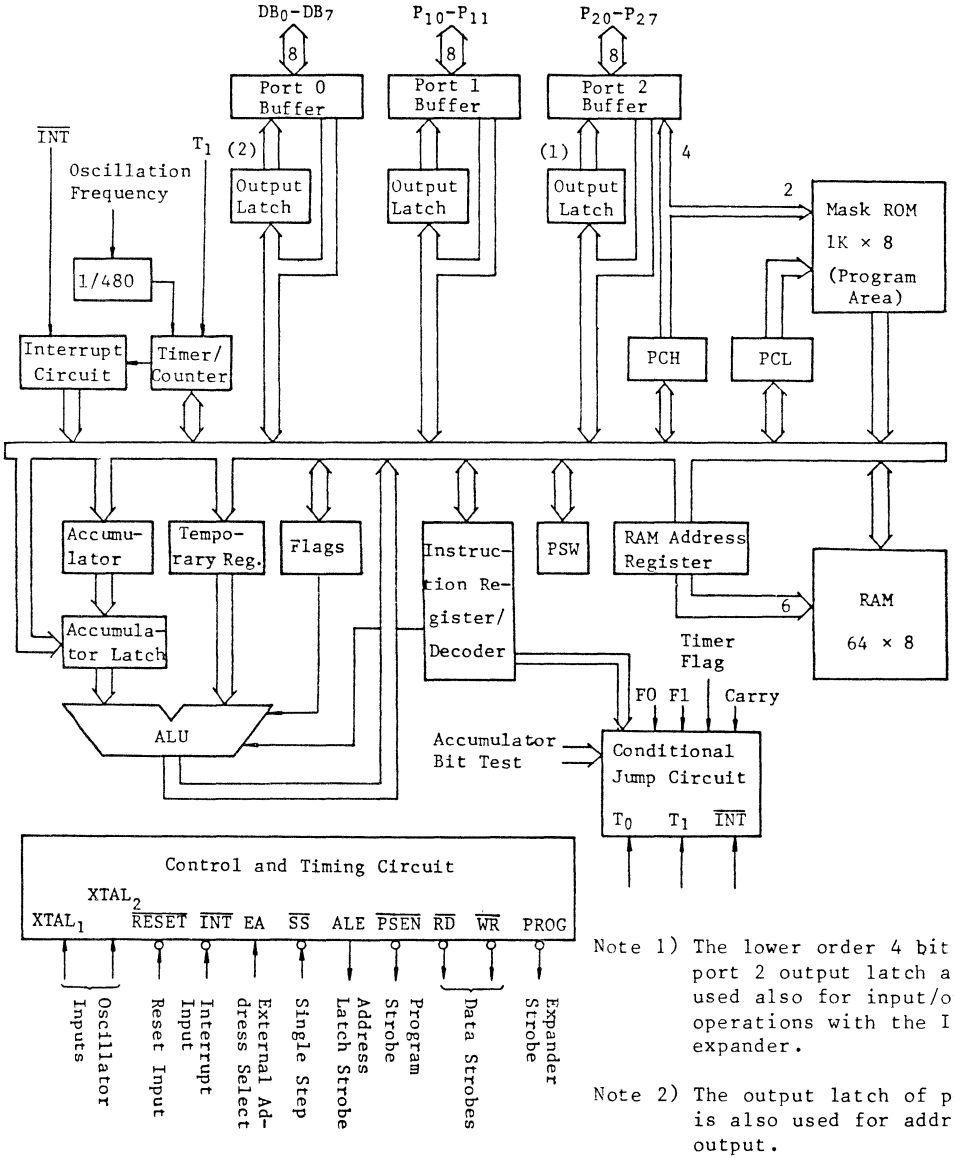
FEATURES

- 2.5 μS Instruction Cycle
- All instruction 1 or 2 cycles
- Over 90 instructions; 70% single byte
- Easy expandable memory and I/O
- 2K x 8 masked ROM
- 128 x 8 RAM
- 27 I/O lines
- Interval Timer/Event Counter
- Single level interrupt
- Single 5V supply
  -40°C to +85°C Operation

PIN CONNECTIONS (Top View)



BLOCK DIAGRAM



Note 1) The lower order 4 bits of port 2 output latch are used also for input/output operations with the I/O expander.

Note 2) The output latch of port 0 is also used for address output.

PIN NAMES AND PIN DESCRIPTION

VSS (Power Supply)
Circuit GND potential

VDD (Power Supply)
+5V during operation Low power standby pin for TMP8049 RAM

VCC (Main Power Supply)
+5V during operation

PROG(Output)
Output strobe for the TMP8243P I/O expander

P10-P17 (Input/Output) Port 1
8-bit quasi -bidirectional port (Internal Pullup=50kΩ).

P20-P27 (Input/Output) Port 2
8-bit quasi-bidirectional port (Internal Pullup=50kΩ).
P20-P23 Contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for the TMP8243P.

DB0-DB7 (Input/Output, 3 State)
True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.

T0 (Input/Output)
Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.

T1 (Input)
Input pin testable using the JT1 and JNT1 instruction. Can be designated the event counter input using the timer/STRT CNT instruction.

$\overline{INT}$ (Input)
External interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active Low)

$\overline{RD}$ (Output)
Output strobe activated during a Bus read. Can be used to enable data onto the Bus from an external device. Used as a Read Strobe to External Data Memory (Active Low).

$\overline{WR}$ (Output)
Output strobe during a Bus write (Active Low) Used as a Write Strobe to External Data Memory.

RESET (Input)
Active Low signal which is used to initialize the Processor. Also used during Power down.

ALE (Output)
Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.

$\overline{\text{PSEN}}$ (Output)
Program Store Enable. This output occurs only during a fetch to external program memory (Active Low).

$\overline{\text{SS}}$ (Input)
Single step input can be used in conjunction with ALE to "single step" processor through each instruction when $\overline{\text{SS}}$ is low the CPU is placed into a wait state after it has completed the instruction being excuted.

EA (Input)
External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug and essential for testing and program verification. (Active High).

XTAL 1 (Input)
One side of crystal input for internal oscillator. Also input for external source.

XTAL 2 (Input)
Other side of crystal input.

FUNCTIONAL DESCRIPTION

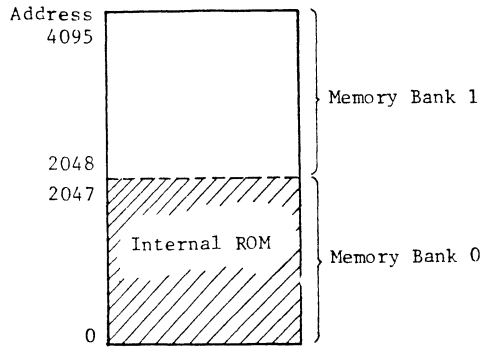
1. System Configuration

The following system functions of the TMP8049 are described in detail.

(1)	Program Memory	(6)	Stack (Stack Pointer)
(2)	Data Memory	(7)	Flag 0, Flag 1
(3)	I/O Port	(8)	Program Status Word (PSW)
(4)	Timer/Counter	(9)	Reset
(5)	Interrupt Control Circuit	(10)	Oscillator Circuit

(1) Program Memory
The maximum memory that can be directly addressed by the TMP8049 is 4096 bytes. The first 2048 bytes from location 0 through 2047 can be internal resident mask ROM. The rest of the 2048 bytes of addressable memory are external to the chip. The TMP8039 has no internal resident memory; all memory must be external.

There are three locations in Program Memory of special importance.



Program Memory Area

. Location 0
Activating the Reset line of the processor causes the first instruction to be fetched from Location 0.

. Location 3
Activating the interrupt line of the processor (if interrupt enabled) causes a jump to subroutine defined by address held in Location 3.

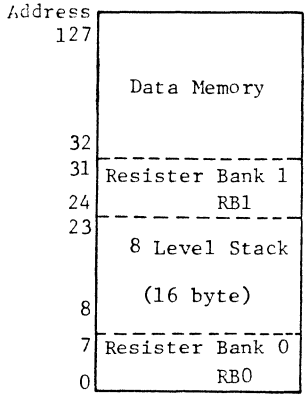
. Location 7
A timer/counter interrupt resulting from a timer/counter overflow (if enabled) causes a jump to a subroutine defined by address held in Location 7.

. Program address 0-2047 and 2048-4095 are called memory banks 0 and 1 respectively switching of memory banks is achieved by changing the most significant bit of the program counter (PC) during execution of an unconditional jump instruction or call instruction executed after using SEL MB0 or SEL MB1.

Reset operation automatically selects Bank 0.

(2) Data Memory

. Resident Data Memory (volatile RAM) is organized as 128 words by 8-bits wide.
. The first 8 locations (0 -7) of the memory array are designated as working registers and are directly addressable by several instructions. By executing a Register Bank switch instruction (SEL RB1) locations 24 - 31 are designated as the working registers in place of 0 - 7.



Internal Data Memory Area

- RAM locations 8 - 23 serve a dual role in that they contain the program counter stack which is a stack 2 bytes wide by 8 levels deep. These locations store returning addresses from subroutines. If the level of subroutine nesting is less than the permitted 8, you free up 2 bytes of RAM for general use for every level of nesting not utilized.

- ALL 128 locations are indirectly addressable through either of two RAM Pointer Registers which reside at R0 and R1 of the Register array.

- The TMP8049 architecture allows extension of the Data Memory to 256 words.

(3)Input/Output Ports

- The TMP8049 has 27 I/O lines which can be used for either input or output. These I/O lines are grouped into 3 ports each having 8 bidirectional lines and 3 "test" inputs which can alter program sequences when tested by conditional jump instructions.

- Ports 1 and 2 are each 8-bits wide and have identical characteristics. Data written to these ports is statically latched and remains unchanged until rewritten. As input ports these lines are non-latching, i.e., inputs must be present until read by an input instruction.

- All lines of Ports 1 and 2 are called quasi-bidirectional because of a special output circuit structure (illustrated in Figure 1). Each line is continously pulled to a +5V level through a high impedance resistive device (50kΩ) which is sufficient to provide the source current for a TTL high level yet can be pulled low by a standard TTL gate thus allowing the same pin to be used for both input and output. In order to speed up the "0" to "1" transition a low impedance device (5kΩ) is switched in momentarily whenever a "1" is written to line. When a "0" is written to line a low impedance device overcomes the pullup and provides TTL current sinking capability.

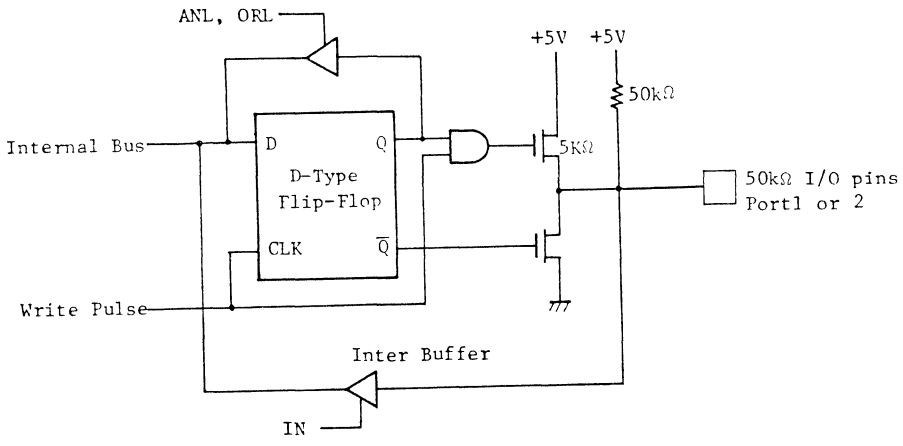


Fig.1 Input/Output Circuit of Port 1, Port 2

- Reset initializes all lines to a high impedance "1" state.

- When external data memory area is not addressed during excution of an internal program, Port 0 (DB0 - DB7) becomes a true bidirectional port (bus) with associated input and output strobes. If bidirectional feature not needed Bus can serve as either a statically latched output port or a non-latched input port. However, I/O lines of this port cannot be intermixed.

- As a static port data is written and latched using the OUTL instruction and inputted using the INS instruction these two commands generate pulses on the corresponding $\overline{RD}$ and $\overline{WR}$ strobe lines.

- As a bidirectional port the MOVX instructions are used to read and write the port which generate the $\overline{RD}$ and $\overline{WR}$ strobes.

- When not being written or read, the Bus lines are in a high impedance state.

(4)Timer/Event Counter

- The 8-bit binary up counter can use either of the following frequency inputs

  (1) Internal clock (1/480 of OSC frequency)
  ..... Timer mode

(2) External input clock form Tl terminal
(minimum cycle time 3 x ALE cycle)
..... Event Counter mode

The counter is presettable and readable with two MOV instructions which transfer the content of the accumulator to the counter and vice versa. The counter content is not affected by a Reset and is initialized solely by the MOVT, A instruction. The counter is stopped by a Reset or STOP TCNT instruction and remains stopped until started by START T instruction or as an event counter by a START CNT. Once started the counter will increment to its maximum count (FF) and overflow to Zero continuing its count until stopped by a STOP TCNT instruction or RESET.

The increment from maximum count to Zero (overflow) results in the setting of an overflow flag and the generation of an interrupt request. When interrupt acknowledged a subroutine call to Location 7 will be initiated. Location 7 should store the starting address of the timer or counter service routine. The state of the overflow flag is testable with the conditional JUMP (JTF). The flag is reset by excuting a JTF or by RESET. Figure 2 illustrates the concept of the timer circuit.

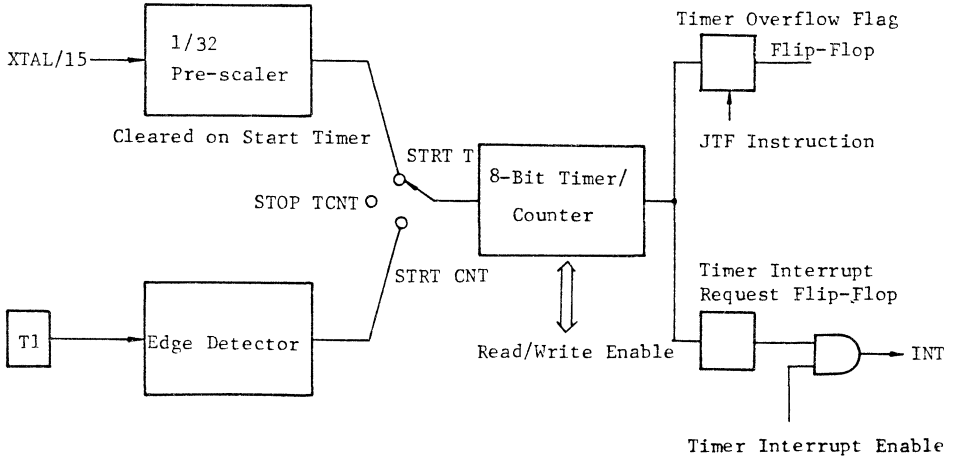


Fig.2 Concept of Timer Circuit

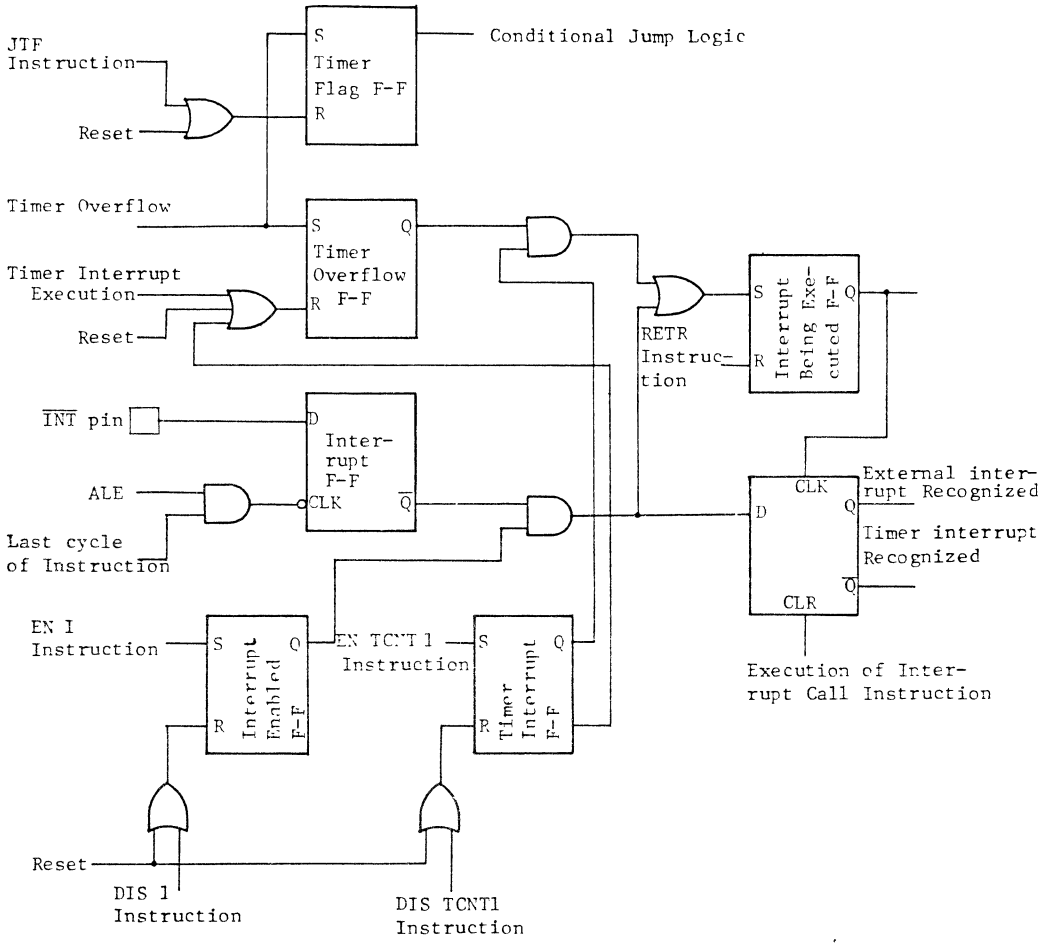


Fig.3 Concept of Interrupt Control Circuit

(5) Interrupt Control Circuit

. There are two distinct types of Interrupts in the TMP8049.

(1) External Interrupt from the $\overline{\text{INT}}$ terminal

(2) Timer Interrupt caused by timer overflow

The interrupt system is single level in that once an interrupt is detected all further interrupt requests are ignored until execution of an RETR (which should occur at the end of an interrupt service routine) reenables the interrupt input logic.

. An interrupt sequence is initiated by applying a low level "0" to the $\overline{INT}$ pin. $\overline{INT}$ is level triggered and active low which allows "Wire Oring" of several interrupt sources. The interrupt level is sampled every machine cycle during ALE and when detected causes a "jump to subroutine" at Location 3. As in any call to subroutine, the Program Counter and Program Status Word are saved in the stack.

. When an overflow occurs in the internal timer/event counter an interrupt request is generated which is reserviced as outlined in previous paragraph except that a jump to Location 7 is used instead of 3. If $\overline{INT}$ and times overflow occur simultaneously then external request $\overline{INT}$ takes precedence.

. If an extra external interrupt is needed in addition to $\overline{INT}$ this can be achieved by enabling the counter interrupt, loading FFH in the counter (one less than the terminal count), and enabling the event counter mode. A "1" to "0" transition on T1 will cause an interrupt vector to Location 7.

. The interrupt service routine pointed to be addresses in Location 3 or 7 must reside in memory between 0 and 2047, i,e., Bank 0.

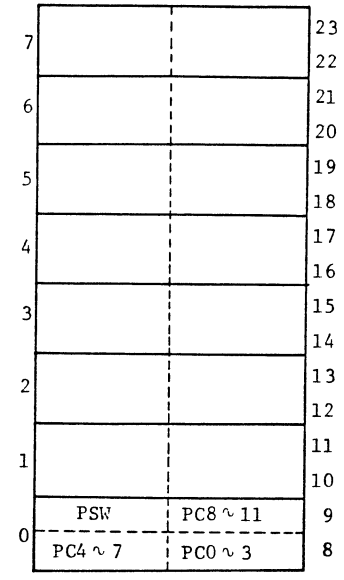
Figure 3 illustrates the concept of the interrupt control circuit.

(6) Stack (stack Pointer)

. An interrupt or Call to subroutine causes the contents of the program counter to be stored in one of the 8 register pairs of the Program Counter Stack. The pair to be used is determined by a 3-bit stack pointer which is part of the Program Status Words (PSW explained in section (8)). Data RAM locations, 8 through 23 are available as stack registers and are used to store the program counter and 4-bits of PSW as shown in the figure.

. The stack pointer when initialized points to RAM location 8 and 9. The first subroutine jump or interrupt results in the program counter contents being transferred to Locations 8 and 9. Then the stack pointer is incremented by one to point to Locations 10 and 11. Eight levels of subroutine are obviously possible.

. At the end of a subroutine signalled by a RET or RETR causes the stack pointer to be decremented by one and the contents of the resulting pair to be transferred to the Program Counter.



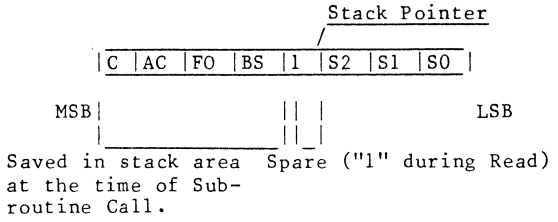
(7) Flag 0, Flag 1, (F0, F1)

. The TMP8049 has two flags F0 and F1 which are used for conditional jump. These flags can be set, reset and tested with the conditional jump instruction JF0.

. F0 is a part of the program status word (PSW) and is saved in the stack area when a subroutine is called.

(8) Program Status Word (PSW)

. An 8-bit status word which can be loaded to and from the accumlator exists called the Program Status Word (PSW). The PSW is read by a MOV A, PSW and written to by a MOV PSW, A. The information available in the PSW is shown in the diagram below.



Bits 0 - 2 : Stack Pointer Bits(S0, S1, S2)
Bit 3 : Not used ("1" level when read.)
Bit 4 : Working Register Bank Switch Bit (BS)

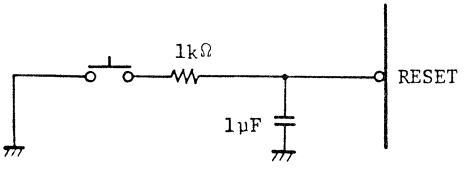
0 = Bank 0
1 = Bank 1

Bit 5 : Flag 0 (F0)
Bit 6 : Auxiliary Carry (AC) carry bit generated by an ADD instruction and used by the decimal adjust instruction DA, A (AC)

Bit 7 : Carry (C) flag which indicates that the previous operation has resulted in the accumulator. (C)

(9) Reset

. The reset input provides a means for initialization of the processor. This Schmitt trigger input has an internal pullup registor which in combination with an external 1μF capacitor provides an internal reset pulse sufficient length to guarantee that all internal logic is initialized.



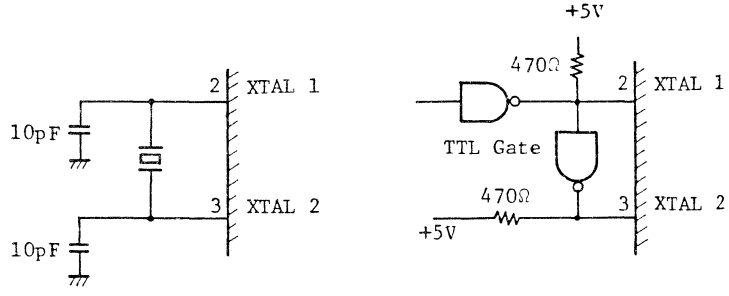
If the pulse is generated externally the reset pin must be held at ground ($\leq$0.5V) for at least 50mS after the power supply is within tolerance.

. Reset performs the following functions within the chip:

(i) Sets PC to Zero.
(ii) Sets Stack Pointer to Zero.
(iii) Selects Register Bank 0.
(iv) Selects Memory Bank 0.
(v) Sets BUS (DB0 - DB 7) to high impedance state. (Except when EA = 5V)
(vi) Sets Ports 1 and 2 to input mode.
(vii) Disables interrupts (timer and external).
(viii) Stops Timer.
(ix) Clears Timer Flag.
(x) Clears F0 and F1.
(xi) Disables clock output from T0.

(10) Oscillator Circuit

. TMP8049 can be operated by the external clock input in addition to crystal oscillator as shown below.



2. Basic Operation and Timing

The following basic operations and timing are explained
(1) Instruction Cycle
(2) External Memory Access Timing
(3) Interface with I/O Expander TMP8243P
(4) Internal Program Verify (Read) Timing
(5) Single Step Operation Timing
(6) Low Power Stand-by Mode

(1) Instruction Cycle

. The instructions of TMP8049 are executed in one or two machine cycles, and one machine cycle contents of five states.

. Fig.4 illustrates its relationship with the clock input to CPU.

. $\phi 2$ clock shown in Fig.4 is derived to outside by ENTO CLK instruction.

. ALE can be also used as the clock to indicate the machine cycle as well as giving the external address latch timing.

(2) External Memory Access Timing

(i) Program Memory Access

. TMP8049 programs are excuted in the following three modes.

(1) Execution of internal program only.
(2) Execution of both external and internal programs.
(3) Execution of external program only.

The external program memory is accessed (instructions are fetched) automatically when the internal ROM address is exceeded in mode (2) and from initial start address 0 in mode (3).

. In the external program memory access operation, the following will occur

. The contents of the 12-bit program counter will be output on BUS(DB0 - DB7) and the lower 4-bits of Port 2.
. Address Latch Enable (ALE) will indicate the time at which address is valid. The trailing edge of ALE is used to latch the address externally.
. Program Store Enable (PSEN) indicates that an external instruction fetch is in progress and serves to enable the external memory device.
. BUS (DB0 - DB7) reverts to Input mode and the processor accepts its 8-bit contents as an Instruction Word.

. Figure 5 illustrates the timing.

(ii) Access of External Data Memory

. In the extended data memory access operation during READ/WRITE cycle the following occurs
. The contents of R0 R1 is output onto BUS (DB0 - DB7).
. ALE indciates address is valid. The trailing edge of ALE is used to latch the address externally.
. A read $\overline{RD}$ or write $\overline{WR}$ pulse on the corresponding output pins indicates the type of data memory access in progress. Output data valid at trailing edge of $\overline{WR}$ and input data must be valid at trailing edge of $\overline{RD}$.
. Data (8-bits) is transferred over BUS.

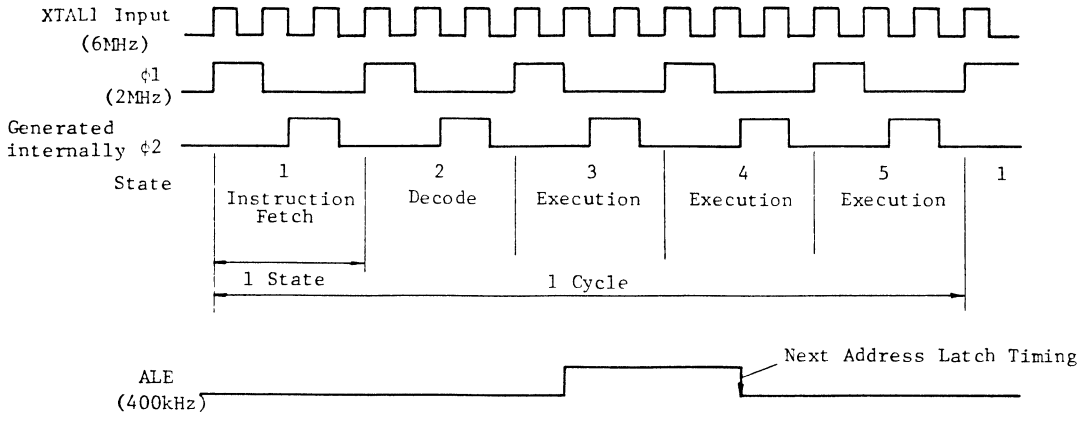


Fig.4 Instruction Cycle Timing

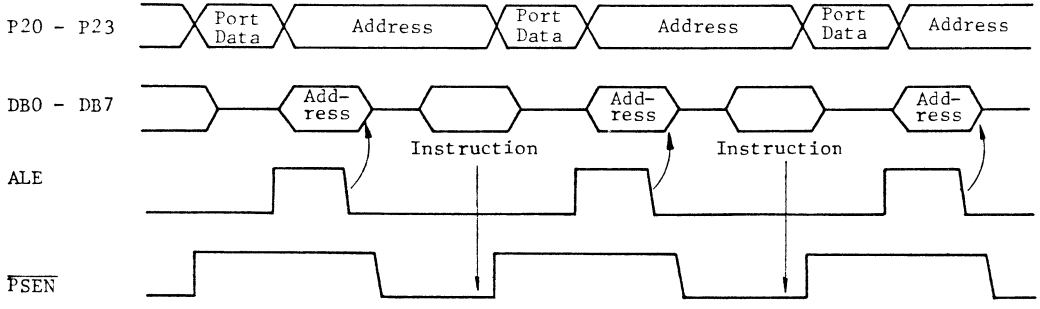
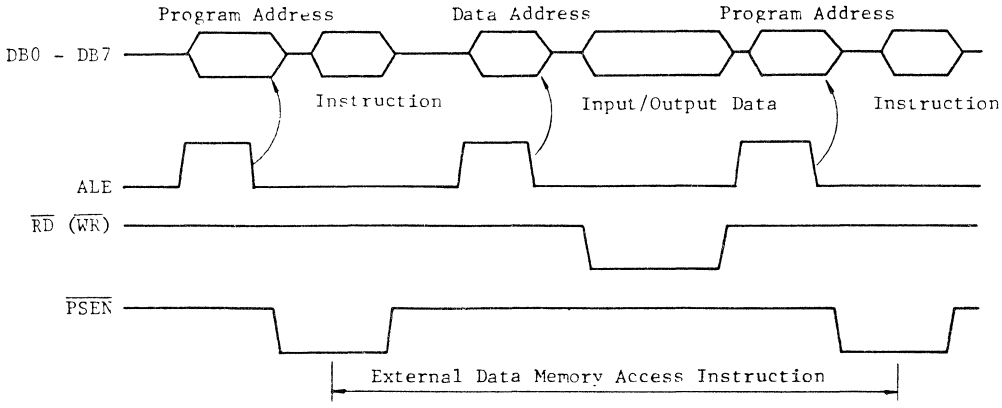


Fig. 5 Timing of External Program Memory Access



Suggest we have diagrams

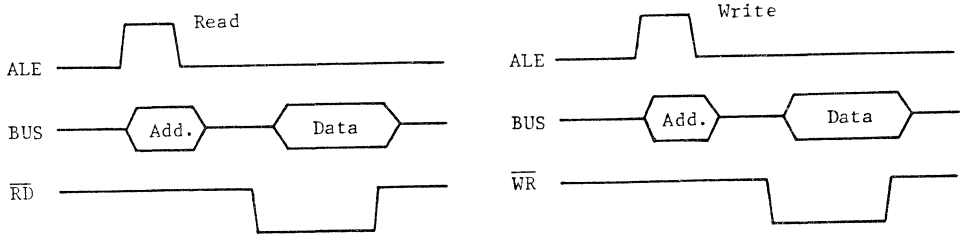


Fig. 6 Timing of Accessing External Data Memory

. Figure 6 illustrates the timing of accessing the external data memory during execution of external program.

(3) Interface with I/O Expander (TMP8243P)

. The TMP8049 I/O can be easily expanded using the TMP8243 I/O Expander. THis device uses only the lower half 4-bits of Port 2 for commuication with the TMP8049. The TMP8243 contains four 4-bit I/O ports which serve as extensions of one chip I/O and are addressed as Ports (4-7). All communication takes place over the lower half of port 2 (P20 - P23) with timing provided by an output pulse on the PROG pin. Each transfer consists of two 4-bit nibbles the first containing the "OP Code" and port address and the second containing the actual 4-bits of data.

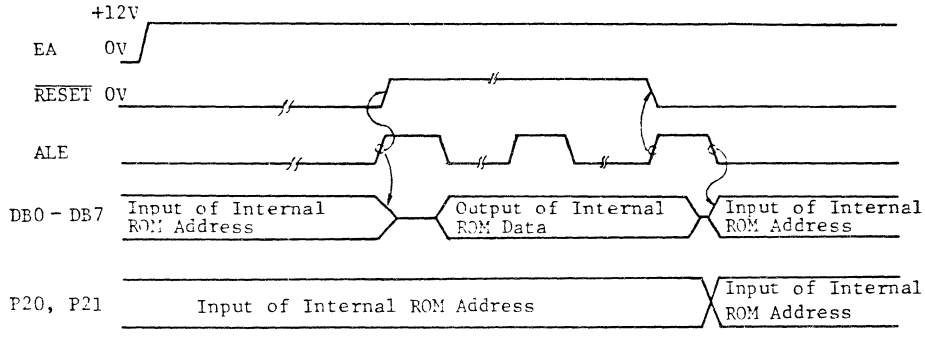


Fig.7 Timing of Reading Internal Program Memory

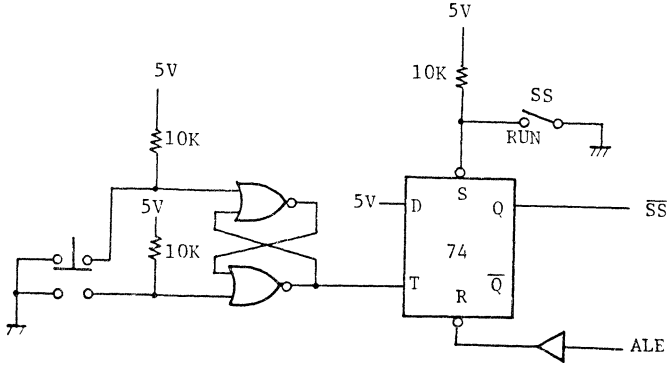


Fig.8 (a) Single Step Circuit

Reading of Internal Program Memory

. The processor is placed in the READ mode by applying +12V to the EA pin and 0V to the $\overline{\text{RESET}}$ pin. The address of the location to be read is then applied to BUS and the low order 2-bits of Port 2. The address is latched by a 0 to 1 transition on $\overline{\text{RESET}}$ and the high level causes the contents of program memory location addressed to appear on the eight lines of BUS.

. Figure 7 illustrates the timing diagram for this operation.

(5) Single Step Operation.

. A single step feature useful for debug can be implemented by utilizing a circuit shown in Figure 8 (a) combined with the $\overline{\text{SS}}$ pin and ALE pin.

. A D-type flip flop with set and reset is used to generate $\overline{\text{SS}}$. In the run mode $\overline{\text{SS}}$ is held high by keeping the flip flop set. To enter single step, set is removed allowing ALE to bring $\overline{\text{SS}}$ low via reset input. The next instruction is started by clocking a "1" into the FF which will not appear on $\overline{\text{SS}}$ unless ALE is high removing reset. In response to $\overline{\text{SS}}$ going high the processor begins an instruction fetch which brings ALE low resetting FF and causing the processor to again enter the stopped state.

. The timing diagram in this case is as shown in Figure 8 (b). (EA = 5V).

(6) Lower Power Stand-by Mode.

. The Lower TMP8049 has been organized to allow power to be removed from all but the volatile, 128 x 8 data RAM array. In power down mode the contents of data RAM can be maintained while drawing typically 10 - 15% of normal operating power requirements.

. VCC serves as the 5V supply for the bulk of the TMP8049 while the VDD supplies only the RAM array. In standby mode VCC is reduced to 0V but VDD is kept at 5V. Applying a low level to reset inhibits any access to the RAM by the processor and guarantees that RAM cannot be inadvertently altered as power is removed from VCC.

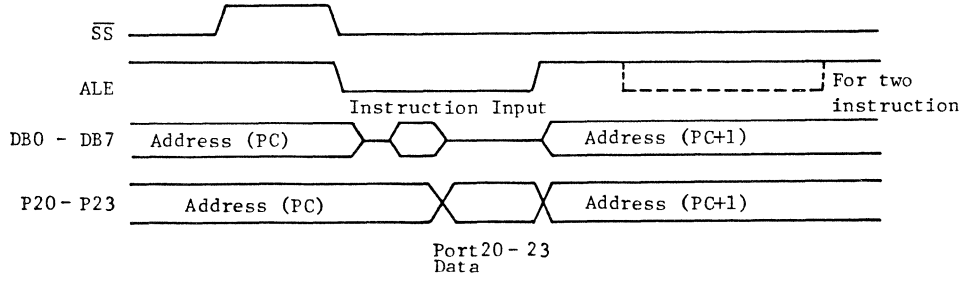


Fig.8(b) Single Step Operation Timing

INSTRUCTION

ACCUMULATOR INSTRUCTION

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
ADD A,Rr	0	1	1	0	1	r	r	r	(A)<-(A)+(Rr) r = 0 - 7	1	1	o	o
ADD A,@Rr	0	1	1	0	0	0	0	r	(A)<-(A)+((Rr)) r = 0, 1	1	1	o	o
ADD A,#Data	0	0	0	0	0	0	1	1	(A)<-(A)+Data	2	2	o	o
	d7	d6	d5	d4	d3	d2	d1	d0					
ADDC A,Rr	0	1	1	1	1	r	r	r	(A)<-(A)+(Rr)+(C) r = 0 - 7	1	1	o	o
ADDC A,@Rr	0	1	1	1	0	0	0	r	(A)<-(A)+((Rr))+(C) r = 0, 1	1	1	o	o
ADDC A,#Data	0	0	0	1	0	0	1	1	(A)<-(A)+Data+(C)	2	2	o	o
	d7	d6	d5	d4	d3	d2	d1	d0					
ANL A,Rr	0	1	0	1	1	r	r	r	(A)<-(A) and (Rr) r = 0 - 7	1	1	-	-
ANL A,@Rr	0	1	0	1	0	0	0	r	(A)<-(A)and ((Rr)) r = 0, 1	1	1	-	-
ANL A,#Data	0	1	0	1	0	0	1	1	(A)<-(A) and Data	2	2	-	-
	d7	d6	d5	d4	d3	d2	d1	d0					
ORL A,Rr	0	1	0	0	1	r	r	r	(A)<-(A) or (Rr) r = 0 - 7	1	1	-	-
ORL A,@Rr	0	1	0	0	0	0	0	r	(A)<-(A) or ((Rr)) r = 0, 1	1	1	-	-
ORL A,#Data	0	1	0	0	0	0	1	1	(A)<-(A) or Data	2	2	-	-
	d7	d6	d5	d4	d3	d2	d1	d0					
XRL A, Rr	1	1	0	1	1	r	r	r	(A)<-(A) EOR (Rr) r = 0 - 7	1	1	-	-
XRL A,@Rr	1	1	0	1	0	0	0	r	(A)<-(A) EOR((Rr)) r = 0, 1	1	1	-	-
XRL A,#Data	1	1	0	1	0	0	1	1	(A)<-(A) EOR Data	2	2	-	-
	d7	d6	d5	d4	d3	d2	d1	d0					
INC A	0	0	0	1	0	1	1	1	(A)<-(A)+1	1	1	-	-
DEC A	0	0	0	0	0	1	1	1	(A)<-(A)-1	1	1	-	-
CLR A	0	0	1	0	0	1	1	1	(A)<-0	1	1	-	-
CPL A	0	0	1	1	0	1	1	1	(A)<-NOT (A)	1	1	-	-
DA A	0	1	0	1	0	1	1	1	Decimal Adjust Accumulator	1	1	o	-
SWAP A	0	1	0	0	0	1	1	1	(A4-7)->(A0-3) <-	1	1	-	-

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
RL A	1	1	1	0	0	1	1	1	(An+1)<-(An) n = 0 - 6 (A0)<-(A7)	1	1	-	-
RLC A	1	1	1	1	0	1	1	1	(An+1)<-(An) n = 0 - 6 (C)<-(A7) (A0)<-(C)	1	1	-	-
RR A	0	1	1	1	0	1	1	1	(An)<-(An+1) n = 0 - 6 (A7)<-(A0)	1	1	-	-
RRC A	0	1	1	0	0	1	1	1	(An)<-(An+1) n = 0 - 6 (C)<-(A0) (A7)<-(C)	1	1	-	-

Input/Output Instruction

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
IN A,Pp	0	0	0	0	1	0	P	P	(A)<-(Pp) P = 1, 2	1	2	-	-
OUTL Pp,A	0	0	1	1	1	0	P	P	(Pp)<-(A) P = 1, 2	1	2	-	-
ANL Pp,#Data	1	0	0	1	1	0	P	P	(Pp)<-(Pp)and Data P = 1, 2	2	2	-	-
	d7	d6	d5	d4	d3	d2	d1	d0					
ORL Pp,#Data	1	0	0	0	1	0	P	P	(Pp)<-(Pp)or Data P = 1, 2	2	2	-	-
	d7	d6	d5	d4	d3	d2	d1	d0					
INS A,BUS	0	0	0	0	1	0	0	0	(A)<-(BUS)	1	2	-	-
OUTL BUS,A	0	0	0	0	0	0	1	0	(BUS)<-(A)	1	2	-	-
ANL BUS,#Data	1	0	0	1	1	0	0	0	(BUS)<-(BUS) and	2	2	-	-
	d7	d6	d5	d4	d3	d2	d1	d0	Data				
ORL BUS,#Data	1	0	0	0	1	0	0	0	(BUS)<-(BUS) or	2	2	-	-
	d7	d6	d5	d4	d3	d2	d1	d0	Data				
MOVD A,Pp	0	0	0	0	1	1	P	P	(A0-3)<-(Pp) (A4-7)<-0 P = 4 - 7	1	2	-	-
MOVD Pp,A	0	0	1	1	1	1	P	P	(Pp)<-(A0-3) P = 4 - 7	1	2	-	-
ANLD Pp,A	1	0	0	1	1	1	P	P	(Pp)<-(Pp)and (A0-3) P = 4 - 7	1	2	-	-
ORLD Pp,A	1	0	0	0	1	1	P	P	(Pp)<-(Pp)or(A0-3) P = 4 - 7	1	2	-	-

Register Instruction

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
INC Rr	0	0	0	1	1	r	r	r	(Rr)<--(Rr)+1	1	1	-	-
									r = 0 - 7				
INC @Rr	0	0	0	1	0	0	0	r	((Rr))<-((Rr))+1	1	1	-	-
									r = 0, 1				
DEC Rr	1	1	0	0	1	r	r	r	(Rr)<--(Rr)-1	1	1	-	-
									r = 0 - 7				

Branch Instruction

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
JMP Address	a10	a9	a8	0	0	1	0	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	(PC8-10)<--(a8-10)				
									(PC11)<--DBF				
JMPP @A	1	0	1	1	0	0	1	1	(PC0-7)<--((A))	1	2	-	-
DJNZ Rr,	1	1	1	0	1	r	r	r	(Rr)<--(Rr)-1	2	2	-	-
Address	a7	a6	a5	a4	a3	a2	a1	a0	if Rr not 0				
									(PC0-7)<--(a0-7)				
JC Address	1	1	1	1	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
									if C = 1				
	a7	a6	a5	a4	a3	a2	a1	a0	(PC) = (PC)+2				
									if C = 0				
JNC Address	1	1	1	0	0	1	1	0	(PC0-7)<-(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if C = 0				
									(PC)<--(PC)+2				
									if C = 1				
JZ Address	1	1	0	0	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if (A) = 0				
									(PC)<--(PC)+2				
									if (A) .NEQ.0				
JNZ Address	1	0	0	1	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if (A) .NEQ.0				
									(PC)<--(PC)+2				
									if (A) = 0				
JTO Address	0	0	1	1	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if TO = 1				
									(PC)<--(PC)+2				
									if TO = 0				
JNTO Address	0	0	1	0	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if TO = 0				
									(PC)<--(PC)+2				
									if TO = 1				
JT1 Address	0	1	0	1	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if T1 = 1				
									(PC)<--(PC)+2				
									if T1 = 0				
JNT1 Address	0	1	0	0	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if T1 = 0				
									(PC)<--(PC)+2				
									if T1 = 1				

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
JF0 Address	1	0	1	1	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if F0 = 1				
									(PC)<--(PC)+2				
									if F0 = 0				
JF1 Address	0	1	1	1	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if F1 = 1				
									(PC)<--(PC)+2				
									if F1 = 0				
JTF Address	0	0	0	1	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if TF = 1				
									(PC)<--(PC)+2				
									if TF = 0				
JNI Address	1	0	0	0	0	1	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if INT = 0				
									(PC)<--(PC)+2				
									if INT = 1				
JBb Address	b2	b1	b0	1	0	0	1	0	(PC0-7)<--(a0-7)	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	if Bb = 1				
									(PC)<-(PC)+2				
									if Bb = 0				
									(b = 0 - 7)				
CALL Address	a10	a9	a8	1	0	1	0	0	((SP))<--	2	2	-	-
	a7	a6	a5	a4	a3	a2	a1	a0	(PC),(PSW4-7)				
									(SP)<--(SP)+1				
									(PC8-10)<--(a8-10)				
									(PC0-7)<--(a0-7)				
									(PC11)<--DBF				
RET	1	0	0	0	0	0	1	1	(SP)<--(SP)-1	1	2		
									(PC)<--((SP))				
RETR	1	0	0	1	0	0	1	1	(SP)<--(SP)-1	1	2		
									(PC)<--((SP))				
									(PSW4-7)<--((SP))				

Flag Manipulation Instruction

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
CLR C	1	0	0	1	0	1	1	1	(C)<-- 0	1	1	0	-
CPL C	1	0	1	0	0	1	1	1	(C)<--NOT(C)	1	1	0	-
CLR F0	1	0	0	0	0	1	0	1	(F0)<-- 0	1	1	-	-
CPL F0	1	0	0	1	0	1	0	1	(F0)<--NOT(F0)	1	1	-	-
CLR F1	1	0	1	0	0	1	0	1	(F1)<-- 0	1	1	-	-
CPL F1	1	0	1	1	0	1	0	1	(F1)<--NOT(F1)	1	1	-	-

Data Transfer Instruction

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
MOV A, Rr	1	1	1	1	1	r	r	r	(A)<-- (Rr) r = 0 - 7	1	1	-	-
MOV A, @Rr	1	1	1	1	0	0	0	r	(A)<-- ((Rr)) r = 0, 1	1	1	-	-
MOV A, #Data	0 d7	0 d6	1 d5	0 d4	0 d3	0 d2	1 d1	1 d0	(A)<--Data	2	2	-	-
MOV Rr, A	1	0	1	0	1	r	r	r	(Rr)<--(A) r = 0 - 7	1	1	-	-
MOV@Rr,A	1	0	1	0	0	0	0	r	((Rr))<-(A) r = 0, 1	1	1	-	-
MOV Rr,#Data	1 d7	0 d6	1 d5	1 d4	1 d3	r d2	r d1	r d0	(Rr)<--Data r = 0 - 7	2	2	-	-
MOV@Rr,#Data	1 a7	0 a6	1 a5	1 a4	0 a3	0 a2	0 a1	r a0	((Rr))<--Data r = 0, 1	2	2	-	-
MOV A,PSW	1	1	0	0	0	1	1	1	(A)<-- (PSW)	1	1	-	-
MOV PSW, A	1	1	0	1	0	1	1	1	(PSW)<--(A)	1	1	-	-
XCH A, Rr	0	0	1	0	1	r	r	r	(A)-->(Rr) <-- r = 0 - 7	1	1	-	-
XCH A,@Rr	0	0	1	0	0	0	0	r	(A)-->((Rr)) <-- r = 0, 1	1	1	-	-
XCHD A,@Rr	0	0	1	1	0	0	0	r	(A0-3)-->((Rr0-3)) <-- r = 0, 1	1	1	-	-
MOVX A,@Rr	1	0	0	0	0	0	0	r	(A)<--((Rr)) r = 0, 1	1	2	-	-
MOVX @Rr,A	1	0	0	1	0	0	0	r	((Rr))<--(A) r = 0, 1	1	2	-	-
MOVP A, @A	1	0	1	0	0	0	1	1	(PC0-7)<--(A) (A)<--((PC))	1	2	-	-
MOVP3 A,@A	1	1	1	0	0	0	1	1	(PC0-7)<--(A) (PC8-11)<--0011 (A)<--((PC))	1	2	-	-

Timer/Counter Instruction

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
MOV A,T	0	1	0	0	0	0	1	0	(A)<--(T)	1	1	-	-
MOV T,A	0	1	1	0	0	0	1	0	(T)<--(A)	1	1	-	-
STRT T	0	1	0	1	0	1	0	1	Counting is started in the timer mode	1	1	-	-
STRT CNT	0	1	0	0	0	1	0	1	Counting is started in the event counter mode	1	1	-	-
STOP TCNT	0	1	1	0	0	1	0	1	Stop both time accumulation and event counting	1	1	-	-
EN TCNTI	0	0	1	0	0	1	0	1	Timer interrupt is enabled	1	1	-	-
DIS TCNTI	0	0	1	1	0	1	0	1	Timer interrupt is disabled	1	1	-	-

Control Instruction

Mnemonic	Instruction Code								Operation	Bytes	Cycles	Flag	
	D7	D6	D5	D4	D3	D2	D1	D0				C	AC
EN I	0	0	0	0	0	1	0	1	External interrupt is enabled	1	1	-	-
DIS I	0	0	0	1	0	1	0	1	External interrupt is disabled	1	1	-	-
SEL RB0	1	1	0	0	0	1	0	1	(BS)<-- 0	1	1	-	-
SEL RB1	1	1	0	1	0	1	0	1	(BS)<-- 1	1	1	-	-
SEL MB0	1	1	1	0	0	1	0	1	(DBF)<-- 0	1	1	-	-
SEL MB1	1	1	1	1	0	1	0	1	(DBF)<-- 1	1	1	-	-
ENTO CLK	0	1	1	1	0	1	0	1	T0 is enabled to act as the clock output	1	1	-	-
NOP	0	0	0	0	0	0	0	0	No operation	1	1	-	-

TMP8049PI/8039PI: INDUSTRIAL SPECIFICATION

ABSOLUTE MAXIMUM RATTINGS

SYMBOL	ITEM	RATTING
VDD	VDD Supply Voltage (with respect to GND (VSS))	-0.5V to + 7V
VCC	VCC Supply Voltage (with respect to GND (VSS))	-0.5V to + 7V
VINA	Input Voltage (Except EA)	-0.5V to + 7V
VINB	Input Voltage (Only EA)	-0.5V to + 13V
PD	Power Dissipation (Ta = 70°C)	1.5W
TSOLDER	Soldering Temperature (Soldering Time 10 sec)	260°C
TSTG	Storage Temperature	-55°C to 150°C
TOPR	Operating Temperature	-40°C to 85°C

DC CHARACTERISTICS

TA=-40°C to 85°C, VCC=VDD=+5V±10%, VSS=0V, Unless Otherwise Noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage (Except XTAL1,XTAL2,$\overline{\text{RESET}}$)		-0.5	-	0.7	V
VIL1	Input Low Voltage (XTAL1,XTAL2,$\overline{\text{RESET}}$)		-0.5	-	0.6	V
VIH	Input High Voltage (Except XTAL1,XTAL2,$\overline{\text{RESET}}$)		2.2	-	VCC	V
VIH1	Input High Voltage (XTAL1,XTAL2,$\overline{\text{RESET}}$)		3.8	-	VCC	V
VOL	Output Low Voltage (BUS)	IOL = 1.6 mA	-	-	0.45	V
VOL1	Output Low Voltage ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, ALE)	IOL = 1.6 mA	-	-	0.45	V
VOL2	Output Low Voltage (PROG)	IOL = 0.8 mA	-	-	0.45	V
VOL3	Output Low Voltage (For other output pins)	IOL = 1.2 mA	-	-	0.45	V
VOH	Output High Voltage (BUS)	IOH =-280μA	2.4	-	-	V
VOH1	Output High Voltage ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, ALE)	IOH =-80μA	2.4	-	-	V
VOH2	Output High Voltage (For other output pins)	IOH =-30μA	2.4	-	-	V
ILI	Input Leak Current (T1, $\overline{\text{INT}}$)	VSS $\leqq$ VIN $\leqq$ VCC	-	-	±10	μA
ILI1	Input Leak Current (P10-17, P20-P27, EA, $\overline{\text{SS}}$)	VSS+0.45$\leqq$VIN$\leqq$VCC	-	-	-700	μA
ILO	Output Leak Current (BUS, T0) (High impedance condition)	VSS+0.45$\leqq$VIN$\leqq$VCC	-	-	±10	μA
IDD	VDD Supply Current		-	-	50	mA
IDD+ICC	Total Supply Current		-	-	170	mA

AC CHARACTERISTICS

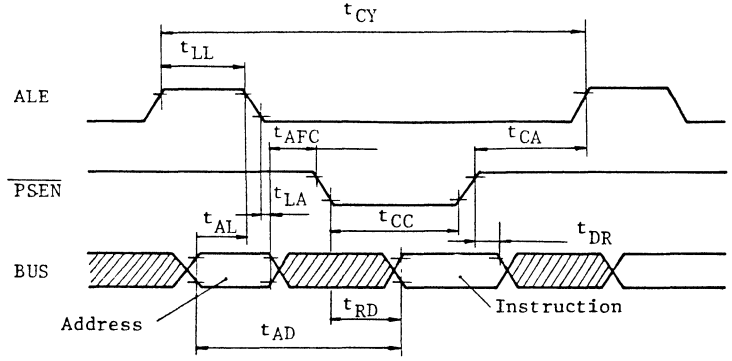
|TA=-40°C to 85°C|, VCC=VDD=+5V±10%, VSS=0V, Unless Otherwise Noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
tLL	ALE Pulse Width		200	-	-	ns
tAL	Address Setup Time (ALE)		120	-	-	ns
tLA	Address Hold time (ALE)		80	-	-	ns
tCC	Control Pulse Width($\overline{PSEN}$,$\overline{RD}$,$\overline{WR}$)		400	-	-	ns
tDW	Data Setup Time ($\overline{WR}$)		420	-	-	ns
tWD	Data Hold Time ($\overline{WR}$)		80	-	-	ns
tCY	Cycle Time		2.5	-	15.0	μs
tDR	Data Hold Time ($\overline{PSEN}$,$\overline{RD}$)	CL = 20 pF	0	-	200	ns
tRD	Data Input Read Time ($\overline{PSEN}$, $\overline{RD}$)		-	-	400	ns
tAW	Address Setup Time ($\overline{WR}$)		230	-	-	ns
tAD	Address Setup Time (Data Input)		-	-	600	ns
tAFC	Address Float Time ($\overline{RD}$, $\overline{PSEN}$)		-40	-	-	ns
tCA	Internal between Control Pulse and ALE		10	-	-	ns
tCP	Port Control Setup Time (PROG)		115	-	-	ns
tPC	Port Control Hold Time (PROG)		65	-	-	ns
tPR	Port 2 Input Data Set Time (PROG)		-	-	860	ns
tDP	Output Data Setup Time (PROG)		230	-	-	ns
tPD	Output Data Hold Time (PROG)		25	-	-	ns
tPF	Port 2 Input Data Hold Time (PROG)		0	-	160	ns
tPP	PROG Pulse Width		920	-	-	ns
tPL	Port 2 I/O Data Setup Time		300	-	-	ns
tLP	Port 2 I/O Data Hold Time		120	-	-	ns

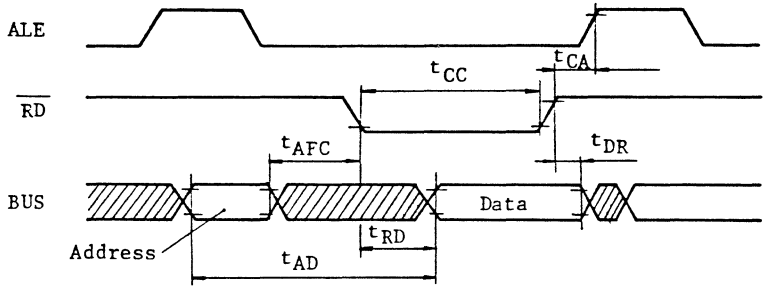
Note : tCY=2.5μs, Control Output: CL=80pF, BUS Output: CL=150pF, PORT20-23: CL=80pF.

TIMING WAVEFORM

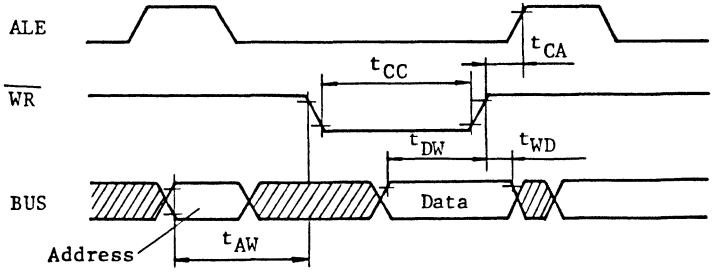
A. Instruction Fetch from External Program Memory



B. Read from External Data Memory

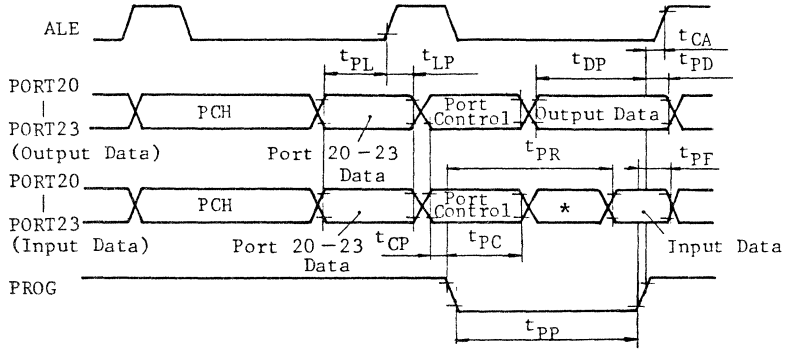


C. Write into External Data Memory



D. Timing of Port 2 during Expander Instruction Execution

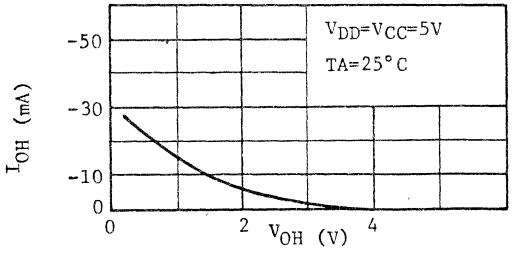
TYPICAL CHARACTERISTICS



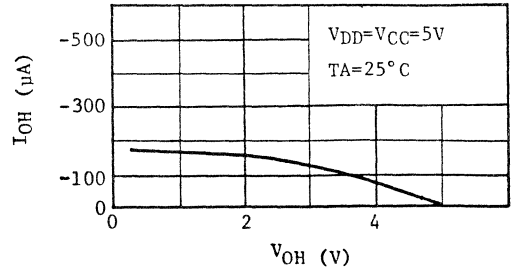
* Input Enabled State

TYPICAL CHARACTERISTICS

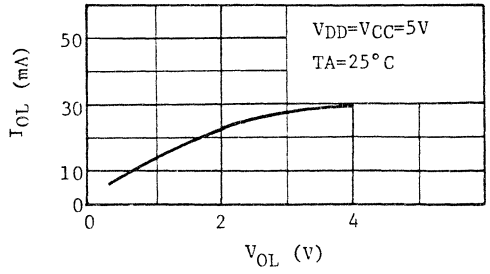
1) BUS: I_{OH} - V_{OH}



2) P1, P2: I_{OH} - V_{OH}



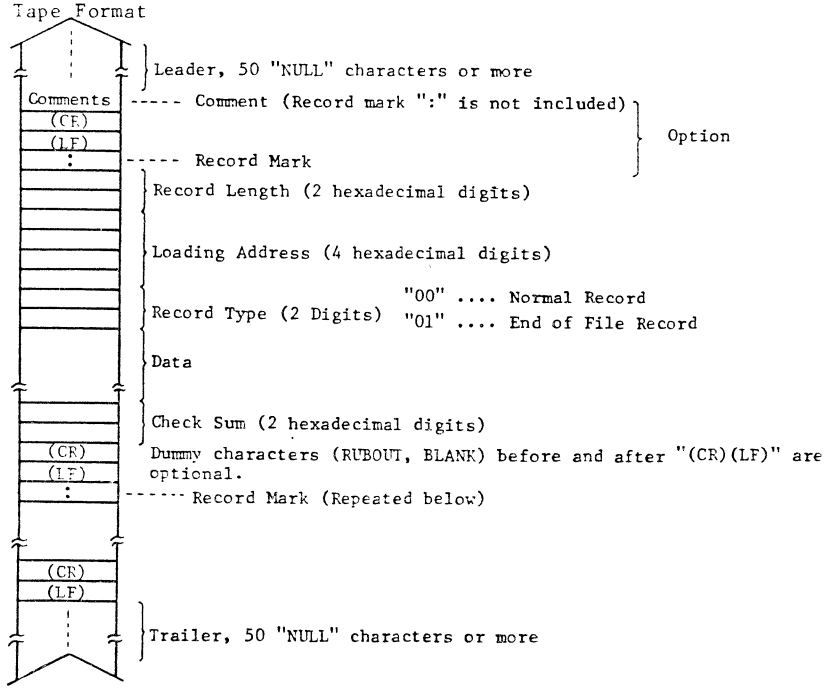
3) BUS, P1, P2: I_{OL} - V_{OL}



PROGRAM TAPE FORMAT

TMP8049 programs are delivered in the form of paper tape with the following format and it is required to attach the tape list. The format of paper tape is same as the Intel type object tape (hexadecimal tape output by Intel MDS system, PROMPT 48 Development Tool, etc.)

(1) Tape Format

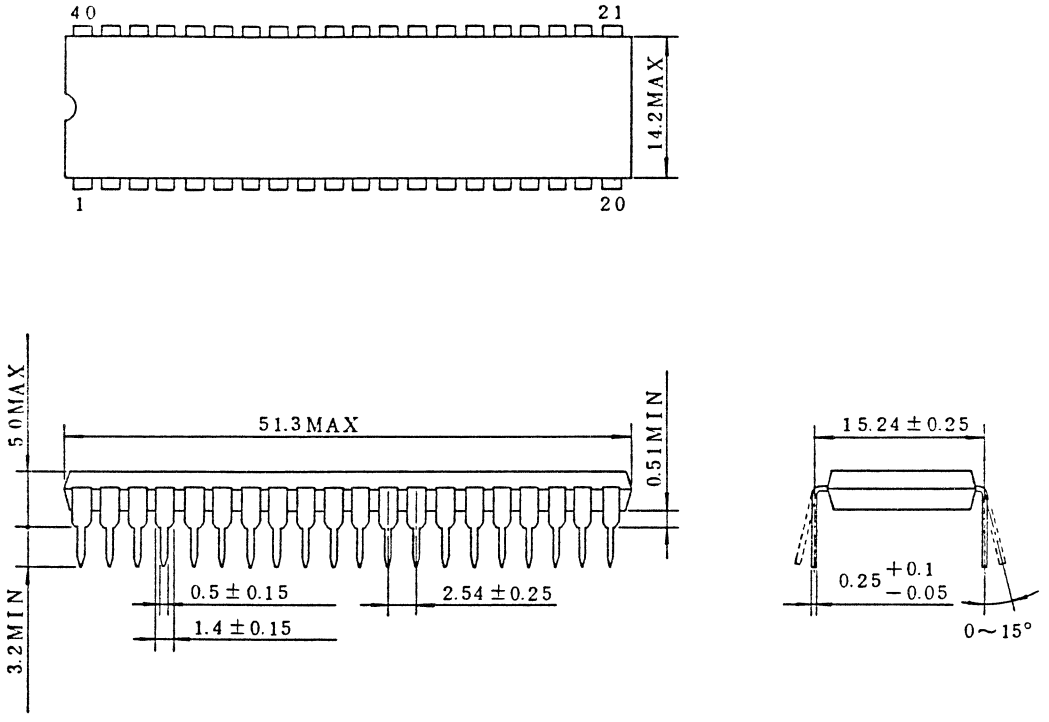


(2) Example of Tape List

```
TOSHIBA MICRO COMPUTER TLCS-48
:100000000665C7D79CF50F3F951FED55A8FF16E570
:1000100088884DDE67D31F5D8ABA6DF292F113F5C1
:100020004FF1FB5DFFDAA96A99CF7DF94A346B7C09
:10003000197352F729F12F79AA9C057C5B851EED77
                    :
                    :
                    :
                    :
:1003C0005DFDB5E556A67277F61A51C631CF9F0E80
:1003D000BD2F6F20E8BB1977E3FB5AD1F41FDAA7E2
:1003E000B53D42E0EC32546025B7308CDD52063D1D
:1003F000B4BE9E9E345B6138060B20VC372BF60BD6
:00000001FF
```

OUTLINE DRAWING

Unit in mm



Note: 1. This dimension is measured at the center of bending point of leads.
2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoritical positions with respect to No.1 and No.40 leads.

INPUT/OUTPUT EXPANDER

GENERAL DESCRIPTION

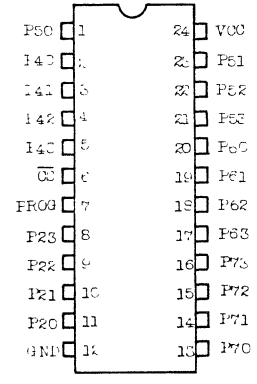
The TMP8243P is an input/output expander designed specifically to provide a low cost means of I/O expansion for the TLCS-84 family.

The I/O ports of the TMP8243P serve as a direct extension of the resident I/O facilities of the TLCS-84 microcomputers and are accessed by their own MOVD, ANLD, and ORLD instructions.

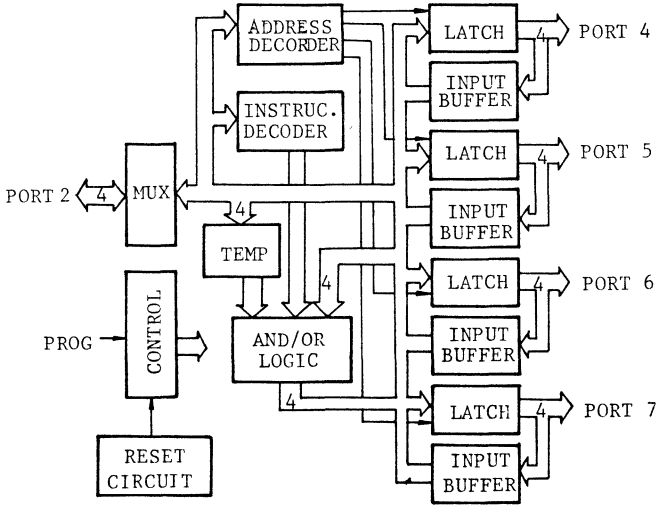
FEATURES

- o Low cost
- o Simple interface to TLCS-84 microcomputers
- o Four 4-bit I/O ports
- o AND and OR directly to ports
- o Single 5V supply
- o High output drive
- o Direct extension of resident TMP8048P/TMP8049P I/O ports.
- o Compatible with intel's 8243
- o -40°C to +85°C Operation (TMP8243PI: Industrial Specification)

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES AND PIN DESCRIPTION

PROG (Input)
Clock Input. A high to low transistion on PROG signifies that address and control are available on P20-23, and a low to high transition signifies that data is available on P20-23.

$\overline{CS}$ (Input)
Chip Select Input. A high on CS inhibits any change of output or internal status.

P20-23 (Input/Output, 3-state)
Four (4) bit bi-directional port contains the address and control bits on a high to low transition of PROG. During a low to high transition contains the data for a selected output port if a write oepration, or the data from a selected port before the low to high transition if a read operation.

P40-43, P50-53, P60-63, P70-73 (Input/Output, 3-state)
Four (4) bit bi-directional I/O ports. May be programmed to be input (during read), low impedance latched output (after write) or a 3-state (after read). Data on pins P20-23 may be directly written, ANDed or ORed with previous data.

V_{CC} (Power)
+5 volt supply

GND (Power)
0 volt supply

FUNCTIONAL DESCRIPTION

General Operation
The TMP8243P contains four 4-bit I/O ports which serve as an extension of the on-chip I/O and are addressed as ports 4-7. The following operations may be performed on these ports.

- o Transfer accumulator to port
- o Transfer port to accumulator
- o AND accumulator to port
- o OR accumulator to port

All communication between the TMP8048P and the TMP8243P occurs over Port 2 (P20-23) with timing provided by an output pulse on the PROG pin of the processor. Each transfer consists of two 4-bit nibbles.

A high to low transition of the PROG line indicates that address is present while a low to high transition indicates the presence of data. Additional TMP8243P'S may be added to the 4-bit bus and chip selected using additional output lines from the TMP8048P/8035P.

Power On Initialization

Initial application of power to the device forces input/output ports 4, 5, 6, and 7 to the tri-state and port 2 to the input mode. The PROG pin may be either high or low when power is applied. The first high to low transition of PROG causes device to exit power on mode. The power on sequence is initiated if V_{CC} drops below 1V.

P21	P20	Address Code	P23	P22	Instruction Code
0	0	Port 4	0	0	Read
0	1	Port 5	0	1	Write
1	0	Port 6	1	0	ORLD
1	1	Port 7	1	1	ANLD

Write Modes

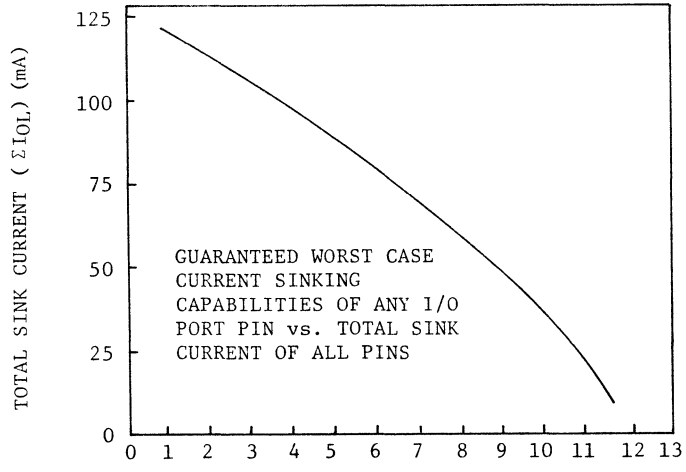
The device has three write modes. MOVD Pi, A directly writes new data into the selected port and old data is lost. ORLD Pi, A takes new data, OR's it with the old data and then writes it to the port. ANLD Pi, A takes new data AND's it with the old data and then writes it to the port. Operation code and port address are latched from the input port 2 on the high to low transition of the PROG pin. On the low to high transition of PROG data on port 2 is transferred to the logic block of the specified output port.

After the logic manipulation is performed, the data is latched and outputed. The old data remains latched until new valid outputs are entered.

Read Mode

The device has one read mode. The operation code and port address are latched from the input port 2 on the high to low transition of the PROG pin. As soon as the read operation and port address are decoded, the appropriate outputs are 3-stated, and the input buffers switched on. The read operation is terminated by a low to high transition of the PROG pin. The port (4, 5, 6 or 7) that was selected is switched to the 3-stated mode while port 2 is returned to the input mode.

Normally, a port will be in an output (write mode) or input (read mode). If modes are changed during operation, the first read following a write should be ignored; all following reads are valid. This is to allow the external driver on the port to settle after the first read instruction removes the low impedance drive from the TMP8243P output. A read of any port will leave that port in a high impedance state.



Sink Capability

The TMP8243P can sink 5 mA@.45V on each of its 16 I/O lines simultaneously. If, however, all lines are not sinking simultaneously or all lines are not fully loaded, the drive capability of any individual line increases as is shown by the accompanying curve.

For example, if only 5 of the 16 lines are to sink current at one time, the curve shows that each of those 5 lines is capable of sinking 9 mA@.45V (if any lines are to sink 9 mA the total I_{OL} must not exceed 45 mA or five 9 mA loads).

Example: How many pins can drive 5 TTL loads (1.6 mA) assuming remaining pins are unloaded?

I_{OL} = 5 x 1.6 mA = 8 mA
εI_{OL} = 60 mA from curve
#pins = 60 mA ÷ 8 mA/pin = 7.5 = 7

In this case, 7 lines can sink 8 mA for a total of 56 mA. This leaves 4 mA sink current capability which can be divided in any way among the remaining 9 I/O lines of the TMP8243P.

Example: This examples shows now the use of the 20 mA sink capability of port 7 affects the sinking capability of the other I/O lines.

An TMP8243P will drive the following loads simultaneously.

2 loads - 20 mA@1V (port 7 only)

8 loads - 4 mA@.45V

6 loads - 3.2 mA@.45V

Is this within the specified limits?
εI_{OL} = (2 x 20) + (8 x 4) + (6 x 3.2) = 91.2 mA. From the curve: for I_{OL} = 4 mA, εI_{OL} = 93 mA since 91.2 mA < 93 mA the loads are within specified limits.

Although the 20 mA@1V load are used in calculating εI_{OL}, it is the largest current required @.45V which determines the maximum allowable εI_{OL}.

TMP8243P

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating
V_{CC}	V_{CC} Supply Voltage with Respect to GND	-0.5V to +7.0V
V_{IN}	Input Voltage with Respect to GND	-0.5V to +7.0V
V_{OUT}	Output Voltage with Respect to GND	-0.5V to +7.0V
P_D	Power Dissipation	800mW
T_{SOLDER}	Soldering Temperature (Soldering Time 10 sec.)	260°C
T_{STG}	Storage Temperature	-55°C to +150°C
T_{OPR}	Operating Temperature	0°C to +70°C

D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ± 10%

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC}+0.5$	V
V_{OL1}	Output Low Voltage Ports 4-7	I_{OL} = 5mA*			0.45	V
V_{OL2}	Output Low Voltage Port 7	I_{OL} = 20mA			1	V
V_{OL3}	Output Low Voltage Port 2	I_{OL}=0.6mA			0.45	V
V_{OH1}	Output High Voltage Ports 4-7	I_{OH}=-240μA	2.4			V
V_{OH2}	Output High Voltage Port 2	I_{OH}=-100μA	2.4			
I_{IL1}	Input Leakage Port 4-7	$0V \leq V_{IN} \leq V_{CC}$	-10		20	μA
I_{IL2}	Input Leadage Port 2, $\overline{CS}$, PROG	$0V \leq V_{IN} \leq V_{CC}$	-10		10	μA
I_{CC}	V_{CC} Supply Current			10	20	mA
I_{OL}	Sum of all IO_L of 16 Outputs	5 mA Each Pin			80	mA

* See following graph for additional sink current capability

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ± 10%

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
t_A	Code Valid Before PROG	C_L = 80pF	100			ns
t_B	Code Valid After PROG	C_L = 20pF	60			ns
t_C	Data Valid Before PROG	C_L = 80pF	200			ns
t_D	Data Valid After PROG	C_L = 20pF	20			ns
t_H	Floating After PROG	C_L = 20pF	0		150	ns
t_K	PROG Negative Pulse Width		700			ns
t_{CS}	$\overline{CS}$ Valid Before/After PROG		50			ns
t_{PO}	Ports 4-7 Valid After PROG	C_L = 100pF			700	ns
t_{LPI}	Ports 4-7 Valid Before/After PROG		100			ns
t_{ACC}	Port 2 Valid After PROG	C_L = 80pF			650	ns

TMP8243PI : INDUSTRIAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating
V_{CC}	V_{CC} Supply Voltage with Respect to GND	-0.5V to +7.0V
V_{IN}	Input Voltage with Respect to GND	-0.5V to +7.0V
V_{OUT}	Output Voltage with Respect to GND	-0.5V to +7.0V
P_D	Power Dissipation	800mW
T_{SOLDER}	Soldering Temperature (Soldering Time 10 sec.)	260°C
T_{STG}	Storage Temperature	-55°C to +150°C
T_{OPR}	Operating Temperature	-40°C to +85°C

D.C. CHARACTERISTICS TA=-40°C to 85°C, V_{CC}=5V±10%

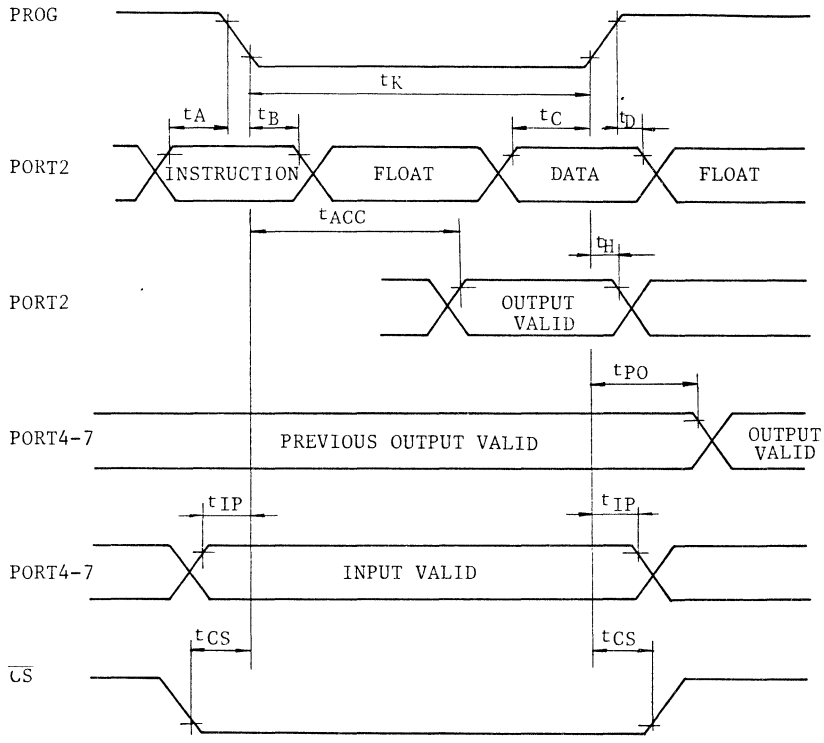
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}+0.5	V
V_{OL1}	Outptu Low Voltage Ports 4-7	I_{OL}=4.5mA			0.45	V
V_{OL2}	Output Low Voltage Port 7	I_{OL}=20mA			1	V
V_{OL3}	Output Low Voltage Port 2	I_{OL}=0.6mA			0.45	V
V_{OH1}	Output High Voltage Ports 4-7	I_{OH}=-240μA	2.4			V
V_{OH2}	Output High Voltage Port 2	I_{OH}=-100μA	2.4			
I_{IL1}	Input Leakage Ports 4-7	$0V \leq V_{IN} \leq V_{CC}$	-10		20	μA
I_{IL2}	Input Leakage Port 2, $\overline{CS}$, PROG	$0V \leq V_{IN} \leq V_{CC}$	-10		10	μA
I_{CC}	V_{CC} Supply Current			10	20	mA
I_{OL}	Sum of all I_{OL} of 16 outputs	4.5mA each pin			72	mA

* See following graph for additional sink current capability

A.C. CHARACTERISTICS TA=-40°C to 85°C, V_{CC}=5V±10%

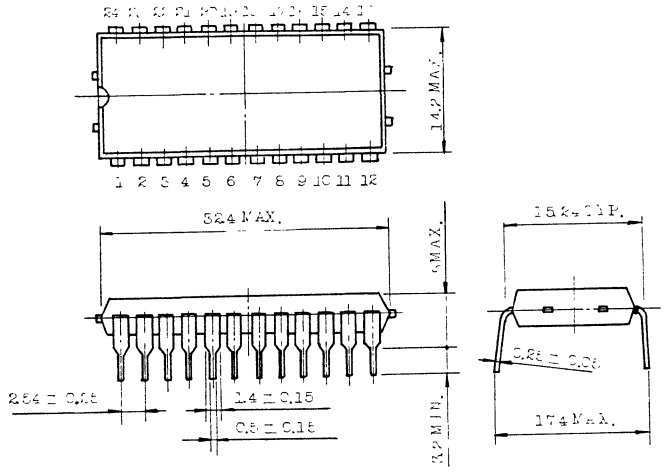
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
t_A	Code Valid before PROG	C_L = 80pF	100			ns
t_B	Code Valid after PROG	C_L = 20pF	60			ns
t_C	Data Valid before PROG	C_L = 80pF	200			ns
t_D	Data Valid after PROG	C_L = 20pF	20			ns
t_H	Floating after PROG	C_L = 20pF	0		150	ns
t_K	PROG Negative Pulse Width		700			ns
t_{CS}	$\overline{CS}$ Valid before/after PROG		50			ns
t_{PO}	Ports 4-7 Valid after PROG	C_L = 100pF			700	ns
t_{LP1}	Ports 4-7 Valid before/after PROG		100			ns
t_{ACC}	Port 2 Valid after PROG	C_L = 80pF			650	ns

TIMING WAVEFORM



OUTLINE DRAWINGS

Unit in mm



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.
All dimensions are in millimeters.

INPUT/OUTPUT EXPANDER

GENERAL DESCRIPTION

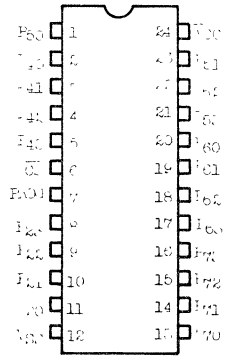
The TMP82C43P is an input/output expander designed specifically to provide a low cost means of I/O expansion for the TLCS-84C family.

The I/O ports of the TMP82C43P serve as a direct extension of the resident I/O facilities of the TLCS-84C microcomputers and are accessed by their own MOVD, ANLD, and ORLD instructions.

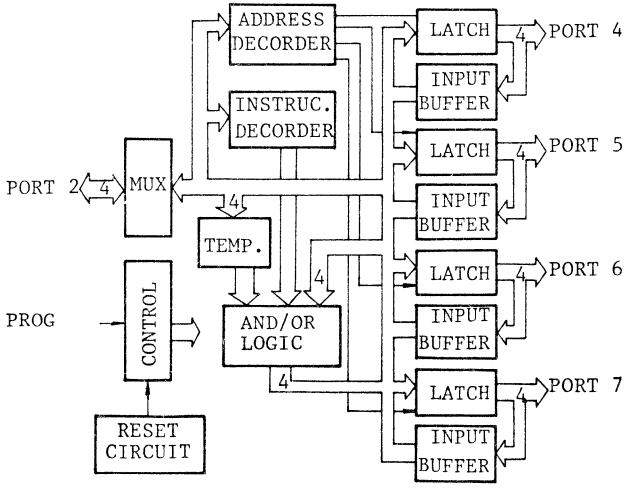
FEATURES

- CMOS LSI for low power dissipation
- Low cost
- Simple interface to TLCS-84C microcomputers
- Four 4-bit I/O ports
- AND and OR directly to ports
- Single 5V supply
- High output drive
- Direct extension of resident TMP80C49P-6 I/O ports.
- PIN compatible with intel's 8243
- Extended operation temperature range -40°C to 85°C

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES AND PIN DESCRIPTION

PROG (Input)

Clock input. A high to low transistion on PROG signifies that address and control are available on P20-23, and a low to high transition signifies that data is available on P20-23.

$\overline{CS}$ (Input)

Chip Select Input. A high on $\overline{CS}$ inhibits any change of output or internal status.

P20-23 (Input/Output, 3-state)

Four (4) bit bi-directional port contains the address and control bits on a high to low transition of PROG. During a low to high transition contains the data for a selected output port if a write operation, or the data from a selected port before the low to high transition if a read operation.

P40-43, P50-53, P60-63, P70-73 (Input/Output, 3-state)

Four (4) bit bi-directional I/O ports. May be programmed to be input (during read), low impedance latched output (after write) or a 3-state (after read). Data on pins P20-23 may be directly written, ANDed or ORed with previous data.

V_{CC} (Power)

+5 volt supply

GND (Power)

0 volt supply

FUNCTIONAL DESCRIPTION

General Operation

The TMP82C43P contains four 4-bit I/O ports which serve as an extension of the on-chip I/O and are addressed as ports 4-7. The following operations may be performed on these ports.

- Transfer accumulator to port
- Transfer port to accumulator
- AND accumulator to port
- OR accumulator to port

All communication between the microcomputer (TMP80C49P-6) and the TMP82C43P occurs over Port 2 (P20-23) with timing provided by an output pulse on the PROG pin of the processor. Each transfer consists of two 4-bit nibbles.

A high to low transition of the PROG line indicates that address is present while a low to high transition indicates the presence of data. Additional TMP82C43P's may be added to the 4-bit bus and chip selected using additional output lines from the microcomputer.

Power On Initialization

Initial application of power to the device forces input/output ports 4, 5, 6, and 7 to the tri-state and port 2 to the input mode. The PROG pin may be either high or low when power is applied. The first high to low transition of PROG causes device to exit power on mode. The power on sequence is initiated if V_{CC} drops below 1V.

P21	P20	Address Code	P23	P22	Instruction Code
0	0	Port 4	0	0	Read
0	1	Port 5	0	1	Write
1	0	Port 6	1	0	ORLD
1	1	Port 7	1	1	ANLD

Write Modes

The device has three write modes. MOVD Pi, A directly writes new data into the selected port and old data is lost. ORLD Pi, A takes new data, OR's it with the old data and then writes it to the port. ANLD Pi, A takes new data AND's it with the old data and then writes it to the port. Operation code and port address are latched from the input port 2 on the high to low transition of the PROG pin. On the low to high transition of PROG data on port 2 is transferred to the logic block of the specified output port.

After the logic manipulation is performed, the data is latched and outputed. T' 'd data remains latched until new valid outputs are entered.

Read Mode

The device has one read mode. The operation code and port address are latched from the input port 2 on the high to low transition of the PROG pin. As soon as the read operation and port address are decoded, the appropriate outputs are 3-stated, and the input buffers switched on. The read operation is terminated by a low to high transition of the PROG pin. The port (4, 5, 6 or 7) that was selected is switched to the 3-stated mode while port 2 is returned to the input mode.

Normally, a port will be in an output (write mode) or input (read·mode). If modes are changed during operation, the first read following a write should be ignored; all following reads are valid. This is to allow the external driver on the port to settle after the first read instruction removes the low impedance drive from the TMP82C43P output. A read of any port will leave that port in a high impedance state.

TMP8243P
ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{CC}	V_{CC} Supply Voltage with Respect to GND	-0.5V to +7.0V
V_{IN}	Input Voltage with Respect to GND	-0.5V to V_{CC}+0.5V
V_{OUT}	Output Voltage with Respect to GND	-0.5V to V_{CC}+0.5V
P_D	Power Dissipation	250mW
T_{SOLDER}	Soldering Temperature (soldering Time 10 sec.)	260°C
T_{STG}	Storage Temperature	-65°C to +150°C
T_{OPR}	Operating Temperature	-40°C to +85°C

D.C. CHARACTERISTICS (I) T_{OPR}=-40°C ~ 85°C, V_{CC}=5V±10%, V_{SS}=0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		2.2			V
V_{OL1}	Output Low Voltage Ports 4-7	I_{OL}=5mA			0.45	V
V_{OL2}	Output Low Voltage Port 7	I_{OL}=20mA			1.0	V
V_{OL3}	Output Low Voltage Port 2	I_{OL}=0.8mA			0.45	V
V_{OH11}	Output High Voltage Ports 4-7	I_{OH}=-1.2mA	2.4			V
V_{OH21}	Output High Voltage Port 2	I_{OH}=-0.6mA	2.4			V
V_{OH12}	Output High Voltage Ports 4-7	I_{OH}=-0.6mA	V_{CC}-0.8			V
V_{OH22}	Output High Voltage Port 2	I_{OH}=-0.3mA	V_{CC}-0.8			V
I_{IL1}	Input Leakage Port 4-7	$V_{SS} \leq V_{IN} \leq V_{CC}$			±10	μA
I_{IL2}	Input Leakage Port 2, $\overline{CS}$, PROG	$V_{SS} \leq V_{IN} \leq V_{CC}$			±10	μA
I_{CC1}	Power Supply Current (1)	V_{CC}=5V, V_{IL}=0.2V V_{IH}=V_{CC}-0.2V PROG PERIOD=5μS			2	mA
I_{CC2}	Power Supply Current (2)	V_{CC}=5V, V_{IL}=0.2V V_{IH}=V_{CC}-0.2V PROG=V_{CC}-0.2V			10	μA
I_{OL}	Sum of all I_{OL} of 16 Outputs	5mA Each pin			80	mA

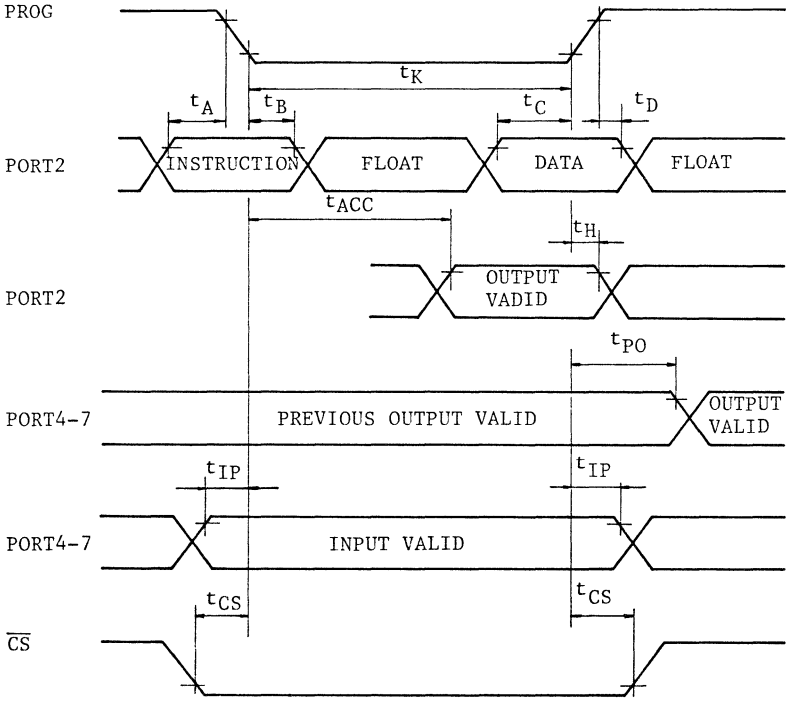
D.C. CHARACTERISTICS (Ⅱ) T_{OPR}=-40°C to 85°C, V_{CC}=5V±20%, V_{SS}=0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
V_{IL}	Input Low Voltage	4.0V≤V_{CC}≤4.5V	-0.5		0.15V_{CC}	V
V_{IH}	Input High Voltage	5.5V≤V_{CC}≤6.0V	0.5V_{CC}		V_{CC}	V
V_{OL1}	Output Low Voltage Ports 4-7	I_{OL}=4mA			0.45	V
V_{OL2}	Output Low Voltage Port 7	I_{OL}=15mA			1.0	V
V_{OL3}	Output Low Voltage Port 2	I_{OL}=0.6mA			0.45	V
V_{OH12}	Output High Voltage Ports 4-7	I_{OH}=-200μA	V_{CC}-0.8			V
V_{OH22}	Output High Voltage Port 2	I_{OH}=-100μA	V_{CC}-0.8			V
I_{OL}	Sum of all I_{OL} of 16 outputs	4mA Each Pin			64	mA

A.C. CHARACTERISTICS T_{OPR}=-40°C to 80°C, V_{CC}=5V±20%, V_{SS}=0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
t_A	Code Valid Before PROG	C_L=80pF	100			ns
t_B	Code Valid After PROG	C_L=20pF	60			ns
t_C	Data Valid Before PROG	C_L=80pF	200			ns
t_D	Data Valid After PROG	C_L=20pF	20			ns
t_H	Floating After PROG	C_L=20pF	0		150	ns
t_K	PROG Negative Pulse Width		700			ns
t_{CS}	$\overline{CS}$ Valid Before/After PROG		50			ns
t_{PO}	Ports 4-7 Valid After PROG	C_L=100pF			700	ns
t_{IP}	Ports 4-7 Valid Before/After PROG		100			ns
t_{ACC}	Port 2 Valid After PROG	C_L=80pF			650	ns

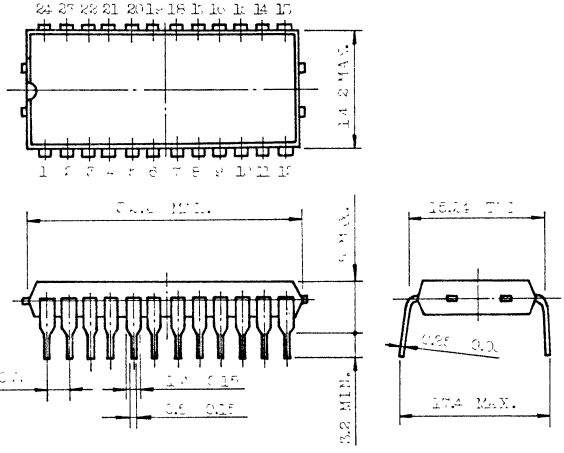
TIMING WAVEFORM



OUTLINE DRAWINGS

PLASTIC PACKAGE

Unit in mm



(Note)

Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.

Super Integrated New CPU Products

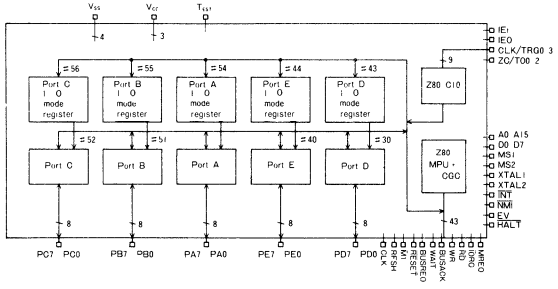
Philosophy

Toshiba has developed the advanced CMOS VLSI technology needed to integrate a Microprocessor and several Peripheral Devices onto a single Monolithic Silicon Die. Using this Super Integration technology Toshiba has the capability to define and produce CMOS devices with a particular configuration of CPU and Peripheral Devices, which will meet the requirements of specific kinds of applications. The first of these APPLICATION SPECIFIC STANDARD PRODUCTS (ASSP) will soon be available. These devices offer the user the benefits of lower system cost, greatly reduced PCB size, higher system reliability, reduced assembly and test costs, and lower power dissipation.

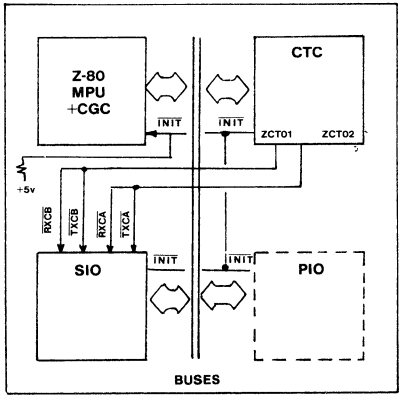
ASSP Products

Type Number	Function	No. of Pins/Pkg	Production Availability
TMPZ84C011AF	Z80 MPU (4Mhz) + CGC + CTC + I/O (8×5)	100/MFP	Nov, 86
TMPZ84C011AF-6	Z80 MPU (6Mhz) + CGC + CTC + I/O (8×5)	100/MFP	Jan, 87
TMPZ84C015AF	Z80 MPU (4Mhz) + CGC + CTC + PIO + SIO	100/MFP	Jan, 87
TMPZ84C015AF-6	Z80 MPU (6Mhz) + CGC + CTC + PIO + SIO	100/MFP	Jan, 87
TMPZ84C013AT	Z80 MPU (4Mhz) + CGC + CTC + SIO	84/PLCC	Feb, 87
TMPZ84C013AT-6	Z80 MPU (6Mhz) + CGC + CTC + SIO	84/PLCC	Feb, 87

TMPZ84C011AF Block Diagram



TMPZ84C013/015 Block Diagram



TMPZ84C011AF Applications

- Industrial Control
- Robotics
- I/O Intensive Processor

TMPZ84C013/015 Applications

- Modems
- LAN's
- Communications Control Processor

*Note These devices also have Watchdog Timer Function

TMPZ84C011AF/TMPZ84C011AF-6
CMOS Z80 MICROPROCESSOR

GENERAL DESCRIPTION

TMPZ840C011A is a high performance and low power CMOS Z80 microprocessor containing peripheral functions such as on-chip clock generator controller (CGC), counter timer circuit (CTC), and five 8-bit parallel input/output ports. TMPZ84C011A is fabricated with Toshiba's C^2 MOS technology and molded in 100 pin flat package.

FEATURES

- Z80® software compatible
- High speed operation (4/6MHz)
- On-chip clock generator controller
- Stand-by control is available.
- Low power consumption
  - Operating power supply current : 15 mA Typ. @ 4MHz
  - Power supply current in IDLE mode : 1 mA Typ. @ 4MHz
  - Stand-by current : 500 nA Typ.
- Single power supply : 5V±10%
- Wide operating temperature range : −40°C to 85°C
- Three operation modes
  - (1) Run Mode (Normal operation)
  - (2) Idle Mode (Only clock generator continues to operate)
  - (3) Stop Mode (All operation is stopped : Stand-by state)
- Five 8-bit ports (can be programmed as input or output for each I/O bit)
- Four independent 8-bit counter/timer channels
- On-chip dynamic memory refresh register
- Three modes of high speed interrupt processing : 8080 similar, non Z-80 peripheral device, and Z80 family peripheral with or without daisy chain.
- 100-pin flat package
- Real-time emulator RTE 80 and emulation board (BM8024) are available.

Note) Five 8-bit parellel I/O ports do not have daisy chain interrupt function.

Z80® is a trademark of Zilog Inc.

PIN NAMES AND PIN DESCRIPTION

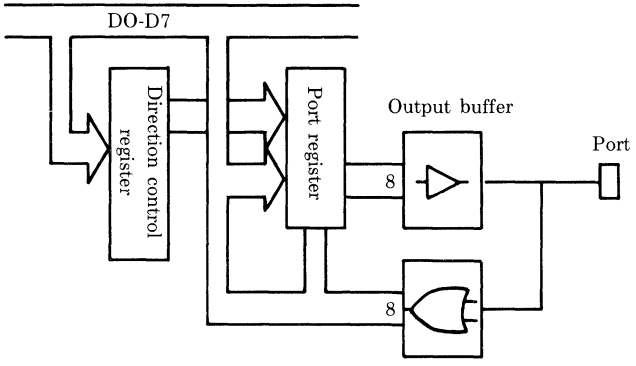
Pin Name	No. of Pins	Direction	Description
D 0 -D7	8	I/O, 3-atate	8-bit bidirectional data bus
A 0 -A15	16	Output, 3-state	16-bit address bus
PA0 -PA 7	8	I/O, 3-atate	Port A : Input / Output port
PB0 -PB 7	8	I/O, 3-atate	Port B : Input / Output port
PCO -PC 7	8	I/O, 3-atate	Port C : Input / Output port
PDO -PD7	8	I/O, 3-atate	Port D : Input / Output port
PEO -PE 7	8	I/O, 3-atate	Port E : Input / Output port
$\overline{M1}$	1	Output, 3-state	Machine cycle 1
$\overline{RD}$	1	Output, 3-state	Memory read
$\overline{WR}$	1	Output, 3-state	Memory write
$\overline{MREQ}$	1	Output, 3-state	Memory request
$\overline{IORQ}$	1	Output, 3-state	Input / Output request
$\overline{WAIT}$	1	Input	Wait request
$\overline{BUSREQ}$	1	Input	Bus request
$\overline{BUSACK}$	1	Output	Bus acknowledge
$\overline{HALT}$	1	Output, 3-state	HALT
$\overline{RFSH}$	1	Output	Refresh
EV	1	Input	Input signal for emulator mode. When EV Terminal is in high level, $\overline{M1}$ and $\overline{HALT}$ output is in high impedance state. When EV terminal is high with active $\overline{BUSREQ}$, TMPZ84C011A will relinquish the internal Z80 cpu portion and will be controlled by another cpu (i.e. cpu in ICE).
TEST	1	Input	Test terminal. It must be tied to ground.
CLK/TRG0 -CLK/TRG3	4	Input	External clock/timer trigger
ZC/T00 -ZC/TC02	3	Output	Zero count/timer out
IEI	1	Input	Interrupt enable input for CTC
IEO	1	Output	Interrupt enable output for CTC
XTAL1/XTAL2	2	Input/Output	X'tal input/output. Two times frequency is required for cpu operation.
MS1, MS2	2	Input	Mode control inputs

MS1	MS2	Mode
0	0	IDLE
0	1	Do not use
1	0	STOP
1	1	RUN

CLK	1	Output	Single phase system clock output.
$\overline{RESET}$	1	Input	Reset input.
$\overline{INT}$	1	Input	Maskable interrupt request.
$\overline{NMI}$	1	Input	Non maskable interrupt request.
Vcc	1		5V power supply.
Vss	1		Ground reference. (OV)

I/O PORT CONFIGURATION AND ASSIGNMENT

(1) Port configuration



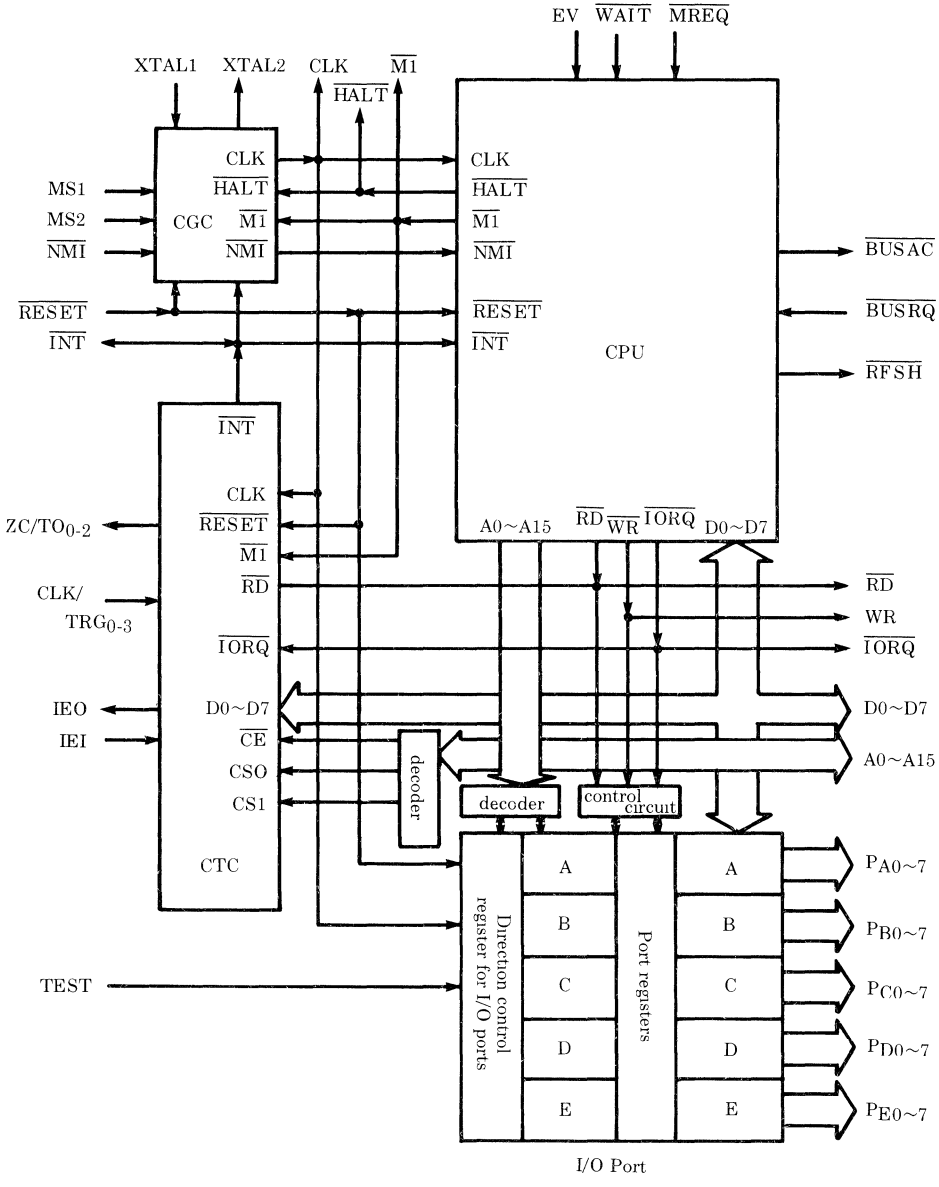
Note) Each I/O bit can be programmed as input or output. When reset occurs, Direction control register and port register are cleared, therefore, all ports are in input mode.

Content in Direction Register	Port Direction
0	Input
1	Output

(2) I/O assignment

I/O Name	Address									I/O Function
	A7	A6	A5	A4	A3	A2	A1	A0		
CTC (Counter /Timer)	0	0	0	1	0	0	0	0	$10	Channel 0
	0	0	0	1	0	0	0	1	$11	1
	0	0	0	1	0	0	1	0	$12	2
	0	0	0	1	0	0	1	1	$13	3
Port A	0	1	0	1	0	1	0	0	$54	Direction Register
	0	1	0	1	0	0	0	0	$50	Port Register A
Port B	0	1	0	1	0	1	0	1	$55	Direction Register
	0	1	0	1	0	0	0	1	$51	Port Register B
Port C	0	1	0	1	0	1	1	0	$56	Direction Register
	0	1	0	1	0	0	1	0	$52	Port Register C
Port D	0	0	1	1	0	1	0	0	$34	Direction Register
	0	0	1	1	0	0	0	0	$30	Port Register D
Port E	0	1	0	0	0	1	0	0	$44	Direction Register
	0	1	0	0	0	0	0	0	$40	Port Register E

BLOCK DIAGRAM



TOSHIBA

Preliminary

TMPZ84C013AT
TMPZ84C013AT-6

(CMOS Z80 Microprocessor)

Communications Control Processor

November 1986

TOSHIBA CORPORATION

TMPZ84C013AT/TMPZ84C013AT-6
(CMOS Z80 MICROPROCESSOR)
COMMUNICATIONS CONTROL PROCESSOR

GENERAL DESCRIPTION

TMPZ84C013AT is a low power CMOS Z80 8-bit microprocessor containing peripheral functions such as on-chip clock generator (CGC), counter timer circuit (CTC), serial input/output controller (SIO) and watch dog timer.

TMPZ84C013AT is designed for broad range of communication applications and has two independent full-duplex channels with separate control and status lines for modems or other devices.

TMPZ84C013A is fabricated with Toshiba's C^2 MOS technology and molded in 84-pin PLCC package.

FEATURES

- Z80® software compatible
- Low Power Consumption
- High speed operation: TMPZ84C013AT 4MHz
  TMPZ84C013AT-6 6MHz
- Single Power Supply: 5V±10%
- On-chip clock generator and controller
- On-chip peripheral functions
  (1) Four independent 8-bit counter/timer channels
  (2) Two independent full-duplex serial channels
    - Data rates of 0 to 800K bits/second in the x1 clock mode with a 4MHz clock.
    - Asynchronous protocols in 5, 6, 7 or 8 bits/character including variable stop bits and several clock-rate multipliers; break generation and detection; parity; overrun and framing error detection.
    - Synchronous protocols: complete bit-or byte oriented IBM Bisync, SDLC, HDLC, CCITT-X.25 and others. Automatic CRC generation/checking, sync character and zero insertion/deletion, abort generation/detection, and flag insertion.
- Watch dog timer
- On-chip dynamic memory refresh register (8-bit)
- Four Operation mode including power save function.
  RUN mode (Normal operation)
  IDLE1 mode (CPU operation is stopped, but only oscillator works)
  IDLE2 mode (CPU operation is stopped, but oscillator, counter/timer and system clock output operation is continued.)
  STOP mode (All operations are stopped)
- Three modes of high speed interrupt processing: 8080 similar, non-Z80 peripheral device, and Z80 family peripheral with or without daisy chain.
- Extended operating temperature: −40°C to 85°C
- Molded in 84-pin plastic leaded chip carrier.

Z80® is a trademark of Zilog Inc.

The following is I/O Assignment and additional functions to the standard Z80 family devices.

1. I/O ASSIGNMENT

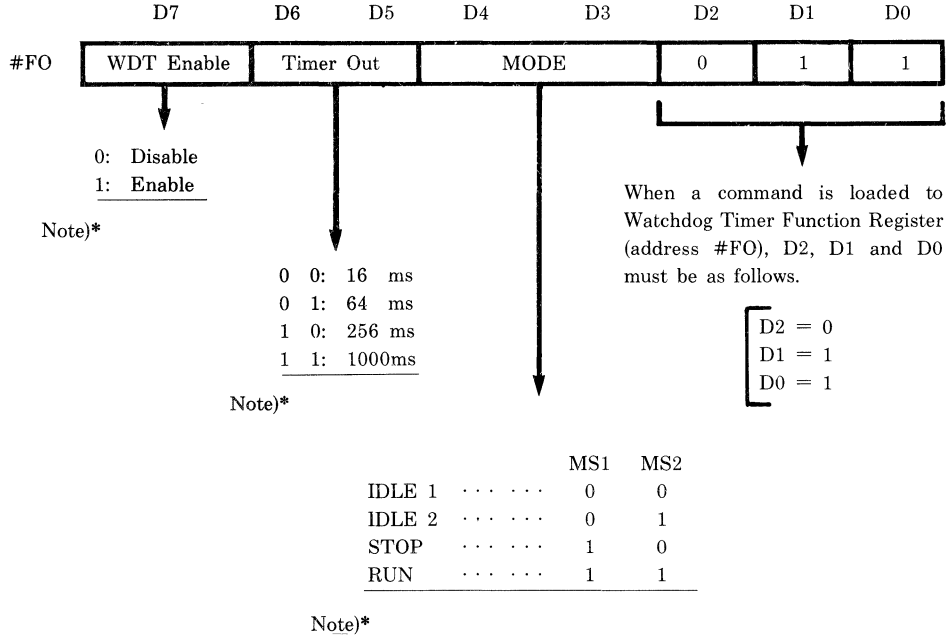
I/O Name	Address									I/O Function
	A7	A6	A5	A4	A3	A2	A1	A0		
:	:	:	:	:	:	:	:	:		
:	:	:	:	:	:	:	:	:		
CTC (Counter /timer)	0	0	0	1	0	0	0	0	#10	Channel 0
	0	0	0	1	0	0	0	1	#11	1
	0	0	0	1	0	0	1	0	#12	2
	0	0	0	1	0	0	1	1	#13	3
:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:
SIO (Serial I/O)	0	0	0	1	1	0	0	0	#18	Channel A Data
	0	0	0	1	1	0	0	1	#19	A Command
	0	0	0	1	1	0	1	0	#1A	B Data
	0	0	0	1	1	0	1	1	#1B	B Command
:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:
Watchdog timer	1	1	1	1	0	0	0	0	#F0	Watch dog Timer
	1	1	1	1	0	0	0	1	#F1	Control
:	:	:	:	:	:	:	:	:	:	:
Daisy chain	1	1	1	1	0	1	0	0	#F4	
:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:

2. WATCHDOG TIMER

FUNCTION REGISTER #FO

(WRITE/READ)

2-1. Write Operation (Command Set)

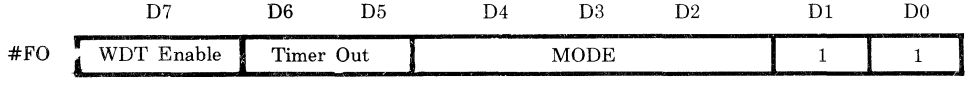


	MS1	MS2
IDLE 1	0	0
IDLE 2	0	1
STOP	1	0
RUN	1	1

Note)*

Note)*When RESET occurs, Timer Out will be set as 1000 ms.
Also cpu will be set in Run Mode and Watchdog Timer is enabled.

2-2. Read Operation (Status Read)



When status is read out from address #FO, D1 and D0 will be always high ("1") and the other (D7 through D2) will be in the status when a command has been loaded.

2-3. Commands

1) D7 (Enabling the watchdog timer)

*) D7=1 : Watch Dog Enable
D7=0 : Watch Dog Disable

Note*) When RESET occurs, watch-dog timer is enabled (D7=1).

2) D6, D5 (Determining time period for prescaler)

D6	D5	Time	
0	0	16 ms	
0	1	64 ms	
1	0	256 ms	
1	1	1000 ms	at 4MHz

*)

Note*) When RESET occurs, prescaler will be set as 1000 ms.

3) D4~D3 (Mode control for clock generator)

D4	D3	
0	0	IDLE1
0	1	IDLE2
1	0	STOP
1	1	RUN

*)

Note*) When RESET occurs, CPU will be set as RUN mode.

Mode	Internal operation					CLKOUT Status
	CG	CPU	WD Timer	CTC	SIO	
IDLE 1	O	S	S	S	S	S
IDLE 2	O	S	S	O	S	O
STOP	S	S	S	S	S	S
RUN	O	O	O	O	O	O

O · · · · · · Operating (CLKOUT and CLKIN must be connected.)
S · · · · · · Stop

4) D1=1, D0=1

When a command is loaded to address #FO, D1 and D0 must be high ("1").

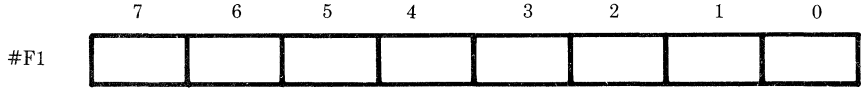
Output Pulse width of $\overline{\text{WDTOUT}}$.

a. When $\overline{\text{WDTOUT}}$ terminal is connected with $\overline{\text{RESET}}$ terminal. : Low level pulse during five clock cycles will be output.

b. When $\overline{\text{WDTOUT}}$ terminal is connected with other than $\overline{\text{RESET}}$ terminal. : Low level pulse will be output until software reset or hardware reset is generated.

3. WATCHDOG TIMER FUNCTION REGISTER #F1

(WRITE ONLY)



(Explanation for commands)

1) "B1" : Disable Watchdog Timer

D7 of I/O address #F0 must be cleared and then #B1 must be loaded to I/O address #F1.

2) "4E" : Clear Watchdog Timer

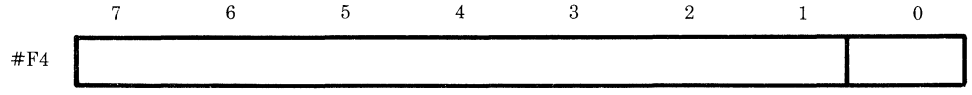
#4E Must be loaded to I/O address #F1. This command is independent of D7 of I/O address #F0.

3) "DB" : Updating content of D4 and D3 in I/O address #F0:

#DB must be loaded to I/O address #F1 before updating D4 and D3.

4. INTERRUPT PRIORITY CONTROL REGISTER

#F4 (WRITE ONLY)



(Priority)

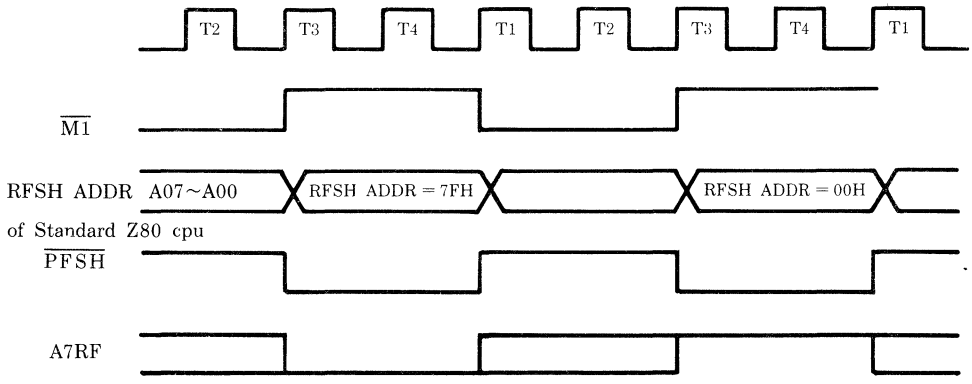
* CTC — SIO 0

SIO — CTC 1

*) After Reset

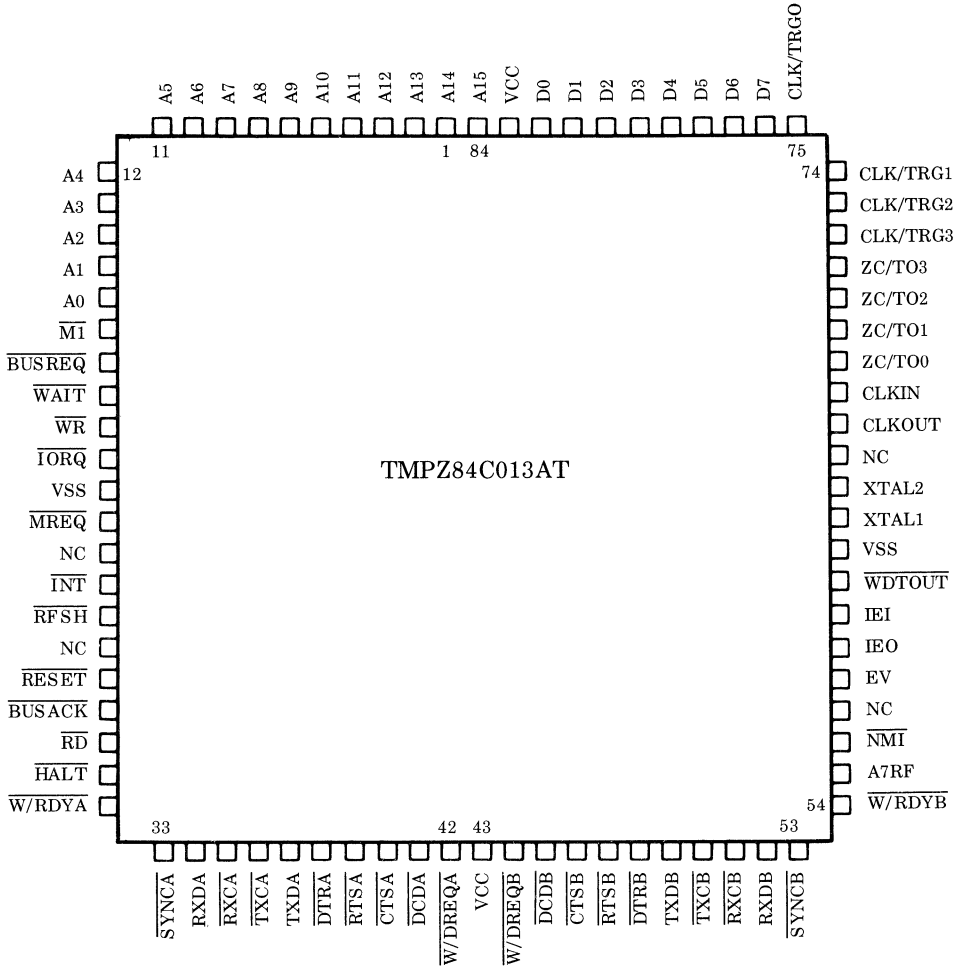
5. $\overline{\text{RFSH}}$ ADDRESS

A7' is added to refresh dynamic RAM in $\overline{\text{M1}}$ cycle automatically.



RFSH ADDR A00~A07 '7FH' '8OH'
of TMPZ84C013A

PIN CONNECTION
84-PIN PLCC



TOSHIBA

Preliminary

TMPZ84C015AF
TMPZ84C015AF-6

(CMOS Z80 Microprocessor)

Communications Control Processor

November 1986

TOSHIBA CORPORATION

TMPZ84C015AF/TMPZ84C015AF-6
(CMOS Z80 MICROPROCESSOR)
COMMUNICATIONS CONTROL PROCESSOR

GENERAL DESCRIPTION

TMPZ84C015A is a low power CMOS Z80 8-bit microprocessor containing peripheral functions such as on-chip clock generator (CGC), counter timer circuit (CTC), parallel input/output (PIO), serial input/output controller (SIO) and watch dog timer.

TMPZ84C015A is designed for broad range of communication applications and has two independent full-duplex channels with separate control and status lines for modems or other devices.

TMPZ84C015A is fabricated with Toshiba's C^2 MOS technology and molded in 100-pin flat package.

FEATURES

- Z80® software compatible
- Low Power Consumption
- High speed operation: TMPZ84C015AF 4MHz
  TMPZ84C015AF-6 6MHz
- Single Power Supply: 5V±10%
- On-chip clock generator and controller
- On-chip peripheral functions
  (1) Four independent 8-bit counter/timer channels
  (2) Two independent full-duplex serial channels
    - Data rates of 0 to 800K bits/second in the x1 clock mode with a 4MHz clock.
    - Asynchronous protocols in 5, 6, 7 or 8 bits/character including variable stop bits and several clock-rate multipliers; break generation and detection; parity; overrun and framing error detection.
    - Synchronous protocols: complete bit-or byte oriented IBM Bisync, SDLC, HDLC, CCITT-X.25 and others. Automatic CRC generation/checking, sync character and zero insertion/deletion, abort generation/detection, and flag insertion.
  (3) Two independent 8-bit input/output ports with handshake function.
- Watch dog timer
- On-chip dynamic memory refresh register (8-bit)
- Four Operation mode including power save function.
  RUN mode (Normal operation)
  IDLE1 mode (CPU operation is stopped, but only oscillator works)
  IDLE2 mode (CPU operation is stopped, but oscillator, counter/timer and system clock output operation is continued.)
  STOP mode (All operations are stopped)
- Three modes of high speed interrupt processing: 8080 similar, non-Z80 peripheral device, and Z80 family peripheral with or without daisy chain.
- Extended operating temperature: −40°C to 85°C
- Molded in 100-pin flat package.

Z80® is a trademark of Zilog Inc.

The following is I/O Assignment and additional functions to the standard Z80 family devices.

1. I/O ASSIGNMENT

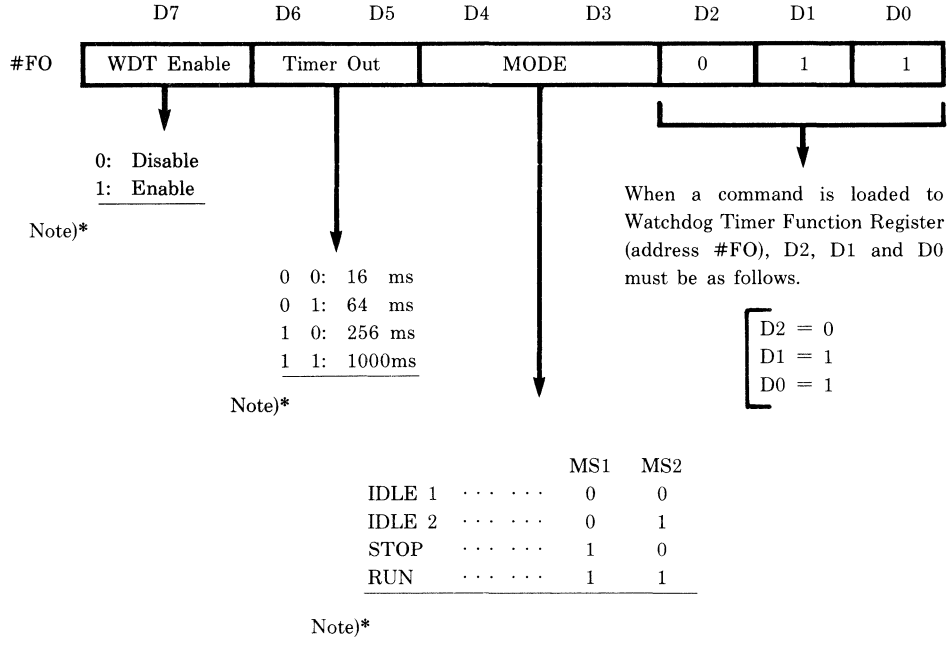
I/O Name	Address									I/O Function
	A7	A6	A5	A4	A3	A2	A1	A0		
:	:	:	:	:	:	:	:	:		
:	:	:	:	:	:	:	:	:		
CTC (Counter /timer)	0	0	0	1	0	0	0	0	#10	Channel 0
	0	0	0	1	0	0	0	1	#11	1
	0	0	0	1	0	0	1	0	#12	2
	0	0	0	1	0	0	1	1	#13	3
:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:
SIO (Serial I/O)	0	0	0	1	1	0	0	0	#18	Channel A Data
	0	0	0	1	1	0	0	1	#19	A Command
	0	0	0	1	1	0	1	0	#1A	B Data
	0	0	0	1	1	0	1	1	#1B	B Command
PIO (Paraller I/O)	0	0	0	1	1	1	0	0	#1C	Channel A Data
	0	0	0	1	1	1	0	1	#1D	A Command
	0	0	0	1	1	1	1	0	#1E	B Data
	0	0	0	1	1	1	1	1	#1F	B Command
Watchdog timer	1	1	1	1	0	0	0	0	#F0	Watch dog Timer
	1	1	1	1	0	0	0	1	#F1	Control
:	:	:	:	:	:	:	:	:	:	:
Daisy chain	1	1	1	1	0	1	0	0	#F4	
:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:

2. WATCHDOG TIMER

FUNCTION REGISTER #FO

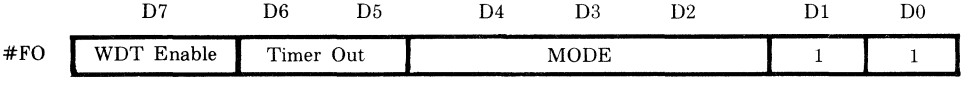
(WRITE/READ)

2-1. Write Operation (Command Set)



Note)*When RESET occurs, Timer Out will be set as 1000 ms.
Also cpu will be set in Run Mode and Watchdog Timer is enabled.

2-2. Read Operation (Status Read)



When status is read out from address #FO, D1 and D0 will be always high ("1") and the other (D7 through D2) will be in the status when a command has been loaded.

2-3. Commands

1) D7 (Enabling the watchdog timer)

*) D7=1 : Watch Dog Enable
D7=0 : Watch Dog Disable

Note*) When RESET occurs, watch-dog timer is enabled (D7=1).

2) D6, D5 (Determining time period for prescaler)

D6	D5	Time	
0	0	16 ms	
0	1	64 ms	
1	0	256 ms	
1	1	1000 ms	at 4MHz

*)

Note*) When RESET occurs, prescaler will be set as 1000 ms.

3) D4~D3 (Mode control for clock generator)

D4	D3	
0	0	IDLE1
0	1	IDLE2
1	0	STOP
1	1	RUN

*)

Note*) When RESET occurs, cpu will be set as RUN mode.

Mode	Internal operation						CLKOUT Status
	CG	CPU	PIO	WD Timer	CTC	SIO	
IDLE 1	O	S	S	S	S	S	S
IDLE 2	O	S	S	S	O	S	O
STOP	S	S	S	S	S	S	S
RUN	O	O	O	O	O	O	O

O · · · · · · Operating (CLKOUT and CLKIN must be connected.)
S · · · · · · Stop

4) D1=1, D0=1

When a command is loaded to address #FO, D1 and D0 must be high ("1").

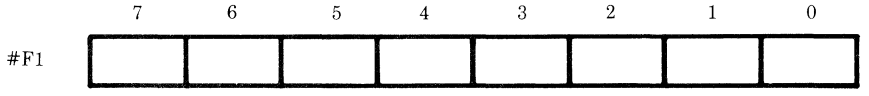
Output Pulse width of $\overline{\text{WDTOUT}}$.

a. When $\overline{\text{WDTOUT}}$ terminal is connected with $\overline{\text{RESET}}$ terminal. : Low level pulse during five clock cycles will be output.

b. When $\overline{\text{WDTOUT}}$ terminal is connected with other than $\overline{\text{RESET}}$ terminal. : Low level pulse will be output until software reset or hardware reset is generated.

3. WATCHDOG TIMER FUNCTION REGISTER #F1

(WRITE ONLY)



(Explanation for commands)

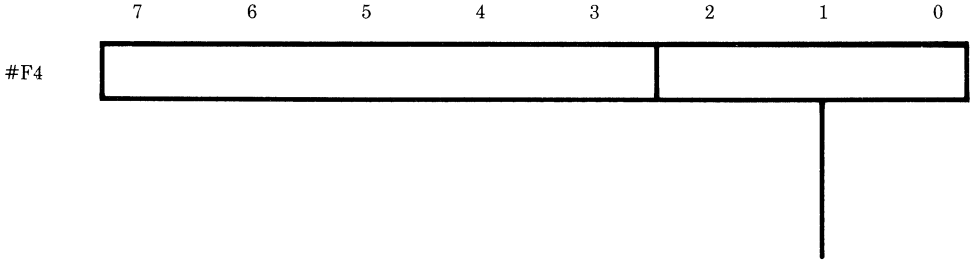
1) "B1" : Disable Watchdog Timer : D7 of I/O address #F0 must be cleared and then #B1 must be loaded to I/O address #F1.

2) "4E" : Clear Watchdog Timer : #4E Must be loaded to I/O address #F1. This command is independent of D7 of I/O address #F0.

3) "DB" : Updating content of D4 and D3 in I/O address #F0:
#DB must be loaded to I/O address #F1 before updating D4 and D3.

4. INTERRUPT PRIORITY CONTROL REGISTER

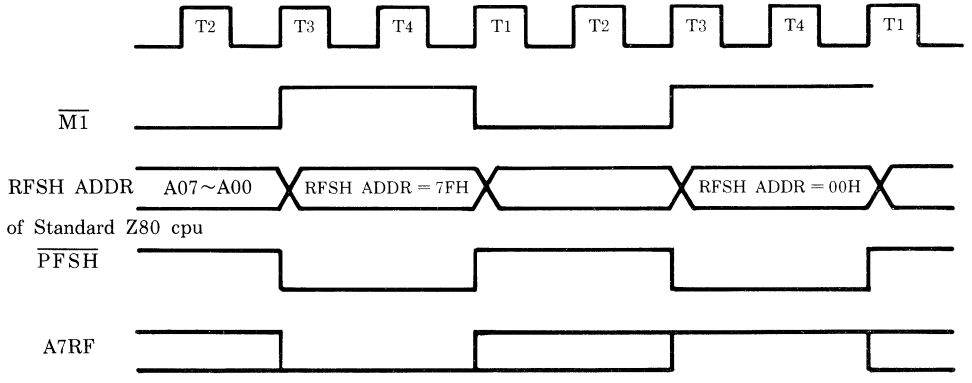
#F4 (WRITE ONLY)



	(Priority)				*)
*	CTC — SIO — PIO	0	0	0	After
	SIO — CTC — PIO	0	0	1	Reset
	CTC — PIO — SIO	0	1	0	
	PIO — SIO — CTC	0	1	1	
	PIO — CTC — SIO	1	0	0	
	SIO — PIO — CTC	1	0	1	

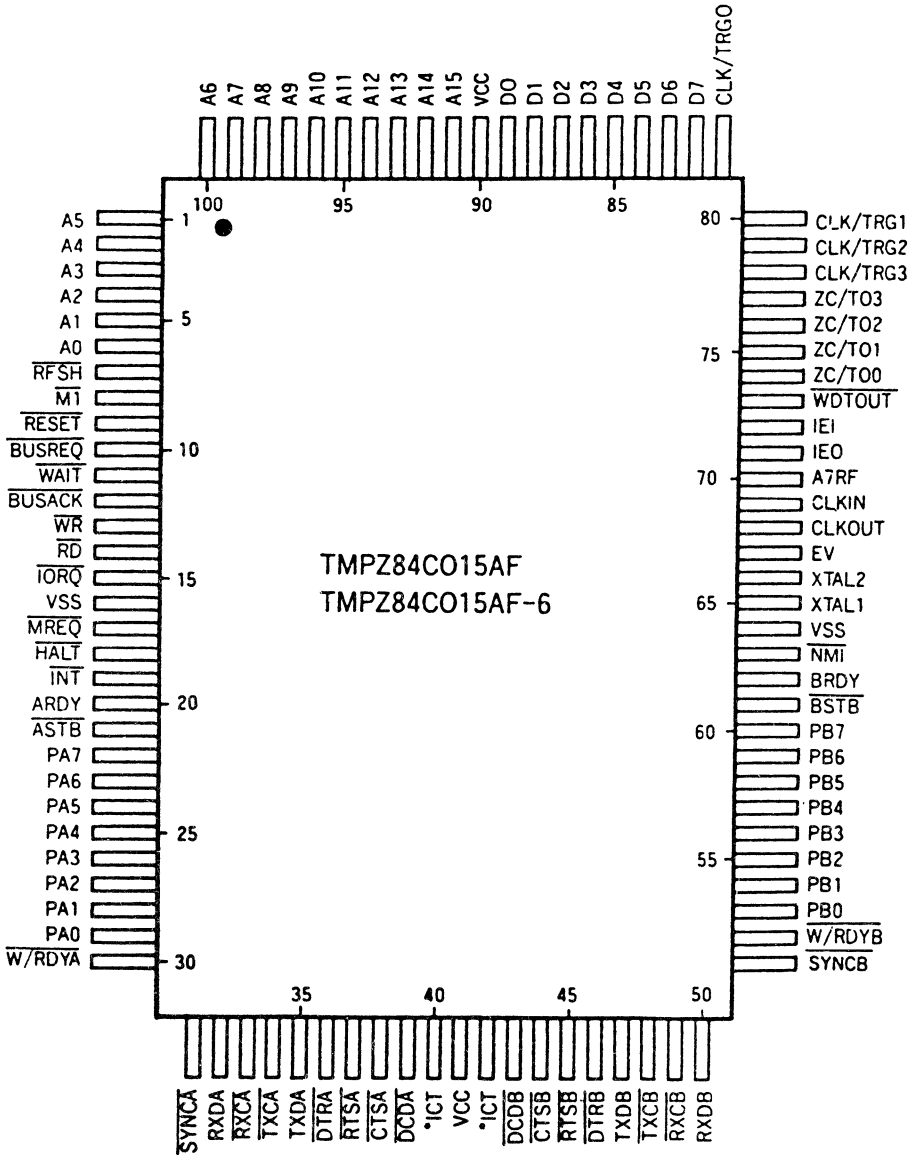
5. $\overline{\text{RFSH}}$ ADDRESS

A7' is added to refresh dynamic RAM in $\overline{\text{M1}}$ cycle automatically.



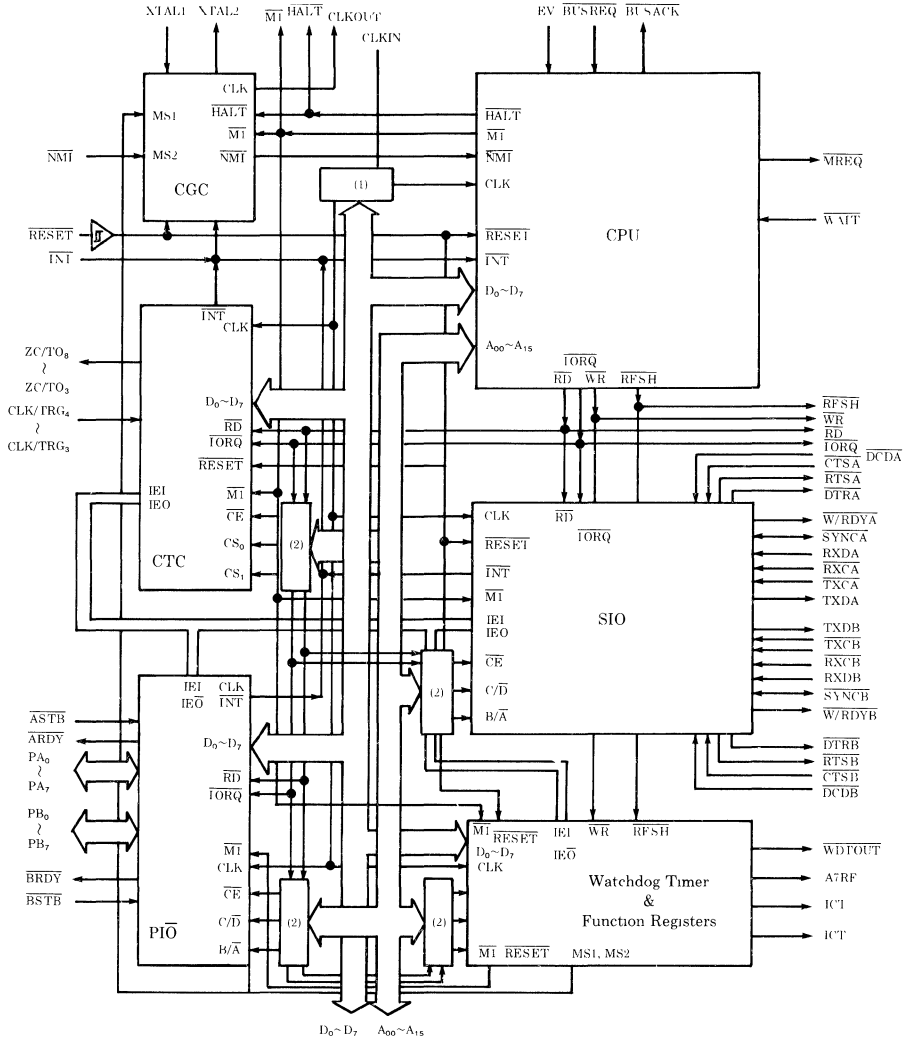
RFSH ADDR A00~A07 '7FH' '8OH'
of TMPZ84C013A

PIN CONNECTION



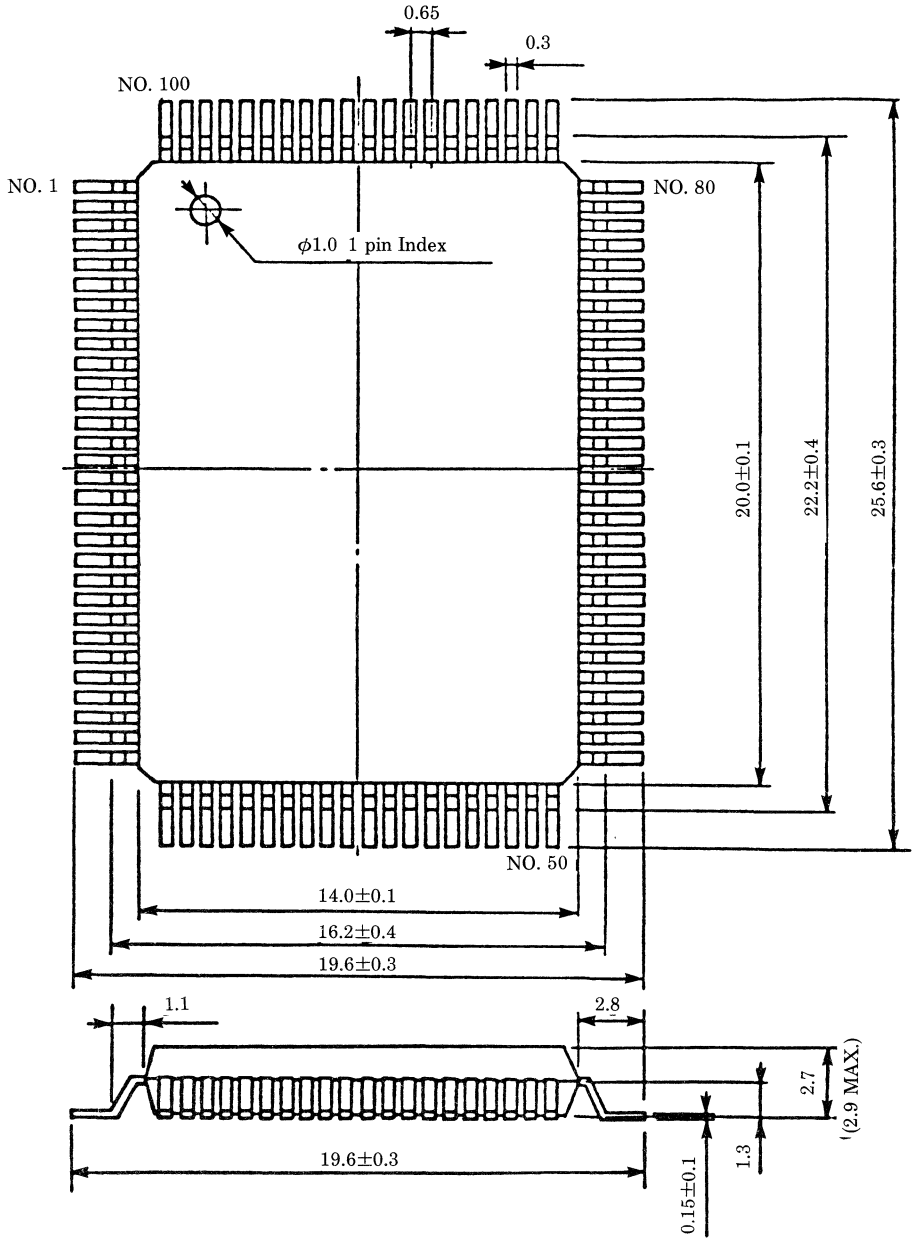
Note) ICT terminal must be open

BLOCK DIAGRAM



Note (1) Control circuit
(2) Decoder

Unit : mm


0.65
0.3
NO. 100
NO. 1
NO. 80
φ1.0 1 pin Index
20.0±0.1
22.2±0.4
25.6±0.3
NO. 50
14.0±0.1
16.2±0.4
19.6±0.3
1.1
2.8
2.7
(2.9 MAX.)
19.6±0.3
1.3
0.15±0.1

TMP82C54P/TMP82C54P-2
PROGRAMMABLE INTERVAL TIMER

The TMP82C54P/P-2 is a programmable counter/timer fabricated in Silicon Gate CMOS technology which provide low power operation and high performance. It is organized as three independent 16-bit counters, with high clock rate input.

The TMP82C54P/P-2 has six operational modes. All modes of operation are software programmable.

The TMP82C54P/P-2 is a superset of TMP82C53P-2.

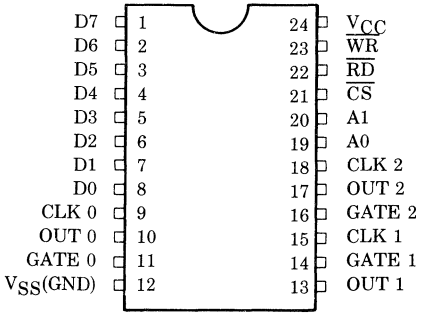
FEATURES

(1) Pin compatible with TMP82C53P-2
(2) Three independent 16-bit counters
(3) Counter latch command
(4) Status Read-Back command
(5) Six programmable Counter Modes
(6) Count Binary or BCD
(7) High speed

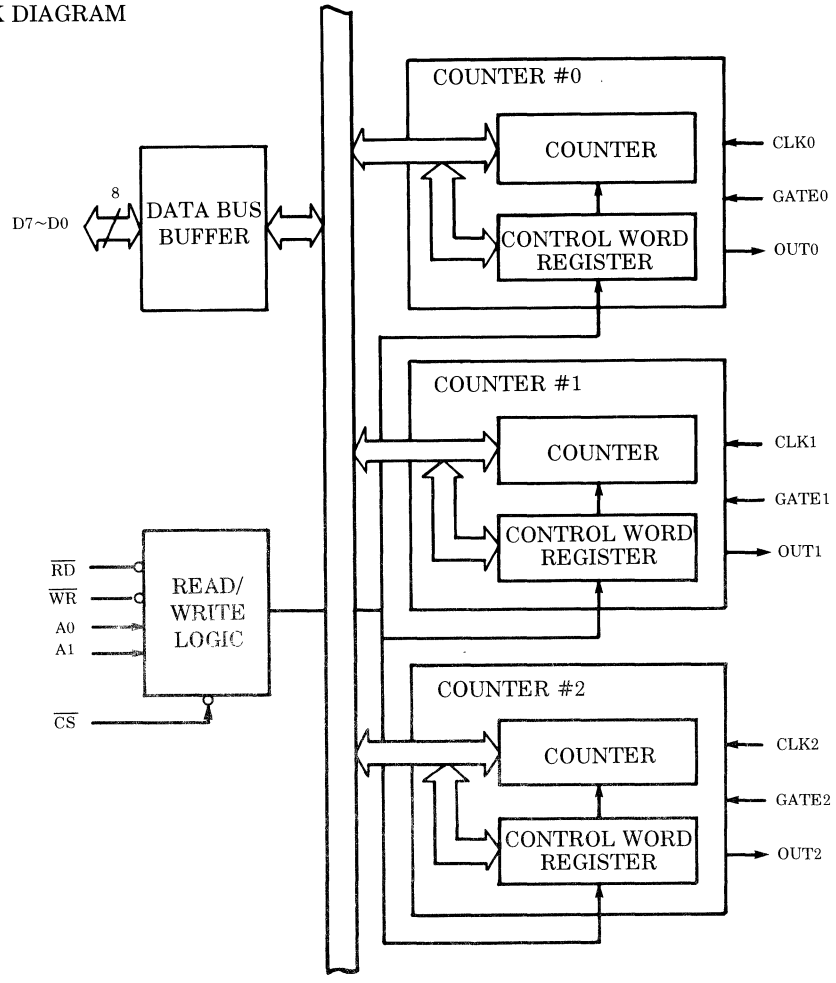
TMP82C54P-2	Clock inputs	10MHz Max.
TMP82C54P	Clock inputs	8MHz Max.

(8) Low power consumption
30mA Max. (at operation)
10μA Max. (at power down)
(9) Operating temperature −40 to 85°C
(10) Supply voltage 5V ± 10%

PIN CONNECTIONS (Top View)



BLOCK DIAGRAM



PIN NAMES AND PIN DESCRIPTION

Pin Name	Input/Output	Function
D7 - D0	I/O	Data bus
CLK 2 - CLK 0	Input	Counter clock inputs
GATE 2 - GATE 0	Input	Counter gate inputs
OUT 2 - OUT 0	Output	Counter outputs
A1 - A0	Input	Counter address
$\overline{RD}$	Input	Read signal
$\overline{WR}$	Input	Write signal
$\overline{CS}$	Input	Chip select
VCC, GND	Power supply	+5V, 0V

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEMS	TEST CONDITION	RATING	UNIT
Vcc	Supply Voltage	With Respect To GND.	−0.5 to +7.0	V
VIN	Input Voltage		−0.5 to Vcc+0.5	V
VOUT	Output Voltage		−0.5 to Vcc+0.5	V
PD	Power Dissipation		250	mW
Tsol	Solder Temperature		260 (10 sec)	°C
Tstg	Storage Temperature		−65 to +150	°C
Topr	Operating Temperature		−40 to +85	°C

DC CHARACTERISTICS (Ta=−40 to +85°C, Vcc=5V±10%, Vss (GND)=OV)

SYMBOL	ITEMS	TEST CONDITONS	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage		−0.5		0.8	V
VIH	Input High Voltage		2.2		Vcc+0.5	V
VOL	Output Low Voltage	IOL=2.2mA			0.45	V
VOH 1	Output High Voltage	IOH=−400mA	2.4			V
VOH 2	Output High Voltage	IOH=−100μA	VCC−0.8			V
IIL	Input Leakage Current	OV ≤ VIN ≤ VCC			±10	μA
IOFL	Output Leakage Current	0.45 ≤ VOUT ≤VCC			±10	μA
ICC 1	Operating Supply Current	CLK=10MHz VIH=VCC−0.2V VIL=0.2V		3	30	mA
ICC 2	Stand-by supply Current	CLK=DC VIH=VCC−0.2V VIL=0.2V			±10	μA

AC CHARACTERISTICS (Ta=−40 to +85°C, VCC=5V±10%, Vss (GND)=OV)
READ/WRITE

SYMBOL	ITEM	TMP82C54P		TMP82C54P-2		UNIT
		MIN.	MAX.	MIN.	MAX.	
tAR	Address Set-up Time (RD)	30		30		ns
tSR	CS Set-up Time (RD)	0		0		ns
tRA	Address Hold Time (RD)	20		20		ns
tRR	RD Pulse Width	150		95		ns
tRD	Valid Data (RD)		120		85	ns
tAD	Valid Data (Address)		220		185	ns
tDF	Data Floating (RD)	5	85	5	65	ns
tAW	Address Set-up Time (WR)	0		0		ns
tSW	CS Set-up Time (WR)	0		0		ns
tWA	Address Hold Time (WR)	0		0		ns
tWW	WR Pulse Width	150		95		ns
tDW	Data Set-up Time (WR)	120		95		ns
tWD	Data Hold Time (WR)	0		0		ns
tRV	Recovery Time	200		165		ns

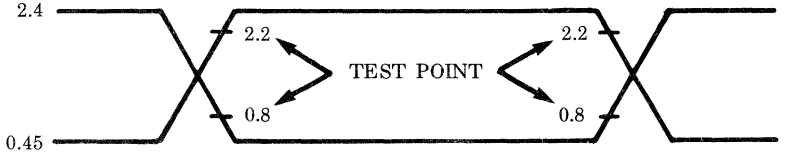
CLOCK/GATE

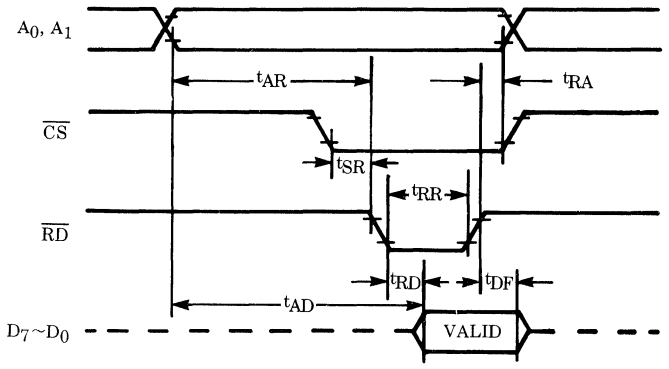
SYMBOL	ITEM	TMP82C54P		TMP82C54P-2		UNIT
		MIN.	MAX.	MIN.	MAX.	
tCLK	Clock Period	125	DC	100	DC	ns
tPWH	CLK High Pulse Width	50		30		ns
tPWL	CLK Low Pulse Width	50		30		ns
tR	CLK Rise Time		25		25	ns
tF	CLK Fall Time		25		25	ns
tGW	GATE Width High	50		50		ns
tGL	GATE Width LOW	50		50		ns
tGS	GATE Set-up Time (CLK)	50		40		ns
tGH	GATE Hold Time (CLK)	50		50		ns
tOD	Output Delay From CLK		150		100	ns
tODG	Output Delay From GATE		120		100	ns
tWC	Count Loading Set-up Time (CLK)	100		80		ns
tWG	WR Set-up Time (GATE)	0		0		ns
tWO	Output Delay From Command Write		260		240	ns
tCL	CLK Set-up Time (Count Latch)	85		68		ns

INPUT CAPACITANCE (Ta=25°C, Vcc=Vss (GND)=V)

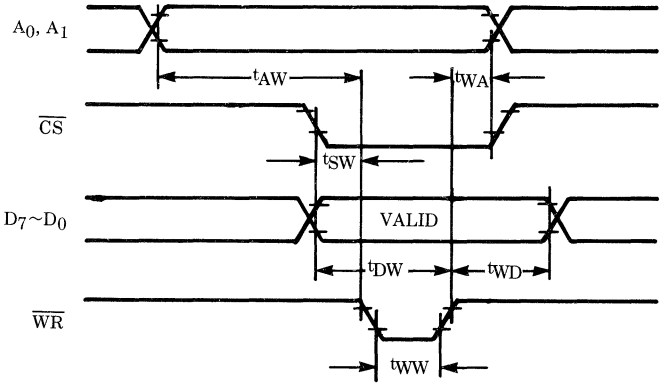
SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CIN	Input Capacitance	fc=1MHz Unmeasured pins, OV			10	pF
CI/O	Input/Output Capacitance				20	pF

AC TESTING INPUT WAVE FORM

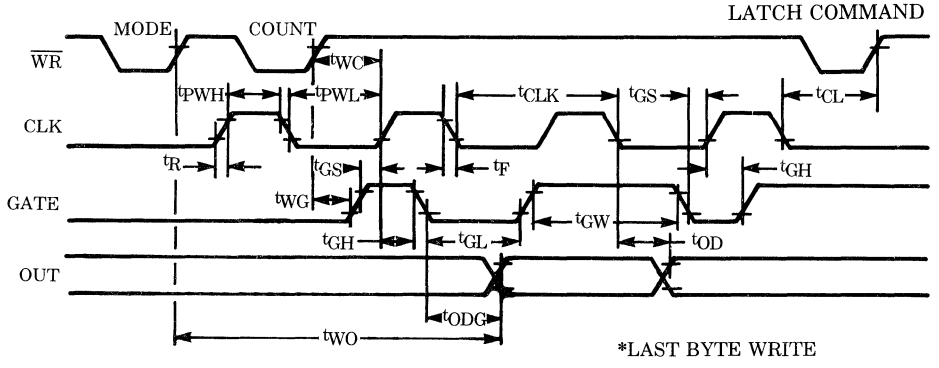




READ TIMING



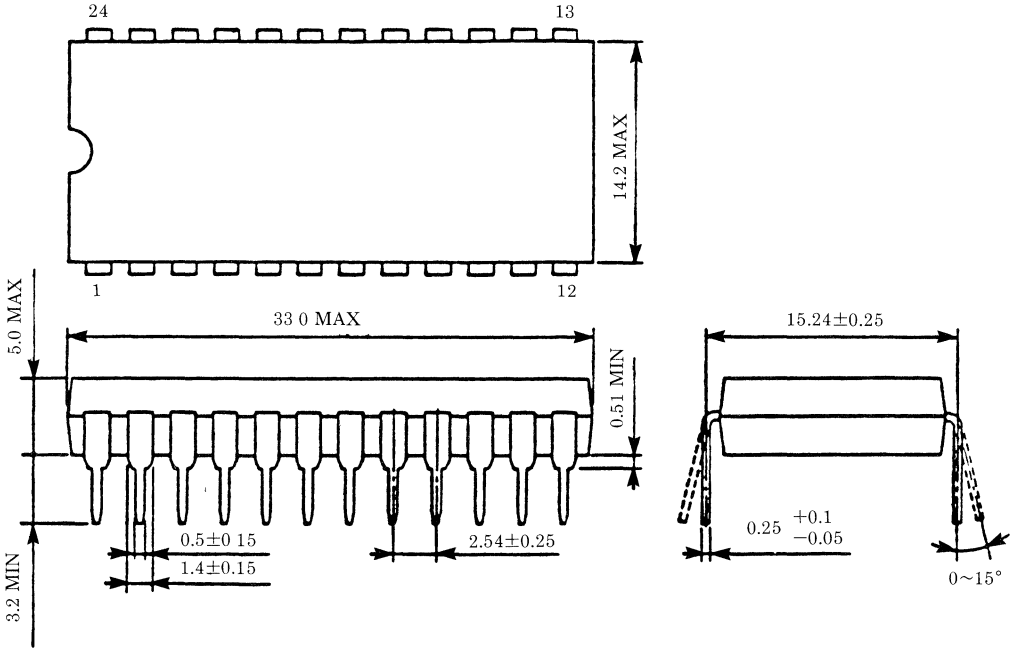
WRITE TIMING



CLOCK & GATE TIMING

PACKAGE OUTLINE
24 Pins PLASTIC DIP

Unit in mm



Note) Lead pitch is 2.54mm and tolerance is ±0.25mm against theoretical center of each lead that is obtained on the basis of No. 1 and No. 24 leads.

TLCS-Z80 CMOS FAMILY IN PLASTIC LEADED CHIP CARRIER.

TMPZ84C00AT/TMPZ84C00AT-6
TMPZ84C10AT/TMPZ84C10AT-6
TMPZ84C20AT/TMPZ84C20AT-6
TMPZ84C30AT/TMPZ84C30AT-6
TMPZ84C44AT/TMPZ84C44AT-6

These devices are CMOS Z-80 Family in 44 pin PLCC.

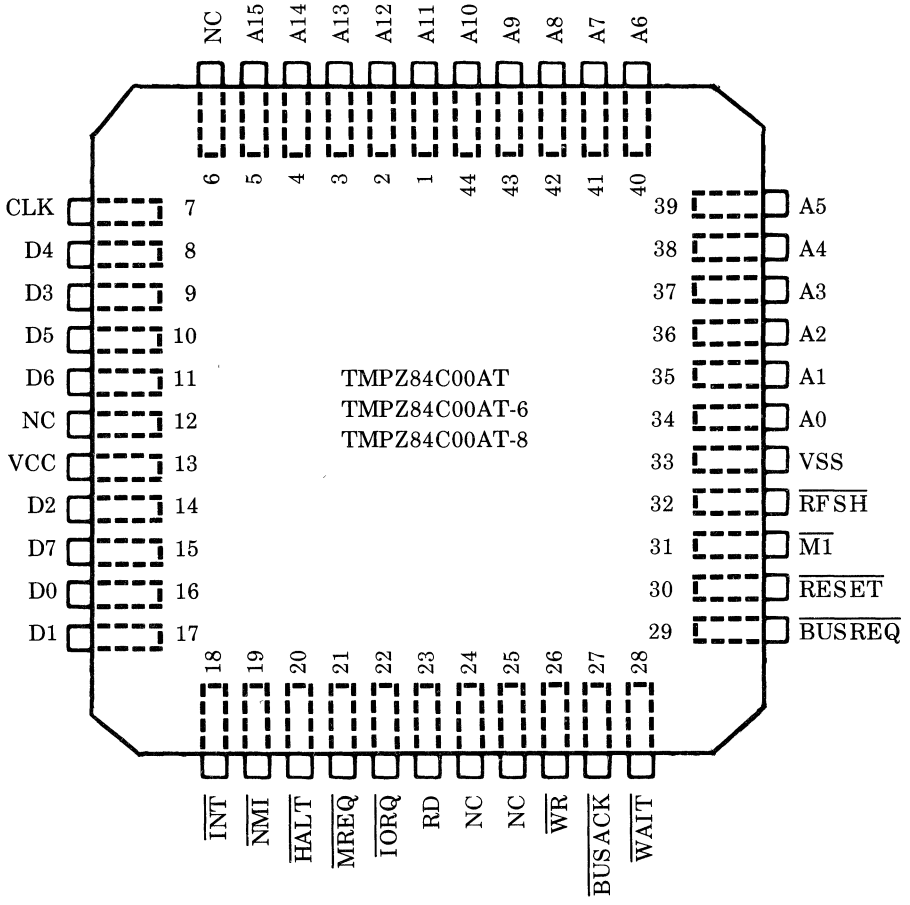
The function, A.C. and D.C. characteristics are same as in DIP or Flat Package.

REFERENCE TABLE

PART NUMBER	FUNCTION	CLOCK	REFERENCE
TMPZ84C00AT	Z80A CPU	4MHZ	TMPZ84C00AP
TMPZ84C10AT	Z80A DMA	4MHZ	TMPZ84C10AP
TMPZ84C20AT	Z80A PIO	4MHZ	TMPZ84C20AP
TMPZ84C30AT	Z80A CTC	4MHZ	TMPZ84C30AP
TMPZ84C44AT	Z80A SIO	4MHZ	TMPZ84C43AF
TMPZ84C00AT-6	Z80B CPU	6MHZ	TMPZ84C00AP-6
TMPZ84C10AT-6	Z80B DMA	6MHZ	TMPZ84C10AP-6
TMPZ84C20AT-6	Z80B PIO	6MHZ	TMPZ84C20AP-6
TMPZ84C30AT-6	Z80B CTC	6MHZ	TMPZ84C30AP-6
TMPZ84C44AT-6	Z80B SIO	6MHZ	TMPZ84C43AF-6

PIN CONNECTION
44-Pin PLCC Package

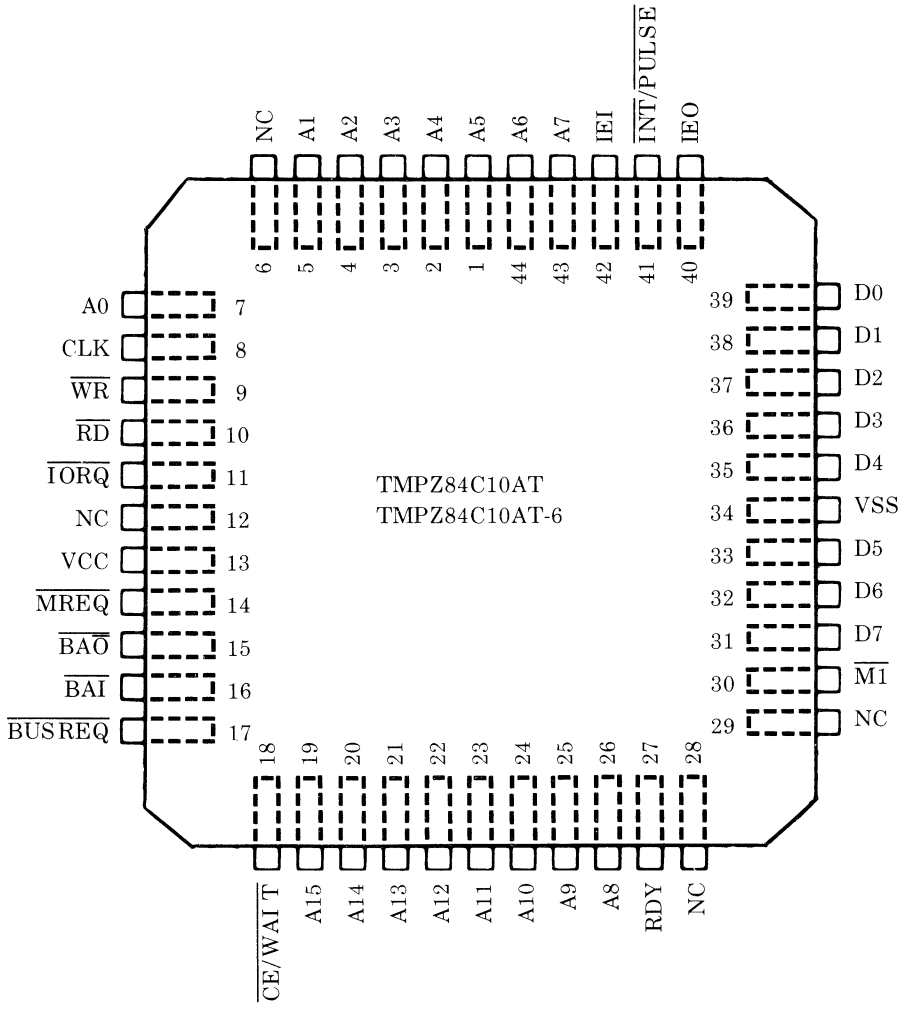
(TLCS-Z80 CPU)



PIN CONNECTION

44-Pin PLCC Package

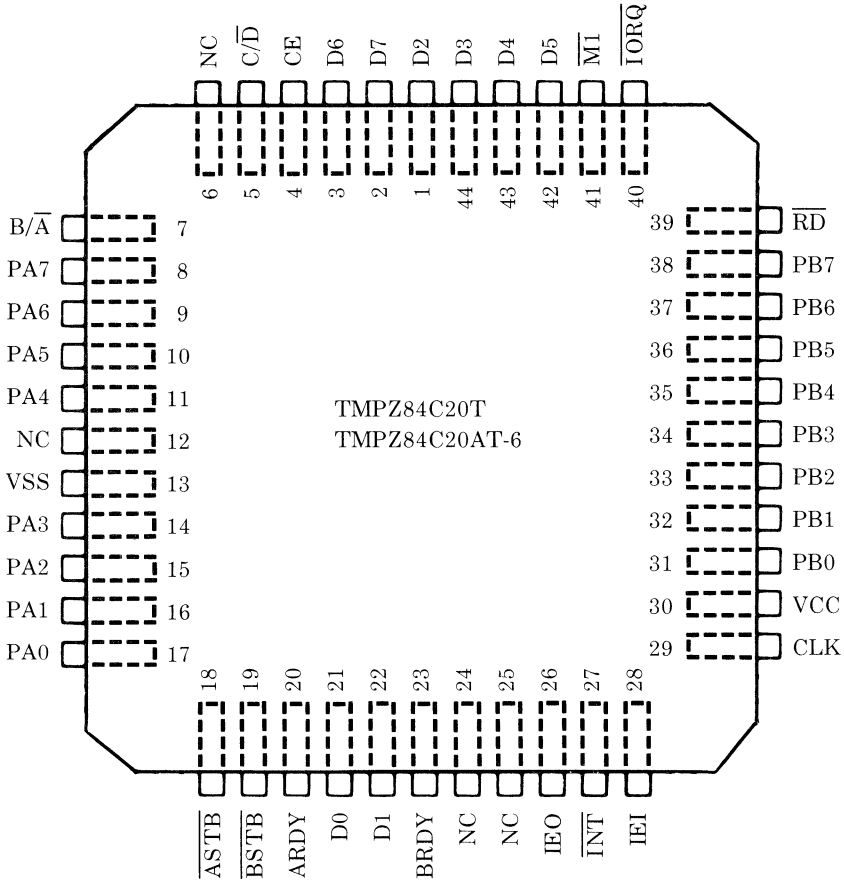
(TLCS-Z80 DMA)



PIN CONNECTION

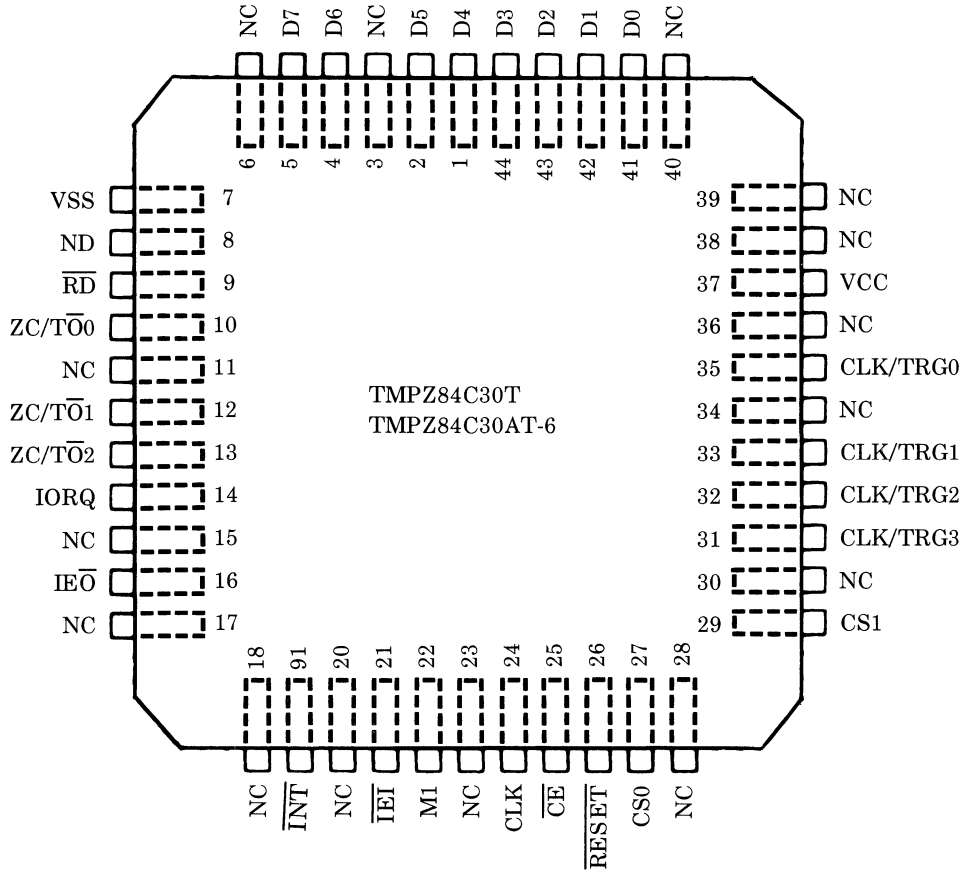
44-Pin PLCC Package

(TLCS-Z80 PIO)



PIN CONNECTION
44-Pin PLCC Package

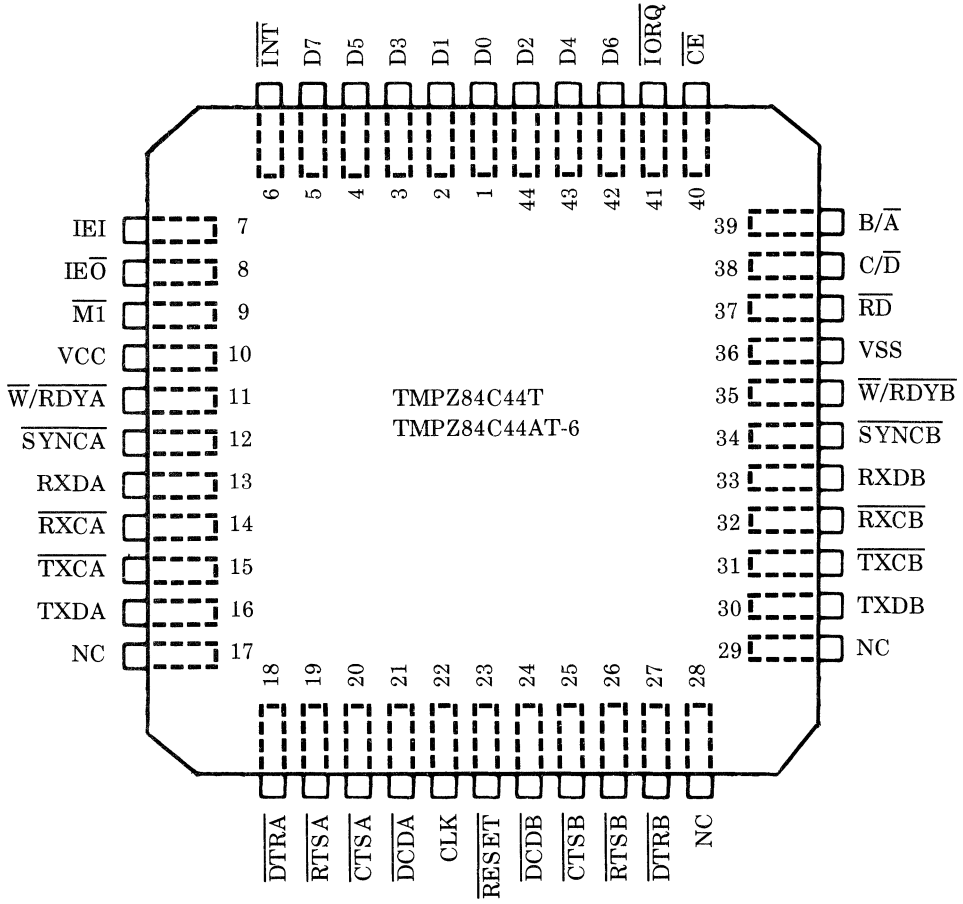
(TLCS-Z80 CTC)



PIN CONNECTION

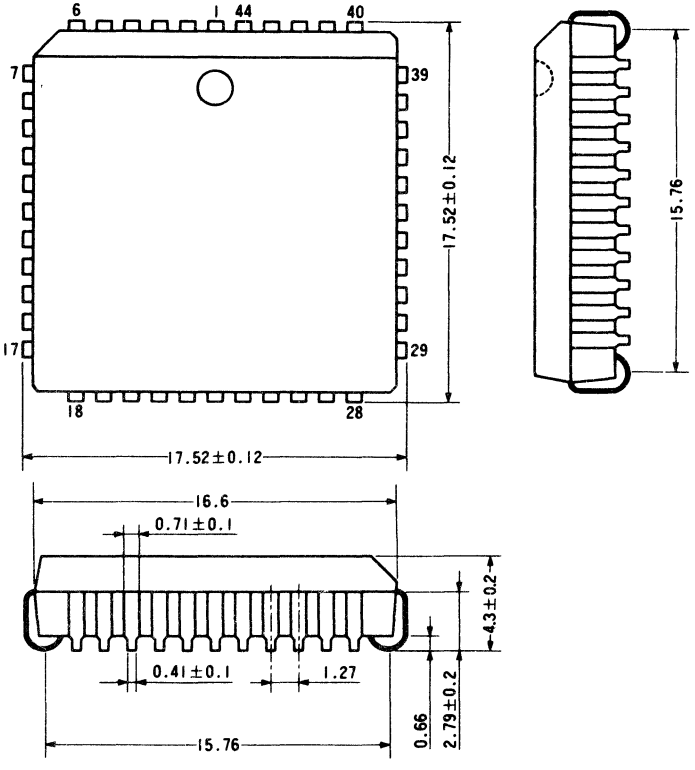
44-Pin PLCC Package

(TLCS-Z80 SIO)



PLASTIC LEADED CHIP CARRIER

44 Pin PLCC



TLCS-48 CMOS FAMILY IN PLASTIC LEADED CHIP CARRIER*

TMP80C48AT/TMP80C49AT/TMP80C50AT
TMP80C35AT/TMP80C39AT/TMP80C40AT

These devices are TLCS-48 Family in 44 pin PLCC.

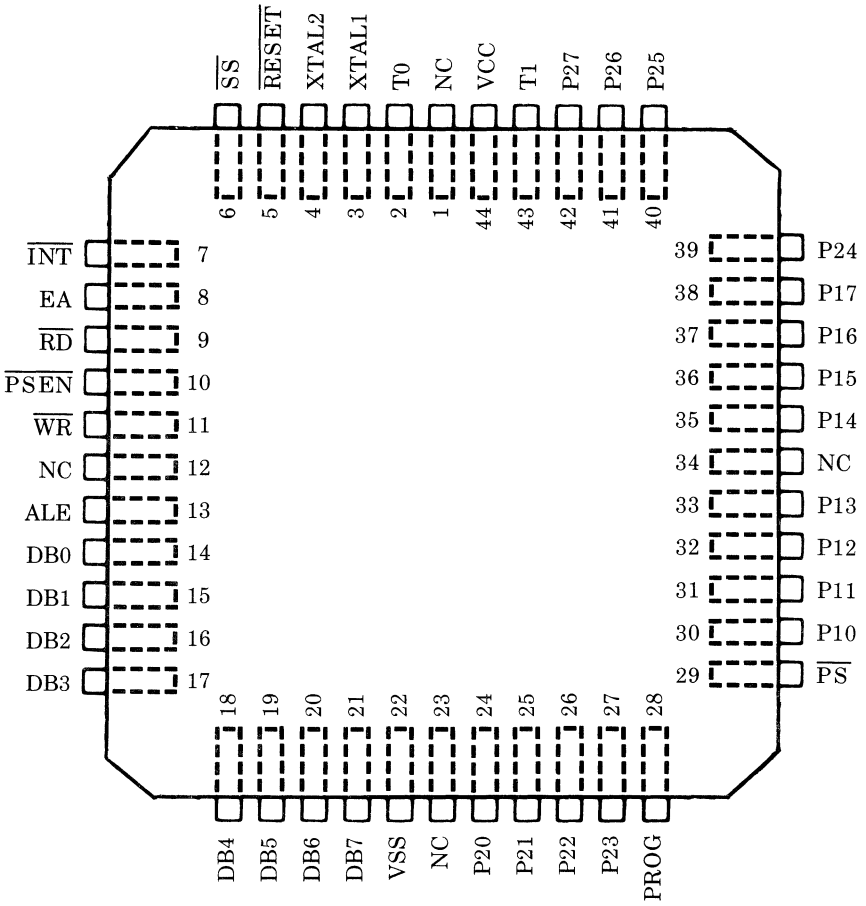
The function, AC and DC characteristics are same as in DIP or Flat Package.

REFERENCE TABLE

PART NUMBER	ROM	RAM	CLOCK (Mhz)	REFERENCE
TMP80C48AT	1k × 8	64 × 8	11	TMP80C48AP
TMP80C49AT	2k × 8	128 × 8	11	TMP80C49AP
TMP80C50AT	4k × 8	256 × 8	11	TMP80C50AP
TMP80C35AT	External	64 × 8	11	TMP80C35AP
TMP80C39AT	External	128 × 8	11	TMP80C39AP
TMP80C40AT	External	256 × 8	11	TMP80C40AP

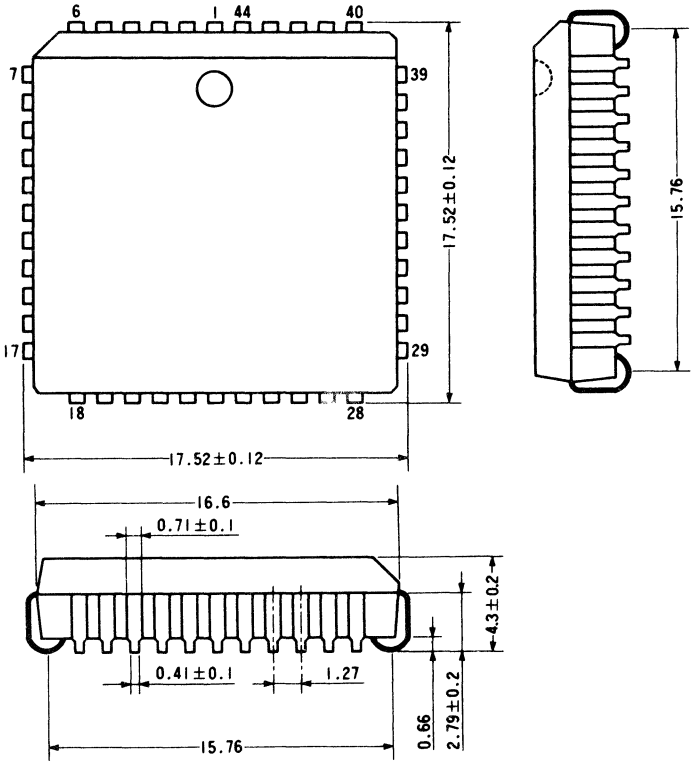
* See Page 597 for description of NMOS TLCS-48 Devices in PLCC.

PIN CONNECTIONS



PLASTIC LEADED CHIP CARRIER

44 Pin PLCC



VOL. 1. CORRECTIONS

PAGE	HEADING/SECTION/ TABLE/FIG./ADDITION	LINE/ FIGURE	CORRECTION	NOW READS
3	Feature / 1.1	9	$\overline{\text{NMI}}$	$\overline{\text{MMI}}$
201	General Description And Features	(15)	28 Pin	40 Pin
229	Fig. 2.2 (a) SIO Version	Fig. 2 & 3	SIO/1 & SIO/2	All Figures SIO/0
274	Fig. 2.1 Pin Connection	Pin Numbering	Pin No. (16-9) should read Top to Bottom	Currently reads (16-23) Top to Bottom
277	Table 3.1, T6497 Operation Modes	Column of MS	$\overline{\text{MS1}}$ | $\overline{\text{MS2}}$ 1 | 1 0 | * 1 | 0	$\overline{\text{MS2}}$ | $\overline{\text{MS2}}$ 1 | 1 0 | * 1 | 1
287	Additional Info.	—	C_L for any output is 100 pF	—
265	AC Electrical Characteristics	15	TdIEI (IEO r) 160 ns Max not Min.	160 Min.
221	Page Heading	Top Corner (right)	TMPZ84C30...	TMPZ84C40...
570	AC Electrical Characteristics	Table	tWW 160 tWD 30	tWW 140 tWD 10

VOL. 1. CORRECTIONS

Page: —639—, —663—, —687—,

Incorrect

tRD1	Data Input Read Time	($\overline{RD}$)		6t-170	-	375	ns
tRD2	Data Input Read Time	($\overline{PSEN}$)		4.5t-170	-	240	ns
tAD1	Address Setup Time	($\overline{RD}$)		10.5t-220	-	730	ns
tAD2	Address Setup Time	($\overline{PSEN}$)		7.5t-200	-	460	ns

Correct

tRD1	Data Input Read Time	($\overline{RD}$)		5.5t-120	-	375	ns
tRD2	Data Input Read Time	($\overline{PSEN}$)		4t-120	-	240	ns
tAD1	Address Setup Time	($\overline{RD}$)		10t-170	-	730	ns
tAD2	Address Setup Time	($\overline{PSEN}$)		7t-170	-	460	ns

Page: —643—, —667—, —691—,

Incorrect

tRD1	Data Input Read Time	($\overline{RD}$)		6t-170	-	830	ns
tRD2	Data Input Read Time	($\overline{PSEN}$)		4.5t-170	-	580	ns
tAD1	Address Setup Time	($\overline{RD}$)		10.5t-220	-	1530	ns
tAD2	Address Setup Time	($\overline{PSEN}$)		7.5t-200	-	1050	ns

Correct

tRD1	Data Input Read Time	($\overline{RD}$)		5.5t-120	-	800	ns
tRD2	Data Input Read Time	($\overline{PSEN}$)		4t-120	-	550	ns
tAD1	Address Setup Time	($\overline{RD}$)		10t-170	-	1500	ns
tAD2	Address Setup Time	($\overline{PSEN}$)		7t-170	-	1000	ns

MEMO

MEMO

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