UMC

T-52-33-61

UM8398

Single-Chip Floppy Disk Controller

Features

- IBM PC XT/AT drive system compatible
- Supports 2 drives (MS-DOS support)
- 1.2M/360K/720K format selectable
- IBM PC drive system address decoder
- Only 3 components for the drive
- Internal write precompensation circuit; precompensation values: 250-125 ns
- Internal data separator circuit
- Supports to control 8", 5¼", 3½" drives

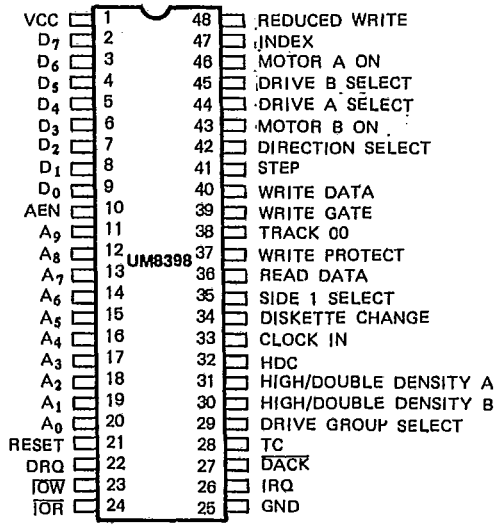
General Description

The UM8398 is a VLSI Floppy Disk Controller (FDC) chip, which contains the circuitry and control functions for interfacing a processor with up to 2 floppy disk drives. It is capable of supporting 360K Bytes, 1.2M Bytes (in 5¼" diskette drives), 720K Bytes, and 1.44M Bytes, (in 3½" diskette drives) FDDs using FM/MFM-coded, and double sided recording. UM8398 includes an internal data separator, write precompensation, circuit address decoder, timing control and other control logics. It simplifies design of a diskette drive system since only 3 components are needed in the IBM PC XT/AT drive system.

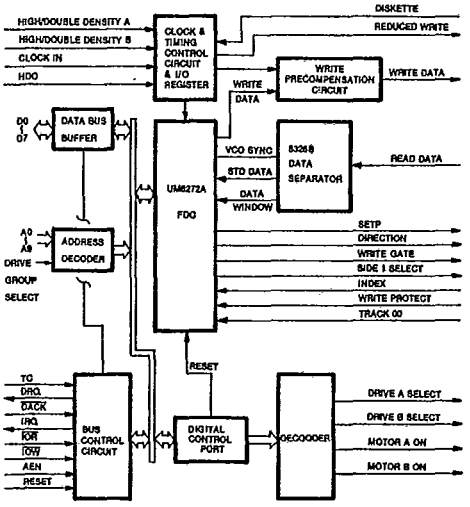
Handshaking signals are provided in UM8398 which makes DMA operation easy to incorporate with the aid of an external DMA control chip. The FDC will operate in either the DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor every time a data byte is available. In the DMA mode, the processor needs only to load the command into the FDC and all data transfers occur under control of the UM8398 and DMA controller.

Many diskette drive parameters are programmable and write-protection feature is supported. One interrupt level is used to indicate when an operation is completed, or a status condition requires microprocessor's attention.

Pin Configurations

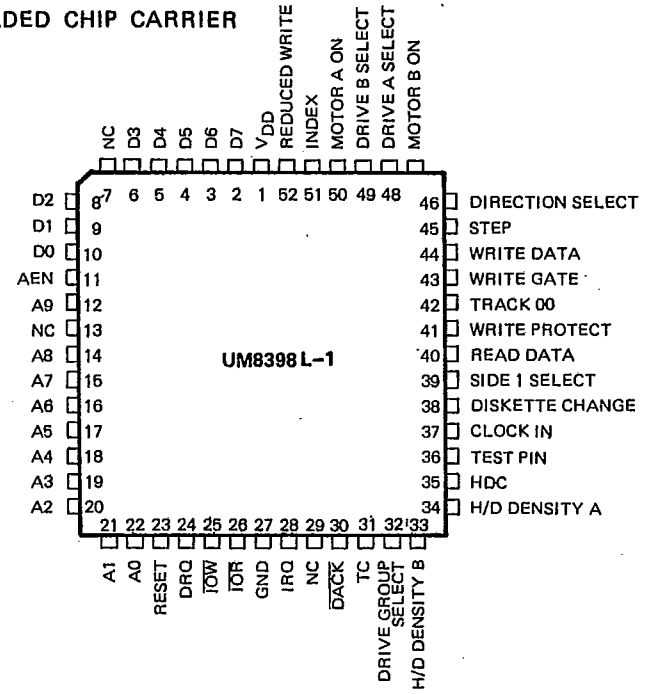


Block Diagram

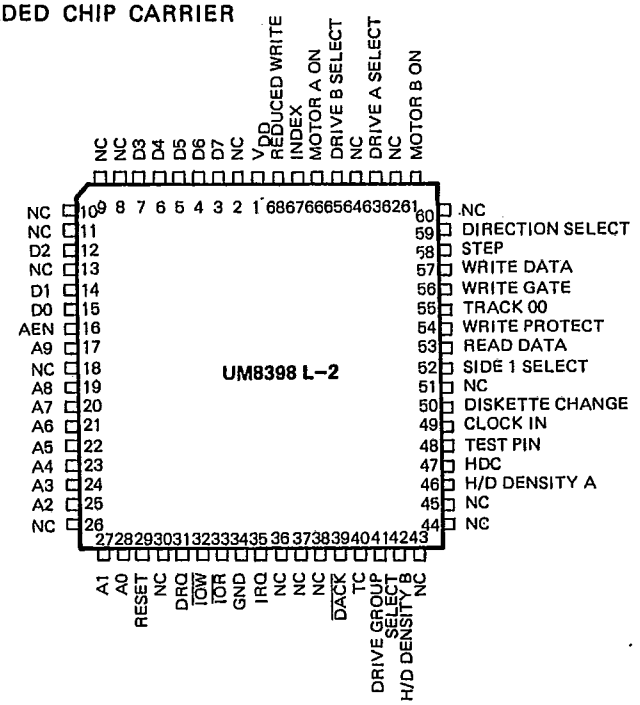


Pin Configurations (Continued)

52 PIN PLASTIC LEADED CHIP CARRIER



68 PIN PLASTIC LEADED CHIP CARRIER



Storage

Absolute Maximum Ratings*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −55°C to +150°C
All Output Voltages . . . . . −0.5 to +7 Volts
All Input Voltages . . . . . −0.5 to +7 Volts
Supply Voltage V_{CC} . . . . . −0.5 to +7 Volts
Power Dissipation . . . . . 1 Watt

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to +70°C, V_{CC} = +5V ± 5%)

Symbol	Parameters	Limits		Unit	Test Conditions
		Min.	Max.		
V_{IL}	Input low voltage		0.8	V	
V_{IH}	Input high voltage	2.0		V	
V_{OL}	Output low voltage		0.4	V	I_{OL} = 2.0mA
V_{OH}	Output high voltage	2.4	V_{CC}	V	I_{OH} = 400μA
I_{CC}	V_{CC} supply current		200	mA	
I_{IL}	Input leakage current		10	μA	$0 \leq V_O \leq V_{CC}$
I_{LOH}	High level output leakage current		10	μA	$V_O = V_{CC}$
I_{OFL}	Output float leakage current		10	μA	$0.4V \leq V_O \leq V_{CC}$

A.C. Characteristics (T_A = 0°C to + 70°C, V_{CC} = +5.0V ± 10%)

PROCESSOR WRITE CYCLE

Symbol	Parameter	Min.	Max.
t_{AW}	address setup to $\overline{IOW}$ ↓	0 ns	
t_{WA}	address hold from $\overline{IOW}$ ↑	0 ns	
t_{WW}	$\overline{IOW}$ pulse width	250 ns	
t_{DW}	data setup to $\overline{IOW}$ ↑	150 ns	
t_{WD}	data hold from $\overline{IOW}$ ↑	10 ns	
t_{WI}	IRQ delay from $\overline{IOW}$ ↑		500 ns*

PROCESSOR READ CYCLE

Symbol	Parameter	Min.	Max.
t_{AR}	address setup to $\overline{IOR}$ ↓	0 ns	
t_{RA}	address hold from $\overline{IOR}$ ↑	0 ns	
t_{RR}	$\overline{IOR}$ pulse width	250 ns	
t_{RD}	data delay from $\overline{IOR}$ ↓		230 ns
t_{DF}	output floating delay from $\overline{IOR}$ ↑	10 ns	30 ns
t_{RI}	IRQ6 delay from $\overline{IOR}$ ↑		500 ns*

Note: *: The values are for 8 MHz clock rate, multiply timings by 2/1.67 when using 4/4.8 MHz clock rates.

DMA OPERATION*

Symbol	Parameter	Min.	Max.
t_{ROCY}	DRQ cycle period	13 μs	
t_{AKRO}	$\overline{DACK}$ ↓ to DRQ ↓		200 ns
t_{ROR}	DRQ ↑ to $\overline{IOR}$ ↓	800 ns	
t_{ROW}	DRQ ↑ to $\overline{IOW}$ ↓	250 ns	
t_{RORW}	DRQ ↑ to $\overline{IOR}$ ↑ or $\overline{IOW}$ ↑		12 μs

Symbol	Parameter	Min.	Typ.	Max.
t_{IDX}	index pulse width		$10t_{CY}$**	
t_{TC}	terminal count width	$1t_{CY}$		
t_{RST}	reset width	$14t_{CY}$		

Notes:
* : The values listed for DMA operation are for 8 MHz clock rate, multiply timings by 2/1.67 when using 4/4.8 MHz clock rates.
**: t_{CY} is the clock rate of Drive System.

FDD INTERFACE

Symbol	Parameter	Min.	Typ.	Max.
t_{WGD}	write gate active before the first significant data bit	4 μs		8 μs
t_{WDG}	write gate inactive after the last significant data bit	4 μs		8 μs
t_{WDD}	write data width	t_{WCH}−50ns**	125/208/250 ns*	
t_{WCY}	write data cycle time		1/1.67/2 μs*	
t_{RDD}	read data active time (high)	40 ns	125/208/250 ns*	
t_{RCY}	read data cycle time		1/1.67/2 μs*	

Storage

SEEK OPERATION***

Symbol	Parameter	Min.	Typ.	Max.
t_{DU}	$US_{A,B}$ hold from DIR	45 μs		
t_{UD}	$US_{A,B}$ setup to DIR	24 μs		
t_{STP}	step active time		5 μs	
t_{SC}	step cycle time	33 μs		
t_{DST}	DIR setup to step ↑	1 μs		
t_{STD}	DIR hold from step ↓	24 μs		

Notes:
* : The specified values are for 8/4.8/4 MHz respectively.
** : t_{WCH} – write clock high time.
***: The values listed for seek operation are for 8 MHz clock period, multiply timings by 2/1.67 when using 4/4.8 MHz clock rates.

Pin Description

Pin	Symbol	I/O	Description
1	V_{CC}	I	Power supply. Connected to +5V power supply.
2~9	$D_7 \sim D_0$	I/O	Bi-directional 8-bit data bus
10	AEN	I	Input from DMA – Address Enable. When this line is active, the DMA controller has control of the address bus.
11~20	$A_9 \sim A_0$	I	Input from processor – 10-bit Address Bus.
21	RESET	I	Input from processor – places FDC in idle state. Reset output lines to FDD to "0" (low). Does not affect SRT, HUT or HLT in Specify command. If RDY pin is held high during Reset, FDC will generate interrupt 1.024 ms later. To clear thisinterrupt,use Sense Interrupt Status command.
22	DRQ	O	Output to DMA – DMA Request is being made by FDC when DRQ 2 = "1".
23	$\overline{IOW}$	I	Input from processor – Control signal for transfer of data to FDC via Data Bus, when "0".
24	$\overline{IOR}$	I	Input from processor – Control signal for transfer of data from FDC to Data Bus, when "0".
25	GND	I	Ground. Normally connected to +0V ground
26	IRQ	O	Output to processor – Interrupt request generated by FDC.
27	$\overline{DACK}$	I	Input from DMA – DMA cycle is active when "0" (low) and controller is performing DMA transfer.
28	TC	I	Input from DMA – Indicates the termination of a DMA transfer when "1" (high). It terminates data transfer during Read/Write/Scan command in DMA or interrupt mode.
29	DRIVE GROUP SELECT	I	The primary address will be applied when this signal is active high.
30	HIGH/DOUBLE DENSITY B	I	Drive B high or double density diskette drive selection. When drive B is high density, set this input to high.
31	HIGH/DOUBLE DENSITY A	I	Drive A high or double density diskette drive format selection. When drive A is high density, set this input to high.
32	HDC	I	Set this input to low, when your system has hard disk control card. Otherwise, set this input to high.
33	CLOCK IN	I	24 MHz clock input.
34	DISKETTE CHANGE	I	Input from FDD – This input is high when a diskette is present and a step pulse is received when the drive is selected.

Pin Description (Continued)

Pin	Symbol	I/O	Description
35	SIDE 1 SELECT	O	Output to FDD — This output is active (high) for the upper head. Otherwise, the lower head is selected.
36	READ DATA	I	Input from FDD — Each bit detected provides a 250 ns (4 MHz), 208 ns (4.8 MHz), 150 ns (8 MHz) active (low) pulse on this line.
37	WRITE PROTECT	I	Input from FDD — This input is active low when a diskette with a write protect notch is inserted.
38	TRACK 00	I	Input from FDD — This signal is low when the upper head is on Track 00 (the outermost track).
39	WRITE GATE	O	Output to FDD — An active level of this input enables the write current circuits, and the Write Data input controls the writing of information.
40	WRITE DATA	O	Output to FDD — A 150 ns (8 MHz), 208 ns (4.8 MHz), 250 ns (4 MHz) pulse on this output causes a bit to be written on the disk if Write Gate is active. When Write Gate is inactive, pulses do not appear on this output.
41	STEP	O	Output to FDD — An active pulse causes the read/write heads to move in the direction determined by the "direction select" signal. Motion is started each time the signal changes from an active to inactive level (at the trailing edge of the pulse).
42	DIRECTION SELECT	O	Output to FDD — This signal determines the direction the read/write head moves when the step signal is pulsed. An active level indicates away from the center of the diskette (out); an inactive level indicates toward the center of the diskette (in).
43	MOTOR B ON	O	Output to FDD — The spindle motor B runs when this input is active. The drive requires a 1 sec (high density)/750 ms (double density) delay after "motor on" becomes active before and after the trailing edge of the step pulse.
44	DRIVE A SELECT	O	Output to FDD — When "Drive A Select" is at the active level, drive A is enabled. When it is at the inactive level, all drive A outputs are disabled.
45	DRIVE B SELECT	O	Output to FDD — When "Drive B Select" is at the active level, drive B is enabled. When it is at the inactive level, all drive B outputs are disabled.
46	MOTOR A ON	O	Output to FDD — The spindle motor A runs when this input is active. Drive A requires a 1 sec (high density)/750 ms (double density) delay after "motor on" becomes active before and after the trailing edge of the read or write operation.
47	INDEX	I	Input from FDD — A pulse appears on this line to indicate the beginning of a disk track when the drive senses the index hole in the diskette.
48	REDUCED WRITE	O	Output to FDD — The inactive state of this signal indicates that high-density media is present, requiring normal write currents, and the active state indicates low-density media is present, requiring a reduced write current.

Register Description

1. Digital Output Register

The digital output register (DOR) is an output-only register controlling drive motors, drive selection, and feature enable. All bits are cleared by the I/O interface reset line. The bit definitions are as follows.

Bit 7	Reserved
Bit 6	Reserved
Bit 5	Drive B Motor Enable
Bit 4	Drive A Motor Enable
Bit 3	Enable Diskette Interrupts and DMA
Bit 2	Diskette Function Reset – Diskette function reset when this bit is low ('0').
Bit 1	Reserved
Bit 0	Drive Select – A "0" on this bit indicates that drive A is selected.

2. Digital Input Register

The digital input register is an 8-bit, read-only register used for diagnostic purposes. The following are bit definitions for this register.

Bit 7	Diskette Change
Bit 0~6	Apply to the currently selected fixed disk drive

3. Transfer Rate Register (Diskette Control Register)

The transfer rate register is a 2-bit, output-only register which controls a programmable divider and provides 8M/4.8M/4M Hz clocks for three different data transfer rates. The definition is given as follows:

Bit 0	Bit 1	Transfer Rates	Clock Rates
0	0	500K bps	8 MHz
1	0	300K bps	4.8 MHz
0	1	250K bps	4 MHz
1	1	reserved	reserved

4. Main Status Register

Those bits in the main status register are defined as follows:

Bit 7	Request for master (RQM) – The data register is ready to send or receive data to or from the processor.
Bit 6	Data Input/Output (DIO) – The direction of data transfer between the diskette control and the processor.
Bit 5	Non-DMA Mode (NDM) – The diskette controller is in the non-DMA mode.
Bit 4	Diskette Control Busy (CB) – A Read or Write command is being executed.
Bit 3	Reserved
Bit 2	Reserved
Bit 1	Diskette Drive B Busy (DBB) – Diskette drive B is in the seek mode.
Bit 0	Diskette Drive A Busy (DAB) – Diskette drive A is in the seek mode.

5. Diskette Data Register

This 8-bit data register actually consists of several registers in a stack and only one register is presented to the data bus at a time when storing data commands, and parameters, or providing diskette-drive status information.

6. Drive Type Register

The drive type register is a 4-bit read-only register for drive type settings. This register is used only when FDC control ROM is at ON condition. The bit definitions are given in the following:

Bit 0	Drive A Type – Drive A is double density when this bit is '0' and high density when this bit is '1'.
Bit 1	Drive B Type – Drive B is double density when this bit is '0' and high density when this bit is '1'.
Bit 2	Ground 0 (Low)
Bit 3	Ground 0 (Low)

7. Fixed Disk Status Register

The contents of this 8-bit fixed disk status register is checked when system BIOS executes self-test. This register is enabled when PC system has no Hard Disk Control card and bit 7 is of this register is fixed to 1 (high). This register shall be disabled when PC system has a Hard Disk Control card.

The I/O addresses of these seven registers mentioned above are given in the following:

Primary	Secondary	Read	Write
3F1	371	Drive type register	
3F2	372		Digital output register
3F4	374	Main status register	Main status register
3F5	375	Diskette data register	Diskette data register
3F7	377	Digital input register	Transfer rate register
1F7	177	Fixed Disk Status register*	

*: Fixed disk function

Command Descriptions

There are 15 separate commands which the UM8398 will execute. Each of these commands requires multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

READ DATA
FORMAT A TRACK
SCAN EQUAL
SCAN LOW OR EQUAL
SCAN HIGH OR EQUAL
RECALIBRATE
READ ID
INVALID
SENSE INTERRUPT STATUS
SPECIFY
SENSE DRIVE STATUS
SEEK
READ DELETED DATA
WRITE DELETED DATA
READ A TRACK

The format of these commands is the same as UM8272A. The UM8398 also has two registers to which the main system processor has access: a status register and a data register just the same as UM8272A. The track stepping rate, head load time, and head unload time may be programmed by the user. The UM8398 offers many additional features such as multiple sector transfers in both read and write with a single command, and full IBM PC XT/AT compatibility in both double and high density models.

Command Symbol Description

Symbol	Name	Description
A_0	Address Line 0	A_0 controls selection of Main Status Register (A_0 = 0) or Data Register (A_0 = 1).
C	Cylinder Number	C stands for the current/selected Cylinder (track) number 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a sector.
D_7-D_0	Data Bus	8-bit Data Bus, where D_7 stands for the most significant bit, and D_0 stands for the least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector.
EOT	End of Track	EOT stands for the final Sector number on a Cylinder. During Read or Write operation FDC will stop data transfer after a sector # equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During Read/Write commands this value determines the number of bytes that VCOs will stay low after two CRC bytes. During Format command it determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. If MT = 1 after finishing Read/Write operation on side 0 FDC will automatically start searching for sector 1 on side 1.
N	Number	N stands for the number of data bytes written in Sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R stands for the Sector number, which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD. (1 to 16 ms in 1 ms increments.) Stepping Rate applies to all drives, (F = 1 ms, E = 2 ms, etc.)
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stands for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A_0 = 0); ST 0-3 may be read only after a command has been executed and contains information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive number 0 or 1.

Table 1. UM8398 Command Set

Phase	R/W	Databus D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Remarks
READ DATA			
Command	W	MT MF SK 0 0 1 1 0	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior to Command execution.
	W	H	
	W	R	
	W	N	
	W	EOT	The 4 bytes are commanded against header on Floppy Disk.
	W	GPL	
	W	DTL	
Execution			Data-transfer between the FDD and main system.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	
READ DELETED DATA			
Command	W	MT MF SK 0 1 1 0 0	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior to Command execution.
	W	H	
	W	R	
	W	N	
	W	EOT	The 4 bytes are commanded against header on Floppy Disk.
	W	GPL	
	W	DTL	
Execution			Data-transfer between the FDD and main system.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	
WRITE DATA			
Command	W	MT MF 0 0 0 1 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior to Command execution.
	W	H	
	W	R	
	W	N	
	W	EOT	The 4 bytes are commanded against header on Floppy Disk.
	W	GPL	
	W	DTL	
Execution			Data-transfer between the FDD and main system.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	
WRITE DELETED DATA			
Command	W	MT MF 0 0 1 0 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior to Command execution.
	W	H	
	W	R	
	W	N	
	W	EOT	The 4 bytes are commanded against header on Floppy Disk.
	W	GPL	
	W	DTL	
Execution			Data-transfer between the FDD and main system.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	

Phase	R/W	Databus D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Remarks
READ A TRACK			
Command	W	0 MF SK 0 0 0 1 0	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior to Command execution.
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	DTL	
Execution			Data-transfer between the FDD and mainsystem. FDC reads all data fields from index hole to EOT.
Result	R	ST 0	Status information after Command execution
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	
READ ID			
Command	W	0 MF 0 0 1 0 1 0	Command Codes
	W	X X X X X HD US1 US0	
Execution			The first correct ID information on the Cylinder is stored in Data Register.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information read during Execution Phase from Floppy Disk.
	R	H	
	R	R	
	R	N	
FORMAT A TRACK			
Command	W	0 MF 0 0 1 1 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	N	Bytes/Sector
	W	SC	Sectors/Track
	W	GPL	Gap 3
	W	D	Filer Byte
Execution			FDC formats an entire track
Result	R	ST 0	Status information after Command execution In this case, the ID information has no meaning.
	R	ST 1	
	R	ST 2	
	R	C	
	R	H	
	R	R	
	R	N	
SCAN EQUAL			
Command	W	MT MF SK 1 0 0 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information Prior to Command execution.
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data-compared between the FDD and main-system.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	

Note: 1 A_0 should equal binary 1 for all operations.
2 X = Don't care, usually made to equal binary 0.

Storage

Table 1. UM8398 Command Set (Continued)

Phase	R/W	Databus D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Remarks
SCAN LOW OR EQUAL			
Command	W	MT MF SK 1 1 0 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior Command execution.
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data-compared between the FDD and main-system.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	
SCAN HIGH OR EQUAL			
Command	W	MT MF SK 1 1 1 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior Command execution.
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data-compared between the FDD and main-system.
Result	R	ST 0	Status information after Command execution.
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution.
	R	H	
	R	R	
	R	N	

Phase	R/W	Databus D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Remarks
RECALIBRATE			
Command	W	0 0 0 0 0 1 1 1	Command Codes
Execution	W	X X X X X HD US1 US0	Head retracted to Track 0
SENSE INTERRUPT STATUS			
Command	W	0 0 0 0 1 0 0 0	Command Codes
Result	R	ST 0	Status information at the end of seek-operation about the FDC.
	R	PCN	
SPECIFY			
Command	W	0 0 0 0 0 0 1 1	Command Codes
	W	SRT HUT	
	W	HLT ND	
SENSE DRIVE STATUS			
Command	W	0 0 0 0 0 1 0 0	Command Codes
	W	X X X X X HD US1 US0	
Result	R	ST 3	Status information about FDD
SEEK			
Command	W	0 0 0 0 1 1 1 1	Command Codes
	W	X X X X X HD US1 US0	
	W	NCN	
Execution			Head is positioned over proper Cylinder on Diskette
INVALID			
Command	W	Invalid Codes	Invalid Command Codes (NoOP – FDC goes into Standby State)
Result	R	ST 0	ST 0 = 80 (16)

Read Data

A set of nine (9) byte words is required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head setting time (defined in the Specify Command), and begins reading ID address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the Data field) byte-by-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command must be terminated by the receipt of a Terminal Count signal. Upon receipt of this signal, the FDC stops outputting data to the processor, while continuing read data from the current sector, checking CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector. It will terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MFM (MFM/FM), and N (Number of Bytes/Sector). Table 2 on the next page shows the Transfer Capacity. The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to 0FFH.

At the completion of the Read Data Command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head setting time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another. If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the Status Register 1's ND (No Data) flag to 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the Status

Register 1's DE (Data Error) flag to 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the Status Register 2's DD (Data Error in Data Field) flag to 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the Status Register 2's CM (Control Mark) flag to 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be served by the processor every 27 μs in the FM Mode, and every 13 μs in the MFM Mode, or the FDC sets the Status Register 1's OR (Over Run) flag to 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 3 shows the values for C, H, R, and N, when the processor terminates the Command.

Table 2. Transfer Capacity

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

Table 3. ID Information When Processor Terminates Command

MT	EOT	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	1A	Sector 1 to 25 at Side 0	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	C + 1	NC	R = 01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C + 1	NC	R = 01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				
1	1A	Sector 1 to 25 at Side 0	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	NC	LSB	R = 01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C + 1	LSB	R = 01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				

Note: 1. NC (No Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

Write Data

A set of nine (9) bytes is required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified, head settling time (defined in the Specify Command), and begins reading ID Fields. When the current sector number ("R"), stored in the ID Register. (IDR) compares with the sector number read off the diskette, then the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD. After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count-signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (Incorrect CRC) in one of the ID Fields, it sets the Status Register 1's DE (Data Error) flag to 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The Following items are the same; refer to the Read Data Command for details.

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command.
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC must occur every 31 μs in the FM mode, and every 15 μs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the Status Register 1's OR (Over Run) flag to 1 (high), and terminates the Write Data Command.

For Mini-floppies, multiple track writes are usually not permitted. This is because of the turn-off time of the erase head coils — the head switches tracks before the erase head turns off. Therefore the system should typically wait 1.3 ms before attempting to step or change sides.

Write Deleted Data

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

Read Deleted Data

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field and SK = 0 (low), it will read all the data in the sector and set the Status Register 2's CM flag to 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

Read A Track

This command is similar to READ DATA Command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering the INDEX HOLE the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the Status Register 1's ND flag to 1 (high) if there is no comparison. unloaded state), waits the specified, head, setting time in the ID Register. (IDR) compares with the sector.

This command terminates when EOT number of sectors have been read. If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, then it sets the Status Register 1's MA (missing address mark) flag to 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

Read ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID Field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the Status Register 1's MA (Missing Address Mark) flag is set to 1 (high), and if no data is found then the Status Register 1's ND (No Data) flag is also set to 1 (high), and the command is terminated.

Format A Track

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette: Gaps, Address Marks, ID Fields and Data Fields, all as per the IBM System 34 (Double Density), or System 3740 (Single Density). The Format is recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor, thus is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

After formatting each sector, the processor must send new values for C, H, R, and N to the UM8398 for each sector on the track. The content of the R Register is incremented by one after each sector is formatted, thus, the R register contains a value of R + 1 when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the Status Register 0's EC flag to 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes command termination.

Table 4 shows the relationship between N, SC, and GPL for various sector sizes:

Table 4. Sector Size Relationships

Format	Sector Size	N	SC	GPL[1]	GPL[2,3]
8" Standard Floppy					
FM Mode	128 bytes/sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode[4]	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5¼" Minifloppy					
FM Mode	128 bytes/sector	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode[4]	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3½" Sony Micro Floppydisk"					
FM Mode	128 bytes/sector	0	0F	07	1B
	256	1	09	0E	2A
	512	2	05	1B	3A
MFM Mode[4]	256	1	0F	0E	36
	512	2	09	1B	54
	1024	3	05	35	74

Notes:
1. Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections.
2. Suggested values of GPL in format command.
3. All values except sector size are hex(decimal.
4. In MFM mode FDC cannot perform a Read/Write/format operation with 128 bytes/sector. (N = 00).

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel Seek operations may be done on up to 2 Drives at once.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the Seek operation, then the Status Register 0's NR (NOT READY) flag is set to 1 (high), and the command is terminated.

Note that the UM8398 Read and Write Commands do not have implied Seeks. Any R/W command should be preceded by: 1) Seek Command; 2) Sense Interrupt Status, and 3) Read ID.

Recalibrate

This command causes the read/write head within the FDD to retract to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 1 (high) and Step Pulses are issued. When the Track 0 signal goes high, the Status Register 0's SE (SEEK END) flag is set to 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulses have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command.

The ability to overlap RECALIBRATE Commands to multiple FDDs, and the loss of the READY signal, as described in the SEEK Command, also applies to the RECALIBRATE Command.

Sense Interrupt Status

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during

normal command operations and are easily discernbile by the processor. However, interrupts caused by reasons 2 and 3 may be uniquely identified with the aid of the Sense Interrupt Status Command. This command when issued, resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

Neither the Seek nor Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of the head position (PCN).

Table 5. Seek, Interrupt Codes

Seek End Bit 5	Interrupt Code		Cause
	Bit 6	Bit 7	
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

Specify

The Specify Command sets the intial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms . . . 0F = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms. . . . FE = 254 ms).

The step rate should be programmed 1 ms longer than the minimum time required by the drive.

The time intervals mentioned above are a direct function of the clock. Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

Sense Drive Status

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information.

Invalid

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command. No interrupt is generated by the UM8398 during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the UM8398 is in the Result Phase and the contents of Status Register 0 (ST0) must be read. When the processor reads Status Register 0 it will find an 80H Indicating an invalid command was received.

A Sense interrupt Status Command must be sent after a Seek or Recalibrate interrupt, otherwise the FDC will consider the next command to be an invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

Table 6. Status Register

Bit No.	Bit Name	Bit Symbol	Description
STATUS REGISTER 0			
D_7	Interrupt Code	IC	D_7 = 0 and D_6 = 0 Normal Termination of Command, (NT). Command was completed and properly executed.
D_6			D_7 = 0 and D_6 = 1 Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.

Bit No.	Bit Name	Bit Symbol	Description
STATUS REGISTER 0 (CONT.)			
D_6			D_7 = 1 and D_6 = 0 Invalid Command Issue, (IC). Command which was issued was never started.
			D_7 = 1 and D_6 = 1 Abnormal Termination because during command execution the ready signal from FDD changed state.

Table 6. Status Registers (Continued)

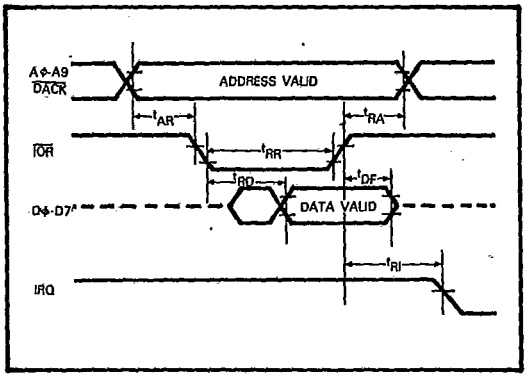
Bit No.	Bit Name	Bit Symbol	Description
STATUS REGISTER 0 (CONT.)			
D_6	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault signal is received from the FDD, or if the Track 0 signal falls to occur after 77 Step Pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US 1	These flags are used to indicate a Drive Unit Number at Interrupt
D_0	Unit Select 0	US 0	
STATUS REGISTER 1			
D_7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D_4	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.
D_1	Not Writable	NW	During execution of WRITE DATA WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the Index hole twice, then this flag is set.

Bit No.	Bit Name	Bit Symbol	Description
STATUS REGISTER 1 (CONT.)			
D_0	Missing Address Mark	MA	If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
STATUS REGISTER 2			
D_7			Not used. This bit is always 0 (low.)
D_6	Control Mark	CM	During executing the READ DATA or SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detect a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related with the ND bit. and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During executing the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
STATUS REGISTER 3			
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RDY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D_1	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD
D_0	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD

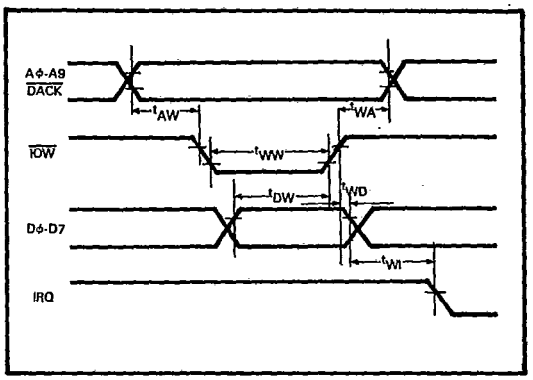
Storage

Timing Waveforms

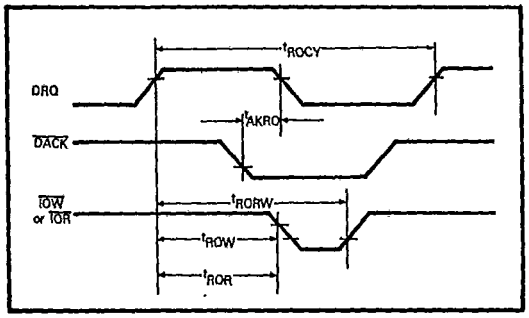
Processor Read Operation



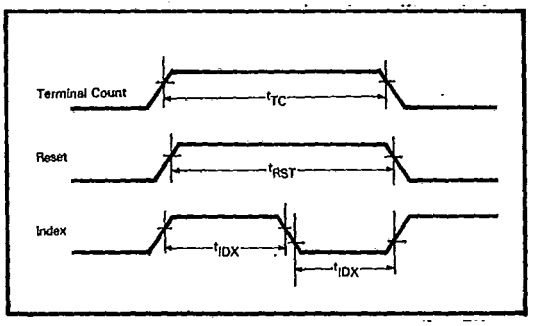
Processor Write Operation



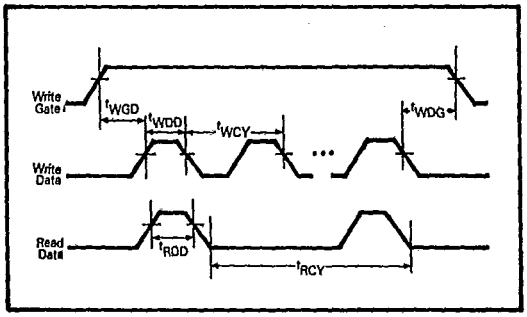
DMA Operation



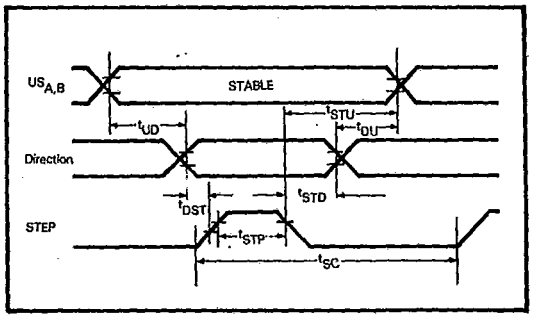
Terminal Count, Reset, Index



FDD Write/Read Operation



Seek Operation



Application Notes

A: General Description

The UM8398 is a VLSI Floppy Disk Controller (FDC) chip, which contains the circuitry and control functions for interfacing a processor up to 2 Floppy Disk Drives. It is capable of supporting 360K Bytes, 1.2M Bytes (in 5¼" diskette drives), 720K Bytes, and 1.44M Bytes (in 3½" diskette drives) FDDs using FM/MFM-coded, double sided recording. The UM8398 provides all the functions of the UM8272A, internal data separator (UM8326B), write precompensation circuit, address decoder, clock & timing control circuit, and other control logic. Therefore, it is very easy to implement into a FDC card or main board since only 3 components (UM8398*1, 7406*2) are needed in the IBM PC XT/AT drive system.

The address decoder of UM8398 is switchable by setting pin 29 of UM8398. If pin 29 is set to 1 (high), then the I/O address of the UM8398 is selected in the primary drive group address (3F1~3F7, 1F7) described in Table A-1.

Table A-1 I/O addresses of the UM8398 registers

Primary	Secondary	Read	Write
3F1	371	Drive type register	
3F2	372		Digital output register
3F4	374	Main status register	Main status register
3F5	375	Diskette data register	Diskette data register
3F7	377	Digital input register	Transfer rate register
1F7	177	Status register*	

* Fixed disk function

B: PC/AT Application

The UM8398's registers described in Table A-1 are the same as the PC/AT floppy disk controller's. Therefore, the UM8398 can be directly implemented into the FDC card of the PC/AT to support 1.2M, 720K, 360K Bytes FDD with only 3 components (UM8398*1, 7406*2) are needed. The application circuit is shown in Figure A-1.

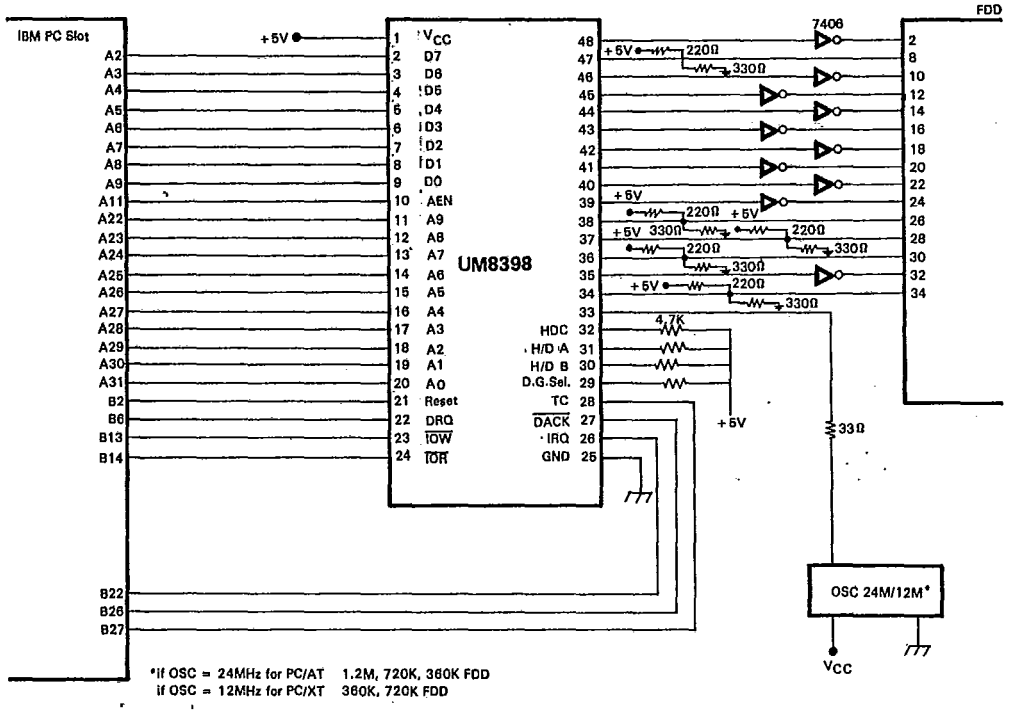


Figure A-1 PC/AT (1.2M, 720K, 360K FDD) and PC/XT (360K, 720K FDD) Application Circuit

C: PC/XT Application

If the UM8398 is implemented into the FDC card of the PC/XT to support 360K Byte and 720K Byte FDD, the application circuit is the same as the PC/AT's of the UM8398 except that the frequency of the oscillation circuit has to be 12 MHz.

If the UM8398 is used to support 1.2M, 720K, 360K Byte FDD in the PC/XT, then an additional FDC program is needed to control the 1.2M Byte FDD since the PC/XT BIOS doesn't support the 1.2M Byte FDD. During the FDD operation, this additional BIOS reads the contents of the UM8398's Drive Type Register set by pin 30 and pin 31, thus selects the drive to be 1.2M or 360K Byte FDD.

The contents of the UM8398's Hard Disk Status Register will be checked when system BIOS executes self-test. This register's bit 7 should be high by setting pin 32 to high when the PC system has no Hard Disk Control card, otherwise the register's bit 7 should be low by setting pin 32 to low.

Table A-2 Shows the definition of pins 30, 31, and 32.

Table A-2

H/D A (Pin 31)	H/D B(Pin 30)	HDC (Pin 32)
"1" High density	High density	Without HDC in system
"0" Double density	Double density	With HDC in system

PC/XT 1.2M, 720K, 360K FDD Application Circuits

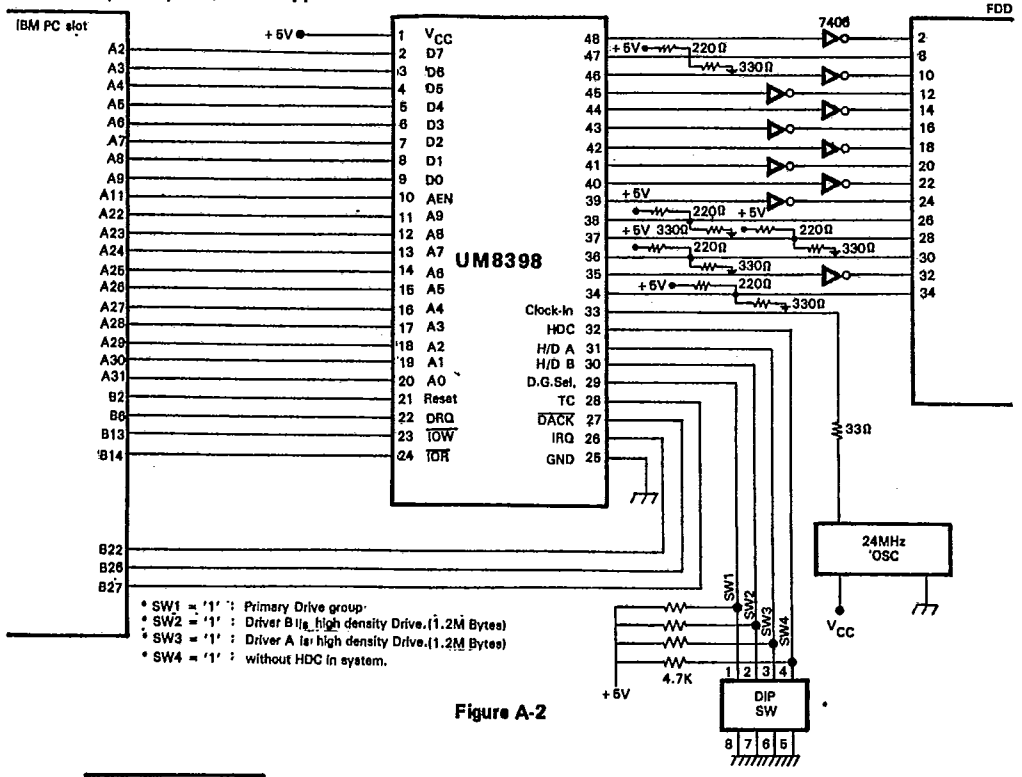


Figure A-2

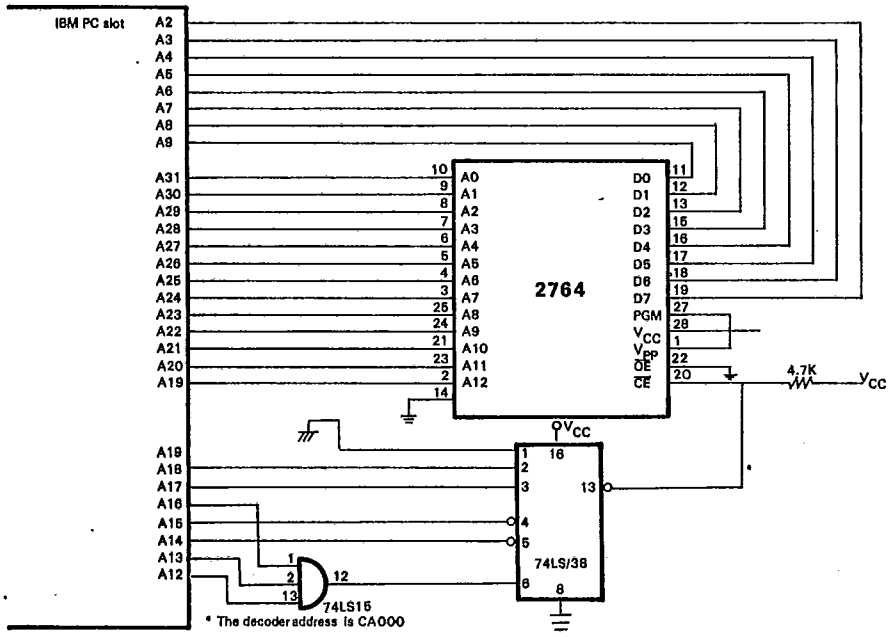


Figure A-3 PC/XT BIOS ROM circuit

Ordering Information

Part Number	Operating Current (Max.)	Package Type
UM8398	200 mA	48L DIP
UM8398L-1	200 mA	52 PLCC
UM8398L-2	200 mA	68 PLCC