Flex III PC/AT
80386DX/80486 Cache/DRAM Controller
SL9795

ADVANCE

FEATURES:

- 100% IBM PC/AT Compatible
- Supports Both 80386DX and 80486 CPU's
- Supports 80387DX Numeric Coprocessor
- 25/33/40 MHz Operation
- ISA Bus Control
- Advanced Testing Features
- Advanced Low Power CMOS Technology
- 208 Pin PQFP

Cache Control

- Direct Map Write Back Cache Controller
- Zero Wait State Cache Hit
- Supports 80486 Burst Mode
- Supports Cache Sizes of 64K, 128K and 256K
- Cacheable RAM Area Of Up To 64M
- Programmable Non-Cacheable Regions
- Supports Bus Snooping and Hidden Refresh

DRAM Control

- Enhanced Page Mode Operation
- Supports up to 64M of Main Memory
- Supports 256K, 1M, and 4M DRAM's
- Supports Intermixing of Different DRAM Sizes
- Shadow RAM Feature
- Selectable Wait States for DRAM Access
- Supports 8 or 16 Bit BIOS ROM
- Selectable Wait States for BIOS ROM
- Staggered RAS Refresh

System Control

- Synchronous or Asynchronous Operation
- Programmable Command Delays
- Programmable Wait States For Local and Off-Board Cycles
- Generates All ISA Bus and Arbitration Control Signals
- Fast Gate A20 and Fast Reset

Peripheral Control

- 7 DMA Channels
- 14 External Interrupt Registers
- 3 Programmable Timer/Counter Channels

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VIA Technologies, Inc. (408) 746-2200
860 East Arques Avenue
Sunnyvale, CA 94086

GENERAL DESCRIPTION

When developing a cache-based 80386DX or 80486 system, the user has to deal with different suppliers for cache controller, system chipset and peripheral controller. Even when one company offers these items as a set, the integration level is not high enough and most of the controllers do not support high performance write back cache architecture.

To solve these problems, the SL9795 integrates a high performance write back cache controller, page interleave DRAM controller, system controller as well as the IBM PC/AT compatible peripheral controller in a single 208 pin chip. The SL9795 is divided into four main sections:

CACHE CONTROLLER

The write back cache controller implemented in SL9795 interfaces directly with the CPU, while all other sections act as slaves to the cache subsystem. Since the majority of CPU cycles are local memory read/write cycles, they are executed from fast cache memory. Occasionally when data is not found in local cache, the cache controller forwards the access to the main memory with standard wait states. To the DRAM controller subsystem, the cache controller looks like the CPU and when a cycle is completed the DRAM controller sends ready back to cache controller which in turn passes it on to CPU. When a remote master (DMA) wants to access the main memory, the cache subsystem will allow direct memory access to cache if the accessed data is contained in cache. However, if the data is not contained in cache, the cache controller will allow the DRAM controller to take over and the DMA cycle is completed in the same manner as in a non-cache sytem. Refresh requests are intercepted by the cache controller, a dummy hold acknowledge is passed to the peripheral controller subsystem, and a "hidden" refresh is carried out without holding the CPU. The smallest amount of information exchanged between cache and main memory (line size) is 4 bytes for 80386 and 32 bytes for 80486.

DRAM CONTROLLER

SL9795 supports an enhanced page mode architecture. Memory misses from the cache controller are sent to the DMA controller. When consecutive (CACHE MISS) accesses are made to the same DRAM page (DRAM HIT), the DRAM controller will take less time to complete the cycle thereby providing better performance on the cache miss cycles as well. The RAS and CAS pulse widths are fully programmable through BIOS. Shadow RAM and 384K remap options are also supported. SL9795 also provides memory address buffers to allow direct interface to 4 banks of DRAM's.

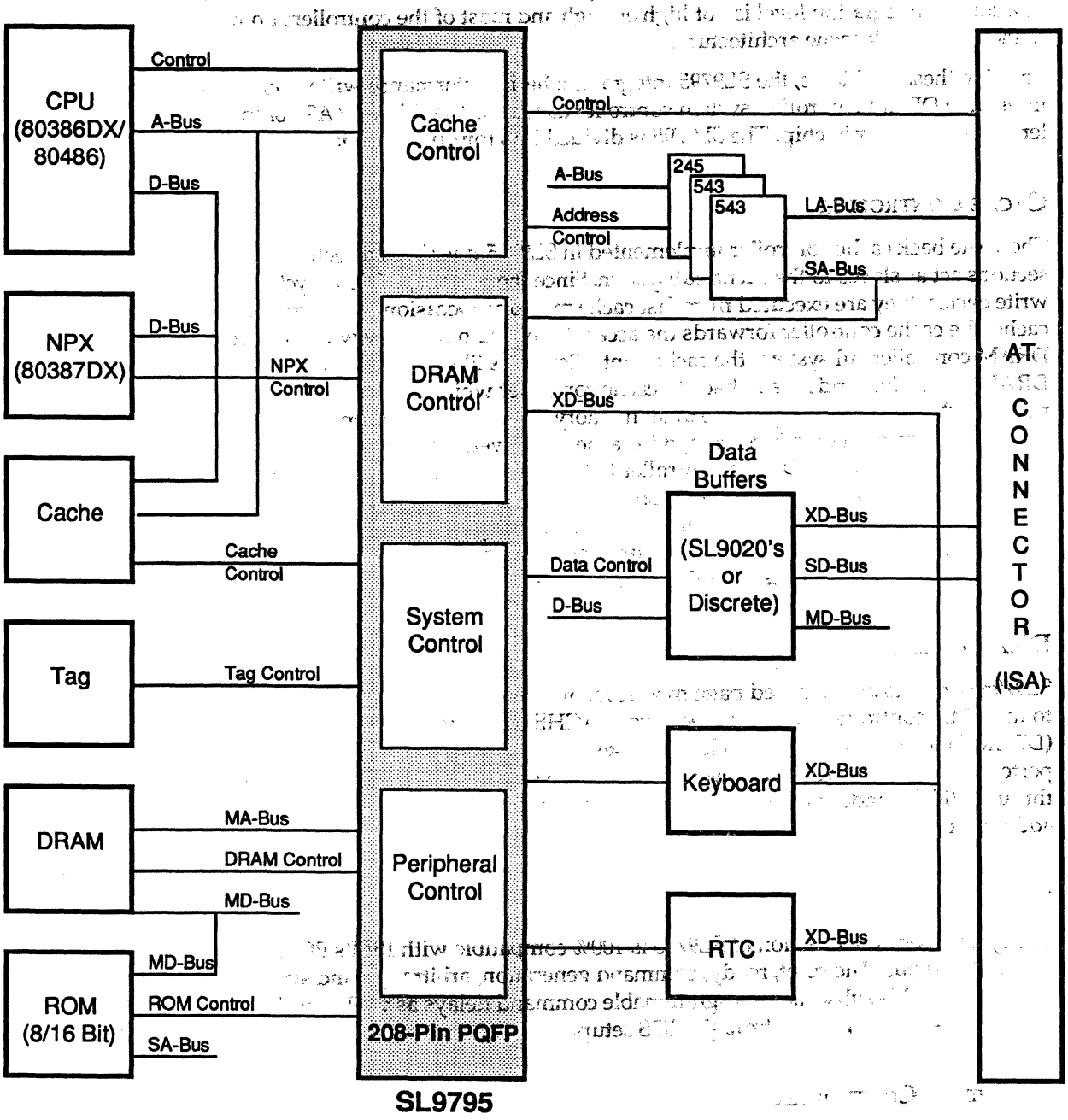
SYSTEM CONTROLLER

The system controller section of SL9795 is 100% compatible with IBM's PC/AT industry standard architecture (ISA) bus. The reset, ready, command generation, arbitration and system control signals are all generated by this subsection. Programmable command delays as well as wait states for 8 or 16 bit off-board I/O's are supported through BIOS setup.

PERIPHERAL CONTROLLER

The peripheral controller subsection is compatible with VIA's industry standard IPC, SL9030. It contains two 8237A DMA controllers, two 8259A-type interrupt controllers, one 8254 timer and one 74LS612-compatible memory mapper. The DMA and refresh arbitration logic supporting the hidden refresh is also included in this section.

BLOCK DIAGRAM SL9795



Flex III SL9795 80386DX/80486 Cache/DRAM Controller
System Level Block Diagram

VIA Technologies, Inc.
860 East Arques
Sunnyvale, CA 94086
Phone: 408/746-2200
or: 800/621-CHIP
FAX 408/746-2222