Data Sheet

K8T890 Version CD Desktop North Bridge

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VIA TECHNOLOGIES, INC.

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1.01	1/27/05	Added "Version CD" to product name on cover page	EY
1.02	2/22/05	Updated mechanical spec. diagrams	EY
1.03	7/20/05	Modified cover page Removed PCI Master read caching in overview section Removed "supports asynchronous interface between HyperTransport and PCI Express"	SV

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K8T890 NORTH BRIDGE

800 MHz AMD Athlon 64 / Opteron HyperTransport Interface
PCI Express Interface
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PRODUCT FEATURES

- **Defines Highly Integrated Solutions for Performance Server / Workstation / PC Designs**
  - High performance North Bridge with HyperTransport interface to AMD Athlon 64 / Sempron / Opteron CPU plus PCI Express with high-speed V-Link interface to the South Bridge
  - Combines with VIA VT8235M / VT8237R / VT8251 V-Link South Bridge for integrated 10/100 LAN, AC97-Link, ATA133 IDE, LPC, USB 2.0, Serial ATA (VT8237R & VT8251), AHCI SATA II RAID controller with NCQ (VT8251), PCI Express (VT8251) and High Definition Audio (VT8251)
  - 933 Ball Grid Array package with 35 x 35 mm body size, 1mm ball pitch, and heat spreader
  - 1.5V core, 0.15 um process
- **High Performance HyperTransport CPU Interface**
  - Processor interface via HyperTransport interface
  - 8 or 16-bit control / address / data transfer both directions (transmit and receive may be different widths)
  - Supports simultaneous bi-directional 1600 / 1200 / 800 / 400 MT/sec (Mega-Transfers per second) at 800 / 600 / 400 / 200 MHz clock rates (up to 6.4 GB/sec using 16-bit data transfer mode)
  - Default 8-bit, 200 MHz operation on startup with speedup to dual 16-bit, 800 MHz operation under software control
- **Advanced High Bandwidth PCI Express Interface**
  - PCI Express 1.0a support
  - Supports up to five PCI Express ports
    - 1st port: a 16-Lane port for high end graphics interface
      - Configurable lane width, 16 / 8 / 4 / 2 / 1, through hand-shaking for transfer rate up to 4 GB/sec bidirectional
      - Supports two upstream virtual channels
    - 2nd port: a 4-Lane port for high bandwidth peripheral devices
      - Configurable lane width, either 4 or 1
    - 3rd port: Optional 1-Lane ports
      - 3rd / 4th / 5th port: an 1-Lane port if the 2nd port is configured as a 1-Lane port
  - Supports interconnect power management
  - Supports polarity inversion and lane reversal
  - Supports Hot Plug
  - Loop-back testing mode for easy debugging mode for PCI Express

- **High Bandwidth 1 GB/Sec "Ultra V-Link" Host Controller**
  - Supports 66 MHz, 4x and 8x transfer modes, Ultra V-Link Host interface with 1 GB/sec total bandwidth
  - Separate command / strobe transfers for 4x half duplex mode and 8x full duplex mode
  - Request / Data split transaction
  - Transaction assurance for V-Link Host to Client access eliminates V-Link Host-Client Retry cycles
  - Intelligent V-Link transaction protocol to minimize data wait-state, throttle transfer latency and avoid data overflow
  - Highly efficient V-Link arbitration with minimum overhead
- **Advanced System Power Management Support**
  - ACPI 2.0 and PCI Bus Power Management 1.1 compliant
  - Supports LDTSTOP# (HyperTransport Bus Stop) protocol
  - Low-leakage I/O pads

K8T890 SYSTEM OVERVIEW

The K8T890 North Bridge is a high performance, cost-effective solution for the implementation of 64-bit capable server, workstation and desktop personal computer systems based on AMD Athlon 64 / Sempron / Opteron processors.

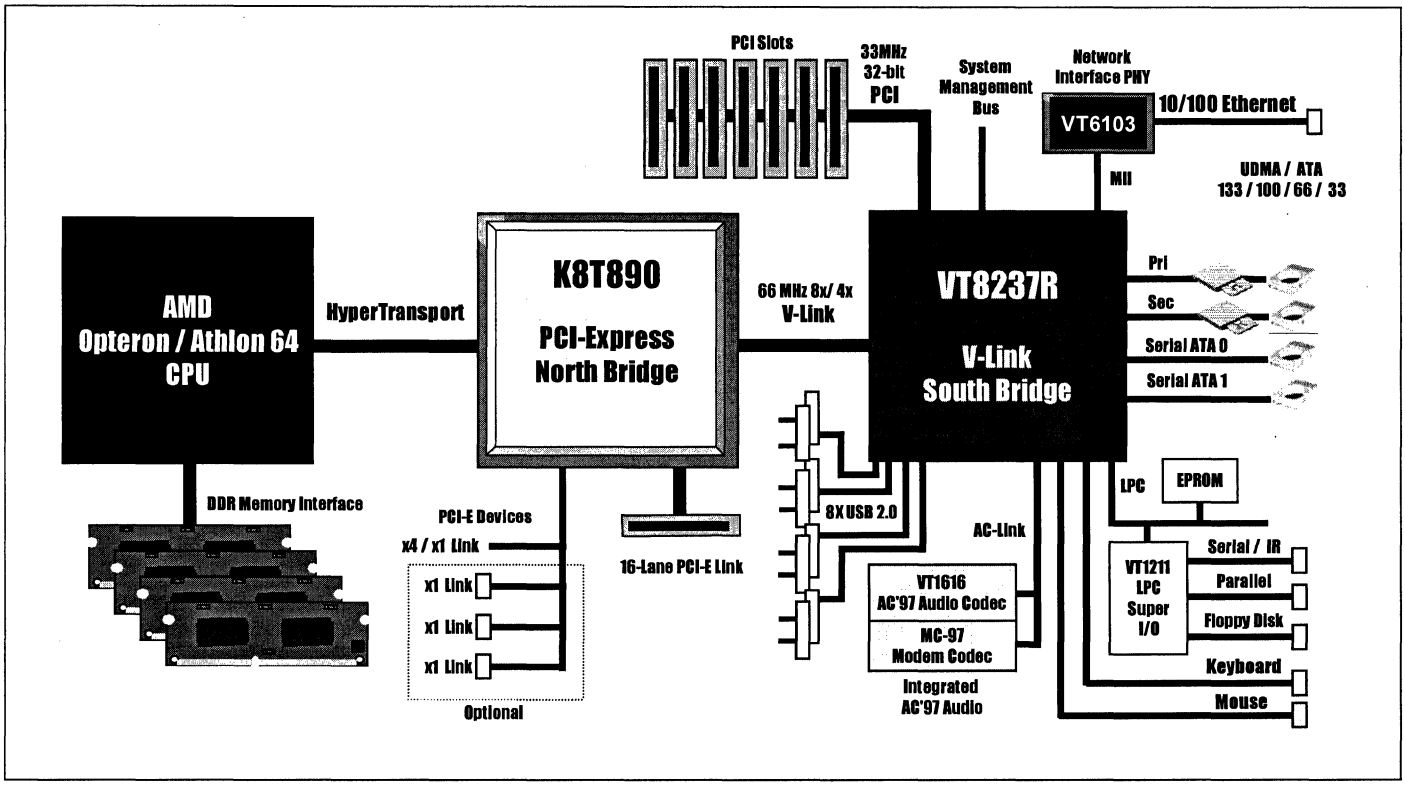

Figure 1. System Block Diagram

A complete 64-bit Athlon 64 / Sempron / Opteron chipset consists of the K8T890 North Bridge and the VT8237R V-Link South Bridge. The K8T890 provides superior performance between CPU / HyperTransport, V-Link and PCI Express bus. The VT8237R is a highly integrated peripheral controller which includes V-Link-to-PCI / V-Link-to-LPC controllers, Ultra DMA IDE controllers, Serial ATA host controller, USB2.0 host controller, 10 / 100 Mb networking MAC, AC97 and system power management controllers.

K8T890 Overview

The K8T890 interfaces to the AMD Athlon 64 / Sempron / Opteron processor via the HyperTransport interface with data transfer rate of 1.6 GT/sec, 1.2 GT/sec, 800 MT/sec or 400 MT/sec each direction (input and output), simultaneously, providing a total maximum data transfer bandwidth of 6.4 GB/sec.

The K8T890 includes a PCI Express 1.0a compliant PCI Express controller, which supports up to five high bandwidth PCI-E ports. A 16-lane port, with up to 4 GB/sec bi-directional data transfer rate and two upstream virtual channels, is implemented to support high-end PCI Express compliant graphics controller. An additional configurable 4-lane port is designed for bandwidth-hungry peripheral devices. If the 4-Lane port is used to connect to a 1-Lane PCI-E peripheral device, the K8T890 allows the un-used lanes re-configured as a 1-Lane PCI-E port.

The K8T890 North Bridge interfaces to the South Bridge through a high speed 8x 66 MHz (1 GB/sec) Data Transfer interconnect bus called Ultra V-Link. Deep pre-fetch and post-write buffers are included to allow for concurrent CPU and V-Link operation. The combined K8T890 North Bridge and VT8237R South Bridge system supports enhanced PCI bus commands such as "Memory-Read-Line", "Memory-Read-Multiple" and "Memory-Write-Invalid" commands to minimize snoop overhead. In addition, advanced features are supported such as CPU write-back forward to PCI master and CPU write-back merged with PCI

post-write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction mechanism is also implemented for further improvement of overall system performance.

System Power Management

For sophisticated system power management, the K8T890 supports LDTSTOP# (HyperTransport Bus Stop) protocol to minimize power consumption during suspend system states (S1 and S3). Coupled with the VT8237R South Bridge chip, a complete power conscious PC main board can be implemented with no external glue-logic.

PINOUTS

Ball Diagram

Figure 2. K8T890 Ball Diagram (Top View)

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A		VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	HTRT COMP	HTR COMPN	VCCA33 HT1	GND	HTR CAD7-	HTR CAD7+	HTR CAD5-	HTR CAD5+	HTR CLK0-	HTR CLK0+
B	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	HTR COMPP	GNDA HT1	HTR CTL-	GND	HTR CAD6-	GND	HTR CAD4-	GND	HTR CAD3-
C	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	HTR CTL+	HTR CAD15+	HTR CAD6+	HTR CAD13+	HTR CAD4+	HTR CLK1+	HTR CAD3+
D	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	HTR CAD15-	GND	HTR CAD13-	GND	HTR CLK1-	GND
E	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	HTR CAD14-	HTR CAD14+	HTR CAD12-	HTR CAD12+	HTR CAD11-
F	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	GND	GND	VCC12 HT	VCC12 HT
G	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	G7	8	9	10	11	12	13	14	15	16	17
H	HTT CTL-	GND	VCCA33 HT2	VCC12 HT	VCC12 HT	VCC12 HT	H7				K8 CPU FSB						
J	HTT CTL+	GND	GNDA HT2	HTT CAD15-	VCC12 HT	VCC12 HT	J7		J9	10	11	12	13	14	15	16	17
K	HTT CAD6-	HTT CAD7+	HTT CAD7-	GND	HTT CAD15+	VCC12 HT	K7		K9	VCC15	VCC15	VCC15	VCC15	VCC15	VCC15	VCC15	VCC15
L	HTT CAD6+	GND	HTT CAD14-	HTT CAD14+	HTT CAD13-	VCC12 HT	L7		L9	VCC15	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT
M	HTT CAD4-	HTT CAD5+	HTT CAD5-	GND	HTT CAD13+	GND	M7		M9	VCC15	VCC12 HT	GND	GND	GND	GND	GND	GND
N	HTT CAD4+	GND	HTT CAD12-	HTT CAD12+	HTT CLK1-	GND	N7		N9	VCC15	VCC12 HT	GND	GND	GND	GND	GND	GND
P	HTT CAD3-	HTT CLK0+	HTT CLK0-	GND	HTT CLK1+	VCC12 HT	P7		P9	VCC15	VCC12 HT	GND	GND	GND	GND	GND	GND
R	HTT CAD3+	GND	HTT CAD11-	HTT CAD11+	HTT CAD10-	VCC12 HT	R7		R9	VCC15	VCC12 HT	GND	GND	GND	GND	GND	GND
T	HTT CAD1-	HTT CAD2+	HTT CAD2-	GND	HTT CAD10+	GND	T7		T9	VCC15	VCC12 HT	GND	GND	GND	GND	GND	GND
U	HTT CAD1+	GND	HTT CAD9-	HTT CAD9+	HTT CAD8-	GND	U7		U9	VCC15	VCC12 HT	GND	GND	GND	GND	GND	GND
V	HTSTOPI#	HTT CAD0+	HTT CAD0-	GND	HTT CAD8+	VCC12 HT	V7		V9	VCC15	VCC12 HT	GND	GND	GND	GND	GND	GND
W	HTSTOPO#	GND	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	W7		W9	VCC15	VCC12 HT	GND	GND	GND	GND	GND	GND
Y	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	Y7		Y9	VCC15	VCC12 HT	GND	GND	GND	GND	GND	GND
AA	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	AA7		AA9	VCC15	NC	GND	GND	GND	GND	GND	GND
AB	GND	GND	GND	GND	GND	GND	AB7		AB9	VCC15	NC	GND	GND	GND	GND	GND	GND
AC	NC	NC	NC	NC	NC	NC	AC7		AC9	VCC15	NC	GND	GND	GND	GND	GND	GND
AD	NC	NC	NC	NC	NC	NC	AD7		AD9	VCC15	NC	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE
AE	NC	NC	NC	NC	NC	NC	AE7		AE9	VCC15	VCC15	VCC15	VCC15	VCC15	VCC15	VCC15	VCC15
AF	NC	NC	NC	NC	NC	NC	AF7		AF9	10	11	12	13	14	15	16	17
AG	NC	NC	NC	NC	NC	NC	AG7					PCI-E Port 0					
AH	NC	NC	NC	NC	NC	NC	AH7	8	9	10	11	12	13	VSUS15 PE0	VCCA33 PE00	GNDA PE00	17
AJ	NC	NC	NC	NC	NC	NC	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	NC	PE0 RX1-	PE0 COMP0	PE0 RX3-	PE0 REXT0	PE0 RX5-	NC
AK	NC	NC	NC	NC	NC	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	NC	PE0 RX1+	GND	PE0 RX3+	GND	PE0 RX5+	GND
AL	NC	NC	NC	NC	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	GND	PE0 RX0-	GND	PE0 RX2-	GND	PE0 RX4-	GND	PE0 RX6-
AM	NC	NC	NC	NC	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	NC	NC	PE0 RX0+	PE0 TX1-	PE0 RX2+	PE0 TX3-	PE0 RX4+	PE0 TX5-	PE0 RX6+
AN	NC	NC	NC	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	NC	GND	NC	PE0 TX0-	PE0 TX1+	PE0 TX2-	PE0 TX3+	PE0 TX4-	PE0 TX5+	PE0 TX6-
AP	NC	NC	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	PEDET	INTR#	NC	PE0 TX0+	GND	PE0 TX2+	GND	PE0 TX4+	GND	PE0 TX6+
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
HTR CAD2-	HTR CAD2+	HTR CAD0-	HTR CAD0+	VCC12 HT	VCC 12HT	VCC12 HT	HCLK-	NC	NC	DEBUG	VCC15	VCC15 VL	VCC15 VL	VCC15 VL	VCC15 VL	VCC15 VL	A
GND	HTR CAD1-	GND	VCC12 HT	VCC12 HT	VCC 12HT	VCC12 HT	HCLK+	NC	GND	TCLK600	VCC15	VCC15 VL	VCC15 VL	VCC15 VL	VCC15 VL	VCC15 VL	B
HTR CAD10+	HTR CAD1+	HTR CAD8+	VCC12 HT	VCC12 HT	VCC 12HT	VCC12 HT	GND	NC	NC	VCLK	VCC15	VCC15 VL	VCC15 VL	VCC15 VL	VCC15 VL	VCC15 VL	C
HTR CAD10-	GND	HTR CAD8-	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCCA33 HCK	NC	NC	VCCA33 VCK	VCC15	VCC15 VL	VCC15 VL	VCC15 VL	VCC15 VL	TCLK	D
HTR CAD11+	HTR CAD9-	HTR CAD9+	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	GNDA HCK	NC	GND	GNDA VCK	VCC15	VCC15 VL	VCC15 VL	TESTIN#	GND	BUSY#	E
VCC12 HT	GND	GND	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC12 HT	VCC15	VCC15	VCC15	VCC15	VCC15 VL	VCC15 VL	DFTIN#	PE PMESCI#	PE HPSCI#	F
18	19	20	21	22	23	24	25	26	27	G28	VCC15	VCC15 VL	VCC15 VL	PWROK	SUSST#	PE WAKE#	G
									Ultra	H28	VCC15	VCC15 VL	VCC15 VL	RESET#	GND	VSUS15	H
18	19	20	21	22	23	24	25	J26	V-Link	J28	VCC15	VCC15 VL	VCC15 VL	VD11	VD15	VD14	J
VCC15	VCC15	VCC15	VCC15	VCC15	VCC15	VCC15	VCC15	K26		K28	VCC15	VCC15 VL	VCC15 VL	VD10	VD6	UP CMD	K
VCC12 HT	VCC12 HT	VCC12 HT	VCC15 VL	VCC15 VL	VCC15 VL	VCC15 VL	VCC15	L26		L28	VCC15	VCC15 VL	VCC15 VL	VD3	GND	VD7	L
GND	GND	GND	GND	GND	GND	VCC15 VL	VCC15	M26		M28	VCC15 VL	VCC15 VL	VCC15 VL	UP STB+	VD2	DN CMD	M
GND	GND	GND	GND	GND	GND	VCC15 VL	VCC15	N26		N28	VCC15 VL	VCC15 VL	VCC15 VL	UP STB-	DN STB-	DN STB+	N
GND	GND	GND	GND	GND	GND	VCC15 VL	VCC15	P26		P28	VCC15 VL	VCC15 VL	VCC15 VL	VLVREF	GND	VD0	P
GND	GND	GND	GND	GND	GND	VCC15 VL	VCC15	R26		R28	VCC15 VL	VCC15 VL	VCC15 VL	VD5	VBE#	VD1	R
GND	GND	GND	GND	GND	GND	VCC15 VL	VCC15	T26		T28	VCC15 VL	VCC15 VL	VCC15 VL	VD4	VD8	VPAR	T
GND	GND	GND	GND	GND	GND	VCC15 VL	VCC15	U26		U28	VCC15 VL	VCC15 VL	VCC15 VL	VD9	GND	VD12	U
GND	GND	GND	GND	GND	GND	VCC15 VL	VCC15	V26		V28	VCC15 VL	VCC15 VL	VCC15 VL	GND	VD13	VLCOMPP	V
GND	GND	GND	GND	GND	GND	VCC33 PE	VCC15	W26	PCI-E	W28	VCC33 PE	VCC33 PE	GNDA PE	VCCA33 PE	PE CLK+	PE CLK-	W
GND	GND	GND	GND	GND	GND	VCC33 PE	VCC15	Y26	Port 4	Y28	VCC33 PE	VCC33 PE	VCC33 PE	GND	PE1 TX3+	PE1 TX3-	Y
GND	GND	GND	GND	GND	GND	VCC33 PE	VCC15	AA26		AA28	VCC33 PE	VCC33 PE	VCC33 PE	PE1 RX3+	PE1 RX3-	GND	AA
GND	GND	GND	GND	GND	GND	VCC33 PE	VCC15	AB26	Port 3	AB28	VCC33 PE	VCC33 PE	VCC33 PE	GND	PE1 TX2+	PE1 TX2-	AB
GND	GND	GND	GND	GND	GND	VCC33 PE	VCC15	AC26		AC28	VCC33 PE	GNDA PE1	VCCA33 PE1	PE1 RX2+	PE1 RX2-	GND	AC
VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	GND	VCC15	AD26	Port 2	AD28	VCC33 PE	VSUS15 PE2	GND	PE1 REXT0	PE1 TX1+	PE1 TX1-	AD
VCC15	VCC15	VCC15	VCC15	VCC15	VCC15	VCC15	VCC15	AE26		AE28	VCC33 PE	VCC33 PE	PE1 COMP0	PE1 RX1+	PE1 RX1-	GND	AE
18	19	20	21	22	23	24	25	AF26	Port 1	AF28	VCC33 PE	VCC33 PE	VCC33 PE	GND	PE1 TX0+	PE1 TX0-	AF
										AG28	VCC33 PE	VCC33 PE	VCC33 PE	PE1 RX0+	PE1 RX0-	GND	AG
18	19	20	VSUS15 PE1	VCCA33 PE01	NC	24	25	26	27	AH28	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	AH
PE0 RX7-	PE0 COMP1	PE0 RX9-	PE0 REXT1	PE0 RX11-	GNDA PE01	PE0 RX13-	GND	PE0 RX15-	VCC33 PE	GND	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	AJ
PE0 RX7+	GND	PE0 RX9+	GND	PE0 RX11+	GND	PE0 RX13+	GND	PE0 RX15+	VCC33 PE	GND	GND	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	AK
GND	PE0 RX8-	GND	PE0 RX10-	GND	PE0 RX12-	GND	PE0 RX14-	GND	VCC33 PE	VCC33 PE	GND	GND	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	AL
PE0 TX7-	PE0 RX8+	PE0 TX9-	PE0 RX10+	PE0 TX11-	PE0 RX12+	PE0 TX13-	PE0 RX14+	PE0 TX15-	VCC33 PE	VCC33 PE	VCC33 PE	GND	GND	VCC33 PE	VCC33 PE	VCC33 PE	AM
PE0 TX7+	PE0 TX8-	PE0 TX9+	PE0 TX10-	PE0 TX11+	PE0 TX12-	PE0 TX13+	PE0 TX14-	PE0 TX15+	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	GND	GND	VCC33 PE	VCC33 PE	AN
GND	PE0 TX8+	GND	PE0 TX10+	GND	PE0 TX12+	GND	PE0 TX14+	GND	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	GND	GND	VCC33 PE	AP
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	

Pin Lists

Table 1. Pin List (Listed by Pin Number)

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
A02	VCC12HT	C08	VCC12HT	E15	HTRCAD12-	H29	VCC15	L32	VD3	P16	GND
A03	VCC12HT	C09	VCC12HT	E16	HTRCAD12+	H30	VCC15VL	L33	GND	P17	GND
A04	VCC12HT	C10	VCC12HT	E17	HTRCAD11-	H31	VCC15VL	L34	VD7	P18	GND
A05	VCC12HT	C11	HTRCTL+	E18	HTRCAD11+	H32	RESET#	M01	HTTCAD4-	P19	GND
A06	VCC12HT	C12	HTRCAD15+	E19	HTRCAD9-	H33	GND	M02	HTTCAD5+	P20	GND
A07	VCC12HT	C13	HTRCAD6+	E20	HTRCAD9+	H34	VSUS15	M03	HTTCAD5-	P21	GND
A08	HTRTCOMP	C14	HTRCAD13+	E21	VCC12HT	J01	HTTCTL+	M04	GND	P22	GND
A09	HTRCOMPN	C15	HTRCAD4+	E22	VCC12HT	J02	GND	M05	HTTCAD13+	P23	GND
A10	VCCA33HT1	C16	HTRCLK1+	E23	VCC12HT	J03	GNDAHT2	M06	GND	P24	VCC15VL
A11	GND	C17	HTRCAD3+	E24	VCC12HT	J04	HTTCAD15-	M10	VCC15	P25	VCC15
A12	HTRCAD7-	C18	HTRCAD10+	E25	GNDAHCK	J05	VCC12HT	M11	VCC12HT	P29	VCC15VL
A13	HTRCAD7+	C19	HTRCAD1+	E27	GND	J06	VCC12HT	M12	GND	P30	VCC15VL
A14	HTRCAD5-	C20	HTRCAD8+	E28	GNDAVCK	J29	VCC15	M13	GND	P31	VCC15VL
A15	HTRCAD5+	C21	VCC12HT	E29	VCC15	J30	VCC15VL	M14	GND	P32	VLVREF
A16	HTRCLK0-	C22	VCC12HT	E30	VCC15VL	J31	VCC15VL	M15	GND	P33	GND
A17	HTRCLK0+	C23	VCC12HT	E31	VCC15VL	J32	VD11	M16	GND	P34	VD0
A18	HTRCAD2-	C24	VCC12HT	E32	TESTIN#	J33	VD15	M17	GND	R01	HTTCAD3+
A19	HTRCAD2+	C25	GND	E33	GND	J34	VD14	M18	GND	R02	GND
A20	HTRCAD0-	C28	VCLK	E34	BUSY#	K01	HTTCAD6-	M19	GND	R03	HTTCAD11-
A21	HTRCAD0+	C29	VCC15	F01	VCC12HT	K02	HTTCAD7+	M20	GND	R04	HTTCAD11+
A22	VCC12HT	C30	VCC15VL	F02	VCC12HT	K03	HTTCAD7-	M21	GND	R05	HTTCAD10-
A23	VCC12HT	C31	VCC15VL	F03	VCC12HT	K04	GND	M22	GND	R06	VCC12HT
A24	VCC12HT	C32	VCC15VL	F04	VCC12HT	K05	HTTCAD15+	M23	GND	R10	VCC15
A25	HCLK-	C33	VCC15VL	F05	VCC12HT	K06	VCC12HT	M24	VCC15VL	R11	VCC12HT
A28	DEBUG	C34	VCC15VL	F06	VCC12HT	K10	VCC15	M25	VCC15	R12	GND
A29	VCC15	D01	VCC12HT	F07	VCC12HT	K11	VCC15	M29	VCC15VL	R13	GND
A30	VCC15VL	D02	VCC12HT	F08	VCC12HT	K12	VCC15	M30	VCC15VL	R14	GND
A31	VCC15VL	D03	VCC12HT	F09	VCC12HT	K13	VCC15	M31	VCC15VL	R15	GND
A32	VCC15VL	D04	VCC12HT	F10	VCC12HT	K14	VCC15	M32	UPSTB+	R16	GND
A33	VCC15VL	D05	VCC12HT	F11	VCC12HT	K15	VCC15	M33	VD2	R17	GND
A34	VCC15VL	D06	VCC12HT	F12	VCC12HT	K16	VCC15	M34	DNCMD	R18	GND
B01	VCC12HT	D07	VCC12HT	F13	VCC12HT	K17	VCC15	N01	HTTCAD4+	R19	GND
B02	VCC12HT	D08	VCC12HT	F14	GND	K18	VCC15	N02	GND	R20	GND
B03	VCC12HT	D09	VCC12HT	F15	GND	K19	VCC15	N03	HTTCAD12-	R21	GND
B04	VCC12HT	D10	VCC12HT	F16	VCC12HT	K20	VCC15	N04	HTTCAD12+	R22	GND
B05	VCC12HT	D11	VCC12HT	F17	VCC12HT	K21	VCC15	N05	HTTCLK1-	R23	GND
B06	VCC12HT	D12	HTRCAD15-	F18	VCC12HT	K22	VCC15	N06	GND	R24	VCC15VL
B07	VCC12HT	D13	GND	F19	GND	K23	VCC15	N10	VCC15	R25	VCC15
B08	VCC12HT	D14	HTRCAD13-	F20	GND	K24	VCC15	N11	VCC12HT	R29	VCC15VL
B09	HTRCOMPP	D15	GND	F21	VCC12HT	K25	VCC15	N12	GND	R30	VCC15VL
B10	GNDAHT1	D16	HTRCLK1-	F22	VCC12HT	K29	VCC15	N13	GND	R31	VCC15VL
B11	HTRCTL-	D17	GND	F23	VCC12HT	K30	VCC15VL	N14	GND	R32	VD5
B12	GND	D18	HTRCAD10-	F24	VCC12HT	K31	VCC15VL	N15	GND	R33	VBE#
B13	HTRCAD6-	D19	GND	F25	VCC12HT	K32	VD10	N16	GND	R34	VD1
B14	GND	D20	HTRCAD8-	F26	VCC15	K33	VD6	N17	GND	T01	HTTCAD1-
B15	HTRCAD4-	D21	VCC12HT	F27	VCC15	K34	UPCMD	N18	GND	T02	HTTCAD2+
B16	GND	D22	VCC12HT	F28	VCC15	L01	HTTCAD6+	N19	GND	T03	HTTCAD2-
B17	HTRCAD3-	D23	VCC12HT	F29	VCC15	L02	GND	N20	GND	T04	GND
B18	GND	D24	VCC12HT	F30	VCC15VL	L03	HTTCAD14-	N21	GND	T05	HTTCAD10+
B19	HTRCAD1-	D25	VCCA33HCK	F31	VCC15VL	L04	HTTCAD14+	N22	GND	T06	GND
B20	GND	D28	VCCA33VCK	F32	DFTIN#	L05	HTTCAD13-	N23	GND	T10	VCC15
B21	VCC12HT	D29	VCC15	F33	PEPMESCI#	L06	VCC12HT	N24	VCC15VL	T11	VCC12HT
B22	VCC12HT	D30	VCC15VL	F34	PEHPSCI#	L10	VCC15	N25	VCC15	T12	GND
B23	VCC12HT	D31	VCC15VL	G01	VCC12HT	L11	VCC12HT	N29	VCC15VL	T13	GND
B24	VCC12HT	D32	VCC15VL	G02	VCC12HT	L12	VCC12HT	N30	VCC15VL	T14	GND
B25	HCLK+	D33	VCC15VL	G03	VCC12HT	L13	VCC12HT	N31	VCC15VL	T15	GND
B27	GND	D34	TCLK	G04	VCC12HT	L14	VCC12HT	N32	UPSTB-	T16	GND
B28	TCLK600	E01	VCC12HT	G05	VCC12HT	L15	VCC12HT	N33	DNSTB-	T17	GND
B29	VCC15	E02	VCC12HT	G06	VCC12HT	L16	VCC12HT	N34	DNSTB+	T18	GND
B30	VCC15VL	E03	VCC12HT	G29	VCC15	L17	VCC12HT	P01	HTTCAD3-	T19	GND
B31	VCC15VL	E04	VCC12HT	G30	VCC15VL	L18	VCC12HT	P02	HTTCLK0+	T20	GND
B32	VCC15VL	E05	VCC12HT	G31	VCC15VL	L19	VCC12HT	P03	HTTCLK0-	T21	GND
B33	VCC15VL	E06	VCC12HT	G32	PWROK	L20	VCC12HT	P04	GND	T22	GND
B34	VCC15VL	E07	VCC12HT	G33	SUSST#	L21	VCC15VL	P05	HTTCLK1+	T23	GND
C01	VCC12HT	E08	VCC12HT	G34	PEWAKE#	L22	VCC15VL	P06	VCC12HT	T24	VCC15VL
C02	VCC12HT	E09	VCC12HT	H01	HTTCTL-	L23	VCC15VL	P10	VCC15	T25	VCC15
C03	VCC12HT	E10	VCC12HT	H02	GND	L24	VCC15VL	P11	VCC12HT	T29	VCC15VL
C04	VCC12HT	E11	VCC12HT	H03	VCCA33HT2	L25	VCC15	P12	GND	T30	VCC15VL
C05	VCC12HT	E12	VCC12HT	H04	VCC12HT	L29	VCC15	P13	GND	T31	VCC15VL
C06	VCC12HT	E13	HTRCAD14-	H05	VCC12HT	L30	VCC15VL	P14	GND	T32	VD4
C07	VCC12HT	E14	HTRCAD14+	H06	VCC12HT	L31	VCC15VL	P15	GND	T33	VD8

Table 2. Pin List Continued (Listed by Pin Number)

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
T34	VPAR	W18	GND	AB03	GND	AE14	VCC15	AK10	VCC33PE	AM24	PE0TX13-
U01	HTTCAD1+	W19	GND	AB04	GND	AE15	VCC15	AK12	PE0RX1+	AM25	PE0RX14+
U02	GND	W20	GND	AB05	GND	AE16	VCC15	AK13	GND	AM26	PE0TX15-
U03	HTTCAD9-	W21	GND	AB06	GND	AE17	VCC15	AK14	PE0RX3+	AM27	VCC33PE
U04	HTTCAD9+	W22	GND	AB10	VCC15	AE18	VCC15	AK15	GND	AM28	VCC33PE
U05	HTTCAD8-	W23	GND	AB12	GND	AE19	VCC15	AK16	PE0RX5+	AM29	VCC33PE
U06	GND	W24	VCC33PE	AB13	GND	AE20	VCC15	AK17	GND	AM30	GND
U10	VCC15	W25	VCC15	AB14	GND	AE21	VCC15	AK18	PE0RX7+	AM31	GND
U11	VCC12HT	W29	VCC33PE	AB15	GND	AE22	VCC15	AK19	GND	AM32	VCC33PE
U12	GND	W30	VCC33PE	AB16	GND	AE23	VCC15	AK20	PE0RX9+	AM33	VCC33PE
U13	GND	W31	GNDAPE	AB17	GND	AE24	VCC15	AK21	GND	AM34	VCC33PE
U14	GND	W32	VCCA33PE	AB18	GND	AE25	VCC15	AK22	PE0RX11+	AN04	VCC33PE
U15	GND	W33	PECLK+	AB19	GND	AE29	VCC33PE	AK23	GND	AN05	VCC33PE
U16	GND	W34	PECLK-	AB20	GND	AE30	VCC33PE	AK24	PE0RX13+	AN06	VCC33PE
U17	GND	Y01	VCC12HT	AB21	GND	AE31	PE1COMP0	AK25	GND	AN07	VCC33PE
U18	GND	Y02	VCC12HT	AB22	GND	AE32	PE1RX1+	AK26	PE0RX15+	AN09	GND
U19	GND	Y03	VCC12HT	AB23	GND	AE33	PE1RX1-	AK27	VCC33PE	AN11	PE0TX0-
U20	GND	Y04	VCC12HT	AB24	VCC33PE	AE34	GND	AK28	GND	AN12	PE0TX1+
U21	GND	Y05	VCC12HT	AB25	VCC15	AF29	VCC33PE	AK29	GND	AN13	PE0TX2-
U22	GND	Y06	VCC12HT	AB29	VCC33PE	AF30	VCC33PE	AK30	VCC33PE	AN14	PE0TX3+
U23	GND	Y10	VCC15	AB30	VCC33PE	AF31	VCC33PE	AK31	VCC33PE	AN15	PE0TX4-
U24	VCC15VL	Y11	VCC12HT	AB31	VCC33PE	AF32	GND	AK32	VCC33PE	AN16	PE0TX5+
U25	VCC15	Y12	GND	AB32	GND	AF33	PE1TX0+	AK33	VCC33PE	AN17	PE0TX6-
U29	VCC15VL	Y13	GND	AB33	PE1TX2+	AF34	PE1TX0-	AK34	VCC33PE	AN18	PE0TX7+
U30	VCC15VL	Y14	GND	AB34	PE1TX2-	AG29	VCC33PE	AL05	VCC33PE	AN19	PE0TX8-
U31	VCC15VL	Y15	GND	AC10	VCC15	AG30	VCC33PE	AL06	VCC33PE	AN20	PE0TX9+
U32	VD9	Y16	GND	AC12	GND	AG31	VCC33PE	AL07	VCC33PE	AN21	PE0TX10-
U33	GND	Y17	GND	AC13	GND	AG32	PE1RX0+	AL08	VCC33PE	AN22	PE0TX11+
U34	VD12	Y18	GND	AC14	GND	AG33	PE1RX0-	AL09	VCC33PE	AN23	PE0TX12-
V01	HTSTOPI#	Y19	GND	AC15	GND	AG34	GND	AL10	GND	AN24	PE0TX13+
V02	HTTCAD0+	Y20	GND	AC16	GND	AH14	VSUS15PE0	AL11	PE0RX0-	AN25	PE0TX14-
V03	HTTCAD0-	Y21	GND	AC17	GND	AH15	VCCA33PE00	AL12	GND	AN26	PE0TX15+
V04	GND	Y22	GND	AC18	GND	AH16	GNDAPE00	AL13	PE0RX2-	AN27	VCC33PE
V05	HTTCAD8+	Y23	GND	AC19	GND	AH21	VSUS15PE1	AL14	GND	AN28	VCC33PE
V06	VCC12HT	Y24	VCC33PE	AC20	GND	AH22	VCCA33PE01	AL15	PE0RX4-	AN29	VCC33PE
V10	VCC15	Y25	VCC15	AC21	GND	AH29	VCC33PE	AL16	GND	AN30	VCC33PE
V11	VCC12HT	Y29	VCC33PE	AC22	GND	AH30	VCC33PE	AL17	PE0RX6-	AN31	GND
V12	GND	Y30	VCC33PE	AC23	GND	AH31	VCC33PE	AL18	GND	AN32	GND
V13	GND	Y31	VCC33PE	AC24	VCC33PE	AH32	VCC33PE	AL19	PE0RX8-	AN33	VCC33PE
V14	GND	Y32	GND	AC25	VCC15	AH33	VCC33PE	AL20	GND	AN34	VCC33PE
V15	GND	Y33	PE1TX3+	AC29	VCC33PE	AH34	VCC33PE	AL21	PE0RX10-	AP03	VCC33PE
V16	GND	Y34	PE1TX3-	AC30	GNDAPE1	AJ07	VCC33PE	AL22	GND	AP04	VCC33PE
V17	GND	AA01	VCC12HT	AC31	VCCA33PE1	AJ08	VCC33PE	AL23	PE0RX12-	AP05	VCC33PE
V18	GND	AA02	VCC12HT	AC32	PE1RX2+	AJ09	VCC33PE	AL24	GND	AP06	VCC33PE
V19	GND	AA03	VCC12HT	AC33	PE1RX2-	AJ10	VCC33PE	AL25	PE0RX14-	AP07	VCC33PE
V20	GND	AA04	VCC12HT	AC34	GND	AJ12	PE0RX1-	AL26	GND	AP08	PEDET
V21	GND	AA05	VCC12HT	AD10	VCC15	AJ13	PE0COMP0	AL27	VCC33PE	AP09	INTR#
V22	GND	AA06	VCC12HT	AD12	VCC33PE	AJ14	PE0RX3-	AL28	VCC33PE	AP11	PE0TX0+
V23	GND	AA10	VCC15	AD13	VCC33PE	AJ15	PE0REXT0	AL29	GND	AP12	GND
V24	VCC15VL	AA12	GND	AD14	VCC33PE	AJ16	PE0RX5-	AL30	GND	AP13	PE0TX2+
V25	VCC15	AA13	GND	AD15	VCC33PE	AJ18	PE0RX7-	AL31	VCC33PE	AP14	GND
V29	VCC15VL	AA14	GND	AD16	VCC33PE	AJ19	PE0COMP1	AL32	VCC33PE	AP15	PE0TX4+
V30	VCC15VL	AA15	GND	AD17	VCC33PE	AJ20	PE0RX9-	AL33	VCC33PE	AP16	GND
V31	VCC15VL	AA16	GND	AD18	VCC33PE	AJ21	PE0REXT1	AL34	VCC33PE	AP17	PE0TX6+
V32	GND	AA17	GND	AD19	VCC33PE	AJ22	PE0RX11-	AM05	VCC33PE	AP18	GND
V33	VD13	AA18	GND	AD20	VCC33PE	AJ23	GNDAPE01	AM06	VCC33PE	AP19	PE0TX8+
V34	VLCOMPP	AA19	GND	AD21	VCC33PE	AJ24	PE0RX13-	AM07	VCC33PE	AP20	GND
W01	HTSTOPO#	AA20	GND	AD22	VCC33PE	AJ25	GND	AM08	VCC33PE	AP21	PE0TX10+
W02	GND	AA21	GND	AD23	VCC33PE	AJ26	PE0RX15-	AM11	PE0RX0+	AP22	GND
W03	VCC12HT	AA22	GND	AD24	GND	AJ27	VCC33PE	AM12	PE0TX1-	AP23	PE0TX12+
W04	VCC12HT	AA23	GND	AD25	VCC15	AJ28	GND	AM13	PE0RX2+	AP24	GND
W05	VCC12HT	AA24	VCC33PE	AD29	VCC33PE	AJ29	VCC33PE	AM14	PE0TX3-	AP25	PE0TX14+
W06	VCC12HT	AA25	VCC15	AD30	VSUS15PE2	AJ30	VCC33PE	AM15	PE0RX4+	AP26	GND
W10	VCC15	AA29	VCC33PE	AD31	GND	AJ31	VCC33PE	AM16	PE0TX5-	AP27	VCC33PE
W11	VCC12HT	AA30	VCC33PE	AD32	PE1REXT0	AJ32	VCC33PE	AM17	PE0RX6+	AP28	VCC33PE
W12	GND	AA31	VCC33PE	AD33	PE1TX1+	AJ33	VCC33PE	AM18	PE0TX7-	AP29	VCC33PE
W13	GND	AA32	PE1RX3+	AD34	PE1TX1-	AJ34	VCC33PE	AM19	PE0RX8+	AP30	VCC33PE
W14	GND	AA33	PE1RX3-	AE10	VCC15	AK06	VCC33PE	AM20	PE0TX9-	AP31	VCC33PE
W15	GND	AA34	GND	AE11	VCC15	AK07	VCC33PE	AM21	PE0RX10+	AP32	GND
W16	GND	AB01	GND	AE12	VCC15	AK08	VCC33PE	AM22	PE0TX11-	AP33	GND
W17	GND	AB02	GND	AE13	VCC15	AK09	VCC33PE	AM23	PE0RX12+	AP34	VCC33PE

NC pins: A26-A27, B26, C26-C27, D26-D27, E26, AA11, AB11, AC01-AC06, AC11, AD01-AD06, AD11, AE01-AE06, AF01-AF06, AG01-AG06, AH01-AH06, AJ01-AJ06, AJ11, AK01-AK05, AK11, AL01-AL04, AM01-AM04, AM09-AM10, AN01-AN03, AN08, AN10, AP01-AP02, AP10

Table 3. Pin List (Listed by Pin Name)

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
E34	BUSY#	P33	GND	Y13	GND	AK28	GND	A17	HTRCLK0+	AJ20	PE0RX9-
A28	DEBUG	R02	GND	Y14	GND	AK29	GND	D16	HTRCLK1-	AK20	PE0RX9+
F32	DFTIN#	R12	GND	Y15	GND	AL10	GND	C16	HTRCLK1+	AL21	PE0RX10-
M34	DNCMD	R13	GND	Y16	GND	AL12	GND	A09	HTRCOMPN	AM21	PE0RX10+
N33	DNSTB-	R14	GND	Y17	GND	AL14	GND	B09	HTRCOMPP	AJ22	PE0RX11-
N34	DNSTB+	R15	GND	Y18	GND	AL16	GND	B11	HTRCTL-	AK22	PE0RX11+
A11	GND	R16	GND	Y19	GND	AL18	GND	C11	HTRCTL+	AL23	PE0RX12-
B12	GND	R17	GND	Y20	GND	AL20	GND	A08	HTRTCOMP	AM23	PE0RX12+
B14	GND	R18	GND	Y21	GND	AL22	GND	V01	HTSTOPI#	AJ24	PE0RX13-
B16	GND	R19	GND	Y22	GND	AL24	GND	W01	HTSTOPO#	AK24	PE0RX13+
B18	GND	R20	GND	Y23	GND	AL26	GND	V03	HTTCAD0-	AL25	PE0RX14-
B20	GND	R21	GND	Y32	GND	AL29	GND	V02	HTTCAD0+	AM25	PE0RX14+
B27	GND	R22	GND	AA12	GND	AL30	GND	T01	HTTCAD1-	AJ26	PE0RX15-
C25	GND	R23	GND	AA13	GND	AM30	GND	U01	HTTCAD1+	AK26	PE0RX15+
D13	GND	T04	GND	AA14	GND	AM31	GND	T03	HTTCAD2-	AN11	PE0TX0-
D15	GND	T06	GND	AA15	GND	AN09	GND	T02	HTTCAD2+	AP11	PE0TX0+
D17	GND	T12	GND	AA16	GND	AN31	GND	P01	HTTCAD3-	AM12	PE0TX1-
D19	GND	T13	GND	AA17	GND	AN32	GND	R01	HTTCAD3+	AN12	PE0TX1+
E27	GND	T14	GND	AA18	GND	AP12	GND	M01	HTTCAD4-	AN13	PE0TX2-
E33	GND	T15	GND	AA19	GND	AP14	GND	N01	HTTCAD4+	AP13	PE0TX2+
F14	GND	T16	GND	AA20	GND	AP16	GND	M03	HTTCAD5-	AM14	PE0TX3-
F15	GND	T17	GND	AA21	GND	AP18	GND	M02	HTTCAD5+	AN14	PE0TX3+
F19	GND	T18	GND	AA22	GND	AP20	GND	K01	HTTCAD6-	AN15	PE0TX4-
F20	GND	T19	GND	AA23	GND	AP22	GND	L01	HTTCAD6+	AP15	PE0TX4+
H02	GND	T20	GND	AA34	GND	AP24	GND	K03	HTTCAD7-	AM16	PE0TX5-
H33	GND	T21	GND	AB01	GND	AP26	GND	K02	HTTCAD7+	AN16	PE0TX5+
J02	GND	T22	GND	AB02	GND	AP32	GND	U05	HTTCAD8-	AN17	PE0TX6-
K04	GND	T23	GND	AB03	GND	AP33	GND	V05	HTTCAD8+	AP17	PE0TX6+
L02	GND	U02	GND	AB04	GND	E25	GNDAHCK	U03	HTTCAD9-	AM18	PE0TX7-
L33	GND	U06	GND	AB05	GND	B10	GNDAHT1	U04	HTTCAD9+	AN18	PE0TX7+
M04	GND	U12	GND	AB06	GND	J03	GNDAHT2	R05	HTTCAD10-	AN19	PE0TX8-
M06	GND	U13	GND	AB12	GND	W31	GNDAPE	T05	HTTCAD10+	AP19	PE0TX8+
M12	GND	U14	GND	AB13	GND	AH16	GNDAPE00	R03	HTTCAD11-	AM20	PE0TX9-
M13	GND	U15	GND	AB14	GND	AJ23	GNDAPE01	R04	HTTCAD11+	AN20	PE0TX9+
M14	GND	U16	GND	AB15	GND	AC30	GNDAPE1	N03	HTTCAD12-	AN21	PE0TX10-
M15	GND	U17	GND	AB16	GND	E28	GNDAVCK	N04	HTTCAD12+	AP21	PE0TX10+
M16	GND	U18	GND	AB17	GND	A25	HCLK-	L05	HTTCAD13-	AM22	PE0TX11-
M17	GND	U19	GND	AB18	GND	B25	HCLK+	M05	HTTCAD13+	AN22	PE0TX11+
M18	GND	U20	GND	AB19	GND	A20	HTRCAD0-	L03	HTTCAD14-	AN23	PE0TX12-
M19	GND	U21	GND	AB20	GND	A21	HTRCAD0+	L04	HTTCAD14+	AP23	PE0TX12+
M20	GND	U22	GND	AB21	GND	B19	HTRCAD1-	J04	HTTCAD15-	AM24	PE0TX13-
M21	GND	U23	GND	AB22	GND	C19	HTRCAD1+	K05	HTTCAD15+	AN24	PE0TX13+
M22	GND	U33	GND	AB23	GND	A18	HTRCAD2-	P03	HTTCLK0-	AN25	PE0TX14-
M23	GND	V04	GND	AB32	GND	A19	HTRCAD2+	P02	HTTCLK0+	AP25	PE0TX14+
N02	GND	V12	GND	AC12	GND	B17	HTRCAD3-	N05	HTTCLK1-	AM26	PE0TX15-
N06	GND	V13	GND	AC13	GND	C17	HTRCAD3+	P05	HTTCLK1+	AN26	PE0TX15+
N12	GND	V14	GND	AC14	GND	B15	HTRCAD4-	H01	HTTCTL-	AE31	PE1COMP0
N13	GND	V15	GND	AC15	GND	C15	HTRCAD4+	J01	HTTCTL+	AD32	PE1REXT0
N14	GND	V16	GND	AC16	GND	A14	HTRCAD5-	AP09	INTR#	AG33	PE1RX0-
N15	GND	V17	GND	AC17	GND	A15	HTRCAD5+	AJ13	PE0COMP0	AG32	PE1RX0+
N16	GND	V18	GND	AC18	GND	B13	HTRCAD6-	AJ19	PE0COMP1	AE33	PE1RX1-
N17	GND	V19	GND	AC19	GND	C13	HTRCAD6+	AJ15	PE0REXT0	AE32	PE1RX1+
N18	GND	V20	GND	AC20	GND	A12	HTRCAD7-	AJ21	PE0REXT1	AC33	PE1RX2-
N19	GND	V21	GND	AC21	GND	A13	HTRCAD7+	AL11	PE0RX0-	AC32	PE1RX2+
N20	GND	V22	GND	AC22	GND	D20	HTRCAD8-	AM11	PE0RX0+	AA33	PE1RX3-
N21	GND	V23	GND	AC23	GND	C20	HTRCAD8+	AJ12	PE0RX1-	AA32	PE1RX3+
N22	GND	V32	GND	AC34	GND	E19	HTRCAD9-	AK12	PE0RX1+	AF34	PE1TX0-
N23	GND	W02	GND	AD24	GND	E20	HTRCAD9+	AL13	PE0RX2-	AF33	PE1TX0+
P04	GND	W12	GND	AD31	GND	D18	HTRCAD10-	AM13	PE0RX2+	AD34	PE1TX1-
P12	GND	W13	GND	AE34	GND	C18	HTRCAD10+	AJ14	PE0RX3-	AD33	PE1TX1+
P13	GND	W14	GND	AF32	GND	E17	HTRCAD11-	AK14	PE0RX3+	AB34	PE1TX2-
P14	GND	W15	GND	AG34	GND	E18	HTRCAD11+	AL15	PE0RX4-	AB33	PE1TX2+
P15	GND	W16	GND	AJ25	GND	E15	HTRCAD12-	AM15	PE0RX4+	Y34	PE1TX3-
P16	GND	W17	GND	AJ28	GND	E16	HTRCAD12+	AJ16	PE0RX5-	Y33	PE1TX3+
P17	GND	W18	GND	AK13	GND	D14	HTRCAD13-	AK16	PE0RX5+	W34	PECLK-
P18	GND	W19	GND	AK15	GND	C14	HTRCAD13+	AL17	PE0RX6-	W33	PECLK+
P19	GND	W20	GND	AK17	GND	E13	HTRCAD14-	AM17	PE0RX6+	AP08	PEDET
P20	GND	W21	GND	AK19	GND	E14	HTRCAD14+	AJ18	PE0RX7-	F34	PEHPSCI#
P21	GND	W22	GND	AK21	GND	D12	HTRCAD15-	AK18	PE0RX7+	F33	PEPMESCI#
P22	GND	W23	GND	AK23	GND	C12	HTRCAD15+	AL19	PE0RX8-	G34	PEWAKE#
P23	GND	Y12	GND	AK25	GND	A16	HTRCLK0-	AM19	PE0RX8+	G32	PWROK

Table 4. Pin List Continued (Listed by Pin Name)

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
H32	RESET#	F21	VCC12HT	AA02	VCC12HT	AE18	VCC15	V30	VCC15VL	AL08	VCC33PE
G33	SUSST#	E22	VCC12HT	AA03	VCC12HT	AE19	VCC15	V31	VCC15VL	AL09	VCC33PE
D34	TCLK	E23	VCC12HT	AA04	VCC12HT	AE20	VCC15	W24	VCC33PE	AL27	VCC33PE
B28	TCLK600	E24	VCC12HT	AA05	VCC12HT	AE21	VCC15	W29	VCC33PE	AL28	VCC33PE
E32	TESTIN#	F01	VCC12HT	AA06	VCC12HT	AE22	VCC15	W30	VCC33PE	AL31	VCC33PE
K34	UPCMD	F02	VCC12HT	A29	VCC15	AE23	VCC15	Y24	VCC33PE	AL32	VCC33PE
N32	UPSTB-	F03	VCC12HT	B29	VCC15	AE24	VCC15	Y29	VCC33PE	AL33	VCC33PE
M32	UPSTB+	F04	VCC12HT	C29	VCC15	AE25	VCC15	Y30	VCC33PE	AL34	VCC33PE
R33	VBE#	F05	VCC12HT	D29	VCC15	A30	VCC15VL	Y31	VCC33PE	AM05	VCC33PE
A02	VCC12HT	F06	VCC12HT	E29	VCC15	A31	VCC15VL	AA24	VCC33PE	AM06	VCC33PE
A03	VCC12HT	F07	VCC12HT	F26	VCC15	A32	VCC15VL	AA29	VCC33PE	AM07	VCC33PE
A04	VCC12HT	F08	VCC12HT	F27	VCC15	A33	VCC15VL	AA30	VCC33PE	AM08	VCC33PE
A05	VCC12HT	F09	VCC12HT	F28	VCC15	A34	VCC15VL	AA31	VCC33PE	AM27	VCC33PE
A06	VCC12HT	F10	VCC12HT	F29	VCC15	B30	VCC15VL	AB24	VCC33PE	AM28	VCC33PE
A07	VCC12HT	F11	VCC12HT	G29	VCC15	B31	VCC15VL	AB29	VCC33PE	AM29	VCC33PE
A22	VCC12HT	F12	VCC12HT	H29	VCC15	B32	VCC15VL	AB30	VCC33PE	AM32	VCC33PE
A23	VCC12HT	F13	VCC12HT	J29	VCC15	B33	VCC15VL	AB31	VCC33PE	AM33	VCC33PE
A24	VCC12HT	F16	VCC12HT	K10	VCC15	B34	VCC15VL	AC24	VCC33PE	AM34	VCC33PE
B01	VCC12HT	F17	VCC12HT	K11	VCC15	C30	VCC15VL	AC29	VCC33PE	AN04	VCC33PE
B02	VCC12HT	F18	VCC12HT	K12	VCC15	C31	VCC15VL	AD12	VCC33PE	AN05	VCC33PE
B03	VCC12HT	F21	VCC12HT	K13	VCC15	C32	VCC15VL	AD13	VCC33PE	AN06	VCC33PE
B04	VCC12HT	F22	VCC12HT	K14	VCC15	C33	VCC15VL	AD14	VCC33PE	AN07	VCC33PE
B05	VCC12HT	F23	VCC12HT	K15	VCC15	C34	VCC15VL	AD15	VCC33PE	AN27	VCC33PE
B06	VCC12HT	F24	VCC12HT	K16	VCC15	D30	VCC15VL	AD16	VCC33PE	AN28	VCC33PE
B07	VCC12HT	F25	VCC12HT	K17	VCC15	D31	VCC15VL	AD17	VCC33PE	AN29	VCC33PE
B08	VCC12HT	G01	VCC12HT	K18	VCC15	D32	VCC15VL	AD18	VCC33PE	AN30	VCC33PE
B21	VCC12HT	G02	VCC12HT	K19	VCC15	D33	VCC15VL	AD19	VCC33PE	AN33	VCC33PE
B22	VCC12HT	G03	VCC12HT	K20	VCC15	E30	VCC15VL	AD20	VCC33PE	AN34	VCC33PE
B23	VCC12HT	G04	VCC12HT	K21	VCC15	E31	VCC15VL	AD21	VCC33PE	AP03	VCC33PE
B24	VCC12HT	G05	VCC12HT	K22	VCC15	F30	VCC15VL	AD22	VCC33PE	AP04	VCC33PE
C01	VCC12HT	G06	VCC12HT	K23	VCC15	F31	VCC15VL	AD23	VCC33PE	AP05	VCC33PE
C02	VCC12HT	H04	VCC12HT	K24	VCC15	G30	VCC15VL	AD29	VCC33PE	AP06	VCC33PE
C03	VCC12HT	H05	VCC12HT	K25	VCC15	G31	VCC15VL	AE29	VCC33PE	AP07	VCC33PE
C04	VCC12HT	H06	VCC12HT	K29	VCC15	H30	VCC15VL	AE30	VCC33PE	AP27	VCC33PE
C05	VCC12HT	J05	VCC12HT	L10	VCC15	H31	VCC15VL	AF29	VCC33PE	AP28	VCC33PE
C06	VCC12HT	J06	VCC12HT	L25	VCC15	J30	VCC15VL	AF30	VCC33PE	AP29	VCC33PE
C07	VCC12HT	K06	VCC12HT	L29	VCC15	J31	VCC15VL	AF31	VCC33PE	AP30	VCC33PE
C08	VCC12HT	L06	VCC12HT	M10	VCC15	K30	VCC15VL	AG29	VCC33PE	AP31	VCC33PE
C09	VCC12HT	L11	VCC12HT	M25	VCC15	K31	VCC15VL	AG30	VCC33PE	AP34	VCC33PE
C10	VCC12HT	L12	VCC12HT	N10	VCC15	L21	VCC15VL	AG31	VCC33PE	D25	VCCA33HCK
C21	VCC12HT	L13	VCC12HT	N25	VCC15	L22	VCC15VL	AH29	VCC33PE	A10	VCCA33HT1
C22	VCC12HT	L14	VCC12HT	P10	VCC15	L23	VCC15VL	AH30	VCC33PE	H03	VCCA33HT2
C23	VCC12HT	L15	VCC12HT	P25	VCC15	L24	VCC15VL	AH31	VCC33PE	W32	VCCA33PE
C24	VCC12HT	L16	VCC12HT	R10	VCC15	L30	VCC15VL	AH32	VCC33PE	AH15	VCCA33PE00
D01	VCC12HT	L17	VCC12HT	R25	VCC15	L31	VCC15VL	AH33	VCC33PE	AH22	VCCA33PE01
D02	VCC12HT	L18	VCC12HT	T10	VCC15	M24	VCC15VL	AH34	VCC33PE	AC31	VCCA33PE1
D03	VCC12HT	L19	VCC12HT	T25	VCC15	M29	VCC15VL	AJ07	VCC33PE	D28	VCCA33VCK
D04	VCC12HT	L20	VCC12HT	U10	VCC15	M30	VCC15VL	AJ08	VCC33PE	C28	VCLK
D05	VCC12HT	M11	VCC12HT	U25	VCC15	M31	VCC15VL	AJ09	VCC33PE	P34	VD0
D06	VCC12HT	N11	VCC12HT	V10	VCC15	N24	VCC15VL	AJ10	VCC33PE	R34	VD1
D07	VCC12HT	P06	VCC12HT	V25	VCC15	N29	VCC15VL	AJ27	VCC33PE	M33	VD2
D08	VCC12HT	P11	VCC12HT	W10	VCC15	N30	VCC15VL	AJ29	VCC33PE	L32	VD3
D09	VCC12HT	R06	VCC12HT	W25	VCC15	N31	VCC15VL	AJ30	VCC33PE	T32	VD4
D10	VCC12HT	R11	VCC12HT	Y10	VCC15	P24	VCC15VL	AJ31	VCC33PE	R32	VD5
D11	VCC12HT	T11	VCC12HT	Y25	VCC15	P29	VCC15VL	AJ32	VCC33PE	K33	VD6
D21	VCC12HT	U11	VCC12HT	AA10	VCC15	P30	VCC15VL	AJ33	VCC33PE	L34	VD7
D22	VCC12HT	V06	VCC12HT	AA25	VCC15	P31	VCC15VL	AJ34	VCC33PE	T33	VD8
D23	VCC12HT	V11	VCC12HT	AB10	VCC15	R24	VCC15VL	AK06	VCC33PE	U32	VD9
D24	VCC12HT	W03	VCC12HT	AB25	VCC15	R29	VCC15VL	AK07	VCC33PE	K32	VD10
E01	VCC12HT	W04	VCC12HT	AC10	VCC15	R30	VCC15VL	AK08	VCC33PE	J32	VD11
E02	VCC12HT	W05	VCC12HT	AC25	VCC15	R31	VCC15VL	AK09	VCC33PE	U34	VD12
E03	VCC12HT	W06	VCC12HT	AD10	VCC15	T24	VCC15VL	AK10	VCC33PE	V33	VD13
E04	VCC12HT	W11	VCC12HT	AD25	VCC15	T29	VCC15VL	AK27	VCC33PE	J34	VD14
E05	VCC12HT	Y01	VCC12HT	AE10	VCC15	T30	VCC15VL	AK30	VCC33PE	J33	VD15
E06	VCC12HT	Y02	VCC12HT	AE11	VCC15	T31	VCC15VL	AK31	VCC33PE	V34	VLCOMPP
E07	VCC12HT	Y03	VCC12HT	AE12	VCC15	U24	VCC15VL	AK32	VCC33PE	P32	VLVREF
E08	VCC12HT	Y04	VCC12HT	AE13	VCC15	U29	VCC15VL	AK33	VCC33PE	T34	VPAR
E09	VCC12HT	Y05	VCC12HT	AE14	VCC15	U30	VCC15VL	AK34	VCC33PE	H34	VSUS15
E10	VCC12HT	Y06	VCC12HT	AE15	VCC15	U31	VCC15VL	AL05	VCC33PE	AH14	VSUS15PE0
E11	VCC12HT	Y11	VCC12HT	AE16	VCC15	V24	VCC15VL	AL06	VCC33PE	AH21	VSUS15PE1
E12	VCC12HT	AA01	VCC12HT	AE17	VCC15	V29	VCC15VL	AL07	VCC33PE	AD30	VSUS15PE2

NC pins: A26-A27, B26, C26-C27, D26-D27, E26, AA11, AB11, AC01-AC06, AC11, AD01-AD06, AD11, AE01-AE06, AF01-AF06, AG01-AG06, AH01-AH06, AJ01-AJ06, AJ11, AK01-AK05, AK11, AL01-AL04, AM01-AM04, AM09-AM10, AN01-AN03, AN08, AN10, AP01-AP02, AP10

Pin Descriptions

HyperTransport Interface

"HyperTransport" Transmit Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
HTTCAD15+/-	K05, J04	O	**Transmit Differential Control / Address / Data Pair 15.**
HTTCAD14+/-	L04, L03	O	**Transmit Differential Control / Address / Data Pair 14.**
HTTCAD13+/-	M05, L05	O	**Transmit Differential Control / Address / Data Pair 13.**
HTTCAD12+/-	N04, N03	O	**Transmit Differential Control / Address / Data Pair 12.**
HTTCAD11+/-	R04, R03	O	**Transmit Differential Control / Address / Data Pair 11.**
HTTCAD10+/-	T05, R05	O	**Transmit Differential Control / Address / Data Pair 10.**
HTTCAD9+/-	U04, U03	O	**Transmit Differential Control / Address / Data Pair 9.**
HTTCAD8+/-	V05, U05	O	**Transmit Differential Control / Address / Data Pair 8.**
HTTCAD7+/-	K02, K03	O	**Transmit Differential Control / Address / Data Pair 7.**
HTTCAD6+/-	L01, K01	O	**Transmit Differential Control / Address / Data Pair 6.**
HTTCAD5+/-	M02, M03	O	**Transmit Differential Control / Address / Data Pair 5.**
HTTCAD4+/-	N01, M01	O	**Transmit Differential Control / Address / Data Pair 4.**
HTTCAD3+/-	R01, P01	O	**Transmit Differential Control / Address / Data Pair 3.**
HTTCAD2+/-	T02, T03	O	**Transmit Differential Control / Address / Data Pair 2.**
HTTCAD1+/-	U01, T01	O	**Transmit Differential Control / Address / Data Pair 1.**
HTTCAD0+/-	V02, V03	O	**Transmit Differential Control / Address / Data Pair 0.**
HTTCLK0+/-	P02, P03	O	**Transmit Differential Clock Pair 0.** Clock for HTTCAD 0-7.
HTTCLK1+/-	P05, N05	O	**Transmit Differential Clock Pair 1.** Clock for HTTCAD 8-15.
HTTCTL+/-	J01, H01	O	**Transmit Differential Control.**

"HyperTransport" Receive Interface			
HTRCAD15+/-	C12, D12	I	**Receive Differential Control / Address / Data Pair 15.**
HTRCAD14+/-	E14, E13	I	**Receive Differential Control / Address / Data Pair 14.**
HTRCAD13+/-	C14, D14	I	**Receive Differential Control / Address / Data Pair 13.**
HTRCAD12+/-	E16, E15	I	**Receive Differential Control / Address / Data Pair 12.**
HTRCAD11+/-	E18, E17	I	**Receive Differential Control / Address / Data Pair 11.**
HTRCAD10+/-	C18, D18	I	**Receive Differential Control / Address / Data Pair 10.**
HTRCAD9+/-	E20, E19	I	**Receive Differential Control / Address / Data Pair 9.**
HTRCAD8+/-	C20, D20	I	**Receive Differential Control / Address / Data Pair 8.**
HTRCAD7+/-	A13, A12	I	**Receive Differential Control / Address / Data Pair 7.**
HTRCAD6+/-	C13, B13	I	**Receive Differential Control / Address / Data Pair 6.**
HTRCAD5+/-	A15, A14	I	**Receive Differential Control / Address / Data Pair 5.**
HTRCAD4+/-	C15, B15	I	**Receive Differential Control / Address / Data Pair 4.**
HTRCAD3+/-	C17, B17	I	**Receive Differential Control / Address / Data Pair 3.**
HTRCAD2+/-	A19, A18	I	**Receive Differential Control / Address / Data Pair 2.**
HTRCAD1+/-	C19, B19	I	**Receive Differential Control / Address / Data Pair 1.**
HTRCAD0+/-	A21, A20	I	**Receive Differential Control / Address / Data Pair 0.**
HTRCLK0+/-	A17, A16	I	**Receive Differential Clock Pair 0.** Clock for HTRCAD 0-7.
HTRCLK1+/-	C16, D16	I	**Receive Differential Clock Pair 1.** Clock for HTRCAD 8-15.
HTRCTL+/-	C11, B11	I	**Receive Differential Control.**

"HyperTransport" Control			
HTSTOPO#	W01	O	**HyperTransport Output.** Connect to LDT stop pin of K8 CPU. 2.5V pull-up.
HTSTOPI#	V01	I	**HyperTransport Stop.** Connect to South Bridge SLP# pin.

"Transmit" pins should be connected to the K8 CPU "In" pins. "Receive" pins should be connected to the K8 CPU "Out" pins. See the HyperTransport specs and the specs for the K8 CPU models to be supported for additional information.

PCI Express Pin Descriptions

PCI Express (PCI-E) Port 0 Receive Channel			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PE0RX15+ **PE0RX15–**	AK26 AJ26	I	**PCI Express Port 0 Receive Data 15.**
PE0RX14+ **PE0RX14–**	AM25 AL25	I	**PCI Express Port 0 Receive Data 14.**
PE0RX13+ **PE0RX13–**	AK24 AJ24	I	**PCI Express Port 0 Receive Data 13.**
PE0RX12+ **PE0RX12–**	AM23 AL23	I	**PCI Express Port 0 Receive Data 12.**
PE0RX11+ **PE0RX11–**	AK22 AJ22	I	**PCI Express Port 0 Receive Data 11.**
PE0RX10+ **PE0RX10–**	AM21 AL21	I	**PCI Express Port 0 Receive Data 10.**
PE0RX9+ **PE0RX9–**	AK20 AJ20	I	**PCI Express Port 0 Receive Data 9.**
PE0RX8+ **PE0RX8–**	AM19 AL19	I	**PCI Express Port 0 Receive Data 8.**
PE0RX7+ **PE0RX7–**	AK18 AJ18	I	**PCI Express Port 0 Receive Data 7.**
PE0RX6+ **PE0RX6–**	AM17 AL17	I	**PCI Express Port 0 Receive Data 6.**
PE0RX5+ **PE0RX5–**	AK16 AJ16	I	**PCI Express Port 0 Receive Data 5.**
PE0RX4+ **PE0RX4–**	AM15 AL15	I	**PCI Express Port 0 Receive Data 4.**
PE0RX3+ **PE0RX3–**	AK14 AJ14	I	**PCI Express Port 0 Receive Data 3.**
PE0RX2+ **PE0RX2–**	AM13 AL13	I	**PCI Express Port 0 Receive Data 2.**
PE0RX1+ **PE0RX1–**	AK12 AJ12	I	**PCI Express Port 0 Receive Data 1.**
PE0RX0+ **PE0RX0–**	AM11 AL11	I	**PCI Express Port 0 Receive Data 0.**

Note: I/O pads for all pins in the table above are powered by VCC33PE.

PCI Express (PCI-E) Port 0 Transmit Channel			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PE0TX15+ **PE0TX15–**	AN26 AM26	O	**PCI Express Port 0 Transmit Data 15.**
PE0TX14+ **PE0TX14–**	AP25 AN25	O	**PCI Express Port 0 Transmit Data 14.**
PE0TX13+ **PE0TX13–**	AN24 AM24	O	**PCI Express Port 0 Transmit Data 13.**
PE0TX12+ **PE0TX12–**	AP23 AN23	O	**PCI Express Port 0 Transmit Data 12.**
PE0TX11+ **PE0TX11–**	AN22 AM22	O	**PCI Express Port 0 Transmit Data 11.**
PE0TX10+ **PE0TX10–**	AP21 AN21	O	**PCI Express Port 0 Transmit Data 10.**
PE0TX9+ **PE0TX9–**	AN20 AM20	O	**PCI Express Port 0 Transmit Data 9.**
PE0TX8+ **PE0TX8–**	AP19 AN19	O	**PCI Express Port 0 Transmit Data 8.**
PE0TX7+ **PE0TX7–**	AN18 AM18	O	**PCI Express Port 0 Transmit Data 7.**
PE0TX6+ **PE0TX6–**	AP17 AN17	O	**PCI Express Port 0 Transmit Data 6.**
PE0TX5+ **PE0TX5–**	AN16 AM16	O	**PCI Express Port 0 Transmit Data 5.**
PE0TX4+ **PE0TX4–**	AP15 AN15	O	**PCI Express Port 0 Transmit Data 4.**
PE0TX3+ **PE0TX3–**	AN14 AM14	O	**PCI Express Port 0 Transmit Data 3.**
PE0TX2+ **PE0TX2–**	AP13 AN13	O	**PCI Express Port 0 Transmit Data 2.**
PE0TX1+ **PE0TX1–**	AN12 AM12	O	**PCI Express Port 0 Transmit Data 1.**
PE0TX0+ **PE0TX0–**	AP11 AN11	O	**PCI Express Port 0 Transmit Data 0.**

Note: I/O pads for all pins in the table above are powered by VCC33PE.

PCI Express (PCI-E) Port 1			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PE1RX0+ **PE1RX0–**	AG32 AG33	I	**PCI Express Port 1 Receive Data.**
PE1TX0+ **PE1TX0–**	AF33 AF34	O	**PCI Express Port 1 Transmit Data.**

PCI Express (PCI-E) Port 2			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PE1RX1+ **PE1RX1–**	AE32 AE33	I	**PCI Express Port 2 Receive Data.**
PE1TX1+ **PE1TX1–**	AD33 AD34	O	**PCI Express Port 2 Transmit Data.**

PCI Express (PCI-E) Port 3			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PE1RX2+ **PE1RX2–**	AC32 AC33	I	**PCI Express Port 3 Receive Data.**
PE1TX2+ **PE1TX2–**	AB33 AB34	O	**PCI Express Port 3 Transmit Data.**

PCI Express (PCI-E) Port 4			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PE1RX3+ **PE1RX3–**	AA32 AA33	I	**PCI Express Port 4 Receive Data.**
PE1TX3+ **PE1TX3–**	Y33 Y34	O	**PCI Express Port 4 Transmit Data.**

Note: I/O pads for all pins in the table above are powered by VCC33PE.

Ultra V-Link Interface

Ultra V-Link Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VD[15:0]	J33, J34 V33, U34 J32, K32 U32, T33 L34, K33 R32, T32 L32, M33 R34, P34	IO	**V-Link Address / Data Bus.** Used to transfer data between the North Bridge and the South Bridge.
VPAR	T34	IO	**Parity.**
VBE#	R33	IO	**Byte Enable.**
UPCMD	K34	I	**Command from Client (South Bridge) to Host (North Bridge).**
UPSTB+	M32	I	**Strobe from Client to Host.**
UPSTB-	N32	I	**Complement Strobe from Client to Host.**
DNCMD	M34	O	**Command from Host (North Bridge) to Client (South Bridge).**
DNSTB+	N34	O	**Strobe from Host to Client.**
DNSTB-	N33	O	**Complement Strobe from Host to Client.**

Clock, Control and Test Pins

Clock, Reset, Power Control and Test			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VCLK	C28	I	**V-Link Clock.** This pin receives the 66 MHz clock used to generate the internal clocks required by V-Link interface between the North Bridge and South Bridge.
HCLK+ **HCLK–**	B25 A25	I	**Host Differential Clock.** These pins receive the host CPU clock (200 MHz) used by all K8T890 logic that is in the host CPU domain.
PECLK+ **PECLK–**	W33 W34	I	**PCI Express Differential Clock.** These pins receive the 100 MHz clock used by the internal PCI Express logic. Multiplied up to 2.5 GHz on-chip for use by the integrated PCI Express PHY to transmit / receive data.
RESET#	H32	I	**Reset.** Input from the South Bridge chip. When asserted, this signal resets the K8T890 and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options.
PWROK	G32	I	**Power OK.** Driven by South Bridge PWROK output from the power supply PWRGOOD input to the South Bridge.
SUSST#	G33	I	**Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pull-up to disable.
PEWAKE#	G34	OD	**PCI Express Wake.** Indicates that a system wake event has occurred on the PCI Express bus. Used to waken the chip from deep sleep mode (S3 / S4 / S5 states). Wire-OR with other system WAKE# signals (including PEWAKE# on the PCI Express bus connector) and connect to the South Bridge PME input. Please refer to K8T890 Design Guide for further details.
PEPMESCI#	F33	OD	**PCI Express PME SCI.** System Control Interrupt to indicate Power Management Event. Connect to South Bridge SCI input (GPIO pin). This pin connects to an external 3.3V suspend power pull-up through a 4.7K-ohm resistor.
PEHPSCI#	F34	OD	**PCI Express Hot-Plug SCI.** System Control Interrupt to indicate Hot Plug occurred. Connect to South Bridge SCI input (GPIO pin). This pin connects to an external 3.3V suspend power pull-up through a 4.7K-ohm resistor.
INTR#	AP9	OD	**PCI Express Interrupt.** Connect to South Bridge interrupt input to indicate that an interrupt condition was detected on PCI Express bus or the internal APIC.
BUSY#	E34	O	**Busy.** Indicates that master cycles are pending in the chip. Used by the power management system to avoid changing the system power state while a master cycle is in progress.
PEDET	AP8	I	**PCI Express Detect.** Used to determine the presence of an external PCI Express device.
TESTIN#	E32	I	**Test In.** This pin is used for testing and must be tied high on all board designs. See Design Guide.
DFTIN#	F32	I	**DFT In.** This pin is used for testing and must be connected to 1.5V through a 4.7K ohm resistor for all board designs.
TCLK	D34	I	**Test Clock.** This pin is used for testing. It is internally pulled high for all board designs.
TCLK600	B28	I	**Test Clock Input.**
DEBUG	A28	I	**Debug.**
NC	(see pin list)		**No Connect.**

Reference Voltages, Compensation, Power and Ground Pins

Reference Voltages			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VLVREF	P32	P	**V-Link Voltage Reference.** Derived using a resistive voltage divider. See Design Guide for details.

Compensation			
Signal Name	**Pin #**	**I/O**	**Signal Description**
HTRCOMPP	B09	AI	**Host CPU P-Channel Compensation.** Connect 50 Ω 1% resistor to GND.
HTRCOMPN	A09	AI	**Host CPU N-Channel Compensation.** Connect 50 Ω 1% resistor to VCC12HT.
HTRTCOMP	A08	AI	**Host CPU Compensation.** Connect 100 Ω 1% resistor to VCC12HT.
VLCOMPP	V34	AI	**V-Link P-Channel Compensation.** See Design Guide.
PE0COMP0	AJ13	AI	**PCI Express Port 0 Compensation 0.** See Design Guide.
PE0REXT0	AJ15	AI	**PCI Express Port 0 External Resistor 0.** See Design Guide.
PE0COMP1	AJ19	AI	**PCI Express Port 0 Compensation 1.** See Design Guide.
PE0REXT1	AJ21	AI	**PCI Express Port 0 External Resistor 1.** See Design Guide.
PE1COMP0	AE31	AI	**PCI Express Port 1-4 Compensation 0.** See Design Guide.
PE1REXT0	AD32	AI	**PCI Express Port 1-4 External Resistor 0.** See Design Guide.

Analog Power Descriptions

Analog Power / Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VCCA33HT2 **VCCA33HT1**	H03 A10	P	**Analog Power for HT Transmit / Receive.** 3.3V ±5%. Connect through a ferrite bead for isolation of digital switching noise.
GNDAHT2 **GNDAHT1**	J03 B10	P	**Analog Ground for HT Transmit / Receive.** Connect to main ground plane through a ferrite bead for isolation of digital switching noise.
VCC33HCK	D25	P	**Analog Power for Host Clock.** 3.3V ±5%.
GNDAHCK	E25	P	**Analog Ground for Host Clock.**
VCCA33VCK	D28	P	**Power for V-Link Clock PLL (3.3V ±5%).**
GNDAVCK	E28	P	**Ground for V-Link Clock PLL.**
VCCA33PE00	AH15	P	**Power for PCI Express Port 0 Clock PLL 0** (3.3V ±5%). For PE0[7:0].
GNDAPE00	AH16	P	**Ground for PCI Express Port 0 Clock PLL 0.** Connect to main ground plane through a ferrite bead.
VCCA33PE01	AH22	P	**Power for PCI Express Port 0 Clock PLL 1** (3.3V ±5%). For PE0[15:8].
GNDAPE01	AJ23	P	**Ground for PCI Express Port 0 Clock PLL 1.** Connect to main ground plane through a ferrite bead.
VCCA33PE1	AC31	P	**Power for PCI Express Port 1-4 Clock PLL** (3.3V ±5%). For PE1[3:0].
GNDAPE1	AC30	P	**Ground for PCI Express Port 1-4 Clock PLL.** Connect to main ground plane through a ferrite bead.
VCCA33PE	W32	P	**Power for PCI Express Clock PLL** (3.3V ±5%). For PECLK clock synthesizer.
GNDAPE	W31	P	**Ground for PCI Express Clock PLL.** Connect to main ground plane through a ferrite bead.

Digital Power Pin Descriptions

Digital Power / Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VCC12HT	(see pin lists)	P	**Power for HyperTransport I/O Interface Logic.** Voltage is HT Interface dependent (typically 1.2V).
VCC15	(see pin lists)	P	**Power for All Other Internal Logic.** 1.5V ±5%
VCC15VL	(see pin lists)	P	**Power for V-Link I/O Interface Logic.** 1.5V ±5%
VCC33PE	(see pin lists)	P	**Power for PCI-E I/O Interface Logic. 3.3V ±5% (PCI-E Port)**
VSUS15	H34	P	**Suspend Power.** 1.5V ±5%. Used to sustain the on-chip 256-byte SRAM.
VSUS15PE2 **VSUS15PE1** **VSUS15PE0**	AD30 AH21 AH14	P	**PCI Express Suspend Power.** 1.5V ±5%. VSUS15PE0 is for PE0[7:0], VSUS15PE1 is for PE0[15:8] and VSUS15PE2 is for PE1[3:0].
GND	(see pin lists)	P	**Digital Ground.** Connect to main ground plane.

Strap Pins

Strap Pins (External pullup / pulldown straps are required to select "H" / "L")				
Signal	**Actual Strap Pin**	**Function**	**Description**	**Status Bit**
VD7	**VT8235M-CD / CE:** SDCS3# **VT8237R / VT8251:** PDCS3#	Test Mode	L: Disable H: Enable **Pull down for normal operation.** *VD7 is sampled during system initialization; The actual strapping pin is located on the South Bridge chip.*	-
VD6	**VT8235M-CD / CE:** SDA2 **VT8237R / VT8251:** PDA2	Auto-Configure (ROMSIP)	L: Disable H: Enable. **ROMSIP defines the default setup values for certain registers, and keeps those values in the BIOS ROM for system initialization.** *VD6 is sampled during system initialization; The actual strapping pin is located on the South Bridge chip.*	-
VD5	**VT8235M-CD / CE:** SDA1 **VT8237R / VT8251:** PDA1	External Loop Test Mode	L: Disable H: Enable **Pull down for normal operation.** *VD5 is sampled during system initialization; The actual strapping pin is located on the South Bridge chip.*	-
VD4	**VT8235M-CD / CE:** SDA0 **VT8237R / VT8251:** PDA0	No HCLK	L: Use external HCLK H: Enable. (No HCLK) **Not use HCLK+/- as host PLL reference.** *VD4 is sampled during system initialization; The actual strapping pin is located on the South Bridge chip.*	
VD2	**VT8235M-CD:** SA18 **VT8235M-CE:** Strap_VAD2 **VT8237R / VT8251:** GPIOB	HT Bus Width	L: 8-bit H: 16-bit **Must pull down for normal operation.** *VD2 is sampled during system initialization; The actual strapping pin is located on the South Bridge chip.*	-
VD3 VD1 VD0	**VT8235M-CD:** SA19 SA17 SA16 **VT8235M-CE:** Strap_VAD3 Strap_VAD[1:0] **VT8237R / VT8251:** GPIOD GPIOA GPIOC	HT Bus Frequency	LLL: 200MHz (default) others: reserved **Must pull down for normal operation.** *VD[3,1:0] are sampled during system initialization; The actual strapping pin is located on the South Bridge chip.*	-

REGISTER DESCRIPTIONS

Miscellaneous I/O

I/O Port Address: 22h
PCI Arbiter Disable **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**PCI2 Arbiter Control** 0: Enable PCI2 Bus Arbiter 1: Disable PCI2 Bus Arbiter
0	RW	0	**PCI Arbiter Control** 0: Enable PCI Bus Arbiter (arbiter will respond to REQ# assertion) 1: Disable PCI Bus Arbiter (arbiter will not respond to PCI-1 REQ# and PREQ# assertion)

PCI Configuration Space I/O

All north bridge's PCI space registers are addressed via the following configuration mechanism:

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

I/O Port Address: CFB-CF8h
PCI Configuration Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Configuration Space Enable** 0: Disabled 1: Convert configuration data port writes to configuration cycles on the PCI bus
30:24	RO	0	**Reserved** (always reads 0)
23:16	RW	0	**PCI Bus Number** Used to choose a specific PCI bus in the system
15:11	RW	0	**Device Number** Used to choose a specific device in the system
10:8	RW	0	**Function Number** Used to choose a specific function if the selected device supports multiple functions
7:2	RW	0	**Register Number (also called the "Offset")** Used to select a specific DWORD in the configuration space
1:0	RW	0	**Fixed** (always reads 0)

I/O Port Address: CFF-CFCh
PCI Configuration Data **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**PCI Configuration Data**

Note. Refer to PCI Bus Specification Version 2.3 for further details on operation of the above configuration registers.

Device 0 Function 0 (D0F0): Host Controller

Device 0 Function 0, a host controller, is connected to the PCI bus through AD11 as the IDSEL. Registers listed in this section are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 0 and function number 0.

Header Registers (0-3Fh)

Offset Address: 1-0h (D0F0)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 3-2h (D0F0)

Device ID **Default Value: 0238h**

Bit	Attribute	Default	Description
15:0	RO	0238h	**Device ID Code**

Offset Address: 5-4h (D0F0)

PCI Command **Default Value: 0006h**

Bit	Attribute	Default	Description	Mnemonic
15:10	—	0	**Reserved**	
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0. (Disable)	
8	RO	0	**SERR# Enable** Hardwired to 0 (Not supported)	
7	RO	0	**Address / Data Stepping** Hardwired to 0 (Not supported)	
6	RW	0	**Parity Checking** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors	**RPTYERR**
5	RO	0	**VGA Palette Snooping** Hardwired to 0 (Not implemented)	
4	RO	0	**Memory Write and Invalidate** Hardwired to 0 (Not supported)	
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles)	
2	RO	1	**PCI Master Function** Hardwired to 1 (May behave as a bus master)	
1	RO	1	**Memory Space Access** Hardwired to 1 (Responds to memory space access)	
0	RO	0	**I/O Space Access** Hardwired to 0 (Does not respond to I/O space)	

Offset Address: 7-6h (D0F0)

PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detect Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error (SERR#)**
13	RW1C	0	**Set when terminated with Master-Abort, except special cycle** 0: No abort received 1: Transaction aborted by the master
12	RW1C	0	**Set when received a Target-Abort** 0: No abort received 1: Transaction aborted by the target
11	RO	0	**Set when signaled a Target-Abort** NB never signals Target Abort
10-9	RO	01	**DEVSEL# Timing** 00: Fast 01: Medium (default) 10: Slow 11: Reserved
8	RW1C	0	**Set when set or observed SERR# and Parity Error** (see RPTYERR (Rx04[6]) for details) 0: Disable 1: Enable
7	RO	0	**Capable of Accepting fast back-to-back as a target** Hardwired to 0 (Not implemented)
6	RO	0	**User Definable Features** Hardwired to 0
5	RO	0	**66 MHz Capable** Hardwired to 0 (Not implemented)
4	RO	1	**Support New Capability List**
3:0	—	0	**Reserved**

Offset Address: 8h (D0F0)

Revision ID **Default Value: 0nh**

Bit	Attribute	Default	Description
7:0	RO	0nh	**North Bridge Chip Revision Code**

Offset Address: 0B-9h (D0F0)

Class Code **Default Value: 060000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Dh (D0F0)

PCI Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:3	RW	0	**PCI Bus Time Slice for CPU as a Master (in Unit of PCI clocks)**	**MLT [7:3]**
2:0	—	0	**Reserved** MLT[2:1] is programmable; however, it's read as 0	**MLT [2:0]**

Offset Address: 0Eh (D0F0)

Header Type **Default Value: —**

Bit	Attribute	Default	Description
7	RO	—	**Multi-Function Device** 0: if MFUNC (Rx4F[0], the multiple function control bit) is set to 0 1: if MFUNC is set to 1
6:0	RO	0	**Reserved**

Offset Address: 0Fh (D0F0)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**BIST Support** Hardwired to 0 (Not supported)
6:0	RO	0	**Reserved**

Offset Address: 2D-2Ch (D0F0)
Subsystem Vendor ID **Default Value: 00h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F0)
Subsystem ID **Default Value: 00h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 37-34h (D0F0)
Capability Pointer **Default Value: 0000 0080h**

Bit	Attribute	Default	Description
31:0	RO	0000 0080	**Capability List Pointer** An offset address from the start of the configuration space: it is 80h if RGHDR_A is set to 1; else, it will be 50h.

Miscellaneous Control (4F–51h)

Offset Address: 4Fh (D0F0)
Multiple Function Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:1	—	0	**Reserved**	
0	RW	0	**Multi-Function Support** 0: Disable; functions 1, 2, 3, 4, 7 cannot be accessed, and the value returned will be 0FFFFFFFFh when accessed 1: Enable; This bit's setting will be reflected on Rx0E[7]	MFUNC

Offset Address: 50h (D0F0)
Capability ID **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Capability ID**

Offset Address: 51h (D0F0)
Next Pointer **Default Value: 60h**

Bit	Attribute	Default	Description
7:0	RO	60h	**Next Pointer**

K8 Configuration Capability Header (58–5Fh)

Offset Address: 58h (D0F0)
Capability ID **Default Value: 08h**

Bit	Attribute	Default	Description
7:0	RO	08h	**Capability ID = 08h**

Offset Address: 59h (D0F0)
Next Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Next Pointer** Always reads 00h ("Null" Pointer)

Offset Address: 5Ah (D0F0)
Index **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Index**

Offset Address: 5Bh (D0F0)
Capability Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Capability Type**

Offset Address: 5F-5Ch (D0F0)
Data Port **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0000 0000	**Data Port**

HyperTransport Control (60–83h)

Offset Address: 63-60h (D0F0)
Device A (CPU) Link Command **Default Value: 0060 5808h**

Bit	Attribute	Default	Description
31:29	RO	000	**Slave / Primary Interface Type**
28:26	—	000	**Reserved**
25:21	RO	03h	**Unit ID Count** Specifies the number of unit IDs used by the chip (3).
20:16	RW	00h	**Base Unit ID** Specifies the link-protocol base Unit ID. Hardware uses this value to determine the Unit IDs for link request and response packets. When a new value is written to this field, the response includes a Unit ID that is based on the new value in this register.
15:8	RO	58h	**Capabilities Pointer** Capability lists: Rx34 => Rx80 (Capability Pointer) / RxA0 (Non AGP30) => Rx50 (PWD) => Rx60 (LDT) => Rx58 (INT) => ...
7:0	RO	08h	**Capabilities ID** Specifies the capabilities ID for the link configuration space.

Offset Address: 67-64h (D0F0)

Device A Link Configuration Control Register **Default Value: 0011 0000h**

Bit	Attribute	Default	Description
31	–	0	**Reserved**
30:28	RW	0	**Link Width Out** Specifies the operating width of the outgoing link. 000: 8 bits 001: 16 bits 010: -reserved- 011: -reserved- 100: 2 bits 101: 4 bits 110: -reserved- 111: Not connected This field is cleared by PWROK but not by RESET#. The default value of this field depends on the link of width of the connecting device per the link specification. After this field is updated, the link width does not change until either RESET# is asserted or a link disconnect sequence occurs via HTSTOP#.
27	–	0	**Reserved**
26:24	RW	0	**Link Width In** Specifies the operating width of the incoming link. 000: 8 bits 001: 16 bits, LDT Link only 010: -reserved- 011: -reserved- 100: -reserved- 101: -reserved- 110: -reserved- 111: Not connected This field is cleared by PWROK but not by RESET#. The default value of this field depends on the link of width of the connecting device per the link specification. After this field is updated, the link width does not change until either RESET# is asserted or a link disconnect sequence occurs via HTSTOP#.
23	–	0	**Reserved**
22:20	RO	001	**Max Link Width Out** Value indicates 16 bits
19	–	0	**Reserved**
18:16	RO	001	**Max Link Width In** The maximum incoming link width is 16 bits for side A.
15	RO	0	**Reserved**
14	RW	0	**Extended Control Time During Initialization** Specifies the time in which LT[B,A]CTL is held asserted during the initialization sequence that follows the HTSTOP# de-assertion after LR[B,A]CTL is detected as being asserted. This bit is cleared by PWROK but not by RESET#. 0: At least 16 bit times 1: About 50 microseconds

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Offset Address: 67-64 (D0F0)

13	RW	0	**Link TriState Enable** During the HTSTOP# disconnect sequence: 0: Link transmitter signals are driven but in an undefined state. Link receiver signals are assumed to be driven 1: Link transmitter signals are in high impedance state. Receivers are prepared for high-impedance mode, including cutting power to the receiver differential amps and insuring that there are no resultant high-current paths in the circuits. This bit is cleared by PWROK but not by RESET#.
12:10	–	0	**Reserved**
9:8	W1C	00	**CRC Error** Bit-9 applies to the upper byte of the link (Device A:C4h only) and bit-8 applies to the lower byte. These bits are cleared by PWROK but not by RESET#. 0: No CRC error 1: Hardware detected a CRC error on the incoming link Write 1 to clear this bit.
7	RO	0	**Transmitter Off** (not implemented)
6	RO	0	**End of Chain** (not implemented)
5	RO	0	**Initialization Complete** This bit is set by hardware when low-level link initialization completes successfully. If there is no device on the other end of the link, or if the device on the other end of the link is unable to properly perform link initialization, then this bit is not set. This bit is cleared when RESET# is asserted or after the link disconnect sequence completes after the assertion of HTSTOP#.
4	W1C	0	**Link Failure** Set to 1 by hardware when a CRC error is detected on the link (if enabled by bit-1) or if the link is not used in the system. This bit is cleared by PWROK but not by RESET#.
3	RW	0	**CRC Error Command** This bit is intended to be used in test mode only to check the CRC failure detection logic of the device on the other side of the link. 0: Transmitted CRC values match the values calculated per the link specification 1: Link transmission logic generates erroneous CRC values
2	–	0	**Reserved**
1	RW	0	**CRC Flood** 0: CRC errors do not result in sync packets to the outgoing link and do not set the Link Fail bit (bit-4 of this register) 1: CRC errors result in sync packets to the outgoing link and set the Link Fail bit (bit-4 of this register).
0	–	0	**Reserved**

Offset Address: 6B-68h (D0F0)

Subordinate Link Status **Default Value: 0000 00D0h**

Bit	Attribute	Default	Description
31:8	–	00h	**Reserved**
7	RO	1	**Transmitter Off** This bit is hardwired high to indicate that there is no subordinate LDT link.
6	RO	1	**End of HT Chain** This bit is hardwired high to indicate that there is no subordinate LDT link.
5	–	0	**Reserved**
4	RO	1	**Link Failure** This bit is hardwired high to indicate that there is no subordinate LDT link.
3:0	–	0	**Reserved**

Offset Address: 6F-6Ch (D0F0)
Link Side A, between CPU and NB, Frequency Capability **Default Value: 0035 0022h**

Bit	Attribute	Default	Description
31:16	RO	0035h	**Link Side A Frequency Capability** These bits indicate that the A side of the tunnel supports 200, 400, 600 and 800 link frequencies.
15:12	—	0000	**Reserved**
11:8	RW	0000	**Link Side A Frequency** Specifies the link side A frequency. 0000: 200 MHz 0010: 400 MHz 0101: 800 MHz 0111: -reserved 00x1: -reserved- 0100: 600 MHz 0110: -reserved- 1xxx: -reserved- After this field is updated, the link frequency does not change until either RESET# is asserted or a link disconnect sequence occurs via HTSTOP#. The default is set on the rising edge of PWROK (the value is unchanged by RESET#).
7:5	RO	001	**Major Revision**
4:0	RO	2h	**Minor Revision** Bits 7-0 above are hardwired to indicate that the logic was designed to conform to link specification 1.02.

Offset Address: 73-70h (D0F0)
Link Side B Frequency Capability **Default Value: 0000 0002h**

Bit	Attribute	Default	Description
31:16	RO	00h	**Link Side B Frequency Capability**
15:12	—	0000	**Reserved**
11:8	RW	0000	**Link Side B Frequency** Specifies the link side B frequency.
7:0	RO	02h	**Link Device Feature Capability Indicator** Read only. Bit-3 is set to indicate that this device requires CTL to be asserted for 50 us during the initialization sequence as specified in Section 12.2 after HTSTOP# disconnect. Bit-1 is set to indicate that chip HTSTOP# is supported.

Offset Address: 77-74h (D0F0)
Link Enumeration Scratchpad **Default Value: 00h**

Bit	Attribute	Default	Description
31:16	—	0	**Reserved**
15:0	RW	0000h	**Enumeration Scratchpad** These bits are reserved for use by software and control no on-chip logic. These bits are cleared by PWROK but are unaffected by RESET#.

Offset Address: 7Ch (D0F0)
CPU Miscellaneous Control **Default Value: 08h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3	RW	1	**CPU Fast Command** This register is cleared only by cold reset and effect on the next warm reset or link frequency change by HTSTOP#.
2:0	RW	000	**LTXPLL Feed Back Delay Fine Tune** These registers are only cleared only by cold reset and effect on the next warm reset or link frequency change by HTSTOP#.

Offset Address: CAPPTR (D0F0 83-80h)
Capability Pointer **Default Value: 0000 5002h**

Bit	Attribute	Default	Description
31:16	—	0	**Reserved**
15:8	R-IW	50h	**Pointer to Next Item**
7:0	R-IW	02h	**Capability ID**

Extended Configuration Space Access Capability (E0–F0h)

Offset Address: E3-E0h (D0F0)

HyperTransport I/O Spec Rev 1.05 Extended Capability – First DW **Default Value: 9800 0008h**

Bit	Attribute	Default	Description
31:27	RO	13h	**Capability Type**
26:16	—	0	**Reserved**
15:8	RO	00	**Capability Next pointer**
7:0	RO	08h	**Capability ID**

Offset Address: E7-E4h (D0F0)

HyperTransport I/O Spec Rev 1.05 Extended Capability – Second DW **Default Value: 0000 0000h**

RxE7-E4 are used to specify a device register to be accessed through reading or writing RxEB-E8.

Bit	Attribute	Default	Description
31:29	—	0	**Reserved**
28	RW	0	**Configuration Type to be Accessed**
27:20	RW	0	**Bus Number to be Accessed**
19:15	RW	0	**Device Number to be Accessed**
14:12	RW	000	**Function Number to be Accessed**
11:2	RW	0	**Register Number to be Accessed**
1:0	—	0	**Reserved**

Offset Address: EB-E8h (D0F0)

HyperTransport I/O Spec Rev 1.05 Extended Capability – Third DW **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Data Port** Read/Write to this register will result in a configuration access to the device and registers specified by RxE7~ RxE4

Offset Address: F0h (D0F0)

PSTATECTL Pulse Width Counter **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**PSTATECTL Pulse Width Counter (LCLK domain)**

Device 0 Function 0 (D0F0) – Extended Space

Virtual Channel Capability (140–14Fh)

Virtual Channel Capability is defined for Egress direction of the device, including TC/VC mapping, VC arbitration and Port arbitration. Hardware Round-Robin arbitration scheme is applied in both Port and VC arbitration. By default, TC0 is mapped to VC0 while TC1, TC2, TC3, TC4, TC5, TC6 and TC7 are mapped to VC1.

Offset Address: 143-140h (D0F0)
Virtual Channel Enhanced Capability Header **Default Value: 0001 0002h**

Bit	Attribute	Default	Description
31:20	RO	0	**Next Capability Offset**
19:16	RO	1	**Capability Version**
15:0	RO	2h	**PCI Express Extended Capability ID**

Offset Address: 147-144h (D0F0)
Port VC Capability Register 1 **Default Value: 0000 0400h**

Bit	Attribute	Default	Description
31:12	—	0	**Reserved**
11:10	RO	01	**Port Arbitration Table Entry Size** 01: Arbitration entry size is 2 bits.
9:8	RO	0	**Reference Clock**
7	—	0	**Reserved**
6:4	RO	0	**Low Priority Extended VC Count**
3	—	0	**Reserved**
2:0	RO	0	**Extended VC Count**

Offset Address: 14B-148h (D0F0)
Port VC Capability Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
31:24	RO	0	**VC Arbitration Table Offset.** Table is not implemented.
23:8	—	0	**Reserved**
7:0	RO	0	**VC Arbitration Capability**

Offset Address: 14D-14Ch (D0F0)
Port VC Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
15:4	—	0	**Reserved**
3:1	RO	0	**VC Arbitration Select**
0	RO	0	**Load VC Arbitration Table**

Offset Address: 14F-14Eh (D0F0)
Port VC Status Register **Default Value: 00h**

Bit	Attribute	Default	Description
15:1	—	0	**Reserved**
0	RO	0	**VC Arbitration Table Status (TL)** Reserved

VC0 Resource Registers (150–15Bh)

Offset Address: 153-150h (D0F0)
VC Resource Capability Register (VC0) **Default Value: 0000 0001h**

Bit	Attribute	Default	Description
31:24	RO	0	**Port Arbitration Table Offset (VC0)** Table is not implemented.
23	—	0	**Reserved**
22:16	RO	0	**Maximum Time Slots (TL)** Reserved
15	RO	0	**Reject Snoop Transactions** Reserved
14	RO	0	**Advanced Packet Switching** Reserved
13:8	—	0	**Reserved**
7:0	RO	01	**Port Arbitration Capability** 01: Non-configurable fixed hardware-fixed Round Robin arbitration scheme.

Offset Address: 157-154h (D0F0)
VC Resource Control Register (VC0) **Default Value: 8002 00FFh**

Bit	Attribute	Default	Description
31	RO	1	**VC Enable**
30:27	—	0	**Reserved**
26:24	RO	0	**VC ID**
23:20	—	0	**Reserved**
19:17	RW	001	**Port Arbitration Select** 01: Non-configurable fixed hardware-fixed Round Robin arbitration scheme
16	RO	0	**Load Port Arbitration Table**
15:8	—	0	**Reserved**
7:0	RW Bit 0: RO	0FFh	**TC/VC Mapping** This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC0 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0 (by software). Note: Bit0 is hardwired to 1 (i.e. TC0 is always mapped to VC0).

Offset Address: 15B-158h (D0F0)
VC Resource Status Register (VC0) **Default Value: 00h**

Bit	Attribute	Default	Description
31:18	—	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)** This bit indicates whether the Virtual Channel negotiation is in Pending state (set/clear by hardware) 0: Negotiation is complete 1: Negotiation is on-going.
16	RO	0	**Port Arbitration Table Status (TL)** Reserved
15:0	—	0	**Reserved**

VC1 Resource Registers (15C–16Fh)

The following registers exist only when Rx144[0] is programmed to 1. If Rx144[0]=0, all the following registers will be read as 0.

Offset Address: 15F-15Ch (D0F0)

VC Resource Capability Register (VC1) **Default Value: 1000 001Fh**

Bit	Attribute	Default	Description
31:24	RO	10	**Port Arbitration Table Offset (VC1)**
23	—	0	**Reserved**
22:16	RO	0	**Maximum Time Slots (TL)** Reserved
15	RO	0	**Reject Snoop Transaction**
14	RO	0	**Advanced Packet Switching** Reserved
13:8	—	0	**Reserved**
7:0	RO	1F	**Port Arbitration Capability** Supported Time-based WRR up to 128 phases

Offset Address: 163-160h (D0F0)

VC Resource Capability Register (VC1) **Default Value: 0102 0000h**

Bit	Attribute	Default	Description
31	RO	0	**VC Enable**
30:27	—	0	**Reserved**
26:24	RW	1	**VC ID**
23:20	—	0	**Reserved**
19:17	RW	1	**Port Arbitration Select** 01: Non-configurable fixed hardware-fixed Round Robin arbitration scheme
16	RO	0	**Load Port Arbitration Table**
15:8	—	0	**Reserved**
7:0	RW Bit 0: RO	0FFh	**TC/VC Mapping** This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC0 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0 (by software). Note: Bit0 is hardwired to 1 (i.e. TC0 is always mapped to VC0).

Offset Address: 167-164h (D0F0)

VC Resource Status Register (VC1) **Default Value: 00h**

Bit	Attribute	Default	Description
31:18	—	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)**
16	RO	0	**Port Arbitration Table Status (TL)** Reserved
15:0	—	0	**Reserved**

Virtual Channel Port Arbitration Table for VC1 (180–19Fh)

Offset Address: 19F-180h (D0F0)

VC1 Port Arbitration Table **Default Value: 00h**

Bit	Attribute	Default	Description
255:254	RW	0	**Phase 127** 00: Time slot to Port 0 01: Time slot to Port 0 10: Time slot to Port 1 11: Time slot to Port 2 **Note: The above time slot assignment applies to Phase 0 – Phase 127 of the VCI Port Arbitration Table.**
2N+1 : 2N	RW	0	Phase N, where 0< N <127
1:0	RW	0	Phase 0

VC Arbitration Timer (200–209h)

PCI Express arbitration scheme is based on the same scheme used in the DRAM Controller. A timer named as Occupancy Timer is used to guarantee the number of time slots one requester will be granted when there is no high priority requesters come in. Another timer named as Promote Timer is used for a requester to upgrade its requests to high priority if it is not served after the Promote Timer times out. However, priority request promoted by the expiration of the Promote Timer will be served once only.

Offset Address: 200h (D0F0)

VC0 Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**VC0 Occupancy Timer (in unit of 125MHz)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 201h (D0F0)

VC0 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**VC0 Promote Timer (in unit of 125MHz)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

Offset Address: 202h (D0F0)

VC1 Port Arbitration Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**VC1 Occupancy Timer (in unit of 125MHz)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 203h (D0F0)

VC1 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**VC1 Promote Timer (in unit of 125MHz)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

Note: Port arbitration timers defined by registers 202h and 203h are not applicable in current VC1 implementation; currently the VC1 arbitration is in strict priority.

Port Arbitration Timer for VC0 (210–229h)

Offset Address: 210h (D0F0)

Root Port 0 (x16) Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Occupancy Timer (in unit of 125MHz)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 211h (D0F0)
Root Port 0 (x16) Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Promote Timer (in unit of 125MHz)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

Offset Address: 212h (D0F0)
Root Port 1 (x4) Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Occupancy Timer (in unit of 125MHz)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 213h (D0F0)
Root Port 1 (x4) Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Promote Timer (in unit of 125MHz)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

Offset Address: 214h (D0F0)
PE1 Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Occupancy Timer (in unit of 125MHz)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 215h (D0F0)
PE1 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Promote Timer (in unit of 125MHz)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

Offset Address: 216h (D0F0)
Root Port 2 (x1) Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Occupancy Timer (in unit of 125MHz)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 217h (D0F0)
Root Port 2 (x1) Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Promote Timer (in unit of 125MHz)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

Offset Address: 218h (D0F0)
Port Arbitration Timers for PE3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Occupancy Timer of PE3 - 125Mhz**

Offset Address: 219h (D0F0)
Port Arbitration Timers for PE3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Promote Timer of PE3 - 125Mhz**

Host Side Upstream Arbitration Timers (230–23Dh)

The upstream traffic controller uses arbitration timers to provide fair arbitration between PCI express devices and other devices like PCI2 master, IOAPIC and V-Link. The arbitration scheme is the same as the one currently implemented in the DRAMC.

Offset Address: 230h (D0F0)
PCI-E – VC0 Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Occupancy Timer (in unit of host frequency)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 231h (D0F0)
PCI-E – VC0 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Promote Timer (in unit of host frequency)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

Offset Address: 232h (D0F0)
PCI-E – VC1 Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PCI-E - VC1 Strict Priority** 0: Disable 1: Enable
6:4	—	0	**Reserved**
3:0	RW	0	**Occupancy Timer (in unit of host frequency)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 233h (D0F0)
PCI-E - VC1 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Promote Timer (in unit of host frequency)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

Offset Address: 234h (D0F0)
V-Link Arbitration Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Strict Priority to GPCI or NVC (PMADS) Request** 0: Disable 1: Enable
6	RW	0	**High Priority to GPCI or NVC (with PMSIO) Request** 0: Disable 1: Enable
5:4	—	0	**Reserved**
3:0	RW	0	**Occupancy Timer (in unit of host frequency)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 235h (D0F0)
V-Link Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Promote Timer (in unit of host frequency)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

Offset Address: 236h (D0F0)
V-Link – VC1 Arbitration Control **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1	**Strict Priority to V-Link – VC1** 0: Disable 1: Enable
6:4	—	0	**Reserved**
3:0	RW	0	**Occupancy Timer (in unit of host frequency)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 237h (D0F0)
V-Link – VC1 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Promote Timer (in unit of host frequency)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

Offset Address: 23Ah (D0F0)
PCI2 / NVC Occupancy Timers **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	—	0	**Reserved**
5:4	RW	0	**NVC Occupancy Timer (in unit of host frequency)** 00: Timer is off (i.e. 1T Round Robin scheme) 01: 4T 10: 8T 11: 16T
3:2	—	0	**Reserved**
1:0	RW	0	**PCI2 Occupancy Timer (in unit of host frequency)** 00: Timer is off (i.e. 1T Round Robin scheme) 01: 4T 10: 8T 11: 16T

Offset Address: 23Bh (D0F0)
PCI2 / NVC Promote Timers **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	—	0	**Reserved**
5:4	RW	0	**NVC Promote Timer (in unit of host frequency)** 00: Timer is off 01: 4T 10: 8T 11: 16T
3:2	—	0	**Reserved**
1:0	RW	0	**PCI2 Promote Timer (in unit of host frequency)** 00: Timer is off 01: 4T 10: 8T 11: 16T

Offset Address: 23Ch (D0F0)
IOAPIC Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Occupancy Timer (in unit of host frequency)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 23Dh (D0F0)
IOAPIC Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Promote Timer (in unit of host frequency)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

DRAM Side Upstream Arbitration Timers (240–241h)
This fair arbitration timer is for upstream traffic to do a fair arbitration between all of the VC1 PCI express devices.

Offset Address: 240h (D0F0)
PCI-E - VC1 Arbitration Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Strict Priority to VC1** 0: Disable 1: Enable
6:4	—	0	**Reserved**
3:0	RW	0	**Occupancy Timer (in unit of DRAMC frequency)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 241h (D0F0)
PCI-E - VC1 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Promote Timer (in unit of DRAMC frequency)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

Device 0 Function 1 (D0F1): Error Reporting

Header Registers (0-3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	Vendor ID
3 – 2h	RO	1238h	Device ID – Error Reporting
5 – 4h	RO	0006h	PCI Command
7 – 6h	RO	0200h	PCI Status
8h	RO	0	Revision ID
0B – 9h	RO	060000h	Class Code
0Dh	RO	0	Latency Timer
0Eh	RO	00h	Header Type
0Fh	RO	0	BIST
13-10h	—	—	Reserved
2D – 2Ch	RW1	0	Subsystem Vendor ID
2F – 2Eh	RW1	0	Subsystem ID
33 – 30h	RO	0	Reserved
37 – 34h	RO	0	Capability Pointer
3F – 38h	—	—	Reserved

V-Link Error Report (50-5Fh)

Offset Address: 50h (D0F1)

V-Link Error Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	—	0	**Reserved**
0	RW1C	0	**V-Link Parity Error Detected** 0: No V-Link Parity Error being detected 1: V-Link Parity Error detected

Offset Address: 58h (D0F1)

V-Link Error Command **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Parity Error / SERR# Report Through NMI** 0: Disable 1: Enable
6	RW	0	**Parity Error / SERR# Report Through V-Link to SB** 0: Disable 1: Enable
5:1	—	0	**Reserved**
0	RW	0	**V-Link Parity Check Report** 0: Disable 1: Enable

Device 0 Function 2 (D0F2): Host Bus Control

Header Registers (0-3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	Vendor ID
3 – 2h	RO	2238h	Device ID – Host Interface
5 – 4h	RO	0006h	PCI Command
7 – 6h	RO	0200h	PCI Status
8h	RO	00	Revision ID
0B – 9h	RO	060000h	Class Code
0Dh	RO	00	Latency Timer
0Eh	RO	00	Header Type
0Fh	RO	00	BIST
13-10h	—	—	Reserved
2D – 2Ch	RW1	00	Subsystem Vendor ID
2F – 2Eh	RW1	00	Subsystem ID
33 – 30h	RO	00	Reserved
37 – 34h	RO	00	Capability Pointer
3F – 38h	—	—	Reserved

Host CPU HyperTransport Control (A0-BBh)

Offset Address: A0h (D0F2)

CPU Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**In-Order Processing of CPU-to-PCI Requests or HT Ordering Rule** 0: Disable 1: Enable
6	RW	0	**In-Order Response of PCI Master Write Ready and PCI Master Read Ready** 0: Disable 1: Enable
5:4	—	0	**Reserved**
3	RW	0	**EOI Cycles to PCI2** 0: Disable 1: Enable
2:0	RW	000	**Number of Outstanding PCI-to-CPU Requests on HT Bus**

Offset Address: A1h (D0F2)

CPU Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	dip	**ROMSIP Support default set from VAD6** 0: Disable 1: Enable
6	RW	0	**Set Isochronous Request Bit for PCI-to-CPU Requests with PMSIO** 0: Disable 1: Enable
5	—	0	**Reserved**
4	RW	0	**Set Isochronous Request Bit for All PCI-to-CPU Requests** 0: Disable 1: Enable
3	—	0	**Reserved**
2	RW	0	**Non-Posted Response of CPU-to-PCI from PCI. Will Wait for Previous PCI-to-CPU Write PCI Write Flush** 0: Disable 1: Enable
1	—	0	**Reserved**
0	RW	0	**256-Byte RAM Access** 0: Disable 1: Enable

Offset Address: A2h (D0F2)

RAM Base Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**256-Byte RAM Base Address**

Offset Address: A3h (D0F2)
LDT Initial Value 1 **Default Value: 31h**

Bit	Attribute	Default	Description
7	—	0	**Reserved**
6:4	RW	011	**HT400 Initialization Counter**
3	—	0	**Reserved**
2:0	RW	001	**HT200 Initialization Counter**

Offset Address: A4h (D0F2)
LDT Initial Value 2 **Default Value: 30h**

Bit	Attribute	Default	Description
7	RW	0	**VADS Read Outstanding Request Number** 0: 16 1: 32
6:4	RW	011	**HT800 Initialization Counter**
3	—	0	**Reserved** (always reads 0)
2:0	RW	000	**HT600 Initialization Counter**

Offset Address: A5h (D0F2)
Arbitration Control 1 **Default Value: 08h**

Bit	Attribute	Default	Description
7:6	—	0	**Reserved**
5	RW	0	**HT Controller Action for PCI-to-CPU Write Cycles With All Byte Enables Set** 0: Issue DoubleWord Write 1: Issue Byte Write
4	—	0	**Reserved**
3	RW	1	**CF8 / CFC I/O Cycles** 0: Disable 1: Enable
2	RW	0	**PCI Master Access Bursting** 0: Allow only 1 request before data phase 1: Allow up to 4 pipelined requests before data phase
1:0	—	0	**Reserved**

Offset Address: A6h (D0F2)
Arbitration Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Clear CPU-to-PCI Read Response PassPW Bit** 0: Disable 1: Enable
6	RW	0	**Set CPU-to-PCI Target Done PassPW Bit** 0: Disable 1: Enable
5	RW	0	**Clear CPU-to-PCI Target Done PassPW Bit** 0: Disable 1: Enable
4	RW	0	**Legacy NMI Encoding for MT[3]** 0: Disable 1: Enable
3	RW	0	**Legacy External Interrupt Encoding for MT[3]** 0: Disable 1: Enable
2	RW	0	**Reduce 1T Latency for Fast Write Cycles (Allow FW 8QW Access to Burst)** 0: Disable 1: Enable
1	RW	0	**VID / FID Change Delay to P-State Control** 0: Disable 1: Enable
0	—	0	**Reserved**

Offset Address: A7h (D0F2)
Miscellaneous Control 1 **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1	**SeqID Value in Graphics Engine Packets**
6	RW	0	**Set Isochronous When VPRI=1 in Graphics Engine Packet** 0: Disable 1: Enable
5:0	–	0	**Reserved**

Offset Address: A8h (D0F2)
Miscellaneous Control 2 **Default Value: 05h**

Bit	Attribute	Default	Description
7	RW	0	**PCI Master SIO for PCI Master ADS As High Priority Arbitration** 0: Disable 1: Enable
6:3	–	0	**Reserved**
2	RW	1	**PCI Master Request for PCI Master ADS As Parking Request** 0: Disable 1: Enable
1:0	–	1	**Reserved**

Offset Address: A9h (D0F2)
Miscellaneous Control 3 **Default Value: 4Fh**

Bit	Attribute	Default	Description
7	–	0	**Reserved**
6:4	RW	100	**PCI Master ADS Read Merge Timer** (for waiting for the next request) 0: Disable 1: Enable
3:0	RW	1111	**PCI Master ADS Write Merge Timer** (for waiting for the next request) 0: Disable 1: Enable

Offset Address: AAh (D0F2)
Transmit Data Drive Control **Default Value: 22h**

Bit	Attribute	Default	Description
7	RW	0	**Data Coarse Delay Control**
6:4	RW	010	**Data Pullup Drive Strength**
3	–	0	**Reserved** (always reads 0)
2:0	RW	010	**Data Pulldown Drive Strength**

Offset Address: ABh (D0F2)
Transmit Clock Drive Control **Default Value: 22h**

Bit	Attribute	Default	Description
7	RW	0	**Clock Coarse Delay Control**
6:4	RW	010	**Clock Pullup Drive Strength**
3	–	0	**Reserved** (always reads 0)
2:0	RW	010	**Clock Pulldown Drive Strength**

Offset Address: ACh (D0F2)
Transmit Auto-compensation Result **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Transmitter Auto-compensation Select** 0: Manual 1: Automatic
6:4	RO	000	**Transmit Data / Clock Pullup Drive Strength from Auto-compensation**
3	–	0	**Reserved** (always reads 0)
2:0	RO	000	**Transmit Data / Clock Pulldown Drive Strength from Auto-compensation**

Offset Address: ADh (D0F2)
Lightning Data Transport (LDT) Controller Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**Read Response Buffer Release Delay** 00: No Delay 01: Delay 1T 10: Delay 2T 11: Delay 3T
5:0	–	0	**Reserved**

Offset Address: AEh (D0F2)
Receive Termination Value Control **Default Value: 22h**

Bit	Attribute	Default	Description
7	RW	0	**Termination Value Auto-compensation Select**
6:4	RW	010	**Receive Data Termination Value**
3	–	0	**Reserved** (always reads 0)
2:0	RW	010	**Receive Clock Termination Value**

Offset Address: AFh (D0F2)
Receive Termination Auto-compensation Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	–	0	**Reserved** (always reads 0)
6:4	RO	000	**Receive Data / Clock Termination Auto-compensation Value**
3	RO	0	**DB4 Receive Clock Delay** 0: 1T 1: 2T
2:0	–	0	**Reserved**

Offset Address: B0h (D0F2)
Response Flow Control Buffer Depth **Default Value: 3Fh**

Bit	Attribute	Default	Description
7	–	0	**Reserved**
6	RO	x	**No HCLK Inputs as the Reference Clock of Host PLL**
5:4	RW	11	**Response Command/Data of Flow Control Buffer Depth (8 Levels in Design)** 00: 1 Level 01: 2 Levels 10: 4 Levels 11: 8 Levels
3:2	RW	11	**Non Posted Command of Flow Control Buffer Depth (4 Levels in Design)** 00: 1 Level 01: 2 Levels 10: 3 Levels 11: 4 Levels
1:0	RW	11	**Post Write Command/Data Buffer Depth (5 Levels in Design)** 00: 1 Level 01: 2 Levels 10: 4 Levels 11: 5 Levels

Offset Address: B1h (D0F2)
Response Post-Write Buffer Depth **Default Value: 10h**

Bit	Attribute	Default	Description
7:6	–	0	**Reserved**
5	RW	0	**Value of Sequence ID in PCI Master Upstream Request Packet default = 0**
4	RW	1	**CPU-to-PCI Response Packet Isochronous Bit** 0: Always clear 1: Same as corresponding request packet
3	RW	0	**Set Value of PassPW bit in VADS Upstream Request Packet**
2:0	–	0	**Reserved**

Offset Address: B2h (D0F2)

Trusted Processing Module (TPM) Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Ignore CPU-to-PCI Accesses to Addresses FED4 4000 through FED4 FFFF (TPM Reserved Range)** 0: Disable 1: Enable
6	RW	0	**TPM Special Command Decoding** 0: Disable 1: Enable
5	RW	0	**Protect Start Address 00 FED4 4020, 00FED4 4024, and 00 FED4 4028 in MMIO Range with Command Length of 1DW** 0: Disable 1: Enable
4	RW	0	**Forward TPM Special Commands to V-Link By I/O Commands** 0:Disable 1: Enable
3:0	—	0	**Reserved** (always reads 0)

Offset Address: B3h (D0F2)

Arbitration **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Always Set VDPHPRIas 1**
6:3	—	0	**Reserved**
2	RW	0	**Always Set GPRI as 1**
1:0	—	0	**Reserved**

Offset Address: B4h (D0F2)

PCI Isochronous Request Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0h	**Reserved**
3:2	RW	00	**HT Controller Parking Arbitration for PCI Isochronous Requests** 00: Park at previous bus 01: Park at PCI Master 10: Reserved 11: Reserved
1:0	—	0h	**Reserved**

Offset Address: B5h (D0F2)

PCI Master Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0h	**HT Controller PCI Master Timer** (programmed in units of 16 HT clocks)
3:0	RW	0h	**HT Controller PCI Master Promotion Timer** (programmed in units of 16 HT clocks)

Offset Address: B8h (D0F2)
TLSID I

Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	**TLSID[3:0]='b0000 ISOCHRONOUS** 0: Disable 1: Enable
6	RW	0	**TLSID[3:0]='b0001 ISOCHRONOUS** 0: Disable 1: Enable
5	RW	0	**TLSID[3:0]='b0010 ISOCHRONOUS** 0: Disable 1: Enable
4	RW	0	**TLSID[3:0]='b0011 ISOCHRONOUS** 0: Disable 1: Enable
3	RW	0	**TLSID[3:0]='b0100 ISOCHRONOUS** 0: Disable 1: Enable
2:1	—	0h	**Reserved**
0	RW	0	**TLSID[3:0]='b0111 ISOCHRONOUS** 0: Disable 1: Enable

Offset Address: B9h (D0F2)
TLSID II

Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	**TLSID[3:0]='b1000 ISOCHRONOUS** 0: Disable 1: Enable
6	RW	0	**TLSID[3:0]='b1001 ISOCHRONOUS** 0: Disable 1: Enable
5	RW	0	**TLSID[3:0]='b1010 ISOCHRONOUS** 0: Disable 1: Enable
4	RW	0	**TLSID[3:0]='b1011 ISOCHRONOUS** 0: Disable 1: Enable
3	—	0h	**Reserved**
2	RW	0	**TLSID[3:0]='b1101 ISOCHRONOUS** 0: Disable 1: Enable
1	—	0h	**Reserved**
0	RW	0	**TLSID[3:0]='b1111 ISOCHRONOUS** 0: Disable 1: Enable

Offset Address: BAh (D0F2)
Programmable MSI Address

Default Value: 00h

Bit	Attribute	Default	Description
7:4	RW	0	**Programmable MSI address**
3	RW	0	**Programmable MSI address decode enable** 0: Disable 1: Enable
2:0	—	00	**Reserved**

Offset Address: BBh (D0F2)
Programmable MSI Address

Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	**Programmable MSI Address**

Offset Address: C0h (D0F2)
HT Transmit CAD[7:0], Rise / Fall Delay Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	Positive Data Signal Rise Delay
5:4	RW	00	Positive Data Signal Fall Delay
3:2	RW	00	Negative Data Signal Rise Delay
1:0	RW	00	Negative Data Signal Fall Delay

Offset Address: C1h (D0F2)
HT Transmit Clock0 Rise / Fall Delay Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	Positive Clock Signal Rise Delay
5:4	RW	00	Positive Clock Signal Fall Delay
3:2	RW	00	Negative Clock Signal Rise Delay
1:0	RW	00	Negative Clock Signal Fall Delay

Offset Address: C2h (D0F2)
HT Transmit CAD[15:8] Rise / Fall Delay Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	Positive Data Signal Rise Delay
5:4	RW	00	Positive Data Signal Fall Delay
3:2	RW	00	Negative Data Signal Rise Delay
1:0	RW	00	Negative Data Signal Fall Delay

Offset Address: C3h (D0F2)
HT Transmit Clock1 Rise / Fall Delay Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	Positive Clock Signal Rise Delay
5:4	RW	00	Positive Clock Signal Fall Delay
3:2	RW	00	Negative Clock Signal Rise Delay
1:0	RW	00	Negative Clock Signal Fall Delay

Offset Address: C4h (D0F2)
HT Receive CAD[7:0], Clock 0 Rise / Fall Delay Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	Data Input Rise Delay
5:4	RW	00	Data Input Fall Delay
3:2	RW	00	Clock Input Rise Delay
1:0	RW	00	Clock Input Fall Delay

Offset Address: C5h (D0F2)
HT Receive CAD[15:8], Clock 1 Rise / Fall Delay Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	Data Input Rise Delay
5:4	RW	00	Data Input Fall Delay
3:2	RW	00	Clock Input Rise Delay
1:0	RW	00	Clock Input Fall Delay

Device 0 Function 3 (D0F3): DRAM Bus Control

Header Registers (0–3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	Vendor ID
3 – 2h	RO	3238h	Device ID – DRAM Control
5 – 4h	RO	0006h	PCI Command
7 – 6h	RO	0200h	PCI Status
8h	RO	00	Revision ID
0B – 9h	RO	060000h	Class Code
0Dh	RO	00h	Latency Timer
0Eh	RO	00h	Header Type
0Fh	RO	00h	BIST
13-10h	—	—	Reserved
2D – 2Ch	RW1	00h	Subsystem Vendor ID
2F – 2Eh	RW1	00h	Subsystem ID
33 – 30h	RO	00h	Reserved
37 – 34h	RO	00h	Capability Pointer
3F – 7Eh	—	—	Reserved

Note: All Function 3, DRAM Controller, registers are implemented in Powell.

Shadow RAM Control (80–89h)

Offset Address: 80h (D0F3)

Page-C ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:6	RW	00	**CC000-CFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable	
5:4	RW	00	**C8000-CBFFFh Memory Space Access Control**	
3:2	RW	00	**C4000-C7FFFh Memory Space Access Control**	
1:0	RW	00	**C0000-C3FFFh Memory Space Access Control**	

Offset Address: 81h (D0F3)

Page-D ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:6	RW	00	**DC000-DFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable	
5:4	RW	00	**D8000-DBFFFh Memory Space Access Control**	
3:2	RW	00	**D4000-D7FFFh Memory Space Access Control**	
1:0	RW	00	**D0000-D3FFFh Memory Space Access Control**	

Offset Address: 82h (D0F3)

Page-E ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**EC000-EFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00	**E8000-EBFFFh Memory Space Access Control**
3:2	RW	00	**E4000-E7FFFh Memory Space Access Control**
1:0	RW	00	**E0000-E3FFFh Memory Space Access Control**

Offset Address: 83h (D0F3)

Page-F ROM, Memory Hole and SMI Decoding **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:6	—	0	**Reserved**	
5:4	RW	00	**F0000-FFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable	
3:2	RW	00	**Memory Hole** 00: None 01: 512K – 640K 10: 15M – 16M (1M) 11: 14M – 16M (2M)	
1	RW	0	**Disable Data Access on SMRAM (Page A, B) in SM mode** 0: In SM mode, page A,B CPU **Data** R/W cycles are forwarded to the memory controller. 1: In SM mode, page A,B CPU **Data** R/W cycles are forwarded to the PCI bus Notes: 1. This bit is effective when Rx83[0] is set to 0. 2. SMRAM page A,B **Code** R/W cycles are always forwarded to the memory controller in SM mode.	**RABKDOFF**
0	RW	0	**Enable Page A, B DRAM Access In Normal Mode** 0: Page A, B CPU R/W cycles could be forwarded to memory controller or PCI bus depends on the setting of RABKDOFF (bit 1), the CPU operating mode (Normal or SM mode) as well as the type (Code or Data) of the CPU cycle. 1: Page A, B CPU R/W cycles (Code and Data) are always (in either Normal or SM mode) forwarded to the memory controller. Check the following table for details.	**RRWABK**

Table 5. CPU-to-SMRAM Cycle Flow

RABKDOFF (Rx83[1])	RRWABK (Rx83[0])	CPU MODE	Target of CODE Acces Cycle	Target of DATA Access Cycle
x	0	Normal	PCI	PCI
0	0	SMM	DRAM	DRAM
1	0	SMM	DRAM	PCI
x	1	Normal / SMM	DRAM	DRAM

Offset Address: 84h (D0F3)

Low Top Address - Low **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000	**Low Top Address - A[23:20]**
3:0	—	0000	**Reserved**

Offset Address: 85h (D0F3)

Low Top Address - High **Default Value: FFh**

Bit	Attribute	Default	Description
7:0	RW	FFh	**Low Top Address – A[31:24]**

Offset Address: 86h (D0F3)

SMM and APIC Decoding **Default Value: 01h**

Bit	Attribute	Default	Description	Mnemonic
7:6	—	0	**Reserved**	
5	RW	0	**APIC Lowest Interrupt Arbitration** 0: Disable 1: Enable	
4	RW	0	**IO APIC Decoding** 0: Cycles accessing FECx_xxxxh are passed to PCI1 1: Cycles accessing FEC7_FFFFh - FEC0_0000h are passed to PCI1; cycles accessing FECF_FFFFh - FEC8_0000h access cycles are passed to PCI2.	**RAPIC2**
3	RW	0	**MSI Support (Processor Message Enable)** 0: Cycles accessing FEEx_xxxxh from masters are passed to PCI1 (PCIC will not claim) 1: Cycles accessing FEEx_xxxxh from masters are passed to the Host side for snooping	
2	RW	0	**Top 1MB SM Memory Enable** 0: Disable 1: Enable TSMMA[31:20] = {LOWTOPA[31:24],4'h0} – {FBSZ[2:0],1'b0}; OSLOWTOPA[31:20] = TSMMA[31:20] – RTSMMEN	**RTSMMEN**
1	—	0	**Reserved**	
0	RW	1	**Compatible SMM Enable** 0: Disable 1: Enable	**RCSMMEN**

Offset Address: 89-88h (D0F3)

Misc. DRAM Address Setting **Default Value:0000h**

Bit	Attribute	Default	Description
15:11	—	0	**Reserved**
10:0	RW	0	**The Address Next to the Last Valid DRAM Address**

Device 0 Function 4 (D0F4): Power Management Control

Header Registers (0–3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	Vendor ID
3 – 2h	RO	4238h	Device ID – Power Management Control
5 – 4h	RO	0006h	PCI Command
7 – 6h	RO	0200h	PCI Status
8h	RO	00	Revision ID
0B – 9h	RO	060000h	Class Code
0Dh	RO	00	Latency Timer
0Eh	RO	00	Header Type
0Fh	RO	00	BIST
13-10h	—	—	Reserved
2D – 2Ch	RW1	00	Subsystem Vendor ID
2F – 2Eh	RW1	00	Subsystem ID
33 – 30h	RO	00	Reserved
37 – 34h	RO	00	Capability Pointer
3F – 38h	—	—	Reserved

Power Management Control (A0–EFh)

Offset Address: A0h (D0F4)

Power Management Mode **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic Power Management** 0: Disable 1: Enable
6	RW	0	**Power Management During HALT / SHUTDOWN** 0: Disable 1: Enable
5	RW	0	**Power Management During STPCLK** 0: Disable 1: Enable
4	RW	0	**Power Management During SUSSTAT** 0: Disable 1: Enable
3:0	—	0	**Reserved**

Offset Address: A2h (D0F4)

Dynamic Clock Stop Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Host Interface Power Management** 0: Disable 1: Enable
6	RW	0	**DRAM Interface Power Management** 0: Disable 1: Enable
5	RW	0	**V-Link Interface Power Management** 0: Disable 1: Enable
4	—	0	**Reserved**
3	RW	0	**PCI2 Interface Power Management** 0: Disable 1: Enable
2	RW	0	**Graphics Interface (GMINT) Power Management** 0: Disable 1: Enable
1	RW	0	**VKCFG Interface Power Management** 0: Disable 1: Enable
0	RW	0	**Host Fast Power-Management (DADS Fast Timing)** 0: Disable 1: Enable

Offset Address: A8h (D0F4)
PCI-E Dynamic Clock Stop **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	—	0	**Reserved**
5	RW	0	**Central Traffic Controller Dynamic Clock STOP** 0: Disable 1: Enable
4	RW	0	**PE0 (x16) Dynamic Clock STOP** 0: Disable 1: Enable
3	RW	0	**Reserved**
2	RW	0	**PE2 (x1) Dynamic Clock STOP** 0: Disable 1: Enable
1	RW	0	**Reserved**
0	PW	0	**PE1 (x4) Dynamic Clock STOP** 0: Disable 1: Enable

Offset Address: DF-D0h (D0F4)
BIOS Extended Scratch Registers D **Default Value: 00h**

Offset Address	Attribute	Default	Description
DF – D0h	RW	0	**BIOS Extended Scratch Registers D**

Offset Address: EF-E0h (D0F4)
BIOS Extended Scratch Registers E **Default Value: 00h**

Offset Address	Attribute	Default	Description
EF – E0h	RW	0	**BIOS Extended Scratch Registers E**

Device 0 Function 5 (D0F5): APIC and Central Traffic Control

Header Registers (0–3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	Vendor ID
3 – 2h	RO	5238h	Device ID – for Power Management Control
5 – 4h	RO	0006h	PCI Command
7 – 6h	RO	0200h	PCI Status
8h	RO	00	Revision ID
0B – 9h	RO	080020h	Class Code
0Dh	RO	00	Latency Timer
0Eh	RO	80h	Header Type
0Fh	RO	00	BIST
13-10h	—	—	Reserved
2D – 2Ch	RW1	00	Subsystem Vendor ID
2F – 2Eh	RW1	00	Subsystem ID
33 – 30h	RO	00	Reserved
37 – 34h	RO	00	Capability Pointer
3F – 38h	—	—	Reserved

Legacy APIC Base I/O Registers (40–5Fh)

Offset Address: 40h (D0F5)

APIC Legacy Configuration — **Default Value: 0Ch**

Bit	Attribute	Default	Description
7	RW	0	**Legacy APIC** 0: Disable 1: Enable; Range FECxyz00 to FECxyzFF, where **x,y,z** are defined in Rx40[3:0] and Rx41[7:0]
6:4	—	0	**Reserved**
3:0	RW	0Ch	**APIC Legacy Address Range - x**

Offset Address: 41h (D0F5)

APIC Legacy Address Range – y / z — **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**APIC Legacy Address Range - y**
3:0	RW	0	**APIC Legacy Address Range - z**

Offset Address: 42h (D0F5)

APIC BT_INTR Control — **Default Value: 03h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3	RW	0	**Disable INTx Transparent Mode** 0: Enable Transparent mode 1: Disable Transparent mode
2	RW	0	**APIC Nonshare Mode Enable**
1	RW	1	**BTIDIS Function of the APIC Module** 0: Disable 1: Enable
0	RW	1	**BT_INTR Function** 0: Disable 1: Enable

Central Traffic - Downstream Control (60–7Fh)

Offset Address: 60h (D0F5)

Extended CFG Address Support **Default Value: 20h**

Bit	Attribute	Default	Description
7	RW	0	**D3F1 and D3F3 Existence** 0: D3F1 and D3F3 are not implemented. Read always returns FFFFFFFFh, write has no effect to registers in D3F1 and D3F3 1: D3F1 and D3F3 are implemented. Registers in D3F1, and D3F3 can be read and written.
6	—	0	**Reserved**
5	RW	1	**Convert Device2 CF8 Cycles to Device1 while Passing it to the SB** (in PCI-E Mode) 0: CF8 access cycles are passed to the SB normally 1: CF8 with data[15:11]=00010 will be changed to data[15:11]=00001
4	RW	0	**CF8 Byte Write Enable** 0: Only supports CF8 write with all BE active 1: Allow CF8 write with partial BE active
3	RW	0	**For Device 2 and Device 3, Configuration Cycles to the Secondary Bus behind the P2P Bridge** 0: Configuration cycles for all the devices will be passed through. 1: Only configuration cycles for device 0 will be passed to the secondary bus.
2	—	0	**Reserved**
1:0	RW	0	**Extended CFG Mode** 00: Extended CFG mode is off 01: Reserved 10: Capability header for extended configuration address support 11: Memory mapped extended CFG address supported (RX61[7:0] should also be programmed.)

Offset Address: 61h (D0F5)

Memory Mapped Extended CFG Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	—	0	**Extended Configuration Address: A[35:28]** 00h: No extended configuration address Else: Extended configuration address A[35:28] from host side

Offset Address: 62h (D0F5)

Memory Mapped Extended RCRB Base Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	—	0	**RCRB Base Address** 00h: no RCRB is supported

Offset Address: 64h (D0F5)

Miscellaneous **Default Value: 33h**

Bit	Attribute	Default	Description
7:6	—	0	**Reserved**
5	RW	1	**Upstream MSI Cycles Forces Flush of the Queued P2C Write Data** 0: Disable 1: Enable Note: Upstream MSI cycles includes FEEx_xxxx from the internal APIC and cycles with address as programmed in Rx74-7B of D2, D3F0 and D3F2.
4	RW	0	**Downstream C2P Forces Flush of the Upstream P2C Write to the Host Side before Return LRDY to the Host Side.** 0: Disable 1: Enable Note: C2P Downstream cycles include MEMR, IOR and IOW
3:2	—	0	**Reserved**
1	RW	1	**Downstream Write Request Timing** 0: Wait for the write data to issue downstream request 1: Issue downstream request once request from the host is received
0	RW	1	**Traffic Controller Downstream Cycles Are Processed in Order** 0: Disable: Downstream post write transaction won't be issued out until the data phase of the previous read transaction is finished 1: Enable: Downstream post write transaction can be issued out before the completion of the data phase of the previous read transaction

Central Traffic - Upstream Control (80h)

Offset Address: 80h (D0F5)

Central Traffic-Upstream Control **Default Value: 05h**

Bit	Attribute	Default	Description
7	—	0	**Reserved (Must pull high on signal pin PEDET)**
6	RW	0	**VC1 Upstream Path** 0: VC1 requests are forwarded to the host side (snoop) 1: VC1 requests are forwarded to the DRAMC side. Those required snoops are reported as MalFunction TLPs.
5	RW	0	**CPU-to-Memory FIFO Snoop Policy for Upstream Request to DRAMC** 0: Upstream requests are sent to DRAMC directly 1: Upstream requests to DRAMC have to wait for the snoop result from CPU-to-Memory FIFO. When hit, DRAMC will postpone handling these upstream requests till cycles in the CMFIFO been flushed to the DRAM.
4:3	—	0	**Reserved**
2	RW	1	**Host Side Upstream Write, Transaction End With 1T earlier notice** 0: Disable 1: Enable
1	RW	0	**Host Side Upstream Read Data Returning Path** 0: 2 levels of synchronous FIFO 1: 1 level synchronous FIFO.
0	RW	1	**Host Side Upstream Write, Data Return With a 1T Notice** 0: Disable 1: Enable

PCI-E Message Controller and Power Management (A0–F0h)

Offset Address: A0h (D0F5)

PCI-E PMU Control and Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RWS	0	**PEWAKE# Activation Control** 0: PEWAKE# function is disabled. 1: PEWAKE# function is enabled.
6	RW	0	**PEPMESCI# (System Control Interrupt) Activation Control** 0: PEPMESCI function is disabled 1: PEPMESCI function is enabled
5	RW	0	**PEHPSCI# (System control Interrupt) Activation Control** 0: SCI2# PEHPSCI# function is disabled 1: SCI2# PEHPSCI# function is enabled
4	RW1C	0	**PE0, a x16 Root Port, L2L3 PME Acknowledge Status** 0: Disable 1: 1 indicates that upon set RPMETOFF (RxF0[7]) to 1, PE0 goes to L2L3 ready state and PME_TO_ACK message has been returned from the device at PE0.
3	—	0	**Reserved**
2	RW1C	0	**PE2, a x1 Root Port, L2L3 PME Acknowledge Status** 0: Disable 1: 1 indicates that upon set RPMETOFF (RxF0[7]) to 1, PE2 goes to L2L3 ready state and PME_TO_ACK message has been returned from the device at PE1.
1	—	0	**Reserved**
0	RW1C	0	**PE1, a x4 Root Port, L2L3 PME Acknowledge Status** 0: disable 1: 1 indicates that upon set RPMETOFF (RxF0[7]) to 1, PE1 goes to L2L3 ready state and PME_TO_ACK message has been returned from the device at PE1.

Offset Address: A1h (D0F5)

PCI-E PMU Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**PM_PME Message Status** 0: No PM_PME message 1: At least one PM_PME message was received at the PCI-E ports. Note: Wake up the system through either PEWAKE# or PEPMESCI# depends on the settings on RxA0[7:6].
6	—	0	**Reserved**
5	RO	0	**Hot Plug Event Status** 0: No Hot Plug event. 1: At least one Hot Plug event was received at the PCI-E ports. This event is triggered by PEHPSCI# (check RxA0[5] for activation control.)
4:0	—	0	**Reserved**

Offset Address: A2h (D0F5)

PMU Downstream Address [15:8] **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Downstream Address Bits [15:8]** This register is used for monitoring S3/S4/S5 downstream command. Refers to RxA3[7] for address [7].

Offset Address: A3h (D0F5)

PMU Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Address Bit [7]** This bit is used for monitoring S3/S4/S5 downstream command. Refers to RxA2 for address [15:8].
6:1	—	0	**Reserved**
0	RW	0	**Monitor S3/S4/S5 Command** 0: Disable 1: Enable When enable, the controller will monitor S3/S4/S5 commands (e.g. IOW 4005, 'h24 or 'h28) in the following procedure: 1. The controller receives the STPGNT cycles from the CPU 2. The controller triggers MSGC to issue PME_TURNOFF message to PCI-E devices (D2F0, D2Fx) 3. The controller waits for the acknowledge from all the devices to issue the STPGNT cycle received in step 1 to SB.

Offset Address: F0h (D0F5)

PMU Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**PCI-E Device Power Management Control** 0: Disable 1: Enable Programmed this bit to 1 will trigger a PME_TURNOFF message sent to PCI-E Root Ports, where devices are activated. This bit has to be programmed to 0 before it can be programmed to 1 again.	**RPMETOFF**
6:1	—	0	**Reserved**	
0	RW	0	**Capability / Status Write of the P2P Header (D2F0, D3F0 and D3F2)** 0: Disable 1: Enable	

Device 0 Function 6 (D0F6): Scratch Registers

Scratch Registers (40–7Fh)

Offset Address	Attribute	Default	Description
40-4Fh	RW	0000 0000	BIOS Scratch Register
50-5Fh	RW	0000 0000	BIOS Scratch Register
60-6Fh	RW	0000 0000	BIOS Scratch Register
70-7Fh	RW	0000 0000	BIOS Scratch Register

Device 0 Function 7 (D0F7): V-Link North Bridge and South Bridge Control

Header Registers (0–3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	Vendor ID
3 – 2h	RO	7238h	Device ID – for V-Link Control
5 – 4h	RO	0006h	PCI Command
7 – 6h	RO	0200h	PCI Status
8h	RO	00	Revision ID
0B – 9h	RO	060000h	Class Code
0Dh	RO	00	Latency Timer
0Eh	RO	00	Header Type
0Fh	RO	00	BIST
13-10h	—	—	Reserved
2D – 2Ch	RW1	00	Subsystem Vendor ID
2F – 2Eh	RW1	00	Subsystem ID
33 – 30h	RO	00	Reserved
37 – 34h	RO	00	Capability Pointer
3F – 38h	—	—	Reserved

V-Link Control Interface (40–B1h)

Offset Address: 40h (D0F7)

V-Link Specification ID **Default Value: 51h**

Bit	Attribute	Default	Description
7:4	RO	5h	**North Bridge V-Link Revision ID**
3:0	RO	1h	**South Bridge V-Link Revision ID** 0, 0Fh: 8-bit V-Link, the operating mode is determined by Rx48[0]. 1h: Support V-Link capability up to mode 1. 2h: Support V-Link capability up to mode 2. 3h: Support V-Link capability up to mode 3. 4h: Support V-Link capability up to mode 4. 5h: Support high priority upstream read. 6h: Support high priority upstream read / write.

Offset Address: 41h (D0F7)

NB V-Link Capability **Default Value: 3Bh**

Bit	Attribute	Default	Description
7:6	—	0	**Reserved**
5	RO	1	**16-Bit Bus Width** 0: Not supported 1: Supported
4	RO	1	**8-Bit Width** 0: Not supported 1: Supported
3	RO	1	**4X Rate** 0: Not supported 1: Supported
2	RO	0	**2X Rate** 0: Not supported 1: Supported
1	—	1	**V-Link Bus Split (native 8X mode)** 0: Not supported 1: Supported
0	RO	1	**8X Rate** 0: Not supported 1: Supported

Offset Address: 42h (D0F7)
NB Downlink (C2P) Configuration **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RW	8h	**C2P, DNCMD, Maximum Pending Request Depth** Maximum # of pending DNCMD, C2P, requests. 0000: 1 level ... 1111: 16 levels
3:0	RW	8h	**C2P Maximum Write Buffer Size** (from 1 to 16 DW)

Offset Address: 43h (D0F7)
NB Uplink (P2C) Status I **Default Value: 82h**

Bit	Attribute	Default	Description
7:4	RO	8h	**P2C, UPCMD, Maximum Pending Request Depth** 0: 16 levels 1: 1 level ... n: n levels, where 0 < n <= 0Fh
3:2	—	0	**Reserved**
1:0	RO	10	**High Priority P2C Read Request Depth** 00: 1 level 01: 4 levels 10: 8 levels 11: 16 levels

Offset Address: 44h (D0F7)
NB Uplink (P2C) Status II **Default Value: 82h**

Bit	Attribute	Default	Description
7:4	RO	1000	**P2C Write Buffer Size** (max # of lines)
3:0	RO	02h	**P2P Write Buffer Size** (max # of lines)

Offset Address: 45h (D0F7)
NB V-Link Arbiter Timer **Default Value: 44h**

Bit	Attribute	Default	Description	Mnemonic
7:4	RW	4h	**V-Link Arbiter Timer for Normal Priority Request from SB** 0000: 0 VCLK 1000: 8*4 VCLK 0001: 1*4 VCLK 1001: 16*4 VCLK 0010: 2*4 VCLK 1010: 32*4 VCLK 0011: 3*4 VCLK 1011: 64*4 VCLK 0100: 4*4 VCLK 11--: NB holds the bus as long as there is pending downstream request	**RNNTM[3:0]**
3:0	RW	4h	**V-Link Arbiter Timer for High Priority Request from SB** 0000: 0 VCLK 1000: 8*2 VCLK 0001: 1*2 VCLK 1001: 16*2 VCLK 0010: 2*2 VCLK 1010: 32*2 VCLK 0011: 3*2 VCLK 1011: 64*2 VCLK 0100: 4*2 VCLK 11--: NB holds the bus as long as there is pending downstream request Note: see Table 13 for more details	**RNHTM[3:0]**

Table 6. NB V-Link Bus Arbitration

RNNTM[3:0] (Rx45[7:4])	RNHTM[3:0] (Rx45[3:0])	SB Request Priority	NB When to Relinquish the Occupied V-Link Bus
0000	xxxx	Normal / high	Immediately
0001,0010,...	0000	High	Immediately
0001,0010,...	0001,0010,...	High	Wait for either Normal or High timer expired
0001,0010,...	00xx	Normal	Wait for Normal timer expired
0001,0010,...	11xx	Normal / high	Wait for Normal timer expired
11xx	0000	High	Immediately
11xx	0000	Normal	Wait until no more pending downstream request
11xx	0001,0010,...	High	Wait for High timer expired
11xx	0001,0010,...	Normal	Wait until no more pending downstream request
11xx	11xx	Normal / high	Wait until no more pending downstream request

Offset Address: 46h (D0F7)

NB V-Link Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**Downstream Read Data Return High Priority** 0: NB will not issue preamble command to SB. 1: Enable NB to issue preamble command to inform SB release V-Link for P2C Read-Request data return	**RNHIRQ**
6	RW	0	**C2P Request Priority** 0: NB will not issue preamble command to SB. 1: Enable NB to issue preamble command to inform SB release V-Link for downstream C2P request. Note: To enable this function, RNHIRQ (bit7) must be set to 1.	
5:4	RW	0	**Options of Combining Multiple STPGNT Cycles Into a V-Link Command** 00: Compatible mode: a V-Link command per STPGNT cycle 01: Combines 2 STPGNT cycles into a V-Link command 10: Combines 3 STPGNT cycles into a V-Link command 11: Combines 4 STPGNT cycles into a V-Link command	
3:2	RW	0	**V-Link Master Read/Write Access Ordering Rules** 00: High Priority Read allows to pass Normal Read (but not pass Write) 01: Read (High/Normal) allows to pass Write (High Priority R>Normal Priority R>Write) 1x: Read / Write are executed in order	**RINORDER RHRPW**
1	RW	0	**Read Around Write** 0: Read always pass Write, if RINORDER (bit3) is 0 1: Allows up to 8 Read-Around-Write cycles before flushing the pending write, if RINORDER is 0 **Read Around Write is disabled if bit3, RINODER, is set to 1**	
0	RW	0	**Downstream DAC (Double Address Cycle) Cycle** 0: Disable 1: Enable	

Offset Address: 47h (D0F7)

NB V-Link Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Upstream High-Priority Write Request Stream** 0: No high-priority write request stream. 1: Enable support of high-priority write request stream.. When V-Link is not operated at 8X (and above), the high-priority write request is always disabled no matter what the setting of this bit is.
6	RW	0	**Upstream High-Priority Read Request Stream** 0: No high-priority read request stream. 1: Enable high-priority read request stream.
5	RW	0	**C2P Read ACK Return Priority** 0: V-Link decodes C2P Read ACK command right when it's received 1: C2P Read ACK command will be handled till pending P2C write cycles are all flushed
4	RW	0	**0CF8h Configuration Cycle Address Bit[27:24] Usage** 0: Normal PCI usage 1: Address bit[27:24] are used as extended register address bit[11:8]
3	RW	0	**Dynamic STOP on Down Strobe** 0: Disable 1: Enable
2	RW	0	**Auto-Disconnect** 0: Disable 1: Enable
1	RW	0	**V-Link Disconnect Sequence for STPGNT Cycle** 0: Disable 1: Enable
0	RW	0	**V-Link Disconnect Sequence for HALT cycle** 0: Disable 1: Enable

Offset Address: 48h (D0F7)

V-Link Configuration – NB / SB **Default Value: 18h**

This register is used to configure V-Link bus controller on both North and South bridge chips.

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**Parity Check** 0: Disable 1: Enable	
6	—	0	**Reserved**	
5	RW	0	**16-Bit Width** 0: Disable 1: Enable	**RX16VK**
4	RW	1	**8-Bit Width** 0: Disable 1: Enable	**RX8VK**
3	RW	1	**4X Rate** 0: Disable 1: Enable	
2	RW	0	**2X Rate** 0: Disable 1: Enable	
1	RW	0	**V-Link Split Bus** 0: Disable 1: Enable	**RVKSPLT**
0	RW	0	**8X Rate** 0: Disable 1: Enable	

	X: Multiples of 66MHz cycle	Bus Width	R8XVK – 8X (D0F7 Rx48[0])	RX16VK – 16bit (D0F7 Rx48[5])	RVKSPLT – Split Bus (D0F7 Rx48[1])
Mode0 - 8-bit VD Half Duplex	4X	8-bit ▲▼	0	0	0
Mode1 – 8-bit VD Full Duplex	8X	4-bit ▲▼	1	0	1
Mode2 – 8-bit VD Half Duplex	8X	8-bit ▲▼	1	0	0
Mode3 – 16-bit VD Half Duplex	4X	16-bit ▲▼	0	1	0
Mode4 – 16-bit VD Full Duplex	8X	8-bit ▲▼	1	1	1

Procedure to Enable / Disable V-Link-8X Mode:

1. BIOS sets Rx48[0] to 1
2. Hardware will automatically enter a disconnect sequence, and then both NB/SB will start V-LINK 8X mode. Then normal operation is then resumed.
3. To return to V-Link 4X mode, BIOS sets Rx48[0] to 0
4. Step 2 is then repeated.

Offset Address: A0h (D0F7)

NVC Configure **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3	RW	0	While returning the P2C read ACK to SB, the NVC start to issue the next read request to reduce the P2C read latency 0: Disable 1: Enable
2:0	—	0	**Reserved**

Offset Address: B0h (D0F7)

V-Link CKG Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**Rising-Time Control for V-Link (R-Port)**
5:4	RW	00	**Falling-Time Control for V-Link (R-Port)**
3:2	RW	00	**Rising-Time Control for V-Link (S-Port)**
1:0	RW	00	**Falling-Time Control for V-Link (S-Port)**

Offset Address: B1h (D0F7)

V-Link CKG Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	—	**Reserved**
3:2	RW	00	**Rising-Time Control for V-Link (D-Port)**
1:0	RW	00	**Falling-Time Control for V-Link (D-Port)**

V-Link North Bridge Driving Control (B3–B7h)

Offset Address: B3h (D0F7)
V-Link Auto Compensation Termination Resistor Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**P Resistor Check Flag for the NB Termination Resistor** 0: Abnormal condition occurred 1: Normal operation
6	RO	0	**N Resistor Check Flag for the NB Termination Resistor** 0: Abnormal condition occurred 1: Normal operation
5	RO	0	**P Pull Down Driving Check Flag for the NB Termination Resistor** 0: Abnormal condition occurred 1: Normal operation.
4	RO	0	**N Pull Down Driving Check Flag for the NB Termination Resistor** 0: Abnormal condition occurred 1: Normal operation.
3	—	0	**Reserved**
2:0	RO	0	**NB V-Link Autocomp Termination Resistor Value** 000: Largest Resistor …. 111: Smallest Resistor

Offset Address: B4h (D0F7)
NB V-Link Compensation Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**V-Link Auto-compensation PMOS Output Value**
4	RW	0	**Reference Voltage of the VKCOMP in 4X V-Link Mode** 0: VREF4X=0.75V 1: VREF4X=0.9V
3:1	RO	0	**V-Link Auto-compensation NMOS Output Value**
0	RW	0	**Compensation Option** 0: Use Auto Compensation (value is kept in bits 7:5) 1: Use Manual setting (use the values of RxB5 and RxB6)

Offset Address: B5h (D0F7)
NB V-Link Manual Driving Control - Strobe **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Manual Setting - NB V-Link Strobe Pullup (PMOS)**
4	—	0	**Reserved**
3:1	RW	0	**Manual Setting - NB V-Link Strobe Pulldown (NMOS)**
0	—	0	**Reserved**

Offset Address: B6h (D0F7)
NB V-Link Manual Driving Control - Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Manual Setting - NB V-Link Data Pullup (PMOS)**
4	—	0	**Reserved**
3:1	RW	0	**Manual Setting - NB V-Link Data Pulldown (NMOS)**
0	—	0	**Reserved**

Offset Address: B7h (D0F7)
NB V-Link Receiving Strobe Delay **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**V-Link Manual Termination Resistor Value** 000: Largest Resistor …. 111: smallest Resistor
4:2	—	0	**Reserved**
1:0	RW	0	**NB V-Link Receiving Strobe Delay** 00: 0.15ns earlier 01: No delay 10: Delay 0.15ns 11: Delay 0.3ns

Device 2 Function 0 (D2F0) – PCI Express Root Port 0 (PCI-to-PCI Virtual Bridge)

Device 2 Function 0 is a 16-Lane PCI Express Root Port that is connected to the PCI bus through AD13 as the IDSEL. Registers listed in this section are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 2 and function number 0.

Header Registers (0-3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	**Vendor ID**
3 – 2h	RO	A238h	**Device ID**

Offset Address: 5-4h (D2F0)

Command Register **Default Value: 0000h**

Bit	Attribute	Default	Description	Mnemonic
15:11	—	0	**Reserved**	
10	RW	0	**Interrupt Disabled** Set when the device is prevented from generating INTx messages	
9	—	0	**Reserved**	
8	RW	0	**SERR# Enable** 0: Disable error report 1: Enable reporting of non-fatal and fatal errors	**RSERR_PEG**
7	—	0	**Reserved**	
6	RW	0	**Parity Error Response** 0: Ignore parity errors & continue 1: Take normal action on detected parity errors	**RPTYERR_PEG**
5:3	—	0	**Reserved**	
2	RW	0	**Bus Master Enable** 0: Disable 1: Enable Controls the ability to forward Memory and I/O Read/Write requests in the upstream direction. Disabling this bit disables MSI messages.	
1	RW	0	**Memory Space** 0: Ignore downstream memory transactions; memory cycles with address falling in the claimed range will be forwarded to the SB 1: Enable downstream memory cycle to this port if its address falling in the claimed range of this device.	
0	RW	0	**I/O Space** 0: Ignore downstream I/O transactions; I/O cycles with address falling in the claimed range will be forwarded to the SB. 1: Enable downstream I/O cycle to this port if its address falling in the claimed range of this device.	

Offset Address: 7-6h (D2F0)
Status Register **Default Value: 0010h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set whenever a poisoned TLP is received, regardless the state of Parity Error Enabled (see RPTYERR_PEG (Rx4[6]) for details)
14	RW1C	0	**Signaled System Error** This bit is set when: 1. A device sends an ERR_FATAL or ERR_NONFATAL message 2. RSERR_PEG (Rx4[8]) = 1
13	RW1C	0	**Received Master Abort** This bit is set when receiving a completion with Unsupported Request Completion Status
12	RW1C	0	**Received Target Abort** This bit is set when receiving a completion with Completer Abort Completion Status
11	RW1C	0	**Signaled Target Abort** This bit is set when completing a Request with Completer Abort Completion Status
10:9	–	0	**Reserved (Always 0)**
8	RW1C	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx4[6]) is set and either one of the following two conditions occurs: 1. Requestor receives a Completion marked poisoned 2. Requestor poisons a write Request
7:5	–	0	**Reserved**
4	RO	1	**Capabilities List** Indicate the presence of an extended capability list item. Always set to 1 for PCI Express device
3	RO	0	**Interrupt Status** Indicate an INTx message is pending internally
2:0	–	0	**Reserved**

Offset Address: 8h (D2F0)
Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Revision Code**

Offset Address: 0B-9h (D2F0)
Class Code **Default Value: 060400h**

Bit	Attribute	Default	Description
23:0	RO	060400h	**Class Code**

Offset Address: 0Ch (D2F0)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Cache Line Size – Reserved (No impact on functionality)**

Offset Address: 0Dh (D2F0)
Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Reserved (Hardwired to 0)**

Offset Address: 0Eh (D2F0)
Header Type **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Header Type Code** 01: PCI-PCI Bridge

Offset Address: 0Fh (D2F0)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**BIST Support**

Offset Address: 17-10h (D2F0)
Base Address Register **Default Value: 00h**

Bit	Attribute	Default	Description
63:0	RO	00h	**Base Address**

Offset Address: 18h (D2F0)
Primary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Primary Bus Number**

Offset Address: 19h (D2F0)
Secondary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Secondary Bus Number**

Offset Address: 1Ah (D2F0)
Subordinate Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Subordinate Bus Number**

Offset Address: 1Ch (D2F0)
I/O Base **Default Value: F0h**

Bit	Attribute	Default	Description
7:4	RW	1111	**I/O Base (AD[15:12] - inclusive)** This bridge will forward the cycles from primary side to PCI if the IO address AD[15:12] is between IO base and IO limit (Rx1D)
3:0	RO	0	**I/O Addressing Capability** 0 means IO addressing is 16-bit only.

Offset Address: 1Dh (D2F0)
I/O Limit **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:4	RW	0	**I/O Limit (AD[15:12] - inclusive)**	**RIOLM_PEG[15:12]**
3:0	RO	0	**I/O Addressing Capability** 0 means IO addressing is 16-bit only.	

Offset Address: 1F-1Eh (D2F0)
Secondary Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set when secondary side receives a poisoned TLP regardless of RPTYERR_PEG (Rx4[6])
14	RW1C	0	**Received System Error** This bit is set when RSERR_PEG (Rx4[8]) is 1 and a device sends an ERR_FATAL or ERR_NONFATAL message
13	RW1C	0	**Received Master Abort**
12	RW1C	0	**Received Target Abort**
11	RW1C	0	**Signaled Target Abort**
10:9	—	0	**Reserved**
8	RW1C	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx4[6]) is set and either one of the following two conditions occurs: 1. Requestor receives a Completion marked poisoned. 2. Requestor poisons a write Request
7:0	—	0	**Reserved**

Offset Address: 21-20h (D2F0)
Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Memory Base (AD[31:20] – inclusive)** The address bits [19:0] is not decoded.
3:0	RO	0000	**Reserved** Always reads 0.

Offset Address: 23-22h (D2F0)
Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	000h	**Memory Limit (AD[31:20] – inclusive)** The address [19:0] is not decoded.
3:0	RO	0000	**Reserved** Always reads 0.

Offset Address: 25-24h (D2F0)
Prefetchable Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Prefetchable Memory Base AD[31:20]**
3:0	RO	0000	**Reserved** Always reads 0.

Offset Address: 27-26h (D2F0)
Prefetchable Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	000h	**Prefetchable Memory Limit AD[31:20]**
3:0	RO	0000	**Reserved** Always reads 0.

Offset Address: 2B-28h (D2F0)
Prefetchable Memory Upper Base **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	00h	**Reserved** Always reads 0.
3:0	RW	0000	**AD[35:32]** This chip supports up to 16G

Offset Address: 2F-2Ch (D2F0)
Prefetchable Memory Upper Limit **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	00h	**Reserved** Always reads 0.
3:0	RW	0000	**AD[35:32]** This chip supports up to 16G

Offset Address: 31-30h (D2F0)
I/O Base Upper **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	00h	**I/O Base Upper 16 bits Address**

Offset Address: 33-32h (D2F0)
I/O Limit Upper **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	00h	**I/O Limit Upper 16 bits Address**

Offset Address: 34h (D2F0)
Capability Pointer **Default Value: 40h**

This register contains the offset address from the start of the configuration space.

Bit	Attribute	Default	Description
7:0	RO	40h	**Capability Pointer** Always reads 40h. Capability Pointer link list: Rx34 → Rx40 → Rx68 → Rx70 → NULL

Offset Address: 3Ch (D2F0)
Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**INT Line** (For Software Use Only)

Offset Address: 3Dh (D2F0)
Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**INT Pin** 01: INTA

Offset Address: 3F-3Eh (D2F0)

Bridge Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:7	—	00h	**Reserved**
6	RW	0	**Secondary Bus Reset** 0: No reset 1: Triggers a warm reset on the corresponding PCI Express Port
5	—	0	**Reserved**
4	RW	0	**Base VGA 16 bits Decode** 0: All VGA alias range will be forwarded 1: Only forward base VGA range (Alias range will not be forwarded)
3	RW	0	**VGA Compatible I/O and Memory Address Range** 0: Do not forward VGA compatible memory and I/O 1: Forward VGA compatible memory and I/O Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.
2	RW	0	**Block/Forward ISA I/O Cycles** 0: Forward all I/O cycles with address in the range defined by the I/O Base and I/O Limit 1: Do not forward ISA I/O that are in the top 768 bytes of each 1K byte block address range
1	RW	0	**SERR Enable** Controls the forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary 0: Disable 1: Enable
0	RW	0	**Parity Error Response Enable** 0: Ignore the response to poisoned TLPs 1: Enable the response to poisoned TLPs

PCI Express Capability Registers (40-63h)

Offset Address: 40-41h (D2F0)

PCI Express List **Default Value: 6810h**

Bit	Attribute	Default	Description
15:8	RO	68h	**Next Pointer**
7:0	RO	10h	**Capability ID**

Offset Address: 43-42h (D2F0)

PCI Express Capabilities **Default Value: 0041h**

Bit	Attribute	Default	Description
15:14	—	0	**Reserved**
13:9	RO	0	**Interrupt Message Number**
8	RO	0	**Slot Implemented** This bit when set indicates that the PCI Express Link associated with this Port is connected to a slot (as compared to being connected to an integrated component or being disabled),
7:4	RO	0100	**Device / Port Type** 0100b: Root Port of PCI Express Root Complex
3:0	RO	1	**Capability Version**

Offset Address: 47-44h (D2F0)
Device Capabilities **Default Value: 0000 0nn1h**

Bit	Attribute	Default	Description
31:28	–	0	**Reserved**
27:26	RO	0	**Captured Slot Power Limit Scale**
25:18	RO	00h	**Captured Slot Power Limit Value**
17:15	–	0	**Reserved**
14	RO	0	**Power Indicator Present** Reserved
13	RO	0	**Attention Indicator Present** Reserved
12	RO	0	**Attention Button Present** Reserved
11:9	RO	111	**Endpoint L1 Acceptable Latency** 111b: more than 64us
8:6	RO	xxx	**Endpoint L0s Acceptable Latency** This field is set up through PHY negotiation process.
5	RO	0	**Extended Tag Field Supported** 0: 5-bit Tag field supported 1: 8-bit Tag field supported
4:3	RO	00	**Phantom Functions Supported** Reserved
2:0	RO	001	**Max Payload Size Supported** 001b: 32QW (256 bytes)

Offset Address: 49-48h (D2F0)
Device Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15	–	0	**Reserved**
14:12	RO	000	**Max Read Request Size** 000b: 128 bytes This field sets the maximum Read Request size for the device as a Requestor.
11	RW	0	**Enable No Snoop** If this bit is set to 1, the device is **permitted** to set the No Snoop bit in the Requestor Attributes of the transactions it initiate that do not require hardware enforced cache coherency.
10	RWS	0	**Auxiliary Power PM Enable** This bit when set enables device to draw AUX power independent of PME AUX power.
9	RO	0	**Phantom Functions Enable** Not supported.
8	RO	0	**Extended Tag Field Enable** Not supported.
7:5	RW	000	**Max Payload Size** Maximum TLP payload size.
4	RW	0	**Enable Relaxed Ordering** If this bit is set to 1, the device is **permitted** to set the Relaxed Ordering bit in the Requestor Attributes of the transactions it initiate that do not require strong write ordering.
3	RW	0	**Unsupported Request Reporting Enable**
2	RW	0	**Fatal Error Reporting Enable** For a Root Port, the reporting of Fatal errors is internal to the root. No external ERR_FATAL message is generated.
1	RW	0	**Non-Fatal Error Reporting Enable** For a Root Port, the reporting of Non-Fatal errors is internal to the root. No external ERR_NONFATAL message is generated.
0	RW	0	**Correctable Error Reporting Enable** For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_COR message is generated.

Offset Address: 4B-4Ah (D2F0)

Device Status **Default Value: 0010h**

Bit	Attribute	Default	Description
15:6	–	0	**Reserved**
5	RO	0	**Transactions Pending** This bit when set indicates that the Port has issued Non-Posted Requests on its own behalf (using the Port's own Requestor ID) which have not been completed.
4	RO	1	**AUX Power Detected**
3	RW1C	0	**Unsupported Request Detected**
2	RW1C	0	**Fatal Error Detected**
1	RW1C	0	**Non-Fatal Error Detected**
0	RW1C	0	**Correctable Error Detected**

Offset Address: 4F-4Ch (D2F0)

Link Capabilities **Default Value: 0000 0D01h**

Bit	Attribute	Default	Description
31:24	RO	00h	**Port Number** This field indicates the PCI Express Port number for the given PCI Express Link.
23:18	–	0	**Reserved**
17:15	RO	000	**L1 Exit Latency** 000: less than 1us. The value reported indicates the length of time this Port requires to complete transition from L1 to L0.
14:12	RO	000	**L0s Exit Latency** 000: less than 64ns. The value reported indicates the length of time this Port requires to complete transition from L0s to L0.
11:10	RO	11	**Active State Link PM (ASPM) Support** 11b: L0s and L1 supported. This field indicates the level of ASPM supported on the PCI Express Link.
9:4	RO	010000	**Maximum Link Width** 010000b: x16 Link width
3:0	RO	1	**Maximum Link Speed** 0001b: 2.5Gb/s Link speed

Offset Address: 51-50h (D2F0)

Link Control **Default Value: 0000h**

Bit	Attribute	Default	Description	Mnemonic
15:8	–	0	**Reserved**	
7	RW	0	**Extended Synch** 0: FCU Timer limit is 30us 1: FCU Timer limit is 120us.	LCES_PEG
6	RW	0	**Common Clock Configuration** 0: Indicates that this Port and the component on the opposite end of the Link are operating with asynchronous reference clock. 1: Indicates that this Port and the component on the opposite end of the Link are operating with a distributed common reference clock.	
5	RW	0	**Retrain Link** A write of 1 to this bit initiates Link retrained by directing the Physical Layer LTSSM to the Recovery state.	
4	RW	0	**Link Disable** This bit disables the Link when set to 1.	
3	RO	0	**Read Completion Boundary** 0: 64 byte	
2	–	0	**Reserved**	
1:0	RW	00	**Link Active State PM (ASPM) Control** 00b: Disabled 01b: L0s Entry Enabled 10b: L1 Entry Enabled 11b: L0s and L1 Entry Enabled	

Offset Address: 53-52h (D2F0)
Link Status **Default Value: 0nn1h**

Bit	Attribute	Default	Description
15:13	—	0	**Reserved**
12	RO	0	**Slot Clock Configuration** 0: Use an independent clock irrespective of the presence of a reference on the connector. 1: Use the same physical reference clock that the platform provides on the connector.
11	RO	0	**Link Training** This bit indicated that Link training is in progress (Physical Layer LTSSM is in Configuration or Recovery state) or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit once Link training is complete.
10	RO	0	**Training Error** Set when a Link training error occurred. Cleared by hardware upon successfully training of the Link to the L0 Link state.
9:4	RO	xxxxxx	**Negotiated Link Width** 000001: x1 000010: x2 000100: x4 001000: x8 010000: x16
3:0	RO	0001	**Link Speed** 0001: 2.5Gb/s negotiated Link speed.

Offset Address: 57-54h (D2F0)
Slot Capabilities **Default Value: 0000 0060h**

Bit	Attribute	Default	Description
31:19	RO	00h	**Physical Slot Number** Physical slot number attached to the Port.
18:17	—	0	**Reserved**
16:15	RO	0	**Slot Power Limit Scale** Write to the field causes the Port to send the Set_Slot_Power_Limit message.
14:7	RO	00h	**Slot Power Limit Value** Write to the field causes the Port to send the Set_Slot_Power_Limit message.
6	RO	1	**Hot-plug Capable**
5	RO	1	**Hot-plug Surprise**
4	RO	0	**Power Indicator Present**
3	RO	0	**Attention Indicator Present**
2	RO	0	**MRL Sensor Present**
1	RO	0	**Power Controller Present**
0	RO	0	**Attention Button Present**

Offset Address: 59-58h (D2F0)
Slot Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	—	0	**Reserved**
10	RO	0	**Power Controller Control** 0: Power On 1: Power Off
9:8	RW	0	**Power Indicator Control** 00: Reserved 01: On 10: Blink 11: Off Writes to this field cause the Port to send the appropriate POWER_INDICATOR_* Message.
7:6	RW	0	**Attention Indicator Control** 00: Reserved 01: On 10: Blink 11: Off Writes to this field cause the Port to send the appropriate ATTENTION_INDICATOR_* Message.
5	RW	0	**Hot-Plug Interrupt Enable** This bit when set enables generation of Hot-Plug interrupt on enabled Hot-Plug events.
4	RW	0	**Command Completed Interrupt Enable** This bit when set enables the generation of Hot-Plug interrupt when a command is completed by the Hot-Plug controller.
3	RW	0	**Presence Detect Changed Enable** This bit when set enables the generation of Hot-Plug interrupt or Wakeup event on a presence detect changed event.
2	RO	0	**MRL Sensor Changed Enable**
1	RO	0	**Power Fault Detected Enable**
0	RW	0	**Attention Button Pressed Enable** This bit when set enables the generation of Hot-Plug interrupt or Wakeup event on an Attention Button pressed event.

Offset Address: 5A-5Bh (D2F0)

Slot Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:7	—	0	**Reserved**
6	RO	0	**Presence Detect State** 0: Slot empty 1: Card present in slot
5	RO	0	**MRL Sensor State**
4	RW1C	0	**Command Completed**
3	RW1C	0	**Presence Detect Changed**
2	RO	0	**MRL Sensor Changed**
1	RO	0	**Power Fault Detected**
0	RW1C	0	**Attention Button Pressed**

Offset Address: 5D-5Ch (D2F0)

Root Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	—	0	**Reserved**
3	RW	0	**PME Interrupt Enable** 0: Disable 1: Enable interrupt generation upon receipt of a PME message as reflected in the PME status register bit. A PME interrupt is also generated if the PME status register bit is set when this bit is set from a cleared state.
2	RW	0	**System Error on Fatal Error Enable** 0: Disable 1: Enable generation of a System Error if a Fatal Error (ERR_FATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
1	RW	0	**System Error on Non-Fatal Error Enable** 0: Disable 1: Enable generation of a System Error if a Non-Fatal Error (ERR_NONFATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
0	RW	0	**System Error on Correctable Error Enable** 0: Disable 1: Enable generation of a System Error if a Correctable Error (ERR_COR) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.

Offset Address: 63-60h (D2F0)

Root Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	—	0	**Reserved**
17	RO	0	**PME Pending** 0: No pending PME 1: Indicates that another PME is pending when the PME Status (bit 16) is set.
16	RW1C	0	**PME Status** Indicates that the PME was asserted by the Requestor ID indicated in PME Requestor ID (bit[15:0]).
15:0	RO	0	**PME Requestor ID** The Requestor ID of the last PME Requestor.

PCI Power Management Capability Structure Registers (68-6Fh)

Offset Address: 6B-68h (D2F0)

Power Management Capabilities **Default Value: C802 7001h**

Bit	Attribute	Default	Description
31:27	RO	11001	**PME Support** Bit 31, 30 and 27 are set to 1b (PME Message will be forwarded).
26	RO	0	**D2 Support**
25	RO	0	**D1 Support**
24:22	RO	0	**AUX Current**
21	RO	1	**Device Specific Initialization**
20:19	—	0	**Reserved**
18:16	RO	010	**Version**
15:8	RO	70h	**Next Capability Pointer**
7:0	RO	01h	**Capability ID**

Offset Address: 6F-6Ch (D2F0)
Power Management Status/Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Power Management Data**
23:16	RO	—	**Reserved**
15	RW1CS	0	**PME Status** This bit's setting is not modified by hot, warm, or cold reset.
14:13	RO	0	**Data Scale**
12:9	RW	0	**Data Select**
8	RWS	0	**PME Enable** This bit's setting is not modified by hot, warm, or cold reset.
7:2	RO	0	**Reserved**
1:0	RW	0	**Power State**

PCI Message Signal Interrupt (MSI) Capability Structure Registers (70-87h)

Offset Address: 73-70h (D2F0)
MSI Capability Support **Default Value: 0180 0005h**

Bit	Attribute	Default	Description
31:25	—	0	**Reserved**
24	RO	1	**This MSI capability supports pre-vector masking capability**
23	RO	1	**This MSI capability supports 64 bit message address only**
22:20	RW	000	**Multiple Message Enable** 000: 1message allocated 001: 2 message allocated 010: 4 message allocated 011: 8 message allocated 100: 16 message allocated 101: 32 message allocated 11x: Reserved
19:17	RO	000	**Multiple Message Capable** 000: 1message requested 001: 2 message requested 010: 4 message allocated 011: 8 message allocated 100: 16 message requested 101: 32 message requested 11x: Reserved
16	RW	0	**MSI Enable** 0: This Port is prohibited from using MSI to request service 1: This Port is permitted to use MSI to request service.
15:8	RO	0	**Next Capability Pointer**
7:0	RO	05h	**Capability ID**

Offset Address: 77-74h (D2F0)
System-Specified Message Address - Low **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	00h	**System-Specified Message Address Bit [31:2]**
1:0	RO	00	**System-Specified Message Address Bit [1:0]** These bits will always read as 0

Offset Address: 7B-78h (D2F0)
System-Specified Message Address - High **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	00h	**System-Specified Message Address Bit [63:36]** These bits will always read as 0 since this chip supports address up to A35.
3:0	RW	0	**System-Specified Message Address Bit [35:32]**

Offset Address: 7D-7Ch (D2F0)
Message Data **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Message Data** The message data is to be put on data [15:0] of MSI cycles

Offset Address: 83-80h (D2F0)
Message Mask Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	00h	**Mask Bit**
0	RW	0	**Mask Bit for Message 0**

Offset Address: 87-84h (D2F0)
Message Pending Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	00h	**Pending Bit**
0	RO	0	**Pending Bit for Message 0**

PCI Express Transaction Layer Registers (A0-A4h)

Offset Address: A0h (D2F0)
Downstream Control I **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Cycles Have Traffic Class TC1** 0: Disabled 1: Enabled.
6	RW	0	**Downstream Cycles Have Attribute "No Snoop" Set** 0: Disabled 1: Enabled.
5	RW	0	**Downstream Cycles Have Attribute "Relaxed Ordering" Set** 0: Disabled 1: Enabled.
4	RW	0	**Downstream Lock Cycle Support** 0: Disabled 1: Enabled.
3	RW	0	**Downstream Arbitration Scheme** 0: Fixed priority: VC1 CPL > VC0 CPL > Down Stream Command 1: Round Robin arbitration priority between VC1 CPL, VC0 CPL and Down Stream Command
2	RW	0	**Downstream Post-Write Allowed to Pass IOW** 0: Not allowed. 1: Allowed.
1	RW	0	**Downstream Post-Write Allowed to Pass Read** 0: Not allowed. 1: Allowed.
0	RW	1	**Downstream Pipeline** 0: Disabled 1: Enabled.

Offset Address: A1h (D2F0)
Downstream Control II **Default Value: 04h**

Bit	Attribute	Default	Description
7	RW1C	0	**Downstream Configuration Completion Status** 0: Normal completion. 1: At least one configuration request ended with a CRS (Configuration Request Retry Status) completion.
6:4	–	0	**Reserved**
3	RW	0	**Reserved**
2:0	RW	100	**C2P Read Completion Timeout Timer** 000: Reserved 001: 1ms 010: Reserved 011: 10ms (Spec. lower bound) 100: 30ms 101: 50ms (Spec. higher bound) 110: 100ms 111: Reserved

Offset Address: A4h (D2F0)

Upstream Control **Default Value: 10h**

Bit	Attribute	Default	Description
7	RW	0	**Upstream Address A35~A31 Forced to 0** 0: Disabled. 1: Enabled for system testing or loop back mode test. The upcoming data may be checked in the system memory
6	—	0	**Reserved**
5	RW	0	**Upstream Checking Malformed TLP through "Byte Enable Rule" And "Over 4K Boundary Rule"** 0: Disabled. 1: Enabled.
4	RW	1	**Downstream Read Wait Till The Upstream Write Data Flushed** 0: Disabled. 1: Enabled.
3:2	—	0	**Reserved**
1	RW	0	**VC1 Request Queue Usage** (when VC1 is disabled in the capability header; i.e. Rx144[0] = 0) 0: Disabled. 1: Enabled, it allows Transaction Layer map non-snoop upstream request through VC1 Request Queue to the Central Traffic Controller (Note that when this bit is 1, bit-0 has to be 0).
0	RW	0	**Disable Virtual Channel 1 Support** 0: Enable VC1, data FIFO of VC1 is used by VC1 1: Disable VC1, data FIFO of VC1 is reallocated to VC0, which doubles the size of VC0 data FIFO..

PCI Express Data Link Layer Registers (B0-B8h)

Offset Address: B0h (D2F0)

Ack/Nak Latency Timer Limit **Default Value: 0Ch**

Bit	Attribute	Default	Description
7:0	RW	0Ch	**Timer Limit for Ack/Nak Latency Timer and Update FC Latency Timer (in unit of 250MHz)** 00: 4 x 1 Clocks 01: 4 x 2 Clocks 02: 4 x 3 Clocks. 0n: 4 x (n+1) Clocks FF: 4 x 256 Clocks.

Offset Address: B1h (D2F0)

Replay Timer Limit **Default Value: 12h**

Bit	Attribute	Default	Description
7:0	RW	12h	**Replay Timer Limit (In unit of 250MHz)** 00: 8 x 1 Clocks 01: 8 x 2 Clocks 02: 8 x 3 Clocks 0n: 8 x (n+1) Clocks FF: 8 x 256 Clocks.

Offset Address: B2h (D2F0)
FCU Control and Status **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW1C	0	**FCU Timeout Status** 1 Means the FCU timeout has occurred
6	RW	1	**FCU Receive Timer Enable Control** 0: Disable the timeout mechanism 1: Enable the timeout mechanism
5	RW	0	**FCU Receive Timer Limit** 0: Timeout limit of 200us 1: Timeout limit of 300us
4	RW	0	**FCU Receive Timer Reset Control** 0: Timer reset by FCI/FCU only 1: Timer reset by any received DLLPs
3:0	–	0	**Reserved**

Offset Address: B3h (D2F0)
Replay Timer Control **Default Value: 80h**

Bit	Attribute	Default	Description
7:6	RW	10	**Replay Timer Control while Rewind** (resend those DLLPs which do not have corresponding ACK/NAK received) 00: Hold Replay Timer during rewind. 01: During rewind, if ACK/NAK comes in, reset and hold the Replay Timer. 10: During rewind, reset and hold the Replay Timer as long as the Retry Buffer is empty. 11: Reserved.
5:3	–	0	**Reserved**
2:0	RW	000	**Count of Replay Timer Expired During RXL0s** (Receiving Physical in L0s state) **Before Resend the TLP** **When Rx50[7], LCES_PEG, is set to 0:** 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 1 x Replay timer expired 010: Resend the TLP after 2 x Replay timer expired 011: Resend the TLP after 4 x Replay timer expired 100: Resend the TLP after 8 x Replay timer expired 101: Resend the TLP after 16 x Replay timer expired 110: Resend the TLP after 32 x Replay timer expired 111: Resend the TLP after 64 x Replay timer expired **When RX50[7], LCES_PEG, is set to 1:** 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 16 x Replay timer expired 010: Resend the TLP after 32 x Replay timer expired 011: Resend the TLP after 64 x Replay timer expired 100: Resend the TLP after 128 x Replay timer expired 101: Resend the TLP after 256 x Replay timer expired 110: Resend the TLP after 512 x Replay timer expired 111: Resend the TLP after 1024 x Replay timer expired

Offset Address: B4h (D2F0)
Arbitration Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	–	0	**Reserved**
3	RW	0	**TLP vs. Flow Control Initialization for VC0 in Arbitration** 0: TLP is not allowed to pass FCI2 for VC0 1: TLP is allowed to pass FCI2 for VC0
2:0	RW	000	**Data Link TX Packets Arbitration Scheme** 000: Round Robin 001: Reserved. 010: Strict priority: TLP > ACK/NAK > FCU 011: Strict priority: TLP > FCU > ACK/NAK 100: Strict priority: ACK/NAK > TLP > FCU 101: Strict priority: ACK/NAK > FCU > TLP 110: Strict priority: FCU > TLP > ACK/NAK 111: Strict priority: FCU > ACK/NAK > TLP

Offset Address: B5h (D2F0)

FCU Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	–	0	**Reserved**
6	RW	0	**FCU (Flow Control Unit) Timer Control** 0: Update flow control credit when either Transaction Layer requested packets being sent or when FCU timer expired 1: Update flow control credit only when FCU timer expired
5:4	RW	00	**ACK DLLP Collapse Method** 00: Send ACK when the latency timer RACKLTLM (RxB0) expired. 01: Send ACK every 4 correct TLP has been received 10: Send ACK every 8 correct TLP has been received 11: Send ACK every 16 correct TLP has been received
3:2	–	0	**Reserved**
1	RW	0	**FCI (Flow Control Initialization) Process End Condition** 0: Complete FCI process when TLP/FCU has been received 1: Do not complete FCI process even when TLP/FCU has been received
0	RW	0	**VC1 FCI DLLP Transmission Scheme** 0: Transmit FCI DLLP only when FCI timer expired 1: Transmit FCI DLLP continuously as long as the FCI process is not finished

Offset Address: B6h (D2F0)

Transaction / Link Layer Checking Control **Default Value: 03h**

Bit	Attribute	Default	Description
7:5	–	0	**Reserved**
4	RW	0	**VC Negotiate Pending Control for VC1** 0: Assert VC negotiation pending after VC1 is enabled 1: Assert VC negotiation pending after RESET is de-asserted
3	–	0	**Reserved**
2	RW	0	**ECRC Checking Control for the Case of TD equals to1 but no ECRC field in TLP** 0: Ignore the error 1: Report error to Transaction Layer, which will mark the TLP as a Malformed TLP
1	RW	1	**Length Malform Report Control** 0: Do not report length malform to Transaction Layer 1: Report length malform to Transaction Layer
0	RW	1	**LCRC Checking Control** 0: Do not check LCRC 1: Check LCRC

Offset Address: B8h (D2F0)

Data Link Layer Header Position **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	–	0	**Reserved**
0	RW	0	**Data Link Layer Header Position:** 0: SDP (Start DLLP) can be in Lane0/4/8/12 1: SDP (Start DLLP) always at Lane0.

PCI Express Physical Layer Registers (C0-CBh)

Offset Address: C3-C0h (D2F0)

PHY Control **Default Value: 0000 0006h**

Bit	Attribute	Default	Description
31:13	—	0	**Reserved**
12:8	RW	00h	**PHY Lane Configuration Setting** 10000: x16 with normal connection 01000: x8 with normal connection 00100: x4 with normal connection 00010: x2 with normal connection 00001: x1 with normal connection 01111: x16 with reverse connection 10111: x8 with reverse connection 11011: x4 with reverse connection 11101: x2 with reverse connection 11110: x1 with reverse connection 10101: force into L0s state (for testing and measurement used only) 00000: Use PHY negotiation Other values are not allowed.
7	RW	0	**Quick Timeout Counter Setting** When set to 1, following timeout counters will be shorter: TIMEOUT_2MS → TIMEOUT_4US TIMEOUT_12MS → TIMEOUT_24US TIMEOUT_24MS → TIMEOUT_48US TIMEOUT_48MS → TIMEOUT_96US TIMEOUT_1024TS → TIMEOUT_32TS Receiver Detection: 15x1024ns → 1x1024ns
6	RW	0	**Disable Data Scrambling/Descrambling** 0: Enable 1: Disable
5:3	RW	000	**Loopback Mode Selection (Applies to All 16 Lanes)** 000 : No loop back 001: PHYLS loopback from TX end to RX end 010: PHYES loopback from TX end to RX end 011: Reserved 100: Reserved 101: PHYLS loopback from RX end to TX end 110: PHYES loopback from RX end to TX end 111: Reserved
2:0	RW	3	**COMMA Detection Window** 000, 001: Illegal values Others: Delay number of T to determine correct lane-to-lane deskew value

Offset Address: C7-C4h (D2F0)

Elastic Buffer Base Registers for Lane 0 to 7 **Default Value: 4444 4444h**

Bit	Attribute	Default	Description
31	—	0	**Reserved**
30:28	RW	4h	**Elastic Buffer Base Register for Lane 7** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
27	—	0	**Reserved**
26:24	RW	4h	**Elastic Buffer Base Register for Lane 6** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
23	—	0	**Reserved**
22:20	RW	4h	**Elastic Buffer Base Register for Lane 5** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
19	—	0	**Reserved**
18:16	RW	4h	**Elastic Buffer Base Register for Lane 4** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
15	—	0	**Reserved**
14:12	RW	4h	**Elastic Buffer Base Register for Lane 3** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
11	—	0	**Reserved**
10:8	RW	4h	**Elastic Buffer Base Register for Lane 2** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
7	—	0	**Reserved**
6:4	RW	4h	**Elastic Buffer Base Register for Lane 1** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
3	—	0	**Reserved**
2:0	RW	4h	**Elastic Buffer Base Register for Lane 0** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations

Offset Address: CB-C8h (D2F0)

Elastic Buffer Base Registers for Lane 8 to 15 **Default Value: 4444 4444h**

Bit	Attribute	Default	Description
31	—	0	**Reserved**
30:28	RW	4h	**Elastic Buffer Base Register for Lane 15** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
27	—	0	**Reserved**
26:24	RW	4h	**Elastic Buffer Base Register for Lane 14** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
23	—	0	**Reserved**
22:20	RW	4h	**Elastic Buffer Base Register for Lane 13** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
19	—	0	**Reserved**
18:16	RW	4h	**Elastic Buffer Base Register for Lane 12** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
15	—	0	**Reserved**
14:12	RW	4h	**Elastic Buffer Base Register for Lane 11** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
11	—	0	**Reserved**
10:8	RW	4h	**Elastic Buffer Base Register for Lane 10** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
7	—	0	**Reserved**
6:4	RW	4h	**Elastic Buffer Base Register for Lane 9** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
3	—	0	**Reserved**
2:0	RW	4h	**Elastic Buffer Base Register for Lane 8** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations

PCI Express Power Management Module Registers (D0-D3h)

Offset Address: D3-D0h (D2F0)

PMC Control **Default Value: 0000 0050h**

Bit	Attribute	Default	Description
31:24	RW	00h	**Idle Period to Enter ASL1** Minimum time period is 128ns 00: 128ns 01: 2x128ns 02: 3x128ns ... FF: 256x128ns
23:16	RW	00h	**Idle Period to Enter L0s** Minimum time period is 128ns (L0SLIM_PEG = 00) 00: 128ns 01: 2x128ns 02: 3x128ns ... FF: 256x128ns
15	RW1C	0	**Error Status Report** This bit is set when device cannot have electrical idle after the waiting period programmed at RxD1[6:4] expired.
14	—	0	**Reserved**
13:12	RW	0	**Electrical Idle Waiting Period before Move to L1 State** (after issue ACK to the L1 request from the device). 00: Always wait for electrical idle 01: Wait 32 clock 10: Wait 64 clock 11: Reserved
11:10	—	0	**Reserved**
9:8	RW	0	**Downstream Cycles Triggered C2P Cycles, Period of Staying at L0 Before Returned to L1 for PHY** (when PMU is in non-D0 state) 00: immediately 01: 1 cfgW or message + delay10T 10: 1 32QW +1cfgW or message+ delay10T 11: 2 32QW +1 cfgW or message +delay10T
7	—	0	**Reserved**
6:4	RW	101	**Timeout Period** This timer is used when waiting for ACK from a device after issued PME_TURNOFF message to notify the device to move to power down mode. 000: 1us 001: 2us 010: 4us 011: 8us 100: 16us 101: 32us 110: 64us 111: 128us
3:2	—	0	**Reserved**
1	RW	0	**Link Loopback** 0: Normal operation 1: Direct device to enter Loopback mode, receiving data in the device will be sent to the transmit side
0	RW	0	**LTSSM State During Link Reconfigure Link Width** 0: When reconfigure link width, LTSSM must be in Detect state 1: When reconfigure link width, LTSSM can be in Configuration state

PCI Express Message Controller Related Registers (D8h)

Offset Address: D8h (D2F0)

PMC Express Message Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	W1C	0	**Excessive Errors Occurred But Not Reported in MSGC** 0: Normal operation. 1: There are errors not reported to the system
6:0	–	0	**Reserved**

PCI Express Electrical PHY Registers (E0-EAh)

Offset Address: E0h (D2F0)

PHYES Module Control (For Both x16 and x4 Root Ports) **Default Value: 02h**

Bit	Attribute	Default	Description
7:4	–	0	**Reserved**
3:1	RW	1	**Charge Pump Current Control**
0	RW	0	**Charge Pump Style Control**

Offset Address: E1h (D2F0)

PHYES Module Related Control **Default Value: 08h**

Bit	Attribute	Default	Description
7:6	–	0	**Reserved**
5	RW	0	**Bypass PHYES Receiver Detection Function** 0: Not Bypass 1: Bypass receiver detection
4	RW	0	**Receiving Polarity Change Control** 0: Have the same polarity on the loop-back/received data 1: Have reverse polarity on the loop-back/received data
3:2	RW	10	**Squelch Window Select (64~175mv)**
1	RW	0	**Electrical Idle State Exit Condition: Number of Non Idle Signal Detected Before Exit Idle State** 0: 2 bits. 1: 10 bits.
0	RW	0	**Electrical Idle State Enter Condition: Number of Idle Signal Detected Before Enter Idle State** 0: 2 bits 1: 10 bits

Offset Address: E2h (D2F0)

First 8 Lanes PHYES Module Control – Rx/Tx I **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	–	0	**Reserved**
5	RW	0	**PHYES Clock Buffer Power Down on Lane 0-7** 0: All enable. 1: Power down
4	RW	0	**Lane 4-7 Clock Buffer Power Down** 0: All enable 1: Lane 4-7 power down
3:2	RW	00	**Receiver Input Rise Delay (duty cycle adjustment for the first 8 lanes)** 00: 0 ps 01: 10 ps 10: 40 ps 11: 80 ps
1:0	RW	00	**Receiver Input Fall Delay (duty cycle adjustment for the first 8 lanes)** 00: 0 ps 01: 10 ps 10: 40 ps 11: 80 ps

Offset Address: E3h (D2F0)
First 8 Lanes PHYES Module Control – Rx/Tx II **Default Value: 02h**

Bit	Attribute	Default	Description
7	RW	0	**PCI-E Pads Driving Control** 0: Autocomp 1: Manual setting through bits [2:0]
6:4	–	0	**Reserved**
3	RW	0	**CDR Filter Depth** 0: Filter depth = 3 1: Filter depth = 2
2:0	RW	010	**First 8 Lanes, Lane 0 –7, Termination Resistance Selection** Resistance Range: 62Ω (000b) ~ 43Ω (111b) Default: 50Ω (010b)

Offset Address: E4h (D2F0)
First 8 Lanes PHYES Module Control – Rx/Tx III **Default Value: 44h**

Bit	Attribute	Default	Description
7:4	RW	4h	**Pre/De-Emphasis Level Selection**
3:0	RW	4h	**Driver Current Source Selection**

Offset Address: E8h (D2F0)
Second 8 Lanes PHYES Module Control – Rx/Tx I **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	–	0	**Reserved**
4	RW	0	**Lane 12-15 Clock Buffer Power Down** 0: All enable 1: Lane 12~15 power down
3:2	RW	00	**Receiver Input Rise Delay (duty cycle adjustment for the second 8 lanes)** 00: 0 ps 01: 10 ps 10: 40 ps 11: 80ps
1:0	RW	00	**Receiver Input Fall Delay (duty cycle adjustment for the second 8 lanes)** 00: 0 ps 01: 10 ps 10: 40 ps 11: 80 ps

Offset Address: E9h (D2F0)
Second 8 Lanes PHYES Module Control – Rx/Tx II **Default Value: 02h**

Bit	Attribute	Default	Description
7	RW	0	**PCI-E Pads Driving Control** 0: Autocomp 1: Manual setting through bits [2:0]
6	–	0	**Reserved**
5	RW	0	**PHYES Clock Buffer Power Down on Lane 8-15** 0: All enable. 1: Power down
4:3	–	0	**Reserved**
2:0	RW	010	**Second 8 Lanes, Lane 8 –15, Termination Resistance Selection** Resistance Range: 62Ω (000b) ~ 43Ω (111b) Default: 50Ω (010b)

Offset Address: EAh (D2F0)
Second 8 Lanes PHYES Module Control – Rx/Tx III **Default Value: 44h**

Bit	Attribute	Default	Description
7:4	RW	4h	**Pre/De-Emphasis Level Selection**
3:0	RW	4h	**Driver Current Source Selection**

PCI Express Electrical PHY Test Registers (F0-F7h)

Offset Address: F3-F0h (D2F0)

PHY Test **Default Value: 0600 0000h**

Bit	Attribute	Default	Description	Mnemonic
31	RW	0	**Electrical PHY Test Mode Enable** Program this bit to 1 to start Electrical PHY test	EPHYTST_PEG
30:28	—	0	**Reserved**	
27:24	RW	6h	**Test Pattern Check Length** Number of T when the receiving side starts to check transmitted and received patterns Suggested Value Settings: (Lane 0 for example) RxC0[5:3] = 001b: RxC4[2:0] + 2 RxC0[5:3] = 010b: RxC4[2:0] + 2 + (Loopback Path Latency/4ns) + 1	
23:20	RW	0	**Select Test Pattern** 0000: Reserved 0001: User define, use RxF6[9:0] 0010: K28.5 test bit sequence 0011: K28.7 test bit sequence 0100: K test for differential pair current 0101: J test for differential pair current 0110: D21.5 test bit sequence 0111: D30.3 test bit sequence 1000: Ten contiguous run of 3 test bit sequence 1001: Low transition density test bit sequence 1010: Half-rate/quarter-rate test bit sequence 1011: Low frequency spectral test bit sequence 1100: Simultaneous switching test bit sequence 1101: Reserved 1110: Reserved 1111: Reserved	
19:16	RW	0	**Select Lane for Loop Back Test** 0000: Loop back test on lane0 0001: Loop back test on lane1 .... 1111: Loop back test on lane15	
15:8	RW	00h	**Repeated Count of the Test Pattern** (as selected in RxF2[7:4]) 00~0Bh: Illegal.value 0Ch: Test pattern repeats 12 times 0Dh: Test pattern repeats 13 times ... FFh: Test pattern repeats 255 times	
7:1	—	0	**Reserved**	
0	RO	0	**Electrical PHY Test Error** 1 indicates that there is an error detected in the receiving side during the loop back test	

Offset Address: F7-F4h (D2F0)

PHY Test Symbol **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	—	0	**Reserved**
25:16	RW	00h	**Transmitted Symbol when EPHYTST_PEG (RxF0[31]) is set to 1** 00 when EPHYTST_PEG is 0
15:10	—	0	**Reserved**
9:0	RO	00h	**Received Symbol when EPHYTST_PEG (RxF0[31]) is set to 1** 00 when EPHYTST_PEG is 0

Device 2 Function 0 (D2F0) – PCI Express Root Port 0 Extended Space

Registers defined in the Extended Space can be accessed through PCI Express Enhanced Configuration Access Mechanism, which utilizes a flat memory-mapped address space to access the configuration registers. Please check PCI Express Specification for the detail information.

Advanced Error Reporting Capability (100-137h)

Offset Address: 103-100h (D2F0)

Advance Error Reporting Enhanced Capability Header **Default Value: 14010001h**

Bit	Attribute	Default	Description
31:20	RO	140h	Next Capability Offset
19:16	RO	1	Capability Version
15:0	RO	0001h	PCI Express Extended Capability ID

Offset Address: 107-104h (D2F0)

Uncorrectable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	–	0	Reserved
20	RW1CS	0	Unsupported Request Error Status (TL)
19	RW1CS	0	ECRC Error Status (TL)
18	RW1CS	0	Malformed TLP Status (TL)
17	RW1CS	0	Receiver Overflow Status (TL)
16	RW1CS	0	Unexpected Completion Status (TL)
15	RW1CS	0	Completer Abort Status (TL)
14	RW1CS	0	Completion Timeout Status (TL)
13	RW1CS	0	Flow Control Protocol Error Status (TL)
12	RW1CS	0	Poisoned TLP Status (TL)
11:5	–	0	Reserved
4	RW1CS	0	Data Link Protocol Error Status (DLL)
3:1	–	0	Reserved
0	RW1CS	0	Training Error Status (PHY)

Offset Address: 10B-108h (D2F0)

Uncorrectable Error Mask **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	–	0	Reserved
20	RWS	0	Unsupported Request Error Mask (TL)
19	RWS	0	ECRC Error Mask (TL)
18	RWS	0	Malformed TLP Mask (TL)
17	RWS	0	Receiver Overflow Mask (TL)
16	RWS	0	Unexpected Completion Mask (TL)
15	RWS	0	Completed Abort Mask (TL)
14	RWS	0	Completion Timeout Mask (TL)
13	RWS	0	Flow Control Protocol Error Mask (TL)
12	RWS	0	Poisoned TLP Mask (TL)
11:5	–	0	Reserved
4	RWS	0	Data Link Protocol Error Mask (DLL)
3:1	–	0	Reserved
0	RWS	0	Training Error Mask (PHY)

Offset Address: 10F-10Ch (D2F0)
Uncorrectable Error Severity **Default Value: 00060011h**

Bit	Attribute	Default	Description
31:21	—	0	Reserved
20	RWS	0	Unsupported Request Error Severity (TL)
19	RWS	0	ECRC Error Severity (TL)
18	RWS	1	Malformed TLP Severity (TL)
17	RWS	1	Receiver Overflow Error Severity (TL)
16	RWS	0	Unexpected Completion Error Severity (TL)
15	RWS	0	Completed Abort Error Severity (TL)
14	RWS	0	Completion Timeout Error Severity (TL)
13	RWS	0	Flow Control Protocol Error Severity (TL)
12	RWS	0	Poisoned TLP Severity (TL)
11:5	—	0	Reserved
4	RWS	1	Data Link Protocol Error Severity (DLL)
3:1	—	0	Reserved
0	RWS	1	Training Error Severity (PHY)

Offset Address: 113-110h (D2F0)
Correctable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:13	—	0	Reserved
12	RW1CS	0	Replay Timer Timeout Status (DLL)
11:9	—	0	Reserved
8	RW1CS	0	REPLAY_NUM Rollover Status (DLL)
7	RW1CS	0	Bad DLLP Status (DLL)
6	RW1CS	0	Bad TLP Status (DLL)
5:1	—	0	Reserved
0	RW1CS	0	Receiver Error Status (PHY)

Offset Address: 117-114h (D2F0)
Correctable Error Mask **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:13	—	0	Reserved
12	RWS	0	Replay Timer Timeout Mask (DLL)
11:9	—	0	Reserved
8	RWS	0	REPLAY_NUM Rollover Mask (DLL)
7	RWS	0	Bad DLLP Mask (DLL)
6	RWS	0	Bad TLP Mask (DLL)
5:1	—	0	Reserved
0	RWS	0	Receiver Error Mask (PHY)

Offset Address: 11B-118h (D2F0)
Advanced Error Capabilities and Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:9	—	0	Reserved
8	RWS	0	ECRC Check Enable (TL)
7	RO	0	ECRC Check Capable (TL)
6	RWS	0	ECRC Generation Enable (TL)
5	RO	0	ECRC Generation Capable (TL)
4:0	ROS	0	First Error Pointer (TL)

Offset Address: 12B-11Ch (D2F0)
Header Log (TL)

Register Offset Address	Attribute	Default	Description
11F - 11C	ROS	00h	**Header Log Register 1st DW**
123 - 120	ROS	00h	**Header Log Register 2nd DW**
127 - 124	ROS	00h	**Header Log Register 3rd DW**
12B – 128	ROS	00h	**Header Log Register 4th DW**

Offset Address: 12F-12Ch (D2F0)
Root Error Command **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:3	—	0	**Reserved**
2	RW	0	**Fatal Error Reporting Enable**
1	RW	0	**Non-Fatal Error Reporting Enable**
0	RW	0	**Correctable Error Reporting Enable**

Offset Address: 133-130h (D2F0)
Root Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	00h	**Advanced Error Interrupt Message Number (TL)**
26:7	—	0	**Reserved**
6	RW1CS	0	**Fatal Error Messages Received (TL)**
5	RW1CS	0	**Non-Fatal Error Messages Received (TL)**
4	RW1CS	0	**First Uncorrectable Fatal Error Message Received (TL)** Set to 1 when the first Uncorrectable Error Message received is for a Fatal Error
3	RW1CS	0	**Multiple ERR_FATAL/NONFATAL Received (TL)**
2	RW1CS	0	**ERR_FATAL/NONFATAL Received (TL)**
1	RW1CS	0	**Multiple ERR_COR Received (TL)**
0	RW1CS	0	**ERR_COR Received (TL)**

Offset Address: 137-134h (D2F0)
Error Source Identification **Default Value: 0000 0000h**

This register is updated regardless of the settings of Root Control register and the Root Error Command register.

Bit	Attribute	Default	Description
31:16	ROS	0000	**ERR_FATAL/NONFATAL Source Identification**
15:0	ROS	0000	**ERR_COR Source Identification**

Virtual Channel Capability (140-14Fh)

Virtual Channel Capability is defined for Egress direction of the device. For Root Port, since only VC0 is defined, there is no implementation of VC Arbitration Table and Port Arbitration Table.

Offset Address: 143-140h (D2F0)
Virtual Channel Enhanced Capability **Default Value: 00010002h**

Bit	Attribute	Default	Description
31:20	RO	000h	**Next Capability Offset**
19:16	RO	1h	**Capability Version**
15:0	RO	0002h	**PCI Express Extended Capability ID**

Offset Address: 147-144h (D2F0)
Port VC Capability I **Default Value: 0000 0000h**

Bit	Attribute	Default	Description	Mnemonic
31:12	–	0	**Reserved**	
11:10	RO	0	**Port Arbitration Table Entry Size** Reserved for root port	
9:8	RO	0	**Reference Clock** Reserved for root port	
7	–	0	**Reserved**	
6:4	RO	0	**Low Priority Extended VC Count**	
3	–	0	**Reserved**	
2:0	RO	0	**Extended VC Count**	VCAEVCC_PEG_[2:0]

Offset Address: 14B-148h (D2F0)
Port VC Capability II **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**VC Arbitration Table Offset** 00 since only VC0 is defined
23:8	–	0	**Reserved**
7:0	RO	00h	**VC Arbitration Capability**

Offset Address: 14D-14Ch (D2F0)
Port VC Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	–	0	**Reserved**
3:1	RW	0	**VC Arbitration Select**
0	RW	0	**Load VC Arbitration Table**

Offset Address: 14F-14Eh (D2F0)
Port VC Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:1	–	0	**Reserved**
0	RO	0	**VC Arbitration Table Status**

VC0 Resource (150-15Bh)

Offset Address: 153-150h (D2F0)
VC Resource Capability (VC0) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**Port Arbitration Table Offset (VC0)**
23	–	0	**Reserved**
22:16	RO	00h	**Maximum Time Slots (TL)** Indicates the maximum number of time slot (minus one) that the VC resource is capable of supporting when it is configured for time-based WRR port arbitration.
15	RO	0	**Reject Snoop Transactions**
14	RO	0	**Advanced Packet Switching**
13:8	–	0	**Reserved**
7:0	RO	00h	**Port Arbitration Capability**

Offset Address: 157-154h (D2F0)
VC Resource Control (VC0) **Default Value: 8000 00FFh**

Bit	Attribute	Default	Description
31	RO	1	**VC Enable** Hardwired to 1.
30:27	–	0	**Reserved**
26:24	RO	0	**VC ID** Hardwired to 0.for VC0.
23:20	–	0	**Reserved**
19:17	RW	0	**Port Arbitration Select**
16	RW	0	**Load Port Arbitration Table**
15:8	–	0	**Reserved**
7:0	RW Bit 0: RO	FFh	**TC/VC Mapping** This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC0 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit0 is hardwired to 1 (i.e. TC0 is always mapped to VC0).

Offset Address: 15B-158h (D2F0)
VC Resource Status (VC0) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	–	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)** This bit indicates whether the Virtual Channel negotiation is in Pending state (set/clear by hardware) 0: Negotiation is complete 1: Negotiation is on-going.
16	RO	0	**Port Arbitration Table Status** Reserved for root port
15:0	–	0	**Reserved**

VC1 Resource (15C-167h)

The following registers exist only when VCAEVCC_PEG_[0] (Rx144[0]) is programmed to 1. If VCAEVCC_PEG_[0] (Rx144[0]) = 0, all the following content will be read as 0.

Offset Address: 15F-15Ch (D2F0)
VC Resource Capability (VC1) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**Port Arbitration Table Offset (VC1)**
23	–	0	**Reserved**
22:16	RO	00h	**Maximum Time Slots (TL)** Indicates the maximum number of time slot (minus one) that the VC resource is capable of supporting when it is configured for time-based WRR port arbitration.
15	RO	0	**Reject Snoop Transactions**
14	RO	0	**Advanced Packet Switching**
13:8	–	0	**Reserved**
7:0	RO	00h	**Port Arbitration Capability**

Offset Address: 163-160h (D2F0)

VC Resource Control (VC1) **Default Value: 0010 0000h**

Bit	Attribute	Default	Description
31	RW	0	**VC Enable**
30:27	–	0	**Reserved**
26:24	RW	1	**VC ID.**
23:20	–	0	**Reserved**
19:17	RW	0	**Port Arbitration Select**
16	RW	0	**Load Port Arbitration Tablet**
15:8	–	0	**Reserved**
7:0	RW, Bit 0: RO	00h	**TC/VC Mapping** This field indicates the TCs that are mapped to VC1. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC1 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit0 is hardwired to 0 (i.e. TC0 is always mapped to VC0).

Offset Address: 167-164h (D2F0)

VC Resource Status (VC1) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	–	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)** This bit indicates whether the Virtual Channel negotiation is in Pending state (set/clear by hardware) 0: Negotiation is complete 1: Negotiation is on-going.
16	RO	00h	**Port Arbitration Table Status**
15:0	–	0	**Reserved**

Device 3 Function 0 (D3F0) – PCI Express Root Port 1 (PCI-to-PCI Virtual Bridge)

Device 3 Function 0 could be configured as a 4-Lane or 1-Lane PCI Express root port that is connected to the PCI bus through AD14 as the IDSEL. Registers listed in this section are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 3 and function number 0.

Header Registers (0-3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	**Vendor ID**
3 – 2h	RO	C238h	**Device ID**

Offset Address: 5-4h (D3F0)

Command Register **Default Value: 0000h**

Bit	Attribute	Default	Description	Mnemonic
15:11	—	0	**Reserved**	
10	RW	0	**Interrupt Disabled** Set when the device is prevented from generating INTx messages	
9	—	0	**Reserved**	
8	RW	0	**SERR# Enable** 0: Disable error report 1: Enable reporting of non-fatal and fatal errors	**RSERR_PE0**
7	—	0	**Reserved**	
6	RW	0	**Parity Error Response** 0: Ignore parity errors & continue 1: Take normal action on detected parity errors	**RPTYERR_PE0**
5:3	—	0	**Reserved**	
2	RW	0	**Bus Master Enable** 0: Disable 1: Enable Controls the ability to forward Memory and I/O Read/Write requests in the upstream direction. Disabling this bit disables MSI messages.	
1	RW	0	**Memory Space** 0: Ignore downstream memory transactions; memory cycles with address falling in the claimed range will be forwarded to the SB 1: Enable downstream memory cycle to this port if its address falling in the claimed range of this device.	
0	RW	0	**I/O Space** 0: Ignore downstream I/O transactions; I/O cycles with address falling in the claimed range will be forwarded to the SB. 1: Enable downstream I/O cycle to this port if its address falling in the claimed range of this device.	

Offset Address: 7-6h (D3F0)
Status Register **Default Value: 0010h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set whenever a poisoned TLP is received, regardless the state of Parity Error Enabled (see RPTYERR_PE0 Rx4[6] for details)
14	RW1C	0	**Signaled System Error** This bit is set when: 1. A device sends an ERR_FATAL or ERR_NONFATAL message 2. RSERR_PE0 (Rx4[8]) = 1
13	RW1C	0	**Received Master Abort** This bit is set when receiving a completion with Unsupported Request Completion Status
12	RW1C	0	**Received Target Abort** This bit is set when receiving a completion with Completer Abort Completion Status
11	RW1C	0	**Signaled Target Abort** This bit is set when completing a Request with Completer Abort Completion Status
10:9	–	0	**Reserved (Always 0)**
8	RW1C	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx4[6]) is set and either one of the following two conditions occurs: 1. Requestor receives a Completion marked poisoned 2. Requestor poisons a write Request
7:5	–	0	**Reserved**
4	RO	1	**Capabilities List** Indicates the presence of an extended capability list item. Always set to 1 for PCI Express device
3	RO	0	**Interrupt Status** Indicate an INTx message is pending internally (TL)
2:0	–	0	**Reserved**

Offset Address: 8h (D3F0)
Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Revision Code**

Offset Address: 0B-9h (D3F0)
Class Code **Default Value: 060400h**

Bit	Attribute	Default	Description
23:0	RO	060400h	**Class Code**

Offset Address: 0Ch (D3F0)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Cache Line Size – Reserved (No impact on functionality)**

Offset Address: 0Dh (D3F0)
Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Reserved (Hardwired to 0)**

Offset Address: 0Eh (D3F0)
Header Type **Default Value: 81h**

Bit	Attribute	Default	Description
7:0	RO	81h	**Header Type Code** A multiple function device.

Offset Address: 0Fh (D3F0)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**BIST Support**

Offset Address: 17-10h (D3F0)
Base Address Register **Default Value: 00h**

Bit	Attribute	Default	Description
63:0	RO	00h	**Base Address Register**

Offset Address: 18h (D3F0)
Primary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Primary Bus Number**

Offset Address: 19h (D3F0)
Secondary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Secondary Bus Number**

Offset Address: 1Ah (D3F0)
Subordinate Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Subordinate Bus Number**

Offset Address: 1Ch (D3F0)
I/O Base **Default Value: F0h**

Bit	Attribute	Default	Description
7:4	RW	1111	**I/O Base (AD[15:12] - inclusive)** This bridge will forward the cycles from primary side to PCI if the IO address AD[15:12] is between IO base and IO limit (Rx1D)
3:0	RO	0	**I/O Addressing Capability** 0 means IO addressing is 16-bit only.

Offset Address: 1Dh (D3F0)
I/O Limit **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:4	RW	0	**I/O Limit (AD[15:12] - inclusive)**	**RIOLM_PE0_[15:12]**
3:0	RO	0	**I/O Addressing Capability** 0 means IO addressing is 16-bit only.	

Offset Address: 1F-1Eh (D3F0)
Secondary Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set when secondary side receives a poisoned TLP regardless of RPTYERR_PE0 (Rx4[6]).
14	RW1C	0	**Received System Error** This bit is set when RSERR_PE0 (Rx4[8]) is 1 and a device sends an ERR_FATAL or ERR_NONFATAL message.
13	RW1C	0	**Received Master Abort**
12	RW1C	0	**Received Target Abort**
11	RW1C	0	**Signaled Target Abort**
10:9	–	0	**Reserved**
8	RW1C	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx4[6]) is set and either one of the following two conditions occurs: 1. Requestor receives a Completion marked poisoned. 2. Requestor poisons a write Request
7:0	–	0	**Reserved**

Offset Address: 21-20h (D3F0)
Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Memory Base (AD[31:20] – inclusive)** The address [19:0] is not decoded.
3:0	RO	0000	**Reserved** Always reads 0.

Offset Address: 23-22h (D3F0)
Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	000h	**Memory Limit (AD[31:20] – inclusive)** The address [19:0] is not decoded.
3:0	RO	0000	**Reserved** Always reads 0.

Offset Address: 25-24h (D3F0)
Prefetchable Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Prefetchable Memory Base AD[31:20]**
3:0	RO	0000	**Reserved** Always reads 0.

Offset Address: 27-26h (D3F0)
Prefetchable Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	000h	**Prefetchable Memory Limit AD[31:20]**
3:0	RO	0000	**Reserved** Always reads 0.

Offset Address: 2B-28h (D3F0)
Prefetchable Memory Upper Base **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	00h	**Reserved** Always reads 0.
3:0	RW	0000	**AD[35:32]** This chip supports up to 16G

Offset Address: 2F-2Ch (D3F0)
Prefetchable Memory Upper Limit **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	00h	**Reserved** Always reads 0.
3:0	RW	0000	**AD[35:32]** This chip supports up to16G

Offset Address: 31-30h (D3F0)
I/O Base Upper **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	00h	**I/O Base Upper 16 bits Address**

Offset Address: 33-32h (D3F0)
I/O Base Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	00h	**I/O Limit Upper 16 bits Address**

Offset Address: 34h (D3F0)
Capability Pointer **Default Value: 40h**

Contains an offset from the start of configuration space.

Bit	Attribute	Default	Description
7:0	RO	40h	**Capability Pointer** Always reads 40h. Capability Pointer link list: Rx34 → Rx40 → Rx68 → NULL

Offset Address: 3Ch (D3F0)
Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**INT Line (For Software Use Only)**

Offset Address: 3Dh (D3F0)
Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**INT Pin** 01: INTA

Offset Address: 3F-3Eh (D3F0)
Bridge Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:7	—	0	**Reserved**
6	RW	0	**Secondary Bus Reset** 0: No reset 1: Triggers a warm reset on the corresponding PCI Express Port
5	—	0	**Reserved**
4	RW	0	**Base VGA 16 bits Decode** 0: All VGA alias range will be forwarded 1: Only forward base VGA range (Alias range will not be forwarded)
3	RW	0	**VGA Compatible I/O and Memory Address Range** 0: Do not forward VGA compatible memory and I/O 1: Forward VGA compatible memory and I/O Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.
2	RW	0	**Block/Forward ISA I/O Cycles** 0: Forward all I/O cycles with address in the range defined by the I/O Base and I/O Limit 1: Do not forward ISA I/O that are in the top 768 bytes of each 1K byte block address range
1	RW	0	**SERR Enable** Controls the forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary 0: Disable 1: Enable
0	RW	0	**Parity Error Response Enable** 0: Ignore the response to poisoned TLPs 1: Enable the response to poisoned TLPs

PCI Express Capability Registers (40-63h)

Offset Address: 40-41h (D3F0)
PCI Express List **Default Value: 6810h**

Bit	Attribute	Default	Description
15:8	RO	68h	**Next Pointer**
7:0	RO	10h	**Capability ID**

Offset Address: 43-42h (D3F0)
PCI Express Capabilities **Default Value: 0041h**

Bit	Attribute	Default	Description
15:14	—	0	**Reserved**
13:9	RO	00h	**Interrupt Message Number**
8	RO	0	**Slot Implemented** This bit when set indicates that the PCI Express Link associated with this Port is connected to a slot (as compared to being connected to an integrated component or being disabled),
7:4	RO	0100	**Device / Port Type** 0100b: Root Port of PCI Express Root Complex
3:0	RO	1	**Capability Version**

Offset Address: 47-44h (D3F0)

Device Capabilities **Default Value: 0000 0nn1h**

Bit	Attribute	Default	Description
31:28	—	0	**Reserved**
27:26	RO	0	**Captured Slot Power Limit Scale**
25:18	RO	00h	**Captured Slot Power Limit Value**
17:15	—	000	**Reserved**
14	RO	0	**Power Indicator Present**
13	RO	0	**Attention Indicator Present**
12	RO	0	**Attention Button Present**
11:9	RO	111	**Endpoint L1 Acceptable Latency** 111b: more than 64us
8:6	RO	xxx	**Endpoint L0s Acceptable Latency**
5		0	**Extended Tag Field Supported** 0: 5-bit Tag field supported 1: 8-bit Tag field supported
4:3	RO	00	**Phantom Functions Supported** Reserved
2:0	RW	001	**Max Payload Size Supported** 001b: 32QW (256 bytes)

Offset Address: 49-48h (D3F0)

Device Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15	—	0	**Reserved**
14:12	RO	000	**Max Read Request Size** 000b: 128 bytes This field sets the maximum Read Request size for the device as a Requestor.
11	RW	0	**Enable No Snoop** If this bit is set to 1, the device is **permitted** to set the No Snoop bit in the Requestor Attributes of the transactions it initiate that do not require hardware enforced cache coherency.
10	RWS	0	**Auxiliary Power PM Enable** This bit when set enables device to draw AUX power independent of PME AUX power.
9	RO	0	**Phantom Functions Enable** Not supported.
8	RO	0	**Extended Tag Field Enable** Not supported.
7:5	RW	0	**Max Payload Size** Maximum TLP payload size.
4	RW	0	**Enable Relaxed Ordering** If this bit is set to 1, the device is **permitted** to set the Relaxed Ordering bit in the Requestor Attributes of the transactions it initiate that do not require strong write ordering.
3	RW	0	**Unsupported Request Reporting Enable**
2	RW	0	**Fatal Error Reporting Enable** For a Root Port, the reporting of Fatal errors is internal to the root. No external ERR_FATAL message is generated.
1	RW	0	**Non-Fatal Error Reporting Enable** For a Root Port, the reporting of Non-Fatal errors is internal to the root. No external ERR_NONFATAL message is generated.
0	RW	0	**Correctable Error Reporting Enable** For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_COR message is generated.

Offset Address: 4B-4Ah (D3F0)

Device Status **Default Value: 0010h**

Bit	Attribute	Default	Description
15:6	—	0	**Reserved**
5	RO	0	**Transactions Pending** This bit when set indicates that the Port has issued Non-Posted Requests on its own behalf (using the Port's own Requestor ID) which have not been completed.
4	RO	1	**AUX Power Detected**
3	RW1C	0	**Unsupported Request Detected**
2	RW1C	0	**Fatal Error Detected (TL)**
1	RW1C	0	**Non-Fatal Error Detected (TL)**
0	RW1C	0	**Correctable Error Detected (TL)**

Offset Address: 4F-4Ch (D3F0)

Link Capabilities **Default Value: 0100 0C41h**

Bit	Attribute	Default	Description
31:24	RO	01h	**Port Number** This field indicates the PCI Express Port number for the given PCI Express Link.
23:18	–	0	**Reserved**
17:15	RO	0	**L1 Exit Latency** 000: less than 1us. The value reported indicates the length of time this Port requires to complete transition from L1 to L0.
14:12	RO	0	**L0s Exit Latency** 000: less than 64ns. The value reported indicates the length of time this Port requires to complete transition from L0s to L0.
11:10	RO	11	**Active State Link PM (ASPM) Support** 11b: L0s and L1 supported. This field indicates the level of ASPM supported on the PCI Express Link.
9:4	RO	04h	**Maximum Link Width** 04h: x4 Link width
3:0	RO	1	**Maximum Link Speed** 0001b: 2.5Gb/s Link speed

Offset Address: 51-50h (D3F0)

Link Control **Default Value: 0000h**

Bit	Attribute	Default	Description	Mnemonic
15:8	–	00	**Reserved**	
7	RW	0	**Extended Synch** 0: FCU Timer limit is 30us 1: FCU Timer limit is 120us	LCES_PE0
6	RW	0	**Common Clock Configuration** 0: Indicates that this Port and the component on the opposite end of the Link are operating with asynchronous reference clock. 1: Indicates that this Port and the component on the opposite end of the Link are operating with a distributed common reference clock.	
5	RW	0	**Retrain Link** A write of 1 to this bit initiates Link retrained by directing the Physical Layer LTSSM to the Recovery state.	
4	RW	0	**Link Disable** This bit disables the Link when set to 1.	
3	RO	0	**Read Completion Boundary** 0: 64 byte	
2	–	0	**Reserved**	
1:0	RW	00	**Link Active State PM (ASPM) Control** 00b: Disabled 01b: L0s Entry Enabled 10b: L1 Entry Enabled 11b: L0s and L1 Entry Enabled	

Offset Address: 53-52h (D3F0)

Link Status **Default Value: 0nn1h**

Bit	Attribute	Default	Description
15:13	–	0	**Reserved**
12	RO	0	**Slot Clock Configuration** 0: Use an independent clock irrespective of the presence of a reference on the connector. 1: Use the same physical reference clock that the platform provides on the connector.
11	RO	0	**Link Training** This bit indicated that Link training is in progress (Physical Layer LTSSM is in Configuration or Recovery state) or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit once Link training is complete.
10	RO	0	**Training Error** Set when a Link training error occurred. Cleared by hardware upon successfully training of the Link to the L0 Link state.
9:4	RO	xxxxxx	**Negotiated Link Width** 000001: x1 000010: x2 000100: x4 001000: x8 010000: x16
3:0	RO	0001	**Link Speed** 0001: 2.5Gb/s negotiated Link speed.

Offset Address: 57-54h (D3F0)

Slot Capabilities **Default Value: 0000 0060h**

Bit	Attribute	Default	Description
31:19	RO	00h	**Physical Slot Number** Physical slot number attached to the Port.
18:17	–	0	**Reserved**
16:15	RO	0	**Slot Power Limit Scale** Write to the field causes the Port to send the Set_Slot_Power_Limit message.
14:7	RO	00h	**Slot Power Limit Value** Write to the field causes the Port to send the Set_Slot_Power_Limit message.
6	RO	1	**Hot-plug Capable**
5	RO	1	**Hot-plug Surprise**
4	RO	0	**Power Indicator Present**
3	RO	0	**Attention Indicator Present**
2	RO	0	**MRL Sensor Present**
1	RO	0	**Power Controller Present**
0	RO	0	**Attention Button Present**

Offset Address: 59-58h (D3F0)

Slot Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	–	0	**Reserved**
10	RO	0	**Power Controller Control** 0: Power On 1: Power Off
9:8	RW	0	**Power Indicator Control** 00: Reserved 01: On 10: Blink 11: Off Writes to this field cause the Port to send the appropriate POWER_INDICATOR_* Message.
7:6	RW	0	**Attention Indicator Control** 00: Reserved 01: On 10: Blink 11: Off Writes to this field cause the Port to send the appropriate ATTENTION_INDICATOR_* Message.
5	RW	0	**Hot-Plug Interrupt Enable** This bit when set enables generation of Hot-Plug interrupt on enabled Hot-Plug events.
4	RW	0	**Command Completed Interrupt Enable** This bit when set enables the generation of Hot-Plug interrupt when a command is completed by the Hot-Plug controller.
3	RW	0	**Presence Detect Changed Enable** This bit when set enables the generation of Hot-Plug interrupt or Wakeup event on a presence detect changed event.
2	RO	0	**MRL Sensor Changed Enable**
1	RO	0	**Power Fault Detected Enable**
0	RW	0	**Attention Button Pressed Enable** This bit when set enables the generation of Hot-Plug interrupt or Wakeup event on an Attention Button pressed event.

Offset Address: 5A-5Bh (D3F0)

Slot Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:7	–	0	**Reserved**
6	RO	0	**Presence Detect State** 0: Slot empty 1: Card present in slot
5	RO	0	**MRL Sensor State**
4	RW1C	0	**Command Completed**
3	RW1C	0	**Presence Detect Changed**
2	RO	0	**MRL Sensor Changed**
1	RO	0	**Power Fault Detected**
0	RW1C	0	**Attention Button Pressed**

Offset Address: 5D-5Ch (D3F0)

Root Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	—	0	**Reserved**
3	RW	0	**PME Interrupt Enable** 0: Disable 1: Enable interrupt generation upon receipt of a PME message as reflected in the PME status register bit. A PME interrupt is also generated if the PME status register bit is set when this bit is set from a cleared state.
2	RW	0	**System Error on Fatal Error Enable** 0: Disable 1: Enable generation of a System Error if a Fatal Error (ERR_FATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
1	RW	0	**System Error on Non-Fatal Error Enable** 0: Disable 1: Enable generation of a System Error if a Non-Fatal Error (ERR_NONFATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
0	RW	0	**System Error on Correctable Error Enable** 0: Disable 1: Enable generation of a System Error if a Correctable Error (ERR_COR) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.

Offset Address: 63-60h (D3F0)

Root Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	—	0	**Reserved**
17	RO	0	**PME Pending** 0: No pending PME 1: Indicates that another PME is pending when the PME Status (bit 16) is set.
16	RW1C	0	**PME Status** Indicates that the PME was asserted by the Requestor ID indicated in PME Requestor ID (bit[15:0]).
15:0	RO	00h	**PME Requestor ID** The Requestor ID of the last PME Requestor.

PCI Power Management Capability Structure Registers (68-6Fh)

Offset Address: 6B-68h (D3F0)

Power Management Capabilities **Default Value: C802 7001h**

Bit	Attribute	Default	Description
31:27	RW	11001	**PME Support** Bit 31, 30 and 27 are set to 1b (PME Message will be forwarded).
26	RW	0	**D2 Support**
25	RW	0	**D1 Support**
24:22	RO	0	**AUX Current**
21	RW	1	**Device Specific Initialization**
20:19	—	0	**Reserved**
18:16	RO	010	**Version**
15:8	RO	70h	**Next Capability Pointer**
7:0	RO	01h	**Capability ID**

Offset Address: 6F-6Ch (D3F0)
Power Management Status/Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**Power Management Data**
23:16	RO	—	**Reserved**
15	RW1CS	0	**PME Status** This bit's setting is not modified by hot, warm, or cold reset.
14:13	RO	0	**Data Scale**
12:9	RW	0	**Data Select**
8	RWS	0	**PME Enable** This bit's setting is not modified by hot, warm, or cold reset.
7:2	RO	0	**Reserved**
1:0	RW	0	**Power State**

PCI Message Signal Interrupt (MSI) Capability Structure Registers (70-87h)

Offset Address: 73-70h (D3F0)
MSI Capability Support **Default Value: 0180 0005h**

Bit	Attribute	Default	Description
31:25	—	0	**Reserved**
24	RO	1	**This MSI capability supports pre-vector masking capability**
23	RO	1	**This MSI capability supports 64 bit message address only**
22:20	RW	000	**Multiple Message Enable** 000: 1message allocated 001: 2 message allocated 010: 4 message allocated 011: 8 message allocated 100: 16 message allocated 101: 32 message allocated 11x: Reserved
19:17	RO	000	**Multiple Message Capable** 000: 1message requested 001: 2 message requested 010: 4 message allocated 011: 8 message allocated 100: 16 message requested 101: 32 message requested 11x: Reserved
16	RW	0	**MSI Enable** 0: This Port is prohibited from using MSI to request service 1: This Port is permitted to use MSI to request service.
15:8	RO	00h	**Next Capability Pointer**
7:0	RO	05h	**Capability ID**

Offset Address: 77-74h (D3F0)
System-Specified Message Address - Low **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	00h	**System-Specified Message Address Bit [31:2]**
1:0	RO	00	**System-Specified Message Address Bit [1:0]** These bits will always read as 0

Offset Address: 7B-78h (D3F0)
System-Specified Message Address - High **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	00h	**System-Specified Message Address Bit [63:36]** These bits will always read as 0 since this chip supports address up to A35.
3:0	RW	0	**System-Specified Message Address Bit [35:32]**

Offset Address: 7D-7Ch (D3F0)
Message Data **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Message Data** The message data is to be put on data [15:0] of MSI cycles

Offset Address: 83-80h (D3F0)
Message Mask Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	00h	**Mask Bit**
0	RW	0	**Mask Bit for Message 0**

Offset Address: 87-84h (D3F0)
Message Pending Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	00h	**Pending Bit**
0	RO	0	**Pending Bit for Message 0**

PCI Express Transaction Layer Registers (A0-A4h)

Offset Address: A0h (D3F0)
Downstream Control I **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Cycles Have Traffic Class TC1** 0: Disabled 1: Enabled.
6	RW	0	**Downstream Cycles Have Attribute "No Snoop" Set** 0: Disabled 1: Enabled.
5	RW	0	**Downstream Cycles Have Attribute "Relaxed Ordering" Set** 0: Disabled 1: Enabled.
4	RW	0	**Downstream Lock Cycle Support** 0: Disabled 1: Enabled.
3	RW	0	**Downstream Arbitration Scheme** 0: Fixed priority: VC1 CPL > VC0 CPL > Down Stream Command 1: Round Robin arbitration priority between VC1 CPL, VC0 CPL and Down Stream Command
2	RW	0	**Downstream Post-Write Allowed to Pass IOW** 0: Not allowed. 1: Allowed.
1	RW	0	**Downstream Post-Write Allowed to Pass Read** 0: Not allowed. 1: Allowed.
0	RW	1	**Downstream Pipeline** 0: Disabled 1: Enabled.

Offset Address: A1h (D3F0)
Downstream Control II **Default Value: 04h**

Bit	Attribute	Default	Description
7	RW1C	0	**Downstream Configuration Completion Status** 0: Normal completion. 1: At least one configuration request ended with a CRS (Configuration Request Retry Status) completion.
6:4	—	0	**Reserved**
3	—	0	**Reserved**
2:0	RW	100	**C2P Read Completion Timeout Timer** 000: Reserved 001: 1ms 010: Reserved 011: 10ms (Spec. lower bound) 100: 30ms 101: 50ms (Spec. higher bound) 110: 100ms 111: Reserved

Offset Address: A4h (D3F0)

Upstream Control **Default Value: 01h**

Bit	Attribute	Default	Description
7	RW	0	**Upstream Address A35~A31 Forced to 0** 0: Disabled. 1: Enabled for system testing or loop back mode test. The upcoming data may be checked in the system memory
6	—	0	**Reserved**
5	RW	0	**Upstream Checking Malformed TLP through "Byte Enable Rule" And "Over 4K Boundary Rule"** 0: Disabled. 1: Enabled.
4	RW	1	**Downstream Read Wait Till The Upstream Write Data Flushed** 0: Disabled. 1: Enabled.
3:2	—	0	**Reserved**
1	RW	0	**Allows TL Map Non-Snoop Upstream Request to VC1 Request Queue Output to the Central Traffic Controller When VC1 Do Not Exist in the Capability Header** (software has to program VCAEVCC_PE0_[0] (Rx144[0] = 0)) 0: Disabled. 1: Enabled (Note that when this bit is 1, bit 0 has to be 0).
0	RW	0	**Disable Virtual Channel 1 Support (i.e. VC1's data FIFO is used by VC0)** 0: No, data FIFO of VC1 is used by VC1 1: Disable VC1, data FIFO of VC1 is reallocated to VC0, which doubles the size of VC0 data FIFO.

PCI Express Data Link Layer Registers (B0-B6h)

Offset Address: B0h (D3F0)

Ack/Nak Latency Timer Limit **Default Value: 3Bh**

Bit	Attribute	Default	Description	Mnemonic
7:0	RW	3Bh	**Timer Limit for Ack/Nak Latency Timer and Update FC Latency Timer (in unit of 250MHz)** 00: 4 x 1 Clocks 01: 4 x 2 Clocks 02: 4 x 3 Clocks. 0n: 4 x (n+1) Clocks FF: 4 x 256 Clocks.	RACKLTLM_PE0_[7:0]

Offset Address: B1h (D3F0)

Replay Timer Limit **Default Value: 59h**

Bit	Attribute	Default	Description
7:0	RW	59h	**Replay Timer Limit (In unit of 250MHz)** 00: 8 x 1 Clocks 01: 8 x 2 Clocks 02: 8 x 3 Clocks 0n: 8 x (n+1) Clocks FF: 8 x 256 Clocks.

Offset Address: B2h (D3F0)
FCU Control and Status **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW1C	0	**FCU Timeout Status** 1 means the FCU timeout has occurred
6	RW	1	**FCU Receive Timer Enable Control** 0: Disable the timeout mechanism 1: Enable the timeout mechanism
5	RW	0	**FCU Receive Timer Limit** 0: Timeout limit of 200us 1: Timeout limit of 300us
4	RW	0	**FCU Receive Timer Reset Control** 0: Timer reset by FCI/FCU only 1: Timer reset by any received DLLPs
3:0	–	0	**Reserved**

Offset Address: B3h (D3F0)
Replay Timer Control **Default Value: 80h**

Bit	Attribute	Default	Description
7:6	RW	10	**Replay Timer Control while Rewind** (resend those DLLPs which do not have corresponding ACK/NAK received) 00: Hold Replay Timer during rewind. 01: During rewind, if ACK/NAK comes in, reset and hold the Replay Timer. 10: During rewind, reset and hold the Replay Timer as long as the Retry Buffer is empty. 11: Reserved.
5:3	–	0	**Reserved**
2:0	RW	000	**Count of Replay Timer Expired During RXL0s** (Receiving Physical in L0s state) **Before Resend the TLP** **When LCES_PE0 (Rx50[7]) is set to 0:** 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 1 x Replay timer expired 010: Resend the TLP after 2 x Replay timer expired 011: Resend the TLP after 4 x Replay timer expired 100: Resend the TLP after 8 x Replay timer expired 101: Resend the TLP after 16 x Replay timer expired 110: Resend the TLP after 32 x Replay timer expired 111: Resend the TLP after 64 x Replay timer expired **When LCES_PE0 (RX50[7]) is set to 1:** 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 16 x Replay timer expired 010: Resend the TLP after 32 x Replay timer expired 011: Resend the TLP after 64 x Replay timer expired 100: Resend the TLP after 128 x Replay timer expired 101: Resend the TLP after 256 x Replay timer expired 110: Resend the TLP after 512 x Replay timer expired 111: Resend the TLP after 1024 x Replay timer expired

Offset Address: B4h (D3F0)
Arbitration Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	–	0	**Reserved**
3	RW	0	**TLP vs. Flow Control Initialization for VC0 in Arbitration Priority** 0: TLP is not allowed to pass FCI2 for VC0 1: TLP is allowed to pass FCI2 for VC0
2:0	RW	000	**Data Link TX Packets Arbitration Scheme** 000: Round Robin 001: Reserved. 010: Strict priority: TLP > ACK/NAK > FCU 011: Strict priority: TLP > FCU > ACK/NAK 100: Strict priority: ACK/NAK > TLP > FCU 101: Strict priority: ACK/NAK > FCU > TLP 110: Strict priority: FCU > TLP > ACK/NAK 111: Strict priority: FCU > ACK/NAK > TLP

Offset Address: B5h (D3F0)

FCU Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	**Reserved**
6	RW	0	**FCU (Flow Control Unit) Timer Control** 0: Update flow control credit when either Transaction Layer requested packets being sent or when FCU timer expired 1: Update flow control credit only when FCU timer expired
5:4	RW	00	**ACK DLLP Collapse Method** 00: Send ACK when the latency timer RACKLTLM (RxB0) expired. 01: Send ACK every 4 correct TLP has been received 10: Send ACK every 8 correct TLP has been received 11: Send ACK every 16 correct TLP has been received
3:2	—	0	**Reserved**
1	RW	0	**FCI (Flow Control Initialization) Process End Condition** 0: Complete FCI process when TLP/FCU has been received 1: Do not complete FCI process even when TLP/FCU has been received
0	RW	0	**VC1 FCI DLLP Transmission Scheme** 0: Transmit FCI DLLP only when FCI timer expired 1: Transmit FCI DLLP continuously as long as the FCI process is not finished

Offset Address: B6h (D3F0)

Transaction / Link Layer Checking Control **Default Value: 03h**

Bit	Attribute	Default	Description
7:5	—	0	**Reserved**
4	RW	0	**VC Negotiate Pending Control for VC1** 0: Assert VC negotiation pending after VC1 is enabled 1: Assert VC negotiation pending after RESET is de-asserted
3	—	0	**Reserved**
2	RW	0	**ECRC Checking Control for the Case of TD equals to1 but no ECRC field in TLP** 0: Ignore the error 1: Report error to Transaction Layer, which will mark the TLP as a Malformed TLP
1	RW	1	**Length Malform Report Control** 0: Do not report length malform to Transaction Layer 1: Report length malform to Transaction Layer
0	RW	1	**LCRC Checking Control** 0: Do not check LCRC 1: Check LCRC

PCI Express Physical Layer Registers (C0-C7h)

Offset Address: C3-C0h (D3F0)

PHY Control **Default Value: 0000 0003h**

Bit	Attribute	Default	Description	Mnemonic
31:16	–	0	**Reserved**	
15:14	RW	00	**Auto/Manual Configuration for Root Port 1 and 2** 00: Auto negotiation 01: 4x1 negotiation 10: Reserved 11: 1x4 negotiation	
13	–	0	**Reserved**	
12:8	RW	00	**PHY Lane Configuration Setting** 00100: x4 with normal connection for Root Port 1 11011: x4 with reverse connection for Root Port 1 00011: Reserved 11111: x1 with normal connection for Root Port 1, 2, 3 and 4 10101: force into L0S state, for testing measurement used only 00000: Use PHY negotiation Other values are not allowed	
7	RW	0	**Quick Timeout Counter Setting** When set to 1, the following timeout will be shorter: TIMEOUT_2MS → TIMEOUT_4US TIMEOUT_12MS → TIMEOUT_24US TIMEOUT_24MS → TIMEOUT_48US TIMEOUT_48MS → TIMEOUT_96US TIMEOUT_1024TS → TIMEOUT_32TS Receiver Detection: 15x1024ns → 1x1024ns	
6	RW	0	**Disable Data Scrambling / Descrambling** 0: Enable data scrambling 1: Disable data scrambling	
5:3	RW	000	**Loopback Mode Selection** 000 : No loop back 001: PHYLS loopback from TX end to RX end 010: PHYES loopback from TX end to RX end 011: Reserved 100: Reserved 101: PHYLS loopback from RX end to TX end 110: PHYES loopback from RX end to TX end 111: Reserved	**LPBK_SEL_PE0_[2:0]**
2:0	RW	011	**COMMA Detection Window** 0, 1: Illegal values Others: delay number of T to determine correct lane-to-lane deskew value	

Offset Address: C7-C4h (D3F0)

Elastic Buffer Base Registers for Lane 0 - 3 **Default Value: 0000 4444h**

Bit	Attribute	Default	Description	Mnemonic
31:15	–	0	**Reserved**	
14:12	RW	4	**Elastic Buffer Base Register for Lane 3** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations	
11	–	0	**Reserved**	
10:8	RW	4	**Elastic Buffer Base Register for Lane 2** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations	
7	–	0	**Reserved**	
6:4	RW	4	**Elastic Buffer Base Register for Lane 1** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations	
3	–	0	**Reserved**	
2:0	RW	4	**Elastic Buffer Base Register for Lane 0** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations	**EB_BASE_00_PE0_[2:0]**

PCI Express Power Management Module Registers (D0-D3h)

Offset Address: D3-D0h (D3F0)

PMC Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RW	00h	**Idle Period to Enter ASL1** Minimum time period is 128ns 00: 128ns 01: 2x128ns 02: 3x128ns ... FF: 256x128ns
23:16	RW	00h	**Idle Period to Enter L0s** Minimum time period is 128ns (L0SLIM_PE0 = 00) 00: 128ns 01: 2x128ns 02: 3x128ns ... FF: 256x128ns
15	RW1C	0	**Error Status Report** This bit is set when device cannot have electrical idle after the waiting period programmed at RxD1[6:4] expired.
14	—	0	**Reserved**
13:12	RW	0	**Electrical Idle Waiting Period before Move to L1 State** (after issue ACK to the L1 request from the device). 00: Always wait for electrical idle 01: Wait 32 clock 10: Wait 64 clock 11: Reserved
11:10	—	0	**Reserved**
9:8	RW	0	**Downstream Cycles Triggered C2P Cycles, Period of Staying at L0 Before Returned to L1 for PHY** (when PMU is in non-D0 state) 00: immediately 01: 1 cfgW or message + delay10T 10: 1 32QW +1cfgW or message+ delay10T 11: 2 32QW +1 cfgW or message +delay10T
7:2	—	0	**Reserved**
1	RW	0	**Link Loopback** 0: Normal operation 1: Direct device to enter Loopback mode, receiving data in the device will be sent to the transmit side
0	RW	0	**LTSSM State During Link Reconfigure Link Width** 0: When reconfigure link width, LTSSM must be in Detect state 1: When reconfigure link width, LTSSM can be in Configuration state

PCI Express Message Controller Related Registers (D8h)

Offset Address: D8h (D3F0)

PMC Express Message Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Excessive Errors Occurred But Not Reported in The MSGC** 0: Normal operation. 1: There are errors not reported to the system
6:0	—	0	**Reserved**

PCI Express Electrical PHY Registers (E1-E4h)

Offset Address: E1h (D3F0)
PHYES Module Related Control **Default Value: 08h**

Bit	Attribute	Default	Description
7:6	–	0	**Reserved**
5	RW	0	**Bypass PHYES Receiver Detection Function** 0: Not Bypass 1: Bypass receiver detection
4	RW	0	**Receiving Polarity Change Control** 0: Have the same polarity on the loop-back/received data 1: Have reverse polarity on the loop-back/received data
3:2	RW	10	**Squelch Window Select (64~175mv)**
1	RW	0	**Electrical Idle State Exit Condition: Number of Non Idle Signal Detected Before Exit Idle State** 0: 2 bits. 1: 10 bits.
0	RW	0	**Electrical Idle State Enter Condition: Number of Idle Signal Detected Before Enter Idle State** 0: 2 bits 1: 10 bits

Offset Address: E2h (D3F0)
PHYES Module Control – Rx/Tx I **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	–	0	**Reserved**
5	RW	0	**PHYES Clock Buffer Power Down on Lane 0-3** 0: All enable. 1: Power down
4	RW	0	**Lane 2-3 Clock Buffer Power Down** 0: All enable 1: Lane 2-3 power down
3:2	RW	00	**Receiver Input Rise Delay (duty cycle adjustment)** 00: 0 ps 01: 10 ps 10: 40 ps 11: 80 ps
1:0	RW	00	**Receiver Input Fall Delay (duty cycle adjustment)** 00: 0 ps 01: 10 ps 10: 40 ps 11: 80 ps

Offset Address: E3h (D3F0)
PHYES Module Control – Rx/Tx II **Default Value: 02h**

Bit	Attribute	Default	Description
7	RW	0	**PCI-E Pads Driving Control** 0: Autocomp 1: Manual setting through bits [2:0]
6:4	–	0	**Reserved**
3	RW	0	**CDR Filter Depth** 0: Filter depth = 3 1: Filter depth = 2
2:0	RW	2	**Lane 0 –3 Termination Resistance Selection** Resistance Range: 62Ω (000b) ~ 43Ω (111b) Default: 50Ω (010b)

Offset Address: E4h (D3F0)
PHYES Module Control – Rx/Tx III **Default Value: 44h**

Bit	Attribute	Default	Description
7:4	RW	4h	**Pre/De-Emphasis Level Selection**
3:0	RW	4h	**Driver Current Source Selection**

PCI Express Electrical PHY Test Registers (F0-F7h)

Offset Address: F3-F0h (D3F0)

PHY Test **Default Value: 0600 0000h**

Bit	Attribute	Default	Description	Mnemonic
31	RW	0	**Electrical PHY Test Mode Enable** Program this bit to 1 to start Electrical PHY test	
30:28	—	0	**Reserved**	
27:24	RW	6	**Test Pattern Check Length** Number of T when the receiving side starts to check transmitted and received patterns Suggested Value Settings: (Lane 0 for example) LPBK_SEL_PE0_[2:0] (RxC0[5:3]) = 001b: EB_BASE_00_PE0_[2:0] (RxC4[2:0]) + 2 LPBK_SEL_PE0_[2:0] (RxC0[5:3]) = 010b: EB_BASE_00_PE0_[2:0] (RxC4[2:0]) + 2 + (Loopback Path Latency/4ns) + 1	
23:20	RW	0	**Select Test Pattern** 0000: Reserved 0001: User define, use TPHYTXD_PE0_[9:0] (RxF4[25:16]) 0010: K28.5 test bit sequence 0011: K28.7 test bit sequence 0100: K test for differential pair current 0101: J test for differential pair current 0110: D21.5 test bit sequence 0111: D30.3 test bit sequence 1000: Ten contiguous run of 3 test bit sequence 1001: Low transition density test bit sequence 1010: Half-rate/quarter-rate test bit sequence 1011: Low frequency spectral test bit sequence 1100: Simultaneous switching test bit sequence 1101: Reserved 1110: Reserved 1111: Reserved	**MODESEL_PE0_[3:0]**
19:18	—	0	**Reserved**	
17:16	RW	0	**Select Lane for Loop Back Test** 00: Loop back test on lane0 01: Loop back test on lane1 10: Loop back test on lane2 11: Loop back test on lane3	
15:8	RW	00	**Repeated Count of the Test Pattern** (as selected in RxF0[23:20]) 00~0Bh: Illegal.value 0Ch: Test pattern repeats 12 times 0Dh: Test pattern repeats 13 times ... FFh: Test pattern repeats 255 times	
7:1	—	0	**Reserved**	
0	RO	0	**Electrical PHY Test Error** 1 indicates that there is an error detected in the receiving side during the loop back test	

Offset Address: F7-F4h (D3F0)

PHY Test Symbol **Default Value: 0000h**

Bit	Attribute	Default	Description	Mnemonic
31:26	—	0	**Reserved**	
25:16	RW	00h	**Transmitted Symbol when EPHYTST_PE0 (RxF0[31]) is set to 1** 00 when EPHYTST_PE0 is 0	**TPHYTXD_PE0_[9:0]**
15:10	—	0	**Reserved**	
9:0	RO	00h	**Received Symbol when EPHYTST_PE0 (RxF0[31]) is set to 1** 00 when EPHYTST_PE0 is 0	

Device 3 Function 0 (D3F0) – PCI Express Root Port 1 Extended Space

Registers defined in the Extended Space can be accessed through PCI Express Enhanced Configuration Access Mechanism, which utilizes a flat memory-mapped address space to access the configuration registers. Please check PCI Express Specification for the detail information.

Advanced Error Reporting Capability (100-137h)

Offset Address: 103-100h (D3F0)

Advanced Error Reporting Enhanced Capability Header **Default Value: 1401 0001h**

Bit	Attribute	Default	Description
31:20	RO	140h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	0001h	PCI Express Extended Capability ID

Offset Address: 107-104h (D3F0)

Uncorrectable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	–	0	Reserved
20	RW1CS	0	Unsupported Request Error Status (TL)
19	RW1CS	0	ECRC Error Status (TL)
18	RW1CS	0	Malformed TLP Status (TL)
17	RW1CS	0	Receiver Overflow Status (TL)
16	RW1CS	0	Unexpected Completion Status (TL)
15	RW1CS	0	Completer Abort Status (TL)
14	RW1CS	0	Completion Timeout Status (TL)
13	RW1CS	0	Flow Control Protocol Error Status (TL)
12	RW1CS	0	Poisoned TLP Status (TL)
11:5	–	0	Reserved
4	RW1CS	0	Data Link Protocol Error Status (DLL)
3:1	–	0	Reserved
0	RW1CS	0	Training Error Status (PHY)

Offset Address: 10B-108h (D3F0)

Uncorrectable Error Mask **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	–	0	Reserved
20	RWS	0	Unsupported Request Error Mask (TL)
19	RWS	0	ECRC Error Mask (TL)
18	RWS	0	Malformed TLP Mask (TL)
17	RWS	0	Receiver Overflow Mask (TL)
16	RWS	0	Unexpected Completion Mask (TL)
15	RWS	0	Completed Abort Mask (TL)
14	RWS	0	Completion Timeout Mask (TL)
13	RWS	0	Flow Control Protocol Error Mask (TL)
12	RWS	0	Poisoned TLP Mask (TL)
11:5	–	0	Reserved
4	RWS	0	Data Link Protocol Error Mask (DLL)
3:1	–	0	Reserved
0	RWS	0	Training Error Mask (PHY)

Offset Address: 10F-10Ch (D3F0)
Uncorrectable Error Severity **Default Value: 00060011h**

Bit	Attribute	Default	Description
31:21	—	0	Reserved
20	RWS	0	Unsupported Request Error Severity (TL)
19	RWS	0	ECRC Error Severity (TL)
18	RWS	1	Malformed TLP Severity (TL)
17	RWS	1	Receiver Overflow Error Severity (TL)
16	RWS	0	Unexpected Completion Error Severity (TL)
15	RWS	0	Completed Abort Error Severity (TL)
14	RWS	0	Completion Timeout Error Severity (TL)
13	RWS	0	Flow Control Protocol Error Severity (TL)
12	RWS	0	Poisoned TLP Severity (TL)
11:5	—	0	Reserved
4	RWS	1	Data Link Protocol Error Severity (DLL)
3:1	—	0	Reserved
0	RWS	1	Training Error Severity (PHY)

Offset Address: 113-110h (D3F0)
Correctable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:13	—	0	Reserved
12	RW1CS	0	Replay Timer Timeout Status (DLL)
11:9	—	0	Reserved
8	RW1CS	0	REPLAY_NUM Rollover Status (DLL)
7	RW1CS	0	Bad DLLP Status (DLL)
6	RW1CS	0	Bad TLP Status (DLL)
5:1	—	0	Reserved
0	RW1CS	0	Receiver Error Status (PHY)

Offset Address: 117-114h (D3F0)
Correctable Error Mask **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:13	—	0	Reserved
12	RWS	0	Replay Timer Timeout Mask (DLL)
11:9	—	0	Reserved
8	RWS	0	REPLAY_NUM Rollover Mask (DLL)
7	RWS	0	Bad DLLP Mask (DLL)
6	RWS	0	Bad TLP Mask (DLL)
5:1	—	0	Reserved
0	RWS	0	Receiver Error Mask (PHY)

Offset Address: 11B-118h (D3F0)
Advanced Error Capabilities and Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:9	—	0	Reserved
8	RWS	0	ECRC Check Enable (TL)
7	RO		ECRC Check Capable (TL)
6	RWS	0	ECRC Generation Enable (TL)
5	RO		ECRC Generation Capable (TL)
4:0	ROS		First Error Pointer (TL)

Offset Address: 12B-11Ch (D3F0)
Header Log (TL)

Register Offset Address	Attribute	Default	Description
11F - 11C	ROS	00h	**Header Log Register 1st DW**
123 - 120	ROS	00h	**Header Log Register 2nd DW**
127 - 124	ROS	00h	**Header Log Register 3rd DW**
12B – 128	ROS	00h	**Header Log Register 4th DW**

Offset Address: 12F-12Ch (D3F0)
Root Error Command **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:3	—	0	**Reserved**
2	RW	0	**Fatal Error Reporting Enable**
1	RW	0	**Non-Fatal Error Reporting Enable**
0	RW	0	**Correctable Error Reporting Enable**

Offset Address: 133-130Ch (D3F0)
Root Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	00h	**Advanced Error Interrupt Message Number (TL)**
26:7	—	0	**Reserved**
6	RW1CS	0	**Fatal Error Messages Received (TL)**
5	RW1CS	0	**Non-Fatal Error Messages Received (TL)**
4	RW1CS	0	**First Uncorrectable Fatal Error Message Received (TL)** Set to 1 when the first Uncorrectable Error Message received is for a Fatal Error
3	RW1CS	0	**Multiple ERR_FATAL/NONFATAL Received (TL)**
2	RW1CS	0	**ERR_FATAL/NONFATAL Received (TL)**
1	RW1CS	0	**Multiple ERR_COR Received (TL)**
0	RW1CS	0	**ERR_COR Received (TL)**

Offset Address: 137-134Ch (D3F0)
Error Source Identification **Default Value: 0000 0000h**

This register is updated regardless of the settings of Root Control register and the Root Error Command register.

Bit	Attribute	Default	Description
31:16	ROS	0000	**ERR_FATAL/NONFATAL Source Identification (TL)**
15:0	ROS	0000	**ERR_COR Source Identification (TL)**

Virtual Channel Capability (140-14Fh)

Virtual Channel Capability is defined for Egress direction of the device. For Root Port, since only VC0 is defined, there is no implementation of VC Arbitration Table and Port Arbitration Table.

Offset Address: 143-140h (D3F0)
Virtual Channel Enhanced Capability **Default Value: 0001 0002h**

Bit	Attribute	Default	Description
31:20	RO	000h	**Next Capability Offset**
19:16	RO	1h	**Capability Version**
15:0	RO	0002h	**PCI Express Extended Capability ID**

Offset Address: 147-144h (D3F0)
Port VC Capability I — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	—	0	**Reserved**
11:10	RO	0	**Port Arbitration Table Entry Size** Reserved for root port
9:8	RO	0	**Reference Clock** Reserved for root port
7	—	0	**Reserved**
6:4	RO	0	**Low Priority Extended VC Count**
3	—	0	**Reserved**
2:0	RO	0	**Extended VC Count**

Offset Address: 14B-148h (D3F0)
Port VC Capability II — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**VC Arbitration Table Offset** 00 since only VC0 is defined
23:8	—	0	**Reserved**
7:0	RO	00h	**VC Arbitration Capability**

Offset Address: 14D-14Ch (D3F0)
Port VC Control — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	—	0	**Reserved**
3:1	RW	0	**VC Arbitration Select**
0	RW	0	**Load VC Arbitration Table**

Offset Address: 14F-14Eh (D3F0)
Port VC Status — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:1	—	0	**Reserved**
0	RO	0	**VC Arbitration Table Status**

VC0 Resource (150-15Bh)

Offset Address: 153-150h (D3F0)
VC Resource Capability (VC0) — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**Port Arbitration Table Offset (VC0)**
23	—	0	**Reserved**
22:16	RO	00h	**Maximum Time Slots (TL)**
15	RO	0	**Reject Snoop Transactions**
14	RO	0	**Advanced Packet Switching**
13:8	—	0	**Reserved**
7:0	RO	00h	**Port Arbitration Capability**

Offset Address: 157-154h (D3F0)
VC Resource Control (VC0) **Default Value: 8000 00FFh**

Bit	Attribute	Default	Description
31	RO	1	**VC Enable**
30:27	—	0	**Reserved**
26:24	RO	0	**VC ID**
23:20	—	0	**Reserved**
19:17	RW	0	**Port Arbitration Select**
16	RW	0	**Load Port Arbitration Table**
15:8	—	0	**Reserved**
7:0	RW Bit 0: RO	FFh	**TC/VC Mapping** This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC0 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit0 is hardwired to 1 (i.e. TC0 is always mapped to VC0).

Offset Address: 15B-158h (D3F0)
VC Resource Status (VC0) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	—	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)**
16	RO	0	**Port Arbitration Table Status**
15:0	—	0	**Reserved**

VC1 Resource (15C-167h)

The following registers exist only when Rx144[0] is programmed to 1. If Rx144[0]=0, all the following content will be read as 0.

Offset Address: 15F-15Ch (D3F0)
VC Resource Capability (VC1) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**Port Arbitration Table Offset (VC1)**
23	—	0	**Reserved**
22:16	RO	00h	**Maximum Time Slots (TL)**
15	RO	0	**Reject Snoop Transactions**
14	RO	0	**Advanced Packet Switching**
13:8	—	0	**Reserved**
7:0	RO	00h	**Port Arbitration Capability**

Offset Address: 163-160h (D3F0)
VC Resource Control (VC1) **Default Value: 0010 0000h**

Bit	Attribute	Default	Description
31	RW	0	**VC Enable**
30:27	—	0	**Reserved**
26:24	RW	1	**VC ID.**
23:20	—	0	**Reserved**
19:17	RW	0	**Port Arbitration Select**
16	RW	0	**Load Port Arbitration Table**
15:8	—	0	**Reserved**
7:0	RW Bit 0: RO	00h	**TC/VC Mapping** This field indicates the TCs that are mapped to VC1. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC1 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit0 is hardwired to 0 (i.e. TC0 is always mapped to VC0).

Offset Address: 167-164h (D3F0)

VC Resource Status (VC1) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	—	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)**
16	RO	00h	**Port Arbitration Table Status**
15:0	—	0	**Reserved**

Device 3 Function 1 (D3F1) – PCI Express Root Port 2 (PCI-to-PCI Virtual Bridge)

Device 3 Function 1 is an optional 1-Lane PCI Express root port that is connected to the PCI bus through AD14 as the IDSEL. Registers listed in this section are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 3 and function number 1.

Header Registers (0-3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	**Vendor ID**
3 – 2h	RO	D238h	**Device ID**

Offset Address: 5-4h (D3F1)

Command Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	–	0	**Reserved**
10	RW	0	**Interrupt Disabled** Set when the device is prevented from generating INTx messages
9	–	0	**Reserved**
8	RW	0	**SERR# Enable** 0: Disable error report 1: Enable reporting of non-fatal and fatal errors
7	–	0	**Reserved**
6	RW	0	**Parity Error Response** 0: Ignore parity errors & continue 1: Take normal action on detected parity errors
5:3	–	0	**Reserved**
2	RW	0	**Bus Master Enable** 0: Disable 1: Enable Controls the ability to forward Memory and I/O Read/Write requests in the upstream direction. Disabling this bit disables MSI messages.
1	RW	0	**Memory Space** 0: Ignore downstream memory transactions; memory cycles with address falling in the claimed range will be forwarded to the SB 1: Enable downstream memory cycle to this port if its address falling in the claimed range of this device.
0	RW	0	**I/O Space** 0: Ignore downstream I/O transactions; I/O cycles with address falling in the claimed range will be forwarded to the SB. 1: Enable downstream I/O cycle to this port if its address falling in the claimed range of this device.

Offset Address: 7-6h (D3F1)
Status Register **Default Value: 0010h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set whenever a poisoned TLP is received, regardless the state of Parity Error Enabled (Rx4[6])
14	RW1C	0	**Signaled System Error** This bit is set when: 1. A device sends an ERR_FATAL or ERR_NONFATAL message 2. Rx4[8] = 1
13	RW1C	0	**Received Master Abort** This bit is set when receiving a completion with Unsupported Request Completion Status
12	RW1C	0	**Received Target Abort** This bit is set when receiving a completion with Completer Abort Completion Status
11	RW1C	0	**Signaled Target Abort** This bit is set when completing a Request with Completer Abort Completion Status
10:9	–	0	**Reserved (Always 0)**
8	RW1C	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx4[6]) is set and either one of the following two conditions occurs: 1. Requestor receives a Completion marked poisoned 2. Requestor poisons a write Request
7:5	–	0	**Reserved**
4	RO	1	**Capabilities List** Indicates the presence of an extended capability list item. Always set to 1 for PCI Express device
3	RO	0	**Interrupt Status** Indicate an INTx message is pending internally (TL)
2:0	–	0	**Reserved**

Offset Address: 8h (D3F1)
Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Revision Code**

Offset Address: 0B-9h (D3F1)
Class Code **Default Value: 060400h**

Bit	Attribute	Default	Description
23:0	RO	060400h	**Class Code**

Offset Address: 0Ch (D3F1)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00	**Cache Line Size – Reserved (No impact on functionality)**

Offset Address: 0Dh (D3F1)
Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00	**Reserved (Hardwired to 0)**

Offset Address: 0Eh (D3F1)
Header Type **Default Value: 81h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Header Type Code** A multiple function device.

Offset Address: 0Fh (D3F1)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST Support**

Offset Address: 17-10h (D3F1)
Base Address Register **Default Value: 00h**

Bit	Attribute	Default	Description
63:0	–	00h	**Reserved**

Offset Address: 18h (D3F1)
Primary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Primary Bus Number**

Offset Address: 19h (D3F1)
Secondary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Secondary Bus Number**

Offset Address: 1Ah (D3F1)
Subordinate Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Subordinate Bus Number**

Offset Address: 1Ch (D3F1)
I/O Base **Default Value: F0h**

Bit	Attribute	Default	Description
7:4	RW	1111	**I/O Base (AD[15:12] - inclusive)** This bridge will forward the cycles from primary side to PCI if the IO address AD[15:12] is between IO base and IO limit (Rx1D)
3:0	RO	0	**I/O Addressing Capability** 0 means IO addressing is 16-bit only.

Offset Address: 1Dh (D3F1)
I/O Limit **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**I/O Limit (AD[15:12] - inclusive)**
3:0	RO	0	**I/O Addressing Capability** 0 means IO addressing is 16-bit only.

Offset Address: 1F-1Eh (D3F1)
Secondary Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set when secondary side receives a poisoned TLP regardless of Rx4[6]
14	RW1C	0	**Received System Error** This bit is set when Rx4[8] is 1 and a device sends an ERR_FATAL or ERR_NONFATAL message.
13	RW1C	0	**Received Master Abort**
12	RW1C	0	**Received Target Abort**
11	RW1C	0	**Signaled Target Abort**
10:9	—	0	**Reserved**
8	RW1C	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx4[6]) is set and either one of the following two conditions occurs: 1. Requestor receives a Completion marked poisoned. 2. Requestor poisons a write Request
7:0	—	0	**Reserved**

Offset Address: 21-20h (D3F1)
Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Memory Base (AD[31:20] – inclusive)** The address [19:0] is not decoded.
3:0	RO	0000	**Reserved**

Offset Address: 23-22h (D3F1)
Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	000h	**Memory Limit (AD[31:20] – inclusive)** The address [19:0] is not decoded.
3:0	RO	0000	**Reserved**

Offset Address: 25-24h (D3F1)
Prefetchable Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Prefetchable Memory Base AD[31:20]**
3:0	RO	0000	**Reserved**

Offset Address: 27-26h (D3F1)
Prefetchable Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	000h	**Prefetchable Memory Limit AD[31:20]**
3:0	RO	0000	**Reserved**

Offset Address: 2B-28h (D3F1)
Prefetchable Memory Upper Base **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	00h	**Reserved**
3:0	RW	0000	**AD[35:32]** This chip supports up to 16G

Offset Address: 2F-2Ch (D3F1)
Prefetchable Memory Upper Limit **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	00h	**Reserved**
3:0	RW	0000	**AD[35:32]** This chip supports up to 16G

Offset Address: 31-30h (D3F1)
I/O Base Upper **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	00h	**I/O Base Upper 16 bits Address**

Offset Address: 33-32h (D3F1)
I/O Base Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	00h	**I/O Limit Upper 16 bits Address**

Offset Address: 34h (D3F1)
Capability Pointer **Default Value: 40h**

Contains an offset from the start of configuration space.

Bit	Attribute	Default	Description
7:0	RO	40h	**Capability Pointer** Always reads 40h. Capability Pointer link list: Rx34 → Rx40 → Rx68 → NULL

Offset Address: 3Ch (D3F1)
Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**INT Line (For Software Use Only)**

Offset Address: 3Dh (D3F1)
Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**INT Pin** 01: INTA

Offset Address: 3F-3Eh (D3F1)

Bridge Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:7	—	00h	**Reserved**
6	RW	0	**Secondary Bus Reset** 0: No reset 1: Triggers a warm reset on the corresponding PCI Express Port
5	—	0	**Reserved**
4	RW	0	**Base VGA 16 bits Decode** 0: All VGA alias range will be forwarded 1: Only forward base VGA range (Aliased range will not be forwarded)
3	RW	0	**VGA Compatible I/O and Memory Address Range** 0: Do not forward VGA compatible memory and I/O 1: Forward VGA compatible memory and I/O Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.
2	RW	0	**Block/Forward ISA I/O Cycles** 0: Forward all I/O cycles with address in the range defined by the I/O Base and I/O Limit 1: Do not forward ISA I/O that are in the top 768 bytes of each 1K byte block address range
1	RW	0	**SERR Enable** Controls the forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary 0: Disable 1: Enable
0	RW	0	**Parity Error Response Enable** 0: Ignore the response to poisoned TLPs 1: Enable the response to poisoned TLPs

PCI Express Capability Registers (40-63h)

Offset Address: 40-41h (D3F1)

PCI Express List **Default Value: 6810h**

Bit	Attribute	Default	Description
15:8	RO	68h	**Next Pointer**
7:0	RO	10h	**Capability ID**

Offset Address: 43-42h (D3F1)

PCI Express Capabilities **Default Value: 0041h**

Bit	Attribute	Default	Description
15:14	—	0	**Reserved**
13:9	RO	0	**Interrupt Message Number**
8	RO	0	**Slot Implemented** This bit when set indicates that the PCI Express Link associated with this Port is connected to a slot (as compared to being connected to an integrated component or being disabled),
7:4	RO	0100	**Device / Port Type** 0100b: Root Port of PCI Express Root Complex
3:0	RO	1	**Capability Version**

Offset Address: 47-44h (D3F1)

Device Capabilities **Default Value: 0000 0nn1h**

Bit	Attribute	Default	Description
31:28	—	0	**Reserved**
27:26	RO	0	**Captured Slot Power Limit Scale**
25:18	RO	0	**Captured Slot Power Limit Value**
17:15	—	000	**Reserved**
14	RO	0	**Power Indicator Present**
13	RO	0	**Attention Indicator Present**
12	RO	0	**Attention Button Present**
11:9	RO	111	**Endpoint L1 Acceptable Latency** 111b: more than 64us
8:6	RO	xxx	**Endpoint L0s Acceptable Latency**
5		0	**Extended Tag Field Supported** 0: 5-bit Tag field supported 1: 8-bit Tag field supported
4:3	RO	00	**Phantom Functions Supported** Reserved
2:0	RW	001	**Max Payload Size Supported** 001b: 32QW (256 bytes)

Offset Address: 49-48h (D3F1)

Device Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15	—	0	**Reserved**
14:12	RO	000	**Max Read Request Size** 000b: 128 bytes This field sets the maximum Read Request size for the device as a Requestor.
11	RW	0	**Enable No Snoop** If this bit is set to 1, the device is **permitted** to set the No Snoop bit in the Requestor Attributes of the transactions it initiate that do not require hardware enforced cache coherency.
10	RWS	0	**Auxiliary Power PM Enable** This bit when set enables device to draw AUX power independent of PME AUX power.
9	RO	0	**Phantom Functions Enable** Not supported.
8	RO	0	**Extended Tag Field Enable** Not supported.
7:5	RW	0	**Max Payload Size** Maximum TLP payload size.
4	RW	0	**Enable Relaxed Ordering** If this bit is set to 1, the device is **permitted** to set the Relaxed Ordering bit in the Requestor Attributes of the transactions it initiate that do not require strong write ordering.
3	RW	0	**Unsupported Request Reporting Enable**
2	RW	0	**Fatal Error Reporting Enable** For a Root Port, the reporting of Fatal errors is internal to the root. No external ERR_FATAL message is generated.
1	RW	0	**Non-Fatal Error Reporting Enable** For a Root Port, the reporting of Non-Fatal errors is internal to the root. No external ERR_NONFATAL message is generated.
0	RW	0	**Correctable Error Reporting Enable** For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_COR message is generated.

Offset Address: 4B-4Ah (D3F1)

Device Status **Default Value: 0010h**

Bit	Attribute	Default	Description
15:6	—	0	**Reserved**
5	RO	0	**Transactions Pending** This bit when set indicates that the Port has issued Non-Posted Requests on its own behalf (using the Port's own Requestor ID) which have not been completed.
4	RO	1	**AUX Power Detected**
3	RW1C	0	**Unsupported Request Detected**
2	RW1C	0	**Fatal Error Detected (TL)**
1	RW1C	0	**Non-Fatal Error Detected (TL)**
0	RW1C	0	**Correctable Error Detected (TL)**

Offset Address: 4F-4Ch (D3F1)
Link Capabilities **Default Value: 0300 0C11h**

Bit	Attribute	Default	Description
31:24	RO	02h	**Port Number** This field indicates the PCI Express Port number for the given PCI Express Link.
23:18	—	0	**Reserved**
17:15	RO	000	**L1 Exit Latency** 000: less than 1us. The value reported indicates the length of time this Port requires to complete transition from L1 to L0.
14:12	RO	000	**L0s Exit Latency** 000: less than 64ns. The value reported indicates the length of time this Port requires to complete transition from L0s to L0.
11:10	RO	11	**Active State Link PM (ASPM) Support** 11b: L0s and L1 supported. This field indicates the level of ASPM supported on the PCI Express Link.
9:4	RO	01h	**Maximum Link Width** 01h: x1 Link width.
3:0	RO	1	**Maximum Link Speed** 0001b: 2.5Gb/s Link speed

Offset Address: 51-50h (D3F1)
Link Control **Default Value: 0000h**

Bit	Attribute	Default	Description	Mnemonic
15:8	—	0	**Reserved**	
7	RW	0	**Extended Synch** 0: FCU Timer limit is 30us 1: FCU Timer limit is 120us	LCES_PE1
6	RW	0	**Common Clock Configuration** 0: Indicates that this Port and the component on the opposite end of the Link are operating with asynchronous reference clock. 1: Indicates that this Port and the component on the opposite end of the Link are operating with a distributed common reference clock.	
5	RW	0	**Retrain Link** A write of 1 to this bit initiates Link retrained by directing the Physical Layer LTSSM to the Recovery state.	
4	RW	0	**Link Disable** This bit disables the Link when set to 1.	
3	RO	0	**Read Completion Boundary** 0: 64 byte	
2	—	0	**Reserved**	
1:0	RW	00	**Link Active State PM (ASPM) Control** 00b: Disabled 01b: L0s Entry Enabled 10b: L1 Entry Enabled 11b: L0s and L1 Entry Enabled	

Offset Address: 53-52h (D3F1)
Link Status **Default Value: 0nn1h**

Bit	Attribute	Default	Description
15:13	—	0	**Reserved**
12	RO	0	**Slot Clock Configuration** 0: Use an independent clock irrespective of the presence of a reference on the connector. 1: Use the same physical reference clock that the platform provides on the connector.
11	RO	0	**Link Training** This bit indicated that Link training is in progress (Physical Layer LTSSM is in Configuration or Recovery state) or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit once Link training is complete.
10	RO	0	**Training Error** Set when a Link training error occurred. Cleared by hardware upon successfully training of the Link to the L0 Link state.
9:4	RO	xxxxxx	**Negotiated Link Width** 000001: x1 000010: x2 000100: x4 001000: x8 010000: x16
3:0	RO	0001	**Link Speed** 0001: 2.5Gb/s negotiated Link speed.

Offset Address: 57-54h (D3F1)

Slot Capabilities **Default Value: 0000 0060h**

Bit	Attribute	Default	Description
31:19	RO	00h	**Physical Slot Number** Physical slot number attached to the Port.
18:17	—	0	**Reserved**
16:15	RO	0	**Slot Power Limit Scale** Write to the field causes the Port to send the Set_Slot_Power_Limit message.
14:7	RO	00h	**Slot Power Limit Value** Write to the field causes the Port to send the Set_Slot_Power_Limit message.
6	RO	1	**Hot-plug Capable**
5	RO	1	**Hot-plug Surprise**
4	RO	0	**Power Indicator Present**
3	RO	0	**Attention Indicator Present**
2	RO	0	**MRL Sensor Present**
1	RO	0	**Power Controller Present**
0	RO	0	**Attention Button Present**

Offset Address: 59-58h (D3F1)

Slot Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	—	0	**Reserved**
10	RO	0	**Power Controller Control** 0: Power On 1: Power Off
9:8	RW	0	**Power Indicator Control** 00: Reserved 01: On 10: Blink 11: Off Writes to this field cause the Port to send the appropriate POWER_INDICATOR_* Message.
7:6	RW	0	**Attention Indicator Control** 00: Reserved 01: On 10: Blink 11: Off Writes to this field cause the Port to send the appropriate ATTENTION_INDICATOR_* Message.
5	RW	0	**Hot-Plug Interrupt Enable** This bit when set enables generation of Hot-Plug interrupt on enabled Hot-Plug events.
4	RW	0	**Command Completed Interrupt Enable** This bit when set enables the generation of Hot-Plug interrupt when a command is completed by the Hot-Plug controller.
3	RW	0	**Presence Detect Changed Enable** This bit when set enables the generation of Hot-Plug interrupt or Wakeup event on a presence detect changed event.
2	RO	0	**MRL Sensor Changed Enable**
1	RO	0	**Power Fault Detected Enable**
0	RW	0	**Attention Button Pressed Enable** This bit when set enables the generation of Hot-Plug interrupt or Wakeup event on an Attention Button pressed event.

Offset Address: 5A-5Bh (D3F1)

Slot Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:7	—	0	**Reserved**
6	RO	0	**Presence Detect State** 0: Slot empty 1: Card present in slot
5	RO	0	**MRL Sensor State**
4	RW1C	0	**Command Completed**
3	RW1C	0	**Presence Detect Changed**
2	RO	0	**MRL Sensor Changed**
1	RO	0	**Power Fault Detected**
0	RW1C	0	**Attention Button Pressed**

Offset Address: 5D-5Ch (D3F1)

Root Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	—	0	**Reserved**
3	RW	0	**PME Interrupt Enable** 0: Disable 1: Enable interrupt generation upon receipt of a PME message as reflected in the PME status register bit. A PME interrupt is also generated if the PME status register bit is set when this bit is set from a cleared state.
2	RW	0	**System Error on Fatal Error Enable** 0: Disable 1: Enable generation of a System Error if a Fatal Error (ERR_FATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
1	RW	0	**System Error on Non-Fatal Error Enable** 0: Disable 1: Enable generation of a System Error if a Non-Fatal Error (ERR_NONFATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
0	RW	0	**System Error on Correctable Error Enable** 0: Disable 1: Enable generation of a System Error if a Correctable Error (ERR_COR) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.

Offset Address: 63-60h (D3F1)

Root Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	—	0	**Reserved**
17	RO	0	**PME Pending** 0: No pending PME 1: Indicates that another PME is pending when the PME Status (bit 16) is set.
16	RW1C	0	**PME Status** Indicates that the PME was asserted by the Requestor ID indicated in PME Requestor ID (bit[15:0]).
15:0	RO	00h	**PME Requestor ID** The Requestor ID of the last PME Requestor.

PCI Power Management Capability Structure Registers (68-6Fh)

Offset Address: 6B-68h (D3F1)

Power Management Capabilities **Default Value: C802 7001h**

Bit	Attribute	Default	Description
31:27	RW	11001	**PME Support** Bit 31, 30 and 27 are set to 1b (PME Message will be forwarded).
26	RW	0	**D2 Support**
25	RW	0	**D1 Support**
24:22	RO	0	**AUX Current**
21	RW	1	**Device Specific Initialization**
20:19	—	0	**Reserved**
18:16	RO	010	**Version**
15:8	RO	70h	**Next Capability Pointer**
7:0	RO	01h	**Capability ID**

Offset Address: 6F-6Ch (D3F1)
Power Management Status/Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**Power Management Data**
23:16	RO	—	**Reserved**
15	RW1CS	0	**PME Status** This bit's setting is not modified by hot, warm, or cold reset.
14:13	RO	0	**Data Scale**
12:9	RW	0	**Data Select**
8	RWS	0	**PME Enable** This bit's setting is not modified by hot, warm, or cold reset.
7:2	RO	0	**Reserved**
1:0	RW	0	**Power State**

PCI Message Signal Interrupt (MSI) Capability Structure Registers (70-87h)

Offset Address: 73-70h (D3F1)
MSI Capability Support **Default Value: 0180 0005h**

Bit	Attribute	Default	Description
31:25	—	0	**Reserved**
24	RW	1	**This MSI capability supports pre-vector masking capability**
23	RO	1	**This MSI capability supports 64 bit message address only**
22:20	RW	000	**Multiple Message Enable** 000: 1message allocated 001: 2 message allocated 010: 4 message allocated 011: 8 message allocated 100: 16 message allocated 101: 32 message allocated 11x: Reserved
19:17	RO	000	**Multiple Message Capable** 000: 1message requested 001: 2 message requested 010: 4 message allocated 011: 8 message allocated 100: 16 message requested 101: 32 message requested 11x: Reserved
16	RW	0	**MSI Enable** 0: This Port is prohibited from using MSI to request service 1: This Port is permitted to use MSI to request service.
15:8	RO	00h	**Next Capability Pointer**
7:0	RO	05h	**Capability ID**

Offset Address: 77-74h (D3F1)
System-Specified Message Address - Low **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	00h	**System-Specified Message Address Bit [31:2]**
1:0	RO	00	**System-Specified Message Address Bit [1:0]** These bits will always read as 0

Offset Address: 7B-78h (D3F1)
System-Specified Message Address - High **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	00h	**System-Specified Message Address Bit [63:36]** These bits will always read as 0 since this chip supports address up to A35.
3:0	RW	0	**System-Specified Message Address Bit [35:32]**

Offset Address: 7D-7Ch (D3F1)
Message Data **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Message Data** The message data is to be put on data [15:0] of MSI cycles

Offset Address: 83-80h (D3F1)
Message Mask Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	00h	**Mask Bit**
0	RW	0	**Mask Bit for Message 0**

Offset Address: 87-84h (D3F1)
Message Pending Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	00h	**Pending Bit**
0	RO	0	**Pending Bit for Message 0**

PCI Express Transaction Layer Registers (A0-A4h)

Offset Address: A0h (D3F1)
Downstream Control I **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Cycles Have Traffic Class TC1** 0: Disabled 1: Enabled.
6	RW	0	**Downstream Cycles Have Attribute "No Snoop" Set** 0: Disabled 1: Enabled.
5	RW	0	**Downstream Cycles Have Attribute "Relaxed Ordering" Set** 0: Disabled 1: Enabled.
4	RW	0	**Downstream Lock Cycle Support** 0: Disabled 1: Enabled.
3	RW	0	**Downstream Arbitration Scheme** 0: Fixed priority: VC1 CPL > VC0 CPL > Down Stream Command 1: Round Robin arbitration priority between VC1 CPL, VC0 CPL and Down Stream Command
2	RW	0	**Downstream Post-Write Allowed to Pass IOW** 0: Not allowed. 1: Allowed.
1	RW	0	**Downstream Post-Write Allowed to Pass Read** 0: Not allowed. 1: Allowed.
0	RW	1	**Downstream Pipeline** 0: Disabled 1: Enabled.

Offset Address: A1h (D3F1)
Downstream Control II **Default Value: 04h**

Bit	Attribute	Default	Description
7	RW1C	0	**Downstream Configuration Completion Status** 0: Normal completion. 1: At least one configuration request ended with a CRS (Configuration Request Retry Status) completion.
6:4	—	0	**Reserved**
3	RW	0	**C2P Read Completion Timer for Vector Development Mode:** When this bit is set to 1, the timer defined in RxA1[2:0] becomes: 0xx: 1us 1xx: 3us
2:0	RW	100	**C2P Read Completion Timeout Timer** 000: Reserved 001: 1ms 010: Reserved 011: 10ms (Spec. lower bound) 100: 30ms 101: 50ms (Spec. higher bound) 110: 100ms 111: Reserved

Offset Address: A4h (D3F1)
Upstream Control **Default Value: 01h**

Bit	Attribute	Default	Description
7	RW	0	**Upstream Address A35~A31 Forced to 0** 0: Disabled. 1: Enabled for system testing or loop back mode test. The upcoming data may be checked in the system memory
6	—	0	**Reserved**
5	RW	0	**Upstream Checking Malformed TLP through "Byte Enable Rule" And "Over 4K Boundary Rule"** 0: Disabled. 1: Enabled.
4	RW	1	**Downstream Read Wait Till The Upstream Write Data Flushed** 0: Disabled. 1: Enabled.
3:2	—	0	**Reserved**
1	RW	0	**VC1 Request Queue Usage** (when VC1 is disabled in the capability header; i.e. Rx144[0] = 0) 0: Disabled. 1: Enabled, it allows Transaction Layer map non-snoop upstream request through VC1 Request Queue to the Central Traffic Controller (Note that when this bit is 1, bit-0 has to be 0).
0	RW	0	**Disable Virtual Channel 1 Support** 0: Enable VC1, data FIFO of VC1 is used by VC1 1: Disable VC1, data FIFO of VC1 is reallocated to VC0, which doubles the size of VC0 data FIFO.

PCI Express Data Link Layer Registers (B0-B6h)

Offset Address: B0h (D3F1)
Ack/Nak Latency Timer Limit **Default Value: 3Bh**

Bit	Attribute	Default	Description
7:0	RW	3Bh	**Timer Limit for Ack/Nak Latency Timer and Update FC Latency Timer (in unit of 250MHz)** 00: 4 x 1 Clocks 01: 4 x 2 Clocks 02: 4 x 3 Clocks. 0n: 4 x (n+1) Clocks FF: 4 x 256 Clocks.

Offset Address: B1h (D3F1)
Replay Timer Limit **Default Value: 59h**

Bit	Attribute	Default	Description
7:0	RW	59h	**Replay Timer Limit (In unit of 250MHz)** 00: 8 x 1 Clocks 01: 8 x 2 Clocks 02: 8 x 3 Clocks 0n: 8 x (n+1) Clocks FF: 8 x 256 Clocks.

Offset Address: B2h (D3F1)
FCU Control and Status **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW1C	0	**FCU Timeout Status** 1 means the FCU timeout has occurred
6	RW	1	**FCU Receive Timer Enable Control** 0: Disable the timeout mechanism 1: Enable the timeout mechanism
5	RW	0	**FCU Receive Timer Limit** 0: Timeout limit of 200us 1: Timeout limit of 300us
4	RW	0	**FCU Receive Timer Reset Control** 0: Timer reset by FCI/FCU only 1: Timer reset by any received DLLPs
3:0	—	0	**Reserved**

Offset Address: B3h (D3F1)

Replay Timer Control **Default Value: 80h**

Bit	Attribute	Default	Description
7:6	RW	10	**Replay Timer Control while Rewind** (resend those DLLPs which do not have corresponding ACK/NAK received) 00: Hold Replay Timer during rewind. 01: During rewind, if ACK/NAK comes in, reset and hold the Replay Timer. 10: During rewind, reset and hold the Replay Timer as long as the Retry Buffer is empty. 11: Reserved.
5:3	–	0	**Reserved**
2:0	RW	000	**Count of Replay Timer Expired During RXL0s** (Receiving Physical in L0s state) **Before Resend the TLP** **When Rx50[7], LCES_PE1, is set to 0:** 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 1 x Replay timer expired 010: Resend the TLP after 2 x Replay timer expired 011: Resend the TLP after 4 x Replay timer expired 100: Resend the TLP after 8 x Replay timer expired 101: Resend the TLP after 16 x Replay timer expired 110: Resend the TLP after 32 x Replay timer expired 111: Resend the TLP after 64 x Replay timer expired **When RX50[7], LCES_PE1, is set to 1:** 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 16 x Replay timer expired 010: Resend the TLP after 32 x Replay timer expired 011: Resend the TLP after 64 x Replay timer expired 100: Resend the TLP after 128 x Replay timer expired 101: Resend the TLP after 256 x Replay timer expired 110: Resend the TLP after 512 x Replay timer expired 111: Resend the TLP after 1024 x Replay timer expired

Offset Address: B4h (D3F1)

Arbitration Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	–	0	**Reserved**
3	RW	0	**TLP vs. Flow Control Initialization for VC0 in Arbitration Priority** 0: TLP is not allowed to pass FCI2 for VC0 1: TLP is allowed to pass FCI2 for VC0
2:0	RW	000	**Data Link TX Packets Arbitration Scheme** 000: Round Robin 001: Reserved. 010: Strict priority: TLP > ACK/NAK > FCU 011: Strict priority: TLP > FCU > ACK/NAK 100: Strict priority: ACK/NAK > TLP > FCU 101: Strict priority: ACK/NAK > FCU > TLP 110: Strict priority: FCU > TLP > ACK/NAK 111: Strict priority: FCU > ACK/NAK > TLP

Offset Address: B5h (D3F1)

FCU Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	**Reserved**
6	RW	0	**FCU (Flow Control Unit) Timer Control** 0: Update flow control credit when either Transaction Layer requested packets being sent or when FCU timer expired 1: Update flow control credit only when FCU timer expired
5:4	RW	00	**ACK DLLP Collapse Method** 00: Send ACK when the latency timer RACKLTLM (RxB0) expired. 01: Send ACK every 4 correct TLP has been received 10: Send ACK every 8 correct TLP has been received 11: Send ACK every 16 correct TLP has been received
3:2	—	0	**Reserved**
1	RW	0	**FCI (Flow Control Initialization) Process End Condition** 0: Complete FCI process when TLP/FCU has been received 1: Do not complete FCI process even when TLP/FCU has been received
0	RW	0	**VC1 FCI DLLP Transmission Scheme** 0: Transmit FCI DLLP only when FCI timer expired 1: Transmit FCI DLLP continuously as long as the FCI process is not finished

Offset Address: B6h (D3F1)

Transaction / Link Layer Checking Control **Default Value: 03h**

Bit	Attribute	Default	Description
7:5	—	0	**Reserved**
4	RW	0	**VC Negotiate Pending Control for VC1** 0: Assert VC negotiation pending after VC1 is enabled 1: Assert VC negotiation pending after RESET is de-asserted
3	—	0	**Reserved**
2	RW	0	**ECRC Checking Control for the Case of TD equals to1 but no ECRC field in TLP** 0: Ignore the error 1: Report error to Transaction Layer, which will mark the TLP as a Malformed TLP
1	RW	1	**Length Malform Report Control** 0: Do not report length malform to Transaction Layer 1: Report length malform to Transaction Layer
0	RW	1	**LCRC Checking Control** 0: Do not check LCRC 1: Check LCRC

PCI Express Physical Layer Registers (C0-C7h)

Offset Address: C3-C0h (D3F1)

PHY Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	–	0	**Reserved**
7	RW	0	**Quick Timeout Counter Setting** When set to 1, the following timeout will be shorter when set: TIMEOUT_2MS → TIMEOUT_4US TIMEOUT_12MS → TIMEOUT_24US TIMEOUT_24MS → TIMEOUT_48US TIMEOUT_48MS → TIMEOUT_96US TIMEOUT_1024TS → TIMEOUT_32TS
6	RW	0	**Disable Data Scrambling/Descrambling** 0: Enable 1: Disable
5:3	RW	000	**Loopback Mode Selection** 000: No loop back 001: PHYLS loopback from TX end to RX end 010: PHYES loopback from TX end to RX end 011: Reserved 100: Reserved 101: PHYLS loopback from RX end to TX end 110: PHYES loopback from RX end to TX end 111: Reserved
2:0	–	0	**Reserved**

Offset Address: C7-C4h (D3F1)

Elastic Buffer Base Registers for Lane 0 **Default Value: 0000 0004h**

Bit	Attribute	Default	Description
31:3	–	0	**Reserved**
2:0	RW	4	**Elastic Buffer Base Register for Lane 0** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations

PCI Express Power Management Module Registers (D0-D3h)

Offset Address: D3-D0h (D3F1)

PMC Control **Default Value: 0000 0050h**

Bit	Attribute	Default	Description
31:24	RW	00h	**Idle Period for Entering ASL1** Minimum time period is 128ns 00: 128ns 01: 2x128ns 02: 3x128ns ... FF: 256x128ns
23:16	RW	00h	**Idle Period for Entering L0s** Minimum time period is 128ns (L0SLIM_PE1 = 00) 00: 128ns 01: 2x128ns 02: 3x128ns ... FF: 256x128ns
15	RW1C	0	**Error Status Report** This bit is set when device cannot have electrical idle after the waiting period programmed at RxD1[6:4] expired.
14	—	0	**Reserved**
13:12	RW	0	**Electrical Idle Waiting Period before Move to L1 State** (after issue ACK to the L1 request from the device). 00: Always wait for electrical idle 01: Wait 32 clock 10: Wait 64 clock 11: Reserved
11:10	—	0	**Reserved**
9:8	RW	0	**Downstream Cycles Triggered C2P Cycles, Period of Staying at L0 Before Returned to L1 for PHY** (when PMU is in non-D0 state) 00: immediately 01: 1 cfgW or message + delay10T 10: 1 32QW +1cfgW or message+ delay10T 11: 2 32QW +1 cfgW or message +delay10T
7:2	—	0	**Reserved**
1	RW	0	**Link Loopback** 0: Normal operation 1: Direct device to enter Loopback mode, receiving data in the device will be sent to the transmit side
0	RW	0	**LTSSM State During Link Reconfigure Link Width** 0: When reconfigure link width, LTSSM must be in Detect state 1: When reconfigure link width, LTSSM can be in Configuration state

PCI Express Message Controller Related Registers (D8h)

Offset Address: D8h (D3F1)

PMC Express Message Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Excessive Errors Happened Occurred But Not Reported in The MSGC** 0: Normal operation. 1: There are errors not reported to the system
6:0	—	0	**Reserved**

PCI Express Electrical PHY Registers (E1h)

Offset Address: E1h (D3F1)

PHYES Module Related Control **Default Value: 08h**

Bit	Attribute	Default	Description
7:5	—	0	**Reserved**
4	RW	0	**Receiving Polarity Change Control** 0: Have the same polarity on the loop-back/received data. 1: Have reverse polarity on the loop-back/received data.
3:2	RW	10	**Sqeulch Window Select. (64~175mv)**
1	RW	0	**Electrical Idle State Exit Condition: Number of Non Idle Signal Detected Before Exit Idle State** 0: 2 bits. 1: 10 bits.
0	RW	0	**Electrical Idle State Enter Condition: Number of Idle Signal Detected Before Enter Idle State** 0: 2 bits 1: 10 bits

Device 3 Function 1 (D3F1) – PCI Express Root Port 2 Extended Space

Registers defined in the Extended Space can be accessed through PCI Express Enhanced Configuration Access Mechanism, which utilizes a flat memory-mapped address space to access the configuration registers. Please check PCI Express Specification for the detail information.

Advanced Error Reporting Capability (100-137h)

Offset Address: 103-100h (D3F1)

Advanced Error Reporting Enhanced Capability Header **Default Value: 1401 0001h**

Bit	Attribute	Default	Description
31:20	RO	140h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	0001h	PCI Express Extended Capability ID

Offset Address: 107-104h (D3F1)

Uncorrectable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	–	0	Reserved
20	RW1CS	0	Unsupported Request Error Status (TL)
19	RW1CS	0	ECRC Error Status (TL)
18	RW1CS	0	Malformed TLP Status (TL)
17	RW1CS	0	Receiver Overflow Status (TL)
16	RW1CS	0	Unexpected Completion Status (TL)
15	RW1CS	0	Completer Abort Status (TL)
14	RW1CS	0	Completion Timeout Status (TL)
13	RW1CS	0	Flow Control Protocol Error Status (TL)
12	RW1CS	0	Poisoned TLP Status (TL)
11:5	–	0	Reserved
4	RW1CS	0	Data Link Protocol Error Status (DLL)
3:1	–	0	Reserved
0	RW1CS	0	Training Error Status (PHY)

Offset Address: 10B-108h (D3F1)

Uncorrectable Error Mask **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	–	0	Reserved
20	RWS	0	Unsupported Request Error Mask (TL)
19	RWS	0	ECRC Error Mask (TL)
18	RWS	0	Malformed TLP Mask (TL)
17	RWS	0	Receiver Overflow Mask (TL)
16	RWS	0	Unexpected Completion Mask (TL)
15	RWS	0	Completed Abort Mask (TL)
14	RWS	0	Completion Timeout Mask (TL)
13	RWS	0	Flow Control Protocol Error Mask (TL)
12	RWS	0	Poisoned TLP Mask (TL)
11:5	–	0	Reserved
4	RWS	0	Data Link Protocol Error Mask (DLL)
3:1	–	0	Reserved
0	RWS	0	Training Error Mask (PHY)

Offset Address: 10F-10Ch (D3F1)
Uncorrectable Error Severity **Default Value: 0006 0011h**

Bit	Attribute	Default	Description
31:21	—	0	Reserved
20	RWS	0	Unsupported Request Error Severity (TL)
19	RWS	0	ECRC Error Severity (TL)
18	RWS	1	Malformed TLP Severity (TL)
17	RWS	1	Receiver Overflow Error Severity (TL)
16	RWS	0	Unexpected Completion Error Severity (TL)
15	RWS	0	Completed Abort Error Severity (TL)
14	RWS	0	Completion Timeout Error Severity (TL)
13	RWS	0	Flow Control Protocol Error Severity (TL)
12	RWS	0	Poisoned TLP Severity (TL)
11:5	—	0	Reserved
4	RWS	1	Data Link Protocol Error Severity (DLL)
3:1	—	0	Reserved
0	RWS	1	Training Error Severity (PHY)

Offset Address: 113-110h (D3F1)
Correctable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:13	—	0	Reserved
12	RW1CS	0	Replay Timer Timeout Status (DLL)
11:9	—	0	Reserved
8	RW1CS	0	REPLAY_NUM Rollover Status (DLL)
7	RW1CS	0	Bad DLLP Status (DLL)
6	RW1CS	0	Bad TLP Status (DLL)
5:1	—	0	Reserved
0	RW1CS	0	Receiver Error Status (PHY)

Offset Address: 117-114h (D3F1)
Correctable Error Mask **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:13	—	0	Reserved
12	RWS	0	Replay Timer Timeout Mask (DLL)
11:9	—	0	Reserved
8	RWS	0	REPLAY_NUM Rollover Mask (DLL)
7	RWS	0	Bad DLLP Mask (DLL)
6	RWS	0	Bad TLP Mask (DLL)
5:1	—	0	Reserved
0	RWS	0	Receiver Error Mask (PHY)

Offset Address: 11B-118h (D3F1)
Advanced Error Capabilities and Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:9	—	0	Reserved
8	RWS	0	ECRC Check Enable (TL)
7	RO		ECRC Check Capable (TL)
6	RWS	0	ECRC Generation Enable (TL)
5	RO		ECRC Generation Capable (TL)
4:0	ROS		First Error Pointer (TL)

Offset Address: 12B-11Ch (D3F1)
Header Log (TL)

Register Offset Address	Attribute	Default	Description
11F - 11C	ROS	00h	**Header Log Register 1st DW**
123 - 120	ROS	00h	**Header Log Register 2nd DW**
127 - 124	ROS	00h	**Header Log Register 3rd DW**
12B – 128	ROS	00h	**Header Log Register 4th DW**

Offset Address: 12F-12Ch (D3F1)
Root Error Command **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:3	–	0	**Reserved**
2	RW	0	**Fatal Error Reporting Enable**
1	RW	0	**Non-Fatal Error Reporting Enable**
0	RW	0	**Correctable Error Reporting Enable**

Offset Address: 133-130Ch (D3F1)
Root Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	00h	**Advanced Error Interrupt Message Number (TL)**
26:7	–	0	**Reserved**
6	RW1CS	0	**Fatal Error Messages Received (TL)**
5	RW1CS	0	**Non-Fatal Error Messages Received (TL)**
4	RW1CS	0	**First Uncorrectable Fatal Error Message Received (TL)** Set to 1 when the first Uncorrectable Error Message received is for a Fatal Error
3	RW1CS	0	**Multiple ERR_FATAL/NONFATAL Received (TL)**
2	RW1CS	0	**ERR_FATAL/NONFATAL Received (TL)**
1	RW1CS	0	**Multiple ERR_COR Received (TL)**
0	RW1CS	0	**ERR_COR Received (TL)**

Offset Address: 137-134Ch (D3F1)
Error Source Identification **Default Value: 0000 0000h**

This register is updated regardless of the settings of Root Control register and the Root Error Command register

Bit	Attribute	Default	Description
31:16	ROS	0000	**ERR_FATAL/NONFATAL Source Identification (TL)**
15:0	ROS	0000	**ERR_COR Source Identification (TL)**

Virtual Channel Capability (140-14Fh)

Virtual Channel Capability is defined for Egress direction of the device. For Root Port, since only VC0 is defined, there is no implementation of VC Arbitration Table and Port Arbitration Table.

Offset Address: 143-140h (D3F1)
Virtual Channel Enhanced Capability **Default Value: 0001 0002h**

Bit	Attribute	Default	Description
31:20	RO	000h	**Next Capability Offset**
19:16	RO	1h	**Capability Version**
15:0	RO	0002h	**PCI Express Extended Capability ID**

Offset Address: 147-144h (D3F1)
Port VC Capability I **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	—	0	**Reserved**
11:10	RO	0	**Port Arbitration Table Entry Size** Reserved for root port
9:8	RO	0	**Reference Clock** Reserved for root port
7	—	0	**Reserved**
6:4	RO	0	**Low Priority Extended VC Count**
3	—	0	**Reserved**
2:0	RO	0	**Extended VC Count**

Offset Address: 14B-148h (D3F1)
Port VC Capability II **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**VC Arbitration Table Offset** 00 since only VC0 is defined
23:8	—	0	**Reserved**
7:0	RO	00h	**VC Arbitration Capability;** Reserved since Low Priority Extended Count (Rx144[6:4]) is 0.

Offset Address: 14D-14Ch (D3F1)
Port VC Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	—	0	**Reserved**
3:1	RW	0	**VC Arbitration Select**
0	RW	0	**Load VC Arbitration Table**

Offset Address: 14F-14Eh (D3F1)
Port VC Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:1	—	0	**Reserved**
0	RO	0	**VC Arbitration Table Status**

VC0 Resource (150-15Bh)

Offset Address: 153-150h (D3F1)
VC Resource Capability (VC0) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**Port Arbitration Table Offset (VC0)**
23	—	0	**Reserved**
22:16	RO	00h	**Maximum Time Slots (TL)**
15	RO	0	**Reject Snoop Transactions**
14	RO	0	**Advanced Packet Switching**
13:8	—	0	**Reserved**
7:0	RO	00h	**Port Arbitration Capability**

Offset Address: 157-154h (D3F1)

VC Resource Control (VC0) **Default Value: 8000 00FFh**

Bit	Attribute	Default	Description
31	RO	1	**VC Enable**
30:27	—	0	**Reserved**
26:24	RO	0	**VC ID**
23:20	—	0	**Reserved**
19:17	RW	0	**Port Arbitration Select**
16	RW	0	**Load Port Arbitration Table**
15:8	—	0	**Reserved**
7:0	RW Bit 0: RO	FFh	**TC/VC Mapping** This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC0 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit0 is hardwired to 1 (i.e. TC0 is always mapped to VC0).

Offset Address: 15B-158h (D3F1)

VC Resource Status (VC0) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	—	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)**
16	RO	0	**Port Arbitration Table Status**
15:0	—	0	**Reserved**

VC1 Resource (15C-167h)

The following registers exist only when Rx144[0] is programmed to 1. If Rx144[0]=0, all the following content will be read as 0.

Offset Address: 15F-15Ch (D3F1)

VC Resource Capability (VC1) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**Port Arbitration Table Offset (VC1)**
23	—	0	**Reserved**
22:16	RO	00h	**Maximum Time Slots (TL)**
15	RO	0	**Reject Snoop Transactions**
14	RO	0	**Advanced Packet Switching**
13:8	—	0	**Reserved**
7:0	RO	00h	**Port Arbitration Capability**

Offset Address: 163-160h (D3F1)

VC Resource Control (VC1) **Default Value: 0010 0000h**

Bit	Attribute	Default	Description
31	RW	0	**VC Enable**
30:27	–	0	**Reserved**
26:24	RW	1	**VC ID.**
23:20	–	0	**Reserved**
19:17	RW	0	**Port Arbitration Select**
16	RW	0	**Load Port Arbitration Table**
15:8	–	0	**Reserved**
7:0	RW Bit 0: RO	00h	**TC/VC Mapping** This field indicates the TCs that are mapped to VC1. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC1 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit0 is hardwired to 0 (i.e. TC0 is always mapped to VC0).

Offset Address: 167-164h (D3F1)

VC Resource Status (VC1) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	–	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)**
16	RO	00h	**Port Arbitration Table Status**
15:0	–	0	**Reserved**

Device 3 Function 2 (D3F2) – PCI Express Root Port 3 (PCI-to-PCI Virtual Bridge)

Device 3 Function 2 is an optional 1-Lane PCI Express root port that is connected to the PCI bus through AD14 as the IDSEL. Registers listed in this section are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 3 and function number 2.

Header Registers (0-3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	**Vendor ID**
3 – 2h	RO	E238h	**Device ID**

Offset Address: 5-4h (D3F2)

Command Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	–	0	**Reserved**
10	RW	0	**Interrupt Disabled** Set when the device is prevented from generating INTx messages
9	–	0	**Reserved**
8	RW	0	**SERR# Enable** 0: Disable error report 1: Enable reporting of non-fatal and fatal errors
7	–	0	**Reserved**
6	RW	0	**Parity Error Response** 0: Ignore parity errors & continue 1: Take normal action on detected parity errors
5:3	–	0	**Reserved**
2	RW	0	**Bus Master Enable** 0: Disable 1: Enable Controls the ability to forward Memory and I/O Read/Write requests in the upstream direction. Disabling this bit disables MSI messages.
1	RW	0	**Memory Space** 0: Ignore downstream memory transactions; memory cycles with address falling in the claimed range will be forwarded to the SB 1: Enable downstream memory cycle to this port if its address falling in the claimed range of this device.
0	RW	0	**I/O Space** 0: Ignore downstream I/O transactions; I/O cycles with address falling in the claimed range will be forwarded to the SB. 1: Enable downstream I/O cycle to this port if its address falling in the claimed range of this device.

Offset Address: 7-6h (D3F2)

Status Register **Default Value: 0010h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set whenever a poisoned TLP is received, regardless the state of Parity Error Enabled (Rx4[6])
14	RW1C	0	**Signaled System Error** This bit is set when: 3. A device sends an ERR_FATAL or ERR_NONFATAL message 4. Rx4[8] = 1
13	RW1C	0	**Received Master Abort** This bit is set when receiving a completion with Unsupported Request Completion Status
12	RW1C	0	**Received Target Abort** This bit is set when receiving a completion with Completer Abort Completion Status
11	RW1C	0	**Signaled Target Abort** This bit is set when completing a Request with Completer Abort Completion Status
10:9	–	0	**Reserved (Always 0)**
8	RW1C	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx4[6]) is set and either one of the following two conditions occurs: 3. Requestor receives a Completion marked poisoned 4. Requestor poisons a write Request
7:5	–	0	**Reserved**
4	RO	1	**Capabilities List** Indicates the presence of an extended capability list item. Always set to 1 for PCI Express device
3	RO	0	**Interrupt Status** Indicate an INTx message is pending internally (TL)
2:0	–	0	**Reserved**

Offset Address: 8h (D3F2)

Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Revision Code**

Offset Address: 0B-9h (D3F2)

Class Code **Default Value: 060400h**

Bit	Attribute	Default	Description
23:0	RO	060400h	**Class Code**

Offset Address: 0Ch (D3F2)

Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00	**Cache Line Size – Reserved (No impact on functionality)**

Offset Address: 0Dh (D3F2)

Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00	**Reserved (Hardwired to 0)**

Offset Address: 0Eh (D3F2)

Header Type **Default Value: 81h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Header Type Code** A multiple function device.

Offset Address: 0Fh (D3F2)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST Support**

Offset Address: 17-10h (D3F2)
Base Address Register **Default Value: 00h**

Bit	Attribute	Default	Description
63:0	–	00h	**Reserved**

Offset Address: 18h (D3F2)
Primary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Primary Bus Number**

Offset Address: 19h (D3F2)
Secondary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Secondary Bus Number**

Offset Address: 1Ah (D3F2)
Subordinate Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Subordinate Bus Number**

Offset Address: 1Ch (D3F2)
I/O Base **Default Value: F0h**

Bit	Attribute	Default	Description
7:4	RW	1111	**I/O Base (AD[15:12] - inclusive)** This bridge will forward the cycles from primary side to PCI if the IO address AD[15:12] is between IO base and IO limit (Rx1D)
3:0	RO	0	**I/O Addressing Capability** 0 means IO addressing is 16-bit only.

Offset Address: 1Dh (D3F2)
I/O Limit **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**I/O Limit (AD[15:12] - inclusive)**
3:0	RO	0	**I/O Addressing Capability** 0 means IO addressing is 16-bit only.

Offset Address: 1F-1Eh (D3F2)
Secondary Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set when secondary side receives a poisoned TLP regardless of Rx4[6]
14	RW1C	0	**Received System Error** This bit is set when Rx4[8] is 1 and a device sends an ERR_FATAL or ERR_NONFATAL message.
13	RW1C	0	**Received Master Abort**
12	RW1C	0	**Received Target Abort**
11	RW1C	0	**Signaled Target Abort**
10:9	–	0	**Reserved**
8	RW1C	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx4[6]) is set and either one of the following two conditions occurs: 1. Requestor receives a Completion marked poisoned. 2. Requestor poisons a write Request
7:0	–	0	**Reserved**

Offset Address: 21-20h (D3F2)
Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Memory Base (AD[31:20] – inclusive)** The address [19:0] is not decoded.
3:0	RO	0000	**Reserved**

Offset Address: 23-22h (D3F2)
Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	000h	**Memory Limit (AD[31:20] – inclusive)** The address [19:0] is not decoded.
3:0	RO	0000	**Reserved**

Offset Address: 25-24h (D3F2)
Prefetchable Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Prefetchable Memory Base AD[31:20]**
3:0	RO	0000	**Reserved**

Offset Address: 27-26h (D3F2)
Prefetchable Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	000h	**Prefetchable Memory Limit AD[31:20]**
3:0	RO	0000	**Reserved**

Offset Address: 2B-28h (D3F2)
Prefetchable Memory Upper Base **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	00h	**Reserved**
3:0	RW	0000	**AD[35:32]** This chip supports up to 16G

Offset Address: 2F-2Ch (D3F2)
Prefetchable Memory Upper Limit **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	00h	**Reserved**
3:0	RW	0000	**AD[35:32]** This chip supports up to 16G

Offset Address: 31-30h (D3F2)
I/O Base Upper **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	00h	**I/O Base Upper 16 bits Address**

Offset Address: 33-32h (D3F2)
I/O Base Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	00h	**I/O Limit Upper 16 bits Address**

Offset Address: 34h (D3F2)
Capability Pointer **Default Value: 40h**

Contains an offset from the start of configuration space.

Bit	Attribute	Default	Description
7:0	RO	40h	**Capability Pointer** Always reads 40h. Capability Pointer link list: Rx34 → Rx40 → Rx68 → NULL

Offset Address: 3Ch (D3F2)
Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**INT Line (For Software Use Only)**

Offset Address: 3Dh (D3F2)
Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**INT Pin** 01: INTA

Offset Address: 3F-3Eh (D3F2)

Bridge Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:7	–	00h	**Reserved**
6	RW	0	**Secondary Bus Reset** 0: No reset 1: Triggers a warm reset on the corresponding PCI Express Port
5	–	0	**Reserved**
4	RW	0	**Base VGA 16 bits Decode** 0: All VGA alias range will be forwarded 1: Only forward base VGA range (Aliased range will not be forwarded)
3	RW	0	**VGA Compatible I/O and Memory Address Range** 0: Do not forward VGA compatible memory and I/O 1: Forward VGA compatible memory and I/O Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.
2	RW	0	**Block/Forward ISA I/O Cycles** 0: Forward all I/O cycles with address in the range defined by the I/O Base and I/O Limit 1: Do not forward ISA I/O that are in the top 768 bytes of each 1K byte block address range
1	RW	0	**SERR Enable** Controls the forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary 0: Disable 1: Enable
0	RW	0	**Parity Error Response Enable** 0: Ignore the response to poisoned TLPs 1: Enable the response to poisoned TLPs

PCI Express Capability Registers (40-63h)

Offset Address: 40-41h (D3F2)

PCI Express List **Default Value: 6810h**

Bit	Attribute	Default	Description
15:8	RO	68h	**Next Pointer**
7:0	RO	10h	**Capability ID**

Offset Address: 43-42h (D3F2)

PCI Express Capabilities **Default Value: 0041h**

Bit	Attribute	Default	Description
15:14	–	0	**Reserved**
13:9	RO	0	**Interrupt Message Number**
8	RO	0	**Slot Implemented** This bit when set indicates that the PCI Express Link associated with this Port is connected to a slot (as compared to being connected to an integrated component or being disabled),
7:4	RO	0100	**Device / Port Type** 0100b: Root Port of PCI Express Root Complex
3:0	RO	1	**Capability Version**

Offset Address: 47-44h (D3F2)
Device Capabilities **Default Value: 0000 0nn1h**

Bit	Attribute	Default	Description
31:28	—	0	**Reserved**
27:26	RO	0	**Captured Slot Power Limit Scale**
25:18	RO	0	**Captured Slot Power Limit Value**
17:15	—	000	**Reserved**
14	RO	0	**Power Indicator Present**
13	RO	0	**Attention Indicator Present**
12	RO	0	**Attention Button Present**
11:9	RO	111	**Endpoint L1 Acceptable Latency** 111b: more than 64us
8:6	RO	xxx	**Endpoint L0s Acceptable Latency**
5		0	**Extended Tag Field Supported** 0: 5-bit Tag field supported 1: 8-bit Tag field supported
4:3	RO	00	**Phantom Functions Supported** Reserved
2:0	RW	001	**Max Payload Size Supported** 001b: 32QW (256 bytes)

Offset Address: 49-48h (D3F2)
Device Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15	—	0	**Reserved**
14:12	RO	000	**Max Read Request Size** 000b: 128 bytes This field sets the maximum Read Request size for the device as a Requestor.
11	RW	0	**Enable No Snoop** If this bit is set to 1, the device is **permitted** to set the No Snoop bit in the Requestor Attributes of the transactions it initiate that do not require hardware enforced cache coherency.
10	RWS	0	**Auxiliary Power PM Enable** This bit when set enables device to draw AUX power independent of PME AUX power.
9	RO	0	**Phantom Functions Enable** Not supported.
8	RO	0	**Extended Tag Field Enable** Not supported.
7:5	RW	0	**Max Payload Size** Maximum TLP payload size.
4	RW	0	**Enable Relaxed Ordering** If this bit is set to 1, the device is **permitted** to set the Relaxed Ordering bit in the Requestor Attributes of the transactions it initiate that do not require strong write ordering.
3	RW	0	**Unsupported Request Reporting Enable**
2	RW	0	**Fatal Error Reporting Enable** For a Root Port, the reporting of Fatal errors is internal to the root. No external ERR_FATAL message is generated.
1	RW	0	**Non-Fatal Error Reporting Enable** For a Root Port, the reporting of Non-Fatal errors is internal to the root. No external ERR_NONFATAL message is generated.
0	RW	0	**Correctable Error Reporting Enable** For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_COR message is generated.

Offset Address: 4B-4Ah (D3F2)
Device Status **Default Value: 0010h**

Bit	Attribute	Default	Description
15:6	—	0	**Reserved**
5	RO	0	**Transactions Pending** This bit when set indicates that the Port has issued Non-Posted Requests on its own behalf (using the Port's own Requestor ID) which have not been completed.
4	RO	1	**AUX Power Detected**
3	RW1C	0	**Unsupported Request Detected**
2	RW1C	0	**Fatal Error Detected (TL)**
1	RW1C	0	**Non-Fatal Error Detected (TL)**
0	RW1C	0	**Correctable Error Detected (TL)**

Offset Address: 4F-4Ch (D3F2)
Link Capabilities **Default Value: 0300 0C11h**

Bit	Attribute	Default	Description
31:24	RO	03h	**Port Number** This field indicates the PCI Express Port number for the given PCI Express Link.
23:18	–	0	**Reserved**
17:15	RO	000	**L1 Exit Latency** 000: less than 1us. The value reported indicates the length of time this Port requires to complete transition from L1 to L0.
14:12	RO	000	**L0s Exit Latency** 000: less than 64ns. The value reported indicates the length of time this Port requires to complete transition from L0s to L0.
11:10	RO	11	**Active State Link PM (ASPM) Support** 11b: L0s and L1 supported. This field indicates the level of ASPM supported on the PCI Express Link.
9:4	RO	01h	**Maximum Link Width** 01h: x1 Link width.
3:0	RO	1	**Maximum Link Speed** 0001b: 2.5Gb/s Link speed

Offset Address: 51-50h (D3F2)
Link Control **Default Value: 0000h**

Bit	Attribute	Default	Description	Mnemonic
15:8	–	0	**Reserved**	
7	RW	0	**Extended Synch** 0: FCU Timer limit is 30us 1: FCU Timer limit is 120us	LCES_PE2
6	RW	0	**Common Clock Configuration** 0: Indicates that this Port and the component on the opposite end of the Link are operating with asynchronous reference clock. 1: Indicates that this Port and the component on the opposite end of the Link are operating with a distributed common reference clock.	
5	RW	0	**Retrain Link** A write of 1 to this bit initiates Link retrained by directing the Physical Layer LTSSM to the Recovery state.	
4	RW	0	**Link Disable** This bit disables the Link when set to 1.	
3	RO	0	**Read Completion Boundary** 0: 64 byte	
2	–	0	**Reserved**	
1:0	RW	00	**Link Active State PM (ASPM) Control** 00b: Disabled 01b: L0s Entry Enabled 10b: L1 Entry Enabled 11b: L0s and L1 Entry Enabled	

Offset Address: 53-52h (D3F2)
Link Status **Default Value: 0nn1h**

Bit	Attribute	Default	Description
15:13	–	0	**Reserved**
12	RO	0	**Slot Clock Configuration** 0: Use an independent clock irrespective of the presence of a reference on the connector. 1: Use the same physical reference clock that the platform provides on the connector.
11	RO	0	**Link Training** This bit indicated that Link training is in progress (Physical Layer LTSSM is in Configuration or Recovery state) or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit once Link training is complete.
10	RO	0	**Training Error** Set when a Link training error occurred. Cleared by hardware upon successfully training of the Link to the L0 Link state.
9:4	RO	xxxxxx	**Negotiated Link Width** 000001: x1 000010: x2 000100: x4 001000: x8 010000: x16
3:0	RO	0001	**Link Speed** 0001: 2.5Gb/s negotiated Link speed.

Offset Address: 57-54h (D3F2)
Slot Capabilities **Default Value: 0000 0060h**

Bit	Attribute	Default	Description
31:19	RO	00h	**Physical Slot Number** Physical slot number attached to the Port.
18:17	–	0	**Reserved**
16:15	RO	0	**Slot Power Limit Scale** Write to the field causes the Port to send the Set_Slot_Power_Limit message.
14:7	RO	00h	**Slot Power Limit Value** Write to the field causes the Port to send the Set_Slot_Power_Limit message.
6	RO	1	**Hot-plug Capable**
5	RO	1	**Hot-plug Surprise**
4	RO	0	**Power Indicator Present**
3	RO	0	**Attention Indicator Present**
2	RO	0	**MRL Sensor Present**
1	RO	0	**Power Controller Present**
0	RO	0	**Attention Button Present**

Offset Address: 59-58h (D3F2)
Slot Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	–	0	**Reserved**
10	RO	0	**Power Controller Control** 0: Power On 1: Power Off
9:8	RW	0	**Power Indicator Control** 00: Reserved 01: On 10: Blink 11: Off Writes to this field cause the Port to send the appropriate POWER_INDICATOR_* Message.
7:6	RW	0	**Attention Indicator Control** 00: Reserved 01: On 10: Blink 11: Off Writes to this field cause the Port to send the appropriate ATTENTION_INDICATOR_* Message.
5	RW	0	**Hot-Plug Interrupt Enable** This bit when set enables generation of Hot-Plug interrupt on enabled Hot-Plug events.
4	RW	0	**Command Completed Interrupt Enable** This bit when set enables the generation of Hot-Plug interrupt when a command is completed by the Hot-Plug controller.
3	RW	0	**Presence Detect Changed Enable** This bit when set enables the generation of Hot-Plug interrupt or Wakeup event on a presence detect changed event.
2	RO	0	**MRL Sensor Changed Enable**
1	RO	0	**Power Fault Detected Enable**
0	RW	0	**Attention Button Pressed Enable** This bit when set enables the generation of Hot-Plug interrupt or Wakeup event on an Attention Button pressed event.

Offset Address: 5A-5Bh (D3F2)
Slot Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:7	–	0	**Reserved**
6	RO	0	**Presence Detect State** 0: Slot empty 1: Card present in slot
5	RO	0	**MRL Sensor State**
4	RW1C	0	**Command Completed**
3	RW1C	0	**Presence Detect Changed**
2	RO	0	**MRL Sensor Changed**
1	RO	0	**Power Fault Detected**
0	RW1C	0	**Attention Button Pressed**

Offset Address: 5D-5Ch (D3F2)

Root Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	–	0	**Reserved**
3	RW	0	**PME Interrupt Enable** 0: Disable 1: Enable interrupt generation upon receipt of a PME message as reflected in the PME status register bit. A PME interrupt is also generated if the PME status register bit is set when this bit is set from a cleared state.
2	RW	0	**System Error on Fatal Error Enable** 0: Disable 1: Enable generation of a System Error if a Fatal Error (ERR_FATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
1	RW	0	**System Error on Non-Fatal Error Enable** 0: Disable 1: Enable generation of a System Error if a Non-Fatal Error (ERR_NONFATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
0	RW	0	**System Error on Correctable Error Enable** 0: Disable 1: Enable generation of a System Error if a Correctable Error (ERR_COR) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.

Offset Address: 63-60h (D3F2)

Root Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	–	0	**Reserved**
17	RO	0	**PME Pending** 0: No pending PME 1: Indicates that another PME is pending when the PME Status (bit 16) is set.
16	RW1C	0	**PME Status** Indicates that the PME was asserted by the Requestor ID indicated in PME Requestor ID (bit[15:0]).
15:0	RO	00h	**PME Requestor ID** The Requestor ID of the last PME Requestor.

PCI Power Management Capability Structure Registers (68-6Fh)

Offset Address: 6B-68h (D3F2)

Power Management Capabilities **Default Value: C802 7001h**

Bit	Attribute	Default	Description
31:27	RW	11001	**PME Support** Bit 31, 30 and 27 are set to 1b (PME Message will be forwarded).
26	RW	0	**D2 Support**
25	RW	0	**D1 Support**
24:22	RO	0	**AUX Current**
21	RW	1	**Device Specific Initialization**
20:19	–	0	**Reserved**
18:16	RO	010	**Version**
15:8	RO	70h	**Next Capability Pointer**
7:0	RO	01h	**Capability ID**

Offset Address: 6F-6Ch (D3F2)
Power Management Status/Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**Power Management Data**
23:16	RO	—	**Reserved**
15	RW1CS	0	**PME Status** This bit's setting is not modified by hot, warm, or cold reset.
14:13	RO	0	**Data Scale**
12:9	RW	0	**Data Select**
8	RWS	0	**PME Enable** This bit's setting is not modified by hot, warm, or cold reset.
7:2	RO	0	**Reserved**
1:0	RW	0	**Power State**

PCI Message Signal Interrupt (MSI) Capability Structure Registers (70-87h)

Offset Address: 73-70h (D3F2)
MSI Capability Support **Default Value: 0180 0005h**

Bit	Attribute	Default	Description
31:25	—	0	**Reserved**
24	RW	1	**This MSI capability supports pre-vector masking capability**
23	RO	1	**This MSI capability supports 64 bit message address only**
22:20	RW	000	**Multiple Message Enable** 000: 1message allocated 001: 2 message allocated 010: 4 message allocated 011: 8 message allocated 100: 16 message allocated 101: 32 message allocated 11x: Reserved
19:17	RO	000	**Multiple Message Capable** 000: 1message requested 001: 2 message requested 010: 4 message allocated 011: 8 message allocated 100: 16 message requested 101: 32 message requested 11x: Reserved
16	RW	0	**MSI Enable** 0: This Port is prohibited from using MSI to request service 1: This Port is permitted to use MSI to request service.
15:8	RO	00h	**Next Capability Pointer**
7:0	RO	05h	**Capability ID**

Offset Address: 77-74h (D3F2)
System-Specified Message Address - Low **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	00h	**System-Specified Message Address Bit [31:2]**
1:0	RO	00	**System-Specified Message Address Bit [1:0]** These bits will always read as 0

Offset Address: 7B-78h (D3F2)
System-Specified Message Address - High **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	00h	**System-Specified Message Address Bit [63:36]** These bits will always read as 0 since this chip supports address up to A35.
3:0	RW	0	**System-Specified Message Address Bit [35:32]**

Offset Address: 7D-7Ch (D3F2)
Message Data **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Message Data** The message data is to be put on data [15:0] of MSI cycles

Offset Address: 83-80h (D3F2)
Message Mask Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	00h	**Mask Bit**
0	RW	0	**Mask Bit for Message 0**

Offset Address: 87-84h (D3F2)
Message Pending Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	00h	**Pending Bit**
0	RO	0	**Pending Bit for Message 0**

PCI Express Transaction Layer Registers (A0-A4h)

Offset Address: A0h (D3F2)
Downstream Control I **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Cycles Have Traffic Class TC1** 0: Disabled 1: Enabled.
6	RW	0	**Downstream Cycles Have Attribute "No Snoop" Set** 0: Disabled 1: Enabled.
5	RW	0	**Downstream Cycles Have Attribute "Relaxed Ordering" Set** 0: Disabled 1: Enabled.
4	RW	0	**Downstream Lock Cycle Support** 0: Disabled 1: Enabled.
3	RW	0	**Downstream Arbitration Scheme** 0: Fixed priority: VC1 CPL > VC0 CPL > Down Stream Command 1: Round Robin arbitration priority between VC1 CPL, VC0 CPL and Down Stream Command
2	RW	0	**Downstream Post-Write Allowed to Pass IOW** 0: Not allowed. 1: Allowed.
1	RW	0	**Downstream Post-Write Allowed to Pass Read** 0: Not allowed. 1: Allowed.
0	RW	1	**Downstream Pipeline** 0: Disabled 1: Enabled.

Offset Address: A1h (D3F2)
Downstream Control II **Default Value: 04h**

Bit	Attribute	Default	Description
7	RW1C	0	**Downstream Configuration Completion Status** 0: Normal completion. 1: At least one configuration request ended with a CRS (Configuration Request Retry Status) completion.
6:4	—	0	**Reserved**
3	RW	0	**C2P Read Completion Timer for Vector Development Mode:** When this bit is set to 1, the timer defined in RxA1[2:0] becomes: 0xx: 1us 1xx: 3us
2:0	RW	100	**C2P Read Completion Timeout Timer** 000: Reserved 001: 1ms 010: Reserved 011: 10ms (Spec. lower bound) 100: 30ms 101: 50ms (Spec. higher bound) 110: 100ms 111: Reserved

Offset Address: A4h (D3F2)
Upstream Control **Default Value: 10h**

Bit	Attribute	Default	Description
7	RW	0	**Upstream Address A35~A31 Forced to 0** 0: Disabled. 1: Enabled for system testing or loop back mode test. The upcoming data may be checked in the system memory
6	—	0	**Reserved**
5	RW	0	**Upstream Checking Malformed TLP through "Byte Enable Rule" And "Over 4K Boundary Rule"** 0: Disabled. 1: Enabled.
4	RW	1	**Downstream Read Wait Till The Upstream Write Data Flushed** 0: Disabled. 1: Enabled.
3:0	—	0	**Reserved**

PCI Express Data Link Layer Registers (B0-B6h)

Offset Address: B0h (D3F2)
Ack/Nak Latency Timer Limit **Default Value: 3Bh**

Bit	Attribute	Default	Description
7:0	RW	3Bh	**Timer Limit for Ack/Nak Latency Timer and Update FC Latency Timer (in unit of 250MHz)** 00: 4 x 1 Clocks 01: 4 x 2 Clocks 02: 4 x 3 Clocks. 0n: 4 x (n+1) Clocks FF: 4 x 256 Clocks.

Offset Address: B1h (D3F2)
Replay Timer Limit **Default Value: 59h**

Bit	Attribute	Default	Description
7:0	RW	59h	**Replay Timer Limit (In unit of 250MHz)** 00: 8 x 1 Clocks 01: 8 x 2 Clocks 02: 8 x 3 Clocks ... 0n: 8 x (n+1) Clocks FF: 8 x 256 Clocks.

Offset Address: B2h (D3F2)
FCU Control and Status **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW1C	0	**FCU Timeout Status** 1 means the FCU timeout has occurred
6	RW	1	**FCU Receive Timer Enable Control** 0: Disable the timeout mechanism 1: Enable the timeout mechanism
5	RW	0	**FCU Receive Timer Limit** 0: Timeout limit of 200us 1: Timeout limit of 300us
4	RW	0	**FCU Receive Timer Reset Control** 0: Timer reset by FCI/FCU only 1: Timer reset by any received DLLPs
3:0	—	0	**Reserved**

Offset Address: B3h (D3F2)
Replay Timer Control **Default Value: 80h**

Bit	Attribute	Default	Description
7:6	RW	10	**Replay Timer Control while Rewind** (resend those DLLPs which do not have corresponding ACK/NAK received) 00: Hold Replay Timer during rewind. 01: During rewind, if ACK/NAK comes in, reset and hold the Replay Timer. 10: During rewind, reset and hold the Replay Timer as long as the Retry Buffer is empty. 11: Reserved.
5:3	–	0	**Reserved**
2:0	RW	000	**Count of Replay Timer Expired During RXL0s** (Receiving Physical in L0s state) **Before Resend the TLP** **When Rx50[7], LCES_PE2, is set to 0:** 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 1 x Replay timer expired 010: Resend the TLP after 2 x Replay timer expired 011: Resend the TLP after 4 x Replay timer expired 100: Resend the TLP after 8 x Replay timer expired 101: Resend the TLP after 16 x Replay timer expired 110: Resend the TLP after 32 x Replay timer expired 111: Resend the TLP after 64 x Replay timer expired **When RX50[7], LCES_PE2, is set to 1:** 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 16 x Replay timer expired 010: Resend the TLP after 32 x Replay timer expired 011: Resend the TLP after 64 x Replay timer expired 100: Resend the TLP after 128 x Replay timer expired 101: Resend the TLP after 256 x Replay timer expired 110: Resend the TLP after 512 x Replay timer expired 111: Resend the TLP after 1024 x Replay timer expired

Offset Address: B4h (D3F2)
Arbitration Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	–	0	**Reserved**
3	RW	0	**TLP vs. Flow Control Initialization for VC0 in Arbitration Priority** 0: TLP is not allowed to pass FCI2 for VC0 1: TLP is allowed to pass FCI2 for VC0
2:0	RW	000	**Data Link TX Packets Arbitration Scheme** 000: Round Robin 001: Reserved. 010: Strict priority: TLP > ACK/NAK > FCU 011: Strict priority: TLP > FCU > ACK/NAK 100: Strict priority: ACK/NAK > TLP > FCU 101: Strict priority: ACK/NAK > FCU > TLP 110: Strict priority: FCU > TLP > ACK/NAK 111: Strict priority: FCU > ACK/NAK > TLP

Offset Address: B5h (D3F2)

FCU Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	–	0	**Reserved**
6	RW	0	**FCU (Flow Control Unit) Timer Control** 0: Update flow control credit when either Transaction Layer requested packets being sent or when FCU timer expired 1: Update flow control credit only when FCU timer expired
5:4	RW	00	**ACK DLLP Collapse Method** 00: Send ACK when the latency timer RACKLTLM (RxB0) expired. 01: Send ACK every 4 correct TLP has been received 10: Send ACK every 8 correct TLP has been received 11: Send ACK every 16 correct TLP has been received
3:2	–	0	**Reserved**
1	RW	0	**FCI (Flow Control Initialization) Process End Condition** 0: Complete FCI process when TLP/FCU has been received 1: Do not complete FCI process even when TLP/FCU has been received
0	RW	0	**VC1 FCI DLLP Transmission Scheme** 0: Transmit FCI DLLP only when FCI timer expired 1: Transmit FCI DLLP continuously as long as the FCI process is not finished

Offset Address: B6h (D3F2)

Transaction / Link Layer Checking Control **Default Value: 03h**

Bit	Attribute	Default	Description
7:5	–	0	**Reserved**
4	RW	0	**VC Negotiate Pending Control for VC1** 0: Assert VC negotiation pending after VC1 is enabled 1: Assert VC negotiation pending after RESET is de-asserted
3	–	0	**Reserved**
2	RW	0	**ECRC Checking Control for the Case of TD equals to1 but no ECRC field in TLP** 0: Ignore the error 1: Report error to Transaction Layer, which will mark the TLP as a Malformed TLP
1	RW	1	**Length Malform Report Control** 0: Do not report length malform to Transaction Layer 1: Report length malform to Transaction Layer
0	RW	1	**LCRC Checking Control** 0: Do not check LCRC 1: Check LCRC

PCI Express Physical Layer Registers (C0-C7h)

Offset Address: C3-C0h (D3F2)

PHY Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	–	0	**Reserved**
7	RW	0	**Quick Timeout Counter Setting** When set to 1, the following timeout will be shorter when set: TIMEOUT_2MS → TIMEOUT_4US TIMEOUT_12MS → TIMEOUT_24US TIMEOUT_24MS → TIMEOUT_48US TIMEOUT_48MS → TIMEOUT_96US TIMEOUT_1024TS → TIMEOUT_32TS
6	RW	0	**Disable Data Scrambling/Descrambling** 0: Enable 1: Disable
5:3	RW	000	**Loopback Mode Selection** 000 : No loop back 001: PHYLS loopback from TX end to RX end 010: PHYES loopback from TX end to RX end 011: Reserved 100: Reserved 101: PHYLS loopback from RX end to TX end 110: PHYES loopback from RX end to TX end 111: Reserved
2:0	–	0	**Reserved**

Offset Address: C7-C4h (D3F2)

Elastic Buffer Base Registers for Lane 0 **Default Value: 0000 0004h**

Bit	Attribute	Default	Description
31:3	–	0	**Reserved**
2:0	RW	4	**Elastic Buffer Base Register for Lane 0** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations

PCI Express Power Management Module Registers (D0-D3h)

Offset Address: D3-D0h (D3F2)

PMC Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RW	00h	**Idle Period for Entering ASL1** Minimum time period is 128ns 00: 128ns 01: 2x128ns 02: 3x128ns ... FF: 256x128ns
23:16	RW	00h	**Idle Period for Entering L0s** Minimum time period is 128ns (L0SLIM_PE2 = 00) 00: 128ns 01: 2x128ns 02: 3x128ns ... FF: 256x128ns
15	RW1C	0	**Error Status Report** This bit is set when device cannot have electrical idle after the waiting period programmed at RxD1[6:4] expired.
14	—	0	**Reserved**
13:12	RW	0	**Electrical Idle Waiting Period before Move to L1 State** (after issue ACK to the L1 request from the device). 00: Always wait for electrical idle 01: Wait 32 clock 10: Wait 64 clock 11: Reserved
11:10	—	0	**Reserved**
9:8	RW	0	**Downstream Cycles Triggered C2P Cycles, Period of Staying at L0 Before Returned to L1 for PHY** (when PMU is in non-D0 state) 00: immediately 01: 1 cfgW or message + delay10T 10: 1 32QW +1cfgW or message+ delay10T 11: 2 32QW +1 cfgW or message +delay10T
7:2	—	0	**Reserved**
1	RW	0	**Link Loopback** 0: Normal operation 1: Direct device to enter Loopback mode, receiving data in the device will be sent to the transmit side
0	RW	0	**LTSSM State During Link Reconfigure Link Width** 0: When reconfigure link width, LTSSM must be in Detect state 1: When reconfigure link width, LTSSM can be in Configuration state

PCI Express Message Controller Related Registers (D8h)

Offset Address: D8h (D3F2)

PMC Express Message Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Excessive Errors Happened Occurred But Not Reported in The MSGC** 0: Normal operation. 1: There are errors not reported to the system
6:0	—	0	**Reserved**

PCI Express Electrical PHY Registers (E1h)

Offset Address: E1h (D3F2)

PHYES Module Related Control **Default Value: 08h**

Bit	Attribute	Default	Description
7:5	—	0	**Reserved**
4	RW	0	**Receiving Polarity Change Control** 0: Have the same polarity on the loop-back/received data. 1: Have reverse polarity on the loop-back/received data.
3:2	RW	10	**Sqeulch Window Select. (64~175mv)**
1	RW	0	**Electrical Idle State Exit Condition: Number of Non Idle Signal Detected Before Exit Idle State** 0: 2 bits. 1: 10 bits.
0	RW	0	**Electrical Idle State Enter Condition: Number of Idle Signal Detected Before Enter Idle State** 0: 2 bits 1: 10 bits

Device 3 Function 2 (D3F2) – PCI Express Root Port 3 Extended Space

Registers defined in the Extended Space can be accessed through PCI Express Enhanced Configuration Access Mechanism, which utilizes a flat memory-mapped address space to access the configuration registers. Please check PCI Express Specification for the detail information.

Advanced Error Reporting Capability (100-137h)

Offset Address: 103-100h (D3F2)

Advanced Error Reporting Enhanced Capability Header **Default Value: 1401 0001h**

Bit	Attribute	Default	Description
31:20	RO	140h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	0001h	PCI Express Extended Capability ID

Offset Address: 107-104h (D3F2)

Uncorrectable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	–	0	Reserved
20	RW1CS	0	Unsupported Request Error Status (TL)
19	RW1CS	0	ECRC Error Status (TL)
18	RW1CS	0	Malformed TLP Status (TL)
17	RW1CS	0	Receiver Overflow Status (TL)
16	RW1CS	0	Unexpected Completion Status (TL)
15	RW1CS	0	Completer Abort Status (TL)
14	RW1CS	0	Completion Timeout Status (TL)
13	RW1CS	0	Flow Control Protocol Error Status (TL)
12	RW1CS	0	Poisoned TLP Status (TL)
11:5	–	0	Reserved
4	RW1CS	0	Data Link Protocol Error Status (DLL)
3:1	–	0	Reserved
0	RW1CS	0	Training Error Status (PHY)

Offset Address: 10B-108h (D3F2)

Uncorrectable Error Mask **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	–	0	Reserved
20	RWS	0	Unsupported Request Error Mask (TL)
19	RWS	0	ECRC Error Mask (TL)
18	RWS	0	Malformed TLP Mask (TL)
17	RWS	0	Receiver Overflow Mask (TL)
16	RWS	0	Unexpected Completion Mask (TL)
15	RWS	0	Completed Abort Mask (TL)
14	RWS	0	Completion Timeout Mask (TL)
13	RWS	0	Flow Control Protocol Error Mask (TL)
12	RWS	0	Poisoned TLP Mask (TL)
11:5	–	0	Reserved
4	RWS	0	Data Link Protocol Error Mask (DLL)
3:1	–	0	Reserved
0	RWS	0	Training Error Mask (PHY)

Offset Address: 10F-10Ch (D3F2)

Uncorrectable Error Severity **Default Value: 0006 0011h**

Bit	Attribute	Default	Description
31:21	—	0	Reserved
20	RWS	0	Unsupported Request Error Severity (TL)
19	RWS	0	ECRC Error Severity (TL)
18	RWS	1	Malformed TLP Severity (TL)
17	RWS	1	Receiver Overflow Error Severity (TL)
16	RWS	0	Unexpected Completion Error Severity (TL)
15	RWS	0	Completed Abort Error Severity (TL)
14	RWS	0	Completion Timeout Error Severity (TL)
13	RWS	0	Flow Control Protocol Error Severity (TL)
12	RWS	0	Poisoned TLP Severity (TL)
11:5	—	0	Reserved
4	RWS	1	Data Link Protocol Error Severity (DLL)
3:1	—	0	Reserved
0	RWS	1	Training Error Severity (PHY)

Offset Address: 113-110h (D3F2)

Correctable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:13	—	0	Reserved
12	RW1CS	0	Replay Timer Timeout Status (DLL)
11:9	—	0	Reserved
8	RW1CS	0	REPLAY_NUM Rollover Status (DLL)
7	RW1CS	0	Bad DLLP Status (DLL)
6	RW1CS	0	Bad TLP Status (DLL)
5:1	—	0	Reserved
0	RW1CS	0	Receiver Error Status (PHY)

Offset Address: 117-114h (D3F2)

Correctable Error Mask **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:13	—	0	Reserved
12	RWS	0	Replay Timer Timeout Mask (DLL)
11:9	—	0	Reserved
8	RWS	0	REPLAY_NUM Rollover Mask (DLL)
7	RWS	0	Bad DLLP Mask (DLL)
6	RWS	0	Bad TLP Mask (DLL)
5:1	—	0	Reserved
0	RWS	0	Receiver Error Mask (PHY)

Offset Address: 11B-118h (D3F2)

Advanced Error Capabilities and Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:9	—	0	Reserved
8	RWS	0	ECRC Check Enable (TL)
7	RO		ECRC Check Capable (TL)
6	RWS	0	ECRC Generation Enable (TL)
5	RO		ECRC Generation Capable (TL)
4:0	ROS		First Error Pointer (TL)

Offset Address: 12B-11Ch (D3F2)
Header Log (TL)

Register Offset Address	Attribute	Default	Description
11F - 11C	ROS	00h	**Header Log Register 1st DW**
123 - 120	ROS	00h	**Header Log Register 2nd DW**
127 - 124	ROS	00h	**Header Log Register 3rd DW**
12B – 128	ROS	00h	**Header Log Register 4th DW**

Offset Address: 12F-12Ch (D3F2)
Root Error Command **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:3	–	0	**Reserved**
2	RW	0	**Fatal Error Reporting Enable**
1	RW	0	**Non-Fatal Error Reporting Enable**
0	RW	0	**Correctable Error Reporting Enable**

Offset Address: 133-130Ch (D3F2)
Root Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	00h	**Advanced Error Interrupt Message Number (TL)**
26:7	–	0	**Reserved**
6	RW1CS	0	**Fatal Error Messages Received (TL)**
5	RW1CS	0	**Non-Fatal Error Messages Received (TL)**
4	RW1CS	0	**First Uncorrectable Fatal Error Message Received (TL)** Set to 1 when the first Uncorrectable Error Message received is for a Fatal Error
3	RW1CS	0	**Multiple ERR_FATAL/NONFATAL Received (TL)**
2	RW1CS	0	**ERR_FATAL/NONFATAL Received (TL)**
1	RW1CS	0	**Multiple ERR_COR Received (TL)**
0	RW1CS	0	**ERR_COR Received (TL)**

Offset Address: 137-134Ch (D3F2)
Error Source Identification **Default Value: 0000 0000h**

This register is updated regardless of the settings of Root Control register and the Root Error Command register

Bit	Attribute	Default	Description
31:16	ROS	0000	**ERR_FATAL/NONFATAL Source Identification (TL)**
15:0	ROS	0000	**ERR_COR Source Identification (TL)**

Virtual Channel Capability (140-14Fh)

Virtual Channel Capability is defined for Egress direction of the device. For Root Port, since only VC0 is defined, there is no implementation of VC Arbitration Table and Port Arbitration Table.

Offset Address: 143-140h (D3F2)
Virtual Channel Enhanced Capability **Default Value: 0001 0002h**

Bit	Attribute	Default	Description
31:20	RO	000h	**Next Capability Offset**
19:16	RO	1h	**Capability Version**
15:0	RO	0002h	**PCI Express Extended Capability ID**

Offset Address: 147-144h (D3F2)
Port VC Capability I **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	–	0	**Reserved**
11:10	RO	0	**Port Arbitration Table Entry Size** Reserved for root port
9:8	RO	0	**Reference Clock** Reserved for root port
7	–	0	**Reserved**
6:4	RO	0	**Low Priority Extended VC Count**
3	–	0	**Reserved**
2:0	RO	0	**Extended VC Count**

Offset Address: 14B-148h (D3F2)
Port VC Capability II **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**VC Arbitration Table Offset** 00 since only VC0 is defined
23:8	–	0	**Reserved**
7:0	RO	00h	**VC Arbitration Capability;** Reserved since Low Priority Extended Count (Rx144[6:4]) is 0.

Offset Address: 14D-14Ch (D3F2)
Port VC Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	–	0	**Reserved**
3:1	RW	0	**VC Arbitration Select**
0	RW	0	**Load VC Arbitration Table**

Offset Address: 14F-14Eh (D3F2)
Port VC Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:1	–	0	**Reserved**
0	RO	0	**VC Arbitration Table Status**

VC0 Resource (150-15Bh)

Offset Address: 153-150h (D3F2)
VC Resource Capability (VC0) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**Port Arbitration Table Offset (VC0)**
23	–	0	**Reserved**
22:16	RO	00h	**Maximum Time Slots (TL)**
15	RO	0	**Reject Snoop Transactions**
14	RO	0	**Advanced Packet Switching**
13:8	–	0	**Reserved**
7:0	RO	00h	**Port Arbitration Capability**

Offset Address: 157-154h (D3F2)

VC Resource Control (VC0) **Default Value: 8000 00FFh**

Bit	Attribute	Default	Description
31	RO	1	**VC Enable**
30:27	–	0	**Reserved**
26:24	RO	0	**VC ID**
23:20	–	0	**Reserved**
19:17	RW	0	**Port Arbitration Select**
16	RW	0	**Load Port Arbitration Table**
15:8	–	0	**Reserved**
7:0	RW Bit 0: RO	FFh	**TC/VC Mapping** This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC0 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit0 is hardwired to 1 (i.e. TC0 is always mapped to VC0).

Offset Address: 15B-158h (D3F2)

VC Resource Status (VC0) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	–	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)**
16	RO	0	**Port Arbitration Table Status**
15:0	–	0	**Reserved**

Device 3 Function 3 (D3F3) – PCI Express Root Port 4 (PCI-to-PCI Virtual Bridge)

Device 3 Function 3 is an optional 1-Lane PCI Express root port that is connected to the PCI bus through AD14 as the IDSEL. Registers listed in this section are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 3 and function number 3.

Header Registers (0-3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	**Vendor ID**
3 – 2h	RO	F238h	**Device ID**

Offset Address: 5-4h (D3F3)
Command Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	–	0	**Reserved**
10	RW	0	**Interrupt Disabled** Set when the device is prevented from generating INTx messages
9	–	0	**Reserved**
8	RW	0	**SERR# Enable** 0: Disable error report 1: Enable reporting of non-fatal and fatal errors
7	–	0	**Reserved**
6	RW	0	**Parity Error Response** 0: Ignore parity errors & continue 1: Take normal action on detected parity errors
5:3	–	0	**Reserved**
2	RW	0	**Bus Master Enable** 0: Disable 1: Enable Controls the ability to forward Memory and I/O Read/Write requests in the upstream direction. Disabling this bit disables MSI messages.
1	RW	0	**Memory Space** 0: Ignore downstream memory transactions; memory cycles with address falling in the claimed range will be forwarded to the SB 1: Enable downstream memory cycle to this port if its address falling in the claimed range of this device.
0	RW	0	**I/O Space** 0: Ignore downstream I/O transactions; I/O cycles with address falling in the claimed range will be forwarded to the SB. 1: Enable downstream I/O cycle to this port if its address falling in the claimed range of this device.

Offset Address: 7-6h (D3F3)
Status Register **Default Value: 0010h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set whenever a poisoned TLP is received, regardless the state of Parity Error Enabled (Rx4[6])
14	RW1C	0	**Signaled System Error** This bit is set when: 5. A device sends an ERR_FATAL or ERR_NONFATAL message 6. Rx4[8] = 1
13	RW1C	0	**Received Master Abort** This bit is set when receiving a completion with Unsupported Request Completion Status
12	RW1C	0	**Received Target Abort** This bit is set when receiving a completion with Completer Abort Completion Status
11	RW1C	0	**Signaled Target Abort** This bit is set when completing a Request with Completer Abort Completion Status
10:9	–	0	**Reserved (Always 0)**
8	RW1C	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx4[6]) is set and either one of the following two conditions occurs: 5. Requestor receives a Completion marked poisoned 6. Requestor poisons a write Request
7:5	–	0	**Reserved**
4	RO	1	**Capabilities List** Indicates the presence of an extended capability list item. Always set to 1 for PCI Express device
3	RO	0	**Interrupt Status** Indicate an INTx message is pending internally (TL)
2:0	–	0	**Reserved**

Offset Address: 8h (D3F3)
Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	Revision Code

Offset Address: 0B-9h (D3F3)
Class Code **Default Value: 060400h**

Bit	Attribute	Default	Description
23:0	RO	060400h	Class Code

Offset Address: 0Ch (D3F3)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00	Cache Line Size – Reserved (No impact on functionality)

Offset Address: 0Dh (D3F3)
Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00	Reserved (Hardwired to 0)

Offset Address: 0Eh (D3F3)
Header Type **Default Value: 81h**

Bit	Attribute	Default	Description
7:0	RO	01h	Header Type Code A multiple function device.

Offset Address: 0Fh (D3F3)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	BIST Support

Offset Address: 17-10h (D3F3)
Base Address Register **Default Value: 00h**

Bit	Attribute	Default	Description
63:0	–	00h	Reserved

Offset Address: 18h (D3F3)
Primary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	Primary Bus Number

Offset Address: 19h (D3F3)
Secondary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	Secondary Bus Number

Offset Address: 1Ah (D3F3)
Subordinate Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Subordinate Bus Number**

Offset Address: 1Ch (D3F3)
I/O Base **Default Value: F0h**

Bit	Attribute	Default	Description
7:4	RW	1111	**I/O Base (AD[15:12] - inclusive)** This bridge will forward the cycles from primary side to PCI if the IO address AD[15:12] is between IO base and IO limit (Rx1D)
3:0	RO	0	**I/O Addressing Capability** 0 means IO addressing is 16-bit only.

Offset Address: 1Dh (D3F3)
I/O Limit **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**I/O Limit (AD[15:12] - inclusive)**
3:0	RO	0	**I/O Addressing Capability** 0 means IO addressing is 16-bit only.

Offset Address: 1F-1Eh (D3F3)
Secondary Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set when secondary side receives a poisoned TLP regardless of Rx4[6]
14	RW1C	0	**Received System Error** This bit is set when Rx4[8] is 1 and a device sends an ERR_FATAL or ERR_NONFATAL message.
13	RW1C	0	**Received Master Abort**
12	RW1C	0	**Received Target Abort**
11	RW1C	0	**Signaled Target Abort**
10:9	–	0	**Reserved**
8	RW1C	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx4[6]) is set and either one of the following two conditions occurs: 1. Requestor receives a Completion marked poisoned. 2. Requestor poisons a write Request
7:0	–	0	**Reserved**

Offset Address: 21-20h (D3F3)
Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Memory Base (AD[31:20] – inclusive)** The address [19:0] is not decoded.
3:0	RO	0000	**Reserved**

Offset Address: 23-22h (D3F3)
Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	000h	**Memory Limit (AD[31:20] – inclusive)** The address [19:0] is not decoded.
3:0	RO	0000	**Reserved**

Offset Address: 25-24h (D3F3)
Prefetchable Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Prefetchable Memory Base AD[31:20]**
3:0	RO	0000	**Reserved**

Offset Address: 27-26h (D3F3)
Prefetchable Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	000h	**Prefetchable Memory Limit AD[31:20]**
3:0	RO	0000	**Reserved**

Offset Address: 2B-28h (D3F3)
Prefetchable Memory Upper Base **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	00h	**Reserved**
3:0	RW	0000	**AD[35:32]** This chip supports up to 16G

Offset Address: 2F-2Ch (D3F3)
Prefetchable Memory Upper Limit **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	00h	**Reserved**
3:0	RW	0000	**AD[35:32]** This chip supports up to 16G

Offset Address: 31-30h (D3F3)
I/O Base Upper **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	00h	**I/O Base Upper 16 bits Address**

Offset Address: 33-32h (D3F3)
I/O Base Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	00h	**I/O Limit Upper 16 bits Address**

Offset Address: 34h (D3F3)
Capability Pointer **Default Value: 40h**

Contains an offset from the start of configuration space.

Bit	Attribute	Default	Description
7:0	RO	40h	**Capability Pointer** Always reads 40h. Capability Pointer link list: Rx34 → Rx40 → Rx68 → NULL

Offset Address: 3Ch (D3F3)
Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**INT Line (For Software Use Only)**

Offset Address: 3Dh (D3F3)
Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**INT Pin** 01: INTA

Offset Address: 3F-3Eh (D3F3)

Bridge Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:7	—	00h	**Reserved**
6	RW	0	**Secondary Bus Reset** 0: No reset 1: Triggers a warm reset on the corresponding PCI Express Port
5	—	0	**Reserved**
4	RW	0	**Base VGA 16 bits Decode** 0: All VGA alias range will be forwarded 1: Only forward base VGA range (Aliased range will not be forwarded)
3	RW	0	**VGA Compatible I/O and Memory Address Range** 0: Do not forward VGA compatible memory and I/O 1: Forward VGA compatible memory and I/O Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.
2	RW	0	**Block/Forward ISA I/O Cycles** 0: Forward all I/O cycles with address in the range defined by the I/O Base and I/O Limit 1: Do not forward ISA I/O that are in the top 768 bytes of each 1K byte block address range
1	RW	0	**SERR Enable** Controls the forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary 0: Disable 1: Enable
0	RW	0	**Parity Error Response Enable** 0: Ignore the response to poisoned TLPs 1: Enable the response to poisoned TLPs

PCI Express Capability Registers (40-63h)

Offset Address: 40-41h (D3F3)

PCI Express List **Default Value: 6810h**

Bit	Attribute	Default	Description
15:8	RO	68h	**Next Pointer**
7:0	RO	10h	**Capability ID**

Offset Address: 43-42h (D3F3)

PCI Express Capabilities **Default Value: 0041h**

Bit	Attribute	Default	Description
15:14	—	0	**Reserved**
13:9	RO	0	**Interrupt Message Number**
8	RO	0	**Slot Implemented** This bit when set indicates that the PCI Express Link associated with this Port is connected to a slot (as compared to being connected to an integrated component or being disabled),
7:4	RO	0100	**Device / Port Type** 0100b: Root Port of PCI Express Root Complex
3:0	RO	1	**Capability Version**

Offset Address: 47-44h (D3F3)

Device Capabilities **Default Value: 0000 0nn1h**

Bit	Attribute	Default	Description
31:28	—	0	**Reserved**
27:26	RO	0	**Captured Slot Power Limit Scale**
25:18	RO	0	**Captured Slot Power Limit Value**
17:15	—	000	**Reserved**
14	RO	0	**Power Indicator Present**
13	RO	0	**Attention Indicator Present**
12	RO	0	**Attention Button Present**
11:9	RO	111	**Endpoint L1 Acceptable Latency** 111b: more than 64us
8:6	RO	xxx	**Endpoint L0s Acceptable Latency**
5		0	**Extended Tag Field Supported** 0: 5-bit Tag field supported 1: 8-bit Tag field supported
4:3	RO	00	**Phantom Functions Supported** Reserved
2:0	RW	001	**Max Payload Size Supported** 001b: 32QW (256 bytes)

Offset Address: 49-48h (D3F3)

Device Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15	—	0	**Reserved**
14:12	RO	000	**Max Read Request Size** 000b: 128 bytes This field sets the maximum Read Request size for the device as a Requestor.
11	RW	0	**Enable No Snoop** If this bit is set to 1, the device is **permitted** to set the No Snoop bit in the Requestor Attributes of the transactions it initiate that do not require hardware enforced cache coherency.
10	RWS	0	**Auxiliary Power PM Enable** This bit when set enables device to draw AUX power independent of PME AUX power.
9	RO	0	**Phantom Functions Enable** Not supported.
8	RO	0	**Extended Tag Field Enable** Not supported.
7:5	RW	0	**Max Payload Size** Maximum TLP payload size.
4	RW	0	**Enable Relaxed Ordering** If this bit is set to 1, the device is **permitted** to set the Relaxed Ordering bit in the Requestor Attributes of the transactions it initiate that do not require strong write ordering.
3	RW	0	**Unsupported Request Reporting Enable**
2	RW	0	**Fatal Error Reporting Enable** For a Root Port, the reporting of Fatal errors is internal to the root. No external ERR_FATAL message is generated.
1	RW	0	**Non-Fatal Error Reporting Enable** For a Root Port, the reporting of Non-Fatal errors is internal to the root. No external ERR_NONFATAL message is generated.
0	RW	0	**Correctable Error Reporting Enable** For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_COR message is generated.

Offset Address: 4B-4Ah (D3F3)

Device Status **Default Value: 0010h**

Bit	Attribute	Default	Description
15:6	—	0	**Reserved**
5	RO	0	**Transactions Pending** This bit when set indicates that the Port has issued Non-Posted Requests on its own behalf (using the Port's own Requestor ID) which have not been completed.
4	RO	1	**AUX Power Detected**
3	RW1C	0	**Unsupported Request Detected**
2	RW1C	0	**Fatal Error Detected (TL)**
1	RW1C	0	**Non-Fatal Error Detected (TL)**
0	RW1C	0	**Correctable Error Detected (TL)**

Offset Address: 4F-4Ch (D3F3)

Link Capabilities **Default Value: 0300 0C11h**

Bit	Attribute	Default	Description
31:24	RO	04h	**Port Number** This field indicates the PCI Express Port number for the given PCI Express Link.
23:18	–	0	**Reserved**
17:15	RO	000	**L1 Exit Latency** 000: less than 1us. The value reported indicates the length of time this Port requires to complete transition from L1 to L0.
14:12	RO	000	**L0s Exit Latency** 000: less than 64ns. The value reported indicates the length of time this Port requires to complete transition from L0s to L0.
11:10	RO	11	**Active State Link PM (ASPM) Support** 11b: L0s and L1 supported. This field indicates the level of ASPM supported on the PCI Express Link.
9:4	RO	01h	**Maximum Link Width** 01h: x1 Link width.
3:0	RO	1	**Maximum Link Speed** 0001b: 2.5Gb/s Link speed

Offset Address: 51-50h (D3F3)

Link Control **Default Value: 0000h**

Bit	Attribute	Default	Description	Mnemonic
15:8	–	0	**Reserved**	
7	RW	0	**Extended Synch** 0: FCU Timer limit is 30us 1: FCU Timer limit is 120us	LCES_PE2
6	RW	0	**Common Clock Configuration** 0: Indicates that this Port and the component on the opposite end of the Link are operating with asynchronous reference clock. 1: Indicates that this Port and the component on the opposite end of the Link are operating with a distributed common reference clock.	
5	RW	0	**Retrain Link** A write of 1 to this bit initiates Link retrained by directing the Physical Layer LTSSM to the Recovery state.	
4	RW	0	**Link Disable** This bit disables the Link when set to 1.	
3	RO	0	**Read Completion Boundary** 0: 64 byte	
2	–	0	**Reserved**	
1:0	RW	00	**Link Active State PM (ASPM) Control** 00b: Disabled 01b: L0s Entry Enabled 10b: L1 Entry Enabled 11b: L0s and L1 Entry Enabled	

Offset Address: 53-52h (D3F3)

Link Status **Default Value: 0nn1h**

Bit	Attribute	Default	Description
15:13	–	0	**Reserved**
12	RO	0	**Slot Clock Configuration** 0: Use an independent clock irrespective of the presence of a reference on the connector. 1: Use the same physical reference clock that the platform provides on the connector.
11	RO	0	**Link Training** This bit indicated that Link training is in progress (Physical Layer LTSSM is in Configuration or Recovery state) or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit once Link training is complete.
10	RO	0	**Training Error** Set when a Link training error occurred. Cleared by hardware upon successfully training of the Link to the L0 Link state.
9:4	RO	xxxxxx	**Negotiated Link Width** 000001: x1 000010: x2 000100: x4 001000: x8 010000: x16
3:0	RO	0001	**Link Speed** 0001: 2.5Gb/s negotiated Link speed.

Offset Address: 57-54h (D3F3)

Slot Capabilities **Default Value: 0000 0060h**

Bit	Attribute	Default	Description
31:19	RO	00h	**Physical Slot Number** Physical slot number attached to the Port.
18:17	–	0	**Reserved**
16:15	RO	0	**Slot Power Limit Scale** Write to the field causes the Port to send the Set_Slot_Power_Limit message.
14:7	RO	00h	**Slot Power Limit Value** Write to the field causes the Port to send the Set_Slot_Power_Limit message.
6	RO	1	**Hot-plug Capable**
5	RO	1	**Hot-plug Surprise**
4	RO	0	**Power Indicator Present**
3	RO	0	**Attention Indicator Present**
2	RO	0	**MRL Sensor Present**
1	RO	0	**Power Controller Present**
0	RO	0	**Attention Button Present**

Offset Address: 59-58h (D3F3)

Slot Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	–	0	**Reserved**
10	RO	0	**Power Controller Control** 0: Power On 1: Power Off
9:8	RW	0	**Power Indicator Control** 00: Reserved 01: On 10: Blink 11: Off Writes to this field cause the Port to send the appropriate POWER_INDICATOR_* Message.
7:6	RW	0	**Attention Indicator Control** 00: Reserved 01: On 10: Blink 11: Off Writes to this field cause the Port to send the appropriate ATTENTION_INDICATOR_* Message.
5	RW	0	**Hot-Plug Interrupt Enable** This bit when set enables generation of Hot-Plug interrupt on enabled Hot-Plug events.
4	RW	0	**Command Completed Interrupt Enable** This bit when set enables the generation of Hot-Plug interrupt when a command is completed by the Hot-Plug controller.
3	RW	0	**Presence Detect Changed Enable** This bit when set enables the generation of Hot-Plug interrupt or Wakeup event on a presence detect changed event.
2	RO	0	**MRL Sensor Changed Enable**
1	RO	0	**Power Fault Detected Enable**
0	RW	0	**Attention Button Pressed Enable** This bit when set enables the generation of Hot-Plug interrupt or Wakeup event on an Attention Button pressed event.

Offset Address: 5A-5Bh (D3F3)

Slot Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:7	–	0	**Reserved**
6	RO	0	**Presence Detect State** 0: Slot empty 1: Card present in slot
5	RO	0	**MRL Sensor State**
4	RW1C	0	**Command Completed**
3	RW1C	0	**Presence Detect Changed**
2	RO	0	**MRL Sensor Changed**
1	RO	0	**Power Fault Detected**
0	RW1C	0	**Attention Button Pressed**

Offset Address: 5D-5Ch (D3F3)

Root Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	—	0	**Reserved**
3	RW	0	**PME Interrupt Enable** 0: Disable 1: Enable interrupt generation upon receipt of a PME message as reflected in the PME status register bit. A PME interrupt is also generated if the PME status register bit is set when this bit is set from a cleared state.
2	RW	0	**System Error on Fatal Error Enable** 0: Disable 1: Enable generation of a System Error if a Fatal Error (ERR_FATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
1	RW	0	**System Error on Non-Fatal Error Enable** 0: Disable 1: Enable generation of a System Error if a Non-Fatal Error (ERR_NONFATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
0	RW	0	**System Error on Correctable Error Enable** 0: Disable 1: Enable generation of a System Error if a Correctable Error (ERR_COR) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.

Offset Address: 63-60h (D3F3)

Root Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	—	0	**Reserved**
17	RO	0	**PME Pending** 0: No pending PME 1: Indicates that another PME is pending when the PME Status (bit 16) is set.
16	RW1C	0	**PME Status** Indicates that the PME was asserted by the Requestor ID indicated in PME Requestor ID (bit[15:0]).
15:0	RO	00h	**PME Requestor ID** The Requestor ID of the last PME Requestor.

PCI Power Management Capability Structure Registers (68-6Fh)

Offset Address: 6B-68h (D3F3)

Power Management Capabilities **Default Value: C802 7001h**

Bit	Attribute	Default	Description
31:27	RW	11001	**PME Support** Bit 31, 30 and 27 are set to 1b (PME Message will be forwarded).
26	RW	0	**D2 Support**
25	RW	0	**D1 Support**
24:22	RO	0	**AUX Current**
21	RW	1	**Device Specific Initialization**
20:19	—	0	**Reserved**
18:16	RO	010	**Version**
15:8	RO	70h	**Next Capability Pointer**
7:0	RO	01h	**Capability ID**

Offset Address: 6F-6Ch (D3F3)
Power Management Status/Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**Power Management Data**
23:16	RO	–	**Reserved**
15	RW1CS	0	**PME Status** This bit's setting is not modified by hot, warm, or cold reset.
14:13	RO	0	**Data Scale**
12:9	RW	0	**Data Select**
8	RWS	0	**PME Enable** This bit's setting is not modified by hot, warm, or cold reset.
7:2	RO	0	**Reserved**
1:0	RW	0	**Power State**

PCI Message Signal Interrupt (MSI) Capability Structure Registers (70-87h)

Offset Address: 73-70h (D3F3)
MSI Capability Support **Default Value: 0180 0005h**

Bit	Attribute	Default	Description
31:25	–	0	**Reserved**
24	RW	1	**This MSI capability supports pre-vector masking capability**
23	RO	1	**This MSI capability supports 64 bit message address only**
22:20	RW	000	**Multiple Message Enable** 000: 1message allocated 001: 2 message allocated 010: 4 message allocated 011: 8 message allocated 100: 16 message allocated 101: 32 message allocated 11x: Reserved
19:17	RO	000	**Multiple Message Capable** 000: 1message requested 001: 2 message requested 010: 4 message allocated 011: 8 message allocated 100: 16 message requested 101: 32 message requested 11x: Reserved
16	RW	0	**MSI Enable** 0: This Port is prohibited from using MSI to request service 1: This Port is permitted to use MSI to request service.
15:8	RO	00h	**Next Capability Pointer**
7:0	RO	05h	**Capability ID**

Offset Address: 77-74h (D3F3)
System-Specified Message Address - Low **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	00h	**System-Specified Message Address Bit [31:2]**
1:0	RO	00	**System-Specified Message Address Bit [1:0]** These bits will always read as 0

Offset Address: 7B-78h (D3F3)
System-Specified Message Address - High **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	00h	**System-Specified Message Address Bit [63:36]** These bits will always read as 0 since this chip supports address up to A35.
3:0	RW	0	**System-Specified Message Address Bit [35:32]**

Offset Address: 7D-7Ch (D3F3)
Message Data **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Message Data** The message data is to be put on data [15:0] of MSI cycles

Offset Address: 83-80h (D3F3)
Message Mask Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	00h	**Mask Bit**
0	RW	0	**Mask Bit for Message 0**

Offset Address: 87-84h (D3F3)
Message Pending Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	00h	**Pending Bit**
0	RO	0	**Pending Bit for Message 0**

PCI Express Transaction Layer Registers (A0-A4h)

Offset Address: A0h (D3F3)
Downstream Control I **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Cycles Have Traffic Class TC1** 0: Disabled 1: Enabled.
6	RW	0	**Downstream Cycles Have Attribute "No Snoop" Set** 0: Disabled 1: Enabled.
5	RW	0	**Downstream Cycles Have Attribute "Relaxed Ordering" Set** 0: Disabled 1: Enabled.
4	RW	0	**Downstream Lock Cycle Support** 0: Disabled 1: Enabled.
3	RW	0	**Downstream Arbitration Scheme** 0: Fixed priority: VC1 CPL > VC0 CPL > Down Stream Command 1: Round Robin arbitration priority between VC1 CPL, VC0 CPL and Down Stream Command
2	RW	0	**Downstream Post-Write Allowed to Pass IOW** 0: Not allowed. 1: Allowed.
1	RW	0	**Downstream Post-Write Allowed to Pass Read** 0: Not allowed. 1: Allowed.
0	RW	1	**Downstream Pipeline** 0: Disabled 1: Enabled.

Offset Address: A1h (D3F3)
Downstream Control II **Default Value: 04h**

Bit	Attribute	Default	Description
7	RW1C	0	**Downstream Configuration Completion Status** 0: Normal completion. 1: At least one configuration request ended with a CRS (Configuration Request Retry Status) completion.
6:4	—	0	**Reserved**
3	RW	0	**C2P Read Completion Timer for Vector Development Mode:** When this bit is set to 1, the timer defined in RxA1[2:0] becomes: 0xx: 1us 1xx: 3us
2:0	RW	100	**C2P Read Completion Timeout Timer** 000: Reserved 001: 1ms 010: Reserved 011: 10ms (Spec. lower bound) 100: 30ms 101: 50ms (Spec. higher bound) 110: 100ms 111: Reserved

Offset Address: A4h (D3F3)
Upstream Control **Default Value: 10h**

Bit	Attribute	Default	Description
7	RW	0	**Upstream Address A35~A31 Forced to 0** 0: Disabled. 1: Enabled for system testing or loop back mode test. The upcoming data may be checked in the system memory
6	–	0	**Reserved**
5	RW	0	**Upstream Checking Malformed TLP through "Byte Enable Rule" And "Over 4K Boundary Rule"** 0: Disabled. 1: Enabled.
4	RW	1	**Downstream Read Wait Till The Upstream Write Data Flushed** 0: Disabled. 1: Enabled.
3:0	–	0	**Reserved**

PCI Express Data Link Layer Registers (B0-B6h)

Offset Address: B0h (D3F3)
Ack/Nak Latency Timer Limit **Default Value: 3Bh**

Bit	Attribute	Default	Description
7:0	RW	3Bh	**Timer Limit for Ack/Nak Latency Timer and Update FC Latency Timer (in unit of 250MHz)** 00: 4 x 1 Clocks 01: 4 x 2 Clocks 02: 4 x 3 Clocks. 0n: 4 x (n+1) Clocks FF: 4 x 256 Clocks.

Offset Address: B1h (D3F3)
Replay Timer Limit **Default Value: 59h**

Bit	Attribute	Default	Description
7:0	RW	59h	**Replay Timer Limit (In unit of 250MHz)** 00: 8 x 1 Clocks 01: 8 x 2 Clocks 02: 8 x 3 Clocks 0n: 8 x (n+1) Clocks FF: 8 x 256 Clocks.

Offset Address: B2h (D3F3)
FCU Control and Status **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW1C	0	**FCU Timeout Status** 1 means the FCU timeout has occurred
6	RW	1	**FCU Receive Timer Enable Control** 0: Disable the timeout mechanism 1: Enable the timeout mechanism
5	RW	0	**FCU Receive Timer Limit** 0: Timeout limit of 200us 1: Timeout limit of 300us
4	RW	0	**FCU Receive Timer Reset Control** 0: Timer reset by FCI/FCU only 1: Timer reset by any received DLLPs
3:0	–	0	**Reserved**

Offset Address: B3h (D3F3)

Replay Timer Control **Default Value: 10h**

Bit	Attribute	Default	Description
7:6	RW	10	**Replay Timer Control while Rewind** (resend those DLLPs which do not have corresponding ACK/NAK received) 00: Hold Replay Timer during rewind. 01: During rewind, if ACK/NAK comes in, reset and hold the Replay Timer. 10: During rewind, reset and hold the Replay Timer as long as the Retry Buffer is empty. 11: Reserved.
5:3	–	0	**Reserved**
2:0	RW	000	**Count of Replay Timer Expired During RXL0s** (Receiving Physical in L0s state) **Before Resend the TLP** **When Rx50[7], LCES_PE3, is set to 0:** 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 1 x Replay timer expired 010: Resend the TLP after 2 x Replay timer expired 011: Resend the TLP after 4 x Replay timer expired 100: Resend the TLP after 8 x Replay timer expired 101: Resend the TLP after 16 x Replay timer expired 110: Resend the TLP after 32 x Replay timer expired 111: Resend the TLP after 64 x Replay timer expired **When RX50[7], LCES_PE3, is set to 1:** 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 16 x Replay timer expired 010: Resend the TLP after 32 x Replay timer expired 011: Resend the TLP after 64 x Replay timer expired 100: Resend the TLP after 128 x Replay timer expired 101: Resend the TLP after 256 x Replay timer expired 110: Resend the TLP after 512 x Replay timer expired 111: Resend the TLP after 1024 x Replay timer expired

Offset Address: B4h (D3F3)

Arbitration Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	–	0	**Reserved**
3	RW	0	**TLP vs. Flow Control Initialization for VC0 in Arbitration Priority** 0: TLP is not allowed to pass FCI2 for VC0 1: TLP is allowed to pass FCI2 for VC0
2:0	RW	000	**Data Link TX Packets Arbitration Scheme** 000: Round Robin 001: Reserved. 010: Strict priority: TLP > ACK/NAK > FCU 011: Strict priority: TLP > FCU > ACK/NAK 100: Strict priority: ACK/NAK > TLP > FCU 101: Strict priority: ACK/NAK > FCU > TLP 110: Strict priority: FCU > TLP > ACK/NAK 111: Strict priority: FCU > ACK/NAK > TLP

Offset Address: B5h (D3F3)

FCU Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	–	0	**Reserved**
6	RW	0	**FCU (Flow Control Unit) Timer Control** 0: Update flow control credit when either Transaction Layer requested packets being sent or when FCU timer expired 1: Update flow control credit only when FCU timer expired
5:4	RW	00	**ACK DLLP Collapse Method** 00: Send ACK when the latency timer RACKLTLM (RxB0) expired. 01: Send ACK every 4 correct TLP has been received 10: Send ACK every 8 correct TLP has been received 11: Send ACK every 16 correct TLP has been received
3:2	–	0	**Reserved**
1	RW	0	**FCI (Flow Control Initialization) Process End Condition** 0: Complete FCI process when TLP/FCU has been received 1: Do not complete FCI process even when TLP/FCU has been received
0	RW	0	**VC1 FCI DLLP Transmission Scheme** 0: Transmit FCI DLLP only when FCI timer expired 1: Transmit FCI DLLP continuously as long as the FCI process is not finished

Offset Address: B6h (D3F3)

Transaction / Link Layer Checking Control **Default Value: 03h**

Bit	Attribute	Default	Description
7:5	–	0	**Reserved**
4	RW	0	**VC Negotiate Pending Control for VC1** 0: Assert VC negotiation pending after VC1 is enabled 1: Assert VC negotiation pending after RESET is de-asserted
3	–	0	**Reserved**
2	RW	0	**ECRC Checking Control for the Case of TD equals to1 but no ECRC field in TLP** 0: Ignore the error 1: Report error to Transaction Layer, which will mark the TLP as a Malformed TLP
1	RW	1	**Length Malform Report Control** 0: Do not report length malform to Transaction Layer 1: Report length malform to Transaction Layer
0	RW	1	**LCRC Checking Control** 0: Do not check LCRC 1: Check LCRC

PCI Express Physical Layer Registers (C0-C7h)

Offset Address: C3-C0h (D3F3)

PHY Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	—	0	**Reserved**
7	RW	0	**Quick Timeout Counter Setting** When set to 1, the following timeout will be shorter when set: TIMEOUT_2MS → TIMEOUT_4US TIMEOUT_12MS → TIMEOUT_24US TIMEOUT_24MS → TIMEOUT_48US TIMEOUT_48MS → TIMEOUT_96US TIMEOUT_1024TS → TIMEOUT_32TS
6	RW	0	**Disable Data Scrambling/Descrambling** 0: Enable 1: Disable
5:3	RW	000	**Loopback Mode Selection** 000 : No loop back 001: PHYLS loopback from TX end to RX end 010: PHYES loopback from TX end to RX end 011: Reserved 100: Reserved 101: PHYLS loopback from RX end to TX end 110: PHYES loopback from RX end to TX end 111: Reserved
2:0	—	0	**Reserved**

Offset Address: C7-C4h (D3F3)

Elastic Buffer Base Registers for Lane 0 **Default Value: 0000 0004h**

Bit	Attribute	Default	Description
31:3	—	0	**Reserved**
2:0	RW	4	**Elastic Buffer Base Register for Lane 0** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations

PCI Express Power Management Module Registers (D0-D3h)

Offset Address: D3-D0h (D3F3)

PMC Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RW	00h	**Idle Period for Entering ASL1** Minimum time period is 128ns 00: 128ns 01: 2x128ns 02: 3x128ns ... FF: 256x128ns
23:16	RW	00h	**Idle Period for Entering L0s** Minimum time period is 128ns (L0SLIM_PE3 = 00) 00: 128ns 01: 2x128ns 02: 3x128ns ... FF: 256x128ns
15	RW1C	0	**Error Status Report** This bit is set when device cannot have electrical idle after the waiting period programmed at RxD1[6:4] expired.
14	–	0	**Reserved**
13:12	RW	0	**Electrical Idle Waiting Period before Move to L1 State** (after issue ACK to the L1 request from the device). 00: Always wait for electrical idle 01: Wait 32 clock 10: Wait 64 clock 11: Reserved
11:10	–	0	**Reserved**
9:8	RW	0	**Downstream Cycles Triggered C2P Cycles, Period of Staying at L0 Before Returned to L1 for PHY** (when PMU is in non-D0 state) 00: immediately 01: 1 cfgW or message + delay10T 10: 1 32QW +1cfgW or message+ delay10T 11: 2 32QW +1 cfgW or message +delay10T
7:2	–	0	**Reserved**
1	RW	0	**Link Loopback** 0: Normal operation 1: Direct device to enter Loopback mode, receiving data in the device will be sent to the transmit side
0	RW	0	**LTSSM State During Link Reconfigure Link Width** 0: When reconfigure link width, LTSSM must be in Detect state 1: When reconfigure link width, LTSSM can be in Configuration state

PCI Express Message Controller Related Registers (D8h)

Offset Address: D8h (D3F3)

PMC Express Message Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Excessive Errors Happened Occurred But Not Reported in The MSGC** 0: Normal operation. 1: There are errors not reported to the system
6:0	—	0	**Reserved**

PCI Express Electrical PHY Registers (E1h)

Offset Address: E1h (D3F3)

PHYES Module Related Control **Default Value: 08h**

Bit	Attribute	Default	Description
7:5	—	0	**Reserved**
4	RW	0	**Receiving Polarity Change Control** 0: Have the same polarity on the loop-back/received data. 1: Have reverse polarity on the loop-back/received data.
3:2	RW	10	**Sqeulch Window Select. (64~175mv)**
1	RW	0	**Electrical Idle State Exit Condition: Number of Non Idle Signal Detected Before Exit Idle State** 0: 2 bits. 1: 10 bits.
0	RW	0	**Electrical Idle State Enter Condition: Number of Idle Signal Detected Before Enter Idle State** 0: 2 bits 1: 10 bits

Device 3 Function 3 (D3F3) – PCI Express Root Port 4 Extended Space

Registers defined in the Extended Space can be accessed through PCI Express Enhanced Configuration Access Mechanism, which utilizes a flat memory-mapped address space to access the configuration registers. Please check PCI Express Specification for the detail information.

Advanced Error Reporting Capability (100-137h)

Offset Address: 103-100h (D3F3)

Advanced Error Reporting Enhanced Capability Header **Default Value: 1401 0001h**

Bit	Attribute	Default	Description
31:20	RO	140h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	0001h	PCI Express Extended Capability ID

Offset Address: 107-104h (D3F3)

Uncorrectable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	–	0	Reserved
20	RW1CS	0	Unsupported Request Error Status (TL)
19	RW1CS	0	ECRC Error Status (TL)
18	RW1CS	0	Malformed TLP Status (TL)
17	RW1CS	0	Receiver Overflow Status (TL)
16	RW1CS	0	Unexpected Completion Status (TL)
15	RW1CS	0	Completer Abort Status (TL)
14	RW1CS	0	Completion Timeout Status (TL)
13	RW1CS	0	Flow Control Protocol Error Status (TL)
12	RW1CS	0	Poisoned TLP Status (TL)
11:5	–	0	Reserved
4	RW1CS	0	Data Link Protocol Error Status (DLL)
3:1	–	0	Reserved
0	RW1CS	0	Training Error Status (PHY)

Offset Address: 10B-108h (D3F3)

Uncorrectable Error Mask **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	–	0	Reserved
20	RWS	0	Unsupported Request Error Mask (TL)
19	RWS	0	ECRC Error Mask (TL)
18	RWS	0	Malformed TLP Mask (TL)
17	RWS	0	Receiver Overflow Mask (TL)
16	RWS	0	Unexpected Completion Mask (TL)
15	RWS	0	Completed Abort Mask (TL)
14	RWS	0	Completion Timeout Mask (TL)
13	RWS	0	Flow Control Protocol Error Mask (TL)
12	RWS	0	Poisoned TLP Mask (TL)
11:5	–	0	Reserved
4	RWS	0	Data Link Protocol Error Mask (DLL)
3:1	–	0	Reserved
0	RWS	0	Training Error Mask (PHY)

Offset Address: 10F-10Ch (D3F3)

Uncorrectable Error Severity **Default Value: 0006 0011h**

Bit	Attribute	Default	Description
31:21	—	0	Reserved
20	RWS	0	Unsupported Request Error Severity (TL)
19	RWS	0	ECRC Error Severity (TL)
18	RWS	1	Malformed TLP Severity (TL)
17	RWS	1	Receiver Overflow Error Severity (TL)
16	RWS	0	Unexpected Completion Error Severity (TL)
15	RWS	0	Completed Abort Error Severity (TL)
14	RWS	0	Completion Timeout Error Severity (TL)
13	RWS	0	Flow Control Protocol Error Severity (TL)
12	RWS	0	Poisoned TLP Severity (TL)
11:5	—	0	Reserved
4	RWS	1	Data Link Protocol Error Severity (DLL)
3:1	—	0	Reserved
0	RWS	1	Training Error Severity (PHY)

Offset Address: 113-110h (D3F3)

Correctable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:13	—	0	Reserved
12	RW1CS	0	Replay Timer Timeout Status (DLL)
11:9	—	0	Reserved
8	RW1CS	0	REPLAY_NUM Rollover Status (DLL)
7	RW1CS	0	Bad DLLP Status (DLL)
6	RW1CS	0	Bad TLP Status (DLL)
5:1	—	0	Reserved
0	RW1CS	0	Receiver Error Status (PHY)

Offset Address: 117-114h (D3F3)

Correctable Error Mask **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:13	—	0	Reserved
12	RWS	0	Replay Timer Timeout Mask (DLL)
11:9	—	0	Reserved
8	RWS	0	REPLAY_NUM Rollover Mask (DLL)
7	RWS	0	Bad DLLP Mask (DLL)
6	RWS	0	Bad TLP Mask (DLL)
5:1	—	0	Reserved
0	RWS	0	Receiver Error Mask (PHY)

Offset Address: 11B-118h (D3F3)

Advanced Error Capabilities and Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:9	—	0	Reserved
8	RWS	0	ECRC Check Enable (TL)
7	RO		ECRC Check Capable (TL)
6	RWS	0	ECRC Generation Enable (TL)
5	RO		ECRC Generation Capable (TL)
4:0	ROS		First Error Pointer (TL)

Offset Address: 12B-11Ch (D3F3)
Header Log (TL)

Register Offset Address	Attribute	Default	Description
11F - 11C	ROS	00h	**Header Log Register 1st DW**
123 - 120	ROS	00h	**Header Log Register 2nd DW**
127 - 124	ROS	00h	**Header Log Register 3rd DW**
12B – 128	ROS	00h	**Header Log Register 4th DW**

Offset Address: 12F-12Ch (D3F3)
Root Error Command **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:3	—	0	**Reserved**
2	RW	0	**Fatal Error Reporting Enable**
1	RW	0	**Non-Fatal Error Reporting Enable**
0	RW	0	**Correctable Error Reporting Enable**

Offset Address: 133-130Ch (D3F3)
Root Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	00h	**Advanced Error Interrupt Message Number (TL)**
26:7	—	0	**Reserved**
6	RW1CS	0	**Fatal Error Messages Received (TL)**
5	RW1CS	0	**Non-Fatal Error Messages Received (TL)**
4	RW1CS	0	**First Uncorrectable Fatal Error Message Received (TL)** Set to 1 when the first Uncorrectable Error Message received is for a Fatal Error
3	RW1CS	0	**Multiple ERR_FATAL/NONFATAL Received (TL)**
2	RW1CS	0	**ERR_FATAL/NONFATAL Received (TL)**
1	RW1CS	0	**Multiple ERR_COR Received (TL)**
0	RW1CS	0	**ERR_COR Received (TL)**

Offset Address: 137-134Ch (D3F3)
Error Source Identification **Default Value: 0000 0000h**

This register is updated regardless of the settings of Root Control register and the Root Error Command register

Bit	Attribute	Default	Description
31:16	ROS	0000	**ERR_FATAL/NONFATAL Source Identification (TL)**
15:0	ROS	0000	**ERR_COR Source Identification (TL)**

Virtual Channel Capability (140-14Fh)

Virtual Channel Capability is defined for Egress direction of the device. For Root Port, since only VC0 is defined, there is no implementation of VC Arbitration Table and Port Arbitration Table.

Offset Address: 143-140h (D3F3)
Virtual Channel Enhanced Capability **Default Value: 0001 0002h**

Bit	Attribute	Default	Description
31:20	RO	000h	**Next Capability Offset**
19:16	RO	1h	**Capability Version**
15:0	RO	0002h	**PCI Express Extended Capability ID**

Offset Address: 147-144h (D3F3)
Port VC Capability I — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	–	0	**Reserved**
11:10	RO	0	**Port Arbitration Table Entry Size** Reserved for root port
9:8	RO	0	**Reference Clock** Reserved for root port
7	–	0	**Reserved**
6:4	RO	0	**Low Priority Extended VC Count**
3	–	0	**Reserved**
2:0	RO	0	**Extended VC Count**

Offset Address: 14B-148h (D3F3)
Port VC Capability II — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**VC Arbitration Table Offset** 00 since only VC0 is defined
23:8	–	0	**Reserved**
7:0	RO	00h	**VC Arbitration Capability;** Reserved since Low Priority Extended Count (Rx144[6:4]) is 0.

Offset Address: 14D-14Ch (D3F3)
Port VC Control — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	–	0	**Reserved**
3:1	RW	0	**VC Arbitration Select**
0	RW	0	**Load VC Arbitration Table**

Offset Address: 14F-14Eh (D3F3)
Port VC Status — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:1	–	0	**Reserved**
0	RO	0	**VC Arbitration Table Status**

VC0 Resource (150-15Bh)

Offset Address: 153-150h (D3F3)
VC Resource Capability (VC0) — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**Port Arbitration Table Offset (VC0)**
23	–	0	**Reserved**
22:16	RO	00h	**Maximum Time Slots (TL)**
15	RO	0	**Reject Snoop Transactions**
14	RO	0	**Advanced Packet Switching**
13:8	–	0	**Reserved**
7:0	RO	00h	**Port Arbitration Capability**

Offset Address: 157-154h (D3F3)

VC Resource Control (VC0) **Default Value: 8000 00FFh**

Bit	Attribute	Default	Description
31	RO	1	**VC Enable**
30:27	—	0	**Reserved**
26:24	RO	0	**VC ID**
23:20	—	0	**Reserved**
19:17	RW	0	**Port Arbitration Select**
16	RW	0	**Load Port Arbitration Table**
15:8	—	0	**Reserved**
7:0	RW Bit 0: RO	FFh	**TC/VC Mapping** This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC0 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit0 is hardwired to 1 (i.e. TC0 is always mapped to VC0).

Offset Address: 15B-158h (D3F3)

VC Resource Status (VC0) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	—	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)**
16	RO	0	**Port Arbitration Table Status**
15:0	—	0	**Reserved**

MECHANICAL SPECIFICATIONS

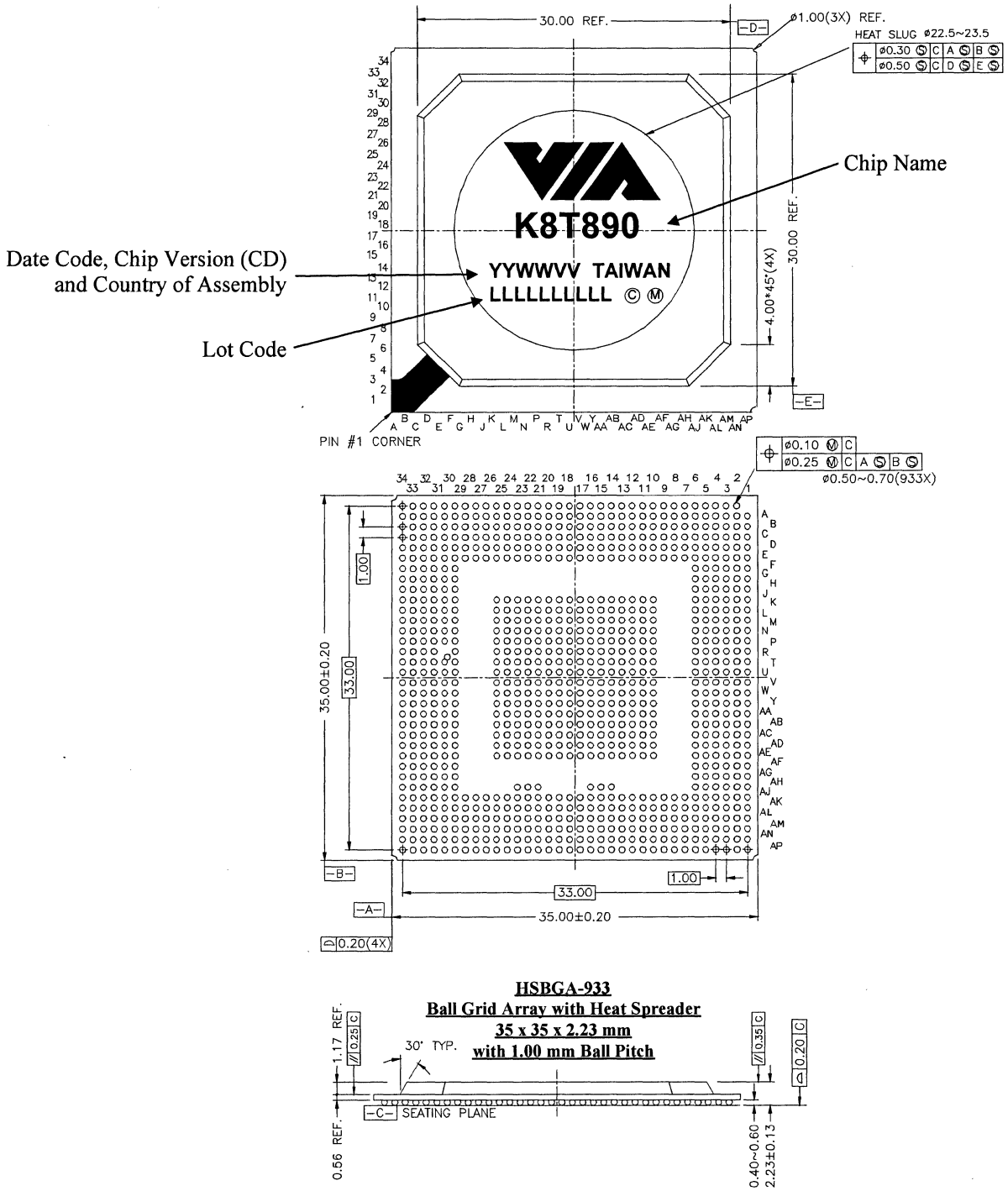

Figure 3. Mechanical Specifications – HSBGA-933 Ball Grid Array Package with Heat Spreader

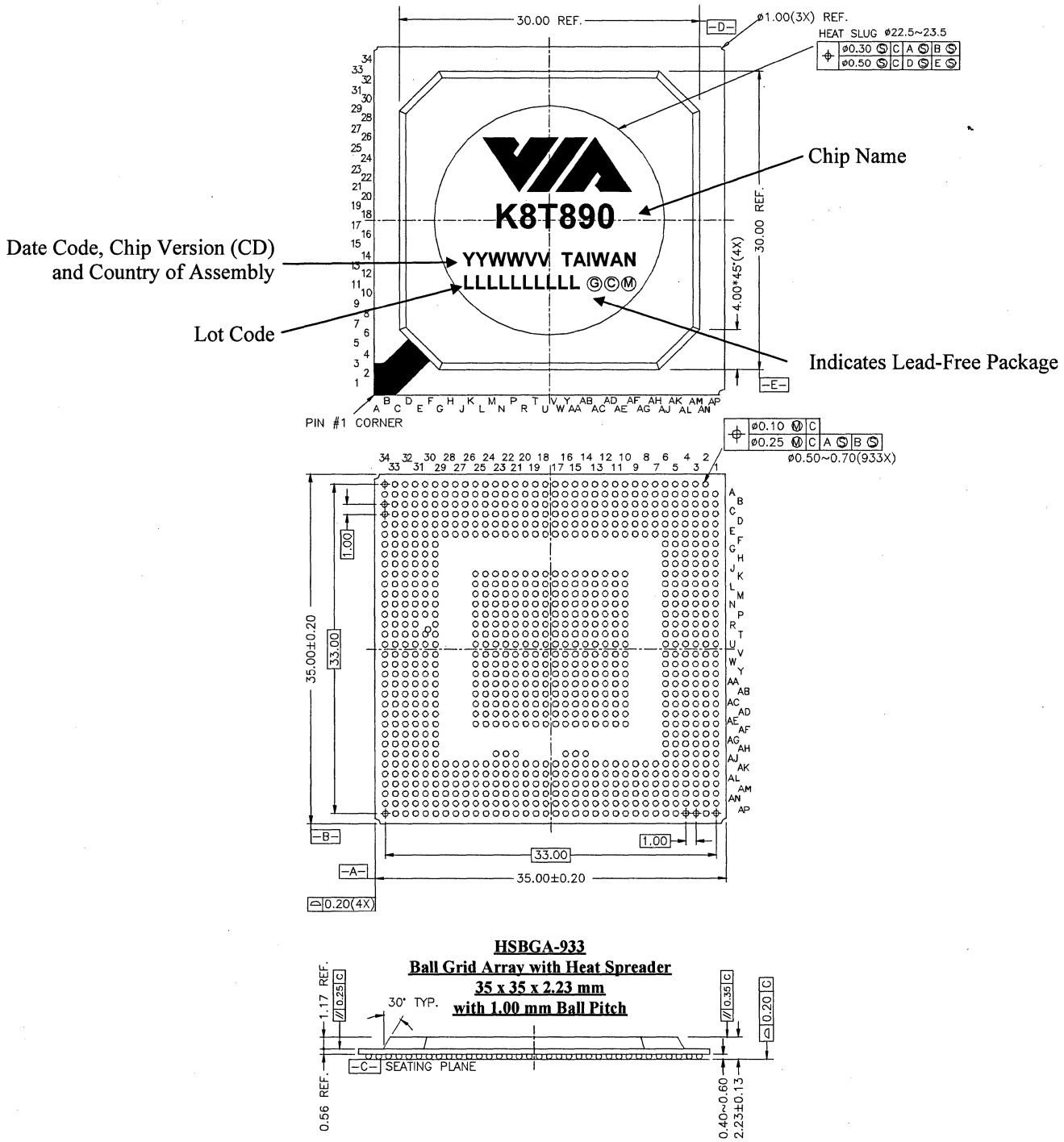

Figure 4. Lead-Free Mechanical Specifications – HSBGA-933 Ball Grid Array Package with Heat Spreader