VLSI TECHNOLOGY, INC.

APPLICATION SPECIFIC LOGIC PRODUCTS DATA BOOK 1986

Application Specific
Logic Products Division

$10.00

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VLSI TECHNOLOGY, INC.

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INTRODUCTION

GENERAL

The primary business objective of VLSI Technology, Inc., (VLSI) is to provide systems designers with total application-specific integrated circuit (ASIC) solutions. To accomplish this, it has created a unique blend of expert design tools, leading-edge process technologies, state-of-the-art fabrication facilities, and a wide range of products, including a variety of "catalog" devices.

The Application Specific Logic Products Division of VLSI Technology is responsible for the manufacture and marketing of a diverse logic-based product line that encompasses both innovative and proven, well-established catalog devices. This line includes microprocessors and coprocessors, peripheral circuits, digital signal processing devices, and products for data communications and telecommunications applications.

Unlike other suppliers of such devices, however, VLSI is also a recognized leader in ASICs. As such, it not only possesses the design, process, and fabrication capabilities necessary to produce the highest-quality off-the-shelf components, but is also able to treat its logic products as an integral part of a complete solution. One of the primary vehicles for accomplishing this is the megacell; the functions represented by individual devices can be implemented as megacells in VLSI's software libraries and used for semicustom circuit design, and functions developed as megacells for specific applications can be turned into catalog products.

MEGACELLS

The megacell is a relatively new concept in the world of IC and system design. As such ASIC companies as VLSI Technology offer better tools for IC design, simulation, and testing, it becomes necessary for systems manufacturers to design custom ICs to keep up with their competition. Megacells help decrease design time by providing large building blocks that are equivalents of standard, off-the-shelf products. By using megacells and VLSI's design tools, manufacturers can have a custom IC design capability without all of the normal custom development costs.

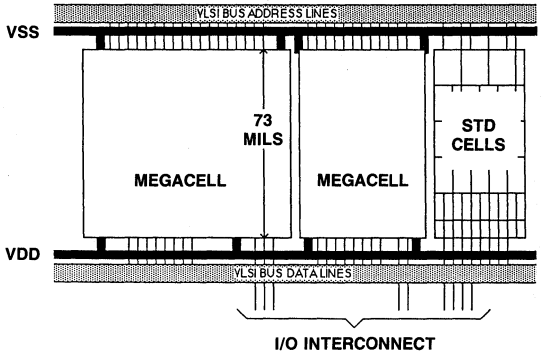
The VLSI Technology family of megacells represents commonly used peripherals that are good candidates for integration as parts of customer-driven designs, which can be either customer-specific or market-specific. In customer-specific designs, it is possible, for example, to combine these integration elements with other megacells and logic to become single-chip equivalents of computer systems that are already in production. This increased level of integration provides cost and space reductions that can keep the system designs competitive. In a market-specific design, upward-compatible enhancements that meet the needs of many customers can be added and the device offered as a new standard product.

VLSI's megacells are designed to have a fixed height and variable widths, offering the best trade-off between unusable internal space and placement ease. As shown in Figure 1, they can be configured to make a very dense final design with a minimum of wasted silicon real estate.

Of equal importance with the physical layout format of the cells is the structure of the interconnect bus. This bus must be generic enough to allow a wide variety of functions to be connected uniformly and efficiently, and must be fast enough to not itself become a limiting factor as system performance increases.

The internal structure of the bus created by VLSI for use with its megacells contains an m-bit data bus and an n-bit address bus, both of which are expandable in width to accommodate changes in system requirements. The bus operates synchronously at a rate of 3 million transfers a second, which is equivalent to the performance of a 10 MHz 8086 or a 12 MHz 68000 microprocessor. The bus definition allows for internal access times of 50 ns and cycle times in the 200 ns range. With standard pad drivers, external loads can be driven while supporting a 3 MHz bus frequency; faster speeds can be obtained by using faster pad drivers. To create a standard product from a megacell, an interface circuit is incorporated that exactly matches the slower timing of the external bus to the internal bus.

FIGURE 1. VLSI TECHNOLOGY MEGACELLS ARE ALL OF A FIXED HEIGHT, WITH VARIABLE WIDTHS.



MEGACELL-BASED DESIGN RATIONALE

There are many reasons why megacells make sense for new designs, including reduced board space, lower power, increased reliability and reduced design times.

Typical applications that can benefit from the use of megacells are those that contain three or four LSI components and a handful of "glue" components. All of these components can be combined into a single component if the functions can be partitioned into logical groups with a reasonable number of I/O pins. In this type of application, the total pin count might be reduced from 300 pins for a discrete solution to less than 100 pins, and the circuit board area reduced from approximately 20 square inches to 2 square inches.

The power consumption of megacell designs can be very small in comparison with the HMOS designs they replace, since all of the VLSI Technology megacell family is implemented in high-speed, low-power, 2-micron CMOS technology. In addition, because several functions can be put on one piece of silicon, the interconnect capacitance and inductances are minimized, thereby reducing the power to a fraction of what was needed in previous designs.

The reliability of a megacell-based design is typically better than the collection of discrete components it replaces because there are fewer pins, fewer bonding wires and lower total power consumption. In most systems, the largest contributor to reliability problems is IC pin connections, with such other factors as die temperature and die size being secondary. The more functional blocks that can be combined on a single piece of silicon, the fewer the number of interconnections that have to be bonded to package pins, resulting in higher overall reliability of the component and system using it.

Since megacells can be used as high-level building blocks, overall design times can be reduced significantly by taking existing designs using standard products and integrating additional support logic directly onto the chip. An example of this technique would be the integration of a VL68C45 CRT controller with a memory interface and video shift registers to form a single-chip video adapter. An additional option might be to include character ROMs or RAM arrays, although the addition of these commodity components is not always cost-effective.

CURRENT FAMILY OF MEGACELLS

Megacells are designed by very carefully studying the data sheets and systems implementations of the original part vendors, but an important part of validating a megacell design is to subject it to many different hardware and software environments. Only after a part has been tested in several applications can a vendor feel confident that the megacell exactly emulates the original function, including all of the undocumented "features." The VLSI Technology philosophy is to offer members of the megacell family as standard products as well as cells so that this validation can take place very quickly after the introduction of the standard product. Since customer-specific design times typically take from 2 to 4 months, megacell designs can be started before the standard product validation has been done. This lead time allows customers to get a head start introducing designs.

DESIGNING A CIRCUIT USING MEGACELLS

The design process is started by using a megacell schematic "icon" as part of the schematic entry of the user's design. Provided with the megacell icon is a data sheet detailing the internal timing requirements of the megacell. The designer works from this data sheet as if using an off-the-shelf standard product, except that the logic and timing of the bus are somewhat easier to use.

USING VLSItest DURING THE DESIGN PHASE

When the schematic entry of the design is complete, the designer uses a test language assistance program (VLSItest) to capture a set of simulation vectors that can be used to test the design after silicon has arrived. Once the designer is satisfied that the vector set is sufficient to cover all possible stuck faults, a final test program can be compiled through this program. The output from this program is a test program containing SETF statements that can be easily moved onto an industry-standard tester, such as a Sentry tester system.

ADDITIONAL LOGIC FOR TEST SIMPLIFICATION

In all cases, some additional logic will be necessary to facilitate testing the megacells. This additional logic consists of multiplexers on pins to allow all of the connections of the megacell to be accessed from the periphery of the circuit. This dictates that all designs be contained in packages having at least as many pins as the most pin-intensive megacell used internally. To enable the test mode, an illegal condition on the interface is often used, such as Read Strobe and Write Strobe being asserted together while the chip is selected. This would normally never occur in an application, so it is a safe combination to use. When enabled, the I/O pads of a specific megacell are connected to the I/O pins of the component, and the standard product test program run to verify the functionality of the core.

USING VLSItest SOFTWARE TO HELP CREATE TEST PROGRAMS

VLSItest is a software package that eliminates the need for the design engineer to be an expert in testers and testing. The designer works in a test language called VLSI Test Language (VTL), which allows simultaneous development of the circuit design and test program, providing notification early in the design stages of when tester-specific details

affect the testability of the design. Through the test language, designers can create a file describing the physical characteristics, timing, stimulus patterns and expected responses of a circuit under development (Figure 2). The remaining software translates the description into commands that run the simulation, verify the expected response, and store requested reponse values predicted from a simulator. Finally, VLSItest generates a complete test program that includes all specifications for the timing generators, strobes, and registers, all pattern-loading, requested dc parametric and summary test routines, and the test vectors needed to test the circuit functionality.

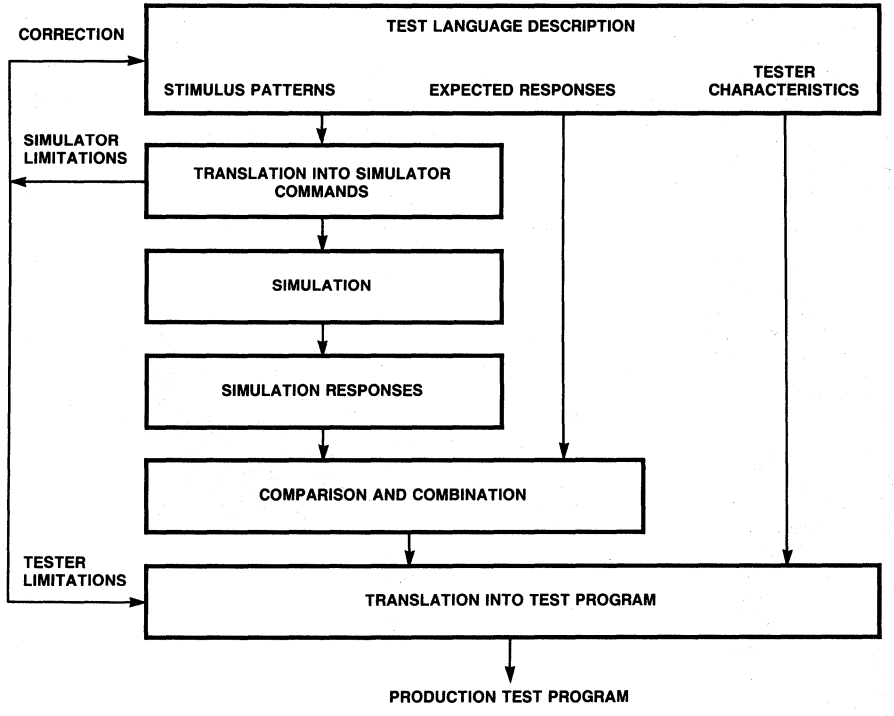
Besides identifying tester limitations associated with the test program, the software suggests ways to work around them. In that way, design engineers can become familiar with tester limitations and make the optimum design-vs.-testing trade-off. When the testability of a circuit becomes a problem, the design engineer can add additional circuitry to help out. Common practice is to break up long counter strings to reduce the number of states required to exercise each individual stage.

The test vectors generated by the software have a one-to-one correspondence with the vectors used during the simulation, so the information normally lost during post-processing is retained. Another benefit is that, since a tester is not needed to develop the test program and initially debug it, the test system is available for production time and work can be done during normal hours.

To interface with specific testers, the software needs routines that contain tester-specific information. These routines also identify portions of the test or simulation language description that can not be executed by the tester, simplifying the task of making portable test software. Interface routines are currently written in Xidak's Mainsail language for both VLSI's simulator and the Sentry Series 7, 10 and 20 testers.

When defining an IC, designers can define the stimuli and the expected responses through the test language, creating modules that describe aspects of the circuit's functions or dc test conditions. The resulting circuit description, which is independent of tester or simulator characteristics, is combined with the tester-specific and simulator-specific routines. Since the circuit description contains a complete set of operational parameters, all information necessary to create a data sheet is present. Since that information actually drives the simulator and develops the test program, it always remains up-to-date.

FIGURE 2. THE STRUCTURE OF THE VLSI TECHNOLOGY TEST LANGUAGE MAKES TEST PROGRAM GENERATION SIMPLE AND STRAIGHT-FORWARD.



DEFINING THE TEST PROGRAM FLOW

Several types of software modules are required to create a complete test description. Designers use the first module, MAIN, both to describe the overall flow of the test and to initialize the test software for execution. The contents of the MAIN module declare the duration of a test, select the required parameter modules, and specify their order of execution. The MAIN module partitions the testing into a number of steps that can be easily understood from a high level.

The DURATION statement determines the length of the tester cycle, and normal-time selects the timing parameter module of that name. The WRITE commands place remarks in the test program file for documentation purposes.

The physical characteristics of the IC are defined through the pin definition (PINDEF) module, which contains a declaration of the number of circuit pins and statements that the test software uses to identify pins during testing. Those pin-definition statements also define pin type (input, output, bidirectional, power, etc.). In addition, the module may define the device type and state whether it is static or dynamic. Labels for each element of the pin list can specify such pin types as input, output, bidirectional, power, ground, three-state, open-drain, open-source, or no-connection.

Minimum, nominal, and maximum timing parameters are defined in the TIMEPARAM module. Designers can test the circuit under different timing conditions by defining multiple modules and assigning each module its own identifier.

An additional module, EDGETIME, creates transition edges using the parameters defined by TIMEPARAM. These edges determine when the stimulus values are placed on the input pins and when the response values are measured during each test cycle, indicating such timing points as when outputs should be sampled and when inputs should be changed. For example, to create a clock that remains LOW for 80 ns, HIGH for 100 ns, and repeats every 200 ns would require the definition of four edges. The first edge would be at 0 ns, the second at 80 ns, the third at 180 ns, and the fourth at 200 ns. The last edge defines the period of the cycle and is also used for the duration declaration.

For each test cycle, the CYCLE module describes the stimulus for input pins and the response for output pins. If parameter values are included within parentheses in the module heading, a variety of values can be placed on the input pins. Each time the module is called, the appropriate values are passed to it. This module takes transition edges from the EDGETIME module and determines when to apply stimulus values to the I/O pins and when to measure outputs during each test cycle. CYCLE statements in the modules specify whether a specific pin is to be stimulated or measured. A transition edge at a pin may be specified by "@" time. If not specified, the stimulus values are placed on the pin at the beginning of the cycle and the responses are measured at the end of the cycle.

With FUNCTIONTEST modules, the designer partitions the test into functional blocks or initialization procedures, particularly if the sections are to be used more than once. The first DCPARAM statement sets the minimum and maximum measurement values as well as the source that creates them (current or voltage). Defaults are provided if exact values have not been selected. An important attribute of this module is that some portions can be used more than once. These modules are executed when called by the MAIN routine or other FUNCTIONTEST routines. They may contain WHILE and other looping constructs to provide a means of conditionally executing statements.

SIMULATION AND TEST PROGRAM GENERATION

As the software generates the test program, it draws on the stimulus and response values to select each pin's timing generators and strobes on the basis of the value of the pin before the cycle starts, the number of transitions occuring on the pin during the cycle, and if the pin is to be an input or output during the cycle.

The selection of mask registers is determined by the state of the registers at the start of the cycle and the pins that have been activated during the cycle. The appropriate values are inserted into a test vector, which is stored in a vector file with the register set or enabling commands. Before storing the test vector, the software attempts to take advantage of any vector compaction capability of the tester.

After the test language is used to create the modules, the resulting description file is loaded into VLSItest, which parses it and ensures that its syntax is correct. While parsing, the software creates a data base from the physical characteristics described in the PINDEF module and from the identifiers used throughout the circuit description. After the program is properly compiled, testing may begin.

The test language itself possesses all the power and flexibility needed to efficiently develop test programs. All variables and constants are 32-bit values that may be manipulated on a bit-by-bit basis by a variety of familiar operators, such as AND, OR, and XOR. Additionally, the language's looping constructs present a compact means of conditionally executing a series of tests.

COMPLETING THE DESIGN

Test engineering effort is still required when using this process, but the time spent can be a matter of only a few weeks, rather than the several-week period traditionally associated with creating a test program for a new product.

When simulation is complete and the design works satisfactorily, the layout process can begin. In most cases, designers are interested in minimizing design time and associated costs, so they pick standard cells for the additional blocks of logic that will surround the megacell cores. Cells are individually compiled, placed and routed to create blocks of logic until the entire non-megacell portion of the design is complete. For the best layout efficiency, the additional logic is either put into a block having the same height as a megacell, or it is put around the megacells to fill in the voids. When each portion of the design is completed, these blocks can be placed and interconnected using a tool called VLSICOMPOSE, which is a top-level composition editor. This editor assists in interconnecting blocks of cells and optimizing both the placement and interconnection of cells. The overall goal of placing blocks to form the chip is to get the ratio of the X and Y dimensions (the aspect ratio) as close to 1:1 as possible. The resulting square die gives the packaging engineer the most flexibility in package selection.

When the entire layout process is complete, a netlist of interconnections is extracted from the physical data base to allow comparison of what was intended to be with what actually was implemented. Once the extraction is complete and the netlist comparison between schematic and layout is successful, the device can be resimulated in software with more accuracy, since values of expected capacitance are extracted along with the connectivity information. Finally, the layout is checked for design rule violations using the design rule checker (DRC) program.

When all of this has been successfully completed, the data base is sent to a design center, where the actual physical layout of the megacells is included in the data base. When everything checks out properly, a mask set is created and silicon is started. From this point, the fabrication time typically takes 8 weeks for the first-pass prototypes.

VL68C45 MEGACELL

The first VLSI Technology megacell to be available both in standard product form and megacell format is the VL68C45 CRT controller. This part is the video timing interface component used in the IBM PC and is commonly used in low-cost video adapters for other personal computers as well. This megacell has been implemented in 2-micron CMOS technology and offers character clock rates of up to 4.5 MHz and bus clock rates at the full bus speed of 3 MHz. The version of the 6845 desired may be strap-selected to choose from the Motorola R or R1 versions, the Hitachi S version or the Synertek E version. In addition to the standard 6845 features, up to 16 bits of display memory may be used, the vertical sync pulse width is programmable and the vertical row counter is programmable to be 7, 8 or 9 bits. In addition to a larger video address space, early address lines are provided to eliminate pipeline stages in CRT adapter designs. Most control signals are the same as those offered on the standard 6845, but additional control signals are provided for ease of interfacing, three-stating address buses and option selection.

SUMMARY

Megacells offer a way to quickly design chips that replace today's board-level functions, while at the same time offering competitive costs, increased reliability, increased performance and reduced board space. The design process requires a wide range of design tools, including standard cells, cell compilers, simulators, routers, test program generators, and libraries of designs. VLSI Technology, Inc., specializes in offering these kinds of tools in addition to complete wafer services to provide a total solution to systems designers.

DATA BOOK

This data book presents a complete technical description of the VLSI Technology, Inc., Application Specific Logic Products Division product line. Where devices have been fully characterized, either by VLSI Technology or by one of its partners, specific information is presented in the form of data sheets. Information on partially characterized devices, and on devices currently under development, is in the form of product briefs. More complete data can be obtained on any device from the Logic Products Division Application Department.

VLSI TECHNOLOGY, INC.

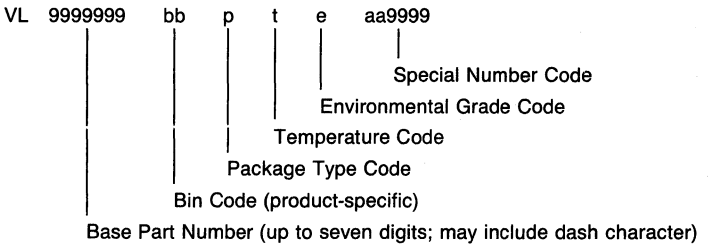
SECTION 2
ORDERING AND PACKAGING INFORMATION

Application Specific
Logic Products Division

GENERAL

VLSI Technology, Inc., Logic Products devices are available in a variety of plastic and ceramic packages, including chip carriers and pin grid arrays, and in different temperature ranges. Specific information on the packages and temperature ranges for particular devices is coded into the part number portion of the order information included in each data sheet of sections 3 through 7.

This information is organized as:



SPECIAL NUMBER CODE

RC9999 is a ROM code number.
SL9999 is a special lead number.
SM9999 is a special marketing number.
SS9999 is a special specification number.
ST9999 is a special test number.

ENVIRONMENTAL GRADE CODE

Blank (no entry) indicates that the information is not applicable.
I indicates a 48-hour dynamic burn-in.

TEMPERATURE CODE

C indicates the commercial operating temperature range of from 0°C to +70°C.

I indicates an industrial operating temperature range of from −40°C to +85°C.

M indicates the military operating temperature range of from −55°C to +125°C.

PACKAGE TYPE CODE

C indicates a ceramic side-brazed dual in-line package (ceramic DIP).
D indicates a cerdip.
G indicates a ceramic pin grid array (PGA).
L indicates a JEDEC type-B leadless chip carrier (LCC).
P indicates a plastic dual in-line package (plastic DIP).
Q indicates a plastic leaded chip carrier (PLCC).

The package forms indicated by the codes are illustrated in the outline drawings contained within this section.

PART NUMBER EXAMPLE

The part number VL68C45R−23PCSS0001 would indicate a CMOS revision R version of the 6845 CRT controller having a 2 MHz bus clock and a 3 MHz character clock, housed in a plastic DIP, operating over the commercial temperature range, and tested to a special specification (#0001).

PACKAGE CONSIDERATIONS

DUAL IN-LINE PACKAGES

The dual in-line package (DIP) has been in high-volume production for nearly twenty years, and is estimated to have been the package of choice for over 80% of all integrated circuits shipped in 1985. Some 1986 usage estimates are as high as 18 billion units worldwide. Generally, devices in DIPs can be purchased in two types of ceramic (cerdip and side-brazed) and in the very-familiar molded plastic package. Over 85% of all DIPs, or over 12 billion, sold worldwide in 1985 were plastic.

The ceramic side-brazed package is relatively expensive and is frequently imported. It has excellent mechanical characteristics, including the ability to survive extreme temperatures, salt water, and corrosive atmospheres. However, as the cost of the integrated circuit it houses becomes less and less expensive, the relative cost of the ceramic DIP becomes a major concern. In a large number of applications, this package is several times more expensive than the chip within it. As would be expected, this package is very popular in military electronics and in other potentially harsh mechanical environments. The side-brazed package, while representing less than 2% of all DIP packages shipped in 1985, represents a higher percentage of DIP revenue, due to its comparatively high average selling price (ASP).

The cerdip is a "sandwich" of two ceramic parts that are joined together by a cement-like epoxy. The die itself is mounted on a lead frame, and enjoys many of the cost economies associated with this approach. The cerdip has some of the mechanical advantages of the side-brazed ceramic at a lower cost. The cerdip represented about 14% of all DIP shipments in 1985.

The plastic DIP has been the catalyst for the computer revolution. The dramatic reduction in the cost of microprocessors, microprocessor peripherals, communications devices, and memories has been passed along to the manufacturers and the final users because plastic packaging has remained extremely inexpensive. In addition, reliable automated 16-pin and 14-pin DIP insertion equipment has dramatically reduced manual "board stuffing" costs of DIPs. The plastic DIP itself is easy to manufacture. The die is mounted on a copper-alloy lead frame and the plastic material is molded around it. It is usually branded by a printing method with an epoxy-based ink but, recently, laser-scribing the number into the plastic body is gaining popularity, reducing costs even further.

Mechanically, the DIP has proven to be an extremely utilitarian package in most applications. Its short, stiff leads on 2.54 mm (0.1 inch, or 100 mil) centers allow reasonably easy insertion for both test and production by both manual and automatic techniques. While more expensive DIPs are placed in sockets, the overwhelming majority are soldered directly into the printed circuit board. The 64-pin DIP, the largest DIP in high-volume production, is used to house VLSI's VL2010 and VL2044 Multiplier/Accumulators. DIP configurations with higher pin counts tend to exhibit unacceptable mechanical problems, such as extremely high insertion and extraction forces.

DIPs are available, in even-pin-count steps, in packages as low as two pins. A variation of the DIP that has gained some acceptance is the SIP, or single in-line package. The SIP, mounted lying on its edge, uses very little printed circuit board space and frequently contains a number of memory die in high-density memory applications. However, as desirable as the SIP may seem, it is not the major evolutionary path of the DIP. The SIP allows little air circulation for cooling, is hard to handle, and is not generally accepted as a standard. The DIP evolution lies in surface mounting the device.

SMALL-OUTLINE INTEGRATED CIRCUITS

The small-outline integrated circuit (SOIC) is a descendant of the DIP. Sometimes called the "Swiss" outline integrated circuit in honor of its country of origin, this package solves many of the problems of the DIP, while retaining many of its advantages. The gull-wing lead rests on top of the printed circuit board rather than going through it. For most types, its leads are exactly half the length that the DIP's are, and it maintains the same basic rectangular package aspect ratio of the DIP. This, however, becomes a disadvantage in high-pin-count applications. For more than 28 pins, many designers prefer the square aspect of the plastic leaded chip carrier (PLCC) to the SOIC. The small package mass of the SOIC does not allow the same thermal dissipation that can be expected in a standard DIP, which becomes a minor problem as more chips are made in the generally lower power consuming CMOS process. Most importantly, the SOIC consumes only about 30% of the real estate consumed by the standard DIP. It is estimated that nearly 1.5 billion SOIC units will be shipped in 1986.

CHIP CARRIERS

Chip carriers have been around for several years in various forms, and are just now coming into widespread usage. Generally, the terminal spacing of chip carriers is 1.27 mm (50 mils), but several special types have 1.0 mm (40 mil) spacing for use by companies engaged in the pocket pager business. Some variations are available in 0.64 mm (25 mils) also. The ceramic versions of chip carriers have become very popular in military applications for the same reason the ceramic side-brazed DIP has: their mechanical ruggedness. Frequently, ceramic leadless chip carriers (LCCs) are soldered in; others use connectors, while still others have their own leads and are inserted as a leaded device. Due to the dissimilar coefficient of expansion of materials (package alumina and printed circuit board fiberglass) and the lack of pins on the leadless versions to provide flexibility or compliance, the ceramic leadless chip carriers should be soldered to a material that has the same thermal expansion characteristics as they have. This has become very popular

in military applications where weight and space are at a premium and, generally, cost is not the primary consideration.

The plastic leaded chip carrier (PLCC) has very quickly become the most popular of all the chip carriers. The PLCC represented about 61% of the chip carriers shipped in 1985 (approximately 400 million units). Although there is debate on the issue of board space consumption, the PLCC and SOIC consume about the same amount of board space in the 24- to 28-pin configurations. In lower pin count applications, the SOIC seems to be more space-effective; when over 24 pins or so, the PLCC seems to have the edge in most applications. In applications over 28 pins, the PLCC is the surface-mount package of choice. Its square aspect ratio allows many chip placements that the highly rectangular package of the SOIC does not. In addition, there are rectangular PLCCs to accommodate such rectangular die, such as memories.

CHIP-ON-BOARD MOUNTING

The ultimate in low-cost chip mounting is achieved by the chip-on-board (COB) technology, in which no discrete package is actually employed. The die is soldered onto a copper pad on a printed circuit board. Bonding wires connect the die to smaller bonding pads around the die. The die and wires are then covered by a dollop of epoxy. This technique, while inexpensive, is not generally accepted in industrial or business equipment. It has been extensively employed in video game cartridges, and seems to work quite well there.

PIN GRID ARRAY

The pin grid array (PGA), or "bed of nails," has only been around for ten years, but had a usage of about 5 million in 1985, and its popularity is growing rapidly. This major package variation allows very high pin counts in relatively small spaces with excellent mechanical and thermal characteristics. The 149-pin VL82C389 Message Passing Co-processor (MPC) for Multibus® II systems is a prime example of PGA high-density trends. The major disadvantage of the PGA is its high cost. Virtually all of the 5 million PGA units shipped in 1985 were ceramic. Plastic pin grid arrays are well along in development, and will provide reliable, inexpensive packaging for the many high-pin-count ASIC, memory, and other circuits coming into wide usage.

FLATPACK

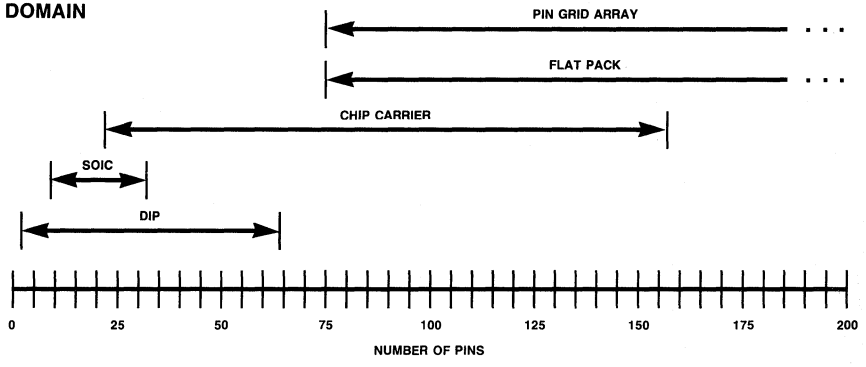
The flatpack holds less than 1% of the IC package market. True to its name, it is flat, small, and has flat leads usually in the same plane as the package body. It is generally harder to handle and test than the other package types, but provides a surface mounting alternative to the pin grid array in very-high-pin-count applications. It is usually surface mounted, "socketed," or suspended through a cut-out hole in the printed circuit board.

SYSTEM CONSIDERATIONS

In the extremely competitive computer market that now exists, every repetitive cost, no matter how small, comes under close scrutiny. Drilling a hole in a printed circuit board costs about $0.001, a fairly small amount until it is multiplied by the thousands of holes that frequently occur in each board. This becomes a significant consideration at the system level. Even though re-tooling costs are high, many companies are converting (some at least partially) to surface-mounting equipment. Surface mounting allows more chips in a much smaller area, but not all functions are yet available in surface-mount packages. Some companies have solved this problem by designing both through-the-board and surface-mount devices onto the same board. Others continue to use the older technology until they can re-tool for 100% surface mount.

Application-specific integrated circuits (ASICs) and their support devices are requiring packages with ever-increasing pin counts. The pin count domain diagram graphically depicts the typical domain of pin counts for five basic package types. While there is a good deal of overlap, chip carriers and pin grid arrays will become the package of choice in future systems containing devices of high pin count. Since the PGA device

PIN COUNT DOMAIN



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does not support surface-mount technology, chip carriers or flatpack technology will have to be implemented as pin counts exceed 170 using surface-mount systems.

CONCLUSION

There will be no panacea package that will exclude the use of all others in the future. While there are several criteria for the system designer, Table 1 examines some of the characteristics of packages that will probably occupy the overwhelming majority of printed circuit boards in the future. Leadless chip carriers will be especially popular in military and harsh industrial applications. The DIP, with many billions already in use, will not disappear, but its percentage of market will decrease steadily. Pin grid arrays will remain and increase in popularity as very large devices become more popular and plastic PGAs become readily available. Surface mounting is definitely a wave of the future for many systems. SOIC packaging will increase rapidly for devices of 28 terminals and under, while the mid-range and higher terminal count devices will be housed in PLCCs or flatpacks.

THERMAL CONSIDERATIONS

The devices in this data book have undergone thorough evaluation and characterization to ensure their operation over the specified temperature ranges. While safety margins are used for all parametric tests over the temperature range, the designer should not exceed the temperature limits, even for extremely short intervals. The following notes are presented to ensure a reliable, long-lived system using VLSI's products:

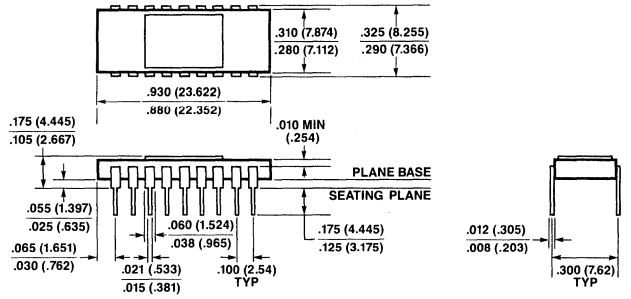
1. While few designs subject devices to extreme cold, such conditions may cause the devices to operate outside of their normal specified ranges. Therefore, the minimum operating temperature specification must be observed as well as the maximum operating temperature.
2. The ambient temperature (TA) specification refers to the air on the surface of the device. The printed circuit board design should be open enough to permit free air flow around the devices.
3. Avoid layouts that place NMOS, HMOS, or CMOS devices near such heat sources as power regulators and devices requiring heat sinks. If the design demands such proximity, ensure that the specified temperature range is not exceeded.
4. Ensure that the power supply voltage is within the specified range. Both low and high voltages beyond the specified limits may cause device overheating.

TABLE 1. PACKAGE CHARACTERISTICS

	JEDEC Leadless Chip Carriers			DIP				
Feature	**A**	**B**	**C**	**Ceramic**	**Plastic**	**SOIC**	**PLCC**	**PGA**
Uses Socket or Connector	Yes	Yes	No	Yes	Yes	No	Yes	Yes
Directly Solderable	No	No	Yes	Yes	Yes	Yes	Yes	Yes
Minimum Usual Terminal Count	14	14	14	6	6	8	16	40
Maximum Usual Terminal Count	156	156	156	64	64	28	156	225
Pin Spacing mm (mils)	1.27 (50)	1.27 (50)	1.27 (50)	2.5 (100)	2.5 (100)	1.27/1.0 (50/40)	1.27/1.0 (50/40)	2.5 (100)
Relative Cost (1 = Most Costly)	3	4	5	2	8	7	6	1

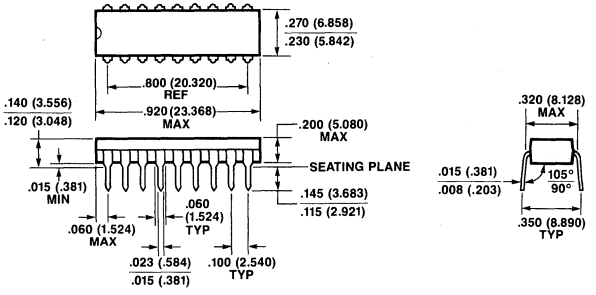
PACKAGE OUTLINES

18-PIN CERAMIC SIDE-BRAZED DUAL IN-LINE PACKAGE (DIP)



NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL METRIC DIMENSIONS ARE IN PARENTHESES ( ).
2. TOLERANCE TO BE ±.005 (0.127).
3. LEAD MATERIAL: ALLOY 42 (OR EQUIVALENT).
4. LEAD FINISH: GOLD PLATE OVER NICKEL.

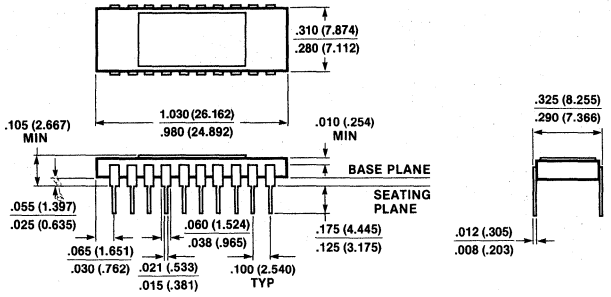
18-PIN PLASTIC DUAL IN-LINE PACKAGE (DIP)



NOTES: UNLESS OTHERWISE SPECIFIED.
1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.
2. LEAD MATERIAL: ALLOY 42 OR COPPER.
3. PACKAGE LENGTH DOES NOT INCLUDE END FLASH BURR, WHICH IS .010 (0.254) MAX. AT EACH END.
4. TOLERANCE TO BE ±.005 (0.127) UNLESS OTHERWISE NOTED.
5. METRIC DIMENSIONS ARE IN PARENTHESES ( ).
6. PIN 1 INDEX MARK MAY VARY IN SIZE AND SHAPE.

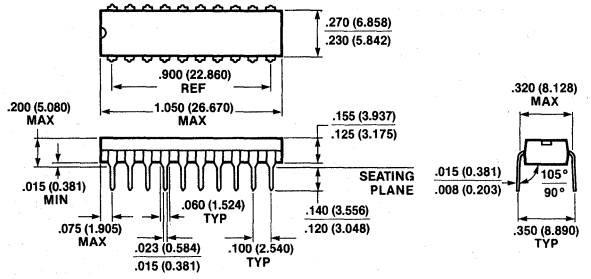
PACKAGE OUTLINES

20-PIN CERAMIC SIDE-BRAZED DUAL IN-LINE PACKAGE (DIP)



NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
2. TOLERANCE TO BE ± .005 (0.127).
3. LEAD MATERIAL: ALLOY 42 (OR EQUIVALENT).
4. LEAD FINISH: GOLD PLATE OVER NICKEL.

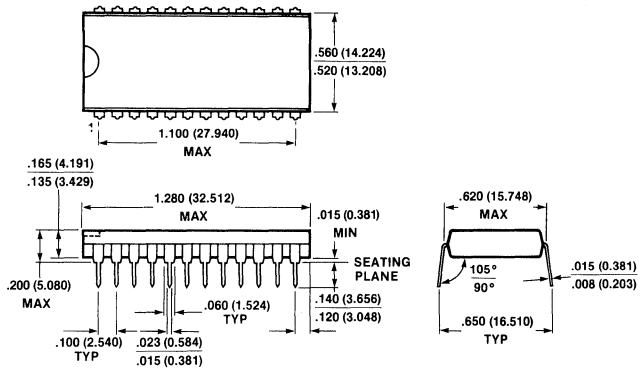
20-PIN PLASTIC DUAL IN-LINE PACKAGE (DIP)



NOTES: UNLESS OTHERWISE SPECIFIED.
1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.
2. LEAD MATERIAL: ALLOY 42 OR COPPER.
3. PACKAGE LENGTH DOES NOT INCLUDE END FLASH BURR, WHICH IS .010 (0.254) MAX AT EACH END.
4. TOLERANCE TO BE ± .005 (0.127).
5. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
6. PIN 1 INDEX MARK MAY VARY IN SIZE AND SHAPE.

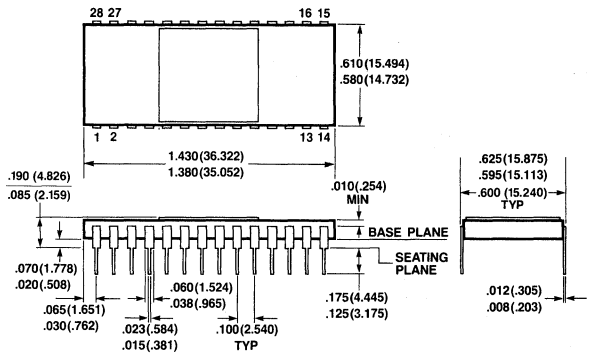
PACKAGE OUTLINES

24-PIN PLASTIC DUAL IN-LINE PACKAGE (DIP)



NOTES: UNLESS OTHERWISE SPECIFIED.
1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.
2. LEAD MATERIAL: ALLOY 42 OR COPPER.
3. PACKAGE LENGTH DOES NOT INCLUDE END FLASH BURR, WHICH IS .010 (0.254) MAX AT EACH END.
4. TOLERANCE TO BE ± .005 (0.127).
5. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
6. PIN 1 INDEX MARK MAY VARY IN SIZE AND SHAPE.

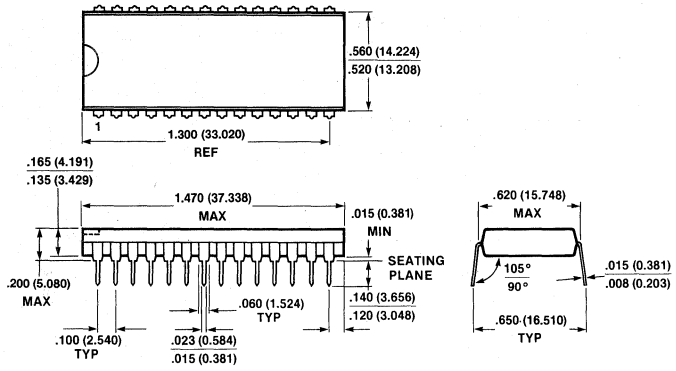
28-PIN CERAMIC SIDE-BRAZED DUAL IN-LINE PACKAGE (DIP)



NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
2. TOLERANCE TO BE ± .005 (0.127).
3. LEAD MATERIAL: ALLOY 42 (OR EQUIVALENT).
4. LEAD FINISH: GOLD PLATE OVER NICKEL.

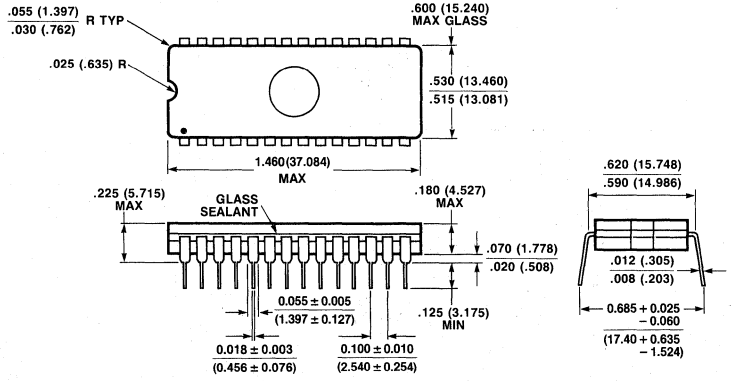
PACKAGE OUTLINES

28-PIN PLASTIC DUAL IN-LINE PACKAGE (DIP)



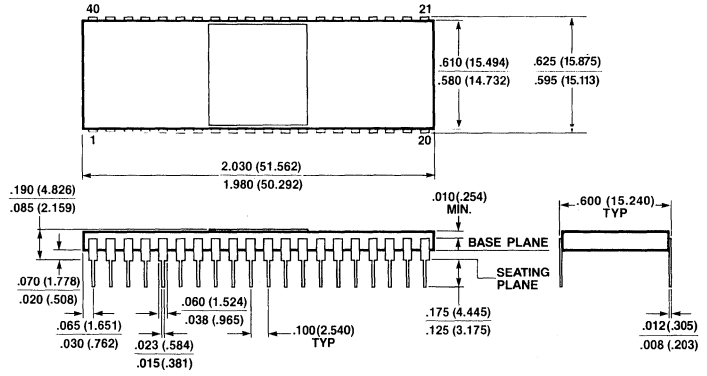
NOTES: UNLESS OTHERWISE SPECIFIED.
1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.
2. LEAD MATERIAL: ALLOY 42 OR COPPER.
3. PACKAGE LENGTH DOES NOT INCLUDE END FLASH BURR WHICH IS .010 (0.254) MAX. AT EACH END.
4. TOLERANCE TO BE ± .005 (0.127) UNLESS OTHERWISE NOTED.
5. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
6. PIN 1 INDEX MARK MAY VARY IN SIZE AND SHAPE.

28-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



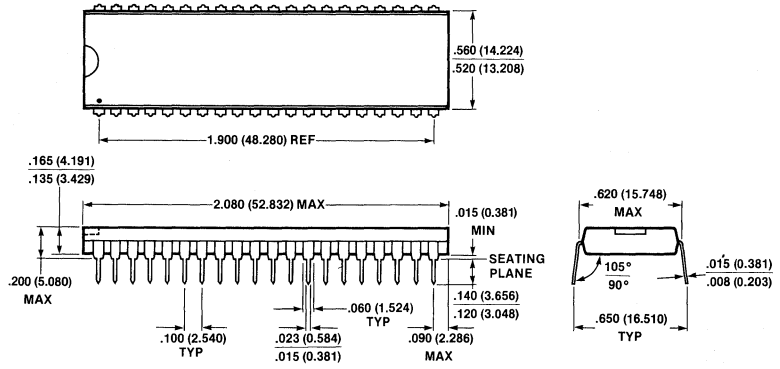
PACKAGE OUTLINES

40-PIN CERAMIC SIDE-BRAZED DUAL IN-LINE PACKAGE (DIP)



NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
2. TOLERANCE TO BE ± .005 (0.127).
3. LEAD MATERIAL: ALLOY 42 (OR EQUIVALENT).
4. LEAD FINISH: GOLD PLATE OVER NICKEL.

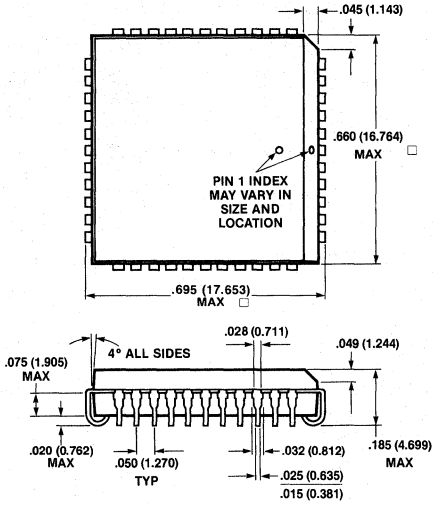
40-PIN PLASTIC DUAL IN-LINE PACKAGE (DIP)



NOTES: UNLESS OTHERWISE SPECIFIED.
1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.
2. LEAD MATERIAL: ALLOY 42 OR COPPER.
3. PACKAGE LENGTH DOES NOT INCLUDE END FLASH BURR, WHICH IS .010 (0.254) MAX AT EACH END.
4. TOLERANCE TO BE ± .005 (0.127).
5. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
6. PIN 1 INDEX MARK MAY VARY IN SIZE AND SHAPE.

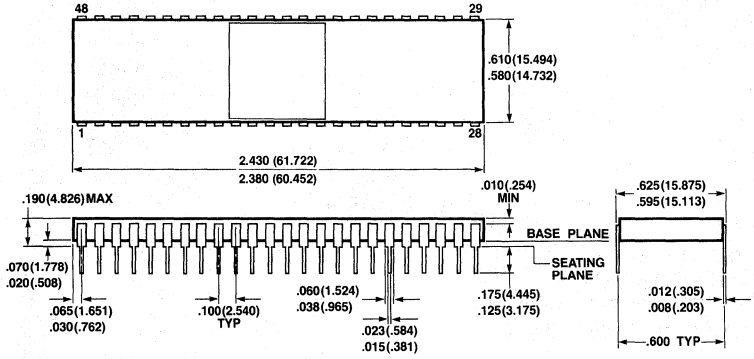
PACKAGE OUTLINES

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE ± .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. ALL METRIC DIMENSIONS ARE IN PARENTHESES.

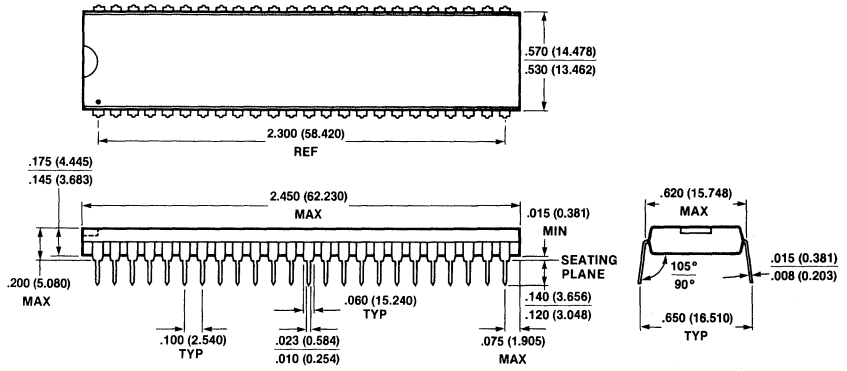
48-PIN CERAMIC SIDE-BRAZED DUAL IN-LINE PACKAGE (DIP)



NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
2. TOLERANCE TO BE ± .005 (0.127).
3. LEAD MATERIAL: ALLOY 42 (OR EQUIVALENT).
4. LEAD FINISH: GOLD PLATE OVER NICKEL.

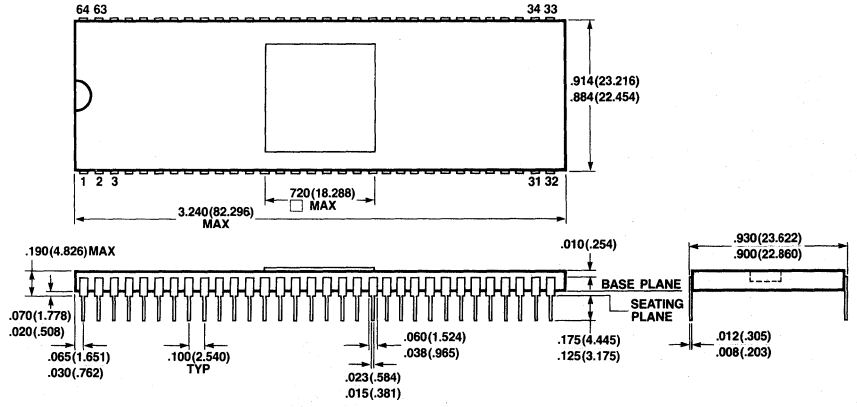
PACKAGE OUTLINES

48-PIN PLASTIC DUAL IN-LINE PACKAGE (DIP)



NOTES: UNLESS OTHERWISE SPECIFIED.
1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.
2. LEAD MATERIAL: ALLOY 42 OR COPPER.
3. PACKAGE LENGTH DOES NOT INCLUDE END FLASH BURR, WHICH IS .010 (0.254) MAX AT EACH END.
4. TOLERANCE TO BE ± .005 (0.127) UNLESS OTHERWISE NOTED.
5. METRIC DIMENSIONS ARE IN PARENTHESES.
6. PIN 1 INDEX MARK MAY VARY IN SIZE AND SHAPE.

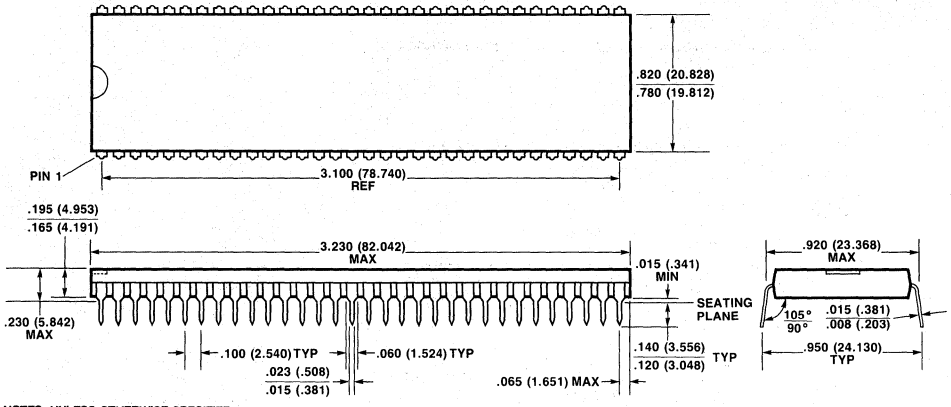
64-PIN CERAMIC SIDE-BRAZED DUAL IN-LINE PACKAGE (DIP)



NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
2. TOLERANCE TO BE ± .005 (0.127).
3. LEAD MATERIAL: ALLOY 42 (OR EQUIVALENT).
4. LEAD FINISH: GOLD PLATE OVER NICKEL.

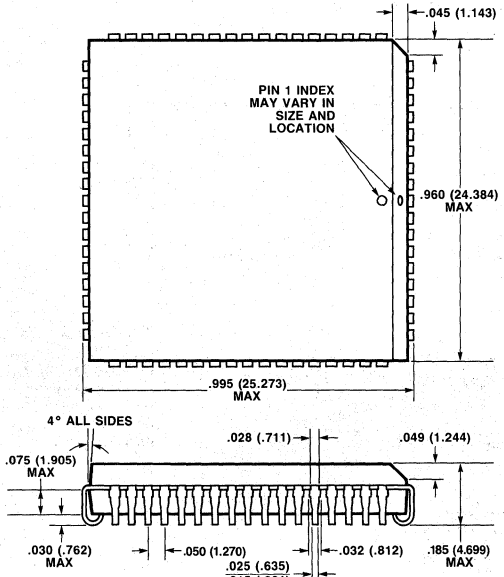
PACKAGE OUTLINES

64-PIN PLASTIC DUAL IN-LINE PACKAGE (DIP)



NOTES: UNLESS OTHERWISE SPECIFIED.
1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.
2. LEAD MATERIAL: ALLOY 42 OR COPPER.
3. PACKAGE LENGTH DOES NOT INCLUDE END FLASH BURR, WHICH IS .010 (0.254) MAX AT EACH END.
4. TOLERANCE TO BE ± .005 (0.127).
5. METRIC DIMENSIONS ARE IN PARENTHESES.
6. PIN 1 INDEX MARK MAY VARY IN SIZE AND SHAPE.

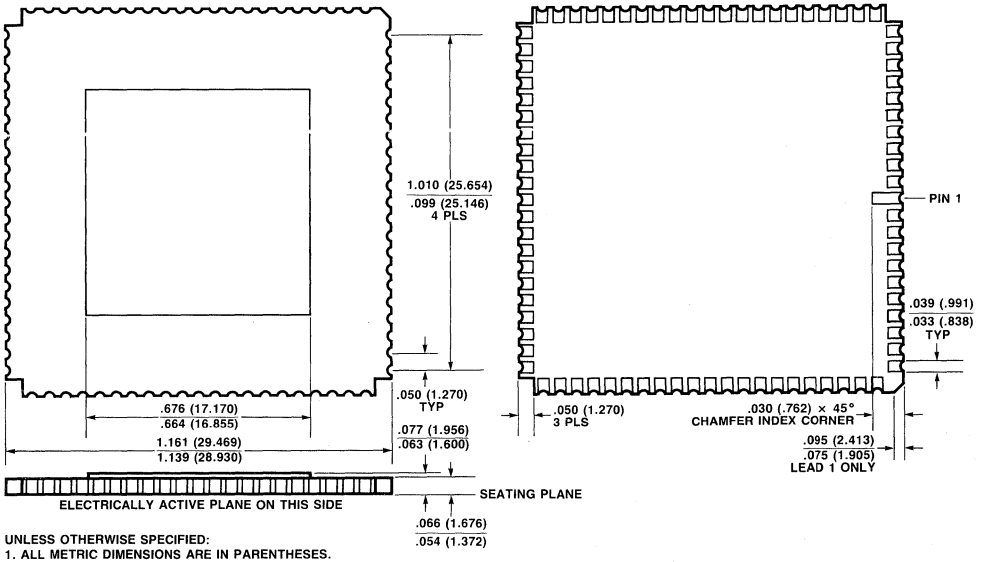
68-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE ± .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. ALL METRIC DIMENSIONS ARE IN PARENTHESES.

PACKAGE OUTLINES

84-PIN LEADLESS CHIP CARRIER (LCC)

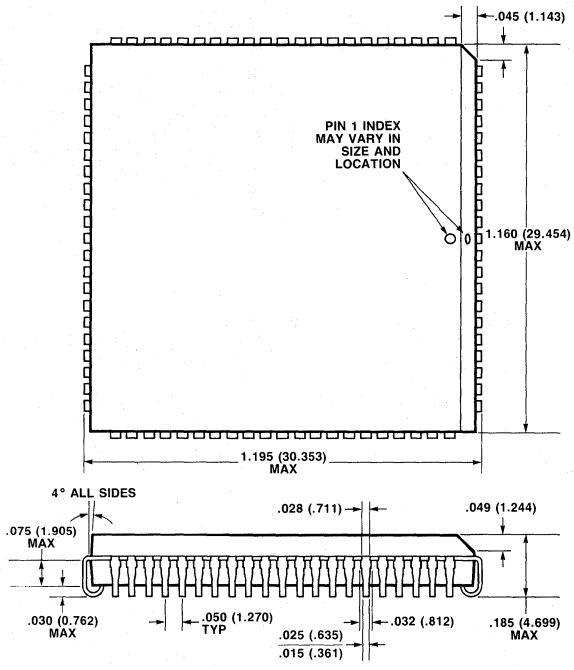


UNLESS OTHERWISE SPECIFIED:

1. ALL METRIC DIMENSIONS ARE IN PARENTHESES. METRIC DIMENSIONS ARE IN MILLIMETERS.
2. TOLERANCE TO BE ±.005 (0.127).
3. ALL EXPOSED METALLIZED AREAS SHALL BE GOLD-PLATED (60 MICROINCHES MIN. THICKNESS) OVER NICKEL (50 MICROINCHES MIN., 350 MICROINCHES MAX.) OVER REFRACTORY METALLIZATION.
4. MATERIAL: Al_2O_3.
5. JEDEC TYPE B PACKAGE.

PACKAGE OUTLINES

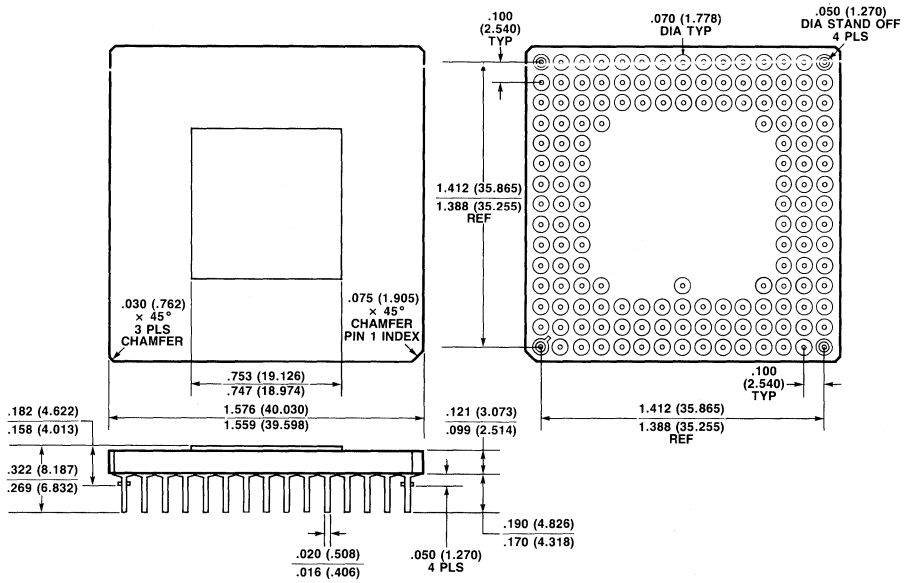
84-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



UNLESS OTHERWISE SPECIFIED:
1. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
   METRIC DIMENSIONS ARE IN MILLIMETERS.
2. TOLERANCE TO BE ±.005 (0.127).
3. LEADFRAME MATERIAL: COPPER.
4. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
5. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
6. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX. ON FOUR SIDES.

PACKAGE OUTLINES

149-PIN CERAMIC PIN GRID ARRAY (PGA)



UNLESS OTHERWISE SPECIFIED:

1. ALL METRIC DIMENSIONS ARE IN PARENTHESES. METRIC DIMENSIONS ARE IN MILLIMETERS.
2. TOLERANCE TO BE ±.005 (0.127).
3. MATERIAL: Al_2O_3.
4. LEAD MATERIAL: KOVAR.
5. LEAD FINISH IS GOLD PLATING (60 MICROINCHES MIN. THICKNESS) OVER NICKEL (100 MICROINCHES NOMINAL THICKNESS).

VLSI TECHNOLOGY, INC.

SECTION 3
PROCESSORS AND COPROCESSORS

Application Specific
Logic Products Division

VL65C02•VL65NC02

CMOS 8-BIT MICROPROCESSOR FAMILY

FEATURES

- CMOS silicon-gate technology
- Low power (1.1 mA/MHz)
- Software-compatible with the NMOS 6502
- Single 5 V power supply required
- 8-bit parallel processing
- True indexing capability
- Programmable stack pointer
- Interrupt capability
- Non-maskable interrupt
- 8-bit bidirectional data bus
- Addressable memory range of up to 64K bytes
- "Ready" input
- Direct memory access (DMA) capability
- Clock speeds up to 4 MHz
- Pipelined architecture
- On-chip clock options:
  - External single-input clock
  - On-board clock, single external crystal

DESCRIPTION

The VL65C02 and VL65NC02 are 8-bit microprocessor devices produced using CMOS silicon-gate technology. These devices provide advanced system architecture for enhancements in system performance, speed, and value over their NMOS counterparts, the 65XX family of microprocessor devices. The VL65NC02 is the CMOS equivalent of the NMOS 6502, and contains some enhancements. The VL65C02 contains significant enhancements. Both CMOS types may exhibit different intermediate cycle information from that resident in the NMOS 6502. Intermediate cycle information is not specified, and should not be used.

Both the VL65C02 and VL65NC02 provide 64K bytes of addressable memory and an interrupt input, as well as options for on-chip oscillators and drivers. Both are bus-compatible and software-compatible with the 65XX CPU family.

CLOCK GENERATOR

The clock generator develops all internal clock signals and (where applicable) external clock signals associated with the device. It is the clock generator that drives the timing control unit and the external timing for slave mode operations.

TIMING CONTROL

The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each phase-one clock pulse for as many cycles as is required to complete the instruction. Each data transfer that takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

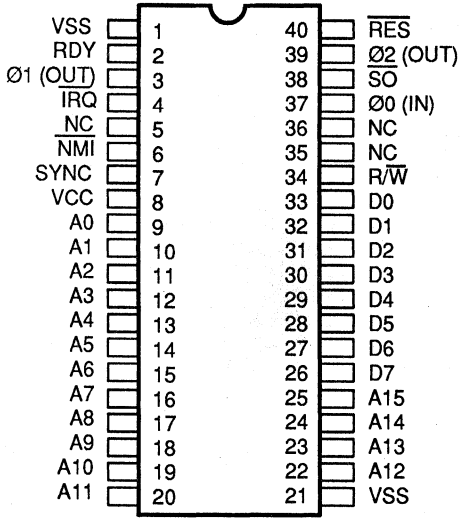
PROGRAM COUNTER

The 16-bit program counter provides the addresses which step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

PIN DIAGRAM

VL65C02
VL65NC02



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL65C02-01PC	1 MHz	Plastic DIP
VL65C02-01CC		Ceramic DIP
VL65NC02-01PC		Plastic DIP
VL65NC02-01CC		Ceramic DIP
VL65C02-02PC	2 MHz	Plastic DIP
VL65C02-02CC		Ceramic DIP
VL65NC02-02PC		Plastic DIP
VL65NC02-02CC		Ceramic DIP
VL65C02-03PC	3 MHz	Plastic DIP
VL65C02-03CC		Ceramic DIP
VL65NC02-03PC		Plastic DIP
VL65NC02-03CC		Ceramic DIP
VL65C02-04PC	4 MHz	Plastic DIP
VL65C02-04CC		Ceramic DIP
VL65NC02-04PC		Plastic DIP
VL65NC02-04CC		Ceramic DIP

Note:
Operating temperature range: 0°C to + 70°C

BLOCK DIAGRAM

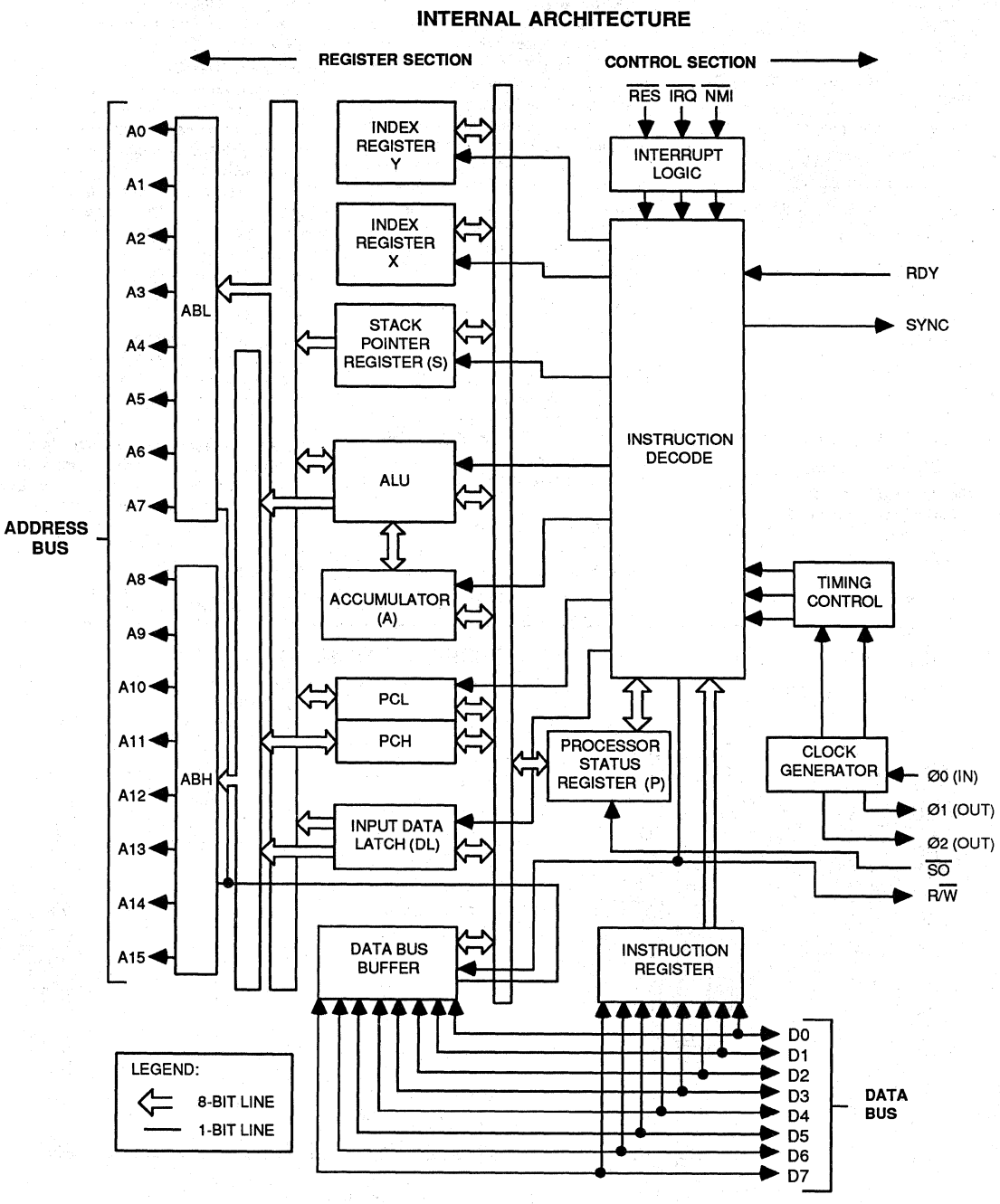


TABLE 1. HARDWARE ENHANCEMENTS

The VL65C02/VL65NC02 microprocessor devices have been designed with several hardware and software enhancements over the NMOS 6502 device while maintaining software compatability. In addition to the increased speed and lower power consumption inherent in CMOS technology, the VL65C02 and VL65NC02 have the following characteristics:

- Two new addressing modes
- Seven software/operational enhancements
- Two hardware enhancements:

VL65C02 only
- 12 new instructions, 68 total
- 59 new opcodes, 210 total

VL65NC02 only
- 8 new instructions, 64 total
- 27 new opcodes, 178 total

Feature	VL65C02 VL65NC02
Pin-compatible with NMOS 6502	x
64K addressable bytes of memory	x
$\overline{IRQ}$ interrupt	x
TTL-level single-phase clock input	x
RC time base clock input	x
Crystal time base clock input	x
Two-phase clock input*	
Two-phase output clock	x
SYNC and RDY signals	x
Bus Enable (BE) signal*	
Memory Lock ($\overline{ML}$) output signal*	
Direct Memory Access (DMA) capability*	
$\overline{NMI}$ interrupt signal	x

*Available on other 650X types

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
Ø0 (IN), Ø1 (OUT), Ø2 (OUT)	37, 3, 39	Clock Signals–The VL65(N)C02 requires an external Ø0 clock. Ø0 is a TTL-level input that is used to generate the internal clocks of the VL65(N)C02. Two full-level output clocks are generated by the VL65(N)C02. The Ø2 clock is in phase with Ø0. The Ø1 clock output is 180° out of phase with Ø0. When Ø0 is stopped, the CPU is in the standby mode.
$\overline{IRQ}$	4	Interrupt Request–This TTL-compatible input requests that an interrupt sequence begin within the microprocessor. The $\overline{IRQ}$ is sampled during Ø2 operation; if the interrupt flag in the processor status register is zero, the current instruction is completed and the interrupt sequence begins during Ø1. The program counter and processor status register are stored in the stack. The microprocessor then sets the interrupt mask flag HIGH so that no further $\overline{IRQ}$s may occur. At the end of this cycle, the program counter low byte is loaded from address FFFE, and program counter high byte from location FFFF, thus transferring program control to the memory vector located at these addresses. The RDY signal must be in the HIGH state for any interrupt to be recognized. A 3 K-ohm external resistor should be used for proper wire-OR operation.
$\overline{NMI}$	6	Non-Maskable Interrupt–A negative-going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor. The $\overline{NMI}$ is sampled during Ø2; the current instruction is completed and the interrupt sequence begins during Ø1. The program counter is loaded with the interrupt vector from locations FFFA (low byte) and FFFB (high byte), thereby transferring program control to the non-maskable interrupt routine. Note - Since this interrupt is non-maskable, another $\overline{NMI}$ can occur before the first is finished. Care should be taken when using $\overline{NMI}$ to avoid this.

SIGNAL DESCRIPTIONS (CONTINUED)

Signal Name	Pin Number	Signal Description
RDY	2	Ready –This input allows the user to single-cycle the microprocessor on all cycles, including write cycles. A negative transition to the LOW state, during or coincident with Ø1, halts the microprocessor with the output address lines reflecting the current address being fetched. This condition remains through a subsequent Ø2 in which the ready signal is LOW. This feature allows micrprocessor interfacing with low-speed memory as well as direct memory access (DMA).
R/$\overline{W}$	34	Read/$\overline{Write}$ –This signal is normally in the HIGH state, indicating that the microprocessor is reading data from memory or I/O bus. In the LOW state, the data bus has valid data from the microprocessor to be stored at the addressed memory location.
$\overline{SO}$	38	Set Overflow – A negative transition on this line sets the overflow bit (V) in the processor status register. The signal is sampled prior to the leading edge of Ø2 by the processor control time (tRWS).
$\overline{RES}$	40	Reset –This input resets the microprocessor. Reset must be held LOW for at least two clock cycles after VCC reaches operating voltage from a power-down. A positive transition on this pin causes an initialization sequence to begin. Likewise, after the system has been operating, a LOW on this line of at least two cycles ceases microprocessing activity, followed by initialization after the positive edge on $\overline{RES}$. When a positive edge is detected, there is an initialization sequence lasting six clock cycles. Then, the interrupt mask flag is set, the decimal mode is cleared, and the program counter is loaded with the restart vector from locations FFFC (low byte) and FFFD (high byte). This is the start location for program control. This input should be HIGH in normal operation.
SYNC	7	Synchronize –This output line identifies those cycles during which the microprocessor is fetching the instruction operation code (op code). The SYNC line goes high during Ø1 of an opcode fetch and stays HIGH for the remainder of that cycle. If the RDY line is pulled LOW during the Ø1 clock pulse in which SYNC went HIGH, the processor stops in its current state and remains in the state until the RDY line goes HIGH. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.
A0-A15	9-25	Address Bus–A0-A15 forms a 16-bit address bus for memory and I/O exchanges on the data bus. The output of each address line is TTL-compatible, capable of driving one standard TTL load and 130 pF.
D0-D7	33-26	Data Bus–The data lines constitute an 8-bit bidirectional data bus used for data exchanges to and from the device and peripherals. The outputs are three-state buffers capable of driving one TTL load and 130 pF.
VCC	8	+5 V ± 5% power supply
VSS	1, 21	Digital ground

TABLE 2. VL65C02/VL65NC02 NO OPERATION (NOP) TIMING FOR UNDEFINED OPCODES

Op code	Number of Bytes Expected (Total, Including Op code)	Number of Cycles
X2	2	2
X3	1	1
X7	1	1*
XB	1	1
XF	1	1*
44	2	3
54	2	4
D4	2	4
F4	2	4
5C	3	8
DC	3	4
FC	3	4

Notes:
"X" – Don't care
* – Applies to VL65NC02 only (valid operation for VL65C02)

INSTRUCTION AND REGISTER DECODE
Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instruction register, then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

ARITHMETIC/LOGIC UNIT
All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

ACCUMULATOR
The accumulator is a general-purpose 8-bit register that stores the results of most arithmetic and logic operations.In addition, the accumulator usually contains one of the two data words used in these operations.

INDEX REGISTER
There are two 8-bit index registers (X and Y) that may be used to count program steps or to provide an index value to be used in generating an effective address.

When executing an instruction that specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible (see addressing modes).

STACK POINTER
The stack pointer is an 8-bit register used to control the addressing of the variable-length stack on page one. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts ($\overline{NMI}$ and $\overline{IRQ}$). The stack allows simple implementation of nested sub-routines and mulitple-level interrupts. The stack pointer should be initialized before any interrupts or stack operations occur.

PROCESSOR STATUS REGISTER
The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled by the program and the CPU. The VL65(N)C02 instruction set contains a number of conditional branch instructions that are designed to allow testing of these flags.

HARDWARE ENHANCEMENTS
The VL65C02 family of CPU devices has incorporated hardware enhancements over its NMOS counterpart, the 6502. These hardware enhancements are:

- The NMOS device would ignore the assertion of a Ready (RDY) during a write operation. The CMOS family stops the processor during Ø2 clock if RDY is asserted during a write operation.
- On the NMOS device, unused input-only pins ($\overline{IRQ}$, $\overline{NMI}$, RDY, $\overline{RES}$, and $\overline{SO}$) must be connected to a low impedance signal to avoid noise problems. These unused pins on the CMOS devices are internally connected by a high-impedance to Vcc (approximately 250 K-ohms).

OPERATIONAL ENHANCEMENTS
Tables 1 and 3 list the operational enhancements that have been added to the CMOS family of CPU devices and compares the results with its NMOS 6502 counterpart.

TABLE 3. SOFTWARE ENHANCEMENTS

Function	VL65C02 Microprocessor	NMOS 6502 Microprocessor
Indexed addressing across page boundary	Extra read of last instruction byte	Extra read of invalid address
Execution of invalid opcodes	All are NOPs (reserved for future use)	Some terminate only by reset; results are undefined
Jump indirect, operand = XXFF	Page address increments and adds one additional cycle	Page address does not increment
Read/modify/write instructions at effective address	Two read and one write cycles	One read and two write cycles
Decimal flag	Initialized to binary mode (D=0) after reset and interrupts	Indeterminate after reset
Flags after decimal operation	Valid flag adds one additional cycle	Invalid N, V and Z flags
Interrupt after fetch of BRK instruction	BRK is executed, then interrupt is executed	Interrupt vector is loaded; BRK vector is ignored

ADDRESSING MODES

The VL65(N)C02 CPU family has 15 addressing modes (two more than the NMOS-equivalent family). In the following discussion of these addressing modes, a bracketed expression follows the title of the mode. This expression is the term used in the Instruction Set Opcode Matrix, Table 8, to make it easier to identify the actual addressing mode used by the instruction.

ACCUMULATOR ADDRESSING
[Accum]- This form of addressing isrepresented by a one-byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING
[IMM] - In immediate addressing, the second byte of the instruction contains the operand, with no further memory addressing required.

ABSOLUTE ADDRESSING
[Absolute] - In absolute addressing, the second byte of the instruction specifies the eight low-order bits of the effective address, while the third byte specifies the eight high-order bits. Thus, the absolute addressing mode allows access to the entire 64K bytes of addressable memory.

ZERO PAGE ADDRESSING
[ZP] - The zero page instructions allow for shorter code and execution times by fetching only the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in a significant increase in code efficiency.

INDEXED ZERO PAGED ADDRESSING
[ZP, X, or Y] - (X, Y Indexing) - This form of addressing is used with the index register and is referred to as "zero page, X" or "zeropage, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "zero page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "zero page" addressing nature of this mode, no carry is added to the high-order eight bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING
[ABS, X, or Y] - (X, Y Indexing) - This form of addressing is used in conjunction with X and Y index register and is referred to as "absolute, X" and "absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields, resulting in reduced coding and execution time.

INDEXED ABSOLUTE INDIRECT
[(IND), X] - (JMP (IND), X) - The contents of the second and third instruction bytes are added to the X register. The 16-bit result is a memory address containing the effective address.

IMPLIED ADDRESSING
[Implied] - In the implied addressing mode, the address containing the operand is implicity stated in the operation code of the instruction.

RELATIVE ADDRESSING
[Relative] - Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand, which is an "offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The 8-bit offset provides a branching range of -128 to +127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING
[(IND, X)] - In indexed indirect addressing, referred to as indirect, X, the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents are the low-order eight bits of the effective address. The next memory location in page zero contains the high-order eight bits of the effective address. Both memory locations specifying the high-and low-order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING
[(IND), Y] - In indirect indexed addressing, referred to as indirect, Y, the second byte of the instruction points to a memory location in page zero. The contents of this memory location are added to the contents of the Y index register, the result being the low-order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high-order eight bits of the effective address.

ABSOLUTE INDIRECT
[Indirect] - The second byte of the instruction contains the low-order eight bits of a memory location. The high-order eight bits of that memory location are contained in the third byte of the instruction. The contents of the fully specified memory location are the low-order byte of the effective address. The next memory location contains the high-order byte of the effective address, which is loaded into the 16 bits of the program counter, (JMP (IND) only).

INDIRECT
[(IND)] - The second byte of the instruction contains a zero page address serving as the indirect pointer. This is not available on the NMOS 6500 family.

TABLE 4. INSTRUCTION SET SUMMARY

Notes:

1. Add 1 to "n" if page boundary is crossed, except STA and STZ.
2. Add 1 to "n" if branch occurs to same page. Add 2 to "n" if branch occurs to different page.
3. Add 1 to "n" if decimal mode.
4. Accumulator address is included in Implied address.
5. "N" and "V" flags are unchanged in immediate mode.
6. "Z" flag indicates AAM result (same as BIT instruction).

X	Index X	+	Add	n	No. Cycles
Y	Index Y	-	Subtract	#	No. Bytes
A	Accumulator	∧	And	M_6	Memory Bit #6
M	Memory per effective address	V	Or	M_7	Memory Bit #7
Ms	Memory per stack pointer	⊻	Exclusive or		

TABLE 4. INSTRUCTION SET SUMMARY (CONTINUED)

MNE-MONIC	OPERATION	IMMEDIATE OP	n	#	ABSOLUTE OP	n	#	ZERO PAGE OP	n	#	(4) IMPLIED OP	n	#	(IND, X) OP	n	#	(1) (IND), Y OP	n	#	ZPG,X OP	n	#	(1) ABS,X OP	n	#	(1) ABS,Y OP	n	#	RELATIVE (2) OP	n	#	INDIRECT OP	n	#	ZPG,Y OP	n	#	PROCESSOR STATUS CODE 7 6 4 3 2 1 0 N V B D I Z C	MNE-MONIC
ADC	A + M + C → A (3)	69	2	2	6D	4	3	65	3	2				61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3				72	5	2				N V • • • Z C	ADC
AND	A∧M → A	29	2	2	2D	4	3	25	3	2				21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3				32	5	2				N • • • • Z •	AND
ASL	C ← [7 0] ←0				0E	6	3	06	5	2	0A	2	1							16	6	2	1E	6	3													N • • • • Z C	ASL
BCC	BRANCH IF C=0 (2)																												90	2	2							• • • • • • •	BCC
BCS	BRANCH IF C=1 (2)																												B0	2	2							• • • • • • •	BCS
BEQ	BRANCH IF Z=1 (2)																												F0	2	2							• • • • • • •	BEQ
BIT	A ∧ M (5)	89	2	2	2C	4	3	24	3	2										34	4	2	3C	4	3													M7 M6 • • • Z •	BIT
BMI	BRANCH IF N=1 (2)																												30	2	2							• • • • • • •	BMI
BNE	BRANCH IF Z=0 (2)																												D0	2	2							• • • • • • •	BNE
BPL	BRANCH IF N=0 (2)																												10	2	2							• • • • • • •	BPL
BRA	BRANCH ALWAYS(2)																												80	2	2							• • • • • • •	BRA
BRK	BREAK										00	7	1																									• • 1 0 1 • •	BRK
BVC	BRANCH IF V=0 (2)																												50	2	2							• • • • • • •	BVC
BVS	BRANCH IF V=1 (2)																												70	2	2							• • • • • • •	BVS
CLC	0 → C										18	2	1																									• • • • • • 0	CLC
CLD	0 → D										D8	2	1																									• • • 0 • • •	CLD
CLI	0 → I										58	2	1																									• • • • 0 • •	CLI
CLV	0 → V										B8	2	1																									• 0 • • • • •	CLV
CMP	A-M	C9	2	2	CD	4	3	C5	3	2				C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3				D2	5	2				N • • • • Z C	CMP
CPX	X-M	E0	2	2	EC	4	3	E4	3	2																												N • • • • Z C	CPX
CPY	Y-M	C0	2	2	CC	4	3	C4	3	2																												N • • • • Z C	CPY
DEC	DECREMENT				CE	6	3	C6	5	2	3A	2	1							D6	6	2	DE	6	3													N • • • • Z •	DEC
DEX	X-1 → X										CA	2	1																									N • • • • Z •	DEX
DEY	Y-1 → Y										88	2	1																									N • • • • Z •	DEY
EOR	A ∀ M → A	49	2	2	4D	4	3	45	3	2				41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3				52	5	2				N • • • • Z •	EOR
INC	INCREMENT				EE	6	3	E6	5	2	1A	2	1							F6	6	2	FE	6	3													N • • • • Z •	INC
INX	X + 1 → X										E8	2	1																									N • • • • Z •	INX
INY	Y + 1 → Y										C8	2	1																									N • • • • Z •	INY
JMP	JUMP TO NEW LOC				4C	3	3							7C	6	3																6C	6	3				• • • • • • •	JMP
JSR	JUMP SUB				20	6	3																															• • • • • • •	JSR
LDA	M → A	A9	2	2	AD	4	3	A5	3	2				A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3				B2	5	2				N • • • • Z •	LDA
LDX	M → X	A2	2	2	AE	4	3	A6	3	2																BE	4	3							B6	4	2	N • • • • Z •	LDX
LDY	M → Y	A0	2	2	AC	4	3	A4	3	2										B4	4	2	BC	4	3													N • • • • Z •	LDY
LSR	0→ [7 0]→ C				4E	6	3	46	5	2	4A	2	1							56	6	2	5E	6	3													0 • • • • Z C	LSR
NOP	NO OPERATION										EA	2	1																									• • • • • • •	NOP
ORA	AVM → A	09	2	2	0D	4	3	05	3	2				01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3				12	5	2				N • • • • Z •	ORA
PHA	A→Ms S-1→S										48	3	1																									• • • • • • •	PHA
PHP	P→Ms S-1→S										08	3	1																									• • • • • • •	PHP
PHX	X→Ms S-1→S										DA	3	1																									• • • • • • •	PHX
PHY	Y→Ms S-1→S										5A	3	1																									• • • • • • •	PHY
PLA	S+1→S Ms→A										68	4	1																									N • • • • Z •	PLA
PLP	S+1→S Ms→P										28	4	1																									N V 1 D I Z C	PLP
PLX	S+1→S Ms→X										FA	4	1																									N • • • • Z •	PLX
PLY	S+1→S Ms→Y										7A	4	1																									N • • • • Z •	PLY
ROL	[7 0] ←C←				2E	6	3	26	5	2	2A	2	1							36	6	2	3E	6	3													N • • • • Z C	ROL
ROR	→C→ [7 0]				6E	6	3	66	5	2	6A	2	1							76	6	2	7E	6	3													N • • • • Z C	ROR
RTI	RTRN INT										40	6	1																									N V 1 D I Z C	RTI
RTS	RTRN SUB										60	6	1																									• • • • • • •	RTS
SBC	A-M-C̄→A (3)	E9	2	2	ED	4	3	E5	3	2				E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3				F2	5	2				N V • • • Z C	SBC
SEC	1 → C										38	2	1																									• • • • • • 1	SEC
SED	1 → D										F8	2	1																									• • • 1 • • •	SED
SEI	1 → I										78	2	1																									• • • • 1 • •	SEI
STA	A → M				8D	4	3	85	3	2				81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3				92	5	2				• • • • • • •	STA
STP	STOP (1 → φ2)										DB	3	1																									• • • • • • •	STP
STX	X → M				8E	4	3	86	3	2																											96	4	2	• • • • • • •	STX
STY	Y → M				8C	4	3	84	3	2										94	4	2																	• • • • • • •	STY
STZ	00 → M				9C	4	3	64	3	2										74	4	2	9E	5	3													• • • • • • •	STZ
TAX	A → X										AA	2	1																									N • • • • Z •	TAX
TAY	A → Y										A8	2	1																									N • • • • Z •	TAY
TRB	A∧M → M (6)				1C	6	3	14	5	2																													• • • • • Z •	TRB
TSB	A∨M → M (6)				0C	6	3	04	5	2																													• • • • • Z •	TSB
TSX	S → X										BA	2	1																									N • • • • Z •	TSX
TXA	X → A										8A	2	1																									N • • • • Z •	TXA
TXS	X → S										9A	2	1																									• • • • • • •	TXS
TYA	Y → A										98	2	1																									N • • • • Z •	TYA
WAI	0 → RDY										CB	3	1																									• • • • • • •	WAI

INSTRUCTION SET

Table 5 lists the instruction set for the CMOS CPU family in alphabetic order according to mnemonic. Table 6 lists the hexadecimal codes for each of the instructions that are new to the CMOS family and were not available in the NMOS 6502 device family. Table 7 lists those instructions that were available on the NMOS family, but have been assigned new addressing modes in the CMOS CPU family.

TABLE 5. INSTRUCTION SET LISTING (ALPHABETIC)

Mnemonic		Function	Mnemonic		Function
(2)	ADC	Add Memory to Accumulator with Carry		NOP	No Operation
(2)	AND	AND Memory with Accumulator			
	ASL	Shift Left One Bit (Memory or Accumulator)	(2)	ORA	OR Memory with Accumulator
(1)(3)	BBR	Branch on Bit Reset		PHA	Push Accumulator on Stack
(1)(3)	BBS	Branch on Bit Set		PHP	Push Processor Status on Stack
	BCC	Branch on Carry Clear	(1)	PHX	Push X Register on Stack
	BCS	Branch on Carry Set	(1)	PHY	Push Y Register on Stack
	BEQ	Branch on Result Zero		PLA	Pull Accumulator from Stack
(2)	BIT	Test Bits in Memory with Accumulator		PLP	Pull Processor Status from Stack
	BMI	Branch on Result Minus	(1)	PLX	Pull X Register from Stack
	BNE	Branch on Result not Zero	(1)	PLY	Pull Y Register from Stack
	BPL	Branch on Result Plus			
(1)	BRA	Branch Always	(1)(3)	RMB	Reset Memory Bit
	BRK	Force Break		ROL	Rotate One Bit Left (Memory or Accumulator)
	BVC	Branch on Overflow Clear		ROR	Rotate One Bit Right (Memory or Accumulator)
	BVS	Branch on Overflow Set		RTI	Return from Interrupt
				RTS	Return from Subroutine
	CLC	Clear Carry Flag			
	CLD	Clear Decimal Mode	(2)	SBC	Subtract Memory from Accumulator with Borrow
	CLI	Clear Interrupt Disable Bit		SEC	Set Carry Flag
	CLV	Clear Overflow Flag		SED	Set Decimal Mode
(2)	CMP	Compare Memory and Accumulator		SEI	Set Interrupt Disable Status
	CPX	Compare Memory and Index X	(1)(3)	SMB	Set Memory Bit
	CPY	Compare Memory and Index Y	(2)	STA	Store Accumulator in Memory
				STX	Store Index X in Memory
(2)	DEC	Decrement Memory by One		STY	Store Index Y in Memory
	DEX	Decrement Index X by One	(1)	STZ	Store Zero
	DEY	Decrement Index Y by One			
				TAX	Transfer Accumulator to Index X
(2)	EOR	Exclusive-OR Memory with Accumulator		TAY	Transfer Accumulator to Index Y
			(1)	TRB	Test and Reset Bits
(2)	INC	Increment Memory by One	(1)	TSB	Test and Set Bits
	INX	Increment Index X by One		TSX	Transfer Stack Pointer to Index X
	INY	Increment Index Y by One		TXA	Transfer Index X to Accumulator
				TXS	Transfer Index X to Stack Register
(2)	JMP	Jump to New Location		TYA	Transfer Index Y to Accumulator
	JSR	Jump to New Location Saving Return Address			
(2)	LDA	Load Accumulator with Memory			
	LDX	Load Index X with Memory			
	LDY	Load Index Y with Memory			
	LSR	Shift One Bit Right (Memory or Accumulator)			

Notes:

(1) CMOS Instruction not available on NMOS family.

(2) Previous NMOS instruction with additional addressing mode(s) added to the CMOS family.

(3) VL65C02 instruction not available on VL65NC02

TABLE 6. HEXADECIMAL CODES (NEW CMOS FAMILY INSTRUCTIONS)

Hex	Mnemonic	Description
80	BRA	Branch Relative Always (Relative)
3A	DEC	Decrement Accumulator (Accum)
1A	INC	Increment Accumulator (Accum)
DA	PHX	Push X on Stack (Implied)
5A	PHY	Push Y on Stack (Implied)
FA	PLX	Pull X from Stack (Implied)
7A	PLY	Pull Y from Stack (Implied)
9C	STZ	Store Zero (Absolute)
9E	STZ	Store Zero (ABS, X)
64	STZ	Store Zero (ZP)
74	STZ	Store Zero (ZP, X)
1C	TRB	Test and Reset Memory Bits with Accumulator (Absolute)
14	TRB	Test and Reset Memory Bits with Accumulator (ZP)
0C	TSB	Test and Set Memory Bits with Accumulator (Absolute)
04	TSB	Test and Set Memory Bits with Accumulator (ZP)
89	BIT	Test Immediate with Accumulator (IMM)
0F-7F(1)	BBR	Branch on Bit Reset (Bit Manipulation, ZP)
8F-FF(1)	BBS	Branch on Bit Set (Bit Manipulation, ZP)
07-77(1)	RMB	Reset Memory Bit (Bit Manipulation, ZP)
87-F7(1)	SMB	Set Memory Bit (Bit Manipulation, ZP)

Note:
(1) Most significant digit change only. Instruction not available on VL65C02.

TABLE 7. HEXADECIMAL CODES (INSTRUCTIONS WITH NEW CMOS ADDRESSING MODES)

Hex	Mnemonic	Description
72	ADC	Add Memory to Accumulator with Carry [(ZP)]
32	AND	AND Memory with Accumulator [(ZP)]
3C	BIT	Test Memory Bits with Accumulator [ABS, X]
34	BIT	Test Memory Bits with Accumulator [ZP, X]
D2	CMP	Compare Memory and Accumulator [(ZP)]
52	EOR	Exclusive-OR Memory with Accumulator [(ZP)]
7C	JMP	Jump (New addressing mode) [(IND), X]
B2	LDA	Load Accumulator with Memory [(ZP)]
12	ORA	OR Memory with Accumulator [(ZP)]
F2	SBC	Subtract Memory from Accumulator with Borrow [(ZP)]
92	STA	Store Accumulator in Memory [(ZP)]

TABLE 8. INSTRUCTION SET OPCODE MATRIX

The following matrix shows the 210 op codes associated with the VL65(N)C02 family of CPU devices. The matrix identifies the hexadecimal code, the addressing mode, and the number of machine cycles associated with each op code.

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK Implied 1 7	ORA (IND, X) 2 6			TSB ZP 2 5	ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2		TSB ABS 3 6	ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*	ORA (IND) 2 5		TRB ZP 2 5	ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*	INC Accum 1 2		TRB ABS 3 6	ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR ABS 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND), Y 2 5*	AND (IND) 2 5		BIT ZP, X 2 4	AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*	DEC Accum 1 2		BIT ABS, X 3 4*	AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*	EOR (IND) 2 5			EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*	PHY Implied 1 3			EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6†			STZ ZP 2 3	ADC ZP 2 3†	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2†	ROR Accum 1 2		JMP (ABS) 3 6	ADC ABS 3 4†	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND), Y 2 5*†	ADC (IND) 2 5†		STZ ZP, X 2 4	ADC ZP, X 2 4†	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*†	PLY Implied 1 4		JMP (ABS, X) 3 6	ADC ABS, X 3 4*†	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8	BRA Relative 2 3*	STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2	BIT IMM 2 2	TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND), Y 2 6	STA (IND) 2 5		STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2		STZ ABS 3 4	STA ABS, X 3 5	STZ ABS, X 3 5	BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*	LDA (IND) 2 5		LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*	CMP (IND) 2 5			CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*	PHX Implied 1 3			CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6†			CPX ZP 2 3	SBC ZP 2 3†	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2†	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4†	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*†	SBC (IND) 2 5†			SBC ZP, X 2 4†	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*†	PLX Implied 1 4			SBC ABS, X 3 4*†	INC ABS, X 3 7	BBS7 ZP 3 5**	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

— New Opcode

0

0 | BRK / Implied / 1 7 | —OP Code / —Addressing Mode / —Instruction Bytes; Machine Cycles

†Add 1 to N if in decimal mode.
*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page;
Add 2 to N if branch occurs to different page.

Note: All of the op codes in column 7 and column F are interpreted as a NOP in the VL65NC02.

CRYSTAL/CLOCK CONSIDERATIONS

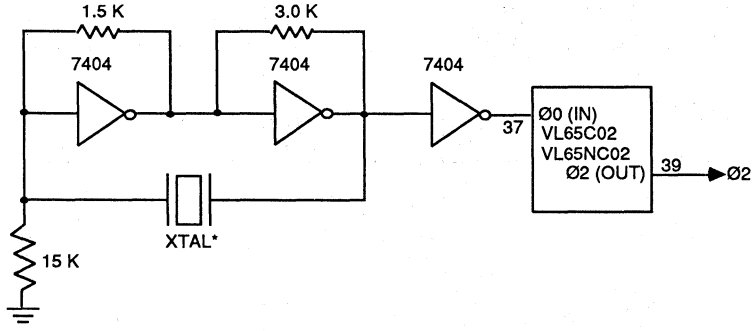
Figure 1 shows a time base generation scheme for 4 MHz operation of the VL65C02 or VL65NC02 that has been tested and proven reliable for normal environments. As with any clock oscillator circuit, stray capacitance due to board layout can cause unpredictable results requiring "fine tuning" of the circuit. Figure 2 shows a possible external clock scheme for standby mode. Table 9 identifies nominal crystal parameters for five crystal frequencies.

TABLE 9. CRYSTAL PARAMETERS

Parameter	Frequency (MHz)					Units
	3.58	4.0	6.0	8.0	10.0	
RS	60	50	30-50	20-40	10-30	Ω
C0	3.5	6.5	4-6	4-6	3-5	pF
C1	0.15	0.025	0.01-0.02	0.01-0.02	0.01-0.02	pF
Q	740K	730K	720K	720K	720K	

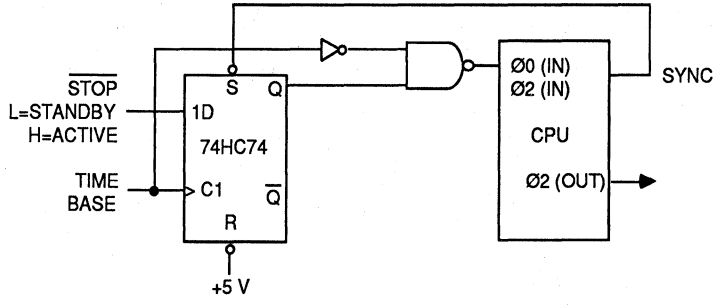
Note: AT-cut crystal parameters only. Ot hers may be used.

FIGURE 1. TIME BASE GENERATOR



Note: CTS Knights MP Series or equivalent.

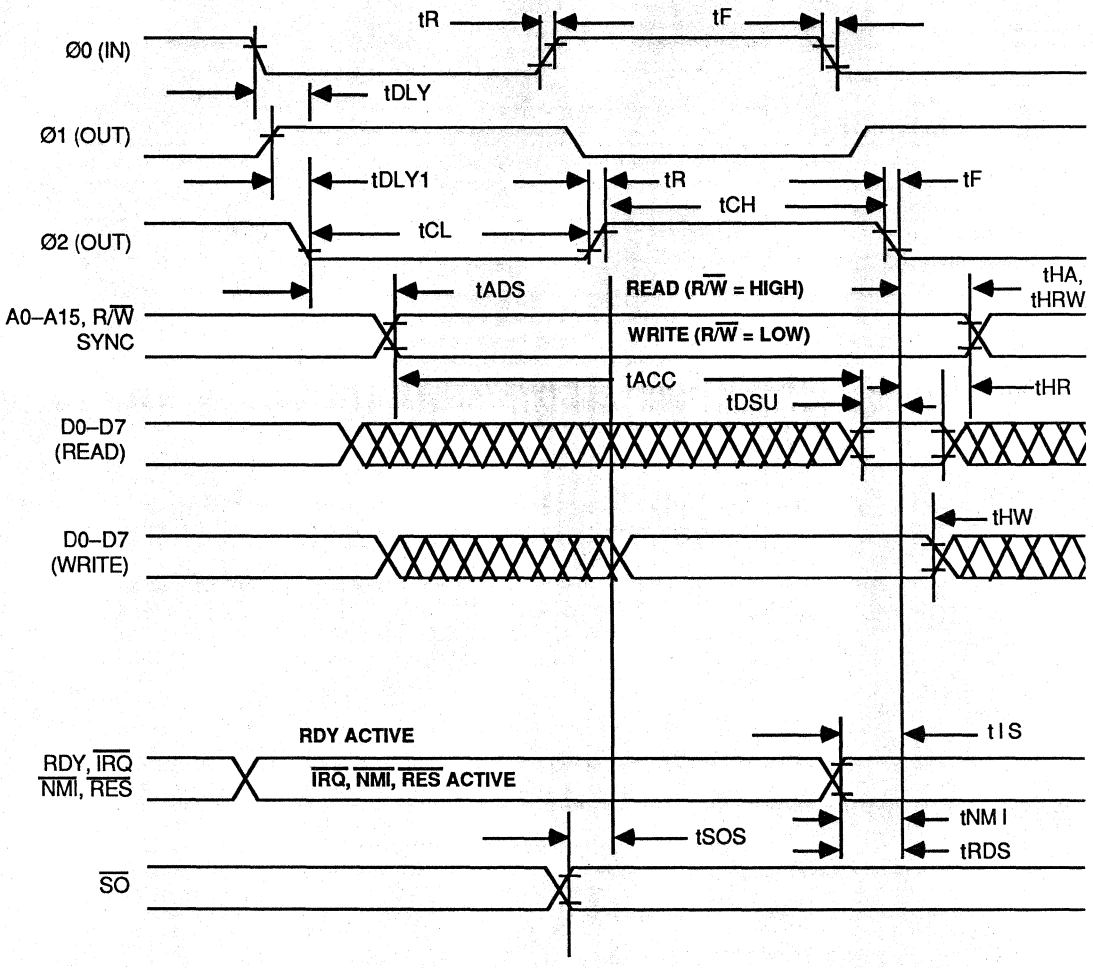
FIGURE 2. STANDBY MODE



STOPPING THE CLOCK-STANDBY MODE

Caution must be exercised when configuring theVL65C02 or VL65NC02 in the standby mode (i.e., Ø0 (IN) clock stopped). The input clock can be held in the HIGH state indefinitely; however, if the input clock is held in the LOW state longer than five microseconds, internal register and data status can be lost. Figure 2 shows a circuit that stops the Ø0 (IN) (VL65C02 or VL65NC02) clock in the HIGH state during standby mode.

FIGURE 3. TIMING DIAGRAM



Note: All timing is referenced from a HIGH level of 2.4 volts and a LOW level of 0.5 volts.

A C CHARACTERISTICS: TA = 0°C to +70°C, VCC = +5 V ± 5%

CLOCK TIMING

Symbol	Parameter	1 MHz		2 MHz		3 MHz		4 MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
tCYC	Ø2 Cycle Time	1000	Note(1)	500	Note(1)	333	Note(1)	250	Note(1)	ns
tCL	Ø2 LOW Pulse Width	430	5000	210	5000	150	5000	100	5000	ns
tCH	Ø2 HIGH Pulse Width	450	-	220	-	160	-	110	-	ns
tSK2	Ø0 to Ø2 LOW Skew	-	50	-	50	-	40	-	30	ns
tSK1	Ø2 LOW to Ø1 HIGH Skew	- 20	20	- 20	20	- 20	20	- 20	20	ns
tR, tF	Clock Rise and Fall Times	-	25	-	20	-	15	-	12	ns

READ/WRITE TIMING

Symbol	Parameter	1 MHz		2 MHz		3 MHz		4 MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
tRWS	R/$\overline{W}$ Setup Time	-	125	-	100	-	75	-	60	ns
tHRW	R/$\overline{W}$ Hold Time	15	-	15	-	15	-	15	-	ns
tADS	Address Setup Time	-	125	-	100	-	75	-	60	ns
tHA	Address Hold Time	15	-	15	-	15	-	15	-	ns
tACC	Read Access Time	775	-	340	-	215	-	160	-	ns
tDSU	Read Data Setup Time	100	-	60	-	40	-	30	-	ns
tHR	Read Data Hold Time	10	-	10	-	10	-	10	-	ns
tMDS	Write Data Delay Time	-	200	-	110	-	85	-	55	ns
tHW	Write Data Hold Time	30	-	30	-	30	-	30	-	ns

CONTROL SIGNAL TIMING

Symbol	Parameter	1 MHz		2 MHz		3 MHz		4 MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
tSYS	SYNC Delay	-	125	-	100	-	75	-	60	ns
tRDS	RDY Setup Time	200	-	110	-	80	-	60	-	ns
tSOS	SO Setup Time	75	-	50	-	40	-	30	-	ns
tIS	$\overline{IRQ}$, $\overline{RES}$ Setup Time	200	-	110	-	80	-	60	-	ns
tNMI	$\overline{NMI}$ Setup Time	200	-	150	-	100	-	70	-	ns

Notes:

(1) VL65C02 and VL65NC02 minimum operating frequency is limited by Ø2 low pulse width. The processors can be stopped with Ø2 held high.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature - Commercial 0°C to +70°C
- Industrial -40°C to +85°C

Storage Temperature -65°C to +150°C

Supply Voltage to Ground Potential -0.3 to +7.0 V

Applied Output Voltage -0.3 to VCC + 0.3 V

Applied Input Voltage -0.3 to VCC + 0.3 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS: TA = 0°C to +70°C, VCC = +5.0 V ± 5% (Notes 1, 2, 3)

Symbol	Parameter		Min	Typ	Max	Units	Test Conditions
VIH	Input HIGH Voltage	Ø0 (IN)	2.4	-	VCC + 0.3	V	
		All Other Inputs	2.0	-	VCC + 0.3	V	
VIL	Input LOW Voltage	Ø0 (IN)	-0.3	-	+ 0.4	V	
		All Other Inputs	-0.3	-	+ 0.8	V	
IIN	Input Leakage Current	Ø0 (IN)	-	-	1.0	µA	VIN = 0 V to +5.25 V VCC = 0 V
		$\overline{NMI}$, $\overline{IRQ}$, RDY, $\overline{RES}$, $\overline{SO}$	-	-	-50	µA	
ITSI	Three-State (Off-State) Input Current D7 - D0		-	-	10	µA	VIN = 0.4 V to +2.4 V VCC = +5.25 V
VOH	Output HIGH Voltage SYNC, D7-D0, A15-A0, R/$\overline{W}$, Ø1, Ø2		2.4	-	-	V	VCC = +4.75 V ILOAD = -100 µA
VOL	Output LOW Voltage SYNC, D7-D0, A15-A0, R/$\overline{W}$, Ø1, Ø2		-	-	+0.4	V	VCC = +4.75 V ILOAD = 1.6 µA
ICC	Supply Current	Standby (4)	-	2.0	10	µA	VCC = +5.0 V
		Active (5)	-	2.6	-	mA/MHz	
		Active (6)	-	-	10	mA	
		Low Power	-	1.1	-	mA/MHz	RDY = 0 V
CIN	Input Capacitance	$\overline{NMI}$, $\overline{IRQ}$, $\overline{SO}$, RDY	-	-	7	pF	VCC = +5.0 V, VIN = 0 V, f = 1 MHz, TA = 25°C
		Ø0 (IN)	-	-	30	pF	
CIO	I/O Capacitance - D7-D0, Ø1, Ø2		-	-	10	pF	
COUT	Output Capacitance - A15-A0, R/$\overline{W}$, SYNC		-	-	10	pF	

Notes:
(1) All units are direct current (D.C.).
(2) A negative sign indicates outward current flow, positive indicates inward flow.
(3) IRQ and NMI require an external pull-up resistor.
(4) Typical values are shown for VCC = +5.0 V and TA = +25°C.
(5) Typical value for power estimation only; dependent on frequency of operation.
(6) Maximum value for power consumption; independent of frequency of operation.

VL65C816•VL65C802

CMOS 16-BIT MICROPROCESSOR FAMILY

FEATURES

- Advanced CMOS design for low power consumption and increased noise immunity
- Single 3 - 6 V power supply, 5 V specified
- Emulation mode allows complete hardware and software compatibility with 6502 designs
- 24-bit address bus allows access to 16M Bytes of memory space
- Full 16-bit ALU, Accumulator, Stack Pointer, and Index Registers
- Valid Data Address (VDA) and Valid Program Address (VPA) output allows dual cache and cycle steal DMA implementation
- Vector Pull (VP) output indicates when interrupt vectors are being addressed
- May be used to implement vectored interrupt design
- $\overline{\text{ABORT}}$ input and associated vector supports interrupting any instruction without modifying internal registers
- Separate program and data bank registers allow program segmentation
- New Direct Register allows "zero page" addressing anywhere in first 64K bytes
- 24 addressing modes: 13 original 6502 modes plus 11 new addressing modes, with 91 instructions using 255 opcodes
- New Wait for Interrupt (WAI) and Stop the Clock (STP) instructions further reduce power consumption, decrease interrupt latency and allow synchronization with external events
- New Co-Processor instruction (COP) with associated vector supports co-processor configurations (i.e., floating point processors)

DESCRIPTION

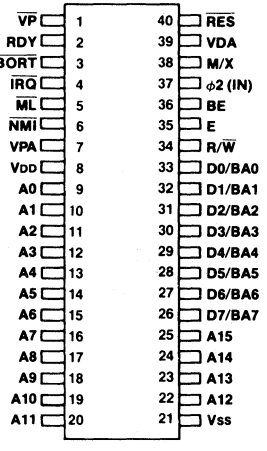
The VLSI VL65C802 and VL65C816 are CMOS 16-bit microprocessors featuring total software compatibility with their 8-bit NMOS and CMOS 6500-series predecessors. The VL65C802 is pin-for-pin compatible with 8-bit devices currently available, while the VL65C816 extends addressing to a full 16 megabytes. These devices offer the many advantages of CMOS technology, including increased noise immunity, higher reliability, and greatly reduced power requirements. A software switch determines whether the processor is in the 8-bit "emulation" mode or in the "native" mode, thus allowing existing systems to use the expanded features.

The Accumulator, ALU, X and Y Index registers, and Stack Pointer Register have all been extended to 16 bits. A new 16-bit Direct PageRegister augments the Direct Page addressing mode (formerly Zero Page addressing). Separate Program Bank and Data Bank Registers allow 24-bit memory addressing.

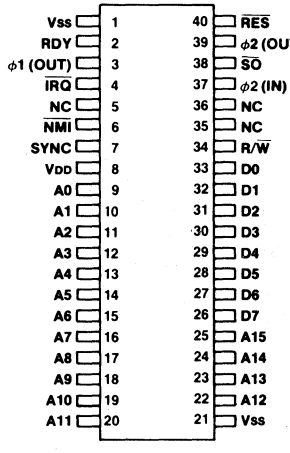
Four new signals provide the system designer with many options. The $\overline{\text{ABORT}}$ input can interrupt the currently executing instruction without modifying internal registers. Valid Data Address (VDA) and Valid Program Address (VPA) outputs facilitate dual cache memory by indicating whether a data segment or program segment is accessed. Modifying a vector is made easy by monitoring the Vector Pull (VP) output.

PIN DIAGRAMS

VL65C816



VL65C802



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL65C802-02PC	2 MHz	Plastic DIP
VL65C802-02CC		Ceramic DIP
VL65C816-02PC		Plastic DIP
VL65C816-02CC		Ceramic DIP
VL65C802-04PC	4 MHz	Plastic DIP
VL65C802-04CC		Ceramic DIP
VL65C816-04PC		Plastic DIP
VL65C816-04CC		Ceramic DIP
VL65C802-06PC	6 MHz	Plastic DIP
VL65C802-06CC		Ceramic DIP
VL65C816-06PC		Plastic DIP
VL65C816-06CC		Ceramic DIP
VL65C802-08PC	8 MHz	Plastic DIP
VL65C802-08CC		Ceramic DIP
VL65C816-08PC		Plastic DIP
VL65C816-08CC		Ceramic DIP

BLOCK DIAGRAM

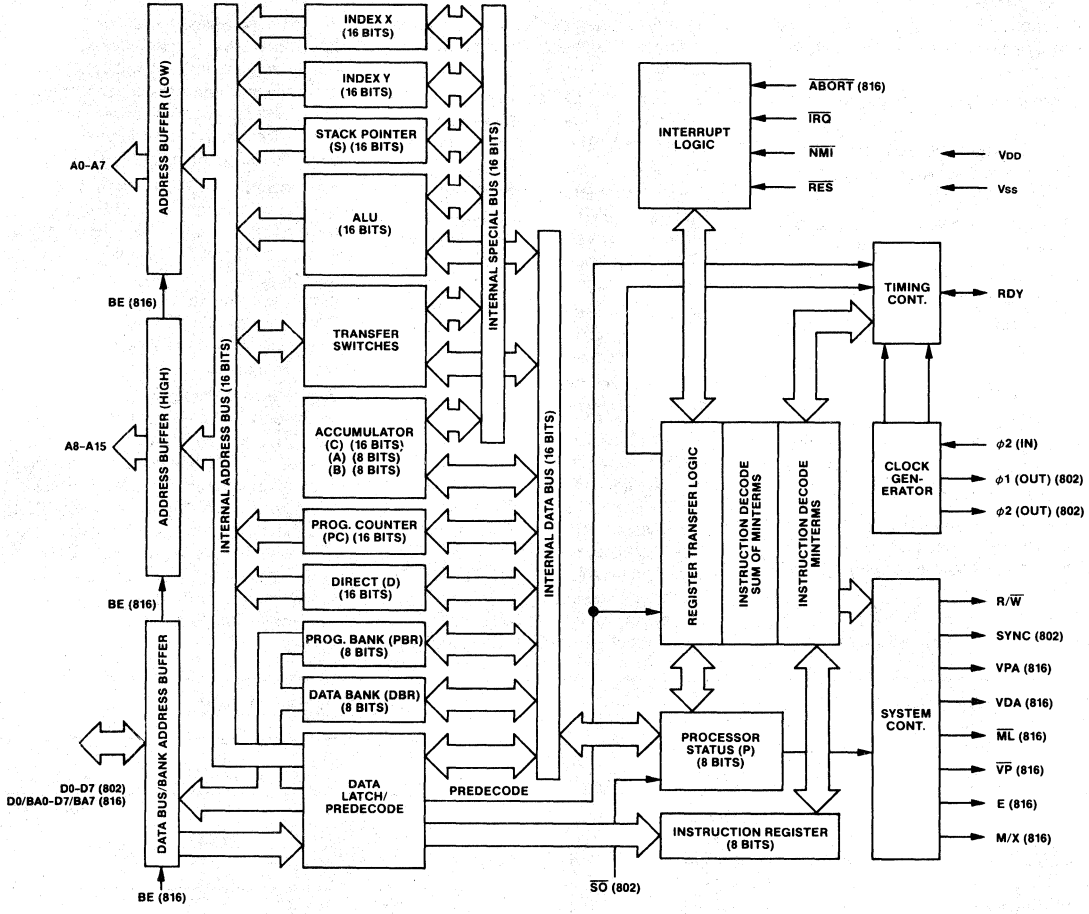


FIGURE 1. STATUS REGISTER

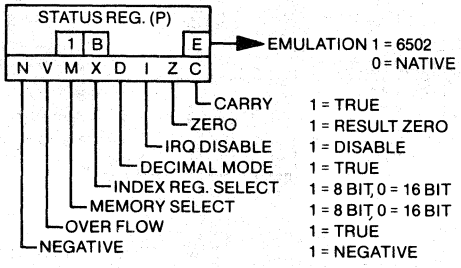


FIGURE 2. PROGRAMMING MODEL

8 BITS	8 BITS		8 BITS
Data Bank Reg. (DBR)	X Register Hi (XH)	(X)	X Register Low (XL)
Data Bank Reg. (DBR)	Y Register Hi (YH)	(Y)	Y Register Low (YL)
00	Stack Register Hi (SH)	(S)	Stack Reg. Low (SL)
= 6502 Registers	Accumulator (B)	(C)	Accumulator (A)
Program Bank Reg. (PBR)	Program (PCH)	(PC)	Counter (PCL)
00	Direct Reg. Hi (DH)	(D)	Direct Reg. Low (DL)

SIGNAL DESCRIPTIONS

Signal Name	Signal Description
Abort ($\overline{\text{ABORT}}$) (VL65C816)	The Abort input is used to abort instructions (usually due to an Address Bus condition). A negative transition will inhibit modification of any internal register during the current instruction. Upon completion of this instruction, an interrupt sequence is initiated. The location of the aborted opcode is stored as the return address in stack memory. The Abort vector address is 00FFF8, 9 (Emulation Mode) or 00FFE8, 9 (Native mode). Since $\overline{\text{ABORT}}$ is an edge-sensitive input, an Abort occurs whenever there is a negative pulse (or level) on the $\overline{\text{ABORT}}$ line during a phase 2 clock.
Address Bus (A0-A15)	These 16 output lines form the Address Bus for memory and I/O exchange on the Data Bus.. When using the VL65C816, the address lines may be set to the high-impedance state by the Bus Enable (BE) signal.
Bus Enable (BE) (VL65C816)	The Bus Enable input signal allows external control of the Address and Data Buffers, as well as the R/$\overline{\text{W}}$ signal. With Bus Enable high, the R/$\overline{\text{W}}$ and Address Buffers are active. The Data/Address Buffers are active during the first half of every cycle and the second half of a write cycle. When BE is low, these buffers are disabled. Bus Enable is an asynchronous signal.
Data Bus (D0-D7) (VL65C802)	The eight Data Bus lines provide an 8-bit bidirectional Data Bus for use during data exchange between the microprocessor and external memory or peripherals. Two memory cycles are required for the transfer of 16-bit values.
Data/Address Bus (D0/BA0-D7/BA7) (VL65C816)	These eight lines multiplex address bits BA0-BA7 with the data value. The address is present during the first half of a memory cycle, and the data value is read or written during the second half of the memory cycle. Two memory cycles are required to transfer 16-bit values. These lines may be set to the high impedance state by the BE signal.
Emulation Status (E) (VL65C816)	The Emulation Status output reflects the state of the Emulation (E) Mode flag in the Processor Status (P) Register. This signal may be thought of as an op code extension and used for memory and system management.
Interrupt Request ($\overline{\text{IRQ}}$)	The Interrupt Request input signal is used to request that an interrupt sequence be initiated. When the IRQ Disable (I) Flag is cleared, a low input logic level initiates an interrupt sequence after the current instruction is completed. The Wait for Interrupt (WAI) instruction may be executed to ensure the interrupt is recognized immediately. The Interrupt Request vector address is 00FFFE,F (Emulation Mode) or 00FFEE,F (Native mode). Since $\overline{\text{IRQ}}$ is a level-sensitive input, an interrupt occurs if the interrupt source was not cleared since the last interrupt. Also, no interrupt occurs if the interrupt source is cleared prior to interrupt recognition.
Memory Lock ($\overline{\text{ML}}$) (VL65C816)	The Memory Lock output may be used to ensure the integrity of Read-Modify-Write instructions in a multiprocessor system. Memory Lock indicates the need to defer arbitration of the next bus cycle. Memory Lock is low during the last three or five cycles of ASL, DEC, INC, LSR, ROL, ROR, TRB, and TSB memory referencing instructions, depending on the state of the M flag.
Memory/Index Select Status (M/X) (VL65C816)	This multiplexed output reflects the state of the Accumulator (M) and Index (X) Select Flags (bits 5 and 4 of the Processor Status (P) Register). Flag M is valid during the Phase 2 clock negative transition and Flag X is valid during the Phase 2 clock positive transition. These bits may be thought of as opcode extensions and may be used for memory and system management.
Non-Maskable Interrupt ($\overline{\text{NMI}}$)	A negative transition on the $\overline{\text{NMI}}$ input initiates an interrupt sequence. A high-to-low transition initiates an interrupt sequence after the current instruction is completed. The Wait for Interrupt (WAI) instruction may be executed to ensure that the interrupt will be recognized immediately. The Non-Maskable Interrupt vector address is 00FFFA,B (Emulation Mode) or 00FFEA,B (Native Mode). Since $\overline{\text{NMI}}$ is an edge-sensitive input, an interrup occurs if there is a negative transition while servicing a previous interrupt. Also, no interrupt occurs if $\overline{\text{NMI}}$ remains low.
Phase 1 Out [ø1 (OUT)] (VL65C802)	This inverted clock output signal provides timing for external read and write operations. Executing the Stop (STP) instruction holds this clock in the low state.
Phase 2 In [ø2 (IN)]	This is the system clock input to the microprocessor internal clock generator (equivalent to ø0 (IN) on the 6502). During the low-power Standby Mode, ø2 (IN) should be held in the high state to preserve the contents of internal registers.
Phase 2 Out [ø2 (OUT)] (VL65C802)	This clock output signal provides timing for external read and write operations. Addresses are valid after the address setup time (Tads), following the negative transition of ø2 (Out). Executing the (STP) instruction holds ø2 (Out) in the high state.

SIGNAL DESCRIPTIONS (CONTINUED)

Signal Name	Signal Description
Read/Write (R/$\overline{W}$)	When the R/$\overline{W}$ output signal is in the high state, the microprocessor is reading data from memory or I/O. When in the low state, the Data Bus contains valid data from the microprocessor that is to be stored at the addressed memory location. When using the VL65C816, the R/$\overline{W}$ signal may be set to the high impedance state by Bus Enable (BE).
Ready (RDY)	This bidirectional signal indicates that a Wait for Interrupt (WAI) instruction has been executed allowing the user to halt operation of the microprocessor. A low input logic level will halt the microprocessor in its current state (note that when in the Emulation Mode, the VL65C802 stops only during a read cycle). Returning RDY to the active high state allows the microprocessor to continue following the next Phase 2 In clock negative transition. The RDY signal is internally pulled low following the execution of a Wait for Interrupt (WAI) instruction, and then returned to the high state when a $\overline{RES}$, $\overline{ABORT}$, $\overline{NMI}$, or $\overline{IRQ}$ external interrupt is provided. This feature may be used to eliminate interrupt latency by placing the WAI instruction at the beginning of the $\overline{IRQ}$ servicing routine. If the $\overline{IRQ}$ Disable Flag has been set, the next instruction is executed when the $\overline{IRQ}$ occurs. The processor does stop after a WAI instruction if RDY has been forced to a high state. The Stop (STP) instruction has no effect on RDY.
Reset ($\overline{RES}$)	The Reset input is used to initialize the microprocessor and start program execution. The Reset input buffer has hysteresis such that a simple R-C timing circuit may be used with the internal pullup device. The $\overline{RES}$ signal must be held low for a least two clock cycles after VDD reaches operating voltage. Ready (RDY) has no effect while $\overline{RES}$ is being held low. During this Reset conditioning period, the following processor initialization takes place: **Registers** D = 0000 SH = 01 DBR = 00 XH = 00 PBR = 00 YH = 00 N V M X D I Z C/E P = * * 1 1 0 1 * */1 * = Not Initialized STP and WAI instructions are cleared. **Signals** E = 1 VDA = 0 M/X = 1 $\overline{VP}$ = 1 R/$\overline{W}$ = 1 VPA = 0 SYNC = 0 When Reset is brought high, an interrupt sequence is initiated: • R/$\overline{W}$ remains in the high state during the stack address cycles. • The Reset vector address is 00FFFC,D.
Set Overflow ($\overline{SO}$) (VL65C802)	A negative transition on this input sets the Overflow (V) Flag, bit 6 of the Processor Status (P) Register.
Synchronize (SYNC) (VL65C802)	The SYNC output is provided to identify those cycles during which the microprocessor is fetching an opcode. The SYNC signal is high during an opcode fetch cycle, and when combined with Ready (RDY), can be used for single instruction execution.
Valid Data Address (VDA) and Valid Program Address (VPA) (VL65C816)	These two output signals indicate the type of memory being accessed by the address bus. The following coding applies: VDA VPA 0 0 Internal operation - Address and Data Bus available. 0 1 Valid program address - May be used for program cache control. 1 0 Valid data address - May be used for data cache control. 1 1 Op code fetch - May be used for program cache control and single step control.
VDD and VSS	VDD is the positive supply voltage and VSS is system logic ground. Pin 21 of the two VSS pins on the VL65C802 should be used for system ground.
Vector Pull ($\overline{VP}$) (VL65C816)	The Vector Pull output indicates that a vector location is being addressed during an interrupt sequence. $\overline{VP}$ is low during the last two interrupt sequence cycles, during which time the processor reads the interrupt vector. The $\overline{VP}$ signal may be used to select and prioritize interrupts from several sources by modifying the vector addresses.

FUNCTIONAL DESCRIPTION

The VL65C802 offers the design engineer the opportunity to utilize both existing software programs and hardware configurations, while also achieving the added advantages of increased register lengths and faster execution times. The VL65C802 "ease of use" design and implementation features provide the designer with increased flexibility and reduced implementation costs. In the Emulation Mode, the VL65C802 not only offers software compatibility, but is also hardware (pin-for-pin) compatible with 6502 designs. It provides the advantages of 16-bit internal operation in 6502-compatible applications. The VL65C802 is an excellent direct replacement microprocessor for 6502 designs.

The VL65C816 provides the design engineer with upward mobility and software compatibility in applications in which a 16-bit system configuration is desired. The VL65C816 16-bit hardware configuration, coupled with current software, allows a wide selection of system applications. In the Emulation Mode, the VL65C816 offers many advantages, including full software compatibility with 6502 coding. In addition, the powerful VL65C816 instruction set and addressing modes make it an excellent choice for new 16-bit designs.

Internal organization of the VL65C802 and VL65C816 can be divided into two parts: 1) the Register Section, and 2) the Control Section. Instructions (or op codes) obtained from program memory are executed by implementing a series of data transfers within the Register Section. Signals that cause data transfers to be executed are generated within the Control Section. Both the VL65C802 and VL65C816 have a 16-bit internal architecture with an 8-bit external data bus.

INSTRUCTION REGISTER
An opcode enters the processor on the Data Bus and is latched into the Instruction Register during the instruction fetch cycle. This instruction is then decoded, along with timing and interrupt signals, to generate the various Instruction Register control signals.

TIMING CONTROL UNIT (TCU)
The Timing Control Unit keeps track of each instruction cycle as it is executed. The TCU is set to zero each time an instruction fetch is executed, and is advanced at the beginning of each cycle for as many cycles as is required to complete the instruction. Each data transfer between registers depends upon decoding the contents of both the Instruction Register and the Timing Control Unit.

ARITHMETIC LOGIC UNIT (ALU)
All arithmetic and logic operations take place within the 16-bit ALU. In addition to data operations, the ALU also calculates the effective address for relative and indexed addressing modes. The result of a data operation is stored in either memory or an internal register. Carry, Negative, Overflow and Zero Flags may be updated following the ALU data operation.

INTERNAL REGISTERS (Refer to figure 2, Programming Model.)

ACCUMULATORS (A, B, C)
The Accumulator is a general purpose register that stores one of the operands, or the result of most arithmetic and logical operations. In the Native Mode (E=0), when the Accumulator Select Bit (M) equals zero, the Accumulator is established as 16 bits wide (A+B=C). When the Accumulator Select Bit (M) equals one, the Accumulator is eight bits wide (A). In this case, the upper eight bits (B) may be used for temporary storage in conjunction with the Exchange B and A Accumulator (XBA) instruction.

DATA BANK REGISTER (DBR)
During modes of operation, the 8-bit Data Bank Register holds the default bank address for memory transfers. The 24-bit address is composed of the 16-bit instruction effective address and the 8-bit Data Bank address. The register value is mulitplexed with the data value and is present on the Data/Address lines during the first half of a data transfer memory cycle for the VL65C816. The Data Bank Register is initialized to zero during Reset.

DIRECT (D)
The 16-bit Direct Register provides an address offset for all instructions using direct addressing. The effective bank zero address is formed by adding the 8-bit instruction operand address to the Direct Register contents. The Direct Register is initialized to zero during Reset.

INDEX (X AND Y)
There are two Index Registers (X and Y), which may be used as general-purpose registers or to provide an index value for calculation of the effective address. When executing an instruction with indexed addressing, the microprocessor fetches the opcode and the base address, and then modifies the address by adding the Index Register contents to the address prior to performing the desired operation. Pre-indexing or post-indexing of indirect addresses may be selected. In the Native Mode (E=0), both Index Registers are 16 bits wide If the Index Select Bit (X) equals zero. If the Index Select Bit (X) equals one, both registers are 8 bits wide, and the high byte is forced to zero.

PROCESSOR STATUS (P)
The 8-bit Processor Status Register contains status flags and mode select bits. The Carry (C), Negative (N), Overflow (V), and Zero (Z) status flags serve to report the status of most ALU operations. These status flags are tested by use of Conditional Branch instructions. The Decimal (D), IRQ Disable (I), Memory/Accumulator (M), and Index (X) bits are used as mode select flags. These flags are set by the program to change microprocessor operations.

The Emulation (E) Select and the Break (B) flags are accessible only through the processor Status Register. The Emulation mode select flag is selected by the Exchange Carry and Emulation Bits (XCE) instruction. Table 1, Compatibility Issues, illustrates the features of the Native (E=0) and Emulation (E=1) Modes. The M and X flags are always equal to one in the Emulation Mode. When an interrupt occurs during the Emulation Mode, the Break Flag is written to stack memory as bit 4 of the Processor Status Register.

PROGRAM BANK REGISTER (PBR)
The 8-bit Program Bank Register holds the bank address for all instruction fetches. The 24-bit address consists of the 16-bit instruction effective address and the 8-bit Program Bank address. The register value is multiplexed with the data value and presented on the Data/Address lines during the first half

of a program memory read cycle. The Program Bank Register is initialized to zero during Reset. The PHK instruction pushes the PBR register onto the Stack.

PROGRAM COUNTER (PC)
The 16-bit Program Counter Register provides the addresses that are used to step the microprocessor through sequential program instructions. The register is incremented each time an instruction or operand is fetched from program memory.

STACK POINTER (S)
The Stack Pointer is a 16-bit register that is used to indicate the next available location in the stack memory area. It serves as the effective address in stack addressing modes as well as subroutine and interrupt processing. The Stack Pointer allows simple implementation of nested subroutines and multiple-level interrupts. During the Emulation Mode, the Stack Pointer high-order byte (SH) is always equal to one. The bank address for all stack operations is bank zero.

PIN DESCRIPTIONS

Pin	Description
A0-A15	Address Bus
$\overline{ABORT}$	Abort Input
BE	Bus Enable
ϕ2 (IN)	Phase 2 In Clock
ϕ1 (OUT)	Phase 1 Out Clock
ϕ2 (OUT)	Phase 2 Out Clock
D0-D7	Data Bus
D0/BA0-D7/BA7	Data Bus, Multiplexed
E	Emulation Select
$\overline{IRQ}$	Interrupt Request
$\overline{ML}$	Memory Lock
M/X	Mode Select (P_M or P_X)

Pin	Description
NC	No Connection
$\overline{NMI}$	Non-Maskable Interrupt
RDY	Ready
$\overline{RES}$	Reset
R/$\overline{W}$	Read/Write
$\overline{SO}$	Set Overflow
SYNC	Synchronize
VDA	Valid Data Address
$\overline{VP}$	Vector Pull
VPA	Valid Program Address
V_{DD}	Positive Power Supply (+5 Volts)
V_{SS}	Internal Logic Ground

TABLE 1. COMPATIBILITY ISSUES

	65C816/802	65C02	NMOS 6502
1. S (Stack)	Always page 1 (E = 1), 8 bits 16 bits when (E = 0).	Always page 1, 8 bits	Always page 1, 8 bits
2. X (X Index Register)	Indexed page zero always in page 0 (E = 1), Cross page (E = 0).	Always page 0	Always page 0
3. Y (Y Index Register)	Indexed page zero always in page 0 (E = 1), Cross page (E = 0).	Always page 0	Always page 0
4. A (Accumulator)	8 bits (M = 1), 16 bits (M = 0)	8 bits	8 bits
5. P (Flag Registor)	N, V, and Z flags valid in decimal mode. D = 0 after reset or interrupt.	N, V, and Z flags valid in decimal mode. D = 0 after reset and interrupt.	N, V, and Z flags invalid in decimal mode. D = unknown after reset. D not modified after interrupt.
6. Timing			
A. ABS, X ASL, LSR, ROL, ROR With No Page Crossing	7 cycles	6 cycles	7 cycles
B. Jump Indirect Operand = XXFF	5 cycles	6 cycles	5 cycles and invalid page crossing
C. Branch Across Page	4 cycles (E = 1) 3 cycles (E = 0)	4 cycles	4 cycles
D. Decimal Mode	No additional cycle	Add 1 cycle	No additional cycle
7. BRK Vector	00FFFE,F (E = 1) BRK bit = 0 on stack if $\overline{IRQ}$, $\overline{NMI}$, $\overline{ABORT}$. 00FFE6, 7 (E = 0) X = X on Stack always.	FFFE,F BRK bit = 0 on stack if $\overline{IRQ}$, $\overline{NMI}$.	FFFE,F BRK bit = 0 on stack if $\overline{IRQ}$, $\overline{NMI}$.
8. Interrupt or Break Bank Address	PBR not pushed (E = 1) RTI PBR not pulled (E = 1) PBR pushed (E = 0) RTI PBR pulled (E = 0)	Not available	Not available
9. Memory Lock ($\overline{ML}$)	$\overline{ML}$ = 0 during Read, Modify and Write cycles.	$\overline{ML}$ = 0 during Modify and Write.	Not available
10. Indexed Across Page Boundary (d),y; a,x; a,y	Extra read of invalid address.	Extra read of last instruction fetch.	Extra read of invalid address.
11. RDY Pulled During Write Cycle.	Ignored (E = 1) for 65C802 only. Processor stops (E = 0).	Processor stops	Ignored
12. WAI and STP Instructions.	Available	Available	Not available
13. Unused OP Codes	One reserved OP Code specified as WDM will be used in future systems. The 65C816 performs a no-operation.	No operation	Unknown and some "hang up" processor.
14. Bank Address Handling	PBR = 00 after reset or interrupts.	Not available	Not available
15. R/$\overline{W}$ During Read-Modify-Write Instructions	E = 1, R/$\overline{W}$ = 0 during Modify and Write cycles. E = 0, R/$\overline{W}$ = 0 only during Write cycle.	R/$\overline{W}$ = 0 only during Write cycle	R/$\overline{W}$ = 0 during Modify and Write cycles.
16. Pin 7	65C802 = SYNC. 65C816 = VPA	SYNC	SYNC
17. COP Instruction Signatures 00-7F user defined Signatures 80-FF reserved	Available	Not available	Not available

TABLE 2. INSTRUCTION SET – ALPHABETICAL SEQUENCE

ADC	Add Memory to Accumulator with Carry
AND	"AND" Memory with Accumulator
ASL	Shift One Bit Left, Memory or Accumulator
BCC	Branch on Carry Clear (P_C = 0)
BCS	Branch on Carry Set (P_C = 1)
BEQ	Branch if Equal (P_Z = 1)
BIT	Bit Test
BMI	Branch if Result Minus (P_N = 1)
BNE	Branch if Not Equal (P_Z = 0)
BPL	Branch if Result Plus (P_N = 0)
BRA	Branch Always
BRK	Force Break
BRL	Branch Always Long
BVC	Branch on Overflow Clear (P_V = 0)
BVS	Branch on Overflow Set (P_V = 1)
CLC	Clear Carry Flag
CLD	Clear Decimal Mode
CLI	Clear Interrupt Disable Bit
CLV	Clear Overflow Flag
CMP	Compare Memory and Accumulator
COP	Coprocessor
CPX	Compare Memory and Index X
CPY	Compare Memory and Index Y
DEC	Decrement Memory or Accumulator by One
DEX	Decrement Index X by One
DEY	Decrement Index Y by One
EOR	"Exclusive OR" Memory with Accumulator
INC	Increment Memory or Accumulator by One
INX	Increment Index X by One
INY	Increment Index Y by One
JML	Jump Long
JMP	Jump to New Location
JSL	Jump Subroutine Long
JSR	Jump to New Location Saving Return Address
LDA	Load Accumulator with Memory
LDX	Load Index X with Memory
LDY	Load Index Y with Memory
LSR	Shift One Bit Right (Memory or Accumulator)
MVN	Block Move Negative
MVP	Block Move Positive
NOP	No Operation
ORA	"OR" Memory with Accumulator
PEA	Push Effective Absolute Address on Stack (or Push Immediate Data on Stack)
PEI	Push Effective Indirect Address on Stack (or Push Direct Data on Stack)
PER	Push Effective Program Counter Relative Address on Stack
PHA	Push Accumulator on Stack
PHB	Push Data Bank Register on Stack
PHD	Push Direct Register on Stack
PHK	Push Program Bank Register on Stack
PHP	Push Processor Status on Stack
PHX	Push Index X on Stack
PHY	Push Index Y on Stack
PLA	Pull Accumulator from Stack
PLB	Pull Data Bank Register from Stack
PLD	Pull Direct Register from Stack
PLP	Pull Processor Status from Stack
PLX	Pull Index X from Stack
PLY	Pull Index Y form Stack
REP	Reset Status Bits
ROL	Rotate One Bit Left (Memory or Accumulator)
ROR	Rotate One Bit Right (Memory or Accumulator)
RTI	Return from Interrupt
RTL	Return from Subroutine Long
RTS	Return from Subroutine
SBC	Subtract Memory from Accumulator with Borrow
SEC	Set Carry Flag
SED	Set Decimal Mode
SEI	Set Interrupt Disable Status
SEP	Set Processor Status Bite
STA	Store Accumulator in Memory
STP	Stop the Clock
STX	Store Index X in Memory
STY	Store Index Y in Memory
STZ	Store Zero in Memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
TCD	Transfer C Accumulator to Direct Register
TCS	Transfer C Accumulator to Stack Pointer Register
TDC	Transfer Direct Register to C Accumulator
TRB	Test and Reset Bit
TSB	Test and Set Bit
TSC	Transfer Stack Pointer Register to C Accumulator
TSX	Transfer Stack Pointer Register to Index X
TXA	Transfer Index X to Accumulator
TXS	Transfer Index X to Stack Pointer Register
TXY	Transfer Index X to Index Y
TYA	Transfer Index Y to Accumulator
TYX	Transfer Index Y to Index X
WAI	Wait for Interrupt
WDM	Reserved for Future Use
XBA	Exchange B and A Accumulator
XCE	Exchange Carry and Emulation Bits

For alternate mnemonics, see Table 7.

TABLE 3. VECTOR LOCATIONS

E = 1		**E = 0**	
OOFFFE,F	—$\overline{IRQ}$/BRK Hardware/Software	OOFFEE,F	—$\overline{IRQ}$ Hardware
OOFFFC,D	—$\overline{RESET}$ Hardware	OOFFEC,D	—(Reserved)
OOFFFA,B	—$\overline{NMI}$ Hardware	OOFFEA,B	—$\overline{NMI}$ Hardware
OOFFF8,9	—$\overline{ABORT}$ Hardware	OOFFE8,9	—$\overline{ABORT}$ Hardware
OOFFF6,7	—(Reserved)	OOFFE6,7	—BRK Software
OOFFF4,5	—COP Software	OOFFE4,5	—COP Software

The VP output is low during the two cycles used for vector location access.
When an interrupt is executed, D = 0 and I = 1 in Status Register P.

TABLE 4. OPCODE MATRIX

MSD	LSD 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK s 2 8	ORA (d,x) 2 6	COP s 2 * 8	ORA d,s 2 * 4	TSB d 2 • 5	ORA d 2 3	ASL d 2 5	ORA [d] 2 * 6	PHP s 1 3	ORA # 2 2	ASL A 1 2	PHD s 1 * 4	TSB a 3 • 6	ORA a 3 4	ASL a 3 6	ORA al 4 * 5	0
1	BPL r 2 2	ORA (d),y 2 5	ORA (d) 2 • 5	ORA (d,s),y 2 * 7	TRB d 2 • 5	ORA d,x 2 4	ASL d,x 2 6	ORA [d],y 2 * 6	CLC i 1 2	ORA a,y 3 4	INC A 1 • 2	TCS i 1 * 2	TRB a 3 • 6	ORA a,x 3 4	ASL a,x 3 7	ORA al,x 4 * 5	1
2	JSR a 3 6	AND (d,x) 2 6	JSL al 4 * 8	AND d,s 2 * 4	BIT d 2 3	AND d 2 3	ROL d 2 5	AND [d] 2 * 6	PLP s 1 4	AND # 2 2	ROL A 1 2	PLD s 1 * 5	BIT a 3 4	AND a 3 4	ROL a 3 6	AND al 4 * 5	2
3	BMI r 2 2	AND (d),y 2 5	AND (d) 2 • 5	AND (d,s),y 2 * 7	BIT d,x 2 • 4	AND d,x 2 4	ROL d,x 2 6	AND [d],y 2 * 6	SEC i 1 2	AND a,y 3 4	DEC A 1 • 2	TSC i 1 * 2	BIT a,x 3 • 4	AND a,x 3 4	ROL a,x 3 7	AND al,x 4 * 5	3
4	RTI s 1 7	EOR (d,x) 2 6	WDM 2 * 2	EOR d,s 2 * 4	MVP xyc 3 * 7	EOR d 2 3	LSR d 2 5	EOR [d] 2 * 6	PHA s 1 3	EOR # 2 2	LSR A 1 2	PHK s 1 * 3	JMP a 3 3	EOR a 3 4	LSR a 3 6	EOR al 4 * 5	4
5	BVC r 2 2	EOR (d),y 2 5	EOR (d) 2 • 5	EOR (d,s),y 2 * 7	MVN xyc 3 * 7	EOR d,x 2 4	LSR d,x 2 6	EOR [d],y 2 * 6	CLI i 1 2	EOR a,y 3 4	PHY s 1 • 3	TCD i 1 * 2	JMP al 4 * 4	EOR a,x 3 4	LSR a,x 3 7	EOR al,x 4 * 5	5
6	RTS s 1 6	ADC (d,x) 2 6	PER s 3 * 6	ADC d,s 2 * 4	STZ d 2 • 3	ADC d 2 3	ROR d 2 5	ADC [d] 2 * 6	PLA s 1 4	ADC # 2 2	ROR A 1 2	RTL s 1 * 6	JMP (a) 3 5	ADC a 3 4	ROR a 3 6	ADC al 4 * 5	6
7	BVS r 2 2	ADC (d),y 2 5	ADC (d) 2 • 5	ADC (d,s),y 2 * 7	STZ d,x 2 • 4	ADC d,x 2 4	ROR d,x 2 6	ADC [d],y 2 * 6	SEI i 1 2	ADC a,y 3 4	PLY s 1 • 4	TDC i 1 * 2	JMP (a,x) 3 • 6	ADC a,x 3 4	ROR a,x 3 7	ADC al,x 4 * 5	7
8	BRA r 2 • 2	STA (d,x) 2 6	BRL rl 3 * 3	STA d,s 2 * 4	STY d 2 3	STA d 2 3	STX d 2 3	STA [d] 2 * 6	DEY i 1 2	BIT # 2 • 2	TXA i 1 2	PHB s 1 * 3	STY a 3 4	STA a 3 4	STX a 3 4	STA al 4 * 5	8
9	BCC r 2 2	STA (d),y 2 6	STA (d) 2 • 5	STA (d,s),y 2 * 7	STY d,x 2 4	STA d,x 2 4	STX d,y 2 4	STA [d],y 2 * 6	TYA i 1 2	STA a,y 3 5	TXS i 1 2	TXY i 1 * 2	STZ a 3 • 4	STA a,x 3 5	STZ a,x 3 • 5	STA al,x 4 * 5	9
A	LDY # 2 2	LDA (d,x) 2 6	LDX # 2 2	LDA d,s 2 * 4	LDY d 2 3	LDA d 2 3	LDX d 2 3	LDA [d] 2 * 6	TAY i 1 2	LDA # 2 2	TAX i 1 2	PLB s 1 * 4	LDY a 3 4	LDA a 3 4	LDX a 3 4	LDA al 4 * 5	A
B	BCS r 2 2	LDA (d),y 2 5	LDA (d) 2 • 5	LDA (d,s),y 2 * 7	LDY d,x 2 4	LDA d,x 2 4	LDX d,y 2 4	LDA [d],y 2 * 6	CLV i 1 2	LDA a,y 3 4	TSX i 1 2	TYX i 1 * 2	LDY a,x 3 4	LDA a,x 3 4	LDX a,y 3 4	LDA al,x 4 * 5	B
C	CPY # 2 2	CMP (d,x) 2 6	REP # 2 * 3	CMP d,s 2 * 4	CPY d 2 3	CMP d 2 3	DEC d 2 5	CMP [d] 2 * 6	INY i 1 2	CMP # 2 2	DEX i 1 2	WAI i 1 • 3	CPY a 3 4	CMP a 3 4	DEC a 3 6	CMP al 4 * 5	C
D	BNE r 2 2	CMP (d),y 2 5	CMP (d) 2 • 5	CMP (d,s),y 2 * 7	PEI s 2 * 6	CMP d,x 2 4	DEC d,x 2 6	CMP [d],y 2 * 6	CLD i 1 2	CMP a,y 3 4	PHX s 1 • 3	STP i 1 • 3	JML (a) 3 * 6	CMP a,x 3 4	DEC a,x 3 7	CMP al,x 4 * 5	D
E	CPX # 2 2	SBC (d,x) 2 6	SEP # 2 * 3	SBC d,s 2 * 4	CPX d 2 3	SBC d 2 3	INC d 2 5	SBC [d] 2 * 6	INX i 1 2	SBC # 2 2	NOP i 1 2	XBA i 1 * 3	CPX a 3 4	SBC a 3 4	INC a 3 6	SBC al 4 * 5	E
F	BEQ r 2 2	SBC (d),y 2 5	SBC (d) 2 • 5	SBC (d,s),y 2 * 7	PEA s 3 * 5	SBC d,x 2 4	INC d,x 2 6	SBC [d],y 2 * 6	SED i 1 2	SBC a,y 3 4	PLX s 1 • 4	XCE i 1 * 2	JSR (a,x) 3 * 6	SBC a,x 3 4	INC a,x 3 7	SBC al,x 4 * 5	F
MSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD

symbol	addressing mode	symbol	addressing mode
#	immediate	[d]	direct indirect long
A	accumulator	[d],y	direct indirect long indexed
r	program counter relative	a	absolute
rl	program counter relative long	a,x	absolute indexed (with x)
i	implied	a,y	absolute indexed (with y)
s	stack	al	absolute long
d	direct	al,x	absolute long indexed
d,x	direct indexed (with x)	d,s	stack relative
d,y	direct indexed (with y)	(d,s),y	stack relative indirect indexed
(d)	direct indirect	(a)	absolute indirect
(d,x)	direct indexed indirect	(a,x)	absolute indexed indirect
(d),y	direct indirect indexed	xyc	block move

Op Code Matrix Legend

INSTRUCTION MNEMONIC

BASE NO. BYTES

* = New 65C816/802 Opcodes
• = New 65C02 Opcodes
Blank = NMOS 6502 Opcodes

ADDRESSING MODE

BASE NO. CYCLES

TABLE 5.

	OPERATION	#	a	al	d	A	i	(d),y	[d],y	(d,x)	d,x	d,y	a,x	al,x	a,y	r	rl	(a)	(d)	[d]	(a,x)	s	d,s	(d,s),y	xyc	PROCESSOR STATUS CODE 7 6 5 4 3 2 1 0 N V M X D I Z C	MNE-MONIC E=0	E=1
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	N V 1 B D I Z C		
ADC	A + M + C → A	69	6D	6F	65			71	77	61	75		7D	7F	79				72	67			63	73		N V . . . . Z C	ADC	
AND	A∧M → A	29	2D	2F	25			31	37	21	35		3D	3F	39				32	27			23	33		N . . . . . Z .	AND	
ASL	C ← 15/7 0 ← 0		0E		06	0A					16		1E													N . . . . . Z C	ASL	
BCC	BRANCH IF C = 0															90										. . . . .	BCC	
BCS	BRANCH IF C = 1															B0										. . . . .	BCS	
BEQ	BRANCH IF Z = 1															F0										. . . . .	BEQ	
BIT	A∧M (NOTE 1)	89	2C		24						34		3C													M7 M6 . . . . Z .	BIT	
BMI	BRANCH IF N = 1															30										. . . . .	BMI	
BNE	BRANCH IF Z = 0															D0										. . . . .	BNE	
BPL	BRANCH IF N = 0															10										. . . . .	BPL	
BRA	BRANCH ALWAYS															80										. . . . .	•	BRA
BRK	BREAK (NOTE 2)																					00				. . . • 0 I . .		BRK
BRL	BRANCH LONG ALWAYS																82									. . . . .	*	BRL
BVC	BRANCH IF V = 0															50										. . . . .		BVC
BVS	BRANCH IF V = 1															70										. . . . .		BVS
CLC	0 → C						18																			 0		CLC
CLD	0 → D						D8																			. . . . 0 . .		CLD
CLI	0 → I						58																			. . . . 0 . .		CLI
CLV	0 → V						B8																			. 0		CLV
CMP	A-M	C9	CD	CF	C5			D1	D7	C1	D5		DD	DF	D9				D2	C7			C3	D3		N . . . . . Z C		CMP
COP	CO-PROCESSOR																					02				. . . . 0 I . .	*	COP
CPX	X-M	E0	EC		E4																					N . . . . . Z C		CPX
CPY	Y-M	C0	CC		C4																					N . . . . . Z C		CPY
DEC	DECREMENT		CE		C6	3A					D6		DE													N . . . . . Z .		DEC
DEX	X - 1 → X						CA																			N . . . . . Z .		DEX
DEY	Y - 1 → Y						88																			N . . . . . Z .		DEY
EOR	A∨M → A	49	4D	4F	45	1A		51	57	41	55		5D	5F	59				52	47			43	53		N . . . . . Z .		EOR
INC	INCREMENTS		EE		E6		E8				F6		FE													N . . . . . Z .		INC
INX	X + 1 → X						C8																			N . . . . . Z .		INX
INY	Y + 1 → Y																									N . . . . . Z .		INY
JML	JUMP LONG TO NEW LOC.																	DC								. . . . .	*	JML
JMP	JUMP TO NEW LOC.		4C	5C														6C			7C					. . . . .		JMP
JSL	JUMP LONG TO SUB.			22																						. . . . .		JSL
JSR	JUMP TO SUB.		20																		FC					. . . . .		JSR
LDA	M → A	A9	AD	AF	A5			B1	B7	A1	B5		BD	BF	B9				B2	A7		A3	B3			N . . . . . Z .		LDA
LDX	M → X	A2	AE		A6							B6			BE											N . . . . . Z .		LDX
LDY	M → Y	A0	AC		A4						B4		BC													N . . . . . Z .		LDY
LSR	0 → 15/7 0 → C		4E		46	4A					56		5E													0 . . . . . Z C		LSR
MVN	M → M BACKWARD																								54	. . . . .	*	MVN
MVP	M → M FORWARD																								44	. . . . .	*	MVP
NOP	NO OPERATION						EA																			. . . . .		NOP
ORA	A∨M → A	09	0D	0F	05			11	17	01	15		1D	1F	19				12	07			03	13		N . . . . . Z .		ORA
PEA	Mpc + 1, Mpc + 2 → Ms - 1, Ms S - 2 → S																					F4				. . . . .	*	PEA
PEI	M(d), M(d + 1) → Ms - 1, Ms S - 2 → S																					D4				. . . . .	*	PEI
PER	Mpc + rl, Mpc + rl + 1 → Ms - 1, Ms S - 2 → S																					62				. . . . .	*	PER
PHA	A → Ms, S - 1 → S																					48				. . . . .		PHA
PHB	DBR → Ms, S - 1 → S																					8B				. . . . .		PHB
PHD	D → Ms, Ms - 1, S - 2 → S																					0B				. . . . .	*	PHD
PHK	PBR → Ms, S - 1 → S																					4B				. . . . .	*	PHK
PHP	P → Ms, S - 1 → S																					08				. . . . .		PHP
PHX	X → Ms, S - 1 → S																					DA				. . . . .	•	PHX
PHY	Y → Ms, S - 1 → S																					5A				. . . . .	•	PHY
PLA	S + 1 → S, Ms → A																					68				N . . . . . Z .		PLA
PLB	S + 1 → S, Ms → DBR																					AB				N . . . . . Z .	*	PLB
PLD	S + 2 → S, Ms - 1, Ms → D																					2B				N . . . . . Z .	*	PLD
PLP	S + 1 → S, Ms → P																					28				N V M X D I Z C		PLP
PLX	S + 1 → S, Ms → X																					FA				N . . . . . Z .		PLX
PLY	S + 1 → S, Ms → Y																					7A				N . . . . . Z .		PLY
REP	M∧P → P	C2																								N V M X D I Z C	*	REP
ROL	C ← 15/7 0 ← C		2E		26	2A					36		3E													N . . . . . Z C		ROL
ROR	C → 15/7 0 → C		6E		66	6A					76		7E													N . . . . . Z C		ROR
RTI	RTRN FROM INT.																					40				N V M X D I Z C		RTI
RTL	RTRN FROM SUB. LONG																					6B				. . . . .	*	RTL
RTS	RTRN SUBROUTINE																					60				. . . . .		RTS
SBC	A - M - C → A	E9	ED	EF	E5			F1	F7	E1	F5		FD	FF	F9				F2	E7			E3	F3		N V . . . . Z C		SBC
SEC	1 → C						38																			 1		SEC
SED	1 → D						F8																			. . . . 1 . .		SED
SEI	1 → I						78																			. . . . 1 . .		SEI
SEP	M∨P → P	E2																								N V M X D I Z C	*	SEP
STA	A → M		8D	8F	85			91	97	81	95		9D	9F	99				92	87			83	93		. . . . .		STA
STP	STOP (1 → φ2)						DB																			. . . . .	•	STP
STX	X → M		8E		86							96														. . . . .		STX
STY	Y → M		8C		84						94															. . . . .		STY
STZ	00 → M		9C		64						74		9E													. . . . .	•	STZ
TAX	A → X						AA																			N . . . . . Z .		TAX
TAY	A → Y						A8																			N . . . . . Z .		TAY
TCD	C → D						5B																			N . . . . . Z .	*	TCD
TCS	C → S						1B																			. . . . .	*	TCS
TDC	D → C						7B																			N . . . . . Z .	*	TDC
TRB			1C		14																					. . . . . Z .	•	TRB
TSB	AVM → M		0C		04																					. . . . . Z .	•	TSB
TSC	S → C						3B																			. . . . .	*	TSC
TSX	S → X						BA																			N . . . . . Z .		TSX
TXA	X → A						8A																			N . . . . . Z .		TXA
TXS	X → S						9A																			. . . . .		TXS
TXY	X → Y						9B																			N . . . . . Z .	*	TXY
TYA	Y → A						98																			N . . . . . Z .		TYA
TYX	Y → X						BB																			N . . . . . Z .	*	TYX
WAI	0 → RDY						CB																			. . . . .	•	WAI
WDM	NO OPERATION (RESERVED)						42																			. . . . .	*	WDM
XBA	B ⟷ A						EB																			N . . . . . Z .	*	XBA
XCE	C ⟷ E						FB																			. . . . . E	*	XCE

TABLE 6. DETAILED INSTRUCTION OPERATION

ADDRESS MODE		CYCLE	VP	ML	VDA	VPA	ADDRESS BUS	DATA BUS	R/W
1. Immediate **#** (LDY,CPY,CPX,LDX,ORA, AND,EOR,ADC,BIT,LDA, CMP,SBC REP,SEP) (14 Op Codes) (2 and 3 bytes) (2 and 3 cycles)	(1)(8)	1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	1	PBR,PC+1	IDL	1
		2a.	1	1	0	1	PBR,PC+2	IDH	1
2a. Absolute **a** (BIT,STY,STZ,LDY, CPY,CPX,STX,LDX, ORA,AND,EOR,ADC, STA,LDA,CMP,SBC) (18 Op Codes) (3 bytes) (4 and 5 cycles)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	1	PBR,PC+1	AAL	1
		3.	1	1	0	1	PBR,PC+2	AAH	1
		4.	1	1	1	0	DBR,AA	Data Low	1/0
	(1)	4a.	1	1	1	0	DBR,AA+1	Data High	1/0
2b. Absolute (R-M-W) **a** (ASL,ROL,LSR,ROR DEC,INC,TSB,TRB) (6 Op Codes) (3 bytes) (6 and 8 cycles)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	1	PBR,PC+1	AAL	1
		3.	1	1	0	1	PBR,PC+2	AAH	1
		4.	1	0	1	0	DBR,AA	Data Low	1
	(1)	4a.	1	0	1	0	DBR,AA+1	Data High	1
	(3)	5.	1	0	0	0	DBR,AA+1	IO	1
	(1)	6a.	1	0	1	0	DBR,AA+1	Data High	0
		6.	1	0	1	0	DBR,AA	Data Low	0
2c. Absolute (JUMP) **a** (JMP)(4C) (1 Op Code) (3 bytes) (3 cycles)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	1	PBR,PC+1	NEW PCL	1
		3.	1	1	0	1	PBR,PC+2	NEW PCH	1
		1.	1	1	1	1	PBR, NEW PC	Op Code	1
2d. Absolute (Jump to subroutine) **a** (JSR) (1 Op Code) (3 bytes) (6 cycles) (different order from N6502)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	1	PBR,PC+1	NEW PCL	1
		3.	1	1	0	1	PBR,PC+2	NEW PCH	1
		4.	1	1	0	0	PBR,PC+2	IO	1
		5.	1	1	1	0	0,S	PCH	0
		6.	1	1	1	0	0,S-1	PCL	0
		1.	1	1	1	1	PBR,NEW PC	Next Op Code	1
★3a. Absolute Long **al** (ORA,AND,EOR,ADC STA,LDA,CMP,SBC) (8 Op Codes) (4 bytes) (5 and 6 cycles)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	1	PBR,PC+1	AAL	1
		3.	1	1	0	1	PBR,PC+2	AAH	1
		4.	1	1	0	1	PBR,PC+3	AAB	1
		5.	1	1	1	0	AAB,AA	Data Low	1/0
	(1)	5a.	1	1	1	0	AAB,AA+1	Data High	1/0
★3b. Absolute Long (JUMP) **al** (JMP) (1 Op Code) (4 bytes) (4 cycles)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	1	PBR,PC+1	NEW PCL	1
		3.	1	1	0	1	PBR,PC+2	NEW PCH	1
		4.	1	1	0	1	PBR,PC+3	NEW BR	1
		1.	1	1	1	1	NEW PBR,PC	Op Code	1
★3c. Absolute Long (Jump to Subroutine Long) **al** (JSL) (1 Op Code) (4 bytes) (7 cycles)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	1	PBR,PC+1	NEW PCL	1
		3.	1	1	0	1	PBR,PC+2	NEW PCH	1
		4.	1	1	1	0	0,S	PBR	0
		5.	1	1	0	0	0,S	IO	1
		6.	1	1	0	1	PBR,PC+3	NEW PBR	1
		7.	1	1	1	0	0,S-1	PCH	0
		8.	1	1	1	0	0,S-2	PCL	0
		1.	1	1	1	1	NEW PBR,PC	Next Op Code	1
4a. Direct **d** (BIT,STZ,STY,LDY, CPY,CPX,STX,LDX, ORA,AND,EOR,ADC, STA,LDA,CMP,SBC) (18 Op Codes) (2 bytes) (3,4 and 5 cycles)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	1	PBR,PC+1	DO	1
	(2)	2a.	1	1	0	0	PBR,PC+1	IO	1
		3.	1	1	1	0	0,D+DO	Data Low	1/0
	(1)	3a.	1	1	1	0	0,D+DO+1	Data High	1/0
4b. Direct (R-M-W) **d** (ASL,ROL,LSR,ROR DEC,INC,TSB,TRB) (6 Op Codes) (2 bytes) (5,6,7 and 8 cycles)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	1	PBR,PC+1	DO	1
	(2)	2a.	1	1	0	0	PBR,PC+1	IO	1
		3.	1	0	1	0	0,D+DO	Data Low	1
	(1)	3a.	1	0	1	0	0,D+DO+1	Data High	1
	(3)	4.	1	0	0	0	0,D+DO+1	IO	1
	(1)	5a.	1	0	1	0	0,D+DO+1	Data High	0
		5.	1	0	1	0	0,D+DO	Data Low	0
5. Accumulator **A** (ASL,INC,ROL,DEC,LSR,ROR) (6 Op Codes) (1 byte) (2 cycles)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	0	PBR,PC+1	IO	1
6a. Implied **i** (DEY, INY, INX, DEX, NOP, XCE, TYA, TAY,TXA, TXS, TAX,TSX,TCS,TSC,TCD, TDC,TXY,TYX,CLC,SEC, CLI,SEI,CLV,CLD,SED) (25 Op Codes) (1 byte) (2 cycles)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	0	PBR,PC+1	IO	1
★6b. Implied **i** (XBA) (1 Op Code) (1 byte) (3 cycles)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	0	PBR,PC+1	IO	1
		3.	1	1	0	0	PBR,PC+1	IO	1

ADDRESS MODE		CYCLE	VP	ML	VDA	VPA	ADDRESS BUS	DATA BUS	R/W
• 6c. Wait For Interrupt (WAI) (1 Op Code) (1 byte) (3 cycles)	(9)	1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	0	1	PBR,PC+1	IO	1
		3.	1	1	0	0	0	PBR,PC+1	IO	1
	IRQ,NMI	1.	1	1	1	1	1	PBR,PC+1	IRQ(BRK)	1
• 6d. Stop-The-Clock (STP) (1 Op Code) (1 byte) (3 cycles)		1.	1	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	0	1	PBR,PC+1	IO	1
	RES=1	3.	1	1	0	0	1	PBR,PC+1	IO	1
	RES=0	1c.	1	1	0	0	1	PBR,PC+1	RES(BRK)	1
	RES=0	1b.	1	1	0	0	1	PBR,PC+1	RES(BRK)	1
	RES=1	1a.	1	1	0	0	1	PBR,PC+1	RES(BRK)	1
See 21a Stack (Hardware interrupt)		1.	1	1	1	1	1	PBR,PC+1	BEGIN	1
7. Direct Indirect Indexed **(d),y** (ORA,AND,EOR,ADC, STA,LDA,CMP,SBC) (8 Op Codes) (2 bytes) (5,6,7 and 8 cycles)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	1	PBR,PC+1	DO	1
	(2)	2a.	1	1	0	0	PBR,PC+1	IO	1
		3.	1	1	1	0	0,D+DO	AAL	1
		4.	1	1	1	0	0,D+DO+1	AAH	1
	(4)	4a.	1	1	0	0	DBR,AAH,AAL+Y		1
		5.	1	1	1	0	DBR,AA+Y	Data Low	1/0
	(1)	5a.	1	1	1	0	DBR,AA+Y+1	Data High	1/0
8. Direct Indirect Indexed Long **[d],y** (ORA,AND,EOR,ADC, STA,LDA,CMP,SBC) (8 Op Codes) (2 bytes) (6,7 and 8 cycles)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	1	PBR,PC+1	DO	1
	(2)	2a.	1	1	0	0	PBR,PC+1	IO	1
		3.	1	1	1	0	0,D+DO	AAL	1
		4.	1	1	1	0	0,D+DO+1	AAH	1
		5.	1	1	1	0	0,D+DO+2	AAB	1
		6.	1	1	1	0	AAB,AA+Y	Data Low	1/0
	(1)	6a.	1	1	1	0	AAB,AA+Y+1	Data High	1/0
9. Direct Indexed Indirect **(d,x)** (ORA,AND,EOR,ADC, STA,LDA,CMP,SBC) (8 Op Codes) (2 bytes) (6,7 and 8 cycles)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	1	PBR,PC+1	DO	1
	(2)	2a.	1	1	0	0	PBR,PC+1	IO	1
		3.	1	1	0	0	PBR,PC+1	IO	1
		4.	1	1	1	0	0,D+DO+X	AAL	1
		5.	1	1	1	0	0,D+DO+X+1	AAH	1
		6.	1	1	1	0	DBR,AA	Data Low	1/0
	(1)	6a.	1	1	1	0	DBR,AA+1	Data High	1/0
10a. Direct,X **d,x** (BIT,STZ,STY,LDY, ORA,AND,EOR,ADC, STA,LDA,CMP,SBC) (11 Op Codes) (2 bytes) (4,5 and 6 cycles)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	1	PBR,PC+1	DO	1
	(2)	2a.	1	1	0	0	PBR,PC+1	IO	1
		3.	1	1	0	0	PBR,PC+1	IO	1
		4.	1	1	1	0	0,D+DO+X	Data Low	1/0
	(1)	4a.	1	1	1	0	0,D+DO+X+1	Data High	1/0
10b. Direct,X(R-M-W) **d,x** (ASL,ROL,LSR,ROR, DEC,INC) (6 Op Codes) (2 bytes) (6,7,8 and 9 cycles)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	1	PBR,PC+1	DO	1
	(2)	2a.	1	1	0	0	PBR,PC+1	IO	1
		3.	1	1	0	0	PBR,PC+1	IO	1
		4.	1	0	1	0	0,D+DO+X	Data Low	1
	(1)	4a.	1	0	1	0	0,D+DO+X+1	Data High	1
	(3)	5.	1	0	0	0	0,D+DO+X+1	IO	1
	(1)	6a.	1	0	1	0	0,D+DO+X+1	Data High	0
		6.	1	0	1	0	0,D+DO+X	Data Low	0
11. Direct,Y **d,y** (STX,LDX) (2 Op Codes) (2 bytes) (4,5 and 6 cycles)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	1	PBR,PC+1	DO	1
	(2)	2a.	1	1	0	0	PBR,PC+1	IO	1
		3.	1	1	0	0	PBR,PC+1	IO	1
		4.	1	1	1	0	0,D+DO+Y	Data Low	1/0
	(1)	4a.	1	1	1	0	0,D+DO+Y+1	Data High	1/0
12a. Absolute,X **a,x** (BIT,LDY,STZ, ORA,AND,EOR,ADC, STA,LDA,CMP,SBC) (11 Op Codes) (3 bytes) (4,5 and 6 cycles)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	1	PBR,PC+1	AAL	1
		3.	1	1	0	1	PBR,PC+2	AAH	1
	(4)	3a.	1	1	0	0	DBR,AAH,AAL+X		1
		4.	1	1	1	0	DBR,AA+X	Data Low	1/0
	(1)	4a.	1	1	1	0	DBR,AA+X+1	Data High	1/0
12b. Absolute,X(R-M-W) **a,x** (ASL,ROL,LSR,ROR, DEC,INC) (6 Op Codes) (3 bytes) (7 and 9 cycles)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	1	PBR,PC+1	AAL	1
		3.	1	1	0	1	PBR,PC+2	AAH	1
		4.	1	1	0	0	DBR,AAH,AAL+X		1
	(1)	5.	1	0	1	0	DBR,AA+X	Data Low	1
	(1)	5a.	1	0	1	0	DBR,AA+X+1	Data High	1
	(3)	6.	1	0	0	0	DBR,AA+X+1	IO	1
	(1)	7a.	1	0	1	0	DBR,AA+X+1	Data High	0
		7.	1	0	1	0	DBR,AA+X	Data Low	0
★13. Absolute Long,X **al,x** (ORA,AND,EOR,ADC, STA,LDA,CMP,SBC) (8 Op Codes) (4 bytes) (5 and 6 cycles)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	1	PBR,PC+1	AAL	1
		3.	1	1	0	1	PBR,PC+2	AAH	1
		4.	1	1	0	1	PBR,PC+3	AAB	1
		5.	1	1	1	0	AAB,AA+X	Data Low	1/0
	(1)	5a.	1	1	1	0	AAB,AA+X+1	Data High	1/0
14. Absolute,Y **a,y** (LDX,ORA,AND,EOR,ADC, STA,LDA,CMP,SBC) (9 Op Codes) (3 bytes) (4,5 and 6 cycles)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	1	PBR,PC+1	AAL	1
		3.	1	1	0	1	PBR,PC+2	AAH	1
	(4)	3a.	1	1	0	0	DBR,AAH,AAL+Y		1
		4.	1	1	1	0	DBR,AA+Y	Data Low	1/0
	(1)	4a.	1	1	1	0	DBR,AA+Y+1	Data High	1/0
15. Relative **r** (BPL,BMI,BVC,BVS,BCC, BCS,BNE,BEQ,BRA) (9 Op Codes) (2 bytes) (2,3 and 4 cycles)		1.	1	1	1	1	PBR,PC	Op Code	1
		2.	1	1	0	1	PBR,PC+1	Offset	1
	(5)	2a.	1	1	0	0	PBR,PC+1	IO	1
	(6)	2b.	1	1	0	0	PBR,PC+1	IO	1
		1.	1	1	1	1	PBR,PC+Offset	Op Code	1

TABLE 6. DETAILED INSTRUCTION OPERATION (CONT.)

	ADDRESS MODE		CYCLE	VP,	ML,	VDA,	VPA	ADDRESS BUS	DATA BUS	R/W
*16.	Relative Long rl		1.	1	1	1	1	PBR,PC	Op Code	1
	(BRL)		2.	1	1	0	1	PBR,PC+1	Offset Low	1
	(1 Op Code)		3.	1	1	0	1	PBR,PC+2	Offset High	1
	(3 bytes)		4.	1	1	0	0	PBR,PC+2	IO	1
	(4 cycles)		1.	1	1	1	1	PBR,PC+Offset	Op Code	1
17a.	Absolute Indirect (a)		1.	1	1	1	1	PBR,PC	Op Code	1
	(JMP)		2.	1	1	0	1	PBR,PC+1	AAL	1
	(1 Op Code)		3.	1	1	0	1	PBR,PC+2	AAH	1
	(3 bytes)		4.	1	1	1	0	0,AA	NEW PCL	1
	(5 cycles)		5.	1	1	1	0	0,AA+1	NEW PCH	1
			1.	1	1	1	1	PBR,NEW PC	Op Code	1
*17b.	Absolute Indirect (a)		1.	1	1	1	1	PBR,PC	Op Code	1
			2.	1	1	0	1	PBR,PC+1	AAL	1
	(JML)		3.	1	1	0	1	PBR,PC+2	AAH	1
	(1 Op Code)		4.	1	1	1	0	0,AA	NEW PCL	1
	(3 bytes)		5.	1	1	1	0	0,AA+1	NEW PCH	1
	(6 cycles)		6.	1	1	1	0	0,AA+2	NEW PBR	1
			1.	1	1	1	1	NEW PBR,PC	Op Code	1
• 18.	Direct Indirect (d)		1.	1	1	1	1	PBR,PC	Op Code	1
	(ORA,AND,EOR,ADC,		2.	1	1	0	1	PBR,PC+1	DO	1
	STA,LDA,CMP,SBC)	(2)	2a.	1	1	0	0	PBR,PC+1	IO	1
	(8 Op Codes)		3.	1	1	1	0	0,D+DO	AAL	1
	(2 bytes)		4.	1	1	1	0	0,D+DO+1	AAH	1
	(5,6 and 7 cycles)		5.	1	1	1	0	DBR,AA	Data Low	1/0
		(1)	5a.	1	1	1	0	DBR,AA+1	Data Low	1/0
*19.	Direct Indirect Long [d]		1.	1	1	1	1	PBR,PC	Op Code	1
	(ORA,AND,EOR,ADC		2.	1	1	0	1	PBR,PC+1	DO	1
	STA,LDA,CMP,SBC)	(2)	2a.	1	1	0	0	PBR,PC+1	IO	1
	(8 Op Codes)		3.	1	1	1	0	0,D+DO	AAL	1
	(2 bytes)		4.	1	1	1	0	0,D+DO+1	AAH	1
	(6,7 and 8 cycles)		5.	1	1	1	0	0,D+DO+2	AAB	1
			6.	1	1	1	0	AAB,AA	Data Low	1/0
		(1)	6a.	1	1	1	0	AAB,AA+1	Data High	1/0
20a.	Absolute Indexed Indirect (a,x)		1.	1	1	1	1	PBR,PC	Op Code	1
	(JMP)		2.	1	1	0	1	PBR,PC+1	AAL	1
	(1 Op Code)		3.	1	1	0	1	PBR,PC+2	AAH	1
	(3 bytes)		4.	1	1	0	0	PBR,PC+2	IO	1
	(6 cycles)		5.	1	1	0	1	PBR,AA+X	NEW PCL	1
			6.	1	1	0	1	PBR,AA+X+1	NEW PCH	1
			1.	1	1	1	1	PBR, NEW PC	Op Code	1
*20b.	Absolute Indexed Indirect (Jump to Subroutine Indexed Indirect) (a,x)		1.	1	1	1	1	PBR,PC	Op Code	1
			2.	1	1	0	1	PBR,PC+1	AAL	1
			3.	1	1	1	0	0,S	PCH	0
	(JSR)		4.	1	1	1	0	0,S-1	PCL	0
	(1 Op Code)		5.	1	1	0	1	PBR,PC+2	AAH	1
	(3 bytes)		6.	1	1	0	0	PBR,PC+2	IO	1
	(8 cycles)		7.	1	1	0	1	PBR,AA+X	NEW PCL	1
			8.	1	1	0	1	PBR,AA+X+1	NEW PCH	1
			1.	1	1	1	1	PBR,NEW PC	Next Op Code	1
21a.	Stack (Hardware Interrupts) s	(3)	1.	1	1	1	1	PBR,PC	IO	1
			2.	1	1	0	0	PBR,PC	IO	1
	(IRQ,NMI,ABORT,RES)	(7)	3.	1	1	1	0	0,S	PBR	0
	(4 hardware interrupts)		4.	1	1	1	0	0,S-1	PCH	0
	(0 bytes)		5.	1	1	1	0	0,S-2	PCL	0
	(7 and 8 cycles)		6.	1	1	1	0	0,S-3	P	0
			7.	0	1	1	0	0,VA	AAVL	1
			8.	0	1	1	0	0,VA+1	AAVH	1
			1.	1	1	1	1	0,AAV	Next Op Code	1
21b.	Stack (Software Interrupts) s	(3)	1.	1	1	1	1	PBR,PC	Op Code	1
			2.	1	1	0	1	PBR,PC+1	Signature	1
	(BRK,COP)	(7)	3.	1	1	1	0	0,S	PBR	0
	(2 Op Codes)		4.	1	1	1	0	0,S-1	PCH	0
	(2 bytes)		5.	1	1	1	0	0,S-2	PCL	0
	(7 and 8 cycles)		6.	1	1	1	0	0,S-3 (COP Latches)	P	0
			7.	0	1	1	0	0,VA	AAVL	1
			8.	0	1	1	0	0,VA+1	AAVH	1
			1.	1	1	1	1	0,AAV	Next Op Code	1
21c.	Stack (Return from Interrupt) s		1.	1	1	1	1	PBR,PC	Op Code	1
			2.	1	1	0	0	PBR,PC+1	IO	1
	(RTI)	(3)	3.	1	1	0	0	PBR,PC+1	IO	1
	(1 Op Code)		4.	1	1	1	0	0,S+1	P	1
	(1 byte)		5.	1	1	1	0	0,S+2	PCL	1
	(6 and 7 cycles)		6.	1	1	1	0	0,S+3	PCH	1
	(different order from N6502)	(7)	7.	1	1	1	0	0,S+4	PBR	1
			1.	1	1	1	1	PBR,PC	New Op Code	1
21d.	Stack (Return from Subroutine) s		1.	1	1	1	1	PBR,PC	Op Code	1
			2.	1	1	0	0	PBR,PC+1	IO	1
	(RTS)		3.	1	1	0	0	PBR,PC+1	IO	1
	(1 Op Code)		4.	1	1	1	0	0,S+1	PCL	1
	(1 byte)		5.	1	1	1	0	0,S+2	PCH	1
	(6 cycles)		6.	1	1	0	0	0,S+2	IO	1
			1.	1	1	1	1	PBR,PC	Op Code	1
*21e.	Stack (Return from Subroutine Long) s		1.	1	1	1	1	PBR,PC	Op Code	1
			2.	1	1	0	0	PBR,PC+1	IO	1
	(RTL)		3.	1	1	0	0	PBR,PC+1	IO	1
	(1 Op Code)		4.	1	1	1	0	0,S+1	NEW PCL	1
	(1 byte)		5.	1	1	1	0	0,S+2	NEW PCH	1
	(6 cycles)		6.	1	1	1	0	0,S+3	NEW PBR	1
			1.	1	1	1	1	NEW PBR,PC	Next Op Code	1

	ADDRESS MODE		CYCLE	VP,	ML,	VDA,	VPA	ADDRESS BUS	DATA BUS	R/W
21f.	Stack (Push) s		1.	1	1	1	1	PBR,PC	Op Code	1
	(PHP,PHA,PHY,PHX,		2.	1	1	0	0	PBR,PC+1	IO	1
	PHD,PHK,PHB)	(1)	3a.	1	1	1	0	0,S	Register High	1
	(7 Op Codes)		3.	1	1	1	0	0,S-1	Register Low	1
	(1 byte)									
	(3 and 4 cycles)									
21g.	Stack (Pull) s		1.	1	1	1	1	PBR,PC	Op Code	1
	(PLP,PLA,PLY,PLX,PLD,PLB)		2.	1	1	0	0	PBR,PC+1	IO	1
	(Different than N6502)		3.	1	1	0	0	PBR,PC+1	IO	1
	(6 Op Codes)		4.	1	1	1	0	0,S+1	Register Low	1
	(1 byte)	(1)	4a.	1	1	1	0	0,S+2	Register High	1
	(4 and 5 cycles)									
*21h.	Stack (Push Effective Indirect Address) s		1.	1	1	1	1	PBR,PC	Op Code	1
			2.	1	1	0	1	PBR,PC+1	DO	1
	(PEI)	(2)	2a.	1	1	0	0	PBR,PC+1	IO	1
	(1 Op Code)		3.	1	1	1	0	0,D+DO	AAL	1
	(2 bytes)		4.	1	1	1	0	0,D+DO+1	AAH	1
	(6 and 7 cycles)		5.	1	1	1	0	0,S	AAH	0
			6.	1	1	1	0	0,S-1	AAL	0
*21i.	Stack (Push Effective Absolute Address) s		1.	1	1	1	1	PBR,PC	Op Code	1
			2.	1	1	0	1	PBR,PC+1	AAL	1
	(PEA)		3.	1	1	0	1	PBR,PC+2	AAH	1
	(1 Op Code)		4.	1	1	1	0	0,S	AAH	0
	(3 bytes)		5.	1	1	1	0	0,S-1	AAL	0
	(5 cycles)									
*21j.	Stack (Push Effective Program Counter Relative Address) s		1.	1	1	1	1	PBR,PC	Op Code	1
			2.	1	1	0	1	PBR,PC+1	Offset Low	1
			3.	1	1	0	1	PBR,PC+2	Offset High	1
	(PER)		4.	1	1	0	0	PBR,PC+2	IO	1
	(1 Op Code)		5.	1	1	1	0	0,S	PCH+OFF+ CARRY	0
	(3 bytes)									
	(6 cycles)		6.	1	1	1	0	0,S-1	PCL+OFFSET	0
*22.	Stack Relative d,s		1.	1	1	1	1	PBR,PC	Op Code	1
	(ORA,AND,EOR,ADL,		2.	1	1	0	1	PBR,PC+1	SO	1
	STA,LDA,CMP,SDC)		3.	1	1	0	0	PBR,PC+1	IO	1
	(8 Op Codes)		4.	1	1	1	0	0,S+SO	Data Low	1/0
	(2 bytes)	(1)	4a.	1	1	1	0	0,S+SO+1	Data High	1/0
	(4 and 5 cycles)									
*23.	Stack Relative Indirect Indexed (d,s),y		1.	1	1	1	1	PBR,PC	Op Code	1
			2.	1	1	0	1	PBR,PC+1	SO	1
	(ORA,AND,EOR,ADC,		3.	1	1	0	0	PBR+PC+1	IO	1
	STA,LDA,CMP,SDC)		4.	1	1	1	0	0,S+SO	AAL	1
	(8 Op Codes)		5.	1	1	1	0	0,S+SO+1	AAH	1
	(2 bytes)		6.	1	1	0	0	0,S+SO+1	IO	1
	(7 and 8 Cycles)		7.	1	1	1	0	DBR,AA+Y	Data Low	1/0
		(1)	7a.	1	1	1	0	DBR,AA+Y+1	Data High	1/0
*24a.	Block Move Positive (forward) xyc (MVP) (1 Op Code) N-2 (3 bytes) Byte (7 cycles) C=2 x = Source Address y = Destination c =Number of Bytes to Move -1 x,y Decrement MVP is used when the destination start address is higher (more positive) than the source start address.		1.	1	1	1	1	PBR,PC	Op Code	1
			2.	1	1	0	1	PBR,PC+1	DBA	1
			3.	1	1	0	1	PBR,PC+2	SBA	1
			4.	1	1	1	0	SBA,X	Source Data	1
			5.	1	1	1	0	DBA,Y	Dest. Data	0
			6.	1	1	1	0	DBA,Y	IO	1
			7.	1	1	0	0	DBA,Y	IO	1
			1.	1	1	1	1	PBR,PC	Op Code	1
			2.	1	1	0	1	PBR,PC+1	DBA	1
			3.	1	1	0	1	PBR,PC+2	SBA	1
			4.	1	1	1	0	SBA,X-1	Source Data	1
			5.	1	1	1	0	DBA,Y-1	Dest. Data	0
			6.	1	1	0	0	DBA,Y-1	IO	1
			7.	1	1	0	0	DBA,Y-1	IO	1
	FFFFFF ▲ Dest. Start N Byte; Source Start Last; Dest. End C=0; Source End; 000000		1.	1	1	1	1	PBR,PC	Op Code	1
			2.	1	1	0	1	PBR,PC+1	DBA	1
			3.	1	1	0	1	PBR,PC+2	SBA	1
			4.	1	1	1	0	SBA,X-2	Source Data	1
			5.	1	1	1	0	DBA,Y-2	Dest. Data	0
			6.	1	1	0	0	DBA,Y-2	IO	1
			7.	1	1	0	0	DBA,Y-2	IO	1
			1.	1	1	1	1	PBR,PC+3	Next Op Code	1
*24b.	Block Move Negative (backward) xyc (MVN) (1 Op Code) N-2 (3 bytes) Byte (7 cycles) C=2 x = Source Address y = Destination c = Number of Bytes to Move -1 x,y Increment FFFFFF ▼ Source End N-1 Byte; Dest.End C=1; Source Start; Dest. Start; 000000 N Byte C=0 MVN is used when the destination start address is lower (more negative) than the source start address.		1.	1	1	1	1	PBR,PC	Op Code	1
			2.	1	1	0	1	PBR,PC+1	DBA	1
			3.	1	1	0	1	PBR,PC+2	SBA	1
			4.	1	1	1	0	SBA,X	Source Data	1
			5.	1	1	1	0	DBA,Y	Dest. Data	0
			6.	1	1	0	0	DBA,Y	IO	1
			7.	1	1	0	0	DBA,Y	IO	1
			1.	1	1	1	1	PBR,PC	Op Code	1
			2.	1	1	0	1	PBR,PC+1	DBA	1
			3.	1	1	0	1	PBR,PC+2	SBA	1
			4.	1	1	1	0	DBA,X-1	Source Data	1
			5.	1	1	1	0	DBA,Y-1	Dest. Data	0
			6.	1	1	0	0	DBA,Y-1	IO	1
			7.	1	1	0	0	DBA,Y-1	IO	1
			1.	1	1	1	1	PBR,PC	Op Code	1
			2.	1	1	0	1	PBR,PC+1	DBA	1
			3.	1	1	0	1	PBR,PC+2	SBA	1
			4.	1	1	1	0	SBA,X+2	Source Data	1
			5.	1	1	1	0	DBA,Y+2	Dest. Data	0
			6.	1	1	0	0	DBA,Y+2	IO	1
			7.	1	1	0	0	DBA,Y+2	IO	1
			1.	1	1	1	1	PBR,PC+3	Next Op Code	1

TABLE 5. NOTES

Notes:
1. Bit immediate N and V flags not affected. When M = 0, $M_{15} \rightarrow$ N and $M_{14} \rightarrow$V.
2. Break Bit (B) in Status register indicates hardware or software break.
3. ★ = New 65C816/802 Instructions
   ● = New 65C02 Instructions
   Blank = NMOS 6502

\+ Add
\- Subtract
∧ AND
V OR
⊻ Exclusive OR
•

TABLE 6. NOTES

Notes:
(1) Add 1 byte (for immediate only) for M=0 or X=0 (i.e. 16 bit data), add 1 cycle for M=0 or X=0
(2) Add 1 cycle for direct register low (DL) not equal 0.
(3) Special case for aborting instruction. This is the last cycle which may be aborted or the Status, PBR or DBR registers will be updated.
(4) Add 1 cycle for indexing across page boundaries, or write, or X=0. When X=1 or in the emulation mode, this cycle contains invalid addresses.
(5) Add 1 cycle if branch is taken.
(6) Add 1 cycle if branch is taken across page boundaries in 6502 emulation mode (E=1).
(7) Subtract 1 cycle for 6502 emulation mode (E=1).
(8) Add 1 cycle for REP,SEP.
(9) Wait at cycle 2 for 2 cycles after $\overline{NMI}$ or $\overline{IRQ}$ active input.

Abbreviations:
AAB Absolute Address Bank
AAH Absolute Address High
AAL Absolute Address Low
AAVH Absolute Address Vector High
AAVL Absolute Address Vector Low
C Accumulator
D Direct Register
DBA Destination Bank Address
DBR Data Bank Register
DO Direct Offset
IDH Immediate Data High
IDL Immediate Data Low
IO Internal Operation
P Status Register
PBR Program Bank Register
PC Program Counter
R-M-W Read-Modify-Write
S Stack Address
SBA Source Bank Address
SO Stack Offset
VA Vector Address
x,y Index Registers
★ = New 35C816/802 Addressing Modes
● = New 65C02 Addressing Modes
Blank = NMOS 6502 Addressing Modes

RECOMMENDED ASSEMBLER SYNTAX STANDARDS

DIRECTIVES

Assembler directives are those parts of the assembly language source program that give directions to the assembler; this includes the definition of data area and constants within a program. This standard excludes any definitions of assembler directives.

COMMENTS

An assembler should provide a way to use any line of the source program as a comment. The recommended way of doing this is to treat any blank line, or any line that starts with a semi-colon or an asterisk, as a comment. Other special characters may be used as well.

THE SOURCE LINE

Any line that causes the generation of a single VL65C816 or VL65C802 machine language instruction should be divided into four fields: a label field, the operation code, the operand, and the comment field.

The Label Field - The label field begins in column one of the line. A label must start with an alphabetic character, and may be followed by zero or more alphanumeric characters. An assembler may define an upper limit on the number of characters that can be in a label, as long as that upper limit is greater than or equal to six characters. An assembler may limit the alphabetic characters to upper-case characters if desired. If lower-case characters are allowed, they should be treated as identical to their upper-case equivalents. Other characters may be allowed in the label, as long as their use does not conflict with the coding of operand fields.

The Operation Code Field - The operation code consists of a three-character sequence (mnemonic) from table 2. It starts no sooner than column two of the line, or one space after the label if a label is coded.

Many of the operation codes in table 2 have duplicate mnemonics; when two or more machine language instructions have the same mnemonic, the assembler resolves the difference based on the operand.

If an assembler allows lower-case letters in labels, it must also allow lower case letters in mnemonics. When lower-case letters are used in the mnemonic, they are treated as equivalent to the upper-case counterpart. Thus, the mnemonics LDA, lda, and LdA must all be recognized, and are equivalent.

In addition to the mnemonics shown in table 2, an assembler may provide the alternative mnemonics shown in table 7.

SJL should be recognized as equivalent to JSR when it is specified with a long absolute address. JML is equivalent to JMP with long addressing force.

The Operand Field - The operand field may start no sooner than one space after the operation code field. The assembler must be capable of at least 24-bit address calculations. The assembler should be capable of specifying addresses as labels, integer constants, and hexadecimal constants. The assembler must allow addition and subtraction in the operand field. Labels are recognized by the fact that they start with alphabetic characters. Decimal numbers are recognized as containing only the decimal digits 0 through 9. Hexadecimal constants shall be recognized by prefixing the constant with a dollar sign ($) character, followed by zero or more of either the decimal digits or the hexadecimal digits A through F. If lower case letters are allowed in the label field, then they are also allowed as hexadecimal digits.

All constants, no matter what their format, provide at least enough precision to specify all values that can be represented by a 24-bit signed or unsigned integer represented in two's complement notation.

Table 9 shows the operand formats that are recognized by the assembler. The symbol **d** is a label or value that the assembler can recognize as being less than #100. The symbol **a** is a label or value which the assembler can recognize as greater than $FF but less than $10000; the symbol **al** is a label or value that the assembler can recognize as being greater than $FFFF. The symbol EXT is a label that cannot be located by the assembler at the time the instruction is assembled. Unless instructed otherwise, an assembler assumes that EXT labels are two bytes long. The symbols r and rl are 8- and 16-bit signed displacements calculated by the assembler.

Note that the operand does not determine whether or not immediate addressing loads one or two bytes; this is determined by the setting of the status register. This forces the requirement for a directive or directives that tell the assembler to generate one or two bytes of space for immediate loads. The directives provided must allow separate settings for the accumulator and index registers.

The assembler shall use the <, >, and ^ characters after the # character in an immediate address to specify which byte or bytes are to be selected from the value of the operand. Any calculations in the operand must be performed before the byte selection takes place. Table 8 defines the action taken by each operand by showing the effect of the operator on an address. The column that shows a two-byte immediate value shows the bytes in the order in which they appear in memory. The coding of the operand is for an asembler that uses 32 bit address calculations, showing the way that the address should be reduced to a 24 bit value.

In any location in an operand in which an address, or expression resulting in an address, can be coded, the assembler recognizes the prefix characters <, |, and >, which force one-byte (direct page), two-byte (absolute) or three-byte (long absolute) addressing. In cases in which the addressing mode is not forced, the assembler shall assume that the address is two bytes unless the assembler is able to determine the type of addressing required by context, in which case that addressing mode is used. Addresses are truncated without error if an addressing mode is forced that does not require the entire value of the address. For example:

```
LDA     $0203
LDA     $010203
```

are completely equivalent. If the addressing mode is not forced, and the type of addressing cannot be determined from context, the assembler assumes that a two-byte address is to be used. If an instruction does not have a short addressing mode (as in LDA, which has no direct page indexed by Y) and a short address is used in the operand, the assembler automatically extends the address by padding the most significant bytes with zeroes in order to extend the address to the length needed. As with immediate addressing, any expression evaluation takes place before the address is selected; thus, the address selection character is only used once, before the address of expression.

The exclamation point (!) character should be supported as an alternative to the vertical bar (|).

A long indirect address is indicated in the operand field of an instruction by surrounding the direct page address where the indirect address is found by square brackets; direct page addresses that contains 16-bit addresses are indicated by being surrounded by parentheses.

The operands of a block move instruction are specified as source bank, destination band (the opposite order of the object bytes generated).

Comment Field -The comment field may start no sooner than one space after the operation code field or operand code field or operand field, depending on instruction type.

TABLE 7. ALTERNATIVE MNEMONICS

Standard	Alias
BCC	BLT
BCS	BGE
CMP A	CMA
DEC A	DEA
INC A	INA
JSL	JSR
JML	JMP
TCD	TAD
TCS	TAS
TDC	TDA
TSC	TSA
XBA	SWA

TABLE 8. BYTE SELECTION OPERATOR

Operand	One Byte Result	Two Byte Result	
#$01020304	04	04	03
#<$01020304	04	04	03
#>$01020304	03	03	02
#^$01020304	02	02	01

TABLE 9. ADDRESS MODE FORMATS

Addressing Mode	Format
Immediate	#d
	#a
	#al
	#EXT
	#<d
	#<a
	#<al
	#<EXT
	#>d
	#>a
	#>al
	#>EXT
	#^d
	#^a
	#^al
	#^EXT
Absolute	!d
	!a
	a
	!al
	!EXT
	EXT
Absolute Long	>d
	>a
	>al
	al
	>EXT
Direct Page	d
	<d
	<a
	<al
	<EXT
Accumulator	A
Implied Addressing	(no operand)
Direct Indirect Indexed	(d),y
	(<d),y
	(<a),y
	(<al),y
	(<EXT),y
Direct Indirect Indexed Long	[d],y
	[<d],y
	[<a],y
	[<al],y
	[<EXT],y
Direct Indexed Indirect	(d,x)
	(<d,x)
	(<a,x)
	(<al,x)
	(<EXT,x)
Direct Indexed by X	d,x
	<d,x
	<a,x
	<al,x
	<EXT,x
Direct Indexed by Y	d,y
	<d,y
	<a,y
	<al,y
	<EXT,y
Absolute Indexed by X	d,x
	!d,x
	a,x
	!a,x
	!al,x
	!EXT,x
	EXT,x

Addressing Mode	Format	
Absolute Indexed by Y	!d,y	
	d,y	
	a,y	
	!a,y	
	!al,y	
	!EXT,y	
	EXT,y	
Absolute Long Indexed by X	>d,x	
	>a,x	
	>al,x	
	al,x	
	>EXT,x	
Program Counter Relative and Program Counter Relative Long	d	(the assembler calculates **r** and **rl**)
	a	
	al	
	EXT	
Absolute Indirect	(d)	
	(!d)	
	(a)	
	(!a)	
	(!al)	
	(EXT)	
Direct Indirect	(d)	
	(<a)	
	(<al)	
	(<EXT)	
Direct Indirect Long	[d]	
	[<a]	
	[<al]	
	[<EXT]	
Absolute Indexed	(d,x)	
	(!d,x)	
	(a,x)	
	(!a,x)	
	(!al,x)	
	(EXT,x)	
	(!EXT,x)	
Stack Addressing	(no operand)	
Stack Relative Indirect Indexed	(d,s),y	
	(<d,s),y	
	(<a,s),y	
	(<al,s),y	
	(<EXT,s),y	
Block Move	d,d	
	d,a	
	d,al	
	d,EXT	
	a,d	
	a,a	
	a,al	
	a,EXT	
	al,d	
	al,a	
	al,al	
	al,EXT	
	EXT,d	
	EXT,a	
	EXT,al	
	EXT,EXT	

Note: The alternate ! (exclamation point) is used in place of the | (vertical bar).

TABLE 10. ADDRESSING MODE SUMMARY

Address Mode	Instruction Times In Memory Cycles		Memory Utilization In Number of Program Sequence Bytes	
	Original 8 Bit NMOS 6502	New 65C816	Original 8 Bit NMOS 6502	New 65C816
1. Immediate	2	2(3)	2	2(3)
2. Absolute	4(5)	4(3,5)	3	3
3. Absolute Long	—	5(3)	—	4
4. Direct	3(5)	3(3,4,5)	2	2
5. Accumulator	2	2	1	1
6. Implied	2	2	1	1
7. Direct Indirect Indexed (d),y	5(1)	5(1,3,4)	2	2
8. Direct Indirect Indexed Long [d], y	—	6(3,4)	—	2
9. Direct Indexed Indirect (d,x)	6	6(3,4)	2	2
10. Direct, X	4(5)	4(3,4,5)	2	2
11. Direct, Y	4	4(3,4)	2	2
12. Absolute, X	4(1,5)	4(1,3,5)	3	3
13. Absolute Long, X	—	5(3)	—	4
14. Absolute, Y	4(1)	4(1,3)	3	3
15. Relative	2(1,2)	2(2)	2	2
16. Relative Long	—	3(2)	—	3
17. Absolute Indirect (Jump)	5	5	3	3
18. Direct Indirect	—	5(3,4)	—	2
19. Direct Indirect Long	—	6(3,4)	—	2
20. Absolute Indexed Indirect (Jump)	—	6	—	3
21. Stack	3-7	3-8	1-3	1-4
22. Stack Relative	—	4(3)	—	2
23. Stack Relative Indirect Indexed	—	7(3)	—	2
24. Block Move X, Y, C (Source, Destination, Block Length)	—	7	—	3

NOTES:
1. Page boundary, add 1 cycle if page boundary is crossed when forming address.
2. Branch taken, add 1 cycle if branch is taken.
3. M = 0 or X = 0, 16 bit operation, add 1 cycle, add 1 byte for immediate.
4. Direct register low (DL) not equal zero, add 1 cycle.
5. Read-Modify-Write, add 2 cycles for M = 1, add 3 cycles for M = 0.

ADDRESSING PREFACE

The VL65C816 is capable of directly addressing 16M Bytes of memory. This address space has special significance within certain addressing modes.

RESET AND INTERRUPT VECTORS

The Reset and Interrupt vectors use the majority of the fixed addresses between 00FFE0 and 00FFFF.

STACK

The stack may use memory from 000000 to 00FFFF. The effective address of Stack and Stack Relative addressing modes is always within this range.

DIRECT

The Direct addressing modes are usually used to store memory registers and pointers. The effective address generated by Direct, Direct,X and Direct,Y addressing modes is always in Bank 0 (000000-00FFFF).

PROGRAM ADDRESS SPACE

The Program Bank Register is not affected by the Relative, Relative Long, Absolute, Absolute Indirect, and Absolute Indexed Indirect addressing modes or by incrementing the Program Counter from FFFF. The only instructions that affect the Program Bank Register are: RTI, RTL, JML, JSL, and JMP Absolute Long. Program code may exceed 64K bytes, although code segments may not span bank boundaries.

DATA ADDRESS SPACE

The data address space is contiguous throughout the 16M Byte address space. Words, arrays, records, or any data structures may span 64K Byte bank boundaries with no compromise in code efficiency. The following addressing modes generate 24-bit effective addresses:

- Direct Indexed Indirect (d,x)
- Direct Indirect Indexed (d), y
- Direct Indirect (d)
- Direct Indirect Long [d]
- Direct Indirect Long Indexed [d], y
- Absolute a
- Absolute a, x
- Absolute a, y
- Absolute Long al
- Absolute Long Indexed al, x
- Stack Relative Indirect Indexed (d), y

The following addressing modes are available for use in the VL65C802 and VL65C816 microprocessors. The "long" addressing modes may be used with the VL65C802; however, the high byte of the address is not available to the hardware. Detailed descriptions of the 24 addressing modes are given in the following section.

ADDRESSING MODES

1. Immediate Addressing—#

The operand is the second byte (second and third bytes when in the 16-bit mode) of the instruction.

2. Absolute—a

With Absolute addressing the second and third bytes of the instruction form the low-order 16 bits of the effective address. The Data Bank Register contains the high-order 8 bits of the operand address.

Instruction:	opcode	addrl	addrh
Operand Address:	DBR	addrh	addrl

3. Absolute Long—al

The second, third, and fourth byte of the instruction form the 24-bit effective address.

Instruction:	opcode	addrl	addrh	baddr
Operand Address:	baddr	addrh	addrl	

4. Direct—d

The second byte of the instruction is added to the Direct Register (D) to form the effective address. An additional cycle is required when the Direct Register is not page aligned (DL not equal 0). The Bank register is always 0.

Instruction:	opcode	offset
		Direct Register
	+	offset
Operand Address:	00	effective address

5. Accumulator—A

This form of addressing always uses a single byte instruction. The operand is the Accumulator.

6. Implied—i

Implied addressing uses a single byte instruction. The operand is implicitly defined by the instruction.

7. Direct Indirect Indexed—(d),y

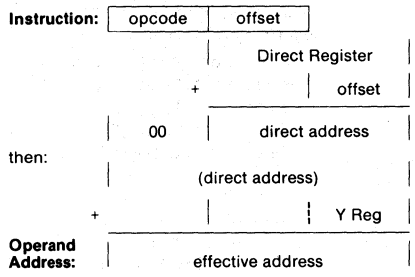
This address mode is often referred to as Indirect,Y. The second byte of the instruction is added to the Direct Register (D). The 16-bit contents of this memory location is then combined with the Data Bank register to form a 24-bit base address. The Y Index Register is added to the base address to form the effective address.

Instruction:	opcode	offset
		Direct Register
	+	offset
	00	direct address
then:		
	00	(direct address)
	+ DBR	
		base address
	+	Y Reg
Operand Address:		effective address

8. Direct Indirect Long Indexed—[d],y

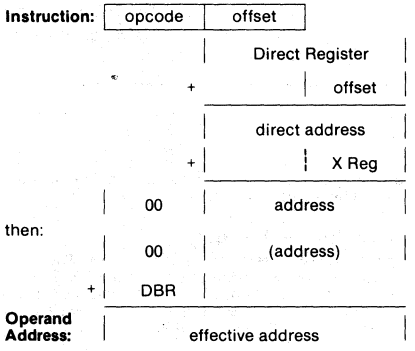
With this addressing mode, the 24-bit base address is pointed to by the sum of the second byte of the instruction and the Direct Register. The effective address is this 24-bit base address plus the Y Index Register.

ADDRESSING MODES (Cont.)



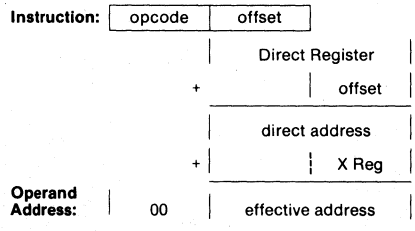
9. Direct Indexed Indirect—(d,x)

This address mode is often referred to as Indirect,X. The second byte of the instruction is added to the sum of the Direct Register and the X Index Register. The result points to the low-order 16 bits of the effective address. The Data Bank Register contains the high-order 8 bits of the effective address.



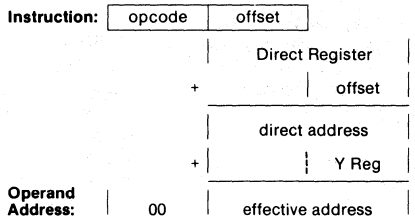
10. Direct Indexed With X—d,x

The second byte of the instruction is added to the sum of the Direct Register and the X Index Register to form the 16-bit effective address. The operand is always in Bank 0.



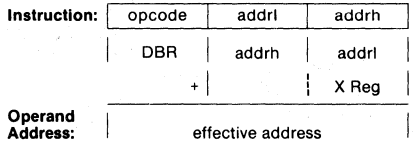
11. Direct Indexed With Y—d,y

The second byte of the instruction is added to the sum of the Direct Register and the Y Index Register to form the 16-bit effective address. The operand is always in Bank 0.



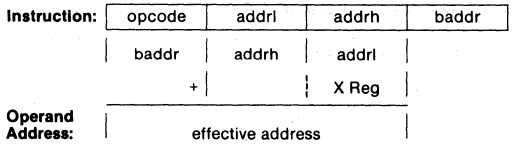
12. Absolute Indexed With X—a,x

The second and third bytes of the instruction are added to the X Index Register to form the low-order 16 bits of the effective address. The Data Bank Register contains the high-order 8 bits of the effective address.



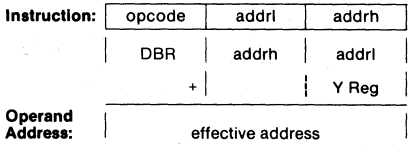
13. Absolute Long Indexed With X—al,x

The second, third and fourth bytes of the instruction form a 24-bit base address. The effective address is the sum of this 24-bit address and the X Index Register.



14. Absolute Indexed With Y—a,y

The second and third bytes of the instruction are added to the Y Index Register to form the low-order 16 bits of the effective address. The Data Bank Register contains the high-order 8 bits of the effective address.



15. Program Counter Relative—r

This address mode, referred to as Relative Addressing, is used only with the Branch instructions. If the condition being tested is met, the second byte of the instruction is added to the Program Counter, which has been updated to point to the opcode of the next instruction. The offset is a signed 8-bit quantity in the range from -128 to 127. The Program Bank Register is not affected.

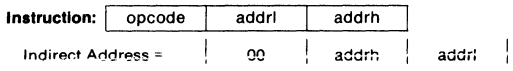
16. Program Counter Relative Long—rl

This address mode, referred to as Relative Long Addressing, is used only with the Unconditional Branch Long instruction (BRL) and the Push Effective Relative instruction (PER). The second and third bytes of the instruction are added to the Program Counter, which has been updated to point to the opcode of the next instruction. With the branch instruction, the Program Counter is loaded with the result. With the Push Effective Relative instruction, the result is stored on the stack. The offset is a signed 16-bit quantity in the range from -32768 to 32767. The Program Bank Register is not affected.

ADDRESSING MODES (Cont.)

17. Absolute Indirect—(a)

The second and third bytes of the instruction form an address to a pointer in Bank 0. The Program Counter is loaded with the first and second bytes at this pointer. With the Jump Long (JML) instruction, the Program Bank Register is loaded with the third byte of the pointer.



New PC = (indirect address)

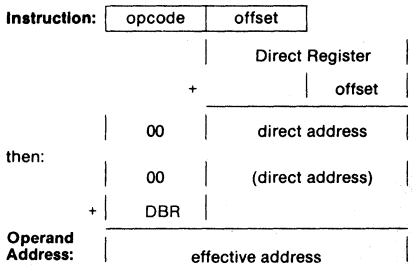
with JML:

New PC = (indirect address)

New PBR = (indirect address +2)

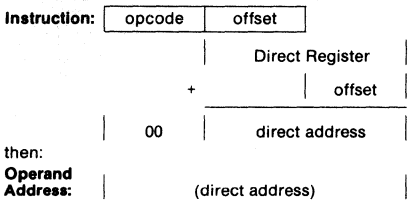
18. Direct Indirect—(d)

The second byte of the instruction is added to the Direct Register to form a pointer to the low-order 16 bits of the effective address. The Data Bank Register contains the high-order 8 bits of the effective address.



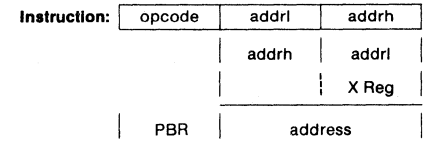
19. Direct Indirect Long—[d]

The second byte of the instruction is added to the Direct Register to form a pointer to the 24-bit effective address.



20. Absolute Indexed Indirect—(a,x)

The second and third bytes of the instruction are added to the X Index Register to form a 16-bit pointer in Bank 0. The contents of this pointer are loaded in the Program Counter. The Program Bank Register is not changed.



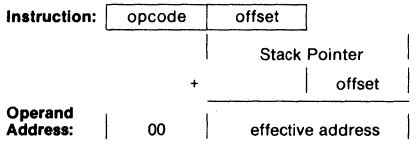
PC = (address)

21. Stack—s

Stack addressing refers to all instructions that push or pull data from the stack, such as Push, Pull, Jump to Subroutine, Return from Subroutine, Interrupts, and Return from Interrupt. The bank address is always 0. Interrupt Vectors are always fetched from Bank 0.

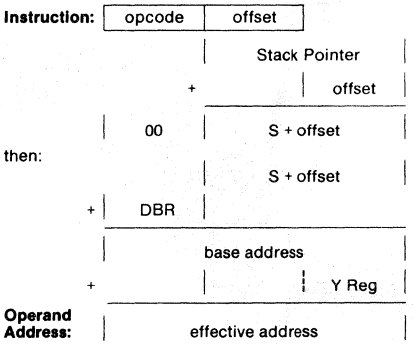
22. Stack Relative—d,s

The low-order 16 bits of the effective address is formed from the sum of the second byte of the instruction and the Stack Pointer. The high-order 8 bits of the effective address is always zero. The relative offset is an unsigned 8-bit quantity in the range of 0 to 255.



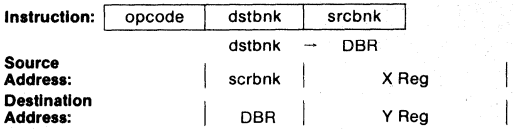
23. Stack Relative Indirect Indexed—(d,s),y

The second byte of the instruction is added to the Stack Pointer to form a pointer to the low-order 16-bit base address in Bank 0. The Data Bank Register contains the high-order 8 bits of the base address. The effective address is the sum of the 24-bit base address and the Y Index Register.



24. Block Source Bank, Destination Bank—xyc

This addressing mode is used by the Block Move instructions. The second byte of the instruction contains the high-order 8 bits of the destination address. The Y index Register contains the low-order 16 bits of the destination address. The third byte of the instruction contains the high-order 8 bits of the source address. The X Index Register contains the low-order 16 bits of the source address. The C Accumulator contains one less than the number of bytes to move. The second byte of the block move instructions is also loaded into the Data Bank Register.



Increment (MVN) or decrement (MVP) X and Y.

Decrement C (if greater than zero), then PC+3 → PC.

TABLE 11. VL65C802 TIMING CHARACTERISTICS TA = 0°C to 70°C, VDD = 5.0 V ± 5%

		2 MHz		4 MHz		6 MHz		8 MHz		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Cycle Time	tCYC	500	DC	250	DC	167	DC	125	DC	nS
Clock Pulse Width Low	tPWL	0.240	10	0.120	10	0.080	10	0.060	10	μS
Clock Pulse Width High	tPWH	240	∞	120	∞	80	∞	60	∞	nS
Fall Time, Rise Time	tF, tR	—	10	—	10	—	5	—	5	nS
Delay Time, $\phi 2$ (IN) to $\phi 1$ (OUT)	tD$\phi 1$	—	20	—	20	—	20	—	20	nS
Delay Time, $\phi 2$ (IN) to $\phi 2$ (OUT)	tD$\phi 2$	—	40	—	40	—	40	—	40	nS
Address Hold Time	tAH	10	—	10	—	10	—	10	—	nS
Address Setup Time	tADS	—	100	—	75	—	60	—	40	nS
Access Time	tACC	365	—	130	—	87	—	70	—	nS
Read Data Hold Time	tDHR	10	—	10	—	10	—	10	—	nS
Read Data Setup Time	tDSR	40	—	30	—	20	—	15	—	nS
Write Data Delay Time	tMDS	—	100	—	70	—	60	—	40	nS
Write Data Hold Time	tDHW	10	—	10	—	10	—	10	—	nS
Processor Control Setup Time	tPCS	40	—	30	—	20	—	15	—	nS
Processor Control Hold Time	tPCH	10	—	10	—	10	—	10	—	nS
Capacitive Load (Address, Data, and R/W)	CEXT	—	100	—	100	—	35	—	35	pF

FIGURE 3. VL65C802 TIMING DIAGRAM

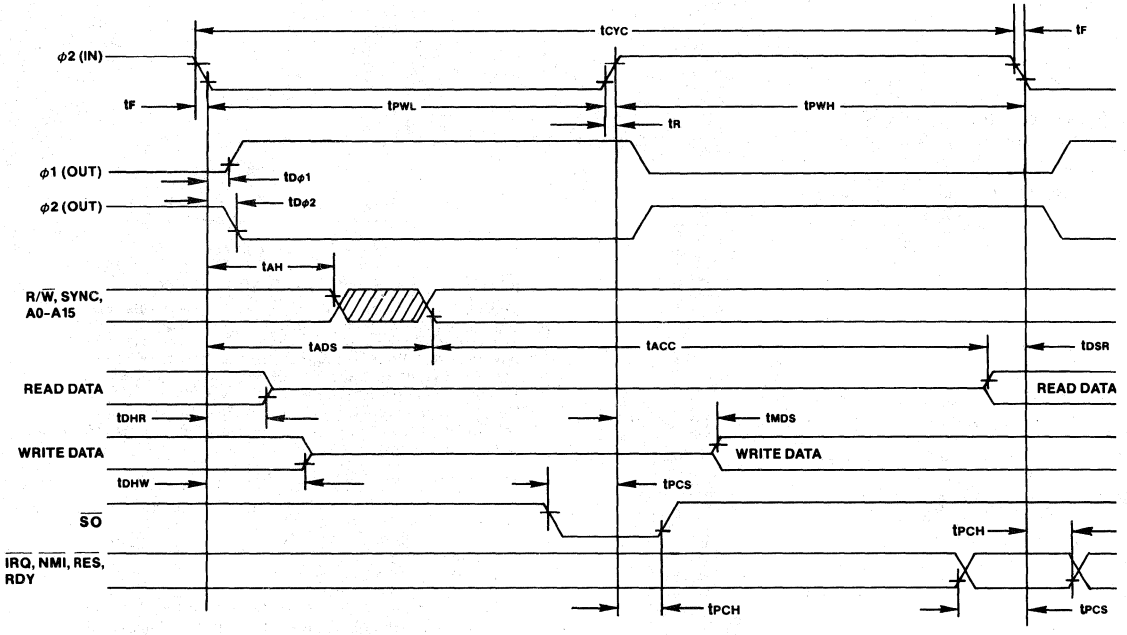
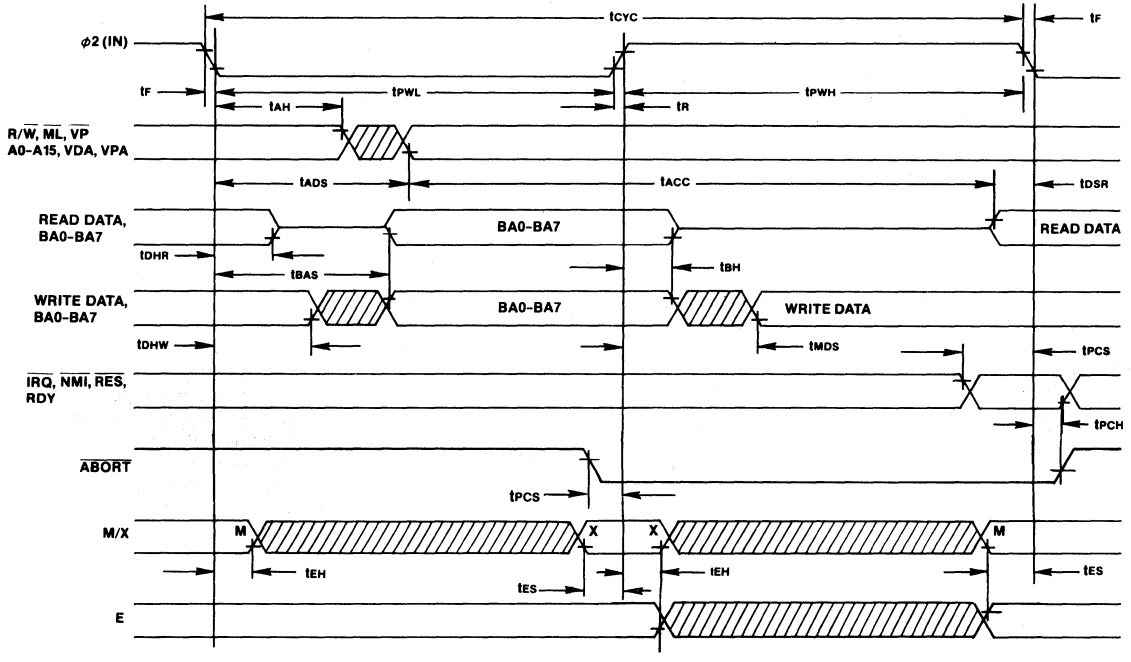


TABLE 12. VL65C816 TIMING CHARACTERISTICS TA = 0°C to 70°C, VDD = 5.0 V ± 5%

		2 MHz		4 MHz		6 MHz		8 MHz		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Cycle Time	tCYC	500	DC	250	DC	167	DC	125	DC	nS
Clock Pulse Width Low	tPWL	0.240	10	0.120	10	0.080	10	0.060	10	μS
Clock Pulse Width High	tPWH	240	∞	120	∞	80	∞	60	∞	nS
Fall Time, Rise Time	tF, tR	—	10	—	10	—	5	—	5	nS
A0–A15 Hold Time	tAH	10	—	10	—	10	—	10	—	nS
A0–A15 Setup Time	tADS	—	100	—	75	—	60	—	40	nS
BA0–BA7 Hold Time	tBH	10	—	10	—	10	—	10	—	nS
BA0–BA7 Setup Time	tBAS	—	100	—	90	—	65	—	45	nS
Access Time	tACC	365	—	130	—	87	—	70	—	nS
Read Data Hold Time	tDHR	10	—	10	—	10	—	10	—	nS
Read Data Setup Time	tDSR	40	—	30	—	20	—	15	—	nS
Write Data Delay Time	tMDS	—	100	—	70	—	60	—	40	nS
Write Data Hold Time	tDHW	10	—	10	—	10	—	10	—	nS
Processor Control Setup Time	tPCS	40	—	30	—	20	—	15	—	nS
Processor Control Hold Time	tPCH	10	—	10	—	10	—	10	—	nS
E,MX Output Hold Time	tEH	10	—	10	—	5	—	5	—	nS
E,MX Output Setup Time	tES	50	—	50	—	25	—	15	—	nS
Capacitive Load (Address, Data, and R/W)	CEXT	—	100	—	100	—	35	—	35	pF
BE to High Impedance State	tBHZ	—	30	—	30	—	30	—	30	nS
BE to Valid Data	tBVD	—	30	—	30	—	30	—	30	nS

FIGURE 4. VL65C816 TIMING DIAGRAM



USER INFORMATION

STACK ADDRESSING

When in the Native mode, the Stack Register may use memory locations 000000 to 00FFFF. The effective address of Stack, Stack Relative and Stack Relative Indirect Indexed addressing modes is always within this range. In the Emulation mode, the Stack address range is 000100 to 0001FF. The following opcodes and addressing modes increment or decrement beyond this range when accessing two or three bytes:

JSL; JSR(a,x); PEA; PEI; PER; PHD; PLD; RTL; d,s; (d,s),y

DIRECT ADDRESSING

The Direct Addressing modes are often used to access memory registers and pointers. The effective address generated by Direct; Direct,X and Direct,Y addressing modes are always in the Native mode range 000000 to 00FFFF. When in the Emulation mode, the Direct addressing range is 000000 to 0000FF, except for [Direct] and [Direct],Y addressing modes and the PEI instruction, which increment from 0000FE or 0000FF into Stack area.

When in the Emulation mode and DH is not equal to zero, the Direct addressing range is 00DH00 to 00DHFF, except for [Direct] and [Direct],Y addressing modes and the PEI instruction which increment from 00DHFE or 00DHFF into the next higher page.

When in the Emulation mode and DL is not equal to zero, the direct addressing range is 000000 to 00FFFF.

ABSOLUTE INDEXED ADDRESSING (VL65C816 ONLY)

The Absolute Indexed addressing modes are used to address data outside the Direct addressing range. The VL65C02 and VL65C802 addressing range is 0000 to FFFF. Indexing from page FFXX may result in a 00YY data fetch when using the VL65C02 or VL65C802. In contrast, indexing from page ZZFFXX may result in ZZ+1,00YY when using the VL65C816.

$\overline{\text{ABORT}}$ INPUT (VL65C816 ONLY)

$\overline{\text{ABORT}}$ should be held low for a period not to exceed one cycle. Also, if $\overline{\text{ABORT}}$ is held low during the Abort Interrupt sequence, the Abort Interrupt will be aborted. It is not recommended to abort the Abort Interrupt. The $\overline{\text{ABORT}}$ internal latch is cleared during the second cycle of the Abort Interrupt. Asserting the $\overline{\text{ABORT}}$ input after the following instruction cycles causes registers to be modified:

- Read-Modify-Write: Processor Status Register modified if $\overline{\text{ABORT}}$ is asserted after a modify cycle.
- RTI: Processor Status Register modified if $\overline{\text{ABORT}}$ is asserted after cycle 3.
- $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$, $\overline{\text{ABORT}}$ BRK, COP: When $\overline{\text{ABORT}}$ is asserted after cycle 2, PBR and DBR become 00 (Emulation mode) or PBRbecomes 00 (Native mode).

The Abort Interrupt has been designed for virtual memory systems. For this reason, asynchronous $\overline{\text{ABORT}}$s may cause undesirable results due to the above conditions.

VDA AND VPA (VL65C816 ONLY)

When VDA or VPA are high and during all write cycles, the Address Bus is always valid. VDA and VPA should be used to qualify all memory cycles. Note that when VDA and VPA are both low, invalid addresses may be generated. The Page and Bank addresses could also be invalid. This will be due to low-byte addition only. The cycle when only low-byte addition occurs is an optional cycle for instructions that read memory when the Index Register consists of eight bits. This optional cycle becomes a standard cycle for the Store instruction, all instructions using the 16-bit Index Register mode, and the Read-Modify-Write instruction when using 8- or 16-bit Index Register modes.

APPLE II, IIe, IIc, AND II+ DISK SYSTEMS (VL65C816 ONLY)

VDA and VPA should not be used to qualify addresses during disk operation on Apple systems. Consult your Apple representative for hardware/software configurations.

DB/BA OPERATION (WHEN RDY IS PULLED LOW -VL65C816 ONLY)

When RDY is low, the Data Bus is held in the data transfer state (i.e., ø2 high). The Bank address external transparent latch should be latched when the ø2 clock or RDY is low.

M/X OUTPUT (VL65C816 ONLY)

The M/X output reflects the value of the M and X bits of the processor Status Register. The REP, SEP, and PLP instructions may change the state of the M and X bits. Note that the M/X output is invalid during the instruction cycle following REP, SEP, and PLP instruction execution. This cycle is used as the opcode fetch cycle of the next instruction.

INSTRUCTIONS

Opcodes - It should be noted that all opcodes function in all modes of operation. However, some instructions and addressing modes are intended for VL65C816 24-bit addressing and are therefore less useful for the VL65C802. The following instructions and addressing modes are primarily intended for VL65C816 use:

JSL; RTL; [d]; [d],y; JMP al; JML; al; al,x

The following instructions may be used with VL65C802 even though a Bank Address is not multiplexed on the Data Bus:

PHK; PHB; PLB

The following instructions have limited use in the Emulation mode:

- The REP and SEP instructions cannot modify the M and X bits when in the Emulation mode. In this mode the M and X bits are always high (logic 1).
- When in the Emulation mode, the MVP and MVN instructions use the X and Y Index Registers for the memory address. Also, the MVP and MVN instructions can only move data within the memory range 0000 (Source Bank) to 00FF (Destination Bank) for the VL65C816, and 0000 to 00FF for the VL65C802.

USER INFORMATION (CONT.)

Indirect Jumps-The JMP (a) and JML (a) instructions use the direct Bank for indirect addressing, while JMP (a,x) and JSR (a,x) use the Program Bank for indirect address tables.

Switching Modes-When switching from the Native mode to the Emulation mode, the X and M bits of the Status Register are set high (logic 1), the high byte of the Stack is set to 01, and the high bytes of the X and Y Index Registers are set to 00. To save previous values, these bytes must always be stored before changing modes. Note that the low byte of the S, X, and Y Registers and the low and high bytes of the Accumulator (A and B) are not affected by a mode change.

How hardware interrupts, BRK, and COP instructions affect the Program Bank and the Data Bank Registers-when in the Native mode, the Program Bank register (PBR) is cleared to 00 when a hardware interrupt, BRK or COP is executed. In the Native mode, the previous PBR contents are automatically saved.

Note that a Return from Interrupt (RTI) should always be executed from the same mode that originally generated the interrupt.

Binary Mode-The Binary mode is set whenever a hardware or software interrupt is executed. The D flag within the Status Register is cleared to zero.

WAI Instruction-The WAI instruction pulls RDY low and places the processor in the WAI low-power mode. $\overline{NMI}$, $\overline{IRQ}$, or RESET terminate the WAI condition and transfer control to the interrupt handler routine. Note that an $\overline{ABORT}$ input aborts the WAI instruction, but does not restart the processor. When the Status Register 1 flag is set ($\overline{IRQ}$ disabled), the $\overline{IRQ}$ interrupt causes the next instruction (following the WAI instruction) to be executed without going to the $\overline{IRQ}$ interrupt handler. This method results in the highest speed response to an $\overline{IRQ}$ input. When an interrupt is received after an $\overline{ABORT}$ that occurs during the WAI instruction, the processor return to the WAI instruction. Other than $\overline{RES}$ (highest priority), $\overline{ABORT}$ is the next-highest priority, followed by $\overline{NMI}$ or $\overline{IRQ}$ interrupts.

STP Instruction-The STP instruction disables the ø2 clock to all circuitry. When disabled, the ø2 clock is held in the high state. In this case, the Data Bus remains in the data transfer state and the Bank address is not multiplexed onto the Data Bus. Upon executing the STP instruction, the $\overline{RES}$ signal is the only input that can restart the processor. The processor is restarted by enabling the ø2 clock, which occurs on the falling edge of the $\overline{RES}$ input. Note that the external oscillator must be stable and operating properly before $\overline{RES}$ goes high.

COP Signatures-Signatures 00-7F may be user defined, while signatures 80-FF are reserved.

RDY Pulled During Write-The NMOS 6502 does not stop during a write operation. In contrast, both the VL65C02 and the VL65C816 do stop during write operations. The VL65C802 stops during a write when in the Native mode, but does not stop when in the Emulation mode.

MVN and MVP Affects on the Data Bank Register -The MVN and MVP instructions change the Data Bank Register to the value of the second byte of the instruction (destination bank address).

INTERRUPTS

Interrupt Priorities-The following interrupt priorities are in effect should more than one interrupt occur at the same time:

$\overline{RES}$	Highest
$\overline{ABORT}$	
$\overline{NMI}$	
$\overline{IRQ}$	Lowest

TRANSFERS

Transfers from 8-Bit to 16-Bit, or 16-Bit to 8-Bit, Registers - All transfers from one register to another result in a full 16-bit output from the source register. The Destination Register size determines the number of bits actually stored in the destination register and the values stored in the processor Status Register. The following are always 16-bit transfers, regardless of the accumulator size:

TCS; TSC; TCD; TDC

Stack Transfers-When in the Emulation mode, a 01 is forced into SH. In this case, the B Accumulator is not loaded into SH during a TCS instruction. When in the Native mode, the B Accumulator is transfered to SH. Note that in both the Emulation and Native modes, the full 16 bits of the Stack Register are transferred to the A, B, and C Accumulators, regardless of the state of the M bit in the Status Register.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to +150°C
Supply Voltage to Ground Potential	-0.3 V to +7.0 V
Applied Input Voltage	-0.3 V to VDD + 0.3 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device under these or any conditions other than those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains input protection against damage due to high static voltages or electric fields. However, precautions should be taken to avoid application of voltages higher than the maximum rating.

DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ± 5%

Parameter	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}			
RES, RDY, IRQ, Data, SO, BE,		2.0	V_{DD} + 0.3	V
φ2 (IN), NMI, ABORT		0.7 V_{DD}	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}			
RES, RDY, IRQ, Data, SO, BE,		-0.3	0.8	V
φ2 (IN), NMI, ABORT		-0.3	0.2	V
Input Leakage Current (V_{IN} = 0 to V_{DD})	I_{IN}			
RES, NMI, RDY, IRQ, SO, BE, ABORT (Internal Pullup)		-100	1	μA
φ2 (IN)		-1	1	μA
Address, Data, R/W (Off State, BE = 0)		-10	10	μA
Output High Voltage (I_{OH} = -100μA)	V_{OH}			
SYNC, Data, Address, R/W, ML, VP, M/X, E, VDA, VPA,				
φ1 (OUT), φ2 (OUT)		0.7 V_{DD}	—	V
Output Low Voltage (I_{OL} = 1.6mA)	V_{OL}			
SYNC, Data, Address, R/W, ML, VP, M/X, E, VDA, VPA,				
φ1 (OUT), φ2 (OUT)		—	0.4	V
Supply Current (No Load)	I_{DD}		4	mA/MHz
Standby Current (No Load, Data Bus = V_{SS} or V_{DD}	I_{SB}	—		
RES, NMI, IRQ, SO, BE, ABORT, φ2 = V_{DD})			10	μA
Capacitance (V_{IN} = 0V, T_A = 25°C, f = 2 MHz)				
Logic, φ2 (IN)	C_{IN}	—	10	pF
Address, Data, R/W (Off State)	C_{TS}	—	15	pF

VL86C010

32-BIT REDUCED INSTRUCTION SET COMPUTER

FEATURES

- 32-bit internal architecture
- 32-bit external data bus
- 64M-byte linear address space
- Bus timing optimized for standard DRAM usage with page mode operation
- 32M-byte/second bus bandwidth
- Simple, powerful instruction set providing an excellent high-level language compiler target
- Hardware support for virtual memory systems
- Low interrupt latency for real-time application requirements
- Full CMOS implementation results in low power consumption
- Single 5 V ± 5% operation
- 84-pin JEDEC Type-B leadless chip carrier or plastic leaded chip carrier (PLCC)

DESCRIPTION

The VL86C010 Acorn RISC Machine (ARM) is a full 32-bit general-purpose microprocessor designed using reduced instruction set computer (RISC) methodologies. The processor is targeted for the microcomputer, graphics, industrial, and controller markets for use in stand-alone or embedded systems. Applications in which the processor is useful include laser printers, graphics engines, N.C. machines, and any other systems requiring fast real-time response to external interrupt sources and high processing throughput.

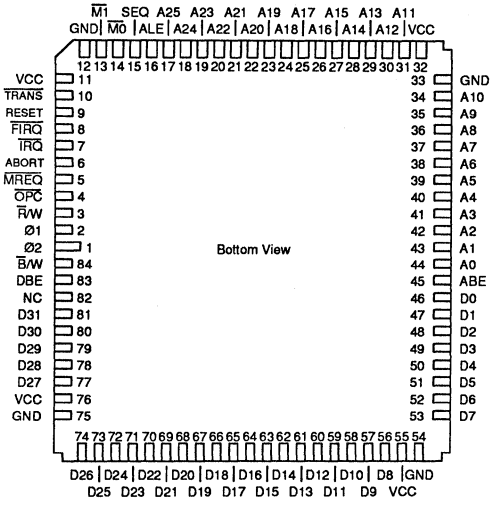
The VL86C010 features a 32-bit data bus, 25 registers of 32 bits each, a load-store architecture, a partially overlapping register set, 3 µs worst-case interrupt latency, conditional instruction execution, a 26-bit linear address space, and an average instruction execution rate of from three to four million instructions per second (MIPS). Additionally, the processor supports two addressing modes: program counter (PC) and base register relative. The ability to do pre- and post-indexing allows stacks and queues to be easily implemented in software. All instructions are 32 bits long (aligned on word boundaries), with register-to-register operations executing in one cycle. The two data types supported are 8-bit bytes and 32-bit words.

Using a load-store architecture simplifies the execution unit of the processor, since only a few instructions deal directly with memory and the rest operate register-to-register. Load and store multiple register instructions provide enhanced performance, making context switches faster and exploiting sequential memory access modes.

The processsor supports two types of interrupts that differ in priority and register usage. The lowest latency is provided by the fast interrupt request (FIRQ), which is used primarily for I/O to peripheral devices. The other interrupt type (IRQ) is used for interrupt routines that do not demand low-latency service or where the overhead of a full-context switch is small compared with the interrupt process execution time.

PIN DIAGRAM

JEDEC Type-B Ceramic Leadless Chip Carrier

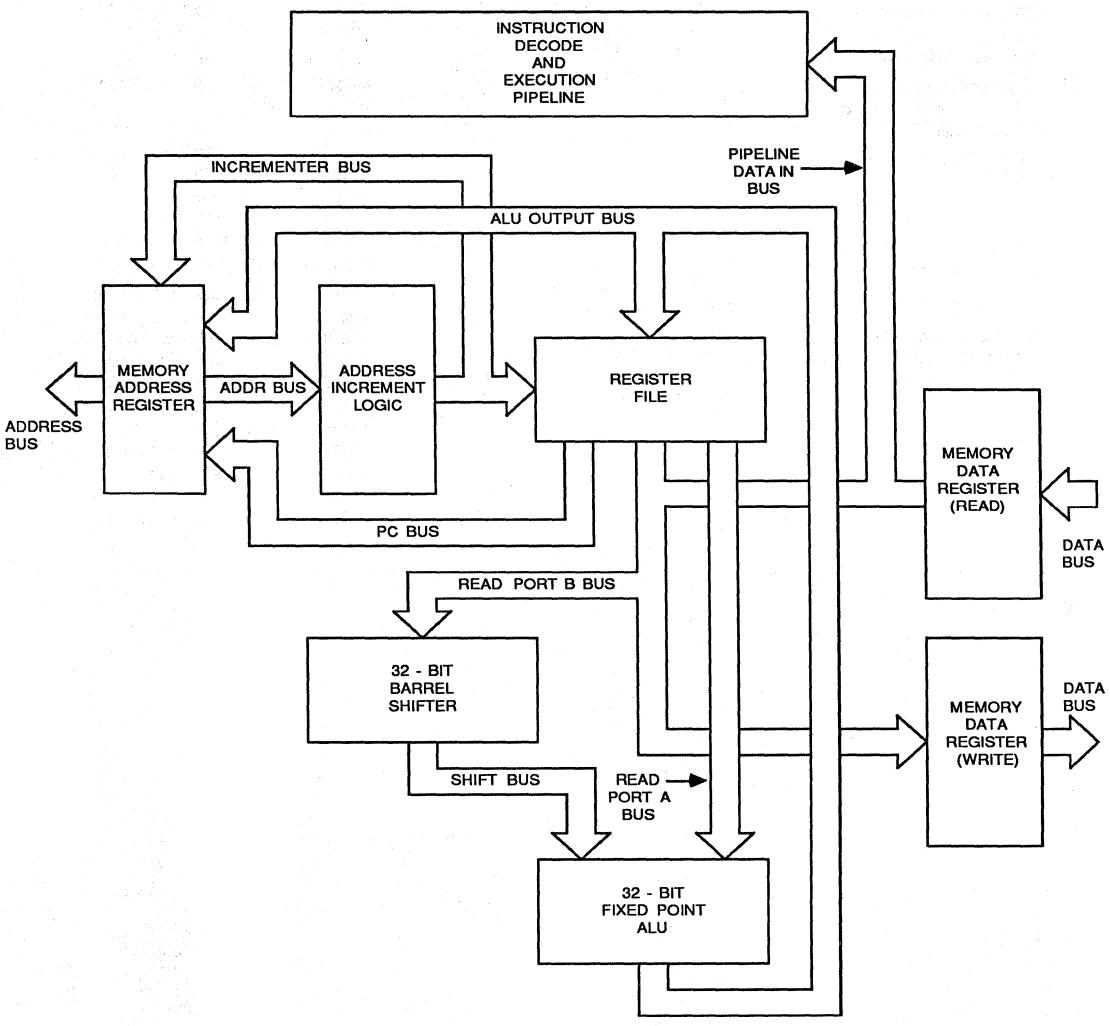


ORDER INFORMATION

Part Number	Clock Frequency	Package
VL86C010-04QC	4 MHz	Plastic Leaded Chip Carrier
VL86C010-04LC		JEDEC Type-B Ceramic Carrier
VL86C010-08QC	8 MHz	Plastic Leaded Chip Carrier
VL86C010-08LC		JEDEC Type-B Ceramic Carrier

Note: Operating temperature range: 0°C to +70°C.

BLOCK DIAGRAM



SIGNAL DESCRIPTIONS

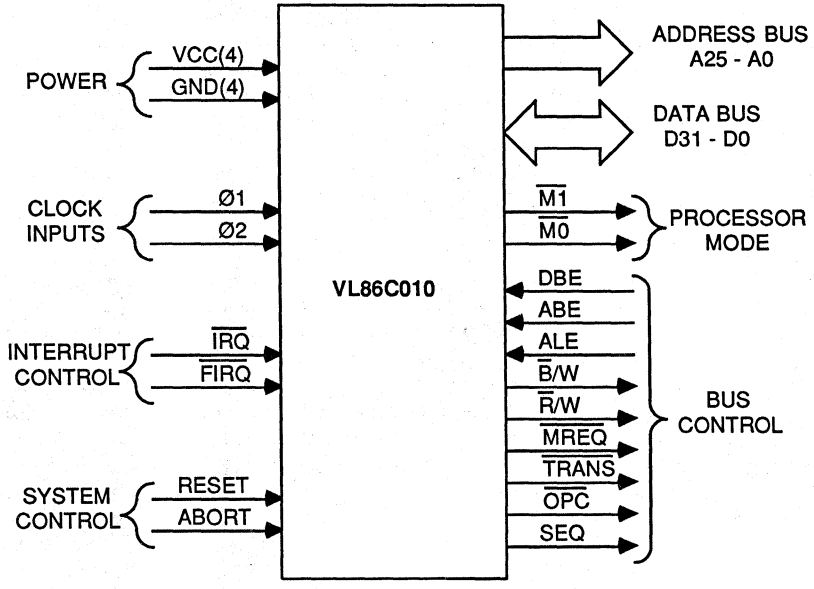
Signal Name	Pin Number (1)	Signal Description
Ø1, Ø2	2,1	Processor Clock Ø1 and Ø2 Inputs - These two inputs provide the clock to the circuit. In order to minimze clock skew, these inputs are not buffered internally and therefore must swing monotonically between GND and VCC without overshoot.The clocks must be non-overlapping and should be driven directly by 74HCXX outputs.
$\overline{IRQ}$	7	Interrupt Request Input - This is the normal interrupt request pin. It may be asserted asynchronously to cause the processor to be interrupted. It is active LIW.
$\overline{FIRQ}$	8	Fast Interrupt Request Input - This interrupt request line has a higher priority than $\overline{IRQ}$, but otherwise is the same. It, too, is active LOW.
RESET	9	Reset Input - This is the reset signal for the processor. While active, the processor will execute no-ops until the signal goes inactive, from which point execution starts at the reset vector location. This signal is active HIGH.
ABORT	6	Abort Input - This signal can be used to abort the current bus cycle being executed by the processor. Typically it is connected to a memory management unit to control accesses for protection. The abort signal is active HIGH.
D0 - D31	46 - 53, 56 - 74, 77 - 81	Data 0 - Data 31 - This is the 32-bit bi directional data bus used to transfer data to and from the memory. These lines are three-state and active HIGH.
DBE	83	Data Bus Enable Input - This is the asynchronous three-state control signal for controlling the drivers of the data bus. When asserted, the data bus is enabled. This signal is active HIGH.
$\overline{B/W}$	84	Byte / Word Output - This early warning signal (note 2) indicates to the memory system that the current fetch is a byte, rather than a word, fetch. It is asserted during the last portion of the cycle preceding the cycle that will require a byte fetch. When asserted (LOW) the memory system should deal with bytes. It is active LOW.
$\overline{M0}$, $\overline{M1}$	14, 13	Mode 0,1 Outputs - These two signals are used to indicate the current operating mode of the processor. They can be used as address space modifiers to increase the address space, or to assist a memory management unit in offering various protection modes. The lines are active LOW and the inverse of bits 0,1 of the processor status register. $\overline{M0}$ $\overline{M1}$ MODE 0 0 Supervisor 0 1 IRQ 1 0 FIRQ 1 1 USER
A0 - A25	44 - 34, 31 - 11	Address 0 - Address 25 Outputs - These are the 26 address lines. A0 and A1 are byte addresses and should be ignored except during byte memory cycles. During word transfers the current mode value will appear on these signals. The address lines are three-state and active HIGH.
ABE	45	Address Bus Enable Input - This is the asynchronous tri-state control signal for controlling the drivers of the address bus. When asserted the address bus is enabled. The signal is active high.
ALE the	16	Address Latch Enable Input- This signal is used to control internal transparent latches on the address outputs. When ALE is HIGH, the address outputs change during phase 2 to value required for the next cycle. Direct interfacing to ROMs requires address lines to be stable until the end of phase 2. Holding ALE LOW until the end of phase 2 will latch the address outputs for ROM cycles. Systems that do not directly interface to ROMs may tie ALE HIGH.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number (1)	Signal	Description
$\overline{R/W}$	3		R/W Output - This is the read / write signal from the processor. When asserted (LOW) it indicates that the processor is performing a read operation. When negated, (HIGH) the processor is performing a write operation. This signal is an early warning signal (note 2) and is active LOW.
$\overline{MREQ}$	5		Next Memory Cycle Start Output - This is an early warning indicator (note 2) that is asserted before the processor will start a memory cycle during the next clock phase. This signal is active LOW.
$\overline{TRANS}$	10		Translate Enable Output - This signal, when asserted by the processor, tells a memory management unit that translation should be done on the current address. When negated it indicates that the address should pass through untranslated. This signal is active LOW.
$\overline{OPC}$	4		Instruction Fetch Output - This early warning signal (note 2), when asserted, indicates that the current bus cycle is an instruction fetch. This signal is active LOW.
SEQ	15		Next Address Sequential Output- This early warning signal (note 2) is asserted when the processor will generate a sequential address during the next memory cycle. It may be used to control fast memory access modes. This signal is active HIGH.

Notes:
1 Pin numbers are for JEDEC Type-B leadless chip carrier only.
2 Early warning signals are asserted during the last portion of the cycle preceding the cycle for which they will be used.

FUNCTIONAL PINOUTS



FUNCTIONAL DESCRIPTION

The philosophy of RISC processor design is based on the idea that some processing functions can be moved from hardware to software, with the result that the simplified hardware can actually execute functions in software faster than with complicated hardware. Analysis done several years ago at major research centers has shown that a processor and compiler combination can replace the traditional processor-alone architectures. One of the sad historical facts of the 16-bit processor world is that, after chip designers spent many man-months figuring out how to implement universally acceptable complicated instructions to do such things as link to a subroutine, few compiler writers actually took advantage of these complex instructions. In fact, most compilers only use a fraction of the instructions and addressing modes of traditional computer architectures.

In addition, the customer pays dearly for the unused silicon required to implement these instructions. The customer pays for the inefficient utilization in both cost of the processor and in lower performance since the silicon spent for complex instruction decoding and micro-sequencing could have been used for additional pipelining, larger register sets, or other special-purpose hardware that can be used efficiently. If the addition of a new instruction causes all instructions to execute 10% slower due to internal processor delays, the new instruction had better be used more than 10% of the time, otherwise overall performance has been sacrificed. This makes an argument for simple performance-oriented architectures that are more dependent on compiler technology to implement less frequently used instructions.

A BETTER MEASURE OF PERFORMANCE

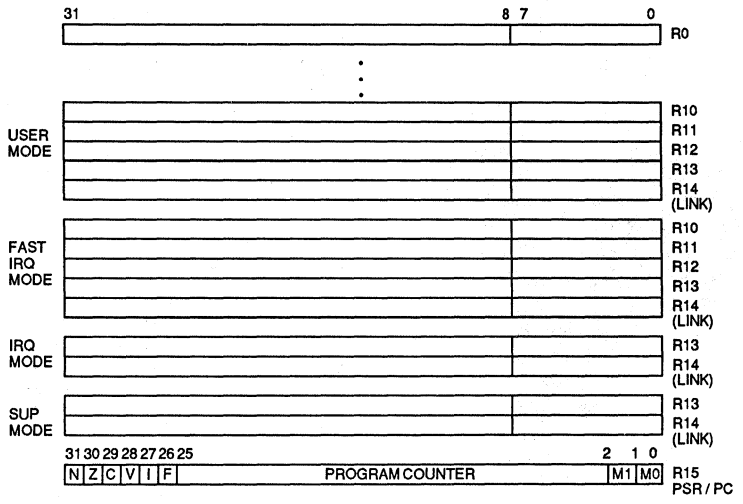
Inherent in the concept of RISC processors is the notion that more instructions are required to implement the same functions than could be done by fewer instructions with a complex instruction set computer (CISC) processor. In most cases, even when more instructions are needed by RISC processors, the function can still be performed more quickly on RISC processors than CISC processors. This is causing the industry to doubt the million instruction per second (MIPS) ratings of RISC processors for good reason. The term MIPS is often used exclusively as a means of benchmarking performance. A better measure of performance is to time actual execution of real-world problems, independent of the number of instructions required to implement the function. An important parameter to keep constant when benchmarking processors is the memory access times, since not all processors will meet performance claims when working with commodity memories.

Another traditional measure of performance in the microprocessor world is the clock frequency of the processor. "Faster is better" has been the rule of thumb, but the most important consideration is the average number of bus cycles per instruction. A processor with a low clock frequency and a low number of bus cycles per instruction can actually outperform a processor with a high clock frequency and a higher number of bus clock cycles per instruction. The best choice of processors is one that benchmarks high while using a relatively low clock frequency and a small number of clocks per instruction executed. The VL86C010 possesses these characteristics giving it the best future evolution path to exploit advances in process technology.

PROGRAMMING MODEL

The VL86C010 contains a large, partially overlapping set of 25 32-bit registers, although the programmer can access only 16 registers in any mode of operation. Fifteen of the registers are general-purpose, with the remaining ten dedicated to such functions as user mode, FIRQ mode, IRQ mode, supervisor mode and the program counter / processor status register. Figure 1 shows the register model of the VL86C010. Registers R0 to R13 are accessible from the user mode for any purpose. The fifteenth register, user mode return-link, is specific to the user mode. Its contents are mapped with those of other return-link registers as the mode is changed. The return-link register is used by the Branch-and-Link instruction in a procedure call sequence, but may be used as a general-purpose register at other times. The least significant two bits of the processor status word (PSW) define the current mode of operation.

FIGURE 1. VL86C010 REGISTER SET



Five registers are dedicated to the FIRQ mode and overlay user mode R10 to R14 when the fast interrupt request is serviced. The registers R10 FIRQ to R13 FIRQ are local to the fast interrupt service routine and are used instead of the user mode registers R10-R13. R14 FIRQ holds the address used to restart the interrupted program, instead of pushing it onto a stack at the expense of another memory cycle. Using a link register helps provide very fast servicing of I/O-related interrupts, without disturbing the contents of the general-purpose register set, although the FIRQ routine can access the R0 to R9 user-mode registers if desired. The FIRQ mode is typically used for very short interrupt service routines that might fetch and store characters in a disk or tape controller application.

The next two registers are dedicated to the IRQ mode and overlay user mode R13 and R14 when the IRQ is serviced. Once again, R14 IRQ is the return-link register that holds the restart address and R13 IRQ is general-purpose and dedicated to the IRQ mode. This mode is used when the interrupt service routine will be lengthy and the overhead of saving and reloading the register set will not be a significant portion of the overall execution time.

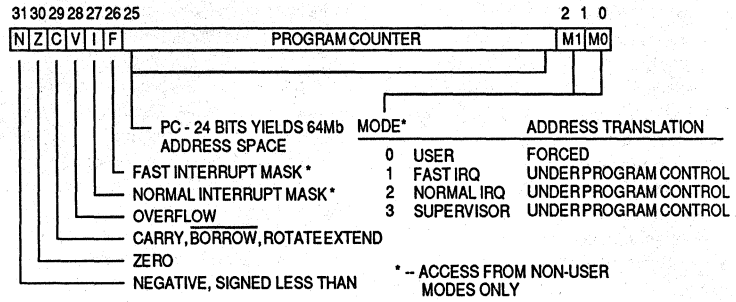
Two registers are dedicated to the supervisor mode and overlay user mode R13 and R14 when a supervisor mode switch is made using a SWI instruction. Operation of these two registers is the same as previously discussed.

The last register (R15) contains the processor status word and program counter and is shared by all modes of operation. The upper six bits are processor status, the next 24 bits are the program counter (word address), and the last two indicate the mode.

PROCESSOR STATUS REGISTER

Like most 32-bit processors the VL86C010 makes a distinction between user and supervisor modes: the user executes at the lowest privilege level, and the supervisor interrupts executes at higher levels of privilege. Figure 2 shows the processor status word containing the control line states associated with each mode.

FIGURE 2. PROCESSOR STATUS REGISTER



Translate is a control signal provided by the processor for control of an external memory management unit. The translate line is enabled in the user mode and disabled in the supervisor, fast interrupt, and normal interrupt modes, since all modes except for the user mode are expected to be running secure code. Translated fetches can be made from the supervisor mode by setting an optional bit in the load / store instructions.

The processor status register contains the program counter, mode control bits, and condition codes, as shown in Figure 2. The bits marked with an asterisk are alterable only from non-user modes. If the user tries to write to these bits, they remain unchanged and the processor continues operation in the user mode. In other words, this is not a trap condition. The flags in the processor status register are the standard Negative, Zero, Carry, and Overflow. The sixteen allowable combinations of the condition code bits are shown in Table 1. These combinations are used for all conditional instruction execution since a conditional branch is nothing more than a jump instruction with conditional execution.

EXCEPTIONS

The VL86C010 supports a partially overlapping register set so that, when interrupts are taken, the contents of the register array does not have to be saved before new operations can begin. Improved response time is accomplished, in the case of the fast interrupt, by dedicating four general-purpose registers, in addition to a return-link register, that are only accessible in the FIRQ mode. These dedicated registers can contain all the pointers and byte-counts for simple I/O service routines, thus incurring no overhead when context-switching between processing and servicing interrupts at high rates. The other modes (IRQ and SUP) each have one general-purpose and one return address (link) register dedicated to them. The general-purpose register is ideally suited for implementing a local stack for each mode. The need for dedicated registers in these modes is not as great, since the time spent in an interrupt or supervisor routine is on the average much greater than the time spent in transition between the routines. The working registers can be saved and restored from stacks without significant overhead.

The interrupt latency of the VL86C010 is very short because the instruction execution time is typically 250 ns, with a maximum of 2.25 µ (for a load multiple instruction, loading sixteen registers). Once the processor recognizes an interrupt is pending, the time to begin processing is 0.5 µ, making a total worst-case interrupt latency of 2.75 µ. In addition to interrupts, six other types of exceptions are supported by the processor. These are address exceptions, data-fetch cycle aborts, instruction-fetch cycle aborts, software interrupts, undefined instruction traps, and reset.

The VL86C010 supports a 26-bit linear address space, allowing a total of 64M-bytes of physical memory. Data

TABLE 1. INSTRUCTION CONDITION CODES

Condition	Encoded Value	Operation
AL	E	Always
CC	3	Carry Clear / Unsigned Lower Than
CS	2	Carry Set / Unsigned Higher Or Same
EQ	0	Equal (Z Set)
GE	A	Greater Than Or Equal ($N \cdot V$) +($\overline{N} \cdot \overline{V}$)
GT	C	Greater ((($N \cdot V$) + ($\overline{N} \cdot \overline{V}$)) $\cdot \overline{Z}$)
HI	8	Higher Unsigned ($C \cdot \overline{Z}$)
LE	D	Less Than Or Equal ((($N \cdot \overline{V}$) + ($\overline{N} \cdot V$)) + Z)
LS	9	Lower Or Same Unsigned ($\overline{C}$ + Z)
LT	B	Less Than (($N \cdot \overline{V}$) + ($\overline{N} \cdot V$))
MI	4	Negative (N)
NE	1	Not Equal ($\overline{Z}$)
NV	F	Never
PL	5	Positive ($\overline{N}$)
VC	7	Overflow Clear
VS	6	Overflow Set

references outside the range 0 to 3FF,FFFFH cause an address exception trap that can be used to detect a run-away program. The program counter will wrap around to 0000H without causing an address exception condition.

If the abort signal is asserted by the memory management unit during a data fetch, the processor will abort data transfer instructions (LDR, STR) as if they had never been executed. If the instruction was a block data transfer (LDM, STM), the processor will allow the instructions to complete. If the write-back control bit in these instructions is set, the base address will be updated even if it would have been overwritten during the instruction execution. An example of this would be execution of a block data transfer instruction with the base register in the list of registers to be overwritten.

Software interrupt instructions (SWI) are used to change from user mode to supervisor mode. When encountered, the processor will save the current program counter (R15) into R14 SUP, set the mode bits to the supervisor mode, and start execution at the software interrupt vector address.

An undefined instruction will cause a trap similar to the execution of a software interrupt, except that the undefined instruction vector will be used as the next address.

Reset is treated similar to the other traps and will start the processor from a known address. When the reset condition is recognized, the currently executing instruction will terminate abnormally, the processor will enter the supervisor mode, disable both the FIRQ and IRQ interrupts, and begin execution at address 0000H. While the reset condition remains, the processor will execute dummy instruction fetches.

The processor exception vector map is illustrated in Figure 3. The exceptions are prioritized to reset (highest), address exception, data abort, FIRQ, IRQ, prefetch abort, undefined instruction, and software interrupt (lowest).These vector addresses normally will contain a branch instruction to the associated service routine, except for the FIRQ entry. In order to further reduce latency, the FIRQ service routine may begin at address 001CH if the software designer so chooses.

Whenever the processor enters the supervisor mode, whether from a SWI, address exception, undefined instruction trap, prefetch, or data abort, the IRQ is disabled and the FIRQ unchanged.

FIGURE 3. EXCEPTION VECTOR MAP

Address(Hex)	Function	Priority Level
000 0000	Reset	0
000 0004	Undefined Instruction Trap	6
000 0008	Software Interrupt	7
000 000C	Abort (Prefetch)	5
000 0010	Abort (Data)	2
000 0014	Address Exception	1
000 0018	Normal Interrupt (IRQ)	4
000 001C	Fast Interrupt (FIRQ)	3

INSTRUCTION SET

The VL86C010 supports five basic types of instructions with several options available to the programmer. These instruction types are: data processing , data transfer, block data transfer, branch, and software interrupt. All instructions contain a 4-bit conditional execution field (shown in Table 1) that can cause an instruction to be skipped if the condition specified is not true. The execution time for a skipped instruction is one sequential cycle (125 ns for an 8 MHz processor).

Data processing instructions operate only on the internal register file and each has three operand references: a destination and two source fields. The destination (Rd) can be any of the registers, including the processor status register, although some bits in R15 can only be changed in particular modes. The source operands can have two forms: both can be registers (Rm and Rn) or a register (Rn) and an 8-bit immediate value. Both forms of operand specification provide for the optional shifting of one of the source values using the on-board barrel shifter. If both operands are registers, the Rm can be

TABLE 2. DATA PROCESSING INSTRUCTIONS

Instruction	Function	Op Code	Operation	Flags Affected
ADC	Add With Carry	5	Rd:=Rn+Shift(S2)+C	N, Z, C, V
ADD	Add	4	Rd:=Rn+Shift(S2)	N, Z, C, V
AND	And	0	Rd:= Rn • Shift(S2)	N, Z, C
BIC	Bit Clear	E	Rd:= Rn • $\overline{\text{Shift(S2)}}$	N, Z, C
CMN	Compare Negative	B	Shift(S2)+Rn	N, Z, C, V
CMP	Compare	A	Rn-Shift(S2)	N, Z, C, V
EOR	Exclusive OR	1	Rd:=Rn⊕ Shift(S2)	N, Z, C
MOV	Move	D	Rd:=Shift(S2)	N, Z, C
MVN	Move Negative	F	Rd:=$\overline{\text{Shift(S2)}}$	N, Z, C
ORR	Inclusive OR	C	Rd:=Rn+Shift(S2)	N, Z, C
RSB	Reverse Subtract	3	Rd:=Shift(S2)-Rn	N, Z, C, V
RSC	Reverse Subtract With Carry	7	Rd:=Shift(S2)-Rn-1+C	N, Z, C, V
SBC	Subtract With Carry	6	Rd:=Rn-Shift(S2)-1+C	N, Z, C, V
SUB	Subtract	2	Rd:=Rn-Shift(S2)	N, Z, C, V
TEQ	Test For Equality	9	Rn ⊕ Shift(S2)	N, Z, C
TST	Test Masked	8	Rn • Shift(S2)	N, Z, C

shifted. For the other case, it is the immediate value that can pass through the shifter. Another field in these instructions allows for the optional updating of the condition codes as a result of execution of the operation. Table 2 shows the possible data processing operations and the status flags affected.

Data transfer instructions are used to move data between memory and the register file (load), or vice-versa (store). The effective address is calculated using the contents of the source register (Rn) plus an offset of either a 12-bit immediate value or the contents of another register (Rm). When the offset is a register, it can optionally be shifted before the address calculation is made. Table 3 shows the addressing modes supported and their corresponding assembler syntax. The offset may be added to or subtracted from index register Rn. Incrementing or decrementing can be either pre- or post-indexing, depending on the desired addressing mode. In the post-indexed mode, the transfer is performed using the contents of the index register as the effective address, and the index register is modified by the offset and rewritten. In the pre-indexed mode, the effective address is the index register modified in the appropriate manner by the offset. The modified index register can be written back to Rn, if the write-back bit is set (or left unchanged, if desired). When a register is used as the offset, it can be pre-scaled by the barrel shifter in a similar manner, as with data processing instructions.

Data transfer instructions can manipulate bytes or words in memory. When a byte is read from the memory, it is placed in the low-order 8 bits of the register and zero-extended to a full word. For byte writes, the lower 8 bits of the register are written to the byte address referenced and the other bytes within the word unaffected.

The VL86C010 supports both logical and physical address spaces at a lower level in hardware than other processors. Data transfer instructions contain a translate enable bit that allows non-user mode programs to select the logical or physical address space as desired. The bit from the instruction is placed on the TRANS pin of the processor to signal an external memory management unit (MMU) whether to translate first or pass the address from the processor bus to the memory. This allows programs executing in the supervisor or interrupt modes to have easy access to user memory areas for page fault correction or to have bounds checking performed on dynamic data structures in the system space by the MMU. In the user mode, addresses are always translated by the MMU if it is implemented in the system.

The block data transfer instructions allow multiple registers to be moved in a single instruction. The instruction has a field containing a bit for each of the sixteen registers visible in the current mode. Bit 0 corresponds to R0, and bit 15 corresponds to R15, the program counter. A bit set in a particular position means that the corresponding register will be affected by the transfer. The register bits are always saved from lowest to highest and R0 will always appear at a lower address than R1. The ability to pre- or post- increment or decrement allows both stacks and queues to be implemented efficiently with any convention chosen by the programmer.

The branch instruction has two forms, branch and branch-with-link. The branch instruction causes execution to start at the current program counter plus a 24-bit offset contained in the instruction.

TABLE 3. MEMORY ADDRESSING MODES

AddressingMode	Operation	Syntax
PC Relative	EA* = PC ± Offset (12 Bits)	LABEL
Base Register Offset With Post-Increment	EA* = Rn Rn ± Offset → Rn	[Rn],Off
Base Register Offset With Pre-Increment**	EA* = Rn ± Offset (12 Bits) Rn ± Offset → Rn	[Rn,Off]
Base Register Index With Post-Increment	EA* = Rn Rn ± Rm → Rn	[Rn],Rm
Base Register Index With Pre-Increment**	EA* = Rn ± Rm Rn ± Rm → Rn	[Rn,Rm]

* - Effective Address
** - Program control of index register update, i.e. Rn may be left unchanged.

The offset is left-shifted by two bits (forming a 26 bit address) before it is added to the program counter. Since all instructions are word-aligned a branch can reach any location in the address space. The branch-with-link instruction copies the program counter and processor status register into R14 prior to branching to the new address. Returning from the branch-with-link simply involves reloading the program counter from R14 (MOV PC,R14). The PSR can optionally be restored from R14 (MOVS PC,R14). The software interrupt instruction format is used primarily for supervisor service calls. When this instruction is executed the PC and PSR are saved in R14 SUP. The PC is then set to the SWI vector location and the processor placed in the supervisor mode.

Instructions operate at speeds that are dependent upon the options selected. Table 4 shows the instruction types, execution rates and adjustments for operand shifting or affecting the program counter. The table is expressed in terms of N and S cycles, representing non-sequential and sequential cycles, respectively. The processor is able to take advantage of memories that have faster access times when accessed sequentially in the nibble or column mode. These faster cycles are designated as S cycles, while the N cycles typically take twice as long. If faster static memory is used, the N and S cycles would be equal.

The VL86C010 is offered in two packages, an 84-pin JEDEC Type-B ceramic leadless chip carrier and an 84-pin plastic leaded chip carrier (PLCC) for lower cost applications.The JEDEC Type-B package requires a suitable socket for mounting the carrier onto a printed circuit board. The PLCC package can be either surface-mounted directly onto the board or socketed with currently available standard sockets, depending on manufacturing requirements and/or capabilities.

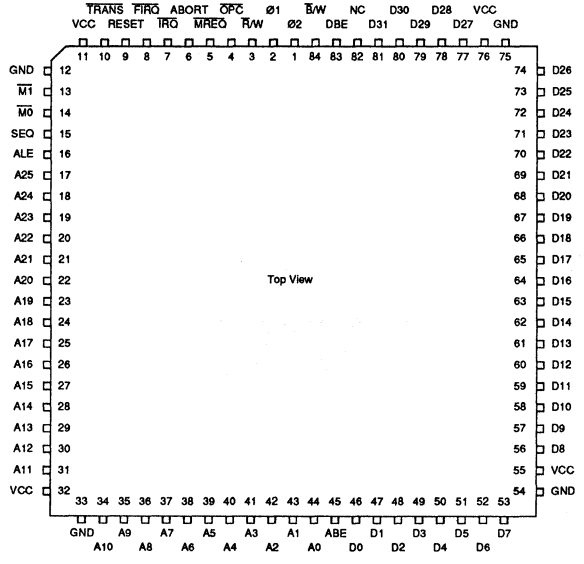
TABLE 4. INSTRUCTION EXECUTION TIMES

Operation	Base Execution Time	Adjustment for Source Shift	Adjustment for PC Modification
RS • #→ RD	1S	1S for Shift(RS)	1S + 1N if PC Modified
RS • RS→ RD	1S	1S for Shift(RS)	1S + 1N if PC Modified
LDR	2S + 1N	1S for Shift(RS)	1S + 1N if PC Modified
STR	2N	1S for Shift(RS)	
LDM	(n* + 1)S + 1N		1S + 1N if PC Modified
STM	(n* - 1)S + 2N		
BR	2S + 1N		
BR & LINK	2S + 1N		
SWI	2S + 1N		

* n - the number of registers trarsferred in a Load /Store Mutiple nstruction.
If the condition field in an instuction is not true, the instruction is skipped and the execution time is 1S cycle.

PIN DIAGRAM

Plastic Leaded Chip Carrier



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	-10 to +80°C
Storage Temperature	-65 to + 150°C
Supply Voltage to Ground Potential	-0.5 to VCC + 0.3 V
Applied Output Voltage	-0.5 to VCC + 0.3 V
Applied Input Voltage	-0.5 to + 7.0 V
Power Dissipation	2.0 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ± 5%

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
VOH	Output High Voltage		VCC-0.5		VCC	V	IOH = -3.0 mA
VOL	Output Low Voltage				0.4	V	IOL = 3.6 mA
VIH	Input High voltage	Ø1, Ø2	VCC-0.3		VCC+0.3	V	
		All Others	2.4		VCC+0.3	V	
VIL	Input Low Voltage	Ø1, Ø2	-0.3		0.3	V	
		All Others	-0.3		0.8	V	
ILI	Input Leakage Current				10	µA	VIN = 0V to VCC
ILO	Output Leakage Current				10	µA	VOUT = 0V to VCC
ICC	Operating Supply Current			20		mA	See Note 3
IOS	Output Short Circuit Current				TBD	mA	

CAPACITANCE TA = 25°C, f = 1.0 MHz

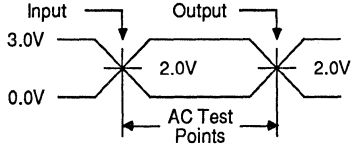
Symbol	Parameter	Min	Max	Unit	Conditions
CI	Input Capacitance		TBD	pF	VIN = 0 V - See Note 4
CO	Output Capacitance		TBD	pF	VOUT = 0 V - See Note 4

Notes:
1 Measured with outputs unloaded.
2 Periodically sampled as opposed to 100% tested.

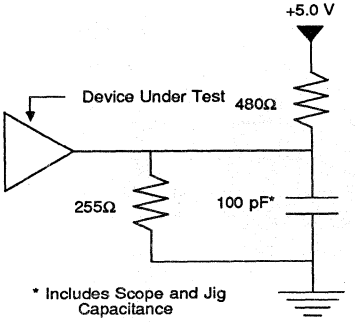
AC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ±5%

Symbol	Parameter	VL86C010 - 4			VL86C010 - 8			Units	Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
TV	Clock Non-Overlap	0			0			ns	Measured at 2 V Point
TCLK	Clock Period	250		10000	125		10000	ns	
TCKL	Clock Low Time	TBD	125	10000	TBD	62.5	10000	ns	
TCKH	Clock High Time	TBD	125	10000	TBD	62.5	10000	ns	
TAOUT	Address Delay Time			0			0	ns	
TAH	Address Hold Time		10	TBD		10	TBD	ns	
TRWS	$\overline{R}$/W Setup Time	0		TBD		0	TBD	ns	
TRWH	$\overline{R}$/W Hold Time		10	TBD		10	TBD	ns	
TDOUT	Data Out Delay Time			100			50	ns	
TDOH	Data Out Hold Time		10	TBD		10	TBD	ns	
TDIS	Data In SetupTime	10			10			ns	
TDIH	Data In Hold Time	20			20			ns	
TDBE	Data Bus Enable Time		60			30		ns	
TDBZ	Data Bus Disable Time		70			35		ns	
TABTS	Abort Setup Time	70			35			ns	
TABTH	Abort Hold Time	0		TBD	0		TBD	ns	
TSEQD	Sequential Delay Time			110			55	ns	
TSEQH	Sequential Hold Time			10			10	ns	

AC TEST CONDITIONS

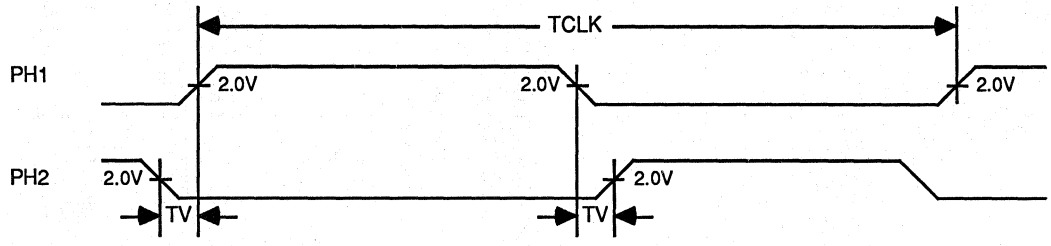


AC TEST LOAD CIRCUIT

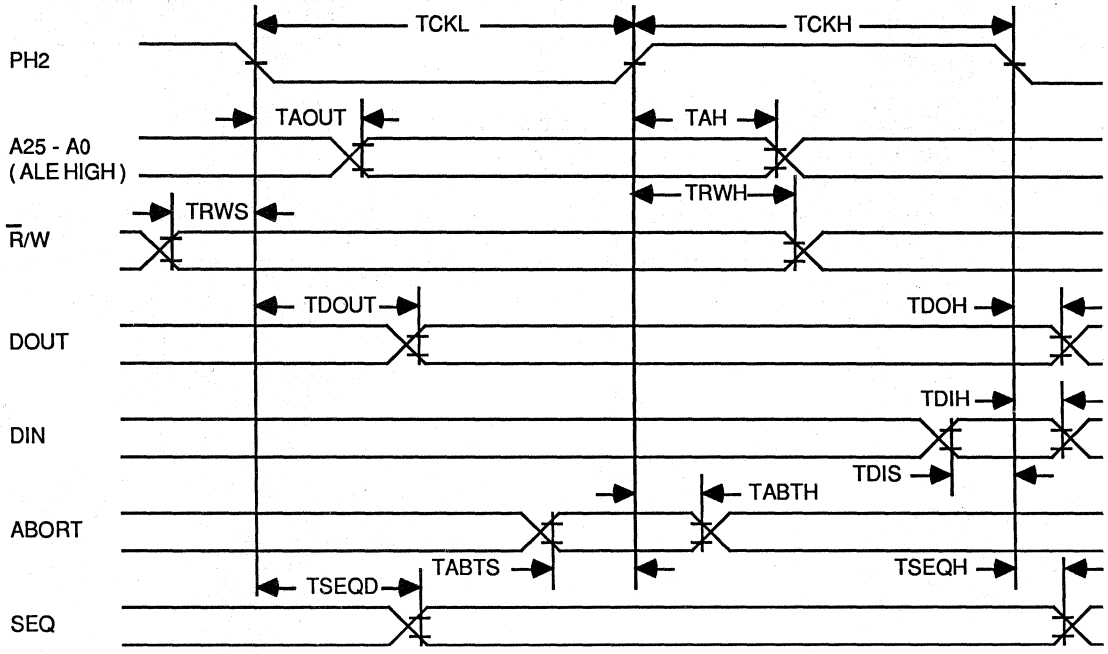


TIMING DIAGRAMS

PROCESSOR CLOCKS

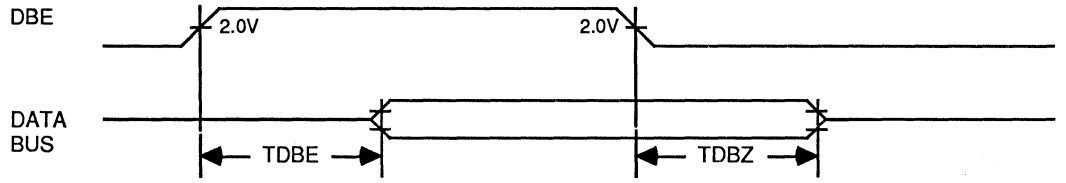


MINIMUM BUS CYCLE



TIMING DIAGRAMS

DATA BUS ENABLE



EXAMPLES OF THE INSTRUCTION SET

The following examples illustrate methods that basic ARM instructions can be combined to yield efficient code. None of the methods saves a large amount of execution time, although they all save some; most result in more compact code.

EXAMPLE 1 - USING THE CONDITIONAL EXECUTION FOR THE LOGICAL OR FUNCTION.

```
        CMP     Rn, #p          ; IF Rn = p OR Rm = q THEN
        BEQ     Label           ;   GOTO Label
        CMP     Rm, #q
        BEQ     Label
```

By using conditional execution, the routine compresses to:

```
        CMP     Rn, #p
        CMPNE   Rm, #q          ; if Rn not equal p, try other test
        BEQ     Label
```

EXAMPLE 2 - ABSOLUTE VALUE

```
        TEQ     Rn, #0          ; check sign
        RSBMI   Rn, Rn, #0      ; and 2's complement if required
```

EXAMPLE 3 - UNSIGNED 32-BIT MULTIPLY

```
; enter with numbers in Ra, Rb - product contained in Rm
        MOV     Rm, #0          ; init result register
LOOP    MOVS    Ra, Ra, LSR #1
        ADDCS   Rm, Rm, Rb
        ADD     Rb, Rb, Rb
        BNE     LOOP            ; stops when Ra becomes zero
                                ; Rm = Ra * Rb
                                ; ( Ra = 0, Rb is altered )
```

EXAMPLE 4 - MULTIPLICATION BY 4, 5, OR 6 AT RUN TIME

```
        MOV     Rc, Ra, LSL #2  ; multiply by 4
        CMP     Rb, #5          ; test multiplier value
        ADDCS   Rc, Rc, Ra      ; complete multiply by 5
        ADDHI   Rc, Rc, Ra      ; complete multiply by 6
```

EXAMPLE 5 - MULTIPLICATION BY CONSTANT 2^N USING THE BARREL SHIFTER (1, 2, 4, 8, 16, 32, ...)

```
        MOV     Ra, Ra, LSL #n
```

EXAMPLE 6 - MULTIPLICATION BY CONSTANT (2^N)+1 USING THE BARREL SHIFTER (3,5,9,17, ...)

```
        ADD     Ra, Ra, LSL #n
```

EXAMPLE 7 - MULTIPLICATION BY CONSTANT (2^N) - 1 (3, 7, 15, ...)

```
        RSB     Ra, Ra, Ra, LSL #n
```

EXAMPLE 8 - MULTIPLICATION BY 6

```
        ADD     Ra, Ra, Ra, LSL #1      ; multiply by 3
        MOV     Ra, Ra, LSL #1          ; and then by 2
```

EXAMPLE 9 - MULTIPLY BY 10 AND ADD EXTRA NUMBER (DECIMAL TO BINARY CONVERSION)

```
        ADD     Ra, Ra, Ra, LSL #2      ; multiply by 5
        ADD     Ra, Rc, Ra, LSL #1      ; multiply by 2 and add in next digit
```

EXAMPLE 10 - DIVISION AND REMAINDER

```
; enter with numbers in Ra and Rb
        MOV     Rcnt, #1                ; bit to control the division
DIV1    CMP     Rb, Ra                  ; move Rb until greater than Ra
        MOVCC   Rb, Rb, ASL #1
        MOVCC   Rcnt, Rcnt, ASL #1
        BCC     DIV1
        MOV     Rc, #0
DIV2    CMP     Ra, Rb                  ; test for possible subtraction
        SUBCS   Ra, Ra, Rb              ; subtract if valid
        ADDCS   Rc, Rc, Rcnt            ; put relevant bits in result
        MOVS    Rcnt, Rcnt, LSR #1      ; shift control bit
        MOVNE   Rb, Rb, LSR #1          ; halve unless finished
        BNE     DIV2
                                        ; result in Rc
                                        ; remainder in Ra
```

MESSAGE - PASSING COPROCESSOR (MULTIBUS® II)

FEATURES

- Full-function, single-chip interface to Parallel System Bus (iPSB)
- Implements full message-passing protocol on iPSB bus
- Offloads managing iPSB bus arbitration, transfer and exception cycles from local CPU
- Compatible with Bus Arbiter/ Controller (BAC) and Message Interrupt Controller (MIC) interface designs
- Maximizes performance on iPSB bus and local on-board bus
- Simplifies highly functional interconnect space implementations for both local and iPSB buses
- Processor-independent interface to iPSB bus
- Supports co-existence of dual-port and message-passing architectures

® MULTIBUS is a registered trademark of Intel Corp.

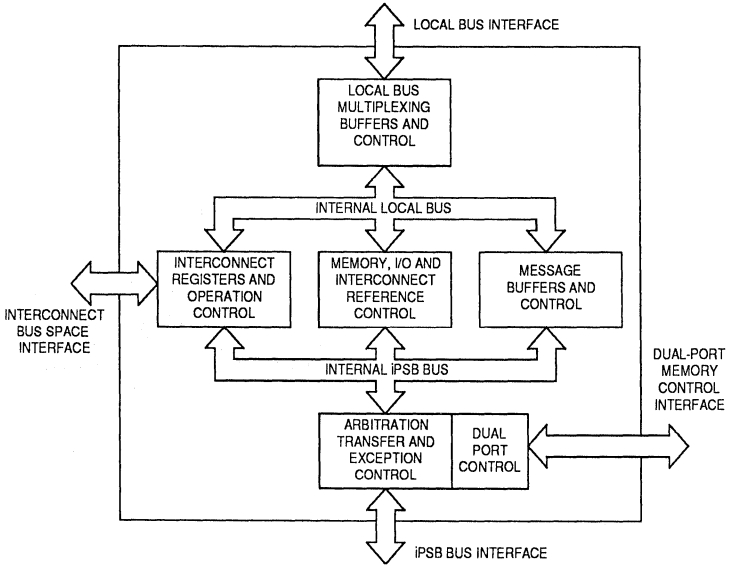
FUNCTIONAL DESCRIPTION

The VL82C389 Message Passing Coprocessor (MPC) provides a high-integration interface solution for the Parallel System Bus (iPSB) of the MULTIBUS II architecture. The device integrates the logic necessary to implement a full bus interface solution, including support for message passing and interconnect spaces, as well as memory and I/O references on the iPSB bus. In addition, the MPC is designed to simplify implementation of dual-port memory functions for those designs that must co-exist with message passing.

The message address space in the MULTIBUS II architecture has been defined to provide a high-performance interprocessor communication mechanism for multiprocessor systems. By performing the message space interface, the VL82C389 MPC offloads the interprocessor communication tasks from the local on-board CPU, which decouples the local bus activities from the iPSB bus activities. Decoupling these two functions eliminates an interface bottleneck present in traditional dual-port architectures. The bottleneck is a result of having a dual-port architecture that requires a tight coupling between a processor and some shared memory resource of limited size. Unfortunately, as the number of processors increases, the dual-port structure degradates system performance even more dramatically.

Using the MPC component to decouple these resources yields several enhancements to system performance. For example, resources on the local processor bus and parallel system bus are not held in wait states while arbitration for other resources is performed. In addition, each transfer can occur at the full bandwidth of the associated bus. The benefit of this is the increased overall system performance that results from processors being able to process other tasks in parallel, with message transfers being handled by the MPC component.

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C389-GC	Ceramic Pin Grid Array (PGA)

Note: Operating temperature range: 0°C to 70°C.

FUNCTIONAL DESCRIPTION

Arbitration, Transfer, and Exception Cycle Protocol Support

The Message-Passing Coprocessor component implements the full arbitration, transfer, and exception cycle protocols required to interface to the iPSB bus. Arbitration is supported for both normal fairness mode and high priority mode.

The MPC component performs the handshake protocols necessary to successfully complete iPSB transfer operations. Transfer operations include access to memory, I/O, message and interconnect address spaces on the iPSB bus. During the transfer cycle, the device generates and checks parity on the System Control (SC) lines and on the Address/Data (AD) lines. In addition, the MPC component recognizes agent errors and bus exceptions that are reported to the local CPU for recovery action.

INTERFACE DESCRIPTION

This section describes each interface noted in the block diagram on the front page. These interfaces include the local bus, the iPSB bus, the interconnect bus, and dual-port memory.

The Local Bus Interface

The local bus interface is used to provide a processor-independent path from the on-board CPU to the iPSB bus. This interface supports direct references (memory, I/O, and interconnect address spaces) to the iPSB bus, references to local on-board interconnect space, and the full protocol for unsolicited and solicited message operations to/from the on-board CPU. Within the MPC component, local bus interface support consists of three logical interfaces: register, reference, and DMA. The register interface is used for message operations and access to interconnect address register on-board. These operations are completed fully asynchronous to the bus clock or interconnect bus operations. The reference interface is used to access resources asynchronous to the CPU (local interconnect space and memory, I/O, and interconnect address spaces on the iPSB bus). The DMA interface is used to transfer data for solicited message operations. This interface is designed to allow either two-cycle or single-cycle transfers. Single-cycle transfers allow direct transfer of data between the MPC component and memory. To achieve higher performance via single-cycle transfers, the DMA interface is optimized for aligned data structures; however, operation on arbitrary byte strings is also supported.

iPSB Bus Interface

The iPSB bus interface implements a full 32-bit interface to the iPSB bus. This implementation includes arbitration, requestor control, replier control, and error handling functions. As a requestor, the MPC component supports references to memory, I/O, and interconnect spaces, as well as message packet transmission. As a replier, the MPC component supports interconnect space and message packet reception. In addition, this interface provides significant management services for external dual port memory. These services include: address recognition, iPSB bus replier handshake, agent error checking, and bus parity generation and checking. Although this device handles the majority of errors, the dual-port memory controller is still responsible for generation and check of memory data parity (not bus parity).

Interconnect Bus Support

Simply stated, the interconnect address space provides a physical addressing mechanism (rather than logical) for software initialization and configuration of system parameters (reduces jumper configuration) and system level diagnostics. The interconnect bus provides a simple 8-bit path between the MPC component and a user-defined design for the implementation of interconnect space. All references to interconnect space (either from the local bus or the iPSB bus) are routed through this path for service. In addition, this interconnect bus can be used for non-reference related activities as diagnostics. An example of a highly functional interconnect space implementation is evidenced by the microcontroller implementation of Intel's iSBC 386/100. Further details of this implementation are available in the iSBC 386/100 Hardware Reference Manual (Intel order number: 146705-001).

Dual Port Memory Support

Although the MULTIBUS II architecture has defined the message address space for optimized performance of interprocessor communicaiton, more traditional designs can use dual-port memory implementations. The iPSB bus interface has been defined to allow co-existence of dual-port memory and message-passing architectures; however, it should be noted that the iPSB bus interface is optimized for message-passing architectures. The MPC component is designed to support this co-existence. The device can be configured to recognize a range of addresses in memory space and act as an iPSB bus replier when appropriate. If an address match is detected, the MPC component signals the external dual-port memory controller of the request. While the MPC component provides an error detection and recovery mechanism for most agent errors and bus exceptions in a dual-port design, it is still the responsibility of the dual-port memory controller to generate and check memory data parity.

Single Board Computer Configuration

The Message Passing Coprocessor component provides a processor-independent iPSB bus interface solution for intelligent SBC boards. Examples include CPU boards, intelligent peripheral controllers, file servers, intelligent data communications controllers, and graphics/image processors. This component is optimized for bus master or intelligent slave designs. Using the MPC component reduces overall board real estate required for the iPSB bus interface. The MPC component improves system reliability by performing the error checking and reporting protocols defined in the iPSB bus interface specification.

Message Support

The MPC provides full support for unsolicited and solicited messages. For solicited messages, the MPC supports a one message deep transmit FIFO and a four message deep receive FIFO. For solicited messages, the MPC supports one output channel and one input channel. Each channel has two packet buffers to allow pipelined operations on the local and iPSB buses. These features provide the required level of support necessary to implement the high-bandwidth message-passing facility defined in the Multibus II architecture.

Unsolicited Message Support

Unsolicited message support in the MPC is provided on the local bus via a register interface and on the iPSB bus

with a packet transfer mechanism. An unsolicited message is initiated by the sending host CPU transferring a message to its local MPC. The transfer is performed as a series of register operations to the transmit FIFO. An unsolicited message may be from 4 to 32 bytes in length in four-byte increments. Once the unsolicited message is transferred to the MPC, the sending host is free to discard the message in memory and process another task if it so chooses. In parallel the MPC requests access to the iPSB bus for the pending transfer. Once the iPSB bus is obtained, the sending MPC transfers the message, as a single packet, to the receiving agent.

The receiving agent recognizes the incoming packet by its destination address field. If the MPC on the receiving agent detects a match between its message host ID and the destination address field, the packet is stored in a buffer and checks for error conditions. Any errors found are signaled to the sending MPC via the iPSB bus protocol.

Assuming the packet received is error-free, the receiving host CPU is informed of the message via an interrupt signal generated by the MPC. The host responds to this interrupt by performing a series of register operations to retrieve the message from the receive FIFO.

If an error occurs during the transfer of an unsolicited message over the iPSB bus, the sending MPC takes recovery action. If the error is a NACK, the MPC retries the message a predetermined number of times. All other errors are reported back to the sending host CPU for recovery actions. The host CPU is signaled via an interrupt and can retrieve the unsolicited message, with error status, through the error FIFO. Again this operation is performed with a series of register operations.

Solicited Message Support

Solicited message transfers can be divided into three basic phases: negotiation, data transfer, and completion. The negotiation phase of the solicited transfer requires the exchange of two special unsolicited messages between the sending and receiving agents. The buffer request message is transferred from the sending agent to the receiving agent and the buffer grant is returned from the receiving agent to the sending agent. The MPC supports the transfer of these messages with the standard transfer protocol on the iPSB bus as previously described for the typical unsolicited message.

A solicited message transfer is initiated by the sending host CPU writing a buffer request message to the sending MPC transmit FIFO. The sending MPC recognizes the message as a buffer request and saves the following information. The destination and source addresses are saved for use in the data transfer phase. The request ID is saved for identification during completion or cancel operations. The transfer length is saved to determine the end of transfer and may contain any number of bytes. The MPC will pad the transfer to an even four-byte increment on the iPSB bus.

The sending MPC then assigns a sender liaison ID and transfers the buffer request message packet on the iPSB bus. The sender liaison ID is used to bind the buffer grant (or reject) to its corresponding buffer request when it is received back at the sending MPC. This allows the protocol to be extended to multiple concurrent transfers in the future.

The transfer phase is handled by the sending and receiving MPCs and their DMA controllers. Neither host CPU is involved in the transfer, and each may be processing other tasks during the transfer. At the sending agent, the transfer phase is slightly overlapped with the negotiation phase. As soon as the buffer request packet is sent error-free on the iPSB bus, the sending MPC pre-fetches up to two packets of data and prepares for transmission. Upon receiving the buffer grant and storing the necessary parameters, the data packet transfer is initiated. Data packets are then sent on the iPSB bus using full bandwidth block transfers, at intervals defined by the duty cycle parameters, until the transfer is complete. The end of transfer is signaled to the receiving MPC by the last data packet. A solicited transfer may consist of from one to 32 packets. Packets are bound to 32 bytes plus header, with total transfers limited to 16 Mbytes.

At the receiving agent, the transfer phase begins after a buffer grant packet has been sent error-free on the iPSB bus. The receiving MPC then detects data packets, verifies the liaison ID, and stores the data. If the solicited input channel is not active (e.g., due to local cancel) or the liaison ID does not match, an agent error is signaled on the iPSB bus. Errors during the transfer phase are rare. Flow control using the duty cycle parameter prevents NACK problems, and the receiver has responded with a buffer grant guaranteeing its existence and ability to perform the transfer. In the rare case that an error does occur, the MPC provides a retry algorithm for NACKs and reports exceptions or other agent errors immediately. The error is signaled to the host CPU by entering the completion phase. Errors generate an interrupt and provide error status.

The completion phase consists of a signal from the MPC to its corresponding host CPU. The signal consists of an interrupt followed by a series of register operations on the local bus. In all cases, the completion operation clears all states associated with the solicited operation in the MPC, allowing another operation to be initiated.

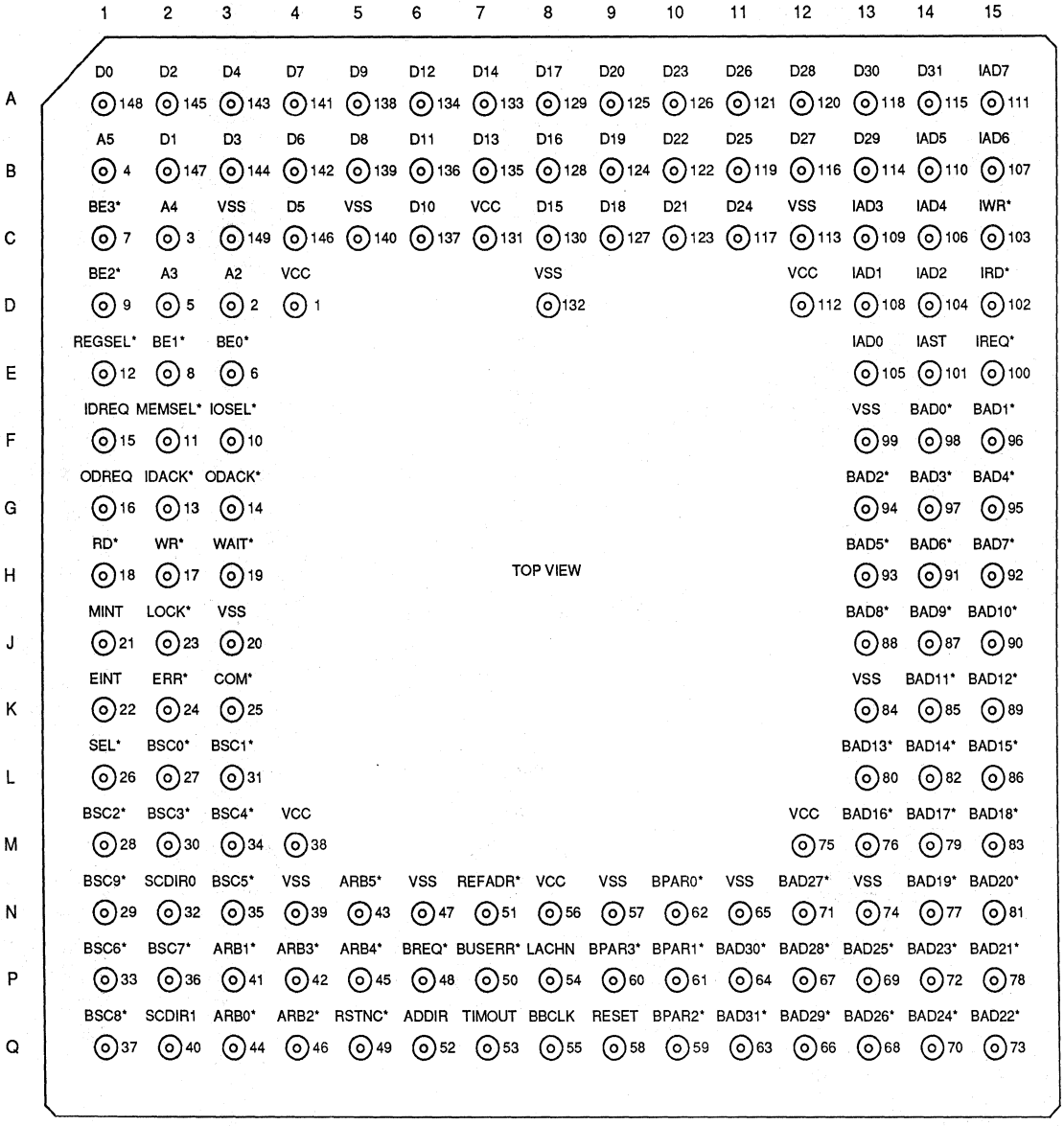
The MPC guarantees fail-safe operation for all aspects of the solicited message transfer, assuming the bus clock remains active (if the bus clock fails, all transfers cease, eliminating the need for recovery). This capability is provided by the error detection and reporting already discussed for bus-related problems and by two fail-safe counters that protect against fatal hardware or software errors on the sending or receiving agents. Recovery is provided to free a solicited message resouce that would otherwise be tied up indefinitely, which eliminates the need for a fail-safe software timer.

It is important to note that the fail-safe counters are not intended for normal flow control. If a receiving host CPU accumulates a significant queue of buffer requests from its MPC, it should use unsolicited messages (and possibly rejects) to free channels in the system for other uses. The fail-safe counters are only intended to replace the need for a software timer to recover from otherwise fatal hardware and software errors.

For a more comprehensive explanation of the MPC function, please refer to the Intel document, Multibus II Message Passing Coprocessor External Product Specification (Engineering Document Number: 149300-001).

PIN DIAGRAM

Ceramic Pin Grid Array (PGA)



SIGNAL DESCRIPTIONS

The MPC signals can be classified into five interface groups: the iPSB bus, the dual-port RAM, the local bus, the interconnect bus and power/ground. This table describes the individual signals for each of these interfaces.

Signal Name	Pin Number	Signal Description
BREQ*	48	The bus request is a bidirectional, open-drain signal with high current drive. It connects directly to the iPSB bus. As an input, it indicates that there are agents awaiting access to the bus. In fair access mode, this inhibits the MPC from activating its own request. As an output this signal is used to request bus access. Further details can be found in the iPSB bus specification.
ARB0*, ARB1*, ARB2*, ARB3*, ARB4*, ARB5*	44, 41, 46, 42, 45, 43	The arbitration signals are bidirectional, open drain signals with high current drive. They connect directly to the iPSB bus.These signals are used during normal operation to identify the mode and arbitration ID of an agent during arbitration cycles. During system initialization (while reset is active) these signals are used to initialize slot and arbitration IDs. Further details are available in the iPSB bus specification.
BAD0*- BAD31*	See Table	The address/data signals are bidirectional lines that connect to the iPSB bus AD* signals through 74F245 or equivalent transceivers. Further details are available in the iPSB bus specification.

BAD31*	BAD30*	BAD29*	BAD28*	BAD27*	BAD26*	BAD25*	BAD24*
63	64	66	67	71	68	69	70
BAD23*	BAD22*	BAD21*	BAD20*	BAD19*	BAD18*	BAD17*	BAD16*
72	73	78	81	77	83	79	76
BAD15*	BAD14*	BAD13*	BAD12*	BAD11*	BAD10*	BAD9*	BAD8*
86	82	80	89	85	90	87	88
BAD7*	BAD6*	BAD5*	BAD4*	BAD3*	BAD2*	BAD1*	BAD0*
92	91	93	95	97	94	96	98

BPAR0*, BPAR1*, BPAR2*, BPAR3*	62, 61, 59, 60	The byte parity signals are bidirectional lines that connect to the iPSB bus PAR* signals through a 74F245 or equivalent transceiver. These signals are used to receive byte parity for incoming operations and to drive byte parity for outgoing operations. The MPC is responsible for parity generation and checking even if the address/data signals are driven from another source (e.g., dual-port memory data, address for reference, etc.). Further details are available in the iPSB bus specification.
ADDIR	52	The AD direction signal is an output used to control the direction of the 74F245 or equivalent transceivers for the BAD0* thru BAD31* and BPAR0* thru BPAR3* signals. Activating this signal drives data to the iPSB bus.
REFADR*	51	The reference address signal is an output from the MPC used to enable external address buffers for memory and I/O reference operations. Activating this signal drives the reference address onto the BAD* bus.
SCDIR0, SCDIR1	32, 40	The control/handshake direction signals are outputs used to control the direction of the 74F245 or equivalent transceivers for the BSC* signals. The SCDIR0 signal is used for BSC0* - BSC3* and BSC9*. The SCDIR1 signal is used for BSC4* - BSC8*. Activating these signals drives data to the iPSB bus.
BSC0*- BSC9* iPSB	See Table	The control/handshake signals are bidirectional lines that connect to iPSB bus SC* signals through 74F245 or equivalent transcievers. Details on the operation of these signals are available in the bus specification.

						BSC9*	BSC8*
						29	37
BSC7*	BSC6*	BSC5*	BSC4*	BSC3*	BSC2*	BSC1*	BSC0*
36	33	35	34	30	28	31	27

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
BBCLK	55	The bus clock input signal is a buffered version of the iPSB bus BCLK* signal. It is assumed that a 74AS1804A or equivalent buffer is used. This clock is used for all synchronous internal MPC timing.
TIMOUT	53	The time out input signal is used to detect a time out condition signalled by the CSM. This signal is connected to the iPSB bus through a 74AS1804A or equivalent buffer.
LACHN	54	The latch signal is an input used during initialization of slot and arbitration IDs. When the RESET signal is active, this signal indicates when slot and arbitration IDs are available. This signal is connected to the iPSB bus through a 74AS1804A or equivalent buffer. Further details on initialization are available in the iPSB bus specification.
RESET	58	The reset signal is an input used to put the MPC in a known state. Only the parts of the MPC involved with initialization of slot and arbitration IDs remain unaffected. This signal is buffered from the iPSB bus by a 74AS1804A or equivalent buffer connected to the RST* signal.
BUSERR*	50	The bus error signal is a bidirectional, open-drain line with high current drive. It connects directly to the iPSB bus. As an input, it is used to detect bus errors signalled by other agents. As an output it is used to signal parity errors detected on either the AD* or SC* signal lines, handshake protocol violations, or for extending exception recovery of a replier.
RSTNC*	49	The reset not complete signal is a bidirectional, open-drain line with high current drive. It connects directly to the iPSB bus. As an input, this signal inhibits the MPC from initiating iPSB bus operations. As an output it is used to prevent iPSB bus operation until an agent is finished with on-board initialization. This signal is activated by the RESET signal going active. It is deactivated by the interconnected microcontroller after the RESET signal is deactivated and initialization is complete.
SEL*	26	The SEL* signal is activated by the MPC to indicate a dual-port access. This signal is used to initiate the dual-port operation and may be used to enable the dual-port data buffers onto the BAD* bus. When the MPC completes the iPSB bus handshake on the iPSB bus, or an exception is detected, this signal deactivates.
COM*	31	The COM* signal is activated by the dual-port memory controller to indicate it is ready to complete the operation. This signal is assumed to be synchronous to the bus clock. The MPC activates replier ready on the iPSB bus on the next bus clock. This signal may not be deactivated until the EOT handshake is complete on the iPSB bus.
ERR*	24	The ERR* signal is activated by the dual-port memory controller to signal a memory data parity error. It must be stable at all times when the COM* signal is active. The MPC responds to this signal by completing the replier handshake on the iPSB bus using a "data error" agent error code. This signal may be asynchronous to the bus clock since it is qualified by the COM* signal.
D0 - D31	See Table	The data bus is a bidirectional group of signals used to transfer data between the host CPU and the MPC. Control is provided to allow operation of this bus with 8-, 16-, or 32-bit processors.

D31	D30	D29	D28	D27	D26	D25	D24
115	118	114	120	116	121	119	117
D23	D22	D21	D20	D19	D18	D17	D16
126	122	123	125	124	127	129	128
D15	D14	D13	D12	D11	D10	D9	D8
130	133	135	134	136	137	138	139
D7	D6	D5	D4	D3	D2	D1	D0
141	142	146	143	144	145	147	148

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
A2, A3, A4, A5	2, 5, 3, 4	The address inputs are used to identify MPC registers for message and interconnect space operations. Note that A0 and A1 are omitted to provide a consistent register address for all data bus width options. These signals are qualified by commands (e.g. RD* or WR*) in the MPC and therefore may glitch outside the specified set-up and hold window.
BE0*, BE1*, BE2*, BE3*	6, 8, 9, 7	The byte enable input signals are used to identify the valid bytes and for data path control during memory and I/O reference operations. Only combinations supported by the iPSB bus specification are valid. These are summarized in the table below. Values not shown are illegal and may result in unpredictable results. These signals are qualified by commands (e.g. RD* or WR*) in the MPC and therefore may glitch outside the specified set-up and hold window. Operation with 32-bit local buses requires all byte enable and data signals to be used. For 16-bit local buses, the BE3* and BE2* signals are held inactive and only D15-D0 are used. For all cases a read operation enables all 32 data signals, even if all byte enables are inactive. For 8-bit local bus operations BE3* is held active, BE2* is held inactive, BE1* is connected to A0*, and BE0* is connected to A0. This mode uses only D7-D0.

				LOCAL BUS				iPSB BUS			
BE3*	BE2*	BE1*	BE0*	D31 - D24	D23 - D16	D15 - D8	D7 - D0	AD31-AD24	AD23-AD16	AD15-AD8	AD7-AD0
L	L	L	L	V3	V2	V1	V0	V3	V2	V1	V0
L	L	L	H	V3	V2	V1	X	V3	V2	V1	X
H	L	L	L	X	V2	V1	V0	X	V2	V1	V0
L	L	H	H	V3	V2	X	X	X	X	V3	V2
H	L	L	H	X	V2	V1	X	X	V2	V1	X
H	H	L	L	X	X	V1	V0	X	X	V1	V0
L	H	H	H	V3	X	X	X	X	X	V3	X
H	L	H	H	X	V2	X	X	X	X	X	V2
H	H	L	H	X	X	V1	X	X	X	V1	X
H	H	H	L	X	X	X	V0	X	X	X	V0
L	H	L	H	X	X	X	V0	X	X	V0	X
L	H	L	H	X	X	X	V0	X	X	X	V0

L - Electrical LOW State (Active)
H - Electrical HIGH State (Inactive)
Vx - Valid Data Bytes
X - Active Bytes With Undefined Data

For References Only

MEMSEL*	11	The memory select input signal is used to idenfity a memory reference operation to the iPSB bus. It is qualified by commands (e.g., RD* or WR*) in the MPC and therefore may glitch outside the specified set-up and hold window.
IOSEL*	10	The I/O select input signal is used to identify an I/O reference operation to iPSB bus. It is qualified by commands (e.g., RD* or WR*) in the MPC and therefore may glitch outside the specified set-up and hold window.
REGSEL*	12	The register select input signal is used to identify operations to internal MPC registers used to perform message and interconnect space operations. This signal is qualified by commands (e.g., RD* or WR*) in the MPC and therefore may glitch outside the specified set-up and hold window.
LOCK*	23	The lock signal is an input to the MPC that allows back-to-back operations to be performed on the iPSB bus or to local interconnect space. When lock is asserted, any resource accessed by the operation (iPSB bus or local interconnect space) is locked until the LOCK* signal is deactivated.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
RD*	18	The read input signal is activated to initiate a read operation. This signal must provide clean transitions.
WR*	17	The write input signal is activated to initiate a write operation. This signal must provide clean transitions.
WAIT*	19	The wait signal is driven by the MPC to hold up a transfer operation. This signal will be used by the MPC for all accesses that require synchronization to another resource. When used, it is activated by a command going active and deactivated when the accessed resource is ready to complete the requested operation.
MINT	21	The message interrupt output signal is used for all message-related signalling to the host CPU. This includes arrival of an unsolicited message, completion of a solicited transfer, error on message transfer, etc.
EINT	22	The error interrupt output signal is used to signal all errors related to memory, I/O or interconnect space operations. Internal registers in the MPC provide exact details of the error via interconnect space. (Even though this is a local bus signal it will be discussed with the interconnect bus signals for simplicity in future sections.)
ODREQ	16	The output channel DMA request signal is generated by the MPC to enable DMA transfer of data to the MPC (e.g., output to the iPSB bus).
IDREQ	15	The input channel DMA request signal is generated by the MPC to enable DMA transfer of data from the MPC (e.g., input from the iPSB bus).
ODACK*	14	The output channel DMA acknowledge input signal is activated to perform a DMA data transfer to the MPC. It is qualified by commands (e.g., RD* or WR*) in the MPC and therefore may glitch outside specified set up and hold window.
the IDACK*	13	The input channel DMA acknowledge input signal is activated to perform a DMA data transfer from the MPC. It is qualified by commands (e.g., RD* or WR*) in the MPC and therefore may glitch outside the specified set-up and hold window.
IAD0-IAD7	See Table	The interconnect address/data bus is a multiplexed bus designed to directly interface to a microcontroller. In addition to the MPC, other interconnect registers can be connected to this bus.

IAD7	IAD6	IAD5	IAD4	IAD3	IAD2	IAD1	IAD0
111	107	110	106	109	104	108	105

IREQ*	100	The interconnect request signal is generated by the MPC when an interconnect operation has been requested either from the local bus or from the iPSB bus. This signal remains active until the microcontroller performs arbitration.
IAST	101	The interconnect address strobe signal is an input to the MPC used to indicate that a valid address is on the interconnect bus.This signal may be directly connected to the ALE output of most microcontrollers. This signal must provide clean transitions.
IRD*	102	The interconnect bus read signal is an input to the MPC. This signal is used to perform a read operation to one of the MPC interconnect interface registers. This signal must provide clean transitions. When this signal is activated in conjunction with the IWR* signal, all MPC outputs are disabled.
IWR*	103	The interconnect bus write signal is an input to the MPC. This signal is used to perform a write operation to one of the MPC interconnect interface registers. This signal must provide clean transitions. When this signal is activated in conjunction with the IRD* signal, all MPC outputs are disabled.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	- 10°C to +80°C
Storage Temperature	- 65°C to +150°C
Supply Voltage to Ground Potential	- 0.5 V to +7.0 V
Applied Output Voltage	- 0.3V to VCC +0.5 V
Applied Input Voltage	- 0.5V to VCC +0.5 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliablity.

DC CHARACTERISTICS TA = 0°C to + 70°C, VCC = 5 V± 5%

Symbol	Parameter		Min	Max	Units	Test Conditions
VIL	Input LOW Voltage		- 0.5	0.8	V	
VIH	Input HIGH Voltage		2.0	VCC+0.5	V	
VOL	Output LOW Voltage	Open Drain		0.55	V	IOL Max
		All Others		0.45	V	IOL Max
VOH	Output HIGH Voltage		2.4		V	IOH Max
ILI	Input Leakage Current	Open Drain	–	± 400	µA	0 ≤ VIN ≤ VCC
		BBCLK	–	± 100	µA	0 ≤ VIN ≤ VCC
		All Others	–	± 10	µA	0 ≤ VIN ≤ VCC
IOL	Output LOW Current	Open Drain	60.0	–	mA	VOL = 0.55 V
		ADDIR and REFADR*	8.0	–	mA	VOL = 0.45 V
		All Others	4.0	–	mA	VOL = 0.45 V
IOH	Output HIGH Current		- 1.0	–		VOH = 2.4 V
ICC	Operating Supply Current		–	400	mA	

CAPACITANCE TA = + 25°C, FC = 1 MHz (Note 1)

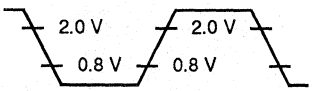
Symbol	Parameter		Min	Max	Units	Test Conditions
CI	Input Capacitance	BBCLK	–	15	pF	
		All Others	–	10	pF	
CIO	I/O Capacitance		–	20	pF	
COC	Output Capacitance		–	20	pF	

Notes:
1. Periodically sampled as opposed to 100% tested.

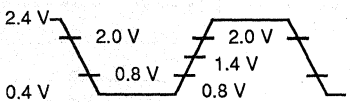
AC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ± 5%

Symbol	Parameter		Min	Max	Units	Test Conditions
T1	Address and BE* Set-Up To Command Active		30	–	ns	
	Select and DACK Set-Up To Command Active		24	–	ns	
T2	Address, BEn*, Select*, and DACK* Hold From Command Active		10	–	ns	
T3	Command Inactive		35	–	ns	
T4	Command Inactive To Read Data Disable (Note 6)		–	24	ns	
T5	Read Data Hold From Command Inactive		3	–	ns	
T6	Read Data Enable From Command Active		0	–	ns	
T7	WAIT* Active From Command Active		–	35	ns	CL = 50 pF
T8	Command Inactive From WAIT* Inactive		0	–	ns	
T9	WAIT* Inactive To Read Data Valid		–	50	ns	CL = 150 pF
T10	Command Active To Write Data Valid		–	200	ns	
T11	Write Data Hold From WAIT* Inactive		0	–	ns	
T12	Command Active To LOCK* Active (Note 2)		–	100	ns	
T13	LOCK* Hold From WAIT* Inactive (Note 3)		0	–	ns	
T14	Command Active		70	–	ns	
T15	Read Data Valid From Command Active		–	60	ns	CL = 150 pF
T16	Write Data Set-Up To Command Inactive	Registers	35	–	ns	
		DMA	25	–	ns	
T17	Write Data Hold From Command Inactive		5	–	ns	
T18	Command Active To MINT Or DREQ Inactive (Note 4,5)		–	70	ns	CL = 50 pF
T19	Command Active To DREQ* Inactive (Note 5)		–	45	ns	CL = 50 pF

AC TEST CONDITIONS

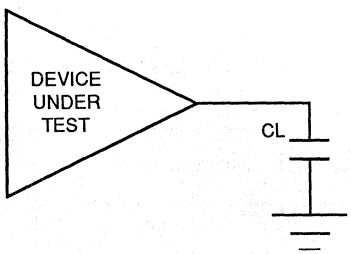


OUTPUT WAVEFORM TEST POINTS



INPUT WAVEFORM TEST POINTS
(1.4 V LEVEL FOR BBCLK ONLY)

AC TEST LOAD CIRCUIT



Notes:
2. Required to guarantee locking of resource.
3. Required to guarantee resource remains locked.
4. MINT deassertion only if no other sources are pending.
5. For DREQ inactive timing, T19 applies to a normal last transfer deassert condition and T18 to an error deassert condition.
6. Disable condition occurs when the output current becomes less than the input leakage specification.

TIMING DIAGRAMS

FIGURE 1 LOCAL BUS REFERENCE

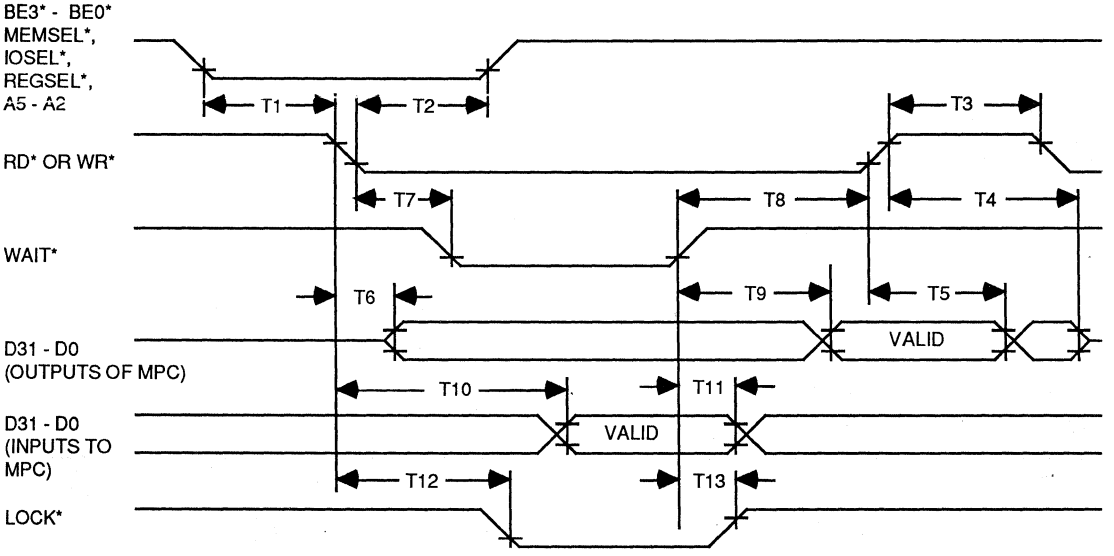
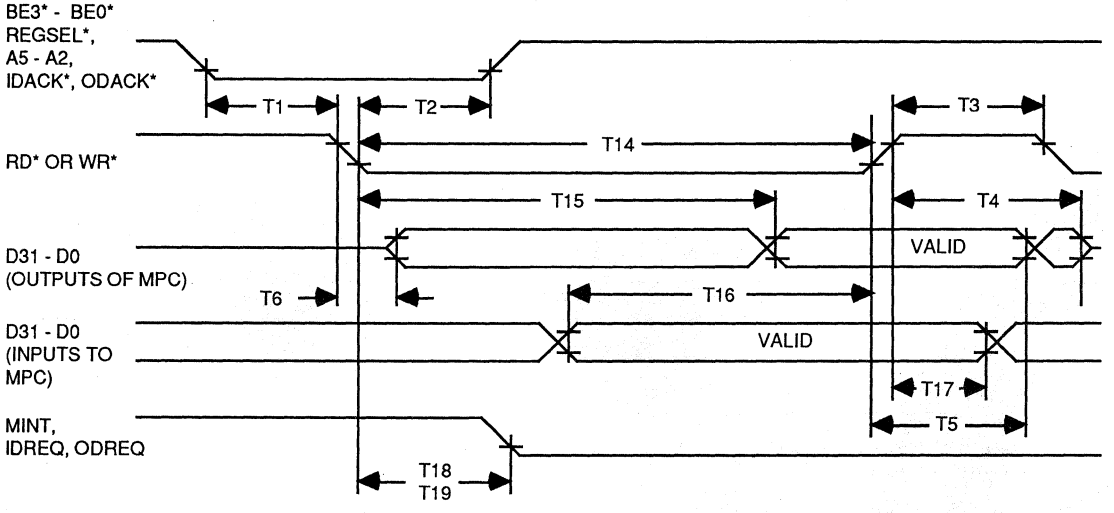


FIGURE 2. LOCAL BUS REGISTER AND DMA OPERATIONS

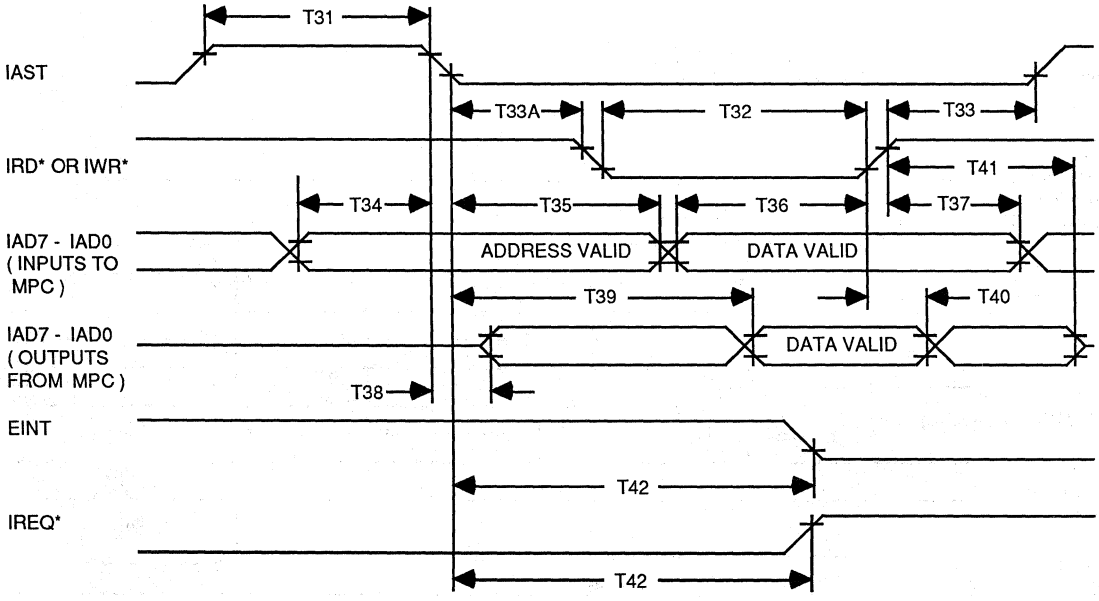


AC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ±5%

Symbol	Parameter	Min	Max	Units	Test Conditions
T31	IAST Active	85	–	ns	
T32	Command Active	250	–	ns	
T33	Command Inactive To IAST Active	25	–	ns	
T33A	IAST Inactive To Command Active	120	–	ns	
T34	Address Set-Up To IAST Inactive	40	–	ns	
T35	Address Hold From IAST Inactive	20	–	ns	
T36	Write Data Set-Up To Command Inactive	120	–	ns	
T37	Write Data Hold From Command Inactive	5	–	ns	
T38	Read Data Enable From Command Active	0	–	ns	
T39	Read Data Valid From Command Active	–	120	ns	CL = 150 pF
T40	Read Data Hold From Command Inactive	0	–	ns	
T41	Read Data Disable From Command Inactive (Note 8)	–	30	ns	
T42	EINT, IREQ* Inactive From Command Active (Note 7)	–	100	ns	CL = 50 pF

TIMING DIAGRAM

FIGURE 3. INTERCONNECT BUS



Notes:

7. EINT inactive only on write to error register. IREQ* inactive only on write to arbitration register.
8. Disable condition occurs when the output current becomes less than the input leakage specification.

AC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ±5%

Symbol	Parameter			Min	Max	Units	Test Conditions
TCP	Clock Period			99.9	–	ns	
TCL	BCLK* LOW Time			40	–	ns	
TCH	BCLK* HIGH Time			40	–	ns	
TBCL	BBCLK LOW Time			38	–	ns	
TBCH	BBCLK HIGH Time			38	–	ns	
TRB	BCLK* Rise Time			1.0	5.0	ns	
TFB	BCLK* Fall Time			1.0	2.0	ns	
TR	BBCLK Rise Time			0.5	1.0	ns	
TF	BBCLK Fall Time			0.5	1.0	ns	
TSK	BCLK* To BBCLK Skew (Note 9)			–0.5	4.0	ns	
TCD	Clock To Output Delay	BREQ*, BUSERR*, RSTNC* (Note 10)		–	36	ns	CL = 500 pF
		ARB5* - ARB0* (Note 10,11)		–	36	ns	CL = 500 pF
		BSC7* - BSC0*, BAD31* - BAD0*		–	29	ns	CL = 75 pF
		BPAR3* - BPAR0*, BSC9*, BSC8*		–	29	ns	CL = 50 pF
		SCDIR0, SCDIR1	HIGH To LOW	–	19	ns	CL = 25 pF
			LOW To HIGH	–	21	ns	CL = 25 pF
		ADDIR	HIGH To LOW	–	27	ns	CL = 50 pF
			LOW To HIGH	–	21	ns	CL = 50 pF
		REFADR*		–	29	ns	CL = 75 pF
		SEL*		–	29	ns	CL = 50 pF
TH	Hold Time From Clock	BREQ*, BUSERR*, RSTNC*		6.5	–	ns	
		ARB5* - ARB0* (Note 11)		6.5	–	ns	
		BAD31* - BAD0*, BPAR3* - BPAR0*		5.0	–	ns	
		BSC9* - BSC0*		4.0	–	ns	
		SCDIR0, SCDIR1		4.0	–	ns	
		ADDIR		5.0	–	ns	
		REFADR*		4.0	–	ns	
		SEL*		4.0	–	ns	

Notes:

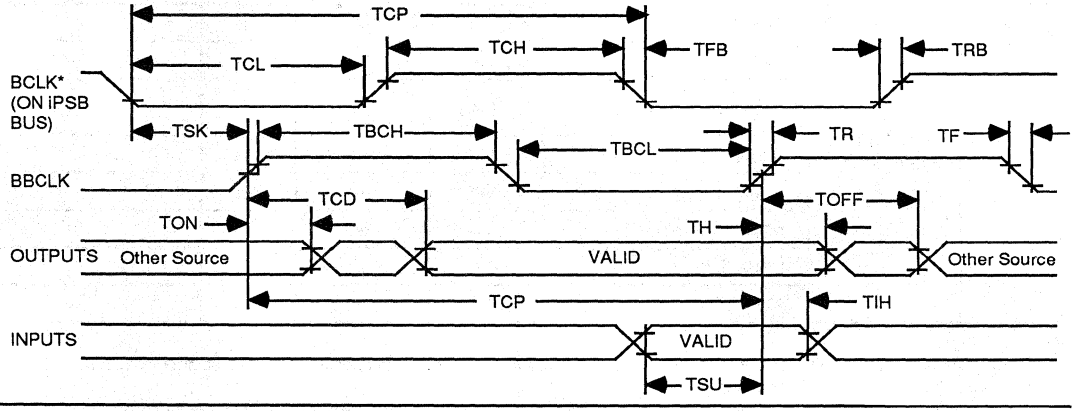
9. The clock timings are provided to reference the MPC specification to the iPSB bus specifications. These specifications assume a 74AS1804 or equivalent buffer.
10. The 500 pF load is a distributed value as defined in the iPSB bus specification. The open drain signals are designed such that the output delay and bus loss meets the iPSB specification requirement. An appropriate test condition that correlates to the distributed load will be determined during characterization.
11. The ARB5* ARB0* signal timings are with respect to the first and last clock of the arbitration period. Details can be found in the iPSB bus specification. Also, the arbitration logic has been designed to meet the loop delay specification accounting for the full path of input to output plus bus loss. An appropriate test condition will be determined during device characterization.

AC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ±5%

Symbol	Parameter		Min	Max	Units	Test Conditions
TON	Turn On Delay From Clock (Note 12)	BREQ*, BUSERR*, RSTNC*	6.5	–	ns	
		ARB5* - ARB0* (Note 9)	6.5	–	ns	
		BAD31* - BAD0*, BPAR3* - BPAR0*	5.0	–	ns	
		BSC9* - BSC0*	4.0	–	ns	
TOFF	Turn Off Delay From Clock (Note 13)	BREQ*, BUSERR*, RSTNC*	–	36	ns	
		ARB5* - ARB0* (Note 11)	–	36	ns	
		BAD31* - BAD0*, BPAR3* - BPAR0*	–	29	ns	
		BSC9* - BSC0*	–	29	ns	
TSU	Input Set-Up To Clock	BREQ*, BUSERR*, RSTNC*	22	–	ns	
		ARB5* - ARB0* (Note 11)	40	–	ns	
		BAD31* - BAD0*, BPAR3* - BPAR0*	24	–	ns	
		BSC9* - BSC0*	24	–	ns	
		TIMOUT, LACHN, RESET	24	–	ns	
		COM*, ERR*	40	–	ns	
TIH	Input Hold From Clock	BREQ*, BUSERR*, RSTNC*	0	–	ns	
		ARB5* - ARB0* (Note 11)	0	–	ns	
		BAD31* - BAD0*, BPAR3* - BPAR0*	3	–	ns	
		BSC9* - BSC0*	2	–	ns	
		TIMOUT, LACHN, RESET	2	–	ns	
		COM*, ERR*	3	–	ns	

TIMING DIAGRAM

FIGURE 4. iPSB BUS



Notes:

12. Minimum turn-on times are measured the same way as hold times. Specifically, the logic level driven by another device on the previous clock cycle must not be disturbed.
13. Maximum turn-off times are measured to the condition where the output leakage current becomes less than the input leakage specification.

VLSI TECHNOLOGY, INC.

SECTION 4
PERIPHERALS

Application Specific
Logic Products Division

VL16160

"RASTER OP" GRAPHICS/BOOLEAN OPERATION ALU

FEATURES

- Provides hardware assist for bit-mapped graphics operations. Includes 32-bit barrel shifter.
- Performance increase over software implementations:
  - Monochrome = 4 X Software
  - Color = 4 X (Planes) X Software
- Supports both CRT dispiays and such hardcopy devices as laser printers.
- Compatible with both monochrome and color displays.
- Implements all 256 possible raster operations on source, destination, and pattern data.
- 28- pin package; 5 V supply.

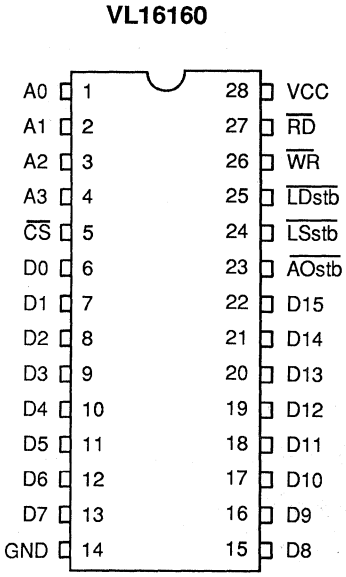
DESCRIPTION

The VL16160 Raster Op ALU (RALU) provides hardware-assisted performance enhancements for bit manipulation operations used in bit-mapped graphics displays. These operations, commonly called Bit Block Translation (BITBLT), allow bit-mapped images to be combined and manipulated by logical operators. These operators include AND, OR, and XOR, and can be used on source, destination, and pattern data. Additionally, support for masking with multiple mask registers for clipping is included.

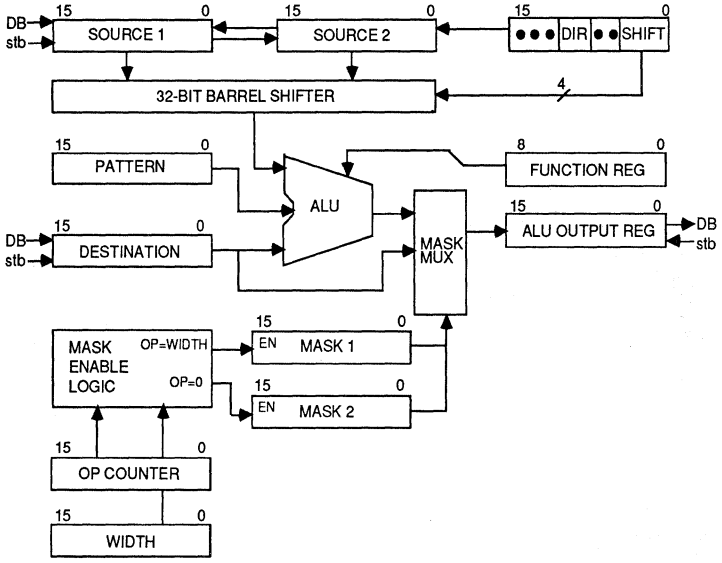
The BITBLT operation is general purpose enough to be used in a wide range of graphics operations, including text display using arbitrary fonts, attributes, and enhancements. Successive applications of BITBLTs can perform such operations as scaling, filling, rotations, and texturing.

In a typical application, the RALU operates on display data in 16-bit words that are latched into its input buffers by external hardware. Once source, destination, pattern, shift, and masking data are loaded into the RALU, the source data is bit-aligned with the destination data and the logical operation specified in the function register takes place. The results are stored in the ALU Output Register, which can be output onto the bus by a single strobe signal.

PIN DIAGRAM



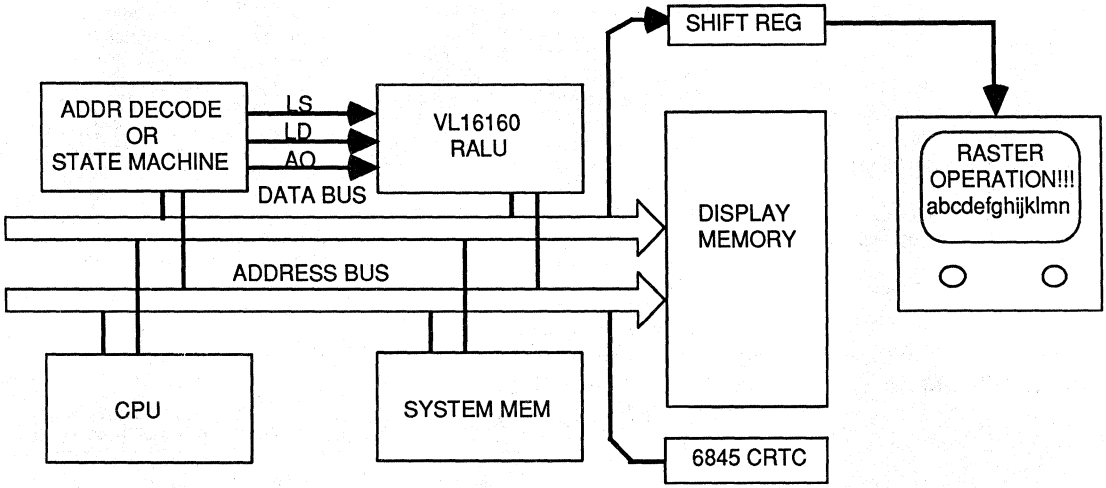
BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL16160PC	Plastic DIP
VL16160CC	Ceramic DIP
VL16160QC	Plastic Leaded Chip Carrier (PLCC)

FIGURE 1. TYPICAL APPLICATION



SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
D0-D15	6-15	Bidirectional data lines; input enabled by $\overline{CS}$ and $\overline{WR}$. Input data to Destination Register must be stable relative to the trailing edge of LDstb. Output enabled by $\overline{CS}$, $\overline{RD}$, and A0-A3 or $\overline{AO}$stb.
$\overline{CS}$	5	Chip Select ; Must be active to write to or read from internal registers.
$\overline{RD}$	27	Read Enable; Input used to strobe any internal register data to the data bus pins. Must be active in conjunction with $\overline{CS}$.
$\overline{WR}$	26	Write Enable; Input used to strobe data on data bus pins into the selected register. Must be active in conjunction with $\overline{CS}$.
A0-A3	1-4	Register Address; Address inputs that specify the internal chip register to be accessed for a read or write operation.
$\overline{AO}$stb	24	ALU Output Strobe; Input used to enable the output of the function decoder onto the data bus pins. Cannot be active when $\overline{CS}$ and $\overline{RD}$ or $\overline{WR}$ are active.
$\overline{LD}$stb	25	Load Destination Register Strobe; Input used to strobe the value (address) on the data bus pins into the Destination Register. Value on A0-A3 need not be valid when $\overline{LD}$stb is used to load the Destination Register. The $\overline{LD}$stb pin also decrements the op counter each time it is pulsed.
$\overline{LS}$stb	24	Load Source Register Strobe; Input used to strobe the value on the data bus into the Source Register specified by the Direction Bit. The other Source Register is loaded with the previous contents of the Source Register being loaded.
GND	14	Ground
VCC	28	+5 V ± 5%

FUNCTIONAL DESCRIPTION

The VL16160 consists of four basic blocks: Source Shifter, Function Decoder, Op Counter, and the Register set. The internal data bus is 16 bits wide, enabling all internal registers to be accessed easily from the I/O bus for context saving and restoring. In operation, the Source Shifter extracts data from the Source Registers and shifts the data to be aligned with the data in the Destination and Pattern Registers. The Function Decoder then performs a 16-bit Boolean operation as specified by the Function Register with the data extracted from the Source Registers and the data in the Destination and Pattern Registers. The result of the Boolean operation is available on the external I/O bus when the AOstb signal is strobed and can easily be written back into display memory. The Op counter and associated registers provide the support for clipping operations as required by the application.

SOURCE SHIFTER

The Source Shifter performs bit alignment on the concatenated 32 bits of data in the Source 1 and Source 2 Registers. The amount of bit alignment performed is based upon the value in the Shift Value Register. Thus, when LSstb is strobed, the Source Shifter extracts 16 contiguous bits from the 32 bits of data in the Source 1 and Source 2 registers as follows:

1. If the low order four bits of the Shift Value Register have a non-zero value, that value specifies the shift count by which the 16-bit field to be extracted is offset from bit 0 of the concatenated source registers, as shown in figure 2. The result is passed on to the Function Decoder.
2. If the low-order four bits of the Shift Value Register is 0, the contents of either Source 1 or Source 2 are passed directly to the Function Decoder and no shifting occurs. The direction bit indicates which source register is used in the operation, as shown in figure 2.

FUNCTION DECODER

The Function Decoder performs a Boolean operation on the contents of the Destination Register, Pattern Register, and the output of Source Shifter. The Boolean operation is specified by the Function Register. With the three operands, 256 different Boolean operations are possible. The result of the operation is available on the I/O bus when the AOstb control signal is active. AOstb signal cannot be active at the same time that $\overline{CS}$ and $\overline{RD}$ or $\overline{WR}$ are active. The result of the Boolean operation is also available by reading the ALU Output Register.

To understand how the Function Decoder performs the desired Boolean operation, note again that with three operands, (data in the Source, Pattern and Destination Registers), a total of 256 different boolean operations is possible. Out of these 256 possible operations, the application defines which are needed to perform the desired task.

For example (see figure 3), to "paint" a new image over an existing image requires the source data (image) to be ORed with the destination data (image). This means "Source Register or Destination Register". For each bit, there are four possible results of this operation between these two registers. However, since the Pattern Register is always included, even when it is a "don't care," a total of eight different possible results of this one Boolean operation is possible. These eight combinations define the "function code" for the OR operation. Thus, the function code is really defined as the result (and the only result possible) of a Boolean combination of the Source, Destination, and Pattern Registers. In using the VL16160, the application defines which of the 256 possible Boolean combinations of the Source, Destination and Pattern Registers define those "functions" required of the application, and when that "function" is required, the corresponding function code is loaded into the Function Register.

In principal, the Function Decoder operates on a bit-by-bit basis as a 1-of-8 data selector with each data bit in the Source, Destination, and Pattern Registers selecting one of eight bits of data from the Function Register.

The function codes required of an application are determined ahead of time by the user and stored in memory to be used as needed. The determination of the correct function code is a matter of simply applying the definitions stated above (see figure 3), in a simple method. The truth table for Pattern, Source, and Destination bits is written, with the desired output. This desired output is read as the desired value of the Function Register, with the least significant bit as shown in figure 3. Using this method, the software engineer can easily define a pattern to suit each specific need.

OP COUNTER

The Op Counter, in conjunction with the Width and Mask Registers, provides for masking of selected bits in the Destination Register. This masking prevents the VL16160 from modifying selected areas of display memory when performing BITBLTs. For example, clipping may be required at the edges of a window. The function of the Op Counter is to keep track of the beginning and end of each row, so that the mask registers can handle this clipping automatically, without additional processor intervention.

The Op Counter must be correctly initialized prior to the beginning of a raster operation. The enabling of masking is internally clocked by the LDstb signal. For this reason, after loading the Op counter with an initial value, LDstb must be pulsed before the LSstb of the first operation. Since this LDstb will decrement the Op Counter, it is necessary to increment the Op Counter to be one more than the intended value, so that this "dummy" LDstb starts out the BITBLT with the correct Op Counter value. This "dummy" LDstb does have to be repeated between scanlines, as the masking remains enabled. If context switching is utilized, however, reinitialization (with the loading of Op Counter and subsequent LDstb) is necessary before leaving a context, or upon re-entering one, in the middle of a BITBLT.

REGISTER DESCRIPTION

As shown in the block diagram, the RALU consists of a number of registers, each connected to the internal 16-bit data path. Of these registers, three are used very often and are directly accessible from the data bus by the assertion of strobe signals.

SOURCE
The Source Register holds a 16-bit word of data to be modified by a raster operation. It is loaded from the data bus by the assertion of the LSstb signal.

DESTINATION
The Destination Register holds a word of data from the bit-mapped display that is modified by the source data and raster operation. It is loaded from the data bus by the assertion of the LDstb signal.

ALU OUTPUT
The ALU Output Register holds the result of the raster operation to be written back to memory. The contents may be put onto the data bus by the assertion of the AOstb signal.

The remainder of the registers are typically set up for a series of operations and are not changed until the end of a scan line.

DIR / SHIFT
This register controls the direction of the raster operation (left-to-right or right-to-left). In addition, it specifies the number of bits to shift to align the source with the destination fields.

MASK 1 and 2
These registers are used to define the left and right boundaries of the area on the screen that is manipulated. (The direction bit affects which register corresponds to left vs. right). A bit set in these registers allows the corresponding bit in the Destination Register to pass through unaltered. When the Op Counter is equal to the Width Register (usually for the first raster operation on each scan line), the Mask 1 Register selects bits to be included in the operation. Masking is disabled until the Op Counter is zero (usually for the last operation on a scan line); at that time, the Mask 2 register is used.

PATTERN
This register contains data to be combined with the output of the bit-shifted source register. This is commonly used for enhancing an image with a background pattern.

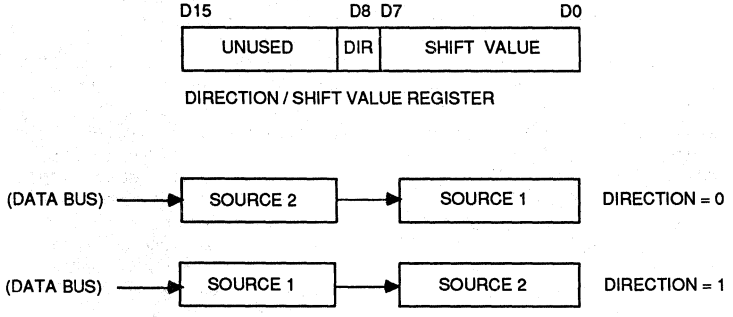
FUNCTION
This register contains the operator that is used to combine the source, destination, and pattern data.

OP COUNTER
The Op Counter Register specifies the current count of the operation in progress. The Op Counter is decremented each time LDstb is brought active. After the Op counter goes to zero, the next LDstb causes the Op counter to be reloaded with the value of the Width register prior to the next operation. The Op counter can be set to the value of the Width Register at the start of a raster operation by beginning an operation with a "dummy" LDstb. This loads the Op counter in preparation for the first scan line.

WIDTH
The Width Register specifies the width of the line (in 16-bit words) on which raster operations will take place.

FLAG REGISTER
The Flag Register is uncommitted and can be used to temporarily store context information for multi-tasking implementations.

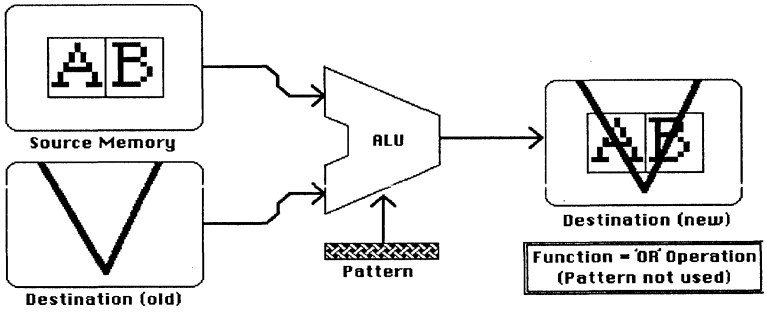
FIGURE 3. SHIFTING AND DIRECTION



REGISTER MAP

0	Destination Register
1	Source 1 Register
2	Source 2 Register
3	Pattern Register
4	Mask 1 Register
5	Mask 2 Register
6	Shift Value Register
7	Function Register
8	Width Register
9	Operation Count Register
10	ALU Output Register
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Flag Register

FIGURE 3. RASTER OPERATIONS EXAMPLE



Pattn	Source	Dest	Funct
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

MSB

LSB

Example

Source XOR Destination = 66 (hex)

Pattn	Source	Dest	Funct
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

MSB

LSB

Example

= Pattn

Source XOR Destination OR Pattern = F6 (hex)

Pattn	Source	Dest	Funct
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

MSB

LSB

Example

Source OR Destination = EE (hex)

Pattn	Source	Dest	Funct
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

MSB

LSB

Example

= Pattn

Source OR Destination OR Pattern = FE (hex)

Pattn	Source	Dest	Funct
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

MSB

LSB

Example

Source AND Destination = 88 (hex)

Pattn	Source	Dest	Funct
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

MSB

LSB

Example

= Pattn

Source AND Destination OR Pattern = F8 (hex)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.5 V to +7.0 V
Input Voltage	-0.5 V to +7.0 V
Output Voltage	-0.5 V to +7.0 V
Operating Temperature	0 °C to +70 °C
Storage Temperature	-65 °C to +150 °C
Lead Temperature (10 s.)	300 °C
Junction Temperature	175 °C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device under these or any other conditions above those listed in this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ± 0.25 V

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
VIH	HIGH-Level Input Voltage		2.4			V	
VIL	LOW-Level Input Voltage				0.6	V	
VOH	HIGH-Level Output Voltage		2.4			V	VCC=Min; IOH=-400 µA
VOL	LOW-Level Output Voltage			0.3	0.45	V	VCC=Min; IOL=4.4 mA
IOH	HIGH-Level Output Current		-400			µA	
IOL	LOW-Level Output Current		4.4			mA	
IIL	Input Leakage Current				10	µA	VI = 0.45 V
II/O	I/O Leakage Current	0.7 V < Vo < Vcc			20	µA	
		0.4 V < Vo < Vcc			100		
ICC	Power Supply Current at DC				120	mA	VCC = Max

CAPACITANCE TA = 0°C to +70°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CI/O	I/O Capacitance			15	pF	
CI	Input Capacitance		6	15	pF	

AC TIMING CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ± 0.25 V

Symbol	Parameter	Min	Max	Unit	Conditions
tCSH	$\overline{CS}$, A0-A3 Hold After $\overline{WR}$ Active	20		ns	
tRWW	$\overline{WR}$, $\overline{RD}$ Signal Width	60		ns	
tCSS	$\overline{CS}$, A0-A3 Setup to $\overline{WR}$ Inactive	0		ns	
CSV	Data Valid After $\overline{CS}$ Active		120	ns	
tRDV	Data Valid After $\overline{RD}$ Active		120	ns	
tRDH	Data Valid After $\overline{RD}$, $\overline{CS}$ Inactive	5		ns	
tWRS	Data Setup to $\overline{WR}$ Inactive	50		ns	
tWRH	Data Hold After $\overline{WR}$ Inactive	30		ns	
tLSW	$\overline{LSstb}$ Pulse Width	60		ns	
tNLS	Time Between $\overline{LSstb}$ Pulses	0		ns	
tSDV	$\overline{LSstb}$ Inactive to Valid Data		120	ns	
LSF	$\overline{LSstb}$ Inactive to $\overline{AOstb}$ Active	30		ns	
tLDV	$\overline{LSstb}$ Active to Valid Data		170	ns	
tLDW	$\overline{LDstb}$ Pulse Width	60		ns	
tNLD	Time Between $\overline{LDstb}$ Pulses	150		ns	
tLDF	$\overline{LDstb}$ Inactive to $\overline{AOstb}$ Active	20		ns	
tLSS	Data Setup to $\overline{LSstb}$ Inactive	20		ns	
tLSH	Data Hold after $\overline{LSstb}$ Inactive	25		ns	
tLDS	Data Setup to $\overline{LDstb}$ Inactive	30		ns	
tLDH	Data Hold After $\overline{LDstb}$ Inactive	25		ns	
tFOV	Data Valid After $\overline{AOstb}$ Active		120	ns	
tDDV	Data Valid After Valid $\overline{LDstb}$ Data		140	ns	
tFDV	Bus High-Impedence After $\overline{AOstb}$ Inactive		40	ns	

FIGURE 4. REGISTER READ/WRITE TIMING

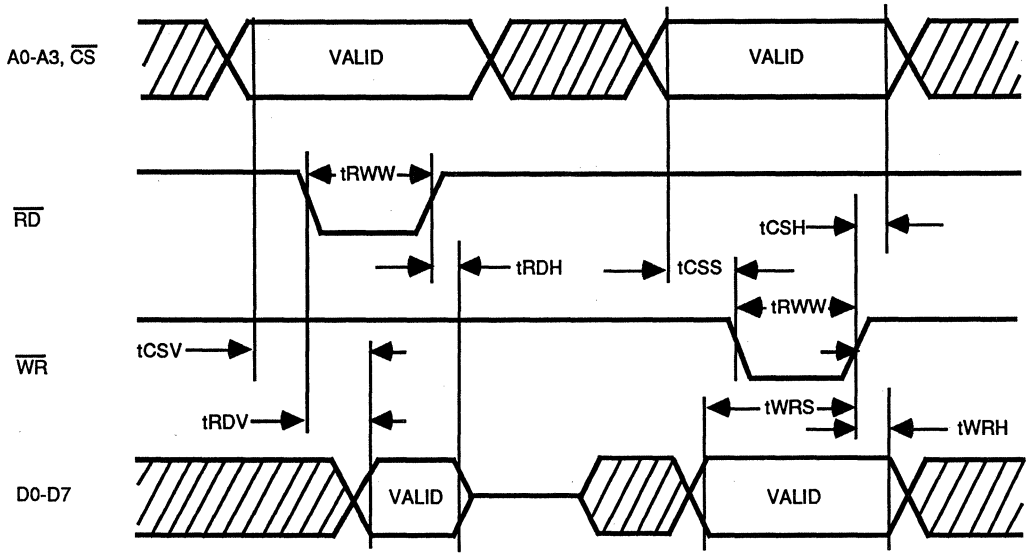
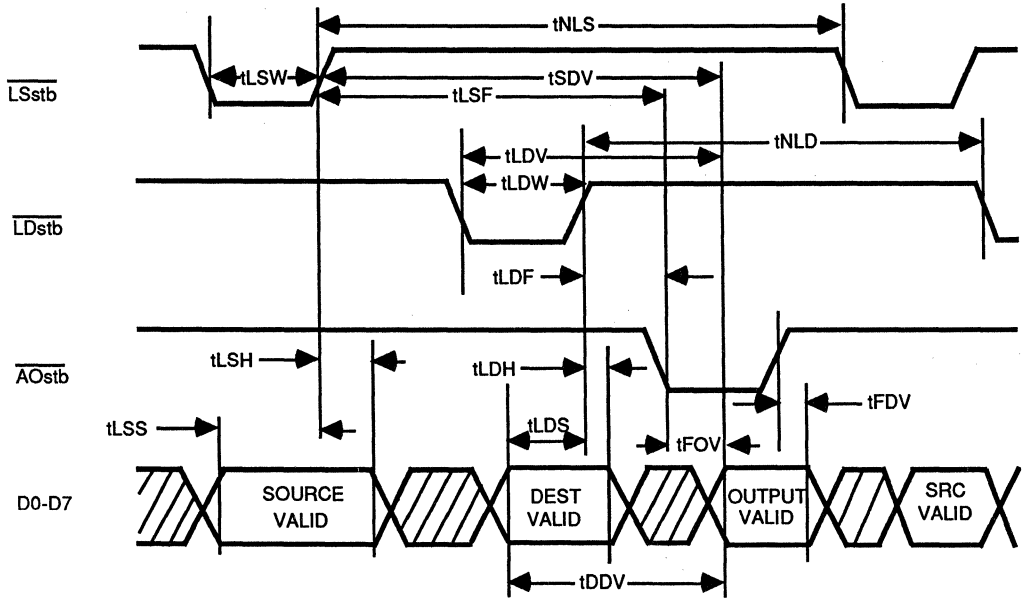


FIGURE 5. SOURCE REGISTER AND ALU OUTPUT CONTROL SIGNAL TIMING



VL1772-02

$5^1/_4$ - INCH FLOPPY DISK CONTROLLER/FORMATTER

FEATURES

- Built-in data separator
- Built-in write precompensation
- 5 1/4-inch single and double density
- Motor control
- 128, 256, 512, or 1024 sector lengths
- TTL compatible
- 8-bit bidirectional data bus
- Fast step rates
- 28-pin DIP
- Single 5 V power supply

DESCRIPTION

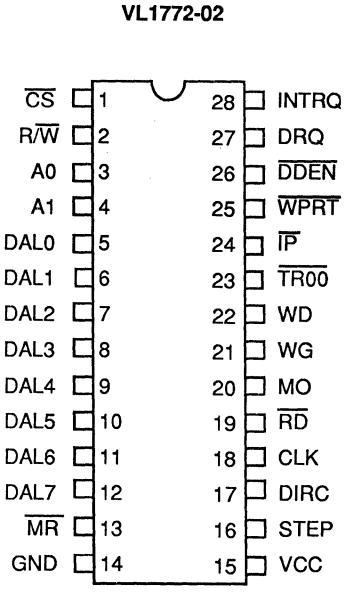
The VL1772-02 is a MOS/LSI device that performs the functions of a 5 1/4-inch Floppy Disk Controller/Formatter. It replaces the older 1770-type device.

The drive side of the interface needs no additional logic except for buffers/receivers. Designed for 5 1/4-inch single-or double-density operation, the device contains a programmable Motor On signal.

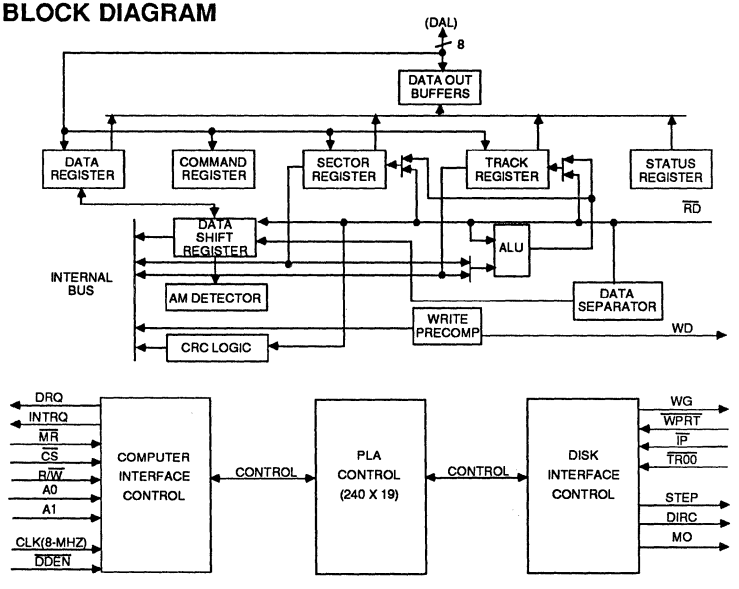
The VL1772-02 is implemented in NMOS silicon gate technology and is available in a 28-pin dual-in-line package. It is a low-cost version of the WD179X Floppy Disk Controller/Formatter and is compatible with generic 179X types. It also has a built-in digital data separator and write precompensation circuits. A single read line (RD, pin 19) is the only input required to recover serial FM or MFM data from the disk drive. The device has been specifically designed for control of 5 1/4-inch floppy disk drives with data rates of 125K bits/s (single density) and 250K bits/s (double density). In addition, it can write a precompensation that is125 ns from nominal, and can be enabled at any point through simple software commands. Another programmable feature, Motor On, has been incorporated to automatically enable the spindle motor prior to operating a selected drive. The VL1772-02 offers stepping rates of 2, 3, 6, and 12 ms.

The processor interface consists of an 8-bit bidirectional bus for transfer of status, data, and commands. All host communication with the drive occurs through these data lines. They are capable of driving one standard TTL load or three LS loads.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL1772-02PC	Plastic DIP
VL1772-02QC	Plastic Leaded Chip Carrier
VL1772-02CC	Ceramic DIP

Note:
Operating temperature range: 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
$\overline{CS}$	1	Chip Select - A logic low on this input selects the chip and enables host communication with the device.
R/$\overline{W}$	2	Read/Write - A logic high on this input controls the placement of data on the $\overline{D0}$-$\overline{D7}$ lines from a selected register, while a logic low causes a write operation to a selected register.
A0, A1	3, 4	Address 0, 1 - These two inputs select a register to read or write data:

$\overline{CS}$	A1	A0	R/$\overline{W}$ = 1	R/$\overline{W}$ = 0
0	0	0	Status Register	Command Register
0	0	1	Track Register	Track Register
0	1	0	Sector Register	Sector Register
0	1	1	Data Register	Data Register

DAL0 - DAL7	5 - 12	Data Access Lines 0 through 7 - Eight-bit bidirectional bus used for transfer of data, control, or status. This bus is enabled by $\overline{CS}$ and R/$\overline{W}$. Each line drives one TTL load.
$\overline{MR}$	13	Master Reset - A logic low pulse on this line resets the device and initializes the status register (internal pull-up).
GND	14	Ground - Ground
VCC	15	Power Supply - +5 V ±5% power supply input.
STEP	16	Step - The Step output contains a pulse for each step of the drive's R/$\overline{W}$ head. This is a pulse to the disk drive.
DIRC	17	Direction - The Direction output is high when stepping in towards the center of the diskette, and low when stepping out.
CLK	18	Clock - This input requires a free-running 50% duty cycle clock (for internal timing) at 8 MHz ±1%.
$\overline{RD}$	19	Read Data - This active-low input is the raw data line containing both clock and data pulses from the drive.
MO	20	Motor On - Active high output used to enable the spindle motor prior to read, write, or stepping operations.
WG	21	Write Gate - This output is made valid prior to writing on the diskette.
WD	22	Write Data - FM or MFM clock and data pulses are placed on this line to be written on the diskette.
$\overline{TR00}$	23	Track 00 - This active-low input informs the VL1772-02 that the drive's R/$\overline{W}$ heads are positioned over Track zero (internal pull-up).
$\overline{IP}$	24	Index Pulse - This active-low input informs the VL1772-02 when the physical index hole has been encountered on the diskette (internal pull-up).
$\overline{WPRT}$	25	Write Protect - This input is sampled whenever a Write Command is received. A logic low on this line prevents any Write Command from executing (internal pull-up).
$\overline{DDEN}$	26	Double Density Enable - This input pin selects either single (FM) or double (MFM) density. When $\overline{DDEN}$ = 0, double density is selected (internal pull-up).
DRQ	27	Data Request - This active-high output indicates that the Data Register is full (on a Read) or empty (on a Write) operation.
INTRQ	28	Interrupt Request - This active-high output is set at the completion of any command or a read of the Status Register.

ARCHITECTURE

TheVL1772-02 Floppy Disk Controller/Formatter block diagram is illustrated on the front page. The primary sections include the parallel processor interface and the floppy disk interface.

Data Shift Register - This 8-bit register assembles serial data from the Read Data input ($\overline{RD}$) during read operations and transfers serial data to the Write Data output during write operations.

Data Register - This 8-bit register is used as a holding register during disk read and write operations. In disk read operations, the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In disk write operations, information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command, the Data Register holds the address of the desired track position. This register is loaded from the Data Access Lines (DAL) and gated onto the DAL under processor control.

Track Register - This 8-bit register holds the track number of the current read/write head position. It is incremented by one every time the head is stepped in and decremented by one every time the head is stepped out (towards Track 00). The contents of the register are compared with the recorded track number in the ID field during disk read, write, and verify operations. The Track Register can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Sector Register (SR) - This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk read or write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) - This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy, unless the new command is a forced interrupt. The Command Register can be loaded from the DAL but not read onto the DAL.

Status Register (STR) - This 8-bit register holds device status information. The meaning of the status bits is a function of the type of command previously executed. This register can be read onto the DAL but not loaded from the DAL.

CRC Logic - This logic is used to check or to generate the 16-bit cyclic redundancy check (CRC). The polynomial is:

$$G(x) = x^{16} + x^{12} + x^5 + 1$$

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

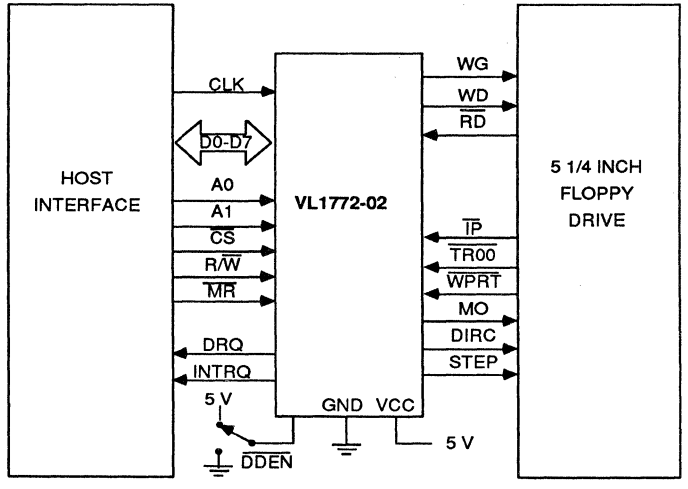
Arithmetic/Logic Unit (ALU) - The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk-recorded ID field.

Timing and Control - All computer and floppy disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock. The VL1772-02 has two different modes of operation according to the state of $\overline{DDEN}$: When $\overline{DDEN}$ = 0, double density (MFM) is enabled. When $\overline{DDEN}$ = 1, single density is enabled.

Address Mark Detector - The AM detector detects ID, data, and index address marks during read and write operations.

Data Separator - A digital data separator, consisting of a ring shift register and data window detection logic, provides read data and a recovery clock to the AM detector.

FIGURE 1. SYSTEM BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight data access lines (DALs) and associated control signals. The DALs are used to transfer data, status, and control words out of, or into the VL1772-02. The DALs are three-state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) = 0 and R/$\overline{W}$ = 1 are active, or act as input receivers when $\overline{CS}$ and R/$\overline{W}$ = 0 are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signal R/$\overline{W}$ during a read or write operation, are interpreted as selecting the following registers:

A1	A0	READ (R/$\overline{W}$ = 1)	WRITE (R/$\overline{W}$ = 0)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

After any register is written to, the same register cannot be read from until 16 µs in MFM or 32 µs in FM have elapsed.

During direct memory access (DMA) types of data transfers between the Data Register of the VL1772-02 and the processor, the Data Request (DRQ) output is used in data transfer control. This signal also appears as status bit 1 during read and write operations.

On disk read operations, the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The read operation continues until the end of sector is reached.

On disk write operations, the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the floppy disk, a byte of zeros is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated; it is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The VL1772-02 has two modes of operation, according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK input is at 8 MHz.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512, or 1024 bytes are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logical "1". For MFM formats, $\overline{DDEN}$ should be placed to a logical "0".

Sector lengths are determined at format time by the fourth byte in the "ID" field.

SECTOR LENGTH TABLE	
SECTOR LENGTH FIELD (HEX)	NUMBER OF BYTES IN SECTOR (DECIMAL)
00	128
01	256
02	512
03	1024

There are from 0 to 244 sectors per track for the VL1772-02, and from 0 to 244 tracks.

GENERAL DISK WRITE OPERATION

When writing is to take place on the disk the Write Gate (WG) output is activated, allowing current to flow into the read/write head. As a precaution to erroneous writing, the first data byte must be loaded into the Data Register in response to a Data Request from the device before the Write Gate signal can be activated.

Writing is inhibited when the Write Protect input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated, and the Write Protect status bit is set.

For write operations, the VL1772-02 provides Write Gate to enable a write condition, and Write Data which consists of a series of active-high pulses. These pulses contain both clock and data information in FM and MFM. Write Data provides the unique missing clock patterns for recording address marks.

The Precompensation Enable bit in Write commands allow automatic write precompensation to take place. The outgoing write data stream is delayed or advanced from nominal by 187ns according to the following table:

PATTERN				MFM	FM
X	1	1	0	Early	N/A
X	0	1	1	Late	N/A
0	0	0	1	Early	N/A
1	0	0	0	Late	N/A

Next Bit to be sent
Current Bit sending
Previous Bits sent

Precompensation is typically enabled on the innermost tracks where bit shifts usually occur and bit density is at its maximum.

COMMANDS

The VL1772-02 accepts eleven commands. Command words should only be loaded in the Command Register when the Busy Status Bit is off (Status Bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy Status Bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault-free. For ease of discussion, commands are divided into four types and are summarized in Table 1.

The Type I Commands (see Figure 2) include the Restore, Seek, Step, Step-in, and Step-out commands. Each of the Type I Commands contains a rate field (r0, r1), which determines the stepping motor rate.

A 4 µs (MFM) or 8 µs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active-high when stepping in and low when stepping out. The Direction signal is valid 24 µs before the first stepping pulse is generated.

After the last directional step, an additional 30 ms of head settling time takes place if the Verify flag is set in Type I commands. There is also a 30 ms head settling time if the E flag is set in any Type II or III command.
When a Seek, Step, or Restore command is executed, an optional verification of read/write head position can be performed by setting bit 2 (V = 1) in the command word to logic 1. The verification operation begins at the end of the 30 ms settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field cyclic redundancy check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC Error Status Bit is set (Status Bit 3), and the next encountered ID field is read from the disk for the verification operation.

The VL1772-02 must find an ID field with correct track number and correct CRC within five revolutions of the media, otherwise, the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

All commands, except the Force Interrupt command, may be programmed via the h Flag to delay for spindle motor start up time. If the h Flag is not set and the Motor On line is low when a command is received, the VL1772-02 will force Motor On to a logic 1 and waits six revolutions before executing the command. At 300 RPM, this guarantees a one-second spindle start-up time. If, after finishing the command, the device

TABLE 1. COMMAND SUMMARY

TYPE	COMMAND	BITS 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step-in	0	1	0	u	h	V	r_1	r_0
I	Step-out	0	1	1	u	h	V	r	r_0
II	Read Sector	1	0	0	m	h	E	0	0
II	Write Sector	1	0	1	m	h	E	P	a_0
III	Read Address	1	1	0	0	h	E	0	0
III	Read Track	1	1	1	0	h	E	0	0
III	Write Track	1	1	1	1	h	E	P	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

FLAG SUMMARY

TYPE I COMMANDS

h = Motor On Flag (Bit 3)

h = 0, Enable Spin-up Sequence
h = 1, Disable Spin-up Sequence

V = Verify Flag (Bit 2)

V = 0, No Verify
V = 1, Verify on Destination Track

r_1, r_0 = Stepping Rate (Bits 1,0)

r_1	r_0	1772-02
0	0	6 ms
0	1	12 ms
1	0	2 ms
1	1	3 ms

u = Update Flag (Bit 4)

u = 0, No Update
u = 1, Update Track Register

TYPE II & III COMMANDS

m = Multiple Sector Flag (Bit 4)

m = 0, Single Sector
m = 1, Multiple Sector

H = Motor On Flag (Bit 3)

H = 0, Enable Spin Up Sequence
H = 1, Disable Spin Up Sequence

a_0 = Data Address Mark (Bit 0)

a_0 = Write Normal Data Mark
a_0 = 1, Write Deleted Data Mark

E = 15ms Settling Delay (Bit 2)

E = 0, No Delay
E = 1, Add 15ms Delay

P = Write Precompensation (Bit 1)

P = 0,Enable Write Precomp
P = 1,Disable Write Precomp

TYPE IV COMMANDS

I_3-I_0 Interrupt Condition (Bits 3-0)

I_0 = 1, Not Used
I_1 = 1, Not Used
I_2 = 1, Interrupt on Index Pulse
I_3 = 1, Immediate Interrupt
I_3-I_0 = 0, Terminate without interrupt

remains idle for ten revolutions, the Motor On line goes back to a logic 0. If a command is issued while Motor On is high, the command executes immediately, defeat-ing the six-revolution start up. This feature allows consecutive read or write commands without waiting for each motor start-up; the VL1772-02 assumes the spindle motor is up to speed.

RESTORE (SEEK TRACK 0)

Upon receipt of this command, the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active-low indicating the read/write head is positioned over Track 00, the Track Register is loaded with zeros and an interrupt is generated. If $\overline{TR00}$ is not active-low, stepping pulses (pin 16) at a rate specified by the r1, r0 field are issued until the $\overline{TR00}$ input is activated. At this time, the Track Register is loaded with zeros and an interrupt is generated. If the $\overline{TR00}$ input does not go active-low after 255 stepping pulses, the VL1772-02 terminates operation, interrupts, and sets the Seek Error Status Bit, providing the V flag is set. A verification operation also takes place if the V flag is set. The h bit allows the Motor On option at the start of command.

FIGURE 2. TYPE I COMMAND FLOWCHART

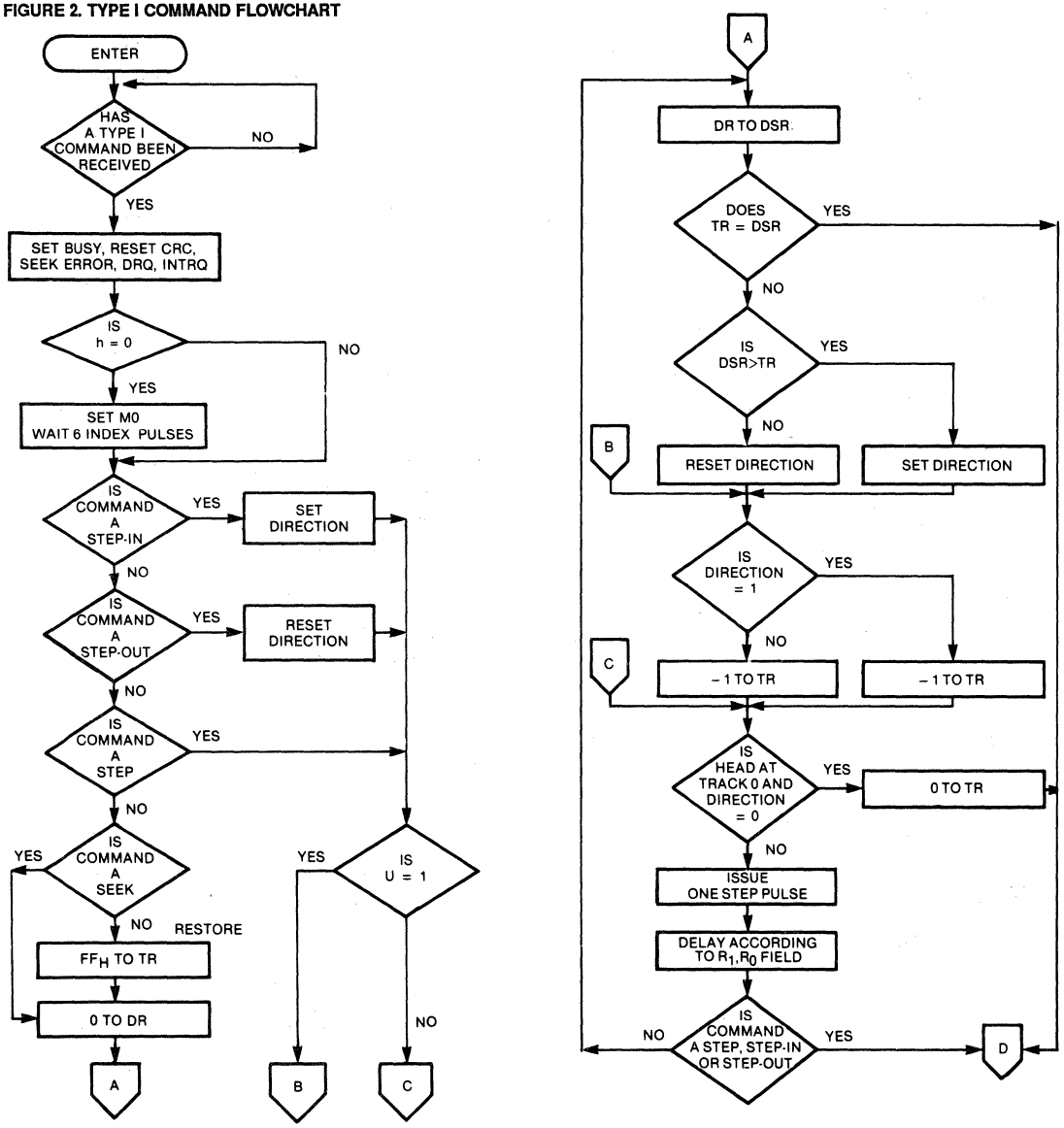


FIGURE 2. TYPE I COMMAND FLOWCHART (Cont.)

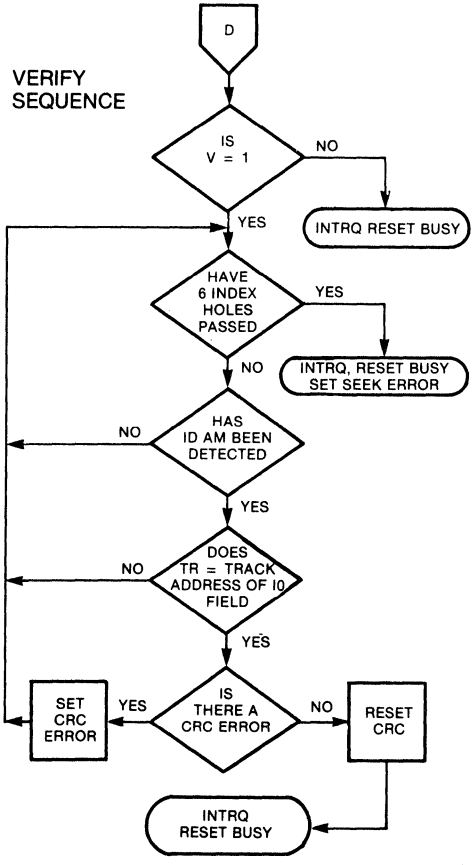
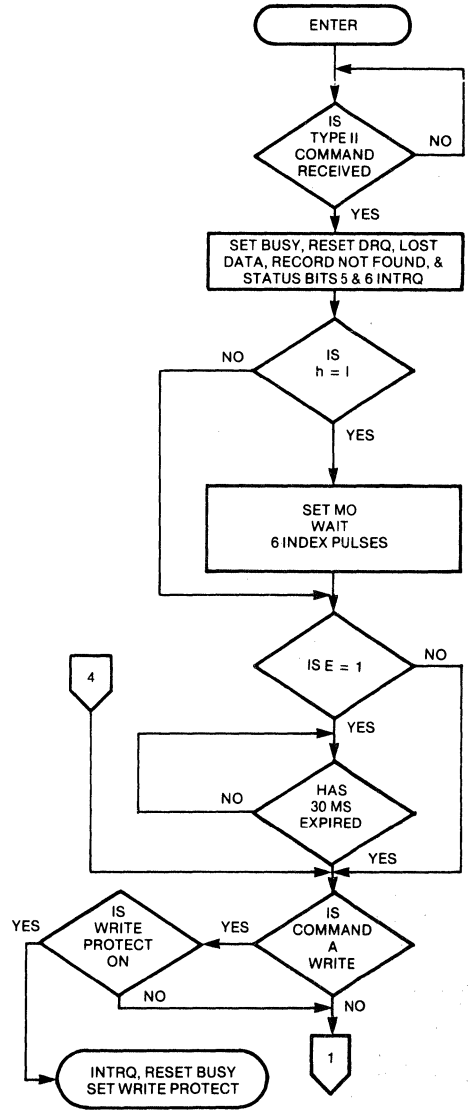


FIGURE 3. TYPE II COMMAND FLOWCHART



SEEK

This command assumes that the Track Register contains the track number of the current position of the read/write head and the Data Register contains the desired track number. The VL1772-02 will update the Track Register and issue stepping pulses in the appropriate direction until the contents of the Track Register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command. (Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.)

STEP

Upon receipt of this command, the VL1772-02 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1, r0 field, a verification takes place if the V flag is on. If the U flag is on, the Track Register is updated. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the VL1772-02 issues one stepping pulse in the direction towards track 76. If the U flag is on, the Track Register is incremented by one. After a delay is determined by the r1, r0 field, a verification takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the VL1772-02 issues one stepping pulse in the direction towards track 0. If the U flag is on, the Track Register is decremented by one. After a delay determined by the r1, r0 field, a verification takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands (see Figure 3) are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status bit is set. If the E flag = 1, the command executes after a 15 ms delay.

When an ID field is located on the disk, the VL1772-02 compares the track number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the sector number of the ID field is compared with the Sector Register. If there is not a sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and is either written into or read from depending upon the command. The VL1772-02 must find an ID field with a track number, sector number, and CRC within four revolutions of the disk; otherwise, the Record Not Found Status Bit is set (Status Bit 4) and the command is terminated with an interrupt (INTRQ).

Each of the Type II Commands contains an m flag that determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The VL1772-02 continues to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: if the VL1772-02 is instructed to read sector 27 and there are only 26 sectors on the track, the sector register exceeds the number available. The VL1772-02 will search for five disk revolutions, interrupt out, reset busy, and set the Record Not Found Status Bit.

READ SECTOR

Upon receipt of the Read Sector command, the Busy status bit is set, and when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The data address mark (DAM) of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the ID field is searched for and verified again followed by the data address mark search. If, after five revolutions the DAM cannot be found, the Record Not Found StatusBit is set and the operation is terminated. When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred, that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been input to the computer. If there is a CRC error at the end of the data field, the CRC Error Status Bit is set, and the command is terminated (even if it is a multiple record command).
At the end of the read operation, the type of data address mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The VL1772-02 counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the disk. At this time, the

FIGURE 3. TYPE II COMMAND FLOWCHART (Cont.)

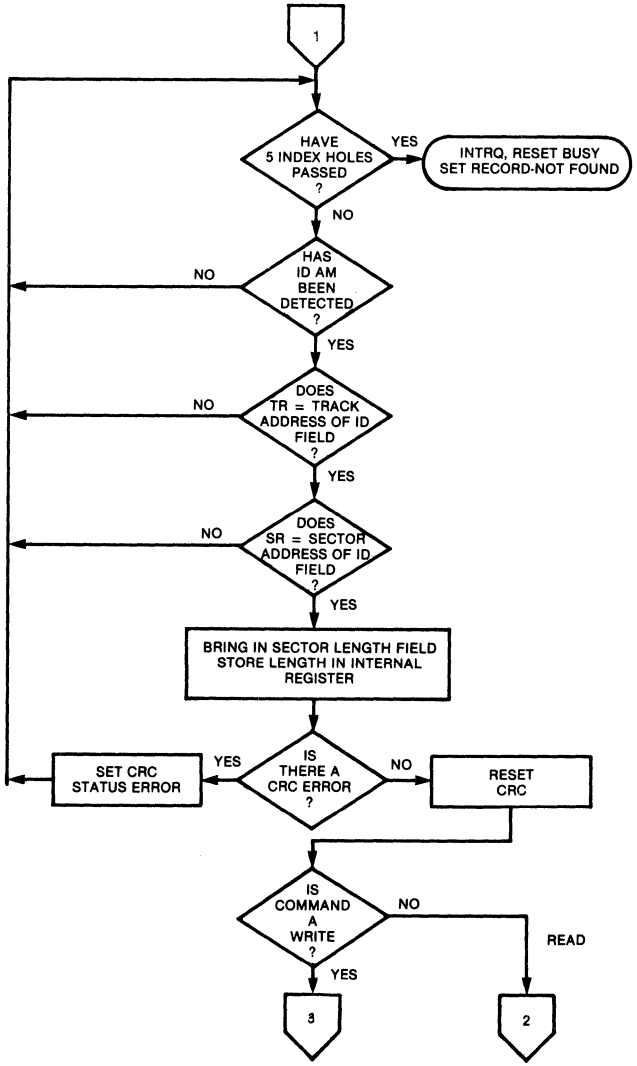


FIGURE 3. TYPE II COMMAND FLOWCHART (Cont.)

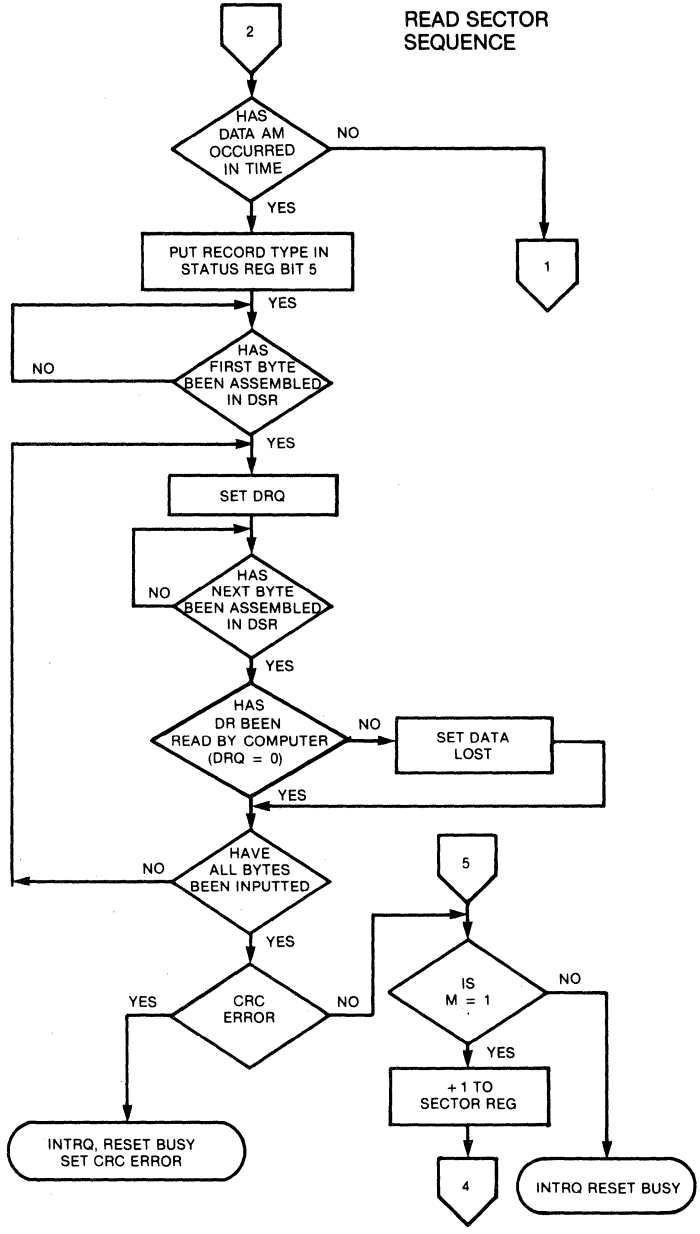
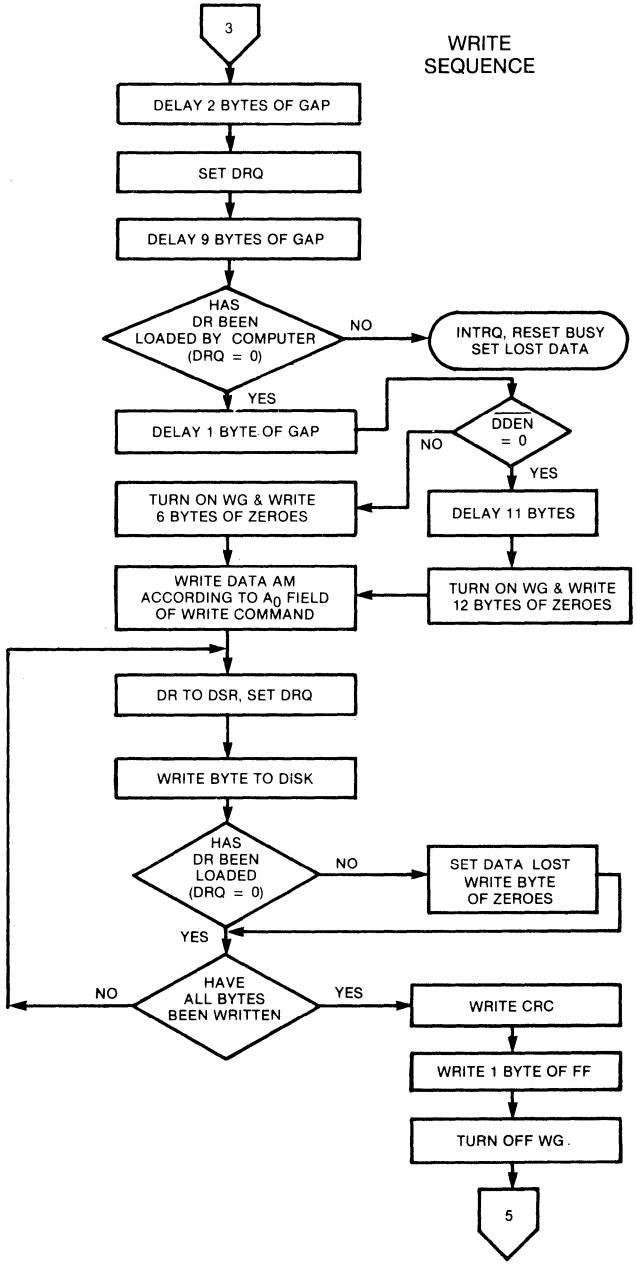


FIGURE 3. TYPE II COMMAND FLOWCHART (Cont.)



data address mark is then written on the disk as determined by the a0 field of the command as shown below:

a_0	DATA ADDRESS MARK (BIT 0)
1	Deleted Data Mark
0	Data Mark

The VL1772-02 then writes the data field and generates DRQs to the computer. If the DRQ is not serviced in time for continuous writing, the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in FMF. The WG output is then deactivated. INTRQ will set 24 µs (MFM) after the last CRC byte is written. For partial sector writing, the proper method is to write data and fill the balance with zeros.

TYPE III COMMANDS

Read Address - Upon receipt of the Read Address command, the Busy Status Bit is set. The next-encountered ID field is then read in from the disk, and six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDR	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the VL1772-02 checks for validity and the CRC Error Status Bit is set if there is a CRC error. The track address of the ID field is written into the Sector Register so that a comparison can be made by the user. At the end of the operation an interrupt is generated and the Busy status is reset.

Read Track - Upon receipt of the READ track command, the head is loaded and the Busy status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All gap, header, and data bytes are assembled and transferred to the Data Register and DRQs are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics that make it suitable for diagnostic purposes. They are: no CRC checking is performed; gap information is included in the data stream; and the address mark detector is on for the duration of the command. Because the AM detector is always on, write splices or noise may cause the chip to look for an AM.

The ID AM, ID Field, ID CRC Bytes, DAM, Data and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.

WRITE TRACK FORMATTING THE DISK

Data and gap information are provided at the computer interface. Formatting the disk is accomplished by positioning the R/$\overline{W}$ head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the Busy Status Bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded within three byte times, the operation is terminated, making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the VL1772-02 detects a data pattern of F5 through FE in the data register, this is interpreted as a data address mark with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern generates two CRC characters in FM or MFM. As a consequence, the patterns F5 through FE must not appear in the gaps, data fields, or ID fields. Also, CRCs must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

TABLE 2. DATA PATTERN DECODE

DATA PATTERN IN DR (HEX)	IN FM ($\overline{DDEN}$ = 1)	IN MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Present CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F9 thru FB	Write F8 thru FB, CLK = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with CLK = D7	Write FC in MFM
FD	Write FD with CLK = FF	Write FD in MFM
FE	Write FE, CLK = C7, Preset CRC	Write FE in MFM
FF	Write FF with CLK = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5.
**Missing clock transition between bits 3 and 4.

TYPE IV COMMANDS

The Forced Interrupt Command is generally used to terminate a multiple sector read or write command or to ensure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set) the command is terminated and the Busy Status Bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

I0 = Don't Care
I1 = Don't Care
I2 = Every Index Pulse
I3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I3-I0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line goes high signifying that the condition specified has occurred. If I3-I0 are all set to zero (HEX D0), no interrupt occurs but any command presently under execution is immediately terminated. When using the immediate interrupt condition (I3 = 1) an interrupt immediately is generated and the current command terminated. Reading the Status or writing to the Command Register does not automatically clear the interrupt. The HEX D0 is the only command that enables the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

Wait 16 µs (double density) or 32 µs (single density) before issuing a new command after issuing a forced interrupt. Loading a new command sooner than this nullifies the forced interrupt.

Force Interrupt Command stops any command at the end of an internal micro instruction and generates INTRQ when the specified condition is met. Force Interrupt waits until ALU operations in progress are complete (CRC calculations, compares, etc.).

Status Register - Upon receipt of any command, except the Force Interrupt command, the Busy Status Bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status Bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data Register is read the DRQ bit in the Status Register and the DRQ line are automatically reset. A write to the Data Register also causes both DRQ's to reset.

The Busy Bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a Busy status check is not recommended because a read of the Status Register to determine the condition of busy resets the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Because of internal synchronization cycles, certain time delays are observed when operating under program I/O as shown.

Operation	Next Operation	Delay Req'd. FM	Delay Req'd. MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	48µsec	24µsec
Write to Command Reg.	Read Status Bits 1-7	64µsec	32µsec
Write Register	Read Same Register	32µsec	16µsec

Shown below is the recommended single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00 (Sector Length)
1	F7 (2 CRC's written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
10	FF (or 00)
369**	FF (or 00)

**Continue writing until VL1772-02 interrupts out. Approximately 369 bytes.

256 BYTES/SECTOR

Shown below is the recommended dual-density format with 256 bytes/sector. In order to format a diskette, the user must issue the Write Track command and load the Data Register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
60	4E
12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01 (Sector Length)
1	F7 (2 CRC's written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (Data Address Mark)
24	4E
668**	4E

** Continue writing until VL1772-02 interrupts out. Approximately 668 bytes.

Non-Standard Formats - Variations in the recommended formats are possible to a limited extent, if the following requirements are met:

1) Sector size must be 128, 256, 512, or 1024 bytes.
2) Gap 2 cannot be varied from the recommended format.
3) Three bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the VL1772-02. Gap 1, 3, and 4 can be as short as two bytes for VL1772-02 operation; however, PLL lock-up time, motor speed variation, write-splice area, etc., add more bytes to each gap to achieve proper operation. For highest system reliability, use the recommended format.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00
*		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.
**Byte counts are minimum, except exactly 3 bytes of A1 must be written.

TABLE 3. STATUS REGISTER

BIT NAME	MEANING
S7 MOTOR ON	This bit reflects the status of the Motor On output.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/SPIN-UP	When set, this bit indicates that the Motor Spin-Up sequence has completed (5 revolutions) on Type I commands. Type 2 & 3 commands, this bit indicates record Type. 0 = Data Mark. 1 = Deleted Data Mark.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error data field. This bit is reset when updated.
S2 LOST DATA/ BYTE	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated. On Type I commands, this bit reflects the status of the TR00 signal.
S1 DATA REQUEST INDEX	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated. On Type 1 commands, this bit indicates the status of the IP signal.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

FIGURE 4. TYPE III COMMAND WRITE TRACK FLOWCHART

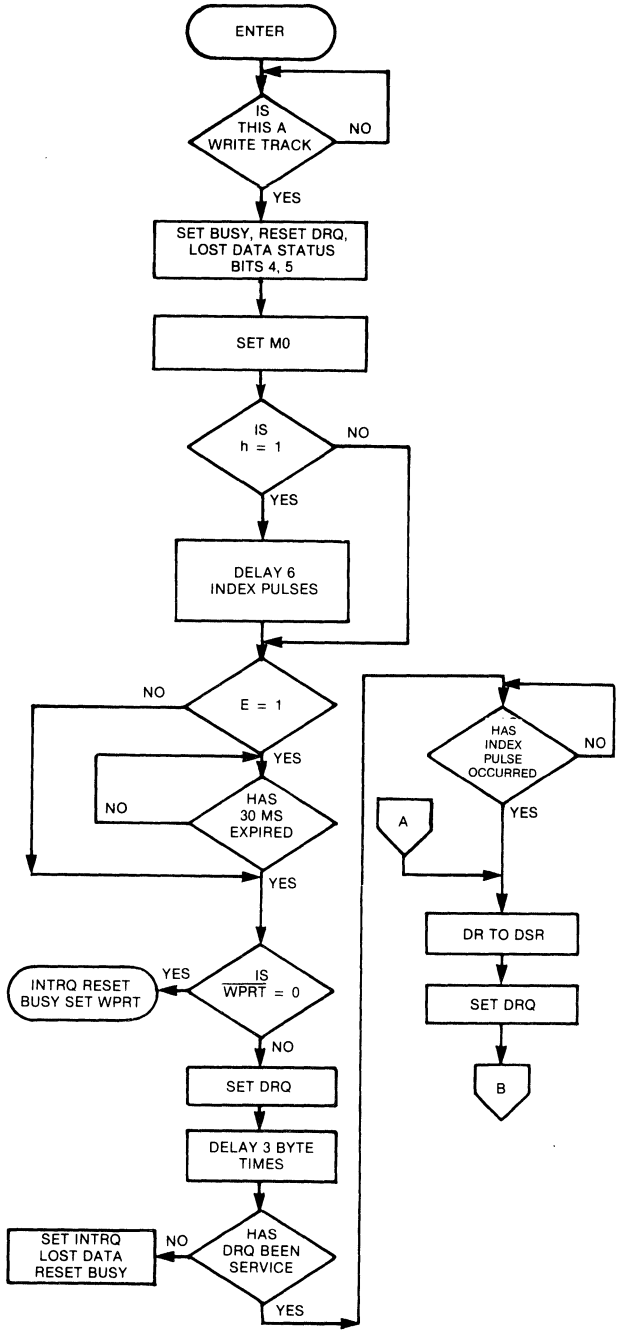


FIGURE 4. TYPE III COMMAND WRITE TRACK FLOWCHART (Cont.)

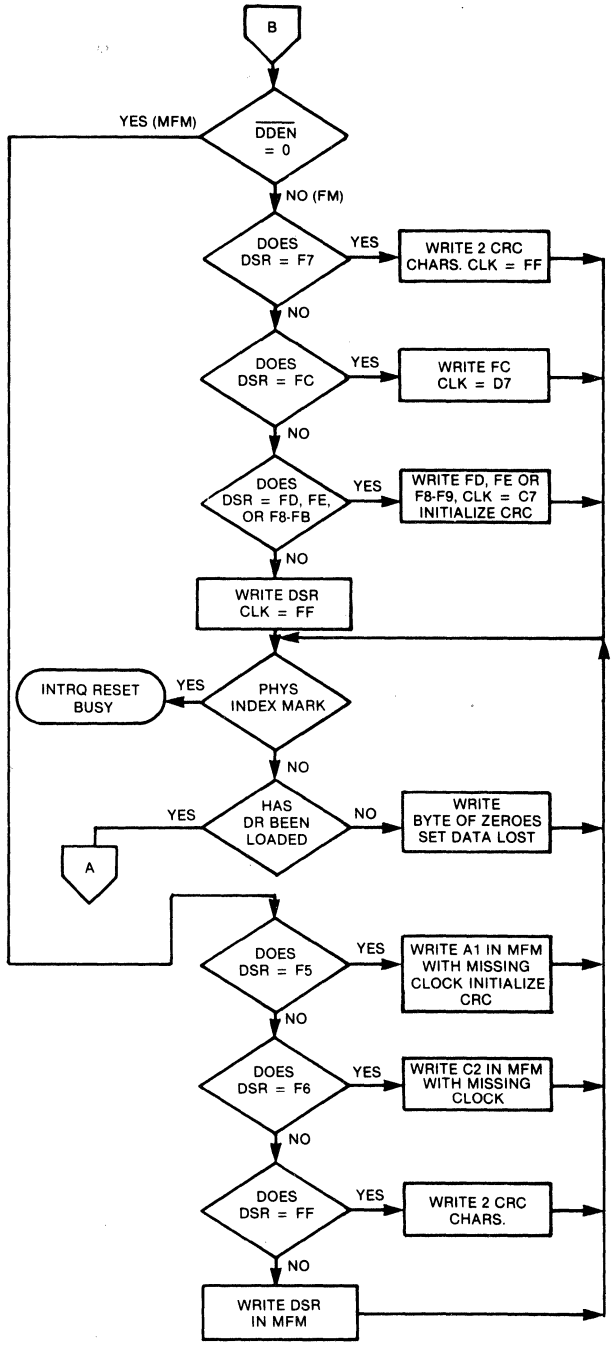


TABLE 4. READ DATA TIMING

CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$\overline{\text{Raw Read}}$ Pulse Width	.200		3	μsec	MFM
	.400		3		FM
$\overline{\text{Raw Read}}$ Cycle Time	3			μsec	

TABLE 5. READ ENABLE TIMING

READ ENABLE TIMING – $\overline{RE}$ such that: R/$\overline{W}$ = 1, CS = 0.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{RE}	$\overline{RE}$ Pulse Width of $\overline{CS}$	200			nsec	C_L = 50 pf
t_{DRR}	DRQ Reset from $\overline{RE}$		200	300	nsec	
t_{DV}	Data Valid from $\overline{RE}$		100	200	nsec	C_L = 50 pf
t_{DOH}	Data Hold from $\overline{RE}$	20		150	nsec	C_L = 50pf
	INTRQ Reset from $\overline{RE}$			8	μsec	

Note: Worst case service time for DRQ is 23.5 μsec for MFM and 47.5 μsec for FM.

FIGURE 5. READ ENABLE TIMING

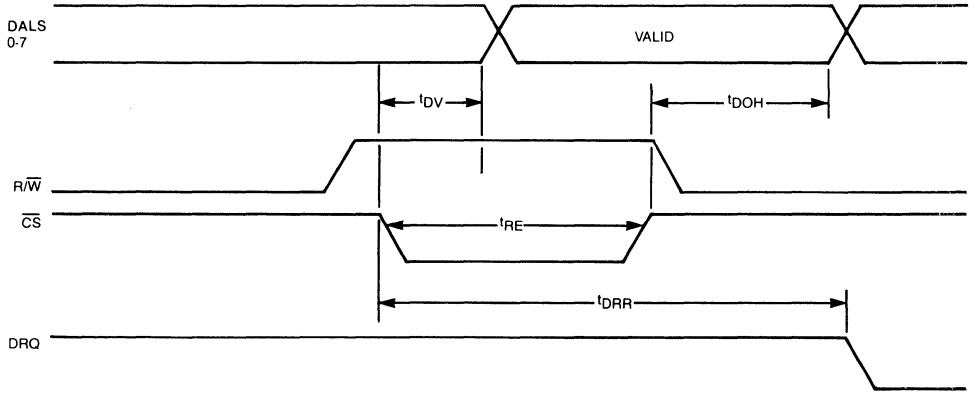


TABLE 6. WRITE ENABLE TIMING

WRITE ENABLE TIMING - $\overline{WE}$ such that: R/$\overline{W}$ = 0, $\overline{CS}$ = 0.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{AS}	Setup ADDR to $\overline{CS}$	50			nsec	
t_{SET}	Setup R/$\overline{W}$ to $\overline{CS}$	0			nsec	
t_{AH}	Hold ADDR from $\overline{CS}$	10			nsec	
t_{HLD}	Hold R/$\overline{W}$ from $\overline{CS}$	0			nsec	
t_{WE}	$\overline{WE}$ Pulse Width	200			nsec	
t_{DRW}	DRQ Reset from $\overline{WE}$		100	200	nsec	
t_{DS}	Data Setup to $\overline{WE}$	150			nsec	
t_{DH}	Data Hold from $\overline{WE}$	0			nsec	
	INTRQ Reset from $\overline{WE}$			8	μsec	

FIGURE 6. WRITE ENABLE TIMING

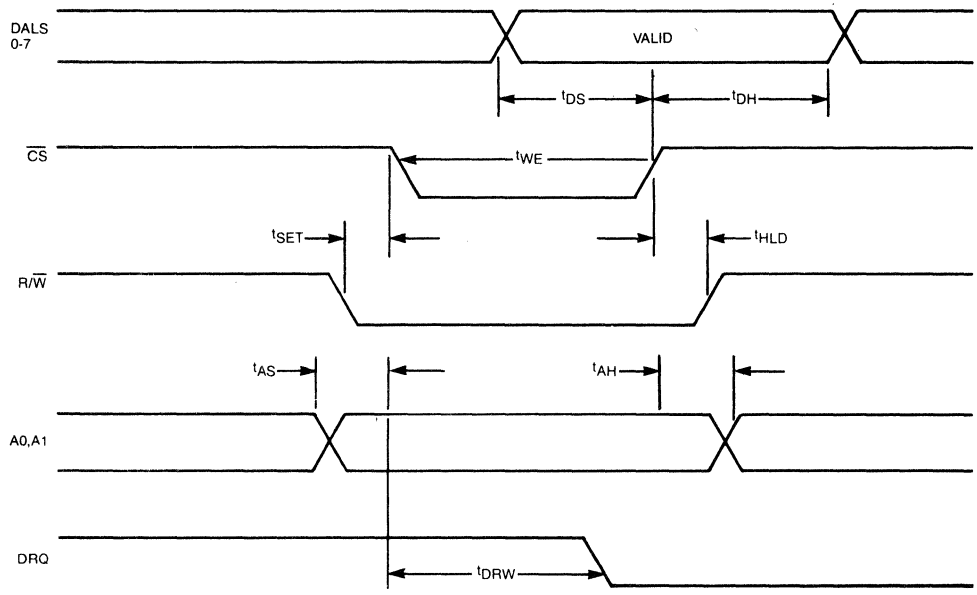


TABLE 7. WRITE DATA TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
	Write Gate to Write Data		4		µsec	FM
			2		µsec	MFM
	Write Data Cycle Time		4,6,8		µsec	
	Write Gate off from WD		4		µsec	FM
			2		µsec	MFM
t_{WP}	Write Data Pulse Width		820		nsec	Early MFM
			690		nsec	Nominal MFM
			570		nsec	Late MFM
			1.38		µsec	FM

FIGURE 7. WRITE DATA TIMING

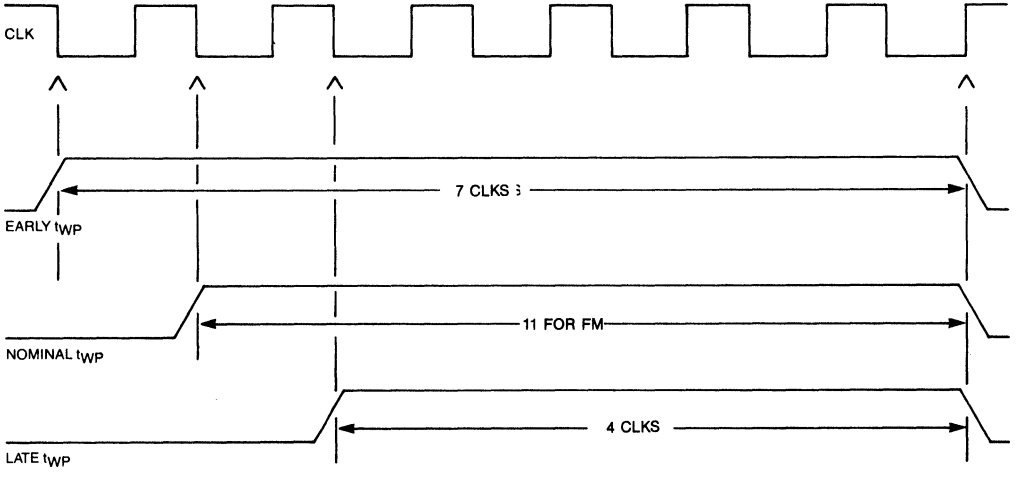


TABLE 8. MISCELLANOUS TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{CD1}	Clock Duty (low)	50	67		nsec	
t_{CD2}	CLock Duty (high)	50	67		nsec	
t_{STP}	Step Pulse Output		4		µsec	MFM
			8			FM
t_{DIR}	Dir Setup to Step		24		µsec	MFM
			48			FM
t_{MR}	Master Reset Pulse Width	50			µsec	
t_{IP}	Index Pulse Width	20			µsec	

FIGURE 8. MISCELLANOUS TIMING

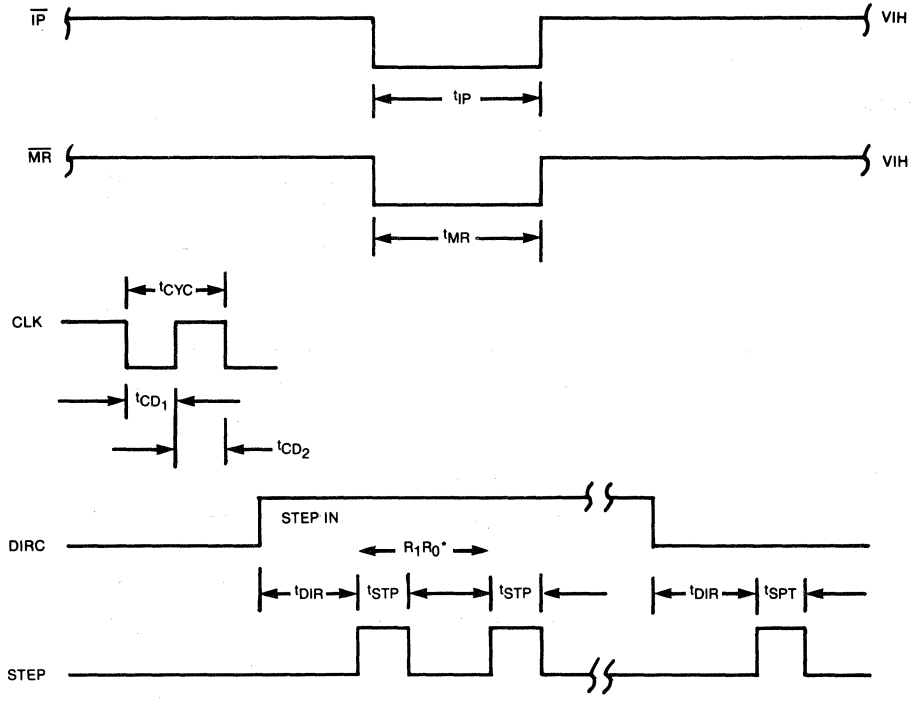
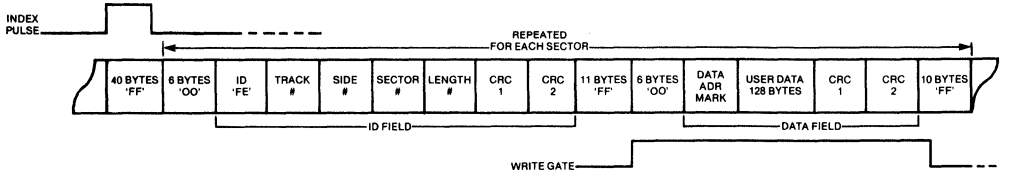
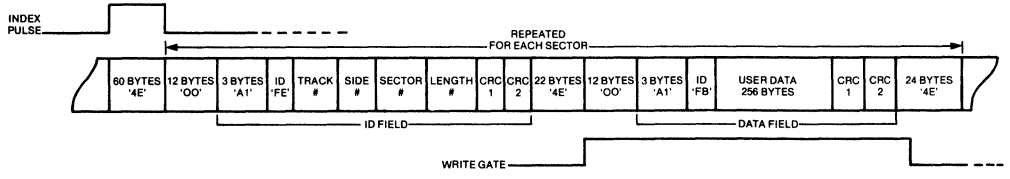


FIGURE 9. FORMATS



SINGLE DENSITY FORMAT



DOUBLE DENSITY FORMAT

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	-10°C to +80°C
Storage Temperature	-65°C to +140°C
Supply Voltage to Ground Potential	-0.5 V to +7.0 V
Applied Output Voltage	-0.5 V to +7.0 V
Applied Input Voltage	-0.5 V to +7.0 V
Power Dissipation	800mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5 v ± 5%

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VOH	Output High Voltage	2.4			V	IO = -100 µA
VOL	Output Low Voltage			0.4	V	IO = 1.6 mA
VIH	Input High voltage	2.0			V	
VIL	Input Low Voltage			0.8	V	
IIL	Input Leakage Current			10	µA	VIN = VCC
IOL	Output Leakage Current			10	µA	VOUT = VCC
RPU	Internal Pull-up	100		1700	µA	VIN = 0 V
ICC	Operating Supply Current		75	150	mA	
PD	Power Dissipation		780		mW	

APPLICATION INFORMATION

VL1772-02: AN IMPROVED VERSION OF THE 1770-00

The 177X family of flexible disk controllers has attracted a great deal of interest from system designers. Allowing compactness and superior performance, this family of advanced ICs has proven to be a success in the marketplace. The original 1770-00 won much approval with its 28-pin package. Its digital data separator allowed consistent operation over temperature, but more was required. The error rate of this data recovery circuit was too high, and a reliable data separator with lower error rates was seen as an important need for computer systems of all types.

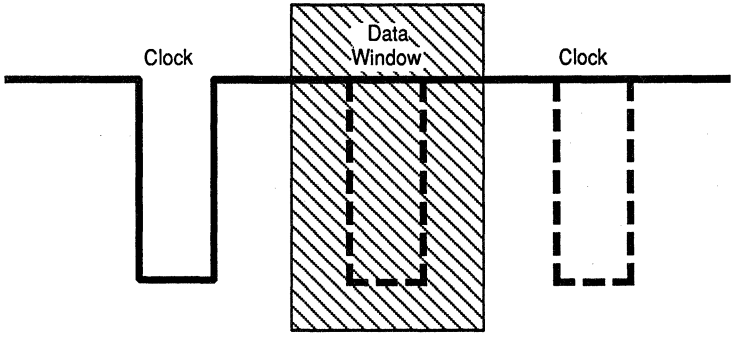
In addition, a small change of step rate selections could ensure faster throughput, while maintaining compatibility with existing designs.

Thus began the design of a new concept in flexible disk controllers. An important need was to maintain compatibility with existing designs using the 1770-00, while extending the capabilities of the 177X family to include higher-performance drives. These criteria have been satisfied with the VL1772-02.

IMPROVING THE DATA SEPARATOR

The improvement of the data separator, or data recovery circuit, as it is called, is an important enhancement to the reliability of the VL1772-02. The operation of this part of the circuit, although critical to system reliability, is simple to understand. Figure 10 shows a train of read data pulses coming from a floppy drive. The clock and data pulses are both in this signal, combined in a simple encoding format. In each bit cell, the data separator chooses a time period within which pulses are recognized as data pulses. The better the resolution for defining this window for the data pulses, the greater the jitter in the signal can be before ones and zeros are incorrectly recognized. This incorrect recognition, and the resultant soft errors, are the basic limiting factor in floppy drive error rates. The VL1772-02, with a wider data window, has a lower chance of incorrect recognition, resulting in lower error rates. This effect will be particularly evident as the user's media degrades with use and jitter increases. This increased reliability of the VL1772-02 can result in fewer returns and greater user satisfaction.

FIGURE 10. WINDOWING READ DATA



STEP RATES

With a different selection of step rates than the 1770-00 (see table 9), the VL1772-02 allows the use of drives with minimum settle times up to 12 ms. At the same time, performance is enhanced to take advantage of floppy drives that require only 2 or 3 ms of delay. If a design is currently using head settle times of 6 or 12 ms (as most are), no modifications are required to use the VL1772-02 in the 1770-00 socket. If the current choice of r1 and r0 calls for 20 or 30 ms of delay, use of the VL1772-02 requires:

— the selection of drives that have head settle time under 12 ms, and modified software to allow correct r1, r0 choice, or

— implementation of head settle time in hardware, with an external interrupt.

Fortunately, almost all modern flexible disk drives have head settle times well under 12 ms, and current 1770 applications have taken this into account, using 6 or 12 ms as the head settle time. Where this change is required, it will mean less waiting for the drives to finish each seek. This will certainly produce higher user satisfaction with the system, as well as appreciably higher performance against most benchmarks.

TABLE 9. STEP RATE SELECTION: 1770-00 AND VL1772-02

Step Rate Select Bits		Step Rate (ms)	
r1	r0	1770-00	VL1772-02
0	0	6	6
0	1	12	12
1	0	20	2
1	1	30	3

VL2793 • VL2797

FLOPPY DISK FORMATTER/CONTROLLER FAMILY

FEATURES

- ON-CHIP PLL DATA SEPARATOR
- ON-CHIP WRITE PRECOMPENSATION LOGIC
- SINGLE +5V SUPPLY
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 (FM)
  - IBM 34 (MFM)
- AUTOMATIC SEEK WITH VERIFY
- MULTIPLE SECTOR READ/WRITE
- TTL COMPATIBLE
- PROGRAMMABLE CONTROL
  - SELECTABLE TRACK-TO-TRACK ACCESS
  - HEAD LOAD TIMING
- SOFTWARE COMPATIBLE WITH THE FD179X SERIES
- SOFT SECTOR FORMAT COMPATIBILITY

DESCRIPTION

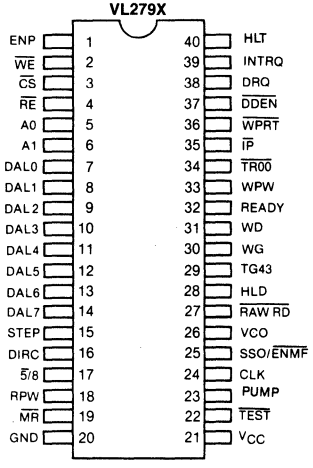
The VL279X are N-Channel Silicon Gate MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The VL279X, which can be considered the end result of both the FD1771 and FD179X designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The VL279X contains all the features of its predecessor the FD179X plus a high performance Phase-Lock-Loop Data Separator as well as Write Precompensation Logic. In Double Density mode, Write Precompensation is automatically engaged to a value programmed via an external potentiometer. In order to maintain compatibility, the FD1771, FD179X and VL279X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The VL279X is set up to operate on a multiplexed bus with other bus-oriented devices.

The VL279X is TTL compatible on all inputs and outputs. The outputs will drive one TTL load or three LS loads. The 2793 is identical to the 2791 except the DAL lines are TRUE for systems that utilize true data busses.

The 2797 has a side select output for controlling double-sided drives.

PIN DIAGRAM



ORDER INFORMATION

Part Number	Format	Package
VL2793-PC	Single-Sided	Plastic DIP
VL2793-CC		Ceramic DIP
VL2797-PC	Double-Sided	Plastic DIP
VL2797-CC		Ceramic DIP

Note:
Operating temperature range: 0°C to +70°C.

PIN DESCRIPTION

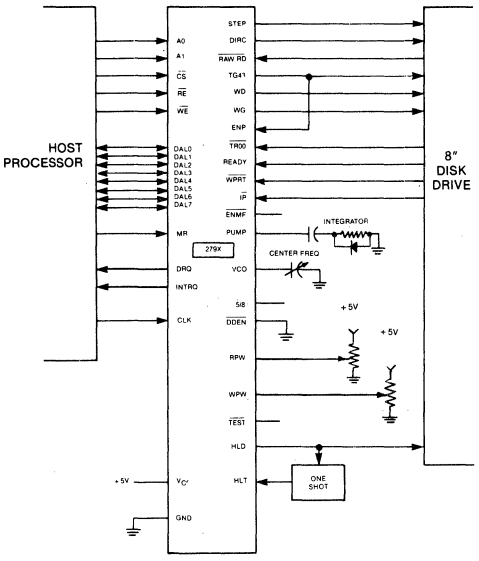
PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	ENABLE PRECOMP	ENP	A Logic high on this input enables write precompensation to be performed on double density Write Data output only.
19	MASTER RESET	$\overline{MR}$	A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during MR ACTIVE. When $\overline{MR}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V ±5%
COMPUTER INTERFACE:			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
5, 6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control:
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit bi-directional bus used for transfer of commands, status, and data. These lines are inverted (active low) on VL279X.
24	CLOCK	CLK	This input requires a free-running 50% duty cycle square wave clock for internal timing reference, 2 MHz ± 1% for 8″ drives, 1 MHz ± 1% for minifloppies.
38	DATA REQUEST	DRQ	This output indicates that the Data Register contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR.
39	INTERRUPT REQUEST	INTRQ	This output is set at the completion of any command and is reset when the Status register is read or the Command register is written to.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	5¼,″ 8″ SELECT	$\overline{5}/8$	This input selects the internal VCO frequency for use with 5¼″ drives or 8″ drives.
18	READ PULSE WIDTH	RPW	An external potentiometer tied to this input controls the phase comparator within the data separator.
22	TEST	$\overline{TEST}$	A logic low on this input allows adjustment of external resistors by enabling internal signals to appear on selected pins.

$\overline{CS}$	A1	A0	$\overline{RE}$	$\overline{WE}$
0	0	0	Status Reg	Command Reg
0	0	1	Track Reg	Track Reg
0	1	0	Sector Reg	Sector Reg
0	1	1	Data Reg	Data Reg

PIN DESCRIPTION (Continued)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
23	PUMP	PUMP	High-Impedance output signal which is forced high or low to increase/decrease the VCO frequency.
25	ENABLE MINI-FLOPPY (2793)	$\overline{\text{ENMF}}$	A logic low on this input enables an internal ÷2 of the Master Clock. This allows both 5¼" and 8" drive operation with a single 2 MHz clock. For a 1 MHz clock on Pin 24, this line must be left open or tied to a Logic 1.
25	SIDE SELECT OUTPUT (2797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the Sector I.D. Field. If they do not compare Status Bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	VOLTAGE-CONTROLLED OSCILLATOR	VCO	An external capacitor tied to this pin adjusts the VCO center frequency.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.
31	WRITE DATA	WD	MFM or FM output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	WRITE PRECOMP WIDTH	WPW	An external potentiometer tied to this input controls the amount of delay in Write precompensation mode.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the VL279X that the Read/Write head is positioned over Track 00.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	This input informs the VL279X when the index hole is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	$\overline{\text{DOUBLE DENSITY}}$	$\overline{\text{DDEN}}$	This input pin selects either single or double density operation. When $\overline{\text{DDEN}}$ = 0, double density is selected. When $\overline{\text{DDEN}}$ = 1, single density is selected.
40	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a 1 shot triggered by HLD.

Figure 1.



APPLICATIONS

8" FLOPPY AND 5¼" MINI FLOPPY CONTROLLER
SINGLE OR DOUBLE DENSITY
CONTROLLER/FORMATTER

The VL279X Family are MOS/LSI devices which perform the functions of a Floppy Disk Controller/Formatter. Software compatible with its predecessor, the FD179X, the device also contains a high performance Phase-Lock-Loop Data Separator as well as Write Precompensation Logic.

When operating in Double Density mode, Write Precompensation may be enabled, its value predetermined by an external potentiometer. An on-chip VCO and phase comparator allows adjustable frequency range for 5¼" or 8" Floppy Disk interfacing.

The VL279X is fabricated in NMOS silicon gate technology and available in a 40 pin dual-in-line package.

FEATURES	2793	2797
Single Density (FM)	X	X
Double Density (MFM)	X	X
True Data Bus	X	X
Inverted Data Bus		
Side Select Out		X
Internal CLK Divide	X	

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register — This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register — This 8-bit register is used as a holding register during Disk Read and Write operations in Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

Sector Register (SR) — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) — This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

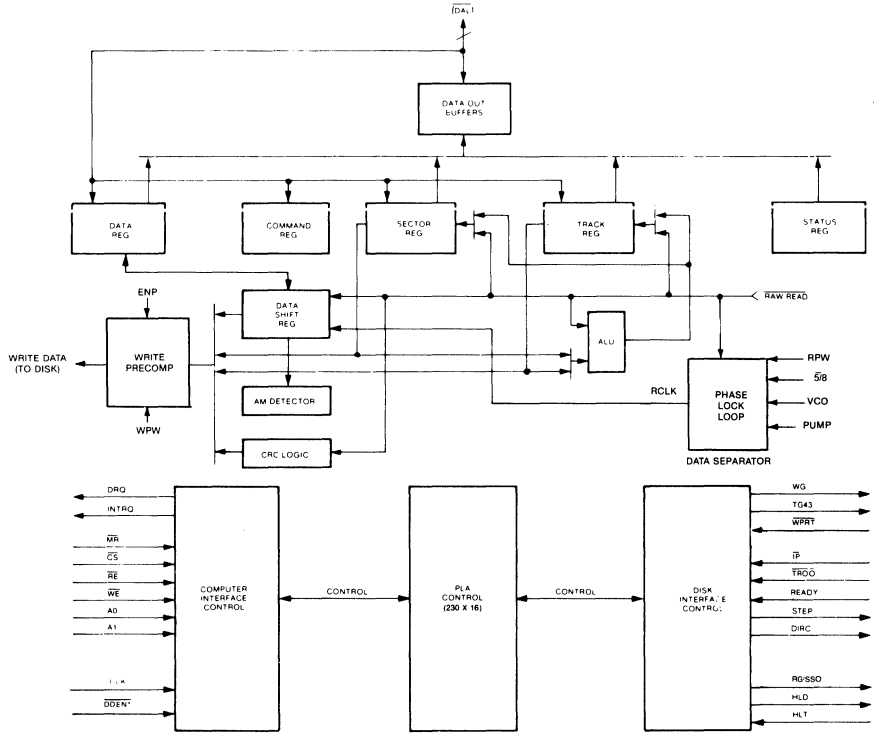
Arithmetic/Logic Unit (ALU) — The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control — All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

AM Detector — The address mark detector detects ID, data and index address marks during read and write operations.

Write Precompensation — enables write precompensation to be performed on the Write Data output.

VL279X BLOCK DIAGRAM



Data Separator — a high performance Phase-Lock-Loop Data Separator with on-chip VCO and phase comparator allows adjustable frequency range for 5¼" or 8" Floppy Disk interfacing.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the VL279X. The DAL are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1	A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the VL279X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The 279X has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, Single Density (FM) is selected. When $\overline{DDEN}$ = 0, Double Density (MFM) is selected. In either case, the CLK input (Pin 24) is set at 2 MHz for 8" drives or 1 MHz for 5¼" drives.

On the 2791/2793, the $\overline{ENMF}$ input (Pin 25) can be used for controlling both 5¼" and 8" drives with a single 2 MHz clock. When $\overline{ENMF}$ = 0, an internal ÷ 2 of the CLK is performed. When $\overline{ENMF}$ = 1, no divide takes place. This allows the use of a 2 MHz clock for both 5¼" and 8" configurations.

The internal VCO frequency must also be set to the proper value. The $\overline{5}$/8 input (Pin 17) is used to select data separator operation by internally dividing the Read Clock. When $\overline{5}$/8 = 0, 5¼" data separation is selected; when 5/8 = 1, 8" drive data separation is selected.

CLOCK (24)	$\overline{ENMF}$ (25)	$\overline{5}$/8 (17)	DRIVE
2 MHz	1	1	8"
2 MHz	0	0	5¼"
1 MHz	1	0	5¼"

FUNCTIONAL DESCRIPTION

The VL279X is software compatible with the FD179X series of Floppy Disk Controllers. Commands, status, and data transfers are performed in the same way. Software generated for the 179X can be transferred to a 279X system without modification.

In addition to the 179X, the 279X contains an internal Data Separator and Write precompensation circuit. The $\overline{TEST}$ (Pin 22) line is used to adjust both data separator and precompensation. When $\overline{TEST}$ = 0, the WD (Pin 31) line is internally connected to the output of the write precomp one-shot. Adjustment of the WPW (Pin 33) line can then be accomplished. A second one-shot tracks the precomp setting at approximately 3:1 to insure adequate Write Data pulse widths to meet drive specifications.

Similarly, Data separation is also adjusted with $\overline{TEST}$ = 0. The TG43 (Pin 29) line is internally connected to the output of the read data one-shot, which is adjusted via the RPW (Pin 18) line. The DIRC (Pin 16) line contains the Read Clock output (.5 MHz for 8" drives). The VCO Trimming capacitor (Pin 26) is adjusted for center frequency.

Internal timing signals are used to generate pulses during the adjustment mode so that these adjustments can be made while the device is in-circuit. The $\overline{TEST}$ line also contains a pull-up resistor, so adjustments can be performed simply by grounding the $\overline{TEST}$ pin, overriding the pull-up. The $\overline{TEST}$ pin cannot be used to disable stepping rates during operation as its function is quite different from the 179X.

Other pins on the device also include pull-up resistors and may be left open to satisfy a Logic 1 condition. These are: ENP, $\overline{5}$/8, $\overline{ENMF}$, $\overline{WPRT}$, $\overline{DDEN}$, HLT, TEST, and $\overline{MR}$.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logical "1." For MFM formats, $\overline{DDEN}$ should be placed to a logical "0." Sector lengths are determined at format time by the fourth byte in the "ID" field.

Sector Length Table*	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

*2793/97 may vary — see command summary.

The VL279X recognizes tracks and sectors numbered 00-FFX. However, due to programming restrictions, only tracks and sectors 00 thru F4 can be formatted.

GENERAL DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the 279X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{Write\ Protect}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set.

For write operations, the 279X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of pulses set to a width approximately three times greater than the precomp adjustment. Write Data provides the unique address marks in both formats.

READY

Whenever a Read or Write command (Type II or III) is received the 279X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated. TG43 may be tied to ENP to enable write precompensation on tracks 44-76.

COMMAND DESCRIPTION

The VL279X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

TABLE 1. COMMAND SUMMARY

A. Commands for Model 2793

B. Commands for Model 2797

Type	Command	Bits 7	6	5	4	3	2	1	0	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0	0	1	1	T	h	V	r_1	r_0
II	Read Sector	1	0	0	m	S	E	C	0	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	S	E	C	a_0	1	0	1	m	L	E	U	a_0
III	Read Address	1	1	0	0	0	E	0	0	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	0	0	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	0	0	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0	1	1	0	1	I_3	I_2	I_1	I_0

TABLE 2. FLAG SUMMARY

Command Type	Bit No(s)		Description
I	0, 1	r_1 r_0 = Stepping Motor Rate See Table 3 for Rate Summary	
I	2	V = Track Number Verify Flag	V = 0, No verify V = 1, Verify on destination track
I	3	h = Head Load Flag	h = 0, Unload head at beginning h = 1, Load head at beginning
I	4	T = Track Update Flag	T = 0, No update T = 1, Update track register
II & III	0	a_0 = Data Address Mark	a_0 = 0, FB (DAM) a_0 = 1, F8 (deleted DAM)
II	1	C = Side Compare Flag	C = 0, Disable side compare C = 1, Enable side compare
II & III	1	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1
II & III	2	E = 15 MS Delay	E = 0, No. 15 MS delay E = 1, 15 MS delay (30 MS for 1 MHz)
II	3	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1
II	3	L = Sector Length Flag	LSB's Sector Length in ID Field 00: L = 0: 256; L = 1: 128 01: L = 0: 512; L = 1: 256 10: L = 0: 1024; L = 1: 512 11: L = 0: 128; L = 1: 1024
II	4	m = Multiple Record Flag	m = 0, Single record m = 1, Multiple records
IV	0-3	I_x = Interrupt Condition Flags I_0 = 1 Not Ready To Ready Transition I_1 = 1 Ready To Not Ready Transition I_2 = 1 Index Pulse I_3 = 1 Immediate Interrupt, Requires A Reset* I_3-I_0 = 0 Terminate With No Interrupt (INTRQ)	

*NOTE: See Type IV Command Description for further information.

Write Precompensation

When operating in Double Density mode ($\overline{DDEN}$ = 0), the 279X has the capability of providing a user-defined precompensation value for Write Data. An external potentiometer (10K) tied to the WPW signal (Pin 33) allows a setting of 100 to 300 ns from nominal.

Setting the Write precomp value is accomplished by forcing the $\overline{TEST}$ line (Pin 22) to a Logic 0. A stream of pulses can then be seen on the Write Data (Pin 31) line. Adjust the WPW Potentiometer for the desired pulse width. This adjustment may be performed in-circuit since Write Gate (Pin 30) is inactive while $\overline{TEST}$ = 0.

Data Separation

The 279X can operate with either an external data separator or its own internal recovery circuits. The condition of the $\overline{TEST}$ line (Pin 22) in conjunction with $\overline{MR}$ (Pin 19) will select internal or external mode.

To program the 279X for external VCO, a $\overline{MR}$ pulse must be applied while $\overline{TEST}$ = 0. A clock equivalent to eight times the data rate (e.g., 4.0 MHz for 8" Double Density) is applied to the VCO input (Pin 26). The feedback reference voltage is available on the Pump output (Pin 23) for external integration to control the VCO. $\overline{TEST}$ is returned to a Logic 1 for normal operation. Note: To maintain this mode, $\overline{TEST}$ must be held low whenever $\overline{MR}$ is applied.

For internal VCO operation, the $\overline{TEST}$ line must be high during the $\overline{MR}$ pulse, then set to a Logic 0 for the adjustment procedure.

A 50K Potentiometer tied to the RPW input (Pin 18) is used to set the internal Read Data pulse for proper phasing. With a scope on Pin 29 (TG43), adjust the RPW pulse for 1/8 of the data rate (250 ns for 8" Double Density). An external variable capacitor of 5-60 pf is tied to the VCO input (Pin 26) for adjusting center frequency. With a frequency counter on Pin 16 (DIRC) adjust the trimmer cap to yield the appropriate Data Rate (500 KHz for 8" Double Density). The $\overline{DDEN}$ line must be low while the 5/8 line is held high or the adjustment times above will be doubled.

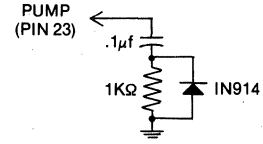
After adjustments have been made, the $\overline{TEST}$ pin is returned to a Logic 1 and the device is ready for operation. Adjustments may be made in-circuit since the DIRC and TG43 lines may toggle without affecting the drive.

The PUMP output (Pin 23) consists of positive and negative pulses, which their duration is equivalent to the phase difference of incoming Data vs. VCO frequency. This signal is internally connected to the VCO input, but a Filter is needed to connect these pulses to a slow moving DC voltage.

The internal phase-detector is unsymmetrical for a random distribution of data pulses by a factor of two, in favor of a PUMP UP condition. Therefore, it is desirable to have a PUMP DOWN twice as responsive to prevent run-away during a lock attempt.

A first order lag-lead filter can be used at the PUMP output (Pin 23). This filter controls the instantaneous response of the VCO to bit-shifted data (jitter) as well as the response to normal frequency shift, i.e., the lock-up time. A balance must be accomplished between the two conditions to inhibit over-responsiveness to jitter and to prevent an extremely wide lock-up response, leading to PUMP run-away. The filter affects these two reactions in mutually opposite directions.

The following Filter Circuit is recommended for 8" FM/MFM:



Since 5¼" Drives operate at exactly one-half the data rate (250 Kb/sec) the above capacitor should be doubled to .2 or .22μf.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-in, and Step-Out commands. Each of the Type I Commands contains a rate field (r_0 r_1), which determines the stepping motor rate as defined in Table 3.

A 2μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid before the first stepping pulse is generated.

The rates (shown in Table 3) can be applied to a Step-Direction Motor through the device interface.

TABLE 3. STEPPING RATES

CLK R1	CLK R0	2 MHz $\overline{TEST}$ = 1	1 MHz $\overline{TEST}$ = 1
0	0	3 ms	6 ms
0	1	6 ms	12 ms
1	0	10 ms	20 ms
1	1	15 ms	30 ms

After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID

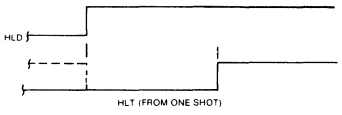
Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation.

The VL279X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the 279X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load timing (HLT) is an input to the 279X which is used for the head engage time. When HLT = 1, the 279X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the 279X.

HEAD LOAD TIMING



When both HLD and HLT are true, the 279X will then read from or write to the media. The "and" of HLD and HLT appears as status Bit 5 in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the 279X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the 279X then waits for HLT to occur.

For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

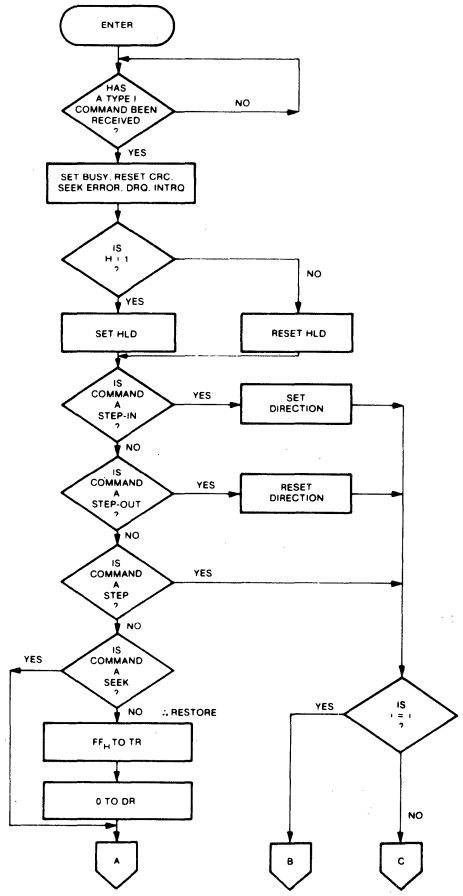
RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses at a rate specified by the r1r0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the 279X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when $\overline{MR}$ goes from an active to an inactive state.

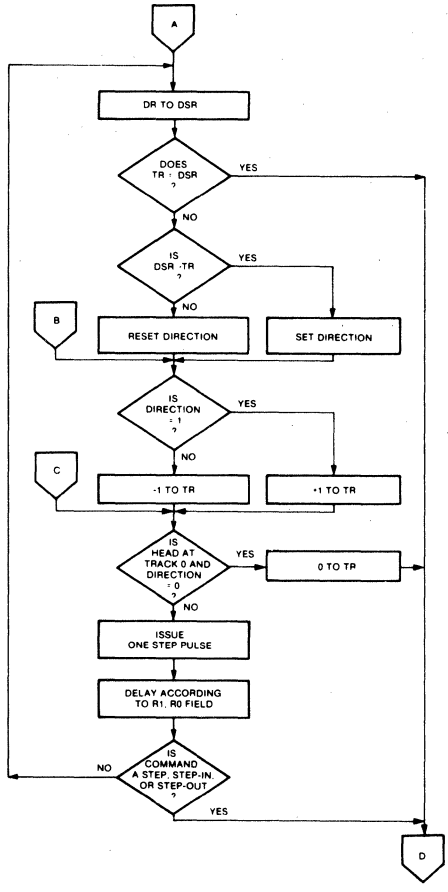
SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The VL279X will update the Track register and issue stepping pulses in the appropriate direction until the

TYPE I COMMAND FLOW

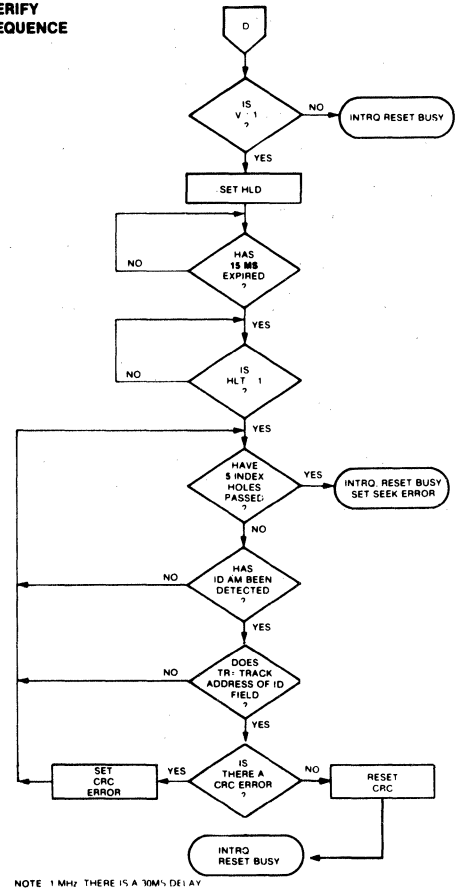


TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

VERIFY SEQUENCE



contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

STEP

Upon receipt of this command, the 279X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the T flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the 279X issues one stepping pulse in the direction towards track 76. If the T flag is on, the Track Register is incremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the 279X issues one stepping pulse in the direction towards track 0. If the T flag is on, the Track Register is decremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

EXCEPTIONS

On the 2797 device, the SSO output is not affected during Type I commands, and an internal side compare does not take place when the (V) Verify Flag is on.

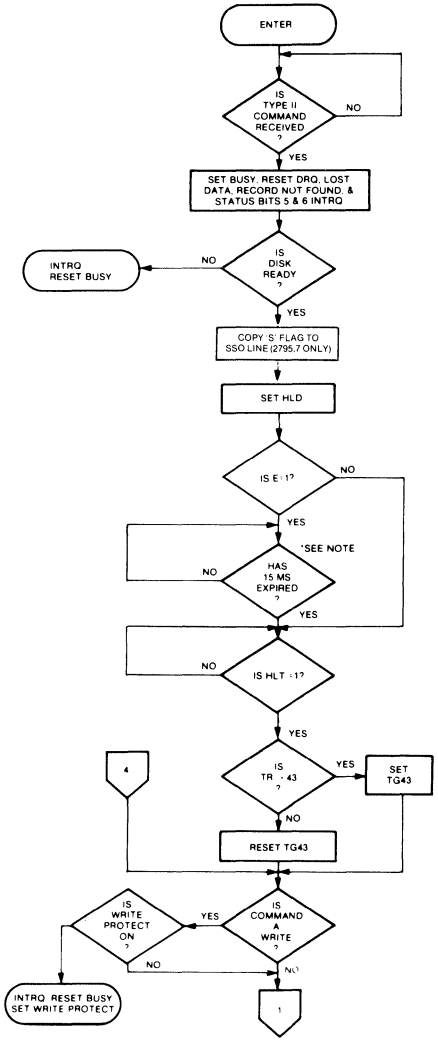
TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the

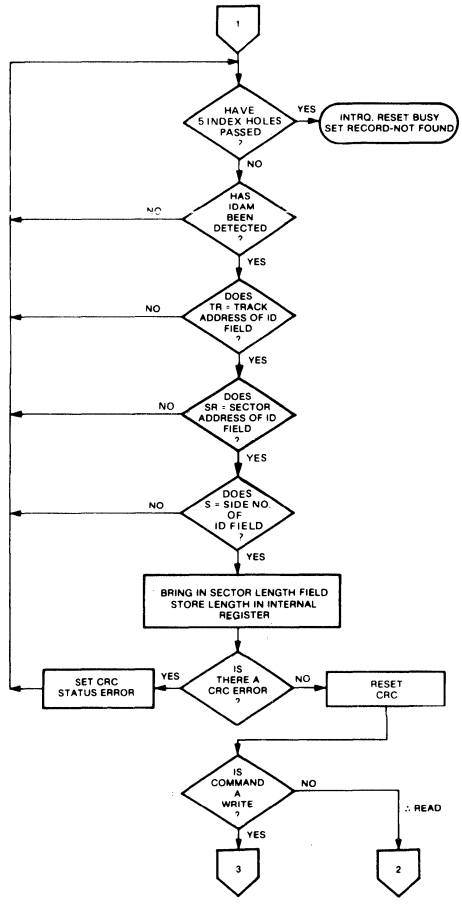
Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay.

When an ID field is located on the disk, the 279X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from

TYPE II COMMAND



TYPE II COMMAND

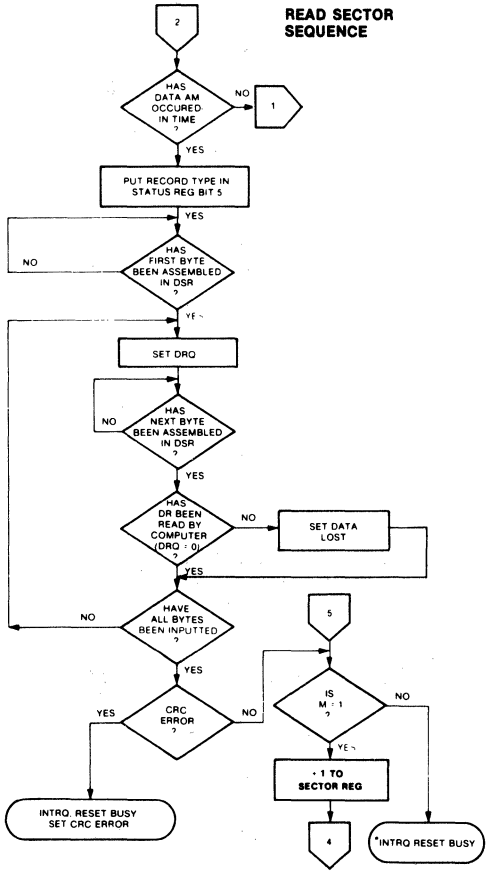


depending upon the command. The 279X must find an ID field with a Track number, Sector number, side number, and CRC within 5 revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 4) and the command is terminated with an interrupt.

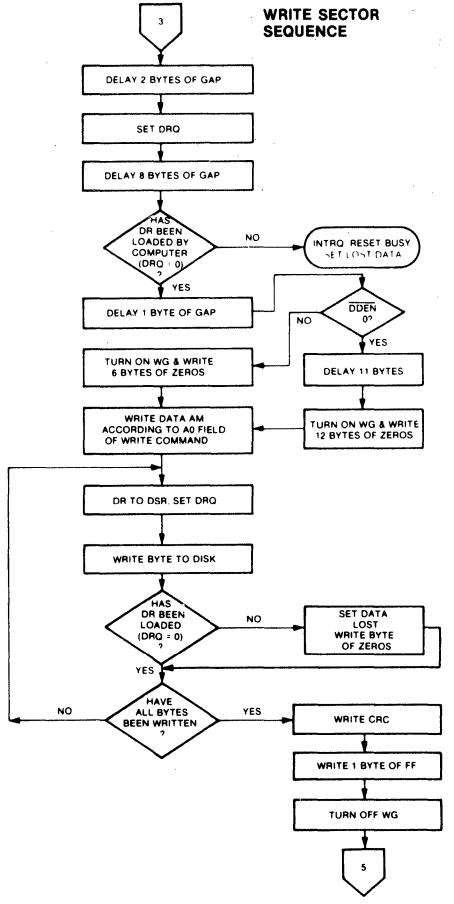
Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The 279X will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the 279X is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds

TYPE II COMMAND



TYPE II COMMAND



the number available. The 279X will search for 5 disk revolutions, interrupt out, reset busy, and set the record not found status bit.

The Type II commands for the 2793 also contain side select compare flags. When C = 0 (Bit 1) no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag (Bit 3). If the S flag compares with the side number recorded in the ID field, the 279X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The Type II and III commands for the 2797 contain a side select flag (Bit 1). When U = 0, SSO is updated to 0. Similarly, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not compare within 5 revolutions the interrupt line is made active and the RNF status bit is set.

The 2797 READ SECTOR and WRITE SECTOR commands include a 'L' flag. The 'L' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatibility, the 'L' flag should be set to a one.

READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the ID field search is repeated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred

that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple sector command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The 279X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The 279X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one bye of FE in FM or in MFM. The WG output is then deactivated. For a 2 MHz clock the INTRQ will set 8 to 12 μsec after the last CRC byte is written. For partial sector writing, the proper method is to write the data and fill the balance with zeroes. By letting the chip fill the zeroes, errors may be masked by the lost data status and improper CRC Bytes.

TYPES III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

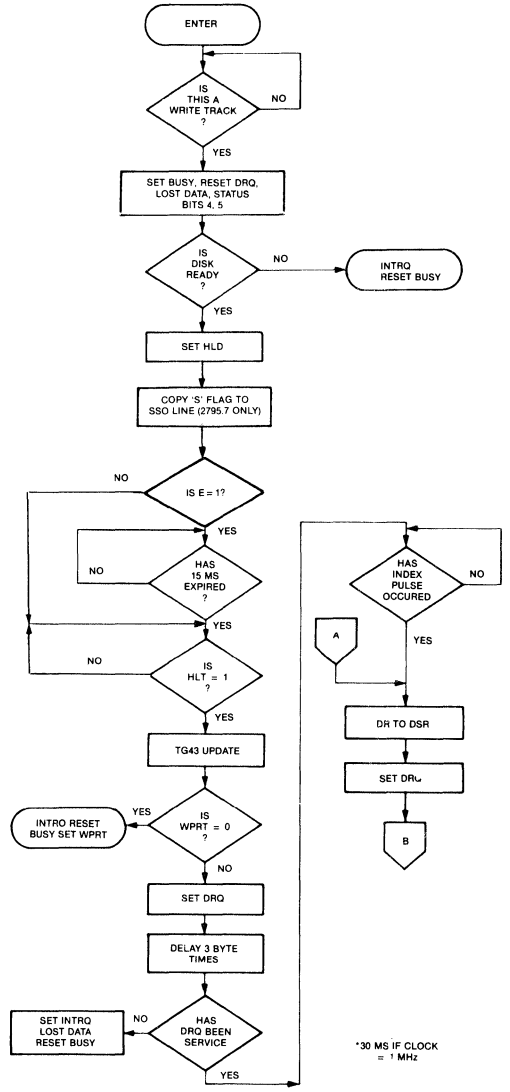
TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the 279X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the host. At the end of the operation an interrupt is generated and the Busy Status is reset.

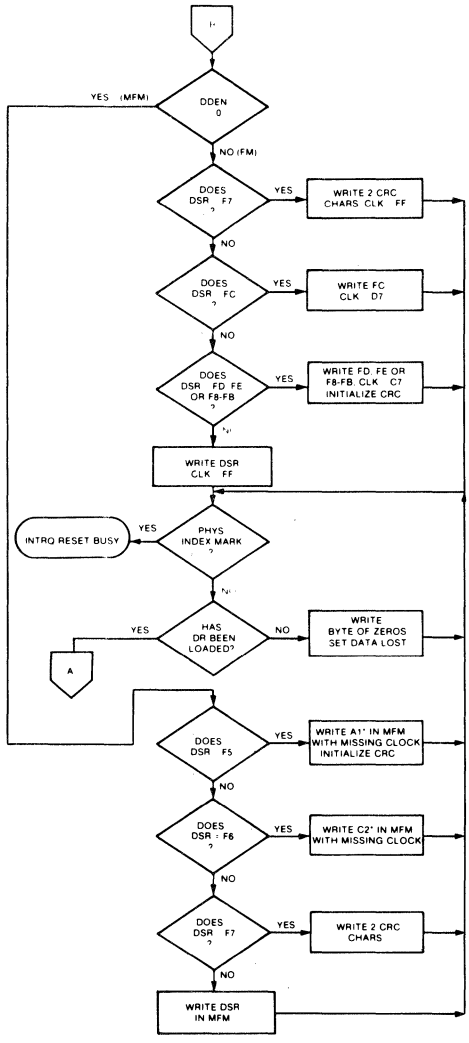
READ TRACK

Upon receipt of the READ track command, the head is loaded, and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The ac-

TYPE III COMMAND WRITE TRACK



TYPE III COMMAND WRITE TRACK



cumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule with the Lost Data status flag being set.

The ID A.M., ID field, ID CRC bytes, DAM, Data and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.

WRITE TRACK FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the 279X detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	VL279X INTERPRETATION IN FM (DDEN = 1)	VL279X INTERPRETATION IN MFM (DDEN = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

* Missing clock transition between bits 4 and 5

** Missing clock transition between bits 3 and 4

or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

TYPE IV COMMANDS

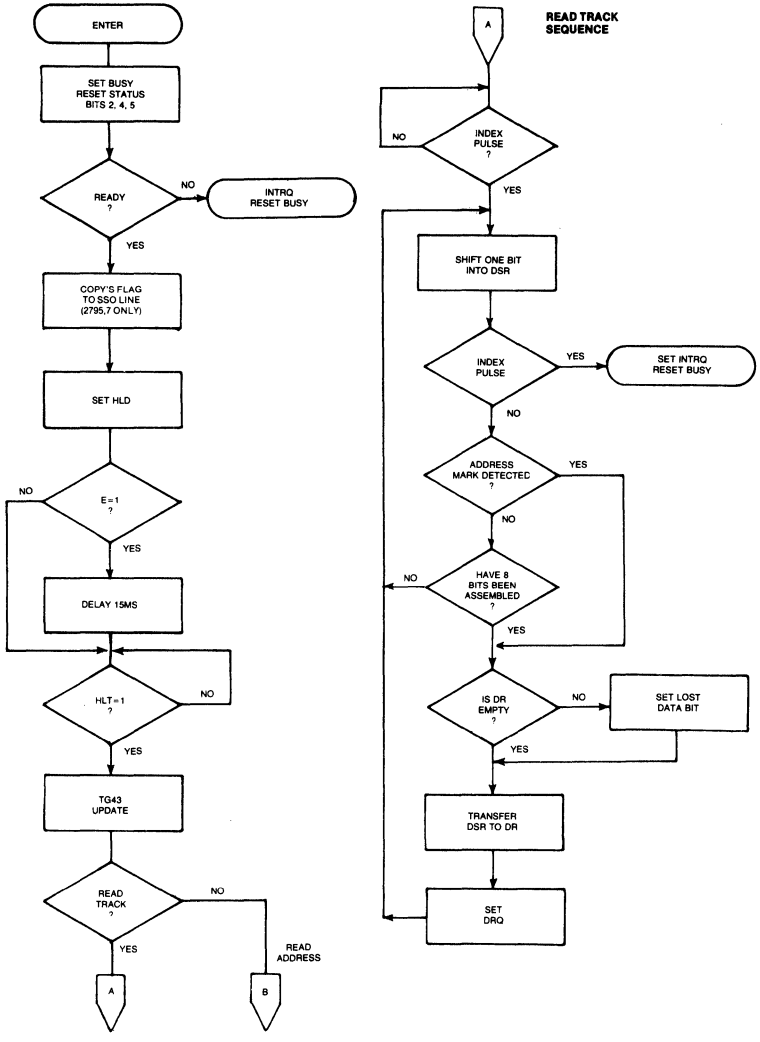
The Forced Interrupt command is generally used to terminate a multiple sector read or write command or to insure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set) the command will be terminated and the busy status bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

I_0 = Not-Ready to Ready Transition
I_1 = Ready to Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I_3 - I_0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I_3 - I_0 are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate

TYPE III COMMAND Read Track/Address



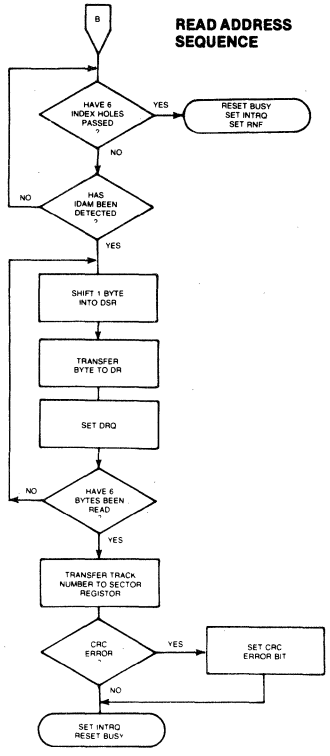
interrupt condition I_3 = 1), an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

Wait 8 micro sec (double density) or 16 micro sec (single density) before issuing a new command after issuing a forced interrupt (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.)

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I_1 = 1) and the Every Index Pulse (I_2 = 1) are both set, the resultant command would be HEX "DA." The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.

TYPE III COMMAND Read Track/Address



STATUS REGISTER

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 4.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are: (times double when clock = 1 MHz)

Operation	Next Operation	Delay Req'd. FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	12μs	6μs
Write to Command Reg.	Read Status Bits 1-7	28μs	14μs
Write Any Register	Read From Diff. Register	0	0

IBM 3740 FORMAT — 128 BYTES/SECTOR

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00)[3]
6	00
1	FC (Index Mark)
1 26	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00 (Sector Length)
1	F7 (2 CRC's written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	FF (or 00)
247[2]	FF (or 00)

1. Write bracketed field 26 times
2. Continue writing until 279X interrupts out. Approx. 247 bytes.
3. A '00' option is allowed.

IBM SYSTEM 34 FORMAT-256 BYTES/SECTOR

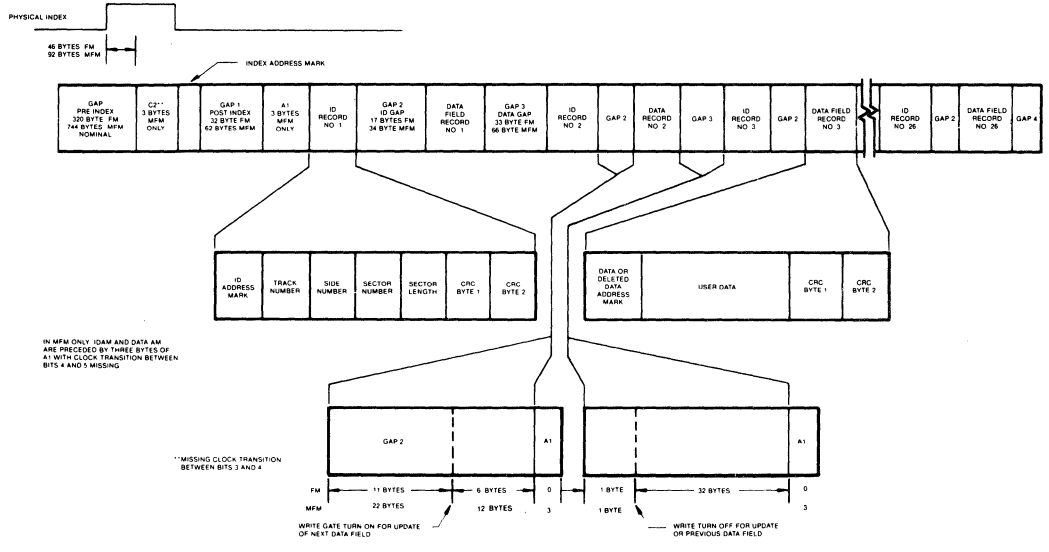
Shown below is the IBM dual-density format with 256 bytes/sector. In order for format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
80	4E
12	00
3	F6 (Writes C2)
1	FC (Index Mark)
* 50	4E
12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01 (Sector Length)
1	F7 (2 CRCs written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRCs written)
54	4E
598**	4E

* Write bracketed field 26 times

** Continue writing until 279X interrupts out. Approx. 598 bytes.

IBM TRACK FORMAT



1. NON-IBM FORMATS

Variations in the IBM formats are possible to a limited extent if the following requirements are met:

1) Sector size must be 128, 256, 512 of 1024 bytes.

2) Gap 2 cannot be varied from the IBM format.

3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the 279X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for 279X operation, however PLL lock up time, motor speed variation, write splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format be used for highest system reliability.

GAP	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00
*		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

* Byte counts must be exact.

** Byte counts are minimum, except exactly 3 bytes of A1 must be written.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Voltage to any input with respect to V_{SS} = +7 to −0.5V

Operating temperature = 0°C to 70°C

Storage temperature = −55°C to +125°C

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

OPERATING CHARACTERISTICS (DC) T_A = 0°C to 70°C, V_{SS} = 0V, V_{CC} = + 5V ± .25V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage			10	μA	$V_{IN} = V_{CC}$
I_{OL}	Output Leakage			10	μA	$V_{OUT} = V_{CC}$
V_{IH}	Input High Voltage	2.0			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OH}	Output High Voltage	2.4			V	I_O = −100μA
V_{OL}	Output Low Voltage			0.45	V	I_O = 1.6 mA
V_{OHP}	Output High PUMP	2.2			V	I_{OP} = −1.0 mA
V_{OLP}	Output Low PUMP			0.2	V	I_{OP} = +1.0 mA
P_D	Power Dissipation			.75	W	All Outputs Open
R_{PU}	Internal Pull-up*	100		1700	μA	V_{IN} = 0V
I_{CC}	Supply Current		70	150	mA	All Outputs Open

* Internal Pull-up resistors on PINS 1, 17, 19, 22, 36, 37 and 40. Also pin 25 on 2793.

TIMING CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{SS} = 0V$, $V_{CC} = +5V \pm .25V$

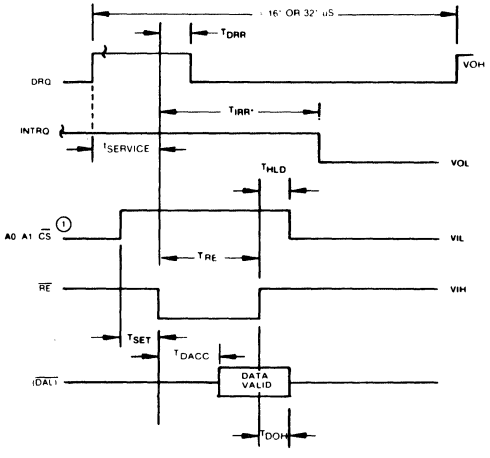
READ ENABLE TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
T_{SET}	Setup ADDR & CS to $\overline{RE}$	50			nsec	
T_{HLD}	Hold ADDR & CS from $\overline{RE}$	10			nsec	
T_{RE}	$\overline{RE}$ Pulse Width	200			nsec	$C_L = 50$ pf
T_{DRR}	DRQ Reset from $\overline{RE}$		100	200	nsec	
T_{IRR}	INTRQ Reset from $\overline{RE}$		500	3000	nsec	See Note
T_{DACC}	Data Valid from $\overline{RE}$		100	200	nsec	$C_L = 50$ pf
T_{DOH}	Data Hold From $\overline{RE}$	20		150	nsec	$C_L = 50$ pf

WRITE ENABLE TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
T_{SET}	Setup ADDR & CS to $\overline{WE}$	50			nsec	
T_{HLD}	Hold ADDR & CS from $\overline{WE}$	10			nsec	
T_{WE}	$\overline{WE}$ Pulse Width	200			nsec	
T_{DRR}	DRQ Reset from $\overline{WE}$		100	200	nsec	
T_{IRR}	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Note
T_{DS}	Data Setup to $\overline{WE}$	150			nsec	
T_{DH}	Data Hold from $\overline{WE}$	50			nsec	

READ ENABLE TIMING

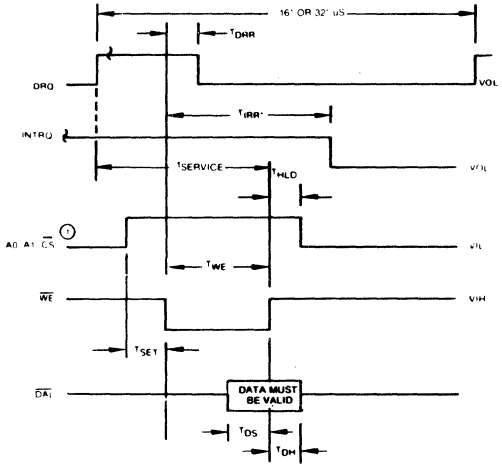


NOTE 1 $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED
*TIME DOUBLES WHEN CLOCK = 1MHz

tSERVICE (WORST CASE)
*FM 27.5 uS
*MFM 13.5 uS

DRQ RISING EDGE: INDICATES THAT THE DATA REGISTER HAS ASSEMBLED DATA.
DRQ FALLING EDGE: INDICATES THAT THE DATA REGISTER WAS READ
INTRQ RISING EDGE: OCCURS AT END OF COMMAND
INTRQ FALLING EDGE: INDICATES THAT THE STATUS REGISTER WAS READ

WRITE ENABLE TIMING



NOTE 1 $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED
2 WHEN WRITING DATA INTO SECTOR TRACK OR DATA REGISTER USER CANNOT READ THIS REGISTER UNTIL AT LEAST 4 μSEC IN MFM AFTER THE RISING EDGE OF WE WHEN WRITING INTO THE COMMAND REGISTER STATUS IS NOT VALID UNTIL SOME 28 μSEC IN FM, 14 μSEC IN MFM LATER. THESE TIMES ARE DOUBLED WHEN CLK = 1 MHz
*TIME DOUBLES WHEN CLOCK = 1MHz

tSERVICE (WORST CASE)
*FM 23.5 uS
*MFM 11.5uS

DRQ RISING EDGE: INDICATES THAT THE DATA REGISTER IS EMPTY
DRQ FALLING EDGE: INDICATES THAT THE DATA REGISTER IS LOADED
INTRQ RISING EDGE: INDICATE THE END OF A COMMAND
INTRQ FALLING EDGE: INDICATES THAT THE COMMAND REGISTER IS WRITTEN TO

INPUT DATA TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
T_{PW}	$\overline{\text{Raw Read}}$ Pulse Width	100	200		nsec	
T_{BC}	$\overline{\text{Raw Read}}$ Cycle Time	1500	2000		nsec	

WRITE DATA TIMING: (ALL TIMES DOUBLE WHEN CLK = 1 MHz) (NO WRITE PRECOMPENSATION)

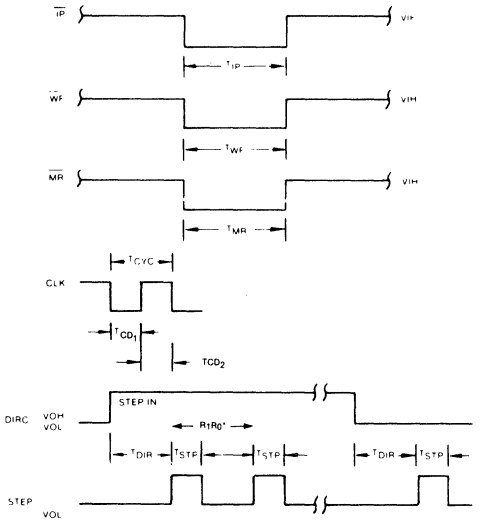
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
T_{WP}	Write Data Pulse Width	400	500	600	nsec	FM
		200	250	300	nsec	MFM
T_{WG}	Write Gate to Write Data		2		µsec	FM
			1		µsec	MFM
T_{WF}	Write Gate off from WD		2		µsec	FM
			1		µsec	MFM

MISCELLANEOUS TIMING:

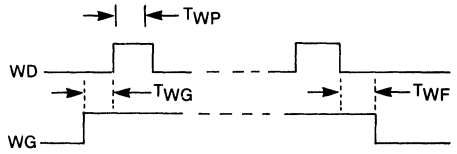
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{CD_1}	Clock Duty (low)	230	250	20000	nsec	
t_{CD_2}	Clock Duty (high)	230	250	20000	nsec	
t_{STP}	Step Pulse Output	2 or 4			µsec	See Note
t_{DIR}	Dir Setup to Step		12		µsec	± CLK ERROR
t_{MR}	Master Reset Pulse Width	50			µsec	
t_{IP}	Index Pulse Width	10			µsec	See Note
RWP	Read Window Pulse Width					Input 0-5V
		120		700	nsec	MFM
		240		1400	nsec	FM ± 15%
	Precomp Adjust.	100		300	nsec	MFM
WPW	Write Data Pulse Width					Precomp = 100 nsec
		200	300	400	nsec	MFM
WPW	Write Data Pulse Width					Precomp = 300 nsec
		600	900	1200	nsec	MFM
VCO	Free Run Voltage Controlled	6.0			MHz	Cext = 0
	Oscillator. Adjustable by ext. capacitor on Pin 26		4.0		MHz	Cext = 35 pf
	Pump Up + 25%	5.0			MHz	PU = 2.2V Cext = 35 pf
VCO	Pump Down − 25%			3.0	MHz	$\overline{PD}$ = 0.2V Cext = 35 pf
	5% Change V_{CC}	3.8		4.2	MHz	Cext = 35 pf
VCO	T_A = 75°C	3.5			MHz	Cext = 35 pf
Cext	Adjustable external capacitor	20	45	100	pf	VCO = 4.0MHz nom
RCLK	Derived read clock = VCO ÷ 8, 16, 32					VCO = 4.0MHz
			500		KHz	$\overline{DDEN}$ = 0 $\overline{5/8}$ = 1
			250		KHz	$\overline{DDEN}$ = 0 $\overline{5/8}$ = 0
			250		KHz	$\overline{DDEN}$ = 1 $\overline{5/8}$ = 1
			125		KHz	$\overline{DDEN}$ = 1 $\overline{5/8}$ = 0
PU/DON	PU/$\overline{PD}$ time on (pulse width)			250	ns	MFM
				500	ns	FM
f_{LOCK}*	Data Separator Capture Range	237.5	250	262.5	kbits/sec	$\overline{5/8}$ = 0

*The f_{LOCK} specification is guaranteed from 10° C to 40° C.

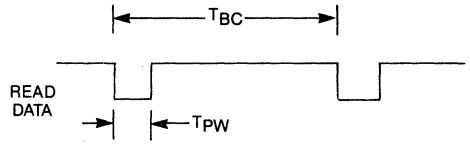
MISCELLANEOUS TIMING



WRITE DATA TIMING



READ DATA TIMING



NOTES:

1. Times double when clock = 1 MHz.
2. Output timing readings are at V_{OL} = 0.8v and V_{OH} = 2.0v.

***FROM STEP RATE TABLE**

TABLE 4. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	0	0
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TROO}}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: Forced to a Zero.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

SUMMARY OF ADJUSTMENT PROCEDURE

WRITE PRECOMPENSATION

1) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.
2) Strobe $\overline{\text{MR}}$ (Pin 19).
3) Set $\overline{\text{TEST}}$ (Pin 22) to a logic low.
4) Observe pulse width on WD (Pin 31).
5) Adjust WPW (Pin 33) for desired pulse width (Precomp Value).
6) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.

DATA SEPARATOR

1) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.
2) Strobe $\overline{\text{MR}}$ (Pin 19). Insure that $\overline{5}/8$, and $\overline{\text{DDEN}}$ are set properly.
3) Set $\overline{\text{TEST}}$ (Pin 22) to a logic low.
4 Observe Pulse Width on TG43 (Pin 29).
5) Adjust RPW (Pin 18) for 1/8 of the read clock (250ns for 8" DD, 500ns for 5¼" DD, etc.).
6) Observe Frequency on DIRC (Pin 16).
7) Adjust variable capacitor on VCO pin for Data Rate (500 KHz for 8" DD, 250 KHz for 5¼" DD, etc.).
8) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.

NOTE: To maintain internal VCO operation, insure that $\overline{\text{TEST}}$ = 1 whenever a master reset pulse is applied.

VL4500A

DYNAMIC RAM CONTROLLER

FEATURES

- Controls operation of 8K/16K/32K/64K dynamic RAMs
- Creates static RAM appearance
- One package contains address multiplexer, refresh control and timing control
- Directly addresses and drives up to 256K bytes of memory without external drivers
- Operates from microprocessor clock
  - — No crystals, delay lines, or RC networks
  - — Eliminates arbitration delays
- Refresh may be internally or externally initiated
- Ability to synchronize or interleave controller with the microprocessor system (including multiple controllers)
- 3-state outputs allow multiport memory configuration
- Performance ranges of 150 ns/200 ns/250 ns
- Compatible with TI TMS 4500A

DESCRIPTION

The VL4500A is a monolithic DRAM system controller designed to provide address multiplexing, timing, control and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

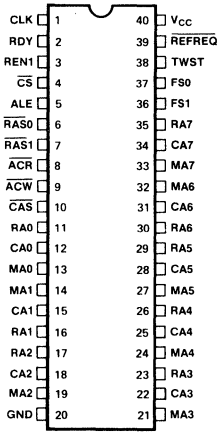
The controller contains a 16-bit multiplexer that generates the address lines for the memory device from the 16 system address bits and provides the strobe signals required by the memory to decode the address. An 8-bit refresh counter generates the 256-row addresses required to refresh.

A refresh timer is provided that generates the necessary timing to refresh the dynamic memories and assure data retention.

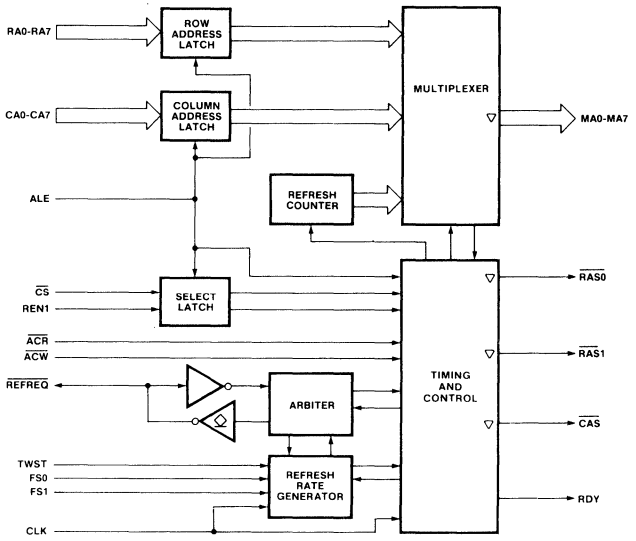
The VL4500A also contains refresh/access arbitration circuitry to resolve conflicts between memory access requests and memory refresh cycles.

PIN DIAGRAM

VL4500A



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Access Time	Package
VL4500A-15PC VL4500A-15CC	150 ns	Plastic DIP Ceramic DIP
VL4500A-20PC VL4500A-20CC	200 ns	Plastic DIP Ceramic DIP
VL4500A-25PC VL4500A-25CC	250 ns	Plastic DIP Ceramic DIP

Note:
Operating temperature range: 0°C to +70°C.

PIN DESCRIPTIONS

RA0-RA7	Input	Row Address — Used to generate the row address for the multiplexer.
CA0-CA7	Input	Column Address — Used to generate the column address for the multiplexer.
MA0-MA7	Output	Memory Address — 3-state outputs designed to drive the addresses of the Dynamic RAM array.
ALE	Input	Address Latch Enable — Used to latch the 16 address inputs, $\overline{CS}$ and REN1. This also initiates an access cycle if Chip Select is valid. The rising edge (LOW-to-HIGH level) of ALE returns $\overline{RAS}$ to HIGH.
$\overline{CS}$	Input	Chip Select — A LOW on this input enables an access cycle. The trailing edge of ALE latches the Chip Select input.
REN1	Input	RAS Enable 1 — Used to select one of two banks of RAM via the $\overline{RAS0}$ and $\overline{RAS1}$ outputs when chip select is present. When LOW, $\overline{RAS0}$ is selected; when HIGH, $\overline{RAS1}$ is selected.
$\overline{ACR}$, $\overline{ACW}$	Input	Access Control, Read; Access Control, Write — A LOW on either of these inputs causes the column address to appear on MA0-MA7 and the Column Address Strobe to pulse active LOW. The rising edge of $\overline{ACR}$ or $\overline{ACW}$ terminates the cycle by ending $\overline{RAS}$ and $\overline{CAS}$ strobes. When $\overline{ACR}$ and $\overline{ACW}$ are both LOW, MA0-MA7, $\overline{RAS0}$, $\overline{RAS1}$, and $\overline{CAS}$ go into a high-impedance (floating) state.
CLK	Input	System Clock — Provides the master timing to generate refresh cycle timings and refresh rate. Refresh rate is determined by the TWST, FS1, FS0 inputs.
$\overline{REFREQ}$	Input/ Output	Refresh Request — (This input should be driven by an open-collector output.) On input, a LOW-going edge initiates a refresh cycle and will cause the internal refresh timer to be reset on the next falling edge of the CLK. As an output, a LOW-going edge signals an internal refresh request and that the refresh timer will be reset on the next LOW-going edge of CLK. $\overline{REFREQ}$ will remain LOW until the refresh cycle is in progress and the current refresh address is present on MA0-MA7. (Note: $\overline{REFREQ}$ contains an internal pull-up resistor with a nominal resistance of 10 kΩ.)
$\overline{RAS0}$, $\overline{RAS1}$	Output	Row Address Strobe — 3-state outputs used to latch the row address into the bank of DRAMs selected by REN1. On refresh both signals are driven.
$\overline{CAS}$	Output	Column Address Strobe — 3-state output used to latch the column address into the DRAM array.
RDY	Output	Ready — Totem-pole output used to synchronize memories that are too slow to guarantee microprocessor access time requirements. This output is also used to inhibit access cycles during refresh when in cycle-steal mode.
TWST	Input	Timing/Wait Strap — A HIGH on this input indicates a wait state should be added to each memory cycle. In addition, it is used in conjunction with FS0 and FS1 to determine refresh rate and timing.
FS0, FS1	Inputs	Frequency Select 0; Frequency Select 1 — Strap inputs used to select Mode and Frequency of operation as shown in Table 1.

TABLE 1: STRAP CONFIGURATION

Strap Input Modes			Wait States For Memory Access	Refresh Rate	Minimum Clk Freq (MHz)	Refresh Freq (kHz)	Clock Cycles For Each Refresh
TWST	FS1	FS0					
L	L	L (1)	0	External	—	Refreq.	4
L	L	H	0	Clk ÷ 31	1.984	64-95 (2)	3
L	H	L	0	Clk ÷ 46	2.944	64-85 (2)	3
L	H	H	0	Clk ÷ 61	3.904	64-82 (3)	4
H	L	L	1	Clk ÷ 46	2.944	64-85 (2)	3
H	L	H	1	Clk ÷ 61	3.904	64-80 (2)	4
H	H	L	1	Clk ÷ 76	4.864	64-77 (2)	4
H	H	H	1	Clk ÷ 91	5.824	64-88 (4)	4

Notes:
1. This strap configuration resets the Refresh Timer circuitry.
2. Upper figure in refresh frequency is the frequency produced if the minimum CLK frequency of the next select state is used.
3. Refresh frequency if CLK frequency is 5 MHz.
4. Refresh frequency if CLK frequency is 8 MHz.

FUNCTIONAL DESCRIPTION

VL4500A consists of six basic blocks; address and select latches, refresh rate generator, refresh counter, the multiplexer, the arbiter, and the timing and control block.

ADDRESS AND SELECT LATCHES

The address and select latches allow the DRAM controller to be used in systems that multiplex address and data on the same lines without external latches. The row address latches are transparent, meaning that while ALE is HIGH, the output at MA0-MA7 follows the inputs RA0-RA7.

REFRESH RATE GENERATOR

The refresh rate generator is a counter that indicates to the arbiter that it is time for a refresh cycle. The counter divides the clock frequency according to the configuration straps as shown in Table 1. The counter is reset when a refresh cycle is requested or when TWST, FS1 and FS0 are LOW. The configuration straps allow the matching of memories to the system access time.

Upon power-up it is necessary to provide a reset signal by driving all three straps to the controller LOW to initialize internal counters. A system's LOW-active, power-on reset ($\overline{\text{RESET}}$) can be used to accomplish this by connecting it to those straps that are desired HIGH during operation. During this reset period, at least four clock cycles should occur.

REFRESH COUNTER

The refresh counter contains the address of the row to be refreshed. The counter is decremented after each refresh cycle. | A LOW-to-HIGH transition on TWST sets the refresh counter to FF_{16} (255_{10}). |

MULTIPLEXER

The multiplexer provides the DRAM array with row, column, and refresh addresses at the proper times. Its inputs are the address latches and the refresh counter. The outputs provide up to 16 multiplexed addresses on eight lines.

ARBITER

The arbiter provides two operational cycles; access and refresh. The arbiter resolves conflicts between cycle requests and cycles in execution, and schedules the inhibited cycle when used in cycle-steal mode.

TIMING AND CONTROL BLOCK

The timing and control block executes the operational cycle at the request of the arbiter. It provides the DRAM array with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals. It provides the CPU with a RDY signal. It controls the multiplexer during all cycles. It resets the refresh rate generator and decrements the refresh counter during refresh cycles.

ABSOLUTE MAXIMUM RATINGS

Operating Ambient Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Supply Voltage Range, V_{CC}, Note 1	−1.5 to +7 V
Input Voltage Range (any input), Note 1	−1.5 to +7 V
Continuous Power Dissipation	1.2 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those listed on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: T_A = 0°C to +70°C

Symbol	Parameter		Min	Typ (3)	Max	Unit	Conditions
V_{IL} (except $\overline{REFREQ}$)	Input LOW Voltage		−1.0 (2)		0.8	V	
V_{IL} ($\overline{REFREQ}$)	Input LOW Voltage		−1.0 (2)		0.8	V	
V_{IH}	Input HIGH Voltage		2.4		6.0	V	
V_{OL}	Output LOW Voltage				0.4	V	I_{OL} = 4 mA V_{CC} = 4.5 V
V_{OH}	Output HIGH Voltage	MA0-MA7, RDY	2.4				I_{OH} = −1 mA V_{CC} = 4.5 V
		$\overline{RAS0}$, $\overline{RAS1}$, $\overline{CAS}$	2.7			V	
		$\overline{REFREQ}$	2.4				I_{OH} = −100 μA V_{CC} = 4.5 V
I_{IH}	Input HIGH Current All pins except $\overline{REFREQ}$				10	μA	V_I = 5.5 V
I_{IL}	Input LOW Current	$\overline{REFREQ}$			−1.25	mA	V_I = 0 V
		All others			−10	μA	
I_{OZ}	Output Off-State Current				±50	μA	V_O = 0 to 4.5 V V_{CC} = 5.5 V
I_{CC}	Operating Supply Current			100	140	mA	T_A = 0°C V_{CC} = 5.5 V

CAPACITANCE: T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Min	Typ (3)	Max	Unit	Conditions	
C_I	Input Capacitance		5		pF	V_I = 0 V	f = 1 MHz
C_O	Output Capacitance		6		pF	V_O = 0 V	f = 1 MHz

Notes:

1. Voltage values are with respect to the ground terminal.
2. The algebraic convention, where the more negative limit is designated as minimum, is used in this data sheet for logic voltage levels only.
3. All typical values are at V_{CC} = 5 V, T_A = 25°C except where otherwise noted.

AC CHARACTERISTICS: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 10\%$

Symbol	Parameter	VL4500A-15		VL4500A-20		VL4500A-25		Unit
		Min	Max	Min	Max	Min	Max	
$t_{C(C)}$	CLK Cycle Time	100		120		140		ns
$t_{W(CH)}$	CLK HIGH Pulse Width	40		40		40		
$t_{W(CL)}$	CLK LOW Pulse Width	40		45		45		
t_t	Transition Time, All Inputs		50		50		50	
t_{AEL-CL}	Time Delay, ALE LOW to CLK Starting LOW, Note 1	10		10		15		
t_{CL-AEL}	Time Delay, CLK LOW to ALE Starting LOW, Note 1	10		10		15		
t_{CL-AEH}	Time Delay, CLK LOW to ALE Starting HIGH, Note 2	15		20		20		
$t_{W(AEH)}$	Pulse Width ALE HIGH	50		60		60		
t_{AV-AEL}	Time Delay, Address, REN1, $\overline{CS}$ Valid to ALE LOW	5		10		15		
t_{AEL-AX}	Time Delay, ALE LOW to Address Not Valid	10		10		10		
$t_{AEL-ACL}$	Time Delay, ALE LOW to $\overline{ACX}$ LOW, Notes 3, 4, 5, 6	$t_{h(RA)} + 30$		$t_{h(RA)} + 40$		$t_{h(RA)} + 50$		
t_{ACH-CL}	Time Delay, $\overline{ACX}$ HIGH to CLK LOW, Notes 3, 7	20		20		20		
t_{ACL-CH}	Time Delay, $\overline{ACX}$ LOW to CLK Starting HIGH (to remove RDY)	30		30		30		
t_{RQL-CL}	Time Delay, $\overline{REFREQ}$ LOW to CLK Starting LOW, Note 8	20		20		20		
$t_{W(RQL)}$	Pulse Width, $\overline{REFREQ}$ LOW	20		20		20		

Notes:

1. Coincidence of the trailing edge of CLK and the trailing edge of ALE should be avoided, as the refresh/access occurs on the trailing CLK edge. A trailing edge of CLK should occur during the interval from $\overline{ACX}$ HIGH to ALE LOW.
2. If ALE rises before $\overline{ACX}$ and a refresh request is present, the falling edge of CLK after t_{CL-AEH} will output the refresh address to MA0-MA7 and initiate a refresh cycle.
3. These specifications relate to system timing and do not directly reflect device performance.
4. On the access grant cycle following refresh, the occurrence of $\overline{CAS}$ LOW depends on the relative occurrence of ALE LOW to $\overline{ACX}$ LOW. If $\overline{ACX}$ occurs prior to or coincident with ALE then $\overline{CAS}$ is timed from the CLK HIGH transition that causes RAS LOW. If $\overline{ACX}$ occurs 20 ns or more after ALE then $\overline{CAS}$ is timed from the CLK LOW transition following the CLK HIGH transition causing RAS LOW.
5. For maximum speed access (internal delays on both access and access grant cycles), $\overline{ACX}$ should occur prior to or coincident with ALE.
6. $t_{h(RA)}$ is the dynamic memory row address hold time. $\overline{ACX}$ should follow ALE by $t_{AEL-CEL}$ in systems where the required $t_{h(RA)}$ is greater than $t_{REL-MAX}$ minimum.
7. Minimum of 20 ns is specified to ensure arbitration will occur on falling CLK edge. t_{ACH-CL} also affects precharge time such that the minimum t_{ACH-CL} should be equal or greater than: $t_{W(RH)}-t_{W(CL)} + 30$ ns (for cycle where $\overline{ACX}$ HIGH occurs prior to ALE HIGH) where $t_{W(RH)}$ is the DRAM $\overline{RAS}$ precharge time.
8. This parameter is necessary only if refresh arbitration is to occur on this falling edge of CLK (in systems where refresh is synchronized to external events).

AC CHARACTERISTICS: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 10\%$

Symbol	Parameter	VL4500A-15 Min	VL4500A-15 Max	VL4500A-20 Min	VL4500A-20 Max	VL4500A-25 Min	VL4500A-25 Max	Unit	Conditions
$t_{AEL-REL}$	Time Delay, ALE LOW to $\overline{RAS}$ Starting LOW		35		40		50		
$t_{t\ (REL)}$	$\overline{RAS}$ Fall Time		15		20		25		$C_L = 160$ pF
$t_{RAV-MAV}$	Time Delay, Row Address Valid to Memory Address Valid		45		50		60		
$t_{AEH-MAV}$	Time Delay, ALE HIGH to Valid Memory Address		65		75		90		
$t_{AEL-RYL}$	Time Delay, ALE to RDY Starting LOW (TWST = 1 or Refresh in Progress)		40		40		40		$C_L = 40$ pF
$t_{AEL-CEL}$	Time Delay, ALE LOW to $\overline{CAS}$ Starting LOW, Note 9	60	150	70	200	80	250		
$t_{AEH-REH}$	Time Delay, ALE HIGH to $\overline{RAS}$ Starting HIGH		30		30		40		$C_L = 160$ pF
$t_{t\ (MAV)}$	Address Transition Time		20		20		25		
$t_{ACL-MAX}$	Row Address Hold from $\overline{ACX}$ LOW	15		20		25			
$t_{MAV-CEL}$	Time Delay, Memory Address Valid to $\overline{CAS}$ Starting LOW	0		0		0			
$t_{t\ (CEL)}$	$\overline{CAS}$ Fall Time		15		20		25		$C_L = 320$ pF
$t_{ACL-CEL}$	Time Delay, $\overline{ACX}$ LOW to $\overline{CAS}$ Starting LOW, Note 9	40	100	45	130	50	165		
$t_{ACH-REH}$	Time Delay, $\overline{ACX}$ to $\overline{RAS}$ Starting HIGH		30		40		50		$C_L = 160$ pF
$t_{t\ (REH)}$	$\overline{RAS}$ Rise Time		15		20		25		
$t_{ACH-CEH}$	Time Delay, $\overline{ACX}$ HIGH to $\overline{CAS}$ Starting HIGH	5	30	10	40	15	50	ns	
$t_{t\ (CEH)}$	$\overline{CAS}$ Rise Time		30		35		45		$C_L = 320$ pF
$t_{ACH-MAX}$	Column Address Hold from $\overline{ACX}$ HIGH	10		15		15			$C_L = 160$ pF
t_{CH-RYH}	Time Delay, CLK HIGH to RDY Starting HIGH (After $\overline{ACX}$ LOW), Note 10		40		45		60		
$t_{RFL-RFL}$	Time Delay, $\overline{REFREQ}$ External Until Supported by $\overline{REFREQ}$ Internal		30		35		35		$C_L = 40$ pF
t_{CH-RFL}	Time Delay, CLK HIGH Until $\overline{REFREQ}$ Internal Starting LOW		30		35		45		
t_{CL-MAV}	Time Delay, CLK LOW Until Refresh Address Valid		75		100		125		
t_{CH-RRL}	Time Delay, CLK HIGH Until Refresh $\overline{RAS}$ Starting LOW	10	50	15	60	20	80		
$t_{MAV-RRL}$	Time Delay, Refresh Address Valid Until Refresh $\overline{RAS}$ LOW	5		5		5			
t_{CL-RFH}	Time Delay, CLK LOW to $\overline{REFREQ}$ Starting HIGH (3-cycle Refresh)		50		55		75		$C_L = 160$ pF
t_{CH-RFH}	Time Delay, CLK HIGH to $\overline{REFREQ}$ Starting HIGH (4-cycle Refresh)		50		55		75		
t_{CH-RRH}	Time Delay, CLK HIGH to Refresh $\overline{RAS}$ Starting HIGH	5	35	10	45	10	60		
t_{CH-MAX}	Time Delay, Refresh Address Hold After CLK HIGH	15		20		25			

Notes:

9. The falling edge of $\overline{CAS}$ occurs as soon as both $t_{AEL-CEL}$ and $t_{ACL-CEL}$ have elapsed. If $\overline{ACX}$ goes LOW prior to ($t_{AEL-CEL}$) - ($t_{ACL-CEL}$) after ALE, the $\overline{CAS}$ timing is determined by $t_{AEL-CEL}$. Otherwise, the access time increases, and the falling edge of $\overline{CAS}$ is measured from the falling edge of $\overline{ACX}$ instead of ALE ($t_{ACL-CEL}$ determines $\overline{CAS}$ timing).
10. RDY returns HIGH on the rising edge of CLK. If TWST = 0, then on an access grant cycle RDY goes HIGH on the same edge that causes access $\overline{RAS}$ LOW. If TWST = 1, then RDY goes to the HIGH level on the first rising CLK edge after $\overline{ACX}$ goes LOW on access cycles and on the next rising edge after the edge that causes access $\overline{RAS}$ LOW on access grant cycles (assuming $\overline{ACX}$ LOW).

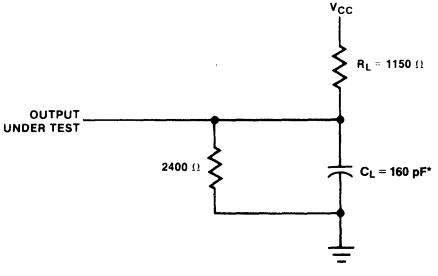
AC CHARACTERISTICS: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 10\%$

Symbol	Parameter	VL4500A-15		VL4500A-20		VL4500A-25		Unit	Conditions
		Min	Max	Min	Max	Min	Max		
t_{CH-REL}	Time Delay, CLK HIGH Until Access $\overline{RAS}$ Starting LOW		60		70		95	ns	$C_L = 160$ pF
t_{CL-CEL}	Time Delay, CLK LOW to Access $\overline{CAS}$ Starting LOW, Note 11		125		140		185		
t_{CL-MAX}	Row Address Hold After CLK LOW	25		30		40			
$t_{W(ACL)}$	$\overline{ACX}$ LOW Width, Note 12	110		140		175			
$t_{REL-MAX}$	Row Address Hold From $\overline{RAS}$ LOW	25		30		35			
$t_{t(RYL)}$	RDY Fall Time		10		15		20		$C_L = 40$ pF
$t_{t(RYH)}$	RDY Rise Time		20		25		35		
t_{dis}	Output Disable Time (3-state Outputs)		100		125		165		$C_L = 160$ pF
$t_{AEH-MAX}$	Column Address Hold From ALE HIGH	10		15		20			
t_{en}	Output Enable Time (3-state Outputs)		75		80		105		
$t_{CAV-CEL}$	Column Address Setup to $\overline{CAS}$ After Refresh	0		0		0			
t_{CH-CEL}	Time Delay, CLK HIGH to Access $\overline{CAS}$ Starting LOW, Note 11		180		200		235		
t_{ACL-CL}	$\overline{ACX}$ LOW to CLK Starting LOW, Note 13	25		35		45			$C_L = 40$ pF
$t_{ACL-RYH}$	$\overline{ACX}$ LOW to RDY Starting HIGH, Note 13		40		50		60		
t_{CL-ACL}	CLK LOW to $\overline{ACX}$ Starting LOW, Note 13	0		0		0			

Notes:

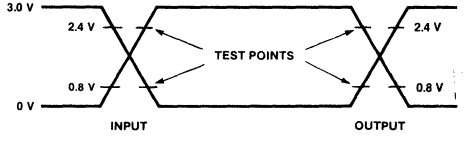
11. On the access grant cycle following refresh, the occurrence of $\overline{CAS}$ LOW depends on the relative occurrence of ALE LOW to $\overline{ACX}$ LOW. If $\overline{ACX}$ occurs prior to or coincident with ALE then $\overline{CAS}$ is timed from the CLK HIGH transition that causes $\overline{RAS}$ LOW. If $\overline{ACX}$ occurs 20 ns or more after ALE then $\overline{CAS}$ is timed from the CLK LOW transition following the CLK HIGH transition causing $\overline{RAS}$ LOW.
12. The specification of $t_{W\ (ACL)}$ is designed to allow a $\overline{CAS}$ pulse. This assures normal operation of the device in testing and system operation.
13. For RDY HIGH transition (during normal access) to be timed from the rising edge of CLK, $\overline{ACX}$ must occur t_{CL-ACL} after the falling edge of CLK. For $\overline{ACX}$ prior to the falling edge of CLK by t_{ACL-CL}, the RDY HIGH transition will be $t_{ACL-RYH}$. Note that t_{ACL-CL} is a limiting parameter for control of RDY to be dependent on $\overline{ACX}$ LOW. During the interval for t_{ACL-CL} < MINIMUM to t_{CL-ACL} > MINIMUM, the control of RDY may vary between the rising clock edge or falling edge of $\overline{ACX}$.

LOAD CIRCUIT



*C_L INCLUDES JIG CAPACITANCE

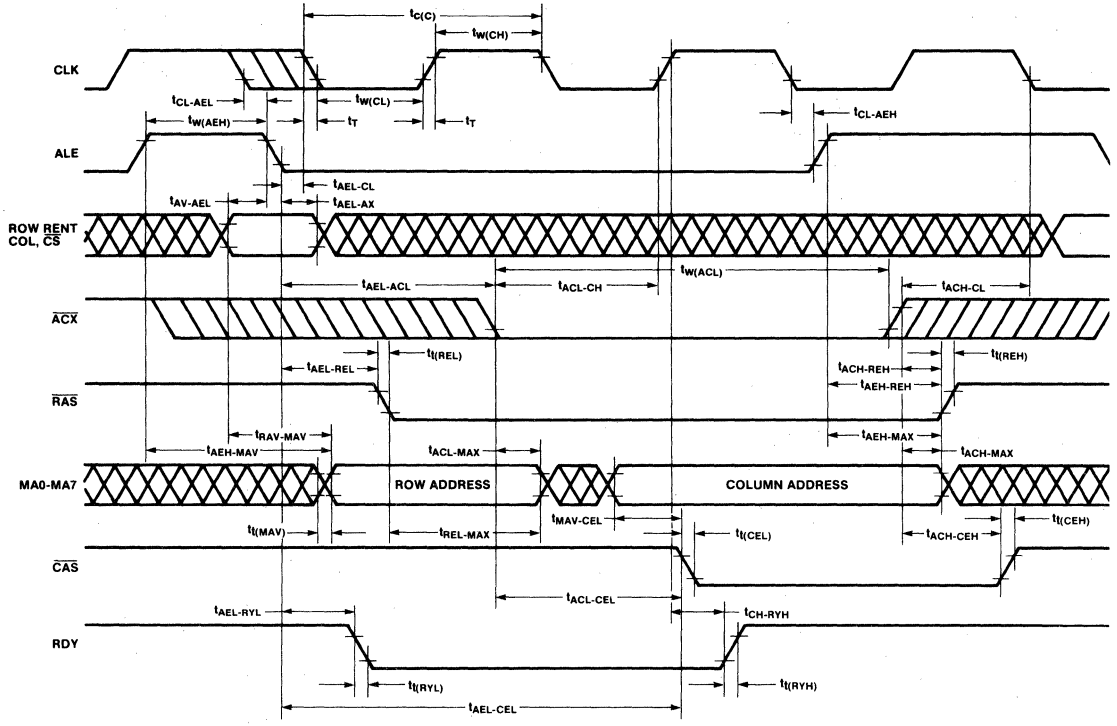
AC TESTING INPUT, OUTPUT WAVEFORM



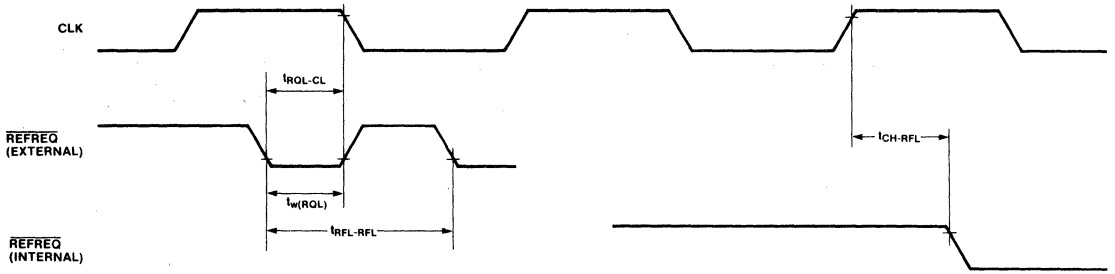
AC testing inputs are driven at 3.0 V for a logic "1" and 0.0 V for a logic "0". Timing measurements are made at 2.2 V for a logic "1" and 0.6 V for a logic "0" at the outputs. The inputs are measured at 2.4 V for a logic "1" and 0.8 V for a logic "0".

TIMING DIAGRAMS

ACCESS CYCLE TIMING

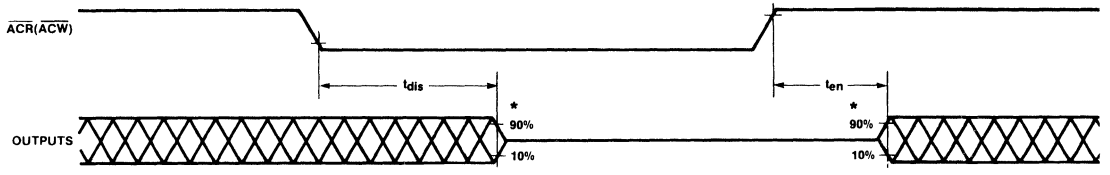


REFRESH REQUEST TIMING

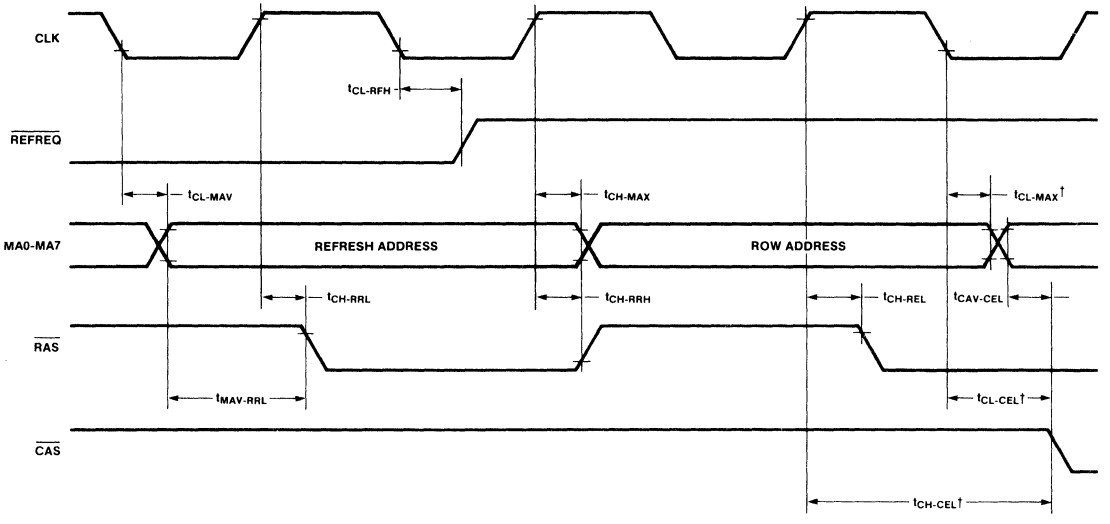


TIMING DIAGRAMS (Cont.)

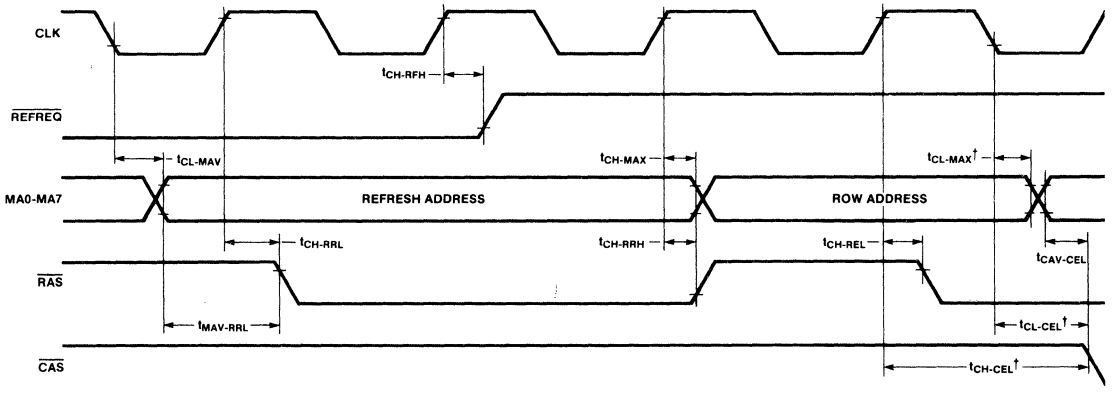
OUTPUT 3-STATE TIMING



REFRESH CYCLE TIMING (3-CYCLE)



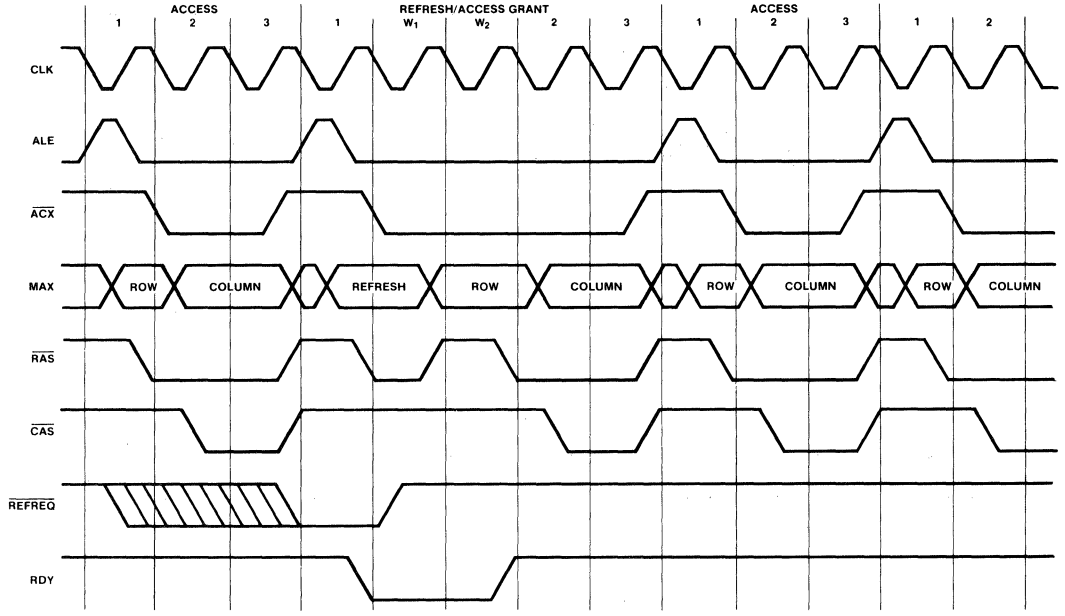
REFRESH CYCLE TIMING (4-CYCLE)



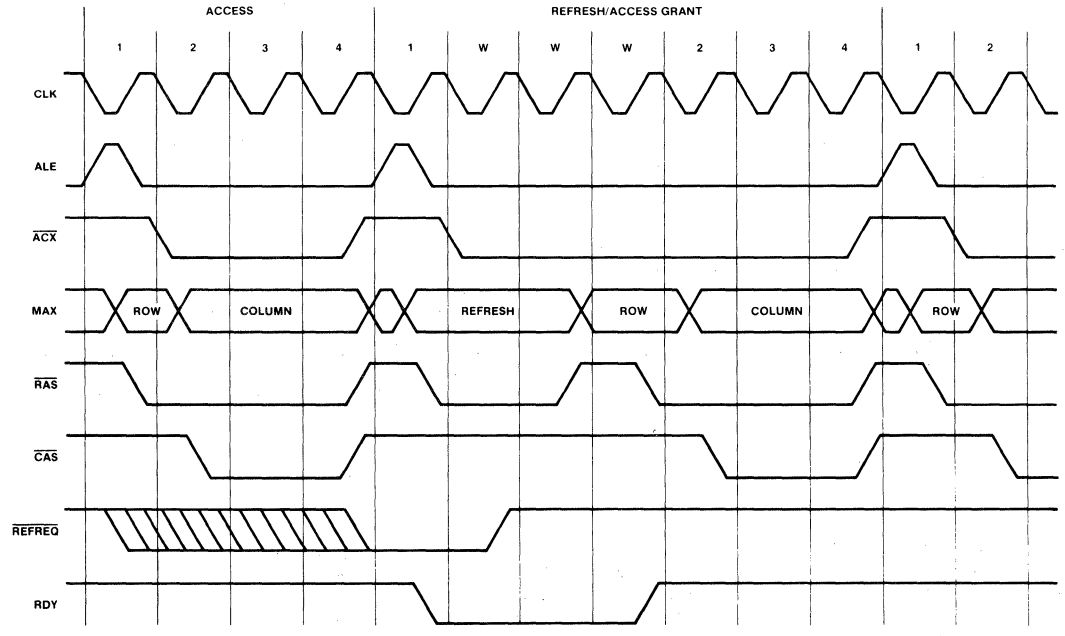
*The voltage levels (on a $\overline{RAS}$ or $\overline{CAS}$ pin) used for testing t_{DIS} and t_{EN} are at 10% and 90% of the V_{OH}-V_{OL} range for that pin.
†On the access grant cycle following refresh, the occurrence of $\overline{CAS}$ LOW depends on the relative occurrence of ALE LOW to $\overline{ACX}$ LOW. If $\overline{ACX}$ occurs prior to or coincident with ALE then $\overline{CAS}$ is timed from the CLK HIGH transition that causes $\overline{RAS}$ LOW. If $\overline{ACX}$ occurs 20 ns or more after ALE then $\overline{CAS}$ is timed from the CLK LOW transition following the CLK HIGH transition causing $\overline{RAS}$ LOW.

TIMING DIAGRAMS (Cont.)

TYPICAL ACCESS/REFRESH/ACCESS CYCLE (3-CYCLE, TWST = 0)

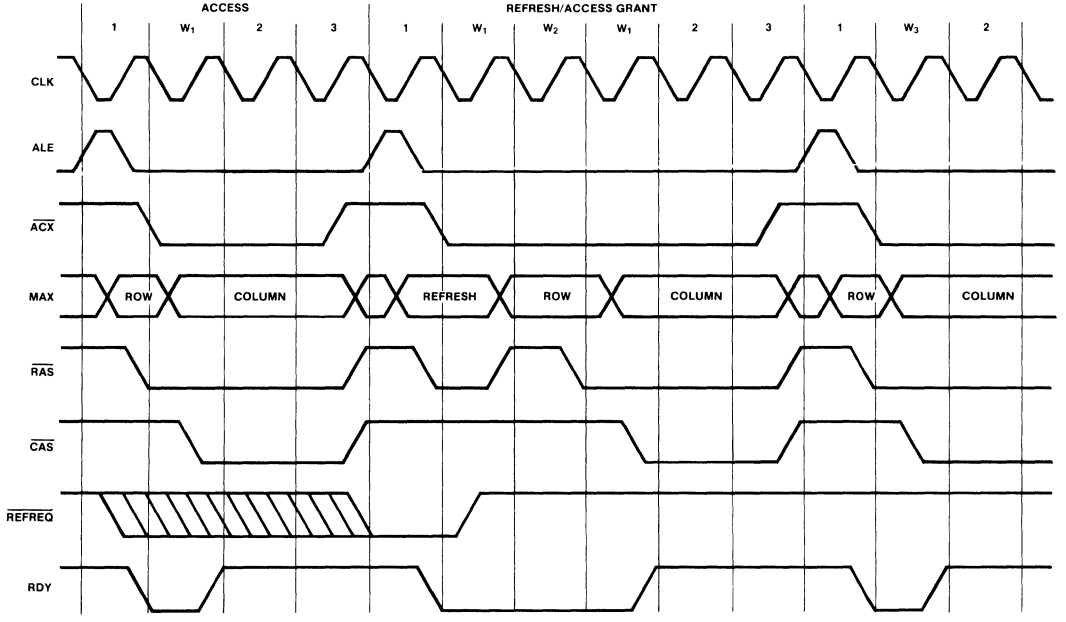


TYPICAL ACCESS/REFRESH/ACCESS CYCLE (4-CYCLE, TWST = 0)

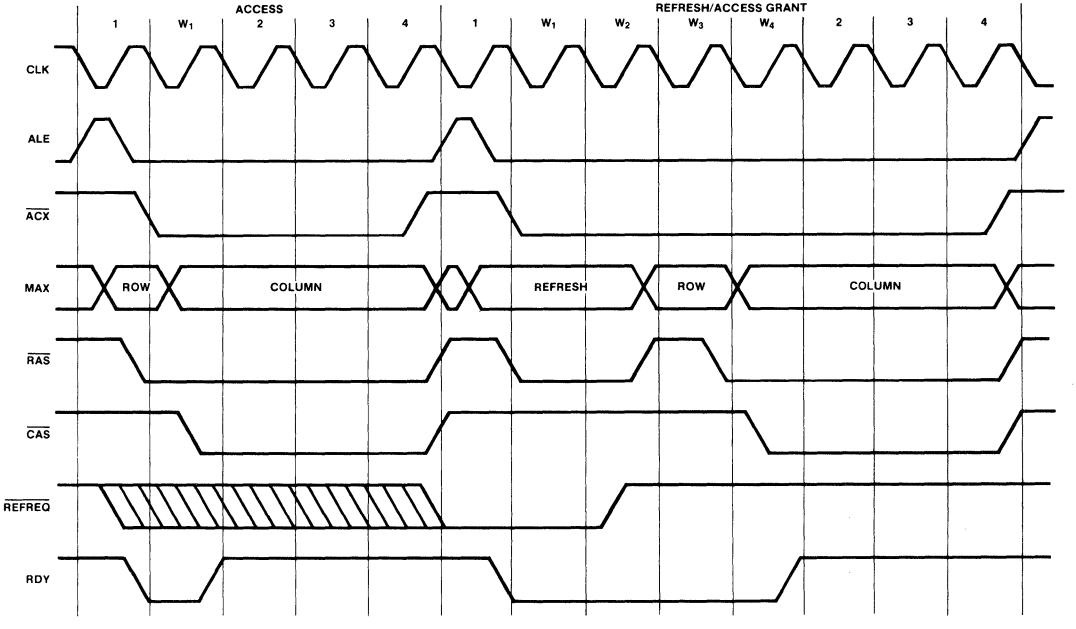


TIMING DIAGRAMS (Cont.)

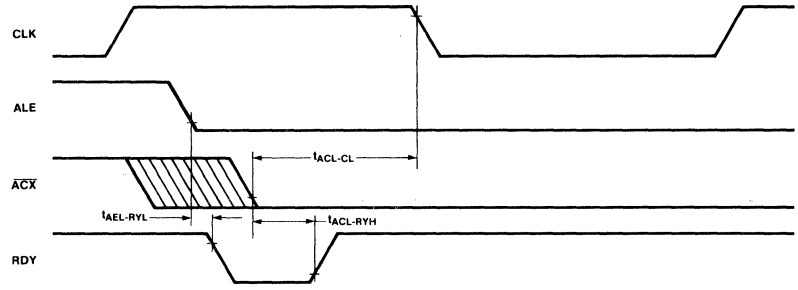
TYPICAL ACCESS/REFRESH/ACCESS CYCLE (3-CYCLE, TWST = 1)



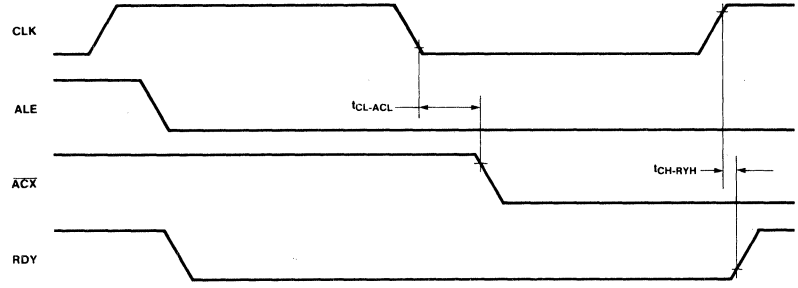
TYPICAL ACCESS/REFRESH/ACCESS CYCLE (4-CYCLE, TWST = 1)



READY (RDY) SIGNAL TIMING (WAIT STATE OPERATION, TWST = 1)



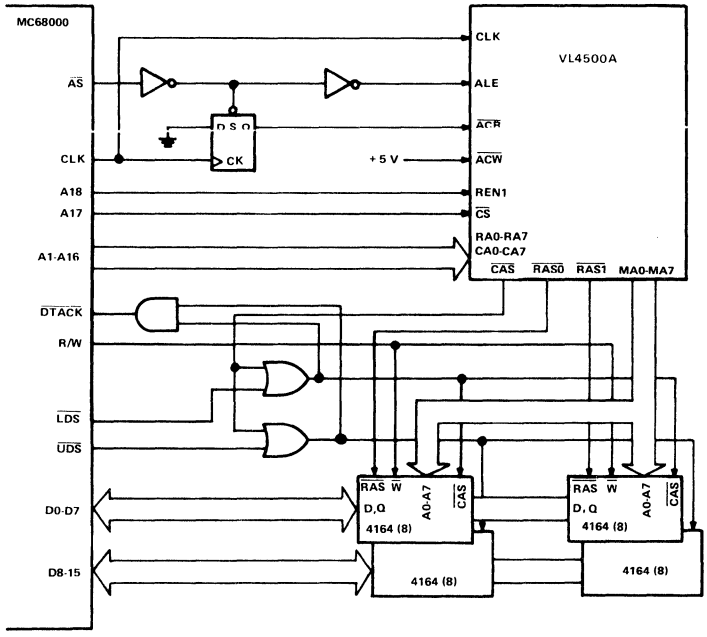
RDY starting HIGH is timed from $\overline{ACX}$ LOW ($t_{ACL-RYH}$) for the condition $\overline{ACX}$ going LOW while CLK HIGH.



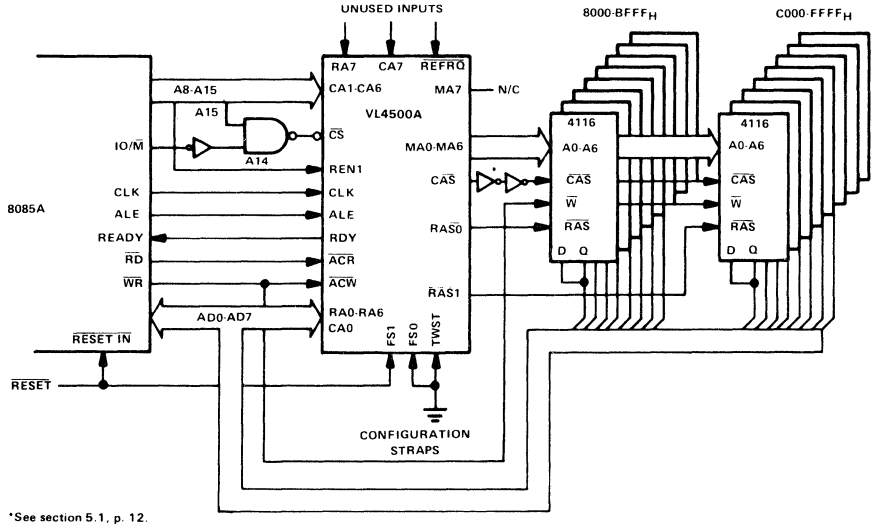
RDY starting HIGH is timed from CLK HIGH (t_{CH-RYH}) for the condition $\overline{ACX}$ going LOW while CLK LOW.

TYPICAL APPLICATIONS

68000 CPU TO VL4500A 128K x 16 MEMORY INTERFACE



8085A CPU INTERFACE TO VL4500A CONTROLLER



*See section 5.1, p. 12.

VL4502

DYNAMIC RAM CONTROLLER

FEATURES

- Inputs are TTL voltage compatible
- Controls operation of 64K and 256K dynamic RAMs
- Creates static RAM appearance
- One package contains address multiplexer, refresh control and timing control
- Directly addresses and drives up to 2 megabytes of memory without external drivers
- Operates from microprocessor clock
  - —No crystals, delay lines, or RC networks
  - —Eliminates arbitration delays
- Refresh may be internally or externally initiated
- High performance CMOS technology
- Strap-selected wait state generation for microprocessor/ memory speed matching
- Ability to synchronize or interleave controller with the microprocessor system (including multiple controllers)
- 3-state outputs allow multiport memory configuration
- Performance ranges of 150 ns/200 ns
- Compatible with VLSI VL4500A and TI TMS4500A, THCT4502

DESCRIPTION

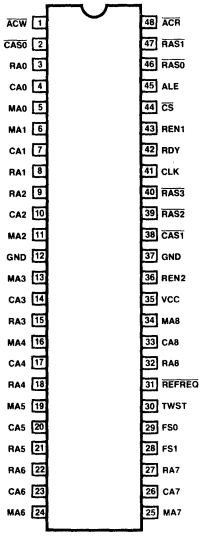
The VL4502 is a monolithic DRAM system controller providing address multiplexing, timing, control and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

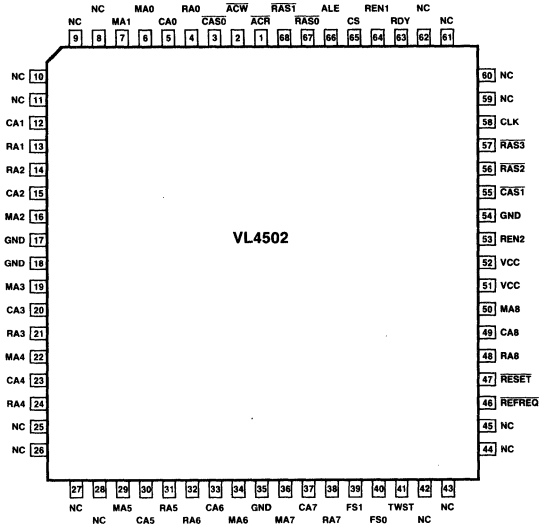
The controller contains an 18-bit multiplexer that generates the address lines for the memory device from the 18 system address bits and provides the strobe signals required by the memory to decode the address. A 9-bit refresh counter generates up to 512 row addresses required to refresh.

A refresh timer is provided that generates the necessary timing to refresh the dynamic memories and assure data retention.

PIN DIAGRAMS

VL4502 DIP



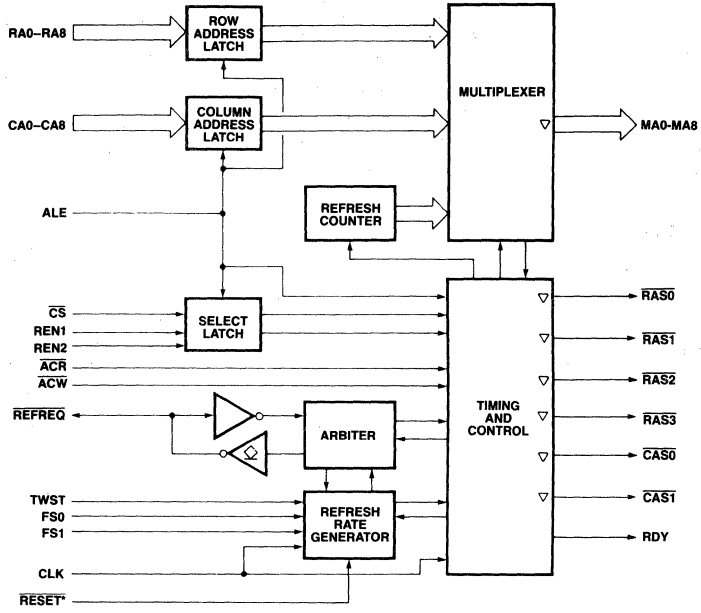


ORDER INFORMATION

Part Number	Access Time	Package
VL4502-15PC	150 ns	Plastic DIP
VL4502-15CC		Ceramic DIP
VL4502-15QC		Plastic Leaded Chip Carrier (PLCC)
VL4502-20PC	200 ns	Plastic DIP
VL4502-20CC		Ceramic DIP
VL4502-20QC		Plastic Leaded Chip Carrier (PLCC)

Note:
Operating temperature range: 0°C to +70°C.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin Name	Pin Number, Note 1	Description
RA0–RA8	3, 8, 9, 15, 18, 21, 22, 27, 32	Row Address—These address inputs are used to generate the row address for the multiplexer.
CA0–CA8	4, 7, 10, 14, 17, 20, 23, 26, 33	Column Address—These address inputs are used to generate the column address for the multiplexer.
MA0–MA8	5, 6, 11, 13, 16, 19, 24, 25, 34	Memory Address—These three-state outputs are designed to drive the addresses of the Dynamic RAM array.
ALE	45	Address Latch Enable—This input is used to latch the 18 address inputs, $\overline{CS}$ and REN1 and REN2. This also initiates an access cycle if chip select is valid. The rising edge (LOW level to HIGH level) of ALE returns $\overline{RAS}$ to the HIGH level.
$\overline{CS}$	44	Chip Select—A LOW on this input enables an access cycle. The trailing edge of ALE latches the chip select input.
REN1, REN2	43, 36	$\overline{RAS}$ Enable 1 and 2—These inputs are used to select one of four banks of RAM. When REN2 is LOW, the lower banks are enabled via $\overline{CAS0}$, $\overline{RAS0}$, and $\overline{RAS1}$. When REN2 is HIGH, the higher banks are enabled via $\overline{CAS1}$, $\overline{RAS2}$, and $\overline{RAS3}$. REN1 selects $\overline{RAS0}$, $\overline{RAS2}$ or $\overline{RAS1}$, $\overline{RAS3}$ when chip select is present.
$\overline{ACR}$, $\overline{ACW}$	48, 1	Access Control, Read; Access Control, Write—A LOW on either of these inputs causes the column addresses to appear on MA0–MA8 and the column address strobe. The rising edge of $\overline{ACR}$ or $\overline{ACW}$ terminates the cycle by ending $\overline{RAS}$ and $\overline{CAS}$ strobes. When $\overline{ACR}$ and $\overline{ACW}$ are both LOW, MA0–MA8, $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$, $\overline{CAS0}$, and $\overline{CAS1}$ go into a HIGH impedance (floating) state.
CLK	41	System Clock—This input provides the master timing to generate refresh cycle timings and refresh rate. Refresh rate is determined by the TWST, FS1, FS0 inputs.
$\overline{REFREQ}$	31	Refresh Request—(This input is driven by an open-collector output.) On input, a LOW-going edge initiates a refresh cycle and will cause the internal refresh timer to be reset on the next falling edge of the CLK. As an output, a LOW-going edge signals an internal refresh request and that the refresh timer will be reset on the next LOW-going edge of CLK. $\overline{REFREQ}$ will remain LOW until the refresh cycle is in progress and the current refresh address is present on MA0–MA8. (Note: $\overline{REFREQ}$ contains an internal pull-up resistor with a nominal resistance of 10 kilohms.)
$\overline{RAS0}$, $\overline{RAS1}$ $\overline{RAS2}$, $\overline{RAS3}$	46, 47 39, 40	Row Address Strobe—These three-state outputs are used to latch the row address into the bank of DRAMs selected by REN1 and REN2. On refresh, all $\overline{RAS}$ signals are active.
$\overline{CAS0}$, $\overline{CAS1}$	2, 38	Column Address Strobe—these three-state outputs are used to latch the column address into the DRAM array.
RDY	42	Ready—This totem-pole output synchronizes memories that are too slow to guarantee microprocessor access time requirements. This output is also used to inhibit access cycles during refresh when in cycle-steal mode.
TWST	30	Timing/Wait Strap—A HIGH on this input indicates a wait state should be added to each memory cycle. In addition it is used in conjunction with FS0 and FS1 to determine refresh rate and timing.
FS0, FS1	29, 28	Frequency Select 0; Frequency Select 1—These are strap inputs to select Mode and Frequency of operation as shown in Table 1.
$\overline{RESET}$	(PLCC only)	$\overline{RESET}$—Active LOW input to initialize the controller asynchronously. Refresh Address is set to 1FFH, internal refresh requests, synchronizer, and frequency divider are cleared. This input is driven by an open collector driver. $\overline{RESET}$ contains an internal pull-up with a nominal resistance of 100 KΩ. This allows the pin to be left open, if desired.

Note:
1. Pin numbers are for dual in-line package only.

TABLE 1: STRAP CONFIGURATION

Strap Input Modes, Note 1			Memory Access Wait States	Refresh Rate, Note 2	Refresh Clock Cycles
TWST	FS1	FSO			
L	L	L(3)	0	External	4
L	L	H	0	External	3
L	H	L	0	Clk÷61	3
L	H	H	0	Clk÷91	4
H	L	L	1	Clk÷61	3
H	L	H	1	Clk÷91	4
H	H	L	1	Clk÷106	4
H	H	H	1	Clk÷121	4

TABLE 2: OUTPUT STROBE SELECTION

Control	Input	Selected Output					
REN2	REN1	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS0}$	$\overline{CAS1}$
0	0	X				X	
0	1		X			X	
1	0			X			X
1	1				X		X

Notes:
1. If the strap configuration is changed, the device should be reset in order to insure normal refresh operation.
2. The maximum refresh rate is a function of the applicable maximum clock frequency (see AC Characteristics).
3. This strap configuration resets the refresh timer circuitry.

FUNCTIONAL DESCRIPTION

VL4502 consists of six basic blocks; address and select latches, refresh rate generator, refresh counter, the multiplexer, the arbiter, and the timing and control block.

ADDRESS AND SELECT LATCHES

The address and select latches allow the DRAM controller to be used in systems that multiplex address and data on the same lines without external latches. The row address latches are transparent, meaning that while ALE is HIGH, the output at MA0–MA8 follows the inputs RA0–RA8.

REFRESH RATE GENERATOR

The refresh rate generator is a counter that indicates to the arbiter that it is time for a refresh cycle. The counter divides the clock frequency according to the configuration straps as shown in Table 1. The counter is reset when a refresh cycle is requested or when TWST, FS1 and FS0 are LOW. The configuration straps allow the matching of memories to the system access time. Upon Power-Up, a reset may be accomplished by driving all three strap inputs LOW, or by driving $\overline{RESET}$ LOW. During this reset period, at least four clock cycles should occur. (See RESET, below.)

REFRESH COUNTER

The refresh counter contains the address of the row to be refreshed. The counter is decremented after each refresh cycle. (A LOW-to-HIGH transition on TWST sets the refresh counter to $1FF_{16}$ (511_{10}).

MULTIPLEXER

The multiplexer provides the DRAM array with row, column, and refresh addresses at the proper times. Its inputs are the address latches and the refresh counter. The outputs provide up to 18 multiplexed addresses on nine lines.

STATIC OPERATION

The VL4502 is designed for static operation. As a result, the user can use a CLK frequency as low as needed, as long as maximum transition times are not exceeded. As the CLK rate is changed, the refresh rate will change accordingly, in keeping with the frequency-divider specifications above.

ARBITER

The arbiter provides two operational cycles; access and refresh. The arbiter resolves conflicts between cycle requests and cycles in execution, and schedules the inhibited cycle when used in cycle-steal mode.

TIMING AND CONTROL BLOCK

The timing and control block executes the operational cycle at the request of the arbiter. It provides the DRAM array with $\overline{RAS}$ and $\overline{CAS}$ signals. It provides the CPU with a RDY signal. It controls the multiplexer during all cycles. It resets the refresh rate generator and decrements the refresh counter during refresh cycles.

RESET

The VL4502 is reset by bringing the timing straps TWST, FS1, and FS0 LOW. The refresh address is set to 1FF, internal refresh requests are synchronized, and the frequency divider is cleared. This reset can occur asynchronously with respect to CLK and control signals. In the PLCC package, the VL4502 can be reset with the $\overline{RESET}$ signal. In either case, at least four clock cycles should occur during the reset period.

ABSOLUTE MAXIMUM RATINGS

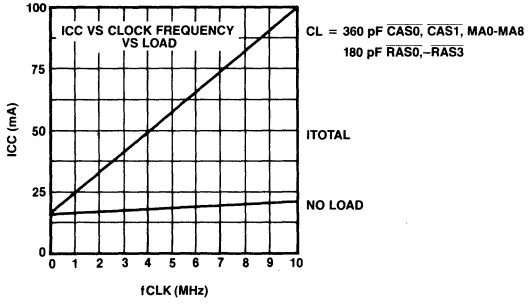
Ambient Temperature Under Bias −10°C to +80°C
Storage Temperature Range −65°C to +140°C
Supply Voltage Range, VCC, Note 1 −0.5 to +7.0 V
Input Voltage Range (any input), Note 1 −0.5 to +7.0 V
Continuous Power Dissipation 1.2 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±10%

Symbol	Parameter		Min	Typ(3)	Max	Unit	Conditions	
VIH	Input HIGH Voltage		2.4			V		
VIL (except $\overline{\text{REFREQ}}$)	Input LOW Voltage		VSS − 0.5		0.8	V		
VIL ($\overline{\text{REFREQ}}$)	Input LOW Voltage		VSS − 0.5		1.2	V		
VOH	Output HIGH Voltage	MA0–MA8 RDY	2.4			V	IOH = −1 mA	VCC = 4.5 V
		RASX, CASX	2.7					
		$\overline{\text{REFREQ}}$	2.4				IOH = −100 µA	VCC = 4.5 V
VOL	Output LOW Voltage				0.4	V	IOL = 4 mA	VCC = 4.5 V
IIH	Input HIGH Current	$\overline{\text{REFREQ}}$			100	µA	VI = 5.5 V	
		All Others			10			
IIL	Input LOW Current	$\overline{\text{REFREQ}}$, $\overline{\text{RESET}}$			−1.25	mA	VI = 0 V	
		All others			−10	µA		
IOZ	Off-state Output Current				±50	µA	VO = 0 to 4.5 V	VCC = 5.5 V
ICC(4)	Operating Supply Current DC				20	mA	TA = 0°C	VCC = 5.5 V
CI	Input Capacitance			5		pF	VI = 0 V	f = 1 MHz
CO	Output Capacitance			6		pF	VO = 0V	f = 1 MHz

GRAPH 1



Notes:
1. Voltage values are with respect to the ground terminal.
2. The algebraic convention, where the more negative limit is designated as minimum, is used in this data sheet for logic voltage levels only.
3. All typical values are at VCC = 5 V, TA = 25°C except where otherwise noted.
4. Refer to Graph 1 for AC Power Consumption Guarantee. In testing, all inputs except CLK are held LOW.

AC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ± 10%

Symbol	Parameter	VL4502-15		VL4502-20		Unit
		Min	Max	Min	Max	
tC(C)	CLK Cycle Time	100		100		ns
tW(CH)	CLK HIGH Pulse Width	25		25		
tW(CL)	CLK LOW Pulse Width	35		35		
tt	Transition Time, All Inputs		30		30	
tAEL-CL	Time Delay, ALE LOW to CLK Starting LOW, Note 1	10		10		
tCL-AEL	Time Delay, CLK LOW to ALE Starting LOW, Note 1	10		10		
tCL-AEH	Time Delay, CLK LOW to ALE Starting HIGH, Note 1	15		20		
tW(AEH)	Pulse Width ALE HIGH	50		60		
tAV-AEL	Time Delay, Address, $\overline{REN}_{1,2}$ $\overline{CS}$ Valid to ALE LOW	5		10		
tAEL-AX	Time Delay, ALE LOW to Address Not Valid	10		10		
tAEL-ACL	Time Delay, ALE LOW to $\overline{ACX}$ LOW, Notes 3, 4, 5, 6	th(RA) + 30		th(RA) + 40		
tACH-CL	Time Delay, $\overline{ACX}$ HIGH to CLK LOW, Notes 3, 7	20		20		
tACL-CH	Time Delay, $\overline{ACX}$ LOW to CLK Starting HIGH (to remove RDY)	40		40		
tRQL-CL	Time Delay, $\overline{REFREQ}$ LOW to CLK Starting LOW, Note 8	35		35		
tW(RQL)	Input Pulse Width, $\overline{REFREQ}$ LOW	20		20		

Notes:

1. Coincidence of the trailing edge of CLK and the trailing edge of ALE should be avoided as the refresh/access occurs during the interval from $\overline{ACX}$ HIGH to ALE LOW.
2. If ALE rises before $\overline{ACX}$ and a refresh request is present, the falling edge of CLK after tCL-AEH will output the refresh address to MA0–MA8 and initiate a refresh cycle.
3. These specifications relate to system timing and do not directly reflect device performance.
4. On the access grant cycle following refresh, the occurrence of $\overline{CAS}$ LOW depends on the relative occurrence of ALE LOW to $\overline{ACX}$ LOW. If $\overline{ACX}$ occurs prior to or coincident with ALE then $\overline{CAS}$ is timed from the CLK HIGH transition that causes RAS LOW. If ACX occurs 20 ns or more after ALE then $\overline{CAS}$ is timed from the CLK LOW transition following the CLK HIGH transition causing RAS LOW.
5. For maximum speed access (internal delays on both access and access grant cycles), $\overline{ACX}$ should occur prior to or coincident with ALE.
6. th(RA) is the dynamic memory row address hold time. $\overline{ACX}$ should follow ALE by tAEL-CEL in systems where the required th(RA) is greater than tREL-MAX minimum.
7. Minimum of 20 ns is specified to ensure arbitration will occur on falling CLK edge. tACH-CL also affects precharge time such that the minimum tACH-CL should be equal or greater than: tW(RH) – tW(CL) + 30 ns (for cycle where $\overline{ACX}$ HIGH occurs prior to ALE HIGH) where tW(RH) is the DRAM $\overline{RAS}$ precharge time.
8. This parameter is necessary only if refresh arbitration is to occur on this LOW-going CLK edge (in systems where refresh is synchronized to external events).

AC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ± 10%

Symbol	Parameter	VL4502-15		VL4502-20		Unit
		Min	Max	Min	Max	
tAEL-REL	Time Delay, ALE LOW to $\overline{RAS}$ Starting LOW		30		40	
tt(REL)	$\overline{RAS}$ Fall Time		15		20	
tRAV-MAV	Time Delay, Row Address Valid to Memory Address Valid		45		50	
tAEH-MAV	Time Delay, ALE HIGH to Valid Memory Address		55		70	
tAEL-RYL	Time Delay, ALE to $\overline{RDY}$ Starting LOW (TWST = 1 or Refresh in Progress)		25		25	
tAEL-CEL	Time Delay, ALE LOW to $\overline{CAS}$ Starting LOW	60	150	70	200	
tAEH-REH	Time Delay, ALE HIGH to $\overline{RAS}$ Starting HIGH		35		35	
tt(MAV)	Address Transition Time		15		20	
tACL-MAX	Row Address Hold from $\overline{ACX}$ LOW	15		20		
tMAV-CEL	Time Delay, Memory Address Valid to $\overline{CAS}$ Starting LOW	0		0		
tt(CEL)	$\overline{CAS}$ Fall Time		15		20	
tACL-CEL	Time Delay, $\overline{ACX}$ LOW to $\overline{CAS}$ Starting LOW	50	90	65	130	
tACH-REH	Time Delay, $\overline{ACX}$ to $\overline{RAS}$ Starting HIGH		40		40	
tt(REH)	$\overline{RAS}$ Rise Time		15		20	
tACH-CEH	Time Delay, $\overline{ACX}$ HIGH to $\overline{CAS}$ Starting HIGH	5	35	10	40	ns
tt(CEH)	$\overline{CAS}$ Rise Time		30		35	
tACH-MAX	Column Address Hold from $\overline{ACX}$ HIGH	15		20		
tCH-RYH	Time Delay, CLK HIGH to RDY Starting HIGH (After $\overline{ACX}$ LOW), Note 9		35		45	
tRFL-RFL	Time Delay, $\overline{REFREQ}$ External Until Supported by $\overline{REFREQ}$ Internal		25		30	
tCH-RFL	Time Delay, CLK HIGH Until $\overline{REFREQ}$ Internal Starting LOW		30		35	
tCL-MAV	Time Delay, CLK LOW Until Refresh Address Valid		75		100	
tCH-RRL	Time Delay, CLK HIGH Until Refresh $\overline{RAS}$ Starting LOW	10	50	15	60	
tMAV-RRL	Time Delay, Refresh Address Valid Until Refresh $\overline{RAS}$ LOW	0		0		
tCL-RFH	Time Delay, CLK LOW to $\overline{REFREQ}$ Starting HIGH (3 Cycle Refresh)		50		55	
tCH-RFH	Time Delay, CLK HIGH to $\overline{REFREQ}$ Starting HIGH (4 Cycle Refresh)		45		55	
tCH-RRH	Time Delay, CLK HIGH to Refresh $\overline{RAS}$ Starting HIGH	5	40	10	45	
tCH-MAX	Time Delay, Refresh Address Hold After CLK HIGH	15		20		

Note:

9. RDY returns HIGH on the rising edge of CLK. If TWST = 0, then on an access grant cycle RDY goes HIGH on the same edge that causes access $\overline{RAS}$ LOW. If TWST = 1, then RDY goes to the HIGH level on the first rising CLK edge after $\overline{ACX}$ goes LOW on access cycles and on the next rising edge after the edge that causes access $\overline{RAS}$ LOW on access grant cycles (assuming $\overline{ACX}$ LOW).

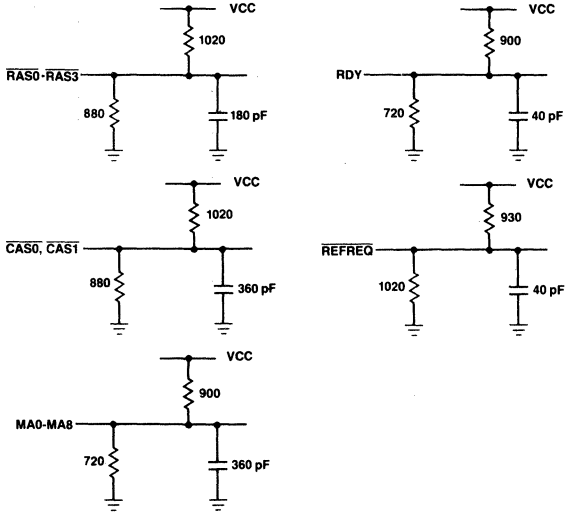
AC CHARACTERISTICS: T_A = 0°C to +70°C, V_{CC} = 5 V ± 10%

Symbol	Parameter	VL4502-15		VL4502-20		Unit
		Min	Max	Min	Max	
tCH-REL	Time Delay, CLK HIGH Until Access $\overline{RAS}$ Starting LOW		60		70	ns
tCL-CEL	Time Delay, CLK LOW to Access $\overline{CAS}$ Starting LOW, Note 10		125		140	
tCL-MAX	Row Address Hold After CLK LOW	25		30		
tW(ACL)	$\overline{ACX}$ LOW Width	95		120		
tREL-MAX	Row Address Hold From $\overline{RAS}$ LOW	25		30		
tt(RYL)	RDY Fall Time		10		15	
tt(RYH)	RDY Rise Time		20		25	
tdis	Output Disable time (3-State Outputs)		100		125	
tAEH-MAX	Column Address Hold From ALE HIGH	10		15		
ten	Output Enable Time (3-State Outputs)		65		80	
tCAV-CEL	Column Address Setup to $\overline{CAS}$ After Refresh	0		0		
tCH-CEL	Time Delay, CLK HIGH to Access $\overline{CAS}$ Starting LOW, Note 9		140		180	
t$\overline{RESET}$	Power Up RESET	Four (4) Clock Cycles				

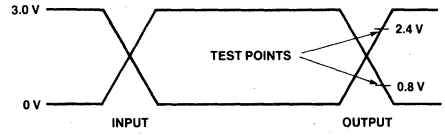
Notes:

10. On the access grant cycle following refresh, the occurrence of $\overline{CAS}$ LOW depends on the relative occurrrence of ALE LOW to ACX LOW. If ACX occurs prior to or coincident with ALE then $\overline{CAS}$ is timed from the CLK LOW transition that causes $\overline{RAS}$ LOW. If $\overline{ACX}$ occurs 20 ns or more after ALE then $\overline{CAS}$ is timed from the CLK LOW transition following the CLK HIGH transition causing $\overline{RAS}$ LOW.

OUTPUT LOAD CONDITIONS: V_{CC} = 5.0 V



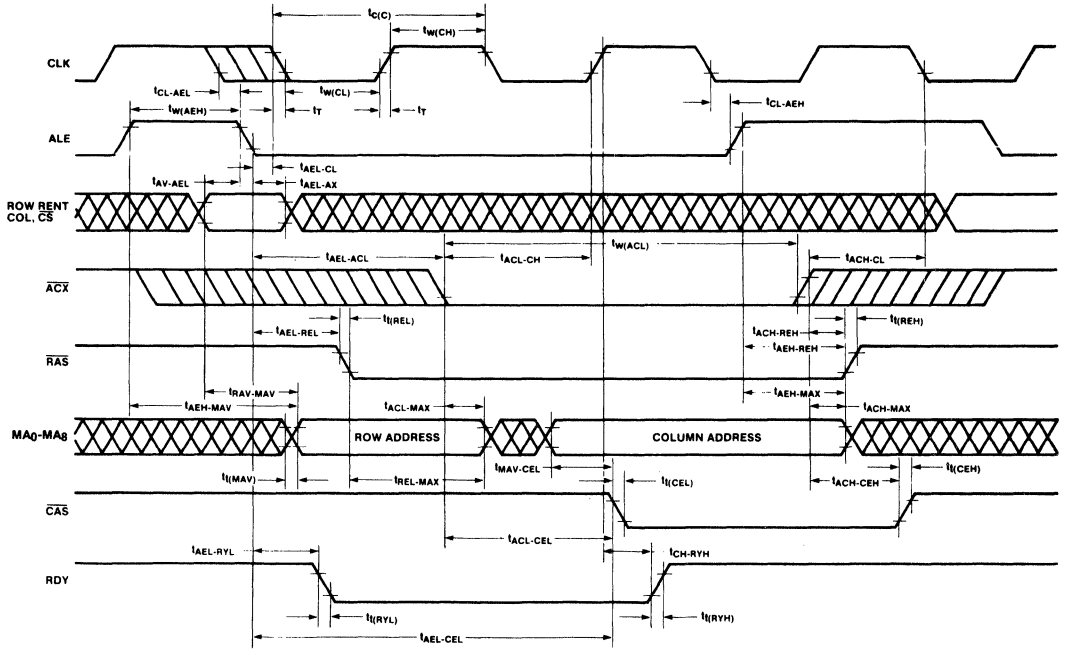
AC TESTING INPUT, OUTPUT WAVEFORM



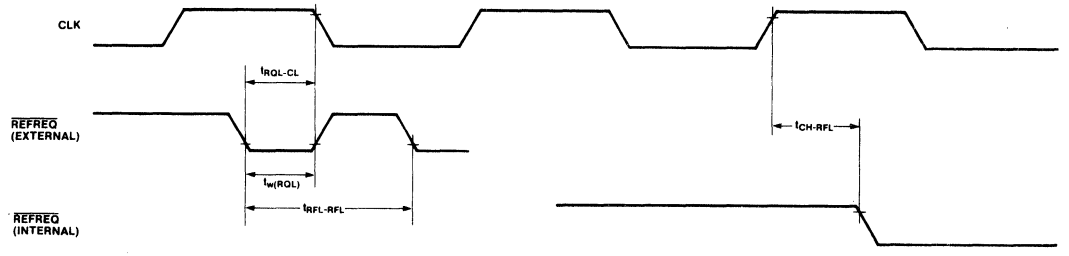
AC TESTING INPUTS ARE DRIVEN AT 3.0 V FOR A LOGIC "1" AND 0.0 V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.4 V FOR A LOGIC "1" AND 0.8 V FOR A LOGIC "0" AT THE OUTPUTS.

TIMING DIAGRAMS

ACCESS CYCLE TIMING

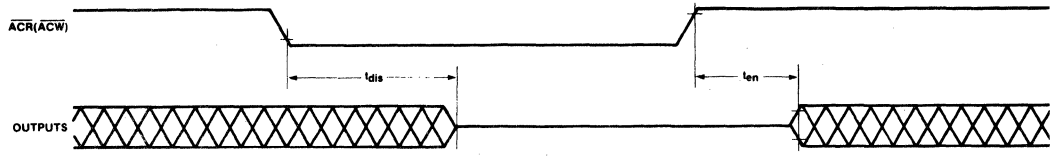


REFRESH REQUEST TIMING

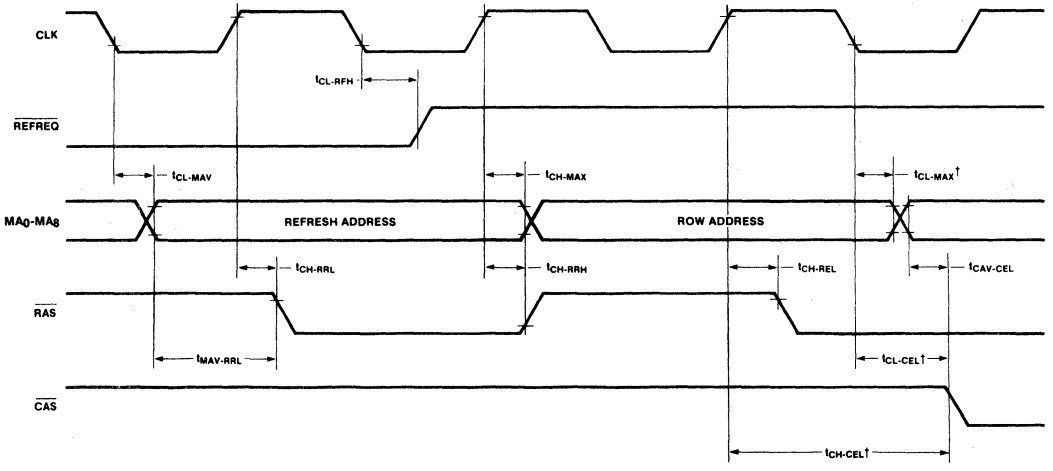


TIMING DIAGRAMS (Cont.)

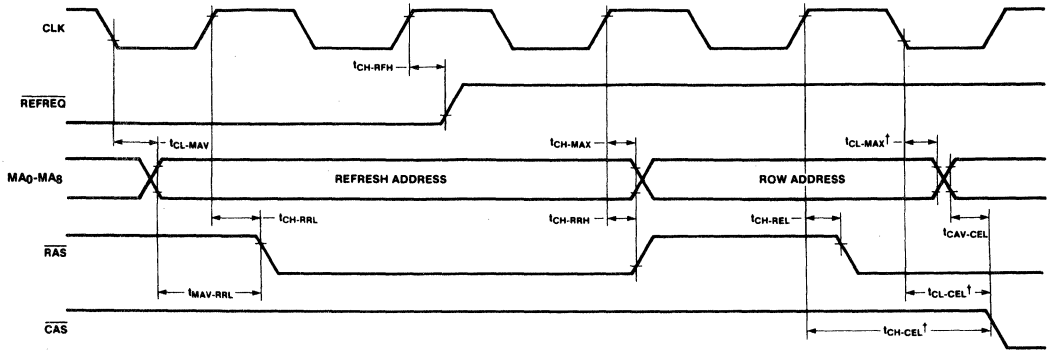
OUTPUT 3-STATE TIMING



REFRESH CYCLE TIMING (3-CYCLE)



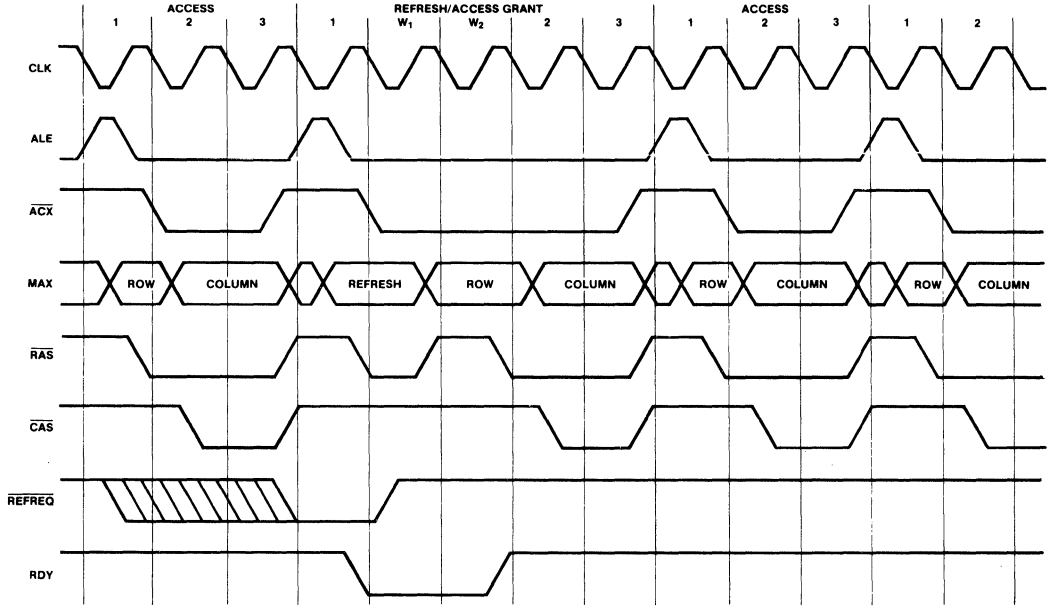
REFRESH CYCLE TIMING (4-CYCLE)



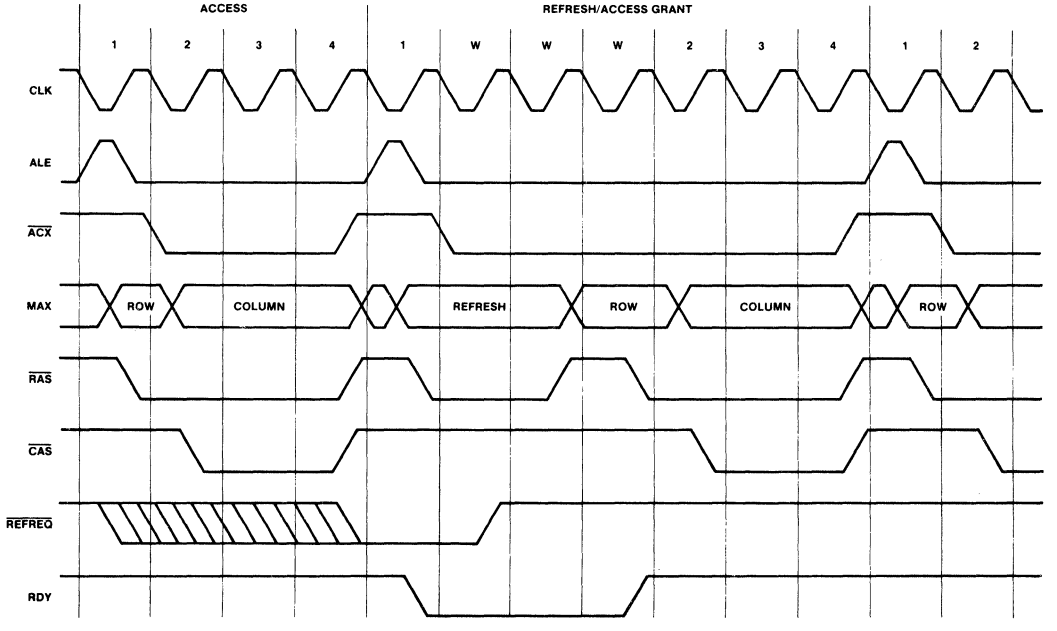
ON THE ACCESS GRANT CYCLE FOLLOWING REFRESH, THE OCCURRENCE OF $\overline{CAS}$ LOW DEPENDS ON THE RELATIVE OCCURRENCE OF ALE LOW TO $\overline{ACX}$ LOW. IF $\overline{ACX}$ OCCURS PRIOR TO OR COINCIDENT WITH ALE THEN $\overline{CAS}$ IS TIMED FROM THE CLK HIGH TRANSITION THAT CAUSES $\overline{RAS}$ LOW. IF $\overline{ACX}$ OCCURS 20 NS OR MORE AFTER ALE THEN $\overline{CAS}$ IS TIMED FROM THE CLK LOW TRANSITION FOLLOWING THE CLK HIGH TRANSITION CAUSING $\overline{RAS}$ LOW.

TIMING DIAGRAMS (Cont.)

TYPICAL ACCESS/REFRESH/ACCESS CYCLE (3-CYCLE, TWST = 0)

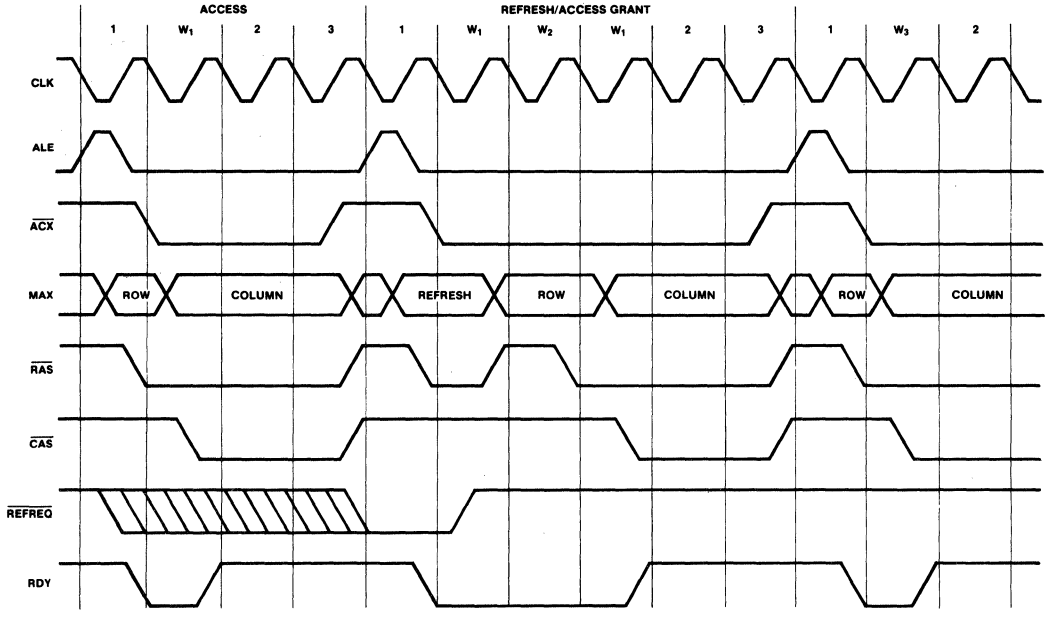


TYPICAL ACCESS/REFRESH/ACCESS CYCLE (4-CYCLE, TWST = 0)

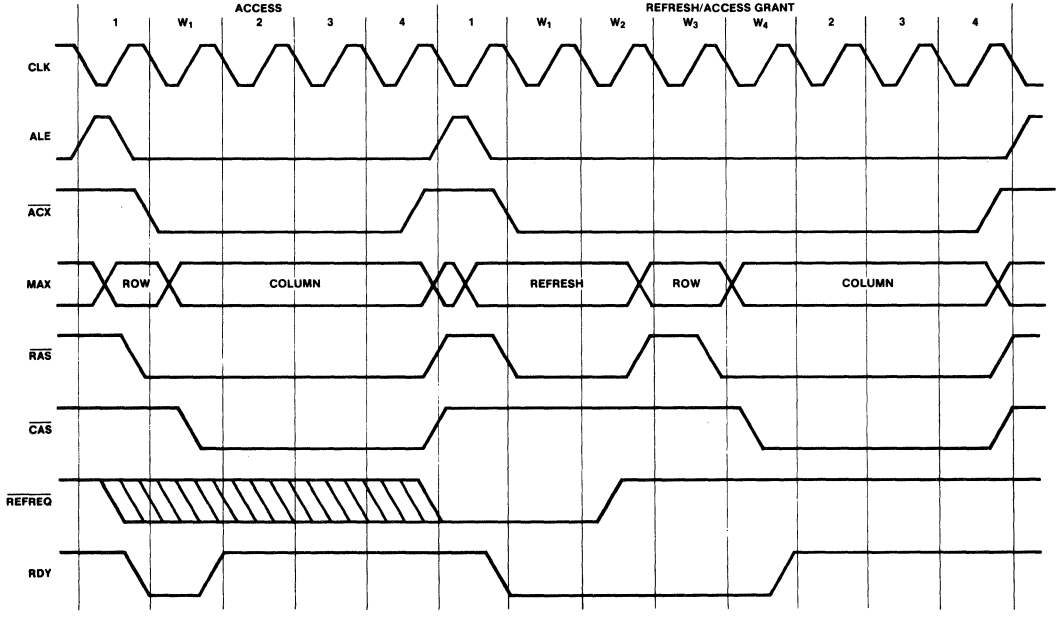


TIMING DIAGRAMS (Cont.)

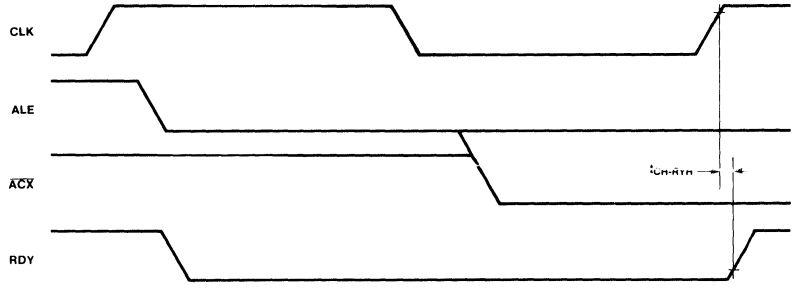
TYPICAL ACCESS/REFRESH/ACCESS CYCLE (3-CYCLE, TWST = 1)



TYPICAL ACCESS/REFRESH/ACCESS CYCLE (4-CYCLE, TWST = 1)



READY (RDY) SIGNAL TIMING (WAIT STATE OPERATION, TWST = 1)



RDY starting HIGH is timed from CLK HIGH (t_{CH-RYH})

VL6522•VL65C22

PARALLEL INTERFACE/TIMER

FEATURES

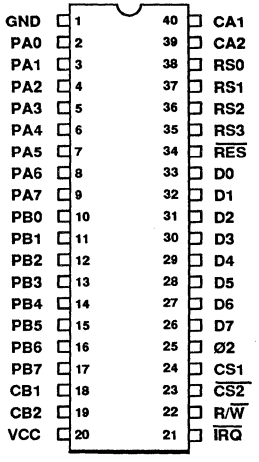
- Low power consuming CMOS Parallel Interface/Timer (VL65C22)
- Low cost HMOS Parallel Interface/Timer (VL6522)
- Two 8-bit bidirectional I/O ports
- Two 16-bit timer/counters
- Serial bidirectional peripheral I/O port
- Enhanced handshake features
- Programmable data direction registers
- TTL-compatible I/O peripheral lines

DESCRIPTION

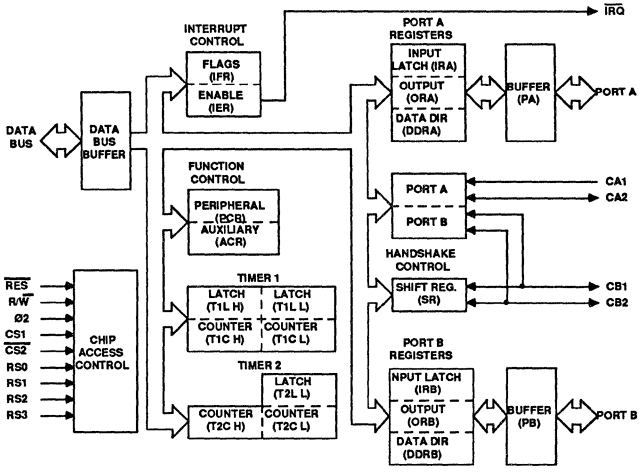
The VL6522/VL65C22 are flexible I/O devices for use with the 65XX family of processors. The VL65C22 is a CMOS implementation of the VL6522 device. Both include functions for programmed control of up to two peripheral devices (ports A and B). Two program-controlled 8-bit bidirectional peripheral I/O ports allow direct interfacing between the microprocessor and selected peripheral devices. Two programmable Data Direction Registers (A and B) allow selection of data direction (input versus output) on an individual line-by-line basis. Also provided are two programmable 16-bit counter/timers with latches. Timer 1 may be operated in a one-shot interrupt mode with interrupts on each count-to-zero, or in a free-running mode with a series of evenly spaced interrupts. Timer 2 functions both as an interval and pulse counter. Serial data transfers are provided by a shift register. Application versatility is further increased by various control registers, including an interrupt flag register, an interrupt enable register, and two function control registers.

PIN DIAGRAM

VL6522
VL65C22



BLOCK DIAGRAM



ORDER INFORMATION

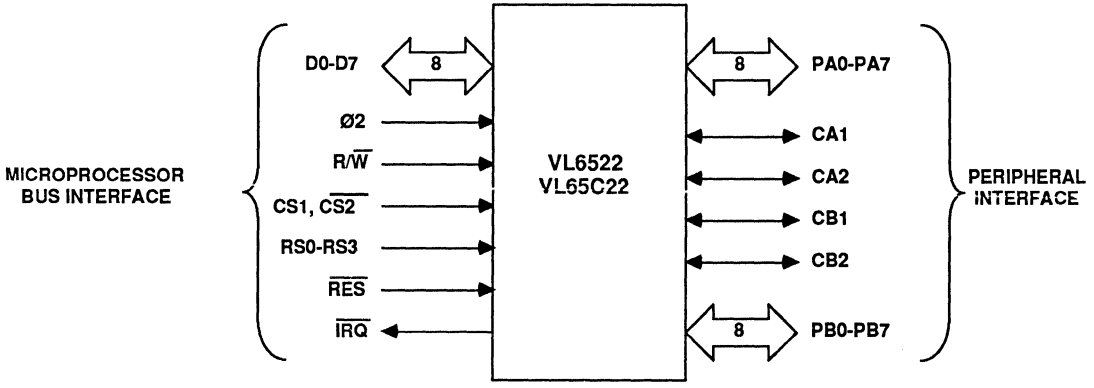
Part Number	Technology	Clock Frequency	Package
VL6522-01PC	HMOS	1 MHz	Plastic DIP
VL6522-01QC	CMOS		Plastic DIP
VL65C22-01PC	HMOS		Plastic Leaded Chip Carrier
VL65C22-01QC	CMOS		Plastic Leaded Chip Carrier
VL6522-02PC	HMOS	2 MHz	Plastic DIP
VL6522-02QC	CMOS		Plastic DIP
VL65C22-02PC	HMOS		Plastic Leaded Chip Carrier
VL65C22-02QC	CMOS		Plastic Leaded Chip Carrier
VL65C22-03PC	CMOS	3 MHz	Plastic DIP
VL65C22-03QC	CMOS		Plastic Leaded Chip Carrier
VL65C22-04PC	CMOS	4 MHz	Plastic DIP
VL65C22-04QC	CMOS		Plastic Leaded Chip Carrier

Note: Operating temperature range: 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
$\overline{RES}$	34	The LOW input reset clears all VL65(C)22 internal registers to logic 0 (except T1 and T2 latches and counters and the shift register). This places all peripheral interface lines in the input state, disables the timers, shift register, etc., and disables interrupting from the chip.
Ø2	25	The input clock is the system Ø2 clock, which triggers all data transfers between the processor bus and the VL65(C)22.
R/$\overline{W}$	22	The direction of the data transfers between the VL65(C)22 and the system processor is controlled by the R/$\overline{W}$ line in conjunction with the CS1 and $\overline{CS2}$ inputs. When R/W is LOW (write operation) and the VL65(C)22 is selected, data is transferred from the processor bus into the selected VL65(C)22 register. When R/W is HIGH (read operation) and the chip is selected, data is transferred from the selected VL65(C)22 register to the CPU.
D0-D7	33-26	The eight bidirectional data bus lines transfer data between the VL65(C)22 and the system processor bus. During read cycles, the contents of the selected VL65(C)22 register is placed on the data bus lines. During write cycles, these lines are high-impedance inputs and data is transferred from the processor bus into the selected register. When the VL65(C)22 is not selected, the data bus lines are high-impedance.
CS1, $\overline{CS2}$	24, 23	The two chip select inputs are normally connected to processor address lines either directly or through decoding. The selected VL65(C)22 register is accessed when CS1 is HIGH and $\overline{CS2}$ is LOW.
RS0, RS1, RS2, RS3	38 - 35	The coding of the four register select inputs selects one of the 16 internal registers of the VL65(C)22, as shown in Table 2.
$\overline{IRQ}$	21	The interrupt request output goes LOW whenever an internal interrupt flag is set and the corresponding interrupt enable bit is a logic 1. This is an open-drain output, which allows the interrupt request signal to be in a wire-OR logic state with other equivalent signals in the system.
PA0 - PA7	2 - 9	Port A consists of eight lines that can be individually programmed to act as inputs or outputs under control of data direction register A. The polarity of output pins is controlled by an output register and input data may be latched into an internal register under control of the CA1 line. All of these modes of operation are controlled by the system processor through the internal control registers. These lines, represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode.
PB0 - PB7	10 - 17	Peripheral data port B is an 8-line, bidirectional bus that is controlled by an output register, input register and data direction register in a manner much the same as data port A. With respect to port B, the output signal on line PB7 may be controlled by Timer 1, while Timer 2 may be programmed to count pulses on line PB6. Port B lines are also capable of sourcing 3.0 mA at 1.5 Vdc in the output mode. This allows the outputs to directly drive Darlington transistor circuits.
CA1, CA2	40, 39	Control lines CA1 and CA2 serve as interrupt inputs or handshake outputs for peripheral data port A. Each line controls an internal interrupt flag with a corresponding interrupt enable bit. CA1 also controls the latching of input data on port A. CA1 is a high-impedance input, while CA2 represents one standard TTL load in the input mode. In the output mode, CA2 will drive one standard TTL load.
CB1, CB2	18, 19	Control lines CB1 and CB2 serve as interrupt inputs or handshake outputs for peripheral data port B. Like port A, these two control lines control an internal interrupt flag with a corresponding interrupt enable bit. These lines also serve as a serial data port under control of the shift register (SR). Each control line represents one standard TTL load in the input mode and can drive one TTL load in the output mode. Note that CB1 and CB2 cannot drive Darlington transistor circuits.
VCC	20	+5 V
GND	1	Ground

FIGURE 1. MICROPROCESSOR AND PERIPHERAL INTERFACE



FUNCTIONAL DESCRIPTION

PERIPHERAL DATA PORTS (PORT A, PORT B)

Each peripheral data port operates in conjunction with a data direction register (DDRA or DDRB). Under program control, the data direction registers specify which lines within the port bus are to be designated as inputs or outputs. A logic 0 in any bit position of the register will cause the corresponding line to serve as an input, while a logic 1 will cause the line to serve as an output.

When a line is programmed as an output, it is controlled by a corresponding bit in the output register (ORA or ORB). A logic 1 in the output register will cause the corresponding output line to go HIGH, while a Logic 0 will cause the line to go LOW. Under program control, data is written into the Output Register bit positions corresponding to the output lines that have been programmed as outputs. Should data be written into bit positions corresponding to lines that have been programmed as inputs, the output lines will be unaffected.

When reading a peripheral data port, the contents of the corresponding Input register (IRA or IRB) are transferred onto the data bus. When the input latching feature is disabled, input register A (IRA) will reflect the logic levels present on the port A bus lines. However, with input latching enabled and the selected active transition on CA1 having occurred, input register A will contain the data present on the port A bus lines at the time of the transition. In this case, once input register A has been read, it will appear transparent, reflecting the current state of the port A bus lines until the next CA1 latching transition.

Input register B operates similar to input register A except that for those port B bus lines that have been programmed as outputs. When reading input register A, the logic level on the bus line determines whether a logic 1 or 0 is sensed. However, when reading input register B, the logic level stored in output register B (ORB) is the logic level sensed. For this reason, those outputs that have large loading effects may cause the reading of input register A to result in the reading of logic 0 when a 1 was actually programmed, and reading a logic 1 when a 0 was programmed. However, when reading input register B, the logic level read will be correct, regardless of loading on the particular bus line.

For information on formats and operation of the peripheral data port registers, refer to Figures 14, 15, 16, and 17. It should be noted that the input latching modes are controlled by the auxiliary control register.

DATA TRANSFER - HANDSHAKE CONTROL

A powerful feature of the VL65(C)22 is its ability to provide absolute control over data transfers between the microprocessor and peripheral devices. This control is accomplished by way of handshake lines. Port A lines (CA1, CA2) handshake data transfers on both read and write operations, while port B lines (CB1, CB2) handshake data on write operations only.

READ HANDSHAKE CONTROL

Read handshaking provides effective control of data transfers from a peripheral device to the microprocessor. To accomplish the read handshake, the peripheral device generates a data ready signal to the VL65(C)22 that indicates valid data is present on the peripheral data port bus. In most cases, this data ready signal will interrupt the microprocessor, which will then read the data and generate a data taken signal. Once the peripheral senses the data taken signal, new data will be placed on the bus. This process continues until the data transfer is complete.

Automatic read handshaking applies to peripheral data port A only. The data ready signal is transmitted by the peripheral device over the CA1 interrupt line, while the data taken signal is generated and transmitted to the peripheral device over the CA2 line. When the data ready signal is received, it sets an internal flag in the interrupt flag register (IFR). This flag may interrupt the microprocessor or it may be polled under program control. As an

option, the data taken signal may be either a pulse or a level. In either case, it is set LOW (logic 0) by the microprocessor and is cleared by the next data ready signal. Refer to Figures 3 and 4 for read handshake timing and operating sequence.

WRITE HANDSHAKE CONTROL

The write handshake operation is similar to read handshaking. For write handshaking, however, the VL65(C)22 generates the data ready signal and the peripheral device must generate the data taken return signal. Note that write handshaking may occur on both data ports (A and B). For a write handshake, CA2 or CB2 serve as the data ready output and can operate in either the handshake mode or the pulse mode. The data taken signal is received by CA1 or CB1. The data taken signal sets a flag in the interrupt flag register and clears the data ready output signal. Note that the selection of read or write handshake operating modes (CA1, CA2, CB1, and CB2) is accomplished by the peripheral control register (PCR).

INTERRUPT OPERATION

There are three basic operations: setting the flag within the interrupt flag register (IFR), enabling the interrupt by way of a corresponding bit in the interrupt enable register (IER), and signaling the microprocessor with an interrupt request (IRQ). An interrupt flag can be set by conditions internal to the chip or by inputs to the chip from external sources. Normally, an interrupt flag remains set until the interrupt is serviced. To determine the source of an interrupt, the micro-processor must examine each flag in order, from highest to lowest priority. This is accomplished by reading the contents of the interrupt flag register into the microprocessor accumulator, shifting the contents either left or right, and then using conditional branch instructions to detect an active interrupt. Each interrupt flag has a corresponding interrupt enable bit in the interrupt enable register. The enable bits are controlled by the microprocessor (set or reset). If an interrupt flag is HIGH (logic 1), and the corresponding interrupt enable bit is HIGH (logic 1), the interrupt request (IRQ) will go LOW (logic 0). IRQ is an open-collector output that can be in a wire-OR logic state with other devices within the system.

All interrupt flags are contained within a single interrupt flag register. Bit 7 of this register will be HIGH (logic 1) whenever an interrupt flag is set, thus allowing convenient polling of several devices within a system to determine the source of the interrupt.

The interrupt flag register (IFR) and interrupt enable register (IER) format and operation is shown in Figures 28 and 29, respectively. The interrupt flag register may be read directly by the micrprocessor, and individual flag bits may be cleared by writing a 1 into the appropriate bit of the IFR. Bit 7 of the IFR indicates the status of the interrupt request (IRQ) output. Bit 7 corresponds to the following logic function: IRQ = IFR6 x IER6 + IFR5 x IER5 + IFR4 x IER4 + IFR3 x IER3 + IFR2 x IER2 + IFR1 x IER1 + IFR0 x IER0. Note x = Logic-AND, + = Logic-OR.

Bit 7 is not a flag. For this reason, bit 7 is not directly cleared by writing a "1" into its bit position. It can be cleared, however, by clearing all the flags within the register, or by disabling all active interrupts as presented in the next section.

TIMER OPERATION

Timer 1 Operation - Interval timer T1 consists of two 8-bit latches and a 16-bit counter. The latches serve to store data that is to be loaded into the counter. Once the counter is loaded under program control, it decrements at a phase 2 (Ø2) clock rate. Upon reaching zero, an interrupt flag is set, causing interrupt request (IRQ) to go LOW (logic 0), if the corresponding interrupt enable bit is set. Once the timer reaches a count of zero, it will either disable any further interrupts (provided it has been programmed to do so), or it will automatically transfer the contents of the latches into the counter and proceed to decrement again. The counter may also be programmed to invert the output signal on PB7 each time it reaches a count of zero. Additional control bits are provided in the auxiliary control register (bits 6 and 7) to allow selection of timer 1 operating modes.

It should be noted that the microprocessor does not write directly into the low-order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low-order register when the microprocessor writes into the high-order register and counter. In fact, it may not be necessary to write to the low-order register in some applications, since the timing operation is triggered by writing to the high-order register and counter.

Timer 1 One-Shot Mode - Interval timer T1 may operate in the one-shot mode which allows the generation of a single interrupt flag each time the timer is loaded. The timer can also be programmed to produce a single negative pulse on data port line PB7.

To generate a single interrupt, it is required that bits 6 and 7 of the auxiliary control register be LOW (logic 0). The low-order T1 counter (T1C-L) or the low-order T1 latch (T1L-L) must then be loaded with the low-order count value. Note that a load to T1C-L is effectively a load to T1L-L. Next, the high-order count value must be loaded into the high-order T1 counter (T1C-H), at which time the value is simultaneously loaded into high-order T1 latch (T1L-H). During this load sequence, the contents of T1L-L is transferred to T1C-L. The counter will start counting down on the next Ø2 clock following the load sequence into T1C-H, and will decrement at the Ø2 clock rate. Once the T1 counter reaches a zero count, the interrupt flag is set. To generate a negative pulse on data port line PB7, the sequence is identical to the above except bit 7 of the auxiliary control register must be HIGH (logic 1). Data port line PB7 will then go LOW (logic 0) following the load to T1C-H, and will go HIGH (logic 1) again when the counter reaches a zero count. Once set, the T1 interrupt flag is reset by either loading T1C-H, which starts a new count, or by reading T1C-L.

Timer 1 Free-Run Mode - An important advantage within the VL65C22 is the

ability of the latches associated with the T1 counter to provide a continuous series of evenly spaced interrupts or a square wave on data port line PB7. It should also be noted that the continuous series of interrupts and square waves are not affected by variations in the microprocessor interrupt response time. These advantages are all produced in the free-run mode. When operating in the free-run mode, the interrupt flag is set and the signal on PB7 is inverted each time the counter reaches a count of zero. In the free-run mode, however, the counter does not continue to decrement after reaching a zero count. Instead, the counter automatically transfers the contents of the latch into the counter (16 bits) and then decrements from the new count value. As can be seen, it is not necessary to reload the timer in order to set the interrupt flag on the next count of zero. When set, the interrupt flag can be cleared by either reading T1C-L, by writing directly into the interrupt flag register (IFR), as will be discussed later, or by a load into T1C-H when a new count value is desired.

Since the interval timers are all retriggerable, reloading the counter will always reinitialize the time-out period. Should the microprocessor continue to reload the counter before it reaches zero, counter time-out can be prevented. Timer 1 is able to operate in this manner provided the microprocessor writes into the high-order counter (T1C-H).

By loading the latches only, the microprocessor can access the timer during each count-down operation without affecting the time-out in progress. In this way, data loaded into the latches will determine the length of the next subsequent time-out period. This capability is of value in the free-run mode with the output enabled. In the free-run mode, the signal on data port line PB7 is inverted and the interrupt flag is set with each counter time-out. When the microprocessor responds to the interrupts with new data for the latches, it can determine the period of the next half-cycle during each half-cycle of the output signal on line PB7. In this way, complex waveforms can be generated.

Timer 2 Operation - Timer 2 operates in the one-shot mode only (as an interval timer), or as a pulse counter for counting negative pulses on data port line PB6.

A single control bit within the auxiliary control register is used to select between these two modes. Timer 2 is made up of a write-only low-order latch (T2L-L), a read-only low-order counter (T2C-L), and a read/write high-order counter (T2C-H). This 16-bit counter decrements at a Ø2 clock rate.

Timer 2 One-Shot Mode - Operation of Timer 2 in the one-shot mode is similar to Timer 1. That is, for each load T2C-H operation, Timer 2 sets the interrupt flag for each countdown to zero. However, after a time-out, the T2 counters roll over to all ones (FFF16) and continue to decrement. This twos-complement decrement allows the user to determine how long the T2 interrupt flag has been set. Since the interrupt flag logic is disabled after the initial interrupt set (zero count), further interrupts cannot be set by a subsequent count to zero. To enable the interrupt flag logic, the microprocessor must reload T2C-H. The interrupt flag is cleared by either reading T2C-L or by loading T2C-H.

Timer 2 Pulse Counting Mode - In the pulse counting mode, timer 2 counts a predetermined number of negative-going pulses on data port line PB6. To accomplish this, a count number is loaded into T2C-H, which clears the interrupt flag logic and starts the counter to decrement each time a negative pulse is applied to data port line PB6. When the T2 counter reaches a count of zero, the interrupt flag is set and the counter continues to decrement with each pulse on PB6. To enable the interrupt flag for subsequent countdowns, it is necessary to reload T2C-H. The decrement pulse on line PB6 must be LOW (logic 0) during the leading edge of the Ø2 clock.

SHIFT REGISTER OPERATION AND MODES

Shift Register Operation - The shift register performs bidirectional serial data transfers on line CB2. These transfers are controlled by an internal modulo-8 counter. Shift pulses can be applied to the CB1 line for controlling external devices. Each shift register operating mode is controlled by control bits within the auxiliary control register. Shift Register Input Modes (Shift Register Disabled, 000) - In the 000 mode, the shift register is disabled from all operation. The microprocessor can read or write the shift register, but shifting is disabled and both CB1 and CB2 are controlled by bits in the peripheral control register (PCR). The shift register interrupt flag is held LOW (disabled).

Shift-In (Counter T2 Control, 001) - In this mode, the shifting rate is controlled by the low-order eight bits of counter T2. Shift pulses are generated on the CB1 line to control shifting in external devices. The time between transitions of the CB1 output clock is determined by the Ø2 clock period and the contents of the low-order T2 latch (N). Shifting occurs by writing or reading the shift register. Data is shifted into the low-order bit first, and is then shifted into the next higher order bit on the negative-going edge of each clock pulse. Input data should change before the positive-going edge of the CB1 clock pulse. This data is then shifted into the shift register during the Ø2 clock cycle following the positive-going edge of the CB1 clock pulse. After eight CB1 clock pulses, the shift register interrupt flag will be set and the IRQ will go LOW (logic 0).

Shift In (Ø2 Clock Control, 010) - In this mode, the shift rate is controlled by the Ø2 clock frequency. Shift pulses are generated on the CB1 line to control shifting in external devices. Timer 2 operates as an independent interval timer and has no influence on the shift register. Shifting occurs by reading or writing the shift register. Data is shifted into the low-order bit first, and is then shifted into the next higher order bit on the trailing edge of the Ø2 clock pulse. After eight clock pulses, the shift register interrupt flag will be set and output clock pulses on the CB1 line will stop.

Shift In (External CB1 Clock Control, 011) - In this mode, CB1 serves as an input to the shift register. In this way, an external device can load the shift register at its own pace. The shift register counter will interrupt the microprocessor after each eight bits have been shifted in. The shift register counter does not stop the shifting operation; its function is simply that of a pulse counter. Reading or writing the shift register resets the interrupt flag and initializes the counter to count another eight pulses. Note that data is shifted during the first Ø2 clock cycle following the positive-going edge of the CB1 shift pulse. For this reason, data

must be held stable during the first full cycle following CB1 going high.

Shift Out (Free Running at T2 Rate, 100) - This mode is similar to mode 101 in which the shifting rate is determined by T2. However, in mode 100 the shift register counter does not stop the shifting operation. Since shift register bit 7 (SR7) is recirculated back into bit 0, the eight bits loaded into the Shift Register will be clocked onto the CR2 line repetitively. In this mode, the shift register counter is disabled and IRQ is never set.

Shift Out (T2 Control, 101) - In this mode, the shift rate is controlled by T2 (as in mode 100). However, with each read or write of the shift register, the shift register counter is reset and eight bits are shifted onto the CB2 line. At the same time, eight shift pulses are placed on the CB1 line to control shifting in external devices. After the eight shift pulses, the shifting is disabled, the interrupt flag is set, and CB2 will remain at the last data level.

Shift Out (Ø2 Clock Control, 110) - In this mode, the shift rate is controlled by the system Ø2 clock.

Shift Out (External CB1 Clock Control, 111) - In this mode, shifting is controlled by external pulses applied to the CB1 line. The shift register counter sets the interrupt flag for each eight-pulse count, but does not disable the shifting function. Each time the microprocessor reads or writes to the shift register, the interrupt flag is reset and the counter is initialized to begin counting the next eight pulses on the CB1 line. After eight shift pulses, the interrupt flag is set. The microprocessor can then load the shift register with the next eight bits of data.

TABLE 1. PERIPHERAL INTERFACE CHARACTERISTICS

TA = 0°C to 70°C, VCC = 5 V ±5%

Symbol	Parameter	Min	Max	Unit
tR, tF	Rise and Fall Time for CA1, CB1, CA2 and CB2 Input Signals		1.0	µS
tCA2	Delay Time, Clock Negative Transition to CA2 Negative Transition (Read Handshake or Pulse Mode)		1.0	µS
tRS1	Delay Time, Clock Negative Transition to CA2 Positive Transition (Pulse Mode)		1.0	µS
tRS2	Delay Time, CA1 Active Transition to CA2 Positive Transition (Handshake Mode)		2.0	µS
tWHS	Delay Time, Clock Positive Transition to CA2 or CB2 Negative Transition (Write Handshake)	0.05	1.0	µS
tDS	Delay Time, Peripheral Data Valid to CB2 Negative Transition	0.20	1.5	µS
tRS3	Delay Time, Clock Positive Transition to CA2 or CB2 Positive Transition (Pulse Mode)		1.0	µS
tRS4	Delay Time, CA1 or CB1 Active Transition to CA2 or CB2 Positive Transition (Handshake Mode)		2.0	µS
t21	Delay Time Required from CA2 Output to CA1 Active Transition (Handshake Mode)	400		nS
tIL	Set-up Time, Peripheral Data Valid to CA1 or CB1 Active Transition (Input Latching)	300		nS
tSR1	Shift-Out Delay Time - Time from Ø2 Falling Edge to CB2 Data Out		300	nS
tSR2	Shift-In Set-up Time - Time from CB2 Data In to Ø2 Rising Edge	300		nS
tSR3	External Shift Clock (CB1) Set-up Time Relative to Ø2 Trailing Edge	100	tCYC	nS
tIPW	Pulse Width - PB6 Input Pulse	2 x tCYC		
tICW	Pulse Width - CB1 Input Clock	2 x tCYC		
tIPS	Pulse Spacing - PB6 Input Pulse	2 x tCYC		
tICS	Pulse Spacing - CB1 Input Pulse	2 x tCYC		
tAL	CA1, CB1 Set Up Prior to Transition to Arm Latch	300		nS
tPDH	Peripheral Data Hold After CA1, CB1 Transition	150		nS

FIGURE 2. TIMING FOR READ HANDSHAKE, PULSE MODE

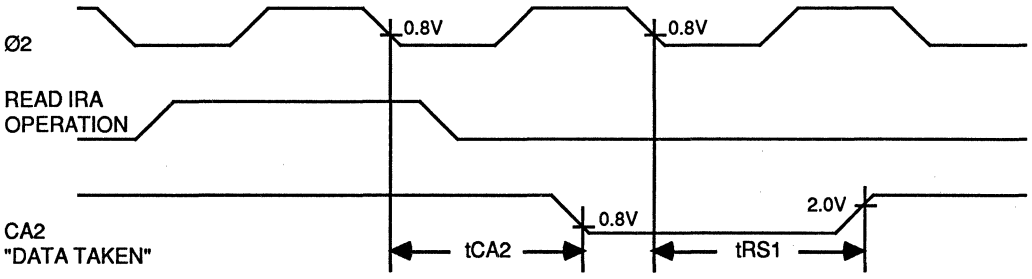


FIGURE 3. TIMING FOR READ HANDSHAKE, HANDSHAKE MODE

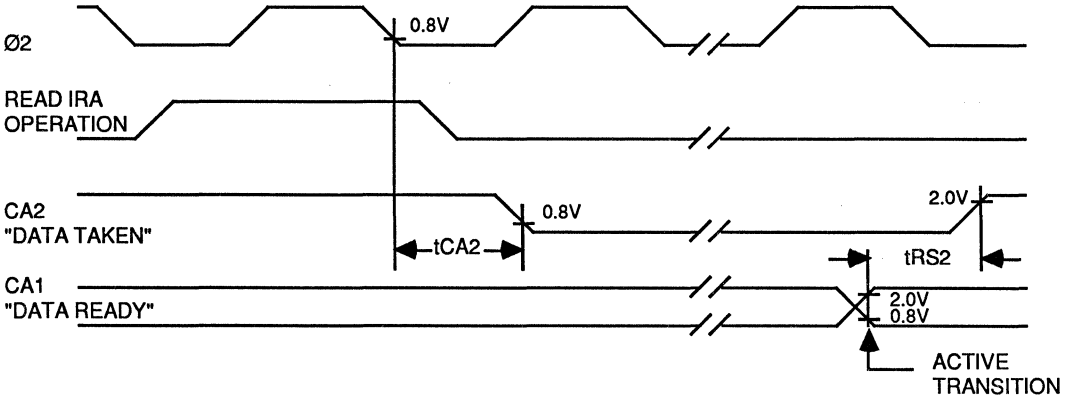


FIGURE 4. TIMING FOR WRITE HANDSHAKE, PULSE MODE

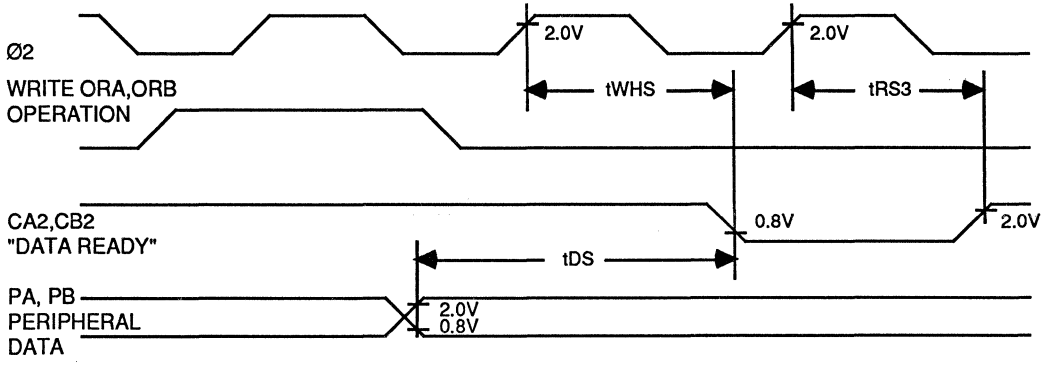


FIGURE 5. TIMING FOR WRITE HANDSHAKE, HANDSHAKE MODE

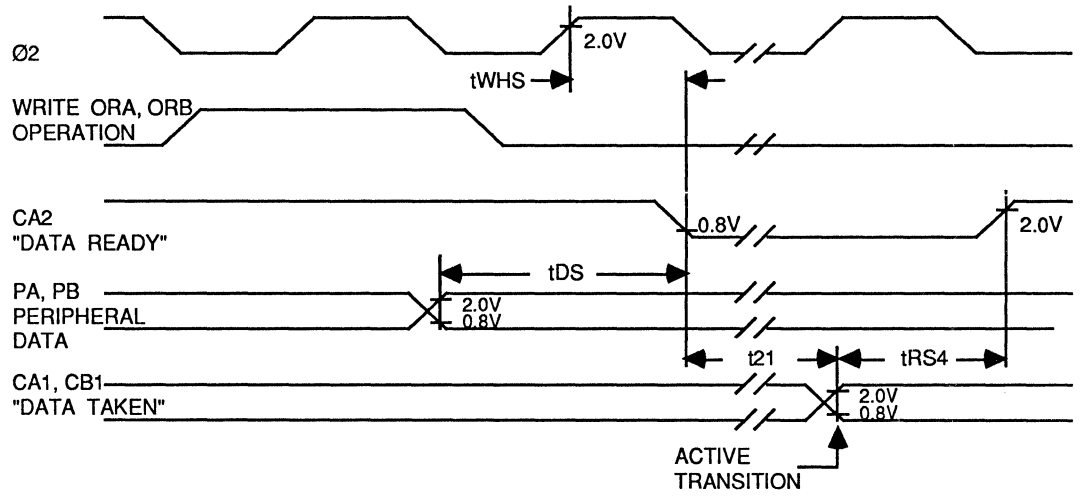


FIGURE 6. PERIPHERAL DATA INPUT LATCHING TIMING

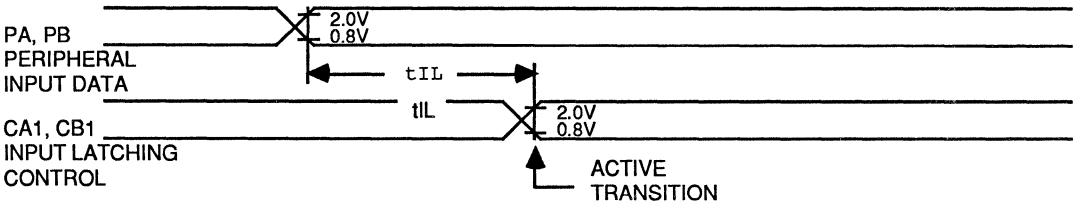


FIGURE 7. TIMING FOR SHIFT OUT WITH INTERNAL OR EXTERNAL SHIFT CLOCKING

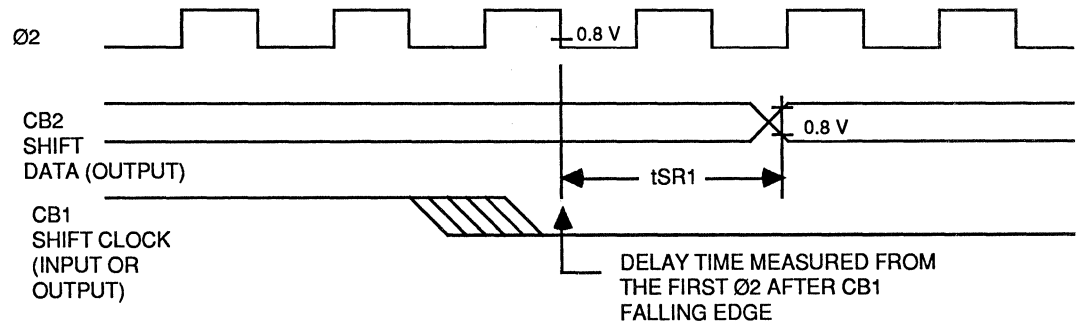


FIGURE 8. TIMING FOR SHIFT IN WITH INTERNAL OR EXTERNAL SHIFT CLOCKING

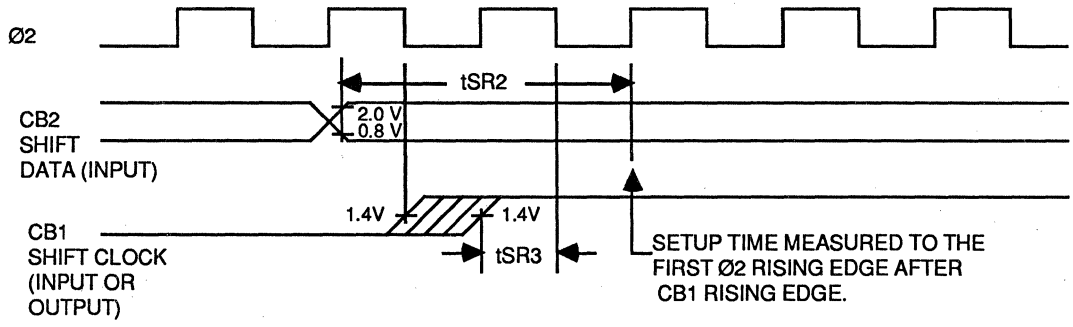


FIGURE 9. EXTERNAL SHIFT CLOCK TIMING

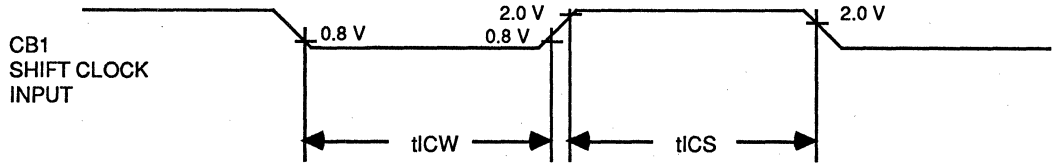


FIGURE 10. PULSE COUNT INPUT TIMING

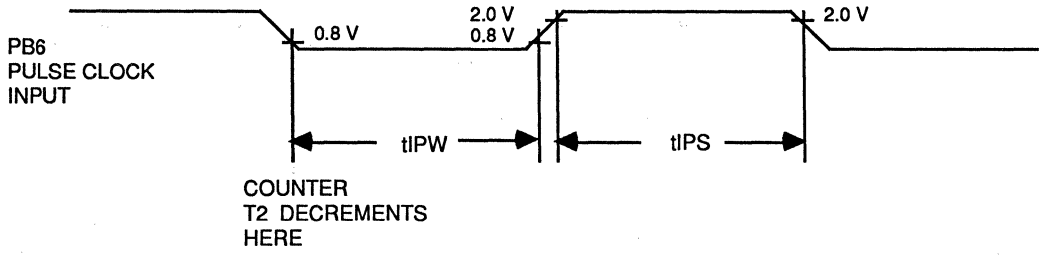


TABLE 2. REGISTER SELECT

Register Number	RS Coding				Register Designation	Register/Description	
	RS3	RS2	RS1	RS0		Write (R/$\overline{W}$ = L)	Read (R/$\overline{W}$ = H)
0	0	0	0	0	ORB / IRB	Output Register B	Input Register B
1	0	0	0	1	ORA / IRA	Output Register A	Input Register A
2	0	0	1	0	DDRB	Data Direction Register B	
3	0	0	1	1	DDRA	Data Direction Register A	
4	0	1	0	0	T1C - L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C - H	T1 High-Order Counter	
6	0	1	1	0	T1L - L	T1 Low-Order Latches	
7	0	1	1	1	T1L - H	T1 High-Order Latches	
8	1	0	0	0	T2C - L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C - H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	Interrupt Enable Register	
15	1	1	1	1	ORA / IRA	Output Register A *	Input Register A *

*Note: Same as register 1, except no handshake

TABLE 3. READ TIMING

Symbol	Parameter	VL6522-01		VL6522-02		VL65C22-01		VL65C22-02		VL65C22-03		VL65C22-04		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TCY	Cycle Time	1	10	0.5	10	1	10	0.5	10	0.33	10	0.25	10	µs
TACR	Address Set-up Time	180	-	90	-	180	-	90	-	65	-	45	-	ns
TCAR	Address Hold Time	0	-	0	-	0	-	0	-	0	-	0	-	ns
TPCR	Peripheral Data Set-up Time	300	-	150	-	300	-	150	-	110	-	75	-	ns
TCDR	Data Bus Delay Time	-	365	-	190	-	365	-	190	-	130	-	90	ns
THR	Data Bus Hold Time	10	-	10	-	10	-	10	-	10	-	10	-	ns

TABLE 4. WRITE TIMING

Symbol	Parameter	VL6522-01		VL6522-02		VL65C22-01		VL65C22-02		VL65C22-03		VL65C22-04		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
TCY	Cycle Time	1	10	0.5	10	1	10	0.5	10	0.33	10	0.25	10	µs
TC	Ø2 Pulse Width	470	-	240	-	470	-	240	-	180	-	120	-	ns
TACW	Address Set-up Time	180	-	90	-	180	-	90	-	65	-	45	-	ns
TCAW	Address Hold Time	0	-	0	-	0	-	0	-	0	-	0	-	ns
TWCW	R/$\overline{W}$ Set-up Time	180	-	90	-	180	-	90	-	65	-	45	-	ns
TCWW	R/$\overline{W}$ Hold Time	0	-	0	-	0	-	0	-	0	-	0	-	ns
TDCW	Data Bus Set-up Time	200	-	90	-	200	-	90	-	65	-	45	-	ns
THW	Data Bus Hold Time	10	-	10	-	10	-	10	-	10	-	10	-	ns
TCPW	Peripheral Data Delay Time	-	1.0	-	0.5	-	1.0	-	0.5	-	0.37	-	0.25	µs
TCMOS	Peripheral Data Delay Time to CMOS Levels	-	2.0	-	1.0	-	2.0	-	1.0	-	0.75	-	0.50	µs

Note: tRISE, tFALL = 10 to 30 ns.

FIGURE 11. READ TIMING

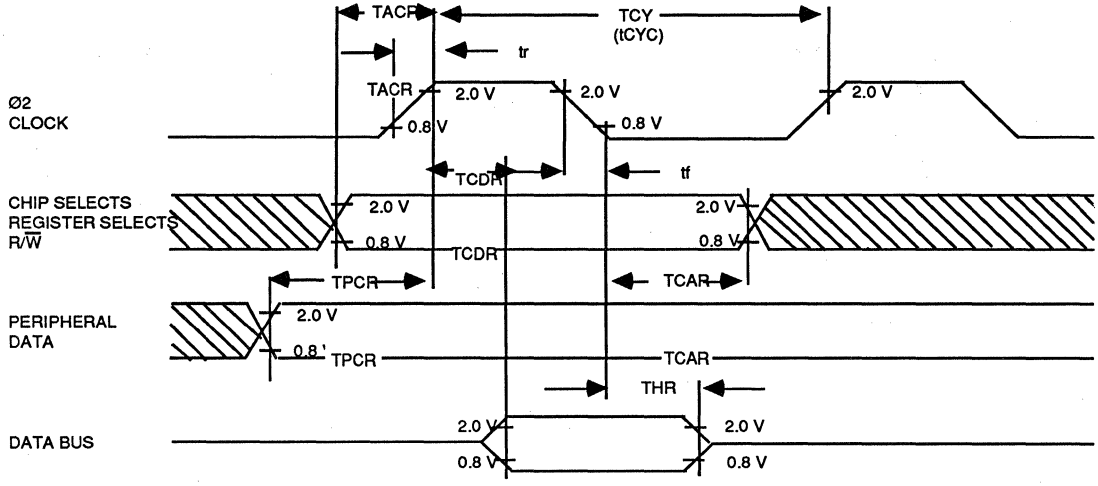


FIGURE 12. WRITE TIMING

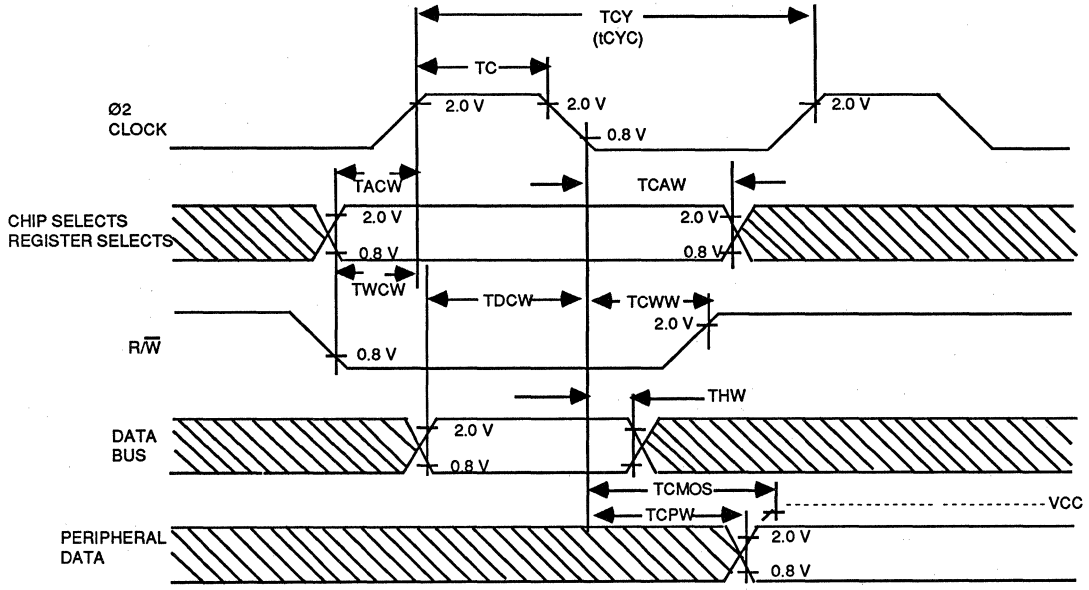
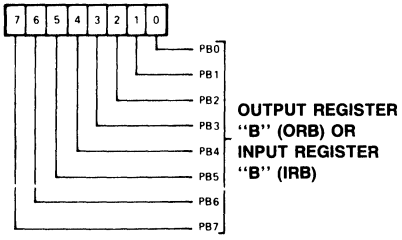
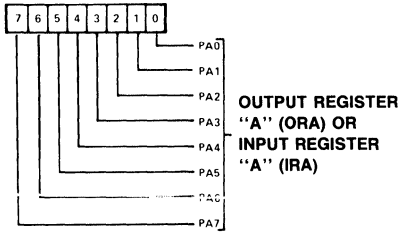


FIGURE 13. REGISTER 0, ORB/IRB



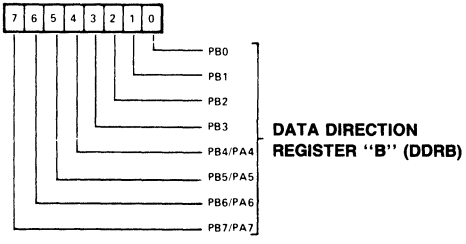
PIN DATA DIRECTION SELECTION	WRITE	READ
DDRB = "1" (OUTPUT)	MPU WRITES OUTPUT LEVEL (ORB)	MPU READS OUTPUT REGISTER BIT IN ORB. PIN LEVEL HAS NO AFFECT
DDRB = "0" (INPUT) (INPUT LATCHING DISABLED)	MPU WRITES INTO ORB, BUT NO EFFECT ON PIN LEVEL, UNTIL DDRB CHANGED	MPU READS INPUT LEVEL ON PB PIN
DDRB = "0" (INPUT) (INPUT LATCHING ENABLED)		MPU READS IRB BIT, WHICH IS THE LEVEL OF THE PB PIN AT THE TIME OF THE LAST CB1 ACTIVE TRANSITION

FIGURE 14. REGISTER 1, ORA/IRA



PIN DATA DIRECTION SELECTION	WRITE	READ
DDRA = "1" (OUTPUT) (INPUT LATCHING DISABLED)	MPU WRITES OUTPUT LEVEL (ORA)	MPU READS LEVEL ON PA PIN
DDRA = "1" (OUTPUT) (INPUT LATCHING ENABLED)		MPU READS IRA BIT WHICH IS THE LEVEL OF THE PA PIN AT THE TIME OF THE LAST CA1 ACTIVE TRANSITION
DDRA = "0" (INPUT) (INPUT LATCHING DISABLED)	MPU WRITES INTO ORA, BUT NO EFFECT ON PIN LEVEL, UNTIL DDRA CHANGED	MPU READS LEVEL ON PA PIN
DDRA = "0" (INPUT) (INPUT LATCHING ENABLED)		MPU READS IRA BIT, WHICH IS THE LEVEL OF THE PA PIN AT THE TIME OF THE LAST CA1 ACTIVE TRANSITION

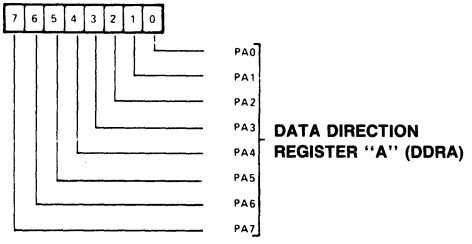
FIGURE 15. REGISTER 2, DDRB



"0" ASSOCIATED PB PIN IS AN INPUT (HIGH IMPEDANCE)

"1" ASSOCIATED PB PIN IS AN OUTPUT WHOSE LEVEL IS DETERMINED BY ORB REGISTER BIT

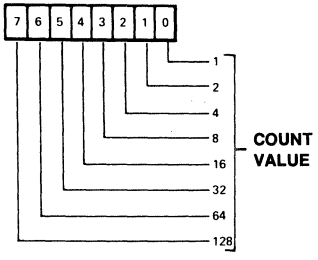
FIGURE 16. REGISTER 3, DDRA



"0" ASSOCIATED PA PIN IS AN INPUT (HIGH IMPEDANCE)

"1" ASSOCIATED PA PIN IS AN OUTPUT WHOSE LEVEL IS DETERMINED BY ORA REGISTER BIT

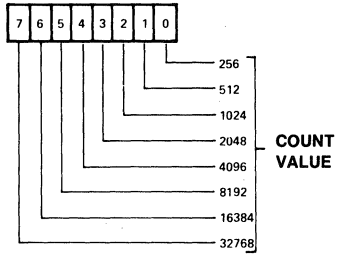
FIGURE 17. REGISTER 4, TIMER 1 LOW-ORDER COUNTER



WRITE – 8 BITS LOADED INTO T1 LOW-ORDER LATCHES. LATCH CONTENTS ARE TRANSFERRED INTO LOW-ORDER COUNTER AT THE TIME THE HIGH-ORDER COUNTER IS LOADED (REG 5).

READ – 8 BITS FROM T1 LOW-ORDER COUNTER TRANSFERRED TO MPU. IN ADDITION, T1 INTERRUPT FLAG IS RESET (BIT 6 IN INTERRUPT FLAG REGISTER).

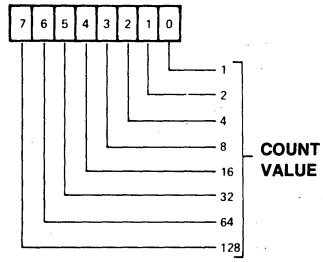
FIGURE 18. REGISTER 5, TIMER 1 HIGH-ORDER COUNTER



WRITE – 8 BITS LODED INTO T1 HIGH-ORDER LATCHES. ALSO, AT THIS TIME BOTH HIGH- AND LOW-ORDER LATCHES TRANSFERRED INTO T1 COUNTER. T1 INTERRUPT FLAG ALSO IS RESET.

READ – 8 IBTS FROM T1 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

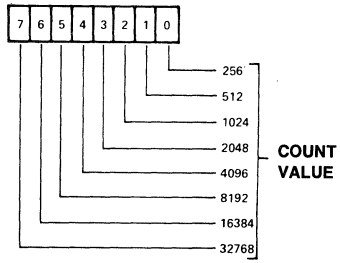
FIGURE 19. REGISTER 6, TIMER 1 LOW-ORDER LATCH



WRITE – 8 BITS LOADED INTO T1 LOW-ORDER LATCHES. THIS OPERATION IS NO DIFFERENT THAN A WRITE INTO REG 4.

READ – 8 BITS FROM T1 LOW-ORDER LATCHES TRANSFERRED TO MPU. UNLIKE REG 4 OPERATION, THIS DOES NOT CAUSE RESET OF T1 INTERRUPT FLAG

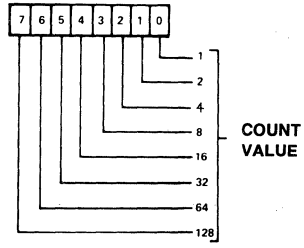
FIGURE 20. REGISTER 7, TIMER 1 HIGH-ORDER LATCH



WRITE – 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. UNLIKE REG 4 OPERATION NO LATCH-TO-COUNTER TRANSFERS TAKE PLACE.

READ – 8 BITS FROM T1 HIGH-ORDER LATCHES TRANSFERRED TO MPU.

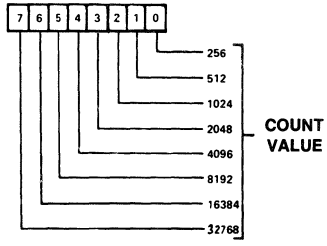
FIGURE 21. REGISTER 8, TIMER 2 LOW-ORDER LATCH/COUNTER



WRITE – 8 BITS LOADED INTO T2 LOW-ORDER LATCH

READ – 8 BITS FROM T2 LOW-ORDER COUNTER TRANSFERRED TO MPU. T2 INTERRUPT FLAG IS RESET.

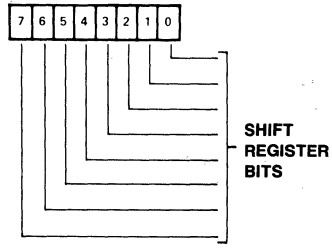
FIGURE 22. REGISTER 9, TIMER 2 HIGH-ORDER LATCH/COUNTER



WRITE – 8 BITS LOADED INTO T2 HIGH-ORDER COUNTER. ALSO, LOW ORDER LATCH TRANSFERRED TO LOW-ORDER COUNTER. IN ADDITION, T2 INTERRUPT FLAG IS RESET.

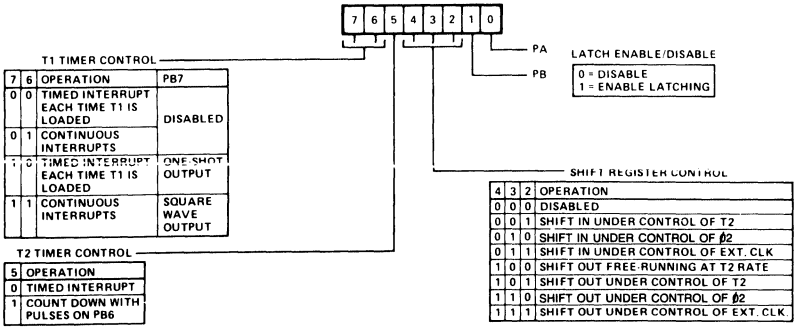
READ – 8 BITS FROM T2 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

FIGURE 23. REGISTER 10, SHIFT REGISTER



NOTES:
1. WHEN SHIFTING OUT, BIT 7 IS THE FIRST BIT OUT AND SIMULTANEOUSLY IS ROTATED BACK INTO BIT 0.
2. WHEN SHIFTING IN, BITS INITIALLY ENTER BIT 0 AND ARE SHIFTED TOWARDS BIT 7.

FIGURE 24. REGISTER 11A, AUXILIARY CONTROL REGISTER

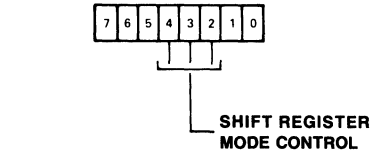


7	6	OPERATION	PB7
0	0	TIMED INTERRUPT EACH TIME T1 IS LOADED	DISABLED
0	1	CONTINUOUS INTERRUPTS	
1	0	TIMED INTERRUPT EACH TIME T1 IS LOADED	ONE-SHOT OUTPUT
1	1	CONTINUOUS INTERRUPTS	SQUARE WAVE OUTPUT

5	OPERATION
0	TIMED INTERRUPT
1	COUNT DOWN WITH PULSES ON PB6

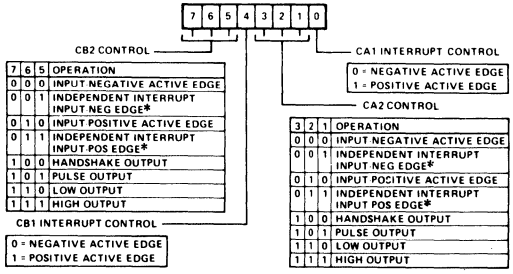
4	3	2	OPERATION
0	0	0	DISABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF $\phi 2$
0	1	1	SHIFT IN UNDER CONTROL OF EXT. CLK
1	0	0	SHIFT OUT FREE-RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF $\phi 2$
1	1	1	SHIFT OUT UNDER CONTROL OF EXT. CLK

FIGURE 25. REGISTER 11B, AUXILIARY CONTROL REGISTER



4	3	2	OPERATION
0	0	0	DISABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF ϕ_2
0	1	1	SHIFT IN UNDER CONTROL OF EXT CLK
1	0	0	SHIFT OUT FREE-RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF ϕ_2
1	1	1	SHIFT OUT UNDER CONTROL OF EXT CLK

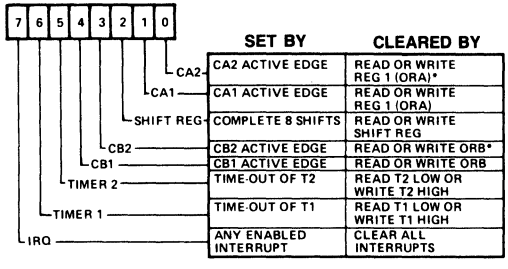
FIGURE 26. REGISTER 12, PERIPHERAL CONTROL REGISTER



7	6	5	OPERATION
0	0	0	INPUT NEGATIVE ACTIVE EDGE
0	0	1	INDEPENDENT INTERRUPT INPUT NEG EDGE*
0	1	0	INPUT POSITIVE ACTIVE EDGE
0	1	1	INDEPENDENT INTERRUPT INPUT POS EDGE*
1	0	0	HANDSHAKE OUTPUT
1	0	1	PULSE OUTPUT
1	1	0	LOW OUTPUT
1	1	1	HIGH OUTPUT

3	2	1	OPERATION
0	0	0	INPUT NEGATIVE ACTIVE EDGE
0	0	1	INDEPENDENT INTERRUPT INPUT NEG EDGE*
0	1	0	INPUT POSITIVE ACTIVE EDGE
0	1	1	INDEPENDENT INTERRUPT INPUT POS EDGE*
1	0	0	HANDSHAKE OUTPUT
1	0	1	PULSE OUTPUT
1	1	0	LOW OUTPUT
1	1	1	HIGH OUTPUT

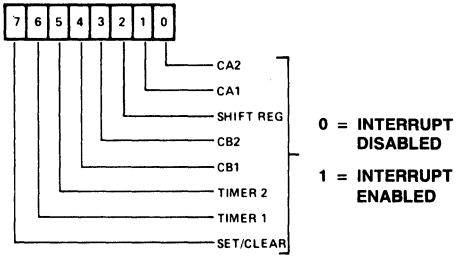
FIGURE 27. REGISTER 13, INTERRUPT FLAG REGISTER



	SET BY	CLEARED BY
CA2	CA2 ACTIVE EDGE	READ OR WRITE REG 1 (ORA)*
CA1	CA1 ACTIVE EDGE	READ OR WRITE REG 1 (ORA)
SHIFT REG	COMPLETE 8 SHIFTS	READ OR WRITE SHIFT REG
CB2	CB2 ACTIVE EDGE	READ OR WRITE ORB*
CB1	CB1 ACTIVE EDGE	READ OR WRITE ORB
TIMER 2	TIME-OUT OF T2	READ T2 LOW OR WRITE T2 HIGH
TIMER 1	TIME-OUT OF T1	READ T1 LOW OR WRITE T1 HIGH
IRQ	ANY ENABLED INTERRUPT	CLEAR ALL INTERRUPTS

* IF THE CA2/CB2 CONTROL IN THE PCR IS SELECTED AS "INDEPENDENT" INTERRUPT INPUT, THEN READING OR WRITING THE OUTPUT REGISTER ORA/ORB WILL NOT CLEAR THE FLAG BIT. INSTEAD, THE BIT MUST BE CLEARED BY WRITING INTO THE IFR, AS DESCRIBED PREVIOUSLY.

FIGURE 28. REGISTER 14, INTERRUPT ENABLE REGISTER



NOTES:
1. IF BIT 7 IS A "0", THEN EACH "1" IN BITS 0 - 6 DISABLES THE CORRESPONDING INTERRUPT.
2. IF BIT 7 IS A "1", THEN EACH "1" IN BITS 0 - 6 ENABLES THE CORRESPONDING INTERRUPT.
3. IF A READ OF THIS REGISTER IS DONE, BIT 7 WILL BE "1" AND ALL OTHER BITS WILL REFLECT THEIR ENABLE/DISABLE STATE.

DC CHARACTERISTICS: VCC = 5.0 V ±5%, VSS = 0 V, T = 0 0°C to 70°C unless otherwise noted

Symbol	Parameter		Min.	Typ.	Max.	Unit	Conditions
VIH	Input High Voltage		2.4		VCC	V	
VIL	Input Low Voltage		- 0.3		0.4	V	
IIN	Input Leakage Current R/W, RES, RS3 - RS0, CS2, CS1, CA1Ø2		-		±2.5	µA	VIN = 0V to 5.0v VCC = 0V
ITSI	Input Leakage Current for Off Stat e D7 - D0		-		±10	µA	VIN = 0.4V to 2.4V VCC = 5.25 V
IIH	Input High Current PA7-PA0, CA2, PB7-PB0, CB1, CB2		- 100		-	µA	VIN = 2.4V
IIL	Input Low Current PA7-PA0, CA2, PB7-PB0, CB1, CB2		-		- 1.8	mA	VIL = 0.4V
VOH	Output High Voltage PA7-PA0, CA2, PB7-PB0, CB1, CB2		2.4		-	V	VCC = 4.75V ILOAD = - 100 µA
VOL	Output Low Voltage		-		0.4	V	VCC = 4.75V ILOAD = 1.6 mA
IOH	Output High Current (Sourcing)	PA7-PA0, PB7-PB0 (TTL drive),D7-D0	- 100		-	µA	VOH = 2.4V
		PB7-PB0 (other drive, e.g., Darlington)	- 1.0		-	mA	VOH = 1.5V
IOL	Output Low Current (Sinking)		1.6		-	mA	VOL = 0.4V
IOFF	Output Leakage Current (Off State) IRQ		-		10	µA	
PD	Power Dissipation (VL6522)		-		700	mW	
ICC	Power Supply Current (VL65C22)			8		mA	

CAPACITANCE: TA = 25°C, f = 1.0 MHz

Symbol	Parameter		Min.	Typ.	Max.	Unit	Conditions
CI	Input Capacitance	R/W, RES, RS3-RS0, CS2,CS1, D7-D0, CA1, CA2, PA7-PA0, PB7-PB0	-		7.0	pF	VCC = 5.0 V VIN = 0 V
		CB1, CB2	-		10	pF	
		Ø2 Input	-		20	pF	
COUT	Output Capacitance		-		10	pF	

Notes:

1. All units are direct current (DC).
2. Negative sign indicates outward current flow, positive indicates inward flow.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	-10 to +80°C
Storage Temperature	-65 to +150°C
Supply Voltage to Ground Potential	-0.5 to +7.0 V
Applied Output Voltage	-0.5 to +7.0 V
Applied Input Voltage	-0.5 to +7.0 V
Power Dissipation	750 mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to conditions for extended periods may affect device reliability.

VL6765

DOUBLE-DENSITY FLOPPY DISK CONTROLLER (DDFDC)

FEATURES

- Address mark detection circuitry
- Software control of
  —Track stepping rate
  —Head load time
  —Head unload time
- IBM compatible in both single- and double-density format
- Programmable data record lengths: 128, 256, 512, 1024, 2048, 4096 or 8192 bytes/sector
- Multi-sector and multi-track transfer capability
- Controls up to four floppy disk drives
- Data scan capability—will scan a single sector or an entire track of data fields, comparing on a byte-by-byte basis data in the processor's memory with data read from the disk
- Data transfers in DMA or non-DMA mode
- Parallel seek operations on up to four drives
- Directly compatible with an 8-bit or 16-bit synchronous microprocessor bus including Z-80/8080A/8085A, 8086, and 8088
- Replaces the NEC μPD765A, Intel 8272A, and Rockwell 6765A
- Single phase 4 or 8 MHz clock
- Single +5 volt power supply

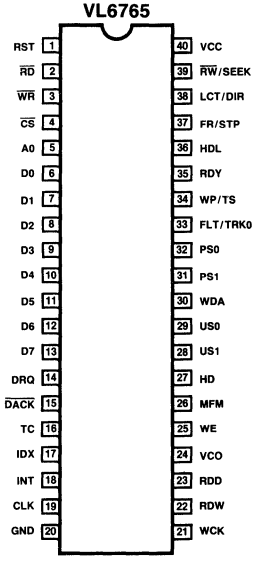
DESCRIPTION

The VL6765 Double-Density Floppy Disk Controller (DDFDC) interfaces up to four floppy disk drives to an 8-bit or 16-bit microprocessor-based system including Z80, 8080A, 8085A, 8086, and 8088. The DDFDC simplifies the system design by minimizing both the number of external hardware components and software steps needed to implement the floppy disk drive (FDD) interface. Control signals supplied by the DDFDC reduce the number of components required in external phase locked loop and write precompensation circuitry. Memory-mapped registers containing commands, status and data simplify the software interface. Built-in functions reduce the software overhead needed to control the FDD interface. The DDFDC supports both the IBM 3740 Single-Density (FM) and IBM System 34 Double-Density (MFM) formats.

The DDFDC interfaces directly to the synchronous microprocessor bus and operates with 8-bit byte length data transferred on the bus in either DMA or non-DMA mode. In DMA mode, the CPU need only load the command into the DDFDC and all data transfers occur under DMA control. The VL6765 is directly compatible with the Z8410/μPD8257 Direct Memory Access Controller (DMAC). In non-DMA mode, the DDFDC generates an interrupt to the CPU indicating that a byte of data is available.

Controller commands, command or device status, and data are transferred between the DDFDC and the CPU via six internal registers. The Main Status Register (MSR) stores the DDFDC status information while four additional status registers provide result information to the CPU following each controller command. The Data Register (DR) stores actual disk data, parameters, controller commands and FDD status information for use by the CPU.

PIN DIAGRAM

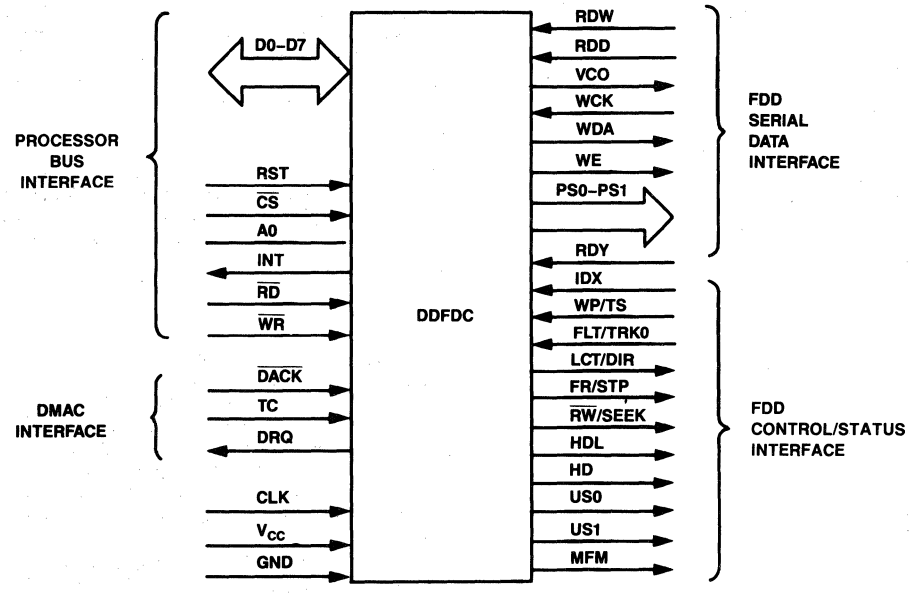


ORDER INFORMATION

Part Number	Clock Frequency	Package
VL6765-04PC VL6765-04CC VL6765-04QC	4 MHz	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)
VL6765-08PC VL6765-08CC VL6765-08QC	8 MHz	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)

Note:
Operating temperature range: 0°C to +70°C.

Figure 1. DDFDC Input and Output Signals



PIN DESCRIPTION

Throughout this document signals are presented using the terms active and inactive, or asserted and negated, independent of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is described below.) Active low signals are denoted by a superscript bar.

BUS INTERFACE

D0-D7—Data Lines. The bidirectional data lines transfer data between the DDFDC and the 8-bit data bus.

CLK—CLOCK. The clock is a TTL compatible 4 or 8 MHz square wave signal.

RST—RESET. This active high input places the DDFDC in the idle state and resets the output lines to the floppy disk drive (FDD) to the low state. RST does not affect the Step Rate Time (SRT), Head Unload Time (HUT) or Head Load Time (HLT) set by a Specify command. If RDY goes high while RST is high, the DDFDC will assert INT within 1.024 ms. This interrupt can be cleared by issuing a Sense Interrupt Status command.

$\overline{CS}$—Chip Select. The DDFDC is selected when the $\overline{CS}$ input is low.

A0—Data/Status Register Select. This input selects the Data or Status Register for reading from or writing to. When A0 = high, the Data Register is selected and the state of $\overline{RD}$ or $\overline{WR}$ determines whether it is a read ($\overline{RD}$ = low) or a write ($\overline{WR}$ = low) operation. When A0 = low, the Status Register is selected. This register may only be read ($\overline{RD}$ = low); the state $\overline{WR}$ = low is invalid when the Status Register is selected.

INT—Interrupt Request. This active high output is the interrupt request generated by the DDFDC to the CPU. INT is asserted upon completion of some DDFDC commands and before a data byte is transferred between the DDFDC and the data bus (in the Non-DMA mode).

$\overline{RD}$—Read. This active low input defines the data bus transfer as a read cycle. When low, the data transfer is from the DDFDC to the data bus.

$\overline{WR}$—Write. This active low input defines the data bus transfer as a write cycle. When low, the data transfer is from the data bus to the DDFDC.

DIRECT MEMORY ACCESS CONTROLLER (DMAC) INTERFACE

$\overline{DACK}$—DMA Acknowledge. The DMA transfer acknowledge signal is a TTL compatible input generated by the DMA controller (DMAC) controlling the DDFDC. The DMA cycle is active when $\overline{DACK}$ is low and the DDFDC is performing a DMA transfer.

DRQ—Data DMA Request. The transfer request signal is a TTL compatible output generated by the DDFDC to request a data transfer operation under control of the DMAC (in the DMA mode). The request is active when DRQ = high. The signal is reset inactive when DMA Acknowledge ($\overline{DACK}$) is asserted (low).

TC—Terminal Count. This input signal is issued to the DDFDC when the DMA transfer for a channel is complete. The signal is active high concurrent with the $\overline{DACK}$ input when the DMA operation is complete as a result of that transfer.

FDD SERIAL DATA INTERFACE

RDD—Read Data. Read Data input from the floppy disk drive (FDD) containing clock and data bits.

RDW—Read Data Window. Data Window input generated by the Phase Locked Loop (PLL) and used to sample data from the FDD.

VCO—Voltage Controlled Oscillator Sync. This output signal inhibits the VCO in the PLL circuit when low and enables the VCO in the PLL circuit when high. This inhibits RDD and RDW from being generated until valid data is detected from the FDD.

WCK—Write Clock. This input clock determines the Write Data rate to the FDD. The data rate is 500 KHz in the FM mode (MFM = low) and 1 MHz in the MFM mode (MFM = high). The pulse width is 250 ns (typical) in both modes.

WDA—Write Data. Serial write data output to the FDD containing both clock and data bits.

WE—Write Enable. This output signal enables the Write Data into the FDD when high.

PS0-PS1—Preshift. These outputs are encoded to convey write compensation status during the MFM mode to determine early, late or normal times as follows:

Write Precompensation Status	Preshift Outputs	
	PS0	PS1
Normal	0	0
Late	0	1
Early	1	0
Invalid	1	1

0 = Low, 1 = High

FDD STATUS INTERFACE

RDY—Ready. An active high input signal indicates the FDD is ready to send data to, or receive data from, the DDFDC.

IDX—Index. An active high input signal from the FDD indicates the index hole is under the index sensor. Index is used to synchronize DDFDC timing.

$\overline{RW}$/SEEK—Read Write/Seek. Mode selection signal to the FDD which controls the multiplexer from the multiplexed signals. When $\overline{RW}$/SEEK is low, the Read/Write mode is commanded; when $\overline{RW}$/SEEK is high, the Seek mode is commanded.

$\overline{RW}$/SEEK	Mode	Active FDD Interface Signals
Low	Read/Write	WP, FLT, LCT, FR
High	Seek	TS, TRK0, DIR, STP

WP/TS—Write Protect/Two Side. An active high multiplexed input signal from the FDD. In the Read/Write mode, WP/TS high indicates the media is write-protected. In the Seek mode, WP/TS high indicates the media is two-sided.

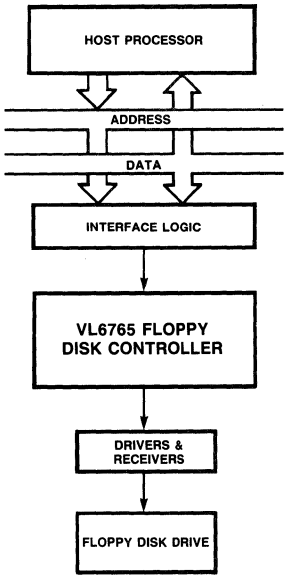
FLT/TRK0—Fault/Track Zero. An active high multiplexed input from the FDD. In the Read/Write mode ($\overline{RW}$/SEEK = low), FLT/TRK0 high indicates an FDD fault. In the Seek mode, FLT/TRK0 high indicates that the read/write head is positioned over track zero.

LCT/DIR—Low Current/Direction. A multiplexed output to the FDD. In the Read/Write mode, LCT/DIR is low when the read/write head is to be positioned over the inner tracks and the LCT/DIR is high when the head is to be positioned over the outer tracks. In the Seek mode, LCT/DIR controls the head direction. When LCT/DIR is high, the head steps to the outside of the disk; when LCT/DIR is low, the head steps to the inside of the disk.

FR/STP—Fault Reset/Step. A multiplexed output to the FDD. In the Read/Write mode, FR/STP high resets the fault indicator in the FDD. An FR pulse is issued at the beginning of each read or write command prior to issuing HDL. In the Seek mode, FR/STP provides the step pulses to move the read/write head to another track in the direction indicated by the LCT/DIR signal.

HDL—Head Load. An active high output to notify the FDD that the read/write head should be loaded (placed in contact with the media). A low level indicates the head should be unloaded.

Figure 2. Typical VL6765 Application



HD—Head Select. An output to the FDD to select the proper read/write head. Head One is selected when HD = high and Head Zero is selected when HD = low.

US0-US1—Unit Select. Output signals for floppy disk drive selection as follows:

Unit Select		Floppy Disk Drive Select
US0	US1	
0	0	0
0	1	1
1	0	2
1	1	3

0 = Low, 1 = High

MFM—MFM Mode. Output signal to the FDD to indicate MFM or FM mode. Selects the MFM mode when MFM = high and the FM mode MFM = Low.

VCC—Power. +5 Vdc.

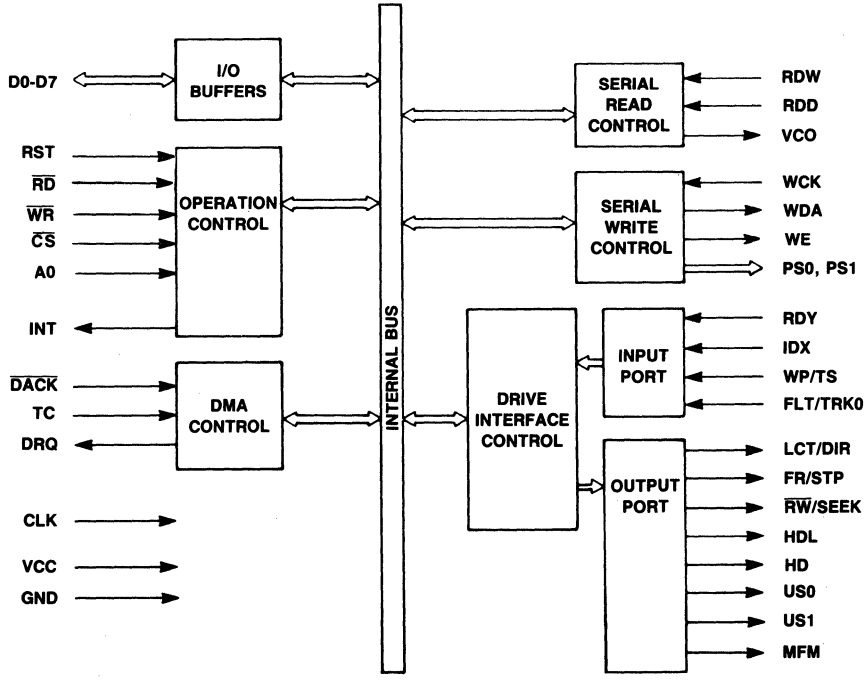
GND-Ground (V_{ss}).

DDFDC REGISTERS

The DDFDC contains six registers which may be accessed by the processor or DMA controller via the system (i.e., microprocessor) bus: a Main Status Register, a Data Register, and four Result Status Registers. The 8-bit Main Status Register (MSR) contains the status information of the DDFDC, and may be accessed at any time. The 8-bit Data Register, consisting of several registers in a stack with only one register presented to the data bus at a time, stores data, commands, parameters and FDD status information. Bytes of data are read out of, or written into, the Data Register in order to initiate a command or to obtain the results of a command execution.

The read-only Main Status Register facilitates the transfer of data between the system and the DDFDC. The other Status Registers (ST0, ST1, ST2 and ST3) are only available during the result phase, and may be read only after completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

Figure 3. DDFDC Block Diagram



The relationship between the status/data registers and the $\overline{WR}$, $\overline{RD}$ and A0 signals is shown below.

A0	$\overline{RD}$	$\overline{WR}$	Function
0	0	0	Illegal
0	0	1	Read Main Status Register
0	1	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

0 = Low, 1 = High

Table 1 shows each of the status registers used by the DDFDC and each bit assignment within the individual registers. Table 2 defines the symbols used throughout the command definitions. Each register bit symbol is defined in the register descriptions that follow Table 2.

REGISTER DEFINITIONS

Main Status Register (MSR)

7	6	5	4	3	2	1	0
RQM	DIO	EXM	CB	D3B	D2B	D1B	D0B

The Main Status Register (MSR) contains the status information of the DDFDC, and must be read by the processor before each byte is written to, or read from, the Data Register during the command or result phase. MSR reads are not required during the execution phase. The Data Input/Output (DIO) and Request for Master (RQM) bits in the MSR indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last $\overline{RD}$ or $\overline{WR}$ during command or result phases and the DIO and RQM getting set or reset is 12 μs. For this reason, every time the MSR is read the processor should wait 12 μs. The maximum time from the trailing edge of the last $\overline{RD}$ in the result phase to when bit 4 (DDFDC Busy) goes low is also 12 μs.

The DIO and RQM timing chart is shown in Figure 4.

MSR
7 RQM —Request for Master.
0 Data Register is not ready.
1 Data Register is ready.

MSR
6 DIO —Data Input/Output.
0 Data transfer is from system to the Data Register.
1 Data transfer is from Data Register to the system.

MSR
5 EXM —Execution Mode. (Non-DMA mode only).
0 Execution phase ended, result phase begun.
1 Execution phase started.

MSR
4 CB —Controller (DDFDC) Busy.
0 DDFDC is not busy, will accept a command.
1 DDFDC is busy, will not accept a command.

MSR
3 D3B —Floppy Disk Drive (FDD) 3 Busy.
0 FDD 3 is not busy, DDFDC will accept read or write command.
1 FDD 3 is busy, DDFDC will not accept read or write command.

MSR
2 D2B —FDD 2 Busy.
0 FDD 2 is not busy, DDFDC will accept read or write command.
1 FDD 2 is busy, DDFDC will not accept read or write command.

MSR
1 D1B —FDD 1 Busy.
0 FDD 1 is not busy, DDFDC will accept read or write command.
1 FDD 1 is busy, DDFDC will not accept read or write command.

MSR
0 D0B —FDD 0 Busy.
0 FDD 0 is not busy, DDFDC will accept read or write command.
1 FDD 0 is busy, DDFDC will not accept read or write command.

Status Register 0 (ST0)

7	6	5	4	3	2	1	0
IC		SE	EC	NR	HD	US	
						US1	US0

The Status Register 0 (ST0) as well as the other status registers (ST1-ST3), are available only during the result phase, and may be read only after completing a command. The particular command executed determines which status registers are used and may be read.

ST0
7 6 IC —Interrupt Code.
0 0 Normal Termination (NT). Command was properly executed and completed.
0 1 Abnormal Termination (AT). Command execution was started, but was not successfully completed.
1 0 Invalid Command (IC). Received command was invalid.
1 1 Abnormal Termination (AT). The Ready (RDY) signal from the FDD changed state during command execution.

ST0
5 SE —Seek End.
0 Seek command is not completed.
1 Seek command completed by DDFDC.

ST0
4 EC —Equipment Check.
0 No error.
1 Either a fault signal is received from the FDD or the track 0 signal failed to occur after 256 step pulses (Recalibrate command).

Table 1. DDFDC Status Register Bit Assignments

	Bit Number							
Main Status Register (MSR)	7	6	5	4	3	2	1	0
Status Register 0 (ST0)	RQM	DIO	EXM	CB	D3B	D2B	D1B	D0B
Status Register 1 (ST1)	IC		SE	EC	NR	HD	US	
							US1	US0
Status Register 2 (ST2)	EN	0	DE	OR	0	ND	NW	MA
Status Register 3 (ST3)	0	CM	DD	WT	SH	SN	BT	MD
	FLT	WP	RDY	TRK0	TS	HD	US1	US0

Table 2. Command Symbol Description

Symbol	Name	Description
A0	Address Line A0	Controls selection of Main Status Register (A0 = low) or Data Register (A0 = high).
D	Data	The data pattern which is going to be written into a sector.
D0-D7	Data Bus	8-bit data bus, where D0 is the least significant data line and D7 is the most significant data line.
DTL	Data Length	When N is defined as 00, DTL is the number of data bytes to read from or write into the sector.
EOT	End of Track	The final sector number on a track. During read or write operation, the DDFDC stops data transfer after reading from or writing to the sector equal to EOT.
GPL	Gap Length	The length of Gap 3. During read/write commands this value determines the number of bytes that the VCO will stay low after two CRC bytes. During the Format a Track command it determines the size of Gap 3.
H	Head Address	Head number 0 or 1, as specified in ID field.
HD (H)	Head	A selected head number 0 or 1 which controls the polarity of pin 27. (H = HD in all command words).
HLT	Head Load Time	The head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	The head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	When MF = 0, FM mode is selected; and when MF = 1, MFM mode is selected.
MT	Multi-Track	When MT = 1, a multi-track operation is to be performed. After finishing a read/write operation on side 0, the DDFDC will automatically start searching for sector 1 on side 1.
N	Bytes/Sector	The number of data bytes written in a sector.
ND	Non-DMA Mode	When ND = 1, operation is in the Non-DMA mode; when ND = 0, operation is in the DMA mode.
NTN	New Track Number	A new track number, which will be reached as a result of the Seek command. Desired head position.
PTN	Present Track Number	The track number at the completion of Sense Interrupt Status command. Present head position.
R	Record (Sector)	The sector number to be read or written.
R/W	Read/Write	Either read (R) or write (W) signal.
ST	Sectors/Track	The number of sectors per track.
SK	Skip	Skip Deleted Data Address Mark.
SRT	Step Rate Time	The stepping rate for the FDD (1 to 16 ms in 1 ms increments). Stepping rate applies to all drives (F = 1 ms, E = 2 ms, etc.)
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by A0 = low). ST0-ST3 may be read only after a command has been executed and contain information relevant to that particular command.
STP	Sector Test Process	During a Scan command, if STP = 01, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA controller); and if STP = 02, then alternate sectors are read and compared.
T	Track Number	The current/selected track number of the medium (0–255).
US0,US1	Unit Select	A selected drive number (0-3).

ST0

3 NR —Not Ready.

0 FDD is ready.

1 FDD is not ready at issue of read or write command. If a read or write command is issued to side 1 of a single-sided drive, this bit is also set.

ST0

2 HD —Head Address. (At Interrupt).

0 Head Select 0.

1 Head Select 1.

ST0

1 0 US —Unit Selected. (At Interrupt).

0 0 FDD 0 selected.

0 1 FDD 1 selected.

1 0 FDD 2 selected.

1 1 FDD 3 selected.

Status Register 1 (ST1)

7	6	5	4	3	2	1	0
EN	0	DE	OR	0	ND	NW	MA

ST1

7 EN —End of Track.

0 No error.

1 DDFDC attempted to access a sector beyond the last sector of a track.

ST1

6 —Not Used. Always Zero.

ST1

5 DE —Data Error.

0 No error.

1 DDFDC detected a CRC error in ID field or the Data field.

ST1

4 OR —Overrun.

0 No error.

1 DDFDC was not serviced by the system during data transfers, within a predetermined time interval.

ST1

3 —Not Used. Always Zero.

ST1

2 ND —No Data.

0 No error.

1 3 possible errors.

1. DDFDC cannot find sector specified in the Internal Data Register (IDR) during execution of Read Data, Write Deleted Data or Scan commands.
2. DDFDC cannot read ID field without an error during Read ID command.
3. DDFDC cannot find starting sector during execution of Read a Track command.

ST1

1 NW —Not Writable.

0 No error.

1 DDFDC detected a write protect signal from FDD during execution of Write Data, Write Deleted Data or Format a Track commands.

ST1

0 MA —Missing Address Mark.

0 No error.

1 2 possible errors.

1. DDFDC cannot detect the ID Address Mark after encountering the index hole twice.
2. DDFDC cannot detect the Data Address Mark or Deleted Data Address Mark. The MD (Missing Address Mark in Data field) of Status Register 2 is also set.

Status Register 2 (ST2)

7	6	5	4	3	2	1	0
0	CM	DD	WT	SH	SN	BT	MD

ST2

7 —Not Used. Always Zero.

ST2

6 CM —Control Mark.

0 No error.

1 DDFDC encountered a sector which contained a Deleted Data Address Mark during execution of a Read Data, Read a Track, or Scan command, or which contained a Data Address Mark during execution of a Read Deleted Data command.

ST2

5 DD —Data Error in Data Field.

0 No error.

1 DDFDC detected a CRC error in the Data field.

ST2

4 WT —Wrong Track.

0 No error.

1 Contents of T on the disk is different from that stored in IDR. Bit is related to ND (Bit 2) of Status Register 1.

ST2

3 SH —Scan Equal Hit.

0 No "equal" condition during a scan command.

1 "Equal" condition satisfied during a scan command.

ST2

2 SN —Scan Not Satisfied.

0 No error.

1 DDFDC cannot find a sector on the track which meets the scan command condition.

ST2

1 BT —Bad Track.
0 No error.
1 Contents of T on the disk is different from that stored in the IDR and T = FF. Bit is related to ND (Bit 2) of Status Register 1.

ST2

0 MD —Missing Address Mark in Data Field.
0 No error.
1 DDFDC cannot find a Data Address Mark or Deleted Data Address Mark during a data read from the disk.

Status Register 3 (ST3)

7	6	5	4	3	2	1	0
FLT	WP	RDY	TRK0	TS	HD	US1	US0

Status Register 3 (ST3) holds the results of the Sense Drive Status command.

ST3

7 FLT —Fault.
0 Fault (FLT) signal from the FDD is low.
1 Fault (FLT) signal from the FDD is high.

ST3

6 WP —Write Protect.
0 Write Protect (WP) signal from the FDD is low.
1 Write Protect (WP) signal from the FDD is high.

ST3

5 RDY —Ready.
0 Ready (RDY) signal from the FDD is low.
1 Ready (RDY) signal from the FDD is high.

ST3

4 TRK0 —Track 0.
0 Track 0 (TRK0) signal from the FDD is low.
1 Track 0 (TRK0) signal is from the FDD is high.

ST3

3 TS —Two Side.
0 Two Side (TS) signal from the FDD is low.
1 Two Side (TS) signal from the FDD is high.

ST3

2 HD —Head Select.
0 Head Select (HD) signal to the FDD is low.
1 Head Select (HD) signal to the FDD is high.

ST3

1 US1 —Unit Select 1.
0 Unit Select 1 (US1) signal to the FDD is low.
1 Unit Select 1 (US1) signal to the FDD is high.

ST3

0 US0 —Unit Select 0.
0 Unit Select 0 (US0) signal to the FDD is low.
1 Unit Select 0 (US1) signal to the FDD is high.

COMMAND SEQUENCE

The DDFDC is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer of data from the system. After command execution, the result of the command may be a multi-byte transfer of data back to the system. Because of this multi-byte transfer of information between the DDFDC and the system, each command consists of three phases:

Command Phase—The DDFDC receives all information required to perform a particular operation from the system.

Execution Phase—The DDFDC performs the instructed operation.

Result Phase—After completion of the operation, status and other housekeeping information are made available to the system.

The bytes of data sent to the DDFDC to form a command, and read out of the DDFDC in the result phase, must occur in the order shown for each command sequence. That is, the command code byte must be sent first followed by the other bytes in the specified sequence. All command bytes must be written and all result bytes must be read in each phase. After the last byte of data in the command phase is received by the DDFDC, the execution phase starts. Similarly, when the last byte of data is read out in the result phase, the command is ended and the DDFDC is ready to accept a new command. A command can be terminated by asserting the Terminal Count (TC) signal to the DDFDC. This ensures that the processor can always get the DDFDC's attention even if the command in process hangs up in an abnormal manner.

COMMAND DESCRIPTION

READ DATA

A command set of nine bytes places the DDFDC into the Read Data mode. After the Read Data command has been received the DDFDC loads the head (if it is unloaded), waits the specified Head Settling Time (defined in the Specify command), then begins reading ID Address Marks and ID fields from the disk. When the current sector number (R) stored in the ID Register (IDR) matches the sector number read from the disk, the DDFDC transfers data from the disk Data field to the data bus.

After completion of the read operation from the current sector, the DDFDC increments the Sector Number (R) by one, and the data from the next sector is read and output to the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Command terminates after reading the last data byte from sector R when R = EOT. ST0 bits 7 and 6 are set to 0 and 1, respectively, and ST1 bit 7 (EN) is set to a 1.

The Read Data command can also be terminated by a high Terminal Count (TC) signal. TC should be issued at the same time that the $\overline{\text{DACK}}$ for the last byte of data is sent. Upon receipt of TC, the DDFDC stops outputting data to the data bus, but continues to read data from the current sector, checks CRC (Cyclic Redundancy Count) bytes, and then at the end of that sector terminates the Read Data command and sets bits 7 and 6 in ST0

to 0. The amount of data which can be handled with a single command to the DDFDC depends upon MT (Multi-Track), MF (MFM/FM), and N (Number of Bytes/Sector) values. Table 3 shows the transfer capacity.

The multi-track function (MT) allows the DDFDC to read data from both sides of the disk. For a particular track, data is transferred starting at sector 1, side 0 and completed at sector L, side 1 (sector L = last sector on the side). This function pertains to only one track (the same track) on each side of the disk.

When N = 0 in command byte 6 (FM mode), the Data Length (DTL) in command byte 9 defines the data length that the DDFDC must treat as a sector. If DTL is smaller than the actual data length in a sector, the data beyond the DTL is not sent to the data bus. The DDFDC reads (internally) the complete sector, performs the CRC check, and depending upon the manner of command termination, may perform a multi-sector Read operation. When N is non-zero (MFM mode), DTL has no meaning and should be set to FF.

At the completion of the Read Data command, the head is not unloaded until the Head Unload Time (HUT) interval defined in the Specify command has elapsed. The head settling time may be avoided between subsequent reads if the processor issues another command before the head unloads. This time savings is considerable when disk contents are copied from one drive to another.

If the DDFDC detects the Index Hole twice in succession without finding the right sector (indicated in R), then the DDFDC sets the No Data (ND) flag in Status Register 1 (ST1) to a 1, sets Status Register 0 (ST0) bits 7 and 6 to 0 and 1, respectively, and terminates the Read Data command.

After reading the ID and Data fields in each sector, the DDFDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the DDFDC sets the Data Error (DE) flag in ST1 to a 1, sets the Data Error in Data Field (DD) flag in ST2 to a 1 if a CRC error occurs in the Data field, sets bits 7 and 6 in ST0 to 0 and 1, respectively, and terminates the command.

If the DDFDC reads a **Deleted Data Address Mark** from the disk, and the Skip Deleted Data Address Mark bit in the first command byte is not set (SK = 0), then the DDFDC reads all the data in the sector, sets the Control Mark (CM) flag in ST2 to a 1, and terminates the command. If SK = 1, the DDFDC skips the sector with the **Deleted Data Address Mark** and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers from the DDFDC to the system, the DDFDC must be serviced by the system within 27 μs in the FM mode, and within 13 μs in the MFM mode, otherwise the DDFDC sets the Over Run (OR) flag in ST1 to a 1, sets bits 7 and 6 in ST0 to 0 and 1, respectively, and terminates the command.

If the processor terminates a read (or write) operation in the DDFDC, then the ID information in the result phase is dependent upon the state of the MT bit in the first command byte and the End of Track (EOT) byte. Table 4 shows the values for Track Number (T), Head Number (H), Sector Number (R), and Number of Data Bytes/Sector (N), when the processor terminates the command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	0	0	1	1	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Table 3. DDFDC Transfer Capacity

Multi-Track (MT)	MFM/FM (MF)	Bytes/Sector (N)	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Disk
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

Table 4. DDFDC Command Termination Values

Command Phase ID		Final Sector Transferred to/from Data Bus	Result Phase ID			
Multi-Track (MT)	Head Number (HD)		Track Number (T)	Head Number (H)	Sector Number (R)	No. of Data Bytes (N)
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	T + 1	NC	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	T + 1	NC	01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	T + 1	LSB	01	NC

Notes:
1. NC (No Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

WRITE DATA

A command set of nine bytes places the DDFDC in the Write Data mode. After the Write Data command has been received the DDFDC loads the head (if it is unloaded), waits the specified Head Settling Time (defined in the Specify command), then begins reading ID fields from the disk. When the four bytes (T, H, R, N) loaded during the command match the four bytes of the ID field from the disk, the DDFDC transfers data from the data bus to the disk Data field.

After writing data into the current sector, the DDFDC increments the sector number (R) by one, and writes into the Data field in the next sector. The DDFDC continues this multi-sector write operation until the last byte is written to sector R when R = EOT. ST0 bits 7 and 6 are set to 0 and 1, respectively, and ST1 bit 7 (EN) is set to a 1.

The command can also be terminated by a high on Terminal Count (TC). If TC is sent to the DDFDC while writing into the current sector, then the remainder of the Data field is filled with 00 (zeros). In this case, ST0 bits 7 and 6 are set to 0 and the command is terminated.

The DDFDC reads the ID field of each sector and checks the CRC bytes. If the DDFDC detects a read error (incorrect CRC) in one of the ID fields, it terminates the Write Data command, sets the DE flag in ST1 to a 1, and sets bits 7 and 6 in ST0 to 0 and 1, respectively.

The Write Data command operates in much the same manner as the Read Data command. Refer to the Read Data command for the handling of the following items:

- Transfer Capacity
- End of Track (EN) flag
- No Data (ND) flag
- Head Unload Time (HUT) interval
- ID information when the processor terminates command (see Table 4)
- Definition of Data Length (DTL) when N = 0 and when N ≠ 0

In the Write Data mode, data transfers from the data bus to the DDFDC must occur within 27 μs in the FM mode, and within 13 μs in the MFM mode. If the time interval between data transfers is longer than this, then the DDFDC terminates the Write Data command, sets the Over Run (OR) flag in ST1 to a 1, and sets bits 7 and 6 in ST0 to 0 and 1, respectively.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	0	0	0	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

WRITE DELETED DATA

The Write Deleted Data command is the same as the Write Data command except a Deleted Data Address Mark is written at the beginning of the Data field instead of the normal Data Address Mark.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	0	0	1	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector(N)

READ DELETED DATA

The Read Deleted Data command is the same as the Read Data command except that if SK = 0 when the DDFDC detects a **Data Address Mark** at the beginning of a Data field, it reads all the data in the sector and sets the CM flag in ST2 to a 1, and then terminates the command. If SK = 1, then the DDFDC skips the sector with the **Data Address Mark** and reads the next sector.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	0	1	1	0	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

READ A TRACK

The Read a Track command is similar to the Read Data command except that this is a continuous read operation where all Data fields from each of the sectors on a track are read and transferred to the data bus. Immediately after encountering the Index Hole, the DDFDC starts reading the Data fields as continuous blocks of data. This command terminates when the number of sectors read is equal to EOT. Multi-track operations are not allowed with this command.

If the DDFDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track. The DDFDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag in ST1 to a 1 if there is no match.

If the DDFDC does not find an ID Address Mark on the disk after it encounters the Index Hole for the second time it terminates the command, sets the Missing Address Mark (MA) flag in ST1 to a 1, and sets bits 7 and 6 of ST0 to 0 and 1, respectively.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	SK	0	0	0	1	0
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Data Length (DTL)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

READ ID

The two-byte Read ID command returns the present position of the read/write head. The DDFDC obtains the value from the first ID field it is able to read, sets bits 7 and 6 in ST0 to 0 and terminates the command.

If no proper ID Address Mark is found on the disk before the Index Hole is encountered for the second time then the Missing Address Mark (MA) flag in ST1 is set to a 1, and if no data is found then the ND flag in ST1 is also set to a 1. Bits 7 and 6 in ST0 are set to 0 and 1, respectively and the command is terminated.

During this command there is no data transfer between DDFDC and the data bus except during the result phase.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	0	0	1	0	1	0
	2	X	X	X	X	X	HD	US1	US0

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

FORMAT A TRACK

The six-byte Format a Track command formats an entire track. After the Index Hole is detected, data is written on the disk: Gaps, Address Marks, ID fields and Data fields; all are recorded in either the double-density IBM System 34 format (MF = 1) or the single-density IBM 3740 format (MF = 0). The particular format written is also controlled by the values of Number of Bytes/Sector (N), Sectors/Track (ST), Gap Length (GPL) and Data Pattern (D) which are supplied by the processor during the command phase. The Data field is filled with the data pattern stored in D.

The ID field for each sector is supplied by the processor in response to four data requests per sector issued by the DDFDC. The type of data request depends upon the Non-DMA flag (ND) in the Specify command. In the DMA mode (ND = 0), the DDFDC asserts the DMA Request (DRQ) output four times per sector. In the Non-DMA mode (ND = 1), the DDFDC asserts Interrupt Request (INT) output four times per sector.

The processor must write one data byte in response to each request, sending (in the consecutive order) the Track Number (T), Head Number (H), Sector Number (R) and Number of Bytes/Sector (N). This allows the disk to be formatted with non-sequential sector numbers, if desired.

The processor must send new values for T, H, R, and N to the DDFDC for each sector on the track. For sequential formatting R is incremented by one after each sector is formatted, thus, R contains the total numbers of sectors formatted when it is read during the result phase. This incrementing and formatting continues for the whole track until the DDFDC, upon encountering the Index Hole for the second time, terminates the command and sets bits 7 and 6 in ST0 to 0.

If the Fault (FLT) signal is high from the FDD at the end of a write operation, the DDFDC sets the Equipment Check (EC) flag in ST0 to a 1, sets bits 7 and 6 of ST0 to 0 and 1, respectively, and terminates the command. Also, a low (RDY) signal at the beginning of a command execution phase causes bits 7 and 6 of ST0 to be set to 0 and 1, respectively.

Table 5 shows the relationship between N, ST, and GPL for various disk and sector sizes.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	MF	0	0	1	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Number of Bytes per Sector (N)							
	4	Sectors per Track (ST)							
	5	Gap Length (GPL)							
	6	Data Pattern (D)							

Table 5. Standard Floppy Disk Sector Size Relationship

Disk Size	Mode	Sector Size Bytes/Sector	No. of Data Bytes/Sector (N)	No. of Sectors/Track (ST)	Gap Length (GPL)[4]		Remarks
					Read/Write Command[1]	Format Command[2]	
8″	FM	128	00	1A	07	1B	
		256	01	0F	0E	2A	
		512	02	08	1B	3A	
		1024	03	04	47	8A	
		2048	04	02	C8	FF-	
		4096	05	01	C8	FF	
	MFM[3]	256	01	1A	0E	36	
		512	02	0F	1B	54	
		1024	03	08	35	74	
		2048	04	04	99	FF	
		4096	05	02	C8	FF	
		8192	06	01	C8	FF	
5¼″	FM	128	00	12	07	09	
		128	00	10	10	19	
		256	01	08	18	30	
		512	02	04	46	87	
		1024	03	02	C8	FF	
		2048	04	01	C8	FF	
	MFM[3]	256	01	12	0A	0C	
		256	01	10	20	32	
		512	02	08	2A	50	
		1024	03	04	80	F0	
		2048	04	02	C8	FF	
		4096	05	01	C8	FF	

Notes:
1. Suggested values of GPL in Read or Write commands to avoid overlapping between Data field and ID field of contiguous sections.
2. Suggested values of GPL in Format a Track command.
3. In MFM mode the DDFDC cannot perform a read/write/format operation with 128 bytes/sector (N = 00).
4. Values of ST and GPL are in hexadecimal.

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)*
	5	Head Number (H)*
	6	Sector Number (R)*
	7	Number of Data Bytes per Sector (N)*

* The ID information has no meaning in this command.

SCAN COMMANDS

The scan commands compare data read from the disk to data supplied from the data bus. The DDFDC compares the data, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{BUS}$, $D_{FDD} \leq D_{BUS}$, or $D_{FDD} \geq D_{BUS}$ (D = the data pattern in hexadecimal). A magnitude comparison is performed (FF = largest number, 00 = smallest number). The hexadecimal byte of FF either from the bus or from FDD can be used as a mask byte because it always meets the condition of the compare. After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following events occur: the conditions for scan are met (equal, low or equal, or high or equal), the last sector on the track is reached (EOT), or TC is received.

If conditions for scan are met, the DDFDC sets the Scan Hit (SH) flag in ST2 to a 1, and terminates the command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the track (EOT), then the DDFDC sets the Scan Not Satisfied (SN) flag in ST2 to a 1, and terminates the command. The receipt of TC from the processor or DMA controller during the scan operation will cause the DDFDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 6 shows the status of bits SH and SN under various conditions of scan.

Table 6. Scan Status Codes

Command	Status Register 2		Comments
	Bit 2 = SN	Bit 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{BUS}$
	1	0	$D_{FDD} \oplus D_{BUS}$
Scan Low or Equal	0	1	$D_{FDD} = D_{BUS}$
	0	0	$D_{FDD} < D_{BUS}$
	1	0	$D_{FDD} > D_{BUS}$
Scan High or Equal	0	1	$D_{FDD} = D_{BUS}$
	0	0	$D_{FDD} > D_{BUS}$
	1	0	$D_{FDD} < D_{BUS}$

If SK = 0 and the DDFDC encounters a Deleted Data Address Mark on one of the sectors, it regards that sector as the last sector of the track, sets the Control Mark (CM) bit in ST2 to a 1 and terminates the command. If SK = 1, the DDFDC skips the sector with the Deleted Data Address Mark, sets the CM flag to a 1 in order to show that a Deleted Sector has been encountered, and reads the next sector.

When either the STP sectors are read (contiguous sectors = 01, or alternate sectors = 02) or MT (Multi-Track) is set, **the last sector on the track must be read.** For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and the scan command starts reading at sector 21. Sectors 21, 23, and 25 are read, then the next sector (26) is skipped and the Index Hole is encountered before the EOT value of 26 can be read. This results in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the scan command would be completed in a normal manner.

During a scan command data is supplied from the data bus for comparison against the data read from the disk. In order to avoid having the Over Run (OR) flag set in ST1, data must be available from the data bus in less than 27 μs (FM mode) or 13 μs (MFM mode). If an OR occurs, the DDFDC terminates the command and sets bits 7 and 6 of ST0 to 0 and 1, respectively.

The following tables specify the command bytes and describe the result bytes for the three scan commands.

SCAN EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	0	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R		
	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SCAN LOW OR EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	1	0	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R		
	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SCAN HIGH OR EQUAL

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	MT	MF	SK	1	1	1	0	1
	2	X	X	X	X	X	HD	US1	US0
	3	Track Number (T)							
	4	Head Number (H)							
	5	Sector Number (R)							
	6	Number of Data Bytes per Sector (N)							
	7	End of Track (EOT)							
	8	Gap Length (GPL)							
	9	Sector Test Process (STP)							

Result Phase:

R	1	Status Register 0 (ST0)
	2	Status Register 1 (ST1)
	3	Status Register 2 (ST2)
	4	Track Number (T)
	5	Head Number (H)
	6	Sector Number (R)
	7	Number of Data Bytes per Sector (N)

SEEK

The three-byte Seek command steps the FDD read/write head from track to track. The DDFDC has four independent Present Track Registers for each drive. They are cleared only by the Recalibrate command. The DDFDC compares the Present Track Number (PTN) which is the current head position with the New Track Number (NTN), and if there is a difference, performs the following operation:

If PTN < NTN: Sets the direction output (LCT/DIR) high and issues step pulses (FR/STP) to the FDD to cause the read/write head to step in.

If PTN > NTN: Sets the direction output (LCT/DIR) low and issues step pulses to the FDD to cause the read/write head to step out.

The rate at which step pulses are issued is controlled by the Step Rate Time (SRT) in the Specify command. After each step pulse is issued, NTN is compared against PTN. When NTN = PTN, then the Seek End (SE) flag in ST0 is set to a 1, bits 7 and 6 in ST0 are set to 0, and the command is terminated. At this point DDFDC asserts INT.

The FDD Busy flag (bit 0-3) in the Main Status Register (MSR) corresponding to the FDD performing the Seek operation is set to a 1.

After command termination, all FDD Busy bits set are cleared by the Sense Interrupt Status command.

During the command phase of the Seek operation the DDFDC sets the Controller Busy (CB) flag in the MSR to 1; but during the execution phase the CB flag is set to 0 to indicate DDFDC non-busy. While the DDFDC is in the non-busy state, another Seek command may be issued, and in this manner parallel seek operations may be performed on all drives at once.

No command other than Seek will be accepted while the DDFDC is sending step pulses to any FDD. If a different command type is attempted, the DDFDC will set bits 7 and 6 in ST0 to a 1 and 0, respectively, to indicate an invalid command.

If the FDD is in a not ready state at the beginning of the command execution phase or during the seek operation, then the DDFDC sets the Not Ready (NR) flag in ST0 to a 1, sets ST0 bits 7 and 6 to 0 and 1, respectively, and terminates the command.

If the time to write the three bytes of the Seek command exceeds 150 μs, the time between the first two step pulses may be shorter than the Step Rate Time (SRT) defined by the Specify command by as much as 1 ms.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	1	1	1	1
	2	X	X	X	X	X	0	US1	US0
	3	New Track Number (NTN)							

Result Phase: None.

RECALIBRATE

This two-byte command retracts the FDD read/write head to the Track 0 position. The DDFDC clears the contents of the PTN counters, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal (TRK0) is low, the direction signal (LCT/DIR) output remains low and step pulses are issued on FR/STP. When TRK0 goes high the DDFDC sets the Seek End (SE) flag in ST0 to a 1 and terminates the command. If the TRK0 is still low after 256 step pulses have been issued, the DDFDC sets Seek End (SE) and Equipment Check (EC) flags in ST0 to 1s, sets bits 7 and 6 of ST0 to 0 and 1, respectively, and terminates the command.

The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the RDY signal, as described in the Seek command, also applies to the Recalibrate command.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	1	1	1
	2	X	X	X	X	X	0	US1	US0

Result Phase: None.

SENSE INTERRUPT STATUS

Interrupt Request (INT) is asserted by the DDFDC when any of the following conditions occur:

1. Upon entering the result phase of:
   a. Read Data command
   b. Read a Track command
   c. Read ID command
   d. Read Deleted Data command
   e. Write Data command
   f. Format a Track command
   g. Write Deleted Data command
   h. Scan commands
2. Ready (RDY) line from the FDD changes state
3. Seek or Recalibrate command termination
4. During execution phase in the Non-DMA mode

INT caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in Non-DMA mode, bit 5 in the MSR is set to 1. Upon entering result phase this bit is set to 0. Reasons 1 and 4 do not require the Sense Interrupt Status command. The interrupt is cleared by reading or writing data to DDFDC. Interrupts caused by reasons 2 and 3 are identified with the aid of the Sense Interrupt Status command. This command resets INT and sets/resets bits 5, 6, and 7 of ST0 to identify the cause of the interrupt. Table 7 defines the seek and interrupt codes.

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no result phase. When the disk drive has reached the desired head position the DDFDC asserts interrupt output. The host CPU must then issue a Sense Interrupt Status command to determine the actual cause of the interrupt, which could be Seek End or a change in ready status from one of the drives (see example in Figure 4).

Issuing a Sense Interrupt Status command without an interrupt pending is treated as an invalid command.

Table 7. ST0 Seek and Interrupt Code Definition for Sense Interrupt Status

Status Register 0 (ST0) Bits			
Interrupt Code (IC)		Seek End (SE)	Cause
7	6	5	
1	1	0	RDY line changed state, either polarity
0	0	1	Normal termination of Seek or Recalibrate command
0	1	1	Abnormal termination of Seek or Recalibrate command

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	1	0	0	0

Result Phase:

R	1	Status Register 0 (ST0)
	2	Present Track Number (PTN)

SPECIFY

The three-byte Specify command sets the initial values for each of the three internal timers. The Head Unload Time (HUT) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (1 = 16 ms, 2 = 32 ms,...F = 240 ms).

The Step Rate Time (SRT) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms,... 0 = 16 ms.)

The Head Load Time (HLT) defines the time between the Head Load (HDL) signal going high and the start of the read/write operation. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms,... 7F = 254 ms).

The time intervals are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock. If the clock is reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of two.

The choice of DMA or Non-DMA operation is made by the Non-DMA mode (ND) bit. When this bit = 1 the Non-DMA mode is selected, and when ND = 0 the DMA mode is selected.

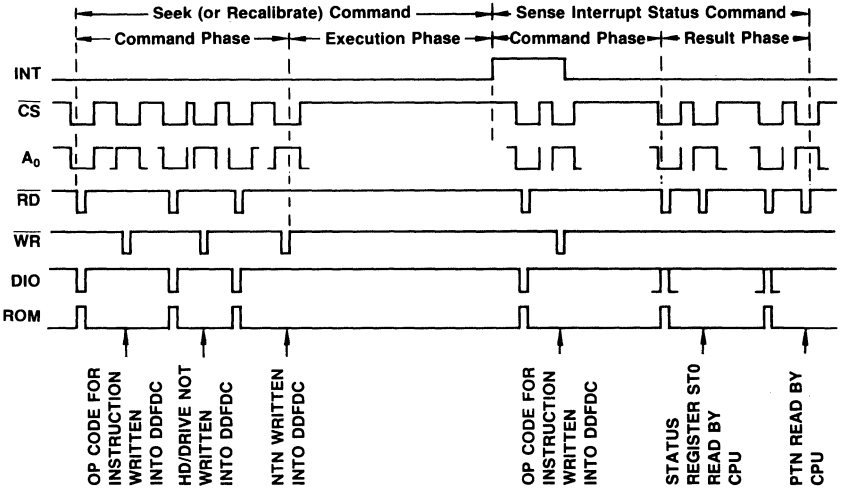
Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	0	1	1
	2	SRT				HUT			
	3	HLT							ND

SRT — Step Rate Time
HUT — Head Unload Time
HLT — Head Load Time
ND — Non-DMA mode

Result Phase: None.

Figure 4. Sense Interrupt Status



SENSE DRIVE STATUS

This two-byte command obtains and reports the status of the FDDs. Status Register 3 (ST3) is returned in the result phase and contains the drive status.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	0	0	0	0	0	1	0	0
	2	X	X	X	X	X	HD	US1	US0

Result Phase:

R	1	Status Register 3 (ST3)

INVALID COMMAND

If an invalid command (i.e., a command not previously defined) is received by the DDFDC, then the DDFDC terminates the command after setting bits 7 and 6 of ST0 to 1 and 0, respectively. The DDFDC does not generate an interrupt during this condition. Bits 6 and 7 (DIO and RQM) in the MSR are both set to a 1 indicating to the processor that the DDFDC is in the result phase and that ST0 must be read. A hex 80 in ST0 indicates that an invalid command was received.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate interrupt, otherwise the DDFDC considers the next command to be an invalid command.

In some applications the user may wish to use this command as a No-Op command, to place the DDFDC in a standby or no operation state.

Command Phase:

R/W	BYTE	7	6	5	4	3	2	1	0
W	1	Invalid Codes							

Result Phase:

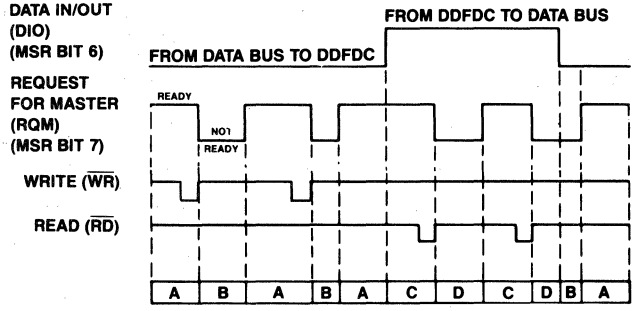
R	1	Status Register 0 (ST0) = 80

PROCESSOR INTERFACE

During the command or result phases, the Main Status Register (MSR) must be read by the processor before each byte of information is transferred to, or from, the DDFDC Data Register. After each byte of data is written to, or read from, the Data Register, the processor should wait 12 μs before reading the MSR. Bits 6 and 7 in the MSR must be a 0 and 1, respectively, before each command byte can be written to the DDFDC. During the result phase, bits 6 and 7 of the MSR must both be 1s prior to reading each byte from the Data Register onto the data bus. Note that this status reading of bits 6 and 7 of the MSR before each byte transfer to and from the DDFDC is required in only the command and result phases and not during the execution phase.

During the result phase all bytes shown in the result phase must be read by the processor. The Read Data command, for example, has seven bytes of data in the result phase. All seven bytes must be read to successfully complete the Read Data command. The DDFDC will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the result phase.

Figure 5. DDFDC and System Data Transfer Timing



NOTES

A DATA REGISTER READY TO BE WRITTEN INTO

B DATA REGISTER NOT READY TO BE WRITTEN INTO

C DATA REGISTER READY FOR NEXT DATA BYTE TO BE READ

D DATA REGISTER NOT READY FOR NEXT DATA BYTE TO BE READ

INTERRUPT REQUEST MODE

During the execution phase, the MSR need not be read. The receipt of each data byte from the FDD is indicated by INT high on pin 18. When the DDFDC is in Non-DMA mode, INT is asserted during the execution phase. When the DDFDC is in the DMA mode, INT is asserted at the result phase. The INT signal is reset by a read ($\overline{RD}$ low) or write ($\overline{WR}$ low) of data to the DDFDC. A further explanation of the INT signal is described in the Sense Interrupt Status command on page 16. If the system cannot handle interrupts fast enough (within 13 μs for MFM mode or 27 μs for FM mode), it should poll bit 7 (RQM) in the MSR. In this case, RQM in the MSR functions as an Interrupt Request (INT). If the RQM bit is not set, the Over Run (OR) flag in ST1 will be set to a 1 and bits 7 and 6 of ST0 will be set to a 0 and 1, respectively.

DMA MODE

When the DDFDC is in the DMA mode (ND = 0 in the third command byte of the Specify command), DRQ (DMA Request) is asserted during the execution phase (rather than INT) to request the transfer of a data byte between the data bus and the DDFDC.

During a read command, the DDFDC asserts DRQ as each byte of data is available to be read. The DMA controller responds to this request with $\overline{DACK}$ low (DMA Acknowledge) and $\overline{RD}$ low (read). When $\overline{DACK}$ goes low the DMA Request is reset (DRQ low). After the execution phase has been completed (TC high or the EOT sector is read), INT is asserted to indicate the beginning of the result phase. When the first byte of data is read during the result phase, INT is reset low.

During a write command, the DDFDC asserts DRQ as each byte of data is required. The DMA controller responds to this request with $\overline{DACK}$ (DMA Acknowledge) and $\overline{WR}$ low (write). When DACK goes low the DMA Request is reset (DRQ low). After the execution phase has been completed (TC high or the EOT sector is written), INT is asserted. This signals the beginning of the result phase. When the first byte of data is read during the result phase, the INT is reset low.

FDD POLLING

After the Specify command has been received by the DDFDC, the Unit Select lines (US0 and US1) begin the polling mode. Between commands (and between step pulses in the Seek Command) the DDFDC polls all the FDD's looking for a change in the RDY line from any of the drives. If the RDY line changes state (usually due to the door opening or closing) then the DDFDC asserts INT. When Status Register 0 (ST0) is read (after Sense Interrupt Status command is issued), Not Ready (NR = 1) will be indicated. The polling of the RDY line by the DDFDC occurs continuously between commands, thus notifying the processor which drives are on- or off-line. Each drive is polled every 1.024 ms except during read/write commands.

Figure 6. DDFDC Formats

FM MODE

FIELD	GAP 4a	SYNC	IAM	GAP 1	SYNC	IDAM	CYL	HD	SEC	NO	CRC	GAP 2	SYNC	DATA AM	DATA		GAP 3	GAP 4b
NO. OF BYTES	40x	6x		26x	6x							11x	6x		①	CRC	①	
DATA	FF	00	FC	FF	00	FE						FF	00	FB OR F8				

MFM MODE

GAP 4a	SYNC	IAM		GAP 1	SYNC	IDAM		CYL	HD	SEC	NO	CRC	GAP 2	SYNC	DATA AM		DATA		GAP 3	GAP 4b
80x	12x	3x		50x	12x	3x							22x	12x	3x	FB	①	CRC	①	
4E	00	C2	FC	4E	00	A1	FE						4E	00	A1	F8				

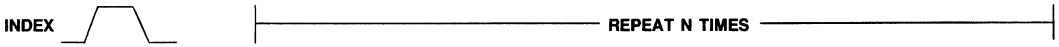


Figure 7. DDFDC Formats

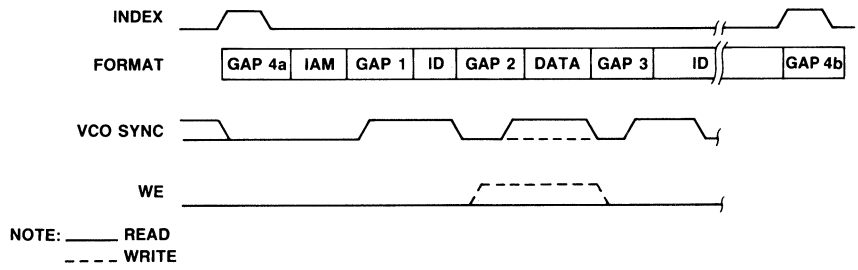


Figure 8. VL6765 DDFDC Interface to Z80

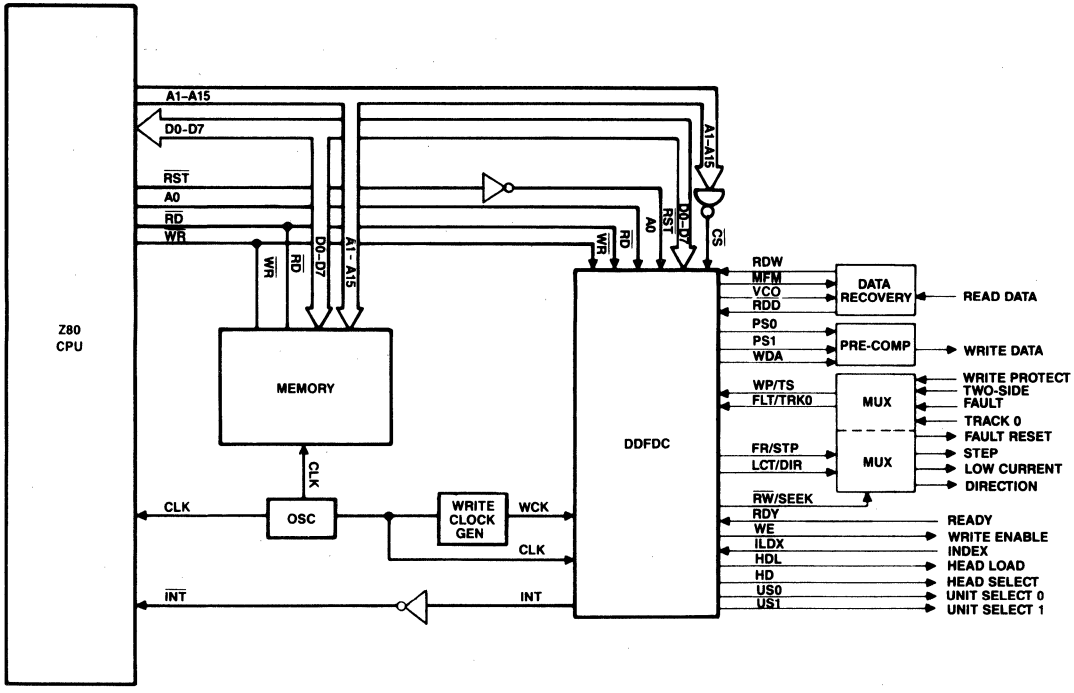


Figure 9. Clock Timing

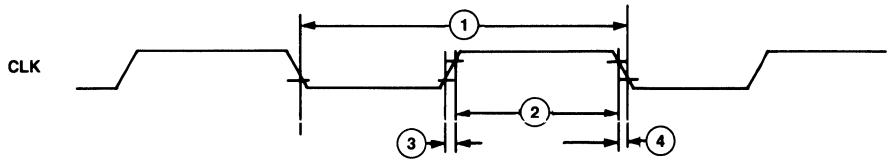


Figure 10. Read Cycle Timing

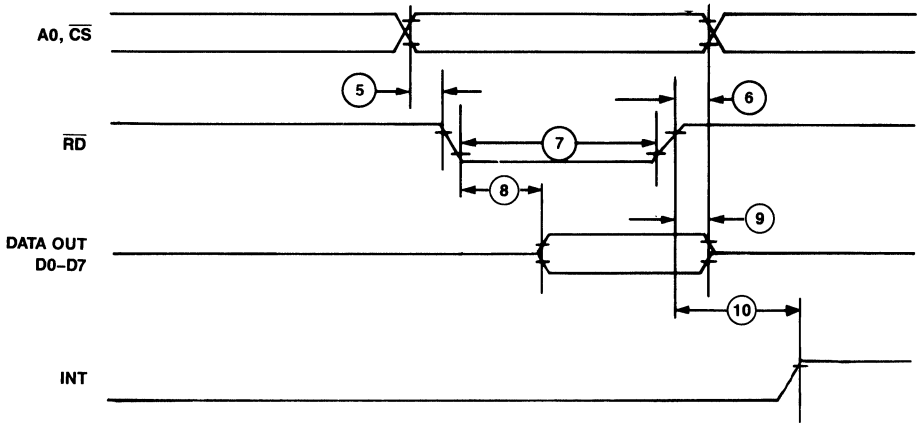


Figure 11. Write Cycle Timing

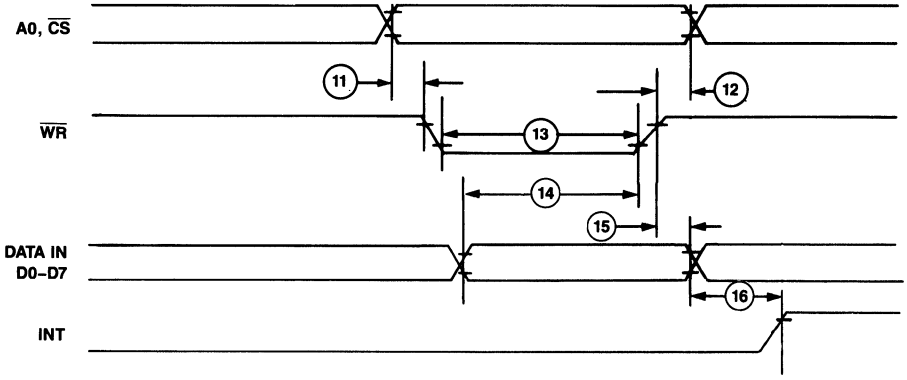


Figure 12. DMA Operation Timing

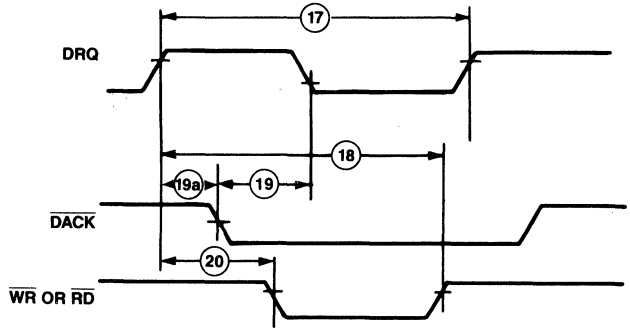


Figure 13. FDD Write Operation Timing

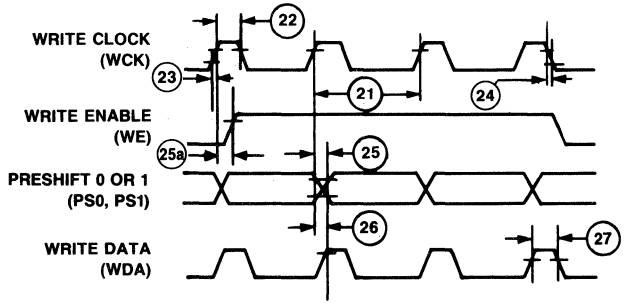
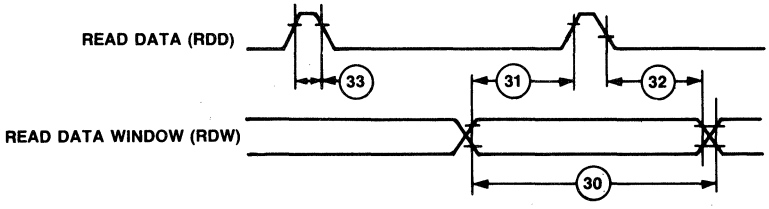


Figure 14. FDD Read Operation Timing



NOTE:
EITHER POLARITY DATA WINDOW IS VALID

Figure 15. Seek Operation Timing

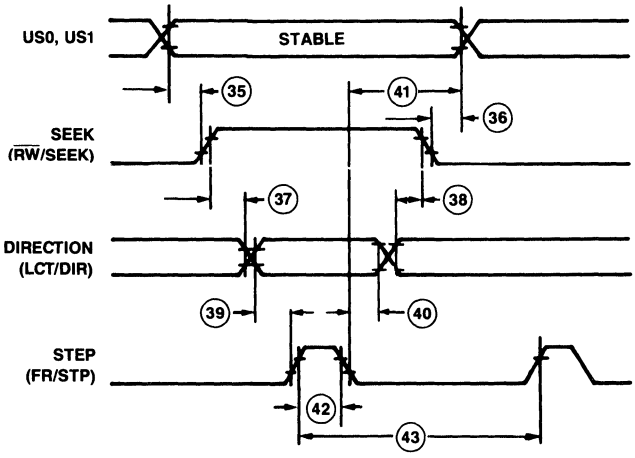


Figure 16. Fault Reset Timing

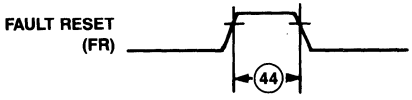


Figure 17. Index Timing

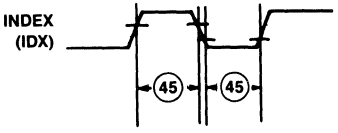


Figure 18. Terminal Count Timing

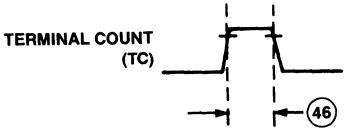


Figure 19. Reset Timing

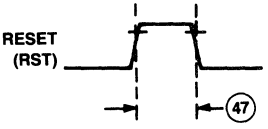
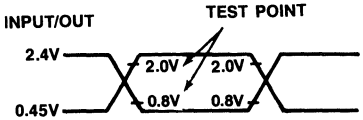
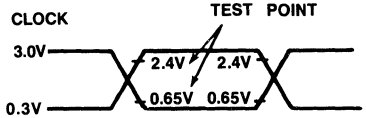


Figure 20. AC Timing Measurement Conditions



INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45 V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0."



CLOCKS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0.3V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 2.4V FOR A LOGIC "1" AND 0.65V FOR A LOGIC "0."

AC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C)

Ref. Fig.	No.	Characteristic		Symbol	Alt. Sym.	Min.	Typ.	Max.	Unit	Test Conditions
	1	Clock Period	(8″ or 3-1/2″ FDD)	t_{CY}	ϕ_{CY}	120	125	500	ns	CLK = 8 MHz
			(5-1/4″ FDD)			—	250	—	ns	CLK = 4 MHz
8	2	Clock High		t_{CA}	ϕ_O	40	—	—	ns	CLK = 8 MHz
	3	Clock Rise Time		t_{CLCH}	ϕ_r	—	—	20	ns	
	4	Clock Fall Time		t_{CHCL}	ϕ_f	—	—	20	ns	
9	5	A0, $\overline{CS}$, $\overline{DACK}$ Valid to $\overline{RD}$ Low (Setup)		t_{SLRL}	t_{AR}	0	—	—	ns	
	6	$\overline{RD}$ High to A0, $\overline{CS}$, $\overline{DACK}$ Invalid (Hold)		t_{RHSH}	t_{RA}	0	—	—	ns	
	7	$\overline{RD}$ Low Width		t_{RLRH}	t_{RR}	250	—	—	ns	
	8	$\overline{RD}$ Low to Data Valid (Access)		t_{RLDV}	t_{RD}	—	—	200	ns	C_L = 100 pF
	9	$\overline{RD}$ High to Output High Z		t_{RHDZ}	t_{DF}	20	—	100	ns	
	10	$\overline{RD}$ High to INT High		t_{RHIH}	t_{RI}	—	—	500	ns	CLK = 8 MHz
10	11	A0, $\overline{CS}$, $\overline{DACK}$ Valid to $\overline{WR}$ Low (Setup)		t_{SLWL}	t_{AW}	0	—	—	ns	
	12	$\overline{WR}$ High to A0, $\overline{CS}$, $\overline{DACK}$ Invalid (Hold)		t_{WHSH}	t_{WA}	0	—	—	ns	
	13	$\overline{WR}$ Low Width		t_{WLWH}	t_{WW}	250	—	—	ns	
	14	Data Valid to $\overline{WR}$ High (Setup)		t_{DVWH}	t_{DW}	150	—	—	ns	
	15	$\overline{WR}$ High to Data Invalid (Hold)		t_{WHDX}	t_{WD}	5	—	—	ns	
	16	$\overline{WR}$ High to INT High		t_{WHIH}	t_{WI}	—	—	500	ns	
11	17	DRQ Cycle Time		t_{QCY}	t_{MCY}	13	—	—	μs	CLK = 8 MHz
	18	DRQ High to $\overline{RD}$, $\overline{WR}$ High (Response)		t_{QHXH}	t_{MRW}	—	—	12	μs	
	19	$\overline{DACK}$ Low to DRQ Low (Delay)		t_{ALQL}	t_{AM}	—	—	200	ns	
	19a	DRQ High to $\overline{DACK}$ Low (Delay)		t_{QHAL}	t_{MA}	200	—	—	ns	t_{CY} = 125 ns
	20	DRQ High to $\overline{RD}$ Low (Delay)		t_{QHRL}	t_{MR}	800	—	—	ns	CLK = 8 MHz
		DRQ High to $\overline{WR}$ Low (Delay)		t_{QHWL}	t_{MW}	250	—	—	ns	
12	21	WCK Cycle Time	(8″ or 3-1/2″ FDD)	t_{KCY}	t_{CY}	—	2	—	μs	MFM = 0
						—	1	—	μs	MFM = 1
			(5-1/4″ FDD)			—	4	—	μs	MFM = 0
						—	2	—	μs	MFM = 1
	22	WCK High Width		t_{KHKL}	t_0	80	250	350	ns	
	23	WCK Rise Time		t_{KLKH}	t_r	—	—	20	ns	
	24	WCK Fall Time		t_{KHKL}	t_f	—	—	20	ns	
	25	WCK High to PS0, PS1 Valid (Delay)		t_{KHPV}	t_{CP}	20	—	100	ns	
	25a	WCK High to WE High (Delay)		t_{DHEN}	t_{CWE}	20	—	100	ns	
	26	WCK High to WDA High		t_{PVDH}	t_{CD}	20	—	100	ns	
	27	WDA High Width		t_{DHDL}	t_{WDD}	t_{KHKL} − 50	—	—	ns	
13	30	RDW Cycle Time	(8″ or 3-1/2″ FDD)	t_{WCY}	t_{WCY}	—	2	—	μs	MFM = 0
						—	1	—	μs	MFM = 1
			(5-1/4″ FDD)			—	4	—	μs	MFM = 0
						—	2	—	μs	MFM = 1
	31	RDW Valid to RDD High (Setup)		t_{WVRH}	t_{WRD}	15	—	—	ns	
	32	RDD Low to RDW Invalid (Hold)		t_{RLWI}	t_{RDW}	15	—	—	ns	
	33	RDD High Width		t_{RHRL}	t_{RDD}	40	—	—	ns	
14	35	US0, US1 Valid to SEEK High (Setup)		t_{UVSH}	t_{US}	12	—	—	μs	CLK = 8 MHz
	36	SEEK Low to US0, US1 Invalid (Hold)		t_{SLUI}	t_{SU}	15	—	—	μs	
	37	SEEK High to DIR Valid (Setup)		t_{SHDV}	t_{SD}	7	—	—	μs	
	38	DIR Invalid to SEEK Low (Hold)		t_{DXSL}	t_{DS}	30	—	—	μs	
	39	DIR Valid to STP High (Setup)		t_{DVTH}	t_{DST}	1	—	—	μs	
	40	STP Low to DIR Invalid (Hold)		t_{TLDX}	t_{STD}	24	—	—	μs	
	41	STP Low to US0, US1 Invalid (Hold)		t_{TLUX}	t_{STU}	5	—	—	μs	
	42	STP High Width		t_{THTL}	t_{STP}	6	7	8	μs	
	43	STP Cycle Time		t_{TCY}	t_{SC}	33[3]	—	note 1	μs	
15	44	FR High Width		t_{FHFL}	t_{FR}	8	—	10	μs	
16	45	IDX High Width		t_{IHIL}	t_{IDX}	10	—	—	t_{CY}	
17	46	TC High Width		t_{THTL}	t_{TC}	1	—	—	t_{CY}	
18	47	RST High Width		t_{RHRL}	t_{RST}	14	—	—	t_{CY}	

1. t_{SC} = 33 μs min. is for different drive units. In the case of the same unit, t_{SC} can range from 1 ms to 16 ms with 8 MHz clock period, and 2 ms to 32 ms with 4 MHz clock, under software control.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{IN}	−0.3 to +7.0	V
Output Voltage	V_{OUT}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	C°
Storage Temperature Range	T_{STG}	−55 to +150	C°

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Range
V_{CC} Power Supply	5.0V ±5%
Operating Temperature	0°C to 70°C

DC CHARACTERISTICS

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C, unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}			V	
Logic		−0.5	0.8		
CLK and WCK		−0.5	0.65		
Input High Voltage	V_{IH}			V	
Logic		2.0	V_{CC} + 0.5		
CLK and WCK		2.4	V_{CC} + 0.5		
Output Low Voltage	V_{OL}		0.45	V	V_{CC} = 4.75V, I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4	V_{CC}	V	V_{CC} = 4.75V, I_{OH} = −200 μA
V_{CC} Supply Current	I_{CC}		150	mA	V_{CC} = 4.75V
Input Load Current	I_{IL}		10	μA	V_{IN} = V_{CC}
All Inputs			−10	μA	V_{IN} = 0V
High Level Output Leakage Current	I_{LOH}		10	μA	V_{CC} = 0V to 5.25V, V_{SS} = 0V V_{OUT} = V_{CC}
Low Level Output Leakage Current	I_{LOL}		−10	μA	V_{CC} = 0V to 5.25V, V_{SS} = 0V V_{OUT} = +0.45V
Internal Power Dissipation	P_{INT}	—	1.0	W	T_A = 25°C

CAPACITANCE

(T_A = 25°C; f_c = 1 MHz; V_{CC} = 0V)

Parameter	Symbol	Max Limit	Unit
Clock Input	$C_{IN(\phi)}$	20	pF
Input	C_{IN}	10	pF
Output	C_{OUT}	20	pF

Note: All pins except pin under test tied to ground.

VL6845R/E • VL68C45R/S

VL6845 CRT CONTROLLER FAMILY AND VMC68C45 MEGACELL DESIGN KIT

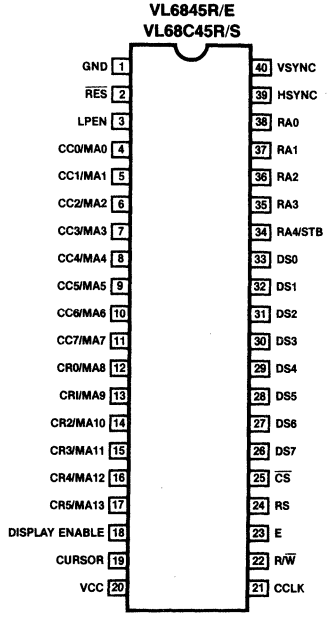
FEATURES

- CRT Controller Family—
  Rev E compatibility with SY6845E
  Rev R compatibility with MC6845
  CMOS versions available:
  CMOS Rev R compatible with MC6845R1, MC6845 and MC146845 CMOS Rev S compatible with HD6845S
- Internal refresh address generation
- Character clocks up to 5 MHz
- Bus clocks up to 3 MHz

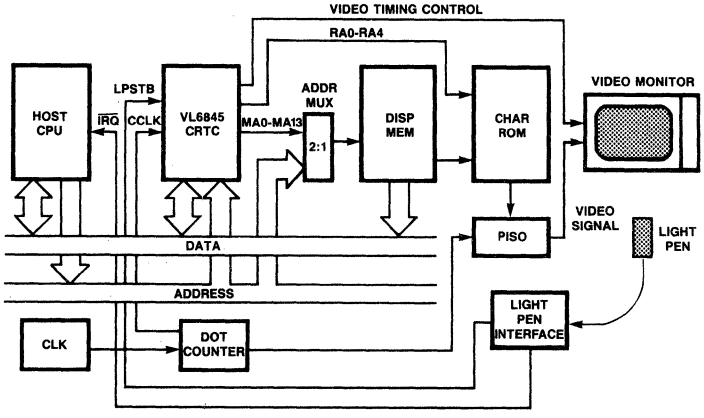
DESCRIPTION

The VL6845X and VL68C45X are a family of CRT controllers that are widely used in both bit-mapped and character-mapped applications for both terminals and personal computers. The VL6845 family offers compatibility with the Motorola family of HMOS controllers while the VL68C45 family allows designs to consume less power through the use of CMOS technology. In addition to compatibility with both the Motorola and Hitachi families, the VL68C45R also contains enhancements found in the MC6845R1. These enhancements allow for higher resolution displays without extra external hardware.

PIN DIAGRAM



SYSTEM DIAGRAM



ORDER INFORMATION

Part Number	Clock Frequency		Part Number	Clock Frequency		Package
	Bus	Character		Bus	Character	
VL6845R-23 VL68C45R-23 VL68C45S-23	2 MHz	3 MHz	VL6845E-33 VL6845R-33 VL68C45R-33 VL68C45S-33	3 MHz	3 MHz	To specify package type, add the appropriate suffix to the part number: PC = Plastic DIP CC = Ceramic DIP QC = Plastic Leaded Chip Carrier (PLCC)
VL6845E-24 VL6845R-24 VL68C45R-24 VL68C45S-24		4 MHz	VL6845E-34 VL6845R-34 VL68C45R-34 VL68C45S-34		4 MHz	
			VL6845R-35 VL68C45R-35 VL68C45S-35		5 MHz	

Note: Operating temperature range: 0°C to +70°C.

PIN DESCRIPTIONS

Pin	Pin Number	Pin Name	Description
MPU Interface			
E	23	Enable	Input that is used as a data strobe; does not have to be a free-running clock. This capability allows the VL6845 to interface with other non-6800/6500-type microprocessors.
R/$\overline{W}$	22	Read/$\overline{\text{Write}}$ Control	Input that, when HIGH, allows the processor to read the data supplied by the VL6845; when this signal is LOW, the processor writes into the VL6845.
$\overline{CS}$	25	$\overline{\text{Chip Select}}$	Input that, when HIGH, deselects VL6845; when this signal is LOW, the VL6845 is selected. This signal is typically connected to the system address bus either directly or through an address decoder.
RS	24	Register Select	Input that, when LOW, selects the Address Register of the VL6845 for a write operation. When this signal is HIGH, an internal register of the VL6845 specified by the contents of the address register is selected.
D0-D7	26-33	Data Bus	Eight bidirectional data lines that are used for transferring data between the microprocessor and the VL6845. These lines are normally high-impedance, except during read and write cycles when the chip is selected.
Video Memory Character Generator Interface			
CC0/MA0-CC5/MA13	4-17	Video Memory Address	Active-HIGH output signals that are used to address the video display memory in binary addressing mode. These memory addresses are generated in a binary sequential fashion. In row/column addressing mode, MA0-MA7 function as column addresses, and MA8-MA13 function as row addresses.
RA0-RA4/STB	34-38	Raster Address	Active-HIGH output signals that are used as address lines to the external character generator ROM. In the transparent addressing mode, RA4 functions as an active-HIGH output strobe.
HSYNC	39	Horizontal Sync	Active-HIGH, TTL-compatible output signal that is used to determine the horizontal position of the displayed text. HSYNC may drive a CRT monitor directly or may be used for composite video generation. Position and width of HSYNC width are fully programmable.
VSYNC	40	Vertical Sync	Active-HIGH, TTL-compatible output signal that is used to determine the vertical position of the displayed text. VSYNC may be used to drive a CRT monitor directly or may be used for composite video generation. VSYNC position is fully programmable.
DISPLAY	18	Display Enable	TTL-compatible output that, when HIGH, indicates that the VL6845 is generating active display information. The number of horizontal displayed characters and the number of vertical displayed rows are both fully programmable and together are used to generate the Display Enable signal.
CURSOR	19	Cursor	TTL-compatible output that when HIGH, indicates a valid cursor address to the external video processing logic.
LPSTB	3	Light Pen Strobe	HIGH-impedance, edge-sensitive input signal that latches the current refresh address into the light pen register. Latching occurs on the LOW-to-HIGH transition edge.
CCLK	21	Character Clock	Input signals derived from the external dot clock, that is used as the time base for all internal count and control functions.
$\overline{RES}$	2	$\overline{\text{Reset}}$	Input signal that when LOW, resets all internal counters. All scan and video outputs are LOW and all control registers are unaffected. RES can be used to synchronize display frame timing with the line frequency.
VCC	20	Supply Voltage	5 V supply
GND	1	Ground	Supply and signal ground

VL6845 FAMILY FUNCTIONAL DESCRIPTION

The VL6845 CRT Controller (CRTC) consists of programmable horizontal and vertical timing generators, programmable linear address registers, programmable cursor logic, a light pen capture register and control circuitry for interface to a processor bus.

All CRTC timing is derived from the character clock (CCLK), which is usually the output of an external dot rate counter. Coincidence circuits internal to the chip continuously compare counter contents to the programmed register file (R0-R17) for generation of Horizontal Sync, Vertical Sync, Display Enable, Cursor and other signals required to interface to a CRT display.

The linear address generator is also driven by the CCLK and locates the positions of characters in memory with respect to their positions on the screen. Fourteen address lines, MA0-MA13 are available for addressing up to 16K characters of memory. The CRTC addresses the memory in the binary sequential fashion. Using the start address register, hardware scrolling through the 16K character memory is possible. The linear address generator continues to increment during the blanking period, so memory refresh can be performed during the blanking periods. The linear address generator repeats the same sequence of addresses for each scan line of a character row. Although the linear address generator continues to increment during the horizontal and blanking periods, the correct address for the first displayed character or row is always maintained.

The Cursor logic determines the cursor location, size and blink rate on the screen.

The Light Pen Strobe latches the current contents of the address counter into the light pen register on LOW-to-HIGH transition.

INTERLACE MODE SELECTION

In the normal sync mode (non-interlace), only one field is available, as shown in Figure 1a. Each scan line is refreshed at the VSYNC frequency (50 or 60 Hz).

Two interlace modes are available as shown in Figure 1b and Figure 1c. The frame time is divided between even and odd alternating fields. The horizontal and vertical timing relationship (VSYNC delayed by one-half scan line time) results in the displacement of scan lines in the odd field with respect to the even field.

In the interlace sync mode, the same information is painted in both fields, as shown in Figure 1b. This is a useful mode for filling in a character to enhance readability.

In the interlace sync and video mode, as shown in Figure 1c, alternating lines of the character are displayed in the even field and the odd field. This effectively doubles the given band width of the CRT monitor.

Care must be taken when using either interlace mode to avoid an apparent flicker effect. This flicker effect is due to the doubling of the refresh time for all scan lines since each field is displayed alternately and may be minimized with proper monitor design i.e., longer persistence phosphors.

VL6845R/VL68C45R REGISTER FILE DESCRIPTIONS

The 19 registers of the CRTC may be accessed through the data bus. Only two memory locations are required, as one location is used as a pointer to address one of the remaining 18 registers. These 18 registers control horizontal timing, vertical timing, interlace operation and row address operation. They also define the cursor, cursor address, start address and light pen register. The register addresses and sizes are shown in Table 1.

ADDRESS REGISTER (AR)

The Address Register is a 5-bit write-only register used as an "indirect" or "pointer" register. It contains the address of one of the other 18 registers. When both RS and $\overline{CS}$ are LOW, the Address Register is selected. When $\overline{CS}$ is LOW and RS is HIGH, the register pointed to by the address register is selected.

FIGURE 1a.
NORMAL SYNC

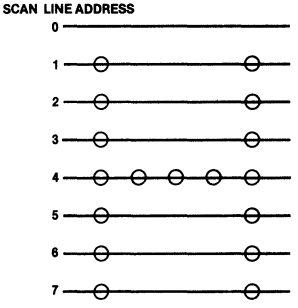


FIGURE 1b.
INTERLACE SYNC

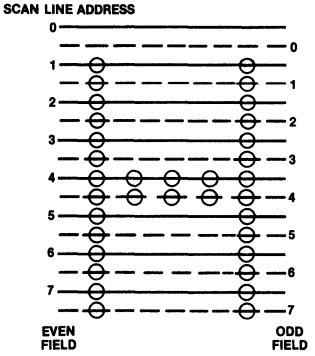
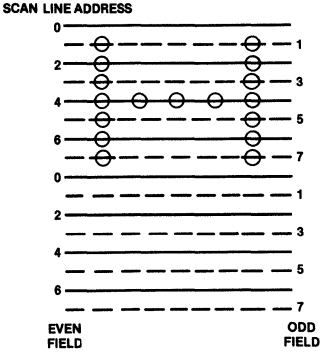


FIGURE 1c.
INTERLACE SYNC AND VIDEO



VL6845R/VL68C45R REGISTER FILE DESCRIPTIONS (Cont.)

HORIZONTAL TOTAL REGISTER (R0)

This 8-bit write-only register determines the horizontal sync (HSYNC) frequency by defining the HSYNC period in character times. It is the total of the displayed characters plus the non-displayed character times (retrace) minus one.

HORIZONTAL DISPLAYED REGISTER (R1)

This 8-bit write-only register determines the number of displayed characters per line. Any 8-bit number may be programmed as long as the contents of R0 are greater than the contents of R1.

HORIZONTAL SYNC POSITION REGISTER (R2)

This 8-bit write-only register controls the HSYNC position, which defines the horizontal sync delay (front porch) and the horizontal scan delay (back porch). When the programmed value of this register is increased, the display on the CRT screen is shifted to the left. When the programmed value is decreased, the display is shifted tot he right. Any 8-bit number may be programmed as long as the sum of the contents of R2 and R3 is less than the contents of R0. The contents of R2 must be greater than R1.

SYNC WIDTH REGISTER (R3)

This 8-bit write-only register determines the width of the HSYNC pulse. The vertical sync pulse width is fixed at 16 scan-line times. HSYNC pulse width may be programmed from 1 to 15 character clock periods, thus allowing compatibility with the HSYNC pulse width specifications of many different monitors. If zero is written into this register, no horizontal sync is provided.

HORIZONTAL TIMING SUMMARY

The difference between R0 and R1 is the horizontal blanking interval. This interval in the horizontal scan period allows the beam to return (retrace) to the left side of the screen. The retrace time is determined by the monitor horizontal scan components. Retrace time is less than the horizontal blanking interval.

A good rule of thumb is to make the horizontal blanking about 20% of the total horizontal scanning period for a CRT. In inexpensive TV receivers the beam over-scans the display screen so that aging of parts does not result in underscanning. Because of this, the retrace time should be about one-third the horizontal scanning period. The horizontal sync delay is typically programmed with a 1:2:2 ratio.

VERTICAL TOTAL REGISTER (R4) AND VERTICAL TOTAL ADJUST REGISTER (R5)

The vertical sync (VSYNC) frequency is determined by both R4 and R5. The

TABLE 1: VL6845R/VL68C45R INTERNAL REGISTER ASSIGNMENTS

$\overline{CS}$	RS	Address Register					Register #	Register File	Program Unit	Read	Write	Number of Bits							
		4	3	2	1	0						7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X	—	—	—	—								
0	0	X	X	X	X	X	AR	Address Register	—	No	Yes								
0	1	0	0	0	0	0	RO	Horizontal Total	Char.	No	Yes								
0	1	0	0	0	0	1	R1	Horizontal Displayed	Char.	No	Yes								
0	1	0	0	0	1	0	R2	H. Sync Position	Char.	No	Yes								
0	1	0	0	0	1	1	R3	Sync Width	—	No	Yes					H	H	H	H
0	1	0	0	1	0	0	R4	Vertical Total	Char. Row	No	Yes								
0	1	0	0	1	0	1	R5	V. Total Adjust	Scan Line	No	Yes								
0	1	0	0	1	1	0	R6	Vertical Displayed	Char. Row	No	Yes								
0	1	0	0	1	1	1	R7	V. Sync Position	Char. Row	No	Yes								
0	1	0	0	0	1	1	R3	Sync Width	—	No	Yes							I	I
0	1	0	1	0	0	1	R9	Max Scan Line Address	Scan Line	No	Yes								
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line	No	Yes		B	P			(Note 2)		
0	1	0	1	0	1	1	R11	Cursor End	Scan Line	No	Yes								
0	1	0	1	1	0	0	R12	Start Address (H)	—	No	Yes	0	0						
0	1	0	1	1	0	1	R13	Start Address (L)	—	No	Yes								
0	1	0	1	1	1	0	R14	Cursor (H)	—	Yes	Yes	0	0						
0	1	0	1	1	1	1	R15	Cursor (L)	—	Yes	Yes								
0	1	1	0	0	0	0	R16	Light Pen (H)	—	Yes	No	0	0						
0	1	1	0	0	0	1	R17	Light Pen (L)	—	Yes	No								

Notes:

1. The interlace bits are described in Table 2.
2. Bit 5 of the cursor start raster register is used for blink period, control, and bit 6 is used to select blink or no-blink.
3. Registers R4, R6 and R7 in the VL68C45R are eight bits wide, instead of seven, for compatibility with the Motorola 6845R1.

VL6845R/VL68C45R REGISTER FILE DESCRIPTIONS (Cont.)

calculated number of character row times is usually an integer plus a fraction to get exactly a 50 Hz or 60 Hz vertical refresh rate. The integer number of character row times minus one is programmed into the 7-bit write-only vertical total register (R4). The fraction of character line times is programmed into the 5-bit write-only vertical total adjust register (R5) as the number of scan lines required.

VERTICAL DISPLAYED REGISTER (R6)

This 7-bit write-only register specifies the number of character rows displayed on the CRT screen, and is programmed in character row times. Any number smaller than contents R$ may be programmed into R6.

VERTICAL SYNC POSITION REGISTER (R7)

This 7-bit write-only register controls the position of vertical sync with respect to the reference. It is programmed in character row times. When programmed value of this register is increased, the display position of the CRT screen is shifted up. When the programmed value is decreased, the display position is shifted down. Any number equal to or less than the contents of R4 and greater than or equal to the R6 may be used.

INTERLACE MODE AND SKEW REGISTER (R8)

The VL6845R only allows control of the interlace modes as programmed by the low-order two bits of this write-only register. Table 2 shows the interlace modes available to the user. These modes are selected using the two low order bits of this 6-bit write-only register.

TABLE 2: INTERLACE MODE REGISTER

Bit 1	Bit 2	Mode
0	0	Normal Sync Mode
1	0	(Non-interlace)
0	1	Interlace Sync Mode
1	1	Interlace Sync and Video Mode

INTERLACE MODE AND SKEW REGISTER (R8) (Cont.)

There are restrictions on the programming of the VL6845R/VL68C45R registers for interlace operation:

1. The Horizontal Total Register (R0) value must be odd (i.e., and even number of character times).
2. For interlace sync and video mode only, the Maximum Scanline Address Register (R9) value must be odd (i.e., an even number of scan lines).
3. For interlace sync and video mode only, the number (Nvd) programmed into the Vertical Display Register (R6) must be one-half the actual number required. The even-numbered scan lines are displayed in the even field and the odd-numbered scan lines are displayed in the odd field.
4. For interlace sync and video mode only, the Cursor Start Register (R10) and Cursor End Register (R11) must both be even or odd, depending on which field the cursor is to be displayed in. A full block cursor will be displayed in both in both the even and the odd field when the Cursor End Register (R11) is programmed to a value greater than the value in the Maximum Scan Line Address Register (R9).

MAXIMUM SCAN LINE ADDRESS REGISTER (R9)

This 5-bit write-only register determines the number of scan lines per character row, including the spacing, thus controlling operation of the row address counter. The programmed value is a maximum address and is one less than the number of scan lines.

CURSOR CONTROL REGISTERS

CURSOR START REGISTER (R10) AND CURSOR END REGISTER (R11)

These registers allow a cursor of up to 32 lines in height to be placed on any scan line of the character block. Register R10 is a 7-bit write-only register used to define the start scan line and the cursor blink rate. Bits 5 and 6 of the Cursor Start Address Register control the cursor operation as shown in table 3. Non-display, display, and two blink modes (16 times or 32 times the field period) are available. Register R11 is a 5-bit write-only register that defines the last scan cursor.

TABLE 3: CURSOR START REGISTER

Bit 6	Bit 5	Cursor Display Mode
0	0	Non-blink
0	1	Cursor Non-display
1	0	Blink, 1/16 field rate
1	1	Blink, 1/32 field rate

When an external blink feature on characters is required, it may be necessary to perform cursor blink externally so that both blink rates are synchronized. Note that an invert/non-invert cursor is easily implemented by programming the CRT for a blinking cursor and externally inverting the video signal with an exclusive-OR gate.

CURSOR REGISTER (R14-H, R15-L)

This 14-bit read/write register pair is programmed to position the cursor anywhere in the refresh RAM area, thus allowing hardware paging and scrolling through memory without loss of the original cursor position. It consists of an 8-bit low-order (MA0-MA7) register and a 6-bit high-order (MA8-MA13) register.

START ADDRESS AND LIGHT PEN REGISTERS

START ADDRESS REGISTER (R12-H, R13-L)

This 14-bit write-only register pair controls the first address output by the CRTC after vertical blanking. It consists of an 8-bit low-order (MA0-MA7) register and a 6-bit high-order (MA8-MA13) register. The start address register determines which portion of the refresh RAM is displayed on the CRT screen. Hardware scrolling by character or page may be accomplished by modifying the contents of this register.

LIGHT PEN REGISTER (R16-H, R17-L)

This 14-bit read-only register pair captures the refresh address output by the CRTC on the positive edge of a pulse input to the LPSTB pin. It consists of an 8-bit low-order (MA0-MA7) register and a 6-bit high-order (MA8-MA13) register. Since the light pen pulse is asynchronous with respect to refresh address timing, an internal synchronizer is designed into the CRTC. Due to delays in this circuit, the value of R16 and R17 will need to be corrected in software. (See the bus timing diagram in the Timing Characteristics section.)

VL68C45S
REGISTER FILE DESCRIPTIONS

TABLE 4: VL68C45S INTERNAL REGISTER ASSIGNMENTS, Note 1

$\overline{CS}$	RS	Address Register 4	3	2	1	0	Register #	Register Name	Program Unit	READ	WRITE	Data Bit 7	6	5	4	3	2	1	0
1	x	x	x	x	x	x			–	–	–								
0	0	x	x	x	x	x	AR	Address Register	–	×	○								
0	1	0	0	0	0	0	R0	Horizontal Total*	Character	×	○								
0	1	0	0	0	0	1	R1	Horizontal Displayed	Character	×	○								
0	1	0	0	0	1	0	R2	Horizontal Sync* Position	Character	×	○								
0	1	0	0	0	1	1	R3	Sync Width	Vertical-Raster, Horizontal-Character	×	○	wv3	wv2	wv1	wv0	wh3	wh2	wh1	wh0
0	1	0	0	1	0	0	R4	Vertical Total*	Line	×	○								
0	1	0	0	1	0	1	R5	Vertical Total Adjust	Raster	×	○								
0	1	0	0	1	1	0	R6	Vertical Displayed	Line	×	○								
0	1	0	0	1	1	1	R7	Vertical Sync* Position	Line	×	○								
0	1	0	1	0	0	0	R8	Interlace & Skew	–	×	○	C1	C0	D1	D0			V	S
0	1	0	1	0	0	1	R9	Maximum Raster Address	Raster	×	○								
0	1	0	1	0	1	0	R10	Cursor Start Raster	Raster	×	○		B	P					
0	1	0	1	0	1	1	R11	Cursor End Raster	Raster	×	○								
0	1	0	1	1	0	0	R12	Start Address (H)	–	○	○								
0	1	0	1	1	0	1	R13	Start Address (L)	–	○	○								
0	1	0	1	1	1	0	R14	Cursor (H)	–	○	○								
0	1	0	1	1	1	1	R15	Cursor (L)	–	○	○								
0	1	1	0	0	0	0	R16	Light Pen (H)	–	○	×								
0	1	1	0	0	0	1	R17	Light Pen (L)	–	○	×								

Note:
1. ○ = yes; × = no

VL68C45S REGISTER FILE DESCRIPTIONS (Cont.)

ADDRESS REGISTER (AR)

This is a 5-bit register that is used to select 18 internal control registers (R0-R17). Its contents are the address of one of 18 internal control registers. Programming the data from 18 to 31 produces no results. Access to R0-R17 requires writing the address of the corresponding control register into this register. When RS and CS are LOW, the address is selected.

HORIZONTAL TOTAL REGISTER (R0)

This 8-bit register is used to program the total number of horizontal characters per line, including the retrace period. The data value should be programmed according to the specification of the CRT. When M is the total number of characters, (M-1) must be programmed into this register. When programming for interlace mode, M must be even.

HORIZONTAL DISPLAYED REGISTER (R1)

This 8-bit register is used to program the number of horizontal displayed characters per line. Any 8-bit number that is smaller than that of horizontal total register contents can be programmed.

HORIZONTAL SYNC POSITION REGISTER (R2)

This 8-bit register is used to program horizontal sync position as multiples of the character clock period. Any 8-bit number that is lower than the horizontal total register contents can be programmed. When H is the character number of the horizontal sync position, (H-1) must be programmed into this register. When the programmed value of this register is increased, the display position on the CRT screen is shifted to the left. When the programmed value is decreased, the position is shifted to the right. Therefore, the optimum horizontal position can be determined by this value.

SYNC WIDTH REGISTER (R3)

This 8-bit register is used to program the horizontal sync (HS) pulse width and the vertical sync (VS) pulse width. The horizontal sync pulse width is programmed in the lower four-bits as multiples of the character clock period (see Table 5); a zero cannot be programmed. The vertical sync pulse width is programmed in the higher four bits as multiples of the raster period (see Table 6). When zeroes are programmed in the higher four bits, a 16-raster period is specified.

VERTICAL TOTAL REGISTER (R4)

This 7-bit register is used to program the total number of lines per frame, including vertical retrace period. The data and its value should be programmed according to the specification of the CRTC. When N is the total number of lines, (N-1) must be programmed into this register.

VERTICAL TOTAL ADJUST REGISTER (R5)

This 5-bit register is used to program the optimum number to adjust the total number of rasters per field. This register enables more precise control of the deflection frequency.

VERTICAL DISPLAYED REGISTER (R6)

This 7-bit register is used to program the number of displayed character rows on the CRT screen. Any 7-bit number that is smaller than that of vertical total register contents can be programmed.

VERTICAL SYNC POSITION REGISTER (R7)

This 7-bit register is used to program the vertical sync position on the screen as multiples of the horizontal character line period. Any number that is equal to or less than the vertical total register content can be programmed. When V is the character number of vertical sync position, (V-1) must be programmed to this register. When programmed value of this register is increased, the display position is shifted up. When the programmed value is decreased, the position is shifted down. Therefore, the optimum vertical position may be determined by this value.

INTERLACE AND SKEW REGISTER (R8)

This register is used to program raster scan mode and skew (delay) of the Cursor signal and Display Enable signals.

INTERLACE MODE PROGRAM BITS (V,S)

Raster scan mode is programmed (see Table 7) by the V and S bits of R8. In the non-interlace mode, duplicate scanning is done of the rasters of even number field and odd number field. In the interlace sync mode, the rasters of the odd number field are scanned in the middle of the even number field. The same character pattern is then displayed in two fields. In the interlace sync and video mode, the raster scan method is the same as in the interlace sync mode, but it is controlled to display different character patterns in two fields.

Note:

1. The registers marked *:
   (written value) = (specified value) − 1
2. Written value of R9:
   a) Non-interlace mode and Interlace Sync Mode (written value Nr) = (specified value) − 1
   b) Interlace sync and video mode: (Written value Nr) = (specified value) − 2
3. CO and C1 specify skew of CURSOR output signal.
   DO and D1 specify skew of Display Enable output signal. When S is one, V specifies video mode. S specifies the Interlace sync mode.
4. B specifies cursor blink.
   P specifies the cursor blink period.
5. wv0~wv3 specify the pulse width of the vertical sync signal. wh0~wh3 specify the pulse width of the horizontal sync signal.
6. RO is normally programmed to be an odd number in interlace mode.
7. 0 = Yes, X = No

VL68C45S
REGISTER FILE DESCRIPTIONS (Cont.)

TABLE 5: PULSE WIDTH OF HORIZONTAL SYNC SIGNAL

VSW/HSW Register (R3)				HSW Pulse Width (multiples of char clock period)
Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	Not Allowed
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

TABLE 6: PULSE WIDTH OF VERTICAL SYNC SIGNAL

VSW/HSW Register (R3)				VSW Pulse Width (multiples of raster period)
Bit 7	Bit 6	Bit 5	Bit 4	
0	0	0	0	16
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

TABLE 7: INTERLACE MODE BITS (BITS 1 AND 0 of R8)

V Bit 1	S Bit 2	Mode
0	0	Normal Sync Mode (Non-interlace)
1	0	
0	1	Interlace Sync Mode
1	1	Interlace Sync and Video Mode

SKEW PROGRAM BITS (C1,C0,D1,D0)

These bits are used to program the skew (delay) of the Cursor and Display Enable signals.

Skew of these two kinds of signals is programmed separately. The skew function is used to provide an on-chip delay for the output timing of the of the Cursor and Display Enable signals to provide the time required to access refresh memory, character generator or pattern generator, and to ensure that they are in phase with the serial video signal.

TABLE 8: DISPLAY ENABLE SKEW BIT (BITS 5 AND 4 OF R8)

D1 Bit 5	D0 Bit 4	Display Enable Signal
0	0	Non-Skew
0	1	One-character Skew
1	0	Two-character Skew
1	1	Non-output

TABLE 9: CURSOR SKEW BITS (BITS 7 & 6 OF R8)

C1 Bit 7	C0 Bit 6	Display Skew
0	0	Non-Skew
0	1	One-character Skew
1	0	Two-character Skew
1	1	Non-output

VL68C45S REGISTER FILE DESCRIPTIONS (Cont.)

MAXIMUM RASTER ADDRESS REGISTER (R9)

This 5-bit register is used to program the Maximum Raster Address. This register defines total number of rasters per character, including space.

This register is programmed as follows:

1. Non-Interlace Mode,
   Interlace Sync Mode:
   When the total number of rasters is RN, (RN-1) must be programmed.
2. Interlace Sync and Video Mode:
   When total number of rasters is RN, (RN-2) must be programmed.

The total number of rasters in non-interlace mode, interlace sync mode and interlace sync and video mode is defined as follows in Table 10.

TABLE 10: RASTER COUNT IN INTERLACE AND NON-INTERLACE MODES

0 ——— Total number of rasters 5

1 ——— Programmed value Nr = 4

2 ——— (The same as displayed total number of rasters)

3 ———

4 ———

Raster Address

INTERLACE SYNC MODE

0 ——— Total number of rasters 5

– – – – – – – – – – – 0 programmed value Nr = 4

1 ———

– – – – – – – – – – – 1

2 ———

– – – – – – – – – – – 2

3 ———

– – – – – – – – – – – 3

4 ———

– – – – – – – – – – – 4

In the interlace sync mode, total number of rasters in both the even and odd fields is ten. On programming, the half of it is defined as total number of rasters.

Raster Address

INTERLACE SYNC AND VIDEO MODE

0 ——— Total Number of Rasters 5

– – – – – – – – – – – 1 Programmed Value Nr = 3

2 ———

– – – – – – – – – – – 3

4 ———

(Total number of rasters displayed in the even field and the odd field)

Raster Address

Note:

1. In the interlace mode, pulse width is changed + ½ raster time when vertical sync signal extends over two fields.

CURSOR START RASTER REGISTER (R10)

This 7-bit register is used to program the cursor start raster address and the cursor display mode. The lower five bits program the raster address and the higher two bits program the display mode (see table 11).

TABLE 11: CURSOR DISPLAY MODE (BITS 6 AND 5 OF R10)

B Bit 6	P Bit 5	Cursor Display Mode
0	0	Non-Blink
0	1	Cursor Non-Display
1	0	Blink, 1/16 Field Rate
1	1	Blink, 1/32 Field Rate

Note:

The blink sequence is follows:

Light	Dark

(16 x or 32 x the field period)

CURSOR END RASTER REGISTER (R11)

This register is used to program the cursor end raster address.

START ADDRESS REGISTER (R12, R13)

This register pair is used to program the first address of refresh memory read out. Paging and scrolling are easily performed using this register. This register can be read but the higher 2-bits of R12 are always zero.

CURSOR REGISTER (R14,R15)

These two read/write registers store the cursor location. The higher 2 bits of R14 are zero.

LIGHT PEN REGISTER (R16,R17)

These read-only registers are used to capture the detection address of the light pen. The higher 2 bits of R16 are always zero. The value of R16 and R17 needs to be corrected by software because there is a time delay from the address output by the CRTC to the signal input to its LPSTB pin that the light pen detects.

CONSIDERATIONS IN UPDATING REGISTERS

The value programmed into the internal registers directly controls the CRT. Consequently, the display may flicker on the screen when the contents of the registers are changed from the bus side asynchronously with display operation.

RESTRICTIONS ON PROGRAMMING INTERNAL REGISTERS

1. $0 \leq Nhd \leq Nht + 1 \leq 256$
2. $0 \leq Nvd \leq Nvt + 1 \leq 128$
3. $0 \leq Nhsp \leq Nht$
4. $0 \leq Nvsp \leq Nvt$, Note 1
5. $0 \leq NCSTART \leq NCEND \leq Nr$ (non-interlace, interlace sync mode)
   $0, NCSTART \leq NCEND \leq Nr + 1$ (interlace sync and video mode)
6. $2 \leq Nr \leq 30$
7. $3 \leq Nht$ (except non-interlace mode)
   $5 \leq Nht$(non-interlace mode only)

UPDATING THE CURSOR REGISTER

Writing into this register at frequent intervals for moving the cursor should be performed during horizontal and vertical retrace periods.

UPDATING THE START ADDRESS REGISTER

Writing into the start address register at frequent intervals for scrolling and paging should be performed during horizontal and vertical display periods.

It is desirable to avoid programming any registers besides the cursor and Start Address Register during display operations.

VL6845E
REGISTER FILE DESCRIPTIONS

TABLE 12: VL6845E INTERNAL REGISTER ASSIGNMENT

		Address Register					Register					Register Bit							
CS	RS	4	3	2	1	0	Number	Register Name	Stored Info.	RD	WR	7	6	5	4	3	2	1	0
1		–	–	–	–	–	–												
0	0	–	–	–	–	–	–	Address Register	Register Number		√				A4	A3	A2	A1	A0
0	0	–	–	–	–	–	–	Status Register		√		U	L	V					
0	1	0	0	0	0	0	R0	Horizontal Total	# Character-1		√								
0	1	0	0	0	0	1	R1	Horizontal Displayed	# Character		√								
0	1	0	0	0	1	0	R2	Horizontal Sync Position	# Character		√								
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	# Scan Lines and # Character TImes		√	V3	V2	V1	V0	H3	H2	H1	H0
0	1	0	0	1	0	0	R4	Vertical Total	# Character Row -1		√								
0	1	0	0	1	0	1	R5	Vertical Total Adjust	# Scan Lines		√								
0	1	0	0	1	1	0	R6	Vertical Displayed	# Character Rows		√								
0	1	0	0	1	1	1	R7	Vertical Sync Position	# Character Rows		√								
0	1	0	1	0	0	0	R8	Mode Control			√	U1	U0	C	D	T	RC	I1	I0
0	1	0	1	0	0	1	R9	Scan Line	# Scan Lines -1		√								
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No.		√		B1	B0					
0	1	0	1	0	1	1	R11	Cursor End	Scan Line Number		√								
0	1	0	1	1	0	0	R12	Display Start Addr (H)	Row		√								
0	1	0	1	1	0	1	R13	Display Start Addr (L)	Column		√								
0	1	0	1	1	1	0	R14	Cursor Position (H)	Row	√	√								
0	1	0	1	1	1	1	R15	Cursor Position (L)	Column	√	√								
0	1	1	0	0	0	0	R16	Light Pen Register (H)		√									
0	1	1	0	0	0	1	R17	Light Pen Register (L)		√									
0	1	1	0	0	1	0	R18	Update Location (H)			√								
0	1	1	0	0	1	1	R19	Update Location (L)			√								
0	1	1	1	1	1	1	R31	Dummy Location											

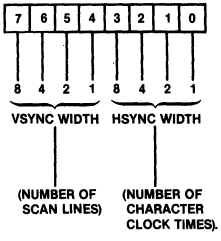
Note:

1. ▒ designates unused bit. Reading this bit is always "0", except for R31, which does not drive the data bus at all, and for $\overline{CS}$ = "1" which operates likewise.

VL6845E REGISTER FILE DESCRIPTIONS (Cont.)

ADDRESS REGISTER
This 5-bit register is used as a "pointer" to direct VL6845E data transfers to and from the system MPU. Its contents are the number of the desired register (0-31). When RS is LOW, the address register may be loaded; when RS is HIGH, the register selected is the one whose identity is stored in this register.

STATUS REGISTER
This 3-bit register is used to monitor the status of the CRTC. It is only accessed in reading, while the Address Register is only accessed in writing. Both these registers are accessed with RS and $\overline{CS}$ LOW.



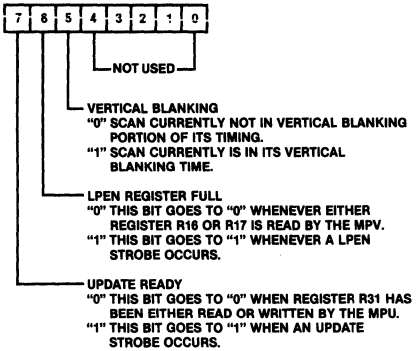
*IF BITS 4-7 ARE ALL "0" THEN VSYNC WILL BE 16 SCAN LINES WIDE.

HORIZONTAL TOTAL REGISTER (R0)
This 8-bit register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The horizontal sync (HSYNC) frequency is thus determined by this register.

HORIZONTAL DISPLAYED REGISTER (R1)
This 8-bit register contains the number of displayed characters per horizontal line.

HORIZONTAL SYNC POSITON REGISTER (R2)
This 8-bit register contains the HSYNC position on the horizontal line, in terms of the character location number on the line. The position of HSYNC determines the left-to-right location of the displayed text on the video screen. In this way, the side margins are adjusted.

HORIZONTAL AND VERTICAL SYNC WIDTH REGISTER (R3)
This 8-bit register contains the widths of both HSYNC and VSYNC, as follows:



Control of these parameters allow the VL6845E to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one shot timing.

VERTICAL TOTAL REGISTER (R4)
This 7-bit register contains the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency RES may be used to provide absolute syncronism.

VERTICAL TOTAL ADJUST REGISTER (R5)
This 5-bit write-only register contains the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

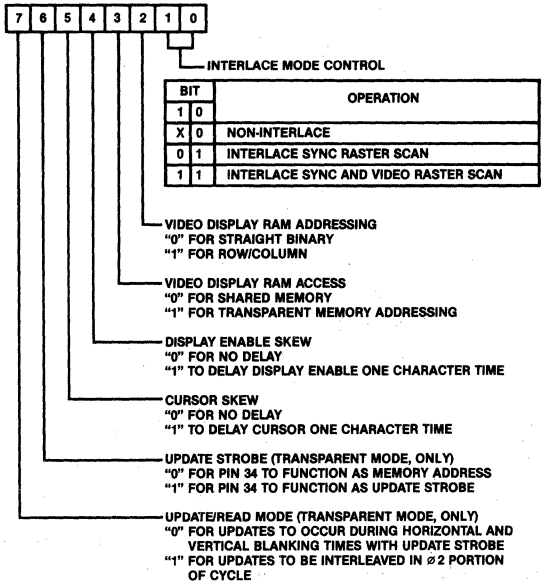
VERTICAL DISPLAYED REGISTER (R6)
This 7-bit register contains the number of displayed character rows in each frame. In this way, the vertical size of the displayed text is determined.

VERTICAL SYNC POSITION REGISTER (R7)
This 7-bit register is used to select the character row time at which the VSYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

VL6845E REGISTER FILE DESCRIPTIONS (Cont.)

MODE CONTROL REGISTER (R8)

This register is used to select the operating modes of the VL6845E and is outlined as follows:



SCAN LINE REGISTER (R9)

This 5-bit register contains the number of scan lines per character row, including space minus one.

CURSOR START REGISTER (R10) AND CURSOR END REGISTER (R11)

These 5-bit registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor mode, as follows:

BIT		
66	55	Cursor Display Mode
60	50	Non-Blink
60	51	Non-Display
61	50	Blink 1/16 Field Rate
61	51	Blink 1/32 Field Rate

Note that the ability to program both the start and end scan line for the cursor enables either block cursor or underline to be accomodated. Registers R14 and R15 are used to control the character position of the cursor over the entire 16K address field.

DISPLAY START ADDRESS AND LOW REGISTERS (R12,R13)

These registers together comprise a 14-bit register whose contents are the memory address of the first character of the displayed scan (the character on the top left of the video display). Subsequent memory addresses are generated by the VL68465E as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well as via R12 and R13.

CURSOR POSITION HIGH AND LOW REGISTERS (R14,R15)

These registers together comprise a 14-bit register whose contents are the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, the Cursor output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the Cursor output by a full CCLK time to accomodate slow-access memories.

LPSTB HIGH AND LOW REGISTERS (R16,R17)

These registers together comprise a 14-bit register whose contents are the light pen strobe position, in terms of the video display address at which the strobe occured. When the LPSTB input changes from LOW to HIGH, then, on the next negative-going edge of CCLK, the contents of the internal scan counter are stored in registers R16 and R17.

UPDATE ADDRESS HIGH AND LOW REGISTERS (R18,R19)

These registers together comprise a 14-bit register whose contents is the memory address at which the next read or update will occur (for transparent addressing mode, only). Whenever a read/update occurs, the update location automatically updates, to allow for fast updates or readouts of consecutive character locations. This is described elsewhere in this document.

DUMMY LOCATION (R31)

This register does not store any data, but is required to detect when transparent addressing updates occur. This is necessary to increment the Update Address Register and to set the Update Ready bit in the Status Register.

VL6845E DESCRIPTION OF OPERATION

REGISTER FORMATS

Register pairs R12/R13, R14/R15, R16/R17, and R18/R19 are formatted in one of two ways:

1) Straight Binary if register R8, bit2 is a zero.
2) Row/Column if register R8, bit 2 is a one. In this case, the low byte is the Character Column, and the high byte is the Character Row.

Figure 2 illustrates the address sequence for the video display control for each mode. Note from Figure 2 that the straight binary mode has the advantage that all display memory addresses

VL6845E
DESCRIPTION OF OPERATION
(Cont.)

are stored in a continuous memory block, starting with address 0 and ending at 1919. The disadvantage with this method is that, if it is desired to change a displayed character location, the row and column identity of the location must be converted to its binary address before the memory may be written. The row/column mode, on the other hand, does not require this conversion. However, memory is not used as efficiently, since the memory addresses are not continuous (gaps exist). This requires that the system be equipped with more memory than is actually used, and this extra memory is wasted. Alternatively, address compression logic may be employed to translate the row/column format into a continuous address block.

In this way, the system designer may select whichever mode is best for the given application. The trade-offs between the modes involve the comparative costs of hardware and software. Straight-binary mode minimizes hardware requirements, and row/column addressing requires minimum software.

VIDEO DISPLAY RAM ADDRESS LINES (MA0-MA13)

These signals are active-HIGH outputs that are used to address the video display RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters per line and lines per frame.

There are two selectable address modes for MA0-MA13:

1. Binary
   Characters are stored in successive memory locations. Thus, the software must be developed so that row and column coordinates are translated in sequentially numbered addresses for video display memory operations.
2. Row/Column
   In this mode, MA0-MA7 function as column addresses CC0-CC7, and MA8-MA13 as row addresses CR0-CR5. In this case, the software may handle addresses in terms of row and column locations, but additional address compression circuits are needed to convert CC0-CC7 and CR0-CR5 into a memory efficient binary scheme.

RASTER ADDRESS LINES (RA0-RA4)

These signals are active-HIGH outputs that are used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

The HIGH-order line, RA4, is unique in that it can also function as a strobe output pin when the VL6845E is programmed to operate in the "transparent address mode". In this case, the strobe is an active-HIGH output that is true at the time the video display RAM update address is gated onto the address lines, MA0-MA13. In this way, updates and readouts of the video display RAM can be made under control of the CRTC with only a small amount of external circuitry.

FIGURE 2. DISPLAY ADDRESS SEQUENCES (WITH START ADDRESS = 0) FOR 80 x 24 EXAMPLE

TOTAL = 90

DISPLAY = 80

TOTAL = 34

DISPLAY = 24

0	1	2	---	---	77	78	79	80	81	---	89
80	81	82	---	---	157	158	159	160	161	---	169
160	161	162	---	---	237	238	239	240	241	---	249
⋮							⋮				⋮
⋮							⋮				⋮
1760	1761	1762	---	---	1837	1838	1839	1840	1841	---	1849
1840	1841	1842	---	---	1917	1918	1919	1920	1921	---	1929
1920	1921	1922	---	---	1997	1998	1999	2000	2001	---	2009
2000	2001	2002	---	---	2077	2078	2079	2080	2081	---	2089
⋮							⋮				⋮
2640	2641	2642	---	---	2717	2718	2719	2720	2721	---	2729

STRAIGHT BINARY ADDRESSING SEQUENCE

TOTAL = 90

DISPLAY = 80

COLUMN ADDRESS (MA0-MA7)

TOTAL = 34

DISPLAY = 24

ROW ADDRESS (MA8-MA13)

0	1	2	---	---	77	78	79	80	81	---	89
0	1	2	---	---	77	78	79	80	81	---	89
256	257	258	---	---	333	334	335	336	337	---	345
512	513	514	---	---	589	590	591	592	593	---	601
⋮							⋮				⋮
⋮							⋮				⋮
5632	5633	5634	---	---	5709	5710	5711	5712	5713	---	5721
5888	5889	5890	---	---	5965	5966	5967	5968	5969	---	5977
6144	6145	6146	---	---	6221	6222	6223	6224	6225	---	6233
6400	6401	6402	---	---	6477	6478	6479	6480	6481	---	6489
⋮							⋮				⋮
8448	8449	8450	---	---	8525	8526	8527	8528	8529	---	8537

ROW/COLUMN ADDRESSING SEQUENCE

VL6845E
DESCRIPTION OF OPERATION
(Cont.)

MEMORY CONTENTION SCHEMES FOR SHARED MEMORY ADDRESSING

In a typical system, it is clear that both the VL6845E CRTC and the system MPU must be capable of addressing the video display memory. The VL6845E CRTC repetitively fetches character information to generate the video signals in order to keep the screen display active. The MPU occasionally accesses the memory to change the displayed information or to read out current data characters. Three ways of resolving this dual-contention requirement are apparent:

1. **MPU PRIORITY**
   In this technique, the address lines to the video display memory are normally driven by the VL6845E unless the MPU needs access, in which case the MPU addresses immediately override those from the VL6845E and the MPU has immediate access.
2. **PHASE 1/PHASE 2 (01/02) MEMORY INTERLEAVING**
   This method permits both the VL6845 and the MPU access the video display memory by time-sharing via system 01 and 02 clocks. During the 01 portion of each cycle (the time when E is LOW), the CRTC address outputs are gated to the video display memory. In the 02 time, the MPU address lines are switched in. In this way, both the CRTC and the MPU have unimpeded access to the memory. (Figure 3a illustrates the timings)
3. **VERTICAL BLANKING**
   With this approach, the address Circuitry is identical to the case for MPU priority updates. The only difference is that the vertical retrace status bit (bit 5 of the status register) is used by the MPU so that access to the video display memory is only made during vertical blanking time (when bit 5 is a one). In this way, no visible screen perturbations result.

TRANSPARENT MEMORY ADDRESSING

In this mode of operation, the video display memory address lines are not switched by contention circuits, but are generated by the CRTC. In effect, the contention is handled by the CRTC. As a result, the schemes for accomplishing MPU memory acces are different:

1. **PHASE 1/PHASE 2 (Ø1/Ø2) INTERLEAVING**
   This mode is similar to the interleave mode used with shared memory. In this case, however, the Ø2 address is generated from the update address register (Registers R18 and R19) in the CRTC. Thus, the MPU must first load the address to be accessed into R18/R19 and then this address is always gated onto the MA lines during Ø2. (Figure 3b illustrates the timing)
2. **HORIZONTAL/VERTICAL BLANKING**
   In this mode, the update address register is loaded by the MPU, but is only gated onto the MA lines during horizontal or vertical blank times, so memory accesses do not interfere with the display appearance. To signal when the update address is on the MA lines, an update strobe (STB) is provided as an alternative function of pin 34. Data hold latches are necessary to temporarily retain the character to be stored until the retrace time occurs. In this way, the system MPU is not halted while waiting for the blanking time to arrive.

FIGURE 3a. PHASE 1/PHASE 2 SHARED INTERLEAVING

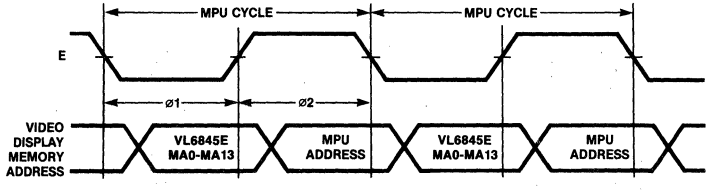
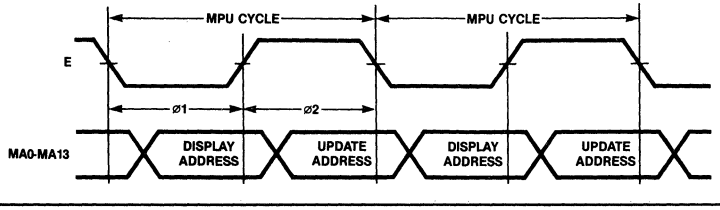


FIGURE 3b. PHASE 1/PHASE 2 TRANSPARENT INTERLEAVING



ABSOLUTE MAXIMUM RATINGS

Supply Voltage −0.3 V to +7.0 V

Input/Output Voltage, VIN −0.3 V to +7.0 V

Operating Temperature, Top 0°C to 70°C

Storage Temperature, TSTG −55°C to 150°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS TA = 0° to 70°C, VCC = 5.0 V ± 5%, unless otherwise noted

Symbol	Characteristic	Min	Typ	Max	Unit
VIH	Input HIGH Voltage	2.0		Vcc	V
VIL	Input LOW Voltage	−0.3		0.8	V
IIN	Input Leakage (o2, R/W, RES, CS, RS, LPSTB, CCLK)	—		2.5	µA
ITSI	Three-State Input Leakage (DBO-DB7) VIN = 0.4 to 2.4 V	—		±10.0	µA
VOH	Output HIGH Voltage ILOAD = −205 µA (DBO-DB7) ILOAD = −100 µA (all others)	2.4		—	V
VOL	Output LOW Voltage ILOAD = 1.6 mA	—		0.4	V
PD	Power Dissipation	—	325	650	mW
CI	Input Capacitance o2,R/W,RES,CS,RS,LPSTB,CLK, DBO-DB7	— —		10.0 12.5	pF pF
CO	Output Capacitance	—		10.0	pF

VL6845 CHARACTERISTICS

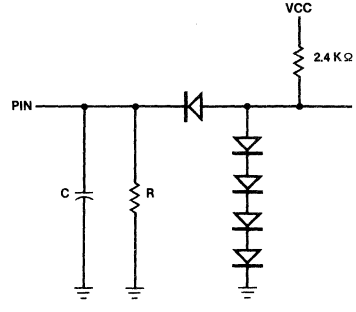
To ensure system compatibility, all CRTC timing is referenced by bus and character clock speed specification rather than device type. Thus, for a given MPU and character clock speed, the entire VL6845 family will adhere to the same timing regardless of version number. Table 13 presents a cross reference between specifications and device numbers.

The bus timing test load is shown in Figure 4. Signal timing for the CRTC is described in Table 14, and Table 15 describes CRTC video timing. Light pen timing is described in Table 16.

TABLE 13: VL6845 SPECIFICATION/ PART NUMBER REFERENCE

VL6845E-24	VTI-24
VL6845E-34	VTI-34
VL6845R-23	VTI-23
VL6845R-24	VTI-24
VL6845R-33	VTI-33
VL6845R-34	VTI-34
VL6845R-35	VTI-35
VL68C45R-23	VTI-23
VL68C45R-24	VTI-24
VL68C45R-33	VTI-33
VL68C45R-34	VTI-34
VL68C45R-35	VTI-35
VL68C45S-23	VTI-23
VL68C45S-24	VTI-24
VL68C45S-33	VTI-33
VL68C45S-34	VTI-34
VL68C45S-35	VTI-35

FIGURE 4. TEST LOAD



R = 11 KΩ FOR DB0—DB7
R = 24 KΩ FOR ALL OTHER OUTPUTS
C = 130 pF TOTAL FOR DO—D7
C = 30 pF ALL OTHER OUTPUTS

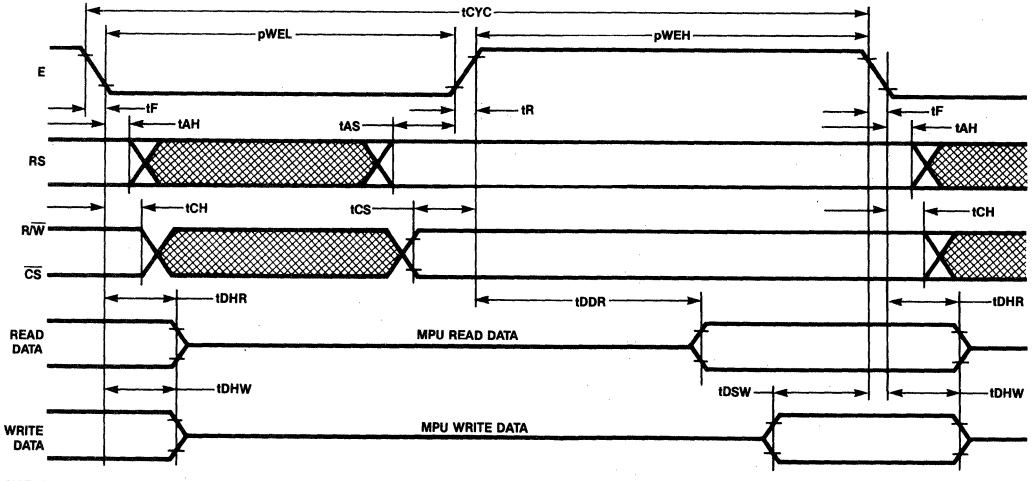
NOTES:
1. VOLTAGE LEVELS SHOWN ARE 0.4 V AND 2.4 V
2. MEASUREMENT POINTS SHOWN ARE 0.8 V AND 2.0 V

VL6845
CHARACTERISTICS (Cont.)
TABLE 14: CRTC BUS TIMING CHARACTERISTICS

		VTI-23		VTI-24		VTI-33		VTI-34 VTI-35		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
tcyc	Cycle Time	500		500		333		333		ns
pWEL	Pulse Width, E LOW	190		190		140		140		ns
pWEH	Pulse Width, E HIGH	200		200		150		150		ns
tR	Clock Rise Time		30		30		30		30	ns
tF	Clock Fall Time		30		30		30		30	ns
tAH	Address Hold Time (RS)	0		0		0		0		ns
tAS	RS Setup Time	40		40		30		30		ns
tCS	R/W, CS Setup	40		40		30		30		ns
tCH	R/W, CS Hold Time	0		0		0		0		ns
tDHR	Read Data Hold Time	20	60	20	60	20	60	20	60	ns
tDHW	Write Data Hold Time	10		10		10		10		ns
tDDR	Peripheral Output Delay Time	0	150	0	150	0	130	0	130	ns
tDSW	Peripheral Setup Time	60		60		60		60		ns

TIMING DIAGRAM

VL6845 BUS TIMING



NOTES:
1. VOLTAGE LEVELS SHOWN ARE V1≤ 0.4V, Vh≥ 2.4V
2. MEASUREMENT POINTS SHOWN ARE 0.8V AND 2.0V.

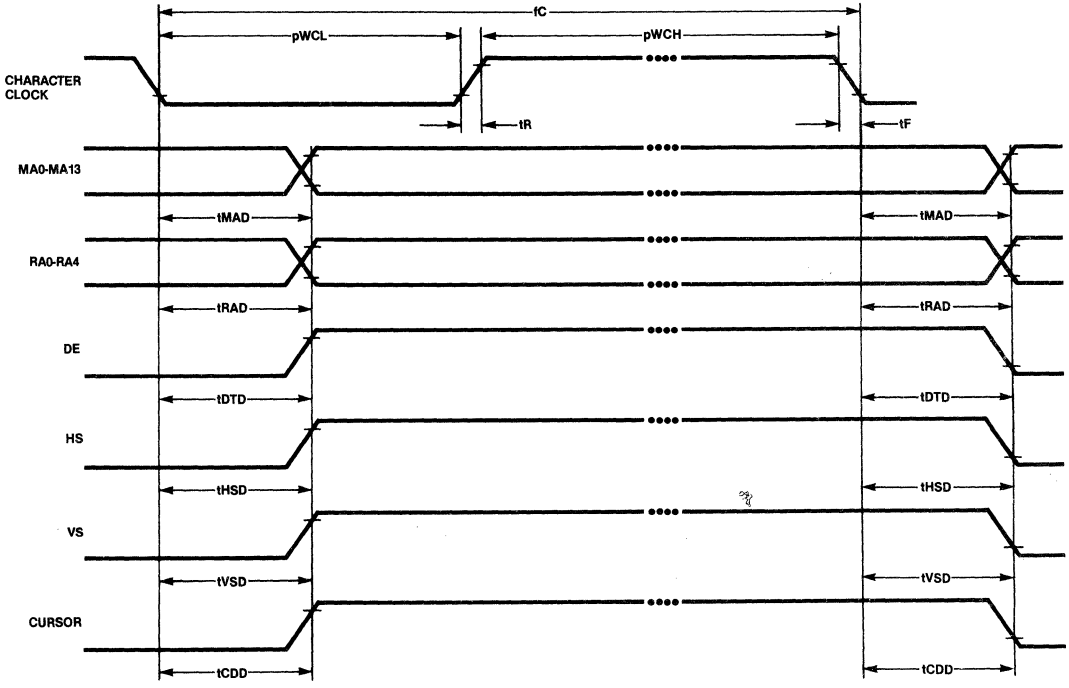
VL6845
CHARACTERISTICS (Cont.)

TABLE 15: CRTC VIDEO TIMING CHARACTERISTICS

Symbol	Parameter	VTI-23		VTI-24		VTI-33		VTI-34		VTI-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
pWCL	Clock Pulse Width, LOW	150		110		150		110		100		ns
pWCH	Clock Pulse Width, HIGH	150		120		150		120		100		ns
fC	Clock Frequency		3.0		4.0		3.0		4.0		5.0	MHz
tR	Clock Rise Time		20		20		20		20		20	ns
tF	Clock Fall Time		20		20		20		20		20	ns
tMAD	Memory Address Delay Time		160		140		160		140		140	ns
tRAD	Raster Address Delay Time		160		150		160		150		140	ns
tDTD	Display Timing Delay Time		250		250		250		250		200	ns
tHSD	Horizontal Sync Delay Time		250		200		250		200		200	ns
tVSD	Vertical Sync Delay Time		250		250		250		250		200	ns
tCDD	Cursor Display Delay Time		250		250		250		250		200	ns

TIMING DIAGRAM

VL6845 VIDEO TIMING



NOTES:
TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS UNLESS OTHERWISE SPECIFIED

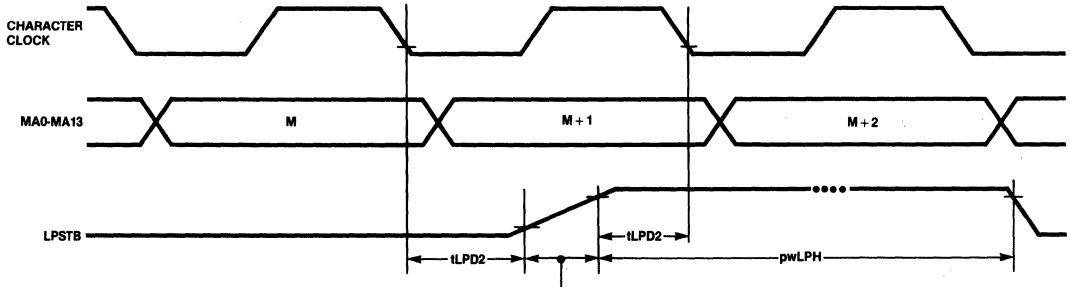
VL6845
AC CHARACTERISTICS

TABLE 16: CRTC LIGHT PEN TIMING CHARACTERISTICS

Symbol	Parameter	VTI-23		VTI-24		VTI-33		VTI-34 VTI-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
pwLPH	Light Pen Strobe Pulse Width	80		60		80		60		ns
tLPD1	Light Pen Display Time 1		120		70		120		70	ns
tLPD2	Light Pen Display Time 2		0		0		0		0	ns

TIMING DIAGRAM

VL6845 LIGHT PEN TIMING



NOTES:
1. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.
2. tLPD1 AND tLPD2 ARE THE PERIODS OF UNCERTAINTY FOR THE REFRESH MEMORY ADDRESS.

CROSS REFERENCE GUIDE

VTI Device	Replaces	Bus Frequency (MHz)	Character Clock (MHz)
VL6845R-23	MC68B45R	2.0	3.0
VL6845R-23	MC68A45	1.5	3.0
VL6845R-23	MC6845R	1.0	3.0
VL68C45R-23	MC68B45R1	2.0	3.0
VL68C45R-23	MC68A45R1	1.5	3.0
VL68C45R-23	MC6845R1	1.0	3.0
VL68C45R-23	HD68B45R	2.0	3.0
VL68C45R-23	HD68A45R	1.5	3.0
VL68C45R-23	HD6845R	1.5	3.0
VL68C45S-24	HD68B45S	2.0	3.7
VL68C45S-24	HD68A45S	1.5	3.7
VL68C45S-24	HD6845S	1.0	3.7
VL6845E-24	SY6845EA	2.0	3.7
VL6845E-24	SY6845E	1.0	3.7
VL6845R-23	SY6845RA	2.0	2.5
VL6845R-23	SY6845R	1.0	2.5

VL6845 REGISTER COMPARISON

Non-interlace

Register	VL68C45R MC6845R1	VL6845R MC6845 HD6845R	VL68C45S HD6845S	SY6545-1	VL6845E
R0 Horizontal Tot	Tot-1	Tot-1	Tot-1	Tot-1	Tot-1
R1 Horizontal Disp	Actual	Actual	Actual	Actual	Actual
R2 Horizontal Sync	Actual	Actual	Actual	Actual	Actual
R3 Horizontal and Vert Sync Width	Horizontal	Horizontal	Horizontal and Vertical	Horizontal and Vertical	Horizontal and Vertical
R4 Vertical Tot	Tot-1 (0-127)	Tot-1	Tot-1	Tot-1	Tot-1
R5 Vertical Tot Adj	Any Value	Any Value	Any Value	Any Value Except R5 = (R9H) • X	Any Value
R6 Vertical Disp	Any Value <R4 (0-255)	Any Value <R4	Any Value <R4	Any Value <R4	Any Value <R4
R7 Vertical Sync Pos	Actual-1 (0-255)	Actual-1	Actual-1	Actual-1	Actual-1
R8 Mode Reg Bits 0 and 1	Interlace Mode Select	Interlace Mode Select	Interlace Mode Select	Interlace Mode Select	Interlace Mode Select
Bits 2	—	—	—	Row/Column or Straight Binary Addressing	Row/Column or Straight Binary Addressing
Bits 3	—	—	—	Shared or Transparent Addr	Shared or Transparent Addr
Bits 4	—	—	Dispen Skew	Dispen Skew	Dispen Skew
Bits 5	—	—	Dispen Skew	Cursor Skew	Cursor Skew
Bits 6	—	—	Cursor Skew	RA4/UPSTB	RA4/UPSTB
Bits 7	—	—	Cursor Skew	Transparent Mode Select	Transparent Mode Select
R9 Scan Lines	Tot-1	Tot-1	Tot-1	Tot-1	Tot-1
R10 Cursor Start	Actual	Actual	Actual	Actual	Actual
R11 Cursor End	Actual	Actual	Actual	Actual	Actual
R12/R13 Disp Addr	Write Only	Write Only	Read/Write	Write Only	Write Only
R14/R15 Cursor POS	Write Only	Write Only	Read/Write	Read/Write	Read/Write
R16/R17 Lpen Reg	Read Only	Read Only	Read Only	Read Only	Read Only
R18/R19 Update Addr Reg	N/A	N/A	N/A	Transparent Mode Only	Transparent Mode Only
R31 Dummy Reg	N/A	N/A	N/A	Transparent Mode Only	Transparent Mode Only
Status Reg	No	No	No	Yes	Yes
Interlace Sync					
R0	Tot-1 = Odd	Tot-1 = Odd	Tot-1 = Odd	Tot-1 = Odd	Tot-1 = Odd or Even
Interlace Sync and Video					
R4 Vertical	Tot-1	Tot-1	Tot-1	Tot/2-1	Tot-1
R6 Vert Disp	Tot/2	Tot/2	Tot	Tot/2	Tot
R7 Vert Sync	Actual-1	Actual-1	Actual-1	Actual/2	Actual-1
R9 Scan Lines	Tot-2 Odd/Even	Tot-1 Only Even	Tot-2 Odd/Even	Tot-1 Odd/Even	Tot-1 Odd/Even
R10 Cursor Start R11 Cursor End	Both Odd or Both Even	Both Odd or Both Even	Odd/Even Odd/Even	Odd/Even Odd/Even	Odd/Even Odd/Even

VMC68C45 MEGACELL DESIGN KIT CRT CONTROLLER MEGACELL

FEATURES

- Completely integrated with VTI's extensive IC design tools and libraries
- 2-micron CMOS 68C45 Megacell configurable as:
  - 68C45R — CMOS equivalent to Motorola 6845R CRTC
  - 68C45R1 — CMOS equivalent to Motorola 6845R1 Enhanced CRTC
  - 68C45S — CMOS equivalent to Hitachi 6845S CRTC
  - 68C45SY — CMOS CRTC similar to Synertek 6545 CRTC
- 4.5 MHz video memory interface
- 3 MHz system processor interface
- Compatible with the VTI bus architecture
- Programmable Display Enable and Cursor delays (standard for S and SY versions—optional for R version)
- Row/column display memory addressing (SY version)
- Double-width character control

OPTIONAL FEATURES

- 16K, 32K, or 64K display Memory Address range (14-, 15-, or 16-bits)
- Programmable Vertical Sync pulse width
- 7-, 8-, or 9-bit Vertical Row counter

DESCRIPTION

Megacells are building block equivalents of standard LSI functions that can be combined with other megacells, standard cells or compiled cells to create custom User Specific ICs (USICs). Megacells are fully compatible with VTI's other cell technologies and design tools.

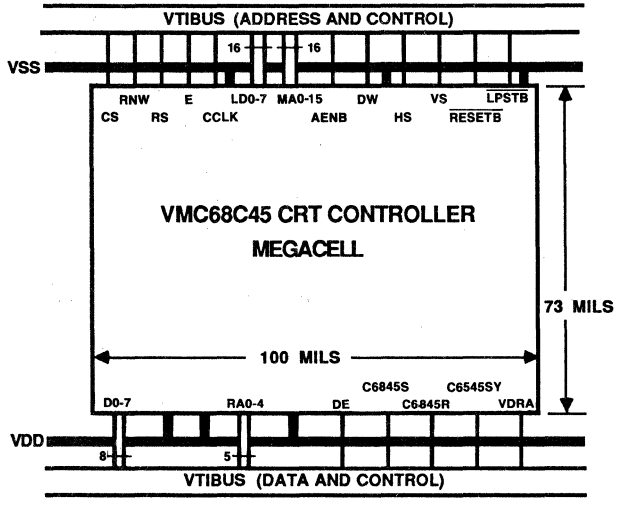
The VTI bus architecture allows multiple megacells to be combined on a single IC, along with additional cells from VTI's extensive libraries. This decreases the design time, cost and size of complex systems. A detailed simulation model provided with each megacell further reduces design verification time.

VMC68C45 MEGACELL DESIGN KIT DESCRIPTION

The VMC68C45 Megacell Design Kit includes the simulation models and icons required to permit designers using VTI's IC design tools to develop custom CRT controller designs.

Using the proven 68C45 LSI functional building block, implementing a specific CRT controller application requires only the combination of a 68C45 megacell with other logic on one or more VLSI ICs. For example, if a 68C45 megacell is combined with a ROM megacell character generator and "glue" logic, a complete CRT adapter for monochrome or color applications can be designed.

CONNECTOR DIAGRAM



SIGNAL DESCRIPTIONS

The following signals function the same on the VMC68C45 megacells and on the VL6845 family of CRT Controller ICs.

Signal	I/O	Description
RS	Input	Register Select
E	Input	Enable
CCLK	Input	Character Clock
LPSTB	Input	Light Pen Strobe
D0-D7	Input/Output	Data Bus
RA0-RA4	Output	Raster Address
HS	Output	Horizontal Sync
RESETB	Output	Reset

The following signals are unique or enhanced on the VMC68C45 megacells.

Signal	I/O	Description
RNW	Input	Same as R/$\overline{W}$, input on VL6845.
CS	Input	Same input as on VL6845, except active HIGH.
DW	Input	Double-width input—this input places the 68C45 in a double-width display mode.
AENB	Input	Address Enable input—when asserted LOW (AENB = "0") the MA outputs are enabled. AENB = "1" forces the MA outputs into a HIGH impedance state.
C6845R, C6845S, C6545SY	Input	One of these three inputs is tied HIGH to select the version of the 68C45 used in your application. The remaining two inputs must be grounded. NOTE: the 68C45SY megacell does not provide 6545 transparent addressing or the 6545 status register.
MA0-MA13, 14, 15	Output	14-, 15-, or 16-bit Video Memory Address bus—These tri-state outputs provide the binary address to the external video RAM. If row/column addressing is selected (SY version only) this bus will provide row/column addressing to the external RAM instead of binary addressing. The AENB input signal can be used to place the MA bus in the HIGH impedance state.
DE	Output	Display Enable output—active (DE = "1") when the 68C45 is generating active display information. The S version can be programmed with a 0, 1, or 2 character delay. The SY version can be programmed for a 0 or 1 character delay.
CURSOR	Output	Cursor output—this signal is HIGH when the raster scan coincides with the programmed cursor position. The S version can be programmed with a 0, 1, or 2 character delay. The SY version can be programmed for a 0 or 1 character delay.
VS	Output	Vertical Sync output—active HIGH pulse which determines the vertical placement of the video data. An optional feature permits programming the Vertical Sync pulse width.
LD0-LD13, 14, 15	Input/ Output	14-, 15-, or 16-bit Advanced Memory Address bus—separate video memory address information on this bus precedes the information on the MA bus by one character clock. This bus is provided to interface with a separate strip of logic for split display capability.
VDRA (reserved)	n/c	Reserved for future expansion—to be left unconnected.

ORDER INFORMATION

VMC68C45-c*-m** Complete Design Kit for CMOS 68C45 Megacell

*c	Computer Type
A	Apollo workstation
V	VAX workstation
R	RIDGE workstation
E	ELXSI workstation
W	WANG workstation

**m	Media Format
1	Floppy diskette
2	Magnetic tape
3	Cartridge

VL82C37A

CMOS DIRECT MEMORY ACCESS (DMA) CONTROLLER

FEATURES

- Low-power CMOS version of popular 8237A DMA controller
- Four DMA channels
- Individual enable/disable control of DMA requests
- Directly expandable to any number of channels
- Independent auto-initialize feature for all channels
- Address increment or decrement
- High-performance: up to 8 MHz (VL82C37A-08)
- Transfers may be terminated by end of process input
- Software controlled DMA requests
- Independent polarity control for DREQ and DACK signals

DESCRIPTION

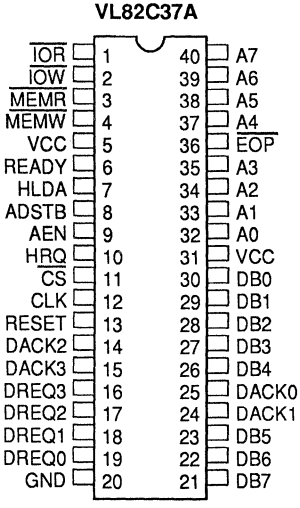
The VL82C37A Direct Memory Access (DMA) Controller serves as a peripheral interface circuit for microprocessor systems, and is designed to improve system performance by allowing external devices to directly transfer information from the system memory. Memory-to-memory transfer capability is also provided. The VL82C37A DMA Controller offers many programmable control features that enhance data throughput and system performance. Dynamic reconfiguration is permitted under program control.

The VL82C37A is designed to be used with an external 8-bit address register such as the 8282. In addition to the four independent channels, the VL82C37A is expandable to any number of channels by cascading additional controller devices.

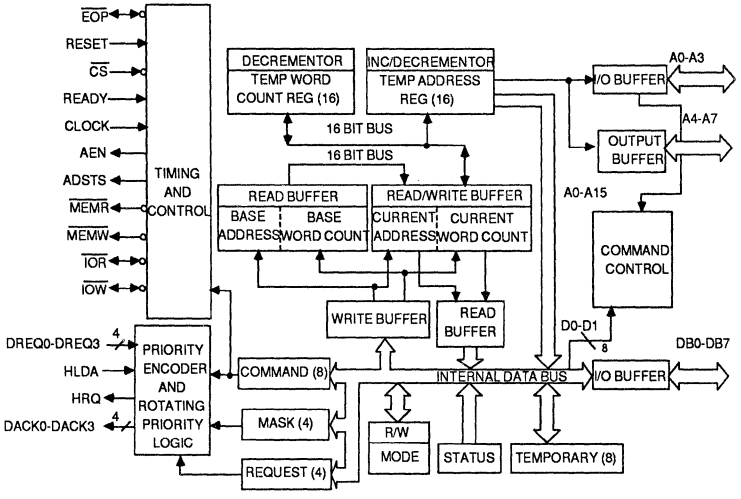
Three basic transfer modes allow the user to program the types of DMA service. Each channel can be individually programmed to auto-initialize to its original condition following an End-of-Process (EOP) input.Each channel also has a 64K address and word count handling ability.

The VL82C37 DMA Controller is available in 4 MHz, 5 MHz, and 8 MHz clock frequencies.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL82C37A-04-PC	4 MHz	Plastic DIP
VL82C37A-04-CC		Ceramic DIP
VL82C37A-04-QC		Plastic Leaded Chip Carrier
VL82C37A-05-PC	5 MHz	Plastic DIP
VL82C37A-05-CC		Ceramic DIP
VL82C37A-05-QC		Plastic Leaded Chip Carrier
VL82C37A-08-PC	8 MHz	Plastic DIP
VL82C37A-08-CC		Ceramic DIP
VL82C37A-08-QC		Plastic Leaded Chip Carrier

Note: Operating temperature is 0°C to +70°C

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
CLK	12	Clock input: Controls the internal operations of the VL82C37A DMA Controller and its rate of data transfers. This input may be driven at up to 4 MHz for the standard VL82C37A-04 and up to 8 MHz for the VL82C37A-08.
$\overline{CS}$	11	Chip Select: An active-low input used to select the VL82C37A as an I/O device during the idle cycle, allows CPU communication on the data bus.
RESET	13	Reset: An active-high input that clears the Command, Request, and Temporary Registers, clears the first/last flip-flop, and sets the Mask Register.The device is in the idle cycle following a Reset signal.
READY	6	Ready: An input that extends the memory read and write pulses from the VL82C37A accomodating slow memories or I/O peripheral devices. During its specified setup/hold time, Ready must not make transitions.
HLDA	7	Hold Acknowledge: This active-high signal from the CPU indicates that it has relinquished control of the system busses.
DREQ0-DREQ3	19 - 16	DMA Request: These lines are individual asynchronous channel request inputs. Peripheral circuits use these lines to obtain DMA service. In fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. Activating the DREQ line of a channel generates a request. DACK then acknowledges the recognition of DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ must be sustained until the corresponding DACK becomes active.
DB0 - DB7	30 - 26, 23 - 21	Data Bus: These lines are bidirectional, three-state signals that connect to the system data bus. The outputs are enabled in the program condition during the I/O read to output the contents of an Address Register, a Status Register, the Temporary Register, or a Word Count Register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the VL82C37A control registers. During DMA cycles the most significant eight bits of the address are sent onto the data bus and are strobed into an external latch by ADSTB. In memory-to-memory operations, data from the memory comes into the VL82C37A on the data bus during the read-from-memory transfer. In the write-to-memory transfer, the data bus outputs determine the placement of the data, not the new memory location.
$\overline{IOR}$	1	I/O Read: This is a bidirectional, active-low, three-state line. In the idle cycle, it is an input control signal used by the CPU to read the control registers. In the active cycle, it is an output control signal used by the VL82C37A to access data from a peripheral during a DMA Write transfer.
$\overline{IOW}$	2	I/O Write: This signal is a bidirectional actie-low, three-state line. It is used by the CPU to load information into the VL82C37A DMA Controller. In the active cycle, it is used as an output control signal used by the VL82C37A to load data to the peripheral during a DMA read transfer.
$\overline{EOP}$	36	End of Process: This is an active-low bidirectional signal, which provides data on the completion of DMA services and is available at the bidirection $\overline{EOP}$ pin. The VL82C37A allows an external signal to terminate an active DMA service, by pulling the $\overline{EOP}$ input low with an external $\overline{EOP}$ signal. The VL82C37A also generates a pulse when the terminal count (TC) for any channel is achieved. This generates an $\overline{EOP}$ signal that is active on the $\overline{EOP}$ Line. When $\overline{EOP}$ is received, either internally or externally, it will cause the VL82C37A to terminate the service, reset the request, and, if auto-initialize is enabled, to write the base registers to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by $\overline{EOP}$, unless the channel is programmed for auto-initialize. In that case, the mask bit remains unchanged. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs.To prevent erroneous end-of-process inputs, $\overline{EOP}$ should be tied high with a pull-up resistor if it is not used.
VCC	5, 31	+5 V ±5% power supply
GND	20	Ground

SIGNAL DESCRIPTIONS (CONT.)

Signal Name	Pin Number	Signal Description
A0 - A3	32 - 35	The four least significant address lines: These lines are bidirectional three-state signals. In the idle cycle, they are inputs used by the CPU to address the register to be loaded or read. In the active cycle they are outputs that provide the lower four bits of the output address to the system.
A4 - A7	37 - 40	The four most significant address lines: These lines are three-state outputs that provide four bits of address. They are enabled only during the DMA service.
HRQ	10	Hold Request: This is the hold request to the CPU. It is used to request control of the system bus. If the corresponding mask bit is clear, the presence of any valid DREQ causes the VL82C37A to issue the HRQ signal. After HRQ is asserted, at least one clock cycle (TCY) must occur before HLDA can be valid.
DACK0 - DACK3	25, 24, 14, 15	DMA Acknowledge: This signal is used to notify an individual peripheral when it has been granted a DMA cycle. The sense of these lines is programmable; Reset initializes them to an active-low.
AEN	9	Address Enable: This active-high line enables the 8-bit latch containing the upper eight address bits onto the system address bus. It can also be used to disable other system bus drivers during DMA transfers.
ADSTB	8	Address Strobe: This active-high is used to strobe the upper address byte into an external latch.
$\overline{\text{MEMR}}$	3	Memory Read: This active-low signal is a three-state output used to access data from a selected memory location during a DMA read or memory-to-memory transfer.
$\overline{\text{MEMW}}$	4	Memory Write: This signal is an active-low three-state output used to write data to a selected memory location during a DMA write or memory-to-memory transfer.

TABLE 1. INTERNAL REGISTERS

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Register	4 bits	1
Request Register	4 bits	1

FUNCTIONAL DESCRIPTION

The internal registers and major logic blocks of the VL82C37A are shown in the block diagram. Data interconnection paths are also shown, but the various control signals between the blocks are not. The VL82C37A contains 344 bits of internal register memory. Figure 3 describes these registers and shows them by size. A complete description of the registers and their functions can be found in the Register Descriptions section.

The VL82C37A contains three basic control logic blocks. The Timing Control block generates internal timing and external control signals for the VL82C37A. The program command control block decodes the various commands given to the VL82C37A by the microprocessor before servicing a DMA Request. Further, it decodes the mode control word used to select the type of DMA during the servicing. The priority encoder block settles priority contention between DMA channels requesting service at the same time.

The external clock drives the timing control block. In most VL82C37A systems, this clock will usually be the Ø2 TTL clock from an VL82C84A. For 8085AH-2 systems above 3.9 MHz, the 8085 CLK(OUT) will not meet VL82C37A-05 (5 MHz) clock low and high time requirements. In this case, an external clock should be used to drive the VL82C37A-05.

DMA OPERATION

The VL82C37A is designed to operate in two major cycles: the idle and active . Several states are contained in each device cycle. The VL82C37A supports seven separate states, each being one full clock period. State I (SI), the inactive state, is entered when the VL82C37A has no valid DMA requests pending. While in SI, the DMA controller is inactive but may be in the program condition, being programmed by the processor. State 0 (S0) is the first state of a DMA service. The VL82C37A has requested a hold, but the processor has not yet responded with an acknowledge. The VL82C37A may still be programmed until it receives HLDA from the CPU. An acknowledge from the CPU signals that DMA transfers may begin. S1, S2, S3 and S4 are the functional states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (WS) can be placed between S2 or S3 and S4 by using the Ready line on the VL82C37A. The data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active simultaneously. The data is not read into or driven out of the VL82C37A during I/O-to-memory or memory-to-I/O DMA transfers.

To complete memory-to-memory transfers requires a read-from and a write-to-memory. The states, which resemble the normal working states, use two-digit numbers for identification. Eight states are needed for each transfer: the first four states (S11, S12, S13, S14), are used for read-from-memory and the last four states (S21, S22, S23, S24), for the write-to-memory of the transfer.

IDLE CYCLE

When no channels are requesting service, the VL82C37A enters the idle cycle and performs SI states, sampling the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device also samples $\overline{CS}$, looking for an attempt by the microprocessor to write or read to the internal registers of the VL82C37A. When $\overline{CS}$ is low and HLDA is low, the VL82C37A initiates the program condition. The CPU now establishes, changes or inspects the internal definition of the part by reading from or writing to the internal register. Address lines AO-A3 are inputs to the device. They select registers that will be read or written. The $\overline{IOR}$ and $\overline{IOW}$ lines are used to select and time reads or writes. Because of the number and size of the internal registers, an internal flip-flop is used to generate one more bit of address. This bit is used to determine the upper or lower byte of the 16-bit address and Word Count Registers. This flip-flop can be reset by a separate software command.

Special software commands executed in the VL82C37A during the program condition are decoded as sets of addresses with the $\overline{CS}$ and $\overline{IOW}$ signals. The commands do not use the data bus. Clear First/Last Flip-Flop and Master Clear instructions are included.

ACTIVE CYCLE

When the VL82C37A is in the idle cycle and a nonmasked channel requests a DMA service, the device outputs an HRQ to the microprocessor and then enters the active cycle. During this cycle the DMA service takes place, in one of four modes.

In the single transfer mode, the device is programmed to make only one transfer. The word count is decremented and the address decremented or incremented, following each transfer. When the word countis completed from zero to FFFFH, a Terminal Count (TC) causes an auto-initialize if the channel has been so programmed.

The DREQ signal must be held active until DACK becomes active, in order to be recognized. If DREQ is held active for the entire single transfer, HRQ will become inactive and release the bus to the system. It again goes active and, upon receipt of a new HLDA, another single transfer is performed. In 8080A, 8085AH, 8088, or 8086 systems this insures one full machine cycle execution between DMA transfers. Details of timing between the VL82C37A and other bus control protocols depends upon the characteristics of the microprocessor involved.

In the block transfer mode, the device is activated by the DREQ signal to continue making transfers during the service until a TC, caused by word count going to FFFFH, or an external end of process ($\overline{EOP}$) is encountered. DREQ need only be held active until DACK becomes active. An auto-initialization will occur at the end of the service, if the channel has been programmed for it.

In the demand transfer mode the device is programmed to continue making transfers until a TC or external $\overline{EOP}$ is encountered or until the DREQ signal goes inactive. Transfers may continue until the I/O device has exhausted its data capacity. After the I/O device has caught up, the DMA service is re-established by a DREQ signal. During the interval between services, when the microprocessor is operating, the intermediate values of address and word count are stored in the VL82C37A Current Address and Current Word Count Registers. Only an $\overline{EOP}$ can cause an auto-initialize at the end of the service. $\overline{EOP}$ is generated either by TC or by an external signal.

The fourth mode cascades multiple VL82C37As together for easy system expansion. The HRQ and HLDA signals from additional VL82C37As are connected to the DREQ and DACK signals of a channel of the primary VL82C37A. This permits the DMA requests of the additonal device to propagate through the priority network circuitry of the preceding device. The priority chain is not broken, and the new device waits for its turn to acknowledge requests. As the cascade channel of the primary VL82C37A is used only to prioritize the additional device, it does not produce any address or control signals of its own, which could conflict with the outputs of the active channel in the added device. The VL82C37A responds to the DREQ and DACK signal, but all other outputs except HRQ are disabled.

Figure 8 shows two devices cascaded into a primary device using two of the previous channels. This forms a two-level DMA system. More VL82C37A's could be added at the second level by using the remaining channels of the first level. More devices can also be cascaded into the channels of the second-level devices, forming a third level.

TRANSFER TYPES

Each of the three modes of active transfer can perform three different types of transfers: read, write and verify. Write transfers move data from an I/O device to the memory by activating $\overline{\text{MEMW}}$ and $\overline{\text{IOR}}$; read transfers move data from memory to an I/O device by activating $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$.

Verify transfers are pseudo routines: the VL82C37A DMA Controller operates as in read or write transfers generating addresses, and responding to $\overline{\text{EOP}}$, and other operations.The memory and I/O control lines remain inactive. The verify mode is not permitted during memory-to-memory operation.

To perform block moves of data from one memory address space to another with a minimum of programming, the VL82C37A includes a memory-to-memory transfer feature. Programming a bit in the Command Register selects channels 0 and 1 to operate as memory-to-memory transfer channels. The transfer is initiated by setting the software DREQ for channel 0. The VL82C37A requests a DMA device as usual. After HLDA is true, the device, using eight-state transfers in block transfer mode, reads data from the memory. The channel 0 Current Address Register is the source for the address, and is decremented or incremented as usual. The data byte read from the memory is then stored in the VL82C37A internal Temporary Register. Channel 1 writes the data from the Temporary Register to memory using the address in its Current Address Register and incrementing or decrementing it as usual. The channel 1 current word count is decremented. When the word count goes to FFFFH, a TC is generated causing an $\overline{\text{EOP}}$ output terminating the service.

Channel 0 may be programmed to hold the same address for all transfers, which permits a single word to be written to a block of memory.

The VL82C37A responds to external $\overline{\text{EOP}}$ signals during memory-to-memory transfers. In block search schemes data comparators may use this input on finding a match. The timing of memory-to-memory transfers is shown in Figure 10. Memory-to-memory operatons can be detected as an active AEN signal with no DACK outputs.

A channel may be set up to auto-initialize by setting a bit in the Mode Register. During nitialization, the original values of the Current Address and Current Word Count Registers are automatically restored from the Base Address and Base Word Count Registers of that channel following $\overline{\text{EOP}}$. The base registers and the current registers are loaded at the same time. They remain unchanged thoughout the DMA service. The mask bit is not set when the channel is in auto-initialize. Following auto-initialize, the channel is prepared to perform another DMA service, without CPU action, as soon as a valid DREQ is detected.

The VL82C37A has two types of priority encoding available as software-selectable options. The fixed priority option sets the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3, then 2,1 and the highest priority channel is 0. After recognizing any one channel for service, the other channels are prevented from interferring with that service until it is completed.

In the rotating priority option, the last channel to get service becomes the lowest priority channel with the others rotating in order.

Rotating priority allows a single chip DMA system. Any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from dominating the system.

To achieve even greater throughput where system characteristics permit, the VL82C37A DMA Controller can compress the transfer time to two clock cycles. State S3 is used to extend the access time of the read pulse. By removing state S3, the read pulse width is made equal to the write pulse width, and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 state still occurswhen A8-A15 need updating (see the Address Generation section.)

To reduce pin count, the VL82C37A multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch, where they may be placed on the address bus. The falling edge of the Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. The lower order address bits are directly sent by the VL82C37A . Lines A0-A7 are connected to the address bus.

During block and demand transfer mode services, including multiple transfers, the addresses generated will be in order. During a large number of transfers the data held in the external address latch will not change. This data will change when a carry or borrow from A7 to A8 takes place in the normal order of addresses. To expedite transfers, the VL82C37A DMA Controller executes S1 states only when needed to update A8-A15 in the latch. For long services, S1 states and address strobes may occur only once every 256 transfers, a savings of 255 clock cycles for each 256 transfers.

REGISTER DESCRIPTION

Current Address Register: Each channel has a 16-bit Current Address Register. This register holds the value of the address used during DMA transfers.

The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address Register throughout the transfer. The microprocessor reads this register in successive 8-bit bytes. It may also be reinitialized by an auto-initialize to its original value which takes place only after an $\overline{EOP}$.

Current Word Register: Each channel has a 16-bit Current Word Count Register that determines the number of transfers to be performed. The actual number of transfers is one more than the number programmed in the Current Word Count Register; programming a count of 100 will result in 101 transfers. The word count is decremented after each transfer; the intermediate value of this word count is stored in the register during the transfer. When the value in the register goes from 0 to FFFFH, a TC is generated. The register is then loaded or read in successive 8-bit bytes by the microprocessor in the program condition. Following the end of a DMA service, it may also be reinitialized by an auto-initialization to its original value which occurs only on $\overline{EOP}$. If it is not auto-initialized, this register has a count of FFFFH after TC.

Base Address and Base Word Count Registers: Each channel has a pair of 16-bit Base Address and Base Word Count Registers that store the orginal value of their associated current registers. Throughout auto-initialization these values are used to restore the current registers to their original values. The base registers are written at the same time with their corresponding current register in 8-bit bytes in the program condition by the microprocessor. These registers cannot be read by the microprocessor.

Command Register: This 8-bit register controls the operation of the VL82C37A, is programmed by the microprocessor in the program condition and is cleared by reset or a master clear instruction. Figure 2 lists and describes the function of the command bits.

Mode Register: All channels have a 6-bit Mode register. When the register is being written to by the microprocessor in the program condition, bits 0 to 1 determine which channel the Mode Register is to be written.

Request Register: The VL82C37A can responds to requests for DMA service that are initiated by software as well as by a DREQ signal. Each channel has a request bit associated with it in the 4-bit Request Register. These are non-maskable and can be prioritized by the priority encoder network.

Each register bit is set or reset separately under software control, or is cleared upon generation of a TC or external $\overline{EOP}$. The entire register is cleared by a Reset. To set or reset a bit, the software loads the correct form of the data word.Table 2 shows register address coding. To make a software request, the channel must be in block mode.

Mask Register: Each channel has an associated mask bit that can be set to disable the incoming DREQ signal. A mask bit is set when its associated channel produces an $\overline{EOP}$, if the channel is not programmed for auto-initialize. Any bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is set by a reset, which disables all DMA requests until a clear Mask Register instruction allows them to occur. This instruction to separately set or clear the mask bits is similar in form to that used with the Request Register.

Status Register: The Status Register is available to be read out of the VL82C37A DMA Controller by the microprocessor and contains information about the status of the devices at this point. This information includes which channels have reached a terminal count and which channels have pending DMA requests.

Bits 0-3 are set each time a TC is reached by that channel or an external $\overline{EOP}$ is applied and are cleared upon reset and on every status read. Bits 4 through 7 are set whenever their corresponding channel is requesting service.

Temporary Register: The Temporary Register is used to hold data during memory-to-memory transfers. The last word moved can be read by the microprocessor in the Program Condition following the completion of the transfers. The Temporary Register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a reset.

Software Commands: These additional special software commands can be executed in the program condition and do not depend on any specific bit pattern on the data bus.

The clear first/last flip-flop command is executed prior to writing or reading new address or word count information to the VL82C37A. This initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

The Master Clear software instruction has the same effect as the hardware reset. The Command, Status, Request, Temporary, and Internal First/Last Flip-Flop Registers are cleared and the Mask Register is set. The VL82C37A enters an idle cycle.

The Clear Mask Register command clears the mask bits of all four channels, enabling them to accept DMA requests.

PROGRAMMING

The VL82C37A DMA Controller accepts programming from the host processor any time that HLDA is inactive, even if the HRQ signal is active. The host must assure that programming and HLDA are mutually exclusive. A problem can occur if a DMA request occurs, on an unmasked channel while the VL82C37A is being programmed.

For example, the CPU may be starting to reprogram the two-byte Address Register of a channel when that channel receives a DMA request. If the VL82C37A is enabled (bit 2 in the command register is 0) and that channel is unmasked, a DMA service will occur after one byte of the Address Register has been reprogrammed. This can be avoided by disabling the controller - setting bit 2 in the command register - or masking the channel before programming another registers. Once the programming is complete, the controller can be enabled (unmasked).

After power-up all internal locations, including the Mode registers, should be loaded with a valid value. This should be done to unused channels as well.

APPLICATION

Figure 1 shows a convenient method for configuring a DMA system with the VL82C37A DMA Controller and an 8080A/8085AH microprocessor system. Whenever there is at least one valid DMA request from a peripheral device, the multimode VL82C37A DMA Controller issues a HRQ to the processor. When the processor replies with a HLDA signal, the VL82C37A takes control of the address, data, and control buses. The address for the first transfer operation is output in two bytes - the least significant eight bits on the eight address outputs, and the most significant eight bits on the data bus. The contents of the data bus are then latched into the 8282 8-bit latch to complete the full 16 bits of the address bus. The 8282 is a high-speed, 8-bit, three-state latch in a 20-pin DIP package. After the initial transfer takes place, the latch is updated only after a carry or borrow is generated in the least significant address byte. Four DMA channels are available when one VL82C37A DMA Controller is used.

FIGURE 1. SYSTEM INTERFACE

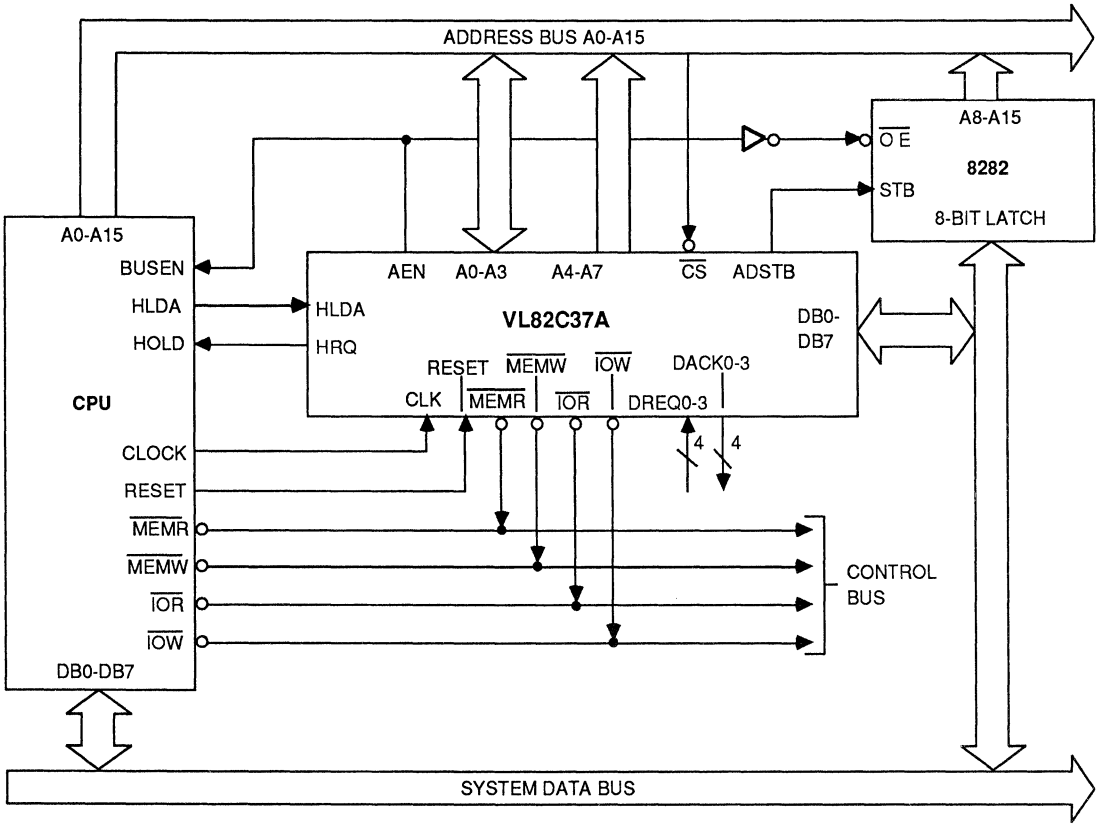


FIGURE 2. COMMAND REGISTER

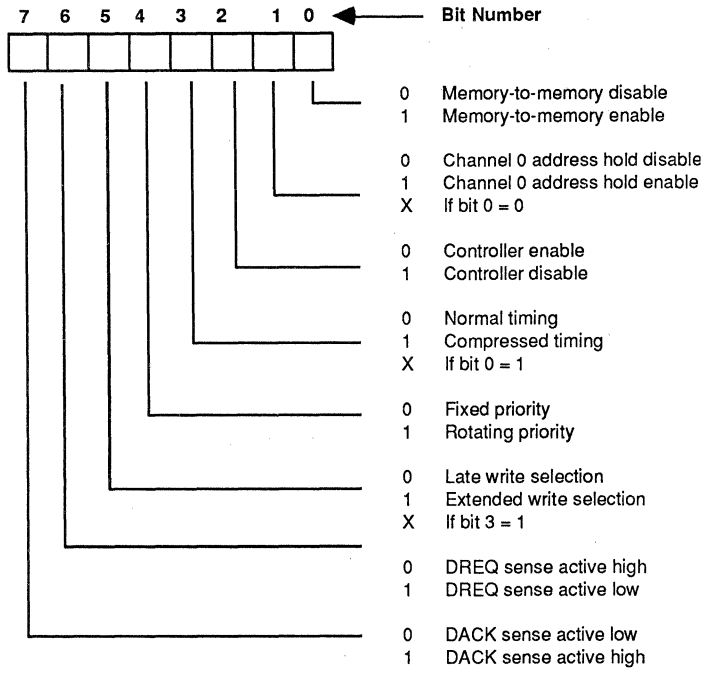


FIGURE 3. MODE REGISTER

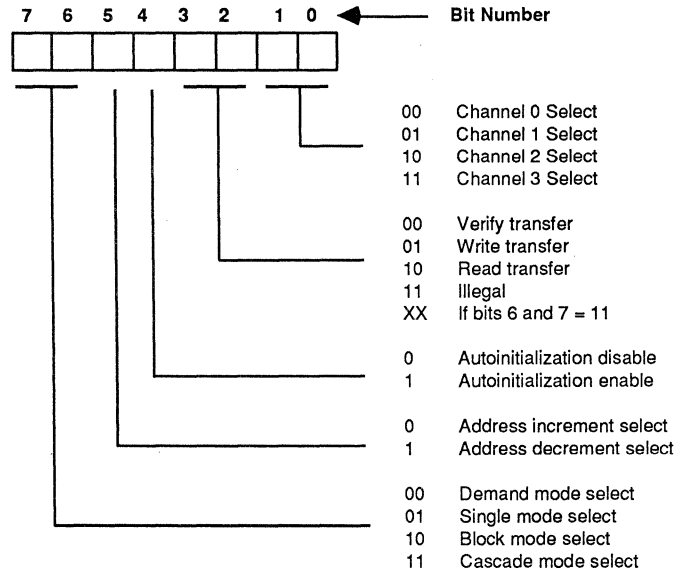


FIGURE 4. REQUEST REGISTER

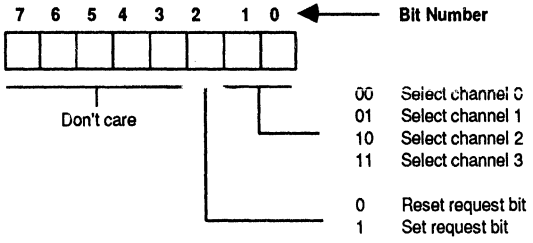


FIGURE 5. STATUS REGISTER

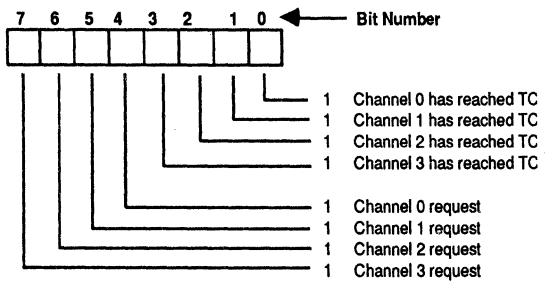


FIGURE 6. MASK REGISTER (SELECT MODE)

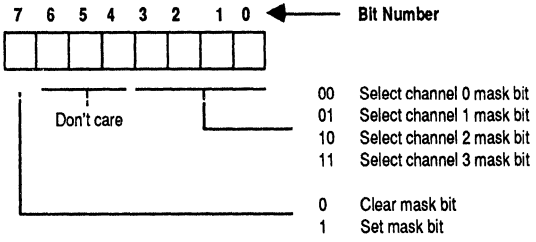


FIGURE 7. MASK REGISTER (MASK MODE)

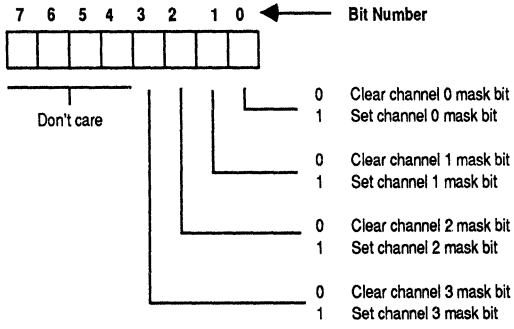


TABLE 2. REGISTER CODES

Register	Operation	Signals						
		$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0
Command	Write	0	1	0	1	0	0	0
Mode	Write	0	1	0	1	0	1	1
Request	Write	0	1	0	1	0	0	1
Mask	Set/Reset	0	1	0	1	0	1	0
Mask	Write	0	1	0	1	1	1	1
Temporary	Read	0	0	1	1	1	0	1
Status	Read	0	0	1	1	0	0	0

TABLE 3. SOFTWARE COMMAND CODES

Signals						Operation
A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$	
1	0	0	0	0	1	Read Status Register
1	0	0	0	1	0	Write Command Register
1	0	0	1	0	1	Illegal
1	0	0	1	1	0	Write Request Register
1	0	1	0	0	1	Illegal
1	0	1	0	1	0	Write Single Mask Register Bit
1	0	1	1	0	1	Illegal
1	0	1	1	1	0	Write Mode Register
1	1	0	0	0	1	Illegal
1	1	0	0	1	0	Clear Byte Pointer Flip/Flop
1	1	0	1	0	1	Read Temporary Register
1	1	0	1	1	0	Master Clear
1	1	1	0	0	1	Illegal
1	1	1	0	1	0	Clear Mask Register
1	1	1	1	0	1	Illegal
1	1	1	1	1	0	Write All Mask Register Bits

FIGURE 8. CASCADED VL82C37A CONTROLLERS

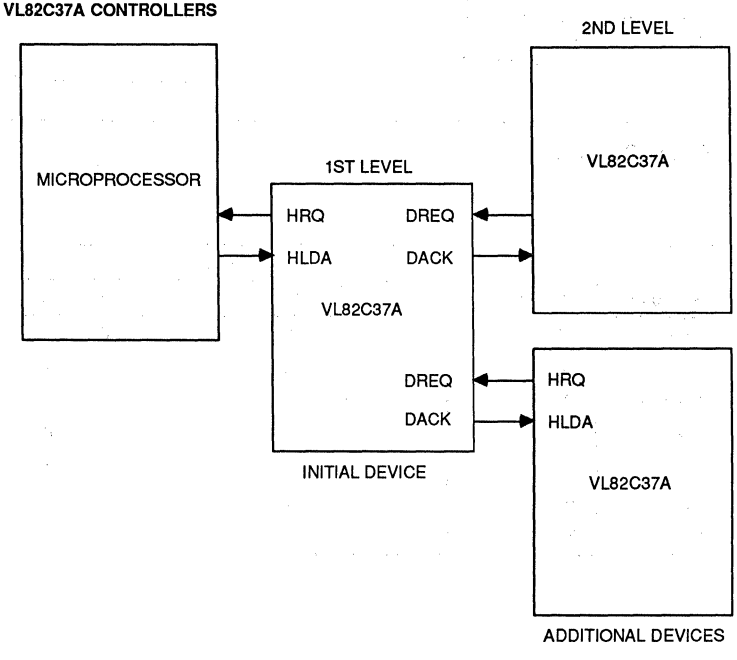


TABLE 4. WORD COUNT AND ADDRESS REGISTER COMMAND CODES

Channel	Register	Operation	Signals							Internal Flip-Flop	Data Bus DB0-DB7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		
0	Base and Current Address	Write	0	1	0	0	0	0	0	0	A0-A7
			0	1	0	0	0	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0-A7
			0	0	1	0	0	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	0	1	0	W0-W7
			0	1	0	0	0	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	0	1	0	W0-W7
			0	0	1	0	0	0	1	1	W8-W15
1	Base and Current Address	Write	0	1	0	0	0	1	0	0	A0-A7
			0	1	0	0	0	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0-A7
			0	0	1	0	0	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	1	1	0	W0-W7
			0	1	0	0	0	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	1	1	0	W0-W7
			0	0	1	0	0	1	1	1	W8-W15
2	Base and Current Address	Write	0	1	0	0	1	0	0	0	A0-A7
			0	1	0	0	1	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0-A7
			0	0	1	0	1	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	0	1	0	W0-W7
			0	1	0	0	1	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	0	1	0	W0-W7
			0	0	1	0	1	0	1	1	W8-W15
3	Base and Current Address	Write	0	1	0	0	1	1	0	0	A0-A7
			0	1	0	0	1	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0-A7
			0	0	1	0	1	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	1	1	0	W0-W7
			0	1	0	0	1	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	1	1	0	W0-W7
			0	0	1	0	1	1	1	1	W8-W15

TABLE 5. DMA MODE AC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ±5%

Symbol	Parameter	VL82C37A-04		VL82C37A-05		VL82C37A-08		Unit
		Min	Max	Min	Max	Min	Max	
TAEL	AEN HIGH from CLK LOW (S1) Delay Time		225		200		105	ns
TAET	AEN LOW from CLK HIGH (S1) Delay Time		150		130		80	ns
TAFAB	ADR Active to Float Delay from CLK HIGH		120		90		55	ns
TAFC	Read or Write Float from CLK HIGH		120		120		75	ns
TAFDB	DB Active Float Delay from CLKHIGH		190		170		135	ns
TAHR	ADR from Read HIGH Hold Time	TCY-100		TCY-100		TCY-75		ns
TAHS	DB from ADSTB LOW Hold Time	40		30		20		ns
TAHW	ADR from Write HIGH Hold Time	TCY-50		TCY-50		TCY-50		ns
TAK	DACK Valid from CLK LOW Delay Time (Note 7)		220		170		105	ns
	$\overline{EOP}$ HIGH from CLK HIGH Delay Time (Note 10)		190		170		105	ns
	$\overline{EOP}$ LOW from CLK HIGH Delay Time		190		170	-	105	ns
TASM	ADR Stable from CLK HIGH		190		170		105	ns
TASS	DB to ADSTB LOW Setup Time	100		100		65		ns
TCH	Clock HIGH Time (Transitions ≤ 10 ns)	100		80		55		ns
TCL	Clock LOW Time (Transitions ≤ 10 ns)	110		68		43		ns
TCY	CLK Cycle Time	250		200		125		ns
TDCL	CLK HIGH to Read or Write LOW Delay (Note 4)		200		190		120	ns
TDCTR	Read HIGH from CLK HIGH (S4) Delay Time (Note 4)		210		190		115	ns
TDCTW	Write HIGH from CLK HIGH (S4) Delay (Note 4)		150		130		80	ns
TDQ1	HRQ Valid from CLK HIGH Delay Time (Note 5)		120		120		75	ns
TDQ2			190		120		75	ns
TEPS	$\overline{EOP}$ LOW from CLK LOW Setup Time	45		40		25		ns
TEPW	$\overline{EOP}$ Pulse Width	225		220		135		ns
TFAAB	ADR Float to Active Delay from CLKHIGH		190		170		100	ns
TFAC	Read or Write Active from CLK HIGH		150		150		90	ns
TFADB	DB Float to Active Delay from CLK HIGH		225		200		110	ns
THS	HLDA Valid to CLK HIGH Setup Time	75		75		45		ns
TIDH	Input Data from $\overline{MEMR}$ HIGH Hold Time	0		0		0		ns
TIDS	Input Data to $\overline{MEMR}$ HIGH Setup Time	190		170		90		ns
TODH	Output Data from $\overline{MEMW}$ HIGH Hold Time	20		10		10		ns
TODV	Output Data Valid to $\overline{MEMW}$ HIGH	125		125		90		ns
TQS	DREQ to CLK LOW (S1,S4) Setup Time	0		0		0		ns
TRH	CLK to READY LOW Hold Time	20		20		20		ns
TRS	READY to CLK LOW Setup Time	60		60		35		ns
TSTL	ADSTB HIGH from CLK HIGH Delay Time		150		130		110	ns
TSTT	ADSTB LOW from CLK HIGH Delay Time		110		90		65	ns

Explanatory notes follow DC Characteristics Table.

FIGURE 9. DMA TRANSFER TIMING (SEE TABLE 5.)

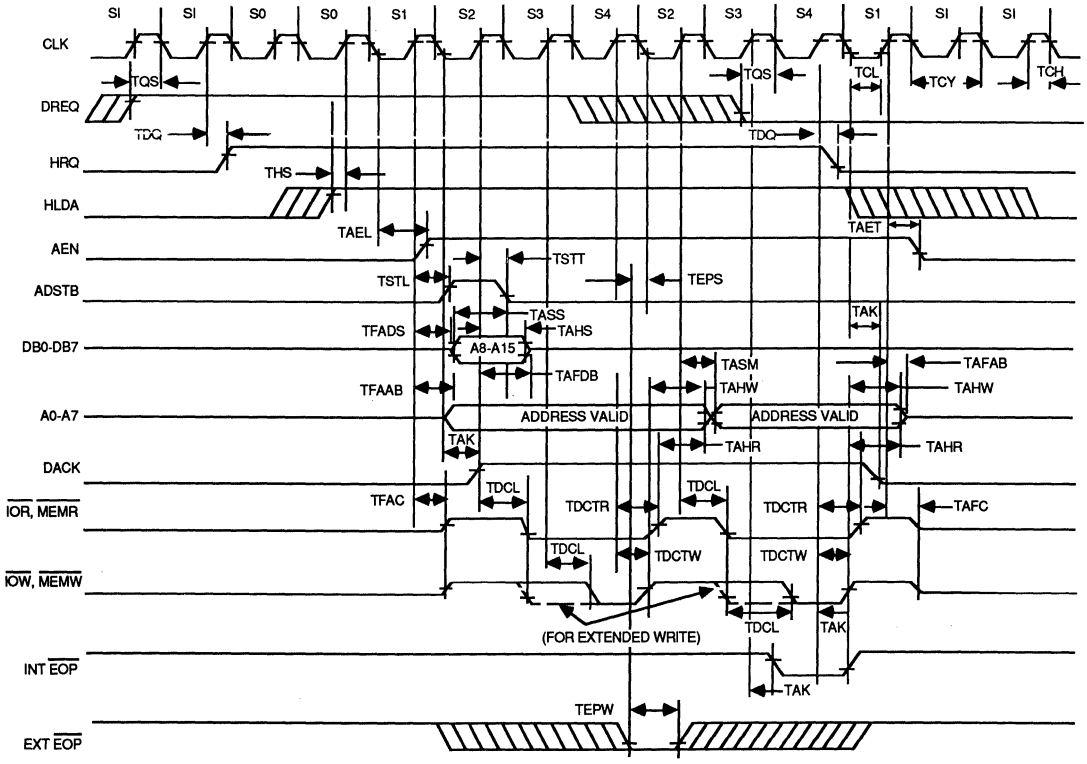


FIGURE 10. MEMORY-TO-MEMORY TRANSFER TIMING (SEE TABLE 5)

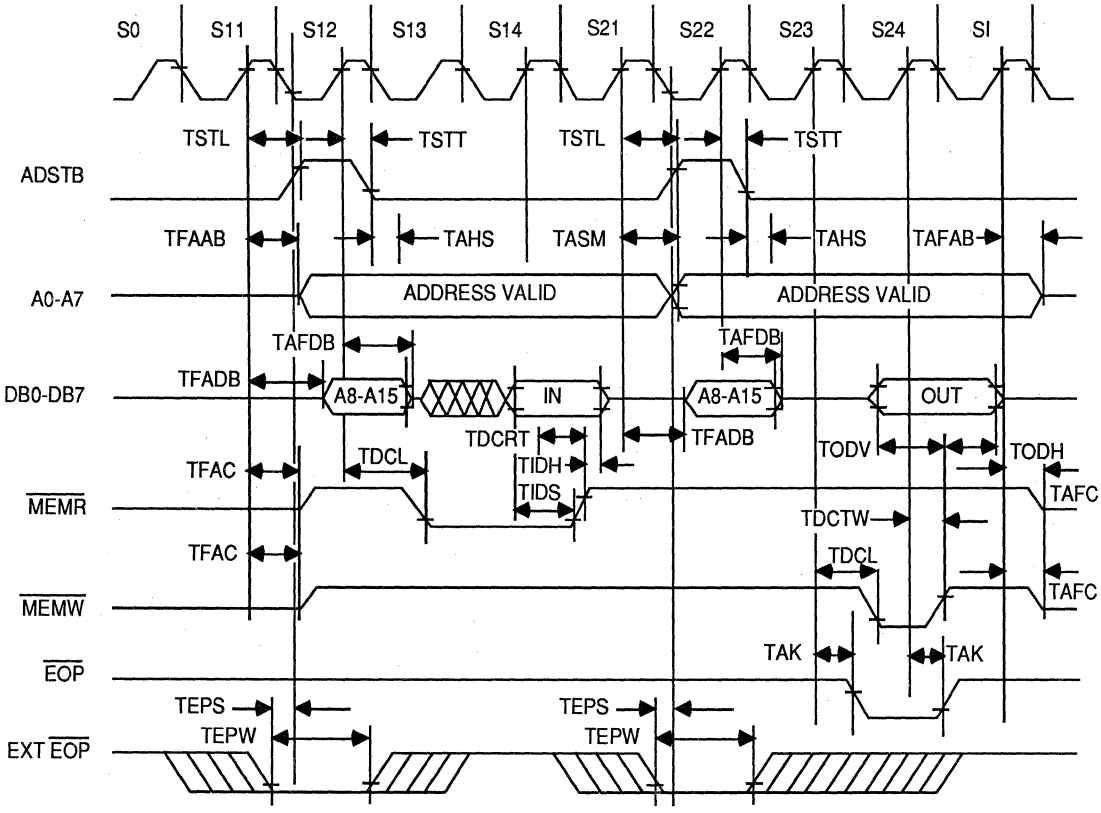


TABLE 6. PERIPHERAL MODE AC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ±5%

Symbol	Parameter	VL82C37A-04		VL82C37A-05		VL82C37A-08		Unit
		Min	Max	Min	Max	Min	Max	
TAR	ADR Valid or $\overline{CS}$ LOW to Read LOW	50		50		30		ns
TAW	ADR Valid to Write HIGH Setup Time	150		130		80		ns
TCW	CS LOW to Write HIGH Setup Time	150		130		80		ns
TDW	Data Valid to Write HIGH Setup Time	150		130		80		ns
TRA	ADR or CS Hold from Read HIGH	0		0		0		ns
TRDE	Data Access from Read LOW (Note 3)		200		140		120	ns
TRDF	DB Float Delay from Read HIGH	20	100	0	70	0	70	ns
TRSTD	Power Supply HIGH to RESET LOW Setup Time	500		500		500		ns
TRSTS	RESET to First $\overline{IOW}$	2TCY		2TCY		2TCY		ns
TRSTW	RESET Pulse Width	300		300		300		ns
TRW	Read Width	250		200		155		ns
TWA	ADR from Write HIGH Hold Time	20		20		10		ns
TWC	CS HIGH from Write HIGH Hold Time	20		20		10		ns
TWD	Data from Write HIGH Hold Time	30		30		20		ns
TWWS	Write Width	200		160		100		ns

Explanatory notes follow DC Characteristics Table.

FIGURE 11. SLAVE MODE WRITE TIMING (SEE TABLE 6)

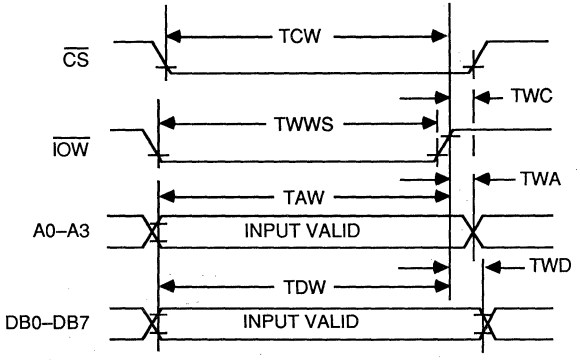


FIGURE 12. SLAVE MODE READ TIMING (SEE TABLE 6)

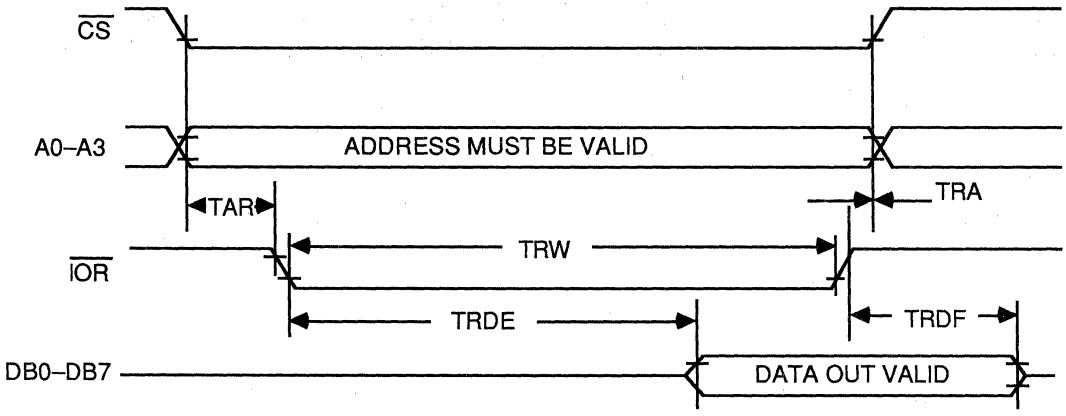


FIGURE 13. READY TIMING (SEE TABLE 5)

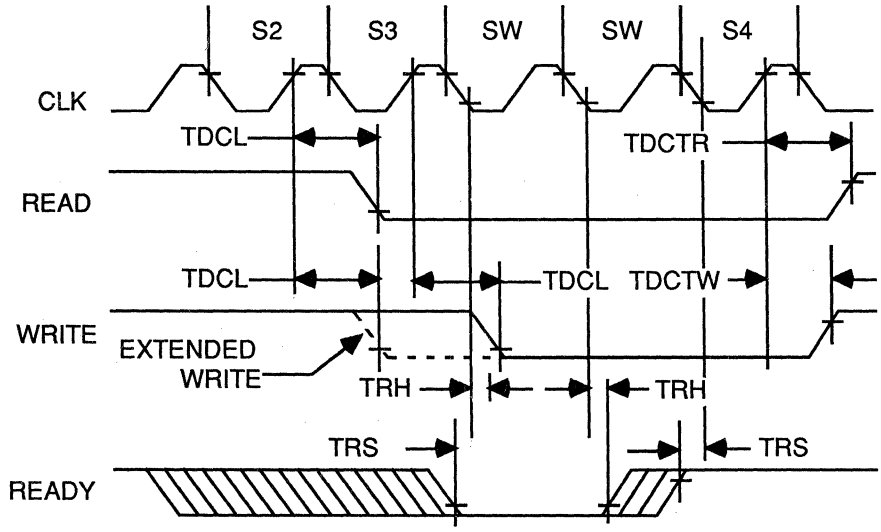


FIGURE 14. COMPRESSED TRANSFER TIMING (SEE TABLE 5)

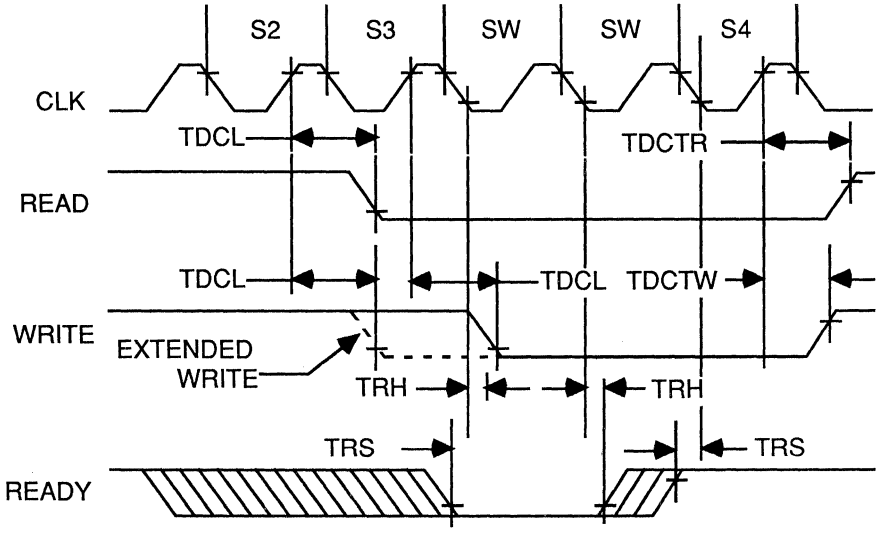
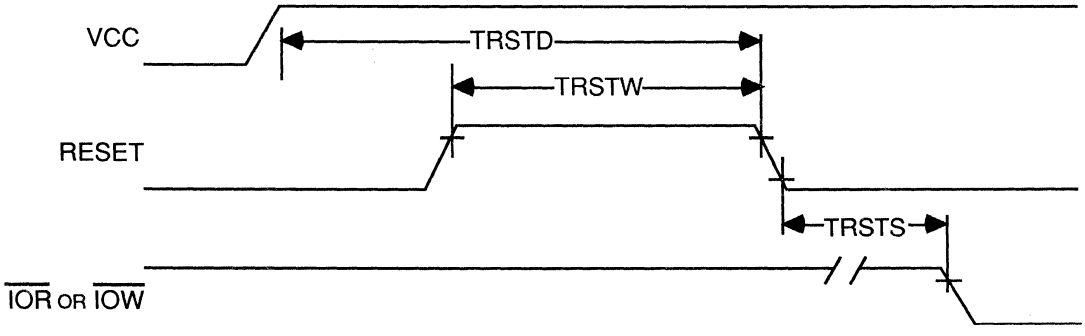


FIGURE 15. RESET TIMING (SEE TABLE 6)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.5 to 7.0 V
Input Voltage	-0.5 to 5.5 V
Output Voltage	-0.5 to 5.5 V
Operating Temperature	0 °C to +150°C
Storage Temperature	-65°C to +150°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ±5%

Symbol	Parameter	Min	Typ (1)	Max	Unit	Test Conditions
VOH	Output HIGH Voltage	2.4			V	IOH = –200 µA
		3.3			V	IOH = –100 µA (HRQ Only)
VOL	Output LOW Voltage			450	mV	IOL = 2.0 mA (data bus) $\overline{EOP}$ IOL = 3.2 mA (other outputs) (Note 8) IOL = 2.5 mA (ADSTB) (Note 8)
VIH	Input HIGH Voltage	2.2		VCC + 0.5	V	
VIL	Input LOW Voltage	–0.5		0.8	V	
ILI	Input Load Current			±10	µA	0 V ≤ VIN ≤ VCC
ILO	Output Leakage Current			±10	µA	0.45 V ≤ VOUT ≤ VCC
ICC	VCC Supply Current		110	130	mA/MHz	TA = +25°C
C0	Output Capacitance		4	8	pF	FC = 1.0 MHz, Inputs = 0 V
C1	Input Capacitance		8	15	pF	
C10	I/O Capacitance		10	18	pF	

AC and DC Characteristics Notes:

1. Typical values are for TA = 25°C, nominal supply voltage, and nominal processing parameters.
2. Input timing parameters assume transition times of 20 ns or less. Waveform measurement points for both input and output signals are 2.0 V for high and 0.8 V for low, unless otherwise noted.
3. Output loading is 1 TTL gate plus 150 pF capacitance, unless otherwise noted.
4. The net $\overline{IOW}$ or $\overline{MEMW}$ pulse width for normal write will be TCY-100 ns and for extended write will be 2TCY-100 ns. The net $\overline{IOR}$ or $\overline{MEMR}$ pulse width for normal read will be 2TCY-50 ns and for compressed read will be TCY-50 ns.
5. TDQ is specified for two different output high levels: TDQ1 is measured at 2.0 V, TDQ2 is measured at 3.3 V. The value for TDQ2 assumes an external 3.3 Kohm pull-up resistor connected from HRQ to VCC.
6. DREQ should be held active until DACK is returned.
7. DREQ and DACK signals may be active high or active low. Timing diagrams assume the active high mode.
8. Successive read and/or write operations, by the external processor, to program or examine the controller must be timed to allow at least 500 ns for the VL82C37A-04, at least 400 ns for the VL82C37A-05 and at least 250 ns for the VL82C37A-08, as recovery time between active read or write pulses.
9. $\overline{EOP}$ is an open-collector output. This parameter assumes the presence of a 2.2 Kohm pull-up resistor to VCC.
10. Pin 5 is an input that should always be at a logic high level. An internal pull-up resistor will establish a logic high when the pin is left floating. It is recommended, however, that pin 5 be tied to VCC.

VL82C54 PRODUCT BRIEF

PROGRAMMABLE INTERVAL TIMER

FEATURES

- Compatible 8080A, 8085A, 8086, 8088, and similiar microprocessors
- Counts in binary or BCD
- Clock inputs from dc to maximum clock operating frequency
- Status may be read back on command
- Single 5 V power supply
- Three independent 16-bit counters
- Six programmable counter modes
- Low power consuming CMOS technology

DESCRIPTION

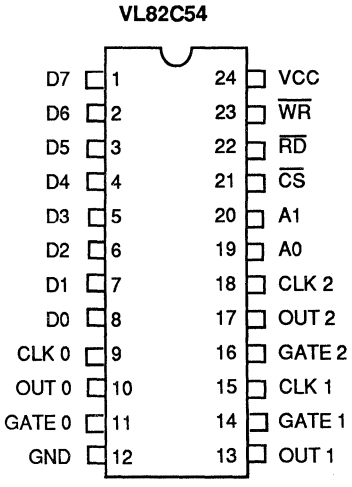
The VL82C54 is a CMOS programmable interval timer/counter designed for use with Intel-type microcomputer systems. It is a general-purpose, multi-timing element that can be considered as three separate counters by the system software.

The VL82C54 solves the problem of generating an accurate timing interval in the microprocessor-based system. Instead of setting up timing loops in software, the programmer configures the VL82C54 to generate the timing intervals required by the system. At the termination of the delay, the VL82C54 generates an interrupt to the CPU. The overhead software is minimal, and variable lengths are easily programmed.

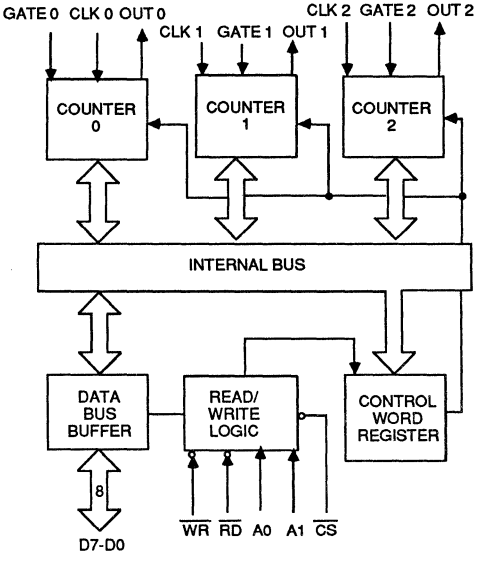
In addition to the three independent 16-bit counters on the VL82C54, it also has its own 8-bit data bus, two address lines, a chip select, and individual read and write control lines.

The VL82C54 is available in 8 MHz and 10 MHz maximum clock frequencies.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL82C54-08PC	8 MHz	Plastic DIP
VL82C54-08QC		Plastic Leaded Chip Carrier
VL82C54-08CC		Ceramic DIP
VL82C54-10PC	10 MHz	Plastic DIP
VL82C54-10QC		Plastic Leaded Chip Carrier
VL82C54-10CC		Ceramic DIP

Note: Operating temperature range: 0°C to +70°C.

VL82C59A PRODUCT BRIEF

PROGRAMMABLE INTERRUPT CONTROLLER

FEATURES

- Compatible with 8086, 8088, and similiar microprocessors
- Low power consuming CMOS
- Interrupt modes are programmable.
- Minimizes software overhead.
- Eight prioritized control levels
- 64 levels of expandability
- Single 5 V power supply
- 28-pin DIP

DESCRIPTION

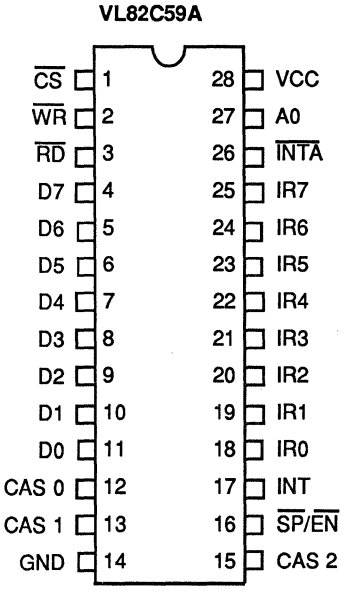
The VL82C59A Programmable Interrupt Controller can manage up to eight vectored priority interrupts for the system's CPU. It can be cascaded to handle up to 64 interrupts. No additional circuitry is required.

The VL82C59A is designed to relieve the software of the burden of handling multi-level priority interrupts. It controls several modes, permitting optimization for a large number of system needs.

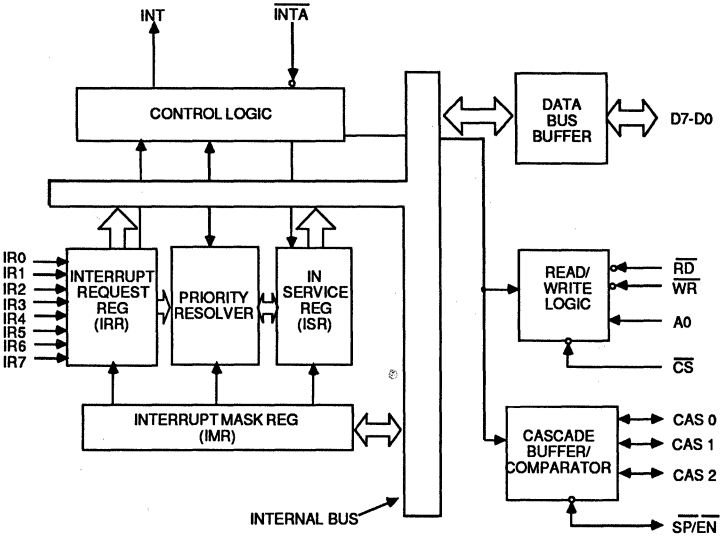
The VL82C59A is fully upward-compatible with the HMOS 8259 or 8259A. Software originally written for the HMOS 8259 or 8259A will operate the VL82C59A in all 8259- or 8259A- equivalent modes.

It is housed in a 28-pin DIP, uses CMOS technology, and requires a single 5 V supply. The circuit is totally static, requiring no clock input.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Bus Speed	Package
VL82C59A-08PC	8 MHz	Plastic DIP
VL82C59A-08QC		Plastic Leaded Chip Carrier
VL82C59A-08CC		Ceramic DIP
VL82C59A-10PC	10 MHz	Plastic DIP
VL82C59A-10QC		Plastic Leaded Chip Carrier
VL82C59A-10CC		Ceramic DIP

Note: Operating temperature range: 0°C to +70°C.

VL82C84A PRODUCT BRIEF

CLOCK GENERATOR AND DRIVER

FEATURES

- Two maximum clock frequencies available:
  - 8 MHz (VL82C84A-08)
  -10 MHz (VL82C84A-10)
- Local READY is provided, as well as Multibus® READY synchronization
- Schmitt-trigger input generates system RESET output
- Clock generator supports the 8086, 8088, and other similiar processors
- Capable of clock synchronization with other VL82C84A devices
- Crystal or TTL input may be used as a frequency source
- 100 mW maximum power dissipation

DESCRIPTION

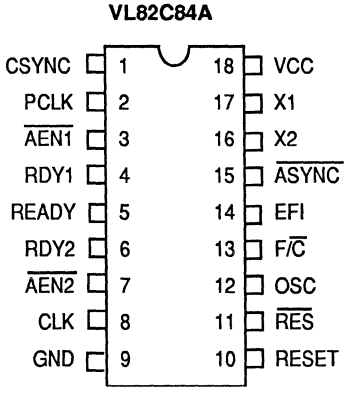
The VL82C84A is a single-chip clock generator/driver for the 8086, 8088, and similiar processors. The device contains a crystal-controlled oscillator and a divide-by-three counter, as well as complete synchronization and reset logic. Handling all of these functions on a singie device allows the VL82C84A to significantly reduce the chip count in a system, while enhancing reliability, production ease, and increasing mean time between failure (MTBF).

Fabricated in low-power CMOS, the VL82C84A provides a convenient way to decrease power consumption of the system. Fully compatible with existing designs using the NMOS 8284A, the VL82C84A provides a low-power cost-effective solution.

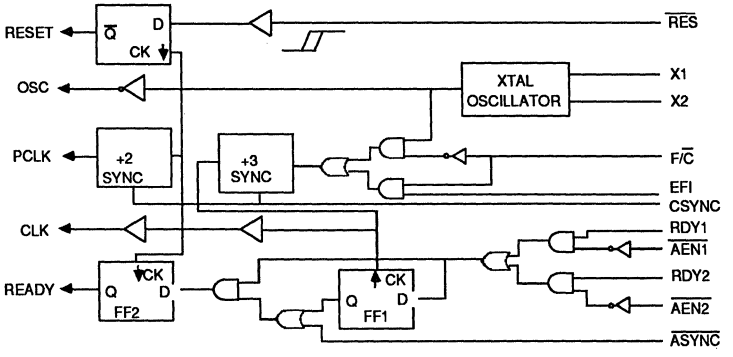
The output drivers of the VL82C84A offer the driving capability of the conventional HMOS device. As a result, they do not require any external drivers.

The VL82C84A is compatible with all the other members of the VL82CXX family of microprocessor peripherals. Offering higher performance and lower power consumption than previously available 82CXX peripherals, these devices offer CMOS advantages to 8086, 8088, and similiar systems.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL82C84A-08PC	8 MHz	Plastic DIP
VL82C84A-08QC		Plastic Leaded Chip Carrier
VL82C84A - 08CC		Ceramic DIP
VL82C84A-10PC	10 MHz	Plastic DIP
VL82C84A-10QC		Plastic Leaded Chip Carrier
VL82C84A-10CC		Ceramic DIP

Note: Operating temperature range: 0°C to +70°C.

Multibus® is a registered trademark of Intel Corporation.

VL82C88 PRODUCT BRIEF

CMOS BUS CONTROLLER

FEATURES

- Compatible with 8086, 8088 and similiar microprocessors
- Three-state command output drivers
- Low-power CMOS technology
- Fully compatible with HMOS 8288
- Advanced commands provided
- Wide flexibility in system configurations
- Can be used with an I/O bus
- Interface to up to two multi-master buses
- Single 5 V power supply

DESCRIPTION

The VL82C88 Bus Controller is a CMOS device intended for use with medium-to-large 8086- and 8088-type microprocessor-based systems. The bus controller provides command and control timing generation, as well as bus drive capability, for optimizing system performance. The VL82C88 decodes the three status lines from the system microprocessor to generate the command and control signals at the specified time.

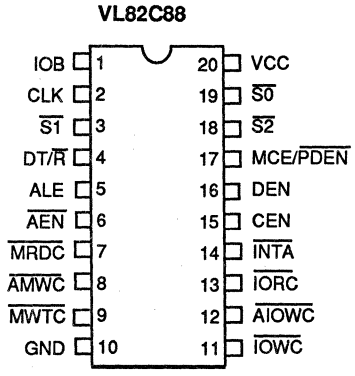
The VL82C88 bus controller generates commands in two ways:

I/O Bus Mode - The VL82C88 is in the I/O Bus mode if the IOB pin is tied HIGH. In the I/O Bus mode, all I/O command lines (IORC, IOWC, AIOWC, INTA) are always enabled.

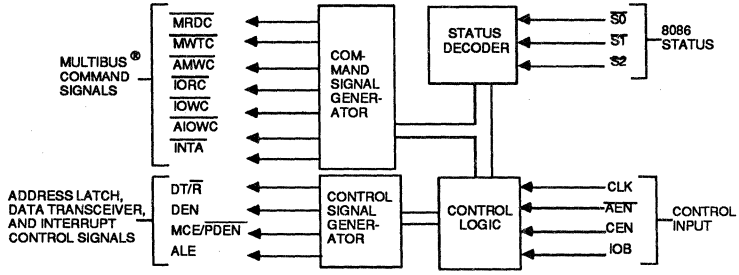
System Bus Mode - The VL82C88 is in the System Bus mode if the IOB pin is tied LOW. In this mode, no command is issued until 115 ns after the AEN Line is activated.

The 20-pin, low-power-consuming, CMOS VL82C88 is available in 8 MHz and 10 MHz clock frequencies.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL82C88-08PC	8 MHz	Plastic DIP
VL82C88-08QC		Plastic Leaded Chip Carrier
VL82C88-08CC		Ceramic DIP
VL82C88-10PC	10 MHz	Plastic DIP
VL82C88-10PC		Plastic Leaded Chip Carrier
VL82C88-10CC		Ceramic DIP

Note: Operating temperature range: 0° to +70°C.

Multibus® is a registered trademark of Intel Corp.

VL85C81 PRODUCT BRIEF

CMOS CLOCK GENERATOR AND CONTROLLER

FEATURES

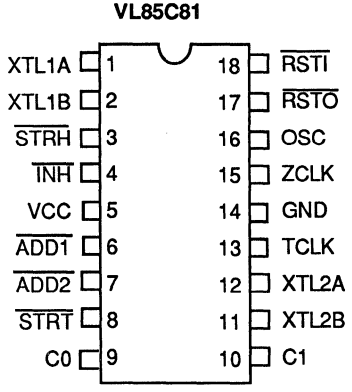
- Two independent 20 MHz oscillators generate two 10 MHz clock outputs and one 20 MHz clock output.
- Oscillator input frequency sources can be either crystals or external oscillators.
- Outputs directly drive the Z80, Z8000, 8086, 8088, and 68000 microprocessor clock inputs.
- Can be used as a general-purpose clock generator.
- Single 5 V power required
- Provides ability to stretch high and/or low phase of clock signa under external control.
- On-chip reset logic

DESCRIPTION

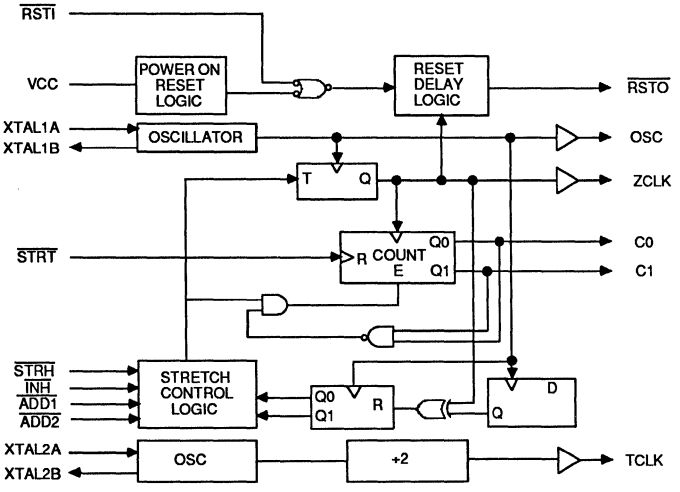
The VL85C81 Clock Generator and Controller is a versatile addition to VLSI's family of "instant ASIC" application-specific logic products. The selective clock-stretching capabilities and variety of timing outputs produced by this device allow it to easily meet the timing design requirements of systems with microprocessors and peripheral devices. The clock output drivers of the VL85C81 also meet the non-TTL voltage requirements for driving NMOS clock inputs with no additional external components. The VL85C81 provides an elegant, single-chip solution to the design of system clocks for microprocessor-based products. The VL85C81 oscillators are referenced to the system clock oscillator and the general-purpose clock oscillator. Both oscillators are driven by external crystals or other frequency sources.

A Reset output on the clock generator allows the VL85C81 system clock output to be synchronized with an incoming reset to the VL85C81. The external reset initiates the Reset output or system reset for a minimum of 30 ms, allowing a "power-up" system initialization.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL85C81-05PC	5 MHz	Plastic DIP
VL85C81-05QC		Plastic Leaded Chip Carrier
VL85C81-05CC		Ceramic DIP
VL85C81-08PC	8 MHz	Plastic DIP
VL85C81-08QC		Plastic Leaded Chip Carrier
VL85C81-08CC		Ceramic DIP

Note: Operating temperature range: 0°C to +70°C.

VLSI TECHNOLOGY, INC.

SECTION 5
DIGITAL SIGNAL PROCESSING PRODUCTS

Application Specific
Logic Products Division

VL2010

16 x 16 PARALLEL MULTIPLIER-ACCUMULATOR

FEATURES

- 16 X 16 parallel multiplication and product accumulation
- High speed
  Multiply-accumulate time:
  VL2010-65 50 ns typ 65 ns max
  VL2010-90 65 ns typ 90 ns max
- CMOS silicon-gate technology
- Low power; 0.2 W typical (VL2010-90)
- Single 5 V supply
- Standard TTL-compatible I/O levels
- Performs double-precision subtraction, addition, and multiplication, including rounding control
- Pin-for-pin functional replacement for WTL1010, WTL2010, TRW TDC1010J, LMA1010, and AMD 29510
- Available in 64-pin ceramic DIP, and soon to be available in plastic DIP, Plastic Leaded Chip Carrier, and Pin Grid Array

DESCRIPTION

The VL2010 is a 16 X 16 parallel multiplier-accumulator (MAC) fabricated using CMOS silicon-gate technology. The VL2010 offers ultra-low power and very high performance. The high performance is achieved through the use of the efficient Booth's algorithm and advanced VLSI processing technology.

The VL2010 operates from a single five volt supply and is compatible with standard TTL logic levels.The VL2010 is a pin-for-pin functional replacement for the WTL1010, WTL 2010, TRW TDC1010J or AMD 29510.

The VL2010, under control of the ACC input (see Block Diagram), performs either the multiply only, or the multiply-accumulate function. In either mode, input data X and Y can be specified as two's complement or unsigned magnitude. Input data representation is selectable via the input control line TC. In the multiply-only mode, extended product (XTP) data is sign-extended or set to zero for two's complement and unsigned-magnitude arithmetic, respectively. Additionally, a RND control is available for rounding up the most significant product (MSP) and extended product (XTP) data. In the multiply-accumulate mode, the double-precision accumulated answer is rounded back to single-precision or single-precision plus XTP bits.

The VL2010 architecture includes input and output data registers, as well as 3-state output data buses with independent, non-registered control. Time-multiplexing is used for the common Least Significant Product (LSP) and Input Data (Y) I/O lines. Input lines TSX, TSM, and TSL, respectively, control the outputs of the XTP, MSP, and LSP registers.

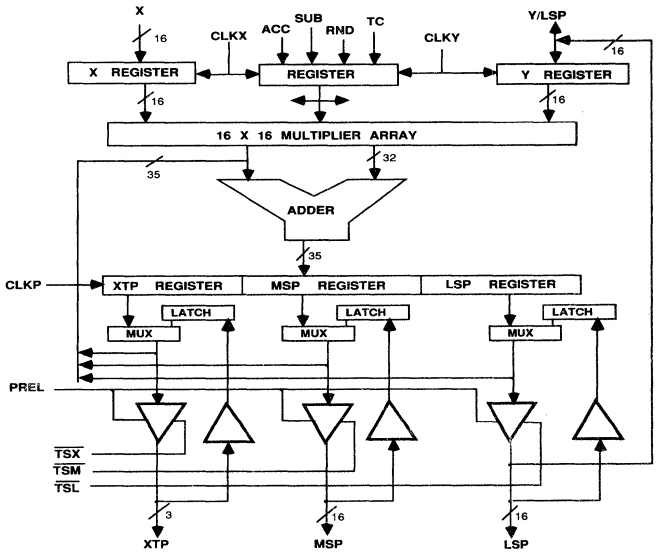
In the multiply-accumulate mode (ACC active), output data can be added to or subtracted from the last product. When SUB is also active, subtraction is performed. Otherwise, addition is performed.

The VL2010 can be efficiently applied in a variety of digital signal processing functions, including digital filtering (recursive, non-recursive, wave) and FFT processing (complex multiplication, butterfly computation). In addition, the VL2010 can be employed effectively in upgrading the computational capability of mini- and microcomputer systems.

ORDER INFORMATION

Part Number	Multiply/ Accumulate Time	Package
VL2010-65CC	65ns	Ceramic DIP
VL2010-65PC		Plastic DIP
VL2010-65QC		PLCC
VL2010-65GC		Pin Grid Array
VL2010-90CC	90ns	Ceramic DIP
VL2010-90PC		Plastic DIP
VL2010-90QC		PLCC
VL2010-90GC		Pin Grid Array

BLOCK DIAGRAM



PIN DESCRIPTIONS

X
Data Input
X is a 16-bit input. Data bits are loaded on the rising edge of CLKX.

Y/LSP
Data Input/
Data Output
These pins share functions between Y (16-bit data input) and LSP (least significant product output). Input data bits are loaded on the rising edge of CLKY. Output LSP data bits are available following the rising edge of CLKP.

MSP
Data Output
The 16-bit most-significant product output. MSP data is available following the rising edge of CLKP.

CLKX, CLKY
Input Clocks
These X and Y data input register clocks are active on their rising edges.

ACC
Accumulate
A HIGH level input permits the contents of the LSP, MSP, and XTP registers to be added to the multiplier output. A LOW level input allows multiplication only. The ACC signal is loaded on the rising edge of either CLKX or CLKY, and must be valid for the entire duration of input data.

SUB
Subtract
When ACC and SUB are both HIGH, the contents of the output register are subtracted from the last product generated, and the difference is stored back into the output registers at the rising edge of the next CLKP. When ACC is HIGH and SUB is LOW, addition instead of subtraction is performed. The SUB signal is loaded into the SUB register at the rising edge of either CLKX or CLKY.

The SUB signal must be valid over the same period that the input data is valid. When ACC is LOW, SUB is a "Don't Care" pin.

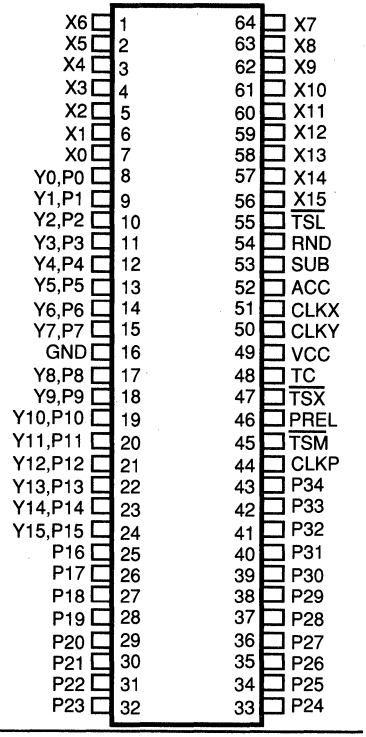
RND
Round
A HIGH-level input causes a "1" to be added to the most significant bit of the LSP to round up MSP and XTP data. RND is loaded on the rising edge of either CLKX or CLKY and must be valid for the duration of the input data.

TC
Two's Complement/ Unsigned Magnitude
A HIGH-level input defines X and Y as two's complement data, while a LOW level defines the input data as unsigned magnitude. As with ACC, SUB, and RND, TC is loaded at the rising edge of either CLKX or CLKY and must be valid for the duration of the input data.

$\overline{TSX}$,$\overline{TSM}$,$\overline{TSL}$
3-state Output Controls
The LSP, MSP, or XTP output buffers are at high-impedance (output disabled) when $\overline{TSL}$, $\overline{TSM}$, or $\overline{TSX}$, respectively, is HIGH. These are direct, nonregistered control signals. The output drivers are enabled when $\overline{TSL}$, $\overline{TSM}$, or $\overline{TSX}$ is LOW.

PIN DIAGRAM

VL2010
DIP



PRELOAD TRUTH TABLE

PREL	$\overline{TSX}$	$\overline{TSM}$	$\overline{TSL}$	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Hi-Z
0	0	1	0	Q	Hi-Z	Q
0	0	1	1	Q	Hi-Z	Hi-Z
0	1	0	0	Hi-Z	Q	Q
0	1	0	1	Hi-Z	Q	Hi-Z
0	1	1	0	Hi-Z	Hi-Z	Q
0	1	1	1	Hi-Z	Hi-Z	Hi-Z
1	0	0	0	Hi-Z	Hi-Z	Hi-Z
1	0	0	1	Hi-Z	Hi-Z	PL
1	0	1	0	Hi-Z	PL	Hi-Z
1	0	1	1	Hi-Z	PL	PL
1	1	0	0	PL	Hi-Z	Hi-Z
1	1	0	1	PL	Hi-Z	PL
1	1	1	0	PL	PL	Hi-Z
1	1	1	1	PL	PL	PL

Note:
Hi-Z = Output buffers at high impedance (Output disabled).
Q = Output buffers at low impedance. Contents of output registers will be transferred to output pins.
PL = Output buffers at high impedance, or output disabled. Preload data supplied externally will be loaded into the output register at the rising edge of CLKP.

DATA FORMATS

FRACTIONAL TWO'S COMPLEMENT

INPUT	X	BIT	15	14	13		3	2	1	0
		VALUE	SGN	2^{-1}	2^{-2}		2^{-12}	2^{-13}	2^{-14}	2^{-15}
	Y	BIT	15	14	13	12	3	2	1	0
		VALUE	SGN	2^{-1}	2^{-2}	2^{-3}	2	2^{-13}	2^{-14}	2^{-15}
OUTPUT	XTP	BIT	34	33	32					
		VALUE	-2^{4}	2^{3}	2^{2}					
	MSP	BIT	31	30	29		19	18	17	16
		VALUE	2^{1}	2^{0}	2^{-1}		2^{-11}	2^{-12}	2^{-13}	2^{-14}
	LSP	BIT	15	14	13		3	2	1	0
		VALUE	2^{-15}	2^{-16}	2^{-17}	2^{-18}	27	2^{-28}	2^{-29}	2^{-30}

Notes:

1. The value of the input sign bits is -2^{0}.
2. The format shown uses a two's complement fractional notation. Note that the location of the binary point signifying the separation of the integer and fractional fields is just after the sign, between the sign (-2^{0}) and and the next most significant bit for the multiplier inputs (-2^{1}). This scheme is carried over to the output format, except that an extended significance to the integer field is provided to extend the utility of the accumulator. Consistent with the input notation, the output binary point is located between the -2^{0} and the -2^{1} bit positions.

   The location of the binary point is arbitrary, as long as one is consistent with both input and output formats. One can consider the number field entirely integer, i.e., with the binary point just to the right of the least significant bit for input, product, and accumulated sum.
3. When nonaccumulating, all first four bits (P34 to P31) will indicate the sign of the product. The P30 term will also indicate the sign, except for the one exceptional case when multiplying -1 X -1. Note that, with the additional significant bits available on this multiplier, -1 X -1 is a valid operation yielding +1 product.
4. Whether accumulating the sum of products or doing single products, there is no change in format. However, the three additional most significant bits (the guard bits) are provided to allow valid summation beyond that available for a single multiplication product. For further clarification, no difference exists between this organization and one which would have the product accumul;ation off-chip in a separate 18-bit adder. Taking the sign at the ost siginificant bit position guarantees that the largest number field will be used. In operation, the sign will be extended into the lesser significant bit positions when the accumulated sum only occupies a right-hand portrion of the accumulator. As an example, when the sum only occupies the least three bit positions, then the sign will be extended through the 16 most significant positions.

INTEGER MAGNITUDE

INPUT	X	BIT	15	14	13		3	2	1	0
		VALUE	2^{15}	2^{14}	2^{13}		2^{3}	2^{2}	2^{1}	2^{0}
	Y	BIT	15	14	13	12	3	2	1	0
		VALUE	2^{15}	2^{14}	2^{13}	2^{12}		2^{2}	2^{1}	2^{0}
OUTPUT	XTP	BIT	34	33	32					
		VALUE	2^{34}	2^{33}	2^{32}					
	MSP	BIT	31	30	29		19	18	17	16
		VALUE	2^{31}	2^{30}	2^{29}		2^{19}	2^{18}	2^{17}	2^{16}
	LSP	BIT	15	14	13	12	3	2	1	0
		VALUE	2^{15}	2^{14}	2^{13}	2^{12}		2^{2}	2^{1}	2^{0}

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.5 to 7.0 V
Input Voltage	-0.5 to 7.0 V
Output Voltage	-0.5 to 7.0 V
Operating Temperature	0 °C to 70 °C
Storage Temperature	-65 °C to 150 °C
Lead Temperature (10 Sec.)	300 °C
Junction Temperature	175 °C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those listed on the operational sections of this specification is not implied and exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC CHARACTERISTICS TA = 0 °C to 70 °C, VCC = 5 V ± .25 V

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIH	HIGH-level Input Voltage	2.0			V	
VIL	LOW-Level Input Voltage			0.8	V	
VOH	HIGH-level Output Voltage		2.4	3.0	V	VCC = Min; IOH = -.04 mA
VOL	LOW-Level Output Voltage		0.3	0.4		VCC = Min; IOL = 4.0 mA
IIH	HIGH-level Input Current		10	75	µA	VCC = Max; VIH = 2.4V
IIL	LOW-Level Input Current		10	75	µA	VCC = Max; VIL = 0.4v
IOH	HIGH-level Output Current	-0.4			mA	
IOL	LOW-Level Output Current	4.0	8.0		mA	
ICC	Supply Current at DC		5	10	mA	VCC = Max; DC Cond.
ICC/F	Supply Current Increase/MHz		4	8	mA/ MHz	VCC = Max

CAPACITANCE TA = 0 °C to 70 °C

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
CI	Input Capacitance	Clocks, Unlatched Controls			20	pF	
		Data, Latched Controls			10		
CO	Output Capacitance			6	10	pF	

AC CHARACTERISTICS TA = 0 °C to 70 °C, VCC = 5 V ± .25 V

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
tD	Output Delay	VL2010-90		25	35	ns	Load 1 (Figure 3)
		VL2010-65		20	30		
tENA	Output Enable Delay			30	35	ns	Load 2 (Figure 4)
tDIS	Output Disable Delay			25	30		
tMA	Multiply-Accumulate Time	VL2010-90		65	90	ns	
		VL2010-65		50	65		
tPW	Clock Pulse Width		25			ns	
tS	Input Register Setup Time		25			ns	
tH	Input Register Hold Time		0			ns	

TIMING DIAGRAM

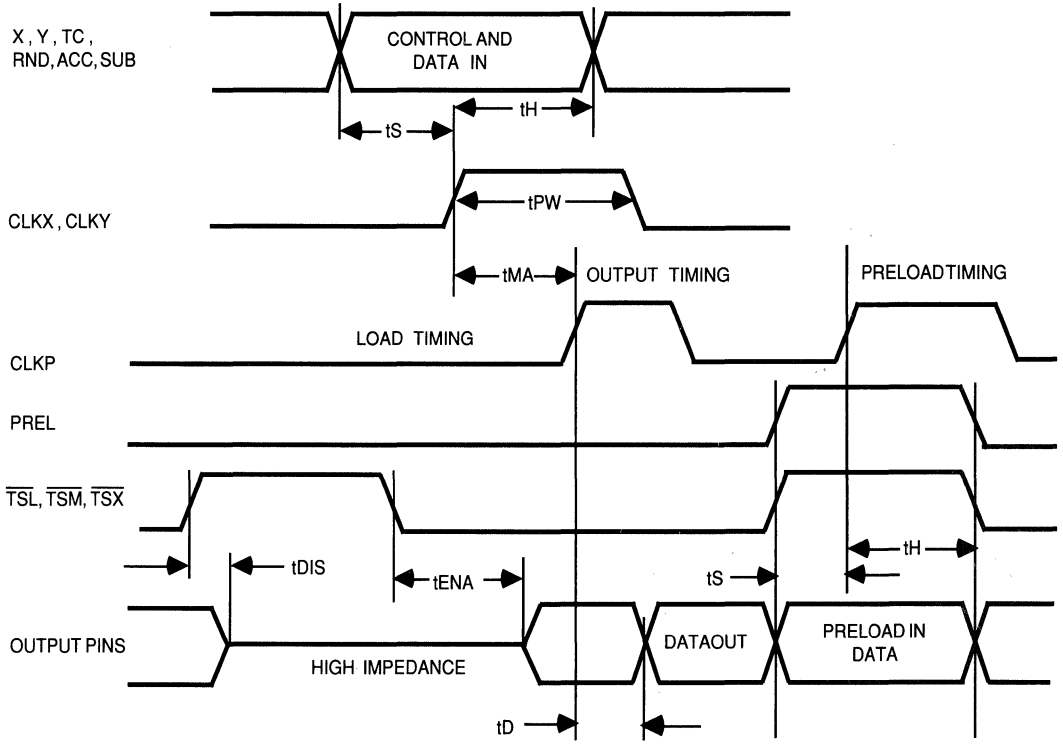


FIGURE 1. INPUT EQUIVALENT CIRCUIT

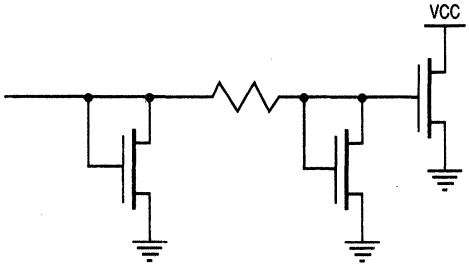


FIGURE 2. OUTPUT CIRCUIT

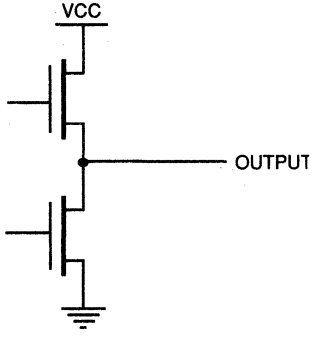


FIGURE 3. TEST LOAD FOR DELAY MEASUREMENT

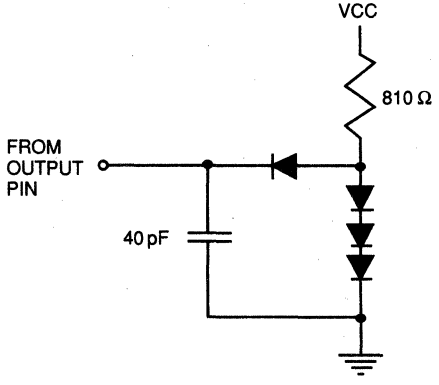


FIGURE 4. TEST LOAD FOR 3-STATE DELAY

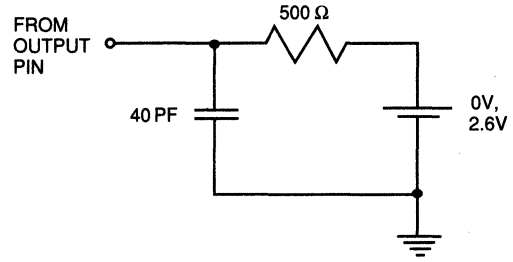


FIGURE 5. SUPPLY CURRENT VS OPERATING FREQUENCY

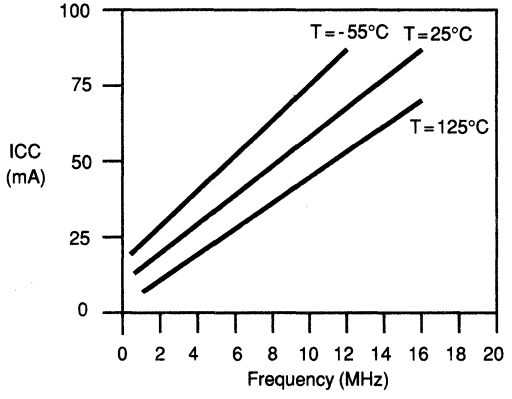
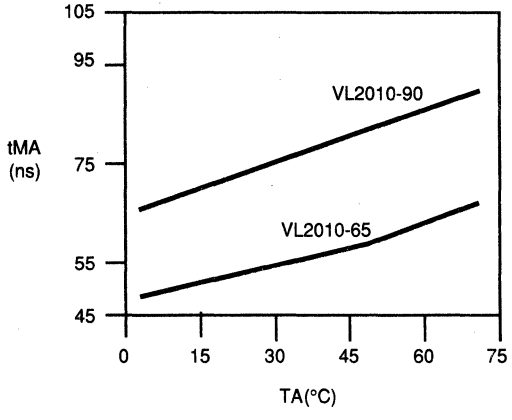


FIGURE 6. MULTIPLY-ACCUMULATE TIME VS AMBIENT TEMPERATURE



VL2044

16 x 16 PARALLEL MULTIPLIER-ACCUMULATOR

FEATURES

- 16 X 16 parallel multiplication and product accumulation
- High speed
  Multiply-accumulate time:
  VL2044-65 50 ns typ 65 ns max
  VL2044-90 65 ns typ 90 ns max
- CMOS silicon-gate technology
- Low power; 0.2 W typical (VL2044-90)
- Single 5 V supply
- Standard TTL-compatible I/O levels
- Performs double-precision subtraction, addition, and multiplication, including rounding control
- With the exception of preload function, pin-for-pin functional replacement for WTL1010, WTL2010, TRW TDC1010J, LMA1010, and AMD 29510
- Available in 64-pin ceramic DIP, and soon to be available in plastic DIP, Plastic Leaded Chip Carrier, and Pin Grid Array
- Pin-for-pin replacement for WTL2044

DESCRIPTION

The VL2044 is a 16 X 16 parallel multiplier-accumulator (MAC) fabricated using CMOS silicon-gate technology. The VL2044 offers ultralow power and very high performance. The high performance is achieved through the use of the efficient Booth's algorithm and advanced VLSI processing technology.

The VL2044 operates from a single five volt supply and is compatible with standard TTL logic levels. Except for the preload function, the VL2044 is a pin-for-pin functional replacement for the WTL1010, WTL 2010, TRW TDC1010J or AMD 29510.

The VL2044, under control of the ACC input (see Block Diagram), performs either the multiply only, or the multiply-accumulate function. In either mode, input data X and Y can be specified as two's complement or unsigned magnitude. Input data representation is selectable via the input control line TC. In the multiply-only mode, extended product (XTP) data is sign-extended or set to zero for two's complement and unsigned-magnitude arithmetic, respectively. Additionally, a RND control is available for rounding up the most significant product (MSP) and extended product (XTP) data. In the multiply-accumulate mode, the double-precision accumulated answer is rounded back to single-precision or single-precision plus XTP bits.

The VL2044 architecture includes input and output data registers, as well as 3-state output data buses with independent, non-registered control. Time-multiplexing is used for the common Least Significant Product (LSP) and Input Data (Y) I/O lines. Input lines $\overline{TSX}$, $\overline{TSM}$, and $\overline{TSL}$, respectively, control the outputs of the XTP, MSP, and LSP registers.

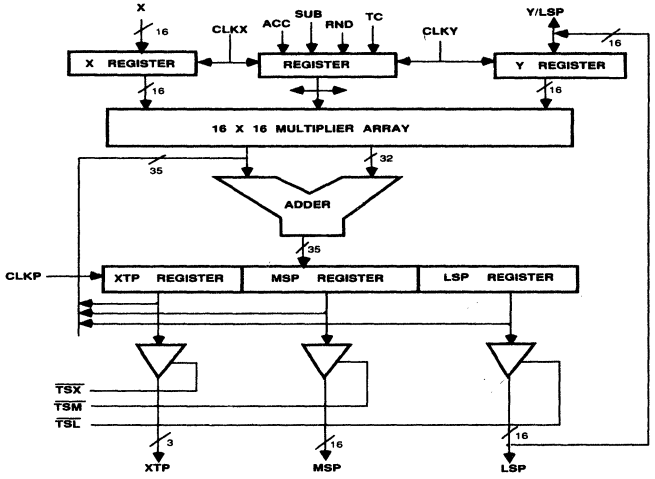
In the multiply-accumulate mode (ACC active), output data can be added to or subtracted from the last product. When SUB is also active, subtraction is performed. Otherwise, addition is performed.

The VL2044 can be efficiently applied in a variety of digital signal processing functions, including digital filtering (recursive, non-recursive, wave) and FFT processing (complex multiplication, butterfly computation). In addition, the VL2044 can be employed effectively in upgrading the computational capability of mini- and microcomputer systems.

ORDER INFORMATION

Part Number	Multiply/ Accumulate Time	Package
VL2044-65CC	65 ns	Ceramic DIP
VL2044-65PC		Plastic DIP
VL2044-65QC		PLCC
VL2044-65GC		Pin Grid Array
VL2044-90CC	90 ns	Ceramic DIP
VL2044-90PC		Plastic Dip
VL2044-90QC		PLCC
VL2044-90GC		Pin Grid Array

BLOCK DIAGRAM



SIGNAL DESCRIPTIONS

X
Data Input
X is a 16-bit input. Data bits are loaded on the rising edge of CLKX.

Y/LSP
Data Input/
Data Output
These pins share functions between Y (16-bit data input) and LSP (least significant product output). Input data bits are loaded on the rising edge of CLKY. Output LSP data bits are available following the rising edge of CLKP.

MSP
Data Output
The 16-bit most-significant product output. MSP data is available following the rising edge of CLKP.

CLKX, CLKY
Input Clocks
These X and Y data input register clocks are active on their rising edges.

ACC
Accumulate
A HIGH level input permits the contents of the LSP, MSP, and XTP registers to be added to the multiplier output. A LOW level input allows multiplication only. The ACC signal is loaded on the rising edge of either CLKX or CLKY, and must be valid for the entire duration of input data.

SUB
Subtract
When ACC and SUB are both HIGH, the contents of the output register are subtracted from the last product generated, and the difference is stored back into the output registers at the rising edge of the next CLKP. When ACC is HIGH and SUB is LOW, addition instead of subtraction is performed. The SUB signal is loaded into the SUB register at the rising edge of either CLKX or CLKY.

The SUB signal must be valid over the same period that the input data is valid. When ACC is LOW, SUB is a "Don't Care" pin.

RND
Round
A HIGH-level input causes a "1" to be added to the most significant bit of the LSP to round up MSP and XTP data. RND is loaded on the rising edge of either CLKX or CLKY and must be valid for the duration of the input data.

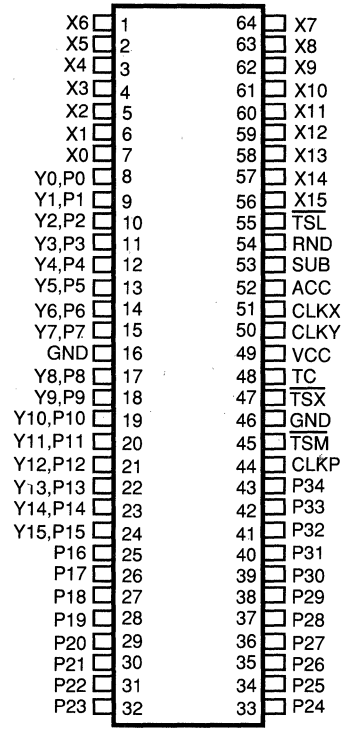
TC
Two's Complement/ Unsigned Magnitude
A HIGH-level input defines X and Y as two's complement data, while a LOW level defines the input data as unsigned magnitude. As with ACC, SUB, and RND, TC is loaded at the rising edge of either CLKX or CLKY and must be valid for the duration of the input data.

$\overline{TSX}$,$\overline{TSM}$,$\overline{TSL}$
3-state Output Controls
The LSP, MSP, or XTP output buffers are at high-impedance (output disabled) when $\overline{TSL}$, $\overline{TSM}$, or $\overline{TSX}$, respectively, is HIGH. These are direct, nonregistered control signals. The output drivers are enabled when $\overline{TSL}$, $\overline{TSM}$, or $\overline{TSX}$ is LOW.

CLKP
Output Clock
The output registers are loaded following the rising edge of CLKP. This rising edge may occur after or before the falling edges of $\overline{TSL}$, $\overline{TSM}$, or $\overline{TSX}$.

PIN CONFIGURATION

VL2044
DIP



DATA FORMATS

FRACTIONAL TWO'S COMPLEMENT

INPUT	X	BIT	15	14	13		3	2	1	0
		VALUE	SGN	2^{-1}	2^{-2}	2	2^{-12}	2^{-13}	2^{-14}	2^{-15}
	Y	BIT	15	14	13	12	3	2	1	0
		VALUE	SGN	2^{-1}	2^{-2}	2^{-3}	12	2^{-13}	2^{-14}	2^{-15}
OUTPUT	XTP	BIT	34	33	32					
		VALUE	-2^{4}	2^{3}	2^{2}					
	MSP	BIT	31	30	29		19	18	17	16
		VALUE	2^{1}	2^{0}	2^{-1}		2^{-11}	2^{-12}	2^{-13}	2^{-14}
	LSP	BIT	15	14	13	1	3	2	1	0
		VALUE	2^{-15}	2^{-16}	2^{-17}	2^{-18}	27	2^{-28}	2^{-29}	2^{-30}

Notes:

1. The value of the input sign bits is -2^{0}.
2. The format shown uses a two's complement fractional notation. Note that the location of the binary point signifying the separation of the integer and fractional fields is just after the sign, between the sign (-2^{0}) and and the next most significant bit for the multiplier inputs (-2^{1}). This scheme is carried over to the output format, except that an extended significance to the integer field is provided to extend the utility of the accumulator. Consistent with the input notation, the output binary point is located between the -2^{0} and the -2^{1} bit positions.

   The location of the binary point is arbitrary, as long as one is consistent with both input and output formats. One can consider the number field entirely integer, i.e., with the binary point just to the right of the least significant bit for input, product, and accumulated sum.
3. When nonaccumulating, all first four bits (P34 to P31) will indicate the sign of the product. The P30 term will also indicate the sign, except for the one exceptional case when multiplying -1 X -1. Note that, with the additional significant bits available on this multiplier, -1 X -1 is a valid operation yielding +1 product.
4. Whether accumulating the sum of products or doing single products, there is no change in format. However, the three additional most significant bits (the guard bits) are provided to allow valid summation beyond that available for a single multiplication product. For further clarification, no difference exists between this organization and one which would have the product accumulation off-chip in a separate 18-bit adder. Taking the sign at the most siginificant bit position guarantees that the largest number field will be used. In operation, the sign will be extended into the lesser significant bit positions when the accumulated sum only occupies a right-hand portion of the accumulator. As an example, when the sum only occupies the least three bit positions, then the sign will be extended through the 16 most significant positions.

INTEGER MAGNITUDE

INPUT	X	BIT	15	14	13		3	2	1	0
		VALUE	2^{15}	2^{14}	2^{13}	2	2^{3}	2^{2}	2^{1}	2^{0}
	Y	BIT	15	14	13	12	3	2	1	0
		VALUE	2^{15}	2^{14}	2^{13}	2^{12}		2^{2}	2^{1}	2^{0}
OUTPUT	XTP	BIT	34	33	32					
		VALUE	2^{34}	2^{33}	2^{32}					
	MSP	BIT	31	30	29		19	18	17	16
		VALUE	2^{31}	2^{30}	2^{29}		2^{19}	2^{18}	2^{17}	2^{16}
	LSP	BIT	15	14	13	12	3	2	1	0
		VALUE	2^{15}	2^{14}	2^{13}	2^{12}		2^{2}	2^{1}	2^{0}

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.5 to 7.0 V
Input Voltage	-0.5 to 5.5 V
Output Voltage	-0.5 to 5.5 V
Operating Temperature	0 °C to 70 °C
Storage Temperature	-65 °C to 150 °C
Lead Temperature (10 Sec.)	300 °C
Junction Temperature	175 °C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those listed on the operational sections of this specification is not implied and exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC CHARACTERISTICS TA = 0 °C to 70 °C, VCC = 5 V ± .25 V

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIH	HIGH-level Input Voltage	2.0			V	
VIL	LOW-Level Input Voltage			0.8	V	
VOH	HIGH-level Output Voltage	2.4	3.0		V	VCC = Min; IOH = -0.4A
VOL	LOW-Level Output Voltage		0.3	0.4	V	VCC = Min; IOL = 4.0 mA
IIH	HIGH-level Input Current		10	75	µA	VCC Max; VIH = 2.4 V
IIL	LOW-Level Input Current		10	75	µA	VCC = Max; VIL = 0.4 V
IOH	HIGH-level Output Current		-0.4	-3.3	mA	VCC = Min; VOH = 2
IOL	LOW-Level Output Current	4.0	8.0		mA	VCC = Min; VOL = 0.4 V
ICC	Supply Current at DC		5	10	mA	VCC = Max; DC Cond
ICC/F	Supply Current Increase/MHz		4	8	mA/ MHz	VCC = Max

CAPACITANCE TA = 0 °C to 70 °C (Note 1)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
CI	Input Capacitance	Clocks, Unlatched Controls			20	pF	
		Data, Latched Controls			10		
CO	Output Capacitance			6	10	pF	

Note: 1. The specifications for capacitance (input and output) are guaranteed by design, but not tested.

AC CHARACTERISTICS TA = 0 °C to 70 °C, VCC = 5 V ± .25 V

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
tD	Output Delay	VL2044-90		25	35	ns	Load 1 (Figure 3)
		VL2044-65		20	30		
tENA	Output Enable Delay			30	35	ns	Load 2 (Figure 4)
tDIS	Output Disable Delay			25	30		
tMA	Multiply-Accumulate Time	VL2044-90		65	90	ns	
		VL2044-65		50	65		
tPW	Clock Pulse Width		25			ns	
tS	Input Register Setup Time		25			ns	
tH	Input Register Hold Time		0			ns	

TIMING DIAGRAM

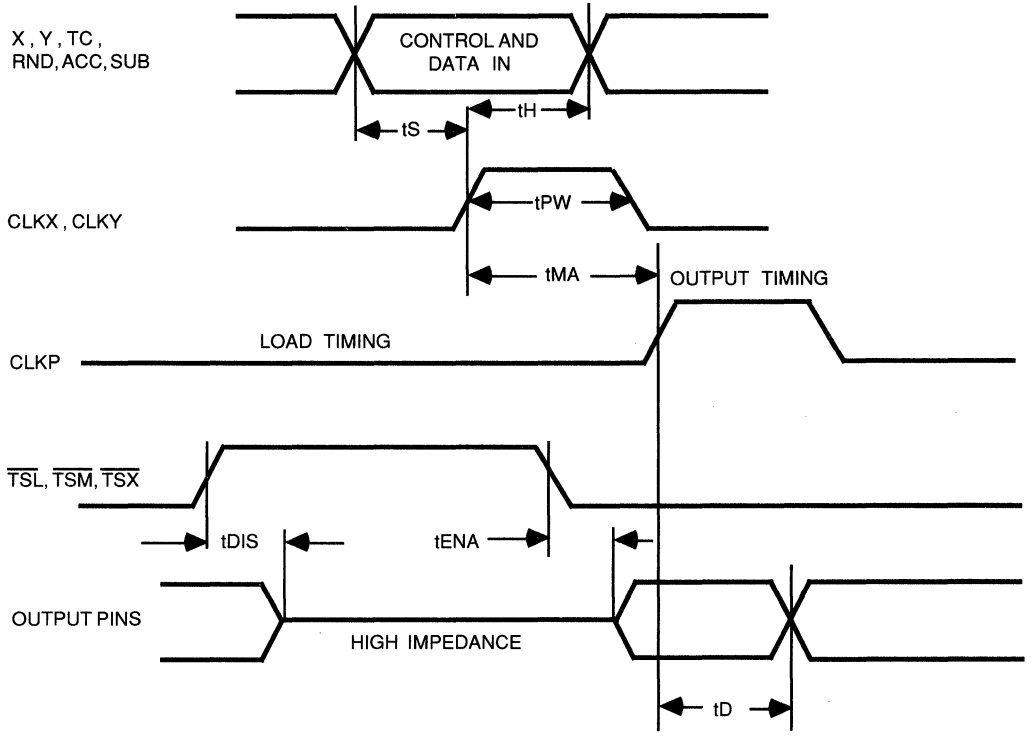


FIGURE 1. INPUT EQUIVALENT CIRCUIT

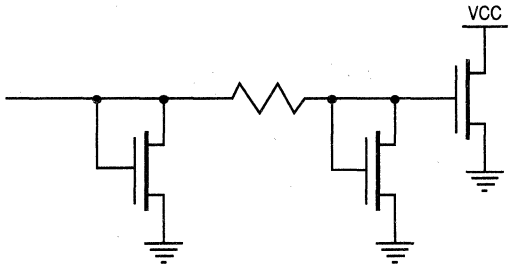


FIGURE 2. OUTPUT CIRCUIT

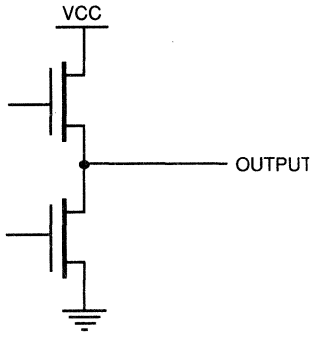


FIGURE 3. TEST LOAD FOR DELAY MEASUREMENT

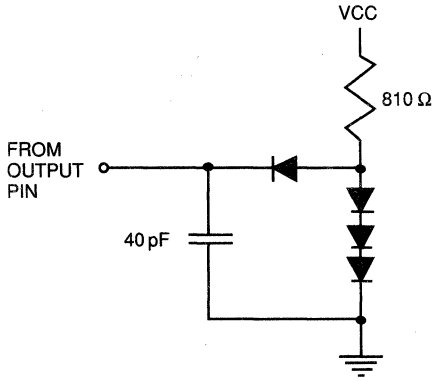


FIGURE 4. TEST LOAD FOR 3-STATE DELAY

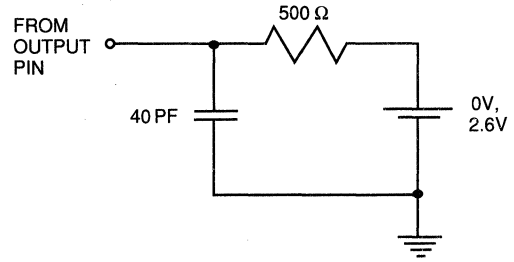


FIGURE 5. SUPPLY CURRENT VS OPERATING FREQUENCY

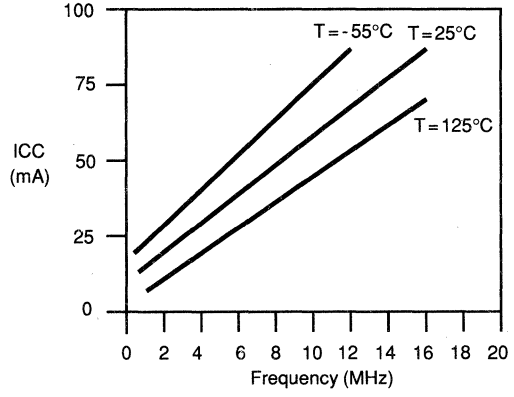
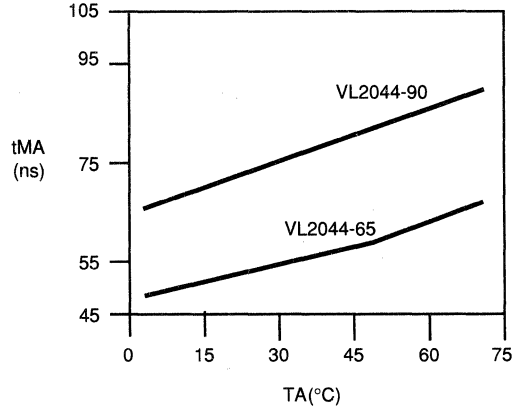


FIGURE 6. MULTIPLY-ACCUMULATE TIME VS AMBIENT TEMPERATURE



VLSI TECHNOLOGY, INC.

SECTION 6
DATA COMMUNICATIONS PRODUCTS

Application Specific
Logic Products Division

VL16C450 • VL82C50A • VL82C50

ASYNCHRONOUS COMMUNICATIONS ELEMENT

FEATURES

- Full double buffering
- Independent control of transmit, receive, line status and data set interrupts
- Modem control signals include $\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$ and $\overline{DCD}$.
- Programmable serial interface characteristics:
  - —5-,6-,7- or 8-bit characters
  - —Even-, odd- or no-parity bit generation and detection
  - —1-, 1½- or 2-stop bit generation
  - —Baud rate generation (dc to 56K baud)
- Full status reporting capabilities
- 3-state TTL drive capabilities for bidirectional data bus and control bus

DESCRIPTION

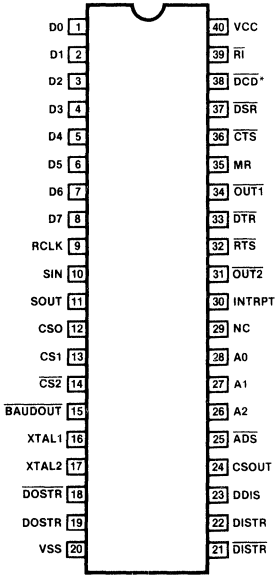
The VL16C450 is an asynchronous communications element (ACE) that is functionally equivalent to the VL82C50A, but is an improved-specification version of that part. The improved specifications provide ensured compatibility with state-of-the-art CPUs.

The VL16C450, VL82C50A, and VL82C50 ACEs serve as serial data input/output interfaces in microcomputer systems. They perform serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of the ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed, and error conditions involving parity, overrun, framing or break interrupt.

A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and (2^{16}-1).

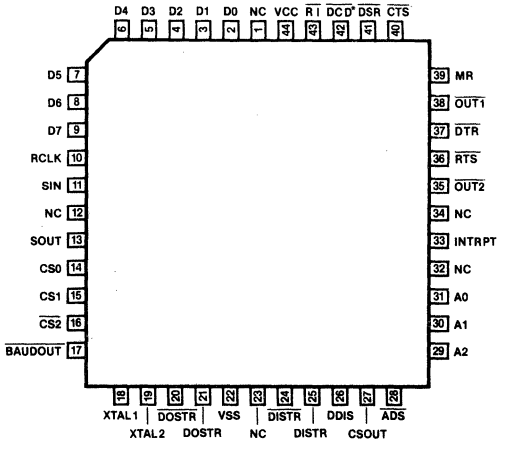
PIN DIAGRAMS

VL16C450
VL82C50A
VL82C50



*ON THE VL82C50, PIN 38 (PIN 42 ON THE PLCC PACKAGE) IS ALSO CALLED $\overline{RLSD}$

VL16C450
VL82C50A
VL82C50

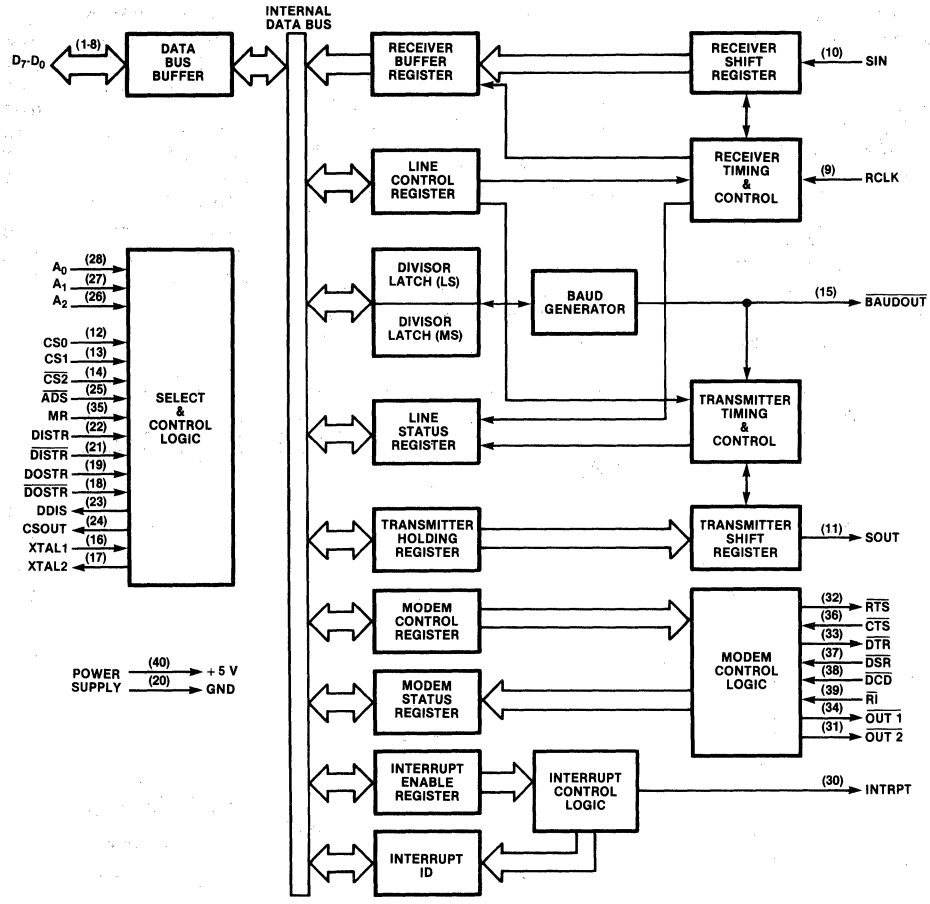


ORDER INFORMATION

Part Number	Maximum External Clock Frequency	Package
VL16C450-PC	3.1 MHz	Plastic DIP
VL16C450-CC		Ceramic DIP
VL16C450-QC		Plastic Leaded Chip Carrier (PLCC)
VL82C50A-PC	3.1 MHz	Plastic DIP
VL82C50A-CC		Ceramic DIP
VL82C50A-QC		Plastic Leaded Chip Carrier (PLCC)
VL82C50-PC	3.1 MHz	Plastic DIP
VL82C50-CC		Ceramic DIP
VL82C50-QC		Plastic Leaded Chip Carrier (PLCC)

Note:
Operating temperature range: 0°C to +70°C.

BLOCK DIAGRAM



NOTE:
APPLICABLE PIN NUMBERS ARE INCLUDED WITHIN PARENTHESES

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on any I/O pin with Respect to Ground	−0.5 V to +7.0 V
Power Dissipation	700 mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ± 5%, VSS = 0 V, unless otherwise specified

		VL16C450		VL82C50A		VL82C50			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units	Conditions
VILX	Clock input LOW Voltage	−0.5	0.8	−0.5	0.8	−0.5	0.8	V	
VIHX	Clock input HIGH Voltage	2.0	VCC	2.0	VCC	2.0	VCC	V	
VIL	Input LOW Voltage	−0.5	0.8	−0.5	0.8	−0.5	0.8	V	
VIH	Input HIGH Voltage	2.0	VCC	2.0	VCC	2.0	VCC	V	
VOL	Output LOW Voltage		0.4		0.4		0.4	V	IOL = 1.6 mA on all Note 1
VOH	Output HIGH Voltage	2.4		2.4		2.4		V	IOH = −1.0 mA Note 1
ICC (Average)	Average Power Supply Current (VCC)		20		20		20	mA	VCC = 5.25 V, No loads on SIN, DSR, RLSD, CTS, DCD. RI = 2.0 V. All other inputs = 0.8 V. Baud rate generator at 4 MHz. Baud rate at 56K.
IIL	Input Leakage		±10		±10		±10	µA	VCC = 5.25 V, VSS = 0 V. All other pins floating.
ICL	Clock Leakage		±10		±10		±10	µA	VIN = 0 V, 5.25 V
IOZ	3-state Leakage		±20		±20		±20	µA	VCC = 5.25 V, VSS = 0 V. VOUT = 0 V, 5.25 V 1) Chip deselected 2) Chip and write mode selected
VILMR	MR Schmitt VIL		0.8		0.8		N/A	V	
VIHMR	MR Schmitt VIH	2.0		2.0		N/A		V	

CAPACITANCE TA = 25°C, f = 1.0 MHz, VCC = VSS = 0 V

Symbol	Parameter	Min	Typ	Max	Units	Conditions
CXTAL2	Clock Input Capacitance		15	20	pF	fc = 1 MHz Unmeasured pins returned to VSS
CXTAL1	Clock Output Capacitance		20	30	pF	
CI	Input Capacitance		6	10	pF	
CO	Output Capacitance		10	20	pF	

AC CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5 V ±5%, Note 5

		VL16C450		VL82C50A		VL82C50				
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
tAW	Address Strobe Width	60		90		90			ns	
tAS	Address Setup Time	60		90		110			ns	
tAH	Address Hold Time	0		0		0			ns	
tCS	Chip Select Setup Time	60		90		110			ns	
tCH	Chip Select Hold Time	0		0		0			ns	
tCSS	Chip Select Output Delay From $\overline{ADS}$							90	ns	
tDID	$\overline{DISTR}$/DISTR Delay From $\overline{ADS}$					0			ns	
tDIW	$\overline{DISTR}$/DISTR Strobe Width	125		175		175			ns	
tRC	Ready Cycle Delay	175		500		1735			ns	
RC	Ready Cycle = tAR(1) + tDIW + tRC	360		755		2000			ns	
tDD	$\overline{DISTR}$/DISTR to Driver Disable Delay		60		75			150	ns	100 pF load, Note 4
tDDD	Delay from $\overline{DISTR}$/DISTR to Data		125		175			250	ns	100 pF load
tHZ	$\overline{DISTR}$/DISTR to Floating Data Delay	0	100	100		100			ns	100 pF load, Note 4
tDOD	$\overline{DOSTR}$/DOSTR delay from ADS					50			ns	
tDOW	$\overline{DOSTR}$/DOSTR Strobe Width	100		175		175			ns	
tWC	Write Cycle Delay	200		500		1785			ns	
WC	Write Cycle = tAW* + tDOW + tWC	360		755		2100			ns	
tDS	Data Setup Time	40		90		175			ns	
tDH	Data Hold Time	40		60		60			ns	
tCSC*	Chip Select Output Delay from Select		100		125			200	ns	100 pF load
tRA*	Address Hold Time from $\overline{DISTR}$/DISTR	20		20		50			ns	Note 2
tRCS*	Chip Select Hold Time from $\overline{DISTR}$/DISTR	20		20		50			ns	Note 2
tAR*	$\overline{DISTR}$/DISTR Delay from Address	60		80		110			ns	Note 2
tCSR*	$\overline{DISTR}$/DISTR Delay from Chip Select	50		80		110			ns	Note 2
tWA*	Address Hold Time from $\overline{DOSTR}$/DOSTR	20		20		50			ns	Note 2
tWCS*	Chip Select Hold Time from $\overline{DOSTR}$/DOSTR	20		20		50			ns	Note 2
tAW*	$\overline{DOSTR}$/DOSTR Delay from Address	60		80		160			ns	Note 2
tCSW*	$\overline{DOSTR}$/DOSTR Delay from Select	50		80		160			ns	Note 2
tMRW	Master Reset Pulse Width	5		10		25			µs	
tXH	Duration of Clock HIGH Pulse	140		140		140			ns	
tXL	Duration of Clock LOW Pulse	140		140		140			ns	External Clock (3.1 MHz Max.)

AC CHARACTERISTICS (Cont.) TA = 0°C to +70°C, VCC = 5 V ±5%

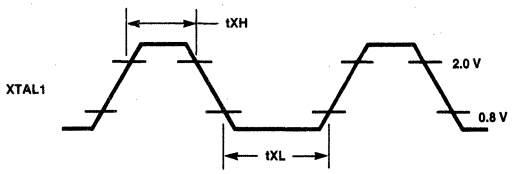
Symbol	Parameter	VL16C450 Min	VL16C450 Max	VL82C50A Min	VL82C50A Max	VL82C50 Min	VL82C50 Typ	VL82C50 Max	Units	Conditions
Transmitter										
tHR1	Delay from rising edge of DOSTR/DOSTR (WR THR) to Reset Interrupt		175		1000			N/A	ns	100 pF load
tHR2	Delay from falling edge of DOSTR/DOSTR (WR THR) to reset interrupt		n/a		n/a		1000		ns	100 pF load
tIRS	Delay from Initial INTR Reset to Transmit Start	8	24	8	24		16		RCLK Cycles	Note 3
tSI	Delay from initial Write to Interrupt	16	32	16	32		24		RCLK Cycles	Note 3
tSS	Delay from Stop to Next Start						1000		ns	
tSTI	Delay from Stop to Interrupt (THRE)	8	8	8	8		8		RCLK Cycles	Note 3
tIR	Delay from DISTR/DISTR (RD IIR) to Reset Interrupt (THRE)		250		1000		1000		ns	100 pF load
Modem Control										
tMDO	Delay from DOSTR/DOSTR (WR MCR) to Output		200		1000		1000		ns	100 pF load
tSIM	Delay to Set Interrupt from MODEM Input				1000		1000		ns	100 pF load
tRIM	Delay to Reset Interrupt from DISTR/DISTR (RS MSR)		250		1000		1000		ns	100 pF load
Baud Generator										
N	Baud Divisor	1	2^{16}-1	1	2^{16}-1	1	2^{16}-1			
tBLD	Baud Output Negative Edge Delay		125		250		250		ns	100 pF load
tBHD	Baud Output Positive Edge Delay		125		250		250		ns	100 pF load
tLW	Baud Output Down Time	425		425		425			ns	fX = 2 MHz, ÷2, 100 pF load
tHW	Baud Output Up Time	330		330		330			ns	fX = 3 MHz, ÷3, 100 pF load
Receiver										
tSCD	Delay from RCLK to Sample Time		2		2		2		µs	
tSINT	Delay from Stop to Set Interrupt	1	1	1	1		2		RCLK Cycles	Note 3
tRINT	Delay from DISTR/DISTR (RD RBR/RDLSR) to Reset Interrupt		1		1		1		µs	100 pF load

Notes:

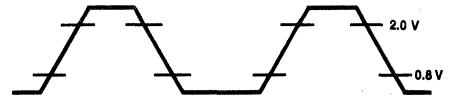
1. Does not apply to XTAL2.
2. Applicable only when ADS is tied LOW.
3. RCLK = tXH and tXL.
4. Charge and discharge time is determined by VOL, VOH and the external loading.
5. All timings are referenced to valid 0 and valid 1 (see AC TEST POINTS).

AC TESTING INPUT/OUTPUT WAVE FORM

EXTERNAL CLOCK INPUT (3.1 MHz MAXIMUM)

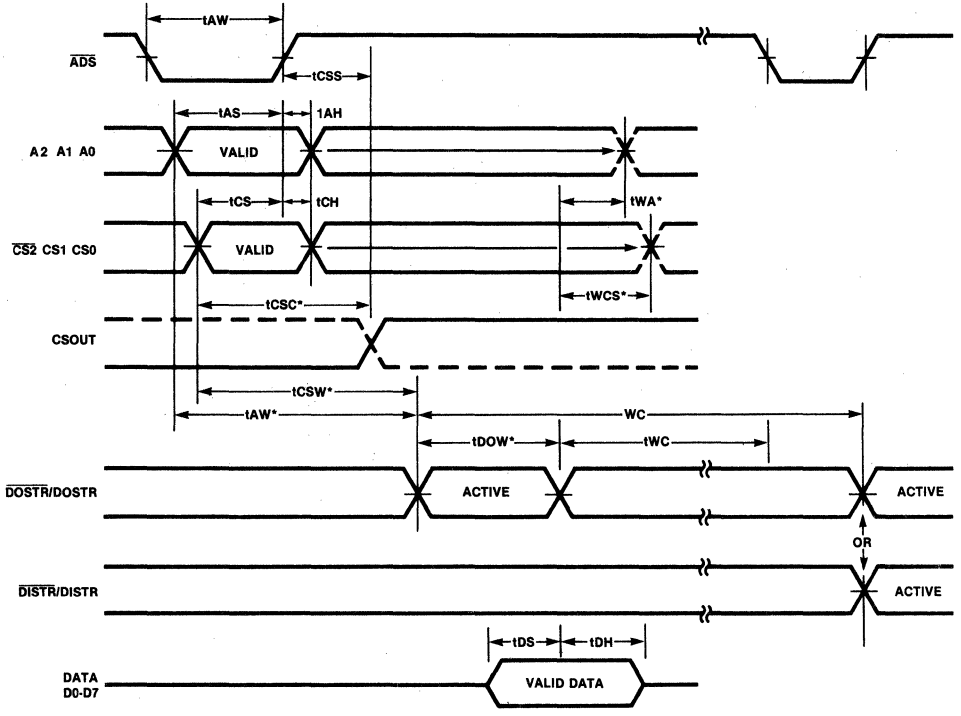


AC TEST POINTS



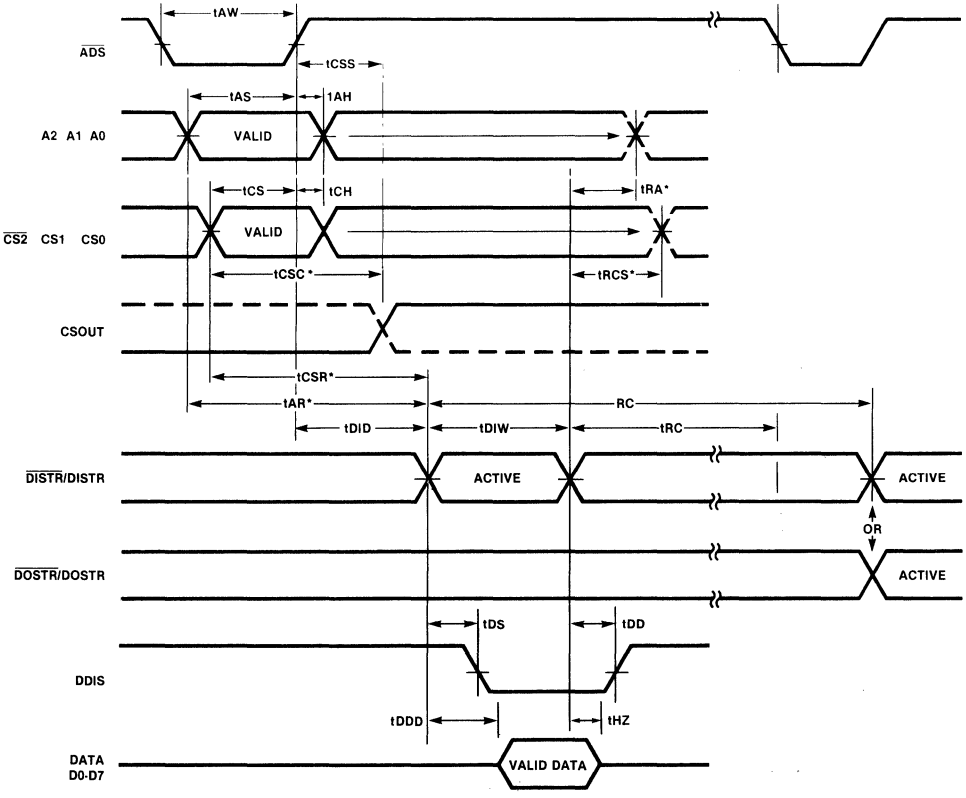
TIMING DIAGRAM

WRITE CYCLE

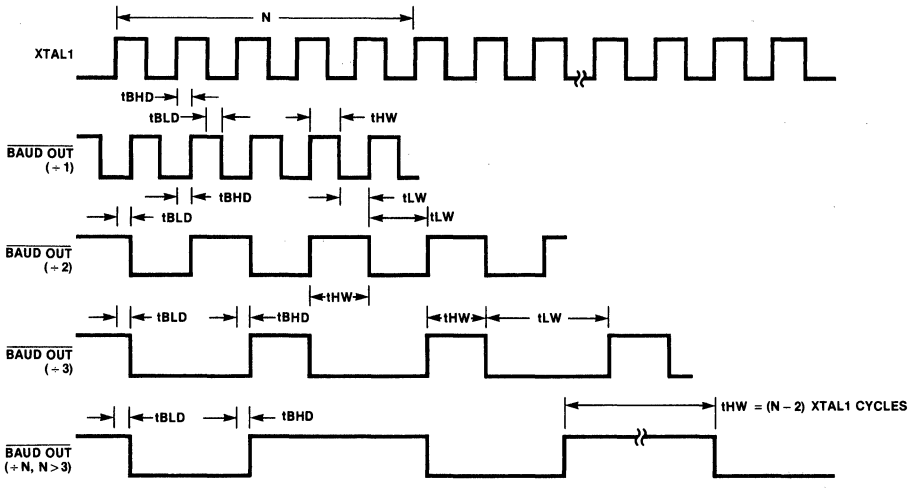


TIMING DIAGRAMS

READ CYCLE

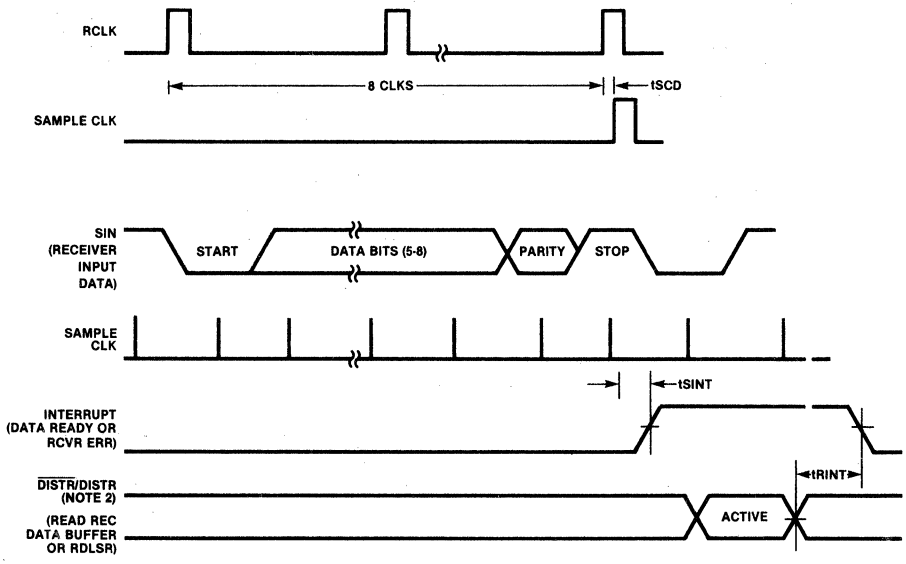


BAUDOUT

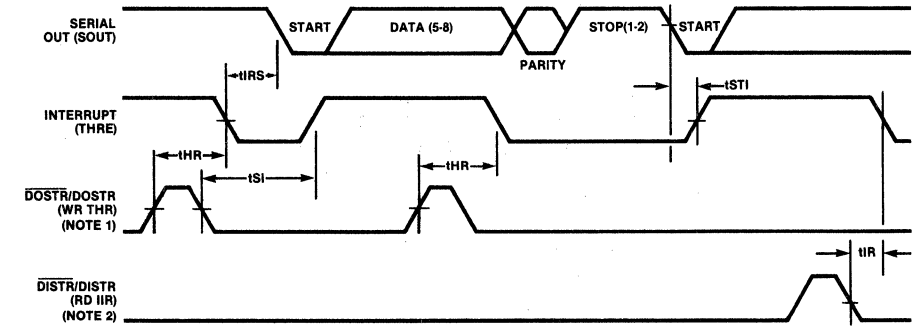


TIMING DIAGRAMS

RECEIVER



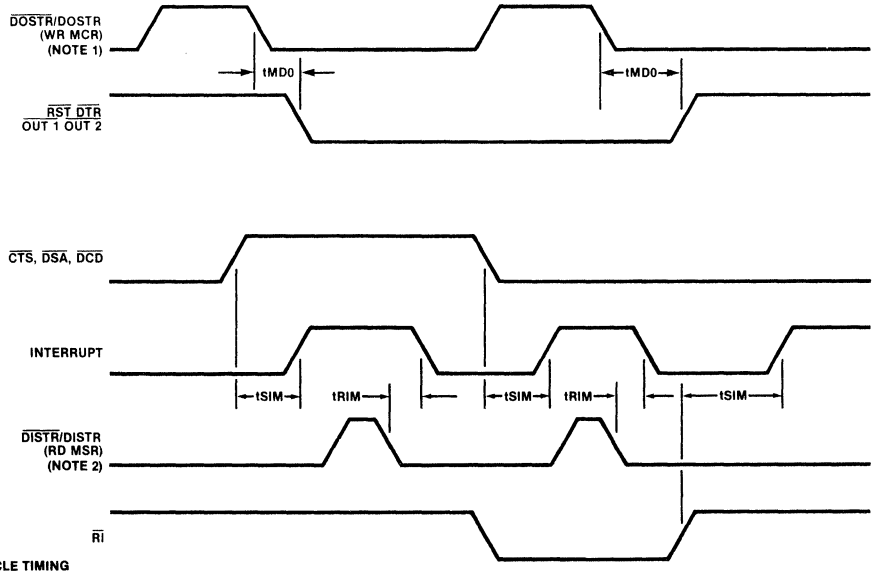
TRANSMITTER



NOTES:
1. SEE WRITE CYCLE TIMING
2. SEE READ CYCLE TIMING

TIMING DIAGRAM

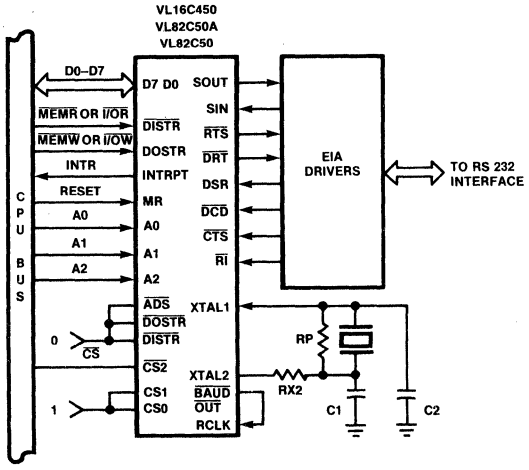
MODEM CONTROLS



NOTES:
1. SEE WRITE CYCLE TIMING
2. SEE READ CYCLE TIMING

BASIC CONFIGURATION

VL16C450, VL82C50A, VL82C50



TYPICAL COMPONENT VALUES

Crystal	RP	RX2	C1	C2
3.072 MHz	1 MΩ	1.5 Ω	10-30 pF	40-90 pF

VL1935

SYNCHRONOUS DATA LINE CONTROLLER

FEATURES

- HDLC, SDLC, ADCCP AND CCITT X.25 COMPATIBLE
- SDLC LOOP DATA LINK CAPABILITY
- FULL OR HALF DUPLEX OPERATION
- DC TO 2.0 MBITS/SEC DATA RATE
- PROGRAMMABLE/AUTOMATIC FCS (CRC) GENERATION AND CHECKING
- PROGRAMMABLE NRZI ENCODE/DECODE
- FULL SET OF MODEM CONTROL SIGNALS
- DIGITAL PHASE LOCKED LOOP
- FULLY COMPATIBLE WITH MOST CPU'S
- ERROR DETECTION: CRC, UNDERRUN, OVERRUN, ABORTED OR INVALID FRAME ERRORS
- STRAIGHT FORWARD CPU INTERRUPTS
- PROGRAMMABLE MODEM CONTROL INTERRUPTS
- DOUBLE BUFFERING OF DATA
- VARIABLE CHARACTER LENGTH (5, 6, 7 OR 8 BITS)
- RESIDUAL CHARACTER CAPABILITY
- ADDRESS COMPARE
- GLOBAL ADDRESS RECOGNITION
- EXTENDABLE ADDRESS FIELD
- EXTENDABLE CONTROL FIELD
- AUTOMATIC ZERO INSERTION AND DELETION
- MAINTENANCE MODE FOR SELF-TESTING
- PIN-COMPATIBLE REPLACEMENT FOR WD1933 AND WD1935

DESCRIPTION

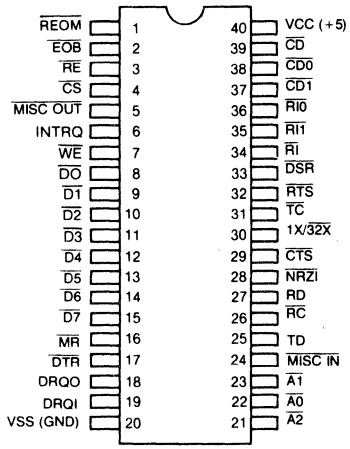
The VL1935 is a MOS/LSI microcomputer peripheral device which performs the functioning of interfacing a parallel digital system to a synchronous serial data communication channel employing ISO's HDLC, IBM's SDLC or ANSI's ADCCP line protocol. These protocols are referred to as Bit-Oriented Protocols (BOP).

The chip is fabricated in N-channel depletion load MOS technology and is TTL compatible on all inputs and outputs. This controller requires a minimum of CPU software by supporting a comprehensive frame-level instruction set and by hardware implementation of the low level tasks associated with frame assembly/disassembly and data integrity. It can be programmed to encode/decode NRZI data. The internal clock is then derived from the NRZI data using a digital phase locked loop.

The receiver and transmitter logic operates as two total independent sections with a minimum of common logic. The frames are automatically checked for errors during reception by verifying correct Frame Check Sequence (FCS). In transmit mode, the FCS is automatically generated by this controller and sent before the final Flag. It also continuously checks for other errors. In case of an error, the CPU is interrupted.

The controller recognizes and can generate Flag, Abort, Idle and GA characters. VL1935 can be used in an SDLC Loop configuration. An End of Block option is supplied to minimize CPU time. A full set of modem control signals are supplied to minimize external hardware.

PIN DIAGRAM



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL1935-10PC VL1935-10CC VL1935-10QC	0.5 MHz	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)
VL1935-11PC VL1935-11CC VL1935-11QC	1.0 MHz	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)
VL1935-12PC VL1935-12CC VL1935-12QC	1.5 MHz	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)
VL1935-13PC VL1935-13CC VL1935-13QC	2.0 MHz	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)

Note:
Operating temperature range: 0°C to +70°C.

PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	FUNCTION
1	$\overline{REOM}$	Received End of Message	Received End of Message with no Errors. This output signal is the inverse of IR7, bit 7 of the Interrupt Register.
2	$\overline{EOB}$	End of Block	This input, when low, function as an FCS command. Is independent of $\overline{CS}$.
3	$\overline{RE}$	Read Enable	This input, when low (and $\overline{CS}$ is active), gates the content of addressed register onto the Data bus.
4	$\overline{CS}$	Chip Select	This input, when low, selects the VL1935 for a read or write operation to/from the Data bus.
5	$\overline{MISC\ OUT}$	Misc Output	This output is an extra programmable output signal for the convenience of the user. Is controlled by the CR10 bit.
6	INTRQ	Interrupt Request	This output is high whenever any of the interrupt register bits IR7-IR3 are set. $\overline{TC}$ must be asserted to assert INTRQ.
7	$\overline{WE}$	Write Enable	This input when low (and $\overline{CS}$ is active), gates the content of the Data bus into the addressed register.
8 thru 15	$\overline{D0}$–$\overline{D7}$	Data Bus	Bidirectional three-state Data Bus. Bit 7 is MSB.
16	$\overline{MR}$	Master Reset	This input, when low, initializes all the registers, and forces the VL1935 into an idle state. The VL1935 will remain idle until a command is issued by the CPU.
17	$\overline{DTR}$	Data Terminal Ready	Modem Control Signal. This output, when low, indicates to the Data Communication Equipment (DCE) that the VL1935 is ready to transmit or receive data.
18	DRQO	Data Request Output	This output, when high, indicates that the Transmitter Holding Register (THR) is empty and ready to receive a data character from the Data bus for a transmit operation.
19	DRQI	Data Request Input	This output, when high, indicates that Receiver Holding Register (RHR) contains a newly received data character, available to be read onto the Data bus.
20	V_{SS}	V_{SS}	Ground
21 thru 23	$\overline{A2}$, $\overline{A0}$, $\overline{A1}$	$\overline{ADDRESS}$	These inputs are used to address the CPU interface registers for read/write operations.
24	$\overline{MISC\ IN}$	$\overline{Misc\ Input}$	This input is an extra input signal for the convenience of the user. The state is shown by the SR4 bit.
25	TD	Transmitted Data	This output transmits the serial data to the Data Communications Equipment/Channel.
26	$\overline{RC}$	Receive Clock	This input is used to synchronize the received data.
27	RD	Received Data	This input receives the serial data from the Data Communication Equipment/Channel.
28	$\overline{NRZI}$	$\overline{NRZI}$	This input, when low, sets the VL1935 in NRZI mode.
29	$\overline{CTS}$	Clear to Send	Modem Control Signal. This input when low, indicates that the DCE is ready to accept data from the VL1935.
30	1X/$\overline{32X}$	DPLL Select	This input controls the internal clock. When high (1X clock), the external clock has the same frequency as the internal clock. When low (32X clock), the external clock is 32 times faster than the internal clock and the DPLL Logic is enabled.
31	$\overline{TC}$	Transmit Clock	This input is used to synchronize the transmitted data, as well as generating either Receive or Transmit INTRQ's.

PIN DESCRIPTION (continued)

PIN NUMBER	MNEMONIC	SIGNAL NAME	FUNCTION
32	$\overline{RTS}$	Request to Send	Modem Control Signal. This output, when low, indicates to the DCE that the VL1935 is ready to transmit data.
33	$\overline{DSR}$	Data Set Ready	Modem Control Signal. This input, when low, indicates that the DCE is ready to receive or transmit data.
34	$\overline{RI}$	Ring Indicator	Modem Control Signal. This input, when low, indicates a ringing signal being received on the communication channel.
35 36	$\overline{RI1}$, $\overline{RI0}$	Ring Indicator Interrupt Control	These inputs are used to program Ring Indicator interrupts.
37 38	$\overline{CD1}$, $\overline{CD0}$	Carrier Detect Interrupt Control	These inputs are used to program Carrier Detect Interrupts.
39	$\overline{CD}$	Carrier Detect	Modem Control Signal. This input, when low, indicates there is a carrier signal received by the local DCE from a distant DCE.
40	V_{CC}	V_{CC}	+5VDC

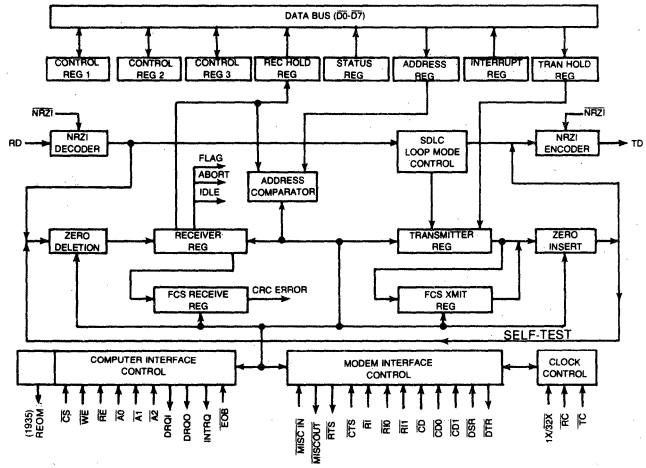
TABLE 1. VL1935 GLOSSARY

TERM	DEFINITION/DESCRIPTION
BOP	Bit-oriented protocols: SDLC, HDLC, and ADCCP
ABORT	11111111 (seven or more contiguous 1's)
GA	Go-ahead pattern. 01111111 (0(LSB) followed by seven 1's)
LSB	First transmitted bit and first received bit. (Least significant bit)
MSB	Last transmitted bit and last received bit. (Most significant bit)
IDLE	11111111 11111111 (15 or more contiguous 1's)
FLAG	01111110. Starts and ends a Frame.
A-FIELD	Address-field in the Frame. Consists of one or more 8-bit characters. Defines the address of a particular station.
C-FIELD	Control field in the Frame. Consists of one or two 8-bit characters.
I-FIELD	Information field in the Frame. Consists of any number of bits.
FCS	Frame Check Sequence. A 16-bit error checking field sequence.
FRAME	A communication element, consisting of a minimum of 32 bits, and delimited by FLAGS.
GLOBAL ADDRESS	An A-field character of eight 1's. When this is compared and matched in the Address comparator, the DRQI will be set, indicating a valid address
RESIDUAL CHARACTER	The last I-field character, consisting of a lesser amount of bits than the other I-field characters in the Frame.
DATA SET	Data Communication Equipment (DCE). May be a modem.
BIT TIME	Length in time of a serial data bit.

APPLICATIONS

COMPUTER COMMUNICATIONS
TERMINAL COMMUNICATIONS
COMPUTER TO MODEM INTERFACING
LINE CONTROLLERS
FRONT END COMMUNICATIONS
NETWORK PROCESSORS
TELECOMMUNICATION SWITCHING NETWORKS
MESSAGE SWITCHING
PACKET SWITCHING
MULTIPLEXING SYSTEMS
DATA CONCENTRATOR SYSTEMS
SDLC LOOP DATA LINK SYSTEMS
DMA APPLICATIONS
COMMUNICATION TEST EQUIPMENT
LOCAL NETWORKS
MULTIDROP LINE SYSTEMS

FIGURE 1. VL1935 BLOCK DIAGRAM



A BRIEF DESCRIPTION OF HDLC, SDLC AND ADCCP PROTOCOLS

The VL1935 is compatible with HDLC, SDLC and ADCCP standard communication Link Protocols. These are bit-oriented, code independent, and ideal for full duplex communication. A single communication element is called a FRAME, which can be used for both link control and data transfer purposes.

The elements of a frame are the beginning eight bit FLAG (F) consisting of one logical "0" six 1's and a 0, an eight bit ADDRESS-FIELD(A), an eight bit CONTROL-FIELD (C), a variable (N bits) INFORMATION-FIELD, a sixteen bit FRAME-CHECK-SEQUENCE (FCS), and an eight bit end FLAG (F), having the same bit-pattern as the beginning flag.

In HDLC, the address (A) and control (C) characters are extendable (more than one character). An important characteristic of a frame is that its contents are made code transparent by use of a zero bit insertion and deletion technique. Thus, the user can adapt any format or code suitable for his system. The frame is bit-oriented, meaning that, bits not characters in each field have specific meanings. The Frame Check Sequence (FCS) is an error detection scheme similar to the Cyclic Redundancy Checkword (CRC) widely used in magnetic disk storage devices. The frame format is shown in Figure 3.

Figure 2. VL1935 TYPICAL SYSTEM INTERFACE

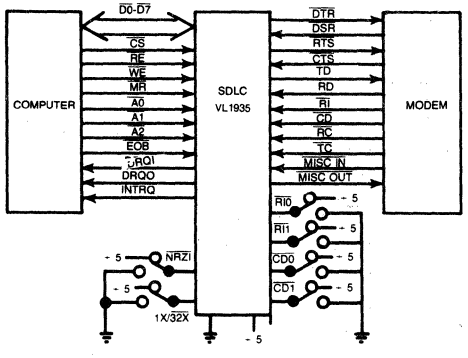
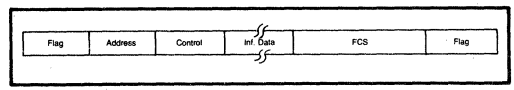


FIGURE 3. VL1935 SDLC/HDLC/ADCCP FRAME FORMAT



Where:

FLAG = 01111110

Address field—One or more 8-bit characters defining the particular station

Control field—One or two 8-bit characters

Information field—Any number of bits (may be zero bits)

Frame Check Sequence—16-bit error checking field

The following features are also part of these protocols.

ZERO INSERTION/ZERO DELETION—Zero insertion/deletion is performed within the 2 Flags of a frame. If there are more than five 1's in a row, a 0 is automatically inserted after the fifth 1 and it is deleted upon reception by the receiver.

FRAME CHECK SEQUENCE (FCS)—A 16 bit cyclic redundancy check (CRC) calculation is performed during transmission of the data in between the 2 flags of the frame. The CRC is then transmitted after the I-field and before the final FLAG. Upon reception the receiver also performs a CRC calculation on the incoming data. If there were no transmission error, the Receiver CRC equals F0B8 (hex).

HARDWARE ORGANIZATION

The VL1935 block diagram is illustrated in Figure 1 and described below.

CPU Interface Registers

All of these registers are addressable and to be read from and/or written into by the CPU via the Data bus. These are 8-bit registers and have to be enabled via Chip Select ($\overline{CS}$) before any data transfer can be done.

CONTROL REGISTER 1, 2, 3 (CR1, 2, 3) Operations are initiated by writing the appropriate commands into these registers. CR1 should be programmed last.

RECEIVER HOLDING REGISTER (RHR) When Data Request Input is set (DRQI=1), contains received assembled character.

ADDRESS REGISTER (AR) Contains the address of the accessed VL1935, which is to be compared to the received address character (A-field).

INTERRUPT REGISTER (IR) Contains the cause of the current interrupt request.

TRANSMITTER HOLDING REGISTER (THR) Is to be loaded with the next in line character to be transmitted, when Data Request Output is set (DRQO=1).

STATUS REGISTER (SR) Contains the overall status of the VL1935 plus some information of the last received frame.

Non-Addressable, Internal Registers

These registers are transparent to the user, but is mentioned in these data sheets to help the understanding of the VL1935.

TRANSMITTER REGISTER (TR) This 8-bit register functions as a buffer between the THR and the TD output. It is loaded from the THR (if Data Command) with the next character to be transmitted. A FLAG character may also be loaded into this register under program control. This character is automatically shifted out to the Transmit Data output. When the last bit of the current transmitted character has left the TR register, a new character will be loaded into this register, setting DRQO (Data command) or INTRQ (Abort, Flag or FSC command). If at the time when only one bit remains left in the TR register, and the THR is not loaded or a new command is not programmed (Data command), an underrun error will occur.

RECEIVER REGISTER (RR) The received data is, via the Zero-Deletion logic shifted into this 8-bit register. The data is here assembled to a 5, 6, 7 or 8-bit character length and then, under the right conditions, parallel transferred to the RHR register.

FCS RECEIVE REGISTER AND FCS XMIT REGISTER The VL1935 contains a 16-bit CRC check register (FCS REC. REG.) and a 16-bit CRC generation register (FCS XMIT REG.). The generating polynomial is:

$$G(X) = X^{16} + X^{12} + X^5 + 1$$

The transmitter and receiver initialize the remainder value to all ones before CRC accumulation starts. The data is multiplied by X^{16} and is divided by G(X). Inserted 0's are not included in the accumulation. Under program control, the complement called the frame check sequence (FCS) is sent with high order bit first.

Various Internal Circuits

ADDRESS COMPARATOR This 8-bit comparator is used to compare the contents of the Address Register with the first address character of the incoming frame. This feature is enabled by a bit in the Command Register. If enabled and there is a match, the received frame is valid and DRQIs are generated for every character received (including the A-field). If enabled and there is not a match or there is no Global Address, the received frame is discarded. If not enabled, all received frames are valid and DRQIs are generated.

ZERO INSERTION The transmitted data stream is continuously monitored by this logic. A zero is automatically inserted following five contiguous 1 bits anywhere between the beginning FLAG and the ending FLAG of a frame. The insertion of the zero bit thus applies to the contents of the Address, Control, Information Data, and the FCS field.

ZERO DELETION The received data stream is continuously monitored by this logic. Upon receiving five contiguous 1 bits, the sixth bit is inspected. If the sixth bit is a 0, it is automatically deleted from the data stream. If the sixth bit is a 1, the seventh bit inspected; if it is a 0, a FLAG is recognized; if it is a 1 an ABORT or GO AHEAD is recognized.

DATA BUS ($\overline{D7}$-$\overline{D0}$) This is an inverted 8-bit bidirectional data bus.

SDLC LOOP-MODE CONTROL This logic supervises the VL1935 running in SDLC Loop mode. It monitors the received data for a GO-AHEAD pattern in the case when SDLC LOOP MODE bit (CR22) and ACT TRAN bit (CR16) are set. When GO-AHEAD pattern is received, this logic suspends the repeater function and initiates the transmitter function. For more details, see functional description of SDLC Loop Mode.

NRZI ENCODER/DECODER When this mode is selected, the NRZI Encoder encodes the "normal" transmitted data to NRZI formatted data and the NRZI Decoder decodes the received NRZI data to "normal" data.

A binary 1 for "normal data" is TD = high.

A binary 1 for NRZI data is TD = no change.

A binary 0 for "normal data" is TD = low.

A binary 0 for NRZI data is TD = change of state.

COMPUTER INTERFACE CONTROL This logic interfaces the CPU, to the VL1935. It supervises the read and write functions to the addressable registers, generates data requests and interrupts, decodes and initiates commands, monitors the status of VL1935, etc.

MODEM INTERFACE CONTROL This logic interfaces and supervises the modem control signals to/from the VL1935. It provides both dedicated (EIA Standard) and user defined control functions.

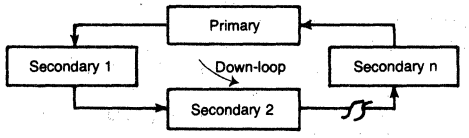
CLOCK CONTROL This logic interfaces the transmit and receive clocks to the VL1935. It converts the external clocks to the necessary internal clocks.

FUNCTIONAL DESCRIPTION

SDLC Loop Mode

The diagram below shows an SDLC Loop Data Link System. VL1935 can be used in any of these stations.

FIGURE 4. VL1935 SDLC LOOP DATA LINK



Each secondary station is normally a repeater in Receive mode (ACT REC bit on). The primary station is the loop controller. Signals sent out on the loop by the primary station are relayed from station to station, then back to the Primary. Any secondary station finding its address in the A-field captures the frame for action at that station. All received frames are relayed to the next station on the loop.

If a secondary station wants to transmit a message, it sets the ACT TRAN bit ($\overline{CTS}$ must be low) and waits for a GO AHEAD (GA) pattern. The ACT REC bit must be asserted for detection of the GA and other existing patterns. Until the GA pattern is received, this secondary station continues operating as a repeater. The primary station has the responsibility to generate the first GA pattern which can be accomplished by a flag followed by continuous 1's. The primary station must continue to send 1's until the GA has circulated through the entire loop. The first secondary station with its ACT TRAN bit set detects the GA and changes the last 1 bit of the GA pattern to a 0, thus generating the start flag of the frame it wants to transmit and preventing the GA pattern from propagating down the loop. The repeater function is then suspended by this secondary station and it goes into the transmit mode. When this secondary station completes its transmission frames, it resets the ACT TRAN bit and reverts back to the repeater mode. It repeats the 1's generated by the primary station to form another GA pattern from the final 0 of its ending flag. The GA pattern propagates through the loop until a secondary station down the loop, that wants to transmit (ACT TRAN bit is set), intercepts the GA pattern and starts to transmit as described, or until the primary station receives the idles (continuous 1's), indicating that the GA pattern has circulated through the entire loop. The primary station then generates another GA pattern or terminates its final data frame with continuous 1's.

Repeaters (Secondary stations) delay the received data by 4 bits (NRZ1 = 5 bits) before transmission.

The $\overline{RC}$ and $\overline{TC}$ clocks must be tied together. The internal DPLL will not function in the loop mode.

1X/32X Clock Option

When 1X clock is selected, the data rate equals the external clock (receiver and transmitter).

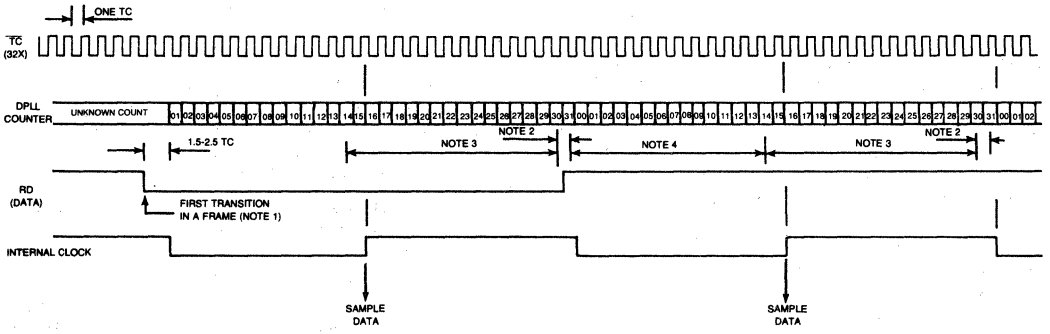
When 32X clock is selected, the external clock rate is 32 times faster than the data rate.

Digital Phase Locked Loop (DPLL)

This feature is particularly useful in NRZI mode and/or when asynchronous modem is used. The purpose of the DPLL is to synchronize the internal 1X clock to the received data, thus insuring that this data is sampled in the middle of the incoming serial data bit. DPLL is automatically in operation when 32X clock is selected.

The DPLL Logic is initiated at the first received data transition in a frame. Corrections, if needed, are then made for each received data transition. A 32-counter is used for this operation. At the beginning of each frame and at the first received data transition, this 32 counter is reset. From this time on, the counter increments with one count for each external clock pulse. At count 16 the internal 1X clock is forced to change state to high (this transition = sampling time). At count 32, the counter resets itself. This forces the internal 1X clock again to change state back to low.

FIGURE 5. VL1935 DPLL TIMING DIAGRAM



NOTE 1. FIRST DATA TRANSITION (FIRST FLAG) SETS THE DPLL COUNTER TO 01.

NOTE 2. DATA TRANSITION IN BETWEEN HERE, OR NO DATA TRANSITION AT ALL, CAUSES NO CORRECTION OF THE DPLL COUNTER.

NOTE 3. DATA TRANSITION IN BETWEEN HERE, WILL INCREMENT ONE COUNT TO THE DPLL COUNTER (ADD 01 TO WHAT IS SHOWN).

NOTE 4. DATA TRANSITION IN BETWEEN HERE, WILL DECREMENT ONE COUNT TO THE DPLL COUNTER (SUBTRACT 01 TO WHAT IS SHOWN).

At each received data transition, if the internal clock and the received data is out of synchronization, a correction is automatically made by ± 1 external clock period. See DPLL Timing Diagram in Figure 5.

End Of Block (EOB)

This is an FCS command. The main purpose of EOB is to allow the user to initiate FCS and FLAG without the need of using extra computer time. This is particularly practical in DMA applications. At the end of a frame, when the last information data character has already been loaded into the THR and once again DRQO is set, either a regular FCS command is written into CR1 Register, or $\overline{EOB}$ is to be activated. At the end of FCS, when INTRQ is set (XMIT OPCOM), the $\overline{EOB}$ if activated is to be reset again.

Serial Data Synchronization

The serial data is synchronized by the externally supplied Transmit Clock ($\overline{TC}$) and Receive Clock ($\overline{RC}$). When 1X clock is selected, the falling edge of $\overline{TC}$ generates new transmitted data and the rising edge of $\overline{RC}$ is used to sample the received data. When 32X clock is selected, a 32-counter (in the DPLL Logic) is used to synchronize the internal clock. At time 0, when the counter is reset to 0, the new transmitted data is generated. At time 16 (counter = 16) the received data is sampled, insuring that sampling is done in the middle of the received serial data bit. At count 32, the counter is reset to 0 again.

Self Test (Diagnostic) Mode

This feature is a programmable Loop back of data, enabling the user to make a complete test of the VL1935 with a minimum of external circuitry. In this mode, transmitted data to the TD pin, is internally routed to the received data input circuitry, thus allowing a CPU to send a message to itself to verify proper operation of the VL1935. The modem control signals $\overline{DTR}$ and $\overline{RTS}$ are deactivated (off) to insure no interference to/from the Data Communication Equipment (DCE). $\overline{DSR}$ and $\overline{CTS}$ are internally activated for proper input conditions. $\overline{TC}$ and $\overline{RC}$ should be supplied by the same source if 1X clock is selected.

Auto Flag

If this is selected and Data Command is executed, continuous Flags will be sent between frames. This eliminates the need to execute the Flag Command. In DMA applications in particular, this is very practical.

Extended Addressing

This type of addressing means, that there is more than one address character in the A-field. In receive mode, the first address character is compared in the Address Comparator of the VL1935. The other address character/s is to be compared by the CPU. The last address character is recognized by the fact that the LSB (bit 2°) is a 1.

PROGRAMMING

Controlling Operation

Prior to initiating data transmission or reception, CONTROL REGISTER 1-3 (CR1-3) must be loaded with control information from the CPU. The contents of these registers will configure the VL1935 for the user's specific data communication environment. These registers should be loaded during power-on initialization and after a reset operation. They can be changed at any time that the respective transmitter or receiver is deactivated. The CR1-3 dictate what the transmitter will send: the type of character (DATA, ABORT, FLAG or FCS), the number of bits per character, and the number of bits in the residual character. Similarly, they tell the receiver the types of frames to look for: the number of bits per I-field character, whether to perform an address compare, and whether to watch for an extended address. The Control Register also control Data Terminal Ready ($\overline{DTR}$), $\overline{Misc\ Out}$ and the activation of both the transmitter and the receiver. For more detailed information, see Register Formats.

Monitoring Operation

Monitoring is done by use of the Interrupt Register (IR) and Status Register (SR). The IR register indicates when a frame is completed (transmitted or received), if there was an error and if there is a Data Set Change. It also monitors the states of INTRQ, DRQO and DRQI.

The SR register indicates if an error is recognized by IR, what type of error. It also monitors the modem control signals; Ring Indicator ($\overline{RI}$), Carrier Detect ($\overline{CD}$), Data Set Ready ($\overline{DSR}$) and $\overline{Misc\ In}$.

Furthermore, the SR register monitors if the Receiver is idle, and also if in receive mode if the user has programmed the Receiver Character Length to be 8 bits per character, this register indicates the number of residual bits received. For more detailed information, see Register Formats.

Read/Write Control Of CPU Interface Registers

These registers are directly accessible from the CPU bus ($\overline{D7}$-$\overline{D0}$) by a read and/or write operation by the CPU.

The CPU must set up the VL1935 register address ($\overline{A2}$-$\overline{A0}$), Chip Select ($\overline{CS}$), Write Enable ($\overline{WE}$) or Read Enable ($\overline{RE}$) before each data bus transfer operation.

During a write operation, the falling edge of $\overline{WE}$ will initiate a VL1935 write cycle. The addressed register will then be loaded with the content of the Data Bus ($\overline{D7}$-$\overline{D0}$). During a read operation, the falling edge of $\overline{RE}$ will initiate a VL1935 read cycle. The addressed register will then place its content onto the Data Bus ($\overline{D7}$-$\overline{D0}$). The read/write operation is completed, when $\overline{CS}$ or $\overline{RE}$/$\overline{WE}$ is brought high.

See Read/Write Timing diagram for more detailed information.

For read and write operation, the CR1-3 registers normally need no external clock. After reset of CR1-3, $\overline{TC}$ clock is required. The AR and THR registers need no external clock, and can only be written into. The RHR, IR and SR registers need Transmit Clock ($\overline{TC}$) or Receive Clock ($\overline{RC}$) to set various bits, and are read-only.

All these registers will get initialized by a Master Reset. A read operation of RHR resets the DRQI. A write operation to THR, resets the DRQO. A read operation of IR, resets IR bits 0 and 3-7. A read operation of SR, resets SR bits 0-2. For addressing and external clocks needed, see TABLE 2.

A more detailed description is shown in Figure 6 of each bit location. It should be known, that because the Data Bus Lines ($\overline{D7}$-$\overline{D0}$) have inverted logic, a logic 1, asserted means low state. Also, a modem control signal which is inverted (example $\overline{DTR}$), is in on-state (asserted) when low.

TABLE 2. DEVICE ADDRESS CODES

$\overline{CS}$	$\overline{A2}$	$\overline{A1}$	$\overline{A0}$	Read	Write	External Clock
L	H	H	H	CR1	CR1	None*
L	H	H	L	CR2	CR2	None*
L	H	L	H	CR3	CR3	None*
L	H	L	L	RHR	AR	RHR=$\overline{RC}$. AR=None
L	L	H	H	IR	THR	IR=$\overline{TC}$. THR=None
L	L	H	L	SR	—	SR0-3=$\overline{RC}$. SR4-7=None.
H	X	X	X	X	X	

L = V_{IL} at pins
H = V_{IH} at pins
X = Don't care

*2.5 $\overline{TC}$ clock cycles are required after a Master Reset to be able to read and write.

REGISTER FORMATS

Below shows a short form register format.

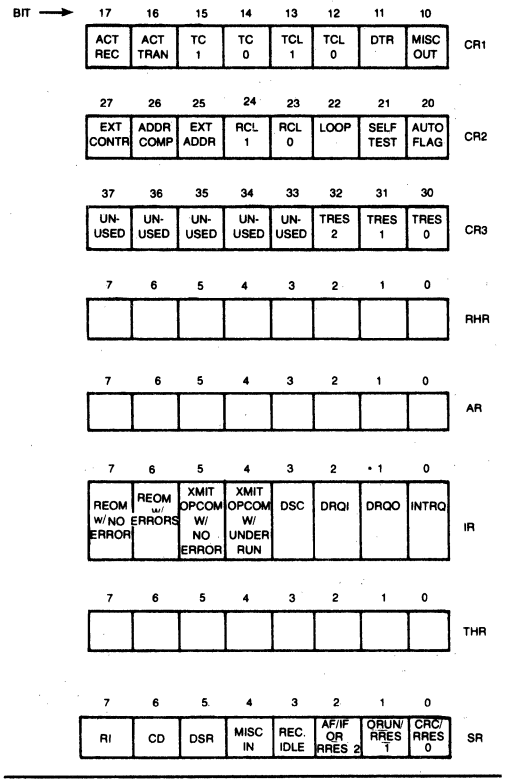


FIGURE 6. VL1935 BIT ASSIGNMENTS

Control Register 1 (CR1)

When initiating a transmit/receive operation, this should be the last register programmed.

Miscellaneous Output (CR10) This bit controls the Miscellaneous Output signal to the data set. When CR10 is a logical 0, $\overline{\text{Misc Out}}$ is off, when it is a logical 1, $\overline{\text{Misc Out}}$ is on.

DTR Command (CR11) This bit controls the data Terminal Ready ($\overline{DTR}$) signal to the data set. When CR11 is a logical 0, $\overline{DTR}$ is off. When CR11 is a logical 1, $\overline{DTR}$ is on. When the Self-Test mode is selected, $\overline{DTR}$ signal is forced to an off state.

Transmitter Character Length (CR13, 12) These bits control the transmitted I-field data character length. The data character may be 5, 6, 7 or 8 bits long.

TABLE 3. TRANSMITTER CHARACTER LENGTH

CR13 (TCL1)	CR12 (TCL0)	Bits Per Character
0	0	8
0	1	7
1	0	6
1	1	5

Transmitter Commands (CR15, 14) These bits control the transmission of DATA (A-field, C-field and I-field), ABORT, FLAG, and FCS (FCS plus FLAG). When these commands are programmed, the previous command currently still in progress, will complete the transmission of its character. When this is done, a new character generated by this new command, will be transmitted.

CR 14, 15 can be programmed as follows:

A. If DATA is programmed, the new character to be transmitted will be the character loaded (or still to be loaded) in the THR REGISTER.
B. If ABORT is programmed, the new character will be eight logical 1's.
C. If FLAG is programmed, the new character will be 01111110.
D. If FCS is programmed, the new character which will be transmitted consists of the residual byte (which was automatically transferred to the XMIT REGISTER, provided that CR30-32 and are set correctly), followed by the 16-bit content of the FCS XMIT REGISTER and the FLAG.

One serial bit ahead of this new character (for FCS command the FLAG character), the CPU is signalled by DRQO or INTRQ that the VL1935 is again ready to receive a new command. DRQO is asserted by a DATA command and INTRQ (XMIT OPCOM) is asserted by an ABORT, FLAG or FCS command.

TABLE 4. TRANSMITTER COMMANDS

CR15 (TC1)	CR14 (TC0)	Command	Character/s Transmitted	Signal to CPU
0	0	DATA	Content of THR	DRQO
0	1	ABORT	1111 1111	INTRQ
1	0	FLAG	0111 1110	INTRQ
1	1	FCS	FCS + 01111110	INTRQ

In the case of the DATA command the user has two choices; 1. Change the command. 2. Keep the DATA command and load a new character into the THR register For more information, please see the Transmission Timing diagram, Figure 7. See Table 4 for programming information.

Activate Transmitter (CR 16) This bit when set, enables the transmitter and sets $\overline{RTS}$ signal. If in SDLC Loop Mode (CR22 = set), the transmitter waits for a Go-Ahead pattern before the transmitter is enabled.

Activate Receiver (CR 17) This bit when set activates the receiver, which begins shifting in frames one character at a time into RR register for inspection.

CONTROL REGISTER 2 (CR2)

Auto Flag (CR20) When set, Flags (without INTRQs) will be continuously transmitted in between frames, when otherwise the transmitter would be in idle state.

Self-Test Mode (CR21) When set, the Transmitter Data Output is internally connected to the Receiver Data input circuitry. The modem control output signals are deactivated (off state). The modem control input signals are internally activated. This mode allows off-line diagnostic.

SDLC Loop Mode (CR22) When set, the VL1935 is conditioned to operate in an SDLC Loop Data Link system (see SDLC Loop Mode).

Receiver Character Length (CR24, 23) These bits indicate to the receiver how many bits per character there are to assemble for the I-field. The I-field characters may be 5, 6, 7 or 8 bits long. The unused bits read from RHR will be logical 0.

TABLE 5. RECEIVER CHARACTER LENGTH

CR24 (RCL1)	CR23 (RCL0)	Bits Per Character
0	0	8
0	1	7
1	0	6
1	1	5

Extended Address (CR25) When set, this bit indicates to the receiver that there is more than one address character in the A-field. The receiver will expect another address character if the LSB in the current address character is a logical 0. The purpose of this bit: If a non-8-bit field character length is expected, the DRQIs will get out of synchronization if the VL1935 does not know exactly when the I-field will start. Not used in transmit mode.

Address Compare (CR26) When set, the first address character will be inspected in the Address Comparator. If there is a match with the AR register, or if the address compared is a Global Address (eight 1's) the frame is considered valid, causing DRQIs to be generated. Otherwise, the receiver does not react, and will continue comparing for a new valid address. If not set, all frames are considered valid.

Extended Control (CR27) When set, indicates that there are two control characters per name. If not set, there is only one control character per frame. The purpose of this bit: If a non-8-bit I-field character length is to be received, the DRQIs will get out of synchronization if the VL1935 does not know when the I-field will start. Not used in transmit mode.

CONTROL REGISTER (CR3)

Transmit Residual Character Length (CR32, 31, 30) (Table 6) These bits inform the transmitter what bit-length the residual character will be. If no residual character is to be sent, these bits must be set to logical 0. (See Transmitter Commands).

Unused (CR33-37) These bits are not used, and are always a logical 0.

INTERRUPT REGISTER (IR)

This register contains the information why an interrupt INTRQ was generated. An IR register read operation, will reset bits 0, and 3-7. The Transmitter clock must be active to generate an interrupt.

Loading the THR register, will reset DRQO (bit 1). Reading the RHR register, will reset DRQI (bit 2). A new interrupt will occur if one is pending.

TABLE 6. TRANSMITTER RESIDUAL COMMANDS

CR32 (TRES 2)	CR31 (TRES 1)	CR30 (TRES 0)	Residual Char. Length
0	0	0	No residual char. sent
0	0	1	1 bit
0	1	0	2 bits
0	1	1	3 bits
1	0	0	4 bits
1	0	1	5 bits
1	1	0	6 bits
1	1	1	7 bits

TABLE 7. DATA SET CHANGE PROGRAMMING

$\overline{CD1}$	$\overline{CD0}$	Interrupting edge of $\overline{CD}$	$\overline{RI1}$	$\overline{RI0}$	Interrupting edge of $\overline{RI}$
LO	LO	Rising and falling	LO	LO	Rising and falling
LO	HI	Falling	LO	HI	Falling
HI	LO	Rising	HI	LO	Rising
HI	HI	None	HI	HI	None

If a new interrupt is generated while the CPU is reading the IR register, this new interrupt will set the respective bit in the IR register one bit time later (this to avoid losing any interrupt). The status of bits 3–7 will accumulate until the IR register is read by CPU.

INTRQ (IR0) When set, indicates an interrupt and that there are one or more bits set in positions 3 through 7 of this register. This bit is a mirror image of INTRQ signal (pin 6).

When pin 6 (INTRQ) is not used for pending interrupts information and only the IR register is read to obtain the status of the interrupt bits (polling method), a minimum of two (2) bits times must be allowed between IR registers "read's" to insure an orderly flow of pending interrupts.

DRQO (IR1) When set, indicates a Data request output. This bit is a mirror image of DRQO signal (pin 18).

DRQI (IR2) When set, indicates a Data Request input. This bit is a mirror image of DRQI signal (pin 19).

Data Set Change (IR3) When set, indicates a change of state of the Data Set (Data Communication Equipment). This is a change of state of $\overline{DSR}$, $\overline{CD}$ or $\overline{RI}$. The type of change of $\overline{CD}$ and $\overline{RI}$ that this bit will react to, is programmed by use of input signals $\overline{CD1}/\overline{CD0}$ and $\overline{RI1}/\overline{RI0}$ (Table 7).

XMIT Operation Complete with Underrun Error (IR4) When set, indicates that the transmitter command has been completed and there was an Underrun error. An Underrun error occurs when the Data Request Output (DRQO) is set, but THR register is not loaded in time.

XMIT Operation with No Error (IR5) When set, indicates that the transmitter command has been completed and there was no error.

Received End of Message With Errors (IR6) When set, indicates that a Received End of Message is detected, and there was an error. Errors include CRC, Overrun, Invalid Frame and Aborted Frame.

The SR Register bits 0–2 will indicate the exact type of error.

Received End of Message With No Error (IR7) When set, indicates that a Received End of Message is detected, and there was no error. The IR7 bit is the inverse of the $\overline{REOM}$ output signal.

STATUS REGISTER (SR)

This register contains the status of the receiver and some modem control signals. It also indicates (if REOM w/Errors) exactly what type of errors. If the Receiver Character Length is 8 bits, this register indicates the amount of Residual bits that was received. A read operation will reset bits 0–2.

Received Error/Received Residual Character Length (SR 2-0) If REOM w/NO ERROR (IR7) is set, these bits (SR 2-0), indicate the number of residual bits received (Table 8).

If REOM WITH ERROR (IR 6) is set, these bits indicate the type of error that occurred (Table 9).

TABLE 8.

CHAR. LENGTH	RES. BITS	SR 0	SR 1	SR 2
8 Bits/Char.	0	0	0	0
	1	0	0	1
	2	0	1	0
	3	0	1	1
	4	1	0	0
	5	1	0	1
	6	1	1	0
	7	1	1	1
7 Bits/Char.	0	0	1	0
	1	0	1	1
	2	1	0	0
	3	1	0	1
	4	1	1	0
	5	1	1	1
	6	0	0	1
6 Bits/Char.	0	1	0	0
	1	1	0	1
	2	1	1	0
	3	0	0	1
	4	0	1	0
	5	0	1	1
5 Bits/Char.	0	0	0	1
	1	0	1	0
	2	0	1	1
	3	1	0	0
	4	1	0	1

TABLE 9.

Bit Set	Error
SR0	CRC
SR1	Overrun
SR2	Aborted or Invalid frame

Receiver Idle (SR 3) When set, indicates that the receiver is currently IDLE.

Miscellaneous Input (SR4) This is a mirror image of $\overline{MISC}$ IN signal. When this signal is set, SR4 bit is set.

Data Set Ready (SR5) This is mirror image of $\overline{DSR}$ signal. When this signal is set, SR5 bit is set.

Carrier Detect (SR6) This is a mirror image of $\overline{CD}$ signal. When this signal is set, SR6 bit is set.

Ring Indicator (SR7) This is the inverse of the $\overline{RI}$ signal. When SR7 bit is set, a ringing signal has been received on the communication channel.

TRANSMITTER OPERATION

Prior to this operation, the programmable inputs and the transmit mode related register bits need to be programmed according to the user's specific data communications environment. The last bit to be set is always the ACT TRAN (CR16) bit.

Before this, the INTRQ has to be cleared, which can be done by reading the IR register. For more detailed information how to program the VL1935 see Programming.

As an example of how to program the VL1935 let's assume a 24-bit information is to be transmitted. The I-field would then consist of three 8-bit characters with no residual bits. CR3 should then be 00 (Hex).

Bits CR23-CR27 are for reception only (see Receiver Operation). The last register to be programmed is CR1. If MISC OUT is not used, this may be ignored. If a modem is used, DTR (CR11) is to be set. CR13 and CR12 should be logical 0's (8-bit char. length). CR15 and CR14 should be logical 0's (Data Command). ACT TRAN (CR16) bit is to be set. The ACT REC (CR17) is for reception only.

The DTR bit, when set, activates the $\overline{DTR}$ signal, indicating to the modem to prepare for communication. When the modem is ready, it sends back a Data Set Ready ($\overline{DSR}$) to the VL1935 . This causes the DSC (IR3) bit to set, which in turn activates INTRQ. The IR register is now read. Simultaneously, when the ACT TRAN (CR16) bit is set, this activates the Request to Send ($\overline{RTS}$) signal, instructing the modem to enter into transmit mode. When the modem is ready to transmit data, it responds by activating the Clear to Send (CTS) signal.

The VL1935 is now conditioned to transmit. Now DRQO gets, set, indicating to the CPU (or DMA) to load the first character (Address) into the THR. When this is done, DRQO will reset. As soon as the VL1935 is ready to be loaded with the next character to be transmitted, DRQO is again set. When the THR register is again loaded with a character, DRQO will again reset.

This same sequence continues until the last I-field character to be transmitted is loaded into the THR. If CRC checking is to be used, the next time when DRQO is set, an FCS command has to be programmed. This is accomplished bv either setting CR15, 14 to both logical 1's or by activating the $\overline{EOB}$ signal.

At the end of the FCS being transmitted, INTRQ will set indicating XMIT Operation Complete. The IR register is to be read to find out whether the frame was sent with or without error. Also the FCS Command which was used as described above has to be changed. If CR15, 14 were set, these have to be reset (to Data Command), or if $\overline{EOB}$ was activated, this signal has to be deactivated. At this same time, the ACT TRAN bit is allowed to be reset, causing the TD output to go idle after the end Flag is sent. If the ACT TRAN bit is kept set, continuous Flags will be sent following the FCS.

If a new frame is to be sent right after this first frame, only one Flag is needed in between frames, meaning the frames have one common Flag character. In this case, the second frame Address character may be loaded at the same time the FCS command is programmed during the first frame. Also, the ACT TRAN bit should be kept set in between frames. Every time DRQO gets set, the user must load the THR register before the last loaded character only has 1.5 bits left to be transmitted. In other words, when DRQO gets set, the user may wait (if 8-bit characters) up to 7.5 serial data bits before loading the THR. If THR is not loaded within this time, an Underrun error will occur.

If Auto Flag is not selected (CR20 = logical 0) the sequence will be a little different than described below. When the first DRQO is set, and after the Address character is loaded into THR. a Flag command is also programmed (CR15, 14 = 10).

This will set an interrupt (INTRQ), which indicates that the IR register must be read. Now, the Data Command is reprogrammed (CR15, 14 =00).

For more information, see Transmission Timing diagram.

ABORT CONDITIONS

The function of prematurely terminating a data link is called an "Abort." The transmitting station aborts by sending eight consecutive 1's. Unintentional Abort caused by 1's in the A-C- or I-field is prevented by zero insertion. Intentional Abort may be sent by programming an Abort command. Abort will also be sent in the case where THR is not loaded in time or FCS command is not programmed in time (= underrun). This means that after the DRQO is set, to avoid Abort; THR must be loaded, $\overline{EOB}$ activated or FCS command programmed before there is only 1.5 bits left of the last character to be transmitted.

If this is not done, INTRQ (XMIT OPCOM w/underrun) is set and Aborts are transmitted until, either the command is changed or the THR is loaded. If in this same case, Auto Flag was programmed, one Abort (with INTRQ) would be generated, and thereafter continuous Flags (with no INTRQs) will be sent.

RECEIVER OPERATION

Prior to this operation, the programmable inputs and the receive mode related register bits have to be programmed according to the user's specific data communication environment. Also, the INTRQ has to be cleared. The last bit to be set is always the ACT REC (CR17) bit.

For more detailed information how to program the VL1935 see Programming. As an example, let's assume a 26-bit information is to be received, and the I-field is made up by 8-bit characters. The CR3 register is only for transmit mode, and may be ignored here. CR20 and CR 12-16 bits are also for transmit mode only, and therefore may also be ignored. CR21 and CR22 are to be logical 0s (no Self-Test and no SDLC Loop Mode). CR24, 23 are to be logical 0's (8-bit character I-field). If only one A-field and one C-field character is expected, and this VL1935 has a specific address, CR25 should be a logical 0, CR26 should be a 1, and CR27 should be a 0. The address to which the A-field should compare should be loaded into the AR register.

The status of the modem is monitored by the SR register, and it may be useful to read it at this time. CR1 is loaded as the last register. CR10 (Misc In) bit is optionable to the user. CR11 (DTR) is to be set if modem is used. CR17 (ACT REC) is now set, starting the input of frame characters into the Receiver Register (RR). When a Flag is detected, the next

8-bit character (address-character), when received, is compared to the character in the AR register. If these match, or if the received character is a Global address, this frame is valid, and the DRQI gets set. If the Address Comparator (CR26) bit is not set, all frames would be considered valid and generate DRQIs. When the RHR register is read, DRQI will be reset. All characters in a valid frame which are input into the RR register will set DRQI, and every time RHR is read by the CPU, DRQI will be reset.

During reception, the receiver also performs a CRC calculation on the incoming data. When the end Flag is received, INTRQ will get set, indicating Received End of Message. If the reception is completed with no error, IR7 (REOM w/no Error) bit will be set. When 8-bit characters are received SR 0-2 bits indicate the number of residual bits, in this case two. If IR6 (REOM w/Error) was set, SR 0-2 bits indicate the type of errors (see Receiver Error Indication).

When all characters including the A-field and the FCS-field are read, and when the REOM interrupt is recognized, it is up to the user to disassemble these mentioned characters from the received data. If non-8-bit characters are received, the amount of residual bits have to be calculated by the CPU after masking out the part of the ending Flag showing up in the last read character.

After end of frame, the receiver begins searching for a new frame.

(For more information, see Figure 8.)

RECEIVER ERROR INDICATION

When a frame is received, and REOM w/Error (IR6) is set, the type of error is indicated by the SR bits 0-2.

CRC Error (SR0) If the CRC calculation performed on the incoming data does not equal to F0B8 (HEX), this bit will be set.

Overrun Error (SR1) After DRQI is set, if the RHR is not read within one character minus one bit time, this bit will be set.

Aborted or Invalid Frame Error (SR2) If the frame is aborted or if in a frame the number of bits between flags are less than the required minimum (see Table 10), this bit will be set.

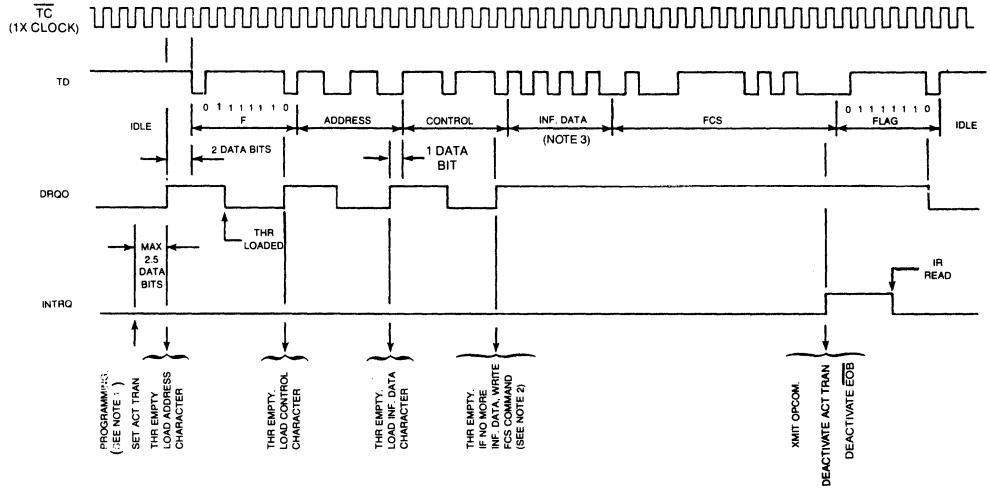
NOTES

1. TC-command—If two or more contiguous ABORTS or FLAGS are executed, the ACT TRAN (CR16) bit has to be reset before DATA-command can be executed.
2. Master Reset ($\overline{MR}$)—Needs no clock during activation of MR. However, 2.5 clock cycles are required to reset the VL1935 after the falling edge of $\overline{MR}$.
3. IR-register—Immediately when IR register is read, bit 0 will reset. Bits 3-7 are reset one bit time later.
4. SR-register—Bits 0-2 are reset one bit time after SR register is read.
5. SDLC Loop mode—Go-ahead pattern may be sent by either sending IDLE or ABORT after Flag.
6. $\overline{TC}$ and $\overline{RC}$ clocks are completely independent of each other.
7. It is recommended to verify that the INTRQ signal (pin 6) is set prior to reading the IR register.
8. End Of Block (EOB) — Minimum activated time must be one (1) character time. It can be activated indefinitely using IDDLE or AUTO FLAG (CR20).

TABLE 10.

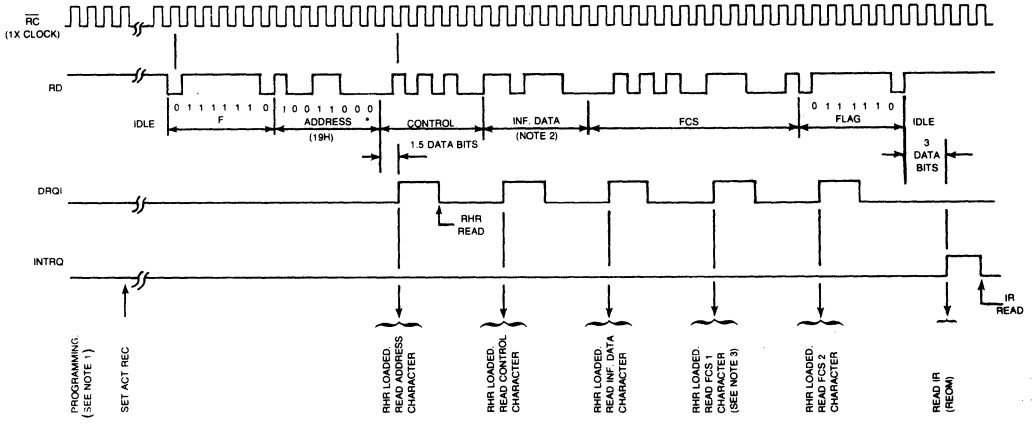
	Valid Frame For VL1935			
Receiver Programmed for	**8 bit char**	**7 bit char**	**6 bit char**	**5 bit char**
1 address, 1 control	≥25 bits	≥23 bits	≥21 bits	≥19 bits
2 addresses, 1 control 1 address, 2 controls	≥25 bits	≥24 bits	≥23 bits	≥22 bits
3 addresses, 1 control 2 addresses, 2 controls	≥25 bits	≥25 bits	≥25 bits	≥25 bits

FIGURE 7. VL1935 TRANSMISSION TIMING DIAGRAM



NOTE 1. CR3 = 00H, CR2 = O1H, CR1 = 02H (FOR THIS EXAMPLE ONLY)
NOTE 2. WRITE FCS COMMAND, OR ACTIVATE $\overline{EOB}$.
NOTE 3. INF. DATA MAY CONSIST OF ANY NUMBER OF BITS.

FIGURE 8. VL1935 RECEPTION TIMING DIAGRAM



NOTE 1. AR = 19H, CR2 = 40H, CR1 = 02H (FOR THIS EXAMPLE ONLY)
NOTE 2. INF. DATA (I-FIELD) MAY CONSIST OF ANY AMOUNT OF BITS.
NOTE 3. CPU DOES NOT KNOW UNTIL RECEIVED END OF MESSAGE (REOM) THAT THIS IS AN FCS CHARACTER.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Storage Temperature	−55°C to +125°C (plastic package)
Storage Temperature	−65°C to +150°C (ceramic package)
Voltage on any pin with respect to GND (V_{SS})	−0.3 to +7.0 V
Power Dissipation	1W

DC Characteristics

T_A = 0°C to +70° V_{SS} = 0 V, V_{CC} = +5 ± 0.25 V

TABLE 11. VL1935 DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{LI}	Input Leakage			10	μA	VIN = V_{CC}
I_{LO}	Output Leakage			10	μA	V_{OUT} = V_{CC} or V_{SS}
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage			0.8	V	All Inputs
V_{OH}	Output High Voltage	2.4			V	I_O = −100μA
V_{OL}	Output Low Voltage			0.4	V	I_O = 1.6mA
I_{CC}	Supply Current		70	210	ma	

AC Characteristics

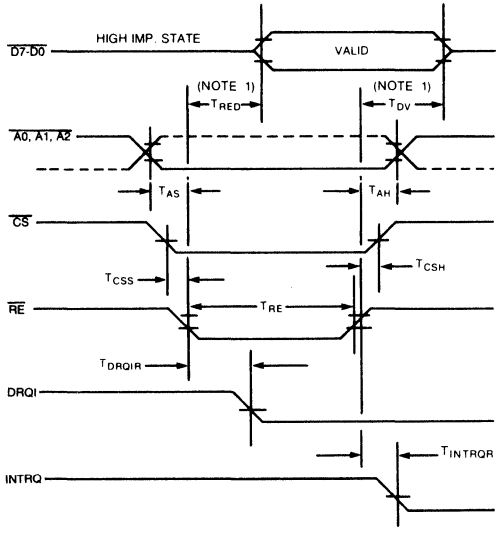
T_A = 0°C to +70° V_{SS} = 0 V, V_{CC} = +5 ± 0.25 V

TABLE 12. VL1935 AC CHARACTERISTICS

		−10		−11		−12		−13			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Units	Conditions
	READ & WRITE (Fig. 9, 10)										
T_{AS}	Address Set-Up	20		20		20		20		ns	
T_{AH}	Address Hold	20		20		20		20		ns	
T_{CSS}	Chip Select Set-up	20		20		20		20		ns	
T_{CSH}	Chip Select Hold	20		20		20		20		ns	
	READ (Fig. 9)										
T_{RED}	Data Delay from $\overline{RE}$ Asserted		315		290		265		240	ns	
T_{DV}	Date Valid from $\overline{RE}$ Deasserted	0	140	0	140	0	140	0	140	ns	
T_{DRQIR}	DRQI Reset Delay		280		280		280		280	ns	
T_{INTRQR}	INTRQ Reset Delay		280		280		280		280	ns	
T_{RE}	$\overline{RE}$ Pulse width	325		300		275		250		ns	
	WRITE (Fig. 10)										
T_{DS}	Data Set-up	200		180		160		140		ns	
T_{DH}	Data Hold	20		20		20		20		ns	
T_{DRQOR}	DRQO Reset Delay		330		330		330		330	ns	
T_{WE}	$\overline{WE}$ Pulse width	200		180		160		140			
	TRANSMIT& RECEIVE (Fig.11)										
T_{RDS}	Receive Data Set Up	150		150		150		150		ns	
T_{RDH}	Receive Data Hold	150		150		150		150		ns	
T_{TDO}	Transmit Data Out Delay		125		125		125		125	ns	
	CLOCK										
$1xF_C$	1X Clock		.5		1.0		1.5		2.0	MH_Z	at 50% duty cycle
$32xF_C$	32X Clock		1.0		1.5		2.0		2.5	MH_Z	at 50% duty cycle
	RISE & FALL (Fig. 12)										
T_R	Rise Time		20		20		20		20	ns	See figure 1
T_F	Fall Time		20		20		20		20	ns	

NOTE: All A.C. Timing Measurements made at 0.8 V and 2.0 V.

FIGURE 9. VL1935 READ TIMING DIAGRAM



NOTE 1. T_{RED} and T_{DV} starts from where both $\overline{CS}$ and $\overline{RE}$ are active.

FIGURE 10. VL1935 WRITE TIMING DIAGRAM

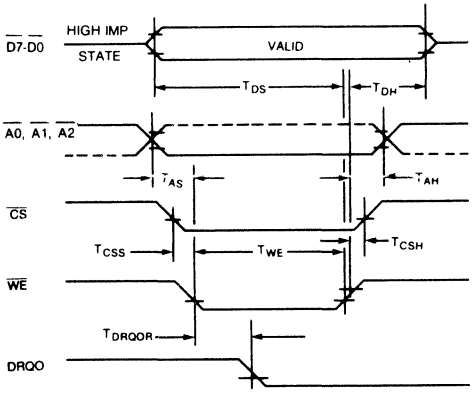


FIGURE 11. RECEIVER AND TRANSMITTER TIMING

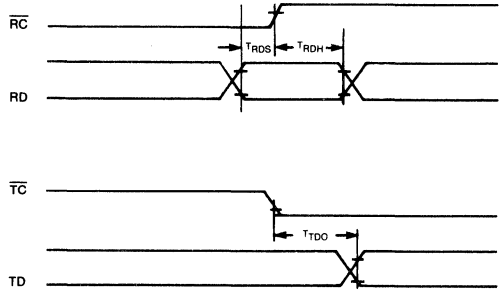


FIGURE 12. VL1935 RISE AND FALL TIMING DIAGRAM

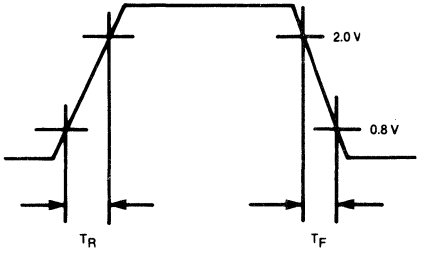


FIGURE 13. VL1935 TRANSMITTER FLOW CHART

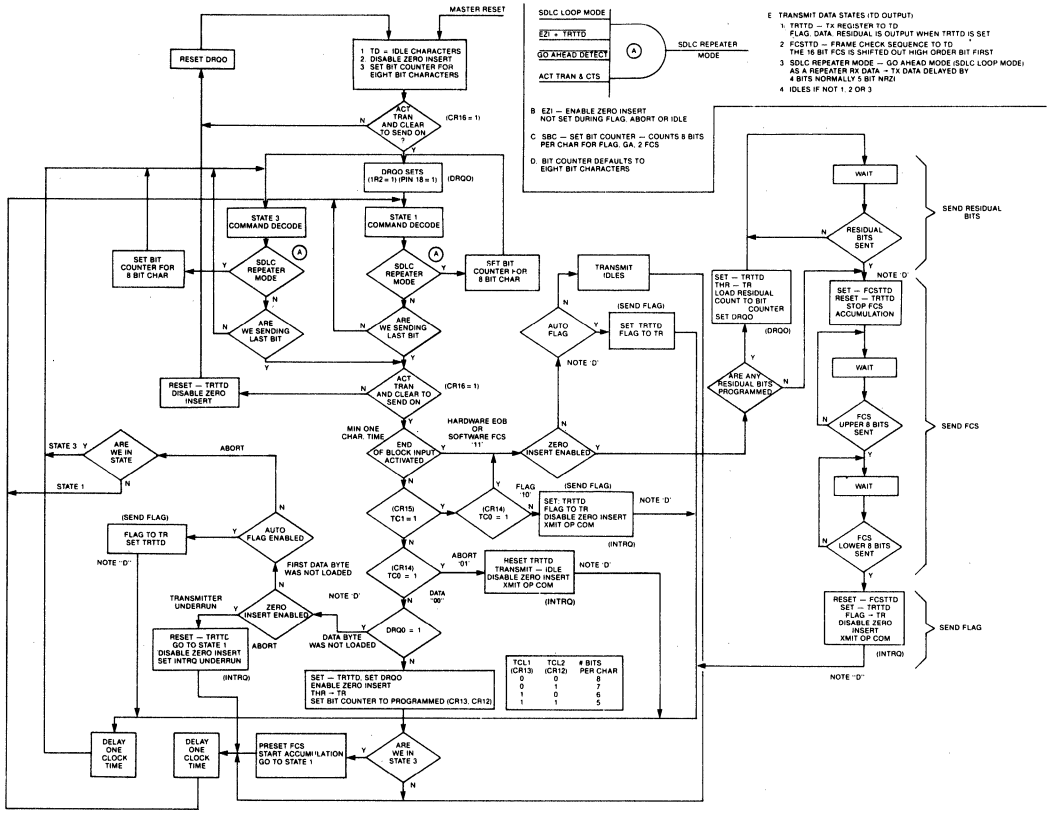
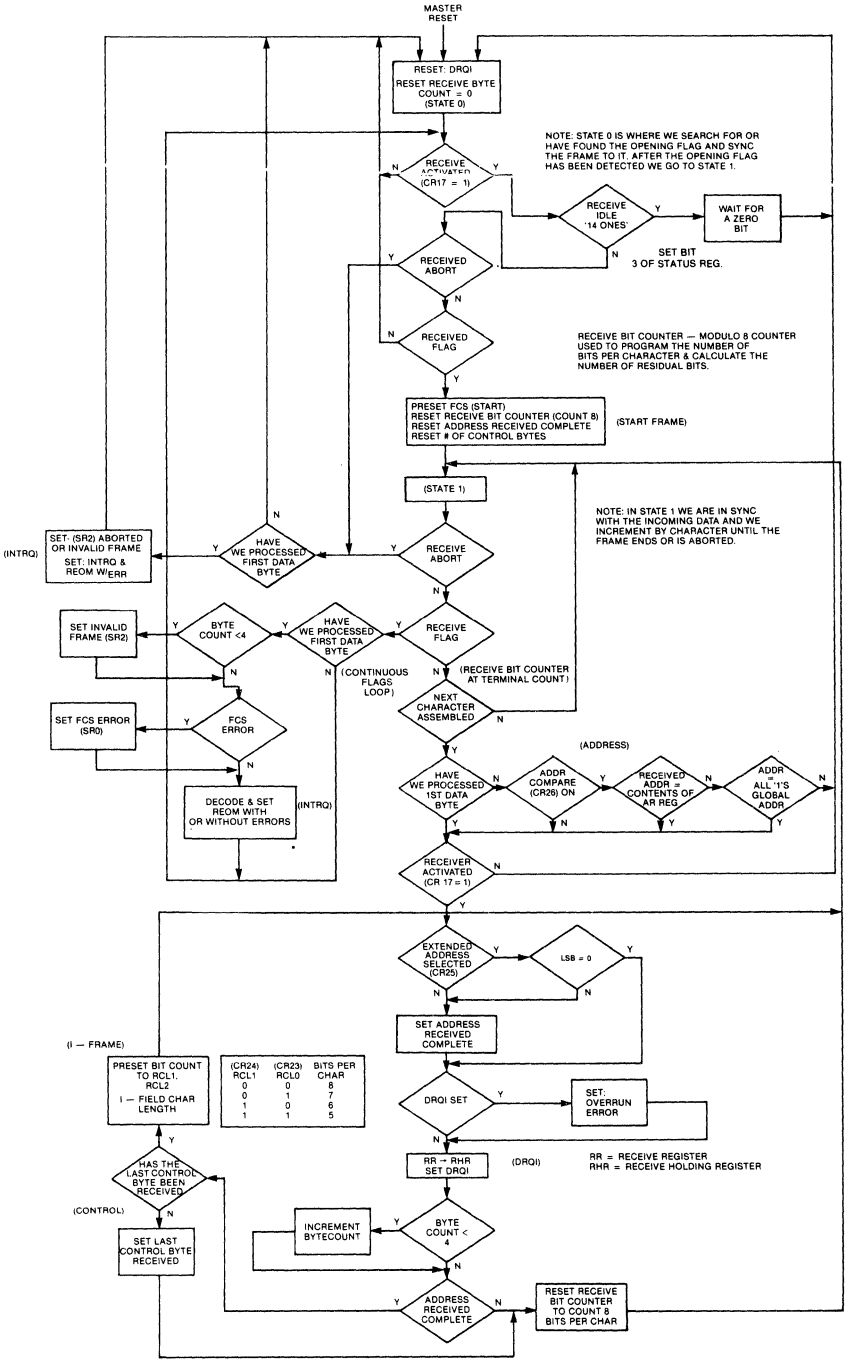


FIGURE 14. VL1935 RECEIVER FLOW CHART



VL2661

ENHANCED PROGRAMMABLE COMMUNICATIONS INTERFACE

FEATURES

SYNCHRONOUS OPERATION

- 5- to 8-bit characters plus parity
- Internal or external character synchronization
- Odd, even or no parity
- Local or remote maintenance loop back mode
- Baud rate: DC to 1 Mbps (1x clock)

ASYNCHRONOUS OPERATION

- 5- to 8-bit characters plus parity
- 1-, 1 1/2- or 2-stop bits transmitted
- Parity, overrun and framing error detection
- Line break detection and generation
- Local or remote maintenance loop back mode
- Baud rate: DC to 1 M bps (1x clock) —DC to 15.625 K bps (64x clock)

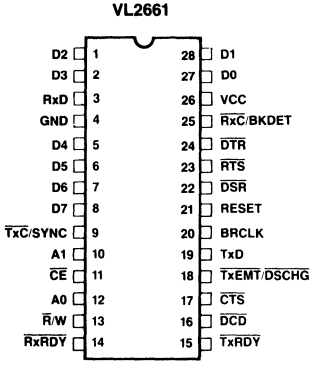
OTHER FEATURES

- 16 internal rates for each set
- Double-buffered transmitter and receiver
- Dynamic character length switching

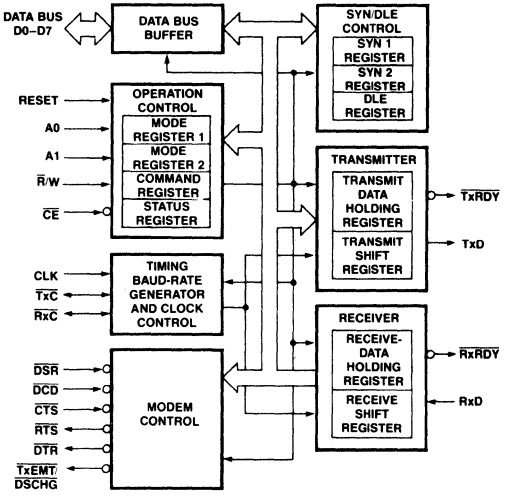
DESCRIPTION

The VL2661 Enhanced Programmable Communications Interface (EPCI) is a programmable microprocessor peripheral which provides a bidirectional interface for data interchange. It contains interface logic for simultaneously transmitting and receiving standard synchronous communications, and provides the data formatting and control to interface serial asynchronous communication with bus-organized systems.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Maximum Baud Rate	Clock Frequency	Package
VL2661-01PC VL2661-01CC VL2661-01QC	19.2 K	4.9152 MHz	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)
VL2661-02PC VL2661-02CC VL2661-02QC	38.4 K		Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)
VL2661-03PC VL2661-03CC VL2661-03QC	19.2 K	5.0688 MHz	Plastic DIP Ceramic DIP Plastic Leaded Chip Carrier (PLCC)

Note:
Operating temperature range: 0°C to +70°C.

PIN DESCRIPTIONS

Pin	Pin Number	Name	Description
CPU Interface			
RESET	21	Reset	Input signal that, when HIGH, performs a master reset of the VL2661. This signal asynchronously terminates any device activity and clears the mode, command and status registers. The VL2661 assumes the idle state and remains there until initialized with appropriate control words.
A0,A1	10,12	Address Lines	Address input lines used to select the internal registers.
$\overline{R}$/W	13	$\overline{Read}$/Write	Input signal that controls the direction of data transfers between the EPCI and the CPU. When CE and $\overline{R}$/W are both LOW, the contents of the selected registers are transferred to the data bus. With $\overline{CE}$ LOW and $\overline{R}$/W HIGH, a write to the select register is performed.
$\overline{CE}$	11	Chip Enable	Input signal that, when LOW, Allows access to the selected register. When HIGH the D0-D7 lines are placed in the HIGH-impedance state.
D0-D7	27,28, 1,2,5-8	Data Bus	Bidirectional 8-bit, 3-state, positive-true data bus used to transfer commands, data and status between the EPCI and the CPU.
$\overline{TxRDY}$	15	Transmitter	Output signal that is the complement of the Status Register (SR) bit SRO. When LOW, this signal indicates that the transmit data holding register (TxHR) is ready to accept a data character from the CPU. It goes HIGH when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open-drain output that can be wire-ORed to the CPU interrupt.
$\overline{RxRDY}$	14	Receiver Ready	Output signal is the complement of Status Register (SR) bit. When LOW, this signal indicates that the receive data holding register (RxHR) has a character ready for input to the CPU. It goes HIGH when the RxHR is read by the CPU and also when the receiver is disabled. It is an open-drain output which can be wire-ORed to the CPU interrupt line.
$\overline{TxEMT}$/ $\overline{DSCHG}$	18	Transmitter Empty/Data Set Change	Output signal that is the complement of the Status Register (SR) bit. When LOW, this signal indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. This signal goes HIGH when the status register is read by the CPU if the TxEMT condition does not exist. Otherwise, the TxHR must be loaded by the CPU for this line to go to HIGH. It is an open-drain output that can be wire OR-ed to the CPU interrupt line.
Transmitter/Receiver Signals			
BRLCK	20	Baud Rate Clock	Clock input to the internal baud rate generator. This is not required when external receiver and transmitter clocks are used.
$\overline{RXC}$/ BKDET	25	Receiver Clock/Break Detect	Bidirectional line that either controls character receive rate or provides a timing output. When the EPCI is programmed for external receiver clock, this pin acts as an input to control the rate at which characters are received. The frequency is programmed in Mode Register 1 and may be 1x, 16x or 64x the baud rate. Data is sampled on the rising edge. If internal receiver clock is programmed, this signal provides an output, either a 1x/16x clock or break detect signal, determined by programming Mode Register 2.
$\overline{TxC}$/ XSYNC	9	Transmitter Clock/ External Sync	Bidirectional line that controls the character transmit rate and provides a timing output. When the EPCI is programmed for external transmitter clock, this signal acts as an input and controls the rate at which the characters are transmitted. The frequency is programmed in Mode Register 1 and be may 1x, 16x or 64x the baud rate. Data changes on the falling edge of this clock. If the EPCI is programmed for internal transmitter clock, this signal can be either an output providing a 1x/16x clock or an input for external synchronization determined by Mode Register 2 programming.

PIN DESCRIPTIONS (Cont.)

Pin	Pin Number	Name	Description
Transmitter/Receiver Signals (Cont.)			
RxD	3	Receive Data	Serial data input to the receiver.
TxD	19	Transmit Data	Serial data output from the transmitter. When the transmitter is disabled, the output is in the HIGH, or "Mark", state.
$\overline{DSR}$	22	Data Set Ready	Input signal that can be used to indicate Data Set Ready or Ring Indicator to the EPCI. Its complement appears in the Status Register as bit 7. A change of state on DSR causes $\overline{TxEMT/DSCHG}$ to go LOW if either Command Register (CR) bit 0 or 2 is a one.
$\overline{DCD}$	16	Data Carrier Dectect	Input signal that must be LOW for the receiver to operate. If $\overline{DCD}$ goes HIGH while receiving, the RxC signal is internally inhibitied. The complement of $\overline{DCD}$ appears in the Status Register (SR) as bit 6. A change of state in $\overline{DCD}$ causes $\overline{TxEMT/DSCHG}$ to go LOW if either Command Register (CR) bit 0 or 2 is a one.
$\overline{CTS}$	17	Clear to Send	Input signal that must be LOW fpr transmitter to operate. If $\overline{CTS}$ goes HIGH while transmitting, the character currently in the transmit shift register is transmitted before termination. The TxD output will then go HIGH.
$\overline{DTR}$	24	Data Terminal Ready	Output signal that is the complement of Command Register (CR) bit 1. This signal is normally used to indicate that the data terminal is ready to transmit or receive data.
$\overline{RTS}$	23	Request to Send	Output signal that is the complement of Command Register (CR) bit 5. If the transmit shift register is not empty when bit 5 is reset, $\overline{RTS}$ will not go HIGH until one $\overline{TxC}$ period after the last serial bit is transmitted.
Power Supply			
VCC	26	Supply	5 V Supply
GND	4	Ground	Supply and Signal Ground

TABLE 1: BAUD RATE GENERATOR CHARACTERISTICS VL2661-01 (BRCLK = 4.9152 MHz)

MR 2				Baud Rate	Actual Frequency 16X Clock (KHz)	Percent Error	Divisor
3	2	1	0				
0	0	0	0	50	0.8	—	6144
0	0	0	1	75	1.2	—	4096
0	0	1	0	110	1.7598	-0.01	2793
0	0	1	1	134.5	2.152	—	2284
0	1	0	0	150	2.4	—	2048
0	1	0	1	200	3.2	—	1536
0	1	1	0	300	4.8	—	1024
0	1	1	1	600	9.6	—	512
1	0	0	0	1050	16.8329	0.196	292
1	0	0	1	1200	19.2	—	256
1	0	1	0	1800	28.7438	-0.19	171
1	0	1	1	2000	31.9168	-0.26	154
1	1	0	0	2400	38.4	—	128
1	1	0	1	4800	76.8	—	64
1	1	1	0	9600	153.6	—	32
1	1	1	1	19200	307.2	—	16

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		−0.3 V +7.0 V
Input/Output Voltage		−0.3 V +7.0 V
Operating Temperature	Top	0°C to 70°C
Storage Temperature	TSTG	−55°C +150°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum conditions for extended periods may affect device reliability.

DC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5.0 V ± 5%, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit
VIH	Input HIGH Voltage	2.0		VCC	V
VIL	Input LOW Voltage			0.8	V
IIN	Input Leakage Current			10	μA
ITSI	Input Leakage Current for HIGH-Impedance State			10	μA
VOH	Output HIGH Voltage, ILOAD = −400 μA	2.4			V
VOL	Output LOW Voltage, ILOAD = 2.2 mA			0.4	V
CI	Input Capacitance, fc = 1 MHz			20	pF
CO	Output Capacitance			20	pF
PD	Power Dissipation, VCC = 5.25 V			650	mW

RECEIVER/TRANSMITTER TIMING CHARACTERISTICS TA = 0°C to 70°C, VCC = 5.0 V ± 5%, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit
tR/TH	$\overline{TxC}$ or $\overline{RxC}$ HIGH	500			ns
tR/T1	$\overline{TxC}$ or $\overline{RxC}$ LOW	500		1.0	ns
fR/T	$\overline{TxC}$ or $\overline{RxC}$ Frequency	DC		1.0	MHz
tBRH	BRCLK HIGH	70			ns
tBRL	BRCLK LOW	70			ns
fBRG	BRCLK Frequency, Note 1		4.9152		MHz
tRxS	RxD Setup	300			ns
tRxH	RxD Hold	350			ns
tTxD	TxD Delay from $\overline{TxC}$, CL = 150 pF			650	ns
tTCS	Skew TxD vs $\overline{TxC}$, CL = 150 pF		0		ns

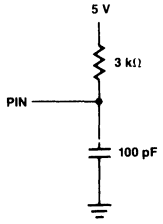
READ/WRITE TIMING CHARACTERISTICS TA = 0°C to 70°C, VCC = 5.0 V ± 5%, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit
tCE	$\overline{CE}$ Pulse Width	250			ns
tCED	$\overline{CE}$ to CE Delay	600			ns
tSET	Address and $\overline{R}$/W Setup	10			—
tHLD	Address and $\overline{R}$/W Hold	10			ns
tDS	Write Data Setup	150			ns
tDH	Write Data Hold	0			ns
tDD	Read Data Delay, CL = 150 pF			200	ns
tDF	Read Data Hold, CL = 150 pF	10		100	ns

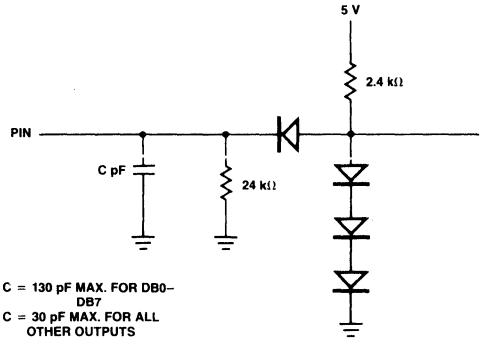
Note:
1. fBRG = 4.9152 MHz for VL2661-1 and -2; fBRG = 5.0688 MHz for VL2661-3

AC TEST CIRCUITS

OPEN-COLLECTOR TEST LOAD

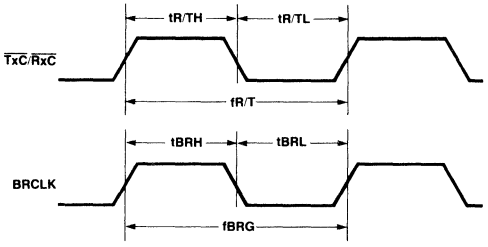


TEST LOAD (ALL OTHER PINS)

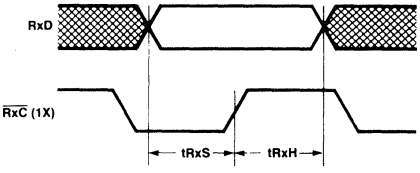


TIMING DIAGRAMS

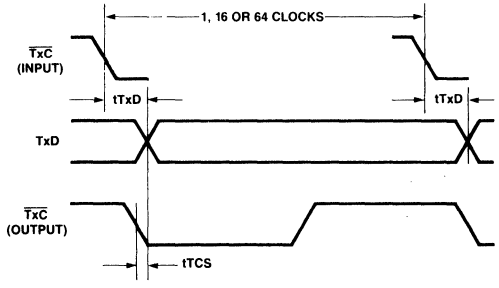
CLOCK TIMING



RECEIVE TIMING



TRANSMIT TIMING



CPU INTERFACE

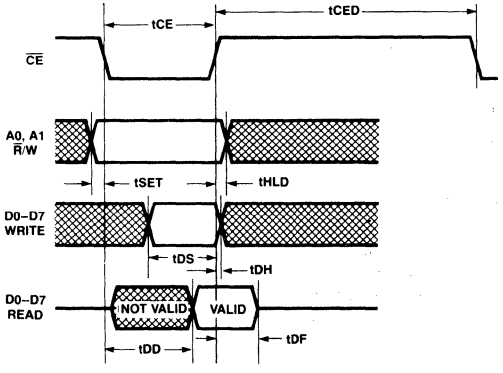


TABLE 1: BAUD RATE GENERATOR CHARACTERISTICS (Cont.)

VL2661-02 (BRCLK = 4.9152 MHz)

MR 2				Baud Rate	Actual Frequency 16X Clock (KHz)	Percent Error	Divisor
3	2	1	0				
0	0	0	0	45.5	0.7279	0.005	6752
0	0	0	1	50	0.8	—	6144
0	0	1	0	75	1.2	—	4096
0	0	1	1	110	1.7598	-0.01	2793
0	1	0	0	134.5	2.152	—	2284
0	1	0	1	150	2.4	—	2048
0	1	1	0	300	4.8	—	1024
0	1	1	1	600	9.6	—	512
1	0	0	0	1200	19.2	—	256
1	0	0	1	1800	28.7438	-0.19	171
1	0	1	0	2000	31.9168	-0.26	154
1	0	1	1	2400	38.4	—	128
1	1	0	0	4800	76.8	—	64
1	1	0	1	9600	153.6	—	32
1	1	1	0	19200	307.2	—	16
1	1	1	1	38400	614.4	—	8

VL2661-03 (BRCLK = 5.0688 MHz)

MR 2				Baud Rate	Actual Frequency 16X Clock (KHz)	Percent Error	Divisor
3	2	1	0				
0	0	0	0	50	0.8	—	6336
0	0	0	1	75	1.2	—	4224
0	0	1	0	110	1.76	—	2880
0	0	1	1	134.5	2.1523	0.016	2355
0	1	0	0	150	2.4	—	2112
0	1	0	1	300	4.8	—	1056
0	1	1	0	600	9.6	—	528
0	1	1	1	1200	19.2	—	264
1	0	0	0	1800	28.8	—	176
1	0	0	1	2000	32.081	0.253	158
1	0	1	0	2400	38.4	—	132
1	0	1	1	3600	57.6	—	88
1	1	0	0	4800	76.8	—	66
1	1	0	1	7200	115.2	—	44
1	1	1	0	9600	153.6	—	33
1	1	1	1	19200	316.8	3.125	16

Note: 16X CLK is used in asynchronous mode. In synchronous mode, clock multiplier is 1X and BRG can be used only for TxC.

FUNCTIONAL DESCRIPTION

The internal organization of the VL2661 EPCI consists of six major functional blocks (See Block Diagram): transmitter; receiver; clock control; modem control; and SYN/DLE control. These blocks communicate internally over common data and control buses. The data bus is also linked to the CPU via a bidirectional 3-state interface.

TRANSMITTER

The transmitter receives parallel data from the CPU and converts it to a serial bit stream, inserting start, stop and parity bits as selected by the user. It outputs a composite serial data stream.

RECEIVER

The receiver accepts serial data from the sending device and converts it to a parallel format, checking for appropriate start, stop and parity bits and control characters, as selected by the user. It sends the assembled character to the CPU.

TIMING CONTROL

The timing control block contains a programmable baud rate generator (BRG). The BRG accepts external transmit ($\overline{TxC}$) or receive ($\overline{RxC}$) clocks to divide an external baud rate clock (BRCLK) for controlling data transfers. The BRCLK input allows the user to program one of 16 commonly used baud rates.

OPERATION CONTROL

The operation control block contains four registers: Mode Registers 1 and 2 (MR1,MR2); the Command Register (CR); and the Status Register (SR). These registers are used to store configurations and operation commands from the CPU. They generate the necessary internal control signals for proper device operation, and maintain status information for the CPU.

MODEM CONTROL
The modem control section provides interfacing for three input signals and three output signals that are used for "handshaking" and status indication between the CPU and a modem.

SYN/DLE CONTROL
This section contains control circuitry and three 8-bit registers storing the SYN2, and DLE character provided by the CPU. Each register is used in the synchronous operation mode to provide the characters required for synchronization, idle fill and data transparency.

OPERATION
The EPCI's operation is determined by programming the mode and command registers. Baud rate, asynchronous or synchronous communication, and SYN characters are established before enabling the transmitter or receiver.

ASYNCHRONOUS RECEIVER OPERATION
After the Mode Registers are configured, the receiver is enabled when the receiver enable (RxEN) bit of the command register (bit 2) is set to a one and $\overline{DCD}$ is LOW. With the receiver enabled, the EPCI then monitors the RxD input, waiting for a HIGH-to-LOW transition. When a transition is detected, the RxD input is again sampled one-half-bit-time later. If RxD is HIGH at that time, a search for a valid start bit is started again. If, however, RxD is still LOW a valid start bit is assumed and the receiver continues to sample the RxD input at one-bit-time intervals until the correct number of data bits, the parity bit and one stop bit have been assembled. The character is then transferred to the receive data holding register (RxHR), the $\overline{RxRDY}$ bit of the Status Register (bit 1) is set, and the $\overline{RxRDY}$ output goes LOW. If the character length is less than 8 bits, the high-order unused bits in the holding register are set to zero. The parity error, framing error and overrun error status bits are strobed into the Status Register on the positive-going edge of RxC, corresponding to the received character boundary (Figures 1 and 2).

If the stop bit is present, the receiver immediately begins its search for the next start bit. If the stop bit is absent (framing error), the receiver interprets it as a space bit if it persists into the next bit time interval. If a break condition is detected (RxD is LOW for the entire character as well as the stop bit), only one character, consisting of all zeros (with the framing error status bit set), will be transferred to the holding register. The RxD input must go HIGH before a search for the next start bit begins (Figure 3).

Pin 25 can be programmed as a Break Detect (BKDET) output by setting bits 4 and 7 of Mode Register 2 (MR2). When these bits are set and a break is detected, the BKDET output will go HIGH. If RxD returns HIGH for at least one RxD time, BKDET returns LOW.

SYNCHRONOUS RECEIVER OPERATION
When the EPCI is programmed for synchronous operation the receiver will remain idle until the receiver enable bit (bit 2) is set. At that time, the EPCI enters the hunt mode. Data is shifted into the receive data shift register (RxSR) one bit at a time. The contents of RxSR are then compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly mode begins.

If the single-SYN operation is programmed, the SYN DETECT bit of the Status Register (bit 5) is set. If double-SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise, the EPCI returns to the hunt mode. (Note that the sequence SYN1-SYN2 does not achieve synchronization).

When synchronization has been achieved, the EPCI continues to assemble characters and transfer them to the holding register, setting the Status Register RxRDY bit and asserting the $\overline{RxRDY}$ each time a character is transferred. The parity error (PE) and overrun error (OE) status register bits are set as appropriate. Further receipt of the appropriate SYN sequence sets the SYN DETECT Status Register bit. If the SYN stripping mode is set, SYN characters are not transferred to the holding register. (Note that the SYN characters used to establish initial synchronization are not transferred to the holding register in any case.)

By setting MR2 bit 4 and MR2 bit 7 to one, pin 9 ($\overline{TxC}$/XSYNC) can be programmed as an external jam synchronization input. When XSYNC is selected, internal SYN1, SYN1-SYN2 and DLE-SYN1 detection is disabled. Each positive-going signal on XSYNC causes the receiver to establish synchronization on the rising edge of the next $\overline{RxC}$ pulse. Character assembly starts with the RxD input at this edge. XSYNC must be prior to the next rising edge of $\overline{RxC}$. This external synchronization causes the SYN DETECT Status Register bit to be set until the Status Register is read.

ASYNCHRONOUS TRANSMITTER OPERATION
When the EPCI is programmed to transmit to the CPU, the transmitter remains idle until $\overline{CTS}$ is LOW and the transmitter enable (TxEN) bit of the Command Register (bit 0 is set. The EPCI responds by setting SR bit 0 and asserting the $\overline{TxRDY}$ output. When the CPU writes a character into the transmit data holding register (TxHR), SR bit 0 is reset and $\overline{TxRDY}$ returns HIGH. The character is then transferred to the transmit shift register (Tx SR) when it is idle or has completed transmission of the previous character. Status Register bit 0 is set again and $\overline{TxRDY}$ goes LOW (Figure 9).

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, with the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the transmit holding register, the TxD output remains in the mark (HIGH) condition and the $\overline{TxEMT}$/DSCHG output and its corresponding status bit are asserted. Transmission resumes when the CPU loads a new character into the holding register. The transmitter can be forced to ouput a continuous LOW (Break) condition by setting CR bit 3.

TIMING DIAGRAMS

FIGURE 1: RECEIVER OPERATION TIMING DIAGRAM

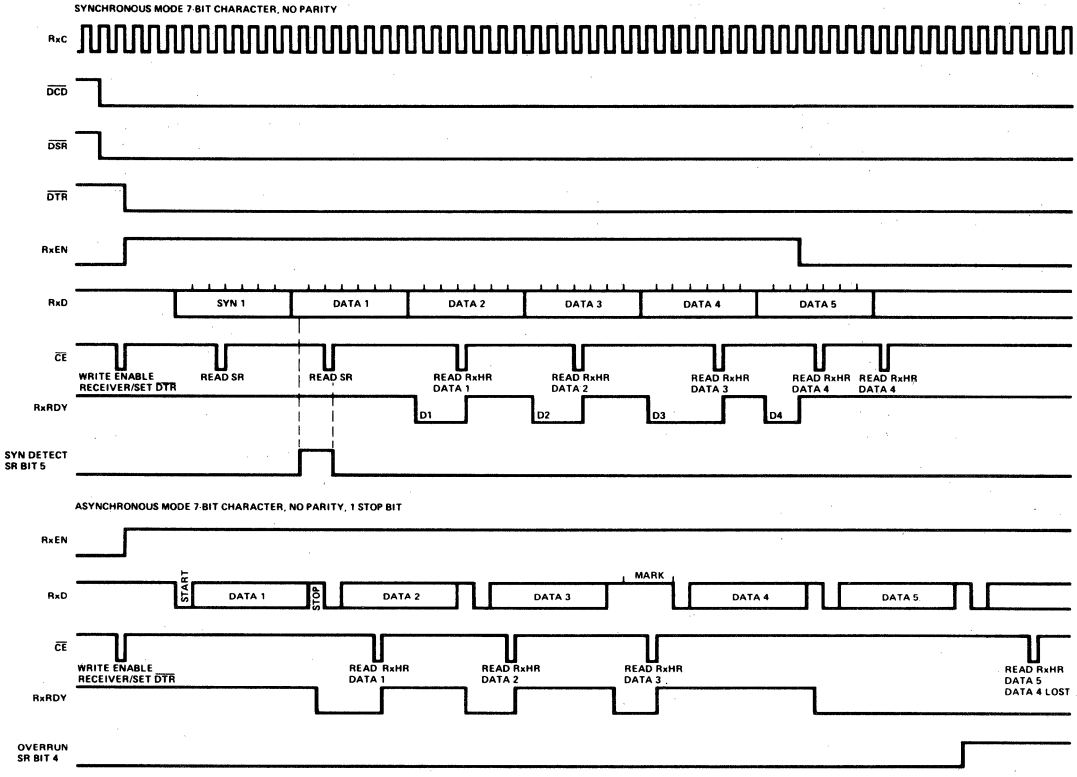
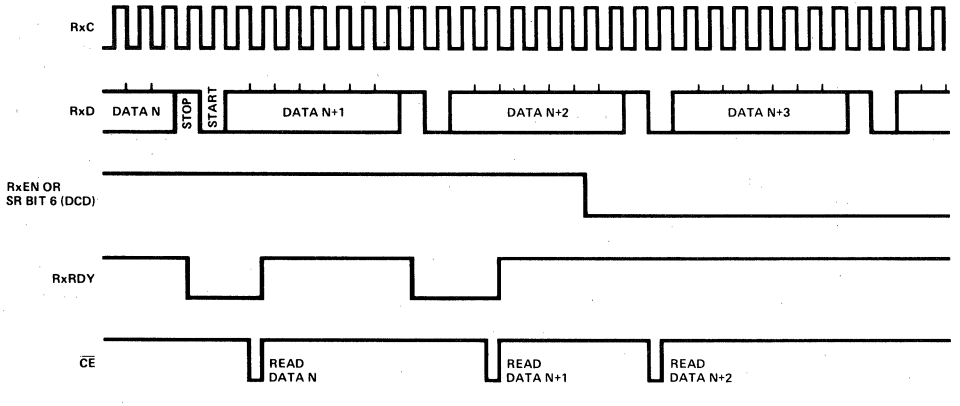


FIGURE 2: ASYNCHRONOUS RECEIVER OPERATION WITH LOSS OF DCD OR DISABLING RxEN



SYNCHRONOUS TRANSMITTER OPERATION

When the EPCI is initially programmed for synchronous transmission, it remains in the idle state (RxD HIGH) until TxEN is set. At this point, TxD remains HIGH and $\overline{\text{TxRDY}}$ goes LOW. Both remain in this state until the first character (usually a SYN character) is written into the TxHR. This starts transmission, with $\overline{\text{TxRDY}}$ going LOW each time a character is shifted from the TxSR. If $\overline{\text{TxRDY}}$ is not serviced before the previous character is shifted out of the TxSR, the $\overline{\text{TxEMT}}$ output goes LOW and the EPCI automatically fills the pending gap with SYN1, SYN1, SYN2 doublets or DLE-SYN1 doublets, depending upon the state of MR1 bit 6 and MR1 bit 7. Transmission is continuous until TxEN is reset to zero.

If the send DLE bit (CR bit 3) is set, the DLE character is automatically transmitted prior to the transmission of any character stored in the TxHR. Since this is a one-time command, CR bit 3 does not have to be reset.

VL2661 EPCI PROGRAMMING

Before data communications can begin, the EPCI must be programmed by writing to its Mode and Command Registers. Additionally, if synchronous communication has been selected, the appropriate SYN1, SYN2 and DLE registers must be loaded. Table 2 describes the register addressing requirements, and Figure 4 illustrates the initialization process.

In Table 2 MR1 and MR2 appear to have the same address. The EPCI has an internal pointer that initially directs the first read or write to MR1. On the next access at that same address, the pointer directs the operation to MR2. A similar sequence occurs for the SYN and DLE registers; first SYN1, then SYN2, then DLE. If more than the required number of accesses is made, the internal pointer resets to the first register. The pointer is also reset to MR1 and SYN1 by a RESET input or a read of the Command Register. It is, however, unaffected by any other read or write operation.

REGISTER FORMATS

The register formats are illustrated in Figures 5 through 8. The Mode Registers (MR1 and MR2) define general operating characteristics and the Command Register (CR) controls the basic operation defined by MR1 and MR2. The status register indicates the EPCI operating status and the condition of external inputs. These registers are cleared by a RESET input (SR bit 6 and SR bit 7 excepted).

MODE REGISTER 1 (MR1)

Mode register/bits 0 and 1 select the communication mode and baud rate multiplier (Figure 5). In asynchronous mode the multiplier applies only if the external input option is selected by MR2 bit 4 and MR2 bit 5.

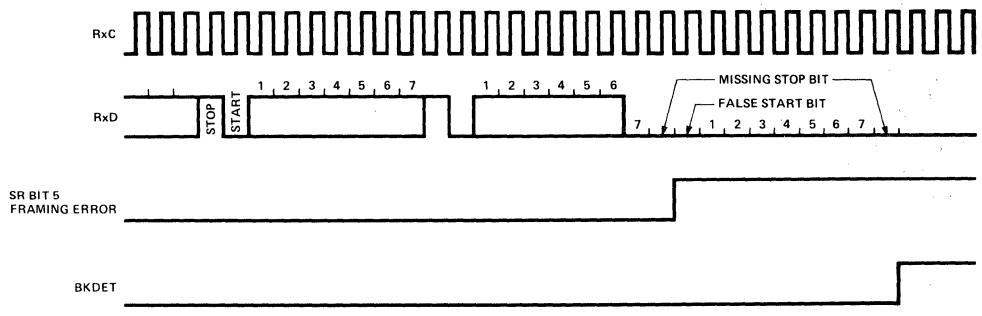
Bits 2 and 3 of MR1 select character length. When selected, character length does not include the parity bit, and does not include the start and stop bits in asynchronous operation.

When set, MR1 bit 4 selects parity. A parity bit is transmitted with each character, and a parity check is performed on each character received.

Bit 5 of MR1 selects either odd or even parity. In asynchronous mode, MR1 bits 6 and 7 select the number of stop bits: 1, 1.5 or 2. If a 1x baud rate is programmed, 1.5 stop bits defaults to 1 on transmit. In the synchronous mode, bit 7 of MR1 controls the number of SYN characters used to establish synchronization, and the number of fill characters to be transmitted when $\overline{\text{TxRDY}}$ and $\overline{\text{TxEMT}}$ are zero. Bit 6 of MR1 controls selection of the transparent mode. When MR1 bit 6 is set (transparent selected), DLE-SYN1 is used for character fill and SYN detect (SR bit 5), but the normal synchronization sequence is used to establish character sync. When transmitting in the synchronous transparent mode, a DLE character in TxHR causes a second DLE character to be transmitted. If the send DLE command (CR bit 3) is active when a DLE character is in the TxHR, only one additional DLE is transmitted.

The bits in the Mode Register affecting character assembly and disassembly (MR1 bit 2-MR1 bit 6) can be changed dynamically (during active receive/transmit operation). The character Mode Register affects both the transmitter and receiver; therefore, in synchronous mode, changes should be made only in half-duplex mode (RxEN OR TxEN HIGH (logical one), but not both simultaneously). In asynchronous

FIGURE 3: FRAMING ERROR AND BREAK DETECTION TIMING



mode, character changes should be made when RxEN and TxEN are zero or when TxEN is one and the transmitter is marking in half-duplex mode (RxEN is zero).

To effect assembly/disassembly of the next received/transmitted character, MR1 bits 2 through 5 must be changed within n bit times of the active-going state of $\overline{RxRDY}/\overline{TxRDY}$. Transparent and non-transparent mode changes must occur within n-1 bit times of the character to be affected when the receiver or transmitter is active. (n is the smaller of the new and old character lengths).

MODE REGISTER 2 (MR2)

Mode Register 2 bits 0 through 3 select the internal baud rate generator (BRG) (Figure 6). There are sixteen selectable rates for each version (Table 1).

Bits 4 through 7 of MR2 define the receive and transmit clock source and the function of pins 9 ($\overline{TxC}$/SYNC) and 25 ($\overline{RxC}$/BKDET).

COMMAND REGISTER (CR)

Command register bit 0 enables or disables the transmitter (Figure 7). When TxEN is a zero, $\overline{TxRDY}$ and $\overline{TxEMT}$ are both HIGH, the transmitter is disabled. When TxEN goes active, $\overline{TxRDY}$ goes LOW, requesting the first character to be written to the TxHR, and the TxD output is enabled to transmit. When TxEN goes inactive, the EPCI completes transmission of any character still in the TxSR. TxD then goes to the marking state and $\overline{TxRDY}$ and $\overline{TxEMT}$ go HIGH. (Refer to Figure 9). Bit 1 of the CR controls the $\overline{DTR}$ output, which is a logical complement of CR bit 1.

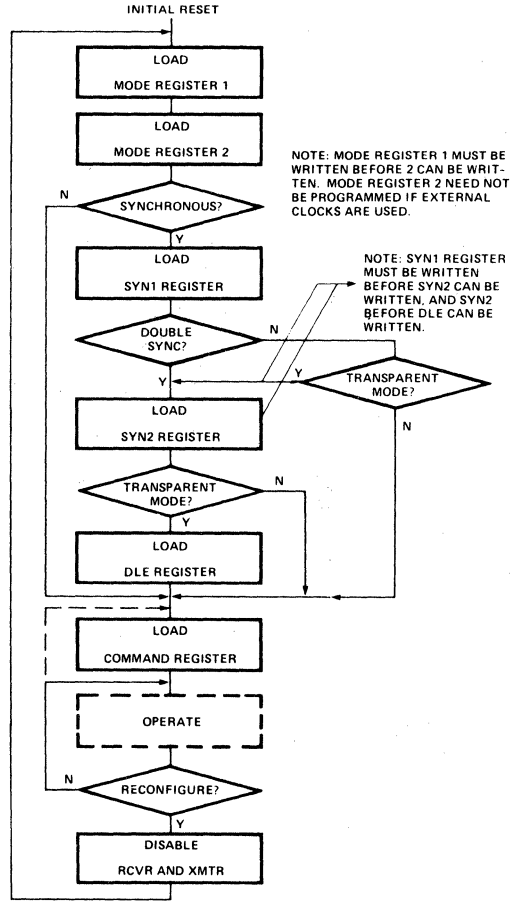
Bit 2 of the command register enables or disables the receiver. When RxEN is a zero, the receiver is in an idle mode with $\overline{RxRDY}$ HIGH. A zero-to-one transition of RxEN initiates a start bit search in asynchronous mode or initiate the hunt mode in synchronous transmission. A one-to-zero transition of RxEN immediately terminates receiver operation.

In the asynchronous mode, setting CR bit 3 forces the TxD output LOW (break condition) at the end of the current transmitted character. TxD remains LOW until CR bit 3 is cleared, at which time TxD goes HIGH for a minimum

TABLE 2: VL2661 REGISTER ADDRESSING

$\overline{CE}$	A_1	A_0	$\overline{R}/W$	Function
1	X	X	X	Three-state Data Bus
0	0	0	0	Read Receive Holding Register (RxHR)
0	0	0	1	Write Transmit Holding Register (TxHR)
0	0	1	0	Read Status Register (SR)
0	0	1	1	Write SYN1/SYN2/DLE Registers
0	1	0	0	Read Mode Registers (MR1, MR1/MR2)
0	1	0	1	Write Mode Registers (MR1, MR1/MR2)
0	1	1	0	Read Command Register
0	1	1	1	Write Command Register

FIGURE 4: INITIALIZATION FLOWCHART



1-bit time before resuming normal transmission.

In the synchronous mode setting, CR bit 3 forces the transmission of the DLE character prior to sending the character in the TxHR. Because this is a one-time command, bit 3 automatically resets.

Bit 5 of the CR controls the state of the $\overline{RTS}$ output. When CR bit 5 is a one, $\overline{RTS}$ goes LOW and the transmit logic enabled. A one-to-zero transistion of bit 5 causes $\overline{RTS}$ to go HIGH one TxC time after the last serial bit is transmitted, if the TxSR was not already empty.

Command Register bits 6 and 7 provide four alternative modes of operation in both synchronous and asynchronous operation. When both bits are zero, normal operation is selected. In the asynchronous mode, when only CR bit 6 is set, automatic echo mode is selected. In this mode, clocked, regenerated received data is automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (bit 2 is a one), but the transmitter need not be enabled. CPU-to-receiver communications continue normally, but the CPU-to-transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output goes HIGH until the next valid start is detected.

The following conditions are true while in automatic echo mode:

1. Data assembled by the receiver is automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. Transmit clock = receive clock.
3. $\overline{TxRDY}$ output = 1.
4. The $\overline{TxEMT}/\overline{DSCHG}$ pin reflects only the data set change condition.
5. The TxEN command (CR bit 0) is ignored.

In the synchronous mode, when only CR bit 6 is set, automatic SYN/DLE stripping is performed. The state of MR1 bits 6 and 7 controls which characters are stripped (Figure 1 and Table 3). Automatic stripping does not affect setting of the SYN and DLE detect status register bits.

FIGURE 5: MODE REGISTER 1

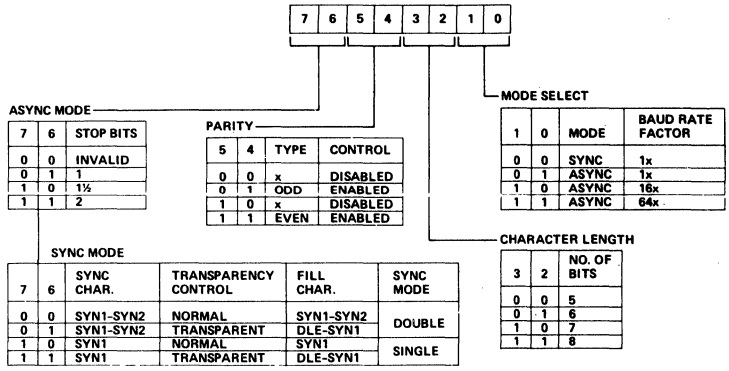


FIGURE 6: MODE REGISTER 2

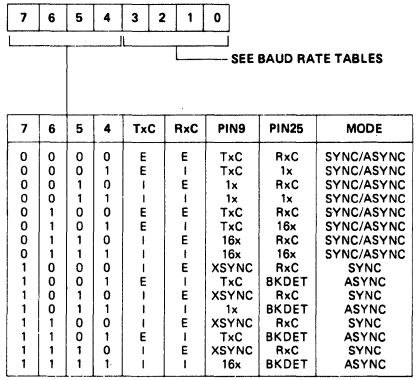
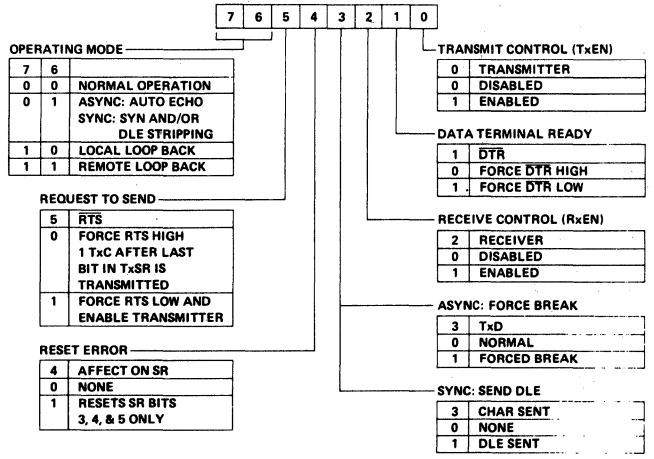


FIGURE 7: COMMAND REGISTER



Two diagnostic modes are achievable in both synchronous and asynchronous operation: local loopback with CR bit 7 a one and CR bit 6 a zero, and remote loopback with both bits ones.

LOCAL LOOPBACK, Note 1

1. The transmitter output is connected to the receiver input.
2. $\overline{DTR}$ is connected to DCE and $\overline{RTS}$ is connected to $\overline{CTS}$.
3. Transmit clock is connected to the receive clock.
4. The $\overline{DTR}$, $\overline{RTS}$ and TxD outputs are held HIGH.
5. The $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ and RxD inputs are ignored.

REMOTE LOOPBACK

1. Data assembled by the receiver is automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. Receive clock is connected to the transmit clock.
3. No data is sent to the local CPU, but the error status conditions (PE, OE, FE) are set.
4. The $\overline{RxRDY}$, $\overline{TxRDY}$, and $\overline{TxEMT}$/$\overline{DSCHG}$ outputs are held HIGH.
5. CR bit 1 (TxEN) is ignored.
6. All other signals operate normally.

STATUS REGISTER (SR)

Status Register bit 0 is the transmitter ready ($\overline{TxRDY}$) status bit. It is the logical complement of the TxRDY output (Figure 8). This bit indicates the state of the TxHR when the transmitter is enabled (TxEN is a one). A zero indicates that TxHR is full, a one indicates that TxHR is empty and requires servicing by the CPU. This bit is cleared by writing to TxHR or by disabling the transmitter (TxEN is a zero). Note that SR bit 0 is not set in either the auto echo or remote loopback modes.

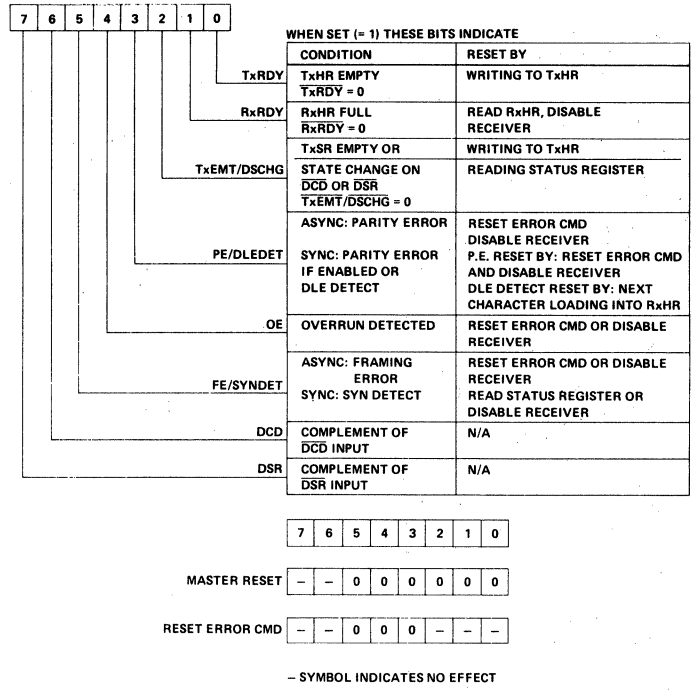
Bit 1 of the SR is the receiver ready ($\overline{RxRDY}$) status bit. It is the logical complement of the $\overline{RxRDY}$ output. This bit indicates the state of the RxHR when the receiver is enabled (RxEN is a one). A zero indicates that the RxHR is empty, a one indicates that the RxHR is full and requires servicing by the CPU. This bit is cleared by writing to the TxHR or by disabling the receiver (RxEN is a zero).

Status Register bit 2 indicates a change of status of either $\overline{DSR}$ or $\overline{DCD}$, or that the TxSR is empty. This bit is the logical complement of the $\overline{TxEMT}$/$\overline{DSCHG}$ output. A read of the status clears bit 2 if a state change on $\overline{DSR}$ or $\overline{DCD}$ has occurred. If a second successive read of the status register indicates bit 2 is a zero, $\overline{DCD}$ or $\overline{DSR}$ has changed. If bit 2 is still set, the TxSR is empty. Because the transmitter does not start until the first character has been written to the TxHR, $\overline{TxEMT}$ status is not reflected until transmission of the first character is complete, $\overline{TxEMT}$ status is cleared by writing to the TxHR or disabling the transmitter. Note that $\overline{TxEMT}$ status is set in synchronous mode even though "fill" characters are being transmitted.

When set, SR bit 3 reflects a parity error when parity checking is enabled in both the synchronous and asynchronous modes. In the synchronous transparent mode (MR2 bit 16 is a one) with the parity enable bit (MR2 bit 4) a zero, SR bit 3 indicates DLE detect when set. This indicates that a character matching the DLE register was received and the present character is neither SYN1 nor DLE. This bit is cleared when the next character following the above sequence is loaded into the RxHR, when the receiver is disabled or by a reset error command.

Bit 4 of the SR indicates an overrun error when set. An overrun condition exists when the CPU does not read the RxHR before the next received character is transferred to it. (The previous character is lost.) Bit 4 is cleared by the reset error command and when the receiver is disabled.

FIGURE 8: STATUS REGISTER



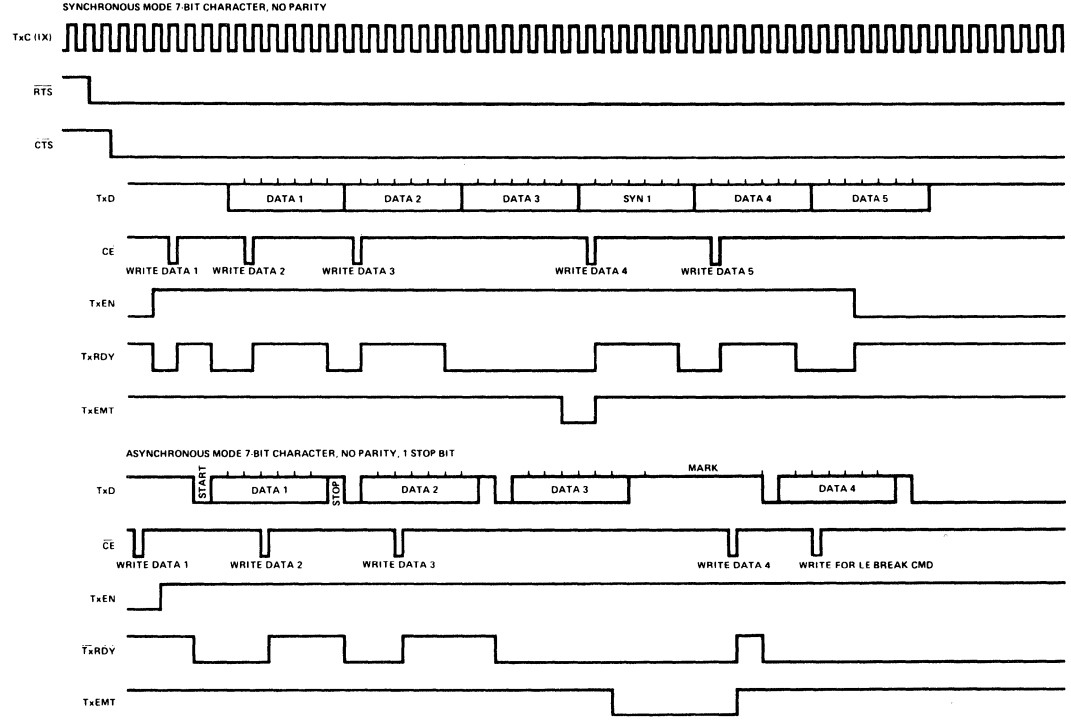
Notes:

1. CR bits 0, 1 and 5 must be set, CR bit 2 is a don't care.

TABLE 3: EFFECT OF MR17 AND MR16 ON CHARACTER FILL AND CHARACTER STRIPPING (SYNCHRONOUS MODE)

MR17	MR16	Mode	Synchronizing Sequence	Character Fill	Character(s) Stripped CR7 = 0, CR6 = 1
0	0	Double SYN Normal	SYN1-SYN2	SYN1-SYN2	SYN1 SYN1-SYN2[1]
1	0	Single SYN Normal	SYN1	SYN1	SYN1[1]
0	1	Double SYN Transparent	SYN1-SYN2	DLE-SYN1	DLE-SYN1[1] SYN1-SYN2[1] (Only Initial Synchronizing Sequence) DLE (also Sets SR3 if Parity Disabled and it is not Following a DLE or SYN1) In a DLE-DLE Sequence Only the First DLE is Stripped
1	1	Single SYN Transparent	SYN1	DLE-SYN1	DLE-SYN1[1] SYN1 (only Initial Synchronizing Sequence) DLE and DLE-DLE same as Double SYN Transparent

FIGURE 9: TRANSMITTER OPERATION TIMING DIAGRAM



Notes:

1. Symbol indicates SYN DET status set upon detection of initial synchronizing characters and after SYNC has been achieved by detection of a DLE-SYN1 pair.

In the asynchronous mode, SR bit 5 indicates that the received character was not framed by a stop bit. If the RxHR is all zeros when bit 5 is set, a break condition was present. In synchronous non-transparent mode, bit 5 indicates receipt of the SYN1 character in single-SYN mode or the SYN1-SYN2 pair in double-SYN mode. In synchronous transparent mode, this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1-SYN2) and after synchronization has been achieved, when a DLE-SYN1 pair is received. The bit is reset when the receiver is disabled, when the reset error command is given in asynchronous mode and when the Status Register is read by the CPU in the synchronous mode.

Status Register bits 6 and 7 reflect the condition of the $\overline{DCD}$ and $\overline{DSR}$ inputs, respectively. Their states are the logical complements of their respective inputs.

VL6551•VL65C51

ASYNCHRONOUS COMMUNICATION INTERFACE ADAPTER

FEATURES

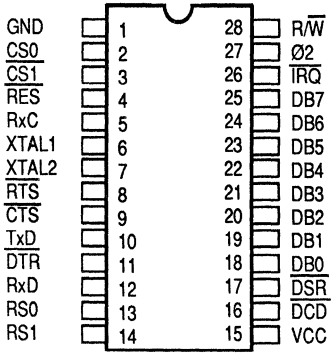
- On-chip baud rate generator: 15 programmable baud rates derived from a standard 1.8432 MHz external crystal (50 to 19,200 baud)
- Programmable interrupt and status register to simplify software design
- Single 5 V power supply
- Serial echo mode
- False start bit detection
- 8-bit bidirectional data bus for direct communication with the microprocessor
- Parity: odd, even, none, mark, space
- External 16x clock input for non-standard baud rates (up to 125K baud)
- Programmable: word lengths, number of stop bits, and parity bit generation and detection
- Data set and modem control signals provided
- Full-duplex or half-duplex operation
- 5, 6, 7, 8, and 9 bit transmission
- Low-cost HMOS technology (VL6551)
- Low power consumption CMOS technology (VL65C51)

DESCRIPTION

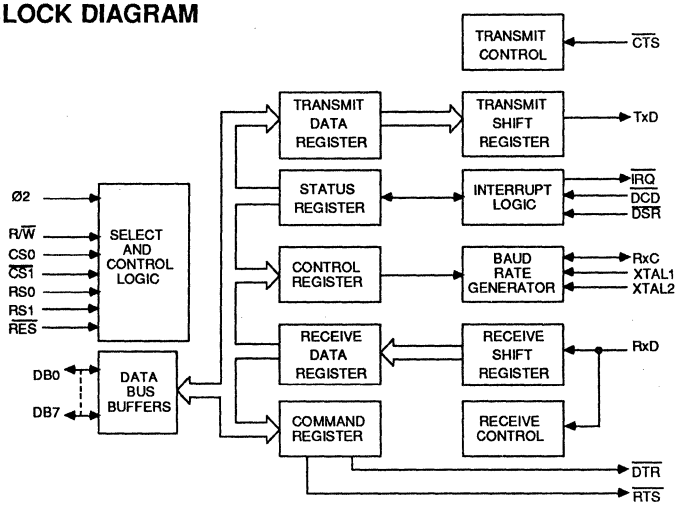
The VL6551/VL65C51 is an Asynchronous Communications Interface Adapter (ACIA) which provides an interface between 6500/6800 microprocessor families and serial communication data sets and modems. A unique feature is the inclusion of an on-chip programmable baud rate generator, with a crystal being the only external component required. The device is available in both very low cost HMOS (VL6551) and very low power CMOS (VL65C51) technologies.

PIN DIAGRAM

VL6551
VL65C51



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Clock Rate	Package
VL6551-01PC	1 MHz	Plastic DIP
VL6551-01CC		Ceramic DIP
VL65C51-01PC		Plastic DIP
VL65C51-01CC		Ceramic DIP
VL6551-02PC	2 MHz	Plastic DIP
VL6551-02CC		Ceramic DIP
VL65C51-02PC		Plastic DIP
VL65C51-02CC		Ceramic DIP
VL65C51-03PC	3 MHz	Plastic DIP
VL65C51-03CC		Ceramic DIP
VL65C51-04PC	4 MHz	Plastic DIP
VL65C51-04CC		Ceramic DIP

Note: Operating temperature is 0°C to +70°C

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
$\overline{RES}$	4	During initialization, low on the Reset input causes internal registers to be cleared.
RxD	12	The RxD input line receives serial NRZ data into the ACIA from the modem, last bit first.
Ø2	27	The input clock is the system Ø2 clock and is used to trigger all data transfers between the microprocessor and the VL65(C)51.
R/$\overline{W}$	28	The Read/Write signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the VL65(C)51. A low on the R/$\overline{W}$ pin allows a write to the VL65(C)51.
$\overline{IRQ}$	26	The interrupt request signal, from the interrupt control logic, is an open drain output, that permits several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.
DB0 - DB7	18 - 25	The DB0-DB7 pins are the eight data lines used for transfer of data between the processor and the VL65(C)51. These lines are bidirectional and are normally high-impedance except when selected during Read cycles.
CS0, $\overline{CS1}$	2, 3	The two Chip Select inputs are normally connected to the processor address lines either directly or through decoders. The VL65(C)51 is selected when CS0 is high and $\overline{CS1}$ is low.
RS0, RS1	13, 14	The two register select lines are normally connected to the processor address lines to allow the processor to select the various VL65(C)51 internal registers. The following table shows the internal register select coding.

RS1	RS0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

The table shows that only the Command and Control Registers are read/write. The programmed reset operation does not cause any data transfer, but is used to clear the VL65(C)51 registers. The programmed reset is slightly different from the hardware reset and these differences are described in the individual register definitions.

XTAL1, XTAL2	6, 7	External crystal (1.8432 MHz) connection that drives the various baud rates. An externally generated clock may be used to drive the XTAL1 pin (XTAL2 pin must float).
TxD	10	The TxD output line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock. This selection is made by programming the Control Register.
RxC	5	The RxC is a bidirectional pin that serves as either the receiver 16x clock input or the receiver 16x clock output. Output results if the internal baud rate generator is selected.
$\overline{RTS}$	8	The $\overline{RTS}$ output is used to control the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.
$\overline{CTS}$	9	The $\overline{CTS}$ input is used to control the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.
$\overline{DTR}$	11	This output pin is used to indicate the status of the VL65(C)51 to the modem. A low on $\overline{DTR}$ indicates the VL65(C)51 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.
$\overline{DSR}$	17	The $\overline{DSR}$ input is used to indicate to the VL65(C)51 the status of the modem. A low indicates the "ready" state and a high, "not-ready". $\overline{DSR}$ is a high-impdeance input and must not be a no-connect. If unused, it should be driven high or low, but not switched.
$\overline{DCD}$	16	The $\overline{DCD}$ input is used to indicate to the VL65(C)51 the status of the carrier-detect output of the mode. A low indicates that the modem carrier signal is present and a high, that it is not. $\overline{DCD}$, like $\overline{DSR}$, is a high-impedance input and must not be a no-connect.

Note:
If Command Register Bit 0 = 1 and a change of state on $\overline{DCD}$ occurs, $\overline{IRQ}$ will be set, and Status Register Bit 5 will reflect the new level. The state of $\overline{DCD}$ does not affect Transmitter operation, but must be low for the receiver to operate.

TRANSMITTER AND RECEIVER OPERATION

CONTINUOUS DATA TRANSMIT

In the normal operating mode, the interrupt request output ($\overline{IRQ}$) signals when the ACIA is ready to accept the next data word to be transmitted. This interrupt occurs at the beginning of the Start Bit. When the processor reads the Status Register of the ACIA, the interrupt is cleared. The processor must then identify that the Transmit Data Register is ready to be loaded and must then load it with the next data word. This must occur before the end of the Stop Bit, otherwise a continuous "Mark" will be transmitted.

CONTINUOUS DATA RECEIVE

Similar to the continuous data transmit case, the normal operation of this mode is to assert $\overline{IRQ}$ when the ACIA has received a full data word. This occurs at about the 9/16 point through the Stop Bit. The processor must read the Status Register and read the data word before the next interrupt, otherwise the overrun condition occurs.

TRANSMIT DATA REGISTER NOT LOADED

If the processor is unable to load the Transmit Data Register in the allocated time, then the TxD line goes to the "Mark" condition until the data is loaded. $\overline{IRQ}$ interrupts continue to occur at the same rate as previously stated, except no data is transmitted. When the processor finally loads new data, a Start Bit immediately occurs, the data word transmission is started, and another interrupt is initiated, signaling for the next data word.

EFFECT OF CTS ON TRANSIMITTER

The Clear-to-Send signal is generated by the modem. It is normally low (true state) but may go high in the event of some modem problems. When this occurs, the TxD line goes to the "Mark" condition after the entire last character (including parity and stop bit) has been transmitted. Bit 4 in the Status Register indicates that the Transmit Data Register is not empty and $\overline{IRQ}$ is not asserted. $\overline{CTS}$ is a transmit control line only, and has no effect on the ACIA receiver operation.

EFFECT OF OVERRUN ON RECEIVER

If the processor does not read the Receive Data Register in the allocated time, when the following interrupt occurs, the new data word is not transferred to the Receive Data Register, but the Overrun Status Bit is set. Thus, the Receive Data Register will contain the last valid data word received and all following data is lost.

ECHO MODE TIMING

In Echo Mode, the TxD line retransmits the data on the RxD line, delayed by one-half of the bit time.

EFFECT OF $\overline{CTS}$ ON ECHO MODE

In Echo Mode, the receiver operation is unaffected by $\overline{CTS}$; however, the transmitter is affected when $\overline{CTS}$ goes High, i.e., the TxD line immediately goes to a continuous "Mark" condition. In this case, however, the status request indicates that the Receive Data Register is full in response to an $\overline{IRQ}$, so the processor has no way of knowing that the transmitter has ceased to echo.

OVERRUN IN ECHO MODE

If overrun occurs in Echo Mode, the receiver is affected the same way as a normal overrun in Receive Mode. For the retransmitted data, when overrun occurs, the TxD line goes to the "Mark" condition until the first Start Bit after the Receive Data Register is read by the processor.

FRAMING ERROR

Framing error is caused by the absence of Stop Bit(s) on received data. A framing error is indicated by the setting of bit 4 in the Status Register at the same time the Receive Data Register Full (RDRF) Bit is set, also in the Status Register. In response to $\overline{IRQ}$, generated by RDRF, the Status Register can also be checked for the framing error. Subsequent data words are tested separately for framing error, so the status bit will always reflect the last data word received.

EFFECT OF $\overline{DCD}$ ON RECEIVER

$\overline{DCD}$ is a modem output indicating the status of the carrier-frequency-detection circuit of the modem. This line goes high for a loss of carrier. Normally, when this occurs, the modem will stop transmitting data some time later. The ACIA asserts $\overline{IRQ}$ whenever $\overline{DCD}$ changes state and indicates this condition via bit 5 in the Status Register. Once such a change of state occurs, subsequent transitions will not cause interrupts or changes in the Status Register until the first interrupt is serviced. When the Status Register is read by the processor, the ACIA automatically checks the level of the $\overline{DCD}$ line, and if it has changed, another $\overline{IRQ}$ occurs.

TIMING WITH 1-1/2 STOP BITS

It is possible to select 1-1/2 Stop Bits, but this occurs only for 5-bit data words with no parity bit. In this case, the $\overline{IRQ}$ asserted for receive data register full occurs halfway through the trailing half-Stop Bit.

TRANSMIT CONTINUOUS "BREAK"

This mode is selected via the ACIA Command Register and causes the transmitter to send continuous "Break" characters, beginning with the next character transmitted. At least one full "Break" character will be transmitted, even if the processor quickly re-programs the Command Register transmit mode. Later, when the Command Register is programmed back to normal transmit mode, an immediate Stop Bit will be generated and transmission will resume. If, while operating in the Transmit Continuous "Break" Mode, the $\overline{CTS}$ should go to a high, the TxD will be overridden by the $\overline{CTS}$ and will go to continuous "Mark" at the beginning of the next character transmitted after the $\overline{CTS}$ goes high.

RECEIVE CONTINUOUS "BREAK"

In the event the modem transmits continuous "Break" characters, the ACIA will terminate receiving. Reception will resume only after a Stop Bit is encountered by the ACIA.

STATUS REGISTER OPERATION

Because of the special functions of the various status bits, there is a suggested sequence for checking them. When an interrupt occurs, the ACIA should be interrogated, as follows:

1. Read Status Register. This operation automatically clears Bit 7 ($\overline{IRQ}$). Subsequent transitions on $\overline{DSR}$ and $\overline{DCD}$ will cause another interrupt.
2. Check $\overline{IRQ}$ (bit 7) in the data read from the Status Register. If not set, the interrupt source is not the ACIA.

3. Check $\overline{DCD}$ and $\overline{DSR}$. These must be compared to their previous levels, which must have been saved by the processor. If they are both 0 (modem "on-line") and they are unchanged, the remaining bits must be checked.
4. Check RDRF (Bit 3). Check for Receive Data Register full.
5. Check Parity, Overrun, and Framing Error (Bits 0-2) if the Receiver Data Register is full.
6. Check TDRE (Bit 4). Check for Transmitter Data Register empty.
7. If none of the above conditions exist, then $\overline{CTS}$ must have gone to the false (high) state.

PROGRAM RESET OPERATION

A program reset occurs when the processor performs a write operation to the ACIA with RS0 low and RS1 high. The program reset operates somewhat differently from the hardware reset ($\overline{RES}$ pin) and is described as follows:

1. Internal registers are not completely cleared. Check register formats for the effect of a program reset on internal registers.
2. DTR line goes high immediately.
3. Receiver and transmitter interrupts are disabled immediately. If $\overline{IRQ}$ is low when the reset occurs, it stays low until serviced, unless the interrupt was caused by $\overline{DCD}$ or $\overline{DSR}$ transition.
4. $\overline{DCD}$ and $\overline{DSR}$ interrupts are disabled immediately. If $\overline{IRQ}$ is Low and was caused by $\overline{DCD}$ or $\overline{DSR}$, then it goes high; also $\overline{DCD}$ and $\overline{DSR}$ status bits subsequently will follow the input lines, although no interrupt will occur.
5. Overrun cleared, if set.

MISCELLANEOUS

1. If Echo Mode is selected, $\overline{RTS}$ goes Low.
2. If Bit 0 of Command Register is 0 (disabled), then:
   a) All interrupts are disabled, including those caused by $\overline{DCD}$ and $\overline{DSR}$ transitions.
   b) Transmitter is disabled immediately.
   c) Receiver is disabled, but a character currently being received will be completed first.
3. Odd parity occurs when the sum of all the 1 bits in the data work (including the parity bit) is odd.
4. In the receiver mode, the received parity bit does not go into the Receiver Data Register, but generates parity error or no parity error for the Status Register.
5. Transmitter and Receiver may be in full operation simultaneously. This is full-duplex mode.
6. If the RxD line inadvertently goes low and then high right after a Stop Bit, the ACIA does not interpret this as a Start Bit, but samples the line again halfway into the bit to determine if it is a true Start Bit or false one. For false Start Bit detection, the ACIA does not begin to receive data; instead, only a true Start Bit initiates receiver operation.
7. Precautions to consider with the crystal oscillator circuit:
   a) The external crystal should be a "series" mode crystal.
   b) The XTALI input may be used as an external clock input. The unused pin (EXTAL0) must be floating and may not be used for any other function.
8. $\overline{DCD}$ and $\overline{DSR}$ transitions, although causing immediate processor interrupts, have no effect on transmitter operation. Data will continue to be sent, unless the processor forces the transmitter to turn off. Since these are high- impedance inputs, they must not be permitted to float (unconnected). If unused, they must be terminated either to GND or VCC.

GENERATION OF NON-STANDARD BAUD RATES

The internal counter/divider circuit selects the appropriate divisor for the crystal frequency by means of bits 0-3 of the ACIA Control Register. By using a different crystal, other baud rates may be generated. These can be determined by the baud rate = crystal frequency ÷ divisor. Furthermore, it is possible to drive the ACIA with an off-chip oscillator to achieve other baud rates. In this case, XTALI (pin 6) must be the clock input and XTAL0 (pin 7) must be a no-connect.

FIGURE 1. TRANSMITTER/RECEIVER CLOCK CIRCUITS

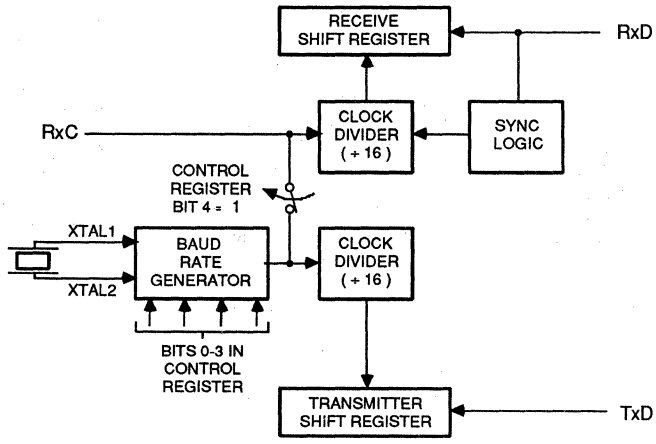


FIGURE 2. CONTROL REGISTER

The Control Register is used to select the desired mode for the VL65(C)51. The word length, number of stop bits, and clock controls are defined below.

CONTROL REGISTER

7	6	5	4	3	2	1	0

STOP BITS

0 = 1 Stop Bit

1 = 2 Stop Bits
1 Stop Bit if Word Length = 8 Bits and Parity*
1.5 Stop Bits if Word Length = 5 Bits and No Parity

WORD LENGTH

BIT 6	BIT 5	DATA WORD LENGTH
0	0	8
0	1	7
1	0	6
1	1	5

RECEIVER CLOCK SOURCE

0 = External Receiver Clock
1 = Baud Rate Generator

BAUD RATE GENERATOR

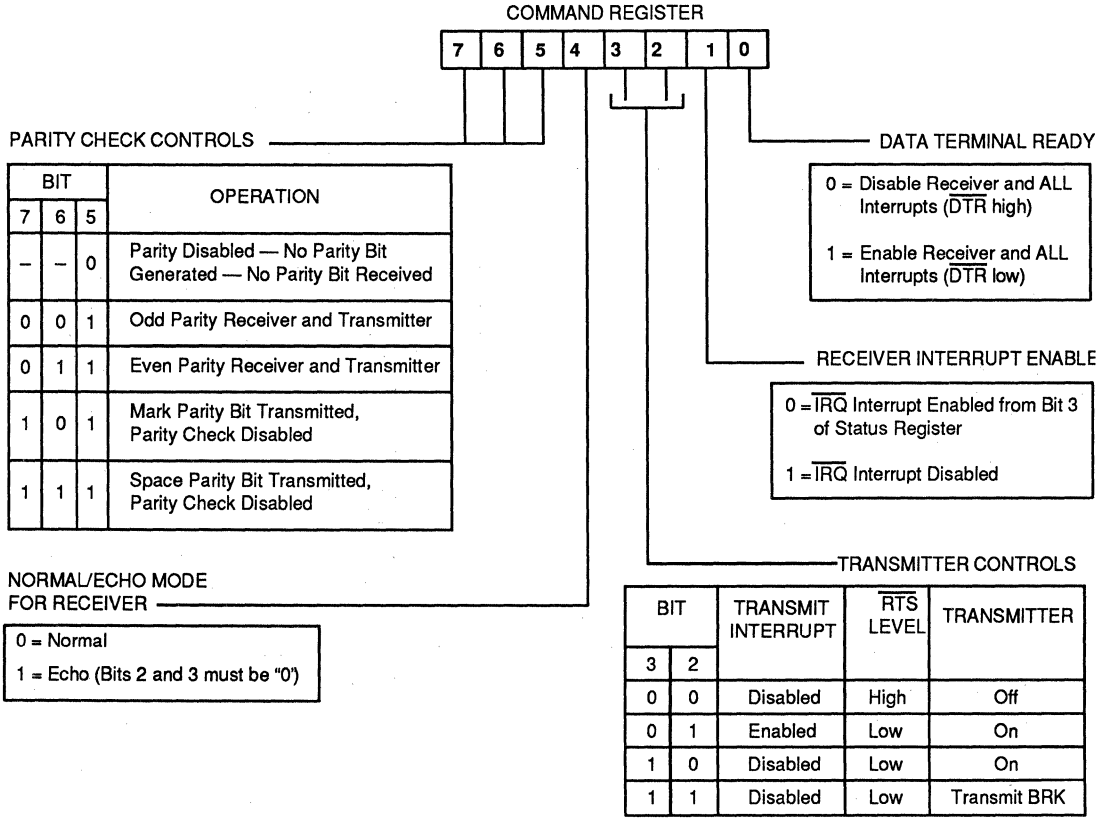
3	2	1	0	
0	0	0	0	16 x EXTERNAL CLOCK
0	0	0	1	50
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

* This allows for 9-bit transmission (8 data bits plus parity).

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	–	–	–	–	–	–	–	–

FIGURE 3. COMMAND REGISTER

The Command Register is used to control specific transmit/receive functions.

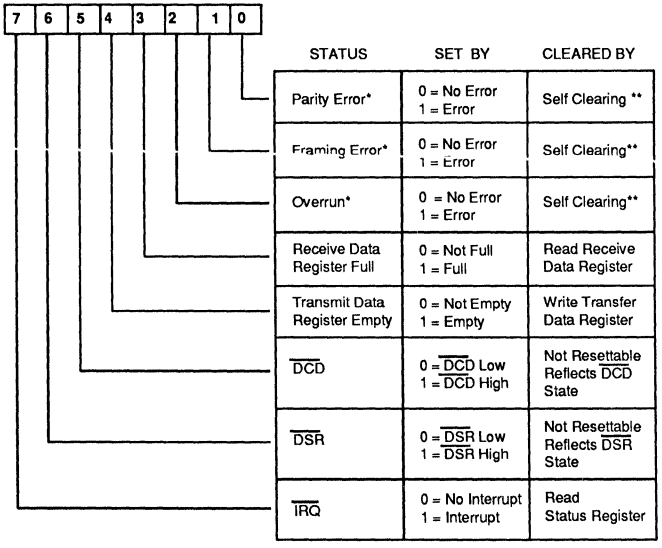


BIT			OPERATION
7	6	5	
–	–	0	Parity Disabled — No Parity Bit Generated — No Parity Bit Received
0	0	1	Odd Parity Receiver and Transmitter
0	1	1	Even Parity Receiver and Transmitter
1	0	1	Mark Parity Bit Transmitted, Parity Check Disabled
1	1	1	Space Parity Bit Transmitted, Parity Check Disabled

BIT		TRANSMIT INTERRUPT	$\overline{\text{RTS}}$ LEVEL	TRANSMITTER
3	2			
0	0	Disabled	High	Off
0	1	Enabled	Low	On
1	0	Disabled	Low	On
1	1	Disabled	Low	Transmit BRK

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	–	–	–	0	0	0	0	0

FIGURE 4. STATUS REGISTER



* NO INTERRUPT GENERATED FOR THESE CONDITIONS.

** CLEARED AUTOMATICALLY AFTER A READ OF RDR AND THE NEXT ERROR-FREE RECEIPT OF DATA.

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	–	–	1	0	0	0	0
PROGRAM RESET	–	–	–	–	–	0	–	–

FIGURE 5. DATA STREAM EXAMPLE

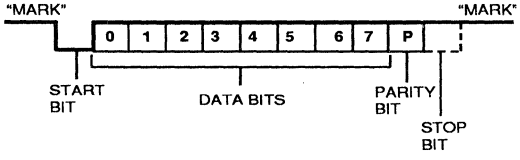


TABLE 1. TRANSMIT/RECEIVE CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ±5%

		VL65(C)51-01		VL65(C)51-02		VL65C51-03		VL65C51-04		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Unit
TCYC	T/R Clock Rate	400*	—	400*	—	400*	—	400*	—	µs
TCH	T/R Clock High Time	175	—	175	—	175	—	175	—	ns
TCL	T/R Clock Low Time	175	—	175	—	175	—	175	—	ns
TDD	XTL1 to TxD Prop. Dly.	—	500	—	500	—	330	—	250	ns
TDLY	Prop. Dly. ($\overline{RTS}$, $\overline{DTR}$)	—	500	—	500	—	330	—	250	ns
TIRQ	$\overline{IRQ}$ Prop. Dly.	—	500	—	500	—	500	—	500	ns

TR, TF = 10 to 30 ns

The baud rate with external clocking is: Baud Rate = 1 ÷ (16 X TCYC)

TABLE 2. READ TIMING TA = 0°C to +70°C, VCC = 5 V ±5%

Symbol	Parameter	VL65(C)51-01		VL65(C)51-02		VL65C51-03		VL65C51-04		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
TCYC	Cycle Time	1.0	—	0.5	—	0.33	—	0.25	—	µs
TC	Ø2 Pulse Width	470	—	240	—	160	—	120	—	ns
TACR	Address Set-Up Time	160	—	90	—	65	—	45	—	ns
TCAR	Address Hold Time	0	—	0	—	0	—	0	—	ns
TWCR	R/$\overline{W}$ Set-Up Time	160	—	90	—	65	—	45	—	ns
TCDR	Read Access Time	—	200	—	150	—	120	—	90	ns
THR	Read Data Hold Time	10	—	10	—	10	—	10	—	ns
THW	Bus Active Time	40	—	40	—	40	—	40	—	ns

TR, TF = 10 to 30 ns

FIGURE 6. READ TIMING (SEE TABLE 2)

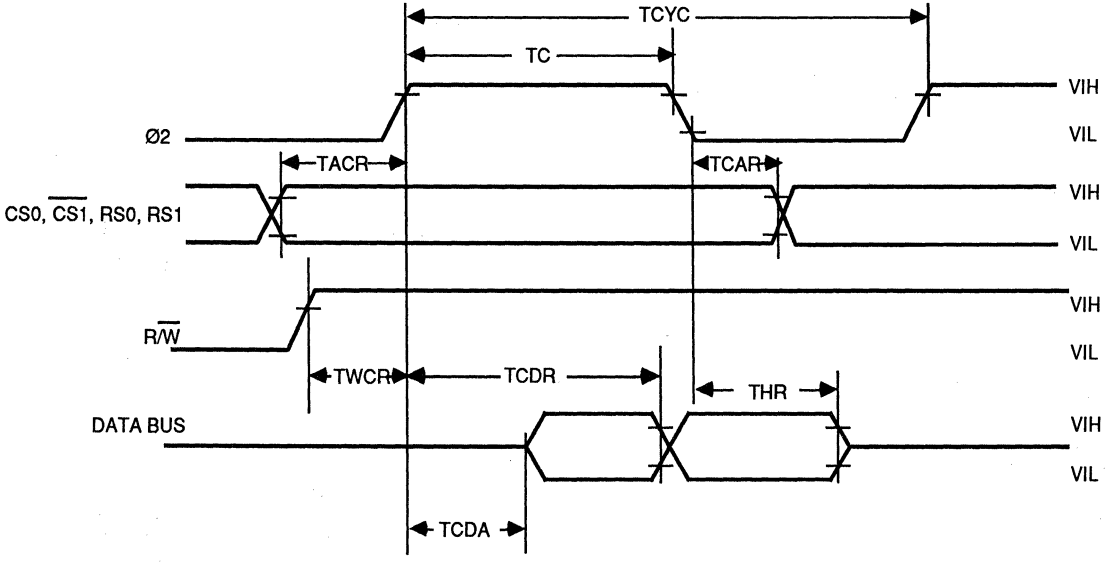


TABLE 3. WRITE TIMING TA = 0°C to +70°C, VCC = 5 V ±5%

Symbol	Parameter	VL65(C)51-01		VL65(C)51-02		VL65C51-03		VL65C51-04		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
TCYC	Cycle Time	1.0	—	0.5	—	0.33	—	0.25	—	µs
TC	Ø2 Pulse Width	470	—	240	—	160	—	120	—	ns
TACW	Address Set-Up Time	160	—	90	—	65	—	45	—	ns
TCAH	Address Hold Time	0	—	0	—	0	—	0	—	ns
TWCW	R/$\overline{W}$ Set-Up Time	160	—	90	—	65	—	45	—	ns
TCWH	R/$\overline{W}$ Hold Time	0	—	0	—	0	—	0	—	ns
TDCW	Data Bus Set-Up Time	195	—	90	—	65	—	45	—	ns
THW	Data Bus Hold Time	10	—	10	—	10	—	10	—	ns

TR, TF = 10 to 30 ns

FIGURE 7. WRITE TIMING (SEE TABLE 3)

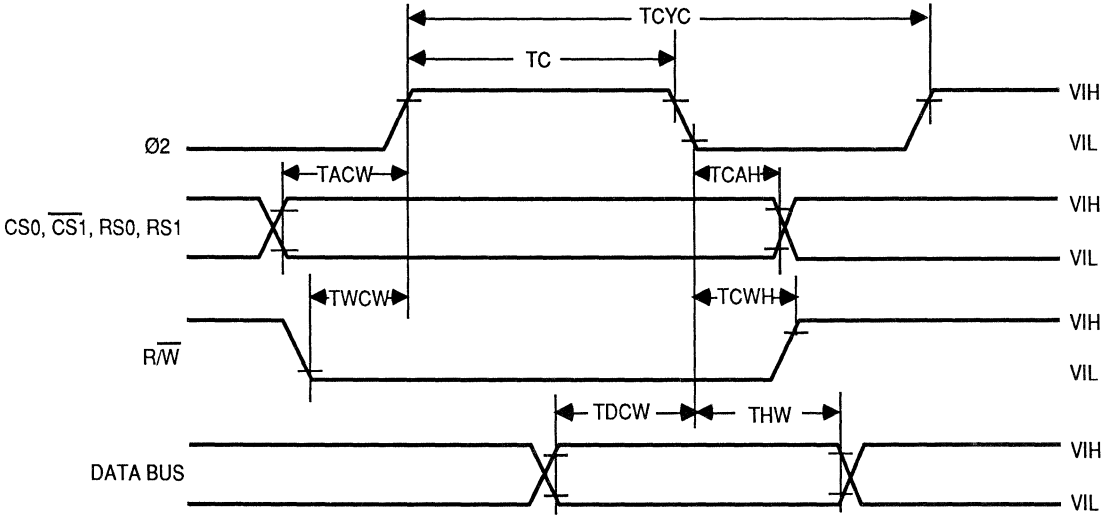
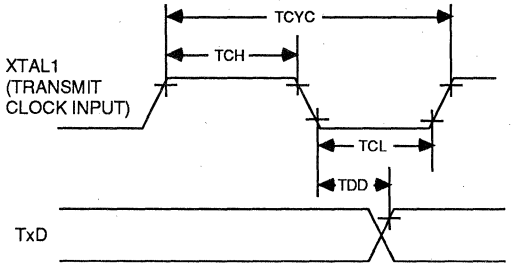


FIGURE 8. TRANSMIT TIMING (SEE TABLE 1)



NOTE: TxD RATE IS 1/16 TxC RATE.

FIGURE 9. INTERRUPT TIMING (SEE TABLE 1)

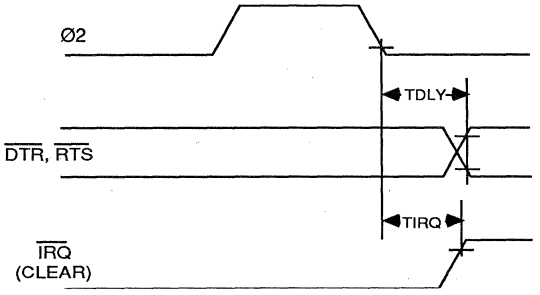
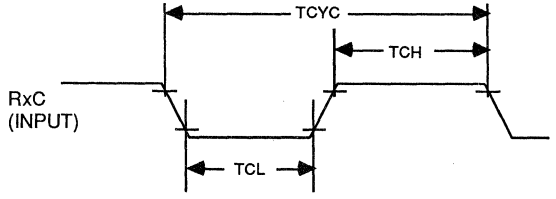
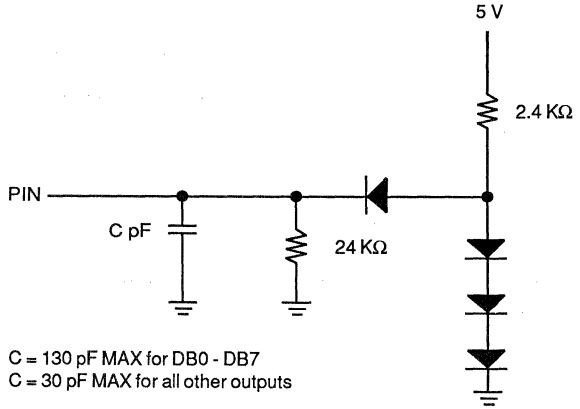


FIGURE 10. RECEIVE EXTERNAL CLOCK TIMING (SEE TABLE 1)



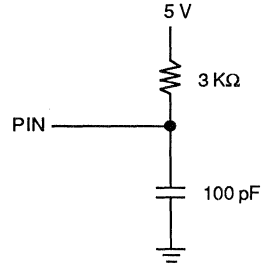
NOTE: RxD RATE IS 1/16 RxC RATE.

FIGURE 11. TEST LOADS



C = 130 pF MAX for DB0 - DB7
C = 30 pF MAX for all other outputs

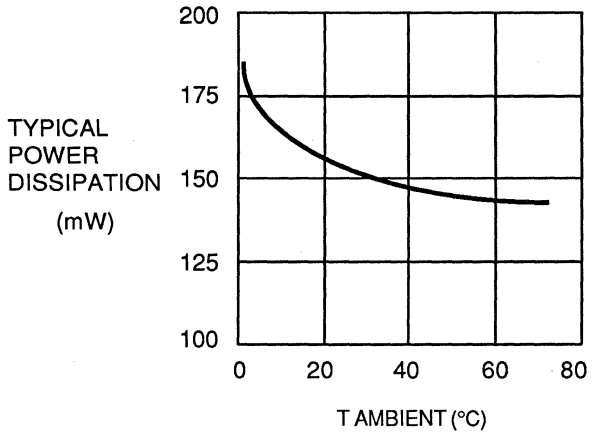
OPEN COLLECTOR
OUTPUT TEST LOAD



DC CHARACTERISTICS (VL6551) TA = 0°C to +70°C, VCC = 5 V ±5%, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions
VIH	Input HIGH Voltage	2.0	—	VCC	V	VIN = 0 to 5 V
VIL	Input LOW Voltage	–0.3	—	0.8	V	
IIN	Input Leakage Current: (Ø2, R/$\overline{W}$, $\overline{RES}$, CS0, $\overline{CS1}$, RS0; RS1, $\overline{CTS}$, RxD, $\overline{DC}$ $\overline{DSR}$)	—	±1.0	±2.5	µA	
ITSI	Input Leakage Current for High Imped.	—	±2.0	±10.0	µA	
VOH	Output HIGH Voltage: (DB0 – DB7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	2.4	—	—	V	ILOAD = –100 µA
VOL	Output LOW Voltage: (DB0 – DB7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	—	—	0.4	V	ILOAD = 1.6 mA
IOH	Output HIGH Current (Sourcing): (DB0 – DB7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	–100	—	—	µA	VOH = 2.4 V
IOL	Output LOW Current (Sinking): VOL = 0.4 V (DB0 – DB7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	1.6	—	—	mA	VOH = 2.4 V
IOFF	Output Leakage Current (Off State): VOUT = 5V ($\overline{IRQ}$)	—	1.0	10.0	µA	
CCLK	Clock Capacitance (Ø2)	—	—	20	pF	
CIN	Input Capacitance (Except XTAL1 and XTAL2)	—	—	10	pF	
COUT	Output Capacitance	—	—	10	pF	
PD	Power Dissipation (See Graph) (TA = 0°C)	—	170	300	mW	VCC = 5.25 V

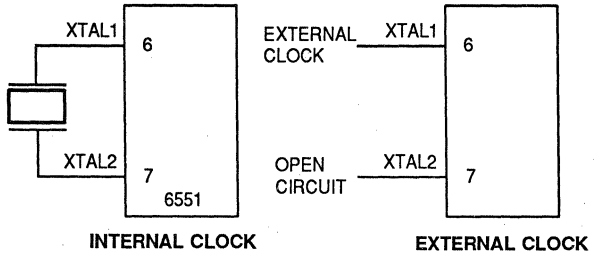
FIGURE 12. HMOS POWER DISSIPATION VS. TEMPERATURE



DC CHARACTERISTICS (VL65C51) TA = 0°C to +70°C, VCC = 5 V ±5%, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions
VIH	Input HIGH Voltage	2.0	—	VCC	V	VIN = 0 to 5 V
VIL	Input LOW Voltage	−0.3	—	0.8	V	
IIN	Input Leakage Current: (Ø2, R/$\overline{W}$, $\overline{RES}$, CS0, $\overline{CS1}$, RS0; RS1, $\overline{CTS}$, RxD, $\overline{DC}$ D$\overline{DSR}$)	—	±1.0	±2.5	µA	
ITSI	Input Leakage Current for High Imped.	—	±2.0	±10.0	µA	
VOH	Output HIGH Voltage: (DB0 – DB7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	2.4	—	—	V	ILOAD = −100 µA
VOL	Output LOW Voltage: (DB0 – DB7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	—	—	0.4	V	ILOAD = I.6 mA
IOH	Output HIGH Current (Sourcing): (DB0 – DB7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	−200	—	—	µA	VOH = 2.4 V
IOL	Output LOW Current (Sinking): VOL = 0.4 V (DB0 – DB7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	1.6	—	—	mA	VOH = 2.4 V
IOFF	Output Leakage Current (Off State): VOUT = 5 V ($\overline{IRQ}$)	—	1.0	10.0	µA	
CCLK	Clock Capacitance (Ø2)	—	—	20	pF	
CIN	Input Capacitance (Except XTAL1 and XTAL2)	—	—	10	pF	
COUT	Output Capacitance	—	—	10	pF	
PD	Power Dissipation (TA = 0°C)	—	7	10	mW/MHz	VCC = 5.25 V

FIGURE 13. CLOCK GENERATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.3 V to +7.0 V
Input/Output Voltage	-0.3 V to +7. 0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°Cto 150°C

All inputs contain protection circuitry to prevent damage to high static charges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

VL8530

SERIAL COMMUNICATIONS CONTROLLER (SCC)

FEATURES

- Two independent full-duplex channels
- 0 to 1.5M bit/second
- Multi-protocol operation for NRZ, NRZI, or FM
- Asynchronous mode includes 1, 1.5, or 2 stop bits per character.
- Programmable clock factor
- Break generation and error detection
- Intelligent SDLC/HDLC
- Local loopback and auto echo modes
- Synchronous support includes internal or external character synchronization.

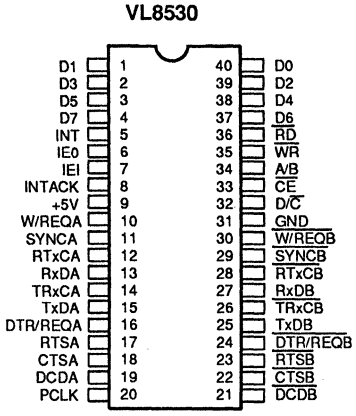
DESCRIPTION

The VL8530 Serial Communications Controller (SCC) is a dual-channel, multiprotocol data communications peripheral designed for use with conventional non-multiplexed buses. The SCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions, including on-chip baud rate generators, digital phase-locked loops, and crystal oscillators that dramatically reduce the need for external logic.

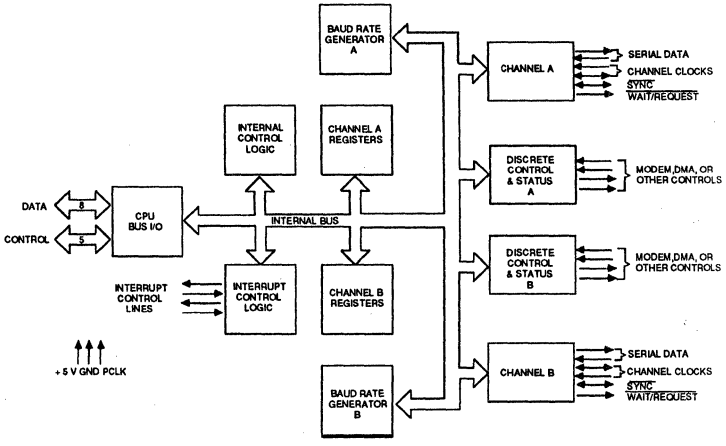
The SCC handles asynchronous formats, synchronous byte-oriented protocols, such as IBM Bisync, and synchronous bit-oriented protocols, such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drives, etc.).

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The SCC also has facilities for modem controls in both channels.

PIN DIAGRAM



BLOCK DIAGRAM

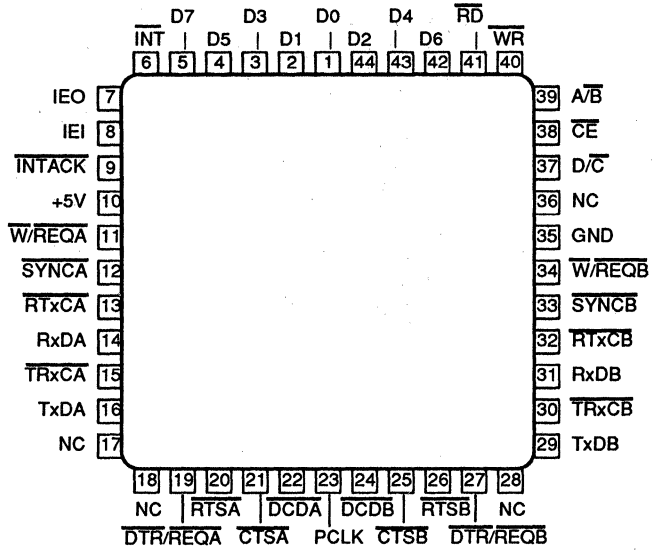


ORDER INFORMATION

Part Number	Clock Frequency	Package
VL8530-04PC	4 MHz	Plastic DIP
VL8530-04QC		Plastic Leaded Chip Carrier
VL8530-04CC		Ceramic DIP
VL8530-06QC	6 MHz	Plastic DIP
VL8530-06PC		Plastic Leaded Chip Carrier
VL8530-06CC		Ceramic DIP

Note: Operating temperature range: 0° to +70°C.

PIN DIAGRAM



SIGNAL DESCRIPTIONS

Signal Name	DIP Pin Number	Signal Description
A/$\overline{B}$	34	Channel A/Channel B Select - This input signal selects the channel on which the read or write operation occurs.
$\overline{C/E}$	33	Chip Enable - This active-LOW input signal selects the SCC for a read or write operation.
$\overline{CTSA}$, $\overline{CTSB}$	18 22	Clear To Send-Active-LOW inputs- If these pins are programmed as auto enables, a LOW on the inputs enables the respective transmitters. If not programmed as auto enables, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs. The SCC detects pulses on these inputs and can interrupt the CPU on both logic level transitions.
D/$\overline{C}$	32	Data/Control Select - This input signal defines the type of information transferred to or from the SCC. A HIGH means data is transferred; a LOW indicates a command.
$\overline{DCDA}$, $\overline{DCDB}$	19 21	Data Carrier Detect-Active-LOW inputs- These pins function as receiver enables if they are programmed for auto enables; otherwise, they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accomodate slow rise-time signals. The SCC detects pulses on these pins and can interrupt the CPU on both logic level transitions.
D0-D7	40,1,39,2,38, 3,37,4	Data Bus - These bidirectional, 3-state lines carry data and commands to and from the SCC.
$\overline{DTR/REQA}$ $\overline{DTR/REQB}$	16, 24	Data Terminal Ready/Request - These active-LOW outputs follow the state programmed into the $\overline{DTR}$ bit. They can also be used as general-purpose outputs or as request lines for a direct memeory access (DMA) controller.
IEI	7	Interrupt Enable In-Active-HIGH output- IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A HIGH IEI indicates that no other higher priority device has an interrupt underservice or is requesting an interrupt.
IEO	6	Interrupt Enable Out-Active-HIGH output - IEO is HIGH only if IEI is HIGH and the CPU is not servicing an SCC interrupt or the SCC is not requesting an interrupt (Interrupt Acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.

SIGNAL DESCRIPTIONS (CONTINUED)

Signal Name	DIP Pin Number	Signal Description
$\overline{INT}$	5	Interrupt Request-Active-LOW open-drain output- This signal is activated when theSCC requests an interrupt.
$\overline{INTACK}$	8	Interrupt Acknowledge-Active-LOW input- This signal indicates an active Interrupt Acknowledge cycle. During this cycle, the SCC interrupt daisy chain settles. When $\overline{RD}$ becomes active, the SCC places an interrupt vector on the data bus (if IEI is HIGH). The $\overline{INTACK}$ signal is latched by the rising edge of PCLK.
PCLK	20	Clock - This input is the master SCC clock used to synchronize internal signals. PCLK is a TTL-level signal.
$\overline{RD}$	36	Read-Active-LOW input - This signal indicates a read operation and, when the SCC is selected, enables the SCC's bus drivers. During the Interrupt Acknowledge cycle, this signal gates the interrupt vector onto the bus if the SCC is the highest priority device requesting an interrupt.
RxDA, RxDB	13, 27	Receive Data-Active-HIGH inputs- These input signals receive serial data at standard TTL levels.
$\overline{RTxCA}$, $\overline{RTxCB}$	12, 28	Receive/Transmit Clocks-Active-LOW inputs - These pins can be programmed in several different modes of operation. In each channel, $\overline{RTxC}$ may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the digital phase locked loop. These pins can also be programmed for use with the respective $\overline{SYNC}$ pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous modes.
$\overline{RTSA}$, $\overline{RTSB}$	17, 23	Request To Send-Active-LOW outputs - When the request-to-send ($\overline{RTS}$) bit in write register 5 (figure 7) is set, the $\overline{RTS}$ signal goes LOW. When the RTS bit is reset in the asynchronous mode and auto enable is on, the signal goes HIGH after the transmitter is empty. In synchronous mode or in asynchronous mode with auto enable off, the RTS pin strictly follows the state of the $\overline{RTS}$ bit. Both pins can be used as general-purpose outputs.
$\overline{SYNCA}$, $\overline{SYNCB}$	11, 29	Synchronization-Active-LOW inputs or outputs - These pins can act either as inputs or outputs, or part of the crystal oscillator circuit. In the asynchronous receive mode (crystal oscillator option not selected), these pins are inputs similar to $\overline{CTS}$ and $\overline{DCD}$. In this mode, transitions on these lines affect the state of the synchronous/hunt status bits in read register 0 (Figure 6) but have no other function. In external synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode, $\overline{SYNC}$ must be driven LOW to receive clock cycles after the last bit in the synchronous character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of $\overline{SYNC}$. In the internal synchronization mode (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which synchronous characters are recognized. The synchronous condition is not latched, so these outputs are active each time a synchronization pattern is recognized (regardless of character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag.
TxDA, TxDB	15, 25	Transmit Data-Active-HIGH outputs - These output signals transmit serial data at standard TTL levels.
$\overline{TRxCA}$, $\overline{TRxCB}$	14, 26	Transmit/Receive Clocks-Active-LOW inputs or outputs - These pins can be programmed in several different modes of operation. $\overline{TRxC}$ may supply the receive clock or the transmit clock in the input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.
$\overline{WR}$	35	Write-Active-LOW input - When the SCC is selected, this signal indicates a write operation. The coincidence of $\overline{RD}$ and $\overline{WR}$ is interpreted as a reset.
$\overline{W/REQA}$, $\overline{W/REQB}$	10, 30	Wait/Request-open-drain outputs when programmed for a wait function, driven HIGH or LOW when programmed for a Request function) - These dual-purpose outputs may be programmed as Request lines for a DMA controller or as Wait lines to synchronize the CPU to the SCC data rate. The reset state is Wait.

FUNCTIONAL DESCRIPTION

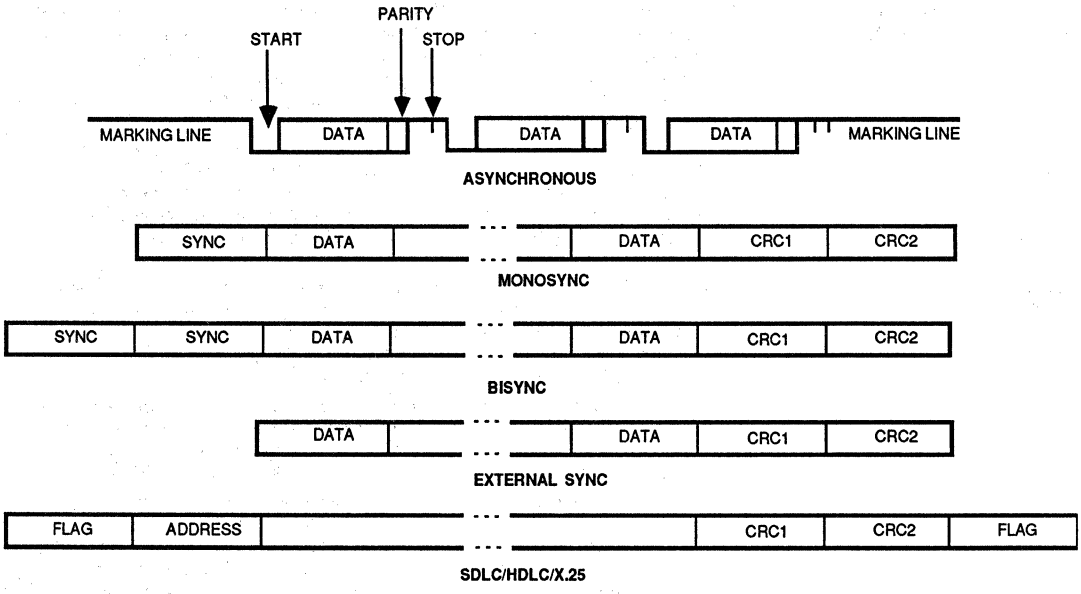
The functional capabilities of the SCC can be described from two different points of view. As a data communications device, it transmits and receives data in a wide variety of data communications protocols. As a microprocessor peripheral, the SCC offers SUCH valuable features as vectored interrupts, polling, and simple handshake capability.

DATA COMMUNICATIONS CAPABILITY

The SCC provides two independent full-duplex channels programmable for use in any common asynchronous or synchronous data communication protocol. Figure 1 and the following description briefly detail these protocols.

Asynchronous modes - Transmission and reception can be accomplished independently on each channel with 5 to 8 bits per character, plus optional

FIGURE 1. SCC PROTOCOLS



even or odd parity. The transmitters can supply 1, 1 1/2, or 2 stop bits per character and can provide a break output at any time. The receiver break-detection logic interrupts the CPU both at the start and at the end of a received break.

Reception is protected from spikes by a transient spike-rejection mechanism that checks the signal one-half a bit time after a LOW level is detected on the receive data input (RxDA or RxDB). If the LOW does not persist (as in the case of a transient), the character assembly process does not start.

Framing errors and overrun errors are detected and buffered together with the partial character on which they occur. Vectored interrupts allow fast servicing or error conditions using dedicated routines. Furthermore, a built-in checking process avoids the interpretation of a framing error as a new start bit: a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit begins.

The SCC does not require symmetric transmit and receive clock signals a feature allowing use of the wide variety of clock sources. The transmitter and receiver can handle data at a rate of 1, 1/16, 1/32, or 1/64 of the clock rate supplied to the receive and transmit clock inputs. In asynchronous modes, the $\overline{SYNC}$ pin may be programmed as an input used for such functions as monitoring a ring indicator.

Synchronous modes. The SCC supports both byte-oriented and bit-oriented synchronous communication. Synchronous byte-oriented protocols can be handled in several modes, allowing character synchronization with a 6-bit or 8-bit synchronous character (Monosync) any 12-bit synchronization pattern (Bisync), or with an external synchronous signal. Leading sync characters can be removed without interrupting the CPU.

5- or 7-bit synchronous characters are detected with 8- or 16-bit patterns in the SCC by overlapping the larger pattern across multple incoming synchronous characters.

The CRC checking for synchronous byte-oriented modes is delayed by one character time so that the CPU may disable CRC checking on specific characters. This permits the implementation of such protocols as IBM Bisync.

Both CRC-16 ($X^{16} + X^{15} + X^2 + 1$) and CCITT ($X^{16} + X^{12} + X^5 + 1$) error checking polynomials are supported. Either polynomial may be selected in all Synchronous modes. Users may preset the CRC generator and checker to all ones or all zeros. The SCC also pro-vides a feature that automatically transmits CRC data when no other data is available for transmission. This allows for high-speed transmissions under DMA control, with no need for CPU intervention at the end of a message. When there is no data or CRC to send in synchronous modes, the transmitter inserts 6-, 8-, or 16-bit synchronous characters, regardless of the programmed character length.

The SCC supports synchronous bit-oriented protocols, such as SDLC and HDLC, by performing automatic flag sending, zero insertion, and CRC generation. A special command can be used to abort a frame in transmission. At the end of a message, the SCC automatically transmits the CRC and trailing flag when the transmitter underruns. The transmitter may also be programmed to send an idle line consisting of continuous flag characters or a steady marking condition.

If a transmit underrun occurs in the middle of a message, an external/status interrupt warns the CPU of this status change so that an abort may be issued. The SCC may also be programmed to send an abort itself in case of an underrun, relieving the CPU of this task. One to eight bits per character can be sent, allowing reception of a message with no prior information about the character structure in the information field of a frame.

The receiver automatically acquires synchronization on the leading flag of a frame in SDLC or HDLC and provides a synchronization signal on the $\overline{SYNC}$ pin (an interrupt can also be programmed). The receiver can be programmed to search for frames addressed by a single byte (or four bits within a byte) of a user-selected address or to a global broadcast address. In this mode, frames not matching either the user-selected or broadcast address are ignored. The number of address bytes can be extended under software control. For receiving data, an interrupt on the first received character, or an interrupt on every character, or on special condition only (end-of-frame) can be selected. The receiver automatically deletes all zeros inserted by the transmitter during character assembly. The CRC is also calculated and is automatically checked to validate frame transmission. At the end of transmission, the status of a received frame is availabe in the status registers. In SDLC mode, the SCC must be programmed to use the SDLC CRC polynomial, but the generator and checker may be preset to all ones or all zeros.

The CRC is inverted before transmission and the receiver checks against the bit pattern 0001110100001111.

The NRZ, NRZI, or FM coding may be used in any 1x mode. The parity options available in asynchronous modes are available in synchronous modes.

The SCC can be conveniently used under DMA control to provide high-speed reception or transmission. In reception, for example, the SCC can interrupt the CPU when the first character of a message is received. The CPU then enables the DMA to transfer the message to memory. The SCC then issues an end-of-frame interrupt and the CPU can check the status of the received messsage.

Thus, the CPU is freed for other service while the message is being received. The CPU may also enable the DMA first and have the SCC interrupt only on end-of-frame. This procedure allows all data to be transferred via the DMA.

SDLC LOOP MODE

The SCC supports SDLC loop mode in addition to normal SDLC. In an SDLC loop, there is a primary controller station that manages the message traffic flow on the loop and any number of secondary stations. In SDLC loop mode, the SCC performs the functions of a secondary station while an SCC operating in regular SDLC mode can act as a controller (Figure 3).

A secondary station in an SDLC Loop is always listening to the messages being sent around the loop, and in fact must pass these messages to the rest of the loop by retransmitting them with a one-bit time delay. The secondary station can place its own message on the loop only at specific times. The controller signals that secondary stations may transmit messages by sending a special character, called an End Of Poll (EOP), around the loop. The EOP character is the bit pattern 11111110. Because of zero insertion during messages, this bit pattern is unique and easily recognized.

When a secondary station has a message to transmit and recognizes an EOP on the line, it changes the last binary 1 of the EOP to a 0 before transmission. This has the effect of turning the EOP into a flag sequence. The secondary station now places its message on the loop and terminates the message with an EOP. Any secondary stations further down the loop with messages to transmit can then append their messages to the message of the first secondary station without messages to send merely echo the incoming messages and are prohibited from placing messages on the loop (except upon recognizing an EOP).

The SDLC loop mode is a programmable option in the SCC. NRZ, NRZI, and FM coding may all be used in SDLC Loop mode.

BAUD RATE GENERATOR

Each channel in the SCC contains a programmable baud rate generator. Each generator consists of two 8-bit time-constant registers that form a 16-bit time constant, a 16-bit down counter, and a flip-flop on the output producing a square wave. On startup, the flip-flop on the output is set in a HIGH state, the value in the time constant register is loaded into the counter, and the counter starts counting down. The output of the baud generator toggles upon reaching 0, the value in the time constant register is loaded into the counter, and the process is repeated. The time constant may be changed at any time, but the new value does not take effect until the next load of the counter.

The output of the baud rate generator may be used as either the transmit clock, the receive clock, or both. It can also drive the digital phase-locked loop (see next section).

If the receive clock or transmit clock is not programmed to come from the $\overline{\text{TRxC}}$ pin, the output of the baud rate generator may be echoed out via the $\overline{\text{TRxC}}$ pin.

The following formula relates the time constant to the baud rate (the baud rate is in bits/second and BR clock period is in seconds):

$$\text{baud rate} = \frac{1}{2\,(\text{time constant}+2) \times (\text{BR clock period})}$$

DIGITAL PHASE-LOCKED LOOP

The SCC contains a digital phase-locked-loop (DPLL) to recover clock information from a data stream with NRZI or FM encoding. The DPLL is driven by a clock that is nominally 32 (NRZI) or 16 (FM) times the data rate. The DPLL uses this clock, along with the data stream, to construct a clock for the data. This clock may then be used as the SCC receive clock, the transmit clock, or both.

FIGURE 2. DETECTING 5- OR 7-BIT SYNCHRONOUS CHARACTERS

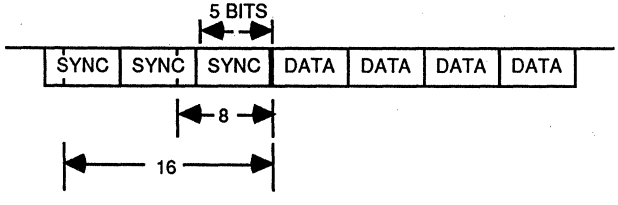
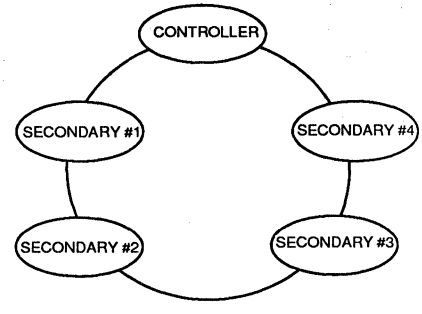


FIGURE 3. AN SDLC LOOP



For NRZI encoding, the DPLL counts the 32x clock to create nominal bit times. As the 32x clock is counted, the DPLL is searching the incoming data stream for edges (either 1 to 0 or 0 to 1). Whenever an edge is detected, the DPLL makes a count adjustment (during the next counting cycle), producing a terminal count closer to the center of the bit cell.

For FM encoding, the DPLL still counts from 0 to 31, but with a cycle corresponding to two bit times. When the DPLL is locked, the clock edges in the data stream should occur between counts 15 and 16, and between counts 31 and 0. The DPLL looks for edges only during a time centered on the 15 to 16 counting transition.

The 32x clock for the DPLL can be programmed to come from either the $\overline{\text{RTxC}}$ input or the output of the baud rate generator. The DPLL output may be programmed to be echoed out of the SCC via the $\overline{\text{TRxC}}$ pin (if this pin is not being used as an input).

DATA ENCODING

The SCC may be programmed to encode and decode the serial data in four different ways (Figure 4). In NRZ encoding, a 1 is represented by a HIGH level and a 0 is represented by a LOW level. In NRZI encoding, a 1 is represented by no change in level and a 0 is represented by a change in level.

In FM1 (more properly, bi-phase mark), a transition occurs at the beginning of every bit cell. A 1 is represented by an additional transition at the center of the bit cell and a 0 is represented by no additional transition at the center of the bit cell. In FMØ (bi-phase space), a transition occurs at the beginning of every bit cell. A 0 is represented by an additional transition at the center of the bit cell, and a 1 is represented by no additional transition at the center of the bit cell.

In addition to these four methods, the SCC can be used to decode Manchester (bi-phase level) data by using the DPLL in the FM mode and programming the receiver for NRZ data. Manchester encoding always produces a transition at the center of the bit cell. If the transition is 0 to 1, the bit is a 0. If the transition is 1 to 0, the bit is a 1.

AUTO ECHO AND LOCAL LOOPBACK

The SCC is capable of automatically echoing everything it receives. This feature is useful mainly in asynchronous modes, but works in synchronous and SDLC modes as well. In auto echo mode, TxD is RxD. Auto Echo mode can be used with NRZI or FM encoding with no additional delay, because the data stream is not decoded before retransmission. In auto echo mode, the $\overline{\text{CTS}}$ input is ignored as a transmitter enable (although transitions on this input can still cause interrupts if programmed to do so). In this mode, the transmitter is actually bypassed and the programmer is responsible for disabling transmitter interrupts and Wait/Request on transmit.

The SCC is also capable of local loopback. In this mode TxD is RxD, just as in auto echo mode. However, in local loopback mode, the internal transmit data is tied to the internal receive data and RxD is ignored (except to be echoed out via TxD). The $\overline{\text{CTS}}$ and $\overline{\text{DCD}}$ inputs are also ignored as transmit and receive enables. However, transitions on these inputs can still cause interrupts. Local Loopback works in asynchronous, synchronous and SDLC modes with NRZ, NRZI or FM coding of the data stream.

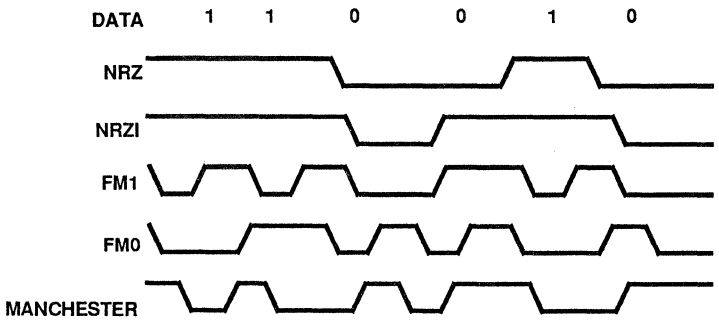
I/O INTERFACE CAPABILITIES

The SCC offers the choice of polling, interrupt (vectored or nonvectored), and block transfer modes to transfer data, status, and control information to and from the CPU. The block transfer mode can be implemented under CPU or DMA control.

POLLING

All interrupts are disabled. Three status registers in the SCC are automatically updated whenever any function is performed . For example, end-of-frame in SDLC mode sets a bit in one of these status registers. The idea behind polling is for the CPU to periodically read a status register until the register contents indicate the need for data to be transferred. Only one register needs to be read; depending on its contents, the CPU either writes data, reads data, or continues. Two bits in the register indicate the need for data transfer.

FIGURE 4. DATA ENCODING METHODS



An alternative is a poll of the Interrupt Pending register to determine the source of an interrupt. The status for both channels resides in one register.

INTERRUPTS

When an SCC responds to an Interrupt Acknowledge signal ($\overline{INTACK}$) from the CPU, an interrupt vector may be placed on the data bus. This vector is written in Write Register 2 (WR2) and may be read in Read Register 2A (RR2A) or Read Register 2B (RR2B) (Figures 6 and 7).

To speed interrupt response time, the SCC can modify three bits in this vector to indicate status. If the vector is read in Channel A, status is never included; if it is read in Channel B, status is always included.

Each of the six sources of interrupts in the SCC (Transmit, Receive, and External/Status interrupts in both channels) has three bits associated with the interrupt source: Interrupt Pending (IP), Interrupt Under Service (IUS), and Interrupt Enable (IE). Operation of the IE bit is straightforward. If the IE bit is set for a given interrupt source, that source can request interrupts. The exception is when the MIE (Master Interrupt Enable) bit in WR9 is reset and no interrupts may be requested. The IE bits are write only.

The other two bits are related to the interrupt priority chain (Figure 5). As a microprocessor peripheral, the SCC may request an interrupt only when no higher priority device is requesting one; e.g., when IEI is HIGH. If the device in question requests an interrupt, it pulls down $\overline{INT}$. The CPU then responds with $\overline{INTACK}$, and the interrupting device places the vector on the data bus.

In the SCC, the IP bit signals a need for interrupt servicing. When an IP bit is 1 and the IEI input is HIGH, the $\overline{INT}$ output is pulled LOW, requesting an interrupt. In the SCC, if the IE bit is not set by enabling interrupts, then the IP for that source can never be set. The IP bits are readable in RR3A.

The IUS bits signal that an interrupt request is being serviced. If an IUS is set, all interrupt sources of lower priority in the SCC and external to the SCC are prevented from requesting interrupts. The internal interrupt sources are inhibited by the state of the internal daisy chain, while lower priority devices are inhibited by the IEO output of the SCC being pulled LOW and propagated to subsequent peripherals. An IUS bit is set during an interrupt acknowledge cycle if there are no higher priority devices requesting interrupts.

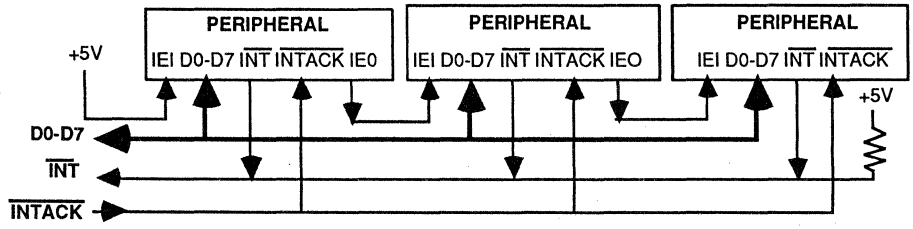
There are three types of interrupts: transmit, receive, and external/status. Each interrupt type is enabled under program control with Channel A having higher priority than Channel B, and with receive, transmit, and external/status interrupts prioritized in that order within each channel. When the transmit interrupt is enabled, the CPU is interrupted when the transmit buffer becomes empty. (This implies that the transmitter must have had a data character written into it so that it can become empty.) When enabled, the receiver can interrupt the CPU in one of three ways:

- On first receive character or special receive condition
- On all receive characters or special receive condition
- On special receive condition only

Interrupt on first character or special condition and interrupt on special condition only are typically used with the block transfer mode. A special receive condition is one of the following: receiver overrun, framing error in asynchronous mode, end-of-frame in SDLC mode and, optionally, a parity error. The special receive condition interrupt is different from an ordinary receive character interrupt only in that the status is placed in the vector during the interrupt acknowledge cycle. In interrupt on first receive character, an interrupt can occur from special receive conditions any time after the first receive character interrupt.

The main function of the external/status interrupt is to monitor the signal transitions of the $\overline{CTS}$, $\overline{DCD}$, and $\overline{SYNC}$ pins; however, an external/status interrupt is also caused by a transmit underrun condition, or a zero count in the baud rate generator, or by the detection of a break (asynchronous mode), Abort (SDLC mode) or EOP (SDLC loop mode) sequence in the data stream.

FIGURE 5. INTERRUPT SCHEDULE



The interrupt caused by the abort or EOP has a special feature allowing the SCC to interrupt when the abort or EOP sequence is detected or terminated. This feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the Abort condition in external logic in SDLC mode. In SDLC ioop mode, this feature allows secondary stations to recognize the wishes of the primary station to regain control of the loop during a poll sequence.

CPU/DMA BLOCK TRANSFER

The SCC provides a block transfer mode to accommodate CPU block transfer functions and DMA controllers. The block transfer mode uses the Wait/Request output in conjunction with the Wait/Request bits in WR1. The Wait/Request output can be defined under software control as a WAIT line in the CPU Block Transfer mode or as a REQUEST line in the DMA block bransfer mode.

To a DMA controller, the SCC REQUEST output indicates that the SCC is ready to transfer data to or from memory. To the CPU, the WAIT line indicates that the SCC is not ready to transfer data, thereby requesting that the CPU extend the I/O cycle. The DTR/REQUEST line allows full-duplex operation under DMA control.

PROGRAMMING

The SCC contains 13 write registers in each channel that are programmed by the system separately to configure the functional personality of the channels.

In the SCC, register addressing is direct for the data registers only, which are selected by a HIGH on the D/$\overline{C}$ pin. In all other cases (with the exception of WR0 and RR0), programming the write registers requires two write operations and reading the read registers requires both a write and a read operation. The first write is to WR0 and contains three bits that point to the selected register. The second write is the actual control word for the selected register, and if the second operation is read, the selected read register is accessed. All of the registers in the SCC, including the data registers, may be accessed in this fashion. The pointer bits are automatically cleared after the read or write operation so that WR0 (or RR0) is addressed again.

The system program first issues a series of commands to initialize the basic mode of operation. This is followed by other commands to qualify conditions within the selected mode. For example, the asynchronous mode, character length, clock rate, number of stop bits, and even or odd parity might be set first. Then the interrupt mode would be set, and, finally, receiver or trans-mitter enable.

READ REGISTERS

The SCC contains eight read registers (nine counting receive buffer RR8) in each channel. Four of these may be read to obtain status information (RR0, RR1, RR10, and RR15). Two registers (RR12 and RR13) may be read to learn the baud rate generator time constant. The RR2 contains either the unmodified interrupt vector (Channel A) or the vector modified by status information (Channel B). The RR3 contains the Interrupt Pending (IP) bits (Channel A). Figures 6 through 13 show the formats for each read register.

The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring; e.g., when the interrupt vector indicates a special receive Condition interrupt, all the appropriate error bits can be read from a single register (RR1).

WRITE REGISTERS

The SCC contains 13 write registers (14 counting the WR8 transmit buffer) in each channel. These write registers are programmed separately to configure the functional personality of the channels. In addition, there are two registers (WR2 and WR9) shared by the two channels that may be accessed through either of them; WR2 contains the interrupt vector for both channels, while WR9 contains the interrupt control bits. Figures 14 through 28 show the format of each write register.

TIMING

The SCC generates internal control signals from $\overline{WR}$ and $\overline{RD}$ that are related to PCLK. Since PCLK has no phase relationship with $\overline{WR}$ and $\overline{RD}$, the circuitry generating these internal control signals must provide time for metastable conditions to disappear. This gives rise to a recovery time related to PCLK. The recovery time applies only between bus transactions involving the SCC. The recovery time required for proper operation is specified from the rising edge of $\overline{WR}$ or $\overline{RD}$ in the first transaction involving the SCC, to the falling edge of $\overline{WR}$ or $\overline{RD}$ in the second transaction involving the SCC. This time must be at least six PCLK cycles plus 200 ns.

READ CYCLE TIMING

Figure 29 illustrates Read cycle timing. Addresses on A/B and D/C and the status on $\overline{INTACK}$ must remain stable through the cycle. If $\overline{CE}$ falls after $\overline{RD}$ falls, or if it rises before $\overline{RD}$ rises, the effective $\overline{RD}$ is shortened.

WRITE CYCLE TIMING

Figure 30 illustrates Write cycle timing. Addresses on A/$\overline{B}$ and D/$\overline{C}$ and the status on $\overline{INTACK}$ must remain stable throughout the cycle. If $\overline{CE}$ falls after $\overline{WR}$ falls, or if it rises before $\overline{WR}$ rises, the effective $\overline{WR}$ is shortened.

INTERRUPT ACKNOWLEDGE CYCLE TIMING

Figure 31 illustrates Interrupt Acknowledge cycle timing. Between the time $\overline{INTACK}$ goes LOW and the falling edge of $\overline{RD}$, the internal and external IEI/IEO daisy chains settle. If there is an interrupt pending in the SCC and IEI is HIGH when $\overline{RD}$ falls, the Acknowledge cycle is intended for the SCC. In this case, the SCC may be programmed to respond to $\overline{RD}$ LOW by placing its interrupt vector on D0-D7, and it then internally sets the appropriate Interrupt-Under-Service latch.

FIGURE 6. READ REGISTER 0

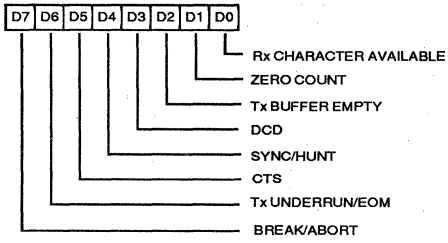


FIGURE 7. READ REGISTER 1

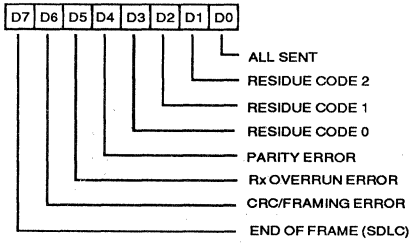


FIGURE 8. READ REGISTER 2

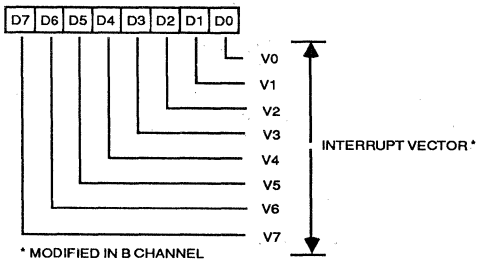


FIGURE 9. READ REGISTER 3

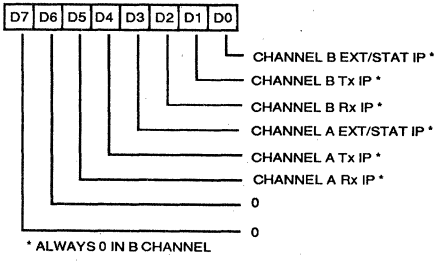


FIGURE 10. READ REGISTER 10

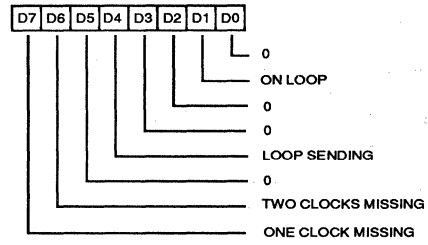


FIGURE 11. READ REGISTER 12

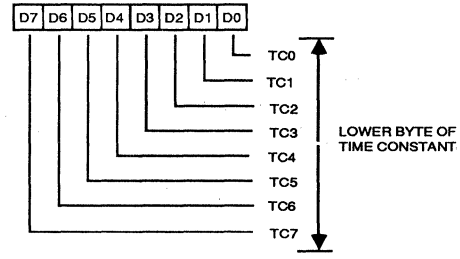


FIGURE 12. READ REGISTER 13

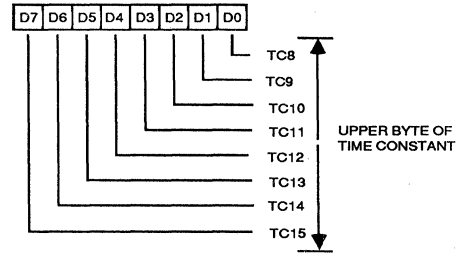


FIGURE 13. READ REGISTER 15

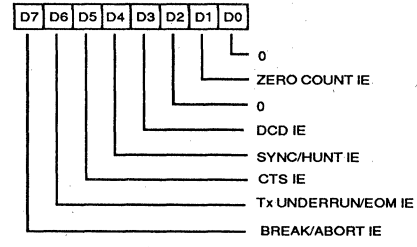


FIGURE 14. WRITE REGISTER 0

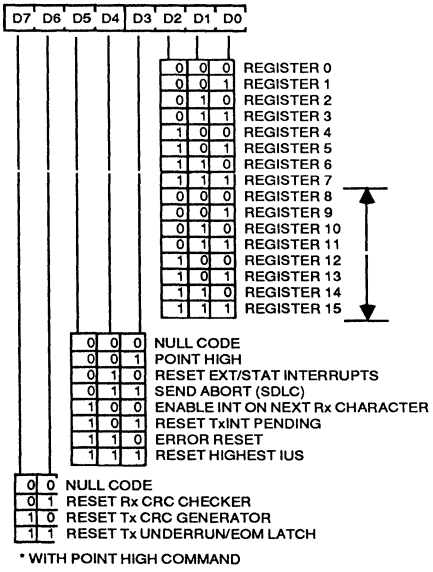


FIGURE 15. WRITE REGISTER 1

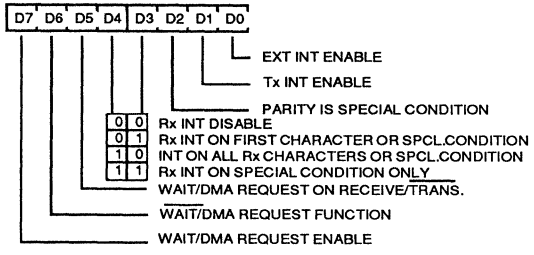


FIGURE 16. WRITE REGISTER 2

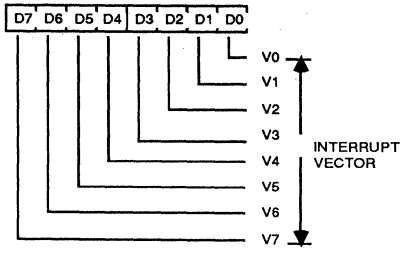


FIGURE 17. WRITE REGISTER 3

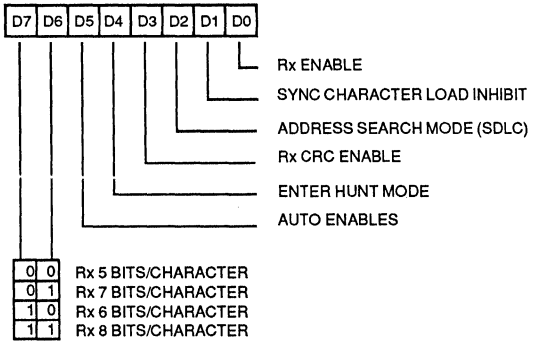


FIGURE 18. WRITE REGISTER 4

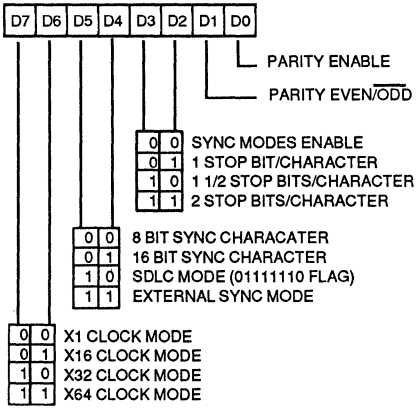


FIGURE 19. WRITE REGISTER 5

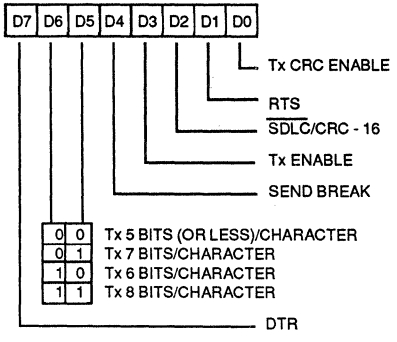


FIGURE 20. WRITE REGISTER 6

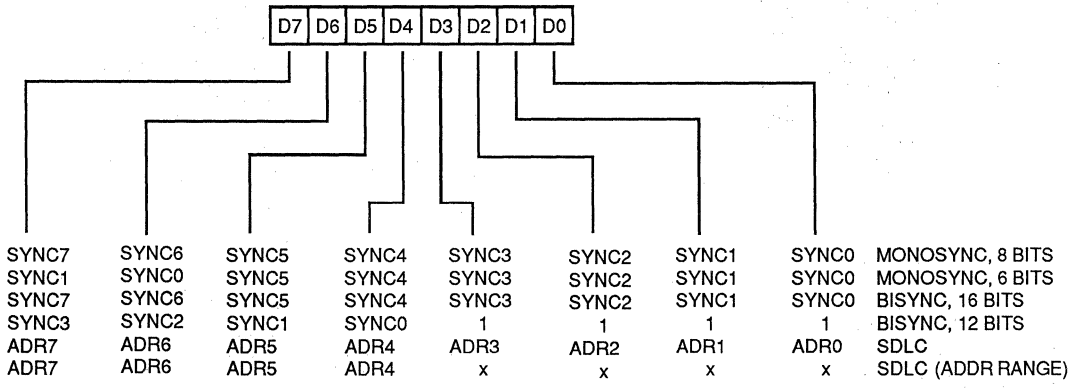


FIGURE 21. WRITE REGISTER 7

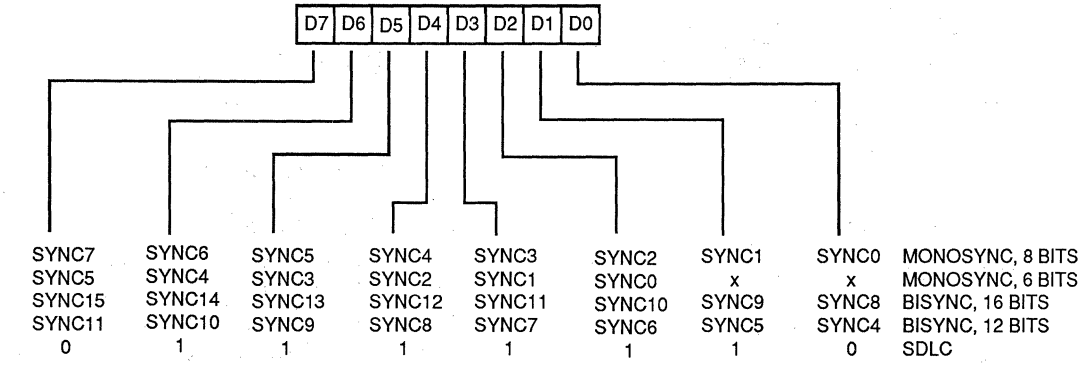


FIGURE 22. WRITE REGISTER 9

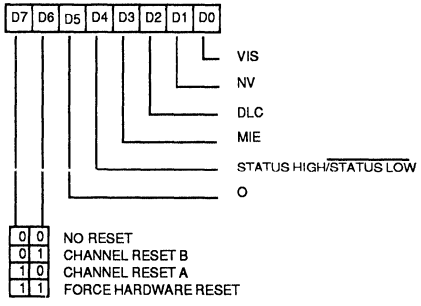


FIGURE 23. WRITE REGISTER 10

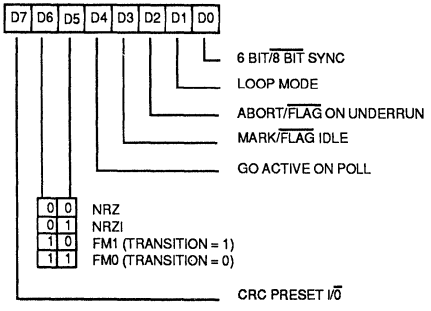


FIGURE 24. WRITE REGISTER 11

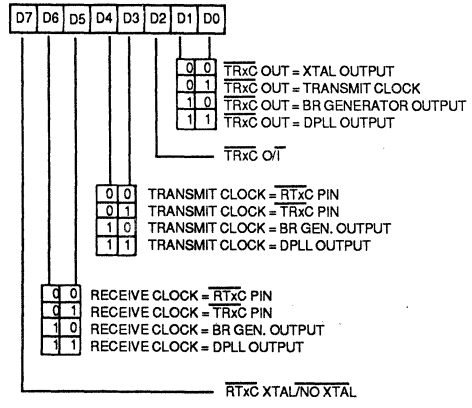


FIGURE 25. WRITE REGISTER 12

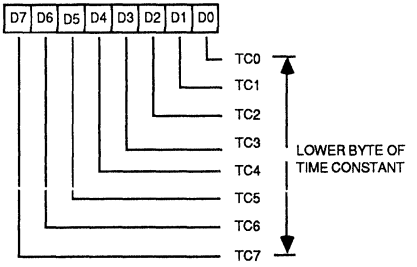


FIGURE 26. WRITE REGISTER 13

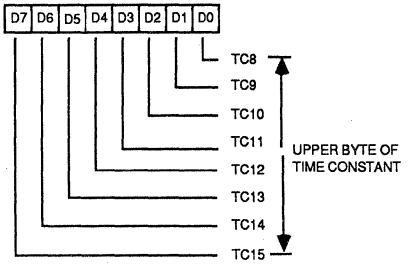


FIGURE 27. WRITE REGISTER 14

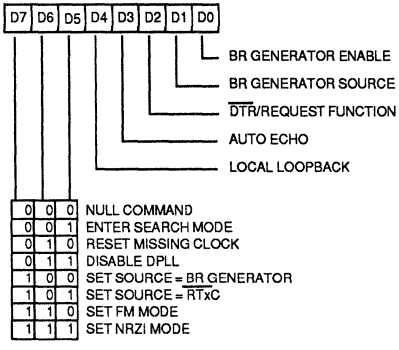


FIGURE 28. WRITE REGISTER 15

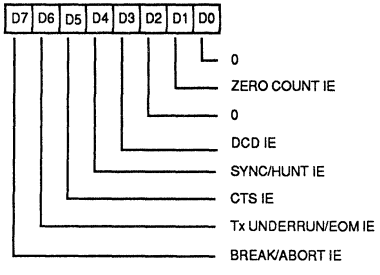


FIGURE 29. READ CYCLE TIMING

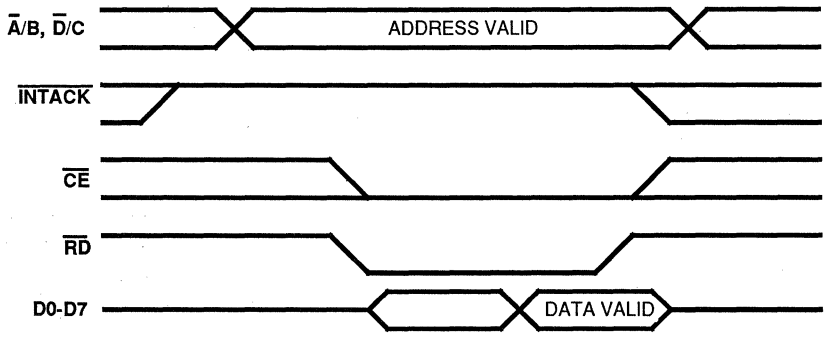


FIGURE 30. WRITE CYCLE TIMING

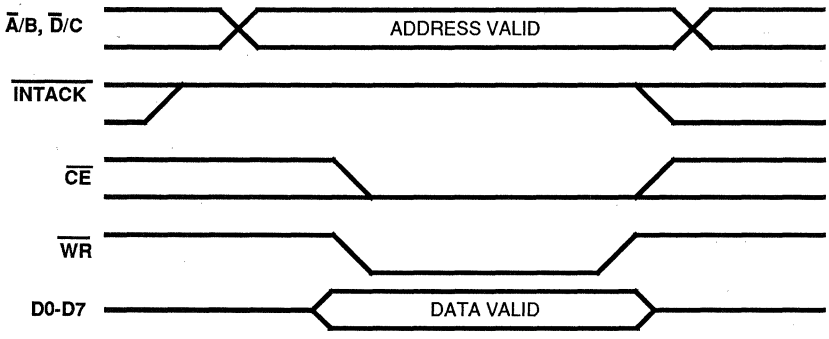


FIGURE 31. INTERRUPT ACKNOWLEDGE CYCLE TIMING

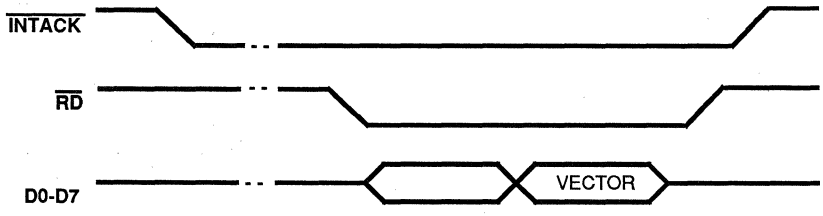


FIGURE 33. READ AND WRITE TIMING (SEE TABLE 1)

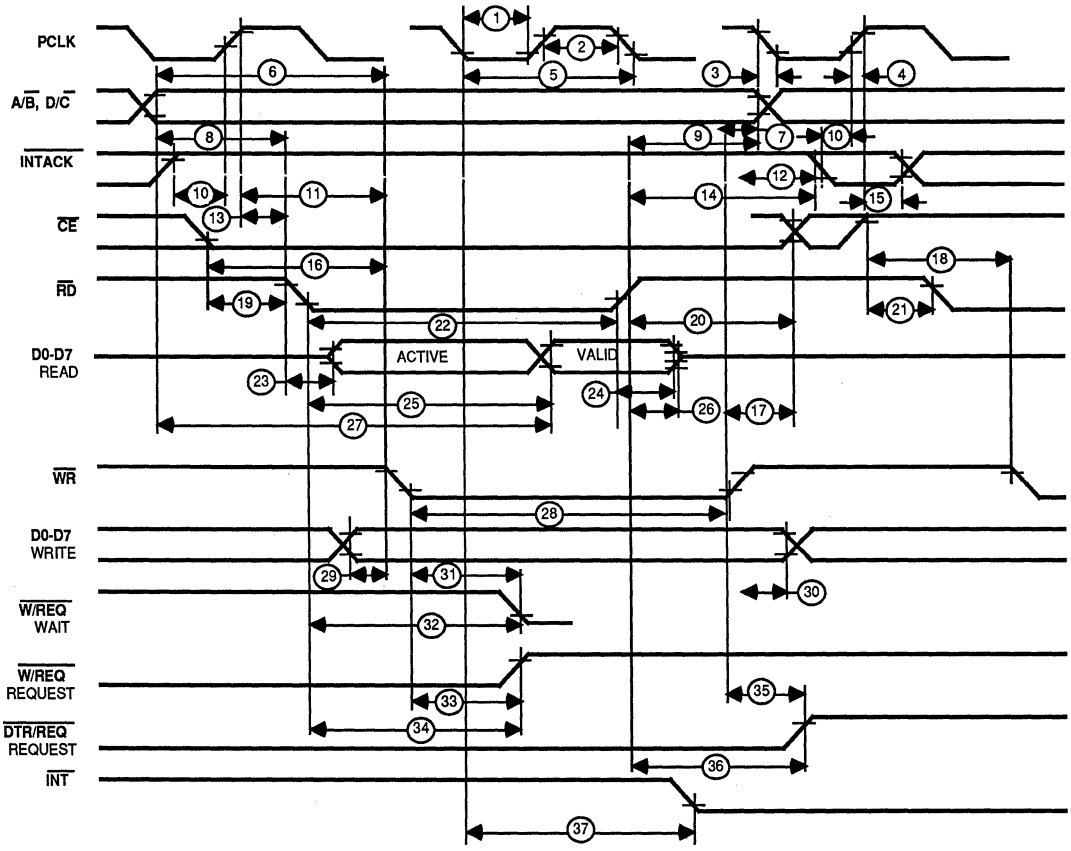


FIGURE 34. RESET TIMING (SEE TABLE 1)

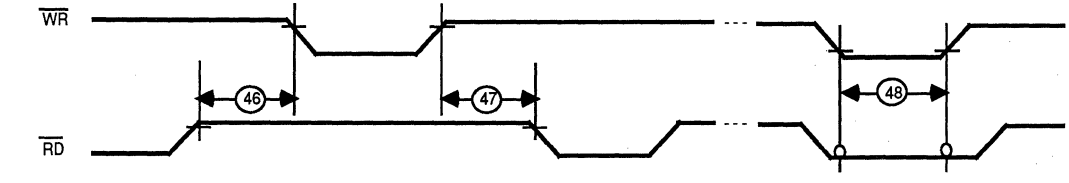


FIGURE 35. CYCLE TIMING (SEE TABLE 1.)

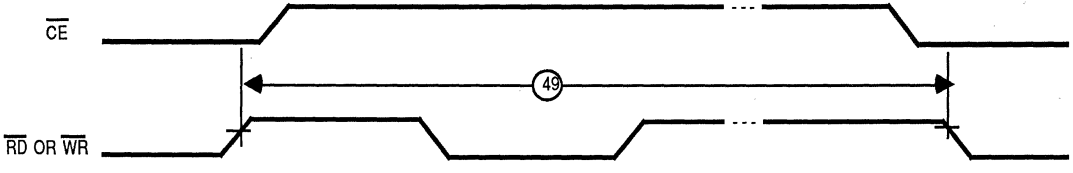


TABLE 1. READ AND WRITE TIMING

No.	Symbol	Parameter	4MHz		6MHz		
			Min	Max	Min	Max	Notes
1	TwPCl	PCLK LOW Width	105	2000	70	1000	
2	TwPCh	PCLK HIGH Width	105	2000	70	1000	
3	TfPC	PCLK Fall Time		20		10	
4	TrPC	PCLK Rise Time		20		15	
5	TcPC	PCLK Cycle Time	250	4000	165	2000	
6	TsA(WR)	Address to $\overline{WR}$ Setup Time	80		80		
7	ThA(WR)	Address to $\overline{WR}$ Hold Time	0		0		
8	TsA(RD)	Address to $\overline{RD}$ Setup Time	80		80		
9	ThA(RD)	Address to $\overline{RD}$ Hold Time	0		0		
10	TslA(PC)	$\overline{INTACK}$ to PCLK Setup Time	0		0		
11	TslAi(WR)	$\overline{INTACK}$ to $\overline{WR}$ Setup Time	200		160		2
12	ThIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ Hold Time	0		0		
13	TslAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ Setup Time	200		160		2
14	ThIA(RD)	$\overline{INTACK}$ to $\overline{RD}$ Hold Time	0		0		
15	ThIA(PC)	$\overline{INTACK}$ to PCLK Hold Time	100		100		
16	TsCE1(WR)	$\overline{CE}$ LOW to $\overline{WR}$ Setup Time	0		0		
17	ThCE(WR)	$\overline{CE}$ to $\overline{WR}$ Hold Time	0		0		
18	TsCEh(WR)	$\overline{CE}$ HIGH to $\overline{WR}$ Setup Time	100		70		2
19	TsCE1(RD)	$\overline{CE}$ LOW to $\overline{RD}$ Setup Time	0		0		2
20	ThCE(RD)	$\overline{CE}$ to $\overline{RD}$ Hold Time	0		0		2
21	TsCEh(RD)	$\overline{CE}$ HIGH to $\overline{RD}$ Setup Time	100		70		2
22	TwRD1	$\overline{RD}$ LOW Width	390		250		
23	TdRD(DRA)	$\overline{RD}$ to Read Data Active Delay	0		0		
24	TdRDr(DR)	$\overline{RD}$ to Read Data Not Valid Delay	0		0		
25	TdRDf(DR)	$\overline{RD}$ to Read Data Valid Delay		250		180	
26	TdRD(DRz)	$\overline{RD}$ to Read Data Float Delay		70		45	3
27	TdA(DR)	Address Required Valid to Read Data Valid Delay		590		420	
28	TwWR1	$\overline{WR}$ LOW Width	390		250		
29	TsDW(WR)	Write Data to $\overline{WR}$ Setup Time	0		0		
30	ThDW(WR)	Write Data to $\overline{WR}$ Hold Time	0		0		
31	TdWR(W)	$\overline{WR}$ to Wait Valid Delay		240		200	5
32	TdRD(W)	$\overline{RD}$ to Wait Valid Delay		240		200	5
33	TdWRf(REQ)	$\overline{WR}$ to W/$\overline{REQ}$ Not Valid Delay		240		200	
34	TdRDf(REQ)	$\overline{RD}$ to W/$\overline{REQ}$ Not Valid Delay		240		200	
35	TdWRr(REQ)	$\overline{WR}$ to DTR/$\overline{REQ}$ Not Valid Delay		(5TcPC +300)		(5TcPC +250)	
36	TdRDr(REQ)	$\overline{RD}$ to DTR/$\overline{REQ}$ Not Valid Delay		(5TcPC +300)		(5TcPC +250)	
37	TdPC(INT)	PCLK to $\overline{INT}$ Valid Delay		500		500	5
38	TdIAi(RD)	$\overline{INTACK}$ to RD (Acknowledge) Delay	250		250		6
39	TwRDA	$\overline{RD}$ (Acknowledge) Width	285		250		
40	TdRDA(DR)	$\overline{RD}$ (Ack.) to Read Data Valid Delay		190		180	
41	TslEI(RDA)	IEI to $\overline{RD}$ (Acknowledge) Setup Time	120		100		
42	ThIEI(RDA)	IEI to $\overline{RD}$ (Acknowledge) Hold Time	0		0		
43	TdIEI(IEO)	IEI to IEO Delay Time		120		100	
44	TdPC(IEO)	PCLK to IEO Delay		250		250	
45	TdRDA(INT)	$\overline{RD}$ to $\overline{INT}$ Inactive Delay		500		500	5
46	TdRD(WRQ)	$\overline{RD}$ to $\overline{WR}$ Delay for No Reset	30		15		
47	TdWRQ(RD)	$\overline{WR}$ to $\overline{RD}$ Delay for No Reset	30		30		
48	TwRES	$\overline{WR}$ and $\overline{RD}$ Coincident Low for Reset	250		250		
49	Trc	Valid Access Recovery Time	(6TcPC +200)		(6TcPC +130)		

READ AND WRITE TIMING (NOTES)

1. Units are in nanoseconds.
2. Parameter does not apply to Interrupt Acknowledge transactions.
3. Float delay is defined as the time required for a ±0.5 V change at the output with a maximum dc load and minimum ac load.
4. Parameter applies only between transactions involving the SCC.
5. Open-drain output, measured with open-drain test load.
6. Parameter is system dependent. For any SCC in the daisy chain, TdIAi(RD) must be greater than the sum of TdPC(IEO) for the highest priority device in the daisy chain, TsIEI(RDA) for the SCC, and TdIEIf(IEO) for each device separating them in the daisy chain.

FIGURE 36. INTERRUPT ACKNOWLEDGE TIMING (SEE TABLE 1)

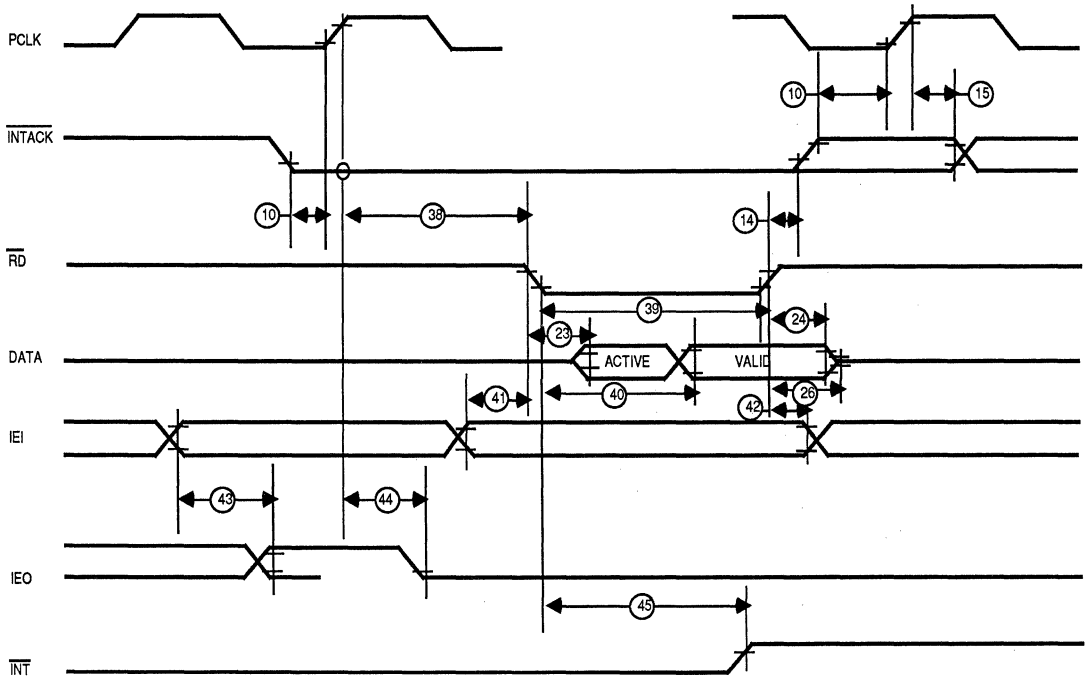


FIGURE 37. GENERAL TIMING (SEE TABLE 2)

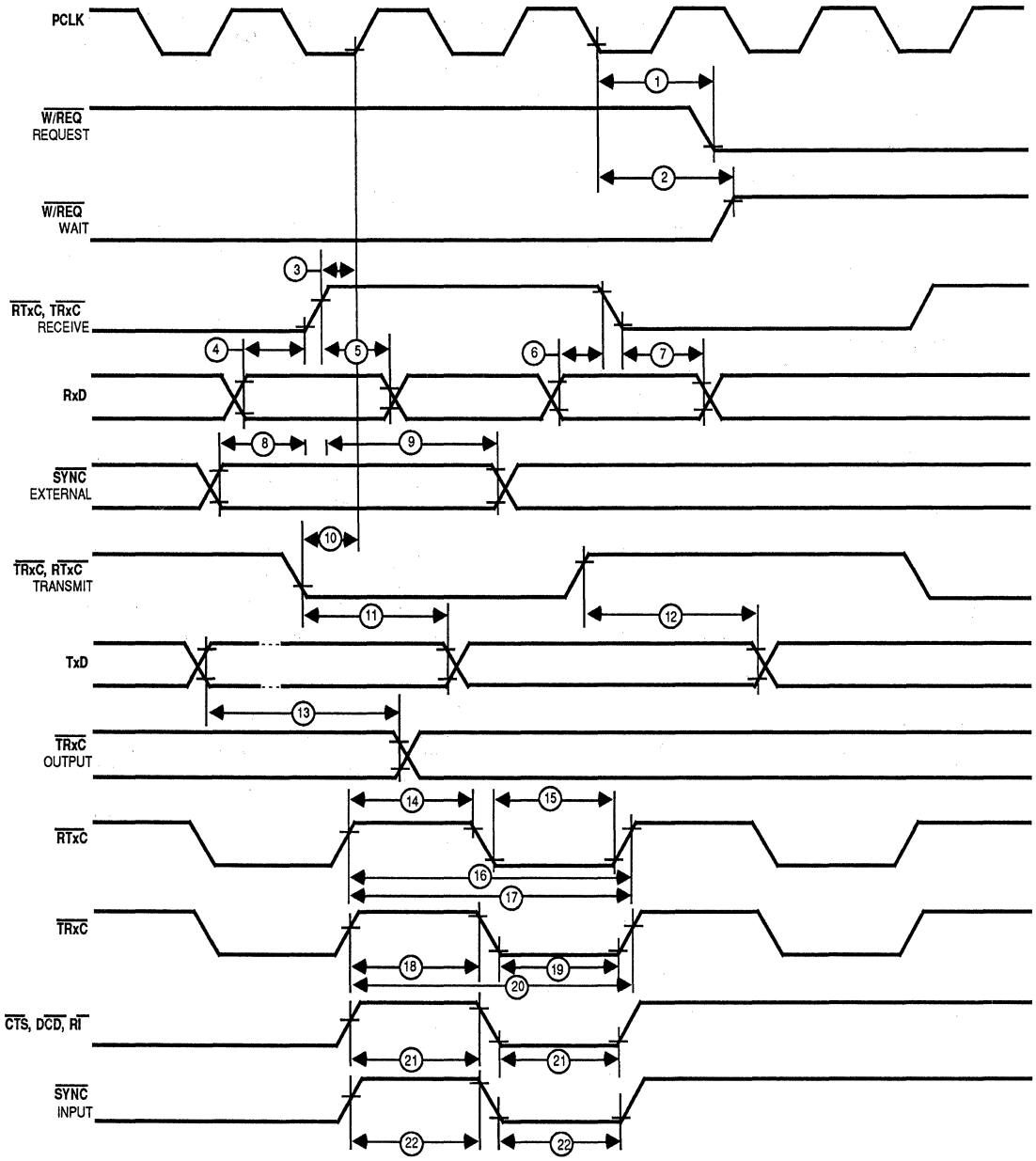


TABLE 2. GENERAL TIMING

No.	Symbol	Parameter	4 MHz		6 MHz		
			Min*	Max*	Min*	Max*	Notes
1	TdPC(REQ)	PCLK to W/REQ Valid Delay		250		250	
2	TdPC(W)	PCLK to Wait Inactive Delay		350		350	
3	Ts RXC(PC)	RxC to PCLK Setup Time (PCLK ÷ 4 Case Only)	80	TwPC1	70	TwPC1	2,5
4	TsRXD(RXCr)	RxD to RxC Setup Time (X1 Mode)	0		0		2
5	ThRXD(RXCr)	RxD to RxC Hold Time (X1 Mode)	150		150		2
6	TsRXD(RXCf)	RxD to RxC Setup Time (X1 Mode)	0		0		2,6
7	ThRXD(RXCf)	RxD to RxC Hold Time (X1 Mode)	150		150		2,6
8	TsSY(RXC)	SYNC to RxC Setup Time	-200		-200		4,2
9	ThSY(RXC)	SYNC to RxC Hold Time	3TcPC +200		3TcPC +200		4, 2
10	TsTXC(PC)	TxC to PCLK Setup Time	0		0		3,5
11	TdTXCf(TXD)	TxC to TxD Delay (X1 Mode)		300		230	3
12	TdTXCr(TXD)	TxC to TxD Delay (X1 Mode)		300		230	3,5
13	TdTXD(TRX)	TxD to TRxC Delay (Send Clock Echo)		200		200	
14	TwRTXh	RTxC HIGH Width	180		180		7
15	TwRTXl	RTxC LOW Width	180		180		7
16	TcRTX	RTxC Cycle Time	400		400		7
17	TcRTXX	Crystal Oscillator Period	250	1000	250	1000	3
18	TwTRXh	TRxC HIGH Width	180		180		4,7
19	TwTRXl	TRxC LOW Width	180		180		4,7
20	TcTRX	TRxC Cycle Time	400		400		4, 7
21	TwEXT	DCD or CTS Pulse Width	200		200		
22	TwSY	SYNC Pulse Width	200		200		

TABLE 3. SYSTEM TIMING

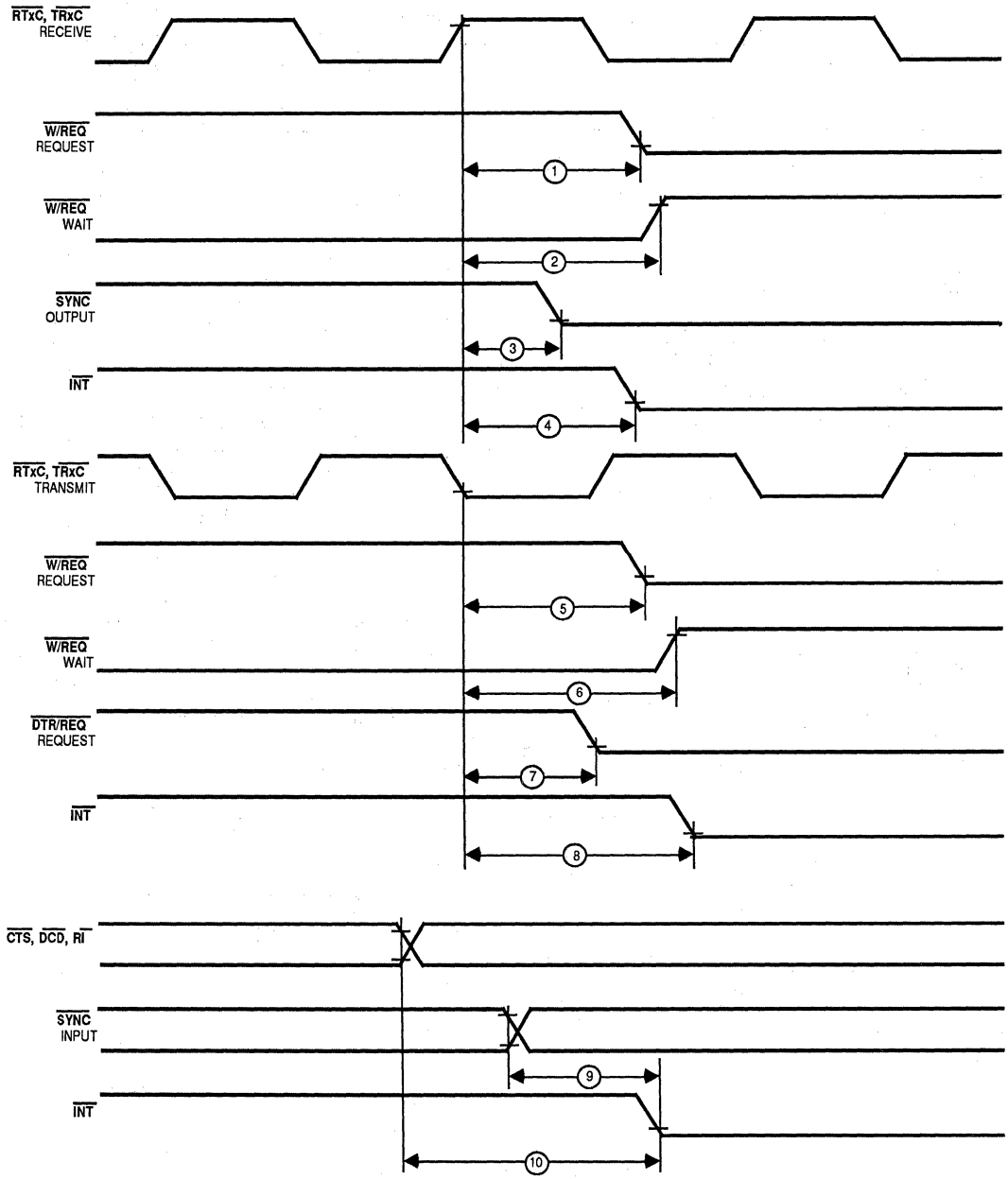
No.	Symbol	Parameter	4 MHz		6 MHz		
			Min*	Max*	Min*	Max*	Notes
1	TdRXC(REQ)	RxC to W/REQ Valid Delay	8	12	8	12	2
2	TdRXC(W)	RxC to Wait Inactive Delay	8	12	8	12	1,2
3	TdRXC(SY)	RxC to SYNC Valid Delay	4	7	4	7	2
4	TdRXC(INT)	RxC to INT Valid Delay	10	16	10	16	1,2
5	TdTXC(REQ)	TxC to W/REQ Valid Delay	5	8	5	8	3
6	TdTXC(W)	TxC to Wait Inactive Delay	5	8	5	8	1,3
7	TdTXC(DRQ)	TxC to DTR/REQ Valid Delay	4	7	4	7	3
8	TdTXC(INT)	TxC to INT Valid Delay	6	10	6	10	1,3
9	TdSY(INT)	SYNC Transition to INT Valid Delay	2	6	2	6	1
10	TdEXT(INT)	DCD or CTS Transition to INT Valid Delay	2	6	2	6	1

General and System Timing Notes:

1. Open-drain output, measured with open-drain test load.
2. RxC is RTxC or TRxC, whichever is supplying the transmit clock.
3. TxC is TRxC or RTxC, whichever is supplying the transmit clock.
4. Both TrxC and SYNC have 30 pF capacitors to ground connected to them.
5. Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between RxC and PCLK or TxC and PCLK is required.
6. Parameter applies only to FM encoding/decoding.
7. Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to chip PCLK requirements.

* Units are in nanoseconds (ns).

FIGURE 38. SYSTEM TIMING (SEE TABLE 3)



ABSOLUTE MAXIMUM RATINGS

Voltages on all pins with respect to GND	-0.3V to + 7.0V
Operating Ambient Temperature	0°C to 70°C
Storage Temperature	-65°C to + 150°C

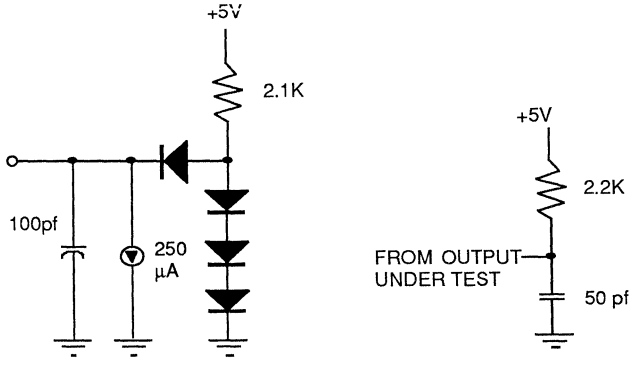
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those listed on the operational sections of this specification is not implied and exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The dc characteristics and capacitance section below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin.

Standard conditions are as follows:

- +4.75 V ≤ Vcc ≤ +5.25 V
- GND = O V
- TA as specified in Ordering Information



DC CHARACTERISTICS: VCC = 5 V ± 5%, TA = 0°C to 70°C

Symbol	Parameter	Min	Max	Unit	Conditions
VIH	Input High Voltage	2.0	VCC + 0.3	V	
VIL	Input Low Voltage	-0.3	0.8	V	
VOH	Ouput High Voltage	2.4		V	I_{OH} = -250 µA
VOL	Output Low Voltage		0.4	V	I_{OH} = +2.0 mA
IIL	Input Leakage		±10.0	µA	0.4 V ≤ V_{IN} ≤ +2.4 V
IOL	Output Leakage		±10.0	µA	
ICC	VCC Supply Current		250	mA	

CAPACITANCE: TA = 0°C to 70°C, f = 1 MHz

Symbol	Parameter	Min	Max	Unit	Conditions
CIN	Input Capacitance		10	pF	
COU	Output Capacitance		15	pF	
CI/O	Bidirectional Capacitance		20	pF	

VL85C35

ENHANCED SERIAL COMMUNICATIONS CONTROLLER (ESCC)

FEATURES

- Enhanced SCC functions support DMA:
  - — 14-bit byte counter
  - — 19- bit-wide FIFO
- Completely downward-compatible with the NMOS 8530
- Two independent full-duplex channels
- Programmable clock factor
- Break generation and error detect
- Intelligent SDLC/HDLC
- Local loopback and auto echo modes
- Internal or external character synchronization
- Low power consuming CMOS

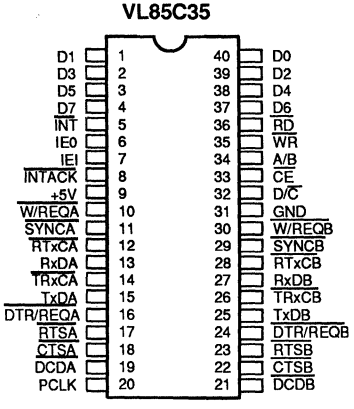
DESCRIPTION

The VL85C35 CMOS Enhanced Serial Communications Controller (ESCC) is a dual-channel, multi-protocol data communications peripheral designed for use with non-multiplexed buses. The ESCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions, including all of the features of the NMOS 8530. In addition, the VL85C35 Enhanced SCC contains a 10 X 19-bit FIFO array and 14-bit byte counter. These features, in addition to the new higher clock frequency capabilities, allow the ESSC to be used with a direct memory access (DMA) controller.

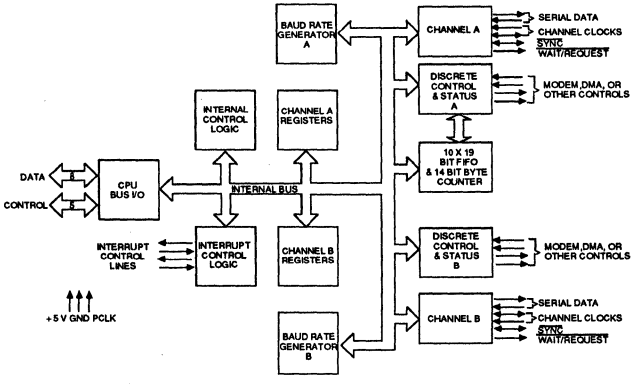
The ESCC handles asynchronous formats, such synchronous byte-oriented protocols as IBM Bisync and synchronous bit-oriented protocols as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drives, etc.), including DMA.

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The ESCC also has facilities for modem controls in both channels, in addition to its Byte-Counting Register, and FIFO in SDLC mode.

PIN DIAGRAM



BLOCK DIAGRAM

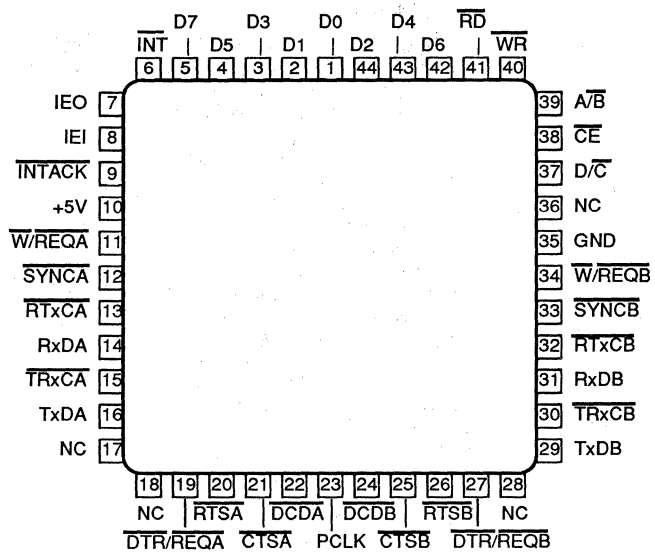


ORDER INFORMATION

Part Number	Clock Frequency	Package
VL85C35-04PC	4 MHz	Plastic DIP
VL85C35-04QC		Plastic Leaded Chip Carrier
VL85C35-04CC		Ceramic DIP
VL85C35-06PC	6 MHz	Plastic DIP
VL85C35-06QC		Plastic Leaded Chip Carrier
VL85C35-06CC		Ceramic DIP
VL85C35-10PC	10 MHz	Plastic DIP
VL85C35-10QC		Plastic Leaded Chip Carrier
VL85C35-10CC		Ceramic DIP

Note: Operating temperature range: 0°C to +70°C.

PIN DIAGRAM



SIGNAL DESCRIPTIONS

Signal Name	DIP Pin Number	Signal Description
A/$\overline{B}$	34	Channel A/Channel B Select input - This signal selects the channel on which the read or write operation occurs.
$\overline{C/E}$	33	Chip Enable Active-LOW input - Selects the ESCC for a read or write operation.
$\overline{CTSA}$, $\overline{CTSB}$	18 22	Clear To Send Active-LOW inputs - If these pins are programmed as auto enables, a LOW on the inputs enables the respective transmitters. If not programmed as auto enables, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs. The ESCC detects pulses on these inputs and can interrupt the CPU on both logic level transitions.
D/$\overline{C}$	32	Data/Control Select input - This signal defines the type of information transferred to or from the ESCC. A HIGH means data is transferred; a LOW indicates a command.
$\overline{DCDA}$, $\overline{DCDB}$	19 21	Data Carrier Detect Active-LOW inputs - These pins function as receiver enables if they are programmed for auto enables; otherwise, they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accomodate slow rise-time signals. The ESCC detects pulses on these pins and can interrupt the CPU on both logic level transitions.
D0-D7	40,1,39,2,38, 3,37,4	Data Bus, bidirectional three-state - These lines carry data and commands to and from the ESCC.
$\overline{DTR/REQA}$ $\overline{DTR/REQB}$	16, 24	Data Terminal Ready/Request Active-LOW outputs - These outputs follow the state programmed into the DTR bit. They can also be used as general-purpose outputs or as request lines for a DMA controller.
IEI	7	Interrupt Enable In Active-HIGH input - IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A HIGH IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.
IEO	6	Interrupt Enable Out Active-HIGH output - IEO is HIGH only if IEI is HIGH and the CPU is not servicing an ESCC interrupt or the ESCC is not requesting an interrupt (Interrupt Acknowledge cycle only). IEO is connected to the next lower priority device's IEI input, and thus inhibits interrupts from lower priority devices.

SIGNAL DESCRIPTIONS

Signal Name	DIP Pin Number	Signal Description
$\overline{INT}$	5	Interrupt Request Active-LOW open-drain ouput- This signal is activated when the ESCC requests an interrupt.
$\overline{INTACK}$	8	Interrupt Acknowledge Active-LOW input - This signal indicates an active Interrupt Acknowledge cycle. During this cycle, the ESCC interrupt daisy-chain settles. When $\overline{RD}$ becomes active, the ESCC places an interrupt vector on the data bus (if IEI is High). $\overline{INTACK}$ is latched by the rising edge of PCLK.
PCLK	20	Clock input - This is the master ESCC clock used to synchronize internal signals. PCLK is a TTL-level signal.
$\overline{RD}$	36	Read Active-LOW input - This signal indicates a read operation and, when the ESCC is selected, enables the ESCC's bus drivers. During the Interrupt Acknowledge cycle, this signal gates the interrupt vector onto the bus if the SCC is the highest priority device requesting an interrupt.
RxDA, RxDB	13, 27	Receive Data Active-HIGH inputs - These input signals receive serial data at standard TTL levels.
$\overline{RTxCA}$, $\overline{RTxCB}$	12, 28	Receive/Transmit Clocks Active-LOW inputs- These pins can be programmed in several different modes of operation. In each channel, $\overline{RTxC}$ may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the Digital Phase-Locked Loop. These pins can also be programmed for use with the respective $\overline{SYNC}$ pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous modes.
$\overline{RTSA}$, $\overline{RTSB}$	17, 23	Request To Send Active-LOW outputs - When the RTS bit in Write Register 5 (Figure 19) is set, the $\overline{RTS}$ signal goes LOW. When the RTS bit is reset in the asynchronous mode and Auto Enable is on, the signal goes HIGH after the transmitter is empty. In Synchronous mode or in Asynchronous mode with Auto Enable off, the $\overline{RTS}$ pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.
$\overline{SYNCA}$, $\overline{SYNCB}$	11, 29	Synchronization Active-LOW inputs or outputs - These pins can act either as inputs or outputs, or as part of the crystal oscillator circuit. In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to $\overline{CTS}$ and $\overline{DCD}$. In this mode, transitions on these lines affect the state of the Synchronous/Hunt status bits in Read Register 0 (Figure 6) but have no other function. In External Synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode, $\overline{SYNC}$ must be driven LOW to receive clock cycles after the last bit in the synchronous character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of $\overline{SYNC}$. In the Internal Synchronization mode (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which synchronous characters are recognized. The synchronous condition is not latched, so these outputs are active each time a synchronization pattern is recognized (regardless of character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag.
TxDA, TxDB	15, 25	Transmit Data Active-HIGH outputs - These output signals transmit serial data at standard TTL levels.
$\overline{TRxCA}$, $\overline{TRxCB}$	14, 26	Transmit/Receive Clocks Active-LOW inputs or outputs - These pins can be programmed in several different modes of operation. The $\overline{TRxC}$ may supply the receive clock or the transmit clock in the input mode or supply the output of the Digital Phase-Locked Loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.
$\overline{WR}$	35	Write Active-LOW input) - When the ESCC is selected, this signal indicates a write operation. The coincidence of $\overline{RD}$ and $\overline{WR}$ is interpreted as a reset.
$\overline{W/REQA}$, $\overline{W/REQB}$	10, 30	Wait/Request outputs: open-drain when programmed for a wait function, driven HIGH or LOW when programmed for a request function - These dual-purpose outputs may be programmed as request lines for a DMA controller or as wait lines to synchronize the CPU to the ESCC data rate. The reset state is wait.

FUNCTIONAL DESCRIPTION

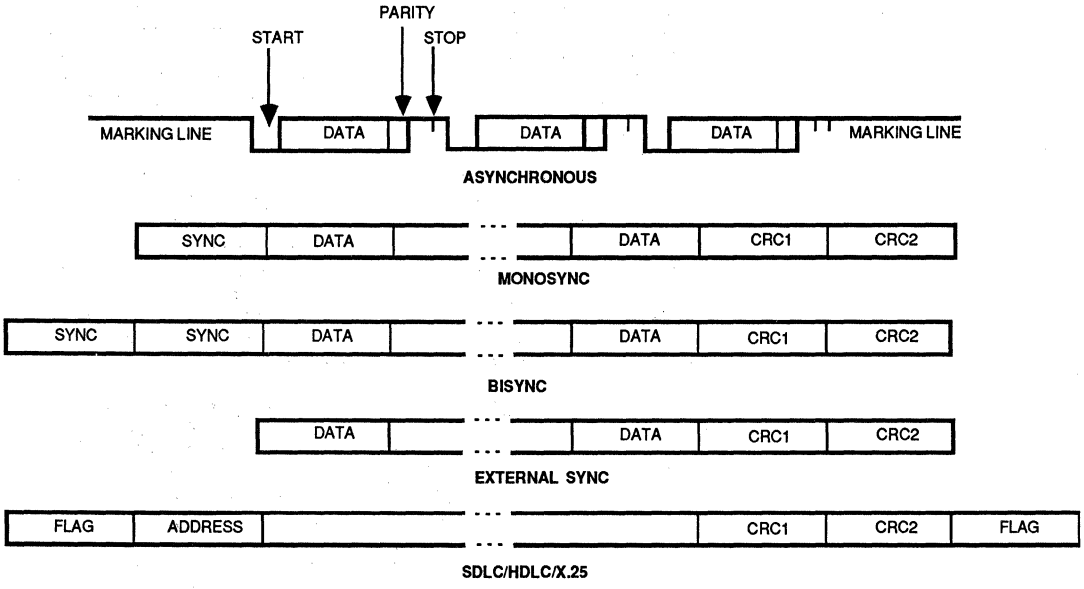
The functional capabilities of the ESCC can be described from two different points of view. As a data communications device, it transmits and receives data in a wide variety of data communications protocols. As a microprocessor peripheral, the ESCC offers such valuable features as vectored interrupts, polling, and simple handshake capability.

DATA COMMUNICATIONS CAPABILITY

The ESCC provides two independent full-duplex channels programmable for use in any common asynchronous or synchronous data communication protocol. Figure 1 and the following description briefly detail these protocols.

Asynchronous Modes - Transmission and reception can be accomplished independently on each channel with 5 to 8 bits per character, plus optional

FIGURE 1. SCC PROTOCOLS



even or odd parity. The transmitters can supply one, 1, 1 1/2, or 2 stop bits per character and can provide a break output at any time. The receiver break-detection logic interrupts the CPU both at the start and at the end of a received break. Reception is protected from spikes by a transient spike-rejection mechanism that checks the signal one-half a bit time after a LOW level is detected on the receive data input (RxDA or RxDB). If the LOW does not persist (as in the case of a transient), the character assembly process does not start.

Framing errors and overrun errors are detected and buffered together with the partial character on which they occur. Vectored interrupts allow fast servicing or error conditions using dedicated routines. Furthermore, a built-in checking process avoids the interpretation of a framing error as a new start bit: a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit begins.

The ESCC does not require symmetric transmit and receive clock signals a feature allowing use of the wide variety of clock sources. The transmitter and receiver can handle data at a rate of 1, 1/16, 1/32, or 1/64 of the clock rate supplied to the receive and transmit clock inputs. In asynchronous modes, the $\overline{\text{SYNC}}$ pin may be programmed as an input used for such functions as monitoring a ring indicator.

Synchronous Modes. The ESCC supports both byte-oriented and bit-oriented synchronous communication. Synchronous byte-oriented protocols can be handled in several modes, allowing character synchronization with a 6-bit or 8-bit synchronous character (Monosync), any 12-bit synchronization pattern (Bisync), or with an external synchronous signal. Leading sync characters can be removed without interrupting the CPU.

Any 5- or 7-bit synchronous characters are detected with 8- or 16-bit patterns in the ESCC by overlapping the larger pattern across multple incoming syn-chronous characters.

The CRC checking for synchronous byte-oriented modes is delayed by one character time, so that the CPU may disable CRC checking on specific characters. This permits the implementation of such protocols as IBM Bisync.

Both CRC-16 ($X^{16} + X^{15} + X^2 + 1$) and CCITT ($X^{16} + X^{12} + X^5 + 1$) error checking polynomials are supported. Either polynomial may be selected in all Synchronous modes. Users may preset the CRC generator and checker to all ones or all zeros. The SCC also pro-vides a feature that automatically transmits CRC data when no other data is available for transmission. This allows for high-speed transmissions under DMA control, with no need for CPU intervention at the end of a message. When there is no data or CRC to send in synchronous modes, the transmitter inserts 6-, 8-, or 16-bit synchronous characters, regardless of the programmed character length.

The ESCC supports synchronous bit-oriented protocols, such as SDLC and HDLC, by performing automatic flag sending, zero insertion, and CRC generation. A special command can be used to abort a frame in transmission. At the end of a message, the ESCC automatically transmits the CRC and trailing flag when the transmitter underruns. The transmitter may also be programmed to send an idle line consisting of continuous flag characters or a steady marking condition.

If a transmit underrun occurs in the middle of a message, an external/status interrupt warns the CPU of this status change so that an abort may be issued. The ESCC may also be programmed to send an abort itself in case of an underrun, relieving the CPU of this task. One to eight bits per character can be sent, allowing reception of a message with no prior information about the character structure in the information field of a frame.

The receiver automatically acquires synchronization on the leading flag of a frame in SDLC or HDLC and provides a synchronization signal on the $\overline{\text{SYNC}}$ pin (an interrupt can also be programmed). The receiver can be programmed to search for frames addressed by a single byte (or four bits within a byte) of a user-selected address or to a global broadcast address. In this mode, frames not matching either the user-selected or broadcast address are ignored. The number of address bytes can be extended under software control. For receiving data, an interrupt on the first received character, or an interrupt on every character, or on special condition only (end-of-frame) can be selected. The receiver automatically deletes all zeros inserted by the transmitter during character assembly. The CRC is also calculated and is automatically checked to validate frame transmission. At the end of transmission, the status of a received frame is availabe in the status registers. In SDLC mode, the ESCC must be programmed to use the SDLC CRC polynomial, but the generator and checker may be preset to all ones or all zeros.

The CRC is inverted before transmission and the receiver checks against the bit pattern 0001110100001111.

The NRZ, NRZI or FM coding may be used in any 1x mode. The parity options available in asynchronous modes are available in synchronous modes.

The ESCC can be conveniently used under DMA control to provide high-speed reception or transmission. In reception, for example, the ESCC can interrupt the CPU when the first character of a message is received. The CPU then enables the DMA to transfer the message to memory. The ESCC then issues an end-of-frame interrupt and the CPU can check the status of the received message.

Thus, the CPU is freed for other service while the message is being received. The CPU may also enable the DMA first and have the ESCC interrupt only on end-of-frame. This procedure allows all data to be transferred via the DMA.

SDLC LOOP MODE

The ESCC supports SDLC loop mode in addition to normal SDLC. In an SDLC loop, there is a primary controller station that manages the message traffic flow on the loop and any number of secondary stations. In SDLC loop mode, the ESCC performs the functions of a secondary station while an ESCC operating in regular SDLC mode can act as a controller (Figure 3).

A secondary station in an SDLC Loop is always listening to the messages being sent around the loop, and in fact must pass these messages to the rest of the loop by retransmitting them with a one-bit time delay. The secondary station can place its own message on the loop only at specific times. The controller signals that secondary stations may transmit messages by sending a special character, called an End Of Poll (EOP), around the loop. The EOP character is the bit pattern 11111110. Because of zero insertion during messages, this bit pattern is unique and easily recognized.

When a secondary station has a message to transmit and recognizes an EOP on the line, it changes the last binary 1 of the EOP to a 0 before transmission. This has the effect of turning the EOP into a flag sequence. The secondary station now places its message on the loop and terminates the message with an EOP. Any secondary stations, further down the loop with messages to transmit, can then append their messages to the message of the first secondary station without messages to send. The following stations merely echo the incoming messages and are prohibited from placing messages on the loop (except upon recognizing an EOP). The SDLC loop mode is a programmable option in the ESCC; NRZ, NRZI, and FM coding may all be used in SDLC Loop mode.

BAUD RATE GENERATOR

Each channel in the ESCC contains a programmable baud rate generator. Each generator consists of two 8-bit time constant registers that form a 16-bit time-constant, a 16-bit down counter, and a flip-flop on the output producing a square wave. On startup, the flip-flop on the output is set in a HIGH state, the value in the time-constant register is loaded into the counter, and the counter starts counting down. The output of the baud rate generator toggles upon reaching 0, the value in the time-constant register is loaded into the counter, and the process is repeated. The time constant may be changed at any time, but the new value does not take effect until the next load of the counter.

The output of the baud rate generator may be used as either the transmit clock, the receive clock, or both. It can also drive the digital phase-locked loop (see next section).

If the receive clock or transmit clock is not programmed to come from the $\overline{TRxC}$ pin, the output of the baud rate generator may be echoed out via the $\overline{TRxC}$ pin.

The following formula relates the time constant to the baud rate (the baud rate is in bits/second and BR clock period is in seconds):

$$\text{baud rate} = \frac{1}{2\,(\text{time constant}+2) \times (\text{BR clock period})}$$

DIGITAL PHASE-LOCKED LOOP

The ESCC contains a digital phase-locked-loop (DPLL) to recover clock information from a data stream with NRZI or FM encoding. The DPLL is driven by a clock that is nominally 32 (NRZI) or 16 (FM) times the data rate. The DPLL uses this clock, along with the data stream, to construct a clock for the data. This clock may then be used as the ESCC receive clock, the transmit clock, or both.

FIGURE 2. DETECTING 5- OR 7-BIT SYNCHRONOUS CHARACTERS

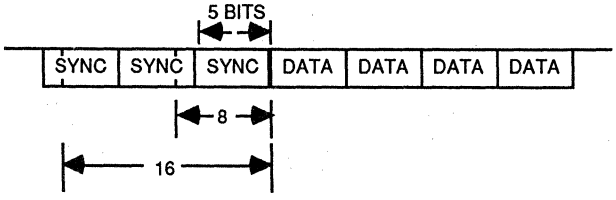
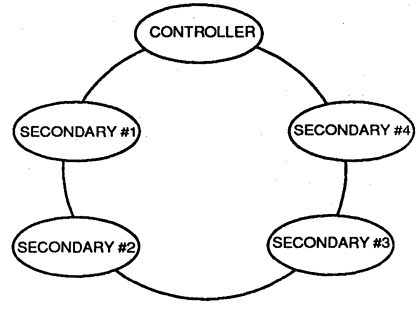


FIGURE 3. AN SDLC LOOP



For NRZI encoding, the DPLL counts the 32x clock to create nominal bit times. As the 32x clock is counted, the DPLL is searching the incoming data stream for edges (either 1 to 0 or 0 to 1). Whenever an edge is detected, the DPLL makes a count adjustment (during the next counting cycle), producing a terminal count closer to the center of the bit cell.

For FM encoding, the DPLL still counts from 0 to 31, but with a cycle corresponding to two bit times. When the DPLL is locked, the clock edges in the data stream should occur between counts 15 and 16, and between counts 31 and 0. The DPLL looks for edges only during a time centered on the 15 to 16 counting transition.

The 32x clock for the DPLL can be programmed to come from either the $\overline{\text{RTxC}}$ input or the output of the baud rate generator. The DPLL output may be programmed to be echoed out of the ESCC via the $\overline{\text{TRxC}}$ pin (if this pin is not being used as an input).

DATA ENCODING

The ESCC may be programmed to encode and decode the serial data in four different ways (Figure 4). In NRZ encoding, a 1 is represented by a HIGH level and a 0 is represented by a LOW level. In NRZI encoding, a 1 is represented by no change in level and a 0 is represented by a change in level.

In FM1 (more properly, bi-phase mark), a transition occurs at the beginning of every bit cell. A 1 is represented by an additional transition at the center of the bit cell and a 0 is represented by no additional transition at the center of the bit cell. In FMØ (bi-phase space), a transition occurs at the beginning of every bit cell. A 0 is represented by an additional transition at the center of the bit cell, and a 1 is represented by no additional transition at the center of the bit cell.

In addition to these four methods, the ESCC can be used to decode Manchester (bi-phase level) data by using the DPLL in the FM mode and programming the receiver for NRZ data. Manchester encoding always produces a transition at the center of the bit cell. If the transition is 0 to 1, the bit is a 0. If the transition is 1 to 0, the bit is a 1.

AUTO ECHO AND LOCAL LOOPBACK

The ESCC is capable of automatically echoing everything it receives. This feature is useful mainly in Asynchronous modes, but works in Synchronous and SDLC modes as well. In Auto Echo mode, TxD is RxD. Auto Echo mode can be used with NRZI or FM encoding with no additional delay, because the data stream is not decoded before retransmission. In Auto Echo mode, the CTS input is ignored as a transmitter enable (although transitions on this input can still cause interrupts if programmed to do so). In this mode, the transmitter is actually bypassed and the programmer is responsible for disabling transmitter interrupts and Wait/Request on transmit.

The ESCC is also capable of local loopback. In this mode TxD is RxD, just as in auto echo mode. However, in local loopback mode, the internal transmit data is tied to the internal receive data and RxD is ignored (except to be echoed out via TxD). The CTS and DCD inputs are also ignored as transmit and receive enables. However, transitions on these inputs can still cause interrupts. Local loopback works in asynchronous, synchronous, and SDLC modes with NRZ, NRZI, or FM coding of the data stream.

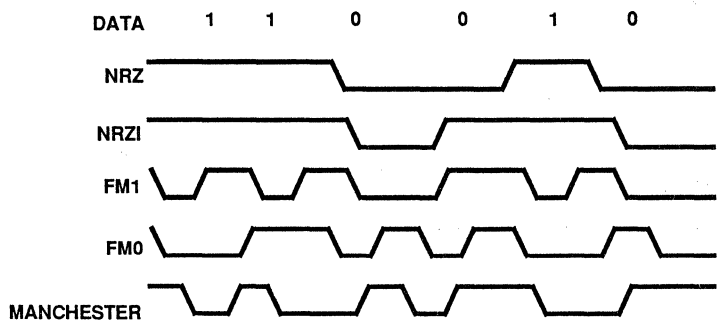
I/O INTERFACE CAPABILITIES

The ESCC offers the choice of polling, interrupt (vectored or nonvectored), and block transfer modes to transfer data, status, and control information to and from the CPU. The block transfer mode can be implemented under CPU or DMA control.

POLLING

All interrupts are disabled. Three status registers in the ESCC are automatically updated whenever any function is performed . For example, end-of-frame in SDLC mode sets a bit in one of these status registers. The idea behind polling is for the CPU to periodically read a status register until the register contents indicate the need for data to be transferred. Only one register needs to be read; depending on its contents, the CPU either writes data, reads data, or continues. Two bits in the register indicate the need for data transfer.

FIGURE 4. DATA ENCODING METHODS



An alternative is a poll of the Interrupt Pending register to determine the source of an interrupt. The status for both channels resides in one register.

INTERRUPTS

When an ESCC responds to an Interrupt Acknowledge signal ($\overline{INTACK}$) from the CPU, an interrupt vector may be placed on the data bus. This vector is written in Write Register 2 (WR2) and may be read in Read Register 2A (RR2A) or Read Register 2B (RR2B) (Figures 8).

To speed interrupt response time, the ESCC can modify three bits in this vector to indicate status. If the vector is read in Channel A, status is never included; if it is read in Channel B, status is always included.

Each of the six sources of interrupts in the ESCC (Transmit, Receive, and External/Status interrupts in both channels) has three bits associated with the interrupt source: Interrupt Pending (IP), Interrupt Under Service (IUS), and Interrupt Enable (IE). Operation of the IE bit is straightforward. If the IE bit is set for a given interrupt source, that source can request interrupts. The exception is when the MIE (Master Interrupt Enable) bit in WR9 is reset and no interrupts may be requested. The IE bits are write only.

The other two bits are related to the interrupt priority chain (Figure 5). As a microprocessor peripheral, the ESCC may request an interrupt only when no higher priority device is requesting one; e.g., when IEI is HIGH. If the device in question requests an interrupt, it pulls down $\overline{INT}$. The CPU then responds with $\overline{INTACK}$, and the interrupting device places the vector on the data bus.

In the ESCC, the IP bit signals a need for interrupt servicing. When an IP bit is 1 and the IEI input is HIGHh, the $\overline{INT}$ output is pulled LOW, requesting an interrupt. In the ESCC, if the IE bit is not set by enabling interrupts, then the IP for that source can never be set. The IP bits are readable in RR3A.

The IUS bits signal that an interrupt request is being serviced. If an IUS is set, all interrupt sources of lower priority in the ESCC and external to the ESCC are prevented from requesting interrupts. The internal interrupt sources are inhibited by the state of the internal daisy chain, while lower priority devices are inhibited by the IEO output of the ESCC being pulled LOW and propagated to subsequent peripherals. An IUS bit is set during an interrupt acknowledge cycle if there are no higher priority devices requesting interrupts.

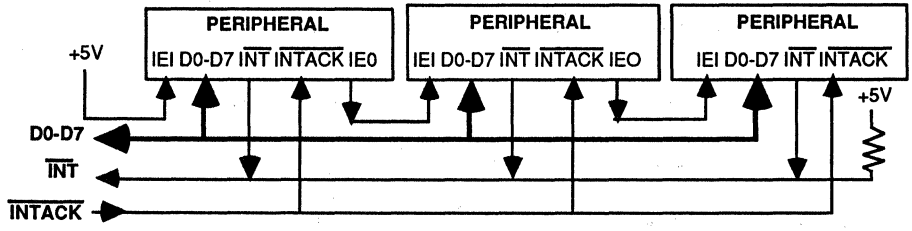
There are three types of interrupts: transmit, receive, and external/status. Each interrupt type is enabled under program control with Channel A having higher priority than Channel B, and with receive, transmit, and external/status interrupts prioritized in that order within each channel. When the transmit interrupt is enabled, the CPU is interrupted when the transmit buffer becomes empty. (This implies that the transmitter must have had a data character written into it so that it can become empty.) When enabled, the receiver can interrupt the CPU in one of three ways:

- On first receive character or special receive condition
- On all receive characters or special receive condition
- On special receive condition only.

Interrupt on first character or special condition and interrupt on special condition only are typically used with the Block Transfer mode. A special receive condition is one of the following: receiver overrun, framing error in Asynchronous mode, end-of-frame in SDLC mode, and optionally, a parity error. The special receive condition interrupt is different from an ordinary receive character interrupt only in that the status is placed in the vector during the Interrupt Acknowledge cycle. In interrupt on first receive character, an interrupt can occur from special receive conditions any time after the first receive character interrupt.

The main function of the external/status interrupt is to monitor the signal transitions of the $\overline{CTS}$, $\overline{DCD}$, and $\overline{SYNC}$ pins; however, an external/status interrupt is also caused by a transmit underrun condition, or a zero count in the baud rate generator, or by the detection of a break (asynchronous mode), abort (SDLC mode) or EOP (SDLC loop mode) sequence in the data stream.

FIGURE 5. INTERRUPT SCHEDULE



The interrupt caused by the abort or EOP has a special feature allowing the ESCC to interrupt when the abort or EOP sequence is detected or terminated. This feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the Abort condition in external logic in SDLC mode.
In SDLC Loop mode, this feature allows secondary stations to recognize the need of the primary station to regain control of the loop during a poll sequence.

CPU/DMA BLOCK TRANSFER
The ESCC provides a Block Transfer mode to accommodate CPU block transfer functions and DMA controllers. The Block Transfer mode uses the Wait/Request output in conjunction with the Wait/Request bits in WR1. The Wait/Request output can be defined under software control as a Wait line in the CPU Block Transfer mode or as a Request line in the DMA Block Transfer mode.

To a DMA controller, the ESCC Request output indicates that the ESCC is ready to transfer data to or from memory. To the CPU, the Wait line indicates that the ESCC is not ready to transfer data, thereby requesting that the CPU extend the I/O cycle. The DTR/Request line allows full-duplex operation under DMA control.

PROGRAMMING

The ESCC contains 13 write registers in each channel that are programmed by the system separately to configure the functional personality of the channels.

In the ESCC, register addressing is direct for the data registers only, which are selected by a HIGH on the D/$\overline{C}$ pin. In all other cases (with the exception of WR0 and RR0), programming the write registers requires two write operations and reading the read registers requires both a write and a read operation. The first write is to WR0 and contains three bits that point to the selected register. The second write is the actual control word for the selected register, and if the second operation is read, the selected read register is accessed. All of the registers in the ESCC, including the data registers, may be accessed in this fashion. The pointer bits are automatically cleared after the read or write operation so that WR0 (or RR0) is addressed again.

The system program first issues a series of commands to initialize the basic mode of operation. This is followed by other commands to qualify conditions within the selected mode. For example, the asynchronous mode, character length, clock rate, number of stop bits, and even or odd parity might be set first. Then the interrupt mode would be set, and, finally, receiver or trans-mitter enable.

READ REGISTERS
The ESCC contains ten read registers (eleven counting receive buffer RR8) in each channel. Four of these may be read to obtain status information (RR0, RR1, RR10, and RR15). Two registers (RR12 and RR13) may be read to learn the baud rate generator time constant. The RR2 contains either the unmodified interrupt vector (Channel A) or the vector modified by status information (Channel B). Both RR7 and RR6 read the DMA FIFO. The RR3 contains the Interrupt Pending (IP) bits (Channel A). Figures 6 through 13 and Figure 41 show the formats for each read register.

The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring; e.g., when the interrupt vector indicates a special receive condition interrupt, all the appropriate error bits can be read from a single register (RR1).

WRITE REGISTERS
The ESCC contains 13 write registers (14 counting WR8, the transmit buffer) in each channel. These write registers are programmed separately to configure the functional personality of the channels. In addition, there are two registers (WR2 and WR9) shared by the two channels that may be accessed through either of them; WR2 contains the interrupt vector for both channels, while WR9 contains the interrupt control bits. Figures 14 through 28 and Figure 41 show the format of each write register.

TIMING

The ESCC generates internal control signals from $\overline{WR}$ and $\overline{RD}$ that are related to PCLK. Since PCLK has no phase relationship with $\overline{WR}$ and $\overline{RD}$, the circuitry generating these internal control signals must provide time for metastable conditions to disappear. This gives rise to a recovery time related to PCLK. The recovery time applies only between bus transactions involving the ESCC. The recovery time required for proper operation is specified from the rising edge of $\overline{WR}$ or $\overline{RD}$ in the first transaction involving the SCC, to the falling edge of $\overline{WR}$ or $\overline{RD}$ in the second transaction involving the ESCC. This time must be at least four PCLK cycles plus 200 ns.

READ CYCLE TIMING
Figure 29 illustrates Read cycle timing. Addresses on A/$\overline{B}$ and D/$\overline{C}$ and the status on $\overline{INTACK}$ must remain stable through the cycle. If $\overline{CE}$ falls after $\overline{RD}$ falls or if it rises before $\overline{RD}$ rises, the effective $\overline{RD}$ is shortened.

WRITE CYCLE TIMING
Figure 30 illustrates Write cycle timing. Addresses on A/$\overline{B}$ and D/$\overline{C}$ and the status on $\overline{INTACK}$ must remain stable throughout the cycle. If $\overline{CE}$ falls after $\overline{WR}$ falls, or if it rises before $\overline{WR}$ rises, the effective $\overline{WR}$ is shortened.

INTERRUPT ACKNOWLEDGE CYCLE TIMING
Figure 31 illustrates Interrupt Acknowledge cycle timing. Between the time $\overline{INTACK}$ goes LOW and the falling edge of $\overline{RD}$, the internal and external IEI/IEO daisy chains settle. If there is an interrupt pending in the ESCC and IEI is HIGH when $\overline{RD}$ falls, the Acknowledge cycle is intended for the ESCC. In this case, the ESCC may be programmed to respond to $\overline{RD}$ LOW by placing its interrupt vector on D0-D7 and it then internally sets the appropriate Interrupt-Under-Service latch.

FIGURE 6. READ REGISTER 0

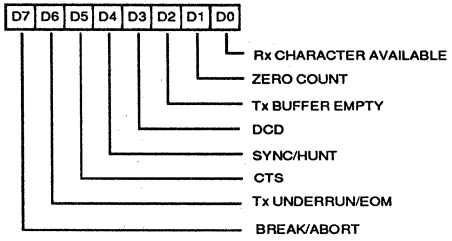


FIGURE 7. READ REGISTER 1

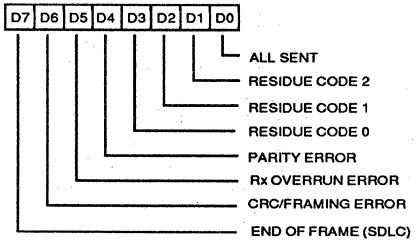


FIGURE 8. READ REGISTER 2

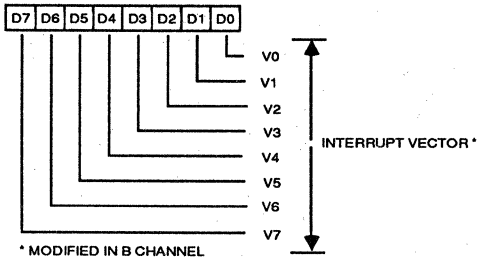


FIGURE 9. READ REGISTER 3

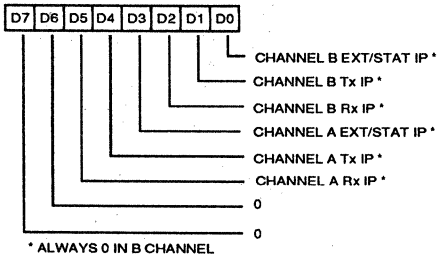


FIGURE 10. READ REGISTER 10

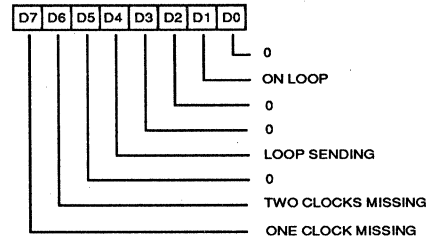


FIGURE 11. READ REGISTER 12

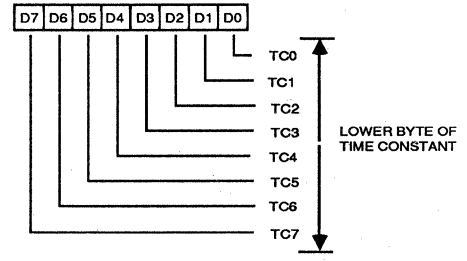


FIGURE 12. READ REGISTER 13

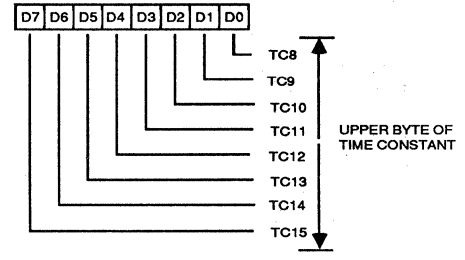


FIGURE 13. READ REGISTER 15

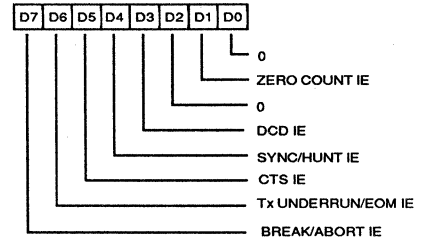
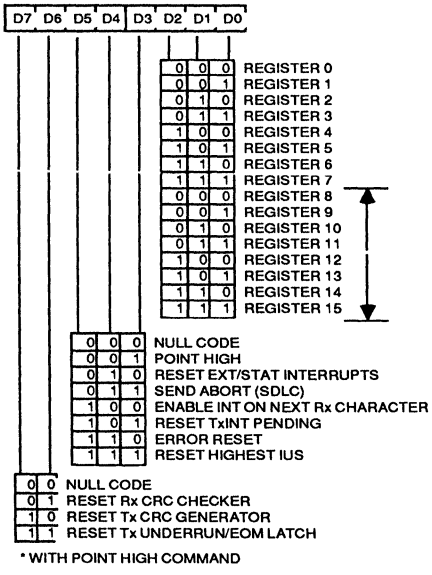


FIGURE 14. WRITE REGISTER 0



* WITH POINT HIGH COMMAND

FIGURE 15. WRITE REGISTER 1

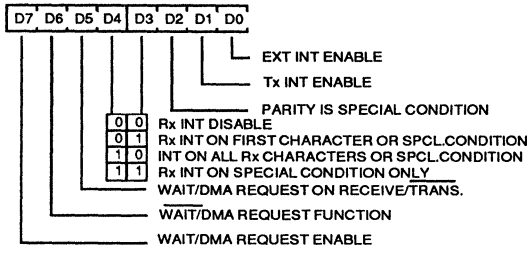


FIGURE 16. WRITE REGISTER 2

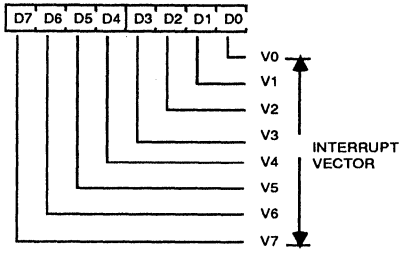


FIGURE 17. WRITE REGISTER 3

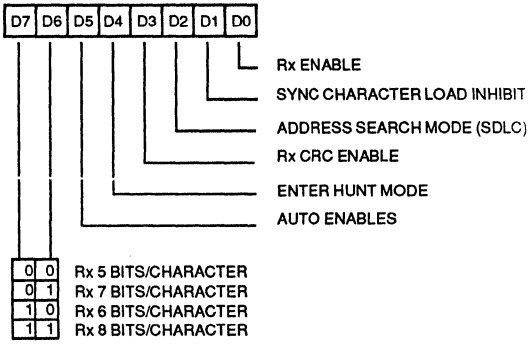


FIGURE 18. WRITE REGISTER 4

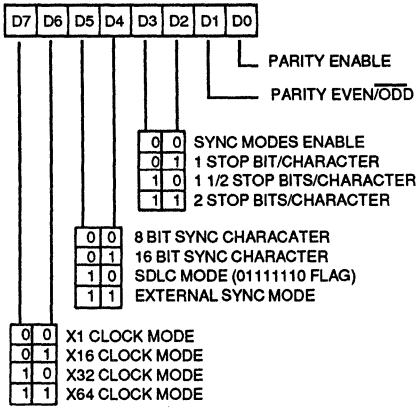


FIGURE 19. WRITE REGISTER 5

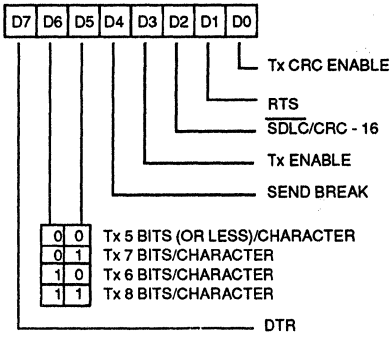


FIGURE 20. WRITE REGISTER 6

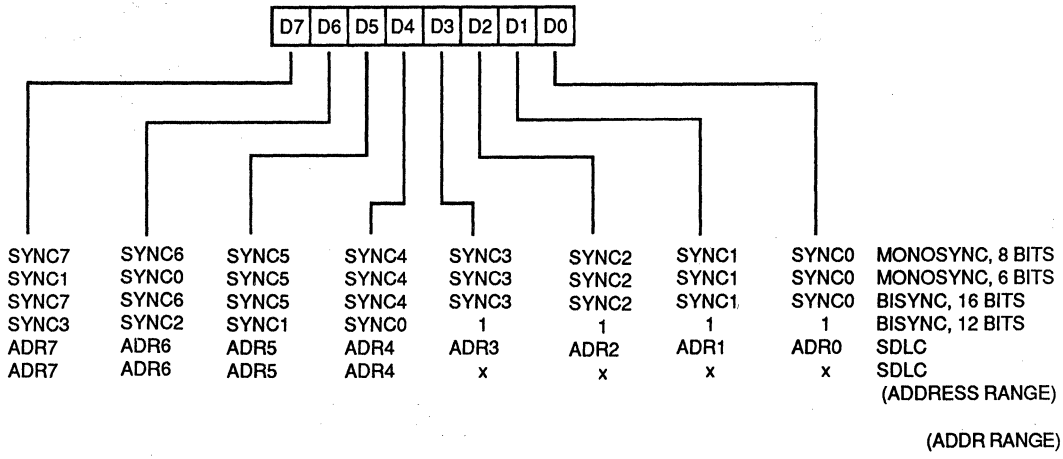


FIGURE 21. WRITE REGISTER 7

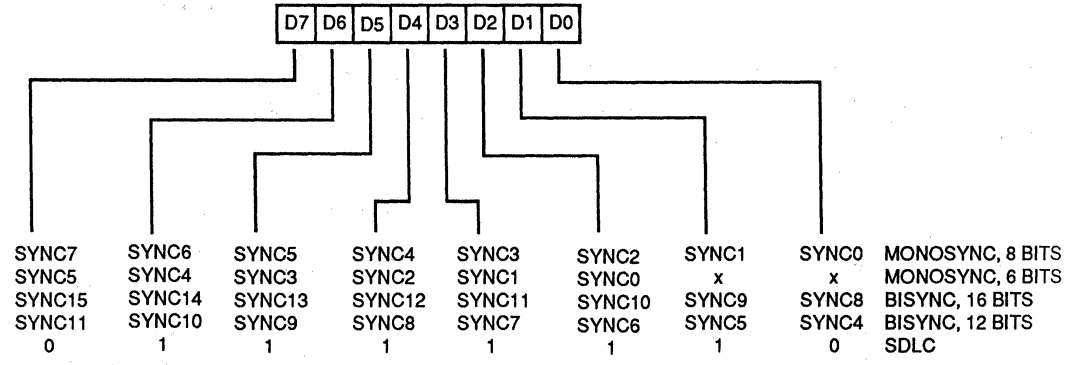


FIGURE 22. WRITE REGISTER 9

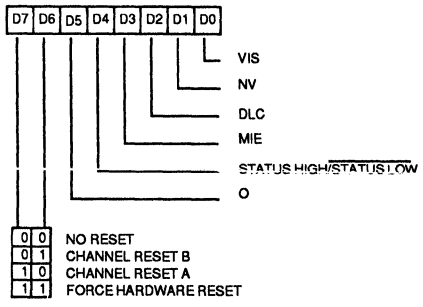


FIGURE 23. WRITE REGISTER 10

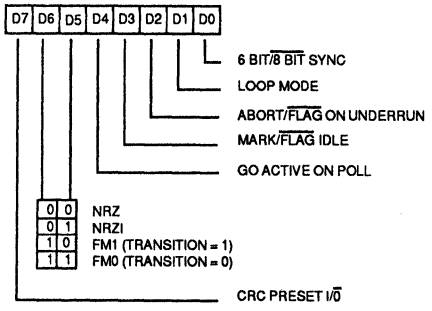


FIGURE 24. WRITE REGISTER 11

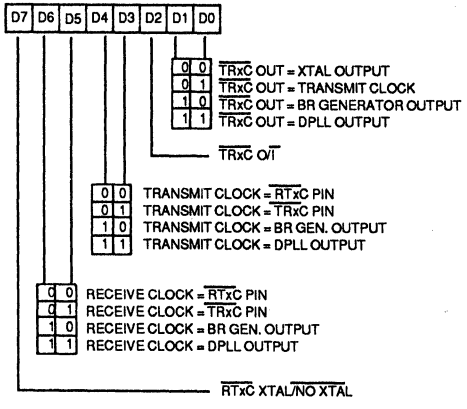


FIGURE 25. WRITE REGISTER 12

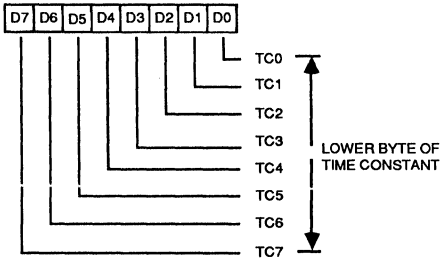


FIGURE 26. WRITE REGISTER 13

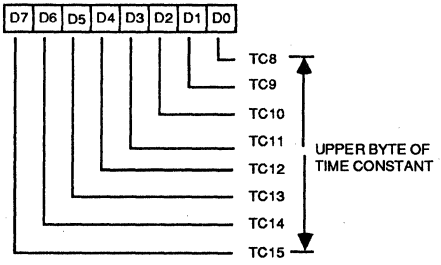


FIGURE 27. WRITE REGISTER 14

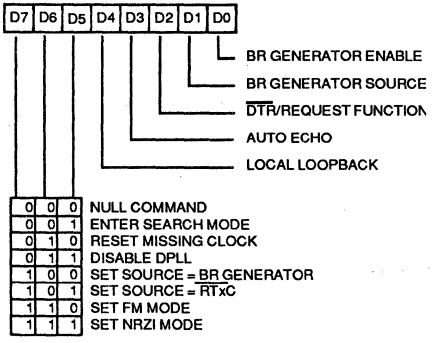


FIGURE 28. WRITE REGISTER 15

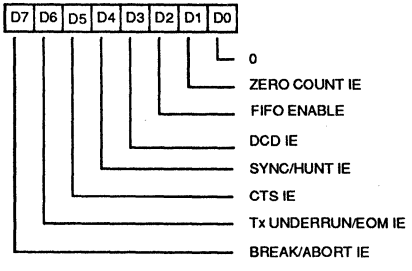


FIGURE 29. READ CYCLE TIMING

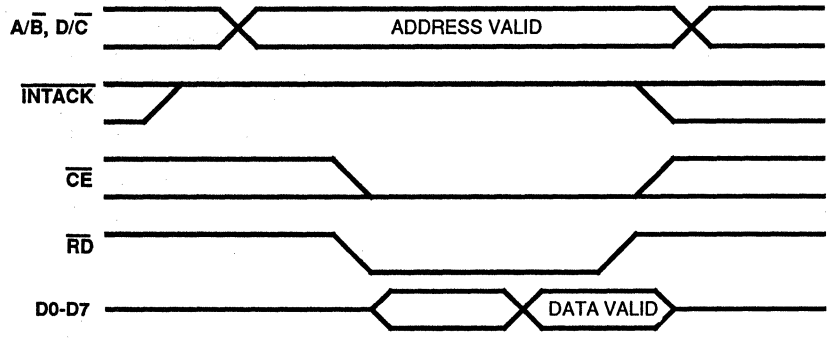


FIGURE 30. WRITE CYCLE TIMING

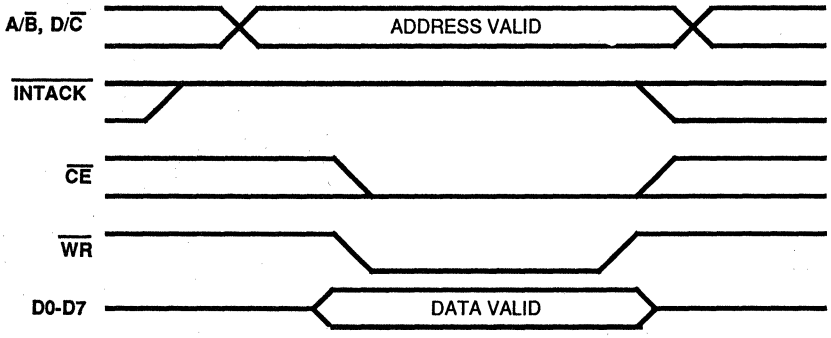


FIGURE 31. INTERRUPT ACKNOWLEDGE CYCLE TIMING

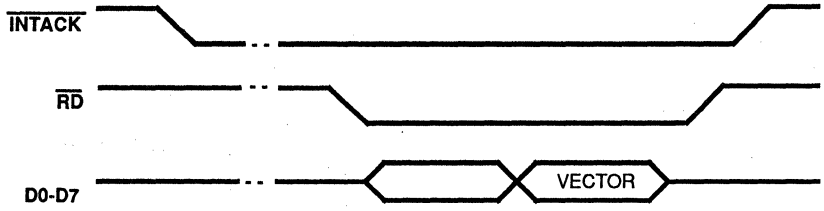


FIGURE 33. READ AND WRITE TIMING (SEE TABLE 1)

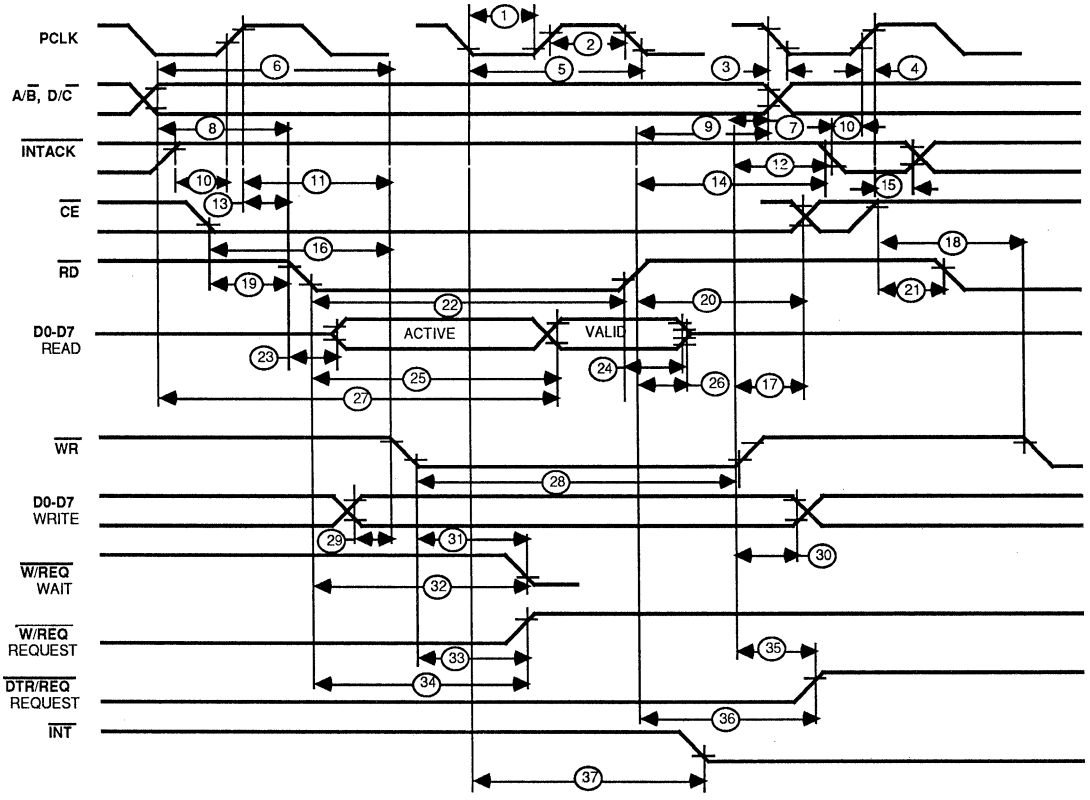


FIGURE 34. RESET TIMING (SEE TABLE 1)

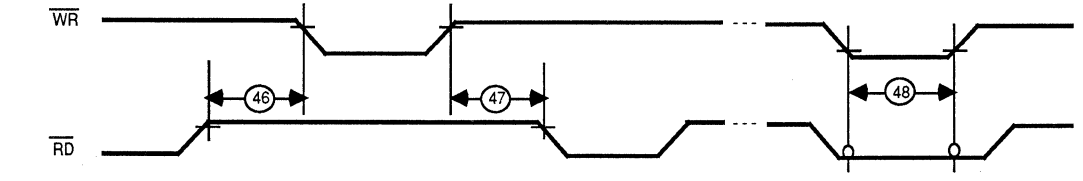


FIGURE 35. CYCLE TIMING (SEE TABLE 1)

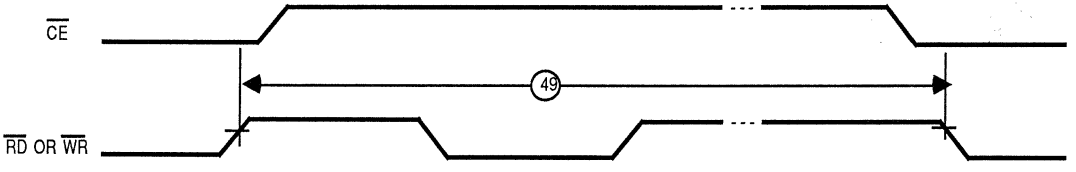


TABLE 1. READ AND WRITE TIMING CHARACTERISTICS: TA = 0°C TO +70°C

No.	Symbol	Parameter	4 MHz		6 MHz		10 MHz		
			Min	Max	Min	Max	Min	Max	Notes
1	TwPCl	PCLK LOW Width	105	2000	70	1000			
2	TwPCh	PCLK HIGH Width	105	2000	70	1000			
3	TfPC	PCLK Fall Time		20		10			
4	TrPC	PCLK Rise Time		20		15			
5	TcPC	PCLK Cycle Time	250	4000	165	2000			
6	TsA(WR)	Address to $\overline{WR}$ Setup Time	80		80				
7	ThA(WR)	Address to $\overline{WR}$ Hold Time	0		0				
8	TsA(RD)	Address to $\overline{RD}$ Setup Time	80		80				
9	ThA(RD)	Address to $\overline{RD}$ Hold Time	0		0				
10	TsIA(PC)	$\overline{INTACK}$ to PCLK Setup Time	0		0				
11	TsIAi(WR)	$\overline{INTACK}$ to $\overline{WR}$ Setup Time	200		160				2
12	ThIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ Hold Time	0		0				
13	TsIAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ Setup Time	200		160				2
14	ThIA(RD)	$\overline{INTACK}$ to $\overline{RD}$ Hold Time	0		0				
15	ThIA(PC)	$\overline{INTACK}$ to PCLK Hold Time	100		100				
16	TsCE1(WR)	$\overline{CE}$ LOW to $\overline{WR}$ Setup Time	0		0				
17	ThCE(WR)	$\overline{CE}$ to $\overline{WR}$ Hold Time	0		0				
18	TsCEh(WR)	$\overline{CE}$ HIGH to $\overline{WR}$ Setup Time	100		70				2
19	TsCE1(RD)	$\overline{CE}$ LOW to $\overline{RD}$ Setup Time	0		0				2
20	ThCE(RD)	$\overline{CE}$ to $\overline{RD}$ Hold Time	0		0				2
21	TsCEh(RD)	$\overline{CE}$ HIGH to $\overline{RD}$ Setup Time	100		70				2
22	TwRD1	$\overline{RD}$ LOW Width	390		250				
23	TdRD(DRA)	$\overline{RD}$ to Read Data Active Delay	0		0				
24	TdRDr(DR)	$\overline{RD}$ to Read Data Not Valid Delay	0		0				
25	TdRDf(DR)	$\overline{RD}$ to Read Data Valid Delay		250		180			
26	TdRD(DRz)	$\overline{RD}$ to Read Data Float Delay		70		45			3
27	TdA(DR)	Address Required Valid to Read Data Valid Delay		590		420			
28	TwWR1	$\overline{WR}$ LOW Width	390		250				
29	TsDW(WR)	Write Data to $\overline{WR}$ Setup Time	0		0				
30	ThDW(WR)	Write Data to $\overline{WR}$ Hold Time	0		0				
31	TdWR(W)	$\overline{WR}$ to Wait Valid Delay		240		200			5
32	TdRD(W)	$\overline{RD}$ to Wait Valid Delay		240		200			5
33	TdWRf(REQ)	$\overline{WR}$ to W/$\overline{REQ}$ Not Valid Delay		240		200			
34	TdRDf(REQ)	$\overline{RD}$ to W/$\overline{REQ}$ Not Valid Delay		240		200			
35	TdWRr(REQ)	$\overline{WR}$ to DTR/$\overline{REQ}$ Not Valid Delay		(4TcPC +300)		(4TcPC +250)			
36	TdRDr(REQ)	$\overline{RD}$ to DTR/$\overline{REQ}$ Not Valid Delay		(4TcPC +300)		(4TcPC +250)			
37	TdPC(INT)	PCLK to $\overline{INT}$ Valid Delay		500		500			5
38	TdIAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ (Acknowledge) Delay	240		250				6
39	TwRDA	$\overline{RD}$ (Acknowledge) Width	285		250				
40	TdRDA(DR)	$\overline{RD}$ (Ack.) to Read Data Valid Delay		190		180			
41	TsIEI(RDA)	IEI to $\overline{RD}$ (Acknowledge) Setup Time	120		100				
42	ThIEI(RDA)	IEI to $\overline{RD}$ (Acknowledge) Hold Time	0		0				
43	TdIEI(IEO)	IEI to IEO Delay Time		120		100			
44	TdPC(IEO)	PCLK to IEO Delay		250		250			
45	TdRDA(INT)	$\overline{RD}$ to $\overline{INT}$ Inactive Delay		500		500			4
46	TdRD(WRQ)	$\overline{RD}$ to $\overline{WR}$ Delay for No Reset	30		15				
47	TdWRQ(RD)	$\overline{WR}$ to $\overline{RD}$ Delay for No Reset	30		30				
48	TwRES	$\overline{WR}$ and $\overline{RD}$ Coincident LOW for Reset	250		250				
49	Trc	Valid Access Recovery Time	(4TcPC +200)		(4TcPC +130)				

READ AND WRITE TIMING (NOTES)

1. Units are in nanoseconds.
2. Parameter does not apply to Interrupt Acknowledge transactions.
3. Float delay is defined as the time required for a ±0.5 V change at the output with a maximum dc load and minimum ac load.
4. Parameter applies only between transactions involving the ESCC.
5. Open-drain output, measured with open-drain test load.
6. Parameter is system-dependent. For any ESCC in the daisy chain, TdIAi(RD) must be greater than the sum of TdPC (IEO) for the highest priority device in the daisy chain, TsIEI(RDA) for the ESCC, and TdIEIf(IEO) for each device separating them in the daisy chain.

FIGURE 36. INTERRUPT ACKNOWLEDGE TIMING (SEE TABLE 1)

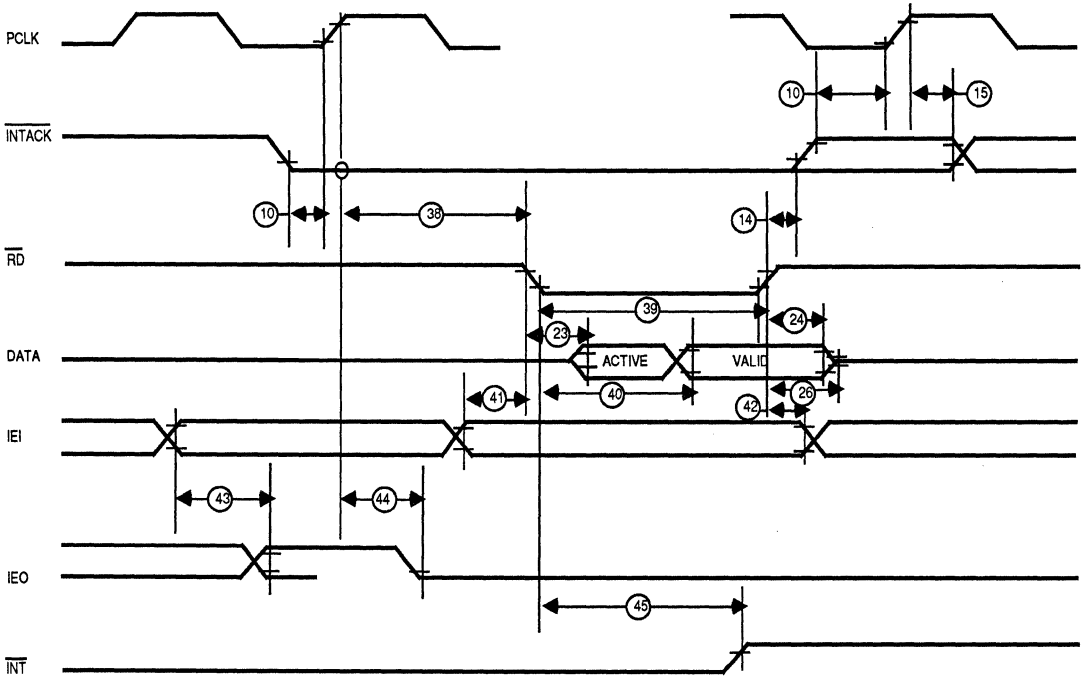


FIGURE 37. GENERAL TIMING (SEE TABLE 2)

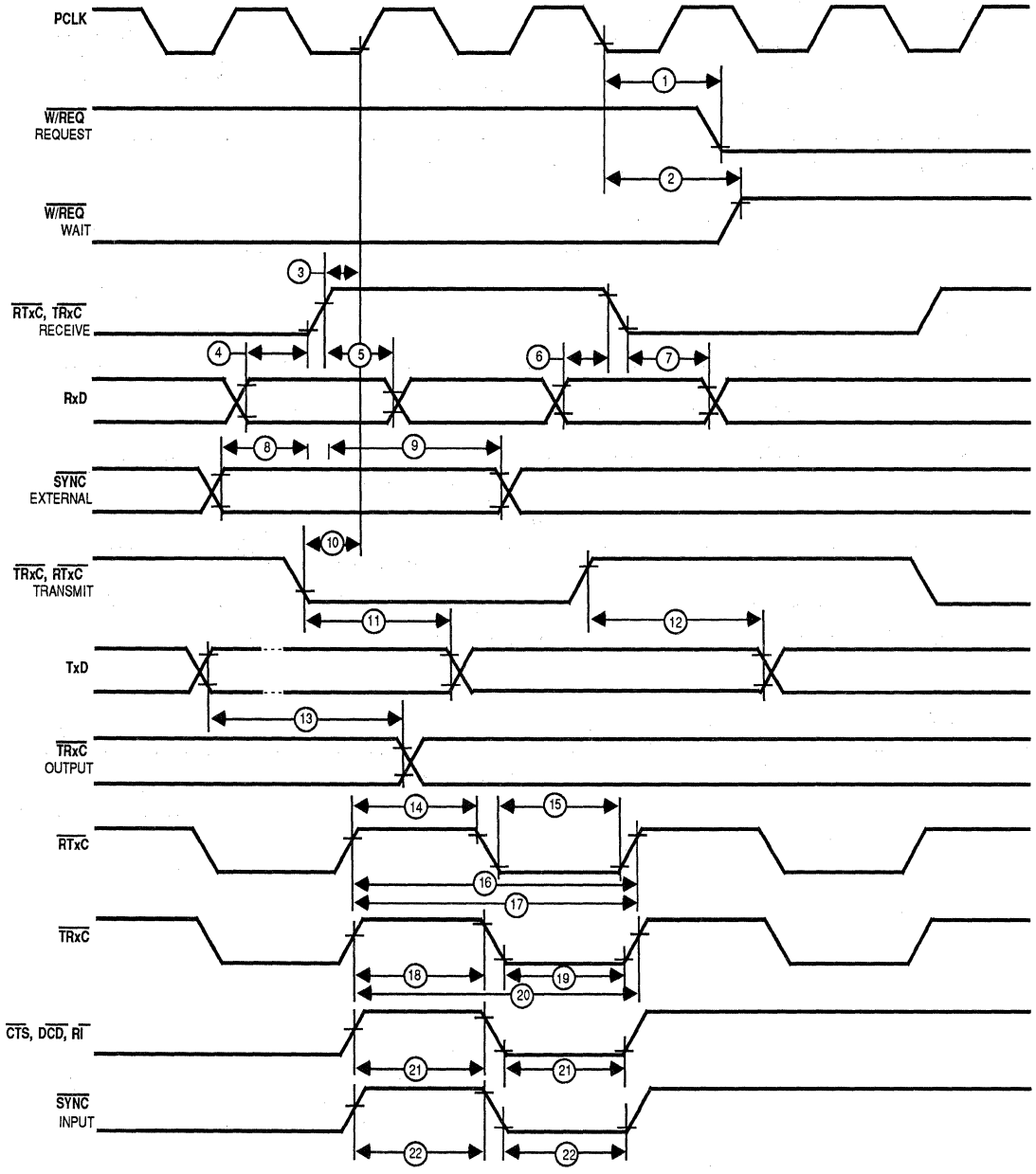


TABLE 2. GENERAL TIMING

No.	Symbol	Parameter	4 MHz		6 MHz		10 MHz		
			Min*	Max*	Min*	Max*	Min*	Max*	Notes
1	TdPC(REQ)	PCLK to W/REQ Valid Delay		250		250			
2	TdPC(W)	PCLK to Wait Inactive Delay		350		350			
3	Ts RXC(PC)	RxC to PCLK Setup Time (PCLK ÷ 4 Case Only)	8	TwPC1	70	TwPC1			2,5
4	TsRXD(RXCr)	RxD to RxC Setup Time (X1 Mode)	0		0				2
5	ThRXD(RXCr)	RxD to RxC Hold Time (X1 Mode)	150		150				2
6	TsRXD(RXCf)	RxD to RxC Setup Time (X1 Mode)	0		0				2,6
7	ThRXD(RXCf)	RxD to RxC Hold Time (X1 Mode)	150		150				2,6
8	TsSY(RXC)	SYNC to RxC Setup Time	-200		-200				4,2
9	ThSY(RXC)	SYNC to RxC Hold Time	3TcPC +200		3TcPC +200				4, 2
10	TsTXC(PC)	TxC to PCLK Setup Time	0		0				3,5
11	TdTXCf(TXD)	TxC to TxD Delay (X1 Mode)		300		230			3
12	TdTXCr(TXD)	TxC to TxD Delay (X1 Mode)		300		230			3,5
13	TdTXD(TRX)	TxD to TRxC Delay (Send Clock Echo)		200		200			
14	TwRTXh	RTxC HIGH Width	180		180				7
15	TwRTXl	RTxC LOW Width	180		180				7
16	TcRTX	RTxC Cycle Time	400		400				7
17	TcRTXX	Crystal Oscillator Period	250	1000	250	1000			3
18	TwTRXh	TRxC HIGH Width	180		180				4,7
19	TwTRXl	TRxC LOW Width	180		180				4,7
20	TcTRX	TRxC Cycle Time	400		400				4,7
21	TwEXT	DCD or CTS Pulse Width	200		200				
22	TwSY	SYNC Pulse Width	200		200				

TABLE 3. SYSTEM TIMING

No.	Symbol	Parameter	4 MHz		6 MHz		10 MHz		
			Min*	Max*	Min*	Max*	Min*	Max*	Notes
1	TdRXC(REQ)	RxC to W/REQ Valid Delay	8	12	8	12			2
2	TdRXC(W)	RxC to Wait Inactive Delay	8	12	8	12			1,2
3	TdRXC(SY)	RxC to SYNC Valid Delay	4	7	4	7			2
4	TdRXC(INT)	RxC to INT Valid Delay	10	16	10	16			1,2
5	TdTXC(REQ)	TxC to W/REQ Valid Delay	5	8	5	8			3
6	TdTXC(W)	TxC to Wait Inactive Delay	5	8	5	8			1,3
7	TdTXC(DRQ	TxC to DTR/REQ Valid Delay	4	7	4	7			3
8	TdTXC(INT)	TxC to INT Valid Delay	6	10	6	10			1,3
9	TdSY(INT)	SYNC Transition to INT Valid Delay	2	6	2	6			1
10	TdEXT(INT)	DCD or CTS Transition to INT Valid Delay	2	6	2	6			1

General and System Timing Notes:

1. Open-drain output, measured with open-drain test load.
2. RxC is RTxC or TRxC, whichever is supplying the transmit clock.
3. TxC is TRxC or RTxC, whichever is supplying the transmit clock.
4. Both TrxC and SYNC have 30 pF capacitors connected to ground.
5. Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between RxC and PCLK or TxC and PCLK is required.
6. Parameter applies only to FM encoding/decoding.
7. Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to chip PCLK requirements.

* Units are in nanoseconds (ns).

FIGURE 38. SYSTEM TIMING (SEE TABLE 3)

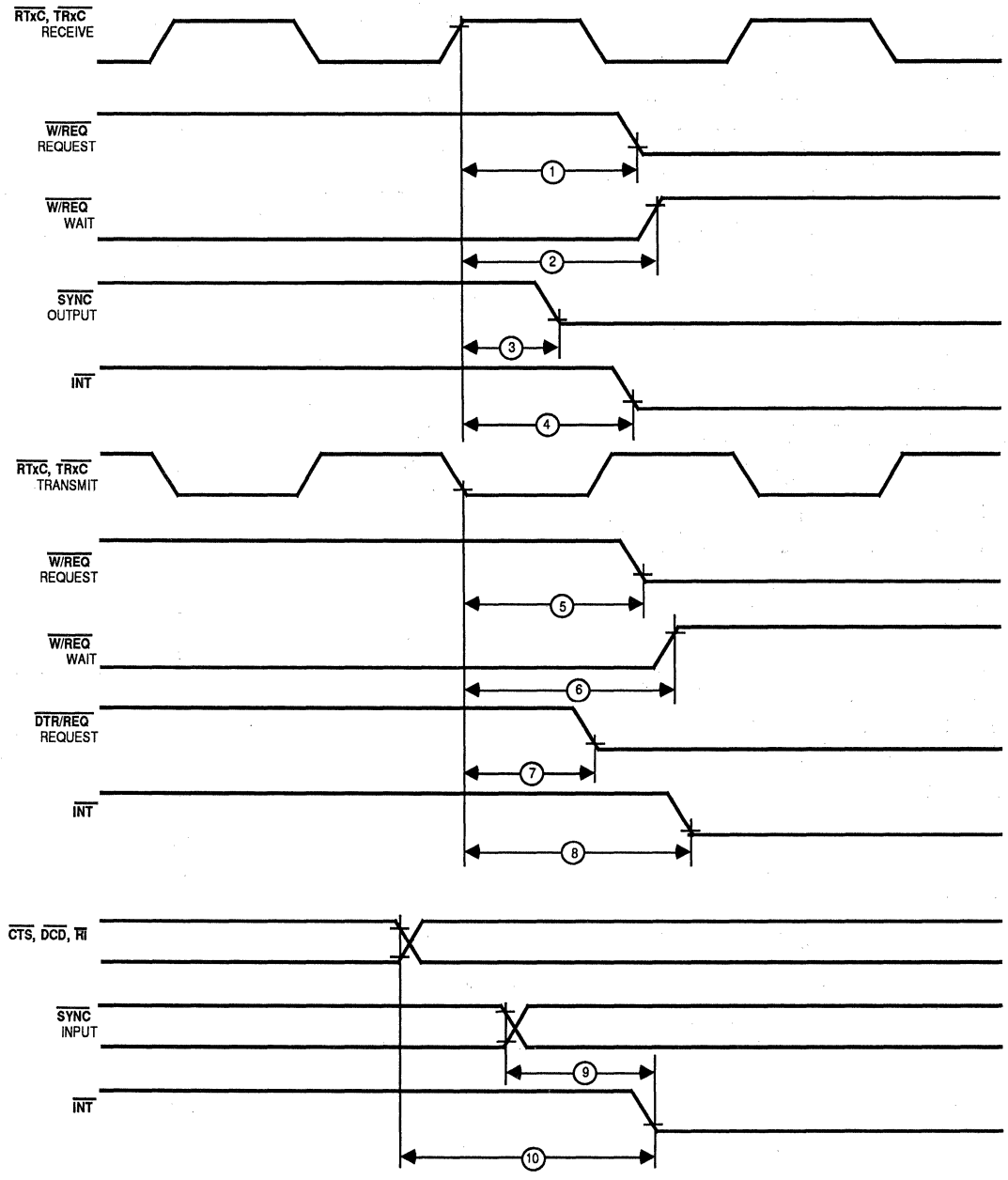
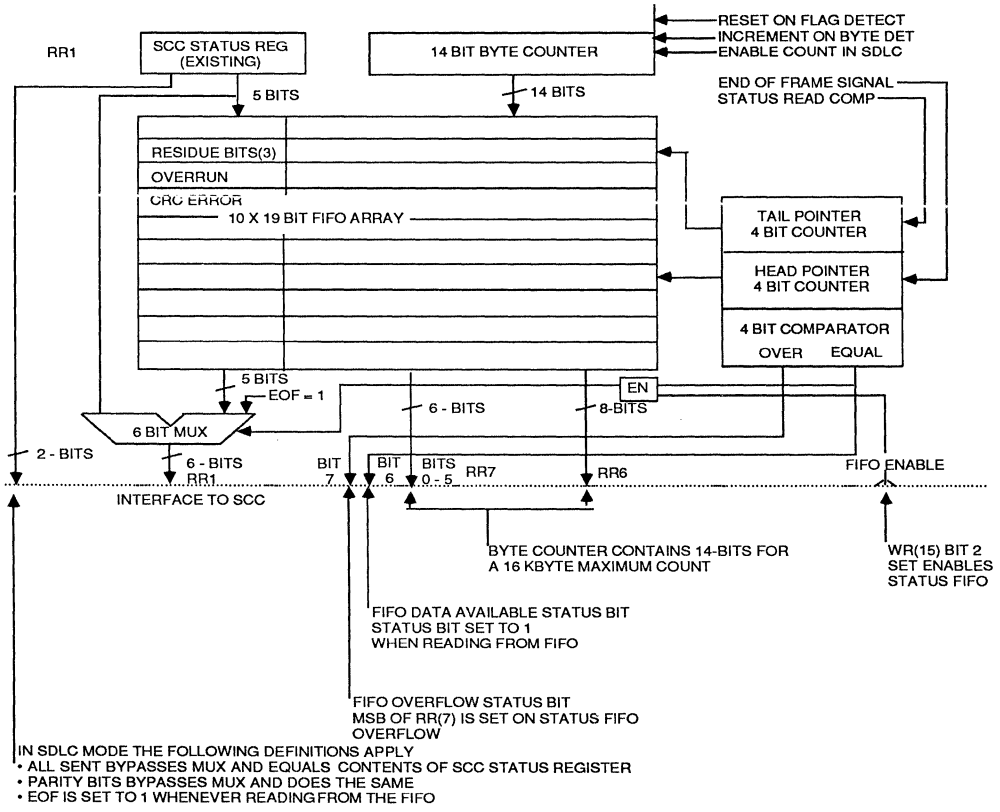


FIGURE 39. ESCC STATUS REGISTER



FIFO DETAIL

For a better understanding of details of the FIFO operation, refer to the block diagram in Figure 39.

ENABLE/DISABLE

This FIFO is implemented so that it is only enabled when Channel A register WR15 bit 2 is set and the ESCC is in the SDLC/HDLC mode, otherwise the status register contents bypass the FIFO and go directly to the bus interface (the FIFO pointer logic is reset either when disabled or via a channel or power-on reset). When the FIFO mode is disabled, the ESCC is completely downward-compatible with the HMOS VL8530. The FIFO mode is disabled on power-up (WR15 bit 2 is set to 0 on reset). The effects of backward compatibility on the register set are that RR4 is an image of RR0, RR5 is an image of RR1, RR6 is an image of RR2, and RR7 is an image of RR3. For details of the added registers, refer to Figure 3. The status of the FIFO Enable signal can be obtained by reading Channel A RR15 bit 2. If the FIFO is enabled, the bit will be set to 1; otherwise, it will be reset. Channel B WR15 and RR15 behave exactly as in the VL8530 standard product.

READ OPERATION

When WR15 bit 2 is set and the FIFO is not empty, the next read to any of status register RR1 or the additional registers RR7 and RR6 will actually be from the FIFO. Reading status register RR1 causes one location of the FIFO to be emptied, so status should be read after reading the byte count, otherwise the count will be incorrect. Before the FIFO underflows, it is disabled. In this case, the multiplexer is switched to allow status to read directly from the status register, and reads from RR7 and RR6 will contain bits that are undefined. Bit 6 of RR7 (FIFO Data Available) can be used to determine if status data is coming from the FIFO or directly from the status register, since it is set to one whenever the FIFO is not empty.

Since not all status bits must be stored in the FIFO, the All Sent, Parity, and EOF bits will bypass the FIFO. The status bits sent through the FIFO will be Residue Bits (3), Overrun, and CRC Error.

The sequence for proper operation of the byte count and FIFO logic is to read the registers in the following order: RR7, RR6, and RR1 (reading RR6 is optional). Additional logic prevents the FIFO from

FIGURE 40. SDLC BYTE COUNTING DETAIL

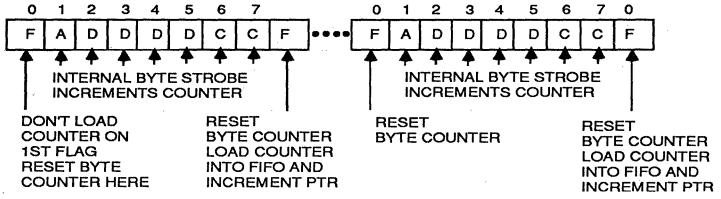
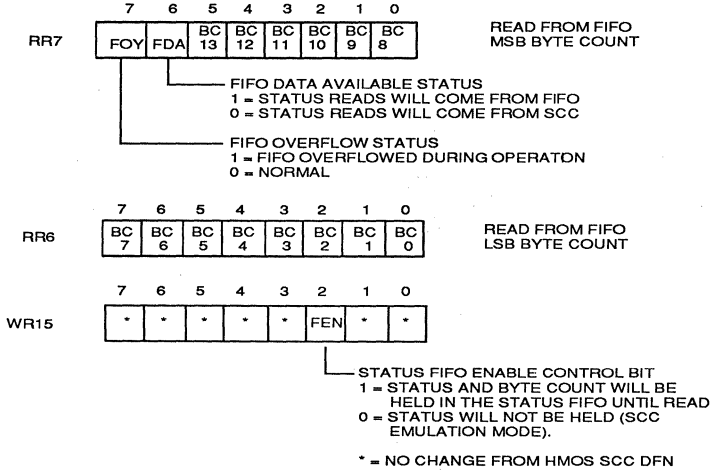


FIGURE 41. ESCC REGISTERS



being emptied by multiple reads from RR1. The read from RR7 latches the FIFO empty/full status bit (bit 6) and steers the status multiplexer to read from the ESCC megacell instead of the status FIFO (since the status FIFO is empty). The read from RR1 allows an entry to be read from the FIFO (if the FIFO was empty, logic is added to prevent a FIFO underflow condition).

WRITE OPERATION

When the end of an SDLC frame (EOF) has been received and the FIFO is enabled, the contents of the status and byte-count registers are loaded into the FIFO. The EOF signal is used to increment the FIFO. If the FIFO overflows, the MSB of RR7 (FIFO Overflow) is set to indicate the overflow. This bit and the FIFO control logic is reset by disabling and re-enabling the FIFO control bit (WR15 bit 2). For details of FIFO control timing during an SDLC frame, refer to Figure 40.

BYTE COUNTER DETAIL

The 14-bit byte counter allows for packets up to 16K bytes to be received. For a better understanding of its operation, refer to Figures 39 and 40.

ENABLE

The byte counter is enabled in the SDLC/HDLC mode.

RESET

The byte counter is reset whenever an SDLC flag character is received. The reset is timed so that the contents of the byte counter are successfully written into the FIFO.

INCREMENT

The byte counter is incremented by writes to the data FIFO. The counter represents the number of bytes received by the ESCC, rather than the number of bytes transferred from the ESCC. (These counts may differ by up to the number of bytes in the receive data FIFO contained in the ESCC.)

ABSOLUTE MAXIMUM RATINGS

Voltages on all pins with respect to GND	-0.3 V to + 7.0 V
Operating Ambient Temperature	0°C to +70°C
Storage Temperature	-65°C to + 150°C

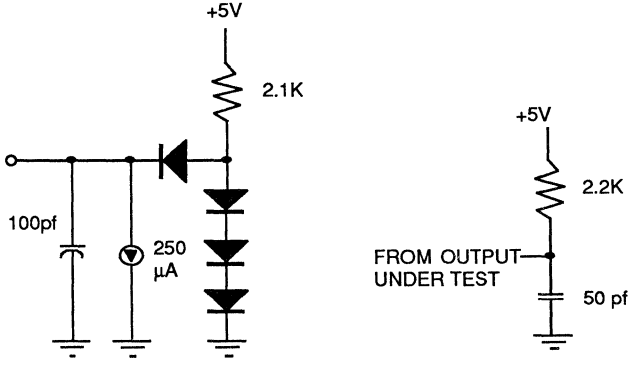
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those listed on the operational sections of this specification is not implied and exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The dc characteristics and capacitance section below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin.

Standard conditions are as follows:

- 4.75 V ≤ VCC ≤ 5.25 V
- GND = O V
- TA = 0°C to +70°C



DC CHARACTERISTICS: VCC = 5 V ± 5%, TA = 0°C to 70°C

Symbol	Parameter	Min	Max	Unit	Conditions
VIH	Input HIGH Voltage	2.0	VCC + 0.3	V	
VIL	Input LOW Voltage	-0.3	0.8	V	
VOH	Ouput HIGH Voltage	2.4		V	IOH = -250 µA
VOL	Output LOW Voltage		0.4	V	IOH = +2.0 mA
IIL	Input Leakage		±10.0	µA	0.4 V ≤ VIN ≤ +2.4 V
IOL	Output Leakage		±10.0	µA	
ICC	VCC Supply Current		250	mA	

CAPACITANCE: VCC = 5 V ± 5%, TA = 0°C to 70°C

Symbol	Parameter	Min	Max	Unit	Conditions
CIN	Input Capacitance		10	pF	
COUT	Output Capacitance		15	pF	
CI/O	Bidirectional Capacitance		20	pF	

f = 1 MHz over specified temperature range. Unmeasured pins returned to ground.

VLSI TECHNOLOGY, INC.

SECTION 7
TELECOMM PRODUCTS

Application Specific
Logic Products Division

VL7C103

300 BAUD MODEM

FEATURES

- Low cost single chip 300 BPS modem
- Full answer and originate option
- Uses switched capacitor filters
- Implements all filters and hybrid circuits on chip
- Output level up to -9 dBm with 600Ω line impedance
- Analog loopback capability for testing
- Power down mode for low power use
- Low power consumption, single +5V CMOS design
- Bell 103 compatible
- Direct replacement for the National Semiconductor NS74HC943
- Functional replacement for Texas Instruments TMS99532

DESCRIPTION

The VL7C103 is a single chip, full duplex, 300 Bit Per Second (BPS) modem compatible with the Bell 103 specifications. It is intended for data communications over the general switched telephone network, and can also be used with other voice band channels.

The VL7C103 requires a single +5 volt power supply and is implemented in 3-micron switched capacitor technology. This part is pin-for-pin compatible with the National Semiconductor NS74HC943, and functionally compatible with the Texas Instruments TMS99532.

Applications include integrated and stand-alone low speed modems for terminals, personal computers, business systems, remote diagnostic systems and business machines. Since the VL7C103 is a CMOS circuit, it is ideal for built-in modems in portable or lap-top computers.

PIN DIAGRAM

VL7C103

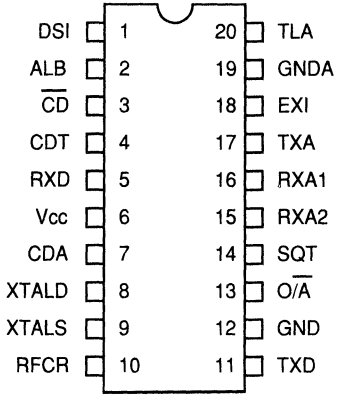
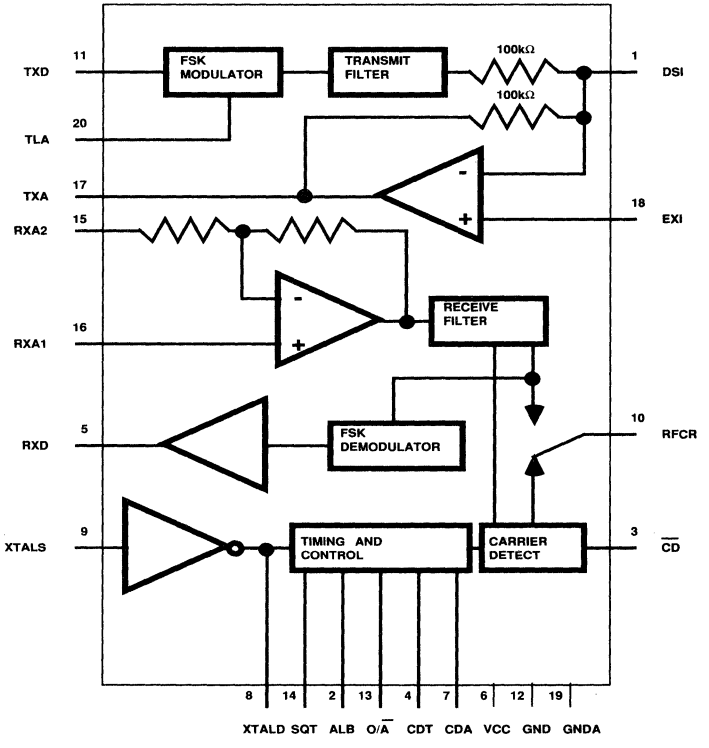


FIGURE 1. BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL7C103-PC	Plastic DIP
VL7C103-CC	Ceramic DIP

Note:
Operating temperature range: 0° to+70°C

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias - 10°C to + 80°C

Storage Temperature Range - 65°C to +140°C

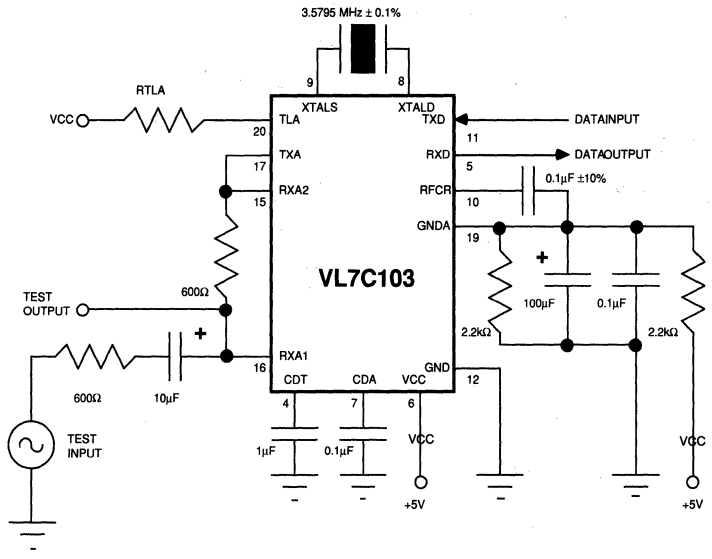
Power Supply Voltage Range - 0.5V to +7.0V

Input Voltage Range (any input) - 0.5V to +7.0V

Continuous Power Dissipation 500mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may effect device reliability.

FIGURE 2. VL7C103 AC SPECIFICATION CIRCUIT



OPERATING CONDITIONS

Parameter	Description	Conditions	Min	Typ	Max	Units
TA	Ambient Temperature		0		70	°C
VCC	Positive Supply Voltage		4.5	5.0	5.5	V
GND	Ground			0		V
GNDA	Analog Ground			1/2 VCC		V
FC	Crystal Frequency		3.576	3.5795	3.583	MHz
TR, TF	Input Rise or Fall Time				500	ns

TABLE 1. BELL 103 TRANSMIT AND RECEIVE TONES

	High Band	Low Band
Mark	2225 Hz	1270 Hz
Space	2025 Hz	1070 Hz

TABLE 2. RESISTOR VALUES FOR THE ADJUSTMENT OF THE TRANSMIT LEVEL AT VCC=5.0VDC

Line Loss (dB)	Transmit Level (dBm)	Programming Resistor (Rtla)
0	-12	Open Circuit
1	-11	19.8kΩ
2	-10	9.2kΩ
3	-9	5.49kΩ

PIN DESCRIPTION

Pin Description

Pin Number	Pin Name	Function
1	DSI	Driver Summing Input; used to transmit externally generated tones such as DTMF dialing signals. When not used, this pin should be left open. See functional description for details on how to use this input.
2	ALB	Analog Loopback; low for normal operation, high for looping back the modulator output to the demodulator input. If ALB and SQT are simultaneously held high, the chip powers down.
3	$\overline{CD}$	Carrier Detect output; goes low when carrier is detected.
4	CDT	Carrier Detect Timing output; a capacitor on this pin sets the time interval that the carrier must be present before CD goes low. For testing purposes, if this pin is connected to pin 12, then RFCR will be connected to the output of the receive filter.
5	RXD	Received Data - the data output.
6	VCC	Positive (+5V) power supply.
7	CDA	Carrier Detect Adjust input; this is used for adjustment of the carrier detect threshold. Carrier detect hysteresis is set at 3 dB. For testing purposes, if this pin is connected to pin 12, the Transmit filter can be tested by using TLA as an input driven from a low output resistance signal source and TXA as the output.
8	XTALD	Crystal oscillator output; should be connected to a 3.579545 MHz crystal. It can also be driven by an external clock.
9	XTALS	Crystal oscillator input; should be connected to a 3.579545 MHz crystal. If external clock is used, this pin must be left open.
10	RFCR	Receive Filter/Carrier Rectifier; this normally connected to the output of the carrier rectifier. If CDT is connected to pin 12, then this pin is disconnected from the rectifier and instead it will be connected to a high impedance output of the receive filter. It may thus be used to evaluate filter performance. For normal modem operation, RFCR is AC grounded (pin 19) via a 0.1 µF bypass capacitor.
11	TXD	Transmit Data - the data input.
12	GND	Ground (0V)
13	O/$\overline{A}$	Originate/Answer mode select; when high (low), this pin selects the originate (answer) mode of operation.
14	SQT	Squelch Transmitter; this disconnects the modulator output from the line driver input when held high. The EXI input, however, remains active. If SQT and ALB are held high simultaneously, the chip will power down.
15	RXA2	Receive Analog (2); RXA2 and RXA1 are analog inputs. When connected as recommended, they produce a balanced hybrid.
16	RXA1	Receive Analog (1); see RXA2 for details.
17	TXA	Transmit Analog output; line driver output.
18	EXI	External Input; this is a high impedance input to the line driver. This input may be used to transmit externally generated tones. When not used for this purpose, it should be connected to pin 19. See functional description for further details on how to use this input.
19	GNDA	Analog Ground (1/2 VCC).
20	TLA	Transmit Level Adjust; a resistor from this pin to VCC sets the transmit level.

FUNCTIONAL DESCRIPTION

The VL7C103 modem can be used to transmit and receive serial digital data over general switched telephone networks, leased lines, or other equivalent narrow band channels. Up to 300 bits per second can be transmitted and received simultaneously.

TRANSMITTER

As shown in the block diagram, the digital input data (TXD) is first modulated by the frequency shift keying (FSK) modulator. FSK modulation is performed according to Bell 103 specifications as listed in Table 1.

To separate the transmit and receive signals, the originating modem transmits in the low band while the answering modem transmits in the high band. The transmit filter smooths and band limits the modulator output. The nominal center frequency of this filter is placed at 2125 Hz or 1170 Hz depending on whether the modem is in the answer mode or in the originate mode, respectively.

The output of the transmit filter goes through the line driver and appears at TXA (Pin 17). The signal level at TXA can be controlled by connecting a resistor between TLA (Pin 20) and VCC (Pin 6). The open circuit voltage on pin 20 is 0.1 VCC. The transmitted power levels shown in Table 2 refer to the power delivered to a 600Ω source impedance. The voltage on the load is half the TXA voltage.

RECEIVER

The analog signal received from the line is buffered by the hybrid circuit and filtered by the receive filter. The receive filter is similar to the transmit filter except that it always operates at the band opposite to the transmit filter band. When the transmit filter operates at the high band, the receive filter operates at the low band and vice versa. The output of the receive filter is hard limited and demodulated by the FSK demodulator. The demodulator output appears at RXD (Pin 5).

CARRIER DETECTOR

An adaptive level detector responds to the presence of signal energy within the receive band and generates an active low logic level on the CD output (Pin 3). This circuit has a built-in hysteresis of 2dB, minimum. Typically, CD is activated when the received signal power exceeds - 44dBm (VON = 4.9mVrms) and CD is deactivated when the signal drops below -47dBm (VOFF=3.5mVrms). This hysteresis prevents oscillatory operation of the carrier detector when the received signal is close to the detection threshold.

CARRIER DETECT THRESHOLDS

The threshold levels can be changed by applying a voltage to CDA (Pin 7) according to the equation below:

VCDA = 244 X VON (Volt)
VCDA = 345 X VOFF (Volt)

VCDA is referenced to pin 19.
The open circuit voltage on pin 7 is 0.24 VCC.
Converting VON and VOFF to equivalent power level (across 600Ω resistor) in dBm:

$$VCDA = 189 \times 10^{PON/20} \text{ or}$$

$$PON = 20 \log_{10}(VCDA/189)$$

$$VCDA = 267 \times 10^{POFF/20} \text{ or}$$

$$POFF = 20 \log_{10}(VCDA/267)$$

where PON and POFF are in dBm and VCDA is in volts.

CARRIER DETECT TIMING

To reduce the effects of impulse noise and false triggering of the carrier detector, CD only goes low (active) when a carrier is detected and present for at least a time equal to TON. Also, to deactivate CD (i.e., going from low to high), the carrier must be removed for at least a time equal to TOFF. TON and TOFF can be adjusted by proper selection of the capacitor on CDT (pin 4) according to the following equations:

TON ~6.4 X CCDT

TOFF ~0.54 X CCDT

where CCDT is in µF and TON and TOFF are in seconds.

LINE HYBRID

To attenuate the transmitted signal at TXA before it is fed back to the receiver input, TXA can be connected externally to RXA2 and also connected via a 600 ohm resistor to RXA1.

If the line impedance is also 600 ohms, then the transmit signal will appear as a common mode signal to the receiver and will effectively be eliminated. However, because the line impedance characteristics vary considerably, a perfect match with a fixed resistor rarely occurs and part of TXA is fed back to the receiver.

TRANSMIT SQUELCH

When SQT is held high, the transmitter will be squelched and only the signals at EXI or DSI, if any, may be transmitted. See DSI below.

ANALOG LOOPBACK

When ALB is held high, the output of the line driver is looped back to the input of the receive filter. This feature can be used for testing the modem if the modem is in the originate mode, then the transmit and receive filters will be turned to the low band. On the other hand, when the modem is in the answer mode, both filters will tune to the high band.

ORIGINATE/ANSWER MODES

When the modem is in the originate mode (O/A = high), it will transmit in the low band and receive in the high band. This situation is reversed when the modem is in the answer mode (O/A = low).

POWER DOWN MODE

To power down, SQT and ALB should be held high simultaneously.

DSI

This input can be used to transmit externally generated signals, such as DTMF tones, while the modem is in the squelched mode. The external tone should be capacitor coupled through a

resistor into this pin. The gain of the transmit amplifier will then be determined by the ratio of the on-chip feedback resistor (typically 100K ohms) and the external series resistor. Since the on-chip resistor value can vary by ±25%, it is recommended that the EXI pin be used as described below for accurate control of transmitted tone level. When this pin is not used, it should be left open.

EXI
This input can be used to transmit externally generated signals, such as DTMF tones, while the modem is in squelched mode with DSI left open. The external tone should be capacitor coupled into this pin with a resistor (typically 100k ohms) connected between this pin and analog ground (pin19). Used in this manner, the transmitted tone level is twice the input tone level since the transmit amplifier is configured internally as a gain of 2 stage. When this pin is not used, it should be connected to pin 19.

RFCR
This output pin is normally connected to the output of the full-wave rectifier of the carrier detect circuit. To test the output of the receive filter, CDT should be connected to pin 12 to disable the rectifier circuit. In this case, RFCR will be connected to the receive filter output and can be used for testing the receive filter.

CHARACTERISTICS

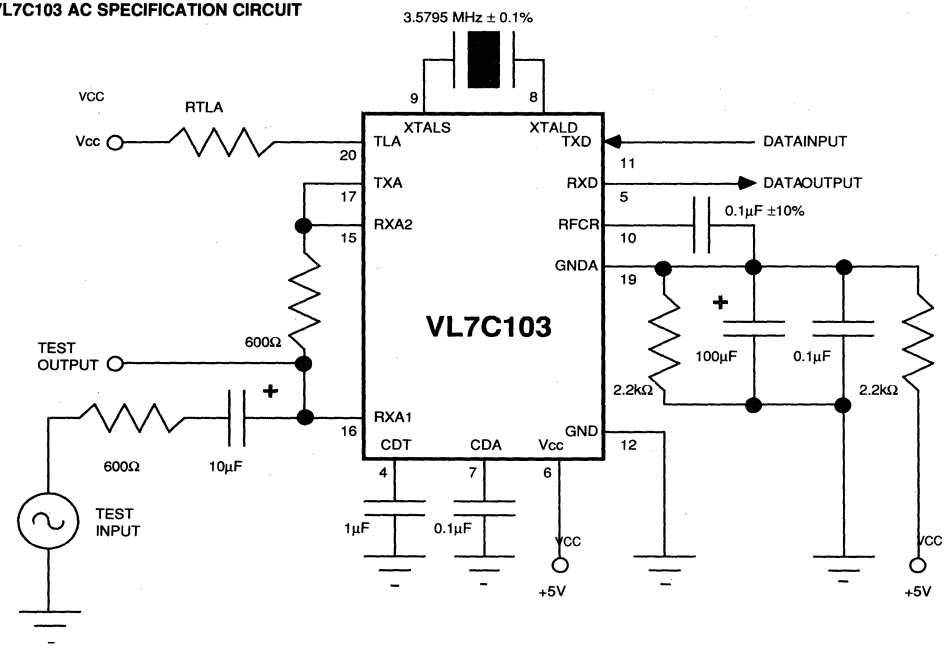
Unless otherwise specified, all specifications apply to the test circuit shown in Figure 2. The demodulator specifications apply to operating VL7C103 with a modulator having frequency accuracy, phase jitter, equal to or better than the VL7C103 modulator. Typical values are at 25°C and VCC = 5.0V (Demodulator includes hybird, receive filter and discriminator.).

Parameter	Conditions	Min.	Typ.	Max.	Units
TRANSMITTER					
Carrier Frequency Error				2	Hz
Power Output Delivered to Line	VCC = 5.0V, RL = 1200Ω RTLA = 5490Ω RTLA open		 -9 -12		 dBm dBm
Second Harmonic Energy	RTLA open		-60		dBm
RECEIVE FILTER AND HYBRID					
Hybrid Input Resistance (pins 15 and 16)			100		kΩ
RFCR Output Resistance	Pin 10, No external Capacitor		30		kΩ
Adjacent Channel Rejection	TXD = GND or VCC Input to RXA1:RXA2 = GNDA	 60			 dB
DEMODULATOR					
Maximum Carrier Amplitude			-12		dBm
Minimum Carrier Amplitude			-47		dBm
Dynamic Range			35		dB
Bit Jitter	SNR = 30dB Input = -38dBm Baud Rate = 300		 100		 µs
Bit Bias Distortion			5		%
Carrier Detect Trip Points	CDA = 1.2V (Referenced to pin 19) Off to On On to Off		-44 -47		dBm dBm

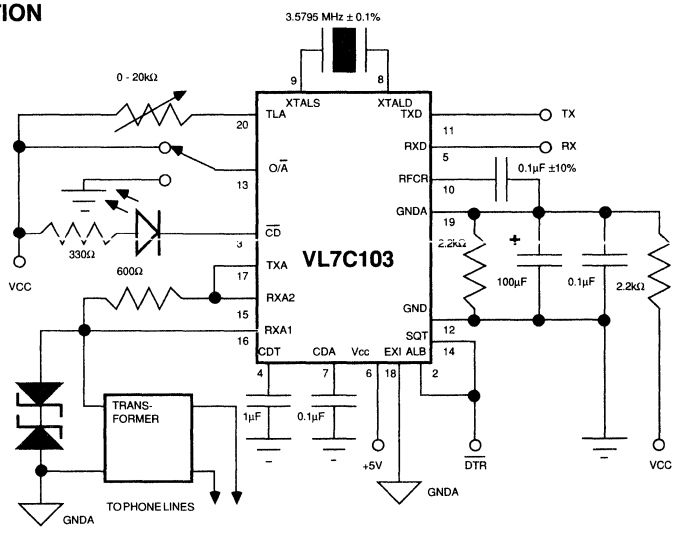
DC CHARACTERISTICS TA= 0°C to +70°C, VCC= 5V ±10%, GND= 0V, Typical values are for 25 °C

Parameter	Description	Conditions	Min	Typ	Max	Units
VIH	High Level Input Voltage		3.15			V
VIL	Low Level Input Voltage				1.0	V
VOH	High Level Output Voltage	VIN = VIH or VIL |IOUT| = 20µA |IOUT| = 4mA, VCC = 4.5V	VCC-0.1 3.7	VCC		V V
VOL	Low Level Output Voltage	VIN = VIH or VIL |IOUT| = 20µA |IOUT| = 4mA, VCC = 4.5V |IOUT| = 15mA (Pin 3)			0.1 0.4 0.5	V V V
IIN	Input Current	VIN = VCC or GND			±1.0	µA
ICC	Quiescent Power Supply Current	ALB or SQT = GND Transmit Level = -9dBm		8		mA
ICC	Power Down Supply Current	ALB = SQT = VCC VIH = VCC VIL = GND			250	µA

FIGURE 3. VL7C103 AC SPECIFICATION CIRCUIT



TYPICAL APPLICATION



VL7C211

212A/V.22 MODEM FILTER

FEATURES

- Transmit-and-Receive filter with half-channel compromise amplitude and group delay equalization
- Built-in Call Progress Mode and Answer / Originate Mode switching
- Bell 212A and CCITT V.22 compatible, with V.22 notch filters included
- Analog loop-back capability for in circuit testing
- Improved data transmission characteristics for lower bit error rate
- No external logic or multiplexers required
- Supports both North American and European modem designs

DESCRIPTION

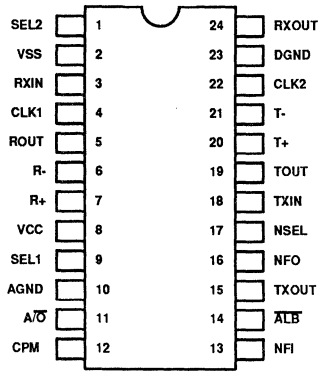
The VL7C211 modem filter is a monolithic CMOS switched-capacitor filter circuit designed for use in full-duplex 1200-bit-per-second modems. It meets the filtering requirements of the Bell 212A and CCITT V.22 modem specifications and includes high-band (2400 Hz) and low-band (1200 Hz) filters, half-channel compromise amplitude and group delay equalizers for both bands, and smoothing filters for both bands. For CCITT V.22 applications, a notch filter is included that can be programmed for either 550 Hz or 1800 Hz. Also included in the VL7C211 filter are two uncommitted operational amplifiers that can be used for anti-aliasing filters or for gain control.

The VL7C211 is pin and function compatible with the Sierra SC11005, the AMI S35212 and S35212A. Further, the high-band filter in this filter can be scaled by a factor of six so that it can be used to monitor call progress tones in an intelligent modem. And, like the S35212A, it contains analog loop-back so that the signal path can be completely tested.

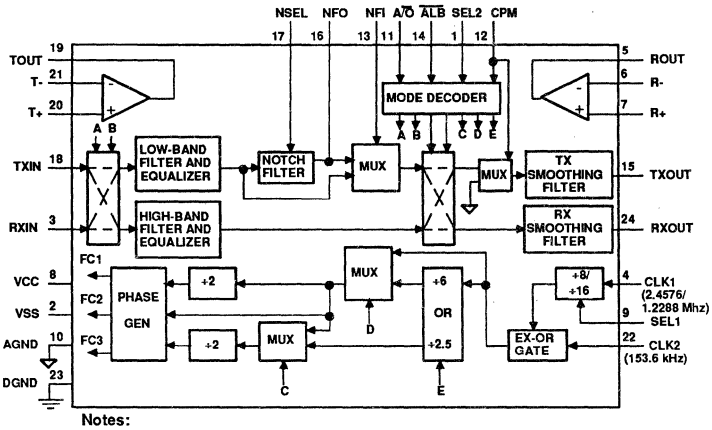
The VL7C211 offers enhanced call progress monitoring features and is pin and function compatible with the Sierra SC11001. It contains two pins, CPM (pin 12) and NFI (pin 13), that allow more accurate call progress monitoring and easier V.22 implementation without the need for extra multiplexers or logic. Besides being able to scale the high-band filter by a factor of six, the low-band filter can be scaled by a factor of 2.5 for better centering over the call progress frequency range of from 300 to 660 Hz. It also allows the unscaled high-band filter to be used for monitoring the modem answer tone, simplifying the design of full auto-dial / auto-answer modems.

PIN DIAGRAM

VL7C211



BLOCK DIAGRAM



Notes:

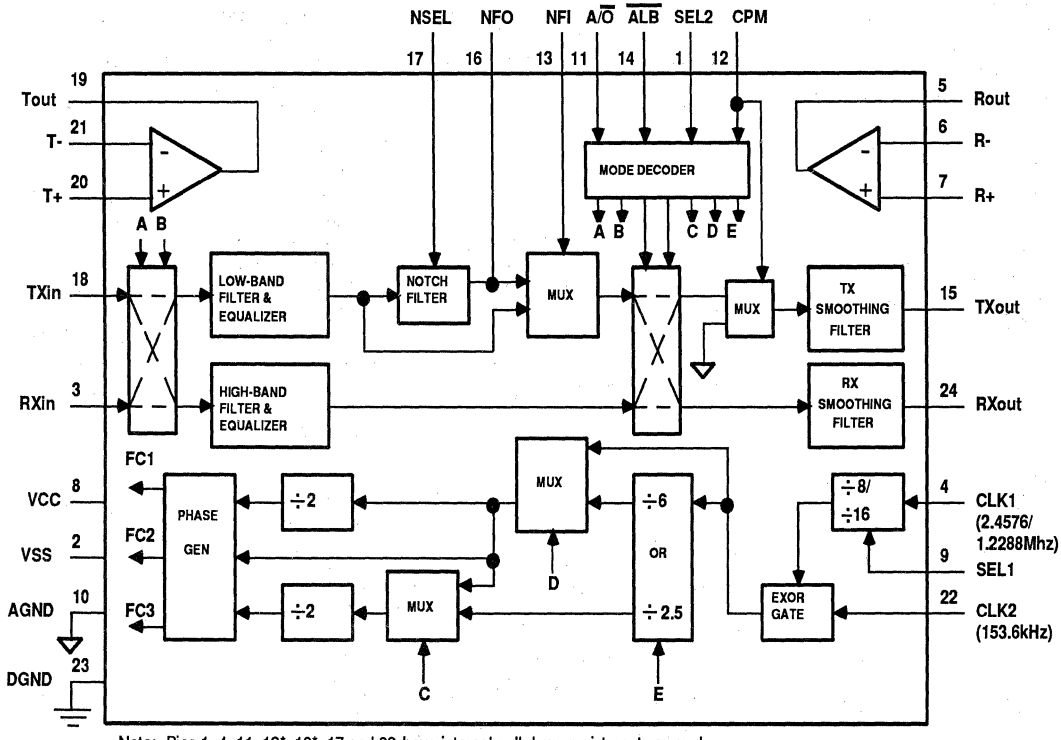
1. Pins 1, 4, 11, 12, 13, 17, and 22 have internal pull-down resistors to ground.
2. Pin 14 has an internal pull-up to VCC.

ORDER INFORMATION

Part Number	Package
VL7C211-PC	Plastic DIP
VL7C211-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range: 0°C to +70°C.

FIGURE 1. BLOCK DIAGRAM



Note: Pins 1, 4, 11, 12*, 13*, 17 and 22 have internal pull-down resistors to ground.
Pin 14 has an internal pull-up to VCC.

SIGNAL DESCRIPTIONS

Pin Number	Signal Name	Description
1	SEL2	Call progress mode selection LOW for normal operation, HIGH for scaling the high-band filter by six for call progress monitor.
2	VSS	Negative supply voltage
3	RXin	Receive signal input
4	CLK1	Clock input 1; 2.4576 MHz with SEL1 HIGH or 1.2288 MHz with SEL1 LOW.
5	Rout	Output of the R amplifier
6	R-	Inverting input of the R amplifier
7	R+	Non-inverting input of the R amplifier
8	VCC	Positive supply
9	SEL1	Selects clock frequency into pin 4; LOW for 1.2288 MHz or HIGH for 2.4576 MHz.
10	AGND	Analog ground
11	A/$\overline{O}$	Answer / originate mode selection; HIGH for answer, LOW for originate.
12	CPM	Enhanced call progress mode selection LOW for normal operation; HIGH to scale down the low-band filter by 2.5 for enhanced call progress monitoring.
13	NFI	Notch filter insert; LOW for notch filter bypass, HIGH to insert notch filter.
14	$\overline{ALB}$	Analog loop-back; HIGH for normal operation, LOW to loop-back TXout to RXin.
15	TXout	Transmit signal output
16	NFO	Notch filter output
17	NSEL	Notch filter selection; LOW for 550 Hz, HIGH for 1800 Hz.
18	TXin	Transmit signal input
19	Tout	Output of the T amplifier
20	T+	Non-inverting input to the T amplifier
21	T-	Inverting input to the T amplifier
22	CLK2	Clock input 2; 153.6 KHz
23	DGND	Digital ground
24	RXout	Receive signal output

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias
-10°C to +80°C
Storage Temperature Range
-65°C to +140°C
Operating Temperature Range
(Plastic DIP, PLCC)
0° to +70°C
Maximum Supply Voltage
VCC = +7 V
VSS = -7 V
Input Analog Voltage Range
(pins 3, 6, 7, 18, 20, 21)
VCC + 0.6 V Max
VSS - 0.6 V Min
Input Digital Voltage Range
(pins 1, 4, 9, 11, 12, 13, 14, 17,22)
VCC + 0.6 V Max
VSS - 0.6 V Min
Maximum Power Dissipation
(Plastic DIP, PLCC)
500 mW @ 25°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device under these or any conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

TA = 0°C to 70°C, VCC = 5.0 V ±10% unless otherwise noted

Symbol	Parameter	Co	Conditions	Min	Typ	Max	Units
ICC	+5V Quiescent Current		No Load		7.5	15	mA
ISS	-5V Quiescent Current		No Load		7.5	15	mA
VIH	High Level Input Voltage; Digital Signal pins 1, 4, 9, 11, 12, 13, 14, 17, 22			2.0			V
VIL	Low Level Input Voltage; Digital Signal pins 1, 4, 9, 11, 12, 13, 14, 17, 22					0.8	V
VOMAX	Output Signal; pins 5, 15, 16, 19, 24		VCC=+5V, VSS=-5V, RL = 10kΩ (pins 5, 19) RL = 20kΩ (pins 15, 16, 24)	±3			V

PERFORMANCE CHARACTERISTICS

TA = 25°C, VCC = +5 V, VSS = VSS = -5 V, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Output Noise RXout, TXout			30	33	dBrnC0
Crosstalk		55	60		%
Total Harmonic Distortion			0.3		dB
Dynamic Range			70		dB
Adjacent Channel Rejection:					dB
Low-Band		55	65		dB
High-Band		55	75		dB
Passband Gain at Center Frequency (1200 Hz, 2400 Hz)		-1		+1	dB
Relative Gain: Low-Band Reference = 1200 Hz	@300 Hz			-35	dB
	@800 Hz	-1		-1	dB
	@1600 Hz	-1.5		+1	dB
	@1800 Hz			-18	dB
	@2000 Hz			-48	dB
	@2400 Hz			-55	dB
	@2800 Hz			-50	dB
Relative Gain: High-Band Reference = 2400 Hz	@800 Hz			-50	dB
	@1200 Hz			-53	dB
	@1600 Hz			-50	dB
	@2000 Hz	-2.5		+0.5	dB
	@2800 Hz	0		+2.5	dB
	@3200 Hz			-10	dB
	@3500 Hz			-20	dB
Relative Gain: Low-Band NFI = HIGH	@550 Hz, NSEL = LOW			-45	dB
	@1800 Hz, NSEL = HIGH			-45	dB

FUNCTIONAL DESCRIPTION

LOW-BAND FILTER

The low-band filter is a 10th-order, switched-capacitor, band-pass filter with a center frequency of 1200 Hz. (See figure 3 for the amplitude response of this filter.) In the originate mode, this filter is used in the transmit direction; in the answer mode, it is used in the receive direction. When analog loop-back is used in the originate mode, this filter, together with the low-band delay equalizer is in the test loop. In the call progress monitoring mode with SEL2 (pin 1) HIGH and CPM (pin 12) LOW, the center frequency of this filter is shifted down by a factor of six to 200 Hz. If pin 12 (CPM) is HIGH, the filter response is scaled down by 2.5, moving the center frequency to 480 Hz.

LOW-BAND DELAY EQUALIZER

The low-band delay equalizer is a 10th-order, switched-capacitor, all-pass filter that compensates for the group delay variation of the low-band and half of the compromise line characteristics, producing a flat delay response within the pass-band. (See figure 4 for the group delay response of the low-band filter cascaded with the low-band delay equalizer.)

HIGH-BAND FILTER

The high-band filter is a 10th-order switched-capacitor, band-pass filter with a center frequency of 2400 Hz. (See figure 5 for the amplitude response of this filter.) In the answer mode, this filter is used in the transmitter direction; in the receive mode, it is used in the receive direction. When analog loop-back is used in the answer mode, this filter, together with the high-band delay equalizer, is in the test loop. In the call

progress monitoring mode with SEL2 (pin 1) HIGH and CPM (pin 12) LOW, the center frequency is shifted down by a factor of six to 400 Hz. If pin 1 is LOW or pin 12 is HIGH, this filter operates in the normal data mode.

HIGH-BAND DELAY EQUALIZER

The high-band delay equalizer is a 10th-order, switched-capacitor, all-pass filter that compensates for the group delay variation of the high-band filter and half of the compromise line characteristics, producing a flat delay response for the high-band filter cascaded with the high-band delay equalizer.

TRANSMIT SMOOTHING FILTER

The transmit smoothing filter is a first-order, low-pass switched-capacitor filter.

RECEIVE SMOOTHING FILTER

The receive smoothing filter consists of a second-order, low-pass switched-capacitor filter cascaded with a second-order, active R-C, low-pass filter.

V.22 NOTCH FILTER

The V.22 notch filter is a second order, switched-capacitor notch filter. The center frequency of the filter is at 550 Hz when NSEL (pin 17) is LOW, and is shifted to 1800 Hz when NSEL is HIGH. This filter is bypassed in the low band if NFI (pin 13) is LOW. Its output, however, is always available at pin 16 (NFO).

UNCOMMITTED OPERATIONAL AMPLIFIERS

Two operational amplifiers, called the R amplifier and the T amplifier, are included as a part of the VL7C211. They are not used by the filter circuit and can be used, for example, as anti-aliasing filters or gain stages in a complete 212A modem circuit.

ANALOG LOOP-BACK

When $\overline{ALB}$ (pin 14) is LOW, the signal transmitted by the modem TXin is looped back to the modem through the RXout pin. If the low (high)-band filter / equalizer is to be tested, the A/$\overline{O}$ pin should be LOW (HIGH). The receive smoothing filter is in this loop regardless of the A/O level. An internal pull-up resistor keeps this pin HIGH when it is not connected externally.

ANSWER / ORIGINATE MODE SELECTION

When A/$\overline{O}$ (pin 11) is LOW, the modem operates in the originate mode, transmitting in the low band and receiving in the high band. If A/$\overline{O}$ is HIGH, the modem operates in the answer mode, transmitting in the high band and receiving in the low band. An internal pull-down resistor keeps this pin LOW when it is not connected externally.

CLOCK SELECTION

SEL1 (pin 9) is used to select the correct internal divider, depending on the frequency of the external clock. SEL1 is set HIGH for use with a 2.4576 MHz clock input on CLK1 (pin 4), and set LOW for a 1.2288 MHz input on CLK1. If a 153.6 KHz clock is used on CLK2 (pin 22), CLK1 (pin 4) should be left open.

NORMAL / CALL PROGRESS MODE

When SEL2 (pin 1) and CPM (pin 12) are LOW, the filter operates in the norm-al data mode. When either pin is HIGH, the filter operates in the call progress monitoring mode. When SEL2 is HIGH and CPM is LOW, the center frequencies of both the low-band and the high-band filters are shifted down to one-sixth of the frequencies used in the normal data mode. SEL2 is internally pulled down to keep it at a LOW level when it is not connected externally.

When CPM is HIGH, the low-band filter is scaled down by a factor of 2.5 (figure 7) and RXout is the output of either the scaled low-band filter, or the unscaled high-band filter, depending on the logic levels at $\overline{ALB}$ (pin 14) and A/$\overline{O}$ (pin 11), as shown in table 1.

TRANSMIT SQUELCH IN CALL PROGRESS MODE

When CPM is HIGH (call progress mode), the input of the transmit smoothing filter is disconnected and shorted to ground, squelching the transmitter. In the handshake sequence of a 212A modem, this feature can be used to eliminate any transmit signal output. An internal pull-down resistor keeps the CPM pin LOW when it is not connected externally.

APPLICATIONS

MODES OF OPERATION

The VL7C211 filter can be operated in three basic modes: a normal data mode, a test mode, and a call progress monitor mode.

NORMAL DATA MODE

Figures 8 through 11 illustrate the signal flow diagrams for the filter in the normal data mode for either a 212A or a V.22 modem. In the originate mode, the transmit signal goes through the low-band filter and the receive signal goes through the high-band filter. In the answer mode, the transmit signal goes through the high-band filter and receive signal goes though the low-band filter.

TEST MODE

The filter can be tested by entering the analog loop-back mode, as illustrated in figures 12 and 13. In this mode, the transmit signal is looped back to the RXout pin after going through either the low-band filter or the high-band filter, depending on originate or answer mode selection. The analog loop-back mode facilitates testing of the modem locally, without having to make a data call.

CALL PROGRESS MONITOR MODE

This filter operates in one of two different call progress monitoring modes, depending on whether the SEL2 or CPM pin is HIGH. If SEL2 is HIGH the center frequency of both the low-band and the high-band filters is shifted down by a factor of six and the bandwidth of the filters is also reduced by a factor of six. Thus, the high-band filter is shifted down to 400 Hz ± 80 Hz, while the low-band filter is shifted down to 200 Hz ± 80 Hz. By selecting the originate mode, the receive signal goes through the modified high-band filter, which now has a pass-band of approximately 300 Hz to 480 Hz. This allows precision dial tone of 350 / 440 Hz as well as audible ringing tone of 440 / 480 Hz to pass. However, only a portion of the busy or reorder tone of 480 / 620 Hz passes through. An external energy detector circuit, combined with a method of cadence and timing determination, distinguishes between different conditions on the line during establishing a call.

FIGURE 2. LOW-BAND AND HIGH-BAND RESPONSE, NORMALIZED

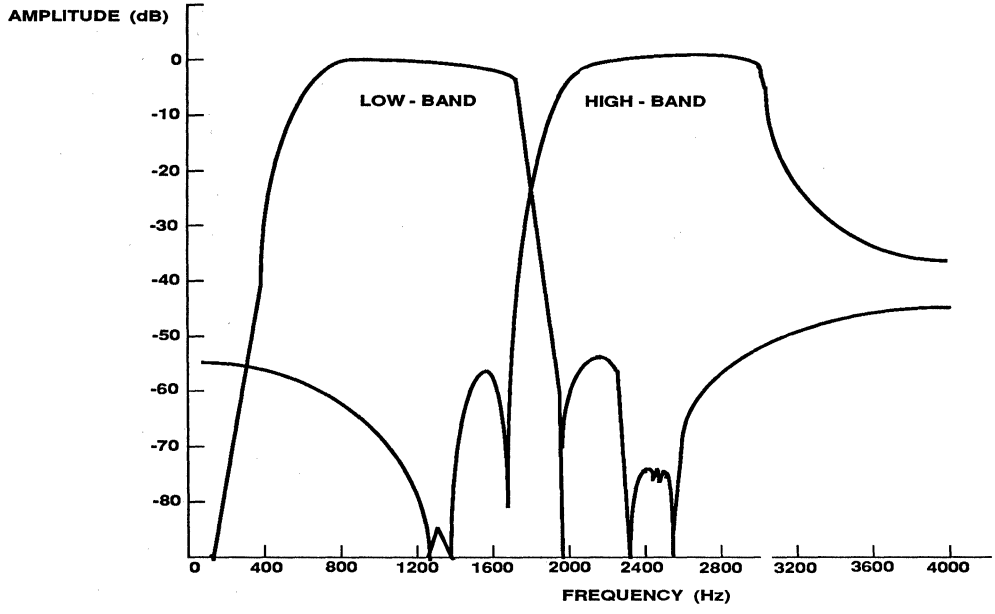


FIGURE 3. LOW-BAND RESPONSE, NORMALIZED

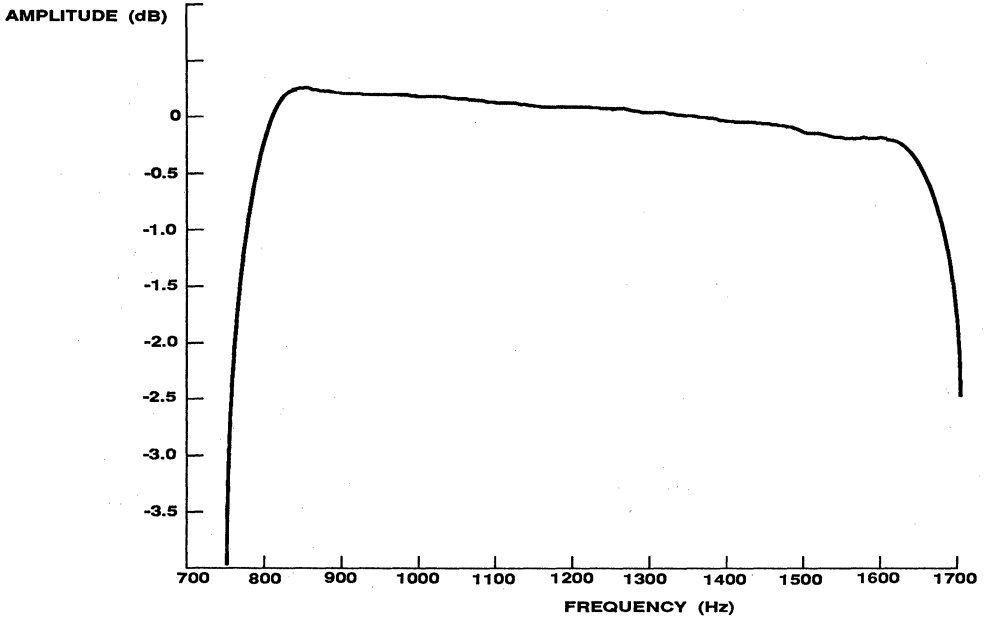


FIGURE 4. LOW-BAND GROUP DELAY (Hz)

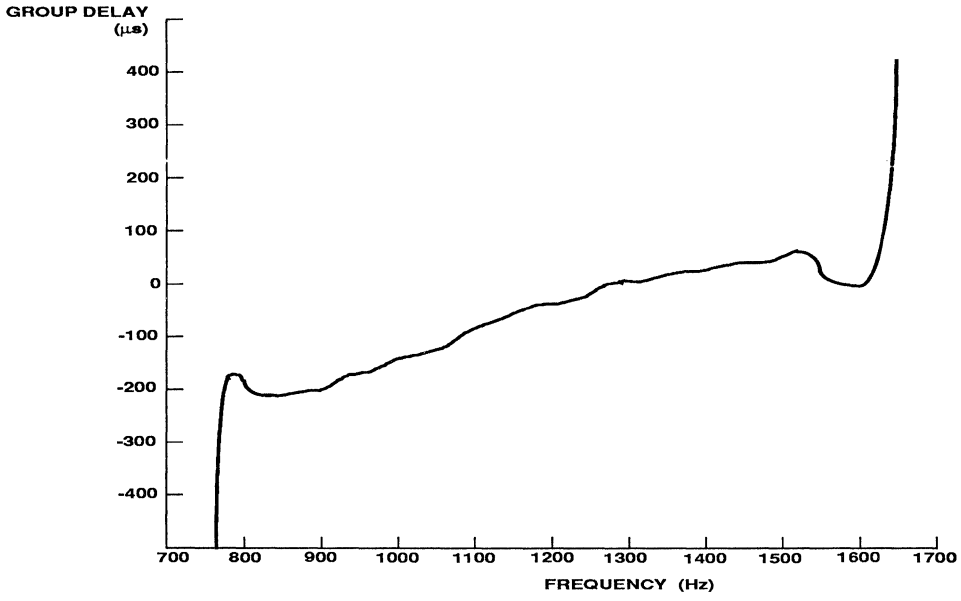


FIGURE 5. HIGH-BAND RESPONSE, NORMALIZED

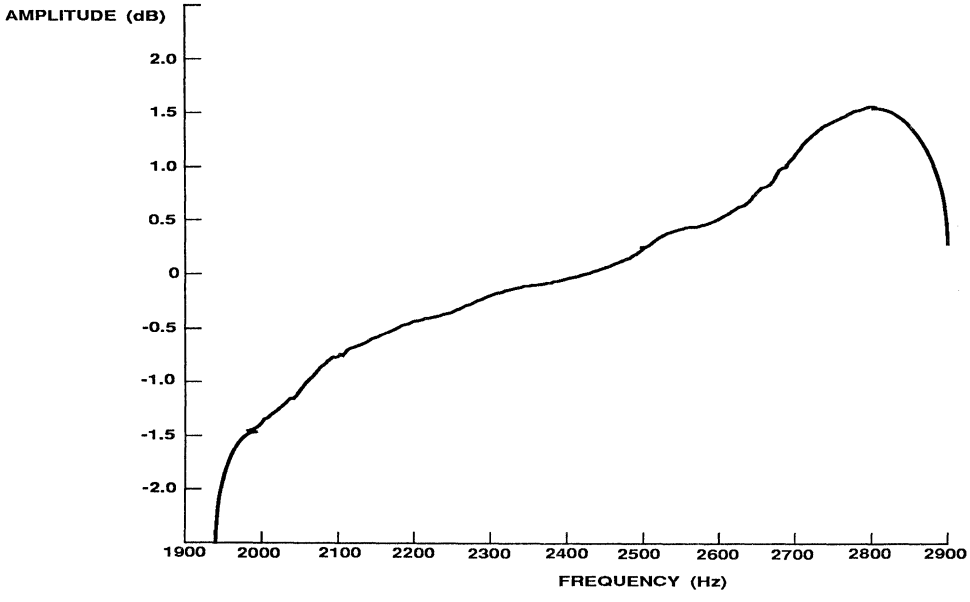


FIGURE 6. HIGH-BAND GROUP DELAY (Hz)

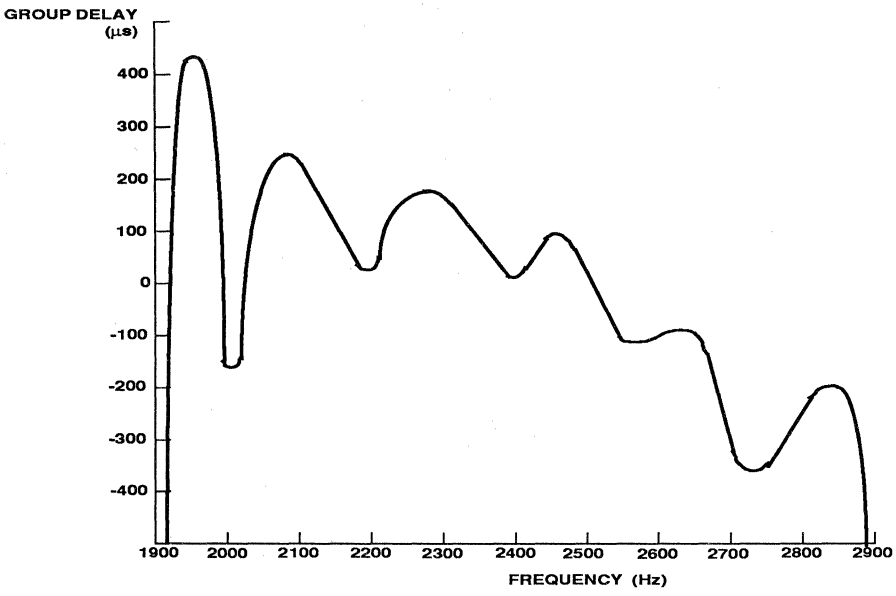


FIGURE 7. LOW-BAND DIVIDED BY 2.5 AMPLITUDE RESPONSE, NORMALIZED

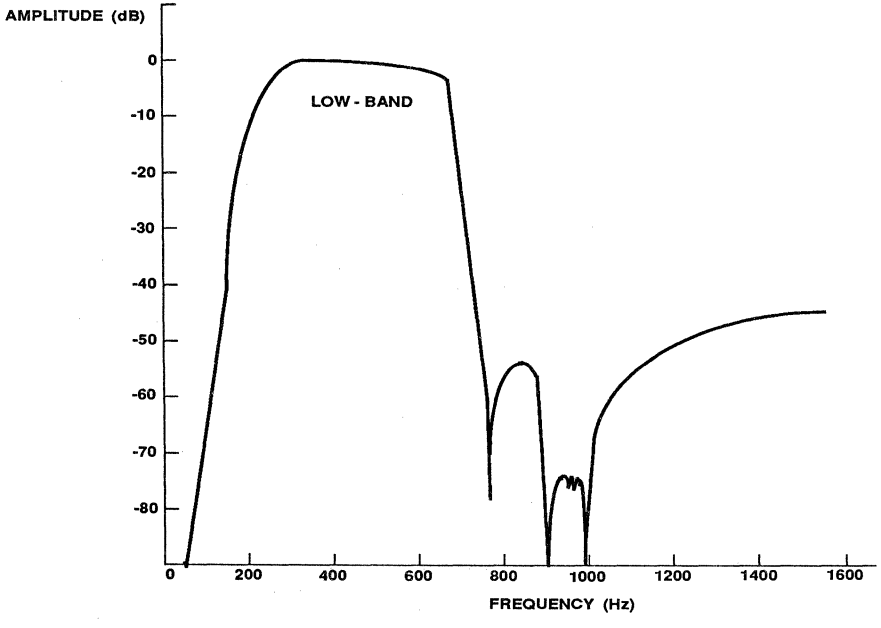


FIGURE 8. 212A ORIGINATE MODE

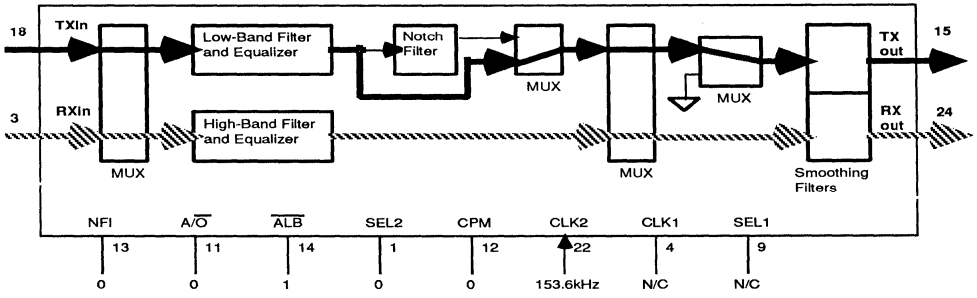


FIGURE 9. 212A ANSWER MODE

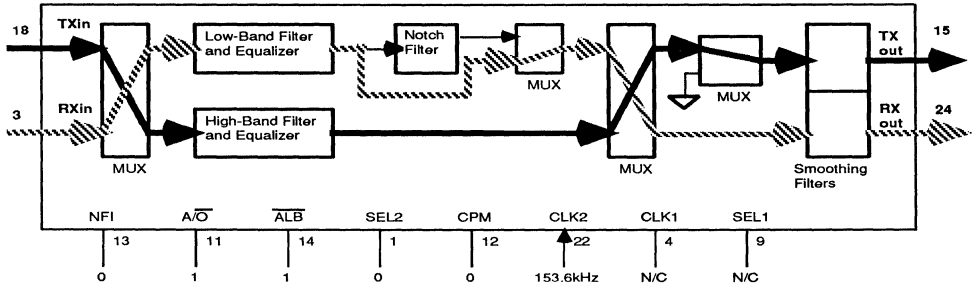


FIGURE 10. V.22 ANSWER MODE

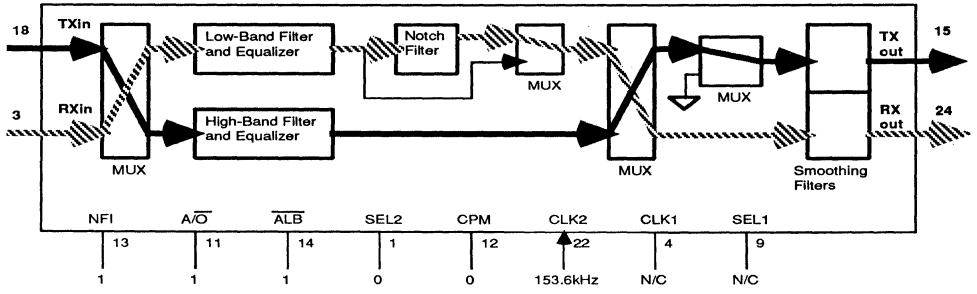


FIGURE 11. V.22 ORIGINATE MODE

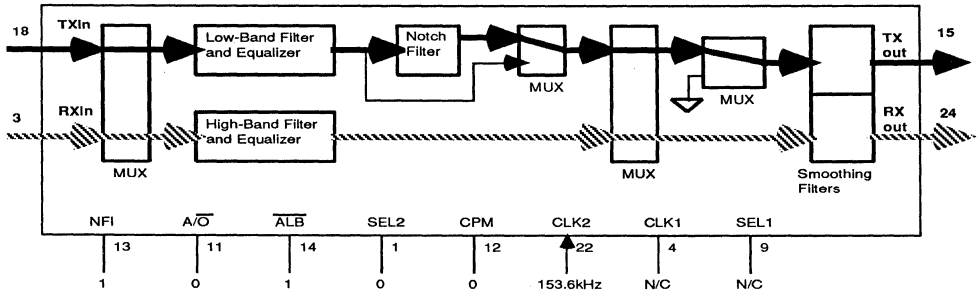


FIGURE 12. 212A ANALOG LOOP-BACK MODE UISNG LOW-BAND FILTER (ORIGINATE MODE)

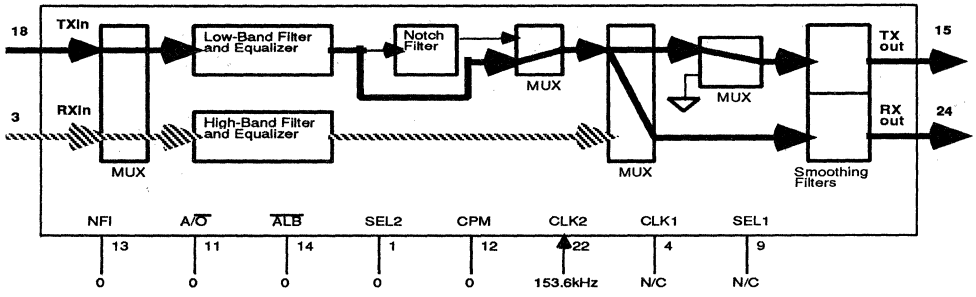


FIGURE 13. 212A ANALOG LOOP-BACK MODE USING HIGH-BAND FILTER (ANSWER MODE)

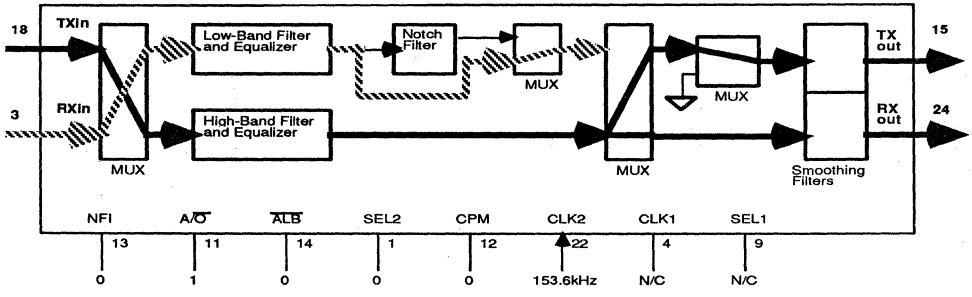


FIGURE 14. CALL PROGRESS MONITOR MODE: MONITORING ANSWER TONE/VOICE

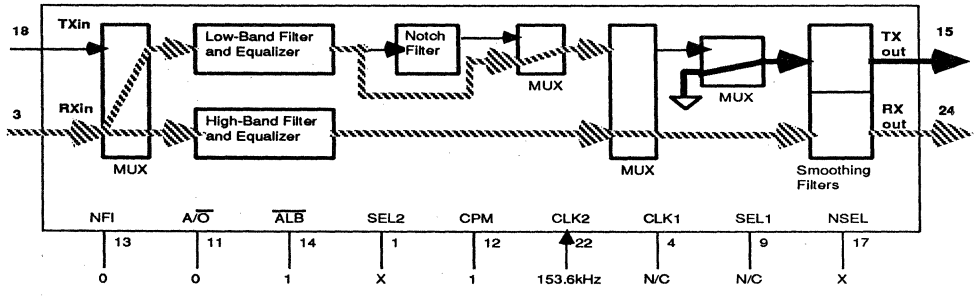


FIGURE 15. CALL PROGRESS MONITOR MODE: MONITORING CALL PROGRESS TONES

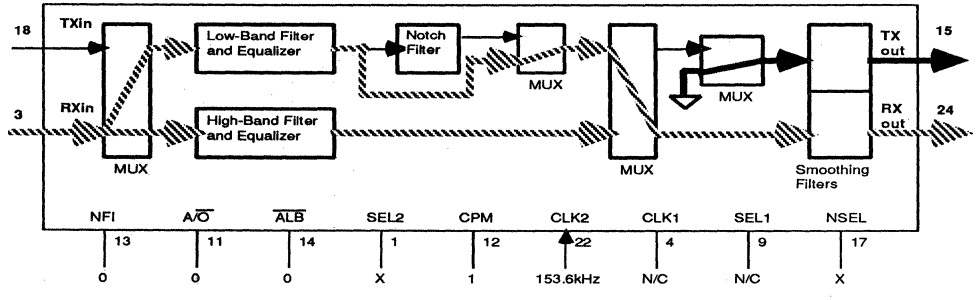


TABLE 1. OPERATING MODES

Mode	CPM	SEL2	$\overline{ALB}$	A/$\overline{O}$	TXIN	TXOUT	RXIN	RXOUT
0	0	0	1	0	L	L	H	H
1	0	0	1	1	H	H	L	L
2	0	0	0	0	L	L	H	H
3	0	0	0	1	H	H	L	H
4	0	1	1	0	L/6	L/6	H/6	H/6
5	0	1	1	1	H/6	H/6	L/6	L/6
6	0	1	0	0	L/6	L/6	H/6	L/6
7	0	1	0	1	H/6	H/6	L/6	H/6
8	1	X	1	0	-	SQT	(L/2.5 + H)	H
9	1	X	1	1	H	SQT	L/2.5	L/2.5
10	1	X	0	0	-	SQT	(L/2.5 + H)	L/2.5
11	1	X	0	1	H	SQT	L/2.5	H

Note:
1. "L" refers to a center frequency of 1200Hz.
2. "H" refers to a center frequency of 2400 Hz.
3. SQT means the transmitter output is squelched.
4. - refers to no filter connection.
5. + means connection to both filters.
6. X means "don't care".
7. By switching between modes 8 and 10, the filter can be used to detect reception of the call progress tones in the L/2.5 band as well as the answer tone in the H band.
8. The SEL2 (pin 1), CPM, $\overline{ALB}$ (pin 14) and A/$\overline{O}$ (pin 11) control the modes of operation of the filter as shown in table 1. For each combination of these pins, the table shows to which each filter input and output is connected. The "L" refers to the low-band filter with the response shown in figure 2. The "H" is used to denote the high-band filter as characterized in figure 2. When L or H is divided by a factor of six (or 2.5), this is indicated by L/6 or H/6, meaning that the frequency response is scaled down by six.

The VL7C211 features an additional mode for monitoring the call progress tones. This mode is initiated by taking the CPM pin HIGH. Two deficiencies, inherent in the first mode described above, are overcome in this enhanced mode. First, the pass-band is more accurately centered over the call progress tone frequencies because the low-band filter is scaled down by a factor of 2.5. The low-band filter thus has a pass-band of from 290 Hz to 670 Hz, which allows the busy tone to pass through completely. Second, since the high-band filter is not scaled, answer tones can be easily monitored.

The receive signal is connected to both the high-band filter and the scaled low-band filter. By toggling the ALB pin between HIGH and LOW levels, either the answer tone or the call progress tone can be monitored on the RXout pin.

Figures 14 and 15 show the signal flow diagrams in the call progress monitor mode. A method for determining conditions on the line during establishing a call is described in the following section.

CIRCUIT DESCRIPTION

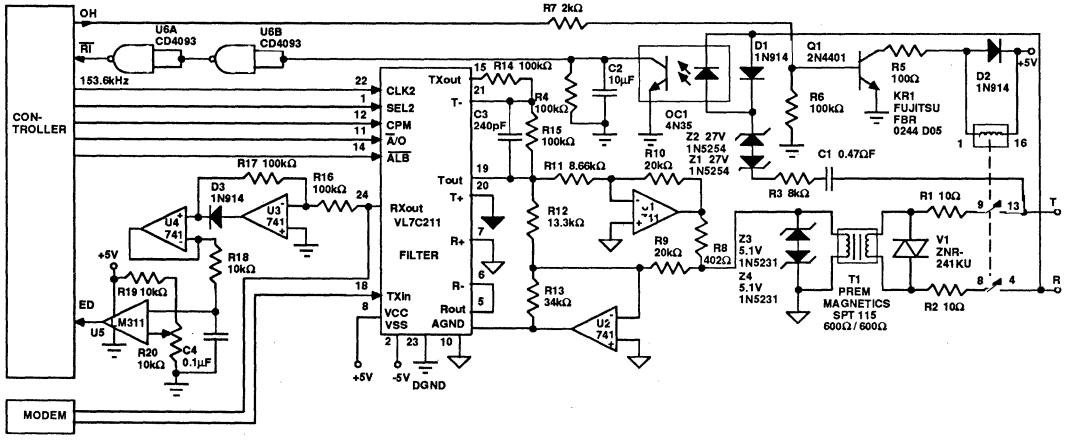
In the circuit of Figure16, op amps U1 and U2 and resistors R8 through R13 form a 2- to 4-wire converter that separates the line signal into the transmit and receive components. The receive signal is connected to the RXin input of the VL7C211 filter. In the call originate mode the signal goes through the high-band filter and comes out on the RXout pin. For call progress monitoring, the low-band filter operates in a scaled mode, thus filtering the receive signal over the range of from 290 Hz to 670 Hz. Op amps U3 and U4, comparator U5, and associated discrete components form the energy detector. U3 operates as a full-wave rectifier. U4 is a buffer that drives a low-pass filter formed by R18 and C4. The filtered signal is compared to a level set by R19 and R20. The output of U5 goes HIGH if the signal level exceeds the level set by R19 and R20. This output corresponds to the cadence information in the call prgress tone signals and can be sampled by the controller according to the detection algoithm.

TABLE 2. CALL PROGRESS TONE CHARACTERISTICS

Call Progress Tone	Hz	Cadence
Dial Tone	350 + 440* 400, 425 600 x 120 IPS**	Continuous steady tone
Audible Ring	440 + 480* 400, 450 420 x 40 IPS** 400 x 25 IPS**	2 s on/ 4 s off 1 s on/ 3 s off
Busy (Station)	480 + 620* 400, 425, 450 600 x 120 IPS**	0.5 s. on/ 0.5 s. off
Busy (circuit)	Same as above	0.25 s on/ 0.25 s off
Off Hook Alert	Multifrequency	1 s/ 1 s

Notes:
*Precision tones specified by AT&T
** IPS means interruptions per second.

FIGURE 16. A CALL PROGRESS MONITORING APPLICATION

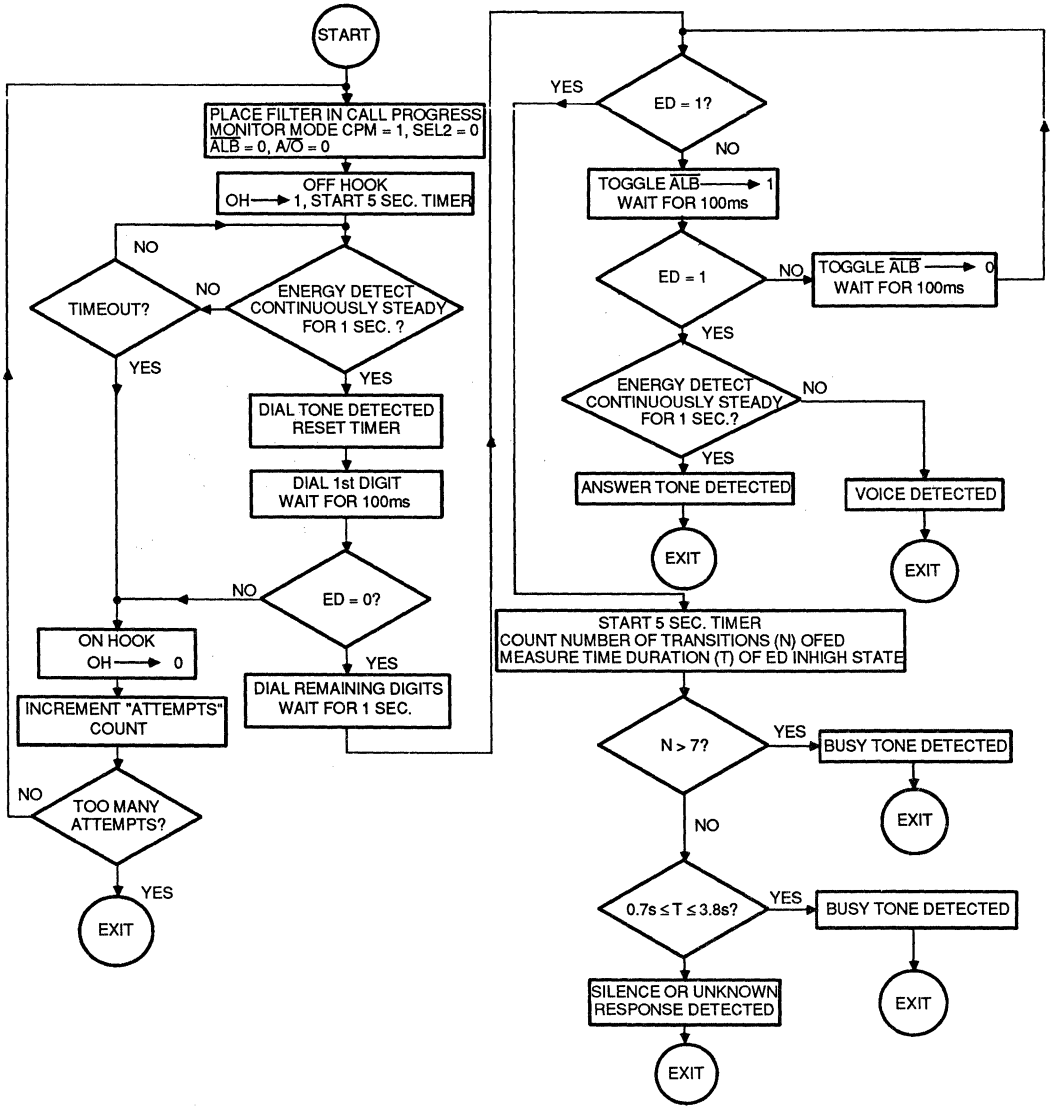


The rest of the circuitry in figure 16 performs the function of the data access arrangemetn (DAA). Transformer T1 provides isolation and sinks the line current in the off-hook state. R1, R2, V1, Z3, and Z4 provide surge protection. Relay KR1 and transistor Q1 control on-hook / off-hook conditions. C1, R3, Z1, Z2, D1 and OC1 limit and rectify the high-voltage ac ringing signal; OC1 provides isolation, R4 and C2 filter the rectified ring signal,and Schmidt trigger IC U6 converts it into a logic level for the controller.

A CALL PROGRESS MONITORING APPLICATION

Figure 16 shows a schematic for using the VL7C211 filter in a call progress monitoring application. Specifically, this arrangement is well-suited for implementing an intelligent 212A or V.22 modem. The modem can be designed to be either stand-alone with RS-232 interface to DTE or integrated into a computer with a parallel bus interface. It is assumed that a controller is available that can control the various operating modes of the filter, monitor the output of the energy

FIGURE 17. CALL PROGRESS MONITORING ALGORITHM



detector and ring indicator and control the switch-hook relay in the data access arrangement. This appli-cation illustrates how the modem filter can be used with a minimum of external circuitry to implement a fully auto-matic call establishment procedure.

Table 2 summarizes various call progress tone frequencies and their cadences. A call progress monitoring algorithm based on timing and cadence characteristics is described in the flow chart of figure 17.

DETECTION ALOGRITHM

Figure 17 shows the flowchart of a detection algorithm that utilizes the features provided in the VL7C211 filter and that uses the cadence information contained in the call progress tones to determine the status of the line. The main criterion in this algorithm was the degree of reliability it provides, rather than the speed with which it executes. For instance, dial tone is detected only when the output of the tone detector iscontinuously HIGH for at least onesecond.

If a dial tone is not detected within five seconds of going off-hook, the call is aborted. Many dialers do not wait for the initial dial tone and begin dialing as soon as going off-hook. This is termed blind dialing and is avoided in this algorithm.

Once the dial tone is detected, the first digit is dialed using the tone mode. Provision is made to check the absence of the dial tone after the first digit is dialed. If dial tone remains on the line, the controller can either hang up the line or try to dial using rotary pulse dialing. If a dial tone is absent, the rest of the digits can be pulse dialed.

The algorithm waits for one second after dialing is done to monitor the energy detector. This ensures that any clicks on the line donot cause a false detection. The $\overline{ALB}$ pin of the filter is then toggled at a 100 millisecond rate and the energy detector output is sampled to see if there is energy in the call progress band. A five second timer is started and the number of transitions of the ED output is counted (N). The cumulative duration in which the ED output is in the HIGH state is also measured (T).

The algorithm makes a determination of various conditions based on N and T. The line is determined to be busy if N exceeds 7. If N is less than 7 and T is in the range of 0.7 - 3.8 seconds, the signal is determined to be audible ringing. The controller can then count the ring cycles or start a timer. It can choose to hang up if the timer overflows or if the number of ring cycles exceeds a preset value. Any other value of N or T is classified as unknown response and is left to the controller to take the next action.

If energy is detected in the high band, the ED output is monitored to see if it is continuously HIGH for at least one second. If so, this is interpreted as the distant modem answer tone, indicating that the connection is made. If not, it indicates either silence or voice. In either case, the controller can terminate the call and take the next step. Minor variations of this algorithm or fine tuning of the decision values can provide the designer with the flexibility needed to deal with different situations. It should be emphasized that the algorithm does not stand alone and must be integrated into the application software for satisfactory performance.

VL7C212A

300/1200 BIT PER SECOND MODEM

FEATURES

- FSK and PSK modulators and demodulators, high-band and low-band filters with compromise amplitude and group delay equalizers
- Built-in call progress mode and tone generators for DTMF and V.22 guard tones
- Bell 212A and CCITT V.22 compatible; V.22 notch filters included
- Serial control interface
- Programmable audio output port
- Analog, digital and remote digital loopback capabilities
- 24 pin DIP and Plastic Leaded Chip Carrier packaging available

BENEFITS

- High level of integration provides highly cost effective 300/1200 bit per second modems
- Eliminates external components easing design of intelligent modems
- Usable in North American and European modem designs
- Simple board layout
- Simple speaker interface for monitoring phone line
- Testable signal path
- Reduced board area

GENERAL DESCRIPTION

The VL7C212A is a complete 300/1200 bit per second modem. All of the signal processing functions needed for a full duplex, 300/1200 bit per second 212A or V.22 modem, including the FSK and PSK modulators and demodulators and the high-band and low-band filters, are integrated on a single chip. Built with VTI's three micron CMOS double polysilicon process that allows analog and digital functions to be combined on the same chip, it includes capabilities for progress monitoring and for generating DTMF as well as V.22 guard tones. The two-to-four wire hybrid is also included, simplifying the interface to a DAA. The VL7C212A also includes analog loopback and remote digital loopback functions for self-testing.

PIN DIAGRAM

VL7C212A

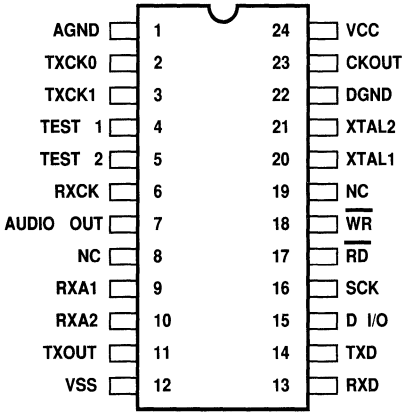
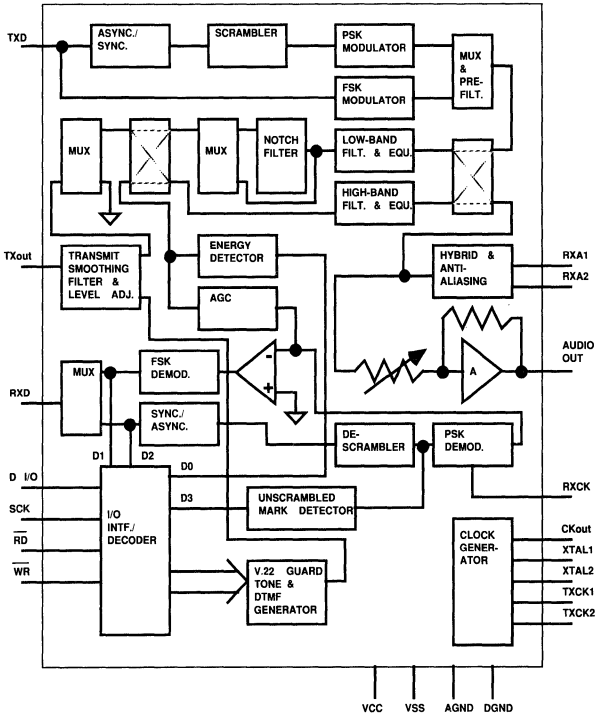


FIGURE 1. BLOCK DIAGRAM

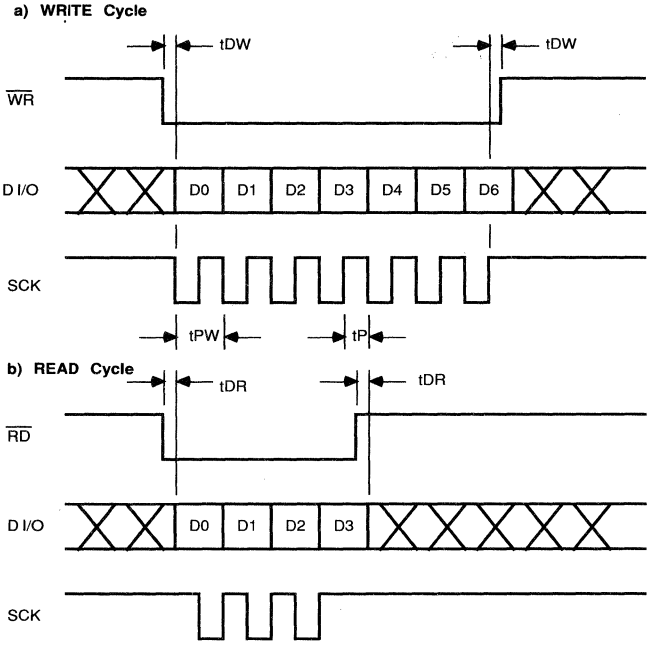


ORDER INFORMATION

Part Number	Package
VL7C212A-PC	Plastic DIP
VL7C212A-QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range:0°C to 70°C

FIGURE 2. WAVEFORMS FOR WRITE AND READ CYCLES



ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias:
-10°C to +80°C
Storage Temperature Range:
-65°C to +140°C
Maximum Supply Voltage:
VCC = +7.0V
VSS = -7.0V
Input Voltage Range:
Analog Pins; VSS-0.6V to VCC+0.6V
Digital Pins; DGND-0.6V to VCC+0.6V
Maximum Power Dissipation @25°C:
500mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional Operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may effect device reliability.

DC CHARACTERISTICS

TA= 0°C to +70°C, VCC= 5V ±5%, VSS= 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VCC	Positive Supply Voltage		4.5	5.0	5.5	V
VSS	Negative Supply Voltage		-4.5	-5.0	-5.5	V
ICC	Quiescent Current	VCC = 5V		15		mA
ISS	Quiescent Current	VCC = -5V		15		mA
Vih	HIGH Level Input Voltage	Digital Signal Pins: $\overline{RD}$, $\overline{WR}$, D I/O, SCK,TXCK1,TXD	2.0			V
Vil	LOW Level Input Voltage	Digital Signal Pins: $\overline{RD}$, $\overline{WR}$, D I/O SCK, TXCK1, TXD			0.8	V
Voh	HIGH Level Output Voltage	(D S Pins: D I/O, CKOUT , @Ioh=40µA	4.0			V
		RXD, TXCK0, RXCK) @Ioh=500µA	2.0			V
Vol	LOW Level Output Voltage	(D S Pins: D I/O, CKOUT, @Iol=160µA RXD, TXCK0, RXCK)			0.4	V
Vom	Maximum Output Signal	TXout, RL=1200Ω (TLC1=1, TLC0=0)	4.0			Vp-p
		Audio Out, RL=50 kΩ	1.0			Vp-p
Vim	Maximum Input Signal	RXA1, RXA2			2.0	Vp-p

DESCRIPTION (Continued)

With the addition of a digital controller, such as an 8-bit microcontroller and a data access arrangement (DAA), a highly cost effective, integrated, intelligent modem can be built. When used with the VTI VL7C213A modem controller, which is an 8-bit processor combined with a UART, a complete Hayes command set compatible modem can be configured, taking up a minimum of board area. For stand-alone applications, the VL7C212A modem, the VL7C213 controller, a DAA and an RS232-interface are all that are required.

The VL7C212A is truly a modem on a chip. All of the signal processing functions needed for a full duplex, 300/1200 bps Bell 212A or CCITT V.22 modem are integrated on a single chip. It operates in a synchronous or asynchronous mode and handles 8, 9, 10, or 11 bit words.

Like all modems, the VL7C212A needs a controller to determine the mode of operation, initiate the call to the remote modem (either pulse or tone dialing), set up the handshaking sequence with the remote modem, monitor the call progress tones on the line (ringing, busy, answer tone and voice) and switch into the data mode. A simple four-line serial data interface was designed for the VL7C212A, enabling it to work with just about any 8-bit microcontroller or microprocessor. The control lines are: DATA INPUT/OUTPUT, SHIFT CLOCK, READ and WRITE.

FUNCTIONAL DESCRIPTION OF THE VL7C212A MODEM

Major sections of the VL7C212A modem are a transmitter, a receiver, low-band and high-band filters, a two-to-four wire hybrid, tone generators and interface logic. It also contains an energy detector that's used for detecting the carrier and call progress monitoring and an audio output for monitoring the line.

The VL7C212A modem requires plus and minus five volts and is available in a 24 pin DIP as well as a 28 lead plastic chip carrier with "J" leads for surface mount applications. The transmitter section consists of an async/sync converter, scrambler, PSK modulator and FSK modulator. In the high speed mode (1200 bps), the PSK modulator is connected to the filter. In the low speed mode (300 bps), the FSK modulator is connected to the filter.

TRANSMITTER

Since data terminals and computers may not have the timing accuracy required for 1200 bps transmission (0.01%), timing correction on the incoming data stream must be made. The async/sync converter accepts asynchronous serial data clocked at a rate between 1200 Hz + 1%, -2.5%. It outputs serial data at a fixed rate of 1200 Hz +/- 0.01% derived from the master clock oscillator. To compensate for the input and output rate differences, a stop bit is either deleted or inserted when necessary. If the input data rate is slower than the output data rate, a stop bit is inserted. If the input data rate is faster than the output data rate, a stop bit is deleted. The output of the async/sync converter is applied to the scrambler.

The scrambler is a 17 bit shift register clocked at 1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with the input data. The resultant data is supplied to the D input of the shift register. Outputs from the first two stages of the shift register form the dibit that is applied to the PSK modulator. The purpose of the scrambler is to randomize data so that the energy of the modulated carrier is spread over the band of interest -- either the high-band centered at 2400 Hz or the low-band, centered at 1200 Hz. A 1200 bps modem actually sends two bits at a time, called a dibit; dibits are sent at 600 baud, the actual rate of transmission; 600 baud is the optimum rate that can be transmitted over the general switched telephone network for a full duplex FDM (frequency division multiplexing) modem because band limit filters in the central office cut off at about 3000 Hz.

The dibit applied to the PSK modulator produces one of four differential phase shifts of the square wave carrier signal (1200 Hz or 2400 Hz) at the 600 Hz baud rate. The resultant waveform is passed through a wave shaping circuit that performs a raised cosine function (this is the shape factor called out in the CCITT V.22 spec, and it also meets the Bell 212A requirement for optimum transmission). The wave shaped signal is then passed through either the low-band or high-band filter depending upon originate or answer mode selection.

For low speed operation the FSK modulator is used. It produces one of four precision frequencies depending on originate or answer mode and the 1 (mark) or 0 (space) level of the transmit data. The frequencies are produced from the master clock oscillator using programmable dividers. The dividers respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence. The output of the FSK modulator is applied to the appropriate filter when the low speed mode of the operation is selected.

The filter section consists of low-band (1200 Hz) and high-band (2400 Hz) filters, half-channel compromise amplitude and group delay equalizers for both bands, smoothing filters for both bands and multiplexers for routing of the transmit and receive signals through the appropriate band filters . For CCITT V.22 applications, a notch filter is included that can be programmed for either 550 Hz or 1800 Hz. In the call progress monitor mode, the low-band filter is scaled down by a factor of 2.5 to center it over a frequency range of 300 to 660 Hz. Thus, during call establishment in the originate mode, call progress tones can be monitored through the scaled low-band filter and the modem answer tone or voice can be monitored through the unscaled high-band filter.

The low-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 1200 Hz. In the originate mode, this filter is used in the transmit direction; in the answer mode it is used in the receive direction. When analog loopback is used in the originate mode, this filter, together with the low-band delay equalizer, is in the test loop. In the Call Progress Monitoring mode the filter response is scaled down by 2.5, moving the center frequency to 480 Hz.

The low-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the low-band filter and half of the compromise line characteristics,

producing a flat delay response within the pass-band.

The high-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 2400 Hz. In the answer mode, this filter is used in the transmit direction; in the originate mode, it is used in the receive direction. When analog loopback is used in the answer mode, this filter, together with the high-band delay equalizer, will be in the test loop.

The high-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the high-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band. The transmit smoothing filter is a second order low-pass switched-capacitor filter that adds the modem transmit signal to the DTMF or V.22 guard tones. It also provides a 3dB per step programmable gain function to set the output level.

RECEIVER

The receiver section consists of an energy detector, AGC, PSK demodulator, FSK demodulator, descrambler, and sync/async converter.

The received signal is routed through the appropriate band-pass filter and applied to both the energy detector and AGC circuit. The energy detector is based on a peak detection algorithm. It provides a detection within 17 to 24 ms. It is set to turn on when the signal exceeds -43 dBm and turn off when the signal falls below -48 dBm. A 2 dB minimum hysteresis is provided between the turn on and turn off levels.

The AGC circuit is a programmable gain amplifier that covers a range of 28 dB in seven steps. The gain is controlled by a 3 bit up/down counter. Output of the AGC amplifier is rectified and compared with two preset levels corresponding to desired high and low limits. Outputs of the comparators control the up/down counter such that the received signal is amplified to the desired level.

The PSK demodulator uses a coherent demodulation technique. Output of the AGC amplifier is applied to a dual phase splitter that produces an in-phase and 90 degree out of phase component. These components are then demodulated to baseband in a mixer stage where individual components are multiplied by the recovered carrier. The baseband components are low-pass filtered to produce I and Q channel outputs. (In-phase and Quadrature). The I and Q channel outputs are rectified, summed, and passed through a band-pass filter giving a 600 Hz signal. This signal is applied to a digital phase lock loop (DPLL) to produce a baud rate clock. Using the recovered clock signal, the I and Q channels are sampled to produce the received dibit data. The recovered carrier for the demodulator is generated by another PLL which is controlled by the amplitude of the error signal formed by the difference of the I and Q outputs.

The descrambler is similar to the scrambler. The received dibit data is applied to the D input of a 17 bit shift register clocked at 1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with input data to produce received data.

In the asynchronous mode, data from the descrambler is applied to the sync/async converter to reconstruct the originally transmitted asynchronous data. For data which had stop bits deleted at the transmitter (overspeed data), these stop bits are reinserted. Underspeed data is passed essentially unchanged. Output of the sync/async converter along with the output of the FSK demodulator is applied to a multiplexer. The multiplexer selects the appropriate output, depending on the operating speed, and outputs received data on the RXD pin.

For low speed operation, the FSK demodulator is used. The output of the AGC amplifier is passed through a zero crossing detector and applied to a counter that is reset on zero crossings. The counter is designed to cycle at a rate four times faster than the carrier signal. The counter output is low-pass filtered and hard limited to generate FSK data.

HYBIRD

The signal on the phone line is the sum of the transmit and receive signals. The hybrid subtracts the transmitted signal from the signal on the line to form the received signal. It is important to match the hybrid impedance as closely as possible to the telephone line to produce only the received signal. This matching provided by an external resistor connected between the RXA1 and RXA2 pins on the VL7C212A. The filter section provides sufficient attenuation of the out of band signals to eliminate leftover transmit signals from the received signal. The hybrid also acts as a first order low-pass antialiasing filter.

TONE GENERATOR

The tone generator section consists of a DTMF generator and a V.22 guard tone generator. The DTMF generator produces all of the tones corresponding to digits 0 through 9 and * and # keys. The V.22 guard tone generator produces either 550 Hz or 1800 Hz. Selection of either the 550 Hz or 1800 Hz tone will cascade the corresponding notch filter with the low-band filter. The tones are selected by applying appropriate codes through the Data I/O pin. Before a tone can be generated, tone mode must be selected. Facility is also provided to generate single tones corresponding to the individual rows or column of the DTMF signal.

AUDIO OUTPUT STAGE

A programmable attenuator that can drive a load impedance of 50 K ohms is provided to allow monitoring of the received line signal through an external speaker. The attenuator is connected to the output of the hybrid. Four levels of attenuation -- no attenuation, 6 dB attenuation, 12 dB attenuation and squelch are provided through the ALC1, ALC0 and audio output level control codes. Output of the attenuator is available on the audio output pin where an external audio amplifier (LM386 type) can be connected to drive a low impedance speaker. The output can directly drive a high impedance transducer, but the volume level will be low.

Functional Description:

VL7C213 & VL7C214 Controllers

The VL7C213 modem controller, implemented in VTI's two micron CMOS process, was designed specifically to handle all of the modem control functions, as well as the interface to a system bus. Besides including an 8-bit microprocessor, 8K by 8 bytes of ROM, and 128 by 8 bytes of RAM, it also contains the functionality of a VL82C50 UART, greatly simplifying the interface to a parallel system bus, such as the one used in IBM's PC. In fact, a

complete, Hayes compatible modem for the PC consists of the VL7C213 controller, the VL7C212A modem and the DAA. All of the popular communications software written for the PC will work with the VL7C212A/ VL7C213 set.

Another version of the controller, the VL7C214, is intended for RS-232 applications. It contains the same processor, memory, and UART as the VL7C213 and has the same interface to the modem chip. The difference is that the UART is turned around so that serial data from the RS-232 port is converted to parallel data handled by the internal processor. Pins are provided for connecting the familiar switches and indicator lamps found on most stand-alone modems, although the switches and lamps are not needed for operation -- all of the switch settings can be done through software.

The VL7C214 provides a standard five volt logic level interface -- RS-232 drivers are required to interface to the port. Like the VL7C213, the VL7C214 comes preprogrammed with the Hayes "AT" command set, and when used with the VL7C212A modem, emulates a Hayes-type stand-alone modem. The VL7C213 and VL7C212A emulate a Hayes-type IBM PC plug-in card modem.

But the chip set is by no means limited to implementing a Hayes-type smart modem. VTI is in the custom IC business and both chips were designed with this in mind. For example, only about 6K bytes of the VL7C213's ROM is used for the handshaking and smart modem code, leaving 2K bytes for additional features that a customer may specify. And since the controller is ROM programmable, any command set, not just the Hayes "AT" set, can be implemented.

Both the VL7C213 and VL7C214 require plus five volts and are available in either a 28 pin DIP or a 28 lead plastic chip carrier with "J" leads for surface mount applications. Besides the four-line interface for the VL7C212A modem, the VL7C213 controller has an 8-bit data port, three address lines, a chip select input, an interrupt line, and the DOST and DIST control lines found in the 8250B UART. It also has control lines for ring indication, the off-hook relay and a data/voice relay; these three lines connect to the DAA.

In the VL7C214, the 8-bit port becomes the switch input lines and the address, chip select, DIST and DOST lines become the six lines for the RS-232 interface. These six lines are also used to drive the LEDs. Internally, all of these lines are treated as programmable I/O ports under software control -- so the main difference between the VL7C213 and VL7C214 is the ROM code. It also contains the same modem and DAA interface lines as the VL7C213.

The VL7C213 and VL7C214 are truly ASIC controllers -- they are designed to control a modem or other peripheral that operates at a moderately slow data rate up to 1200 bits per second. What's unique about the VL7C213, for example is that it allows a slow peripheral to interface to a high speed bus, without making the main processor slow down.

This is done through the UART interface and the on-chip registers which look somewhat like dual port registers. The main processor can write to and read from them at will, while the on-chip controller can do the same. The controller was designed this way because most communications software has to have unrestrained access to the UART registers. To make the VL7C213 compatible with this software, the registers were included.

The internal processor monitors the registers to determine the mode of operation -- command mode or data mode; at power-up it is automatically put in the command mode and it looks for instructions. Once carrier is detected, it goes into the data mode, and stays there until escape sequence is three + signs -- +++ -- in the default mode, but it can be changed in software.

The actual processor contains an 8-bit data path and can execute 19 instructions with five different addressing modes: direct, indirect, immediate, register direct, and register indirect. There is 8K by 8 of ROM on-chip for program storage.

To the system bus, the VL7C213 looks and acts just like a VL82C50 UART. All of the communications software written for this UART will work with the VL7C213 and VL7C214. The VTI chip set is truly a Hayes-type modem in two chips.

THE VL7C212A & VL7C213/VL7C214 SYSTEM

The only external components required by the VL7C212A are the 600 ohm line matching resistor, a 7.3728 MHz crystal -- a standard frequency -- and a 20 pf capacitor from each leg of the crystal to ground. That's all! If it is desired to drive a speaker to monitor the line, an amplifier like the LM386 can be added, but the output provided on the VL7C212A can directly drive a high impedance (50 K ohm) earphone-type transducer.

The VL7C213 modem controller's clock in line is driven by the VL7C212A's clock out line, so only one crystal is needed. The VL7C213 interfaces directly to an IBM PC bus -- no buffers are required. The only external parts may be an eight input NAND gate for COM1 and COM2 decoding inside the PC.

For tone dialing, the controller sends a code to the modem chip which in turns puts out the called for DTMF tone on the line via the on-chip DTMF generator. For pulse dialing, the controller pulses the OH (off-hook) relay. Both dialing modes work with the built-in call progress algorithm so they won't start dialing until a dial tone is detected.

All modems require a DAA. A DAA or data access arrangement is a piece of equipment required by the FCC to connect anything to the general switched telephone network. It consists of an isolation transformer, typically 600 ohms to 600 ohms; a relay for disconnecting the modem from the line; a ring detector, typically an opto-isolator; and high voltage surge protectors. The DAA has to be FCC registered and this can be done by any of many consultants and labs around the country. The fee is typically $2,000 and it takes several months. Another alternative is to buy a DAA, supplied by several manufacturers.

212A is a Bell specification that calls for 1200 bit per second, full or half duplex data transmission with a fallback mode of 300 baud (Bell 103). It is not 1200 baud; the spec calls for transmission of dibits -- 2 bits per baud so the 1200 bps transmission takes place at 600 baud. The same is true for V.22 -- it's 1200 bps or 600 baud. V.22 does not call for a 300 baud fallback; there is a CCITT standard for 300 and that's V.21. It is

not a required fallback for V.22 and it is not included in the VL7C212A.

V.22 also calls for guard tones to be sent along with the data. In most of Europe the tone is 1800 Hz except in Sweden where 550 Hz is used. The VL7C212A modem has the 550 Hz and 1800 Hz tone generators built in as well as the 550 and 1800 Hz notch filter to remove the guard tone when in the receive mode.

All modems require a hybrid. Hybrid is a term used to describe a circuit, passive or active, that takes the separate transmit and receive signals and combines them to go over the phone line. In the VL7C212A, this is done with op amps, but the separate signals - - TXout and RXA2 -- are also brought out so an external hybrid can be used, if desired. The combined signal comes out on the RXA1 pin and a matching resistor -- typically 600 ohms -- is connected between RXA1 and RXA2.

PIN/FUNCTION DESCRIPTIONS

14	**TXD**	Transmit data. Data on this input is modulated by the modem and output on TXout pin. A logic low is space and a logic high is mark.
13	**RXD**	Receive data. The modem demodulates the received carrier and outputs data on this pin. A logic low level is space and a logic high level is mark. The controller can force the demodulator output to the mark state by sending the code 02.
15	**D I/O**	Data I/O pin. Data is shifted in serially when WR is low on rising edges of SCK clock. Data is transferred to a latch when WR goes high. Up to seven data bits can be sent. Input codes are defined in table 1. Data is read from the modem serially when RD is low, on rising edges of SCK clock. Up to four data bits can be read. Output codes are defined in table 1.
18	**$\overline{WR}$**	Strobe output from the controller for shifting data to the modem.
17	**$\overline{RD}$**	Strobe output from the controller for serially reading data from the modem.
16	**SCK**	Serial shift clock is applied to this pin. It is normally high until data is sent to, or read from, the modem.
11	**TXout**	Transmit data carrier output.
9 10	**RXA1** **RXA2**	Received data carriers.
7	**Audio Out**	Output of the hybrid is passed through a programmable attenuator and brought out on this pin. Four levels of received signal can be programmed using the control codes listed in Table 1.
20 21	**XTAL1** **XTAL**	Pins for connecting a 7.3728 MHz crystal. An external clock signal can be applied to the XTAL1 pin.
23	**CKOUT**	Buffered crystal oscillator signal is output on this pin. It can drive one LS TTL load.
2	**TXCKO**	Transmitter clock output. In high speed, synchronous, internal mode, this output supplies a 1200 Hz clock to the DTE.
3	**TXCK1**	In high speed, synchronous external mode this pin is an input for receiving a 1200 Hz clock from the DTE.
6	**RXCK**	Receiver clock output. In high speed, synchronous, external mode, the modem supplies a 1200 Hz clock on this output.
24	**VCC**	+ 5V power supply.
12	**VSS**	- 5V power supply.
22	**DGND**	Digital ground.
1	**AGND**	Analog ground.
4 5	**TEST1** **TEST2**	Used by VTI for testing. Make no connection to these pins -- they must be left floating.
8 19	**NC** **NC**	No connect. No internal connection is made to these pins and they may be left floating.

TABLE 1. DEFINITION OF I/O CODES

1. Instructions to the modem IC

Data on the D I/O pin is shifted into the modem when WR is low, on rising edges of the SCK clock. Data is transferred into a latch when WR goes high. (See Figure 2 for write cycle waveforms.) Up to seven data bits (D0--D6) can be sent to the device. These bits control the operating modes of the modem as show below:

D6	D5	D4	D3--D0	Mode/Function
				Non Tone Mode:
0	1/0	0	0	Reset (set default values)
0	1/0	0	1	Tone On/Off
0	1/0	0	2	Force Receive Data to Mark Off/On
0	1/0	0	3	TLC0 Transmit Level Control Bit 0 (default 0)
0	1/0	0	4	TLC1 Transmit Level Control Bit 1 (default 0)
0	1/0	0	5	TX Transmitter On/Off
0	1/0	0	6	ALB Analog Loopback On/Off
0	1/0	0	7	CPM Call Progress Monitor Mode On/Off
0	1/0	0	8	Connection Indicator (CI) On/Off
0	1/0	0	9	ALCO Audio Output Level Control Bit 0 (default 0)
0	1/0	0	A	ALC1 Audio Output Level Control Bit 1 (default 0)
0	1/0	0	B	WLS0 Word Length Select 0 (default 0)
0	1/0	0	C	WLS1 Word Length Select 1 (default 1)
0	1/0	0	D	Sync/Async
0	1/0	0	E	LS/HS: Low Speed/High Speed
0	1/0	0	F	A/0: Answer/Originate
0	1/0	1	0	Transmit Mark On/Off
0	1/0	1	1	Transmit Space On/Off
0	1/0	1	2	Scrambler Disable On/Off
0	1/0	1	3	DLB Digital Loopback On/Off
0	1/0	1	4	TXDP Transmit Dotting Pattern On/Off
0	1/0	1	5	Locked/Internal
0	1/0	1	6	External/Slave
0	1/0	1	7	V.22 2100 Hz Tone On/Off. Must select low speed of mode for operation
				Tone Mode:
1	1/0	0	0	Dial 0
1	1/0	0	1	Dial 1
1	1/0	0	2	Dial 2
1	1/0	0	3	Dial 3
1	1/0	0	4	Dial 4
1	1/0	0	5	Dial 5
1	1/0	0	6	Dial 6
1	1/0	0	7	Dial 7
1	1/0	0	8	Dial 8
1	1/0	0	9	Dial 9
1	1/0	0	A	Dial *
1	1/0	0	B	Dial #
1	1/0	0	C	Output 550 Hz and Insert 550 Hz Notch in Low-Band Filter
1	1/0	0	D	Output 1800 Hz and Insert 1800 Hz Notch inLow-Band Filter
1	1/0	0	E	Row Disable On/Off
1	1/0	0	F	Column Disable On/Off

TABLE 1. DEFINITION OF I/O CODES (continued)

WLS1	WLS0		Word Length
	0		8 Bits
0	1	9 Bits	
	0	10 Bits	(default)
	1	11 Bits	

TLC1	TLC0	Transmitter Output Level (dBm) at the Phone Line
	0	-12 (default)
	1	-
	0	-
	1	

ALC1	ALC0	Audio Output Level
	0	Output Off (default)
	1	12 dB Attenuation
	0	6 dB Attenuation
	1	No Attenuation

2. Information from the Modem IC

Data is read serially from the modem when RD is low, on rising edges of the SCK clock. (See Figure 1 for read cycle waveforms.) Up to four data bits (D0--D3) can be read as defined below:

D0	Energy Detect	0 - No Energy 1 - Energy Present

In the CPM mode, the energy detector is connected to the output of the high band filter, if ALB is off, or the scaled low-band filter, if ALB is on.

D1	Received Data (FSK)	1 - Mark 0 - Space
D2	Received Data (PSK)	1 - Mark 0 - Space
D3	Unscrambled Mark	1 - Detected 0 - Not Detected

Notes:
1) Default values for the operating modes on power up are those shown to the right of the "/" unless otherwise specified.

2) Data is shifted in and out of the modem with LSB first.

VL80C75 PRODUCT BRIEF

T1 INTERFACE

FEATURES

- Supports T1, T1C and CEPT data rates
- AMI, B8ZS, HDB3 coding
- Full implementation of CCITT recommendations G.703, G.732, G.733 & Bell Technical Advisories on clear channel and extended framing format
- Compatible with:
  - MTEL TDMA 10xx
  - SDSI
  - LITEL TAS
  - T1 Video Teleconference Equipment
- On-chip voltage comparators and AGC
- Input frequency memory
- Jitter smoothing FIFO
- Loop control feedback
- Error detection & flagging
- Self test provision
- Microprocessor compatible interface
- Low power CMOS technology

DESCRIPTION

The VL80C75 is a general purpose PCM Line Interface circuit. It is designed to support the bipolar interface of T1 (1.544 Mbps), T1C (3.152M bps), or CEPT (2.048 Mbps) specifications. It is capable of sending (coding) and receiving (decoding) AMI, B8ZS or HDB3 data formats with appropriate error correction.

The incorporation of on-chip voltage reference levels and comparators, allow the device decoder section to accept incoming ternary/bipolar data directly. Sensitivity is optimized by monitoring the level and waveform of the incoming bipolar signal.

An injection locking divider permits clock recovery from the incoming serial data stream. A 32-bit long FIFO (elastic buffer) may be used in either the decoder or the encoder path to smooth clock jitter. Status information is provided to facilitate the control of an external VCO.

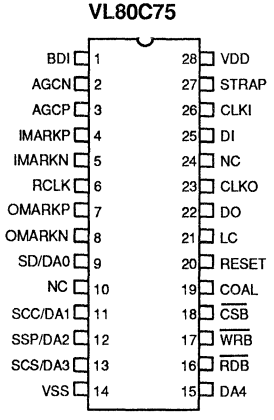
The VL80C75 will indicate the presence of bipolar violation in the input data as well as a FIFO underflow/overflow.

Interfacing to the external bipolar line output circuits is facilitated by the provision of 50% duty cycle drive pulses. The system interface is microprocessor compatible. The T1 Interface internal registers may be accessed by either a serial or parallel interface.

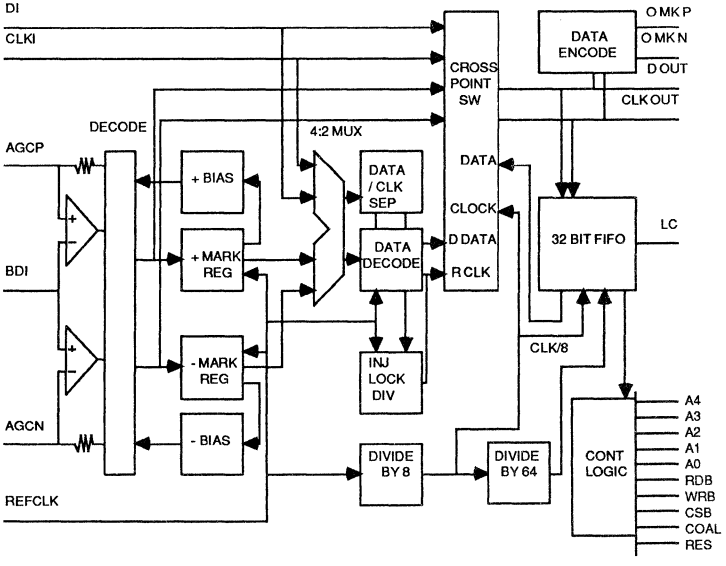
System test is assisted by the provision of a loopback feature which operates in both directions.

The VL80C75 is fabricated in a double metal, n well, 2 micron silicon gate CMOS process and is housed in a 28 pin DIP or ceramic package.

PIN DIAGRAM



BLOCK DIAGRAM



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NEW JERSEY
Fairfield, 201-575-5300
Marlton, 609-596-8000

NEW MEXICO
Albuquerque, 505-243-4566

NEW YORK
Long Island, 516-231-1000
Rochester, 716-427-0300
Syracuse, 315-652-1000

NORTH CAROLINA
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Winston-Salem, 919-725-8711

OHIO
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Columbus, 614-885-8362
Dayton, 513-435-5563

OKLAHOMA
Tulsa, 918-665-7700

OREGON
Portland, 503-684-1690

PENNSYLVANIA
Philadelphia, 215-928-1800
Pittsburgh, 412-856-7000

RHODE ISLAND
East Providence, 401-431-0980

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Austin, 512-835-4180
Dallas, 214-380-6464
Houston, 713-530-4700

UTAH
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WISCONSIN
Milwaukee, 414-792-0150

PUERTO RICO
San Juan, 809-723-6500

CANADA
Montreal, 514-735-5511
Ottawa, 613-226-6903
Quebec City, 418-687-4231
Toronto, 416-661-0220

VLSI TECHNOLOGY, INC.

VLSI Technology, Inc.
Application Specific
Logic Products Division
10220 South 51st Street
Phoenix, AZ 85044
602-893-8574/VLSI

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