WD90C26A

Integrated Low Power VGA LCD

Controller with Simultaneous Display

WESTERN DIGITAL

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1.0 INTRODUCTION

This section introduces and describes the Western Digital® WD90C26A Integrated Low Power VGA LCD Controller with Simultaneous Display (hereinafter referred to as WD90C26A or WD90C26A controller). The introduction is divided into the following subsections:

- Purpose
- WD90C26A Features
- General Description

1.1 PURPOSE

The WD90C26A controller provides control of all flat-panel displays along with simultaneous display on a traditional CRT. The WD90C26A supports all current monochrome and color flat-panel technologies.

The WD90C26A has improved power management and a performance-scaling capabilities that make it an ideal video solution for low battery drain portable computer applications.

1.2 WD90C26A FEATURES

- Supports VGA flat panel or CRT video displays or both simultaneously
- Fully supports LCD, plasma, and Electro-Luminescent (EL) flat-panel technologies.
- Operates on standard 5 VDC, low power 3.3 VDC, or a mix of both
- Provides 256K colors on 8-bit or 16-bit STN LCD panels (with WD90C55), 180K colors on 9-bit TFT color LCD panels and 226K on 12-bit TFT color LCD panels
- Compatible with WD90C55 color STN LCD interface
- True 64-gray scale with programmable gray shade mapping including in 640 x 480 x 256 color video modes
- Up to 45 Mhz maximum video clock rate on flat panel display when using 5 VDC operating voltage, or 36 MHz when using 3.3 VDC operating voltage.
- Up to 65 Mhz maximum video clock rate on CRT display when using 5 VDC operating voltage, or 55 MHz when using 3.3 VDC operating voltage.
- Supports 800 x 600 x 256 and 1024 x 768 x 16 non-interlaced modes on CRT display
- Simultaneous display with all types of flat panels (patent pending)
- Up to 36 Mhz maximum video clock rate in dual-panel simultaneous display mode.
- Full downward compatibility with CGA, MDA, and Hercules graphics standards
- Hardware vertical expansion and auto-centering in both simultaneous and single display mode.
- Up to 16 loadable fonts
- Hidden register support for 100% hardware compatibility with IBM's VGA standards
- On-board VGA compatible RAMDAC with internal CRT detection circuit
- On-chip 8 or 16-bit ISA Bus (AT bus) interface
- On-chip 16-bit MicroChannel interface
- On-chip 386SL PI Bus Interface
- True 16-bit CPU to display memory data transfer in all video modes
- Flexible display memory configuration (4 or 5 256Kx4 DRAMs, one 256Kx16 DRAM, or one 256Kx16 DRAM and one 256Kx4 DRAM)
- Up to 44.3 Mhz maximum memory clock rate when using 5 VDC operating voltage, or 40 MHz when using 3.3 VDC or mixed operating voltage.
- Selectable 8- or 16-bit I/O and memory interface
- Zero wait-state performance
- Adjustable video FIFO depth and fast page mode memory timing
- System interface write buffering
- Typical power dissipation of 660 mW at 5 VDC, or 330 mW at 3.3 VDC or mixed operation voltage
- Enhanced power down modes
- I/O mapping to improve board level testability
- 144-pin MQFP package
- Supports ISO CRT display
- Supports 8-bit video BIOS
- Virtual memory/linear addressing support

1.3 GENERAL DESCRIPTION

The WD90C26A is a 0.9 micron CMOS VGA controller designed to simultaneously drive a flat-panel display and the traditional analog CRT with a minimum of external components. The only additional components required for a complete flat-panel VGA subsystem are 2 to 5 DRAMs and video/memory clock sources. Contained on-chip are a flat-panel interface and a RAMDAC. The full-featured flat-panel interface is capable of supporting LCD, plasma, and EL flat-panel technologies. The full-featured RAMDAC is capable of directly driving PS/2 style analog color or monochrome monitors.

The WD90C26A's scalable architecture allows it to be used with either 2 to 5 external 256Kx4 DRAMs, one 256Kx16 DRAM or one 256Kx16 DRAM and one 256Kx4 DRAM. Basic VGA performance is available with the minimum configuration of two 256Kx4 DRAMs or one 256Kx16 DRAM. Added panel support and enhanced VGA modes are available using 3 or 4 256Kx4 DRAMs. Sixteen-bit video memory performance is also available using the four 256Kx4 or one 256Kx16 DRAM configuration. DRAM use is firmware controllable, allowing the decrease of DRAM power consumption or the increase of system performance.

Western Digital's superior orthogonal 64-gray scale to 64-gray shade mapping technology allows system developers to 'hand tune' each of the shades in the 64-gray scale to provide the most realistic and visually linear gray scale shading for a particular model of panel. This is achieved through use of a system programmable on-chip 64-word gray scale lookup table or mapping RAM.

As with all Western Digital VGA controllers, the WD90C26A is fully compatible with IBM VGA, CGA, MDA, and Hercules video standards.

Through the use of its hidden, or "shadow" registers, the WD90C26A can be programmed to support various video modes and standards using fixed resolution flat-panel screen sizes, yet appear to the system as capable of displaying the variety of screen sizes and resolutions available with analog monitors. System modification of register content, thus shadowed or hidden, does not destroy the WD90C26A controller's ability to display the desired information on a flat-panel display as well.

The WD90C26A controller's vertical expansion and auto-centering features provide full-screen or center screen flat-panel displays even in video modes with lower resolutions than those of the panel. A unique expansion algorithm provides for realistic appearance of both text and graphics on expanded displays, without requiring the use of special expanded display fonts.

Advanced power management features include:

- Separate supply pins for certain functions so that parts of the chip may be externally powered off
- The capability to slow down internal clocks to conserve power
- Power sequencing that can be used to control power supply and interface signals to prevent panel burnout

Also included in the WD90C26A is an advanced TFT support circuit that allows display from a palette of 180K colors on 9-bit interface color panels.

The WD90C26A directly supports TFT LCD displays with 12-bit interfaces by using undithered 12-bit direct colors from a 226K palette for optimum 12-bit display performance.

2.0 ARCHITECTURE

This section describes the architecture of the WD90C26A. A block diagram of the architecture is shown in Figure 2-1. The components described are:

- System Interface Logic
- CRT Controller
- Video Sequencer
- Video Graphics Controller
- Video Attribute Controller
- RAMDAC
- Flat Panel Adapter
- Display Memory Interface
- Power-Down Control

2.1 SYSTEM INTERFACE LOGIC

The WD90C26A includes a host system interface for direct connection to an Industry Standard Architecture (ISA) bus, IBM compatible MicroChannel (MC) bus, or 386SL Peripheral Interface (PI) bus. The interface allows the following features:

- Full 16-bit I/O and memory cycles
- Zero wait-state performance capability
- 16-bit to 8-bit memory data path conversion
- Full decoding of 16 MBytes of memory space for mapping of video memory, without requiring external decode logic
- Internal buffering of system operations to speed performance
- External video BIOS ROM

2.2 CRT CONTROLLER

A VGA-compatible CRT controller includes the following functions:

- Generates video buffer addresses for screen refresh operations
- Generates monitor synchronization signals
- Controls an alpha-numeric cursor
- May be set with remapped register locations to operate as a CGA, MDA, or Hercules CRT controller
- Register shadowing

2.3 VIDEO SEQUENCER

The VGA compatible video sequencer is the central timing and memory control section of the WD90C26A. Its functions include the following:

- Generation of memory handshake signals
- Control of CRT controller timings
- Provision of general interface timing and control signals to the balance of the WD90C26A

2.4 VIDEO GRAPHICS CONTROLLER

The VGA video graphics controller performs VGA graphics operations on video data such as AND, OR, XOR, rotate, and color comparison functions.

2.5 VIDEO ATTRIBUTE CONTROLLER

The WD90C26A controller's video attributes are added to display data by the Video Attribute Controller. Data added includes:

- Standard text attributes
- VGA graphics mode attributes
- Cursor display
- Screen border color

The Video Attribute Controller also performs data conversion from modes like packed pixel, planar, or text mode into video data to be presented to the RAMDAC.

2.6 RAMDAC

Integrated into the WD90C26A is a fully VGA-compatible high-speed 6-bit RAMDAC. This RAMDAC directly drives VGA and super-VGA color or monochrome analog monitors.

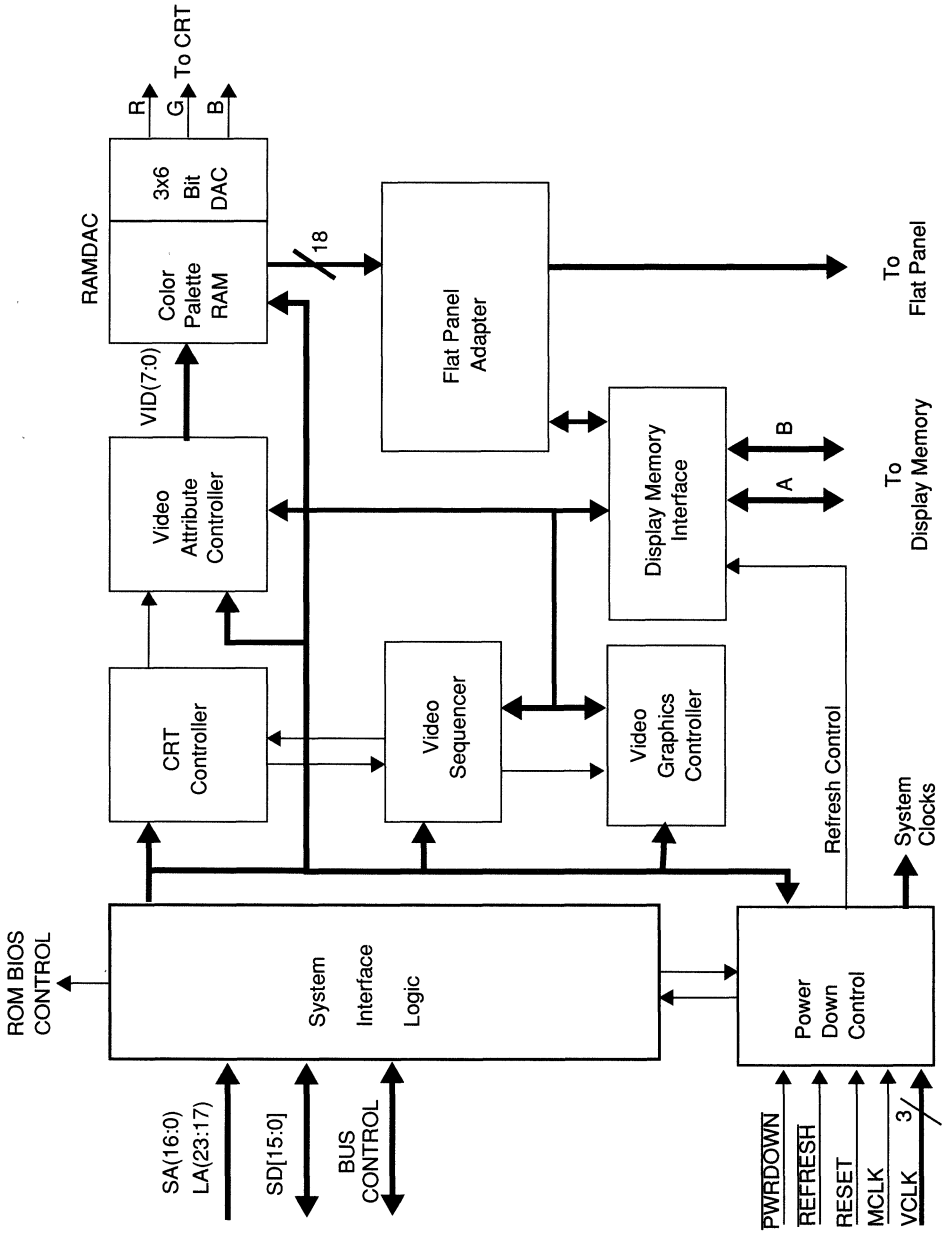

FIGURE 2-1 WD90C26A BLOCK DIAGRAM

2.7 FLAT-PANEL ADAPTER

The flat-panel adapter takes video information from the WD90C26A controller's internal RAM-DAC color palette RAM and converts it into the format appropriate for the type of panel to be attached.

The following functions occur in the flat-panel adapter:

- "Digital DAC" color to monochrome gray scale conversion
- Gray scale mapping
- Gray shade dithering
- Color STN LCD panel dithering circuitry
- Color TFT LCD panel dithering
- Direct 12-bit panel support
- Plasma panel support
- Row buffering
- Frame buffering
- Panel format conversion

These functions are shown in Figure 2-2.

2.7.1 Color to Gray Scale Conversion

For monochrome flat-panel display of what normally would be a color analog video output, a digital equivalent of the RAMDAC function is required to sum color information together into video signals. This function is accomplished through use of a digital equivalent of the DAC function, which takes the RGB color palette RAM outputs and converts them to their digitally weighted monochrome equivalent. Weighting is performed using NTSC standard algorithms. Color to gray scale conversion can be disabled for Monochrome Display Adapter emulation applications.

2.7.2 Gray Scale Mapping

The WD90C26A controller's flat-panel adapter circuits incorporate an orthogonal 64-word x 6 bit gray-scale to gray-shade mapping RAM. This mapping RAM serves as a firmware-programmable lookup table that can be configured to map gray scale values from color-to-gray scale conversion into the dithered gray-scale shades best suited to a particular panel model.

Maximum flexibility in 'tuning' the WD90C26A to work with the characteristics of a particular panel is possible via this mapping RAM. Its size also allows finer control when selecting dithering patterns from the 64-shade monochrome dithering circuit, allowing any monochrome panel to perform to its best in displaying visually accurate gray scales.

Western Digital utility programs are available for the WD90C26A that can simplify the task of selecting mapping RAM programming values for a panel type (refer to Appendix B). Gray scale mapping may be bypassed for 1:1 gray scale to gray shade mapping.

2.7.3 Gray Shade Dithering

Monochrome gray shade dithering circuit provides a total of 64 shades of gray on monochrome flat-panel displays. All 64 shades can be simultaneously displayed. Simultaneous display of 64 shades in VGA modes is possible in 256 color video modes only.

2.7.4 Color STN Dithering

The WD90C26A dithering circuity supports color display from the full 256K VGA palette for dual-bit interface color STN panels.

2.7.5 Color TFT Panel Dithering Circuit

For 9-bit interface color TFT panels, the dithering circuit supports a total of 27K colors.

2.7.6 Direct 12-Bit TFT Panel Support

The WD90C26A drives 12-bit TFT panels with direct undithered color for a palette of 4K colors.

2.7.7 Plasma Panel Support

The WD90C26A drives plasma panels with undithered data direct from the outputs of the mapping RAM. Plasma panels are also "tunable" though the use of the mapping RAM for optimum use of their limited gray scale capability.

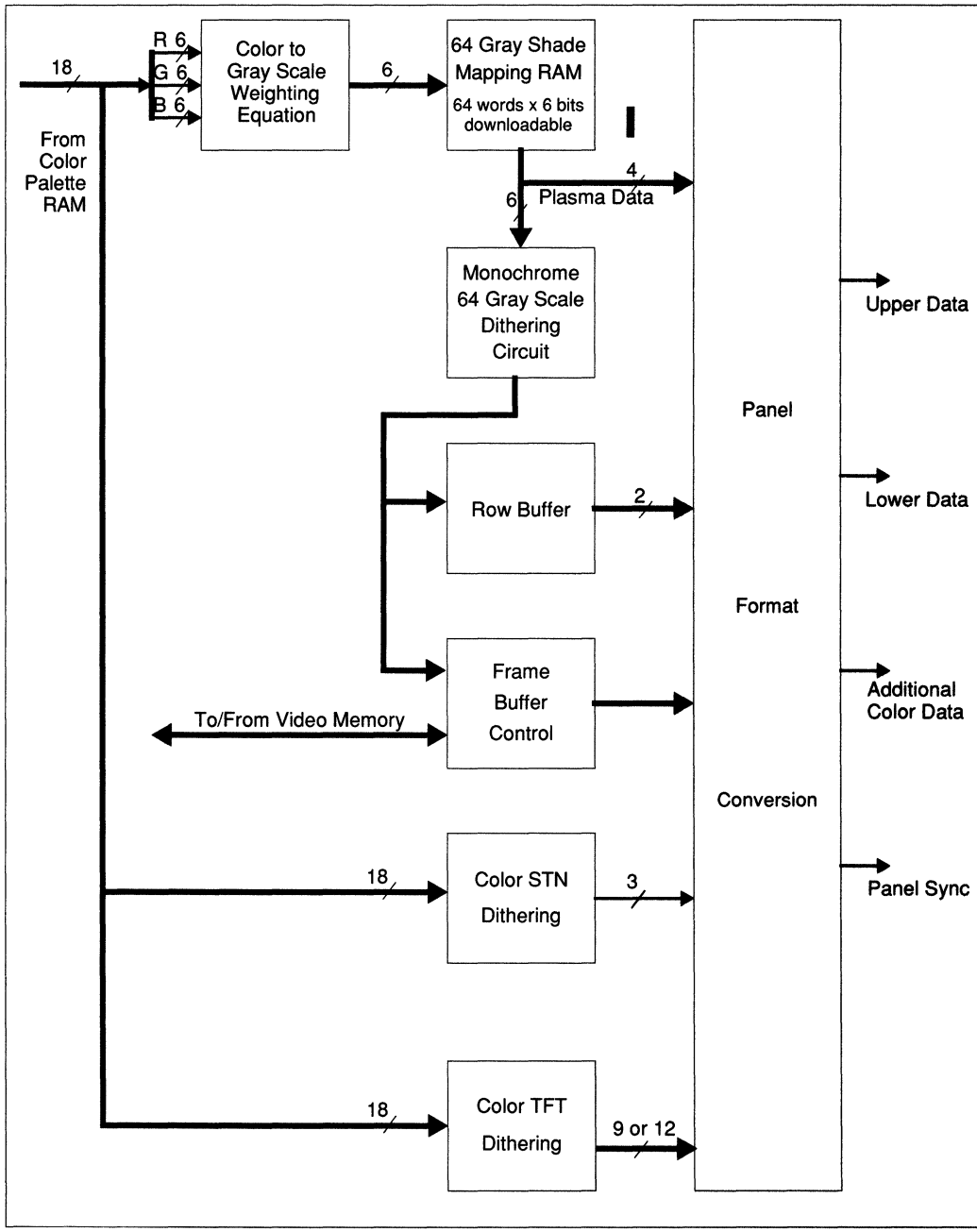

FIGURE 2-2 FLAT PANEL ADAPTER SECTION BLOCK DIAGRAM

2.7.8 Row Buffering

Monochrome dual-panel displays (most monochrome LCDs) are directly supported by the WD90C26A due to its capability to internally buffer alternating panel data without requiring external memory buffering.

2.7.9 Frame Buffering

The WD90C26A includes a frame buffering capability that allows simultaneous display on a CRT and on a dual-panel monochrome display. This function requires that a 256Kx4 DRAM be attached to the Bank B memory interface.

When simultaneous display is not required, the WD90C26A controller's internal row buffering provides all the required support for a dual-panel display.

2.7.10 Panel Format Conversion

The internal panel format conversion circuit provides the flexibility to reformat color or monochrome panel data into the particular pixel grouping required. The panel format conversion also includes the conversion circuits needed for the WD90C26A to drive the WD90C55 VGA Color LCD Interface.

2.8 DISPLAY MEMORY INTERFACE

The display memory interface that controls video-memory DRAM connects to video memory DRAM via two separate external memory buses. These buses allow accommodation of the changing needs of performance, feature support, and power conservation. Descriptions of these buses follow.

The Bank A bus is used to interface 8-bit video memory configurations, or as the lower byte interface for 16-bit video memory configurations.

The Bank B bus is used as the frame buffer interface when simultaneous display on a CRT and a dual-panel display is required.

When simultaneous display with a dual-panel display is not required, the Bank B bus is used to access the upper byte of 512 Kbyte of video memory organized as 256Kx16, or Bank B memory interface signals can be held static.

2.9 POWER-DOWN CONTROL

The WD90C26A controller's ability to control power consumption allows it to work successfully in portable applications. Power consumption is managed by the power-down control block, which performs the following functions:

- Turns off clocks to unused portions of the WD90C26A
- Provides refresh signals to video memory when normal refresh functions are shut down
- Controls wakeup/sleep cycling
- Reduces chip power during power-down mode
- Sequences chip reset operations

3.0 INTERFACES

3.1 INTRODUCTION

This section describes the following WD90C26A interfaces:

- System Interface - Allows the WD90C26A to directly interface to ISA bus-based systems, to MicroChannel bus-based systems, or to the 386SL Peripheral Interface bus.
- BIOS Support Interface - Allows the WD90C26A to provide an enable output for external video BIOS memory
- Video Memory Interface - Allows connection of either 2, 3, or 4 256K x 4 DRAMS or one 256Kx16 DRAM
- Video Interface - Allows direct connection to most PC-compatible CRTs and to a wide range of industry-standard flat-panel types
- Clock Interface - Controls clock oscillators or allows up to four separate frequency inputs

3.2 SYSTEM INTERFACE

The WD90C26A is designed to directly interface to ISA bus based or MicroChannel based systems, and also to the 386SL Peripheral Interface bus.

System interface selection is done by pulling high or low a video memory data line during device reset. Refer to the hardware configuration options in Section 6 for details on system interface bus selection.

3.2.1 Register Map

For both MicroChannel and ISA Bus operations, the WD90C26A is mapped into the system I/O address space as the standard set of VGA I/O registers.

Extended indexed "PR" registers at locations 3B5h/3D5h and 3C5h and 3CFh are used to control many features beyond those of standard VGA operation.

Refer to Section 5 for specific information about the use of each standard and PR register.

The WD90C26A has a 1-1/2 word write buffer which operates as a 2-cycle write buffer. This allows the WD90C26A to operate with a very high percentage of true zero wait state performance.

3.2.2 Power Conserving Bus Drivers

The WD90C26A is designed to be a portable computing device where driving a large capacitive bus, such as found in traditional PCs, is not a factor. To reduce power consumption, the WD90C26A controller's system interface has been designed to drive typical loads found in laptop applications where bus devices are fewer and closely grouped. For additional information on power consumption, refer to the Electrical Specifications in Section 9.

3.2.3 ISA Bus Interface Signals

The WD90C26A interfaces to an ISA bus at bus clock rates of up to 12.5 MHz. The WD90C26A supports full 16-bit memory and I/O transfers. Support of 16-bit memory transfers is independent of whether the WD90C26A has an 8-bit or 16-bit video memory path, although increased performance occurs when a 16-bit video memory is available.

The following ISA Bus signals are directly supported by the WD90C26A:

AEN	$\overline{\text{MEMR}}$
BALE	$\overline{\text{MEMW}}$
IOCHRDY	$\overline{\text{0WS}}$ (SRDY)
$\overline{\text{IOCS16}}$	$\overline{\text{REFRESH}}$
$\overline{\text{IOR}}$	RESET
$\overline{\text{IOW}}$	SA [16:0]
IRQ	$\overline{\text{SBHE}}$
LA[23:17]	SD[15:0]
$\overline{\text{MEMCS16}}$	

LA(23:17) addresses are latched internal to the WD90C26A by the BALE signal to eliminate bus timing problems in some common system implementations.

I/O and memory operation (8/16-bit I/0 and 8/16 bit memory) can be separately enabled by selectively enabling IOCS16 and MEMCS16 bus interface signals.

3.2.4 MicroChannel Interface Signals

The WD90C26A directly supports the following MicroChannel interface signals:

A[23:0]	MADE24
CDCHRDY	M/$\overline{IO}$
$\overline{CDDS16}$	$\overline{SBHE}$
$\overline{CDSETUP}$	$\overline{S0}$
$\overline{CDSFBK}$	$\overline{S1}$
CHRESET	$\overline{IRQ}$
$\overline{CMD}$	$\overline{REFRESH}$
D[15:0]	

In addition, the WD90C26A supports both an internal and external decode of I/O address 3C3 bit 0 as a video memory and I/O decode enable.

For full MicroChannel compatibility, only the lower 16 bits of system address bus are decoded for I/O accesses.

3.2.5 Peripheral Interface Bus Signals

The WD90C26A directly supports the following 386SL Peripheral Interface signals:

LA[23:17]	PW/$\overline{R}$
$\overline{PSTART}$	$\overline{SBHE}$
$\overline{PCMD}$	SA[19:0]
PRDY	SD[15:0]
PM/$\overline{IO}$	

3.3 BIOS SUPPORT INTERFACE

The WD90C26A can be configured to provide an enable output for an external 8-bit video BIOS PROM. The WD90C26A can be configured to automatically map this external BIOS in to the system memory map at time of reset, and then selectively map it in or out thereafter. Decodes are provided for the 32K of VGA video BIOS address space as defined in the VGA architecture. The WD90C26A also supports the ability to dynamically map out the highest 2K of the 32K VGA BIOS space.

Refer to *Using Features* in Section 6, for information on how to configure the WD90C26A for video BIOS support.

3.4 VIDEO MEMORY INTERFACE

The WD90C26A is designed to operate with 4 or 5 256Kx4 DRAMs, a single 256Kx16 DRAM, or a single 256Kx16 DRAM and 1 256Kx4 DRAM.

The video memory interface configuration is selected by pulling high or low on video memory data lines during device reset. Refer to the hardware configuration options in Section 6 for details on video memory interface configuration selection.

There are different performance options available for each configuration. The supported configurations are listed by number in Table 3-1.

DISPLAY MEMORY CONFIGURATION		PERFORMANCE	FIGURE REFERENCE
NO.	DRAMS		
1	4 256Kx4	• Use of 16-bit 256 Kbyte video RAM except when dual-panel multiplexed display and CRT are used simultaneously. • Supports 256 color mode on 640x400 and 640x480 resolution display. • Supports 12-bit TFT panel.	3-1
2	1 256Kx16	• Simultaneous display operation with all flat panel types except dual-panel LCDs • Supports 256 color mode on 640x400 and 640x480 resolution displays. • Supports 12-bit TFT panel.	3-2
3	5 256Kx4	• Use of 16-bit 256 Kbyte video RAM except when dual-panel multiplexed display and CRT are used simultaneously. • Supports 256 color mode on 640x400 and 640x480 resolution display. • Supports a separate 256Kx4 frame buffer.	3-3
4	1 256Kx16 and 1 256Kx4	• Simultaneous display operation with all flat panel types except dual-panel LCDs • Supports 256 color mode on 640x400 and 640x480 resolution displays. • Supports a separate 256Kx4 frame buffer.	3-4

NOTES:

1. Configuration No. 1 accommodates 2 and 3 256Kx4 DRAM interfaces with a correspondingly reduced performance.
2. To select the display memory configuration, refer to the hardware configuration options in Section 6.

TABLE 3-1 DISPLAY MEMORY INTERFACE CONFIGURATIONS AND REQUIRED DRAM

3.4.1 Display Memory Configuration No. 1 (Four 256Kx4 DRAMs)

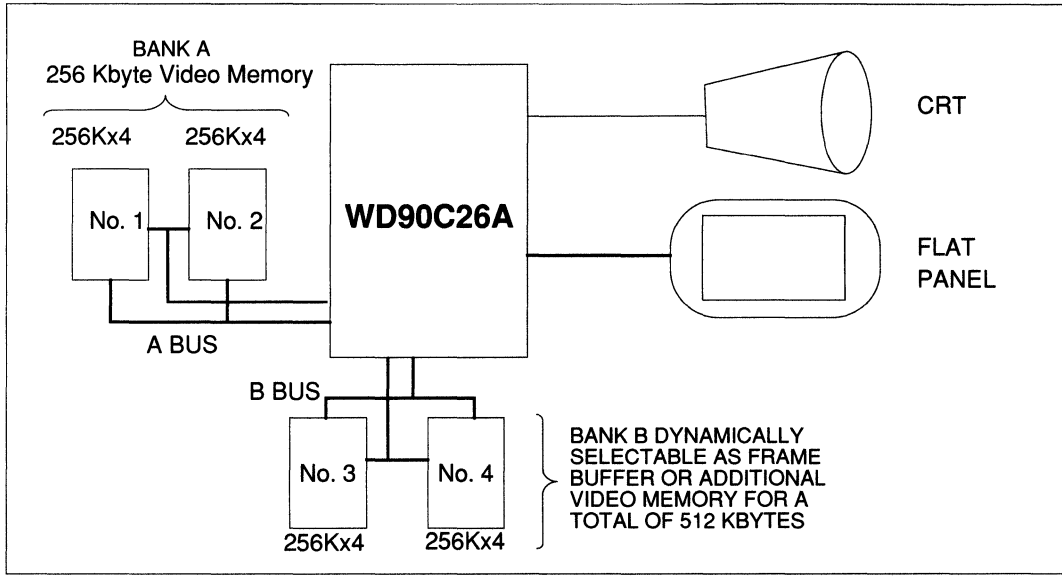

FIGURE 3-1 FOUR 256Kx 4 DRAM IMPLEMENTATION

The following features are supported when 4 256Kx4 DRAMs are used:

- The ability to use 512K video RAM except in those occasional times when a dual panel multiplexed display and a CRT are used simultaneously.
- Support of 640x400x256 and 640x480x256 color modes.
- Support for 12-bit TFT panel.

Bank B of DRAM can be disabled by firmware for power reduction, and DRAM #3 can be used alone for simultaneous display support of a dual panel display and CRT, while DRAM #4 is disabled.

3.4.2 Display Memory Configuration No. 2 (One 256Kx16 DRAM)

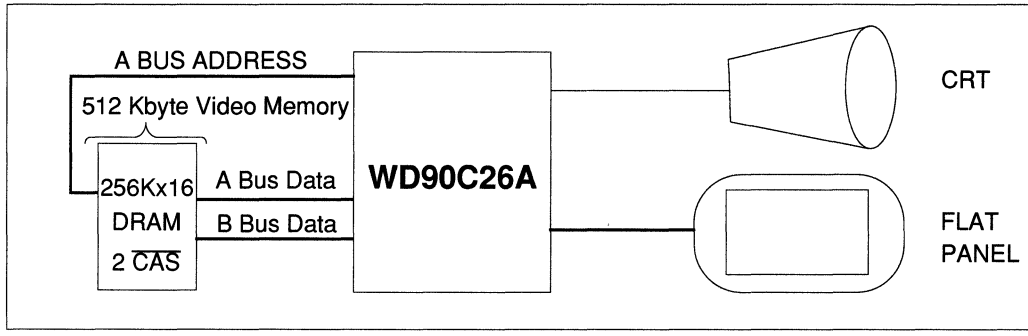

FIGURE 3-2 SINGLE 256K x 16 DRAM IMPLEMENTATION

The WD90C26A may be used with a single 2 $\overline{CAS}$ 256Kx16 DRAM, which provides 512 Kbytes of video memory and 16-bit memory performance. The following features are supported:

- Simultaneous display operation with all flat-panel types except dual-panel LCDs is allowed
- support of 640x400x256 and 640x480x256 color modes
- Support for 12-bit TFT panel.

3.4.3 Display Memory Configuration No. 3 (Five 256Kx4 DRAMs)

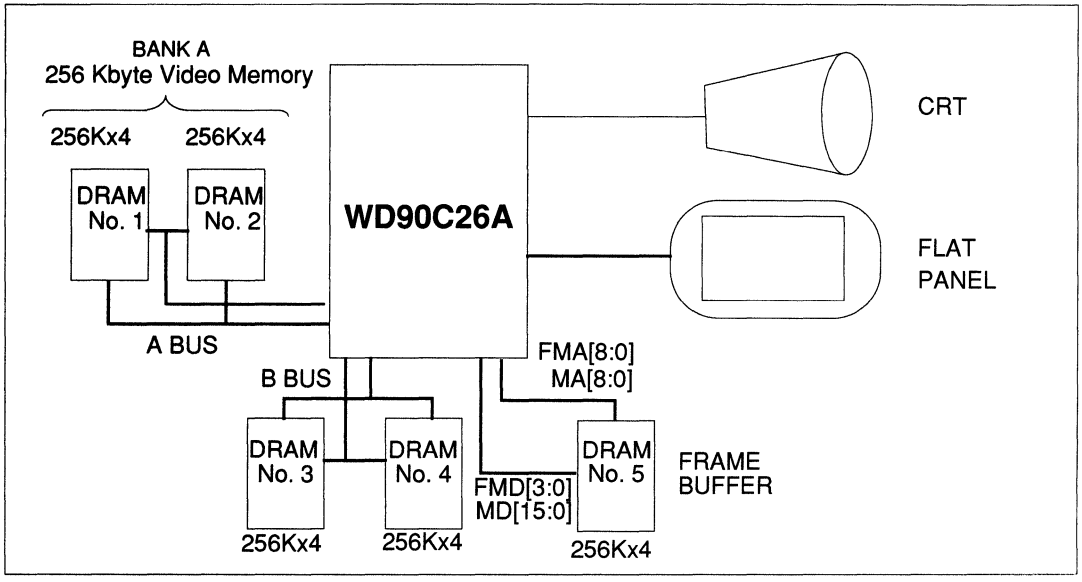

FIGURE 3-3 FIVE 256Kx 4 DRAM IMPLEMENTATION

The following features are supported when 4 256Kx4 DRAMs are used:

- The ability to use 512K video RAM except in those occasional times when a dual panel multiplexed display and a CRT are used simultaneously.
- Support of 640x400x256 and 640x480x256 color modes
- Supports a separate 256K x 4 frame buffer.

Bank B of DRAM can be disabled by firmware for power reduction, and DRAM #3 can be used alone for simultaneous display support of a dual panel display and CRT, while DRAM #4 is disabled.

3.4.4 Display Memory Configuration No. 4 (One 256Kx16 DRAM and One 256Kx4 DRAM)

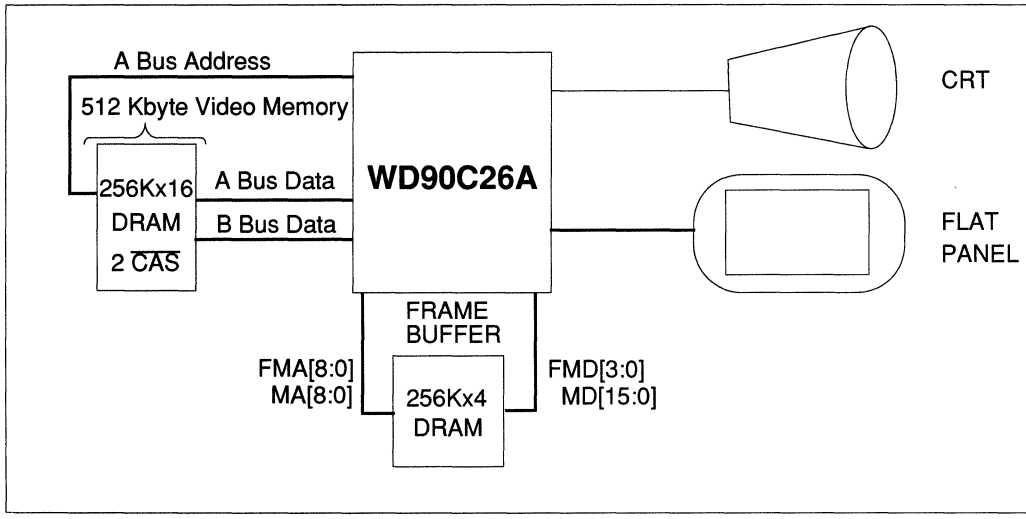

FIGURE 3-4 ONE 256K x 16 AND ONE 256 x 4 DRAM IMPLEMENTATION

The WD90C26A may be used with a single 2 $\overline{CAS}$ 256Kx16 DRAM and a single 256Kx4 DRAM, which provides a separate 265x4 frame buffer in addition to 512 Kbytes of video memory and 16-bit memory performance. The following features are supported:

- Simultaneous display operation with all flat-panel types except dual-panel LCDs is allowed
- Support for 640x400x256 and 640x480x256 color modes.
- Supports a separate 256K x 4 frame buffer.

3.5 VIDEO INTERFACES

The WD90C26A supports a number of video interfaces allowing it to directly connect to most PC compatible CRTs and to a wide range of industry-standard flat-panel types. This support is achieved through configurable CRT and flat-panel interfaces.

3.5.1 Flat Panel Interface

One of the key features of the WD90C26A is a configurable video output port designed for support of a number of flat-panel technologies. This port is designed to directly support a number of panel types without requiring external interface formatting circuitry. Refer to *Panel Interfacing* in Section 6 for a description of the different panel interfaces available and the methods for configuring the WD90C26A for each type of interface.

Programmable flat-panel timing signals allow wide degrees of flexibility in configuring panel interfaces, making the WD90C26A usable with most popular flat-panel designs for PC applications.

The flat panel interface may also be programmed to interface with the WD90C55 VGA Color LCD Interface for certain color multiplexed STN LCD panels with special interface requirements.

3.5.2 Analog CRT Interface

The WD90C26A includes a complete VGA compatible CRT interface with on-board 256 x 18-bit RAMDAC, which can directly drive analog VGA compatible color or monochrome displays.

3.5.3 External RAMDAC Interface

For applications where use of an external RAMDAC or equivalent external function is desired, the WD90C26A flat-panel interface can be configured as an industry-standard RAMDAC interface instead of flat-panel pixel data. This allows the WD90C26A to be used in special applications where a 24-bit RAMDAC is needed or where special panel pixellization techniques are required.

3.5.4 Video Modes

The WD90C26A supports a number of video modes including standard IBM modes, VESA defined extended modes, and Western Digital/Paradise Video modes. All VGA and most VESA modes are supported on both a panel and a CRT. Modes with higher resolution than that of the attached panel are supported in CRT only modes of operation.

Refer to Section 7 for information about screen characteristics.

3.6 CLOCK INTERFACE

The WD90C26A has four clock input signal pins:

- VCLK0
- VCLK1
- VCLK2
- MCLK

Three of these (VCLK 2, 1, and 0) are normally connected to pixel rate oscillators. VCLK1 and VCLK2 may alternately be configured to control an external clock multiplexer or clock generator. In this configuration, VCLK0 becomes the clock input while VCLK1 and VCLK2 become outputs used to drive the multiplexor select inputs.

The memory clock input, MCLK, is used by the internal logic to generate all memory timing and may be up to 44.3 MHz for 70 nsec DRAMs.

4.0 SIGNAL DESCRIPTIONS

4.1 INTRODUCTION

This section contains a pin diagram, a pin out table, and a signal description summary for the following groups of pins:

NOTE

For a listing of multiplexed pins, refer to Section 4.12.

System Interface Pins

AEN/3C3D0
BALE/MADE24/$\overline{\text{PSTART}}$
$\overline{\text{EBROM}}$/$\overline{\text{46E8}}$
IOCHRDY/CDCHRDY/$\overline{\text{PRDY}}$
$\overline{\text{IOCS16}}$/$\overline{\text{CDSETUP}}$
$\overline{\text{IOR}}$/$\overline{\text{S1}}$
$\overline{\text{IOW}}$/$\overline{\text{CMD}}$
IRQ/$\overline{\text{IRQ}}$
LA[19:17]
LA20
LA21
LA22
LA23/BLW1M
$\overline{\text{MEMCS16}}$/$\overline{\text{CDDS16}}$/PM/$\overline{\text{IO}}$
$\overline{\text{MEMR}}$/M/$\overline{\text{IO}}$/$\overline{\text{MEMR}}$
$\overline{\text{MEMW}}$/$\overline{\text{S0}}$/PWR
$\overline{\text{0WS}}$/$\overline{\text{CDSFBK}}$/PCMD
$\overline{\text{REFRESH}}$
RESET
SA[16:0]
$\overline{\text{SBHE}}$
SD[15:0]

Display Buffer Memory Interface Pins

AMA[8:0]/MA[8:0]
$\overline{\text{ACAS}}$/$\overline{\text{CASL}}$/$\overline{\text{CAS}}$
AMD[7:0]/MD[7:0]
$\overline{\text{AOE}}$/$\overline{\text{OE}}$
$\overline{\text{ARAS}}$/$\overline{\text{RAS}}$
$\overline{\text{AWE}}$/$\overline{\text{WEL}}$/$\overline{\text{WE}}$
$\overline{\text{BCAS}}$/$\overline{\text{CASU}}$/$\overline{\text{FCAS}}$
BMA[8:0]/FMA[8:0]
BMD[7:0]/MD[15:8]
$\overline{\text{BOE}}$/$\overline{\text{FOE}}$
$\overline{\text{BRAS}}$/$\overline{\text{FRAS}}$
$\overline{\text{BWE}}$/$\overline{\text{WEU}}$/$\overline{\text{FWE}}$
$\overline{\text{ENDATA}}$/$\overline{\text{FWE}}$/$\overline{\text{FCAS}}$
$\overline{\text{LA22}}$/$\overline{\text{FMD3}}$
$\overline{\text{LA21}}$/$\overline{\text{FMD2}}$
$\overline{\text{LA20}}$/$\overline{\text{FMD1}}$
$\overline{\text{RPLT}}$/$\overline{\text{FMD0}}$

Internal DAC/CRT Interface Pins

ANABLU
ANAGRN
ANARED
FSADJ/$\overline{\text{MDET}}$
HSYNC
V_{REF}/$\overline{\text{DACDISA}}$
VSYNC

Clock Generation Interface Pins

MCLK
VCLK0/VCKIN
VCLK1/$\overline{\text{VCSLD}}$/VCSELL
VCLK2/$\overline{\text{VCSEL}}$/$\overline{\text{VCSELH}}$

Panel Interface Pins

ENDATA
FP
FR/$\overline{\text{BLANK}}$
LD(3:0)
LP
PCLK
$\overline{\text{PNLENA}}$
PNLOFF/$\overline{\text{WPLT}}$/VGADET
$\overline{\text{RPLT}}$/FMD0
UD(3:0)
XSCLK

Power Down Control Pins

$\overline{\text{PWRDOWN}}$

Power Pins

AV_{DD}
AV_{SS}
BV_{DD}
RV_{DD}
RV_{SS}
PV_{DD}
V_{DD}
V_{SS}

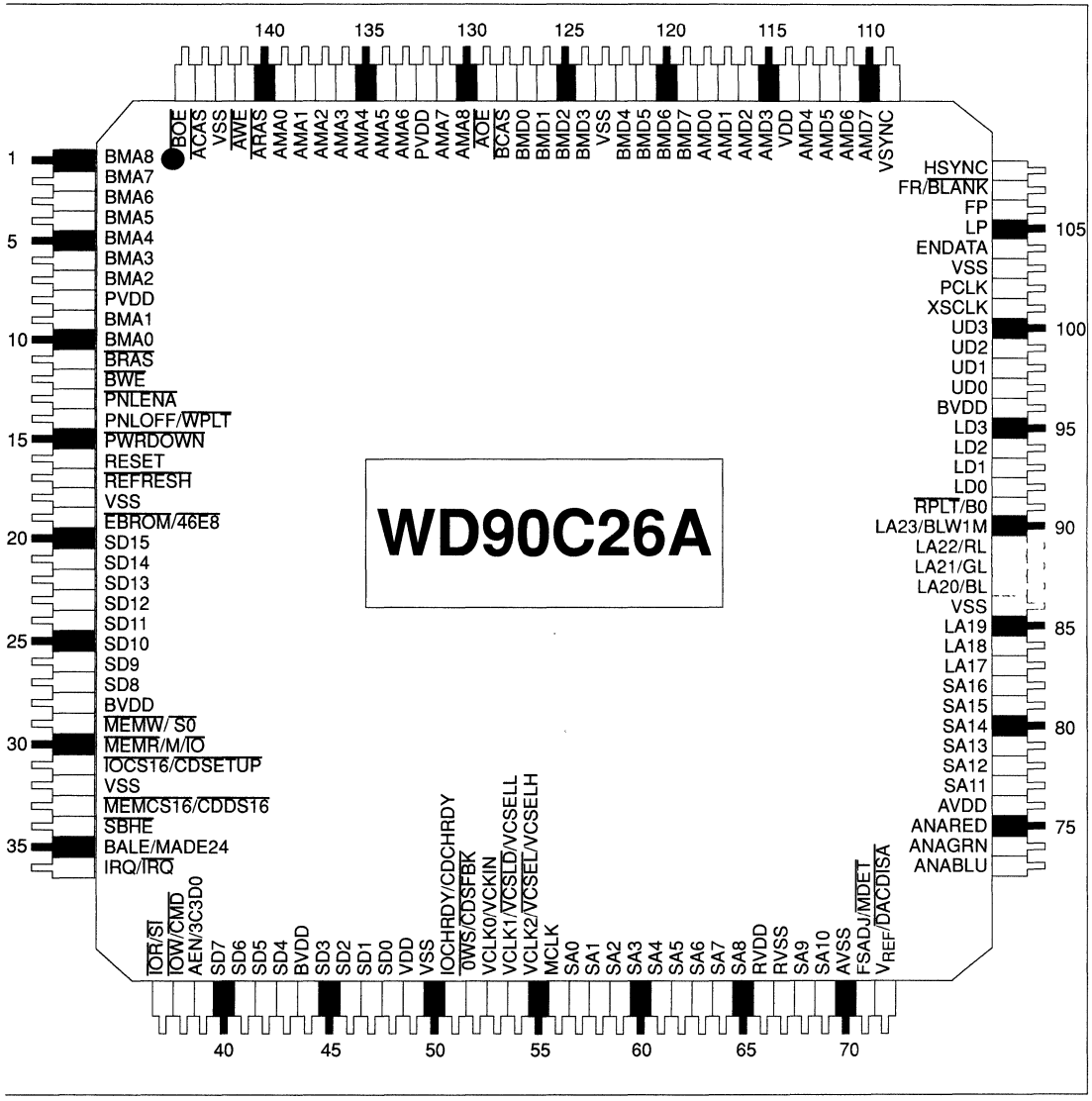

FIGURE 4-1 WD90C26A PIN DIAGRAM, 144 PIN JEDEC MQFP PACKAGE

1.	BMA8/FMA8	30.	MEMR/M/IO/ MEMR	59.	SA2	88.	LA21/FMD2	117.	AMD1/MD1
2.	BMA7/FMA7	31.	IOCS16/ CDSETUP	60.	SA3	89.	LA22/FMD3	118.	AMD0/MD0
3.	BMA6/FMA6	32.	V_{SS}	61.	SA4	90.	LA23/BLW1M	119.	BMD7/MD15
4.	BMA5/FMA5	33.	MEMCS16/ CDDS16/ PM/IO	62.	SA5	91.	RPLT/FMD0/ B0	120.	BMD6/MD14
5.	BMA4/FMA4	34.	SBHE	63.	SA6	92.	LD0	121.	BMD5/MD13
6.	BMA3/FMA3	35.	BALE/ MADE24 PSTART	64.	SA7	93.	LD1	122.	BMD4/MD12
7.	BMA2/FMA2	36.	IRQ/IRQ	65.	SA8	94.	LD2	123.	V_{SS}
8.	PV_{DD}	37.	IOR/SI	66.	RV_{DD}	95.	LD3	124.	BMD3/MD11
9.	BMA1/FMA1	38.	IOW/CMD	67.	RV_{SS}	96.	BV_{DD}	125.	BMD2/MD10
10.	BMA0/FMA0	39.	AEN/3C3D0	68.	SA9	97.	UD0	126.	BMD1/MD9
11.	BRAS/FRAS	40.	SD7	69.	SA10	98.	UD1	127.	BMD0/MD8
12.	BWE/WEU/ FWE	41.	SD6	70.	AV_{SS}	99.	UD2	128.	BCAS/CASU/ FCAS
13.	PNLENA	42.	SD5	71.	FSADJ/MDET	100.	UD3	129.	AOE/OE
14.	PNLOFF/ WPLT/ VGADET	43.	SD4	72.	V_{REF}/ DACDISA	101.	XSCLK	130.	AMA8/MA8
15.	PWRDOWN	44.	BV_{DD}	73.	ANABLU	102.	PCLK	131.	AMA7/MA7
16.	RESET	45.	SD3	74.	ANAGRN	103.	V_{SS}	132.	PV_{DD}
17.	REFRESH	46.	SD2	75.	ANARED	104.	ENDATA	133.	AMA6/MA6
18.	V_{SS}	47.	SD1	76.	AV_{DD}	105.	LP	134.	AMA5/MA5
19.	EBROM/46E8	48.	SD0	77.	SA11	106.	FP	135.	AMA4/MA4
20.	SD15	49.	V_{DD}	78.	SA12	107.	FR/BLANK	136.	AMA3/MA3
21.	SD14	50.	V_{SS}	79.	SA13	108.	HSYNC	137.	AMA2/MA2
22.	SD13	51.	IOCHRDY/ CDCHRDY/ PRDY	80.	SA14	109.	VSYNC	138.	AMA1/MA1
23.	SD12	52.	0WS/ CDSBFK/ PCMD	81.	SA15	110.	AMD7/MD7	139.	AMA0/MA0
24.	SD11	53.	VCLK0/VCKIN	82.	SA16	111.	AMD6/MD6	140.	ARAS/RAS
25.	SD10	54.	VCLK1/ VCSLD/ VCSELL	83.	LA17/SA17	112.	AMD5/MD5	141.	AWE/WEL/ WE
26.	SD9	55.	VCLK2/ VCSEL/ VCSELH	84.	LA18/SA18	113.	AMD4/MD4	142.	V_{SS}
27.	SD8	56.	MCLK	85.	LA19/SA19	114.	V_{DD}	143.	ACAS/CASL/ CAS
28.	BV_{DD}	57.	SA0	86.	V_{SS}	115.	AMD3/MD3	144.	BOE/FOE
29.	MEMW/SO/ PW/R	58.	SA1	87.	LA20/FMD1	116.	AMD2/MD2	145.	

TABLE 4-1 PIN LIST

4.2 SYSTEM INTERFACE PINS

The following table describes each system interface pin on the WD90C26A. The WD90C26A system interface can be configured for either ISA bus or MicroChannel interface support by setting CNF/2 high or low by pulling high or low the AMD2 pin at reset. Other configuration options may also be selected by setting configuration bits high or low at reset through pulling memory data lines high or low. The section called "Using Chip Features" contains a complete description of the various configuration options available by setting these configuration bits.

Where more than one signal name is indicated on the same pin, signals are usually separated by a virgule (/), the pin usage changes depending upon the bus interface as follows:

1. The letters AT in the bus column indicate an ISA bus compatible signal.
2. The letters MC in the bus column indicate a MicroChannel bus compatible signal.
3. The letters PI in the bus column indicate a 386SL Peripheral Interface bus compatible signal.

PIN	SYMBOL	BUS	TYPE	DESCRIPTION
16	RESET	All	Active High Input	**WD90C26A Controller Initialization Signal** Typical usage in ISA Bus based system: connected to ISA Bus RESET signal. Typical usage in MicroChannel based system: connected to MicroChannel RESETDRV signal.
17	$\overline{\text{REFRESH}}$	All	Active Low Input	**DRAM Refresh** The WD90C26A uses this input to initiate refresh operations to its video buffer memory. It also uses this signal as a negative qualifier for memory operations. $\overline{\text{REFRESH}}$ must be inactive high for memory reads or writes to occur.
19	$\overline{\text{EBROM}}$	All	Active Low Output Totem-pole	**Enable BIOS ROM** $\overline{\text{EBROM}}$ if CNF(0)=0, independent of CNF(2) setting. In BIOS ROM Map-in mode, where CNF(0)=0 the WD90C26A drives this output low when it decodes system accesses to video BIOS ROM and a memory read operation is requested from an address range identified within the WD90C26A as a video BIOS ROM address. This function may be disabled by setting PR1 register bit 0 to 1, which forces CNF(0) to 1 until the next reset operation.
	$\overline{\text{46E8}}$	All	Active Low Output Totem-pole	**46E8 I/O Write** If CNF(2)=1 and CNF(0)=1 This pin is an external decode of I/O address 46E8 writes, which can be used as BIOS ROM page select. In this mode, writes to I/O addresses 46E8, 56E8, 66E8, and 76E8 appear as lows at this pin. This decode of writes to 46E8 is disabled by setting PR16(7) high. Descriptions of internal I/O port registers provide more details on how this feature is used.

TABLE 4-2 SYSTEM INTERFACE PINS

15

PIN	SYMBOL	BUS	TYPE	DESCRIPTION
29	$\overline{\text{MEMW}}$	AT	Active Low Input	**Memory Write** $\overline{\text{MEMW}}$ if CNF(2)=1 Memory write input from ISA bus. When the WD90C26A is in ISA Bus Mode, this pin is the industry-standard $\overline{\text{MEMW}}$ bus signal, and indicates to the WD90C26A that a memory write bus cycle is occurring. Because $\overline{\text{MEMW}}$ may also be active during refresh cycles, the WD90C26A internally gates $\overline{\text{MEMW}}$ with $\overline{\text{REFRESH}}$.
	$\overline{\text{S0}}$	MC	Active Low Input	**$\overline{\text{S0}}$ Cycle Decode** $\overline{\text{S0}}$ if CNF(2)=0 When the WD90C26A is in MicroChannel Mode, this pin is the MicroChannel $\overline{\text{S0}}$ channel status input, which the WD90C26A uses, along with $\overline{\text{S1}}$, M/$\overline{\text{IO}}$, and $\overline{\text{CMD}}$, to decode MicroChannel bus cycles.
	PW/$\overline{\text{R}}$	PI	Active Low Input	**PI Bus Write or Read Cycle** Indicates the type of access currently executing on the PI Bus. When high the access is a write operation, and when low the access is a read operation.
30	$\overline{\text{MEMR}}$	AT PI	Active Low Input	**Memory Read** $\overline{\text{MEMR}}$ if CNF(2)=1 This pin is the industry-standard $\overline{\text{MEMR}}$ bus signal and is also shared with the PI bus. This indicates to the WD90C26A that a memory read bus cycle is occurring. Because $\overline{\text{MEMR}}$ may also be active during refresh cycles, the WD90C26A internally gates $\overline{\text{MEMR}}$ with $\overline{\text{REFRESH}}$.
	M/$\overline{\text{IO}}$	MC	Active Low Input	**Memory/IO Cycle** M/$\overline{\text{IO}}$ if CNF(2)=0 When the WD90C26A is in MicroChannel Mode, this pin is the M/$\overline{\text{IO}}$ signal from the MicroChannel bus. A high input at this pin is interpreted by the WD90C26A as a MicroChannel Bus Memory cycle. A low signal at this pin indicates a MicroChannel Bus I/O cycle to the WD90C26A.

TABLE 4-2 SYSTEM INTERFACE PINS

PIN	SYMBOL	BUS	TYPE	DESCRIPTION
31	$\overline{IOCS16}$	AT PI	Active Low Output O.C.	**I/O Chip Select 16** $\overline{IOCS16}$ if CNF(2)=1 Open Collector. Indicates the WD90C26A supports 16-bit I/O operations at the "current" I/O address. In ISA Bus and PI Bus Modes, pin 31 becoming active low as an indication to the bus that it supports 16-bit I/O transfers at the I/O address being presented to it. Otherwise this pin is in a high-impedance state. $\overline{IOCS16}$ is not gated by any other signals. Its function is independent of other bus control lines, bus modes, or register settings. $\overline{IOCS16}$ is not gated by AEN, $\overline{REFRESH}$, or $\overline{PWRDOWN}$, but it is disabled until wakeup. $\overline{IOCS16}$ may also be disabled by host released ($\overline{PWRDOWN}$ with PR35 bit 5=1). After wakeup, PR31 bits 1 and 2 may be used to disabled $\overline{IOCS16}$.
	$\overline{CDSETUP}$	MC	Active Low Output O.C.	**Card Setup** $\overline{CDSETUP}$ if CNF(2)=0). In MicroChannel mode, this pin is the card setup input indicating to the WD90C26A to perform setup functions.
33	$\overline{MEMCS16}$	AT	Active Low Output O. C.	**Memory Chip Select 16** $\overline{MEMCS16}$ if CNF(2)=1 In ISA bus mode, Pin 33 is an indication to the system that the WD90C26A supports 16-bit memory transfers at the system address being presented. If 16-bit transfers are not supported at the address, the WD90C26A tri-states this pin. In ISA Bus applications, pin 33 is typically connected to the ISA Bus $\overline{MEMCS16}$ signal. $\overline{MEMCS16}$ is forced inactive whenever $\overline{REFRESH}$ or $\overline{PWRDOWN}$ are active low. $\overline{MEMCS16}$ is an open-collector output in ISA bus mode.
	$\overline{CDDS16}$	MC	Active Low Output Totem-pole	**Card Data Size 16** $\overline{CDDS16}$ if CNF(2)=0 In MicroChannel applications pin 33 indicates a 16-bit resource available at the address. $\overline{CDDS16}$ is a totem-pole type output in MicroChannel mode.
	PM/$\overline{IO}$	PI	Active Low Input	**PI Bus Memory or I/O.** Indicates the type of cycle currently executing on the PI Bus. When high the cycle is a memory operation, and when low the cycle is an Input/Output operation.

TABLE 4-2 SYSTEM INTERFACE PINS

PIN	SYMBOL	BUS	TYPE	DESCRIPTION
34	$\overline{\text{SBHE}}$	All	Active Low Input	**System Byte Hi Enable** $\overline{\text{SBHE}}$ indicates to the WD90C26A the mapping of bytes into high or low registers on write operations and the ordering of high and low bytes during read operations.
35	BALE	AT	Active High Input	**Address Latch Enable** BALE if CNF(2)=1 (ISA Bus Mode) When the WD90C26A is in ISA Bus Mode this pin is the industry standard BALE signal input to the WD90C26A. A high level is interpreted by the WD90C26A as an indication that the system address is setting up on its SA bus inputs to be latched on the falling edge of this signal. To ensure compatibility across a variety of platforms, the WD90C26A latches LA17-LA23 with the fall of BALE. Typical usage in ISA Bus based system: connected to ISA Bus BALE signal.
	MADE24	MC	Active High Input	**Memory Address Enable 24** MADE24 if CNF(2)=0 (MicroChannel Mode). When the WD90C26A is in MicroChannel Mode, this pin is the MicroChannel MADE24 input to the WD90C26A and is used by the WD90C26A as an indication that the system address is in the below-16 Mbyte range.
	$\overline{\text{PSTART}}$	PI	Active Low Input	**PI Bus start signal** Indicates the start of a PI-bus cycle.

TABLE 4-2 SYSTEM INTERFACE PINS

PIN	SYMBOL	BUS	TYPE	DESCRIPTION
36	IRQ	AT	Active High Output Totem-Pole	**Interrupt Request, Active High** IRQ if CNF(2)=1 When bit 5 of the VGA Vertical Retrace End Register (I/O Address 3?5h index 11) is set to 0, this signal is set active at the occurrence of the end of vertical display of a frame of active video. IRQ stays active until cleared by momentarily setting bit 4 of the Vertical Retrace End Register to 0 and then back to 1. When bit 5 of the VGA Vertical Retrace End Register is set to 1 the activation of this pin is disabled, forcing its output to be low in ISA Bus Mode or high impedance in MicroChannel Mode. NOTE: This pin can only be configured or the interrupt cleared if the Vertical Retrace End Register is unlocked by setting PR3 bit 0 to 1.
	$\overline{IRQ}$	MC	Active Low Output O.C.	**Interrupt Request, Active Low** $\overline{IRQ}$ if CNF(2)=0 Open collector in MicroChannel Mode. Function is identical as IRQ, described above, except active level is low and the signal is open-collector.
37	$\overline{IOR}$	AT PI	Active Low Input	**I/O Read** $\overline{IOR}$ if CNF(2)=1 When the WD90C26A is in ISA Bus or PI Bus Mode, this pin indicates to the WD90C26A that an I/O read bus cycle is to occur. $\overline{IOR}$ may also be active during DMA cycles and is therefore internally qualified by AEN low.
	$\overline{S1}$	MC	Active Low Input	**S1 Cycle Decode** $\overline{S1}$ if CNF(2)=0. When the WD90C26A is in MicroChannel Mode (AMD2 low at reset), this pin is the MicroChannel S1 channel status input, which the WD90C26A uses, along with $\overline{S0}$, M/$\overline{IO}$, and $\overline{CMD}$, to decode MicroChannel bus cycles.

TABLE 4-2 SYSTEM INTERFACE PINS

PIN	SYMBOL	BUS	TYPE	DESCRIPTION
38	$\overline{IOW}$	AT PI	Active Low Input	**I/O Write** $\overline{IOW}$ if CNF(2)=1 When the WD90C26A is in ISA Bus or PI Bus Mode, this pin indicates to the WD90C26A that an I/O read bus cycle is to occur. The WD90C26A internally qualifies $\overline{IOW}$ write requests with AEN low.
	$\overline{CMD}$	MC	Active Low Input	**Command** $\overline{CMD}$ if CNF(2)=0 When the WD90C26A is in MicroChannel Mode, this pin is interpreted by the WD90C26A as the $\overline{CMD}$ signal from a MicroChannel bus. The WD90C26A uses this signal to properly decode cycle types.
39	AEN	AT PI	Active High Input	**Address Enable** AEN if CNF(2)=1 When active high, this signal disables the WD90C26A from performing ISA bus and PI bus read or write accesses. When low, system accesses to the WD90C26A are enabled.
	$\overline{3C3D0}$	MC	Active Low Input	**Video Subsystem Enable Port** $\overline{3C3D0}$ if CNF(2)=0 In MicroChannel mode, this input when pulled active high 'wakes up' the WD90C26A in a manner identical to setting the Wakeup register (3C3h) bit 0 to 1.

TABLE 4-2 SYSTEM INTERFACE PINS

PIN	SYMBOL	BUS	TYPE	DESCRIPTION
51	IOCHRDY	AT	Active High Output O.C.	**I/O Channel Ready Status** IOCHRDY if CNF(2)=1 I/O Channel Ready status when active hi. When the WD90C26A is in ISA Bus Mode pin 51 is the industry-standard IOCHRDY bus signal, and indicates readiness of the WD90C26A in responding to ISA bus read and write cycles. When the WD90C26A cannot complete the desired bus cycle within the standard or 0 wait cycle times, it will de-assert IOCHRDY by pulling it low until it is ready to complete the transfer, otherwise the IOCHRDY output is tri-stated.
	CDCHRDY	MC	Active High Output O.C.	**Channel Ready** CDCHRDY if CNF(2)=1 When the WD90C26A is in MicroChannel Mode, CNF(2)=0), pin 51 is the CDCHRDY signal to a MicroChannel bus. The WD90C26A drives this pin low when additional cycle time is required. In MicroChannel mode, CDCHRDY is brought to its high-impedance inactive state by the rising edge of the signal to $\overline{\text{CMD}}$. Under typical conditions of video memory speeds and bus rates, the WD90C26A does not cause IOCHRDY or CDCHRDY to go inactive low or cause CDCHRDY to occur later than the minimum requirement, except in certain instances when a write operation results in an internal write data buffer overflow.
	$\overline{\text{PRDY}}$	PI	Active Low Output	**PI Bus Ready** Terminates a PI-bus cycle. This signal must be asserted until the rising edge of $\overline{\text{PCMD}}$ to be recognized and terminate the bus cycle.

TABLE 4-2 SYSTEM INTERFACE PINS

PIN	SYMBOL	BUS	TYPE	DESCRIPTION
52	$\overline{0WS}$	AT	Active Low Output O. C.	**Zero Wait State** $\overline{0WS}$ if CNF(2)=1 This pin is the WD90C26A controller's indication of readiness to support zero wait state option. The description of PR32 includes information on how to configure the WD90C26A controller's support of $\overline{0WS}$. Open-collector output in ISA bus mode. The WD90C26A drives this signal low when 0 wait cycles can be supported, otherwise, this signal is tri-stated.
	$\overline{CDSFBK}$	MC	Active Low Output O. C.	**Card Selected Feedback** $\overline{CDSFBK}$ if CNF(2)=0 Feedback to the MicroChannel interface of CD status. Totem-pole output in MicroChannel mode. Driven active low by the WD90C26A as an acknowledgment of its selection. Does not go active if $\overline{CDSETUP}$ is being driven active low.
	$\overline{PCMD}$	PI	Active Low Input	**PI Bus Cycle Command** When asserted during write cycles, this signal indicates valid data on the PI bus, or that data is ready to read. This signal must be asserted during read cycles to provide an output enable.

TABLE 4-2 SYSTEM INTERFACE PINS

4.3 SYSTEM INTERFACE DATA SIGNALS

PIN	SYMBOL	TYPE	DESCRIPTION
SD15 is the MSB and SD0 is the LSB of the 16-bit system data bus in ISA, PI, and MicroChannel bus architectures. The WD90C26A controller's system data signals may be directly connected to the host system data bus, provided the WD90C26A drivers are adequate when host system data bus loading considerations are made. Sections 10-12 provide specifics about the WD90C26A controller's bus drive capabilities.			
20	SD15	I/O	System Data 15
21	SD14	I/O	System Data 14
22	SD13	I/O	System Data 13
23	SD12	I/O	System Data 12
24	SD11	I/O	System Data 11
25	SD10	I/O	System Data 10
26	SD9	I/O	System Data 9
27	SD8	I/O	System Data 8
40	SD7	I/O	System Data 7
41	SD6	I/O	System Data 6
42	SD5	I/O	System Data 5
43	SD4	I/O	System Data 4
45	SD3	I/O	System Data 3
46	SD2	I/O	System Data 2
47	SD1	I/O	System Data 1
48	SD0	I/O	System Data 0

TABLE 4-3 SYSTEM INTERFACE DATA SIGNALS

4.4 SYSTEM INTERFACE ADDRESS SIGNALS

PIN	SYMBOL	TYPE	DESCRIPTION
SA15-SA0 are used by the WD90C26A as the I/O address during ISA, PI, or MicroChannel bus I/O cycles. LA23-LA17 and SA16-SA0 are used by the WD90C26A as the system address bus during memory cycles. SA16-SA0 are used as the lower 17 bits of the WD90C26A controller's 24-bit memory address during ISA, PI, or MicroChannel bus memory cycles. SA16 is the MSB and SA0 is the LSB of the system address bus (SA[16:0]).			
57	SA0	Input	System Address 0
58	SA1	Input	System Address 1
59	SA2	Input	System Address 2
60	SA3	Input	System Address 3
61	SA4	Input	System Address 4
62	SA5	Input	System Address 5
63	SA6	Input	System Address 6
64	SA7	Input	System Address 7
65	SA8	Input	System Address 8
68	SA9	Input	System Address 9
69	SA10	Input	System Address 10
77	SA11	Input	System Address 11
78	SA12	Input	System Address 12
79	SA13	Input	System Address 13
80	SA14	Input	System Address 14
81	SA15	Input	System Address 15
82	SA16	Input	System Address 16

TABLE 4-4 SYSTEM INTERFACE ADDRESS SIGNALS

4.5 SYSTEM INTERFACE EXTENDED/LATCHABLE ADDRESS SIGNALS

LA19-LA17 (SA19-SA17) are extended/ latchable system address signals. LA19 is the MSB of the 20-bit below-1 Mbyte (BLW1M) memory address bus in the ISA, PI, and MC bus architectures, formed by using LA19-LA17 and SA16-SA0. The WD90C26A uses the resulting memory address, along with either the BLM1M signal or a decoded LA23-LA20 address, for accesses to its video memory buffer DRAM.
In other modes, the WD90C26A uses the address formed by LA19-SA0, along with the 1 Mbyte block decode from LA23-LA20, to access the controller's buffer as above-1 Mbyte memory.

In ISA bus mode, when CNF1=0 and CNF2=1, LA19-LA17 are inputs to a transparent latch internal to the WD90C26A that allows LA19-LA17 to propagate in while BALE is active high. LA19-LA17 are then captured when BALE goes inactive low.

In MC mode, when CNF1=0 and CNF2=0, SA19-SA17 are unlatched address inputs.

83	LA17/SA17	Input	**Latchable System Address 17**
84	LA18/SA18	Input	**Latchable System Address 18**
85	LA19/SA19	Input	**Latchable System Address 19**
87	LA20	Input	**Latchable System Address Bit 20** If CNF(7)=0, LA20 is selected as an input. If CNF(7)=1, LA20 is selected as an output.
	FMD1	Output	**External Frame Buffer Data Bit 1, Memory Configurations 3 and 4.** Used in a separate 256Kx4 frame buffer interface for memory configurations No. 3 and 4. Refer to Table 4-14.
88	LA21	I/O	**Latchable System Address Bit 21** If CNF(7)=0, LA21 is selected as an input. If CNF(7)=1, LA21 is selected as an output.
	FMD2	Output	**External Frame Buffer Data Bit 2, Memory Configurations 3 and 4.** Used in a separate 256Kx4 frame buffer interface for memory configurations No. 3 and 4. Refer to Table 4-14.
89	LA22	I/O	**Latchable System Address Bit 22** If CNF(7)=0, LA22 is selected as an input. If CNF(7)=1, LA22 is selected as an output.
	FMD3	Output	**External Frame Buffer Data Bit 3, Memory Configurations 3 and 4.** Used in a separate 256Kx4 frame buffer interface for memory configurations No. 3 and 4. Refer to Table 4-14.
90	LA23	I/O	**Latchable System Address Bit 23** LA23 is the LSB of the 24-bit system address formed by LA(23:17) and SA(16:0).
	BLW1M	Input	**Below 1 Megabyte Address Decode** BLWIM (12-bit I/F mode). Active high input from external decode indicating that the system address is in the below-1 Mbyte address range of 00000h to FFFFFh.
91	RPLT	Output	**Read Palette** If not configured for a color TFT interface, this pin is the active low read pulse to the external RAMDAC or equivalent circuit. The subsection "Using an External RAMDAC" in Section 6, describes how an external RAMDAC is connected to the WD90C26A.
	FMD0	Output	**External Frame Buffer Data Bit 0, Memory Configurations 3 and 4.** Used in a separate 256Kx4 frame buffer interface. Refer to Table 4-14.

TABLE 4-5 SYSTEM INTERFACE EXTENDED/LATCHABLE ADDRESS SIGNALS

4.6 DISPLAY BUFFER MEMORY INTERFACE PINS

The display memory interface is designed for connection of up to five 256Kx4 or one 256Kx16 and one 256Kx4 fast-page-mode DRAMs.

This section is divided into the following subsections, which provide tables describing the signals below:

- Bank A Video Memory Signals
- Bank B Video Memory Signals
-

4.6.1 Bank A Video Memory SignalS

PIN	SYMBOL	TYPE	DESCRIPTION
Bank A Video Memory Data Bits			
110	AMD7/MD7	I/O	Bank A Data Bit 7/ Data Bit 7 for Memory Configurations 2 - 4.
111	AMD6/MD6	I/O	Bank A Data Bit 6/ Data Bit 6 for Memory Configurations 2 - 4.
112	AMD5/MD5	I/O	Bank A Data Bit 5/ Data Bit 5 for Memory Configurations 2 - 4.
113	AMD4/MD4	I/O	Bank A Data Bit 4/ Data Bit 4 for Memory Configurations 2 - 4.
115	AMD3/MD3	I/O	Bank A Data Bit 3/ Data Bit 3 for Memory Configurations 2 - 4.
116	AMD2/MD2	I/O	Bank A Data Bit 2/ Data Bit 2 for Memory Configurations 2 - 4.
117	AMD1/MD1	I/O	Bank A Data Bit 1/ Data Bit 1 for Memory Configurations 2 - 4.
118	AMD0/MD0	I/O	Bank A Data Bit 0/ Data Bit 0 for Memory Configurations 2 - 4.
Bank A Video Memory Address Bits			
130	AMA8/MA8	Output	Bank A Address Bit 8/ Address Bit 8 for Memory Configurations 2 - 4.
131	AMA7/MA7	Output	Bank A Address Bit 7/ Address Bit 7 for Memory Configurations 2 - 4.
133	AMA6/MA6	Output	Bank A Address Bit 6/ Address Bit 6 for Memory Configurations 2 - 4.
134	AMA5/MA5	Output	Bank A Address Bit 5/ Address Bit 5 for Memory Configurations 2 - 4.
135	AMA4/MA4	Output	Bank A Address Bit 4/ Address Bit 4 for Memory Configurations 2 - 4.
136	AMA3/MA3	Output	Bank A Address Bit 3/ Address Bit 3 for Memory Configurations 2 - 4.
137	AMA2/MA2	Output	Bank A Address Bit 2/ Address Bit 2 for Memory Configurations 2 - 4.
138	AMA1/MA1	Output	Bank A Address Bit 1/ Address Bit 1 for Memory Configurations 2 - 4.
139	AMA0/MA0	Output	Bank A Address Bit 0/ Address Bit 0 for Memory Configurations 2 - 4.
Primary 9-bit video buffer DRAM address bus. AMA8 is the MSB and AMA0 the LSB.			

TABLE 4-6 BANK A VIDEO MEMORY SIGNALS

PIN	SYMBOL	TYPE	DESCRIPTION
			Bank A Video Memory Control Signals
143	$\overline{ACAS}$	Output	**CAS Bank A, Memory Configuration 1** Column address strobe for video memory buffer DRAM bank A, consisting of four 256Kx4 DRAMs.
	$\overline{CASL}$	Output	**CAS Lower, Memory Configurations 2 and 4.** When a 256Kx16 DRAM is used, this is the lower $\overline{CAS}$ strobe output and the $\overline{CASU}$ signal is the upper $\overline{CAS}$ strobe output.
	$\overline{CAS}$	Output	**CAS, Memory Configuration 3** Column address strobe for video memory buffer consisting of five 256Kx4 DRAMs.
129	$\overline{AOE}$	Output	**Output Enable Bank A, Memory Configuration 1** Output Enable control for video memory buffer DRAM bank A.
	$\overline{OE}$	Output	**Output Enable, Memory Configurations 2 - 4** Output Enable control for video memory buffer DRAM. When a 256Kx16 DRAM or five 256Kx4 DRAMs are used, this is the DRAM output enable strobe
140	$\overline{ARAS}$	Output	**RAS Bank A, Memory Configuration 1** Row address strobe for video memory buffer DRAM banks A, consisting of four 256Kx4 DRAMs.
	$\overline{RAS}$	Output	**RAS, Memory Configurations 2 - 4** Row address strobe for video memory buffer DRAM. When a 256Kx16 DRAM or five 256K x4 DRAMs are used, this is the DRAM $\overline{RAS}$ strobe output.
141	$\overline{AWE}$	Output	**Write Enable Bank A, Memory Configuration 1** Write Enable control for video memory buffer DRAM bank A.
	$\overline{WE}$	Output	**Write Enable, Memory Configurations 2 and 4.** Write Enable control for video memory buffer. When a 256Kx16 DRAM is used this is the DRAM write enable output.
	$\overline{WEL}$	Output	**Write Enable Low, Memory Configuration 3** Write Enable Low control for video memory buffer consisting of five 256Kx4 DRAMs. $\overline{WEU}$ is the upper control for memory configuration 3.

TABLE 4-6 BANK A VIDEO MEMORY SIGNALS

4.6.2 Bank B Video Memory Signals

PIN	SYMBOL	TYPE	DESCRIPTION
Bank B Video Memory Data Bits			
119	BMD7/MD15	I/O	Bank B Data Bit 7/Data Bit 15 for Memory Configurations 2 - 4.
120	BMD6/MD14	I/O	Bank B Data Bit 6/Data Bit 14 for Memory Configurations 2 - 4
121	BMD5/MD13	I/O	Bank B Data Bit 5/Data Bit 13 for Memory Configurations 2 - 4.
122	BMD4/MD12	I/O	Bank B Data Bit 4/Data Bit 12 for Memory Configurations 2 - 4
124	BMD3/MD11	I/O	Bank B Data Bit 3/Data Bit 11 for Memory Configurations 2 - 4.
125	BMD2/MD10	I/O	Bank B Data Bit 2/Data Bit 10 for Memory Configurations 2 - 4
126	BMD1/MD9	I/O	Bank B Data Bit 1/Data Bit 9 for Memory Configurations 2 - 4.
127	BMD0/MD8	I/O	Bank B Data Bit 0/Data Bit 8 for Memory Configurations 2 - 4
Bank B Video Memory Address Bits			
1	BMA8/FMA8*	Output	Bank B Address Bit 8/Address Bit 8 for Memory Configurations 3 and 4.
2	BMA7/FMA7*	Output	Bank B Address Bit 7/Address Bit 7 for Memory Configurations 3 and 4.
3	BMA6/FMA6*	Output	Bank B Address Bit 6/Address Bit 6 for Memory Configurations 3 and 4.
4	BMA5/FMA5*	Output	Bank B Address Bit 5/Address Bit 5 for Memory Configurations 3 and 4.
5	BMA4/FMA4*	Output	Bank B Address Bit 4/Address Bit 4 for Memory Configurations 3 and 4.
6	BMA3/FMA3*	Output	Bank B Address Bit 3/Address Bit 3 for Memory Configurations 3 and 4.
7	BMA2/FMA2*	Output	Bank B Address Bit 2/Address Bit 2 for Memory Configurations 3 and 4.
9	BMA1/FMA1*	Output	Bank B Address Bit 1/Address Bit 1 for Memory Configurations 3 and 4.
10	BMA0/FMA0*	Output	Bank B Address Bit 0/Address Bit 0 for Memory Configurations 3 and 4.
BMA8 is the MSB and BMA0 the LSB. *Not Used for Memory Configuration 2			
Bank B Video Memory Control Signals			
11	$\overline{\text{BRAS}}$	Output	**RAS Bank B, Memory Configuration 1** Row address strobe for video memory buffer DRAM bank B, consisting of four 256Kx4 DRAMs.
	$\overline{\text{FRAS}}$*	Output	**RAS Bank B, Memory Configuration 3 and 4** Row address strobe for a frame buffer consisting of a separate 256Kx4 DRAM.

TABLE 4-7 BANK B VIDEO MEMORY SIGNALS

PIN	SYMBOL	TYPE	DESCRIPTION
12	$\overline{BWE}$	Output	**Write Enable Bank B, Memory Configuration 1** Write Enable control for video memory buffer DRAM bank B.
	$\overline{WEU}$	Output	**Write Enable Upper, Memory Configuration 3** Write Enable Upper control for video memory buffer consisting of five 256Kx4 DRAMs. $\overline{WEL}$ is the lower control for memory configuration 3.
	$\overline{FWE}$*	Output	**Write Enable, Frame Buffer, Memory Configuration 4** Write Enable control for a frame buffer consisting of a separate 256Kx4 DRAM. $\overline{FWE}$ for Memory Configuration 3 is on pin 104.
104	ENDATA	Output	**Enable Data** This is a data enable output for panels. In a Plasma interface, it is an "enable video" signal.
	$\overline{FWE}$	Output	**Write Enable, Frame Buffer, Memory Configuration 3** Write Enable control for a frame buffer consisting of a separate 256Kx4 DRAM. $\overline{FWE}$ for Memory Configuration 4 is on pin 12.
	$\overline{FCAS}$	Output	**CAS, Frame Buffer, Memory Configuration 4** Column address strobe for a frame buffer consisting of a separate 256Kx4 DRAM. $\overline{FCAS}$ for Memory Configuration 3 is on pin 128.
128	$\overline{BCAS}$	Output	**CAS Bank B, Memory Configuration 1** Column address strobe for video memory buffer DRAM bank B consisting of four 256Kx4 DRAMs.
	$\overline{CASU}$	Output	**CAS Upper, Memory Configurations 2 and 4.** When a 256Kx16 DRAM is used, this is the upper $\overline{CAS}$ strobe output and the $\overline{CASL}$ signal is the lower $\overline{CAS}$ strobe output.
	$\overline{FCAS}$	Output	**CAS, Frame Buffer, Memory Configuration 3** Column address strobe for a frame buffer consisting of a separate 256Kx4 DRAM. $\overline{FCAS}$ for Memory Configuration 4 is on pin 104.
144	$\overline{BOE}$	Output	**Output Enable Bank B, Memory Configuration 1** Output Enable control for video memory buffer DRAM bank B.
	$\overline{FOE}$*	Output	**Output Enable, Frame Buffer, Memory Configurations 3 and 4** Output Enable control for a frame buffer consisting of a separate 256Kx4 DRAM.

TABLE 4-7 BANK B VIDEO MEMORY SIGNALS

4.7 INTERNAL DAC/CRT INTERFACE Pins

Internal DAC analog interface pins are described in the following table.

PIN	SYMBOL	TYPE	DESCRIPTION
75	ANARED	Output Analog	CRT Red Drive
74	ANAGRN	Output Analog	CRT Green Drive
73	ANABLU	Output Analog	CRT Blue Drive
72	V_{REF}	Input Analog	**Attach External Precision Reference Input** V_{REF} if above Vss DAC reference voltage. The input for attachment of an external precision reference used by the WD90C26A controller's internal DAC for regulation purposes. Section 10, "Internal DAC Specifics" contains specifics on reference voltage requirements.
	$\overline{DACDISA}$	Input	**Disable Internal DAC** $\overline{DACDISA}$ if tied to Vss. If the internal DAC is not needed to drive a CRT, this input may be grounded to disable the internal DAC.
71	FSADJ	Input Analog	**DAC Full-Scale Adjustment** FSADJUST if pin 72 is above Vss. If pin 72 is above Vss, this pin serves as the input for a DAC full-scale current adjust external resistor or potentiometer. Refer to the subsection entitled "CRT Interfacing" in Section 6 for a description of how to determine full-scale resistance values to be attached to this pin. **CAUTION:** Do not ground this pin unless $\overline{DACDISA}$ is tied to Vss.
	$\overline{MDET}$	Input	**Monitor Detect Input** $\overline{MDET}$ if pin 72 is tied to Vss. When pin 72 is tied to Vss, this pin is a digital input to which may be connected an external monitor detect circuit as part of an external RAMDAC support. When pin 72 is tied to Vss, the internal monitor detection circuitry is disabled, and instead a low level at this pin causes bit 4 of the VGA input status register 0 to go high. See the description of Input Status Register 0 in Section 5 for details on how the level at this input appears.

TABLE 4-8 INTERNAL DAC ANALOG INTERFACE PINS

PIN	SYMBOL	TYPE	DESCRIPTION
108	HSYNC	Output	**CRT Horizontal Sync** HSYNC is the CRT horizontal sync control signal output. It may be directly attached to CRT monitor connections. Its active low or high level is programmable as is its position and duration. This pin is inactive when the WD90C26A is in power-down modes or CRT display is not enabled. Control of horizontal sync polarity is done by setting register bits in the VGA Miscellaneous Output Register and in PR3 and PR39.
109	VSYNC	Output	**CRT Vertical Sync** VSYNC is the CRT vertical sync control signal output. It may be directly attached to CRT monitor connections. Its active low or high level is programmable. This pin is inactive when the WD90C26A is in power-down modes or CRT display is not enabled. Control of vertical sync polarity is done by setting register bits in the VGA Miscellaneous Output Register and in PR3 and PR39.

TABLE 4-8 INTERNAL DAC ANALOG INTERFACE PINS

4.8 CLOCK GENERATION INTERFACE PINS

Clock generation interface pins are described in the following table. Refer to the subsection "Clock Interfacing" in Section 6 for descriptions of how various clock interfaces may be attached to these clock signals.

PIN	SYMBOL	TYPE	DESCRIPTION
53	VCLK0	Input	**Video Clock 0** VCLK0 if CNF(3) = 0. The primary of four possible video clock inputs to the WD90C26A. VCLK0 is the main video clock to the WD90C26A.
	VCKIN	Input	**Video Clock Input** VCKIN if CNF(3) = 1 If CNF(3) = 1, this pin is VCKIN, the video clock input from an external frequency source or multiplexer, whose frequency is controlled by Miscellaneous Write Register bit 2, and depending on PR15 bit 5, bit 3, of the Miscellaneous Write Register. Selection of the video shift clock is internally overridden if MCLK has been selected by the setting of PR15 bit 4.
54	VCLK1	Input	**Video Clock 1** VCLK1 if CNF(3) = 0. VCLK1 is the second of four possible video clock inputs to the WD90C26A, which are internally selected to provide video shift clock rates for various screen formats and display types.
	$\overline{\text{VCSLD}}$	Output	**Video Clock Select Load** $\overline{\text{VCSLD}}$ if CNF(3) = 1 and PR15(5) = 0. This signal is typically used as a video clock select load control line to an external clock synthesizer. It is a decode of 3C2h writes.
	VCSELL	Output	**Video Clock Select Low** VCSELL if CNF(3) = 1 and PR15(5) = 1 This signal is the lower order signal of the pair (VCSELH and VCSELL), which are outputs used as select lines to an external video clock source multiplexer. VCSELL is set to the level of the VGA Miscellaneous Output Register, bit 2.

TABLE 4-9 CLOCK GENERATION INTERFACE PIN TABLE

PIN	SYMBOL	TYPE	DESCRIPTION
55	VCLK2	Input	**Video Clock 2** VCLK2 if CNF(3) = 0. The third of four possible video clock inputs to the WD90C26A, which are internally selected to provide video shift clock rates for various screen formats and display types.
	$\overline{\text{VCSEL}}$	Output	**Video Clock Select** $\overline{\text{VCSEL}}$ if CNF(3) = 1 and PR15(5) = 0. VCSEL is typically used as a video clock select control link to an external multiple video frequency source. Its output follows the setting of WD90C26A register PR2 bit 1.
	VCSELH	Output	**Video Clock Select Hi** $\overline{\text{VCSELH}}$ if CNF(3) = 1 and PR15(5) = 1. This signal is the higher order signal of VCSELH and VCSELL, which are outputs used as select lines to an external video clock source multiplexer. VCSELH is set to the level of the VGA Miscellaneous Output Register, bit 3.
56	MCLK	Input	**Memory Timing Clock Input** This signal is the memory timing clock input to the WD90C26A. Its speed dictates video memory access timing and speeds as well as system I/O timing. MCLK may also serve as a fourth possible source of video clock.

TABLE 4-9 CLOCK GENERATION INTERFACE PIN TABLE

4.9 PANEL INTERFACE PINS

PIN	SYMBOL	TYPE	DESCRIPTION
13	$\overline{\text{PNLENA}}$	Output, Active Low	**Panel Enable** $\overline{\text{PNLENA}}$ is used to control the power supply for the attached panel. Refer to the subsection "Panel Protection" in Section 6 for a description of the special features of this signal.
14	PNLOFF	Output, Active High	**Panel Power Off** PNLOFF if PR57 bit 1 is set to 0 and PR57 bit 7 is set to 0. The Power-Off active high signal to the bias supply circuit of an LCD panel. The PNLOFF signal is used as a power enable/disable to the high voltage bias inverter of a panel, and is tied to the WD90C26A controller's power management circuit. The WD90C26A sequences this signal as part of the panel power/powerdown procedures designed to protect panel power circuit. A high at this output indicates power-off to the panel and a low power-on. Refer to the subsection called "Panel Protection" in Section 6 for a description of the special features of this signal.
	$\overline{\text{WPLT}}$	Output, Active Low	**Write Palette** $\overline{\text{WPLT}}$ if PR57 bit 1 is set to 1 and PR57 bit 7 is set to 0. If the WD90C26A has been configured for external DAC mode, $\overline{\text{WPLT}}$ is the write pulse to the external RAMDAC or equivalent circuit.
	VGADET	Output, Active High	**VGA Detect** VGADET if PR57 bit 7 is set to 1. Provides a hardware VGA device output signal that can be used for external power control. Refer to Section 6 for a description of VGA detect operation.
91	$\overline{\text{RPLT}}$	Output, Active Low	**Read Palette** If not configured for a color TFT interface, this pin is the active low read pulse to the external RAMDAC or equivalent circuit. The subsection "Using an External RAMDAC" in Section 6, describes how an external RAMDAC is connected to the WD90C26A.
	FMD0	Output, Active High	**External Frame Buffer Data Bit 0, Memory Configurations 3 and 4.** Used in a separate 256Kx4 frame buffer interface. Refer to Table 4-14.
	B0	Output	Blue Data Bit If the WD90C26A is configured for a 9-bit color TFT interface, this pin is the low-order blue video data output to a panel. If the WD90C26A is configured for a 12-bit color TFT interface, this pin is the second-to-low-order blue video data output to a panel.

TABLE 4-10 PANEL INTERFACE PINS

PIN	SYMBOL	TYPE	DESCRIPTION
102	PCLK	Output, Active High	**Pixel Clock** This pin serves as a pixel clock output which may be used to latch pixel data from the WD90C26A controller's video output bus into an external RAMDAC or panel interface. Pixel data from the WD90C26A changes on the rising edge of PCLK and is intended to be latched into an external RAMDAC or panel interface by the falling edge of PCLK. PR4 bit 6 controls the characteristics of PCLK. The subsection called "Using an External RAMDAC" in Section 6 contains information on how to configure the WD90C26A to operate with an external RAMDAC.
107	FR	Output, Active High	**Frame Rate Signal** Whenever the WD90C26A is operating in any LCD mode, FR is a free-running clock which is intended to be connected to FR inputs on some LCD panels. Frequency of its signal is programmable and is controlled by setting PR62. LCD modes are defined when PR19 bit 4 = 1 and PR18(1:0) = 00 or 11.
	$\overline{\text{BLANK}}$	Output, Active Low	**Blanking Control Signal** $\overline{\text{BLANK}}$ is the standard analog VGA RAMDAC blanking signal. Output when the WD90C26A is not operating in any LCD modes.
106	FP	Output, Active High	**Frame Pulse** FP is output as an indication to attached panels that a frame has begun.
105	LP	Output, Active High	**Latch Pulse** The LP output is intended to be used by a panel to latch all the current panel data into the current scan line of the panel.
104	ENDATA	Output, Active High	**Enable Data** This is a data enable output for panels. In a Plasma interface, it is an "enable video" signal.
	$\overline{\text{FWE}}$	Output	**Write Enable, Frame Buffer, Memory Configuration 3** Write Enable control for a frame buffer consisting of a separate 256Kx4 DRAM. $\overline{\text{FWE}}$ for Memory Configuration 4 is on pin 12.
	$\overline{\text{FCAS}}$		**CAS, Frame Buffer, Memory Configuration 4** Column address strobe for a frame buffer consisting of a separate 256Kx4 DRAM. $\overline{\text{FCAS}}$ for Memory Configuration 3 is on pin 128.
101	XSCLK	Output, Active High	**X Driver Shift Clock** In a dual panel interface, this signal is used to shift the upper and lower panel data into the X-driver.

TABLE 4-10 PANEL INTERFACE PINS

PIN	SYMBOL	TYPE	DESCRIPTION
100 99 98 97	UD3 UD2 UD1 UD0	Output	Upper Panel Data Bit 3 to Bit 0 In a dual-panel LCD interface, these signals are used for the upper panel data bus. In a single-panel LCD interface these pins also provide video data to the panel. In a plasma interface, they provide the pure 4-bit video data interface. Refer to Section 6, the subsection called "Panel Interfacing" for further information on how these bits are defined for various panel interfaces. In a CRT interface, they are the upper four bits of pixel video outputs to the RAMDAC. The section called "Using an External RAMDAC" in Section 6 describes how to use the WD90C26A with an external RAMDAC.
95 94 93 92	LD3 LD2 LD1 LD0	Output	Lower Panel Data Bit 3 to Bit 0 In an LCD interface, these signals are used for the lower panel data bus. In a 4-bit plasma interface, they are reserved. In an 8-bit plasma interface these provide the second pixel of video data to the panel. Refer to Section 6, the subsection called "Panel Interfacing" for further information on how these bits are defined for various panel interfaces. In a CRT interface, they are the lower four bits of pixel video outputs to the RAMDAC.

TABLE 4-10 PANEL INTERFACE PINS

4.10 POWER DOWN CONTROL PINS

PIN	SYMBOL	TYPE	DESCRIPTION
15	$\overline{\text{PWRDOWN}}$	Input	**Input Active Low Power Down Control** When active low, this pin causes flat-panel and CRT display update circuitry to halt. $\overline{\text{PNLENA}}$ goes inactive, PNLOFF goes active high, and $\overline{\text{BLANK}}$ goes active low (if not configured for $\overline{\text{FR}}$ output). The internal RAMDAC's red, green, and blue outputs to pins 73-75 are shut off. Flat-panel and CRT timing signals are halted.

TABLE 4-11 POWER DOWN CONTROL PINS

4.11 POWER PINS

PINS	SYMBOL	TYPE	DESCRIPTION
8, 132	PV_{DD}	Power	Powerdown section V_{DD} supply.
18, 32, 50, 86, 103, 123, 142	V_{SS}	Ground	Ground. V_{SS} = 0V.
28, 44, 96	BV_{DD}	Power	Bus interface V_{DD} supply for system bus, panel, CRT, and clock interfaces.
49, 114	V_{DD}	Power	WD90C26A main V_{DD} supply to core and memory data buses.
66	RV_{DD}	Power	RAM palette V_{DD} supply.
67	RV_{SS}	Ground	RAM palette V_{SS} connection.
70	AV_{SS}	Ground	Internal DAC V_{SS} connection.
76	AV_{DD}	Power	Internal DAC V_{DD} power connection.

TABLE 4-12 POWER PINS

4.12 MULTIPLEXED SIGNALS

The following tables are provided for reference to quickly identify the WD90C26A controller pins that have multiple uses. Multiple use is accomplished by multiplexing more than one signal on the same pin. Section 6.6 describes how multiplexing is accomplished through hardware configuration.

The multiplexed pins except display memory are listed by pin numbers in Table 4-13. The pin numbers and signal names are given for the pins that have multiple uses only (refer to the notes at the end of the table). Multiplexed display memory pins are listed in Table 4-14.

PIN		ISA BUS	PI BUS	MICROCHANNEL
NO.	NAME			
14	PNLOFF/$\overline{\text{WPLT}}$/ VGADET[5]	PNLOFF/$\overline{\text{WPLT}}$/ VGADET[5]	PNLOFF/$\overline{\text{WPLT}}$/ VGADET[5]	PNLOFF/$\overline{\text{WPLT}}$/ VGADET[5]
19	$\overline{\text{EBROM}}$/46E8[3]	$\overline{\text{EBROM}}$/46E8[3]	$\overline{\text{EBROM}}$/46E8[3]	$\overline{\text{EBROM}}$/46E8[3]
29	$\overline{\text{MEMW}}$	$\overline{\text{MEMW}}$	PW/$\overline{\text{R}}$	$\overline{\text{S0}}$
30	$\overline{\text{MEMR}}$	$\overline{\text{MEMR}}$	$\overline{\text{MEMR}}$[1]	M/$\overline{\text{IO}}$
31	$\overline{\text{IOCS16}}$	$\overline{\text{IOCS16}}$	$\overline{\text{IOCS16}}$	$\overline{\text{CDSETUP}}$
33	$\overline{\text{MEMCS16}}$	$\overline{\text{MEMCS16}}$	PM/$\overline{\text{IO}}$	$\overline{\text{CDDS16}}$
35	BALE	BALE	$\overline{\text{PSTART}}$	MADE24
36	IRQ	IRQ	IRQ	$\overline{\text{IRQ}}$
37	$\overline{\text{IOR}}$	$\overline{\text{IOR}}$	$\overline{\text{IOR}}$[2]	S1
38	$\overline{\text{IOW}}$	$\overline{\text{IOW}}$	$\overline{\text{IOW}}$[2]	$\overline{\text{CMD}}$
39	AEN	AEN	AEN[2]	3C3D0
51	IOCHRDY	IOCHRDY	$\overline{\text{PRDY}}$	CDCHRDY
52	$\overline{\text{OWS}}$	$\overline{\text{OWS}}$	$\overline{\text{PCMD}}$	$\overline{\text{CDSFBK}}$
53	VCLK0/VCKIN[6]	VCLK0/VCKIN[6]	VCLK0/VCKIN[6]	VCLK0/VCKIN[6]
54	VCLK1/$\overline{\text{VCSLD}}$/ VCSELL[6]	VCLK1/$\overline{\text{VCSLD}}$/ VCSELL[6]	VCLK1/$\overline{\text{VCSLD}}$/ VCSELL[6]	VCLK1/$\overline{\text{VCSLD}}$/ VCSELL[6]
55	VCLK2/VCSEL/ VCSELH[6]	VCLK2/VCSEL/ VCSELH[6]	VCLK2/VCSEL/ VCSELH[6]	VCLK2/VCSEL/ VCSELH[6]
71	FSADJ/$\overline{\text{MDET}}$[4]	FSADJ/$\overline{\text{MDET}}$[4]	FSADJ/$\overline{\text{MDET}}$[4]	FSADJ/$\overline{\text{MDET}}$[4]
72	V_{REF}/$\overline{\text{DACDISA}}$[4]	V_{REF}/$\overline{\text{DACDISA}}$[4]	V_{REF}/$\overline{\text{DACDISA}}$[4]	V_{REF}/$\overline{\text{DACDISA}}$[4]
83	LA17	LA17	LA17	SA17
84	LA18	LA18	LA18	SA18
85	LA19	LA19	LA19	SA19
87	LA20/FMD1[7]	LA20/FMD1[7]	LA20/FMD1[7]	LA20/FMD1[7]
88	LA21/FMD2[7]	LA21/FMD2[7]	LA21/FMD2[7]	LA21/FMD2[7]
89	LA22FMD3[7]	LA22FMD3[7]	LA22FMD3[7]	LA22FMD3[7]
90	LA23/BLW1M6[7]	LA23/BLW1M6[7]	LA23/BLW1M6[7]	LA23/BLW1M6[7]
91	RPLT/FMD0/B05	RPLT/FMD0/B05	RPLT/FMD0/B05	RPLT/FMD05
107	FR/$\overline{\text{BLANK}}$[5]	---	---	---

TABLE 4-13 PIN MULTIPLEXING

PIN		ISA BUS	PI BUS	MICROCHANNEL
NO.	NAME			

NOTES:

1. Used to generated $\overline{\text{EBROM}}$ output. The BIOS memory address range is from the ISA bus, so the PI bus connection is not required.
2. The ISA Bus signals IOR and IOW are used to wake up the VGA.
3. Use depends upon configuration. Refer to description in Table 4-2.
4. These pins interface between the DAC and CRT. Use depends on application. Refer to the description in Table 4-8.
5. These pins are used for flat panel and external RAMDAC support. Refer to the description in Table 4-10.
6. These are clock generation interface pins and their usage is determined by a configuration bit (CNF3) and register PR15 bit 5. Refer to the description in Table 4-9.
7. These are system memory address signals. Refer to the description in Table 4-5.

TABLE 4-13 PIN MULTIPLEXING

4.12.1 Display Memory Pin Multiplexing

Display memory signal multiplexing depends on the number and type of external DRAMs used for the memory configuration. The following four configurations are listed in Table 4-14:

1. Configuration No. 1 supports four 256K x 4 DRAMs.
2. Configuration No. 2 supports one 256K x 16 DRAM.
3. Configuration No. 3 supports five 256K x 4 DRAMs.
4. Configuration No. 4 supports one 256K x 4 DRAM and one 256K x 16 DRAM.

PIN		DISPLAY MEMORY CONFIGURATION			
NO.	NAME	NO. 1	NO. 2	NO. 3	NO. 4
1-7, 9, 10	BMA[8:0]	BMA[8:0]	Not Used	FMA[8:0]	FMA[8:0]
11	$\overline{\text{BRAS}}$	$\overline{\text{BRAS}}$	Not Used	$\overline{\text{FRAS}}$	$\overline{\text{FRAS}}$
12	$\overline{\text{BWE}}$	$\overline{\text{BWE}}$	Not Used	$\overline{\text{WEU}}$	$\overline{\text{FWE}}$
87	LA20	See Note 1	See Note 1	FMD1	FMD1
88	LA21	See Note 1	See Note 1	FMD2	FMD2
89	LA22	See Note 1	See Note 1	FMD3	FMD3
91	$\overline{\text{RPLT}}$	See Note 2	See Note 2	FMD0	FMD0
104	ENDATA	See Note 3	See Note 3	$\overline{\text{FWE}}$	$\overline{\text{FCAS}}$
110-113, 115-118	AMD[7:0]	AMD[7:0]	MD[7:0]	MD[7:0]	MD[7:0]
119-122, 124-127	BMD[7:0]	BMD[7:0]	MD[15:8]	MD[15:8]	MD[15:8]
128	$\overline{\text{BCAS}}$	$\overline{\text{BCAS}}$	$\overline{\text{CASU}}$	$\overline{\text{FCAS}}$	$\overline{\text{CASU}}$
129	$\overline{\text{AOE}}$	$\overline{\text{AOE}}$	$\overline{\text{OE}}$	$\overline{\text{OE}}$	$\overline{\text{OE}}$
130-139	AMA[8:0]	AMA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
140	$\overline{\text{ARAS}}$	$\overline{\text{ARAS}}$	$\overline{\text{RAS}}$	$\overline{\text{RAS}}$	$\overline{\text{RAS}}$
141	$\overline{\text{AWE}}$	$\overline{\text{AWE}}$	$\overline{\text{WE}}$	$\overline{\text{WEL}}$	$\overline{\text{WE}}$
143	$\overline{\text{ACAS}}$	$\overline{\text{ACAS}}$	$\overline{\text{CASL}}$	$\overline{\text{CAS}}$	$\overline{\text{CASL}}$
144	$\overline{\text{BOE}}$	$\overline{\text{BOE}}$	Not Used	$\overline{\text{FOE}}$	$\overline{\text{FOE}}$

NOTE:

1. Used in host address bus or 12-bit TFT panel interface.
2. Used in external RAMDAC or color TFT panel interface.
3. Used in plasma, single panel color STN and TFT color interface.
4. Configurations 3 and 4 cannot be used in mixed supply voltage operations.
5. In configurations 3 and 4, names starting with the letter F are used in a separate 256K x 4 frame buffer interface.

TABLE 4-14 DISPLAY MEMORY PIN MULTIPLEXING

5.0 REGISTER DESCRIPTIONS

This section provides descriptions of the internal registers of the WD90C26A controller. These internal registers provide the VGA implementation as well as the functional equivalence of the Hercules, MDA, and CGA standards using the 6845 CRT Controller compatible register functions.

The VGA registers are described in detail followed by the Compatibility registers, PR registers, and Internal I/O registers used for Hercules, MDA, and CGA standard compatibility. For additional information on the use of VGA registers, compatibility registers, and internal I/O port registers refer to the reference documents listed in the Appendix A of this data sheet.

Unless stated otherwise, all bit graphic descriptions and definitions apply to VGA mode.

At reset, all PR register bits are initially set to 0 unless otherwise stated. Other registers in the WD90C26A are not specifically initialized at reset and should be considered undefined after reset.

The registers are presented in the following order:

- VGA General Registers
- VGA Sequencer Registers
- VGA CRT Controller Registers
- VGA Graphics Controller Registers
- VGA Attribute Controller Registers
- VGA RAMDAC Palette Registers
- Compatibility Registers
- Paradise (PR) Registers
- Internal I/O Port Registers

All VGA registers incorporated inside the WD90C26A are functionally equivalent to the VGA implementation.

Compatibility registers provide the additional register functions required for Hercules, MDA, and CGA hardware compatibility.

Paradise (PR) registers provide control functions beyond the basic VGA functions, which include support of Flat Panel displays. They are accessed using the existing Sequencer (3C5h), CRT Controller (3B5h), and Graphics Controller (3CFh) I/O registers. They use index values beyond those defined in VGA specifications for Sequencer, CRT, or Graphics Controller functions.

Internal I/O port registers are accessed in locations reserved for video system wakeup.

The following tables provide the I/O port addresses used to access the register locations of the WD90C26A controller.

WD90C26A REGISTER GROUPS	I/O PORT ADDRESSES USED
VGA General Registers	3BA 3DA 3CA 3C2 3CC
VGA Sequencer Registers	3C4 3C5
VGA CRTC Registers	3B4 3B5 3D4 3D5
VGA Graphics Controller Registers	3CE 3CF
VGA Attribute Controller Registers	3C0 3C1
Compatibility Registers	Various Addresses Required for Register-Level Compatibility associated with Hercules, MDA, and CGA Video Standards
PR Registers	Various indexed locations at Sequencer, Graphics Controller, and Attribute Controller I/O addresses.
Internal I/O Port Registers	46E8h for ISA mode, 3C3h for MicroChannel mode, 102 for both modes.

TABLE 5-1 WD90C26A REGISTER ADDRESS LOCATIONS

5.1 WD90C26A REGISTER SUMMARY

The following tables provide a summary of I/O address location, and index where appropriate, for each type of register previously listed.

NOTES

Reserved bits should be set to zero.

"?" Value is controlled by Bit 0 of the Miscellaneous Output Register.

"B" if Miscellaneous Output Register bit 0=0.

"D" if Miscellaneous Output Register bit 0=1.

5.1.1 VGA General Registers Information

REGISTER NAME	READ/ WRITE	PORT (HEX)		
		MONO	COLOR	EITHER
Miscellaneous Output	W			3C2h
Miscellaneous Output	R			3CCh
Input Status 0	R			3C2h
Input Status 1	R	3BAh	3DAh	
Feature Control	W	3BAh	3DAh	
Feature Control	R			3CAh

TABLE 5-2 VGA GENERAL REGISTERS SUMMARY

5.1.2 VGA Sequencer Registers Information

The WD90C26A controller's standard VGA implementation of sequencer registers requires that these registers be accessed by first writing the register index value to the sequencer index register at I/O address 3C4h. Next, the selected register is read or written by accessing I/O address 3C5h.

Writes to sequencer registers can be performed in a single 16-bit cycle where the upper byte (I/O address 3C4h) contains the sequencer register index and the lower byte (I/O address 3C5h) contains the value to be written to the desired register.

I/O REGISTERS	PORT (HEX)		
	MONO	COLOR	EITHER
Sequencer Index			3C4h
Sequencer Reset			3C5h.00h
Sequencer Clocking Mode			3C5h.01h
Sequencer Map Mask			3C5h.02h
Sequencer Character Map Select			3C5h.03h
Sequencer Memory Mode			3C5h.04h

TABLE 5-3 VGA SEQUENCER REGISTER SUMMARY

5.1.3 VGA CRT Controller Registers Information

Table 5-4 lists the WD90C26A controller's CRTC registers with their register names in VGA mode and their equivalent register name when the controller is operating in Hercules, MDA, or CGA compatibility modes. If a register name does not appear in the 6845 Compatibility Mode column, the register is accessible in VGA mode only. The selection of VGA mode or Compatibility mode access to the CRTC registers is controlled by PR2 register bit 6.

For flat panel support, certain bits of the CRTC registers are write-protected by the setting of the PR3 register.

VGA MODE REGISTER NAME	6845 COMPATIBILITY MODE REGISTER NAME	PORT (HEX)		
		MONO	COLOR	EITHER
Index Register	Index Address Register	3B4h	3D4h	
Horizontal Total	Horizontal Total	3B5.00h	3D5.00h	
Horizontal Display Enable End	Horizontal Display	3B5.01h	3D5.01h	
Start Horizontal Blanking		3B5.02h	3D5.02h	
End Horizontal Blanking		3B5.03h	3D5.03h	
Start Horizontal Retrace		3B5.04h	3D5.04h	
End Horizontal Retrace		3B5.05h	3D5.05h	
Vertical Total	Vertical Display	3B5.06h	3D5.06h	
Overflow Vertical		3B5.07h	3D5.07h	
Preset Row Scan		3B5.08h	3D5.08h	
Maximum Scan Line	Max. Scan Line	3B5.09h	3D5.09h	
Cursor Start	Cursor Start	3B5.0Ah	3D5.0Ah	
Cursor End	Cursor End	3B5.0Bh	3D5.0Bh	
Start Address High	Start Addr High	3B5.0Ch	3D5.0Ch	
Start Address Low	Start Addr Low	3B5.0Dh	3D5.0Dh	
Cursor Location High	Cursor Loc High	3B5.0Eh	3D5.0Eh	
Cursor Location Low	Cursor Loc Low	3B5.0Fh	3D5.0Fh	
Vertical Retrace Start	Light Pen Hi	3B5.10h	3D5.10h	
Vertical Retrace End	Light Pen Lo	3B5.11h	3D5.11h	
Vertical Display Enable End Low		3B5.12h	3D5.12h	
Offset		3B5.13h	3D5.13h	
Underline Location		3B5.14h	3D5.14h	
Start Vertical Blank		3B5.15h	3D5.15h	
End Vertical Blank		3B5.16h	3D5.16h	
CRT Mode Control		3B5.17h	3D5.17h	
Line Compare		3B5.18h	3D5.18h	

TABLE 5-4 VGA CRT CONTROLLER (CRTC) REGISTER SUMMARY

5.1.4 VGA Graphics Controller Registers (GCR) Information

I/O REGISTER NAME	PORT (HEX)		
	MONO	COLOR	EITHER
Graphics Controller Data Register			3CFh
Graphics Controller Index Register			3CEh
Set/Reset			3CF.00h
Enable Set/Reset			3CF.01h
Color Compare			3CF.02h
Data Rotate			3CF.03h
Read Map Select			3CF.04h
Graphics Mode			3CF.05h
Miscellaneous			3CF.06h
Color Don't Care			3CF.07h
Bit Mask			3CF.08h

TABLE 5-5 VGA GRAPHICS CONTROLLER REGISTER SUMMARY

5.1.5 VGA Attribute Controller Registers (ACR) Information

I/O REGISTER NAME	PORT (HEX)		
	MONO	COLOR	EITHER
Attribute Controller Data Register			3C0h
Attribute Controller Index Register			3C0h
Palette Register			3C0.00- 3C0.0F
Attribute Mode Control Register			3C0.10h
Overscan Color Register			3C0.11h
Color Plane Enable Register			3C0.12h
Horizontal PEL Panning Register			3C0.13h
Color Select Register			3C0.14h

TABLE 5-6 VGA ATTRIBUTE CONTROLLER REGISTER SUMMARY

5.1.6 VGA Internal RAMDAC Palette Registers Information

I/O REGISTER NAME	PORT (HEX)		
	MONO	COLOR	EITHER
RAM Write Address Register			3C8h
Palette RAM Read Address Register			3C7h
DAC Status Register			3C7h
Palette RAM Data Register			3C9h
RAMDAC Pixel Mask Register			3C6h

TABLE 5-7 VGA RAMDAC PALETTE REGISTER SUMMARY

5.1.7 Compatibility Registers Information

FUNCTIONS	MDA	CGA	AT&T	HERCULES
Mode Control Register	3B8h	3D8h	3D8h	3B8h
Color Select Register		3D9h	3D9h	
Status Register	3BAh	3DAh	3DAh	3BAh
Preset Light Pen Latch Register	3B9h	3DCh	3DCh	
Reset Light Pen Latch Register	3BBh	3DBh	3DBh	
M24 Register			3DEh	
Hercules Register				3BFh

TABLE 5-8 COMPATIBILITY REGISTERS SUMMARY

5.1.8 PR Registers Information

The Paradise Registers (PR) provide functions that are beyond the scope of standard VGA compatibility, and also provide control functions for the flat panel interface and additional features for which Western Digital/Paradise video solutions are known.

The PR registers are generally write-protected so that an unlocking sequence is required before the register contents can be modified. After they are unlocked, all of the register bits are readable and writable except where specifically noted otherwise. The PR registers are located in register locations unused in the IBM VGA standard.

REGISTER NAME	PORT (HEX)		
	MONO	COLOR	EITHER
PR0(A) Address Offset A Register			3CF.09h
PR0(B) Alternate Address Offset B Register			3CF.0Ah
PR1 Memory Size and Bus Interface Select Register			3CF.0Bh
PR2 Video Select Register			3CF.0Ch
PR3 CRT Lock Control Register			3CF.0Dh
PR4 Video Control Register			3CF.0Eh
PR5 Unlock Graphics Controller Extended Paradise Register			3CF.0Fh
PR10 Unlock (PR11through PR17) Register	3B5.29h	3D5.29h	
PR11 Configuration Bits Register	3B5.2Ah	3D5.2Ah	
PR12 Scratch Pad Register	3B5.2Bh	3D5.2Bh	
PR13 Interlace H/2 Start Register	3B5.2Ch	3D5.2Ch	
PR14 Interlace H/2 End Register	3B5.2Dh	3D5.2Dh	
PR15 Miscellaneous Control 1 Register	3B5.2Eh	3D5.2Eh	
PR16 Miscellaneous Control 2 Register	3B5.2Fh	3D5.2Fh	
PR17 Miscellaneous Control 3 Register	3B5.30h	3D5.30h	
PR18 Flat Panel Status Register	3B5.31h	3D5.31h	
PR19 Flat Panel Control I Register	3B5.32h	3D5.32h	
PR1A Flat Panel Control II Register	3B5.33h	3D5.33h	

TABLE 5-9 PARADISE REGISTER (PR) SUMMARY

REGISTER NAME	PORT (HEX)		
	MONO	COLOR	EITHER
PR1B Flat Panel Unlock Register	3B5.34h	3D5.34h	
PR20 Unlock Sequencer Extended Register			3C5.06h
PR21 Display Configuration Status & Scratch Pad Register			3C5.07h
PR30 Mapping RAM Unlock Register	3B5.35h	3D5.35h	
PR30A Memory Interface Write Buffer& FIFO Control Register			3C5.10h
PR31 System Interface Control Register			3C5.11h
PR32 Miscellaneous Control 4 Register			3C5.12h
PR33 Mapping RAM Address Counter Register	3B5.38h	3D5.38h	
PR34 Mapping RAM Data Register	3B5.39h	3D5.39h	
PR34A Video Memory Virtual Page Register			3C5.14h
PR35 Mapping RAM Control and Power Down Register	3B5.3Ah	3D5.3Ah	
PR36 LCD Panel Height Select Register	3B5.3Bh	3D5.3Bh	
PR37 Flat Panel Blinking Control Register	3B5.3Ch	3D5.3Ch	
PR39 Color LCD Control Register	3B5.3Eh	3D5.3Eh	
PR41 Vertical Expansion Initial Value Register	3B5.37h	3D5.37h	
PR44 Power-Down Memory Refresh Control Register	3B5.3Fh	3D5.3Fh	
PR45 Video Signature Analyzer Control Register			3C5.16h
PR45A Signature Analyzer Data Low			3C5.17h
PR45B Signature Analyzer Data High			3C5.18h
PR57 WD90C26A Feature Register I			3CF.10h
PR58 WD90C26A Feature Register II			3CF.11h
PR59 WD90C26A Operation Voltage and Memory Arbitration Cycle Setup Register			3CF.12h
PR62 FR Timing Register			3Cf.15h

TABLE 5-9 PARADISE REGISTER (PR) SUMMARY

NOTES

1. Registers PR0 through PR4, PR11 through PR17, and PR57 through PR61 are write-protected at power up by hardware reset. In order to load those registers, the appropriate Unlock register must be loaded first with binary xxxxx101; a register remains unlocked until any other value is written to its Unlock register.
2. Registers PR0 through PR5 are readable only if PR4(1)=0.
3. Registers PR10 through PR17 are read-protected at power up by hardware reset. In order to read those registers, PR10 must be loaded first with binary 1xxx0xxx; a register remains readable until any other value is written to PR10. Reading PR10 through PR17, if they are read-protected, returns data FFh. Setting PR4(1) to 1 does not read-protect registers PR10 through PR17.
4. All PR register bits are cleared to 0 at power up by hardware reset, except where otherwise noted.

5.1.9 Internal I/O Port Registers Information

I/O REGISTER NAME	PORT (HEX)		
	MONO	COLOR	EITHER
AT Mode I/O Port Register			46E8h 56E8h 66E8h 76E8h
MicroChannel Mode Register			03C3h
Setup Mode Video Enable Register			0102h

TABLE 5-10 INTERNAL I/O PORT REGISTER SUMMARY

5.2 VGA GENERAL REGISTERS

Refer to Table 5-2 for a summary of the VGA General Registers. Each VGA General Register is described in the following sections.

5.2.1 VGA Miscellaneous Output Register

Read Port = 3CCh, Write Port = 3C2h

Bit	FUNCTION
7	Vertical Sync Polarity Select
6	Horizontal Sync Polarity Select
5	Odd/Even Memory Page Select
4	Reserved
3	Clock Select 1
2	Clock Select 0
1	Enable Video RAM
0	I/O Address Select

Bit 7

Vertical Sync Polarity Selection

Determines whether the vertical sync pulse appearing at the VSYNC pin pulses high or low. This bit is typically used to signal VGA monitors to adjust their resolution.

0 = Positive vertical sync polarity; pulses high.
1 = Negative vertical sync polarity; pulses low.

NOTE

This ability to set vertical sync polarity is controlled by the setting of PR3 register bit 7 and PR39 register bit 2.

Bit 6

Horizontal Sync Polarity Selection

Determines whether the horizontal sync pulse appearing at the HSYNC pin pulses high or low.

0 = Positive horizontal sync polarity; pulses high.
1 = Negative horizontal sync polarity; pulses low.

NOTE

The ability to set horizontal sync polarity is affected by PR3 register bit 6 and by PR39 register bit 2.

Bit 5

Odd or Even Memory Page Select

In video modes 0 through 5, bit 5 selects which of the two 64 Kbyte pages of video memory is accessed.

0 = Lower 64 Kbyte page is selected.
1 = Upper 64 Kbyte page is selected.

Bit 4

Reserved in the WD90C26A. Should be set to '0' on writes to 3C2h.

Bit 3:2

Clock Select 1,0

Bits 2 and 3 of the miscellaneous output registers are used to select the video clock source used by the 90C26 to generate pixel data.

Selection of the video clock source is overridden if PR15 bit 4 is set, forcing the video clock source to be MCLK.

If AMD(3) is low at reset, bits 3 and 2 are used to select the video clock frequency from either the VCLK0, VCLK1, VCLK2 input pins.

If AMD(3) is high at reset, bits 3 and 2 are used to control an external video clock synthesizer or multiplexer.

NOTES

PR11 register bit 2 must be set to 0 in order to change the clock select bits.

If configured for separate VCLK0, 1, and 2 inputs, PR2 register bit 1 must be set to 0 in order to select the clock source.

For details on how bits 2 and 3 are used to control an external synthesizer or multiplexer, please refer to the information in Section 6 about Clock Interfacing.

Bit 3	Bit 2	FUNCTION
0	0	Selects VCLK0 for VGA applications. (Typically VCLK0=25.175 Mhz for 640 dots/line)
0	1	Selects VCLK1 for VGA applications. (Typically VCLK1=28.322 MHz for 720 dots/line in CRT-only modes)
1	0	Selects VCLK2 ("external clock" user defined input) if Config. Register bit 3 = 0
1	1	Reserved

Bit 1

System Processor Video RAM Access Enable. Allows video RAM to be accessed via the CPU interface.

0 = Disable CPU access of video memory
1 = Enable CPU access of video memory

Bit 0

CRT Controller I/O Address Range Selection. Selection for Monochrome (3B4 and 3B5), or Color (3D4 and 3D5) mode. Bit 0 also maps Input Status Register 1 at the MDA address (3BA) or CGA address (3DA).

0 = CRTC and input status addresses for Monochrome video standards (3B4, 3B5 and 3BA).
1 = CRTC and status addresses for color VGA/ CGA video standards (3D4, 3D5 and 3DA).

NOTE

When an I/O register address is given with a question mark for the center digit, it indicates that the digit could be a D or B depending upon the state of bit 0. If bit 0 is high, the addresses are 3D4, 3D5, and 3DA. If bit 0 is low, the addresses are 3B4, 3B5, and 3BA.

5.2.2 VGA Input Status Register 0

Read Only Port = 3C2h

BIT	FUNCTION
7	CRT Interrupt
6:5	Reserved
4	Monitor Detect Bit for Color/ Monochrome Display
3:0	Reserved

Bit 7

CRT Vertical Retrace Interrupt Pending or Cleared

This bit may be read to determine when a vertical sync pulse has occurred and with input status register 1 bits 3 and 0 is useful for timing updates to occur during refresh.

0 = Vertical retrace interrupt cleared.
1 = Vertical retrace interrupt pending.

Bit 6:5

Reserved

Returns 00 on reads of Input Status Register 0.

Bit 4

Monitor Detection in VGA Mode

When V_{REF} is at its reference voltage level, this bit (4) indicates the status from an internal monitor detection circuit. This indication is valid only when video data is being actively displayed. Refer to "CRT Interface" in Section 6.11 for details of this function.

0 = No monitor attached
1 = Monitor attached.

When V_{REF} (pin 72) is grounded, this bit is set to the inverse of the level at pin 71, the $\overline{MDET}$ input.

0 = Pin 71 ($\overline{MDET}$) input high.
1 = Pin 71 ($\overline{MDET}$) input active low.

Bit 3:0

Reserved

Returns 0000 on reads of Input Status Register 0.

NOTE

PR4 register bit 0 must be set to 0 for these bits to read 0000.

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5.2.3 VGA Input Status Register 1

Read Only Port = 3?Ah

BIT	FUNCTION
7:6	Reserved
5	Diagnostic 0
4	Diagnostic 1
3	Vertical Retrace
2	Reserved
0	Display Enable Status

Bit 7:6

Reserved

Returns 00 on reads of Input Status Register 1.

Bit 5:4

Color Plane Diagnostics

These bits allow the reading of two out of eight colors of a color plane. Selection of which colors from the plane are read is controlled by activating the Attribute Controller's Color Plane Enable Register bits 4 and 5. The 8 bits of the color plane are designated VID (7:0). These bits represent the 8 bits of input to the internal RAMDAC.

COLOR PLANE ENABLE REGISTER SETTING		INPUT STATUS REGISTER 1 DATA	
Bit 5	Bit 4	Bit 5	Bit 4
Bit 0	Bit 0	VID2 (Red)	VID0 (Blue)
Bit 0	Bit1	VID5 (I. Blue)	VID4 (Green)
Bit 1	Bit 0	VID3 (I. Red)	VID1 (I. Green)
Bit 1	Bit 1	VID7	VID6

Bit 3

Vertical Retrace Status

Used along with bit 0 and Input Status Register bit 7 to time screen updates.

0 = Vertical frame is displayed.
1 = Vertical retrace is active.

Bits 2:1

Reserved

Returns 00 on reads of Input Status Register 1.

Bit 0

Display Enable Status

Used along with bit 3 and input status register 0 to synchronize screen updates.

0 = CRT screen display in process.
1 = CRT screen display disabled for horizontal or vertical retrace interval.

5.2.4 VGA Feature Control Register

Read Port = 3CAh, Write Port = 3?Ah

BIT	FUNCTION
7:4	Reserved
3	Vertical Sync Control
2:0	Reserved

Bits 7:4

Reserved

Should be set to 0000 on writes to the Feature Control Register. Returns 0000 on reads of the Feature Control Register.

Bit 3

Vertical Sync Control

0 = VSYNC output enabled
1 = VSYNC output is logical "OR" of VSYNC and Vertical Display Enable.

NOTE

For the VSYNC signal to appear at the VSYNC pin, PR39 register bit 2 must be set to 1.

Bit 2:0

Reserved

No hardware function is defined on writes to the VGA Feature Control Register. Bit 2 is 0 on reads of the register. Bits 0 and 1 are read/write.

5.3 VGA SEQUENCER REGISTERS

Refer to Section 5.1 for a summary of VGA Sequencer Registers and all registers described in this book.

NOTE

VGA Sequencer Registers are accessible only in VGA mode.

5.3.1 VGA Sequencer Index Register

Read/Write Port = 3C4h

BIT	FUNCTION
7:6	
5:0	Sequencer Address/Index Bits

Bits 7:6

Reserved.
Returns 00 on reads. No function is defined on writes.

Bit 5:0

Sequencer Register Bank/Index

The Sequencer Index Register is written with the index value (00h- 04h) of the Sequencer register to be accessed. Certain PR Registers are also accessed by using the sequencer register bank index 3C4 and read/write port 3C5h.

NOTE

Bite 5:2 are undefined on reads of the Sequencer Index Register unless the Extended Sequencer Registers are unlocked. Refer to the description of PR20 for additional information.

5.3.2 VGA Sequencer Reset Register

Read/Write Port = 3C5h, Index = 00h

BIT	FUNCTION
7:2	Reserved
1	Synchronous Reset
0	Asynchronous Reset

Bit 7:2

Reserved

Returns 0s on reads of the Sequencer Reset Register. No function is defined on writes.

Bit 1

Synchronous Reset

0 = Sequencer is cleared and halted synchronously, thereby preserving the memory contents.
1 = Operational mode (if bit 0=1).

A synchronous reset must be performed before the clocking mode register is modified.

Bit 0

Asynchronous Reset

0 = Sequencer is cleared and halted asynchronously.
1 = Operational mode (if bit 1 = 1).

If operating in VGA mode, bit 0 is a synchronous reset with the same function as bit 1.

5.3.3 VGA Clocking Mode Register

Read/Write Port = 3C5h, Index = 01h

BIT	FUNCTION
7:6	Reserved
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load
1	Reserved
0	8/9 Dot Clock

Bits 7:6

Reserved

Returns 00 on reads. No function is defined on writes.

Bit 5

Screen Off

When set to '1', video data I/O, the CRT and/or LCD is shut off.

0 = Normal screen operation.
1 = Screen turned off. CRT and panel sync signals remain active. This bit may be used for quick full screen updates.

Bit 4

Video Serial Shift Register Loading

0 = Video serial shift registers are loaded according to the bit 2 setting.
1 = Serial shift registers loaded every 4th character clock (32 bit fetches).

Bit 3

Dot Clock Selection

0 = Dot clock is the selected VCLK frequency.
1 = Dot clock is the selected VCLK frequency divided by 2 (used for 320/360 pixel screen widths).

NOTE

The setting of Clocking Mode register bit 3 is overridden when PR2 register bit 0 is set to 1.

Bit 2

Shift Load

(Effective only if bit 4 = 0).

0 = Video serial shift registers are loaded every character clock.
1 = Video serial shift registers are loaded every other character clock.

Bit 1

Reserved

This bit is returns a 0 on reads and may be set to '0' or '1' on writes without affecting the register function. In EGA emulation, this bit would normally control 2 out of 5 memory cycle bandwidth selection. This function is not required in the Clocking Mode Register as a similar function exists in the CRTC Horizontal Retrace End Register.

Bit 0

8/9 Dot Clock

Controls whether sequencer generates 8 or 9 dot wide character clock, thereby causing single characters to be 8 or 9 dots wide.

0 = 9 dot wide character clock.
1 = 8 dot wide character clock.

Typically this bit is set to '1' for support of most flat panels. This setting may be modified by the settings of PR2 bits 3 and 4 and PR11 bit 0.

5.3.4 VGA Map Mask Register

Read/Write Port 3C5h, Index = 02h

BIT	FUNCTION
7:4	Reserved
3	Map 3 Enable
2	Map 2 Enable
1	Map 1 Enable
0	Map 0 Enable

Bit 7:4

Reserved

Returns 0000 on reads from the Map Mask register. No function is defined on writes.

Bit 3:0

Map Enable

Controls writing to memory maps (0 through 3) respectively.

0 = Writing to indicated maps disallowed.
1 = Writing to indicated maps enabled.

5.3.5 VGA Character Map Select Register

Read/Write Port= 3C5h, Index = 03h

BIT	FUNCTION
7:6	Reserved
5	Character map Select A Bit 2
4	Character map Select B Bit 2
3	Character map Select A Bit 1
2	Character map Select A Bit 0
1	Character map Select B Bit 1
0	Character map Select B Bit 0

If Sequencer Register 4 bit 1 is 1, then the attribute byte bit 3 in text modes is redefined to control switching between character sets.

A '0' selects character map B.
A '1' selects character map A.

Character Map selection from either plane 2 or plane 3 is determined by PR2(2), PR2(5) and bit 4 of the attribute code.

Bit 7:6

Reserved

Returns 00 on reads of the Character Map Select Register. No function is defined on writes.

Bit 5

Character Map select A MSB

The Most Significant Bit (MSB) of character map A, along with bits 3 and 2, select the location of character map A as listed in the following table.

BITS 5,3,2	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
000	0	1st 8 Kbyte
001	1	3rd 8 Kbyte
010	2	5th 8 Kbyte
011	3	7th 8 Kbyte
100	4	2nd 8 Kbyte
101	5	4th 8 Kbyte
110	6	6th 8 Kbyte
111	7	8th 8 Kbyte

Bit 4

Character Map select B MSB.

The MSB of character map B, along with bits 1 and 0, selects the location of character map B as shown below.

BITS 4,1,0	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
000	0	1st 8 Kbyte
001	1	3rd 8 Kbyte
010	2	5th 8 Kbyte
011	3	7th 8 Kbyte
100	4	2nd 8 Kbyte
101	5	4th 8 Kbyte
110	6	6th 8 Kbyte
111	7	8th 8 Kbyte

Bit 3:2

Character Map Select A MID and LSB
See description of bit 5.

Bit 1:0

Character Map Select B MID and LSB
See description of bit 4.

5.3.6 VGA Memory Mode Register

Read/Write Port= 3C5h, Index = 04h

BIT	FUNCTION
7:4	Reserved
3	Chain 4 mode
2	Odd/Even mode
1	Extended Memory
0	Reserved

Bit 7:4

Reserved

Returns 0000 on reads of the Memory Mode Register. No function is defined on writes.

Bit 3

Chain 4 mode selections

0 = Processor sequentially accesses data using the map mask register.
1 = Chain 4 mode. Causes CPU video memory access to be organized around four chained maps, with the two lower order video memory address pins (MA0, MA1) selecting the map to be addressed. The map selections are listed in the following table:

MA1	MA0	MAP SELECTED
0	0	0
0	1	1
1	0	2
1	1	3

NOTE

An MA address designation indicates at video memory address prior to RAS/CAS address multiplexing.

Bit 2

Odd/Even Mode Selection

0 = Causes CPU accesses at even system addresses to access maps 0 and 2. CPU accesses at odd processor addresses to access maps 1 and 3.
1 = Causes CPU accesses to be to sequential accesses as defined by map mask register.

Bit 1

Extended Video Memory

0 = 64 Kbyte of video memory.
1 = Greater than 64 Kbyte of memory for VGA modes.

Bit 0

Reserved

Returns 00 on reads of the Memory Mode Register. No function is defined on writes.

5.3.7 VGA Sequencer Index Register

Read/Write Port = 3C5h, Index = 05h

This register exists for IBM VGA compatibility. It has no other function.

BIT	FUNCTION
7:4	Unused
3:0	Reserved

Bits 7:4

Unused.

Returns 0000 on reads of the Sequencer Index Register. No function is defined on writes.

Bits 3:0

Reserved

Returns 1111 on reads of the Sequencer Index Register. No function is defined on writes.

5.4 CRT CONTROLLER REGISTERS

Refer to the introduction in Section 5.1 for a summary of CRT Controller Registers.

5.4.1 CRTC Index Register

Read/Write Port = 3?4h

BIT	FUNCTION
7:5	Reserved
4:0	Index bits

Bit 7:5

Unused

Returns 000 on reads of the CRTC Index Register. Should be set to 000 on writes.

Bit 4:0

Index Register Bits

CRT Controller Index pointer bits to specify the register to be addressed. Its value is programmed in hex.

5.4.2 CRTC Horizontal Total Register

Read/Write Port = 3?5h, Index = 00h

To unlock, set PR3 register bit 5 and CRTC Vertical Retrace End Register bit 7 both to 0.

BIT	FUNCTION
7:0	Horizontal Total

Bit 7:0

Horizontal Total

In VGA mode, the horizontal total is the total character count including retrace time less 5, per horizontal scan line.

Bits 7:0 are shadowed.

5.4.3 CRTC Horizontal Display Enable End Register

Read/Write Port = 3?5h, Index = 01h.

To unlock, set PR3 register bit 5 and CRTC Vertical Retrace End Register bit 7 both to 0.

BIT	FUNCTION
7:0	Horizontal Display Enable End

Bit 7:0

Horizontal Display Enable End

The total displayed characters less one are programmed in this register. This register is locked if PR3 register bit 5 or the vertical retrace end register bit 7 are set to 1.

5.4.4 CRTC Start Horizontal Blanking Register

Read/Write Port = 3?5h, Index = 02h.

To unlock, set PR3 register bit 5 and CRTC Vertical Retrace End Register bit 7 both to 0.

BIT	FUNCTION
7:0	Start Horizontal Blanking

Horizontal blanking when the horizontal character counter reaches this character clock value. This register is locked if the PR Register PR3(5) = 1 or the Vertical Retrace End Register bit 7 = 1.

Bits 7:0 are shadowed.

5.4.5 CRTC End Horizontal Blanking Register

Read/Write Port = 3?5h, Index = 03h.

To unlock, set PR3 register bit 5 and CRTC Vertical Retrace End Register bit 7 both to 0.

BIT	FUNCTION
7	Reserved
6:5	Display Enable Signal Skew Control
4:0	End Horizontal Blanking (lower 5 bits)

This register is locked if the PR Register PR3(5) = 1 *or* the Vertical Retrace End Register bit 7 = 1.

Bit 7

Reserved

Returns 0 on reads of the End Horizontal Blanking Register. No function is defined on writes.

Bits 6:5

Display Enable Signal Skew Control

These bits define the display enable signal skew time in relation to horizontal synchronization pulses.

The skew values are listed below.

BIT 6	BIT 5	DISPLAY ENABLE SKEW IN CHARACTER CLOCKS
0	0	0
0	1	1
1	0	2
1	1	3
Bits 5 and 6 are shadowed.		

Bit 4:0

End Horizontal Blank

Start blanking register plus the width of the horizontal blank in character clocks. The least significant five bits are programmed in this register, while the most significant bit is the End Horizontal Retrace Register (Index 05h) bit 7. When the least significant five bits of the horizontal character counter matches these six bits, the horizontal blanking is ended.

Bits 4:0 are shadowed.

5.4.6 CRTC Start Horizontal Retrace Register

Read/Write Port = 3?5h, Index = 04h.

To unlock, set PR3 register bit 5 and CRTC Vertical Retrace End Register bit 7 both to 0.

BIT	FUNCTION
7:0	Start Horizontal Retrace Character Count

Bit 7:0

Start Horizontal Retrace Character Count

Hex value in character count at which horizontal retrace output pulse becomes active. This register

is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register bit 7 = 1.

Bits 7:0 are shadowed.

5.4.7 CRTC End Horizontal Retrace Register

Read/Write Port = 3?5h, Index = 05h.

To unlock, set PR3 register bit 5 and CRTC Vertical Retrace End Register bit 7 both to 0.

BIT	FUNCTION
7	End Horizontal Blank bit 6
6:5	Horizontal Retrace Delay
4:0	End Horizontal Retrace

This register is locked if the PR Reg. PR3 (5) = 1 *or* the Vertical Retrace End Reg. bit 7 = 1.

Bit 7

MSB (Sixth) Of End Horizontal Blanking Register

Bit 7 is shadowed.

Bit 6:5

Horizontal Retrace Delay

These bits define horizontal retrace signal delay.

Refer to the following table for details:

BIT 6	BIT 5	CHARACTER CLOCK DELAYS
0	0	0
0	1	1
1	0	2
1	1	3
Bits 5 and 6 are shadowed.		

Bit 4:0

End Horizontal Retrace

Start retrace register value is added to the width of the horizontal retrace in character clock count. The least significant five bits are programmed in this register. When the least significant five bits of the Horizontal Character Counter matches these five bits, the horizontal retrace signal is turned off.

Bits 4:0 are shadowed.

5.4.8 CRTC Vertical Total Register

Read/Write Port = 3?5h, Index = 06h.

To unlock, set PR3 register bit 0 and CRTC Vertical Retrace End Register bit 7 both to 0.

BIT	FUNCTION
7:0	Vertical Total Scan Lines

Bit 7:0

Raster Scan Line Total Less 2

The least significant eight bits of a 11-bit count of raster scan lines for a display frame. The loaded value includes vertical total scan lines minus 2. Time for vertical retrace, and vertical sync are also included. Bit 8 and bit 9 of this count are loaded into the Vertical Overflow Register (index = 07h) bit 0 and bit 5 respectively. Bit 10 of this count is in the 3?5, index 3E, bit 0.

In 6845 modes, total vertical display time in rows is programmed into bit 6:0, while bit 7 is reserved. Scan count reduction is not necessary. (The number of scan lines in a row is determined by the maximum Scan Line Register (index 09hbits 4:0). This register is locked if PR Register PR3 (0)=1 or Vertical Retrace End Register bit 7=1.

Bits 7:0 are shadowed.

5.4.9 CRTC Overflow Vertical Register

Read/Write Port = 3?5h, Index - 07h.

To unlock, refer to the individual bit descriptions.

BIT	FUNCTION
7	Vertical Retrace Start Bit 9
6	Vertical Display Enable End Bit 9
5	Vertical Total Bit 9
4	Line Compare Bit 8
3	Start Vertical Blank Bit 8
2	Vertical Retrace Start Bit 8
1	Vertical display Enable End Bit 8
0	Vertical Total Bit 8

Bit 7[1]

Vertical Retrace Start Bit 9 (index = 10h).

Bit 7 is shadowed.

Bit 6[2]

Vertical Display Enable End Bit 9.

The Vertical Display Enable End register count bit 9, which is appended, along with bit 1 of this register, to the CRTC Vertical Display Enable End register at index 12h to provide a 10-bit Vertical Display Enable End count.

Bit 5[1]

Vertical Total Bit 9.

The Vertical Total register count value bit 9, which is appended, along with bit 0 of this register, to the value in the CRTC Vertical Total register at index 06h to provide a 10-bit Vertical Total count.

Bit 5 is shadowed.

Bit 4

Line Compare Bit 8.

The Line Compare count value bit 8, which is appended, along with bit 6 of the CRTC Maximum Scan Line register, to the CRTC Line Compare register at index 18h to provide a 10-bit line compare value.

Bit 3[1]

Start Vertical Blank Bit 8.

The Start Vertical Blank count value bit 8, which is appended, along with bit 5 of the CRTC Maximum Scan LIne register, to the CRTC Vertical Blanking register at index 15h to provide a 10-bit Vertical Blank Count value.

Bit 3 is shadowed.

Bit 2[1]

Vertical Retrace Start Bit 8.

The Vertical Retrace Start count value bit 8, which is appended to the CRTC Vertical Retrace register at index 10h to provide a 9-bit Vertical Retrace Start value.

Bit 2 is shadowed.

Bit 1[2]

Vertical Display Enable End Bit 8.

The Vertical Display Enable End register count bit 8, which is appended, along with bit 6 of this register, to the CRTC Vertical Display Enable End register at index 12h to provide a 10-bit Vertical Display Enable End count.

Bit 0[1]

Vertical Total Bit 8

The Vertical Total register count value bit 8, which is appended, along with bit 5 of this register, to the value in the CRTC Vertical Total register at index 06h to provide a 10-bit Vertical Total count.The Vertical Total register count value bit 8, which is appended to the value in the CRTC Vertical Total register at index 06h.

Bit 0 is shadowed.

NOTES

1. This register is locked if PR3 register bit 0 is set to 1 or the Vertical Retrace End register bit 7 is set to 1.
2. This register is locked if PR3 register bit 1 is set to 0 and the Vertical Retrace End register bit 7 is set to 1.

5.4.10 CRTC Preset Row Scan Register

Read/Write Port = 3?5h, Index = 08h

BIT	FUNCTION
7	Reserved
6,5	Byte Panning Control
4:0	Preset Row Scan Count

Bit 7

Reserved

Returns 0 on reads of the Preset Row Scan Register. No function is defined on writes.

Bit 6:5

Byte Panning Control

These bits allow up to 3 bytes to be panned in modes programmed as multiple shift modes.

BIT 6	BIT 5	OPERATION
0	0	Normal
0	1	1 byte left shift
1	0	2 bytes left shift
1	1	3 bytes left shift

Bit 4:0

Preset Row Scan Count

These bits preset the vertical row scan address counter once after each vertical retrace, which allows the first row of character cells to begin on any scan line. This counter is incremented after each horizontal retrace period until the maximum row scan count is reached. For all subsequent rows, the row scan address count begins at 0. This register can be used for smooth vertical scrolling of text.

5.4.11 CRTC Maximum Scan Line Register

Read/Write Port = 3?5h, Index 09h.

Bit 5 is lockable; refer to the bit 5 description.

BIT	FUNCTION
7	200 to 400 Line Conversion
6	Line Compare bit 9
5	Start Vertical Blank bit 9
4:0	Maximum Scan Line

Bit 7

200 to 400 Line Conversion.

0 = Normal operation.
1 = Activate line doubling. The row scan (row address) counter is incremented every other horizontal scan instead of every horizontal scan, which allows 200-line modes to display 400 scan lines (each line is double scanned).

Bit 6

Line Compare.

This is the Most Significant Bit (MSB) of the 10-bit Line Compare count, which is formed by the CRTC Line Compare register at index 18h, bit 8 from the Line Compare Count from the CRTC Overflow register bit 4 (index 07h), and this bit.

Bit 5

Start Vertical Blank

This is bit 9 of the 10-bit Start Vertical Blank count, which is formed by formed by the CRTC Start Vertical Blank register at index 15h, bit 3 of the CRTC Overflow Vertical register at 07h, and this bit. Bit 5 is locked if either PR3 register bit 0 or 3?5.11h register bit 7 is set to 1.

Bit 4:0

Maximum Scan Line

Maximum number of scanned lines for each row of characters. The value programmed is the maximum row scan address, which is the number of scanned rows per character minus 1. In 6845 mode (PR2 register bit 2 is set to 1), bits 7:5 are reserved, and bits 4:0 are programmed with the maximum scan line count, less 1 for non-interlaced modes.

NOTE

In simultaneous display, interlaced modes are not supported by the WD90C26A controller.

5.4.12 CRTC Cursor Start Register

Read/Write Port = 3?5h, Index = 0Ah

BIT	FUNCTION
7:6	Reserved
5	Cursor Control
4:0	Cursor Start Scan Line

Bit 7:6

Reserved

Returns 00 on reads of the Cursor Start Register. No function is defined on writes.

Bit 5

Cursor Control

Turns text cursor on or off.

0 = Cursor Off
1 = Cursor On

Bit 4:0

These bits specify the first raster scan line, or the row scan address where the text cursor begins within the character box. The first raster of a character box is at row scan address 0. If this value is programmed with a value greater than the CRTC Cursor End Register (index = 0Bh), no cursor text is generated.

5.4.13 CRTC Cursor End Register

Read/Write Port= 3?5h, Index= 0Bh

BIT	FUNCTION
7	Reserved
6:5	Cursor Skew
4:0	Cursor End Scan Line

Bit 7

Reserved

Returns 0 on reads of the Cursor End Register. No function is defined on writes.

Bit 6:5

Cursor Skew Bits

Delays the displayed cursor to the right by the skew value in character clocks, for example, 1 character clock skew moves the cursor right by 1 character cell on the screen. Cursor skew is selected according to the information listed in the following table.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4:0

Cursor End Scan Line.

These bits specify the last raster scan line or row scan address within the character box during which the cursor is active. If this row scan address is less than the cursor start row address, no cursor is displayed.

5.4.14 CRTC Start Address High Register

Read/Write Port= 3?5h, Index = 0Ch

BIT	FUNCTION
7:0	Start Address High Byte

Bit 7:0

Upper byte of Display Screen Start Address

These are the eight high order bits of the 16 bit video memory start, from which the screen is refreshed. The low order eight bits of the Display Screen Start address are taken from the CRTC Start Address Low register at index 0Dh.

In non-6845 modes (PR2 register bit 6 is set to 0), PR3 bits 3 and 4 extend the video memory start address range to 18 bits.

In 6845 modes (PR2 register bit 6 is set to 0), bits 6 and 7 of this register are ignored and the video memory start address is a 14-bit value.

5.4.15 CRTC Start Address Low Register

Read/Write Port = 3?5, Index = 0Dh

BIT	FUNCTION
7:0	Start Address Low Byte

Bit 7:0

Lower byte of Display Screen Start Address

5.4.16 CRTC Cursor Location High Register

Read/Write Port= 3?5h, Index= 0Eh

BIT	FUNCTION
7:0	Cursor Location High Byte

Bit 7:0

Upper byte bits of the Cursor Location address.

These are the eight higher order bits of the 16 bit cursor location address. In VGA mode, the PR Register PR3 bits 3 and 4 extend the cursor location High Register to 18 bits. In 6845 modes, bits 6 and 7 are forced, too.

5.4.17 CRTC Cursor Location Low Register

Read/Write Port= 3?5h, Index = 0Fh

BIT	FUNCTION
7:0	Cursor Location Low Byte

Bit 7:0

Lower byte of the Cursor Location Address

The lower order eight bits of the 16 bit video memory address.

5.4.18 CRTC Vertical Retrace Start/Light Pen High Register

Read/Write Port = 3?5h, Index = 10h

BIT	FUNCTION
7:0	Vertical Retrace Start

Bit 7:0

Vertical Retrace Start Pulse

These are the lower eight bits of the 10-bit vertical retrace start register. Bits 8 and 9 are located in the Overflow Register (index = 07h). In 6845 compatible mode, this register shows the six low order bits in positions 5:0 as the high byte of the light pen read-back value. Bits 6 and 7 are reserved. The lower order eight bits of the light pen read-back register are at index 11h. This register is locked if PR register PR3 (0)=1.

Bits 7:0 are shadowed.

5.4.19 CRTC Vertical Retrace End/Light Pen Low Register

Read/Write Port = 3?5h, Index = 11h

BIT	FUNCTION
7	CRTC 0-7 Write Protect
6	Select 3/5 DRAM Refresh
5	Enable Vertical Interrupt
4	Clear Vertical Interrupt
3:0	Vertical Retrace End

In 6845-compatible mode, bits 7:0 are the low bye of the light pen location. Otherwise bits are defined as follows.

Bit 7

CRTC Registers Write Protect

0 = Enables writes to CRT index registers 00h - 07h.
1 = Write protects CRT Controller index registers in the range of index 00h - 07h. The line compare bit 4 in the Overflow Register (07h) is not protected.

Bit 6

DRAM Refresh/Horizontal Scan Line

This bit select DRAM refresh cycles per horizontal scan line.

0 = Generates 3 refresh cycles for each horizontal scan line for normal VGA operation.
1 = Generates 5 DRAM refresh cycles per horizontal scan line.

NOTE

This bit setting can be overridden by PR19 [1:0].

Bit 5

The Enable Vertical Retrace Interrupt signal causes vertical retrace to trigger an interrupt request by activating the IRQ (or $\overline{IRQ}$ in MicroChannel mode) signal.

0 = Enables vertical retrace interrupt.
1 = Disable vertical retrace interrupt.

Bit 4

Clear Vertical Retrace Interrupt

0 = Clears vertical retrace interrupt by resetting (re-enable) an internal interrupt capture latch.
1 = Vertical retrace interrupt. Allows an interrupt to be generated after the last displayed scan of the frame has occurred (i.e. the start of the bottom border).

Bit 3:0

Vertical Retrace End

This is the row scan count at which vertical sync becomes inactive. For a desired retrace signal pulse width "W", add the scan count for "W" to the value programmed in the Vertical Retrace Start Register. Use the low order 4 bits of this result as the value to program-in the vertical retrace and register.

Bits 3:0 are shadowed.

5.4.20 CRTC Vertical Display Enable End Register

Read/Write Port = 3?5h, Index = 12h

BIT	FUNCTION
7:0	Vertical Display Enable End

Bit 7:0

These are the eight lower bits of the 10-bit Vertical Display Enable End register.

These bits define where the active display data ends. The programmed value is in number of scan lines minus 1. Bits 8 and 9 of the Vertical Display Enable End register are in the Overflow Register (index 07h) at bit 1 and 6 respectively.

5.4.21 CRTC Offset Register

Read/Write Port = 3?5h, Index 13h

BIT	FUNCTION
7:0	Logical Line Screen width

Bit 7:0

Logical Line Screen Width

This register specifies the width of display memory in terms of an offset from the current row start address to the next character row. The offset value is a word address adjusted for word or double word display memory access. It is calculated as follows:

Next Row Scan Start Address = Current Row scan Start Address + (K * Value in Offset Register)

where K=2 in byte mode and K=4 in word mode.

5.4.22 CRTC Underline Location Register

Read/Write Port = 3?5h, Index = 14h

BIT	FUNCTION
7	Reserved
6	Doubleword Mode
5	Count by 4
4:0	Underline Location

Bit 7

Reserved

Returns 0 on reads of the Underline Location Register. No function is defined on writes.

Bit 6

Doubleword Mode

0 = Display memory addressed for byte or word access.
1 = Display memory addressed for double word access.

Bit 5

Count by 4 for Doubleword Access

0 = Memory address counter is clocked for byte or word access. See CRT Mode Control register bit 6.
1 = Memory address counter is clocked for doubleword access at the character clock rate divided by 4.

Bit 4:0

Underline Location

These bits specify the row scan address within a character matrix where underlines are to be displayed. A value of 1 less than the desired number of scan lines at which the underline appears should be loaded.

5.4.23 CRTC Start Vertical Blank Register

Read/Write Port = 3?5h, Index = 15h

This register is locked if PR3 (0)=1.

BIT	FUNCTION
7:0	Start Vertical Blank (lower eight bits)

Bit 7:0

Start Vertical Blank Lower Eight Bits

These are the lower eight bits of the 10-bit Start Vertical Blank Address Register. Bit 8 is in the Overflow Register (index = 07h) and bit 9 is in the Maximum Scan Line Register (index = 09h). The 10-bit value programmed in this register should be less than the desired number of scan lines where the vertical blanking signal should start.

Bits 7:0 are shadowed.

5.4.24 CRTC End Vertical Blank Register

Read/Write Port = 3?5h, Index = 16h

This register is locked if PR Register PR3 (0)=1.

BIT	FUNCTION
7:0	End Vertical Blank

Bit 7:0

Vertical Blank Inactive Count

End Vertical is an 8-bit value calculated as follows:

8-bit End Vertical Blank value = (value of Start Vertical Blank minus 1) + (value of Vertical Blank signal width in scan lines).

Bits 7:0 are shadowed.

5.4.25 CRTC Mode Control Register

Read/Write Port = 3?5h, Index = 17h

This register is locked if PR Register PR3 (5)=1.

BIT	FUNCTION
7	Hardware Reset
6	Word or Byte Mode
5	Address Wrap
4	Reserved
3	Count by 2
2	Horizontal Retrace Select
1	Select Row Scan Counter
0	CGA Compatibility

Bit 7

Hardware Reset

0 = Horizontal and vertical retrace outputs to be inactive.
1 = Horizontal and vertical retrace outputs enabled.

Does not affect panel sync signals.

Bit 6

Word Or Byte Mode

0 = Word address mode. All memory address counter bits are shifted down by 1 bit before becoming the video memory address. The MSB of the address counter appears in the LSB. Refer to the description of memory organization given with PR1 in Section 5.9.2.
1 = Byte address mode.

Bit 5

Address Wrap

0 = This bit enables A13 of the CRTC video memory address counter to appear as the LSB of the video memory address whenever the WD90C26A is in word address mode. Otherwise, A 0 appears as the video memory address LSB.

1 = Select A15 of the CRTC video memory address counter to appear as the LSB of the video memory address to external DRAM. Used for odd/even mode when 256 Kbyte of video memory is used on the system board.

Bit 4

Reserved

Returns 0 on reads of the Mode Control Register. No function is defined on writes.

Bit 3

Count by 2

0 = Character clock increments the CRTC video memory address counter.

1 = Character clock divided by 2 increments the CRTC video memory address counter.

Bit 2

Horizontal Retrace Clock Rate Select for Vertical Timing Counter

0 = Selects horizontal retrace clock rate

1 = Selects horizontal retrace clock rate divided by 2.

Bit 1

Select Row Scan Counter

0 = Selects character row scan counter address bit 1 as output as A14 address signal to external DRAM.

1 = Selects A14 of the CRTC video memory address counter as the A14 video memory address to external DRAM.

Bit 0

6845 CRT Controller compatibility mode support for CGA operation.

0 = Row scan address bit 0 is substituted for memory address bit 13 video memory address output during active display time.

1 = Enable CRT address counter bit 13 to be output as bit 13 of video memory address.

5.4.26 CRTC Line Compare Register

Read/Write Port = 3?5h, Index = 18h

BIT	FUNCTION
7:0	Line Compare (lower eight bits)

Bit 7:0

Line Compare Lower Eight Bits

Lower eight bits of the 10-bit Scan Line Compare Register. Bit 8 is in the Overflow Register (index = 07h) and bit 9 is in the Maximum Scan Line Register (index = 09h). When the vertical counter reaches this value, the internal start of the line counter is cleared.

5.5 GRAPHICS CONTROLLER REGISTERS

Refer to Section 5.1 for an summary of Graphics Controller Registers (GCR).

Read/Write Port = 3CEh

BIT	FUNCTION
7:0	Graphics Index Bits

Bit 7:0

Graphics Controller Register Index Pointer Bits

NOTE

Some PR registers reside at the Graphics Controller I/O address, at indices beyond those defined for VGA Graphics Controller registers.

5.5.1 GCR Set/Reset Register

Read/Write Port = 3CFh, Index = 00h

BIT	FUNCTION
7:4	Reserved
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bit 7:4

Reserved

Returns 0000 on reads of the Set/Reset Register. No function is defined on writes.

Bit 3:0

Set/Reset Map

When the CPU executes display memory write with Write Mode 0 selected and the Enable Set/Reset Register (index = 01h) activated, the eight bits of the bit value, which have been operated on by the Bit Mask Register (index =08h), are then written to the corresponding display memory map. The result is an eight bit fill operation. The map designations are defined in the following table.

0 = Reset.
1 = Set.

BIT	SET/RESET
3	Map 3
2	Map 2
1	Map 1
0	Map 0

NOTE

The selection of Write Mode 0 is determined by the Graphics Mode Register (index = 05h) bit 1 and bit 0.

5.5.2 GCR Enable Set/Reset Register

Read/Write Port = 3CFh, Index = 01h

BIT	FUNCTION
7:4	Reserved
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bit 7:4

Reserved

Returns 0000 on reads of the Enable Set/Reset Register. No function is defined on writes.

Bit 3:0

Enable Set/Reset Register (Index 01h)

0 = When these bits are set to 0, Write Mode 0 is selected. The Set/Reset Register (index = 00h) and the corresponding memory map accesses are disabled, and the map is written with the rotated 8-bit data from the system microprocessor as defined by the Data Rotate Register (index=03h).

1 = When any of these bits are set to '1' and Write Mode 0 is selected, corresponding memory map access is enabled, as defined by the Set/Reset Register (index = 00h). The respective memory map is written with the bit value in the Set/Reset Register (index = 00h).

5.5.3 GCR Color Compare Register

Read/Write Port 3CFh, Index = 02h

BIT	FUNCTION
7:4	Reserved
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bit 7:4

Reserved

Returns 0000 on reads of the Color Compare Register. No function is defined on writes.

Bit 3:0

Color Compare

The color compare bit contains the value to which all 8 bits of the corresponding memory map are compared. This comparison also occurs across all four maps, and a 1 is returned for each of the map positions where the bits of all four maps equal the Color Compare Register. If a system read is done with bit 3=0 for the Graphics Mode Register (index=05h), data is returned without comparison. Color compare map coding is shown below:

BIT	COLOR COMPARES
3	Map 3
2	Map 2
1	Map 1
0	Map 0

5.5.4 GCR Data Rotate Register

Read/Write Port = 3CFh, Index = 03h

BIT	FUNCTION
7:5	Reserved
4	Function Select 1
3	Function Select 2
2	Rotate Count Bit 2
1	Rotate Count Bit 1
0	Rotate Count Bit 0

Bit 7:5

Reserved

Returns 0000 on reads of the Data Rotate Register. No function is defined on writes.

Bit 4:3

Function Select

Function select for any of the write mode operations defined in the Graphics Mode Register (index = 05h), is defined as follows:

BIT 4	BIT 3	FUNCTION*
0	0	Data unmodified
0	1	Data ANDed with the data the read latches
1	0	Data ORed with the data the read latches
1	1	Data XORed with the data the read latches

* The data refers to CPU data after going through the data rotation. The latches contains the memory data from the last memory read.

Bit 2:0

Rotate Count

The setting of bits 2:0 determines the number of bit positions of rotation of CPU data to the right. Data written by the CPU is rotated in write mode 0 (see Graphics Mode Register, index=05h).

5.5.5 GCR Read Map Select Register

Read/Write Port = 3CFh, Index = 04h

BIT	FUNCTION
7:2	Reserved
1	Map Select 1
0	Map Select 0

Bit 7:2

Reserved

Returns 000 on reads of the Read Map Select Register. No function is defined on writes.

Bit 1:0

Map Select

Map read selection is defined as follows:

BIT 1	BIT 0	READ MAP
0	0	0
0	1	1
1	0	2
1	1	3

These bits select the Memory Map to be accessed in memory read operations. These bit settings have no effect in the color compare read mode. In odd/even modes, these bit settings select chained maps 0 and 1 (bit 1=0), or value chained maps 2 and 3 (Bit 1=1).

5.5.6 GCR Graphics Mode Register

Read/Write Port = 3CFh, Index = 05h

BIT	FUNCTION
7	Reserved
6	256 Color Mode
5	Shift Register Load Control
4	CGA Odd/Even
3	Read Mode
2	Reserved
1	Write Mode bit 1
0	Write Mode bit 0

Bit 7

Reserved

Returns 0000 on reads of the Graphics Mode Register. No function is defined on writes.

Bit 6+

256 Color Mode

0 = Enables bit 5 of this register to control loading of the video shift registers. Each four bit pixel from video memory is expanded to six bits through the internal palette and is sent out on the lower six bits (VID5 through VID0) pins every dot clock. The remaining two video outputs (VID6, VID7) are determined by bits 2 and 3 of the Color Select Register within the Attribute Controller (Attribute Controller index=14h).

1 = Load video shift registers to support 256 color mode.

Bit 5

Shift Register Load Control

Shift Register Load Control determines the way in which memory data is formatted in the four video shift registers.

0 = For Map 0 through Map 3 data is loaded into the shift register for normal operations.

1 = For CGA graphics mode compatibility, even numbered bits from all the maps are shifted out of even numbered shift registers, odd numbered bits from all the maps are shifted out of odd numbered shift registers. The MSB is shifted out in either case.

Bit 4

Odd/Even Mode

0 = Normal

1 = CGA compatible odd/even system access mode. Sequential addressing as defined by bit 2 of the sequencer memory mode register (index = 04h). Even system addresses access maps 0 or 2 and odd system addresses access maps 1 or 3.

Bit 3

Read Mode

0 = System reads data from memory maps selected by Read Map Select Register (index = 04h) This setting has no effect if bit 3 of the Sequencer Memory Mode Register = 1.

1 = System reads the comparison of the memory maps and the Color Compare Register.

Bit 2

Reserved

Returns 0 on reads of the Graphics Mode Register. No function is defined on writes.

Bit 1:0

Write Mode

The following table defines the four write modes.

BIT 0	BIT 1	WRITE MODE
0	0	**Write Mode 0.** If the Set/Reset Register function is enabled for any of the maps, the eight bits of the bit value in the Set/Reset Register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. If the Set/Reset Register function is disabled, the map is written with the CPU data, which is right-rotated by the number of bits defined in the Data Rotate Register, with the old LSB now the new MSB.
0	1	**Write Mode 1.** This mode can be used to write the same value to many memory locations. The 32 bits of data in the system latches are written into each of the four memory maps. The system read operation loads the latches.
1	0	**Write Mode 2.** Memory maps are filled with the 8 bit value of the corresponding CPU data bits (3:0). The 32 bit output of the four memory maps is then operated on by the Bit Mask Register. The resulting data is written to the four memory maps.
1	1	**Write Mode 3.** Eight bits of the value contained in the Set/Reset Register (index = 00h) is written into the corresponding map, regardless of the Enable Set/Reset Register (index = 01h). The right-rotated CPU data (see Write Mode 0) is ANDed with Bit Mask Register data to form an 8-bit mask value that performs the same function as the Bit Mask Register in Write Modes 0 and 2.

5.5.7 GCR Miscellaneous Register

Read/Write Port = 3CFh, Index = 06h

BIT	FUNCTION
7:4	Reserved
3	Memory Map 1
2	Memory Map 0
1	Odd/Even Mode
0	Graphics Mode

Bit 7:4

Reserved

Returns 0000 on reads of the Miscellaneous Register. No function is defined on writes.

Bit 3:2

Memory Map 1,0

Display memory map control into the CPU address space is shown below:

BIT 3	BIT 2	CPU ADDRESS RANGE	LENGTH
0	0	A000:0h-BFFF:Fh	128 Kbyte
0	1	A000:0h-AFFF:Fh	64 Kbyte
1	0	B000:0h-B7FF:Fh	32 Kbyte
1	1	B800:0h-BFFF:Fh	32 Kbyte

Bit 1

Odd/Even Mode

0 = CPU address bit A0 is the memory address bit MA0.

1 = CPU address bit A is replaced by a higher order address bit. A0 is then used to select odd or even maps.

A0 = 0 selects map 0 or 2

A0 = 1 selects map 1 or 3

Bit 0

Graphics/Alphanumeric Mode

This bit is programmed the same way as bit 0 of the Attribute Mode Control Register.

0 = Alphanumeric mode selected.

1 = Graphics mode selected.

5.5.8 GCR Color Don't Care Register

Read/Write Port 3CFh, Index = 07h

BIT	FUNCTION
7:4	Reserved
3	Memory Map 3
2	Memory Map 2
1	Memory Map 1
0	Memory Map 0

Bit 7:4

Reserved

Returns 0000 on reads of the Color Don't Care Register. No function is defined on writes.

Bit 3:0

Memory Map Color Compare Operation

0 = Disable color compare operation.

1 = Enable color compare operation.

5.5.9 GCR Bit Mask Register

Read/Write Port = 3CFh, Index = 08h

BIT	FUNCTION
7:0	Bit Mask Operation

Bit 7:0

Bit Mask Operation

Bit mask operation applies simultaneously to all four maps. In Write Modes 0 and 2, this register provides selective changes to any bit stored in the system latches during processor writes. Data must first be latched by reading the addressed byte. After setting the Bit Mask Register, new data is written to the same byte in a subsequent operation. Bit mask operation is applicable to any data written by the processor.

0 = Bit position value is masked or is not changeable.

1 = Bit position value is unmasked and can be changed in the corresponding map.

5.6 ATTRIBUTE CONTROLLER REGISTERS

Refer to Section 5.1 for a summary of Attribute Controller Registers (ACR).

5.6.1 ACR Attribute Index Register

Read/Write Port = 3C0h

BIT	FUNCTION
7:6	Reserved
5	Palette Address Source
4:0	Attribute Address Bits

The Attribute Index register has an internal flip-flop, rather than an input bit, which controls the selection of the address and data registers. Reading Input Status Register 1 (port = 3?Ah) clears the flip-flop and selects the Address Register, which is read through address 3C1h and written at address 3C0h. Once the address register has been loaded with an index, the next write operation to 3C0h loads the data register. The flip-flop toggles between the address and the data registers after every write to address hex 3C0h, but does not toggle for reads to address 3C1h.

Bit 7:6

Reserved

Returns 00 on reads of the Attribute Index Register. No function is defined on writes.

Bit 5

Palette Address Source

0 = Disable internal color palette outputs and video outputs to allow CPU access to color palette registers (index 00 through 0Fh).
1 = Enable internal color palette and normal video translation.

Bit 4:0

Attribute Controller Index Register Address Bits

5.6.2 ACR Palette Registers (Index 00h through 0Fh)

Read Port = 3C1h/Write Port = 3C0h

BIT	FUNCTION
7:6	Reserved
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit 7:6

Reserved

Returns 00 on reads of the Palette Registers. No function is defined on writes.

Bit 5:0

Palette Pixel Colors

0 = Current pixel color deselected.
1 = Enable corresponding pixel color per the following table:

Bit 5	VID5
Bit 4	VID4
Bit 3	VID3
Bit 2	VID2
Bit 1	VID1
Bit 0	VID0

5.6.3 ACR Mode Control Register

Read Port = 3C1h/Write Port = 3C0h, Index = 10h

BIT	FUNCTION
7	VID5, VID4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved
3	Enable Blink/Select Background Intensity
2	Enable Line Graphics Character Code
1	Mono/Color Emulation
0	Graphics/Alphanumeric Mode Enable

Bit 7

VID5, VID4 Select

0 = VID5 and VID4 palette register outputs are selected.
1 = Color Select Register (index 14h) bits 1 and 0 are selected for outputs at VID5 and VID4 pins.

Bit 6

Pixel Width

0 = Disable 256 color mode pixel width. The PCLK output is the same as the internal dot clock rate.
1 = Enable pixel width for 256 color mode. The PCLK output is the internal dot clock divided by two.

Bit 5

PEL Panning Compatibility Line Compare in the CRT Controller

0 = A line compare has no effect on the PEL Panning Register.
1 = Allows a successful line compare to disable the PEL Panning Register and bits 5 and 6 of CRT Controller Register 08 until VSYNC occurs. Allows pixel panning of a selected portion of the screen.

Bit 4

Reserved

Returns 0 on reads of the Mode Control Register. No function is defined on writes.

Bit 3

Background Intensity/Blink Selection

0 = Selects background intensity from the MSB of the attribute byte.
1 = Selects blink attribute.

Bit 2

Enable Line Graphics Character Code

Set this bit to zero for character fonts that do not use line graphics character codes.

0 = Forces ninth dot to be the same color as background in line graphics character codes.
1 = Used in MDA line graphics modes. The ninth dot character is forced to be identical to the eighth character dot.

Bit 1

Mono/Color Emulation

0 = Color display attributes.
1 = MDA attributes

Bit 0

Graphics/Alphanumeric Mode Enable

0 = Alphanumeric mode.
1 = Graphics mode.

5.6.4 ACR Overscan Color Register

Read Port = 3C1h/Write Port = 3C0h, Index = 11h

BIT	FUNCTION
7	Overscan/Border Color Address

Bit 7:0

Overscan/Border Color

Border color is selected by selecting the desired address from available colors programmed into the RAMDAC.

These bits also select which of the 256 RAMDAC locations is used for the border color.

For Monochrome display, this register should be set to 0.

5.6.5 ACR Color Plane Enable Register

Read Port = 3C1h/Write Port = 3C0h,
Index 12h

BIT	FUNCTION
7:6	Reserved
5	Video Status MUX1
4	Video Status MUX0
3:0	Enable Color Plane

Bit 7:6

Reserved

Returns 00 on reads of the Color Plane Enable Register. No function is defined on writes.

Bit 5:4

Video Status Control

These bits select 2 out of the 8 color plane bits (VID [7:0])which can be read by the Input Status Register 1 (port = 03?A) bits 4 and 5.

COLOR PLANES		INPUT STATUS VALUE	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID 2	VID 0
0	1	VID 5	VID 4
1	0	VID 3	VID 1
1	1	VID 7	VID 6

Bit 3:0

Color Plane Enable

0 = Disables respective color planes. Forces pixel bit to 0 before it addresses palette.
1 = Enables the respective display memory color plane.

5.6.6 ACR Horizontal Pixel Panning Register

Read Port = 3C1h/Write Port = 3C0h, Index = 13h

BIT	FUNCTION
7:4	Reserved
3:0	Horizontal Pixel Panning

Bit 7:4

Reserved

Returns 0000 on reads of the Horizontal Pixel Panning Register. No function is defined on writes.

Bit 3:0

Horizontal Pixel Panning

Horizontal Pixel Panning is available in text or graphics modes. These bits select pixel shift to the left horizontally. For 9 dots/character modes, up to 8 pixels can be shifted horizontally to the left. Likewise, for 8 dots/character, up to 7 pixels can be shifted horizontally to the left. For 256 colors, up to a 3-position pixel shift can occur. The following table defines the shift in different modes.

LEFT SHIFT PIXEL VALUE			
Register Value	9 Dots Char-acter	8 Dots Char-acter	256 Color Mode
0	1	0	0
1	2	1	---
2	3	2	1
3	4	3	---
4	5	4	2
5	6	5	---
6	7	6	3
7	8	7	---
8	0	---	---

5.6.7 ACR Color Select Register

Read Port = 3C1h/Write Port = 3C0h, Index = 14h

BIT	FUNCTION
7:4	Reserved
3	S_Color 7
2	S_Color 6
1	S_Color 5
0	S_Color 4

Bit 7:4

Reserved

Returns 0000 on reads of the Color Select Register. No function is defined on writes.

Bit 3:2

Color Value MSB

These are the two most significant bits of the eight digit color value for the video DAC. They are normally used in all modes except 256 color graphics.

Bit 3 = Set color bit VID 7.
Bit 2 = Set color bit VID 6.

Bit 1:0

Substituted Color Value Bits

These bits can be substituted for VID 5 and VID 4 output by the Attribute Controller Palette registers to create 8-bit color value. They are selected by the Attribute Controller Mode Control Register (index = 10h).

Bit 1 = Set color bit VID 5.
Bit 0 = Set color bit VID 4.

5.7 RAMDAC REGISTERS

See Section 5.1 for a summary of these registers.

5.7.1 RAMDAC Write Address Register

Read/Write Port=3C8h

BIT	FUNCTION
7:0	RAMDAC Write Address

Bit 7:0

RAMDAC Write Address

This register contains the eight-bit address used to access one of the 256 Color Registers during a write operation. During reads, the RAMDAC Write Address is the address of the next location to be modified during write operations.

The RAMDAC Write Address should be read only after completion of a three-write (red-green-blue) sequence. Reads in the middle of this sequence can produce unpredictable results.

5.7.2 RAMDAC Read Address Register

Write Port = 3C7h

BIT	FUNCTION
7:0	RAMDAC Read Address

Bit 7:0

RAMDAC Read Address

This register contains the eight-bit address used to access one of the 256 Color Registers during a read operation.

5.7.3 RAMDAC State Register

Read Port = 3C7h

BIT	FUNCTION
7:0	RAMDAC State

Bit 7:0

RAMDAC State

These RAMDAC State bits reflect whether a read or a write operation is in effect:

00h = A read operation is in effect. The address read register was accessed last.
03h = A write operation is in effect. The address write register was accessed last.

5.7.4 RAMDAC Pixel Data Register

Read/Write Port = 3C9

BIT	FUNCTION
7:0	RAMDAC Pixel Data Register

Bit 7:0

RAMDAC Pixel Data Register

This is an 18-bit wide data register used for reading and writing RAMDAC color values. Three sequential reads or writes to this register are required to access all 18-bits of data at a particular read or write address.

5.7.5 RAMDAC Pixel Mask Register

Read/Write Port = 3C6

BIT	FUNCTION
7:0	Mask Value

Bit 7:0

Mask Value

This register is a read/write register. However, it is not to be modified by applications programs. It should be initialized to FFh by BIOS firmware during a Mode Set call.

5.8 COMPATIBILITY REGISTERS

Refer to Section 5.1 for a summary of Compatibility Registers.

5.8.1 Enable Mode Register

MDA Write Only Port = 3B8h

This register is accessible in Hercules and MDA modes with hardware emulation.

BIT	FUNCTION
7	Reserved/Display Memory Page Select
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Port 3BFh Enable
0	High Resolution Mode

Bit 7

Reserved in MDA Mode

If Bit 1=1 and Port 3BFh bit 0=1, then this bit, in Hercules Graphics mode, selects the Display Memory Page.

0 = Display memory page address starts at B000:0h.
1 = Display memory page address starts at B800:0h.

Bit 6

Reserved

No function is defined on writes to the Enable Mode Register.

Bit 5

Enable Blink

0 = Disable Blink
1 = Enable Blink

Bit 4

Reserved

Bit 3

Video Enable

0 = Video Disable
1 = Video activated

Bit 2

Reserved.

No function is defined on writes to the Enable Mode Register.

Bit 1

Port 3BFh Enable

0 = Prevents setting of Port 3BF bit 1:0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BFh bits 1:0 to switch for the alpha or graphics mode selection.

Bit 0

High Resolution Mode

This bit should be set to 1.

0 = High resolution disabled.
1 = High resolution is enabled.

5.8.2 Hercules Mode Register

Write Only Port = 3BFh

BIT	FUNCTION
7:2	Reserved
1	Upper Memory Page Address
0	Enable Graphics

The Hercules Mode register is a 2-bit write only register located at I/O port address 3BFh. It affects device operation only in 6845 mode. The enable mode register located at address 3B8h overrides write port 3BFh functions defined by its bits 0 and 1. The associated details are given in the following descriptions.

Bits 7:2

Reserved

No function is defined on writes to the Hercules Mode Register.

Bit 1

Upper Memory Page Address

Enable Mode Control Register (3B8h) bit 7 selects the displayed memory page address in graphics mode. When it is reset, bit 1 prevents access to the second memory page, located at B000:0h for the 32K Byte memory space.

0 = Upper memory page is mapped out.
1 = Upper memory page is accessible.

Bit 0

Enable Graphics

Selects alpha or graphics mode. May be overridden by Hercules Enable Mode Register, bit 1.

0 = Alpha mode display.
1 = Graphics modes may be displayed.

5.8.3 CGA Color Operation Register

Write Only Port - 3D8h

BIT	FUNCTION
7:6	Reserved
5	Enable Blink
4	B/W Graphics Mode
3	Enable Video
2	B/W/Color Mode Select
1	Graphics/Alpha Mode Select
0	Alpha Mode

Bit 7:6

Reserved.

No function is defined on writes to the CGA Color Operation Register.

Bit 5

Enable Blink Function

0 = Disables blinking function.
1 = For normal operation, set this bit to allow blinking

Bit 4

B/W Graphics Mode Enable

0 = Disable 640 x 200 B/W graphics mode.
1 = Enable 640 x 200 B/W graphics mode.

Bit 3

Activate Video Signal

0 = Disables video signal. This is done during mode changes.
1 = B/W mode enabled.

Bit 2

B/W or Color Display Mode

0 = Color mode selected
1 = B/W mode selected

Bit 1

Text or Graphics Mode Selection

0 = Alpha mode enable.
1 = Graphics mode (320 x 200) enabled.

Bit 0

(40 x 25) or (80 x 25) Text Mode Selection.

0 = 40 x 25 alpha mode enabled.
1 = 80 x 25 alpha mode enabled.

5.8.4 CGA Color Select Register

Write Only Port = 3D9h

BIT	FUNCTION
7:6	Reserved
5	Graphics Mode Color Set
4	Alternate Color Set
3	Border Intensity
2	Red Border
1	Green Border
0	Blue Border

Bit 7:6

Reserved.

No function is defined on writes to the Color Select Register.

Bit 5

Set CGA 320x200 Color in 2 bits per pixel modes.

0 = Background, Green, Red, Brown
1 = Background, Cyan, Magenta, White

Bit 4

Alternate Color Set Enable

0 = Background color in alpha mode.
1 = Enable alternate color set in graphics mode.

Bit 3

Border Intensity

Border color select in text modes. Screen background color in 320x200 and 640x200 graphics mode.

Text Mode.

1 = Selects intensified border color.

320 x 200 Graphics mode.

1 = Selects intensified background and border color (C0-C1).

640 x 200 Graphics Mode.

1 = Selects red foreground color.

Bit 2

Red Border/Background

Border color select in text modes. Screen background color in 320x200 and 640x200 graphics modes.

Text Mode:

1 = Selects red border color

320 x 200 Graphics Mode:

1 = Selects red background and border color

640 x 200 Graphics Mode:

1 = Selects red foreground color.

Bit 1

Green Border/Background

Border Color select in text modes. Screen background color in 320x200 and 640x200 graphics mode.

Text Mode.

1 = Selects green border color.

320 x 200 Graphics mode.

1 = Selects green background and border color (C0-C1).

640 x 200 Graphics Mode.

1 = Selects green foreground color.

Bit 0

Blue border/Background

Border Color select in text modes. Screen background color in 320x200 and 640x200 graphics mode.

Text Mode.

1 = Selects Blue border color.

320 x 200 Graphics mode.

1 = Selects Blue background and border color (C0-C1).

640 x 200 Graphics Mode.

1 = Selects Blue foreground color.

5.8.5 CRT Status Register, MDA Operation

Read Only Port = 3BAh

BIT	FUNCTION
7	VSYNC Inactive
6:4	Reserved
3	B/W Video Enabled
2:1	Reserved
0	Display Enable Inactive

Bit 7

Vertical Retrace

0 = Indicates that the raster is in vertical retrace mode.
1 = Indicates that the vertical retrace is inactive (inverted VSYNC if I/O is mapped into 3BX).

Bit 6:4

Reserved.

No function is defined on writes to the MDA CRT Status Register.

Bit 3

Black/White Video Status

0 = B/W Video disabled.
1 = B/W Video enabled.

Bit 2:1

Reserved.

No function is defined on writes to the MDA CRT Status Register.

Bit 0

Display Enable

0 = Display enable is active.
1 = Screen border or blanking is active. Display Enable is inactive.

5.8.6 CRT Status Register, CGA Operation

MDA Read Only Port = 3DAh

BIT	FUNCTION
7:4	Reserved
3	VSYNC Active
2	Light Pen Switch Status
1	Light Pen Latch Set
0	Display Enable Inactive

Bit 7:4

Reserved.

No function is defined on writes to the CGA CRT Status Register.

Bit 3

Vertical Retrace

0 = Vertical retrace is inactive.
1= Raster is in vertical retrace mode.

Bit 2

Light Pen Switch Status

0 = Light pen switch closed.
1 = Light pen switch open.

Bit 1

Light Pen Latch

0 = Light pen latch cleared.
1 = Light pen latch set.

Bit 0

Display Enable

0 = Display enable is active.
1 = Screen border or blanking is active. Display Enable is inactive.

5.9 PARADISE REGISTERS

Refer to Section 5.1 for a summary of PR Registers and general information.

5.9.1 PR0(A) and PR0(B) - Address Offset Registers

PR0(A)

Read/Write Port = 3CFh, Index = 09h
Unlock: PR5 (3CF.0Fh) = 05h

BITS	FUNCTION
7	Undefined
6:0	Video Memory Address Offset A

PR0(B)

Read/Write Port = 3CFh, Index = 0Ah
Unlock: PR5 (3CF.0Fh)=05h

BITS	FUNCTION
7	Undefined
6:0	Video Memory Address Offset B

Bit 7

Reserved. Undefined on reads. Should be set to 0 on writes.

Bit 6:0

Offset Values

The WD90C26A can interface with up to 512 Kbytes of video memory. However, the system memory map for VGA compatibility defines only 128 Kbytes of video memory accessible via the system bus interface, at locations A000:0h through BFFF:Fh. Access, in some cases, is further limited to a 64 Kbyte range to support two video controllers within the same 128 Kbyte memory map.

Because of these system addressing limitations, the WD90C26A has two video memory address offset registers available that can be used to access up to 512 Kbytes of linear addressed memory through the 64 Kbyte or 128 Kbyte system address space for system memory.

These offset registers are PR0(A) and PR0(B). The registers contain offsets that are added to the system address to allow access to more than 64 Kbytes of video memory. PR0(A) is the default Address Offset register used for video memory access. PR0(B) can be enabled to provide a different offset over half of the memory map. PR0(B) is enabled as the offset register when PR1 register bit 3 is set to 1.

The 7-bit offset provided by either PR0(A) or PR0(B) that is added to address bits A (18:12) of the system address to form a 20-bit address, which allows access to up to 512 Kbyte of video memory. Unlike most VGA controllers that allow video memory access only on 64 Kbyte boundaries, the WD90C26A provides offsetting of the 64 or 128 Kbyte 'window' to video memory on 4 Kbyte boundaries. This arrangement is similar to segment registers DS and ES architecture of the 8088/80X86 with PR0(A) or PR0(B) providing the 4 Kbyte offsets.

When the WD90C26A is configured in a 64 Kbyte system address space (as defined by the setting of Graphics Miscellaneous Register Bits 3 and 2), and PR0(B) is enabled by setting PR1 register bit 3 to 1, PR0(A) and PR0(B) can be used to access two separate 32 Kbyte video RAM 'windows'. The video memory is accessed using the PR0(A) offset in the system memory address range from A800:0h through AFFF.Fh, or using the PR0(B) offset in the system memory address range from A000:0h through A7FF:Fh.

When the WD90C26A is configured in a 128 Kbyte system address space (as defined by the setting of Graphics Miscellaneous Register bits 3 and 2), and PR0(B) is enabled, PR0(A) is the offset for system access from B000:0h through BFFF:Bh, while PR0(B) is the offset for system accesses from A000:0h through AFFF:Fh.

Also, PR0(A) can be set to provide address offsets during read cycles only while PR0(B) provides address offsets during write cycles only. Refer to the description for PR31 register bit 7.

5.9.2 PR1 - Memory Size and Bus Interface Select Register

Read/Write Port = 3CFh, Index = 0Bh
Unlock: PR5 (3CF.0Fh)=05h

BITS	FUNCTION
7:6	Memory Organization
5:4	System Memory Map Mode
3	Enable Alternate Address Offset Register PR0(B)
2	$\overline{\text{MEMCS16}}$/$\overline{\text{CDDS16}}$ Enable
1	AT/MC or PI Bus Interface Status
0	Enable BIOS ROM

Bit 7:6

Memory Organization Select

These bits must be set to reflect the amount of usable video memory installed. These bits, in conjunction with PR16 register bit 1, also select the way that memory is mapped into the System Address.

Where Bank B memory is not present, PR1 register bits 6 and 7 should be set for 256 Kbytes of video memory.

Also, PR1 register bits 6 and 7 should be set for 256 Kbytes of video memory if Bank B is used as a frame buffer in dual-panel LCD and CRT simultaneous display environments, or where system power reduction is desired by reducing the amount of active memory

BITS 7:6		PR16 BIT 1*	VIDEO MEMORY ADDRESSING MODE
0	0	0	256K (Bank A Qty 2 256Kx4 DRAMS) Standard VGA Memory Organization
0	1	0	256K (Bank A Qty 2 256Kx4 DRAMS) Using WD90C26A Memory Organization
1	0	0	512K [Bank A Qty 2 256Kx4 and Bank B Qty 2 256Kx4 (non-frame buffer) or 256Kx16 DRAM] Using WD90C26A Memory Organization
1	1	0	Reserved - Defaults to 256K Standard VGA Memory Organization
X	X	1	Force to 256K - forces size to 256K Standard VGA Memory Organization

NOTE

*When PR16 register bit 1 is set to 1, the settings of PR1 register bits 6 and 7 are overridden and the standard VGA 256 Kbyte memory organization is selected.

Tables 5-12 through 5-14 list the memory organization for valid conditions of PR1 register bits 7 and 6. Refer also to descriptions of PR16 register bits 6, 5, 2, and 1, and the Sequencer Memory Mode Register.

Table 5-12 lists the memory organization for byte, word, and double word access when PR1 register bits 7 and 6 are both set to 0. This setting provides the standard VGA memory organization with 256 Kbytes of video memory on four planes of 64 Kbytes each. Refer to notes on the following page.

WD90C26A DRAM INTERFACE ADDRESS	BYTE ACCESS 3?5.14h, Bit 6 = 0 3?5.16h, Bit 6 = 1		WORD ACCESS 3?5.14h, Bit 6 = 0 3?5.16h, Bit 6 = 0		DBL WORD ACCESS 3?5.14h, Bit 6 = 1 3?5.16h, Bit 6 = x[4]	
	CPU	CRT	CPU	CRT	CPU	CRT
[1]MA(17)	0	0	0	0	0	0
MA(16)	0	0	0	0	0	0
MA(15)	[2]SA(15)	[3]CA(15)	SA(15)	CA(14)	SA(15)	CA(13)
MA(14)	SA(14)	CA(14)	SA(14)	CA(13)	SA(14)	CA(12)
⋮	⋮	⋮	⋮	⋮	⋮	⋮
MA(2)	SA(2)	CA(2)	SA(2)	CA(1)	SA(2)	CA(0)
MA(1)	SA(1)	CA(1)	SA(1)	CA(0)	SA(15)	CA(13)
MA(0)	SA(0)	CA(0)	SA(16) o r 3C2(5)	CA(15) or CA(13)	SA(14)	CA(12)

TABLE 5-15 256K STANDARD VGA MEMORY ORGANIZATION

Table 5-13 lists the memory organization for byte, word, and double word access when PR1 register bits 7 and 6 are set to 0 and 1, respectively. This setting provides the WD90C26A memory organization with 256 Kbytes of video memory on four planes of 64 Kbytes each. Refer to notes on the following page.

WD90C26A DRAM INTERFACE ADDRESS	BYTE ACCESS 3?5.14h, Bit 6 = 0 3?5.16h, Bit 6 = 1		WORD ACCESS 3?5.14h, Bit 6 = 0 3?5.16h, Bit 6 = 0		DBL WORD ACCESS 3?5.14h, Bit 6 = 1 3?5.16h, Bit 6 = x[4]	
	CPU	CRT	CPU	CRT	CPU	CRT
[1]MA(17)	0	0	0	0	0	0
MA(16)	0	0	0	0	0	0
MA(15)	[2]SA(15)	[3]CA(15)	SA(15)	CA(14)	SA(15)	CA(13)
MA(14)	SA(14)	CA(14)	SA(14)	CA(13)	SA(14)	CA(12)
⋮	⋮	⋮	⋮	⋮	⋮	⋮
MA(2)	SA(2)	CA(2)	SA(2)	CA(1)	SA(2)	CA(0)
MA(1)	SA(1)	CA(1)	SA(1)	CA(0)	SA(17)	CA(15)
MA(0)	SA(0)	CA(0)	SA(16)	CA(15)	SA(16)	CA(14)

TABLE 5-16 256K WD90C26A VGA MEMORY ORGANIZATION

Table 5-14 lists the memory organization for byte, word, and double word access when PR1 register bits 7 and 6 are set to 1 and 0, respectively. This setting provides the WD90C26A memory organization with 512 Kbytes of video memory on four planes of 128 Kbytes each. Each plane has two banks of 64 Kbytes. Refer to the following notes.

WD90C26A DRAM INTERFACE ADDRESS	BYTE ACCESS 3?5.14h, Bit 6 = 0 3?5.16h, Bit 6 = 1		WORD ACCESS 3?5.14h, Bit 6 = 0 3?5.16h, Bit 6 = 0		DBL WORD ACCESS 3?5.14h, Bit 6 = 1 3?5.16h, Bit 6 = x[4]	
	CPU	CRT	CPU	CRT	CPU	CRT
[1]MA(17)	0	0	0	0	0	0
MA(16)	[2]SA(16)	[3]CA(16)	SA(17)	CA(16)	SA(18)	CA(16)
MA(15)	[2]SA(15)	[3]CA(15)	SA(15)	CA(14)	SA(15)	CA(13)
MA(14)	SA(14)	CA(14)	SA(14)	CA(13)	SA(14)	CA(12)
⋮	⋮	⋮	⋮	⋮	⋮	⋮
MA(2)	SA(2)	CA(2)	SA(2)	CA(1)	SA(2)	CA(0)
MA(1)	SA(1)	CA(1)	SA(1)	CA(0)	SA(17)	CA(15)
MA(0)	SA(0)	CA(0)	SA(16)	CA(15)	SA(16)	CA(14)

TABLE 5-17 512K WD90C26A VGA MEMORY ORGANIZATION

NOTES FOR TABLES 5-12 THROUGH 5-14

1. MA indicates address lines to video DRAM before RAS/CAS multiplexing.
2. SA indicates WD99C26A internally modified System Addresses (SA19:SA0).
3. CA indicates CRT Controller Character Address Counter bits (CA19:CA0).
4. The x indicates that the bit value does not affect this operation.
5. The symbol with three vertical dots indicates a continuation of the same pattern of address signal mapping.
6. In video hardware emulation modes, CA(13) supports only 64 Kbytes of video DRAM.

Bit 5:4

System Memory Map Mode

Video memory usually occupies the 128 Kbyte CPU address range from 0A0000h through 0BFFFFh. Bits 5 and 4 of this register allow video memory to be mapped to other pages of system memory above the 1 Mbyte limit. In the area above the 1 Mbyte limit, video memory can be accessed linearly instead of in segments. The description of PR34A lists the available address ranges for this mapping feature.

5	4	VIDEO MEMORY MAP MODE
0	0	Standard IBM VGA Video Memory Mapping. System addresses from 0A0000h - 0BFFFFh (From the lowest 1 Mbyte CPU address space) are used to access the WD90C26A memory. The accessible area within this space depends upon the setting VGA Miscellaneous registers bits 2 and 3).
0	1	First 256 Kbytes of video memory in a linear address range of system memory addresses on a 1 Mbyte boundaries, as determined by PR34A(3:0). If 512K is installed, the second 256K is accessible over the standard (below 1 Mbyte) video memory address range.
1	0	All 512K byte of video memory (if Qty 4, 256Kx4s or one 256Kx16 of video memory installed) in a linear address range of system memory addresses on 1 Mbyte boundaries determined by PR34A(3:0).
1	1	Reserved

PR34A register bits3 through 0 control which 1Mbyte of system memory address space the WD90C26A is mapped to. This feature is disabled if operation is configured for 12-bit TFT panel support.

Bit 3

Alternate Address Offset Enable

This bit allows PR0(B) to be enabled for alternate offset functions as defined by PR31 register bit 7 and Graphics Miscellaneous register bits 2 and 3.

BIT 3	ALTERNATE ADDRESS OFFSET REGISTER ENABLE
0	PR0(A) is used by the WD90C26A as the Address Offset Register for the entire memory range.
1	PR0(A) and PR0(B) are both used as offsets registers as determined by Miscellaneous register bits 2 and 3 and by PR31 register bit 7.

Bit 2

Enable $\overline{\text{MEMCS16}}$/$\overline{\text{CDDS16}}$

Enables 16-bit video memory access for ISA bus ($\overline{\text{MEMCS16}}$) or the MicroChannel bus (CDDS16. Refer to the PR1 and PR16 descriptions for video memory address range.

NOTE

Bit 2 may be set to 1 whenever 8 bits of video memory are used. Internal circuits perform 16-bit bus memory cycle to 8-bit DRAM cycle conversion).

BIT 2	$\overline{\text{MEMCS16}}$ or $\overline{\text{CDDS16}}$ ENABLE
0	$\overline{\text{MEMCS16}}$ or $\overline{\text{CDDS16}}$ disabled
1	$\overline{\text{MEMCS16}}$ or $\overline{\text{CDDS16}}$ goes active low for memory video addresses.

Bit 1

AT/MC or PI Bus Interface Status (Read-Only)

This bit is initialized at reset as CNF(1) and indicates CNF(1) status on reads. CNF(1) is pulled up or down at reset to select either the AT and Microchannel buses or the Peripheral Interface (PI) bus, respectively. If CNF(1) is pulled up, then CNF(2) is pulled up or down to select either the AT bus or the MicroChannel bus.

BUS INTERFACE	AMD1		AMD2
	PR1 PIN 1	CNF(1)	CNF(2)
AT Bus	0	Pullup (0)	Pullup (0)
MicroChannel	0	Pullup (0)	Pulldown (1)
PI Bus	1	Pulldown (1)	Don't Care

Refer to Section 6 for information on hardware configuration options

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PR1 register bit 1 is undefined on writes.

BIT 1	STATUS
0	AT or MicroChannel Bus Interface
1	PI Bus Interface

Bit 0

Enable BIOS ROM

This bit controls whether or not the WD90C26A enables its $\overline{\text{EBROM}}$ output for memory addresses in the video BIOS range.

This bit is initialized at reset to the level on AMD (0) during reset. The setting is known as CNF(0) and may be modified at any time after reset.

BIT 0	BIOS ROM MAP OUT
0	BIOS ROM Support Enable
1	BIOS ROM Support Not Enabled

5.9.3 PR2 - Video Select Register

Read/Write Port = 3CFh, Index = 0Ch
Unlock: PR5 (3CF.0Fh)=05h

BIT	FUNCTION
7	AT&T/M24 Mode Enable
6	6845 Compatibility
5	Character Map Select
4:3	Character Clock Period Control
2	Underline/Character Map
1	Third Clock Select Line VCLK2
0	Force Dot Clock = VCLK

Bit 7

Enable AT&T/M24 Mode.

Sets the WD90C26A to be operationally and interface compatible with AT&T/M24 video systems.

Bit 6

6845 Compatibility

Sets the CRTC operation and register access to be 6845 compatible.

0 = VGA modes
1 = Non-VGA modes

Bit 5

Character Map Select

In text modes, this bit, bit 2 of this same register, and bit 4 of the corresponding attribute code in video memory, determine whether the character map from video memory plane 2 or 3 is used as the font for text display.

The description of PR1 explains memory plane organizations for the WD90C26A.

PR2(5)	PR2(2)	Attrb(4)	Selects Plane
0	0	X	2
0	1	X	2
1	0	X	3
1	1	0	2
1	1	1	3

NOTE

The Character Map Select functions given in the previous list are overridden by setting PR15 register bit 2 to 1. Page Mode addressing overrides this selection of character the map plane and uses a selection method suited for page mode, which is given in the description of PR15.

Bit 3:4

Text Mode Character Clock Period Control

Selects the width of character boxes in text mode by determining hoe many dot clock pulses per character clock The relationship of dot clock to VCLK input is controlled by Sequencer Clocking Mode register bit 3.

BIT 4	BIT 3	TEXT MODE CHARACTER CLOCK PERIOD CONTROL
0	0	IBM VGA character width (8 or 9 dots)
0	1	7 dots (used for 132 character mode)
1	0	9 dots
1	1	10 dots

Selecting 10 dots/character modifies the function of the VGA Horizontal pixel Panning Register (3C0.13h).

NOTE

The character clock period control functions of PR2 have no effect in graphics modes

Bit 2

Underline and Character Map Select

Setting this bit to 1 enables underline for all odd values of attribute codes, and overrides the background color function of the corresponding attribute code in video memory. Therefore, only eight choices of background color are selectable. This function allows trading background colors for more character maps (see description of bit 5).

This bit is also decoded, in conjunction with bit 5, to enable the character maps to be selected from Plane 3 (see description of bit 5).

Bit 1

VCSEL (Pin 55) Select

This bit is the third clock select line sent to an external clock if CNF(3) is set to 1 and PR15 register bit 5 is set to 0.

BIT 1	VCSEL (Pin 55)
0	VCSEL is low
1	VCSEL is high

When CNF(3) and PR15 register bit 5 are both set to 1, this register bit (PR2, bit 1) has no affect, and Miscellaneous Output register bit 3 determines the level at pin 55.

If CNF(3) is set to 0, this register bit (PR2, bit 1) locks the Internal Video Clock Select determined by bits 2 and 3 of the VGA Miscellaneous Output register.

BIT 1	INTERNAL VCLK MULTIPLEXER
0	Unlocked
1	Locked

Bit 0

Force Dot Clock = VCLK

Forces the Dot Clock source to the horizontal timing section of the CRTC to VCLK. This is used for flat panel modes that require locking the CRTC timing parameters but need undivided dot clocks.

BIT 0	FORCE DOT CLOCK
0	Dot Clock Selected by Sequencer Clock Control Register Bit 3
1	Dot Clock Forced to the Selected VCLK input

5.9.4 PR3 - CRT Lock Control Register

Read/Write Port = 3CFh, Index = 0Dh
Unlock: PR5(3CFh.0Fh) = 05h

BIT	FUNCTION
7	Lock VSYNC Polarity
6	Lock HSYNC Polarity
5	Lock Horizontal Timing
4	Bit 9 of Start Memory Address High
3	Bit 8 of Start Memory Address High
2	Double Row Counts
1	Vertical Timing Group 1 Lock Prevention
0	Vertical Timing Groups 2 and 3 Unlock Prevention

Bit 7

Lock VSYNC Polarity

This bit causes the VSYNC polarity set in the Miscellaneous Output register (3C2h) bit 7 to be locked.

Bit 6

Lock HSYNC Polarity

This bit causes the HSYNC polarity set in the Miscellaneous Output register (3C2h) bit 6 to be locked.

Bit 5

Lock Horizontal Timing

Locks CRTC registers of Groups 0 and 4. Overrides attempt by applications software to unlock Group 0 registers by setting the Vertical Retrace End register 3?5h, index 11h, bit 7 to 0. (refer to Group Definitions given in the following paragraphs.)

Bit 4

Bit 9 of Start Memory Address High

Combines bit 9 of CRT Controller Start Memory Address High register (3?5.0Ch) as well as bit 9 of Cursor Location High register (3?5.0Eh). This bit (PR3, bit 4) corresponds to CRTC Character Address A17.

Bit 3

Bit 8 of Start Memory Address High

Combines bit 8 of CRT Controller Start Memory Address High register (3?5.0Ch), and bit 8 of Cursor Location High register (3?5.0Eh). This bit (PR3, bit 4) corresponds to CRTC Character Address A16.

Bit 2

Double Row Counts

When bit 2 is set, cursor start, stop, preset row scan, and maximum scan line address register counts are doubled.

Bit 1

Vertical Timing Group 1 Lock Prevention

Overrides any attempt by applications software to lock registers of Group 1 by its setting (3?5.11h) bit 7 to 1 (refer to the following Group Definitions).

Bit 0

Vertical Timing Groups 2 and 3 Unlock Prevention

Locks CRTC registers of Groups 2 and 3. Overrides any attempt by applications software to unlock Group 2 and 3 registers by its setting (3?5.11h) bit 7 to 0 (refer to the following Group Definitions).

Group Definitions

Register locking is controlled by 4 bits. They are PR3 bits 5, 1, and 0 and the Vertical Retrace End register (3?5.11) bit 7. When 3?5.11 bit 7 is set to 1, CRT controller registers (R0 through R7) are write protected in five groups per VGA definition.

For more information on the five groups, and their locking schemes, refer to the following descriptions.

- Group 0

The following registers are locked if PR3 register bit 5 is set to 1 **or** CRTC register 3?5.11h bit 7 is set to 1.

3?5 index 00 -- Horiz Total Characters per scan
3?5 index 01 -- Horiz Display Enable End
3?5 index 02 -- Start Horiz Blanking
3?5 index 03 -- End Horiz Blanking
3?5 index 04 -- Start Horiz Retrace
3?5 index 05 -- End Horiz Retrace

- Group 1

The following registers are locked if PR3 register bit 1 is set to 0 **and** CRTC register 3?5.11h bit 7 is set to 1.

3?5 index 07, bit 6 - Vertical Display Enable End bit 9
3?5 index 07, bit 1 - Vertical Display Enable End bit 8
3?5 index 3E, bit 1 - Vertical Display Enable End bit 10

- Group 2

The following registers are locked if PR3 register bit 0 is set to 1 **or** CRTC register 3?5.11h bit 7 is set to 1

3?5 index 06 -- Vertical total
3?5 index 07 (Bit 7) - Vertical Retrace Start bit 9
3?5 index 07 (bit 5) - Vertical Total bit 9
3?5 index 07 (bit 3) - Start Vertical Blank bit 8
3?5 index 07 (bit 2) - Vertical Retrace Start bit 8
3?5 index 07 (bit 0) - Vertical Total bit 8
3?5 index 09 (bit 5) - Start Vertical Blank bit 9
3?5 index 3E (bit 0) - Vertical total bit 10
3?5 index 3E (bit 2) - Vertical Retrace Start bit 10
3?5 index 3E (bit 3) - Start Vertical Blank bit 10

- Group 3

The following registers are locked if PR3 register bit 0 is set to 1.

3?5 index 10 - Vertical Retrace Start
3?5 index 11 - [(bits 3:0)] - Vertical Retrace End
3?5 index 15 - Start Vertical Blanking
3?5 index 16 - End Vertical Blanking

- Group 4

The following register is locked if PR3 register bit 5 is set to 1.

CRTC mode control register 17 (bit 2) - Selects divide by two vertical timing.

5.9.5 PR4 - Video Control Register

Read/Write Port = 3CFh, Index = 0Eh
Unlock: PR5 (3CF.0Fh)=05h

This register can be programmed to tri-state the CRT display control outputs as well as video data for the RAMDAC, and memory control outputs.

BIT	FUNCTION
7	$\overline{\text{BLANK}}$ / Display Enable
6	Force PCLK equal to VCLK
5	Tri-state Video Outputs
4	Tri-state Memory Control Outputs
3	Force CGA Enable Video
2	Lock Internal Palette and Overscan Registers
1	Reserved
0	Extended 256 color Shift Register Control

Bit 7

$\overline{\text{BLANK}}$ / Display Enable

This bit controls the output signal at the FR/$\overline{\text{BLANK}}$ pin on the WD90C26A. In external RAMDAC applications the FR/$\overline{\text{BLANK}}$ pin can be configured to provide a video DAC blanking signal.

If this bit is set to 1 and the CRT only function is enabled (PR19 register bits 5 and 4 are set to 10), the FR/$\overline{\text{BLANK}}$ output pin supplies a Display Enable signal. A choice of two types of Display Enable timing can be made available at the FR/$\overline{\text{BLANK}}$ pin, as determined by PR15 register bit 1.

If this bit is set to 0, PR19 register bit 5 is set to 1 (CRT), and PR19 register bit 4 is set to 0 (no panel), the FR/$\overline{\text{BLANK}}$ output is held at static low.

Whenever PR19 register bit 4 is set to1 (flat panel support is enabled), this bit is the frame rate signal to the panel and is controlled by PR62 (3CF.15h).

Bit 6

Force PCLK equal to VCLK

0 = PCLK is the inverted internal VCLK (video dot clock), or VCLK divided-by-two, depending upon the video mode.
1 = PCLK is the non-inverted, selected VCLK input signal, independent of video mode.

Bit 5

Tri-state Video Outputs

Tri-state the outputs UD(3:0), LD(3:0), HSYNC, VSYNC, FP, LP, $\overline{\text{RPLT}}$/B0, WPLT/PNLOFF (if PR57 register bit 7 is set to 1) and FR/$\overline{\text{BLANK}}$. This bit is typically used only for manufacturing test.

Bit 4

Tri-state the Memory Control Outputs

Memory address bus AMA(8:0), BMA(8:0), and all DRAM control signals are tri-stated when this bit is set to 1. This bit is typically used only for manufacturing test.

Bit 3

Force CGA Enable Video

Overrides the setting of CGA Mode (3D8h) register bit 3, if the bit is set to 1 in 80 x 25 alpha CGA mode. This forcing causes video to be enabled independent of CGA Mode register bit 3. Reset clears this bit to 0.

Bit 2

Lock Palette and Overscan Registers

Bit 1

Reserved

Must be set to 0 on writes to PR4 for proper function of the WD90C26A. Undefined on reads of PR4.

Bit 0

Extended 256 color Shift Register Control

Configures the video shift registers for Extended 256-color mode. This bit is used in conjunction with Graphics Mode register bit 6 for 256 color mode support.

5.9.6 PR5 - Unlock Graphics Controller Extended Paradise Registers

Read/Write Port = 3CFh, Index = 0Fh

BIT	FUNCTION
7	CNF (7) Status
6	CNF (6) Status
5	CNF (5) Status
4	CNF (4) Status
3	CNF (8) Status
2	PR0-PR4, PR57-PR62 Unlock
1	PR0-PR4, PR57-PR62 Unlock
0	PR0-PR4, PR57-PR62 Unlock

Bit 7:3

These are configuration bits that, at time of reset, reflect the pulled up/pulled down state of the configuration bits given in the following list. Refer to the Section 6 discussion of hardware configuration options to interpret the reading of these bits.

BIT	FUNCTION
7	= CNF(7) [Read Only]
6	= CNF(6)
5	= CNF(5)
4	= CNF(4)
3	= Inverse of CNF(8)

Bits 2:0

Control writing to registers PR0-PR4 as follows:

BITS 2:0			PR0-PR4
0	X	X	Write-protected
X	1	X	Write-protected
X	X	0	Write-protected
1	0	1	Writing enable of PR0-PR4

Cleared to 0 at reset.

5.9.7 PR10 - Unlock PR11 through PR1A Register

Read/Write Port = 3?5h, Index = 29h
Read Unlock: PR10(3?5.29h) = 1xxx0xxx

This register is read/write and cleared to 0 by reset. PR11 through PR17 can be loaded if it contains XXXXX101. PR10 through PR17 can be read only if it contains 1XXX0XXX. Bits 7 and 3 enable register read operation for PR10 through PR17. Bits (6:4) may be used as scratch pad. Bits (2:0) enable register write operation for PR11 through PR17.

BIT	FUNCTION
7	PR11 - PR17 - Read Enable Bit 1
6:4	Scratch Bits/Mfg Test
3	PR11 - PR17 - Read Enable Bit 0
2:0	PR11 - PR17 - Write Enable

This eight bit register is READ/WRITE and cleared to 0 by hardware reset.

Bit 7,3

These bits enable reading registers PR10 through PR17.

7	3	PR11-PR17
0	X	Read-protected, read FFh.
X	1	Read-protected, read FFh.
1	0	Reading enabled.
Also, bit 7 must be set to 1 in order to read the device ID (refer to Section 6.17).		

Bit 2:0

These bits enable writing to registers PR11 through PR17.

2	1	0	PR11-PR17
0	X	X	Write-protected.
X	1	X	Write-protected.
X	X	0	Write-protected.
1	0	1	Writing enabled.

Bits 6:4

These bits may be used as a scratch pad, but the bit combination X101XXXX is reserved for manufacturing test.

6	5	4	PR10(6:4)
0	X	X	Scratch Pad
X	1	X	Scratch Pad
X	X	0	Scratch Pad
1	0	1	Reserved
Also, bit 4 must be set to 0 in order to read the device ID (refer to Section 6.17).			

5.9.8 PR11 - Configuration Bits Register

Read/Write Port = 3?5h, Index = 2Ah
Unlock: PR10 (3?5.29h) = 85h

Configuration details are stored in the PR11 register bits as well as controls related to panel support.

BIT	FUNCTION
7	CNF15
6	CNF14
5	CNF13
4	CNF12
3	Reserved
2	Lock Clock Select
1	Lock Graphics and Sequencer Screen Control
0	Lock 8/9 Character Clock

Bit 7:4

Configuration Bits [CNF(15) through CNF(12)]

These bits are read/write and latched internally at power-on-reset from corresponding memory data bus pins BMD(7:4), which must be provided with either pull-up or pull-down external resistors. For addition information on hardware configuration, refer to Section 6.

Bit 3

Reserved

Must be set to 0 on writes to PR11. Undefined on reads.

Bit 2

Lock Clock Select

When set to 1, this bit:

- Prevents modification of VGA Miscellaneous Output register bits 2 and 3.
- If the internal clock multiplexer is used, it prevents changing of the clock input selection.
- If an external clock IC is used, it prevents toggling of VCLK controls to the external clock IC.

Bit 1

Lock Graphics Controller & Sequencer Screen Control

When PR11 register bit 1 is set to 1, modification of the following bits of other registers is prevented:

Graphics Controller	3CF.05	bits (6:5)
Sequencer	3C5.01	bits (5:2)
Sequencer	3C5.03	bits (5:0)

Although the internal functions selected by these Graphics Controller and Sequencer bits are locked by setting PR11 register bit 1 to 1, these bits appear to the system processor as unlocked when being read.

Bit 0

Lock 8/9 dots

Setting this bit to 1 locks the VGA Clocking Mode register (3C5.01h bit 0). Although 8- or 9-dot character timing is locked by setting this bit (PR11 bit 0) to 1, 3C5.01h bit 0 still appears to the system processor as unlocked.

NOTE

For Flat-panel or Simultaneous display, 8-dot character timing should be selected and then locked by using this bit.

5.9.9 PR12 - Scratch Pad Register

Read/Write Port = 3?5h, Index = 2Bh
Unlock: PR10 (3?5.29h) = 85h

This 8-bit read/write register can be loaded only if PR10 contains xxxxx101, and can be read only if PR10 contains 1xxx0xxx.

BIT	FUNCTION
7:0	Scratch Pad Bits (7:0)

Bit 7:0

The data in this register is unaffected by hardware reset and undefined at power up.

5.9.10 PR13 - Interlace H/2 Start Register

Read/Write port = 3?5h, Index = 2Ch
Unlock: PR10 (3?5.29h) = 85h

BIT	FUNCTION
7:0	Interlaced H/2 Start

This 8-bit READ/WRITE register can be loaded only if PR10 contains xxxxx101, and can be read only if PR10 contains 1xxx0xxx.

The data in this register is unaffected by hardware reset and undefined at power up. This register defines the starting horizontal character count at which vertical timing is clocked on alternate fields in interlaced operation. Interlaced operation is enabled by setting PR14(5) to 1.

All other standard non-interlaced modes are unaffected by the contents of this register.

This register must be programmed with a value derived from the values chosen to be programmed into the Horizontal Retrace Start Register (3?5.04h) and Horizontal Total Register (3?5.00h):

PR13(7:0) = [HORIZ RET START] - [(HORIZ TOT + 5) / 2] + HRD

NOTE

In the above expression, HRD = Horizontal Retrace Delay, defined by bits 6 and 5 of the Horizontal Retrace End Register (3?5.05).

5.9.11 PR14 - Interlace H/2 End Register

Read/Write Port = 3?5h, Index = 2Dh
Unlock: PR10 (3?5.29h) = 85h

BIT	FUNCTION
7	Enable IRQ
6	Vertical Double Scan for EGA on PS/2 Display
5	Enable Interlaced Mode
4:0	Interlaced H/2 End

This 8-bit read/write register can be loaded only if PR10 contains xxxxx101, and can be read only if PR10 contains 1xxx0xxx. Bits 7 through 5 are cleared to 0 by reset.

Bits 4 through 0 are unaffected by hardware reset and undefined at power up. Bits 7 through 5 are cleared to 0 by reset.

Bit 7

Enable IRQ

When this bit is set to 1, the IRQ/$\overline{\text{IRQ}}$ pin is tristated.

This bit may be set to enable CRT interrupts to be generated when configured for ISA(AT) BUS operation. For VGA operation with an ISA(AT) BUS, interrupts are usually not used, and this bit should be set to 0. This bit should be set to 1 for Micro-Channel operation.

Bit 6

Vertical Double Scan

This bit should be set to 1 when emulating EGA on a PS/2 display.

Setting this bit to 1 causes the CRTC Vertical Displayed line counter and Row Scan counter to be clocked by divide-by-two horizontal timing if Vertical Sync polarity is programmed positive [3C2h bit 7=0].

Therefore, the relationship between the actual number of lines displayed [N] and the data [n] programmed into the Vertical Display Enable End register is:

N = 2(n+1)

Likewise is the relationship between the actual number of scan lines per character row [N] and the data [n] programmed in the Maximum Scan Line register.

Usually, this bit is set to 0.

Bit 5

Interlaced Mode

Setting this bit to 1 selects interlaced mode. Interlaced mode can be used in those video modes in which the data programmed into the Maximum Scan Line Address register [3?5.09] = 0xx00000. Line compare and double scan are not supported.

Bits 4:0

Interlace H/2 End Bits (4:0)

Add the contents of the Interlace H/2 Start Register to the horizontal sync width (same as defined by 3?5.04h,05h), and program the 5 LSB of the sum into these bits.

5.9.12 PR15 - Miscellaneous Control Register 1

Read/Write Port = 3?5h, Index = 2Eh
Unlock: PR10 (3?5.29h) = 85h

BIT	FUNCTION
7	Read 46E8 Enable
6	Low VCLK
5	VCLK1, VCLK2 Latched Outputs
4	VCLK = MCLK
3	8514/A Interlaced Compatibility
2	Enable Page Mode
1	Select Display Enable
0	Disable Border

This 8-bit READ/WRITE register can be loaded only if PR10 contains xxxxx101, and can be read only if PR10 contains 1xxx0xxx.

Bit 7

Enable reading port 46E8h

This bit is functional only if ISA(AT) BUS architecture [CNF(2)=1] is selected.

Setting this bit to 1 enables I/O port 46E8h to be read, regardless of the state of its own bits 3 and 4 and of port 102 bit 0 (sleep bit). Only bits (4:0) of port 46E8 are readable; bits (7:5) are 0.

Bit 6

Low VCLK

Setting this bit to 1 adjusts the memory timing to allow use of a video clock (VCLK) frequency which is much lower than the memory clock (MCLK) frequency (such as LCD applications). This bit should be set to 1 if the selected VCLK frequency is less than half of the MCLK frequency.

Bit 5

This bit is used only if CNF(3)=1, configuring pins 54 and 55 as outputs. Setting this bit to 1 causes pins 54 and 55 to equal bits 2 and 3, respectively, of I/O write register 3C2 (Miscellaneous Output).

Bit 4

Select MCLK as the Video Clock

Setting this bit to 1 causes the MCLK input to become selected for the source of all video timing. None of the three VCLK inputs can be selected when this bit is set.

Bit 3

8514/A Interlaced Compatibility

This bit should be used only if interlaced mode is selected (see PR14). If exact timing emulation of the IBM 8514/A's interlaced video timing is required, set this bit to 1. This setting causes vertical sync to be generated from the trailing edge of non-skewed horizontal sync, instead of the leading edge, as generated for VGA timing. It also removes two VCLK delays from the default VGA video dot path delay chain.

Bit 2

Select Page Mode Addressing

Setting this bit to 1 forces screen refresh memory read cycles to use page mode addressing in alphanumeric modes. Page mode addressing is automatically used in graphics modes. Page mode addressing requires less time than RAS-CAS addressing; therefore, selecting page mode addressing increases the bandwidth for the CPU to access video memory by 30 to 40%.

This bit must be set to 1 if 132-character mode timing is selected (see description of PR2).

Setting this bit overrides the Character Map Select functions of PR2(2) and PR2(5).

Setting this bit to 1 redefines the Character Map Select Register (3C5.03). One of eight, 8K memory segments containing a pair of maps in Plane 2 and Plane 3 is addressed by bits (2:0) of this register, and the map selected is determined by bits (4:3). A pair of adjacent 8K character maps in Planes 2 and 3 (adjacent in the sense that they have the same addressing) may be selected by bit 3 of the attribute code.

Character attribute bit 3, in conjunction with bits 3 and 4 of the Character Map Select Register (3C5.03), selects a character map from either Plane 2 or Plane 3:

3C5.03h Bit 4	3C5.03h Bit 3	Attribute (3)	Selects Plane
0	0	X	2
1	1	X	3
1	0	0	2
1	0	1	3
0	1	0	3
0	1	1	2

NOTE

The above Character Map Select functions override the functions of PR2(5) and PR2(2). This bit must be set to 1 before loading the character maps into video DRAM, because the addressing of the page mode character plane differs from addressing of the default, non-page mode. However, setting this bit to 1 internally redirects all necessary addressing to make loading the character maps the same, whether page-mode or non-page mode.

Bit 1

Display Enable Timing Select

This bit is used to select between two types of Display Enable timings available at output pin FR/$\overline{\text{BLANK}}$ if PR4(7)=1. If PR4(7)=0, this bit has no effect.

0 = FR/$\overline{\text{BLANK}}$ supplies Pre-Display Enable. Pre-Display Enable timing precedes active video by one dot clock.

1 = FR/$\overline{\text{BLANK}}$ supplies Display Enable. Display Enable timing coincides with active video timing.

Bit 0

Disable Border

Setting this bit to 1 forces the CRT and panel video outputs to 0 (black) during the interval when border (overscan) color would be active.

5.9.13 PR16 - Miscellaneous Control Register 2

Read/Write Port = 3?5h, Index = 2Fh
Unlock: PR10 (3?5.29h) = 85h

This 8-bit READ/WRITE register can be loaded only if PR10 contains xxxxx101, and can be read only if PR10 contains 1xxx0xxx. All bits are cleared to 0 by reset.

BIT	FUNCTION
7	External register 46E8h lock
6	CRTC Address Count Width bit 1
5	CRTC Address Count Width bit 0
4	CRTC Address Counter Offset bit 1
3	CRTC Address Counter Offset bit 0
2	Enable Odd/Even Page bit
1	VGA Mapping Enable
0	Lock RAMDAC Write Strobe

Bit 7

Lock External 46E8 Register

Setting this bit to 1 disables output $\overline{\text{EBROM/46E8}}$ pin from going active low during I/O writes to port 46E8h. This bit has no effect on accesses to the internal port 46E8 register.

Bits 6:5

CRTC Address Counter Width

Power-on-reset clears these bits to 0. These two bits determine the modulus of the CRT Controller's Address Counter, allowing its count width to be limited to 64K or 128K locations (byte, word, or double-word).

These bits may be used in virtual VGA applications containing 512K of video memory in which it is required to limit the memory access by the CRT Controller to only 64K or 128K locations.

Bit PR16(6) should be set to 1 to ensure VGA-compatible operation of the Address Counter, limited to 64K locations.

PR16(6)	PR16(5)	COUNT WIDTH
0	0	256K
0	1	128K
1	X	64K

Bits 4:3

CRTC Address Counter Offset

Bits 4 and 3 are summed with the CRT Controller's Address Counter bits CA(17) and CA(16), respectively, and the 2-bit result defines the starting location of the displayed video buffer at one of four 64K boundaries.

Bit 2

Enable Page Bit for Odd/Even

This bit affects addressing of memory by the system processor if chain 2 (odd/even) has been selected by setting one of the following:

- 3CF.06(1) to 1
- 3C5.04(1) has been set to 1,
- selecting Extended Memory, and 3C5.04(3) is 0,
- deselecting chain 4 addressing.

It enables the Page Bit for Odd/Even [3C2(5)] to select between two pages of memory by controlling video RAM address 0, regardless of the Memory Size bits PR1(7:6).

This bit should be set to 0 for suggested memory implementations.

Bit 1

VGA Memory Mapping

Setting this bit to 1 selects 256K IBM VGA mapping, regardless of the Memory Size bits PR1(7:6). Refer to the description of PR1.

Bit 0

Lock RAMDAC Write Strobe (3C6h through 3C9h)

Setting this bit to 1 causes output $\overline{\text{WPLT}}$ to be forced to 1, disabling I/O writes to the Internal RAMDAC registers. The Internal RAMDACs State register, located inside the WD90C26A, is also protected from modification but may still be read at port 3C7h.

5.9.14 PR17 - Miscellaneous Control Register 3

Read/Write Port = 3?5h, Index = 30h
Unlock: PR10 (3?5.29h) = 85h

This two bit register can be loaded only if PR10(3?5.29h) contains XXXXX101, and can be read only if PR10 contains 1XXX0XXX.

BIT	FUNCTION
7:2	Reserved
1	MDA Compatibility
0	Map out 2 Kbyte from BIOS ROM

Bit 7:2

Reserved

Bit 1

MDA Compatibility Enable Bit

Setting this bit to 1 enables MDA compatibility by:

1. disabling I/O writes to the Hercules register(3BF).
2. forcing bit 7 of 3BA to 1.
3. causing the underline decode attribute to XXXXX001 (if this bit is 0, underline decode is X000X001).

Hardware reset sets this bit to 0.

Bit 0

Map out 2K of BIOS ROM.

Setting this bit to 1 disables $\overline{\text{EBROM}}$ decode of the BIOS ROM in the system address range C6000 through C67FF. Reset sets this bit to 0.

Clearing this bit to 0 enables $\overline{\text{EBROM}}$ decode of all 32K addresses of BIOS ROM, from C0000 through C7FFF if PR1 register bit 0 is set to 0.

5.9.15 PR18 - Flat Panel Status Register

Read/Write Port = 3?5h, Index = 31h
Unlock: PR1B (3?5.34h) = A0h/A6h

This register is used to select different flat panel support features. These parameters should be locked after loading.

BIT	FUNCTION
7	DAC Shut Off
6	Enable Free Running Clock
5	Enable 256K Colors STN Dithering
4	Select TFT Panel Data Polarity and Enable Reverse Video
3	Enable Highest Contrast
2	TFT Color LCD Select
1:0	Flat Panel Select

Bit 7

DAC Shut Off

This bit is used to shut off the internal DAC outputs. Usually, the DAC is shut off whenever PR19 bit 5 is low. Should an external DAC be used, the setting of this bit keeps the internal DAC disabled even when PR19 bit 5 is high.

0 = The internal DAC is enabled as normal.
1 = The internal DAC is held disabled.

Bit 6

Enable Free Running Shift Clock

This bit allows the XSCLK shift clock to free-run instead of being disabled during blanking periods.

For most plasma and TFT panels, this bit is set to 1.

0 = Disable free running clock.
1 = Enable free running clock.

Bit 5

Enable 256K Colors in STN Dithering

This bit is used to select color palette size for color STN multiplexed panel support. Usually, this bit is set to 1. However, it may be set to 0 for a smaller dithering palette for use with panels where the appearance is improved by 4K dithering.

0 = Select 4K color palette dithering.
1 = Select 256K color palette dithering

Bit 4

Select TFT Panel Data Polarity and Enable Reverse Video

This bit is used to Select TFT panel data polarity, and in conjunction with PR39 bit 3, to enable reverse video in flat panel mode. For best viewing of a flat panel display, it is often desirable to have the panel display in reverse video for text display. The the setting of PR18 register bit 4 along with PR39 register bit 3 in the following table allow selection of conditions for text and graphics displays in reverse image on a panel.

Normally a setting of '11' should be used for reverse image text and normal image graphics (11).

The settings of PR18 register bit 4 and PR39 register bit 3 do not affect CRT display.

PR18 Bit 4	PR39 Bit 3	Panel Display Polarity
0	x	TFT Panel Data active high
1	x	TFT Panel Data active low
0	0	Normal text and graphics
0	1	Reserved
1	0	Reverse image text and graphics
1	1	Reverse image text, and normal image graphics
NOTE: x indicates don't care.		

NOTE

Reverse image settings are not recommended for color panels. For color panels. PR18 register bit 4 and PR39 register bit 3 should both be set to 0 for color panel support.

Bit 3

Enable highest contrast intensity in text mode.

Normal text in VGA text modes is not set to maximum intensity. Since contrast of most flat panels is limited, it is often desirable to display normal text at the maximum possible contrast for best readability. When this bit is set to 1, normal text is displayed at full contrast or brightness instead of the normal VGA text intensity.

1 = Maximum intensity in text mode.
0 = Normal VGA text contrast.

The setting of bit 3 does not affect CRT contrast nor brightness.

Bit 2

TFT color LCD Select

Configures the panel interface for supported TFT panels by selecting TFT dithering and the 9 or 12 bit TFT panel interface. This bit should be set to 1 for color TFT active matrix panel support and to 0 for multiplexed STN color panel support.

1 = Enable TFT type color LCD panel interface. Color TFT Active Matrix panel support enabled.

0 = Disable TFT type color LCD panel interface. Multiplexed STN color panel support enabled.

Bits1:0

Panel Select Bit 1 and Bit 0

Configures the panel interface for a particular panel type.

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PSB(1)	PSB(0)	
0	0	Dual panel passive matrix monochrome LCD display.
0	1	Plasma display.
1	0	EL display.
1	1	Single panel LCD display.

Bits 1 and 0 are initialized at reset as CNF(9) and CNF(11), respectively. If BMD1 is high during reset, PR18 register bit 1 is initially set to 1. Also, if BMD0 is high during reset, PR18 register bit 0 is initially set to 1.

5.9.16 PR19 - Flat Panel Control I Register

Read/Write Port = 3?5h, Index = 32h
Unlock: PR1B (3?5.34h) = A0h/A6h

BIT	FUNCTION
7	Plasma Panel Select/Hsync Timing Select
6	FP Timing Select
5	CRT Display Enable
4	Flat Panel Display Enable
3	Screen Auto-Center/Vertical Expand
2	Enable Auto Center/Vertical Expand
1:0	Adjustment of LP Timing

Bit 7

Plasma Panel Type Select

When in plasma mode (PR18[1:0], this bit is used to select either a 4-bit or 8-bit Plasma panel interface.

0 = Select 4 data bits/single pixel interface.
1 = Select 8 data bits/two pixels interface.(4 bits per pixel)

This bit also determines the range of HSYNC delay selectable by programming bits 1 and 0.

Bit 6

FP Timing Select

This bit is used to select from two different FP (frame pulse) occurrence times. Some panels require that the FP pulse be activated at the first horizontal line and other panels require waiting until the first line is filled and the second line has begun.

BIT 6	FP TIMING SELECT
0	FP pulse occurs during first horizontal line
1	FP pulse occurs during second horizontal line

This bit also affects the HSYNC timing delay (refer to the description of bits 1:0 for this register).

Bit 5

CRT Display Enable

This bit is used to enable CRT display support circuitry.

0 = Disable CRT display (default value at reset)
1 = Enable CRT display

NOTE

For saving power, this bit (PR19 bit 5) should be set to 0 whenever CRT display is not required.

Bit 4

Flat Panel Display Enable

This bit is used to enable the flat panel display.

0 = Disable Flat Panel display
1 = Enable Flat Panel display (value after reset).

NOTES

1. For saving power, this bit (PR19 bit 4) should be set to 0 whenever flat panel display is not required.
2. For simultaneous display on flat panel and CRT, PR19 register bits 4 and 5 should both be set to 1.

Bit 3

Screen auto-centering/vertical expansion select.

Selects whether a panel display with fewer than 480 lines is automatically centered or vertically expanded when PR19 register bit 2 is set.

0 = Auto-centering (default value at reset).
1 = Vertical expansion.

Bit 2

Enable auto-centering & vertical expansion

Enables either vertical expansion or auto-centering as determined by the setting of PR19 register bit 3.

0 = Disable (default value at reset).
1 = Enable.

NOTE

In simultaneous display, vertical expansion should be normally enabled. This allows CRT and LCD displays that have fewer than 480 lines to fill the full screen.

Bits 1:0

Adjustment of HSYNC Timing

Bits 1 and 0 are used in conjunction with bit 7 to program a delay of the HSYNC pulse position in one VCLK (one dot) increments. This is used to horizontally adjust the position of the picture displayed on flat panels. This LP timing adjustment does not affect the delay of the LP signal to panels.

PR19			Number of VCLK Delay of Hsync
BIT 7	BIT 1	BIT 0	
0	0	0	No Delay
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

5.9.17 PR1A - Flat Panel Control II Register

Read/Write Port = 3?5h, Index = 33h
Unlock: PR1B (3?5.34h) = A0h/A6h

BIT	FUNCTION
7:3	Scratch Pad Bits
2	Reserved
1	Select # of Memory Refresh Cycles
0	Select Mem Refresh Cycles Control

Bit 7:3

Scratch Pad Bits

These bits may be written and read as needed.

Bit 2

Reserved

Must be set to 0 on writes. Undefined on reads.

Bit 1

Select Number of Memory Refresh Cycles

This bit (PR1A bit 1) allows selection of the number of refresh operations to occur during horizontal retrace when PR1A register bit 0 is set to 1. Setting PR1A register bit 0 to 1 overrides the standard number of retrace operations produced by the CRTC.

0 = Select one memory refresh cycle per horizontal line.

1 = Select two memory refresh cycles per horizontal line.

Bit 0

Select Memory Refresh Cycles Control

The CRT controller normally generates three refresh operations per horizontal retrace interval. If this bit (PR1A, bit 0) is set to 1, the normal number of refresh cycles is overridden and the state of PR1A register bit 1 determines the number of refresh operations to occur during horizontal retrace.

Reducing the number of refresh cycles can increase memory bandwidth and reduce power consumption during power down operations.

0 = Number of memory refresh cycles per refresh operation controlled by the CRT controller.

1 = Number of memory refresh cycles per refresh operation controlled by PR1A register bit 1.

5.9.18 PR1B - Flat Panel Unlock Register

Write Only Port = 3?5h, Index = 34h

BIT	FUNCTION
7:0	Flat Panel Unlock

Bit 7:0

This register is used to read/write protect PR18, PR19, PR1A, PR36-PR41, and PR44. To read (write) these registers, PR1B must be loaded first with 101XXXXX. PR18, PR19, PR1A, PR30, PR36, PR37, PR39, PR41 and PR44 remain unlocked until a different value is written to the PR1B register.

NOTE

The flat panel registers must be locked in order to read the device ID (refer to Section 6.17).

PR1B is also used to lock all shadow registers. In order to unlock shadow registers, PR1B must be loaded first with XXXXX110. Refer to Section 6 for a description of the shadow registers and under what conditions they are to remain locked or unlocked.

5.9.19 PR20 - Unlock Sequencer Extended Registers

Write Only Port = 3C5h, Index = 06h

BIT	FUNCTION
7:0	Unlock Sequencer Extend

A value of X1X0 1XXX (48h) must be loaded to allow read/write of the Sequencer Extended registers PR21, 30A, 31, 32, and 34A.

A read of the Sequencer Index register can be used to indicate whether or not the Sequencer Extended Registers are locked. When the Sequence Extended registers are locked, the Sequencer Index register is readable as three bits only. When unlocked, a Sequencer index read returns a 6-bit value. Therefore, the locked or unlocked status of the Sequencer Extended registers can be checked by first writing a 6-bit value to the Sequencer Index register. Then, reading to see whether a 3-bit or a 6-bit value is returned. Any 6-bit value would indicate that the Sequencer Extended registers are unlocked.

5.9.20 PR21 - Display Configuration Status and Scratch Pad Register

Read/Write Port = 3C5h, Index = 07h
Unlock: PR20 (3?5.06h) = 48h.

BIT	FUNCTION
7:4	Scratch Pad Bits
3:0	Reserved

Bits 7:4

Scratch Pad Bits

Read/Write scratch pad for any BIOS status data that may need to be saved. Reset state is 1111.

Bits 3:0

Reserved

Should be set to 0 on writes. Undefined on reads.

5.9.21 PR30 - Mapping RAM Unlock

Read/Write Port = 3?5, Index 35h

Unlock: PR1B (3?5.34h) = A0h/A6h

BITS	FUNCTION
7:0	Mapping RAM Unlock

This register is used to protect mapping RAM registers (PR33 through PR35) from being accessed. To read or write to these registers, PR30 must be loaded first with 30h (X011 XXXX); all mapping RAM registers remain unlocked until a different value is written to the PR30 register.

NOTE

The Mapping RAM registers must be locked in order to read the device ID (refer to Section 6.17).

5.9.22 PR30A - Memory Interface Write Buffer and FIFO Control Register

Read/Write Port = 3C5h, Index = 10h
Unlock: PR20 (3?5.06h) = 48h

BITS	FUNCTION
7:6	Reserved
5	8- or 16-bit memory data path
4	Reserved
3	Write buffer extension enable
2	4- or 8-level FIFO
1:0	Display memory bandwidth

This register controls display memory data width and its bandwidth. All of the bits are reset to zero at power on reset

Bit 7:6

Reserved. Should be set to 0 on writes to PR30A. Undefined on reads.

Bit 5

8- or 16-Bit Memory Data Path

When set to 1, the video DRAM memory data path becomes 16 bits wide, using both Bank A and Bank B video memory data buses. Otherwise, the data path is 8 bits wide using Bank A only. This bit should be set to 1 when a 256 K x 16 DRAM is being used or four 256K x 4 DRAMS are being used for 512K of video memory. In any other case, this bit should be set to 0.

Bit 4

Reserved. Must be set to 0.

Bit 3

Enable Write Buffer Extension

0 = Disables the write buffer extension.
1 = Enables the write buffer extension.

This makes the write buffer for system writes to the WD90C26A effectively two write cycles deep. This bit should be set to 1 under normal conditions.

Bit 2

4- or 8-Level FIFO

0 = FIFO set to 8 levels deep
1 = FIFO set to 4 levels deep.

When 16-bits of DRAM memory are available the 4-level FIFO depth should be used. In Super VGA modes, such as 800 x 600 x 256K color, an 8-level FIFO depth is required and this bit should be set to 0.

Bit 1:0

Display Memory Bandwidth

These two bits are used to tune the display memory bandwidth. Bits 1 and 0 should be set to 0 and 1, respectively, to accommodate most applications.

These two bits have no effect in any text mode. When text mode is selected, bits 1 and 0 are overridden to 00 internally.

BIT	FUNCTION	Levels
00	FIFO requests video memory cycle when FIFO is:	one level empty
01	FIFO requests video memory cycle when FIFO is:	two levels empty
10	FIFO requests video memory cycle when FIFO is:	three levels empty
11	FIFO requests video memory cycle when FIFO is:	four levels empty

5.9.23 PR31 - System Interface Control Register

Read/Write Port = 3C5h, Index = 11h
(Reset State = 00h)
Unlock: PR20 (3C5.06h)=48h

This register provides the control bits for the system interface. It should be set during the post-initialization routines of the VGA BIOS.

BIT	FUNCTION
7	Read/Write Offset Enable
6	Turbo Mode for Blanked Lines
5	Turbo Mode for Text
4	CPU Read RDY Release Control 1
3	CPU Read RDY Release Control 0
2	Enable 16-bit Write Buffer
1	Enable 16-bit Video Attribute Controller
0	Enable 16-bit CRTC, Sequencer, and Graphics Controller Registers

Bit 7

Read/Write Offset Enable

Bit 7 is used during some of the enhanced video modes.

0 = Normal (Refer to PR0(A) and PR0(B) definitions in Section 5.9.1).
1 = The offset register PR0(A) value is added to CPU address for read cycles, while PR0(B) is added for write cycles.

Bit 6

Turbo Mode for Blanked Lines

1 = System performance is improved by 10% by removing extra screen refresh memory cycles on vertical blank.
0 = Normal refresh cycles during vertical blanking.

Bit 5

Turbo Mode for Text

1 = Improves Text mode performance.
0 = Normal.

Bits 4:3

CPU Read RDY Release Controls 1,0

Bits 4 and 3 set the CPU IOCHRDY or CDCHRDY timing to be optimized for different system timing.- For slower host systems, to prevent read cycles from taking longer than necessary, it may be desirable to reactivate the IOCHRDY or CDCHRDY signal early.

For 10 MHz or slower host system bus speed, the recommended settings for bits 4 and 3 are 0 and 1, respectively.

For 12 MHz or faster host system bus speed, the recommended settings for bits 4 and 3 are 1 and 1, respectively.

BIT 4	BIT 3	FUNCTION
0	0	Power on reset condition. IOCHRDY or CDCHRDY is reactivated at the end of a CPU memory cycle
0	1	IOCHRDY or CDCHRDY is reactivated one MCLK before the end of a CPU memory cycle.
1	0	IOCHRDY or CDCHRDY is reactivated two MCLKs before the end of a CPU memory cycle.
1	1	IOCHRDY or CDCHRDY is reactivated one MCLK after the end of a CPU memory cycle.

Bit 2

Enable 16-bit Write Buffer

1 = The 16-bit Write buffer is enabled. This greatly reduces the number of wait states for CPU writes to display memory.

0 = The 16-bit Write buffer is disabled

Bit 1

Enable 16-Bit Video Attribute Controller

For 16-bit reads and writes, the Attribute Controller index and data are located at port addresses 3C0h and 3C1h, respectively, and the address toggle is disabled. The 16-bit chip select ($\overline{\text{IOCS16}}$ for the ISA bus and CDDS16 for the MicroChannel bus) is asserted for all cycles to port addresses 3C0h and 3C1h.

1= Attribute Controller is configured for 16-bit reads and writes. Use with bit 0 to enable 16-bit reads and writes.

0= Attribute Controller is configured for 8-bit reads and writes. The address toggle operates in the standard way for 8-bit cycles.

Bit 0

Enable 16-bit CRTC, Sequencer and Graphics Controller registers.

Allows the 16-bit chip select ($\overline{\text{IOCS16}}$ for the ISA bus and CDDS16 for the MicroChannel bus) to be asserted for all cycles to port addresses for the CRTC, Sequencer, and Graphics Controller registers. This also applies to PR registers that use CRTC, Sequencer, or Graphics Controller Index/Data I/O addresses.

1 = Enables 16-bit reads and writes to the following registers:

- CRTC registers 3?4h and 3?5h
- Sequencer registers 3C4h and 3C5h
- Graphics Controller registers 3CE and 3CF

0 = I/O is all 8-bit to the listed registers.

NOTE

This bit (PR31 bit 0) must be set to 0 for mapping RAM access via PR33 and PR34.

5.9.24 PR32 - Miscellaneous Control 4 Register

Read/Write Port = 3C5h, Index=12h
Unlock: PR20 (3C5.06h) = 48h

This register provides control of miscellaneous features in the WD90C26A.

BIT	FUNCTION
7	Reserved
6	Cursor blink
5	Reserved
4	Reserved
3	$\overline{\text{0WS}}$ Control High
2	$\overline{\text{0WS}}$ Control Low
1	Compatible Read Back Enable
0	Standard Addressing, 132 Columns

Bit 7

Reserved

Should be set to '0' on writes to Miscellaneous Control register 4. Undefined on reads.

Bit 6

When set to 1, the text cursor blink is disabled and the cursor remains on. This option can be used if cursor blink is not desired.

Bit 5

Reserved

Should be set to 0 on writes to Miscellaneous Control register 4. Undefined on reads.

Bit 4

Reserved

Should be set to 0 on writes to Miscellaneous Control register 4. Undefined on reads.

Bit 3

$\overline{\text{0WS}}$ Control High

Provides the high order bit for the zero wait-state control setting.

Bit 2

$\overline{0WS}$ Control Low

Provides the low order bit for the zero wait-state control setting.

The settings for $\overline{0WS}$ (PR32 bits 3 and 2) control are listed in the following table.

BIT 3 $\overline{0WS}$ CTRL HIGH	BIT 2 $\overline{0WS}$ CTRL LOW	FUNCTION
0	0	$\overline{0WS}$ goes active-low for all write cycles*.
0	1	$\overline{0WS}$ becomes active low whenever the system address is within the VGA address range of A000-BFFF*.
1	0	$\overline{0WS}$ goes active low in response to MEMW becoming active low if the system address is within the VGA address range and the internal system write buffer is not full.
1	1	$\overline{0WS}$ goes active low*, in response to either of the following: a) $\overline{MEMW}$ going active low when the system address is within VGA memory range. b) $\overline{IOW}$ going active low when the I/O address is within the VGA I/O register space.

*Unless the WD90C26A controller's internal system write buffer is full.

Setting bits 2 and 3 does not affect MicroChannel timing.

Bit 1

Compatible Read Back Enable

When set to 1, this bit allows reading the registers that are usually not readable in Hercules, MDA, or CGA compatibility modes. This option may be used either as a test feature or by the BIOS during mode changes.

Bit 0

Standard Addressing, 132 Column

Used only for video memory virtual page applications. This bit allows setting of the page mode font access for 132 column modes to occur at the virtual memory 1 Mbyte page or at the standard below-1-Mbyte video addresses.

1=Enables address mapping for page mode font access in 132-column text. This bit is set for standard mapping without disturbing the display. For additional 132-column (character) mapping refer to PR15 register bit 2 and PR2 register bits 3 and 4.

0=Disables address mapping for page mode font access in 132-column text.

5.9.25 PR33 - Mapping RAM Address Counter Register

Read/Write Port = 3?5, Index 38h
Unlock: PR30 (3?5.35h) = 30h

BIT	FUNCTION
7:6	Reserved
5:0	Mapping RAM Address Counter

This register is used to select the RAM Address Counter register.

NOTES

PR31 register bit 0 must be set to 0 before accessing the mapping RAM address counter.

Any I/O Read or Write to the PR34 Mapping RAM Data register (3?5.39h) increments the Mapping RAM Address Counter by one.

5.9.26 PR34 - Mapping RAM Data Register

Read/Write Port = 3?5, Index 39h
Unlock: PR30 (3?5.35h) = 30h

BIT	FUNCTION
7:6	Reserved
5:0	Mapping RAM Data

This register is used to read or write data to the mapping RAM location determined by the setting of PR33.

NOTE

PR31 register bit 0 must be set to 0 before accessing the mapping RAM address counter.

5.9.27 PR34A - Video Memory Virtual Page Register

Read/Write Port 3C5.14h
Unlock: PR20 (3C5.06h) = 48h

BITS	FUNCTION
7:4	Scratch Pad Bits
3:0	Video Memory Virtual Page

Bit 7:4

Scratch Pad Bits

Bit 3:0

Video Memory Address Virtual Page

Allows mapping of the below-1 Mbyte video memory address space to above 1 Mbyte system memory areas, in increments of 1 Mbyte offsets. This allows video memory to be accessed as virtual memory by applications supporting video memory operations at above 1 Mbyte addresses.

3	2	1	0	1 MBYTE PAGE
0	0	0	0	Standard below-1 Mbyte video addresses.
0	0	0	1	Video addresses remapped to 2nd Mbyte space.
0	0	1	0	to 3rd Mbyte space
0	0	1	1	to 4th Mbyte space
0	1	0	0	to 5th Mbyte space
0	1	0	1	to 6th Mbyte space
0	1	1	0	to 7th Mbyte space
0	1	1	1	to 8th Mbyte space
1	0	0	0	to 9th Mbyte space
1	0	0	1	to 10th Mbyte space
1	0	1	0	to 11th Mbyte space
1	0	1	1	to 12th Mbyte space
1	1	0	0	to 13th Mbyte space
1	1	0	1	to 14th Mbyte space
1	1	1	0	to 15th Mbyte space
1	1	1	1	to 16th Mbyte space

The default setting for bits 3:0 at reset is 0000 so that standard below-1Mbyte video memory access is enabled.

PR1 bits 4 and 5 must be set to 01h or 11h in order for video memory to be set to above-1-Mbyte addresses and the WD90C26A must not be in 12-bit TFT mode since LA23 through LA20 must be internally decoded for this feature.

5.9.28 PR35 - Mapping RAM Control and Power Down Register

Read/Write Port = 3?5h, Index = 3Ah
Unlock: PR30 (3?5.35h) = 30h

BITS	FUNCTION
7	Select Power Down Mode
6	Select Internal Clock (÷8)
5	Host Release During Power Down
4	Scratchpad Bit
3	Mapping RAM Bypass
2	Scratch Pad Bit
1	Enable Weighting Equation
0	Scratchpad Bit

Bit 7

Select Power Down Mode

If PR44 register bit 7 is set to 0, then this bit selects the type of powerdown mode to be entered when the $\overline{\text{PWRDOWN}}$ pin is activated.

0 = Display idle mode (default).
1 = System power down sleep mode.

Bit 6

Select Internal Clock (÷8)

When general power down modes are selected (PR44 register bit 7 is set to 1), this bit selects whether or not VCLK and MCLK are internally divided by 8 while $\overline{\text{PWRDOWN}}$ is active.

0 = Disable.
1 = Enable.

Bit 5

Host Release During Power Down

This bit is designed to allow another VGA controller on the I/O bus. When PR35 register bit 5 is set to 1 and the $\overline{\text{PWRDOWN}}$ input is low (active) the WD90C26A does not respond to any CPU memory or I/O access. The default value at reset is 0.

When $\overline{\text{PWRDOWN}}$ is low, all output buffers of the system interface are turned off including $\overline{\text{IOCS16}}$, $\overline{\text{MEMCS16}}$, IOCHRDY, and $\overline{\text{0WS}}$ and the IRQ output is tri-stated.

In MicroChannel mode, CDSFBK is also tri-stated and input 3C3D0 is disabled.

Bit 4

Scratchpad bit

Bit 3

Mapping RAM Bypass

Usually set to 0.

0 = Enables mapping RAM for programmable gray scale to gray shade mapping. for normal operation.

1 = Sets bypass mapping RAM for 1:1 gray scale to gray shade mapping. for monochrome LCD panels only.

NOTE

Mapping RAM bypass can be set to 1 for monochrome LCD panels only.

Bit 2

Scratch Pad Bit

Bit 1

Enable Weighting Equation

This bit is used to on/off toggle the color-to-gray scale weighting equation.

0 = Weighting equation is off. The six bits of green RAMDAC data are output instead of the weighting values.

1 = Standard NTSC color to monochrome weighting.

Normally, this bit should be set to 1. In monochrome video modes, contrast can be enhanced by setting this bit to 0.

Bit 0

Scratchpad Bit

5.9.29 PR36 - LCD Panel Height Select Register

Read/Write Port = 3?5h, Index = 3Bh
Unlock: PR1B (3?5.34h) = A0h/A6h

This register is used to select the height-per-single panel on dual-panel displays in order to implement auto-centering, vertical expansion and other related calculations.

The value programmed is the number of rows in one of the panels -1, which can also be expressed as (panel height/2)-1.

The Panel Height Select Register Value is not used for single panel display support

BIT	FUNCTION
7:0	LCD Panel Height Selection

Typical settings are shown in the following table.

PANEL	SETTING
640 x 480	EFh
640 x 400	C7h
640 x 350	AEh

NOTE

The default setting of PR36 at reset is 00h.

5.9.30 PR37 - Flat Panel Blinking Control Register

Read/Write Port = 3?5h, Index = 3Ch
Unlock: PR1B (3?5.34h) = A0h/A6h

This register is used to select cursor or character blinking rate on flat panel. In CRT mode, this register is ignored.

BITS	FUNCTION
7	LCD LP Signal Select
6	Shift-Clock Polarity Select
5:3	Character Blink-Rate Select
2:0	Cursor Blink-Rate Select

Bit 7

LCD LP Signal Select

Some panels require that the LP (Latch Pulse) signal be constant free-running while others require that LP stop at the last line at the bottom of the panel and start again at the first line on the top when the top line is refreshed. When this bit (PR37 register bit 7) is set to 1, the LP signal on the WD90C26A panel interface free-runs during retrace (blanking) intervals. This free-run occurs from the last line pulse at the bottom to the first line pulse at the top of the panel.

0 = LP is disabled during vertical blanking period.

1 = LP is generated continuously during vertical blanking period (XSCLK is turned off).

Bit 6

Shift Clock Polarity Select

Allows XSCLK polarity to be set so that it will make either a low-to-high or high-to-low transition at the time when panel data should be latched into the panel.

BIT 6	FUNCTION
0	Data changes with rising edge of XSCLK: data should be latched into panel by falling edge of XSCLK.
1	Data changes with falling edge of XSCLK: data should be latched into panel by rising edge of XSCLK.

Bit 5:3

Character Blink-Rate Select
Bits 5 through 3 select the character blink rate as given in the following list.

Bits [5:3]			CHARACTER BLINK-RATE SELECT
1	1	1	No character blinking
0	0	1	8 frames (8 on, 8 off)
0	1	0	16 frames (16 on, 16 off)
0	1	1	32 frames
1	0	0	64 frames
1	0	1	128 frames

Bit 2:0

Cursor Blink-Rate Select
Bits 2 through 0 select the cursor blink rate as given in the following list.

BITS [2:0]			CURSOR BLINK-RATE SELECT
1	1	1	No cursor blinking
0	0	1	8 frames (8 on, 8 off)
0	1	0	16 frames (16 on, 16 off)
0	1	1	32 frames
1	0	0	64 frames
1	0	1	128 frames

5.9.31 PR39 - Color LCD Control Register

Read/Write Port = 3?5, Index = 3Eh
Unlock: PR1B (3?5.34h) = A0h/A6h

This register is used to support color LCD panels.

BIT	FUNCTION
7	Enable Border LP Control
6	Color LCD Panel Border Select
5	Enable Color LCD Panel
4	Synchronous Extended I/O cycle
3	Enable Reverse Video
2	Enable CRT VSYNC and HSYNC
1	FP Polarity Select
0	LP Polarity Select

Bit 7

Enable Border LP Control

This bit is used to generate a special LP pulse to latch border information (black or white).

0 = Disable LP border control.
1 = Enable LP border control.

Bit 6

Color LCD Panel Border Select

0 = Select black border.
1 = Select white border.

Bit 5

Enable Color LCD Panel

This bit is used to select monochrome or color LCD interface support. When set to 1, this bit enables ENDATA for TFT panel, selects color panel FP, LP, and FR timing, and selects color dithering.

0 = Monochrome LCD panel interface.
1 = Color LCD panel interface.

Bit 4

Synchronous Extended I/O Cycle Enable

When in MicroChannel mode, this bit when set allows the WD90C26A to operate in Synchronous Extended I/O Cycle mode. CDCHRDY timing is modified accordingly.

This bit defaults to 1 at reset.

Bit 3

Enable Reverse Video

Refer to PR18 register bit 4.

Bit 2

Enable CRT VSYNC and HSYNC.

PR39 (2)	Pin 109 VSYNC	Pin 108 HSYNC
0	Inactive Hi	Inactive Hi
1	CRT VSYNC	CRT HSYNC

At reset, PR39 register bit 2 defaults to 1. Also, it may be set to 0 for power saving when CRT support is not needed.

Bit 1

FP Polarity Select

If PR39 (1)=0, then FP has normal polarity.
If PR39 (1)=1, then FP has reverse polarity.

Bit 0

LP Polarity Select

If PR39 (0)=0, then LP has normal polarity.
If PR39 (1)=1, then LP has reverse polarity.

5.9.32 PR41 - Vertical Expansion Initial Value Register

Read/Write Port = 3?5h, Index = 37h
Unlock: PR1B (3?5.34h) = A0h/A6h

BITS	FUNCTION
7:0	Vertical Expansion Initial Value

Bit 7:0

This register is used to decide which horizontal line is repeated in the very beginning when vertical expansion is enabled. It is very useful to implement smooth scrolling when 200, 350 or 400 line-mode displayed on a 480-line panel.

5.9.33 PR44 - Power-Down Memory Refresh Control Register

Read/Write Port = 3?5h, Index = 3F
Unlock: PR1B (3?5.34h) = A0h/A6h

This register is used to provide an extra power saving feature in general power down mode. During the power-down period, memory refresh is the only activity which is needed to prevent a loss of data. The power consumption of the CMOS chip is proportional to the clock frequency. PR44 is used to accelerate the memory refresh cycle when the external clocks gradually slow down in general power-down mode. PR35(6) is provided as an option to the system designer, when the designer wishes to select internal divided by 8 clocks instead of slowing down external clocks.

BIT	FUNCTION
7	General Power Down Mode Enable
6:0	Memory Refresh Cycle Period Select

Bit 7

General Power-Down Mode Enable Bit

This bit is used to select general power down mode (=1) or select the other power down modes (system power down mode, or display idle mode).

Bit 6:0

Memory Refresh Cycle Period Select

Controls the memory refresh cycle period when in general powerdown modes. The refresh period = (internally selected VCLK period) (8 or 9 dots/character) (PR44 value +5). For additional detail, refer to *Calculation of General Power Down Mode Refresh Timing*, in Section 6.6.5.

5.9.34 PR45 - Video Signature Analyzer Control Register

Read/Write Port = 3C5, Index = 16h
Unlock: PR20 (3?5.06h) = 48h

Bit	Function
7:4	Reserved
3	Unlock Signature Read Registers
2	Test Pattern
1	Initialize
0	Start

Bits 7:4

Reserved
Should be set to 0000 on writes to PR45. Undefined on reads.

Bit 3

Unlock Signature Read Registers

Setting this bit to 1 enables reading of PR45A and PR45B. The setting of this bit is readable.

Bit 2

Test Pattern

Setting this bit to 1 substitutes a fixed all zeros test pattern instead of the RAMDAC inputs into the signature analyzer. This all zeros test pattern

is used, along with the capability of initializing the signature to 0001, to test the signature analyzer circuit. Setting of this bit is readable.

Bit 1

Initialize

Setting this bit to a 0 causes an initialization of the signature analyzer by preloading the signature to 0001h. This bit must be set to 1 before a video signature can be generated. The setting of this bit is readable.

Bit 0

Start

Setting this bit to a 1 causes the signature analyzer to generate a signature of a video frame.

This bit must be set to 0 and then back to1 to restart generation of a new signature. The setting of this bit is readable.

5.9.35 PR45A - Signature Analyzer Data Low

Read/Write Port = 3C5, Index = 17h
Unlock: PR20 (3?5.06h) = 48h, PR45 bit 3 = 1.
Value after Reset: 01h.

Bit	FUNCTION
7:0	Low Data Byte

5.9.36 PR45B - Signature Analyzer Data High

Read/Write Port = 3C5, Index = 18h
Unlock: PR20 (3?5.06h) = 48h, PR45 bit 3 = 1.
Value after Reset: 00h.

Bit	FUNCTION
7:0	High Data Byte

5.9.37 PR57 - WD90C26A Feature Register I

Read/Write Port = 3CFh, Index = 10h
Unlock: PR5 (3C5.0Fh) = 05h

BIT	FUNCTION
7	Enable VGA Activity Detection
6	Select VGA Activity Detection Polarity
5	Self-Refresh
4:3	TFT Dithering Mode Select
2	Panel Power Control
1	PNLOFF/$\overline{\text{WPLT}}$ SELECT
0	Bank B Enable

Bit 7

Enable VGA Activity Detection

The VGA Activity Detection provides a hardware VGA device detection output signal that can be used for external power control and other applications. For example, it could control power to an LCD backlight.

This bit works with PR57 register bits 1 and 6, and with PR58 register bits 7:1 to provide VGA activity detection.:

PR57			
BIT 7	BIT 6	BIT 1	DESCRIPTION
0	x	0	Enable Panel Power Control (PNLOFF)
0	x	1	Enable External RAMDAC Write Strobe ($\overline{\text{WPLT}}$)
1	0	x	Enable VGA Activity Detect (VGADET) with high to low pulse. (Default)
1	1	x	Enable VGA Activity Detect (VGADET) with low to high pulse.

NOTES:

1. The x indicates Don't Care.
2. The PNLOFF., $\overline{\text{WPLT}}$, and VGADET signals are on connector pin 14.
3. All three bits are set to 0 at reset.
4. PR58 register bit 7:1 provide an activity detection counter. Refer to the PR58 description.
5. Any VGA I/O or memory cycle resets the counter and VGADET to its original state.

Bit 6

Select VGA Activity Detection Polarity

This bit works with PR57 register bit 7 to enable VGA Activity Detection. Refer to the previous list.

BIT 6	DESCRIPTION
0	Enable VGA detect on low to high pulse (Default)
1	Enable VGA detect on high to low pulse

Bit 5

Self-Refresh

The self-refresh control-high setting causes the power-down block REFRESH signal to go high.

This bit is write only.

Bits 4:3

TFT Dithering Mode Select

These bits are used with PR59 register bit 3 to select the mode of operation and colors for the 27K TFT dithering engine. Selection of modes depends upon the TFT interface as listed in Tables 5-18 and 5-19.:

PR57		PR59	
BIT 4	BIT 3	BIT 3	MODE
0	0	0	2-Frame Dithering, 27K Colors (Default)
0	0	1	2-Frame Dithering, 180K Colors
0	1	0	4-Frame Dithering, 27K Colors
0	1	1	4-Frame Dithering, 27K Colors
1	0	x	No Dithering, 512 Colors
1	1	0	Space Dithering, 27K Colors
1	1	1	Space Dithering, 180K Colors

TABLE 5-18 MODES FOR 9-BIT TFT

PR57		PR59	
BIT 4	BIT 3	BIT 3	MODE
0	0	x	2-Frame Dithering, 226K Colors (Default)
0	1	x	4-Frame Dithering, 226K Colors
1	0	x	No Dithering, 4K Colors
1	1	x	Space Dithering, 226K Colors

TABLE 5-19 MODES FOR 12-BIT TFT

Bit 2

Panel Power Control

When PR19 register bit 4 is set to 1 and PR57 register bit 1 is set to 0, setting this bit to 1 (2 times) causes the PNLOFF/$\overline{\text{WPLT}}$ pin to output a low.

Setting this bit to 0 (2 times) causes a high level to appear at PNLOFF/$\overline{\text{WPLT}}$ when the WD90C26A is not configured to operate as external RAMDAC (refer to bit 1).

This bit is set to 0 at reset causing PNLOFF/$\overline{\text{WPLT}}$ to go active high. PNLOFF automatically goes high whenever PR19 register bit 4 is shut off, RESET is activated, or PWRDOWN is activated. Once the conditions causing PNLOFF to go high are removed, PNLOFF may be set low again to do two writes of 1 to PR57 register bit 2.

Bit 1

PNLOFF/$\overline{\text{WPLT}}$ Select

When this bit is set to 1 the PNLOFF/$\overline{\text{WPLT}}$ output serves as an external RAMDAC write strobe instead of panel power control. Default at reset or power-down is 0.

Bit 0

Bank B Enable

When this bit is set to 1, memory accesses and refresh operations to Bank B video memory are enabled. Bank B operation occurs as dictated by the setting of bit 1 of this register.

When this bit is set to 0 all accesses and refresh operations to Bank B are halted. The Bank B address and control lines are static and the control lines at inactive levels. Bank B data lines are three-stated, being pulled high or low by their power-on configuration pullups or pulldowns.

This bit is set to 1 by default at reset.

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5.9.38 PR58 - WD90C26A Feature Register II

Read/Write Port = 3CFh, Index = 11h
Unlock: PR5 (3C5.0Fh) = 05h

BIT	FUNCTION
7:1	VGA Activity Detection Counter
0	Scratch Pad Bit

Bit 7:1

VGA Activity Detection Counter

This 7-bit programmable counter is used with PR57 register bits 7 and 6 to detect VGA activity. The counter should be preset and initialize during the Power ON Self Test (POST) that usually runs automatically when any IBM AT compatible computer is turned on.

Then, when VGADET (pin 14) changes state (depending on the setting of PR57 register pin6), the counter counts to the preset value while VGADET remains at the same state. Any VGA I/O or memory cycle will reset the counter and VGADET to the original state.

The WD90C26A divides the vertical retrace signal by 1024, and the resulting VERT1024 signal is used as the clock input to the counter. Refer to the following examples:

Example 1

VCLK = 25 MHz,
Vertical Scan Rate = 60 Hz,
PR58[7:0] = 8Ch
VERT = 1/60 = 0.016667 sec
VERT1024 = 0.016667 sec x 1024 = 17.06667 sec
VGADET = 17.06667 sec x 70 = 1194.667 sec = 19.911 sec minimum

Example 2

VCLK = 28 MHz,
Vertical Scan Rate = 70 Hz,
PR58[7:0] = 64h
VERT = 1/70 = 0.0142857 sec
VERT1024 = 0.0142857 sec x 1024 = 14.62857 sec
VGADET = 14.62857 sec x 50 = 731.4285 sec = 12.19 sec minimum

Bit 0

Scratch Pad Bit

5.9.39 PR59 - WD90C26A Operation Voltage and Memory Arbitration Cycle Setup Register

Read/Write Port = 3CFh, Index = 12h
Unlock: PR5 (3C5.0Fh) = 05h

Bit 7 and 6 reflect the operation voltages for the WD90C26A.

Bit 2:0 of this register is used to setup the total length of the frame buffer memory fixed arbitration cycle, as a method of adjusting arbitration cycle length to the speed of the memory and speed of the CRT and Flat Panel Displays

BIT	FUNCTION
7	Host and Flat Panel Voltage (BV_{DD})
6	Powerdown (PV_{DD}), Memory Data Interface (V_{DD}), and Internal RAMDAC Palette (RV_{DD}) Voltage
5	ENDATA Polarity
4	Mode 13 Enhancement
3	TFT Panel Color Enhancement
2	FCP2
1	FCP1
0	FCP0

Bit 7

Host and Flat Panel Voltage (BV_{DD})

This is a read-only bit that reflects the status of configuration bit CNF(10). CNF(10) is pulled down at reset to select 5 VDC or pulled up at reset to select 3.3 VDC. For additional information on hardware configuration options, refer to Section 6.

Bit 6

Powerdown (PV_{DD}), Memory Data Interface (V_{DD}), and Internal RAMDAC Palette (RV_{DD}) Voltage

This bit is programmed by software to select either 5 VDC or 3.3 VDC for PV_{DD}, V_{DD}, and RV_{DD} (refer to the following list). The internal DAC RGB Output (AV_{DD}), including the RESET and REFRESH system bus signals should always be connected to 5 VDC.

Following reset, when bits 7 and 6 are read, the following data should be returned:

OPERATION VOLTAGE	PR59	
	BIT 7	BIT6
5 VDC	0	0
3.3VDC	1	1
Mixed	0	1

Bits 5

ENDATA Polarity

Bit 5 selects the polarity of ENDATA as follows:

BIT 4	DESCRIPTION
0	ENDATA Active High (Default)
1	ENDATA Active Low

Bits 4

Mode 13 Enhancement

In STN Color and Monochrome LCD Modes, the WD90C26A provides space dithering to enhance the low resolution mode (Mode 13). Space dithering is selectable as follows:

BIT 4	DESCRIPTION
0	Disable Space Dithering in Mode 13
1	Enable Space Dithering in Mode 13 (Default)

Bits 3

TFT Panel Color Enhancement

This bit works with PR57 register bits 3 and 4 to provide TFT color enhancement. Refer to the description for PR57.

Bits 2:0

Setting these bits adjusts the arbitration cycle length in increments of 160 ns. The default arbitration cycle at reset is the 101b setting, or 800 ns. Cycle increments are based on a VCLK rate of 25 MHz and should be scaled accordingly for differing VCLK values.

5.9.40 PR62 - FR/M Timing Register

Read/Write Port = 3CFh, Index = 15h
Unlock: PR5 (3C5.0Fh) = 05h

BIT	FUNCTION
7:0	FR/M Timing

For STN monochrome and color LCD flat panels, this register controls the period of panel AC driving signal (FR/M) in relation to the refresh rate.

The FR signal appears at the FR/$\overline{\text{BLANK}}$ pin anytime that PR19 register bit 4 is set to 1.

The default rate of the FR signal is once every 480 lines for a default-at-reset FR signal synchronized with the panel refresh rate of 480 line panels.

The rate of the FR signal may be adjusted faster or slower in increments of 4 horizontal scan lines.

The FR pulse rate generated is at a line count rate of 8 times the value stored in PR62.

For an FR pulse rate of once every 480 lines, PR62 should be set to 60d (3Ch).

The FR pulse is 50% duty cycle.

PR62 should not be set to 00h as this setting is reserved for test purposes.

5.10 INTERNAL I/O PORT REGISTERS

Refer to Section 5.1 for a summary of VGA Internal I/O Port Registers.

5.10.1 ISA Bus Mode Setup Register

Write Only Port 46E8h
(Also at 56E8h, 66E8h, 76E8h)
Accessible only in ISA bus mode (CNF(2)=1).

This register is compatible with typical ISA bus wake-up sequence operations such as:

Write 16h to 46E8h
Write 01h to 102h
Write 0Eh to 46E8h

NOTE

This register is only readable if PR15 bit 7 is set to 1.

BIT	FUNCTION
7:5	Unused
4	Setup
3	Enable I/O and Memory
2:0	External BIOS ROM Page Select

Bit 7:5

Unused

No function is defined on writes to the ISA Bus Mode Setup Register. If PR15 register bit 7 is set to 1, bits 7:5 return 000 on reads to 46E8h. Otherwise, bits 7:5 are tristated during reads.

Bit 4

Setup

Puts WD90C26A into setup mode so that only I/O port 102h is accessible.

Bit 3

I/O and Memory Accesses

Bit 2:0

Unused Internally

Used for BIOS ROM Page select. On I/O accesses to 46E8h, $\overline{\text{EBROM}}$ becomes the I/O write strobe for external implementation of BIOS ROM page mapping. Bits 2:0 are latched data bits to define 4 Kbyte pages on BIOS ROM. The external mapping logic affects the three most significant bits of address applied to the BIOS ROM. The ROM can, therefore, be thought of as consisting of eight, 4 Kbyte pages. External circuitry is required to implement the BIOS ROM page selection using bits D2:D0.

5.10.2 Setup Mode Video Enable Register

Read/Write Port = 102h
(XXXX XXXX XXXX X010b)

This register is used in both ISA(AT) and MicroChannel modes.

BIT	FUNCTION
7:1	Unused
0	Wakeup VGA

Bit 7:1

Unused

Bit 0

Wakeup VGA for I/O and Memory Accesses

Only the lower three address bits are decoded for this port. The WD90C26A must be in the SETUP mode.

The VGA Enable Sleep bit or Programmable Option Select (POS) register 102h bit 0 is used to awaken the WD90C26A after power-on in MicroChannel ISA(AT) mode.

To enter the setup mode in ISA(AT) bus applications, bit 4 of the partially decoded internal I/O port 46E8h is set to 1 before accessing I/O port 102h.

In MicroChannel mode, when the $\overline{\text{CDSETUP}}$ (BALE) signal pin is active low, the WD90C26A is in setup mode and port 102h can be accessed.

5.10.3 Video Subsystem Enable Register

Read/Write Port = 3C3h

BIT	FUNCTION
7:1	Unused
0	Video Subsystem Enable

Bit 7:1

Unused

No function is defined on writes to the Video Subsystem Enable Register. These bits are tristated during reads.

Bit 0

Video Subsystem Enable.

In MicroChannel mode, if this bit is set to '1' or the 3C3D0 pin is high, the WD90C26A responds to MicroChannel accesses.

If this bit is set to '0'and the 3C3D0 pin is low, the WD90C26A is disabled from servicing MicroChannel operations.

6.0 USING FEATURES

This section describes the following WD90C26A features and how to use them:

- Power Distribution
- Recommended Power Supply Isolation and Decoupling
- System Interfaces
- Enabling and Disabling the WD90C26A
- Video RAM Configuration
- Chip Configuration
- Powerdown/Reset Modes
- Panel Protection
- Activating CRT and Flat Panel Displays
- Clock Interfacing
- Panel Interfacing
- CRT Interfacing
- Register Shadowing
- Mapping-RAM Programming
- Using an External RAMDAC
- I/O Mapping
- Direct Access to Video Memory
- Chip Initialization
- Video Signature Analyzer

6.1 POWER DISTRIBUTION

6.1.1 Introduction

The WD90C26A Controller supports supply voltages of 3.3 VDC or 5.0 VDC. In addition, the WD90C26A operates with a mix of both supply voltages. This allows the WD90C26A to be used in situations where portions of a design operate at 3.3 VDC for power savings, while other portions operate at the traditional 5 VDC for interface compatibility.

Table 6-1 lists the power pin designators, and the following figures show power distribution for each version.

- Powering of WD90C26A I/O Pins (Figure 6-1)
- Power Distribution Block Diagram (Figure 6-2)
- Power Configuration for 5.0 VDC Operation (Figure 6-3)
- Power Configuration for 3.3 VDC Operation (Figure 6-4)
- Power Configuration for Mixed Voltage Operation (Figure 6-5)

6.1.2 Power Distribution Sections

For the purpose of power distribution, the WD90C26A is divided into functional sections. Each section is provided with its own power input pins and given a distinct designator as shown in Figure 6-2. The separate power distributions sections are:

- Core Section
- Host System Bus Interface Section
- Powerdown Section
- Internal RAMDAC Palette Section
- DAC Section

The Core section contains the VGA Controller core logic, DRAM data I/O pins, and Memory Data Interface.

The Host System Bus Interface section contains the system I/O interface signals including the data bus, memory and I/O control pins and other bus control signals, CRT sync signals, and the panel and clock I/O.

The Powerdown section contains the DRAM address and control pins, and two system bus input signals.

The Internal RAMDAC Palette section contains the 256x18 VGA Palette array.

The DAC section contains the analog drivers for the R,G,B color signals to the CRT.

In the following discussions, specific power pins are referred to by their designator, or by the generic designator V_{DD}.

6.1.3 5 VDC Operation

The WD90C26A may be operated at 5 VDC by connecting all its V_{DD} pins to a 5 VDC power source (see Figure 6-3).

6.1.4 3.3 VDC Operation

For 3.3 VDC operation, each V_{DD} pin of the WD90C26A is connected to 3.3 VDC power source, except the AV_{DD} pin (see Figures 6-4 and 6-5). In systems where the WD90C26A operates in a 3.3 VDC environment, the DAC AV_{DD} pin must be connected to 5.0 VDC in order to directly drive a CRT.

6.1.5 Mixed Voltage Operation

To describe operation of the WD90C26A in a mixed voltage environment, the following assumptions are made:

- The WD90C26A is connected to a ISA compatible bus operating at 5 VDC.
- The WD90C26A drives its sections with output levels corresponding to voltage level provided at the V_{DD} pin for that section.
- The DRAMs operate at 3.3 VDC.
- The Core section of the WD90C26A operates at 3.3 VDC and does not interface with any 5 VDC logic.
- The Host System Bus Interface section drives the system bus interface at 5 VDC from the BV_{DD} pin.
- The Powerdown section of the WD90C26A is operated at the same voltage as the core, so that the DRAM interface has the same voltages on address and data interfaces.

In Figure 6-5, showing mixed voltage operation, the Powerdown section does not directly interface with any 5.0 VDC logic and is powered by the PV_{DD} pins at 3.3 VDC.

NOTE

The RESET and $\overline{\text{REFRESH}}$ input signals could be power by either 5 VDC or 3.3 VDC.

The internal RAMDAC palette section is a RAM array that operates at 3.3 VDC, connected to the RV_{DD} pin, and does not interface with any 5.0 VDC logic. The RV_{DD} pin does not connect to any I/O pins.

When operation with a CRT is required, the DAC section is driven by the AV_{DD} pin at 5 VDC. Otherwise, when CRT operation is not required, the AV_{DD} pin can be tied to ground.

CIRCUIT	DESIGNATOR
Clock Interface	BV_{DD}
CRT Sync Interface	BV_{DD}
Internal Digital Core	V_{DD}
Memory Address	PV_{DD}
Memory Control	PV_{DD}
Memory Data Bus	V_{DD}
Panel Interface Pins	BV_{DD}
Host System Bus Interface	BV_{DD}
Power Control/Reset	PV_{DD}
Internal RAMDAC Palette	RV_{DD}
Internal DAC, RGB Out	AV_{DD}
External RAMDAC Interface	PV_{DD}

TABLE 6-1 POWER PIN DESIGNATORS FOR CIRCUITS WITHIN POWER DISTRIBUTION SECTIONS

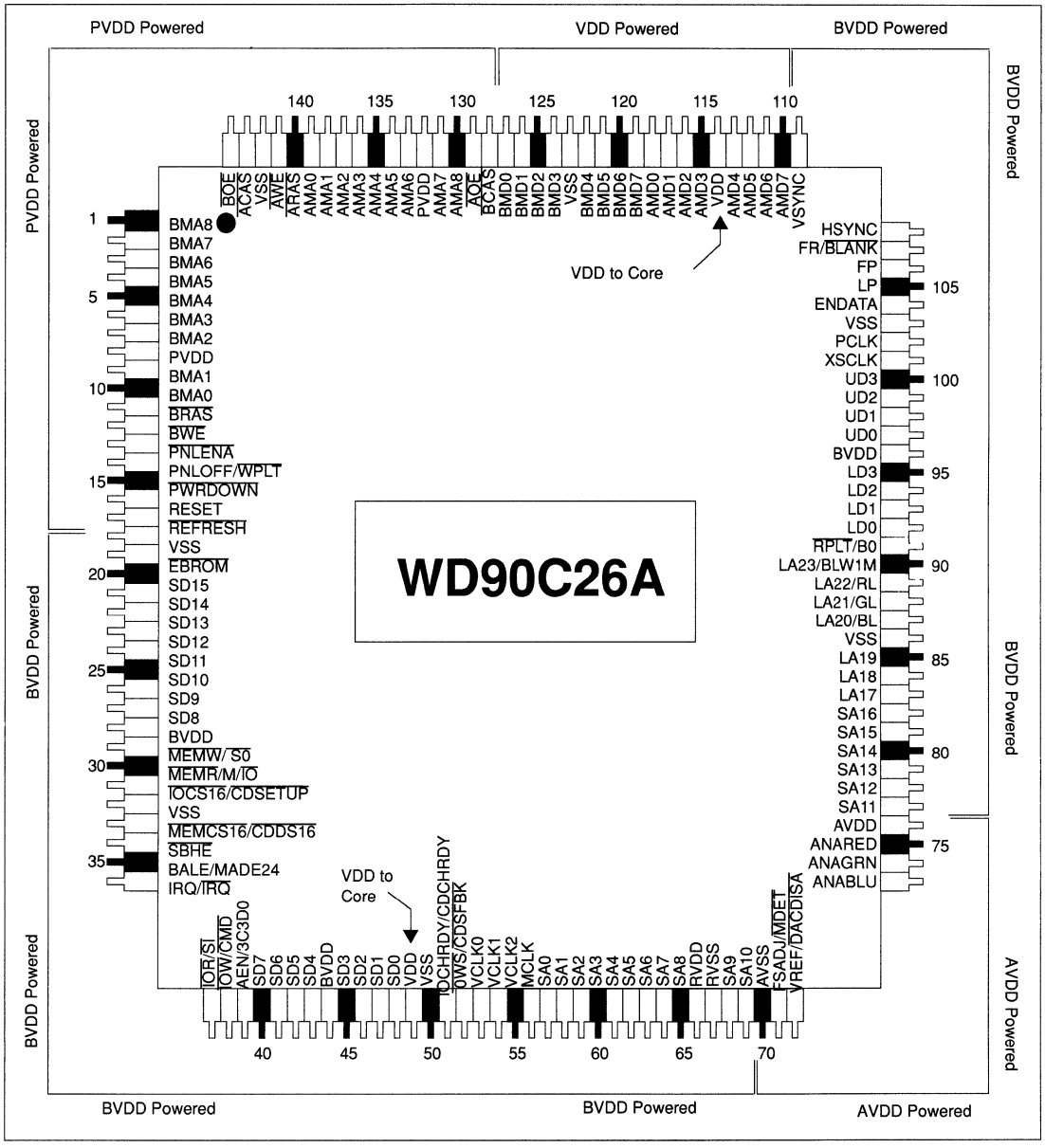

FIGURE 6-1 POWERING OF WD90C26A I/O PINS

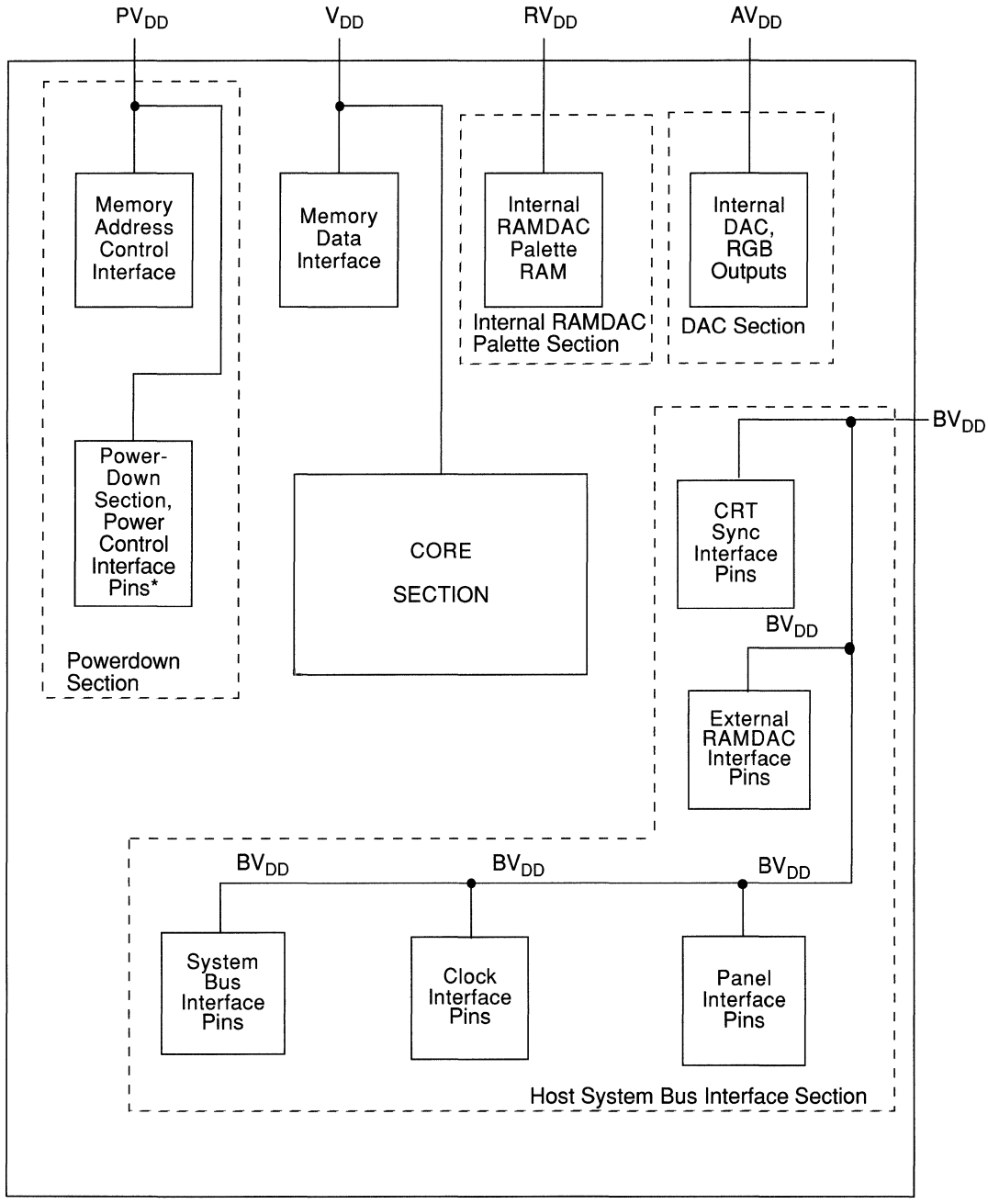

FIGURE 6-2 POWER DISTRIBUTION BLOCK DIAGRAM

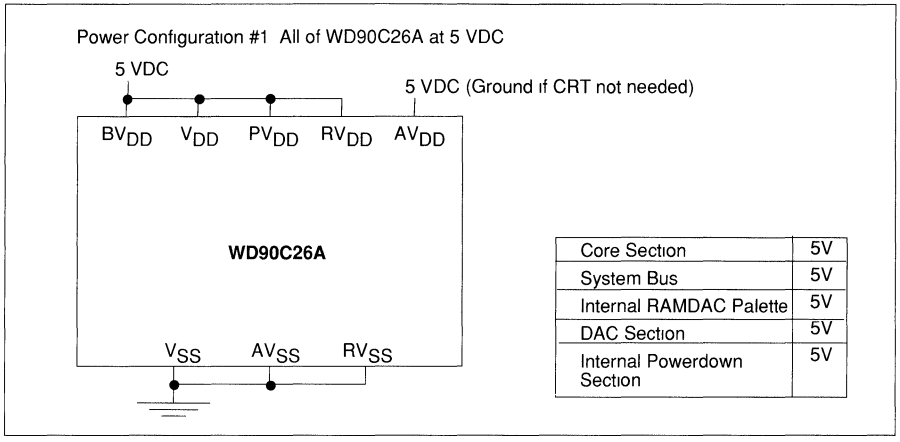

FIGURE 6-3 POWER CONFIGURATION FOR 5 VDC OPERATION

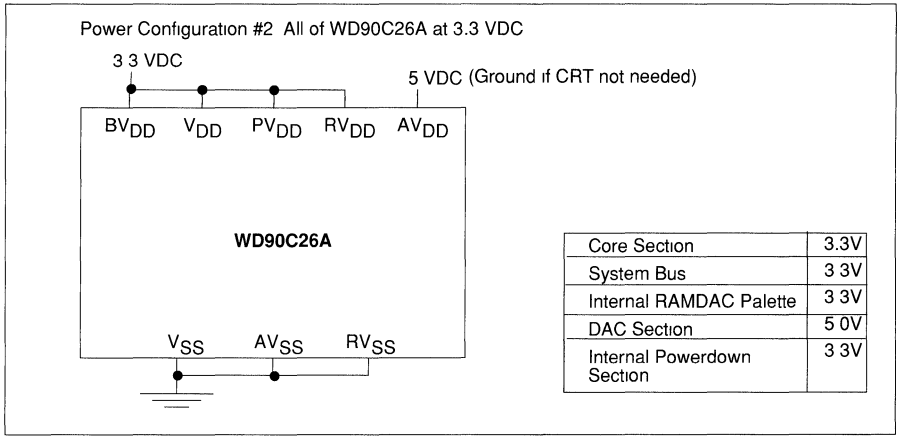

FIGURE 6-4 POWER CONFIGURATION FOR 3.3 VDC OPERATION

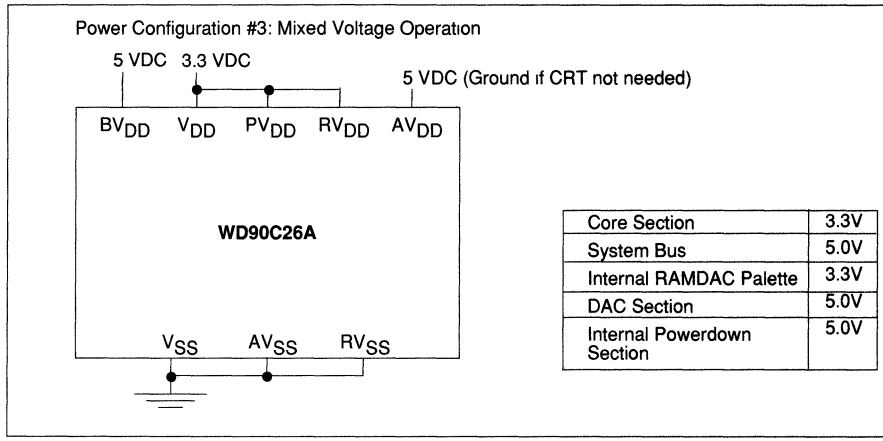

FIGURE 6-5 POWER CONFIGURATION FOR MIXED VOLTAGE OPERATION

6.2 RECOMMENDED POWER SUPPLY ISOLATION AND DECOUPLING

The recommended power supply connections for isolation and decoupling are shown in Figures 6-6 and 6-7. Figure 6-6 shows the recommended connections for single voltage operation, while in Figure 6-7 mixed voltage operation is shown. In either case, the DAC section (AV_{DD}) must be powered by 5 VDC.

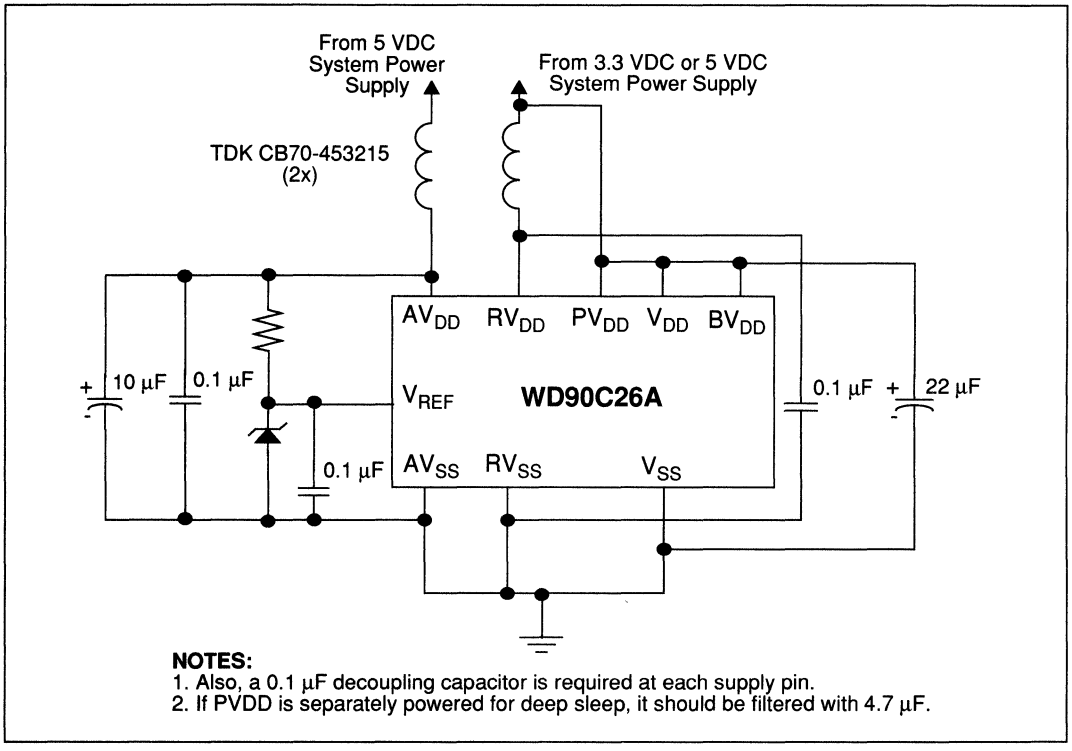

FIGURE 6-6 RECOMMENDED POWER SUPPLY ISOLATION AND DECOUPLING FOR SINGLE VOLTAGE OPERATION

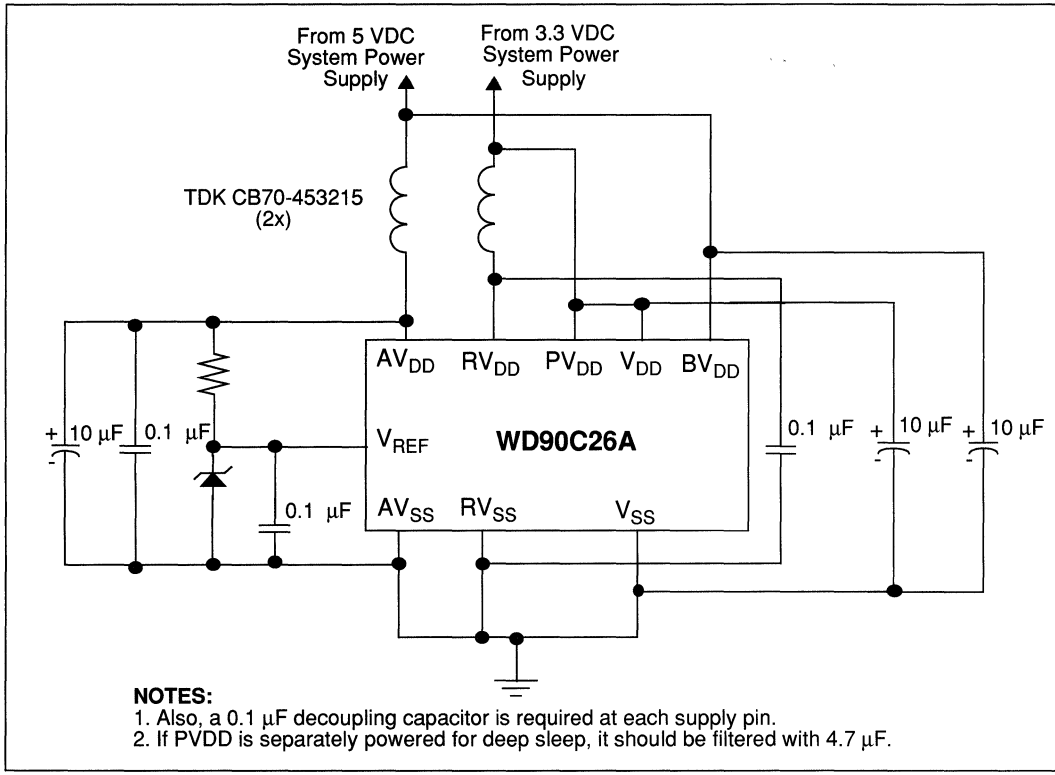

FIGURE 6-7 RECOMMENDED POWER SUPPLY ISOLATION AND DECOUPLING FOR MIXED VOLTAGE OPERATION

6.3 SYSTEM INTERFACES

The figures shown in this section describe the following system interfaces:

- 8-Bit ISA Bus (AT) Interface with 8-Bit BIOS, Figure 6-8.
- 16-Bit ISA Bus (AT) Interface with 8-Bit BIOS, Figure 6-9.
- 16-Bit MicroChannel Bus Interface with 8-Bit BIOS, Figure 6-10.

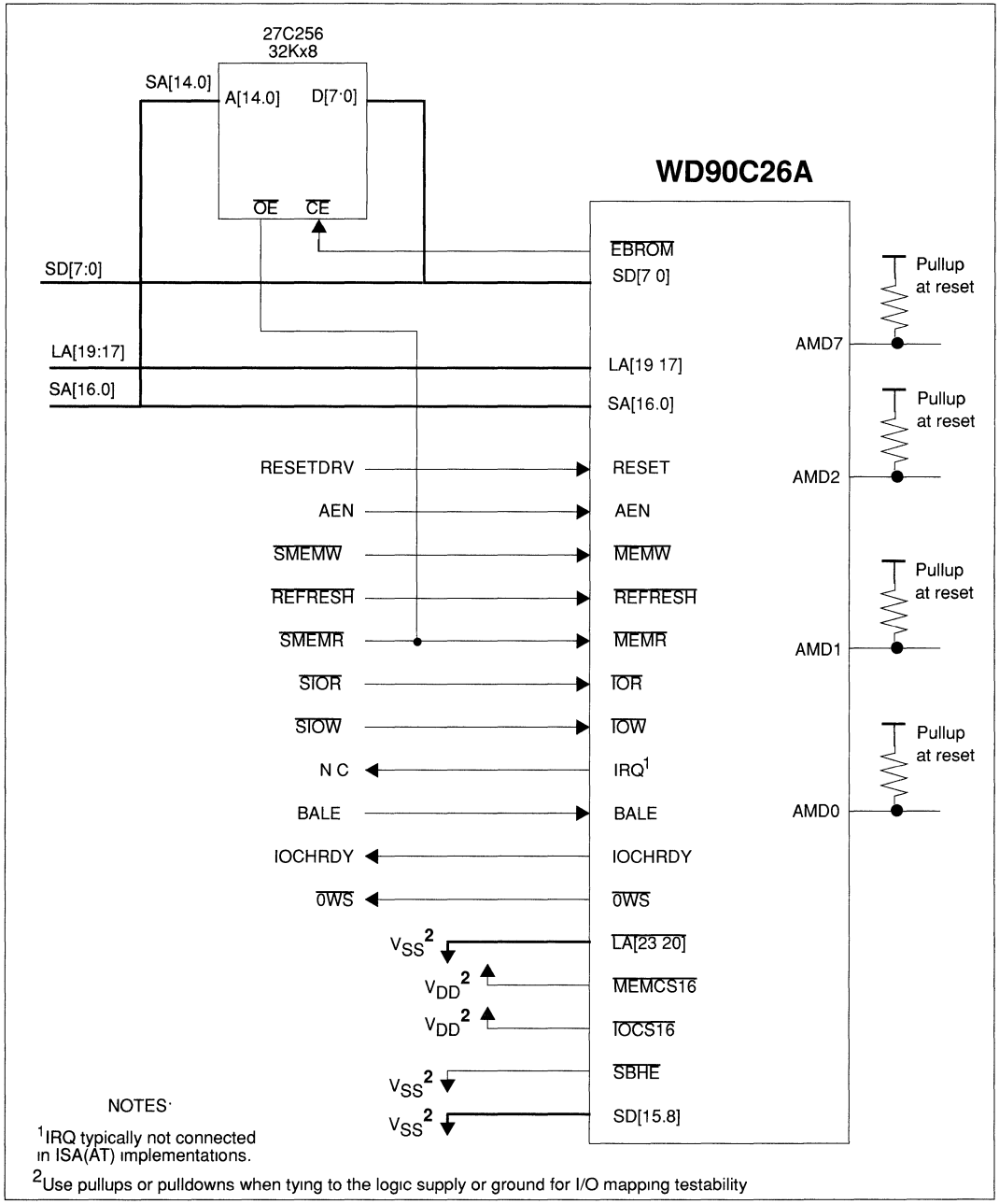

FIGURE 6-8 8-BIT ISA BUS (AT) INTERFACE

Figure 6-8 shows a typical 8-bit ISA Bus (AT) interface. The system data bus SD(7:0) and address bus SA(19:0) are shown with the BIOS ROM.

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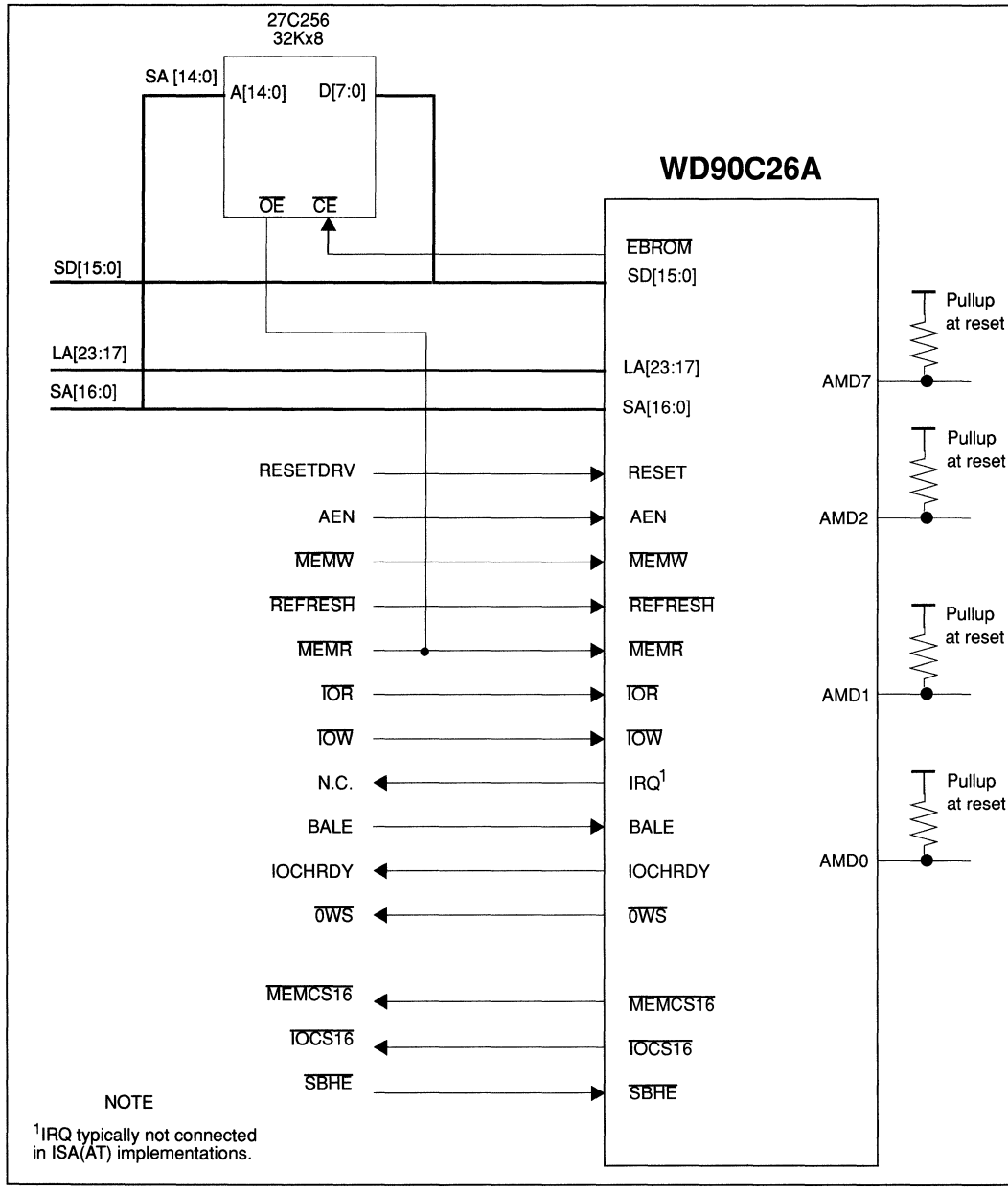


FIGURE 6-9 16-BIT ISA BUS (AT) INTERFACE

Figure 6-9 shows a typical 16-bit ISA Bus (AT) interface.

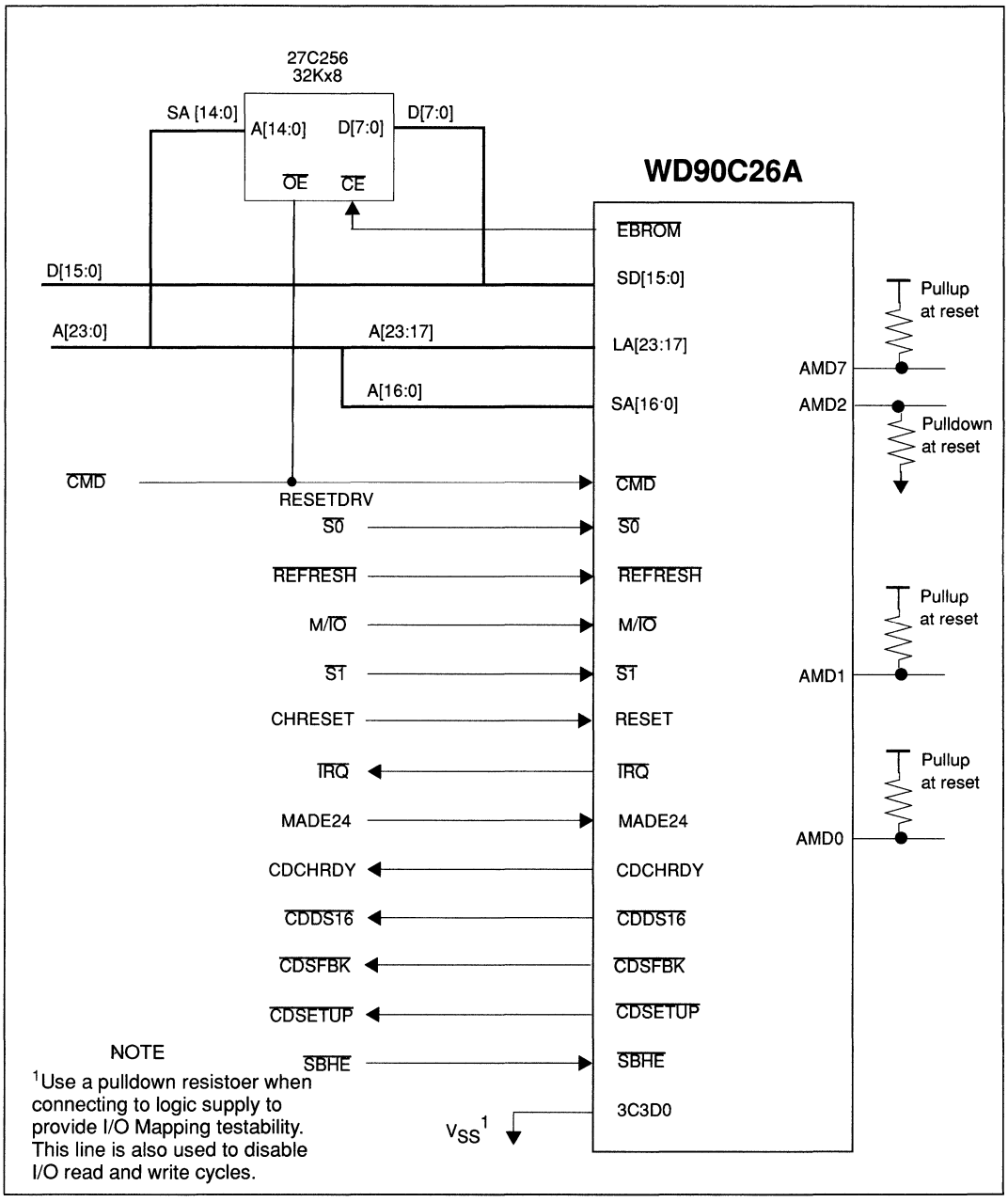


FIGURE 6-10 16-BIT MICROCHANNEL BUS INTERFACE

Figure 6-10 shows a typical MicroChannel Bus Interface and 8-bit BIOS ROM.

6.4 ENABLING AND DISABLING THE WD90C26A

This section describes the steps necessary to bring up a WD90C26A after reset or power-on and the steps that can be taken to disable the WD90C26A if necessary. The WD90C26A can be disabled for power savings or to allow another video subsystem to be used in its place.

6.4.1 Enabling the WD90C26A

The basic steps to bring up the WD90C26A are:

- Apply RESET to initialize functions
- Select the hardware configuration options at reset
- Deactivate VGA Reset and VGA Sleep functions
- Wake up the chip
- Initialize register settings for panel type
- Program the mapping RAM

Each step is described in detail below:

6. 4.1.1 RESET Signal Characteristics

When RESET is activated, the WD90C26A chooses by default the VCLK0 signal as the internal video clock source, or if configured to control an external clock circuit, the input to the VCKIN pin of that circuit. For a reset to the WD90C26A to be valid, the appropriate video clock source must be valid for 10 clock periods before RESET goes inactive.

6. 4.1.2 Hardware Configuration Options

The first step taken to setup up the WD90C26A is done while the RESET pulse is active; that of configuring its hardware option. During power-on or a 'hard' reset, various hardware configuration options are selected by pulling memory data lines high or low while reset is active. Section 6.5 describes the function of each configuration option and the data bits that are pulled high or low during reset to select the options.

6. 4.1.3 Waking Up the WD90C26A

When the WD90C26A is brought out of reset, its hardware configuration options are set but registers are not yet accessible. Standard VGA wakeup procedures must then be followed to enable the WD90C26A and allow register and video memory access. Typically the system BIOS performs these wakeup functions.

NOTE

The video clock source and MCLK source to the WD90C26A must be valid for at least 10 clock cycles after the end of the reset period before any register access is performed.

In ISA bus mode, the wakeup bit in the Setup Mode Video Enable Register (102h) is made accessible by setting the ISA Bus Mode Setup Register (46E8h) bit 0 high. Thereafter, the WD90C26A is awakened by setting Setup Mode Video Enable Register (102h) bit 0 high. Then, I/O and memory accesses are enabled. Setup Mode register access is then disabled by setting the ISA Bus Mode Setup Register (46E8h) bit 4 low and bit 3 high.

In MicroChannel Mode, a similar procedure is followed. First, access to the Setup Mode Video Enable Register is made possible by setting the Video Subsystem Enable Register (3C3h) bit 0 high. Thereafter, the WD90C26A is awakened by setting Setup Mode Video Enable Register (102h) bit 0 high. $\overline{\text{CDSETUP}}$ is then deactivated.

In PI bus mode, the WD90C26A uses the same wakeup sequence described above for the ISA bus mode.

6. 4.1.4 Deactivating VGA Reset and Enabling Video Memory

Before programing the WD90C26A, VGA reset must be deactivated by writing a 03h to the VGA Sequencer Reset Register (3C5h, Index 00h). Video memory access is then enabled by setting the VGA Miscellaneous Output Register (3C2h) bit 1 to 1.

6. 4.1.5 Initializing Register Settings and Loading the Mapping RAM

After the chip has been awakened, register settings are loaded which are appropriate to the panel type being supported, type of clock circuit attached, and other factors. The mapping RAM is also loaded with a mapping table appropriate to the panel type. Typically the video BIOS supplied for the WD90C26A provides this initialization as well as loading the mapping RAM.

6.4.2 Disabling the WD90C26A

Under certain conditions it is desirable to disable the WD90C26A. This can be done in a variety of ways, with varying degrees of impact:

First, the chip can be put back into its pre-wake up mode by reversing the wake-up procedure or activating the RESET pin.

Second, four different powerdown modes are available that disable portions of the WD90C26A for power reduction purposes.

A total disable of the WD90C26A can be achieved by placing the chip in host release mode, where any time the chip is in System Powerdown mode all I/O and memory access is disabled as well as most bus status signals.

6.5 VIDEO RAM CONFIGURATION

Refer to *Video Memory Interface* in Section 3 for a description of the different RAM configurations. This section describes how DRAMs are connected.

Minimum systems based on the WD90C26A have two 256Kx4 DRAMs connected to the A Bank memory address and control lines and to the lower byte of the 16-bit video memory data bus.

Unused pins of the B memory data bus must be biased by the external configuration pullup or pulldown resistors.

Systems that use the dual-panel multiplexed LCD interface, and that require simultaneous display capability have 256K x 4 DRAM #3 connected to the B bank memory address and control connections and to BMD[3:0].

Maximum systems that have full 16-bit video buffer architecture, in addition to DRAM #3, have 256K x 4 DRAM #4 connected to the Bank B memory address and control lines and to BMD[7:4], allowing the B memory bank to serve as the upper byte of the 16-bit video memory buffer data bus.

In 16-bit video memory applications using four 256Kx4 DRAMs, BMD7 is the most significant bit of the 16-bit memory bus. AMD0 is the least significant bit. AMD3 through AMD0 are connected to the first DRAM, AMD7 through 4 to the second, BMD3 through 0 to the third, and BMD7 through 4 to the fourth DRAM.

Systems that use a single 256Kx16 DRAM do not use the B address/control lines and are restricted to operations that do not use the B memory interface as a frame buffer.

Figure 6-11 shows a typical 256K x 16 DRAM interface.

NOTE

The example used is the Hitachi HM51-4260 or NEC uPD424260.

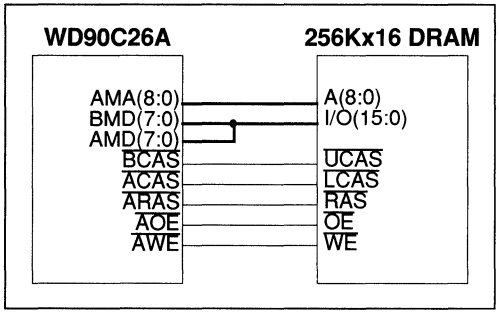


FIGURE 6-11 TYPICAL 256Kx16 DRAM INTERFACE

To support a frame buffer for applications that use either four 256Kx4 DRAMs or one 256Kx16 DRAM, a separate 256Kx4 frame buffer DRAM can be added (refer to Figures 3-3 and 3-4).

6.6 WD90C26A HARDWARE CONFIGURATION OPTIONS

This section provides the following information:

- A general description of the WD90C26A hardware configuration options.
- Table 6-2 shows how to select configuration options.
- Table 6-3 provides a hardware configuration option summary.

At reset, the WD90C26A floats the video memory data buses and disables memory data output from video RAM by holding the memory control signals inactive. This prevents the AMD and BMD memory buses from being driven by either the WD90C26A or any attached video memory when reset is active.

During reset, while these buses are not being driven, hardware configuration options for the WD90C26A are selected by pulling the memory data lines up or down until reset is removed.

The inputs are not pulled up or down internally. Therefore, external configuration resistors are used to bias the data bus signals while in this RESET-active high-impedance mode. Tables 6-2 and 6-3 list the configuration options that are controlled by pulling video memory data lines up (high) or down (low) during reset.

PIN NO.	MEMORY DATA BUS	CONFIG BIT	CONFIGURATION FUNCTION AT RESET
119	BMD7	CNF(15)	Pullup: CNF(15) = 1. Pulldown: CNF(15) = 0. CNF(15) is reserved for BIOS. CNF(15)can be read and written as PR11 register bit 7.
120	BMD6	CNF(14)	Pullup: CNF(14) = 1. Selects 12-bit FTF Interface, if PR5 register bit 7, CNF(7), is set to 1. Pulldown: CNF(14) = 0. Selects separate frame buffer configuration for display memory configurations 3 and 4. CNF(14) can be read or written as PR11 register bit 6.
121	BMD5	CNF(13)	Pullup: CNF(13) = 1. Pulldown: CNF(13) = 0. CNF(13) is reserved for BIOS. CNF(13) can be read or written as PR11 register bit 5.
122	BMD4	CNF(12)	Pullup: CNF(12) = 1. Pulldown: CNF(12) = 0. CNF(12) is reserved for BIOS. CNF(12)can be read or written as PR11 register bit 4.
124	BMD3	CNF(8)	Pullup: CNF(8) = 0. Pulldown: CNF(8) = 1. CNF(8) is reserved for BIOS. The inverse of CNF(8) can be read or written as PR5 register bit 3.
125	BMD2	CNF(10)	Pullup: CNF(10) = 1. Select 3.3 VDC operation for BV_{DD}. Pulldown: CNF(10) = 0. Select 5.0 VDC operation for BV_{DD}. BV_{DD} is also 5.0 VDC for mixed voltage operation. CNF(10) can be read (read-only) as PR59 register bit 7.

TABLE 6-2 PIN CONFIGURATION FUNCTIONS AT RESET/HARDWARE CONFIGURATION OPTIONS

PIN NO.	MEMORY DATA BUS	CONFIG BIT	CONFIGURATION FUNCTION AT RESET
126	BMD1	CNF(9)	Pullup: CNF(9) = 1. Pulldown: CNF(9) = 0. Following reset, CNF(9) and CNF(11) determine which panel interface is supported by the WD90C26A as follows: CNF(9) Panel Select High / CNF(11) Panel Select Low 0 0 Dual Panel STN Mono LCD 0 1 Monochrome Plasma Panel 1 0 Monochrome EL Panel 1 1 Single Panel Mono/Color LCD CNF(9), Panel Select High, can be read or written as PR18 register bit 1.
127	BMD0	CNF(11)	Pullup: CNF(11) = 1. Pulldown: CNF(11) = 0. Following reset, CNF(9) and CNF(11) determine which panel interface is supported by the WD90C26A. Refer to CNF(9). CNF(11), Panel Select Low, can be read or written as PR18 register bit 0.
110	AMD7	CNF(7)	Pullup: CNF(7) = 0. LA22 through LA20 are address inputs. Pulldown: CNF(7) = 1. LA22 through LA20 are address outputs. Determines whether LA(22-20) are address outputs or address inputs. LA(22-20) must be address inputs for virtual memory support. CNF(7) can be read (read-only) as PR5 register bit 7.
111	AMD6	CNF(6)	Pullup: CNF(6) = 0. Pulldown: CNF(6) = 1. CNF(6) is reserved for BIOS. CNF(6) can be read or written as PR5 register bit 6.
112	AMD5	CNF(5)	Pullup: CNF(5) = 0. Select one 256Kx16 DRAM with 2 CAS interface support. Pulldown: CNF(5) = 1: Select four 256Kx4 DRAMs with 2 WEN interface support CNF(5) selects memory configuration No. 1 or No. 2 and modifies the DRAM interface accordingly. CNF(5) can be read or written as PR5 register bit 5.

TABLE 6-2 PIN CONFIGURATION FUNCTIONS AT RESET/HARDWARE CONFIGURATION OPTIONS

PIN NO.	MEMORY DATA BUS	CONFIG BIT	CONFIGURATION FUNCTION AT RESET
113	AMD4	CNF(4)	Pullup: CNF(4) = 0. Pulldown: CNF(4) = 1. CNF(4) is reserved for BIOS. CNF(4) can be read or written as PR5 register bit 4.
115	AMD3	CNF(3)	Pullup: CNF(3) = 1. Selects VCLK1 and VCLK2 as outputs. Pulldown: CNF(3) = 0. Selects VCLK1 and VCLK2 as inputs. CNF(3) is not readable or writable.
116	AMD2	CNF(2)	Pullup: CNF(2) = 1. Selects AT bus interface. Pulldown: CNF(2) = 0. Selects MicroChannel bus interface. CNF(2) is not readable or writable.
117	AMD1	CNF(1)	Pullup: CNF(1) = 0. Enables CNF(2) to selects the AT Bus or the MicroChannel Bus. Pulldown: CNF(1) = 1. Selects the PI Bus. CNF(1) can be read (read-only) as PR1 register bit 1.
118	AMD0	CNF(0)	Pullup: CNF(0) = 0. Enable BIOS ROM. The WD90C26A supports external video BIOS interfacing to the host system and controls access cycles to the BIOS ROM. Pulldown: CNF(0) = 1. Disable BIOS ROM. The WD90C26A does not perform video BIOS ROM cycle control. CNF(0) can be read or written as PR1 register bit 0.

TABLE 6-2 PIN CONFIGURATION FUNCTIONS AT RESET/HARDWARE CONFIGURATION OPTIONS

PIN NO.	PIN NAME	PULLUP DURING RESET			PULLDOWN DURING RESET		
		HARDWARE FUNCTION	READABLE AS	CNF(BIT) SET TO	HARDWARE FUNCTION	READABLE AS	CNF(BIT) SET TO
119	BMD7	BIOS[1]	PR11 Bit 7=1	CNF(15)=1	BIOS[1]	PR11 Bit 7=0	CNF(15)=0
120	BMD6	12-Bit TFT	PR11 Bit 6=1	CNF(14)=1	Frame Buffer	PR11 Bit 6=0	CNF(14)=0
121	BMD5	BIOS[1]	PR11 Bit 5=1	CNF(13)=1	BIOS[1]	PR11 Bit 5=0	CNF(13)=0
122	BMD4	BIOS[1]	PR11 Bit 4=1	CNF(12)=1	BIOS[1]	PR11 Bit 4=0	CNF(12)=0
124	BMD3	BIOS[1]	PR5 Bit 3=1	CNF(8)=0	BIOS[1]	PR5 Bit 3=0	CNF(8)=1
125	BMD2	3.3 BV_{DD}	PR59 Bit 7=1	CNF(10)=1	5.0 BV_{DD}	PR59 Bit 7=0	CNF(10)=0
126	BMD1	Panel Select High = 1	PR18 Bit 1=1 (Modifiable)	CNF(9)=1	Panel Select High = 0	PR18 Bit 1=0 (Modifiable)	CNF(9)=0
127	BMD0	Panel Select Low = 1	PR18 Bit 0=1 (Modifiable)	CNF(11)=1	Panel Select Low = 0	PR18 Bit 0=0 (Modifiable)	CNF(11)=0
110	AMD7	Select LA22-LA20 as Inputs	PR5 Bit 7=0	CNF(7)=0	Select LA22-LA20 as Outputs	PR5 Bit 7=1	CNF(7)=1
111	AMD6	BIOS[1]	PR5 Bit 6=0	CNF(6)=0	BIOS[1]	PR5 Bit 6=1	CNF(6)=1
112	AMD5	Select four 256K x 4 DRAMs with 2 WEN support	PR5 Bit 5=0	CNF(5)=0	Select one 256K x 16 DRAM with 2 CAS support	PR5 Bit 5=1	CNF(5)=1
113	AMD4	BIOS[1]	PR5 Bit 4=0	CNF(4)=0	BIOS[1]	PR5 Bit 4=1	CNF(4)=1
115	AMD3	Select VCLK1 and VCLK2 as outputs	---	CNF(3)=1	Select VCLK1 and VCLK2 as inputs	---	CNF(3)=0
116	AMD2	AT Bus Mode	---	CNF(2)=1	MicroChannel Bus Mode	---	CNF(2)=0
117	AMD1	AT or Micro-Channel Bus	PR1 Bit 1=0	CNF(1)=0	PI Bus	PR1 Bit 1=1	CNF(1)=1
118	AMD0	BIOS ROM Support Enabled	PR1 Bit 0=0 (Modifiable)	CNF(0)=0	BIOS ROM Support Disabled	PR1 Bit 0=1 (Modifiable)	CNF(0)=1
NOTE: BIOS1 indicates functions reserved for BIOS.							

TABLE 6-3 HARDWARE CONFIGURATION OPTION SUMMARY

6.7 POWERDOWN/RESET MODES

This section describes the following Powerdown/ Reset Modes:

- Sleep (VGA Powerdown) Mode
- Display Idle Mode
- General Powerdown Modes

These powerdown modes are shown in Figure 6-12. Tables 6-4 through 6-6 provide a summary of information about the powerdown modes and states of WD90C26A signals on the ISA Bus and MicroChannel.

6.7.1 Sleep (VGA Powerdown) Mode

Sleep, or VGA Powerdown, mode is used when the entire VGA subsystem can be shut off. This mode provides the most power savings of the powerdown modes, and requires the most system overhead. When the VGA subsystem has been placed in Sleep Mode, its only action is the preserving of video RAM. This is done by the WD90C26A generating an AC-timed $\overline{CAS}$ before $\overline{RAS}$ refresh operation each time its $\overline{REFRESH}$ input is activated. In this mode, the host system should not attempt to access video memory or any registers.

To achieve maximum power savings in Sleep Mode, the WD90C26A takes the following actions:

- Turns off the panel display.
- Shuts down the DACs (if in CRT mode).
- Gates off the internal MCLK and VCLK signals.
- Executes AC-timed $\overline{CAS}$ before $\overline{RAS}$.
- Disables CPU access to its internal I/O registers.

If the host release bit is set (PR35 register bit 5 is set to 1), Sleep Mode also does the following:

- Releases host interface signals
- Disables host access to registers
- Disables host access to video RAM

The following paragraphs describe how to enter and exit Sleep Mode.

6. 7.1.1 Entering Sleep Mode

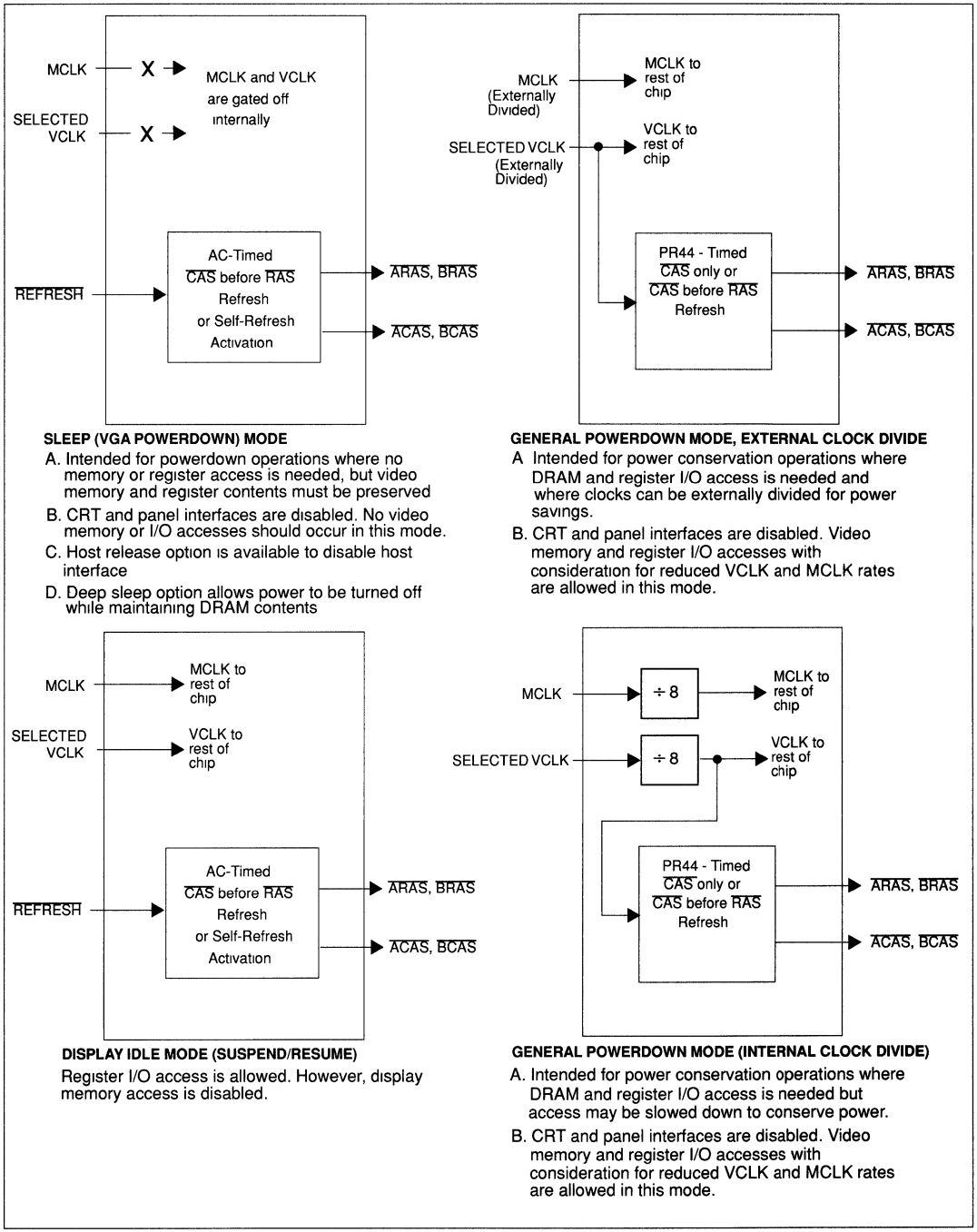
Sleep Mode is selected as the powerdown mode when PR35 register bit 7 is set to 1 and PR44 register bit 7 is set to 0. The WD90C26A then enters Sleep Mode when its $\overline{PWRDOWN}$ input is driven low.

When Sleep Mode is entered, the WD90C26A waits for 4 horizontal scan lines PLUS 3 $\overline{REFRESH}$ cycles and then turns off VCLK and MCLK internally.

This display memory refresh is the only WD90C26A activity during this powerdown mode because the internal RAMDAC is also turned off.

The power pins (V_{DD}) of the WD90C26A must remain powered to maintain the contents of the video display buffer.

Before the VCLK and MCLK inputs can be turned off, the following time interval must elapse: time to display 4 horizontal lines PLUS 3 $\overline{REFRESH}$ cycles.



SLEEP (VGA POWERDOWN) MODE

A. Intended for powerdown operations where no memory or register access is needed, but video memory and register contents must be preserved

B. CRT and panel interfaces are disabled. No video memory or I/O accesses should occur in this mode.

C. Host release option is available to disable host interface

D. Deep sleep option allows power to be turned off while maintaining DRAM contents

GENERAL POWERDOWN MODE, EXTERNAL CLOCK DIVIDE

A Intended for power conservation operations where DRAM and register I/O access is needed and where clocks can be externally divided for power savings.

B. CRT and panel interfaces are disabled. Video memory and register I/O accesses with consideration for reduced VCLK and MCLK rates are allowed in this mode.

DISPLAY IDLE MODE (SUSPEND/RESUME)

Register I/O access is allowed. However, display memory access is disabled.

GENERAL POWERDOWN MODE (INTERNAL CLOCK DIVIDE)

A. Intended for power conservation operations where DRAM and register I/O access is needed but access may be slowed down to conserve power.

B. CRT and panel interfaces are disabled. Video memory and register I/O accesses with consideration for reduced VCLK and MCLK rates are allowed in this mode.

FIGURE 6-12 POWERDOWN/RESET MODES

6. 7.1.2 Exiting Sleep (System Powerdown) Mode

Before returning to normal display mode, the system first returns the WD90C26A clock inputs back to their original frequencies (if they were slowed down or stopped during the Sleep Mode).

NOTE

Care must be taken to ensure that the clock inputs to the WD90C26A are stable BEFORE driving the $\overline{\text{PWRDOWN}}$ input back to its high state.

To return to normal mode, the $\overline{\text{PWRDOWN}}$ input should be driven high. Then, after 4 horizontal scan lines PLUS 3 $\overline{\text{REFRESH}}$ cycles, the information retained in video memory is displayed again and registers are again accessible. If host release was active, the system bus interface signals are reactivated.

6.7.2 Display Idle Mode

The Display Idle Mode is used to turn off the display when the keyboard has been idle for a preset time interval. The DAC and LCD panel interfaces are turned off in this mode. The CPU can access I/O registers of the WD90C26A, but it can not access display memory.

To achieve power savings in the display mode. the WD90C26A takes the following action:

- Turns off the panel display.
- Turns off the CRT Interface DACs.
- Executes powerdown $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh with each activation of the REFRESH pin, or triggers self-refresh.
- Inhibits the CPU access to video memory.

The following paragraphs describe how to enter and exit Display Idle Mode.

6. 7.2.1 Entering Display Idle Mode

Display Idle Mode is selected as the powerdown mode when PR35 register bit 7 and PR44 register bit 7 are both set to 0 (0 is the default value). The WD90C26A enters Display Idle Mode when its $\overline{\text{PWRDOWN}}$ input is driven low. Then:

- External clocks must maintain their original frequencies for the Display Idle Mode.
- The CRT and flat panel displays are stopped.
- The WD90C26A uses the $\overline{\text{REFRESH}}$ input to generate AC-timed $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles to refresh display memory.
- There is no system access of video memory while in Display Idle Mode.
- While in the Display Idle Mode, the video system continues to run, allowing the user to read/write WD90C26A I/O registers.
- Power consumption in Display Idle Mode is approximately 1/10 of normal consumption.

6. 7.2.2 Exiting Display Idle Mode

To return to normal mode, the $\overline{\text{PWRDOWN}}$ input is driven high. After 4 horizontal scan lines PLUS 3 $\overline{\text{REFRESH}}$ cycles, the information retained in video memory is automatically displayed again.

6.7.3 General Powerdown Modes

There are two General Powerdown modes:

- General Powerdown Mode with External Clock Control
- General Powerdown Mode with Internal Clock Control

These modes are used:

- When CRT or flat panel display is not required but I/O register or video DRAM access is required.
- To keep the system running, but at reduced frequencies for both MCLK and VCLK

When using General Powerdown Modes, video system performance is reduced for significant power savings. Also, activating the WD90C26A $\overline{\text{PWRDOWN}}$ input is the only software interaction required to achieve the power savings.

General Powerdown mode with external clock divide is designed to interface with an intelligent clock generator like the WD90C63, which has the capability of slowing down the clocks to the WD90C26A to a selectable frequency during the powerdown interval.

General Powerdown mode with internal clock divide is designed so that the external clock may maintain the same frequencies during powerdown. However, internal clock circuitry in the WD90C26A divides the input clocks by eight.

Both General Powerdown modes allow the system to access I/O registers and display memory.

To achieve power savings during General Powerdown Modes, the WD90C26A takes the following action:

- Turns off the panel display.
- Turns off the DACs (if in CRT mode).
- Turns off internal clocks to circuit areas that are not required during powerdown.

6. 7.3.1 General Powerdown Mode With External Clock Divide

Before entering this mode, PR44 register bits 6 through 0 must be preloaded with the correct values based on the powerdown clock frequency. Refer to Section 6.6.5 for an example of how to calculate PR44 register values for $\overline{\text{PWRDOWN}}$ refresh. When entering General Powerdown modes, refresh timing circuits based on the values in the PR44 register replace the CRTC as the source of memory refresh operations.

With PR44 register bits 6 through 0 pre-loaded, the General Powerdown mode is entered by setting PR44 register bit 7 to 1 and PR35 register bit 6 to 0, and then driving $\overline{\text{PWRDOWN}}$ low.

Before returning to normal display mode, the system must first return the WD90C26A clock inputs back to their original frequencies.

NOTE

Care must be taken to ensure that the clock inputs to the WD90C26A are stable BEFORE driving the $\overline{\text{PWRDOWN}}$ input back to its high state.

When the $\overline{\text{PWRDOWN}}$ input is driven high, The WD90C26A returns to normal operating mode and the information retained in video memory is automatically displayed.

6. 7.3.2 General Powerdown Mode With Internal Clock Divide

Before entering this mode, PR44 register bits 6 through 0 should be preloaded with there correct value based on the po00werdown clock frequency. Refer to Section 6.6.5 for an example of how to calculate PR44 register values for $\overline{\text{PWRDOWN}}$ refresh. When entering General Powerdown modes, refresh timing circuits based on the values in the PR44 register replace the CRTC as the source of memory refresh operations.

With PR44 register bits 6 through 0 pre-loaded, General Powerdown mode with internal clock divide is entered by setting PR44 register bit 7 to 1, PR35 register bit 6 to 1, and then driving $\overline{\text{PWRDOWN}}$ low.

The WD90C26A returns to normal operating mode and the information retained in video memory is automatically displayed when the $\overline{\text{PWRDOWN}}$ input is returned to a high state.

6.7.4 Deep Sleep Mode

The WD90C26A also supports a Deep Sleep mode that is intended to allow the video DRAM to be refreshed while disconnecting power to most of the chip. This feature provides the maximum reduction in power use. In Deep Sleep mode all contents of internal registers, mapping RAM, and RAMDAC are lost. Therefore, the contents should be saved before entering this mode.

To initiate the Deep Sleep operation, the power down manager should first save all WD90C26A I/O registers, color palette RAM, and mapping RAM. The WD90C26A is then put into Sleep mode through the appropriate setting of PR bits and activation of the $\overline{\text{PWRDOWN}}$ pin. After waiting for 4 horizontal scan lines PLUS 3 $\overline{\text{REFRESH}}$ cycles, the RESET signal is activated and the WD90C26A is in Deep Sleep mode (see Figure 6-13).

While in Deep Sleep mode, power to all supply pins, except the P_{VDD} pins, may be removed. PVDD could be removed a minimum of 100 msec after RESET is activated. AC-timed $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh operations occur with each pulse of the $\overline{\text{REFRESH}}$ input, regardless of other register settings.

Deep Sleep mode is exited by the following procedure:

1. Reconnecting the disconnected supply pins.
2. Delay 100 msec and then deactivate the RESET input.
3. Delay an additional 100 msec and then wake up the WD90C26A, unlock the shadow registers, and restore all CRTC registers.
4. Delay an additional 100 msec and then restore the rest of the I/O registers, RAMDAC, and mapping RAM.
5. Finally, deactivate $\overline{\text{PWRDOWN}}$.

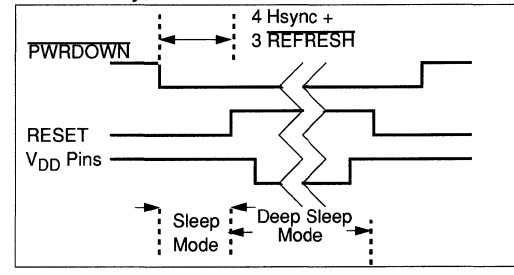


FIGURE 6-13 PIN SEQUENCING FOR DEEP SLEEP OPERATION

PR44 BIT 7	PR35 BIT 7	PR35 BIT 6	MODE ENTERED ON PWRDOWN	CRT I/F	PANEL I/F	VIDEO MEMORY CONTENTS	VIDEO DRAM REFRESH
0	0	X	Display Idle (Suspend/ Resume	Disabled	Disabled	Retained, not accessible[2]	DRAM self-refresh, or AC-Timed $\overline{CAS}$ before $\overline{RAS}$ refresh with each $\overline{REFRESH}$ pulse
0	1	X	Sleep (System Powerdown)	Disabled	Disabled	Retained, not accessible[2]	DRAM self-refresh, or AC-Timed $\overline{CAS}$ before $\overline{RAS}$ refresh with each $\overline{REFRESH}$ pulse
1	X	0	General Power-down, External Clock Divide	Disabled	Disabled	Accessible	$\overline{CAS}$ before $\overline{RAS}$ refresh according to PR44 (6:0) interval and PR1A(1:0)
1	0	1	General Power-down, Internal Clock Divide	Disabled	Disabled	Accessible	$\overline{CAS}$ before $\overline{RAS}$ refresh according to PR44 (6:0) interval and PR1A(1:0)
0	1	X	Deep Sleep (Reset Activated)	Disabled	Disabled	Retained, not accessible	DRAM self-refresh or AC-Timed $\overline{CAS}$ before $\overline{RAS}$ refresh with each $\overline{REFRESH}$ pulse

TABLE 6-4 POWERDOWN

REGISTER CONTENTS	MAPPING RAM TABLE	INTERNAL RAMDAC PALETTE	CLOCK INPUTS	NECESSARY POWER CONNECTIONS	ACTIONS TO RETURN TO NORMAL OPERATION
Accessible	Retained, not accessible	Retained, not accessible	MCLK and VCLK must be maintained	PV_{DD}, V_{DD}, BV_{DD}, RV_{DD} required. AV_{DD} may be disconnected	(Reconnect power), bring $\overline{PWRDOWN}$ high.
[1]Retained, not accessible	[1]Retained, not accessible	[1]Retained, not accessible	VCLK and MCLK may be stopped	PV_{DD}, RV_{DD} V_{DD}, and BV_{DD} required. RV_{DD} & AV_{DD} may be disconnected	(Reconnect power), restore VCLK, MCLK, bring $\overline{PWRDOWN}$ high.
Accessible	Accessible	Accessible	MCLK and VCLK must be maintained (May be externally divided)	PV_{DD}, V_{DD}, BV_{DD}, RV_{DD} required. AV_{DD} may be disconnected	(Reconnect power), return VCLK, MCLK to operating frequency, bring $\overline{PWRDOWN}$ high
Accessible	Accessible	Accessible	MCLK and VCLK must be maintained. Internally divided by 8	PV_{DD}, V_{DD}, BV_{DD}, RV_{DD} required. AV_{DD} may be disconnected	(Reconnect power), bring $\overline{PWRDOWN}$ high
Not retained if V_{DD} is removed	Not retained if RV_{DD} is removed	Not retained if RV_{DD} is removed	VCLK and MCLK may be stopped	PV_{DD} required, all others may be disconnected	(Reconnect power); deactivate RESET and PWRDOWN; and restore all registers, mapping RAM, and internal RAMDAC palette

MODES

NOTES

[1]Should not be accessed in Sleep mode. Access is disabled if the host release bit (PR35 register bit 5) is set to 1.

[2]System refresh signal to $\overline{REFRESH}$ input or self-refresh type DRAM required to maintain video memory contents.

I/O OR OUTPUT NAME	STATE WHILE RESET ACTIVE HIGH	STATE AFTER RESET GOES INACTIVE LOW	DEFAULT STATE AT WAKE-UP	STATE WHILE AEN ACTIVE HIGH	STATE WHILE INTERNAL REFRESH ACTIVE	STATE WHILE REFRESH ACTIVE LOW	SLEEP MODE (SYSTEM POWER-DOWN)	DISPLAY IDLE MODE	GENERAL POWER-DOWN MODES
$\overline{\text{IOCS16}}$	N	N		N	N	N	N	N	N
$\overline{\text{MEMCS16}}$						Z	N	N	Z
IRQ		L		L	L	N	Z	N	N
IOCHRDY				Z	N	N	Z	N	N
$\overline{\text{0WS}}$				N	N	P	P	P	P
SD(15:0)							Z	N	N
LA20/BL							N^1	N^1	N^1
LA21/GL							N^1	N^1	N^1
LA22/RL							N^1	N^1	N^1
NOTE: Refer to key and notes for Table 6-5, 6-6, and 6-7 on the following page.									

TABLE 6-5 RESET AND POWERDOWN STATES OF WD90C26A SYSTEM BUS INTERFACE --- ISA BUS MODE

I/O OR OUTPUT NAME	STATE WHILE RESET ACTIVE HIGH	STATE AFTER RESET GOES INACTIVE LOW	DEFAULT STATE AT WAKE-UP	STATE WHILE INTERNAL REFRESH ACTIVE	STATE WHILE REFRESH ACTIVE LOW	SLEEP MODE (SYSTEM POWER-DOWN)	DISPLAY IDLE MODE	GENERAL POWER-DOWN MODES	HOST RELEASE DURING SLEEP MODE
$\overline{\text{CDSETUP}}$	I	I	I	I	I	I	I	I	
$\overline{\text{CDDS16}}$	H	H	H	N	N	N/Z	N/Z^9	N/Z^9	
$\overline{\text{IRQ}}$	Z	Z	Z	N	N	N	N	N	
CDCHRDY	L	N	N	N	N	N/Z^9	N/Z^9	N/Z^9	
$\overline{\text{CDSFBK}}$	N	N	N	N	N	P/N	P/N	P/N	H
SD(15:0)	Z	Z	N	N	N	Z	N	N	
LA20/BL	N^1	N^1		N^1		N^1	N^1	N^1	
LA21/GL	N^1	N^1		N^1		N^1	N^1	N^1	
LA22/RL	N^1	N^1		N^1		N^1	N^1	N^1	
NOTE: Refer to key and notes for Table 6-5, 6-6, and 6-7 on the following page.									

TABLE 6-6 RESET AND POWERDOWN STATES OF WD90C26A SYSTEM BUS INTERFACE --- MICROCHANNEL BUS MODE

KEY FOR TABLES 6-5, 6-6, AND 6-7

I = pin in input mode
Z = pin in high-impedance output mode
P = previous state held
U = undetermined
L = pin in output mode
H = pin in output high
N = normal operation state
N/÷8 = Normal frequency divided by 8

NOTES FOR TABLES 6-5, 6-6, AND 6-7

1. Dependent on CNF(7). If AMD(7) is low during reset, LA(22:20) are configured as panel interface outputs.
2. $\overline{RAS}$ and $\overline{CAS}$ outputs are high except during refresh functions, where they operate as normal for the duration of the refresh cycle. If self-refresh is activated, $\overline{RAS}$ and $\overline{CAS}$ are sequenced low during powerdown modes.
3. Dependent on whether the WD90C26A is operating in 9-bit or 12-bit TFT mode. If operating in one of these modes, $\overline{RPLT}$/B0 is a normal operation output during powerdown modes whose idle state may be low or high when system clocks are stopped.
4. Input or output as determined by CNF(3) [AMD(3) high or low at reset].
5. Low if configured as an FR output, otherwise the normal $\overline{BLANK}$ signal to the external RAMDAC.
6. HSYNC and VSYNC affected by polarity selection options.
7. Memory control signals and addresses appropriate for refresh operations.
8. Output enable is usually low and write enable usually high to allow read cycles from display memory for screen updating.
9. Signal is tri-stated when $\overline{PWRDOWN}$ is active low if in host release mode (PR35 bit 5=1).
10. Low until MCLK goes active, then assumes normal state.

I/O OR OUTPUT NAME	STATE WHILE RESET ACTIVE HIGH	STATE AFTER RESET GOES INACTIVE LOW	DEFAULT STATE AT WAKE-UP	STATE WHILE AEN ACTIVE HIGH	STATE WHILE INTERNAL REFRESH ACTIVE	STATE WHILE REFRESH ACTIVE LOW	SLEEP MODE (SYSTEM POWER-DOWN)	DISPLAY IDLE MODE	GENERAL POWER-DOWN MODES
$\overline{\text{EBROM}}$/ 46E8	H	H		N	N	N	N	N	N
AMD(7:0)					N	N	N	N	N
AMA(8:0)						Z	N	N	Z
$\overline{\text{ACAS}}$					L	N	Z	N	N
$\overline{\text{AOE}}$					N	N	Z	N	N
$\overline{\text{ARAS}}$					N	P	P	P	P
$\overline{\text{AWE}}$							Z	N	N
BMD(7:0)							N[1]	N[1]	N[1]
BMA(8:0)							N[1]	N[1]	N[1]
$\overline{\text{BRAS}}$							N[1]	N[1]	N[1]
$\overline{\text{BWE}}$							Z	N	N
$\overline{\text{BCAS}}$							N	N	N
$\overline{\text{BOE}}$							H/L/N[2]	H/L/N[2]	H/L/N[2]
ANARED/ ANAGRN/ ANABLU							N[8]	N[8]	N[8]
$\overline{\text{RPLT}}$/B0							H/L/N[2]	H/L/N[2]	H/L/N[2]
HSYNC							H	H	N
VSYNC							Z	Z	N
VCLK1/ VCSLD/ VCSELL							N	N	N
VCLK2/ VCSEL/ VCSELH							H/L/N[2]	H/L/N[2]	H/L/N[2]
$\overline{\text{PNLENA}}$	H	H		N			H	H	N[8]
PNLOFF/ $\overline{\text{WPLT}}$	H						H/L/N[2]	H/L/N[2]	H/L/N[2]
PCLK							N[8]	N[8]	N[8]
FR/ $\overline{\text{BLANK}}$							L	L	L
UD(3:0), LD(3:0)							H/N[3]	N	N
XSCLK							N[6]	N[6]	N[6]
ENDATA							N[6]	N[6]	N[6]
FP							I/N[4]	I/N[4]	I/N[4]
LP							I/N[4]	I/N[4]	I/N[4]

NOTE: Refer to key and notes for Table 6-5, 6-6, and 6-7 on the previous page.

TABLE 6-7 RESET AND POWERDOWN STATES OF WD90C26A VIDEO AND VIDEO MEMORY INTERFACE OUTPUTS AND I/Os

6.7.5 Calculation of General Powerdown Mode Refresh Timing

In General Powerdown Modes, the WD90C26A internally generates the necessary refresh cycles to maintain DRAM contents and allow access to video memory. This is performed by internal refresh circuits that time refresh operations based on the value in PR44[6:0]. Presented below is an explanation of the steps to be taken to determine the appropriate value to program into PR44 to achieve correct refresh operations during General Powerdown modes.

6. 7.5.1 Understanding DRAM requirements

In order to calculate the appropriate values for PR44 when in General Powerdown Modes, it is first necessary to understand DRAM parameters that determine its refresh needs. The WD90C26A supports DRAM that requires 512 refresh cycles for a complete refresh operation. Therefore, all DRAM used with the WD90C26A requires 512 refresh cycles over a maximum refresh period referred to as t_{REF}. Typical t_{REF} values range from 8 to 64 ms. Another DRAM requirement which needs to be understood before calculating PR44 values is the random cycle time required to do one refresh cycle, referred to as t_{rc}. For 100 nsec DRAM, t_{rc} is typically 180 ns, and for 70 nsec DRAM t_{rc} is typically 130 ns.

6. 7.5.2 Determining Number of Refresh Cycles Per Refresh Operation

The values in PR1A[1:0] and the Vertical Retrace End Register bit 6 determine whether 1, 2, 3 or 5 refresh cycles will occur per refresh operation.

6. 7.5.3 MCLK Frequency Requirements During General Powerdown Modes

Each refresh cycle requires 6 MCLK periods, plus a setup of a maximum of 6 MCLK periods before refresh operations begin. Each system access during General Powerdown modes requires 6 MCLK periods as well. Thus the required MCLK frequency during General Powerdown is calculated by determining the total number of MCLK cycles required during the refresh operation.

The total number of MCLK cycles required per refresh operation is represented as...

6(1 + #system accesses + #refresh cycles)

6. 7.5.4 VCLK Frequency Requirements and PR44[6:0]

In General Powerdown modes, the internal VCLK frequency and PR44[6:0] value have the following relationship:

Refresh Operation Period (ROP) = VCLK period x Dots per Char x (Value in PR44[6:0]+5)

Of that value, the portion of the period dedicated to DRAM refresh is determined by using the above equation except with the PR44+5 value divided by two and the fraction discarded. The difference between the amount used for refresh and the total refresh operation period is the amount used for system access of video DRAM during powerdown refresh cycles.

6. 7.5.5 Example

This example assumes the following conditions:

A. DRAM has 190 ns t_{rc} and 8 msec t_{REF}.
B. Internal VCLK and MCLK frequencies of 5 MHz during the selected General Powerdown mode.
C. PR44 register bits 6:0 set to 14d

With these conditions, calculate the refresh operation period as follows:

ROP = 1/(5 MHz)(8 dots/char)(14+5) = 30.4 µsec

Refresh time per ROP = 1/(5 MHz)(8dots/char)(9)=14.4 µsec

Assuming a trc of 200 nsec for a margin of safety and a 5 MHz MCLK, we get one refresh cycle per 1.2 µsec + a 1.2 µsec setup. Therefore, there is enough margin to program PR1A[1:0] and the Vertical Retrace End Register bit 6 for 1-5 refresh cycles per refresh operation.

For this example we will select two refresh cycles.

Since we need a total of 512 refresh cycles to completely refresh the DRAM and we are doing 2 refresh cycles per refresh operation, we need 256(30.4 µsec)=7.78 msec to completely refresh the DRAM. This figure is within the 8 msec t_{REF} specified and will work.

From this example it can be seen that values of PR44, VCLK, and MCLK can be further optimized if additional reductions in clock frequencies are desired.

6.8 PANEL PROTECTION

The WD90C26A is designed to ensure proper control of $\overline{\text{PNLENA}}$ and PNLOFF signals during cycling of system power and entering or exiting powerdown modes. This is done to allow these signals to be used as controls for power to LCD or other technology panels that require power sequencing to prevent damage. The $\overline{\text{PNLENA}}$ signal is intended for connection to the primary power control and PNLOFF to the negative bias. Typically, these two biases have particular sequencing requirements, as shown in Figure 6-14.

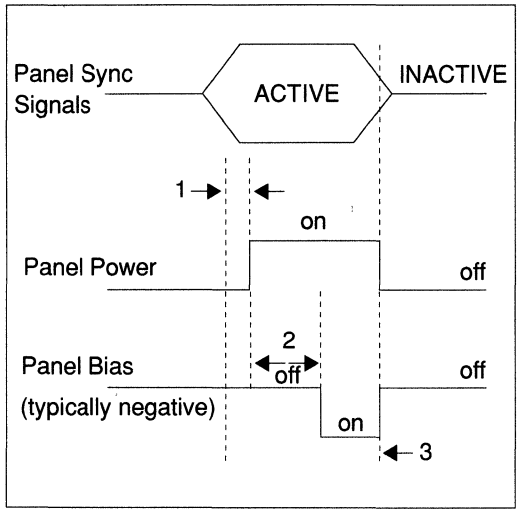


FIGURE 6-14 TYPICAL PANEL SEQUENCING REQUIREMENTS

NOTES

1. Panel manufacturers typically require a minimum setup of sync signals active at the panel before power is applied to the panel.
2. Panel specifications usually list a minimum setup of sync signals active and panel power on before the panel bias is turned on.
3. To prevent panel damage, manufacturers usually require a relationship between loss of panel sync signals and shut-down of panel supply and bias.

6.8.1 Panel Protection During System Power-On

If the system power-on reset signal ensures that RESET is active low until system power meets WD90C26A minimums, the WD90C26A will hold $\overline{\text{PNLENA}}$ inactive and PNLOFF active until software activates these signals.

After system power stabilizes and RESET goes inactive, $\overline{\text{PNLENA}}$ remains inactive and PNLOFF remains active, holding an attached panel in a powered-off state until software actions cause their state to change.

6.8.2 Enabling Panel Power Controls After Power-Up

When a panel is to be enabled, the software must set PR19 register bit 4 high, indicating that the flat panel display mode is active. Software also sets up the various other registers required to generate flat panel timing. Two FP pulses after the FP signal to the flat panel activates the panel. Then $\overline{\text{PNLENA}}$ goes active low, which activates panel power.

The PNLOFF signal is active high at reset because PR57 register bit 2 and PR19 register bit 4 default to 0. After system software has activated $\overline{\text{PNLENA}}$, it can set PR57 bit 2 to 1 (2 times) causing the PNLOFF signal to go low. PNLOFF low may be used to activate negative bias power for a panel.

6.8.3 Disabling Panel Power When Active

When panel support is no longer needed the panel power control signals are returned to their power-up state using the following procedure:

1. Set PR57 register bit 2 to 0 (2 times)
2. Set PR19 register bit 4 to 0

This causes $\overline{\text{PNLENA}}$ to go high (inactive) before PNLOFF goes active high.

6.8.4 Panel Protection During Power-Off

When main power is turned off, the system RESET signal is expected to cause the RESET input to go active high. This causes the WD90C26A to force PNLENA and PNLOFF high, disabling panel power (see Figure 6-15).

While RESET or PWRDOWN are active, PNLENA and PNLOFF remain high until PV_{DD} drops below 2.0V, below which time they become undefined.

6.8.5 PWRDOWN and Panel Protection

Whenever the WD90C26A is put in a powerdown mode by activating PWRDOWN, the PNLENA and PWROFF signals become high, just as in RESET operations. The signals are not set low until PWRDOWN goes inactive high.

NOTE

After PWRDOWN goes inactive high, PR57 register bit 2 must be set to 1 (2 times) before PNLOFF can go low again.

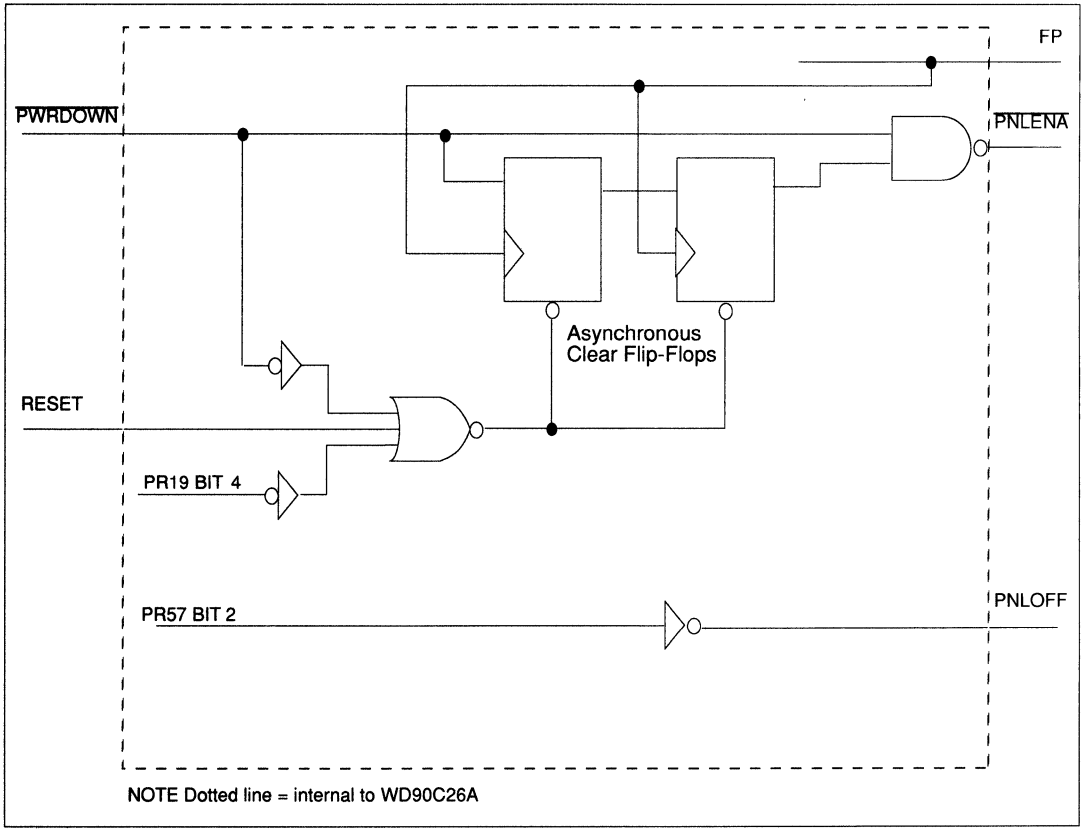


FIGURE 6-15 PNLENA AND PNLOFF PANEL PROTECTION SIGNALS

6.9 REGISTER SHADOWING

The shadowing feature allows certain key registers affecting screen timing and resolution to be locked (once properly programmed) and then overlaid with a base register with the same read/write characteristics. This register shadowing capability allows the CRT controller to be set for a screen resolution compatible with its flat-panel resolution. Then, system applications can modify the CRTC registers without affecting flat-panel display operation (see Figure 6-16). Other circuits in the CRT controller compensate for the fixed-display resolution on panel displays by using hardware algorithms to adjust displayed information to its intended size.

The CRTC Shadow registers control flat panel and CRT timing. When the regular CRTC registers are written to, the shadow timing registers, if unlocked, receive the same data. Locking the shadow timing registers is controlled by PR1B.

In Flat Panel and in Simultaneous Display mode, the shadow timing registers should be loaded once and then locked by PR1B. Once they are locked, data written to the base registers is not passed through to the shadow timing registers and the flat panel timing is not affected.

In CRT only modes, shadow registers should remain locked.

There are eleven sets of registers which have this base/shadow register pair function. All are indexed in port 3?5h.

NAME	INDEX	BITS SHADOWED	TYPICAL SHADOW VALUES
Horizontal Total	00h	3:0	5Fh
Start Horizontal Blanking	02h	7:0	50h
End Horizontal Blanking	03h	6:0	82h
Start Horizontal Retrace	04h	7:0	54h
End Horizontal Retrace	05h	7:0	80h
Vertical Total	06h	7:0	F2h
Overflow	07h	7,5,3,2,0	10h
Vertical Retrace Start	10h	7:0	EFh
Vertical Retrace End	11h	3:0	F2h
Start Vertical Blank	15h	7:0	EAh
End Vertical Blank	16h	7:0	02h

TABLE 6-8 SHADOWED CRTC REGISTERS

The typical shadow values are for a monochrome dual panel LCD with 640 by 480 pixels when operating in LCD only mode.

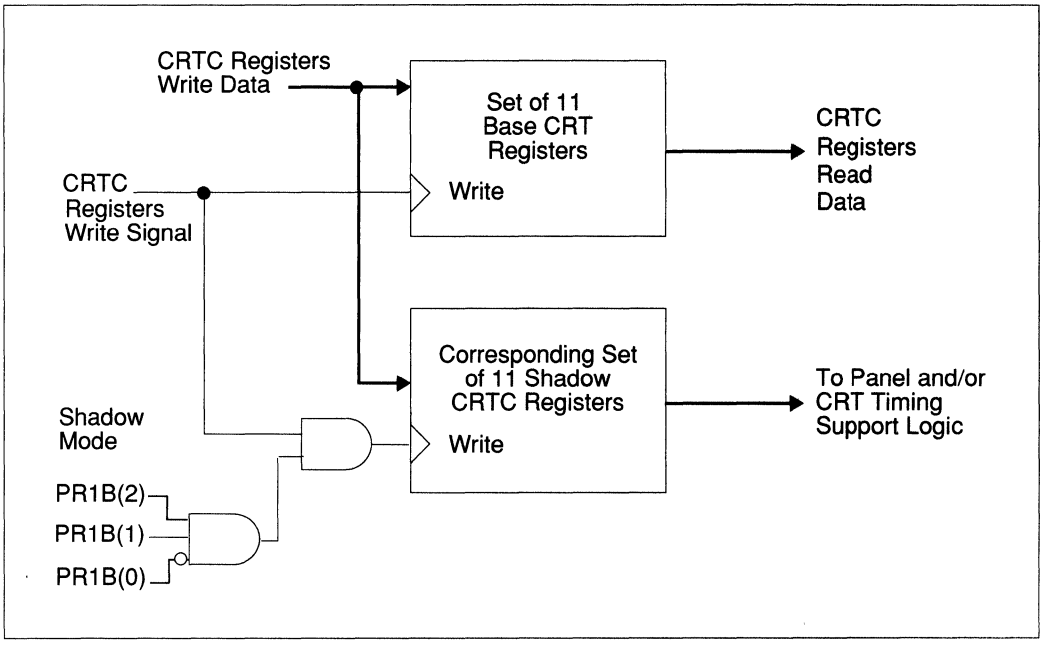


FIGURE 6-16 RELATIONSHIP BETWEEN SHADOW AND BASE CRTC REGISTERS

6.10 ACTIVATING CRT AND FLAT PANEL DISPLAYS

This section describes how to do the following operations:

- Set up the WD90C26A for flat panel only display mode
- Set up the WD90C26A for CRT only display mode
- Set up the WD90C26A for simultaneous display mode with the video image displayed on both a flat panel and a CRT
- Switch from one mode of operation to any other

The WD90C26A supports flat panel displays using paired CRTC registers that are accessible at the same I/O address. The paired CRTC registers are referred to as:

- Shadow CRTC register.
- Base CRTC register.

Base registers are used as a method of making the CRTC settings appear unaltered to the system interface when CRTC register settings need to be modified to fit the timing needs of flat panel displays.

Base CRTC registers are mapped to the I/O address of their equivalent Shadow CRTC registers. Base CRTC registers are read on I/O reads. However, Base CRTC registers do not affect CRTC or flat panel timing.

Shadow CRTC registers have direct control over CRTC operation but are not accessed by system reads of the CRTC registers. Writing to the Shadow CRTC registers is enabled by entering shadow mode.

After the shadow CRTC registers are configured for flat panel operation, there values are locked in by exiting shadow mode. Then, any modifications to the CRTC register values that cause video mode changes will not cause corresponding changes to the flat panel configuration. This ensures that flat panel timing remains unchanged.

6.10.1 Flat Panel Only Display

The procedure for configuring the WD90C26A to support flat panel only display is the same under any of the following circumstances:

- The WD90C26A is being brought up in Flat-Panel Only Display Mode
- The configuration is being switched from CRTC Only to Flat-Panel Only Display Mode
- The configuration is being switched from simultaneous Display to Flat-Panel Only Mode

Use the following procedure to configure the WD90C26A to operate in flat-panel only display mode.

NOTE

Perform this procedure outside of any active application.

1. Ensure that a video mode is programmed into the CRTC registers. If a mode is not programmed, the panel power control pins will not be activated by step 9 until panel synchronizing signals are received.
2. Disable both CRT only and flat-panel only display modes by setting PR19 register bits 4 and 5 to 0.
3. Configure the Paradise Registers for the particular panel type.
4. Save the current Base CRTC register values.
5. Set PR1B to XXXXX110b to enter shadow mode.
6. Load the Base and Shadow CRTC registers with values appropriate to the panel type.
7. Set PR1B to other than XXXXX110b to exit shadow mode.
8. Reload the saved Base CRTC Register values.
9. Enable flat panel display mode by setting PR19 register bit 4 to 1.
10. Sequence flat panel power on after a delay for sync signals to activate.

6.10.2 CRT Only Display

The procedure for configuring the WD90C26A to support CRT Only Display is the same under any of the following circumstances:

- The WD90C26A is being brought up in CRT Only Display Mode
- The configuration is being switched from Flat-Panel Only Display Mode to CRT Only display mode.
- The configuration being switched from simultaneous Display Mode to CRT Only Display Mode

Use the following procedure to configure the WD90C26A to operate in CRT only display mode.

NOTE

Perform this procedure outside of any active application.

1. Sequence panel power off.
2. Disable both CRT and flat panel display modes by setting PR19 register bits 4 and 5 to "0".
3. Configure the Paradise Registers for the particular CRT type.
4. Set PR1B to XXXXX110b to enable write to Shadow CRTC Registers.
5. Load the Base and Shadow CRTC registers with values appropriate to the video mode.
6. Enable CRT display mode by setting PR19 register bit 5 to 1.

6.10.3 Simultaneous Display Mode

The procedure for configuring the WD90C26A to support Simultaneous Display Mode is the same under any of the following circumstances:

- The WD90C26A is being brought up in Simultaneous Display Mode.
- The configuration is being switched from CRTC Only or Flat-Panel Only Display Mode to the Simultaneous Display Mode.

Use the following procedure to configure the WD90C26A to operate in Simultaneous display mode.

NOTE

Perform this procedure during power-on initialization routines where no previous video mode is being preserved.

1. Sequence panel power off.
2. Disable both CRT and flat-panel display modes by setting PR19 register bits 4 and 5 to 0.
3. Configure the Paradise Registers for the particular CRT and panel types.
4. Save the current Base CRTC Register values.
5. Set PR1B to XXXXX110b to enable write to Shadow CRTC Registers.
6. Load the Base and Shadow CRTC registers with simultaneous display values appropriate to the panel type.
7. Set PR1B to other than XXXXX110b to disable write to Shadow CRTC Registers.
8. Restore the Base CRTC Register values appropriate to the video mode.
9. Enable panel and CRT simultaneous display mode by setting PR19 register bits 4 and 5 to 1.
10. Sequence the flat panel power on after a delay for sync signals to activate.

NOTE

For dual-panel type flat panel displays, video memory use changes when switching back and forth from single display to simultaneous display operation. Changing to or from simultaneous display mode from within applications is not recommended because the video image is not preserved when switching to or from simultaneous display modes.

6.11 CLOCK INTERFACING

This section describes clock interfacing for connection of sources to the WD90C26A.

The clock interface supports video and memory clock frequency inputs from a variety of signal sources. The clock interface allows various connections as described and illustrated in the following subsections:

- Using a WD90C26A with an Separate External Clock Sources (see Figure 6-17).
- Using a WD90C26A with an External Synthesizer (see Figure 6-18).
- Using a WD90C26A with an External Clock Multiplexer (see Figure 6-19).
- Typical Oscillator or Clock Frequencies for Standard VGA Monitor Support (see Figure 6-20).

Configure the interface by setting CNF(3), as determined by the level of AMD(3) at reset and by PR15 register settings. The setup parameters are listed in Table 6-9.

CNF(3)	PR15(5)	MODE	PIN 53	PIN 54	PIN 55
0	X	Discrete clock or oscillator inputs	VCLK0 Clock Input	VCLK1 Clock Input	VCLK2 Clock Input
1	0	External Synthesizer Interface	VCKIN Clock Input from Synthesizer	VCSEL 3C2h Write Strobe to Synthesizer	VCSLD Synthesizer Lock or Data = PR2 bit 1
1	1	Multiplexer Control Interface	VCLKIN Clock Input from Mux	VCSELL Clock Mux Sel = 3C2 bit 2	VCSELH Clock Mux Sel = 3C2 bit 3

TABLE 6-9 CLOCK INTERFACE SETUP

NOTES:

1. Pin 56 is always an MCLK input, regardless of mode.
2. An MCLK frequency of 33 MHz is typical for most 100 nsec DRAMs and an MCLK of 44.3 MHz is typical for most 70 nsec DRAMS.

6.11.2 Using a WD90C26A with Separate External Clock Sources

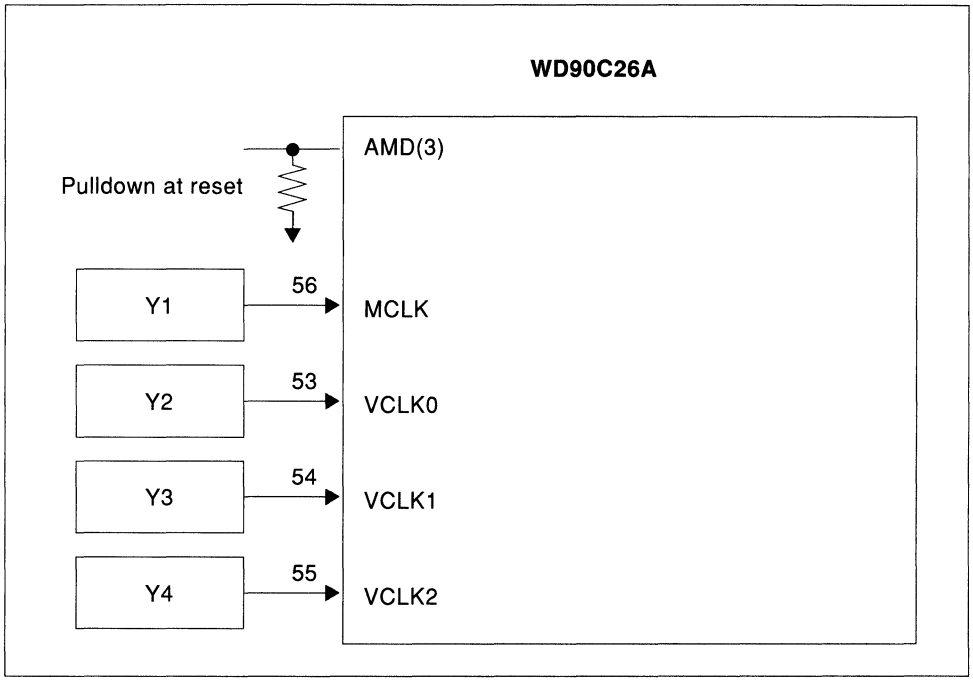


FIGURE 6-17 USING A WD90C26A WITH SEPARATE EXTERNAL CLOCK SOURCES

Configure the WD90C26A for operation with external oscillators or clock sources by pulling AMD(3) low during reset. The external oscillators or clock sources are expected to provide any needed frequencies to the VCLK0 through 2 and MCLK inputs.

An internal multiplexer selects which of the four external sources is used as the internal VCLK for generation of video. The VGA miscellaneous output register at I/O address 3C2h controls selection of VCLK0, VCLK1, or VCLK2 and the selection of MCLK as the internal VCLK source is controlled by PR15 register bit 4.

NOTE:

PR2 register bit 1 must be set to 0 in order to change selection of the VCLK source from VCLK0, 1, or 2.

6.11.3 Using a WD90C26A with an External Synthesizer

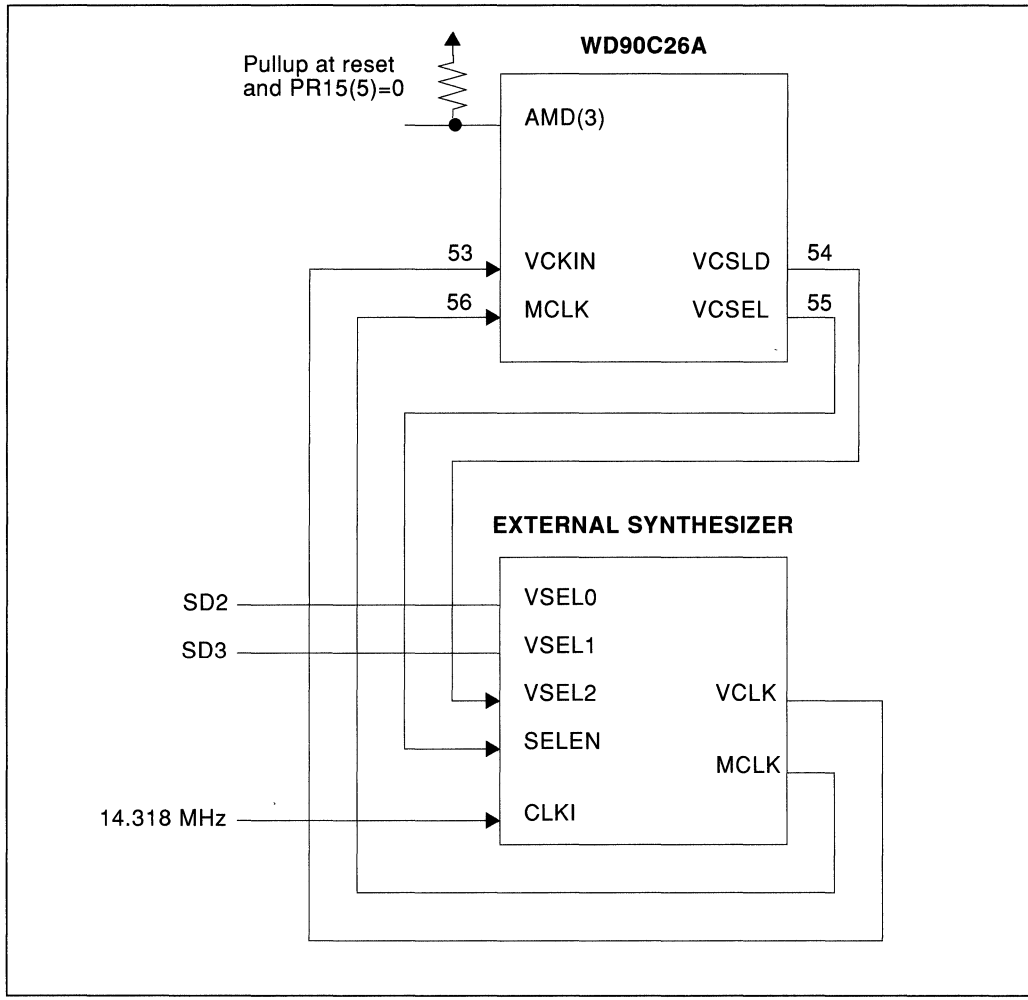


FIGURE 6-18 USING A WD90C26A WITH AN EXTERNAL SYNTHESIZER

Configure the WD90C26A for operation with an external synthesizer by pulling [AMD(3) high at reset and setting PR15 register bit 5 to 0. Then, pin 53 on the WD90C26A is an input for the synthesized frequency from the clock synthesizer chip. Pin 54 on the WD90C26A becomes a write strobe output that is activated on system I/O writes to address 3C2h. This is the address of the VGA miscellaneous output register. By connecting system data bits 2 and 3 to select lines on the multiplexer, writes by BIOS or applications to 3C2h bits 2 and 3 perform video frequency selection from the external synthesizer instead of from the internal multiplexer.

Pin 55 can be used as a select line to choose an alternate bank of available frequencies for ISO refresh rates or as a lock bit to disable external synthesizer changes. Pin 55 is controlled by PR2 register bit 1 in this mode.

In this mode MCLK can still be selected as the internal VCLK source by setting PR15 register bit 4.

6.11.4 Using a WD90C26A with an External Clock Multiplexer

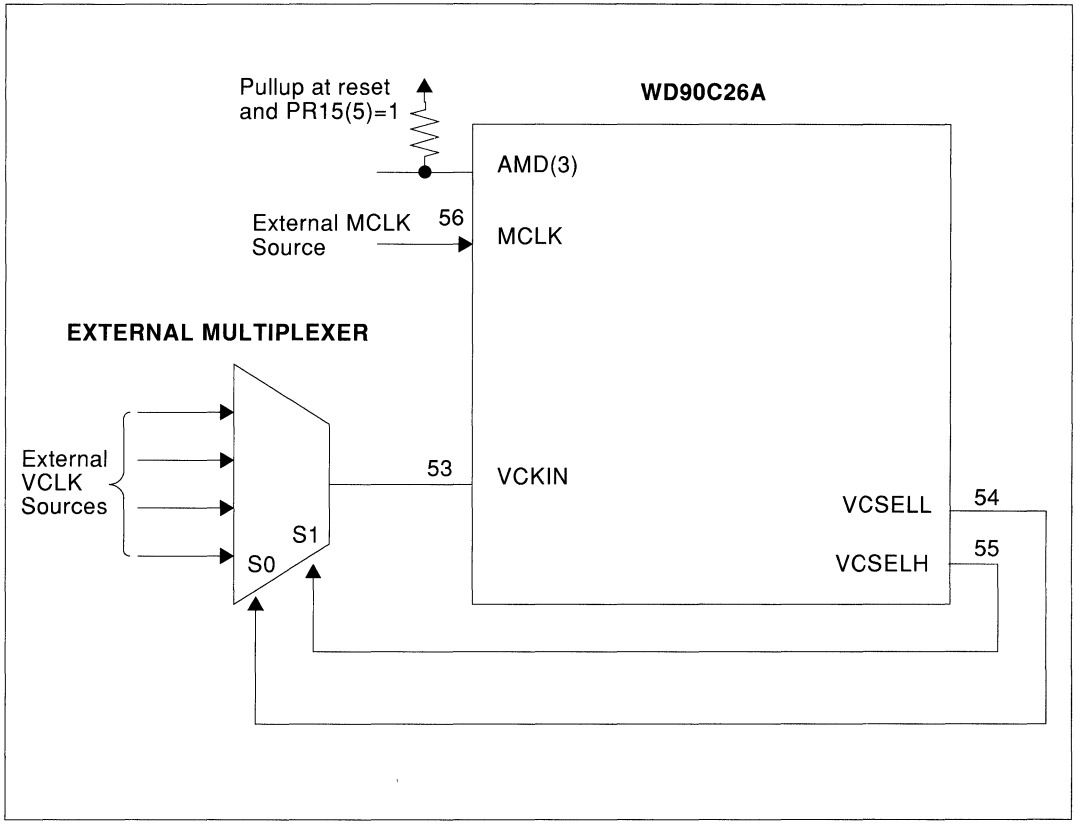


FIGURE 6-19 USING A WD90C26A WITH AN EXTERNAL CLOCK MULTIPLEXER

Configure the WD90C26A for operation with an external multiplexer by pulling AMD(3) high at reset and setting PR15 register bit 5 to 1. Then, pin 53 on the WD90C26A is an input from an external VCLK source multiplexer. Pins 54 and 55 on the WD90C26A become select lines to the external multiplexer and are set to the same levels as the miscellaneous output register 3C2h bits 2 and 3 respectively.

In this mode, MCLK can be selected as the internal VCLK source by setting PR15 register bit 4.

6.11.5 Typical Oscillator or Clock Frequencies for Standard VGA Monitor Support

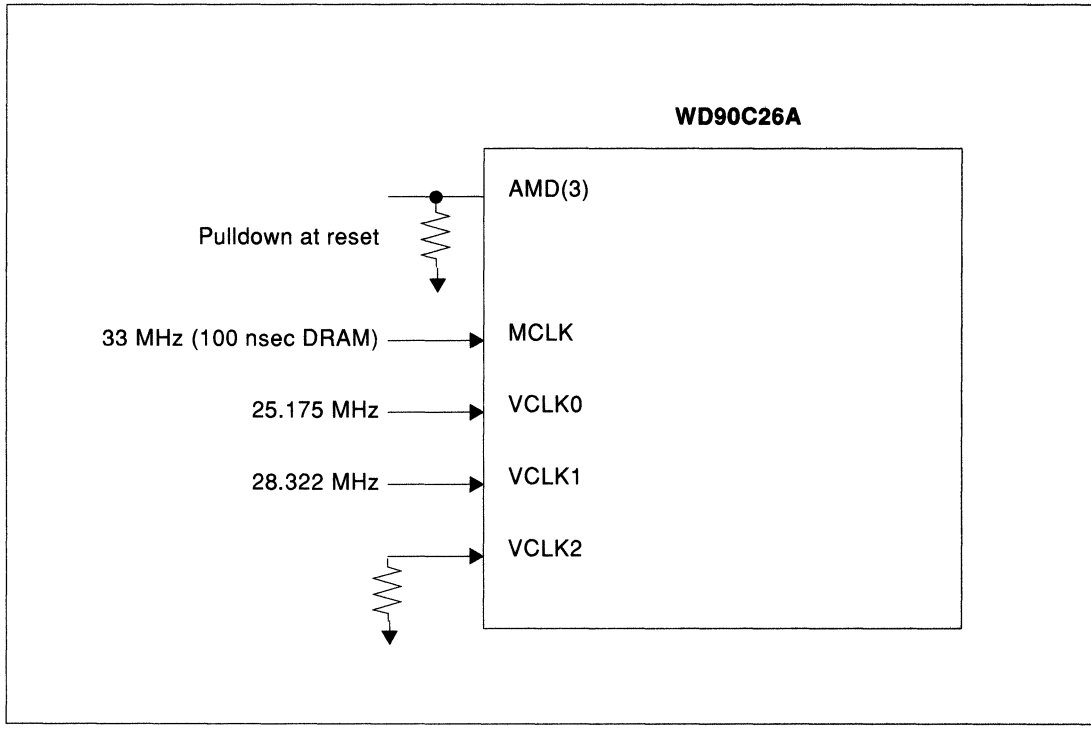


FIGURE 6-20 TYPICAL OSCILLATOR OR CLOCK FREQUENCIES FOR STANDARD VGA MONITOR SUPPORT

For typical applications where compatibility with VGA monitors is desired, VCLK0 is supplied with a 25.175 MHz source and VCLK1 with a 28.322 MHz source. VCLK2 is typically unused.

6.12 PANEL INTERFACING

6.12.1 Introduction

The WD90C26A supports several different types of flat panel designs. A combination of Paradise Register and configuration bit settings are used to interface the WD90C26A to each flat panel type. Tables 6-8 and 6-9 provide general information on characteristics of flat panel support configurations and general guidelines on how to set up the WD90C26A for each type of flat panel.

NOTE

Some panel modes have particular timing or interface requirements that are not addressed in these tables.

In addition to the panel interfaces listed, the WD90C26A interfaces with the WD90C55, which provides additional panel support flexibility.

This section is divided as follows:

- Pin Functions
- 12-Bit Panel Interface
- System Interface when Using a 12-Bit Panel

The following figures and tables are included:

- Types of Panel Interfaces (Table 6-10)
- Pin Functions for Types of Panel Interfaces (Table 6-11)
- Monochrome LCD Panel Interface (Figure 6-21)
- Multiplexed Color Stn 8/16 Bit Interface (Figure 6-22)
- 9-Bit Color LCD Panel Interface (Figure 6-23)
- 12-Bit Color LCD Panel Interface (Figure 6-24)
- 4-Bit Monochrome Plasma Panel Interface (Figure 6-25
- Dual Panel LCD Data Organization (Figure 6-26)
- Single-panel Multiplexed STN Color LCD Data Organization (Figure 6-27)
- Using BLW1M when Connecting a 12-Bit RGB Panel Interface (Figure 6-28)
- Using $\overline{\text{SMEMR}}$ and $\overline{\text{SMEMW}}$ when Connecting a 12-Bit RGB Panel Interface (Figure 6-29

6.12.2 Pin Functions

Table 6-11 lists the functions of interface pins for each type of interface.

NOTE

Control signal requirements for individual panel models may vary, therefore control signal usage listed by panel type is general.

6.12.3 12-Bit Panel Interface

When using a color panel with a 12-bit interface the LA22 through 21 address inputs become re-defined as the least significant red, green, and blue bits of the 12-bit interface. This makes it necessary for the system to provide the WD90C26A with decodes of the memory addresses in the "below-1 Mbyte" range. Figures 6-23 and 6-24 show two ways in which this can be done: by using the BLW1M input signal as an indication of address range, or by using the $\overline{\text{SMEMR}}$ and $\overline{\text{SMEMW}}$ memory strobes from the system buses.

Many system logic chips, such as the WD77C10, include an output which decodes addresses in the below-1 Mbyte range.

TYPE OF INTERFACE[1]	DUAL 4-BIT MONO LCD[2]	DUAL 3-BIT COLOR INTERFACE[3]	9-BIT COLOR LCD[4]	12-BIT COLOR LCD[5]	4-BIT PLASMA NON-PWM[6]	8-BIT PLASMA NON-PWM[7]	4-BIT EL[8]
VIDEO DATA ORGANIZATION	4 pixel upper panel, 4 pixel lower panel per shift clock. One bit per pixel.	2 adjacent pixel triads per shift clock: 1 bit per triad color. 1 background bit.	Single pixel triad per shift clock, 3 bits per triad color for a total of 9 bits per pixel.	Single pixel triad per shift clock, 4 bits per triad color for a total of 12 bits per pixel.	Single pixel per shift clock, 4 bits per pixel.	2 adjacent pixels per shift clock. 4 bits per pixel	Single pixel per shift clock, 4 bits per pixel.
PALETTE	64 shades NTSC conversion from internal 256K palette.	256K colors dithered from internal 256K palette.	27K colors dithered from internal 256K palette.	4K undithered subset of 256K internal palette.	16 of 64 shades NTSC conversion from internal 256K palette.	16 of 64 shades NTSC conversion from internal 256K palette.	16 of 64 shades NTSC conversion from internal 256K palette.
METHOD OF INTERFACE SELECTION	PR18(1,0) = 00 PR18(2)=0 PR39(5)=0) CNF(10)=0 CNF(9)=0	PR18(1,0) = 11 PR18(2)=0 PR39(5)=1 CNF(10)=1 CNF(9)=1	PR18(1,0) = 11 PR18(2)=1 PR39(5)=1 CNF(10)=1 CNF(9)=1	PR18(1,0) = 11 PR18(2)=1 PR39(5)=1 CNF(10)=1 CNF(9)=1 CNF(7)=1	PR18(1,0) = 01 PR18(2)=0 PR19(7)=0 CNF(10)=0 CNF(9)=1	PR18(1,0) = 01 PR18(2)=0 PR19(7)=1 CNF(10)=0 CNF(9)=1	PR18(1,0) = 10 PR18(2)=0 CNF(10)=1 CNF(9)=0
COLOR PALETTE/GRAY SCALE OPTIONS	Mapping RAM - All 64 gray shades to 64-step gray scale.	Selectable 4K/256K colors.	Selectable 2/4 frame dithering or space only dithering.	4K direct dithered colors	Mapping RAM - All 64 gray shades to 16-step gray scale.	Mapping RAM - All 64 gray shades to 16-step gray scale.	

TABLE 6-10 TYPES OF PANEL VIDEO INTERFACES

NOTE: For notes, refer to next page.

PIN NO.	SIGNAL NAME	DUAL 4-BIT MONO LCD[2]	DUAL 3-BIT COLOR LCD[3]	9-BIT COLOR LCD[4]	12-BIT COLOR LCD[5]	4-BIT PLASMA NON-PWM[6]	8-BIT PLASMA NON-PWM[7]	4-BIT EL[8]
VIDEO DATA PINS								
89	LA22/RL				R0			
88	LA21/GL				G0			
87	LA20/BL				B0			
100	UD3	UD0	R1	R2	R3	VD3	D03	VD3
99	UD2	UD1	G1	R1	R2	VD2	D02	VD2
98	UD1	UD2	B1	R0	R1	VD1	D01	VD1
97	UD0	UD3	BORDER	G2	G3	VD0	D00	VD0
95	LD3	LD0	R2	G1	G2		D13	
94	LD2	LD1	G2	G0	B1		D12	
93	LD1	LD2	B2	B2	B3		D11	
92	LD0	LD3		B1	B2		D10	
91	RPLT/B0			B0	B1			
PANEL SYNC PINS								
107	FR/ $\overline{\text{BLANK}}$	FR	FR	FR	FR			
106	FP	FP	FP	FP	FP	VS	VS	VS
105	LP	LP	LP	LP	LP	HS	HS	HS
104	ENDATA	WGTCLK	WGTCLK	WGTCLK	WGTCLK	ENABLE	ENABLE	ENABLE
101	XSCLK	XSCLK	XSCLK				XSCLK	XSCLK

TABLE 6-11 PIN FUNCTIONS FOR TYPES OF PANEL VIDEO INTERFACES

NOTES:

The following notes apply to the column heads for Tables 6-10 and 6-11.

1. The column heads represent seven types of flat panels interfaced by the WD90C26A.
2. Dual Panel, Dual 4-bit, Monochrome LCD Panel Interface designed for passive matrix panel support. For the WD90C26A, UD0 is the leftmost pixel of UD(3:0), which corresponds to the UD3 pin on most monochrome LCD panel interfaces.
3. Single Panel, Dual 3-bit, Color LCD Panel Interface designed for passive matrix multiplexed supertwisted nematic (STN) panel support via a WD90C55.
4. Single Panel, 9-bit, Color LCD Panel Interface designed for active matrix thin-film transistor (TFT) panel support.
5. Single Panel, 12-bit, Color LCD Panel Interface (TFT)
6. Single Panel, 4-bit Monochrome, Plasma Panel Interface non-Pulse Width Modulated (PWM)
7. Single Panel, Dual 4-bit Monochrome, 8-bit Plasma Panel Interface (Non -PWM)

8. Single Panel, 4-bit, Monochrome, Electro-Luminescent (EL) Panel Interface.

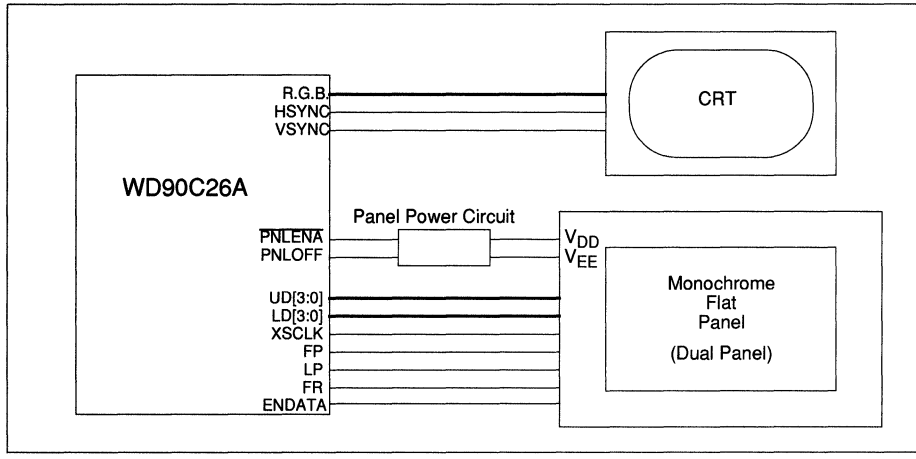


FIGURE 6-21 MONOCHROME LCD PANEL INTERFACE

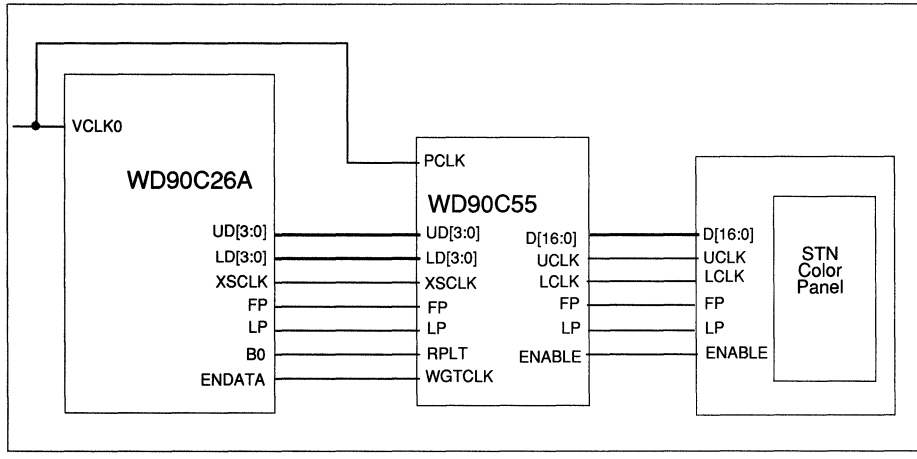


FIGURE 6-22 MULTIPLEXED COLOR STN 8/16 BIT INTERFACE

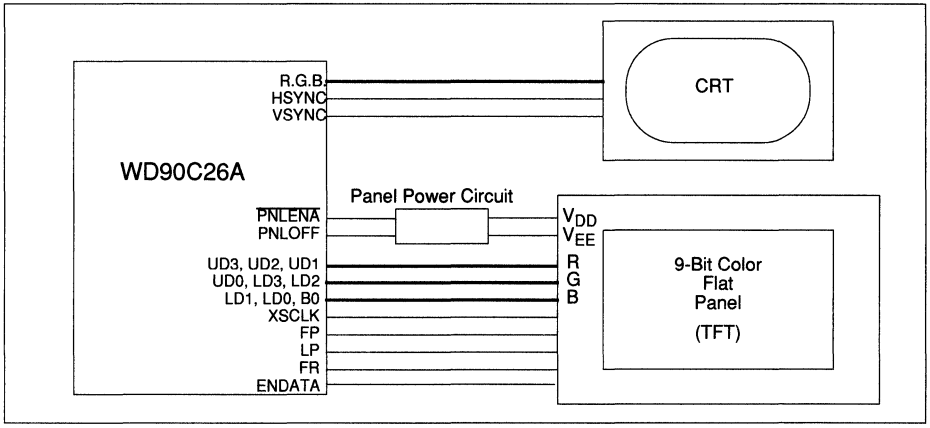


FIGURE 6-23 9-BIT COLOR LCD PANEL INTERFACE

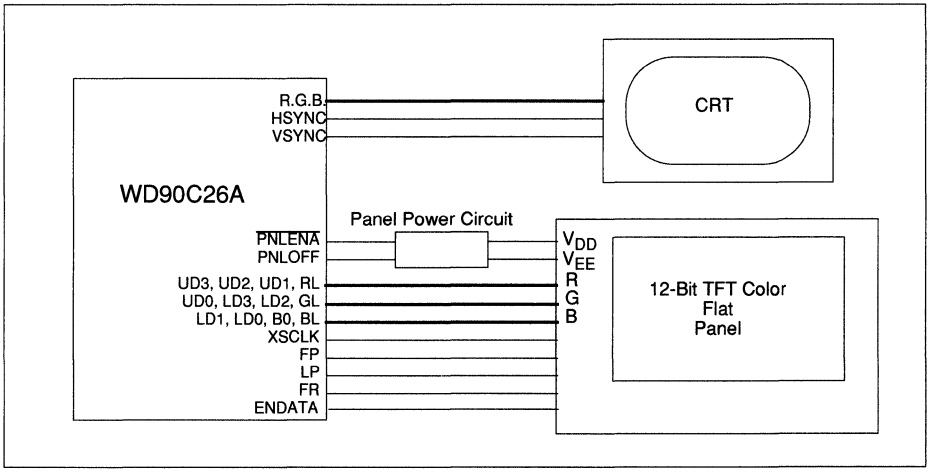


FIGURE 6-24 12-BIT COLOR LCD PANEL INTERFACE

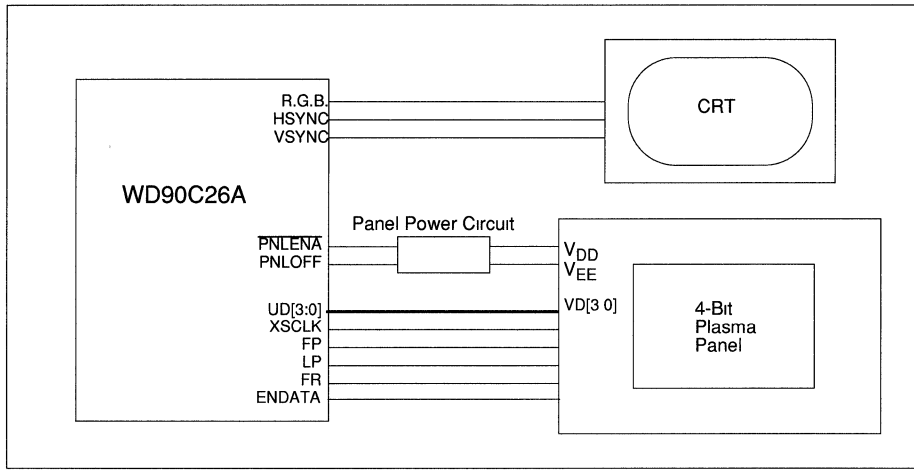


FIGURE 6-25 4-BIT MONOCHROME PLASMA PANEL INTERFACE

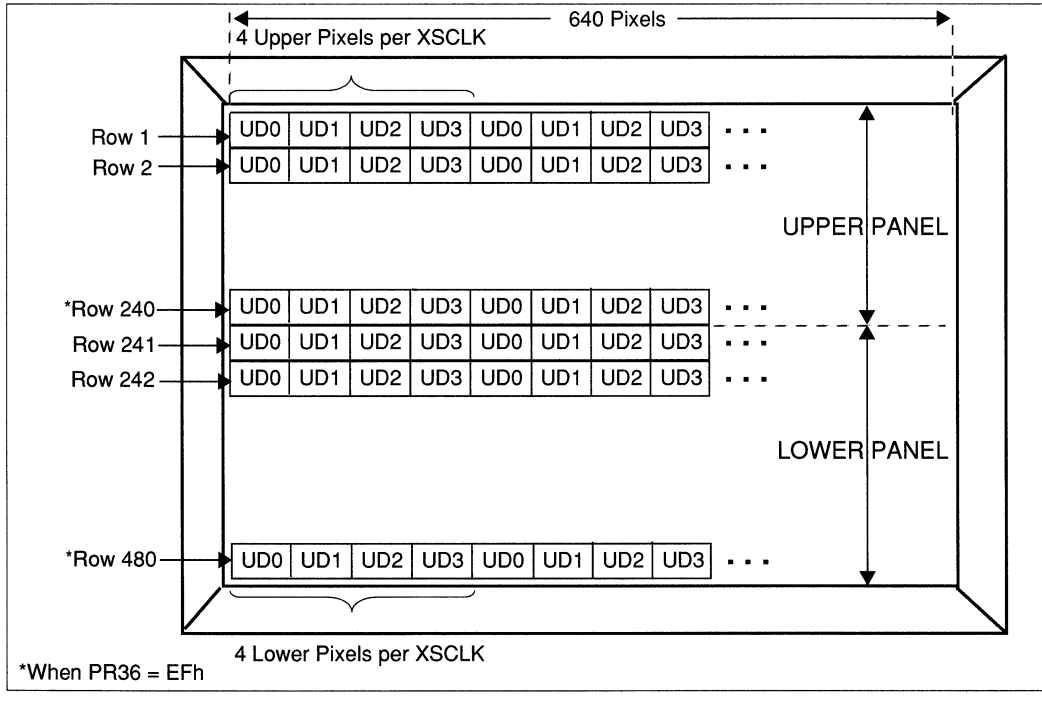


FIGURE 6-26 DUAL PANEL LCD DATA ORGANIZATION

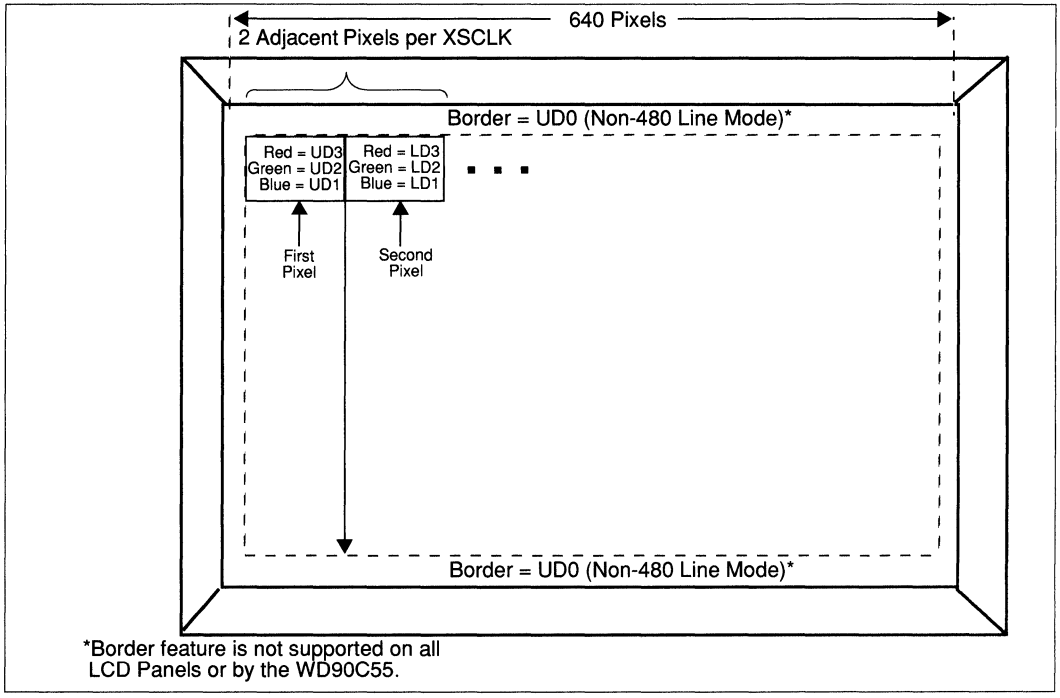


FIGURE 6-27 SINGLE-PANEL MULTIPLEXED STN COLOR LCD DATA ORGANIZATION (BEFORE WD90C55 8/16 BIT STN INTERFACE CONVERSION)

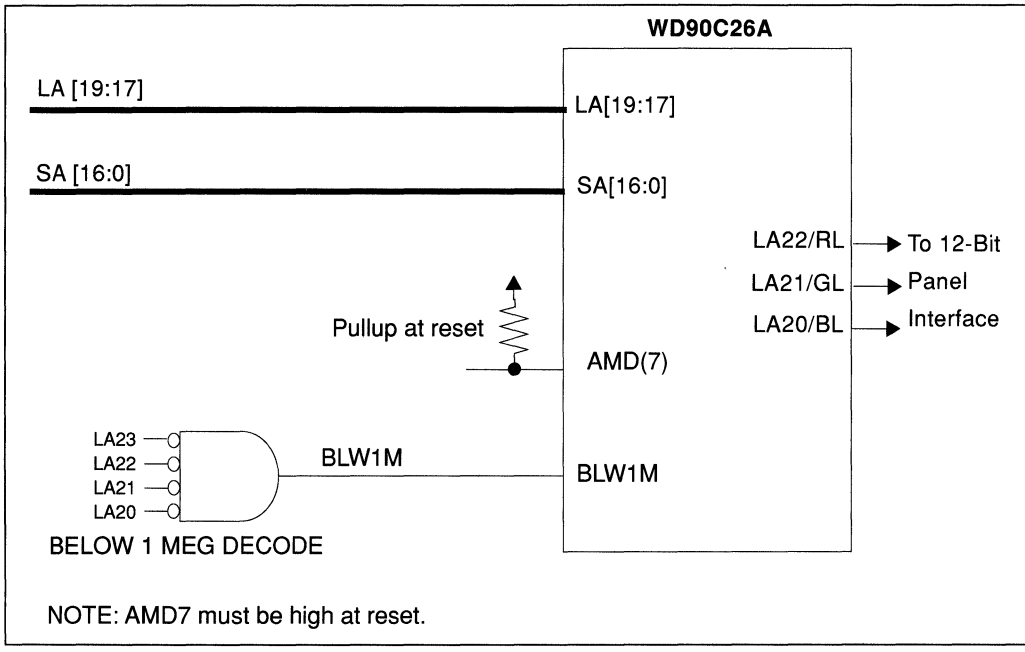


FIGURE 6-28 USING BLW1M WHEN CONNECTING A 12-BIT RGB PANEL INTERFACE

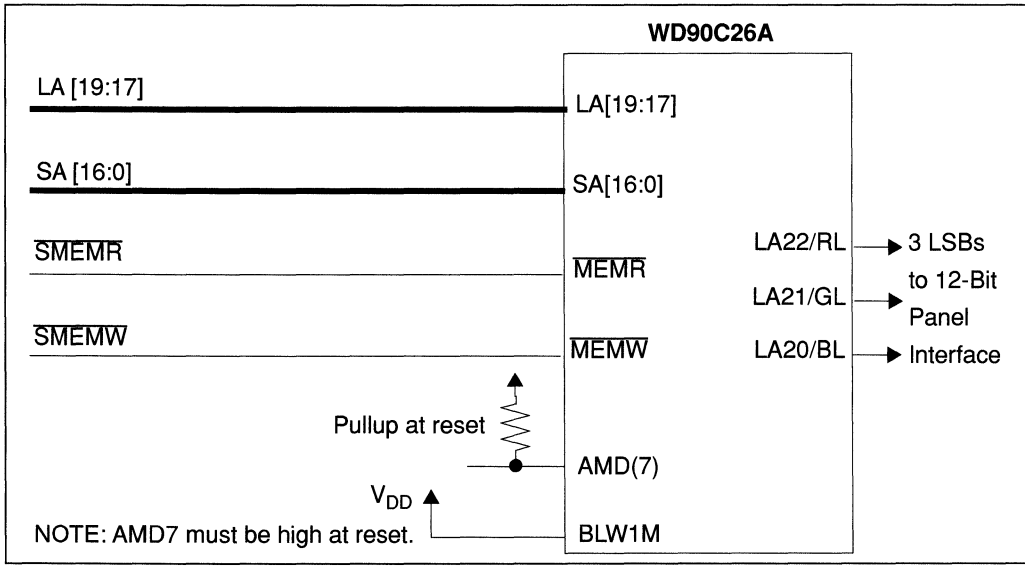


FIGURE 6-29 USING $\overline{\text{SMEMR}}$ AND $\overline{\text{SMEMW}}$ WHEN CONNECTING A 12-BIT RGB PANEL INTERFACE

6.13 CRT INTERFACE

6.13.1 Introduction

This section provides the following information:

- Calculating the R_{SET} Value (Figure 6-30)
- Internal RAMDAC Monitor Detection (Figure 6-31)
- Internal RAMDAC Outputs
- VSYNC and HSYNC Connections

6.13.2 Calculating R_{SET} Value

The I_{DAC} output currents I_{RED}, I_{GREEN}, and I_{BLUE} develop a voltage across the load resistance R_{LD}. These voltages are compared against a voltage derived from the external voltage reference V_{REF}.

The output current (I_{DAC}) is determined with the following formula:

$$I_{DAC} = \frac{V_{REF} \times 1.067 \times code}{R_{SET}}$$

where the code range from 0 to 63 (0h to 3Fh) is for 6-bit DACs. Using the full-scale code of 63 and an R_{SET} value of 5.9 Kohms in the formula yields a full-scale I_{DAC} value of 14.071 mA for each DAC output.

NOTE:

R_{SET} values must be selected that do not violate the maximum full scale current limits.

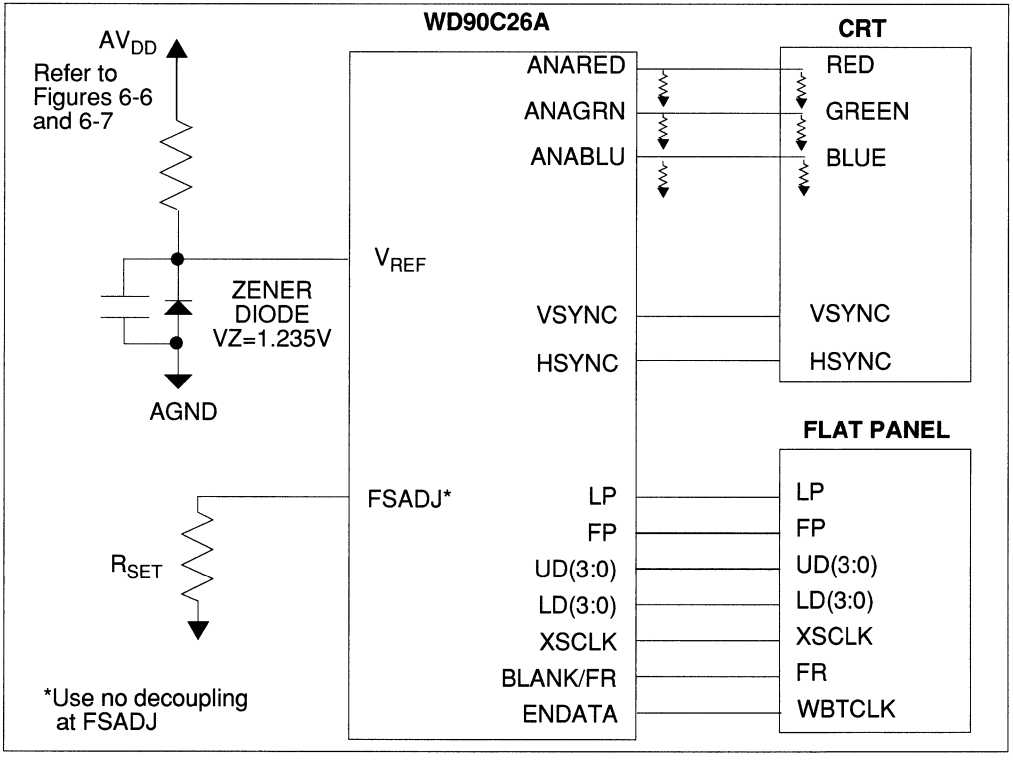


FIGURE 6-30 EXAMPLE OF CRT INTERFACE SHOWING V_{REF} AND FSADJ CIRCUITS

6.13.3 Internal RAMDAC Monitor Detection

Figure 6-31shows the monitor detection connections for the internal RAMDAC.

The output signal MDETECT is readable at port 3C2h bit 4.

NOTE

It is important to read MDETECT during active video output. Do not read MDETECT during retrace or any other blanking period.

The internal monitor detection circuit of the WD90C26A is designed to allow detection of whether or not a monitor is connected to CRT out puts and also if that monitor is monochrome only or color. The monitor detection circuit relies on differences in voltages at DAC outputs depending on whether a CRT is attached that has internal RGB termination resistors.

Voltages generated at DAC outputs are compared against an internal reference that is approximately the half-scale voltage if a monitor were attached. If voltages on all three DAC outputs are below this internal reference voltage, then the MDETECT signal goes active. The active MDETECT can be read as bit 4 high in VGA Input Status Register 0 (I/O address 3C2h).

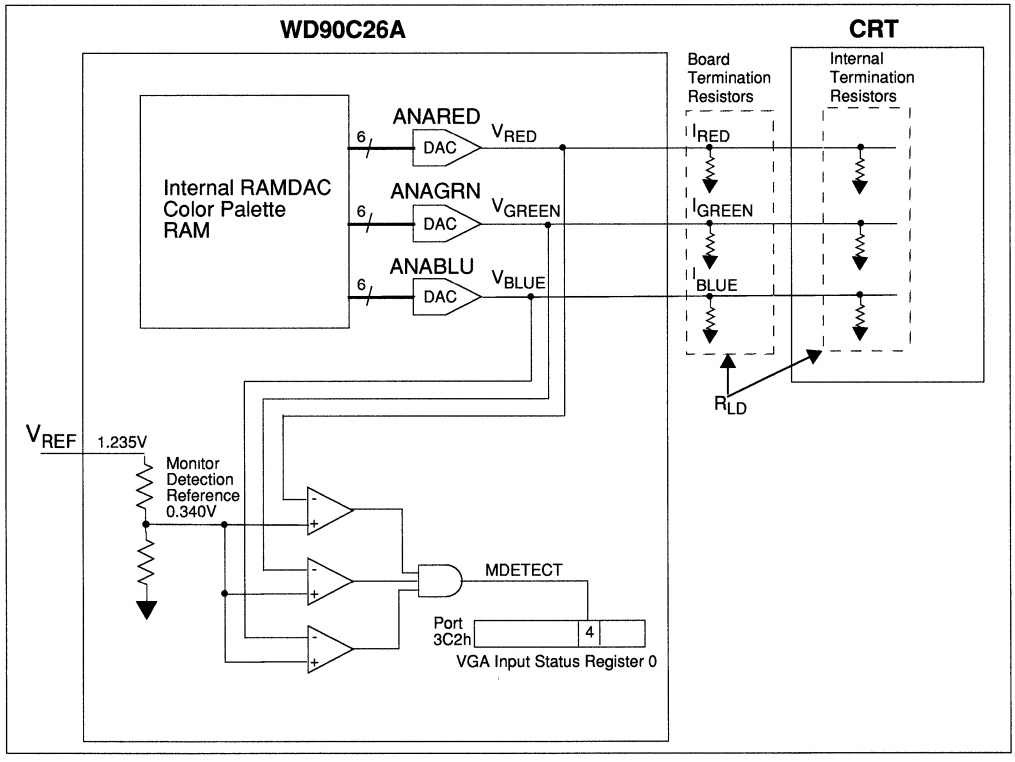


FIGURE 6-31 MONITOR DETECTION CIRCUIT FOR INTERNAL RAMDAC

Typically monitors have a 75 Ohm internal termination and boards have either a 150 Ohm or 75 Ohm source termination. From the source termination value and 75 Ohm monitor termination an R_{LD} value can be calculated, and from that the relationship between DAC output voltage, R_{LD}, and DAC input code can be determined by using the equation in the previous section. Then, DAC codes can be supplied to each of the three internal DACs that should cause the generated voltages at the DAC outputs to be below the monitor detect reference voltage if a monitor is attached, or above the monitor detect voltage if no monitor is attached.

By separately programming each DAC code so that only one of the comparators would change output based on the monitor connection the red, green, and blue monitor connections can be separately sensed. This allows the detection of whether a monochrome-only monitor is attached by looking for green monitor connection, with red and blue monitor connections missing.

DAC codes are controlled by reprogramming the color palette RAM of the internal RAMDAC during monitor detect functions. It is recommended that monitor detect operations be done at power-up to avoid the need to save and restore RAMDAC palette contents required by an application.

The monitor detection comparators require stable DAC output voltages for a minimum of 300 nanoseconds in order to correctly indicate monitor detect status at 3C2h bit 4. To allow DAC outputs to remain stable for this minimum period and to allow reading of the results of monitor detect, it is recommended that CRTC parameters be adjusted during the test to eliminate blanking periods that would disable DAC outputs. After monitor detect functions have completed, CRTC parameters would be returned to their normal values.

6.13.4 Internal RAMDAC Outputs

Pins 73 through 75 are the analog PS/2 monitor compatible video outputs. They are active when the WD90C26A has been configured to drive a CRT monitor. Otherwise, Pins 73 through 75 are zero-current outputs because the DAC portion of the WD90C26A is only operational when an external CRT is being driven from the internal RAMDAC.

In most applications, Pins 73 through 75 are doubly terminated with 150 Ohm loads (on the PC board) from each pin to ground, and also within a PS/2 compatible monitor from each signal to ground.

Pins 73 through 75 are zero-current outputs when the WD90C26A is not enabled or when it is in powerdown modes where screen display does not occur. Pins 73 through 75 are also shut off when the WD90C26A is performing retrace activities.

6.13.5 VSYNC and HSYNC Connections

NOTE

VGA monitors that are fully IBM compatible can be driven directly by the VSYNC and HSYNC pins. Older, noncomplying monitor designs may require external buffering.

For VGA compatible monitor connections, VSYNC and HSYNC polarity settings are used by some monitors to adjust screen resolution. Standard VGA monitor resolution selection is shown in the following table. These bits determine the vertical size of the vertical frame by the monitor. Their encoding is also shown in the table.

HSYNC PULSE LEVEL	VSYNC PULSE LEVEL	Vertical Frames
+	+	Reserved
+	-	350 Lines/Frame
-	+	400 Lines/Frame
-	-	480 lines/Frame

The WD90C26A allows control of VSYNC and HSYNC polarity selection as well as allowing locking of selected polarities.

NOTE

For Simultaneous Display Mode operation, VSYNC and HSYNC pulse polarities are set and locked to 480 lines per frame.

6.13.6 Selecting the CRT Interface

The following table lists the setting for PR18 and PR19 required to select the CRT or panel display. The table also indicates which categories of CRTC Shadow Register values should be used for the proper timing of CRT or panels displays.

PR18 (1)	PR18 (0)	PR19 (5)	PR19 (4)	CRTC PARAM (TIMING)
0	0	0	1	LCD
0	0	1	0	CRT
0	1	0	1	Plasma
0	1	1	Note	CRT
1	0	0	1	EL
1	0	1	Note	CRT

NOTE

If both PR19 bits 4 and 5 are both set to 1, program CRTC parameters for simultaneous display.

6.14 MAPPING RAM PROGRAMMING

The 64x6 mapping RAM is designed for dithering pattern selection. This memory is used to adjust the color-to-gray scale mapping from the weighting equation. This mapping RAM is read from or written to by the CPU. The outputs from the weighting equation (6 bits) are connected to the inputs of the mapping RAM (address input). The outputs of the mapping RAM (6 bits) are connected to the dithering logic. For plasma display support, the lower four bits of mapping RAM output are connected to the panel interface circuit. (See Figure 2-2.)

NOTE

To program mapping RAM, PR19 register bit 4 must be set to 1 and no powerdown modes can be active.

Before accessing the mapping RAM, PR31 register bit 0 should be set to 0. The following procedure describes a write access to the mapping RAM. A similar procedure is followed to read mapping RAM values.

NOTE

In ISA Mode, the internal mapping RAM is an 8-bit I/O device. In MicroChannel mode, the internal mapping RAM is an 8-bit resource.

1. Load PR1B with A0h to unlock the Flat Panel Registers.
2. Load PR20 with 48h to unlock Sequencer Extended Registers
3. Set PR31 bits 1 and 0 low to disable $\overline{\text{IOCS16}}$/$\overline{\text{CDDS16}}$.
4. Set PR30A bit 4 to '1' to disable 16-bit system interface
5. Disable system interrupts to prevent undesired access of mapping RAM
6. Poll VGA Status Register I and wait for display inactive and retrace active.
7. Load PR30 with 30h to unlock the mapping RAM
8. Load PR33 with the desired mapping RAM address(00-3Fh)
9. Do a 'dummy read' to other-than-PR34 CRTC index
10. Write the desired mapping RAM value into PR34
11. Wait the minimum of 4 VLCK and MCLK cycles.
12. Repeat steps 7-11 until the mapping RAM is programmed as desired.
13. Change the CRTC index to other-than-PR34
14. Do a 'dummy read' to other-than-PR34 CRTC index.
15. Set PR30 to 00h to lock the mapping RAM
16. Re-enable system interrupts.

NOTE

There is a recovery time requirement between two consecutive mapping RAM reads or writes of 4 VCLK and 4 MCLK periods. Appropriate measures should be taken in firmware to ensure this recovery time is met.

6.15 USING AN EXTERNAL RAMDAC

The WD90C26A is used with an external RAMDAC when special color modes are required and are not available with the VGA compatible internal RAMDAC.

Figure 6-32 shows a typical connection for an external RAMDAC.

NOTE

The RPLT signal should not be used to strobe data out of an external DAC onto the SD bus. Palette reads in the WD90C26A always access the internal RAMDAC.

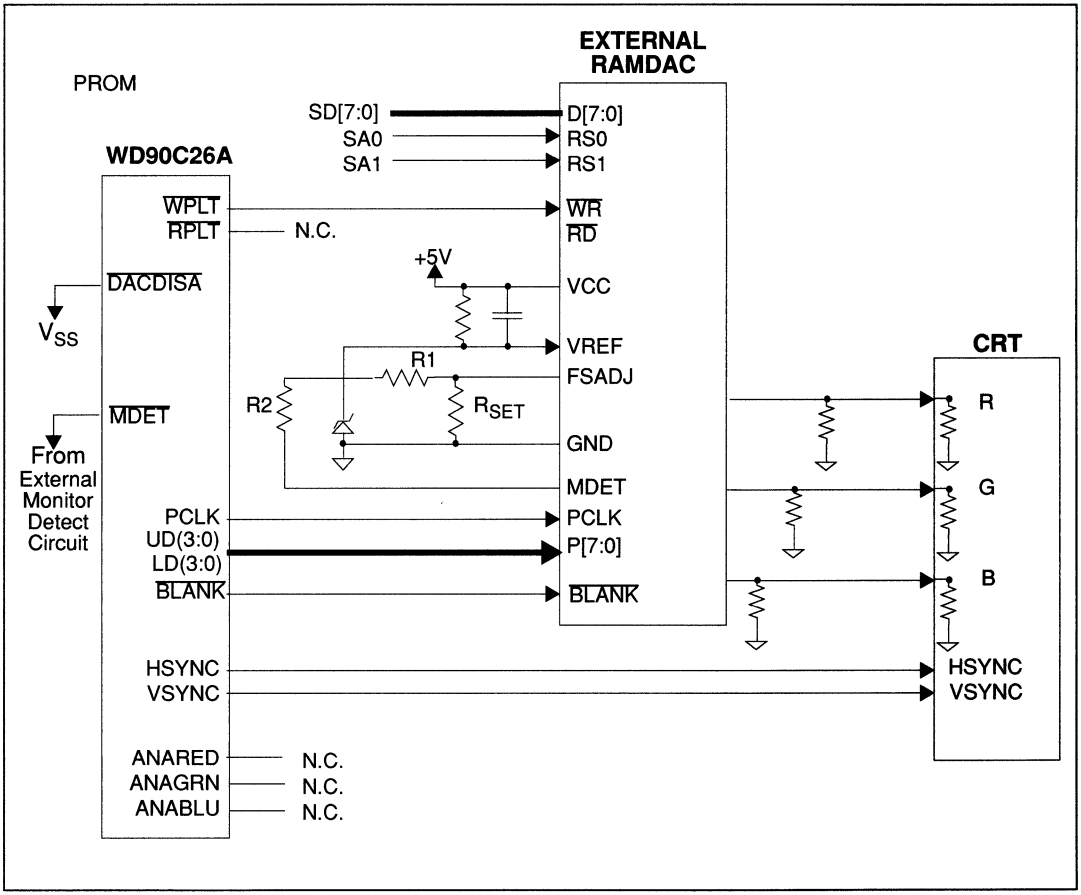


FIGURE 6-32 WD90C26A WITH EXTERNAL RAMDAC INTERFACE

6.16 VIDEO SIGNATURE ANALYZER

The WD90C26A contains a signature analyzer circuit that records 16-bit digital signatures of video frames, previous to their conversion to analog colors by the internal RAMDAC. A unique 16-bit signature can be generated for a given frame of video data. Then, the generated signature can be used to verify correctness of the video output and system function.

The basis of the signature analyzer is a linear feedback shift register, or LFSR. The LFSR implements the CCITT CRC16 polynomial of $x_{16}+x_{12}+x_5+1$, adapted from serial implementation to one accepting the 8 bits of RAMDAC input. The inputs to the LFSR are connected to the 8 bit internal RAMDAC inputs which represent the video data previous to RAMDAC color lookup, weighting, gray scale mapping, dithering, etc.

For non-interlaced video modes, the signature analyzer samples video data over single frame intervals. For interlaced video modes, the video signature is generated over an odd and even pair of frames.

When the signature analyzer is enabled it begins shifting in the video signature at the falling edge of the internal VSYNC signal. Video signal generation is complete at the rising edge of the internal VSYNC so that the signature represents an entire display screen of video information.

For interlaced video modes, signal generation is complete at the rising edge of the internal VSYNC following the second frame of the odd and even pair of frames.

The signature analyzer is controlled by its own register at PR45. This register cannot be accessed for reads or writes until the general read/write locks of PR20 are removed. The setting of PR20 (3?5.06h) to 48h allows signature analyzer registers to be accessed. PR45 bit 3 must also be set to 1 to allow reading of the low and high bytes of the signature from PR45A and PR45B, respectively.

The sequence of operations required for the LFSR to capture a video frame signature is as follows:

1. Set PR20 to 48h, which enables read/write of signature analyzer registers.
2. Set PR45 register bit 3 to 1, which enables reading of the signature from PR45A and PR45B.
3. Set PR45 register bit 0 to 0 to disable signature generation.
4. Set PR45 register bit 1 to 0 and then set it back to 1, which initializes the signature to 0001h.
5. Verify that the signature is initialized by checking the contents of PR45A and PR45B as follows:

   PR45A = 01h
   PR45B = 00h
6. Set PR45 register bit 0 to 1, to enable the capturing of a frame signature.
7. Wait for a minimum of two VSYNC intervals before reading the video signature.
8. Read low and high bytes of the captured signature from PR45A and PR45B.
9. Compare the captured signature against the expected values for a given screen display.
10. Change PR20 settings to lock the signature analyzer control register and stop signature analyzer functions.

6.17 READING THE WD90C26A DEVICE ID

To read the device ID, the WD90C26A has a register bank that can be overlaid on Paradise registers 3?5.31h through 3?5.3Fh. The device ID is accessed, instead of the normal PR registers, by performing the following steps:

1. Set PR1B (3?5.34) to any value except 101xxxxxb to allow register overlaying by PR10.
2. Set PR30 to 00h to ensure that the mapping RAM registers are locked.
3. Set PR10 to 1xxx0xxxb to overlay the WD90C26A device ID on Paradise registers 3?5.31h through 3?5.3Fh (15 bytes).
4. Read the device ID from Paradise registers 3?5.31h through 3?5.3Fh. The values read are encoded in standard ASCII with one byte per character in the following string:

   WD90C26AREVx199y

   where **x** indicates the revision level (A through Z) and **y** indicates the last digit of the year (0 through 9).

NOTE

The revision level and year represent the die revision only and do not indicate bond-out, package, or parameter range options.

6.18 I/O MAPPING

This section provides the following information:

- A Description of WD90C26A I/O Mapping
- A list of I/O Mapping groups (Table 6-12)
- An I/O Mapping Group Diagram (Figure 6-31)

The I/O Mapping allows the WD90C26A to enter a test mode where all of its pins are divided into groups with inputs and outputs. The path for each group goes from the input pin(s), through the WD90C26A, and to the output pin. Each group can be treated as a separate resistive path to check for open and shorted circuits within the group and between groups. Table 6-12 lists each group (path) with its corresponding input and output pins.

The WD90C26A must meet the following four requirements in order to enter the I/O Mapping test mode.

- $\overline{\text{MEMR}}$ is LOW
- $\overline{\text{IOR}}$ is LOW
- CNF(2) is HIGH (AMD2 is pulled high)
- RESET is ACTIVE HIGH then goes LOW
- $\overline{\text{PWRDOWN}}$ is HIGH

If both $\overline{\text{MEMR}}$ and $\overline{\text{IOR}}$ are low at the same time, it becomes an illegal condition in ISA(AT) machines and a reserved condition in the PS/2 machines. AMD2 high ensures that WD90C26A is in ISA(AT) mode.

Reset controls a transparent latch as shown in Figure 6-30:

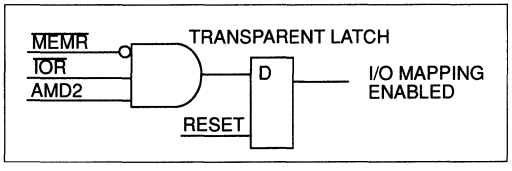


FIGURE 6-33 ENABLING I/O MAPPING ON THE WD90C26A

Figure 6-31 provides a diagram of the I/O mapping groups (paths).

INPUT PINS		OUTPUT PINS	
PIN	**NAME**	**PIN**	**NAME**
26	SD9	140	$\overline{\text{ARAS}}$
25	SD10	141	$\overline{\text{AWE}}$
119	BMD7	1	BMA8
20	SD15	13	$\overline{\text{PNLENA}}$
21	SD14	11	$\overline{\text{BRAS}}$
22	SD13	12	$\overline{\text{BWE}}$
23	SD12	14	PNLOFF/ $\overline{\text{WPLT}}$
24 128	$\overline{\text{REFRESH}}$ $\overline{\text{BCAS}}$	129	$\overline{\text{AOE}}$
27	SD8	130	AMA8
29 34	$\overline{\text{MEMW}}$/S0 $\overline{\text{SBHE}}$	52	$\overline{\text{0WS}}$/ $\overline{\text{CDSFBLK}}$
30 35	$\overline{\text{MEMR}}$/M/$\overline{\text{IO}}$ BALE/ MADE24	51	IOCHRDY/ CDCHRDY
31 37	$\overline{\text{IOCS16}}$/ $\overline{\text{CDSETUP}}$ $\overline{\text{IOR}}$/S1	19	$\overline{\text{EBROM}}$
38	$\overline{\text{IOW}}$/$\overline{\text{CMD}}$	33	MEMS16/ CDDS16
39	AEN/3C3DO	36	IRQ/$\overline{\text{IRQ}}$
45	SD3	136	AMA3
40	SD7	131	AMA7
41	SD6	133	AMA6
42	SD5	134	AMA5
45	SD4	135	AMA4
46	SD2	137	AMA2
47	SD1	138	AMA1
48	SD0	139	AMA0

TABLE 6-12 I/O MAPPING GROUPS

INPUT PINS		OUTPUT PINS	
PIN	**NAME**	**PIN**	**NAME**
53 56	VCLK0 MCLK	92	LD0
54 57	VCLK1 SA0	93	LD1
55	VCLK2	94	LD2
58 63	SA1 SA6	95	LD3
59 64	SA2 SA7	97	UD0
60 65	SA3 SA8	98	UD1
61 68	SA4 SA9	99	UD2
62 69	SA5 SA10	100	UD3
71	FSADJ/ $\overline{\text{MDET}}$		
72	V_{REF}/ $\overline{\text{DACDISA}}$		
77	SA11	91	$\overline{\text{RPLT}}$/BO
78	SA12	101	XSCLK
79	SA13	104	ENDATA
80	SA14	102	PCLK
81	SA15	105	LP
87 82	LA20/BL LA16	108	HSYNC
83 88	LA17 LA21/GL	107	FR/$\overline{\text{BLANK}}$
84 89	LA18 LA22/RL	106	FP
83 88	LA17 LA21/GL	107	FR/$\overline{\text{BLANK}}$

TABLE 6-12 I/O MAPPING GROUPS

INPUT PINS		OUTPUT PINS	
PIN	**NAME**	**PIN**	**NAME**
83 88	LA17 LA21/GL	107	FR/$\overline{\text{BLANK}}$
84 89	LA18 LA22/RL	106	FP
90 85	LA23/ BLW1M LA19	109	VSYNC
90 85	LA23/ BLW1M LA19	109	VSYNC
110	AMD7	2	BMA7
112 121	AMD5 BMD5	4	BMA5
113 122	AMD4 BMD4	5	BMA4
115 124	AMD3 BMD3	6	BMA3
116 125	AMD2 BMD2	7	BMA2
117 126	AMD1 BMD1	9	BMA1
118 127	AMD0 BMD0	10	BMA0
120 111	BMD6 AMD6	3	BMA6
24 143	SD11 $\overline{\text{ACAS}}$	144	$\overline{\text{BOE}}$

TABLE 6-12 I/O MAPPING GROUPS

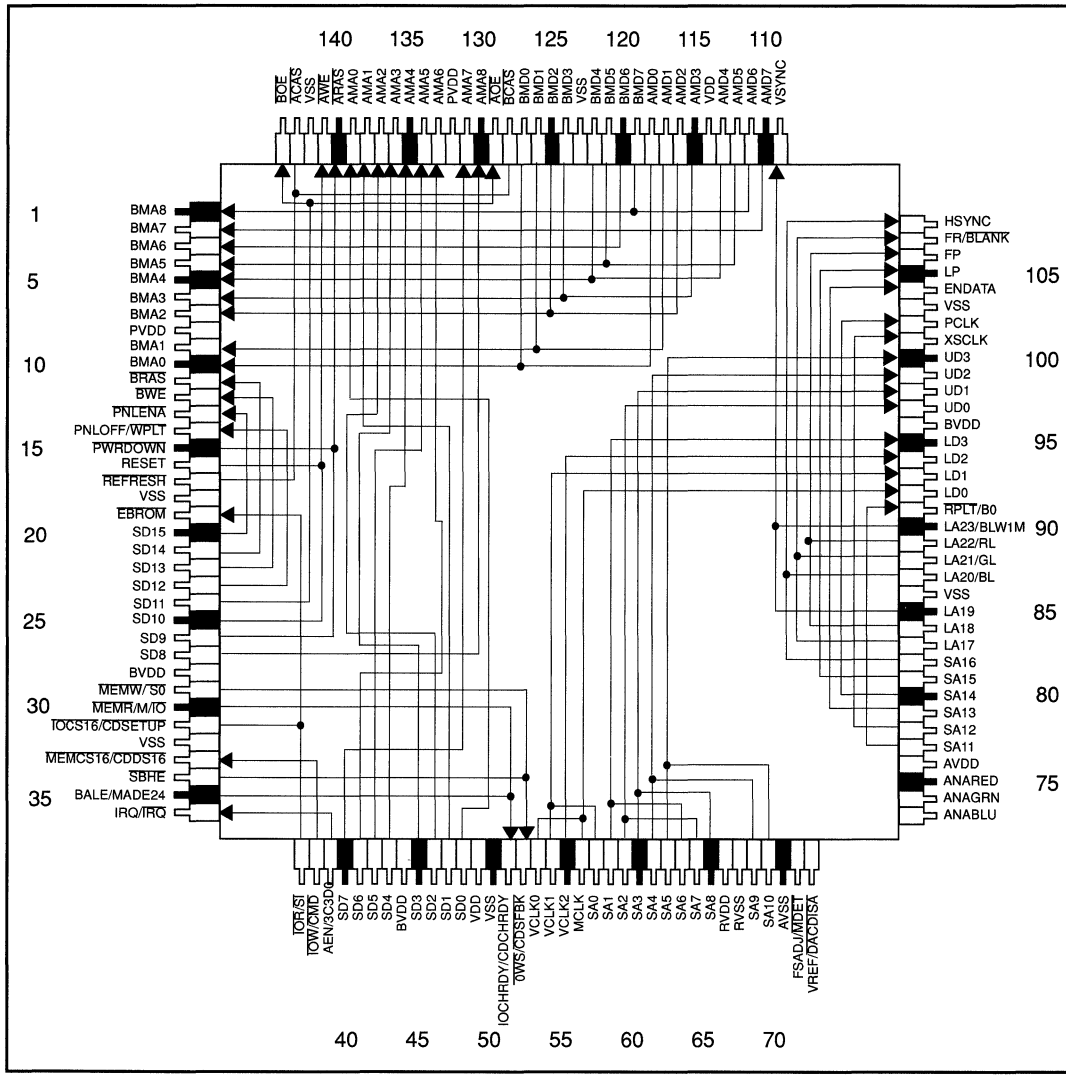


FIGURE 6-34 I/O MAPPING GROUP DIAGRAM

7.0 SCREEN CHARACTERISTICS

7.1 SCREEN CHARACTERISTICS

This section provides information about the WD90C26AA screen characteristics when it is configured to display in the following video modes:

- IBM display mode
- Paradise display mode
- VESA display mode

The video BIOS determines the actual modes in which the WD90C26AA can operate. The tables in this section list characteristics of typically chosen modes (supported in BIOS).

Sync rate and refresh rate characteristics for typical pixel clock rates are given, as well as some refresh rate ranges for conditions where a panel only is being driven. When a panel only is being driven, there is more latitude in selecting refresh rate parameters.

The following tables are included in this section:

- Simultaneous Display Screen Characteristics (IBM, Paradise, VESA Screen Sizes)
- Display Characteristics for Flat Panel Only (IBM, Paradise, VESA Screen Sizes)
- Display Characteristics for CRT Only (IBM, Paradise, VESA Screen Sizes)
- CRT Only Display - Commonly Used Increased Refresh Rates

Mode No. (Hex)	Mode Type	Native Resolution	Displayed CRT Resolution[3]	Displayed Panel Resolution[3]	Alpha Format	Font Size	VCLK[7] Frequency
0,1	Alpha	320x200	640x400/480	640x400/480	40x25	8x8	25.175 MHz
0,1[1]	Alpha	320x350	640x350/480	640x350/480	40x25	8x14	25.175 MHz
0,1[2]	Alpha	360x400	640x400/480	640x400/480	40x25	8x16	28.322 MHz
2,3	Alpha	640x200	640x400/480	640x400/480	80x25	8x8	25.175 MHz
2,3[1]	Alpha	640x350	640x350/480	640x350/480	80x25	8x14	25.175 MHz
2,3[2]	Alpha	720x400	640x400/480	640x400/480	80x25	8x16	28.322 MHz
4,5	Graphics	320x200	640x400/480	640x400/480	40x25	8x8	25.175 MHz
6	Graphics	640x200	640x400/480	640x400/480	80x25	8x8	25.175 MHz
7	Alpha	720x350	640x350/480	640x350/480	80x25	8x14	28.322 MHz
7[2]	Alpha	720x400	640x400/480	640x400/480	80x25	8x16	28.322 MHz
D	Graphics	320x200	640x400/480	640x400/480	40x25	8x8	25.175 MHz
E	Graphics	640x200	640x400/480	640x400/480	80x25	8x8	25.175 MHz
F	Graphics	640x350	640x350/480	640x350/480	80x25	8x14	25.175 MHz
10	Graphics	640x350	640x350/480	640x350/480	80x25	8x14	25.175 MHz
11	Graphics	640x480	640x480	640x480	80x30	8x16	25.175 MHz
12	Graphics	640x480	640x480	640x480	80x30	8x16	25.175 MHz
13	Graphics	320x200	640x400/480	640x400/480	40x25	8x8	25.175 MHz
5E/100[9]	Graphics	640x400	640x400/480[3]	640x400/480[3]	80x25	8x16	25.175 MHz
5F/101[9]	Graphics	640x400	640x400/480	640x400/480	80x30	8x16	25.175 MHz

TABLE 7-1 SIMULTANEOUS DISPLAY SCREEN CHARACTERISTICS

NOTES FOR

1. EGA compatible.
2. VGA enhanced mode.
3. For 640x480 panels, 350 and 400 line alphanumeric modes may be vertically expanded to 480 lines.
4. An additional 256Kx4 DRAM is required for frame acceleration when a dual-panel display and CRT are used simultaneously.
5. A 16-bit video memory path is required for 640x400, 256-color mode at the listed VCLK frequency.
6. A palette size of 256K is available for CRTs and color STN displays. Monochrome LCD displays map the 256K palette into 64 shades. Color TFT LCDs with a 9-bit interface map the 256K palette into 27K colors. Color TFT LCDs with a 12-bit interface use a subset of the 256K palette to produce 4K colors. Plasma and Electoluminescent (EL) panels map the 256K palette into 16 shades.

Number of Colors	Panel Refresh Rate[8]	CRT VSYNC Rate	Required Memory[4]	Memory Pages	Buffer Start
16/256K	70 Hz	70 Hz	256Kx8	8	B8000
16/256K	70 Hz	70 Hz	256Kx8	8	B8000
16/256K	70 Hz	70 Hz	256Kx8	8	B8000
16/256K	70 Hz	70 Hz	256Kx8	8	B8000
16/256K	70 Hz	70 Hz	256Kx8	8	B8000
16/256K	70 Hz	70 Hz	256Kx8	8	B8000
4/256K	70 Hz	70 Hz	256Kx8	1	B8000
2/256K	70 Hz	70 Hz	256Kx8	1	B8000
mono	70 Hz	70 Hz	256Kx8	8	B8000
mono	70 Hz	70 Hz	256Kx8	8	B8000
16/256K	70 Hz	70 Hz	256Kx8	8	A0000
16/256K	70 Hz	70 Hz	256Kx8	4	A0000
mono	70 Hz	70 Hz	256Kx8	2	A0000
16/256K	70 Hz	70 Hz	256Kx8	2	A0000
2/256K	60 Hz	60 Hz	256Kx8	1	A0000
16/256K	60 Hz	60 Hz	256Kx8	1	A0000
256/256K	70 Hz	70 Hz	256Kx8	1	A0000
256/256K	70 Hz	70 Hz	256Kx16[5]	1	A0000
256/256K	70 Hz	70 Hz	256Kx16	1	A0000

(IBM, PARADISE, AND VESA SCREEN SIZES)

TABLE 7-1

7. The frequency of selected VCLK source is determined from VCLK0, VCLK, and VCLK2 configurations. Frequencies listed are those needed to generate CRT timing compatible with standard VGA monitors. If higher CRT and panel refresh rates are desired, VCLK frequencies may be increased up to specified maximums.
8. Panel refresh rates are identical to the listed CRT refresh rates when in simultaneous display mode. This is true for dual-panel as well as single-panel construction.
9. The 5Eh and 5Fh modes are supported with single-panel constructed flat panels, and are not supported in simultaneous display when using a dual-panel monochrome LCD due to the 256Kx16 memory requirements.

SCREEN CHARACTERISTICS

Mode # (Hex)	Mode Type	Number of Colors[5]	Mode Native Resolution[3]	Displayed Panel Resolution	Alpha Format
0,1	Alpha	16/256K	320x200	640x400/480	40x25
0,1[1]	Alpha	16/256K	320x350	640x350/480	40x25
0,1[2]	Alpha	16/256K	360x400	640x400/480	40x25
2,3	Alpha	16/256K	640x200	640x400/480	80x25
2,3[1]	Alpha	16/256K	640x350	640x350/480	80x25
2,3[2]	Alpha	16/256K	720x400	640x400/480	80x25
4,5	Graphics	4/256K	320x200	640x400/480	40x25
6	Graphics	2/256K	640x200	640x400/480	80x25
7	Alpha	mono	720x350	640x350/480	80x25
7[1]	Alpha	mono	720x400	640x400/480	80x25
D	Graphics	16/256K	320x200	640x400/480	40x25
E	Graphics	16/256K	320x200	640x400/480	40x25
F	Graphics	mono	640x350	640x350/480	80x25
10	Graphics	16/256K	640x350	640x350/480	80x25
11	Graphics	2/256K	640x480	640x480	80x30
12	Graphics	16/256K	640x480	640x480	80x30
13	Graphics	256/256K	320x200	640x400/480	40x25
5E/100	Graphics	256/256K	640x400	640x400/480	80x25
5F/101	Graphics	256/256K	640x480	640x480	80x30

TABLE 7-2 DISPLAY CHARACTERISTICS FOR FLAT PANEL ONLY

NOTES FOR

1. EGA compatible.
2. VGA enhanced mode.
3. For 640x480 panels, 350 and 400 line alphanumeric and graphics modes may be vertically expanded to 480 lines.
4. 16-bit video memory path is required for 640x400 256-color mode.
5. A palette size of 256K is available for CRTs and color STN displays. Monochrome LCD displays map the 256K palette into 64 shades. Color TFT LCDs with a 9-bit interface map the 256K palette into 27K colors. Color TFT LCDs with a 12-bit interface use a subset of the 256K palette to produce 4K colors. Plasma and Electoluminescent (EL) panels map the 256K palette into 16 shades.

Font Size	Max Panel Refresh Rates - 5V[7]	Max Panel Refresh Rates - 3.3V[8]	Memory Required	Memory Pages	Buffer Start
8x8	125 Hz	100 Hz	256Kx8	8	B8000
8x14	125 Hz	100 Hz	256Kx8	8	B8000
8x16	125 Hz	100 Hz	256Kx8	8	B8000
8x8	125 Hz	100 Hz	256Kx8	8	B8000
8x14	125 Hz	100 Hz	256Kx8	8	B8000
8x16	125 Hz	100 Hz	256Kx8	8	B8000
8x8	125 Hz	100 Hz	256Kx8	1	B8000
8x8	125 Hz	100 Hz	256Kx8	1	B8000
8x14	125 Hz	100 Hz	256Kx8	8	B8000
8x16	125 Hz	100 Hz	256Kx8	8	B8000
8x8	125 Hz	100 Hz	256Kx8	8	A0000
8x8	125 Hz	100 Hz	256Kx8	4	A0000
8x14	125 Hz	100 Hz	256Kx8	2	A0000
8x14	125 Hz	100 Hz	256Kx8	2	A0000
8x16	125 Hz	100 Hz	256Kx8	1	A0000
8x16	125 Hz	100 Hz	256Kx8	1	A0000
8x8	125 Hz	100 Hz	256Kx8	1	A0000
8x16	125 Hz	100 Hz	256Kx16[4]	1	A0000
8x16	125 Hz	100 Hz	256Kx16	1	A0000

(IBM, PARADISE, AND VESA SCREEN SIZES)

TABLE 7-2

6. The frequency of selected VCLK source, determined from VCLK0, VCLK, and VCLK2 configurations. Frequencies listed are those needed to generate CRT timing compatible with standard VGA monitors. If higher CRT and panel refresh rates are desired, VCLK frequencies may be increased up to specified maximums.
7. Range of refresh rates at 5V is based on VCLK frequencies from 13.8 to 45 MHz.
8. Range of refresh rates at 3.3V is based on VCLK frequencies from 13.8 to 36 MHz.

Mode No. (Hex)	Mode Type	Number of Colors	Mode Native Resolution	Displayed CRT Resolution	Alpha Format	Font Size
0,1	Alpha	16/256K	320x200	320x200	40x25	8x8
0,1[1]	Alpha	16/256K	320x350	320x350	40x25	8x14
0,1[2]	Alpha	16/256K	360x400	360x400	40x25	8x16
2,3	Alpha	16/256K	640x200	640x200	80x25	8x8
2,3[1]	Alpha	16/256K	640x350	640x350	80x25	8x14
2,3[2]	Alpha	16/256K	720x400	720x400	80x25	8x16
4,5	Graphics	4/256K	320x200	320x200	40x25	8x8
6	Graphics	2/256K	640x200	640x200	80x25	8x8
7	Alpha	mono	720x350	720x350	80x25	8x14
7[1]	Alpha	mono	720x400	720x400	80x25	8x16
D	Graphics	16/256K	320x200	320x200	40x25	8x8
E	Graphics	16/256K	640x200	640x200	80x25	8x8
F	Graphics	mono	640x350	640x350	80x25	8x14
10	Graphics	16/256K	640x350	640x350	80x25	8x14
11	Graphics	2/256K	640x480	640x480	80x30	8x16
12	Graphics	16/256K	640x480	640x480	80x30	8x16
13	Graphics	256/256K	320x200	320x200	40x25	8x8
21	Alpha	16/256K	1188x396	1188x396	132x44	9x9
41	Alpha	16/256K	720x476	720x476	80x34	9x14
47	Alpha	16/256K	1188x448	1188x448	132x28	9x16
54	Alpha	16/256K	1056x344	1056x344	132x43	9x9
55	Alpha	16/256K	1056x400	1056x400	132x25	8x16
58/6A/102	Graphics	16/256K	800x600	800x600	100x75	8x8
5C	Graphics	256/256K	800x600	800x600	100x75	8x8
5D/104	Graphics	16/256K	1024x768	1024x768	128x48	8x16
5E/100[3]	Graphics	256/256K	640x400	640x400	80x25	8x16
5F/101	Graphics	256/256K	640x480	640x480	80x30	8x16

TABLE 7-3 CRT ONLY DISPLAY

NOTES FOR

1. EGA compatible.
2. VGA enhanced mode.
3. 16-bit video memory path is required for 640x400 256-color mode.

VCLK[4] Frequency	CRT VSYNC Rate	CRT HSYNC Rate	Required Memory[4]	Memory Pages	Buffer Start
25.175MHz	70 Hz	31.5 KHz	256Kx8	8	B8000
25.175 MHz	70 Hz	31.5 KHz	256Kx8	8	B8000
28.322 MHz	70 Hz	31.5 KHz	256Kx8	8	B8000
25.175 MHz	70 Hz	31.5 KHz	256Kx8	8	B8000
25.175 MHz	70 Hz	31.5 KHz	256Kx8	8	B8000
28.322 MHz	70 Hz	31.5 KHz	256Kx8	8	B8000
25.175 MHz	70 Hz	31.5 KHz	256Kx8	1	B8000
25.175 MHz	70 Hz	31.5 KHz	256Kx8	1	B8000
28.322 MHz	70 Hz	31.5 KHz	256Kx8	8	B8000
28.322 MHz	70 Hz	31.5 KHz	256Kx8	8	B8000
25.175 MHz	70 Hz	31.5 KHz	256Kx8	8	A0000
25.175 MHz	70 Hz	31.5 KHz	256Kx8	4	A0000
25.175 MHz	70 Hz	31.5 KHz	256Kx8	2	A0000
25.175 MHz	60 Hz	31.5 KHz	256Kx8	1	A0000
25.175 MHz	60 Hz	31.5 KHz	256Kx8	1	A0000
25.175 MHz	70 Hz	31.5 KHz	256Kx8	1	A0000
44.9 MHz	67.8 Hz	31.06 KHz	256Kx8	2	B8000
28.2 MHz	59.7 Hz	31.34 KHz	256Kx8	8	B8000
44.9 MHz	59.9 Hz	31.45 KHz	256Kx8	2	B8000
44.9 MHz	70 Hz	31.5 KHz	256Kx8	2	B8000
44.9 MHz	69Hz	31.5 KHz	256Kx8	4	B0000
36 MHz	56 Hz	35.1 KHz	256Kx8	1	A0000
36 MHz	56 Hz	35.1 KHz	256Kx16	1	A0000
44.9 MHz	87 Hz int.	35.5 KHz	256Kx16	1	A0000
25.175 MHz	70 Hz	31.5 KHz	256Kx16[3]	1	A0000
25.175 MHz	70 Hz	31.5 KHz	256Kx16	1	A0000

CHARACTERISTICS

TABLE 7-3

4. The frequency of a selected VCLK source is determined from VCLK0, VCLK, and VCLK2 configurations. Frequencies listed are those needed to generate CRT timing compatible with standard VGA monitors. If higher CRT and panel refresh rates are desired, VCLK frequencies may be increased up to the specified maximums.
5. At listed VCLK frequency.

Mode Number	Displayed Resolution	Increased VCLK Frequency	VSYNC Rate	HSYNC Rate
5C	800x600	40 MHz	60 Hz	37.84 KHz
5D/104	1024x768	65 MHz	60 Hz non-int.	45.5 KHz
58/6A/102	800x600	40 MHz	60 Hz	38 KHz
58,6A,102	800x600	50 MHz	72 Hz	47.5 KHz

TABLE 7-4 COMMONLY USED INCREASED REFRESH RATES FOR SUPER VGA MODES CRT ONLY DISPLAY

7.2 ISO COMPLIANT SCEEN REFRESH RATES

The ISO compliant refresh rates are listed in Table 7-5.

MODE NUMBER	DISPLAYED RESOLUTION	INCREASED VCLK FREQUENCY[3]	VSYNC RATE (Hz)	HSYNC RATE (KHz)
0, 1	320x400	31.5 MHz	87.7	39.4
0, 1[1]	320x350	31.5 MHz	87.7	39.4
0, 1[2]	360x 400	31.5 MHz	87.7	39.4
2, 3	640x400	31.5 MHz	87.7	39.4
2, 3[1]	640x350	31.5 MHz	87.7	39.4
2, 3[2]	720x400	35.5 MHz	87.7	39.4
4, 5	320x400	31.5 MHz	87.7	39.4
6	640x400	31.5 MHz	87.7	39.4
7	720x350	35.5 MHz	87.7	39.4
7[2]	720x400	35.5 MHz	87.7	39.4
D	320x400	31.5 MHz	87.7	39.4
E	640x400	31.5 MHz	87.7	39.4
F	640x350	31.5 MHz	87.7	39.4
10	640x350	31.5 MHz	87.7	39.4
11	640x480	31.5 MHz	75.0	39.4
12[4]	640x480	31.5 MHz	75.0	39.4
13	320x400	31.5 MHz	87.7	39.4
5E/100	640x400	31.5 MHz	87.7	39.4
5F/101	640x480	31.5 MHz	87.7	39.4

1. EGA Compatible.
2. VGA Compatible.
3. Typically, the increased VCLK frequency for modes 0 through 13 is selected by setting VSEL3 low on a WD90C63/4.
4. Use mode 12 increased VCLK frequency, VSYNC rate, and HSYNC rates for simultaneous display refresh rate calculations.

TABLE 7-5 ISO COMPLIANT INCREASED REFRESH RATES FOR CRT ONLY

8.0 OPERATING ENVIRONMENT

The following table lists the WD90C26A controller's absolute maximum ratings.

Package temperature range (operating)	0°C to 80°C (Refer to note.)
Storage Temperature	-40°C to 125°C
Absolute Maximum Power Supply Voltage	6.0 Volts
Voltage on all inputs and outputs with respect to V_{SS}	V_{SS} -0.3 to 7 Volts
Maximum Power Dissipation	1 Watt
Electrostatic Discharge	700V Human Body Model
Latch up Threshold	+/- 100 mA
Maximum Input Current	+/– 20 mA
NOTE: The package temperature of 80°C corresponds approximately to a 70°C ambient temperature when the WD90C26A is mounted on FR4 or equivalent PC board material.	

TABLE 8-1 ABSOLUTE MAXIMUM RATINGS

CAUTION

Stresses above those listed in the table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

9.0 DC ELECTRICAL SPECIFICATIONS

9.1 SPECIFICATIONS

This section describes the DC electrical specifications for 5 VDC and 3.3 VDC operation.

- DC Electrical Specification for 5 VDC operation.
- DC Electrical Specification or 3.3 VDC operation.
- Pin capacitances for both 5 VDC and 3.3 VDC.

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9. 2 DC ELECTRICAL SPECIFICATION FOR 5 VDC OPERATION

This subsection contains the following tables:

- Power Supply Voltage for 5 VDC Operation
- Typical Current/Power Consumption for 5 VDC Operation
- DC Input Characteristics for 5 VDC Operation
- DC Output Characteristics for 5 VDC Operation
- I/O Pin Characteristics for 5 VDC Operation

9.2.1 Power Supply Voltage for 5 VDC Operation

The following DC electrical specifications apply to the WD90C26A operating at 5 volts. When a WD90C26A is used in mixed voltage applications, the specifications in this section apply to those pins which are powered by a 5 volt supply. Refer to Figure 6-5 for information on which pins operate at 5 VDC in a mixed voltage environment.

SUPPLY	MIN (VDC)	MAX (VDC)	PINS	COMMENTS
V_{DD}	4.5	5.5	49, 114	Core and Memory Data Interface Power
AV_{DD}	4.5	5.5	76	DAC Power for Internal RAMDAC
BV_{DD}	4.5	5.5	28, 44, 96	Bus Power for System Clock, panel, and CRT sync Interfaces
PV_{DD}	4.5	5.5	8, 132	Power-Down Power for Memory Address Control Interface
RV_{DD}	4.5	5.5	66,	RAMDAC RAM Power for Internal RAMDAC
V_{SS}, AV_{SS}, RV_{SS}	0.0	0.0	18, 32, 50, 67, 70, 86, 103, 123, 142	Grounds

TABLE 9-1 POWER SUPPLY VOLTAGE FOR 5 VDC OPERATION

9.2.2 Typical Current/Power Consumption for 5 VDC Operation

MODE	CRT/PANEL FREQUENCY				
	25 MHZ	28 MHZ	32MHZ	36 MHZ	45MHZ
Display Active, LCD Only	90 mA 450 mW	100 mA 500 mW	110 mA 550 mW	120 mA 600 mW	140 mA 700 mW
Display Active, CRT Only	90 mA 450 mW	100 mA 500 mW	110 mA 550 mW	120 mA 600 mW	140 mA 700 mW
Display Active, Single Panel Simultaneous Display	90 mA 450 mW	100 mA 500 mW	110 mA 550 mW	120 mA 600 mW	140 mA 700 mW
Display Active, Dual Panel Simultaneous Display	90 mA 450 mW	100 mA 500 mW	110 mA 550 mW	120 mA 600 mW	140 mA 700 mW
System Power-Down[1]	1.5 mA 7.5 mW	1.5 mA 7.5 mW	1.5 mA 7.5 mW	1.5 mA 7.5 mW	1.5 mA 7.5 mW
Display Idle	15 mA 75 mW	16 mA 80 mW	18 mA 90 mW	20 mA 100 mW	23 mA 60 mW
General Power-Down with Internal Clock Control	15 mA 75 mW	16 mA 80 mW	18 mA 90 mW	20 mA 100 mW	23 mA 115 mW
General Power-Down with External Clock Control[2]	28 mA 140 mW	31 mA 155 mW	35 mA 175 mW	40 mA 200 mW	44 mA 220 mW

TABLE 9-2 WD90C26A TYPICAL CURRENT/POWER CONSUMPTION FOR 5 VDC OPERATION

NOTES

Conditions: $V_{DD}=AV_{DD}=BV_{DD}=PV_{DD}=RV_{DD}=5.0$ volts. Dual panel monochrome LCD with typical windowed application displayed. VCLK = CRT/Panel frequency (unless otherwise noted). MCLK = 44.3 MHz (unless otherwise noted). System configured with four 256Kx4, 70 ns video memory.

[1]VCLK = MCLK = 0 Hz.

[2]VCLK = 5 MHz, MCLK = 44.3 MHz.

9.2.3 DC Input Pin Characteristics for 5 VDC Operation

Table 9-3 provides the DC input characteristics for the following signals when their respective input pins are powered by 5 VDC:

NOTE

Refer to Figure 6-1 and Table 9-1 for the minimum and maximum voltage values to reference for each signal.

$\overline{\text{PWRDOWN}}$	RESET	$\overline{\text{REFRESH}}$
$\overline{\text{MEMW}}$/S0	$\overline{\text{MEMR}}$/M/$\overline{\text{IO}}$	$\overline{\text{SBHE}}$
BALE/MADE24	$\overline{\text{IOR}}$/$\overline{\text{S1}}$	$\overline{\text{IOW}}$/$\overline{\text{CMD}}$
AEN/3C3D0	VCLK0/VCKIN	MCLK
SA0-SA16	LA17-LA19	LA23/BLW1M

PARAMETER	MIN)	MAX	CONDITIONS
V_{IL}	-0.5V	0.8V	$V_{DDMIN} < V_{DD} < V_{DDMAX}$
V_{IH}	2.0V	V_{DD}+0.6	$V_{DDMIN} < V_{DD} < V_{DDMAX}$
I_{IL}	-10 µA	+10 µA	V_{IN} = 0V to V_{DD}

TABLE 9-3 INPUT PINS - VOLTAGE/CURRENT CHARACTERISTICS FOR 5 VDC OPERATION

9.2.4 DC Output Pin Characteristics for 5 VDC Operation

Table 9-4 provides the DC output pin voltage/current characteristics for the following signals:

NOTE

Refer to Figure 6-1 and Table 9-1 for the minimum and maximum voltage values to reference for each signal.

AMA0-AMA8	EBROM/46E8	PWROFF/WPLT
AOE	FR/BLANK	RPLT/B0
BMA0-BMA8	IRQ/IRQ	UD0-UD3
BOE	LD0-LD3	

PARAMETER	MIN	MAX	CONDITIONS
V_{OL}		0.4V	I_{OL} = 3.0 mA $V_{DDMIN} < V_{DD} < V_{DDMAX}$
V_{OH}	2.4V		I_{OH} = 4.8 mA $V_{DDMIN} < V_{DD} < V_{DDMAX}$
I_{OZ} (Where Applicable)		10 µA	V_{OUT} = 0V to V_{DD}

TABLE 9-4 OUTPUT PINS - VOLTAGE/CURRENT CHARACTERISTICS FOR 5 VDC OPERATION

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TABLE 9-5 OUTPUT PINS - VOLTAGE/CURRENT CHARACTERISTICS FOR 5 VDC OPERATION

Table 9-6 provides the DC output pin voltage/current characteristics for the following signals:

NOTE

Refer to Figure 6-1 and Table 9-1 for the minimum and maximum voltage values to reference for each signal.

ACAS	BWE	PCLK
ARAS	ENDATA	PNLENA
AWE	FP	VSYNC
BCAS	HSYNC	XSCLK
BRAS	LP	

PARAMETER	MIN	MAX	CONDITIONS
V_{OL}		0.4V	I_{OL} = 6.0 mA $V_{DDMIN} < V_{DD} < V_{DDMAX}$
V_{OH}	2.4V		I_{OH} = 6.0 mA $V_{DDMIN} < V_{DD} < V_{DDMAX}$

TABLE 9-6 OUTPUT PINS - VOLTAGE/CURRENT CHARACTERISTICS FOR 5 VDC OPERATION

Table 9-7 provides the DC output pin voltage/current characteristics for the following signals:

NOTE

Refer to Figure 6-1 and Table 9-1 for the minimum and maximum voltage values to reference for each signal.

$\overline{\text{MEMCS16}}$/$\overline{\text{CDDS16}}$ IOCHRDY/$\overline{\text{CDCHRDY}}$ 0WS/CDSFBK

PARAMETER	MIN	MAX	CONDITIONS
V_{OL}		0.4V	I_{OL} = 16.0 mA $V_{DDMIN} < V_{DD} < V_{DDMAX}$
V_{OH}	2.4V		I_{OH} = 8.0 mA $V_{DDMIN} < V_{DD} < V_{DDMAX}$
I_{OZ} (Where Applicable)		10 µA	V_{OUT} = 0V to V_{DD}

TABLE 9-7 OUTPUT PINS - VOLTAGE/CURRENT CHARACTERISTICS FOR 5 VDC OPERATION

9.2.5 DC I/O Pin Characteristics for 5 VDC Operation

Table 9-8 provides the DC input/output pin voltage and current characteristics for the following signals:

NOTE

Refer to Figure 6-1 and Table 9-1 for the minimum and maximum voltage values to reference for each signal.

AMD0-AMD7
BMD0-BMD7
LA20/FMD1
LA21/FMD2
LA22/FMD3
VCLK1/VCSLD/VCSELL
VCLK2/VCSEL/VCSELH

PARAMETER	MIN	MAX	CONDITIONS
V_{IL}	-0.5V	0.8V	$V_{DDMIN} < V_{DD} < V_{DDMAX}$
V_{IH}	2.0V	V_{DD}+0.6	$V_{DDMIN} < V_{DD} < V_{DDMAX}$
V_{OL}		0.4 V	I_{OL} = 3.0 mA $V_{DDMIN} < V_{DD} < V_{DDMAX}$
V_{OH}	2.4V		I_{OH} = 4.8 mA $V_{DDMIN} < V_{DD} < V_{DDMAX}$
I_{OZ} (Where Applicable)		10 µA	V_{OUT} = 0V to V_{DD}

TABLE 9-8 I/O PINS - VOLTAGE/CURRENT CHARACTERISTICS FOR 5 VDC OPERATION

Table 9-9 provides the DC input/output pin voltage and current characteristics for the following signals:

NOTE

Refer to Figure 6-1 and Table 9-1 for the minimum and maximum voltage values to reference for each signal.

SD0-SD15

PARAMETER	MIN	MAX	CONDITIONS
V_{IL}	-0.5V	0.8V	VDDMIN < VDD < VDDMAX
V_{IH}	2.0V	V_{DD}+0.6	VDDMIN < VDD < VDDMAX
V_{OL}		0.4 V	IOL =8.0 mA VDDMIN < VDD < VDDMAX
V_{OH}	2.4V		IOH = 9.8 mA VDDMIN < VDD < VDDMAX
I_{OZ} (Where Applicable)		10 µA	VOUT = 0V to VDD

TABLE 9-9 I/O PINS - VOLTAGE/CURRENT CHARACTERISTICS FOR 5 VDC OPERATION

Table 9-10 provides the DC input/output pin voltage and current characteristics for the following signals:

NOTE

Refer to Figure 6-1 and Table 9-1 for the minimum and maximum voltage values to reference for each signal.

$\overline{IOCS16}/\overline{CDSETUP}$

PARAMETER	MIN	MAX	CONDITIONS
V_{IL}	-0.5V	0.8V	$V_{DDMIN} < V_{DD} < V_{DDMAX}$
V_{IH}	2.0V	V_{DD}+0.6	$V_{DDMIN} < V_{DD} < V_{DDMAX}$
V_{OL}		0.4 V	I_{OL} = 16.0 mA $V_{DDMIN} < V_{DD} < V_{DDMAX}$
V_{OH}	2.4V		I_{OH} = 8.0 mA $V_{DDMIN} < V_{DD} < V_{DDMAX}$
I_{OZ} (Where Applicable)		10 µA	V_{OUT} = 0V to V_{DD}

TABLE 9-10 I/O PINS - VOLTAGE/CURRENT CHARACTERISTICS FOR 5 VDC OPERATION

9. 3 DC ELECTRICAL SPECIFICATION FOR 3.3 VDC OPERATION

The following DC electrical specifications apply to the WD90C26A operating at 3.3 VDC. Refer to the previous section for DC electrical specifications when the WD90C26A is operating at 5 VDC. When a WD90C26A is used in mixed voltage applications, the specifications in this section apply to those pins powered by a 3.3 VDC supply. The DC electrical specifications described in the previous section apply to those pins powered by a 5 VDC supply. Figure 6-1 illustrates the powering of WD90C26A I/O pins.

This section contains the following tables:

- Power Supply Voltage
- Typical Current/Power Consumption
- Maximum Current/Power Consumption
- I/O Pin Voltage/Current Specifications
- Input Capacitance, Input Pins

9.3.1 Power Supply Voltage for 3.3 VDC Operation

SUPPLY	MIN (VDC)	MAX (VDC)	PINS	COMMENTS
V_{DD}	3.0	3.6	49, 114	Core and Memory Data Interface Power
AV_{DD}	3.0	3.6	76	DAC Power for Internal RAMDAC
BV_{DD}	3.0	3.6	28, 44, 96	Bus Power for System Clock, panel, and CRT sync Interfaces
PV_{DD}	3.0	3.6	8, 132	Power-Down Power for Memory Address Control INterface
RV_{DD}	3.0	3.6	66,	RAMDAC RAM Power for Internal RAMDAC
V_{SS}, AV_{SS}, BV_{SS}, PV_{SS}, RV_{SS}	0.0	0.0	18, 32, 50, 67, 70, 86, 103, 123, 142	Grounds

TABLE 9-11 POWER SUPPLY VOLTAGE FOR 3.3 VDC OPERATION

9.3.2 Typical Current and Power Consumption For 3.3 VDC Operation

Table 9-12 lists the typical current and power consumption for operation at 3.3 VDC.

MODE	CRT/PANEL FREQUENCY				
	25 MHZ	28 MHZ	32MHZ	36 MHZ	45MHZ
Display Active, LCD Only	53 mA 175 mW	60 mA 198 mW	65 mA 215 mW	71 mA 234 mW	83 mA 274 mW
Display Active, CRT Only	53 mA 175 mW	60 mA 198 mW	65 mA 215 mW	71 mA 234 mW	83 mA 274 mW
Display Active, Single Panel Simultaneous Display	53 mA 175 mW	60 mA 198 mW	65 mA 215 mW	71 mA 234 mW	83 mA 274 mW
Display Active, Dual Panel Simultaneous Display	53 mA 175 mW	60 mA 198 mW	65 mA 215 mW	71 mA 234 mW	83 mA 274 mW
System Power Down[1]	1.5 mA 5 mW	1.5 mA 5 mW	1.5 mA 5 mW	1.5 mA 5 mW	1.5 mA 5 mW
Display Idle	6 mA 20 mW	6.5 mA 21.5 mW	7 mA 23 mW	8 mA 26 mW	9 mA 30 mW
General Power-Down with Internal Clock Control[2]	9 mA 30 mW	10 mA 33 mW	11 mA 36 mW	12 mA 40 mW	14 mA 46 mW
General Power-Down with External Clock Control[2]	16 mA 53 mW	18 mA 59 mW	20 mA 66 mW	22 mA 73 mW	26 mA 86 mW

NOTES

Conditions: V_{DD}=BV_{DD}=PV_{DD}=RV_{DD}=3.3V, AV_{DD}=5.0V. Typical windowed application displayed. VCLK = CRT/Panel Frequency (unless otherwise noted). MCLK = 44.3 MHz (unless otherwise noted). System configured with 256Kx8 70 nsec video memory.

[1]VCLK = = MCLK = 0 Hz.

[2]VCLK = 5 MHz, MCLK = 45 MHz (unless otherwise noted).

TABLE 9-12 TYPICAL CURRENT/POWER CONSUMPTION FOR 3.3 VDC OPERATION

9.3.3 DC Input Pin Characteristics for 3.3 VDC Operation

Table 9-13 provides the DC input characteristics for the following signals when their respective input pins are powered by 3.3 VDC:

NOTE

Refer to Figure 6-1 and Table 9-11 for the minimum and maximum voltage values to reference for each signal.

$\overline{\text{PWRDOWN}}$	RESET	$\overline{\text{REFRESH}}$
$\overline{\text{MEMW}}$/S0	$\overline{\text{MEMR}}$/M/$\overline{\text{IO}}$	$\overline{\text{SBHE}}$
BALE/MADE24	$\overline{\text{IOR}}$/S1	$\overline{\text{IOW}}$/$\overline{\text{CMD}}$
AEN/3C3D0	VCLK0/VCKIN	MCLK
SA0-SA16		LA17-LA19
LA23/$\overline{\text{BLW1M}}$		

PARAMETER	MIN	MAX	CONDITIONS
V_{IL}	-0.5V	0.8V	$V_{DDMIN} < V_{DD} < V_{DDMAX}$
V_{IH}	2.0V	V_{DD}+0.6	$V_{DDMIN} < V_{DD} < V_{DDMAX}$
I_{IL}	-10 µA	+10 µA	V_{IN} = 0V to V_{DD}

TABLE 9-13 INPUT PINS - VOLTAGE/CURRENT CHARACTERISTICS FOR 3.3 VDC OPERATION

9.3.4 DC Output Pin Characteristics for 3.3 VDC Operation

Table 9-14 provides the DC output pin voltage/current characteristics for the following signals:

NOTE

Refer to Figure 6-1 and Table 9-11 for the minimum and maximum voltage values to reference for each signal.

AMA0-AMA8	EBROM/46E8	PWROFF/WPLT
AOE	FR/BLANK	RPLT/B0
BMA0-BMA8	IRQ/IRQ	UD0-UD3
BOE	LD0-LD3	

PARAMETER	MIN	MAX	CONDITIONS
V_{OL}		0.4V	I_{OL} = 3.0 mA $V_{DDMIN} < V_{DD} < V_{DDMAX}$
V_{OH}	2.4V		I_{OH} = 4.8 mA $V_{DDMIN} < V_{DD} < V_{DDMAX}$
I_{OZ} (Where Applicable)		10 µA	V_{OUT} = 0V to V_{DD}

TABLE 9-14 OUTPUT PINS - VOLTAGE/CURRENT CHARACTERISTICS FOR 3.3 VDC OPERATION

Table 9-15 has been left blank intentionally.:

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TABLE 9-15 OUTPUT PINS - VOLTAGE/CURRENT CHARACTERISTICS FOR 3.3 VDC OPERATION

Table 9-16 provides the DC output pin voltage/current characteristics for the following signals:

NOTE

Refer to Figure 6-1 and Table 9-11 for the minimum and maximum voltage values to reference for each signal.

ACAS	BWE	PCLK
ARAS	ENDATA	PNLENA
AWE	FP	VSYNC
BCAS	HSYNC	XSCLK
BRAS	LP	

PARAMETER	MIN	MAX	CONDITIONS
V_{OL}		0.4V	I_{OL} = 6.0 mA $V_{DDMIN} < V_{DD} < V_{DDMAX}$
V_{OH}	2.4V		I_{OH} = 6.0 mA $V_{DDMIN} < V_{DD} < V_{DDMAX}$

TABLE 9-16 OUTPUT PINS - VOLTAGE/CURRENT CHARACTERISTICS FOR 3.3 VDC OPERATION

Table 9-17 provides the DC output pin voltage/current characteristics for the following signals:

NOTE

Refer to Figure 6-1 and Table 9-11 for the minimum and maximum voltage values to reference for each signal.

$\overline{\text{MEMCS16}}$/$\overline{\text{CDDS16}}$ IOCHRDY/$\overline{\text{CDCHRDY}}$ 0WS/CDSFBK

PARAMETER	MIN	MAX	CONDITIONS
V_{OL}		0.4V	I_{OL} = 16.0 mA $V_{DDMIN} < V_{DD} < V_{DDMAX}$
V_{OH}	2.4V		I_{OH} = 8.0 mA $V_{DDMIN} < V_{DD} < V_{DDMAX}$
I_{OZ} (Where Applicable)		10 µA	V_{OUT} = 0V to V_{DD}

TABLE 9-17 OUTPUT PINS - VOLTAGE/CURRENT CHARACTERISTICS FOR 3.3 VDC OPERATION

9.3.5 DC I/O Pin Characteristics for 3.3 VDC Operation

Table 9-18 provides the DC input/output pin voltage and current characteristics for the following signals:

NOTE

Refer to Figure 6-1 and Table 9-11 for the minimum and maximum voltage values to reference for each signal.

AMD0-AMD7 LA21/FMD2 VCLK1/VCSLD/VCSELL
BMD0-BMD7 LA22/FMD3 VCLK2/VCSEL/VCSELH
LA20/FMD1

PARAMETER	MIN	MAX	CONDITIONS
V_{IL}	-0.5V	0.8V	$V_{DDMIN} < V_{DD} < V_{DDMAX}$
V_{IH}	2.0V	V_{DD}+0.6	$V_{DDMIN} < V_{DD} < V_{DDMAX}$
V_{OL}		0.4V	I_{OL} = 3.0 mA $V_{DDMIN} < V_{DD} < V_{DDMAX}$
V_{OH}	2.4V		I_{OH} = 4.8 mA $V_{DDMIN} < V_{DD} < V_{DDMAX}$
I_{OZ} (Where Applicable)		10 µA	V_{OUT} = 0V to V_{DD}

TABLE 9-18 I/O PINS - VOLTAGE/CURRENT CHARACTERISTICS FOR 3.3 VDC OPERATION

9.3.6 DC I/O Pin Characteristics for 3.3 VDC Operation

Table 9-19 provides the DC input/output pin voltage and current characteristics for the following signals:

NOTE

Refer to Figure 6-1 and Table 9-11 for the minimum and maximum voltage values to reference for each signal.

SD0-SD15

PARAMETER	MIN	MAX	CONDITIONS
V_{IL}	-0.5V	0.8V	VDDMIN < VDD < VDDMAX
V_{IH}	2.0V	V_{DD}+0.6	VDDMIN < VDD < VDDMAX
V_{OL}		0.4V	IOL = 8.0 mA VDDMIN < VDD < VDDMAX
V_{OH}	2.4V		IOH = 9.8 mA VDDMIN < VDD < VDDMAX
I_{OZ} (Where Applicable)		10 µA	VOUT = 0V to VDD

TABLE 9-19 I/O PINS - VOLTAGE/CURRENT CHARACTERISTICS FOR 3.3 VDC OPERATION

Table 9-20 provides the DC input/output pin voltage and current characteristics for the following signals:

NOTE

Refer to Figure 6-1 and Table 9-11 for the minimum and maximum voltage values to reference for each signal.

$\overline{IOCS16}$/CDSETUP

PARAMETER	MIN	MAX	CONDITIONS
V_{IL}	-0.5V	0.8V	$V_{DDMIN} < V_{DD} < V_{DDMAX}$
V_{IH}	2.0V	V_{DD}+0.6	$V_{DDMIN} < V_{DD} < V_{DDMAX}$
V_{OL}		0.4V	I_{OL} = 16.0 mA $V_{DDMIN} < V_{DD} < V_{DDMAX}$
V_{OH}	2.4V		I_{OH} = 8.0 mA $V_{DDMIN} < V_{DD} < V_{DDMAX}$
I_{OZ} (Where Applicable)		10 µA	V_{OUT} = 0V to V_{DD}

TABLE 9-20 I/O PINS - VOLTAGE/CURRENT CHARACTERISTICS FOR 3.3 VDC OPERATION

9.4 PIN CAPACITANCE

Table 9-21 lists the capacitance for all pins with output only signals:

ALL OUTPUT ONLY PINS		
PINS	**MAX**	**CONDITIONS**
C_{OUT}	20 pF	F_C = 1 MHz

TABLE 9-21 CAPACITANCE FOR OUTPUT ONLY PINS

Table 9-22 lists the capacitance for all pins with input only signals:

ALL INPUT ONLY PINS		
PINS	**MAX**	**CONDITIONS**
C_{IN}	7 pF	F_C = 1 MHz

TABLE 9-22 CAPACITANCE FOR INPUT ONLY PINS

Table 9-23 lists the capacitance for all pins that provide both input and output paths for signals:

ALL INPUT/OUTPUT PINS		
PINS	**MAX**	**CONDITIONS**
C_{OUT}	20 pF	F_C = 1 MHz
C_{IN}	7 pF	F_C = 1 MHz

TABLE 9-23 CAPACITANCE FOR INPUT/OUTPUT (I/O) PINS

10.0 INTERNAL DAC SPECIFICATIONS

10.1 INTERNAL DAC SPECIFICATIONS

Table 10-1lists the specifications for the ANARED, ANAGRN, and ANABLU DACs from the internal RAMDAC of the WD90C26A.

PARAMETER	MIN	TYP	MAX	CONDITIONS
DAC Resolution	6 Bits per Output			
Integral Linearity Error			1/2 LSB	Least Squares Fit
Differential Linearity Error			1/2 LSB	Least Squares Fit
White Level Relative to Black	13.3 mA	14.0 mA	14.7 mA	V_{REF} = 1.235V, R_{SET} = 5.9K Ω
Black Level	-20 µA		+20 µA	
Gray Scale Current Range			20 mA	
LSB Size		222 µA		V_{REF} = 1.235V, R_{SET} = 5.9K Ω
Gray Scale Error			5%	
Glitch Energy			50 pJ	
Settling Time			20 ns	100 pF Load
Clock Feed Through			20 pC	
DAC to DAC Matching			5%	
Output Compliance Current Tolerance	-5%		+5%	
Output Compliance Voltage Range	-0.5V		+1.5V	
Voltage Reference (V_{REF}) Range	1.14V	1.235V	1.26V	**NOTE:** *The V_{REF} input must be grounded in order to use the FSADJ/MDET pin as a monitor detect input instead of a reference.
Voltage Reference Input Current (V_{REF}) DACDISA pin*			10 µA	
R_{set} Value, FASDJ Input		5.9K 4.42K		50 Ω Load 37.5 Ω Load
Input Current, $\overline{MDET}$			10 µA	VREF/$\overline{DACDISA}$ tied to 0V.
DAC Power-on Time			70 µs	Measured from RESET high-to-low or $\overline{PWRDOWN}$ low-to-high
DAC Power-off Time			20 µs	Measured from RESET low-to-high or $\overline{PWRDOWN}$ high-to-low

TABLE 10-1 DAC SPECIFICATIONS

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11.0 TIMING CHARACTERISTICS

11.1 TIMING CHARACTERISTICS

This section describes the WD90C26A timing characteristics. It contains the following tables and their corresponding diagrams.

- Clock and External RAMDAC Timing
- Reset Timing
- I/O and Memory Read/Write ISA(AT) Mode Timing
- MicroChannel Mode Bus Timing
- 256K x 4 and 256K x 16 DRAM Timing
- Flat Panel Timing, Panel Only Mode (No CRT)
- Flat Panel Timing, Simultaneous Display Mode
- STN Color LCD Interface Timing
- TFT Color LCD Interface Timing
- External RAMDAC Timing
- CAS before RAS DRAM Refresh Timing
- Power Down Mode CAS before RAS Refresh
- Self-Refresh Timing
- Timing Parameter Measurement Information

No	Symbol/Parameter	Min[4]	Max[4]	Notes
1	VCLK Period[1, 2]	15.4	72[3]	13.8 to 65MHz
2	VCLK High Duty Cycle [1]	40%	60%	% of period
3	VCLK Low Duty Cycle[1]	40%	60%	% of period
4	VCLK, MCLK Clock Rise Time[1]	-	3	0.8 to 2.0V
5	VCLK, MCLK Clock Fall Time[1]	-	3	2.0 to 0.8V
6	VCLK High to PCLK low Delay[1,5]	8	45	max @ 120 pF load
7a	VCLK High to HSYNC active Delay[1]	8	35	
7b	VCLK High to VSYNC active Delay[1]	8	35	
7c	VCLK High to $\overline{\text{BLANK}}$ active Delay[1]	8	30	
7d	VCLK High to UD(3:0, LD(3:0) Delay[1]	8	30	45ns max @120 pF load up to 45 MHz data rate
8	MCLK Period[3,2]	22.6	30.3	(33 to 44.3 MHz)
9	MCLK High Duty Cycle	40%	60%	
10	MCLK Low Duty Cycle	40%	60%	
11	UD(3:0), LD(3:0) setup to PCLK	3		
12	UD(3:0), LD(3:0) hold from PCLK	3		

TABLE 11-1 CLOCK AND EXTERNAL RAMDAC TIMING FOR 5 VDC OPERATION

NOTES

TA = 25°C, at V_{DD} pins = 5.0 VDC.

Timing specifications for 5 VDC operation are measured from a 1.4V switch point unless otherwise noted.

[1]VCLK = Selected VCLK source: VCLK0, VCLK1, VCLK2, or MCLK, or selected frequency applied to VCKIN.

[2]Operational. Clocks may be stopped or slowed down further for power reduction purposes with limited operation.

[3]$VCLK_{max}$ = 65 MHz for 5 VDC operation, CRT only display. $VCLK_{max}$ = 45 MHz for flat panel only operation or for simultaneous display with single-panel type flat panels. $VCLK_{max}$ = 36 MHz for simultaneous display when using a dual panel-type flat panel.

[4]Numbers listed are in nanoseconds unless other units are given.

[5]Maximum delay is the same for PCLK = inverted VCLK or PCLK = VCLK divided by 2.

No	Symbol/Parameter	Min[4]	Max[4]	Notes
1	VCLK Period[1]	27.8	72[3]	13.8 to 36 MHz
2	VCLK High Duty Cycle [1]	40%	60%	% of period
3	VCLK Low Duty Cycle[1]	40%	60%	% of period
4	VCLK, MCLK Clock Rise Time[1]	-	3	1V to BV_{DD}-1V
5	VCLK, MCLK Clock Fall Time[1]	-	3	1V to BV_{DD}-1V
6	VCLK High to PCLK low Delay[1,5]	8	45	max @ 120 pF load
7a	VCLK High to HSYNC active Delay[1]	8	35	
7b	VCLK High to VSYNC active Delay[1]	8	35	
7c	VCLK High to $\overline{\text{BLANK}}$ active Delay[1]	8	30	
7d	VCLK High to UD(3:0, LD(3:0) Delay[1]	8	30	45ns max @120 pF load up to 45 MHz data rate
8	MCLK Period[3,2]	22.6	30.3	(33 to 44.3 MHz)
9	MCLK High Duty Cycle	40%	60%	
10	MCLK Low Duty Cycle	40%	60%	
11	UD(3:0), LD(3:0) setup to PCLK	3		
12	UD(3:0), LD(3:0) hold from PCLK	3		

TABLE 11-2 CLOCK AND EXTERNAL RAMDAC TIMING FOR 3.3 VDC OPERATION

NOTES

TA = 25°C, at V_{DD} pins = 3.3 VDC.

Timing specifications for 3.3 VDC operation are measured from a 1.0V switch point unless otherwise noted.

[1]VCLK = Selected VCLK source: VCLK0, VCLK1, VCLK2, or MCLK, or selected frequency applied to VCKIN.

[2]Operational. Clocks may be stopped or slowed down further for power reduction purposes with limited operation.

[3]VCLK max = 36 MHz for 3.3 VDC operation for CRT only, panel only, or simultaneous display.

[4]Numbers listed are in nanoseconds unless other units are given.

[5]Maximum delay is the same for PCLK = inverted VCLK or PCLK = VCLK divided by 2.

TIMING CHARACTERISTICS

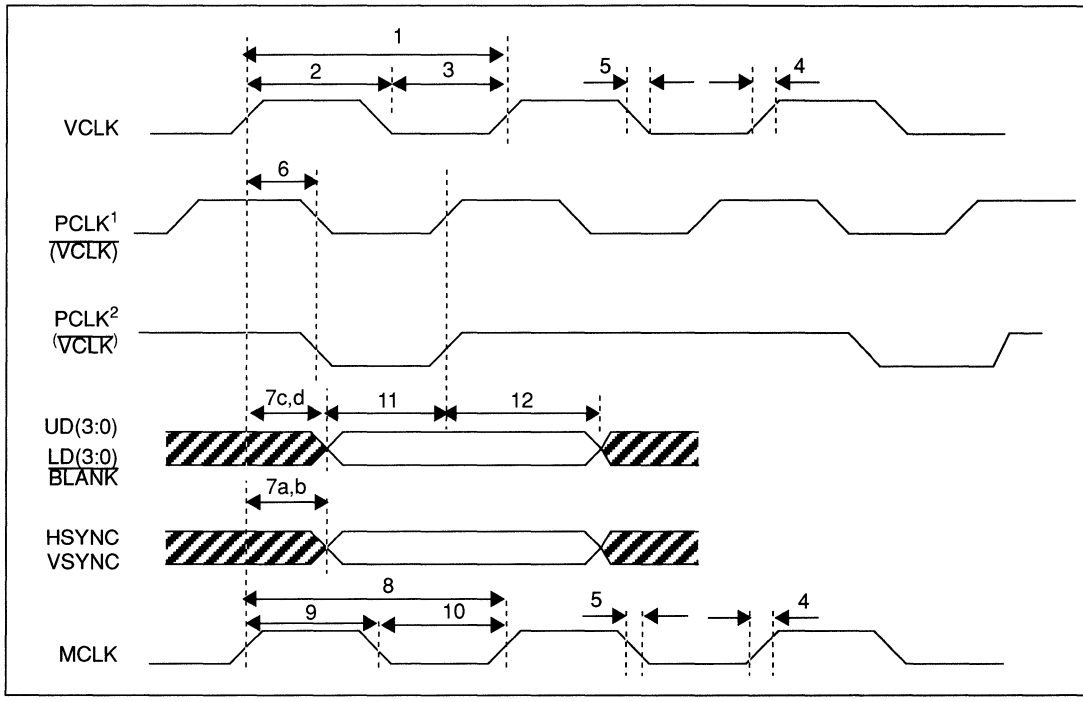


FIGURE 11-1 CLOCK AND EXTERNAL RAMDAC TIMING FOR 5 VDC AND 3.3 VDC OPERATION

NOTES

[1]When PCLK is from the inverted VCLK. PR4 bit 6 and the selected video mode determines whether PCLK = the inverted VCLK or VCLK divided by 2.

[2]When PCLK is from VCLK divided by 2.

No.	Symbol/Parameter	Min[1]	Max[1]	Notes
1	Reset Pulse Width	10T		T = $^{1}/_{MCLK}$
2	AMD(7:0), BMD(7:0) Setup to RESET low		50	For hardware configuration options
3	AMD(7:0), BMD(7:0) Hold from RESET low		30	For hardware configuration options
4	RESET low to first $\overline{IOW}$		10T	
[1]Numbers listed are in nanoseconds unless otherwise noted.				

TABLE 11-3 RESET TIMING FOR 5 VDC AND 3.3 VDC OPERATION

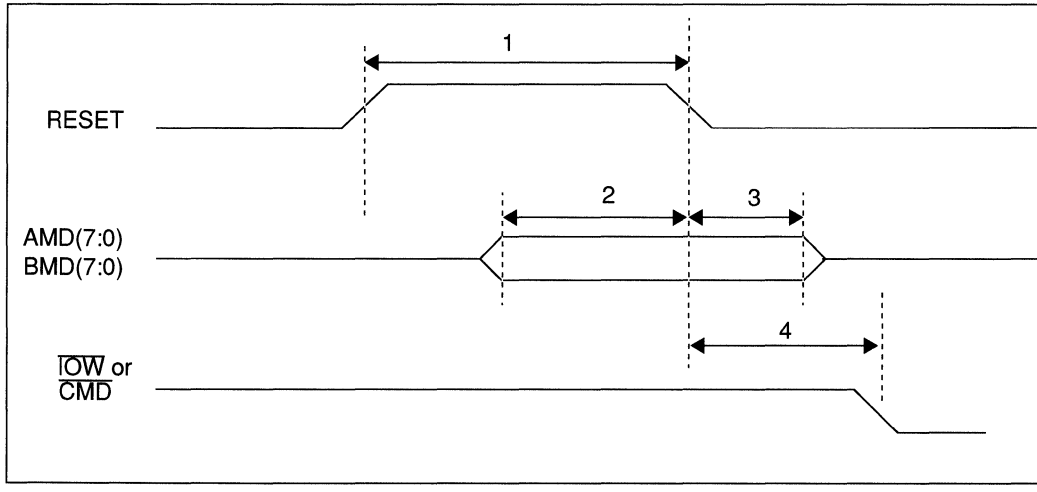


FIGURE 11-2 RESET TIMING

No.	Symbol / Parameter	Min	Max	Notes
1	$\overline{SBHE}$, SA(16:0) setup to $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$, $\overline{MEMW}$ low	20		
2	$\overline{SBHE}$, SA(16:0) hold from $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$,$\overline{MEMW}$ low	15		
3	LA(23:17) setup to BALE low	20		
4	LA(23:17) hold from BALE low	15		
5	$\overline{AEN}$ setup to $\overline{IOR}$ / $\overline{IOW}$ low	20		
6	$\overline{AEN}$ hold from $\overline{IOR}$ / $\overline{IOW}$ high	15		
7	SD(15:0) write data setup before $\overline{IOW}$, $\overline{MEMW}$ high	20		
8	SD(15:0) write data hold from $\overline{IOW}$ high or $\overline{MEMW}$ high	10		
9	SD(15:0) write data hold from $\overline{IOW}$ high	15		
10	SD(15:0) read data valid from $\overline{IOR}$ low		90	
11	$\overline{IOR}$, $\overline{IOW}$, $\overline{MEMW}$, $\overline{MEMR}$ high Cycle Recovery Time	$2t + 15$		$t = {}^{1}/_{MCLK}$ (Note 2)
12	IOCHRDY high from $\overline{MEMR}$ / $\overline{MEMW}$ low	10	2.45 µs	(Note 1)
13	Memory read data valid from IOCHRDY high		40	C_L = 70 pF
14	$\overline{0WS}$, low from $\overline{IOW}$, $\overline{MEMW}$ low		40	C_L= 70 pF
15	$\overline{IOR}$, $\overline{IOW}$, $\overline{MEMW}$, $\overline{MEMR}$ low pulse width	$2t + 15$		$t = {}^{1}/_{MCLK}$ (Note 2)
16	$\overline{0WS}$, tristate after $\overline{IOW}$, $\overline{MEMW}$ high		15	
17	IOCHRDY active from $\overline{MEMW}$ / $\overline{MEMR}$ low	10	30	C_L = 100 pF (Note 3)
18	IOCHRDY tri-state from $\overline{MEMW}$ / $\overline{MEMR}$ high	10	30	C_L = 100 pF (Note 3)
19	$\overline{EBROM}$ low from valid LA(23:17) and SA(16:0)		40	
20	$\overline{EBROM}$ hold from $\overline{MEMR}$ high		40	
21	$\overline{WPLT}$ low from $\overline{IOW}$ low		30	
22	$\overline{RPLT}$ low from $\overline{IOR}$ low		30	
23	$\overline{WPLT}$ high from $\overline{IOW}$ high		30	
24	$\overline{RPLT}$ high from $\overline{IOR}$ high		30	
25	$\overline{VCSLD}$ low from $\overline{IOW}$ low (3C2 port)		40	
26	$\overline{VCSLD}$ high from $\overline{IOW}$ high (3C2 port)		40	
27	SA(16:0) valid to $\overline{IOCS16}$ low		35	C_L = 100 pF
28	$\overline{IOCS16}$ hold from $\overline{IOW}$ high		40	C_L = 100 pF
29	LA(23:17) valid to $\overline{MEMCS16}$		35	C_L = 100 pF
30	$\overline{MEMCS16}$ hold after LA(23:17) is valid to invalid.		20	

TABLE 11-4 I/O AND MEMORY READ / WRITE ISA(AT) MODE TIMING FOR 5 VDC OPERATION

NOTES FOR TABLE 11-4

1. Memory map reads require a 130 nsec delay before data is valid.
2. Maximum value listed is for standard VGA modes. Other values may be used by setting PR31(3C5, index 11) bit 4,3 as follows:

Bit 4	Bit 3	Max IOCHRDY High from $\overline{\text{MEMW}}$, $\overline{\text{MEMR}}$ Low
0	0	40 (default)
0	1	40 + 1*t*
1	0	40 + 2*t*
1	1	40- 1*t*

3. $t = {}^{1}/_{MCLK}$
4. IOCHRDY is a totem-pole high or low output when $\overline{\text{MEMW}}$ is active. Otherwise, IOCHRDY is a tristate (open collector) signal.

No.	Symbol / Parameter	Min	Max	Notes
1	$\overline{SBHE}$, SA(16:0) setup to $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$, $\overline{MEMW}$ low	20		
2	$\overline{SBHE}$, SA(16:0) hold from $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$,$\overline{MEMW}$ low	15		
3	LA(23:17) setup to BALE low	20		
4	LA(23:17) hold from BALE low	15		
5	$\overline{AEN}$ setup to $\overline{IOR}$ / $\overline{IOW}$ low	20		
6	$\overline{AEN}$ hold from $\overline{IOR}$ / $\overline{IOW}$ high	15		
7	SD(15:0) write data setup before $\overline{IOW}$, $\overline{MEMW}$ high	20		
8	SD(15:0) write data hold from $\overline{IOW}$ high or $\overline{MEMW}$ high	10		
9	SD(15:0) write data hold from $\overline{IOW}$ high	15		
10	SD(15:0) read data valid from $\overline{IOR}$ low		90	
11	$\overline{IOR}$, $\overline{IOW}$, $\overline{MEMW}$, $\overline{MEMR}$ high Cycle Recovery Time	$2t + 15$		$t = {}^{1}/_{MCLK}$ (Note 2)
12	IOCHRDY high from $\overline{MEMR}$ / $\overline{MEMW}$ low	10	2.45 µs	(Note 2)
13	Memory read data valid from IOCHRDY high		40	C_L = 70 pF
14	$\overline{0WS}$, low from $\overline{IOW}$, $\overline{MEMW}$ low		40	C_L= 70 pF
15	$\overline{IOR}$, $\overline{IOW}$, $\overline{MEMW}$, $\overline{MEMR}$ low pulse width	$2t$+15		$t = {}^{1}/_{MCLK}$ (Note 2)
16	$\overline{0WS}$, tristate after $\overline{IOW}$, $\overline{MEMW}$ high		40	
17	IOCHRDY active from $\overline{MEMW}$ / $\overline{MEMR}$ low	10	30	C_L=100 pF (Note 3)
18	IOCHRDY tri-state from $\overline{MEMW}$ / $\overline{MEMR}$ high	10	30	C_L=100 pF (Note 3)
19	$\overline{EBROM}$ low from valid LA(23:17) and SA(16:0)		40	
20	$\overline{EBROM}$ hold from $\overline{MEMR}$ high		40	
21	$\overline{WPLT}$ low from $\overline{IOW}$ low		30	
22	$\overline{RPLT}$ low from $\overline{IOR}$ low		30	
23	$\overline{WPLT}$ high from $\overline{IOW}$ high		30	
24	$\overline{RPLT}$ high from $\overline{IOR}$ high		30	
25	$\overline{VCSLD}$ low from $\overline{IOW}$ low (3C2 port)		40	
26	$\overline{VCSLD}$ high from $\overline{IOW}$ high (3C2 port)		40	
27	SA(16:0) valid to $\overline{IOCS16}$ low		35	C_L = 100 pF
28	$\overline{IOCS16}$ hold from $\overline{IOW}$ high		40	C_L = 100 pF
29	LA(23:17) valid to $\overline{MEMCS16}$		35	C_L = 100 pF
30	$\overline{MEMCS16}$ hold after LA(23:17) is valid to invalid.		Next ALE	

TABLE 11-5 I/O AND MEMORY READ / WRITE ISA(AT) MODE TIMING FOR 3.3 VDC OPERATION

NOTES FOR TABLE 11-5

1. Memory map reads require a 136 nsec delay before data is valid.
2. Maximum value listed is for standard VGA modes. Other values may be used by setting PR31(3C5, index 11) bit 4,3 as follows:

Bit 4	Bit 3	Max IOCHRDY High from $\overline{\text{MEMW}}$, $\overline{\text{MEMR}}$ Low
0	0	40 (default)
0	1	40 + 1*t*
1	0	40 + 2*t*
1	1	40- 1*t*

3. $t = {}^{1}/_{\text{MCLK}}$
4. IOCHRDY is a totem-pole high or low output when $\overline{\text{MEMW}}$ is active. Otherwise, IOCHRDY is a tristate (open collector) signal.

TIMING CHARACTERISTICS

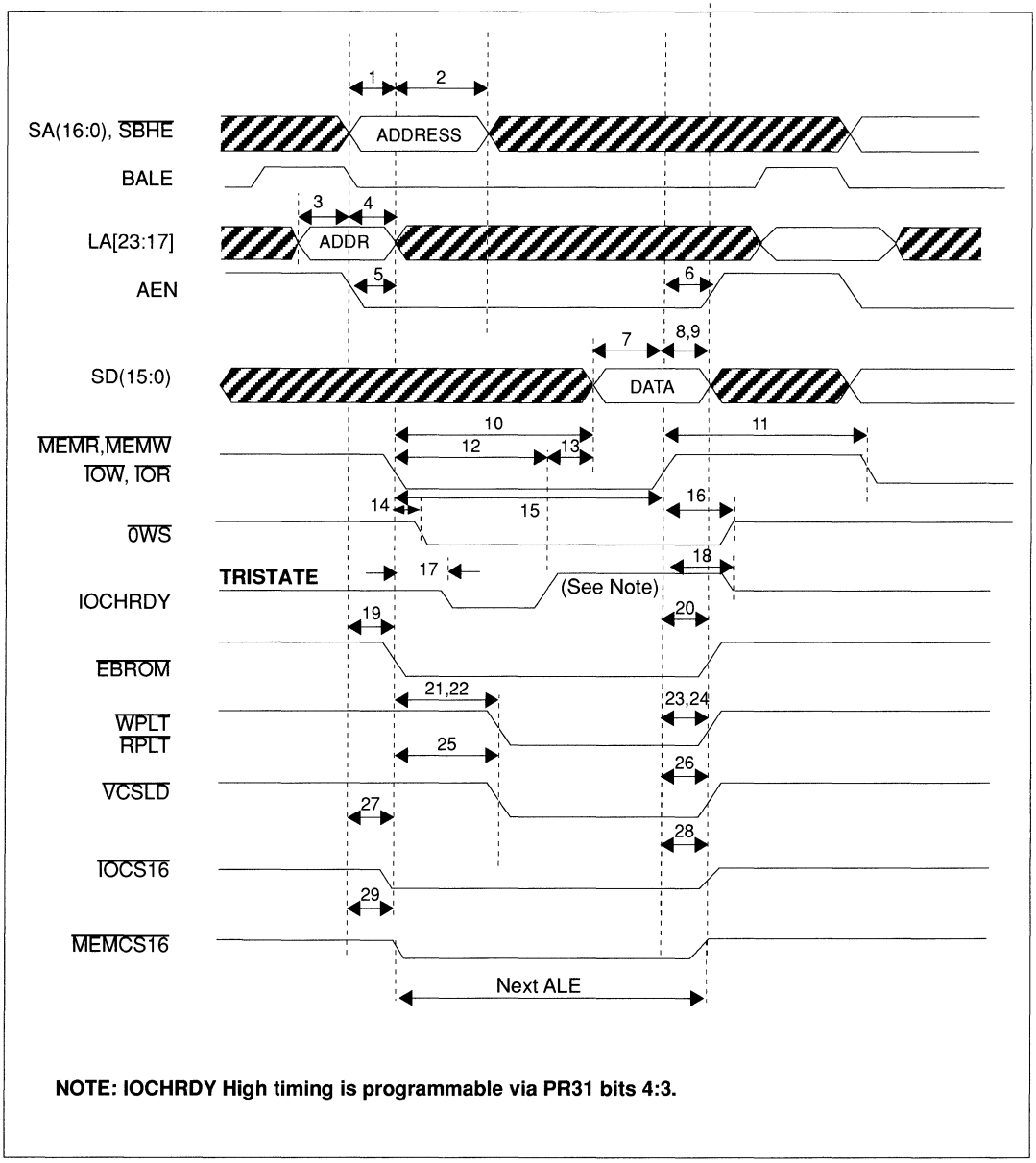


FIGURE 11-3 I/O AND MEMORY READ/WRITE ISA (AT) MODE TIMING FOR 5 VDC AND 3.3 VDC OPERATION

No	Symbol / Parameter	Min.	Max.	Notes
1	LA(23:17), SA(16:0) BLW1M, $\overline{SBHE}$ setup to $\overline{CMD}$ low	20		
2	LA(23:17), SA(16:0) BLW1M, $\overline{SBHE}$ setup to $\overline{CMD}$ low	15		
3	$\overline{CDSETUP}$, setup to $\overline{CMD}$ low	20		
4	$\overline{CDSETUP}$, hold from $\overline{CMD}$ low	15		
5	$\overline{S0}$, $\overline{S1}$, M/$\overline{IO}$ Status setup to $\overline{CMD}$ low	20		
6	$\overline{S0}$, $\overline{S1}$, M/$\overline{IO}$ Status hold from $\overline{CMD}$ low	15		
11	$\overline{CDSFBK}$ delay from valid address / status		40	C_L = 100 pF
12	$\overline{CDSFBK}$ hold from $\overline{CMD}$ high (I/O cycle)		30	C_L = 100 pF
13	$\overline{CDSFBK}$ hold from invalid address (memory cycle)		30	C_L = 100 pF
14	$\overline{CDDS16}$ delay from valid address		40	
15	$\overline{CDDS16}$ hold from invalid address		30	
16	SD(15:0) Write data setup to $\overline{CMD}$ high	20		
17a	SD(15:0) hold after $\overline{CMD}$ high, I/O write cycle	15		
17b	SD(15:0) hold after $\overline{CMD}$ high, mem write cycle	0		
17c	SD(15:0) hold from $\overline{CMD}$ high, I/O read cycle	5	20	
17d	SD(15:0) hold after $\overline{CMD}$ high, memory read cycle			
18	SD(15:0) valid from $\overline{CMD}$ low, I/O read cycle		90	
19	CDCHRDY high delay from $\overline{CMD}$ low, standard cycle	0	2.45 µs	(Note1)
20	SD(15:0) memory read data valid from CDCHRDY high, standard cycle		40	
21a	$\overline{CMD}$ high (inactive)	2t +15		
21b	$\overline{CMD}$ low	2t		
21c	CDCHRDY high delay from $\overline{CMD}$ low, synchronous extended I/O cycle		30	(Note 3)
22	CDHCHRDY low delay from valid address / status, synchronous extended I/O cycle	30		(Note 3)
23	$\overline{EBROM}$ low from valid address	40		
24	$\overline{EBROM}$ high from $\overline{CMD}$ high	30		
25	$\overline{WPLT}$ / $\overline{RPLT}$ low from $\overline{CMD}$ low	30		
26	$\overline{WPLT}$ / $\overline{RPLT}$ high from $\overline{CMD}$ high	30		

TABLE 11-6 MICROCHANNEL MODE BUS TIMING FOR 5 VDC OPERATION

TIMING CHARACTERISTICS

NOTES FOR TABLE 11-6

1. Memory map reads require a 130 nsec delay before data is valid.
2. For memory and standard asynchronous I/O cycles (PR39 bit 4 is set to 0), the maximum value depends on the setting of PR31(3C5, index 11) bits 4:3.

Bit 4	Bit 3	Max CDCHRDY High from Low
0	0	40
0	1	40 + 1*t*
1	0	40 + 2*t*
1	1	40 + 1*t*

3. $t = {}^{1}/_{MCLK}$
4. IOCHRDY is a totem-pole high or low output when $\overline{MEMW}$ is active. Otherwise, IOCHRDY is a tristate (open collector) signal.

No	Symbol / Parameter	Min.	Max.	Notes
1	LA(23:0), $\overline{BLW1M}$, $\overline{SBHE}$ setup to $\overline{CMD}$ low	20		
2	LA(23:0), $\overline{BLW1M}$, $\overline{SBHE}$ hold from $\overline{CMD}$ low	15		
3	$\overline{CDSETUP}$, setup to $\overline{CMD}$ low	20		
4	$\overline{CDSETUP}$, hold from $\overline{CMD}$ low	15		
5	Status setup to $\overline{CMD}$ low	20		
6	Status hold from $\overline{CMD}$ low	15		
11	$\overline{CDSFBK}$ delay from valid address / status		40	C_L = 100 pF
12	$\overline{CDSFBK}$ hold from $\overline{CMD}$ high (I/O cycle)		30	C_L = 100 pF
13	$\overline{CDSFBK}$ hold from invalid address (memory cycle)		30	C_L = 100 pF
14	$\overline{CDDS16}$ delay from valid address		40	
15	$\overline{CDDS16}$ hold from invalid address		30	
16	SD(15:0) Write data setup to $\overline{CMD}$ high	20		
17a	SD(15:0) hold after $\overline{CMD}$ high, I/O write cycle	15		
17b	SD(15:0) hold after $\overline{CMD}$ high, mem write cycle	0		
17c	SD(15:0) hold from $\overline{CMD}$ high, I/O read cycle	5	20	
17d	SD(15:0) hold after $\overline{CMD}$ high, memory read cycle			
18	SD(15:0) valid from $\overline{CMD}$ low, I/O read cycle		90	
19	CDCHRDY high delay from $\overline{CMD}$ low	0	2.45 µs	(Note 1)
20	SD(15:0) memory read data valid from CDHCRDY high		40	
21a	$\overline{CMD}$ high (inactive)	2t +15		
21b	$\overline{CMD}$ low	2t		
21c	CDCHRDY high delay from $\overline{CMD}$ low, synchronous extended I/O cycle		30	(Note 3)
22	CDCHRDY low delay from valid address/status, synchronous extended I/O cycle		30	(Note 2)
23	$\overline{EBROM}$ low from valid address	40		
24	$\overline{EBROM}$ high from $\overline{CMD}$ high	30		
25	$\overline{WPLT}$ / $\overline{RPLT}$ low from $\overline{CMD}$ low	30		
26	$\overline{WPLT}$ / $\overline{RPLT}$ high from $\overline{CMD}$ high	30		

TABLE 11-7 MICROCHANNEL MODE BUS TIMING FOR 3.3 VDC OPERATION

NOTES FOR TABLE 11-7.

1. Memory map reads require a 136 nsec delay before data is valid.
2. For memory and standard asynchronous I/O cycles (PR39 bit 4 is set to 0), the maximum value depends on the setting of PR31(3C5, index 11) bits 4:3.

Bit 4	Bit 3	Max CDCHRDY High from Low
0	0	40
0	1	40 + 1*t*
1	0	40 + 2*t*
1	1	40 + 1*t*

3. $t = {}^{1}/_{MCLK}$
4. IOCHRDY is a totem-pole high or low output when $\overline{MEMW}$ is active. Otherwise, IOCHRDY is a tristate (open collector) signal.

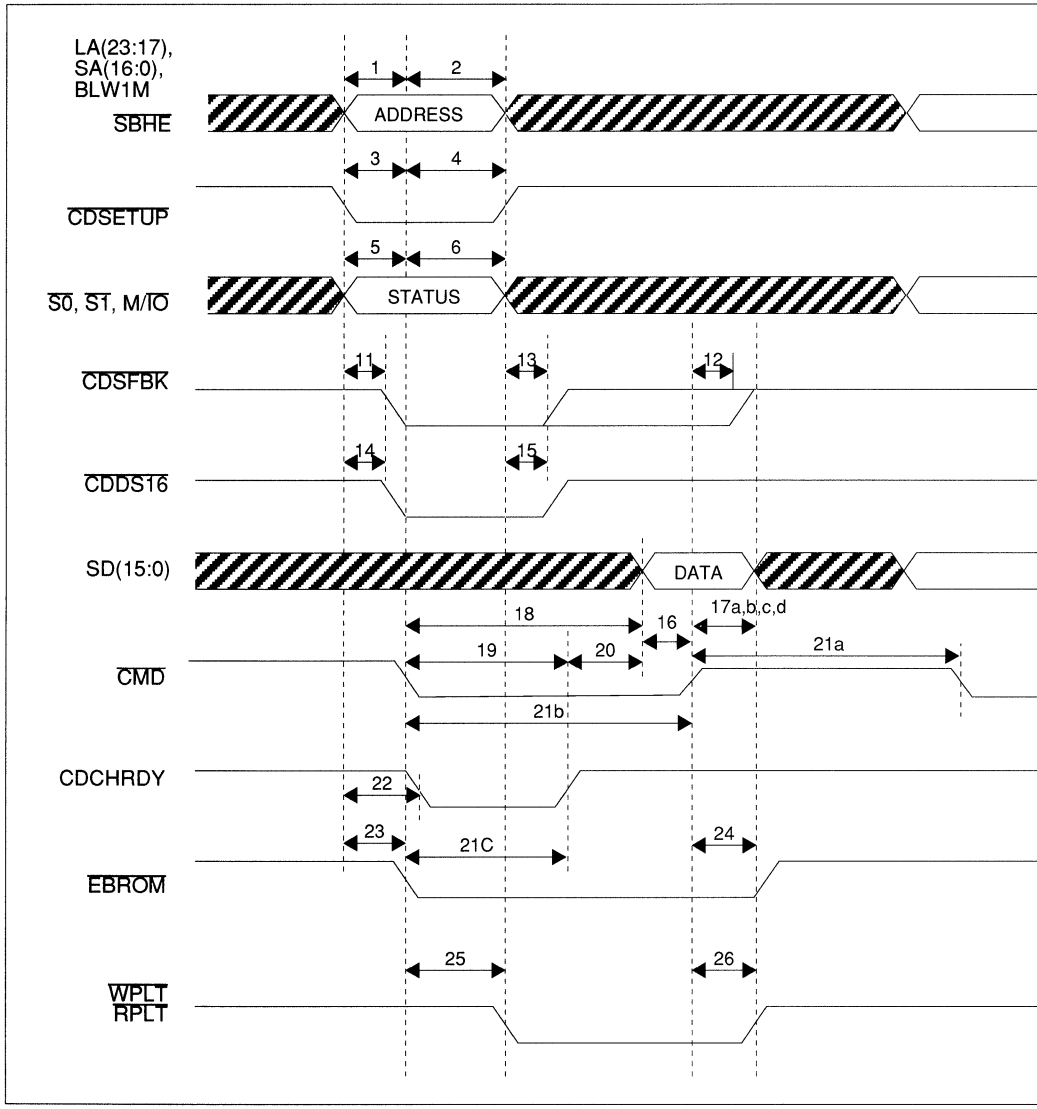


FIGURE 11-4 MICROCHANNEL MODE BUS TIMING

No	Symbol / Parameter	Min.	Max.	Min @ 44.3 MHz	Notes
1	$\overline{ARAS}$, $\overline{BRAS}$ cycle time	6t	456.5t	138	Note 4
2	$\overline{ARAS}$, $\overline{BRAS}$ pulse width low	3.5t-6	454t	74	Note 4
3	$\overline{ARAS}$ high time (precharge)	2.5t+6		63	Note 4
4	$\overline{ARAS}$, $\overline{BRAS}$ low to $\overline{ACAS}$ low, $\overline{BRAS}$ low to $\overline{BCAS}$ low	2.5t-9	2.5t-6	48	Note 4
5	$\overline{ACAS}$, $\overline{BCAS}$ cycle time	2t		46	
6	$\overline{ACAS}$, $\overline{BCAS}$ pulse width low	1t + 6		29	Note 4
7	$\overline{ACAS}$, $\overline{BCAS}$ high time (precharge)	1t - 6	1t+4	17	Note 4
8	Row address setup to $\overline{ARAS}$, $\overline{BRAS}$ low	1t-10	1.5t+10	13	
9	Row address hold time from $\overline{ARAS}$, $\overline{BRAS}$ low	1t-6	1t+12	12	
10	Column address setup to $\overline{ACAS}$, $\overline{BCAS}$ Low	1t-10		13	
11	Column address hold from $\overline{ACAS}$, $\overline{BCAS}$ low	1t		23	
12	Read Data valid before $\overline{ACAS}$, $\overline{BCAS}$ high	3		3	
13	Read data hold after $\overline{ACAS}$, $\overline{BCAS}$ high	0		0	
14	Write Data setup to $\overline{ACAS}$, $\overline{BCAS}$ low	1t-15		8	
15	Write Data hold after $\overline{ACAS}$, $\overline{BCAS}$ low	1t-5		18	
16	$\overline{AWE}$, $\overline{BWE}$ low before $\overline{ACAS}$ low, $\overline{AWE}$, $\overline{BWE}$ low before $\overline{BCAS}$ low setup	1t-5		18	
17	$\overline{AWE}$, $\overline{BWE}$ low after $\overline{ACAS}$ low, $\overline{AWE}$, $\overline{BWE}$ low after $\overline{BCAS}$ low hold	1t-5	10	18	
18	$\overline{AOE}$, $\overline{BOE}$ high before $\overline{AWE}$, $\overline{BWE}$ low, $\overline{BOE}$ high before $\overline{BWE}$ low	2t-10		36	
19	$\overline{AOE}$ low after $\overline{AWE}$ high, $\overline{BOE}$ low after $\overline{BWE}$ high	1t-10		13	
20	$\overline{ACAS}$, $\overline{BCAS}$ high for CAS before RAS refresh	1t		23	
21	$\overline{ARAS}$, $\overline{BRAS}$ low from $\overline{ACAS}$ low, $\overline{BRAS}$ low from $\overline{BCAS}$ low for $\overline{ACAS}$, $\overline{BCAS}$ before $\overline{RAS}$ refresh	1.5t		35	

TABLE 11-8 256K x 4 AND 256K x 16 DRAM TIMING FOR 5 VDC OPERATION

NOTES FOR TABLE 11-8

[1]All times listed are in nanoseconds.

[2]MCLK edge to respective $\overline{RAS}$, $\overline{CAS}$, MA(8:0) edge delay may be up to 40 ns

[3]The timing is the result of setting PR_33(3C5, Index = 13) = XXX00000

[4]Timings are adjustable by PR_33.

[5]Memory write uses fast page early write, while keeping $\overline{OE}$ = 1

[6]Memory read uses fast page read, while keeping $\overline{OE}$ = 1

[7]$T = {}^{1}/_{MCLK}$

[8]MCLK = 37.5MHz for 80 ns DRAM. MCLK = 40 MHZ for some faster 80ns DRAM. MCLK = 44.3 MHZ for 70ns DRAM.

No	Symbol / Parameter	Min.	Max.	Min @ 44.3 MHz	Notes
1	$\overline{ARAS}$, $\overline{BRAS}$ cycle time	6t	456.5t	138	Note 4
2	$\overline{ARAS}$, $\overline{BRAS}$ pulse width low	3.5t-6	454t	74	Note 4
3	$\overline{ARAS}$ high time (precharge)	2.5t+6		63	Note 4
4	$\overline{ARAS}$, low to $\overline{ACAS}$ low, $\overline{BRAS}$ low to $\overline{BCAS}$ low	2.5t-9	2.5t-6	48	Note 4
5	$\overline{ACAS}$, $\overline{BCAS}$ cycle time	2t		46	
6	$\overline{ACAS}$, $\overline{BCAS}$ pulse width low	1t + 6		29	Note 4
7	$\overline{ACAS}$, $\overline{BCAS}$ high time (precharge)	1t - 6	1t+4	17	Note 4
8	Row address setup to $\overline{ARAS}$, $\overline{BRAS}$ low	1t-10	1.5t+10	13	
9	Row address hold time from $\overline{ARAS}$, $\overline{BRAS}$ low	1t-6	1t+12	12	
10	Column address setup to $\overline{ACAS}$, $\overline{BCAS}$ Low	1t-10		13	
11	Column address hold from $\overline{ACAS}$, $\overline{BCAS}$ low	1t		23	
12	Read Data valid before $\overline{ACAS}$, $\overline{BCAS}$ high	3		3	
13	Read data hold after $\overline{ACAS}$, $\overline{BCAS}$ high	0		0	
14	Write Data setup to $\overline{ACAS}$, $\overline{BCAS}$ low	1t-15		8	
15	Write Data hold after $\overline{ACAS}$, $\overline{BCAS}$ low	1t-5		18	
16	$\overline{AWE}$, $\overline{BWE}$ low before $\overline{ACAS}$ low, $\overline{AWE}$, $\overline{BWE}$ low before $\overline{BCAS}$ low setup	1t-5		18	
17	$\overline{AWE}$, $\overline{BWE}$ low after $\overline{ACAS}$ low, $\overline{AWE}$, $\overline{BWE}$ low after $\overline{BCAS}$ low hold	1t-5	10	18	
18	$\overline{AOE}$, $\overline{BOE}$ high before $\overline{AWE}$, $\overline{BWE}$ low, $\overline{BOE}$ high before $\overline{BWE}$ low	2t-10		36	
19	$\overline{AOE}$ low after $\overline{AWE}$ high, $\overline{BOE}$ low after $\overline{BWE}$ high	1t-10		13	
20	$\overline{ACAS}$, $\overline{BCAS}$ high for CAS before RAS refresh	1t		23	
21	$\overline{ARAS}$, $\overline{BRAS}$ low from $\overline{ACAS}$ low, $\overline{BRAS}$ low from $\overline{BCAS}$ low for $\overline{ACAS}$, $\overline{BCAS}$ before $\overline{RAS}$ refresh	1.5t		35	

TABLE 11-9 256K x 4 AND 256K x 16 DRAM TIMING FOR 3.3 VDC OPERATION

NOTES FOR TABLE 11-9

[1]All times listed are in nanoseconds.

[2]MCLK edge to respective $\overline{RAS}$, $\overline{CAS}$, MA(8:0) edge delay may be up to 40 ns

[3]The timing is the result of setting PR_33(3C5, Index = 13) = XXX00000

[4]Timings are adjustable by PR_33.

[5]Memory write uses fast page early write, while keeping $\overline{OE}$ = 1

[6]Memory read uses fast page read, while keeping $\overline{OE}$ = 1

[7]$T = {}^{1}/_{MCLK}$

[8]MCLK = 37.5MHz for 80 ns DRAM. MCLK = 40 MHZ for some faster 80ns DRAM. MCLK = 44.3 MHZ for 70ns DRAM.

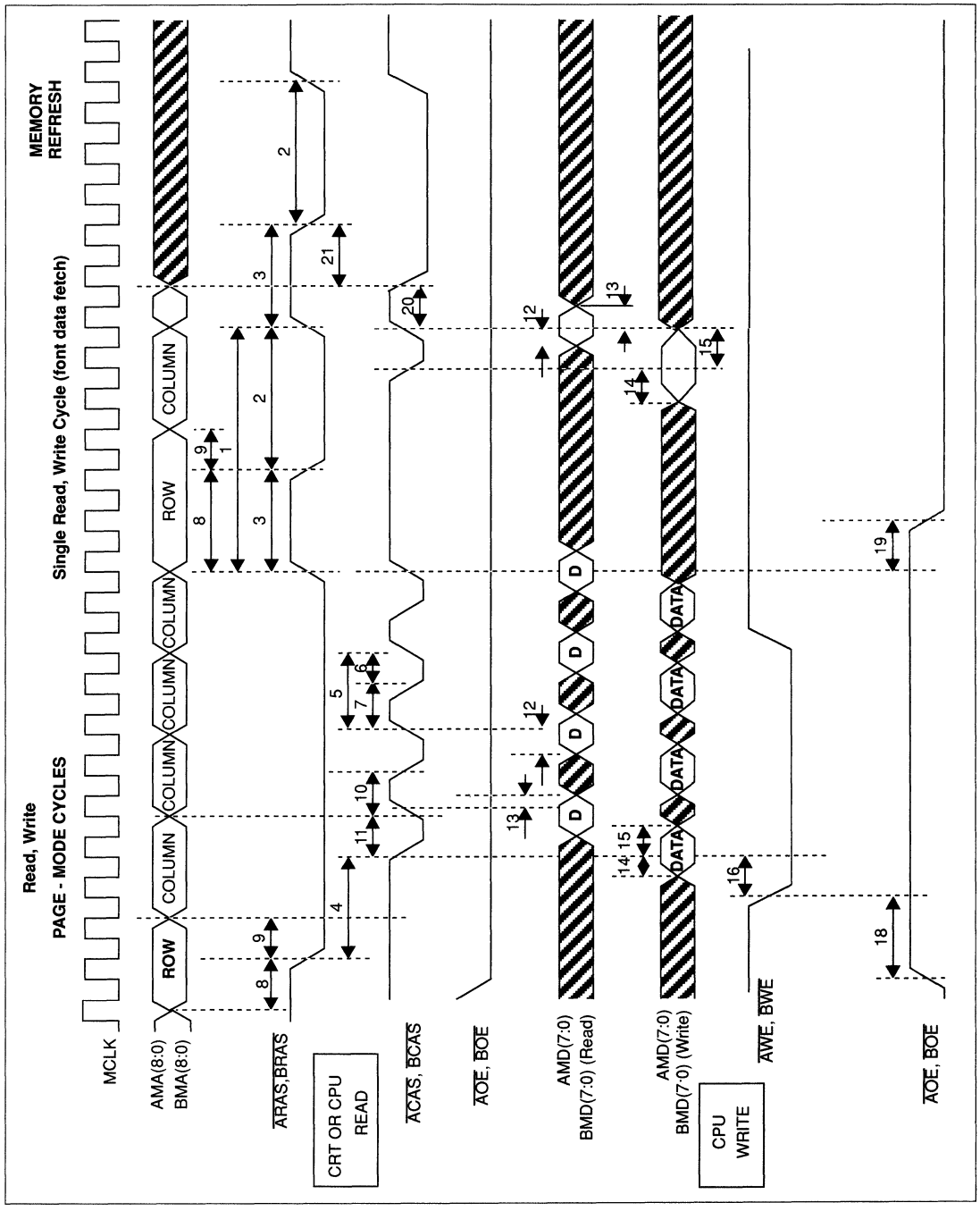


FIGURE 11-5 256K x 4 AND 256K x 16 DRAM TIMING

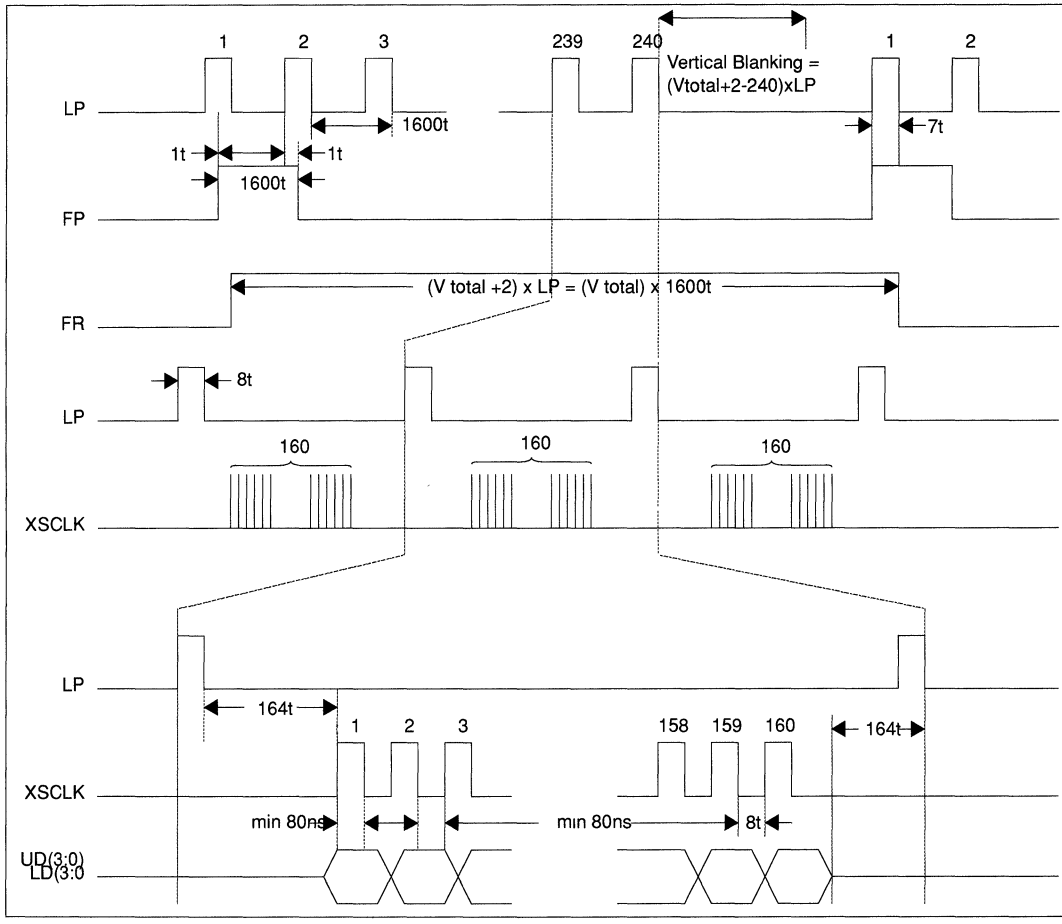


FIGURE 11-6 DUAL-PANEL MONO LCD FUNCTIONAL TIMING, PANEL ONLY MODE (NO CRT)

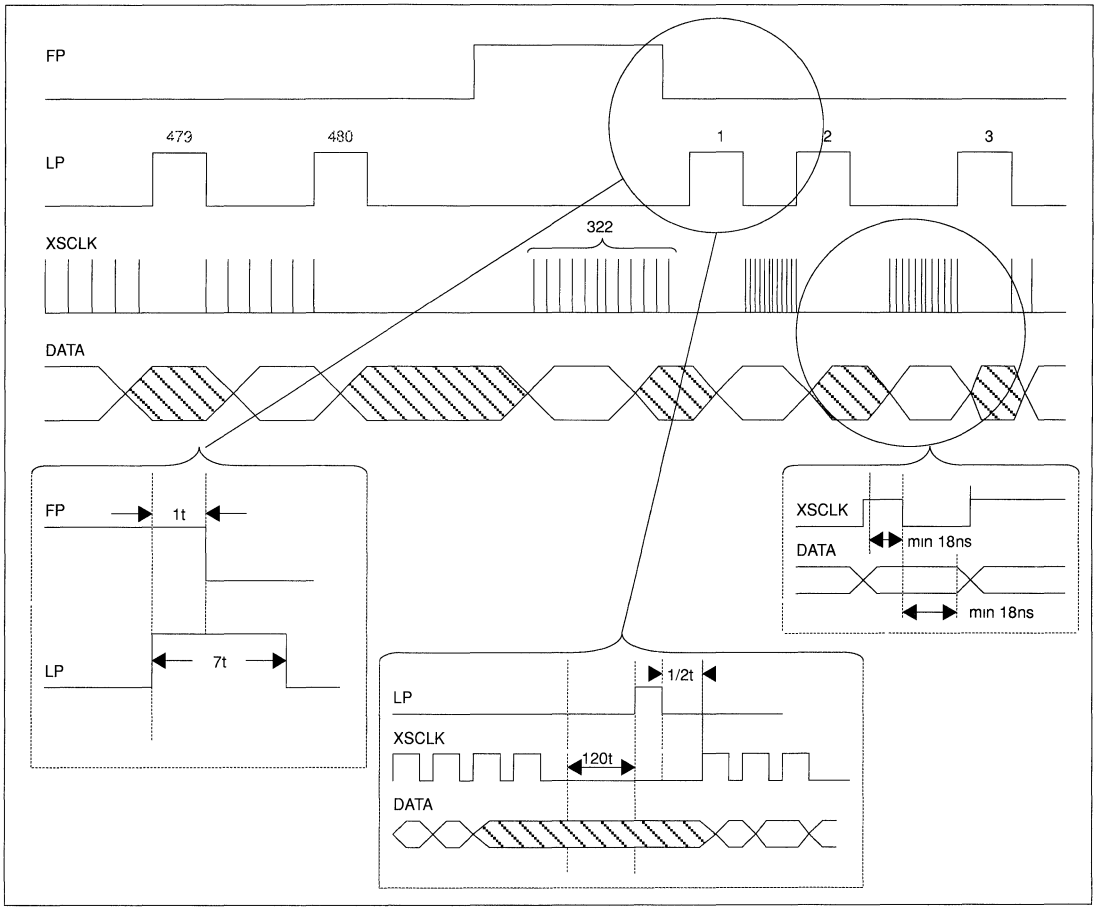
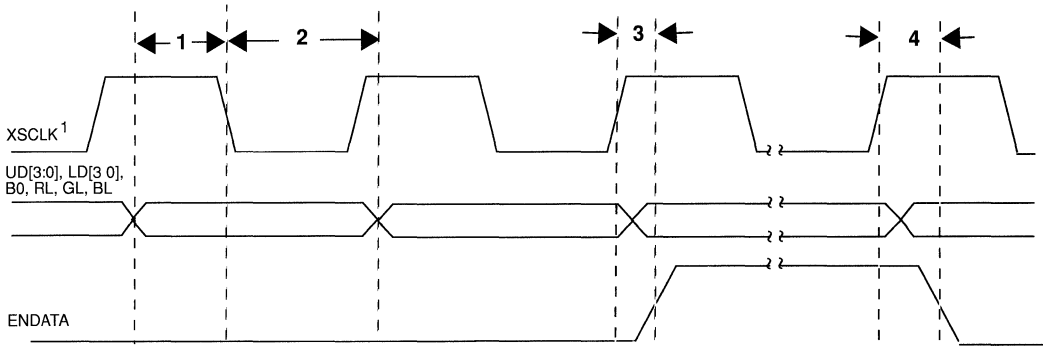


FIGURE 11-7 STN COLOR LCD INTERFACE FUNCTIONAL TIMING

TIMING CHARACTERISTICS



ITEM NO.	DESCRIPTION	MIN.	TYPICAL[2]	MAX.
1	Panel data setup time before the fall of XSCLK		15 ns	
2	Panel data hold time after fall of XSCLK.		21 ns	
3	Rising edge of XSCLK to ENDATA active high		16 ns	
4	Rising edge of XSCLK to ENDATA low.		18 ns	

NOTES:
1. The XSCLK signal is set for normal polarity.
2. Values shown are for VCLK = 28 MHz.

FIGURE 11-8 TFT PANEL AC TIMING

TIMING CHARACTERISTICS

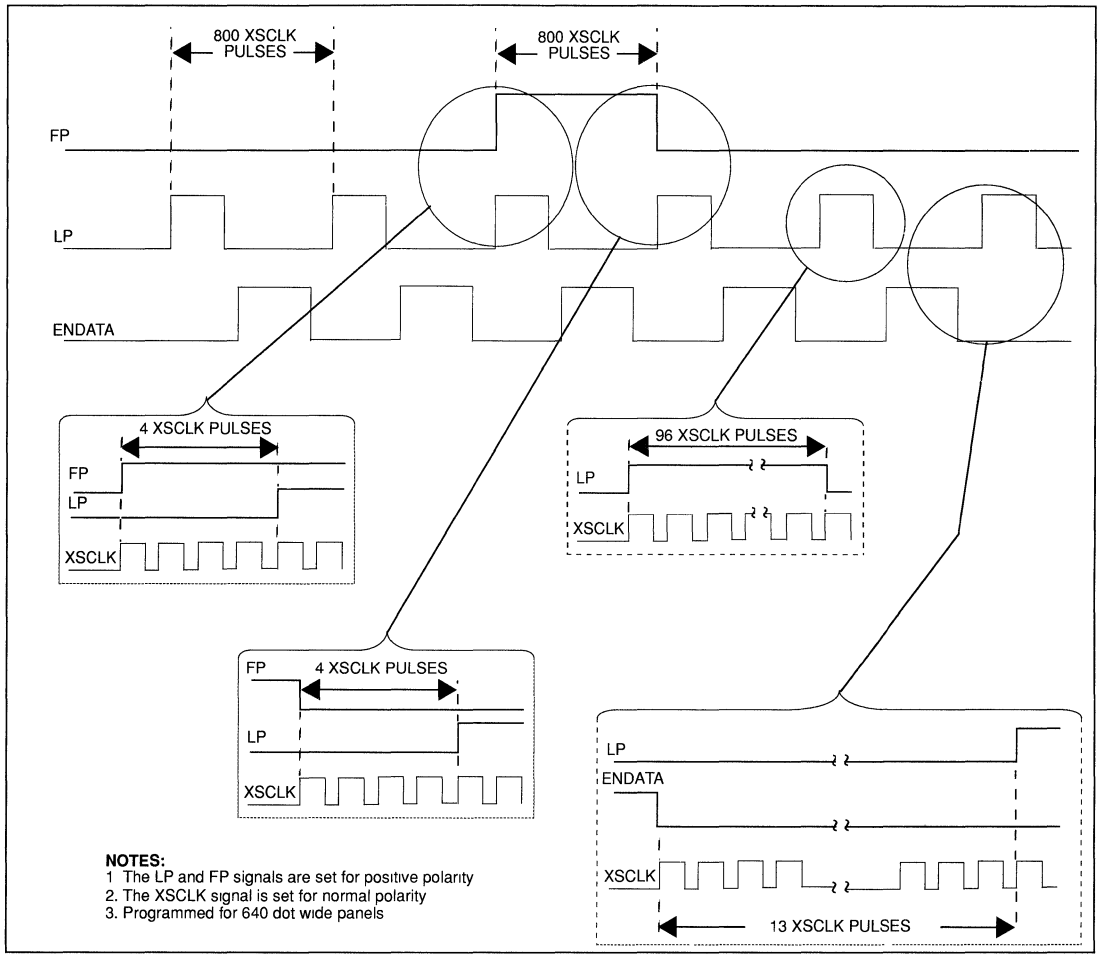


FIGURE 11-9 TFT PANEL FUNCTIONAL TIMING

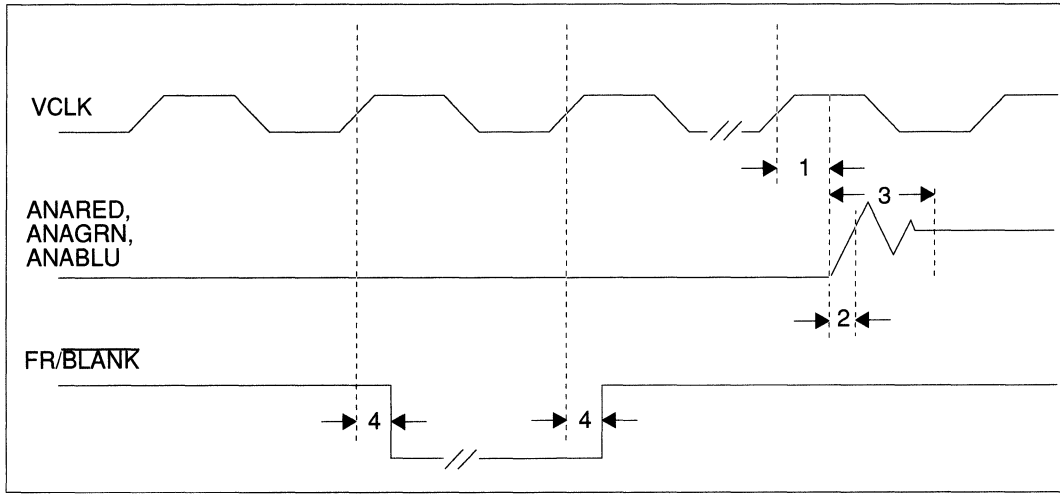


FIGURE 11-10 RAMDAC TIMING

NO.	PARAMETER	MIN.	TYP.	MAX.	UNITS
1	Analog Output Delay			25	ns
2	Analog Output Rise/Fall Time[1]		3		ns
3	Analog Output Settling Time[2]		20		ns
4	Blanking Delay Time from $\overline{\text{BLANK}}$			45	ns

NOTES:

1. Defined as 10% to 90% of final value.
2. Defined as the time from when the DAC output begins to change until the time overshoot/undershoot falls below clock feedthrough.

TABLE 11-10 RAMDAC TIMING

NO	CAS BEFORE RAS DRAM REFRESH TIMING	MIN	MAX
1A 1B	$\overline{ARAS}$,$\overline{BRAS}$, pulse width low $\overline{ARAS}$,$\overline{BRAS}$ pulse width high	5t-10 5t-10	5t+10 5t+10
2A 2B	$\overline{ACAS}$,$\overline{BCAS}$ pulse width low $\overline{ACAS}$,$\overline{BCAS}$ pulse width high	4t-5 6t-5	45+5 6t+5
3	$\overline{ACAS}$,$\overline{BCAS}$ low to $\overline{ARAS}$,$\overline{BCAS}$ low	2t-10	2t+10
4	$\overline{ARAS}$,$\overline{BRAS}$ low to $\overline{ACAS}$,$\overline{BCAS}$ hi	2t-10	2t+10
5	$\overline{AOE}$,$\overline{BOE}$ hi to $\overline{ARAS}$,$\overline{BRAS}$ hi	4t-8	5t+8
6	$\overline{ARAS}$,$\overline{BRAS}$ low to $\overline{AOE}$,$\overline{BOE}$ low	30t	
7	$\overline{ARAS}$,$\overline{BRAS}$ high (precharge) to $\overline{ACAS}$,$\overline{BCAS}$ low	3t-5	3t+20

TABLE 11-11 CAS BEFORE RAS DRAM REFRESH TIMING

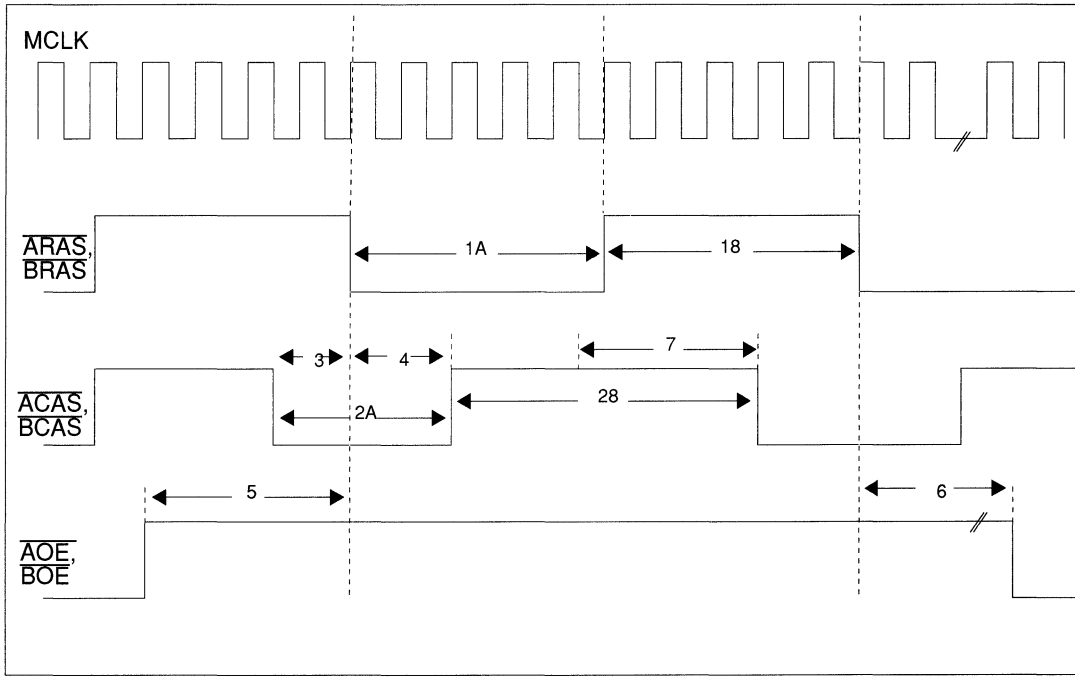


FIGURE 11-11 CAS BEFORE RAS DRAM REFRESH TIMING, NORMAL OPERATION AND POWER DOWN MODES

TIMING CHARACTERISTICS

NO	POWER DOWN MODE CAS BEFORE RAS DRAM REFRESH TIMING	MIN	MAX
1	CAS Low from REFRESH	20	
2	RAS Low from CAS Low	30	
3	CAS High from REFRESH	20	
4	RAS High from CAS High	30	

TABLE 11-12 DISPLAY IDLE/SLEEP MODE AC-TIMED CAS BEFORE RAS REFRESH TIMING

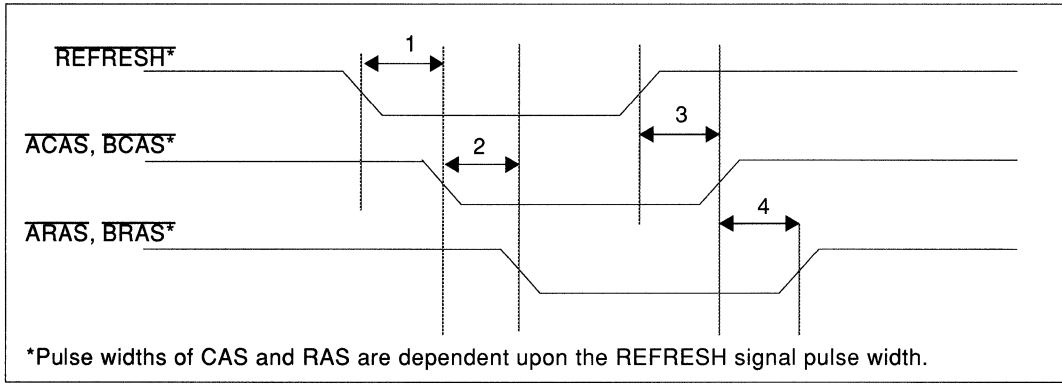
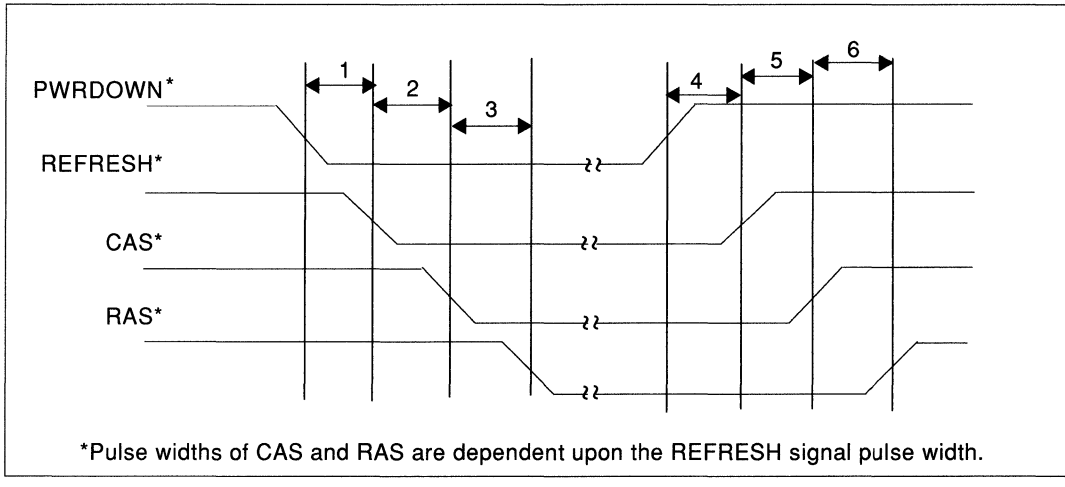


FIGURE 11-12 DISPLAY IDLE/SLEEP MODE AC-TIMED CAS BEFORE RAS REFRESH TIMING

NO	SELF- REFRESH TIMING	MIN	MAX
1	REFRESH Low from PWRDOWN Low	20	
2	CAS Low from REFRESH	20	
3	RAS Low from CAS Low	30	
4	REFRESH High from PWRDOWN High	20	
5	CAS High from REFRESH	20	
6	RAS High from CAS High	30	

TABLE 11-13 SELF-REFRESH TIMING, SLEEP/DISPLAY IDLE MODES



*Pulse widths of CAS and RAS are dependent upon the REFRESH signal pulse width.

FIGURE 11-13 SELF-REFRESH TIMING, SLEEP/DISPLAY IDLE MODES

11.2 TIMING PARAMETER MEASUREMENT INFORMATION

Figure 11-13 shows the test setup for timing parameter measurements and Table 11-14 lists the timing parameter measurement information.

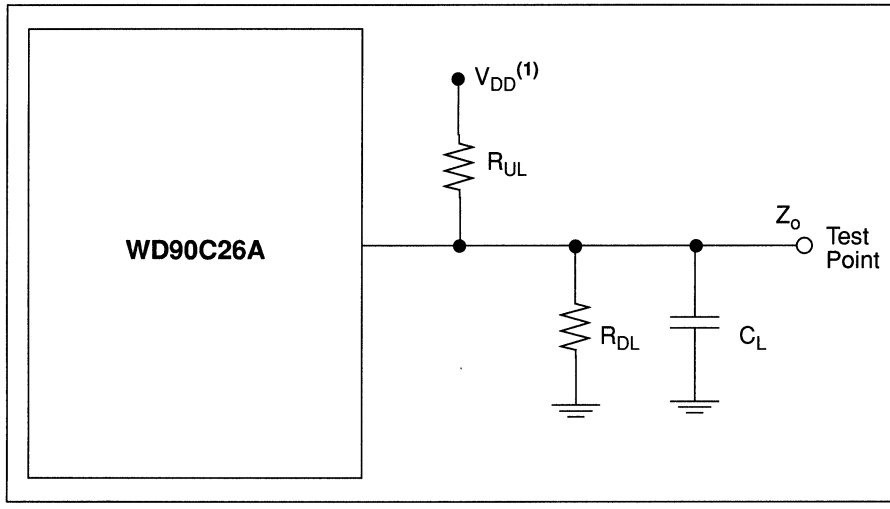


FIGURE 11-14 SETUP FOR TIMING PARAMETER MEASUREMENTS

NOTE

[1]V_{DD} = The supply voltage for the particular output signal.

SIGNAL NAME	C_L[1]	R_{UL}	R_{DL}	NOTES
$\overline{\text{EBROM}}$	50 pF			
$\overline{\text{IOCS16}}$/$\overline{\text{CDSETUP}}$	70 pF	300 Ω		
$\overline{\text{MEMCS16}}$/$\overline{\text{CDDS16}}$	70 pF	300 Ω		
IRQ/$\overline{\text{IRQ}}$	70 pF	1K Ω[2]	1K Ω[3]	Notes 2 & 3
IOCHRDY/CDCHRDY	100 pF	1K Ω		
$\overline{\text{0WS}}$/$\overline{\text{CDSFBK}}$	70 pF	300 Ω		
SD(15:0)	70 pF			
LA22/RL	50 pF			
LA21/GL	50 pF			
LA20/BL	50 pF			
$\overline{\text{ARAS}}$, $\overline{\text{ACAS}}$, $\overline{\text{AOE}}$, $\overline{\text{AWE}}$, $\overline{\text{BRAS}}$, $\overline{\text{BCAS}}$, $\overline{\text{BOE}}$, $\overline{\text{BWE}}$	70 pF			
AMA(8:0)	70 pF			
BMA(8:0)	70 pF			
AMD(7:0)	70 pF			
BMD(7:0	70 pF			
ANARED, ANAGRN, ANABLU	40 pF		37.5 Ω	Z_0=75Ω @65 MHz
$\overline{\text{RPLT}}$/B0	50 pF			
HSYNC, VSYNC	70 pF			
VCLK1/VCSLD/VCSELL	50 pF			Note 3
VCLK2/VCSEL/VCSELL	50 pF			
$\overline{\text{PNLENA}}$	50 pF			
PNLOFF/$\overline{\text{WPLT}}$	50 pF			
PCLK	30 pF			
FR/$\overline{\text{BLANK}}$	50 pF			
UD(3:0), LD(3:0)	50 pF			
XSCLK	50 pF			
ENDATA	50 pF			
FP, LP	50 pF			
VREF/$\overline{\text{DACDISA}}$		4.32		

NOTES:

1. The values listed for C_L were used for the AC timing specified in this data sheet, unless otherwise indicated in the specific timing diagram.
2. VDD = The supply voltage for the particular output signal. Figure 11-14 shows the setup for timing parameter measurements.
3. MicroChannel Mode only.
4. ISA Bus Mode only.

TABLE 11-14 TIMING PARAMETER MEASUREMENT INFORMATION

12.0 PACKAGE DIMENSIONS

12.1 MECHANICAL DRAWINGS

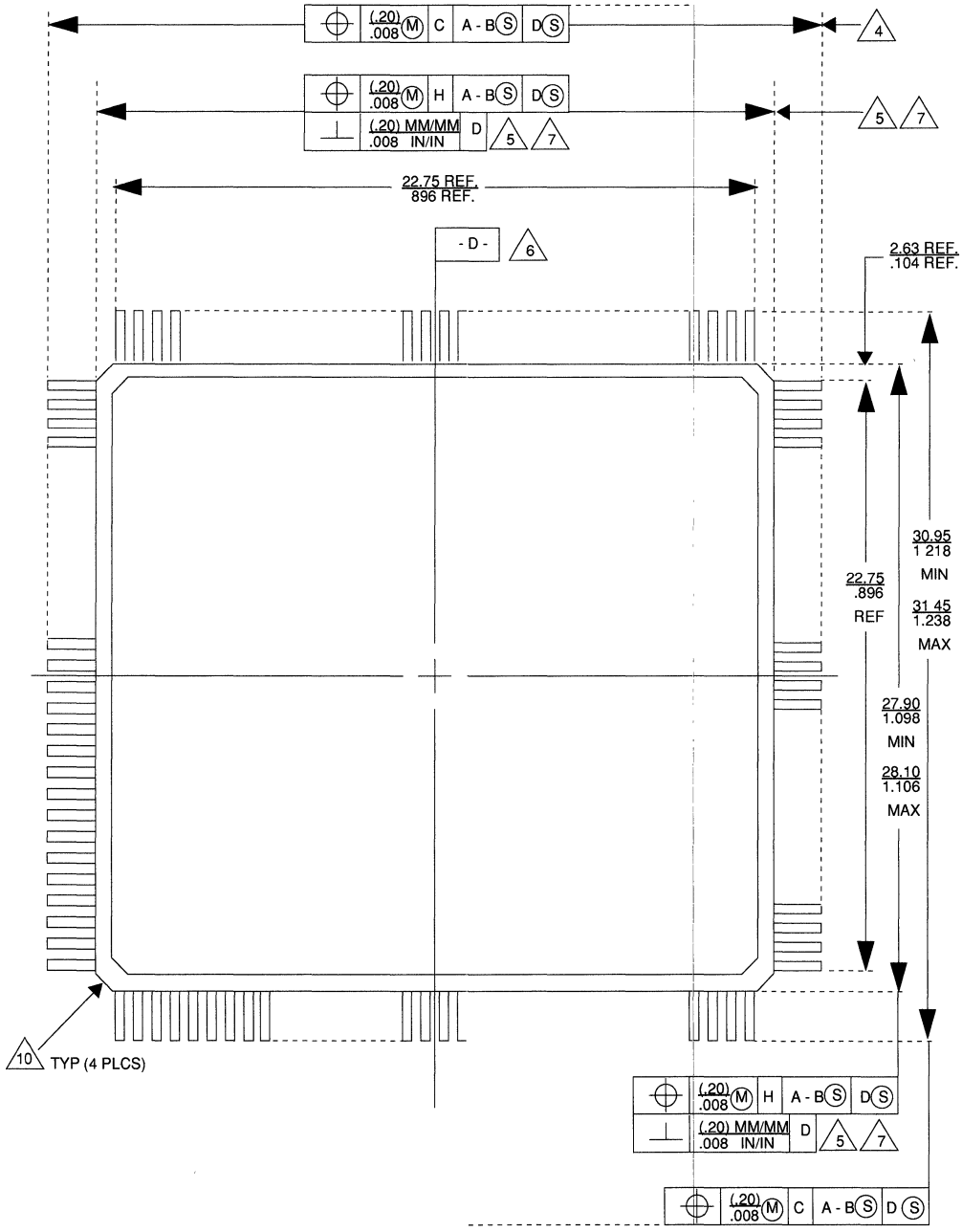
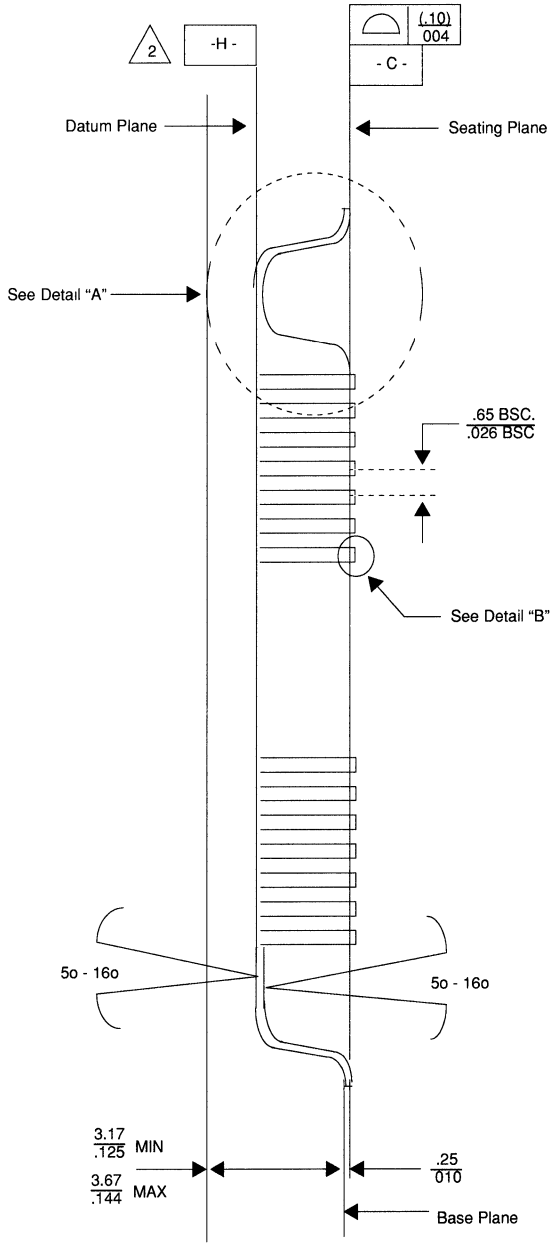
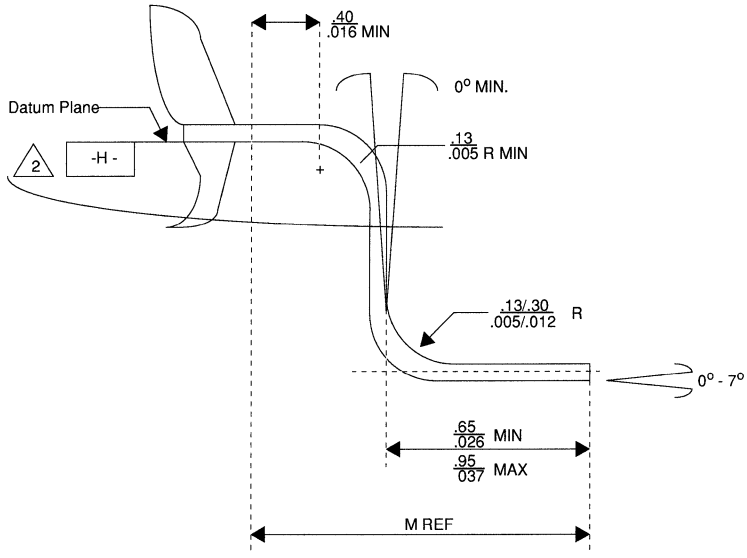
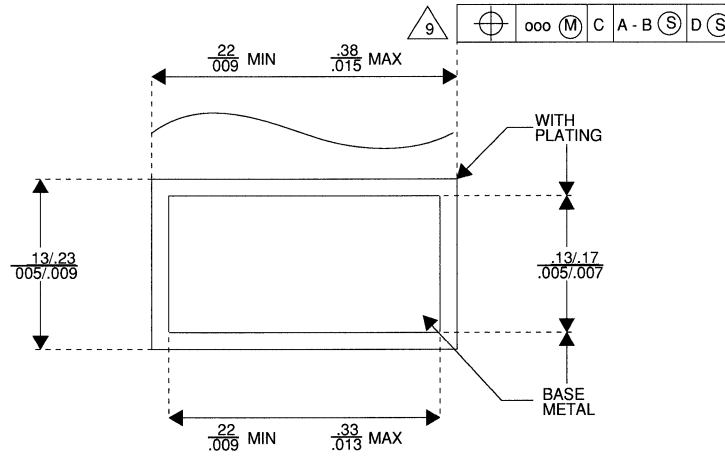


FIGURE 12-1 WD90C26A 144-PIN MQFP PACKAGE MECHANICAL DRAWING


2
-H -
(.10)
004
- C -
Datum Plane
Seating Plane
See Detail "A"
.65 BSC.
.026 BSC
See Detail "B"
5o - 16o
5o - 16o
3.17
.125
MIN
3.67
.144
MAX
.25
010
Base Plane



DETAIL A
SCALE· NONE



DETAIL B
SCALE. NONE

NOTES - UNLESS OTHERWISE SPECIFIED:

10 The exact shape of this feature is optional.

9 Dimension B does not include DAMBAR protrusion. The allowable DAMBAR protrusion shall be .08mm/.003 total in excess of the B dimension at maximum material condition. DAMBAR cannot be located on the lower radius or the foot.

8 Controlling dimension: millimeter.

7 These dimensions are to be determined at datum plane [-H-].

6 Details of pin 1 identifier are optional but must be located within the zone indicated.

5 Dimensions D1 and D1 do not include hold protrusion. Allowable protrusion is.25mm/.010 per side. Dimensions D1 and E1 do include hold mismatch and are determined at datum plane [-H-].

4 To be determined at seating plane [-C-].

3 Datums [A-B] and [-D-] are to be determined at datum plane [-H-].

2 Datum plane [-H-] is located at the hold parting line and is coincident with the bottom of the lead where the lead exits the plastic body.

1 All dimensions and tolerances conform to ANSI Y14.5M-1982.

13.0 I/O ADDRESS USAGE

13.1 INTRODUCTION

This section provides a list of I/O addresses and indexed register addresses used by the WD90C26A.

I/O ADDRESS[1]	BITS	I/O REGISTER NAME
0000-03B3	---	Unused (except for Video Enable Register during setup)
0102	0	Setup Mode Video Enable Register (only 3 LSBs of address are decoded - only accessible in setup)
03B4	7:0	CRTC Index (monochrome emulation)
03B5	(2)	CRTC Data, (monochrome emulation) See 3D4h, 3D5h for CRTC-indexed registers)
03B6-03B7	---	Unused
03B8	7:0	Enable Mode (MDA/Hercules H/W Emulation)
03B9	7:0	Preset Light Pen Latch (MDA H/W Emulation)
03BA	7:0	Input Status Register I (on reads - monochrome emulation) or Feature Control Register (on writes - monochrome emulation) or Status Register (MDA/Hercules H/W Emulation)
03BB	7:0	Reset Light Pen Latch (MDA H/W Emulation)
03BC-03BE	---	Unused
03BF	7:0	Hercules Register (Hercules H/W Emulation)
03C0	7:0	Attribute Controller Index/Data Write
03C1	7:0	Attribute Controller Index/Data Read
		ATTRIBUTE CONTROLLER INDEXED REGISTERS
		3C0 INDEX / **BITS** / **INDEXED REGISTER NAME**
		00-0F / 7:0 / Palette Registers
		10 / 7:0 / Mode Control Register
		11 / 7:0 / Overscan Color Register
		12 / 7:0 / Color Plane Enable Register
		13 / 7:0 / Horizontal Pixel Panning Register
		14 / 7:0 / Color Select Register
		15-1F / - / Unused
		20-FF / - / Repeats of Previous Decodes
03C2	7:0	VGA Miscellaneous Output Register (on writes) or Input Status Register 0 (on reads)
03C3	0	Video Subsystem Enable (only accessible in MicroChannel mode)
03C4	7:0	Sequencer Index
03C5	(2)	Sequencer Data

TABLE 13-1 I/O ADDRESS MAP

I/O ADDRESS[1]	BITS	I/O REGISTER NAME		
		SEQUENCER INDEXED REGISTERS		
		3C4 INDEX	BITS	INDEXED REGISTER NAME
		00	7:0	Sequencer Reset
		01	7:0	Sequencer Clocking Mode
		02	7:0	Sequencer Map Mask
		03	7:0	Sequencer Character Map Select
		04	7:0	Sequencer Memory Mode
		05	7:0	VGA Sequencer Index 5
		06	7:0	PR20 VGA Status Unlock
		07	7:0	PR21 Paradise VGA Status
		08	7:0	Reserved Scratchpad
		09	7:0	Reserved Scratchpad
		0A-0F	-	Unused
		10	7:0	PR30A Memory Interface Write Buffer & FIFO Control
		11	7:0	PR31 System Interface Control
		12	7:0	PR32 Miscellaneous Control Register 4
		13	-	Unused
		14	7:0	PR34A Video Virtual Page
		15	-	Unused
		16	7:0	PR45 Video Signature Analyzer Control
		17	7:0	PR45A Signature Analyzer Data Low
		18	7:0	PR45B Signature Analyzer Data High
		19-1F	-	Unused
		20-FF	-	Repeats of Previous Decodes
03C6	7:0	Internal RAMDAC Pixel Mask		
03C7	7:0	Internal RAMDAC Read Address Register (on writes) or Internal RAMDAC Status Register (on reads)		
03C8	7:0	Internal RAMDAC Write Address		
03C9	7:0	Internal RAMDAC Data		
03CA-03CB	---	Unused		
03CC	7:0	Miscellaneous Output (on reads)		
03CD	---	Unused		
03CE	7:0	Graphics Controller Index		
03CF	7:0	Graphics Controller Data		
		GRAPHICS CONTROLLER INDEXED REGISTERS		
		3CE INDEX	BITS	INDEXED REGISTER NAME
		00	7:0	Set/reset
		01	7:0	Enable Set/reset

TABLE 13-1 I/O ADDRESS MAP

I/O ADDRESS[1]	BITS	I/O REGISTER NAME		
		GRAPHICS CONTROLLER INDEXED REGISTERS (Continued)		
		3CE INDEX	**BITS**	**INDEXED REGISTER NAME**
		02	7:0	Color Compare
		03	7:0	Data Rotate
		04	7:0	Read Map Select
		05	7:0	Mode
		06	7:0	Miscellaneous
		07	7:0	Color Don't Care
		08	7:0	Bit Mask
		09	6:0	PR0A Address Offset A
		0A	6:0	PR0B Alternate Address Offset B
		0B	7:0	PR1 Memory Size
		0C	7:0	PR2 Video Select
		0D	7:0	PR3 CRT Lock Control
		0E	7:0	PR4 Video Control
		0F	7:0	PR5 Unlock PR0-PR4
		10	5:0	PR57 90C26 Feature Register I
		11	0	PR58 90C26 Feature Register II
		12	2:0	PR59 Memory Arbitration Cycle Setup
		13-14	-	Reserved - manufacturing test registers
		15	7:0	PR62 FR Pulse Timing Setup
		16-1F	-	Unused
		20-FF	-	Repeats of Previous Decodes
03D0-03D3	---	Unused		
03D4	7:0	CRTC Index (color emulation)		
03D5	(2)	CRTC Data (color emulation)		
		CRTC INDEXED REGISTERS		
		3B4/3D4 INDEX	**BITS**	**INDEXED REGISTER NAME**
		00	7:0	Horizontal Total
		01	7:0	Horizontal Display End
		02	7:0	Start Horizontal Blanking
		03	7:0	End Horizontal Blanking
		04	7:0	Start Horizontal Retrace
		05	7:0	End Horizontal Retrace
		06	7:0	Vertical Total
		07	7:0	Overflow
		08	7:0	Preset Row Scan

TABLE 13-1 I/O ADDRESS MAP

I/O ADDRESS[1]	BITS	I/O REGISTER NAME		
		CRTC INDEXED REGISTERS (Continued)		
		3B4/3D4 INDEX	BITS	INDEXED REGISTER NAME
		09	7:0	Maximum Scan Line
		0A	7:0	Cursor Start
		0B	7:0	Cursor End
		0C	7:0	Start Address High
		0D	7:0	Start Address Low
		0E	7:0	Cursor Location High
		0F	7:0	Cursor Location Low
		10	7:0	Vertical Retrace Start
		11	7:0	Vertical Retrace End
		12	7:0	Vertical Display Enable End
		13	7:0	Offset
		14	7:0	Underline Location
		15	7:0	Start Vertical Blank
		16	7:0	End Vertical Blank
		17	7:0	Mode Control
		18	7:0	Line Compare
		19	-	Unused
		20-28	-	Reserved - Manufacturing Test Registers
		29	7:0	PR10 Unlock PR11-PR17
		2A	7:0	PR11 Configuration Bits
		2B	7:0	PR12 Scratch Pad
		2C	7:0	PR13 Interlace H/2 Start
		2D	7:0	PR14 Interlace H/2 End
		2E	7:0	PR15 Miscellaneous Control 1
		2F	7:0	PR16 Miscellaneous Control 2
		30	7:0	PR17 Miscellaneous Control 3
		31	2:0	PR18 Flat Panel Status
		32	7:0	PR19 Flat Panel Control I
		33	7:0	PR1A Flat Panel Control II
		34	7:0	PR1B Flat Panel Unlock
		35	7:0	PR30 Mapping Ram Unlock
		36	-	Reserved - Manufacturing Test Register
		37	7:0	PR41 Vertical Expansion Initial Value
		38	7:0	PR33 Mapping RAM Address Count
		39	5:0	PR34 Mapping RAM Data

TABLE 13-1 I/O ADDRESS MAP

I/O ADDRESS[1]	BITS	I/O REGISTER NAME		
		CRTC INDEXED REGISTERS (Continued)		
		3B4/3D4 INDEX	BITS	INDEXED REGISTER NAME
		3A	7:0	PR35 Mapping RAM and Power Down Control
		3B	7:0	PR36 LCD Panel Height Select
		3C	7:0	PR37 Flat Panel Blinking Control
		3D	-	Reserved - Manufacturing Test Register
		3E	7:0	PR39 Color LCD Control
		3F	7:0	PR44 Power-down Memory Refresh Control
		40-FF	-	Repeats of previous index decodes
03D6-03D7	---	Unused		
03D8	7:0	Mode Control (when in CGA/AT&T Hardware Emulation)		
03D9	7:0	Color Select (when in CGA/AT&T Hardware Emulation)		
03DA	7:0	Status Register I (on reads - color emulation) or Feature Control Register (on writes - color emulation) or Status Register (CGA/AT&T Hardware Emulation)		
03DB	7:0	Reset Light Pen Latch (CGA/AT&T H/W Emulation)		
03DC	7:0	Preset Light Pen Latch (CGA/AT&T H/W Emulation)		
03DD	---	Unused		
03DE	7:0	M24 (AT&T Hardware Emulation)		
03DF-46E7	---	Unused		
46E8	7:0	Setup (Accessible in ISA Bus Mode Only)		
46E9-56E7	---	Unused		
56E8	7:0	Repeat Decode of 46E8		
56E9-66E7	---	Unused		
66E8	7:0	Repeat Decode of 46E8		
66E9-76E7	---	Unused		
76E8	7:0	Repeat Decode of 46E8		
76E9-FFFF	---	Unused		

NOTES

1. I/O addresses are decoded using 16 lower address bits.
2. Bits defined for these registers are dependent upon the index values.
3. All address and index numbers are given in hexadecimal notation.

TABLE 13-1 I/O ADDRESS MAP

APPENDIX A
REFERENCE DOCUMENTS

1.0 REFERENCE DOCUMENTS

For further information on Personal Computer (PC) video display applications, refer to the manuals in the following list.

- IBM PC Hardware User Guide (IBM # 6322510)
- IBM PC XT Hardware User Guide (IBM # 6322511)
- IBM PC AT Hardware User Guide (IBM # 6280066)
- IBM PS/2 Model 30 Hardware User Guide (IBM # 68x2230)
- IBM PC AT Technical Reference Manual (IBM # 6280070)
- IBM PS/2 Model 30 Technical Reference Manual (IBM # 68x2201)
- IBM PC Options & Adapters Technical Reference Manual (IBM # 6322509)
- IBM PS/2 BIOS Reference Manual (IBM # 68x2260)
- IBM PC Reference Manual (IBM # 6025005)
- AT&T Video Display Controller VDC 750 / VDC 600 Installation Guide
- Hercules Graphics Card Owner's Manual

APPENDIX B
APPLICATION NOTES AND SOFTWARE UTILITIES

1.0 APPLICATION NOTES

A number of application notes are available from Western Digital sales representatives concerning the WD90C26A Integrated Low Power VGA LCD Controller with Simultaneous Display and the Western Digital family of laptop VGA controllers.

2.0 SOFTWARE UTILITIES

Software utilities are also available to assist customer efforts in evaluating the WD90C26A capabilities and in customizing of the WD90C26A for particular panel applications.

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WD90C26A REGISTERS

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WD90C26A REGISTERS
(Continued)