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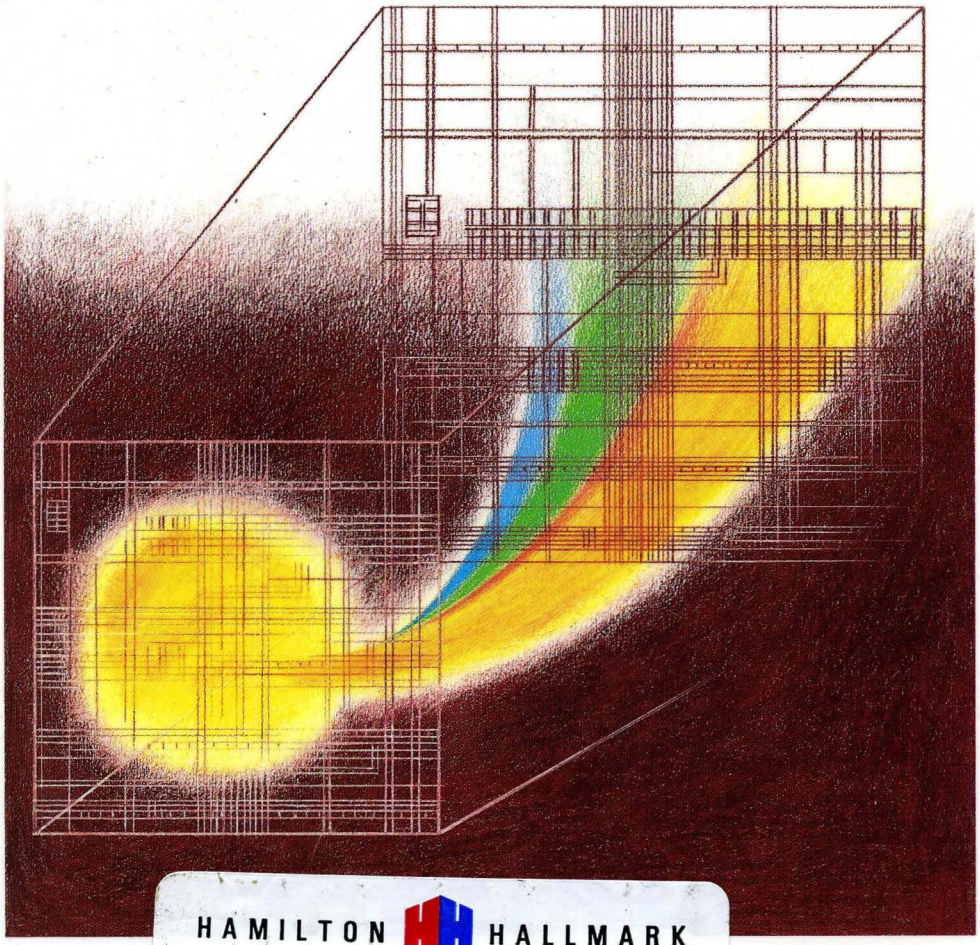
HardWire™ Data Book



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SECTION TITLES

XILINX®

TABLE OF CONTENTS

XILINX®

SECTION 1

Xilinx HardWire Overview

Table of Contents

XILINX®

Xilinx HardWire™ Overview

Advantages of Using Xilinx HardWire

Xilinx programmable solutions offer customers a unique time-to-market and ease-of-development advantage for today's complex system design. Combining the proven benefits of Xilinx Programmable technology with Xilinx' HardWire mask programmed technology provides customers with a no-risk, 100% pin-for-pin compatible path to dramatic cost reductions. Other conversion methodologies require customer engineering resources and are inherently risky.

Choosing the HardWire Option

Whenever a system incorporating Xilinx FPGA's ramps to high production volumes, the HardWire mask programmable solution should be the first consideration for cost reduction. Because the HardWire implementation dramatically reduces the die size by removing programmable elements, the resulting device is much smaller. Often, it is more than 50% less than the equivalent FPGA. Xilinx converts the FPGA design database (.LCA file), which contains all the elements of the verified FPGA design to a HardWire implementation that preserves functionality and all of the nets, pinouts and relative timing of the FPGA. Xilinx conversion requires very little customer involvement, no additional tools, simulations, vectors or test development. Usually, the design can be reviewed within days, and conversion takes 4 weeks to production ready prototypes.

No simulation files or test vectors are required to complete the HardWire device. The customer receives production ready 100% tested devices in the same package as the equivalent Xilinx FPGA. The HardWire design is "self-verifying". Because Xilinx uses the actual .LCA file for conversion, the verified physical database of the design is preserved. 100% fault coverage is guaranteed with Xilinx proprietary ATG.

The HardWire Product Family

For every Xilinx FPGA family, there is a corresponding HardWire Device. HardWire device and packaging specifications match the FPGA specifications.

As listed in table 1-1, the HardWire product chart, there are a range of products available. For an FPGA developed using Xilinx XC4000 family, there are two HardWire options. The XC4400 family is based on Xilinx advanced technology. It is most beneficial for higher volume applications. For applications where low volumes (as low as 1500 pieces per year) are indicated, and where a low NRE is required, the XC4300 family will provide the best fit. Xilinx also supports the low-power 3.3 V XC3000L families, the enhanced features of the "A" families as well as the low cost XC4010D device.

For all products, industrial temperature grades are available.

HardWire versus Full ASIC Gate Array Implementation

Converting a device from FPGA to HardWire has many advantages over gate array redesign. The most important is that Xilinx HardWire methodology requires NO ADDITIONAL CUSTOMER ENGINEERING to convert the FPGA design into a fully tested, completely verified device.

This is because the .LCA file is the actual physical data base that has been previously created and verified in the process of developing the customer FPGA design. Xilinx has the only methodology that preserves all attributes of the original physical data base file. If the design is mapped to a third party library for conversion at the schematic level to another technology, the design must be reverified and a new database must be verified and prototyped. Third party implementation will change the placement, routing and can change the performance of the original device. When this happens, the device needs to be reverified to be certain that the functionality and performance are still intact.

Reverifying the Design

In conventional gate array conversion (redesign), after the schematic is translated or recaptured, the design must be reverified. The process of reverifying a design is rigorous and time consuming. Functional simulation vectors need to be created, and the device must be exhaustively simulated before and after place and route. In addition, testability must be considered and a suitable test methodology must be developed.

Fault Coverage and Test Vectors

All designs need to be testable. In a traditional gate array or conversion the designer is required to build in testability and generate test vectors that verify chip performance by excercising as much of the chip's circuitry as possible. Most designers strive for >95% fault coverage but may settle for less, because the iterative process is extremely time consuming and increases exponentially as fault coverage increased.

Any third party conversion from an FPGA to gate array or other similar technology will require test vector generation. Most customers want the designers to create the vectors, because they are the individuals most familiar with the design implementation. This method ties up valuable design resources and reverses the value of the original decision to use FPGAs for their ease of design and time-to-market advantages. The other method is to contract the conversion or gate array vendor to create the test vectors. This method can be a time consuming and expensive process, since vendors usually charge by the vector. In some cases, conversion or gate array vendors will accept a design without test vectors, but the customer accepts all the liability of determining whether the resulting device is production worthy. In today's competitive market, not many customers can afford the risk of possible respins if the design doesn't work.

Converting from a Xilinx programmable to a HardWire device requires NO TEST VECTOR GENERATION. In the XC3400, XC4300 and XC4400 families, full JTAG implementation is available. Xilinx guarantees 100% fault coverage through a proprietary ATG methodology. All HardWire devices are 100% fully guaranteed to work in the customer's system.

Packaging and Silicon Considerations

Another unique feature of Xilinx ability to convert volume FPGA devices to HardWire LCAs is that all of the physical attributes of the HardWire device are virtually identical to the FPGA. Xilinx uses the same qualified fabrication facilities for both the FPGA and HardWire devices. The same IC process and even the same package and assembly facilities are used. This allows customers to circumvent costly and time consuming requalification efforts. When the product containing the HardWire device nears end-of-life, customers can switch back to the FPGA to avoid end-of-life excess inventory of custom product.

Converting from a Xilinx FPGA to anything but a Xilinx HardWire device means a change to silicon, packaging, assembly and test. Each of these changes add an element of risk into the qualification process .

Table 1-1. HardWire Product Chart

PLD Family	H/W Equivalent	Minimum Order Quantity (Ku)	Minimum Shipment (Ku)
XC4000	XC4403	10	2
	XC4403H	10	2
	XC4405	10	2
	XC4405H	5	1
	XC4406	5	1
	XC4408	5	1
	XC4410	5	1
	XC4410D	5	1
	XC4413	3.5	1
	XC4425	2.5	0.5
	XC4495	10	2
	XC4303	6	2
	XC4305	4	1
	XC4310	1.5	0.4
XC3000	XC3330	10	2
	XC3342	6	1
	XC3390	4	0.5
XC3000L	XC3330L	10	2
	XC3342L	6	1
	XC3390L	4	0.5
XC3000A	XC3330A	10	2
	XC3342A	6	1
	XC3390A	4	0.5
XC3100A	XC3430A	10	2
	XC3442A	6	1
	XC3490A	4	0.5
XC2000	XC2318	7	2

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SECTION 2

HardWire Product Descriptions and Specifications

Table of Contents

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XC4400 HardWire™ LCA Family

Preliminary

Product Specification

Features

- Mask-programmed versions of Programmable Logic Cell Arrays (LCA) FPGA
  - Specifically designed for easy XC4000H and XC4000 series FPGA conversions
  - Significant cost reduction for high volume applications
  - Transparent conversion from FPGA device
  - On-chip scan-path test registers
  - High performance CMOS process
  - Meets XC4000 series -4 speeds (system clock rates of 60-70 MHz)
  - On-chip RAM
- Easy conversion with guaranteed results
  - No customer engineering resource required
  - Fully pin-for-pin compatible
  - Supports most popular package types
  - Same specifications and architecture as programmable FPGA devices
  - Up to 25,000 gate complexity
  - All nets and CLBs preserved
  - FPGA .LCA file used to generate production ready prototypes
  - Prototypes built on production fab line, fully tested to production specification in four weeks

Description

The XC4000 FPGA family provides a group of high-performance, high-density digital integrated circuits. The result of experience gained with two successful FPGA families (XC2000 and XC3000), the XC4000 family provides a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile and abundant routing resources, and surrounded by a perimeter of programmable Input/Output Blocks (IOBs). The general structure of an LCA device is shown in Figure 1.

The XC4400 HardWire LCA are advanced mask-programmed versions of the XC4000 programmable devices. In high-volume applications where the design is stable, the programmable FPGA devices used for prototyping and initial production can be replaced by their HardWire LCA equivalents. This offers a significant cost reduction with virtually no risk or engineering resources required.

In a programmable FPGA device, the logic functions and interconnections are determined by the configuration program data, loaded and stored in internal static-memory cells. The HardWire device has the identical functional architecture as the programmed FPGA device it replaces. In the HardWire device, the logic is optimized for area but maintains the relative CLB placement and logic as the programmed LCA.

Xilinx manufactures the HardWire device using the information from the programmed FPGA design file. Since the

HardWire Device	Replacement for Pin-Compatible Programmable Device	Speed Grade of HardWire Conversion*	File Submitted to Xilinx	Packages											
					PLCC			TQFP/VQFP				PQFP			
				Number of Pins	44	68	84	64	100	144	176	100	160	208	240
XC4402	XC4002	-4	XC4002.LCA	Number of I/Os	-	-	-	-	64	-	-	64	-	-	-
XC4403	XC4003	-4	XC4003.LCA		-	-	80	-	96	-	-	96	-	-	-
XC4403H	XC4003H	-4	XC4003H.LCA		-	-	-	-	-	-	-	-	156	-	-
XC4405	XC4005	-4	XC4005.LCA		-	-	80	-	-	-	-	96	112	-	-
XC4405H	XC4005H	-4	XC4005H.LCA		-	-	-	-	-	-	-	-	156	172	-
XC4406	XC4006	-4	XC4006.LCA		-	-	80	-	-	-	-	96	128	-	-
XC4408	XC4008	-4	XC4008.LCA		-	-	-	-	-	140	-	96	144	144	-
XC4410	XC4010/D	-4	XC4010.LCA		-	-	-	-	-	-	-	96	156	160	-
XC4413	XC4013	-4	XC4013.LCA		-	-	-	-	-	-	-	-	156	192	192
XC4425	XC4025	-4	XC4025.LCA			-	-	-	-	-	-	-	-	-	232

* Consult factory for information if faster speed grades are required.

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HardWire device is both pinout and architecturally identical to the programmable FPGA device, it is easily created without all the costly and time-consuming customer engineering activity that other semicustom solutions would require – no redesign time, no expensive and time-consuming simulation runs, no place and route, no test-vector generation. Xilinx proprietary software checks the design and maintains timing relationships as well as automatically generating test vectors.The combination of the programmable FPGA device and the HardWire LCA offers the fastest and easiest way to get a new product to market, while ensuring low cost, low risk, and high-volume cost reduction.

XC4400 Compared to XC3300

For those readers already familiar with the XC3300 family of Xilinx HardWire LCAs, here is a concise list of the major new features in the XC4400 family.

CLB has two **independent** 4-input function generators.
A **third** function generator combines the outputs of the two other function generators with a ninth input.
All function inputs are swappable, all have full access; none are mutually exclusive.
CLB has **very fast arithmetic carry** capability.
CLB function generator look-up table can also be used as high-speed **RAM.**
CLB flip-flops have asynchronous set **or** reset.
CLB has **four outputs**, two flip-flops, two combinatorial.
CLB connections symmetrically located on all **four** edges.

IOB has more versatile clocking polarity options.
IOB has programmable input set-up time:
long to avoid potential hold time problems,
short to improve performance.
IOB has Long Line access through its own TBUF.
XC4400 can sink up to 24 mA and source up to 12 mA per output.

IEEE 1149.1- type **boundary scan** is supported in the I/O.

Wide decoders on all four edges of the LCA.

Increased **number of interconnect resources.**
All CLB inputs and outputs have **access to most interconnect lines.**
Switch Matrices are simplified to increase speed.
Eight global nets can be used for clocking or distributing logic signals.
TBUF output configuration is more versatile and 3-state control less confined.

Program is single-function input pin, overrides everything.
INIT pin also acts as Configuration Error output.

Start-up can be **synchronized** to any user clock (this is a configuration option).
No Powerdown, but instead a **Global 3-state input** that does not reset any flip-flops.
No on-chip **crystal oscillator** amplifier.

Configuration Clock can be increased to **8 MHz.**

Parameter	XC4400	XC3300	XC2300
Max number of flip-flops	2560	928	174
Max number of user I/O	256	144	74
Max number of RAM bits	32,768	0	0
Function generators per CLB	3	2	2
Number of logic inputs per CLB	9	5	4
Number of logic outputs per CLB	4	2	2
Number of low-skew global nets	8	2	2
Dedicated decoders	yes	no	no
Fast carry logic	yes	no	no
Internal 3-state drivers	yes	yes	no
Output slew-rate control	yes	yes	no
Power-down option	no	yes	yes
Crystal oscillator circuit	no	yes	yes

Comparison of Xilinx HardWire LCA Families

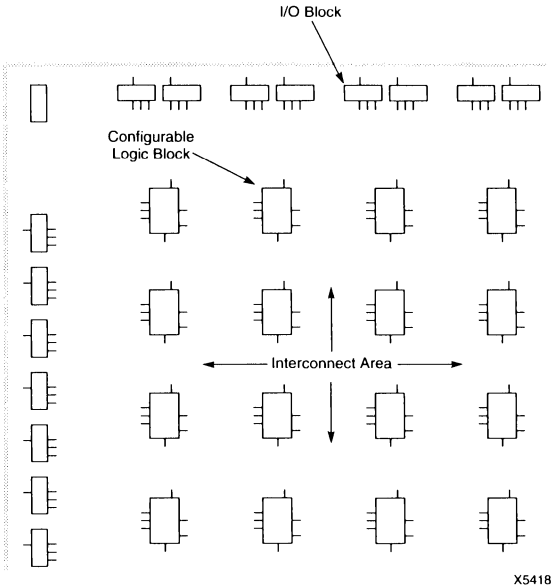


Figure 1. Logic Cell Array Structure

Architectural Overview

The XC4400 family achieves high speed through advanced semiconductor technology and through improved architecture, and supports system clock rates of 60 to 70 MHz. Compared to older Xilinx FPGA families, the new family is more powerful, offering on-chip RAM and wide-input decoders. It is more versatile in its applications, and design cycles are faster due to a combination of increased routing resources and more sophisticated software. And last, but not least, it more than doubles the available complexity, up to the 25,000-gate level.

As shown in Figure 1, the HardWire LCA has the same architecture as the programmable FPGA device it replaces. The perimeter of I/O Blocks (IOBs) provides an interface between the internal logic array and the device package pins. The array of Configurable Logic Blocks (CLBs) performs user-specified logic functions. The interconnect resources are programmed to form networks carrying logic signals among blocks, analogous to printed-circuit-board traces connecting SSI/MSI packages.

I/O Block

Each user-defined IOB, shown in Figure 3, provides an interface between the external package pin and the internal user logic. It can be defined for input, output or bidirectional signals. The IOB is identical to that used in the programmable LCA device. There are a wide variety of I/O options available to the user.

Summary of I/O Options

Inputs

- Direct
- Latched/registered
- Programmable pull-up/pull-down resistor

Outputs

- Direct/registered
- Inverted/not inverted
- 3-state/on/off
- Full speed/slew limited
- 3-state/output enable (active Hi or Lo)
- Programmable pull-up/pull-down resister

See *The XC4000 Data Book* for more details on IOB operation.

Configurable Logic Block

The array of Configurable Logic Blocks (CLBs) provides the functional elements from which the user's logic is constructed. The powerful and flexible XC4000/4400 CLB provides more capability than previous generations of LCA devices, resulting in more "effective gates per CLB." See Figure 4.

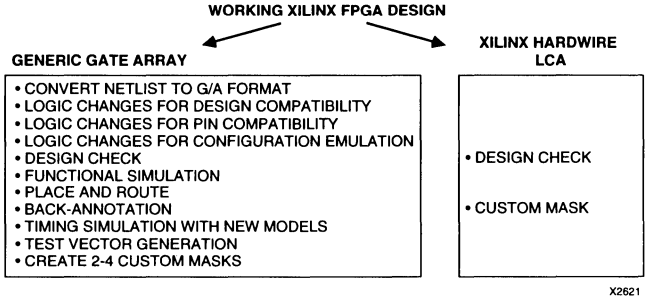


Figure 2. Design Conversion: HardWire LCA vs. Generic Gate Array

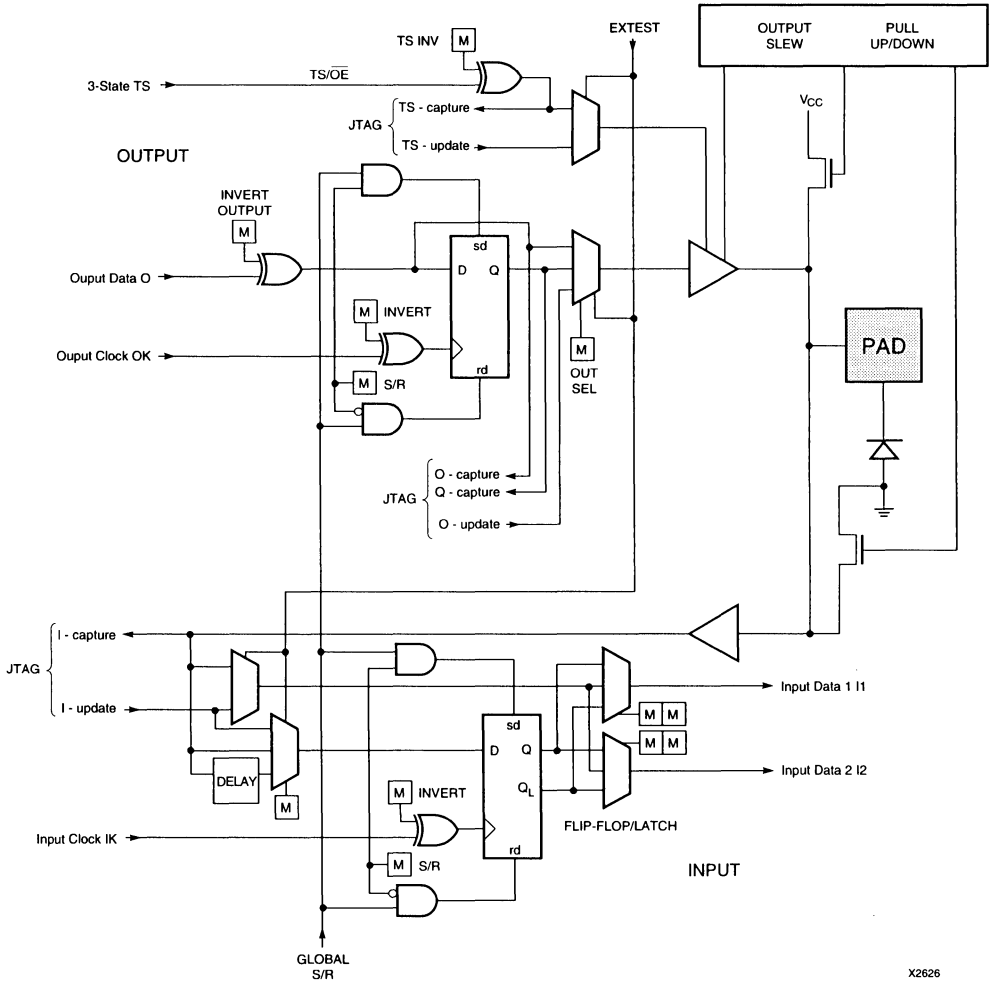


Figure 3. I/O Block

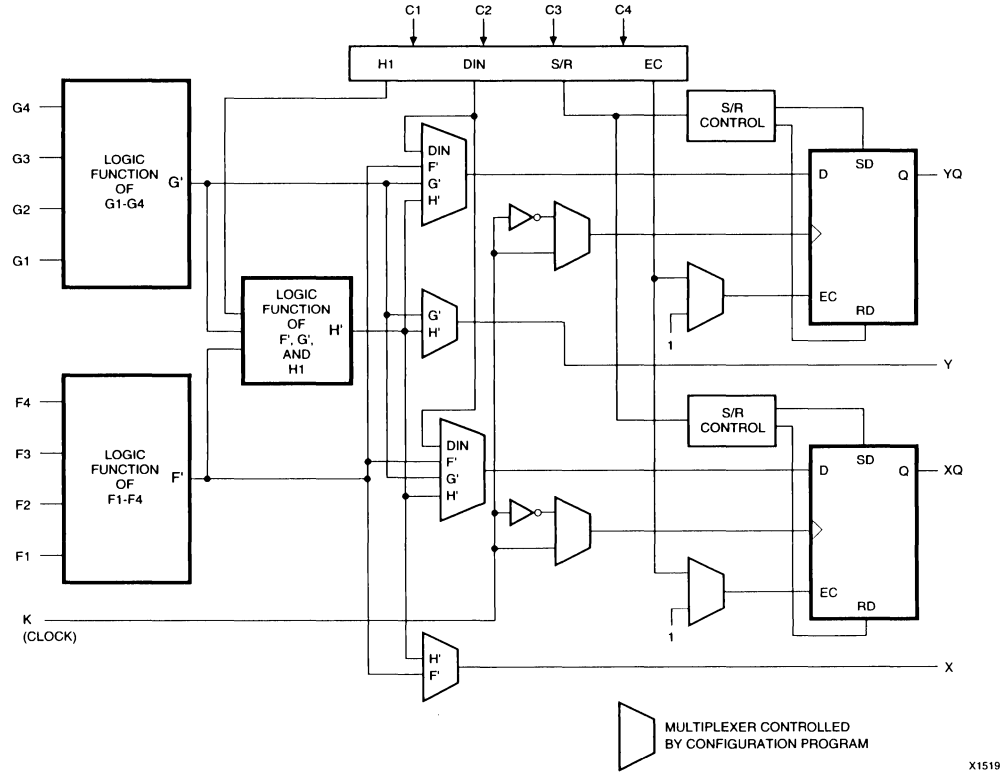


Figure 4. Simplified Block Diagram of XC4000 Configurable Logic Block

The XC4400 family is similar to the XC4300 with further silicon area optimization. It maintains the same fundamental HardWire philosophy of guaranteed compatibility so that no re-engineering of the design in the conversion process is necessary. The customer engineers the FPGA design once, and Xilinx provides a low-cost, high-volume production solution with no extra work from the customer. In contrast, most gate array conversion path requires significant re-engineering.

The XC4400 HardWire technology further optimizes silicon area by removing all unused logic in a CLB, and removing any unused CLBs. In fact, all unused FPGA features are eliminated in the XC4400. However, using our DesignLock™ technology, the implementation of the CLB (including placement and routing) are maintained. This unique conversion process also eliminates the need for timing simulation. Timing is guaranteed through our Design Review process with the aid of our proprietary software.

The versatility of the CLB function generators improves system speed significantly. In addition, the CLB can pass the combinatorial outputs to the interconnect network, and can also store the combinatorial results or other incoming data in one or two flip-flops, and connect their outputs to the interconnect network as well. The flip-flops can be used as registers or shift registers without blocking the function generators from performing a different, perhaps unrelated, task. This increases the functional density of the device.

See The *XC4000 Data Book* for more information on Configurable Logic Blocks.

Interconnect

User-defined interconnect resources in the LCA provide routing paths to connect inputs and outputs of the I/O and logic blocks into logic networks.

The speed of the interconnect paths of the HardWire LCA is significantly faster, since all interconnections are fixed metal connections.

Architectural Enhancements

Compared to older LCA families, XC4400 HardWire LCAs provide significant enhancements. Powerful system features, as listed below, are incorporated to improve system speed, device flexibility, and ease of use.

- On-Chip Memory
  The XC4000/XC4400 family provides very fast on-chip RAM/ROM capability. Each CLB can be configured as a small memory block that can be combined with as many other CLBs as desired. This reduces the cost of distributed memory dramatically.

- Wide Decoding
  The XC4400 family has up to 16 very fast decoders located at the chip periphery, four on each chip edge. They accept I/O signals and internal signals as input and generate a very fast decoded output. This fast-decoding feature makes designing with FPGAs easier in many applications.

- Fast Carry Logic
  Each CLB includes high-speed carry logic. The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods, like carry generate/propagate, are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level.

  The fast-carry logic opens the door to many new applications involving arithmetic operation where the previous generations of FPGAs were not fast or efficient enough. High-speed address offset calculations in microprocessors or graphics systems, and high-speed addition in digital-signal processing are two typical applications.

- JTAG Boundary Scan
  The XC4000/XC4400 family implements IEEE 1149.1 Boundary-scan methodology. This technique permits systems manufacturers to test their PC boards more safely, thoroughly, and efficiently, at significantly lower cost than using the traditional bed-of-nails test.

Configuration Sequence

The XC4400 has two general modes of powering-up: "Instant-On", and "Configuration Emulation." Both of these modes will be discussed in detail in the **"Configuration Modes for HardWire LCAs"** section.

If the customer chooses the "Instant-On" option, the XC4400 becomes operational after Power-On-Reset (POR). If the customer chooses the "Configuration Emulation" option, the sequence of events at Power-On is as follows:

1. Power-On Reset (POR)
2. Initialization
3. Configuration
4. Startup
5. Operation

The first step, Power-On Reset (POR), begins as power is being applied to the device. When V_{CC} reaches approximately 3 V, and after a delay of approximately 16 ms, the HardWire LCA releases a special Power-On Reset to guarantee each flip-flop comes to a known state. During the time POR is held and up until the end point specified by the start-up sequence, the I/O buffers are 3- stated. As soon as the POR is released, an internal counter waits for a specific amount of time to guarantee power up. If the device is a master device, then the delay will be four times the delay for any slaves. This ensures that all daisy-chained slave devices will have sufficient time to power-up. The HardWire LCA then begins the Initialization stage.

The second step, Initialization, behaves differently than the programmable LCA. A XC4000 programmable FPGA will drive the INIT pin in slave mode while it is clearing its internal configuration RAM. This step is superfluous in a HardWire LCA since there is no RAM to configure. The XC4400 HardWire LCA in slave mode generates a LOW on the INIT pin for the duration of its POR, but releases it as soon as POR is complete. The XC4000 programmable LCA in master mode will wait until it has complete clearing its own memory, and then sample the INIT pin to ensure that all slaves, if any have been initialized. The master mode HardWire LCA samples the INIT pin for a High and waits in the initalization step until after its INIT pin is High. This time is normally around 250 µs if an XC4000 device is present in the chain. If the customer's board has all XC4400 HardWire LCAs on the board, this time will be almost instantaneous. Following the end of the Initialization stage, the HardWire LCA proceeds to the Configuration stage.

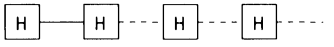
This next step, Configuration, is detailed under the **"Configuration Modes for HardWire LCAs"** section.

The XC4400 HardWire LCA can be a standalone replacement of the corresponding XC4400 FPGA, as shown in the example in Figure 4a. In a daisy chain, the XC4400 is fully interchangeable with any programmable device in the chain as shown in example 2, 3, and 4 in Figure 4a. For more information on the specifics of the startup mechanism, please see the XC4000 Data Sheet.

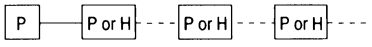
The final stage is normal operation for the device. This is exactly as it was for the programmable LCA that the HardWire LCA is replacing.

Mode 1. As a stand alone HardWire LCA Device.

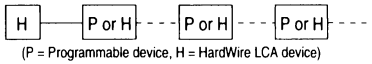
Mode 2. As a daisy chain of all HardWire LCA Devices.



Mode 3. As a HardWire LCA or programmable slave in a daisy chain with a Programmable device as a master.



Mode 4. As a HardWire LCA device acting as a Serial Master with any combination of Programmable and HardWire LCA devices as slaves.



(P = Programmable device, H = HardWire LCA device)

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Figure 4a.

The fourth step, Startup, is the normal startup sequence that programmable LCAs go through at the end of the configuration process. The Startup step is a means for the customer to control the way that the HardWire LCA transists between the configuration stage and the operational stage. The customer sets the order in which three major events take place:

- When the DONE pin goes High
- When the Outputs are no longer 3-stated
- When the internal Global Reset is Released

The default sequence of events is: I/Os active, release of internal global reset, and Done pin High. At the end of the Startup stages, the HardWire LCA with the "Configuration Emulation" option will behave like a programmed LCA.

Configuration Modes for HardWire LCAs

Instant-On

The HardWire LCA provides greater flexibility than the XC4000 programmable FPGA equivalent because it supports an "Instant-On" feature. This feature permits the HardWire LCA to "Power-On" as if it were already programmed.

The "Instant-On" option may also be used in a daisy chain of LCAs. In this mode, the HardWire LCA simply passes the DIN to the DOUT pin via an internal buffer. The HardWire LCA that uses "Instant-On" may not be a master LCA device, because it does not emulate any configuration mode. The customer would have to remove the configuration bitstream for the HardWire device using this option from the storage element used for programming the LCA chain.

Configuration Emulation

The HardWire LCA is capable of emulating all of the XC4000 programmable FPGA configuration modes. The M2, M1, and M0 bit definitions are the same as the XC4000 LCA, and are listed in Table 2-1. The HardWire Master-mode LCA differs slightly from the programmable equivalent in that it is not capable of changing the startup sequence. This information is fixed at the time of the Design Review with Xilinx, and can not be altered once masks have been generated. In master mode, the XC4400 HardWire LCA is capable of switching to fast 8 MHz CCLK generation, if the configuration bitstream indicates this mode. All slave-mode HardWire LCAs support the slow or fast configuration.

When the HardWire LCA is in configuration mode, it simply swallows (or ignores) the configuration data until it is 'configured'. This means that the HardWire LCA is capable of mixing with programmable LCAs in a daisy chain as shown in figure 4a. At the Design Submittal, the customer will document to Xilinx the setting of the M2, M1, and M0 bits, along with the size of the programmable LCA (e.g. XC4005A). This information will be used to determine how many bits of the bit-stream to swallow. When the XC4400 HardWire LCA begins to receive its configuration data stream, it simply counts the correct number of bits. The HardWire LCA ignores the incoming data until it has reached the end of its configuration data stream. If there is another LCA downstream, the HardWire will then begin passing data down stream until all LCAs in the chain are configured. When the last FPGA/HardWire is programmed, all the FPGA/HardWire LCAs will go into the Startup mode.

Table 2-1. Configuration Modes

Mode	M2	M1	M0	CCLK	Data
Master Serial	0	0	0	output	Bi-Serial
Slave serial	1	1	1	input	Bi-Serial
Master Parallel up	1	0	0	output	Byte-Wide, 00000 ↑
Master parallel down	1	1	0	output	Byte-Wide, 3FFFF ↓
Peripheral Synchr.	0	1	1	input	Byte-Wide
Peripheral Asynchr.	1	0	1	output	Byte-Wide
Reserved	0	1	0	—	—
Reserved	0	0	1	—	—

Peripheral Synchronous can be considered Slave Parallel

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Power Distribution

Power for the HardWire LCA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the device, dedicated V_{CC} and ground rings surround the logic array and provide power to the I/O drivers. An independent matrix of V_{CC} and ground lines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically a 0.1-µF capacitor connected near the V_{CC} and ground pins will provide adequate decoupling.

Output buffers capable of driving the specified 12-mA/24-mA loads under worst-case conditions may be capable

of driving many times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads. The I/O Block output buffers have a slew-limited mode which should be used where output rise and fall times are not speed critical. Slew-limited outputs maintain their dc drive capability, but generate less external reflections and internal noise. A maximum total external capacitive load for simultaneous fast-mode switching in the same direction is 200 pF per power/ground pin pair. For slew-rate limited outputs this total is four times larger.

HardWire LCA Design Considerations

It is important to observe good design practices while using HardWire LCAs. It is possible for a programmable device to "hide" some less obvious design shortcomings. However, these can manifest themselves when the design is converted to a HardWire LCA.

For example, a small glitch generated from unstable inputs to a CLB function block can be easily "swallowed" if the output is driving a long net. This is because the "pass transistors" act as a Low pass filter and this net's loads may never see the glitch. However, in a HardWire LCA, this glitch may propagate to the loads since there are only metal lines and vias in the routing path.

Gated Clocks and Reset Directs

Glitching function generators driving CLOCK and RESET DIRECT pins can inadvertently trigger flip-flops to an undesirable state. Avoid these so-called "gated" clock and reset direct nets; if unavoidable, design the logic so that the inputs are always stable and the signal changes are at least a CLB delay (T_{ILO}) apart.

Multiplexers Implemented in Function Generators

Two input multiplexers can be easily implemented in a single F or G function generator. However, there is a possibility of a glitch if the selected signal and the selected input changes within a CLB's Tilo delay. This is generally not a problem with data and address multiplexers as long as the output is given enough time to settle; but if the multiplexer output is feeding a CLOCK and/or a RESET DIRECT pin, it is possible to toggle the register at undesired times.

The edge(s) of select signals for a CLOCK and/or RESET DIRECT multiplexers should be stable before and after the edges of the inputs. The edges should be at least a CLB (T_{ILO}) delay apart.

Race Conditions

All race conditions in the circuit need to go through a careful analysis. Depending on the routing resources responsible for the net delays, the correct signal may always "win the race" in a programmable FPGA; however, once converted to HardWire LCA, this may not be the case. (See Figure 5.)

Delay Generators

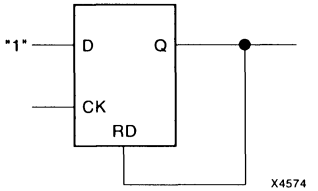
Using the routing resources as delay lines in programmable FPGAs is undesirable. In HardWire LCAs, it is an invitation for timing problems. All submitting delay generators should be removed and the circuit redesigned before submitting it for HardWire LCA conversion.

Combinational Loops

Combinational feedback loops may cause incorrect circuit operation due to differences in routing delays. These should be avoided when ever possibe. If they must be used, the customer should report such information, including correct functional timing relationships to Xilinx.

One-Shots

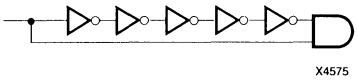
One-shots, implemented by feeding Q back to the RD pin where the pulse width is determined by the RD to Q delay, will have a different pulse width in the XC4400 HardWire. Care should be taken in the use of such circuits. These circuits should be identified to Xilinx.



One Shot Circuit

Choppers or Differential Circuits

Choppers or differential circuits where the pulse width is determined by the difference in delays between two reconvergent paths should not be used.



Differential Circuits

Ring Oscillators

Ring Oscillators where the oscillation frequency is determined by the propagation delay time through all the inverters in the ring should not be used.

"Tweaked" FPGA Design

Any design technique or structure that is normally unpredictable, but is "tweaked" to work in the FPGA may not work in the XC4400 HardWire device. "Tweaking" includes deliberate lengthening of routing to meet hold time, addition of extra delay gates to lengthen a path, etc.

Interfacing with External Devices

Almost all LCAs interface with external devices–FIFOs, memories, processors and peripherals, etc. Handshaking with devices requires specific setup/hold times. Ample hold

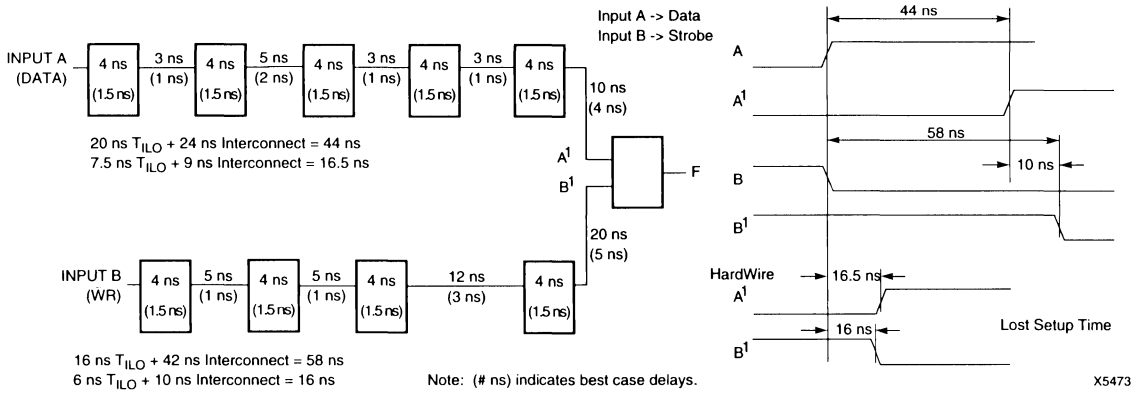


Figure 5. Race Condition Example

time on a data bus from a programmable FPGA may no longer meet spec in HardWire LCA. An external data bus clocked by a HardWire LCA generated signal may no longer meet the system hold time requirements. This can happen because interconnects are much faster than in a programmable device. This requires you to also review the system timing specs when converting to a HardWire LCA.

In reality, all designers using LCAs (programmable or HardWire) face the same issues. Due to improvements in process and circuit design, a part specified at -6 today may actually be running as fast as -5 or even close to -4 in the future. Xilinx does NOT guarantee a part against minimum timing specs. A "glitch" that was swallowed in a device today may crop up in a future device due to faster pass transistors in the routing paths. When using any Xilinx LCAs, the above issues should be addressed in the design phase.

Other HardWire Design Considerations

Simultaneous Switching Outputs

If the time difference between two outputs switching is less than 8 ns, those outputs are considered to be simultaneous. When several output signals are switched on at the same time, the current surge combined with wire inductance generates noise on the supply lines. The high output buffer current (I_{OL} = 24 mA maximum) increases noise problems further. To minimize this noise, spare pads should be allocated to V_{SS}.

The maximum number of simultaneous outputs is 32, provided the following three conditions are met.

1. The input pins are separated from the output pins.
2. V_{SS} pads are allocated to the pads on either side of a simultaneous output buffer.
3. Extra V_{SS} pads are allocated in accordance with the information below.

For example, in the case of 16 simultaneous outputs, if the external load is 50 pF and I_{OL} is 12 mA, the table indicates that two V_{SS} pads will be required. These should be added as shown in figure 6.

Each V_{DD} pad provide about 100 mA of simultaneous switching capability. Additional V_{DD} pads should be added accordingly.

The simultaneous switching output design rules should be observed during the FPGA design process in order for the XC4400 HardWire conversion process to go more smoothly.

Pad Allocations

Input Pads

Input pads, particularly clock input pads, are easily affected by noise and should be positioned away from output pads.

24 mA Output Drive

There is a restriction as to which pad can be used to drive 24 mA. These pads are located in the top and bottom of the XC4400 die where special power rails are reserved. Table 2 shows which pin can be used for each device/package combination:

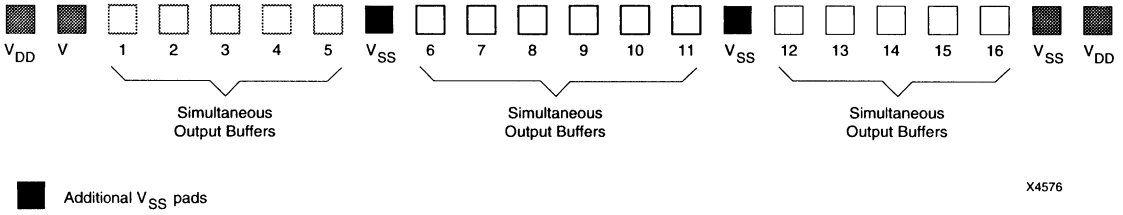


Figure 6. Simultaneous Switching Outputs

Table 1. Simultaneous Switching Outputs

Number of simultaneous outputs	Drive Current I_{OL} (mA)	Additional V_{ss} pads		
		Ext load = 50 pF	Ext load = 100 pF	Ext load = 200 pF
8	4	0	1	2
	12	1	2	3
	24	1	2	4
16	4	1	2	4
	12	2	3	5
	24	2	4	6
24	4	1	3	6
	12	2	5	7
	24	3	6	8
32	4	2	4	8
	12	3	6	12
	24	4	8	16

Table 2. 24 mA Output Pin Allocation

Device	Package	Pins Capable of 24 mA Drive			Total Pins Available
XC4002A	PC84	P1 to P11,	P33 to P53,	P75 to P84	42
	PQ100	P1 to P2,	P29 to P52,	P79 to P100	48
	VQ100	P1 to P25,	P51 to P75		50
XC4003A	PC84	P1 to P11,	P33 to P53,	P75 to P84	42
	PQ100	P1 to P2,	P29 to P52,	P79 to P100	48
	VQ100	P1 to P25,	P51 to P75		50
XC4004A	PC84	P12 to P32,	P54 to P74		42
	TQ144	P1 to P36,	P73 to P108		72
	PQ160	P4 to P37,	P81 to P120		67*
XC4005A	PC84	P12 to P32,	P54 to P74		42
	TQ144	P1 to P36,	P73 to P108		72
	PQ160	P4 to P37,	P81 to P120		67*
	PQ208	P4 to P49,	P108 to P153		80*

* Actual number of pins available is less than the total number specified in the ranges. For example, one cannot use all 46 pins of the XC4005A PQ208 specified in the range "P108 to P153". Only 40 of them can be used.

XC4000/XC4400-Family Pin Assignments

Xilinx offers members of the XC4400 family in a variety of surface-mount package types, with pin counts from 84 to 240.

Each chip is offered in several package types to accommodate the available PC-board space and manufacturing technology. Most package types are also offered with different chips to accommodate design changes without requiring PC-board changes.

Pin Descriptions

Permanently Dedicated Pins.

V_{CC}
Eight or more (depending on package type) connections to the nominal +5 V supply voltage. All must be connected.

GND
Eight or more (depending on package type) connections to ground. All must be connected.

TDO
If boundary scan is used, this is the Test Data output. If boundary scan is not used, this pin is a 3-state output without a register, after configuration is completed.

This pin can be a user output only when called out by special schematic definitions.

TDI, TCK, TMS
If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively, coming directly from the pads and bypassing the IOBs. These pins can also be used as inputs to the CLB logic after configuration is completed.

If the boundary-scan option is not selected, all boundary-scan functions are inhibited once configuration is completed; these pins then become user-programmable I/O.

PGCK1 - PGCK4
Each of four Primary Global inputs drives a dedicated internal global net with short delay and minimal skew. If not used for this purpose, any of these pins can be used as a user-programmable I/O.

SGCK1 - SGCK4
Each of four Secondary Global inputs can drive a dedicated internal global net that alternatively can also be driven from internal logic.

Unrestricted User-Programmable I/O Pins.

An I/O pin may be programmed by the user to be an Input or an Output pin following configuration. Before configuration is completed, these pins have an internal high-value pull-up resistor that defines the logic level as High.

Dedicated or Special Pins on XC4400 HardWire LCA

Pin Function			
		Configuration Emulation Mode	
Pin Name	**Instant-On**	**During Configuration**	**During Operation**
M0	M0/User Input (1,2)	M0	User Input (1,2)
M1	M1/User Output (1,2)	M1	User Output (1,2)
M2	M2/User Input (1,2)	M2	User Input (1,2)
CCLK	HIGH - Internal Pull-up	Master: Output, Slave; Input	HIGH - Internal Pull-up
$\overline{\text{PROGRAM}}$	Global Reset Device	$\overline{\text{PROGRAM}}$ Input	Global Reset Device - "Reconfigure"
DONE	User I/O	DONE Output	HIGH - Internal Pull-up
HDC	User I/O	HDC Output	User I/O
$\overline{\text{LDC}}$	User I/O	$\overline{\text{LDC}}$ Output	User I/O
$\overline{\text{INIT}}$	User I/O	Master: $\overline{\text{INIT}}$ Input, Slave POR Output	Open Drain
DIN	User I/O	DIN Pin	User I/O
DOUT	User I/O	DOUT Pin	User I/O

Notes:
1. User Pin is only accessible through special schematic I/O Macros
2. Pin does not have an associated IOB register(s)

X5477

XILINX®

XC4300 HardWire™ LCA Family

Product Specification

Features

- Mask-programmed versions of Programmable Logic Cell Arrays (LCA) FPGA
  - Specifically designed for easy XC4000 series FPGA conversions
  - Significant cost reduction for high volume applications
  - Transparent conversion from FPGA device
  - On-chip scan-path test latches
  - High performance submicron (0.8 µ) CMOS process
  - Meets XC4000 series -4 speeds (system clock rates of 60-70 MHz)
  - On-chip ultra-fast RAM
- Easy conversion with guaranteed results
  - No customer engineering resource required
  - Fully pin-for-pin compatible
  - Supports most popular package types
  - Same specifications and architecture as program mable FPGA devices
  - Up to 10,000 gate complexity
  - All nets and CLBs preserved
  - FPGA .LCA file used to generate production ready prototypes
  - Prototypes built on production FAB line, fully tested to production specification in four weeks

Description

The XC4000 LCA family provides a group of high-performance, high-density digital integrated circuits. The result of experience gained with two successful LCA families (XC2000 and XC3000), the XC4000 family provides a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile and abundant routing resources, and surrounded by a perimeter of programmable Input/Output Blocks (IOBs). The general structure of an LCA device is shown in Figure 1.

The XC4300 HardWire LCA are mask-programmed versions of the XC4000 programmable devices. In volume applications where the design is stable, the programmable FPGA devices used for prototyping and initial production can be replaced by their HardWire LCA equivalents. This offers a significant cost reduction with virtually no risk or engineering resources required.

In a programmable LCA device, the logic functions and interconnections are determined by the configuration program data, loaded and stored in internal static-memory cells. The HardWire LCA has the identical architecture as the programmable FPGA device it replaces. All CLBs, IOBs, interconnect topology, power distribution and so on are the same. In the HardWire LCA, the memory cells and the logic they control are replaced by metal connections. Thus the HardWire LCA is a semicustom device manufactured to provide a customer specific function, yet is completely compatible with the programmable FPGA device it replaces.

Xilinx manufactures the HardWire LCA using the information from the programmable LCA design file. Since the HardWire device is both pinout and architecturally identical to the programmable LCA device, it is easily created without all the costly and time-consuming engineering activity that other semicustom solutions would require – no redesign time, no expensive and time-consuming simulation runs, no place and route, no test-vector generation. The combination of the programmable FPGA device and the HardWire LCA offers the fastest and easiest way to get a new product to market, while ensuring low cost, low risk, and high-volume cost reduction.

HardWire Device	Replacement for Pin-Compatible Programmable Device	Approximate Usable Gate Count	File Submitted to Xilinx	No. of I/Os Available per Package									
				PLCC		VQFP	TQFP		PQFP			PGA	BGA
				Pins	84	100	100	144	100	160	208	191	225
XC4303	XC4002A, XC4003/A	3,000	4003.LCA	I/Os	61	–	77	–	77	–	–	–	–
XC4305	XC4004A, XC4005/A	5,000	4005.LCA		61	–	–	112	–	112	112	–	–
XC4310	XC4006, XC4008, XC4010/D	10,000	4010.LCA		–	–	–	–	–	160	160	160	–

Electrical Characteristics

The XC4300 HardWire LCA family is form, fit and function compatible with the XC4000 FPGA family. Accordingly, all XC4300 HardWire devices meet the electrical specifications of the respective XC4000 FPGA device for the -4 Speed Grade. For specific data, please see the XC4000 section of the Xilinx Programmable Logic Data Book. Absolute Maximum Ratings, Operating Conditions, DC Characteristics, Input to Output Parameters (Pin-to-Pin) and Switching Characteristics of the -4 Speed Grade of the appropriate device type apply.

XC4300 Compared to XC3300

For those readers already familiar with the XC3300 family of Xilinx HardWire LCA's, here is a concise list of the major new features in the XC4300 family.

CLB has two **independent** 4-input function generators.
A **third** function generator combines the outputs of the two other function generators with a ninth input.
All function inputs are swappable, all have full access; none are mutually exclusive.
CLB has **very fast arithmetic carry** capability.
CLB function generator look-up table can also be used as high-speed **RAM.**
CLB flip-flops have asynchronous set **or** reset.
CLB has **four outputs**, two flip-flops, two combinatorial.
CLB connections symmetrically located on all **four** edges.

IOB has more versatile clocking polarity options.
IOB has programmable input set-up time:
long to avoid potential hold time problems,
short to improve performance.
IOB has Long Line access through its own TBUF.
Outputs are **n-channel only**, lower VOH increases speed, outputs do not clamp to V_{CC}.
XC4303 and XC4305 can sink 24 mA per output; XC4310 12 mA per output

IEEE 1149.1- type **boundary scan** is supported in the I/O.

Wide decoders on all four edges of the LCA.

Increased **number of interconnect resources.**
All CLB inputs and outputs have **access to most interconnect lines.**
Switch Matrices are simplified to increase speed.
Eight global nets can be used for clocking or distributing logic signals.
TBUF output configuration is more versatile and 3-state control less confined.

Program is single-function input pin, overrides everything.
INIT pin also acts as Configuration Error output.

Start-up can be **synchronized** to any user clock (this is a configuration option).
No Powerdown, but instead a **Global 3-state input** that does not reset any flip-flops.
No on-chip **crystal oscillator** amplifier.

Configuration Bit Stream includes **CRC error checking.**
Configuration Clock can be increased to **>8 MHz.**
Configuration Clock is **fully static**, no constraint on the maximum Low time.

Parameter	XC4300	XC3300	XC2300
Max number of flip-flops	2280	928	174
Max number of user I/O	240	144	74
Max number of RAM bits	28,800	0	0
Function generators per CLB	3	2	2
Number of logic inputs per CLB	9	5	4
Number of logic outputs per CLB	4	2	2
Number of low-skew global nets	8	2	2
Dedicated decoders	yes	no	no
Fast carry logic	yes	no	no
Internal 3-state drivers	yes	yes	no
Output slew-rate control	yes	yes	no
Power-down option	no	yes	yes
Crystal oscillator circuit	no	yes	yes

Three Generations of Xilinx HardWire LCA Families

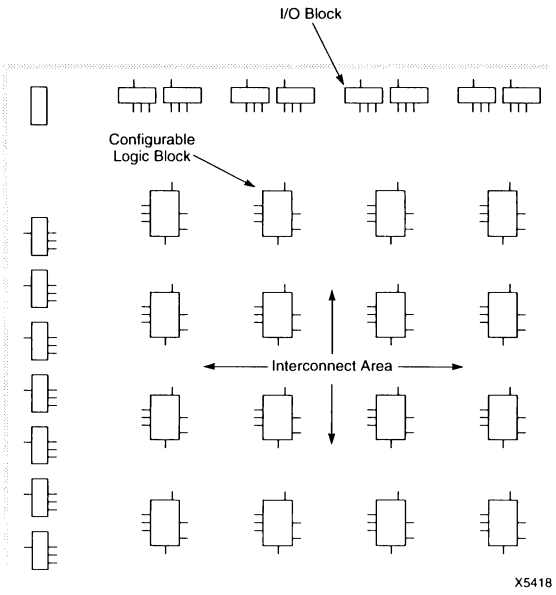


Figure 1. Logic Cell Array Structure

HardWire LCA Application

HardWire LCAs are designed to provide a simple, low-risk method for achieving significant cost-reductions on a high-volume design that initially used a programmable FPGA device. In the prototype and early production stages, and for low-to-moderate volume applications, the programmable FPGA device is the best choice. Later in the life cycle – when the design is stable and in high-volume production – the HardWire LCA can be used in place of the original programmable device.

Figure 2 shows the typical life cycle of a high-volume product, and illustrates the optimal way for using the programmable and HardWire devices. During the development and prototype stages, the programmable FPGA device is used.

Production is started using a programmable device and the design includes a method for storing the configuration bitstream. Using a programmable device at this stage reduces risk, assures a faster time to market, and permits design modifications to be made without obsoleting any LCA devices. After production has begun with the programmable device, the HardWire LCA can be substituted in the circuit. This may also permit removal of an EPROM used for bitstream storage.

Since the circuit board was designed initially for a programmable device, production can be switched back if the situation warrants. For example, if demand for the product increases dramatically, production can be increased in days or weeks by using programmable devices. A change can be quickly made to the product with a programmable device. There is no manufacturing lead time with off-the-shelf, standard programmable devices. As another example, production can be switched to programmable devices as the product nears the end of the life cycle. This avoids end-of-life buys and the risk of obsolescence.

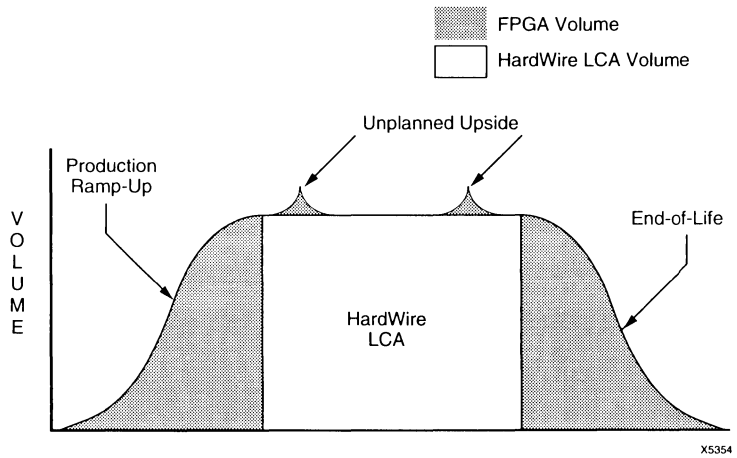


Figure 2. Typical High-Volume Product Life Cycle

HardWire Design/Production Interface

Figure 3 shows how the design, development and production activities are sequenced for both the programmable and HardWire products. Notice that no additional activity is needed for the HardWire LCA until the design is in volume production. If simulation of the FPGA design is done during development, special HardWire speed files may also be used for design verification. At that time, Xilinx makes a simple design check prior to generating the custom mask; then the HardWire prototypes are manufactured. An in-system verification is performed by the customer and the HardWire LCA is released to full production. As the architectures of the programmable FPGA device and the HardWire LCA are identical, virtually no engineering resources are needed to move from one to the other. By comparison, using a traditional masked gate array to attempt assembly of these logic functions from NAND gates to emulate the LCA device would require extensive design simulation and test development activity. A comparison of the activities required to convert to a HardWire LCA versus a standard gate array is shown in Figure 4.

Architectural Overview

The XC4300 family achieves high speed through advanced semiconductor technology and through improved architecture, and supports system clock rates of 60 to 70 MHz. Compared to older Xilinx FPGA families, the new family is more powerful, offering on-chip RAM and wide-input decoders. It is more versatile in its applications, and design cycles are faster due to a combination of increased routing resources and more sophisticated software. And last, but not least, it more than doubles the available complexity, up to the 10,000-gate level.

As shown in Figure 1, the HardWire LCA has the same architecture as the programmable FPGA device it replaces. The perimeter of I/O Blocks (IOBs) provides an interface between the internal logic array and the device package pins. The array of Configurable Logic Blocks (CLBs) performs user-specified logic functions. The interconnect resources are programmed to form networks carrying logic signals among blocks, analogous to printed-circuit-board traces connecting SSI/MSI packages.

The logic functions of the blocks are implemented by look-up tables. Functional options are implemented by user-defined multiplexers. Interconnecting networks between blocks are implemented with user-defined fixed metal connections.

I/O Block

Each user-defined IOB, shown in Figure 5, provides an interface between the external package pin and the internal user logic. It can be defined for input, output or bidirectional signals. The IOB is identical to that used in the programmable LCA device. There are a wide variety of I/O options available to the user.

Summary of I/O Options

Inputs

- Direct
- Latched/Registered
- Programmable pull-up/pull-down resistor

Outputs

- Direct/registered
- Inverted/not inverted
- 3-state/on/off
- Full speed/slew limited
- 3-state/output enable (inverse)

See *The XC4000 Data Book* for more details on IOB operation.

Configurable Logic Block

The array of Configurable Logic Blocks (CLBs) provides the functional elements from which the user's logic is constructed. The powerful and flexible XC4000/4300 CLB provides more capability than previous generations of LCA devices, resulting in more "effective gates per CLB." See Figure 6.

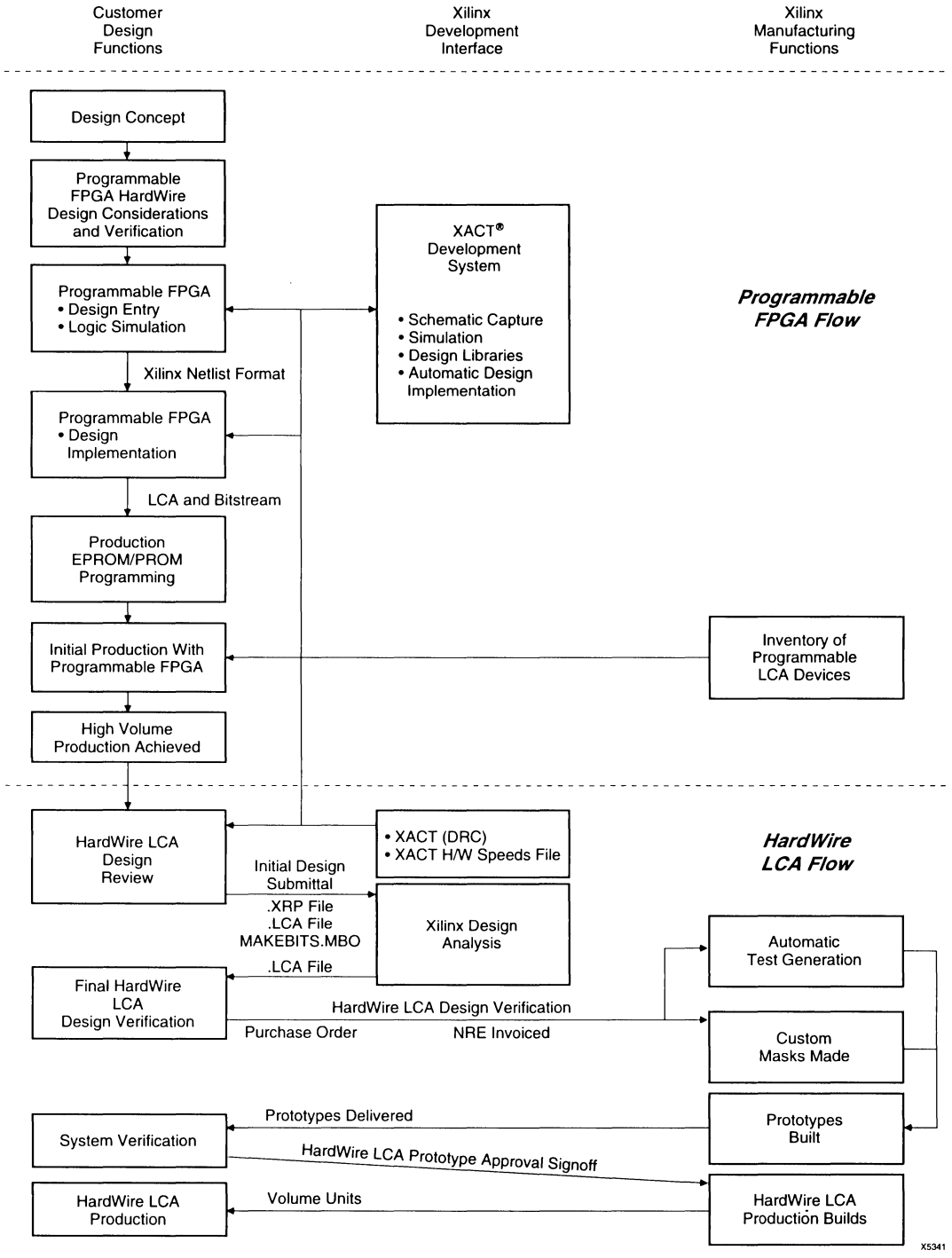


Figure 3. Programmable/HardWire Design/Production Interface.

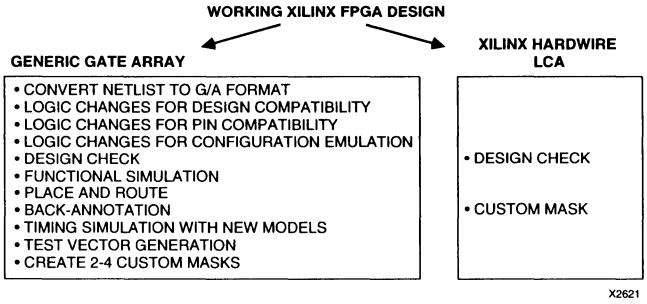


Figure 4. Design Conversion: HardWire LCA vs. Generic Gate Array.

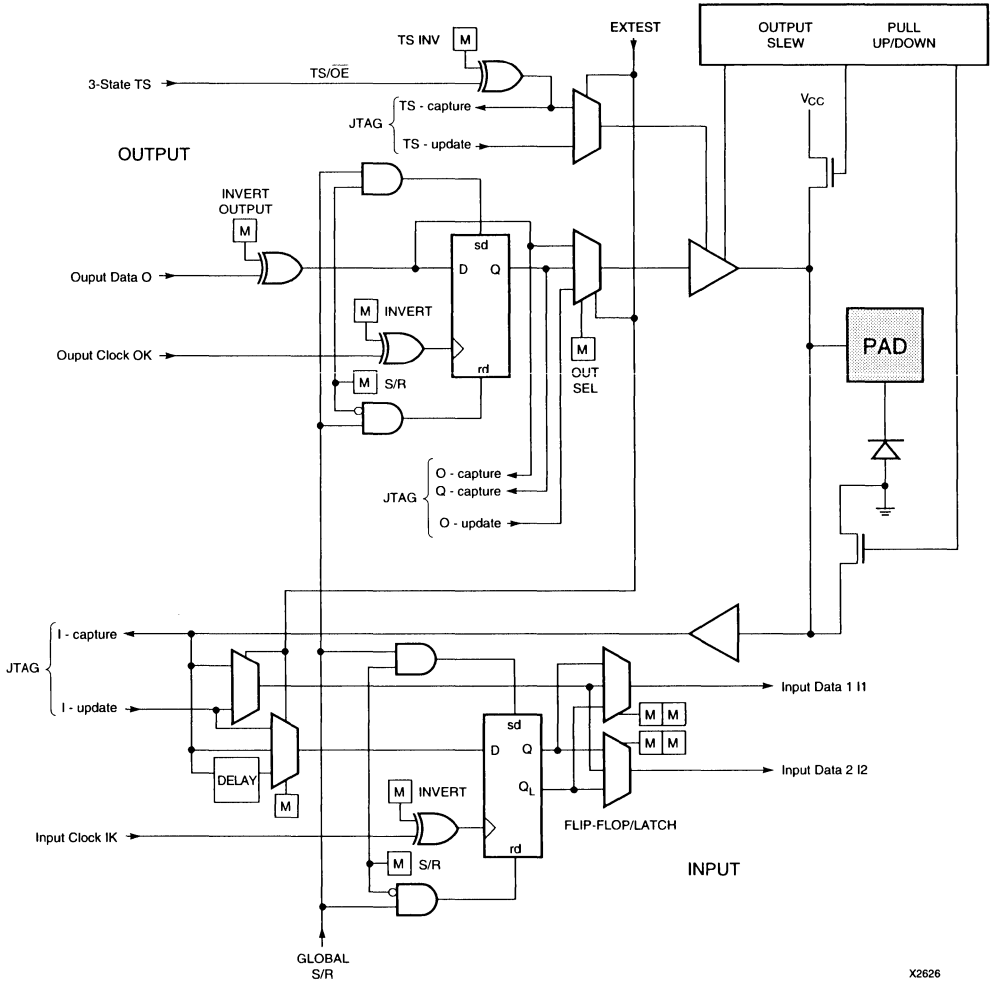


Figure 5. I/O Block

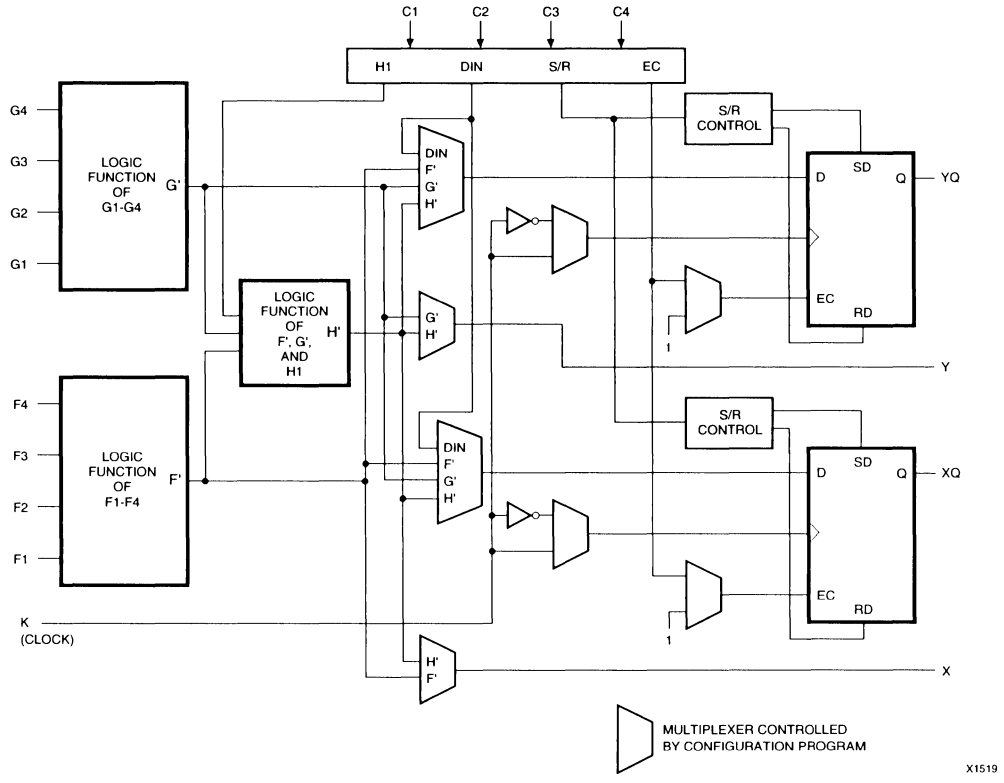


Figure 6. Simplified Block Diagram of XC4000 Configurable Logic Block

The XC4300 CLB is identical to that used in the XC4000 family of FPGA devices. Each CLB has two flip-flops and two independent 4-input function generators. A total of thirteen CLB inputs and four CLB outputs provide access to the function generators and flip-flops. These inputs and outputs connect to the user-defined fixed metal interconnects.

The versatility of the CLB function generators improves system speed significantly. In addition, the CLB can pass the combinatorial outputs to the interconnect network, and can also store the combinatorial results or other incoming data in one or two flip-flops, and connect their outputs to the interconnect network as well. The flip-flops can be used as registers or shift registers without blocking the function generators from performing a different, perhaps unrelated, task. This increases the functional density of the device.

See The *XC4000 Data Book* for more information on Configurable Logic Blocks.

Interconnect

User-defined interconnect resources in the LCA provide routing paths to connect inputs and outputs of the I/O and logic blocks into logic networks. Three types of metal interconnects are provided to accommodate various network-interconnect requirements:

- General purpose
- Direct connect
- LongLines.

The topology of all these interconnect resources is identical with that of the FPGA, but the speed of the interconnect paths is significantly faster, since all interconnections are fixed metal connections.

Architectural Enhancements

Compared to older LCA families, XC4300 HardWire LCAs provide significant enhancements. Powerful system features, as listed below, are incorporated to improve system speed, device flexibility, and ease of use.

- On-Chip Memory
  The XC4000/XC4300 family provides very fast on-chip RAM/ROM capability. Each CLB can be configured as

a small memory block that can be combined with as many other CLBs as desired. This reduces the cost of distributed memory dramatically.

- Wide Decoding
  The XC4300 family has 16 very fast programmable decoders located at the chip periphery, four on each chip edge. They accept I/O signals and internal signals as input and generate a very fast decoded output. This fast-decoding feature makes designing with FPGAs easier in many applications.

- Fast Carry Logic
  Each CLB includes high-speed carry logic. The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods, like carry generate/propagate, are meaningless even at the 16-bit level, and are of marginal benefit at the 32-bit level.

  The fast-carry logic opens the door to many new applications involving arithmetic operation where the previous generations of FPGAs were not fast or efficient enough. High-speed address offset calculations in microprocessors or graphics systems, and high-speed addition in digital-signal processing are two typical applications.

- JTAG Boundary Scan
  The XC4000/XC4300 family implements IEEE 1149.1 Boundary-scan methodology. This technique permits systems manufacturers to test their PC boards more safely, thoroughly, and efficiently, at significantly lower cost than using the traditional bed-of-nails test.

Configuration and Start-up

The XC4300 family of HardWire LCAs are designed to be fully compatible with their XC4000 programmable LCA-device equivalents. While the HardWire LCAs do not require the loading of configuration data, they support a wide variety of configuration modes.

Configuration

The XC4300 HardWire LCA can be used as a stand-alone device or in a daisy chain with other LCA or HardWire-LCA devices. It is designed to emulate the configuration sequence of the XC4000 LCA device for most configuration modes. The HardWire LCA cannot act as the first device in a daisy-chain in Master Parallel or Peripheral Mode; however it can operate downstream from an LCA device operating in these modes. Stand-alone LCA designs using these modes are also acceptable, since the HardWire LCA provides an "instant-on" option.

The "instant-on" option bypasses the normal configuration emulation sequence. This mode can also be used for systems where the normal configuration delay is not acceptable.

If "instant-on" is not selected, the user can select either the "bit-swallowing" or "no-data" option. With the bit-swallowing option, the device fully supports Serial Configuration Modes, and may be used anywhere in a daisy chain of LCA devices with no change to the configuration bitstream required. With the no-data option, the HardWire LCA does not "swallow" its own configuration data. Whatever bits are fed into the DIN pin will appear at the DOUT pin after a delay "TDIO". This mode is useful for a stand-alone HardWire LCA, or in a daisy chain where the designer wants to reduce the total number of required configuration bits.

Start-Up Sequence

The XC4300 HardWire LCAs are designed to emulate the start-up sequence of the FPGA devices as closely as possible, however, multiple options are available. The start-up sequence may be thought of as three stages: power-on-reset; internal clear; and configuration. There are three basic sequence options:

- Standard configuration
- Rapid reset
- Instant-on

Standard Configuration Sequence

An internal power-on reset circuit is triggered when power is applied. When V_{CC} reaches approximately 3 V, the device generates a POR (power-on reset) pulse. During the reset, the I/O output buffers are disabled and all inputs are pulled High. The POR pulse has a nominal delay of 22 ms. If the M0 pin is held Low during the POR cycle, (see chart) the POR pulse is extended to four times its nominal delay. This ensures that all daisy-chained slave devices will have sufficient time to power up.

Following the POR cycle, the HardWire LCA enters a "clearing" state. This state emulates the memory clear performed by a FPGA upon power-up. The length of the clear cycle is nominally 250 µs.

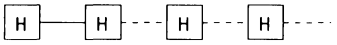
At the completion of the clear cycle the $\overline{\text{INIT}}$ pin is sampled. If the $\overline{\text{INIT}}$ pin is held Low, the "configuration" is delayed until $\overline{\text{INIT}}$ is driven High and the value of the Mode pins is latched. If the device is in Master Mode (see chart) it begins to produce CCLKs. If the device is in Slave Mode it requires CCLKs to be supplied from another device.

If "no-data" is chosen after four CCLK cycles the part is "configured" and the Done pin is released. (If the device is in a daisy chain with the DONE pins tied together the DONE pin will remain Low until all devices have completed configuration.)

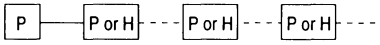
M0	M1	POR	CCLK
0	X	4X	Mstr
1	0	1X	Mstr
1	1	1X	Slv

Mode 1. As a stand alone HardWire LCA Device.

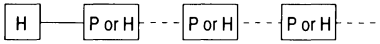
Mode 2. As a daisy chain of all HardWire LCA Devices.



Mode 3. As a HardWire LCA or programmable slave in a daisy chain with a Programmable device as a master.



Mode 4. As a HardWire LCA device acting as a Serial Master with any combination of Programmable and HardWire LCA devices as slaves.



(P = Programmable device, H = HardWire LCA device)

X5346

One CCLK after the DONE pin goes High the I/Os will become active. The internal global reset is user-defined to release either one CCLK cycle before or after the I/O pins become active. A HardWire LCA operating in Master Mode will stop producing CCLKs one cycle after the I/Os become active.

If "bit-swallowing" is chosen, the device will behave exactly like a serial mode XC4000. A complete bit stream is required to configure the LCA. The full range of start-up options offered by the XC4000 are available.

Rapid Reset

The rapid-reset cycle follows the same three stages as the standard configuration sequence, however the time delays are significantly reduced. The POR pulse is shortened and is nominally 1 µs. The clearing-state delay is also reduced to approximately 1 µs. Following the clearing state, the configuration stage is the same as for the standard configuration sequence.

Instant-On

When the Instant-On option is selected, the HardWire LCA has a short POR delay of nominally 1 µs. If the $\overline{\text{INIT}}$ pin is not held Low, the LCA goes active within an additional 1 µs. The DONE pin goes High, the I/Os become active, and the internal global set/reset signal goes inactive. Holding the $\overline{\text{INIT}}$ pin Low delays start-up until the $\overline{\text{INIT}}$ pin is released, at which time the device goes active within 1 µs. The CCLK pin is disabled during the entire power-up and start-up sequence.

Performance

The XC4300 family of HardWire LCAs are manufactured using the same high-performance 0.8 µ CMOS technology as the programmable-LCA device equivalents. Compared to the previous-generation 1.2-µ-process technology, this technology provides approximately a 25% improvement in performance, even before any architectural improvements are taken into account.

Actual LCA performance is determined by the timing of critical paths, including the timing for the logic and storage elements in that path and the timing of the associated interconnect. HardWire LCA logic-block performance is equal to or slightly faster than the equivalent FPGA performance, while the interconnect performance is significantly faster.

All HardWire LCAs are specified and tested for operation at the fastest equivalent FPGA speed available at the time the HardWire device is introduced. For the XC4300 family, this means all parts are guaranteed to the -4 speed grade. Since the finished HardWire product is customized for a specific customer and application, speed grading is not available.

Power

Power for the HardWire LCA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the device, dedicated V_{CC} and ground rings surround the logic array and provide power to the I/O drivers. An independent matrix of V_{CC} and ground lines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically a 0.1-µF capacitor connected near the V_{CC} and ground pins will provide adequate decoupling.

Output buffers capable of driving the specified 12-mA/24-mA loads under worst-case conditions may be capable of driving many times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads. The I/O Block output buffers have a slew-limited mode which should be used where output rise and fall times are not speed critical. Slew-limited outputs maintain their dc drive capability, but generate less external reflections and internal noise. A maximum total external capacitive load for simultaneous fast-mode switching in the same direction is 200 pF per power/ground pin pair. For slew-rate limited outputs this total is four times larger.

HardWire LCA Design Considerations

It is important to observe good design practices while using HardWire LCAs. It is possible for a programmable device to "hide" some less obvious design shortcomings. However, these can manifest themselves when the design is converted to a HardWire LCA.

For example, a small glitch generated from unstable inputs to a CLB function block can be easily "swallowed" if the output is driving a long net. This is because the "pass transistors" act as a Low pass filter and this net's loads may never see the glitch. However, in a HardWire LCA, the glitch may propagate to the loads since there are only metal lines and vias in the routing path.

Gated Clocks and Reset Directs

Glitching function generators driving CLOCK and RESET DIRECT pins can inadvertently trigger flip-flops to an undesirable state. Avoid these so-called "gated" clock and reset direct nets; if unavoidable, design the logic so that the inputs are always stable and the signal changes are at least a CLB delay (T_{ILO}) apart.

Multiplexers Implemented in Function Generators

Two input multiplexers can be easily implemented in a single F or G function generator. However, there is a possibility of a glitch if the selected signal and the selected input changes within a CLB's Tilo delay. This is generally not a problem with data and address multiplexers as long as the output is given enough time to settle; but if the multiplexer output is feeding a CLOCK and/or a RESET DIRECT pin, it is possible to toggle the register at undesired times.

The edge(s) of select signals for a CLOCK and/or RESET DIRECT multiplexers should be stable before and after the edges of the inputs. The edges should be at least a CLB (T_{ILO}) delay apart.

Race Conditions

All race conditions in the circuit need to go through a careful analysis. Depending on the routing resources responsible for the net delays, the correct signal may always "win the race" in a programmable FPGA; however, once converted to HardWire LCA, this may not be the case. (See Figure 8.)

Delay Generators

Using the routing resources as delay lines in programmable FPGAs is undesirable. In HardWire LCAs, it is an invitation for timing problems. All delay generators should be removed and the circuit redesigned before converting it to HardWire.

Interfacing with External Devices

Almost all LCAs interface with external devices–FIFOs, memories, processors and peripherals, etc. Handshaking with devices requires specific setup/hold times. Ample hold time on a data bus from a programmable FPGA may no longer meet spec in HardWire LCA. An external data bus clocked by a HardWire LCA generated signal may no longer meet the system set-up time requirements. This can happen because interconnects are much faster than in a programmable device. This requires system timing specs to be reviewed when converting to a HardWire LCA.

In reality, all designers using LCAs (programmable or HardWire) face the same issues. Due to improvements in process and circuit design, a part specified at -6 today may actually be running as fast as -5 or even close to -4 in the future. Xilinx does NOT guarantee a part against minimum timing specs. A "glitch" that was swallowed in a device today may crop up in a future device due to faster pass transistors in the routing paths. When using any Xilinx LCAs, the above issues should be addressed in the design phase.

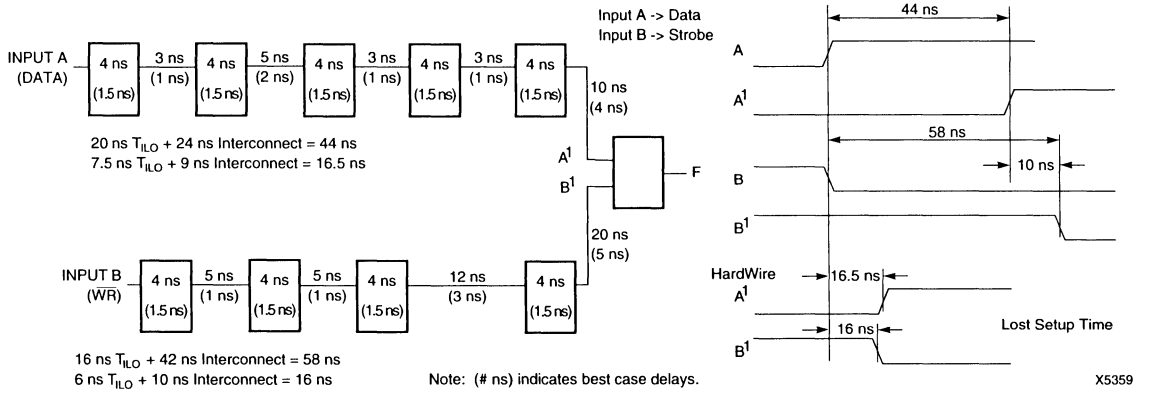


Figure 8. Race Condition Example

XC4000/XC4300-Family Pin Assignments

Xilinx offers members of the XC4300 family in a variety of surface-mount and through-hole package types, with pin counts from 84 to 225.

Each chip is offered in several package types to accommodate the available PC-board space and manufacturing technology. Most package types are also offered with different chips to accommodate design changes without requiring PC-board changes.

Pin Descriptions

Permanently Dedicated Pins.

V_{CC}
Eight or more (depending on package type) connections to the nominal +5 V supply voltage. All must be connected.

GND
Eight or more (depending on package type) connections to ground. All must be connected.

CCLK
During configuration, Configuration Clock is an output of a HardWire gate array in Master mode, or an input in Slave mode.

After configuration, an internal pull-up maintains a High when the pin is not being driven.

DONE
This is a bidirectional signal with an optional pull-up resistor. As an output, it indicates the completion of the configuration process. The configuration mode determines the exact timing, the clock source for the Low-to High transition, and the enable status of the pull-up resistor.

As an input, DONE can be configured to delay the global initialization, or to enable the outputs.

$\overline{\text{PROGRAM}}$
This is an active-Low input that forces the HardWire LCA to return to the "memory clear" stage of the start-up sequence. When PROGRAM goes High, the device finishes the current clear cycle and executes another complete clear cycle, before it goes into a WAIT state and releases INIT.

User I/O Pins that can have special functions.

M0, M1
As Mode inputs, these pins are sampled before the start of configuration to determine the configuration mode to be used.

After configuration, M0 and M2 can be used as inputs, and M1 can be used as a 3-state output. These three pins have no associated input or output registers.

These pins can be user inputs or outputs only when called out by special schematic definitions.

TDO
If boundary scan is used, this is the Test Data output. If boundary scan is not used, this pin is a 3-state output without a register, after configuration is completed.

This pin can be a user output only when called out by special schematic definitions.

TDI, TCK, TMS
If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively, coming directly from the pads and bypassing the IOBs. These pins can also be used as inputs to the CLB logic after configuration is completed.

If the boundary-scan option is not selected, all boundary-scan functions are inhibited once configuration is completed; these pins then become user-programmable I/O.

HDC
During configuration, this output is held at a High level to indicate that configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin.

$\overline{\text{LDC}}$
During configuration, this output is held at a Low level to indicate that the configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin.

$\overline{\text{INIT}}$
Before and during configuration, this is a bidirectional signal. An external pull-up resistor is recommended.

INIT is an active-Low open-drain output that is held Low during the Power-On Reset cycle and during the clearing state of the start-up sequence. It can be used to hold the device in the internal WAIT state before the start of configuration.

During configuration, a Low on this output indicates that a configuration-data error has occurred. After configuration, this is a user-programmable I/O.

PGCK1 - PGCK4
Each of four Primary Global inputs drives a dedicated internal global net with short delay and minimal skew. If not used for this purpose, any of these pins can be used as a user-programmable I/O.

SGCK1 - SGCK4
Each of four Secondary Global inputs can drive a dedicated internal global net that alternatively can also be driven from internal logic.

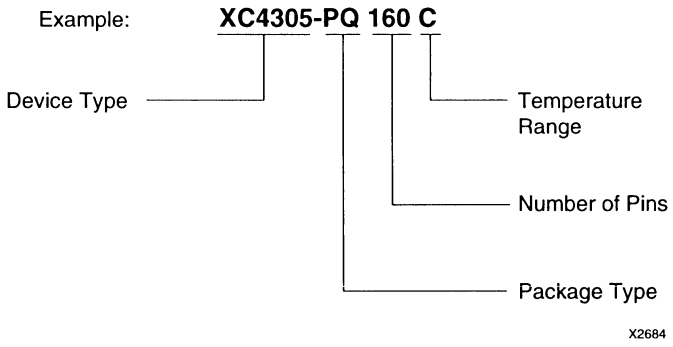
DIN
During Slave or Master Serial configuration, this pin is used as a serial-data input. After configuration, DIN is a user-programmable I/O pin.

DOUT
During configuration, this pin is used to output serial-configuration data to the DIN pin of a daisy-chained slave.DOUT data changes on the falling edge of CCLK, one-and-a-half CCLK periods after it was received at the DIN input. After configuration, DOUT is a user-programmable I/O pin.

Unrestricted User-Programmable I/O Pins.
I/O
An I/O pin may be programmed by the user to be an Input or an Output pin following configuration. Before configuration is completed, these pins have an internal high-value pull-up resistor that defines the logic level as High.

For a discussion on device testability, see the XC3330A/L and XC3400 Datasheets.

Ordering Information



XC4303 Pinouts

Pin Description	PC84	PQ100	Bound Scan
VCC	2	92	–
I/O (A8)	3	93	32
I/O (A9)	4	94	35
I/O	–	95	38
I/O	–	96	41
I/O (A10)	5	97	44
I/O (A11)	6	98	47
–	–	–	–
I/O (A12)	7	99	50
I/O (A13)	8	100	53
–	–	–	–
–	–	–	–
I/O (A14)	9	1	56
SGCK1 (A15,I/O)	10	2	59
VCC	11	3	–
GND	12	4	–
PGCK1 (A16, I/O)	13	5	62
I/O (A17)	14	6	65
–	–	–	–
–	–	–	–
I/O (TDI)	15	7	68
I/O (TCK)	16	8	71
–	–	–	–
I/O (TMS)	17	9	74
I/O	18	10	77
I/O	–	–	80
I/O	–	11	83
I/O	19	12	86
I/O	20	13	89
GND	21	14	–
VCC	22	15	–
I/O	23	16	92
I/O	24	17	95
I/O	–	18	98
I/O	–	–	101
I/O	25	19	104
I/O	26	20	107
I/O	27	21	110
I/O	–	22	113
–	–	–	–
I/O	28	23	116
SGCK2 (I/O)	29	24	119
O (M1)	30	25	122
GND	31	26	–
I (M0)	32	27	125†
VCC	33	28	–
I (M2)	34	29	126†
PGCK2 (I/O)	35	30	127
I/O (HDC)	36	31	130
–	–	–	–
–	–	–	–
I/O	–	32	133
I/O (LDC)	37	33	136
I/O	38	34	139
I/O	39	35	142
I/O	–	36	145
I/O	–	37	148
I/O	40	38	151
I/O (ERR, INIT)	41	39	154
VCC	42	40	–

Pin Description	PC84	PQ100	Bound Scan
GND	43	41	–
I/O	44	42	157
I/O	45	43	160
I/O	–	44	163
I/O	–	45	166
I/O	46	46	169
I/O	47	47	172
I/O	48	48	175
I/O	49	49	178
–	–	–	–
–	–	–	–
I/O	50	50	181
SGCK3 (I/O)	51	51	184
GND	52	52	–
DONE	53	53	–
VCC	54	54	–
PROG	55	55	–
I/O (D7)	56	56	187
PGCK3 (I/O)	57	57	190
–	–	–	–
–	–	–	–
I/O (D6)	58	58	193
I/O	–	59	196
I/O (D5)	59	60	199
I/O (CS0)	60	61	202
I/O	–	62	205
I/O	–	63	208
I/O (D4)	61	64	211
I/O	62	65	214
VCC	63	66	–
GND	64	67	–
I/O (D3)	65	68	217
I/O (RS)	66	69	220
I/O	–	70	223
I/O	–	–	226
I/O (D2)	67	71	229
I/O	68	72	232
I/O (D1)	69	73	235
I/O (RCLK-BUSY/RDY)	70	74	238
–	–	–	–
–	–	–	–
I/O (D0, DIN)	71	75	241
SGCK4 (DOUT, I/O)	72	76	244
CCLK	73	77	–
VCC	74	78	–
O (TDO)	75	79	–
GND	76	80	–
I/O (A0, WS)	77	81	2
PGCK4 (A1, I/O)	78	82	5
–	–	–	–
–	–	–	–
I/O (CS1, A2)	79	83	8
I/O (A3)	80	84	11
I/O (A4)	81	85	14
I/O (A5)	82	86	17
I/O	–	87	20
I/O	–	88	23
I/O (A6)	83	89	26
I/O (A7)	84	90	29
GND	1	91	–

* Indicates unconnected package pins.
† Contributes only one bit (.i) to the boundary scan register.
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 247 = BSCANT.UPD

XC4305 Pinouts

Pin Description	PC84	PQ160	PQ208	Bound Scan
VCC	2	142	183	–
I/O (A8)	3	143	184	44
I/O (A9)	4	144	185	47
I/O	–	145	186	50
I/O	–	146	187	53
–	–	–	188*	–
–	–	–	189*	–
I/O (A10)	5	147	190	56
I/O (A11)	6	148	191	59
I/O	–	149	192	62
I/O	–	150	193	65
GND	–	151	194	–
–	–	–	195*	–
–	–	–	196*	–
–	–	152*	197*	–
–	–	153*	198*	–
I/O (A12)	7	154	199	68
I/O (A13)	8	155	200	71
–	–	–	–	–
I/O	–	156	201	74
I/O	–	157	202	77
I/O (A14)	9	158	203	80
SGCK1 (A15, I/O)	10	159	204	83
VCC	11	160	205	–
–	–	–	206*	–
–	–	–	207*	–
–	–	–	208*	–
–	–	–	1*	–
GND	12	1	2	–
–	–	–	3*	–
PGCK1 (A16, I/O)	13	2	4	86
I/O (A17)	14	3	5	89
I/O	–	4	6	92
I/O	–	5	7	95
–	–	–	–	–
I/O (TDI)	15	6	8	98
I/O (TCK)	16	7	9	101
–	–	8*	10*	–
–	–	9*	11*	–
–	–	–	12*	–
–	–	–	13*	–
GND	–	10	14	–
I/O	–	11	15	104
I/O	–	12	16	107
I/O (TMS)	17	13	17	110
I/O	18	14	18	113
–	–	–	19*	–
–	–	–	20*	–
I/O	–	15	21	116
I/O	–	16	22	119
I/O	19	17	23	122
I/O	20	18	24	125
GND	21	19	25	–
VCC	22	20	26	–
I/O	23	21	27	128
I/O	24	22	28	131
I/O	–	23	29	134
I/O	–	24	30	137
–	–	–	31*	–
–	–	–	32*	–
I/O	25	25	33	140
I/O	26	26	34	143
I/O	–	27	35	146
I/O	–	28	36	149
GND	–	29	37	–
–	–	–	38*	–
–	–	–	39*	–
–	–	30*	40*	–
–	–	31*	41*	–
I/O	27	32	42	152
I/O	–	33	43	155
I/O	–	34	44	158

Pin Description	PC84	PQ160	PQ208	Bound Scan
I/O	–	35	45	161
–	–	–	–	–
I/O	28	36	46	164
SGCK2 (I/O)	29	37	47	167
O (M1)	30	38	48	170
GND	31	39	49	–
I (M0)	32	40	50	173†
–	–	–	51*	–
–	–	–	52*	–
–	–	–	53*	–
–	–	–	54*	–
VCC	33	41	55	–
I (M2)	34	42	56	174†
PGCK2 (I/O)	35	43	57	175
I/O (HDC)	36	44	58	178
I/O	–	45	59	181
–	–	–	–	–
I/O	–	46	60	184
I/O	–	47	61	187
I/O (LDC)	37	48	62	190
–	–	49*	63*	–
–	–	50*	64*	–
–	–	–	65*	–
–	–	–	66*	–
GND	–	51	67	–
I/O	–	52	68	193
I/O	–	53	69	196
I/O	38	54	70	199
I/O	39	55	71	202
–	–	–	72*	–
–	–	–	73*	–
I/O	–	56	74	205
I/O	–	57	75	208
I/O	40	58	76	211
I/O (ERR, INIT)	41	59	77	214
VCC	42	60	78	–
GND	43	61	79	–
I/O	44	62	80	217
I/O	45	63	81	220
I/O	–	64	82	223
I/O	–	65	83	226
–	–	–	84*	–
–	–	–	85*	–
I/O	46	66	86	229
I/O	47	67	87	232
I/O	–	68	88	235
I/O	–	69	89	238
GND	–	70	90	–
–	–	–	91*	–
–	–	–	92*	–
–	–	71*	93*	–
–	–	72*	94*	–
I/O	48	73	95	241
I/O	49	74	96	244
I/O	–	75	97	247
I/O	–	76	98	250
I/O	50	77	99	253
SGCK3 (I/O)	51	78	100	256
GND	52	79	101	–
–	–	–	102*	–
DONE	53	80	103	–
–	–	–	104*	–
–	–	–	105*	–
VCC	54	81	106	–
–	–	–	107*	–
PROG	55	82	108	–
I/O (D7)	56	83	109	259
PGCK3 (I/O)	57	84	110	262
I/O	–	85	111	265
–	–	–	–	–
I/O	–	86	112	268
I/O (D6)	58	87	113	271

Pin Description	PC84	PQ160	PQ208	Bound Scan
I/O	–	88	114	274
–	–	89*	115*	–
–	–	89*	115*	–
–	–	90†	116*	–
–	–	–	117*	–
–	–	–	118*	–
GND	–	91	119	–
I/O	–	92	120	277
I/O	–	93	121	280
I/O (D5)	59	94	122	283
I/O (CS0)	60	95	123	286
–	–	–	124*	–
–	–	–	125*	–
I/O	–	96	126	289
I/O	–	97	127	292
I/O (D4)	61	98	128	295
I/O	62	99	129	298
VCC	63	100	130	–
GND	64	101	131	–
I/O (D3)	65	102	132	301
I/O (RS)	66	103	133	304
I/O	–	104	134	307
I/O	–	105	135	310
–	–	–	136*	–
–	–	–	137*	–
I/O (D2)	67	106	138	313
I/O	68	107	139	316
I/O	–	108	140	319
I/O	–	109	141	322
GND	–	110	142	–
–	–	–	143*	–
–	–	–	144*	–
–	–	111*	145*	–
–	–	112*	146*	–
I/O (D1)	69	113	147	325
I/O (RCLK-BUSY/RDY)	70	114	148	328
I/O	–	115	149	331
–	–	–	–	–
I/O	–	116	150	334
I/O (D0, DIN)	71	117	151	337
SGCK4 (DOUT, I/O)	72	118	152	340
CCLK	73	119	153	–
VCC	74	120	154	–
–	–	–	155*	–
–	–	–	156*	–
–	–	–	157*	–
–	–	–	158*	–
O (TDO)	75	121	159	–
GND	76	122	160	–
I/O (A0,WS)	77	123	161	2
PGCK4 (A1,I/O)	78	124	162	5
I/O	–	125	163	8
–	–	–	–	–
I/O	–	126	164	11
I/O (CS1,A2)	79	127	165	14
I/O (A3)	80	128	166	17
–	–	129*	167*	–
–	–	130*	168*	–
–	–	–	169*	–
–	–	–	170*	–
GND	–	131	171	–
I/O	–	132	172	20
I/O	–	133	173	23
I/O (A4)	81	134	174	26
I/O (A5)	82	135	175	29
–	–	–	176*	–
–	–	136*	177*	–
I/O	–	137	178	32
I/O	–	138	179	35
I/O (A6)	83	139	180	38
I/O (A7)	84	140	181	41
GND	1	141	182	–

* Indicates unconnected package pins.

Boundary Scan Bit 0 = TDO.T

XC4310 Pinouts

Pin Description	PQ160	PG191	PQ208	Boundary Scan Order
VCC	142	J4	183	-
I/O (A8)	143	J3	184	62
I/O (A9)	144	J2	185	65
I/O	145	J1	186	68
I/O	146	H1	187	71
I/O	-	H2	188	74
I/O	-	H3	189	77
I/O (A10)	147	G1	190	80
I/O (A11)	148	G2	191	83
I/O	149	F1	192	86
I/O	150	E1	193	89
GND	151	G3	194	-
I/O	-	F2	195	92
I/O	-	D1	196	96
I/O	152	C1	197	98
I/O	153	E2	198	101
I/O (A12)	154	F3	199	104
I/O (A13)	155	D2	200	107
I/O	156	B1	201	110
I/O	157	E3	202	113
I/O (A14)	158	C2	203	116
SGCK1 (A15, I/O)	159	B2	204	119
VCC	160	D3	205	-
-	-	-	206*	-
-	-	-	207*	-
-	-	-	208*	-
-	-	-	1*	-
GND	1	D4	2	-
-	-	-	3*	-
PGCK1 (A16, I/O)	2	C3	4	122
I/O (A17)	3	C4	5	125
I/O	4	B3	6	128
I/O	5	C5	7	131
I/O (TDI)	6	A2	8	134
I/O (TCK)	7	B4	9	137
I/O	8	C6	10	140
I/O	9	A3	11	143
I/O	-	B5	12	146
I/O	-	B6	13	149
GND	10	C7	14	-
I/O	11	A4	15	152
I/O	12	A5	16	155
I/O (TMS)	13	B7	17	158
I/O	14	A6	18	161
I/O	-	C8	19	164
I/O	-	A7	20	167
I/O	15	B8	21	170
I/O	16	A8	22	173
I/O	17	B9	23	176
I/O	18	C9	24	179
GND	19	D9	25	-
VCC	20	D10	26	-
I/O	21	C10	27	182
I/O	22	B10	28	185
I/O	23	A9	29	188

Pin Description	PQ160	PG191	PQ208	Boundary Scan Order
I/O	24	A10	30	191
I/O	-	A11	31	194
I/O	-	C11	32	197
I/O	25	B11	33	200
I/O	26	A12	34	203
I/O	27	B12	35	206
I/O	28	A13	36	209
GND	29	C12	37	-
I/O	-	B13	38	212
I/O	-	A14	39	215
I/O	30	A15	40	218
I/O	31	C13	41	221
I/O	32	B14	42	224
I/O	33	A16	43	227
I/O	34	B15	44	230
I/O	35	C14	45	233
I/O	36	A17	46	236
SGCK2 (I/O)	37	B16	47	239
M1	38	C15	48	242
GND	39	D15	49	-
M0	40	A18	50	245†
-	-	-	51*	-
-	-	-	52*	-
-	-	-	53*	-
-	-	-	54*	-
VCC	41	D16	55	-
M2	42	C16	56	246†
PGCK2 (I/O)	43	B17	57	247
I/O (HDC)	44	E16	58	250
I/O	45	C17	59	253
I/O	46	D17	60	256
I/O	47	B18	61	259
I/O (LDC)	48	E17	62	262
I/O	49	F16	63	265
I/O	50	C18	64	268
I/O	-	D18	65	271
I/O	-	F17	66	274
GND	51	G16	67	-
I/O	52	E18	68	277
I/O	53	F18	69	280
I/O	54	G17	70	283
I/O	55	G18	71	286
I/O	-	H16	72	289
I/O	-	H17	73	291
I/O	56	H18	74	295
I/O	57	J18	75	298
I/O	58	J17	76	301
I/O ($\overline{ERR}$, $\overline{INIT}$)	59	J16	77	304
VCC	60	J15	78	-
GND	61	K15	79	-
I/O	62	K16	80	307
I/O	63	K17	81	310
I/O	64	K18	82	313
I/O	65	L18	83	316
I/O	-	L17	84	319
I/O	-	L16	85	322
I/O	66	M18	86	325

* Indicates unconnected package pins.

† Contributes only one bit (.i) to the boundary scan register.

XC4310 Pinouts

Pin Description	PQ160	PG191	PQ208	Boundary Scan Order
I/O	67	M17	87	328
I/O	68	N18	88	331
I/O	69	P18	89	334
GND	70	M16	90	-
I/O	-	N17	91	337
I/O	-	R18	92	340
I/O	71	T18	93	343
I/O	72	P17	94	346
I/O	73	N16	95	349
I/O	74	T17	96	352
I/O	75	R17	97	355
I/O	76	P16	98	358
I/O	77	U18	99	361
SGCK3 (I/O)	78	T16	100	364
GND	79	R16	101	-
-	-	-	102*	-
DONE	80	U17	103	-
-	-	-	104*	-
-	-	-	105*	-
VCC	81	R15	106	-
-	-	-	107*	-
$\overline{\text{PROG}}$	82	V18	108	-
I/O (D7)	83	T15	109	367
PGCK3 (I/O)	84	U16	110	370
I/O	85	T14	111	373
I/O	86	U15	112	376
I/O (D6)	87	V17	113	379
I/O	88	V16	114	382
I/O	89	T13	115	385
I/O	90	U14	116	388
I/O	-	V15	117	391
I/O	-	V14	118	394
GND	91	T12	119	-
I/O	92	U13	120	397
I/O	93	V13	121	400
I/O (D5)	94	U12	122	403
I/O ($\overline{\text{CSO}}$)	95	V12	123	406
I/O	-	T11	124	409
I/O	-	U11	125	412
I/O	96	V11	126	415
I/O	97	V10	127	418
I/O (D4)	98	U10	128	421
I/O	99	T10	129	424
VCC	100	R10	130	-
GND	101	R9	131	-
I/O (D3)	102	T9	132	427
I/O ($\overline{\text{RS}}$)	103	U9	133	430
I/O	104	V9	134	433
I/O	105	V8	135	436
I/O	-	U8	136	439
I/O	-	T8	137	442
I/O (D2)	106	V7	138	445
I/O	107	U7	139	448
I/O	108	V6	140	451
I/O	109	U6	141	454
GND	110	T7	142	-
I/O	-	V5	143	457

* Indicates unconnected package pins.

Pin Description	PQ160	PG191	PQ208	Boundary Scan Order
I/O	-	V4	144	460
I/O	111	U5	145	463
I/O	112	T6	146	466
I/O (D1)	113	V3	147	469
I/O ($\overline{\text{RCLK}}$-$\overline{\text{BUSY}}$/RDY)	114	V2	148	472
I/O	115	U4	149	475
I/O	116	T5	150	478
I/O (D0, DIN)	117	U3	151	481
SGCK4 (I/O)	118	T4	152	484
CCLK	119	V1	153	-
VCC	120	R4	154	-
-	-	-	155*	-
-	-	-	156*	-
-	-	-	157*	-
-	-	-	158*	-
TDO	121	U2	159	-
GND	122	R3	160	-
I/O (A0, $\overline{\text{WS}}$)	123	T3	161	2
PGCK4 (I/O, A1)	124	U1	162	5
I/O	125	P3	163	8
I/O	126	R2	164	11
I/O (CS1, A2)	127	T2	165	14
I/O (A3)	128	N3	166	17
I/O	129	P2	167	20
I/O	130	T1	168	23
I/O	-	R1	169	26
I/O	-	N2	170	29
GND	131	M3	171	-
I/O	132	P1	172	32
I/O	133	N1	173	35
I/O (A4)	134	M2	174	38
I/O (A5)	135	M1	175	41
I/O	-	L3	176	44
I/O	136	L2	177	47
I/O	137	L1	178	50
I/O	138	K1	179	53
I/O (A6)	139	K2	180	56
I/O (A7)	140	K3	181	59
GND	141	K4	182	-

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 487 = BSCAN.UPD

XC3300A, XC3300L, XC3400A HardWire™ LCA Families

Preliminary

Product Specification

Features

- Mask-programmed versions of Xilinx Programmable Logic Cell Arrays (LCA) XC3000A, XC3000L, XC3100, XC3100A
  - Cost reduction for high volume applications
  - Transparent conversion from FPGA device
  - IEEE 1149.1-compatible boundry scan logic support
  - On-chip scan path test latches
  - High performance 0.8 µ CMOS process
- Easy conversion from Programmable FPGA
  - Architecturally identical to Programmable FPGA
  - Fully pin and performance compatible
  - Same specifications as Programmable FPGA
  - Supports daisy-chained configuration modes
  - Test program automatically generated
  - Emulates Programmable Configuration Signals
- Advanced Second Generation Architecture
  - Compatible arrays up to 9000 gate complexity
  - Extensive register, combinational and I/O capabilities
  - High fan-out signal distribution, low-slew clock
  - Internal 3-state bus capabilities
  - On-chip crystal oscillator amplifier

Description

The Xilinx Logic Cell Array (LCA) family provides a group of high-performance, high-density digital integrated circuits. Their regular, extendable, flexible architecture is composed of three types of configurable elements: a perimeter of IOBs, a core array of CLBs and circuitry for interconnection. The general structure of a LCA device is shown in Figure 1.

The Xilinx XC3300A/L/XC3400A family of HardWire LCAs are mask programmed versions of the Xilinx XC3000A/L/XC3100A FPGAs. In high-volume applications where the design is stable, the programmable FPGAs used for prototyping and initial production can be replaced by their HardWire LCA equivalents. This offers a significant cost reduction with virtually no risk or engineering resources required.

In a Programmable FPGA the logic functions and interconnections are determined by the configuration program data loaded and stored in internal static memory cells. The HardWire LCA has architecture identical to the Programmable FPGA it replaces. All CLBs, IOBs, interconnect topology, power distribution and other elements are the same. In the HardWire LCA the memory cells and the logic they control are replaced by metal connections. Thus the HardWire LCA is a semicustom device manufactured to provide a customer specific function, yet is completely compatible with the FPGA it replaces.

HardWire Device	Replacement for Pin-Compatible Programmable Device	Maximum Speed Grade for HardWire Conversion*	File Submitted to Xilinx	Packages												
					PLCC			TQFP/VQFP				PQFP			PPGA	
				Number of Pins	44	68	84	64	100	144	176	100	160	208	132	175
XC3330A	XC3020A, XC3030A	-6	XC3030A.LCA	Number of I/Os	34	58	74	54	80	-	-	80	-	-	-	-
XC3330L	XC3020L, XC3030L	-8	XC3030L.LCA		34	58	74	54	80	-	-	-	-	-	-	-
XC3342A	XC3042A	-6	XC3042A.LCA		-	-	74	-	82	120	-	82	-	-	-	-
XC3342L	XC3042L	-8	XC3042L.LCA		-	-	74	-	82	120	-	-	-	-	-	-
XC3390A	XC3064A, XC3090A	-6	XC3090A.LCA		-	-	70	-	-	120	144	-	138	144	110	144
XC3390L	XC3064L, XC3090L	-8	XC3090L.LCA		-	-	70	-	-	120	144	-	-	-	-	-
XC3430A	XC3120, XC3130	-3	XC3130.LCA		34	58	74	54	80	-	-	80	-	-	-	-
	XC3120A, XC3130A	-3	XC3130A.LCA													
XC3442A	XC3142	-3	XC3142.LCA		-	-	74	-	82	120	-	82	-	-	-	-
	XC3142A	-3	XC3142A.LCA													
XC3490A	XC3164, XC3190	-3	XC3190.LCA		-	-	70	-	-	120	144	-	138	144	110	144
	XC3164A, XC3190A	-3	XC3190A.LCA													

- FPGA and HardWire Device not available in this package

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* Consult factory for information if faster speed grades are required.

Xilinx manufactures the HardWire LCA using the information from the FPGA design file. Since the HardWire LCA device is both pinout and architecturally identical with the FPGA it is easily created without the need for all the costly and time-consuming engineering activities which other semicustom solutions would require. No redesign time; no expensive and time consuming simulation runs; no place and route; no test vector generation. The combination of the Programmable LCA and HardWire LCA products simply offer the fastest and easiest way to get your product to market, and ensures a subsequent low-cost, low-risk high-volume cost reduction path.

Electrical Characteristics

The XC3300A, XC3300L and XC3400A HardWire LCA families are form, fit and function compatible with the XC3000/XC3100 FPGA families. Accordingly, all XC3300A, XC3300L and XC3400A HardWire devices meet the electrical specifications of the respective XC3000/XC3100 FPGA device for the Speed Grade shown in the selection table on page 2-29. For specific data, please see the XC3000/XC3100 sections of the Xilinx Programmable Logic Data Book. Absolute Maximum Ratings, Operating Conditions, DC Characteristics and Switching Characteristics of the appropriate device type apply.

Architecture

As shown in Figure 1, the HardWire LCA has the same architecture as the FPGA it replaces. The perimeter of I/O Blocks (IOBs) provides an interface between the internal logic array and the device package pins. The array of Configurable Logic Blocks (CLBs) performs user-specified logic functions. The interconnect resources are programmed to form networks carrying logic signals among blocks, analogous to printed circuit board traces connecting SSI/MSI packages.

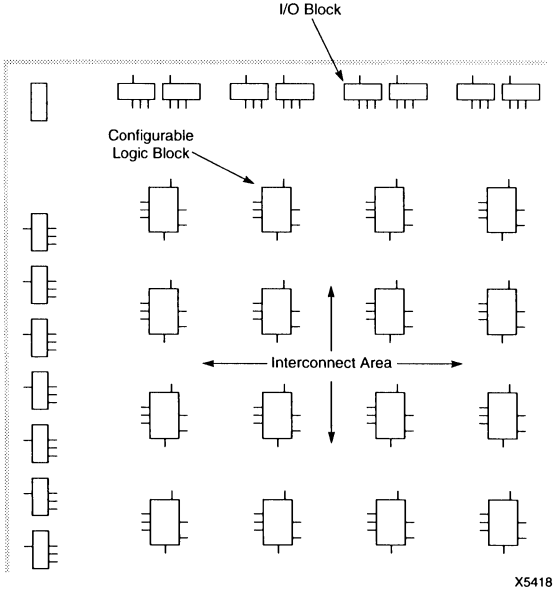


Figure 1. Logic Cell Array Structure

The logic functions of the blocks are implemented by look-up tables. Functional options are implemented by user-defined multiplexers. Interconnecting networks between blocks are implemented with user-defined fixed metal connections.

I/O Block

Each user-defined IOB (shown in Figure 2) provides an interface between the external package pin of the device and the internal user logic. The IOB is identical with that used in the FPGA. There are a wide variety of I/O options available to the user.

Summary of I/O Options

- Inputs
  - Direct
  - Flip-flop/latch
  - CMOS/TTL threshold (chip inputs)
  - Pull-up resistor/open circuit
- Outputs
  - Direct/registered
  - Inverted/not
  - 3-state/on/off
  - Full speed/slew limited
  - 3-state/output enable (inverse)

Configurable Logic Block

The array of Configurable Logic Blocks (CLBs) provides the functional elements from which the user's logic is constructed. The logic blocks are arranged in a matrix within the perimeter of IOBs. For example, the XC3330A/L has 100 such blocks arranged in 10 rows and 10 columns.

The configurable logic block is identical to that used in the XC3000A/L family of FPGAs. Each configurable logic block has a combinatorial logic section, two flip-flops, and an internal control section. (See Figure 3.) There are: five logic inputs [*.a*, *.b*, *.c*, *.d* and *.e*]; a common clock input [*.k*]; an asynchronous direct reset input [*.rd*]; and an enable clock [*.ec*]. All may be driven from the interconnect resources adjacent to the blocks. Each CLB also has two outputs [*.x* and *.y*] which may drive interconnect networks.

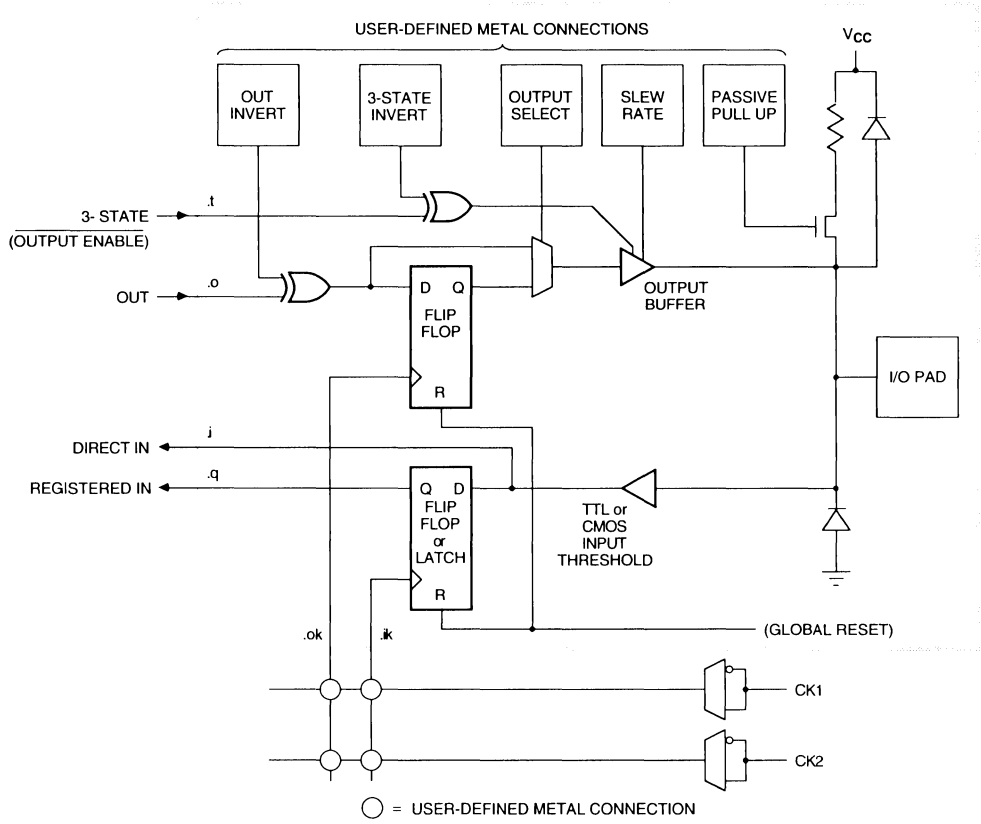


Figure 2. Input/Output Block. Each IOB includes input and output storage elements and I/O options pre-defined by the user. A choice of two clocks is available on each die edge. The polarity of each clock line (not each flip-flop or latch) is selectable. A clock line that triggers the flip-flop on the rising edge is an active Low Latch Enable (Latch transparent) signal and vice versa. Passive pull-up can only be enabled on inputs, not on outputs. All user inputs are selectable for TTL or CMOS thresholds.

Interconnect

User-defined interconnect resources in the Logic Cell Array provide routing paths to connect inputs and outputs of the I/O and logic blocks into logic networks. Interconnections between blocks are composed from a two-layer grid of metal segments. The XACT development system provides automatic routing of these interconnections. The inputs of the IOBs and CLBs are multiplexers that are defined to select an input network from the adjacent interconnect segments.

Three types of metal resources are provided to accommodate various network interconnect requirements:

- General Purpose Interconnect
- Direct Connection
- Long Lines

The topology of all these interconnect resources is identical with that of the FPGA, but the speed of the interconnect paths is significantly faster (since all interconnections are fixed metal connections).

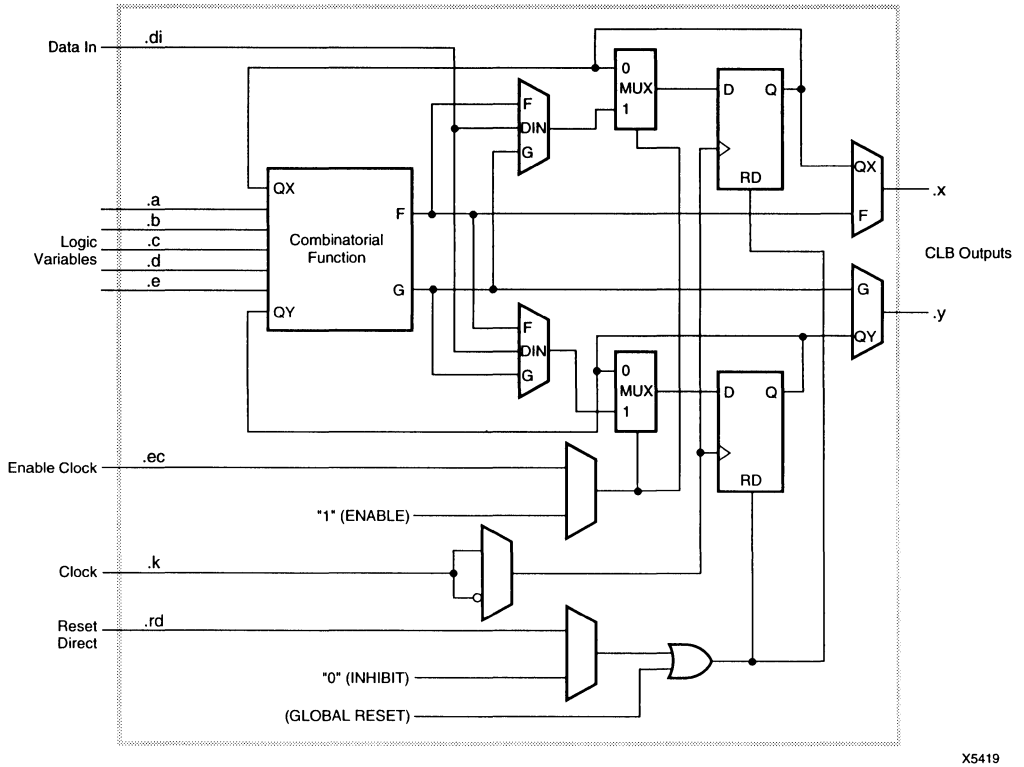


Figure 3. Configurable Logic Block. Each CLB includes a combinatorial logic section, two flip-flops and a user-defined multiplexer selection of function.

It has: five logic variable inputs .a, .b, .c, .d and .e.
a direct data in .di
an enable clock .ec
a clock (invertible) .k
an asynchronous reset .rd
two outputs .x and .y

Configuration and Start-Up

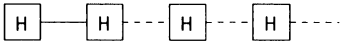
The HardWire LCA devices are designed to be fully compatible with their Programmable LCA equivalents. While the HardWire LCA parts do not require the loading of configuration data, they fully support a wide variety of configuration modes.

Configuration

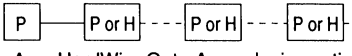
HardWire LCA devices can be used stand-alone or in a daisy chain with other LCAs. A HardWire LCA device cannot act in Master Parallel or Peripheral Mode. However, designs which use these modes can be supported by selection of a mask option which forces the device into Master Mode. This allows the HardWire LCA to be used when the original design used Peripheral Mode, without requiring any changes to the circuit board.

Mode 1. As a stand alone HardWire LCA Device.

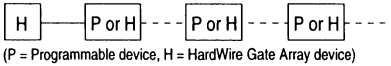
Mode 2. As a daisy chain of all HardWire LCA Devices.



Mode 3. As a HardWire LCA or programmable slave in a daisy chain with a Programmable device as a master.



Mode 4. As a HardWire Gate Array device acting as a Serial Master with any combination of Programmable and HardWire LCA devices as slaves.



(P = Programmable device, H = HardWire Gate Array device)

X5346

An XC3300A/L or XC3400A HardWire LCA device will not "swallow" its own configuration data. Whatever configuration bits are fed into the DIN pin will appear on the DOUT pin after a delay TDIO. In any case where a HardWire LCA device is ahead of a Programmable device in a daisy chain (as in Mode 3 and 4 shown above) the configuration data will need to be modified.

Start-up Sequence

The HardWire LCAs are designed to emulate the start-up sequence of the FPGA devices as closely as possible, however, some differences do exist. The start-up sequence may be thought of as three stages: power-on-reset; internal clear; and configuration.

An internal power-on-reset circuit is triggered when power is applied. When VCC reaches the voltage at which portions of the LCA begin to operate, the device generates a POR (power-on reset) pulse. The I/O output buffers are disabled and a high-impedance pull-up resistor is provided for the user I/O pins. The length of the POR pulse is user-defined to be either 64 µs or 16 ms. The 64 µs pulse is used for a rapid reset cycle; the 16 ms pulse emulates the power-on sequence of a FPGA. If the M0 pin is held Low during the POR cycle (or if the mask option to force the HardWire LCA into Master Mode is selected) the device will operate as a Master Mode device and the POR pulse will be extended to 4 times its nominal delay. This ensures that all daisy-chained slave devices will have sufficient time to power up.

Following the POR cycle, the HardWire LCA enters a "clearing" state. This state emulates the configuration memory clear performed by a FPGA upon power-up. The length of the clear cycle is 256 cycles (nominally 256 µs) for a standard POR, but is only 2 cycles if the rapid reset cycle was selected.

At the completion of the clear cycle the $\overline{\text{RESET}}$ pin is sampled. If the RESET pin is being held Low, the "configuration" will be delayed (with the $\overline{\text{INIT}}$ pin held Low) until $\overline{\text{RESET}}$ is driven High. If the $\overline{\text{RESET}}$ pin is being driven High (or once it has been driven High following a delayed "configuration") the open drain $\overline{\text{INIT}}$ pin will be released and the value of the M0 pin will be latched. If the device is in Master Mode (M0 = Low) it will begin to produce CCLKs. If the device is in Slave Mode (M0 = High) it will require CCLKs to be supplied from another device. After 4 CCLK cycles the part is "configured" and the Done/Program (D/P) pin will be released. (If the device is in a daisy chain with the D/P pins tied together the D/$\overline{\text{P}}$ pin will remain Low until all devices have completed configuration.) One CCLK after the D/P pin goes High the I/Os will become active. The internal user-logic reset is user-defined to release either one CCLK cycle before or after the I/O pins become active. A HardWire LCA operating in Master Mode will stop producing CCLKs one cycle after the I/Os become active.

Instant-On

When the Instant-On option is selected, the HardWire LCA has a short POR delay of nominally 4 µs. If the $\overline{\text{RESET}}$ pin is not held Low, the LCA goes active within an additional 1 µs. The DONE pin goes High, the I/Os become active, and the internal global set/reset signal goes inactive, Holding the $\overline{\text{RESET}}$ pin Low delays start-up until it is released, at which time the device goes active within 8 µs. The CCLK pin is disabled during the entire power-up and start-up sequence.

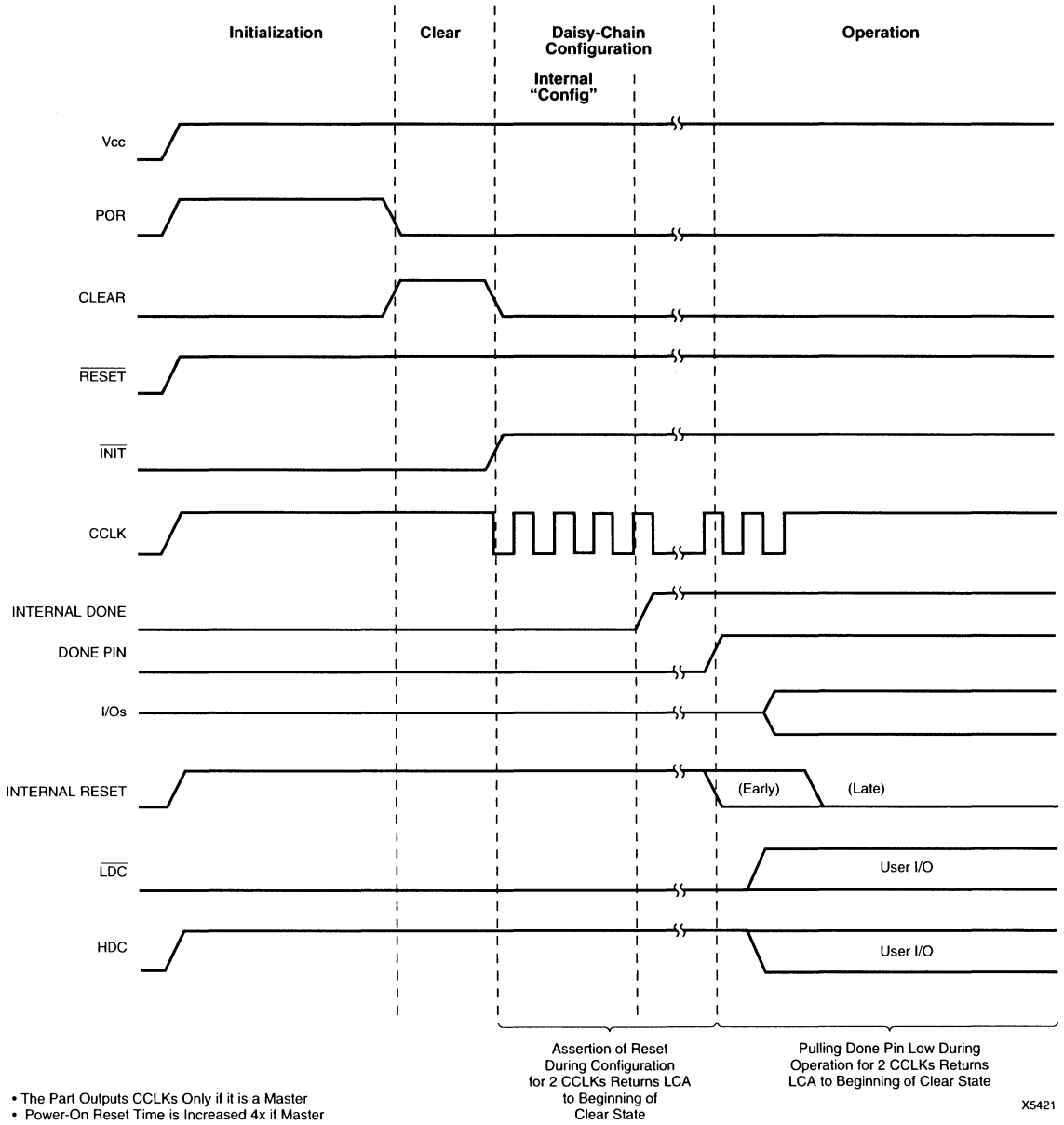


Figure 4. Psuedo-Configuration Waveform (Normal Power-Up)

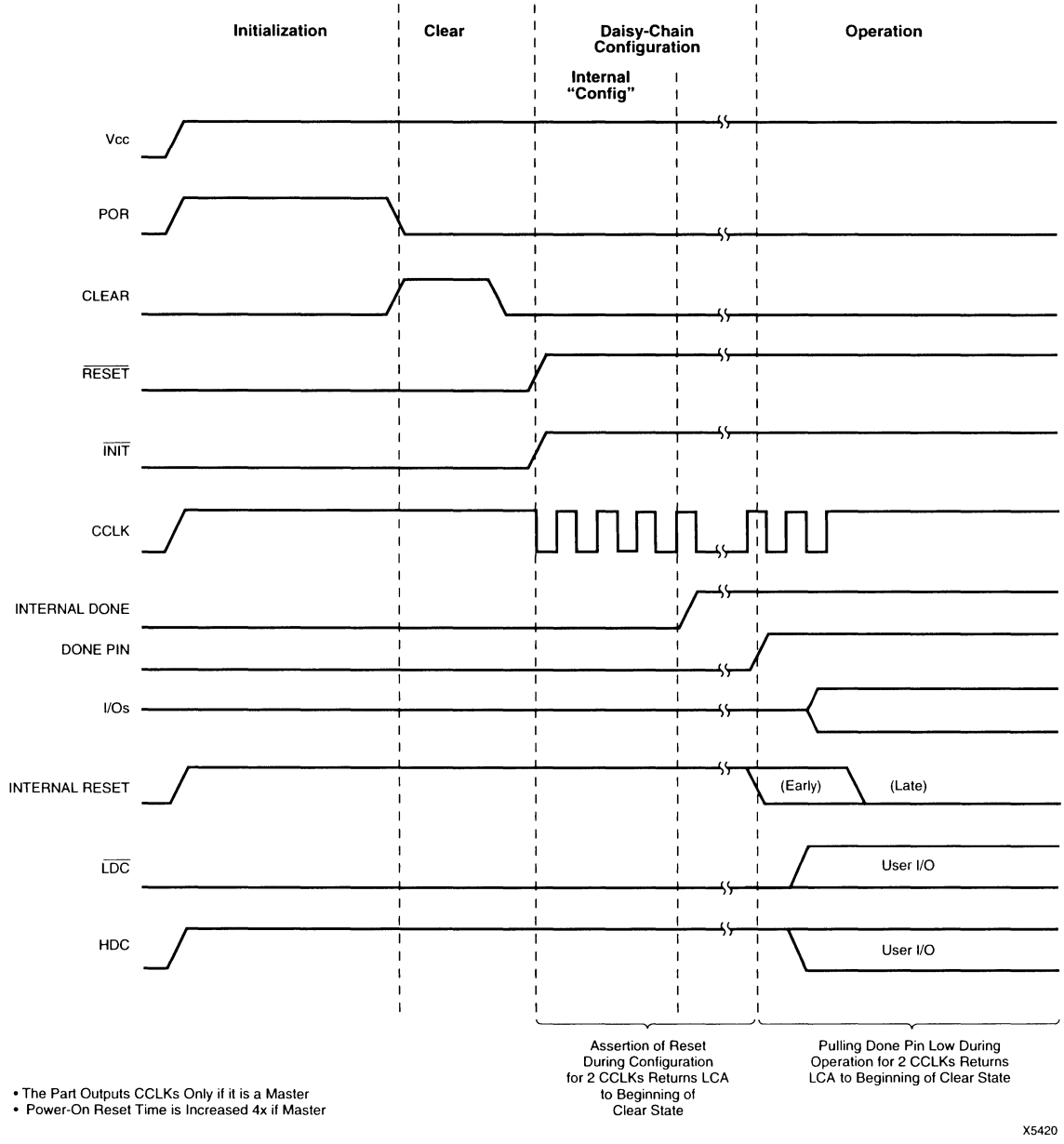


Figure 5. Psuedo-Configuration Waveform (Configuration Delay by Reset)

XC3300A/L/XC3400A series Boundary-Scan support:

The family supports IEEE 1149.1 compatible BYPASS, PRE-LOAD/SAMPLE and EXTEST Boundary-Scan instructions. Boundary-Scan is supported by a mask option selectable circuit built into the XC3300A/L/XC3400A family devices.

As more and more sophisticated assembly methods like surface mount technology become common place, Boundary-Scan can be used as a board level testing strategy where the traditional "bed of nails" testing is less appropriate. By using Boundary-Scan, test and design engineers can implement a test structure of a serial and/or parallel connections of a four-pin interface on any Boundary-Scan compatible IC. By scan methodology the user can easily load command and data into these devices to control the output drivers and sample the input signals.

The Boundary-Scan support logic is comprised of a 16-state, state machine, an instruction register and a number of data registers. A register operation begins with a "capture" where in a set of data is parallel loaded into the designated register for shifting out. The next state is "shift", where captured data are shifted out while the desired data are shifted in. States are provided for Wait operations. The last state of a register sequence is the update where the shifted content of the register is loaded into the appropriate instruction or data-holding register, either for instruction-register decode or for data-register pin control.

The primary data register is the Boundary-Scan register. Each IOB pin in the HardWire device includes three bits of shift register and three update latches for In, Out and 3-state control. Each Extest Capture captures all available input pins.

The other standard data register is the single flip-flop bypass register. It re-synchronizes data being passed through a device that need not be involved in the current scan operation.

The XC3300A/L/XC3400A family Boundary-Scan circuit is a mask option selected by the user. If Boundary-Scan is selected the user has the option of when it's enabled.

1) ALWAYS ENABLED: The Boundary-Scan pins are permanent. Boundary-Scan will be active and functional upon power-up. It will not wait for the DONE/PROGRAM pin to go high. The user can power up the device while holding the RESET pin low (delaying start-up) and still operate Boundary-Scan. However, dual function I/O pins such as: HDC, LDC, INIT and DOUT will stay in their "configuration" state until the device is in user-mode.
2) M1 pin controlled: The device will sample the M1 pin after the initialization state (at the same time it samples M0 pin to determine master/ slave configuration control). If the M1 pin is found to be in the "enable Boundary-Scan" mode (logic level to be determined by user as a mask option), the device will be in Boundary-Scan mode, and the Boundary-Scan pins will be enabled. When the M1 pin is driven to the opposite state, the Boundary-Scan pins will become user I/O. To reenter the Boundary-Scan mode, the user must "re-configure" the part (pull DONE/PROGRAM and RESET low) with the M1 pin driven to the "enable Boundary-Scan" state.

Unlike the XC4000 Boundary Scan pins, the TDI, TCK, TMS and TDO can be assigned to any user I/O by mask options. However, the dual function pins: HDC, LDC, INIT and DOUT cannot be used as Boundary-Scan pins due to circuit limitations.

The following instructions are supported in the XC3300A/L/XC3400A Boundary-Scan:

1) EXTEST
2) SAMPLE (only the I/O pad level is sampled)
3) BYPASS (The data shift register will not clock during the BYPASS instruction, unlike the XC4000)
4) 3-STATE (When this instruction is active, all user I/Os are 3-stated)

INTEST is not supported, and SAMPLE does not capture the values of internal nodes --only the I/O pad levels.

Three bits will be used to decode the four instructions, leaving room for extra, user-defined instructions. These extra instructions must be supported by "user-logic" JTAG circuitry that would co-exist with the regular design logic. By keeping the same pins for the JTAG circuit between the programmable design and the converted XC3300/XC3400 design, a seamless transition between the two JTAG circuits can be achieved.

The four supported instructions are decoded as follows:

Instruction I2	I1	I0	Test selected	TDO source	I/O Data
0	0	0	EXTEST	Data Register	Data Register
0	0	1	SAMPLE	Data Register	Pin Logic
1	1	1	BYPASS	Bypass Register	Pin Logic
1	0	0	3-STATE		

In order to support Boundary-Scan during the design phase in which programmable XC3000A/L/XC3100A part are used, there will be a Boundary-Scan emulation circuit which will be available in an application note along with a sample .LCA file. By using this .LCA design file and reconfigurability, the user can put the design into Boundary-Scan test mode, run the tests then re-configure the device for user mode.

Performance

The XC3300A/L/XC3100A family of HardWire LCAs are manufactured in the same high-performance sub-micron CMOS technology as their FPGA equivalents. Traditionally the toggle frequency of a flip-flop has been used to describe the overall performance of a semi-custom device. The configuration used for determining this rate is shown in Figure 6.

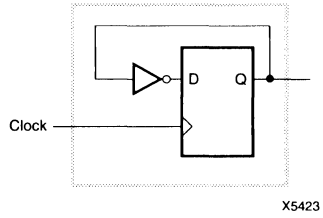


Figure 6. Toggle Flip-Flop. This is used to characterize device performance.

Actual LCA performance is determined by the timing of critical paths, including the timing for the logic and storage elements in that path and the timing of the associated interconnect. HardWire LCA logic block performance is equal to or slightly faster than the equivalent FPGA, while the interconnect performance is significantly faster.

All HardWire LCA devices are specified and tested for operation at the fastest equivalent FPGA speed available at the time the HardWire LCA device is introduced.

Power

Power for the LCA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the LCA, dedicated V_{CC} and ground rings surround the logic array and provide power to the I/O drivers. (See Figure 7.) An independent matrix of V_{CC} and ground lines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically a 0.1-µF capacitor connected near the V_{CC} and ground pins will provide adequate decoupling.

Output buffers capable of driving the specified 4-mA loads under worst-case conditions may be capable of driving 25 to 30 times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads. The I/O Block output buffers have a slew-limited mode which should be used where output rise and fall times are not speed critical. Slew-limited outputs maintain their dc drive capability, but generate less external reflections and internal noise. A maximum total external capacitive load for simultaneous fast mode switching in the same direction is 500 pF per power/ground pin pair. For slew-rate limited outputs this total is four times larger.

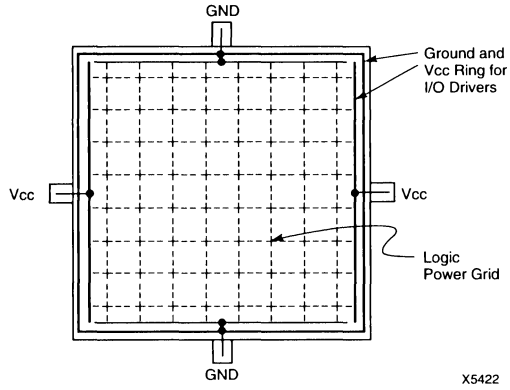


Figure 7. LCA Power Distribution.

HardWire LCA Design Considerations

It is important to observe good design practices while using HardWire LCAs. It is possible for a programmable device to "hide" some less obvious design shortcomings. However, these can manifest themselves when the design is converted to a HardWire LCA.

For example, a small glitch generated from unstable inputs to a CLB function block can be easily "swallowed" if the output is driving a long net. This is because the "pass transistors" act as a Low pass filter and that nets loads may never see the glitch. However, in a HardWire LCA, this glitch may propagate to the loads since there are only metal lines and vias in the routing path.

Gated Clocks and Reset Directs

Glitching function generators driving CLOCK and RESET DIRECT pins can inadvertently trigger flip-flops to an undesirable state. Avoid these so-called "gated" clock and reset direct nets; if unavoidable, design the logic so that the inputs are always stable and the signal changes are at least a CLB delay (Tilo) apart.

Multiplexers Implemented in Function Generators

Two input multiplexers can be easily implemented in a single F or G function genterator. However, there is a possibility of a glitch if the selected signal and the selected input changes within a CLB's T_{ILO} delay. This is generally not a problem with data and address multiplexers as long as the output is given enough time to settle; but if the multiplexer output is feeding a CLOCK and/or a RESET DIRECT pin, it is possible to toggle the register at undesired times.

The edge(s) of select signals for a CLOCK and/or RESET DIRECT multiplexers should be stable before and after the edges of the inputs. The edges should be at least a CLB (T_{ILO}) delay apart.

Race Conditions

All race conditions in the circuit need to go through a careful analysis. Depending on the routing resources responsible for the net delays, the correct signal may always "win the race" in a programmable FPGA; however, once converted to HardWire LCA, this may not be the case. (See Figure 8.)

Delay Generators

Using the routing resources as delay lines in programmable FPGAs is undesirable. In HardWire LCAs, it is an invitation for timing problems. You should remove all these delay generators and redesign the circuit before converting it to HardWire.

Interfacing with External Devices

Almost all LCAs interface with external devices–FIFOs, memories, processors and peripherals, etc. Handshaking with devices requires specific setup/hold times. Ample hold time on a data bus from a programmable FPGA may no longer meet spec in HardWire LCA. An external data bus clocked by a HardWire LCA gererated signal may no longer meet the system set-up time requirements. This can happen because interconnects are much faster than in a programmable device. This requires you to also review the system timing specs when converting to a HardWire LCA.

In reality, all designers using LCAs (programmable or HardWire) face the same issues. Due to improvements in process and circuit design, a part specified at a given speed grade today may actually run faster in the future. Xilinx does not guarantee a part against minimum timing specs. A "glitch" that was swallowed in a device today may crop up in a future device due to faster pass transistors in the routing paths. When using any Xilinx LCAs, the above issues should be addressed in the design phase.

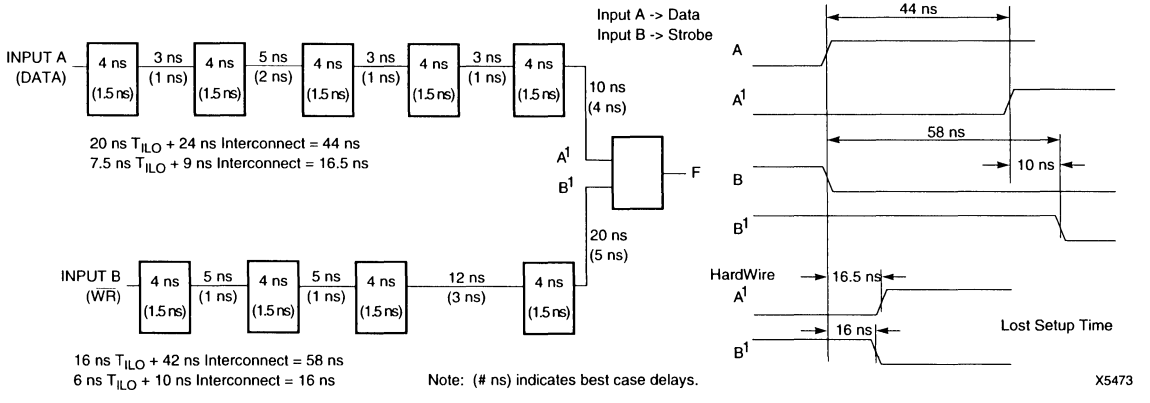


Figure 8. Race Condition Example

HardWire LCA Testability

The HardWire LCA products contain significant on-chip logic to facilitate manufacturability and testing. This logic, combined with Xilinx's internal Automatic Test Generation (ATG) software, assures 100% functionality. In fact, the HardWire LCA can be 100% functionally tested by Xilinx without the need for customer generated test vectors (as is required with custom gate arrays).

This section examines the two basic block structures and the special test circuitry in the HardWire LCA.

Test Architecture

The HardWire LCA contains two types of internal blocks: the Input/Output Block (IOB) and the Configurable Logic Block (CLB). To accomplish 100% functional testing special test circuitry is designed into the device. This circuitry allows testing of each block (CLB and IOB) in a synchronized procedure known as "Scan Test". Special dedicated test latches (called TBLKs) are included on all HardWire devices. They are completely transparent to the normal operation of the circuit. Scan testing allows the contents of all internal flip-flops to be serially shifted off-chip, and for Xilinx generated test vectors to be shifted into the device, thus enabling all flip-flops to be initialized to any desired state.

These special dedicated test latches are placed into each CLB and IOB. Each CLB has four internal test latches, (placed at the CLB outputs), while each IOB contains four test latches (placed at the IOB inputs) as shown in Figures 9 and 10. The placement of these test latches is very important, since each CLB output or IOB input can fanout to multiple destinations. All sources and destinations of logic blocks come from other logic blocks, thus this placement of the latches provides complete access to all nets and synchronized control of all CLBs and IOBs.

The test latches are connected into a daisy chain which passes through every flip-flop in the LCA. Figure 11 shows an overview of the scan path. The path begins at the Scan In pin, sequences through each CLB, then through the IOBs, and finally exits at the Scan Out pin. This scan path can be seen in more detail in Figure 12, which shows the precise sequence with which the CLB and IOB internal test latches are loaded or read.

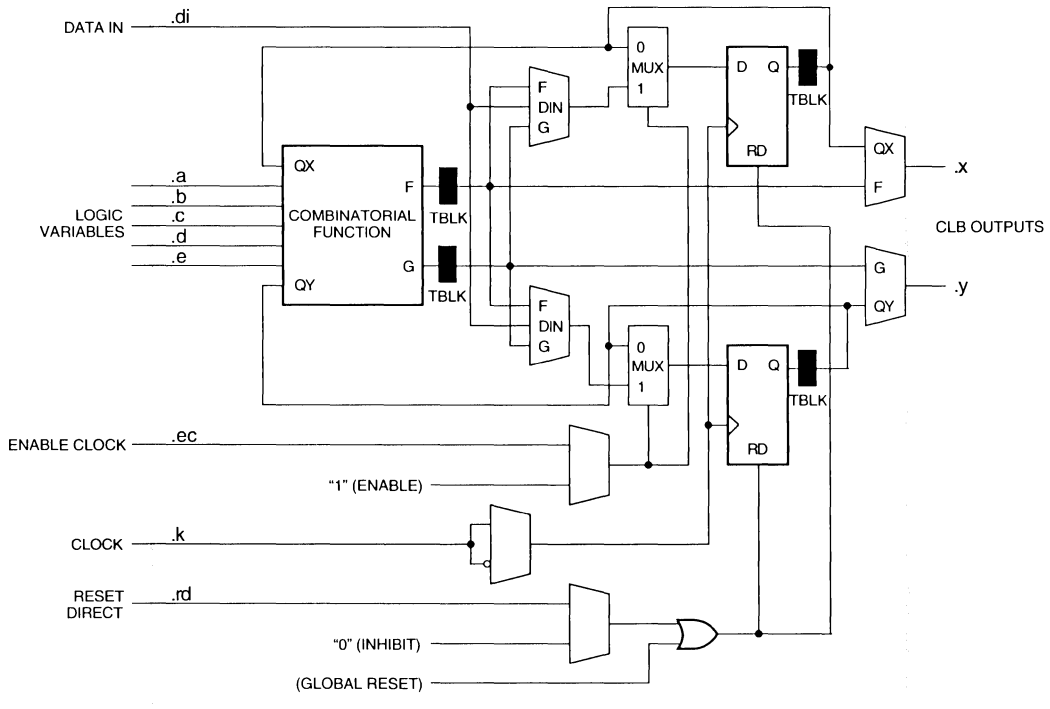


Figure 9. XC3300A, XC3300L, XC3400A HardWire CLB Test Latch Locations

X1350

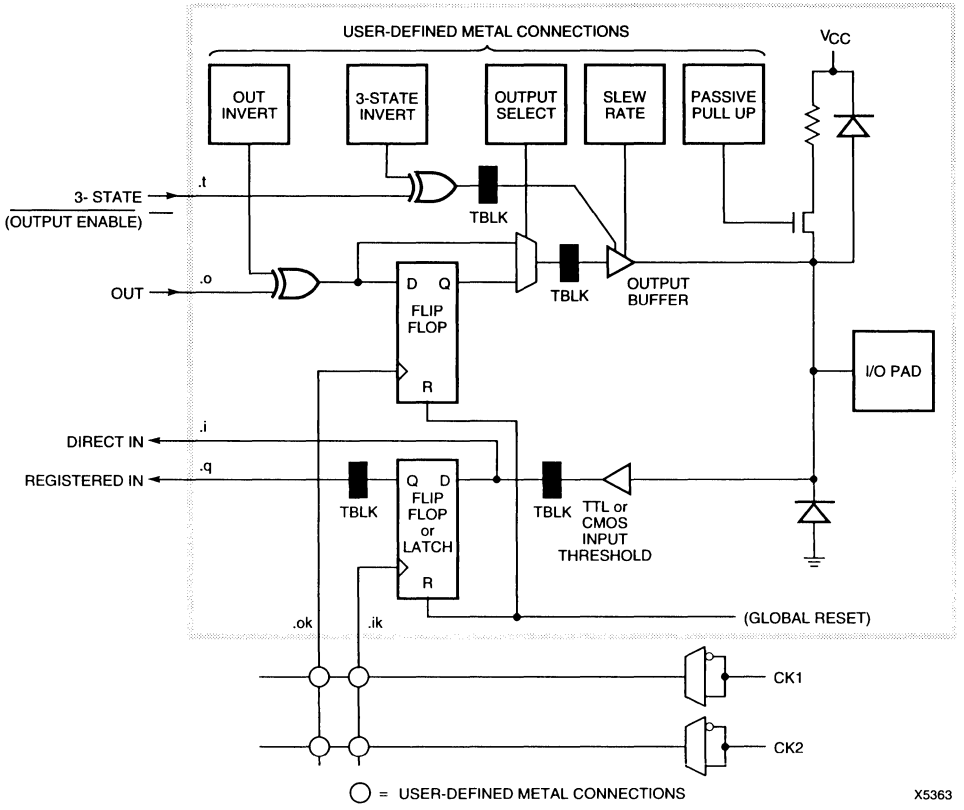


Figure 10. XC3300A, XC3300L, XC3400A HardWire IOB Test Latch Location

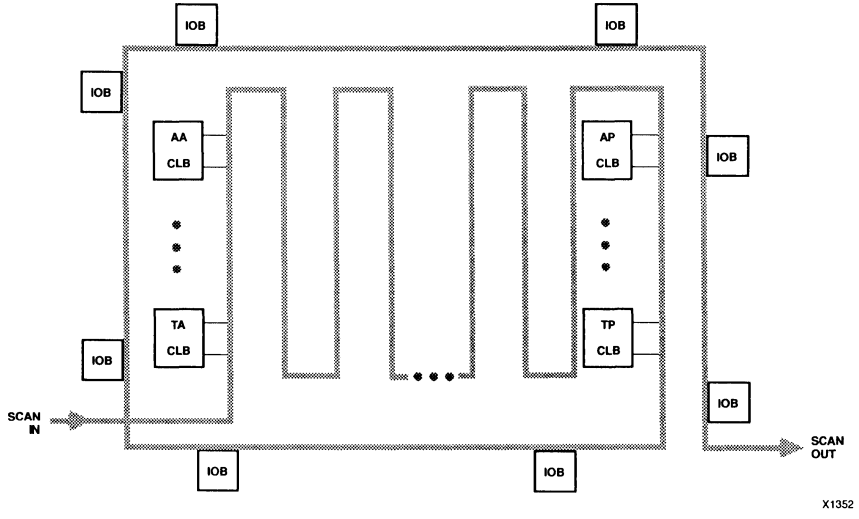


Figure 11. Scan Path Overview

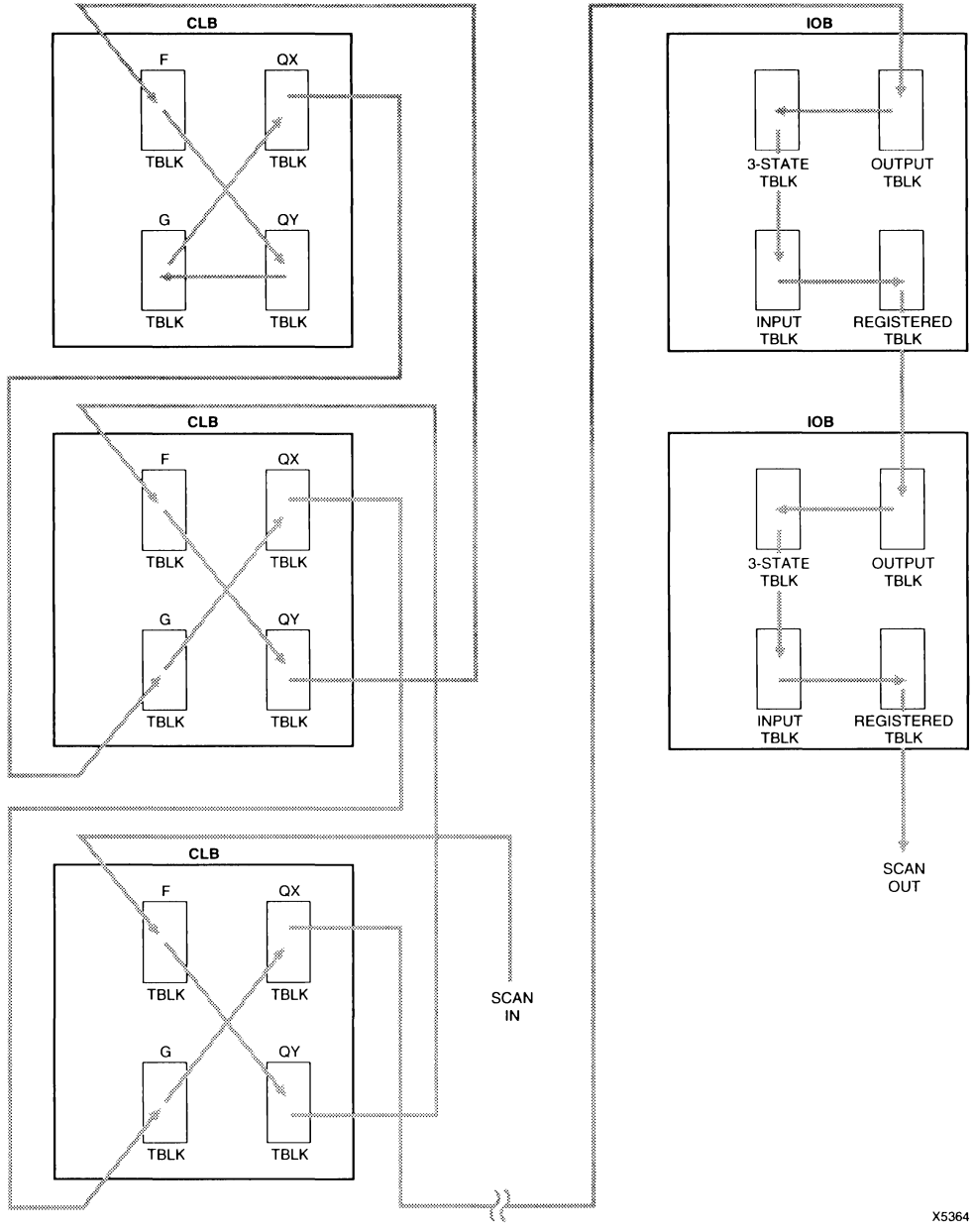


Figure 12. Detailed Scan Path

The internal architecture of a TBLK is shown in Figure 13. In the normal operation mode of the HardWire LCA, SW1 is in position A and all the test latches are bypassed completely. The HardWire LCA device is set into Test Mode (SW1 = position B) by Xilinx ATG software. This software inputs unique conditions on several control pins while serially loading a "password" into the device. For this reason, it is not possible for a customer design to inadvertently place the HardWire LCA into Test Mode. When SW1 is in position B (Test Mode) all the latches can receive data from either the CLB output or the previous latch in the daisy chain (SQn).

Synchronized together by a special test clock, all the test latches operate in two phases. The first phase serially loads all the latches to place a specific vector at the inputs of the logic block to be tested. The second phase is a parallel load of all latches, storing the expected output data of the logic block being tested (SW2 = A). At this point testing returns to phase one and serially clocks out the results, while simultaneously clocking in a new input vector.

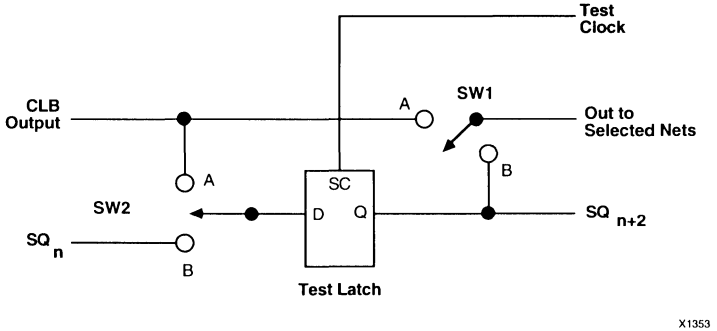


Figure 13. TBLK Block Diagram

XC3300A, XC3300L, XC3400A Family Configuration Pin Assignments

CONFIGURATION MODE: <M0>												
SLAVE <1>	MASTER <0>	44 PLCC	68 PLCC	84 PLCC	100 PQFP	100 TQFP/ VQFP	132 PPGA	160 PQFP	176 TQFP	208 PQFP	175 PPGA	USER OPERATION
PWR DWN	PWR DWN	7	10	12	29	26	A1	159	1	3	B2	PWR DWN (I)
VCC	VCC	12	18	22	41	38	C8	20	23	26	D9	VCC
M1 (I)	M1 (I)	16	25	31	52	49	B13	40	45	48	B14	M1
M0 (HIGH) (I)	M0 (HIGH) (I)	17	26	32	54	51	B14	42	47	50	B15	M0 (I)
		18	27	33	56	53	D14	44	51	56	C15	I/O
HDC (HIGH)	HDC (HIGH)	19	28	34	57	54	G14	45	50	57	C15	I/O
LDC (LOW)	LDC (LOW)	20	30	36	59	56	H12	49	54	61	D16	I/O
INIT *	INIT *	22	34	42	65	62	M13	59	65	77	H15	I/O
GND	GND	23	35	43	66	63	P14	19	67	79	J14	GND
		26	43	53	67	73	N13	76	85	100	P15	XTL2 or I/O
RESET (I)	RESET (I)	27	44	54	78	75	P14	78	87	102	R15	RESET (I)
DONE	DONE	28	45	55	80	77	N13	80	89	107	R14	PROGRAM (I)
			46	56	81	78	M12	81	90	109	N13	I/O
		30	47	57	82	79	P13	82	91	110	T14	XTL1 or I/O
			48	58	83	80	N11	86	92	115	P12	I/O
			49	60	87	84	M9	92	93	122	T11	I/O
			50	61	88	85	N9	93	94	123	R10	I/O
			51	62	89	86	N8	98	95	128	R9	I/O
VCC	VCC	34	52	64	91	88	M8	100	110	130	N9	VCC
			53	65	92	89	N7	102	112	132	P8	I/O
			54	66	93	90	P6	103	113	133	R8	I/O
			55	67	94	91	M6	108	114	138	R7	I/O
			56	70	98	95	M5	114	115	145	R5	I/O
			57	71	99	96	N4	115	116	146	P5	I/O
DIN (I)	DIN (I)	38	58	72	100	97	N2	119	130	151	R3	I/O
DOUT	DOUT	39	59	73	1	98	M3	120	131	152	N4	I/O
CCLK (I)	CCLK	40	60	74	2	99	P1	121	132	153	R2	CCLK (I)
			61	75	5	2	M2	124	135	161	P2	I/O
			62	76	6	3	N1	125	136	162	M3	I/O
			63	77	8	5	L2	128	138	165	P1	I/O
			64	78	9	6	L1	129	139	166	N1	I/O
			65	81	12	9	K1	132	140	172	M1	I/O
			66	82	13	10	J2	133	141	173	L2	I/O
			67	83	14	11	H1	136	144	178	K2	I/O
			68	84	15	12	H2	137	145	179	K1	I/O
GND	GND	1	1	1	16	13	H3	139	154	182	J3	GND
			2	2	17	14	G2	141	156	184	H2	I/O
			3	3	18	15	G1	142	157	185	H1	I/O
			4	4	19	16	F2	147	158	192	F2	I/O
			5	5	20	17	E1	148	159	193	E1	I/O
			6	8	23	20	D1	151	162	199	D1	I/O
			7	9	24	21	D2	152	163	200	C1	I/O
			8	10	25	22	B1	155	164	203	E3	I/O
			9	11	26	26	C2	156	165	204	C2	I/O
		X	X	X	X	X						XC3330
				X	X	X						XC3342
				X			X	X	X	X	X	XC3390

Represents a 50-kΩ to 100-kΩ Pull-Up

* INIT is an Open Drain Output During Configuration

(I) Represents an Input

X5476

Note: Pin assignments of "PGA Footprint" PLCC sockets and PGA packages are not electically identical. Generic I/O pins are not shown

XC3300A, XC3300L, XC3400A Family Pin Assignments

Xilinx offers the three different array size in the XC3300A/L/3400A series in a variety of surface-mount and through-hole package types, with pin counts from 44 to 208.

Each chip is offered in several package types to accomodate the available PC board space and manufacturing technology. Most package types are also offered with different chips to accommodate design changes without the need for PC board changes.

Note that there may not be a perfect match between the number of I/O pads on the chip and the number of pins on a package. In some cases, the chip has more I/O pads than there are pins on the package, as indicated below on the following table. The IOBs of the unconnected pads can still be used as storage elements if the specified propagation delays and set-up times are acceptable.

Number of Available I/O Pins

		Number of Package Pins												
	Max I/O	44	64	68	84	100	132	144	160	175	176	191	196	208
XC3330A/L, XC3430A	80	34	54	58	74	80								
XC3342A/L, XC3442A	96				74	82								
XC3390A/L, XC3490A	144				70		110	120	138	144	144			144

X5362

Pin Descriptions

Permanently Dedicated Pins.

V_{CC}
Two to eight (depending on package type) connections to the nominal +5 V supply voltage. All must be connected.

GND
Two to eight (depending on package type) connections to ground. All must be connected.

PWRDWN
A Low on this CMOS-compatible input stops all internal activity. All flip-flops and latches are reset, all outputs are 3-stated, and all inputs are interpreted as High, independent of their actual level. While PWRDWN is Low, V_{CC} may be reduced to any value >2.3 V. When PWDWN returns High, the LCA becomes operational with DONE Low for two cycles of the internal 1-MHz clock. During configuration, PWRDWN must be High. If not used, PWRDWN must be tied to V_{CC}.

RESET
This is an active Low input which has three functions.

Prior to the start of configuration, a Low input will delay the start of the configuration process. An internal circuit senses the application of power and begins a minimal time-out cycle. When the time-out and RESET are complete, the level of the M0 line is sampled and configuration begins.

If RESET is asserted during a configuration, the LCA device is re-initialized and restarts the configuration at the termination of RESET.

If RESET is asserted after configuration is complete, it provides a global asynchronous reset of all IOB and CLB storage elements of the LCA device.

CCLK
During configuration, Configuration Clock is an output of an LCA in Master mode or Peripheral mode, but an input in Slave mode.

CCLK drives dynamic circuitry inside the LCA. The Low time may, therefore, not exceed a few microseconds. When used as an input, CCLK must be "parked High". An internal pull-up resistor maintains High when the pin is not being driven.

DONE/PROG
DONE is an open-drain output, configurable with or without an internal pull-up resistor. At the completion of configuration, the LCA circuitry becomes active in a synchronous order, and DONE/PROG goes active High one cycle before the outputs go active.

Once configuration is done, a High-to-Low transition of this pin will cause an initialization of the device and start a reconfiguration.

M0
As Mode 0, this input sampled is before the start of configuration to establish the configuration mode to be used.

M1
This input is used only for manufacturer test. The user must tie this pin either High or Low in-system.

User I/O Pins that can have special functions.

HDC
During configuration, this output is held at a High level to indicate that configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin.

LDC
During Configuration, this output is held at a Low level to indicate that the configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin. $\overline{\text{LDC}}$ is particularly useful in Master mode as a Low enable for an EPROM, but it must then be programmed as a High after configuration.

$\overline{\text{INIT}}$
This is an active Low open-drain output which is held Low during the power stabilization and internal clearing of the configuration memory. It can be used to indicate status to a configuring microprocessor, as a wired AND of several slave mode devices, or as a hold-off signal for a master mode device. After configuration this pin becomes a user programmable I/O pin.

BCLKIN
This is a direct CMOS level input to the alternate clock buffer (Auxiliary Buffer) in the lower right corner.

XTL1
This user I/O pin can be used to operate as the output of an amplifier driving an external crystal and bias circuitry.

XTL2
This user I/O pin can be used as the input of an amplifier connected to an external crystal and bias circuitry. The I/O Block is left unconfigured. The oscillator configuration is activated by routing a net from the oscillator buffer symbol output.

DIN
During Slave or Master Serial configuration, this pin is used as a serial-data input.

DOUT
During configuration this pin is used to output serial-configuration data to the DIN pin of a daisy-chained slave.

TCLKIN
This is a direct CMOS level input to the global clock buffer.

Unrestricted User I/O Pins.

I/O
An I/O pin may be programmed by the user to be an Input or an Output pin following configuration. All unrestricted I/O pins, plus the special pins mentioned previously, have a weak pull-up resistor of 50 kΩ to 100 kΩ that becomes active as soon as the device powers up, and stays active until the end of configuration.

XC3300A, XC3300L, XC3400A Family 44-Pin PLCC Pinouts

Pin Number	XC3330A/L, XC3430A
1	**GND**
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	PWRDWN
8	TCLKIN-I/O
9	I/O
10	I/O
11	I/O
12	**VCC**
13	I/O
14	I/O
15	I/O
16	M1-RDATA
17	M0-RTRIG
18	M2-I/O
19	HDC-I/O
20	LDC-I/O
21	I/O
22	INIT-I/O

Pin Number	XC3330A/L, XC3430A
23	**GND**
24	I/O
25	I/O
26	XTL2(IN)-I/O
27	RESET
28	DONE-PGM
29	I/O
30	XT1(OUT)-BCLK-I/O
31	I/O
32	I/O
33	I/O
34	**VCC**
35	I/O
36	I/O
37	I/O
38	DIN-I/O
39	DOUT-I/O
40	CCLK
41	I/O
42	I/O
43	I/O
44	I/O

XC3330A, XC3330L, and XC3430A Family 64-Pin Plastic VQFP Pinouts

Pin No.	XC3330A/L, XC3430A
1	I/O
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	**GND**
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	PWRDN
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	**VCC**
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	M1-RDATA
32	M0-RTRIG

Pin No.	XC3330A/L, XC3430A
33	M2-I/O
34	HDC-I/O
35	I/O
36	LDC-I/O
37	I/O
38	I/O
39	I/O
40	INIT-I/O
41	**GND**
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	XTAL2(IN)-I/O
48	RESET
49	DONE-PG
50	I/O
51	XTAL1(OUT)-BCLKN-I/O
52	I/O
53	I/O
54	I/O
55	I/O
56	**VCC**
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	DIN-I/O
63	DOUT-I/O
64	CCLK

XC3330A, XC3330L, XC3430A, XC3342A, XC3342L, XC3442L Family
68-Pin and 84-Pin PLCC Pinouts

XC3330A/L, XC3430A, XC3342A/L,XC3442A	68 PLCC	84 PLCC
PWRDN	10	12
TCLKIN-I/O	11	13
I/O		14
I/O	12	15
I/O	13	16
I/O	—	17
I/O	14	18
I/O	15	19
I/O	16	20
I/O	17	21
VCC	18	22
I/O	19	23
I/O	—	24
I/O	20	25
I/O	21	26
I/O	22	27
I/O	—	28
I/O	23	29
I/O	24	30
M1	25	31
M0	26	32
I/O	27	33
HDC-I/O	28	34
I/O	29	35
LDC-I/O	30	36
I/O	31	37
I/O		38
I/O	32	39
I/O	33	40
I/O		41
INIT-I/O	34	42
GND	35	43
I/O	36	44
I/O	37	45
I/O	38	46
I/O	39	47
I/O	40	48
I/O	41	49
I/O		50
I/O		51
I/O	42	52
XTL2(IN)-I/O	43	53

XC3330A/L, XC3430A, XC3342A/L,XC3442A	68 PLCC	84 PLCC
RESET	44	54
DONE-PG	45	55
I/O	46	56
XTL1(OUT)-BCLKIN-I/O	47	57
I/O	48	58
I/O	—	59
I/O	49	60
I/O	50	61
I/O	51	62
I/O	—	63
VCC	52	64
I/O	53	65
I/O	54	66
I/O	55	67
I/O	—	68
I/O		69
I/O	56	70
I/O	57	71
DIN-I/O	58	72
DOUT-I/O	59	73
CCLK	60	74
I/O	61	75
I/O	62	76
I/O	63	77
I/O	64	78
I/O		79
I/O		80
I/O	65	81
I/O	66	82
I/O	67	83
I/O	68	84
GND	1	1
I/O	2	2
I/O	3	3
I/O	4	4
I/O	5	5
I/O		6
I/O		7
I/O	6	8
I/O	7	9
I/O	8	10
I/O	9	11

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

This table describes the pinouts of two different chips in two different packages. The first column lists 84 of the 118 pads on the XC3x42x (and 84 of the 98 pads on the XC3x30x) that are connected to the 84 package pins. Six pads, indicated by a dash (–) in the 68 PLCC column, have no connections in the 68 PLCC package, but are connected in the 84-pin package.

XC3390A, XC3390L, XC3490A Family
84-Pin PLCC Pinout

PLCC Pin Number	XC3390A/L, XC3490A
12	$\overline{\text{PWRDN}}$
13	TCLKIN-I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	**GND***
22	**VCC**
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	M1
32	M0
33	I/O
34	HDC-I/O
35	I/O
36	$\overline{\text{LDC}}$-I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	INIT/I/O*
42	**VCC***
43	**GND**
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	I/O
53	XTL2(IN)-I/O

PLCC Pin Number	XC3390A/L, XC3490A
54	$\overline{\text{RESET}}$
55	DONE-$\overline{\text{PG}}$
56	I/O
57	XTL1(OUT)-BCLKIN-I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	**VCC**
65	**GND***
66	I/O*
67	I/O*
68	I/O*
69	I/O
70	I/O
71	I/O
72	DIN-I/O
73	DOUT-I/O
74	CCLK
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	I/O
84	I/O
1	**GND**
2	**VCC***
3	I/O*
4	I/O*
5	I/O*
6	I/O*
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed ouptuts are default slew-rate limited.

* Different pin definition than XC3x42x PC84 package

XC3330A, XC3330L, XC3430A, XC3342A, XC3342L, XC3442A Family
100-Pin PQFP, TQFP, VQFP Pinouts

TQFP/ VQFP Pin No.	PQFP Pin No.	XC3330A/L, XC3430A, XC3342A/L, XC3442A
13	16	**GND**
14	17	I/O
15	18	I/O
16	19	I/O
17	20	I/O
18	21	I/O
19	22	I/O
20	23	I/O
21	24	I/O
22	25	I/O
23	26	I/O
24	27	**VCC**
25	28	**GND**
26	29	PWRDN
27	30	TCLKIN-I/O
28	31	I/O**
29	32	I/O
30	33	I/O
31	34	I/O
32	35	I/O
33	36	I/O
34	37	I/O
35	38	I/O
36	39	I/O
37	40	I/O
38	41	**VCC**
39	42	I/O
40	43	I/O
41	44	I/O
42	45	I/O
43	46	I/O
44	47	I/O
45	48	I/O
46	49	I/O

TQFP/ VQFP Pin No.	PQFP Pin No.	XC3330A/L, XC3430A, XC3342A/L, XC3442A
47	50	I/O
48	51	I/O
49	52	M1
50	53	**GND**
51	54	M0
52	55	**VCC**
53	56	I/O
54	57	HDC-I/O
55	58	I/O
56	59	LDC-I/O
57	60	I/O
58	61	I/O
59	62	I/O
60	63	I/O
61	64	I/O
62	65	INIT-I/O
63	66	GND
64	67	I/O
65	68	I/O
66	69	I/O
67	70	I/O
68	71	I/O
69	72	I/O
70	73	I/O
71	74	I/O
72	75	I/O
73	76	XTAL2-I/O
74	77	**GND**
75	78	RESET
76	79	**VCC**
77	80	DONE-PG
78	81	I/O
79	82	BCLKIN-XTAL1-I/O
80	83	I/O

TQFP/ VQFP Pin No.	PQFP Pin No.	XC3330A/L, XC3430A, XC3342A/L, XC3442A
81	84	I/O
82	85	I/O
83	86	I/O
84	87	I/O
85	88	I/O
86	89	I/O
87	90	I/O
88	91	**VCC**
89	92	I/O
90	93	I/O
91	94	I/O
92	95	I/O
93	96	I/O
94	97	I/O
95	98	I/O
96	99	I/O
97	100	DIN-I/O
98	1	DOUT-I/O
99	2	CCLK
100	3	**VCC**
1	4	**GND**
2	5	I/O
3	6	I/O
4	7	I/O**
5	8	I/O
6	9	I/O
7	10	I/O
8	11	I/O
9	12	I/O
10	13	I/O
11	14	I/O
12	15	I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs.
Programmed outputs are default slew-rate limited.

This table describes the pinouts of two different chips in two different packages. The third column lists 100 of the 118 pads on the XC3x42x that are connected to the 100 package pins. Two pads, indicated by double asterisks, do not exist on the XC3x30x, which has 98 pads; therefore the corresponding pins have no connections.

XC3390A, XC3390L, XC3490A Family
132-Pin Plastic PGA Pinout

PGA Pin Number	XC3390A/L, XC3490A	PGA Pin Number	XC3390A/L, XC3490A	PGA Pin Number	XC3390A/L, XC3490A	PGA Pin Number	XC3390A/L, XC3490A
C4	**GND**	B13	M1	P14	$\overline{\text{RESET}}$	M3	DOUT-I/O
A1	$\overline{\text{PWRDN}}$	C11	**GND**	M11	**VCC**	P1	CCLK
C3	I/O-TCLKIN	A14	M0	N13	DONE-$\overline{\text{PG}}$	M4	**VCC**
B2	I/O	D12	**VCC**	M12	I/O	L3	**GND**
B3	I/O	C13	I/O	P13	XTAL1-I/O-BCLKIN	M2	I/O
A2	I/O	B14	HDC-I/O	N12	I/O	N1	I/O
B4	I/O	C14	I/O	P12	I/O	M1	I/O
C5	I/O	E12	I/O	N11	I/O	K3	I/O
A3	I/O	D13	I/O	M10	I/O	L2	I/O
A4	I/O	D14	$\overline{\text{LDC}}$-I/O	P11	I/O	L1	I/O
B5	I/O	E13	I/O	N10	I/O	K2	I/O
C6	I/O	F12	I/O	P10	I/O	J3	I/O
A5	I/O	E14	I/O	M9	I/O	K1	I/O
B6	I/O	F13	I/O	N9	I/O	J2	I/O
A6	I/O	F14	I/O	P9	I/O	J1	I/O
B7	I/O	G13	I/O	P8	I/O	H1	I/O
C7	**GND**	G14	$\overline{\text{INIT}}$-I/O	N8	I/O	H2	I/O
C8	**VCC**	G12	**VCC**	P7	I/O	H3	**GND**
A7	I/O	H12	**GND**	M8	**VCC**	G3	**VCC**
B8	I/O	H14	I/O	M7	**GND**	G2	I/O
A8	I/O	H13	I/O	N7	I/O	G1	I/O
A9	I/O	J14	I/O	P6	I/O	F1	I/O
B9	I/O	J13	I/O	N6	I/O	F2	I/O
C9	I/O	K14	I/O	P5	I/O	E1	I/O
A10	I/O	J12	I/O	M6	I/O	F3	I/O
B10	I/O	K13	I/O	N5	I/O	E2	I/O
A11	I/O	L14	I/O	P4	I/O	D1	I/O
C10	I/O	L13	I/O	P3	I/O	D2	I/O
B11	I/O	K12	I/O	M5	I/O	E3	I/O
A12	I/O	M14	I/O	N4	I/O	C1	I/O
B12	I/O	N14	I/O	P2	I/O	B1	I/O
A13	I/O	M13	XTAL2(IN)-I/O	N3	I/O	C2	I/O
C12	I/O	L12	**GND**	N2	DIN-I/O	D3	**VCC**

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

XC3342A, XC3342L, XC3442A Family
144-Pin Plastic TQFP Pinouts

Pin Number	XC3342A/L, XC3442A
1	PWRDN
2	I/O-TCLKIN
3	–
4	I/O
5	I/O
6	–
7	I/O
8	I/O
9	–
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	–
16	I/O
17	I/O
18	**GND**
19	**VCC**
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	–
29	I/O
30	I/O
31	–
32	–
33	I/O
34	–
35	I/O
36	M1
37	**GND**
38	MO
39	**VCC**
40	I/O
41	HDC-I/O
42	I/O
43	I/O
44	I/O
45	LDC-I/O
46	–
47	I/O
48	I/O

Pin Number	XC3342A/L, XC3442A
49	I/O
50	–
51	I/O
52	I/O
53	INIT-I/O
54	**VCC**
55	**GND**
56	I/O
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	–
64	–
65	I/O
66	I/O
67	I/O
68	I/O
69	XTL2(IN)-I/O
70	**GND**
71	RESET
72	**VCC**
73	DONE-PG
74	D7-I/O
75	XTL1(OUT)-BCLKIN-I/O
76	I/O
77	I/O
78	D6-I/O
79	I/O
80	–
81	I/O
82	I/O
83	–
84	I/O
85	I/O
86	–
87	–
88	I/O
89	I/O
90	**VCC**
91	**GND**
92	I/O
93	I/O
94	–
95	–
96	I/O

Pin Number	XC3342A/L, XC3442A
97	I/O
98	I/O
99	–
100	I/O
101	–
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	CCLK
109	**VCC**
110	**GND**
111	/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	I/O
119	I/O
120	I/O
121	–
122	–
123	I/O
124	I/O
125	–
126	**GND**
127	**VCC**
128	I/O
129	I/O
130	–
131	–
132	–
133	I/O
134	I/O
135	I/O
136	I/O
137	I/O
138	I/O
139	I/O
140	I/O
141	I/O
142	I/O
143	**VCC**
144	**GND**

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

XC3390A, XC3390L, XC3490A Family
160-Pin PQFP Pinout

PQFP Pin Number	XC3390A/L, XC3490A
1	I/O
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	**GND**
20	**VCC**
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O
39	I/O
40	M1

PQFP Pin Number	XC3390A/L, XC3490A
41	**GND**
42	M0
43	**VCC**
44	I/O
45	HDC-I/O
46	I/O
47	I/O
48	I/O
49	$\overline{\text{LDC}}$-I/O
50	I/O
51	I/O
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	$\overline{\text{INIT}}$-I/O
60	**VCC**
61	**GND**
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	XTAL2-I/O
77	**GND**
78	$\overline{\text{RESET}}$
79	**VCC**
80	DONE/$\overline{\text{PG}}$

PQFP Pin Number	XC3390A/L, XC3490A
81	I/O
82	XTAL1-I/O-BCLKIN
83	I/O
84	I/O
85	I/O
86	I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	**VCC**
101	**GND**
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	I/O
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	I/O
119	DIN-I/O
120	DOUT

PQFP Pin Number	XC3390A/L, XC3490A
121	CCLK
122	**VCC**
123	**GND**
124	I/O
125	I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	I/O
131	I/O
132	I/O
133	I/O
134	I/O
135	I/O
136	I/O
137	I/O
138	I/O
139	**GND**
140	**VCC**
141	I/O
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	I/O
152	I/O
153	I/O
154	I/O
155	I/O
156	I/O
157	**VCC**
158	**GND**
159	$\overline{\text{PWRDWN}}$
160	TCLKIN-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed IOBs are default slew-rate limited.

XC3390A, XC3390L, XC3490A Family
175-Pin Plastic PGA Pinout

PGA Pin Number	XC3390A/L, XC3490A
B2	PWRDN
D4	TCLKIN-I/O
B3	I/O
C4	I/O
B4	I/O
A4	I/O
D5	I/O
C5	I/O
B5	I/O
A5	I/O
C6	I/O
D6	I/O
B6	I/O
A6	I/O
B7	I/O
C7	I/O
D7	I/O
A7	I/O
A8	I/O
B8	I/O
C8	I/O
D8	**GND**
D9	**VCC**
C9	I/O
B9	I/O
A9	I/O
A10	I/O
D10	I/O
C10	I/O
B10	I/O
A11	I/O
B11	I/O
D11	I/O
C11	I/O
A12	I/O
B12	I/O
C12	I/O
D12	I/O
A13	I/O
B13	I/O
C13	I/O
A14	I/O

PGA Pin Number	XC3390A/L, XC3490A
D13	I/O
B14	M1
C14	**GND**
B15	M0
D14	**VCC**
C15	I/O
E14	HDC-I/O
B16	I/O
D15	I/O
C16	I/O
D16	LDC-I/O
F14	I/O
E15	I/O
E16	I/O
F15	I/O
F16	I/O
G14	I/O
G15	I/O
G16	I/O
H16	I/O
H15	INIT-I/O
H14	**VCC**
J14	**GND**
J15	I/O
J16	I/O
K16	I/O
K15	I/O
K14	I/O
L16	I/O
L15	I/O
M16	I/O
M15	I/O
L14	I/O
N16	I/O
P16	I/O
N15	I/O
R16	I/O
M14	I/O
P15	XTAL2(IN)-I/O
N14	**GND**
R15	RESET
P14	**VCC**

PGA Pin Number	XC3390A/L, XC3490A
R14	DONE-PG
N13	I/O
T14	XTAL1(OUT)-BCLKIN-I/O
P13	I/O
R13	I/O
T13	I/O
N12	I/O
P12	I/O
R12	I/O
T12	I/O
P11	I/O
N11	I/O
R11	I/O
T11	I/O
R10	I/O
P10	I/O
N10	I/O
T10	I/O
T9	I/O
R9	I/O
P9	I/O
N9	**VCC**
N8	**GND**
P8	I/O
R8	I/O
T8	I/O
T7	I/O
N7	I/O
P7	I/O
R7	I/O
T6	I/O
R6	I/O
N6	I/O
P6	I/O
T5	I/O
R5	/O
P5	I/O
N5	I/O
T4	I/O
R4	I/O
P4	I/O

PGA Pin Number	XC3390A/L, XC3490A
R3	DIN-I/O
N4	DOUT-I/O
R2	CCLK
P3	**VCC**
N3	**GND**
P2	I/O
M3	I/O
R1	I/O
N2	I/O
P1	I/O
N1	I/O
L3	I/O
M2	I/O
M1	I/O
L2	I/O
L1	I/O
K3	I/O
K2	I/O
K1	I/O
J1	I/O
J2	I/O
J3	**GND**
H3	**VCC**
H2	I/O
H1	I/O
G1	I/O
G2	I/O
G3	I/O
F1	I/O
F2	I/O
E1	I/O
E2	I/O
F3	I/O
D1	I/O
C1	I/O
D2	I/O
B1	I/O
E3	I/O
C2	I/O
D3	**VCC**
C3	**GND**

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

Pins A2, A3, A15, A16, T1, T2, T3, T15 and T16 are not connected.
Pin A1 does not exist.

XC3390A, XC3390L, XC3490A Family
176-Pin TQFP Pinouts

Pin Number	XC3390A/L, XC3490A
1	$\overline{\text{PWRDWN}}$
2	TCLKIN-I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	**GND**
23	**VCC**
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	–

Pin Number	XC3390A/L, XC3490A
45	M1
46	**GND**
47	M0
48	**VCC**
49	I/O
50	I/O
51	I/O
52	I/O
53	I/O
54	I/O
55	–
56	I/O
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	I/O
65	$\overline{\text{INIT}}$-I/O
66	**VCC**
67	**GND**
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	–
83	–
84	I/O
85	XTAL2(IN)-I/O
86	**GND**
87	$\overline{\text{RESET}}$
88	**VCC**

Pin Number	XC3390A/L, XC3490A
89	DONE-$\overline{\text{PG}}$
90	I/O
91	XTAL1(OUT)-BCLKIN-I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	I/O
101	I/O
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	I/O
109	I/O
110	**VCC**
111	**GND**
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	I/O
119	I/O
120	I/O
121	I/O
122	I/O
123	I/O
124	I/O
125	I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	I/O
131	I/O
132	CCLK

Pin Number	XC3390A/L, XC3490A
133	**VSS**
134	**GND**
135	I/O
136	I/O
137	–
138	I/O
139	I/O
140	I/O
141	I/O
142	–
143	–
144	I/O
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	I/O
152	I/O
153	I/O
154	**GND**
155	**VCC**
156	I/O
157	I/O
158	I/O
159	I/O
160	–
161	–
162	I/O
163	I/O
164	I/O
165	I/O
166	I/O
167	I/O
168	–
169	I/O
170	I/O
171	I/O
172	I/O
173	I/O
174	I/O
175	**VCC**
176	**GND**

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

XC3390A, XC3390L, XC3490A Family
208-Pin PQFP Pinouts

Pin Number	XC3390A/L, XC3490A
1	–
2	GND
3	PWRDWN
4	TCLKIN-I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	–
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	**GND**
26	**VCC**
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	–
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	M1-RDATA
49	**GND**
50	M0-RTRIG
51	–
52	–

Pin Number	XC3390A/L, XC3490A
53	–
54	–
55	**VCC**
56	M2-I/O
57	HDC-I/O
58	I/O
59	I/O
60	I/O
61	LDC-I/O
62	I/O
63	I/O
64	–
65	–
66	–
67	–
68	I/O
69	I/O
70	I/O
71	I/O
72	–
73	–
74	I/O
75	I/O
76	I/O
77	I/O
78	**VCC**
79	**GND**
80	I/O
81	I/O
82	I/O
83	–
84	–
85	I/O
86	I/O
87	I/O
88	I/O
89	I/O
90	–
91	–
92	–
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	XLT2-I/O
101	**GND**
102	RESET
103	–
104	–

Pin Number	XC3390A/L, XC3490A
105	–
106	**VCC**
107	D/P
108	–
109	D7-I/O
110	XLT1-BCLKIN-I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	D6-I/O
116	I/O
117	I/O
118	I/O
119	–
120	I/O
121	I/O
122	D5-I/O
123	CS0-I/O
124	I/O
125	I/O
126	I/O
127	I/O
128	D4-I/O
129	I/O
130	**VCC**
131	**GND**
132	D3-I/O
133	CS1-I/O
134	I/O
135	I/O
136	I/O
137	I/O
138	D2-I/O
139	I/O
140	I/O
141	I/O
142	–
143	I/O
144	I/O
145	I/O
146	BUSY-RDY-RCLK-I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	DIN-D0-I/O
152	DOUT-I/O
153	CCLK
154	**VCC**
155	–
156	–

Pin Number	XC3390A/L, XC3490A
157	–
158	–
159	–
160	**GND**
161	WS-A0-I/O
162	CS2-A1-I/O
163	I/O
164	I/O
165	A2-I/O
166	A3-I/O
167	I/O
168	I/O
169	–
170	–
171	–
172	A15-I/O
173	A4-I/O
174	I/O
175	I/O
176	–
177	–
178	A14-I/O
179	A5-I/O
180	I/O
181	I/O
182	**GND**
183	**VCC**
184	A13-I/O
185	A6-I/O
186	I/O
187	I/O
188	–
189	–
190	I/O
191	I/O
192	A12-I/O
193	A7-I/O
194	–
195	–
196	–
197	I/O
198	I/O
199	A11-I/O
200	A8-I/O
201	I/O
202	I/O
203	A10-I/O
204	A9-I/O
205	**VCC**
206	–
207	–
208	–

XILINX®

XC3300 HardWire™ LCA Family

Product Specification

Features

- Mask-programmed versions of Xilinx Programmable Logic Cell Arrays (LCA)
  - Cost reduction for high volume applications
  - Transparent conversion from FPGA device
  - On-chip scan path test latches
  - High Performance 1.2 µ CMOS process
  - 100 MHz flip-flop toggle rate
- Easy conversion from Programmable FPGA
  - Architecturally identical to Programmable FPGA
  - Fully pin and performance compatible
  - Same specifications as Programmable FPGA
  - Supports daisy-chained configuration modes
  - Test program automatically generated
  - Emulates Programmable Configuration Signals
- Advanced Second Generation Architecture
  - Compatible arrays up to 9000 gate complexity
  - Extensive register and I/O capabilities
  - Two global clocks (less than 1 ns skew)
  - Internal 3-state bus capabilities
  - On-chip oscillator

Description

The Xilinx Logic Cell Array (LCA) family provides a group of high-performance, high-density digital integrated circuits. Their regular, extendable, flexible architecture is composed of three types of configurable elements: a perimeter of IOBs, a core array of CLBs and circuitry for interconnection. The general structure of a LCA device is shown in Figure 4.

The Xilinx XC3300 family of HardWire LCAs are mask programmed versions of the Xilinx XC3000 FPGAs. In high-volume applications where the design is stable, the programmable LCAs used for prototyping and initial production can be replaced by their HardWire LCA equivalents. This offers a significant cost reduction with virtually no risk or engineering resources required.

In a Programmable LCA the logic functions and interconnections are determined by the configuration program data loaded and stored in internal static memory cells. The HardWire LCA has architecture identical to the Programmable LCA it replaces. All CLBs, IOBs, interconnect topology, power distribution and other elements are the same. In the HardWire LCA the memory cells and the logic they control are replaced by metal connections. Thus the HardWire LCA is a semicustom device manufactured to provide a customer specific function, yet is completely compatible with the FPGA it replaces.

Xilinx manufactures the HardWire LCA using the information from the FPGA design file. Since the HardWire LCA device is both pinout and architecturally identical with the FPGA it is easily created without the need for all the costly and time-consuming engineering activities which other semicustom solutions would require. No redesign time; no expensive and time consuming simulation runs; no place and route; no test vector generation. The combination of the Programmable LCA and HardWire LCA products simply offer the fastest and easiest way to get your product to market, and ensures a subsequent low-cost, low-risk high-volume cost reduction path.

Electrical Characteristics

The XC3300 HardWire LCA family is form, fit and function compatible with the XC3000 FPGA family. Accordingly, all XC3300 HardWire devices meet the electrical specifications of the respective XC3000 FPGA device for the -100

HardWire Device	Replacement for Pin-Compatible Programmable Device	Total Available Gates	File Submitted to Xilinx	Maximum Flip-Flop Toggle Frequency	Packages									
					PLCC				TQFP VQFP	PQFP			PPGA	
					Pins	44	68	84	100	100	160	208	132	175
XC3330	XC3020, XC3030	3000	3030.LCA	100 MHz	I/Os	34	58	74	80	80	–	–	–	–
XC3342	XC3042	4200	3042.LCA	100 MHz		–	58	74	82	82	–	–	–	–
XC3390	XC3064, XC3090	9000	3090.LCA	100 MHz		–	–	70	–	–	138	144	110	144

device for the -100 Speed Grade. For specific data, please see the XC3000 section of the Xilinx Programmable Logic Data Book. Absolute Maximum Ratings, Operating Conditions, DC Characteristics and Switching Characteristics of the -100 Speed Grade of the appropriate device type apply.

HardWire LCA Application

HardWire LCA products are designed to provide a simple, low-risk path for a customer to achieve significant cost-reductions on a high-volume design which initially used the FPGA. In the prototype and early production stages, and for low to moderate volume applications, the Programmable device is the solution of choice. Later in the life cycle - when the design is stable and goes into high-volume production - the HardWire LCA can be used in place of the original Programmable device.

Figure 1 shows the typical life cycle of a high-volume product, and illustrates the optimal way for using the FPGA and HardWire LCA. During the development and prototype stages the Programmable device is used.

Production is started using a Programmable device and the design includes a method for storing the configuration bitstream. Using a Programmable device at this stage reduces risk, allows a faster time to market, and permits design modifications to be made without obsoleting any LCA devices. After a few months of production with the Programmable device, the HardWire LCA can be substituted in the circuit. This may also permit removal of an EPROM used for bitstream storage.

Since the circuit board was designed initially for a Programmable device, production can be switched back if the situation warrants. For example, if demand for the product increases dramatically, production can be increased in days or weeks by using Programmable devices. A change can be quickly made to the product with a Programmable device. There is no manufacturing leadtime with off-the-shelf, standard product Programmable devices. As another example, production can be switched to Programmable devices as the product nears the end of the life cycle. This avoids end-of-life buys and the risk of obsolescence.

HardWire LCA Design/Production Interface

Figure 2 shows how the design, development and production activities are sequenced for both the Programmable and HardWire products. Notice that no additional activity is needed for the HardWire LCA until the design is in volume production. At that time there is a simple design analysis (done by Xilinx) prior to generating the custom mask, and then the HardWire prototypes are manufactured. An in-system verification is performed by the customer, and the HardWire LCA is released to full production. As the architectures of the FPGA and HardWire LCAs are identical, virtually no engineering resources are needed to move from one to the other. By comparison, a traditional masked gate array attempting to "assemble" these logic functions from NAND gates to emulate the LCA would require extensive design activity. A comparison of the activities required to convert to a HardWire LCA versus a gate array is shown in Figure 3.

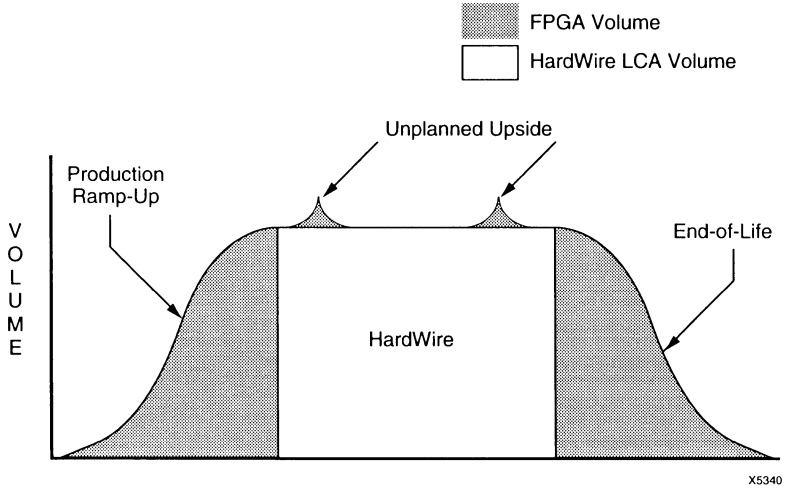


Figure 1. Typical High-Volume Product Life Cycle

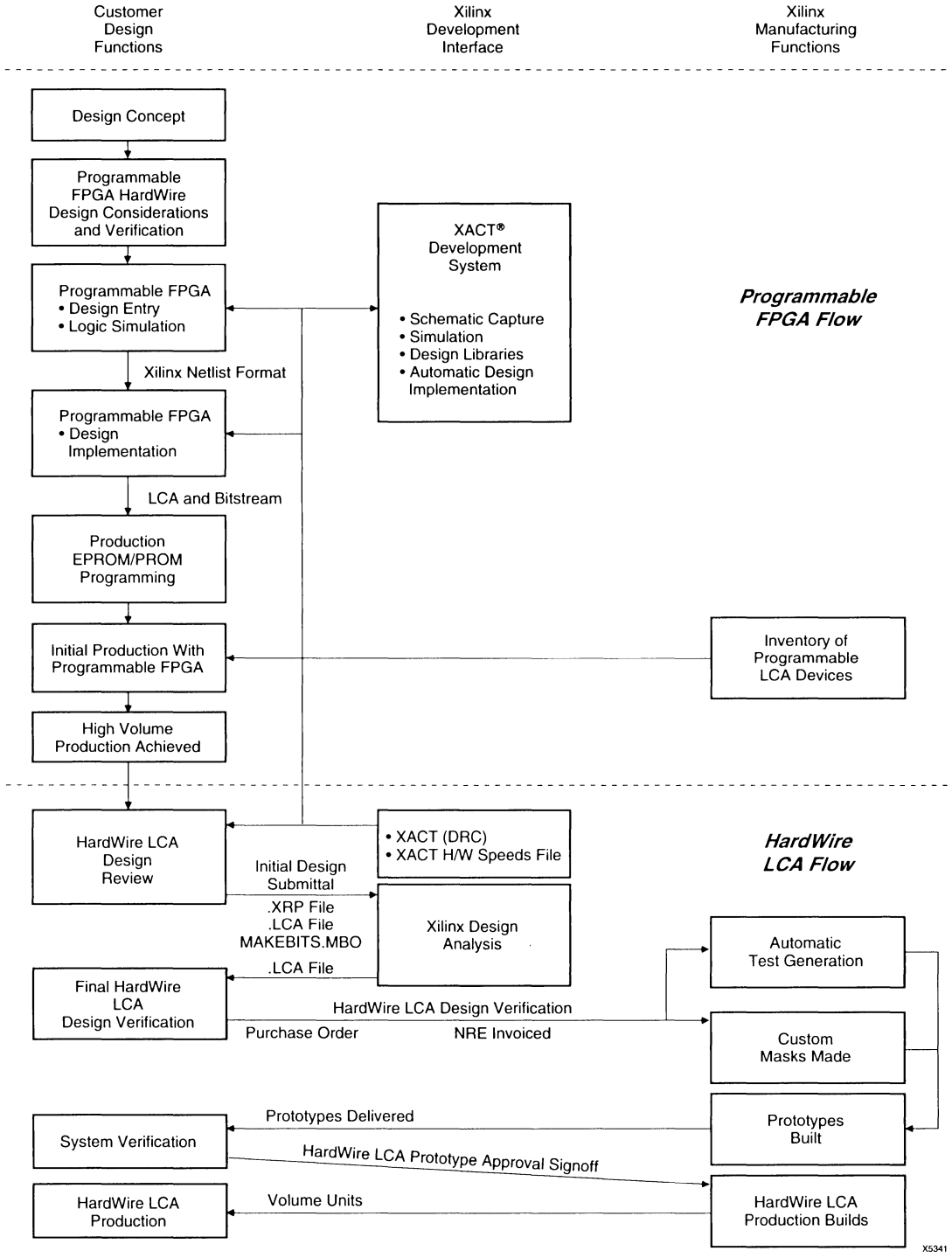


Figure 2. Programmable/HardWire Design/Production Interface.

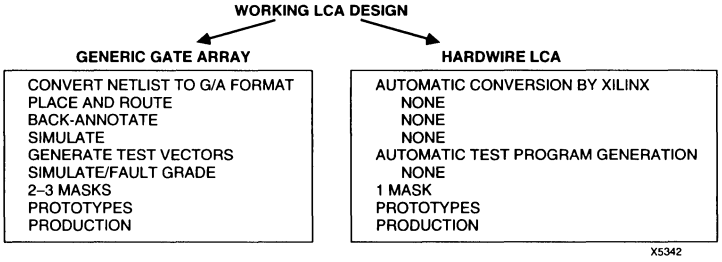


Figure 3. Design Flow Comparison: Gate Array versus Hardwire LCA.

Architecture

As shown in Figure 4, the HardWire LCA has the same architecture as the FPGA it replaces. The perimeter of I/O Blocks (IOBs) provides an interface between the internal logic array and the device package pins. The array of Configurable Logic Blocks (CLBs) performs user-specified logic functions. The interconnect resources are programmed to form networks carrying logic signals among blocks, analogous to printed circuit board traces connecting SSI/MSI packages.

The logic functions of the blocks are implemented by look-up tables. Functional options are implemented by user-defined multiplexers. Interconnecting networks between blocks are implemented with user-defined fixed metal connections.

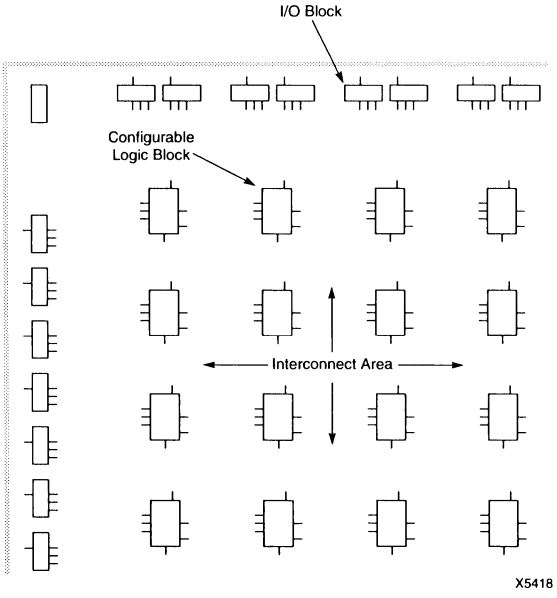


Figure 4. Logic Cell Array Structure

I/O Block

Each user-defined IOB (shown in Figure 5) provides an interface between the external package pin of the device and the internal user logic. The IOB is identical with that used in the FPGA. There are a wide variety of I/O options available to the user.

Summary of I/O Options

- Inputs
  - Direct
  - Flip-flop/latch
  - CMOS/TTL threshold (chip inputs)
  - Pull-up resistor/open circuit
- Outputs
  - Direct/registered
  - Inverted/not
  - 3-state/on/off
  - Full speed/slew limited
  - 3-state/output enable (inverse)

Configurable Logic Block

The array of Configurable Logic Blocks (CLBs) provides the functional elements from which the user's logic is constructed. The logic blocks are arranged in a matrix within the perimeter of IOBs. For example, the XC3330 has 100 such blocks arranged in 10 rows and 10 columns.

The configurable logic block is identical to that used in the XC3000 family of FPGAs. Each configurable logic block has a combinatorial logic section, two flip-flops, and an internal control section. (See Figure 6.) There are: five logic inputs [*.a*, *.b*, *.c*, *.d* and *.e*]; a common clock input [*.k*]; an asynchronous direct reset input [*.rd*]; and an enable clock [*.ec*]. All may be driven from the interconnect resources adjacent to the blocks. Each CLB also has two outputs [*.x* and *.y*] which may drive interconnect networks.

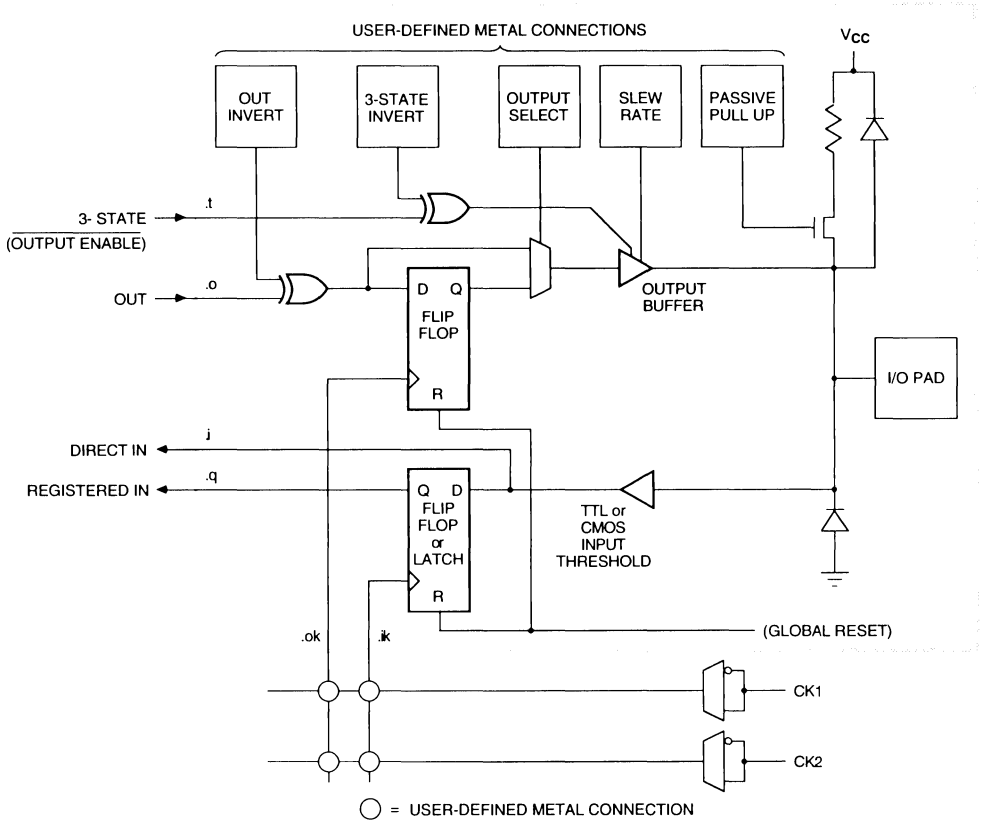


Figure 5. Input/Output Block. Each IOB includes input and output storage elements and I/O options pre-defined by the user. A choice of two clocks is available on each die edge. The polarity of each clock line (not each flip-flop or latch) is selectable. A clock line that triggers the flip-flop on the rising edge is an active Low Latch Enable (Latch transparent) signal and vice versa. Passive pull-up can only be enabled on inputs, not on outputs. All user inputs are selectable for TTL or CMOS thresholds.

Interconnect

User-defined interconnect resources in the Logic Cell Array provide routing paths to connect inputs and outputs of the I/O and logic blocks into logic networks. Interconnections between blocks are composed from a two-layer grid of metal segments. The XACT development system provides automatic routing of these interconnections. The inputs of the IOBs and CLBs are multiplexers that are defined to select an input network from the adjacent interconnect segments.

Three types of metal resources are provided to accommodate various network interconnect requirements:

- General Purpose Interconnect
- Direct Connection
- Long Lines

The topology of all these interconnect resources is identical with that of the FPGA, but the speed of the interconnect paths is significantly faster (since all interconnections are fixed metal connections).

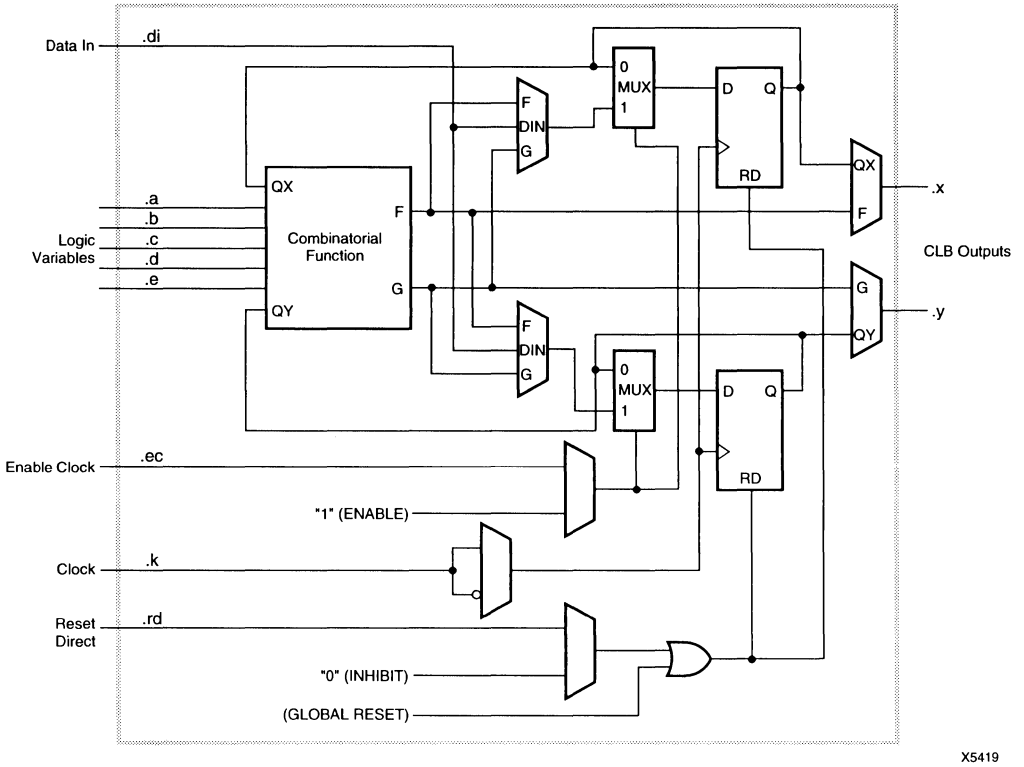


Figure 6. Configurable Logic Block. Each CLB includes a combinatorial logic section, two flip-flops and a user-defined multiplexer selection of function.

It has: five logic variable inputs .a, .b, .c, .d and .e.
a direct data in .di
an enable clock .ec
a clock (invertible) .k
an asynchronous reset .rd
two outputs .x and .y

Configuration and Start-Up

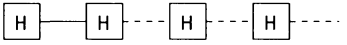
The XC3300 family of HardWire LCA devices are designed to be fully compatible with their Programmable LCA equivalents. While the HardWire LCA parts do not require the loading of configuration data, they fully support a wide variety of configuration modes.

Configuration

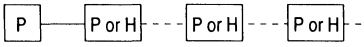
HardWire LCA devices can be used stand-alone or in a daisy chain with other LCAs. A HardWire LCA device cannot act in Master Parallel or Peripheral Mode. However, designs which use these modes can be supported by selection of a mask option which forces the device into Master Mode. (See Mask Option Applications Note page 4-3 for further information). This allows the HardWire LCA to be used when the original design used Peripheral Mode, without requiring any changes to the circuit board.

Mode 1. As a stand alone HardWire LCA Device.

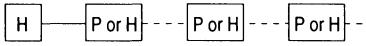
Mode 2. As a daisy chain of all HardWire LCA Devices.



Mode 3. As a HardWire LCA or programmable slave in a daisy chain with a Programmable device as a master.



Mode 4. As a HardWire Gate Array device acting as a Serial Master with any combination of Programmable and HardWire LCA devices as slaves.



(P = Programmable device, H = HardWire Gate Array device)

X5346

An XC3300 HardWire LCA device will not "swallow" its own configuration data. Whatever configuration bits are fed into the DIN pin will appear on the DOUT pin after a delay TDIO. In any case where a HardWire LCA device is ahead of a Programmable device in a daisy chain (as in Mode 3 and 4 shown above) the configuration data will need to be modified.

Start-up Sequence

The XC3300 HardWire LCAs are designed to emulate the start-up sequence of the FPGA devices as closely as possible, however, some differences do exist. The start-up sequence may be thought of as three stages: power-on-reset; internal clear; and configuration.

An internal power-on-reset circuit is triggered when power is applied. When VCC reaches the voltage at which portions of the LCA begin to operate, the device generates a POR (power-on reset) pulse. The I/O output buffers are disabled and a high-impedance pull-up resistor is provided for the user I/O pins. The length of the POR pulse is user-defined to be either 64 µs or 16 ms. The 64 µs pulse is used for a rapid reset cycle; the 16 ms pulse emulates the power-on sequence of a FPGA. If the M0 pin is held Low during the POR cycle (or if the mask option to force the HardWire LCA into Master Mode is selected) the device will operate as a Master Mode device and the POR pulse will be extended to 4 times its nominal delay. This ensures that all daisy-chained slave devices will have sufficient time to power up.

Following the POR cycle, the HardWire LCA enters a "clearing" state. This state emulates the configuration memory clear performed by a FPGA upon power-up. The length of the clear cycle is 256 cycles (nominally 256 µs) for a standard POR, but is only 2 cycles if the rapid reset cycle was selected.

At the completion of the clear cycle the $\overline{\text{RESET}}$ pin is sampled. If the $\overline{\text{RESET}}$ pin is being held Low, the "configuration" will be delayed (with the $\overline{\text{INIT}}$ pin held Low) until $\overline{\text{RESET}}$ is driven High. If the $\overline{\text{RESET}}$ pin is being driven High (or once it has been driven High following a delayed "configuration") the open drain $\overline{\text{INIT}}$ pin will be released and the value of the M0 pin will be latched. If the device is in Master Mode (M0 = Low) it will begin to produce CCLKs. If the device is in Slave Mode (M0 = High) it will require CCLKs to be supplied from another device. After 4 CCLK cycles the part is "configured" and the Done/Program (D/P) pin will be released. (If the device is in a daisy chain with the D/$\overline{\text{P}}$ pins tied together the D/$\overline{\text{P}}$ pin will remain Low until all devices have completed configuration.) One CCLK after the D/$\overline{\text{P}}$ pin goes High the I/Os will become active. The internal user-logic reset is user-defined to release either one CCLK cycle before or after the I/O pins become active. A HardWire LCA operating in Master Mode will stop producing CCLKs one cycle after the I/Os become active.

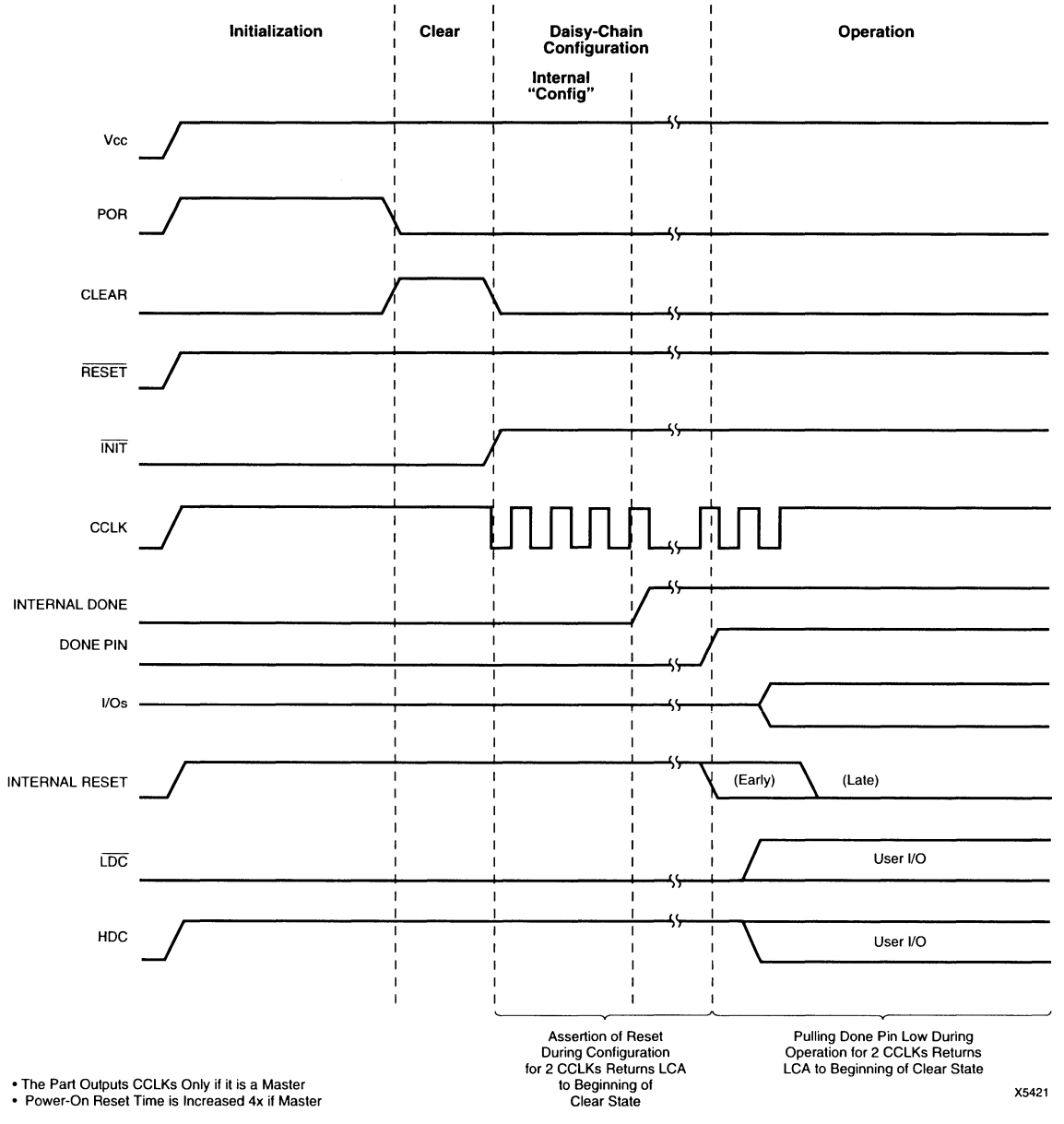


Figure 7. Psuedo-Configuration Waveform (Normal Power-Up)

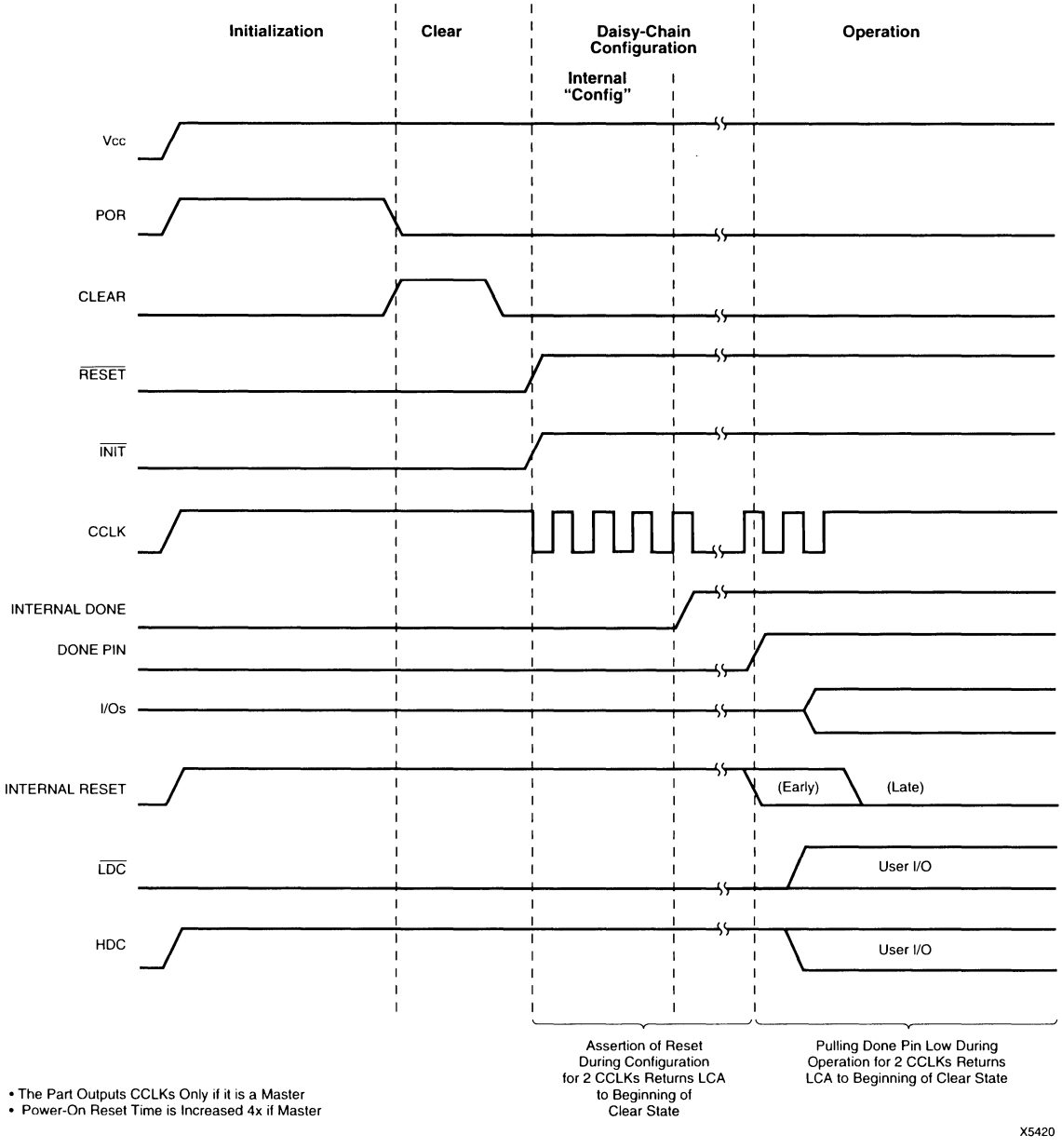


Figure 8. Psuedo-Configuration Waveform (Configuration Delay by Reset)

Performance

The XC3300 family of HardWire LCAs are manufactured in the same high-performance 1.2µ CMOS technology as their FPGA equivalents. Traditionally the toggle frequency of a flip-flop has been used to describe the overall performance of a semi-custom device. The configuration used for determining this rate is shown in Figure 9.

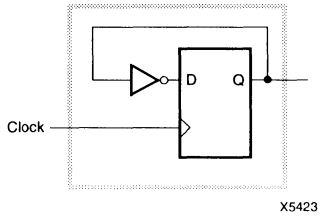


Figure 9. Toggle Flip-Flop. This is used to characterize device performance.

Actual LCA performance is determined by the timing of critical paths, including the timing for the logic and storage elements in that path and the timing of the associated interconnect. HardWire LCA logic block performance is equal to or slightly faster than the equivalent FPGA, while the interconnect performance is significantly faster.

All HardWire LCA devices are specified and tested for operation at the fastest equivalent FPGA speed available at the time the HardWire LCA device is introduced. For the XC3300 family, this means all parts are guaranteed to the -100 speed grade.

Power

Power for the LCA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the LCA, dedicated V_{CC} and ground rings surround the logic array and provide power to the I/O drivers. (See Figure 10.) An independent matrix of V_{CC} and ground lines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically a 0.1-µF capacitor connected near the V_{CC} and ground pins will provide adequate decoupling.

Output buffers capable of driving the specified 4-mA loads under worst-case conditions may be capable of driving 25 to 30 times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads. The I/O Block output buffers have a slew-limited mode which should be used where output rise and fall times are not speed critical. Slew-limited outputs maintain their dc drive capability, but generate less external reflections and internal noise. A maximum total external capacitive load for simultaneous fast mode switching in the same direction is 500 pF per power/ground pin pair. For slew-rate limited outputs this total is four times larger.

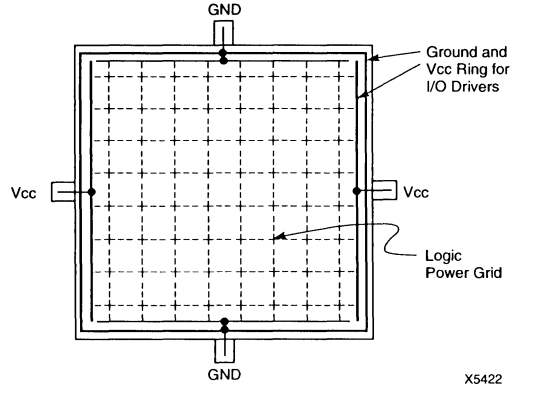


Figure 10. LCA Power Distribution.

HardWire LCA Design Considerations

It is important to observe good design practices while using HardWire LCAs. It is possible for a programmable device to "hide" some less obvious design shortcomings. However, these can manifest themselves when the design is converted to a HardWire LCA.

For example, a small glitch generated from unstable inputs to a CLB function block can be easily "swallowed" if the output is driving a long net. This is because the "pass transistors" act as a Low pass filter and this net's loads may never see the glitch. However, in a HardWire LCA, this glitch may propagate to the loads since there are only metal lines and vias in the routing path.

Gated Clocks and Reset Directs

Glitching function generators driving CLOCK and RESET DIRECT pins can inadvertently trigger flip-flops to an undesirable state. Avoid these so-called "gated" clock and reset direct nets; if unavoidable, design the logic so that the inputs are always stable and the signal changes are at least a CLB delay (T_{ILO}) apart.

Multiplexers Implemented in Function Generators

Two input multiplexers can be easily implemented in a single F or G function genterator. However, there is a possibility of a glitch if the selected signal and the selected input changes within a CLB's T_{ILO} delay. This is generally not a problem with data and address multiplexers as long as the output is given enough time to settle; but if the multiplexer output is feeding a CLOCK and/or a RESET DIRECT pin, it is possible to toggle the register at undesired times.

The edge(s) of select signals for a CLOCK and/or RESET DIRECT multiplexers should be stable before and after the edges of the inputs. The edges should be at least a CLB (T_{ILO}) delay apart.

Race Conditions

All race conditions in the circuit need to go through a careful analysis. Depending on the routing resources responsible for the net delays, the correct signal may always "win the race" in a programmable FPGA; however, once converted to HardWire LCA, this may not be the case. (See Figure 10a.)

Delay Generators

Using the routing resources as delay lines in programmable FPGAs is undesirable. In HardWire LCAs, it is an invitation for timing problems. All delay generators should be removed and the circuit redesigned before converting it to HardWire.

Interfacing with External Devices

Almost all LCAs interface with external devices–FIFOs, memories, processors and peripherals, etc. Handshaking with devices requires specific setup/hold times. Ample hold time on a data bus from a programmable FPGA may no longer meet spec in HardWire LCA. An external data bus clocked by a HardWire LCA gererated signal may no longer meet the system set-up time requirements. This can happen because interconnects are much faster than in a programmable device. This requires you to also review the system timing specs when converting to a HardWire LCA.

In reality, all designers using LCAs (programmable or HardWire) face the same issues. Due to improvements in process and circuit design, a part specified at -50 today may actually be running as fast as -70 or even close to -100 in the future. Xilinx does NOT guarantee a part against minimum timing specs. A "glitch" that was swallowed in a device today may crop up in a future device due to faster pass resistors in the routing paths. When using any Xilinx LCAs, the above issues should be addressed in the design phase.

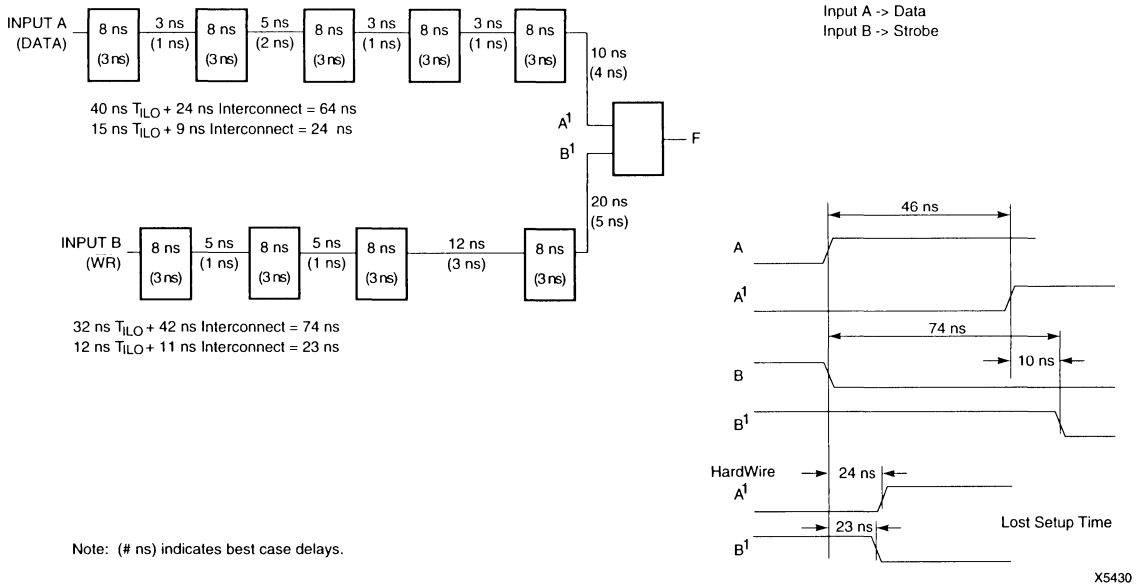


Figure 10a. Race Condition Example

HardWire Testability

The XC3300 HardWire LCA products contain significant on-chip logic to facilitate manufacturability and testing. This logic, combined with Xilinx's internal Automatic Test Generation (ATG) software, assures 100% functionality. In fact, the HardWire LCA can be 100% functionally tested by Xilinx without the need for customer generated test vectors (as is required with custom gate arrays).

This section examines the two basic block structures and the special test circuitry in the HardWire LCA. An example of a small XC3300 LCA design and the vectors generated for test are included.

Test Architecture

The HardWire LCA contains two types of internal blocks: the Input/Output Block (IOB) and the Configurable Logic Block (CLB). To accomplish 100% functional testing special test circuitry is designed into the device. This circuitry allows testing of each block (CLB and IOB) in a synchronized procedure known as "Scan Test". Special dedicated test latches (called TBLKs) are included on all HardWire devices. They are completely transparent to the normal operation of the circuit. Scan testing allows the contents of all internal flip-flops to be serially shifted off-chip, and for Xilinx generated test vectors to be shifted into the device, thus enabling all flip-flops to be initialized to any desired state.

These special dedicated test latches are placed into each CLB and IOB. Each CLB has four internal test latches, (placed at the CLB outputs), while each IOB contains three test latches (placed at the IOB inputs) as shown in Figures 11 and 12. The placement of these test latches is very important, since each CLB output or IOB input can fanout to multiple destinations. All sources and destinations of logic blocks come from other logic blocks, thus this placement of the latches provides complete access to all nets and synchronized control of all CLBs and IOBs.

The test latches are connected into a daisy chain which passes through every flip-flop in the LCA. Figure 13 shows an overview of the scan path. The path begins at the Scan In pin, sequences through each CLB, then through the IOBs, and finally exits at the Scan Out pin. This scan path can be seen in more detail in Figure 14, which shows the precise sequence with which the CLB and IOB internal test latches are loaded or read.

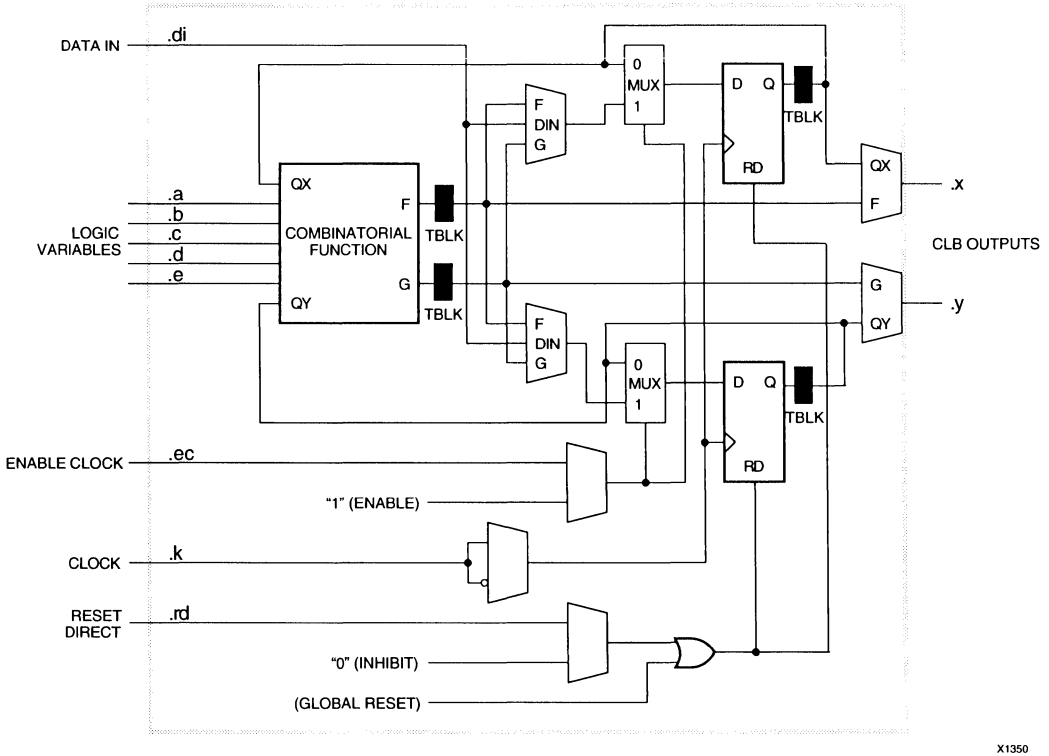


Figure 11. XC3300 HardWire CLB Test Latch Locations

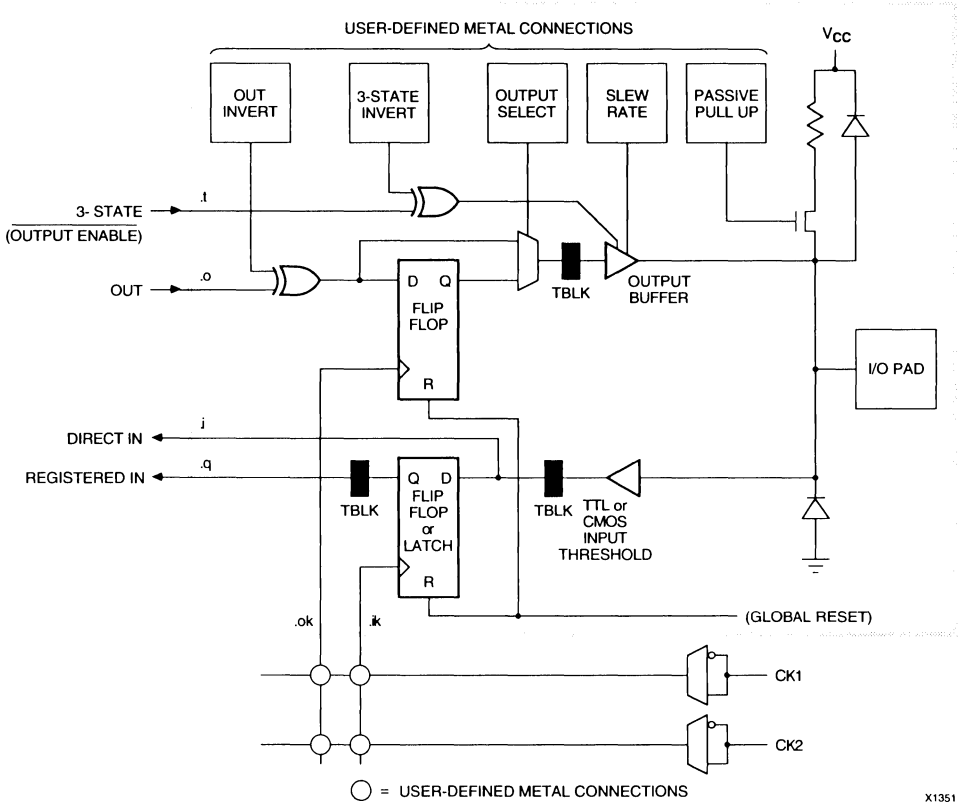


Figure 12. XC3300 HardWire IOB Test Latch Location

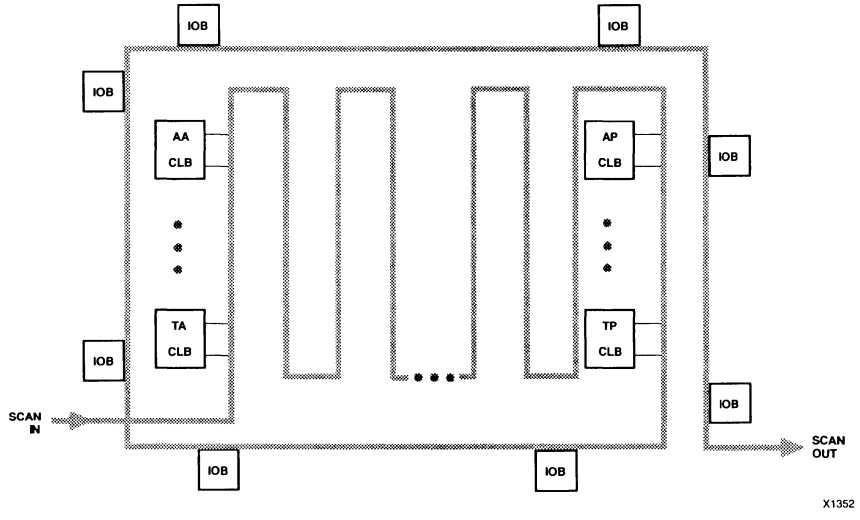


Figure 13. XC3390 Scan Path Overview

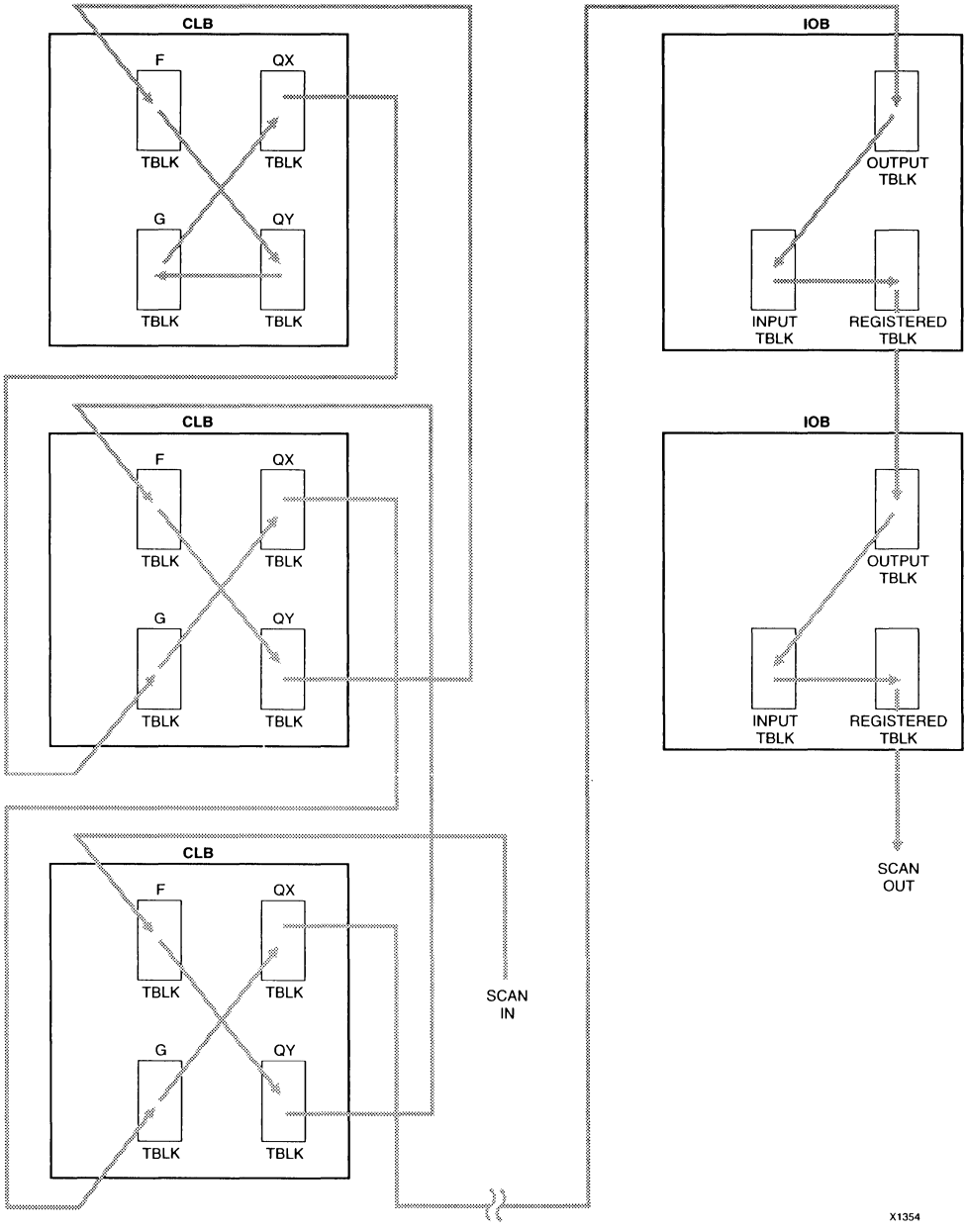


Figure 14. Detailed Scan Path

The internal architecture of a TBLK is shown in Figure 15. In the normal operation mode of the HardWire LCA, SW1 is in position A and all the test latches are bypassed completely. The HardWire LCA device is set into Test Mode (SW1 = position B) by Xilinx ATG software. This software inputs unique conditions on several control pins while serially loading a "password" into the device. For this reason, it is not possible for a customer design to inadvertently place the HardWire LCA into Test Mode. When SW1 is in position B (Test Mode) all the latches can receive data from either the CLB output or the previous latch in the daisy chain (SQn).

Synchronized together by a special test clock, all the test latches operate in two phases. The first phase serially loads all the latches to place a specific vector at the inputs of the logic block to be tested. The second phase is a parallel load of all latches, storing the expected output data of the logic block being tested (SW2 = A). At this point testing returns to phase one and serially clocks out the results, while simultaneously clocking in a new input vector.

Scan Test

To see how scan testing can be used to provide complete functional test coverage, consider the logic shown in Figure 16. This diagram shows a CLB (CLB2) with three inputs being driven by three different CLBs and the other two inputs being driven by two different IOBs. If we apply every possible combination of inputs to CLB2 and all expected output conditions are met, then CLB2 has been 100% functionally tested. The input conditions applied also include any register control signals (such as Clock, Reset, or Clock Enable). The same procedure is used for testing IOBs.

Looking again at Figure 16, CLB2 is tested by first serially loading the X output latches of CLB1, CLB3, and CLB4 and the input latches of IOB1 and IOB2. Note that the latches on CLB2's outputs are also loaded in this first phase. Not all CLBs and IOBs can be tested at once, due to signal dependencies. To position the correct data into the latches all unused latches still need "don't cares" loaded. Regardless of which CLBs and IOBs are being tested by a particular scan vector, the complete scan path is always shifted in and out for testing and verification. The state of CLB2's output latches will be opposite to their expected results in phase two. This guarantees that CLB2's input data changed the state of its output latches and therefore, is current data.

CLB or IOB data registers using a synchronous or asynchronous clock are not a problem during this special test mode. All customer-used registers are clock inhibited during the phase one load. The inhibit of register clocking is accomplished by logically "ANDing" the register clocks with the global inhibit control line.

The test vectors needed to perform this thorough testing are created by Xilinx. No additional effort or engineering time is required from the user to ensure proper device performance. The customer design file used to create the HardWire LCA is used in conjunction with specially developed Xilinx Automatic Test Generation software, which creates the complete set of test vectors required to perform 100% functional testing. This software creates the data for all possible input conditions and corresponding output data for each CLB and IOB used in the customer design. This data is then compiled into the test vectors used to perform the actual testing.

Scan Test Example

Finally, Figure 17 shows an example of a very simple design implemented in an XC3300 HardWire LCA. This example uses only two CLBs and one IOB, and therefore contains only 11 test latches. The sample test vectors in Figure 18 show how scan test would be used to perform functional testing of this design. Note that the set of vectors shown tests only one input condition (input A of the CLB under test). The actual test file would contain all the additional vectors needed to completely test this design.

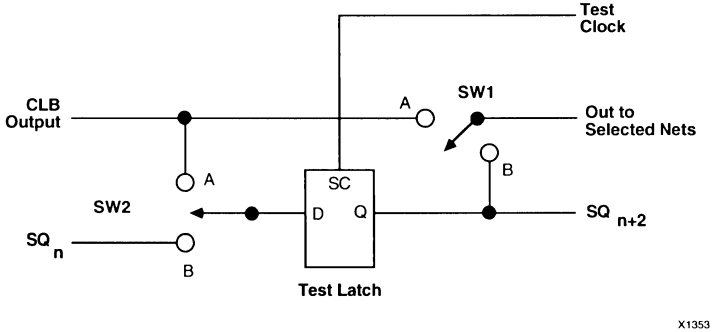


Figure 15. TBLK Block Diagram

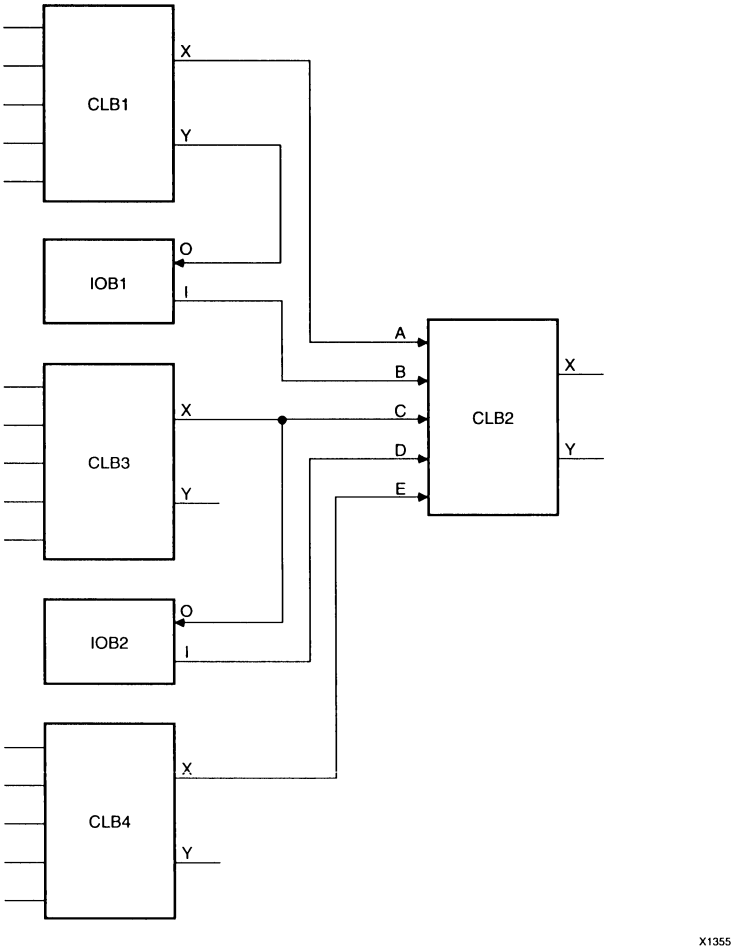


Figure 16. 5 Input CLB (CLB2) Driven by 3 Different CLB Outputs and 2 Different IOB Inputs

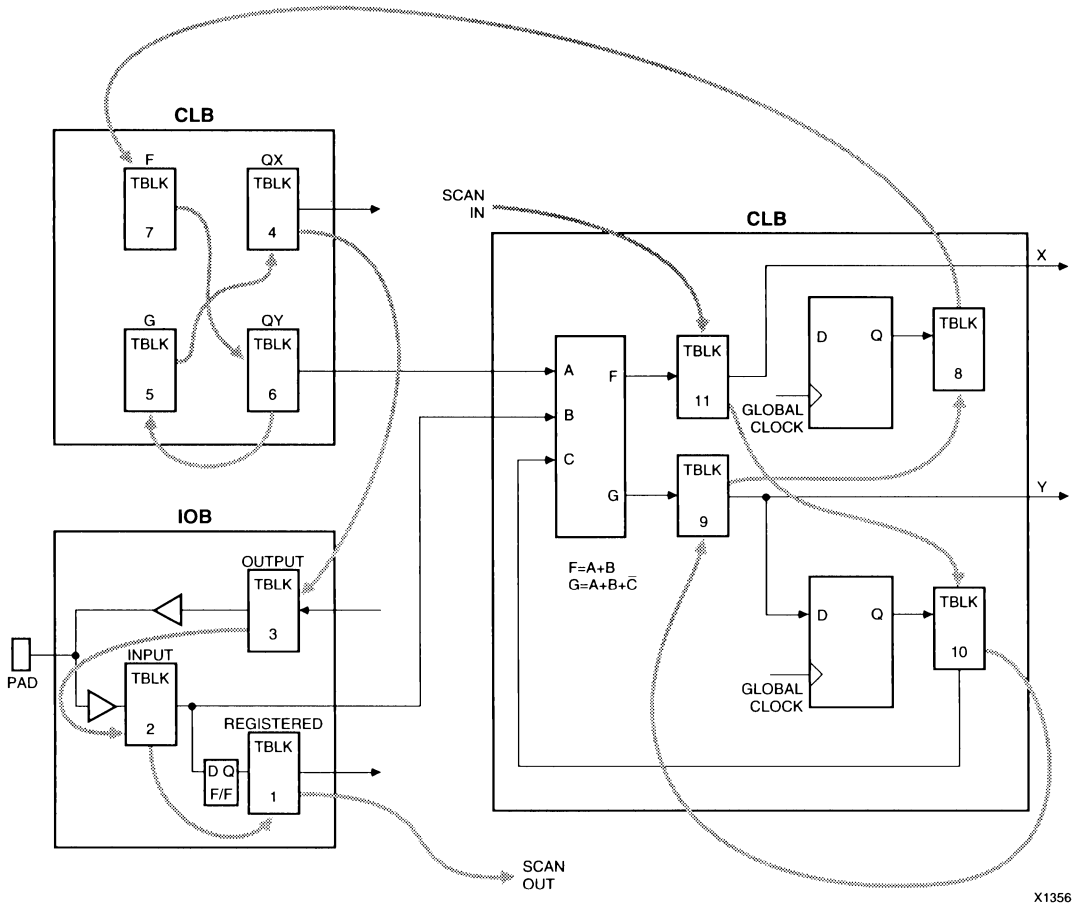


Figure 17. Test Example

The following vectors and comments show the testing of one input condition (input A of the CLB under test).

SCAN CLOCK	SCAN IN	SCAN OUT	GLOBAL CLOCK	COMMENTS
c	x	x	x	Load a "don't care" (0 or 1) into latch #1, not used.
c	1	x	x	Load a 1 into Scan In pin, knowing it will be positioned in latch #2, input B. The global clock is inhibited and the scan out data are "don't cares".
c	x	x	x	Load a "don't care" into latch #3, not used.
c	x	x	x	Load a "don't care" into latch #4, not used.
c	x	x	x	Load a "don't care" into latch #5, not used.
c	1	x	x	Load a 1 into Scan In pin for input A (latch #6).
c	x	x	x	Load a "don't care" into latch #7, not used.
c	x	x	x	Load a "don't care" into latch #8, not used.
c	0	x	x	Load a 0 into latch #9, expecting the G output to be a 1 after phase two.
c	0	x	x	Load a 0 into latch #10, expecting the register output to be a 1 after phase two.
c	0	x	x	Load a 0 into latch #11, exepcting the F output to be a 1 after phase two.
At this point all the latches are loaded. Enter phase two by changing the control pin (not shown here).				
0	x	x	c	Clock the data register after entering phase two. Now the register data is current but latch #10 still has a 0 inside.
c	x	x	0	Load all the latches with their functional results.
This completes phase two. Return to phase one and load the next set of input data, while simultaneously verifying the scan out pin. We expect to see latches 9, 10, and 11 with ones as we scan the data out.				
c	x	x	x	Load a "don't care" into latch #1, not used.
c	1	x	x	Load a 1 into Scan In pin, knowing it will be positioned in latch #2, input B.
c	x	x	x	Load a "don't care" into latch #3, not used.
c	x	x	x	Load a "don't care" into latch #4, not used.
c	x	x	x	Load a "don't care" into latch #5, not used.
c	0	x	x	Load a 0 into Scan In pin for input A (latch #6). This is a different from the first load.
c	x	x	x	Load a "don't care" into latch #7, not used.
c	x	x	x	Load a "don't care" into latch #8, not used.
c	1	1	x	Load a 1 into latch #9, expecting the G output to be a 0 after phase two. The Scan out pin will be showing the results of latch #9 from the previous load.
c	0	1	x	Load a 0 into latch #10, expecting the register output to be a 1 after phase two. The Scan out pin shows latch #10 results.
c	0	1	x	Load a 0 into latch #11, expecting the F output to be a 1 after phase two. The Scan out pin shows latch #11 results.

Figure 18. Sample Test Vectors for Simple Design Example

XC3300 Family Configuration Pin Assignments

CONFIGURATION MODE: <M0>											
SLAVE <1>	MASTER <0>	44 PLCC	68 PLCC	84 PLCC	100 PQFP	100 TQFP/ VQFP	132 PPGA	160 PQFP	208 PQFP	175 PPGA	USER OPERATION
PWR DWN	PWR DWN	7	10	12	29	26	A1	159	3	B2	PWR DWN (I)
VCC	VCC	12	18	22	41	38	C8	20	26	D9	VCC
M1 (I)	M1 (I)	16	25	31	52	49	B13	40	48	B14	M1
M0 (HIGH) (I)	M0 (HIGH) (I)	17	26	32	54	51	B14	42	50	B15	M0 (I)
		18	27	33	56	53	D14	44	56	C15	I/O
HDC (HIGH)	HDC (HIGH)	19	28	34	57	54	G14	45	57	C15	I/O
LDC (LOW)	LDC (LOW)	20	30	36	59	56	H12	49	61	D16	I/O
$\overline{\text{INIT}}$ *	$\overline{\text{INIT}}$ *	22	34	42	65	62	M13	59	77	H15	I/O
GND	GND	23	35	43	66	63	P14	19	79	J14	GND
		26	43	53	67	73	N13	76	100	P15	XTL2 or I/O
$\overline{\text{RESET}}$ (I)	$\overline{\text{RESET}}$ (I)	27	44	54	78	75	P14	78	102	R15	$\overline{\text{RESET}}$ (I)
DONE	DONE	28	45	55	80	77	N13	80	107	R14	PROGRAM (I)
			46	56	81	78	M12	81	109	N13	I/O
		30	47	57	82	79	P13	82	110	T14	XTL1 or I/O
			48	58	83	80	N11	86	115	P12	I/O
			49	60	87	84	M9	92	122	T11	I/O
			50	61	88	85	N9	93	123	R10	I/O
			51	62	89	86	N8	98	128	R9	I/O
VCC	VCC	34	52	64	91	88	M8	100	130	N9	VCC
			53	65	92	89	N7	102	132	P8	I/O
			54	66	93	90	P6	103	133	R8	I/O
			55	67	94	91	M6	108	138	R7	I/O
			56	70	98	95	M5	114	145	R5	I/O
			57	71	99	96	N4	115	146	P5	I/O
DIN (I)	DIN (I)	38	58	72	100	97	N2	119	151	R3	I/O
DOUT	DOUT	39	59	73	1	98	M3	120	152	N4	I/O
CCLK (I)	CCLK	40	60	74	2	99	P1	121	153	R2	CCLK (I)
			61	75	5	2	M2	124	161	P2	I/O
			62	76	6	3	N1	125	162	M3	I/O
			63	77	8	5	L2	128	165	P1	I/O
			64	78	9	6	L1	129	166	N1	I/O
			65	81	12	9	K1	132	172	M1	I/O
			66	82	13	10	J2	133	173	L2	I/O
			67	83	14	11	H1	136	178	K2	I/O
			68	84	15	12	H2	137	179	K1	I/O
GND	GND	1	1	1	16	13	H3	139	182	J3	GND
			2	2	17	14	G2	141	184	H2	I/O
			3	3	18	15	G1	142	185	H1	I/O
			4	4	19	16	F2	147	192	F2	I/O
			5	5	20	17	E1	148	193	E1	I/O
			6	8	23	20	D1	151	199	D1	I/O
			7	9	24	21	D2	152	200	C1	I/O
			8	10	25	22	B1	155	203	E3	I/O
			9	11	26	26	C2	156	204	C2	I/O
		X	X	X	X	X					XC3330
				X	X	X					XC3342
				X			X	X	X	X	XC3390

Represents a 50-kΩ to 100-kΩ Pull-Up

* INIT is an Open Drain Output During Configuration

(I) Represents an Input

X5475

Note: Pin assignments of "PGA Footprint" PLCC sockets and PGA packages are not electically identical.
Generic I/O pins are not shown

XC3000 Family Pin Assignments

Xilinx offers the three members of the XC3300 family in a variety of surface-mount and through-hole package types, with pin counts from 44 to 208.

Each chip is offered in several package types to accomodate the available pc board space and manufacturing technology. Most package types are also offered with different chips to accommodate design changes without the need for pc board changes.

Note that there may not be a perfect match between the number of bonding pads on the chip and the number of pins on a package. In some cases, the chip has more pads than there are pins on the package, as indicated by the information ("unused" pads) below the line in the following table. The IOBs of the unconnected pads can still be used as storage elements if the specified propagation delays and set-up times are acceptable.

In other cases, the chip has fewer pads than there are pins on the package; therefore, some package pins are not connected (n.c.), as shown above the line in the following table.

		Number of Package Pins							
Device	**Pads**	**44**	**68**	**84**	**100**	**132**	**160**	**175**	**208**
XC3330	98	54 unused	30 unused	14 unused	2 n.c.	—	—	—	—
XC3342	118	—	—	34 unused	18 unused	—	—	—	—
XC3390	166	—	—	82 unused	—	32 unused	6 unused	9 n.c.	42 n.c.

Pin Descriptions

Permanently Dedicated Pins.

V_{CC}
Two to eight (depending on package type) connections to the nominal +5 V supply voltage. All must be connected.

GND
Two to eight (depending on package type) connections to ground. All must be connected.

$\overline{PWRDWN}$
A Low on this CMOS-compatible input stops all internal activity. All flip-flops and latches are reset, all outputs are 3-stated, and all inputs are interpreted as High, independent of their actual level. While $\overline{PWRDWN}$ is Low, V_{CC} may be reduced to any value >2.3 V. When $\overline{PWDWN}$ returns High, the LCA becomes operational with DONE Low for two cycles of the internal 1-MHz clock. During configuration, $\overline{PWRDWN}$ must be High. If not used, $\overline{PWRDWN}$ must be tied to V_{CC}.

$\overline{RESET}$
This is an active Low input which has three functions.

Prior to the start of configuration, a Low input will delay the start of the configuration process. An internal circuit senses the application of power and begins a minimal time-out cycle. When the time-out and $\overline{RESET}$ are complete, the level of the M0 line is sampled and configuration begins.

If $\overline{RESET}$ is asserted during a configuration, the LCA device is re-initialized and restarts the configuration at the termination of $\overline{RESET}$.

If $\overline{RESET}$ is asserted after configuration is complete, it provides a global asynchronous reset of all IOB and CLB storage elements of the LCA device.

CCLK
During configuration, Configuration Clock is an output of an LCA in Master mode or Peripheral mode, but an input in Slave mode.

CCLK drives dynamic circuitry inside the LCA. The Low time may, therefore, not exceed a few microseconds. When used as an input, CCLK must be "parked High". An internal pull-up resistor maintains High when the pin is not being driven.

DONE/$\overline{PROG}$
DONE is an open-drain output, configurable with or without an internal pull-up resistor. At the completion of configuration, the LCA circuitry becomes active in a synchronous order, and DONE/$\overline{PROG}$ goes active High one cycle before the outputs go active.

Once configuration is done, a High-to-Low transition of this pin will cause an initialization of the device and start a reconfiguration.

M0

As Mode 0, this input sampled is before the start of configuration to establish the configuration mode to be used.

M1

This input is used only for manufacturer test. The user must tie this pin either High or Low in-system.

User I/O Pins that can have special functions.

HDC

During configuration, this output is held at a High level to indicate that configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin.

LDC

During Configuration, this output is held at a Low level to indicate that the configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin. LDC is particularly useful in Master mode as a Low enable for an EPROM, but it must then be programmed as a High after configuration.

INIT

This is an active Low open-drain output which is held Low during the power stabilization and internal clearing of the configuration memory. It can be used to indicate status to a configuring microprocessor, as a wired AND of several slave mode devices, or as a hold-off signal for a master mode device. After configuration this pin becomes a user programmable I/O pin.

BCLKIN

This is a direct CMOS level input to the alternate clock buffer (Auxiliary Buffer) in the lower right corner.

XTL1

This user I/O pin can be used to operate as the output of an amplifier driving an external crystal and bias circuitry.

XTL2

This user I/O pin can be used as the input of an amplifier connected to an external crystal and bias circuitry. The I/O Block is left unconfigured. The oscillator configuration is activated by routing a net from the oscillator buffer symbol output.

DIN

During Slave or Master Serial configuration, this pin is used as a serial-data input.

DOUT

During configuration this pin is used to output serial-configuration data to the DIN pin of a daisy-chained slave.

TCLKIN

This is a direct CMOS level input to the global clock buffer.

Unrestricted User I/O Pins.

I/O

An I/O pin may be programmed by the user to be an Input or an Output pin following configuration. All unrestricted I/O pins, plus the special pins mentioned previously, have a weak pull-up resistor of 50 kΩ to 100 kΩ that becomes active as soon as the device powers up, and stays active until the end of configuration.

XC3300 Family 44-Pin PLCC Pinouts

Pin Number	XC3300
1	GND
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	PWRDWN
8	I/O
9	I/O
10	I/O
11	I/O
12	VCC
13	I/O
14	I/O
15	I/O
16	M1-RDATA
17	M0-RTRIG
18	M2-I/O
19	HDC-I/O
20	LDC-I/O
21	I/O
22	INIT-I/O

Pin Number	XC3300
23	GND
24	I/O
25	I/O
26	XTL2(IN)-I/O
27	RESET
28	DONE-PGM
29	I/O
30	XT1(OUT)-BCLK-I/O
31	I/O
32	I/O
33	I/O
34	VCC
35	I/O
36	I/O
37	I/O
38	DIN-I/O
39	DOUT-I/O
40	CCLK
41	I/O
42	I/O
43	I/O
44	I/O

XC3300 Family 68-Pin and 84-Pin PLCC Pinouts

XC3330, XC3342	68 PLCC	84 PLCC
PWRDN	10	12
TCLKIN-I/O	11	13
I/O		14
I/O	12	15
I/O	13	16
I/O	—	17
I/O	14	18
I/O	15	19
I/O	16	20
I/O	17	21
VCC	18	22
I/O	19	23
I/O	—	24
I/O	20	25
I/O	21	26
I/O	22	27
I/O	—	28
I/O	23	29
I/O	24	30
M1	25	31
M0	26	32
I/O	27	33
HDC-I/O	28	34
I/O	29	35
LDC-I/O	30	36
I/O	31	37
I/O		38
I/O	32	39
I/O	33	40
I/O		41
INIT-I/O	34	42
GND	35	43
I/O	36	44
I/O	37	45
I/O	38	46
I/O	39	47
I/O	40	48
I/O	41	49
I/O		50
I/O		51
I/O	42	52
XTL2(IN)-I/O	43	53

XC3330, XC3342	68 PLCC	84 PLCC
RESET	44	54
DONE-PG	45	55
I/O	46	56
XTL1(OUT)-BCLKIN-I/O	47	57
I/O	48	58
I/O	—	59
I/O	49	60
I/O	50	61
I/O	51	62
I/O	—	63
VCC	52	64
I/O	53	65
I/O	54	66
I/O	55	67
I/O	—	68
I/O		69
I/O	56	70
I/O	57	71
DIN-I/O	58	72
DOUT-I/O	59	73
CCLK	60	74
I/O	61	75
I/O	62	76
I/O	63	77
I/O	64	78
I/O		79
I/O		80
I/O	65	81
I/O	66	82
I/O	67	83
I/O	68	84
GND	1	1
I/O	2	2
I/O	3	3
I/O	4	4
I/O	5	5
I/O		6
I/O		7
I/O	6	8
I/O	7	9
I/O	8	10
I/O	9	11

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

This table describes the pinouts of two different chips in two different packages. The first column lists 84 of the 118 pads on the XC3342 (and 84 of the 98 pads on the XC3330) that are connected to the 84 package pins. Six pads, indicated by a dash (–) in the 68 PLCC column, have no connections in the 68 PLCC package, but are connected in the 84-pin package.

XC3390 84-Pin PLCC Pinout

PLCC Pin Number	XC3390
12	PWRDN
13	TCLKIN-I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	**GND***
22	**VCC**
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	M1
32	M0
33	I/O
34	HDC-I/O
35	I/O
36	LDC-I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	INIT/I/O*
42	**VCC***
43	**GND**
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	I/O
53	XTL2(IN)-I/O

PLCC Pin Number	XC3390
54	RESET
55	DONE-PG
56	I/O
57	XTL1(OUT)-BCLKIN-I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	**VCC**
65	**GND***
66	I/O*
67	I/O*
68	I/O*
69	I/O
70	I/O
71	I/O
72	DIN-I/O
73	DOUT-I/O
74	CCLK
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	I/O
84	I/O
1	**GND**
2	**VCC***
3	I/O*
4	I/O*
5	I/O*
6	I/O*
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed ouptuts are default slew-rate limited.

* Different pin definition than XC3342 PC84 package

XC3300 Family 100-Pin PQFP, TQFP, VQFP Pinouts

TQFP/ VQFP Pin No.	PQFP Pin No.	XC3330 XC3342
13	16	**GND**
14	17	I/O
15	18	I/O
16	19	I/O
17	20	I/O
18	21	I/O
19	22	I/O
20	23	I/O
21	24	I/O
22	25	I/O
23	26	I/O
24	27	**VCC**
25	28	**GND**
26	29	$\overline{\text{PWRDN}}$
27	30	TCLKIN-I/O
28	31	I/O**
29	32	I/O
30	33	I/O
31	34	I/O
32	35	I/O
33	36	I/O
34	37	I/O
35	38	I/O
36	39	I/O
37	40	I/O
38	41	**VCC**
39	42	I/O
40	43	I/O
41	44	I/O
42	45	I/O
43	46	I/O
44	47	I/O
45	48	I/O
46	49	I/O

TQFP/ VQFP Pin No.	PQFP Pin No.	XC3330 XC3342
47	50	I/O
48	51	I/O
49	52	**M1**
50	53	**GND**
51	54	**M0**
52	55	**VCC**
53	56	I/O
54	57	HDC-I/O
55	58	I/O
56	59	$\overline{\text{LDC}}$-I/O
57	60	I/O
58	61	I/O
59	62	I/O
60	63	I/O
61	64	I/O
62	65	$\overline{\text{INIT}}$-I/O
63	66	GND
64	67	I/O
65	68	I/O
66	69	I/O
67	70	I/O
68	71	I/O
69	72	I/O
70	73	I/O
71	74	I/O
72	75	I/O
73	76	XTAL2-I/O
74	77	**GND**
75	78	$\overline{\text{RESET}}$
76	79	**VCC**
77	80	DONE-$\overline{\text{PG}}$
78	81	I/O
79	82	BCLKIN-XTAL1-I/O
80	83	I/O

TQFP/ VQFP Pin No.	PQFP Pin No.	XC3330 XC3342
81	84	I/O
82	85	I/O
83	86	I/O
84	87	I/O
85	88	I/O
86	89	I/O
87	90	I/O
88	91	**VCC**
89	92	I/O
90	93	I/O
91	94	I/O
92	95	I/O
93	96	I/O
94	97	I/O
95	98	I/O
96	99	I/O
97	100	DIN-I/O
98	1	DOUT-I/O
99	2	CCLK
100	3	**VCC**
1	4	**GND**
2	5	I/O
3	6	I/O
4	7	I/O**
5	8	I/O
6	9	I/O
7	10	I/O
8	11	I/O
9	12	I/O
10	13	I/O
11	14	I/O
12	15	I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

This table describes the pinouts of two different chips in two different packages. The third column lists 100 of the 118 pads on the XC3342 that are connected to the 100 package pins. Two pads, indicated by double asterisks, do not exist on the XC3330, which has 98 pads; therefore the corresponding pins have no connections.

XC3300 Family 132-Pin Plastic PGA Pinout

PGA Pin Number	XC3390
C4	**GND**
A1	PWRDN
C3	I/O-TCLKIN
B2	I/O
B3	I/O
A2	I/O
B4	I/O
C5	I/O
A3	I/O
A4	I/O
B5	I/O
C6	I/O
A5	I/O
B6	I/O
A6	I/O
B7	I/O
C7	**GND**
C8	**VCC**
A7	I/O
B8	I/O
A8	I/O
A9	I/O
B9	I/O
C9	I/O
A10	I/O
B10	I/O
A11	I/O
C10	I/O
B11	I/O
A12	I/O
B12	I/O
A13	I/O
C12	I/O

PGA Pin Number	XC3390
B13	M1
C11	**GND**
A14	M0
D12	**VCC**
C13	I/O
B14	HDC-I/O
C14	I/O
E12	I/O
D13	I/O
D14	LDC-I/O
E13	I/O
F12	I/O
E14	I/O
F13	I/O
F14	I/O
G13	I/O
G14	INIT-I/O
G12	**VCC**
H12	**GND**
H14	I/O
H13	I/O
J14	I/O
J13	I/O
K14	I/O
J12	I/O
K13	I/O
L14	I/O
L13	I/O
K12	I/O
M14	I/O
N14	I/O
M13	XTAL2(IN)-I/O
L12	**GND**

PGA Pin Number	XC3390
P14	RESET
M11	**VCC**
N13	DONE-PG
M12	I/O
P13	XTAL1-I/O-BCLKIN
N12	I/O
P12	I/O
N11	I/O
M10	I/O
P11	I/O
N10	I/O
P10	I/O
M9	I/O
N9	I/O
P9	I/O
P8	I/O
N8	I/O
P7	I/O
M8	**VCC**
M7	**GND**
N7	I/O
P6	I/O
N6	I/O
P5	I/O
M6	I/O
N5	I/O
P4	I/O
P3	I/O
M5	I/O
N4	I/O
P2	I/O
N3	I/O
N2	DIN-I/O

PGA Pin Number	XC3390
M3	DOUT-I/O
P1	CCLK
M4	**VCC**
L3	**GND**
M2	I/O
N1	I/O
M1	I/O
K3	I/O
L2	I/O
L1	I/O
K2	I/O
J3	I/O
K1	I/O
J2	I/O
J1	I/O
H1	I/O
H2	I/O
H3	**GND**
G3	**VCC**
G2	I/O
G1	I/O
F1	I/O
F2	I/O
E1	I/O
F3	I/O
E2	I/O
D1	I/O
D2	I/O
E3	I/O
C1	I/O
B1	I/O
C2	I/O
D3	**VCC**

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

XC3300 Family 160-Pin PQFP Pinout

PLCC Pin Number	XC3390
1	I/O
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	**GND**
20	**VCC**
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O
39	I/O
40	M1

PLCC Pin Number	XC3390
41	**GND**
42	M0
43	**VCC**
44	I/O
45	HDC-I/O
46	I/O
47	I/O
48	I/O
49	$\overline{\text{LDC}}$-I/O
50	I/O
51	I/O
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	INIT-I/O
60	**VCC**
61	**GND**
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	XTAL2-I/O
77	**GND**
78	RESET
79	**VCC**
80	DONE/PG

PLCC Pin Number	XC3390
81	I/O
82	XTAL1-I/O-BCLKIN
83	I/O
84	I/O
85	I/O
86	I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	**VCC**
101	**GND**
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	I/O
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	I/O
119	DIN-I/O
120	DOUT

PLCC Pin Number	XC3390
121	CCLK
122	**VCC**
123	**GND**
124	I/O
125	I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	I/O
131	I/O
132	I/O
133	I/O
134	I/O
135	I/O
136	I/O
137	I/O
138	I/O
139	**GND**
140	**VCC**
141	I/O
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	I/O
152	I/O
153	I/O
154	I/O
155	I/O
156	I/O
157	**VCC**
158	**GND**
159	$\overline{\text{PWRDWN}}$
160	TCLKIN-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed IOBs are default slew-rate limited.

XC3390 Family 175-Pin Plastic PGA Pinout

PGA Pin Number	XC3390
B2	PWRDN
D4	TCLKIN-I/O
B3	I/O
C4	I/O
B4	I/O
A4	I/O
D5	I/O
C5	I/O
B5	I/O
A5	I/O
C6	I/O
D6	I/O
B6	I/O
A6	I/O
B7	I/O
C7	I/O
D7	I/O
A7	I/O
A8	I/O
B8	I/O
C8	I/O
D8	**GND**
D9	**VCC**
C9	I/O
B9	I/O
A9	I/O
A10	I/O
D10	I/O
C10	I/O
B10	I/O
A11	I/O
B11	I/O
D11	I/O
C11	I/O
A12	I/O
B12	I/O
C12	I/O
D12	I/O
A13	I/O
B13	I/O
C13	I/O
A14	I/O

PGA Pin Number	XC3390
D13	I/O
B14	M1
C14	**GND**
B15	M0
D14	**VCC**
C15	I/O
E14	HDC-I/O
B16	I/O
D15	I/O
C16	I/O
D16	LDC-I/O
F14	I/O
E15	I/O
E16	I/O
F15	I/O
F16	I/O
G14	I/O
G15	I/O
G16	I/O
H16	I/O
H15	INIT-I/O
H14	**VCC**
J14	**GND**
J15	I/O
J16	I/O
K16	I/O
K15	I/O
K14	I/O
L16	I/O
L15	I/O
M16	I/O
M15	I/O
L14	I/O
N16	I/O
P16	I/O
N15	I/O
R16	I/O
M14	I/O
P15	XTAL2(IN)-I/O
N14	**GND**
R15	RESET
P14	**VCC**

PGA Pin Number	XC3390
R14	DONE-PG
N13	I/O
T14	XTAL1(OUT)-BCLKIN-I/O
P13	I/O
R13	I/O
T13	I/O
N12	I/O
P12	I/O
R12	I/O
T12	I/O
P11	I/O
N11	I/O
R11	I/O
T11	I/O
R10	I/O
P10	I/O
N10	I/O
T10	I/O
T9	I/O
R9	I/O
P9	I/O
N9	**VCC**
N8	**GND**
P8	I/O
R8	I/O
T8	I/O
T7	I/O
N7	I/O
P7	I/O
R7	I/O
T6	I/O
R6	I/O
N6	I/O
P6	I/O
T5	I/O
R5	/O
P5	I/O
N5	I/O
T4	I/O
R4	I/O
P4	I/O

PGA Pin Number	XC3390
R3	DIN-I/O
N4	DOUT-I/O
R2	CCLK
P3	**VCC**
N3	**GND**
P2	I/O
M3	I/O
R1	I/O
N2	I/O
P1	I/O
N1	I/O
L3	I/O
M2	I/O
M1	I/O
L2	I/O
L1	I/O
K3	I/O
K2	I/O
K1	I/O
J1	I/O
J2	I/O
J3	**GND**
H3	**VCC**
H2	I/O
H1	I/O
G1	I/O
G2	I/O
G3	I/O
F1	I/O
F2	I/O
E1	I/O
E2	I/O
F3	I/O
D1	I/O
C1	I/O
D2	I/O
B1	I/O
E3	I/O
C2	I/O
D3	**VCC**
C3	**GND**

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

Pins A2, A3, A15, A16, T1, T2, T3, T15 and T16 are not connected.
Pin A1 does not exist.

XC3390 Family 208-Pin PQFP Pinouts

Pin Number	XC3390	Pin Number	XC3390	Pin Number	XC3390	Pin Number	XC3390
1	–	53	–	105	–	157	–
2	GND	54	–	106	VCC	158	–
3	PWRDWN	55	VCC	107	D/P	159	–
4	TCLKIN-I/O	56	M2-I/O	108	–	160	GND
5	I/O	57	HDC-I/O	109	D7-I/O	161	WS-A0-I/O
6	I/O	58	I/O	110	XLT1-BCLKIN-I/O	162	CS2-A1-I/O
7	I/O	59	I/O	111	I/O	163	I/O
8	I/O	60	I/O	112	I/O	164	I/O
9	I/O	61	LDC-I/O	113	I/O	165	A2-I/O
10	I/O	62	I/O	114	I/O	166	A3-I/O
11	I/O	63	I/O	115	D6-I/O	167	I/O
12	I/O	64	–	116	I/O	168	I/O
13	I/O	65	–	117	I/O	169	–
14	I/O	66	–	118	I/O	170	–
15	–	67	–	119	–	171	–
16	I/O	68	I/O	120	I/O	172	A15-I/O
17	I/O	69	I/O	121	I/O	173	A4-I/O
18	I/O	70	I/O	122	D5-I/O	174	I/O
19	I/O	71	I/O	123	CS0-I/O	175	I/O
20	I/O	72	–	124	I/O	176	–
21	I/O	73	–	125	I/O	177	–
22	I/O	74	I/O	126	I/O	178	A14-I/O
23	I/O	75	I/O	127	I/O	179	A5-I/O
24	I/O	76	I/O	128	D4-I/O	180	I/O
25	GND	77	I/O	129	I/O	181	I/O
26	VCC	78	VCC	130	VCC	182	GND
27	I/O	79	GND	131	GND	183	VCC
28	I/O	80	I/O	132	D3-I/O	184	A13-I/O
29	I/O	81	I/O	133	CS1-I/O	185	A6-I/O
30	I/O	82	I/O	134	I/O	186	I/O
31	I/O	83	–	135	I/O	187	I/O
32	I/O	84	–	136	I/O	188	–
33	I/O	85	I/O	137	I/O	189	–
34	I/O	86	I/O	138	D2-I/O	190	I/O
35	I/O	87	I/O	139	I/O	191	I/O
36	I/O	88	I/O	140	I/O	192	A12-I/O
37	–	89	I/O	141	I/O	193	A7-I/O
38	I/O	90	–	142	–	194	–
39	I/O	91	–	143	I/O	195	–
40	I/O	92	–	144	I/O	196	–
41	I/O	93	I/O	145	I/O	197	I/O
42	I/O	94	I/O	146	BUSY-RDY-RCLK-I/O	198	I/O
43	I/O	95	I/O	147	I/O	199	A11-I/O
44	I/O	96	I/O	148	I/O	200	A8-I/O
45	I/O	97	I/O	149	I/O	201	I/O
46	I/O	98	I/O	150	I/O	202	I/O
47	I/O	99	I/O	151	DIN-D0-I/O	203	A10-I/O
48	M1-RDATA	100	XLT2-I/O	152	DOUT-I/O	204	A9-I/O
49	GND	101	GND	153	CCLK	205	VCC
50	M0-RTRIG	102	RESET	154	VCC	206	–
51	–	103	–	155	–	207	–
52	–	104	–	156	–	208	–

XILINX®

XC2318 HardWire™ LCA Family

Product Specification

Features

- Mask-programmed version of Xilinx Field Programmable Gate Arrays (FPGA)
  - Cost reduction for high volume applications
  - Transparent conversion from FPGA device
  - On-chip scan path test latches
  - High Performance 1.5 µ CMOS process
  - 70 MHz flip-flop toggle rate
- Easy conversion from Programmable FPGA
  - Architecturally identical to Programmable FPGA
  - Pin and performance compatible
  - Same specifications as Programmable FPGA
  - Supports daisy-chained configuration
  - Test program automatically generated
- Flexible High-Performance Architecture
  - User-definable I/O functions
  - 100% factory tested
  - Low-power CMOS technology
  - Complete development system support

Description

The Xilinx Logic Cell Array family provides a group of high-performance, high-density digital integrated circuits. Their regular, extendable, flexible architecture is composed of three types of configurable elements: a perimeter of IOBs, a core array of CLBs and circuitry for interconnection. The general structure of a Logic Cell Array device is shown in Figure 4.

The Xilinx XC2318 HardWire LCA device is a mask programmed version of the Xilinx XC2018 FPGA. In high-volume applications where the design is stable, the FPGAs used for prototyping and initial production can be replaced by their HardWire LCA equivalents. This offers a significant cost reduction with virtually no risk or engineering resources required.

In an FPGA device the logic functions and interconnections are determined by the configuration program data loaded and stored in internal static memory cells. The HardWire LCA architecture identical to the FPGA it replaces. All CLBs, IOBs, interconnect topology, power distribution and other elements the same. In the HardWire LCA the memory cells and the logic they control are replaced by metal connections. Thus the HardWire LCA is a semicustom device manufactured to provide a customer specific function, yet is completely compatible with the FPGA device it replaces.

Xilinx manufactures the HardWire LCA using information from the FPGA design file. Since the HardWire LCA device is both pinout and architecturally identical with the FPGA, it is easily created without the need for all the costly and time-consuming engineering activities which other semicustom solutions would require. No redesign time; no expensive and time consuming simulation runs; no place and route; no test vector generation. The combination of the Programmable and HardWire LCA products simply offer the fastest and easiest way to get your product to market, and ensures a subsequent low-cost, low-risk high-volume cost reduction path.

Electrical Characteristics

The XC3300 HardWire LCA family is form, fit and function compatible with the XC3000 FPGA family. Accordingly, all

HardWire Device	Replacement for Pin-Compatible Programmable Device	Total Available Gates	File Submitted to Xilinx	Maximum Flip-Flop Toggle Frequency	Packages						
						VQFP	PLCC		PQFP		TQFP VQFP
					Pins	64	68	84	64	100	100
XC2318	XC2018, XC2064	1800	2018.LCA	70 MHz	I/Os	54	58	74	54	74	74

Accordingly, all XC3300 HardWire devices meet the electrical specifications of the respective XC3000 FPGA device for the -100 Speed Grade. For specific data, please see the XC3000 section of the Xilinx Programmable Logic Data Book. Absolute Maximum Ratings, Operating Conditions, DC Characteristics and Switching Characteristics of the -100 Speed Grade of the appropriate device type apply.

HardWire LCA Application

HardWire LCA products are designed to provide a simple, low-risk path for a customer to achieve significant cost-reductions on a high-volume design which initially used the Programmable FPGA. In the prototype and early production stages, and for low to moderate volume applications, the FPGA is the solution of choice. Later in the life cycle - when the design is stable and reaches high-volume production - the HardWire device can be used in place of the original FPGA device.

Figure 1 shows the typical life cycle of a high-volume product, and illustrates the optimal way for using the Programmable and HardWire LCAs. During the development and prototype stages the FPGA is used.

Production is started using a Programmable device and the design includes a method for storing the configuration bitstream. Using an FPGA at this stage reduces risk, allows a faster time to market, and permits design modifications to be made without obsoleting any LCA devices. After a few months of production with the Programmable device, the HardWire LCA device can be substituted in the circuit. This may also permit removal of an EPROM used for bitstream storage.

Since the circuit board was designed initially for a Programmable device, production can be switched back if the situation warrants. For example, if demand for the product increases dramatically, production can be increased in days or weeks by using Programmable devices. A change can be quickly made to the product with a Programmable device. There is no manufacturing leadtime with off-the-shelf, standard product FPGA devices. As another example, production can be switched to Programmable devices as the product nears the end of the life cycle. This avoids end-of-life buys and the risk of obsolescence.

HardWire LCA Design/Production Interface

Figure 2 shows how the design, development and production activities are sequenced for both the Programmable and HardWire products. Notice that no additional activity is needed for the HardWire LCA device until the design is in volume production. At that time there is a simple design analysis (done by Xilinx) prior to generating the custom mask, and then the HardWire LCA prototypes are manufactured. An in-system verification is performed by the customer, and the HardWire LCA device is released to full production. As the architectures of the Programmable and HardWire LCA are identical, virtually no engineering resources are needed to move from one to the other. By comparison, a traditional masked gate array attempting to "assemble" these logic functions from NAND gates to emulate the LCA would require extensive design activity. A comparison of the activities required to convert to a HardWire LCA versus a generic gate array is shown in Figure 3.

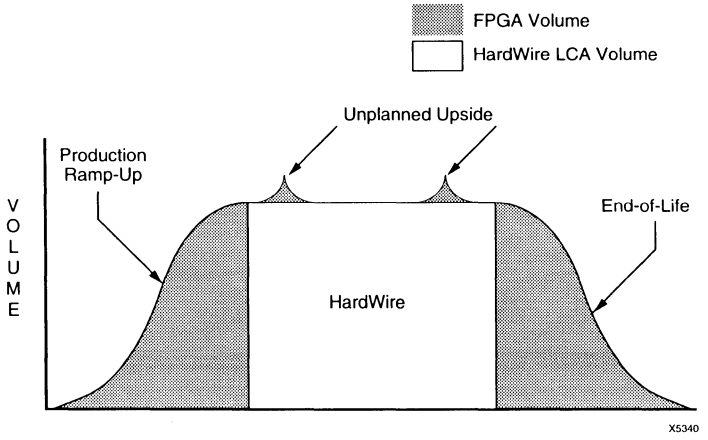


Figure 1. Typical High-Volume Product Life Cycle

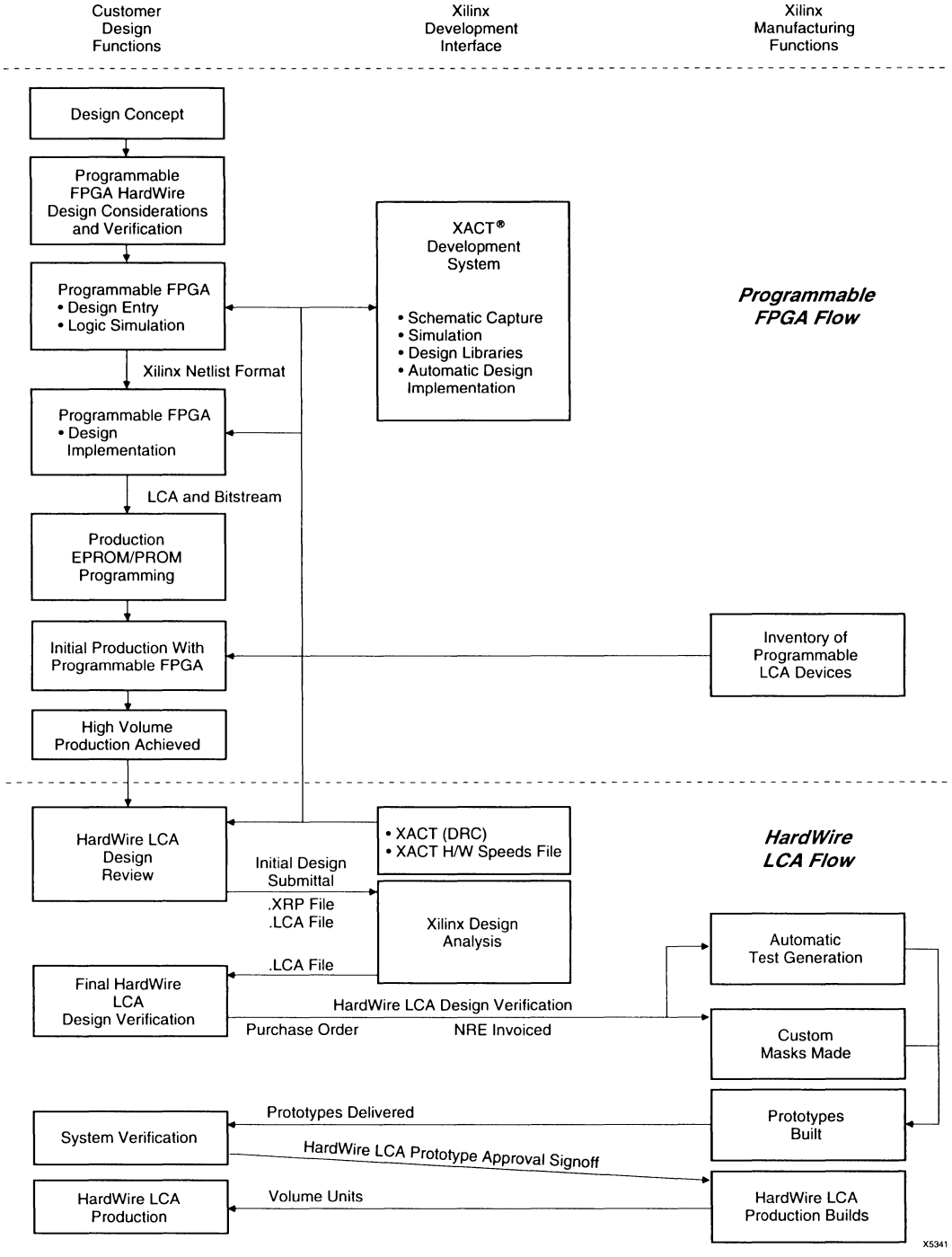


Figure 2. Programmable/HardWire Design/Production Interface

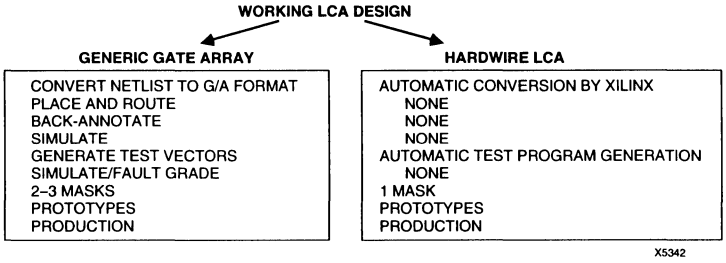


Figure 3. Design Flow Comparison: Gate Array versus HardWire.

Architecture

As shown in Figure 4, the HardWire LCA has the same architecture as the FPGA it replaces. The perimeter of I/O Blocks (IOBs) provides an interface between the internal logic array and the device package pins. The array of Configurable Logic Blocks (CLBs) performs user-specified logic functions. The interconnect resources are programmed to form networks carrying logic signals among blocks, analogous to printed circuit board traces connecting SSI/MSI packages.

The logic functions of the blocks are implemented by look-up tables. Functional options are implemented by user-defined multiplexers. Interconnecting networks between blocks are implemented with user-defined fixed metal connections.

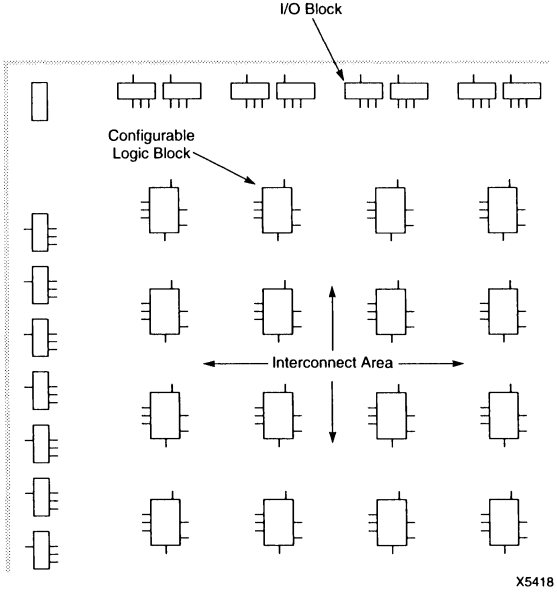


Figure 4. Logic Cell Array Structure

I/O Block

Each user-defined IOB (shown in Figure 5) provides an interface between the external package pin of the device and the internal user logic. The IOB is identical with that used in the FPGA. There are a wide variety of I/O options available to the user.

Summary of I/O Options

- Inputs
  - Direct/Flip-flop
  - CMOS/TTL threshold (chip inputs)
  - Pull-up resistor/open circuit
- Outputs
  - 3-state/on/off
  - 3-state/output enable (inverse)

Configurable Logic Block

The array of Configurable Logic Blocks (CLBs) provides the functional elements from which the user's logic is constructed. The logic blocks are arranged in a matrix within the perimeter of IOBs. The XC2318 has 100 such blocks arranged in 10 rows and 10 columns.

The configurable logic block is identical to that used in the XC2000 family of FPGA devices. Each configurable logic block has a combinatorial logic section, a storage element, and an internal routing and control section. Each CLB has four general-purpose inputs: A, B, C and D; and a special clock input (K), which may be driven from the interconnect adjacent to the block. Each CLB also has two outputs, X and Y, which may drive interconnect networks. Figure 6 shows the resources of a Configurable Logic Block.

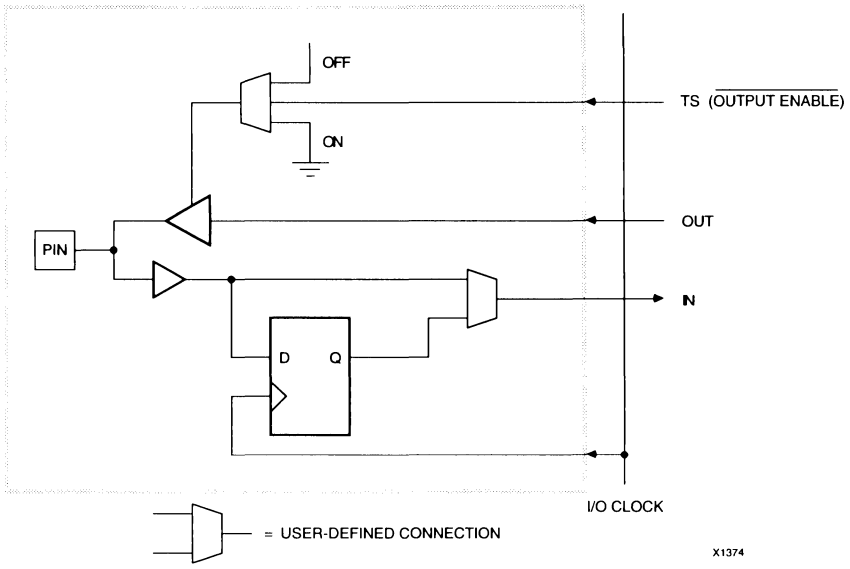


Figure 5. Input/Output Block. Each IOB includes an input storage element and I/O options pre-defined by the user. Passive pull-up can only be enabled on inputs, not on outputs. All user inputs are selectable for TTL or CMOS thresholds.

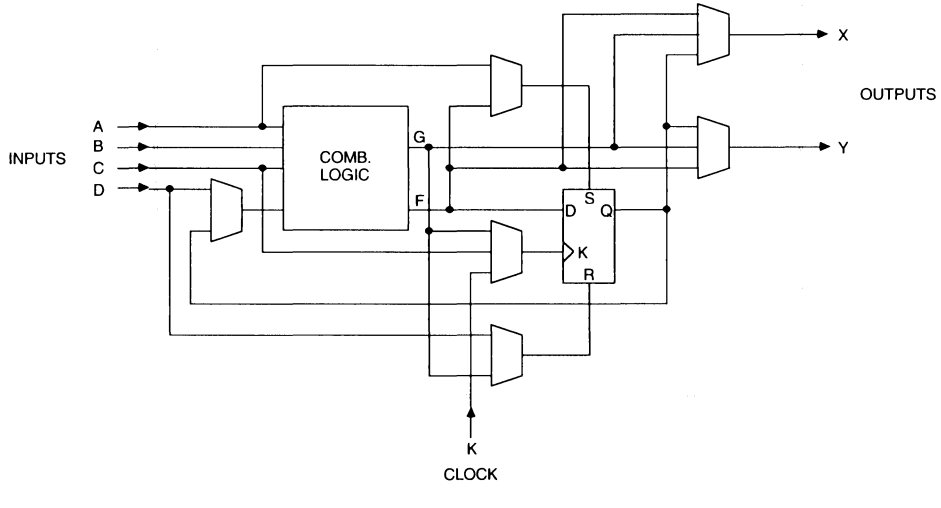


Figure 6. Configurable Logic Block

Interconnect

User-defined interconnect resources in the Logic Cell Array provide routing paths to connect inputs and outputs of the I/O and logic blocks into logic networks. Interconnections between blocks are composed from a two-layer grid of metal segments. The XACT development system provides automatic routing of these interconnections. The inputs of the IOBs and CLBs are multiplexers that are defined to select an input network from the adjacent interconnect segments.

Three types of metal resources are provided to accommodate various network interconnect requirements:

- General Purpose Interconnect
- Direct Connection
- Long Lines

The topology of all these interconnect resources is identical with that of the FPGA, but the speed of the interconnect paths is significantly faster (since all interconnections are fixed metal connections).

Configuration and Start-Up

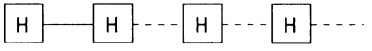
The start-up sequence of the XC2318 HardWire LCA is generally similar to that of the XC2000 FPGA. However, there are some differences which need to be considered before using the HardWire device in a socket designed for the programmable part. While the XC2318 does not require the loading of configuration data, it does support certain configuration modes.

Configuration

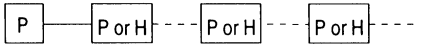
The XC2318 HardWire device can be used stand-alone or in a daisy chain with other LCAs. It does not produce CCLKs, and therefore cannot operate in Master Mode. Peripheral Mode is also not supported.

Mode 1. As a stand alone HardWire LCA

Mode 2. In a daisy chain of all HardWire LCA



Mode 3. As a HardWire LCA in a daisy chain with a Programmable device as a master.



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A HardWire device will not "swallow" its own configuration data. If the appropriate mask option is selected, whatever configuration bits are fed into the DIN pin will appear on the DOUT pin after a delay. If not, DOUT will be held in a high impedance state. In any case where a HardWire LCA device is ahead of a FPGA in a daisy chain (as in Mode 3 shown above) the configuration data will need to be modified. (See Mask Options Applications Note page 4-4 for further information).

Start-up Sequence

The XC2318 HardWire LCA start-up sequence has a number of differences from that of the XC2000 FPGAs. An internal power-on-reset circuit is triggered when power is applied. When V_{CC} reaches the voltage at which portions of the LCA begin to operate, the device enters a time-out period. During the time-out period the I/O buffers are disabled and a high-impedance pull-up resistor is provided for the user I/O pins. The length of this time-out period is user-defined to be either 64 µs or 16 ms.

The 64 µs period is used for a rapid reset cycle; the 16 ms period emulates the power-on sequence of an FPGA device.

After the time-out period the D/P pin will be released. When it goes High the I/O pins become active immediately, and the HDC and LDC pins become inactive. The time-out period can be extended by holding the D/P pin Low. If the XC2318 is in a daisy chain with FPGAs all the D/P pins should be tied together. This will ensure a synchronous start-up of all devices in the chain.

Performance

The single parameter which most accurately describes the overall performance of the Logic Cell Array is the maximum toggle rate for a logic block storage element configured as a toggle flip-flop. The configuration for determining the toggle performance of the Logic Cell Array is shown in Figure 7. The clock for the storage element is provided by the global clock buffer and the flip-flop output Q is fed back through the combinatorial logic to form the data input for the next clock edge.

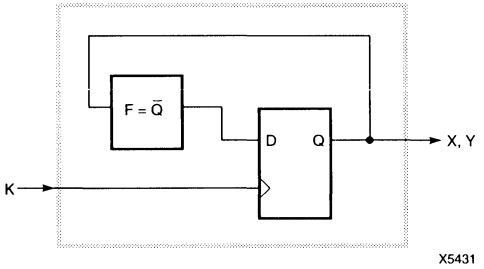

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Figure 7. Logic Block Configuration for Toggle Rate Measurement

Actual LCA performance is determined by the timing of critical paths, including the timing for the logic and storage elements in that path and the timing of the associated interconnect. HardWire logic block performance is equal to or slightly faster than the equivalent FPGA device, while the interconnect performance is significantly faster.

All HardWire devices are specified and tested for operation at the fastest equivalent FPGA speed available at the time the HardWire device is introduced. For the XC2318, this means all parts are guaranteed to the -70 speed grade. Since the finished HardWire LCA product is customized for a specific customer and application, speed grading is not available.

Power

Power for the HardWire LCA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the LCA, dedicated V_{CC} and ground rings surround the logic array and provide power to the I/O drivers. (See Figure 8.) An independent matrix of V_{CC} and ground lines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically a 0.1 µF capacitor connected near the V_{CC} and ground pins will provide adequate decoupling.

Output buffers capable of driving the specified 4 mA loads under worst-case conditions may be capable of driving 25 to 30 times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads.

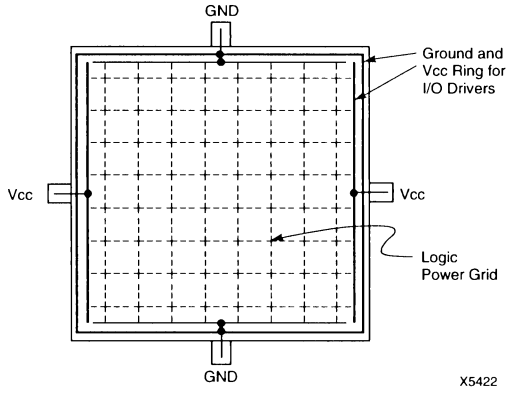


Figure 8. LCA Power Distribution.

HardWire LCA Design Considerations

It is important to observe good design practices while using HardWire LCAs. It is possible for a programmable device to "hide" some less obvious design shortcomings. However, these can manifest themselves when the design is converted to a HardWire LCA.

For example, a small glitch generated from unstable inputs to a CLB function block can be easily "swallowed" if the output is driving a long net. This is because the "pass transistors" act as a Low pass filter and this net's loads may never see the glitch. However, in a HardWire LCA, this glitch may propagate to the loads since there are only metal lines and vias in the routing path.

Gated Clocks and Reset Directs

Glitching function generators driving CLOCK and RESET DIRECT pins can inadvertently trigger flip-flops to an undesirable state. Avoid these so-called "gated" clock and reset direct nets; if unavoidable, design the logic so that the inputs are always stable and the signal changes are at least a CLB delay (T_{ILO}) apart.

Multiplexers Implemented in Function Generators

Two input multiplexers can be easily implemented in a single F or G function genterator. However, there is a possibility of a glitch if the selected signal and the selected input changes within a CLB's Tilo delay. This is generally not a problem with data and address multiplexers as long as the output is given enough time to settle; but if the multiplexer output is feeding a CLOCK and/or a RESET DIRECT pin, it is possible to toggle the register at undesired times.

The edge(s) of select signals for a CLOCK and/or RESET DIRECT multiplexers should be stable before and after the edges of the inputs. The edges should be at least a CLB (T_{ILO}) delay apart.

Race Conditions

All race conditions in the circuit need to go through a careful analysis. Depending on the routing resources responsible for the net delays, the correct signal may always "win the race" in a programmable FPGA; however, once converted to HardWire LCA, this may not be the case. (See Figure 8a.)

Delay Generators

Using the routing resources as delay lines in programmable FPGAs is undesirable. In HardWire LCAs, it is an invitation for timing problems. Remove all delay generators and redesign the circuit before converting it to HardWire.

Interfacing with External Devices

Almost all LCAs interface with external devices–FIFOs, memories, processors and peripherals, etc. Handshaking with devices requires specific setup/hold times. Ample hold time on a data bus from a programmable FPGA may no longer meet spec in HardWire LCA. An external data bus clocked by a HardWire LCA gererated signal may no longer meet the system set-up time requirements. This can happen because interconnects are much faster than in a programmable device. This requires reviewing the system timing specs when converting to a HardWire LCA.

In reality, all designers using LCAs (programmable or HardWire) face the same issues. Due to improvements in process and circuit design, a part specified at -50 today may actually be running as fast as -70 or even close to -100 in the future.

Xilinx does NOT guarantee a part against minimum timing specs. A "glitch" that was swallowed in a device today may crop up in a future device due to faster pass transistors in the routing paths. When using any Xilinx LCAs, the above issues should be addressed in the design phase.

HardWire LCA Testability

The XC2318 HardWire LCA contains significant on-chip logic to facilitate manufacturability and testing. This logic, combined with Xilinx's internal Automatic Test Generation (ATG) software, assures 100% functionality. In fact, the HardWire device can be 100% functionally tested by Xilinx without the need for customer generated test vectors (as is required with custom gate arrays).

This section examines the two basic block structures and the special test circuitry in the HardWire LCA. An example of a small XC2318 LCA design and the vectors generated for test are included.

Test Architecture

The HardWire LCA contains two types of internal blocks: the Input/Output Block (IOB) and the Configurable Logic Block (CLB). To accomplish 100% functional testing special test circuitry is designed into the device. This circuitry allows testing of each block (CLB and IOB) in a synchronized procedure known as "Scan Test". Special dedicated test latches (called TBLKs) are included on all HardWire devices. They are completely transparent to the normal operation of the circuit. Scan testing allows the contents of all internal flip-flops to be serially shifted off-chip, and for Xilinx generated test vectors to be shifted into the device, thus enabling all flip-flops to be initialized to any desired state.

These special dedicated test latches are placed into each CLB and IOB. Each CLB has three internal test latches, (placed at the CLB outputs), while each IOB contains one test latch (placed at the IOB input) as shown in Figures 9 and 10. The placement of these test latches is very important, since each CLB output or IOB input can fanout to multiple destinations. All sources and destinations of logic blocks come from other logic blocks, thus this placement of the latches provides complete access to all nets and synchronized control of all CLBs and IOBs.

The test latches are connected into a daisy chain which passes through every flip-flop in the LCA. Figure 11 shows an overview of the scan path. The path begins at the Scan In pin, sequences through each CLB, then through the IOBs, and finally exits at the Scan Out pin.

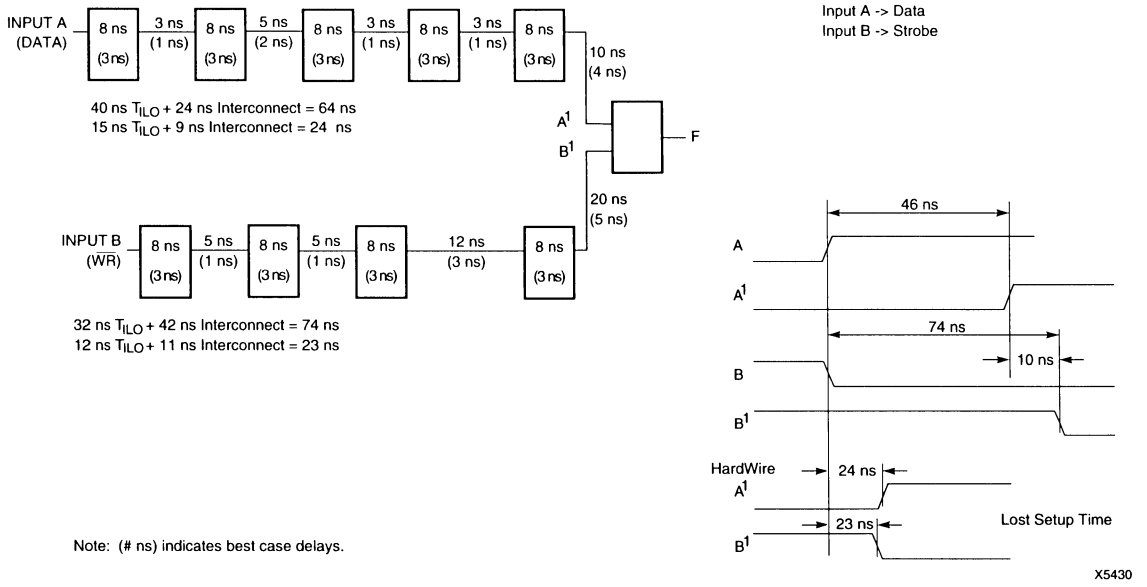


Figure 8a. Race Condition Example

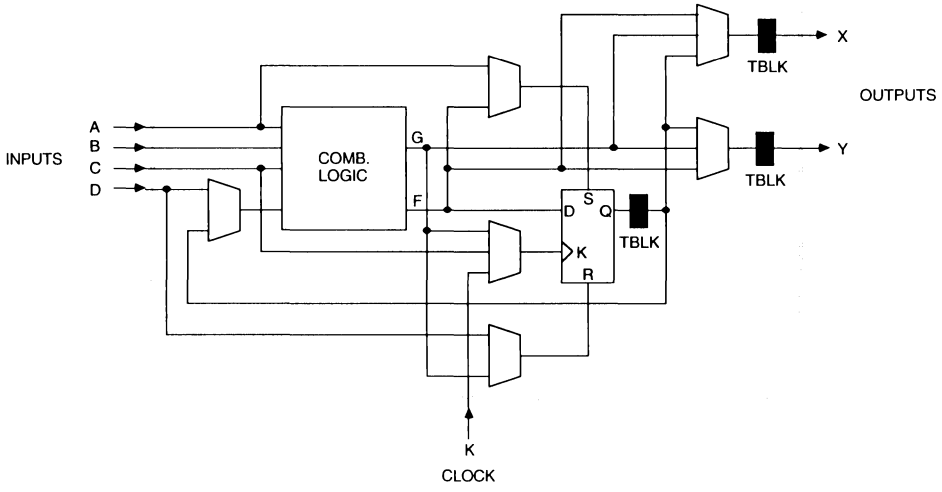


Figure 9. XC2318 HardWire LCA CLB Test Latch Locations

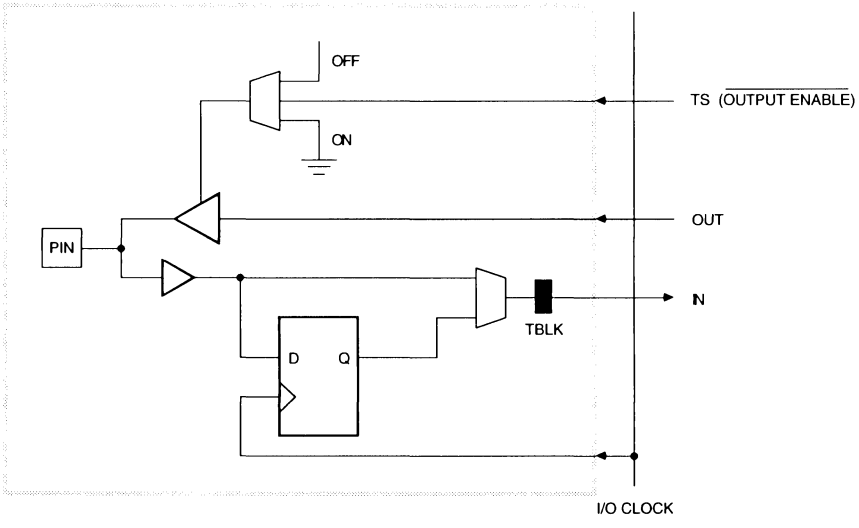


Figure 10. XC2318 HardWire LCA IOB Test Latch Location

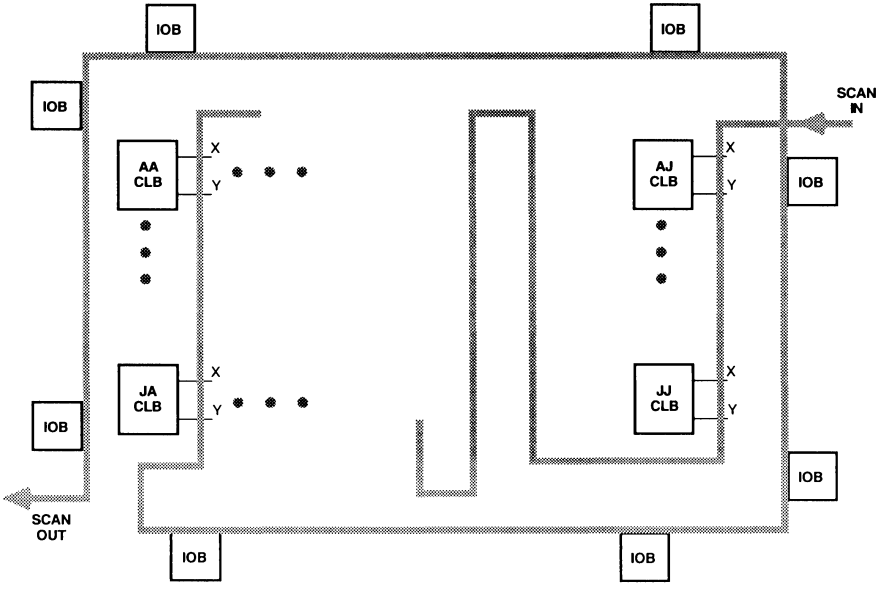


Figure 11. XC2318 HardWire LCA Scan Path Overview

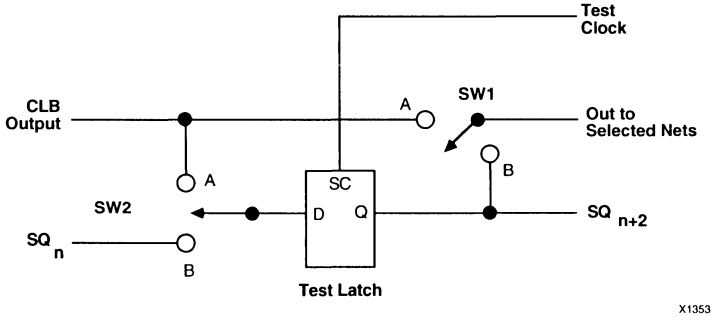


Figure 12. TBLK Block Diagram

The internal architecture of a TBLK is shown in Figure 12. In the normal operation mode of the HardWire LCA, SW1 is in position A and all the test latches are bypassed completely. The HardWire device is set into Test Mode (SW1 = position B) by Xilinx ATG software. This software inputs unique conditions on several control pins while serially loading a "password" into the device. For this reason, it is not possible for a customer design to inadvertently place the device into Test Mode. When SW1 is in position B (Test Mode) all the latches can receive data from either the CLB output or the previous latch in the daisy chain (SQn).

Synchronized together by a special test clock, all the test latches operate in two phases. The first phase serially loads all the latches to place a specific vector at the inputs of the logic block to be tested. The second phase is a parallel load of all latches, storing the expected output data of the logic block being tested (SW2 = A). At this point testing returns to phase one and serially clocks out the results, while simultaneously clocking in a new input vector.

Scan Test

To see how scan testing can be used to provide complete functional test coverage, consider the logic shown in Figure 13. This diagram shows a CLB (CLB2) with two inputs being driven by two different CLBs and the other two inputs being driven by two different IOBs. If we apply every possible combination of inputs to CLB2 and all expected output conditions are met, then CLB2 has been 100% functionally tested. The input conditions applied also include any register control signals (such as Clock, Reset, or Clock Enable). The same procedure is used for testing IOBs.

Looking again at Figure 13, CLB2 is tested by first serially loading the X output latches of CLB1 and CLB3 and the input latches of IOB1 and IOB2. Note that the latches on CLB2's outputs are also loaded in this first phase. Not all CLBs and IOBs can be tested at once, due to signal dependencies. To position the correct data into the latches all unused latches still need "don't cares" loaded. Regardless of which CLBs and IOBs are being tested by a particular scan vector, the complete scan path is always shifted in and out for testing and verification. The state of CLB2's output latches will be opposite to their expected results in phase two. This guarantees that CLB2's input data changed the state of its output latches and therefore, is current data.

CLB or IOB data registers using a synchronous or asynchronous clock are not a problem during this special test mode. All customer-used registers are clock inhibited during the phase one load. The inhibit of register clocking is accomplished by logically "ANDing" the register clocks with the global inhibit control line.

The test vectors needed to perform this thorough testing are created by Xilinx. No additional effort or engineering time is required from the user to ensure proper device performance. The customer design file used to create the HardWire LCA is used in conjunction with specially developed Xilinx Automatic Test Generation software. This creates the complete set of test vectors required to perform 100% functional testing. This software creates the data for all possible input conditions and corresponding output data for each CLB and IOB used in the customer design. This data is then compiled into the test vectors used to perform the actual testing.

Scan Test Example

Finally, Figure 14 shows an example of a very simple design implemented in an XC2318 HardWire LCA. This example uses only two CLBs and one IOB, and therefore uses only six test latches. The sample test vectors in Figure 15 show how scan test would be used to perform functional testing of this design. Note that the set of vectors shown tests only one input condition (input A of the CLB under test). The actual test file would contain all the additional vectors needed to completely test this design.

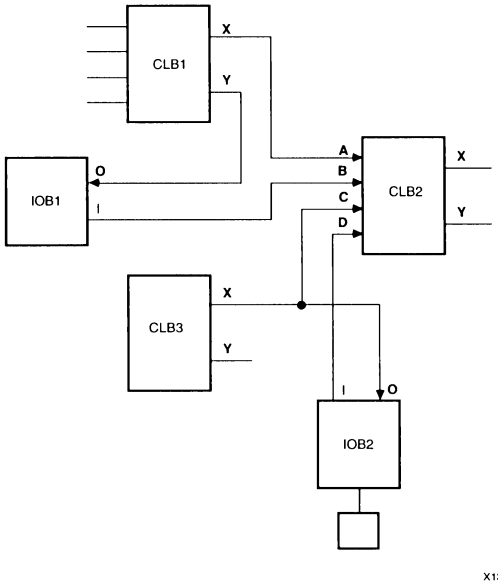


Figure 13. Four Input CLB (CLB2) Driven by Two Different CLB Outputs and Two different IOB Outputs

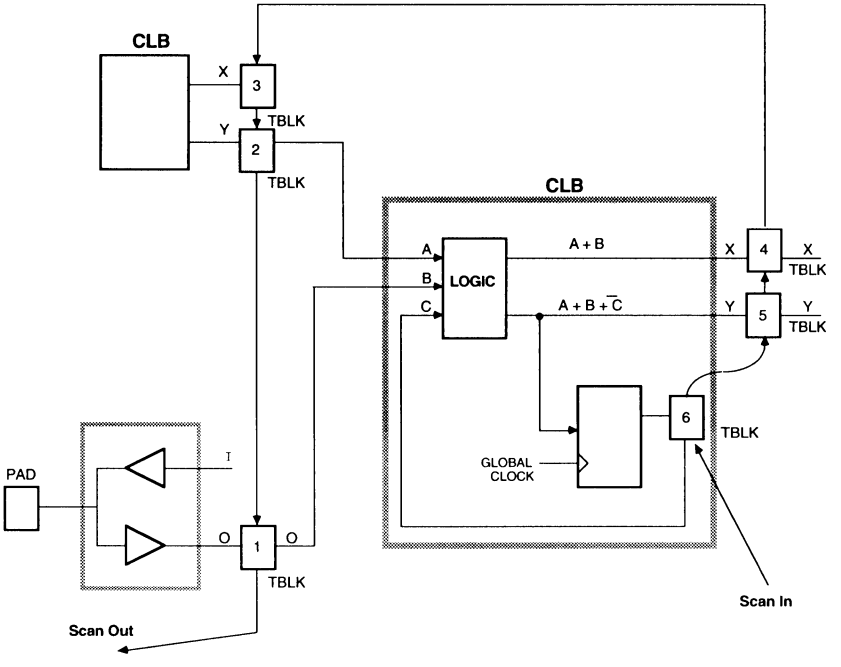


Figure 14. XC2318 Scan Test Example

The following vectors and comments show the testing of one input condition (input A of the CLB under test).

SCAN CLOCK	SCAN IN	SCAN OUT	GLOBAL CLOCK	COMMENTS
C	1	X	X	Load a 1 into Scan In pin, knowing it will be positioned in latch #1, input B. The global clock is inhibited and the scan out data are "don't cares".
C	1	X	X	Load a 1 into Scan In pin for input A.
C	X	X	X	Load a "don't care" (0 or 1) into latch #3, not used.
C	0	X	X	Load a 0 into latch #4, expecting the X output to be a 1 after phase two.
C	0	X	X	Load a 0 into latch #5, expecting the Y output to be a 1 after phase two.
C	0	X	X	Load a 0 into Scan #6, expecting the register output to be a 1 after phase two.
At this point all the latches are loaded. Enter phase two by changing the control pin (not shown here).				
0	X	X	C	Clock the data register after entering phase two. Now the register data is current but Latch #6 still has a 0 inside.
C	X	X	0	Load all the latches with their functional results.
This completes phase two. Return to phase one and load the next set of input data, while simultaneously verifying the scan out pin. We expect to see latches 4, 5, and 6 with ones as we scan the data out.				
C	1	X	X	Load a 1 into Scan In pin, knowing it will be positioned in latch #1, input B.
				The global clock is inhibited and the first three Scan Out data are "don't cares".
C	0	X	X	Load a 0 into Scan In pin for input A. This is the difference from the first load.
C	X	X	X	Load a "don't care" into latch #3, not used.
C	1	1	X	Load a 1 into latch #4, expecting the X output to be a 0 after phase two (input A = 0).
				The Scan Out pin will be showing the results of latch 4 from the previous load.
C	0	1	X	Load a 0 into latch #5, expecting the Y output to be a 1 after phase two.
				The Scan Out pin shows latch 5 results.
C	0	1	X	Load a 0 into latch #6, expecting the register output to be a 1 after phase two.
				Scan Out pin shows latch 6 results.

Figure 15. Sample Test Vectors for XC2318 Simple Design Example

Pin Descriptions

Permanently Dedicated Pins.

V_{CC}
Two connections to the nominal +5 V supply voltage. Both must be connected.

GND
Two connections to ground. Both must be connected.

$\overline{PWRDWN}$
A Low on this CMOS-compatible input stops all internal activity. All flip-flops and latches are reset, all outputs are 3-stated, and all inputs are interpreted as High, independent of their actual level. While $\overline{PWRDWN}$ is Low, V_{CC} may be reduced to any value >2.3 V. When $\overline{PWDWN}$ returns High, the LCA becomes operational within 1 µs. During configuration, $\overline{PWRDWN}$ must be High. If not used, $\overline{PWRDWN}$ must be tied to V_{CC}.

RESET
This is an active Low input. If $\overline{RESET}$ is asserted after configuration is complete, it provides a global asynchronous reset of all IOB and CLB storage elements of the LCA device.

CCLK
This pin is used only for manufacturer test. The user must either select the mask option to tie it High, or must tie it either High or Low in-system.

DONE/$\overline{PROG}$
DONE/$\overline{PROG}$ is an open-drain output, configurable with or without an internal pull-up resistor. At the completion of the start-up sequence, DONE/$\overline{PROG}$ will be released. When it goes High the I/O pins become active immediately.

M0
This pin is used only for manufacturer test. The user must either select the mask option to tie it High, or must tie it either High or Low in-system.

M1
This pin is used only for manufacturer test. The user must tie this pin either High or Low in-system.

User I/O Pins that can have special functions.

HDC
During configuration, this output is held at a High level to indicate that configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin.

$\overline{LDC}$
During configuration, this output is held at a Low level to indicate that the configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin.

XTL1
This user I/O pin can be used to operate as the output of an amplifier driving an external crystal and bias circuitry.

XTL2
This user I/O pin can be used as the input of an amplifier connected to an external crystal and bias circuitry. The I/O Block is left unconfigured. The oscillator configuration is activated by routing a net from the oscillator buffer symbol output.

DIN
During Slave configuration, this pin is used as a serial-data input.

DOUT
During configuration this pin is used to output serial-configuration data to the DIN pin of a daisy-chained slave.

TCLKIN
This is a direct CMOS level input to the global clock buffer.

Unrestricted User I/O Pins.

I/O
An I/O pin may be programmed by the user to be an Input or an Output pin following configuration. All unrestricted I/O pins, plus the special pins mentioned previously, have a weak pull-up resistor of 20 kΩ to 50 kΩ that becomes active as soon as the device powers up, and stays active until the end of configuration.

CONFIGURATION MODE		64 VQFP	68 PLCC	84 PLCC		100 TQFP/ VQFP	USER OPERATION
GND		8	1	1		13	GND
		9	2	2		14	
				3		15	
				4		16	
		10	3	5		17	
		11	4	6		18	I/O
<<HIGH>>		12	5	7		19	
		13	6	8		20	
		14	7	9		21	
		15	8	10		22	
		16	9	11		23	
PWRDWN (I)		17	10	12		26	PWR DWN
		18	11	13		27	
		19	12	14		29	
		20	13	15		30	
			14	16		32	
<<HIGH>>		21	15	17		33	I/O
				18		34	
		22	16	19		35	
				20		36	
		23	17	21		37	
VCC		24	18	22		38	VCC
		25	19	23		39	
				24		40	
		26	20	25		41	
<<HIGH>>				26		42	I/O
		27	21	27		43	
		28	22	28		45	
		29	23	29		47	
		30	24	30		48	
M1 (LOW or HIGH)		31	25	31		49	M1 (LOW or HIGH)
M0 (LOW or HIGH)		32	26	32		51	M0 (LOW or HIGH)
		33	27	33		53	
HDC (HIGH)		34	28	34		54	
<<HIGH>>		35	29	35		55	
LDC (LOW)		36	30	36		56	
		37	31	37		57	I/O
		38	32	38		58	
<<HIGH>>				39		59	
		39	33	40		60	
		40	34	41		61	
				42		62	
GND		41	35	43		63	GND
				44		64	
		42	36	45		65	
			37	46		66	
		43	38	47		67	
<<HIGH>>				48		68	I/O
		44	39	49		69	
			40	50		70	
		45	41	51		71	
		46	42	52		72	
		47	43	53		73	XTL2 OR I/O
		48	44	54		75	RESET
DONE (O)		49	45	55		77	PROG (I)
		50	46	56		78	XTL1 OR I/O
		51	47	57		79	
		52	48	58		80	
<<HIGH>>				59		82	
		53	49	60		84	I/O
				61		85	
		54	50	62		86	
		55	51	63		87	
VCC		56	52	64		88	VCC
		57	53	65		89	
		58	54	66		90	
				67		91	
<<HIGH>>		59	55	68		92	
				69		93	I/O
		60	56	70		95	
		61	57	71		96	
DIN (I)		62	58	72		97	
DOUT (O)		63	59	73		98	
CCLK (I)		64	60	74		99	CCLK (I)
		1	61	75		2	
		2	62	76		3	
		3	63	77		5	
		4	64	78		6	
			65	79		7	I/O
<<HIGH>>		5	66	80		8	
		6	67	81		9	
				82		10	
				83		11	
		7	68	84		12	

<<HIGH>> IS HIGH IMPEDANCE WITH A 20-5 kΩ
INTERNAL PULL-UP DURING CONFIGURATION

X5344

Table 2. XC2318 Pin Assignments

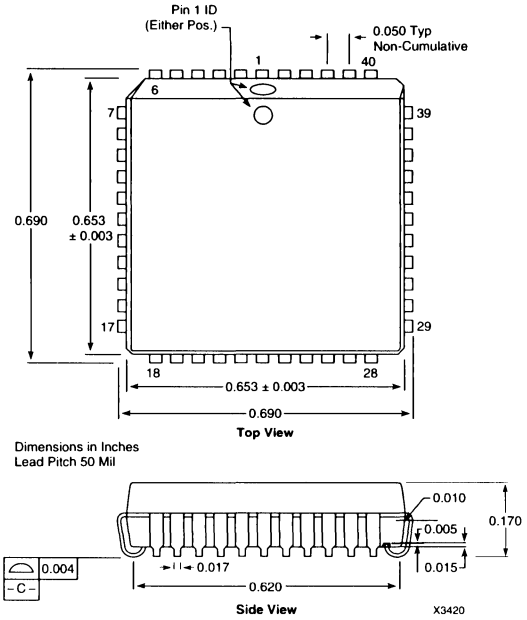
XILINX®

SECTION 3

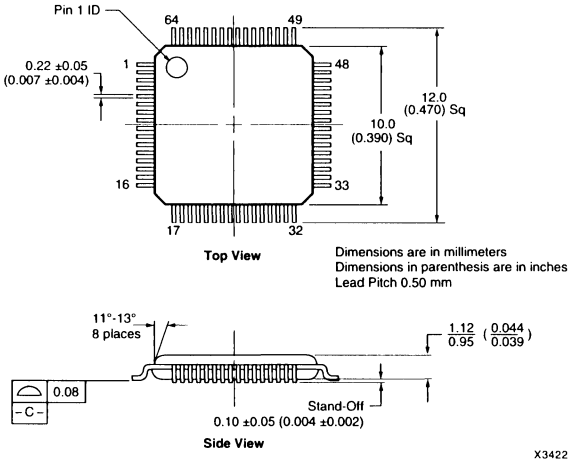
Packages

Table of Contents

Physical Dimensions

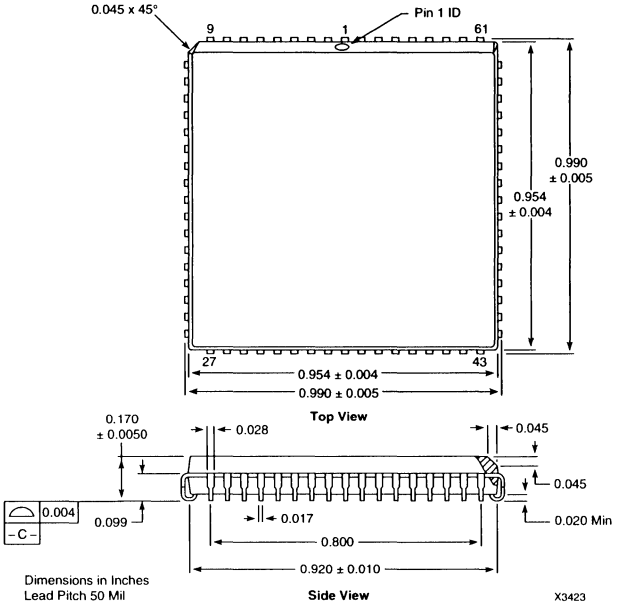


44-Pin Plastic PLCC (PC44)

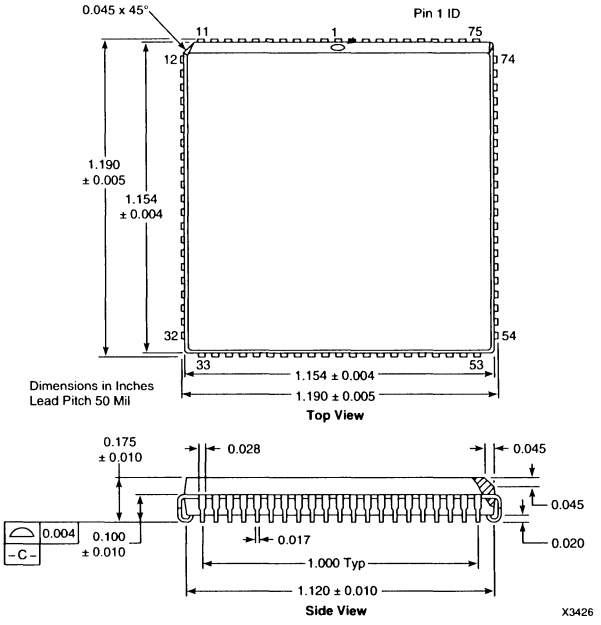


64-Pin Plastic VQFP (VQ64)

Physical Dimensions

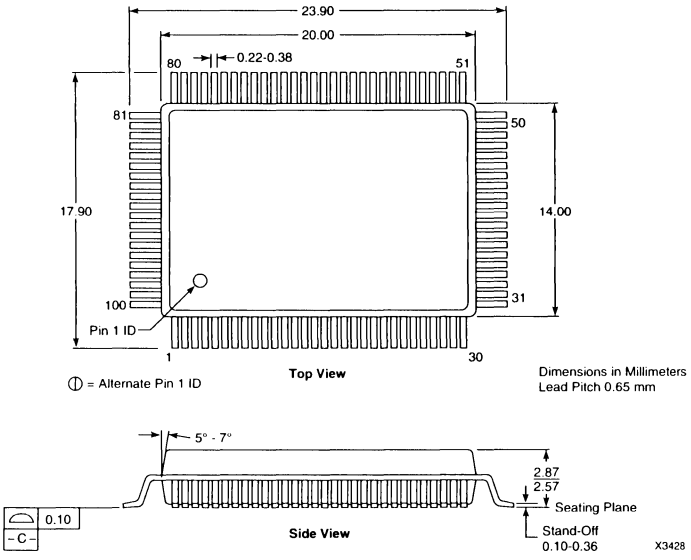


68-Pin Plastic PLCC (PC68)

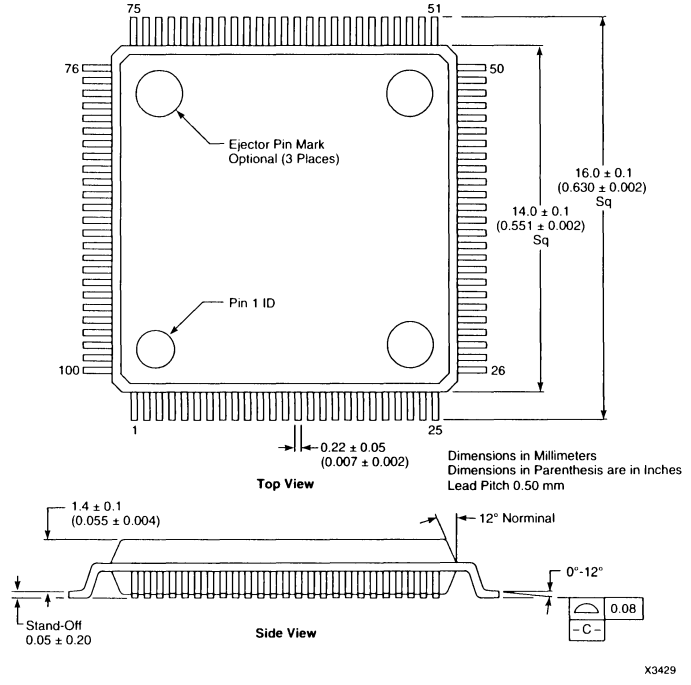


84-Pin Plastic PLCC (PC84)

Physical Dimensions

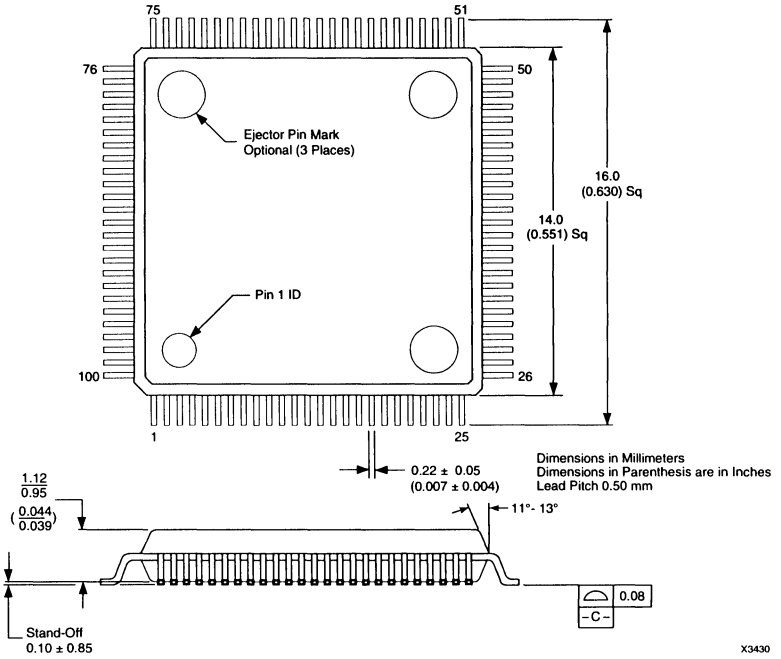


100-Pin Plastic PQFP (PQ100)

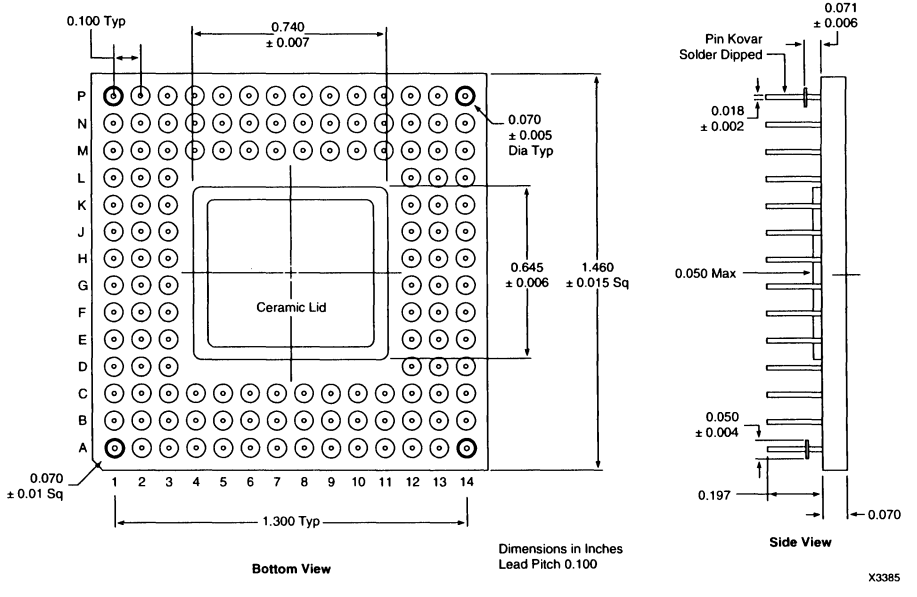


100-Pin Plastic TQFP (TQ100)

Physical Dimensions

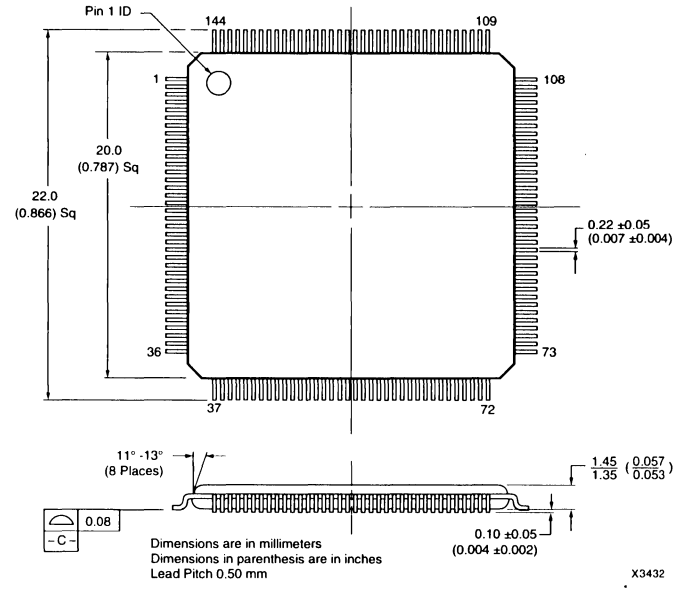


100-Pin Plastic VQFP (VQ100)

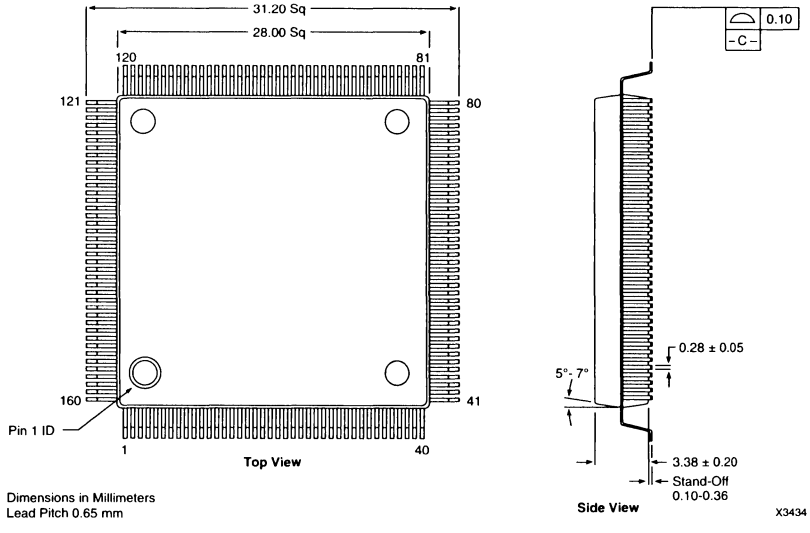


132-Pin Plastic PGA (PP132)

Physical Dimensions



144-Pin Plastic TQFP (TQ144)



160-Pin Plastic PQFP (PQ160)

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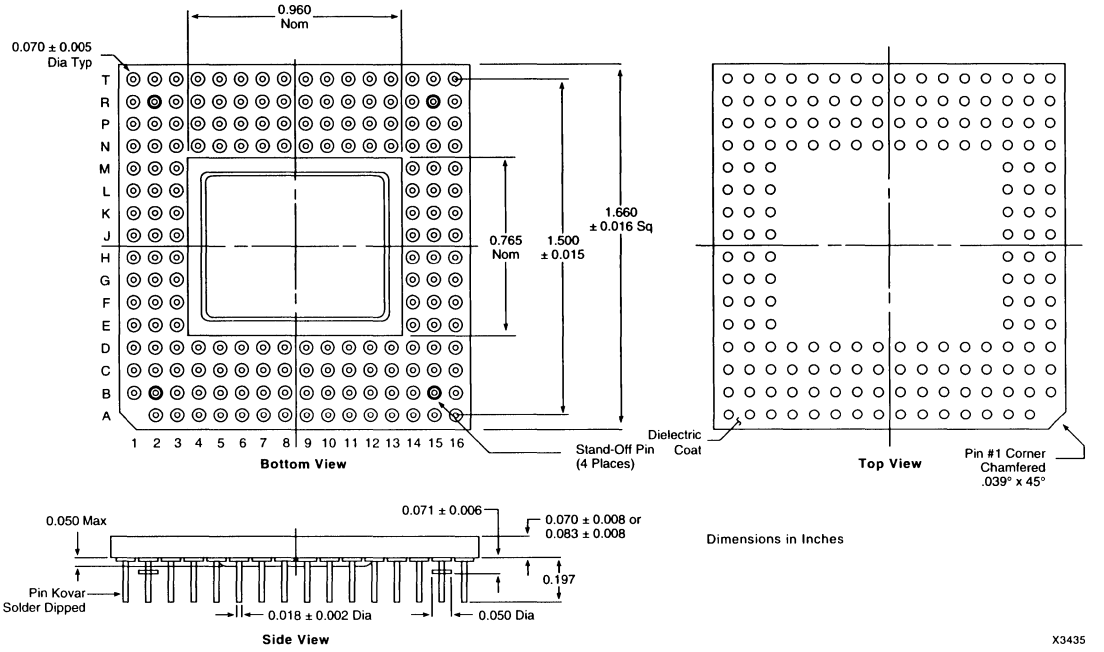
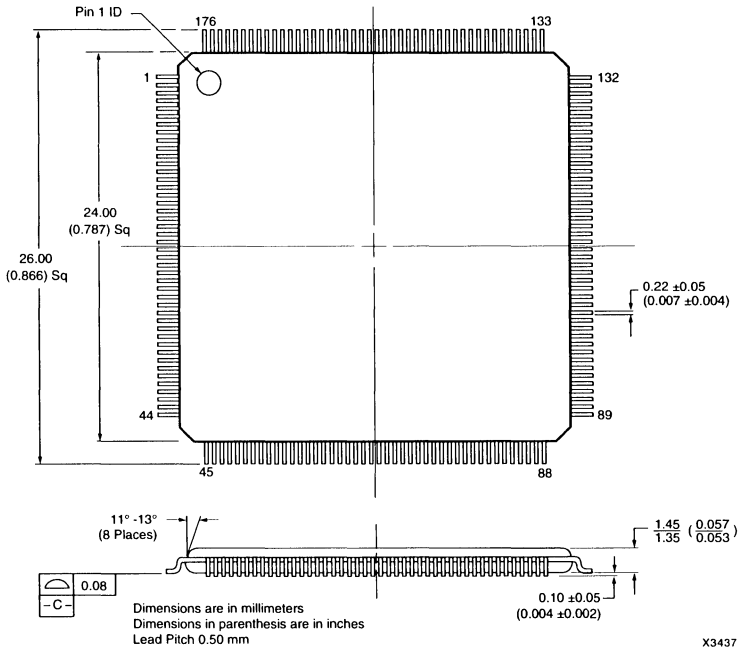
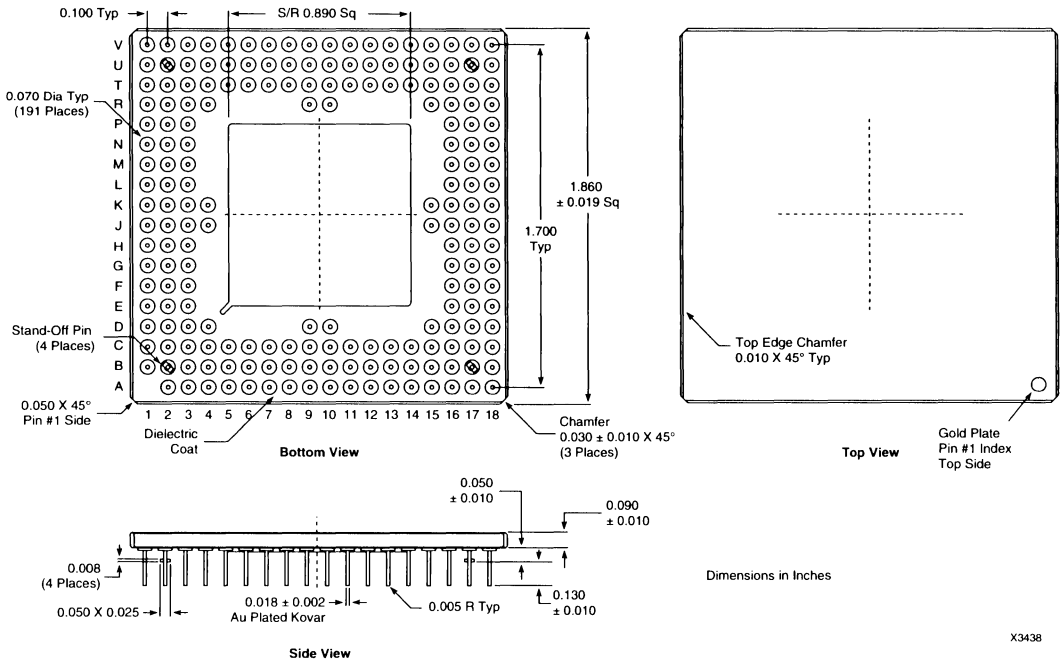


175-Pin Plastic PGA (PP175)

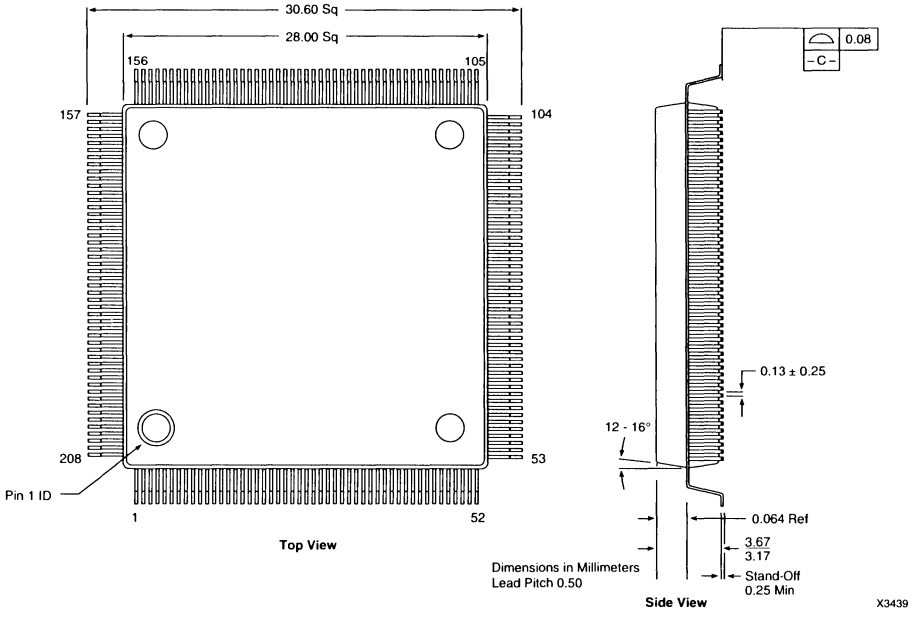


176-Pin Plastic TQFP (TQ176)

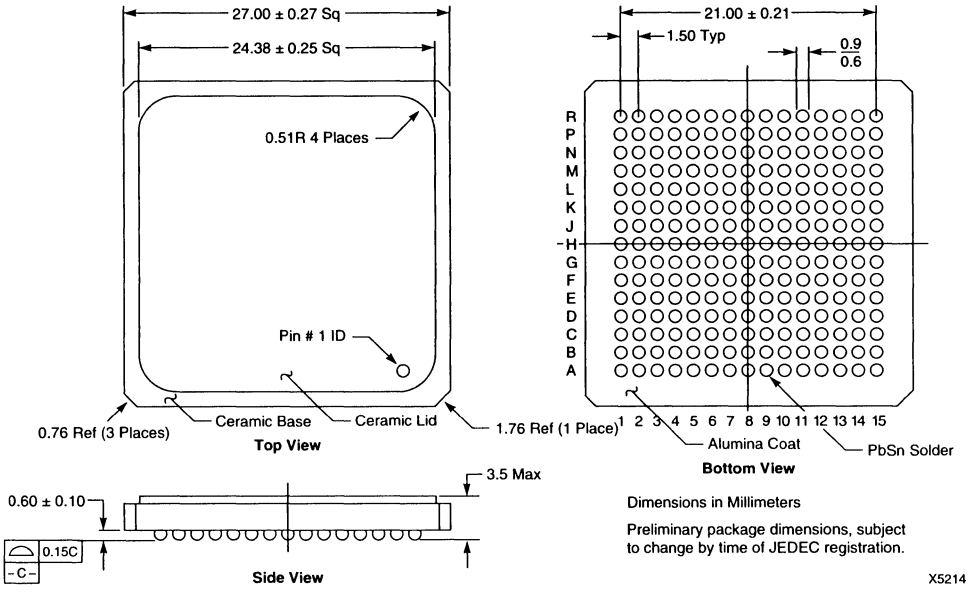
Physical Dimensions



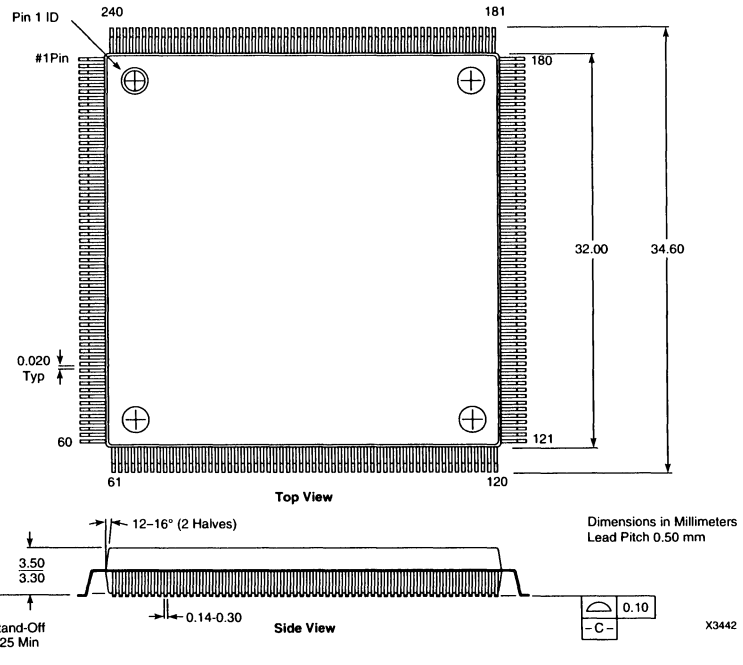
191-Pin Ceramic PGA (PG191)



208-Pin Plastic PQFP (PQ208)

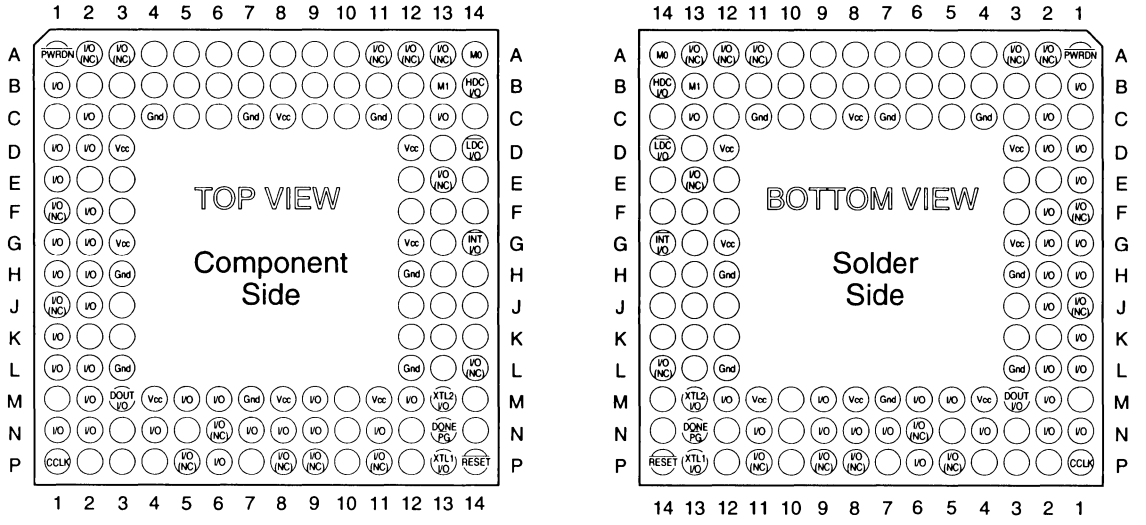


225-Pin Ceramic (CG225)

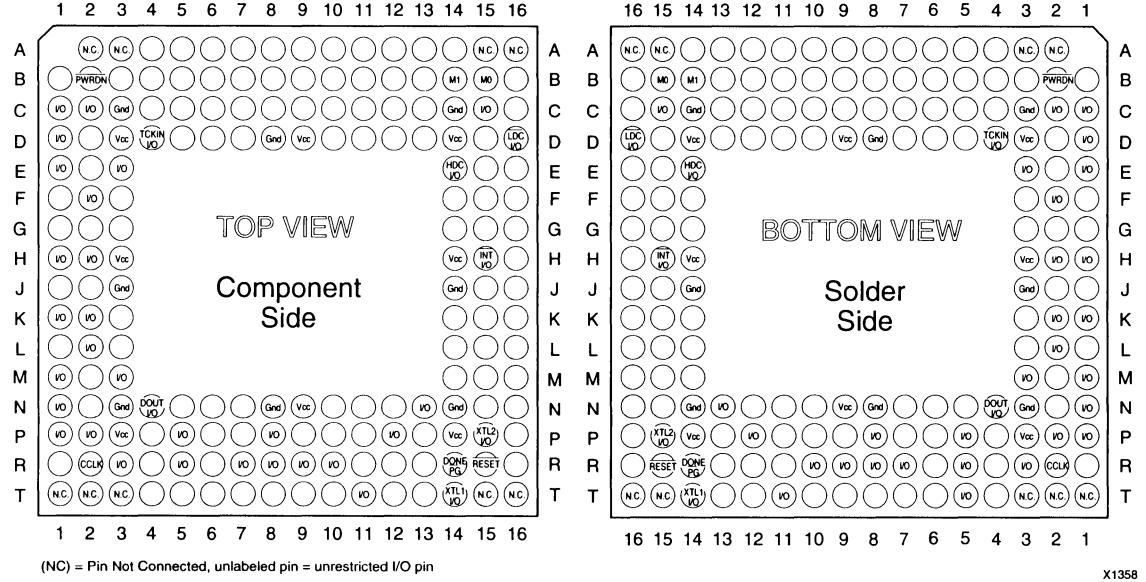


240-Pin Plastic PQFP (PQ240)

PGA Pinouts



PG132 Pinout (XC3390, XC3390A, XC3390L, XC3490A)



PG175 Pinout (XC3390, XC3390A, XC3390L, XC3490A)

HardWire LCA Mask Options

Table of Contents

XILINX®

XC4300 Mask Options

Because HardWire LCAs emulate most of the configuration and start-up options in the programmable versions, there are various mask options that need to be specified to best emulate the programmable devices.

The options must be specified in the XC4300 HardWire Design Verification form and verified by Xilinx Applications Engineering before design signoff.

Most of these mask options are MAKEBITS program options that are specified at the time MAKEBITS is run. Use the *design.MBO* file, (the MAKEBITS option output file) as the starting point to pick the proper options.

Here are the list of options that need to be specified:

RESISTOR OPTIONS:

There are three pins with resistor options;

DONE, M1, and TDO.

The DONE pin has a PULL-UP only, if the circuit board does not have an external pull-up then the pull-up option must be ON. The start up circuitry of the HardWire devices relies on the DONE signal going high to get the start up sequence running.

The M1 pin has a PULL-UP or PULL-DOWN or NEITHER option.

The TDO (test DATA OUT) pin is a dedicated pin for Boundary Scan. This pin has a PULL-UP, PULL-DOWN or NEITHER option.

CONFIGURATION EMULATIONS OPTIONS:

The user must specify one:

1. Long Power-On-Reset

   This option emulates the complete power on reset time of the programmable devices.

2. Short Power-On-Reset

   The power on reset time is dramatically reduced to allow for faster start-up. The device will start-up in the order of several µs with this option.

3. "Instant On"

   The HardWire device starts up immediately after power up, no configuration emulation is performed. The device goes into the start-up phase immediately.

START-UP OPTIONS:

There are three separate options to specify:

1. Start-up clock

   There is a choice of either using the configuration clock (CCLK) or a user supplied start-up clock (UCLK). The user clock option is for designs that require the start-up sequence to be synchronized with a particular system clock.

2. Sync-to-Done

   The start-up sequence can be further controlled by synchronizing it to the release of the Done pin (going high). This option can be used for designs that require synchronization of several devices starting up with one common event.

3. Start-up sequence options

   There are three events that happen during the start-up phase, each one of these can be specified to occur at a particular start-up clock cycle:

   Done pin goes active
   I/Os goes active
   Global Set/Reset gets released

   Each of these events can happen at either C1, C2, C3 or C4 if the CCLK is used for start-up. If the UCLK is used for start-up, the cycles are U1, U2, U3 or U4.

XC3300A/L, XC3400A Mask Options

The XC3300A/L, XC3400A HardWire product has several mask options that need to be specified by the customer. These options are MAKEBITS options in the programmable versions.

The options must be specified in the XC3400A HardWire Design Verification Form and verified by Xilinx Applications before design signoff.

There are a total of eight mask options that must be selected:

1. INPUT VOLTAGE LEVELS

Just like the input buffers in the programmable versions, the input buffers can either be TTL or CMOS. This option is on a GLOBAL basis and NOT per input.

For XC3300L devices this option defaults automatically to CMOS since TTL level is not available for the "L" family.

2. CONFIGURATION TIME INTERVAL

This option sets the time interval between the initial power up condition and when the D/$\overline{P}$-pin goes High. The 64 µs option is for designs that are not dependent on how fast the HardWire device powers up and goes active. The 16 ms option emulates the initialization delay time of the programmable device. When the device is set as Master Mode, both of these periods are multiplied by 4 (this is to ensure that in designs containing multiple LCAs in a daisy chain, the slave mode devices will be ready before the master device).

3. INTERNAL RESET RELEASES

There are three events that happen at start-up: I/Os go active, D/P- releases, and the internal reset signal releases. The release of the internal reset signal happens relative to the I/Os going active. This can be set either one CCLK cycle BEFORE the I/Os go active or one CCLK cycle AFTER the I/Os go active. The default condition is AFTER I/Os. Xilinx recommends the default option. In rare instances where the internal FFs need to be written prior to the output drivers going active, then BEFORE I/Os needs to be selected. "BEFORE I/O" cannot be used if the "Instant On" option was selected.

4. D/P-PULL-UP RESISTOR

The D/$\overline{P}$-resistor option MUST be selected if there is no external pull-up on this pin. The HardWire device depends on the state of the D/$\overline{P}$- feeding back into the device to start up the device. A high signal must be present for the HardWire to recognize the end of the "pseudo configuration" process.

5. OSCILLATOR

If the internal oscillator is used on the programmable design, choose the ACTIVE option. If the divide by 2 option is used, choose the ACTIVE/2 option.

6. MASTER MODE

This option is for programmable designs that use the Peripheral mode to program the LCA. Because the HardWire devices do *not* support Peripheral mode emulation, and the M0 pin in Peripheral mode is either tied High or pulled up, the HardWire device needs to be selected as a Master for it to start up. By turning this option on, the HardWire device ignores the state of the M0 pin and assumes it is a Master mode device and starts up on its own. For designs that use Slave mode or any of the Master mode configuration schemes, this option should be turned off, since the M0 pin will be tied to the proper level.

If the LCA configures in slave mode, the system still needs to provide CCLK to the HardWire device.

7. M1 "NORMAL" MODE POLARITY OPTION

This option works in conjunction with the Boundary Scan enable option. The user selects whether the M1 pin interprets "normal" mode to be a HIGH or LOW signal.

8. IN ADDITION, THE XC3300A/XC3000L/XC3400A DEVICES SUPPORT IEEE 1149.1 COMPATIBLE BOUNDARY SCAN INSTRUCTIONS. To access this feature, one of the following options must be selected.

Enable Boundary Scan:
1. ALWAYS enable
2. Active when M1 is Low
3. Active when M1 is High
4. Not Used

If ALWAYS is selected, the BSCAN pins are permanent and can be used for Boundary Scan test purposes.

If Active when M1 is LOW is selected, the device will stay in BSCAN test mode as long as the M1 pin is driven High. If Active when M1 is HIGH is selected, the device will stay in BSCAN test mode as long as the M1 pin is driven Low. i.e. during the start-up phase (after initialization state), the device will enter BSCAN mode when it samples the M1 pin and finds it to be in the BSCAN active state. When M1 is driven back to the opposite state, the BSCAN pins go back to user I/Os.

If the Boundary Scan feature is not used, select the NOT USED option.

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XC3300 Mask Options

The 3300 HardWire LCA product has several mask options that need to be specified by the customer. Usually these are MakeBits options in the programmable FPGA device.

These options must be specified in the XC3300 HardWire Design Verification Form and verified by Xilinx Applications before signing off the design.

There are a total of six mask options that must be selected:

1. INPUT VOLTAGE LEVELS

Like the input buffers in the FPGA versions, the HardWire LCA input buffers can either be TTL or CMOS. This option is on a ***global*** basis and ***not*** per input.

2. CONFIGURATION TIME INTERVAL

This option sets the time interval between the initial power up condition and when the D/P-pin goes High. The 64 µs option is for designs that do not care how fast the HardWire LCA device powers up and becomes active. The 16 ms option emulates the initialization delay time of the programmable LCA device. When the device is set as "Master Mode", both of these periods are multiplied by 4 (this is to ensure that in designs containing multiple LCAs in a daisy chain, the slave mode devices will be ready before the master device is ready).

3. INTERNAL RESET RELEASES

Three events occur at start up: I/Os go active, D/P-releases, and the internal reset signal releases. The release of the internal reset signal occurs relative to the I/Os going active. This can be set either one CCLK cycle ***before*** the I/Os go active or one CCLK cycle ***after*** the I/Os go active. The default condition is "after I/Os". Xilinx recommends the default option. In rare instances where the internal FFs need to be written prior to the output drivers going active, "before I/Os" needs to be selected.

4. D/$\overline{P}$-PULL-UP RESISTOR

The D/$\overline{P}$-resistor option ***must*** be selected if there is no external pull-up on this pin. The HardWire device depends on the state of the D/$\overline{P}$-resistor feeding back into the device to start up the device. A high signal must be present for the HardWire to recognize the end of the "pseudo configuration" process.

5. OSCILLATOR

If the internal oscillator is used on the FPGA design, choose the "Active" option. If the divide by 2 option is used, choose the "Active/2" option.

6. MASTER MODE

This option is for FPGA/LCA designs that use the Peripheral mode during programming. Because the HardWire devices do ***not*** support Peripheral mode emulation, and the M0 pin in Peripheral mode is either tied High or pulled up, the HardWire LCA device needs to be selected as a Master for it to start up. By turning this option on, the HardWire LCA device ignores the state of the M0 pin and assumes it is a Master mode device and starts up on its own. For designs that use Slave or any of the Master mode configuration schemes, this option should be turned off, since the M0 pin will be tied to the proper level.

If the FPGA configures in slave mode, the system still needs to provide CCLK to the HardWire LCA device.

XC2318 Mask Options

The 2318 HardWire LCA product has several mask options that need to be specified by the customer. Usually these options are MakeBits options in the FPGA versions.

These options must be specified in the XC2318 HardWire Design Verification Form and verified by Xilinx Applications before signing off the design.

There are a total of six mask options

1. INPUT VOLTAGE LEVELS

Just like the input buffers in the FPGA versions, the input buffers can either be TTL or CMOS. This option is on a ***global*** basis and ***not*** per input.

2. CONFIGURATION TIME INTERVAL

This option sets the time interval between initial power up condition and when the D/P̄-pin goes High. The 64 µs option is for designs that do not care how fast the HardWire LCA device powers up and becomes active. The 16 ms option emulates the initialization delay time of the FPGA device. When the device is set as "Master Mode" both of these periods are multiplied by 4 (this is to ensure that in designs containing multiple LCAs in a daisy chain, the slave mode devices will be ready before the master device is ready).

3. THERE ARE PULL-UP RESISTOR OPTIONS ON FOUR PINS

D/P̄-:	This option ***must*** be selected if there is **no** external pull-up on this node.
CCLK:	A pull-up can be added on the CCLK pin.
M0:	A pull-up can be added on the M0 pin.
PWRDWN:	A pull-up can be added on the PWRDWN pin.

4. HDC AND LDC OPERATION

If the FPGA version of the device is using the HDC and/or LDC signals to disable certain functions in the system, the HDC and LDC option(s) should be turned on. If the state of these pins are "don't care" or are not being used at all, then the option should be turned off.

5. DOUT DURING CONFIGURATION

The HardWire LCA device has the ability to act as a Serial Master device. Although it will not swallow its own bitstream it can drive the CCLK line and pass the serial data to downstream slave devices. If the design needs this capability then pick the "DOUT = DIN" option, otherwise pick the "High Impedance" option.

6. OSCILLATOR

If the design uses the internal oscillator function, then the "Active" option should be selected.

Forms

Table of Contents

HardWire™ LCA Initial Design Submittal Form

Company Name _____ Customer Name _____

Address _____ City _____ State _____ Zip _____

Telephone ( ) _____ FAX ( ) _____

Customer Part Number _____

√	Device	Option		√	Device	√	Device	√	Device	Option		√	Device
	XC2318				XC4303		XC3430A		XC4402A				XC4408
	XC3330	A	L		XC4305		XC3442A		XC4403	A	H		XC4410
	XC3342	A	L		XC4310		XC3490A		XC4405	A	H		XC4413
	XC3390	A	L						XC4406				XC4425

• Check approprate box (circle option if applicable).

Design Information Submitted to Xilinx

.LCA Design Filename (Required) _____

.XRP "DRC Informational" Filename (Required) _____

.MBO Filename (Required) _____

.BID Filename (Required) _____

Design Schematic (Required) _____

Timing Diagram of System I/Os (Optional) _____

Design Block Diagram (Optional) _____

Development Methodology Used

Design entry method used (Check all that applies):

☐ Schematic type_____ ☐ X-BLOX ☐ XABEL ☐ Synthesis type_____

Simulation: ☐ Not done ☐ Done with _____

Programmable FPGA Design Information

FPGA Device _____ Speed Grade _____ Temperature Grade _____

Configuration Mode used in Programmable FPGA:

☐ Peripheral Synchronous (XC4400)
☐ Peripheral Asynchronous (XC4400)
☐ Master Serial
☐ Master Parallel Up
☐ Peripheral Parallel
☐ Slave Serial
☐ Master Parallel Down

Is Configuration Emulation Needed? ☐ Yes ☐ No

JTAG Emulation ☐ Yes ☐ No

RAM Description (Name, Size, Cycle, Time, etc.) _____

_____

First Year Projected Volume for HardWire LCA Device (Required)_____

For Xilinx Use Only

Marketing _____

Application Engineer _____

HardWire LCA Design Number (HD Code) _____

XILINX®

XC4400 HardWire™ LCA Design Verification Form

Company Name _____ Customer Name _____

Address _____ City _____ State _____ Zip _____

Telephone ( ) _____ Customer Part Number ( ) _____

HardWire LCA ☐ XC4402 ☐ XC4403 ☐ XC4403H ☐ XC4405 ☐ XC4405H ☐ XC4406
☐ XC4408 ☐ XC4410 ☐ XC4410D ☐ XC4413 ☐ XC4425 ☐ XC4495

Package _____ Temperature Grade _____

XC4400 HardWire Options:

Configuration Mode:
☐ Master Serial ☐ Slave Serial
☐ Master Parallel Up ☐ Master Parallel Down
☐ Peripheral Synchro (XC4000) ☐ Peripheral Asynchro (XC4000)
☐ Peripheral (XC3000)

Configuration Mode Emulation needed? ☐ No ☐ Yes

Boundary Scan Emulation needed? ☐ No ☐ Yes

XC4400 Design To Be Used for Mask Generation

.LCA Filename and Time stamp from line 1 _____

.MBO Filename and Time stamp _____

Customer Part Marking for Device Package (11Characters max.) _ _ _ _ _ _ _ _ _ _ _

HardWire Terms and Conditions:

Please put a check mark against the following items as applicable. All items need to be checked for a signoff.

☐ The application circuit board must have a provision for configuration program storage (i.e., XC17128, EPROM, etc.). The socket can be left unpopulated when conversion to the HardWire device is made. The HardWire device is designed to provide a cost reduction path for existing fully debugged programmable designs.

☐ I certify that the above listed .LCA file is the correct design.

☐ I have reviewed the attached Xilinx HardWire Review Report (including the list of potentially hazardous nets) and have determined that none of the issues raised will be a problem in the system.

☐ I authorize Xilinx to start the HardWire mask making and fabrication process.

Customer Name _____ Signature _____ Date: _____

For Xilinx Use Only

Xilinx Design Applications Manager: _____ Signature _____ Date _____

Xilinx Design Number (HD Code): _____

Xilinx Part Number (HPC Code): _____

Xilinx Customer Service: _____ Signature _____ Date _____

NRE PO Number: _____

XILINX®

XC4300 HardWire™ LCA Design Verification Form

Company Name _____ Customer Name _____

Address _____ City _____ State _____ Zip _____

Fax Number ( ) _____ Telephone ( ) _____

Customer Part Number _____ Package Type and Temp Grade _____

• LCA File Name (to be used for mask generation) _____

• MBO Filename _____ (required)

Device Checklist ☐ XC4303 ☐ XC4305 ☐ XC4310

HardWire Mask Options (see XC4300 Mask Options in the HardWire Data Book for more information)

Configuration Emulation:

Instant ON ☐ Long Power on RESET ☐

Short Power on RESET ☐ Data Swallowing ON ☐

Data Swallowing OFF ☐

Internal Resistor Options:

Done Pull Up ☐	M1 Pull Up ☐	TDO Pull Up ☐
	M1 Pull Down ☐	TDO Pull Down ☐
	None ☐	None ☐

Boundary Scan Enabled ? Yes ☐ No ☐

Customer Part Marking for Device Package (Optional - 11 Characters max.) _ _ _ _ _ _ _ _ _ _ _

Customer Text on Silicon:

☐ No customer text (This is default)

☐ 3 lines of 9 large (20 µ x 30 µ) characters each _____

☐ 4 lines of 13 small (12 µ x 18 µ) characters _____

(optional-valid characters: "0-9", "A-Z", "! @$%() [] {} ./+-_")

HardWire Terms and Conditions:

Please put a check mark against the following items as applicable. All items need to be checked for a signoff.

☐ The application circuit board must have a provision for configuration program storage (i.e., XC17128, EPROM, etc.). The socket can be left unpopulated when conversion to the HardWire device is made. The HardWire device is designed to provide a cost reduction path for existing fully debugged programmable designs.

☐ I certify that the above listed .LCA file is the correct design.

☐ I have reviewed the attached Xilinx HardWire Review Report (including the list of potentially hazardous nets) and have determined that none of the issues raised will be a problem in the system.

☐ I authorize Xilinx to start the HardWire mask making and fabrication process.

Customer Name _____ Signature _____ Date: _____

Xilinx Design Applications Manager: _____ Signature _____ Date: _____

Xilinx Design Number (HD Code): _____

Xilinx Customer Service: _____ Signature _____ Date: _____

NRE PO Number: _____

Xilinx Product Engineering Manager: _____ Signature _____ Date: _____

Xilinx Part Number (HPC Code): _____

XILINX®

XC3400/XC3300A HardWire™ LCA Design Verification Form

Company Name _____ Customer Name _____

Address _____ City _____ State _____ Zip _____

Telephone ( ) _____ FAX ( ) _____

Customer Part Number _____ Package Type and Temp Grade _____

Device Checklist

☐XC3300A ☐XC3342A ☐XC3390A ☐XC3430A ☐XC3442A ☐XC3490A

HardWire LCA Options

Master Mode Selectable (Controlled by M0) _____ Unselectable (Forced On) _____

Boundary Scan: ☐ Not Used ☐ Always Active ☐ Active When M1 is High ☐ Active When M1 is Low

If Boundary Scan enabled: Pin assignment for TCK: _____ Pin assignment for TDO: _____

Pin assignment for TDI: _____ Pin assignment for TMS: _____

Input Voltage Levels	TTL _____	CMOS _____		
Configuration Time Interval	64 µs _____	16 ms _____	"Instant On" _____	
Internal Reset Release	Before I/O's _____	After I/O's _____	(forced to "After I/Os with	
D/P Pull-up Resistor	Yes _____	No _____	"Instant On")	
Oscillator	Inactive _____	Active _____	Active/2 _____	

XC3300A/XC3400A LCA Design To Be Used for Mask Generation

Filename and Revision Date (.LCA file) _____

Customer Part Marking for Device Package (Optional - 11 Characters max.) _ _ _ _ _ _ _ _ _ _ _

Customer Text on Silicon:

☐ No customer text (This is default)

☐ 3 lines of 9 large (20 µ x 30 µ) characters each _____

☐ 4 lines of 13 small (12 µ x 18 µ) characters _____

(optional-valid characters: "0-9", "A-Z", "! @$%() [] {} .,/+-_")

HardWire Terms and Conditions:

Please put a check mark against the following items as applicable. All items need to be checked for a signoff.

☐ The application circuit board must have a provision for configuration program storage (i.e., XC17128, EPROM, etc.). The socket can be left unpopulated when conversion to the HardWire device is made. The HardWire device is designed to provide a cost reduction path for existing fully debugged programmable designs.

☐ I certify that the above listed .LCA file is the correct design.

☐ I have reviewed the attached Xilinx HardWire Review Report (including the list of potentially hazardous nets) and have determined that none of the issues raised will be a problem in the system.

☐ I authorize Xilinx to start the HardWire mask making and fabrication process.

Customer Name _____ Signature _____ Date: _____

Xilinx Design Applications Manager: _____ Signature _____ Date: _____

Xilinx Design Number (HD Code): _____

Xilinx Customer Service: _____ Signature _____ Date: _____

NRE PO Number: _____

Xilinx Product Engineering Manager: _____ Signature _____ Date: _____

Xilinx Part Number (HPC Code): _____

XILINX®

XC3300L HardWire™ LCA Design Verification Form

Company Name _____ Customer Name _____

Address _____ City _____ State _____ Zip _____

Telephone ( ) _____ FAX ( ) _____

Customer Part Number _____ Package Type _____

XC33XX HardWire LCA Options

Device	XC3330L	_____	XC3342L	_____	XC3390L	_____
Configuration Time Interval	64 µs	_____	16 ms	_____	"Instant On"	_____
Internal Reset Release	Before I/O's	_____	After I/O's	_____	(forced to "After I/Os with	
D/P Pull-up Resistor	Yes	_____	No	_____	"Instant On")	
Oscillator	Inactive	_____	Active	_____	Active/2	_____
Master Mode	Selectable (Controlled by M0)	_____	Unselectable (Forced On)	_____		

Boundary Scan: ☐ Not Used ☐ Always Active ☐ Active When M1 is High ☐ Active When M1 is Low

Customer Part Marking for Device Package (Optional - 11 Characters max.) _ _ _ _ _ _ _ _ _ _ _

Customer Text on Silicon:

☐ No customer text (This is default)

☐ 3 lines of 9 large (20 µ x 30 µ) characters each _____

☐ 4 lines of 13 small (12 µ x 18 µ) characters _____

(optional-valid characters: "0-9", "A-Z", "! @$%() [] {} .,/+-_")

XC3300L LCA Design To Be Used for Mask Generation

Filename and Revision Date (.LCA file) _____

HardWire Terms and Conditions:

Please put a check mark against the following items as applicable. All items need to be checked for a signoff.

☐ The application circuit board must have a provision for configuration program storage (i.e., XC17128, EPROM, etc.). The socket can be left unpopulated when conversion to the HardWire device is made. The HardWire device is designed to provide a cost reduction path for existing fully debugged programmable designs.

☐ I certify that the above listed .LCA file is the correct design.

☐ I have reviewed the attached Xilinx HardWire Review Report (including the list of potentially hazardous nets) and have determined that none of the issues raised will be a problem in the system.

☐ I authorize Xilinx to start the HardWire mask making and fabrication process.

Customer Name _____ Signature _____ Date: _____

Xilinx Design Applications Manager: _____ Signature _____ Date: _____

Xilinx Design Number (HD Code): _____

Xilinx Customer Service: _____ Signature _____ Date: _____

NRE PO Number: _____

Xilinx Product Engineering Manager: _____ Signature _____ Date: _____

Xilinx Part Number (HPC Code): _____

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XC3300 HardWire™ LCA Design Verification Form

Company Name _____ Customer Name _____

Address _____ City _____ State _____ Zip _____

Telephone ( ) _____ FAX ( ) _____

Customer Part Number _____ Package Type and Temp Grade _____

XC33XX HardWire LCA Options

Device		XC3330	_____	XC3342	_____	XC3390 _____
Input Voltage Levels		TTL	_____	CMOS	_____	
Configuration Time Interval		64 µs	_____	16 ms	_____	
Internal Reset Release		Before I/O's	_____	After I/O's	_____	
D/P Pull-up Resistor		Yes	_____	No	_____	
Oscillator		Inactive	_____	Active	_____	Active/2 _____
Master Mode	Selectable (Controlled by M0)		_____	Unselectable (Forced On)		_____

Customer Part Marking for Device Package (Optional - 11 Characters max.) _ _ _ _ _ _ _ _ _ _ _

Customer Text on Silicon:

☐ No customer text (This is default)

☐ 2 lines of 10 large (20 µ x 30 µ) characters _____

☐ 3 lines of 17 small (12 µ x 18 µ) characters _____

(optional-valid characters: "0-9", "A-Z", "! @$%() [] {} .,/+-_")

XC33XX LCA Design To Be Used for Mask Generation

Filename and Revision Date (.LCA file) _____

HardWire Terms and Conditions:

Please put a check mark against the following items as applicable. All items need to be checked for a signoff.

☐ The application circuit board must have a provision for configuration program storage (i.e., XC17128, EPROM, etc.). The socket can be left unpopulated when conversion to the HardWire device is made. The HardWire device is designed to provide a cost reduction path for existing fully debugged programmable designs.

☐ I certify that the above listed .LCA file is the correct design.

☐ I have reviewed the attached Xilinx HardWire Review Report (including the list of potentially hazardous nets) and have determined that none of the issues raised will be a problem in the system.

☐ I authorize Xilinx to start the HardWire mask making and fabrication process.

Customer Name _____ Signature _____ Date: _____

Xilinx Design Applications Manager: _____ Signature _____ Date: _____

Xilinx Design Number (HD Code): _____

Xilinx Customer Service: _____ Signature _____ Date: _____

NRE PO Number: _____

Xilinx Product Engineering Manager: _____ Signature _____ Date: _____

Xilinx Part Number (HPC Code): _____

XILINX®

XC2318 HardWire™ LCA Design Verification Form

Company Name _____ Customer Name _____

Address _____ City _____ State _____ Zip _____

Telephone ( ) _____ FAX ( ) _____

Customer Part Number _____ Package Type and Temp Grade _____

XC2318 HardWire LCA Options

Device	XC2064	_____	XC2018	_____
Input Voltage Levels	TTL	_____	CMOS	_____
Configuration Time Interval (D/$\overline{P}$ High)	64 µs	_____	16 ms	_____
Internal Pull-up Resistors:				
D/$\overline{P}$	Yes	_____	No	_____
CCLK	Yes	_____	No	_____
M0	Yes	_____	No	_____
PWRDWN	Yes	_____	No	_____
HDC Operation	Yes	_____	No (I/O Only)	_____
LDC Operation	Yes	_____	No (I/O Only)	_____
DOUT During Configuration	DOUT = DIN	_____	High Impedance	_____
Oscillator	Inactive	_____	Active	_____

Customer Part Marking for Device Package (Optional - 11 Characters max.) _ _ _ _ _ _ _ _ _ _ _

XC2318 LCA Design for Mask Generation

Filename and Revision Date (.LCA file) _____

HardWire Terms and Conditions:

Please put a check mark against the following items as applicable. All items need to be checked for a signoff.

- ☐ The application circuit board must have a provision for configuration program storage (i.e., XC17128, EPROM, etc.). The socket can be left unpopulated when conversion to the HardWire device is made. The HardWire device is designed to provide a cost reduction path for existing fully debugged programmable designs.
- ☐ I certify that the above listed .LCA file is the correct design.
- ☐ I have reviewed the attached Xilinx HardWire Review Report (including the list of potentially hazardous nets) and have determined that none of the issues raised will be a problem in the system.
- ☐ I authorize Xilinx to start the HardWire mask making and fabrication process.

Customer Name _____ Signature _____ Date: _____

Xilinx Design Applications Manager: _____ Signature _____ Date: _____
Xilinx Design Number (HD Code): _____

Xilinx Customer Service: _____ _____ Signature _____ Date: _____
NRE PO Number: _____

Xilinx Product Engineering Manager: _____ Signature _____ Date: _____
Xilinx Part Number (HPC Code): _____

HardWire™ LCA Custom Mark Request

Customer _____

Address _____

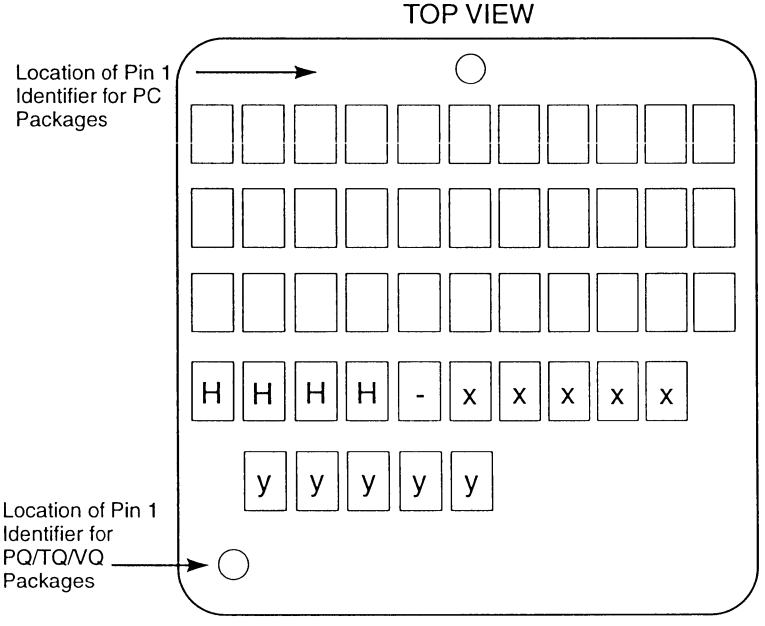
City _____ State _____ Zip _____

Customer Part Number _____

Customer Part Description _____

Xilinx Part Number Number _____

Customer requests that their HardWire devices of the referenced Xilinx part number be custom marked as shown below. Customer acknowledges that if they subsequently desire to change the custom marking, they are responsible for existing inventory at the standard purchase price.



Notes:

1. A maximun 3 lines (including any desired logo or graphics)
2. Max 11 characters per line
3. Mark is center justified
4. Camera-ready artwork must be provided for all desired graphics or logos.
5. $500 setup fee for custom marking

Legend:

HHHH = Xilinx HPC code

xxxxx = reserved

yyyyy = Date Code ID

Customer Acceptance:

Signature _____ Date _____

Title _____ ☐ CUSTOMER ARTWORK ATTACHED

HardWire™ LCA Pre-production Release Authorization

Customer _____

Address _____

City _____ State _____ Zip _____

Customer Part Number _____

Customer Part Description _____

Customer P.O. Number _____

Quantity Ordered _____

Device Price _____

Xilinx Part Number _____

Xilinx H.D. Number _____

Customer acknowledges that he is requesting Xilinx to manufacture additional quantities of custom HardWire product prior to customer approval of HardWire prototypes. By so doing, Customer accepts liability for the requested quantity of devices at the mutually agreed upon price. The acceptance criteria for these pre-production units are that the product must pass the Xilinx test program based upon the approved Customer design (.LCA) file.

The Customer also acknowledges that the purchase order for this product is non-cancellable, and that the pre-production devices are nonrefundable.

Customer Acceptance:

Signature _____

Title _____

Date _____

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HardWire™ LCA Prototype Approval Form

This form certifies that the HardWire prototypes have been fully evaluated and function correctly in the intended application. Xilinx is authorized to commit this design to production upon receipt of customer Purchase Order. A change in the design will result in customer liability for any work in process.

HardWire LCA Device _____

Customer Part Number _____

HardWire LCA Device Number _____

Name _____

Signature _____ Date _____

Title _____

Company _____

Address _____

City _____ State _____ Zip _____

Phone ( ) _____

For Xilinx Internal Use Only

- Customer Part Number _____
- Xilinx Part Number (HPC Code) _____
- Xilinx HardWire Design Number (HD Code) _____

Xilinx Inc.
2100 Logic Drive
San Jose, California 95124-3400
(408) 559-7778
FAX: (408) 559-7114

XILINX®

SECTION 6

Index, Sales Offices

Table of Contents

Index

Sales Offices

HEADQUARTERS

XILINX, Inc.
2100 Logic Drive
San Jose, CA 95124 U.S.A.
1 (408) 559-7778
TWX: 510-600-8750
FAX: 408-559-7114

XILINX SALES OFFICES

NORTH AMERICA

XILINX, Inc.
3235 Kifer Road
Suite 320
Santa Clara, CA 95051
(408) 245-1361
FAX: 408-245-0517

XILINX, Inc.
15615 Alton Parkway
Suite 280
Irvine, CA 92718
(714) 727-0780
FAX: 714-727-3128

XILINX, Inc.
61 Spit Brook Rd.
Suite 403
Nashua, NH 03060
(603) 891-1096
FAX: 603-891-0890

XILINX, Inc.
65 Valley Stream Parkway
Suite 140
Malvern, PA 19355
(610) 296-8302
FAX: 610-296-8378

XILINX, Inc.
939 North Plum Grove Road
Suite H
Schaumburg, IL 60173
(708) 605-1972
FAX: 708-605-1976

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5952 Six Forks Road
Raleigh, NC 27609
(919) 846-3922
FAX: 919-846-8316

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4141 Blue Lake Circle
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FAX: 214-960-0927

EUROPE

XILINX, Ltd.
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Tel: (44) 932-349401
FAX: (44) 932-349499
XILINX Sarl
Z.I. de la Bonde-Bât.B
1 bis, rue Marcel Paul
91742 Massy Cedex
France
Tel: (33)1-60-13-34-34
FAX: (33)1-60-13-04-17

XILINX GmbH
Dorfstr. 1
85609 Aschheim
Germany
Tel: (49) 89-904-5024
FAX: (49) 89-904-4748

JAPAN

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