PCDC V6366

APPLICATION MANUAL

YAMAHA

V6366アプリケーションマニュアル
CATALOG No. : LSI-2463660
1987.6

PREFACE

This Manual is a collection of interfacing information and sample applications which focuses on the internal register functions and methods for use of the V6366 PCDC (Panel Display & CRT Display Controller). We hope this Manual will be a useful reference during your use of the V6366.
The V6366 incorporates the MC6845 CRT Controller and is compatible with the IBM PC, so we recommend that you refer to the following materials in conjunction with this Manual:

- The MC6845 Data Book (for example, the sections regarding "HD6845" and "HD6845S" of the Hitachi Microcomputer Data Book)
- The sections regarding the "Monochrome Display" and "Color/Graphics Monitor Adapter" of the IBM PC Technical Reference
- The Owner's Manual for the Hercules Graphics Card

We hope that you will inform us of any comments and questions that you might have regarding the contents of this Manual.

November 1986

NIPPON GAKKI, Ltd.
Semiconductor Division

TABLE OF CONTENTS

1. GENERAL DESCRIPTION

The PCDC (Panel Display & CRT Display Controller) is a display controller that has the two functions: (1) the display control of a high-capacity flat-panel display (hereafter referred to as a "Panel") and (2) the display control of a raster-scan type CRT. By merely performing initialization, however, even the Panel can be used without changing the software for conventional CRTs, enabling the simple system configuration of a handheld or portable computer which uses the Panel. (If so required, the PCDC can also be used to switch the display monitor between a CRT and a Panel.)

The PCDC is compatible with the CGA (Color Graphics Adapter), MDA (Monochrome Display Adapter), and HGC (Hercules Graphics Card), all for IBM PC application. In case the software and hardware for connecting a regular monitor come as a pair, the PCDC offers compatibility without requiring software changes (initialization is also unnecessary). Even in case of connecting different monitors, initialization will only be performed once at Power Start-Up, then compatibility will be available without requiring any software changes. It is thus possible, for example, to run CGA software using an IBM monochrome monitor and the Panel. (A gray scaling/hatching display can be used with a monochrome monitor.)

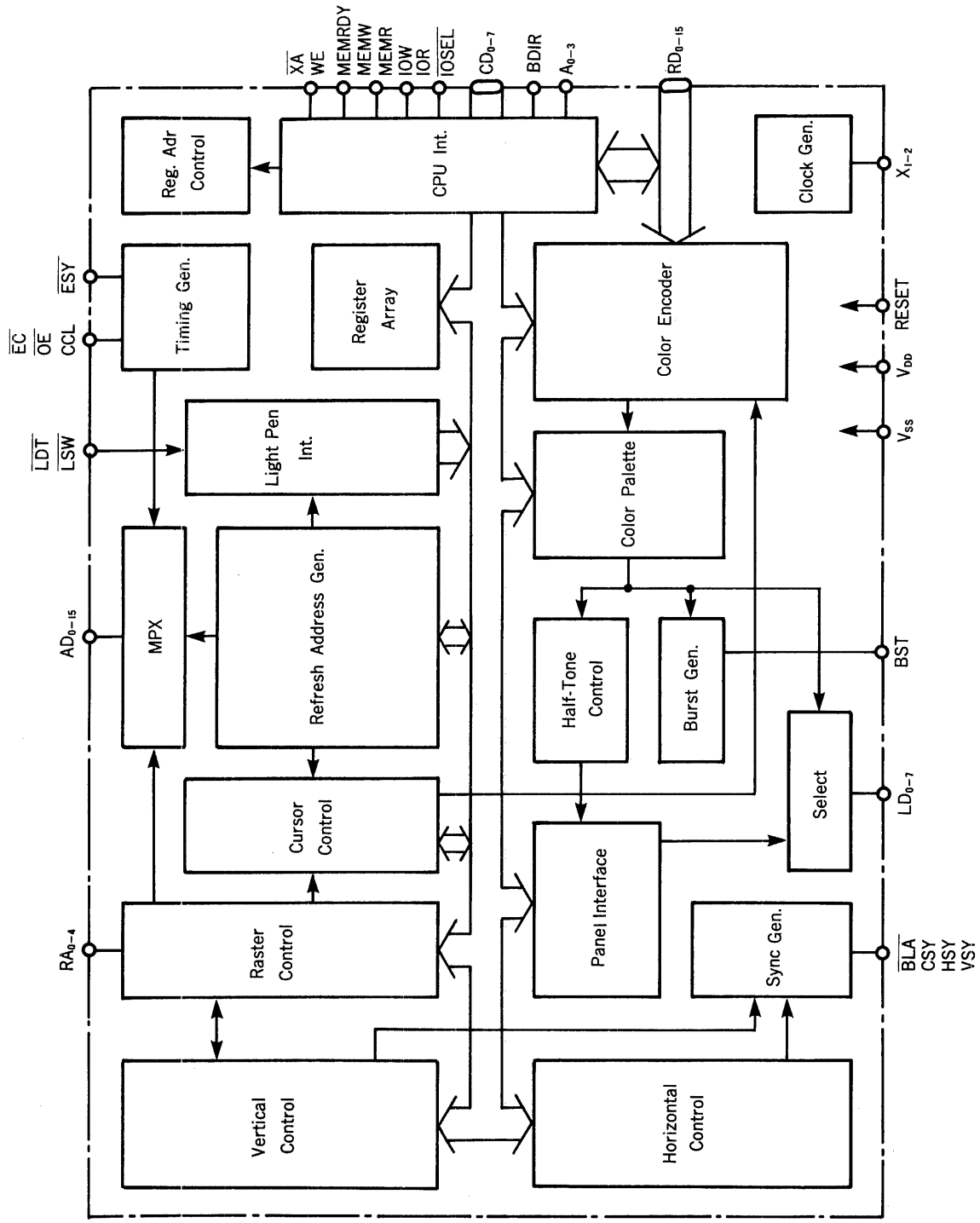
Because the PCDC has the display capacity of the IBM PC as well as numerous other expansion functions, including Kanji display, Color Palette, and the capability to simultaneously display up to 256 colors, a high-performance display system can be easily configured.

1-1. FEATURES

- All functions of MC6845 are built in (excluding the Interlacing & Video Mode and the Skew function).
- In addition to a CRT or LCD, a EL and Plasma Display can also be connected.
- A 640 by 400 PEL Panel can be driven (a 720 by 350 PEL Panel can also be driven).
- A one-screen Panel or two-screen Panel (split into top and bottom halves) can be used.
- Selection of 1-, 2-, 4- or 8-bit parallel transmission of data to the Panel.
- A two-screen panel allows, at a maximum 1/256 duty, display of up to 512 lines.
- A gray scaling/hatching display can be used with the Panel or a monochrome monitor.
- IBM PC software for 640 by 200 PELs can be directly displayed on a 640 by 400 PEL screen. (An 8 by 16 character font can be used, and can be displayed even in Double Scan Mode.)
- In addition to the standard IBM PC Graphics Modes, a variety of other Graphics Modes are provided: 320 by 200 PELs x 16 or 256 colors, 320 by 400 PELs x 4 or 16 colors, 640 by 200 PELs x 4 or 16 colors, 640 by 400 PELS x 4 colors, 640 by 350 PELs x 16 colors, and so on.
- A Protect Bit is provided for software protection.
- An SRAM or DRAM can be used as the VRAM. (Because the timing for display and the CPU are separate, the CPU can access VRAM at any time (without awaiting the retrace-timing.))
- Built-in interface for the Light Pen
- With a linear RGB monitor, 16 out of 512 colors can be simultaneously displayed.
- With an EGA monitor, 16 out of 64 colors can be simultaneously displayed.
- A Color Lookup Table can even be used with an IBM color monitor.
- A Standby function is provided to conserve power dissipation.
- Kanji display capacity of 16 by 16, 24 by 24 or 32 by 32 "PELs" (picture elements or pixels). (Attributes can also be used).
- The font configuration can be selected. Horizontal: 6, 7, 8, 9, 10, or [8 x integer] PELs (capable of a mixed display of half-width and full-width text); Vertical: 1 to 32 PELs.
- Capable of smooth scrolling and (in Interlace Mode only) external synchronization
- The simultaneous display capability with an IBM color monitor and a one-screen LCD of 640 x 200.
- CMOS, 5V power supply, 100-pin QFP or 84-pin PLCC

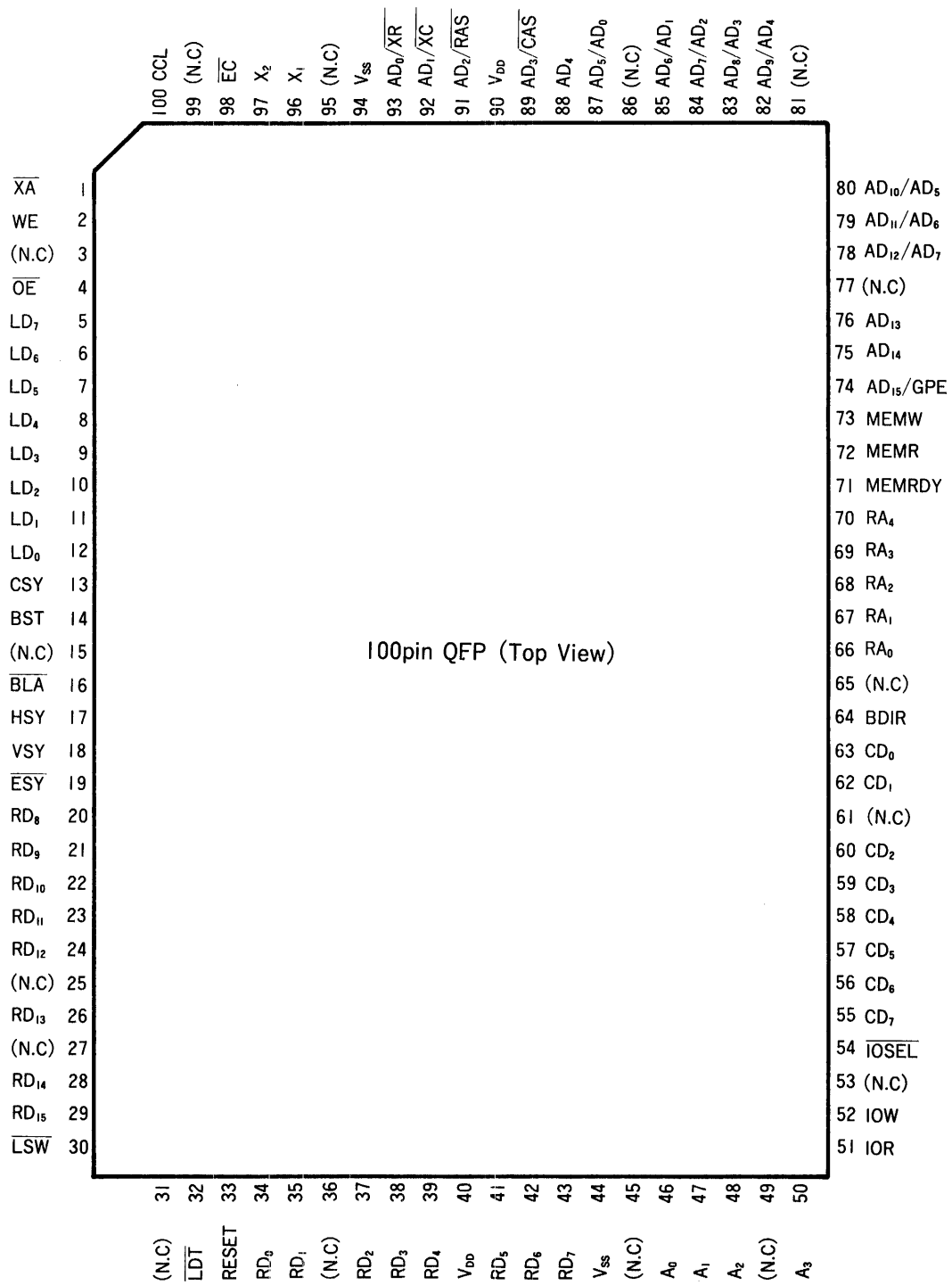
2. FUNCTIONAL OVERVIEW

2-1. BLOCK DIAGRAM

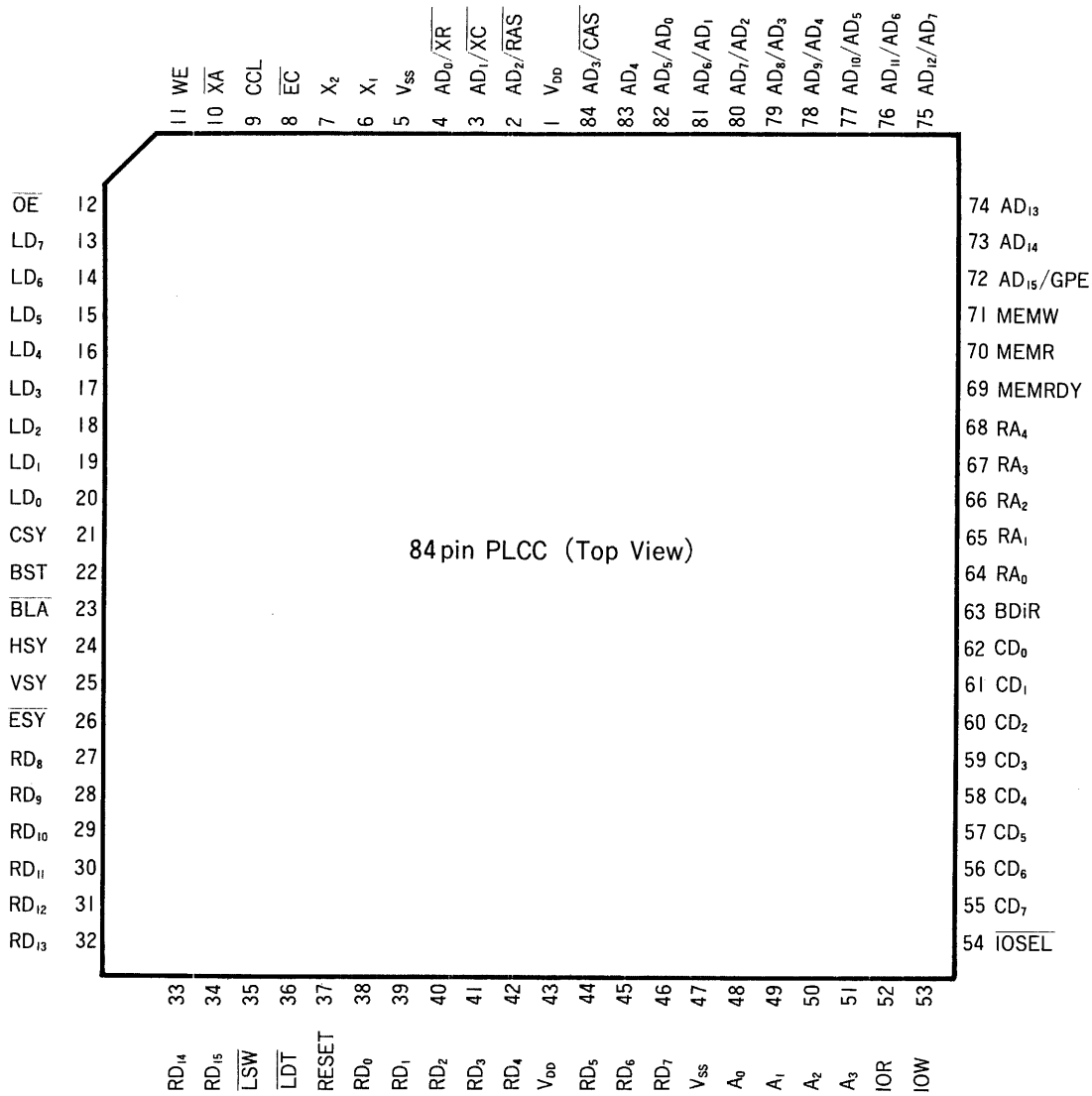


2-2. PIN ASSIGNMENT

2-2-1. 100-Pin QFP



2-2-2. 84-Pin PLCC



2-3. DESCRIPTION OF TERMINAL FUNCTIONS

Signal Name	I/O	Terminal Functions
A_0 ~ A_3	I I	Address for I/O register selection. A_0 is also used for selecting the high or low byte.
CD_0 ~ CD_7	I/O I/O	Data Bus for the CPU
MEMRDY	O	Read/Write Ready signal for the Memory ('0': Wait)
MEMW	I	Controls writing to Memory
MEMR	I	Controls reading from Memory
IOW	I	Controls writing to the I/O registers
IOR	I	Controls reading from the I/O registers
$\overline{\text{IOSEL}}$	I	Enable signal to the I/O Register D and E ('0': Enable)
RESET	I	Reset signal
$\overline{\text{LSW}}$	I	Light Pen Switch signal (At RESET, specifies an 8- or 16-bit Data Bus for VRAM)
$\overline{\text{LDT}}$	I	Light Pen Detection signal (At RESET, specifies VRAM from SRAM or DRAM)
X_1	I	For X'tal oscillation or external clock input
X_2	I/O	
BDIR	O	Direction control of the bi-direction buffer for the CPU Data Bus
RA_0 ~ RA_3	O O	Raster Address
RA_4	I/O	Raster Address or AC Conversion signal (At RESET, specifies the Hercules or CGA Mode)
RD_0 ~ RD_7	I/O I/O	Data bus for VRAM (Low side)
RD_8 ~ RD_{15}	I/O I/O	Data bus for VRAM (High side)
$\overline{\text{EC}}$	O	Transmission control for the RD Bus of Character Font Data
$\overline{\text{OE}}$	O	Output control (for SRAM)
CCL	O	Latch clock for character codes
WE	O	Controls writing of VRAM
$\overline{\text{XA}}$	O	CPU-related timing for VRAM
V_{SS}	I	0V
V_{SS}	I	
V_{DD}	I	+5V
V_{DD}	I	

Signal Name	I/O	Terminal Functions
AD0/$\overline{XR}$	O	CPU RAS Address timing for DRAM
AD1/$\overline{XC}$	O	CPU CAS Address timing for DRAM
AD2/$\overline{RAS}$	O	$\overline{RAS}$ for DRAM
AD3/$\overline{CAS}$	O	$\overline{CAS}$ for DRAM
AD4	O	
AD5/AD0	O	
AD6/AD1	O	
AD7/AD2	O	Addresses of SRAM / Addresses of DRAM
AD8/AD3	O	
AD9/AD4	O	
AD10/AD5	O	
AD11/AD6	O	
AD12/AD7	O	
AD13	O	
AD14	O	
AD15/GPE	O	Also, OR output of Bits 0 and 1 of the Control Register in Hercules Mode

LD4	O	DB	for IBM color monitor	Primary	B	for EGA monitor	B0	for linear RGB monitor	LD4
LD5	O	DG		Primary	G		B1		LD5
LD6	O	DR		Primary	R		B2		LD6
LD7	O	DI		Secondary	G		G0		LD7
LD0	O	$\overline{BFP}$		←			←		LD0
LD1	O						G1		LD1
LD2	O			Secondary	R		G2		LD2
LD3	O	Video		Secondary	B		R0		LD3
$\overline{BLA}$	O	$\overline{BLANK}$		←			R1		$\overline{HSY}$
BST	O	Color Burst		←			R2		SCK
CSY	O	Composite Sync		←			←		$\overline{VSY}$
HSY	O	Horizontal synchronization		←			←		(ECK)
VSY	O	Vertical synchronization		←			←		
$\overline{ESY}$	I/O	for external synchronization							

for Panel

3. I/O REGISTERS

All operations of the PCDC are controlled by the settings of the I/O registers. For example, the setting of the monitor's cycle and Sync signal position is performed by the 6845 Index/Data Register, and the switching between the alphanumeric display and graphics display is performed by the Mode Register. A large number of the I/O registers have IBM PC-compatible addresses and functions. The expansion functions for IBM PC, beginning the setting for the connection method with the Panel, are organized within the Register Bank. Therefore, by merely performing initialization at Power Start-Up, IBM PC software can be used without requiring any changes. (In case of the standard combination consisting of software and a monitor which do not require the expansion functions, initialization also becomes unnecessary.)

ADDRESS					DATA								R/W	
Hex	A_3	A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0, 2, 4, 6	0	×	×	0	×	×	×	6845 Index					W	
1, 3, 5, 7	0	×	×	1	6845 Data								R/W	(× : Don't care)
8	1	0	0	0	Mode	×	Mode						R/W	★
9	1	0	0	1	×	×	Color						R/W	★ Preset Light-Pen (in Hercules Mode)
A	1	0	1	0	Sta-tus	×	×	×	Status				R	
B	1	0	1	1	×	×	×	×	×	×	×	×	W	Clear Light-Pen
C	1	1	0	0	×	×	×	×	×	×	×	×	W	Preset Light-Pen (in CGA Mode)
D	1	1	0	1	×	×	Bank Address						W	
E	1	1	1	0	Bank Data								W	
F	1	1	1	1	Control/ID								R/W	★

NOTES:

1. The register marked with a "★" symbol can be read when RREG = '1' (for a multi-tasking OS; see subsection 3-6-15, "Address 29H").
2. Registers D and E (Bank Address and Data) can only be written when the $\overline{\text{IOSEL}}$ pin is '0'. (Furthermore, they cannot be written unless Bit 7 ($\overline{\text{Protect}}$) of the Control/ID Register is '1'.)
3. When a write-only register is read, it will assume high-impedance status (and the BDIR pin will also output '0').

Writing to the registers is controlled by the IOW pin. (While IOW = '1', the contents of Data Bus CD_0-CD_7 are written to the registers). Reading of the registers is controlled by the IOR pin. (While IOR = '1', the data from the registers are output to Data Bus CD_0-CD_7.) With a 80 type CPU, writing to the registers is executed by the I/O OUT command, whereas reading of the registers is executed by the I/O IN command. A register is selected according to the lower four bits of the Address signal from the CPU at the A_0-A_3 pins.

When an I/O register has been read, the conditions for output to Data Bus CD_0-CD_7 are as follows: [(I/O Registers 8 + 9) x RREG + (I/O Registers A + F) + 6845 Data Register] x IOR

In all other cases, the I/O register will assume high-impedance status. The BDIR pin will also be set to '1' under the preceding conditions. Consequently, when PCDC is used as an MDA, the I/O Registers C, D, and E will be assigned for printer use by IBM PC; however, even when those registers are read, there is no fear of their data colliding on the Data Bus. If the $\overline{\text{IOSEL}}$ pin is set to a decode value that differs from "3BH" for monochrome use, any attempts to write to the Register Bank will be unsuccessful (That is, even if the $\overline{\text{IOSEL}}$ pin is decoded as "3BH", the registers will be protected by Bit 7 ($\overline{\text{Protect}}$) of the Control/ID Register.), thereby maintaining the PCDC's compatibility with IBM PC.

3-1. 6845 INDEX/DATA REGISTERS

6845 performs such functions as the generation of Horizontal and Vertical Sync signals, generation of the Refresh address to the VRAM for storing the Display Data, cursor control, Light Pen detection, and so on.

Index					Reg. No.	Reg. Type	Data								R/W	Preset Mode
A_4	A_3	A_2	A_1	A_0			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	0	0	0	0	R_0	Horiz. Total									W	Pre
0	0	0	0	1	R_1	Horiz. Disp									W	
0	0	0	1	0	R_2	Hsy. Position									W	OS
0	0	0	1	1	R_3	Sync. Width	V_3	V_2	V_1	V_0	H_3	H_2	H_1	H_0	W	Pre
0	0	1	0	0	R_4	Vert. Total									W	Pre
0	0	1	0	1	R_5	Vert. Adjust	×	×	×						W	Pre
0	0	1	1	0	R_6	Vert. Disp									W	
0	0	1	1	1	R_7	Vsy. Position									W	OS
0	1	0	0	0	R_8	Interlace	×	×	×	×	×	×	×	S	W	Fix
0	1	0	0	1	R_9	Max. Scan	×	×	×						W	Pre
0	1	0	1	0	R_{10}	Cur. Start	×	B	P						W	OS
0	1	0	1	1	R_{11}	Cur. End	×	×	×						W	OS
0	1	1	0	0	R_{12}	Start Adr. (H)	×	×							R/W	
0	1	1	0	1	R_{13}	Start Adr. (L)									R/W	
0	1	1	1	0	R_{14}	Cur. Adr. (H)	×	×							R/W	
0	1	1	1	1	R_{15}	Cur. Adr. (L)									R/W	
1	0	0	0	0	R_{16}	Light Pen (H)	×	×							R	
1	0	0	0	1	R_{17}	Light Pen (L)									R	

Preset Mode
[Pre:
Preset value
OS:
Offset value
Fix:
Fixed to Non-Interlace Mode
Blank:
Use of 6845 Register
⇧
When PRE = '1'

(× : Don't care)

NOTES:

1. A11'0' will be output when a write-only register is read (and the BDIR pin will also output '1').
2. When a read/write register is read, the registers marked with an "X" will output '0'.
3. Bit 7 of R_4, R_6, and R_7 as well as V_3-V_0 of R_3 are valid only when 45S = '1'. (The default status after Reset is 45S = '0'. See subsection 3-6-5, "Address 3FH.")

3-1-1. Index Register

The Index Register is a five-bit address register for specifying R0 to R17 of the 6845 Register. Prior to writing to or reading R0-R17, it is necessary to write the addresses to this register.

3-1-2. Horizontal Total Register (R0)

This register sets the cycle for horizontal scanning. When the total quantity of horizontal characters is "M", "M-1" shall be written to this register. In Interlace Mode, the "M" value must be an even number. Set this "M" value to an even number in High Resolution Text Mode as well (because if the value is set to an odd number, it will be regarded as "an odd number + 1").

3-1-3. Horizontal Displayed Register (R1)

This register sets the total quantity of display characters per line, and is set with an arbitrary value that is smaller than the total quantity of horizontal characters. In High Resolution Text Mode, an even number shall be set (because the setting of an odd number will be regarded as "an odd number - 1").

3-1-4. Horizontal Sync Position Register (R2)

This register sets the position of the Horizontal Sync signal, and is set in horizontal character units. An arbitrary value that is smaller than the total quantity of horizontal characters can be set. When the horizontal sync position is set to the "Hth" character, "H - 1" will be written to this register.

3-1-5. Sync Pulse Width Register (R3)

This register sets the respective pulse widths for Horizontal and Vertical Sync signals. The pulse width for Horizontal Sync signals is set in horizontal character units within a range of 1-15 ("0" cannot be used) at the lower four bits of this register. The pulse width for Vertical Sync signals is set in horizontal scan units at its upper four bits. When 45S = '1', a value in the 1-16 range (an "0" setting will be regarded as "16") can be set at the upper four bits; when 45S = '0', the upper four bits will be set to "16" regardless of their contents.

3-1-6. Vertical Total Register (R4)

This register sets the cycle for vertical scanning. When the total quantity of character-lines is "N", "N - 1" will be written to this register.

3-1-7. Total Raster Adjust Register (R5)

This register adjusts the total quantity of scan lines per field, and the raster quantity that is appended to the end of one field shall be set within a 0-31 range. Write "0" when a two-screen panel is in use. (In case the software prevents "0" from being written, assume Preset Mode then set Vert. Adjust to "0".)

3-1-8. Vertical Displayed Register (R6)

This register sets the time period for vertical display, and shall be set in character-line units to an arbitrary value that is smaller than the total quantity of vertical characters.

3-1-9. Vertical Sync Position Register (R7)

This register sets the position of the Vertical Sync signal, and is set in character-line units. An arbitrary value that is smaller than the total quantity of vertical characters can be set. When the vertical sync position is set to the "Vth" line, "V - 1" will be written to this register.

NOTE:

When 45S = '1', writing to Bit 7 of R4, R6 and R7 can be performed; when 45S = '0', however, '0' will be compulsorily written.

3-1-10. Interlace Register (R8)

This register specifies the Raster Scan Mode. Setting the LSB "S" to '0' will select Non-Interlace Mode; setting it to '1' will select Interlace Mode. (The Interlacing & Video Mode is not supported. The CUDISP Skew and DISPTMG Skew functions are also not supported.)
In Interlace Mode, scanning will be performed so that the rasters of the odd fields will interpolate those of the even fields.
In Non-Interlace Mode, these rasters of even and odd fields follow the same track.
The Panel can only use the Non-Interlace Mode.

3-1-11. Maximum Raster Address Register (R9)

This register sets the quantity of rasters for one character-line, including the space between lines. When the raster quantity for one line is "RN", "RN - 1" will be written to this register.

3-1-12. Cursor Start Raster Register (R10)

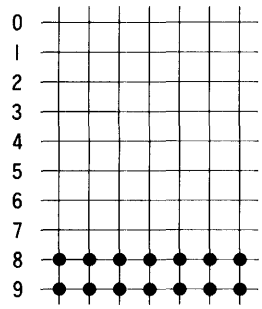
This register specifies the Raster address for starting the cursor display as well as specifying the cursor display mode. The Raster address for starting cursor display is set at the lower five bits of this register, and the cursor display mode is specified at its higher two bits.

D6 B	D5 P	Cursor Display Modes
×	0	Cursor blinks in 16-field cycles (ON : OFF ratio = 1 : 1)
0	1	Cursor is not displayed
1	1	Cursor blinks in 32-field cycles (ON : OFF ratio = 1 : 3)

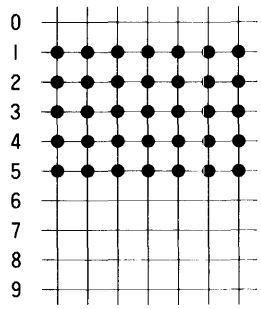
(× : Don't care)

3-1-13. Cursor End Raster Register (R11)

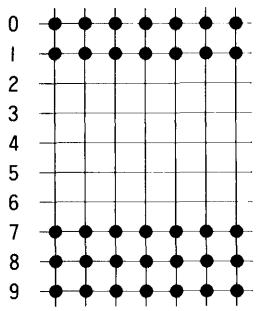
This register sets the Raster address for ending the cursor display.



Cursor Start Address = 8
Cursor End Address = 9



Cursor Start Address = 1
Cursor End Address = 5



Cursor Start Address = 7
Cursor End Address = 1

Cursor Setting Values and Display Examples

The Cursor Start Address and Cursor End Address will generally satisfy the following condition:

$0 \leqq$ Cursor Start Address $\leqq$ Cursor End Address $\leqq$ Maximum Raster Address

However, in case the relationship between the Cursor Start and End Addresses is the opposite of the above, the cursor will be displayed as split into top and bottom halves. If only the Cursor End Address is larger than the Maximum Raster Address, the cursor will be displayed at all rasters (in character units). Conversely, if only the Cursor Start Address is larger than the Maximum Raster Address, the cursor will not be displayed.

3-1-14. Start Address Registers (R12, R13)

These registers set the Memory Address for starting the screen display. (R12 is the high-order portion of the address, and the total address consists of 14 bits). By dynamically rewriting the contents of these registers, paging and scrolling can be easily performed.

3-1-15. Cursor Address Registers (R14, R15)

These registers set the Display Address of the cursor. (R14 is the higher-order portion of the address, and the total address consists of 14 bits.)

3-1-16. Light Pen Registers (R16, R17)

These registers memorizes the Detection Address for the Light Pen. (R16 is the higher-order portion of the address, and the total address consists of 14 bits.) Since the Memory Address at the rising edge of the Light Pen Strobe signal ($\overline{\text{LDT}}$ pin) is memorized, it is necessary to consider the delay of the Light Pen Detection Circuit and rectify the Memory Address. With LCDs and similar panels, this register is invalid (that is, the register can be read, but its contents will have no meaning).

3-1-17. Precautions on Usage

Be sure to write to the Cursor Address Register during the horizontal/vertical retrace timing, and write to the Start Address Register during the displayed timing. For the other registers, avoid writing during display as much as possible (in case writing is performed, a momentary flickering of the screen may occur). Especially in the case of the Horizontal Total Register, Vertical Total Register, Interlace Register, and Maximum Raster Address Register, the scanning cycles are likely to become chaotic.

If Bit 3 (Enable Video) of the Mode Register is set to '0', the display will be switched OFF, eliminating the need to consider the timing for writing to the registers.
The CRT Controller 6845 is available in two types, 6845 and 6845S, which are slightly different. The relationship and differences between these two types and the PCDC are summarized as follows:

Different Functions	6845	6845S	PCDC
Interlacing & Video Mode	The method for setting the quantity in the vertical direction, the quantity of rasters per line, and the cursor display are different.		No support
Vertical Sync signal Pulse width	Fixed to 16-raster width	Programmable from 1 to 16	Similar to 6845 when 45S = '0'
			Similar to 6845S when 45S = '1'
Skew function	None	DISPTMG and CUDISP have the Skew function	None
Start Address	Reading impossible	Reading possible	Reading possible
Cursor display (When Start Address is larger than End Address)	Displayed split into top and bottom halves	No display	Displayed split into top and bottom halves
Cursor Display Mode (When B = P = 0)	Cursor does not blink	Cursor does not blink	Cursor blinks every 16 fields
Vertical-direction setting Bit quantity of registers	7 bits	7 bits	7 bits when 45S = '0' 8 bits when 45S = '1'

NOTES:

1. The registers for setting the vertical direction indicate the Vertical Total Register (R4), Vertical Displayed Register (R6), and Vertical Sync Position Register (R7). (With PCDC, the bits up to Bit 8 can be set.)
2. The Default status after RESET of PCDC is 45S = '0'.
3. The IBM-PC sets the cursor display mode at B = P = 0 while enabling the 16 field blinking in the external circuit.

3-1-18. Sample Setting Values using IBM PC

Reg. No.	Reg. Type	CGA			Hercules	
		Text		Graphic	Text	Graphic
		80×25	40×25		80×25	
R 0	Horiz.Total	71	38	38	61	35
R 1	Horiz.Disp	50	28	28	50	2D
R 2	Hsy.Position	5A	2D	2D	52	2E
R 3	Sync.Width	0A	0A	0A	0F	07
R 4	Vert.Total	1F	1F	7F	19	5B
R 5	Vert.Adjust	06	06	06	06	02
R 6	Vert.Disp	19	19	64	19	57
R 7	Vsy.Position	1C	1C	70	19	57
R 8	Interlace	02	02	02	02	02
R 9	Max.Scan	07	07	01	0D	03
R 10	Cur.Start	06	06	—	0B	—
R 11	Cur.End	07	07	—	0C	—

(in Hexadecimal)

Generally, the values listed in the preceding table are the setting values for IBM PC. In the following, the horizontal/vertical cycle shall be calculated from the master clock frequency.

1. Since the master clock frequency of CGA is 14.318 MHz, a character unit in Graphics Mode consists of 16 PELs, and R0 (Horiz. Total) is "56" in decimal, the horizontal cycle will be as follows:

$$\frac{14.318/16}{56+1} = 0.01569956 \text{ MHz} \rightarrow 15.7 \text{ KHz}$$

R4 (Vert. Total), R5 (Vert. Adjust), and R9 (Max. Scan, which determines the bank number for bank switching) are respectively "127", "6", and "1" in decimal, and the quantity of scan lines becomes (127 + 1) x (1 + 1) + 6 = 262 lines, so that the vertical cycle will be as follows:

$$\frac{15.69956}{262} = 0.05992 \text{ KHz} \rightarrow 59.9 \text{ Hz}$$

These values are close to the values of Horizontal Cycle = 15.75 KHz and Vertical Cycle = 60 Hz, which are the specifications of the IBM color monitor.

2. Since the master clock frequency of HGC is 16.257 MHz, the font configuration in Text Mode is 9 by 14 PELs (Max. Scan is determined according to the 14 PELs in the vertical direction), and R0 is "97" in decimal, the horizontal cycle will be as follows:

$$\frac{16.257/9}{97+1} = 0.01843197 \text{ MHz} \rightarrow 18.43 \text{ KHz}$$

R4, R5, and R9 are respectively "25", "6", and "13" in decimal, and the quantity of scan lines becomes (25 + 1) x (13 + 1) + 6 = 370 lines, so that the vertical cycle will be as follows:

$$\frac{18.43197}{370} = 0.049816 \text{ KHz} \rightarrow 49.8 \text{ Hz}$$

These values are close to the values of Horizontal Cycle = 18.432 KHz and Vertical Cycle = 50 Hz, which are the specifications of the IBM monochrome monitor.

3-2. MODE REGISTER (I/O Register 8)

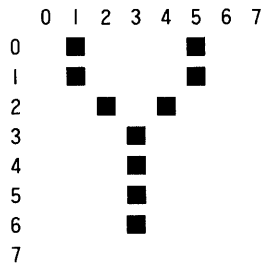
(Cleared by RESET)			(Can be read when RREG='1')
Bit	**0**	High Resolution Text	(Fixed to "1" in Hercules Mode)
	1	Graphics	
	2	Black/White	(Fixed to "1" in Hercules Mode)
	3	Enable Video	
	4	High Resolution Graphics	(Fixed to "1" in Hercules Mode)
	5	Blink	
	7	Page Set	(Valid only in Hercules Mode)

NOTE:

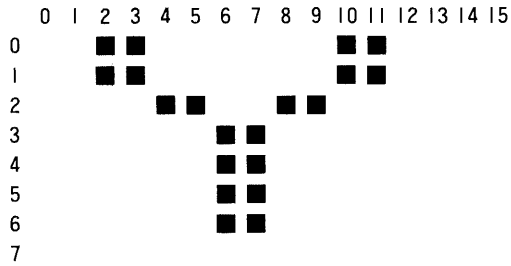
In Hercules Mode, Bit 1 (Graphics) can only be written when Bit 0 of the Control/ID Register is '1'. Bit 7 (Page Set) can only be written when Bit 1 of the Control/ID Register is '1'.

This register sets the Operating Mode. The function of each bit is described as follows:

Bit 0: Selects the text resolution for Text Mode (Bit 1 (Graphics) = '0'). When Bit 0='1' (High Resolution Text Mode), the data from the CG-ROM is sequentially displayed in PEL units; however, when Bit 0='0' (Low Resolution Text Mode), the data is expanded so that two PELs (a Double PEL) are displayed at a time.



Bit 0 = '1'



Bit 0 = '0'

Bit 1: Selects either Text Mode or Graphics Mode. Setting Bit 1='1' selects the Graphics Mode.

Bit 2: Selects either Color or B/W Mode. This bit is only valid for Composite signals and 2 Bit Graphics Mode, however, and RGB output will result in color display regardless of this bit's set value. When Bit 2='1', the B/W Mode will be assumed and the Color Burst signals for Composite signals will not be output.

Bit 3: Controls the Display ON/OFF status. When switching modes, be sure to switch the display OFF for a fixed period to avoid the display of disorderly contents on the screen. When Bit 3='0', the display will be switched OFF. At this time, the display of the cursor and border will be continued.

Bit 4: Selects the resolution of Graphics Modes. Setting Bit 4='1' selects High Resolution Graphics Mode. With IBM PC, Bit 4='1' will result in a 640 by 200 PEL Graphics Mode and Bit 4='0' will result in a 320 by 200 PEL Graphics Mode.

Bit 5: Controls the blinking of text (valid only in Text Mode). When Bit 5='1', the MSB of Attribute assumes blinking control and one out of eight colors can be selected for the text background. When Bit 5='0', blinking will be disabled and one out of 16 colors can be selected for the text background. A blink cycle consists of 32 fields.

Bit 7: The Hercules Mode employs 32K bytes for one screen. The 64K-byte FULL Mode has the capacity for two pages, however, and the page is selected by Bit 7. When Bit 7='1', the second page will be displayed.

The mode settings for IBM PC are summarized below. (For details on the Operating modes, see CHAPTER 4, "OPERATING MODES.")

Mode Reg. Bit 5	4	3	2	1	0	MODE	IBM-PC Standard Mode
1	×	1		0	0	Low Resolution Text	40 x 25 A/N
1	×	1		0	1	High Resolution Text	80 x 25 A/N
×	0	1		1	×	Low Resolution Graphic	320 x 200 GR
×	1	1	1	1	×	High Resolution Graphic	640 x 200 GR

Black/White
Enable Video
Blink

× : Don't care

3-3. COLOR REGISTER (I/O Register 9)

Bit 0	SEL—B	}	Selects the border/background colors
1	G		
2	R		
3	I		
4	SEL—Intensified	}	Selects the color in 2 Bit Graphics Mode
5	SEL—Color Set		

This register performs color specification of the border color in Text Mode or color selection in Graphics Modes.

Bits 0-3: Specify the border color in Text Mode or Graphics Modes (excluding 1 Byte High Resolution Graphics Mode). In 2 Bit (four-color) Graphics Mode, they also specify the background color. In 1 Byte High Resolution Graphics Mode, they also specify the color of the PELs. Bits 0 to 3 respectively specify B, G, R, and Intensity.

Bit 4: Specifies the intensity of Colors 1-3 in 2 Bit (four-color) Graphics Mode.

Bit 5: Selects one of two color settings (SET1 or SET2) in 2 Bit (four-color) Graphics Mode. Setting Bit 5 = '1' selects SET2. When Bit 2 of the Mode Register is '1', both SET1 and SET2 will become identical.

The colors in 2 Bit (four-color) Graphics Mode are summarized as follows:

C_1	C_0	Color	SET1				SET2				B/W = 1			
			I	R	G	B	I	R	G	B	I	R	G	B
0	0	Background	SEL I	SEL R	SEL G	SEL B	SEL I	SEL R	SEL G	SEL B	SEL I	SEL R	SEL G	SEL B
0	1	Color 1	SEL IN	0	1	0	SEL IN	0	1	1	SEL IN	0	1	1
1	0	Color 2	SEL IN	1	0	0	SEL IN	1	0	1	SEL IN	1	0	0
1	1	Color 3	SEL IN	1	1	0	SEL IN	1	1	1	SEL IN	1	1	1

NOTES:

1. The background color is specified by Bits 0 to 3.
2. SEL IN is equivalent to Bit 4, and the SET1/SET2 selection is performed by Bit 5.

3-4. STATUS REGISTER (I/O Register A)

	Hercules Mode	CGA Mode
Bit 0	Hsync	$\overline{\text{Display Timing}}$
1	Light Pen Trigger	Light Pen Trigger
2	Light Pen Switch	Light Pen Switch
3	Video	Vsync
7	Vsync	

This read-only register is used to know the LSI internal status. For a large number of 6845 registers, including the Cursor Address Register, it is advisable to perform writing during the horizontal/vertical retrace timing; and it is advisable to write to the Start Address Register during the displayed timing. It is thus necessary to know the LSI internal status (retrace timing or displayed timing). At this time, the Status Register shall be used. (If Bit 3 (Enable Video) of the Mode Register is '0', the display will be switched OFF, eliminating the need for considering the timing for writing to the registers.) The functions of each bit are as follows:

Bit 0: Indicates the timing of Horizontal Sync signals in Hercules Mode (when Bit 0 = '1'), or indicates the displayed timing in CGA Mode (indicating that displayed timing is in process when Bit 0 = '0').

Bit 1: Indicates the contents of the Light Pen flip-flop which shows whether or not the Light Pen Address has been newly memorized at the rising edge of the Light Pen Strobe signal. ($\overline{\text{LDT}}$ pin) Bit 1 = '1' indicates the memorized status.

Bit 2: Indicates the status of the Light Pen's Switch signal ($\overline{\text{LSW}}$ pin). (For IBM PC, Bit 2 = '0' indicates the Switch ON status.) Since chattering prevention circuit is not built-in, chattering must be eliminated by software.

Bit 3: Indicates that Video Dot data is being output in Hercules Mode. This bit is for testing purposes and a '1' setting indicates that the data is being output. It indicates the Vertical Sync signal in CGA Mode (when Bit 3 = '1').

Bit 7: Indicates the Vertical Sync signal only in Hercules Mode (when Bit 7 = '1'). ('0' will be output in CGA Mode.)

3-5. CLEAR/PRESET LIGHT PEN

	Hercules Mode	CGA Mode
Preset Light Pen	I/O 9	I/O C
Clear Light Pen	I/O B	I/O B

The Light Pen flip-flop that indicates whether the Light Pen Address has been newly memorized can be cleared by writing to I/O Register B (any data can be written). Setting of the Light Pen flip-flop can be accomplished by writing to I/O Register 9 in Hercules Mode or to I/O Register C in CGA Mode. (Since this bit is for testing purposes, any data can be written at such time.)

The procedure for reading the Light Pen Address is as follows:

1. Clear the Light Pen flip-flop by writing to Register B.
2. Read to Status Register to know whether or not the Light Pen flip-flop was set at the rising edge of the Light Pen Strobe signal.
3. If it was not set, repeat Step 2 above.
   If it was set, read the Light Pen Address (R_{16} and R_{17}) then return to Step 1.

3-6. BANK ADDRESSES AND DATA

Address						Data							
A_5	A_4	A_3	A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	×	×	×	×	×	R_2	R_1	R_0
0	0	0	0	0	1	×	G_2	G_1	G_0	×	B_2	B_1	B_0
0	1	1	1	1	0	×	×	×	×	×	R_2	R_1	R_0
0	1	1	1	1	1	×	G_2	G_1	G_0	×	B_2	B_1	B_0
1	0	0	0	0	0	Duty							
1	0	0	0	0	1	H size							
1	0	0	0	1	0	V adj							
1	0	0	0	1	1	SCT SCU	H adj						
1	0	0	1	0	0	MON ULE	GRM 2 1 0				FON 2 1 0		
1	0	0	1	0	1	SYTH HERC SRAM 8BUS 16CP BINH					CLK 1 0		
1	0	0	1	1	0	RA4 A15 EXP	PB 1 0				PAG 2 1 0		
1	0	0	1	1	1	LS 1 0	IEN EXTS IINH ACM CPLE PRE						
1	0	1	0	0	0	SWC VST SSY SSCK H/E R/M					2SCR 1 0		
1	0	1	0	0	1	STBY RREG ESIO	EH 4 3 2 1 0						
1	0	1	0	1	0	TST 2 1 0	SS 4 3 2 1 0						
1	0	1	0	1	1	CON 7 6 5 4 3 2 1 0							
1	1	0	0	0	0	Horiz. Total							
1	1	0	0	0	1	Hsy. Offset							
1	1	0	0	1	0	Vsy. Offset							
1	1	0	0	1	1	Sync. Width							
1	1	0	1	0	0	Vert. Total							
1	1	0	1	0	1	×	×	×	Vert. Adjust				
1	1	0	1	1	0	×	×	×	Max. Scan				
1	1	0	1	1	1	F/O	TDS 1 0		Cur. Offset				
1	1	1	0	0	0	Horiz. Total							
1	1	1	0	0	1	Hsy. Offset							
1	1	1	0	1	0	Vsy. Offset							
1	1	1	0	1	1	Sync. Width							
1	1	1	1	0	0	Vert. Total							
1	1	1	1	0	1	GOE HDB LAS			Vert. Adjust				
1	1	1	1	1	0	×	×	×	Max. Scan				
1	1	1	1	1	1	45S	GDS 1 0		UL. Position				

The bank address is automatically incremented each time data is written in (I/O register — E).

Color Palette #0

Color Palette #15

Pre OS OS Pre Pre Pre Pre — 6845 Preset Data (For Text)

Pre OS OS Pre Pre Pre Pre — 6845 Preset Data (For Graphics)

x: don't care

The expansion functions from IBM PC are organized within the Register Bank by Registers D and E. Register D serves to specify the address of a register bank, and Register E serves to set the data. (The configuration is similar to that of the 6845 Index/Data Register.) Since the addresses of the register banks are provided with an Auto Increment function, the mere setting of the first address will cause the successive addresses to be automatically incremented by one each time data is written to Register E. In the case of the Color Palette and 6845 Preset Data, this convenient function enables data to be consecutively written.
Due to their relationship to the expansion functions from IBM PC, Registers D and E are provided with software protection by a double-protection feature. Data can be written to the registers only in the case both the $\overline{\text{IOSEL}}$ pin is '0' and Bit 7 ($\overline{\text{Protect}}$) of the Control/ID Register is '1'. Because the contents written to the register are valid regardless of the $\overline{\text{IOSEL}}$ and Bit 7 ($\overline{\text{Protect}}$) status, IBM PC software can be run with confidence if the $\overline{\text{IOSEL}}$ = '1' and Bit 7 ($\overline{\text{Protect}}$) = '0' settings are implemented as soon as initialization is completed.

3-6-1. Color Palette (Addresses 00H-1FH)

Regarding the PEL color data IRGB as input, the Color Palette has a 16-address x 9-bit data capacity with respect to the data that is to be converted to the PEL color data which will actually be displayed. Consequently, if three bits each of the nine-bit data are respectively assigned to R, G, and B, then and a linear RGB monitor is connected via a digital-to-analog converter, any 16 out of 512 colors can be simultaneously displayed. If an EGA monitor is connected, six bits can be used as a Color Palette for a simultaneous display of any 16 out of 64 colors. And if an IBM color monitor is connected, four bits can be used as a Color Lookup Table. In any of the above cases, CPLE must be set to '1' (For the linear RGB monitor, the SWC = '1' setting is also required.) When CPLE = '0', the Color Palette will not operate and the PEL color data IRGB will be directly output. The functions of each bit of the Color Palette and their method for use with each monitor is summarized below:

Bit Name for Color Palette	Linear RGB Monitor	EGA Monitor	IBM Color Monitor	Panel
R_2	Red 2^2			Intensity
R_1	Red 2^1			Intensity 2^3
R_0	Red 2^0	Secondary B		Intensity 2^2
G_2	Green 2^2	Secondary R		Intensity 2^1
G_1	Green 2^1			Intensity 2^0
G_0	Green 2^0	Secondary G	I	
B_2	Blue 2^2	Primary R	R	
B_1	Blue 2^1	Primary G	G	
B_0	Blue 2^0	Primary B	B	

NOTE:

The monochrome monitor can also be used in a manner similar to the Panel.
Intensity is used with a monochrome monitor or a plasma display capable of gray scaling.

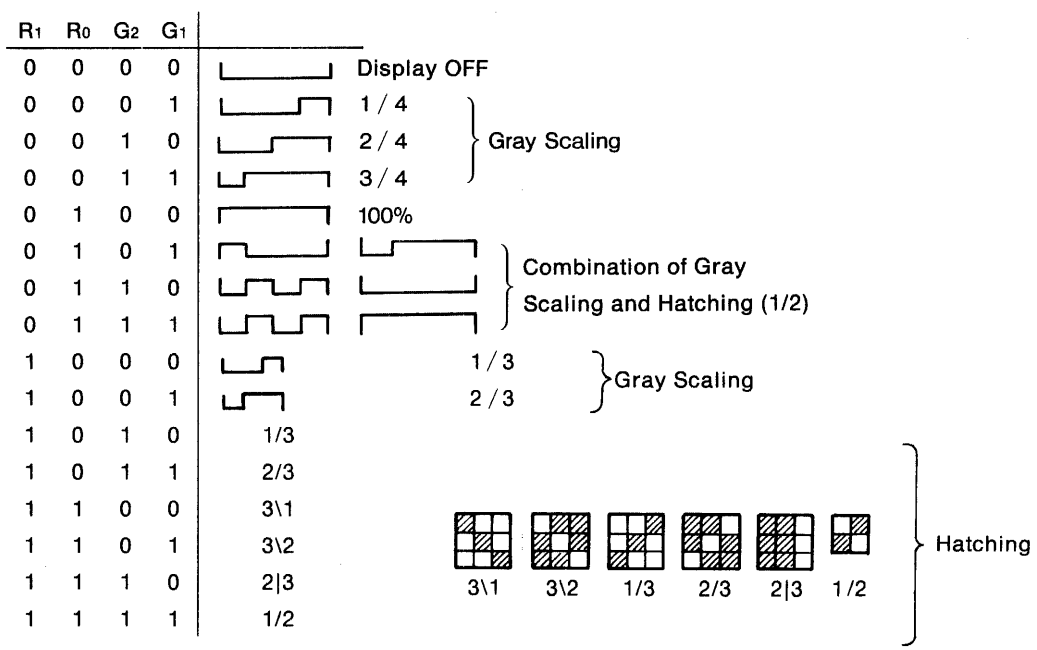
For the Panel, the Color Palette is also used for converting the PEL color data either to a specified half-tone or to a specified hatching pattern. (With a monochrome monitor, the Color Palette can similarly be used for converting to a half-tone or a hatching pattern.) Since the Panel cannot perform

color display, in the case CGA software has been executed, the color data will be indistinguishable unless the color data is converted to some half-tone or hatching pattern. The Color Palette is used for correspondence of the colors with the half-tone and hatching patterns (and must be used with CPLE = '1').

One datum of the Color Palette consists of two bytes, and writing of the data must be performed in the sequence of an even address byte followed by an odd address byte. The data will actually become valid for the Color Palette upon writing an odd address byte.

3-6-2. Gray Scaling and Hatching

In case of display of the CGA software, the Panel (including Monochrome monitors) will be incapable of color display and gray scaling, so the display pattern cannot be distinguished. In such cases, by synchronizing Fields 3 and 4 and changing the transmission frequency of the display data, a graded display can be achieved and converted to a hatching pattern which deals with the color display problem. Because the response rate of an LCD is slow, this method for applying a graying scale is very effective. But the use of a hatching pattern is recommended because flickering of a graying scale will result when a quick responsive papel (plasma display, EL or monochrome monitor) is used. When R1-G1 is set at the upper four bits of the Color Palette, the display will be converted to gray scaling and Hatching according to the below correspondence. (A combined display of gray scaling and hatching is also possible.)



With CGA graphics software, a four-color display is adequate, so it is recommended that the user sets the gray scaling and hatching of his/her own preference. (Since a maximum 16-color display is possible in Text Mode, it is recommended that MON be set to '1' to convert to a monochrome display, then a clear display be implemented (Set Black as Display OFF and White as 100%.).)

With a monochrome monitor or a Panel capable of Intensity input, if IEN is set to '1' and Intensity is set for output to LD7-LD4, a good gray scaling or hatching display can be achieved. (A double-sequence input can be made to the monitor so high or low intensity can be used even for hatching alone.)

3-6-3. 6845 Preset Data (Addresses 30H-36H, 38H-3EH)

In cases of executing CGA software with an IBM color monitor or executing Hercules software with an IBM monochrome monitor, the software and monitor form a standard combination. In such cases, proper operation can be achieved by setting PRE = '0' (Default status after RESET) and using the 6845 Register as is. In cases of executing CGA software with an IBM monochrome monitor or executing CGA software (for 640 by 200 PEL display) with a display having a 640 by 400 PEL display area, it will become necessary to convert the data for 6845 Register to values suitable for the monitor being used. Since certain software may switch often between Text and Graphics Modes, merely initializing the 6845 Register will not result in proper operation in some cases. (The 6845 is rewritten upon changing modes, resulting in improper operation.) To cope with this problem, the 6845 Preset Data is provided. (There are two types of Preset Data each for the Text and Graphics Modes, so proper operation is ensured even if the mode is switched.) That is, the registers related to the horizontal and vertical cycles, which are fixed values according to the monitor (The values cannot be rewritten by software. With the IBM PC software, however, the values written to 6845 and those suitable for the monitor are different.), are set to Preset values (When PRE = '1' in Preset Mode, the Raster Scan Mode will always be fixed to Non-Interlace Mode.) then used in place of the 6845 Registers (thereby enabling the setting of horizontal and vertical cycles that are suitable for the monitor in use). Moreover, the Offset value is introduced to the registers related to the horizontal/vertical sync position and the Cursor Start/End Raster Addresses, which are values that can be rewritten by software but will not directly match the monitor in use, so that the contents of the 6845 Registers will be shifted by this Offset value for use. Furthermore, the other registers, which have a high possibility of being rewritten by software but can be used directly with no problem, the 6845 Registers shall be used as they are.

The 6845 Preset Data is only valid when PRE = '1' in Preset Mode. The Preset value for the Horizontal Total and the Offset value for the Horizontal Sync Position should be written with values in High Resolution Text Mode. In Low Resolution Text Mode, these values will be automatically halved for use.

3-6-3-1. Horiz. Total (Addresses 30H, 38H)

This is the Preset value for the Horizontal Total Register (R_0). In Preset Mode, this value is used in place of the R_0 value. Its setting procedure is identical to that for the 6845 Register R_0.

3-6-3-2. Sync. Width (Addresses 33H, 3BH)

This is the Preset value for the Sync Pulse Width Register (R_3). In Preset Mode, this value is used in place of the R_3 value. Its setting procedure is identical to that for the 6845 Register R_3. (In Preset Mode, this function is equivalent to the 45S = '1' status, regardless of the 45S setting.)

3-6-3-3. Vert. Total (Addresses 34H, 3CH)

This is the Preset value for the Vertical Total Register (R4). In Preset Mode, this value is used in place of the R4 value. Its setting procedure is identical to that for the 6845 Register R4.

3-6-3-4. Vert. Adjust (Addresses 35H, 3DH)

This is the Preset value for the Total Raster Adjust Register (R5). In Preset Mode, this value is used in place of the R5 value. Its setting procedure is identical to that for the 6845 Register R5.

3-6-3-5. Max. Scan (Addresses 36H, 3EH)

This is the Preset value for the Maximum Raster Address Register (R9). In Preset Mode, this value is used in place of the R9 value. Its setting procedure is identical to that for the 6845 Register R9.

Even in cases where the monitor and software do not form the standard combination, this register enables the use of a font suitable to the monitor. For example, CGA software that employs a font of an 8 by 8 PEL matrix can be displayed on a monochrome monitor that uses a 9 by 14 PEL matrix (when this register (Address 36H) is set to 0DH.)

3-6-3-6. Hsy. Offset (Addresses 31H, 39H)

This is the Offset value for the Horizontal Sync Position Register (R2). In Preset Mode, this value is added to the 6845 Register R2 value for use. Since the Offset value is expressed in two's complements, it can be set in the range of −128 to +127. In the case an underflow occurs due to the offset, the sync position is regarded as 00H. Attention is required because no countermeasures are provided in case of an overflow. If no offset is desired, write 00H to the Offset value.

3-6-3-7. Vsy. Offset (Addresses 32H, 3AH)

This is the Offset value for the Vertical Sync Position Register (R7). In Preset Mode, this value is added to the 6845 Register R7 value for use. Since the Offset value is expressed in two's complements, it can be set in the range of −128 to +127. (Care is necessary when a negative value will be set, because unless such setting is performed with 45S set to '1', '1' will not be written to its MSB.) In the case an underflow occurs due to the offset, the sync position is regarded as 00H. Attention is required because no countermeasures are provided in case of an overflow. If no offset is desired, write 00H to the Offset value.

3-6-3-8 Address 3DH

D7	D6	D5	D4	D3	D2	D1	D0
GOE	HDB	LAS	Vert. Adjust				

(GOE, HDB, and LAS are cleared by resets.)

(1) LAS: Output the preset values for the light pen address

With multitasking software such as MS Windows or Sidekick, it is necessary to know whether display is handled in A/N mode or in graphics mode. In the PCDC when RREG goes to '1', it is possible to read the mode registers, etc. but on CGA boards for the IBM-PC, this function is lacking so the mode is inferred with the light pen address. (When the software operates

through the BIOS, the current mode is written in the BIOS RAM, so there is no need for such inference, but some software (for example, Lotus 1-2-3) changes the mode directly without going through the BIOS, so this type of inference is necessary.) For example, such as MS windows when the start of display is detected from the display timing status, the light pen address is latched by the preset light pen (I/O C) and the address (the value near the start address (R12, R13) of the 6845) at the start of display is read in. In addition, when the rising edge of the Vsy status is detected, the light pen address is latched by the preset light pen again and the address at the end of display is read in. The current display mode is inferred from the difference between the address at the end of display and the address at the start of display.
Sidekick assumes 0000H as the start address for the 6845, latches the light pen address with the preset light pen when the falling edge of the Vsy status is detected to read in the current address, and infers the current display mode from this address. Thus when the progress of addresses differs from that for a CRT, as it does for example for LCDs that are divided into top and bottom halves, then the special software compatibility is lost and misoperation occurs. The way that this problem is handled is that when LAS is set to '1' the preset values are output to the light pen address for each mode and the system operates just as if a CRT were connected. Here are the preset values.

Display mode	During the vertical retrace	During display
40 x 25 A/N	0 4 x x H	0 0 x x H
80 x 25 A/N	0 9 x x H	0 0 x x H
Graphics	1 1 x x H	0 0 x x H

Note: Only R16 (uppermost bit of the light pen address) is preset.

(2) HDB: Disable Hercules mode

When Ms Word (Version 4) is started up, it checks the status of Bit 7. If this bit is active, the system judges that an HGC is connected and begins writing the data into Page 1. If the PCDC used with a full Hercules circuit, there would be no problem, but with a half-hercules board (which can only display Page 0) such as the PCDC evaluation board and with MDA circuits, there is misoperation. (When WORD/C is entered, there is no problem, but when just WORD is keys in, there are problems. Version 3 asked which board was being used, so this problem did not occur with Version 3.) This problem is handled by setting HDB to '1' so that Status Bit 7, Control/ID Bit 1 and Bit 0, and Mode Bit 7 do not function, providing compatibility with MDA.

(3) GOE: Output '1' to GPE

GPE is the OR of the outputs from Bits 0 and 1 of the Control/ID register and is used in space management for the VRAM. (See A15 in 3-6-12.) However, since Bits 0 and 1 of the Control/ID register are only valid in Hercules mode, in CGA mode they could not be used. (Therefore, even though the PCDC evaluation board had 32K bytes of VRAM, only 16K bytes could be used in CGA mode.) A bit, GOE, has been established that can set GPE to 1 to make it easier to manage space in the VRAM.

3-6-4. Address 37H

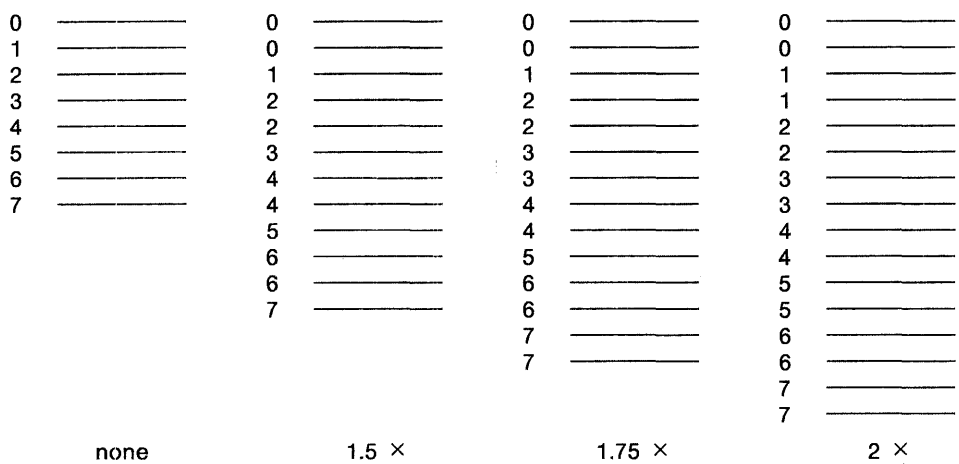
(Cleared by RESET)

TDS 1,0: Double Scan control (for Text Mode)

TDS 1	TDS 0	
0	0	none
0	1	1.5 X
1	0	1.75
1	1	2

(200 Line → 300
200 Line → 350
200 Line → 400)

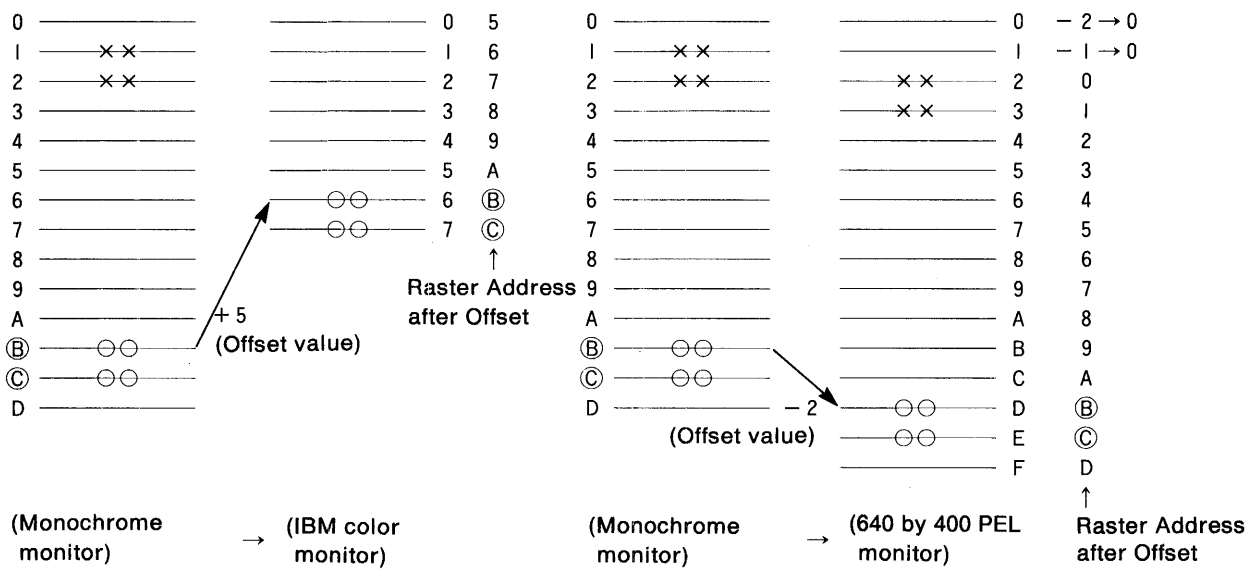
Software for CGA (requiring a 640 by 200 PEL display area) is based on a font with eight vertical PELs. In case this software will be run either with a monochrome or EGA monitor having 350 vertical display lines or with a display having a 640 by 400 PEL display area, two methods can be considered. One method involves preparing a separate font and setting the Maximum Raster Address to a value suitable for the monitor. The other method involves performing Double Scan control of the rasters and using the font for CGA. (A monochrome or EGA monitor employs a 1.75x Double Scan, whereas a display with a 640 by 400 PEL display area employs a 2x Double Scan.)
As shown below, Double Scan control repeats scanning of a Raster Address according to a given convention and is a method for increasing the total quantity of rasters. In case of 2x Double Scan, the same Raster Address is output two rasters at a time.



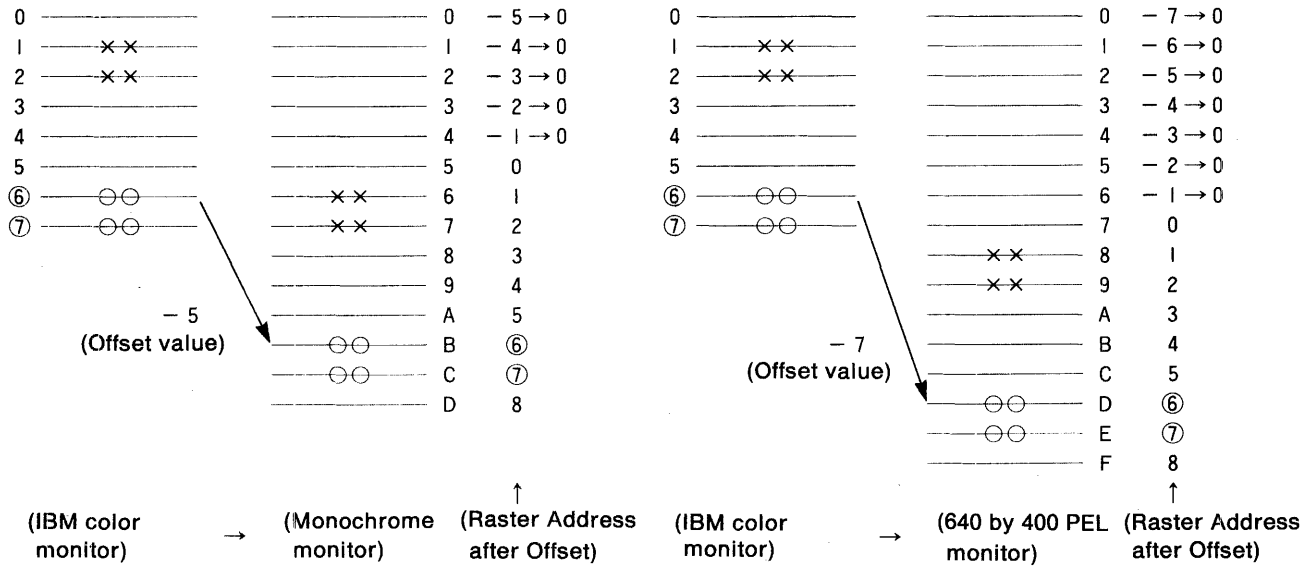
(The numerals on the left indicate the Raster Address and the bar indicates the raster.)
In case the total raster quantity is a multiple of four, the raster quantity will be increased according to the multiplying factor of the settings listed in the above figure. In other cases, however, the multiplying factor may differ from the setting. Because Double Scanning will be performed in two- line cycles even when the maximum raster quantity is two (regarding the maximum raster quantity as the equivalent of four), the raster quantity will be increased by the multiplying factor which conforms to the setting. Note that Double Scan control will affect neither the pulse width of Vertical Sync signals nor the Total Raster Adjust value.

(1) Cur. Offset: Sets the Offset value for the cursor

In case CGA software will be used with a monochrome monitor, display is possible by Double Scan control. In cases of using a separate font without relying on Double Scan control or of using MDA software with either an IBM color monitor or a Panel having a 640 by 200 PEL display area (Double Scan control is dedicated to expanded display and cannot be used for condensed display), the maximum raster quantity written by the software varies from the value suitable for the monitor. (Because the MDA software uses a 350-line display and the IBM color monitor uses a 200-line display, they each require a different number of rasters per character in order to display the same 25 characters.) Consequently, the cursor position must also be changed accordingly. For example, as shown below, the MDA software attempts to display the cursor at Raster Addresses BH and CH; with the IBM color monitor, however, the cursor must be displayed at Raster Addresses 6H and 7H. (For the IBM color monitor, the Raster Address per character only goes up to 7H.) In such a case, use Cur. Offset to shift the PCDC-internal Raster Addresses for the cursor by +5, thereby respectively converting Raster Addresses 0H to 7H into 5H to CH. This method thus allows the cursor to be displayed at Raster Addresses 6H and 7H.



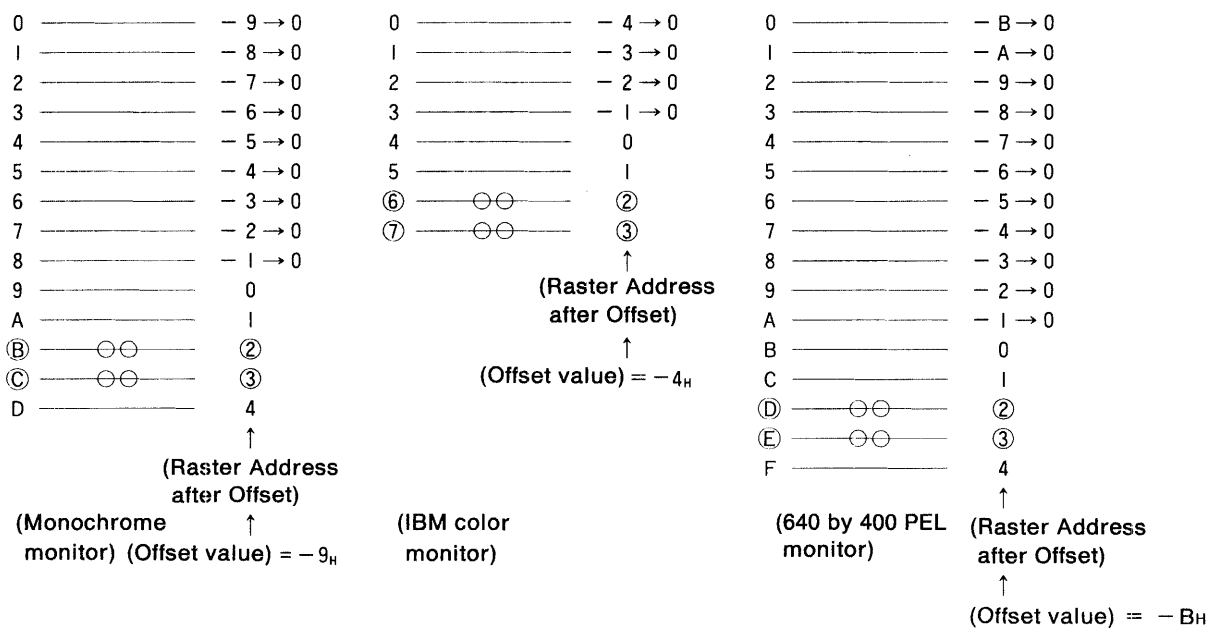
Although CGA software will attempt to display the cursor at Raster Addresses 6H and 7H, it must be displayed at Raster Addresses BH and CH in the case of a monochrome monitor. (If the cursor position is not offset, it will appear in the center of the character.) In this case, use Cur. Offset to shift the Raster Addresses for the cursor by −5, thereby respectively converting Raster Addresses 0H to DH into −5H to 8H. (A negative value resulting from underflow shall be corrected by "0H". In this case, therefore, the values will be converted into 0H to 8H.) This method thus allows the cursor to be displayed at Raster Addresses BH and CH.



Since the Offset value is expressed in two's complements, the range of its setting is from −16 to +15. In case an underflow occurs due to the offset, it shall be corrected to "0". If the Offset is unnecessary, write all '0' (the default status upon RESET).

(2) F/O: Selects the fixed cursor

If F/O = '0', similar to the description of Cur. Offset, the cursor position corresponding to the value set by the software is shifted to a value suitable for the monitor in use. In this case, no problem is posed by the usual set values of IBM PC (which are set so that the cursor is displayed at the bottom of the characters). If the cursor position is set to display the cursor at the top of the characters, however, the cursor will either be displayed at the center of the characters (represented by the "X" marked in the preceding figure), not be displayed at all, or be displayed at all rasters for one character. To prevent such display, the cursor position is fixed (the Raster Addresses that have been offset for the cursor are displayed at the 2H and 3H positions) and a mode has been provided which does not rely on setting the Cursor Start/End Registers by software. (This mode is assumed by setting F/O = '1'.)



3-6-5. Address 3FH

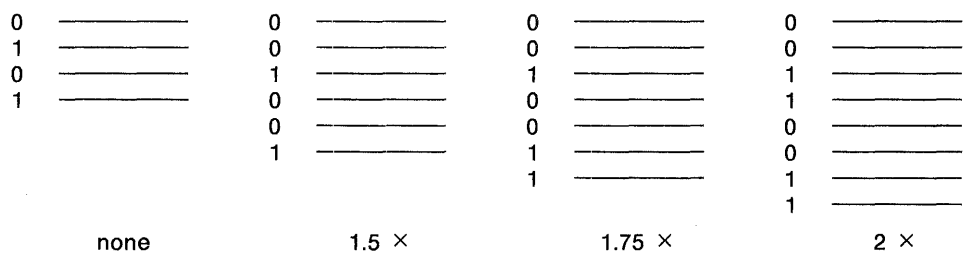
45S	GDS 1	GDS 0	UL.Position

0 0 0 0 1 1 0 0 ← Default values due to RESET

GDS 1	GDS 0	
0	0	none
0	1	1.5 X
1	0	1.75
1	1	2

(200 Line → 300
200 Line → 350
200 Line → 400)

This register performs Double Scan control similar to that of TDS1 and TDS0 of the preceding subsection 3-6-4, "Address 37H." GDS1 and GDS0 are used in Graphics Modes, whereas TDS1 and TDS0 are used in Text Modes. In case of CGA graphics software employing 640 by 200 PELs will be used with a monochrome monitor, 1.5x Double Scan is used. Similarly, 1.75x Double Scan is used with an EGA monitor, and 2x Double Scan is used with a Panel having a 640 by 400 PEL display area. (The monochrome monitor has 350 display lines in the vertical direction. With the CGA Graphics Mode which can only display 640 PELs of the horizontal 720-PEL display area, however, a 300-line display is recommended out of consideration for the aspect ratio.)
Though the maximum raster quantity for CGA graphics software is two, Double Scan is performed in two-line cycles (regarding the maximum raster quantity as the equivalent of four), so the raster quantity will be increased by the multiplying factor which conforms to the setting.



(The numeral on the left indicates the Raster Address, and the bar indicates the raster.)

(1) UL. Position: Controls the Underline position

When ULE = '1' in Text Mode, underlining equivalent to one raster will be displayed (In Double Scan Mode, a two-raster underline may be displayed according to the Raster Address) for characters that are specified to have a BLUE Foreground (the lower 3 Bits of Attribute is "001"). For specifying the position indicating the Raster Address to be displayed with underlining, however, UL. Position is used. For a monochrome monitor, the default underline position upon RESET becomes CH. Set the underline position to 7H for an IBM color monitor, or to EH for a display having a 640 by 400 PEL display area. If the set value is greater than the Maximum Raster Address, no underlining will be displayed.

(2) 45S: Enables the 6845 Expansion Functions

Writing to the MSB can be performed to the registers which set the vertical direction (Vertical Total Register (R4), Vertical Displayed Register (R6), and Vertical Sync Position Register (R7)) as well as to the MSB of their corresponding 6845 Preset Data (Vert. Total and Vsy. Offset) only when 45S = '1'. (When 45S = '0', '0' will be compulsorily written.) Because the written contents will be valid regardless of the 45S value, however, it is possible to set 45S = '1' at initialization, write the 6845 Preset Data, then later set 45S = '0' and execute the IBM PC software.
The pulse width of Vertical Sync signals becomes programmable according to the setting of the Sync Pulse Width Register (R3) and the settings of the higher four bits V3-V0 of its corresponding 6845 Preset Data (Sync. Width), but 45S = '0' will set a constant 16-raster width. Preset Mode constantly functions as if 45S = '1' (regardless of the actual 45S setting).

3-6-6. Address 20H (Duty)

This register sets the duty of a two-screen Panel (split into top and bottom halves). (The reciprocal of the duty value equals the number of lines per screen.) Duty is set in a similar manner for either a dual-drive type two-screen LCD which simultaneously transmits data of the top and bottom screens or a single-drive type two-screen LCD which alternately transmits one line each from the top and bottom screens. (This register need not be set for one-screen Panels, such as an EL, plasma display, etc.)
When the duty is set to "1/D", "D - 1" will be written to this register. For example, 63H will be written for 1/100 duty, and C7H will be written for 1/200 duty. The duty can be set in a 1/2 to 1/256 range. (The duty should be set so that the total raster quantity, determined by the vertical total and Maximum Raster Address, is larger than the duty.)

3-6-7. Address 21H (H size)

This register sets the quantity of PELs per line for the Panel. With a dual-drive type two-screen LCD, setting is performed in four-PEL units. For other Panels (one-screen Panels or single-drive type two-screen LCDs), setting is performed in eight-PEL units. When the quantity of PELs per line is set to "ND", the following values are written to this register:

For a dual-drive type two-screen LCD ("9FH" is written in case of 640 PELs)
$$\frac{ND}{4} - 1$$

For other Panels ("4FH" is written in case of 640 PELs)
$$\frac{ND}{8} - 1$$

For a dual-drive type two-screen LCD, the quantity of PELs per line can be set in a range of 4 to 1024 PELs (in four-PEL units); for other Panels, it can be set in a range of 8 to 2048 PELs (in eight-PEL units). (Set the value so that the total quantity of PELs, determined by the horizontal total, is larger than the quantity of PELs per line for the Panel.)

NOTE:

The PCDC requires horizontal/vertical return time for the panel. For details, refer to the setting examples in 10-3.

3-6-8. Address 22H (V Adj)

This register serves to correct the display positions in the vertical direction for the Panel, and specifies (in line units) the quantity of lines from the rising edge of VSY until the beginning of line display. This setting changes the FLM position for LCDs or the $\overline{VSY}$ position for ELs or plasma displays so that the display positions can be corrected without losing any characters at the top or bottom edges of the Panel. The correction value can be set in a range of 1 to 256 lines, but normal operation can be achieved only if the setting satisfies the conditions of the following equation:

$$NV + 1 + 2 \times D \leq N \times RN$$

Where:

- NV = The correction value at Address 22H (the value written to the register)
- D − 1 = The Duty value set at Address 20H (the value written to the register)
- N − 1 = The value written to the Vertical Total Register (and, in Preset Mode, its corresponding Vert. Total)
- RN − 1 = The value written to the Maximum Raster Address Register (and, in Preset Mode, its corresponding Max. Scan)

3-6-9. Address 23H (H Adj)

SCT	SCU	H Adj

(SCT and SCU are cleared by RESET)

This register serves to correct the display positions in the horizontal direction for the Panel, and specifies the quantity of PELs from the rising edge of $\overline{HSY}$ until the beginning of display. (In Text Mode, this value is set in units conforming to the number of horizontal PELs in the High Resolution Text font or in eight-PEL units for kanji display; in Graphics Mode, it is set in eight-PEL units.) This setting changes the LC position for LCDs or the $\overline{HSY}$ position for ELs or plasma displays so that the character positions can be correctly adjusted to the right and left edges of the Panel. The correction value can be set in a range of 8 to 512 PELs in case of 8-PEL setting units, but normal operation can be achieved only if the setting satisfies the conditions of the following equation:

$$2M - \frac{ND}{8} - \alpha \geq H + HA$$

Where:

- HA = The correction value at Address 23H (the value written to the register)
- ND = The quantity of PELs per Panel line at Address 21H
- M − 1 = The value written to the Horizontal Total Register (and, in Preset Mode, its corresponding Horiz. Total)
- H − 1 = The value written to the Horizontal Sync Position Register (and, in Preset Mode, its shifted by Hsy. Offset)
  (In Low Resolution Text or Graphics Mode, however, doubled M and H values shall be substituted into the above equation.)
- α = The integer "12" for dual-drive type two-screen LCDs or "9" for other Panels.
  (In Low Resolution Text or Graphics Mode, decrement the integer by 1.)

(1) SCT: Selects the timing for CPU-VRAM access

The PCDC uses separate timing with respect to VRAM for the display and the CPU, permitting the CPU to be accessed by VRAM at any time. Because the timing of the input of Read/Write instructions from the CPU and the timing assigned by the PCDC for the CPU are asynchronous, however, the PCDC employs the method of forcing the CPU to enter a Wait state by using MEMRDY. In recent years, the increased operating speed of CPUs has been accompanied by the problem of an long Wait time.
For this reason, PCDC provides its high-speed CPU with a timing that can minimize the average Wait time, and this high-speed timing can be used by setting SCT = '1'. (For details, see CHAPTER 5, "MEMORY.")

(2) SCU: Selects the cursor-blink cycle

Although the IBM PC uses a cursor-blink cycle that is fixed to 16 fields, the blinking may become hazy and hard to see in the case of LCDs with a slow display response rate. (The blinking will become hazy particularly when the field frequency has been set to a high value (70-80 Hz) to prevent flickering.) By setting SCU = '1' in such cases, the cursor will blink in 32-field cycles (ON : OFF ratio = 1 : 3), enabling the blinking to be easily distinguished. (Even when P = '0' for the Cursor Start Raster Register (R_{10}), the cursor will be blink in 32-field cycles. In other case, the functions will conform exactly to the table within subsection 3-1-12, "Cursor Start Raster Register.")

3-6-10. Address 24H

MON	ULE	GRM 2	GRM 1	GRM 0	FON 2	FON 1	FON 0

0	0	0	0	0	0	1	0	←	Default values due to RESET For CGA Mode (When the RA4 pin is '0' upon RESET)
1	1	1	0	0	0	1	1	←	Default values due to RESET For Hercules Mode (When the RA4 pin is '1' upon RESET)

(1) MON: Enables the monochrome display

With MDA, by performing the following conversion for a monochrome monitor that cannot perform color display, a monochrome display will be possible regardless of the values set for the Attribute data which specifies the text color.

Background R	Background G	Background B	Foreground R	Foreground G	Foreground B	Function	Text (Foreground) Color	Background color
0	0	0	0	0	0	Display OFF	Black	Black
1	1	1	0	0	0	Reverse	Black	White
Other combinations						Normal	White	Black

This conversion will be valid if MON = '1' regardless of being in CGA or Hercules Mode. Therefore, when executing CGA software not only with a monochrome monitor but also with a Panel, the text can be displayed in monochrome, providing an easily visible display. Note that the I (Intensity) bit of the Background and Foreground will function independently of this conversion.

(2) ULE: Enables the underline display

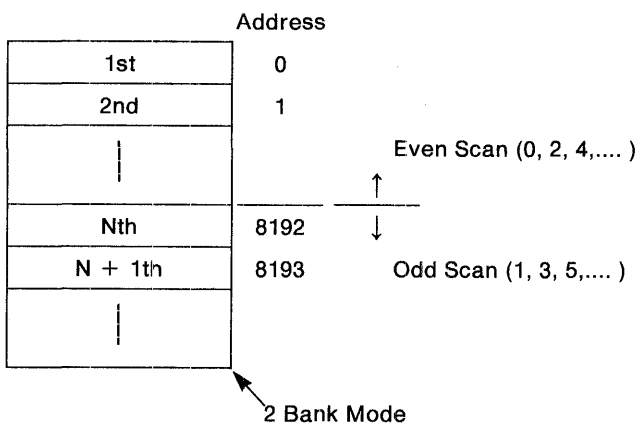
With MDA, an underline display is provided as one means for a monochrome monitor, that is capable of only monochrome display, to emphasize its text. When RGB = "001" in the Foreground of the Attribute data (that is, when the text (Foreground) color has been specified as BLUE), the rasters specified by UL. Position (described in Paragraph (1) of subsection 3-6-5, "Address 3FH") will be displayed as underlined. The setting of the UL. Position becomes valid when ULE = '1'. In case of setting MON = '0' and displaying the underlining, the Foreground color of BLUE which specifies underlining will not be displayed as is, but will be converted to Foreground RGB = "111" and displayed as WHITE. (The Intensity bit will operate independently of this conversion.)

GRM 1	GRM 0				
0	0	1 byte	640 x 1 bit,	320 x 2 bit	← IBM PC Standard Graphics Mode
0	1	2 byte	640 x 2	320 x 4	
1	0	4 byte	640 x 4	320 x 8	
1	1	1 byte		160 x 4	

The PCDC has numerous graphics functions besides the graphics functions standard to the CGA or Hercules Mode. (The PEL resolution will remain unchanged but the quantity of colors that can be simultaneously displayed will be increased.) GRM_1 and GRM_0 are used to select these graphics functions. In the two righthand columns of the above table, the numerals on the left signify the quantity of horizontal PELs displayed, and the numerals on the right signify the quantity of bits used per PEL for color specification. For 2 bits, 4 bits, and 8 bits, therefore, the quantity of colors that can be simultaneously displayed are, respectively, 4 colors, 16 colors, and 256 colors. Note that in order to use these expanded graphics functions, it is necessary to increase the VRAM capacity accordingly.

GRM2 = '0': 2 Bank Mode RA0 is used for bank switching (CGA Standard)
GRM2 = '1': 4 Bank Mode RA1 and RA0 are used for bank switching (Hercules Standard)

Since the setting range of 6845 in the vertical direction is a maximum of 127 (seven bits), IBM PC performs bank switching according to the Raster Address in order to cope with the 200 lines for CGA Mode and the 348 lines for Hercules Mode. In CGA Mode, the odd and even lines are divided into two groups, and each is entered into a bank containing different Display Data (the 2 Bank Mode).



In Hercules Mode, the data of Lines 0, 4, 8, ... is placed in the first 8K bytes, the data of Lines 1, 5, 9, ... is placed in the next 8K bytes, the data of Lines 2, 6, 10, ... is placed in the next 8K bytes, and the data of Lines 3, 7, 11, ... is placed in the last 8K bytes (4 Bank Mode).

FON 2	1	0	Font Size (horizontal)	
0	0	0	6 Dot	Either HRES and LRES is possible (Double Dots for LRES)
0	0	1	7	
0	1	0	8	
0	1	1	9	
1	0	0	10	
1	0	1	8 x N Kanji (Chinese character)	N is an integer
1	1	0	16 x N Kanji (")	← Only in LRES (but no Double Dots are possible)

The quantity of horizontal PELs in the character font for Text Mode can be selected. Although either 6-10 PELs or an integer multiple of eight can be used to select either the High Resolution or Low Resolution Mode by setting Bit 0 of the Mode Register, if an integer multiple of 16 is used, set Bit 0 of the Mode Register to '0'.

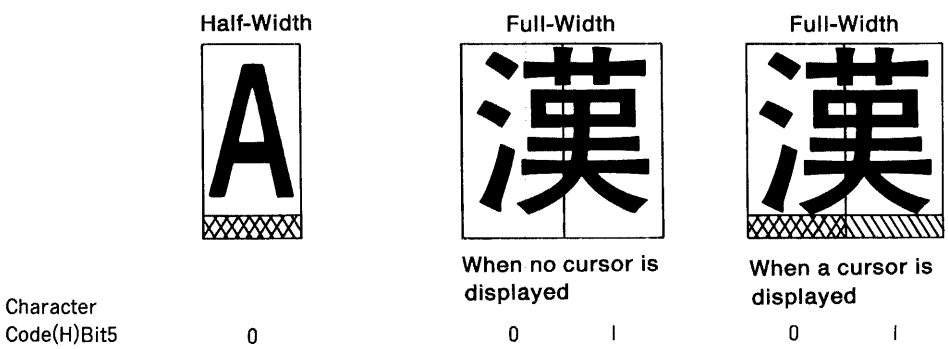
Setting an integer multiple of 8 or 16 enables a kanji display that combines half- and full-width characters. (In this case, a Character Code is required for each 8 or 16 PELs.) In case of a combined display of 8-PEL half-width characters and 16-PEL full-width characters, the characters are processed in 8-PEL units (by splitting each 16-PEL full-width character into two 8-PEL units: left and right). For a 24-PEL kanji display as well, the characters are processed in eight-PEL units (Each 24-PEL kanji is split into three 8-PEL units: left, center, and right. A large number of kanji ROMs having this configuration are commercially available.), a Character Code is also required for each 8-PEL unit. Because a 12-bit Character Code is required to select the Level No. 1 Kanji, and an additional two bits are required to support the half- and full-width characters and the Level No. 2 Kanji, two bytes will be required for the Character Code alone. Consequently, the basic procedure for kanji is to set GRM0 = '1' and use four-byte units.

0	Character Code (L)
1	Character Code (H)
2	Not used
3	Attribute (can provided all attribute functions)

NOTE:

In case of non-kanji display (for horizontal font sizes of 6-10), GRM0 = '0' must always be set.

When processing characters in 8-PEL units, as in the case of supporting half- and full-width characters or 24-PEL kanji, the addresses will also be processed in 8-PEL units, so the cursor will basically assume an 8-PEL width. When Bit 5 of Character Code (H) is set to '1', however, the left side of the cursor will be copied for display, enabling the cursor to be properly displayed in character units. (This Bit 5 can also function to support half- and full-width characters. That is, Bit 5 = '0' signifies the half-width characters and the left side of full-width characters, while Bit 5 = '1' signifies the right side of full-width characters.)



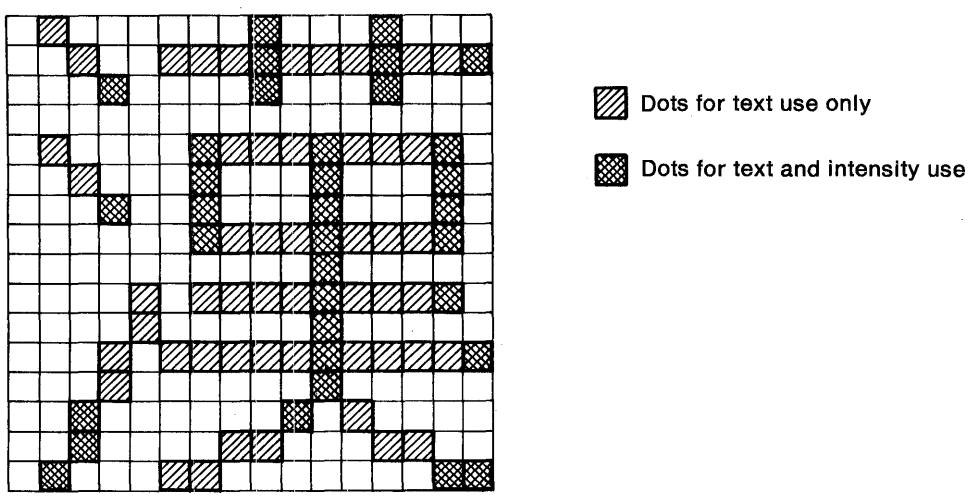
Represents the cursor displayed according to the Cursor Address Register.
Indicates the status wherein the left side of the cursor has been copied and displayed, according to Bit 5 of Character Code (H).

Since the top two bits of Character Code (H) are not used, GRM0 can be set to '0' for display in two-byte units. In such case, however, the Attribute functions will be extremely simplified. (Note that MON should be set to '1' at this time.)

Functions of the upper bits of Character Code (H)

0	Character Code (L)	D7: Cursor blinking
1	Character Code (H)	D6: Reverse/Normal selection
	+ simple Attributes	D5: Cursor continuation

When D6 = '1', the effect is identical to Reverse described in subsection 3-6-10, "Address 24H," providing a black text (foreground) and a white background. D6 = '0' provides a white text (foreground) and a black background. D5 is identical to the case of four-byte units when GRM0 = '1'.
When Bit 5 of the Mode Register is '1', the text set to D7 = '1' will blink in 32-field cycles. Bit 5 of the Mode Register is '0', D7 becomes the Intensity bit of the Background attribute. (The Intensity bit of the Foreground is fixed to '0'.)
When GRM1 = '1', the Intensity bit of the Foreground can be externally controlled in PEL units (but only when the quantity of horizontal PELs in the character font is 6-8 or an integer multiple of 8). One pair of Font ROM shall be prepared for text use and intensity use, the text data shall be connected to RD0-RD7, and the intensity data shall also be connected to RD8-RD15. (See CHAPTER 6, "MONITOR INTERFACES," regarding the connection between the ROM's peripheral circuitry and PCDC.) Intensity can thus be controlled for each PEL of the text, so the characters can be clearly displayed even with a small quantity of PELs. (Particularly in the case of kanji, a 16 by 16 PEL configuration can be displayed to equal a 24 by 24 PEL configuration.)



Sample kanji display using intensity data

NOTE:

In cases where the quantity of horizontal PELs in the character font is 6 or 7, where GRM1 and GRM0 are set to "10" (4 Byte Mode), or where kanji is being processed in four-byte units (GRM0 = '1'), attention is required because the upper limit of the master clock frequency will become 16.35 Mhz. (These functions can be actualized only when the VRAM data bus has a 16-bit configuration.) In the case of other functions, the master clock's upper limit will be 22.5 Mhz. When the VRAM data bus has an eight-bit configuration, the master clock's upper limit will be 16.35 Mhz.

3-6-11. Address 25H

SYTH	HERC	SRAM	8BUS	16CP	BINH	CLK 1	CLK 0

0 0 0 0 0 ← Defaults due to RESET (CGA Mode) (When RA4 pin = '0' upon RESET)

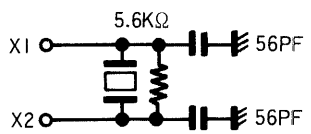
1 0 1 0 0 ← Defaults due to RESET (Hercules Mode) (When RA4 pin = '1' upon RESET)

Determined by status of $\overline{LSW}$ pin upon RESET

Determined by status of $\overline{LDT}$ pin upon RESET

Determined by status of RA4 pin upon RESET

CLK 1	CLK 0	
0	0	Input from X1 pin is used as clock (Default upon RESET)
0	1	Input from X2 pin is used as clock
1	×	X'tal oscillates when externally mounted (X1: input pin; X2: output pin)



When CLK1 = '0', PCDC operates according to clock input from an external source. Clock input can selected from either the X1 pin or X2 pin, which is very convenient in cases such as switching between two monitor types (two frequency types) for operation. For example, input 14.318 Mhz for the IBM color monitor into the X1 pin, input 16.257 MHz for a monochrome monitor into the X2 pin, then use them by switching according to CLK0. When CLK1 = '1', the external mounting of X'tal forms a self-excited oscillator circuit so that clock input from an external sources becomes unnecessary.

(1) BINH: Inhibits border display

With CGA software, the border is displayed in color during Text or Low Resolution Graphics Mode. With a monochrome monitor or EGA monitor, however, a looped scan line will appear in the border for an undesirable display. When BINH is set to '1' in such a case, black will always be displayed as the border, eliminating the appearance of the looped scan line for an easy-to-see screen.

(2) 16CP: Selects the 16-bit CPU

16CP = '1' enables a 16-bit bus CPU to be connected (and 16CP = '0' enables an 8-bit bus CPU to be connected). When the A0 pin is '0', the CPU can perform reading and writing using the lower-order RD7-RD0 (the even address bytes) of the VRAM data bus via PCDC. The higher-order RD15-RD8 (the

odd address bytes) of the VRAM data bus is connected with the CPU via an external circuit. (See CHAPTER 7, "SYSTEM CONFIGURATIONS.")

(3) 8Bus: Selects the VRAM data bus configuration

An 8- or 16-bit configuration can be selected for the VRAM's data bus. (8Bus = '1' selects the 8-bit configuration.) Initialization can be performed according to the status of the $\overline{LSW}$ pin upon RESET without relying on software. (That is, when the $\overline{LSW}$ pin is '1' upon RESET, the 8-bit configuration is selected; when it is '0', the 16-bit configuration is selected.)
In case of the 16-bit configuration, the data of the even addresses (A_0 pin = '0') is stored in a VRAM which has been connected to RD_7-RD_0. (In Text Mode, the data of the Character Codes are stored.) The data of the odd addresses (A_0 pin = '1') is stored in a VRAM which has been connected to RD_{15}-RD_8.
In case of the 8-bit configuration, all data is stored in a VRAM which has been connected to RD_7-RD_0.
The following table describes the valid status of the higher- or lower-order bits of the VRAM data bus according to the bus configuration of VRAM and CPU. The data bus which is not valid during writing will assume high-impedance status.

CPU	VRAM Bus Configuration	A_0 = '0'		A_0 = '1'	
		Read	write	Read	write
8-bit bus CPU	8-bit bus configuration	$RD_{7\sim0}$	$RD_{7\sim0}$	$RD_{7\sim0}$	$RD_{7\sim0}$
	16-bit bus configuration	$RD_{7\sim0}$	$RD_{7\sim0}$	$RD_{15\sim8}$	$RD_{15\sim8}$
16-bit bus CPU	16-bit bus configuration	$RD_{7\sim0}$	$RD_{7\sim0}$	$RD_{7\sim0}$	High Impedance

(4) SRAM: Selects the VRAM type

When SRAM = '1', an SRAM can be used for the VRAM (and when SRAM = '0', a DRAM can be used). Initialization can be performed according to the status of the $\overline{LDT}$ pin upon RESET without relying on software. (That is, when the $\overline{LDT}$ pin is '1' upon RESET, SRAM is selected; when it is '0', DRAM is selected.)

(5) HERC: Controls switching between CGA software and Hercules software (including MDA software)

HERC = '1' enables handling of Hercules software. Initialization can also be performed according to the status of the RA4 pin upon RESET without relying on software. (That is, when the RA4 pin is '1' upon RESET, Hercules software can be processed; when it is '0', CGA software can be processed.)
With PCDC, the main differences between the handling of CGA and Hercules software is as follows:

(a) A different I/O register is used to set the Light Pen flip-flop

(b) Different functions for Bits 0, 3, and 7 of the Status Register

(c) For Hercules software, the Color Register is disabled (Bits 3-0 are fixed to 7H)

(d) For Hercules software, Bits 0, 2, 4 of the Mode Register are fixed to '1'

(e) Bit 7 of the Mode Register and Bits 0 and 1 of the Control/ID Register are valid only for Hercules software (these bits are fixed to '0' in CGA software)

(f) Due to a different VRAM capacity being required for display, addresses corresponding to that capacity are output (Unused address bits will output '0')

	Text Mode	Graphics Mode
HERC = '1' (Hercules Mode)	4K bytes	32K bytes
HERC = '0' (CGA Mode)	16K bytes	16K bytes

(6) SYTH: Selects the pulse width of Horizontal/Vertical Sync signals and the polarity of Vertical Sync signals

It is possible to select whether to output the width of the Sync signals in exact accordance with the set value written to the Sync Pulse Width Register (R_3 or, in Preset Mode, its corresponding Sync. Width) or to output a narrowed width. (SYTH = '1' selects an output conforming to the set value). The polarity of the VSY pin can also be selected at the same time (SYTH = '1' selects a negative output). Consequently, use SYTH = '1' with an EGA or monochrome monitor, and use SYTH = '0' with an IBM color monitor. (With a Panel, the SYTH polarity may be set to negative or positive.)
CGA software in Low Resolution Text Mode enables setting of Horizontal Sync signals to a 10-character width and of Vertical Sync signals to a 16-line width. When SYTH = '0', however, these signals will be respectively narrowed to a 4-character width and a 3-line width for output (because the width and timing are converted to match the standard of Composite signals for NTSC). When the respectively set widths of Horizontal Sync signals and Vertical Sync signals are narrower than these 4-character and 3-line widths, the widths will not be further narrowed despite an SYTH = '0' setting, and will be output as is. Note that the Sync signals for blanks or status purposes will employ their set widths even when SYTH = '0'.

3-6-12. Address 26H

(Cleared by RESET)

(1) RA_4: Selects the I/O status of the RA_4 pin

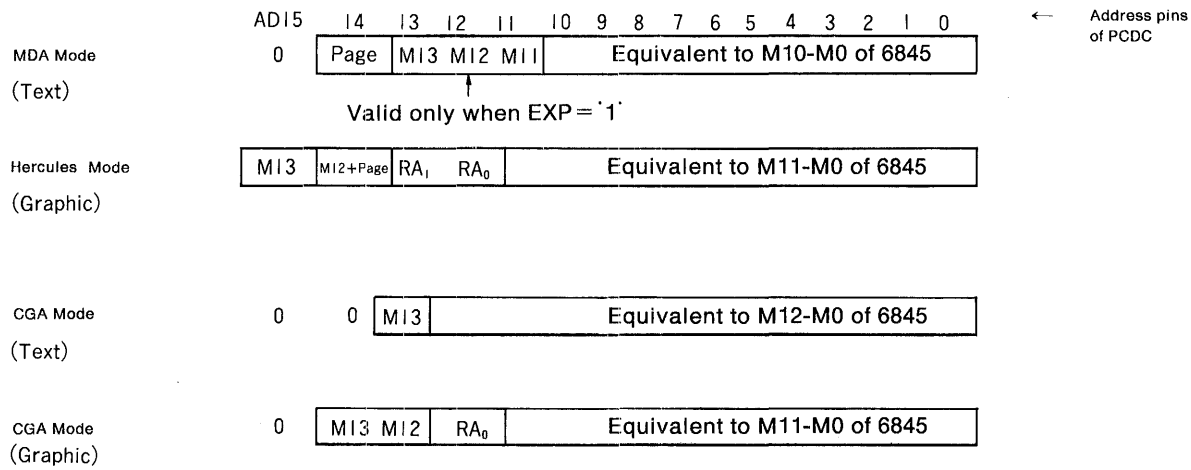
Set RA_4 = '1' when you wish to output the Raster Address RA_4 or the AC Conversion signal M from the RA_4 pin. The default status during and after RESET will be RA_4 = '0' so that the RA_4 pin will become an input pin. Consequently, the CGA or Hercules Mode can be selected according to the input level to the RA_4 pin at RESET. (When the input level is '1', the Hercules Mode is selected.)

(2) A_{15}: Selects the function of the AD_{15} pin

When A_{15} = '1', the AD_{15} pin becomes an Address pin for VRAM (valid only in SRAM Mode). When A_{15} = '0', the AD_{15} pin outputs the ORed result (GPE) of the output of Bits 0 and 1 of the Control/ID Register. GPE is used in Hercules Mode and is employed to specify (by an external circuit) the 4K bytes to be used in Text Mode from among the 32K bytes of the VRAM area. Normally, the addresses A_{12}-A_{14} above the 4K bytes are ANDed by GPE (see CHAPTER 7, "SYSTEM CONFIGURATIONS") for use.

(3) EXP: Selects the Address Expansion Mode

When EXP = '1', the Address Expansion Mode is assumed. When EXP = '0', the IBM PC Compatible Mode is assumed. There is a 14-bit address output to 6845. With IBM PC, however, only 11 bits and 13 bits are respectively used for MDA and CGA, but the higher-order addresses are not used. When EXP is set to '1', these unused high-order addresses are output to the higher-order empty addresses. (When EXP = '0', '0' are output.)



M11-M13, which are enclosed in boxes within the above figure, are valid only when EXP = '1'. Page is the output for Bit 7 of the Mode Register. (Page is valid only in Hercules Mode. Unless '1' has been written to Bit 1 of the Control/ID Register, writing to Page is impossible. In CGA Mode, Page is always '0'.)

RA0 and RA1 are the lowest two bits of the Raster Address. The above figure depicts address output in case both an SRAM is used for the VRAM and the VRAM's data bus has a 16-bit configuration.

The preceding figure used the IBM PC (1 Byte Mode) as reference, but the 2 Byte and 4 Byte Modes - which are expanded Graphics Modes - are formed by respectively shifting the contents of the preceding figure to the left by one and two bits. (Any bits exceeding the left edge are ignored. The address used for byte selection is input to the lower-order bits.)

PB 1	PB 0	
0	0	No Page Mode
0	1	1 Bit Page Mode (AD15 = PAG2)
1	0	2 Bit Page Mode (AD15 = PAG2, AD14 = PAG1)
1	1	3 Bit Page Mode (AD15 = PAG2, AD14 = PAG1, AD13 = PAG0)

(4) PAG2-PAG0: Specifies the page

Regardless of EXP, 2 Byte or 4 Byte Mode, etc., if there is any vacant area (the status from which '0' is usually output) in the higher-order bits of the address that is to be ultimately output, the Page Mode can be used. According to the status of the unused bits, selection can be made from the 1 Bit Page Mode (in case of only an empty MSB) up to the 3 Bit Page Mode (in case of three highest-order empty bits), according to the need. Since a fixed value determined by PAG2-PAG0 will be output in Page Mode, a specific page can be displayed out of a large VRAM area.

3-6-13. Address 27H

(Cleared by RESET)

I.S 1	I.S 0	
0	0	1 Bit Serial
0	1	2 Bit Even/Odd
1	0	4 Bit Parallel
1	1	8 Bit Parallel

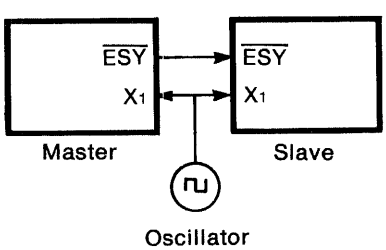
Selects the quantity of bits for data transmission to the Panel. (Be sure to set the display to Gray Scaling/Hatching in case of using the Panel.) This bit quantity corresponds to one sequence, and also applies to the double-sequence required when performing simultaneous two-screen output to a dual-drive type two-screen LCD, when using Intensity output according to IEN (Intensity Enable), or other such cases. (Since the ultimate output consists of eight bits, however, an 8-bit parallel format cannot be used in case of a double-sequence transmission.) In case of using Gray Scaling/Hatching with an IBM Monochrome monitor, select "1 Bit Serial" (which also permits Intensity output by IEN to be used).

(1) IEN: Enables Intensity output to the Panel

In Gray Scaling/Hatching Mode, colors can be converted by gray scaling/hatching patterns for display. In consideration of a display which has Intensity input, such as the IBM monochrome monitor or a Panel capable of displaying four half-tone, however, it is also possible to output an addition Intensity sequence besides the usual output (when IEN = '1'). Intensity is determined by R2 of the Color Palette, and the data the Intensity ON/OFF status according to color is written into the Color Palette. Note that IEN cannot be used with a dual-drive type two-screen Panel (Dual Drive type) (because double sequences are already being used by its two-screen drive).

(2) EXTS: Specifies the External Sync Mode

When EXTS = '1', the External Sync Mode is assumed, but external synchronization is valid only in Non-Interlace Mode. Synchronization is achieved between two chips according to the $\overline{ESY}$ pin.



Set EXTS = '1', then set the master side to ESIO = '1' (the $\overline{ESY}$ pin becomes an output pin) and set the slave side to ESIO = '0' (the $\overline{ESY}$ pin becomes an input pin). Since this procedure will synchronize two chips, one chip can be assigned to Text display and the other to Graphics display for a combined superimposed display (superimposing is performed by an external circuit).

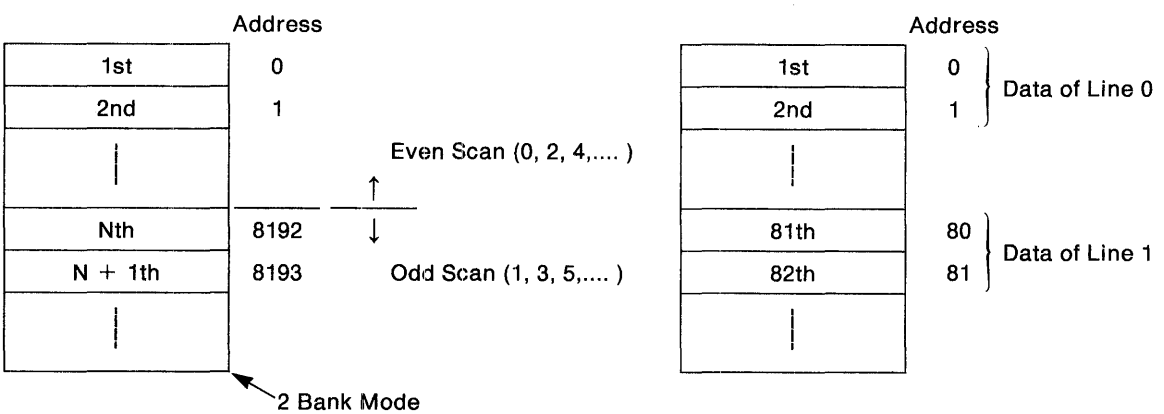
(3) IINH: Inhibits the OFF status of Enable Video in High Resolution Text Mode

In the High Resolution Text Mode of IBM PC, rewriting of the screen data is achieved by setting Bit 3 (Enable Video) of the Mode Register to '0' (Display OFF) with respect to the scrolling required for rewriting the screen data. Because no time is allotted for the CPU during the display time of the IBM PC, the display must be switched OFF to avoid screen disturbance; however, the phenomenon

of a flashing screen will occur which leads to poor visibility. Since the PCDC allots time for the CPU during its display time, enabling reading and writing to be performed at any time with respect to VRAM without screen disturbance, there is no need to take the trouble to switch OFF the display to write the screen data. When IINH is set to '1', the Display OFF status for rewriting screen data will be ignored in only the High Resolution Text Mode (for a constant Display ON status) and the screen will not flash, thus providing an easily visible screen (by following the Display OFF status upon mode switching).

(4) ACM: Selects the Consecutive Addressing Mode during Graphics Mode

As previously touched upon in subsection 3-6-10, "Address 24H," the IBM PC performs bank switching in order to implement a 200-line or 348-line Graphics display with respect to the maximum vertical-direction setting of "127" for 6845. For example, since CGA stores the respective data for even and odd lines in separate banks, bank switching must be considered for each line in case of writing the vertical, and diagonal vector data as screen data to VRAM. When ACM is set to '1', the screen data can be stored in consecutive addresses without requiring bank switching, thereby simplifying the considerations required when, for example, creating new software.



When ACM = '0' (Data is stored in a different bank according to the even/odd status of the Line No.)

When ACM = '1' (Data is sequentially stored from the top line to the bottom line)

(5) CPLE: Enables the Color Palette

Set CPLE = '1' when the Color Palette will be used. When the Color Palette will be used either as a Color Lookup Table with respect to a linear RGB, EGA or CGA monitor, or as a Conversion Table in Gray Scaling/Hatching Mode for converting a color display into half-tone and hatching patterns, set CPLE = '1'. When CPLE is set to '0' for a CGA monitor, the Color Palette will be disabled and the PEL color data IRGB will be directly output as is. In case of the 320 x 8 bit (simultaneous display of 256 colors) Graphics Mode, the Color Palette cannot be used so set CPLE to '1'.

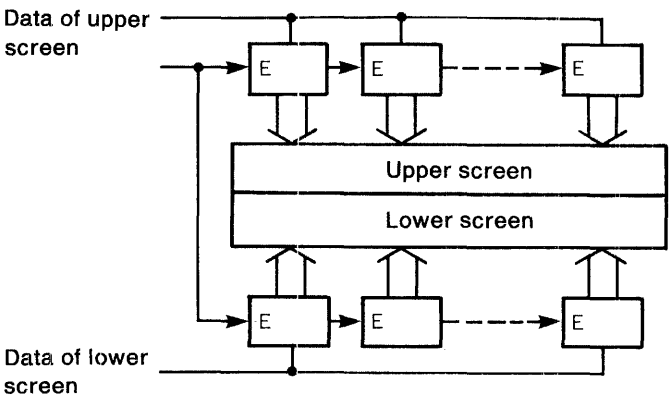
(6) PRE: Enables the Preset Mode

When the 6845 Preset Data described in subsection 3-6-3, "6845 Preset Data," will be used, set PRE = '1' to enable the Preset Mode. In Preset Mode, the 6845 Preset Data will enable the software and monitor to operate properly, even if they do not conform to IBM PC standards. When PRE = '0', the 6845 Registers will be used.

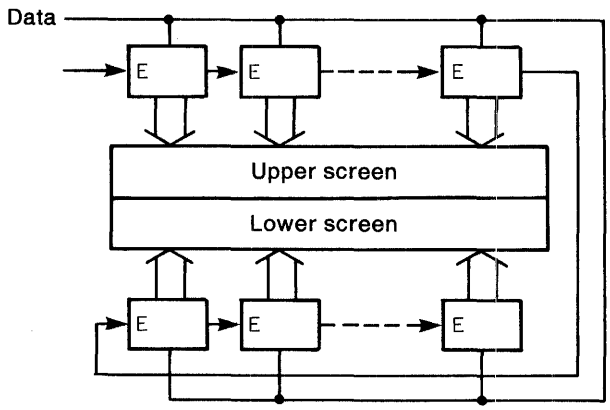
3-6-14. Address 28H

(Cleared by RESET)

2SCR 1	2SCR 0		
0	0	No Gray Scaling/Hatching	
0	1	One-screen Panel (EL, plasma display, etc.)	Gray Scaling/Hatching Mode
1	0	Dual-drive type two-screen LCD	
1	1	Single-drive type two-screen LCD	



Dual-Drive Type Two-Screen LCD
(Simultaneous transmission of data for upper/lower screens)



Single-Drive Type Two-Screen LCD
(Alternate transmission of data for one line each of the top and bottom screens)

With a Panel, a color display will be converted into gray scaling or hatching patterns for display in Gray Scaling/Hatching Mode. (The color correspondence for conversion is performed by the Color Palette.) In case of performing a gray scaling/hatching display with an IBM Monochrome monitor, perform setting for a one-screen panel. With a linear RGB, CGA, EGA or monochrome monitor, set 2SCR to "00" so that the Gray Scaling/Hatching Mode will not be assumed.

(1) R/M: Selects the function for RA4-pin output

The R/M determines whether the RA4 pin will output Raster Address RA4 or the AC Conversion signal M for an LCD. (R/M = '1' selects output of the AC Conversion signal M.) Take special note that unless RA4 (described in Paragraph (1) of subsection 3-6-12, "Address 26H") has been set to '1' at this time, the RA4 pin will not function as an output terminal.

(2) H/E: Selects the function of the HSY pin

The H/E determines whether the HSY pin will output the Horizontal Sync signal HSY for a CRT or the Enable Clock signal ECK for an LCD driver. (H/E = '1' selects output of the Enable Clock signal ECK.) Although numerous drivers can be used with the LCD Panel, there has been an increasing number of cases wherein a driver provided with a Chip Select function is used for reduced power dissipation. (Reduced power dissipation is achieved by enabling the driver is enabled only during data transmission, then sending the Enable signal to the next driver upon receiving the data, so that

only one of multiple drivers is enabled at any time.) ECK is used in the transmission of this Enable signal and its cycle is set by EH_4-EH_0.

(3) SSCK: Selects the output time of Shift Clock SCK

The SSCK determines whether the Shift Clock SCK for data transmission is constantly output or output only during the horizontal display time. (SSCK = '1' selects constant output.) In general, constant output (SSCK = '1') is used for ELs, and output only during horizontal display time (SSCK = '0') is used for other Panels. (Select the appropriate output time according to the Panel specifications.)

(4) SSY: Selects the polarity of the Sync signals for Panel use

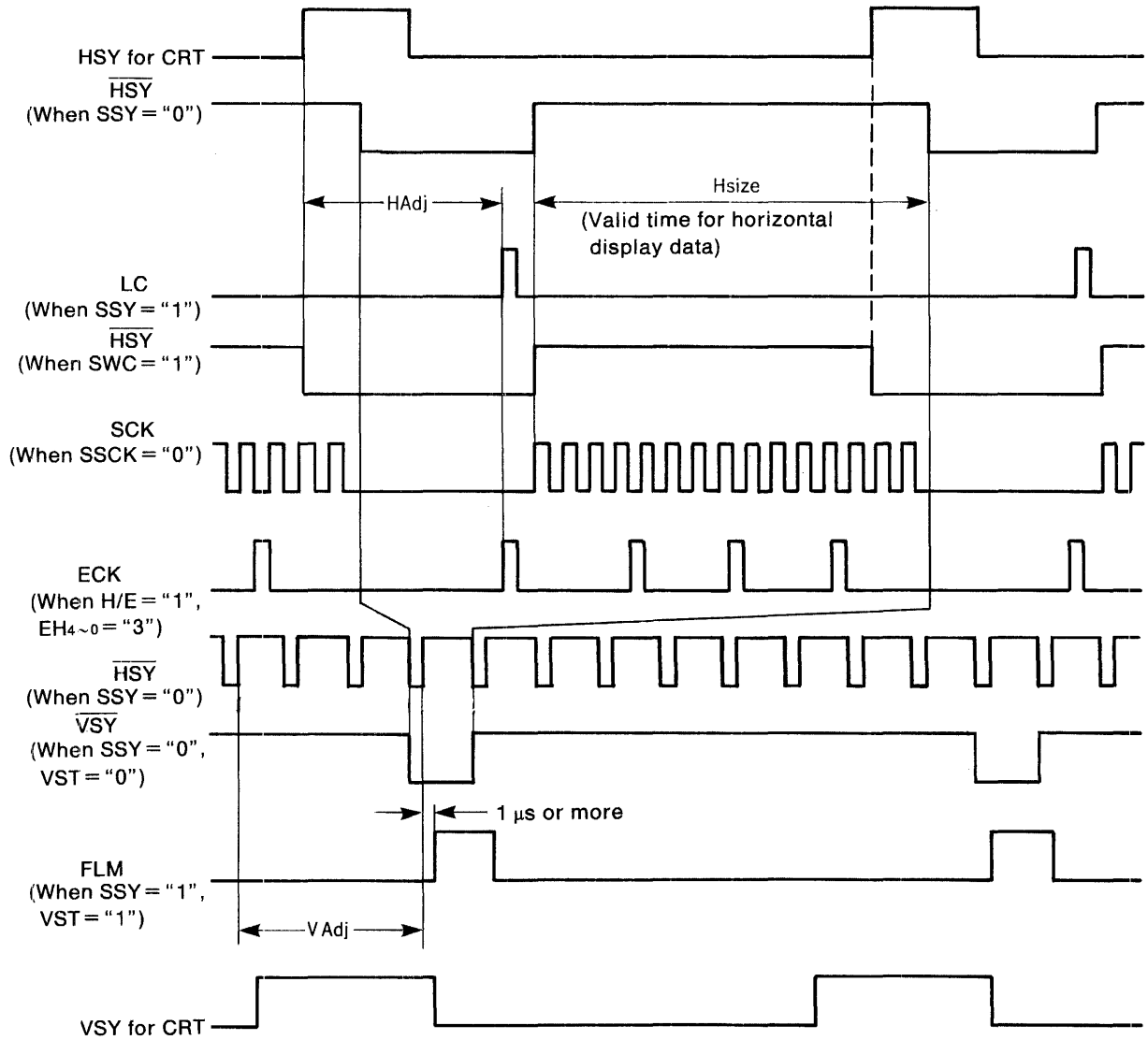
The SSY selects the polarity of $\overline{HSY}$ and $\overline{VSY}$ for Panel use. SSY = '1' selects output of positive polarity so that the Data Latch signal LC for LCDs as well as the Scan Start signal FLM are output. SSY = '0' selects output of negative polarity, so that the Horizontal Sync signal $\overline{HSY}$ and Vertical Sync signal $\overline{VSY}$ (for ELs or plasma displays) are output. (The Horizontal Sync signal $\overline{HSY}$ is identical to the valid time for horizontal display data. The Latch Clock signal LC for LCDs is output at a fixed width upon the start of display data. The Vertical Sync signal $\overline{VSY}$ and the FLM signal for LCDs are output at a width corresponding to the interval of one horizontal scan.

(5) VST: Selects the $\overline{VSY}$ output timing for Panel use

The VST determines whether the $\overline{VSY}$ output for Panel use will be synchronized with the falling edge of $\overline{HSY}$ or approximately 1 microseconds after the rising edge of $\overline{HSY}$ (or the falling edge of LC for LCDs). (VST = '0' selects synchronization with the falling edge of $\overline{HSY}$.) In general, synchronization with the falling edge of $\overline{HSY}$ (VST = '0') is used for ELs, and VST = '1' is used for LCDs and plasma displays. (Select the appropriate method of synchronization according to the Panel specifications.)

(6) SWC: Controls the $\overline{HSY}$ output width for the Panel

Set SWC to '1' for a high-level $\overline{HSY}$ width for Panel use that is narrower than the valid time for horizontal display data. Because the Horizontal Sync signals for CRTs will narrow the high-level $\overline{HSY}$ width for Panel use, set the horizontal sync position and sync pulse width to conform to applicable specifications. Note that when SSCK = '0' so that the Shift Clock SCK is output only during the horizontal display time, the width prior to narrowing will be used, so the quantity of pulses conforming to the Hsize setting will be output.
When a linear RGB monitor will be used, set CPLE to '1' and also set SWC to '1' (thereby causing all nine bits of the Color Palette to be output from PCDC). If only CPLE is set to '1', the two bits R2 and R1 will not be output. For the 320 x 8 bit (simultaneous display of 256 colors) Graphics Mode as well, set CPLE = '1' and SWC = '1'.) The timing of the signals described in the preceding paragraphs is shown in the following figure.


HSY for CRT
$\overline{\text{HSY}}$
(When SSY = "0")
HAdj
Hsize
(Valid time for horizontal
display data)
LC
(When SSY = "1")
$\overline{\text{HSY}}$
(When SWC = "1")
SCK
(When SSCK = "0")
ECK
(When H/E = "1",
EH4~0 = "3")
$\overline{\text{HSY}}$
(When SSY = "0")
$\overline{\text{VSY}}$
(When SSY = "0",
VST = "0")
1 μs or more
FLM
(When SSY = "1",
VST = "1")
V Adj
VSY for CRT

3-6-15. Address 29H

(Cleared by RESET)

(1) EH4-EH0: Sets the ECK synchronization

The EH4-EH0 sets the cycle of the Enable Clock signal ECK for LCD drivers. The first ECK signal is output during the first half of the LC signal, then one pulse is later output each time the Shift Clock SCK is counted as being a plus-one increment of the value set at EH4-EH0 (see the preceding figure). For example, for outputting ECK every 20 SCK signals, set EH4-EH0 to "10011". Note that the cycle setting of the Enable Clock signal ECK is valid only when H/E = '1'. When H/E = '0', set all '0' to EH4-EH0.

When a CRT is used, the Internal Clock signals preceding the rising edge of HSY can be stopped for an period equivalent to the set Clock No. of EH4-EH0 in order to change the phase of the Color Burst Clock signal for Composite use according to each line. (Special attention is required in this case, because the horizontal scan cycle will be lengthened for a period equivalent to the stopping of the Internal Clock signals.)

EH_1	EH_0	
0	0	No Improvement
0	1	1 Clock
1	0	2 Clock
1	1	3 Clock

(During the Master Clock signals of these numbers, the Internal Clock signals will stop just before HSY)

When the Master Clock is 14.318 MHz, Clock 1 will result in a 90-degree phase deviation, Clock 2 will result in a 180-degree phase deviation per line, and Clock 3 will result in a 270-degree phase deviation per line. Although the the displayed pattern, the color deviation phenomenon characteristic of Composite signals will disappear depending on the phase deviation between lines. On the other hand, according to the displayed pattern, the boundaries of the pattern may flow in the vertical directions or a conspicuous color deviation may occur in some cases. (The flicker similar to the Interlace Mode may occur).

(2) ESIO: Selects the I/O status of the $\overline{\text{ESY}}$ pin

When ESIO = '1', the $\overline{\text{ESY}}$ pin becomes an output pin. Via the combined setting of ESIO and EXTS, the $\overline{\text{ESY}}$ pin will function as follows:

EXTS	ESIO	
0	0	9Font input
0	1	PEN output
1	0	External sync (Slave side)
1	1	External sync (Master side)

(a) 9Font Input: Although MDA or HGC for IBM PC uses a 9 by 14 PEL font, certain Character Codes create the 9th PEL by copying the 8th PEL. (The other Character Codes set the 9th PEL to data '0'.) While Font Size 9 is selected, setting the $\overline{\text{ESY}}$ pin to '0' causes the 9th PEL to become a copy of the 8th PEL, and setting it to '1' causes the 9th PEL to become '0'. Therefore, by merely decoding the Character Code you wish to copy and inputting the result to the $\overline{\text{ESY}}$ pin, an MDA-equivalent display can be easily achieved.

(b) PEN Output: This function outputs Bit 1 of the Control/ID Register. It is the Page Enable signal for FULL Hercules Mode, and is employed when the use of all 64K bytes of VRAM is desirable. With Hercules Graphics software, 32K bytes of VRAM will be required per screen. (The IBM PC memory map uses Addresses B0000-B7FFF, whereas that for CGA uses Addresses B8000-BFFFF.) When using Page Mode for full use of a 64K byte VRAM, however, it is necessary to convert the decode values of the memory map in order to also cover the CGA area. PEN Output is the switching signal used for this conversion. (The decode values are switched by an external circuit.)

(3) RREG: Enables reading of I/O Registers 8, 9, and F

In case of executing multiple software programs in parallel, if the current status can be memorized (particularly the contents of the Mode Register) when interrupting one program and shifting to another task, the restarting of the previous software program will be smoothly carried out. Because setting RREG = '1' enables reading of I/O Register 8, 9, and F, the internal status under a multi-tasking OS becomes easy to grasp. When I/O Register F is read while RREG = '0', the ID Code C1H of the chip will be output; but when it is read while RREG = '1', the contents of the Control Register will be output. Even if reading of I/O Registers 8 and 9 is attempted while RREG = '0', the CPU Data Bus CD_0-CD_7 will assume high-impedance status and no data will be output (and the BDIR pin will output '0').

(4) STBY: Enables the Standby Mode

STBY = '1' enables the Standby Mode provided for power conservation. In Standby Mode, the Internal Clock stops and the majority of the circuits cease operation so that power dissipation is reduced. Since the majority of the circuits will not be operating (the contents of the Internal Registers will be stored), when a DRAM requiring refreshing is used as VRAM, the contents of that DRAM will be destroyed. Some output pins will assume high-impedance status (RD bus, AD bus, and MEMRDY), while the others will continuously output a fixed value. (Such negative-logic pins as $\overline{EC}$ and $\overline{XA}$ will continuously output a high signal, the other pins will continuously output a low signal, and certain pins will continuously output a signal of random (but constant) level.) To cancel Standby Mode, first set Bit 3 (Enable Video) of the Mode Register to '0' to assume the Display OFF status, next set STBY to '0', then set the Display ON status (Enable Video = '1') after the operation of the internal circuits has stabilized (Assume Display OFF status during the interval of two vertical scans. In case DRAM is used, also write Display Data.) (Read/write operations with the I/O registers is also possible during Standby Mode.)

3-6-16. Address 2AH

(Cleared by RESET)

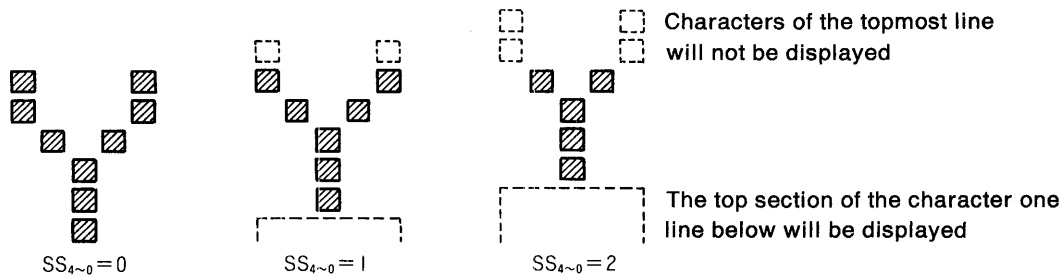
(1) TST_2-TST_0: For PCDC testing

TST_2-TST_0 must always be set to '0' for use. (When '1' are set, normal operation cannot be achieved.)

(2) SS_4-SS_0: Offset value for smooth scrolling

The display will be shifted upward for the quantity of lines set by this Offset value. (Any lines overflowing the top edge will not be displayed.) When the offset amount is sequentially increased from

0 to the quantity of rasters forming the Font, therefore, smooth scrolling can be actualized. (After the Offset amount reaches the Maximum Raster Address, line scrolling will be performed according to the Start Address of 6845, and the offset amount will concurrently be set to "0".) The Offset value can be set in the same range as the Maximum Raster Address, and any settings exceeding that range will result in abnormal operation. The $SS_{4\text{-}0}$ setting should be done in the vertical return time.



3-6-17. Address 2BH (Control Data)

(Cleared by RESET)

The contents of this register will be output from the RD_0-RD_7 pins about the time of the rising edge of the VSY pin (VSY will rise even when set to negative polarity by SYTH='1'). Therefore, if this register is latched at the rising edge of the VSY pin, it can be used as a signal for external control (for monitor switching, Font ROM switching, etc.). This function is enabled during Non-Interlace Mode (In Interlace Mode, the register contents will not be output from the RD_0-RD_7 pins around the rising edge of the VSY pin.) when the rising edge of the VSY pin does not occur during the vertical display time. (When the rising edge of the VSY pin occurs during the vertical display time, a partial disorder of the display may occur due to the collision of Display Data and Control Data.)

3-7. CONTROL/ID REGISTER (I/O Register F)

3-7-1. Control

(Cleared by RESET) (Reading possible when RREG='1')

Bit 0 Graphic Set Enable
1 Page Set Enable (Becomes '0' in CGA Mode for HGC)
7 $\overline{\text{Protect}}$

Writing is possible to Bit 1 of the Mode Register only while Graphic Set Enable is set to '1'. Similarly, writing is possible to Bit 7 of the Mode Register only while Page Set Enable is set to '1'. Writing is possible to I/O Registers D and E (the Register Bank) only when both $\overline{\text{Protect}}$ is '1' and the $\overline{\text{IOSEL}}$ pin is '0', thereby providing protection for the Register Bank which holds the expansion functions from IBM PC.

3-7-2. ID

When this register is read while RREG='0', the ID Code C1H of the chip will be output.

4. OPERATING MODES

The Operating Modes consist basically of two types: Text Modes and Graphics Modes. The Operating Mode is specified at the Mode Register (I/O Register A). (For specifying the expanded Graphics functions or the horizontal font size for text, it will be necessary to write to Bank Register Address 24H in some cases.)

Mode Reg. Bit 5	4	3	2	1	0	MODE	IBM-PC Standard Mode
	×			0	0	Low Resolution Text	40 x 25 A/N
	×			0	1	High Resolution Text	80 x 25 A/N
×	0			1	×	Low Resolution Graphic	320 x 200 GR
×	1			1	×	High Resolution Graphic	640 x 200 GR

← The quantity of colors that can be displayed will vary according to GRM1 and GRM0.

Black/White
Enable Video
Blink

×: don't care

4-1. TEXT MODES

Except in Kanji Display Mode, one character is defined by two bytes. That is, the even bytes are used for specifying the Character Codes (The higher-order addresses of an external Font ROM are used. The Raster Address RA0-RA4 is used for the lower-order address.), and the odd bytes are used for specifying the Attribute Codes.

Character-Code Byte (cc)

7	6	5	4	3	2	1	0

↑
The addresses of the Character Font ROM

Attribute Byte (AT)

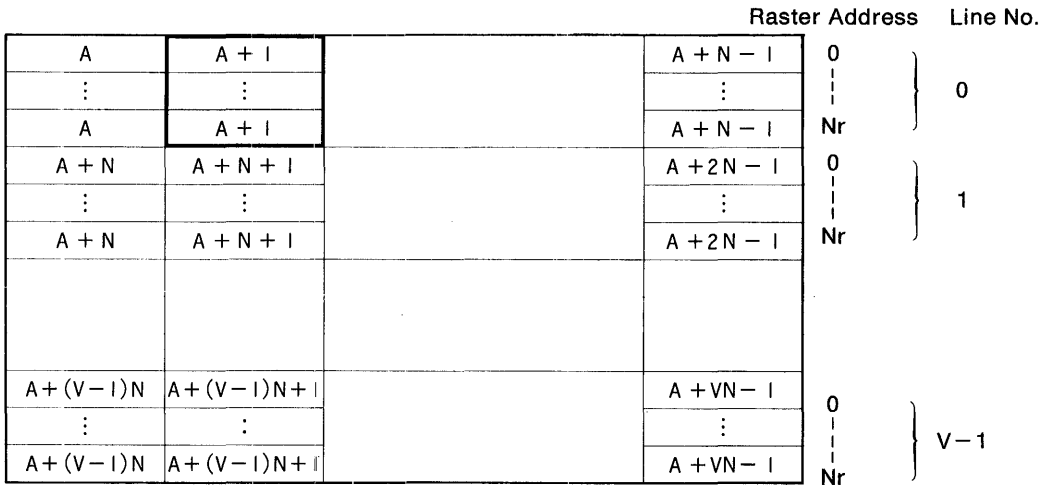
7	6	5	4	3	2	1	0
BL	R	G	B	I	R	G	B

↑ Blink ↑ Background ↑ Foreground

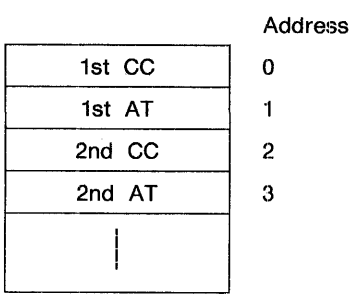
The Font ROM data is input to PCDC by the $\overline{EC}$ pin via the RD bus. (The leading Display Data is connected for sequential input from RD7 to RD0. If the data consists of nine or more bits, the ninth bit and any consecutive bits are connected in the sequence of R15 to RD8.)
When data from the Font ROM exists (when RD = '1'), the color (out of 16 possible colors) specified by the lower four bits (Foreground) of the Attribute code is displayed. When no data from the Font ROM exists (when RD = '0'), the color (out of 8 possible colors equivalent to Intensity bit = '0' of IRGB) specified by Bits 4, 5, and 6 (Background) of the Attribute code is displayed. However, the above holds true in case Bit 5 (Blink) of the Mode Register is '1'. When Blink = '0', the text will not blink and, when no data from the Font ROM exists, the color specified by the highest four bits of the Attribute code is displayed. (The MSB of the Attribute code will become the Intensity bit of the Background to enable selection from 16 colors.)
When Blink = '1', any character for which the MSB BL of the Attribute Code is '1' will blink in 32-field cycles. That is, the Background color (one of 8 colors) will be displayed during a 16-field interval, regardless of the presence/absence of data from the Font ROM; then, during the next 16-field interval, the Foreground and Background colors will be displayed according to the presence/absence of data from the Font ROM.

The difference between the Low Resolution and High Resolution Text Modes is that the text is respectively displayed as single and double PELs. For details, see section 3-2, "MODE REGISTER."

The shape of the cursor is controlled by the Cursor Start Raster Register (R10) and Cursor End Raster Register (R11), and its display position is specified using the Cursor Address Registers (R14, R15).



When Start Address (R12, R13) = "A", horizontal display character = "N", vertical display character = "V", and Maximum Raster Address = "Nr" have been set, the relationship between the screen display position of the Refresh Memory Addresses and the Raster Addresses conforms to the above figure. Taking the character at Address "A + 1" as an example, the address of A + 1 is output "Nr + 1" times (at each output, the Raster Address is sequentially incremented from 0 to Nr), and the VRAM data having that address is read at each output (in two-byte units, with the even bytes signifying the Character Codes and the odd bytes signifying the Attribute Codes). Next, the Character Code read from VRAM is latched by an external circuit and input to the higher-order address of the Font ROM. Since the Raster Address is input to the lower-order address, each time the Address A + 1 arrives, the data of the consecutive lines (from 1st to lower) is read. (Line switching is performed according to the Raster Addresses.) Then, according to the Attribute Code that is read together with the Character code from VRAM, the color is selected for the higher- or lower-order bits depending on whether Font data is present or absent, and the character is displayed. At this time, when A + 1 has been set at the Cursor Address Registers (R14, R15), the cursor will also be displayed over the character being described above. Similar to the case when Font data is present, the cursor color will be selected according to the lower four bits (Foreground) of the Attribute Code. In case both B and P of the Cursor Start Raster Register are set to '0' as with the IBM PC Standard, the cursor will blink in 16-field cycles. The border of the display area will be displayed in the color selected by Bits 0-3 of the Color Register. (When BINH = '1', the border will be displayed in black, the equivalent of IRGB = "0000".)



The memory map for Text Mode consists of two-byte units as shown on the left. (Be sure that the even bytes are Character Codes and the odd bytes are Attribute Codes.)

There are two types of Kanji Display Modes: one processes kanji in two-byte units and the other in four-byte units. In case of two-byte units (GRM0 = '0'), a portion of the odd bytes used for Character Code(H) is used, so the Attributes will become simplified. In case of four-byte units (GRM0 = '1'), two bytes are used for the Character Code, one byte is unused, and the remaining byte is used for the Attribute Code (with functions identical to those of Text Mode). For details, see the description of kanji display on Page 30 of subsection 3-6-10, "Address 24H."

0	Character Code (L)
1	Character Code (H)
	+ simple Attributes

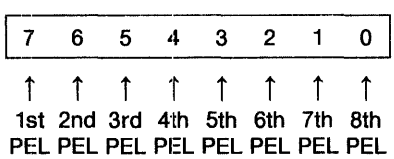
0	Character Code (L)
1	Character Code (H)
2	Not used
3	Attribute

4-2. GRAPHICS MODES

4-2-1. 1 Byte Modes

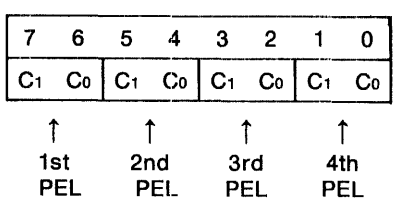
There are two types of IBM PC Standard Graphics Modes: the 640 x 1 Bit Mode (with 200 rows of 640 PELs, and referred to as the High Resolution Graphics Mode for the IBM PC) wherein each bit of a byte has a 1:1 correspondence with the display PELs, and the 320 x 2 Bit Mode (with 200 rows of 320 PELs, and referred to as the Medium Resolution Graphics Mode for the IBM PC) which controls the display color using two-bit units of one byte (so that the size of display PELs in the horizontal direction is double that of the 640 x 1 Bit Mode).
The numerals 640 and 320 are representative examples of the quantity of display PELs in the horizontal direction and that quantity is changed by the setting at the Horizontal Displayed Register (R1). Therefore, the 720 x 348 Graphics Mode of Hercules can also be displayed. (Its Display Mode is identical to that of the 640 x 1 Bit Mode, but the only quantity of display PELs differs.)

4-2-1-1. 640 x 1 Bit Mode



This mode is enabled when GRM1 = GRM0 = '0' and Bit 4 of the Mode Register is '1'. The display PELs have a 1 : 1 correspondence with each bit of the bytes read from VRAM. When data exists (RD = '1'), the color (out of 16 possible colors) selected by Bits 3-0 of the Color Register is displayed. When no data exists (RD = '0'), black (IRGB = "0000") is displayed. The border is similar displayed in black (IRGB = "0000").

4-2-1-2. 320 x 2 Bit Mode



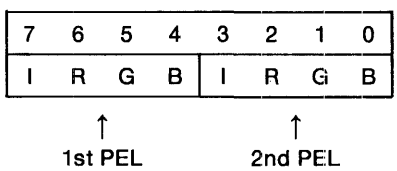
This mode is enabled when GRM1 = GRM0 = '0' and Bit 4 of the Mode Register is '0'. Since two bits of each datum read from VRAM specify the color of the display PEL, up to four colors can be simultaneously displayed.
The size of the display PELs in the horizontal direction is double that of the 640 x 1 Bit Mode.

The four colors that can be displayed are preset as two types (SET1 and SET2), and are selected by Bit 5 of the Color Register. (Bit 5 = '1' selects SET2.) When Bit 2 of the Mode Register is '1' (B/W = '1'), however, both SET1 and SET2 become the same color set.

C_1	C_0	Color	SET1				SET2				B/W = 1			
			I	R	G	B	I	R	G	B	I	R	G	B
0	0	Background	SEL I	SEL R	SEL G	SEL B	SEL I	SEL R	SEL G	SEL B	SEL I	SEL R	SEL G	SEL B
0	1	Color 1	SEL IN	0	1	0	SEL IN	0	1	1	SEL IN	0	1	1
1	0	Color 2	SEL IN	1	0	0	SEL IN	1	0	1	SEL IN	1	0	0
1	1	Color 3	SEL IN	1	1	0	SEL IN	1	1	1	SEL IN	1	1	1

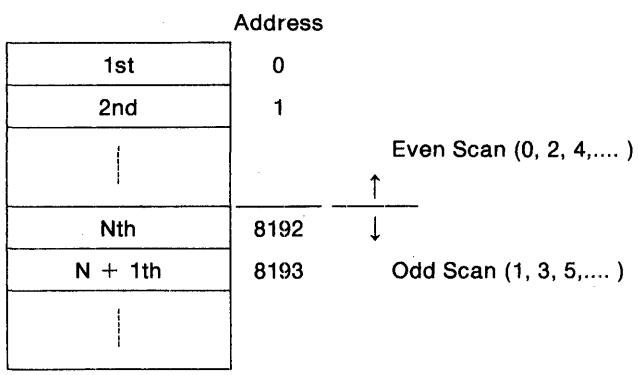
When $C_1 = C_0 =$ '0', the color is selected by Bits 3-0 (sequentially, SEL-I, -R, -G, and -B) of the Color Register for display. (The same holds true for the border, but when BINH = '1', the border will be displayed in black (IRGB = "0000").)
Each of the color 1-3 is able to select SET1 or SET 2. Bit 4 (SEL-IN) of the Color Register also controls the Intensity of the color 1-3.

4-2-1-3. 160 x 4 Bit Mode



This mode is enabled when $GRM_1 = GRM_0 =$ '1'. Since the color of each display PEL is specified in four-bit units of the data read from VRAM, up to 16 colors can be simultaneously displayed. The size of the display PELs in the horizontal direction is four times that of the 640 x 1 Bit Mode. The border will be displayed in the color selected by Bits 3-0 of the Color Register (but when BINH = '1', the border will be displayed in black (IRGB = "0000")).

(Memory Map)
The CGA software for the IBM PC is designed so that the data of the even lines and odd lines is stored in separate banks, then the banks are switched according to the Raster Address RA_0 for the reading of the data (2 Bank Mode).



With Hercules software, the data is stored in separate banks in four-line cycles, then the banks are switched according to the Raster Address RA_0, RA_1 (4 Bank Mode). That is, the data of Lines 0, 4, 8, ... is placed in the first 8K bytes, the data of Lines 1, 5, 9, ... is placed in the next 8K bytes, the

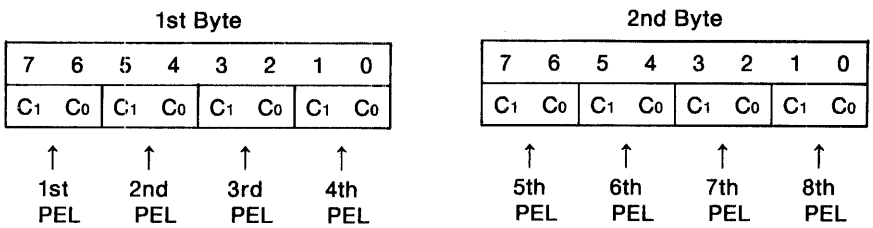
data of Lines 2, 6, 10, ... is placed in the next 8K bytes, and the data of Lines 3, 7, 11, ... is placec in the last 8K bytes. As result, a memory capacity that is double that for the 2 Bank Mode is required.

The units (per character) for setting the horizontal- related 6845 registers is 16-PEL units by 640 x 1 Bit Mode conversion in case of the Graphics Mode. Be sure to use memory from a even-numbered address.

4-2-2. 2 Byte Modes

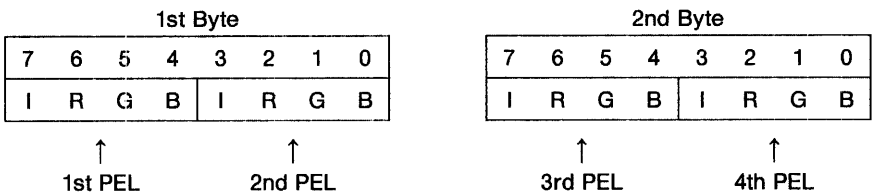
In the Graphics Modes expanded beyond the IBM PC Standard, a memory capacity double (per bank) that of the 1 Byte Mode is required, but an increased quantity of colors can be simultaneously displayed.

4-2-2-1. 640 x 2 Bit Mode



This mode is enabled when GRM1 = '0', GRM0 = '1', and Bit 4 of the Mode Register is '1'. The display colors are identical to those of the 320 x 2 Bit Mode (simultaneous display of four colors), and the size of display PELs is identical to that of the 640 x 1 Bit Mode.

4-2-2-2. 320 x 4 Bit Mode

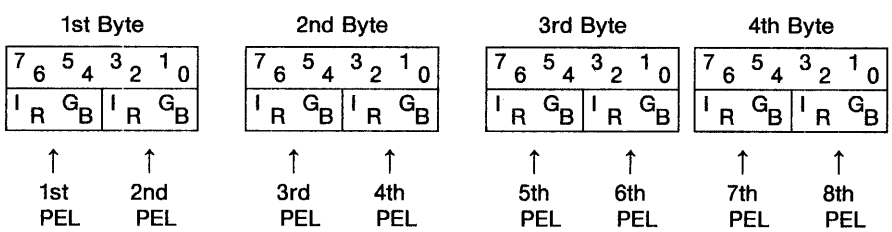


This mode is enabled when GRM1 = '0', GRM0 = '1', and Bit 4 of the Mode Register is '0'. The display colors are identical to those of the 160 x 4 Bit Mode (simultaneous display of 16 colors), and the size of display PELs is identical to that of the 320 x 2 Bit Mode.

4-2-3. 4 Byte Modes

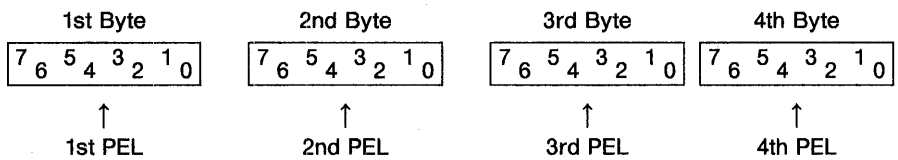
In the Graphics Modes expanded beyond the IBM PC Standard, a memory capacity four times (per bank) that of the 1 Byte Mode is required, but an increased quantity of colors can be simultaneously displayed, making possible a variegated display.

4-2-3-1. 640 x 4 Bit Mode



This mode is enabled when GRM1 = '1', GRM0 = '0', and Bit 4 of the Mode Register is '1'. The display colors are identical to those of the 160 x 4 Bit Mode (simultaneous display of 16 colors), and the size of display PELs is identical to that of the 640 x 1 Bit Mode.

4-2-3-2. 320 x 8 Bit Mode



This mode is enabled when GRM1 = '1', GRM0 = '0', and Bit 4 of the Mode Register is '0'. Since the color of each display PEL is specified in byte units, up to 256 colors can be simultaneously displayed. The size of the display PELs is identical to that of the 320 x 2 Bit Mode. The border will be displayed in the color selected by Bits 3-0 of the Color Register (but when BINH = '1', the border will be displayed in black (IRGB = "0000")).

7	6	5	4	3	2	1	0
R_2	R_1	R_0	G_2	G_1	G_0	B_2	B_1

(B0 is identical to B2)

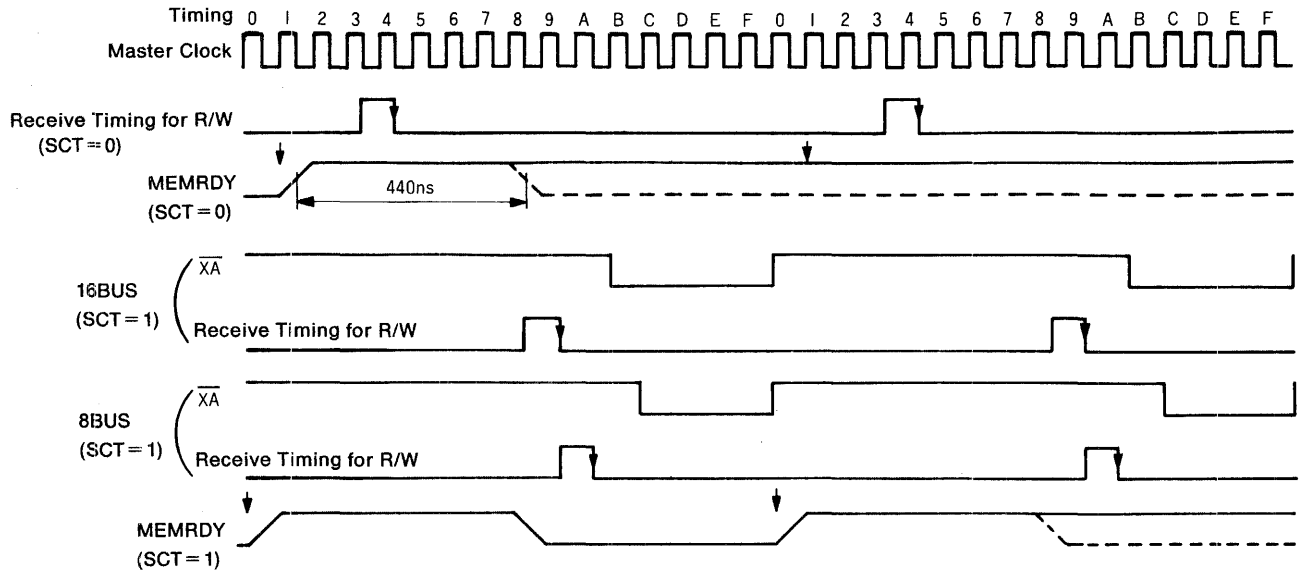
When CPLE = '1' and SWC = '1', the eight-bit data will be sequentially output to correspond to each bit of the Color Palette as shown above. (The Color Palette will not be used, but set CPLE = '1'.) This eight-bit output is used as the addresses of an external Color Lookup Table, enabling the simultaneous display of 256 colors out of large number of colors (for example, 4096 colors). B_0 is made an output identical to B_2 so that the Blue 2 bit is converted into a pseudo Blue 3 bit as shown below:

B 1	B 0	B_2	B_1	B_0
0	0	0	0	0
0	1	0	1	0
1	0	1	0	1
1	1	1	1	1

Consequently, 256 colors can be simultaneously displayed even if the three respective bits of R, G, and B are connected via a digital-to-analog converter to a linear RGB monitor.

5. MEMORY

Since the PCDC allots time for the CPU even during display time, CPU can also read and write with respect to VRAM. (Reading and writing are possible at any time without waiting the retrace line time and without any display disturbance.) Since the timing the PCDC allots for the CPU and the timing for the arrival of Read/Write instructions from the CPU are asynchronous, a method has been adopted in which a Wait state is applied to the CPU by MEMRDY. This enables the CPU to read from and write to memory without requiring consideration for the timing during PCDC-VRAM data transfer.



The rising edge of MEMRDY is synchronized with Timing 1 of the above figure. On the other hand, the timing for Read/Write instructions from the CPU to VRAM conforms to Timing 4. Consequently, the minimum Wait time consists of approximately 13 Master Clock cycles from the time a Read/Write instruction is input at Timing 4, while the maximum Wait time consists of approximately "13 + 16" Master Clock cycles from the time a Read/Write instruction is input at Timing 5. For example, in case the Master Clock frequency is 14.318 MHz, the Wait time will be 0.9 to 2.0 microseconds.
Since the interval between the rising edge of MEMRDY until the Read/Write instruction is received consists of only about three Master Clock cycles (210 ns in case the Master Clock frequency is 14.318 MHz). As result, when a high-speed CPU is used, even if the next Read/Write instruction arrives 440 ns after the Wait state is canceled, it cannot be received and must await the next R/W Receive timing. The Wait time in case of a 14.318 MHz Master Clock frequency will thus be as follows:

$$\frac{1000}{14.318} \times 16 \times 2 - 440 = 1795 \text{ ns} \fallingdotseq 1.8 \ \mu\text{s}$$

Since the use of a high-speed CPU is meaningless at the above speed, the PCDC provides a timing for a high-speed CPU in order to minimize the Wait time. When SCT is set to '1' (see Paragraph (1) of subsection 3-6-9, "Address 23H"), the rising edge of MEMRDY will synchronize with Timing 0 of the preceding figure, and the Receive Timing for Read/Write instructions will synchronized with either Timing 9 for a 16-bit bus configuration of the VRAM or Timing A for an eight-bit bus configuration of the VRAM. (In case the horizontal font size if 6 or 7, SCT will be invalid.)

Consequently, the interval from the rising edge of MEMRDY to the Receive Timing for a Read/Write instruction will consist of approximately nine Master Clock cycles (550 ns even in case of a 16.257 MHz Master Clock Frequency). When a high-speed CPU used, since a Read/Write instruction arriving 440 ns after the Wait state is canceled will be received, the Wait time in case of a 14.318 MHz Master Clock frequency will be as follows:

$$\frac{1000}{14.318} \times 16 - 440 = 677 \text{ ns} \fallingdotseq 0.68\ \mu s$$

With an 8 MHz high-speed CPU, assuming that the interval following the cancellation of the Wait state until the output of the next Read/Write instruction lasts approximately 3.5 to 4.5 Processor Clock cycles, the Wait time will be 437.5 to 562.5 ns, so the Wait time reduction by SCT = '1' will become effective.

5-1. ADDRESS CONNECTION

The PCDC permits selection of either SRAM or DRAM for use as VRAM. In addition, an 8-bit or 16-bit bus configuration can be selected for the VRAM data bus. In subsection 3-6-12, "Address 26H," the address output in case of a 16-bit bus configuration using SRAM was previously discussed. The table below describes the address output for the other cases.

Pin Name / Conditions of Use	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
SRAM, 16-bit bus	V15	V14	V13	V12	V11	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0
SRAM, 8-bit bus	V14*	V13	H/L	V12	V11	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0
DRAM, 16-bit bus	GPE			V12/V15	V11/V13	V10/V4	V9/V3	V8/V2	V7/V1	V6/V0	V5/V14		$\overline{CAS}$	$\overline{RAS}$	$\overline{XC}$	$\overline{XR}$
DRAM, 8-bit bus	GPE			V12/V14	V11/H/L	V10/V4	V9/V3	V8/V2	V7/V1	V6/V0	V5/V13		$\overline{CAS}$	$\overline{RAS}$	$\overline{XC}$	$\overline{XR}$

V15-V0 in the above table are the addresses output to the AD15-AD0 pins described in subsection 3-6-12. The "H/L" bit of the 8-bit bus configuration is the address for selecting the odd or even address byte. (H/L = '1' selects the odd address byte. With the 16-bit bus configuration, two bytes (odd and even) are simultaneously accessed, so H/L is not output.) When Register Bank A15 = '0', V14* of a SRAM 8-bit bus outputs GPE. (GPE is the ORed output of Bits 0 and 1 of the Control/ID Register.) When DRAM is in use, the Row addresses and Column addresses are output according to time sharing, and "a" and "b" of an address expressed as "a/b" respectively signifies a Row Address and Column address. In addition, the $\overline{RAS}$ and $\overline{CAS}$ timing required for DRAM use as well as the $\overline{XR}$ and $\overline{XC}$ signals for switching the CPU addresses are also output from the AD3-AD0 pins.
PCDC employs a method of outputting only the addresses for display use to VRAM, with the addresses from CPU for accessing VRAM being externally multiplexed. The LSB of the CPU-side addresses are used for specifying the even and odd address bytes. With an 8-bit bus configuration, therefore, the LSB on the CPU side is connected to the bit corresponding to H/L. With a 16-bit bus configuration, the $\overline{WE}$ signal of VRAM is externally generated from the WE signal of PCDC and the LSB on the CPU side (see CHAPTER 7, "SYSTEM CONFIGURATIONS") and controls writing to the even and odd address bytes. (At this time, the output to the VRAM data bus, the switching between the odd and even address bytes during reading, and so on, are performed by the A0 pin, which is connected to the lowest-order address on the CPU side.) The other addresses of CPU are sequentially connected from the lowest bit to correspond to V0-V15.

CPU	VRAM Bus Configuration	$A_0=0$		$A_0=1$	
		Read	write	Read	write
8-bit bus CPU	8-bit bus configuration	$RD_{7\sim0}$	$RD_{7\sim0}$	$RD_{7\sim0}$	$RD_{7\sim0}$
	16-bit bus configuration	$RD_{7\sim0}$	$RD_{7\sim0}$	$RD_{15\sim8}$	$RD_{15\sim8}$
16-bit bus CPU	16-bit bus configuration	$RD_{7\sim0}$	$RD_{7\sim0}$	$RD_{7\sim0}$	High Impedance

The above table describes whether the higher- or lower-order side of the VRAM data bus will be valid, depending on the bus configuration of VRAM and CPU. The data bus that is disabled during writing will assume the high-impedance state.

5-2. DRAM REFRESH

DRAM requires refreshing for each of the 128 Row addresses within 2 ms at most, or for each of the 256 Row addresses within 4 ms at most. Though the address output for display use should preferably satisfy the above conditions, the screen configuration will prevent them from being satisfied in some cases.

For this reason, PCDC outputs the address for Refreshing outside of display time (during retrace line time). Since the addresses for display use are output during an period formed by the "value set to the Horizontal Displayed Register during Low Resolution Text or Graphics Mode + 1" (The value for High Resolution Text Mode must be divided by two for conversion into the value of the Low Resolution Text Mode), the difference of horizontal total character minus this period will become the timing for outputting the address for Refreshing. The addresses for Refreshing are output while counting only this interval. The count of the Refresh address at the next line will begin from the next address of the last one for Refreshing. The Refresh address counter consists of eight bits and the Refresh timing is output as a Row address, so $\overline{RAS}$-only Refreshing can be performed. (Outside the display time, $\overline{CAS}$ is output at high level.) Assuming the setting of the horizontal total character to "M", the horizontal displayed character to "D", and the time for one horizontal character as "T", perform setting so that the below relationship is satisfied:

$$M \times T \times \left[\!\left[\frac{128}{M - (D + 1)} \right]\!\right] < 2\ ms \qquad \text{Equation 1}$$

In the above equation, the double brackets "[[ ]]" signify that all values shall be rounded to integers. Taking the example of a CGA-Standard setting with a Master Clock frequency of 14.318 MHz, since $M = 38_H + 1$ and $D = 28_H$, their decimal equivalents become $M = 57$ and $D = 40$, resulting in the below equation:

$$T = \frac{1}{14.318} \times 16 = 1.117\ \mu S \qquad \text{Equation 2}$$

Substituting Equation 2 into Equation 1 gives the following result, so it is evident that the Refresh conditions have been satisfied:

$$57 \times 1.117 \times \left[\!\left[\frac{128}{57 - 41} \right]\!\right] = 57 \times 1.117 \times 8 = 509\ \mu s < 2\ ms$$

With SRAM, note that refreshing is unnecessary and that setting can be freely performed without the above restrictions.

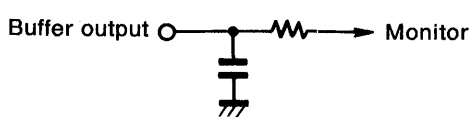
6. MONITOR INTERFACES

6-1. DIGITAL INPUT CRT

A digital input CRT, such as the IBM color monitor, IBM monochrome monitor, EGA monitor, etc., is connected via a buffer (74LS244). (A buffer is required due to the large lead-in current of the monitor.) Any of these monitors is connected using a 9-pin D-shell connector, but be sure that the output from PCDC avoids conflict within its pin arrangement.

Connector Pin No.	Color Monitor	Monochrome Monitor	EGA Monitor	PCDC Pin Name	Bit of Color Palette
1	Gnd	Gnd	Gnd	Vss	
2	(Gnd)	(Gnd)	Secondary Red	LD_2	G_2
3	Red		Primary Red	LD_6	B_2
4	Green		Primary Green	LD_5	B_1
5	Blue		Primary Blue	LD_4	B_0
6	Intensity	Intensity	Secondary Green	LD_7	G_0
7		Video	Secondary Blue	LD_3	R_0
8	Hsy	Hsy	Hsy	Hsy	
9	Vsy	−Vsy	−Vsy	Vsy	

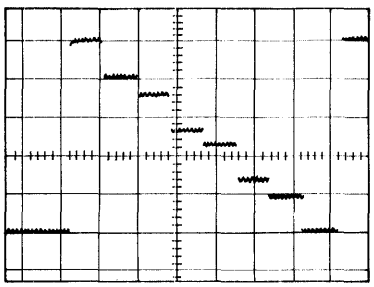
Since Pin 2 requires grounding with a color or monochrome monitor (PCDC will output '0' level to Pin 2), so allow selection of Gnd or LD_2 between an EGA monitor and others. With a monochrome monitor, even in case of using Gray Scaling/Hatching Mode and setting IEN to '1' to use Intensity, the Intensity signal will be output from the same pin listed in the above table (Set $LS_1 = LS_0 = $ '0' to enable the 1 Bit Serial Mode.). In case an EGA monitor will be used, perform setting so that the desired output can be achieved using the Color Palette (referring to the correspondence between the Color Palette bits in the above table). The same hold trues when using the Color Palette with a color monitor (also setting CPLE = '1' to enable the Color Palette). Since the Vertical Sync signals will be positive pulses for a color monitor, and will be negative pulses for a monochrome or EGA monitor, their polarity is reversed. But since the polarity is controlled by SYTH (SYTH = '1' selects negative pulses), external control of polarity is unnecessary.



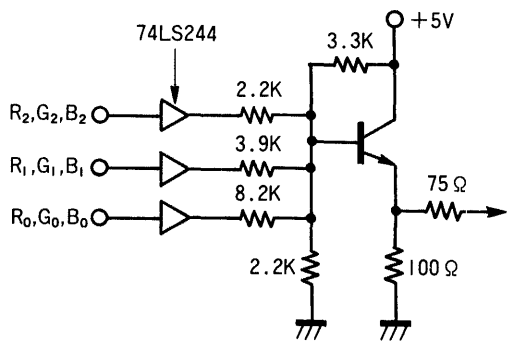
Note that the insertion of a capacitor and resistor after the buffer is effective in reducing the interference between signals and preventing color deviation. (The respective values of the capacitor and resistors should be about 47p and 30 ohms.

6-2. LINEAR RGB MONITOR

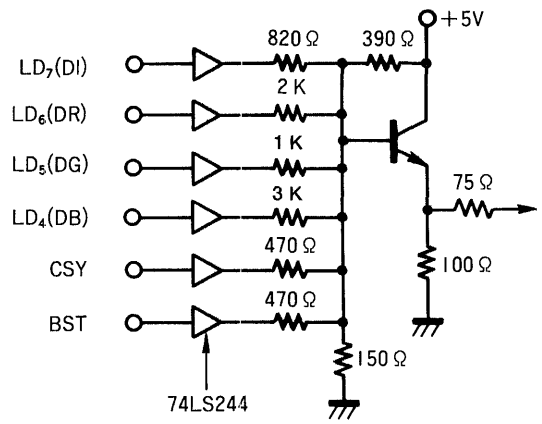
Using a simplified method of digital-to-analog conversion which mixes the signal which outputs three bits each of R, G, and B via mixing resistors that conform to the weighting of those bits, the signal is converted into an analog signal for connection to a linear RGB monitor. The method of digital-to-analog conversion is simple but requires only a small number of bits, and provides a satisfactory linearity similar to that of a photograph. When a linear RGB monitor will be used, be sure to set CPLE='1' and SWC='1' CSY shall be used as the Sync signal. (CSY is a Composite Sync signal created from the Horizontal and Vertical Sync signals, and is output from the CSY pin.)



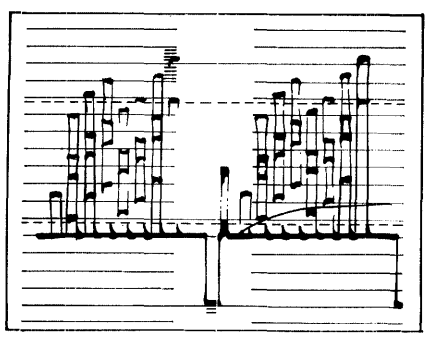
(A Waveform after Digital-to-Analog Conversion)



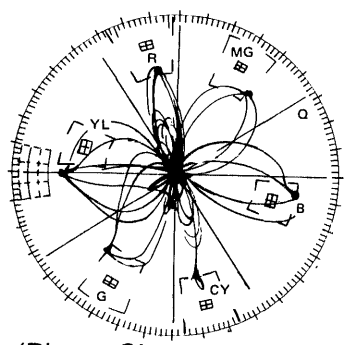
6-3. COMPOSITE INPUT CRT



The Composite signals are created by resistor mixing. An NTSC color display is valid only with a 14.318 MHz (4fsc) Master Clock frequency. The mixing of DR, DG, and DB serves to provide the differences in intensity according to color, but colors will be displayed without the mixing. Mixing of $\overline{BLA}$ or LD0 ($\overline{BFP}$) respectively enables the control of the pedestal level or of the Color Burst signal offset. The B/W Composite signals can be achieved by avoiding mixing of BST, but gray scaling of 16 shades can be achieved by mixing DI, DR, DG, and DB (the mixing resistors will differ from those used for color display).



(Output Waveform)

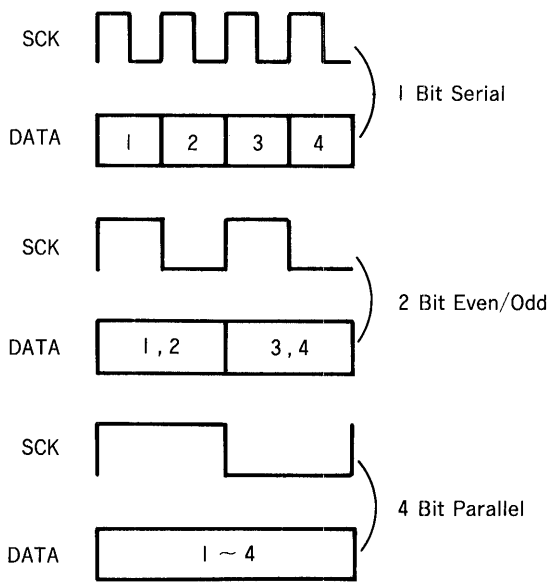


(Phase Characteristics)

The preceding photographs depict the output of an NTSC-standard Composite signal and its phase characteristics in the case of a 14.318 MHz Master Clock frequency (when using the previously-shown circuit).
The Composite signals can also be created from the signals used for a linear RGB monitor, by inputting the signals for linear RGB (R, G, B, and CSY) into a commercially available NTSC encoder (Motorola's MC1377, Rohm's BA7230L, etc.) and externally mounting a 3.58 MHz (fsc) X'tal for oscillation of the color subcarriers. (For details, refer to the reference materials on NTSC encoders.)

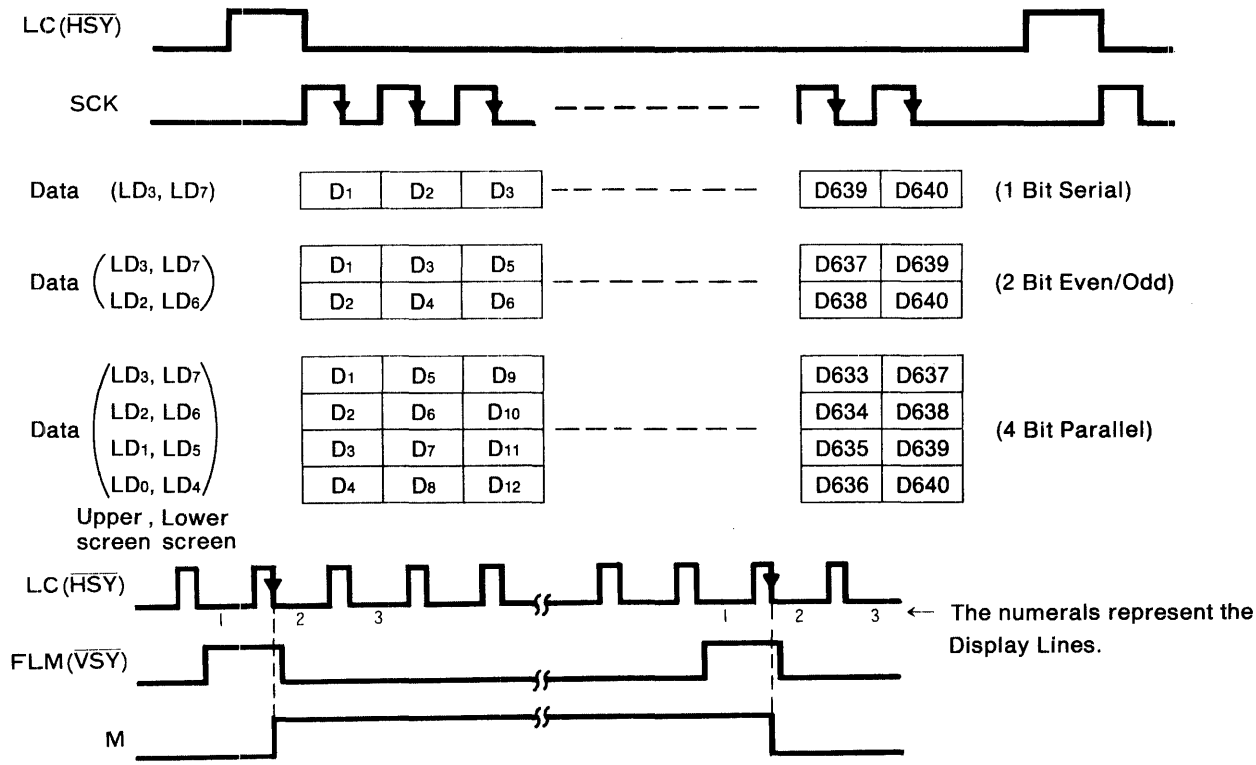
6-4. LCD

Manufacturers are marketing a variety of LCD panels (with one- or two-screens or differences in the duty, quantity of horizontal display PELs, quantity of bits for data transmission, etc.). Nevertheless, PCDC is capable of connection to these various LCDs by setting the Register Bank. (Connection can be made either directly or via a CMOS buffer).

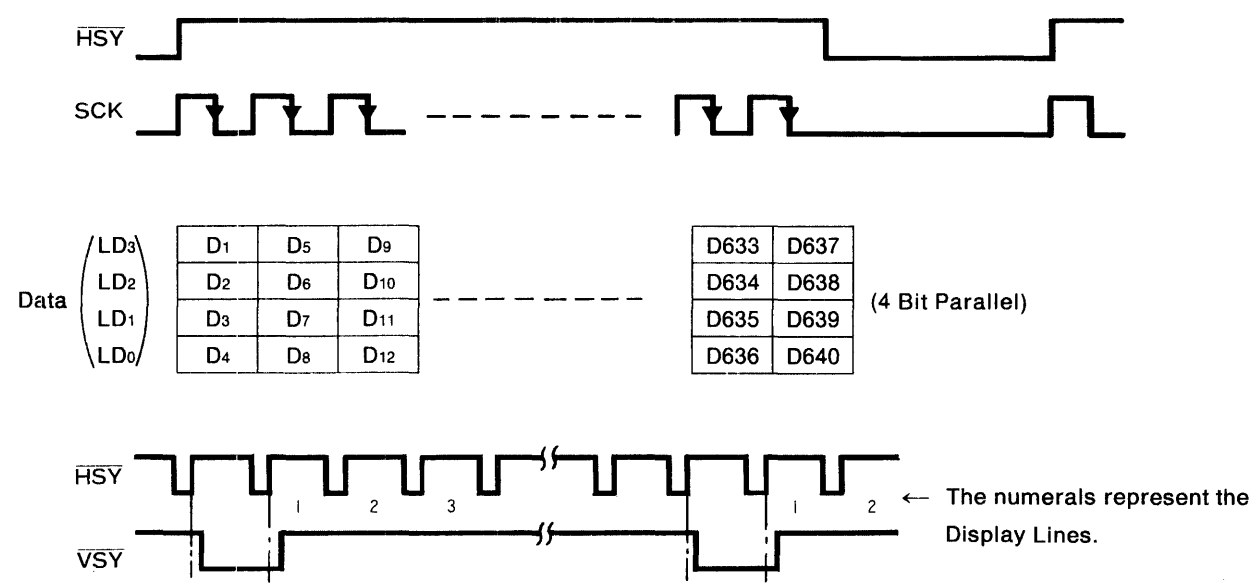


According to the increase in the quantity of data transmission bits, the relationship between the transmission data (DATA) and the Shift Clock (SCK) conforms to the figure on the left. Though the time required for sending the data for four PELs is the same in any case, an increase in the quantity of transmission bits will reduce the SCK frequency. In case of 8Bit Parallel, the SCK frequency will be further reduced by half. In all cases, the first half of the data is sent when SCK='1' and the last half is sent when SCK='0', so starting the transmission of data at the falling edge of SCK is appropriate for LCD panels. When using a one-screen LCD or a single-drive type two-screen LCD, the SCK cycles during 1Bit Serial Mode are identical to those of the Master Clock. Since the data for both the top and bottom screens are simultaneously transmitted for a dual-drive type two-screen LCD, however, the SCK cycles in 1Bit Serial Mode are double those of the Master Clock.

With a dual-drive type two-screen LCD, the data of the upper and lower screens is respectively output to LD_{3}-LD_{0} and LD_{7}-LD_{4}. For other LCDs, the data is output to LD_{3}-LD_{0}.



6-5. PLASMA DISPLAY

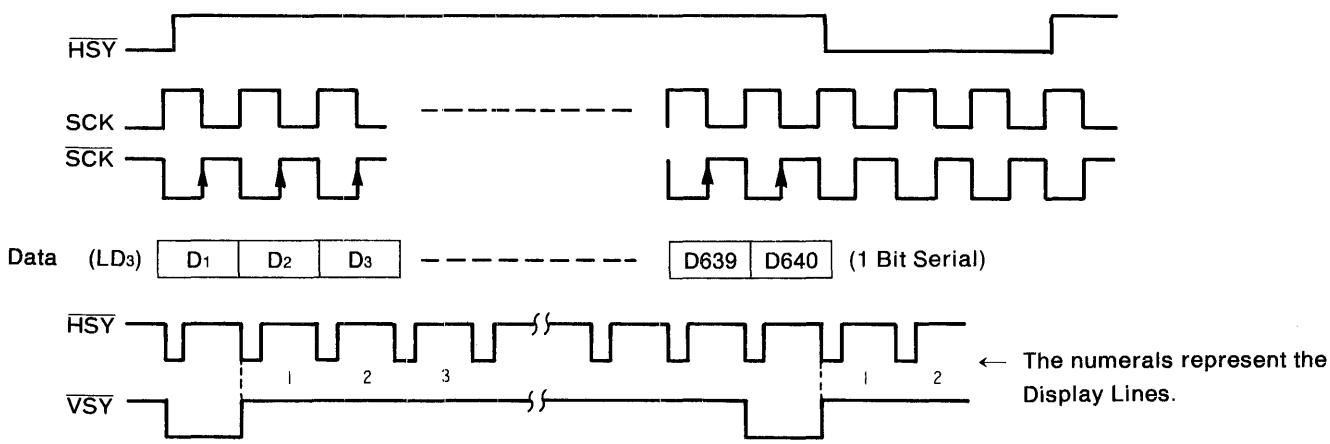


(Though the quantity of bits used for data transmission is varied, the above figure illustrates the case of 4Bit Parallel Mode.)

For plasma displays as well, manufacturers are marketing a variety of types (with differences in the quantity of horizontal/vertical display PELs, quantity of bits for data transmission, etc.). Nevertheless, PCDC is capable of connection to these various types of panels by setting the Register Bank. Though $\overline{HSY}$ and $\overline{VSY}$ for Panel use do not satisfy interface specifications in some panels, HSY and VSY for CRT use can be inverted and used to achieve connection. Consequently, connection can be made either directly or via a CMOS buffer (an inverting buffer in some cases).
With a one-screen plasma panel, the relationship between DATA and the Shift Clock SCK is identical to the case of LCDs. For panels capable of Intensity input, set IEN to '1' and perform connection to output Intensity to LD_7-LD_4. (A double-sequence output will be formed, but it will not affect the relationship between DATA and SCK.)

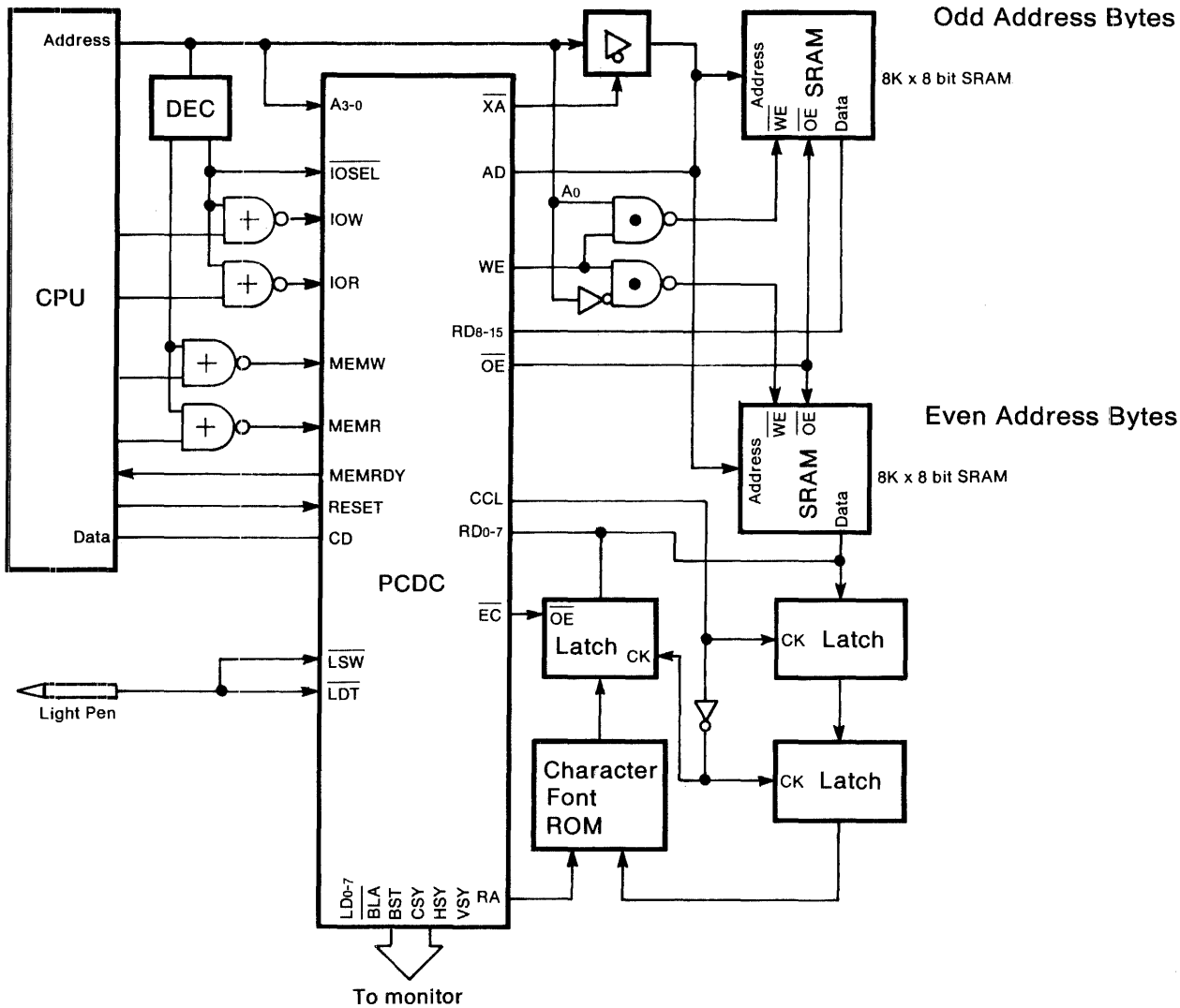
6-6. EL PANEL

EL panels can also be connected to PCDC. Although a few manufacturers presently exists, the interface specifications can be satisfied by inverting the Shift Clock for connection. (Connection can be made either directly or via a CMOS buffer (an inverting buffer for SCK only).)
With a one-screen EL panel as well, the relationship between DATA and the Shift Clock SCK is identical to the case of LCDs. (Actually, since inverted SCK signals are used, the first half of the data is sent when $\overline{SCK}$ = '0' and the last half is sent when $\overline{SCK}$ = '1', which is suited for beginning data transmission at the rising edge of $\overline{SCK}$.)

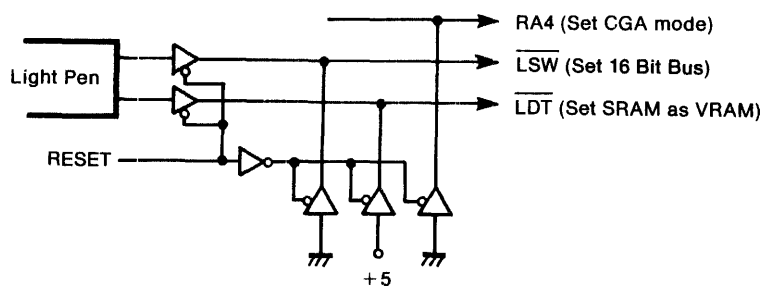


7. SYSTEM CONFIGURATIONS

7-1. USE OF SRAM (For 16-Bit Bus, CGA)

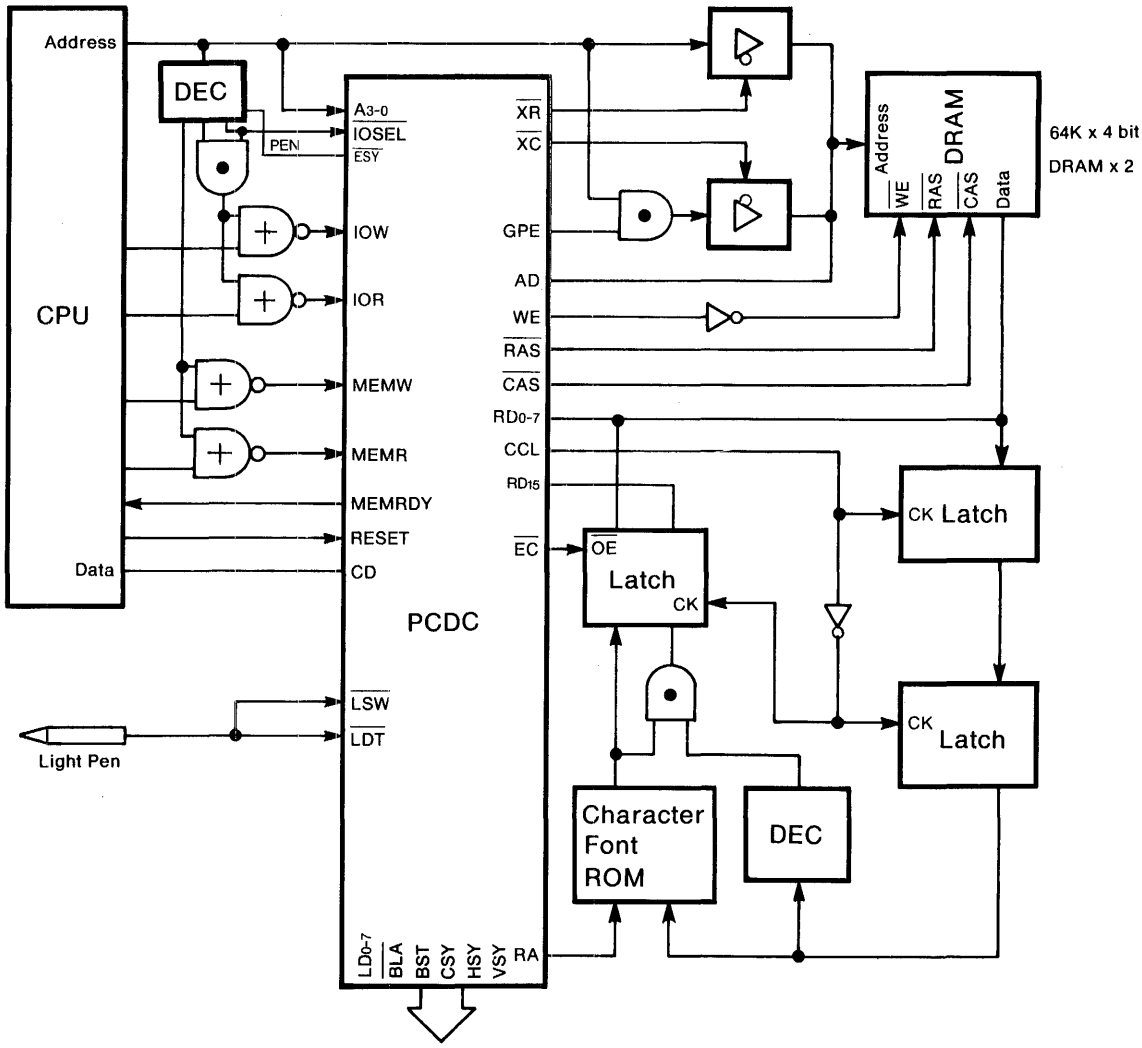


Initialization can be achieved by software according to the above figure.
Initialization by hardware will conform to the below figure.



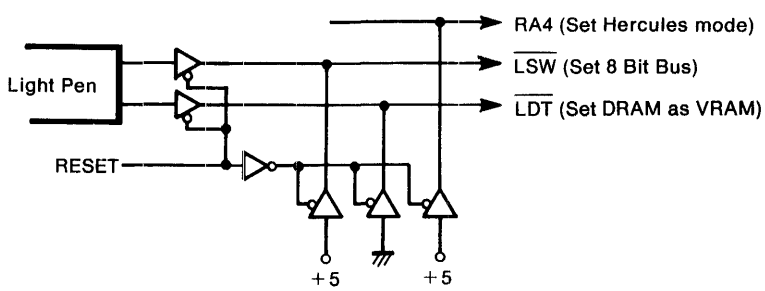
The above configuration also permits display in the expanded Graphics Modes (The memory capacity, however, needs to be expanded.).
In case only graphics will be displayed, the Latch and Character Font ROM can be omitted.
Since SRAMs are being used, the Hercules Mode or an 8-bit bus configuration is also possible.

7-2. USE OF DRAM (For 8-Bit Bus, Hercules)



Initialization can be achieved by software according to the above figure.
Initialization by hardware will conform to the below figure.

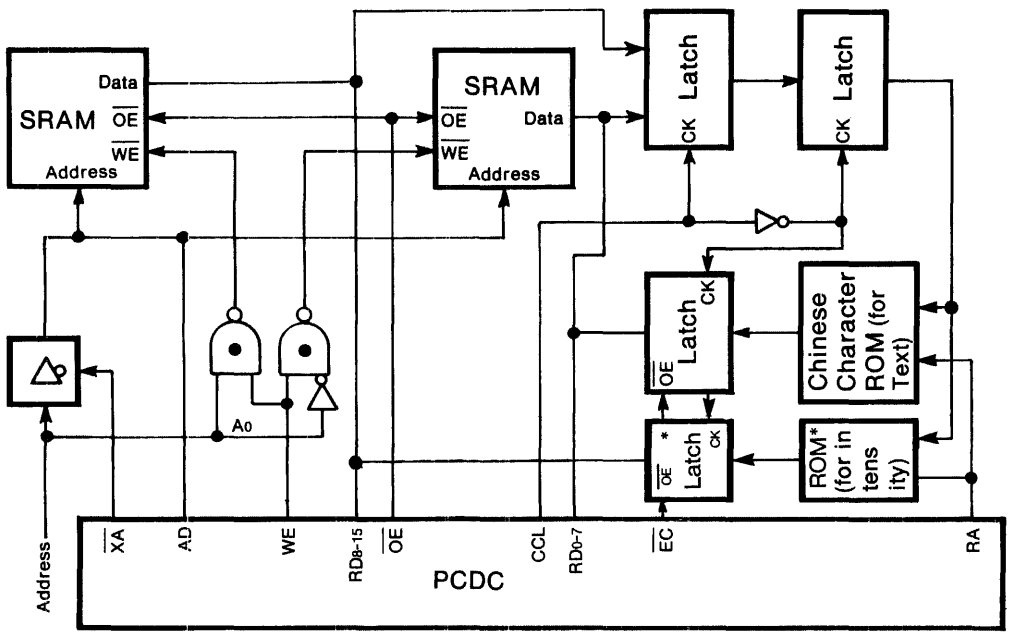
As shown in the above diagram, the ESIO = 1 setting is required for the HGC Full mode (For ones with other modes, the initial hardware setting is acceptable). In the case of the Half mode, adapt the $\overline{\text{ESY}}$ terminals for the 9 font input to enable for the initial hardware setting (Since the DC output from the character Font ROM will be connected to the $\overline{\text{ESY}}$terminals, the bit used for AND and LATCH are not necessary. Refer to the PCDC board diagram in 10-2 for details.).



The above configuration also permits display in the expanded Graphics Modes (except 4 Byte Graphics Mode).
In case only graphics will be displayed, the Latch and Character Font ROM can be omitted.
Since DRAMs are being used, the CGA Mode or a 16-bit bus configuration is also possible.

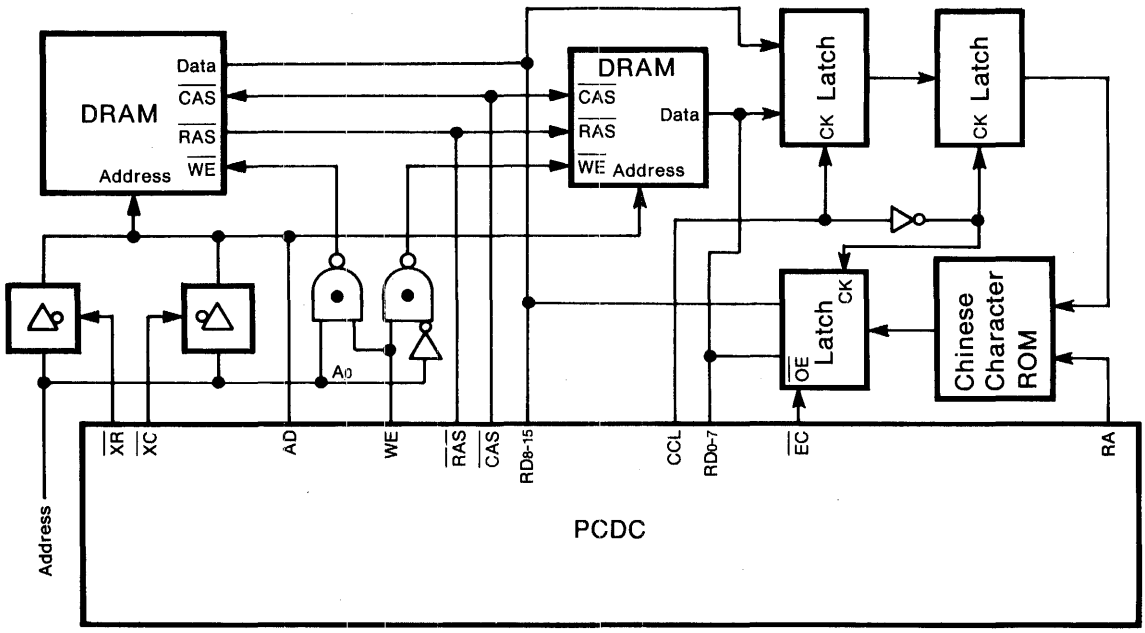
7-3. KANJI DISPLAY

7-3-1. For 8 x n (FON = 101)



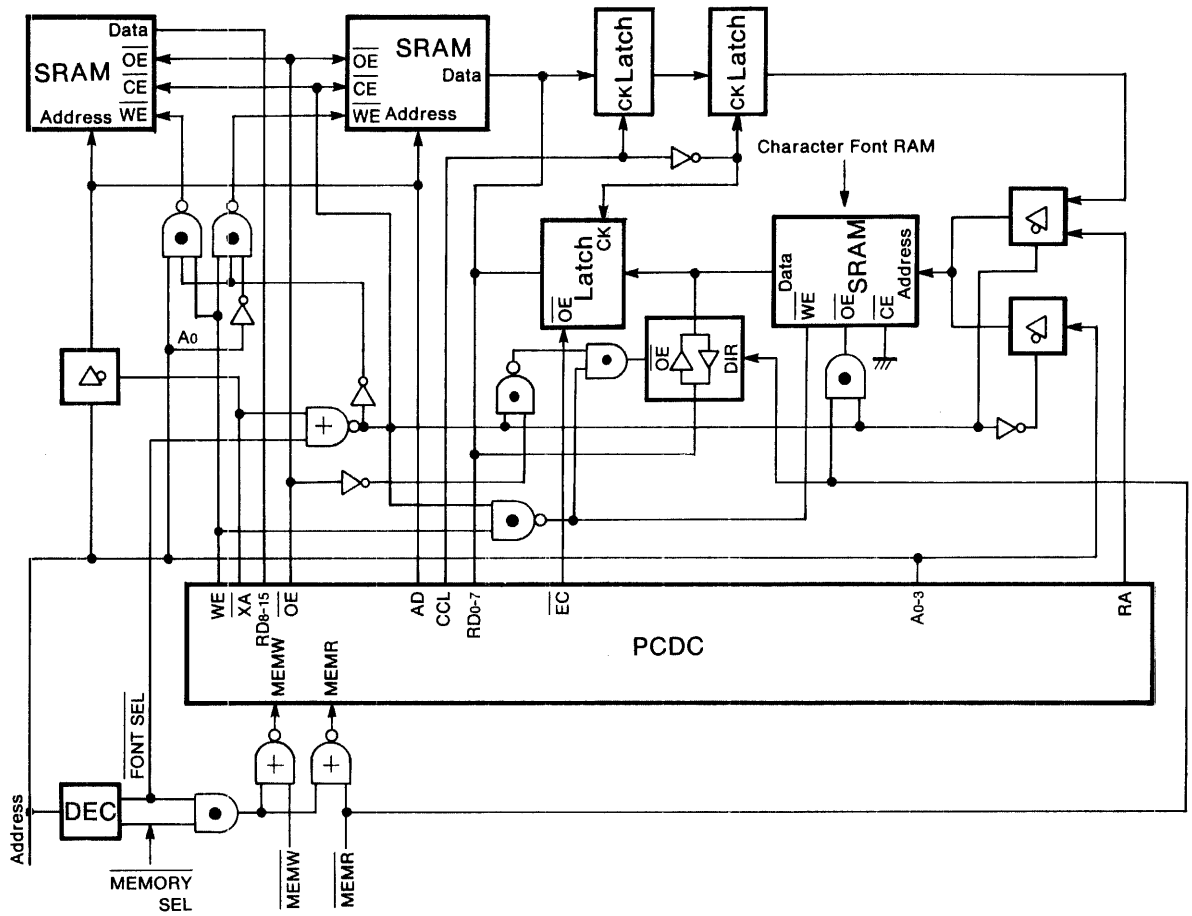
DRAMs can also be substituted.
Kanji cannot be displayed using an 8-bit bus configuration.
The Latch marked with an asterisk and the ROM (for intensity) are required only for controlling Intensity after setting GRM1 = '1'.

7-3-2. For 16 x n (FON = 110)



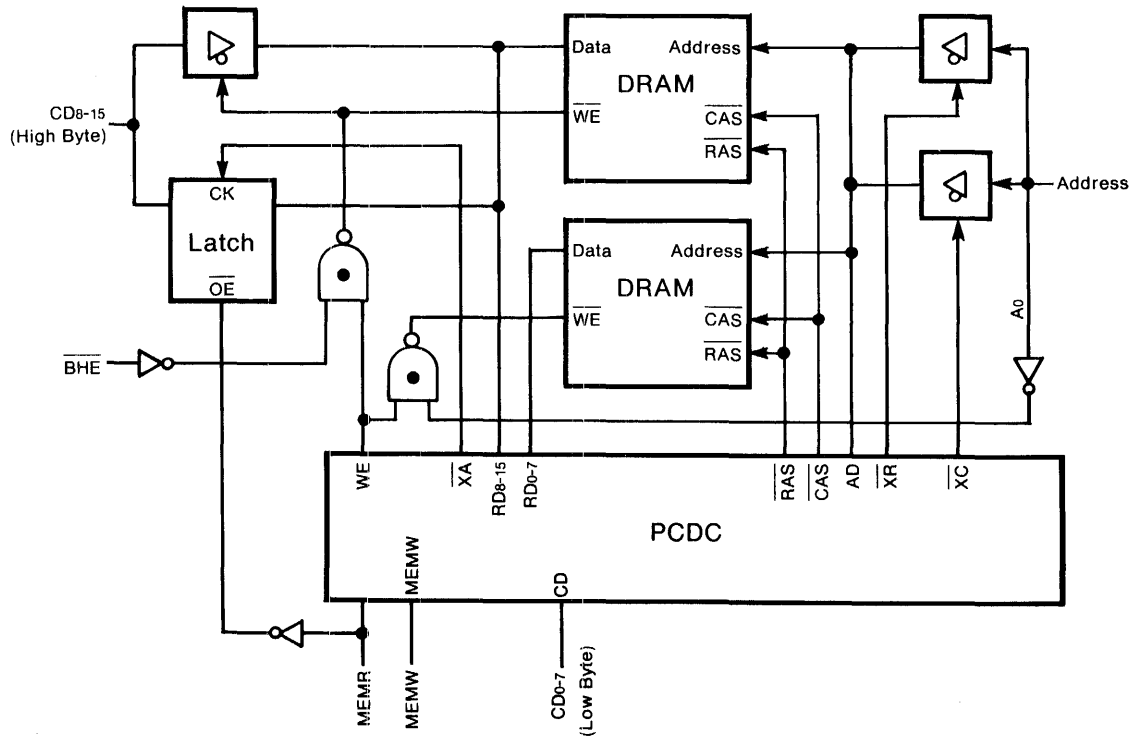
SRAMs can also be substituted.
In Interlace Mode, the RA4 pin is connected to the lowest-order address of ROM. Because an signal inverted at every field will be output from the RA4 pin (set RA4 = R/M = '1'), the kanji will be displayed by interpolation of the even and odd fields.

7-4. USE OF A CHARACTER FONT RAM



DRAMs can also be used as VRAM. (Only SRAM can be used for the Character Font RAM.)

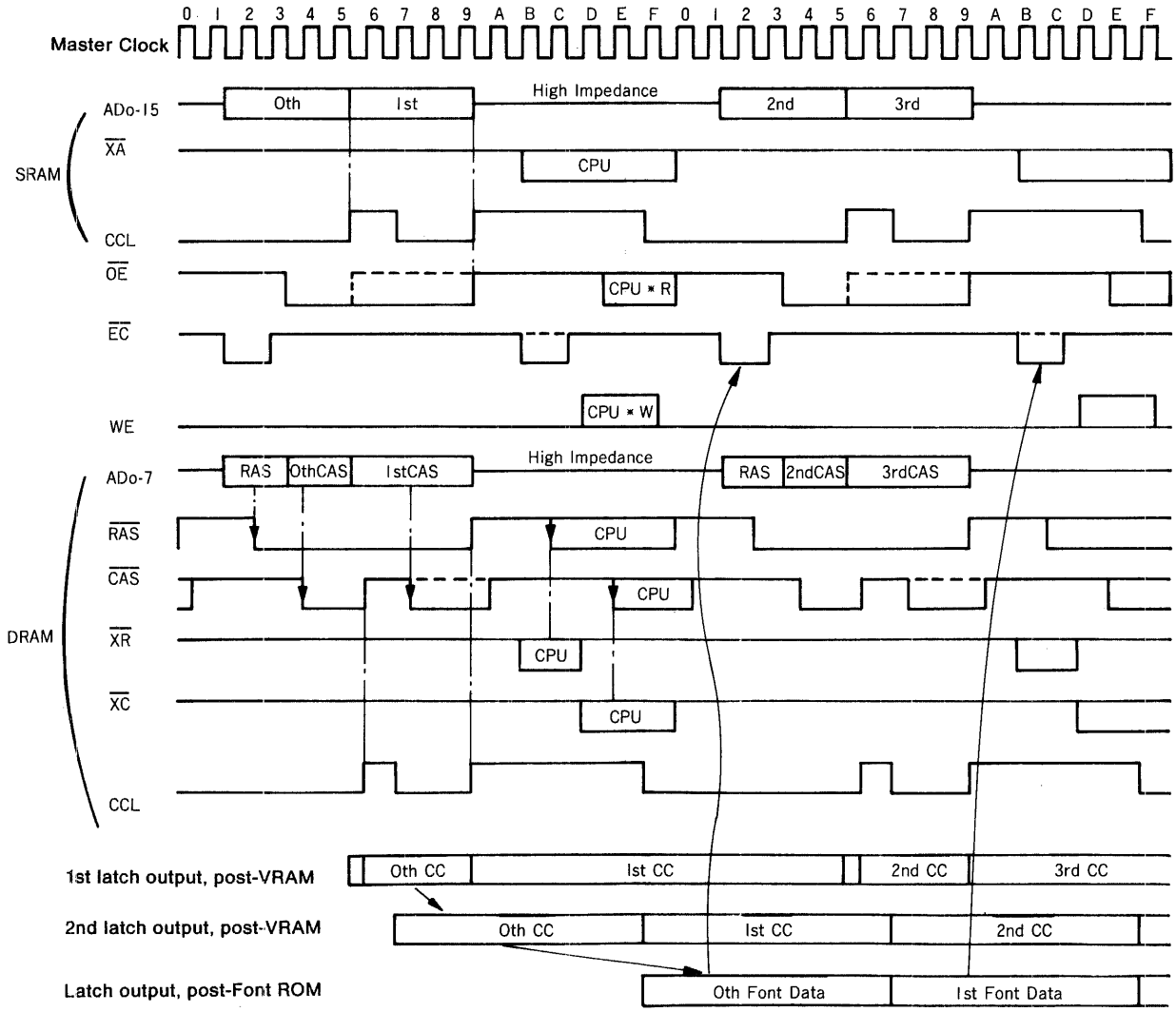
7-5. USE OF A 16-BIT BUS CPU



SRAMs can also be substituted. Alphanumerical or Chinese character display is possible.

7-6. OPERATING TIMING

7-6-1. 16-Bit Bus Configuration

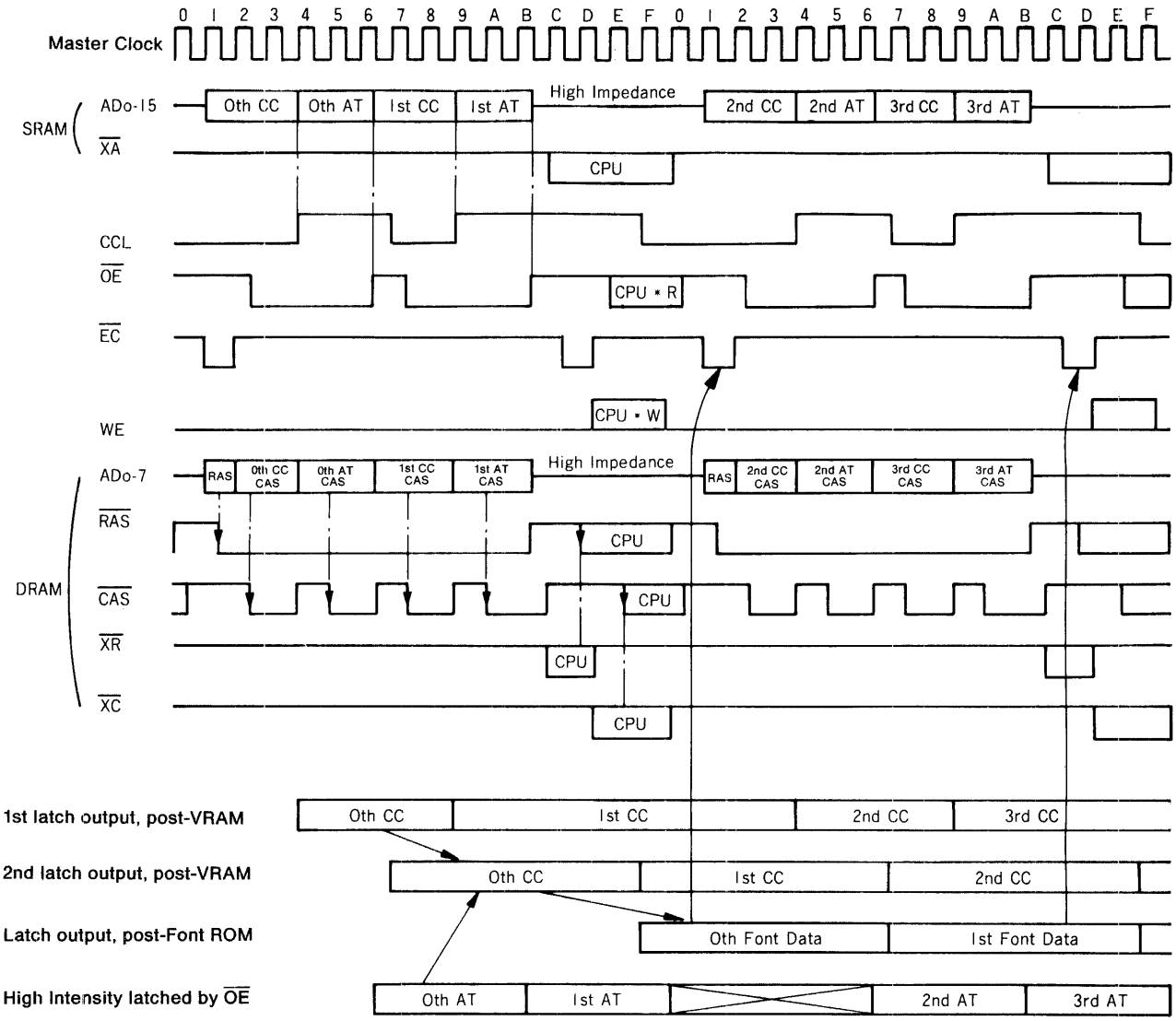


The above figure shows the timing of the various signals in High Resolution Text Mode (in case the horizontal font size is 8 PELs). The Character Codes are latched by an external circuit at the rising edge of CCL, then are latched again at the falling edge of CCL in order to provide leeway in the access time of the Font ROM. After the data from the Font ROM is latched at the falling edge of CCL, it is input to PCDC by $\overline{EC}$ via the RD bus.
The Attribute data is directly input to PCDC. (A lag occured between the timing of the Attribute and Font data is internally adjusted at PCDC.)

In case of performing display by switching the Font ROM addresses in accordance with different Intensity value in the Attribute Code (for example, when normally using a Single PEL Font, but

switching to a Double PEL Font in High Intensity Mode to achieve a Bold effect), increase the quantity of bits for the 1st and 2nd Latches to allow latching of the High Intensity value. (Since the Character Code and Attribute Code are simultaneously accessed due to the 16-bit bus configuration of VRAM, latching can be easily performed.) In Low Resolution Text Mode, the 0th and 1st address (as well as the 2nd and 3rd addresses) will be identical, and $\overline{OE}$, $\overline{EC}$, and $\overline{CAS}$ will change as depicted by the broken-line status in the preceding figure (but the data flow of Text display will be the same as that in High Resolution Text Mode). In (1 Byte) Graphics Mode, the timing of the various signals will be the same as that in Low Resolution Text Mode, but all display data will be directly input to PCDC from the RD bus.

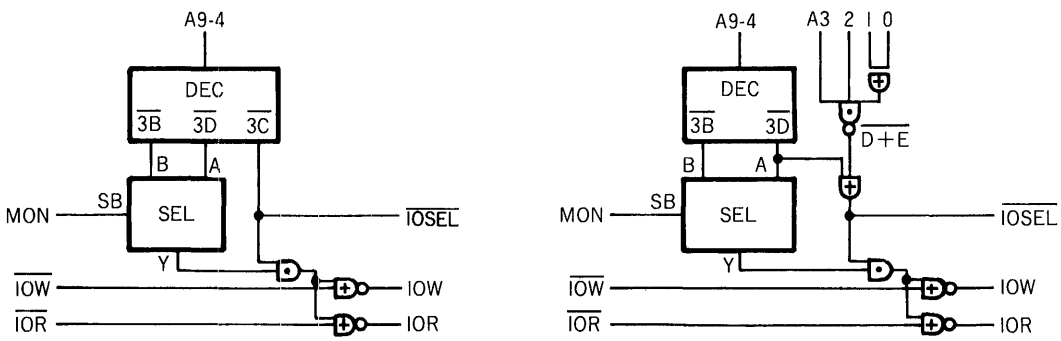
7-6-2. 8-Bit Bus Configuration



The above figure shows the timing of the various signals in High Resolution Text Mode (in case the horizontal font size is 8 PELs). The data flow is identical that for the 16-bit bus configuration, but the Character Codes and Attribute Codes are alternately accessed with an 8-bit bus configuration. For this reason, in achieve use a Bold effect, the High Intensity value in the Attribute Code must be latched at the rising edge of $\overline{OE}$, latched again at the falling edge of CCL, then supplied to the Font ROM addresses.

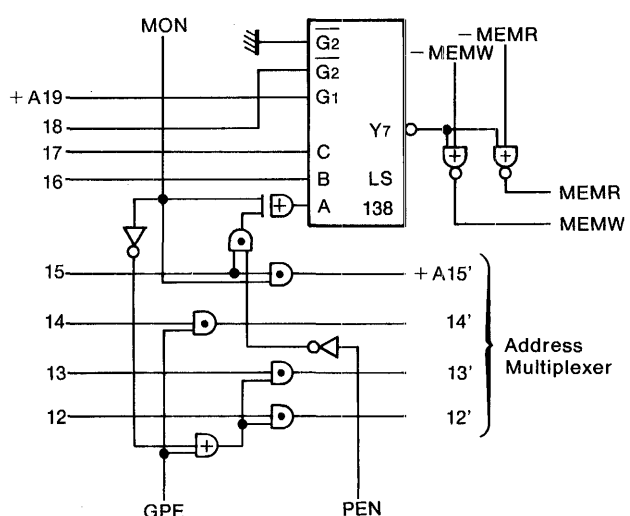
7-7. OTHER PRECAUTIONS

Be sure that any unnecessary input pins of PCDC are pulled up or down in order to conserve power dissipation and to prevent destruction by static electricity. For the same reason, also be sure that any unnecessary I/O pins are pulled up or down. (In the sense of preventing a short-circuited current after Power Start-Up until the input/output have settled, do not directly connect to the power supply or GND, but pull it up or down via a resistor of about 10 Kohms.)
The Register Bank, which hold the expanded functions beyond the IBM PC, are protected using a double-protection feature. If Bit 7 (Protect) of the Control Register will not be set to '1' using commercially available software, IOSEL will become unnecessary. In that case, IOSEL either should be pulled down to '0' level or can be used by direct coupling with the decode output (3BH or 3DH) for the I/O registers. (In the circuit example shown in CHAPTER 10, "PCDC EVALUATION BOARD," IOSEL is directly coupled with the decode output.) In cases where it is possible to set Protect to '1', protection must be provided using IOSEL and two methods may be considered. One method sets IOSEL to a decode value that is different from the I/O registers. When set to 3CH, for example, the circuit will be as shown at the below left:



The other method utilizes the fact that the I/O Registers D and E are unused in CGA Mode and employs the same I/O ports as those of CGA for writing to the Register Bank, even with an MDA or HGC. A sample circuit for this method is shown at the above right. The MON signal therein is used by CGA, MDA, and HGC for switching the decode values for the I/O registers.

The PCDC outputs GPE (see the description on A15 on page 3-6-12) and PEN (see the description on PEN output on page 3-6-15) as the Control signals for HGC. An example of the use of these signals is shown in the below figure (for full Hercules compatibility).



GPE is made to correspond to the 4K byte capacity of VRAM under MDA and is ANDed with A12 to A14. In case pages or graphics will be used with HGC, however, GPE will become '1' so that A12 to A14 will be enabled. In CGA mode, A12 and A13 are constantly being used. Therefore, when MON = '0' (for use with CGA), the OR operation on GPE and MON will cause the AND circuit to operate simply as a buffer.

In Hercules PAGE mode, PEN is used in the case where the values of the memory map will be decoded as B0000 to BFFFF. When PEN = '0', the memory map values of HGC will be decoded as B0000 to B7FFF. When PCDC will be used in CGA mode, PEN will constantly equal '0' and the memory map values will be decoded as B8000 to BFFFF.

8. ELECTRICAL CHARACTERISTICS

8-1. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit
Supply voltage	V_{DD}	−0.3	+7.0	V
Input voltage	V_I	−0.3	V_{DD}+0.3	V
Output voltage	V_O	−0.3	V_{DD}+0.3	V
Operating temperature	T_{OP}	0	+70	°C
Storage temperature	T_{STG}	−50	+125	°C

(Based on the reference voltage of V_{SS} = 0.0V)

8-2. RECOMMENDED CONDITIONS FOR USE

Supply voltage: +5V ± 5% (based on V_{SS} = 0.0V)
Operating temperature: 0-70 °C

8-3. DC CHARACTERISTICS (V_{DD} = 5V ± 5%, Top = 0-70 °C)

Item	Symbol	Condition	Min.	Max.	Unit
High-level output voltage (for TTL driving)	V_{OH}	I_{OH} = −0.4mA	2.7		V
Low-level output voltage (for TTL driving)	V_{OL}	I_{OL} = 0.8mA		0.4	V
High-level output voltage (for CMOS driving)	V_{OH}	$\|I_{OH}\| < 10\mu A$	V_{DD} − 0.4		V
Low-level output voltage (for CMOS driving)	V_{OL}	$\|I_{OL}\| < 10\mu A$		0.4	V
High-level input voltage	V_{IH}		2.2		V
Low-level input voltage	V_{IL}			0.8	V
Input leak current	I_L		−10	10	μA
OFF status leak current	I_{LZ}		−10	10	μA
Power current (during normal operation)	I_{DD}			70	mA
Power current (during Standby)	I_{DD}			10	mA

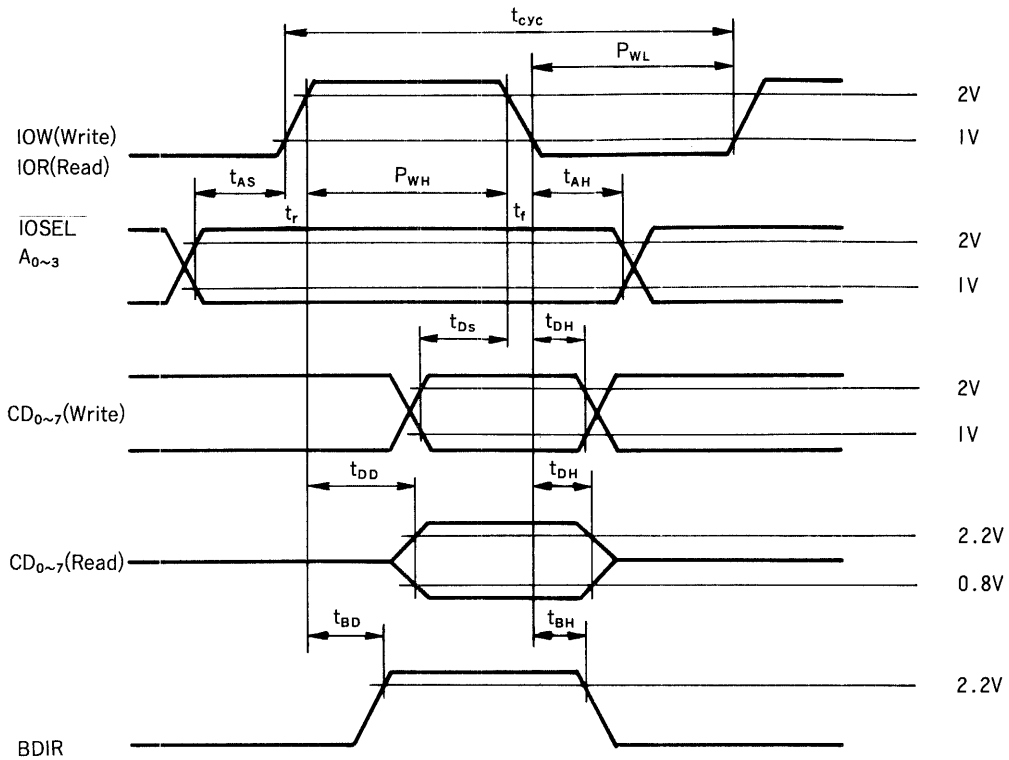
NOTE:

ILZ applies while the CD0-CD7, RD0-RD15, X2, RA4, or $\overline{ESY}$ pins are in input status or while the AD0/$\overline{XR}$-AD15/GPE or MEMRDY pins are in high-impedance status.

8-4. AC CHARACTERISTICS (V_{DD} = 5V ± 5%, Top = 0-70 °C)

8-4-1. I/O Registers-CPU Interface (@C_L = 100pF + 2LSTTL (CD_0-CD_7, BDIR))

Item	Symbol	Min.	Max.	Unit
Cycle time	t_{CYC}	300		ns
Read/Write pulse width	PW_L,PW_H	120		ns
Read/Write rise/fall time	t_r,t_f		25	ns
Address set-up time	t_{AS}	40		ns
Address hold time	t_{AH}	10		ns
Data set-up time	t_{DS}	60		ns
Data hold time	t_{DH}	10		ns
Data delay time	t_{DD}		100	ns
Hold time for bus-direction switching	t_{BH}	10		ns
Delay time for bus-direction switching	t_{BD}		80	ns

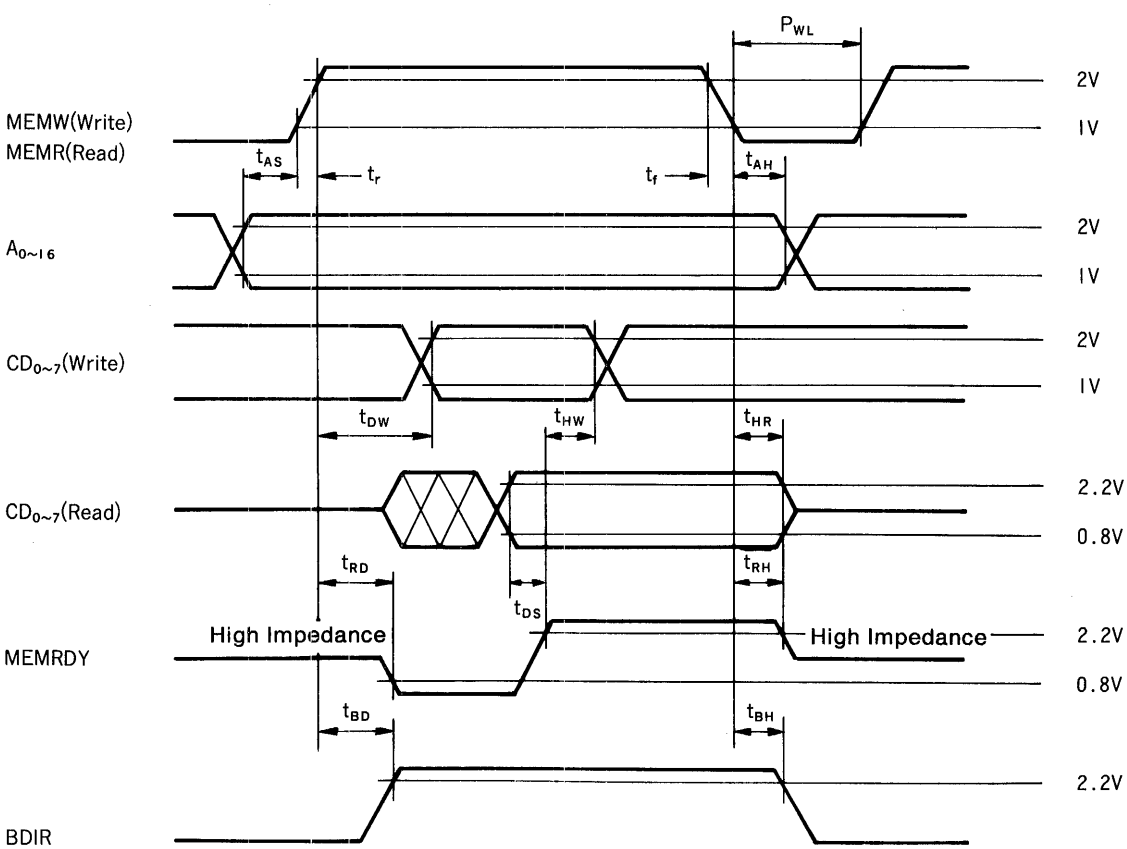


8-4-2. VRAM-CPU Interface (@C_L = 100pF + 2LSTTL (CD_0-CD_7, BDIR, MEMRDY))

Item	Symbol	Min.	Max.	Unit
Read/Write low-level pulse width	P_{WL}	50		ns
Read/Write rise/fall times	t_r,t_f		25	ns
Address set-up time	t_{AS}	0		ns
Address hold time	t_{AH}	0		ns
Data delay time (during Write)	t_{DW}		350	ns
Data hold time (during Write)	t_{HW}	0		ns
Data set-up time (during Read)	t_{DS}	0		ns
Data hold time (during Read)	t_{HR}	10		ns
Delay time for bus-direction switching	t_{BD}		80	ns
Hold time for bus-direction switching	t_{BH}	10		ns
MEMRDY low-level delay time	t_{RD}		80	ns
MEMRDY high-level hold time	t_{RH}	10		ns

NOTE:

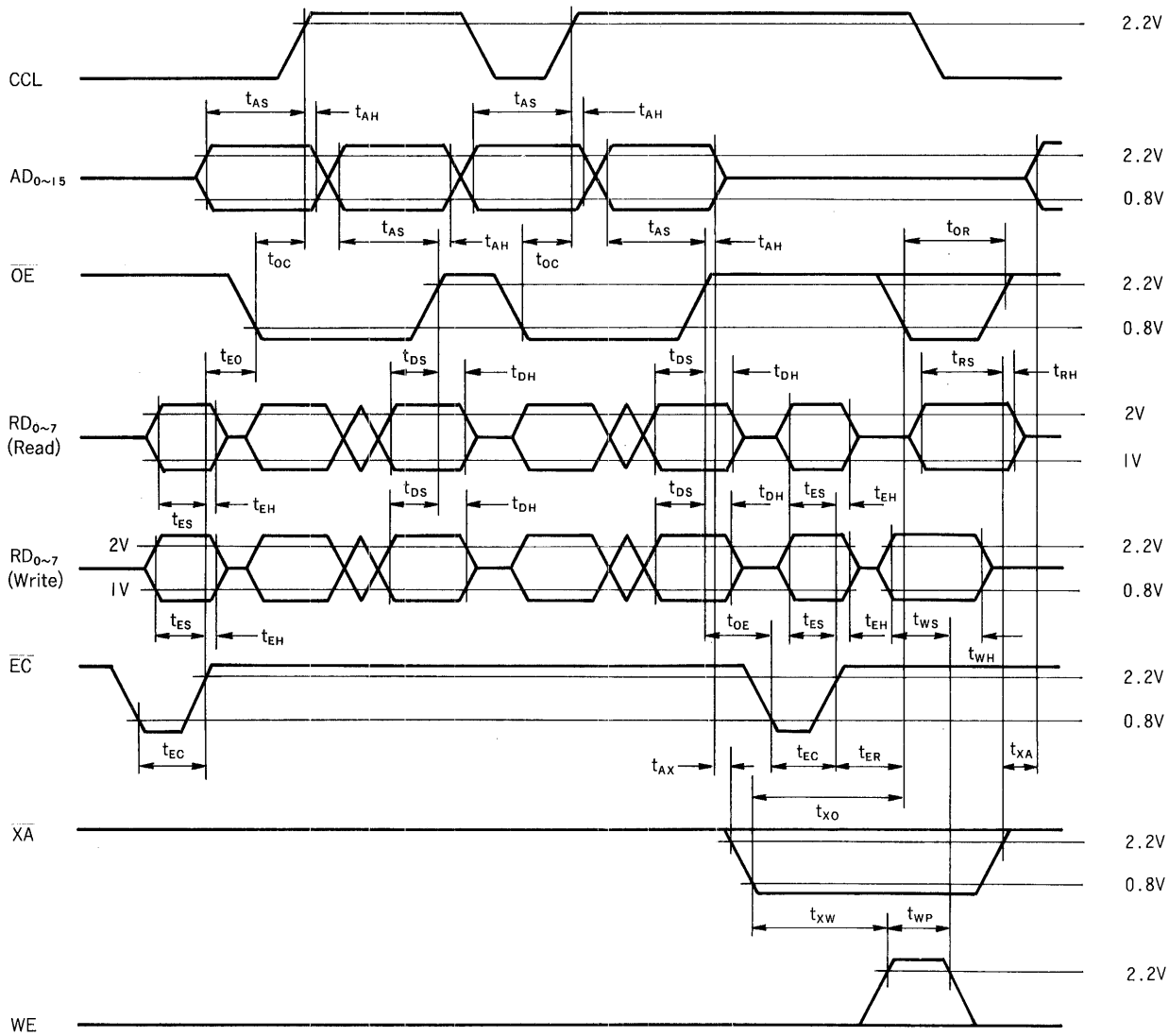
When SCT = 1, the maximum value of t_{DW} will be 3 x CK (3.5 x CK when the VRAM is of a 16 bit bus configuration) and the minimum value of t_{DS} be −0.5 x CK (MEMRDY output will be advanced). CK indicates synchronization of the Master Clock.



8-4-3. VRAM-PCDC Interface

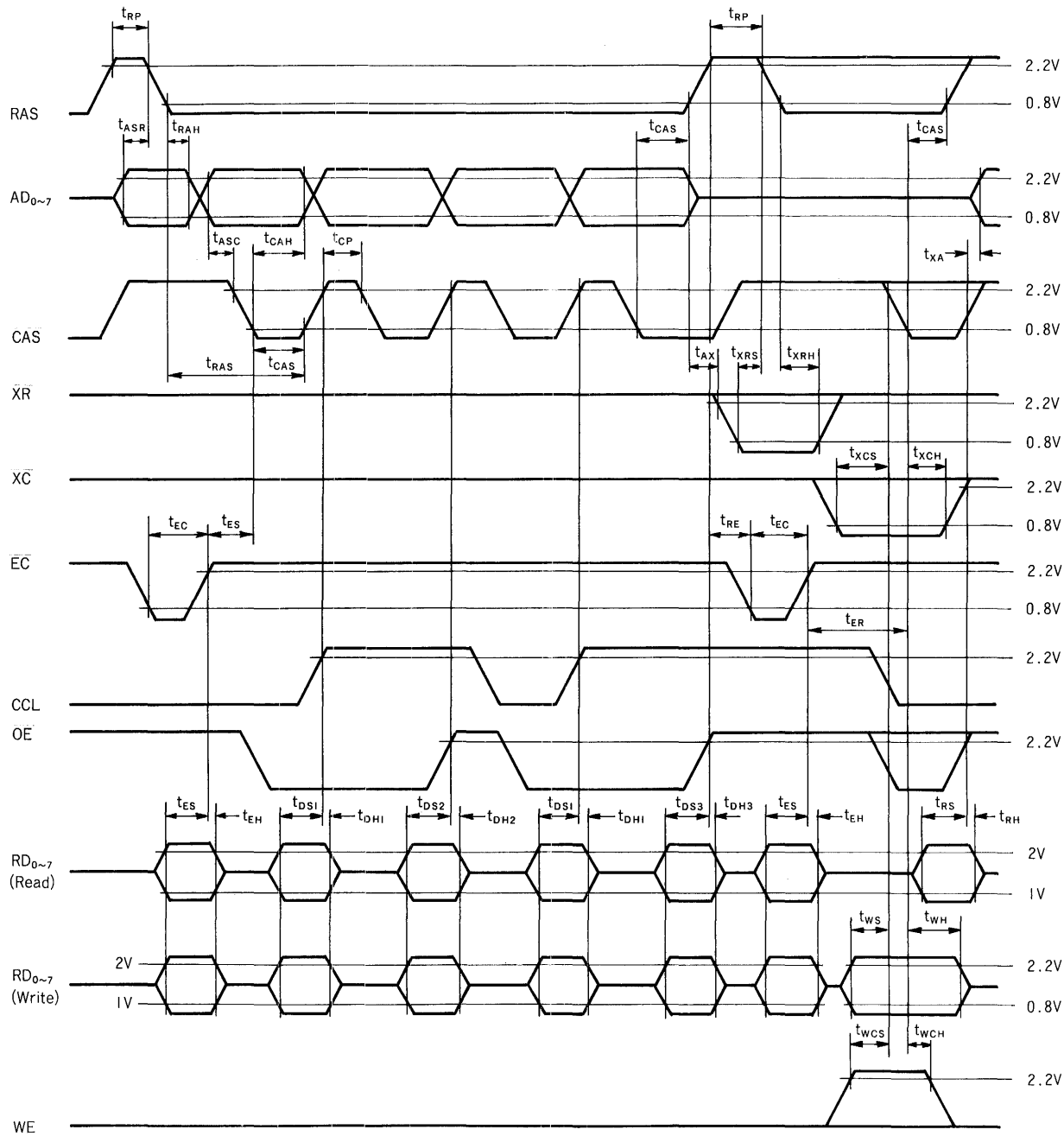
8-4-3-1. 8-Bit Bus in SRAM Mode (@fMaster Clock = 16.257 MHz, CL = 100pF + 2LSTTL)

Item	Symbol	Min.	Typ.	Max.	Unit
CCL,$\overline{OE}$-Address set-up time	t_{AS}	140	150		ns
CCL,$\overline{OEodd}$ -Address hold time	t_{AH}	0			ns
$\overline{OE}$-Data set-up time	t_{DS}	20			ns
$\overline{OE}$-Data hold time	t_{DH}	10			ns
$\overline{EC}$-Data set-up time	t_{ES}	30			ns
$\overline{EC}$-Data hold time	t_{EH}	0			ns
$\overline{EC}$ pulse width	t_{EC}	60			ns
$\overline{OE}$-CCL delay time	t_{OC}	85	92		ns
$\overline{EC}$-$\overline{OE}$ delay time	t_{EO}	20	30		ns
$\overline{OE}$-$\overline{EC}$ delay time	t_{OE}	40	60		ns
$\overline{XA}$-$\overline{OE}$ delay time (during Read)	t_{XO}	130	150		ns
$\overline{EC}$-$\overline{OE}$ delay time (during Read)	t_{ER}	40	60		ns
$\overline{OE}$ pulse width (during Read)	t_{OR}	85	92		ns
$\overline{XA}$-Data set-up time (during Read)	t_{RS}	25			ns
$\overline{XA}$-Data hold time (during Read)	t_{RH}	10			ns
WE-Data set-up time (during Write)	t_{WS}	85			ns
WE-Data hold time (during Write)	t_{WH}	20			ns
WE pulse width (during Write)	t_{WP}	100	120		ns
$\overline{XA}$-WE delay time (during Write)	t_{XW}	85	92		ns
Address Disable-$\overline{XA}$ delay time	t_{AX}	0	30		ns
$\overline{XA}$-Address Enable delay time	t_{XA}	40	60		ns


CCL
AD0~15
OE
RD0~7 (Read)
RD0~7 (Write)
EC
XA
WE
2.2V
0.8V
2V
1V
tAS
tAH
tOC
tOR
tEO
tDS
tDH
tRS
tRH
tES
tEH
tOE
tWS
tWH
tEC
tER
tAX
tXA
tXO
tXW
tWP

8-4-3-2. 8-Bit Bus in DRAM Mode (@fMaster Clock = 16.257 MHz, C_L = 100pF + 2LSTTL)

Item	Symbol	Min.	Typ.	Max.	Unit
Row address set-up time	t_{ASR}	0	25		ns
Row address hold time	t_{RAH}	20	30		ns
Column address set-up time	t_{ASC}	0	25		ns
Column address hold time	t_{CAH}	60	85		ns
$\overline{RAS}$ precharge time	t_{RP}	90			ns
$\overline{CAS}$ precharge time	t_{CP}	60			ns
$\overline{RAS}$ pulse width	t_{RAS}	140			ns
$\overline{CAS}$ pulse width	t_{CAS}	80			ns
Address Disable-$\overline{XR}$ delay time	t_{AX}	0	30		ns
$\overline{XC}$-Address Enable delay time	t_{XA}	40	60		ns
$\overline{XR}$-$\overline{RAS}$ set-up time	t_{XRS}	40	60		ns
$\overline{XR}$-$\overline{RAS}$ hold time	t_{XRH}	20	30		ns
$\overline{XC}$-$\overline{CAS}$ set-up time	t_{XCS}	40	60		ns
$\overline{XC}$-$\overline{CAS}$ hold time	t_{XCH}	60	85		ns
CCL,$\overline{CAS}$-Data set-up time	t_{DS1}	20			ns
CCL,$\overline{CAS}$-Data hold time	t_{DH1}	10			ns
$\overline{OE}$,$\overline{CAS}$-Data set-up time	t_{DS2}	20			ns
$\overline{OE}$,$\overline{CAS}$-Data hold time	t_{DH2}	10			ns
$\overline{OE}$,$\overline{RAS}$-Data set-up time	t_{DS3}	20			ns
$\overline{OE}$,$\overline{RAS}$-Data hold time	t_{DH3}	10			ns
$\overline{EC}$-Data set-up time	t_{ES}	30			ns
$\overline{EC}$-Data hold time	t_{EH}	0			ns
$\overline{EC}$ pulse width	t_{EC}	60			ns
$\overline{EC}$-$\overline{CAS}$ delay time	t_{ES}	20	30		ns
$\overline{RAS}$-$\overline{EC}$ delay time	t_{RE}	40	60		ns
$\overline{EC}$-$\overline{CAS}$ delay time (during Read)	t_{ER}	40	60		ns
$\overline{XC}$-Data set-up time (during Read)	t_{RS}	25			ns
$\overline{XC}$-Data hold time (during Read)	t_{RH}	10			ns
$\overline{CAS}$-Data set-up time (during Write)	t_{WS}	20	30		ns
$\overline{CAS}$-Data hold time (during Write)	t_{WH}	60	85		ns
WE-$\overline{CAS}$ set-up time (during Write)	t_{WCS}	40	60		ns
WE-$\overline{CAS}$ hold time (during Write)	t_{WCH}	40	60		ns

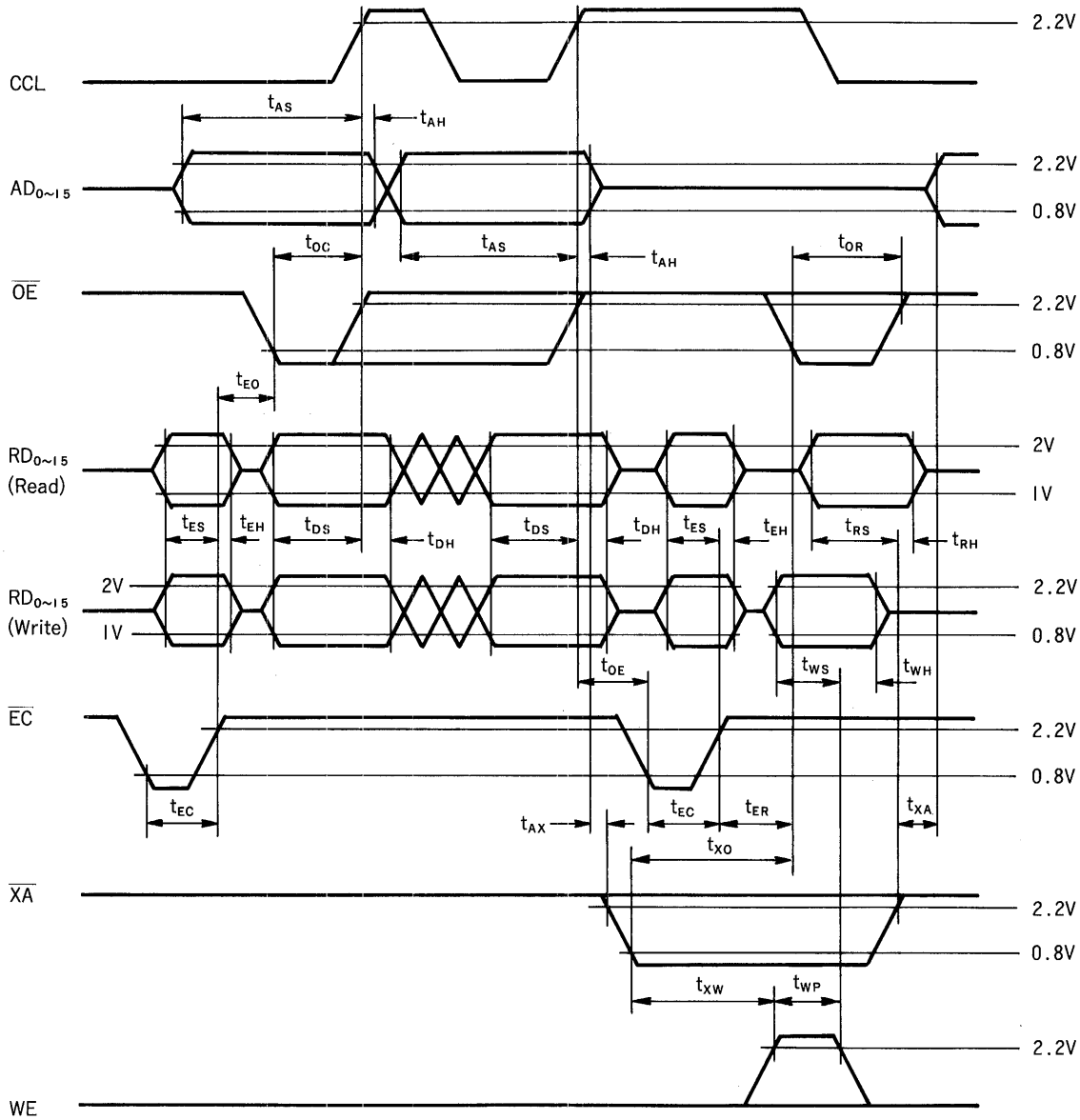

RAS
AD0~7
CAS
XR
XC
EC
CCL
OE
RD0~7 (Read)
RD0~7 (Write)
WE
tRP
tRP
tASR
tRAH
tCAS
tCAS
tASC
tCAH
tCP
tXA
tRAS
tCAS
tAX
tXRS
tXRH
tXCS
tXCH
tEC
tES
tRE
tEC
tER
tES
tEH
tDS1
tDH1
tDS2
tDH2
tDS1
tDH1
tDS3
tDH3
tES
tEH
tRS
tRH
tWS
tWH
tWCS
tWCH
2.2V
0.8V
2V
1V

8-4-3-3. 16-Bit Bus in SRAM Mode (@C_L = 100pF + 2LSTTL)

Item	Symbol	Min.	Typ.	Min.	Typ.	Unit
CCL-Address set-up time	t_{AS}	170	180	170	180	ns
CCL-Address hold time	t_{AH}	0		0		ns
CCL-Data set-up time	t_{DS}	20		20		ns
CCL-Data hold time	t_{DH}	10		10		ns
$\overline{EC}$-Data set-up time	t_{ES}	30		30		ns
$\overline{EC}$-Data hold time	t_{EH}	0		0		ns
$\overline{EC}$ pulse width	t_{EC}	55		55		ns
$\overline{OE}$-CCL delay time	t_{OC}	80	90	85	92	ns
$\overline{EC}$-$\overline{OE}$ delay time	t_{EO}	10	20	20	30	ns
$\overline{OE}$-$\overline{EC}$ delay time	t_{OE}	40	65	40	60	ns
$\overline{XA}$-$\overline{OE}$ delay time (during Read)	t_{XO}	120	130	130	150	ns
$\overline{EC}$-$\overline{OE}$ delay time (during Read)	t_{ER}	40	65	85	92	ns
$\overline{OE}$ pulse width (during Read)	t_{OR}	80	90	85	92	ns
$\overline{XA}$-Data set-up time (during Read)	t_{RS}	25		25		ns
$\overline{XA}$-Data hold time (during Read)	t_{RH}	10		10		ns
WE-Data set-up time (during Write)	t_{WS}	80		85		ns
WE-Data hold time (during Write)	t_{WH}	15		20		ns
WE pulse width (during Write)	t_{WP}	100	110	100	120	ns
$\overline{XA}$-WE delay time (during Write)	t_{XW}	80	90	85	92	ns
Address Disable-$\overline{XA}$ delay time	t_{AX}	40	65	40	60	ns
$\overline{XA}$-Address Enable delay time	t_{XA}	40	65	40	60	ns

Horizontal PEL quantity = 8-10
fMaster Clock = 22.4 MHz

Horizontal PEL quantity = 6, 7, 4 Byte Graphics Mode, or 4 Byte Kanji Mode
fMaster Clock = 16.257 MHz

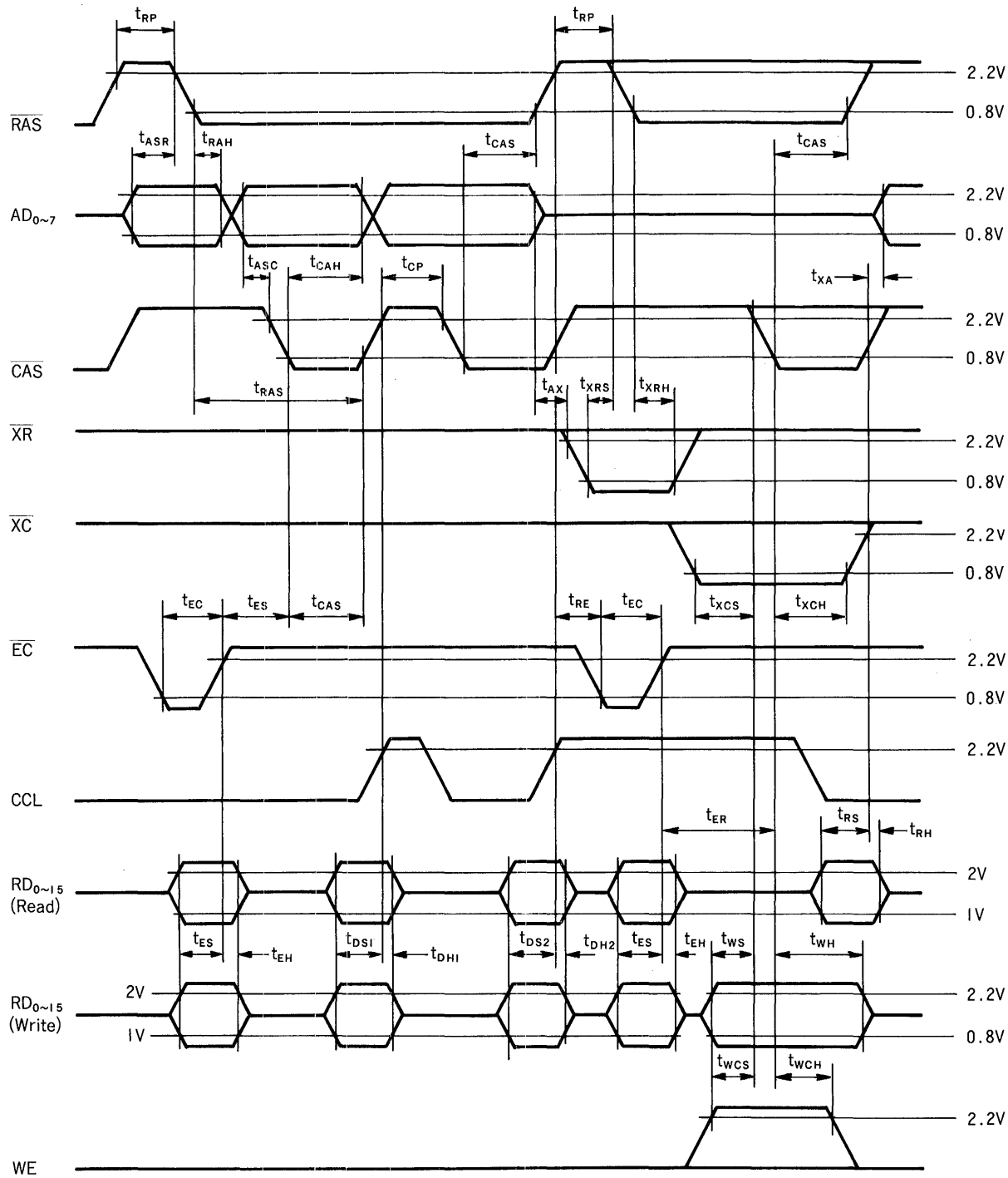

CCL
AD0~15
OE
RD0~15 (Read)
RD0~15 (Write)
EC
XA
WE
2.2V
0.8V
2V
1V
tAS
tAH
tOC
tOR
tEO
tES
tEH
tDS
tDH
tRS
tRH
tOE
tWS
tWH
tEC
tER
tAX
tXA
tXO
tXW
tWP

8-4-3-4. 16-Bit Bus in DRAM Mode (@CL = 100pF + 2LSTTL)

Item	Symbol	Min.	Typ.	Min.	Typ.	Unit
Row address set-up time	t_{ASR}	20	40	40	60	ns
Row address hold time	t_{RAH}	20	40	20	30	ns
Column address set-up time	t_{ASC}	0	20	20	30	ns
Column address hold time	t_{CAH}	40	65	40	60	ns
$\overline{RAS}$ precharge time	t_{RP}	100		100		ns
$\overline{CAS}$ precharge time	t_{CP}	60		60		ns
$\overline{RAS}$ pulse width	t_{RAS}	140		140		ns
$\overline{CAS}$ pulse width	t_{CAS}	80		80		ns
Address Disable-$\overline{XR}$ delay time	t_{AX}	40	65	40	60	ns
$\overline{XC}$-Address Enable delay time	t_{XA}	40	60	40	60	ns
$\overline{XR}$-$\overline{RAS}$ set-up time	t_{XRS}	25	40	40	60	ns
$\overline{XR}$-$\overline{RAS}$ hold time	t_{XRH}	25	40	20	30	ns
$\overline{XC}$-$\overline{CAS}$ set-up time	t_{XCS}	25	40	40	60	ns
$\overline{XC}$-$\overline{CAS}$ hold time	t_{XCH}	60	90	85	92	ns
CCL,$\overline{CAS}$-Data set-up time	t_{DS1}	20		20		ns
CCL,$\overline{CAS}$-Data hold time	t_{DH1}	10		10		ns
CCL,$\overline{RAS}$-Data set-up time	t_{DS2}	20		20		ns
CCL,$\overline{RAS}$-Data hold time	t_{DH2}	10		10		ns
$\overline{EC}$-Data set-up time	t_{ES}	30		30		ns
$\overline{EC}$-Data hold time	t_{EH}	0		0		ns
$\overline{EC}$ pulse width	t_{EC}	55		55		ns
$\overline{EC}$-$\overline{CAS}$ delay time	t_{ES}	25	40	40	60	ns
$\overline{RAS}$-$\overline{EC}$ delay time	t_{RE}	40	65	40	60	ns
$\overline{EC}$-$\overline{CAS}$ delay time (during Read)	t_{ER}	40	65	85	92	ns
$\overline{XC}$-Data set-up time (during Read)	t_{RS}	25		25		ns
$\overline{XC}$-Data hold time (during Read)	t_{RH}	10		10		ns
$\overline{CAS}$-Data set-up time (during Write)	t_{WS}	10	20	20	30	ns
$\overline{CAS}$-Data hold time (during Write)	t_{WH}	60	90	85	92	ns
WE-$\overline{CAS}$ set-up time (during Write)	t_{WCS}	25	40	40	60	ns
WE-$\overline{CAS}$ hold time (during Write)	t_{WCH}	40	65	40	60	ns

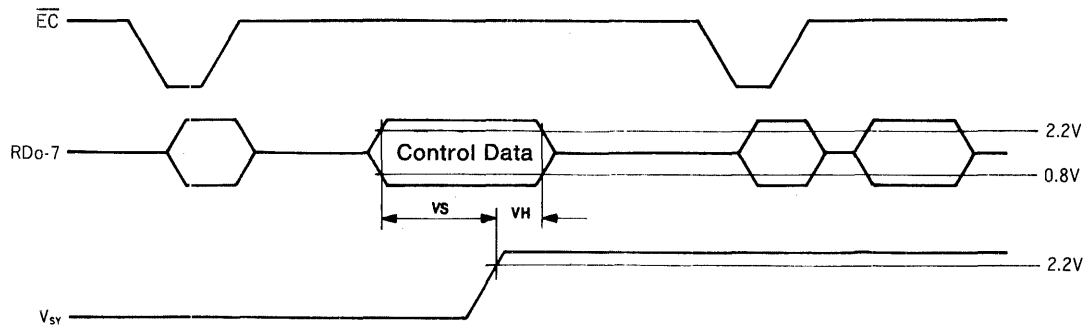
Horizontal PEL quantity = 8-10
fMaster Clock = 22.4 MHz

Horizontal PEL quantity = 6, 7, 4 Byte Graphics Mode, or 4 Byte Kanji Mode
fMaster Clock = 16.257 MHz


t_{RP}
t_{RP}
$\overline{RAS}$
2.2V
0.8V
t_{ASR}
t_{RAH}
t_{CAS}
t_{CAS}
$AD_{0\sim7}$
2.2V
0.8V
t_{ASC}
t_{CAH}
t_{CP}
t_{XA}
$\overline{CAS}$
2.2V
0.8V
t_{RAS}
t_{AX}
t_{XRS}
t_{XRH}
$\overline{XR}$
2.2V
0.8V
$\overline{XC}$
2.2V
0.8V
t_{EC}
t_{ES}
t_{CAS}
t_{RE}
t_{EC}
t_{XCS}
t_{XCH}
$\overline{EC}$
2.2V
0.8V
CCL
2.2V
t_{ER}
t_{RS}
t_{RH}
$RD_{0\sim15}$ (Read)
2V
1V
t_{ES}
t_{EH}
t_{DSI}
t_{DHI}
t_{DS2}
t_{DH2}
t_{ES}
t_{EH}
t_{WS}
t_{WH}
$RD_{0\sim15}$ (Write)
2V
1V
2.2V
0.8V
t_{WCS}
t_{WCH}
WE
2.2V

8-4-4. Control Data Interface (@CL = 100pF + 2LSTTL)

Item	Symbol	Min.	Typ.	Max.	Unit
VSY Data set-up time	VS	100			ns
VSY Data hold time	VH	20			ns



NOTE:

The Control Data is valid when the rising edge of VSY occurs outside the display time (when it occurs during the horizontal/vertical retrace line time). In such a case, which includes the Control Data output time, the $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ pins will go high.

8-4-5. Monitor Interface

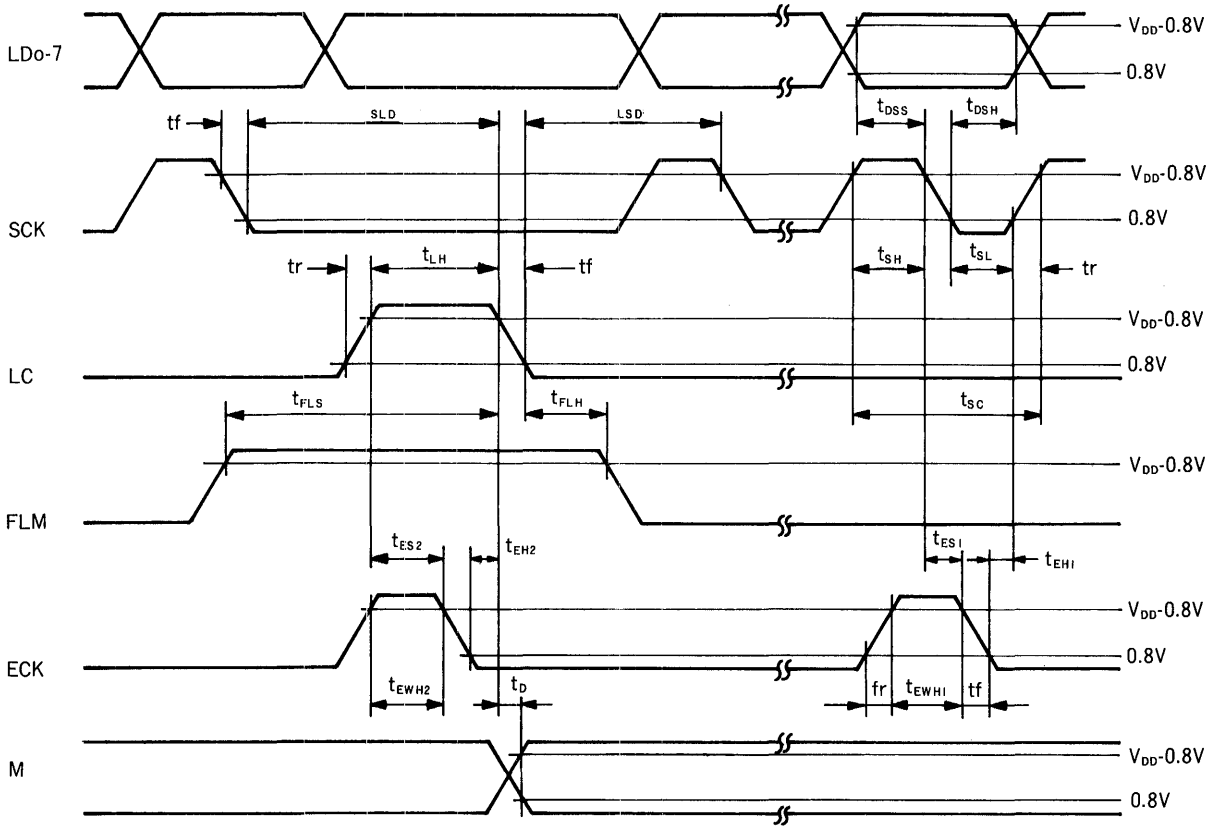
PCDC is capable of a diversity of interfacing methods for various monitors due to its setting of the Register Bank. The examples introduced for reference herein describe the LCD and CRT.

8-4-5-1. LCD (@CL = 100pF (Capacitive load only))

Item	Symbol	Min.	Typ.	Max.	Unit
FLM-LC set-up time	tFLS	1			µs
FLM-LC hold time	tFLH	1			µs
LC high-level pulse width	tLH		8xCK		ns
LC-SCK delay time	tLSD	0.6			µs
SCK-LC delay time	tSLD	0.4			µs
DATA-SCK set-up time	tDSS		tsc/2		ns
DATA-SCK hold time	tDSH		tsc/2		ns
LC, SCK, ECK rise/fall times	tr, tf			30	ns
SCK pulse width	tSH, tSL		Tsc/2		ns
SCK cycle time	tsc		tsc		ns
ECK set-up time-1	tES1		2xCK		ns
ELK hold time-1	tEH1		tsc/2-2xCK		ns
ELK high-level pulse width-1	tEWH1		tsc/2		ns
ECK set-up time-2	tES2		4xCK		ns
ECK hold time-2	tEH2		4xCK		ns
ECK high-level pulse width-2	tEWH2		4xCK		ns
M delay time	tD			30	ns

NOTES:

1. CK represents the Master Clock cycles.
2. The SCK cycle time (tsc) is the product of the quantity of data transmission bits times CK. With 2 Bit Even/Odd, for example, tsc = 2 x CK. Since tsc will be doubled for a two- screen LCD (dual-drive type). For 4Bit Parallel, for example, tsc = 2 x 4 x CK = 8 x CK.
3. ECK becomes valid during 4Bit Parallel Mode.
4. Values listing only a Typical value with no Min. value, should be considered as follows: Typ. – 30 ns = Min.

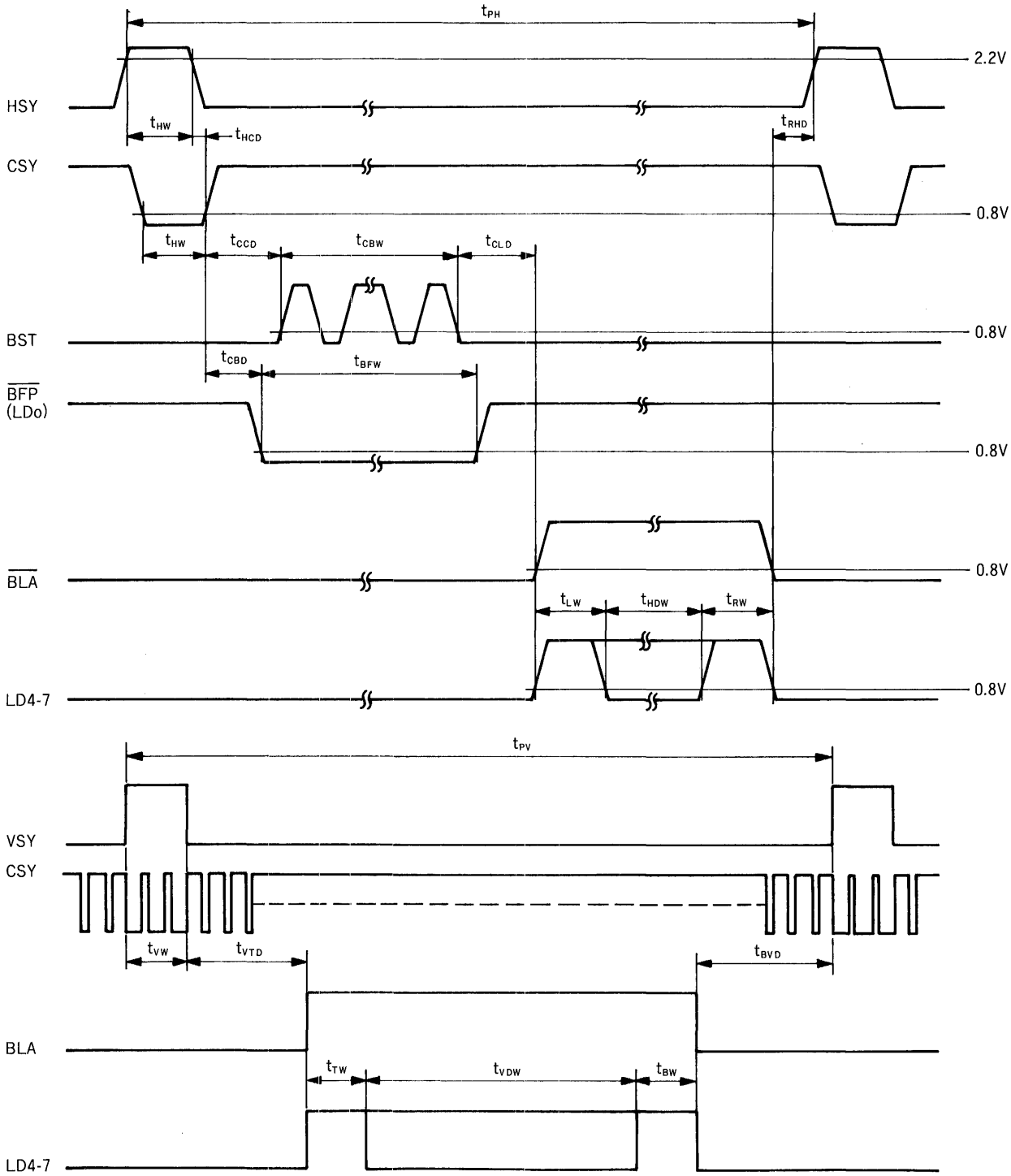


8-4-5-2. CRT (@fMaster Clock = 14.318 MHz, C_L = 100pF + 2LSTTL)

Item	Symbol	Min.	Typ.	Max.	Unit
HSY pulse width	t_{HW}		4.47		µs
HSY-CSY delay time	t_{HCD}		0.56		µs
CSY-Color Burst delay time	t_{CCD}		0.7		µs
CSY-$\overline{BFP}$ delay time	t_{CBD}		1.19		µs
$\overline{BFP}$ time width	t_{BFW}		2.23		µs
Color Burst time width	t_{CBW}		2.1		µs
Color Burst-Left Border delay time	t_{CLD}		1.4		µs
Left Border time width	t_{LW}		2.5		µs
Right Border time width	t_{RW}		5.3		µs
Right Border-Hsy delay time	t_{RHD}		1.96		µs
Vertical displayed time width	t_{HDW}		44.7		µs
Vsy-Top Border delay time	t_{VTD}		773		µs
Top Border time width	t_{TW}		1.53		ms
Bottom Border time width	t_{BW}		1.4		ms
Bottom Border-Vsy delay time	t_{BVD}		55		µs
Horizontal displayed time width	t_{VDW}		12.74		ms
Hsy cycle	t_{PH}		63.7		µs
Vsy cycle	t_{PV}		16.69		ms
Vsy pulse width	t_{VW}		191		µs
Output rise/fall times	tr, tf			30	ns

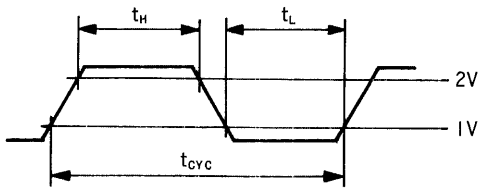
NOTE:

The above timing applies to the case where the CGA-Standard values have been set at the 6845 registers. (See subsection 3-1-18, "Sample Setting Values using IBM PC")


tPH
2.2V
HSY
tHW
tHCD
tRHD
CSY
0.8V
tHW
tCCD
tCBW
tCLD
BST
0.8V
tCBD
tBFW
BFP
(LDo)
0.8V
BLA
0.8V
tLW
tHDW
tRW
LD4-7
0.8V
tPV
VSY
CSY
tVW
tVTD
tBVD
BLA
tTW
tVDW
tBW
LD4-7

8-4-6. External Clock

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency-1	t_{C1}	1		16.35	MHZ
Clock frequency-2	t_{C2}	1		22.5	MHZ
Clock duty	Duty	40	50	60	%



$$Duty = \frac{t_H}{t_{CYC}} \text{ or } \frac{t_L}{t_{CYC}}$$

NOTE:

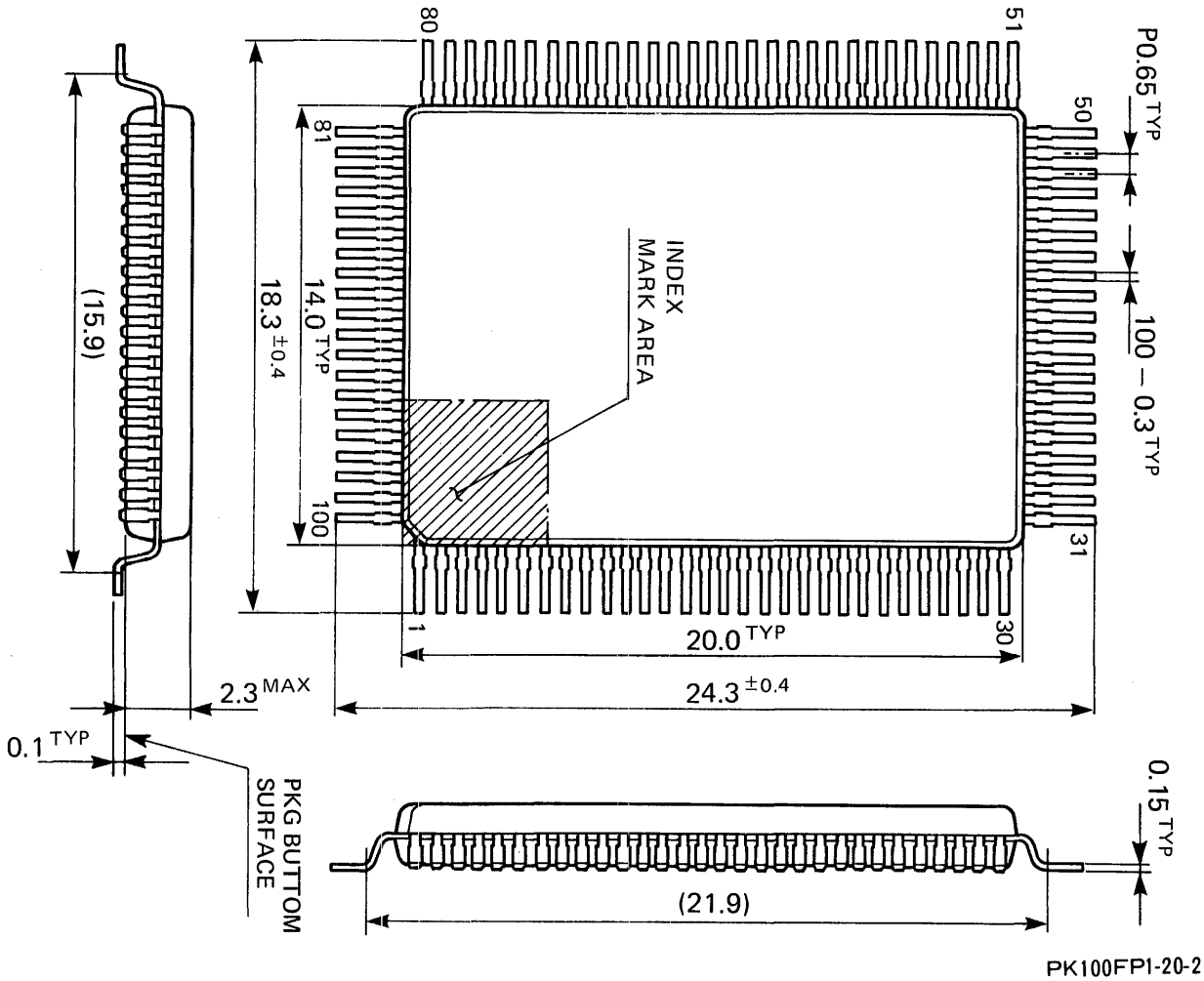
An external clock of "clock frequency - 1" will apply in cases where the VRAM data bus has a 16-bit bus configuration with a horizontal font size of 6, 7 PELs or in 4 Byte Graphics Mode or 4 Byte Kanji Mode, or in cases where the VRAM data bus has an 8-bit bus configuration. "Clock frequency - 2" will apply in all other cases when the VRAM data bus has a 16-bit bus configuration.

8-4-7. Terminal Capacity

Item	Symbol	Condition	Min.	Max.	Unit
Input terminal	C_I			8	PF
Output terminal	C_O	No load		10	PF
Input/Output terminals	$C_{I/O}$	No load		12	PF
Output load capacity	C_L			100	PF

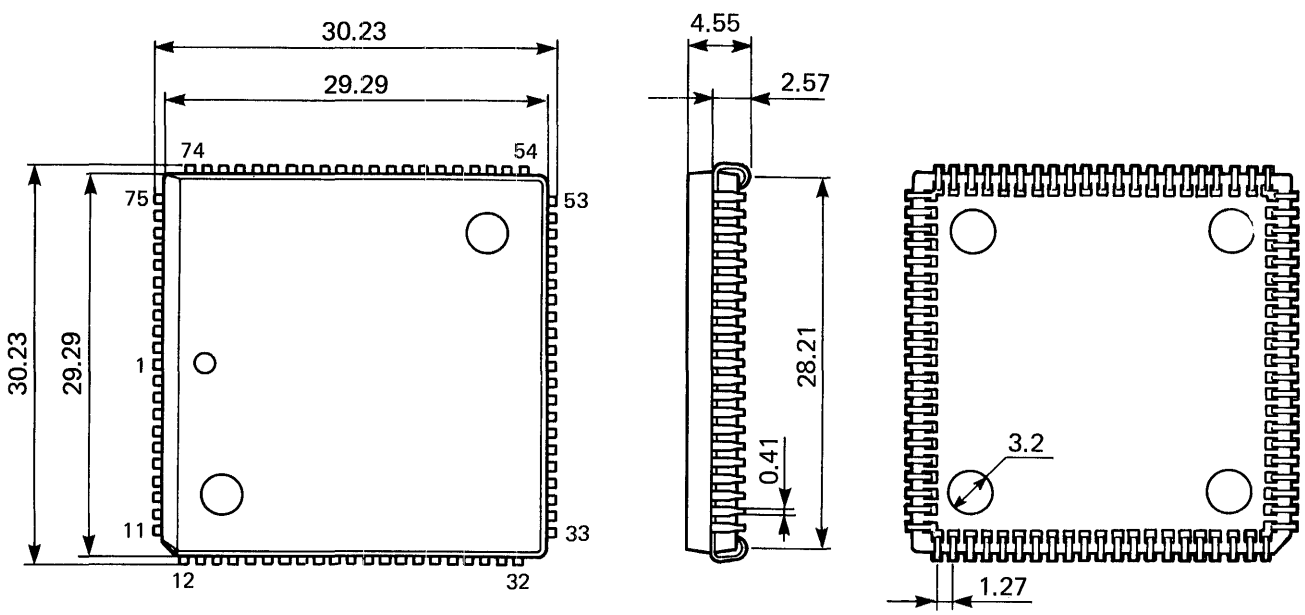
9. PACKAGE OUTLINES

9-1. 100-PIN QFP



PK100FP1-20-2

9-2. 84-PIN PLCC



PK84JP1-00-1

10. PCDC EVALUATION BOARD

This chapter describes the Graphics Board which was designed for evaluation of PCDC and is compatible with CGA, MDA, and HGC for the IBM PC. The main specifications of this Graphics Board are as follows:

VRAM Used: One 256K SRAM with a 32k byte x 8 bit configuration

VRAM Data Bus: 8-bit bus configuration

Connectable Monitors: IBM color/monochrome monitor, EGA monitor, NTSC-Standard composite input CRT, and various Panels (LCD, Plasma Display, EL)

Fonts Used: 8 by 8 PELs (Double PEL Font) or 8 by 14 PELs

Light Pen Connection: Possible

Printer Interface: None

A switch (SW3) is provided for enabling selection of the default status after Power Start-Up as CGA, MDA or HGC. In case of a standard combination of software and a monitor, therefore, initialization by software becomes unnecessary. (The VRAM type and data bus configuration are also initialized by hardware according to the level of $\overline{\text{LDT}}$ pin and $\overline{\text{LSW}}$ pin at RESET, which are set to "1" by pull-up resistors. After resetting, the clock input terminals function as X_1 terminals — input 16.257 μHz to these terminals in the case of MDA and HGC.) SW1 is used for switching the higher-address decode values for the I/O registers and memory into values for use by CGA, MDA or HGC. SW2 is used for font selection.

A 640 by 400 PEL LCD, plasma display or EL will require a power supply other than +5V and -12V (such as −25V, +200V, +15V, +30V, etc.), so connect such voltages directly to the Panel from the outside of the board.

10-1. LIST OF CONNECTORS

IBM System Expansion Slots

Pin	Name	Name	Pin
A 1		GND	B 1
A 2	+D7	+RESET	B 2
A 3	+D6	+5V	B 3
A 4	+D5		B 4
A 5	+D4		B 5
A 6	+D3		B 6
A 7	+D2	−12V	B 7
A 8	+D1		B 8
A 9	+D0	+12V	B 9
A 10	+I/O CHRDY	GND	B 10
A 11	+AEN	−MEMW	B 11
A 12	+A 19	−MEMR	B 12
A 13	+A 18	−IOW	B 13
A 14	+A 17	−IOR	B 14
A 15	+A 16		B 15
A 16	+A 15		B 16
A 17	+A 14		B 17
A 18	+A 13		B 18
A 19	+A 12		B 19
A 20	+A 11		B 20
A 21	+A 10		B 21
A 22	+A 9		B 22
A 23	+A 8		B 23
A 24	+A 7		B 24
A 25	+A 6		B 25
A 26	+A 5		B 26
A 27	+A 4		B 27
A 28	+A 3		B 28
A 29	+A 2	+5V	B 29
A 30	+A 1	+OSC	B 30
A 31	+A 0	GND	B 31

NOTE: Except for Panels, all connections have the same pin arrangement as that of the IBM PC.

For the Panel

Pin	Name	Name	Pin
1		GND	16
2	M	GND	17
3	LC	GND	18
4	SCK	GND	19
5	ECK	GND	20
6	LDo	GND	21
7	LD1	GND	22
8	LD2	GND	23
9	LD3	GND	24
10	LD4	GND	25
11	LD5	GND	26
12	LD6	GND	27
13	LD7	GND	28
14	+5V	GND	29
15	FLM	−12V	30

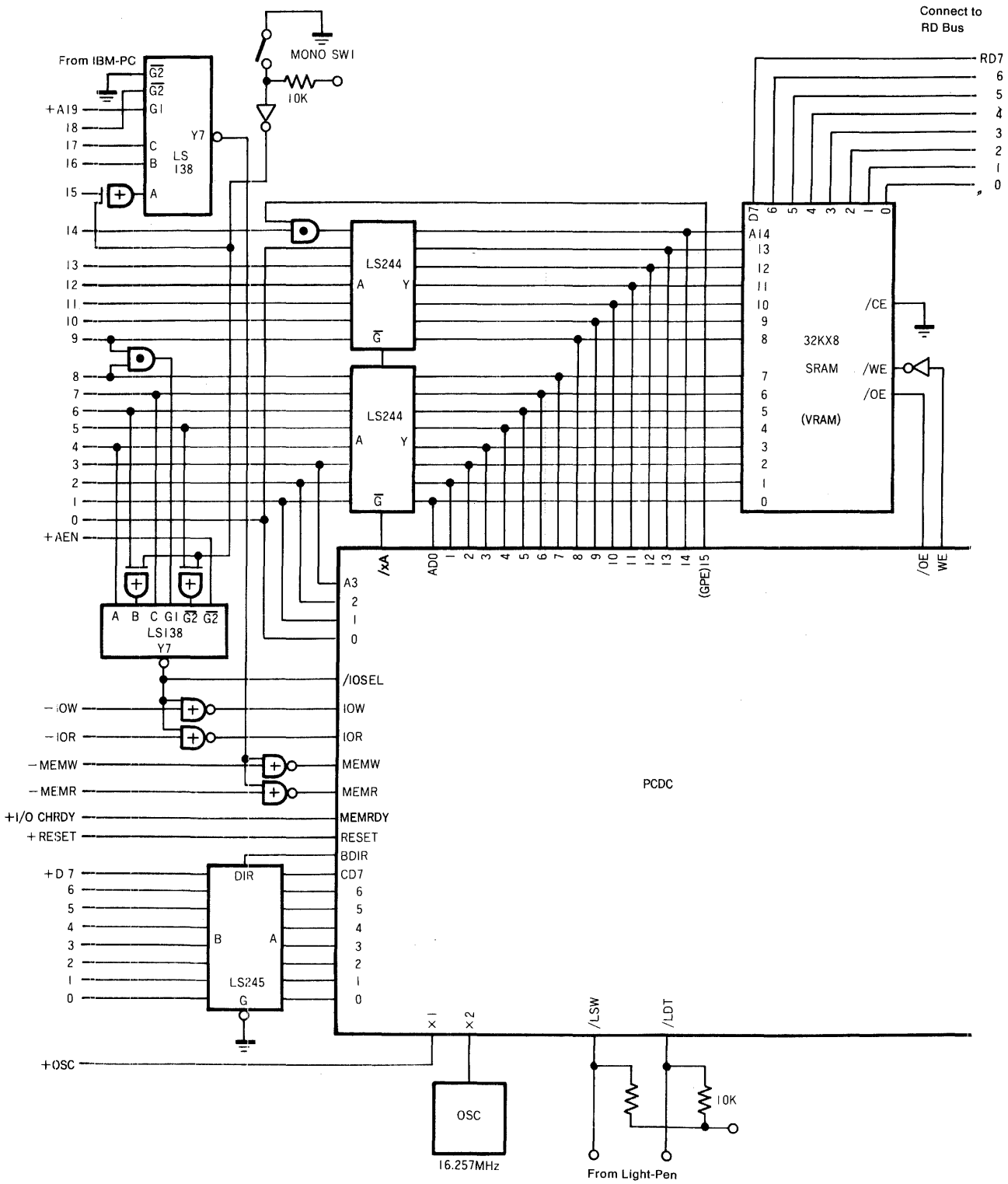
For the IBM Monitor (D-Shell Connector)

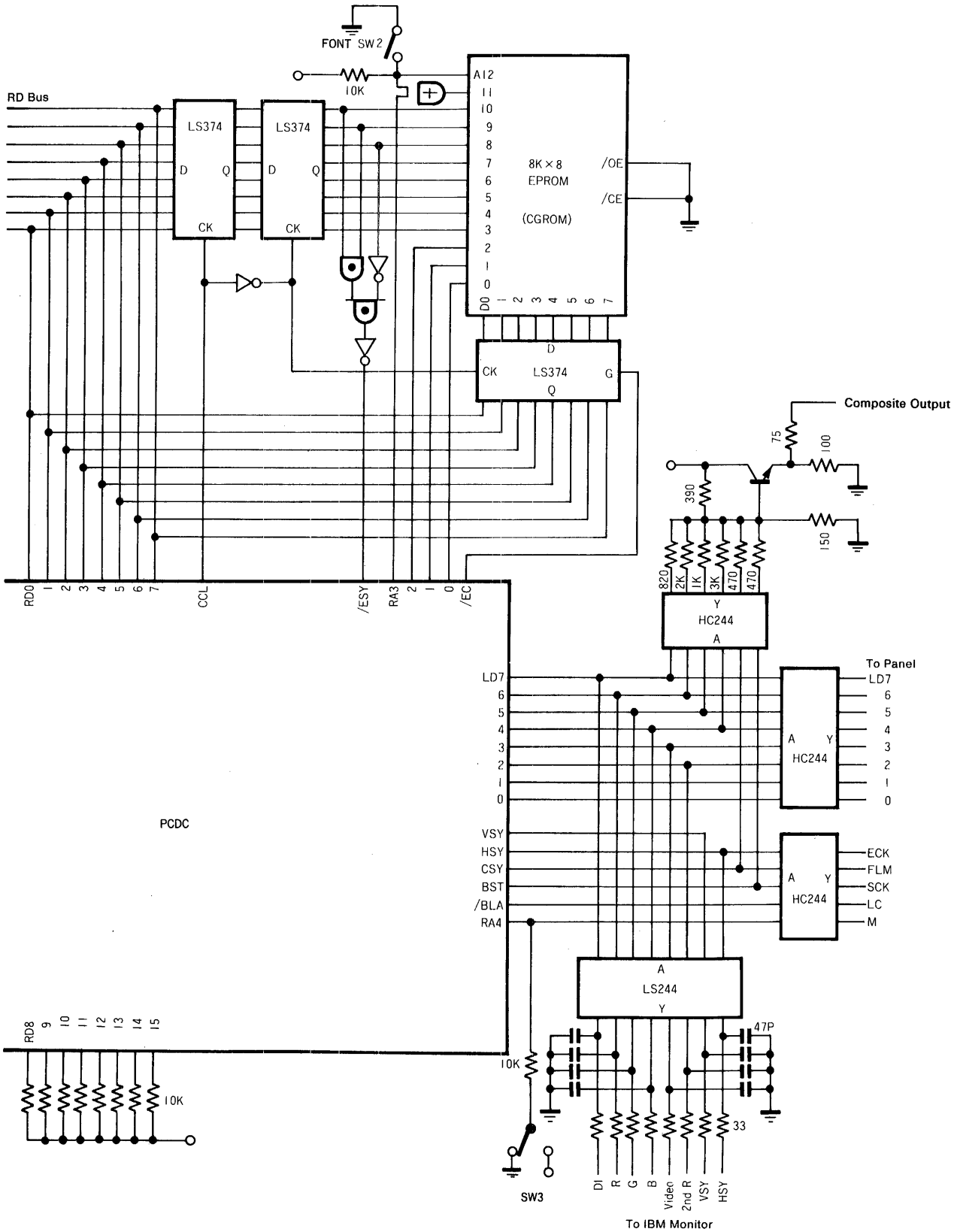
Pin	Name
1	GND
2	2nd R
3	DR
4	DG
5	DB
6	DI
7	Video
8	HSY
9	VSY

For the Light Pen

Pin	Name
1	−Light Pen Input(/LDT)
2	
3	−Light Pen Switch(/LSW)
4	GND
5	+5V
6	+12V

10-2. CIRCUIT DIAGRAMS




FONT SW2
10K
RD Bus
LS374
LS374
D
Q
CK
A12
11
10
9
8
7
6
5
4
3
2
1
0
8K × 8
EPROM
(CGROM)
/OE
/CE
D0
D
CK
LS374
G
Q
Composite Output
75
100
390
150
820
2K
1K
3K
470
470
Y
HC244
A
RD0
CCL
/ESY
RA3
/EC
LD7
6
5
4
3
2
1
0
To Panel
A
Y
HC244
PCDC
VSY
HSY
CSY
BST
/BLA
RA4
ECK
FLM
SCK
LC
M
A
LS244
Y
RD8
9
10
11
12
13
14
15
10K
47P
10K
33
SW3
DI
R
G
B
Video
2nd R
VSY
HSY
To IBM Monitor

10-3. INITIALIZATION SETTINGS

In case the software and monitor used are different from the standard combination, initialization by software will be required after system start-up. (Once initialization has been performed, IBM PC software will be capable of being used as is without requiring any modification.) The initial setting of the Register Bank is achieved using the following procedure. (Any Read/Write operations with respect to VRAM shall be performed after initialization is completed.)

1. Set Bit 7 ($\overline{\text{Protect}}$) of the Control/ID Register to '1'. (Though $\overline{\text{IOSEL}}$ must be set to '0' to enable writing to the Register Bank, because $\overline{\text{IOSEL}}$ is decoded by the PCDC Evaluation Board as 3DH or 3BH, the selection of an I/O register automatically sets $\overline{\text{IOSEL}}$ to '0'.)

2. Set Bit 7 (45S) of the Register Bank Address 3FH to '1' (thereby enabling a negative value to be written in case Vsy. Offset is used).

3. Write the Register Bank's leading address 00H from I/O Register D. (20H is written if the Color Palette will not be used.)

4. Write the data to the Register Bank from I/O Register E. (The addresses of the Register Bank are provided with an Auto Increment function, so the following data will be sequentially written.)

5. After completing the writing of the data required for initialization, set Bit 7 ($\overline{\text{Protect}}$) of the Control/ID Register to '0' (to inhibit any latter attempts to write to the Register Bank).

   The tables of the next two pages show sample initialization settings. (For correspondence with CGA software, IINH is set to '1' to prevent the screen from flashing during scrolling. The Hatching display is set for monitor types having a high display response speed, such as the IBM monochrome monitor, plasma display, and EL panels; Gray Scaling is set for monitor types having a slow display response speed, such as an LCD.)

   The first character of a file name represents the type of software used. (For example, the "C" in "CCOL" signifies software for the Color/Graphics Monitor Adapter, and the "H" of "HMON" signifies software for a Hercules Graphic Card or Monochrome Display Adapter.) The remaining characters represent the type of monitor used.

COL: IBM color monitor or an NTSC-Standard composite input CRT

EGA: IBM EGA monitor

MON: IBM monochrome monitor

LCD4: 640 by 400 PEL LCD (1/200-duty two-screen LCD of single-drive type)
(Seiko Electronics' F642F, etc.)
The numeric values enclosed in parentheses correspond to a 1/200-duty two-screen LCD of dual-drive type.
(Tottori Sanyo Electric's LCM-5213-01A, Seiko Electronics' F642F, etc.)

LCD2: 640 by 200 PEL LCD (1/100-duty two-screen LCD of dual-drive type)
(Optrex's DMF613, Hitachi's LM236SB, Sharp's LM64007G, etc.)

LCD1: 640 by 200 PEL 1/200-duty one-screen LCD
(Hitachi's LM250X, Sharp's LM64012W, etc.)

PLA: 640 by 400 PEL plasma display
(Matsushita Electronics' MD400F640PD2)

EL: 640 by 400 PEL EL panel
(Sharp's LJ640U06).

Conformity to panel specifications will be achieved by using an 18 MHz Master Clock with LCD4 and PLA, and using an 8.5 to 10 MHz Master Clock with LCD2 and LCD1. The 16 bit bus configuration is necessary because the master clock upper limit: 16.35 MHz will be surpassed.
Modification of the initialization settings will enable other LCDs (of 2 Bit Even/Odd type) or plasma displays to be easily connected. And by modifying the Color Palette, a display of the desired Gray Scaling or Hatching patterns can be achieved.

Correspondence with Software for CGA

Bank Address	Bank Data	CCOL	CEGA	CMON	CLCD4	CLCD2	CLCD1	CPLA	CEL
00,01	Color Palette # 0		00,00	00,00	00,00		(00, 00)	00,00	
02,03	Color Palette # 1		00,01	00,00	00,00		(00, 01)	00,00	
04,05	Color Palette # 2		00,02	03,60	02,20		(02, 22)	03,60	
06,07	Color Palette # 3		00,03	03,60	02,20		(02, 23)	03,60	
08,09	Color Palette # 4		00,04	02,60	02,00		(02, 04)	02,60	
0A,0B	Color Palette # 5		00,05	02,60	02,00		(02, 05)	02,60	
0C,0D	Color Palette # 6		00,06	01,00	01,00		(01, 06)	01,00	
0E,0F	Color Palette # 7		00,07	01,00	01,00	←	← (01, 07)	01,00	←
10,11	Color Palette # 8		01,50	04,00	00,00		(00, 10)	00,00	
12,13	Color Palette # 9		01,01	04,00	00,00		(00, 11)	00,00	
14,15	Color Palette # 10		00,12	07,60	02,20		(02, 32)	03,60	
16,17	Color Palette # 11		01,13	07,60	02,20		(02, 33)	03,60	
18,19	Color Palette # 12		00,44	06,60	02,00		(02, 14)	02,60	
1A,1B	Color Palette # 13		01,45	06,60	02,00		(02, 15)	02,60	
1C,1D	Color Palette # 14		00,56	05,00	01,00		(01, 16)	01,00	
1E,1F	Color Palette # 15		01,57	05,00	01,00		(01, 17)	01,00	
20	Duty			00	C7	63 (200L)	00 (100L)	00	00
21	Hsize			00	4F(9F)	9F	4F	4F	4F
22	Vadj			00	0F	07	07 (25)	0E	0F
23	SCT SCU Hadj	00	00	00	01	01	01 (13)	1F	01
24	MON ULE GRM 2 1 0 FON 2 1 0	02	02	03	02	02	02	02	02
25	SYTH HERC SRAM 8BUS 16CP BINH CLK 1 0	30	B5	B5	B1	B0	B0 (30)	31	B1
26	RA4 AI5 EXP PB 1 0 PAG 2 1 0	00	00	00	80	80	80	00	00
27	LS 1 0 IEN EXTS IINH ACM CPLE PRE	08	0B	2B	8B	8B	8B	8B	0B
28	SWC VST SSY SSCK H/E R/M 2SCR 1 0	00	00	01	67(66)	6E	65	C1	11
29	STBY RREG ESIO 4 3 EH 2 1 0	00	00	00	00	13	00	00	00
2A	TST 2 1 0 4 3 SS 2 1 0	00	00	00	00	00	00	00	00
2B	7 6 5 CON 4 3 2 1 0	00	00	00	00	00	00	00	00
30	Horiz. Total		5D	61	55	55	55 (71)	59	53
31	Hsy. Offset		F7	F8	F6(F8)	F8	F6 (00)	DC	F4
32	Vsy. Offset		FD	FD	FD	FD	FD (00)	FD	FD
33	Sync. Width		DA	OF	OA	0A	0A	0A	0A
34	Vert. Total		19	19	19	19	19 (1F)	19	19
35	X X X Vert.Adjust		02	06	00	00	00 (06)	00	00
36	X X X Max.Scan		0D	0D	07	07	07	07	07
37	F/0 TDS 1 0 Cur. Offset	00	1B	1B	60	00	00	60	60
38	Horiz. Total		2E	35	2A	2A	2A (38)	2C	29
39	Hsy. Offset		FB	FF	FB(FC)	FC	FB (00)	EE	FA
3A	Vsy. Offset		F4	FD	F4	F4	F4 (00)	F4	F4
3B	Sync. Width		D5	07	0A	0A	0A	0A	0A
3C	Vert. Total		67	79	67	67	67 (7F)	67	67
3D	X X X Vert.Adjust		02	02	00	00	00 (06)	00	00
3E	X X X Max.Scan		01	01	01	01	01	01	01
3F	45S GDS 1 0 UL.Position	07	4C	2C	67	07	07	67	67

Correspondence with Software for MDA and HGC

Bank Address	Bank Data	HMON	HEGA	HCOL	HLCD4	HLCD2	HLCD1	HPLA	HEL
00,01	Color Palette # 0		00,00		00,00			00,00	
02,03	Color Palette # 1		00,01		00,00			00,00	
04,05	Color Palette # 2		00,02		00,00			00,00	
06,07	Color Palette # 3		00,03		00,00			00,00	
08,09	Color Palette # 4		00,04		00,00			00,00	
0A,0B	Color Palette # 5		00,05		00,00			00,00	
0C,0D	Color Palette # 6		00,06		00,00			00,00	
0E,0F	Color Palette # 7		00,07		01,00	←	←	01,00	←
10,11	Color Palette # 8		01,50		00,00			00,00	
12,13	Color Palette # 9		01,01		00,00			00,00	
14,15	Color Palette # 10		00,12		00,00			00,00	
16,17	Color Palette # 11		01,13		00,00			00,00	
18,19	Color Palette # 12		00,44		00,00			00,00	
1A,1B	Color Palette # 13		01,45		00,00			00,00	
1C,1D	Color Palette # 14		00,56		00,00			00,00	
1E,1F	Color Palette # 15		01,57		02,20			03,60	
20	Duty				C7	63	00	00	00
21	Hsize				4F(9F)	9F	4F	4F	4F
22	Vadj				0F	07	07	0E	0F
23	SCT SCU | Hadj	00	00	00	01	01	01	1F	01
24	MON ULE | GRM 2 1 0 | FON 2 1 0	E3	E2	E2	E2	E2	E2	E2	E2
25	SYTH HERC SRAM 8BUS 16CP BINH | CLK 1 0	F5	F5	74	F5	F4	F4	75	F5
26	RA4 AI5 EXP | PB 1 0 | PAG 2 1 0	00	00	00	80	80	80	00	00
27	LS 1 0 | IEN EXTS IINH ACM CPLE PRE	00	03	01	83	83	83	83	03
28	SWC VST SSY SSCK H/E R/M | 2SCR 1 0	00	00	00	67(66)	6E	65	C1	11
29	STBY RREG ESIO | EH 4 3 2 1 0	00	00	00	00	13	00	00	00
2A	TST 2 1 0 | SS 4 3 2 1 0	00	00	00	00	00	00	00	00
2B	CON 7 6 5 4 3 2 1 0	00	00	00	00	00	00	00	00
30	Horiz. Total		5D	71	55	55	55	59	53
31	Hsy. Offset		FF	06	FE(00)	00	FE	E4	FC
32	Vsy. Offset		00	03	00	00	00	00	00
33	Sync. Width		DA	0A	0A	0A	0A	0A	0A
34	Vert. Total		19	1F	19	19	19	19	19
35	X X X | Vert. Adjust		02	06	00	00	00	00	00
36	X X X | Max. Scan		0D	07	07	07	07	07	07
37	F/O | TDS 1 0 | Cur. Offset	00	00	05	65	05	05	65	65
38	Horiz. Total		2E		2E			2D	2D
39	Hsy. Offset		FA		FE(FF)			EE	FD
3A	Vsy. Offset		01		08			08	08
3B	Sync. Width		D5		0A			0A	0A
3C	Vert. Total		5B		67			67	67
3D	X X X | Vert. Adjust		00		00			00	00
3E	X X X | Max. Scan		03		03			03	03
3F	45S | GDS 1 0 | UL. Position	0C	0C	07	07	07	07	07	07

NOTES:

1. The 6845 Preset Data (for Graphics Modes) have not been set because the 720 by 348 PEL display of HGC software cannot be displayed using either the 640 by 200 PEL display of an IBM color monitor or the 640 by 200 PEL display of an LCD.
2. For the 640 by 400 PEL display of a Panel or the 640 by 350 PEL display of an EGA monitor, the above setting enables the display of 640 dots from the left in the case of HGC software for a 720 by 348 PEL display. (With an EGA monitor, however, a looped scan line will be displayed at the right edge of the screen.)
3. Simultaneous display of an IBM color monitor and a 640 x 200, 1/200 duty one-screen LCD, can be enabled when a value in ( ) for the CLCDC is used (The SCK frequency, however, will be 3.5 MHz, exceeding the panel specified frequency of 2.5 MHz).

The specifications of this product are subject to improvement changes without prior notice.

AGENCY

NIPPON GAKKI CO., LTD

Address inquiries to:
Electronic System Division

- **Toyooka Factory** 203, Matsunokijima, Toyooka-mura, Iwata-gun, Shizuoka-ken, 438-01
  Electronic Equipment business section
  Tel. 053962-3125
- **Tokyo Office** 3-4, Surugadai Kanda, Chiyoda-ku, Tokyo, 104
  Ryumeikan Bldg. 4F
  Tel. 03-255-4481
- **Osaka Office** 1-16, Shin-ashiyashimo, Suita-shi, Osaka, 565
  Tel. 06-877-7731
- **U.S.A.** YAMAHA International Corp.
  6600 Orangethorp Ave.
  Buena Park California 90620

0.2K-0605 Printed in Japan 87. 1