

Tom Beaver on
VME/Futurebus

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OCTOBER 1, 1990

COMPUTER DESIGN

*Technology
and Design
Directions*

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS

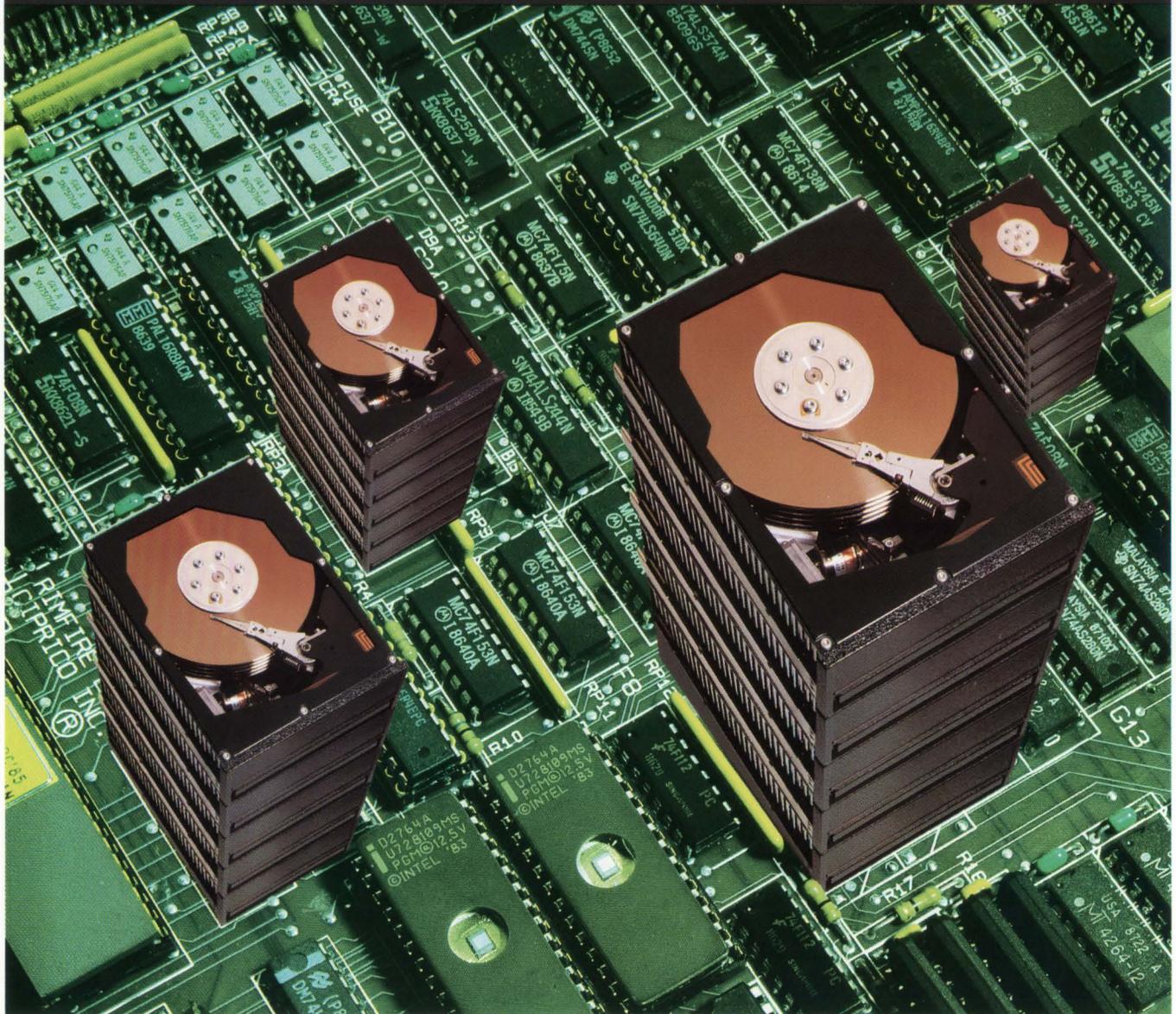
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CAD framework vendors
wrestle with standards

High-speed PALs keep pace
with today's processors



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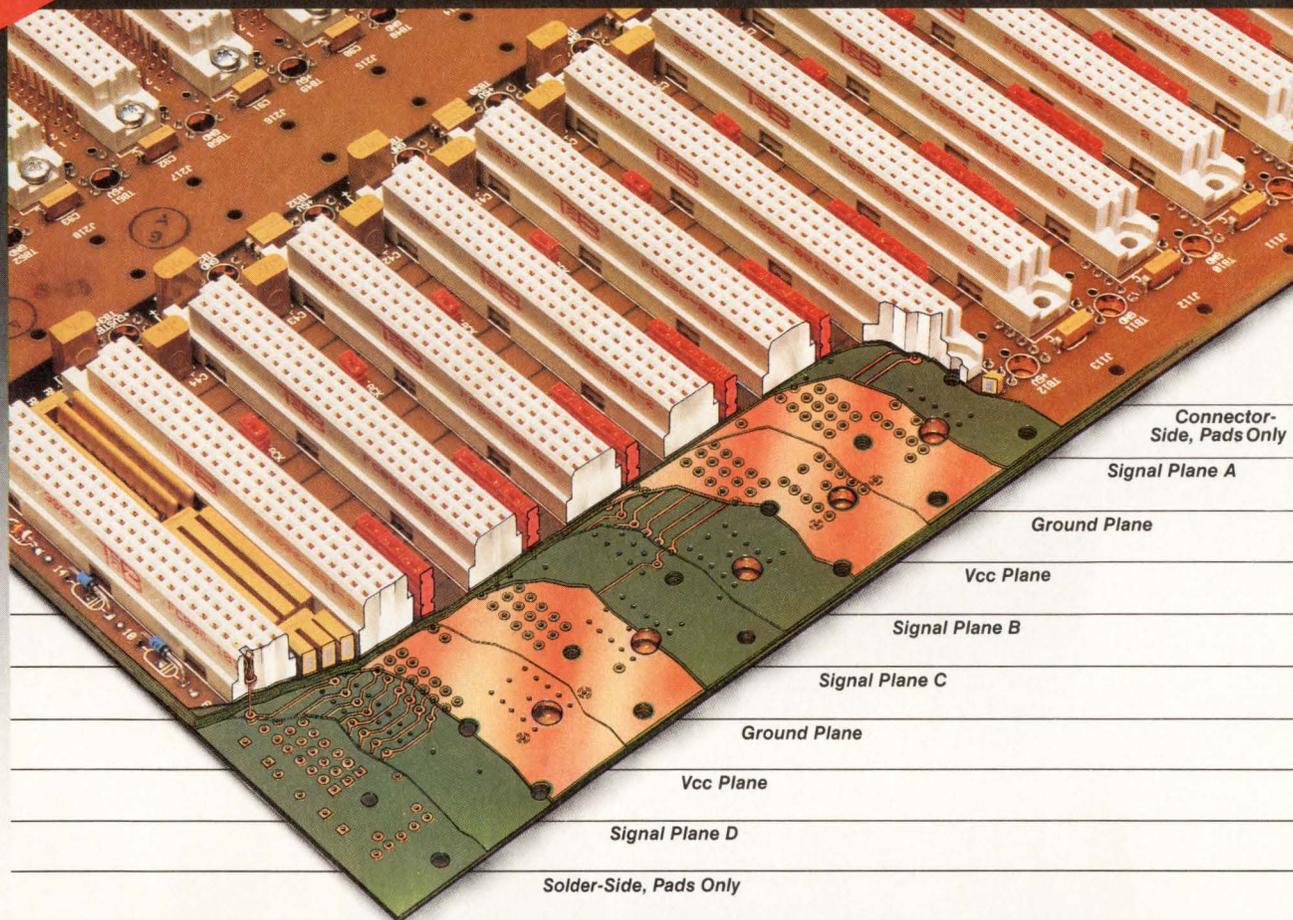
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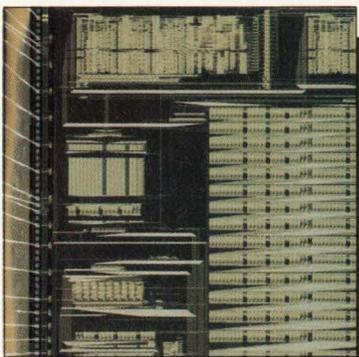


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FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS



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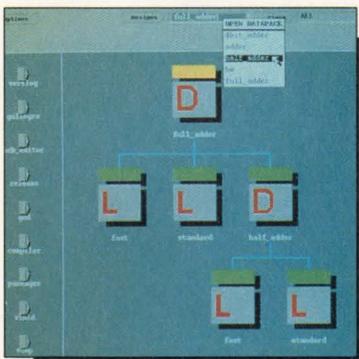
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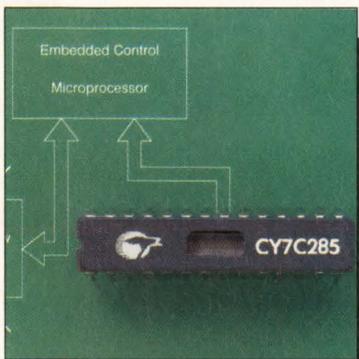
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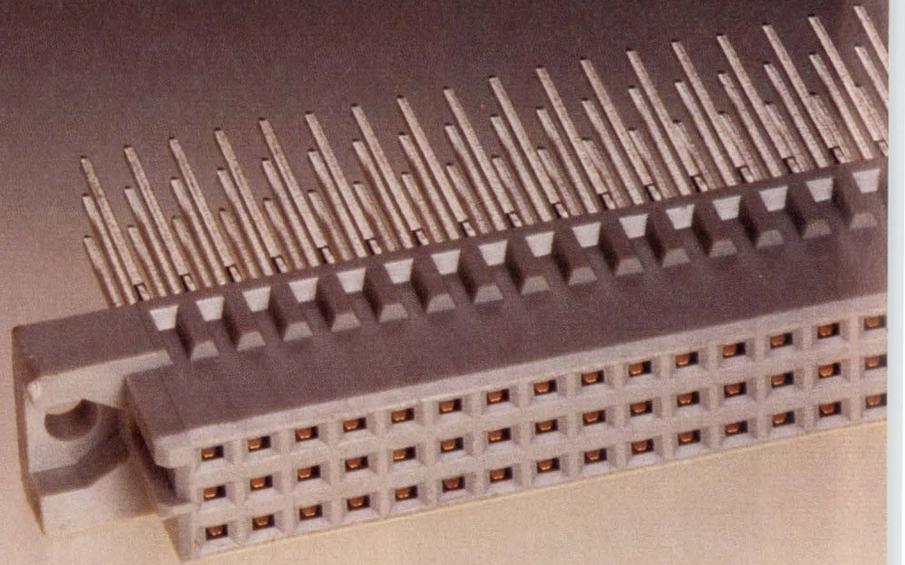
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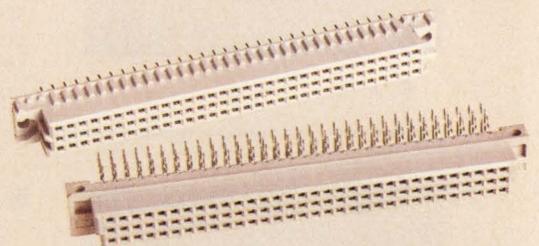
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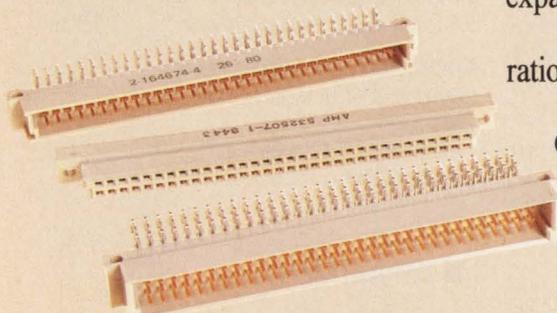
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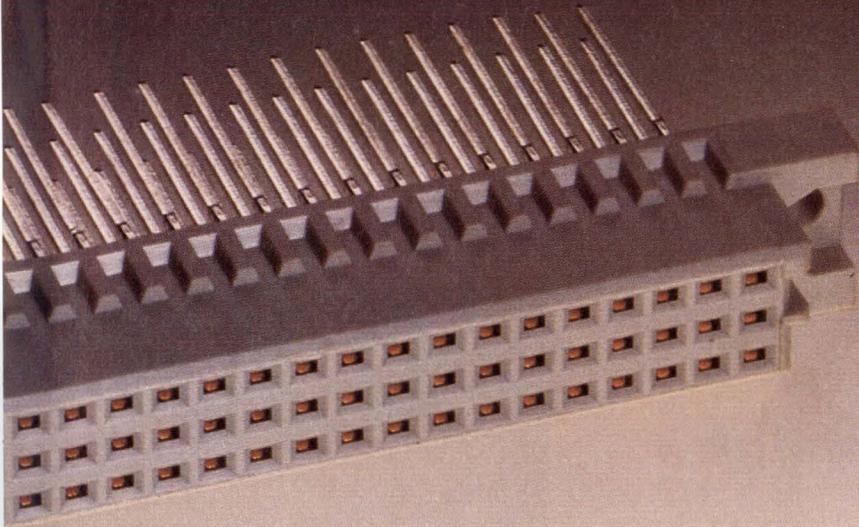
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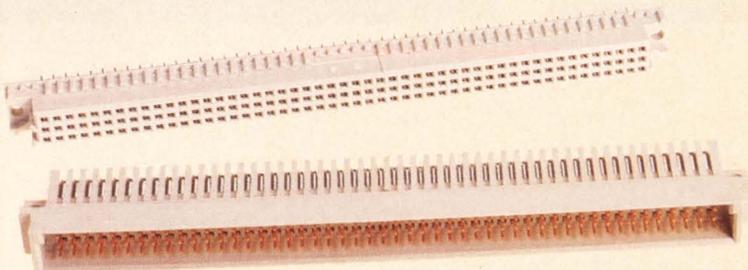
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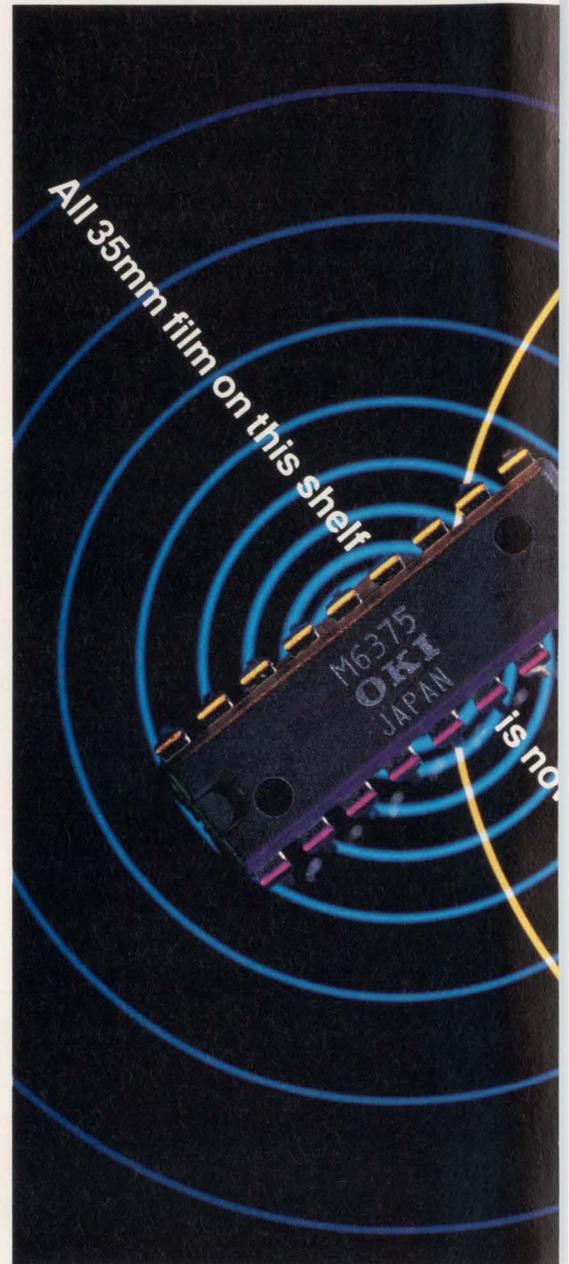
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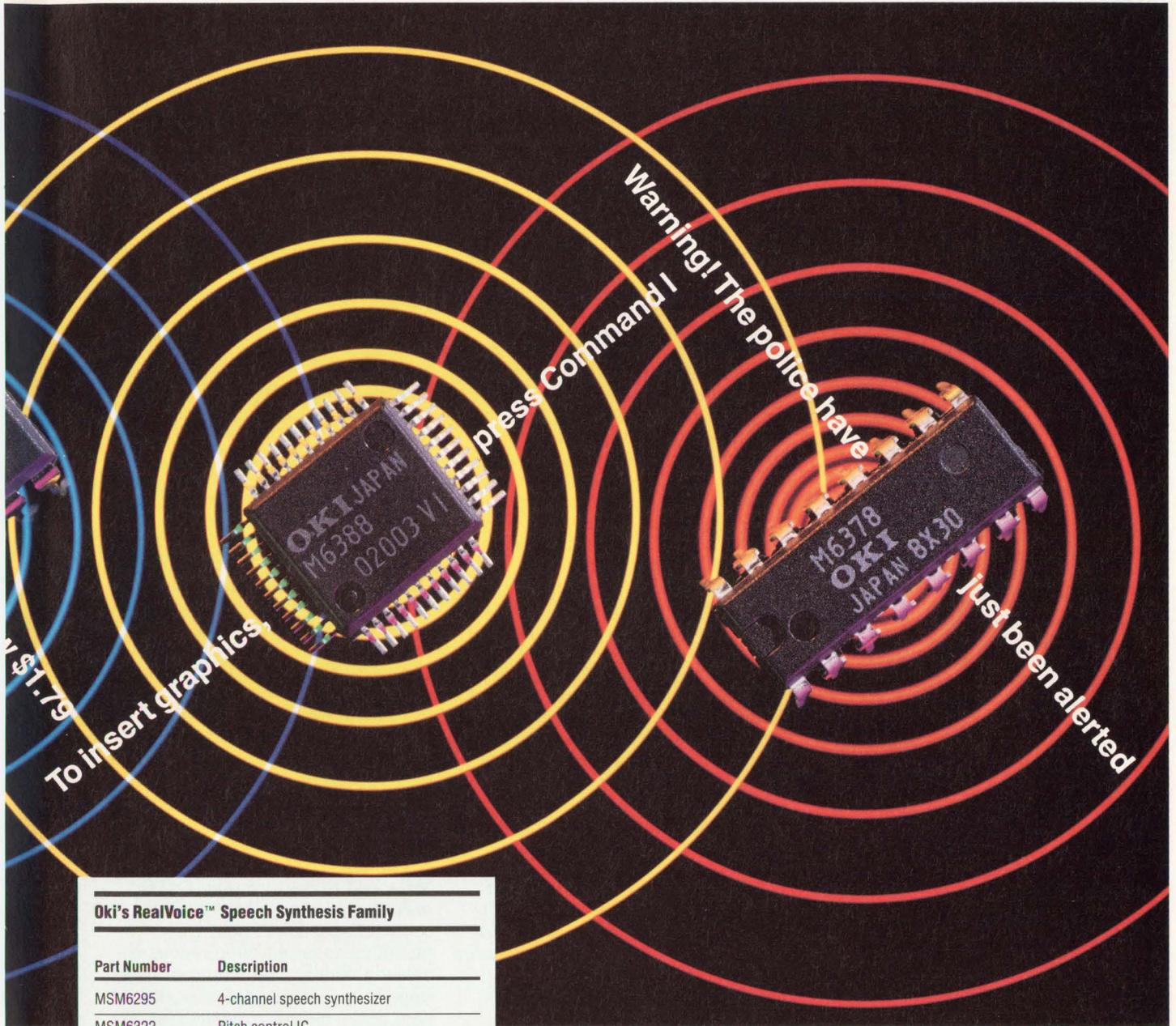
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JESSI SRAM development suspended

The Joint European Submicron Silicon Initiative (JESSI) suffered a setback last month when financially troubled Philips (Eindhoven, The Netherlands)—the number one European semiconductor maker—withdrawed from its role as next-generation SRAM technology developer under JESSI. Since Philips was pursuing that technology alone under JESSI, the European Community is hopeful that its only other SRAM maker, SGS-Thomson (Agrate, Italy and Paris, France), will apply for funds to continue the key JESSI development goal. SGS-Thomson is developing EPROM technology under another JESSI program.

Pursuing its own JESSI objective, Siemens (Munich, Germany) continues 64-Mbit DRAM development with cooperation from IBM (Armonk, NY), a DRAM client of Siemens. Joint development of a 0.5- μ m process technology has been under way at IBM's Advanced Semiconductor Technology Center in East Fishkill, NY, for several months.

Development costs have been estimated by JESSI at roughly \$450 million. But with at least 80 percent of the world merchant supply of advanced memories coming from Asia, neither Europe nor the United States figures it can afford not to develop a world-standard 64-Mbit chip. Both Siemens and IBM will market the giant DRAM, expected to be available in 1995.

—Barbara Tuck

Vitesse foresees 1M GaAs transistors

Long-time gallium-arsenide proponent Vitesse (Camarillo, CA) claims that it has finally broken through one of the barriers that has restrained the use of GaAs digital ICs: limited density. With a new process said to be simply a shrink of its existing H-GaAs II technology to 0.6 μ m, the vendor says that it can reach densities of 1 million transistors and operating speeds of 1 GHz. This would put most existing microprocessors and many medium-sized memory

devices within the reach of GaAs for the first time, making it possible to contemplate all-GaAs workstation CPU boards, for example.

Vitesse says reliability should be excellent because the new process uses the same four-metal, self-aligned gate configuration as its existing process. The company points out that compared with the complexity of most ECL and Bi-CMOS processes, its own 13-mask-layer process is simple. Yet even as its technology begins to validate its current claims, GaAs still seems to suffer from the hype with which it was announced several years ago.

—Ron Wilson

Group claims PCB design breakthrough

A research team at the University of California (Berkeley, CA) has stumbled upon a polymer film that it claims could revolutionize the printed circuit board manufacturing process. The newly discovered method uses a type of photoresistant polymer called arylated poly p-phenylene. The method lets electrical circuits be directly printed in one step instead of the current multistep process. When a negative image of a circuit pattern is placed over a board made of this material and then is exposed to light, the exposed regions of film become conductors, while the unexposed regions act as insulators.

Specialists in the field of board design are taking a wait-and-see attitude toward the film's performance before judging its importance. Questions regarding the conductivity of the polymer, as well as how fine a pitch it can attain, must be answered before the process gains industry acceptance.

—Mike Donlin

IBM/Metaphore pact aims to develop operating system link

Patriot Partners, a new joint venture launched by IBM (Armonk, NY) and Metaphore (Mountain View, CA), is aimed at developing a software technology that would let an application developer write

an application once—to the new interface—and then be able to run it on different operating systems. The new software would act as an intermediary between applications and DOS, OS/2 and Unix, a function that could probably be done without incurring much overhead on the newer 32-bit CISC and RISC workstations.

The move is seen by many as a way for IBM to reduce its dependence on Microsoft (Redmond, WA) and a way of working out its pique with Microsoft over the delays in delivering OS/2. The delay has aroused suspicions in IBM that, since the introduction of Windows 3.0, Microsoft may be hedging on its pledge that OS/2 would be the operating system of the future for advanced workstations.

—Tom Williams

Zilog buys into RISC in Germany

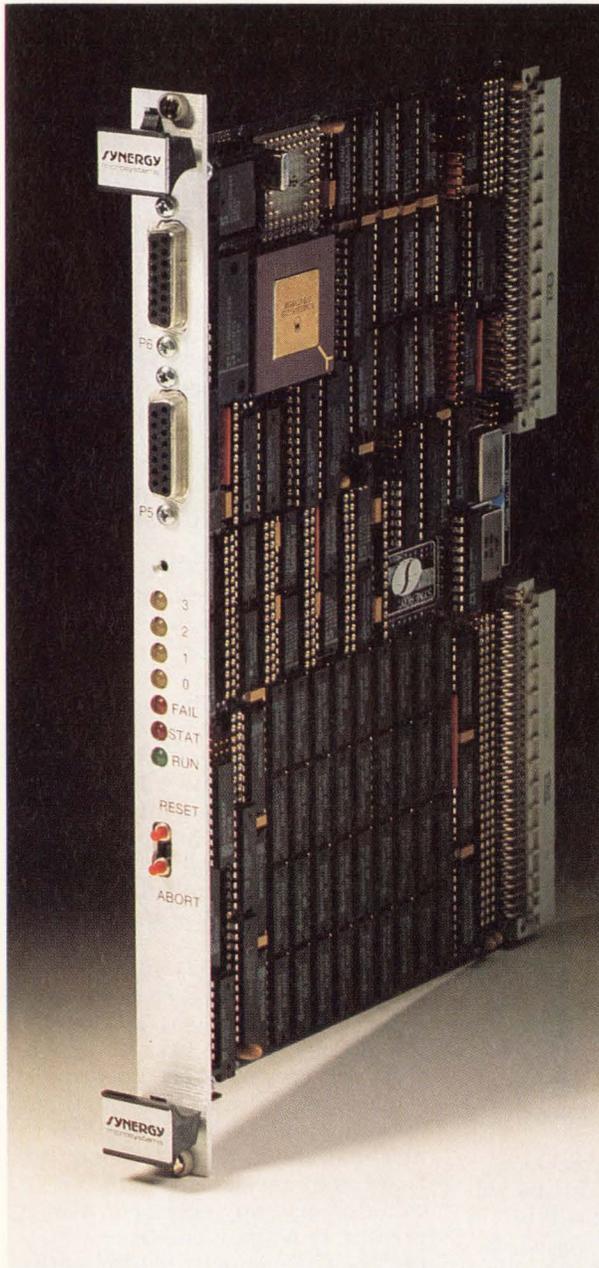
Zilog (Campbell, CA), a company that hasn't exactly been known as an architectural giant since the disappointing showing of the Z8000 nearly a decade ago, is staking out new territory in 32-bit CPU land. Rather than attempt yet another architecture launch on its own—remember the Z80,000, anyone?—the company has purchased the rights to a very compact, extremely fast RISC core from Hyperstone Electronics GMBH (Konstanz, West Germany).

The Hyperstone core, developed by Hyperstone president Otto Mueller, should exactly meet Zilog's needs for high-end processing. The device is said to crank out 33,000 Dhrystones at 25 MHz and to require only 64,000 mils² for implementation. Such compact speed will be a tremendous asset as Zilog moves its already widely used communications and control products into new performance ranges. The Hyperstone architecture abandons the RISC gospel of fixed-length instructions, relying on many 16-bit instruction codes to reduce program size. This also should be a big plus for embedded applications.

—Ron Wilson

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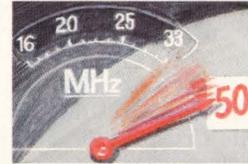
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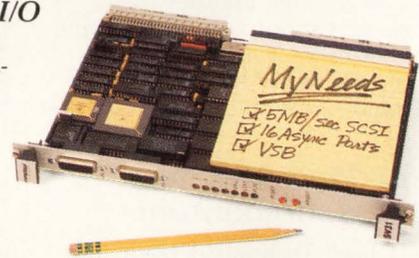


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Continued from page 8

HP tosses hat out of EDA tool ring

The electronic design division of Hewlett-Packard (Fort Collins, CO) will phase out its involvement in the electronic CAD/CAE market and will refocus its efforts on mechanical CAD/CAE and data-management tools. HP's acquisition of Apollo Computer (Chelmsford, MA) was part of the reason given for the tool phaseout. With Apollo's existing presence as an electronic design platform, particularly in conjunction with tools from Mentor Graphics (Beaverton, OR), HP found itself competing with potential customers.

The company assures current users of the electronic design tools that HP will continue to support them for at least another five years—news that will surely bring a sigh of relief from designers in Japan, where HP has at least a thousand seats. —Mike Donlin

Embedded ASIC test gathers momentum

CrossCheck Technology (San Jose, CA) and Credence Systems (Fremont, CA) recently have signed an agreement to jointly develop and market an interface linking Credence's digital VLSI test systems with CrossCheck's future ASIC diagnostic software products. The interface will let users access the internal device nodes provided by the embedded CrossCheck test structures for analysis and debug operations. The pact gives CrossCheck its first partner in the automatic test arena, while positioning Credence as the only ASIC tester vendor to have ready access to the on-chip test structures unveiled by CrossCheck last year.

At the International Test Conference (Washington, DC) in September, the two companies demonstrated joint technological capabilities using a simple interface to let the CrossCheck test electronics obtain data from an

ASIC connected to a Credence system. The test was conducted on a 28,000-gate device from LSI Logic (Milpitas, CA) using a Credence ASIX-2 tester. LSI Logic was CrossCheck's first technology licensee and is a user of Credence VLSI testers worldwide.

—Mike Donlin

Futurebus+ to take back seat to VME64 at Buscon

Futurebus+ has been so much in the media recently that it's hard to remember there are other buses. But at Buscon/90-East, Futurebus+ may take a back seat to some of the more conventional buses. VMEbus manufacturers have been looking to Futurebus+ as a next step in the progression of bus performance. "VMEbus has pretty much run out of gas with this generation's processor, the 68040," said Fred Rehhausser, director of marketing at Force Computers (Campbell, CA).

But a reality check on Futurebus+ indicates that real-world implementation—and a core infrastructure of vendors and suppliers—may be a bit farther off than at first anticipated. While it was expected that the rush of such giants as Digital Equipment Corp into the Futurebus+ world would have semiconductor makers scrambling to develop and make standard interface and controller chips, the giants have elected to use custom ASICs for the current generation. Semiconductor makers appear to have slowed activity until the specification and profiles settle down and a solid market emerges.

In the meantime, it looks as if previously unheralded VME64 will take up the slack. Force will be developing some VME64 products early next year, and between 10 and 15 VME64 boards will be shown at the upcoming Buscon. Though VME64 may not offer the magic of Futurebus+, it does provide the outspoken Futurebus+ advocates with a face-saving alternative. —Warren Andrews

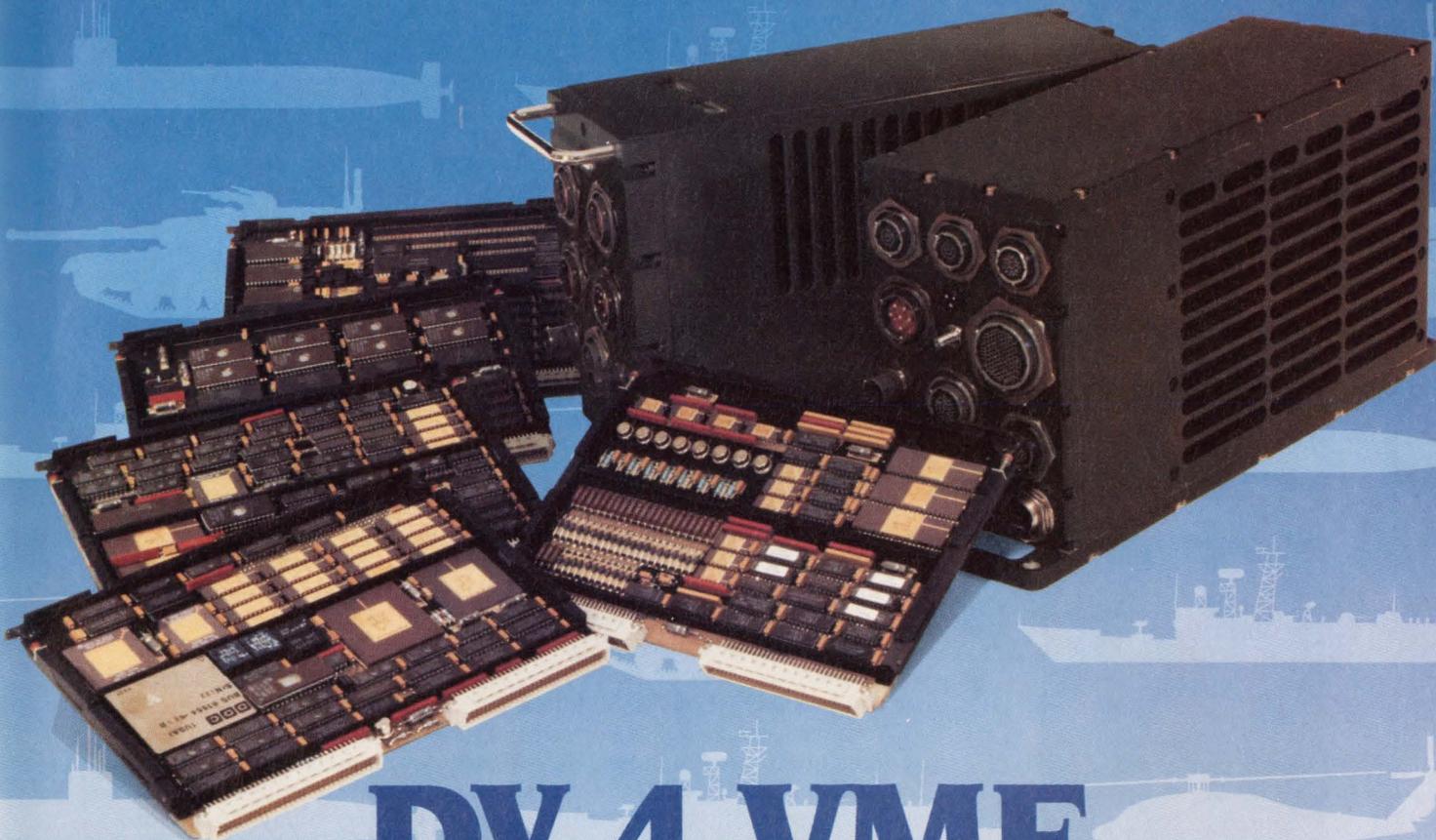
Buscon to see strong showing of STD 32 products

Although STD 32 has been raising eyebrows for almost a year since its introduction at Buscon/89-East, vendors haven't had anything to show—until now. Jim Eckford, director of marketing at Ziotech (San Luis Obispo, CA), reported that at Buscon/90-East, at least nine STD 32 products will be on display from three vendors.

Versallogic (Eugene, OR) will parade the industry's first-ever 16-bit peripheral, a high-performance analog-to-digital card capable of spitting out full 16-bit words. Technology 80 (Minneapolis, MN), another Task Group 32 member, will introduce a high-performance motion controller taking advantage of the extra interrupt capability borrowed from the EISA specification.

The first STD 32 CPU to hit the street will be Ziotech's 286-like multibus master, including the EISA bus-master protocols. Eckford wouldn't say too much about the card, aside from indicating that it would include the company's digital I/O ASIC. Ziotech will also show a 16-bit digital I/O card, a bus arbitration board for slot 0, a full-blown 16-bit Arcnet card (making it the fastest STD communications card), and a variety of backplanes and cabinets.

And while the STD 32 accomplishments look good so far, it's just the tip of the iceberg, according to Eckford. The first full 32-bit CPU will be a 960-based board—“Unless we're eclipsed by another manufacturer with a 386 or 486 machine,” he said. He claimed the board is under development but wouldn't give any details on the product or when it can be expected. The company is also working on a STD 32 interface/controller ASIC intended to make STD 32 easier to use, according to Eckford. —Warren Andrews



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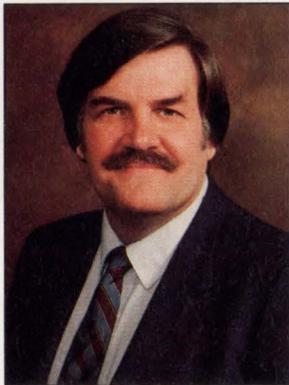
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CIRCLE NO. 7

Managed markets and managed trade are what everyone really believes in and practices.



John C. Miklosz
Associate Publisher/
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Stop worshipping a free market

This may sound like heresy, but the concepts, theories and principles—call them what you will—of free markets and free trade aren't gospel. The adherence to free markets and free trade isn't decreed by the Bible, the Torah, the Koran or the writings of Confucius. That's a good thing, too, because there's certainly no government, and probably very few individuals, that believe in totally free markets or totally free trade. Not the United States, not Great Britain, not Germany, not France, not Brazil and not Japan.

What's more, no one has ever demonstrated that a completely free market economy or unrestricted free trade provides either a maximum in benefits or an optimum mix of benefits—low prices, good jobs, growth, stability, a strong economy—for individual citizens and their countries over the long term.

Recent events in the Middle East have only served to underscore this reality. There has never been, at least within recent memory, a "free" market in oil. For some time now, the price of oil has been determined by OPEC, with one of its goals to keep the industrialized nations—in particular, the United States—from developing alternative sources. Because we've been foolish enough to slavishly apply free market principles to oil for the last 15 years, we did precisely what the Middle Eastern oil producers wanted.

We never supported the development of alternative energy sources or conservation, nor did we pursue the development of fuel-efficient automobiles because in a "free market" the costs couldn't be justified. As a result, we're now going to pay dearly for putting free market principles on an altar. The cost of this most recent oil crisis, in terms of lost production and economic growth, has so far been estimated in the trillions of dollars; how many trillions will depend on how high the price of oil goes and how long it stays there.

The time has long since past for our representatives in government, industry, finance and academia to stop worshipping free market and free trade principles as if they had been handed down from God, and to look instead to rationally *managed* markets and trade. Managed markets and managed trade, whether it be in oil, ICs, computers, airplanes or tobacco, are what everyone *really* believes in and practices, regardless of the proselytizing for a free market religion.

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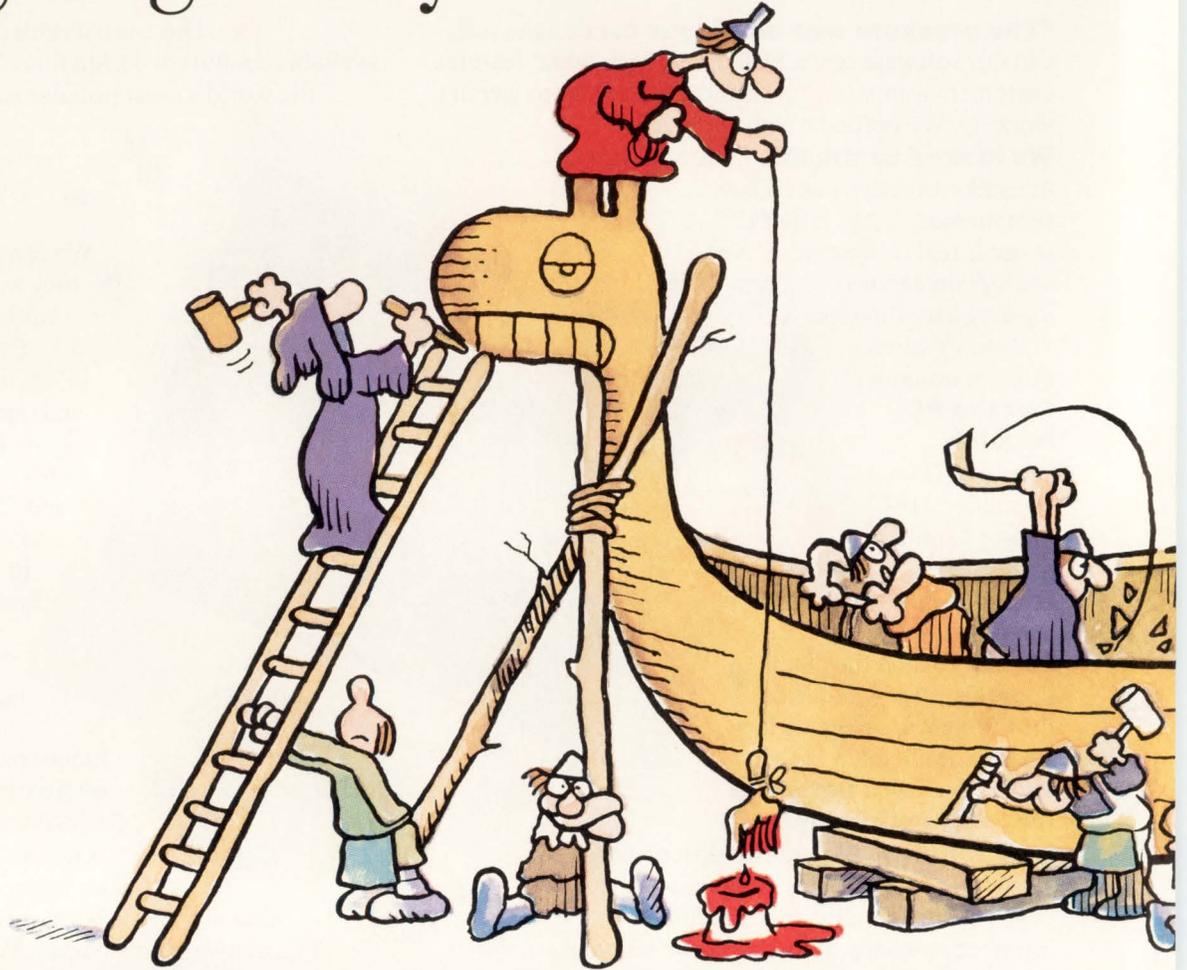
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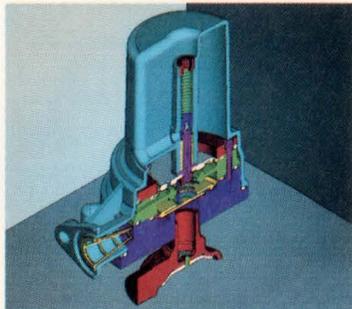
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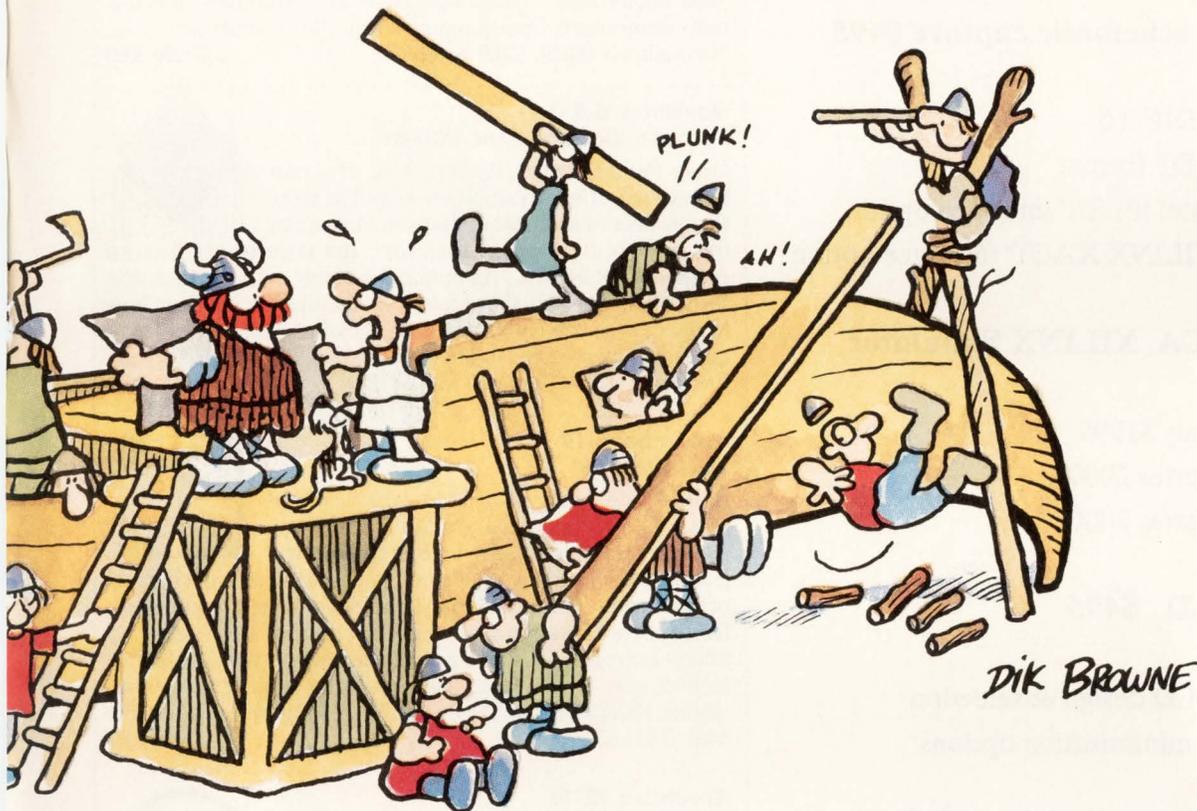
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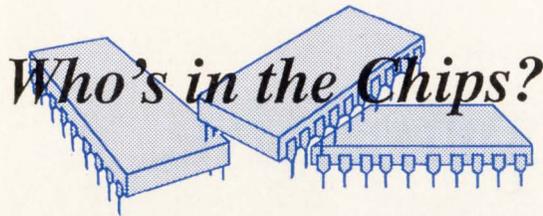
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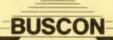
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CONFERENCES

October 15-18

Buscon/90-East

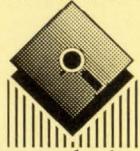
Royal Plaza Trade Center, Marlborough, MA. This conference for bus board and systems-level technology will highlight issues and applications for embedded systems programming, VME, Multi-bus II, PC bus platforms, emerging architectures and military applications. Buscon will include over 200 exhibitors. Information: Conference Management Corp, 200 Connecticut Ave, Norwalk, CT 06856 (203) 852-0500. **Circle 360**



November 6-9

Software Development '90-Fall

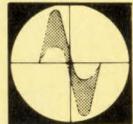
Omni Parker House, Boston, MA. The conference will offer an exhibition as well as more than 60 lectures and workshops in four areas: object-oriented programming, management, design methodologies and C. An optional one-day seminar on teamwork will be presented by Larry Constantine, focusing on how to build, organize and manage effective project teams. Information: Software Development Seminars, 500 Howard St, San Francisco, CA 94105 (415) 995-2472. **Circle 361**



November 6-10

Electronica '90

Munich Trade Fair Centre, Munich, West Germany. The International Trade Fair for Components and Assemblies in Electronics will feature exhibits in electronic components, electromechanical products and quality assurance and development equipment. Related events include conferences focusing on microelectronic sensors and on the use of semiconductor technologies in switching and regulating applications. Information: Kallman Associates, 5 Maple Ct, Ridgewood, NJ 07450-4431 (201) 652-7070. **Circle 362**



November 12-16

Comdex/Fall '90

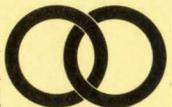
Las Vegas, NV, nine locations. The 12th Comdex conference and trade show will feature more than 1,800 exhibitors and is targeted at computer distribution professionals, including volume resellers of small computers, peripherals, software and accessories. Ten tracks will encompass over 48 sessions on topics including portable computing, imaging systems, buyer/seller issues, communications, multimedia and industry perspectives. Information: The Interface Group, 300 First Ave, Needham, MA 02194 (617) 449-6600. **Circle 363**



November 13-15

Wescon

Anaheim Convention Center, Anaheim, CA. This year's conference will offer 36 technical sessions, 22 tutorials, a panel discussing world engineering issues, a professional development panel, a technology initiatives panel and over 1,000 exhibits, including one demonstrating the state of the art in PC-based design tools. Information: Electronic Conventions Management, 8110 Airport Blvd, Los Angeles, CA 90045 (800) 877-2668. **Circle 364**





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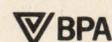
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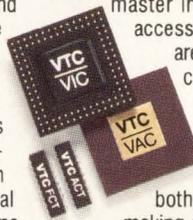
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CIRCLE NO. 18

Tom Beaver on VME/ Futurebus

Since its introduction, VME has become the predominant 32-bit bus architecture for open systems and is used in many diverse applications. Its uses range from low-end single-user and industrial-control systems to complex multicratered scientific data-collection and artificial-reality systems. Its acceptance in the market has resulted in the 200-member VFEA International Trade Association, a model in the microcomputer industry. There are also numerous VME user groups throughout the world.

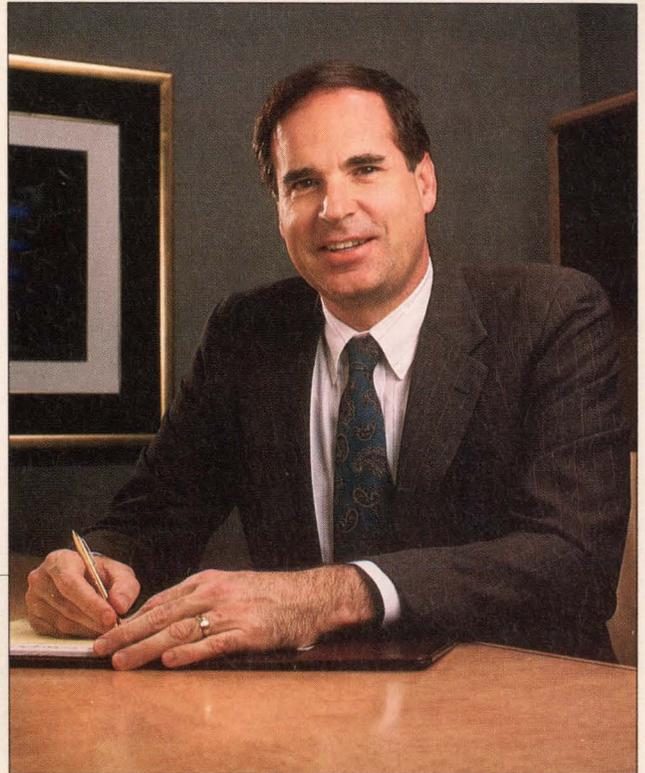
In the past three years, the VME industry has been actively and openly revising and enhancing the VME architecture through VITA. The most visible and talked-about aspect of this activity has been the adoption of Futurebus+ as the high-end multiprocessor interconnect that coexists with VME in a dual-bus architecture.

This strategy has raised the question many times in the past three years, "Why was the introduction of VFEA (VME Futurebus Extended Architecture) necessary, and will this mean the end of VME?"

The reasons given for the introduction of VFEA are most often based on technology: it was prompted by the introduction of RISC microprocessors, increased execution rates, extensive use of cache, multiprocessing Unix and the need for fault-tolerant systems. All these reasons are certainly valid, and the new technologies do indeed require major enhancements to the open systems architecture.

■ The system hierarchy

To answer the question from a different angle, let's look at the major ingredients in a system hierarchy. One can identify layers that have very distinct characteristics. To be most useful, each layer must be able to absorb multiple generations of the layers immediately below. We would like to manipulate information such as a database, for example, that has been accumulated over many years, and to do so with different applications (word processors, spreadsheets, database managers), regardless of the underlying operating system and independently of the hardware architecture (single or multiple processor, bus- or network-based) or the specific technology used (such as RISC



or CISC). This is the challenge facing our industry.

The first layer in the system hierarchy contains the base technologies used to build computer systems—components such as microprocessors, memory chips and mass storage devices. As time goes by, the life cycles of these base technologies get ever shorter. For example, Motorola introduced the first 16-bit 68000 in 1979. Five years later, the first 32-bit microprocessor, the MC68020, was introduced. Three years after that, Motorola introduced the MC68030, the first microprocessor to use the Harvard architecture. In quick succession to the MC68030 were the MC88100 RISC, in 1988, and the MC68040 CISC, in 1990.

In the face of such quick and revolutionary advances in base technologies, how can users determine which is the right solution to address their needs—not only today, but tomorrow? Will the "advanced" system they bought today be obsolete in two years? Can anything be done to ensure that the investment made in today's technology will be preserved tomorrow when the next wave of technology hits?

The industry's challenge will be to guarantee customer satisfaction and ensure that the life expectancy of the next layer—hardware—is increased. This layer contains the hardware components and subassemblies that make up a computer system. Typical components in this layer would be processor boards, memory boards, peripheral controllers and mass-storage subsystems.

The 1970s, viewed as the decade of the proprietary system, did not promote the life expectancy of system architectures. The majority of computer systems sold were based on proprietary architectures. Once a system was bought, the only way to enhance its capabilities was to acquire additional proprietary components from a single vendor. The introduction of more capable

or faster technology usually meant discarding the old equipment and purchasing a new, more advanced system. The numerous examples of this scenario range from mainframes to minicomputers. Generally, proprietary systems have very limited scalability and don't preserve the user's investment.

In the early 1980s, the concept of open systems was conceived to solve the problems associated with proprietary systems. It has since become a major requirement of users worldwide. Initial developments that responded to this need were in the area of industry-wide standard bus technology. One of the most important requirements of these buses is that they be forward-looking—able to absorb new technologies as they became available.

When VMEbus was introduced in 1981, for example, its capabilities exceeded those required to support the available microcomputer technology. The first revision of VMEbus already supported the 32-bit data and address buses, while current microprocessor technology was just evolving from an 8- to a 16-bit data bus and from a 16- to a 24-bit address bus. At a time when microcomputer systems required single-digit data-transfer rates, the VMEbus could deliver a throughput of over 30 Mbytes/s.

As a result of these capabilities, VMEbus was ideally positioned to absorb 32-bit technology when the MC68020 was introduced in 1984. Indeed, the introduction of that technology has caused explosive growth in the design wins of VMEbus. A major reason for that success is VMEbus' ability to absorb multiple generations of technology offered by different vendors at different times, allowing existing equipment to be saved.

This "technology independence" was a guiding light in the development of VFEA, and it will indeed lengthen the life expectancy of the base hardware. As with VMEbus, the data-transfer and addressing capabilities of Futurebus+ far exceed the requirements of today's technology. In addition, the hierarchical nature of the VFEA—that is, the ability of multiple VMEbus and Futurebus+ subsystems to coexist and interoperate in a system environment—ensures that customers' hardware investments are preserved.

■ Move toward standards

But perhaps more important than the absorption of emerging technologies is the ability to enhance capabilities within a standard environment. This establishes a platform with the necessary long-term stability to increase the life expectancy of successive generations of the next layer—the operating system.

The third layer in the hierarchy of a computer, the operating system, is significantly more expensive to develop and maintain. It's the part of the system that interfaces to the hardware layer below and offers services to the applications layer above. By studying the history of operating systems, one can identify a definite move toward standards.

Initially, users were satisfied with proprietary operating systems such as Digital Equipment Corp's VMS and IBM's MVS. But they were again at the

mercy of a single source for all their computing needs. This held true for hardware and associated technology as well as for application software.

In the late 1980s, that trend began to change as the user community started to require compliance to standards for the systems they chose. As a result, the computer industry has actively pursued the standardization of Unix via formal activities within both the industry and the IEEE. Even vendors who have been the strongholds of proprietary solutions are actively participating in these activities and offering standards-based solutions.

■ The challenges ahead

Various projects are under way to address users' needs for standardization. Unix International is aggressively establishing standards for both the Driver Device Interface and Driver Kernel Interface. VITA is drafting the Bridge Specification so that it offers a software-transparent interface to both VME and Futurebus+ systems, while 88Open, a group of manufacturers supporting the 88000, is developing a common interface between device drivers and hardware. All these activities are designed to ensure that in the process of enhancing a system's hardware capabilities, the more costly investment in operating systems is preserved.

In addition, to make sure that the underlying software technology offers a common and lasting environment for the fourth layer—applications—the standardization of the interface between the operating system and application software is being pursued as

well. VITA has published the Open Real-Time Kernel Interface Definition, which offers a common interface to real-time applications. The IEEE has published Posix, a standard system-calls interface to Unix that increases source-level portability of applications software. Unix International is establishing a generic Application Binary Interface (ABI) standard that increases portability of binary modules. Motorola is extending ABI so it provides a common interface to both 88000- and 68000-based systems.

The goal of all of these activities is the same: to increase the value of delivered products so that the effort to migrate from one architecture and system generation to the next is minimized. However, while significant progress is being made to promote ever-increasing life expectancy of products in the higher layers of the system hierarchy, critical challenges are still ahead.

The effort to establish industry-wide standards for data-exchange formats is in its infancy. Even if such standards are indeed established, it's doubtful that the vast amount of information already accumulated over four decades of computing—and still in use—will be compatible. I strongly believe that it is this last frontier of standardization that will pose the most serious challenge.

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Tom Beaver is senior vice-president and general manager of the Motorola Computer Group (Tempe, AZ).

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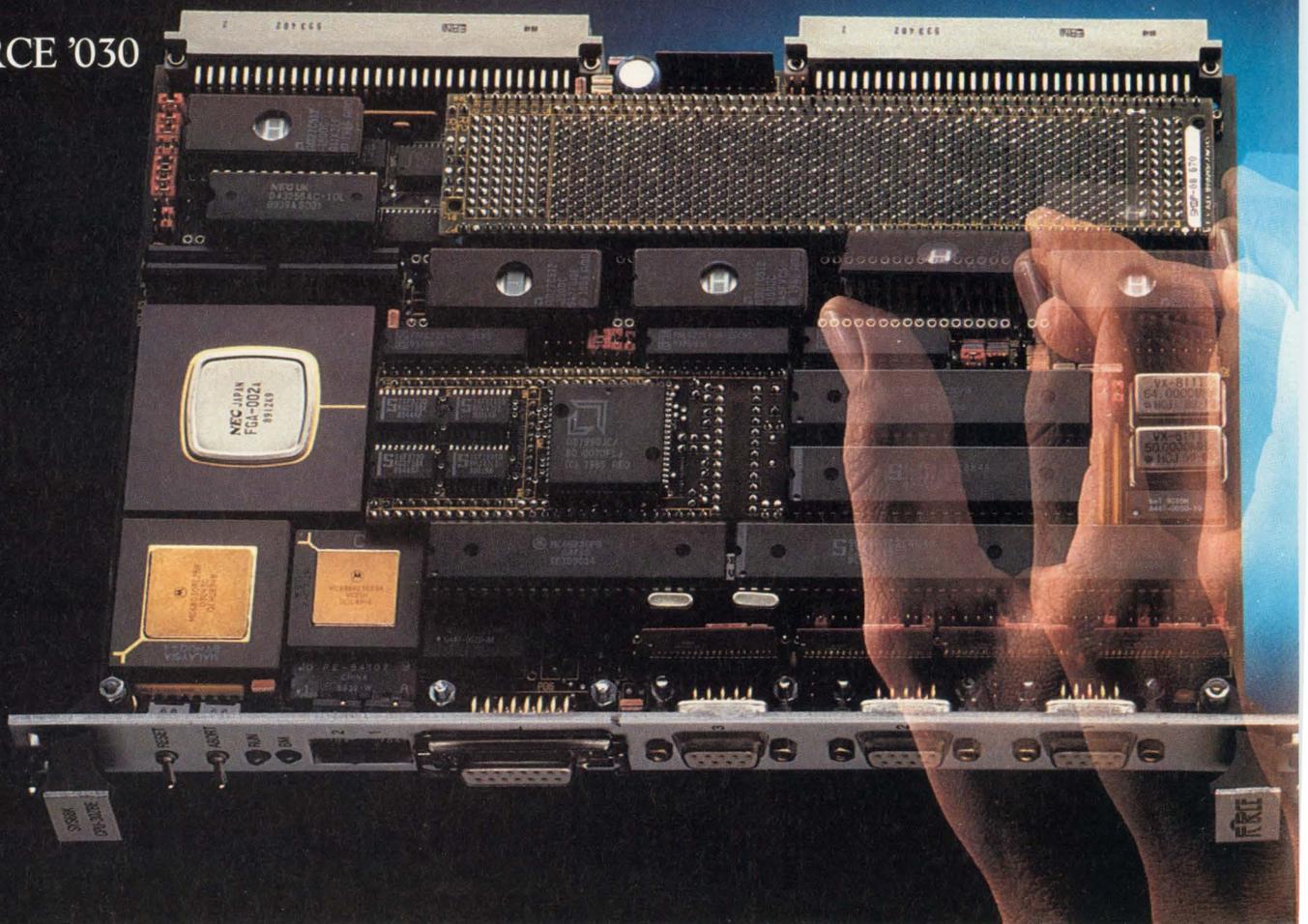
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AMD beats Intel to the punch with single-chip AT motherboard

Ron Wilson, Senior Editor

It had to happen sooner or later. Someone was going to combine the core logic of the PC/AT with a CPU to make a single-chip AT motherboard. The big surprise is who got there first—not Intel (Santa Clara, CA), who had the CPU designs, or any of the established chip set vendors, who had the logic designs, but Advanced Micro Devices (Sunnyvale, CA).

The choices AMD made in bringing its chips—the Am286ZX and Am286LX—to market reflect a variety of legal, technical and business constraints. And while the company's decisions make the new part particularly suited to some applications, it is far from a general-purpose solution.

The primary constraint faced by any would-be designer of a single-chip motherboard is the need for a CPU. Obviously, the product has to have an Intel-compatible processor. But Intel remains the only source for the 80386DX and SX architectures—only the venerable 286 has been licensed to other vendors. So designers are faced with the choice of exercising a 286 license—if they have one—or confronting the daunting technical task and legal perils of reverse-engineering the 386.

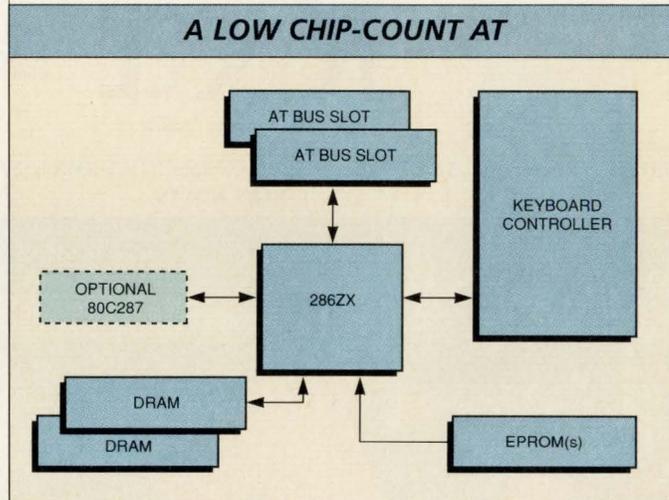
Hard technical choices

This bind put AMD, one of the original 286 licensees and most aggressive 286 alternate source, a leg up in the race to one chip. "We used AMD's CMOS 286 hardware design, together with the 286 microcode licensed from Intel," says Rajesh Tanna, AMD technical marketing manager for the new chip. That solved the CPU problem, but left AMD with another hurdle. The company hasn't produced a commercial chip set of its own. To overcome this problem, the design team, based in Austin, TX, gathered up some existing AMD parts and combined them with newly created logic to reach state-of-the-market chip set functionality.

Choosing the logic for the chip forced AMD into a series of difficult technical decisions. The state of CMOS technology won't permit a whole AT—peripheral controllers, memory and all—to fit on a single chip. In fact, price competition at the low end of the PC market is so fierce that every bit of additional die area comes at the expense of lower margins. But too much compromise on functionality would produce a use-

One shut-down mode simply turns off the 285 processor; another shuts off all clocks except the DRAM refresh circuitry. And the DRAM controller staggers refresh and supports slow-refresh DRAMs, two techniques that are being used in notebook designs to extend battery life.

Another design problem that has challenged chip set designers, even at much lower levels of integration, is drivers. Transistors big enough to drive lots of banks of DRAM and lots of AT bus slots take up lots of real estate. And the more drivers you put on a fast chip, the more problems you're likely to have with ground bounce. This would be a particular problem for a single-chip motherboard, which must source three in-



By combining a 286 CPU with an AT chip set on one die, AMD has produced the lowest chip-count motherboard yet—with just the new Am286ZX or LX, a keyboard controller, an EPROM and some DRAM. The ZX supports two banks of DRAM and two AT bus slots without external drivers.

less product. In this environment, AMD focused its part on two specific applications: the ZX for low-end desktops and the LX for laptop/palmtops, letting the needs of these markets direct its technical decisions.

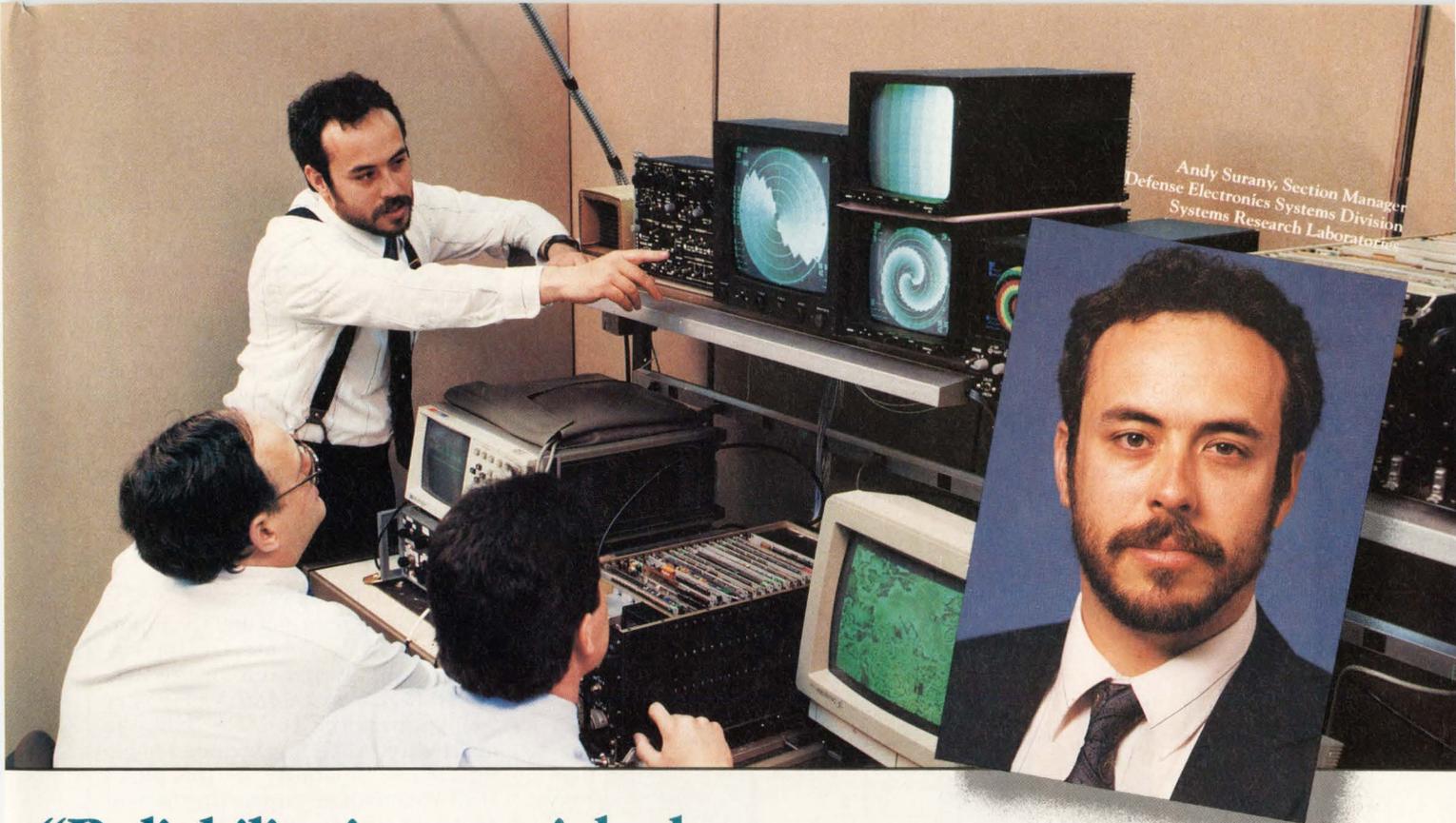
The team decided on a no-compromise approach to the current AT feature set. Consequently, the chip has such advanced features as 128-register EMS hardware, which permits good performance on memory-intensive applications such as Windows 3.0; and Gate-A20 support, which is necessary to good performance under OS/2. Unlike many highly integrated chip sets, the Am286 parts include a real-time clock and SRAM.

For the laptop-targeted LX, the designers took advantage of having all the logic on one die to get some advanced power-saving features.

dependent buses: the memory (or M) bus, the peripheral (or X) bus and the AT bus itself.

AMD's approach was to include drivers just big enough for two banks of DRAM on the M bus and for two AT slots. That should be plenty for laptop and notebook use, and larger configurations in desktop machines can be reached by adding external buffers.

Another important compromise the team made was in excluding some peripheral control logic. The 8042 keyboard controller had to go. "There just wasn't room for it," Tanna says. And the technology wasn't ready for inclusion of floppy, hard disk or display controllers. AMD has plans in this area, Tanna suggests, but they will involve a second highly integrated chip rather than an ex-



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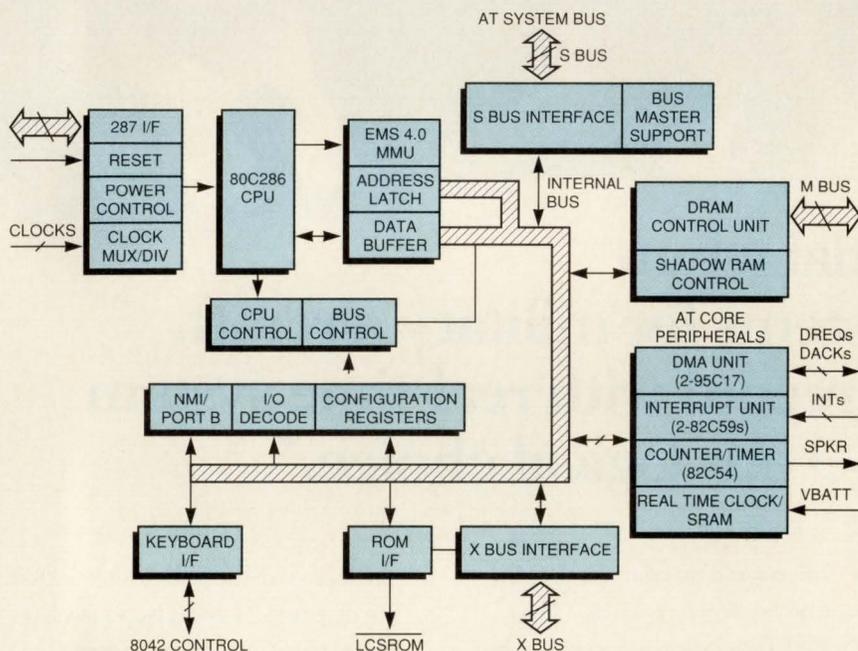
pansion of the current die.

Even with these compromises, the product has to struggle against high cost. The chip will compete in a market where huge volumes have driven the prices of 286 CPUs and single-chip AT logic implementations into the ground. With its large new die, the part can't compete on raw parts cost. This will be particularly apparent in the desktop market.

An issue in these cost-sensitive markets is how to package the chip with three major buses coming out of it. A huge, expensive package could price the part out of the market regardless of die cost. AMD's solution was to license tape-pack technology from National Semiconductor (Santa Clara, CA). The part will come in a 216-pin plastic quad flat pack with flat leads mounted in

working on a single-chip design, but won't discuss introduction dates or product features. A few vendors from the chip-set side of the industry are rumored to be working on reverse-engineered 386 CPUs for use in highly integrated sets, but these efforts are likely to be a year from fruition. And, of course, there's the problem of legal protection of the 386 hardware and microcode. So the AMD part could have the one-chip market to itself for some time.

INSIDE THE 286ZX



Internally, the Am286ZX and LX parts look very much like a typical AT motherboard. The AMD CPU core is surrounded by the functional blocks found in most current-generation chip sets, including EMS hardware and a real-time clock. Like most chip sets, the part creates three buses: memory, peripheral and system.

"For desktop use, the chip will sell at about a 20 percent premium to existing 286 CPUs and AT chip sets," Tanna admits. "But you have to look at the system cost, not just the chip set cost. This part will significantly reduce the number of packages on the board, cutting board size and assembly/test time, even for desktop systems. And in the laptop/notebook markets, where space is critical, we have the added advantage of the power-saving features of the Am286LX. Just the size and power consumption will make the chip very competitive there," he says.

a plastic ring. Customers will need trim-and-form hardware to excise the package from the ring, form the leads and mount the chip on a board.

Even with the functionality and cost arguments addressed, there remains one big strategic question. Is it just too late to introduce a new product based on the 286 architecture? This turns out to be a more complicated question than Intel, which has been pushing the 386SX as a 286-killer, might admit.

To start with, AMD got there with the 286 first. Intel claims to have both CPU and chip set design teams

Compatibility woes

Performance may not be an important issue in the debate. On applications originally written for the 286, the 16-MHz Am286ZX/LX may very well outperform 16-MHz 386s. To make sure, AMD has included page-interleave capability in the part's DRAM controller, supporting two- or four-way interleaving. This will reduce wait states to near zero, even when the company moves the part to 20 MHz later on.

The big problem will be compatibility. If a significant portion of PC software is recoded for the 386, 286-based machines could be sealed off from new software products or perhaps even from updates on existing code. But this move, long predicted by Intel, seems slow in developing.

Even though there are significant performance advantages in writing for the 386's flat address space instead of the 286's segmented, EMS-backed model, vendors look at the fact that about two-thirds of the PC market is still running 286s. That makes them hesitate to jump.

So the new chip probably has an excellent chance, especially in the emerging notebook/palmtop end of the market where elimination of a few more packages would be crucial. But AMD will have to live looking over its shoulder, as the shadow of a single 386SX motherboard chip grows longer on the floor.

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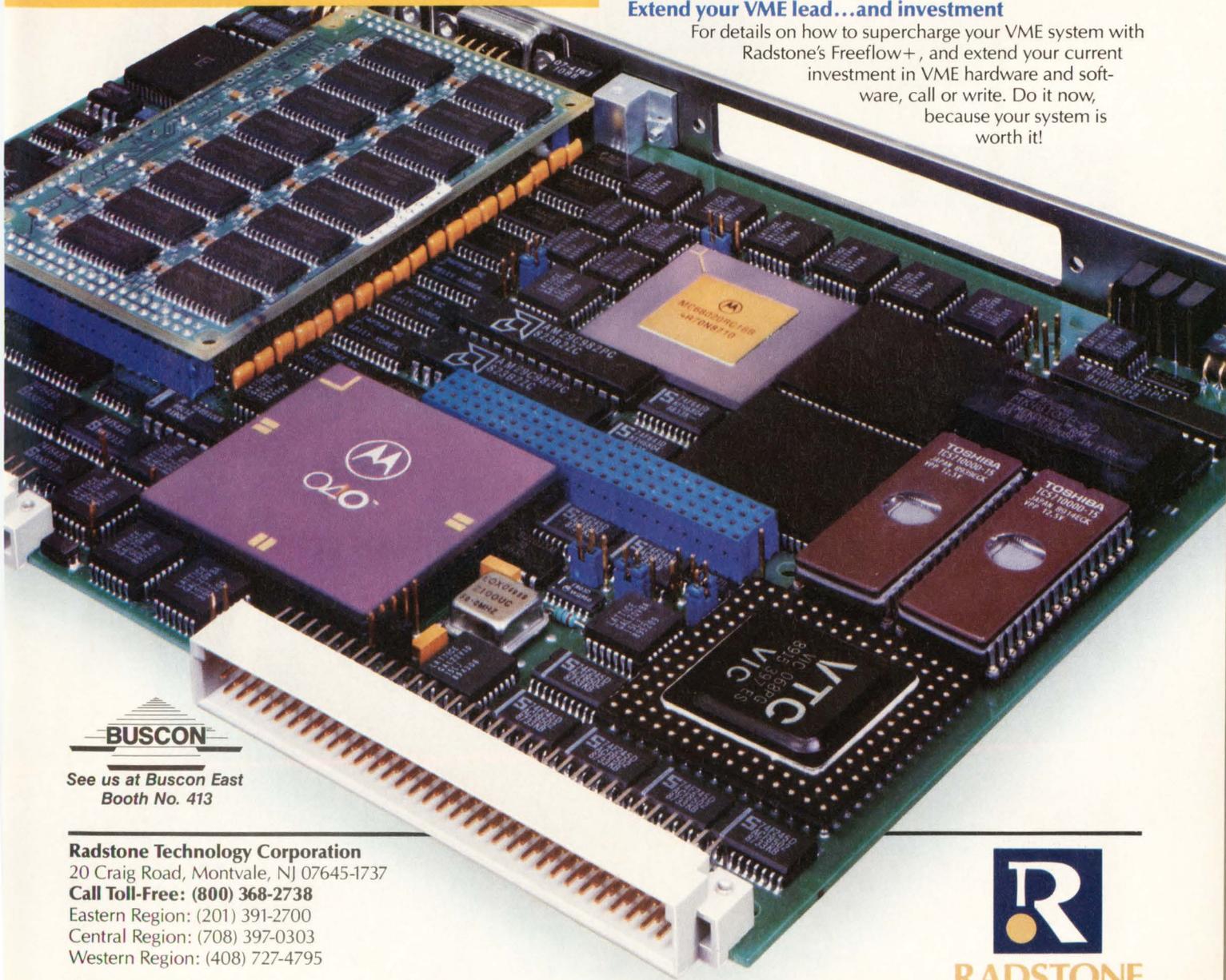
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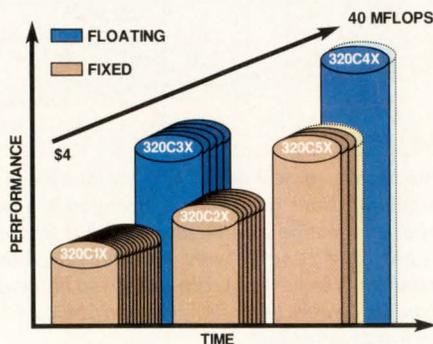
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DSP chip reinforces trend toward parallel multichip solutions

Warren Andrews, Senior Editor

The latest entry in the single-chip digital signal processing market is a Texas Instruments device designed to be used in multiple-chip configurations. While this sounds contradictory, Ray Simar, senior member of the technical staff at TI (Houston, TX), says, "Whether or not to apply DSP chips in parallel is a moot question. The price/performance ratio continues to improve and continues to make a strong case for the use of multiple chips."

TI's new chip, the TMS320C40, is specifically designed to be used with other TMS320C40s, reflecting the strong movement in both chip and board architectures toward multiple, parallel chips and/or boards. At the chip level, almost every sophisticated application ranging from image enhancement to speech recognition employs multiple DSP chips tied together. For example, most of the standard-architecture DSP boards such as VME and Multibus boards from makers such as Sky Computers (Chelmsford, MA), AT&T (Berkeley Heights, NJ) and Spectrum Signal Processing (Burnaby, British Columbia, Canada) employ multiple DSP chips. In addition, advanced PC-based DSP boards—such as Ariel (Highland Park, NJ) boards containing Motorola's latest 32-bit floating-point DSP chip, the 962000—are using multichip solutions.

Further underscoring the trend toward multiple-processor DSP architectures, TI cites several examples where multiple TMS320C30s (TI's initial 32-bit floating-point single-chip DSP offering) have been used. These include graphics workstations from Silicon Graphics, Hewlett-Packard and Intergraph, each sporting a minimum of three C30s and operating at rates from just over a half billion to better than 1.25 billion operations per second.

NASA used three C30s in a virtual-world astronaut trainer and achieved a performance of 550 MOPS, while Compression Labs

uses 15 C30s in a video conferencing application that operates at 2.75 billion operations per second.

Still other DSP chips have been used in multiple-chip applications. AT&T's DSP32C, for example, is used in one of the company's own VME boards and each board uses two clusters of three DSP chips. Similarly, Motorola's 962000 DSP chip has been used in a multiple-chip, parallel-architecture, high-performance VMEbus application developed in Europe.

One of the key elements that has distinguished the latest flurry of floating-point chips such as those from AT&T, TI and Motorola is the additional ports provided to allow

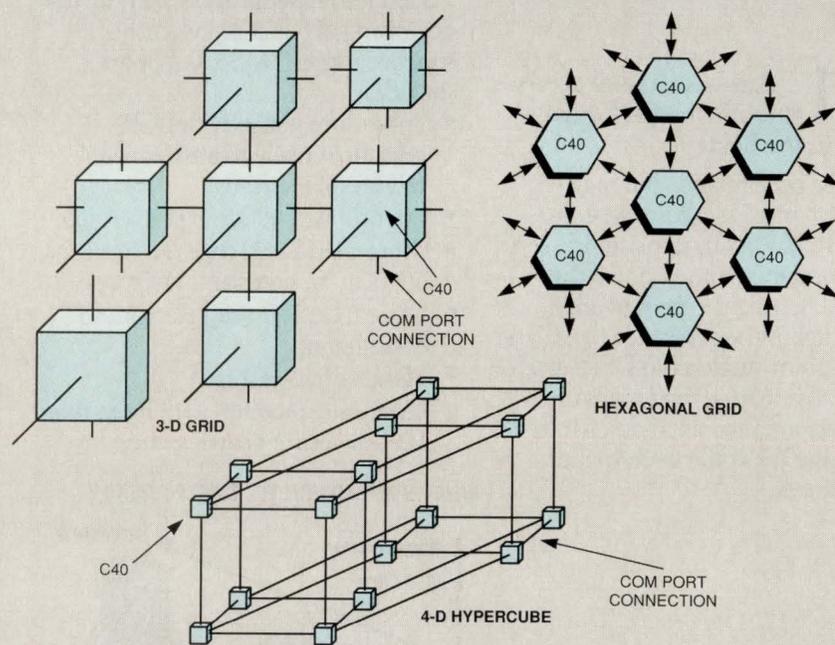
for multichip configurations. Motorola's chip, for example, has two 32-bit data and address ports in addition to serial ports. And most board-level implementations also bring out the processor ports for faster communications and to permit many boards to be tied together.

A step further

TI, however, has taken the idea of multiple ports for multichip parallel-processing configurations a step further in its C40, providing not only high-speed global and local buses but also a complete six-channel DMA controller and six communications ports. Even though more-conventional DSP devices boast as much as two complete sets of ports, the C40's data transfer rate of 320 Mbytes/s makes these devices look slow in comparison.

Each communication port allows for direct processor-to-processor or processor-to-memory communication at a rate of 20 Mbytes/s. The

CONFIGURATION OPTIONS FOR THE TMS320C40



In some parallel-processing configurations for the Texas Instruments TMS320C40, all six communications ports can be arranged in a hexagonal grid using a six-nearest-neighbor connection architecture, which is frequently used in numerical analysis and image processing applications. Alternatively, a three-dimensional grid could be architected for hierarchical processing used in image understanding and finite element analysis. Or, a four-dimensional hypercube could be arranged for more-conventional processing applications.

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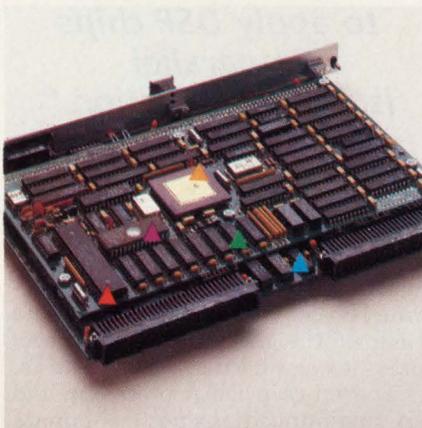
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communications channels are bi-directional and allow direct interconnection from one processor to another, greatly simplifying wiring.

According to Simar, the multiple ports give designers a great deal of architectural flexibility. For example, a parallel system can be configured as a pipelined linear array for performing such operations as correlations and convolutions; as a bi-directional ring with additional ports grouped for more I/O; as a tree structure supporting broadcasting and data structures for recognition tasks; or as a two-dimensional array for image processing.

Adding buses

Besides the six communications ports, the C40 includes both a local and a global bus. Using a combination of the communications ports and the two buses, designers have what Simar refers to as a "limitless variety of system configurations." For example, multiple C40s can be tied together, each with its own private local memory, yet sharing a larger global memory space. Alternatively, memory can be shared on the global and local buses. In addition, the communications ports can be programmed to off-load some of the traffic off the other buses to optimize performance.

The on-chip parallel DMA coprocessor contributes significantly to the chip's performance. The coprocessor provides concurrent I/O to maximize sustained performance over all six DMA channels. The DMA processor supports data transfers to and from anywhere in the chip's memory space as well as to and from the communications ports. To achieve the 75-MOPS rate TI boasts for the processor alone, the DMA processor performs three operations simultaneously within the 40-ns clock cycle. It handles a 32-bit data transfer and then updates the address register and transfer counter in a single clock tick.

But in total, the DMA processor contributes only a small portion of the 275 MOPS—the other 200 MOPS come from the chip's CPU. The CPU comprises a floating-point and integer multiplier, floating-point and integer ALU, 12 external precision registers, a pair of address generators, eight auxiliary registers

and 15 control registers. In operation, the CPU performs eight operations in each 40-ns cycle: a floating-point multiply, a floating-point addition, two data accesses, two address register updates, a zero-overhead counter update and a loop counter update.

While the chip boasts significant MOPS ratings, it also claims a very high data transfer rate as indicated—320 Mbytes/s. And while TI might not measure the data transfer rate in the conventional way, adding the individual transfer rates of each port does result in the sum of 320.

"Whether or not to apply DSP chips in parallel is a moot question."

—Ray Simar, Texas Instruments



Both the global and local ports provide 100-Mbyte/s transfer rates, and each of the communications ports provides an additional 20 Mbytes/s.

The on-chip DMA processor and six communications ports eliminate many of the traditional barriers to parallel DSP. Signals on the part can connect directly to the same pins on another processor for a simple, yet effective processing interface.

Development and support

TI has also had enough experience in the DSP business to realize the significance of development and support tools. For the C40, the first tools released focus on three key areas: code generation, hardware development and verification. First, like the C30, the chip will be supported by TI's ANSI-compatible optimizing C compiler only with a parallel processing run-time support library. The library will simplify development of algorithms for parallel processing by supporting key parallel operations such as message sending and receiving.

The compiler is also designed to optimize programs in several key areas. It takes care of global optimization and such loop optimiza-

tions as strength and reduction; it analyzes code to optimize memory and register variable usage; it searches out vector and matrix operations and maps memory access to chip addressing modes optimized for vector and matrix operations; and it produces fast and compact code for high-performance parallel DSP.

The assembler and linker provided for the C40 include directives for targeting program and data in a system. This is of particular significance since the assembler and linker are critical to manipulating program and data distribution in a parallel system.

Software behavioral models for the C40 are being developed by Logic Automation (Beaverton, OR). These hardware verification models are designed to let system designers simulate several chips in a parallel system along with simulating associated memory systems. The models are supported on most leading industry platforms, including Mentor's and Valid's.

Industry first

The C40 also boasts the first on-chip analysis module, which closely tracks and links the C40 activity with the company's in-circuit emulator. The embedded analysis function therefore monitors the overall operations of the chip and gives designers a visual report card on the device's behavior. The analysis module includes breakpoints for program address, data address and DMA address. It also permits any number of C40s to be single stepped individually or globally, halted and started simultaneously or independently. ■

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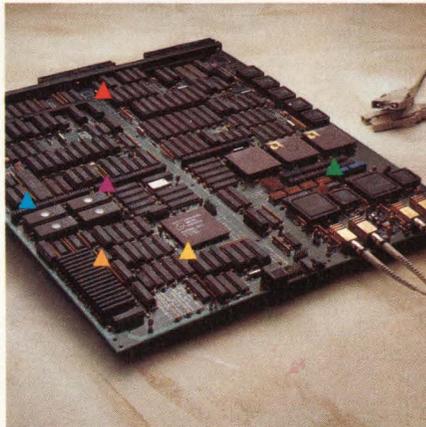
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Capturing video for desktop use

Ron Wilson, Senior Editor

Personal computers ought to have video inputs. At least that seems to be the belief of planners in the PC market, who point to a wide range of things you could do with them. You could analyze and edit images from a TV camera. You could add moving images to your presentations. You could watch the World Series in one window while running a simulation in another.

There is a common problem, though, standing in the way of all these applications. The composite video signal, as carefully worked out by standards committees over the years, is wonderful for stuffing synch, brightness and color data down the narrow channel of a broadcast transmitter and an inexpensive home receiver. But it isn't wonderful for interfacing to the crystal-locked, RGB world of computer displays.

As the idea of desktop video grows more attractive to systems developers, chip vendors from at least three different backgrounds are taking on the problems of harnessing composite video to the needs of desktop computing.

One group, traditional vendors of analog-to-digital converters, is looking to the desktop as a huge opportunity to sell medium-resolution flash converters. Other vendors traditionally involved in RAMDAC hardware for computer displays see video as a logical extension of their expertise in handling RGB signals. A third group, coming in from the increasingly digital world of consumer television, feels that it brings proprietary knowledge to the problems of working with digitized video signals.

The digitizing challenge

Even getting the video signal converted from its native analog into digital data is a complex problem. It might seem that all you need to do is insert a sufficiently fast A-D converter in front of the composite video signal and the job is done. Not so, according to vendors.

"There's no standard way to digitize video," warns Sergio Maggi, ap-

plications manager at A-D converter vendor Micro Power Systems (Santa Clara, CA). "Some people convert the composite signal directly and then separate the colors with software. Some people separate the colors as analog and then convert the individual R, G and B signals. It gets very hard to produce highly integrated parts because it's hard to know what the user wants."

Even once you decide on an approach, there are some unforeseen technical issues. "The biggest problem is getting a stable clock on the front end of your system," says Tom Kovanic, imaging product manager at Brooktree (San Diego, CA). Kovanic points out that the video signal may be coming from a nice stable camera, or from a VCR whose tape speed is wandering all over the place, or from a satellite receiver with challenging signal-to-noise specs. Under all of these conditions, the video-capture circuitry has to lock onto each line and digitize pixels from the right place in the signal.

The converter must be consistent—within at least one-fifth of a pixel width—in where it samples the video signal for each pixel. Otherwise the digitized image will show visible jitter. Worse, the jitter

will render many image-processing algorithms all but useless. So in addition to fast 8-bit A-Ds, vendors are starting to supply chips that lock onto the horizontal sync pulse in the video signal and parcel out pixel clocks based on the incoming horizontal line rate. Such chips are being provided by both Brooktree and Signetics (Sunnyvale, CA), a division of North American Philips, which developed the Signetics chips.

Dealing with color

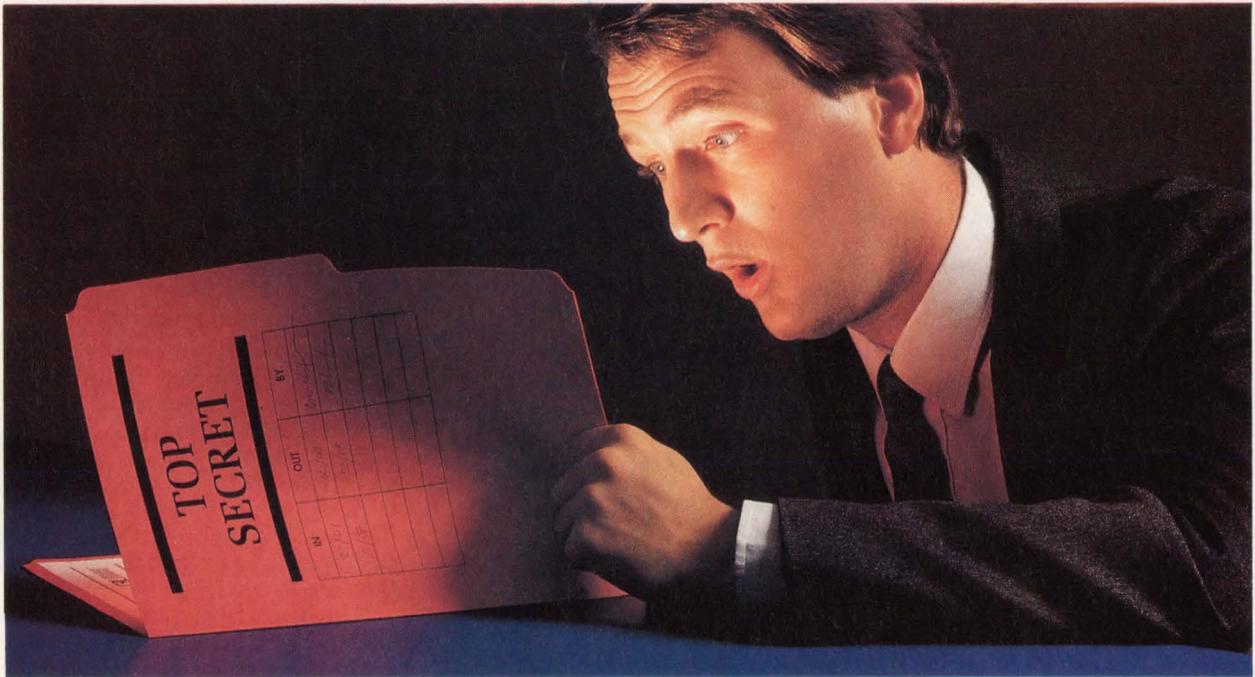
That would just about have the problem solved if we were dealing with monochrome signals. But the addition of color complicates everything. The color information in a video signal does not come in RGB form, but in the form of two signals—luminance and chrominance—that are encoded together in the composite waveform. Even getting the two signals out of the digitized video is an interesting exercise in signal processing.

Here Philips comes to the rescue with a series of Digital Multistandard Decoder (DMSD) chips with a range of cost and performance needs. Each of these devices takes in a stream of 8-bit digitized composite video and produces luminance, chrominance and horizontal and vertical sync at its outputs. The parts can shift automatically between PAL/NTSC and SECAM (sequential color and memory) video formats, and in most cases produce



Stephen Solari, imaging products marketing engineer at Signetics, argues that digitized video is a natural form of data for desktop computers. But capturing video signals and converting them to a form compatible with computer-generated graphics are non-trivial problems. Cost-effective solutions will have to come in silicon.

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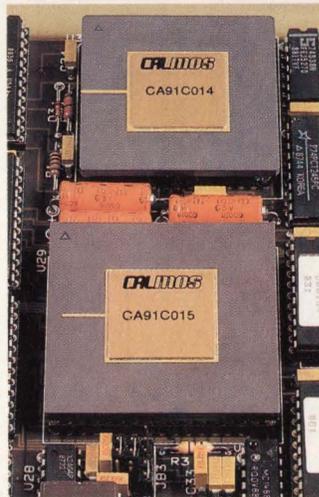
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CCIR601-compliant outputs.

It's in this process that Philips' experience in consumer television really comes to the fore, according to Stephen Solari, Signetics marketing engineer. He notes that a huge collection of tricks has accumulated in the TV industry as the market went digital, such as changing the filter profiles on the chrominance and luminance signals and coring the 8-bit values at the inputs to suppress high-frequency noise. These are built into the DMSD chips as register-controlled options, available for manipulation by an external microcontroller.

Once you've produced good, solid luminance and chrominance values for each pixel, the job still isn't over. Although the data may be in just the right format for image processing, it's still not compatible with the RGB format used in computer displays. So both Brooktree and Philips are offering format-conversion chips that can translate a data stream in real time between color formats. This lets the system maintain its frame buffers in whatever format is best suited to the processing being done. "You may want to translate

directly into RGB," says Kovanic, "because there's a ton of software based on that format. But it's not that great for image manipulation. So we provide translators to let you move between video spaces."

Once again, the problem isn't as

"People are already thinking of what they want to do with desktop video. Making it happen is a matter of technical issues that need silicon solutions."

—Stephen Solari, Signetics



trivial as it might seem. The basic translation between spaces is a simple matrix multiplication. But a small matter called gamma correction gets in the way. "The gamma curve is supposed to correct for the temperature dependencies of a picture tube phosphor," says Solari.

"Strictly, you need to take the gamma correction out of the color signal before you translate to RGB. Perhaps it's a nuance at this point, but our chips do it."

At the RGB conversion stage, both companies' chips also provide for input from other digital RGB sources. This lets the video be mixed with, for instance, computer-generated information from a VGA controller.

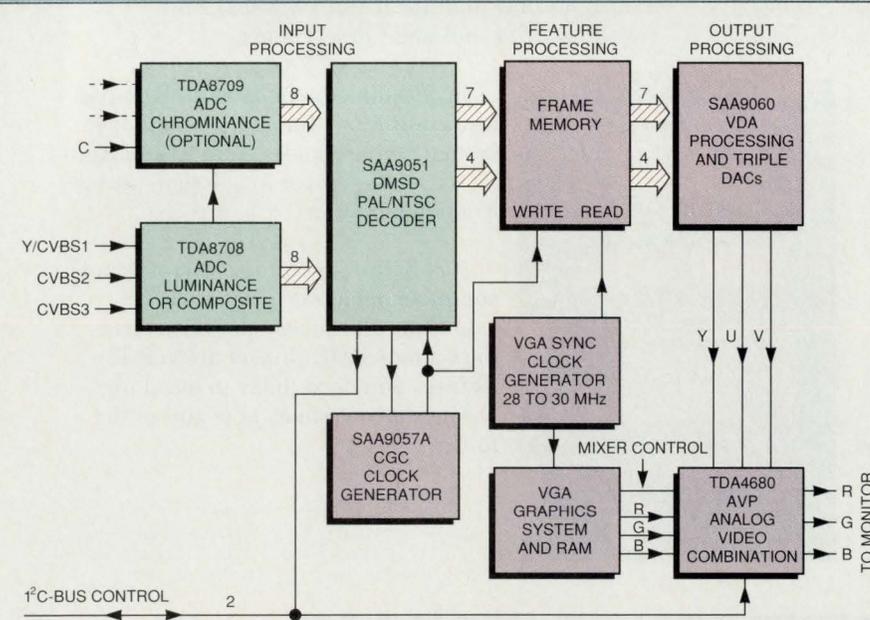
The integrated video PC

The level of integration demonstrated in the growing families from Philips and Brooktree not only shows that the companies take this market seriously but suggests the direction in which digital video capture is moving: from specialized hardware to highly integrated, low-cost boards to eventual inclusion in the core of the PC.

"Until recently, you've seen video capture just from third-party board vendors," says Micro Power Systems' Maggi. "But now IBM and Apple have stepped in with their own products—some of them using our flash converters. And when the solutions are down to one or two chips, expect to see them migrating to the PC motherboard."

Solari agrees on the direction. He sees the integration process as one of incorporating the algorithms that have already been developed in the world of analog television and eliminating the myriad of manual tweaks that were necessary in the analog sets. This should produce a family of very flexible, programmable video-manipulation components that can put the system cost into the right range. "Right now, people are already thinking of what they want to do with desktop video," he says. "Making it happen is a matter of technical issues that need silicon solutions."

PARTITIONED VIDEO DIGITAL DECODER



The Philips-Signetics approach to video capture partitions the pipeline into a few big chips. Here the process of digitizing, decoding and converting video for use with a standard VGA display system is implemented in a handful of special-purpose Philips devices.

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PLDs catch up to FPGAs in logic capacity and I/O

Barbara Tuck, Senior Editor

It seems no turf is secure in the ASIC market. Boundaries are becoming increasingly blurry as high-density programmable logic devices target the field-programmable gate array (FPGA) market and continue to compete with other high-density PLDs. In addition, both PLDs and FPGAs are going after a portion of the gate array business.

Two weeks ago, Altera (Santa Clara, CA) began shipping the densest member of its Multiple Array Matrix (MAX) 5000 EPLD family. With 192 macrocells and 7,500 equivalent gates, the 84-pin part is playing catch-up in complexity to FPGAs from Xilinx (San Jose, CA), Actel (Sunnyvale, CA) and Plessey Semiconductors (Scotts Valley, CA). And in answer to customer demands, Altera has increased the pin count by 50 percent over the 128-macrocell EPM5128, previously the largest MAX EPLD. The new 128-macrocell, 100-pin part, packaged in a quad flatpack, addresses register-intensive designs such as bus controllers. Users can expect an even higher density family of MAX parts later this month.

At the same time, Advanced Micro Devices (Sunnyvale, CA) is just beginning to ship the first member of its Macro Array CMOS high-speed, high-density (MACH) family of PLDs. The initial device has 900 gates and 32 macrocells. AMD plans to bring a 128-macrocell, 3,600-gate device to market by mid-1991, and then expects to double that density before the family runs out of steam.

Flexibility first

Altera's strategic marketing manager Stan Kopec claims that the two new MAX EPLD parts make the family compatible in density and I/O counts to layout-sensitive FPGAs. Moreover, he claims that "even when one takes into account the additive interconnect delays associated with the MAX architecture, the MAX family is 1.5 to three times faster than FPGAs." Altera MAX parts will

compete well with Xilinx parts, according to Kopec, since the MAX devices are "easier to design than the difficult-to-optimize logic cell arrays, which require many hours of compilation. Designers can have difficulty getting even 4,000 gates out of a 9,000-gate logic cell array." The availability of windowed erasable MAX parts presents an immediate advantage over one-time-programmable Actel parts, continues Kopec.

As for competition from the AMD MACH family, Kopec points out that

ns specified propagation delay. It can replace as many as 10 dozen SSI/MSI TTL packages, or two dozen conventional bipolar PALs. The 5192 has 384 shareable expander product terms, up to 72 inputs or 64 outputs and I/O tri-state buffers.

The 100-pin EPM5130 is a higher pin-count version of the 128-macrocell MAX part and is the first PLD, according to Altera, to be available in a quad flatpack. The 5130 has 20 dedicated input pins that allow high-speed input latching of 16-bit functions. One of these inputs can be configured as a synchronous system clock to provide enhanced clock-to-output delays for bus-oriented functions. The 5130 also has 64 I/O pins, eight in each logic array block, that can be configured for input, output



The 84-pin, UV-erasable EPM-5192JC MAX programmable logic device from Altera, in a windowed, ceramic J-lead chip carrier, has 192 macrocells and 7,500 gates. The EPM5130QC MAX part, in a one-time programmable plastic quad flatpack, pushes PLD pin counts to 100.

the MAX family has nearly a two-year head start on the MACH. "And the MACH devices have a stripped-down architecture for the highest speed and smallest size, resulting in an internal interconnect that's not nearly as flexible as Altera's," he claims. Kopec questions the efficiency of the MACH architecture for integrating anything more than low-density PALs and 22V10s. "Because of routing problems, designers will be able to use only 20 or so of the 32 macrocells in the new MACH110," he says.

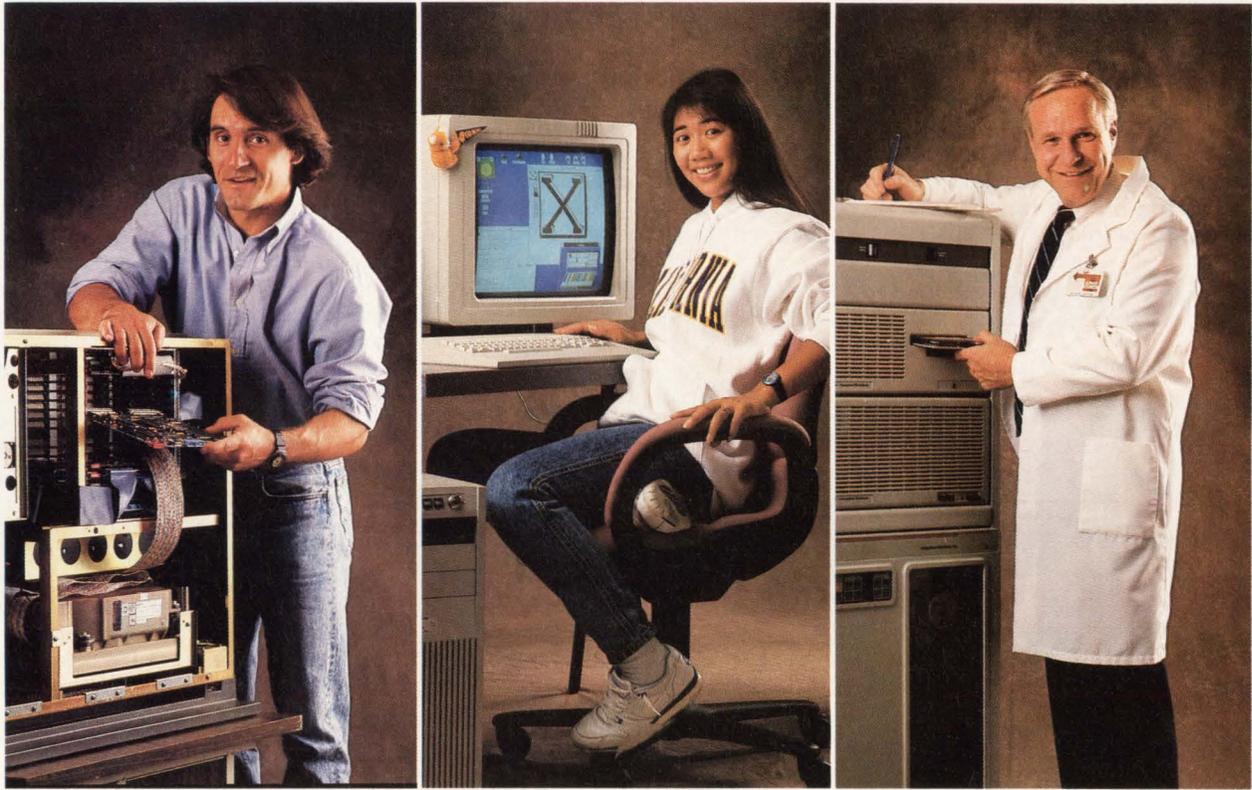
Altera compares the density of its 192-macrocell part with the Xilinx 3090. The new EPM5192 MAX device provides 1.5 times the density of the company's 128-macrocell EPM5128, yet provides the same 25-

or bidirectional data flow. Dual feedback on the I/O pins provides the most efficient use of the device's pin resources.

Other features of the new chip are a 25-ns propagation delay, 256 shareable expander product terms and synchronous clocking for fast clock-to-Q delays in bus-oriented functions. Both MAX devices support 50-MHz clock rates for registered logic functions such as counters and shift registers.

Though Altera claims an advantage over the variable/cumulative delays encountered with conventional channel routing in FPGAs, Kopec admits that Altera's own Programmable Interconnect Array, which connects the multiple logic array blocks, can indeed involve

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more than a single uniform delay. "But whereas a Xilinx FPGA, once routed for a 16-bit counter, will probably be derated to between 15 and 20 MHz," claims Kopec, "a MAX part will be derated to the 30-MHz-plus range." One way a designer can stack up delays with the MAX parts is by relying on the innovative Altera logic expanders to get the most

out of the parts' resources.

Although AMD's MACH family is coming to market later than Altera's MAX, AMD director of marketing for programmable logic Andy Robin reports "tons of design wins" for the MACH devices from customers "waiting for higher speed." With a 15-ns propagation delay, the MACH parts will be twice as fast as 30-ns

MAX parts and 40 percent faster than 25-ns parts. Plus, they'll be half as expensive as MAX parts, claims Robin.

Though both MACH and MAX architectures are globally interconnected, the programmable interconnects are radically different, according to Robin. The MACH interconnect lets designers route from any macrocell to any other macrocell and incur no more than the predictable worst-case speed in all applications requiring up to 12 or 16 product terms per macrocell, explains Robin. The AMD programmable interconnect, a switch matrix, does involve a 1- or 1.5-ns delay, but AMD buried that delay within the 15-ns delay.

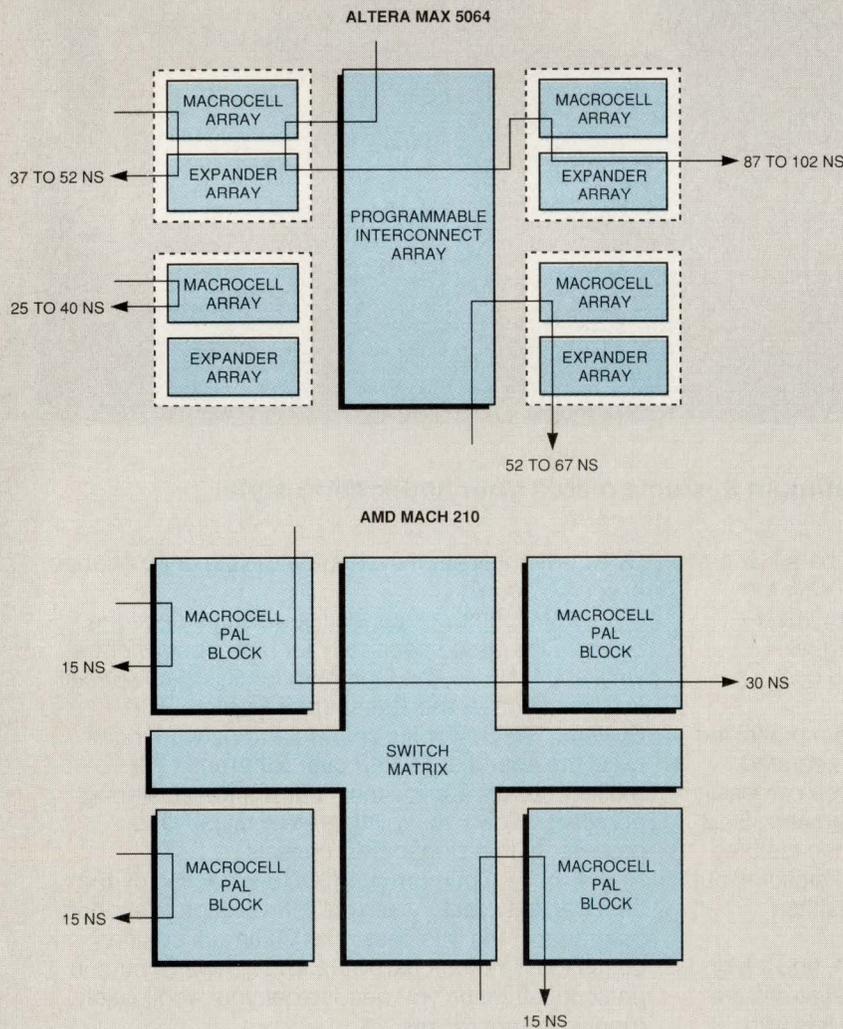
The MAX interconnect, on the other hand, while giving the designer greater flexibility, says Robin, involves about a 13-ns delay and also takes up a lot of die area. If MAX users require more than three or four product terms, they pay the cost of an additional delay for using logic expanders. And if they need more than seven inputs and have to go through the Programmable Interconnect Array, they'll incur yet another delay.

Three times the logic

The 44-pin MACH110, the first member of the AMD CMOS MACH 1 family, has approximately three times the logic macrocell capability of the popular PAL22V10, claims AMD. Each of two PAL blocks contains a 64-product-term logic array, a logic allocator, 16 macrocells and 16 I/O cells. The logic allocator takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 12 product terms. Altera claims that AMD's use of the logic allocator to compensate for sparseness of logic—four product terms per MACH macrocell compared with seven product terms plus two expanders for each MAX macrocell—helps one macrocell boost its logic capability to the detriment of adjacent macrocells.

A switch matrix in the MACH110 connects the two PAL blocks to each other and to all input pins. It feeds the PAL blocks with 22 inputs, which makes each block look effectively like an independent PAL-

HOW MAX COMPARES WITH MACH



Both the Altera MAX and the Advanced Micro Devices MACH programmable logic device architectures are globally interconnected, but the interconnect schemes are radically different. Though speed is dependent on the application, the 48-macrocell MACH210 operates at 15 ns when using up to 16 product terms. When using more than 16 product terms, the part operates at 30 ns. The 64-macrocell MAX EPM5064 PLD, on the other hand, could range from 25 to 67 ns, depending on the combination of paths. Though the combination of paths with additive delays of 87 to 102 ns is a possibility, Altera says that its software would find such delays unacceptable.

INTEGRATED CIRCUITS

22V16. Each macrocell provides either registered or combinatorial outputs with programmable polarity, and all macrocells can be connected to an I/O cell.

The next MACH device to be shipped will be the 15-ns, 64-macrocell 210, the first member of the MACH 2 family. It will let designers use up to 16 product terms per macrocell without a change in timing delay. According to Robin, the MACH architecture will allow AMD to expand to 128 macrocells comfortably without increasing the 15-ns propagation delay. The MACH family will eventually be extended to about 7,200 gates, predicts Robin.

■ Jostling for position

AMD doesn't expect its MACH devices to face competition from either Plus Logic (San Jose, CA) Plus Array devices or International CMOS Technology (San Jose, CA) Peel ar-

rays. The story may change if Plus Logic, which has a strategy of surrounding fixed portions of high-speed logic with programmable logic, moves from 2- and 3- μ m to a faster technology, says Robin. The ICT Peel arrays, in the 45- to 50-ns range, will be more competitive in the medium-density market.

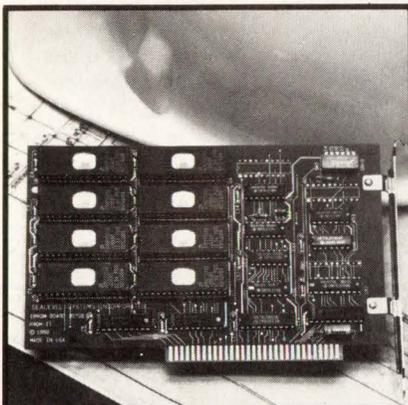
What AMD expects to happen is that MACH and MAX devices will compete at intermediate densities, and that FPGAs, though slow and unpredictable at lower densities, will be relied on for scaling up to about 50,000 gates. Meanwhile, both high-density PLDs and FPGAs will capture a portion of the gate array business.

At this point, high-density PLDs are a step behind FPGAs, FPGAs are a few steps behind gate arrays and gate arrays are merging with standard cells. With boundaries blurring as technologies blend to-

gether, the opportunity for ASIC designers to explore various technologies within a universal design methodology increases. And competition will help make vendors more responsive to designers' demands for easier migration from one technology to another. ■

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Dedicated DSP chips carry high-performance applications

Warren Andrews, Senior Editor

Though general-purpose digital signal processors have shown dramatic increases in speed and algorithm complexity over the past few years, many emerging DSP functions are calling for even higher performance of relatively common algorithms. Microprocessor-based DSP devices simply don't have the power to handle the sampling rates required in applications such as very-high-speed modems and digital receivers. And when arrays or multiprocessor designs are brought to bear on such designs, they're fraught with high chip counts and partitioning problems.

In response to these needs, the industry has developed function-specific DSP chips targeted at DSP algorithms associated with particular applications. The latest in the emergence of such specialized chips is a family of DSP devices from Plessey Semiconductor (Scotts Valley, CA) designed to solve coherent digital transmission and receiver system problems. The new chips include a 20-MHz, 16×16-bit multiplier, a high-precision, direct digital synthesizer—billed as the industry's first with an on-chip in-phase/quadrature (I/Q) splitter—and a family of finite impulse response (FIR) filters.

These new devices, says Plessey marketing manager John Vigilante, aren't necessarily intended to replace general-purpose DSP chips, but rather to be an adjunct to them in high-performance transmission and receiver systems. "The new parts have a tremendous amount of computational power," says Vigilante. "One of our FIR chips, for example, has the equivalent computational power of 16 TMS320C25s when harnessed to do the same task."

High bandwidth signals

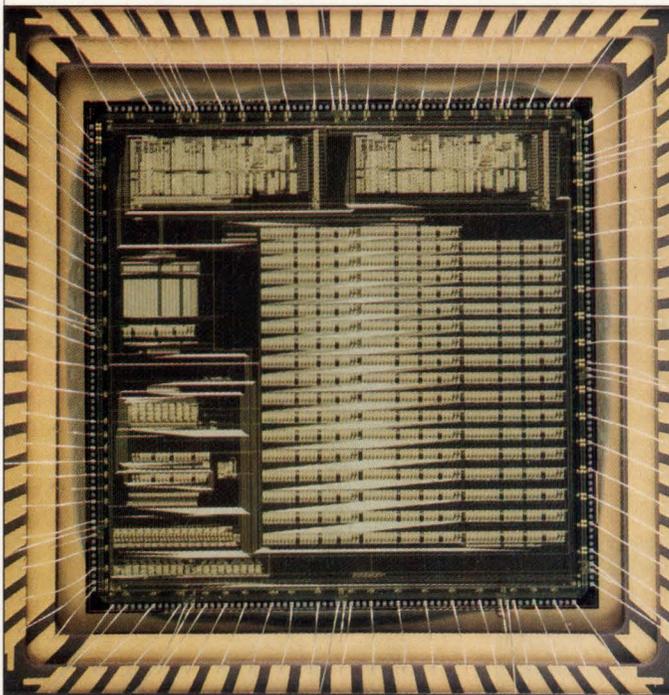
The new family of Plessey DSP devices is designed to handle sampling rates up to 20 MHz, with signal bandwidth exceeding 1 MHz. Rates

such as these are often required in digital communications systems, radar, sonar, telemetry and spectrum analysis. The Plessey devices are geared to manage the front end of such digital receivers, allowing the back-end processing to be handled by more conventional microprocessor-based DSP devices. Coherent processing of such high-bandwidth signals requires fast iterations of complex-number arithmetic.

To best understand the function of

channel is shifted 90 degrees in phase from the other channel. This precise 90-degree phase shift is a primary requirement for unambiguous time measurements, the key to coherent systems.

Compared with an equivalent analog circuit using a voltage-controlled oscillator and quadrature hybrid mixer, or splitter, the digital solution provides faster frequency shifting, a more accurate center frequency, finer frequency resolution, a purer frequency spectrum and better stability. In addition, the 16350 offers a better third-order intercept figure, better linearity and far better 90-degree phase offset tracking across frequency and amplitude than are possible with purely analog techniques.

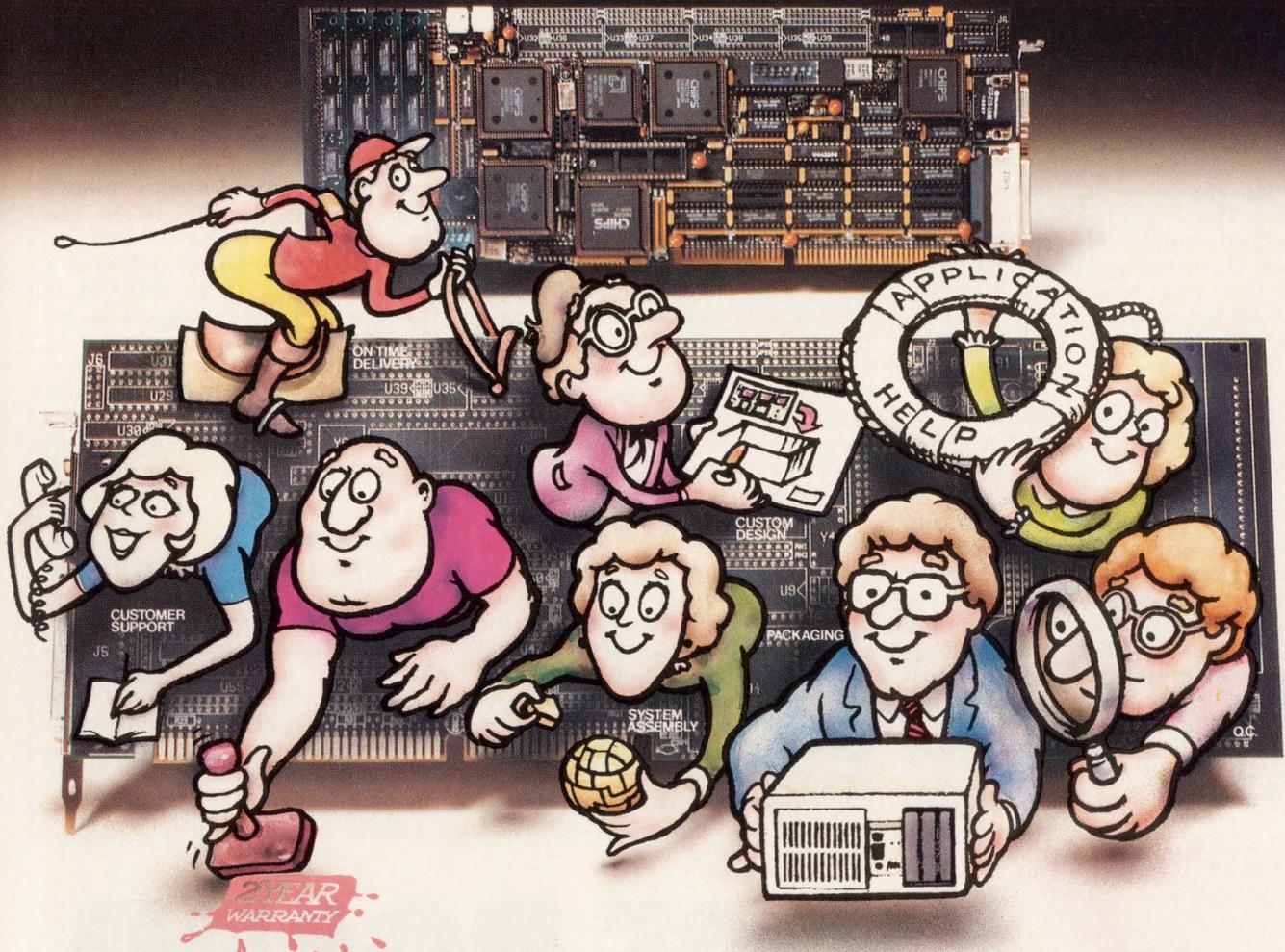


Plessey Semiconductor's PDSP16350 high-precision direct digital synthesizer with 34-bit phase accumulation and 16-bit amplitude precision is fabricated in 1.5- μ m CMOS. Because the part is made as a gate array, a shrink to a more advanced 1- μ m technology will be almost seamless and will allow close to double the current 20-MHz sample rate.

Plessey's chips, however, it's easiest to look at a digital receiver and see the functions performed by the various components (see figure above). At the front end, after an appropriate analog-to-digital conversion, the PDSP16350 with on-chip I/Q splitter handles the translation of the desired bandwidth from an intermediate frequency to baseband, and into the commonly called I and Q, or the real and imaginary components. The resultant I and Q signals are in fact the same signal, except one

The 16350 can also adapt to a wide range of other applications, including use as a numerically controlled oscillator, quadrature signal generator, AM/FM or PM modulator, constellation generator or synchronous demodulator. The chip itself comprises a high-precision direct digital synthesizer with 34-bit phase accumulation and 16-bit amplitude precision, in addition to the on-chip I/Q splitter.

Another of the key elements in Plessey's trio of high-performance



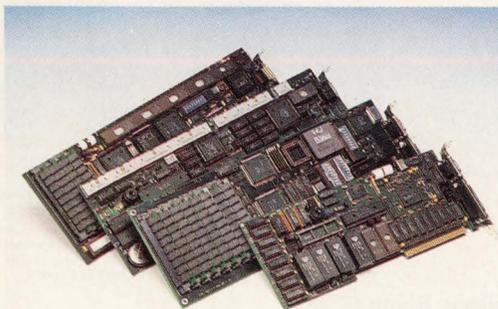
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DSP chips is the upgraded version of its 16x16-bit high-speed multiplier. The PDSP16116A can multiply two complex (16x16-bit) words every 50 ns and can be configured to output the complete complex (32x32-bit) result within a single cycle. The data format is fractional two's complement.

Handling analog functions

Plessey's PDSP16256 FIR filter takes over the analog functions of filtering in successive stages of a receiver. In the receiver application, the chip filters out unwanted frequency components from the down-converted signal and handles the decimation (reduction in sample rate) of the digital data stream to let lower performance processors (such as more conventional, microprocessor-based units) operate at a rate that won't overwhelm their processing capabilities.

The 16256 is made up of 16 com-

plete 16x12-bit multiplier/accumulators that can be multicycled to provide from 16 to 128 stages of digital filtering at sample rates from 2.5 to 20 MHz. In the 16-tap mode, the device samples data at the 20-MHz system clock rate. If a lower sample rate is acceptable, the number of stages can be increased in powers of two up to 128. Each time the number of stages is doubled, the clock rate is halved with respect to the system clock rate. The chip can also be configured either as one long filter or two filters with half the number of taps in each.

In the digital-receiver application, the 16256 was illustrated only in its most simple application. In the digital-receiver chain, additional functions such as matched filtering, pulse compression, coherent convolution, chirp-z transforms, phase-lock loops, correlation and convolution may be necessary and can be implemented with the 16256 by

modifying the filter coefficients and inventive interconnection schemes.

Coefficients for the 16256 are stored internally and can be downloaded from a host system or a simple EPROM. If an EPROM is used, no additional support is required, letting the part be used in stand-alone applications. A full set of coefficients is then automatically loaded at power-on by the chip or at system request. A single EPROM can provide coefficients for up to 16 devices.

Just the beginning

The PDSP16350 and PDSP16256 provide only the rudiments of the receiver front end, and many additional processing steps may be required at a high bandwidth. One such step could be the addition of frequency translation of the signal to a new frequency. In this case, a PDSP16116 works with the 16350. The main difference is that the sig-

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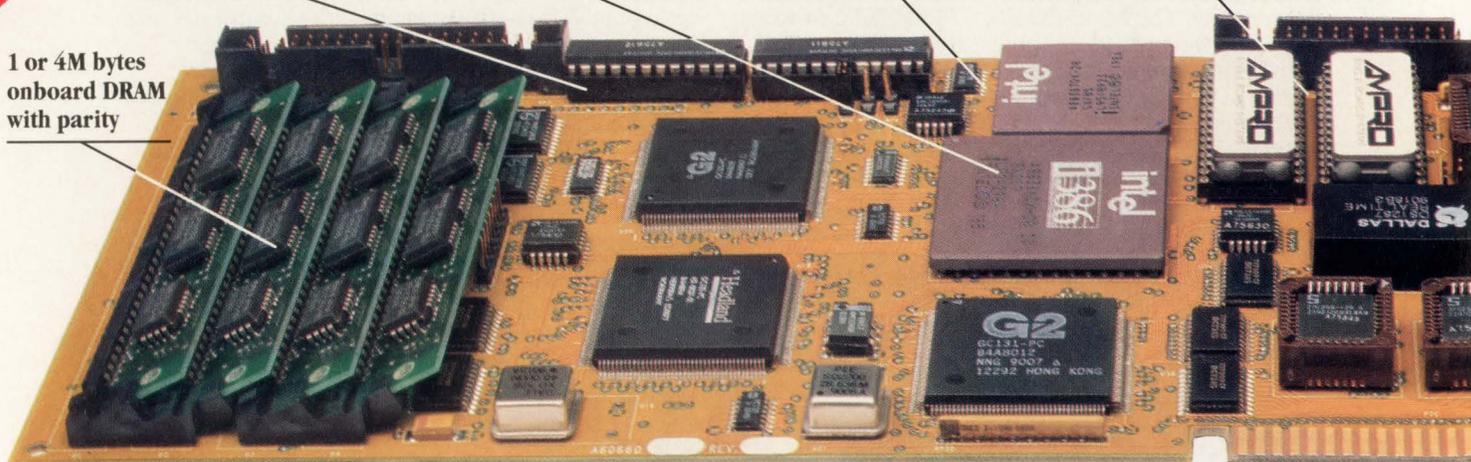
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nal is now complex and requires four real multipliers to step through the translation, as opposed to the two required when doing the more elementary I/Q split. The 16116 complex multiplier also provides a single pin for complex conjugation, necessary when performing modulation or rotation algorithms.

The examples mentioned above only begin to exploit the complexity of digital receivers, according to Vigilante. The addition of other existing and/or emerging high-performance DSP components will satisfy other needs.

Additional channelization may be necessary for detection problems over a wide bandwidth, Vigilante adds, which can be handled by a soon-to-be-announced FFT processor (PDSP16510). This dedicated FFT chip is designed to perform up to 256 complex-point FFTs at a sustainable sample rate of 10 MHz. Once again, the chip uses a data flow

approach, allowing its inclusion with no external memory.

More and faster

Though general-purpose devices tend to focus on narrow bandwidths with increasing algorithm complexity, Vigilante sees an increasing need for DSP devices that implement more common algorithms at a higher sample rate to handle available media bandwidths. The Plessey DSP product family is geared to provide that type of performance and, according to Vigilante, is just the beginning of a growing line of increasingly higher performance products.

"Our current family of chips is made in Plessey's 1.5- μ m CMOS process, giving it the 20-MHz sample rate required for many of today's systems," says Vigilante. "But today's systems require even wider bandwidths. Plessey plans to shrink geometries to about one micron in the near future, practically doubling

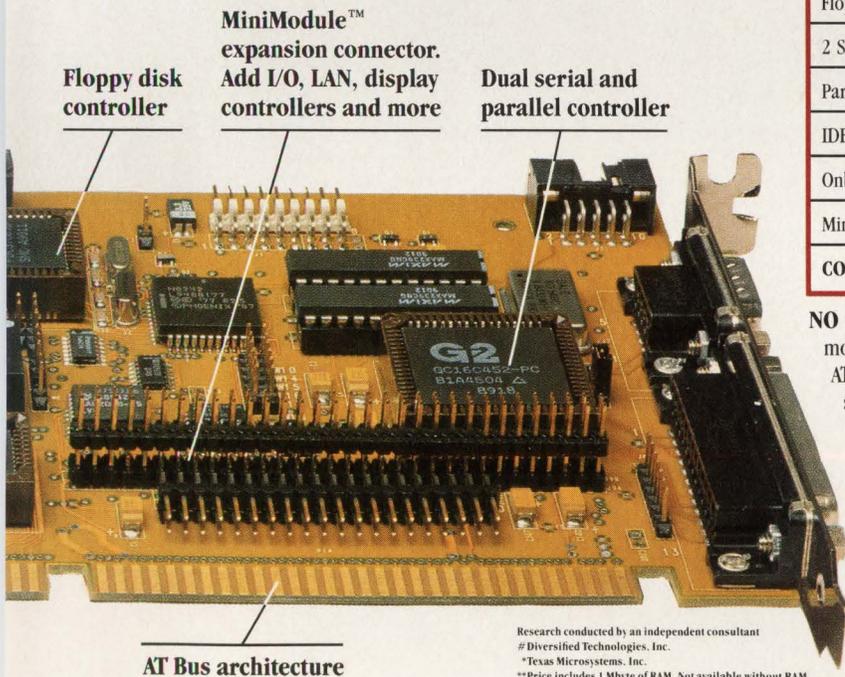
the effective sampling rate."

The key to the performance of the Plessey chips, Vigilante says, is through architectures using many computational resources on a single chip. Several multiplier/adder pipelined stages, for example, are cascaded to implement specific functions such as demodulation, down conversion, filtering or detection. This data flow architecture—compared with architectures such as the more common Harvard type—restricts the range of algorithms due to the dedicated interconnect scheme, but provides the highest possible performance available from given hardware resources. ■

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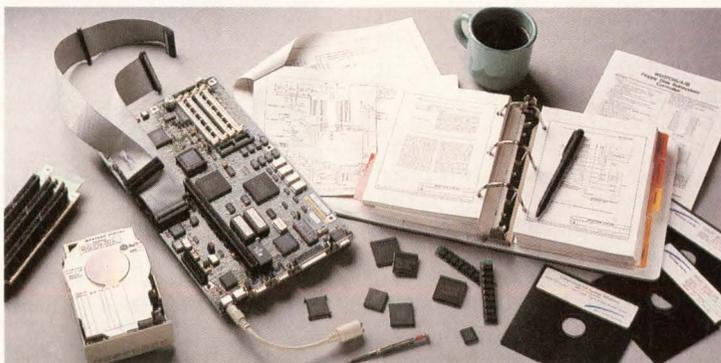
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High-speed PCBs pose problems for timing analysis tools

Mike Donlin, Senior Editor

Today's high-performance circuit boards demand tightly packed traces running between custom, semicustom and standard high-speed CMOS devices. The effects that such complex designs produce—namely, ringing, crosstalk and reflection—can cause clocking and triggering problems and system-crippling glitches. Unfortunately, most tools that predict and analyze these problems are run after the layout is finished, a trait that separates them from the front end of the design cycle. The perfect analysis tool would allow a designer to analyze, correct and back annotate high-speed timing and transmission-line effects into the layout tool, before the prototype stage. Such a tool would eliminate extra prototype cycles, which directly affect a product's performance, cost and time-to-market.

"What people are doing today is hanging logic analyzer probes all over a prototype and that's certainly not a complete, worst-case evaluation," says Pat Wolfram, marketing product manager at Mentor Graphics (Beaverton, OR). "Today's multilayered boards and fine-pitch circuits are making that kind of analysis almost impossible."

The primary problem a designer faces when analyzing circuit board timing is getting data that accurately reflects how a board's components will behave in a real operating environment. Timing analysis data can't be too optimistic, or potential problems will be overlooked. On the other hand, an overly pessimistic set of parameters will tag false timing hazards and place undue restrictions on the final design.

Noise impedes performance

Today's high-speed components only complicate matters. Reflections caused by anomalies in transmission lines may cause false triggering, thus forcing the designer to redesign the board to accommodate lower clock rates. In any case, performance is sacrificed. Most design-

ers prefer to route these critical paths by hand, but as circuit boards employ more and more high-speed devices, hand routing is consuming an inordinate amount of the design

"Gate delay, etch delay and settling time must all be taken into account for accurate timing analysis."

—Shiv Tasker, Valid Logic Systems

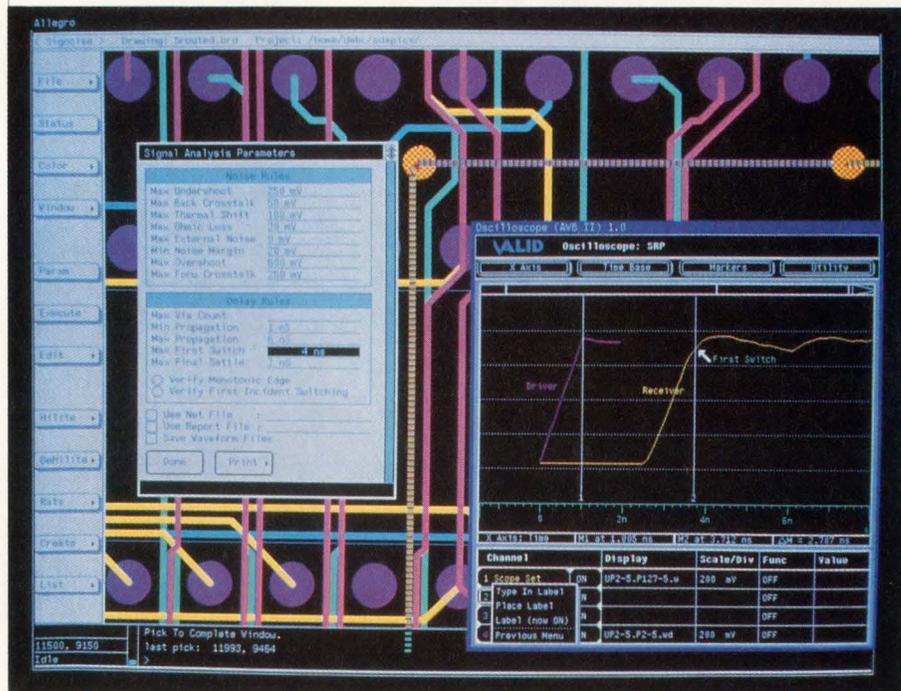


cycle. Better timing data, even for postlayout analysis, would help predict prototype performance.

"Most timing analysis tools on the

market look at schematics and use the gate delays between different components to try and define the critical paths," says Shiv Tasker, director of product marketing at Valid Logic Systems' printed circuit board division (Chelmsford, MA). "That approach doesn't take into account other elements that affect timing. In addition to gate delay, there's etch delay and settling time, each of which must be taken into account for accurate timing analysis."

Once this timing information is defined, it can be used to set limits on a postlayout simulation before the critical prototype phase. "In a circuit where a driver goes from zero to one, the receiver should be ready after a certain amount of etch delay," says Tasker. "But sometimes there isn't sufficient drive, so the signal goes halfway and lingers there before it ramps up. A designer needs to know that there's insufficient drive and that it may be necessary to look at the whole network—a major fix that would require changing the whole design. Finding something like that after routing is a lot better than finding it after the board has



Valid's signal integrity tool, SigDelay, analyzes high-speed circuit board signal transmissions for the timing effects of logic transitions. Here, though the maximum allowable propagation delay is only 3.4 ns, the receiver pin doesn't change states until 4.0 ns. The offending signal is highlighted in the Allegro layout tool, and the corresponding waveform is displayed within Analog Workbench.

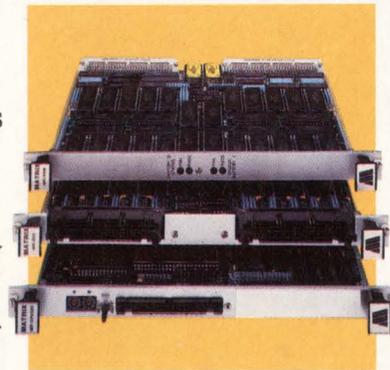


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been fabricated."

To solve the high-speed signal delay problem, Valid has just unveiled SigDelay, a timing analysis tool that's part of the Allegro PCB design system. SigDelay works directly with Valid's Signal Noise Analysis Tool, which lets users make simultaneous detailed analyses of high-speed board characteristics such as crosstalk, thermal shift, reflections and ohmic loss. It uses the transmission-line simulation results provided by the Signal Noise Analysis Tool to analyze the speed and smoothness of the signal. SigDelay then verifies length and delay constraints that may have been established on the signal, and uses RapidSim, Valid's high-speed digital simulator, to extract the minimum and maximum pin-to-pin delay data for postlayout timing simulation.

Recognizing this need for physical timing data in the preprototype stage of board design, Mentor Graphics has teamed up with Quad Design Technology (Camarillo, CA) to provide pin-to-pin delay calculations from Quad's transmission-line and crosstalk analysis tools. Though Mentor is currently referring ac-

counts that require high-speed circuit board design tools to Quad Design, plans are in place to incorporate the analysis tools into Mentor's Concurrent Design Environment by the end of this year. The Quad toolset includes the Pre-Route Delay

"There's nothing available today that can evaluate the vector set and determine if the tool is exercising all the timing paths."

—Pat Wolfram, Mentor Graphics



Quantifier, which evaluates component placement and calculates signal interconnect delays in circuit designs; the Transmission Line Calculator, which simulates transmission-line effects in conductors such as cables, backplanes and traces; and the Crosstalk Tool Kit, which predicts the effects of signal

coupling on system performance.

Though the analysis tools from Quad Design and Valid give designers critical information before the circuit board layout is committed to prototype, the ideal situation would be to extract timing analysis information before simulation. Then the placement of components would be an informed task instead of one that relies solely on the experience of the designer.

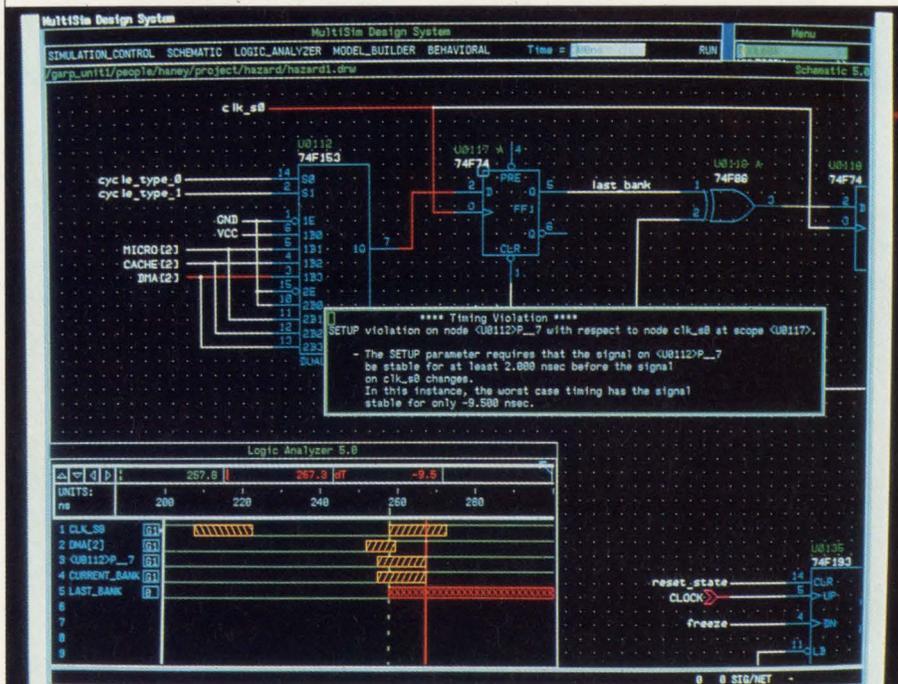
"Design verification has traditionally been a back-end process," says Brian Miller, product marketing manager at Teradyne (Boston, MA). "But that's becoming impractical as designs get more complex. A tool that merely points to a problem in a design is inadequate. There might be 20 paths that lead to the affected circuit, and they might affect 20 other paths. It's time-consuming to weed through all the possibilities."

One solution would be to bring postlayout information into simulation, but there are no standard interfaces for layout systems to communicate delays to the simulator. "We're working on a graphic display that would highlight which paths caused timing hazards," says Miller. "Ideally, you'd like a warning in simulation that would tell you, for instance, that there's a set-up violation on certain pins. Then a description would point out what the violation was, what paths caused it and what pads were affected."

■ The best solution

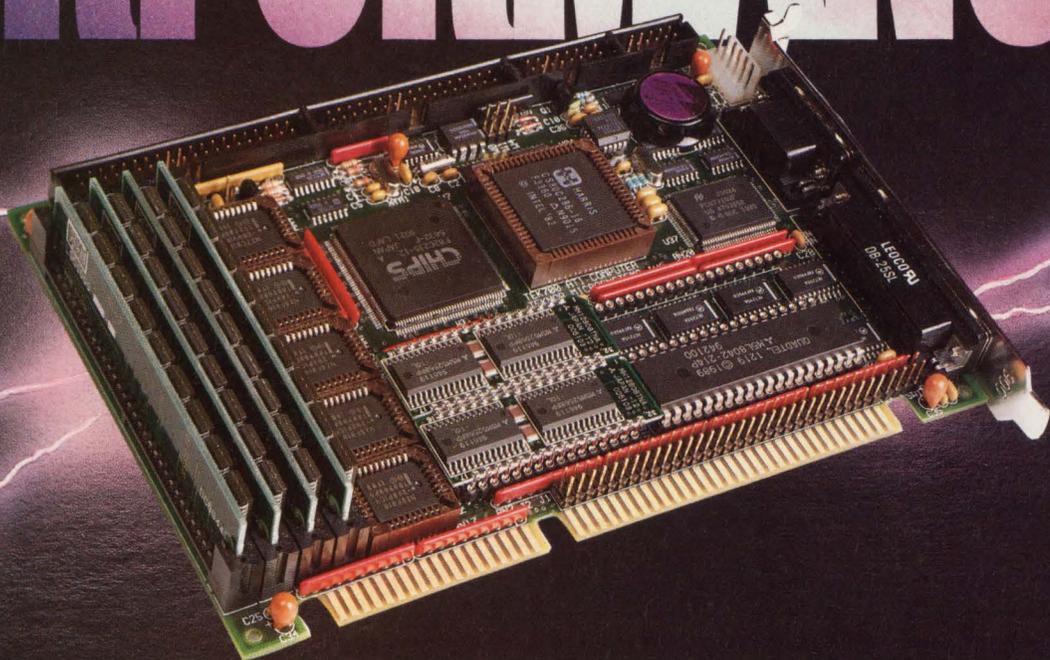
Right now, the best solution rests on supplying timing analysis data to static and dynamic timing analyzers, though the results can be misleading unless there is tight integration of data to analyzer. "A static timing analyzer is going to be pessimistic because it has to assume worst-case performance," says Mentor's Wolfram. "It looks at every path, and that means it might report on a lot of paths that aren't of any concern."

To avoid producing pessimistic results, static analyzers need control logic to determine which paths are valid, as well as adequate test vectors applied to the parts under analysis to ensure that they're in the right delay mode. A DRAM, for example, will have a different delay if it's in a read/write mode than if it's



Worst-case timing analysis capabilities in Teradyne's MultiSim Interactive Designer help identify subtle timing problems that don't show up in hardware prototypes. In this example, the set-up parameters require the signal to be stable for 2.0 ns. Worst-case timing shows the signal stable for -9.5 ns.

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in a read/modify/write mode. "Dynamic timing tools would solve this, but they have a downside," Wolfram points out. "If they don't have a robust vector set, they might mask paths that should be examined. There's nothing available today that

can evaluate the vector set and determine if the tool is exercising all the timing paths. The ideal analyzer would be a combination of static and dynamic capabilities."

The hope, therefore, is that timing analyzers will be able to give ade-

quate data to designers for use in prelayout simulation. The key is keeping the analyzer as flexible as possible, so that neither too many nor too few timing hazards are flagged. "Our approach with our Veritime timing analysis tool is to provide enough case-analysis capability," says Chris Brawy, product marketing manager at Cadence Design Systems (San Jose, CA). "This gives a designer the chance to describe the parameters in which a circuit will operate. As long as you do that, you can get an accurate analysis with few false hazards."

Relief in sight

Until the ideal solution is developed, designers will have to be content with tools that point out potential timing hazards for postlayout verification. Products are on the horizon, however, that promise relief. Racal-Redac (Westford, MA) is set to release its High Performance Engineering EDA system later this year. Users will be able to specify delay, crosstalk and reflection limits on the schematic, and these delay parameters will be automatically converted to spacing rules. Racal-Redac's Visula placement system will then position components close enough to achieve the desired delays, and the autorouter will rip up traces that exceed delay specifications.

Though the day when accurate transmission-line effects and timing analysis data can be plugged into a simulator isn't yet here, the processes are creeping closer to the top of the design cycle. And as system frequencies approach 20 MHz and beyond, the need for this capability has never been more critical. ■

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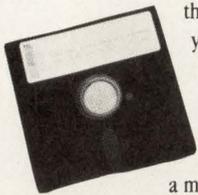
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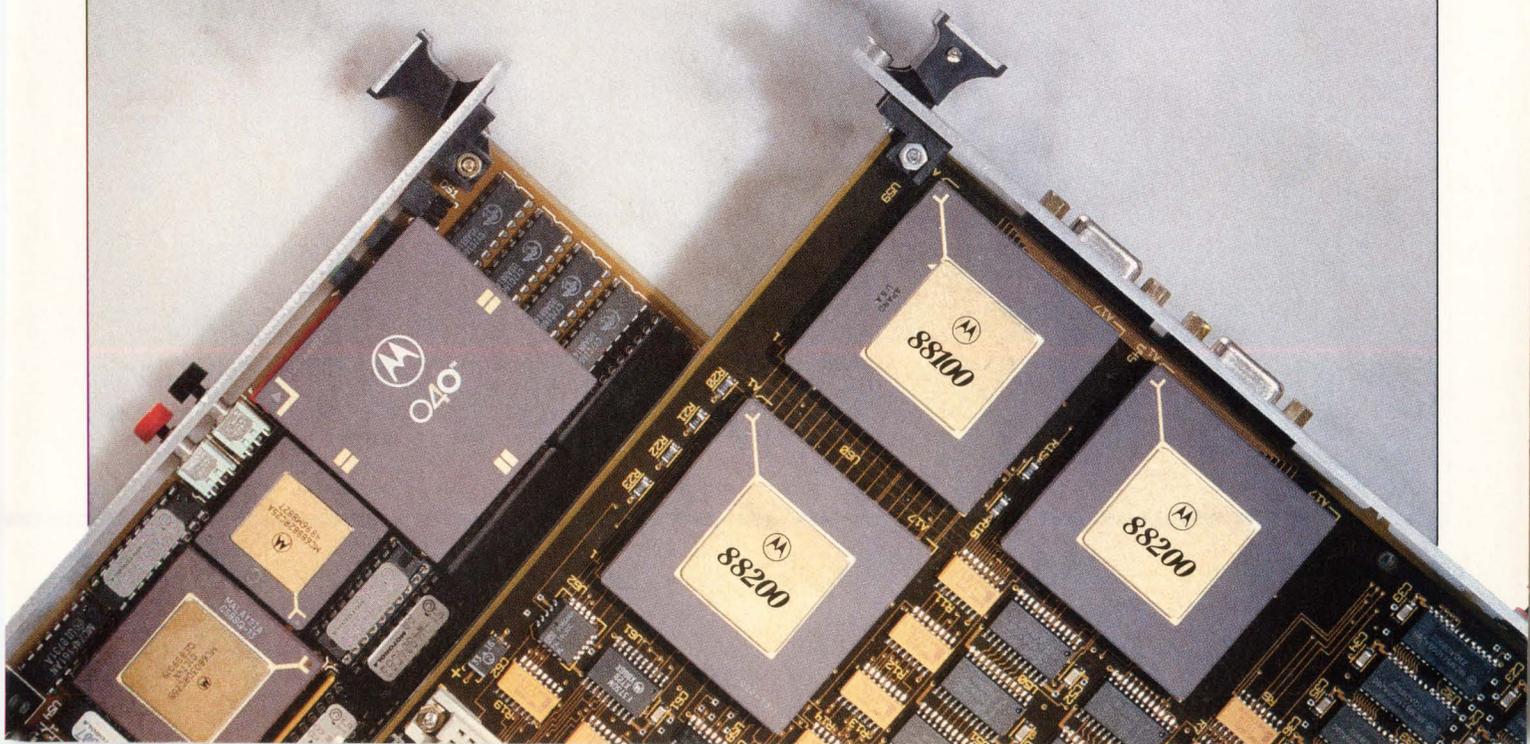
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Forth engine accelerates VME response time

Warren Andrews, Senior Editor

Though VME single-board computers based on conventional RISC and CISC processors and associated software are doing an increasingly better job of responding to real-time events, latency times for the processor to respond to such things as interrupt requests are often too slow. It can take many clock cycles for a processor to acknowledge an interrupt, and even more to initiate a response. In critical systems, this timing can be crucial.

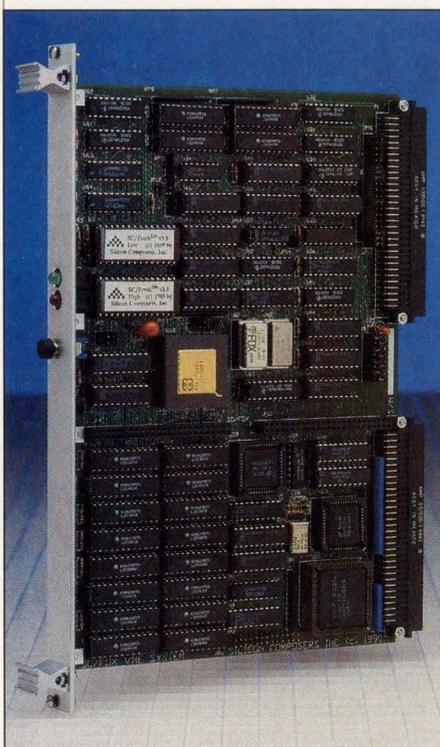
Knocking down latency time to as little as a single clock cycle for normal operation, and four cycles for worst-case operation, hasn't been possible with conventional micro-coded processors. But by using a hardware engine that directly executes a high-level language and executes several instructions simultaneously, a 12-MHz processor from Harris Semiconductor (Melbourne, FL) was able to run routinely at 18 Mips with bursts up to 60 Mips. The key to this performance lies in the power of the RTX 2000 Forth engine.

The new board, now offered by Forth system and software developer Silicon Composers (Palo Alto, CA), combines the Harris Forth engine with memory and I/O to provide a compact, fully VME-compatible single-board computer.

"The Forth engine really excels in real-time control applications," says Silicon Composers president George Nicol. He reports that the RTX 2000 can respond to an event in a single clock cycle, which translates to 100 ns at 10 MHz and 83 ns at 12 MHz. A similar response from a conventional processor can take many machine cycles just to service an interrupt routine.

Additional performance and flexibility come to the board's interrupt structure with SC/Forth, Silicon Composers' version of Forth. A single SC/Forth command, for example, can assert any of the seven VMEbus interrupts and pass a full 16-bit vector to the VMEbus. The interrupt handler first services an interrupt

with release-on-acknowledge, and then maps the interrupt and interrupt acknowledge to E12 of the RTX 2000, while the AC fail signal is mapped to the nonmaskable interrupt of the RTX 2000.



Silicon Composers uses the power of Harris Semiconductor's RTX 2000 processor with its own version of Forth on a VME board to provide high-speed performance for real-time applications. The combination of the Forth engine, which can directly execute a high-level language, and Silicon Composers' SC/Forth language allows for the simultaneous execution of multiple instructions, letting a 12-MHz board operate at 16 Mips routinely and in bursts of up to 60 Mips.

Called the SC/Fox VME, Silicon Composers' board represents the company's first foray into the VME marketplace, as well as the first emergence of Harris' Forth engine on the bus. Silicon Composers took

care to see that the board complied with all the VMEbus rules to serve as either a master system controller or a slave. The board includes such functions as IACK daisy-chain driver, system clock driver, bus time-out timer and bus arbiter for all four bus priorities enabling maximum system flexibility. In addition, the board transfers data by words or bytes to ease system integration into a variety of systems.

In a board of this type, the availability of a processor interface is significant in that it lets users prototype using Forth technology for ultimate use in an embedded application or custom boards.

To allow straightforward I/O interfacing, all RTX 2000 signals are carried out to two 50-pin expansion headers on the board. With the optional SC/VME PROTO prototyping plug-on board, application-specific hardware can be added directly to the board and, if required, interfaced to the P2 connector of the VME board.

Processor performance key

"The key to the performance of the board is the RTX 2000 with its 14 prioritized interrupts," says Nicol. Following an interrupt request, the board responds in between one and four clock cycles. The return to normal operation takes zero clock cycles, giving it a large advantage over more conventional processors in returning to normal operation.

Another differentiating factor of the RTX 2000 over conventional processors is a private processor bus that Harris calls its ASIC Bus. This bus is made up of eight channels of 16-bit I/O, which allows the processor to input and output data rapidly. "Data can be acquired at a 24-Mbyte/s rate over Harris' ASIC Bus," says Nicol. "In addition, the processor has a 16x16-bit on-chip parallel multiplier that provides a 32-bit result in a single clock cycle."

While the hardware resources are significant, the Forth language capability really differentiates Silicon Composers' product from the masses. Unlike conventional processors, which run machine code compiled from a higher-level language, the RTX 2000 directly runs Forth language code.

"Running SC/Forth, the board is

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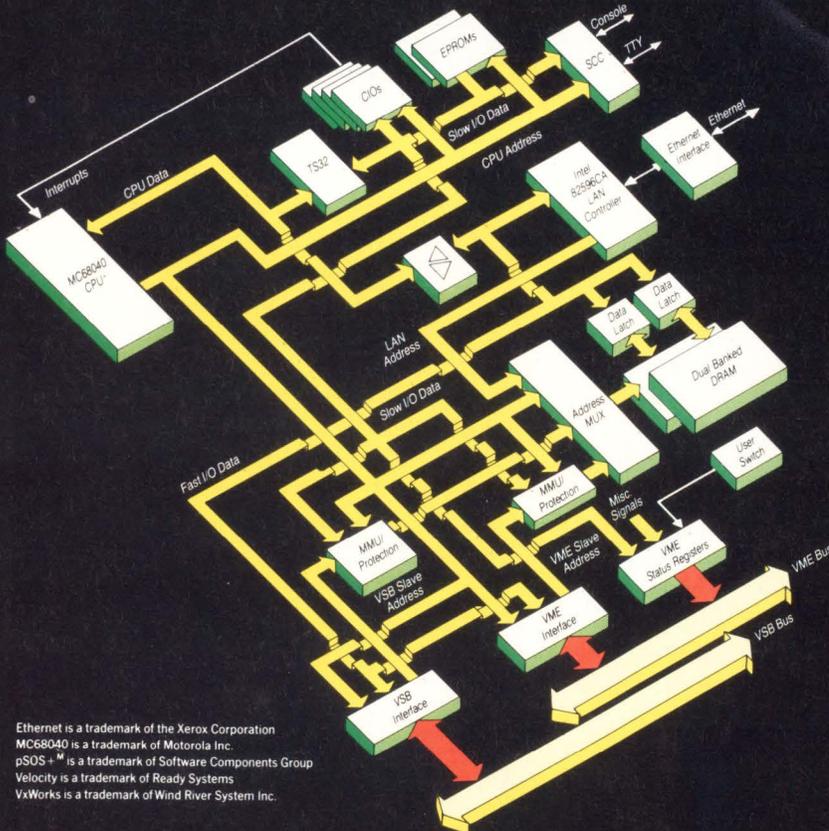


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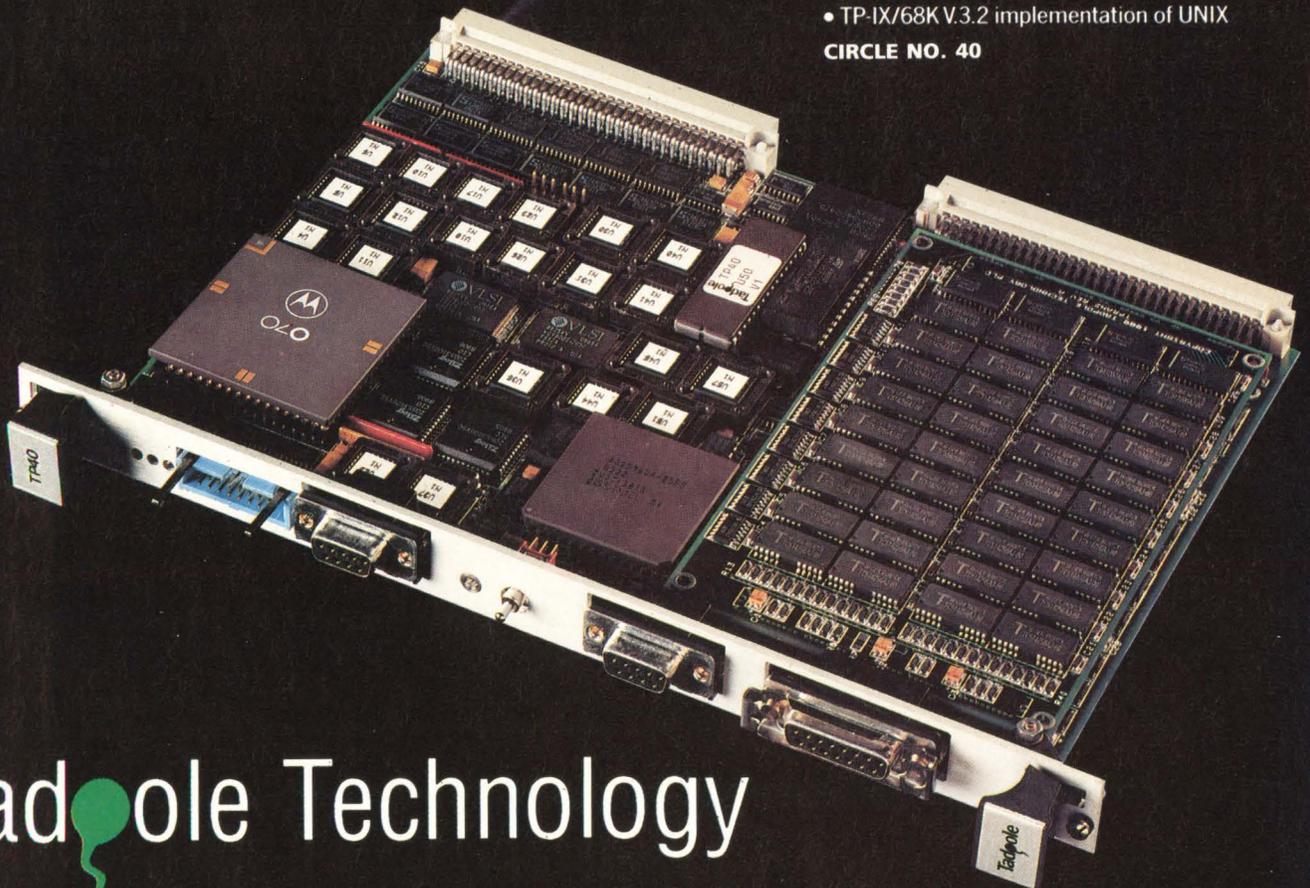
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able to achieve sustained performance of 18 Mips for a 12-MHz clock," says Nicol. "SC/Forth speeds operation by executing multiple instructions per clock cycle. In this way, the processor is able to achieve burst speeds of up to 60 Mips.

SC/Forth takes full advantage of the RTX 2000 instruction set by automatically optimizing multiple Forth primitives, such as OVER SWAP-, into single machine-cycle instructions, permitting far higher speeds than are normally achievable."

The RTX 2000 is a stack-oriented microprocessor whose instruction set resembles the high-level language Forth. According to Nicol, the language can be easily learned by a competent programmer in a matter of hours, and programming in Forth is considerably easier than in other high-level languages.

Forth not always a plus

"But the same things that make Forth relatively easy to program in also make it tough to maintain," says Ed Rathje, vice-president of JMI Software Consultants (Springhouse, PA). Rathje says that Forth tends to be very programmer-specific and relates horror stories of code having to be totally rewritten because the original programmer was no longer available to explain it.

While Rathje is quick to point out a negative aspect of Forth, he also admits that it has advantages. Obviously, in an engine such as the Harris RTX 2000, there are some performance advantages for certain applications, such as those calling for lightning-fast interrupt response time. And, he says, for prototyping and in small operations Forth can be a quick way to get an operation up and running with good performance.

Forth has been around for well over a decade, but despite its ubiquity, there are still few commercial or industrial Forth applications compared with those for languages such as C, Pascal and Fortran.

Undoubtedly Silicon Composers' board will find some applications in areas where fast real-time performance is required and programmers are willing to learn Forth. Despite its superior performance in many areas, though, it's likely to gain only limited application until the company releases a C compiler, which is being developed now. Design engineers remain a relatively conservative group that tends to stick with known approaches. ■

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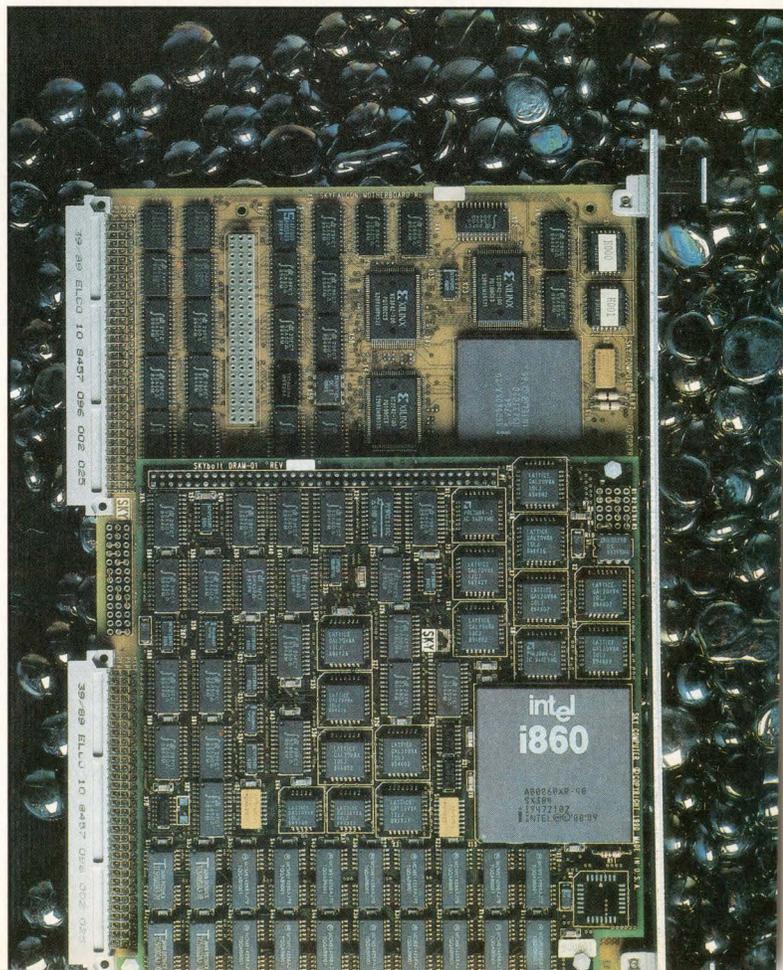
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CIRCLE NO. 36



SOFTWARE

On-chip test logic aids emulation of complex processors

Tom Williams, Senior Editor

The increasing complexity and speed of microprocessors present a challenge to real-time software developers who need emulation capability for debugging—namely, how to look at the internal machine states that aren't accessible via normal pins. The status of internal pipelines, caches, memory and so on is often hidden from the user, but it's needed by the programmer to track down software problems.

Some manufacturers have provided in-circuit emulation (ICE) modules and special bond-out versions of their processors to allow access to the internals for emulation. This method allows true real-time emulation, but it can be a burden because of the extra pins and the huge ICE modules involved. It becomes truly unwieldy when one is trying to debug a multiprocessor system. Just getting a number of ICE modules plugged into multiple boards that are themselves plugged into a card cage is often virtually impossible.

A different strategy, being pursued by Texas Instruments (Dallas, TX), uses the logic originally built into the chips for testing purposes, along with some extra logic to control the processor to give programmers access to the internal machine state. The testability logic works by halting the processor and then scanning out the state of all the internal gates over a serial line. The same logic can be used to read the contents of registers, caches and pipelines and can then be used by a debugger to correlate the internal state of the processor with the assembler listing or high-level source code of the program.

Using scan-based emulation

TI calls this technique scan-based emulation. Although it doesn't give the full benefits of true real-time emulation—such as hardware breakpoints and buffering—it does let programmers halt execution on software breakpoints and extract

the status of the processor.

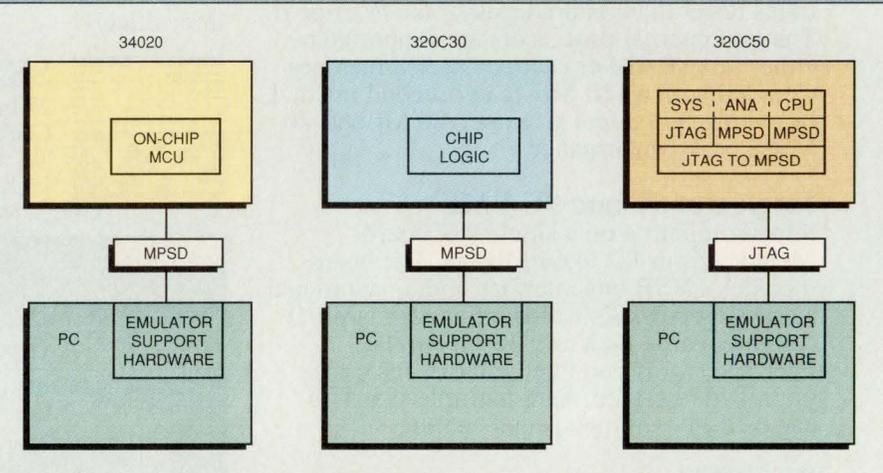
Equally important, it lets multiple processors be chained together for multiprocessor emulation without the cumbersome use of huge ICE pods. Scan-based emulation uses only four extra pins with no software or ROM-based monitor or other processor overhead. It can thus be used for field service in installed equipment as well as for application development.

One can start and stop the processor on any given clock cycle, for instance, but when it's halted in emulation mode, it will execute all the instructions remaining in the pipeline. Programmers must consider this when setting software breakpoints. You can't run the processor one clock cycle at a time and see what all the flip-flops are doing in real time, but you can single-step it and have access to all the registers and internal states once you've halted the processor.

The modular port scan device

The interface to this control and scanning logic is through TI's proprietary modular port scan device (MPSD) interface. MPSD provides a

THE EVOLUTION OF EMULATION



For chips designed before the JTAG/IEEE protocol was finalized, Texas Instruments uses its own modular port scan device (MPSD) interface to access internal processor states. For the 34020, MPSD talks to the on-chip microcontroller. For the 320C30, it directly scans the chip logic. On later processor generations, the JTAG protocol allows boundary scan of the processor pins, as well as scanning of internal states via an interface to MPSD.

TI got started on scan-based emulation with its TMS320C30 digital signal processor, according to Tony Coomes, TI DSP development system manager. By adding some extra control logic to the scan-chain circuitry used for testing, "We now have total control over the processor through our own private port," he says, "and we can see every individual flip-flop and register in the device, including the memory."

There are certain caveats associated with scan-based emulation.

serial interface to a single chip. A similar interface is used to provide emulation for TI's newest graphics processor, the TMS34020, but the emulation doesn't use on-chip testability logic. Instead, it sends commands to the processor's on-chip front-end microcontroller to shift out the internal state. Thus, via a MPSD interface, the same kinds of commands give emulation capability to both parts, albeit in a slightly different manner, based on their architectures.

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SOFTWARE

The advantages of scan-based emulation appear to be so appealing, however, that TI is working on a more standard method of implementing it on its newer generations of processors. And TI's approach may prompt other manufacturers to provide access to internal machine states that could ease the way for more general-purpose debuggers and compilers to work with different

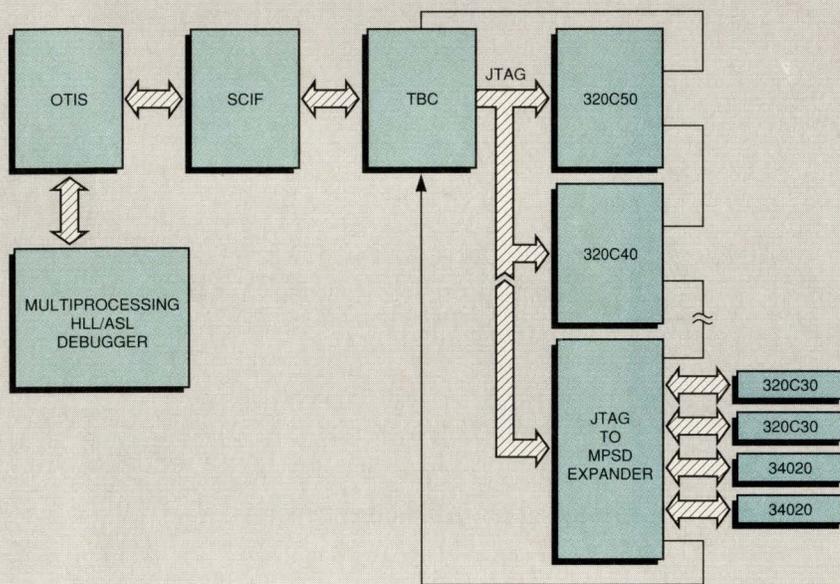
while MPSD is designed to get information about the gate-level status of an IC. Boundary scan on a microprocessor or DSP chip looks at the information available at the pads on the edge of the die—for instance, the same information that's available at the pins. But boundary scan can retrieve the information nonintrusively via the four-wire serial port. Thus, with a JTAG controller on-

etary internal logic could conceivably use a JTAG front end to allow emulation.

While the chip internals can only be scanned when it's halted, the JTAG controller can be monitored when it's running, so there's access to the status of the processor's pins via the boundary scan. The only problem is that JTAG is an asynchronous-type interface that runs at a clock speed other than that of the processor. This suggests that some useful real-time debugging is possible if one can correlate the state of the JTAG controller with that of the processor's pins in time—a task that doesn't appear to be supported by any current debuggers.

The use of JTAG suggests a possible way around the bond-out issue as well. One could bring bond-out pads to the periphery of the die without having to bring external pins out of the chip. Boundary scan could then provide internal register, cache and pipeline status as well as information on the user-accessible pins. Whether this could be done and could provide for true real-time emulation is still unclear.

MULTIPROCESSING EMULATION IN SCOPE



In a Scope environment, the high-level language or assembly language debugger talks to the system via the Otis interface standard, which calls processor-specific primitive target interface (PTI) commands to implement the scanning functions. The serial controller interface (SCIF) communicates with the test bus hardware. 320C40 and 320C50 DSP chips can be daisy-chained directly via their on-chip JTAG interfaces. Earlier processors such as the 320C20 and 34020 require an ASIC-based JTAG interface to their MPSD ports.

processor architectures.

For the newest family of DSP chips—the TMS320C40 and 320C50—and future designs, TI is marrying the Joint Testability Action Group (JTAG)/IEEE-P1149.1 protocol format with its own internal MPSD. Under this approach, commands can be sent to a chip in standard JTAG format and be converted to MPSD to extract internal processor information.

JTAG was originally conceived for doing boundary scan for highly integrated board testing, says Coomes,

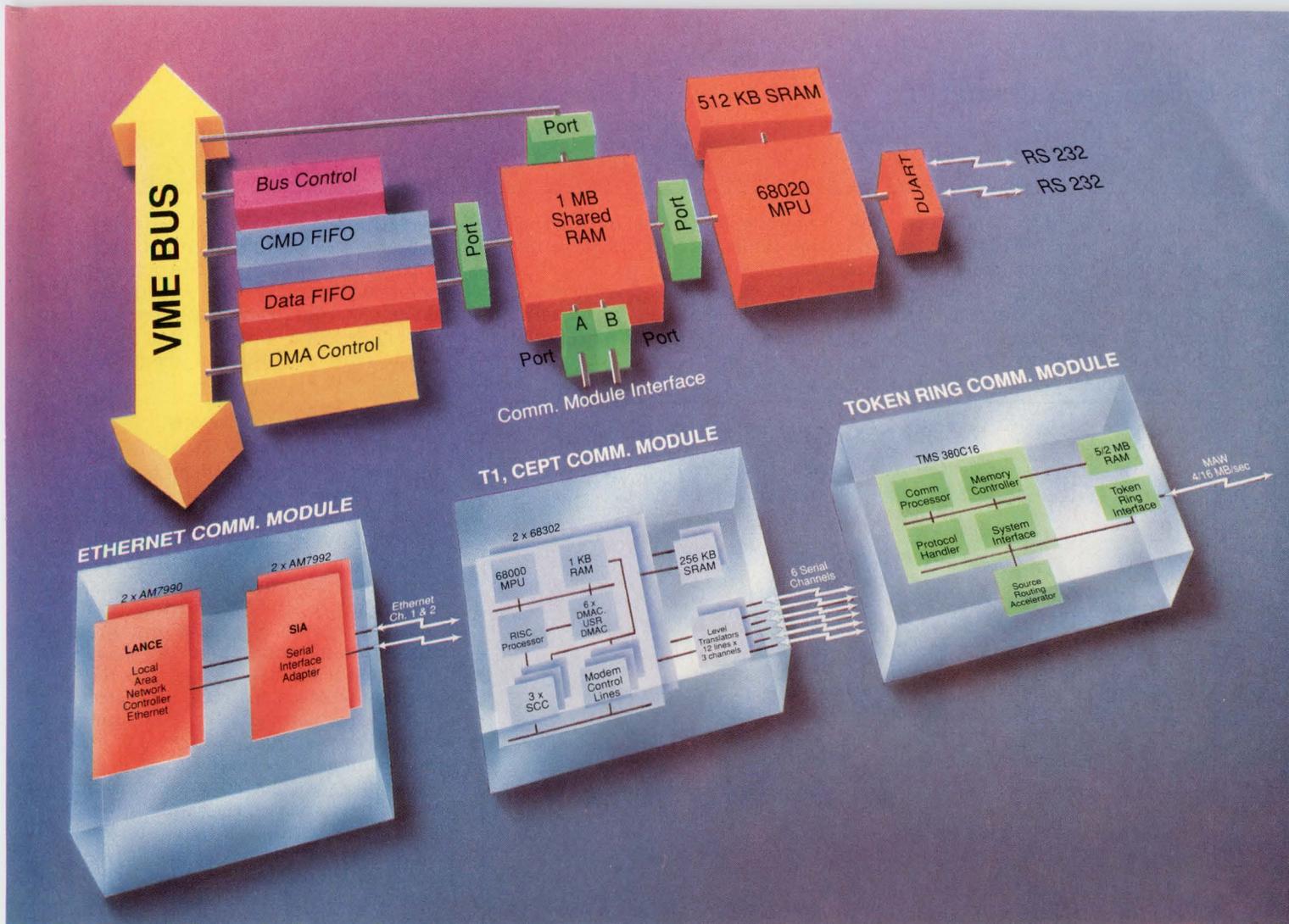
chip and a JTAG-to-MPSD interface, programmers have access to both the states of the pins (via boundary scan) and all internal state information (via MPSD). And they have both levels of that access via an IEEE standard protocol.

"It's not just JTAG that makes emulation work," says Coomes. "You must have the internal logic that lets you single-step the processor, set breakpoints and stop the processor." And you must have the logic to scan out the information. Other processors with different propri-

Emulating multiple processors

"The nice thing about JTAG vs. MPSD is that JTAG lets you serially connect devices on a chain," says Coomes. To scan the information out of a series of processors, the scan-out of one device goes to the scan-in of the next in a daisy chain until all the information reaches the user working on a host system. On a JTAG ring, it's possible to halt one processor and let others run, and to mix and match processors with the same interface. For devices such as the 320C30 and the 34020 that don't have the JTAG interface built in, an ASIC- or PAL-based JTAG-to-MPSD expander can be used to connect to the MPSD end of several devices and to present a JTAG interface to the rest of the development environment.

The multiprocessing emulation environment has evolved from TI's system controllability/observability partitioning environment (Scope)—the company's comprehensive design-for-testability framework. "Emulation came because we had built the testability logic into the circuit and realized that there were



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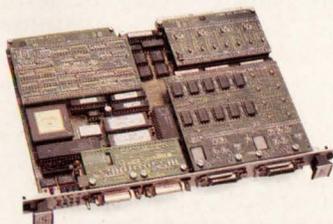
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SOFTWARE

other uses for it," Coomes says. "We expanded from MPSD to JTAG and took the hit on silicon die size just to provide emulation." Scope provides connectivity and software interfaces to let the user stop the processor(s), extract the information and look up

compiler-generated data in the symbol tables so that it can be used by a debugger.

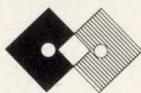
Scope provides three levels of software to let a debugger talk to a processor or set of processors connected in a JTAG ring. The open

target interface standard (Otis) is a set of processor-independent software functions such as read memory and write memory. Otis shields the debugger from needing to have specific knowledge of how to scan information into and out of a given processor.

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Second level of software

Below Otis is the primitive target interface (PTI), which does hold all the knowledge on how to scan the 320C30 and the 320C40 to get valid information. Since MPSD is a test protocol, it knows about flip-flops. Programmers aren't test engineers; they want to look at registers, not individual gates. PTI helps organize the gate information in a way that's meaningful for debugging. The debugger accesses a given processor via Otis, which calls the PTI functions. For instance, to carry out an Otis command to modify a value in memory in a 320C30 system, PTI would have to scan the value into a register, scan the address into another register, scan the proper instruction into an instruction register and then tell the processor to execute.

A third software layer is the serial controller interface (SCIF), which is essentially a device driver that communicates to the hardware test environment via an ASIC called the test bus controller.

TI has developed compilers and debuggers for its graphics and DSP processors that use the common object file format (COFF) for their symbolic information. The use of COFF and the JTAG standard suggest opportunities for third-party software tool vendors and development system vendors, and also a way for manufacturers of complex RISC and CISC processors to provide a level of emulation without expensive and cumbersome hardware systems.

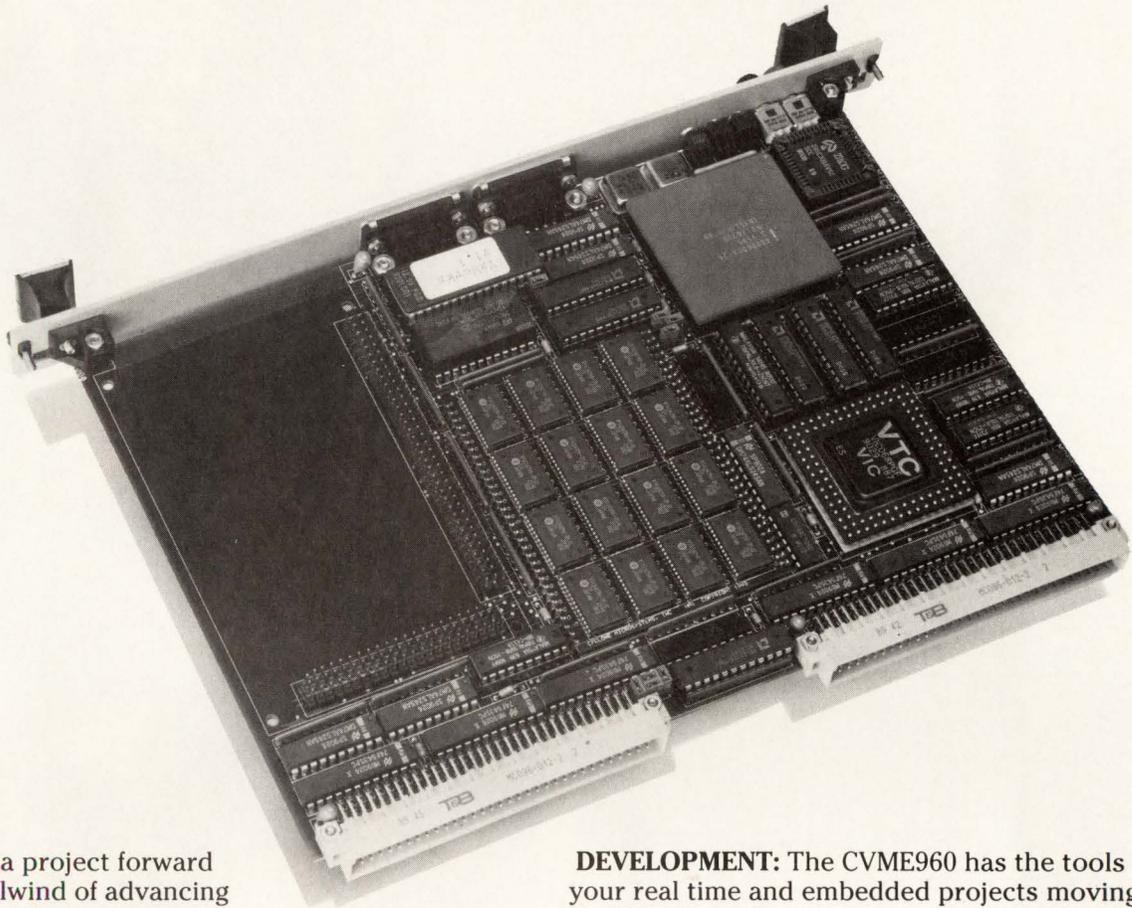
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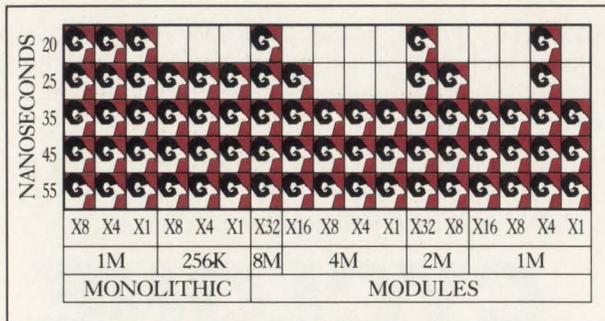
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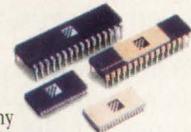


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CIRCLE NO. 47

High-speed PALs keep pace with today's processors

Pinout and process advances are propelling TTL and ECL PALs to 5 ns and faster—with BiCMOS parts lurking in the wings.

Barbara Tuck
Senior Editor

About the only thing that makers of high-speed PALs agree on is that designers will need parts fast enough to support their 40- and 50-MHz microprocessors. To meet that demand, PAL vendors are demonstrating Yankee ingenuity at its best by offering designers a rich set of industry-standard products differentiated by process technology, pinout and circuit design techniques.

For systems requiring 16XX and 20XX PAL devices of 5 ns and faster, designers can choose bipolar TTL parts or high-speed and very pricey ECL parts. High-speed BiCMOS PALs will become a reality early next year. Customers that have opted for TTL are finding themselves in the middle of a pinout controversy between Advanced Micro Devices (Sunnyvale, CA) and Texas Instruments (Dallas, TX). AMD has designed a proprietary pinout to minimize ground bounce in its 4.5-ns PALs, which should be shipping in volume by now. TI, on the other hand, is relying on the standard pinout and the use of ECL configurations internally with TTL I/O for its two 5-ns parts, available in production quantities since the spring. National Semiconductor (Santa Clara, CA) has chosen to stick with the standard pinout for its 5-ns TTL bipolar PALs, scheduled for introduction before the end of the year.

For designers of computer and workstation applications that require the highest speed, National offers a 2-ns ECL PAL, the fastest in the industry. Philips Components-Signetics (Sunnyvale, CA), perhaps more bullish on BiCMOS as a mainstream technology than any other semiconductor vendor, will be sampling 5-ns BiCMOS PALs in the first quarter of 1991.

■ Ground bounce an issue

At speeds of 5 ns and higher, the most significant design consideration is ground bounce, or the ringing on an output signal when one or more outputs on the same device is being switched from high to low. The ringing in a high-speed device can last so long that a slower device could actually be a faster solution since a system can't consider data as valid until the ringing settles to below the low-level input voltage of the receiving devices.

Though the ringing caused by a single output's switching is normally below the low threshold voltage, the voltage at the ground pad is coupled



Because National Semiconductor kept the supply current drawn by its 2-ns ECL PAL at 220 mA maximum, the company was able to use a relatively inexpensive PLCC package for an ECL device for the first time. National uses the extra four pins of the 28-pin PLCC to balance the I/O ratio.

■ HIGH-SPEED PALs

to any low output through its output transistor, and is thus proportional to the number of outputs switching simultaneously. If enough outputs switch, ringing on the ground pad will cause the detection of false highs. The culprits responsible for ground bounce are the inductance and resistance of the ground connection in the PAL.

To minimize the noise that can be generated by high-speed signals, AMD went with a proprietary-pinout 28-lead PLCC for its TTL PAL16R8-4 family. The pinout, radically different from the standard, results in a 500-ps advantage. Maximum propagation delay is 4.5 ns, and worst-case maximum frequency

7.5-ns TTL PALs.

Unlike AMD, TI has retained the standard pinout for its 5-ns PALs, relying on ECL design techniques rather than a change in packaging to control ground bounce and crosstalk. The 20-pin TIBPAL16L8 and the 24-pin TIBPAL20L8 have 5-ns max. propagation delays, 125-MHz min. cycle times and 4-ns max. clock-to-Q times. The first parts to be available, TI's devices come in 20- and 24-pin DIPs, and 20- and 28-pin PLCCs with conventional corner power and ground pins. Supply current drawn is 180 mA max. for the 20-pin device, and 210 mA max. for the 24-pin part.

As for noise, TI claims that its

ing gate with ECL techniques replaces a true and a complement phase to eliminate one delay. And a differential input turns a single transistor on and off at the sense amp, which is combined with the matrix to save another delay. By using an ECL configuration, TI reduced the voltage swing at the sense amp input (input to the output gate) by more than 50 percent, as compared to TTL voltage swings.

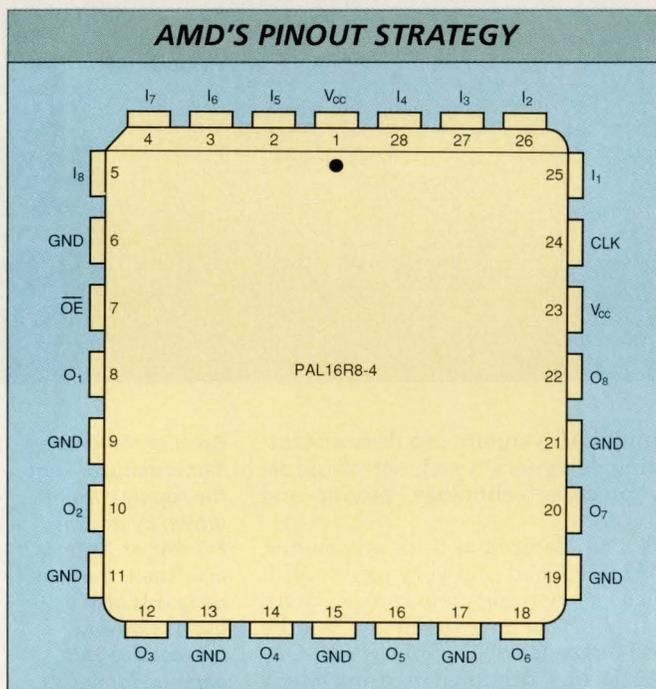
Since ECL is used through the sense amp, the small ECL input swings have to be converted to 2.5-V TTL output swings. To avoid the customary 2-ns cost of converting TTL into and out of ECL, TI used a specially compensated regulator outside the data path to control levels used inside the gates.

Throughout the PALs, TI uses sets of temperature-compensated voltage reference circuits. These circuits set a high-level output voltage of less than 3 V to reduce noise and subsequent undershoot and oscillation problems. By clamping the external high-level output voltage and internal voltage swings, these circuits prevent extreme drops in the internal supply from affecting circuit operation. A voltage reference circuit applied at the input of the ECL gate sets the input threshold.

■ Output kickers boost current

TI has made two improvements on the output—called output kickers—to provide extra output drive capability. A low-to-high output kicker provides the ability to change the short-circuit output current from 90 mA to 180 mA during an output transition, permitting system designers to drive 200- to 300-pF loads with less performance degradation. A high-to-low output kicker disengages when the output reaches 0.5 V. Most high-to-low drive enhancements disengage somewhere between 1.6 V and 2.6 V. System designers prefer at least a 0.8-V high-to-low speedup, allowing them to switch through to the next device's threshold. In addition to setting the threshold at 0.5 V to solve this problem, TI has added a timed current source that automatically shuts the kicker off after 20 ns.

According to Schnettler, "TI has shown that the key to controlling ground bounce and crosstalk noise in fast-switching bipolar devices is not in the packaging but in the circuit design." Furthermore, he says that being the first vendor to go to



To minimize the noise that can be generated by high-speed signals, Advanced Micro Devices designed a proprietary 28-pin PLCC pinout for its PAL16R8-4 family. The new pinout, which adds one power pin and seven ground pins, shaves 500 ps off the 5-ns propagation delay. By reducing the effective lead inductance, the multiple ground signals and the shorter lead lengths minimize ground bounce.

is 125 MHz in registered mode.

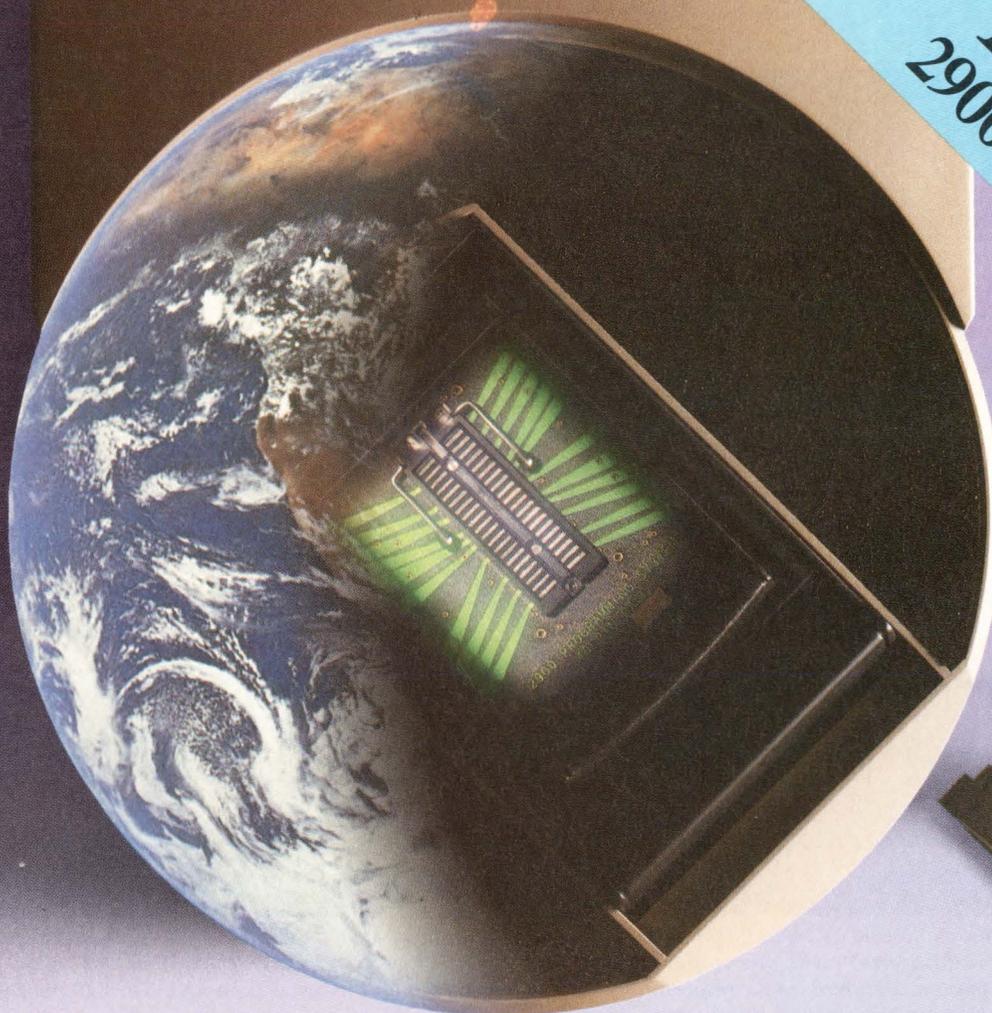
In addition to adding an extra power pin, AMD has added seven ground pins and has situated them in between outputs. By reducing the effective lead inductance, the multiple ground signals and the shorter lead lengths minimize ground bounce. Moreover, isolating the outputs from each other eliminates crosstalk. According to Andy Robin, AMD programmable logic marketing director, the new pinout will help customers solve their critical-path timing problems.

For those customers requesting standard pinouts, AMD is providing the 5-ns PAL16R8-5 family in 20-pin DIPs and PLCCs. They are pin- and fuse-map compatible with AMD's

high-speed parts offer about a 20 percent improvement over previous parts. "Our 5-ns devices generate less noise than either our or our competitors' previous-generation 7- and 10-ns PLDs," says Tim Schnettler, TI strategic marketing manager for programmable logic devices.

The new PLD circuitry, overlaid on TI's 1.5- μ m Impact-X bipolar process, is largely based on ECL techniques. Only the outside world sees TTL levels. Whereas conventional TTL-based PLD designs comprise five delay elements (two inverters at the input, a matrix, sense amp and the output), TI's design comprises only three delay elements. At the input, a single inverting/noninvert-

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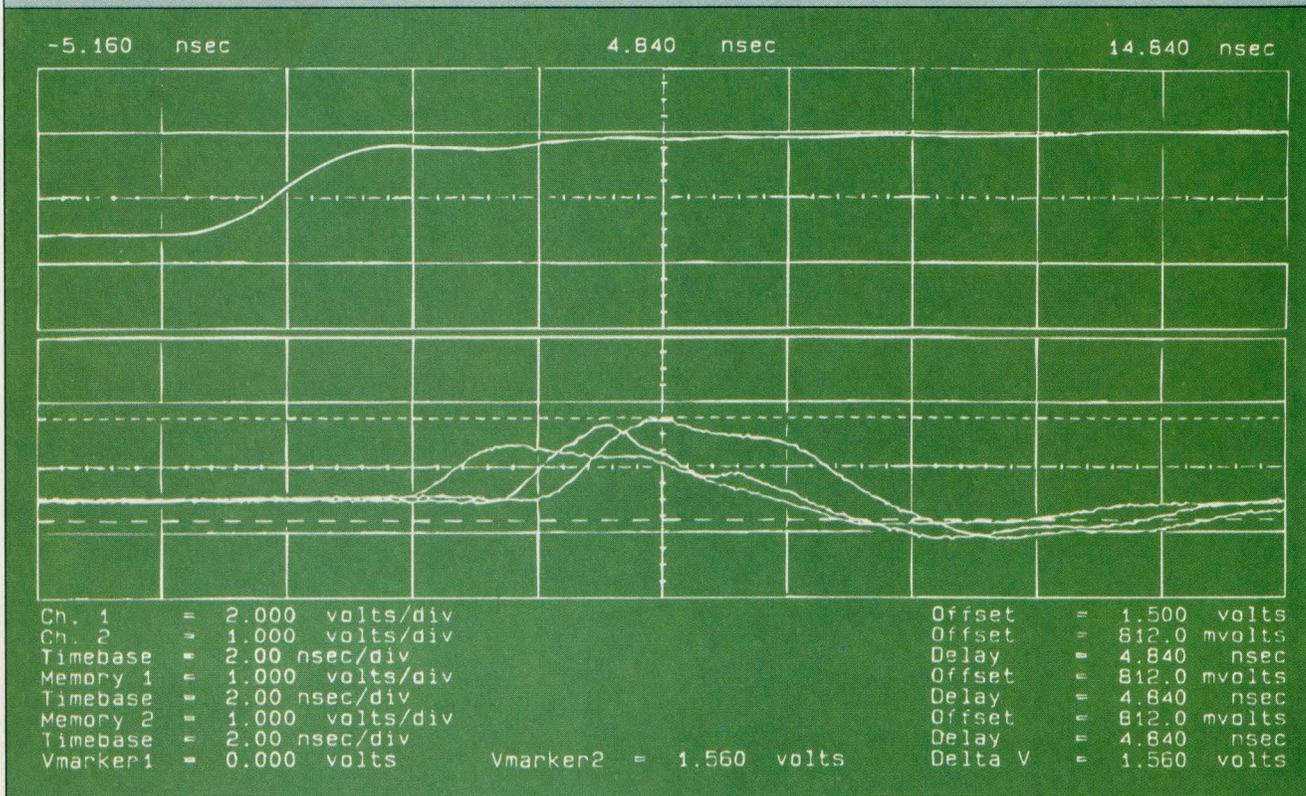
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CIRCLE NO. 48

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TESTING TI PALs FOR NOISE



In a silent-low test conducted by Texas Instruments on its 16L8 PALs, comparative data shows that the standard-pinout 5-ns PAL exhibits less noise (first trace)—with one output held low and the other seven outputs switching from high to low—than the TI 7.5- and 10-ns parts (second and third traces, respectively). The 5-ns 16L8 used for the test was packaged in a 20-pin DIP with conventional corner power and ground pins. (Upper trace shows input waveform.)

production with 5-ns PALs will allow TI to be a mainstream supplier. "TI's 5-ns bipolar PALs will be very competitive against any other 5-ns parts," claims Schnettler.

By the end of the year, National plans to be sampling its 5-ns bipolar PALs. They will have a standard pinout and will employ National's vertical fuse technology. In designing its 5-ns bipolar parts, National has also sought to minimize ground bounce problems. To avoid ground noise causing a false sense and change of state, for instance, National is using a split leadframe package that isolates the output buffer ground lead from that of the input and sense amp. The split leadframe package isolates the two grounds electrically all the way to the package ground pin.

Since the 4.5- and 5-ns bipolar PALs are so new to the market, it's too early to tell whether most customers will choose the standard pinout or AMD's proprietary pinout. As blazing-fast RISC and CISC microprocessors requiring 5-ns PAL sup-

port become generally available, customer preferences on the pinout issue will become clearer.

For the fastest-switching circuits of superminicomputers, high-end workstations and high-speed test equipment, National offers the 2-ns ECLPAL10016C4-2, the industry's fastest PAL. Only for ultrafast designs, where the difference of a few nanoseconds is significant to system performance, are users likely to pay the high price of this 2-ns part.

National fabricates this speed demon in its Aspect II process, which uses a tungsten fuse technology, to achieve high speed without high power consumption. Twice as fast as the industry's previous speed leader, the 2-ns device draws 220 mA, giving it the best ECL speed/power ratio in the industry, according to National. And with ECL's narrower voltage swings, ground bounce isn't even an issue.

Because National was able to hold down the power consumption of its 2-ns PAL to the equivalent amount of power as a standard 24-pin TTL

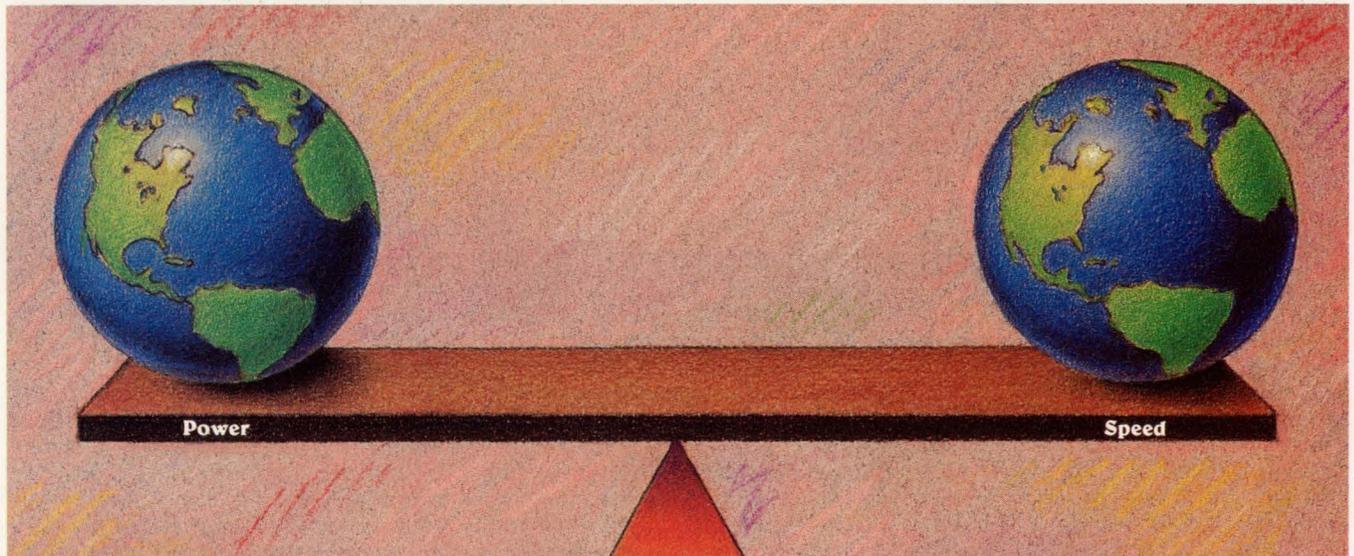
PAL, it can offer the part in a PLCC. The shorter lead lengths of that package reduce impedance for a propagation delay improvement over a DIP of between 300 and 500 ps. As the next size PLCC up from a 24-pin DIP has 28 leads, the logic function of the 2-ns PALs has been modified to take advantage of the extra pins. The 16C4 function in a PLCC has four additional outputs, one for each corresponding complementary output.

The ECLPAL10016C4-2 is a combinational device that uses no clocking signals. It accepts 16 input lines and generates four output functions, with each output containing eight product terms for a total of 32 product terms.

As the leader in ECL PALs, National offers 10K- and 100K-compatible parts with 3-, 4- and 6-ns propagation delays. Both Aspen Semiconductor (San Jose, CA), a subsidiary of Cypress Semiconductor, and TI offer a few parts that are pin-compatible with National PALs. Jay Kamdar, National's PLD mar-

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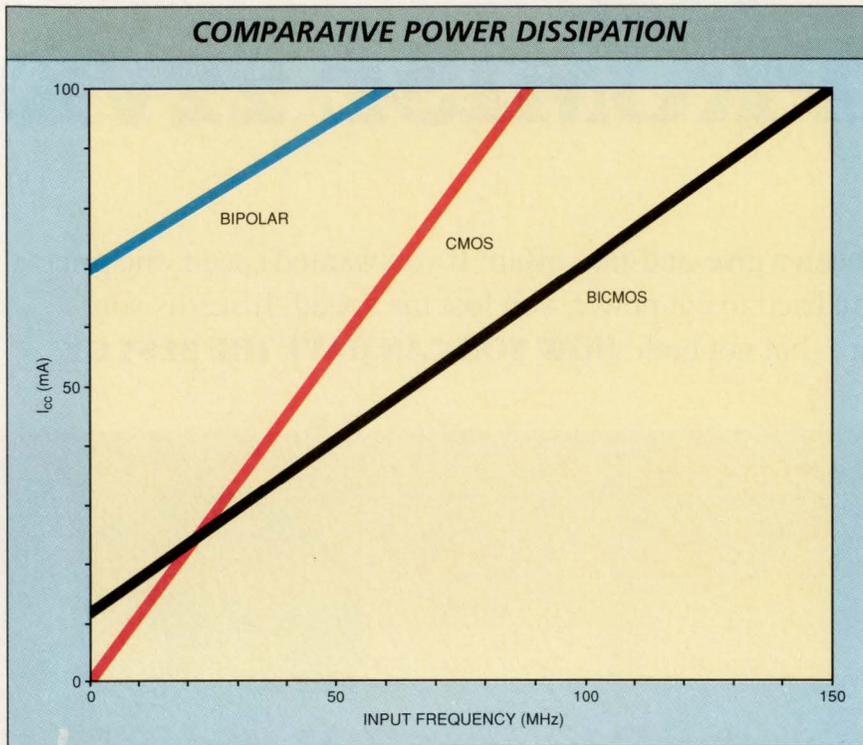
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A Signetics graph of supply current vs. speed shows that the power dissipation cross-over point between CMOS and BiCMOS tends to occur well below the typical operating frequency of today's systems. Signetics will supply 5-ns standard-pinout BiCMOS PALS sometime next quarter.

keting director, doesn't expect that TI will be a player in the really high-speed ECL market. Nor does he feel that Aspen, which offers 2- and 3.5-ns ECL PALS, will be in the market over the long term. "ECL requires a process might that small companies can't continue to afford," Kamdar maintains. "National, on the other hand, has the fundamental infrastructure to support the ongoing process development that's required."

As for National's future plans regarding ECL PALS, Kamdar says that whether National pushes performance below 2 ns will be determined by the marketplace. A higher-speed ECL process than that used for the 2-ns PAL—Aspect III—is already in production, he says.

■ BiCMOS gets support

Perhaps the most significant development in the high-speed PAL market is the push toward BiCMOS, with Philips Components-Signetics leading the way. Sometime next quarter, Signetics is scheduled to sample 5-ns BiCMOS PALS in its 20- and 24-pin standard-pinout PLQ16XX and PLQ20XX families.

President Jim Dykes has been a vocal backer of BiCMOS. Process

limits of bipolar and CMOS technologies, he says, will be a driving force in the emergence of BiCMOS as a mainstream technology. Bipolar is nearing its limits in terms of power and packing density, whereas CMOS will never be able to provide the drive capability required for truly high-speed performance, according to Dykes. "CMOS will give you the density. Bipolar will give you the speed and high current drive. But BiCMOS can give the edge where the customer needs two or all three attributes," Dykes says.

Signetics' fully integrated Qubic BiCMOS process, developed for the high-performance market, lets designers put bipolar transistors anywhere in the circuit where speed is critical. Qubic bipolar transistors exhibit a maximum operating frequency of 13 GHz. Bipolar gate delays are less than 70 ps. "Because of its power and flexibility, we expect Qubic to become a key building block process for Signetics in the 1990s," says Dykes. "In the area of programmable logic, BiCMOS is an attractive alternative where you need speed and more speed with smaller die size."

Signetics PAL product marketing manager Frank Logan claims that

specs for the 5-ns BiCMOS parts are competitive with those of TI's 5-ns bipolar parts: supply current drawn is specified at a maximum of 210 mA. Unlike TI, Signetics didn't see that much of an advantage to using ECL internally. Its parts are TTL internally and externally. As for ground bounce, Signetics slowed down rise and fall times from what they could have been to minimize noise. In a benchmark test with the company's 7.5-ns bipolar parts, initial numbers for BiCMOS silicon samples show 100 mV more ground bounce: 700 mV for the BiCMOS vs. 600 mV for the bipolar.

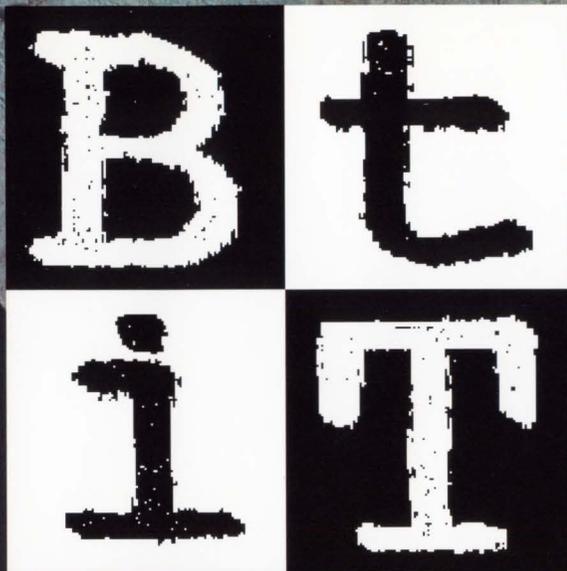
Signetics also considers metastability a concern with high-speed parts and claims the only solution is to design circuitry that's metastable-immune. "If you never violated setup and hold times, you wouldn't have to worry about metastability," Logan says. "But at higher speeds it gets harder to guarantee those times."

National is also backing BiCMOS as the appropriate mainstream technology for high-speed PALS. "BiCMOS will be the mainstream technology of choice for 5-ns and sub-5-ns TTL-I/O PLDs," claims National's Kamdar. Though the company won't be pinned down to a release schedule, future plans include implementing the 16XX and 20XX PAL families and other standard PLDs in National's new ABIC 1V BiCMOS process, also being used for gate arrays and standard logic.

So years after the first PAL was introduced, there's no end to them in sight. Processes are changing to suit system requirements, and pinouts have been modified to accommodate high-speed signals, but functionality remains the same. In a fast-moving industry where familiarity is a stranger, the ability of PALS to keep up and yet remain essentially the same is a welcome switch. ■

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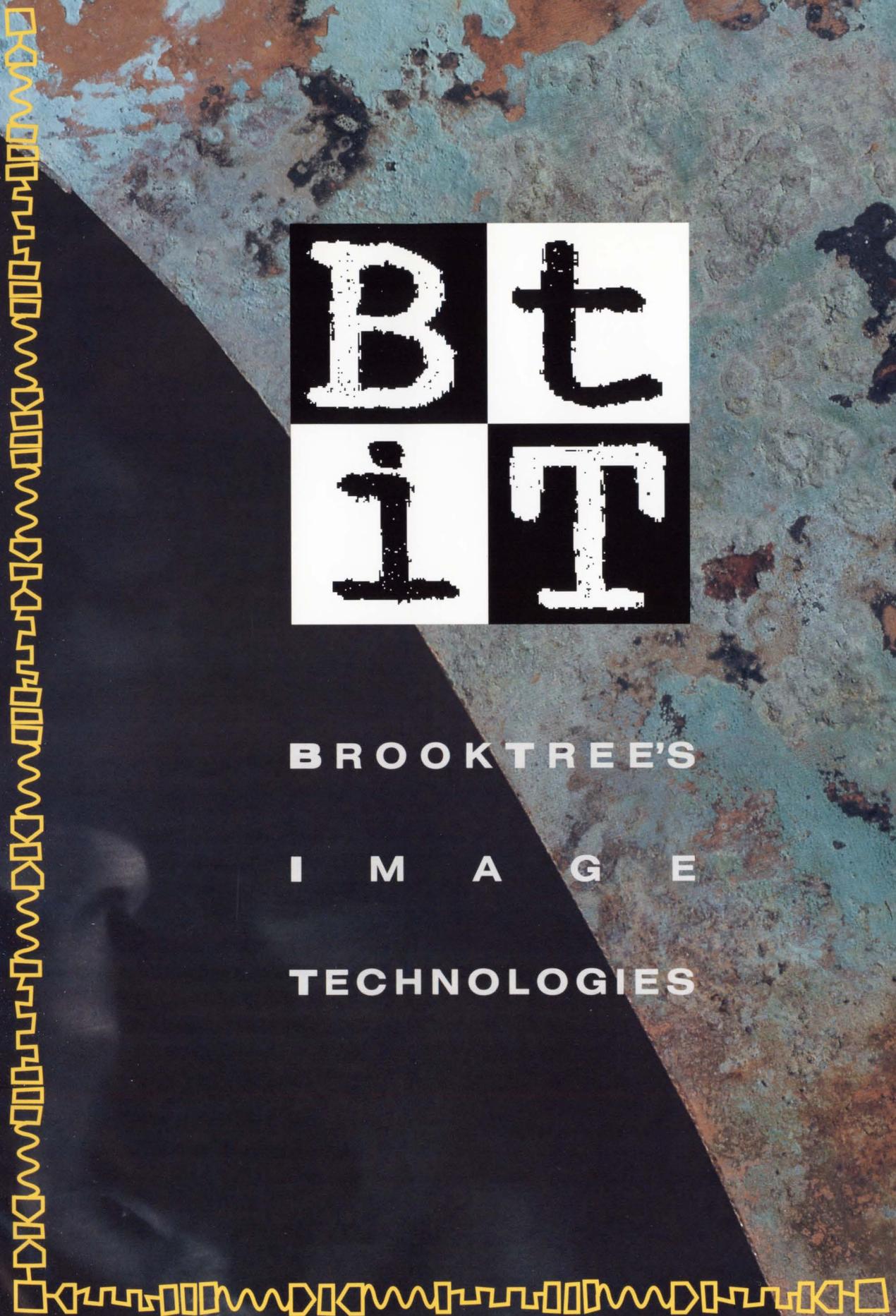
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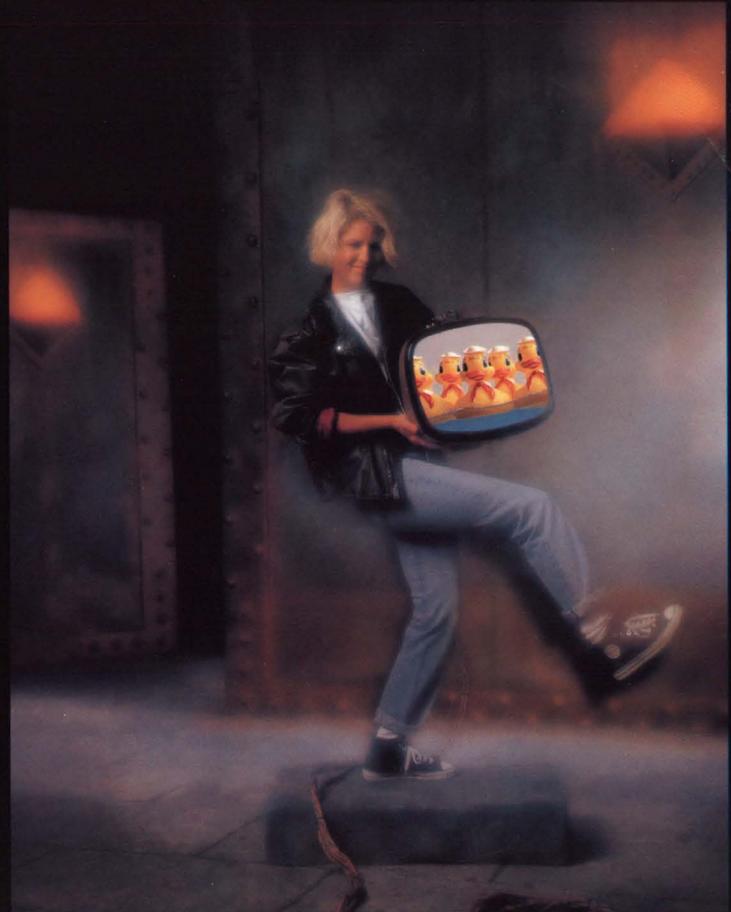
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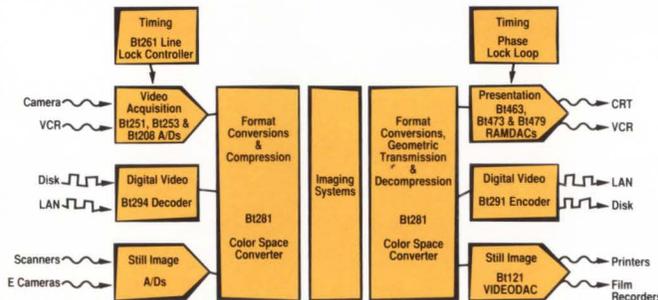
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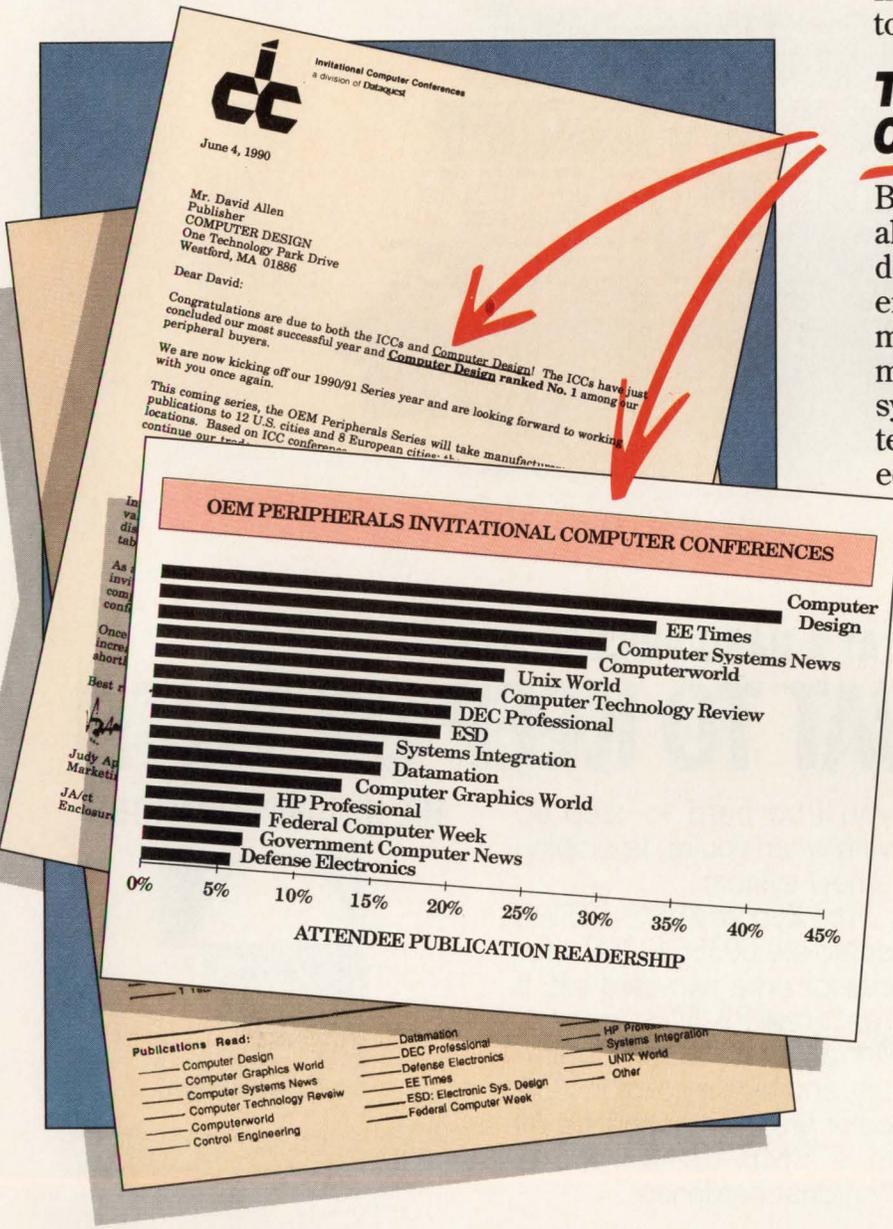
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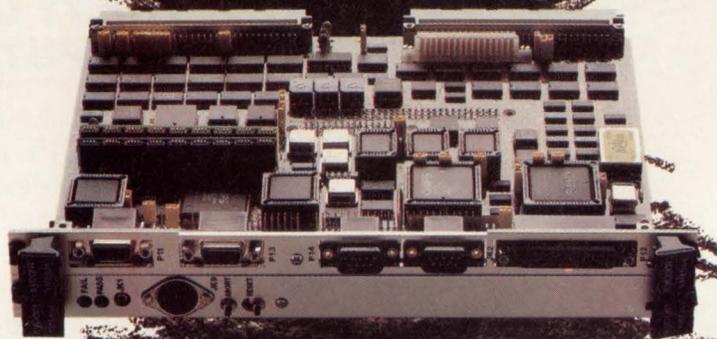
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CAD framework vendors wrestle with standards

Though vendors agree on the open-framework concept, they're still debating what constitutes a truly open standard. And the key issue is who's going to sacrifice what.

Mike Donlin
Senior Editor

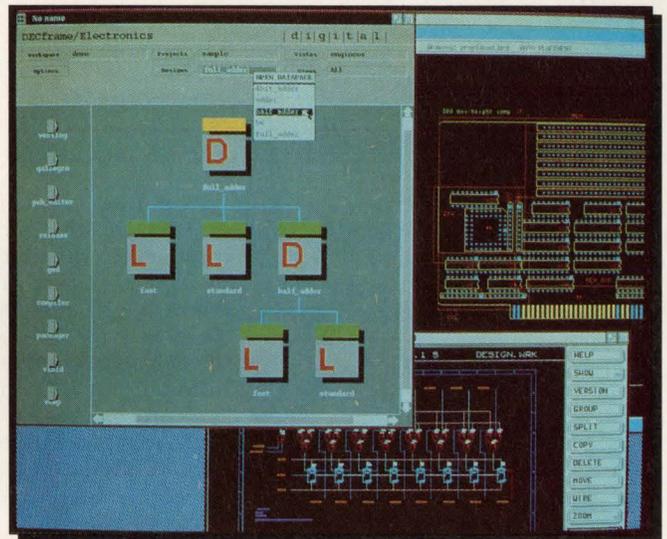
The concept of an open CAD framework is a lot like world peace; everyone thinks it's a great idea, but wars often break out over how to achieve it. Part of the debate over what constitutes a perfect framework comes from its very nature, that is, an open software infrastructure that lets multiple tools from multiple vendors work on multiple platforms. Anything that tries to accommodate that many architectures and corporate strategies is bound to run into problems. And though the notion of a framework has existed since the early 1980s, the first commercially available framework is only about four years old—the Design Framework from Cadence Design Systems (San Jose, CA).

While there's general agreement over the basic definition of a framework, there are many ways to implement the idea, and no vendor wants to refocus a corporate strategy if it means a major overhaul of existing tools or database structures. As a result, many models for a framework standard have been proposed to the CAD Framework Initiative (Boulder, CO), a body of CAD tool users, vendors and systems integrators organized to define the elements that constitute a truly open framework.

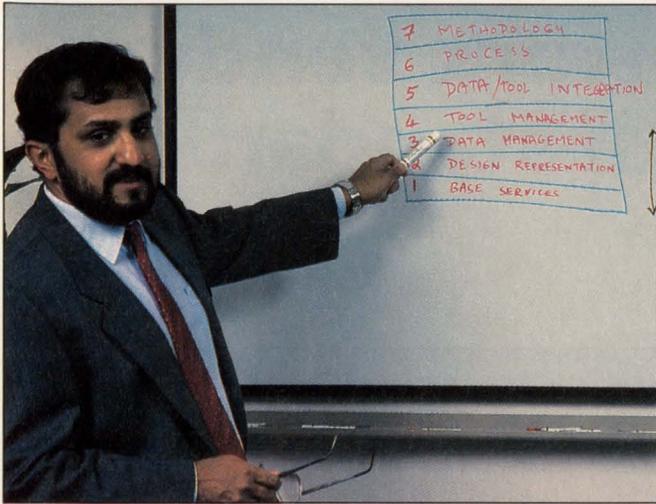
Cadence and Digital Equipment Corp (Maynard, MA), for instance, have suggested a seven-layer model to the CAD Framework Initiative (CFI) that is based on a combination of Cadence's newest framework offering, Design Framework II, and DEC's PowerFrame. The model contains many of the elements that other proposals have, though the CFI hasn't yet adopted any of the models completely.

The Cadence-DEC model begins with base services, such as database access, and moves up through design representation (gates, transistors, ports and so forth) to data management services, tool management capabilities, data/tool integration, process management and, finally, methodologies, which reflect the design philosophy of the users. "The seven-layer model evolved over time," says Jayaram Bhat, director of frameworks at Cadence. "We added services as needs dictated. The key to a successful framework is that it should be open and make a design environment more efficient. Our model increases the levels of abstraction, and this removes the complexities of file handling from the designer."

Other vendors have proposed models with the same general characteris-



A key function of a framework is to help the user manipulate a suite of tools through the complicated design path. DEC's PowerFrame manages the design process by calling on a previously encapsulated toolset. Here, the GED schematic editor and Allegro PCB layout tool, both from Valid Logic Systems, have been summoned from the PowerFrame menu in the foreground.



The Cadence-DEC seven-layer framework model can be reduced to two categories: tool frameworks and design management frameworks. "Levels one through three offer tight tool integration," says Jayaram Bhat, director of frameworks at Cadence. "The rest may be thought of as a super operating system."

tics, while some tool developers are taking a wait-and-see attitude about an emerging standard. There is, however, one point of agreement—frameworks are an idea whose time has come.

"There will always be a group of people who wait on the sidelines before they take action," says Andy Graham, president of CFI, "but I think users have made it clear that they can't afford any more inefficiency. People are saying that they can't spend time and money trying to force tools that weren't designed to work together into a design environment, and vendors are realizing that openness must be a cornerstone of their business strategies. A framework standard will be the result of these realizations."

The need for a framework standard is also being driven by the design trends of the 1990s—computer systems and their components will become more complex, while the time allowed to develop them will shrink. These constraints will make it necessary for a project to be divided among many engineers, each working on a different portion of the design—a concurrent engineering environment.

■ **Need for cohesion**

This engineering team will have unprecedented demands on their abilities to divide a complex task and keep the flow of design data cohesive. "If you talk to companies about their respective design processes, they'll laugh, because no company or site has a single design process," says Bill Stevens, product marketing manager of the advanced products division at Mentor Graphics (Beaverton, OR). "The processes vary by pro-

gram and project with different teams working on segments of a product throughout the design cycle."

Though there are several framework-based systems on the market that address the problems facing a concurrent engineering team, they often force the team to use tools that are preselected by the CAD vendor, or to spend an inordinate amount of time trying to interface their own tools into the environment.

"An object-oriented architecture enables you to model the complexity of design automation data without compromising storage efficiency or performance."

—Thanasis Kalekos, Mentor Graphics



In addition, each time a tool is used, the data that it manipulates is affected. The challenge, then, is to make sure that the data being manipulated is in fact the latest revision, or costly errors could occur—for instance, a simulation could be run on the wrong release of a schematic's database. Directing this ever-changing data through the workstations of a multifaceted design team is at the heart of a successful framework architecture.

"A team of, say, 12 designers is part of a larger group that includes logic designers, layout specialists,

test engineers and project leaders running upwards of 35 to 40 applications throughout the life of a project," says Fumio Taku, manager of electronic design marketing at DEC. "Trying to produce an environment that's error-free and productive across so many disciplines and platforms is a formidable task. The problem is that designers are spending too much time trying to manage files. When it's time to release a design for manufacturing, it's critical that the final set of files is the one that's released. That's why data/file management is such a crucial issue."

■ **Keeping on track**

The main function of the data management part of a framework is to match the physical organization of design data to the logical view of the design while at the same time managing and tracking that data as it changes along the design path. A design consisting of several logical blocks such as CPU, memory and I/O, for example, will be represented by data that exists in many different files, directories and libraries. The data management function of a framework must tie this data to the actual device being designed so that the engineer can concentrate on the design itself and not be distracted by all the data manipulation that occurs throughout the design process.

Cadence's Design Framework II management system, for instance, tracks, controls and automates the manipulation and operation of tools, designs and libraries in distributed design environments. According to Cadence, the manager uses a graphical roadmap of the design process to guide users through their designs. As the users proceed, the design-flow system tracks and indicates their progress.

This critical point—how the unwieldy data in a design environment is represented, addressed and manipulated—is debated among framework vendors. "There are some vendors saying that you need a single integrated database for everything from CASE [computer-aided software engineering] to mechanical engineering, and we think that's ludicrous," says Larry Rice, senior product marketing manager at Valid Logic Systems (San Jose, CA). "The actual amount of data that a set of tools may have to share is relatively small, so there's no sense in burdening the

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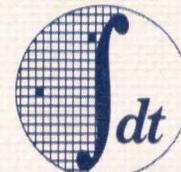
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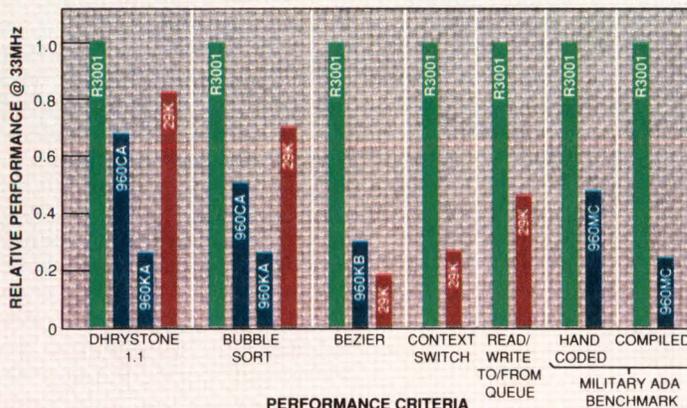
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■ CAD FRAMEWORKS

system with a huge database.”

Valid's Design Process Framework is being developed around the coordination of multiple open databases rather than on a single proprietary database. According to Valid, this strategy enables a tool to operate at peak performance by using its own separate database. When users want to integrate a commercial or proprietary tool into the framework, it requires less work to port the application to the coordinated database scheme, which doesn't entail the use of proprietary database constructs. Valid is using a commercially available object-oriented database management package from Objectivity (Menlo Park, CA) to handle the administrative part of its framework. This strategy allows data management to be separated from application-specific data.

■ Multiple vs. single approach

Much of the controversy over database structure revolves around this multiple vs. single database approach. “People are misusing terms,” says Thanasis Kalekos, Mentor's director of marketing for the advanced products division. “There's a difference between the database access mechanism (the part that knows how to get the data) and the data that's used (the data model). An IC layout editor, for instance, needs to work from a data model that's different from the one that the simulator's using. That doesn't mean there's a separate database access mechanism for every tool; it only means we have multiple data models with a common access mechanism. Our database isn't an unwieldy, monolithic structure. It's a unified structure with many parts.”

Mentor Graphics uses a proprietary object-oriented database written in C++ as the basis for its Falcon Framework. This object orientation permeates the framework architecture, from its C++ implementation to its data management environment, so that tools and data are managed as design objects in a unified way.

Though the confusion, claims and counterclaims about databases aren't likely to go away soon, there seems to be a consensus among the large EDA vendors that the object-oriented database is the right approach. “The key advantage of the

“If CFI comes up with an interface standard, then any tool should be able to access any database.”

—Bill Holbrook, Viewlogic



object-oriented architecture is that it enables you to model the complexity of design automation data without compromising storage efficiency or performance,” says Mentor's Kalekos. “A second advantage is its extensible base, which lets data models, files and tools establish relationships with each other.”

Even the object-oriented approach to data management, however, can be partitioned into different strategies. “You can use an object-oriented database in two ways,” says Al Blazevecius, vice-

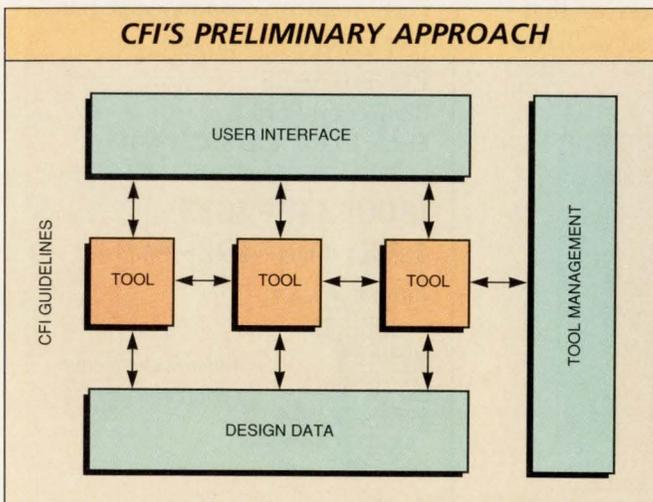
president of engineering at Interact (New York, NY), a vendor of a tool-independent framework. “The first way is to use a set of existing tools that already have their own data files, and then use data objects to point to those files—the meta-data, or data about data, approach. The other is the more tightly coupled approach where each tool agrees on a lower level, like what a NAND gate looks like and how it's called up, and accesses this information directly in the database. We prefer the meta-data approach.”

A meta-data structure points to the files generated by a schematic editor, for instance, but does more than merely point as a file directory would. A meta-data layer also gives information about the data in the file, so the data manager knows that the file it's calling isn't only data from a schematic editor but an editor from a specific vendor. “By knowing the nature of the files, you can understand what files are compatible with what tools,” Blazevecius points out. “This allows you to describe the file so that the database can behave like a shadow directory of, say, the Unix operating system, but with more information.”

While the database management system is at the heart of a successful framework, some vendors think that the CFI doesn't need to devise a standard that deals with the specifics of a database structure. “If you have a standard way of interfacing to those databases, it shouldn't matter whether it's a large database distributed among platforms or a single database for each tool,” says Bill Holbrook, senior framework engineer at Viewlogic (Marlboro, MA). “I don't think the CFI standard will have to concern itself with too many particulars about the database. If the group comes up with an interface standard, then any tool should be able to access any database.”

■ Tying tools together

Another critical component of a truly open framework is its ability to easily encapsulate tools, whether they're proprietary in-house tools or from third-party vendors. Unlike simple tool integration that provides interfaces between tools and system services, tool encapsulation ties an application into a framework through user-supplied code that supplies the appropriate invocation command to the system. In any case, tool encapsulation is a necessary, al-



The CAD Framework Initiative's preliminary framework model adopts a modular rather than monolithic structure. This approach emphasizes a key point—that integration standards must exist between the modular functions as well as between the tools themselves.

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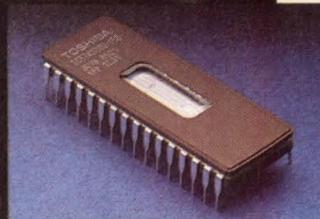
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CIRCLE NO. 52

CFI—Who we are and what we plan to do



For many CAD experts, frameworks connote open, seamless CAD tool integration and, as such, are a required element of vendor offerings. But there's

a great deal of confusion over what elements constitute a framework environment and what benefits users should derive from it.

Several companies are striving to deliver open framework-based products, and we should be encouraged by this; nevertheless, users want to know more about the problems these products are intended to solve and how they should be evaluated.

The increasing complexity of electronic products is forcing users to decide on new design methodologies and CAD tools. In this sense, a framework can be viewed as an enabling technology that brings together diverse computer hardware, applications and design data. It's a problem-solving agent that supports the designer's methodology and CAD tools.

A key element of a framework that addresses these issues is the need for openness—a highly desirable objective that can only be realized through accepted industry standards combined with a real-world problem-solving perspective. Through standard interfaces to CAD framework components, the cost of combining multisourced CAD tools into an effective CAD system can be reduced. And this is where the CAD Framework Initiative (CFI) enters the picture.

With participation by more than 50 companies, CFI was formed in 1988 to

develop worldwide industry guidelines for design automation tools and their supporting frameworks to remove barriers to integration. CFI defines a framework as a software infrastructure that provides a common operating environment for CAD tools. Beyond that, many CFI members have contributed framework requirements defined for their own use. Requirements have also been drawn from standards-development efforts carried out by other engineering domains similar to CAD, such as CASE (computer-aided software engineering), and from documentation produced by

Frameworks could turn out to be the operating systems of the 1990s.



the Engineering Information System Project funded by the Department of Defense.

In November 1989, CFI published draft requirements specifications for its framework guidelines, and draft proposals were available to members last June. Initial Version 1.0 draft guidelines will be published next month for balloting.

CFI is striving to develop guidelines that companies can use directly in the product development process prior to broad market adoption. A good example of the CFI approach is the Procedural Interface (PI) developed as a demonstration project for the Design Automation Conference (DAC) last June.

Visitors to the CFI exhibit viewed design data from 17 "producer" software tools being freely accessed over the CFI PI by 15 "consumer" tools from a total of 22 separate vendors. The software was running on workstations from Hewlett-Packard, Digital Equipment

Corp, IBM and Sun Microsystems.

Some participants in the DAC demo have already begun to implement the PI in their tools, and three major CAD tool vendors—Cadence Design Systems (San Jose, CA), Mentor Graphics (Beaverton, OR) and Valid Logic Systems (San Jose, CA)—announced their intent to do so in future product development.

In the future, I foresee computer vendors taking a more active role in the evolution of frameworks. The framework, after all, can also be viewed as a set of CAD-specific extensions to the operating system environment offered by a computer vendor. Because the application domain supported by framework technology extends from CAD through CAM to CASE, and so on, it seems likely that computer vendors will play a major role in providing framework solutions.

If these vendors do get involved, frameworks could turn out to be the operating systems of the 1990s—a development that could make them more economical by distributing the technology to a wide customer base.

The environment offered by a framework/operating system combination can provide users with virtual resources (CPU, main memory, secondary storage and so on) that differ in useful ways from those provided by the basic hardware on which the CAD tools operate. The framework therefore presents the CAD user with a virtual machine more applicable to engineering design than the underlying physical machine.

In sum, CFI's role is to define guidelines for design automation frameworks that will be proven through prototype implementation—not by endorsing a given vendor's solution or any single standard framework implementation.

Andy Graham, president, CAD Framework Initiative, and design automation systems group manager, Motorola

be it difficult to provide, function.

"Writing the code to pull tools into a framework is a pretty formidable task," says Mike Gianfagna, director of mixed-signal marketing at Harris Semiconductor (Melbourne, FL). "Certainly if a framework is going to be not only open but open to the average user, it must contain integration services that don't require high-level expertise to operate. If an integrator is reasonably good, users should be able to write their own

environments."

This need for integration services has been recognized by framework vendors and will undoubtedly become an important part of a CFI standard. In DEC's PowerFrame, for instance, tools are called through an agent, or piece of code written in C. A window-based tool template provides a graphical means to represent a tool's inputs and outputs. The user can define operating parameters and default options,

though the template's generic routines will handle only about 30 percent of typical encapsulation code needs. DEC provides training courses to assist designers through the manual portion of the encapsulation process.

Interact has taken a further step toward simplifying this process with the Tool Encapsulator, a window-based editor that lets users incorporate tools through a series of fill-in-the-blank parameters. The

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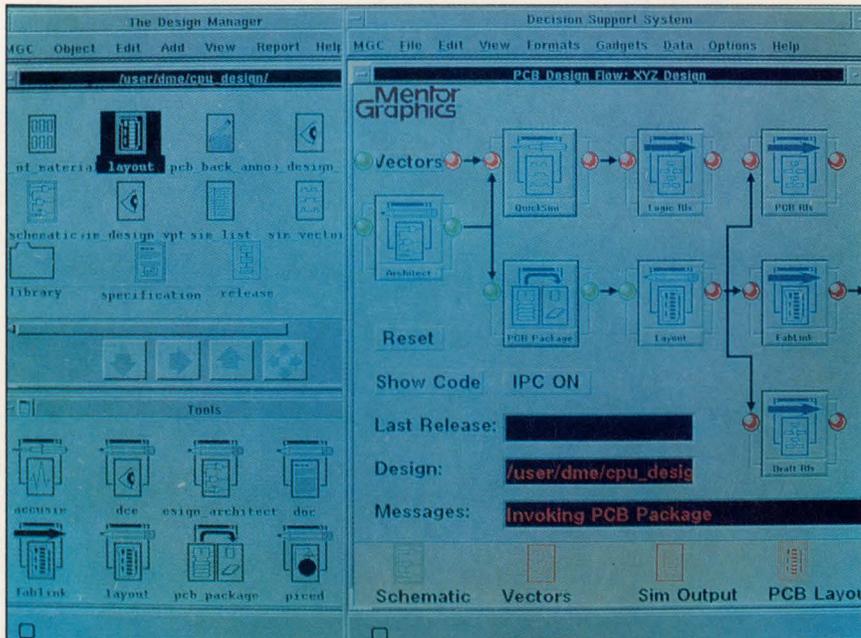
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CAD FRAMEWORKS



With Mentor Graphics' Falcon Framework and Decision Support System, the user can create a graphical representation of the design process. The process floor applications shown here establish logical relationships between tools, tasks and data. Having established the prerequisite design steps, the user can then select a particular function, and the invocation sequence for the desired tool will be automatically initiated.

program, part of Interact's Integrator framework product, specifies pertinent tool information such as inputs, outputs, their relationships and command line options, as well as pre- and post-processing operations. The Tool Encapsulator lets users customize their applications by changing parameters prior to invocation or they can run with a set of changeable default parameters.

Once the individual tools have been encapsulated, Interact's Tool Sequencer automatically chains tools together for specific applications, a task that can be as difficult as the encapsulation process. If an environment contains multiple schematic capture systems, translators, simulators and post processors, for example, appropriate combinations of tools can be automatically sequenced so that end users can perform a simulation on multiple schematic pages from different sources. The encapsulation process and sequencing are related, because the same information that's needed to place the tool in a framework contains the key to its place in an operating sequence in a given set of tools.

The soon-to-be-released Falcon Framework from Mentor Graphics also supports tool sequencing, but allows for more global process management through the Decision Sup-

port System, a spreadsheet program allowing users to analyze the impact of design decisions on other phases of the design process. "Giving a palette of tools to users and asking them to apply a sequence to a task simply isn't enough," says Mentor's Stevens.

"An engineer must have flexibility in specifying a process. When you're entering a simulation phase, for instance, you need to know what kind of data is appropriate for the simulation. Has electronic rule checking been run? Is the simulation vector file big enough? The design sequence that takes place is dependent on the type, amount and quality of the data that precedes it."

Need for flexibility

In addition to the proper encapsulation and sequencing of tools, a framework must also be adaptable to the needs of the technology that's being designed on it. "A framework doesn't care what you're designing," says Nitin Deo, product marketing engineer at Fujitsu (San Jose, CA), "but as an ASIC vendor we need to make sure that a standard has what we need. CFI might not worry about issues such as testability and reliability, but we have to or we'll produce silicon from a design that doesn't work. In our own framework

product, ASICOpen, we must be sure that a simulation is accurately tied to our process. We just have to make sure that the emerging standard is flexible enough to encompass the tools that concern us."

It's clear, then, that with so many agendas, strategies, concerns and technologies involved, CAD framework standards will need to be constantly tested to make sure that they actually do what they promise. To this end, the CAD Framework Laboratory (CFL), located at Microelectronics and Computer Technology Corp (Austin, TX), has been created to standardize the interfaces between CAD tools and frameworks, as well as to provide technical support to CFI. CFL will prototype, verify and validate CFI guidelines across a network of workstations from DEC, Hewlett-Packard, IBM and Sun Microsystems.

Once the standard begins to evolve, CFL will test tools and frameworks for compliance with the CFI model. One thing is certain, the road to a truly open framework is paved with uncertainty. "I really believe that the way we think about frameworks and standardization will shift over the years, but I'm not a prophet, so I have no idea where," says Tom Rhyne, manager of CFL. "One thing I am sure of is that we've awakened a sleeping giant; and in a couple of years, I think we'll see that what we've actually done is different from what we set out to do." ■

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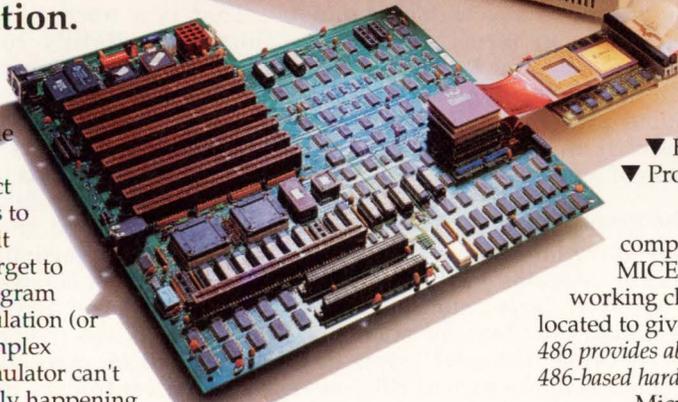
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CIRCLE NO. 54

Real-time operating systems struggle with multiple tasks

Tom Williams
Senior Editor

Large and complex applications are demanding more operating system services, pushing designers toward distributed and multiprocessor solutions. As operating systems suffer growing pains to keep up, some new ways of looking at the problem will be needed.

Don't force it, son. You can always get a bigger hammer." This bit of fatherly advice was meant to be ironic, but when applied to real-time systems it could almost be taken literally. Don't try to shoehorn ever larger and more complex applications into limited hardware resources. Get a "bigger hammer"—more processing power—to allow a complex real-time application to run comfortably and reliably.

But the irony returns with the realization that more processing power to handle increasingly demanding applications also requires more intelligence on the part of the real-time operating system. It also requires careful orchestration between the operating system and the system architecture.

Real-time applications, such as factory process control, flight simulation and on-line transaction processing (OLTP) are making more than simple demands for processor speed. They are also demanding more operating system services than are provided by the real-time executives traditionally used for single-board controllers. Services include networking, disk I/O and man/machine interfaces to name a few. In addition, there are various

ways of increasing processing power. It can be boosted by using a single, more powerful CPU or by adopting a multiprocessor architecture. A real-time operating system must be able to cope with such multiprocessing in terms of multiple CPUs on a single backplane bus. But it must also often deal with distributed processing over some sort of network in order to meet the demands of applications.

■ The determinism myth

A key question about such large real-time systems centers around the ability of large, multiprocessor and/or distributed systems to maintain real-time behavior given the fact that networks such as Ethernet are not entirely predictable, coupled with the contention problems of processors accessing shared memory and the sheer volume of asynchronous input received from the real world. Back when real-time systems consisted mainly of dedicated single-board controllers for washing machines and process control, it was convenient—even comforting—to talk about determinism.

Deterministic behavior requires that every aspect of the system be predictable, that all timings and

latencies, such as context switching, be precisely known and that all software be thoroughly tested to ensure that the system will always respond correctly to interrupts.

That is a worthy ideal, but one that immediately breaks down when you try to incorporate a network such as Ethernet. Since Ethernet uses carrier sense multiple access/collision detect (CSMA/CD) to resolve contentions for use of the network, the time it takes to send or receive a message cannot be predicted with precision. Therefore, Ethernet cannot behave deterministically. But even the strict determinism that was thought the be-all and end-all on mission-critical single-board controllers may turn out to have been an illusion.

Bernard Mushinsky, marketing manager for Industrial Programming (Jericho, NY), points out that real-time executives, in addition to being able to respond to interrupts, have a repertoire of service calls, such as sending a message to a mailbox. If an interrupt occurs during one of those service calls, the call is preempted in order to service the interrupt. "So if we say sending a message to a mailbox takes $n \mu s$, then we have to realize that it's $n + i$

where i is the time to service the interrupt," he says. In fact, the times could be cascaded such that the time is $n+(x*i)$ if additional interrupts preempt the first one. The service call would resume when no more interrupts were being serviced. "So it doesn't turn out to be deterministic for reasons that are in the nature of things," Mushinsky says.

■ Cure worse than disease

Of course, there is a way to force rigid determinism, and that is to lock out interrupts during a service call. But that cure is worse than the disease because the system would begin to lose data and perform incorrectly due to missed interrupts. Thus Mushinsky speaks of "fuzzy determinism," the ability to do the job within an acceptable time frame rather than the ability to run every service or module in a fixed time. "That's not possible," he says.

In reality, the fuzzy determinism Mushinsky describes is what designers have been doing all along and calling it determinism. This illusion has been supported by applications that were slow enough and processors that were fast enough for the system to be idling a good bit of the time. Nor did interrupts occur



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enough to stretch out service call times. But as systems get loaded with more demanding applications and interrupts occur more often, this illusion will break down.

When adding processing speed with a faster CPU or multiple CPUs, and when adding services like networking that are cursed by the epithet "nondeterministic," it is well to keep in mind the motto of Ready Systems (Sunnyvale, CA). "The

operating services, we can let go of the illusion of determinism while retaining the standard of reliable on-time behavior. In this way, large systems can be built around real-time constraints with confidence.

Increasing system complexity

Designers are faced with different system architecture options to attack applications and consequently must choose the best operating sys-

process. These are the familiar single-board controllers featuring a ROMed kernel, fast response times (under 100 μ s) and diskless operation. Typical applications are motor, machine and instrument control.

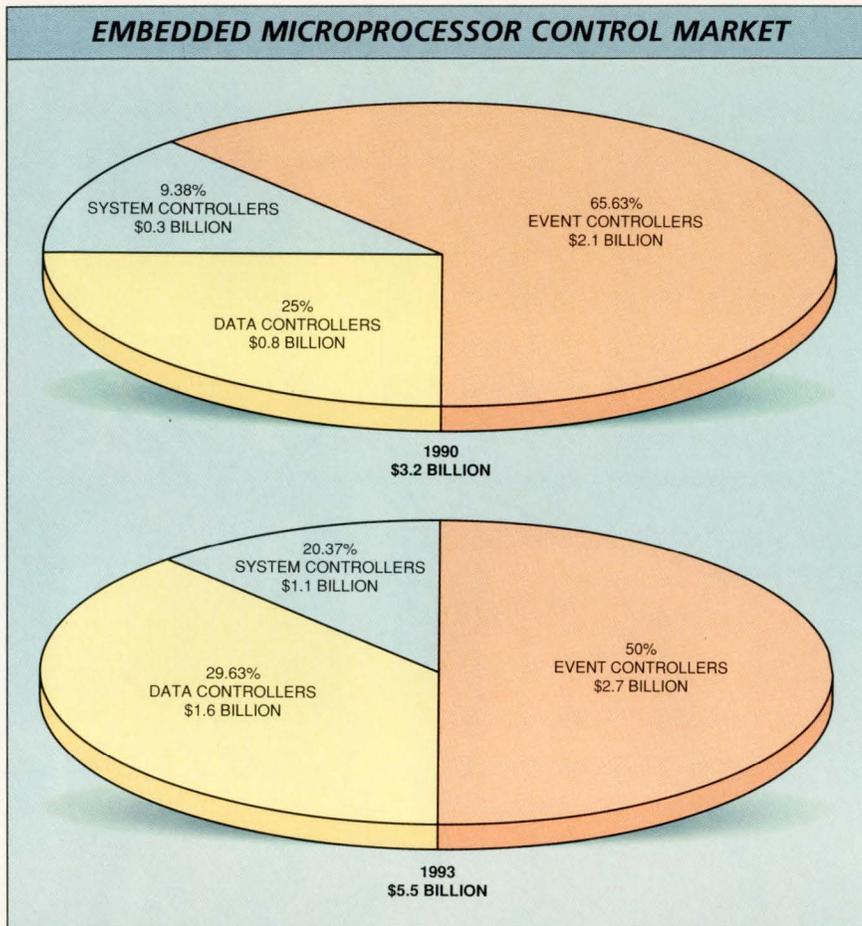
At the next level are "data controllers," embedded systems controlling one or more processes. In their simplest form, they are event controllers linked by a network. They may or may not be diskless and include a man/machine interface but they usually incorporate networking, either among themselves or to a supervisor system running Unix. Typical response times are fast to medium (100 to 500 μ s). Thus they require more operating system services than event controllers. Typical applications include factory process control, communications protocol handling and military command and control.

At the high end, "system controllers" are not embedded, but reside in the host development platform and may control other systems such as data and event controllers. They may include tightly coupled multiple processors and have a man/machine interface, a disk system and networking. System controllers need a full-blown suite of operating system services and feature slow to medium real-time responses (500-plus μ s). Applications include process control, OLTP, simulation and telecommunications.

While these distinctions are useful as a kind of shorthand, many real-time systems can be hybrids of event controllers linked to form data controllers that are in turn supervised by a system controller. Tasks are then organized hierarchically and distributed over the system.

Growing to larger systems

The key feature of operating systems that are trying to span such a hierarchy is modularity. Kernel vendors such as Software Components Group (San Jose, CA) and Ready Systems are providing add-on options to handle networking and real-time operating systems. Vendors such as Microware (Des Moines, IA) and Digital Research (Monterey, CA) already offer operating systems made of modular building blocks that can be left out or included to fit varying system needs. A major challenge for traditional kernel vendors appears to be how to grow their products to meet the demands of networking and how this affects the



At the low end of the market are event controllers, which feature a ROMed kernel, very fast response times and diskless operation. The more complex data controllers and system controllers—which involve one or more of the following elements: networking, multiple processors, disk and user interfaces—require more operating system services than are normally supplied by traditional real-time kernels. According to Intel estimates, the data and system controllers market will grow from under 35 percent of the worldwide embedded control market in 1990 to 50 percent of a \$5.5 billion market in 1993, with system controllers accounting for the bulk of the growth.

right answer late is wrong."

That statement still holds true for real-time systems but it makes a conceptual difference whether the answer arrives on time or in time. As long as behavior takes place in time to satisfy the demands of an application, it is reliable. And by extending that criterion upward to multiple processors and higher level

tem environments to fit those architectures—or vice versa. Intel (Santa Clara, CA) has proposed a rough classification for real-time system hierarchy that has found resonance among some other companies, including VenturComm (Cambridge, MA). At the low end are what are called "event controllers,"—embedded systems controlling a dedicated

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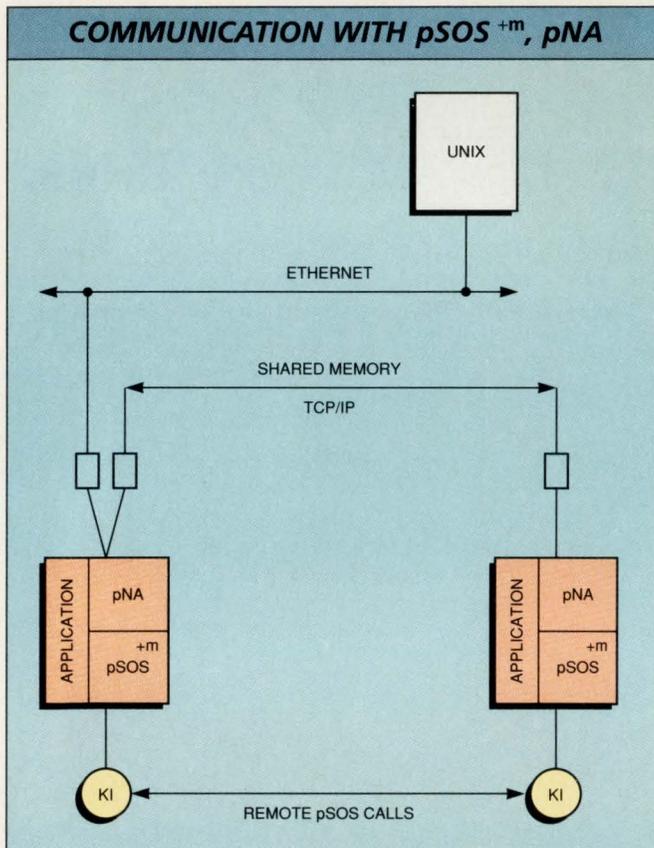
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idea of deterministic behavior.

Software Components Group has long provided a real-time executive called pSOS⁺ and additional ROMable software modules for interprocessor communication (pRISM) and communication with Unix systems (pUCP). SCG recently introduced a network architecture component called pNA that allows pSOS⁺ to communicate with any system supporting Transmission Control Protocol/Internet Protocol (TCP/IP). In addition, a new version of pSOS⁺, called pSOS^{+m}, allows direct intertask communication among multiple processors, bypass-

and can be used to set up a direct link between copies of pSOS^{+m} residing on different processors. In this way an application's tasks can be spread over different processors and still exchange data, communicate and synchronize tasks as if it was running on a single processor.

Modular real-time operating systems such as Digital Research's Flex/OS and Microware's OS/9 and OS/9000 let the designer pick and choose components such as user interface, networking and file system support according to the needs of the architecture environment and the application.



In a multiprocessing/multinode scheme using Software Components Group's pSOS^{+m} multi-processing kernel and pNA network architecture module, pNA provides access to bus-based shared memory using TCP/IP protocols for intertask communication. The same protocols allow communication over a slower and less deterministic Ethernet with a supervisor system such as Unix. For very fast kernel calls between tasks running on different processors, a direct link can be set up using the kernel interface (KI), which is media-independent.

of determinism. "Most people get around it by having a hierarchical system and isolating the real hard real-time," Chao says. In other words, to design what would be classified as a data controller system, the designer must orchestrate the system design to make sure that critical tasks execute entirely on local nodes without having to access the network. Network accesses start to be called "soft real time" as opposed to "hard real time" tasks—which execute locally. "I don't think people consider networking a real problem," Chao maintains. "It's something you design around."

It is important, then, to set tasks that access the network at a lower priority than the critical local tasks and to make it possible to preempt the processes using the network. According to Jerry Fiddler, president of Wind River Systems (Emeryville, CA), "Because the VxWorks system is fully preemptive, you can have tasks that are of a higher priority than the network and can preempt the network process." That, at least, allows for fast response to what might be mission-critical tasks if one is willing to pay the price to dedicate hardware resources to those tasks.

Similarly, Modcomp (Fort Lauderdale, FL) has, in the latest release of its Real/IX real-time Unix system, modified all the TCP/IP code in the kernel so that it is preemptable and has developed a preemptable driver for its Ethernet board. "Once the packet goes out over the net," says Modcomp's senior product manager for operating systems Alan Scharf, "there is no determinism. But the preemptable code adds functionality—networking that does not compromise the determinism and predictability that we've built into Real/IX."

Toward multiprocessing

Networking multiple real-time nodes becomes a solution when one needs physically distributed I/O points, as in a factory automation or process control application. In general, however, it is desirable to concentrate most of the real-time functionality in one place and leave networking for background or low-priority tasks. Increasing the power of the system with a single, more powerful CPU or adding multiple, tightly coupled CPUs that communicate over a fast backplane are techniques that must also be supported by the operating system.

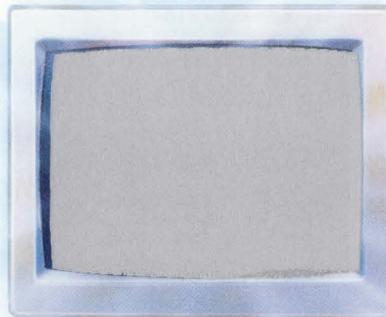
ing the network protocols.

TCP/IP can be used over a standard LAN such as Ethernet or in a shared memory configuration over a backplane bus to communicate with operating systems such as Unix or MS-DOS. pNA allows intertask communication via Unix 4.3 BSD-type sockets. It also allow designers to set up gateways between a shared memory backplane network, for instance, and a wider area Ethernet. For more efficient, direct intertask communication, pSOS^{+m} can call a kernel interface (KI). The KI is independent of communications media

In all these cases the companies readily admit that strict determinism (or what passes for it) breaks down when you start going off-board for services. But it hasn't stopped designers from building useful, reliable real-time systems using these operating systems.

According to Alfred Chao, president of Software Components Group, "Giving up determinism is not the end of the world if you know what you're doing." There comes a point when the black box has to communicate over a distance, and you have to give up clinging to the idea

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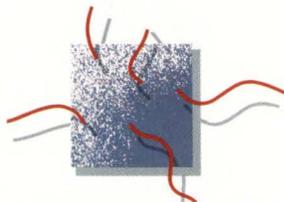
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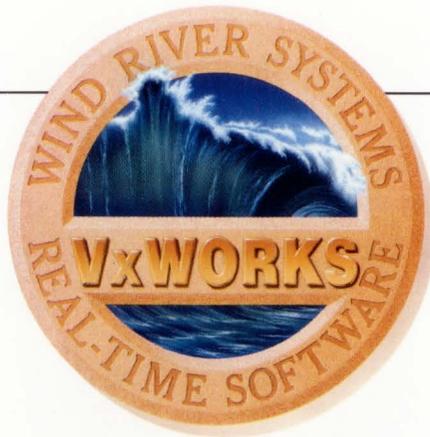
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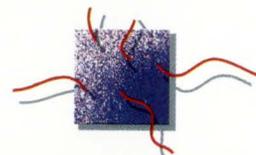
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Supporting distributed configurable applications



Building a data management system for a space station poses some exciting challenges. For example, how do you design a system that will have a 30-year-plus life

span? Or a system that can be easily and quickly upgraded or serviced with no impact on its operation? An Earth orbit, after all, is not on most companies' service routes.

These are just some of the constraints on the design of the European Space Agency's (ESA) Columbus Project, the European Space Station. The three primary requirements for the Columbus Data Management System (DMS) are to provide a real-time, multitasking environment for Ada application in a distributed architecture and to provide an interapplication communications scheme; provide support for dynamic reallocation of applications with minimal impact on the system and application; and build the system to be both hardware and network independent.

Dynamic reallocation is important because there are more than 100 machines on the space station. No machine except the one being serviced should be affected during maintenance or repair.

Another important requirement is that the DMS will have to accommodate a mix of nodes to run different tasks. Some will be dedicated, real-time nodes, used to monitor space station environmental conditions continuously or take scientific measurements. Others will be more sophisticated, providing interactive displays for crew members' use.

The requirements to support Ada applications and dynamic configuration and reconfiguration have led ESA to develop what it calls SoftWare Replaceable Units—or SWRUs. These operational units can be managed like hardware in that they can be replaced easily for updating or repair.

■ The microkernel solution

Requirements of this sort, however, call for more than a conventional operating environment. To implement these kinds of services in one of today's monolithic operating systems would result in a com-

plex system that would be difficult to maintain and upgrade. ESA has found that by building the data management system using a communications-oriented, high-performance, distributed operating system kernel, it has been able to integrate the level of interapplication communications the DMS needs, add services as necessary and upgrade or maintain the system even in Earth orbit.

ESA asked Chorus Systems SA (Paris, France) to demonstrate how the company's Chorus operating system could meet the requirements of the Columbus DMS. The study proved that Chorus could do so because of key properties of the kernel-based architecture: it has a real-time, communications orientation; and it is highly modular.

Chorus's modularity makes it possible to build an operating environment that can support a range of services. Its flexibility allows a complex operating environment that can be dynamically configured to suit the system's requirements. Its communications scheme supports the necessary dynamic configuration and reconfiguration of applications.

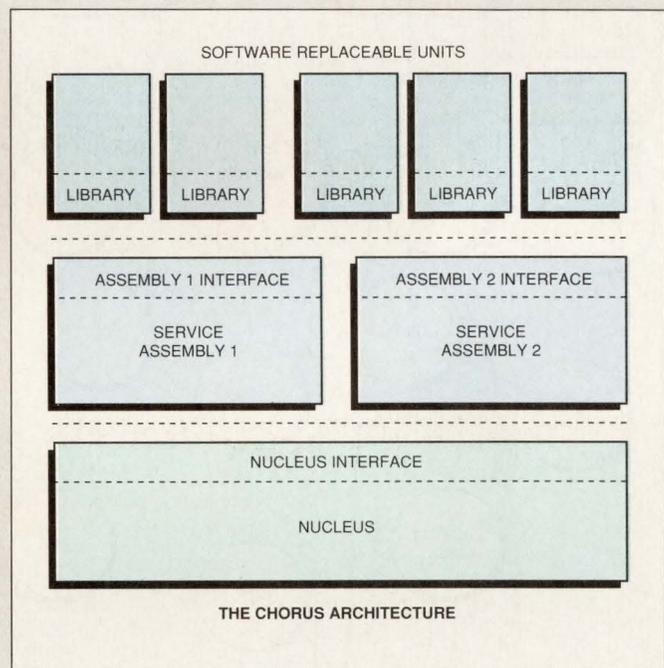
Its flexibility allows a complex operating environment that can be dynamically configured to suit the system's requirements. Its communications scheme supports the necessary dynamic configuration and reconfiguration of applications.

■ Three-layer architecture

The Chorus system for the Columbus DMS comprises three layers (see figure). The first layer is the small real-time kernel, called the nucleus, with integrated interapplication communications. The nucleus insulates the higher level software from the hardware and the network structure. Second is a set of system servers, which complement the nucleus by providing the necessary higher level services as service assemblies. These service assemblies are part of the integrated distributed nature of

the architecture. When necessary, different assemblies can be built on top of the same nucleus. The third layer is the application layer, mainly SWRUs, which run on top of the assemblies.

All software on board Columbus is made up of SWRUs. These must be replaceable by one or several other SWRUs, and for some critical functions, system operation cannot be affected. Applications can migrate from one processor to another for repair or maintenance without disrupting the system's operation.



The study done by Chorus Systems shows that by exploiting the features of the Chorus architecture it is possible to build the kind of real-time system the ESA Columbus project needs.

Today's monolithic operating systems are already too complex and extending their capabilities into the real-time realm will only make them more so. With that complexity comes all the attendant difficulties of upgrading, maintenance and system evolution.

Microkernel architectures such as Chorus, on the other hand, afford system designers the communications orientation and modularity they need to reduce the cost and risks of building advanced, real-time systems.

Marc Guillemont, cofounder and product development director, Chorus Systems

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Still, a distributed architecture isn't simply a matter of physical separation. A sufficiently reduced communications rate—even across a bus—may have the same effect as distributed hardware on a network. Multiple processors that contend inefficiently for shared memory over a backplane may behave slower and less predictably than processors that communicate over a high-speed fiberoptic network.

One way to increase the efficiency

recently." That is, a higher priority process can preempt a process using the kernel code without the preempted process having to complete—it can simply be suspended.

This is a smoother arrangement than previous versions of real-time Unix kernels where the preempting process might start up immediately on an interrupt, preempting the lower level task that had been using kernel resources. And the task would run fine until it tried to get

kernels of this nature are starting to be discussed for inclusion in the POSIX real-time standard.

The decision to move to a true multiprocessing system—where multiple CPUs work on the same application—will make heavy demands on the operating system. But it is a decision designers are making as applications become increasingly demanding.

Multiprocessing architectures

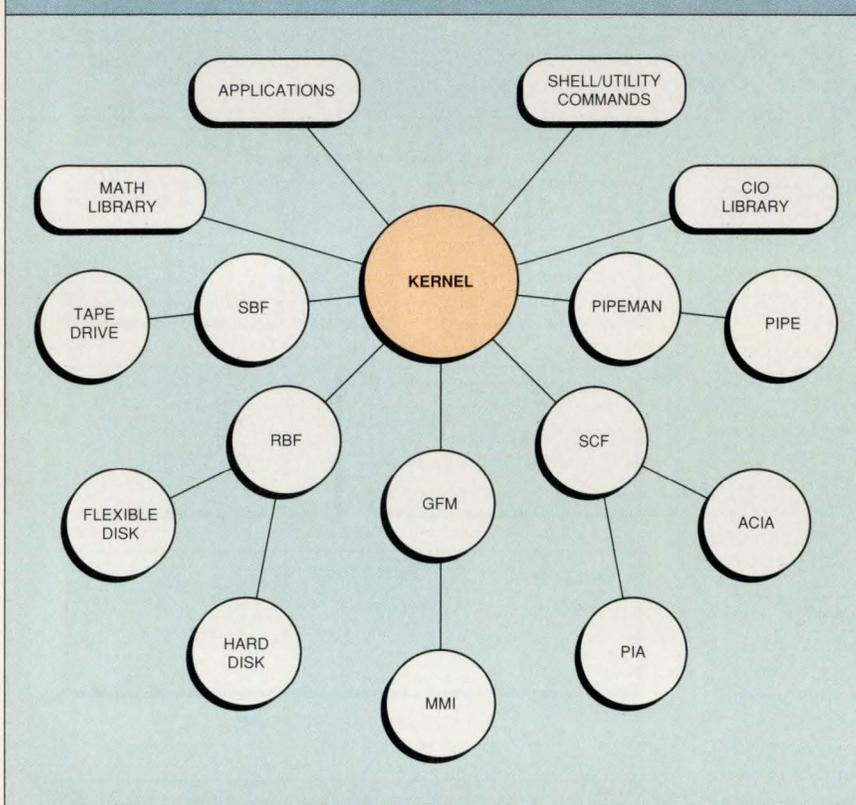
"Multitasking versus multiprocessing is a never-ending dichotomy," says Mike Richmond, product marketing manager for Intel (Hillsboro, OR). "Five years ago it would have taken 10 boards to do the same thing as the CPUs we're selling today with 15- and 20-Mips boards." Still, Richmond admits that the more power people can pull together, the more complex applications they will attempt, and that's where multiprocessing comes in.

The architecture chosen for a multiprocessing real-time system has to be closely orchestrated with the operating system. For example, some schemes dedicate a copy of the operating system kernel to every CPU on the system, while others use a single copy of the kernel to control all the processors. To pass messages and share data between processors, high-speed networking can be used, shared memory over the system bus or a combination of the two.

Richmond, not surprisingly, recommends using a Multibus II architecture running the iRMX operating system in which the system bus can be treated like a high-speed LAN with a packet communications model like Ethernet. "But unlike Ethernet, it's 30 times faster and it's deterministic," says Richmond. It would also allow the same inter-processor communication to be used for remote nodes connected via an actual Ethernet. "The applications programmer can't tell the difference because you have the same Open Systems Interconnection transport software on the backplane that you are running on Ethernet," he says. Except, of course, that there would be differences in speed, which might affect which tasks the programmer chose to assign to which processors.

Speed notwithstanding, any shared memory scheme will have to resolve bus contention. And while that resolution may be the job of the communications software, the operating system and the application

MICROWARE'S REAL-TIME KERNEL-BASED SYSTEM



Microware's OS/9 and OS/9000 operating systems provide a real-time kernel and a host of add-on modules, some of which are proprietary, for run-time libraries, disk and tape access, networking and graphic/multimedia user interfaces. Different combinations of modules can be used to configure systems from single-board embedded controllers to full-blown system controllers, all using the same operating system, application and programming interfaces.

of a Unix-like real-time operating system so that it takes better advantage of single or multiple CPU resources is with a multithreaded kernel. In a single-threaded kernel such as Unix, if a process decides to use a system service within the kernel, it locks out other processes until it is finished.

According to Naren Nachiappan, vice-president of engineering for VenturComm, a multithreaded kernel "allows more than one process to use the kernel's resources concur-

into the kernel, at which point it would be blocked and have to restart the preempted task until that task relinquished kernel resources. With a multithreaded kernel, a higher priority task can preempt a lower priority task for use of the kernel. "If multiple tasks need to request kernel services, they don't mutually exclude each other," says Nachiappan.

VenturComm is not currently working on implementing a multithreaded kernel in its Venix/386 real-time Unix, but multithreaded

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will have to accommodate delays so that the appearance of deterministic behavior is maintained.

When a shared-memory multiprocessor system uses a single copy of the kernel to coordinate all CPUs, it is usually in a very tightly coupled, single-chassis design. Multiple copies of the kernel can extend the concept of a shared memory space over a network. The faster the network—or the bus communication for that matter—the more realistic the feel-

tions within the frame rate of the display. As the simulation model gets more complex, CPUs can be added and the operating system can keep them busy by load balancing or symmetrical multiprocessing. One CPU, however, will usually be dedicated to handling inputs from the pilot's controls and must be dedicated to servicing those interrupts. That CPU will be idling if the pilot doesn't move the controls, but when he does, its interrupt service rou-

(Paris, France). Chorus can be adapted to various memory architectures such as hypercube or bus connected, or to multiple processors across a network. And it can handle different virtual memory schemes including paged virtual memory and segmented memory.

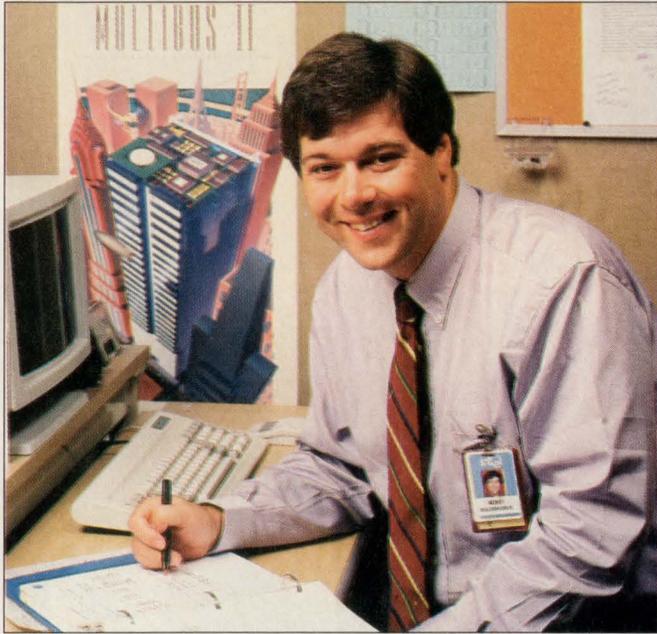
According to Will Neuhauser, president of Chorus's U.S. operation (Beaverton, OR), "Distributed real-time today equals real-time nodes supervised by some non-real-time system. We've worked to provide what people need for real-time performance on single nodes. On multiple nodes we provide a communication mechanism but we don't make any claims about speed or reliability. So much depends on the medium." An application makes calls to Chorus via a Unix System V 3.2-compatible application programming interface (API). Unix calls to the API invoke Chorus processes which can access files, devices and the Chorus nucleus.

The nucleus consists of four main parts. There is a machine-dependent supervisor and three portable parts. These include a real-time executive with 256 levels of priority divided into two types of scheduling.

Half of the priorities are dedicated to real-time preemptive scheduling while the other half use a round-robin type scheduler. All of the priorities in the latter set can be preempted by the real-time priorities. There is also a memory manager for handling virtual memory modes and a communications facility called the IPC (interprocess communication) manager.

Using the services of the IPC, the system is able to pass messages among "threads" which roughly correspond to processes, and which execute within entities known as "actors." An actor defines a protected space in virtual memory and a collection of resources such as memory range and ports. Thus the actor is the execution environment of the thread.

Here, a thread is a different concept than the multithreaded kernel used by VenturComm. A thread is a piece of code that is a sequential flow of control. It is characterized by a context that corresponds to the state of the processor (registers, program counter, stack pointer and so on). A thread is tied to a single actor, although multiple threads can be created and run within the same actor. This gives the system some of the



"Multitasking versus multiprocessing is a never-ending dichotomy," says Mike Richmond, product marketing manager for Intel. "Five years ago it would have taken 10 boards to do the same thing as the CPUs we're selling today with 15- and 20-Mips boards."

ing that there's one system with a single big memory array.

An example of a multiprocessor system that uses shared memory with a single copy of the kernel to coordinate all the processors is Silicon Graphics's (Mountain View, CA) Power Series of project supercomputers running the Irix version of real-time Unix. The Power Series can have from one to eight VME-based CPU cards plugged into its chassis, all of which share common memory. In addition to the multiple CPUs, the Power Series has a set of boards that form the graphics pipeline to scale, clip, rotate, render and finally display the graphics image.

In a flight simulation application, several CPUs might be assigned to cycle a set of equations which model the aircraft—position of control surfaces, aircraft position, instruments and so on—and which compute the out-the-window display that appears to the pilot on the screen or screens. The major time constraint on the system is to do the computa-

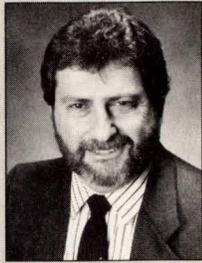
tions generate new variables to plug into the modeling equations and update the display.

This is a point where real-time multiprocessing can differ from non-real-time multiprocessing, where the goal of the latter is often to keep all processors as busy as possible to assure maximum aggregate throughput. In real-time systems, a designer may wish to add an extra margin of safety by dedicating CPU and other hardware resources to servicing critical interrupts, even if it means that processor will often be idle. That is a choice real-time designers can and must be able to make based on the nature of their applications' functions and how much they are willing to pay for an extra margin of safety.

Real time on single nodes

An example of a distributed Unix-like real-time operating system that dedicates a copy of its kernel to each processor node is the Chorus operating system from Chorus Systems

Real-time operating systems for non-real-time applications



Real-time operating systems have become a popular topic in the industry and in the trade press lately because the features inherent in the system make it an ideal solution for a number of applications.

The traditional domain for real-time operating systems has been applications that require deterministic response to time-critical external events. Some examples of this are vehicle simulation, industrial control and telemetry. Each of these applications has an inherent need for fast, predictable response to unsolicited interrupts caused by the occurrence of external events. Without timely acknowledgement and response to real world events there can be a loss of valuable information, material, money and, in some cases, even life.

A common misconception confines real-time operating systems primarily to those applications that require microsecond-type responses. On the contrary, a real-time operating system can offer many benefits to non-real-time applications.

■ Most useful features

Let's take a close look at the features which appear most useful to the widest array of non-real-time applications and why they are beneficial. These features include operating system optimization, priority-based task scheduling, task memory locking, real-time file systems, asynchronous I/O, prioritized disk I/O, real-time interprocess communications and robust interprocess communication.

Operating system optimization cannot exactly be classified as a "feature" of a real-time operating system because it doesn't add functionality but it is quite possibly the most beneficial item on the above list. It is simply the optimization of basic operating system services and functions which let application processes run as quickly as possible.

For example, when Modcomp was implementing Real/IX, its fully preemptive real-time Unix operating system, it exam-

ined all of the standard Unix operating system services and optimized them to improve performance significantly for most applications.

Most non-real-time operating systems have some type of task scheduling algorithm which attempts to distribute CPU time more or less equally to all eligible tasks without regard for the importance of the task. A real-time operating system's priority-based task scheduler allows for the prioritization of tasks according to their relative importance.

A common misconception confines real-time operating systems primarily to applications that require microsecond-type responses.



a hierarchy of emergency situations, each of which is assigned a relative priority.

Task memory locking lets tasks be "preloaded" into system memory before they are actually needed. If an emergency situation occurs, the operating system should not be burdened with loading the required task into memory from disk. Not only is it time-consuming, but additional time may be wasted in swapping out all or part of other lower priority tasks to free up memory.

Many non-real-time applications can also benefit from features found in a real-time file system. There are four main features of a real-time file system to be examined. The ability to allocate contiguous file space on disk coupled with the ability to perform I/O operations using large logical block sizes provides a significant increase in I/O throughput for a task. Applications in the financial and medical communities may greatly benefit from this feature when large amounts of data have to be written to or read from disk.

A real-time file system also includes the ability to write directly to the disk, as well as bypass or complement any memory buffering, such as the Unix operating system's buffer cache facility. This is particularly critical to applications such as on-line transaction processing (OLTP), where the integrity of data written to disk cannot be compromised.

For many applications, such as communications and OLTP, I/O operations can be performed (usually write operations) without requesting the task to wait for the I/O completion. If it is relatively important that the task continue processing as soon as possible, then the asynchronous I/O feature of a real-time operating system is just what is needed. When an asynchronous I/O operation is initiated, the requesting task continues execution and is notified asynchronously of the I/O completion, at which time any final processing may be done.

■ Valuable features

Priority-based task scheduling has proven to be a valuable feature for a variety of non-real-time applications such as in emergency vehicle dispatch systems. An equally important feature is prioritized disk I/O. If a high-priority task initiates a disk I/O operation, that disk I/O request should ideally be performed before any queued disk I/O requests associated with lower priority tasks.

In applications such as hospital monitoring systems, OLTP and MRP, there is frequent communications among operating system tasks. It is important when a task is being sent messages simultaneously by more than one task that it does not lose any of the messages. A real-time operating system includes a robust interprocess communications facility that can handle this requirement.

The features described above are some of the most useful to non-real-time applications and there are numerous other applications than those mentioned which could benefit from the real-time features. In the future, many of these real-time features will become an integral part of what we currently consider non-real-time operating systems.

Alan Scharf, senior product manager, operations systems, Modcomp

REAL-TIME OPERATING SYSTEMS

characteristics of an object-oriented system in that actors are encapsulated like objects and messages are used to invoke action on objects by threads—corresponding roughly to “methods” in classical object-oriented terminology.

Among the advantages of a thread/actor arrangement are a kind of load balancing in a multiprocessor environment. Also, context switching for threads involves far less overhead than would an actor context switch. Threads within an actor can preempt each other with more speed because the actor's resources do not have to be saved. Actors, however, being virtual memory entities, are not always at the

support up to 16 processors on a single bus with a copy of MTOS on each processor board. According to Industrial Programming's Mushinsky, while some customers have indeed implemented 16-processor systems on proprietary buses, the more usual configuration holds from four to six processors.

Tasks are classified as either local or global. Local tasks reside and execute in the on-board memory of an individual processor. Global tasks are stored in shared memory and accessed by individual processors across the system bus. They execute in the on-board memory of whichever processor picks them off the ready queue.

In an MTOS system, the user can add CPUs to a chassis, redistribute tasks and immediately increase throughput without changing the application code. “We provide a safety net if you find you can't get the job done, which is different than standing there preaching fire and brimstone about determinism,” Mushinsky says.

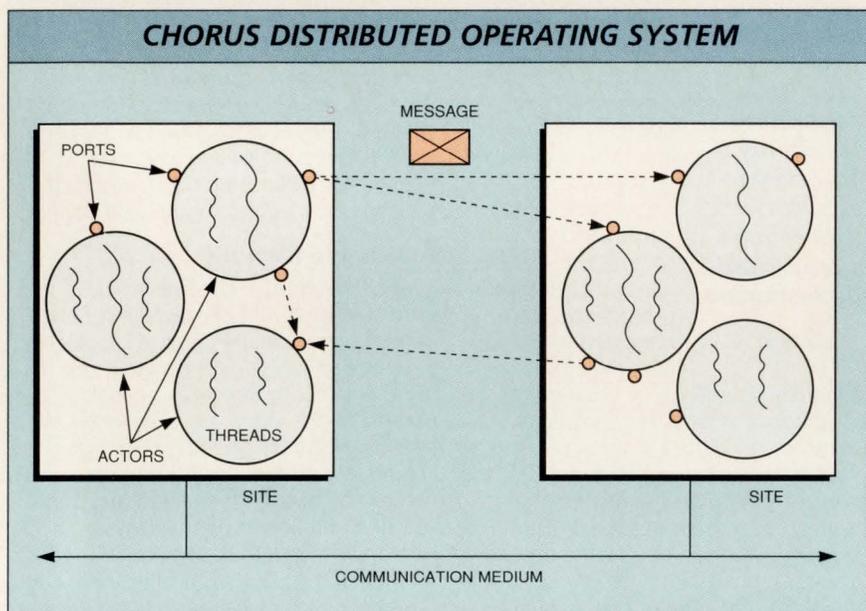
In a system where several processors must access the same memory there will undoubtedly be contention for memory access, and timing will be less predictable for global tasks than for local tasks. MTOS itself makes no assumptions about the communications scheme or conflict resolution. That is handled by bus contention hardware or other communication software.

In very large multiprocessor distributed systems, the problems of counting microseconds of latency time pale before the immense complexity that applications can acquire. A 256-node system, no matter how fast its response, could run applications so complex that no programmer could verify—let alone predict—what combinations of events might confront the system or exactly how it would respond.

Exhaustively testing all the code in such huge systems is unfeasible. “It's not possible to test all possible paths,” says Wind River's Fiddler. “Even if we gave the designer a system that says, ‘This is exactly how it will operate in every case,’ the behavior would still be so complex that even if expressed in differential equations it wouldn't do anybody any good. The formula would be unsolvable anyway.” Thus it is the sheer complexity of real-world applications—not a breakdown of so-called determinism—that appears to be the real barrier to very large distributed real-time systems based on multiprocessors.

A different paradigm

When the phone system routes a call between Phoenix and Buffalo, the call doesn't travel the same path every time. The system routes the call based on network traffic and other conditions that cannot be predicted. But the call goes through. That is the mission of the phone system. Similarly, a very large real-time system is oriented toward a single mission, such as keeping a plane in the air or managing a nuclear plant where many unforeseen scenarios can arise. But fulfilling



In the Chorus operating system, messages are used for threads to move via ports to execute in actors. Threads are analogous to processes, while actors are passive, encapsulated areas of virtual memory with sets of resources such as memory space, data structures and ports. Threads can move among actors in the same site (processing node) or move among sites transparently via a network.

same physical location.

According to Neuhauser, “We're working on partitioning hardware responsibility as well. Currently, there's no way to lock a thread onto a given processor.” This means that to ensure response time fast enough for critical interrupts, the aggregate power of the system will have to be sufficiently upgraded.

Global and local tasks

One way to combine load balancing with the ability to dedicate hardware to critical tasks has been devised by Industrial Programming with its MTOS operating system. A multiprocessor MTOS system can

It is important that global tasks execute in the same locations in each local processor's memory because a running global task might be preempted, have its context saved and go back on the ready queue to be picked off by the next available processor. In this way global tasks may seem to roam from CPU to CPU, but it is only their execution, not their code.

Global tasks tend to be assigned lower priority than local tasks. Global tasks can take advantage of load balancing, while local tasks are bound to specific CPUs and may require immediate processing of mostly local data.

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CIRCLE NO. 57



Object orientation allows kernel solution



Software is becoming the central technological challenge of our time. Processors are getting faster and more powerful, memory is getting bigger and cheaper and communications speeds are increasing. All of these are making applications, and therefore software, larger, more complex and more difficult to develop. Applications are exceeding our capability to design and implement them promptly and reliably, even those deployed in life-critical situations.

What's the answer? One approach is to look at the most complex engineering feats in nature and try to learn from them. How did nature create plants, animals and people? Through evolution. No one sat down at a drawing board and designed the human body. The design of the whole and the components—muscles, nerves, brain—evolved over time.

How can we, as software designers, apply evolution to software and become omnipotent directors of an evolutionary process by which software evolves into systems as complex and reliable as the human body? Unfortunately, no one has yet developed a way to make software evolve by itself. We can, however, structure our software in a way that its functionality and reliability can be incrementally improved. Object orientation is a modest step in that direction.

A common structure

The latest release of the VxWorks real-time operating system, Version 5.0, draws heavily on object-oriented concepts in the internal design of its kernel and in its overall structure. The operating system defines a number of classes of objects, all of which share a common structure. These object classes include binary, counting and mutual exclusion semaphores, watchdog timers, message queues, symbol tables, tasks and memory partitions. All of the object classes have a number of methods associated with them. A method is essentially a subroutine that operates on data in the object. Methods common to all VxWorks objects include create, init, de-

stroy, show and help.

By structuring the software in this way, several advantages are achieved. First, the data itself is encapsulated by the methods. Therefore, a higher level routine doesn't need to know about the internal operation of a particular object; it merely needs to know how to call a method—and this calling sequence is the same for all classes of objects. For instance, a single routine can call the show method (which provides some human-readable information about the status of the object) for all objects. Whether it is showing information about a task or a memory partition, the call is the same. The higher level routine doesn't need to know anything about the structures of the objects themselves, which are, of course, quite different internally.

Another advantage is provided by runtime binding. Code is bound only to the objects it uses only by an object ID, which is returned by the system when the object is created. The underlying object may change without recompiling or modifying the code that uses the object.

One major motivation for object orientation is the realization that we don't know all the answers.



important of these is the queue class. Much of an operating system's behavior is determined by the data structures and queueing algorithms it uses internally. Some of the queue algorithms VxWorks has defined are singly-linked list, doubly-linked list, delta-queue, heap and bitmap queue. Each of these algorithms has different characteristics that make it appropriate for different applications. For instance, the bitmap queue is a structure unique to VxWorks that has the advantage that nodes can be inserted, ordered, moved and removed quickly and in constant time. The disadvantage is that it is memory-intensive. It is very appropriate, for instance, for the task ready list where the advantages outweigh the disadvantages.

By contrast, the singly-linked list is very memory efficient but the time nec-

essary to insert in a sorted order increases with the number of items on the list. The singly-linked list is often appropriate for a semaphore queue, where the queue is usually quite small.

By defining all these objects and binding them at run time, the default decisions can be changed. This might occur for several reasons. The application programmer might decide that, for a particular semaphore, the bitmap queue is a more appropriate data structure than the default singly-linked list. Or if an application programmer needs a queue based on some completely different structure, he can write it himself. Different data structures can be distributed later by designers or by third parties with no change, recompilation or rebuilding of the code that uses the queue.

Plan for tomorrow

One motivation for object orientation is the realization that we don't know all the answers. A real-time operating system that's state-of-the-art today will be obsolete and inadequate tomorrow unless it is designed to grow and change. Designers can add a hard deadline scheduler or rate-monotonic scheduler, a new interprocess communications paradigm or whatever is demanded next year or in five years with minimum disruption to the existing operating system and applications. We can improve the system incrementally rather than wholesale.

VxWorks is not yet fully object-oriented. There is no inheritance, for instance. Inheritance allows convenient creation of new classes based on an existing class. But it is difficult to implement in a way that is efficient enough for a hard real-time system. It also requires support at the language/compiler level. Also, there is no binding to a true object-oriented language yet, although this will probably come later.

Even today, though, the system benefits greatly from the limited object-oriented structure that we have implemented. Although a good deal of that structure is below the surface, application programmers will benefit from a more maintainable system that will resist obsolescence and evolve with their needs. It works for biology and it will work for software.

Jerry Fiddler, president, Wind River Systems

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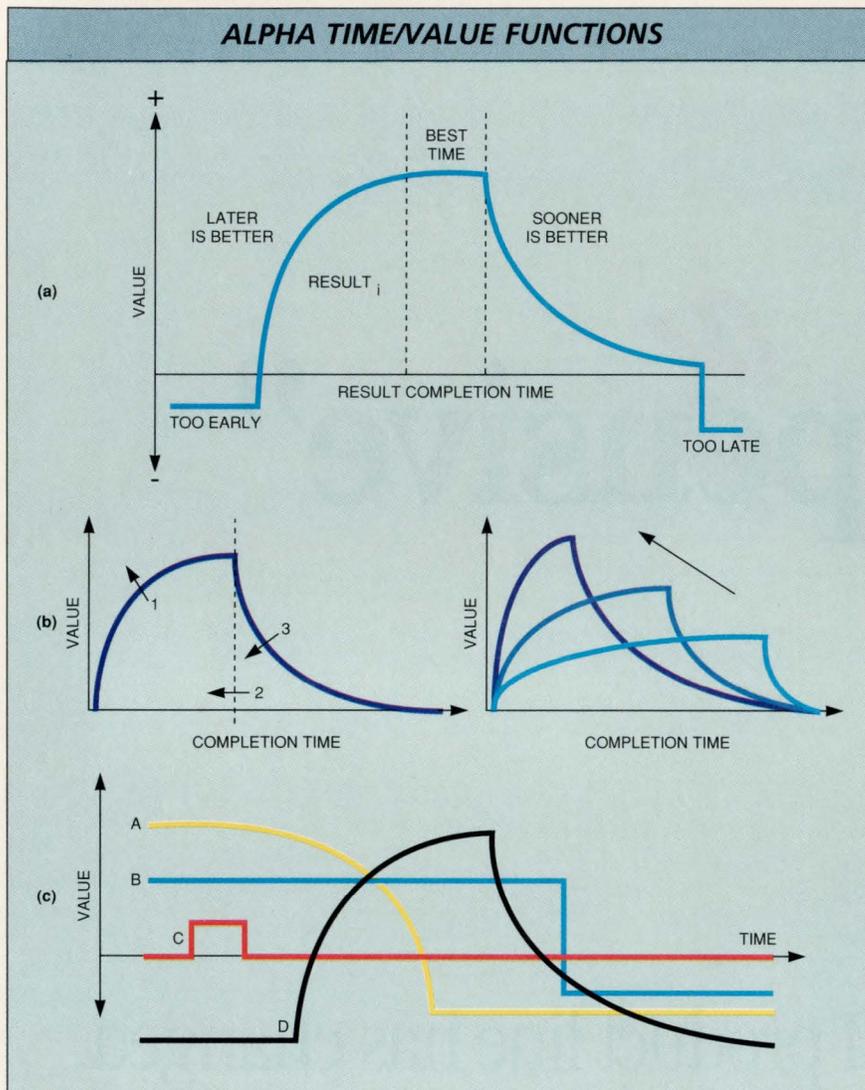
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(a) Using a generalized Alpha time/value function to represent firing at an incoming missile, the graph shows a time when firing too early is of little or no value, an optimum time window to fire and a time past which firing becomes increasingly less valuable. (b) In a course correction for an interceptor, curve segments 1 and 2 show the best time for course change and the absolute deadline, respectively, where both depend on predicted time-to-intercept. Curve segment 3 is determined by the perceived threat of target. If the perceived threat increases (right), it will also influence the other two factors, causing, for instance, an earlier absolute deadline. (c) Alpha evaluates time/value functions collectively for all contending results, where the results have been scheduled according to an application-defined plan to maximize their accrued value to the system.

the mission is the overall purpose of the system, and different real-world conditions may dictate different strategies for accomplishing it.

Real-time systems, no matter how large, are still characterized by time constraints. The right answer late is still wrong. But, according to E. Douglas Jensen, chief scientist and director of R&D at Concurrent Computer (Westford, MA), real-time constraints are two-dimensional. On one axis is the urgency, or time criticality; on the other axis is the im-

portance, or functional criticality, to the system. So a strict integer-based priority cannot adequately describe the time constraint, especially when other functions are contending for the system's attention. A programmer may have been able to sort out some strict priorities in a small system and test them thoroughly but that paradigm breaks down as complexity increases.

Firing at an incoming missile, for example, would rate very high on the functional criticality axis. The

graph would include a time when firing too early would be of little or no value, an optimum time window to fire and a time past which firing becomes increasingly less valuable or useful. In the overall scenario, there may be circumstances when taking evasive action is of higher functional (survival) value to the system than firing. Evasive action, too, has a time window where it may be of little value if done too early, an optimal time and a time when it's just too late. The system, at any given instant, must be able to resolve the conflicting demands of the two options and their relative values in a way that is optimal to the overall mission of the system.

The Alpha operating system developed at Concurrent would characterize the missile scenario as two functions with soft time constraints. A hard time constraint would be one which, if not satisfied, would have either zero or negative value to the system. A classical binary deadline—detecting the missile in time to sort out the options or not—is an example of a hard time constraint. Alpha tasks can be classified according to hard and soft time constraints or as combinations of the two.

Unpredictability accepted

Alpha abandons the idea of determinism on the large scale, but not the idea of speed or deadlines. It can link together small local nodes (event controllers) that run kernels such as Ready Systems's VRTX or Software Components Group's pSOS⁺, where the kernels can respond to local interrupts as deterministically as they ever did.

Such unpredictability makes people understandably nervous, but it is an unpredictable world that dictates the need for a flexible system that is itself not internally predictable. Large-scale real-time systems are faced with the dilemma of accommodating uncertainty while assuring dependability.

Such uncertainties call for dynamic resource management by the application with the assistance of the operating system. Admittedly, there may be circumstances (such as an overwhelming onslaught of missiles) that the system won't be able to handle. "But if we just abandon doing things that we don't completely understand, we're in big trouble," Jensen says. So elaborate ways of sorting priorities from among these complex time/value

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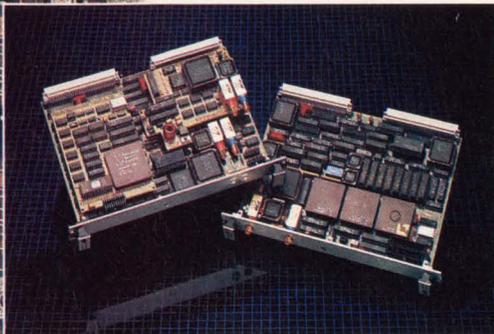
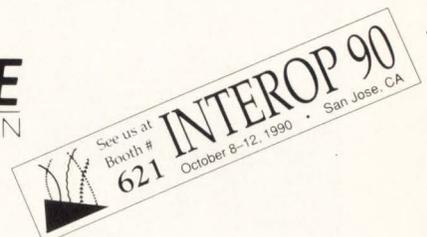
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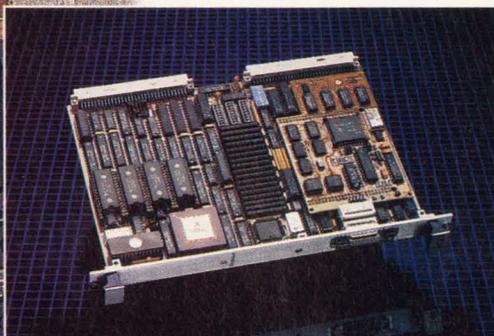


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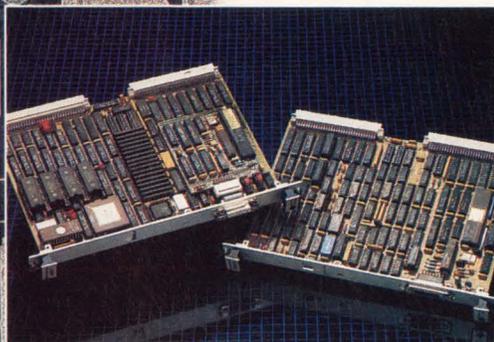
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CIRCLE NO. 59

REAL-TIME OPERATING SYSTEMS

functions will aid the application designer in approaching the optimal mix of flexibility and reliability. These methods could range from simple algorithms to approaches that include artificial intelligence and expert systems.

As a global, distributed operating system, Alpha is object-oriented and can be spread among many computing nodes on a system via shared

memory. A system can consist of multiple processors in a backplane and multiple backplanes connected via a network, usually Fiber Distributed Data Interface (FDDI), although Ethernet is possible. The network essentially acts as a means of extending the shared memory space among remote nodes. Alpha's computing model uses a concept of threads similar to those described

for Chorus, except that threads activate and execute in "objects."

While threads—which may be thought of as wandering virtual processors implemented in software—are not confined to an address space or even to a node, each object has a private address space that serves to encapsulate the object. When the thread—as a sort of locus of execution—moves to an object, it executes that object's code and then moves to the next object, bringing with it the machine states, values and attributes it has acquired from executing the previous object.

Alpha, which Concurrent plans to place in the public domain early next year, has recently undergone technical evaluation by the Navy's Next Generation Computing Resources program, where it beat out POSIX to come in first.

Whether Alpha or some as-yet undiscovered approach proves ultimately to be the wave of the future, it is clear that we will have to change our thinking about what large-scale real-time systems are supposed to do. What those changes will be is still unclear. Can we be comfortable with the idea that systems can work reliably even if we can't predict the details of their inner behavior? Can we live with systems, even trust our lives to them, if there is no way to test them in exhaustive detail? These questions raise cultural and emotional issues as well as the technical. One thing is sure. A bigger hammer alone won't do the job. ■

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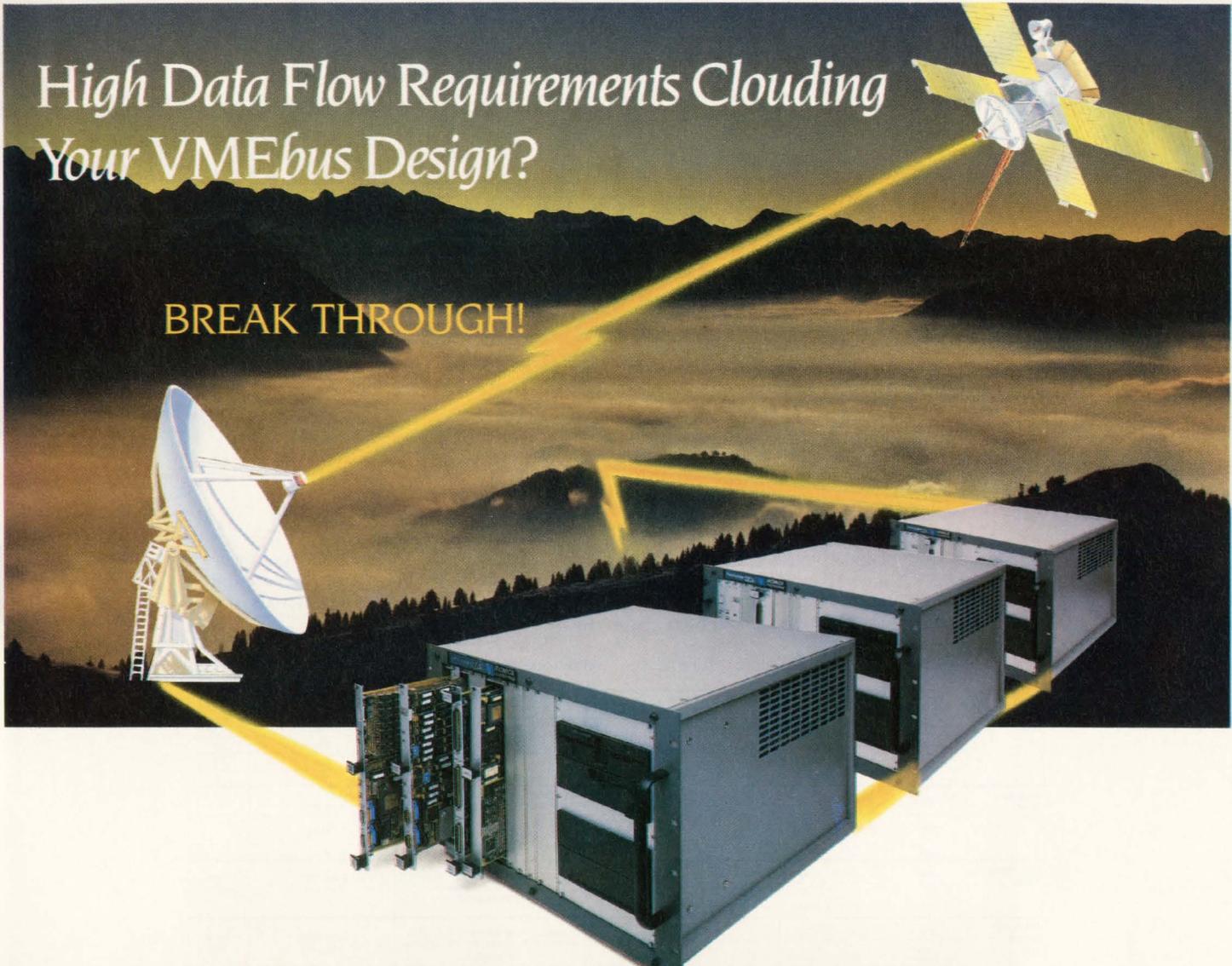
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CIRCLE NO. 60

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Component Family	Memory Size (Total)	Org. (Bits)	Speed (ns)	Package						Special Features	Availability	Military Qualified
				DIP	ZIP	SOJ	PLCC	TSOP	PQFP			
SRAMs	1MEG	x1,x4,x8	25-45	X		X				x4 option: OE	Now	2H90
	256K	x1,x4,x8	20-45	X	X	X				x4 option: OE	Now	X
	64K	x1,x4,x8	12-45	X		X				x4 options: Separate I/O, OE	Now	X
	16K	x1,x4,x8	12-45	X		X				x4 options: Separate I/O, OE	Now	X
Cache Data SRAMs	288K	x9	14-34				X			486 Compatible, Self-timed write, Fast toe 7ns, 486 Burst and extended burst support	Samp: 1H91, Prod: 2H91	
	144K	x18	20-35				X	X		386/486 Compatible, Fast toe 8ns, Auto write completion, Parity bits	Now	
	128K	x16	20-35				X	X		386 Compatible, Fast toe 8ns	Now	
Synchronous SRAMs	288K	x18	15-25				X			Registered address, chip enables and write control; Data latch, Fast toe 6ns, Byte write capability	Samp: 2H90, Prod: 1H91	Samp: 1H91
	256K	x16	15-25				X					
SRAMs with Address Latch	288K	x18	15-35				X			Address, data and chip enable latches; Byte write capability, Fast toe 6ns, 3.0 Volt output buffer option	Samp: 2H90, Prod: 1H91	Samp: 1H91
	256K	x16	15-35				X					
	16K	x8	100	X		X				Intel 8051 and 8096 compatible	Now	X
	16K	x8	15-35	X		X				Compatible with high end micro controllers	Now	X
FIFOs	18K	2Kx9	15-35	X			X			Family options: 300 mil DIP package, Programmable flags	Samp: 1H91	2H91
	9K	1Kx9	15-35	X			X				Samp: 1H91	2H91
	4.5K	512x9	15-35	X			X				Samp: 1H91	2H91
DRAMs	4MEG	x1,x4,x8,x16	60-100	X	X	X		X		x4,x8 options: Write per bit x16 options: 2 WE/1CAS, 1WE/2CAS and 1WE/1CAS with write per bit	x1,x4 Samp: Now, Prod: 1H91; x8,x16 Samp: 1H91	Samp: 1H91
	1MEG	x1,x4,x16	70-120	X	X	X		X		x16 options: Byte write or write per bit	Now	X
	256K	x1,x4	100-120	X	X	X		X			Now	X
	64K	x1	100-150	X			X				Now	X
Quad CAS DRAMs	4MEG	x4	60-100			X				Separate CAS control for each DQ input/output, Enhanced write per bit capabilities	Samp: 1991	
	1MEG	x4	70-100			X					Now	
Pseudo Static DRAM	1MEG	x8	80-120	X		X		X		Unmultiplexed addresses, Simple refresh control	Samp: 2H90, Prod: 1H91	
Dual Port DRAMs (VRAMs)	1MEG	x4,x8	80-120		X	X				CMOS, Fully static SAM, Serial input, Split read transfer	Now	Samp: 1H91
	256K	x4	100-120	X	X					CMOS, Fully static SAM, Serial input	Now	X
Triple Port DRAMs	1MEG	x4,x8	80-120			X	X			CMOS, Two fully static SAMs, Transfer mask, Split transfers, Functional superset of 1MEG VRAM	Samp: Now, Prod: 2H90	
DRAM Modules	2MEG, 1MEG, 512K, 256K	x36	70-120		X		X			Industry standard pin-out	256K, 512K: Now; 1MEG, 2MEG Samp: 2H90	
	4MEG, 1MEG, 256K	x9	70-120			X	X			Industry standard pin-out	256K, 1MEG: Now; 4MEG Samp: 2H90	
	4MEG, 1MEG, 256K	x8	70-120			X	X			Industry standard pin-out	256K, 1MEG: Now; 4MEG Samp: 2H90	
SRAM Modules	256K, 128K, 64K, 16K	x32	15-45		X					Industry standard pin-out with OE	16K, 64K: Now; 128K, 256K: 2H90	1H91
	64K, 32K	x16	30-45	X						Industry standard pin-out with OE	Now	1H91
	128K	x8	30-45	X						Compatible with 1MEG monolithic	Now	1H91

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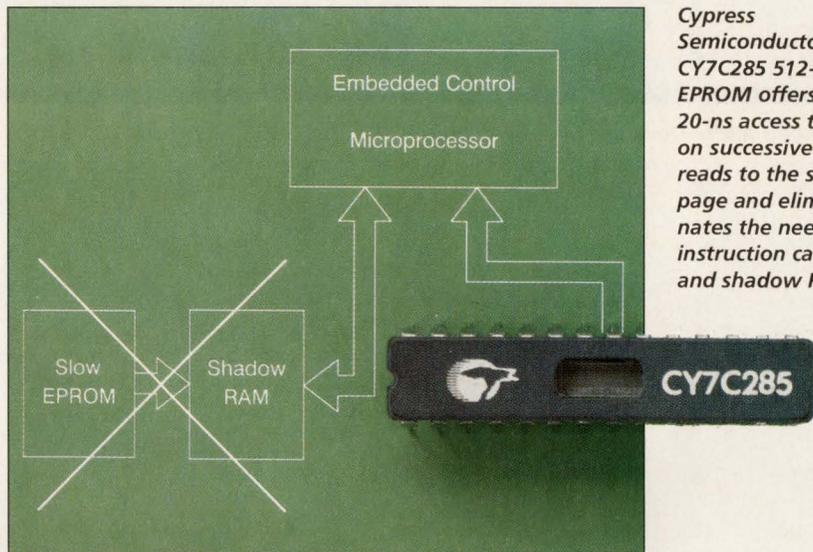
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CIRCLE NO. 62

INTEGRATED CIRCUITS

EPROMs get denser, faster and cheaper to hold PROM market lead

Jeffrey Child, Associate Editor



Cypress Semiconductor's CY7C285 512-kbit EPROM offers 20-ns access times on successive reads to the same page and eliminates the need for instruction caches and shadow RAMs.

Increasing densities, higher speeds and reduced power consumption are making EPROMs more suited to a wide range of niche applications. System designers are using higher density EPROMs, for instance, in high-volume embedded applications such as laser printers, electronic games, cellular phones and fax machines—all of which require that large quantities of code receive occasional updates. EPROMs with faster access speeds are also finding a niche in systems designed around high-speed microprocessors in workstations and mainframes.

The industry sees a jump in EPROM density every few years. As each density emerges, manufacturers compete to make their products faster and cheaper. Last year two companies combined efforts to produce the industry's fastest 1-Mbit EPROM. Advanced Micro Devices (Sunnyvale, CA) provided the fabrication facility, and International CMOS Technology (San Jose, CA) provided the design, creating a device that accesses data at speeds down to 45 ns. Although ICT announced the device first, both companies hold marketing rights for the product.

As densities increase, the demand for $\times 16$ configurations rises. Providing better modularity, a $\times 16$ EPROM interfaces easily with 16-bit microprocessors and microcontrollers. With a 4-Mbit EPROM part organized as 512k \times 8 bits, for example, data must be stored in groups of

512 kbits. When organized as 256k \times 16 bits, an EPROM with the same 4-Mbit density permits memory storage in smaller increments.

As the accompanying charts show, most manufacturers are meeting demands for high-density $\times 16$ EPROMs. Mitsubishi offers a 4-Mbit, 256 \times 16-bit device. Offered in a 40-pin ceramic DIP, the M5M27C402k has a 100-ns access time.

But achieving a $\times 16$ organization presents some hurdles at higher speeds. "To implement a $\times 16$ organization, you must contend with a lot of grounding and noise concerns," says Robin Jigour, director of marketing for ICT. "The chip must be laid out to accommodate those concerns. With those design rules, the speed is forced down from 5 to 10 ns."

Handling burst mode

Although speed and density are the features that typically distinguish EPROM products, some manufacturers differentiate their EPROMs by adding features to cope with burst-mode operations. The added features take advantage of some of the speed-enhancing characteristics already present in microprocessor architecture.

One such device is the 1-Mbit 27960 EPROM from Intel, which takes advantage of the burst-mode feature found in devices such as Intel's 80960. In burst mode, a microprocessor inserts an address by loading that address plus four or more succeeding addresses. In this

way the 27960 can send data from an address as well as from the four succeeding locations. The EPROM can then burst that data onto the bus at a zero wait state. The logic to implement this feature is very small, allowing zero-wait-state performance without much added cost, according to Intel.

Taking the next step in adapting to burst-mode operations, Cypress Semiconductor (San Jose, CA) offers a 64k \times 8-bit Fast-Column EPROM with two access times. At 75 ns, the initial read accesses a 64-byte page of the EPROM. Subsequent accesses require only 20 ns until an address goes beyond the current page. The part is available in two styles: the basic CY7C285 and the CY7C289, which offers additional chip-select pins and an internal address register/latch. Up to 16 of these EPROMs can be attached to a Cypress 40-MHz Spare chip.

Cypress's CY7C287 is another high-performance 512-kbit EPROM with special features. This part contains registers on its outputs, eliminating the need for external registers. "People frequently want to bring data out and hold it, and then strobe it and get it exactly when they want it," says Joe Nichols, PROM product marketing manager at Cypress. "To do this, they typically use external registers. The CY7C287 incorporates those registers internally into its circuitry."

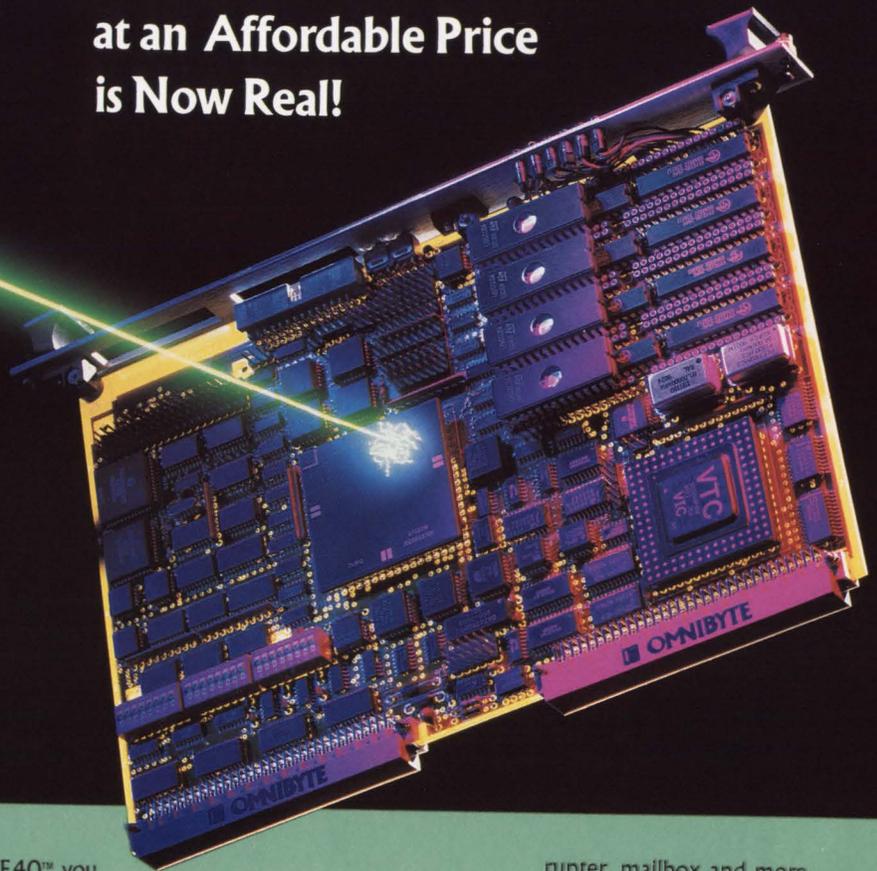
Despite these latest performance enhancements and the new applica-

PRODUCT FOCUS/High-density EPROMs

Model	Process	Organization (bits)	Access time (ns)	Programming time (s)	Current operating/standby (mA)	Packages	Price (quantity)	Comments
Advanced Micro Devices 901 Thompson Pl, PO Box 3453, Sunnyvale, CA 94088-3453 (800) 222-9323 Circle 301								
AM27C256	CMOS	32k×8	55 to 300	10	25/100 μA	CDIP, LCC, PDIP, PLCC	\$3.30 to \$4.30 (100s)	—
AM27C512	CMOS	64k×8	70 to 300	15	40/100 μA	CDIP, LCC, PDIP, PLCC	\$5.15 to \$5.75 (100s)	—
AM27C010	CMOS	128k×8	100 to 300	30	30/100 μA	CDIP, LCC, PDIP, PLCC	\$9.30 to \$13.95 (100s)	—
AM27C100	CMOS	128k×8	100 to 300	30	30/100 μA	CDIP, LCC, PDIP, PLCC	\$9.30 to \$13.95 (100s)	ROM-compatible pinout, EIAJ
AM27C1024	CMOS	64k×16	90 to 300	30	50/200 μA	CDIP, PLCC, PDIP, PLCC	\$11.80 to \$19.65 (100s)	—
AM27C020	CMOS	256k×8	100 to 300	60	30/100 μA	CDIP, LCC, PDIP, PLCC	\$21.45 to \$24 (100s)	—
AM27C2048	CMOS	128k×16	100 to 300	15	50/100 μA	CDIP, LCC, PDIP, PLCC	\$28.75 to \$44.20 (100s)	—
AM27C040	CMOS	512k×8	150 to 300	120	40/100 μA	CDIP, LCC, PDIP, PLCC	\$57.20 (100s)	—
AM27H010	CMOS	128k×8	45 to 90	30	30/—	—	\$27 to \$40 (1,000s)	—
Atmel 2125 O'Nel Dr, San Jose, CA 95131 (408) 441-0311 Circle 302								
AT27C256R	CMOS	32k×8	90	0.1 ms/byte	20/100 μA	CDIP, CLCC, LCC, PDIP	\$4.70 (1,000s)	—
AT27C512R	CMOS	64k×8	120	0.1 ms/byte	20/100 μA	CDIP, CLCC, LCC, PDIP	\$5.60 (1,000s)	—
AT27C010	CMOS	128k×8	120	0.1 ms/byte	25/100 μA	CDIP, CLCC, LCC, PDIP	\$9.30 (1,000s)	—
AT27C1024	CMOS	64k×16	120	0.1 ms/byte	30/100 μA	CDIP, CLCC, LCC, PDIP	\$11.10 (1,000s)	—
Catalyst Semiconductor 2231 Calle de Luna, Santa Clara, CA 95054 (408) 748-7700 Circle 303								
CAT27HC256	CMOS	32k×8	55, 70, 90, 120	100 μs/byte, 1 ms/byte	60/40	CERDIP, DIP, LCC	\$8 (10,000s)	available in industrial and military temperature ranges
CAT27HC256L	CMOS	32k×8	70, 90, 120	100 μs/byte, 1 ms/byte	60/500 μA	CERDIP, LCC, PDIP	\$9 (10,000s)	same as above
CAT27HC010	CMOS	128k×8	70, 90, 120	100 μs/byte, 1 ms/byte	60/500 μA	CERDIP, PDIP	\$13.50 (10,000s)	same as above
CAT27C210	CMOS	64k×16	150, 170, 200, 250	100 μs/byte, 1 ms/byte	50/100 μA	CERDIP, PDIP, PLCC	\$12 (10,000s)	same as above
Cypress Semiconductor 3901 N First St, San Jose, CA 95134 (408) 943-2902 Circle 304								
CY7C271	CMOS	32k×8	35	—	120/30	DIP, LCC	\$142 (100s)	auto power-down, 45-ns military
CY7C274	CMOS	32k×8	35	—	120/30	DIP	\$142 (100s)	EPROM pinout, 45-ns military
CY7C277	CMOS	32k×8	30/15	—	120	DIP, LCC	\$153 (100s)	output registers, 40/20 military
CY7C279	CMOS	32k×8	35	—	120/30	DIP, LCC	\$139 (100s)	address registers/latches, 45-ns military
CY7C285	CMOS	64k×8	55/20*	—	180	DIP	\$204 (100s)	*20 ns for successive access to same memory page
CY7C286	CMOS	64k×8	55/20*	—	120	DIP	\$193 (100s)	EPROM pinout
CY7C287	CMOS	64k×8	55/20*	—	160/—	DIP	\$265 (100s)	output registers
CY7C289	CMOS	64k×8	55/20*	—	180/—	DIP	\$265 (100s)	address registers/latches, on-chip select decoding

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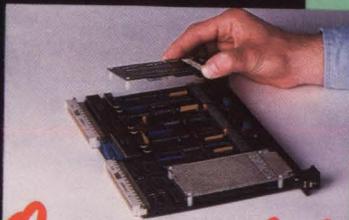
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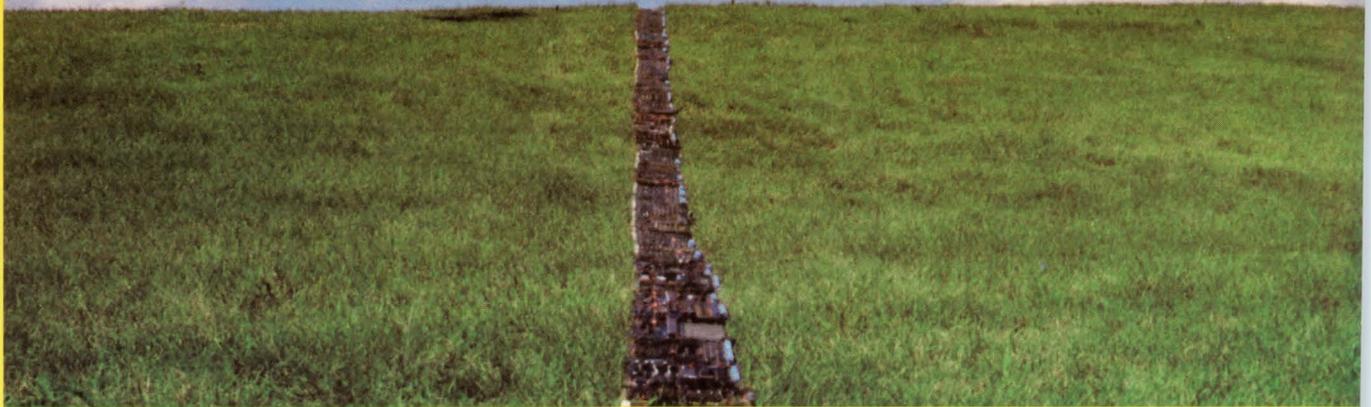


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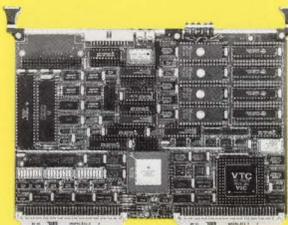
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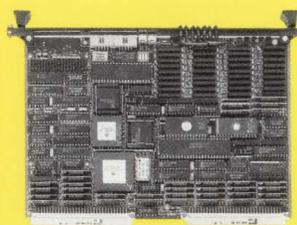
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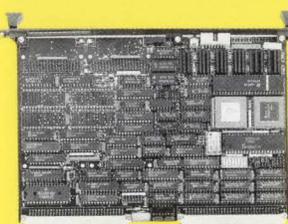
- 68020 16.66 - 33 MHz CPU
- (8) 28-pin RAM sockets for up to 265KB of dual-access zero-wait-state RAM
- (8) 32-pin sockets for up to 8MB of ROM, (4) sockets may be EEPROM
- (2) RS232C asynch serial ports
- (16) lines of parallel I/O
- (1) OMNIMODULE socket for a wide variety of I/O (i.e. 2 serial ports, 20 parallel lines)
- VICO68 VME Interface Controller

OB68K/VSBC20™ VME SINGLE BOARD COMPUTER



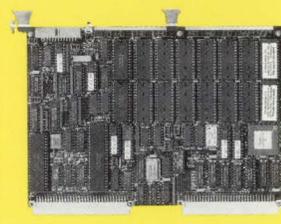
- 68020 16-33MHz, CPU
- 1-4 MB of dual-access, zero-wait-state DRAM with parity
- 68882 (optional)
- (2) 32-pin ROM sockets
- (2) RS232C serial ports
- (2) 8-bit parallel ports
- (1) OMNIMODULE socket for a wide variety of I/O (i.e. 2 serial ports, 20 parallel lines)
- 4 level bus arbiter (optional)

OB68K/VSBC1™ VME SINGLE BOARD COMPUTER



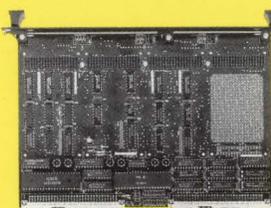
- 68000 12.5MHz 16/32 bit CPU
- 512KB of dual-access, zero-wait-state DRAM with parity
- (4) 28-pin ROM sockets
- (3) 16-bit counter/timers
- (2) Omnimodule™ I/O sockets for a wide variety of I/O (i.e. 4 serial ports, 40 parallel lines)
- DMA controller (optional)
- VME bus interrupt generator (optional)
- Optional 4 level bus arbiter
- Two year limited warranty

OB68K/VME1™ VME SINGLE BOARD COMPUTER



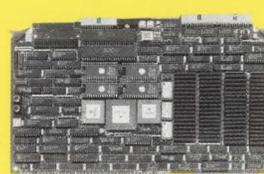
- 12.5 MHz 68000 CPU
- (8) pairs of 28-pin sockets for RAM or ROM
- (2) RS-232C serial ports
- (2) 8-bit parallel I/O ports
- System Controller

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- 68882 Math Co-Processor (optional)
- 2 channel DMA controller (optional)
- (2) RS232c synclasync serial ports
- (2) 8-bit parallel ports
- (1) OMNIMODULE™ socket
- (4) 32-pin ROM sockets

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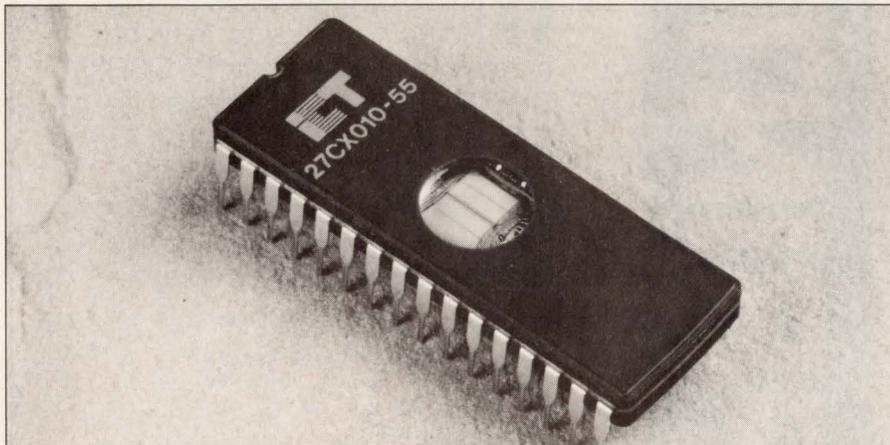
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Model	Process	Organization (bits)	Access time (ns)	Programming time (s)	Current operating/standby (mA)	Packages	Price (quantity)	Comments
Fujitsu Microelectronics, IC Div 3545 N First St, San Jose, CA 95134 (800) 642-7616						Circle 305		
27C256A	CMOS	32kx8	150	1-ns pulse	—	DIP, LCC	\$4 (1,000s)	2 pulses typical
27C512	CMOS	64kx8	150	1-ns pulse	—	DIP, LCC	\$5 (1,000s)	same as above
27C1001	CMOS	128kx8	150	1-ns pulse	—	DIP, LCC	\$8 (1,000s)	same as above
Hitachi America, Semiconductor & IC Div 2000 Sierra Point Pkwy, Brisbane, CA 94005 (800) 448-2244						Circle 306		
HN27C101A	CMOS	128kx8	120 to 250	14	50/20 μ A	CERDIP, flatpack, PDIP	\$8.70 to \$10.70 (1,000s)	—
HN27C1024	CMOS	64kx16	100 to 120	200 μ s	100/25	CERDIP, JLCC	\$13.35 to \$17.35 (1,000s)	PLCC in 4Q90, 85-ns part available in JLCC only
HN27C4096	CMOS	256kx16	100 to 150	3.5	100/20 μ A	CERDIP, JLCC	\$70.65 to \$91.35 (1,000s)	PLCC in 1Q91
Intel 1900 Prairie City Rd, Folsom, CA 95630 (916) 351-8080						Circle 307		
27256	HMOS	32kx8	170, 200, 250	4	100/40	CERDIP	\$3.50 (10,000s)	extended temperature, burn-in
27C256	CHMOS	32kx8	120, 150, 200	4	30/100 μ A	CERDIP, PDIP, PLCC	\$2.50 (10,000s)	extended temperature, burn-in
87C257	CHMOS	32kx8	150, 200	4	15/100 μ A	CERDIP, PLCC	\$4.15 (10,000s)	—
27513	HMOS	4x16kx8	170, 200, 250	6 min	125/40 μ A	CERDIP	\$7.90 (10,000s)	—
27512	HMOS	64kx8	170, 200, 250	6 min	125/40 μ A	CERDIP	\$3.90 (10,000s)	extended temperature, burn-in
27C512	CHMOS	64kx8	120, 150, 200	8	30/100 μ A	CERDIP	\$3.90 (10,000s)	—
27C011	CHMOS	8x16kx8	200	15	30/100 μ A	CERDIP	\$8.30 (10,000s)	—
27C010	CHMOS	128kx8	120, 150, 200	15	30/100 μ A	CERDIP, PDIP, PLCC	\$7.50 (10,000s)	—
27C210	CHMOS	64kx16	130, 150, 200	8	50/100 μ A	CERDIP, PLCC	\$8.80 (10,000s)	extended temperature, burn-in
27960KX	CHMOS	128kx8	—	17	125/30 μ A	CERQUAD, PLCC	\$15 (10,000s)	burst mode: 16, 20, 25 MHz
27960CX	CHMOS	128kx8	—	17	125/30 μ A	CERQUAD, PLCC	\$17.50 (10,000s)	burst mode: 16, 20, 25, 33 MHz
27C020	CHMOS	256kx8	150, 200	30	30/100 μ A	CERDIP, PDIP, PLCC	\$16.30 (10,000s)	—
27C220	CHMOS	128kx16	150, 200	15	50/100 μ A	ceramic, PLCC	\$17.90 (10,000s)	—
27C040	CHMOS	512kx8	150, 200	60	50/100 μ A	CERDIP	\$49 (10,000s)	—
27C240	CHMOS	256kx16	150, 200	30	50/100 μ A	—	\$75 (100s)	—
International CMOS Technology 2125 Lundy Ave, San Jose, CA 95131 (408) 434-0678						Circle 308		
27CX256	CMOS	32kx8	35, 45, 55	30	90/1	CERDIP	\$25.20 to \$42 (1,000s)	—
27CX010	CMOS	128kx8	45, 55, 70	30	90/1	CERDIP	\$35 to \$56 (1,000s)	—
Microchip Technology 2355 W Chandler Blvd, Chandler, AZ 85224 (602) 963-7373						Circle 309		
27C256	CMOS	32kx8	150	3.28	20/2	CDIP, LCC, PDIP, PLCC, SOIC	\$2.86 to \$3.40 (1,000s)	factory programming, industrial and military versions available, tape and reel packaging available
27HC256	CMOS	32kx8	45	3.28	55/35	CDIP, LCC, PDIP, PLCC, SOIC	\$5.10 to \$5.75 (1,000s)	factory programming, industrial and military versions available
27C512	CMOS	64kx8	120	6.5	35/2	CDIP, LCC, PDIP, PLCC, SOIC	\$5.85 to \$7.15 (1,000s)	same as above
27HC1616	CMOS	16kx16	45	1.64	90/2	CDIP, LCC, PDIP, PLCC, SOIC	\$17 to \$20 (1,000s)	same as above

PRODUCT FOCUS/High-density EPROMs

Model	Process	Organization (bits)	Access time (ns)	Programming time (s)	Current operating/standby (mA)	Packages	Price (quantity)	Comments
Mitsubishi Electronics America 1050 E Arques Ave, Sunnyvale, CA 94086 (408) 730-5900								Circle 310
M5M27C256AK	CMOS	32k×8	85 to 250	130	30/0.1	CERDIP	\$4.50 (1,000s)	JEDEC-standard pinout, industrial -40° C to 85° C version available
M5M27C512AK	CMOS	64k×8	100 to 150	260	50/0.1	CERDIP	\$5.90 (1,000s)	JEDEC-standard pinout
M5M27C100K M5M27C100JK	CMOS	128k×8	120 to 250	52 byte, 13 page mode	50/0.1	CERDIP, CLCC	\$9.60 to \$11.25 (1,000s)	masked-ROM compatible
M5M27C101K	CMOS	128k×8	120 to 250	52 byte, 13 page mode	50/0.1	CERDIP	\$9.60 (1,000s)	JEDEC-standard pinout
M5M27C101JK	CMOS	128k×8	120 to 250	52 byte, 13 page mode	50/0.1	CLCC	\$11.25 (1,000s)	same as above
M5M27C102K M5M27C102JK	CMOS	64k×16	120 to 250	52 byte, 13 page mode	50/0.1	CERDIP, CLCC	\$9.60 to \$11.25 (1,000s)	same as above
M5M27C201K	CMOS	256k×8	100 to 150	105 byte, 26 page mode	30/0.1	CERDIP	\$24 (1,000s)	same as above
M5M27C201JK	CMOS	256k×8	100 to 150	105 byte, 26 page mode	30/0.1	CLCC	\$28 (1,000s)	same as above
M5M27C202K M5M27C202JK	CMOS	128k×16	100 to 150	105 byte, 26 page mode	30/0.1	CERDIP, CLCC	\$24 to \$28.80 (1,000s)	same as above
M5M27C401K	CMOS	512k×8	120 to 150	52	30/0.1	CERDIP	\$56.25 (1,000s)	same as above
M5M27C402K	CMOS	256k×16	120 to 150	52	30/0.1	CERDIP	\$56.25 (1,000s)	—
NEC Electronics 401 Ellis St, Mountain View, CA 94043 (415) 960-6000								Circle 311
μPD28C256	CMOS	32k×8	200	10	20/100 μA	PDIP	—	—
μPD27C1024A	CMOS	64k×16	120	0.1	15/100 μA	CERDIP	—	—
μPD27C4001	CMOS	512k×8	150	0.1	30/100 μA	CERDIP	—	—
μPD27C2001	CMOS	256k×8	150	0.1	30/100 μA	CERDIP	—	—
μPD27C1001A	CMOS	128k×8	120	0.1	25/100 μA	CERDIP	—	—
Seeq Technology 1849 Fortune Dr, San Jose, CA 95131 (408) 432-7400								Circle 312
86063	NMOS	32k×8	200, 250, 300	5 ms/byte	50/150 μA	CDIP, CLCC	\$15	SMD qualified supplier of UV-EPROM, DESC mil drawing
27C256	CMOS	32k×8	200, 250, 300, 450	5 ms/byte	50/150 μA	CDIP, CLCC	\$15	883C compliant temperature; commercial, industrial, military
SGS-Thomson Microelectronics 1000 E Bell Rd, Phoenix, AZ 85022-2699 (602) 867-6100								Circle 313
M27C256B	CMOS	32k×8	100 to 250	3	50/1	CDIP	\$2 (25,000s)	—
M87C257	CMOS	32k×8	100 to 200	3	50/1	CDIP	\$4.25 (25,000s)	latches on all addresses
M27C512	CMOS	64k×8	100 to 250	6	50/200 μA	CDIP	\$3 (25,000s)	—
M27C516	CMOS	32k×16	100 to 200	3	50/200 μA	CDIP	\$4.25 (25,000s)	—
M27C1000	CMOS	128k×8	120 to 250	12	50/1	CDIP	\$6.50 (25,000s)	—
M27C1001	CMOS	128k×8	120 to 250	12	50/1	CDIP	\$6.50 (25,000s)	—
M27C1024	CMOS	64k×16	120 to 250	6	50/1	CDIP	\$6.50 (25,000s)	—
M27C2001	CMOS	256k×8	120 to 250	24	50/100 μA	CDIP	\$13 (25,000s)	—
M27C4001	CMOS	512k×8	100 to 250	48	50/100 μA	CDIP	\$125 (25,000s)	—
M27C4002	CMOS	256k×16	100 to 250	24	50/100 μA	CDIP	\$125 (25,000s)	—
M27256	NMOS	32k×8	170 to 450	90	100/40	CDIP	\$2 (25,000s)	—
M27512	NMOS	64k×8	200 to 400	50	125/40	CDIP	\$3 (25,000s)	—

Model	Process	Organization (bits)	Access time (ns)	Programming time (s)	Current operating/standby (mA)	Packages	Price (quantity)	Comments
Texas Instruments PO Box 809066, Dallas, TX 75380 (800) 232-3200								Circle 314
TMS27C010	CMOS	128k×8	170, 200, 250, 300	0.5	—	CERDIP	—	—
TMS27C210	CMOS	64k×16	100, 120, 150, 170, 200, 250	0.5	—	CERDIP	—	—
TMS27C040	CMOS	512k×8	150	0.5	—	CERDIP	—	product in development
Toshiba America Electronic Components 9775 Toledo Way, Irvine, CA 92718 (714) 455-2000								Circle 315
TC571024D	CMOS	64k×16	150, 200	0.1 ms/byte	40/100 μA	CERDIP	\$12.80 (1,000s)	—
TC57256AD	CMOS	32k×8	120, 150, 200	0.1 ms/byte	30/100 μA	CERDIP	\$5.50 (1,000s)	—
TC571000/1D	CMOS	128k×8	150, 200	0.1 ms/byte	100 μA	CERDIP	\$8.45 (1,000s)	—
TC574000D	CMOS	512k×8	120, 150	0.05 ms/byte	60/100 μA	CERDIP	\$47.50 (1,000s)	industrial temperature range, ±10% V _{cc} tolerance
TC574000D1	CMOS	512k×8	150, 200	0.05 ms/byte	100 μA	CERDIP	\$47.50 (1,000s)	same as above
TC574200D	CMOS	512k×8, 256k×16	120, 150, 200	0.05 ms/byte	60/100 μA	CERDIP	\$57.50 (1,000s)	±10% V _{cc} tolerance
TC57H1025AD-55	CMOS	64k×16	55	100 μs/byte	60/10	CERDIP, JEDEC	\$15.05 (1,000s)	—
TC57512AD	CMOS	64k×8	150, 200	100 μs/byte	30/100 μA	CERDIP	\$7.40 (1,000s)	—
TC571000AD TC571001AD	CMOS	128k×8	85, 100	100 μs/byte	30/100 μA	CERDIP	\$8.45 (1,000s)	±10% V _{cc} tolerance
57H256D	CMOS	32k×8	70, 85	0.1 ms/byte	50/100 μA	CERDIP	\$5.55 (1,000s)	—



Advanced Micro Devices and International CMOS Technology have jointly developed a 1-Mbit EPROM with access speeds as fast as 45 ns. Users can program 128k×8 bits of nonvolatile data. Stored data can be erased by UV light from a window.

tions, the future of the EPROM isn't completely secure. Emerging rapidly onto the nonvolatile market, flash memories are poised to erode the EPROM's market share. Although EPROMs now hold the largest share of worldwide PROM applications,

some analysts predict that flash memories will capture up to one-quarter of all PROM applications in several years. Dramatic drops in the price of flash memories are contributing to the perceived threat to EPROMs.

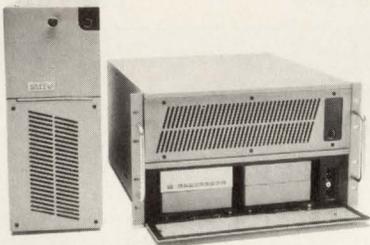
Flash memories provide some attractive benefits. Offering faster and simpler programmability than EPROMs, flash parts let users update and change code offsite in significantly less time and with lower labor costs than UV EPROMs require. Flash memories are ideal for applications such as process-control software and instrument calibration that requires periodic sector or bulk erase, which occasionally must be done in the field.

Still, there other issues beyond price and programming ease to be considered in the EPROM vs. flash struggle. More people buy EPROMs for flexibility than for reprogrammability, for instance. "Only 20 percent of the EPROMs we sell are actually reprogrammed," says Tony Barre, product marketing manager of programmable memory products at Intel (Folsom, CA).

Many customers buy EPROMs for the "comfort factor" that erasability offers, he says. Others use them because they simplify inventory. In-

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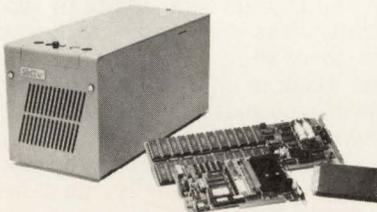
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PRODUCT FOCUS/High-density EPROMs

INTEGRATED CIRCUITS

stead of stocking a variety of coded ROMs, customers can stock EPROMs and program them as needed.

In a typical scenario, designers will use a windowed EPROM during development and switch to a lower cost one-time-programmable part when they move to full production. Given that these devices are often programmed once and soldered directly onto boards, an ever-growing number of EPROMs are being used in surface mount. This is especially desirable when space is a concern or when surface-mount technology is implemented across a production line.

Various packaging available

Manufacturers are also offering plastic one-time-programmable versions of their EPROMs as a low-cost alternative. Among those devices, a 2-Mbit EPROM from Intel is offered as a 32-pin plastic DIP or as a 32-lead

PLCC for surface mount. Called the 27C020, the unit is compatible with both TTL and CMOS environments. The traditional windowed ceramic DIP package is also available.

Most manufacturers agree that UV EPROMs won't be overshadowed by flash memories overnight. "An EPROM device will always be slightly less expensive if it's in a plastic package," says Steve Grossman, director of marketing for memory products at AMD. "EPROM technology is a little simpler and the circuitry to do the erasure in flash does take up some space. So there will be a market for both."

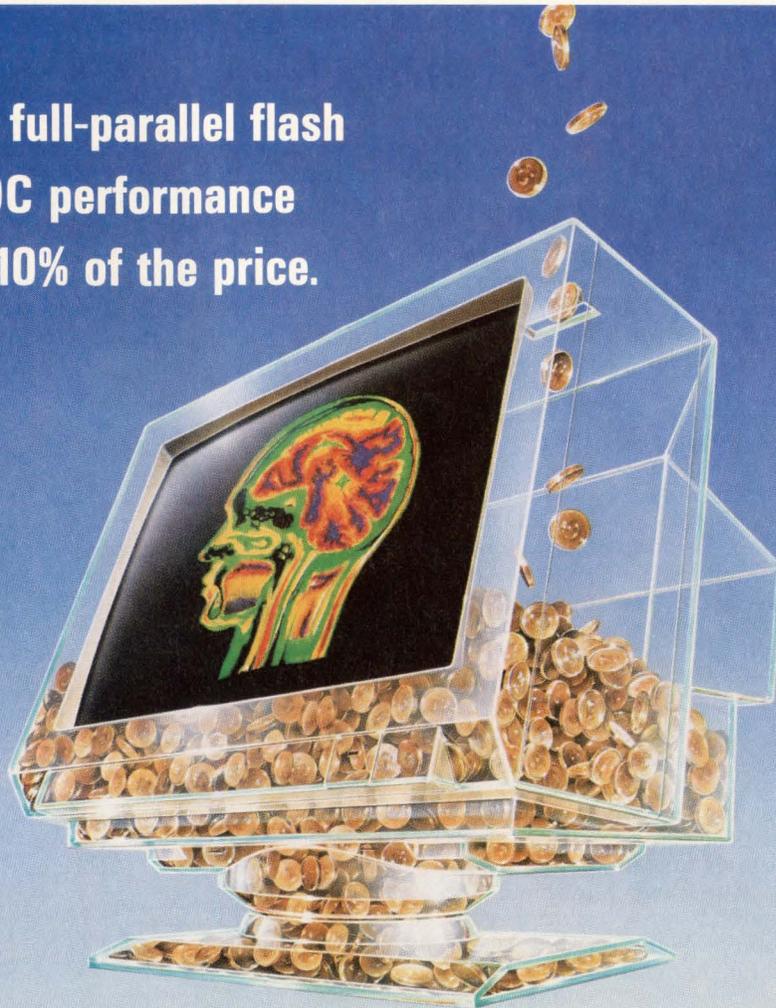
Grossman points out, however, that flash will probably be the preferred technology over the long term when users want any kind of reprogramming capability. As it stands now, though, it will likely take several years before flash actually crosses over the price of windowed ceramic EPROMs. ■

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TDA 8708*	30	365	Clamp/AGC CVBS Signal
TDA 8709*	30	380	Clamp/Adj. Gain R,G,B,Y,U,V, C Signals

* in DIL and SO versions.

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INTEGRATED CIRCUITS

AMD 29000 family adds on-chip FPU

When Apple Computer announced it would use Advanced Micro Devices' 29000 in a graphics controller, the original 29000 ran into an application to which it was not ideally suited. This prompted AMD to develop a microprocessor that would meet the needs of high-profile graphics applications. The 29050, as the latest addition to the AMD 29000 family, addresses those needs.

Two forces led to the development of the new CPU. First and most obvious, the 29000 has no on-chip floating-point support, while many graphics applications depend on floating-point computation. Second, with several years of application data to ponder, the AMD team saw numerous ways to speed up the integer execution of the 29000.

The most obvious addition to the chip was on-chip floating-point support. AMD has created a pipelined single-/double-precision FPU for the new part that maxes out at 80 MFlops. Essentially, the FPU contains three independent execution units: an adder, a multiplier and a divide/square-root unit. The three can function independently to produce the big MFlop numbers and may actually be used in this manner in some tight loops.

An important design feature of the FPU is that it uses the main 29000 register file—a huge, windowed bank of 192 32-bit registers. This substantially reduces the command latency, since operands don't have to be shuffled between register files for execution.

Boosting integer speed

After the FPU, the biggest change in the 29050 is increased overall performance. This comes primarily from increasing the clock frequency of the part to 40 MHz. But the higher clock rate and the opportunity to include some new ideas led to additional design changes.

"One change was enlarging the branch target cache," says Subodh Toprani, AMD director of marketing. This caches the instructions that are executed immediately after a branch is taken. The next time through a loop, the CPU doesn't have to wait for the branch address to work its way through the execu-

tion unit, fetch logic and the bus. It can start fetching instructions from the branch target cache. AMD claims that this arrangement, combined with the chip's elaborate streaming-mode instruction bus, delivers excellent performance at high clock rates without primary caches. But as the clock rate goes up, the number of instructions in the cache has to go up too, so AMD doubled the cache size.

AMD made additional changes in the 050 purely to accommodate the graphics-intensive codes that it sees as the big growth market for the chip. The on-chip MMU, for example, has been arranged so that large regions of physical addresses can be mapped with one translation look-aside buffer entry to make large frame or page buffers more practical.

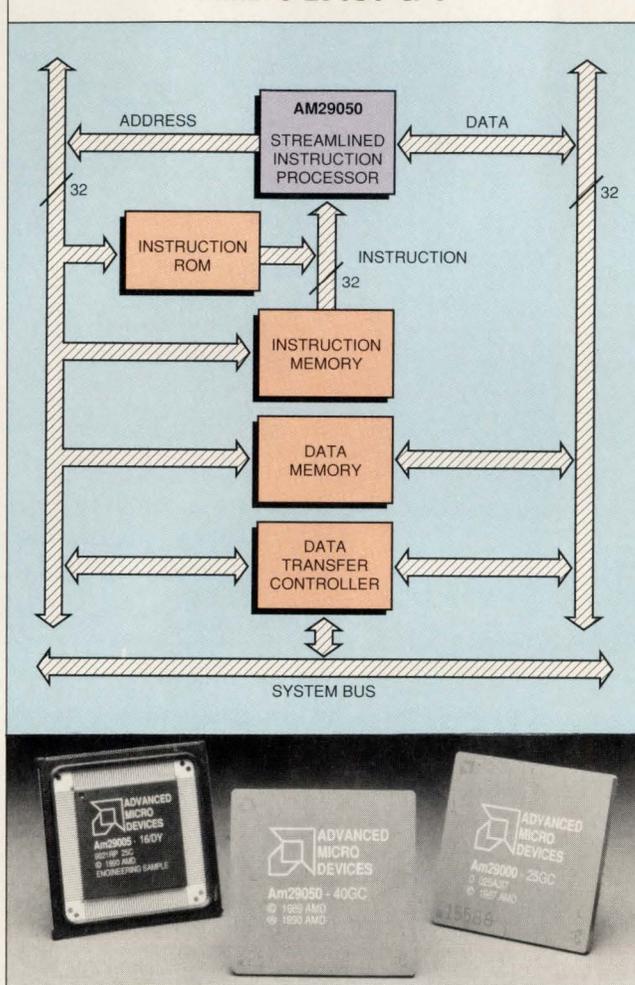
Through all these changes, the AMD part has remained pin-compatible with the original 29000. Of course, that doesn't imply that you can drop a 29050 and a new crystal into your old board and have a 40-MHz design. "You can plug an 050 into your existing system and it will run at your existing clock rate," Toprani says.

AMD admits, though, that the 40-MHz design isn't entirely trivial. "Probably the hardest part is getting burst-access writes to work," Relph says. "It's difficult to get most memory systems to write blocks of data at that speed."

As in fast 29000 designs, many 050 implementations will probably opt for combinations of page-mode

DRAM and data SRAM. Toprani maintains that this technique will still work with the faster 050. "We have customers now using DRAM and SRAM at 33 MHz," he says. "You need to use two- or four-way interleaving on the instruction DRAM, but you don't have to go to external caches to extract the per-

AMD'S 29050 CPU



formance from this part."

The 29050 and its compiler will sample in the fourth quarter of this year, and AMD expects production in the first quarter of 1991. A 20-MHz version will cost \$255, and the 40-MHz, \$410 (1,000s). —Ron Wilson

Advanced Micro Devices

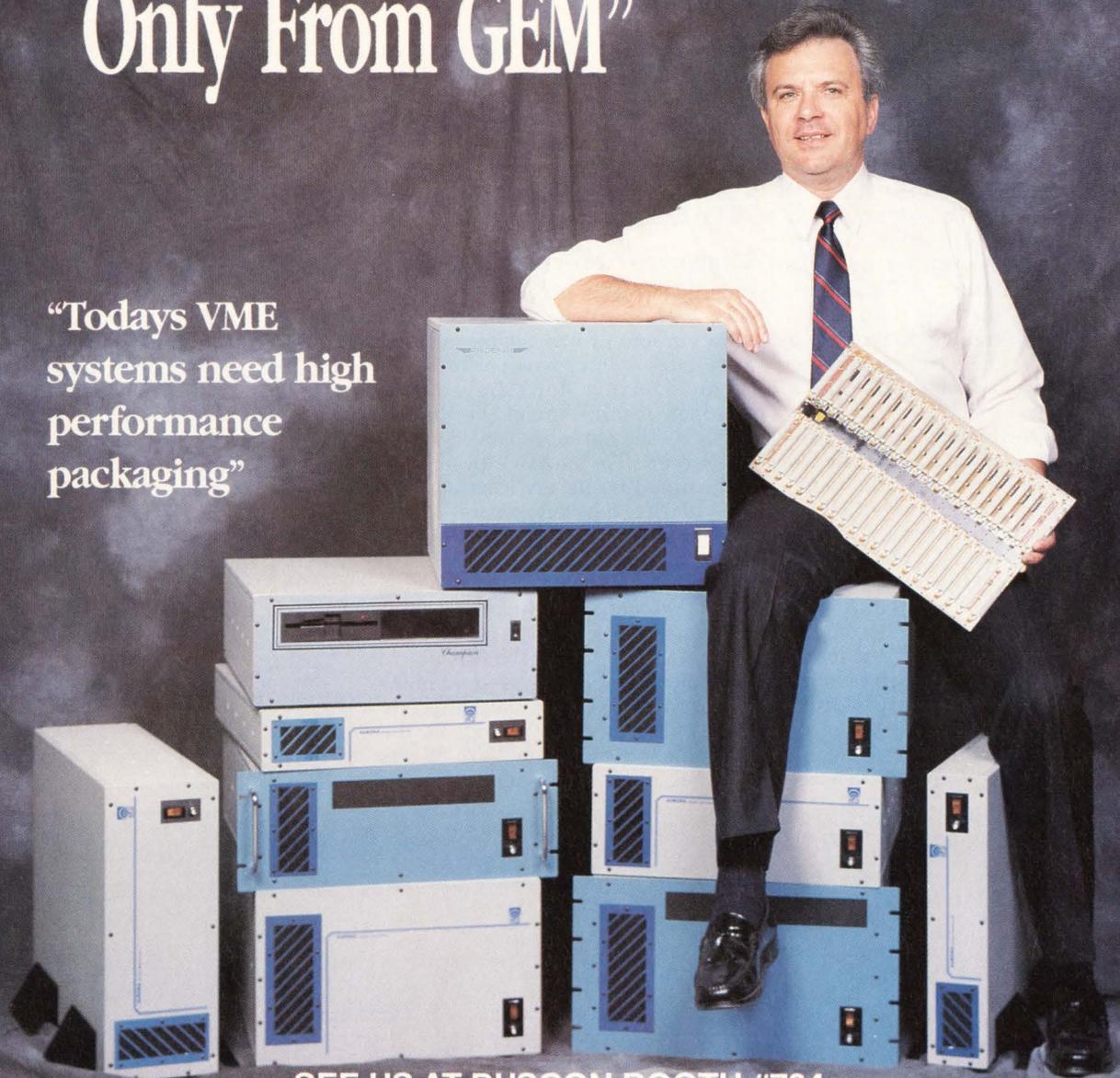
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INTEGRATED CIRCUITS

Video controller family features integration, speed, flexibility

A family of single-chip video controllers from the Inmos division of SGS-Thompson combines a high degree of integration, high resolution and the ability to interface with virtually any host processor, monitor or display memory architecture. The IMS G332 and IMS G364 are aimed at high-resolution and high-performance color workstation applications. Each contain a 256-position, 24-bit color lookup table with triple-video digital-to-analog converter, a programmable video timing generator, a phase-locked loop (PLL) and a microport.

The PLL technology allows programmable multiplication of the input clock frequency for all the video rate signals on the chip. This eliminates the need for high-frequency signals on the board and reduces emissions. Since the on-chip frequencies are programmable, the controllers can be configured to drive any monitor, whether it's a domestic TV set, interlaced or non-interlaced video or a high-resolution monitor—even multiple, synchronous video systems.

A gamma-correcting RAM is asso-

ciated with the color lookup table. Since color intensity doesn't increase linearly among red, green and blue, a gamma-correcting table adjusts the values to compensate the output voltages of the D-A converters to produce gamma-corrected 24-bit true color.

Improved cursor performance

In addition, a 64-pixel on-chip hardware cursor allows design of full-color cursors of any shape. A hardware cursor improves performance because pixels don't have to be swapped in and out of the display buffer as the cursor is moved across the screen. The cursor's position is determined by its x,y location relative to the top left corner of the screen. This is simpler than defining it in terms of synch and vertical blanking signals and is in keeping with the widely programmable video frequencies.

Both the G332 and the G364 have multiplexed pixel ports that allow use of interleaved frame buffers to supply pixel data fast enough for the high video rates. In the G332, 32 bits of pixel data are loaded alterna-

tively from one video RAM (VRAM) bank and then another. The G364 can shift in 64 bits at a time. In the G332, the pixel depth can be up to 16 bits/pixel for true color, or from 2 to 8 bits for pseudocolor using the lookup table. The G364 supports up to 24 bits/pixel of true color.

The microport is a bidirectional 24-bit interface with multiplexed address and data bus and several control signals. Multiplexing the lines makes the port usable with 32- and 64-bit processors. The port can also be used for VRAM shift register transfer to the pixel port via DMA. This operation is synchronized with the pixel port to allow seamless update of the VRAM's shift registers.

The G332 is available in 100-pin flat packs at video rates of 85, 100 and 110 MHz; the G364 is available in 132-pin pin grid arrays at the same speeds. Units with higher rates—between 110 and 135 MHz—will be available in 1991. Pricing for the 85-MHz G332 is \$95, and for the 85-MHz G364, \$125 (1,000s).

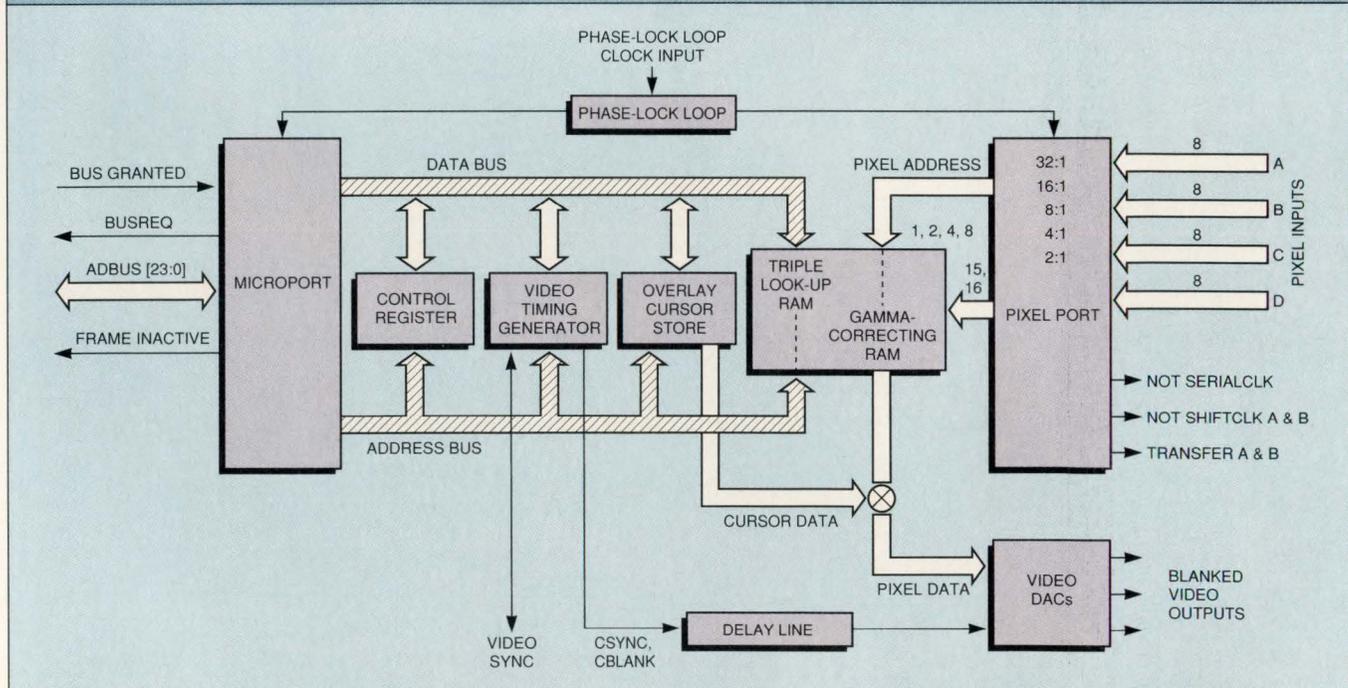
—Tom Williams

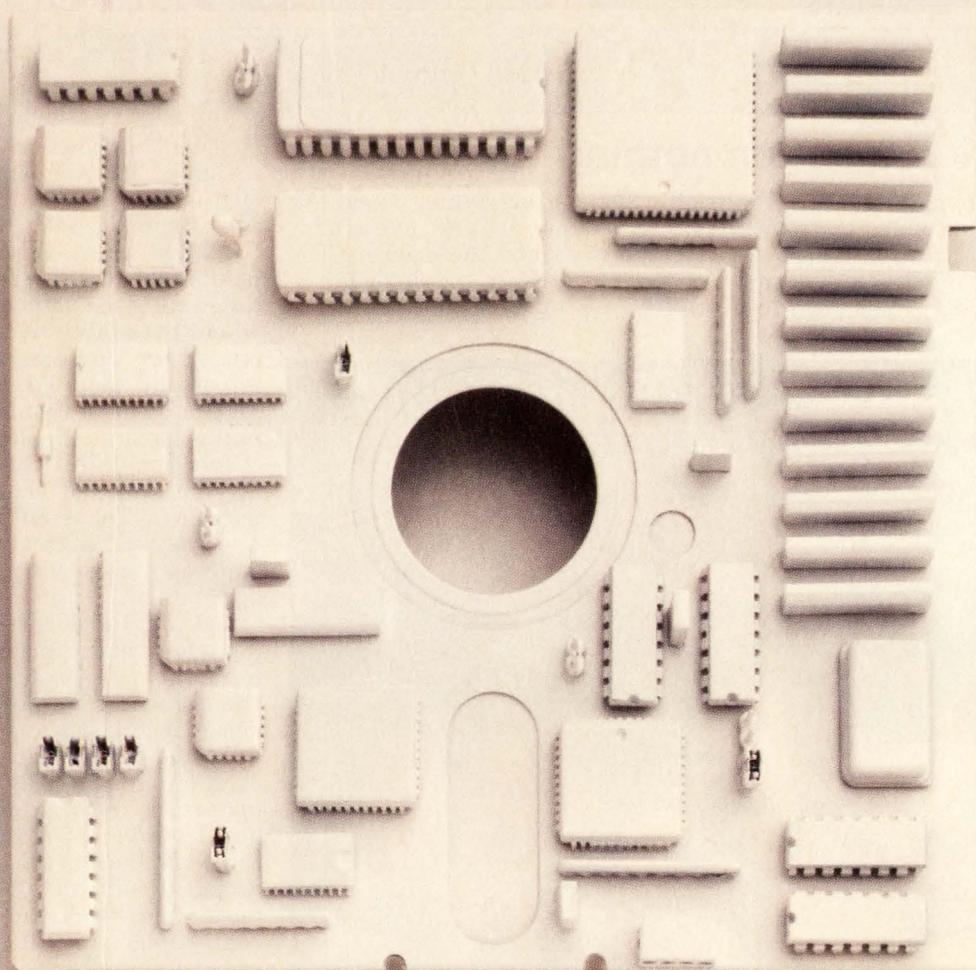
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INTEGRATED CIRCUITS

8051 tries to run on nothing

Philips Components/Signetics has been on something of a mission with the 8051 architecture. As Intel's interest in the 8-bit MCU family seems to be waning, Philips has been try-

ing a little of everything—new I/O devices, speeds and even processes—to extend the market span of the parts. Now the vendor has taken a step that may directly

threaten the homeland of 4-bit MCUs.

Philips has implemented a version of the 8051 in its proprietary self-aligning CMOS process. Called SACMOS, the idea was brought to fruition in Europe for the consumer divisions of the giant multinational, where the ability to run forever on one or two tiny cells is much more important than speed. The SACMOS process eliminates many of the bulky isolation regions needed in conventional CMOS layouts, reducing die size and sharply reducing parasitics. The result is a conservative process that can run at very low supply voltages with almost no leakage current.

SACMOS makes the perfect medium for a high-efficiency 8051. The part can run—not just idle, but run—at voltages as low as 1.5 V. The design is fully static, so the part can be halted between clocks in a couple of different power-down states. In operating mode, the chip draws about 1 mA at 1.5 V. In what Philips calls idle mode, this consumption drops in half, to 0.5 mA. In this mode, the CPU is inactive, but interrupts, timers and the I²C serial port are operational.

Finally, the part has a power-down mode, in which consumption plunges to 1 mA again at 1.5 V. In this mode, the part is completely moribund but can be awakened by any of eight external interrupts. The awakened part doesn't need a reset—it can simply resume execution where it left off.

The 83CL410 is configured as a standard 8051, with 4 kbytes of ROM, 128 bytes of RAM, 32 I/O pins and two timers. Philips substitutes its increasingly popular I²C interface for the normal 8051's UART to round out the chip.

The part is now sampling, and production is scheduled for the fourth quarter. Pricing is \$5.50 in a 40-pin DIP and \$6.30 in a tiny but speedy very-small-outline package (10,000s). A version of the part that greedily demands 2.5 V instead of 1.5 V is in production now.

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March 21, 1990 cover story

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INTEGRATED CIRCUITS

Motorola spotlights bandwidth in 68340 MCU entry

Motorola seems to have hit a winning combination with the 68300 family of application-directed CPUs. The parts integrate the company's CPU32 core—an upgraded 68010 execution unit with some 68020 extensions and 030-like bus timing—with various complex I/O modules, producing single-chip solutions that lack only external memory to become board-level systems.

The first introduction in the product family was the 68332, a chip directed at engine control. The part used a fast intermodule bus to attach sophisticated on-chip timing and serial communications processors to the CPU32 core. Although the die was large and the part expensive, the opportunity to get a highly integrated version of the revered 68000 CPU and the sophistication of the peripherals attracted

design wins far afield from Detroit's engine compartments.

Having secured a place for the 332, Motorola is now extending the product line downward into applications with simpler peripheral processing needs. The most recent step in this process is the 68340. The new chip includes simplified 2681-compatible serial I/O capabilities, timers and parallel I/O. But its primary claim to fame will be an enormously fast on-chip DMA controller.

Motorola claims that new applications will require both significant amounts of computing and very high data-moving capabilities. Hence the new two-channel DMA controller. "The module uses the 32-bit bus very efficiently," claims Motorola strategic program manager Tom Starnes. "We can get up to 32 Mbytes/s DMA bandwidth, with no

dead time between CPU and DMA bus cycles. The device operates in either fly-by or flow-through modes and can modify the word size of data as it flows through."

In addition, a 16-bit external bus helps keep down layout space requirements and the cost of off-chip peripherals. Fully static design lets the part be run at any speed from dc to 16.78 MHz—particularly useful for halting the CPU to conserve power.

The 68340 should be in production by the end of the year and will cost under \$50 (1,000s).

—Ron Wilson

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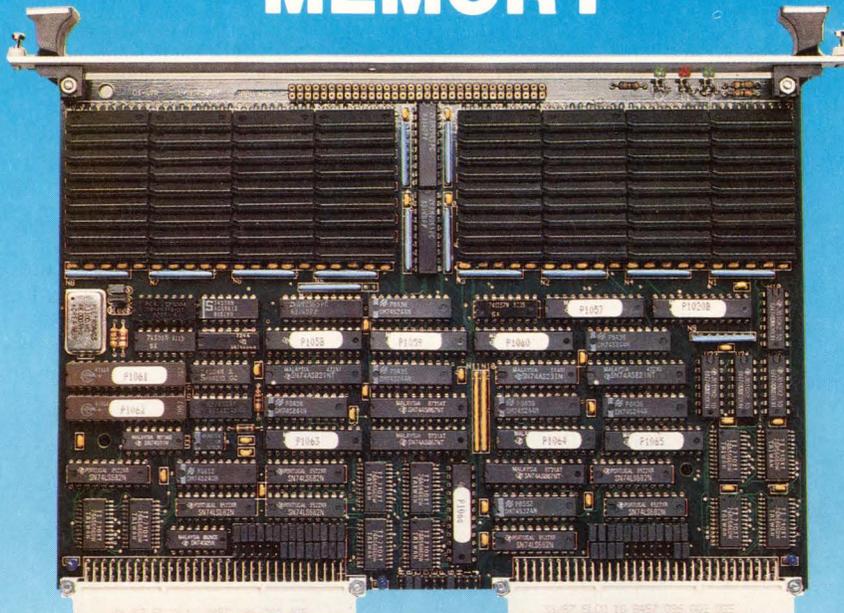
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CIRCLE NO. 70

SOFTWARE

Productivity tools and cross-compilers ease Ada development

TeleSoft has recently announced a number of additions to the TeleGen2 Ada development environment, including a pair of productivity tools and two new cross-compilers. In addition to cross-compilers, the TeleGen2 Ada environment already includes a library manager, source-level debuggers, an Ada profiler, a global optimizer, a set of language and object tools and an Ada run-time environment.

For the 68000 family of processors, TeleSoft has added TeleAda-Link, a downloading facility, and TeleAda-Kit, a facility for creating low-level operating system functions. Running over Ethernet, TeleAda-Link lets programmers download a 1-Mbyte program in less than one minute, compared with 20 minutes over a serial link. It also lets programmers use a target-code-capture feature to perform debugging on the target machine without ever leaving the host system. The link facility's capture feature can also be used with the profiler running on the target system to output to the host.

TeleAda-Kit is designed to relieve some of the tedium of writing low-level operating system functions by providing a set of reusable packages for low-level interfacing. These functions, including LAN, file and I/O packages, are intended to be easily adaptable to different hardware configurations. TeleAda-LAN conforms to TCP/IP protocols and provides interfaces for creating loosely coupled distributed Ada applications. TeleAda-File provides file-handling facilities, such as copying and renaming, and supports all pre-defined Ada I/O packages. TeleAda-IO offers a high-level interface for I/O drivers.

Two new cross-compilers

The two cross-compilers support the 80386 and the 88000 CPUs. The 80386 compiler is part of an 80386 version of the TeleGen2 Ada development environment that runs on an 80386-based machine under Unix V.3. So it's possible to develop and debug embedded 80386 code on a native platform. Another version of

the compiler is available for Digital Equipment Corp VAX machines running VMS 5.0 or above. Previously available only through Intel, the compiler is now offered directly by TeleSoft.

Both versions of the 80386 cross-compiler are closely integrated to work with Intel's ICE-386 in-circuit emulator. The ICE module can be driven directly from the TeleSoft source-level debugger to provide both Ada source-level and low-level

suite, which involves more than 3,600 tests.

The 88000 version of the compiler uses TeleSoft's optimizing compiler technology to include code inlining and other optimization techniques. The run-time package is multi-threaded and designed to provide predictable interrupt latencies that are important for embedded applications. The VAX/VMS-based 88000 cross-compiler joins a set of announced development products for the 88000 that run under the Unix operating system.

Pricing for the development tools and cross-compiler products varies



(emulation) debugging in the same utility. In addition, the Ada compiler can support host and target boards on Multibus II, and it supports Intel's RMK real-time kernel, which provides Multibus II message passing directly from Ada.

The second new TeleSoft cross-compiler is hosted on VAX/VMS systems and targets embedded systems using the 88000 RISC microprocessor. It comes with complete turnkey target environment support for the Motorola MVME181 board and can be adapted to other 88000 target systems. Such adaptation is aided by a comprehensive adaptation guide supplied with the product. The cross-compiler has been validated under Version 1.10 of the ACVC test

with system configuration. Pricing for the TeleAda-Link tool ranges from \$2,500 to \$20,200. Pricing for the TeleAda-Kit is \$8,000 to \$64,600. The VAX and 80386 versions of TeleGen2 Ada, which include the cross-compiler, are priced between \$13,000 and \$85,000. The 88000 cross-compilers hosted on VAX/VMS are priced between \$12,600 and \$102,000.

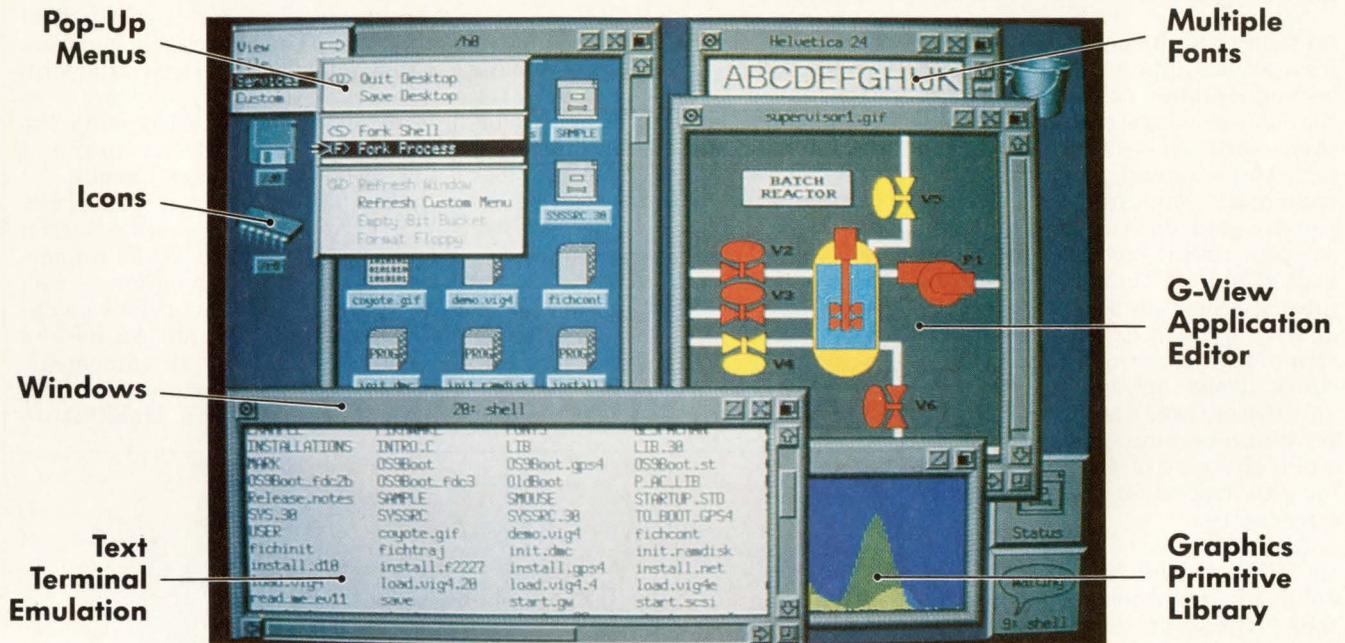
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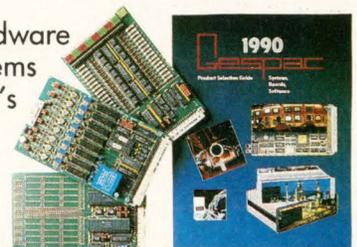
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DESIGN AND DEVELOPMENT TOOLS

Logic analyzer's state and timing features target complex PCB designs

As today's high-speed circuit board frequencies approach 20 MHz and beyond, designers must rely on more sophisticated logic analyzers to help them through system debug and test. Unfortunately, logic analyzers have had a reputation for being expensive and difficult to use. On a complex circuit board, for instance, it used to take hours to hook up all the necessary probes. And because analyzers were expensive, one instrument was normally shared by a whole design group. Traditionally, only two or three designers on a project would become analyzer experts, while the rest of the group would have to depend on them for debugging chores.

A new family of logic analyzers, the Philips PM 3580 series from John Fluke, promises relief from these traditional headaches by reducing state and timing measurements to one probe connection. In addition, the analyzers feature a single setup and fully integrated state and timing triggering for a common user interface. All measurements are time-tagged with up to 5 ns of resolution.

The PM 3580 family also boasts a dual-analyzer-per-pin architecture. This lets both state data (relating to software functions) and timing data (relating to hardware performance) be acquired simultaneously from the system on up to 96 channels, using just a single set of probes. Performance specifications provide up to 50-MHz state capability, up to 200-MHz timing functions and 2 kbits of memory per channel.

The single-probe approach eliminates not only the difficulty and unreliability of attaching multiple probes, but also the excessive loading factors that burden the target system, according to Fluke. In addition, fewer channels are needed for digital debug. A user working on an 80286-based system who wants to look at state information and bus timing, for example, would need 48 channels for state recording and perhaps 32 channels for timing analysis—a total of 80 channels. The 3580 architecture would require only 48 channels for the same

data.

The 3580's architecture reduces capacitance loading to 7 pF, even when both state and timing information are recorded. The dual capability also applies to clocks and clock qualifiers. Any channel can be defined as a clock or qualifier and still be recorded as a timing signal.

Timing features

Other features of the 3580 family include integrated triggering and complete time-tagging functions. On each of eight trigger levels, the user

depth is automatically adjusted to the speed of the recorded signals, always using the highest available resolution (5 ns for the PM 3585 analyzer). The completely separate glitch detector runs in parallel with the timing analyzer, allowing it to store glitches down to 3 ns, while the timing analyzer continues to run at full speed in transitional mode.

The 3580 analyzers feature a VGA-compatible gray-scale screen and a video output socket for connection to an external monitor as well as a parallel printer port for conventional hardcopy output. An RS-232 serial port is available for diagnostic testing and for future option support. The analyzer's architecture



can select from three timing words—in addition to edge, glitch and time out—or from up to eight state words. On each level, selective storage for the state record can be set (range, state word or a combination of state conditions).

All PM 3580 models incorporate the Philips transitional timing principle, which ensures that memory is used optimally in the acquisition of timing data. Instead of continually acquiring data regardless of whether there's any change in state, an acquisition is made only when a change takes place, together with a time reference to indicate when it was made.

In transitional timing, memory

also includes boundary-scan test capabilities (IEEE-1149.1) for reduced diagnostic and service time.

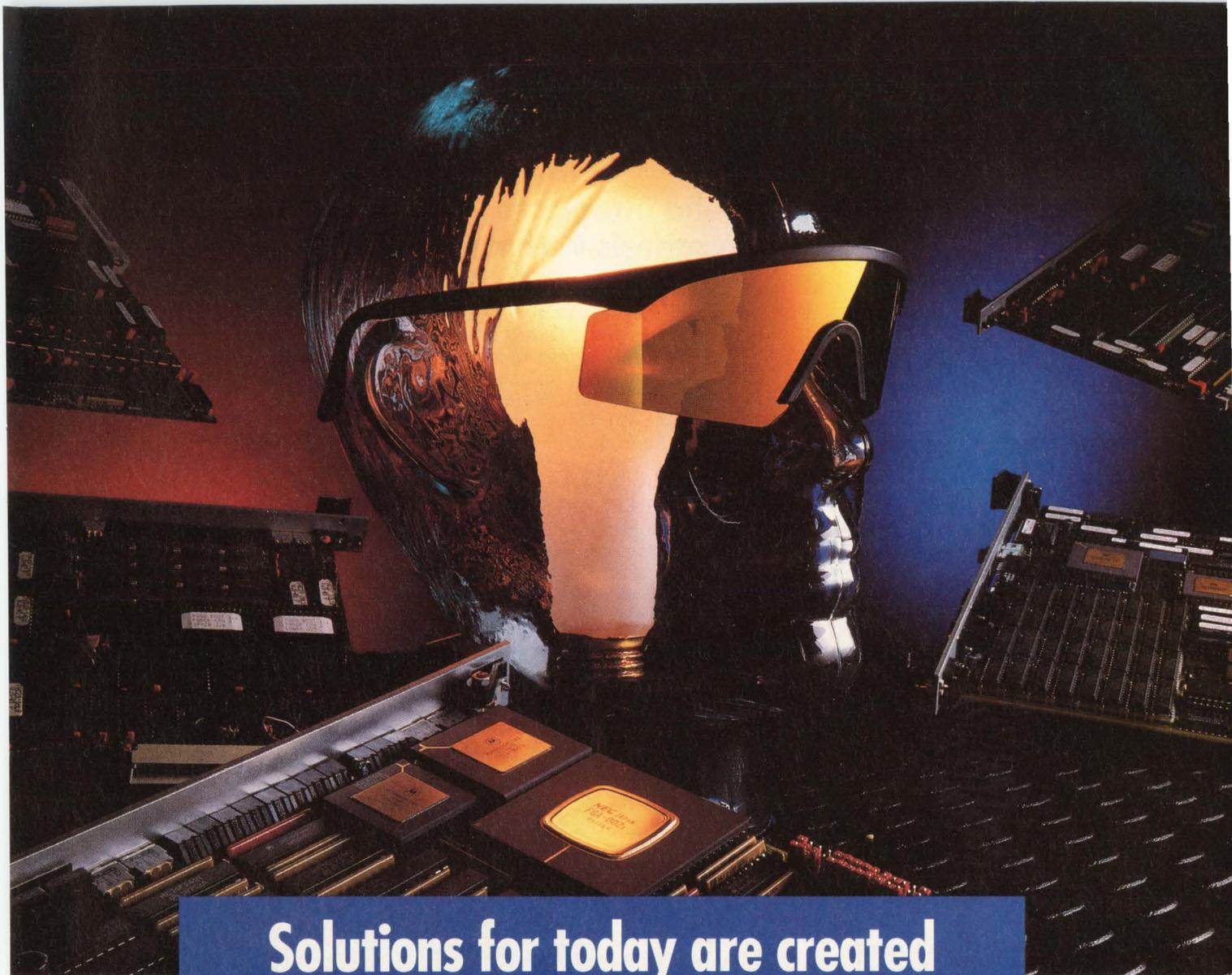
Prices for the 3580 series begin at \$4,250 for the 3580/30, with 32 channels of 50-MHz state recording, 32 channels of 100-MHz timing capability and 1 kbit of memory. At \$10,950, the 3585/90 offers 96 channels of 50-MHz state and 200-MHz timing recording with 2 kbits of memory.

—Mike Donlin

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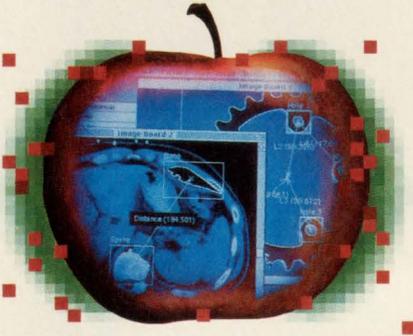
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NEW PRODUCT HIGHLIGHTS

DESIGN AND DEVELOPMENT TOOLS

Valid integrates PLD and FPGA synthesis within system design

Focusing on programmable logic device and field-programmable gate array synthesis in the context of system design, Valid Logic Systems has integrated two programmable device synthesis tools from Minc within its own Valid Workbench digital design environment.

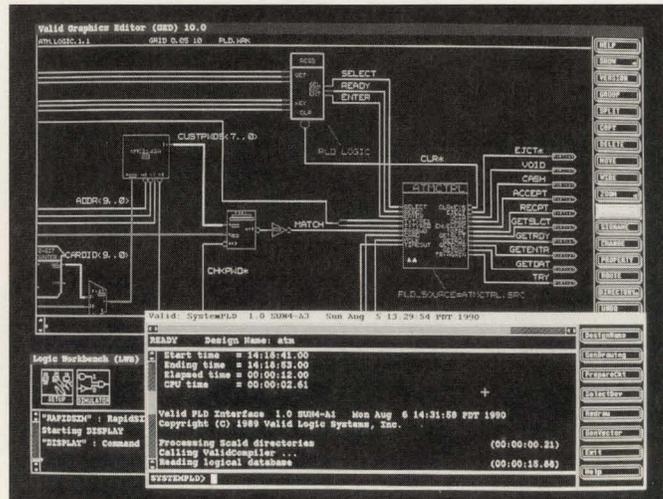
The SystemPLD and SystemPGA synthesis tools let system designers mix PLD and FPGA logic throughout the schematic hierarchy in the ValidGED design-entry system. Designers can synthesize functional models for system-level simulation with the RapidSIM digital simulator before device selection or partitioning. SystemPLD/SystemPGA users can re-target designs from one technology or vendor to another without design description changes, claims Valid. Users can also migrate from PLDs to FPGAs transparently. Moreover, an automatic schematic-redraw capability smoothes the integration with physical design, packaging and back annotation.

SystemPLD/SystemPGA users can mix microprocessors and PLD logic in design and simulation, and can then move on to layout, says Valid. "Being able to simulate the entire system early in the design process gives users tremendous time savings over the current methodology," says Don Mazur, product marketing manager for Valid. "Before SystemPLD and SystemPGA, users had to wait until the end of the design cycle to simulate the PLD or FPGA in the context of the overall system."

Users can describe designs in schematics, hardware description languages, waveforms, state machines, truth tables and Boolean equations. They can hierarchically

combine these methods in the same schematic without selecting a target device or technology. Users can also include constraints such as manufacturer, specific PLD type, speed and cost in schematics to drive device selection and partitioning. And they can select specific devices manually. Designs that require more than one device due to their size are automatically partitioned across multiple devices.

Library support for SystemPLD, which starts at \$13,500, extends to nearly all PLD vendors and architect-



tures. FPGAs supported by SystemPGA, which starts at \$19,500, include Xilinx's Logic Cell Array, Actel's Act devices, Altera's Max family and Advanced Micro Devices' MACH family. —Barbara Tuck

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Circle 354

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DESIGN AND DEVELOPMENT TOOLS

Software lets ASIC designers compare FPGAs up front

A new translation package from Exemplar Logic promises to be a cost-effective aid for ASIC designers. The FPGA Compiler lets designers analyze and optimize for different architectures before buying vendor-specific software.

Embedded with detailed knowledge about how to best implement a target device, the FPGA Compiler synthesis tools provide more than simple translation of logic descriptions. The software, for example, will synthesize different state encoding schemes depending on the target field-programmable gate array architecture.

Designers can control the optimization process using a single constraint file. This file directs the FPGA compiler to make the appropriate speed/area trade-offs based on maximum delay, required times, clock frequencies and maximum area. Constraint-driven optimization eases the task of prototyping since designs can be captured as a programmable logic device and later targeted to an FPGA.

Easier optimization

With the FPGA Compiler, users can optimize designs for devices from Xilinx, Actel and Plessey Semiconductors as well as estimate final area and timing. From that information, they can generate a list of candidate FPGA devices for comparison. Until now, designers have had to rely on descriptive literature to compare FPGA specs and architectures; or they've had to incur the cost of the various vendors' software tools, build their design in each of the technologies and then compare the FPGAs in working systems.

At the implementation phase, the new software generates the FPGA-specific netlist for input to the vendor-supplied place-and-route software. After executing place-and-route, designers can automatically back-annotate the actual delays to the FPGA Compiler for timing analysis.

Using a single report format, designers can evaluate actual area, timing and cost characteristics of competing design alternatives. De-

sign choices can then be made, for example, in favor of the cheapest part for reduced part costs, or for faster parts to meet the needs of speed-critical applications.

A VHDL input path to the FPGA Compiler is currently in beta test and is expected to be available at the same time as the software. "ASIC users will be able to capture a design in VHDL and take it onto an FPGA or gate array, or take a gate array netlist and map it onto an FPGA," said Ron Ranauro, director of marketing and sales at Exemplar. The FPGA Compiler will also accept EDIF (Electronic Design Interchange Format) 2.0 netlists. And a Palasm input path is scheduled to be available by mid-January, 1991.

The FPGA Compiler is written in portable C and runs under Unix and extended DOS operating environments. Due to ship in November, prices for the software range from \$5,000 to \$20,000, depending on input options and output technologies. The FPGA Compiler also accommodates PLD and gate array design styles.

—By Barbara Tuck

Exemplar Logic

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Circle 367

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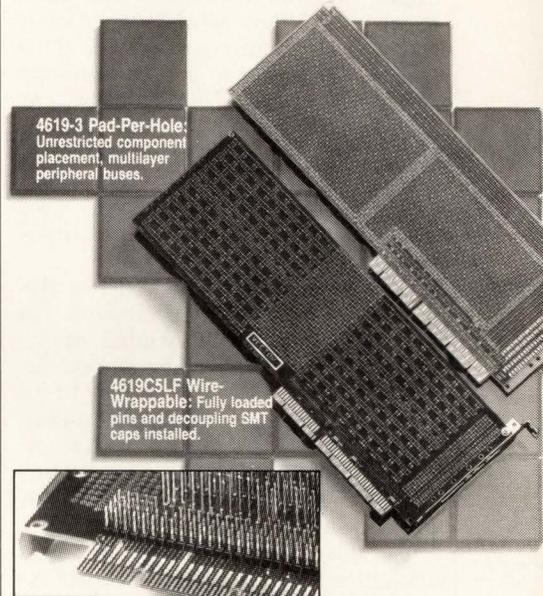
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CIRCLE NO. 74

COMPUTERS AND SUBSYSTEMS

960-based VME board offers local expansion bus

The CVME960 high-performance VME single-board computer (SBC) from Cyclone Microsystems is among the latest VMEbus boards to sport the 80960 second-generation RISC microprocessor. The CVME960 features a fast memory subsystem, a VMEbus for system communications, the Squall Module Expansion bus for local I/O devices, a real-time clock with battery backup and 1-Mbyte of EPROM. Two asynchronous serial communication ports are also provided.

At the heart of the board is the 960 microprocessor. Optimized for high-performance embedded applications, this chip executes two instructions per clock cycle. Key to its performance are its 1-kbyte on-chip instruction cache and 1-kbyte on-chip data RAM. The 960 also includes four DMA channels and an on-chip interrupt controller.

A high-bandwidth memory subsystem is linked to the microprocessor. Composed of 35-ns SRAM, the memory is pipelined and dual ported to both the processor and the VMEbus. Using burst-mode reads and writes, the memory enhances processor and bus operation, providing a sustained memory bandwidth of 66 Mbytes/s.

The VIC068 VMEbus interface controller is the avenue for systems communications on the CVME960. This device offers master/slave operation, support for block transfers, and a full set of system controller functions. The VIC068 also generates and handles interrupts on the VMEbus.

Standard, custom I/O modules

To take full advantage of the 960's capabilities as an embedded controller and an I/O server, Cyclone developed a set of Squall modules. These cards let systems integrators handle a variety of I/O requirements. If the standard modules don't fit a system's requirements, then the user, Cyclone or a third party can develop custom modules.

The interface for the Squall modules is an enhanced set of the 960's address, data and control signals. The microprocessor's four DMA

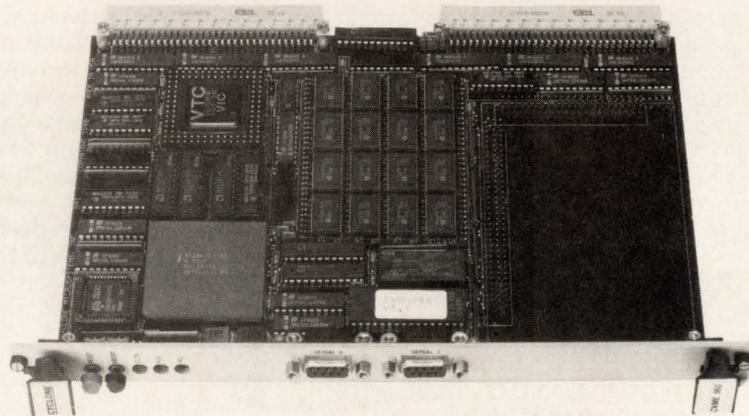
channels, also part of the interface, let the data be efficiently exchanged between the memory and I/O devices using the local processor/memory bus.

The Squall modules screw directly onto an area of the SBC that doesn't contain any components. Unlike traditional daughterboard configurations, this arrangement gives the module a low profile that doesn't block air flow to the board, causing heat-dissipation problems. Also, because no circuitry resides on the main board below the module,

the Squall module can request the local bus and transfer 32-bit words to memory at a sustained 66 Mbytes/s.

For customized configurations, the Squall module has 11 in.² of usable space in which to add components. With allowable component heights up to 0.438 in., the SBC and the Squall module together can occupy one card slot. This generous height tolerance allows DIPs, PLCCs and pin grid arrays to be socketed without restricting air flow.

Systems integrators who require a more cost-sensitive platform may prefer to use the CVME961 SBC. This alternate solution from Cy-



designs may be integrated into a single printed circuit board for high-volume production.

The Squall module can function as a simple slave interface to handle low-speed I/O requirements. In this mode, the processor can perform DMA transfers between the I/O device and main memory.

Alternatively, the module can function as a complex master interface, doing high-speed data transfers with direct access to the memory's full bandwidth. At 33 MHz, for example, the CVME960 can directly access 32-bit words into memory via the microprocessor's DMA channels at a sustained 33 Mbytes/s, according to Cyclone. A DMA controller on

clone is identical to the CVME960 except that instead of SRAM, it contains either 1, 2, 4 or 8 Mbytes of DRAM. Using burst read and write transfers, the CVME961's DRAM is also dual-ported.

The boards will be available later this month. Pricing depends on configuration. A 25-MHz CVME960 with 1 Mbyte of SRAM costs \$3,996. The 16-MHz CVME961 with 1 Mbyte of DRAM costs \$1,996.

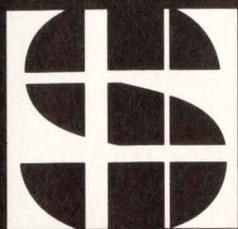
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COMPUTERS AND SUBSYSTEMS

■ CPU boards aid design of multiprocessing transputer networks

The GESPPU pair of transputer-based CPU boards from Gespac are targeted at image-processing, graphics and multi-axis motion-control applications. Designers can use

multiple combinations of these boards to form a multiprocessing transputer network.

The GESPPU-1 includes a 20-MHz T800 transputer, up to 4

Mbytes of RAM and a complete G-64/96 bus interface. A 1.5-Mbyte/s DMA controller speeds communications between the GESPPU-1 and the host CPU. The transputer's four 20-Mbit/s serial ports are accessible off-card, easing the design of multiprocessing transputer networks.

The GESPPU-2 sports two 20-MHz T800 transputers, each provided with up to 4 Mbytes of local memory. But it has no G-64/96 interface or DMA capability. So when it's used in G-64/96 systems, it must be used in conjunction with a GESPPU-1 board. Multiple GESPPU-2 boards are linked by a backplane that supports custom wiring.

Application programs for transputer networks are developed on a host G-64 system. These programs are then downloaded to GESPPU-1 host modules through the G-64 bus. Once on the board, the object code is routed to the appropriate transputer. Each transputer can run a separate program, computing in parallel. The transputer network uses the disk file system, user interface and I/O facilities of the host system.

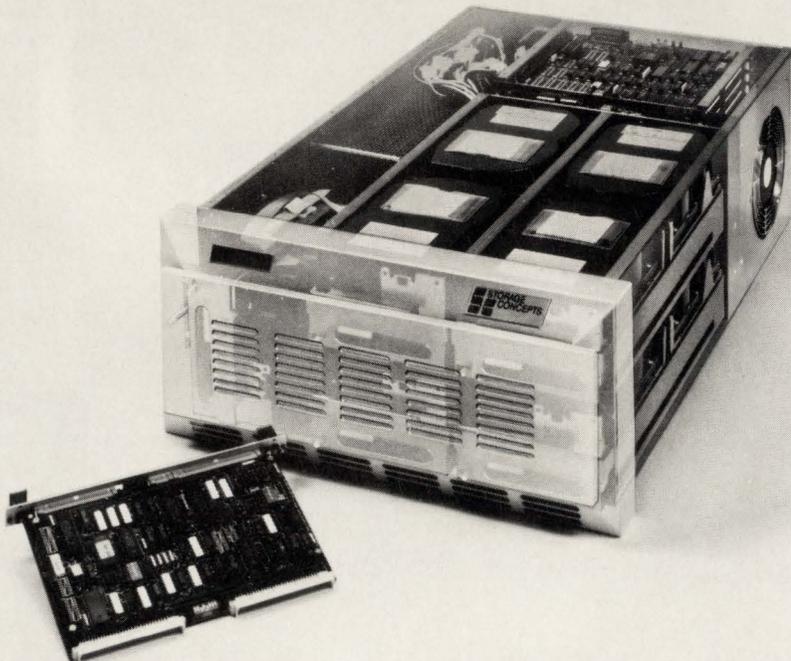
At the core of both boards is the 20-MHz T800 transputer, which integrates the functions of several devices into a single component. Included in the T800 are a 32-bit RISC CPU, a 64-bit floating-point unit, 4 kbytes of zero-wait-state RAM, a timer and four 20-Mbit/s serial ports. Providing process swapping for multitasking applications, a built-in microcoded scheduler is also included on the device.

Extensive software support is provided for the two boards, available for G-64 systems running either MS-DOS or OS-9. Among the development aids offered are the TDS2 OCCAM-2 development system and the Toolset cross-development tools from Inmos.

The GESPPU-1 is priced at \$2,250 and the GESPPU-2 at \$2,950. Both are available immediately.

—Jeffrey Child

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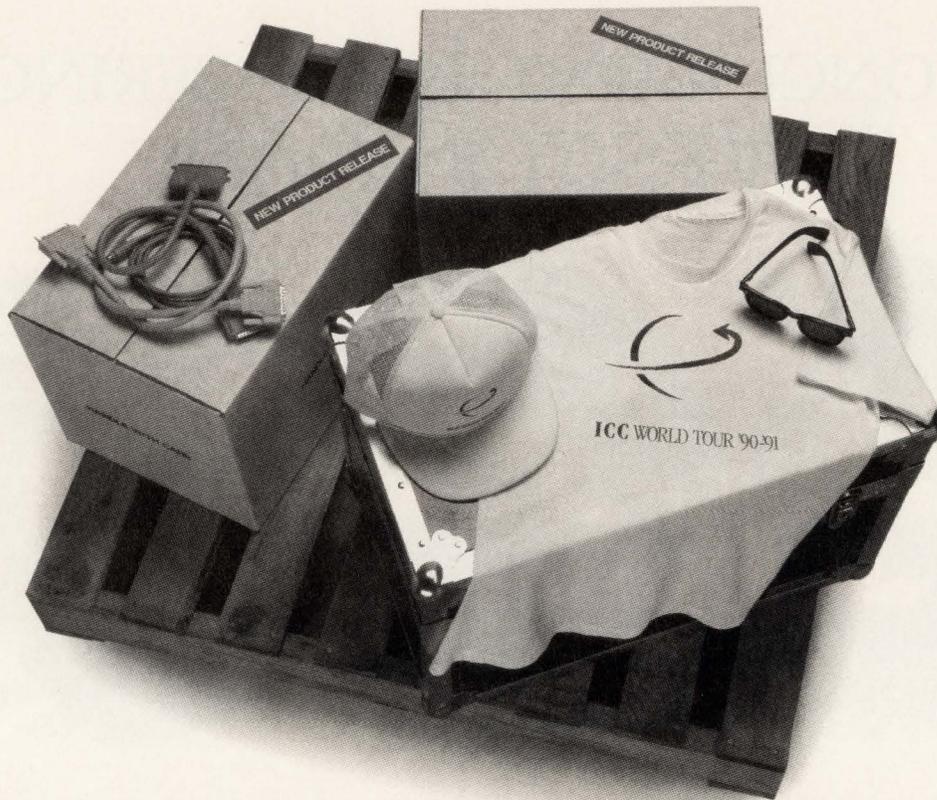
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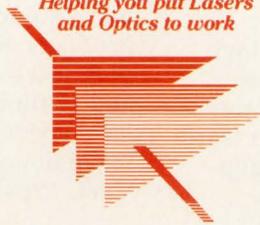
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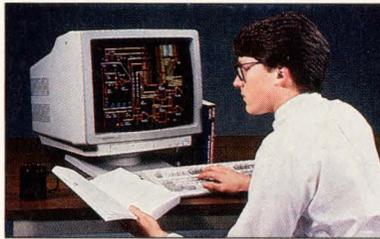
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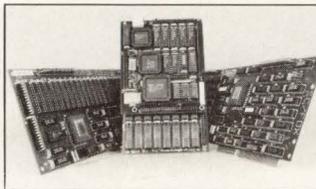
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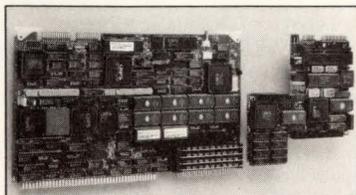
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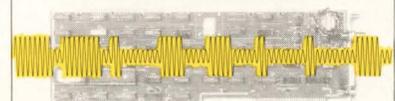
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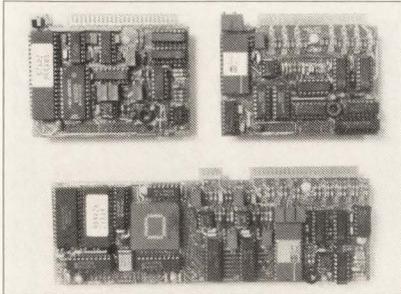
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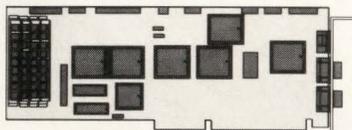
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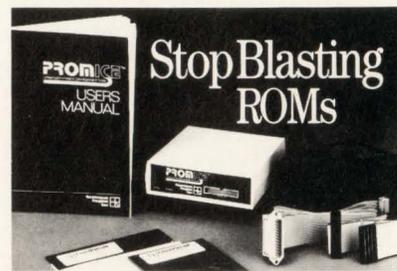
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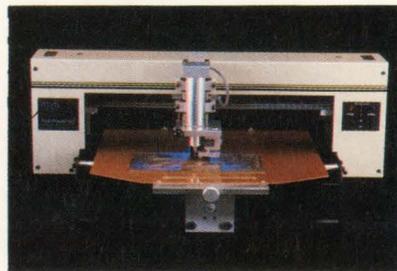
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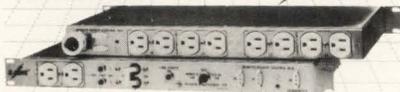
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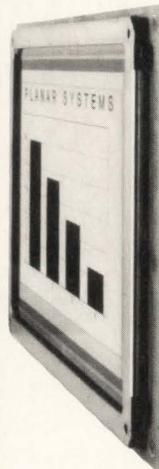
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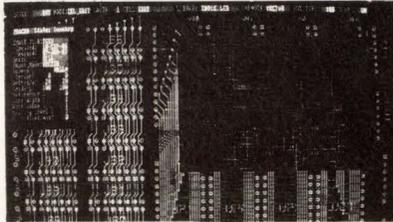


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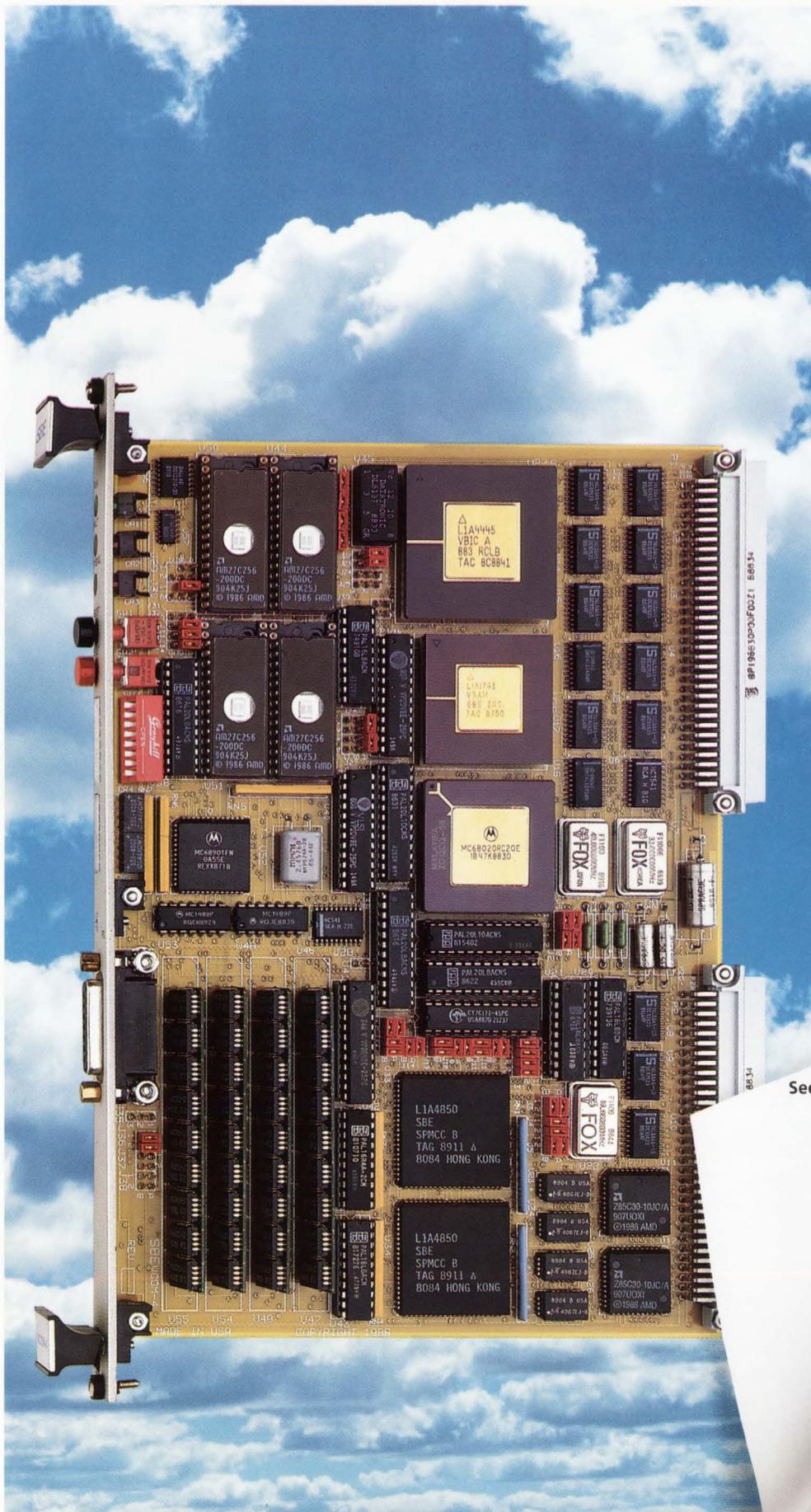
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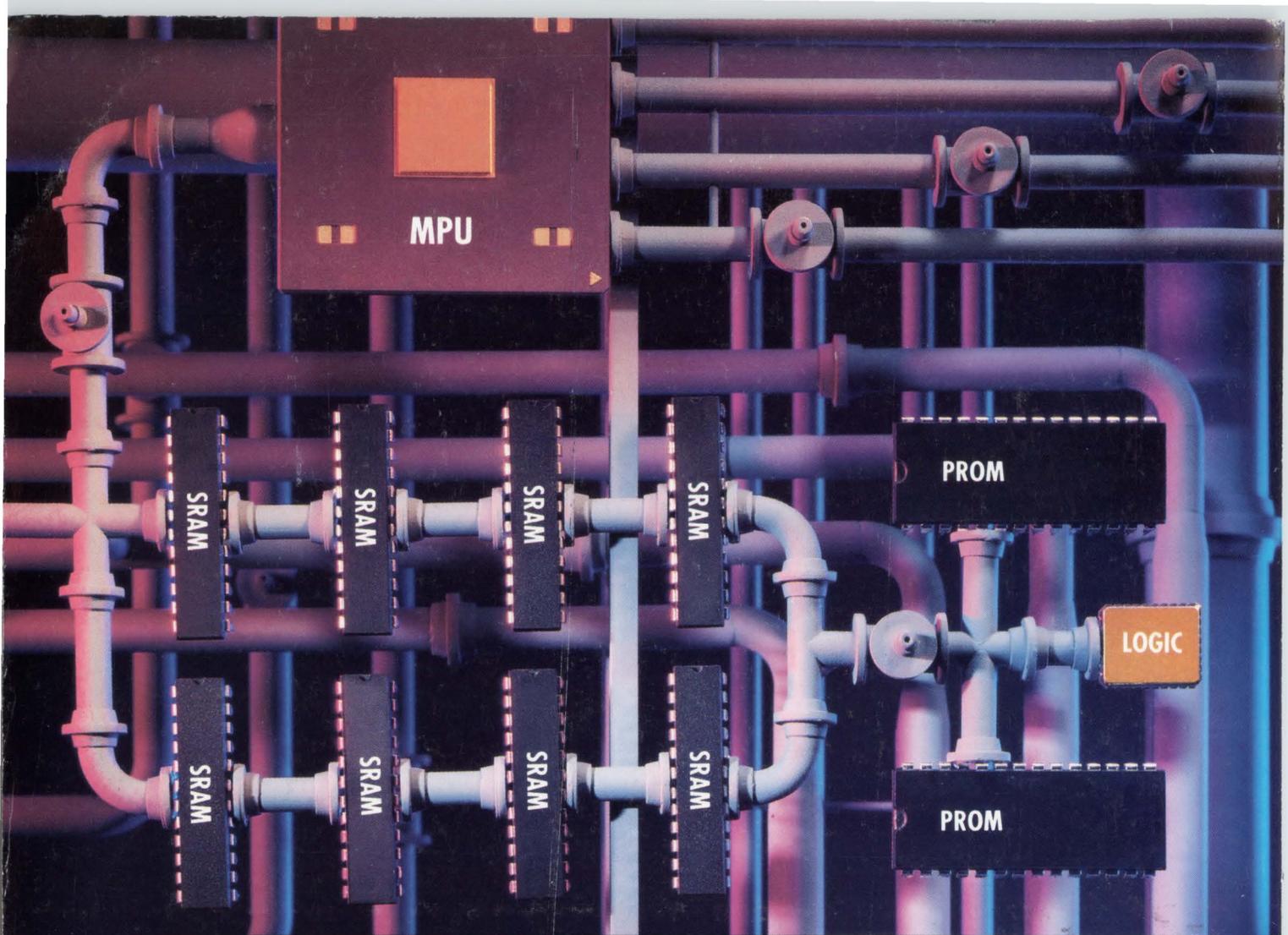
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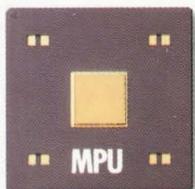
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