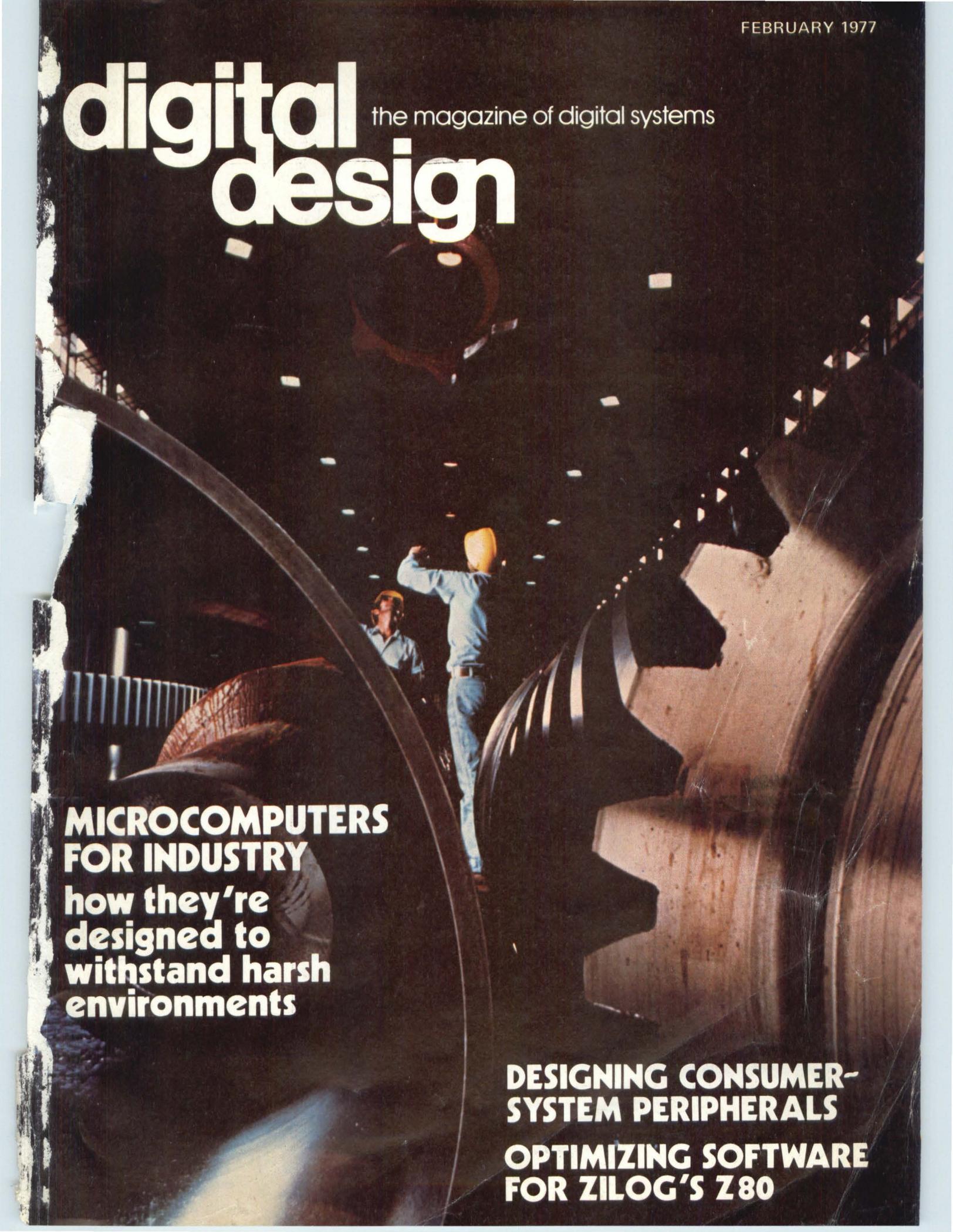


FEBRUARY 1977

# digital design

the magazine of digital systems



**MICROCOMPUTERS  
FOR INDUSTRY**  
how they're  
designed to  
withstand harsh  
environments

**DESIGNING CONSUMER-  
SYSTEM PERIPHERALS**

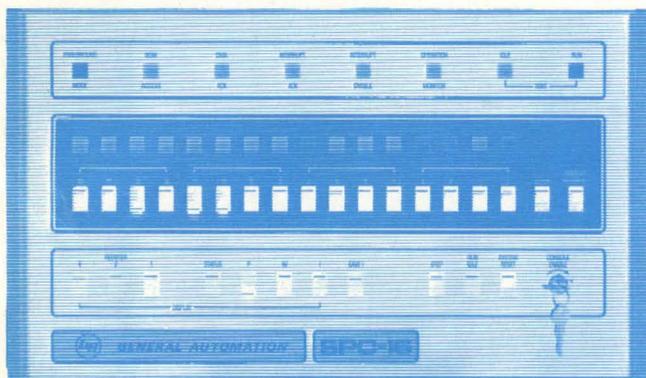
**OPTIMIZING SOFTWARE  
FOR ZILOG'S Z80**

# Standard Memories offers MORE for LESS...

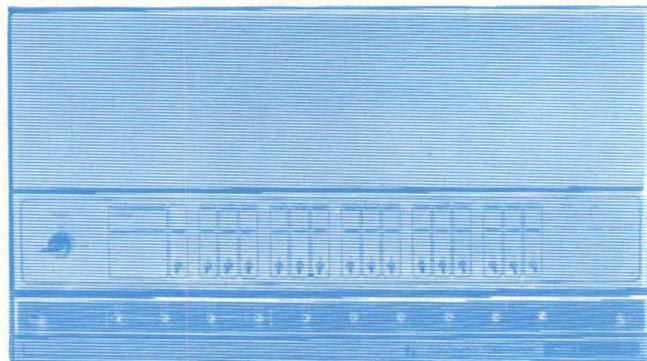
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**LESS:** Initial Cost, Less Spares Cost, Less Downtime

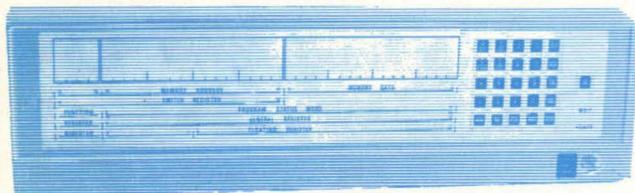
Increase the data storage capacity of your CPU by simply adding the applicable **PINCOMM**® or **BUSCOMM**® Memory...



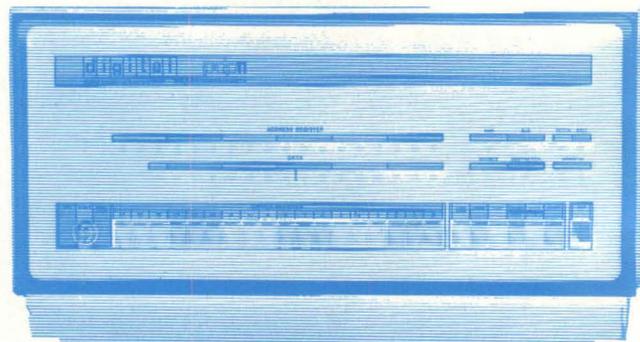
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# Scientific Micro Systems

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## Is An SMS ROM Simulator Necessary To Develop A Custom Bipolar Processor System?

**NO ... BUT** the money you spend on a ROM Simulator will more than pay for itself. Here's why:

Even the AMD 2900, the industry standard chip set for building bipolar controller and processor systems, requires support hardware and software during development. The SMS ROM Simulator and RAPID, a user defined assembler, provide this support.

The ROM Simulator is a *real time* (70 ns worst case) *in-circuit* debugging instrument which replaces the ROMS and PROMS in any bipolar system during development. It significantly increases productivity by allowing the microcode and macrocode to be debugged in a modular fashion. It allows the user to check a program segment thoroughly by inserting loops and breakpoints and then modifying or patching a segment of code until it is working properly. To change every other bit of a 64 bit instruction would take less than one minute and would be accomplished without touching the circuit. Each ROM Simulator can accept up to 16 Simulation modules—one Simulation Module exactly emulates one PROM—to allow either the microcode (up to 128 bits wide) or macrocode (up to 16K bytes deep) or both simultaneously to be simulated during debug. Even if you have never used a ROM Simulator, it can be installed and working effectively in your system in less than four hours.

The optimum system debug procedure is to —

1. Write and debug the microcode for each macroinstruction—first by single stepping through the program, then in real time.
2. Write and debug in real time critical macroprogram subroutines.
3. Write and debug remainder of application program.

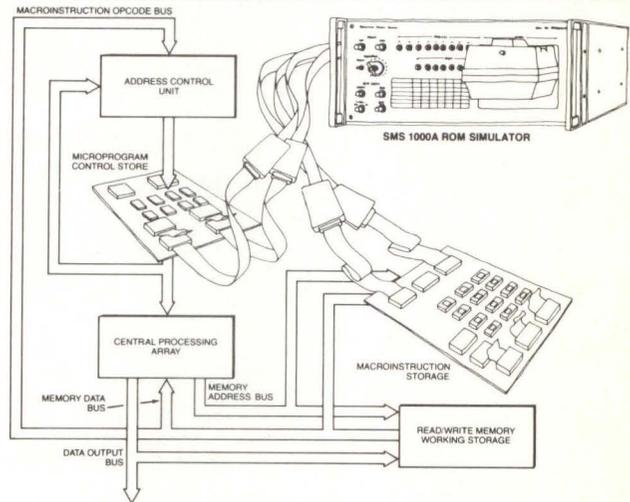
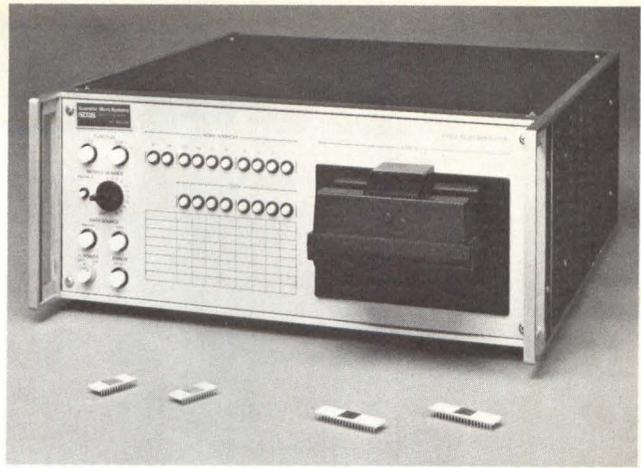
However, most designers find that changes in system performance requirements or unexpected difficulties require additional steps:

- 2a. Modify macroinstructions and debug new microcode to meet design criteria.
- 2b. Rewrite and debug critical macroprogram subroutines based on new macroinstructions.
- 2c. Repeat steps 2a and 2b as necessary.

The ROM Simulator not only speeds the initial development, but prevents these extra steps from turning a simple project into a development nightmare.

No development system is complete without an assembler. If you're already using one, chances are that its output is compatible with the ROM Simulator, or a minor modification will make it so. If you're just starting out, SMS offers Rapid, a meta assembler. It allows the user to define a set of instructions and instruction formats which are optimized for the processor being developed. The symbolic language thus created can be used to write and debug a program. Rapid permits symbolic addressing making it easy to add or delete program code as required.

**Over 80% of our customers have purchased more than one ROM Simulator. Find out why for yourself: Circle the reader service number or fill out the enclosed card.**



In the system shown, the ROM simulator simultaneously replaces the ROMS in both the microprogram and macroprogram store allowing the machine language code to be changed to find or patch a problem.

### European Representatives

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- The ROM Simulator seems to be what I need. Have a salesman call me for a free, half hour demonstration.
- I am building a bipolar system. Send me literature on the ROM Simulator including your ROM cross reference chart.
- I am a literature collector, but send me data sheets and cross reference anyway.

Processor Type \_\_\_\_\_

ROM Type(s) \_\_\_\_\_

Name \_\_\_\_\_ Title \_\_\_\_\_

Company \_\_\_\_\_ Phone \_\_\_\_\_

Street \_\_\_\_\_

City \_\_\_\_\_ State \_\_\_\_\_ Zip \_\_\_\_\_

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With the name Tandberg



# you know it's gotta be good.

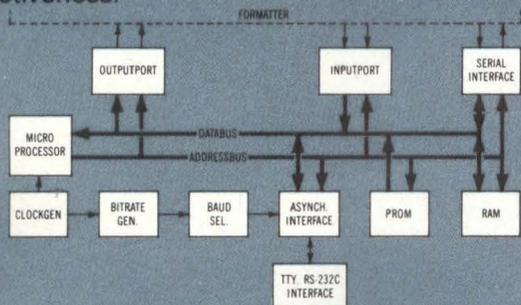
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There's a complete family of interfaces for the Tandberg TDC 3000. From the original design conceived by Tandberg of Norway, the \$150-million electronics firm that pioneered tape recorders internationally. The company that is to high quality electronic equipment what Rolls Royce is to automobiles. With a tradition of excellence that continues in a wide range of computer peripherals from Tandberg Data in the United States.

With total communications compatibility, the microprocessor-based RS-232 controller/interface from Tandberg Data is engineered according to EIA Standard RS-232-C, type D and E, and a "teletype-compatible current loop," recording in ANSI/ECMA/ISO-compatible format.

And from the substantial savings in line charges alone, the TDC 3000 with the RS-232 controller/interface will recoup its modest cost in a matter of months. It's hard to beat that kind of cost-effectiveness.



The Tandberg controller/interface is contained on one p.c. board which mounts inside the Recorder. Power is internal from the TDC 3000 built-in power supply. Two interface connectors are provided so that the Recorder can be connected both to a local I/O terminal (such as the Tandberg TDV 2100 Series CRT terminals) and a modem for remote operation.

Thirteen standard baud rates, 75-9600, are user selectable. Data buffers range from a minimum of 256 bytes up to 1024 bytes. The controller/interface responds to all ASCII command codes. Read and write speed is 30 ips and search speed 90 ips.

And for special communications requirements, the 6800 microprocessor allows the Tandberg controller/interface to be OEM-customer programmed.

Conceived in the rugged Norse heritage, the Tandberg TDC 3000 is no wilting lily when it comes to tough environments. Put it to work in subzero snow country or under a desert sun and don't worry about the bad vibes or emissions from nearby equip-

ment. The TDC 3000 is engineered to roll with environmental punches.

You might ask us about some of our more difficult applications. Modular construction of the TDC 3000 enables the user to configure a system to individual needs. Applications include minicomputer input/output, minicomputer peripheral storage, terminal peripheral storage, software distribution, data entry via keyboard, local data collection, data transmission, and text editing. And a few other things yet to be dreamed up.

Besides RS-232, Tandberg Data provides TDC 3000 interfaces for HP 21MX, PDP 11, Alpha LSI 2, and 8-bit parallel general purpose. All give up to 48K bits transfer rate.

Tandberg Data Inc.  
4901 Morena Blvd., Suite 407  
San Diego, Calif. 92117  
(714) 270-3990



Shown in test position.

Mr. Bruce B. Greenfield, Vice President, Tandberg Data Inc.  
4901 Morena Blvd., Suite 407, San Diego, California 92117

I'd like to know more about the RS-232 controller/interface for your TDC 3000. Please send me the RS-232 data sheet and have a Tandberg engineer give me a call to discuss my needs.

Name \_\_\_\_\_ Position \_\_\_\_\_

Company \_\_\_\_\_

Address \_\_\_\_\_

City \_\_\_\_\_ State \_\_\_\_\_ Zip \_\_\_\_\_

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Computer / terminal type \_\_\_\_\_

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**PRINTRONIX 300**  
It's your best buy!

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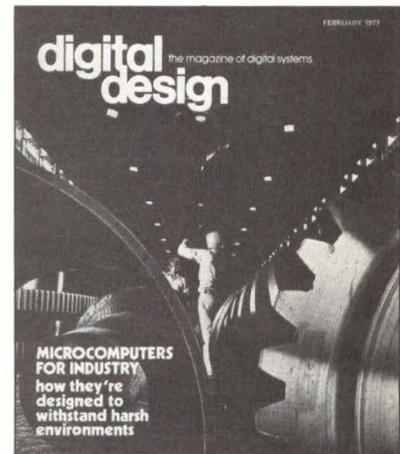
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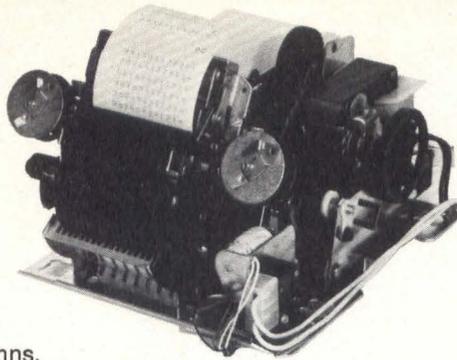


Workers assemble components for a mechanical press at E.W. Bliss' Salem, OH, plant — a typical industrial environment in which microprocessor based controllers must work. To learn about the techniques such controllers' designers use to cope with these environments, turn to page 36. Photo courtesy Gulf + Western Industries, Inc.; cover design by Mike Barisano.

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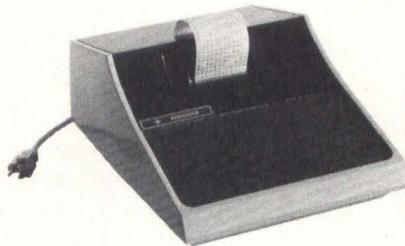


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# letters

## data-converter myopia: a second look

• Data-converter users are by no means as myopic as your September Viewpoint ("Data-Converter Design Myopia") would have them. Indeed, the piece's headline hits the nail on the head; the myopia is with the designer, not the user. Users, on the other hand, have definitely contracted "monolithic mania." They know that monolithic converters are not only up to date and useful, but also cost less, have higher reliability, are becoming available from more than one supplier, have faster conversion times, consume less power and in general are as accurate as their hybrid or modular counterparts.

While it is true that 14- and 16-bit converters are beyond current monolithic capability, 12-bit A/Ds are available now and 12-bit D/As will be later in 1977, despite the contrary opinions of hybrid and module manufacturers.

Since the introduction of the first 6- and 8-bit monolithic D/A converters in 1970, hybrid manufacturers have fired a steady barrage of propaganda in an apparent effort to transfer their myopia to the user. They typically fire both barrels at once, claiming that a monolithic component has "performance limitations" and "needs external components such as references, op amps, resistors, capacitors and clocks." Let's look at these charges in detail.

The primary converter performance parameter is conversion accuracy, which is limited by the resolution of the converter. A 6-bit converter only has a resolution of  $\pm 0.78\%$  F.S., 8 bits only  $\pm 0.19\%$ , and so on. By definition, an accuracy of  $\pm \frac{1}{2}$  LSB means the non-linearity of the converter is as good as its resolution. Monolithic converters are available from PMI, Analog Devices

and other firms with 6- to 10-bit resolution and  $\pm \frac{1}{4}$  LSB nonlinearity, twice as accurate as the resolution limit.

An internal reference is convenient in some but by no means all applications. Many users prefer to use one very good reference for several converters in the same system and thereby eliminate the reference drift from the conversion accuracy. Also, many applications use converters in a multiplying mode, where an external reference is mandatory. Finally, the world's first monolithic converter, introduced by our firm in 1970, does have an internal reference, as do many others introduced since then.

An output op amp is required only if a current output DAC has insufficient compliance to drive a load. Early converter designs are such that the output current cannot move off ground without degrading the accuracy. Modern DAC designs have eliminated this problem. Adding an op amp to a true current output DAC only slows it down, consumes more power, adds error, adds cost and reduces reliability.

Converter usage has progressed beyond the custom-design phase, where resistors, capacitors and clocks were put in the converter for a single-purpose application. No one would think of buying (or trying to sell) an op amp with built-in feedback resistors to pre-set the gain. Converters are no longer the mystery they once were. Non-myopic users now know how to trim up the converter to optimize the interface and clock rate for their particular application and thereby utilize the performance, reliability and cost advantages of standardized monolithic converters as they do any other IC component's.

Hybrid and modular converters certainly have their applications, but their manufacturers' myopia will not prevent monolithics from becoming the predominant converter technology.

EARL ROGERS  
President  
Precision Monolithics, Inc.  
Santa Clara, CA

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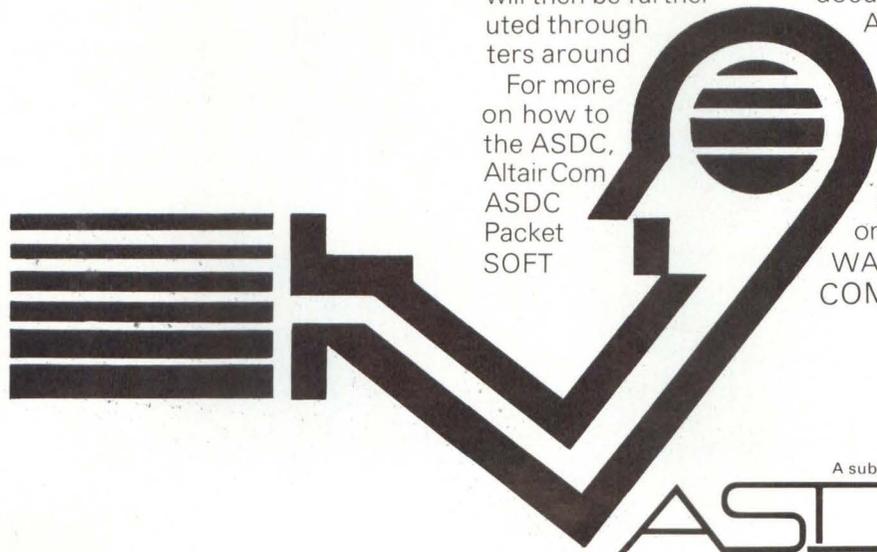
# Have you written Software for your Altair<sup>T.M.</sup> Computer?

The Altair 8800 computer was the first micro produced for the general public and remains number one in sales, with more than 8,000 mainframes in the field. The wide acceptance of the Altair computer and its rapid adaptation to many diversified applications has truly turned the dream of the affordable computer into a reality.

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- MM54C929, MM74C929 (1K x 1, 16-pin)
- MM54C930, MM74C930 (1K x 1, 18-pin)

(54 series numbers are military temperature, range, 74 series are commercial.)

- Other CMOS RAMs \_\_\_\_\_
- Other Memory Components \_\_\_\_\_

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COMPANY \_\_\_\_\_

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# technology trends

## Core system reads data nondestructively, cuts noise-and outage-induced bit losses

Aimed at applications that its developer claims require "idiot-proof nonvolatility," a recently introduced 4K x 8 core memory system can read the data it stores without having to rewrite that data afterwards. The developer claims this nondestructive readout capability suits the system to severe-environment and military-system uses, where noise spikes and power outages can sometimes produce dropped bits.

With a 1- $\mu$ s write cycle and a 350-ns access time, the system suits the timing requirements of the Intel 8080 microprocessor's bus, says Bruce Kaufman, president of Controlex Corp., Van Nuys, CA. But if necessary, he adds, it could operate faster and serve as an electrically alterable ROM in bit-slice microprocessor systems.

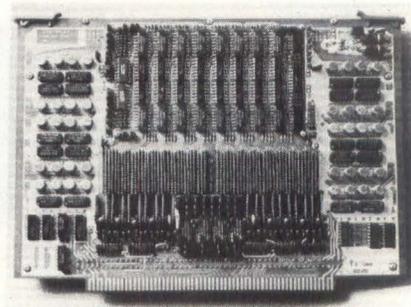
**No restore required.** Kaufman explains that conventional core memory systems store one bit per core; by convention a clockwise current and its resulting magnetic field represent a "1" and a counterclockwise current a "0". Reading a particular core requires that sense circuitry first reverse the core's state and then detect the flux change that the reversal produces. The circuitry must rewrite the original informa-

tion afterwards.

Under normal operating conditions, such rewrites occur without incident, and under normal power-down conditions, a core system remains nonvolatile and maintains the information represented in it. But if a spike or power outage occurs after readout but before the restore operation, lost bits can result.

The modified core system, however, can read the information it stores without altering that information. Incorporating conventional 18-mil, 200-mA ferrite cores, the CM203 represents a bit in two of those cores, unlike a conventional, one-bit-per-core system. Designers first investigated the scheme 10 or 15 years ago, says Kaufman, but no commercial system resulted from their work.

**Wiggling flux.** The system reads the information represented in one of the core pairs by subjecting the pair to a short-duration current pulse that switches only the core's elastic, or reversible, flux components; the pair's state remains unchanged after this action. "Wiggling" the flux this way produces a smaller output than does the conventional sensing method, says



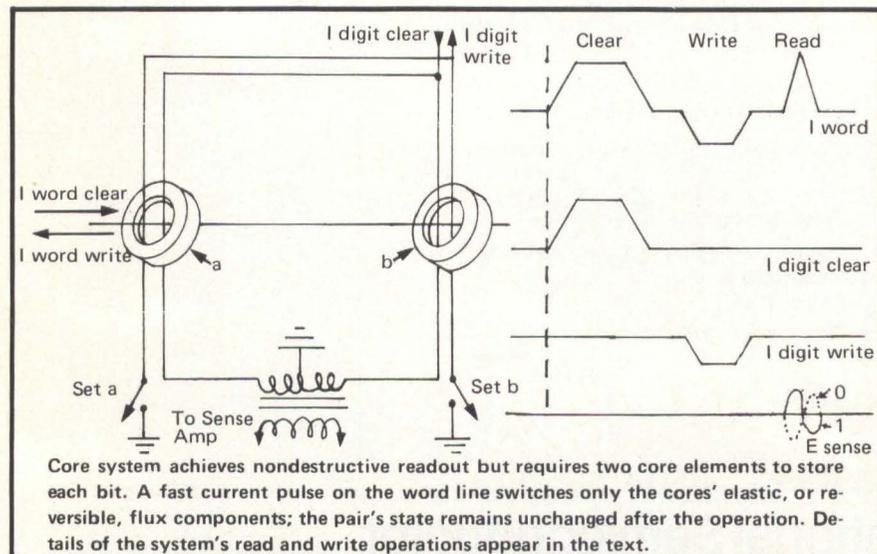
Accessing in 350 ns, the CM203 core system suits the Intel 8080's timing requirements. But it can also operate faster to serve as an electrically alterable ROM.

Kaufman.

Detailing a core pair's operation, he explains that the coincidence of two current pulses — half select word clear and half select digit clear — clears all cores on a selected word line. Then, depending on the data to be stored, the coincidence of two more pulses — half select digit write and half select word write — drives either the "a" or the "b" core of a pair into its "set" state. Unselected cores on the digit and word lines receive only a half select pulse, which lies below their threshold.

The system reads a pair by driving a fast pulse into a selected word line. Outputs occur for all bits on the selected word, and the selected sense amplifier channels then amplify, shape and present their inputs for strobing into a D latch.

The readout method's output is bipolar; a positive signal represents a "1", while a negative signal denotes a "0". By contrast, conventional core-system readouts have the same sign regardless of whether they represent a "1" or a "0"; if the signal for a "0" is positive, for example, the signal for a "1" is "more positive." These unipolar outputs can make discriminating between a "1" and a "0" difficult in conventional core systems, claims Kaufman. The bipolar outputs also allow the use of cheaper sense amplifiers

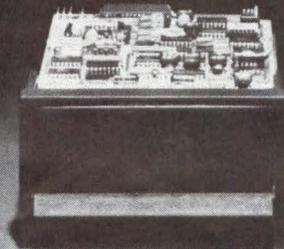


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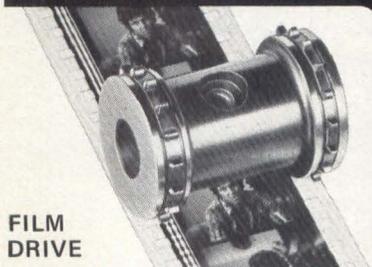
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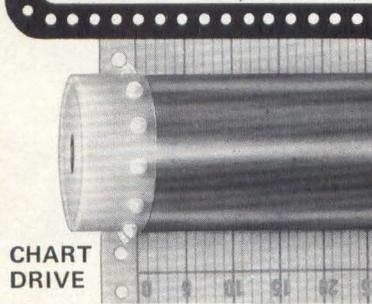
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than those in conventional systems.

No threat to conventional core. The company president hastens to add, however, that he doesn't foresee the core system's direct competition with either conventional core or semiconductor memory systems. Instead, it is aimed at applications in which electrical noise, high temperature, shock and vibration abound and in which nonvolatility is vital.

Two current installations of the system serve a programmable controller and an automatic welding machine; in both applications an operator on the factory floor must edit data stored in the system. Kaufman says he has also received inquiries about the use of the system in agricultural applications, and he notes that the firm plans soon to market a version of the system that substitutes CMOS circuitry for the current TTL configuration.

Field selectable write disable. The core system can operate either as a non-volatile RAM or as an electrically alterable ROM. A RAM/ROM mix is also possible; a user can write data in a portion of the memory system and by means of a write disable switch can protect the data from system malfunctions or unauthorized write commands.

Housed on an 8.5" x 12" PC board, the system incorporates all required timing and control drivers and a TTL interface. It costs \$500 in OEM quantities, and Kaufman notes that one obvious tradeoff between it and conventional core systems is its need for twice as many cores to store a given amount of information. But he claims that the continually dropping price of core elements makes using cores in such numbers economically feasible.

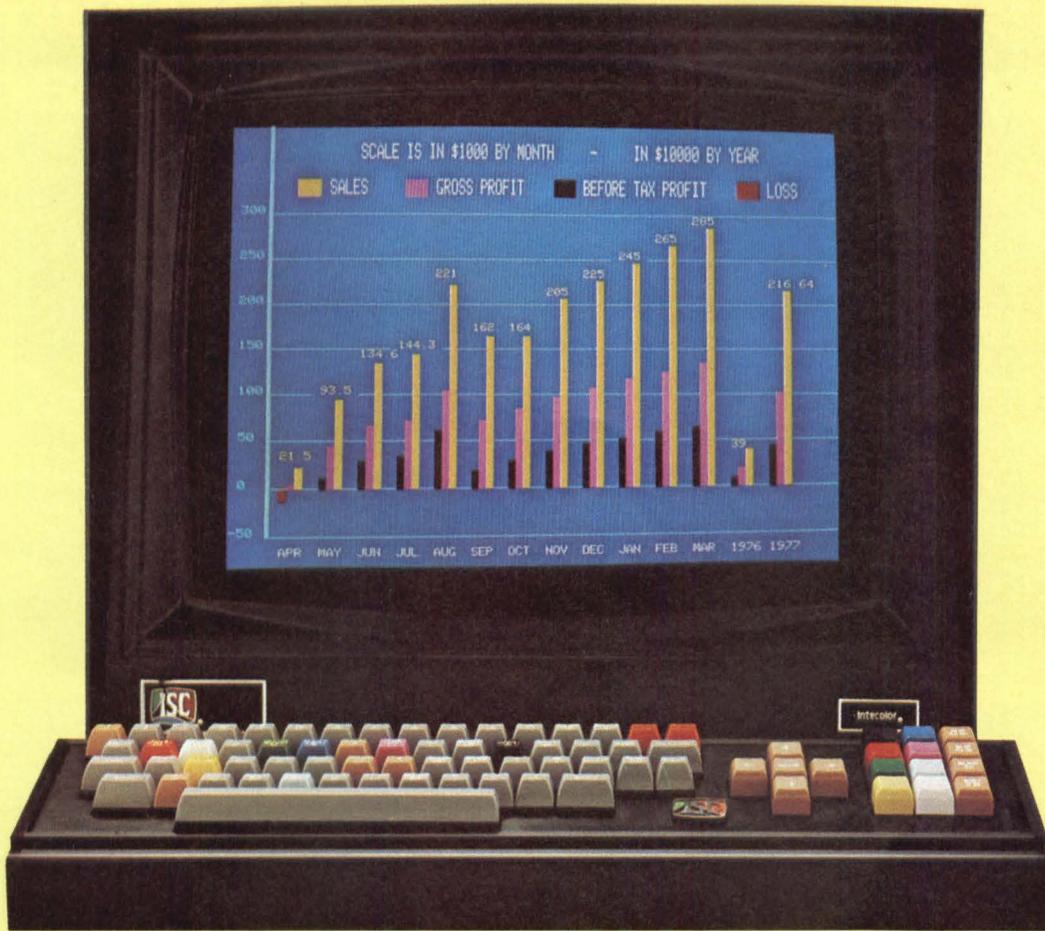
## Microcoded I/O eases CPU's tasks in 32-bit mini

Targeted at computational scientific applications and such measurement and control functions as power management and seismic monitoring, a recently developed medium-scale computer provides microprogrammability at both its CPU and I/O levels. With a 26.67-Mbytes/sec throughput rate, the 32-bit parallel SEL 32/75 can support up to 14 Mbytes of 600 or 900-ns core memory accessed through 20 ports.

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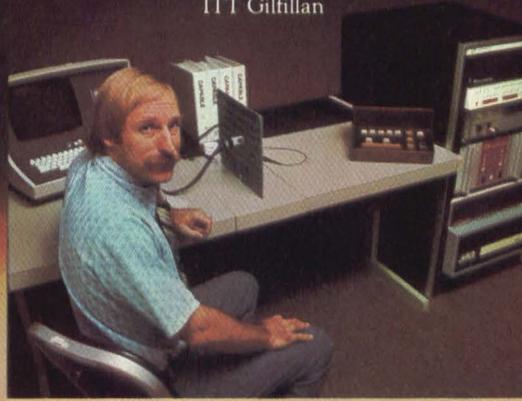
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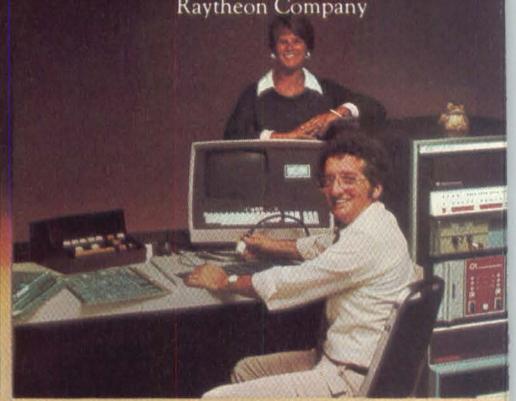
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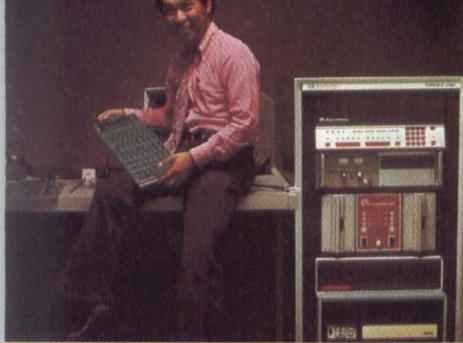
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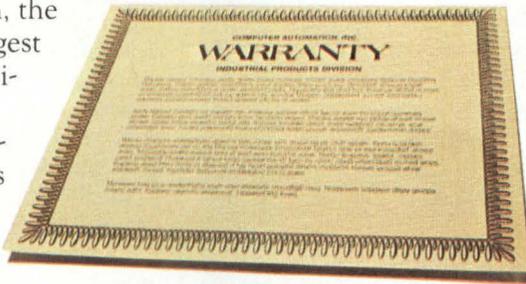
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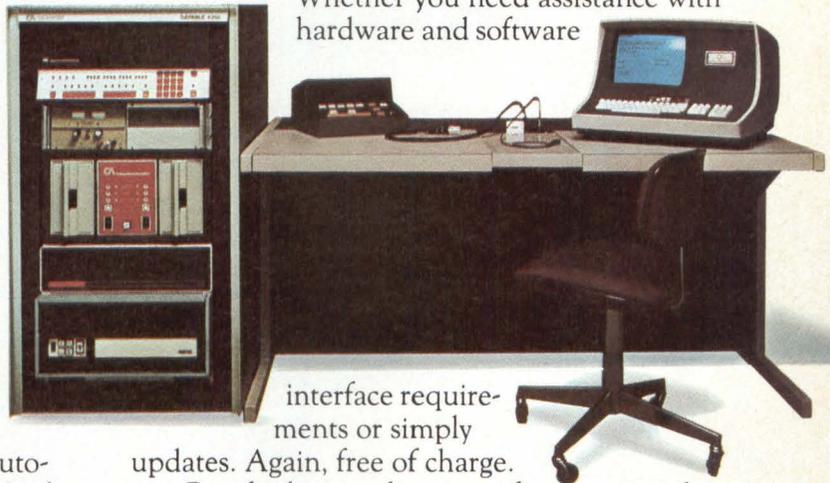
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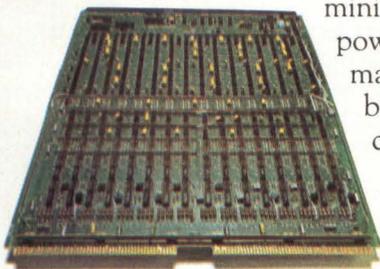
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technology trends

17 of which are privileged, according to N. A. Glatzer, director of product planning at Systems Engineering Laboratories, Ft. Lauderdale, FL. Its optional CPU writeable control store, designated Model 2344, provided 2K x 64 of RAM for storage of both user- and factory-generated microcodes. The computer can support up to two of these units.

**Microcoded I/O.** To ease its CPU's burden in certain applications, the computer can also support two types of intelligent input/output microprogrammable processors (IOMs); Model 9102 general-purpose IOM incorporates PROM control storage while Model 9103 microprogrammable device sub-controller kit utilizes writeable control store.

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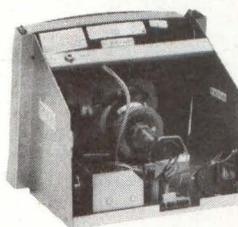
The Model 9103 plugs into the computer's SEL bus, which connects all functional elements of the computer system. It incorporates a microprogrammable device subcontroller (MDS) and a device interface board for applications that don't require writable control storage. The MDS consists of an interface to the computer's SEL bus (which connects all functional elements of the computer system), an interface to the device interface board, an interface to the writable control storage module, an interface to 2K x 32 of PROM and a microprogrammable processor.

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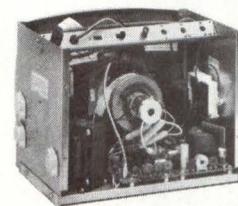
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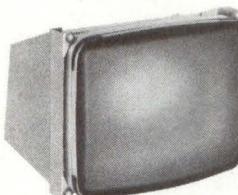
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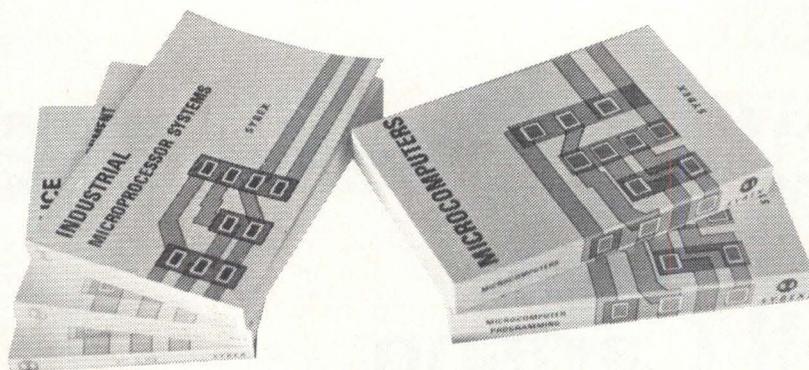
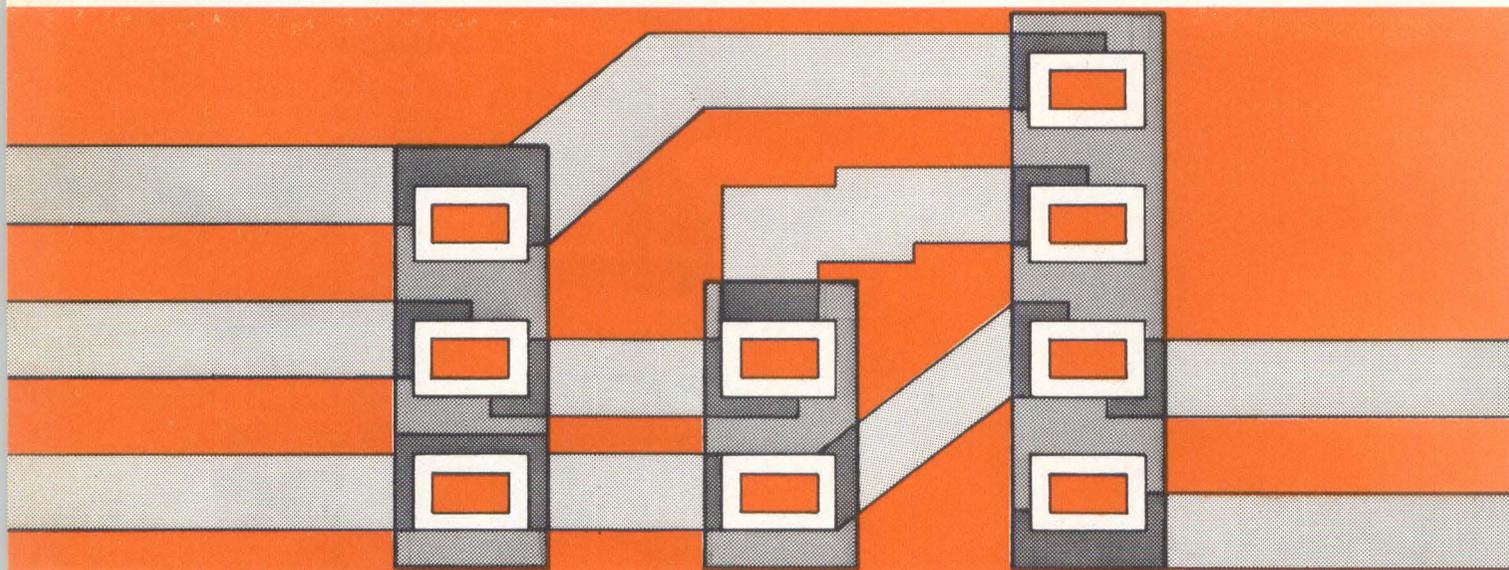
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## Special-purpose chips ease $\mu$ P's burden in RAM-based portable computer terminal

Rather than let its microprocessor minutely supervise all its I/O operations, a recently introduced portable computer terminal instead divides those operations among several special-purpose ICs, each operating under software control. One of the designers of the terminal's microprocessor system explains that this division of labor reflects the system's parallel-processing orientation, in which "I/O devices with intelligence can pick up and handle things like keyboard servicing without constant attention from the CPU."

Marketed by Wordsmith, Inc., Marina Del Rey, CA, the terminal stores input data in 4K RAMs, unlike many similar devices that use tape cassettes

as an input-storage medium. Its microprocessor system, developed by Rockwell International's Microelectronic Device Div., Anaheim, CA, incorporates

**Storing inputs in RAM simplifies error corrections; the terminal can retransmit a faulty data record as soon as its host computer detects an error.**

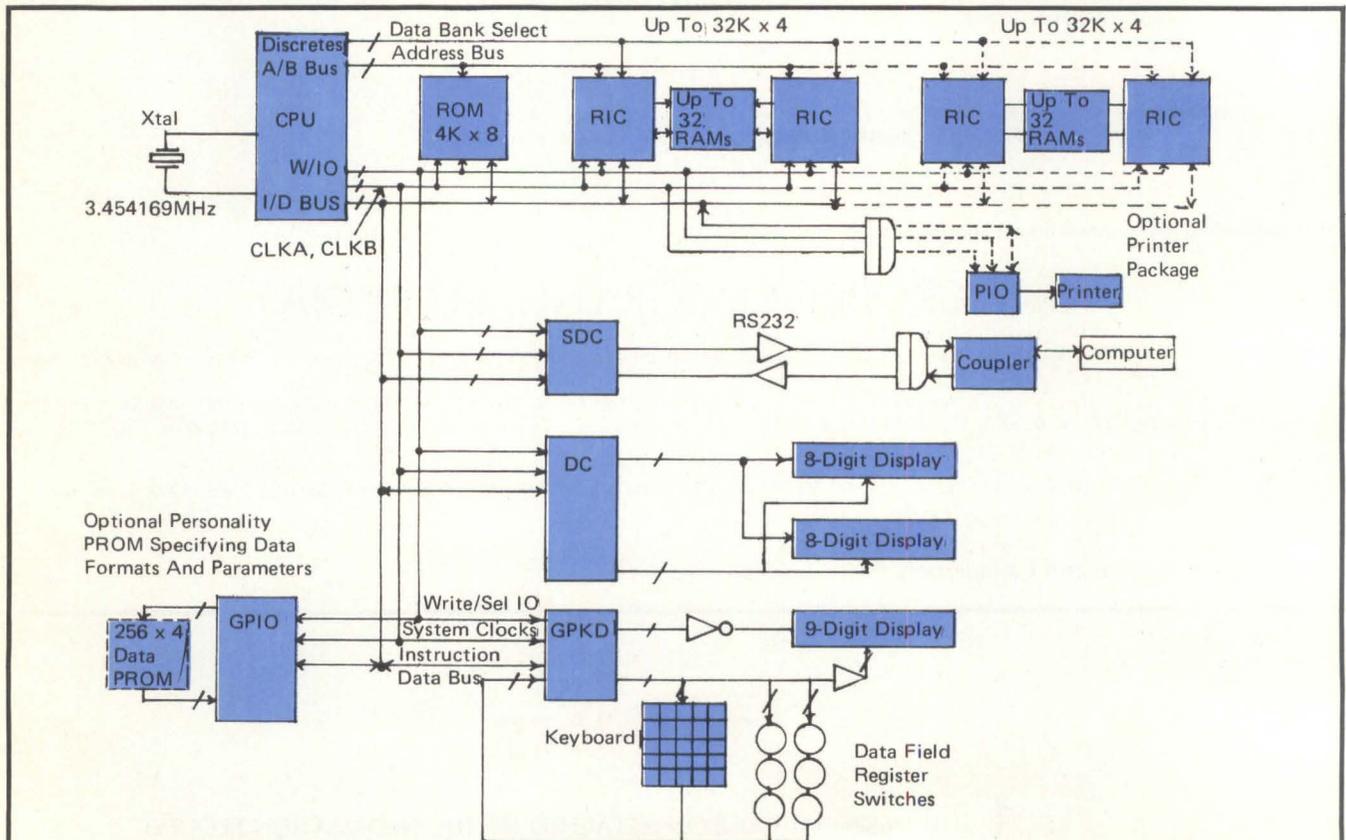
that firm's PPS-4/2 microprocessor.

**Good fit.** "The beauty of the system was that it fit so well with the set of chips — there seemed to be a chip

available for just about every function required," says John Lishman, Rockwell design engineer on the Wordsmith project. The system's special-purpose chips include a serial data controller (SDC), a general-purpose keyboard/display circuit and a display controller.

Controlled by the SDC via software, the terminal's RAM-stored data goes at 1200 baud to a central computer through an acoustic coupler and an RS 232 interface. A printer port lets a user also obtain a local hardcopy readout of the terminal's contents.

The general-purpose keyboard/display circuit monitors the terminal's 25-station keyboard and six register switches and controls the unit's lower,



A serial data controller (SDC) oversees the transfer of data between the portable terminal's RAM and a central computer, thereby easing the processing task of the system's microprocessor. The terminal's basic storage capacity equals 4K x 4 characters; expansions extend this capacity to 64K x 4. Other system components include a Rockwell PPS 4/2 microprocessor CPU, a general-purpose keyboard-display chip (GPKD), a general-purpose input/output chip (GPIO), a display controller (DC), a RAM interface chip (RIC) and a programmable I/O controller (PIO).



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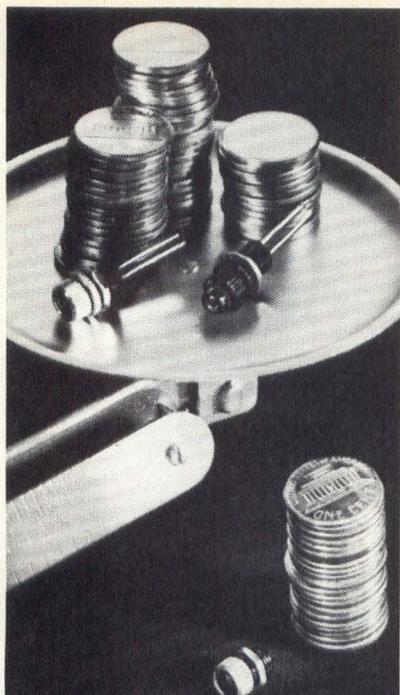
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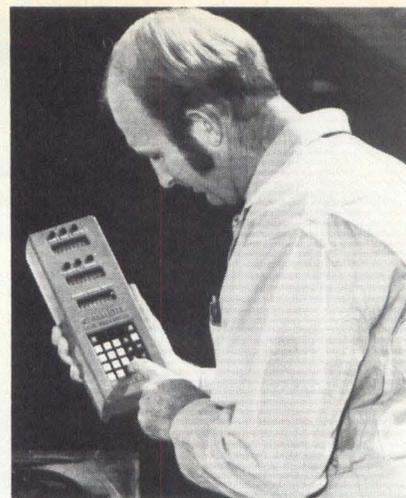
CIRCLE 17

9-digit entry register. The display controller circuit handles the unit's two upper, 8-digit displays; a user transfers a data field for a given input from the entry register to the appropriate portion of the upper displays and thereby builds up the input field-by-field to minimize data-entry errors.

When all data fields for the input are complete, activating the terminal's "enter" key transfers the input to RAM. Lishman notes that the basic microprocessor-system configuration stores 4K x 4 characters and that memory expansions allow a maximum 64K x 4 addressing capability. In an application that requires storing 28 decimal digits for each input, one 4K RAM can accommodate about 145 inputs.

The terminal's design philosophy differs from that of at least one tape cassette-based portable terminal; that unit's designer (*Digital Design*, October, page 32) rejected using special-purpose I/O chips to ease its microprocessor's burden because he wished to minimize the unit's power consumption and size.

**Solid state cuts error rate.** In specifying that the terminal should use RAM rather than tape as an input medium, Wordsmith aimed to capitalize on the ease with which a computer can detect and correct errors in RAM-stored data, explains Wordsmith president Vince Kennedy. If a computer detects an error in a transmission from a cassette, it must ask for a retransmission of the



Portable terminal's user enters a data field for an input and then transfers the field from the terminal's lower entry register to the appropriate part of the upper two displays. After entering all fields this way, the user transfers the entire input to RAM. The terminal's manufacturer claims this field-by-field entry procedure cuts data errors.

entire data block and repeat this process until the transmission arrives error-free, he explains.

By contrast, with data stored in RAM, "we check after each record is sent; it's just like two computers talking to each other." If an error occurs, the terminal can retransmit the faulty record immediately. "We didn't see any way to do that with a cassette."

## Microcomputerized traffic analyzer guides faithful in Moslem pilgrimage

Although it could have designed a comparable system with hardwired logic for about the same \$59,000 cost, a manufacturer of proprietary electronic equipment chose instead to build its automated traffic-analysis network around microprocessors, an approach that the firm's chief engineer says accommodates display-format changes and expansions more easily than alternative design schemes.

Installed early last October by the Saudi Arabian government, the distributed microcomputer network gathers and processes traffic-flow data during the Haj, one of the great spiritual events in the Islamic world. During the two-week annual festival, 1.5 million Moslem faithful from Saudi Arabia and other countries journey to the holy cities of Mecca and Medina, where they perform a complex series of religious rituals dating back over 1300 years.

To help Saudi police control the traffic jams created by this population influx, the traffic-analysis system incorporates a computerized central processing station and ten microprocessor based data-acquisition systems situated along strategic roads in and around Mecca. Developed by Martek International, Salt Lake City, the system requires about 30 fewer ICs than a comparable hardwired design, says chief engineer Ronald Ward.

Each of the ten remote monitoring systems incorporates an inductive wire loop that for one week continuously measures traffic volume in 15-minute intervals. Buried in the highway pavement, this wire loop continuously transfers the raw traffic data first to a detector and then to a nearby Model 6502 microprocessor, manufactured by MOS Technology, Norristown, PA.

The microprocessor divides its asso-

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ciated RAM into slots corresponding to each 15-minute observation period. When it receives a loop detector's output, the microprocessor, clocked at 1 MHz, files the data in the appropriate memory location. It also converts the input from parallel to serial form for subsequent transmission to the central computer. After one week, Saudi traffic-control officials empty each microprocessor's memory to make room for another batch of information.

**Microwave communication.** From microprocessor memory, the remotely gathered traffic data goes to an on-site

subcarrier modulator, which continuously relays the information by microwave transmission to the central processor at traffic-analysis headquarters. Martek chose microwave transmission to serve the Saudis' need for real-time analysis, but in applications not requiring continuous data transfer, the system could temporarily store traffic-flow information in a portable tape recorder.

Like its counterparts in the field, the central microcomputer incorporates a Model 6502 microprocessor. Equipped with 65K of memory, the central computer mathematically analyzes the data

and converts its calculations into four display formats: digital readouts of current traffic-flow rates at each of the ten monitoring stations, bar charts, tables and digital readouts of cumulative traffic volumes.

The tabular format incorporates two data columns—one for displaying total traffic volume for the current day, the other for breaking down that traffic-volume figure by minute and hour. The fourth format displays cumulative traffic volumes for each day of the week.

By displaying traffic data in different formats, the system lets Saudi police almost immediately visualize traffic conditions on each monitored road at any time of the day, Ward says. From these readouts, police can determine which highways are open and which have reached saturation levels so that they can plan appropriate control measures.

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**Gathering traffic data during a Moslem pilgrimage, the microprocessor based traffic-control system requires about 30 fewer ICs than a comparable hardwired design.**

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By viewing the displays singly or in various combinations, police can also detect traffic-flow patterns, predict trends, compare current readings with past figures and compile histories of the roads' traffic conditions.

**Dual fonts required.** After the central computer completes its processing functions, the system's traffic data goes through a switcher to a subcarrier demodulator and finally to a Model 588 printer manufactured by Centronics, Hudson, N.H.

Martek aimed chiefly to provide the system with as many data-display formats as possible, says Ward, adding that the most serious design problem was the system's initial inability to generate legible printer output.

The firm's first effort to print traffic data in Arabic ended in "disaster," Ward admits. Many of the characters generated by the printer fit together incorrectly or for other reasons proved illegible to the company's Saudi clients. Much of the difficulty stemmed from the lack of a character font large enough to accommodate the Arabic alphabet and all its possible variations. Arabic characters vary in shape and size depending on whether they appear at the beginning, middle or end of a word.

To generate all the necessary Arabic characters, Ward and his colleagues configured the printer to alternate under program control between two charac-

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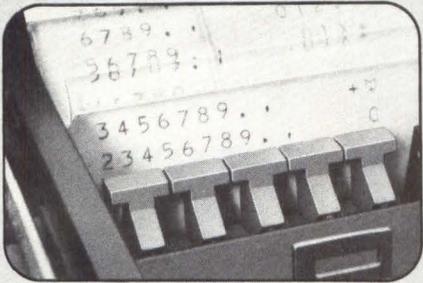
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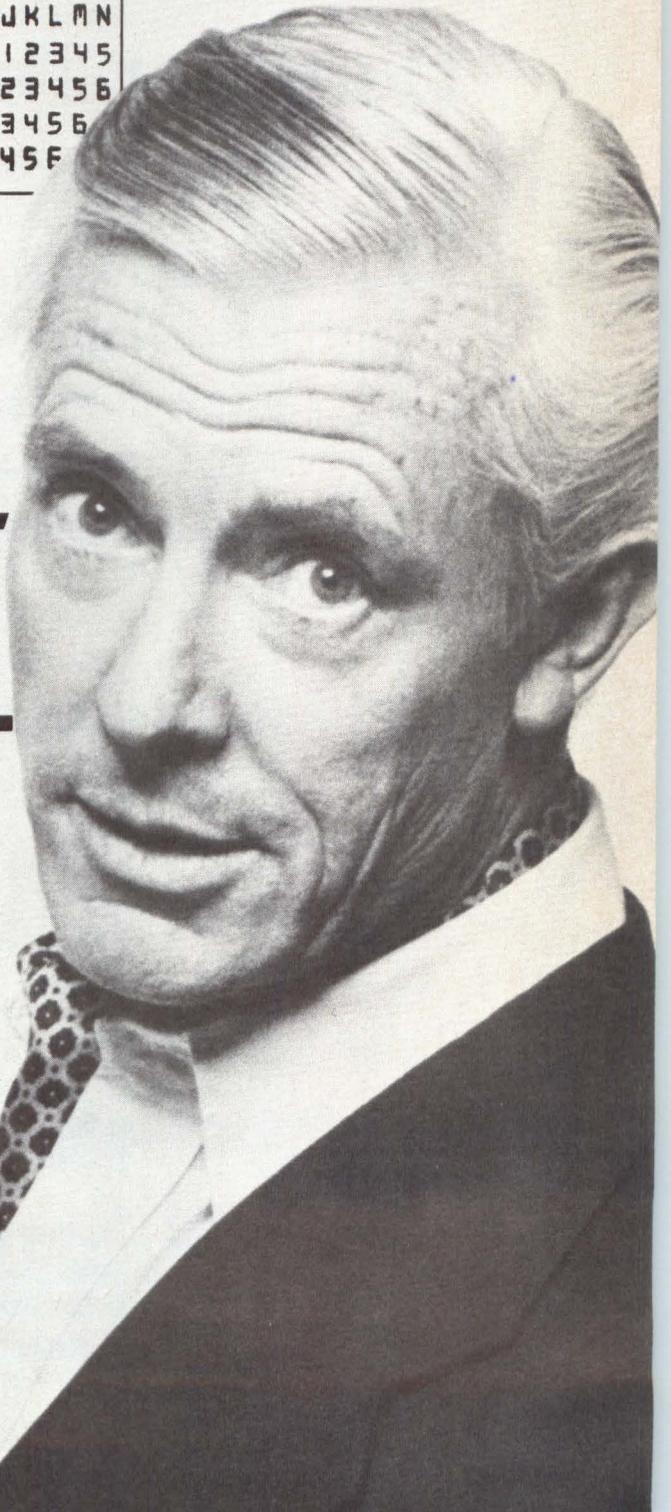
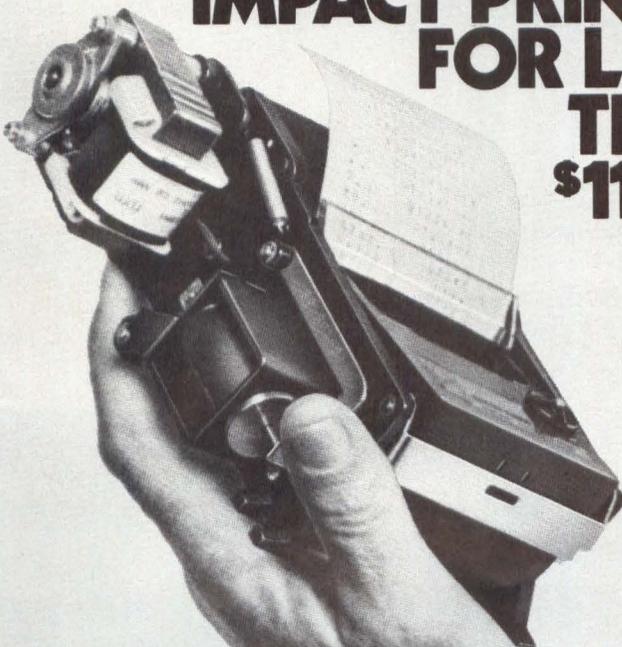
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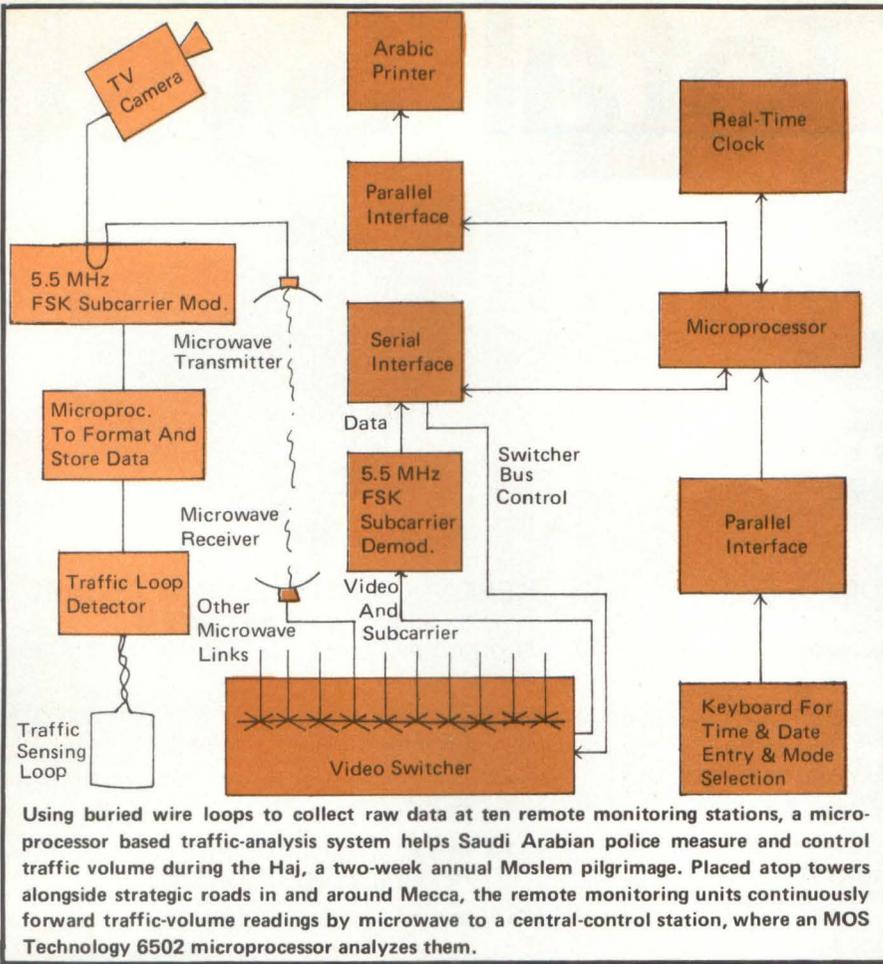
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ter fonts. As a test, they then printed the system's hexadecimal code, which they asked the Saudis to translate along with a series of statements, including error messages and titles. After noting the resulting translation errors, they rewrote the system's software to alternate the two character fonts in different combinations and repeated the procedure by trial and error until they had eliminated all mistakes.

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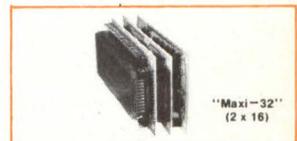
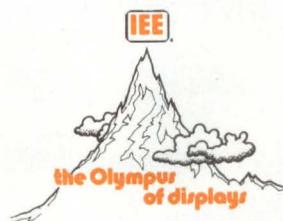
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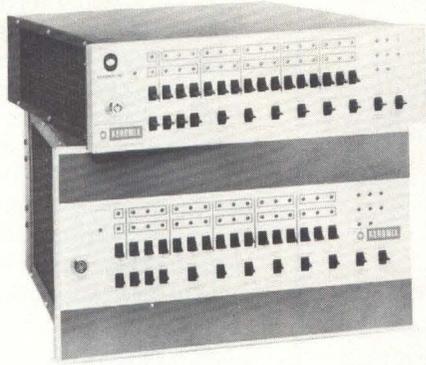
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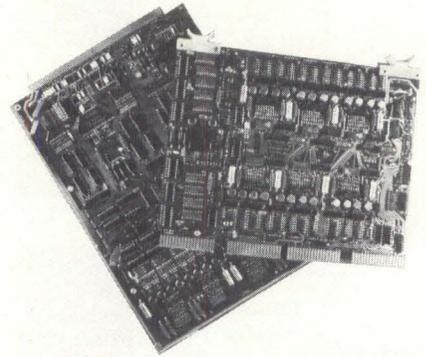


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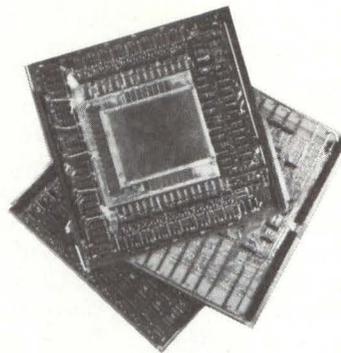
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can thus continue to use the 8080 and switch over to the newer CPU and its support chips as they appear in larger quantities, says William Davidow, VP and general manager at the Santa Clara, CA, firm.

The 8085 CPU and its support chips differ in detailed structure from the 8080 family; the hardware modifications allow these major system changes:

★ A typical 3-chip system — 8085 CPU; 8155 2K RAM, I/O and timer; and 8355 16K ROM and I/O (or 8755 16K EPROM and I/O) — can replace ten or more 8080-system components.

★ Operating rate with standard-speed memory measures 3 MHz, compared with 2 MHz for the 8080.

★ All 8085-system components require one +5 V supply; the 8080 system requires +5, +12 and -5 V.

**Performance improvements.** Detailing some of the performance upgrades allowed by the 8085 and its support chips, MCS-85 product manager D.W. Sohn points out that all components in the family incorporate circuitry that eliminates the need for buffers or decoders except in large systems. Each component sources up to 400  $\mu$ A and provides a full TTL load of sink current.

The 8085 CPU sports a 1.3- $\mu$ s typical instruction time, compared with 2

$\mu$ s for the 8080. A designer can further increase throughput by utilizing the 8085's built-in interval timer and interrupt control to replace conventional software and external devices.

The 8085 CPU contains six general-purpose 8-bit registers, an accumulator, an arithmetic logic unit, a 16-bit program counter and a 16-bit stack pointer. A designer can use the registers in pairs for 16-bit operations and the processor for binary or BCD arithmetic operations. The CPU addresses up to 65K bytes and up to 256 I/O ports; the built-in interrupt control handles four levels of vectored priority interrupts.

Unlike the 8080 CPU, which drives separate 16-line address and 8-line data buses, the 8085 has an 8-line address bus and an 8-line multiplexed address/data bus. The change frees eight CPU pins for the four interrupt inputs and serial-in and serial-out ports. Users must modify existing 8080 software only if they wish to utilize the 8085's added features.

## Hardware/services

**TMS-9900 evaluation board.** Incorporating the Texas Instruments TMS-9900 16-bit microprocessor, this 7" x

16" board provides a 13-instruction monitor that allows inspection of that microprocessor's register. It also incorporates an EPROM programmer for writing user programs into TMS-2708 UV PROMs. You can expand the system to form a 65K byte computer by adding two 32K memory boards. Price, with documentation and wall-chart schematic: \$269 unassembled, \$369 assembled. Technico, 9130 Red Branch Rd., Columbia, MD 21045. (800) 638-2893 **Circle 139**

### Z-80/MDS microcomputer board.

This board allows users of Intel's Intellect microcomputer development system to upgrade that system to a Z-80 processor and a Z-80 disk based assembler. It provides switch activated single-cycle capability and incorporates LEDs to indicate memory or I/O access. The unit will run with ICE-80, ICE-30, ROM simulators and other Intel accessories. You can obtain either a disk based assembler (for use with the ISIS DOS system) or a stand-alone version (for systems without a floppy disk). Price, with software: \$1490. Relational Memory Systems, 150 Saratoga Ave. # 332, Santa Clara, CA 95050. (408) 248-6356 **Circle 134**

# MDB SYSTEMS presents... The NOVA\* Connection

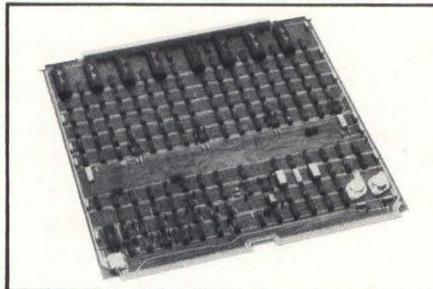
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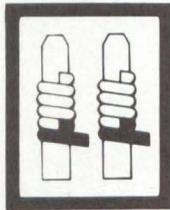
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CIRCLE 24 FOR NOVA; 25 FOR PDP-11; 26 FOR INTERDATA; 27 FOR LSI-11.



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# HOT TIME

## In The Old Factory

Neither heat, dirt, electrical noise nor interconnection problems stay industrial microcomputers from the performance of their tasks — if they're properly designed.

by G.E. Kimble

Gene Smurda 77'

A chicken in every pot, a car in every garage, a microprocessor in every factory — while politicians attempt to realize the first two parts of this dream, semiconductor manufacturers and electronic-equipment builders push to fulfill the third. That way, industry will be able to manufacture enough pots and cars to accommodate all those garages and chickens.

But car and pot factories — indeed most factories — lack the docile environment that electronic designers crave for their equipment. So designing control systems for use in damp paper mills, dusty warehouses, caustic-atmosphered steel mills or oil-laden machine shops can prove difficult.

Consider the case of a complex dc logic control system installed near a window on the west side of a coil-steel processing plant, where its oil-tight cabinet felt the full effect of the afternoon sun. One day, a high-pressure hydraulic line near the cabinet burst and sprayed fluid into the cabinet's open door. Surprisingly, the electronics continued functioning — until someone removed a PC card and then replaced it. Oil on the contacts had caused the malfunction, and the situation deteriorated rapidly as the maintenance staff removed and replaced more cards in their attempts to diagnose the problem. This case could be a little extreme, but it illustrates the problems facing designers of even moderately high-speed industrial electronic control systems.

Computerized controllers present those designers with even greater difficulties. With their TTL voltage levels and nanosecond response times, they make even more critical the

electrical transients and long interconnections that arise in industrial applications. Although today's semiconductors exhibit improved temperature characteristics, their higher operating speeds (Table 1) aggravate system susceptibility to the broadband, random white noise that envelops most industrial operations.

### design constraints and goals

Faced with these problems, how can a designer of an industrial microprocessor control system best deal with them?

Recognizing the super-hostile environment for which your system is probably destined, investigate such constraints as maximum ambient operating temperature, conducted and radiated noise susceptibility limits, and structural limits such as shock and vibration tolerance. Such constraints generally stem from the engineering standards of your firm, and they are often "component limited." Some typical numbers appear in Table 2.

Design constraints established, you're ready to firm up your overall system design goals. The noise susceptibility of any semiconductor family is well-established — the higher a family's logic threshold, the better its noise immunity (Table 3). But you'll derive maximum benefit from using a particular logic family only if a primary goal in your design is to maintain careful circuit-to-circuit interconnections, especially between ground points.

The ground bus is the one bus common to all circuits in your system. And in a "spider web" ground system, unwanted signals can appear at key circuit points. The circuit furthest from the bus' main ground point experiences all of the noise the circuits closer to that point generate, and it can misfire in response to combinations of those circuits' random noise signals.

*Gene Kimble is an administrative engineer at the Eagle Signal Industrial Controls Div. of Gulf + Western Manufacturing Co., Davenport, IA.*

To deal with this problem in our Eptak industrial microprocessor controller, we strove to achieve single-point grounding by using ground planes with wide ground runners and by minimizing the number of current nodes tied to any of these ground runners. Minor field modifications have sometimes improved on this approach, but we have found that providing a single common connecting point for the power supply dc return, the chassis connection and an earth-ground connecting point normally produces the best results (Fig 1).

The individual ground return paths for each circuit in the optimum grounding layout shown in Fig 2 generally don't suit systems with a computer bus structure, however. But utilizing empty backplane area as a ground bus provides results that approach this ideal layout. The wide expanse of ground surface also serves as an electrostatic shield (Fig 3).

Minimizing the effects of transmission-medium discontinuities should constitute another primary design goal. The slower a semiconductor device responds to an input, the less likely it is to respond to transients. But the nanosecond switching times exhibited by today's electronics — and mandated by the need for "near real-time" operations in industrial control applications — can produce ringing, overshoots and reflections in connections unless you utilize matched line terminations at junctions between modules and backplanes and between backplanes and interchassis cables.

Establishing such matched terminations involves making connections through resistors and capacitors whose values — usually determined empirically — tend to reduce the magnitude of the circuit disturbances (Fig 4).

### implementing a design

Once you've investigated design constraints and set overall design goals, you can begin choosing the family of devices that will meet your needs. Decisions in this area are highly subjective, but some guidelines I consider basic are:

- ★ Choose the most up-to-date microprocessor available from a reputable source.
- ★ Develop a general-purpose rather than a dedicated system.
- ★ Continually strive to achieve greater computing power and system speed — set your sights high.
- ★ Develop your own medium- to high-power language; existing languages rarely suit the characteristics of your system.

**Table 1. Semiconductor Operating Speeds**

Semiconductor Type	Vintage	Switching Time
silicon junction transistor	early 1950s	0.5 - 1.0 $\mu$ s
silicon planar transistor	early 1960s	20 - 30 ns
TTL integrated circuit	late 1960s	10 - 15 ns

**Table 2. Typical Design Constraints For An Industrial  $\mu$ P System**

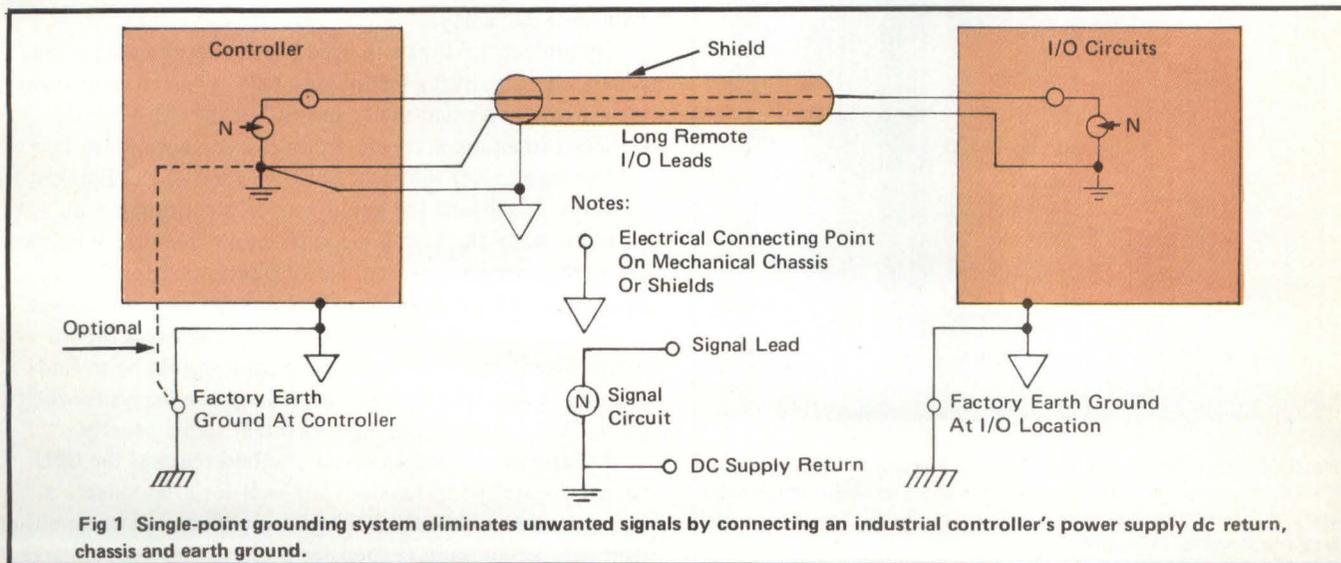
Operating temperature	0-140° F
Operating supply voltage variation	Standard input voltage, +10% -15%
Conducted noise susceptibility	1000 V spike superimposed on input voltage
Vibration	2.5 G @33 Hz - three axes

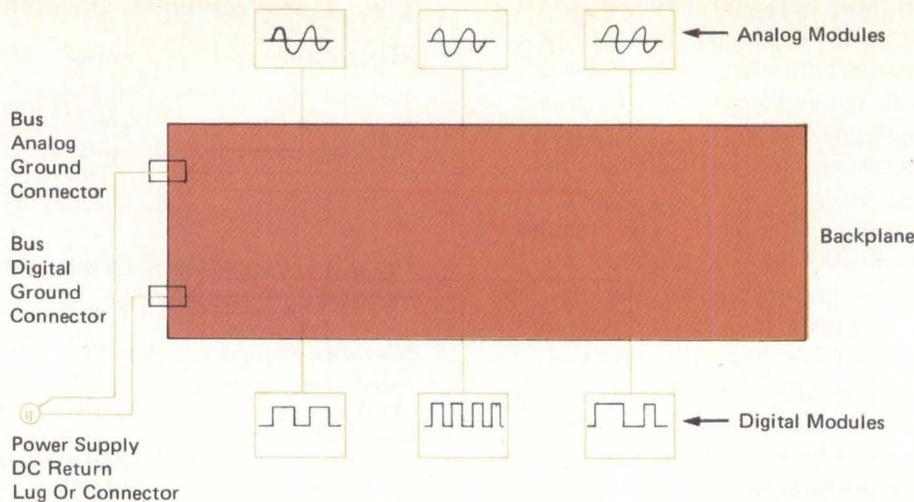
**Table 3. Semiconductor Logic Thresholds**

Semiconductor Family	Threshold Voltage (V)	
	Low	High
Silicon transistor	0.5	1
TTL	0.8	2
HINIL (1)	5.0	6.5
MHTL (2)	6.5	8.5

(1) High Noise Immunity Logic  
(2) Motorola High Threshold Logic

In general, strive to utilize the newest technology available. ROM choice constitutes one area that could require some difficult decisions. You probably won't consider unalterable, fusible link units for a general-purpose system, but should you use UV PROMs or "electrically alterable" MNOS units? Currently the most popular type of PROM, a UV-erasable unit offers access times compatible with current microprocessor speeds. You can program it in your system by using an extender card to take advantage of system power supplies,





**Fig 2 Optimum grounding layout utilizes single-point configuration. Systems that utilize a computer bus structure may require compromises on the optimum arrangement to suit physical limitations.**

timing signals and program source. MNOS devices, on the other hand, offer the advantage of alterability of selected memory locations, but they have not gained wide use yet because of their need for periodic refreshing.

Now consider some specific design areas and the techniques you can apply to solving the problems that can arise in each of them.

**Temperature requirements.** Despite every engineer's awareness that "heat is bad for electronics," many designers cram too much power in too small a volume. And when specifying

an ambient temperature, they often forget to consider internal cabinet-temperature rises.

When you establish a maximum operating ambient, consider both the design limits of the components you use and the zeal with which you intend to stuff those heat-generating components into a small package. The Eptak's Intel 8080 and its support chips can withstand temperatures ranging to 70°C; we focused on an open-construction cabinet design to achieve the required convection cooling of these devices through external air movements.

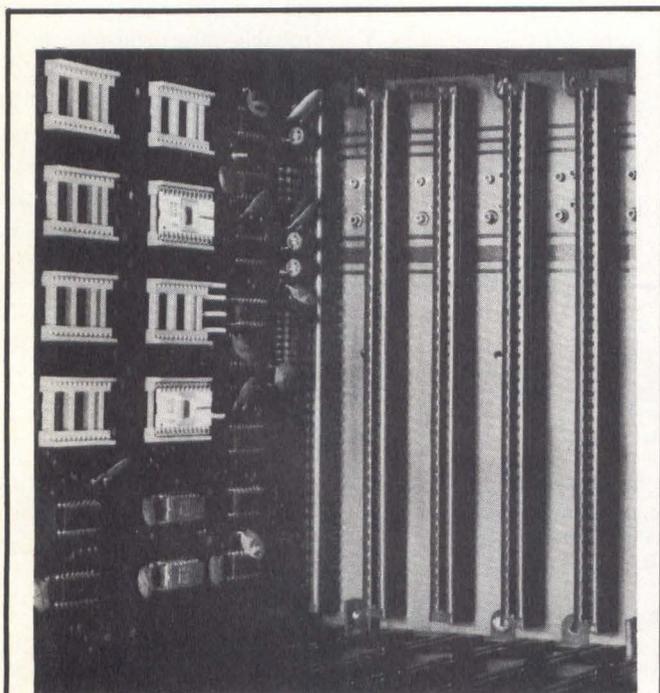
**Electrical noise.** Communicating noise specs can be like describing a sunset to a person who has never seen the sky. Little commonality in noise testing and noise definition exists in the industrial world, though military and aerospace specs provide a starting point.

But the elaborate test equipment used to measure military and aerospace equipment performance generally isn't used in industry, either because it doesn't accurately simulate factory noise or because it's too expensive. However, you can purchase some controlled noise testing by commercial labs for \$500 to \$600 a day.

We subject the Eptak to broad-spectrum radiated noise generated by sparking techniques. One of our most grueling tests, lovingly termed the "zap test" or the "Q.A. sting," utilizes a small-diameter electrode charged with 3600 V @ 60 Hz. Passed over the most sensitive areas of the Eptak's anatomy, it subjects the equipment to a continuous arc.

**I/O system.** Because some applications require an industrial microprocessor system to control hundreds of input/output signals, the system's I/O circuitry represents a large percentage of total system cost and thus deserves careful design attention. Your primary concern should be to find the most cost-effective way of handling line delays for remote I/O without paying an exorbitant speed penalty.

The simplest communication method requires the CPU to interrogate the I/O system and wait for a response — a time-consuming process. Such interrogations can occur either over parallel hookups (expensive because they require large



**Fig 3 Utilizing empty backplane area as a ground bus suits a controller with computer-system architecture and approaches the ground performance of the ideal layout shown in Fig 2. The ground surface also serves as an electrostatic shield.**

*Cont'd p. 42*

# /ability.

## It Comes Naturally With The Altair™ 8800b

The Altair 8800b from MITS: the second generation design of the microcomputer that started it all. The mainframe that has the abilities everyone is demanding from microcomputers today:

### Expand-ability:

The Altair 8800b power supply and one-piece, 18-slot motherboard allow efficient and easy expandability for memory and I/O options. All Altair PC boards are designed to give you maximum capability/lowest power usage possible per board. This means that for each slot used you get more features and require less power, than with any of the "off-brand" Altair-bus-compatible boards.

Whether you buy an entire system up front or choose to expand gradually, it's easy to get the configuration you need with the complete family of Altair peripheral equipment, including floppy disk, line printer, audio cassette record interface, A/D converter, PROM programmer, serial and parallel I/O boards.

choice of four different memory boards and many others.

### Reli-ability:

The unique design features of the Altair 8800b, which have set the standard for the microcomputer industry, make it the most reliable unit of its kind. The Altair 100-pin bus, the now-standard design used by many imitators, has been "standard" all along at MITS. The unique Front Panel Interface Board on the Altair 8800b isolates and filters front panel noise before it can be transmitted to the bus. The all-new CPU board utilizes the 8080A microprocessor, Intel 8224 clock generator and 8216 bus drivers.

### Flex-ability:

Meeting the diversified demands of an ever-increasing microprocessor market requires flexibility: not just hardware flexibility but

software flexibility as well. MITS software, including the innovative Altair BASIC language, allows the full potential of the Altair 8800b computer to be realized.

8K ALTair BASIC has facilities for variable length strings with LEFT\$, RIGHT\$, and MID\$ functions, a concatenation operator, and VAL AND STR\$ functions to convert between strings and numbers.

Extended ALTair BASIC allows integer, single and double precision variables, automatic line numbering and renumbering, user-defined string functions, PRINT USING for formatted output and a powerful EDIT command for editing program files during or after entry. Extended statements and commands include IF... THEN... ELSE, LIST and DELETE program lines, SWAP variables and Trace On and Off for debugging.

Disk ALTair BASIC has all the features of Extended BASIC with the additional capability to maintain sequential and random access disk files. Utilities are provided for formatting disks and printing directories.

In all versions of ALTair BASIC you get the ease and efficiency of BASIC for the solution of real world problems.

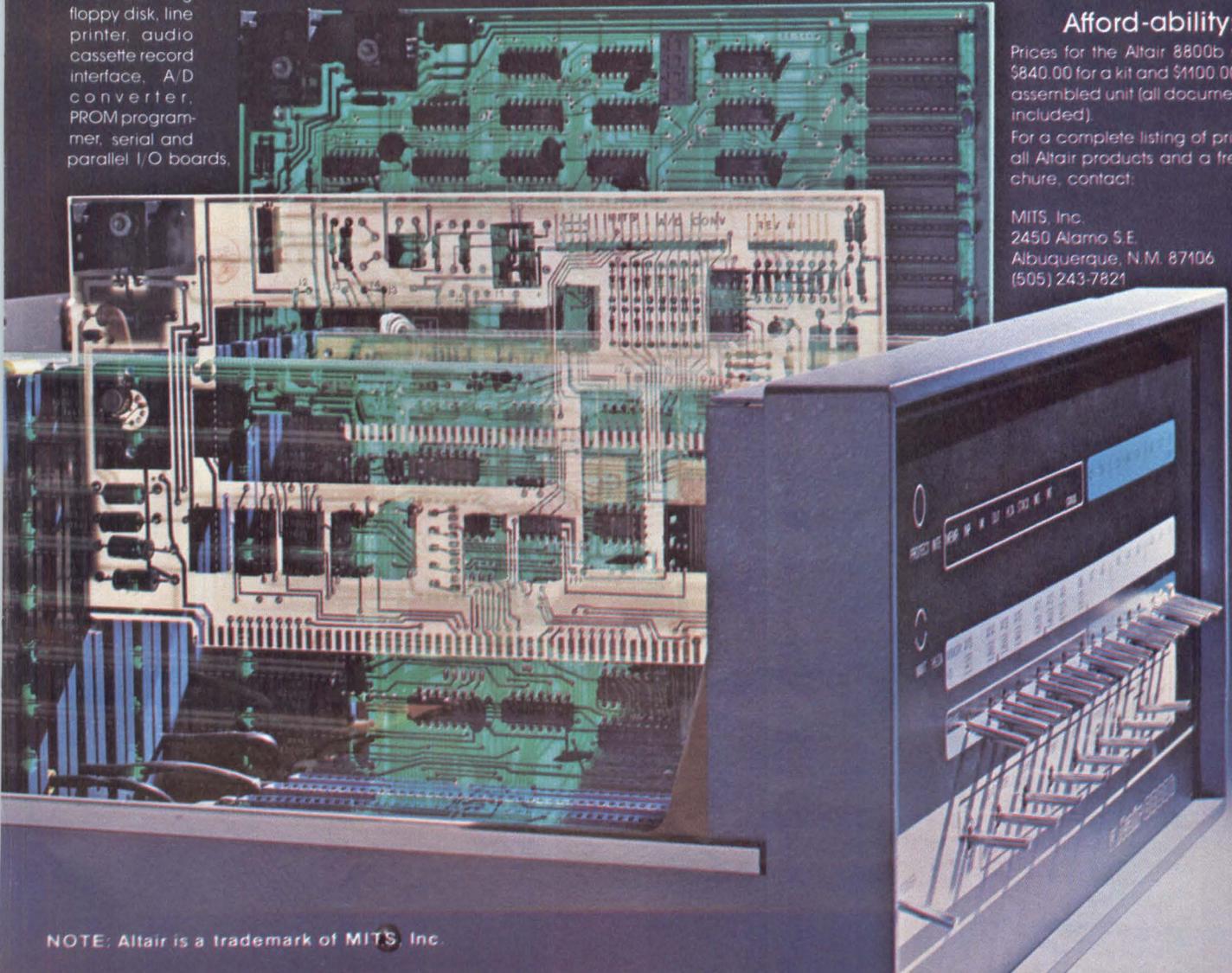
Package II, an assembly language development system for the Altair 8800b, includes system monitor, text editor, assembler and debug.

### Afford-ability:

Prices for the Altair 8800b start at \$840.00 for a kit and \$1100.00 for an assembled unit (all documentation included).

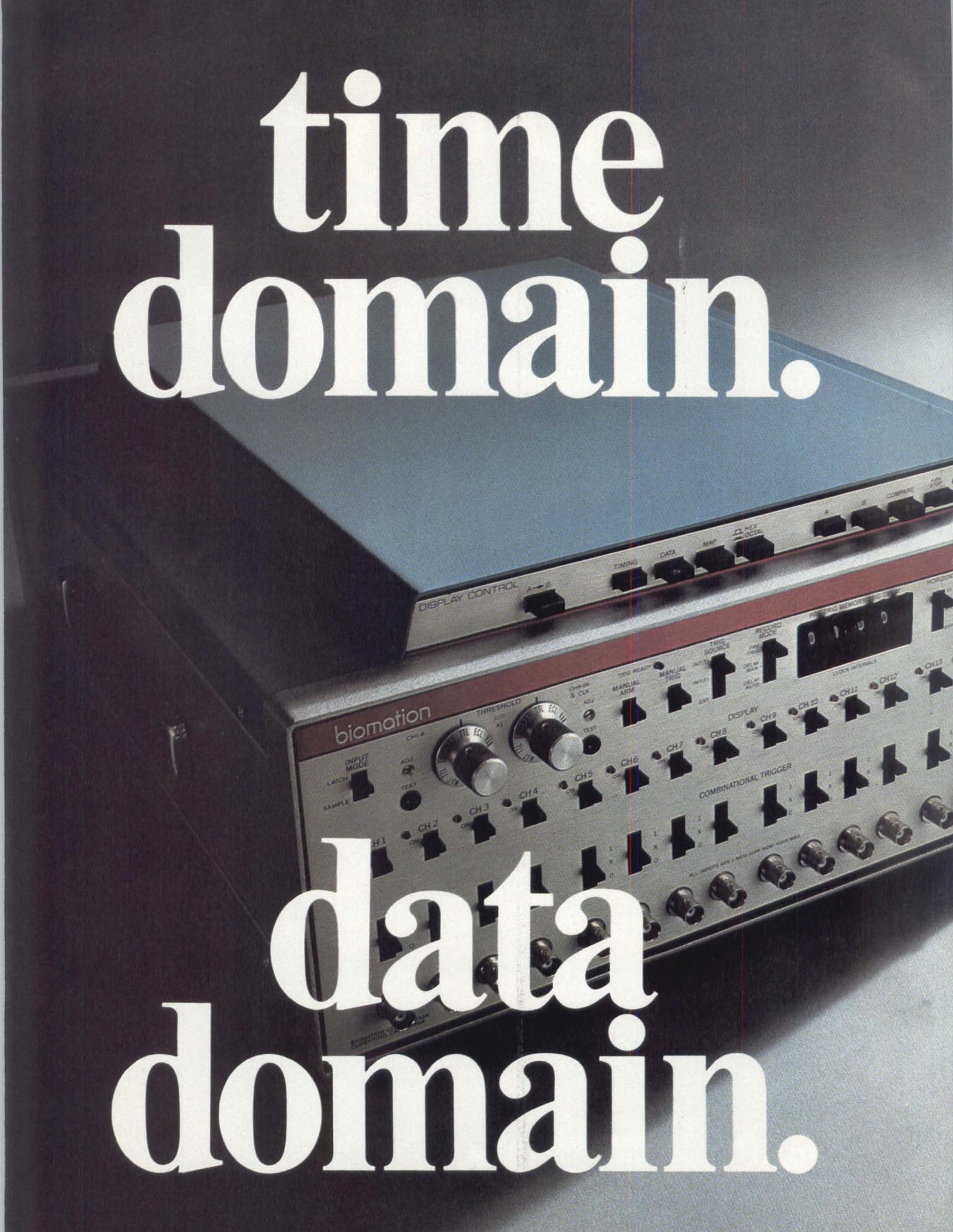
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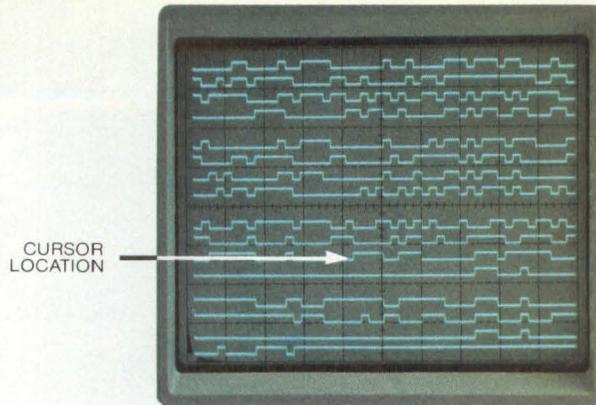
That's why we're providing a new set of tools which let you display timing information as well as logic word content—in the language of your choice.

Our new 1650-D logic analyzer gives you 16 channels at 50MHz. Our 851-D gives you 8 channels at the same speed.

Accessories can now give you a logic state (1's and 0's) display of any 16 stored words; hex or octal translation; and a vector map of memory contents. The 8 and 16-channel logic analyzers feature:

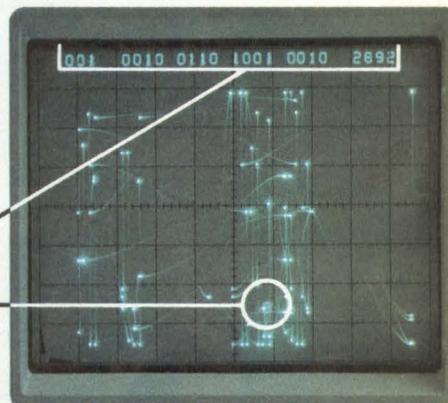
- Pretrigger and delayed trigger recording
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These are complex instruments and we can't give you all significant details here. But please write, call, or use the reader service card. We want to get this useful information into your hands. Biomatics, 10411 Bubb Road, Cupertino, CA 95014, (408) 255-9500. TWX: 910-338-0226.



CURSOR LOCATION

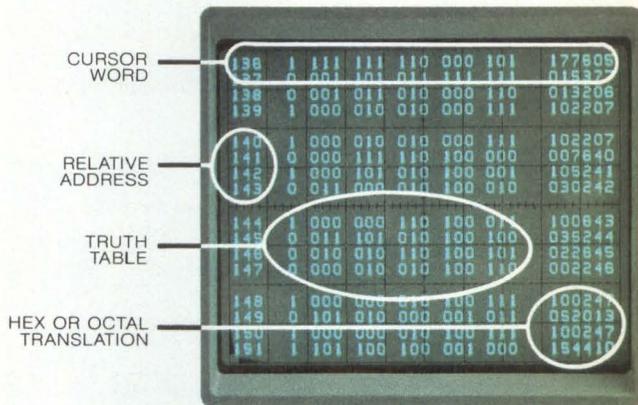
Biomatic's new 1650-D produces a repetitive display output reconstructing precisely 500 bits per line for a 16-line timing diagram on a conventional oscilloscope or CRT display. Separate selection of individual channel outputs allows viewing of 1, 2...16 channels at one time with automatic vertical expansion.



CURSOR WORD

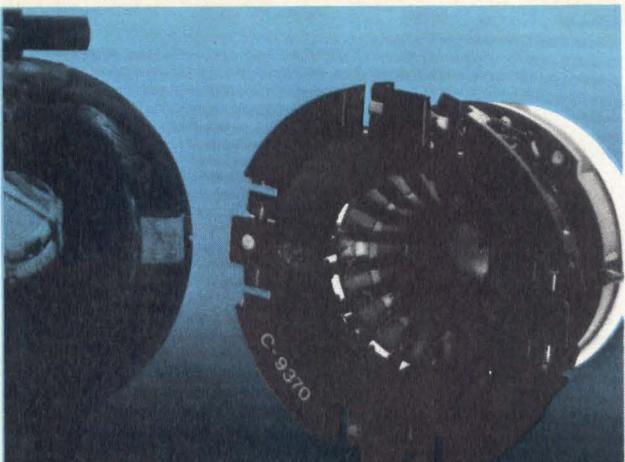
CURSOR

Map—each word in memory is transformed via two DAC's to form a unique dot which characterizes that word. All 512 words of the 1650's memory can be accessed for mapping. The cursor word is circled in the map as well as displayed at the top of the screen in alphanumeric form. The cursor may be moved to any of the points in the map for positive identification of that word. In addition, a map of only 16 words may be selected.



Logic state—provides memory address location, binary output of the 16 channels and selectable octal or hexadecimal translation. 16 words are displayed at one time with the cursor address location at the top of the screen. Movement of the cursor control allows accessing any 16 words of the entire 512 words stored in the 1650-D. The display control memory can store 16 words while a different set of 16 is selected from the 1650's main memory (or a new recording is made). These two sets of 16 words can then be overlaid on the CRT. Any differences will blink and be easily identified.

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Cost of labor to attach magnets	\$ _____	(not necessary)
Cost of labor to adjust magnets	\$ _____	(not necessary)
Cost of replacing rejected yokes that fall short of meeting customer standards	\$ _____	(not necessary)
Cost of recycling product that does not meet Q.A. standards due to yoke deficiencies	\$ _____	(not necessary)
Cost of field service to make adjustments to satisfy customer	\$ _____	(not necessary)
Extra sales expense and "persuasion" necessary to sell non-competitive displays	\$ _____	(not necessary)

"Bottom line" total \$ \_\_\_\_\_ \$25



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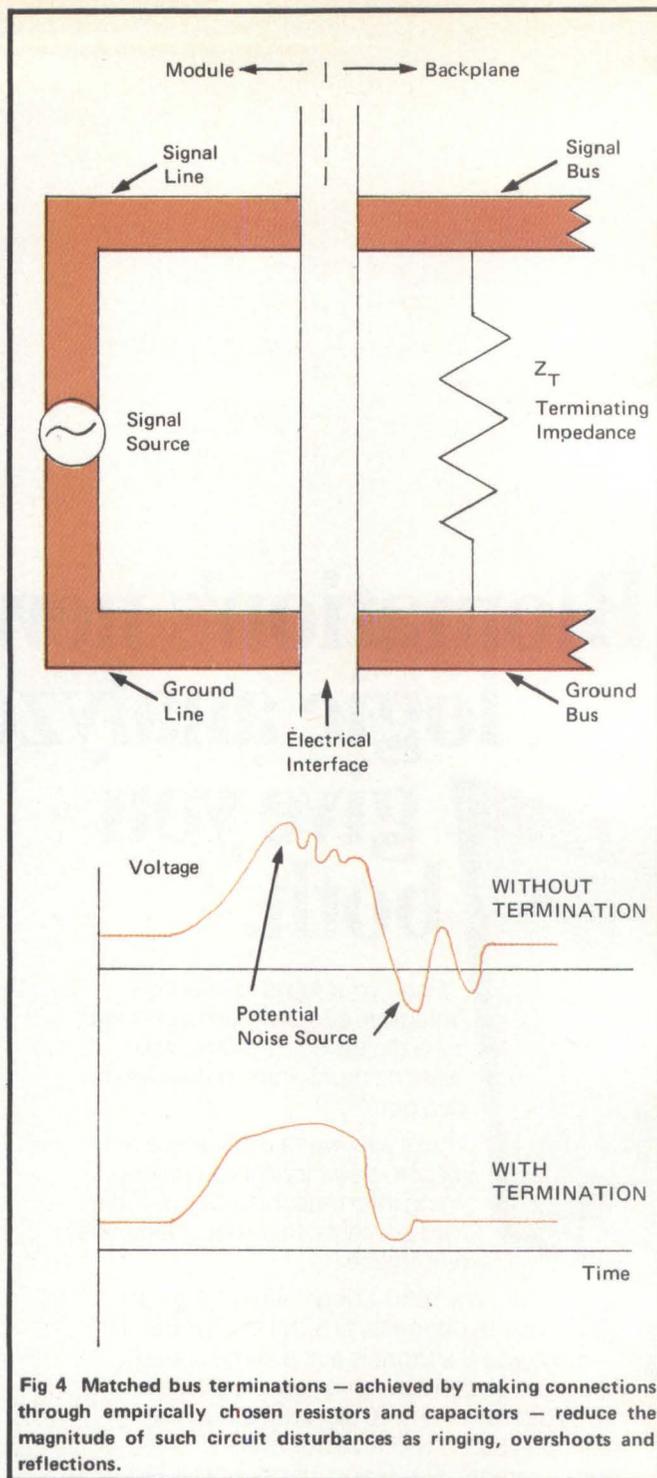


Fig 4 Matched bus terminations — achieved by making connections through empirically chosen resistors and capacitors — reduce the magnitude of such circuit disturbances as ringing, overshoots and reflections.

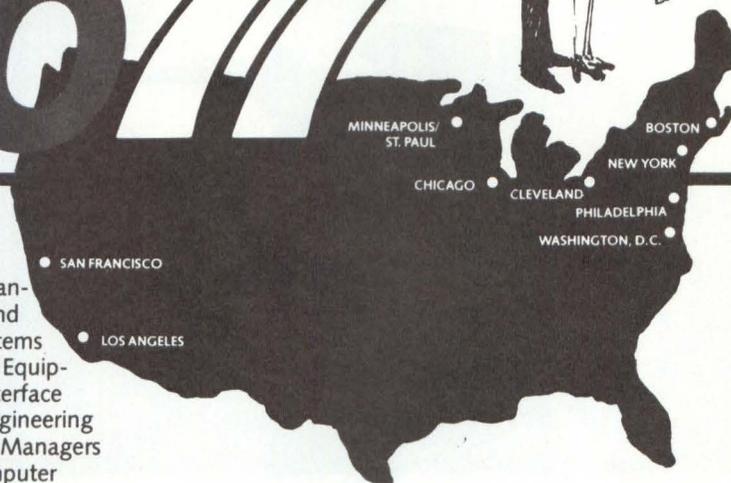
amounts of wire) or serial arrangements (cheaper but slower than the parallel approach).

Our approach in Eptak, chosen to make optimum use of the controller's computing time, is to continuously accept asynchronous serial data and store it in the controller until needed. Then, when the controller must address a particular I/O device, it can obtain the required information without delay.

This approach complicates the system's total I/O circuitry, but its time advantages outweigh that disadvantage. Another approach (probably the best way, but expensive in terms of both hardware and software) utilizes separate microprocessor circuits to process data at each remote point. ♦

# How to get your own free ticket to

# COMPUTER EXPO 77



**1. Circle the job title that most nearly describes your responsibilities:**  
Executive Management; Marketing Management; Engineering Management and Staff involved in: Computer-based Systems Design, Digital Systems Design, Digital Equipment Design, Digital Circuit Design, Interface Engineering, Data Communications Engineering and Consulting; as well as Operational Managers and Senior Professional Staff from Computer Using Organizations.

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**Los Angeles** Convention Center—April 5–7  
**Cleveland** Convention Center—April 19–21  
**Minneapolis/St. Paul**, St. Paul Civic Center—April 26–28  
**Chicago**, McCormick Place—May 3–5  
**New York** Coliseum—May 10–12  
**Philadelphia** Convention Center—May 24–26  
**Washington, DC**, Sheraton Park Hotel—May 31–June 2  
**Boston**, Northeast Trade Center (Rte 128, exit 39)—June 7–9

**3. Circle those dates on your business calendar.**  
Then show up and register! As a qualified professional, that's all you need to do to take part in the varied exhibits, demonstrations and exhibitor seminars.

**SEE:** *Live Demonstrations and Displays* of new computer products and services, including Minicomputers, Printers, Microcomputers, Microprocessors, Printer Terminals, ROM's and RAM's, Flexible Disk Drives, Power Supplies, Keyboards, Modems, Readouts and Displays, Cassette Systems, Magnetic Tape Transports, Core Memories, Graphics Systems, Miniperipherals, Small Business Computers, Software, Data Communications Equipment, and much more! Every day from 10 AM to 5 PM.

**VISIT:** *Free Exhibitor Seminars* covering the selection and use of these products and services. These free seminars will be held every day.

**ENROLL:** *Designer Forums\** will be conducted in five cities by leading designers and independent experts. Topics are Evaluating and Using Microprocessors (Tuesday) • Evaluating Peripherals for Mini- or Microcomputers (Wednesday) • Evaluating Memory and Storage Devices (Thursday) • (Designer Forums are scheduled in San Francisco, Los Angeles, Chicago, New York and Boston.)

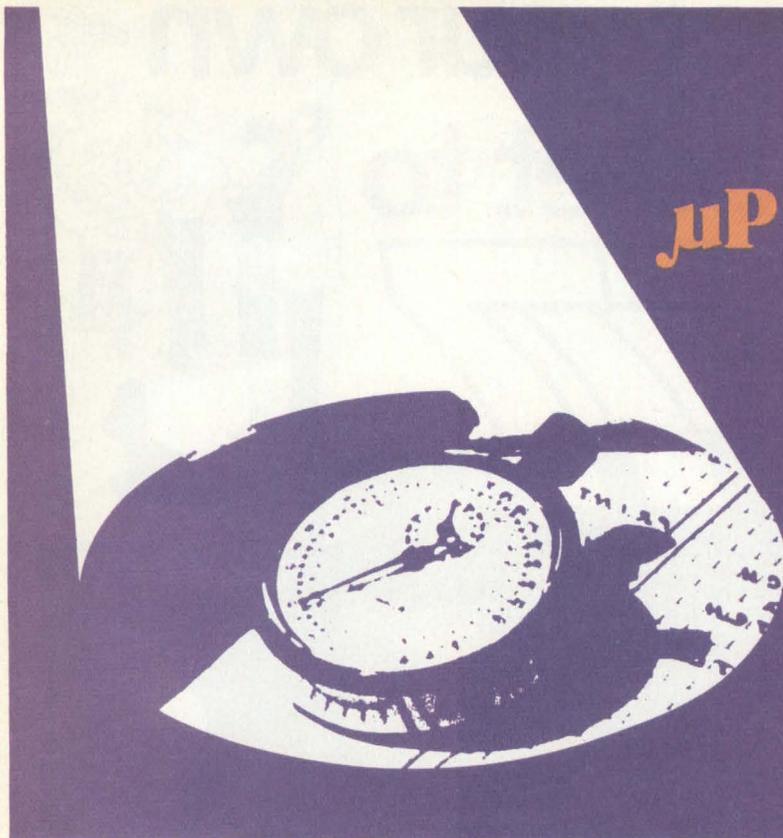
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## μP SOFTWARE:

# HOW TO OPTIMIZE TIMING & MEMORY USAGE

by Terry Dollhoff

Back in November, I started this series by examining the Intel 8080 – probably today's most popular 8-bit processor. This month I'll consider a chip that I feel thoroughly upstages the 8080. Zilog's Z80 offers all of the software and hardware features of the 8080 and more; software for the 8080 can run directly on the Z80 without change. But the Z80 offers more instructions than the 8080, so most programs written expressly for the Zilog processor are more efficient. The Z80 also offers several hardware advantages, including on-chip clock generation, which eliminates a chip from the system, and on-chip dynamic RAM refresh, which eliminates some external logic and headaches.

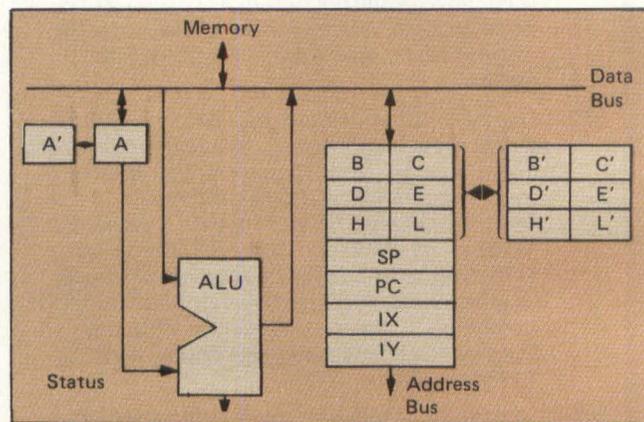
### structure and instructions

The Z80 (Fig 1) contains all of the registers of the 8080 and some extra ones as well. Register A functions as the accumulator just as in the 8080; register A' stores the primary accumulator and greatly improves interrupt response time. The other 8080 registers – B,C,D,E,H and L – are matched by a second set of 8-bit registers – B',C',D',E',H' and L' – which provide temporary storage for the primary registers and also help improve interrupt response time. Only the primary registers are manipulated by the Z80's instruction set; they hold temporary results or provide the operands of instructions that can modify the accumulator. Unlike the 8080, the Z80 also has a set of instructions that modify these working registers without modifying the accumulator.

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The Z80 incorporates four 16-bit registers – PC, SP, IX and IY. The program counter (PC) is the same as the 8080's, as is the stack pointer, which contains the address of the next available location in a last-in, first-out pushdown stack stored in RAM. The other registers – IX and IY – are index registers and resemble the 16-bit pair (H,L).

The Z80's two special-purpose registers are denoted by I and R. You'll rarely use the latter; it contains a memory refresh counter to enable the Z80 to perform dynamic memory refresh. You can load R by a program, but it automatically increments after each instruction fetch. The other special register – I – controls interrupts. The Z80 can operate in a mode where an indirect call to any memory loca-



**Fig 1** The Zilog Z80 contains the same complement of 8-bit registers as the Intel 8080, plus A', which stores the primary accumulator; and B', C', D', E', H' and L', which provide temporary storage for the primary registers.

tion can occur in response to an interrupt; the I register serves this mode of interrupt processing and stores the high-order eight bits of the indirect address. The low-order eight bits come from the interrupting device; this feature eliminates the need to store all interrupt response routines in the first few locations of memory.

Fig 5 summarizes the Z80's instruction set. Although the unit's designers chose different opcode mnemonics, you'll recognize the entire 8080 instruction set within the larger set (shaded portions). The nature of each instruction determines which of six addressing methods a program uses to obtain the instruction's operand, if any. The first four of these methods are the same as the 8080's:

★ **Direct addressing.** The operand lies in the memory location whose address is specified by the second and third bytes of the instruction. Because the Z80 is compatible with 8080 programs, the address is stored just like the 8080's direct address — least-significant byte first and most-significant byte second. A typical direct addressed instruction is

```
LD    A,(1234H) ; load A with 1234(hex)
```

It loads the contents of memory location 1234 (hexadecimal) into the accumulator and is stored in memory as 3A3412 (hexadecimal).

★ **Register addressing.** The operand lies in one of the general registers. For example, the instruction

```
BIT   1,D      ; test bit 1 of D
```

tests Bit One of register D. It sets status flags according to the result (1=EQ, 0=NE); this instruction is unique to the Z80.

★ **Register indirect addressing.** If the address of the operand lies in registers (B,C), (D,E) or (H,L), you can often reference that operand by a register indirect instruction. The register pair (H,L) provides the most flexibility for the operation. The 8080 treats the contents of the memory location referenced by (H,L) as M, a mythical 8-bit register; by contrast, the Z80 refers to the contents of (H,L) as (HL).

For example, the instruction

```
OR    (HL)     ; A=A or (HL)
```

logically ORs the contents of the memory location addressed by the register pair (H,L) with the accumulator and places the result in the accumulator.

★ **Immediate addressing.** The operand is provided by the second byte of the instruction. For example, the instruction

```
SUB   2        ; A=A-2
```

subtracts the constant 2 from the accumulator. Notice that the Z80 uses the same opcode mnemonic for immediate addressing as it does for register addressing; the assembler determines the proper instruction by examining the operand field.

★ **Indexed addressing.** The operand lies in the memory location whose address is specified by the arithmetic sum of the third byte of the instruction and one of the two index registers (IX,IY). Some of these instructions (e.g. INC) are three bytes long, while some (e.g. BIT) require four bytes. In both cases the offset is stored in the third byte of the instruction. For example,

```
RES   1,(IX+10) ; reset bit 1 of (IX+10)
```

resets Bit One of the memory location addressed by the contents of register IX plus 10 and stores the result in memory as DDCB018E. In Fig 5, denoting the opcode as DDCB.8E highlights the location of the offset.

★ **Relative addressing.** This method uses the byte that follows an opcode to specify a displacement from the existing program to which a jump can occur. This displacement is a signed two's complement number, added to the address of the opcode of the next instruction (address of the current instruction plus 2). The operation allows a transfer within the range of +129 to -126 of the current instruction. If

```
JR    +2       ; jump to (PC+2) + 2
```

were located at address 234 (hex), it would transfer control to address 238.

### using the index registers and manipulating bits

You can use the Z80's index registers to provide a powerful method of addressing data in memory. One of the 8080's major limitations is that you can't use any memory location except the one addressed by (H,L) as an arithmetic operand. But you can use one of the Z80's index registers to increase this capability to 256 locations. For example, the instruction

```
ADD   (IX+10)  ; add contents of (IX+10) to A
```

adds the contents of the memory location addressed by IX+10 to the accumulator. If you use the EQU (assembly time equivalence) instruction, you create the same operation by using this sequence:

```
ABC   EQU     10      ; ABC=10
```

```
ADD   (IX+ABC) ; add contents of (IX+10) to A
```

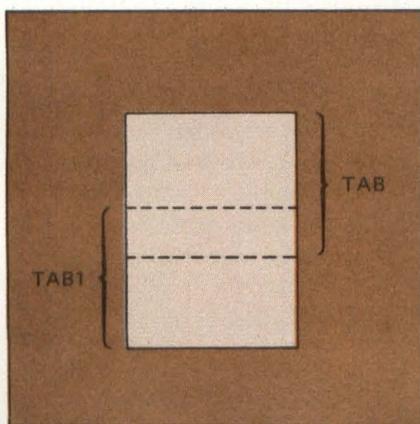


Fig 2 Organizing data in overlapping tables precludes the use of the Z80's LDI or LDIR instructions to move data from location TAB to location TAB1.

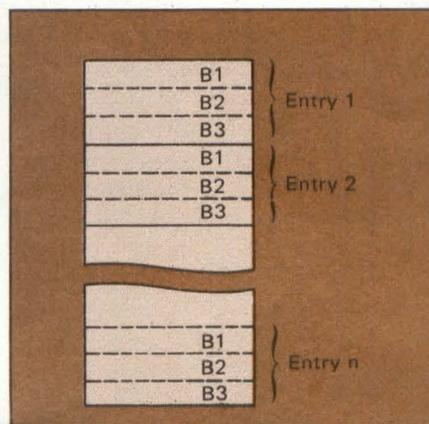


Fig 3 Organizing tables horizontally so that each entry's bytes are stored sequentially precludes effective use of the Z80's block-search instructions.

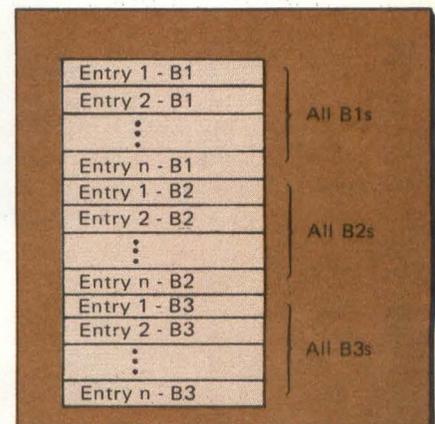


Fig 4 One way to avoid the time penalty that results from the search of a horizontally organized table involves reorganizing the table vertically.

EQU doesn't generate any Z80 code; it merely indicates to the assembler that the label ABC is the same as the constant 10. If you define a group of variables as:

```
VAR1 EQU 0 ; VAR1 is byte 0
XYZ EQU 1 ; XYZ is byte 1
THIS EQU 2 ; THIS is byte 2
```

```
LAST EQU 255 ; LAST is byte 255
```

you can reference each one as in the previous sequence. Because EQU doesn't generate any code, you must still reserve memory space and then initialize the index register so that it addresses the reserved area of memory. Code

```
MEM BSS 256 ; reserve 256 locations
LD IX, MEM ; preset IX to location MEM
```

to achieve this goal. If you've established your variables and reserved memory this way, you can use sequences like the following one, which adds XYZ to VAR1 and places the result in THIS:

```
LD A,(IX+VAR1) ; A=VAR1
ADD (IX+XYZ) ; A=A+XYZ
LD (IX+THIS),A ; THIS=A
```

This sequence requires nine bytes of code and replaces the following 11-byte 8080 sequence:

```
LDA MEM+VAR1 ; A=VAR1 (same as location MEM)
MOV B,A ; save A in B
LDA MEM+XYZ ; A=XYZ (same as location MEM+1)
ADD B ; calculate the sum
STA MEM+THIS ; THIS=A (same as location MEM+2)
```

Because the Z80 has two index registers, you can actually access two groups of 256 locations using this scheme, which isn't the only use for the index registers but is worthy of careful examination if you randomly address many different variables in memory.

The Z80 offers three instructions designed for bit manipulation — BIT, RES and SET; they test a bit, reset a bit to zero or set a bit to one and are useful for manipulating flags. For example, you can assign one of the general registers, say D, as a flag register, which provides the program with eight individual flags. To increase program readability, use EQU to define the flags. Here's an example:

```
FLAGA EQU 2 ; FLAGA is bit 2
SET FLAGA,D ; set the flag
```

```
BIT FLAGA,D ; test the flag
```

If you define variables as described earlier, you can put the flags in memory and avoid having to use a register. As a first step, define the flag word; then define the flags within the word. This sequence defines two flags (FLAGA and FLAGB) within the flag word FLAG:

```
FLAG EQU 14 ; flag word is word 14
FLAGA EQU 0 ; FLAGA is bit 0
FLAGB EQU 1 ; FLAGB is bit 1
```

To test one of the flags, use

```
BIT FLAGA,(IX+FLAG) ; test bit FLAGA of word FLAG
```

You can also use the bit-manipulation instructions to test the sign of one of the registers without modifying the accumulator. This sequence transfers control to YES if the

number in register E is negative:

```
BIT 7,E ; test the sign bit of E
JP NZ,YES ; jump if sign bit is set
```

If the number lies in the accumulator, a faster sequence to test for a negative number is still the one I discussed for the 8080:

```
OR A ; A=A or A
JP N,YES
```

### 8080-compatibility: less than 100%

Literature always describes the Z80 as 8080 instruction-set-compatible, but there's one little exception to this description. The incompatibility involves the Z80's parity/overflow flag; the Z80 expands the 8080's parity flag so it sometimes indicates parity and sometimes indicates arithmetic overflow (a condition that cannot be directly tested in the 8080.) The Z80 uses the flag as a parity flag whenever it performs logical operations (e.g. AND) and as an overflow flag whenever it performs arithmetic operations (e.g. ADD). The problem is that the 8080 *always* uses the flag to indicate parity. If the accumulator contains 120(78 hexadecimal) and you add the constant 104(68 hexadecimal) to it, you obtain

```
+120 0111 1000
+104 0110 1000
-----
1110 0000
```

The answer is negative, yet both operands are positive, so an overflow has occurred. In this situation the Z80 sets its parity/overflow flag, but if you perform the same operation on the 8080, the microprocessor ignores the overflow and sets the flag according to the parity of the result, which in this case is odd. This means that the 8080 would not set the parity flag. Therefore an incompatibility exists. This sequence branches to location Z80 if executed on the Z80 and to location I8080 if executed on the Intel 8080:

```
LD A,120 ; A=120
ADD 104 ; A=120+104
JP PE,Z80 ; jump to Z80 if parity is set
JP PO,I8080 ; jump to I8080 if parity is reset
```

This is the only incompatibility between the two microprocessors that I discovered, and it appears to be a very minor one. However, if you are a computer hobbyist using a Mits Altair computer, you'll quickly discover that this sequence or a similar one is used in the firm's version of Basic.

### table manipulation

Manipulating data stored in tables is a common task in microprocessor systems, and the Z80 has a special group of instructions that both move tables of data and locate an entry within a table. The four table-move instructions — LDI, LDIR, LDD and LDDR — each require that you preset the registers this way:

```
(D,E) = address of the destination
(H,L) = address of the source
(B,C) = number of words to be transferred
```

Each time the microprocessor executes the block transfer

Fig 5 Clip and save this summary of the Z80's instruction set. Though the opcode mnemonics are different, the shaded portions represent the 8080 instruction set, which forms a subset of the Z80's.

# Zilog Z80 Instruction Set

	A	B	C	D	E	H	L	(HL)	Imm	(IX+d)	(IY+d)	
ADD	87	80	81	82	83	84	85	86	C6	DD86	FD86	add register to A
ADC	8F	88	89	8A	8B	8C	8D	8E	CE	DD8E	FD8E	add register to A with carry
AND	A7	A0	A1	A2	A3	A4	A5	A6	E6	DDA6	FDA6	and register with A
BIT 0	CB47	CB40	CB41	CB42	CB43	CB44	CB45	CB46	—	DDCB.46	FDCB.46	test bit 0
BIT 1	CB4F	CB48	CB49	CB4A	CB4B	CB4C	CB4D	CB4E	—	DDCB.4E	FDCB.4E	test bit 1
BIT 2	CB57	CB50	CB51	CB52	CB53	CB54	CB55	CB56	—	DDCB.56	FDCB.56	test bit 2
BIT 3	CB5F	CB58	CB59	CB5A	CB5B	CB5C	CB5D	CB5E	—	DDCB.5E	FDCB.5E	test bit 3
BIT 4	CB67	CB60	CB61	CB62	CB63	CB64	CB65	CB66	—	DDCB.66	FDCB.66	test bit 4
BIT 5	CB6F	CB68	CB69	CB6A	CB6B	CB6C	CB6D	CB6E	—	DDCB.6E	FDCB.6E	test bit 5
BIT 6	CB77	CB70	CB71	CB72	CB73	CB74	CB75	CB76	—	DDCB.76	FDCB.76	test bit 6
BIT 7	CB7F	CB78	CB79	CB7A	CB7B	CB7C	CB7D	CB7E	—	DDCB.7E	FDCB.7E	test bit 7
CP	BF	B8	B9	BA	BB	BC	BD	BE	FE	DDBE	FD8E	compare register with A
DEC	3D	05	0D	15	1D	25	2D	35	—	DD35	FD35	decrement register
INC	3C	04	0C	14	1C	24	2C	34	—	DD34	FD34	increment register
IN (C)	ED78	ED40	ED48	ED50	ED58	ED60	ED68	—	—	—	—	input to register
LD A	7F	78	79	7A	7B	7C	7D	7E	3E	DD7E	FD7E	load A with register
LD B	47	40	41	42	43	44	45	46	06	DD46	FD46	load B with register
LD C	4F	48	49	4A	4B	4C	4D	4E	0E	DD4E	FD4E	load C with register
LD D	57	50	51	52	53	54	55	56	16	DD56	FD56	load D with register
LD E	5F	58	59	5A	5B	5C	5D	5E	1E	DD5E	FD5E	load E with register
LD H	67	60	61	62	63	64	65	66	26	DD66	FD66	load H with register
LD L	6F	68	69	6A	6B	6C	6D	6E	2E	DD6E	FD6E	load L with register
LD (HL)	77	70	71	72	73	74	75	—	36	—	—	load (HL) with register
LD (IX+d)	DD77	DD70	DD71	DD72	DD73	DD74	DD75	—	DD36	—	—	load (IX+d) with register
LD (IY+d)	FD77	FD70	FD71	FD72	FD73	FD74	FD75	—	FD36	—	—	load (IY+d) with register
OR	B7	B0	B1	B2	B3	B4	B5	B6	F6	DDB6	FDB6	or register with A
OUT (C)	ED79	ED41	ED49	ED51	ED59	ED61	ED69	—	—	—	—	output register
RES 0	CB87	CB80	CB81	CB82	CB83	CB84	CB85	CB86	—	DDCB.86	FDCB.86	reset bit 0
RES 1	CB8F	CB88	CB89	CB8A	CB8B	CB8C	CB8D	CB8E	—	DDCB.8E	FDCB.8E	reset bit 1
RES 2	CB97	CB90	CB91	CB92	CB93	CB94	CB95	CB96	—	DDCB.96	FDCB.96	reset bit 2
RES 3	CB9F	CB98	CB99	CB9A	CB9B	CB9C	CB9D	CB9E	—	DDCB.9E	FDCB.9E	reset bit 3
RES 4	CBA7	CBA0	CBA1	CBA2	CBA3	CBA4	CBA5	CBA6	—	DDCB.A6	FDCB.A6	reset bit 4
RES 5	CBAF	CBA8	CBA9	CBAA	CBAB	CBAE	CBAE	—	—	DDCB.AE	FDCB.AE	reset bit 5
RES 6	CB87	CB80	CB81	CB82	CB83	CB84	CB85	CB86	—	DDCB.B6	FDCB.B6	reset bit 6
RES 7	CB8F	CB88	CB89	CB8A	CB8B	CB8C	CB8D	CB8E	—	DDCB.BE	FDCB.BE	reset bit 7
RL	CB17	CB10	CB11	CB12	CB13	CB14	CB15	CB16	—	DDCB.16	FDCB.16	rotate left
RLC	CB07	CB00	CB01	CB02	CB03	CB04	CB05	CB06	—	DDCB.06	FDCB.06	rotate left circular
RR	CB1F	CB18	CB19	CB1A	CB1B	CB1C	CB1D	CB1E	—	DDCB.1E	FDCB.1E	rotate right
RRC	CB0F	CB08	CB09	CB0A	CB0B	CB0C	CB0D	CB0E	—	DDCB.0E	FDCB.0E	rotate right circular
SBC	9F	98	99	9A	9B	9C	9D	9E	DE	DD9E	FD9E	subtract register from A with borrow
SET 0	CB07	CB00	CB01	CB02	CB03	CB04	CB05	CB06	—	DDCB.C6	FDCB.C6	set bit 0
SET 1	CB0F	CB08	CB09	CB0A	CB0B	CB0C	CB0D	CB0E	—	DDCB.CE	FDCB.CE	set bit 1
SET 2	CB17	CB10	CB11	CB12	CB13	CB14	CB15	CB16	—	DDCB.D6	FDCB.D6	set bit 2
SET 3	CB1F	CB18	CB19	CB1A	CB1B	CB1C	CB1D	CB1E	—	DDCB.DE	FDCB.DE	set bit 3
SET 4	CB27	CB20	CB21	CB22	CB23	CB24	CB25	CB26	—	DDCB.E6	FDCB.E6	set bit 4
SET 5	CB2F	CB28	CB29	CB2A	CB2B	CB2C	CB2D	CB2E	—	DDCB.EE	FDCB.EE	set bit 5
SET 6	CB37	CB30	CB31	CB32	CB33	CB34	CB35	CB36	—	DDCB.F6	FDCB.F6	set bit 6
SET 7	CB3F	CB38	CB39	CB3A	CB3B	CB3C	CB3D	CB3E	—	DDCB.FE	FDCB.FE	set bit 7
SLA	CB27	CB20	CB21	CB22	CB23	CB24	CB25	CB26	—	DDCB.26	FDCB.26	shift left arithmetic
SRA	CB2F	CB28	CB29	CB2A	CB2B	CB2C	CB2D	CB2E	—	DDCB.2E	FDCB.2E	shift right arithmetic
SRL	CB37	CB30	CB31	CB32	CB33	CB34	CB35	CB36	—	DDCB.3E	FDCB.3E	shift right logical
SUB	97	90	91	92	93	94	95	96	D6	DD96	FD96	subtract register from A
XOR	AF	A8	A9	AA	AB	AC	AD	AE	EE	DDAE	FDAE	exclusive-or register with A

	(PSW,A)	(B,C)	(D,E)	(H,L)	SP	IX	IY	
ADD HL	—	09	19	29	39	—	—	add pair to HL
ADD IX	—	DD09	DD19	—	DD39	DD29	—	add pair to IX
ADD IY	—	FD09	FD19	—	FD39	—	FD29	add pair to IY
ADC HL	—	ED4A	ED5A	ED6A	ED7A	—	—	add pair to HL with carry
SBC HL	—	ED42	ED52	ED62	ED72	—	—	subtract pair from HL with borrow
DEC	—	08	18	28	38	DD2B	FD2B	decrement register pair
INC	—	03	13	23	33	DD23	FD23	increment register pair
LD A, (r)	—	0A	1A	7E	—	—	—	load A indirect
LD (r), A	—	02	12	77	—	—	—	store A indirect
LXI	—	01	11	21	31	DD21	FD21	load register pair immediate
POP	F1	C1	D1	E1	—	DDE1	FDE1	pop register pair from stack
PUSH	F5	C5	D5	E5	—	DDE5	FDE5	push register pair onto stack
LD r, (n)	—	ED4B	ED5B	2A	ED7B	DD2A	FD2A	load register pair from memory
LD (n), r	—	ED43	ED53	22	ED73	DD22	FD22	store register pair in memory

	Inc	Inc&rap.	Dec	Dec&rep.	
CP	EDA1	EDB1	EDA9	EDB9	compare, inc(dec) HL, dec BC
LD	EDA0	EDB0	EDA8	EDB8	load (DE) with (HL), inc(dec) HL and DE, dec BC
OUT	EDA3	EDB3	EDA8	EDB8	output (HL), inc(dec) HL, dec B
IN	EDA2	EDB2	EDAA	EDBA	input to (HL), inc(dec) HL, dec B

	0	1	2	3	4	5	6	7	
RST	C7	CF	D7	DF	E7	EF	F7	FF	restart call to location i*8

	Unc.	Zero/ Not Zero	Carry/ No Carry	Plus/ Minus	Even Parity/ Odd Parity	
CALL	CD	CC/C4	DC/D4	F4/FC	EC/E4	call subroutine if condition true
JP	C3	CA/C2	DA/D2	F2/FA	EA/E2	jump if condition true
JR	18	28/20	38/30	—	—	jump relative if condition true
RET	C9	C8/C0	D8/D0	F0/F8	E8/E0	return if condition true

CCF	3F	complement carry
CPL	2F	complement A (1's)
DAA	27	decimal adjust A
DI	F3	disable interrupts
DJNZ	10	decrement B, jump B≠0
EI	FB	enable interrupts
EX DE,HL	EB	exchange (D,E)&(H,L)
EX AF,AF'	08	exchange (A,F)&(A,F)'
EXX	D9	exchange (B,C,D,E,H,L) & (B',C',D',E',H',L)'
EX (SP),HL	E3	exchange (H,L) & top of stack
EX (SP),IX	DDE3	exchange IX & top of stack
EX (SP),IY	FDE3	exchange IY & top of stack
HALT	76	halt processor
IM0	ED46	interrupt mode 0
IM1	ED56	interrupt mode 1
IM2	ED5E	interrupt mode 2

IN	DB	input to A
JP (HL)	E9	jump to (HL)
JP (IX)	DDE9	jump to IX
JP (IY)	FDE9	jump to IY
NEG	ED44	complement A (2's)
NOP	00	no operation
OUT	D3	output from A
RETI	ED4D	return from interrupt
RETN	ED45	return for NMI interrupt
RLA	17	rotate A left thru carry
RRA	1F	rotate A right thru carry
RLCA	07	rotate A left circular
RRC	0F	rotate A right circular
RLD	ED6F	rotate left digit
RRD	ED67	rotate right digit
SCF	37	set carry flag

### Special load group, coded as LD source, destination:

A,I	ED57	A=I
A,R	ED5F	A=R
R,A	ED4F	R=A
I,A	ED47	I=A
(N),A	32	store A
A, (n)	3A	load A
SP, IX	DDF9	SP=IX
SP, IY	FD99	SP=IY
SP, HL	F9	SP=HL

instruction, these registers are updated. LDI and LDIR increment (D,E) and (H,L) after each move, and LDD and LDDR decrement (D,E) and (H,L) after each move. All four instructions decrement (B,C) after each move. The repeat instructions – LDIR and LDRR – continue to transfer data until (B,C)=0; the single-move group – LDI and LDD – transfer just one byte of data.

Assume you have two tables, TAB and TAB1. If each contains 100 bytes, this sequence transfers TAB to TAB1 (The actual transfer is performed by a single LDIR):

```
LD DE,TAB1 ;(D,E)=destination address
LD HL,TAB ;(H,L)=source address
LD BC,100 ;(B,C)=number of words
LDIR ; transfer the data
```

This sequence requires 11 memory bytes and requires 2095 clock cycles to execute LDIR. If you try to perform the same operation without LDIR, you must replace LDIR with

```
LOOP LD A,(DE) ; get one byte
LD (HL),A ; save it
INC DE ; update DE
INC HL ; update HL
DEC BC ; update BC
LD A,B ; test BC=0
OR C
JP NZ,LOOP ; continue to end
```

This sequence requires 5000 clock cycles for the move. Thus, for this example, the Z80 can perform the move 2.4 times as fast as the 8080 (assuming equal clock rates). The block transfer group can thus greatly speed program execution. LDIR can also set a given area of memory to a constant. If you want to set TAB to all zero, use

```
LD HL,TAB ;(H,L)=address of TAB
LD (HL),0 ; clear the first location
LD DE,TAB+1 ;(D,E)=address of TAB+1
LD BC,99 ;(B,C)=length-1
LDIR ; clear the table
```

This sequence copies the first location (set to zero) into the second, then copies the second (set to zero by the first copy) into the third, and so on.

What about LDI, LDD and LDDR? Use LDI or LDD if you want to manipulate the data as it is being transferred. Assume that you only want to transfer nonzero data from TAB to TAB1; because LDI doesn't alter the zero flag, you can perform the move as

```
LD DE,TAB1 ;(D,E)=destination address
LD HL,TAB ;(H,L)=source address
LD BC,100 ;(B,C)=number of transfers
LOOP LD A,(HL) ; set zero flag if (H,L)=0
OR A
LDIR ; transfer one byte
JP NZ,LOOP1 ; if data was not zero, repeat
DEC DE ; erase last move
LOOP1 JP PE,LOOP ; jump if (B,C) nonzero
```

Notice that LDI sets the parity flag when (B,C) is nonzero. Also remember that DEC DE won't alter the flags.

The two decrement block transfers – LDD and LDDR – move overlapping data. If TAB and TAB1 are organized in memory as shown in Fig 2, you can't use LDI or LDIR to move the data from TAB to TAB1. If you did, the last locations of TAB1 would be erroneously set to the same value as the first locations. On the other hand, LDD or LDDR

won't destroy the last locations of TAB until after they're transferred. When would you require overlapping tables? Most commonly when the microprocessor must buffer data. In that case you may want to open the buffer, by copying the end data, to allow insertion of new data.

For the block-search instructions – CPI, CPIR, CPD, CPDR – you must preset the registers this way:

```
(H,L) = address of the area to search
(B,C) = length of the search area
A = data to be found
```

The repeat versions – CPIR or CPDR – repeat until (B,C)=0 or until the desired data is located. If you have a table – TAB – that contains one-byte entries, the following sequence locates an item (contained in the accumulator) in the table. It jumps to ERROR if the item is not in the table and returns to the calling program if it finds the item:

```
FIND LD HL,TAB ;(H,L)=address of TAB
LD BC,2144 ;(B,C)=table length
CPIR ; search
RET Z ; return if found (Z flag set)
JP ERROR ; jump to error routine
```

To make effective use of the block-search instructions, you must organize tables properly. Because (H,L) is incremented by one after each search, it isn't convenient to organize tables horizontally, so that every byte of the entry

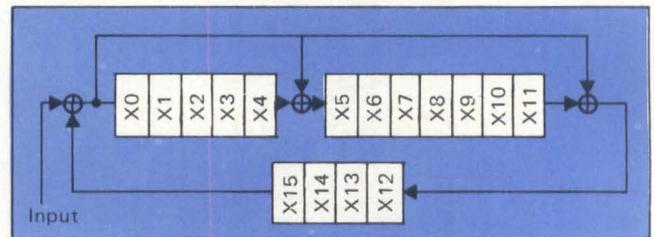


Fig 6 Feedback shift register serves IBM's SDLC protocol; it provides several parity bits for use in checks of transmitted data.

is sequential (Fig 3). If you want to locate an entry associated with a specific key, and each entry contains three bytes, modify the search program this way:

```
FIND LD HL,TAB ;(H,L)=address of TAB
LD BC,2144 ;(B,C)=table length
FIND1 CPI ; search one entry
RET Z ; return if found
INC HL ; advance to next entry
INC HL
JP PE,FIND1 ; continue till (B,C)=0
JP ERROR ; data not found
```

The memory penalty for this modification is small, but the time penalty is large. The original search requires 21 cycles; this one requires 43 cycles. How can you avoid the penalty? One way is to reorganize the table. Instead of placing each byte of each entry in sequence, put all of the first bytes first, then all of the second bytes, then all of the third bytes (Fig 4). Such a vertically organized table lets you use the original search program. To obtain the other two bytes of the entry, execute this sequence after the entry has been found:

```
LD BC,2144 ;(B,C)=table length
ADD HL,BC ;(H,L)=address of byte two
LD D,(HL) ; D=byte two
ADD HL,BC ;(H,L)=address of byte three
LD E,(HL) ; E=byte three
```

The sequence puts Bytes Two and Three of the table entry into the registers (D,E).

### relative addressing

If I had to name the single most important group of improvements in the Z80, the relative address jumps would definitely win the title; the six instructions in this group — JR, JR C, JR NC, JR Z, JR NZ, DJNZ — are more effective in reducing program size than any other group. The examples I've presented so far use normal jump instructions, but most of those instructions could be replaced by the relative address version and save one byte per jump. Alas, the relative address versions have one drawback — a relative address jump takes more time to execute than the normal jump if the condition is met and the jump is performed. For example, JP takes 10 cycles and JR takes 12. This 20% increase in processor time may be significant in some routines, especially subroutines that handle interrupts. In those cases it may be wise to use the extra byte of memory to save the processor time. As usual you're faced with an application-dependent memory/time tradeoff.

One of the relative jumps — DJNZ — deserves further examination; it's particularly useful for controlling loops. Each time it is executed the B register is decremented by one, and if B is not zero after the decrement, the jump is performed. For example, this loop is executed 22 times:

```

LD B,22 ; B=loop count
LOOP .
.
.
DJNZ LOOP-$ ; continue till B=0

```

DJNZ can often replace a 2-instruction sequence — DEC, JP. This saves one byte of memory and 3 processor cycles each time it is executed — a significant savings for large loop counts.

### arithmetic manipulations with shifts

The shift repertoire for the Z80 has been greatly expanded; not only does the microprocessor allow more types of shifts, but any register — not just the accumulator — can be shifted. For example, the sequence

```
SLA D ; shift register D left
```

replaces this common 8080 sequence:

```

LD A,D ; A=D
OR A ; clear carry
RLA ; shift A left
LD D,A ; put answer back in D

```

One immediate advantage of this capability is the ability to create a multi-word shift. For example, this sequence shifts the (H,L) pair left one bit (zero fill):

```

SLA L ; shift L left, 0 fill
RL H ; shift H left, carry fill

```

Though it illustrates the concept, it's a poor example because the approach I outlined in November is still faster and uses less memory:

```
ADD HL,HL ; shift HL left, 0 fill
```

I chose this example to illustrate a point: DON'T AUTOMATICALLY DISCARD AN OLD CONCEPT JUST BECAUSE YOU HAVE A FEW NEW FLASHY INSTRUCTIONS TO PLAY WITH. The flashy approach may not be the best one. On the other hand, if you want to right shift (H,L) by one,

### Listing 1. General-Purpose, High-Precision Multiply Routine

```

MULT LD B,LEN ; B=length of numbers
LD IX,ANSW ; clear the answer
MULT1 LD (IX+0),0 ; clear one byte
INC IX ; advance to the next byte
DJNZ MULT1-$ ; continue till all bytes cleared
MULT2 LD B,LEN-1 ; shift the first operand right—
; zero fill
LD IX,NUM1
SRL (IX+0)
MULT3 INC IX ; advance to next byte - does not
; change CY
RR (IX+0) ; shift next byte
DJNZ MULT3-$ ; continue till all bytes shifted -
; doesn't affect CY
JR NC,MULT5-$ ; skip partial product add if no
; carry
LD B,LEN ; set ANSW=ANSW+NUM2
LD IX, ; both indexes start at the end
; NUM2+LEN-1 of the number
LD IY,
; ANSW+LEN-1
CCF ; clear carry (it was set, so
; complement it)
MULT4 LD A,(IY+0) ; add corresponding bytes
ADC (IX+0)
LD (IY+0),A
DEC IX ; advance to the next bytes
DEC IY
DJNZ MULT4
MULT5 LD B,LEN ; shift the second operand left
; by one - zero fill
LD IX,
; NUM2+LEN-1 ; index from the end
XOR A ; be sure carry is cleared
MULT6 RL (IX+0) ; rotate one byte
DEC IX ; advance to next byte
DJNZ MULT6-$ ; continue till done
LD B,LEN ; if NUM1=0, we are done
LD IX,NUM1
MULT7 OR (IX+0) ; or all bytes together (A was
; zero at start)
DJNZ MULT7-$
JR NZ,MULT2-$ ; continue the multiply
RET

```

the new approach is the *only* one:

```

SRA H ; shift H right, 0 fill
RR L ; shift L right, carry fill

```

Remembering the shift mnemonics might be difficult, but the guidelines are straightforward. Those that start with 'S' are shifts, and the vacated bit is filled with zero (SLA, SRL) or the previous sign (SRA). Those that start with 'R' are rotates, and the vacated bit is filled with carry (RL,RR) or the bit shifted out of the register (RLC,RRC). In all cases the bit shifted out of the register goes into the carry flag. Finally, the special rotates that end in 'A' modify the accumulator (RLCA, RRCA, RLA, RRA) and require only a

one-byte opcode. In addition, the accumulator shifts — which are the same ones offered by the 8080 — affect the carry but not the other flags; all other shifts affect all flags. Thus, these two accumulator shifts are different because the first uses only one byte, and only changes carry, whereas the second uses two bytes and changes all flags:

```
RLCA          ; rotate A left
RLC  A        ; rotate A left (set flags)
```

One particularly good use of the extended shift repertoire lies in the creation of a multiply routine. The following routine calculates  $(H,L)=(B,C)*(D,E)$ :

```
MULT  LD  HL,0          ; reset the answer to zero
MLOOP SRL B            ; shift (B,C) right - zero fill
      RR  C
      JR  NC,NOA-$      ; skip the partial product add
                          ; if no carry
      ADD HL,DE         ; (H,L)=(H,L)+(D,E)
NOA   EX  HL,DE         ; shift (D,E) left by one — use and
      ADD HL,HL
      EX  HL,DE
      LD  A,B           ; if (B,C)=0 we are done
      OR  C
      JR  NZ,MLOOP-$   ; continue till done
      RET              ; exit
```

This routine resembles the one offered by Zilog in its manual, but it's faster, because it terminates the multiply when  $(B,C)=0$  rather than just going through the loop 16 times. For small numbers, say  $161*33$ , this results in an order-of-magnitude speed increase.

This routine also doesn't check for overflow — answers could be more than 16 bits long. One last note: The relative address jumps must have the displacement in the operand field — the assembler refuses to calculate it for you, as you would expect. Thus, you must write 'X-\$' to generate a transfer to X. This is a rather silly restriction, but you must live with it.

If you examine the Z80's opcodes carefully you'll notice that you can shift memory locations relative to IX or IY. For example,

```
SLA  (IY+2)
```

shifts the memory location  $(IY+2)$ . Using this type of shift, you can create a general-purpose high-precision multiply. The routine in Listing 1 multiplies two numbers (NUM1, NUM2) and puts the answer in ANSW. The numbers can be any number of bytes long, but all three of them are the same length. Again I'll ignore overflow, but you could easily include that check also. In this version, the length of the numbers is set by the assembly language constant LEN, but you could pass the length as one more parameter.

The routine in Listing 1 may be slow, but it can multiply 64 bits just like the big machines. It can even do more than 64 — if you have the time.

Recall the algorithm for calculating Sin/Cos that I discussed in December; it relied heavily on shift operations. The multi-precision shifting approach I've just outlined could be used with that algorithm to create very high-accuracy Sin/Cos routines. If you want to duplicate the precision of the better calculators by using the CORDIC algorithm, which I also discussed in December, you would

need about a 60-bit shift.

What else can you do with shifts? Another area where shift algorithms find use is in error correct schemes. In one simple error detection scheme — parity — a single bit is added to the data so that the total number of one-bits is either even (even parity) or odd (odd parity). If the resulting data is then transmitted or stored and later retrieved and its parity isn't correct, a transmission error has occurred. You can expand the parity check concept to provide a more substantial data check. Instead of adding a single parity bit, add several by using a feedback shift register. The one in Fig 6 serves the IBM SDLC data convention; here's how it works. The register is initially set to zero. When a character is transferred, it is simultaneously shifted into the accumulator. After all of the characters are transferred, the accumulator's contents (the cyclic redundancy check character) go to the receiver, where they are used to determine correctness of the data. The receiver simultaneously receives the data and shifts it into another accumulator (constructed just like the one used to transmit). After all data, including the CRC, has arrived, the accumulator can detect and correct errors. Correction is slightly complicated, but detection is easy: If the accumulator contains zero, no errors occurred.

How can you implement this or any other feedback shift network in software? Emulation of the hardware (shift by one and exclusive-OR as appropriate) is one way, albeit a time consuming one. Another way, more complicated but worth the extra effort, is to analyze the accumulator and determine an equation for what it contains after all shifts have occurred. Assume you're dealing with 8-bit characters. After one shift, the accumulator contains  $(B7-B0)$  is the input character,  $(X15-X0)$  the old accumulator):

$$\begin{array}{l} X_{14} X_{13} X_{12} (X_{11}+X_{15}+B_7) X_{10} X_9 X_8 X_7 X_6 X_5 \\ \underline{-(X_4+X_{15}+B_7) X_3 X_2 X_1 X_0 (X_{15}+B_7)} \end{array}$$

All + signs, of course, signify exclusive ORs. If you continue this analysis, you'll create a terribly complicated mess. Notice that at each step, the common term  $(X_{15}+B_i)$  is used to calculate three of the bits. If you use  $Y_i$  to represent this common term, you obtain for the first step:

$$\begin{array}{l} X_{14} X_{13} X_{12} (X_{11}+Y_7) X_{10} X_9 X_8 X_7 X_6 X_5 (X_4+Y_7) \\ \underline{-X_3 X_2 X_1 X_0 (Y_7)} \end{array}$$

where

$$Y_7 = X_{15}+B_7$$

If you continue the analysis, you'll obtain the contents of the accumulator after all eight shifts:

$$\begin{array}{l} X_7+Y_3, X_6+Y_2, X_5+Y_1, X_4+Y_0+Y_7, X_3+Y_6, X_2+Y_5, X_1+Y_4, \\ \underline{-X_0+Y_3, Y_7+Y_2, Y_6+Y_1, Y_5+Y_0, Y_4, Y_3, Y_2, Y_1, Y_0} \end{array}$$

where

$$Y_7 = X_{15}+B_7$$

$$Y_6 = X_{14}+B_6$$

$$Y_5 = X_{13}+B_5$$

$$Y_4 = X_{12}+B_4$$

$$Y_3 = X_{11}+B_3+Y_7$$

$$Y_2 = X_{10}+B_2+Y_6$$

$$Y_1 = X_9+B_1+Y_5$$

$$Y_0 = X_8+B_0+Y_4$$

What can you do with this information? Try rewriting the equations in terms of 16-bit computer words;  $X_{15}$  to  $X_0$  is

one computer word. The exclusive ORs become

```
X7 X6 X5 X4 X3 X2 X1 X0 - - - - -
Y3 Y2 Y1 Y0 - - - - -
- - - Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0 - - - - -
- - - - - Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0
```

Finally, light appears at the end of the tunnel. You've reduced the 8-bit feedback shift to three 16-bit exclusive ORs. The same analysis works for any feedback shift. To implement the reduced equations, use the program in Listing 2. The (H,L) pair serves as the accumulator, and the character lies in the accumulator. Clear (H,L) the first time you call the routine.

**Listing 2. Routine For Implementing A Feedback Shift Network**

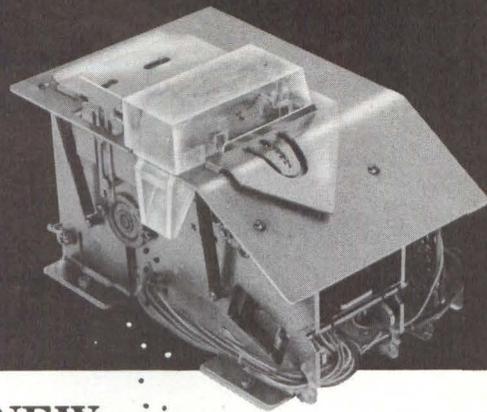
```
XOR H ; calculate Y7-Y0
LD B,A
RRA
RRA
RRA
RRA
RRA
XOR B
LD B,A ; B=Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0
RRCA
RRCA
RRCA
LD C,A ; C=Y2 Y1 Y0 Y7 Y6 Y5 Y4 Y3
AND 1FH
LD D,A ; D= - - - Y7 Y6 Y5 Y4 Y3
LD A,C
RRCA
AND OFOH ; A=Y3 Y2 Y1 Y0 - - - -
XOR D ; A=Y3 Y2 Y1 Y0+Y7 Y6 Y5
Y4 Y3

XOR L
LD H,A ; H=upper bits of new accumulator
LD A,C
AND OE0H ; A=Y2 Y1 Y0
XOR B
LD L,A ; L=lower bits of new accumulator
```

If you want more information on CRC generation, try these three references. The Lin text is the most readable, but most experts consider the Peterson reference the authoritative source:

W. W. Peterson, *Error Correcting Codes*, MIT Press, Cambridge, MA.  
 S. Lin, *An Introduction to Error Correcting Codes*, Prentice Hall, Englewood Cliffs, NJ.  
 K. Helness, "Implementation of a Parallel Cyclic Redundancy Check Generator," *Computer Design*, March 1974.

*Next month, Dollhoff will conclude his exploration of microprocessor software optimization with a discussion of the National Semiconductor SC/MP and the Electronic Arrays EA9002.* ♦



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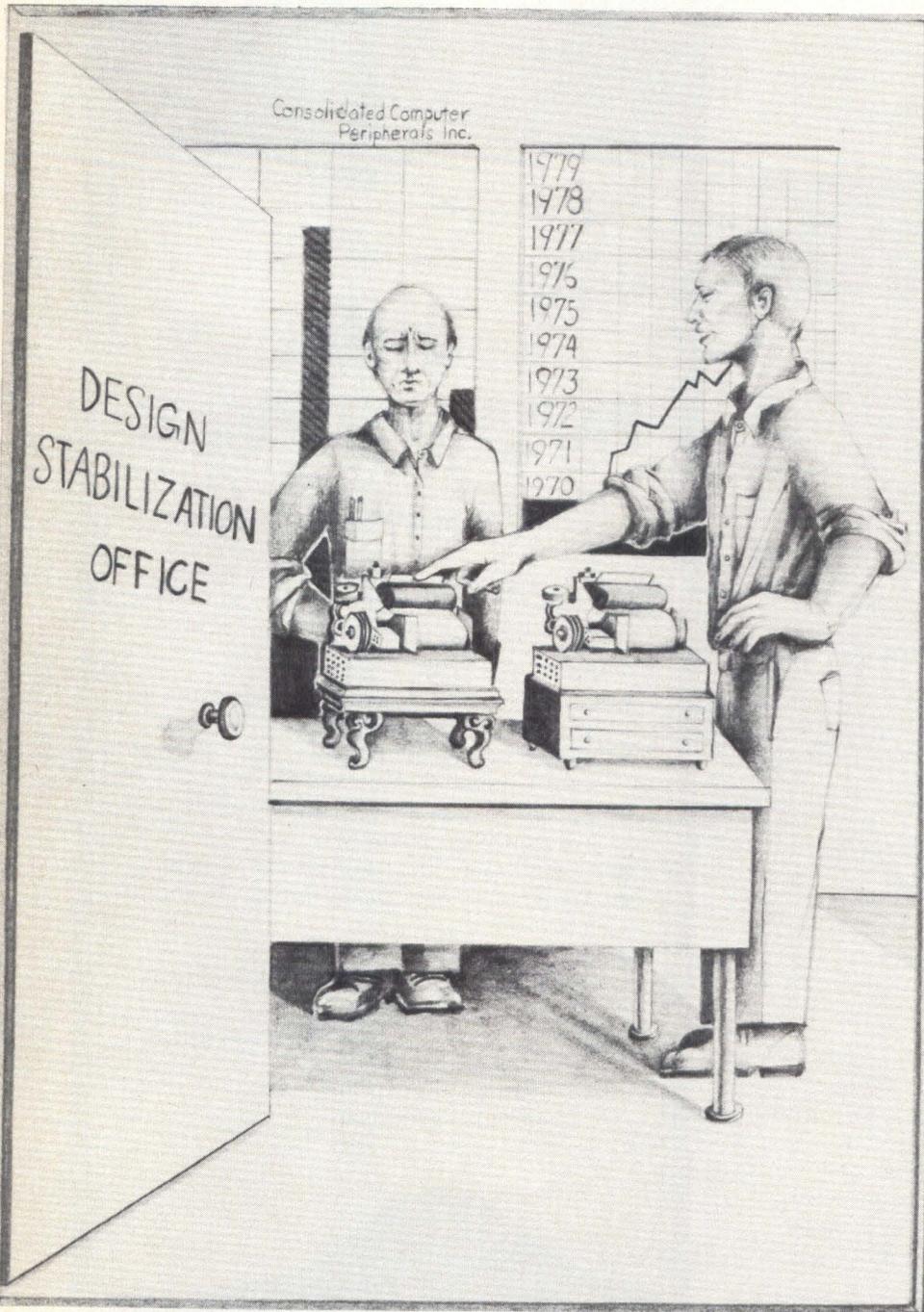
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CIRCLE 33

# DESIGNING SYSTEM



## PERFORMANCE, PRICE AND PACKAGING POSE TOUGH PROBLEMS FOR POTENTIAL "HOME-COMPUTER" PERIPHERALS DESIGNERS

Most designers no longer doubt that microcomputers will appear in an increasingly wide range of future industrial and scientific instrumentation and control devices — systems that formerly would have utilized hardwired logic. And with the growth of computer games and hobby-computer kits, such microcomputers have now also begun appearing in consumer applications.

This second, consumer oriented phase of the microprocessor revolution has just recently arrived. Most current home-computer systems are hobby systems, assembled from kits by persons versed in computer techniques — much as some stereo enthusiasts assemble hi-fi systems from audio components. But by the end of this year, according to Venture Development Corp. (VDC), preassembled computer systems will appear. Analogous to the prepackaged stereo sets now sold to enthusiasts more interested in using entertainment systems than in building them, these "home computers" will serve users less sophisticated than today's computer hobbyists.

The market for "home computers" will double every year thereafter, at least through the early 1980s, projects Alan Kaplan, senior consultant at the Wellesley, MA, firm and author of the firm's recent study, *The Home Computer*. He explains that VDC has had contact with at least three manufacturers — a consumer electronics firm, a hobby-computer maker and a manufacturer of traditional mini- and microcomputers — each of which is "quite serious" about introducing a "home computer" by the end of this year. Both consumer-electronics stores and general merchandisers will distribute these planned "home computer" systems.

# CONSUMER PERIPHERALS

The burgeoning hobby-computer market and the potentially larger market for "home computers" will each generate continued demand for computer peripherals. According to the VDC study, a questionnaire mailed to over 1200 home-computer users (mostly hobbyists) yielded this data on current standard-peripheral use in home systems in mid-1976:

Peripheral	Percentage of Respondents		
	Now Have	Plan to Add in One Year	No Plans
Floppy	38.7*	—	61.3
Keyboard Entry	89.0	9.7	0.3
CRT/Video	64.5	29.0	6.5
Cassette	59.7	19.3	21.0
Paper Tape**	40.3	9.7	50.0
Printer	22.6	14.5	62.9

\* Also includes respondents who plan to add in one year or less  
 \*\* Reader and/or punch

And the accompanying pie charts show how the hobbyist's dollar

was apportioned among the standard peripherals last year, and how VDC expects sales in the hobby market (excluding "home computers") for standard peripherals to divide up in 1981.

A key trend highlighted in the VDC study focuses on greater systems integration in home-computer peripherals; more users, especially buyers of "home computers," will favor systems with built-in peripherals. Hobbyists, on the other hand, will continue to buy peripherals as components.

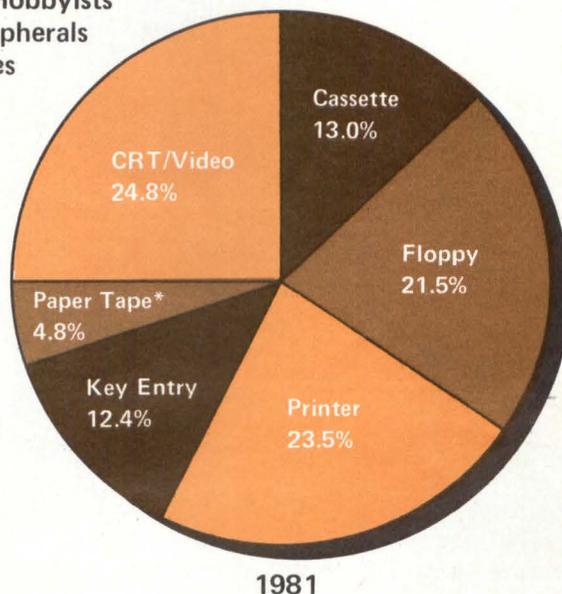
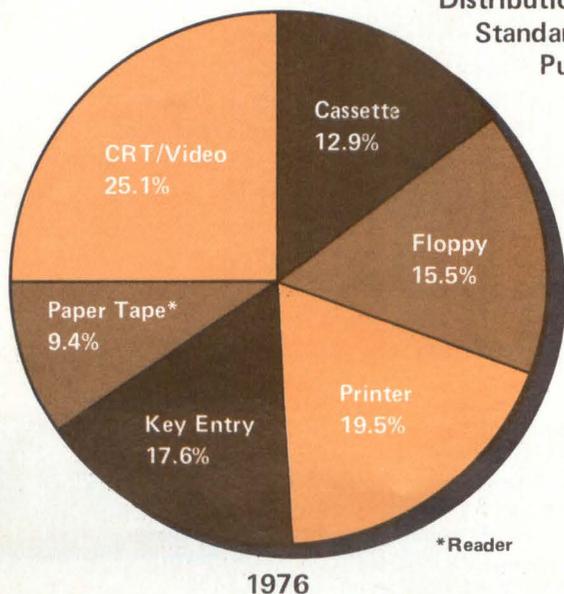
Says Kaplan: "For hobbyists, price is overwhelmingly the most important factor, much more so than it would be in the commercial area." Hobbyists are more concerned with low mean time to repair than are commercial users of peripherals; those users stress high reliability — reflected by high mean time before failure. Thus, he says, manufacturers and designers of peripherals slated for the hobby-computer market will do well to develop their systems with such factors in mind.

What other factors influence the design of peripherals for hobby-computer systems? What performance requirements will designers of "home computer" systems specify for the peripherals they integrate into those systems? How can peripherals designers best meet these requirements?

The design case-histories that follow attempt to answer some of these questions; you'll read in them of the design goals that governed the development of three peripheral systems aimed specifically at hobby-computer applications. If you're a designer of similar hobby-computer peripherals, read how some of your colleagues met their design goals, and apply their expertise to the solution of your problems. And if you're a designer of a potential "home computer" system, read about the capabilities of some of the peripherals you may want to specify for use in that system.

Jordan Backler  
 Managing Editor

Distribution of Hobbyists' Standard-Peripherals Purchases



Source: Venture Development Corp.

# DESIGNING CONSUMER- SYSTEM PERIPHERALS

## INTELLIGENT-TERMINAL DESIGNERS OPT FOR 8080-COMPATIBLE CIRCUITRY

by Lee Felsenstein and Robert Marsh

Because the "home computer" serves a consumer market, both it and the peripherals designed for use with it must exhibit high-volume production and adequate customer support. With these fundamental requirements in mind, we designed the Sol product line to simultaneously meet the needs of two applications. Both Sol-10 and Sol-20 function as intelligent terminals—each unit lacks only a CRT monitor. Additionally, Sol-20 incorporates a power supply and expansion chassis, which with adequate memory allow it to operate as a stand-alone computer. And the system's basic electronics, housed on one board and designated Sol-PC, serves OEM applications that require a single-board computer.

To provide Sol with the required customer support, we developed Basic and Focal language packages as well as application and game programs. We also developed two ROM-resident programs—Solos, which optimizes Sol-20 functions for stand-alone computer applications, and Soled, which implements the functions of an intelligent terminal on either Sol-10 or Sol-20.

*Lee Felsenstein is the founder of LGC Engineering, Berkeley, CA, and a consultant to Processor Technology, Emeryville, CA. Robert Marsh is vice president of Processor Technology.*

All of these actions hinged on one major development in the hobby-computer market. Within the past year, several peripheral-interface and memory kits have appeared, each of which utilizes the "hobbyist," or S-100, bus structure used in several 8080-based computers. To take advantage of such kits, we decided to design the Sol family around this same S-100 bus structure. In essence, Sol is the combination of a microprocessor circuit with several S-100 peripheral modules.

### implementing the design

As initially conceived by one of us (Marsh), Sol consists of a typewriter-sized cabinet on whose flat top a video monitor can rest (Fig 1). One 10" x 16" PC card contains all electronics except the unit's keyboard and power supply, and the video signal generated by the device serves any EIA-standard monitor. A PC edge connector on the board accepts a backplane daughter board that holds as many as five S-100 cards. All I/O connectors, also available on the rear edge of the PC card, are accessible from the cabinet's rear.

To implement this basic structure (Fig 2), we buffered the system's 8080 address and data lines to the circuit and bus connector through tri-state drivers, much as do other S-100-type processors. Next, we paralleled two unidirectional data buses to form a bidirectional bus and thereby eliminated the need to run eight additional lines around what promised and proved to be a very crowded card. We also connected a 4-input multiplexer to select data input to the processor from the keyboard port, the parallel port and an internal data bus, as well as from the external data bus.

We created the internal bus as a unidirectional circuit for low-drive, on-card memory and I/O devices that cannot meet the heavy drive requirement of the full external data bus; it allows maximum utilization of the tri-state capabilities of the universal asynchronous receiver/transmitters (UARTs) used in the serial and tape channels. The flag and status outputs of these devices arrive in parallel at the 8080 chip; port addresses from the board's address decoder section enable the outputs. The decoder also controls the multiplexer's switching; default direction comes from the system's external bus. We defined the 4K bytes of memory in Page C (high-order hex digit of the address) as on-card memory, divided between 2K of ROM, 1K of RAM and 1K of

**Fig 1** Housed in a typewriter-sized cabinet on which a CRT monitor can sit, Sol-20 contains all circuitry necessary to function either as an intelligent terminal or a stand-alone computer. The system's designers chose to configure it around the "hobbyist," or S-100, bus structure used in several 8080-based computers; Sol is basically the combination of several S-100 peripheral modules with a microprocessor circuit.



“visible RAM” in the video display circuit.

The display section treats its RAM as 2-port memory; the processor has the highest priority. We placed the second port under control of the screen refresh circuitry, which calls up data as required for conversion by the character-generator ROM into video signals for display. We didn't connect the video display section to the internal bus because we felt we had to allow for its being loaded directly from an external DMA device, which can gain control of the data bus but

“crash” conditions to which previous S-100 processors are prone. An R-C charge-up network provides automatic power-up reset sequencing of the processor.

The 8080 initializes with its program counter at 0000, but much software currently in use, as well as the vectored interrupt instruction subset in the 8080, requires the location of RAM at Page 0. To allow for temporary relocation of ROM to Page 0 during the first four fetches after reset, we configured a “phantom” circuit, which provides a signal to a

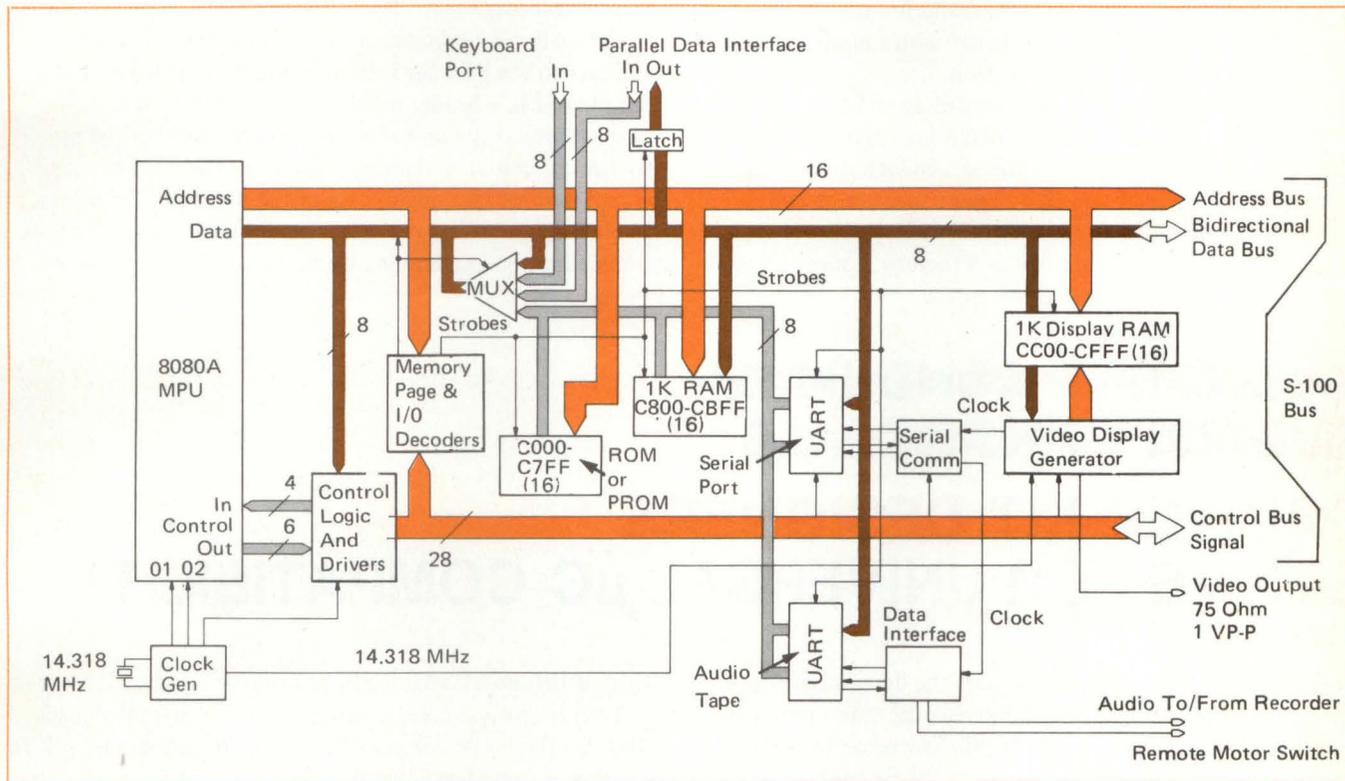


Fig 2 The internal bus in the Sol circuitry functions as a unidirectional circuit for low-drive, on-card memory and I/O devices that can't meet the drive requirement of the system's full external data bus.

not the internal bus. We made the data bus the source of all data fed to memory and I/O, both on-card and off; the only other data input to the processor from on-card circuitry through the data bus comes from the sense switches, an 8-wide DIP array that lets the CPU sense an alterable parameter byte under program control through input port FF.

We derived board timing from a 14.31818-MHz crystal oscillator; the frequency, four times that of the NTSC color burst, provides compatibility with color video graphics devices. This “dot clock” goes to an external connector and feeds the output shift register and character divider of the video display section as well as the 8080 clock divider. We configured the clock circuit using MSI and SSI TTL chips rather than the Intel 8224 LSI chip to allow for several selectable microprocessor clock rates; that way, we can retrofit higher-speed processor chips into the same board. When designing the clock, we took care to ensure non-overlapping phases and used a switch-tail ring counter to eliminate ambiguous states during clocking. An AH 0026 dual MOS clock-driver chip feeds the 8080.

The circuitry synchronizes all control inputs to the 8080 with the clock and forces a “wait state” immediately after the reset condition; these two techniques help eliminate

It allows Sol to fully utilize the tri-state capabilities of the UARTs used in the intelligent-terminal system's serial-interface and tape-interface channels.

bus pin during that period; the memory-page decoder consists of exclusive ORs that respond to C or 0 depending on the state of this circuit. The first instruction in the ROM is always a NOP, followed by a Jump to the first page of C000, so when the “phantom” signal ceases the program counter is set to the location in ROM where it will next appear.

We placed the ROM on a 1.75" x 3.5" plug-in personality module card that fits into a 30-pin edge connector at the rear of the unit. Originally implemented to allow for multiple EPROM sourcing, this connection method also lets unskilled users interchange monitor firmware without removing the cabinet.

### interfaces

Sol's parallel interface circuit follows the model of the hobbyist standard proposed by Harold Mauch of Percom, Inc. Because this standard calls for a minimum strobe width of 1  $\mu$ s for interfacing to MOS logic, we inserted a wait state in all I/O operations to widen their strobes. The video display also requires a wait state to allow for settling of the 2-port address multiplexers, so we decided to insert one wait state in all on-card memory references. The insertion allows the use of higher-speed 8080 chips without requiring re-

placement of on-card memory. High-speed access still occurs to all off-card memory that resides on the bus.

The serial interface drives its baud clock from a 1200-Hz signal extracted from a divider in the video display section. A 153.6-kHz signal locks to this lower frequency through a CMOS 4046 phase-locked loop that works through a 4024 CMOS divider; the divider's outputs provide clocks for all rates between 75 and 9600 baud, except 110 baud. For that rate, a 4029 CMOS programmable counter performs a divide-by-eleven on a 19.2-kHz signal and produces a 109-baud clock. The outputs of the divider also function as timing signals in the tape interface section.

The tape interface allows data recording at 1200 baud on audio cassettes or other audio media; it uses Manchester or phase encoding with a bit-cell time of 1667  $\mu$ s. In response to suggestions originally made by Don Lancaster of Synergetics, the interface feeds a UART with a clock that is phase-locked to the incoming data rate and thereby assures recov-

ery of the data independent of real-time distortion introduced by tape-speed variation over the lock range of the loop. Automatic gain control provides another necessary dimension of adaptability. This recording and recovery method, termed CUTS (Computer Users Tape Standard), represents a refinement of the "Kansas City" or "Byte" standard defined in 1975. The audio tape interface is software-switchable between these two standards, and two motor-control relays on the Sol board replace the switches of the usual low-cost cassette recorder.

The system's keyboard, a custom unit from Key Tronic, connects to the PC board through a ribbon cable connector that plugs into a header soldered to the board. A capacitance crossbar-type unit that uses no LSI encoder and no mechanical contacts, the unit has a key assembly that can be removed for cleaning in case of the dreaded "Coke Test." A combination of "upper case" and "repeat" keys performs a reset function and eliminates the need for a reset switch.

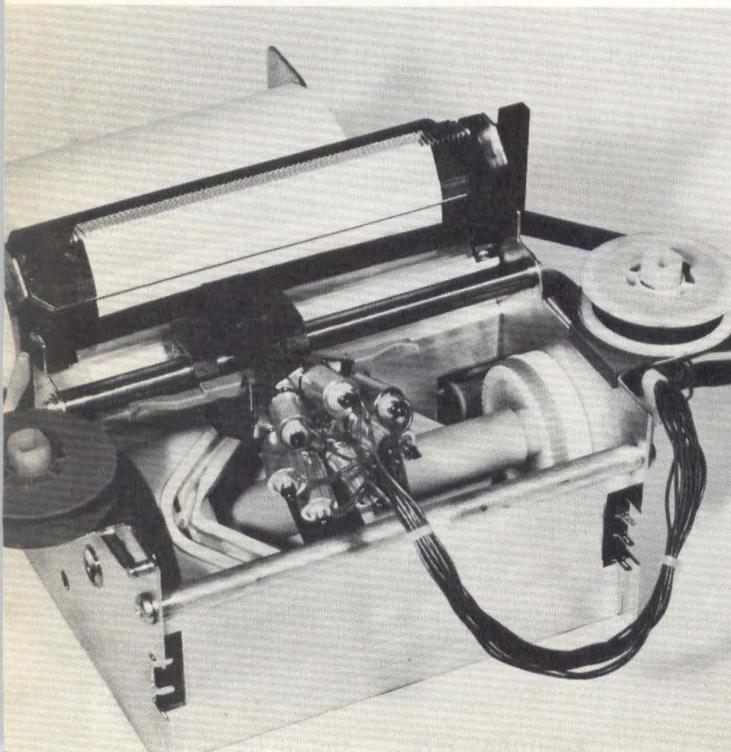
## DESIGNING CONSUMER- SYSTEM PERIPHERALS

# PRINTER-KIT DESIGNERS STRIVE FOR UNIVERSAL $\mu$ C COMPATIBILITY

by Gary Kay

As home-computer use grows, so does the demand for low-cost printers. Although many hobbyists use video terminals for I/O because of their comparatively low price, low operation cost and silent operation, many of these same users also require a hardcopy capability for listing important data and programs—it's awfully difficult to debug a long program

*Gary Kay is a project engineer at Southwest Technical Products Corp., San Antonio, TX.*



without the use of a hardcopy printout.

Teletypewriters constitute one source of hardcopy capability for the home-computer user, but the late-model ASCII versions of these terminals are relatively expensive, while the older Baudot versions have limited character sets and lack code compatibility. Furthermore, both types of teletypewriter are bulky and noisy.

Searching for low-cost alternatives to these printer systems, we quickly eliminated expensive 80-column mechanisms and focused on the printers used in point-of-sale (POS) terminals. But many of these smaller POS printers are also expensive, and most of them print less than 20 char./line — a length insufficient to accommodate hobbyists' program listings.

One unit met our cost and mechanical requirements, however. Manufactured by LRC, Riverton, WY, and distributed by C. Itoh, New York City, the 40-column, 5x7 impact dot matrix printer outputs 75 lpm and incorporates a printhead similar to the devices used in Centronics Model 101 printers (Fig 1).

A rotating cylinder, measuring slightly longer than the head's printing width on the paper and housed below the head, moves the head across the paper at a constant velocity (except at the extreme ends of the head's motion, where no printing occurs). Rotated by a synchronous ac motor

**Fig 1** Printer used in the kit outputs 40-column lines at 75 lpm. Manufactured by LRC Corp. and distributed by C. Itoh Corp., it requires no head-positioning circuitry and thereby simplifies the requirements placed on its driver electronics.

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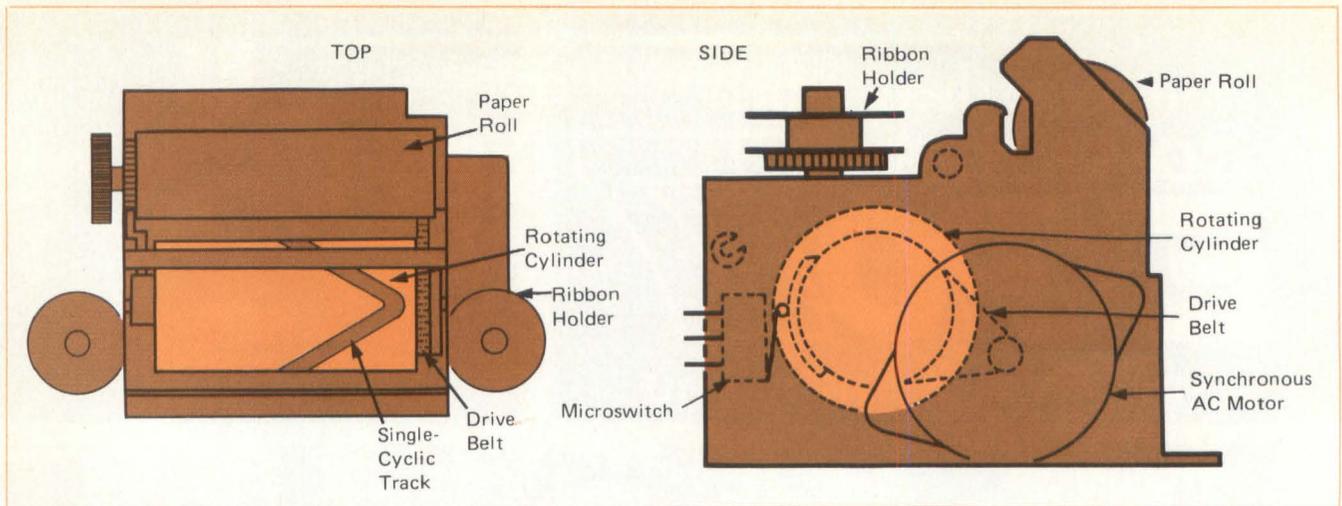


Fig 2 Printhead-motion generator incorporates a cylinder that makes one rotation for each line the printer outputs. A projection

coupled to it by a ribbed nylon drive belt, the cylinder makes one revolution for each line the printer outputs. A uniform, single-cyclic, zig-zag track on the cylinder's surface runs from the cylinder's left side to its right side and back to the left; a projection on the printhead rides in this track, and as the cylinder rotates, the printhead moves back and forth across the paper (Fig 2).

Because it requires no head-positioning circuitry, this motion-generation scheme greatly simplified the requirements placed on the electronics we designed to drive the printer. That circuitry senses the printhead's "start of line" position through a microswitch actuated by a cam attached to the cylinder's right side. The printer also incorporates an

in the printhead rides in a single-cyclic zig-zag track on the cylinder and moves the printhead back and forth across the paper.

eccentric-cam-driven pawl arm, mounted on the cylinder's left side, that advances the paper one line for each cylinder revolution.

### design goal: universal compatibility

In designing all of our peripheral systems, which include kits for video terminals, graphics terminals and audio cassette interfaces as well as a kit for the PR-40 printer system, we attempt to achieve compatibility with any minicomputer or microcomputer equipped with accessible serial or parallel interfaces. We feel that a peripheral should have a minimum amount of power, memory, data bus and software dependence on its host computer; it should interface with the

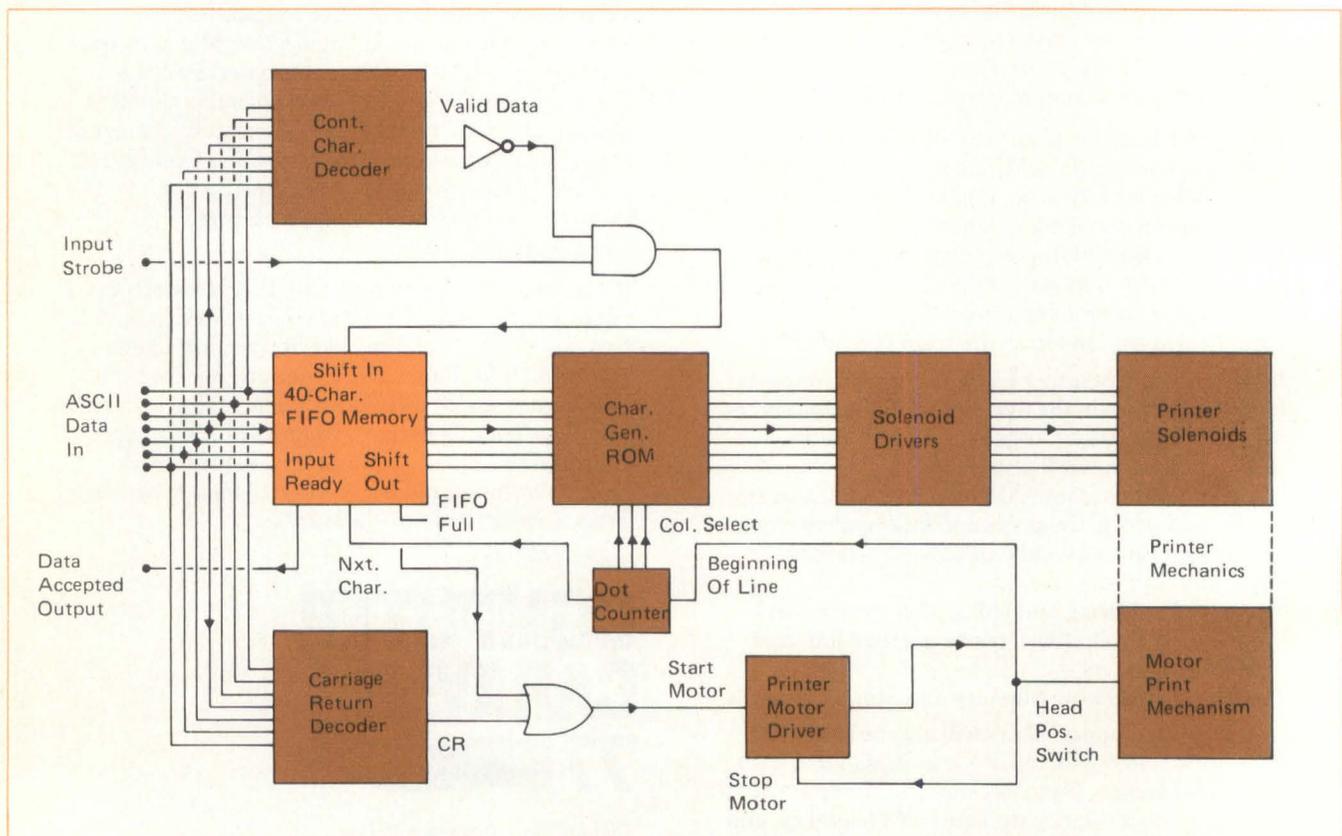
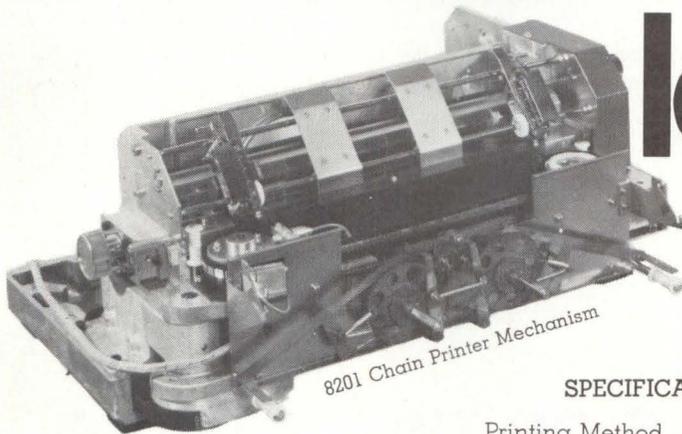


Fig 3 Driver electronics for the printer kit reflects its designers' goal of making the system as independent of its host as possible. To

simplify the host's software and timing overheads, the circuitry stores one line of character data in a FIFO buffer memory.

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host either through RS 232 or TTY serial circuitry or an 8-bit parallel link.

This approach lets the peripheral's user attach it to a variety of hosts and doesn't preclude future host-computer upgrades. By contrast, many peripherals designers now configure systems compatible with the Mits Altair bus, an approach that limits future upgrades to 8080-type bus structures. But given today's rate of technological development, what are the chances that this bus structure will remain the most popular approach? And what can users do with such dedicated, plug-on peripherals if they wish to switch to a 16-bit number-crunching microcomputer or a non-8080 type 8-bit unit?

Starting with this constraint of making the \$250 printer system as independent of its host as possible, we designed the system's driver electronics (Fig 3) to store one complete line of character data in a FIFO buffer memory. The alternative approach—storing the characters in the host's memory and outputting them sequentially whenever the printer must print a line—creates both software and timing overhead for the host. Overcoming these drawbacks can prove especially limiting to a computer hobbyist, who often lacks the necessary software background to program around them.

The driver electronics incorporates all of the timing and

control circuitry required to transfer a line of data from FIFO memory to the printhead; the operation doesn't require software-generated control signals. The electronics interfaces with the host through an 8-bit parallel connection, and an "input strobe" control line from the printer informs the host of a character's acceptance. Sent over seven data lines, the ASCII character information for an entire line is printed whenever the electronics receives a carriage return ( $OD_{16}$ ) signal or whenever the 40-character buffer fills.

The printer ignores all control characters except carriage return; the electronics initiates repeated line feeds by outputting multiple carriage-return commands. Because the printer can output only upper-case ASCII characters, the electronics also translates all lower-case characters into their upper-case equivalents.

A hardware power-up reset circuit automatically clears the FIFO memory when a user first turns on the system. Triac-controlled and powered by the 120 Vac secondary on its power supply transformer, the printer's motor remains isolated from the system's main power line. And because the power transformer has two primaries that can connect either in series or in parallel, the entire system can accommodate 240 Vac European power sources as well as 120 Vac power supplies.

## DESIGNING CONSUMER- SYSTEM PERIPHERALS

# FLOPPY-DISK SYSTEM PARTITIONS FUNCTIONS ON TWO BOARDS

by Thomas Durston

The design goals we formulated in March 1975 for the Altair floppy-disk system were essentially the same as those formulated for other Altair products. Striving to keep our approach general at first, we decided to

- ★ Design the hardware to interface the Altair 8800 computer to currently available floppy-disk drives
- ★ Design the hardware to allow efficient use of software
- ★ Design the system for low cost without sacrificing reliability
- ★ Complete the hardware design in a minimum time
- ★ Design for the simplest circuitry to allow easy troubleshooting
- ★ Create a product that a user can build from a kit
- ★ Use a minimum number of special components
- ★ Design a product that can operate from a variety of ac supply voltages and frequencies.

As a first step toward making these goals more specific, we had to define the system configuration, decide upon the most efficient read/write format and consider the software required to drive the system. After examining our options, we set these more specific design goals:

- ★ Utilize hard-sectored formatting

Thomas Durston is engineering program director at Mits, Inc., Albuquerque, NM.

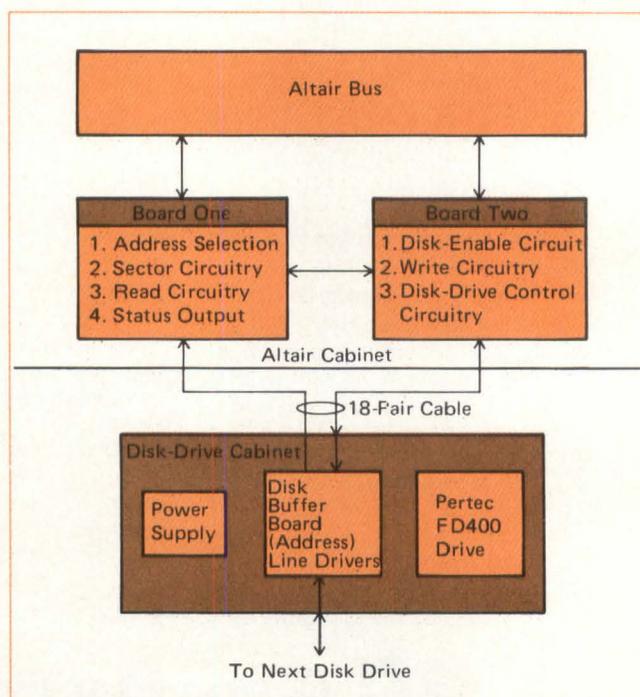


Fig 1 Floppy-disk system designed to mate with the Altair CPU incorporates a Pertec drive, chosen partly for its dc drive motor, which is insensitive to line frequency variations and requires no drive belt.

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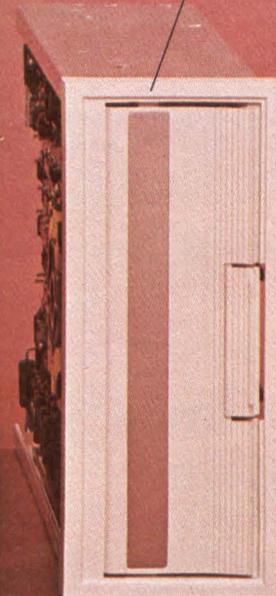
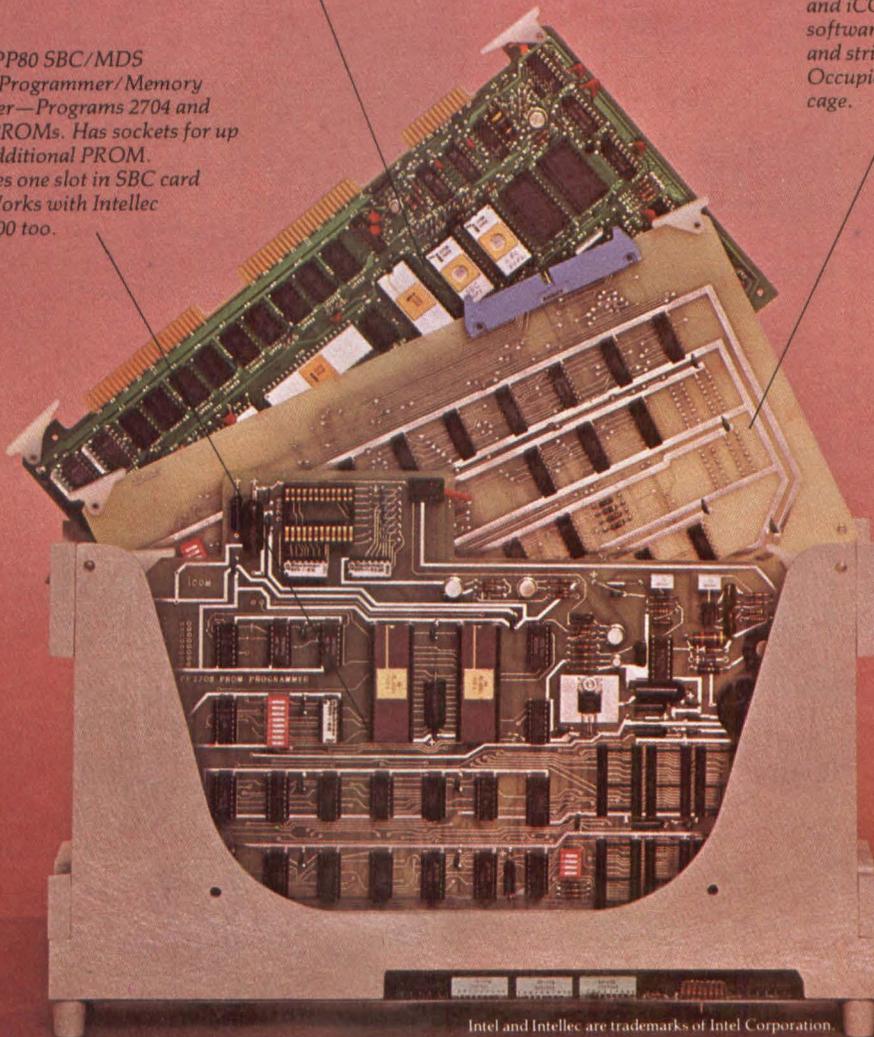
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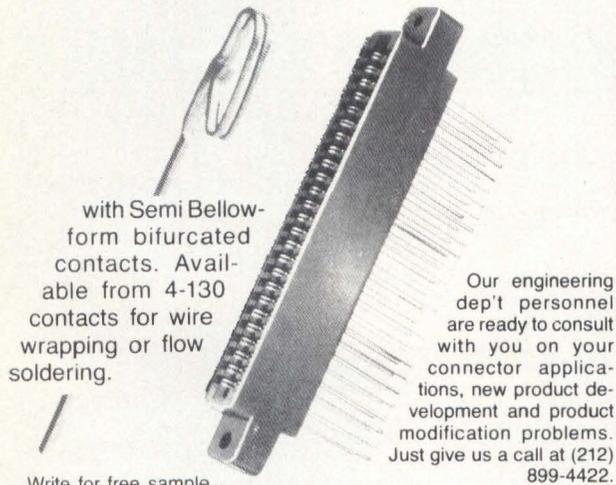
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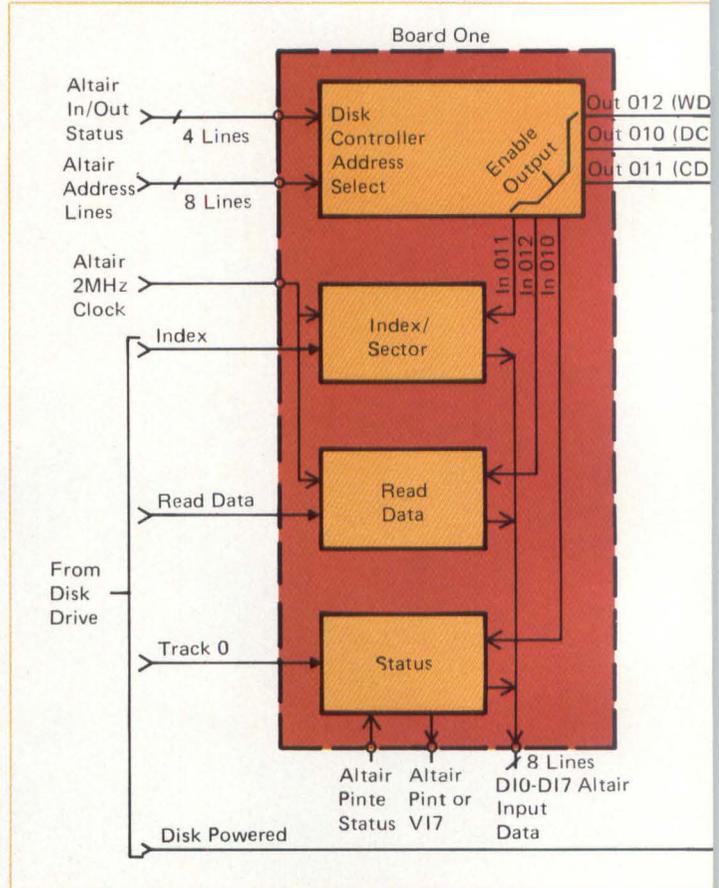
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- ★ Install one drive per cabinet, with provisions for connecting up to 16 drives in a system
- ★ Partition the disk controller into seven major circuit groups. These groups include addressing circuits for communication with the computer, index/sector circuitry, a Read Data circuit, disk-drive and controller status circuits, a Write Data circuit, a disk-drive-selection circuit and disk-drive function-control circuitry.

### achieving the goals

After we completed this initial design phase, we discovered that the required controller circuitry, which incorporates

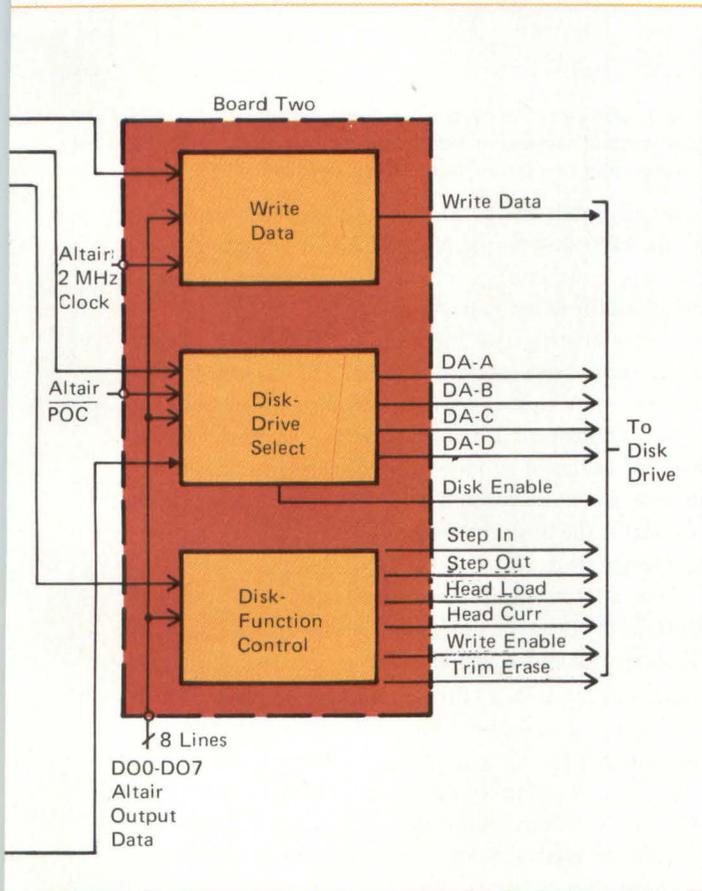


**Fig 2 Floppy-disk controller circuitry incorporates about 60 TTL ICs, too many to fit on one of the 5" x 10" boards used in the Altair. So designers partitioned the controller's seven major circuit**

about 60 TTL ICs, was too dense to fit on one of the 5" x 10" cards used in the Altair computer. So we split the circuit functions — Disk Controller Board One provides address selection and also contains the three circuits that transfer information to the Altair CPU (input instruction), while Disk Controller Board Two handles outputs from the CPU (Fig 1). Dividing the controller functions this way has simplified troubleshooting in the floppy-disk system.

Some of the seven circuit groups (Fig 2) were easily implemented. For the address selection logic on Board One, we used standard 7400-type gates to decode the system's eight address and four I/O status lines into the lines that enable the six disk controller circuits. Designing the logic for the index/sector circuitry and the Read Data circuit was tougher. We used synchronous logic where possible; where timing delays were required, we achieved them through careful application of one-shot multivibrators. We designed

the timing circuits in the index/sector decoder to allow a 20% variation in pulse width output, and we used 5% tolerance Mylar capacitors to ensure accuracy and stability. We also bypassed the Vcc supply at each one-shot, using 0.1 $\mu$ F ceramic disk capacitors, and we located the timing components as close as possible to their respective pins on the IC. The Read Data circuit utilizes the only monostable multivibrator in the disk controller that requires 10% accuracy, and 5% tolerance mica capacitors minimize variations in it. The rest of the circuitry consists of logic connected synchronously to provide the sector count and the read data presented to the data input bus in the computer.



groups; Board One provides address selection and input instruction functions while Board Two handles outputs from the Altair central processing unit.

The other input circuitry on Board One is the status circuit, which we also designed as simply as possible. It consists of line drivers with their inputs connected to the various circuits as required by software and their outputs connected to the Altair data input bus. To reduce noise in the system, the +5 V Vcc supply for Board One contains bypass capacitors, and all unused inputs are either grounded or connected to Vcc through 1K  $\Omega$  pullup resistors.

The same design principles used on Board One apply to Board Two. We made the design of the Write Data circuit on Board Two completely synchronous, including the 9316 counters used to generate the write clock and data timing. This type of circuitry is highly stable and eliminates the ripple through counting noise found in nonsynchronous logic. The disk-drive-select circuitry is uncomplicated; it consists of a 4-bit latch, a flip flop and a one-shot timer. We designed the disk function-

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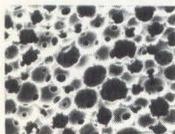
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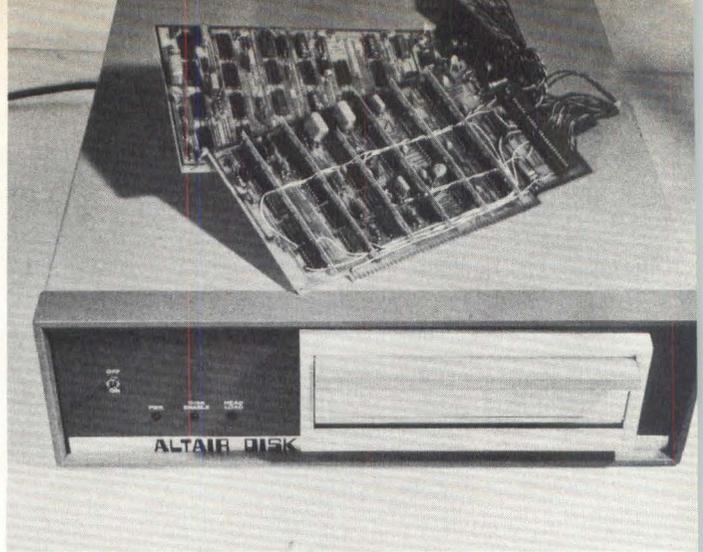


Fig 3 Complete floppy-disk system stores more than 300K bytes/diskette and accesses in less than 1 sec. A typical computer system incorporates two drives; up to 16 can serve one CPU.

control circuit to operate the individual disk drive functions; each function requires at least one timing circuit. As before, we configured the required one-shot timers to allow for worst-case variations.

After investigating interconnect and wiring alternatives, we chose a method in which 0.1" center-pin connectors mate to sockets with crimp or solder pins; the scheme allows a kit builder to assemble typically expensive cables at good savings. For the interconnect wiring, we chose twisted-pair flat cable to provide what we feel is the best noise immunity and signal transfer characteristics.

For a floppy-disk drive, we selected the Pertec FD-400, both for its dc motor and performance characteristics (its dc motor is insensitive to line frequency variations and requires no drive belts) and its price. We designed a power supply to accommodate the floppy's requirements and keep special parts usage and cost to a minimum; to simplify the design and guarantee supply stability we chose 7800-type voltage regulators. The system's heatsinking utilizes aluminum extrusions and a cooling fan; external interconnections occur through DC-37 rectangular connectors, chosen because of availability, reliability and low cost.

The resulting floppy-disk system (Fig 3) can store over 300K bytes/diskette and has an access time of less than one second. It usually uses Altair Disk Basic software, which resides in the lower 20K of memory and provides disk utilization routines. The system's two controller cards plug into the computer's bus; all control, status and data I/O goes through three I/O ports dedicated to disk control. ♦

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## Monitor network spots tape-skew effects

When recording digital data in such high-density formats as the 800-character/in NRZ mode, many digital tape drives exhibit a sharp rise in their character reading failure rates. Many of these reading errors arise from skew, the failure of a tape drive to record characters perpendicularly to the tape's edge.

Skew can result from both static and dynamic conditions. In static skew, character reading errors stem from physical misalignment of the recording head, tape guides or individual track recording gaps within the head assembly. In dynamic skew, the tape wanders and squirms as it passes across the recording head. Both types of skew cause serious problems when tapes are recorded and read on different machines or when data is interchanged between computers.

Seeking to reduce these harmful effects of skew, Robert

McKenna of NASA's Goddard Space Flight Center, Greenbelt, MD, has devised and patented a network that automatically checks the skew and character spacing of digital tape drive systems. The network pinpoints skewed data recordings and determines whether the flaws require correction.

In the network's 9-track version, a series of pulse shapers receive input information derived from the system's conventional peak detectors. To establish skew-time displacement, outputs from these pulse shapers go to the circuit's first-pulse detector. And to locate individual track errors, the network parallel-processes inputs from the drive's tracks. The network also incorporates a circuit for indicating character spacing errors.

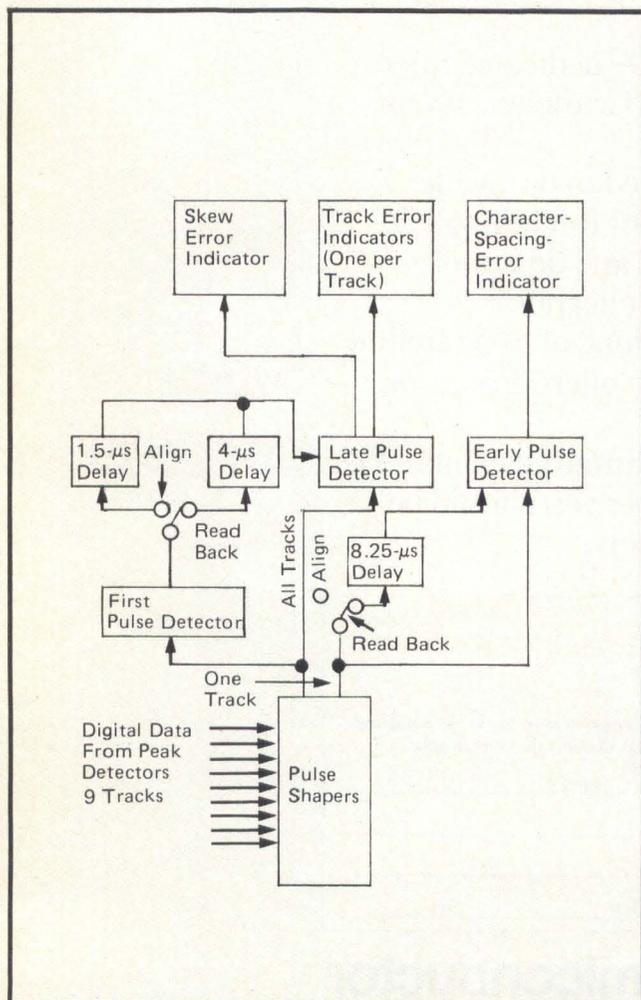
To align a tape system's reading heads, McKenna flips an align/readback switch to its align position — an action that activates a 1.5- $\mu$ s delay, corresponding to the read-head skew typical of 800 character/in, NRZ recordings. For other recording densities and tape speeds, this delay differs.

After the input tape drive reads a skew alignment tape, detected signals arrive on the input tracks, and the first-pulse detector identifies the initial shaped pulse, triggers the 1.5- $\mu$ s delay and applies a signal to a late-pulse detector. Any pulses arriving after the 1.5- $\mu$ s delay also go to the late-pulse detector, which activates a skew-error detector and warns of any read-head misalignments. To make subsequent identification and alignment easier, track-error indicators also identify the track or tracks where late pulses appear.

To align a drive's recording heads, McKenna follows a similar procedure except that he flips the network's align/readback switch to its readback position and allows a 4.0- $\mu$ s delay. (As before, the length of this delay varies with the drive's recording speed and density.) Using the recording head slated for testing, he then records a series of ones and plays them back into the indicator circuits, which pinpoint any skews and the offending track or tracks.

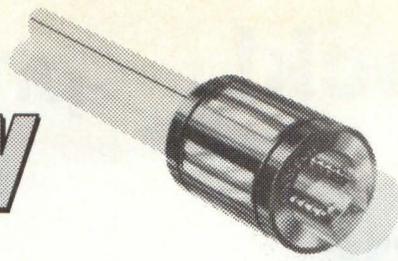
A character-spacing-error indicator couples to one of the network's tracks, whose output goes to an early-pulse detector, adds McKenna. If the network's switch is in its readback position, the output then goes through another align/readback switch to an 8.25- $\mu$ s delay, and then to the early-pulse detector, whose output in turn drives a character-spacing-error indicator.

A signal received on any track triggers the delay circuit, which inhibits the early-pulse detector until the end of the 8.25- $\mu$ s delay. After that period, says McKenna, pulses on the line trigger the detector, which in turn activates the character-spacing-error indicator and readies the system to spot excessively dense character recordings.

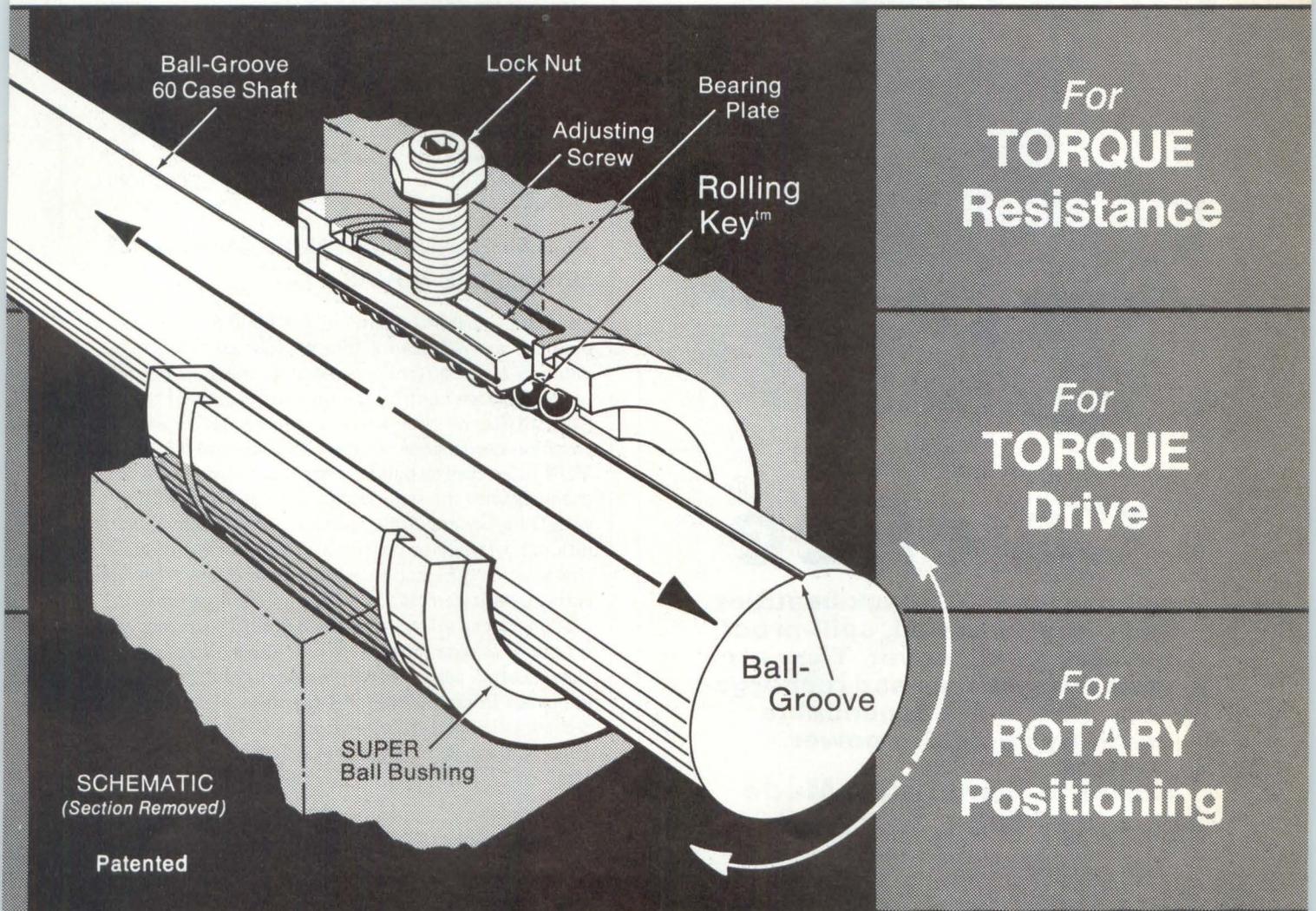


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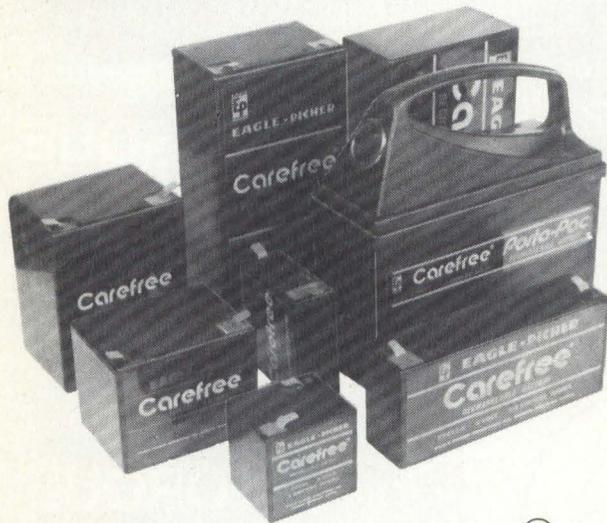


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## product news

### **DC-DC CONVERTER POWERS GAS-DISCHARGE DISPLAYS**

The EP6746A dc-to-dc converter accepts inputs in the 4-11 Vdc range (450mA max.) and outputs  $\pm 110$  Vdc regulated (5mA each output) with a 70% efficiency. It measures 3" x 0.4" x 0.655" and has logic controlled enable/disable circuitry that can turn off outputs and lower standby current drain to 2 mA. Applications include powering gas-discharge displays in portable, battery operated terminals and in peripherals. Price: \$8.50 in quantity. PCA Electronics, 16799 Schoenborn St., Sepulveda, CA 91343.

(213) 892-0761

Circle 292

### **4-OR 8-CHANNEL ASYNCHRONOUS MUX SERVES D.G. NOVAS**

For Data General Nova minis, the 8063 multiplexer provides an interface for four or eight asynchronous data sets or local terminals. All data transfers occur under program control; the unit treats each of the transmit/receive channels as a separate device with a common device code address. You can add additional MUX interfaces to build a system with as many as 64 channels with the same device address. Compatible with Data General 4060 software, the device has additional software to control and monitor baud rate, character length, stop bit(s), parity and line break generation, parity errors, data overrun and line break detection. Other software features govern such modem functions as data terminal ready, request to send, clear to send, carrier detect, data set ready and ring indicator. Price: \$1250 for 4-channel unit, \$2250 for 8-channel unit, both in singles. MDB Systems, Inc., 1995 N. Batavia St., Orange, CA 92665. (714) 998-6900

Circle 300

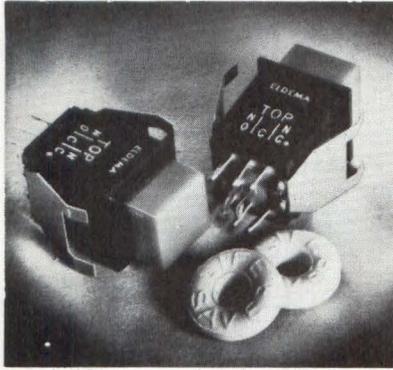
### **250 W SUPPLIES SWITCH AT 40 KHZ**

These five power supplies, designated the 9E Series, switch at 40 kHz and output 250 W. Measuring 2.25" x 4.94" x 15.0" and weighing 6 lb. 3 oz., each unit fits crosswise in a standard 5.25" Retma rack while using 2.25" of rack depth. Input voltage range measures 115/230Vac +10/-20%, with a 20ms hold-up. Ripple and noise equal 50 mV p-p, and regulation measures 2mV for a full 30% line change and 0.2% for a full load change. Overall efficiency equals 80% minimum. Price: \$395 in singles. Powertec, 9168 De Soto Ave., Chatsworth, CA 91311. (213) 882-0004

Circle 297

## 1" INDICATOR LIGHTS MOUNT ON PCB'S OR SNAP-IN PANELS

These 1" indicator lights fit the manufacturer's "Shorty" family of illuminated pushbutton switches and come in four configurations for PC board or snap-in panel mounting of T 1-3/4 bi-pin base or T 1-3/4 midget flange base lamps. Series 856 and 857 indicators accept the T 1-3/4 bi-pin base



lamp; they have 0.025" square terminations. Snap-in panel-mounted Series 965 indicators accept the midget flange lamp and offer faston 0.110" or 0.025" square terminations, while Series 969 indicators also accept the midget flange lamp. Eldema Div., Genisco Technology Corp., 18435 Susana Rd., Compton, CA 90221. (213) 393-9494 **Circle 282**

## VACUUM-COL. TAPE DRIVE TRANSFERS 120 KBYTES/SEC

This medium-speed tape drive, designated the TME, can operate at any speed from 12.5 to 75 ips and utilizes vacuum column tape buffering. It accommodates standard 10½" and 8½" reels or minireels and transfers 20,000 to 120,000 bytes/sec with a maximum rewind time of three minutes. Start time at 75 ips equals 5.5 ± 1.0 ms, and maximum stop time equals 6 ms. Recording densities of 556, 800, 1600 and 800/1600 bpi are standard. The unit rewinds at 200 ips and has optional fast forward speed of 150 ips. The TME comes in three configurations: TME-03: NRZI I/O compatible with the manufacturer's TM-100 or TMB-03; TME-04: PE, I/O compatible with the manufacturer's TM-100 or TMB-04; and TME-05: PE/NRZI, I/O compatible with the manufacturer's TM-100 or TMB-05. Ampex, 401 Broadway, Redwood City, CA 94063. (415) 367-4151 **Circle 284**

## RS 232 INTERFACE SERVES CART. RECORDER

This RS 232 interface serves the manufacturer's TDC 3000 digital cartridge recorder and mounts on one PC board, which in turn mounts inside the recorder. It runs on power from the TDC 3000 built-in supply and responds to control characters from a local terminal or modem. An internal 6800 microprocessor provides special requirements such as generation of communication protocols and format checking. The interface operates in binary write, binary read, ASCII and binary block modes; error messages include invalid command code, drive unsafe, CRC error detected, transmission parity error detected, data transmission overflow detected and drive off-line. Tandberg Data, 4901 Morena Blvd., Suite 407, San Diego, CA 92117. **Circle 283**

## ANALOG DATA ACQ. SYSTEMS REQUIRE NO HOST OVERSEER

Series 500 analog data acquisition modules provide crystal controlled sampling (4.8 MHz) and processing of up to eight analog signals without supervision from a host computer. They digitize input signals into a normalized 16-bit floating point format using a Fortran-compatible language. Processing rate for standard units is 125 kHz with 12-bit resolution, and a high-speed model offers 250 kHz digitization and 10-bit resolution. The units interface to the manufacturer's MAP floating point array processors and occupy two slots in the MAP chassis. CSP, Inc., 209 Middlesex Turnpike, Burlington, MA 01803. (617) 272-6020 **Circle 273**

## \$24.95 KEYBOARD APES ASR-33 ARRAY

For terminal applications, Model KSA-33 keyboard uses the ASR-33 Teletype key array and has 53 switches, space bar mechanism and keycaps. The unit incorporates DI-100 switches, which contain two sets of normally open crosspoint contacts internally connected in parallel, and has been tested to 100 x 10<sup>6</sup> operations without electrical or mechanical failure. Price: \$24.95 in 1000s. Data Interfaces, Inc., 12 Cambridge St., Burlington, MA 01803. (617) 272-7456 **Circle 280**



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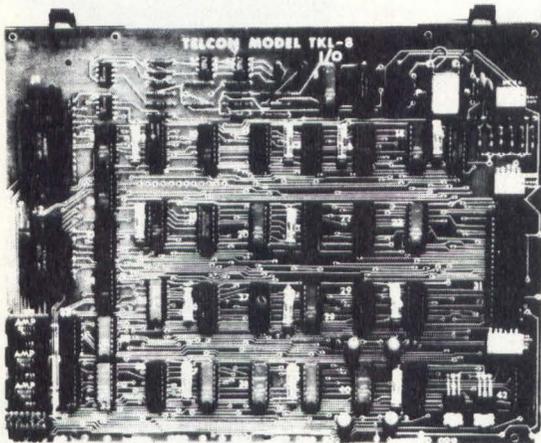
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CIRCLE 46

## product news

### PORTABLE LOGIC ANALYZER CAPTURES EIGHT 50-MHZ CHANNELS

Model 50D Logiscope can simultaneously capture eight digital data streams at sample rates to 50 MHz. It works with any externally triggered oscilloscope or X-Y display, and its True Sample mode lets you exclude from the record all "glitches" that endure for a sample period or less. With a dual memory feature, two 512 x 8 semiconductor memories can each simultaneously capture up to eight data streams; you can then view all 16 streams on a two-channel scope. The unit measures 4½" x 8½" x 14½" and weighs 18 lbs. Price: \$3375. BP Instruments, Inc., 10601 S. De Anza Blvd., Cupertino, CA 95014. (408) 446-4322 **Circle 295**

### 3350-COMPATIBLE DISK HEADS WRITE 6400 BPI

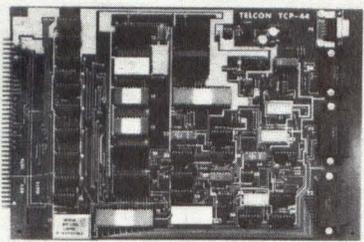
For use in disk drives compatible with the IBM 3350, these disk heads provide storage capacities of 317 Mbytes/spindle in typical applications. Operating at up to 6400 bpi, 480 tpi, the heads incorporate integrated circuits, mounted on each head arm, that perform write driver, read amplifier, head select and fault detection functions. Included in the series are Model 355004 data head with four read/write air-bearing elements, Model 335002 data head with two read/write air-bearing elements and Model 335001 servo head with one read-only air-bearing element and an arm-mounted differential read amplifier. The heads contact the oxide disk surface when a disk is at rest and fly at about 20 μin. at the inside track when the disk rotates at 3600 rpm. Track width measures 1.45 mils, gap length equals 55 μin., and write current ranges from 35 mA 0-to-peak (inner heads) to 40 mA 0-to-peak (outer heads). The heads' 1F and 2F frequencies equal 2.4 MHz and 4.8 MHz respectively, and output from the data head read amplifier measures 14 mV peak-to-peak (minimum) and 140 mV peak-to-peak (maximum). Applied Magnetics, Magnetic Head Div., 75 Robin Hill Rd., Goleta, CA 93017. (805) 964-4881 **Circle 296**

### SWITCHING POWER SUPPLIES USE 60-HZ MAGNETICS

These switching power supplies utilize 60-Hz magnetics and thereby eliminate such 20-kHz switching problems as output spikes, high ripple content, radiation into associated equipment and power line feedback, according to the manufacturer. Peak-to-peak ripple of the Series 100 measures less than 2mV, and maximum no-load-to-full-load regulation measures no more than 3mV. Outputs range from 1.5-6 Vdc to 6-28 Vdc, with additional combinations available. Caltech Mfg. Co., Inc., 3305 Vincent Rd., Pleasant Hill, CA 94523. (415) 932-3911 **Circle 299**

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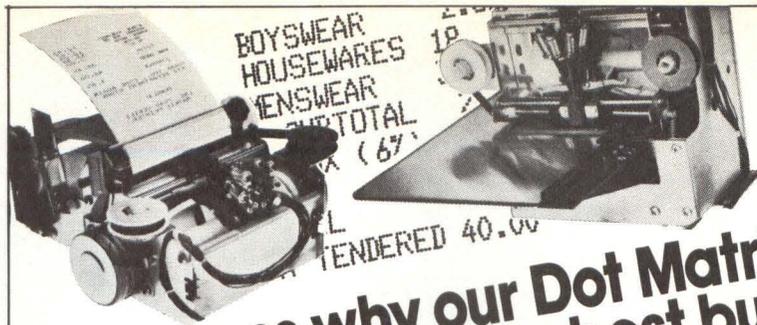
A processor board, 1200-baud modem with I/O port, dual serial port board, dual parallel port board, 4K, 8K or 16K memory board with EPROM programming and hexadecimal readout are also available. Telcon Industries, Inc., 5701 N.W. 31st Ave., Fort Lauderdale, FL 33309. (305) 971-2250 **Circle 281**

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Model 399 A/D conversion system provides 16-bit resolution with a 3- $\mu$ s conversion time. It comes with or without sample and hold, power supply, and single-ended or differential multiplexing. Standard inputs equal  $\pm 5$  or  $\pm 10$  V;  $\pm 1$  and  $\pm 100$  V are optional. Datawest Corp., 7333 E. Helm Dr., Scottsdale, AZ 85260. (602) 948-3280 **Circle 275**

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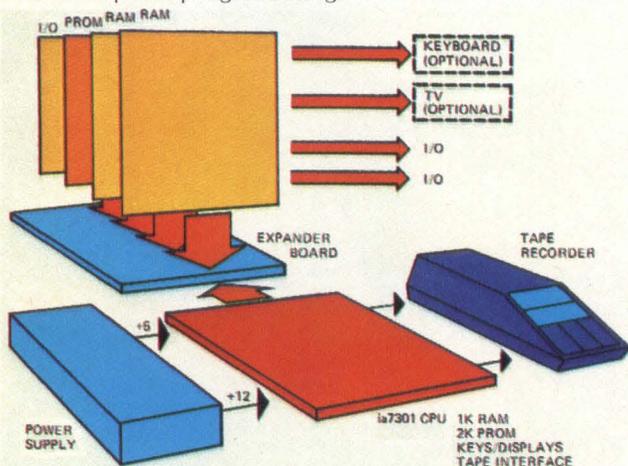
The fact is that right now microcomputer programming is a bear. Microprocessors are loaded with subtleties which make software development a long, arduous process. That's why we developed the ia7301 Computer in a Book.\* It's a fully operational microcomputer system and a 250 page programming course all contained in a 3-ring binder. This is not a kit or a toy but a powerful, microcomputer system (based on the industry standard, the 8080) and a practical programming course specifically designed to quickly bring you up to a high level of understanding and proficiency in programming 8080 based microcomputer systems.

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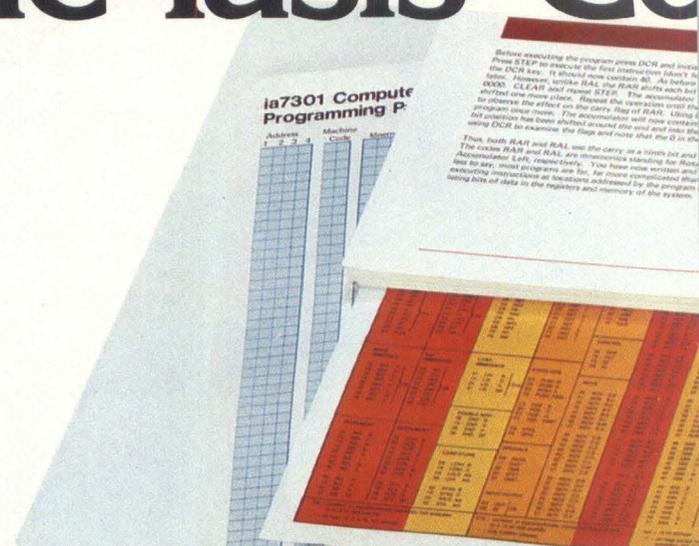
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\*U.S. Patent Pending  
Pong is a trademark of Atari, Inc.



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Also the write tape and read tape mode keys have been carefully designed for accurate and convenient operation with any home cassette tape recorder that has an earphone and remote microphone jack. Two LED indicator lamps tell how long it takes to dump or reload programs from the system's memory onto tape and back again. But in the reloading cycle, if any errors have occurred such as a lost piece of data or the volume knob is too low, the readout displays will indicate errors. This little feature prevents untold problems in debugging a reloaded program.

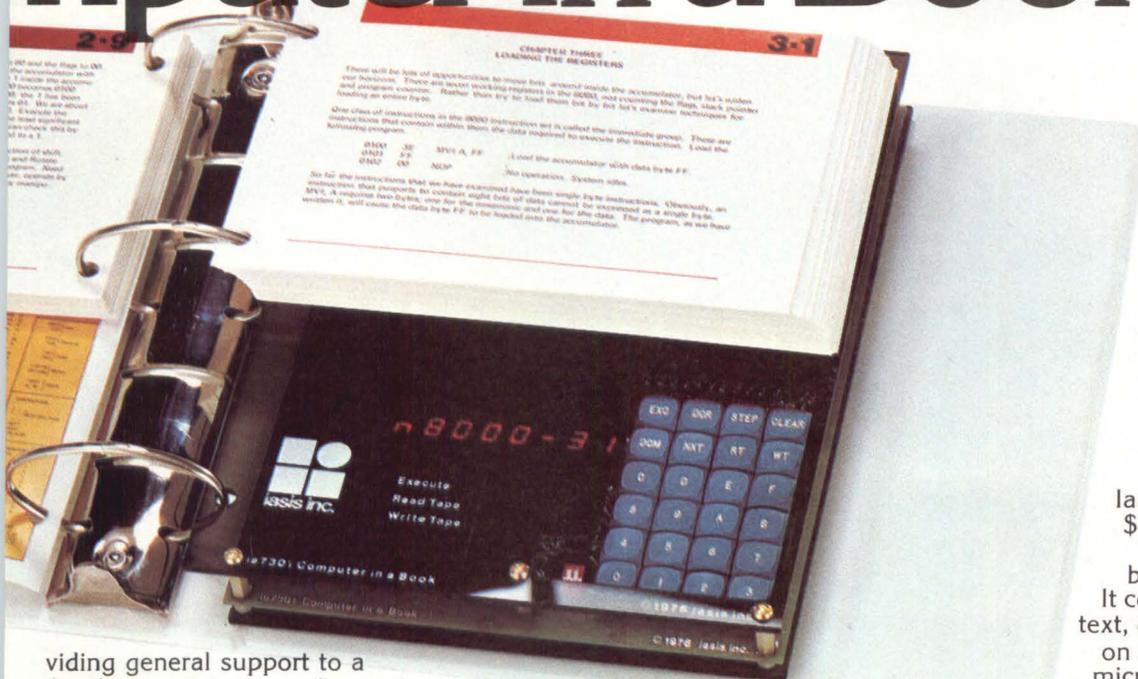
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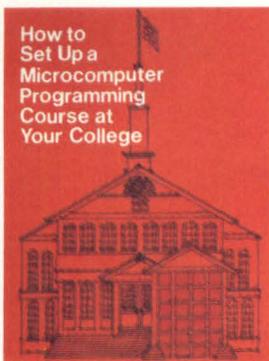
Thus what served as an educational system can now be upgraded for many new applications. We've included a machine language coding pad for writing and documenting programs, working out subroutines and pro-

# programming is a snap computer in a Book



viding general support to a development system when extensive programming or debugging is necessary. The Computer in a Book may also be used to train field service technicians by putting verbal information and programs on cassette tapes. We are coming out with preprogrammed PROMs and extension tapes containing new application packages such as floating point arithmetic and micro-assembler programs. Our goal is simple. We want to provide microcomputers that are useful and practical.

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## Stay Small, Think Big and Grow

Until recently, most design engineers who wished to work on projects at the frontiers of current technology found themselves limited to employment with large corporations in large metropolitan areas. Only those corporate giants could afford the cash and time outlays required to conduct state-of-the-art research and development. Now, however,

many smaller industrial firms have access to the esoteric equipment the giants routinely use; as a result, designers in smaller firms work on challenging projects like those formerly reserved for their colleagues in the conglomerates.

In many ways, however, small-firm designers face even greater challenges than their large-firm counterparts. Rather than confining their efforts to one small subsystem in a large project, they must often also assume responsibility for such factors as make-or-buy decisions, budget balancing, and customer and vendor relations.

Placed on the firing line this way, many of the design engineers I've recently dealt with fail to measure up. Why? Today's engineers have the talent required to handle such multi-function job responsibilities, so the problem lies not so much in developing that talent as in forcing engineers to recognize that they have it.

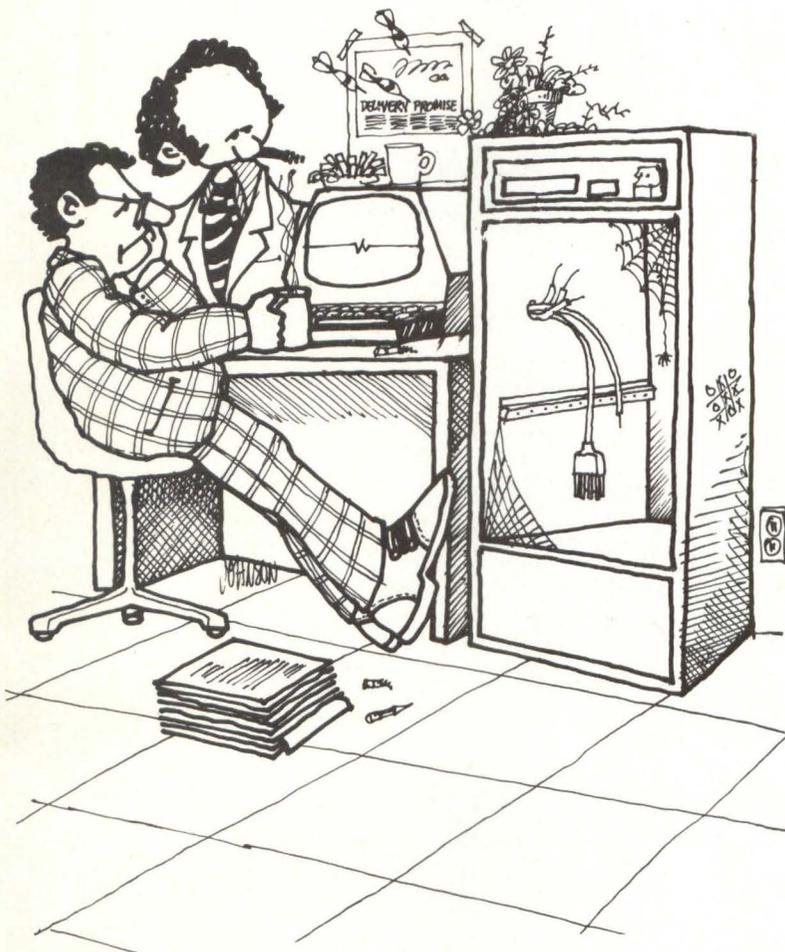
Given the proper environment, how can engineers in smaller firms approach their work so they develop the attitudes and methods that allow them to assume overall project responsibilities? How can they break out of the structured but limiting cocoon that mere competence in college courses weaves around them?

The key word is "volunteer." Just as air rushes in to fill a vacuum, small firms always find *someone* to take responsibility. Small-firm designers must realize that because their companies have fewer people to handle company-wide projects, all levels of company management remain intimately concerned with corporate goals. To help shape these goals, a designer need only speak up. Most small-firm designers who do find their companies highly receptive to good ideas — and grateful to the designers who generate them.

A handwritten signature in black ink that reads "Lewis G. Zirkle". The signature is written in a cursive, flowing style.

*Lewis Zirkle is president and chairman of KeyTronic Corp., Spokane, WA. We will be pleased to provide space for opposing views.*

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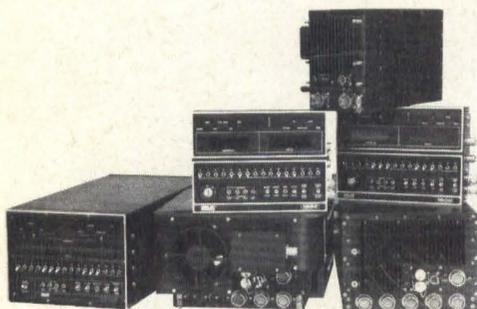
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