A CAHNERS PUBLICATION
MARCH 4, 1987

EDN

Scan-path methods ease sequential-logic test

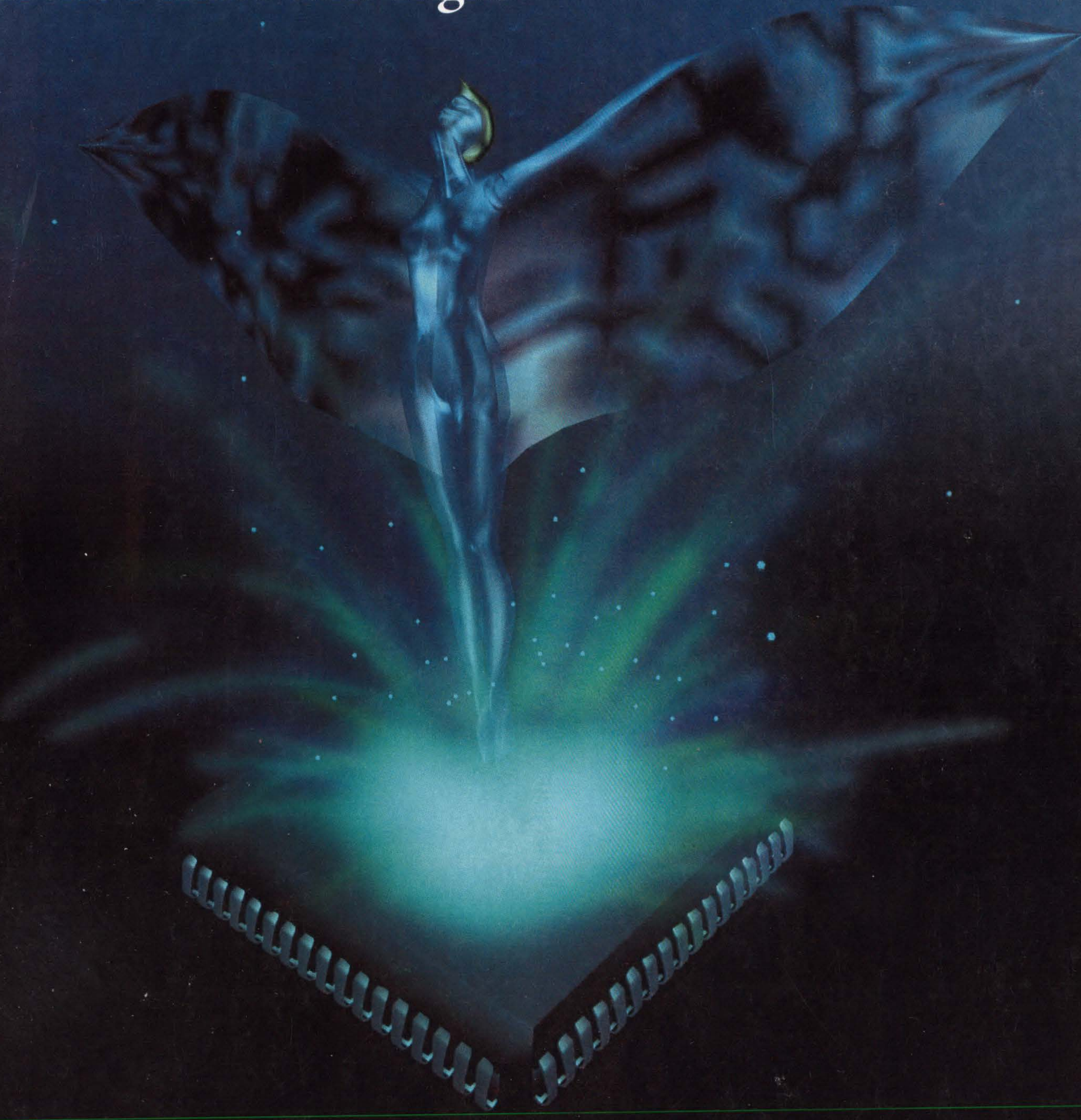
Boards let IBM PCs emulate fax machines

New core materials help power-supply designers

ADEE preview

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Graphics ICs help the artist's muse take flight



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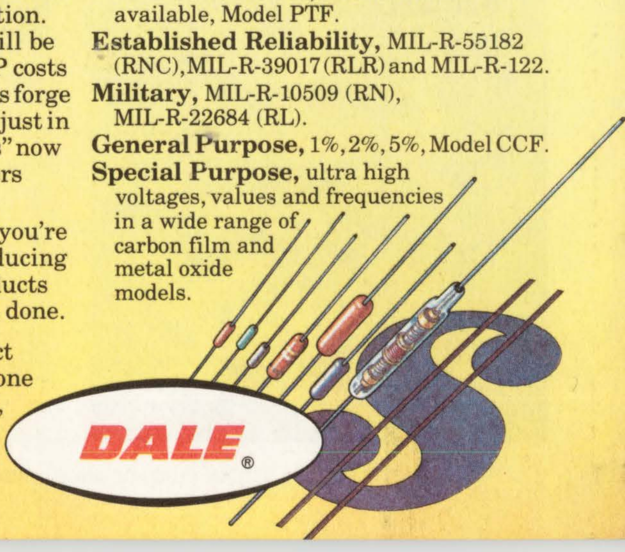

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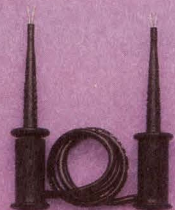
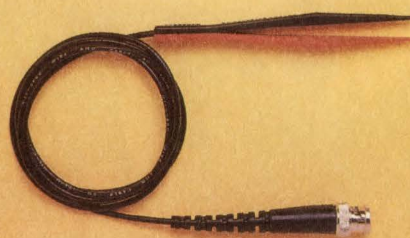


SMD TEST TWEEZER™ TO BNC MALE: MODEL 5142 (SHOWN). TO TWO SINGLE STACKING BANANA PLUGS: MODEL 5143



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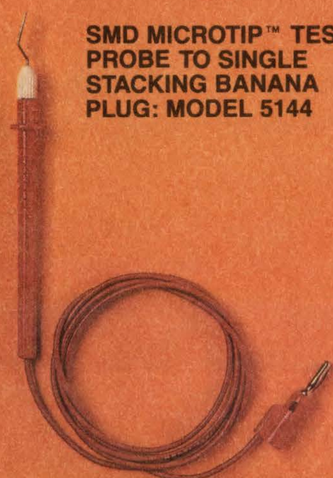

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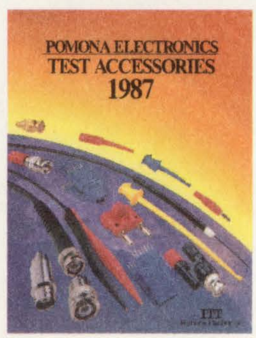

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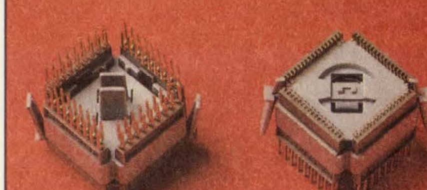

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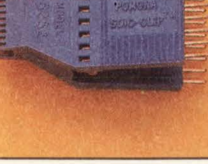

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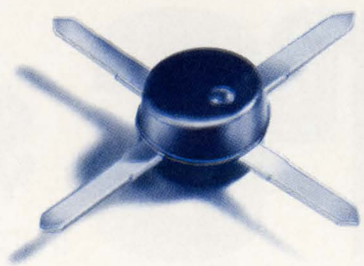

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MAR-3	DC-2000	8	+8	6.0	1.70	(25)
MAR-4	DC-1000	7	+11	7.0	1.90	(25)
MAR-7	DC-2000	8.5	+4	5.0	1.90	(25)
MAR-8	DC-1000	21	+10	3.5	2.20	(25)

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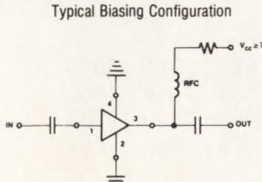

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CIRCLE NO 90

Volume 32, Number 5 — EDN — March 4, 1987

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

On the cover: *Powerful graphics-processor ICs can amplify an artist's skills. The Superset system used to produce this issue's cover incorporates the TMS34061 video system controller; in the future, such systems will employ graphics engines like those discussed in this issue's Special Report (pg 112). Those engines will lower the systems' cost, but they won't do away with the need for artistic talent, as Regional Editor Margery Conner notes in this issue's Editorial (pg 47). The cover image and the wire-frame image on pg 113 were recorded on a Matrix QCR-Z film recorder. (Photo courtesy David Hamby Design, Torrance, CA)*

DESIGN FEATURES

Continued on page 7

EDN (ISSN 0012-7515) is published 45 times a year, biweekly with one additional issue in January, February, March, August, and December, two additional issues in April, June, July, September, and November, and three additional issues in May and October by Cahners Publishing Co, a Division of Reed Publishing USA, 275 Washington Street, Newton, MA 02158. William M Platt, President; Terrence M McDermott, Executive Vice President; Jerry D Neth, Vice President of Publishing Operations; J J Walsh, Financial Vice President/Magazine Division; Thomas J Dellamaria, Vice President Production & Manufacturing; Frank Sibley, Group Vice President. Saul Goldweitz, Chairman; Ronald G Segel, President and Chief Executive Officer, Robert L Krakoff, Executive Vice President. Circulation records maintained at Cahners Publishing Co, 270 St Paul St, Denver, CO 80206. Second class postage paid at Denver, CO 80202 and additional mailing offices. Postmaster: Send address changes to EDN, 270 St Paul St, Denver, CO 80206.

BPA ABP

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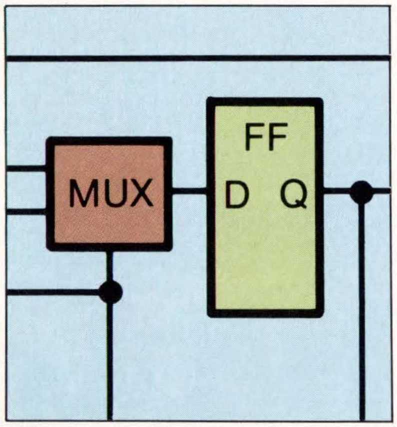

***Placing a multiplexer** in front of each flip-flop sets the stage for scan-path testing. You can now find tools that allow you to implement the scan-path technique without sacrificing circuit performance and die size (pg 67).*

TECHNOLOGY UPDATE

PRODUCT UPDATE

DESIGN IDEAS

Continued on page 9

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Continued from page 7

EDITORIAL 47

We have previously contested the suggestion that computers and software can make it unnecessary for humans to master basic writing skills. This issue's cover story, on graphics ICs, makes a similar warning appropriate for graphics-arts skills.

NEW PRODUCTS

PROFESSIONAL ISSUES 227

A study in contrasts: US engineers recall their visit to Japan.—*Deborah Asbrand, Associate Editor*

LOOKING AHEAD 241

Annual growth rate is 10.2% for rectifier market . . . Molecular electronic devices to be commercial by 2000.

DEPARTMENTS

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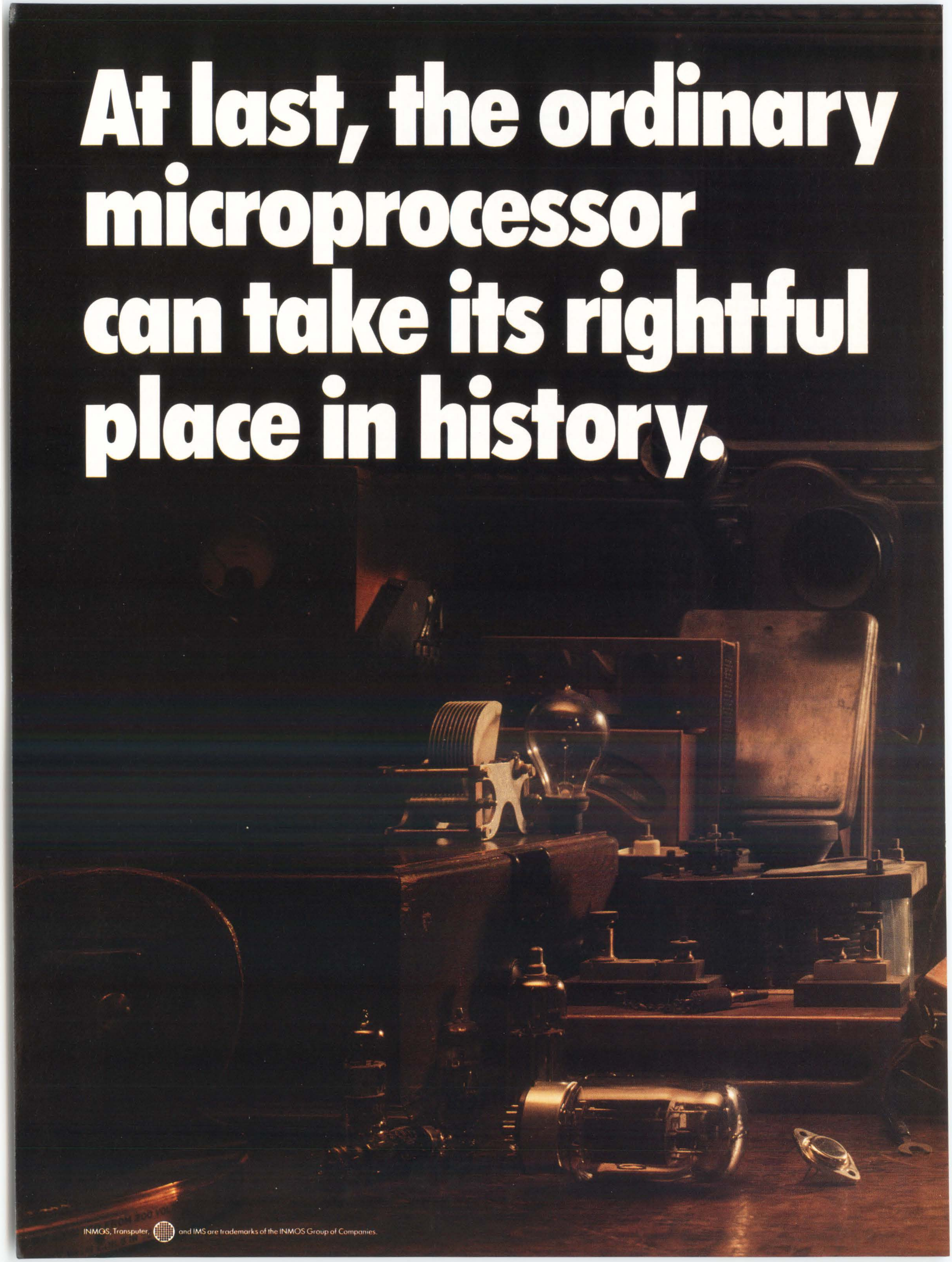
At last, the ordinary microprocessor can take its rightful place in history.
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It had to happen—the conventional microprocessor has had its day. Relegated to the ranks of yesterday's devices by the new transputer family from INMOS. It's history in the making.

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While transputers excel in single-processor systems, their real power can be unleashed by connecting any number of transputers together via the high-speed serial links. Multi-transputer systems can deliver the performance you need today, and can be easily expanded in the future as your processing requirements increase.

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INMOS transputers are available now and have already found their way into companies who are evaluating, prototyping and manufacturing transputer-based systems. Applications include supercomputers, DSP, graphics, robotics, AI, distributed control systems, PC's, engineering workstations and many others.

Write or phone for more information on the transputer family and start making history yourself.

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IMS T212	16 bit Transputer–2Kbyte —4 links
IMS M212	16 bit Disc Processor–1Kbyte—2 links
DEVELOPMENT TOOLS	
IMS D701-2	IBM PC—Transputer Development System.
IMS D600	VAX/VMS—Transputer Development System.
EVALUATION BOARDS	
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IMS B003-1	Double Eurocard + 4 x IMS T414 + 4 x 256Kbyte DRAM.
IMS B004-2	IBM PC Format + IMS T414 + 2Mbyte DRAM.
IMS B006-2	Double Eurocard + 9 x IMS T212 + 128Kbyte SRAM.
IMS B007-1	Double Eurocard + IMS T414 + 0.5Mbyte DRAM + 0.5Mbyte Video RAM.
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CIRCLE NO 83

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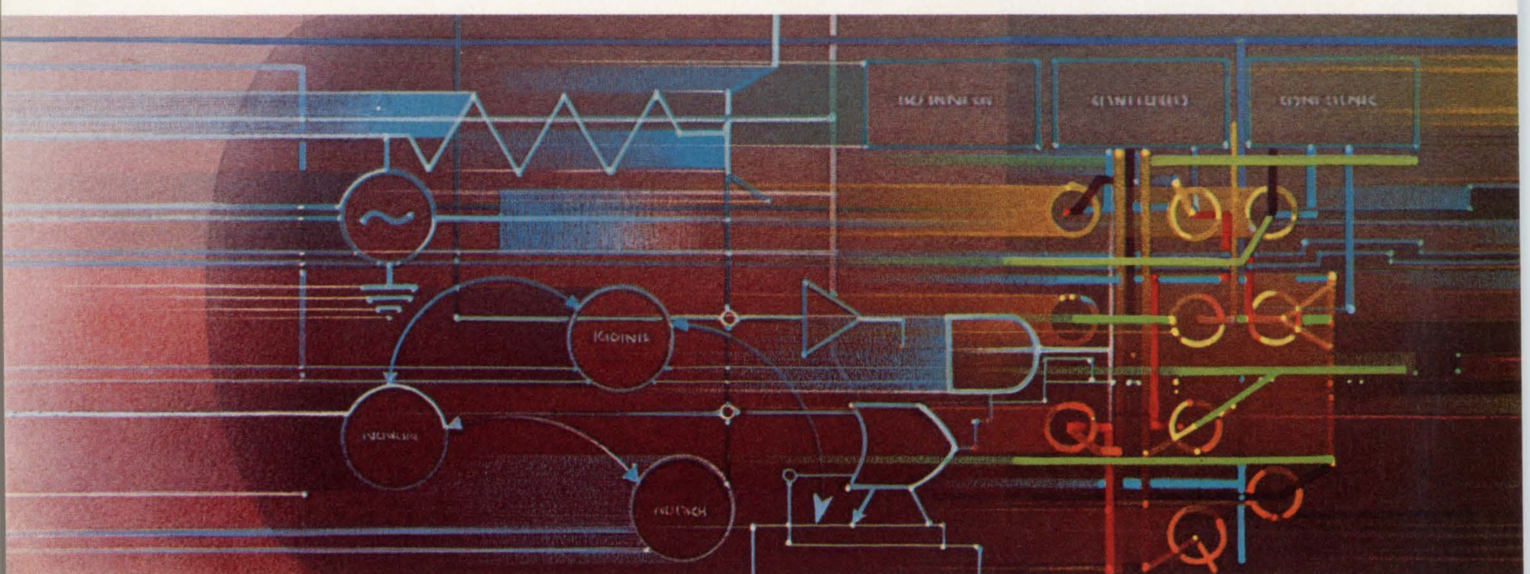

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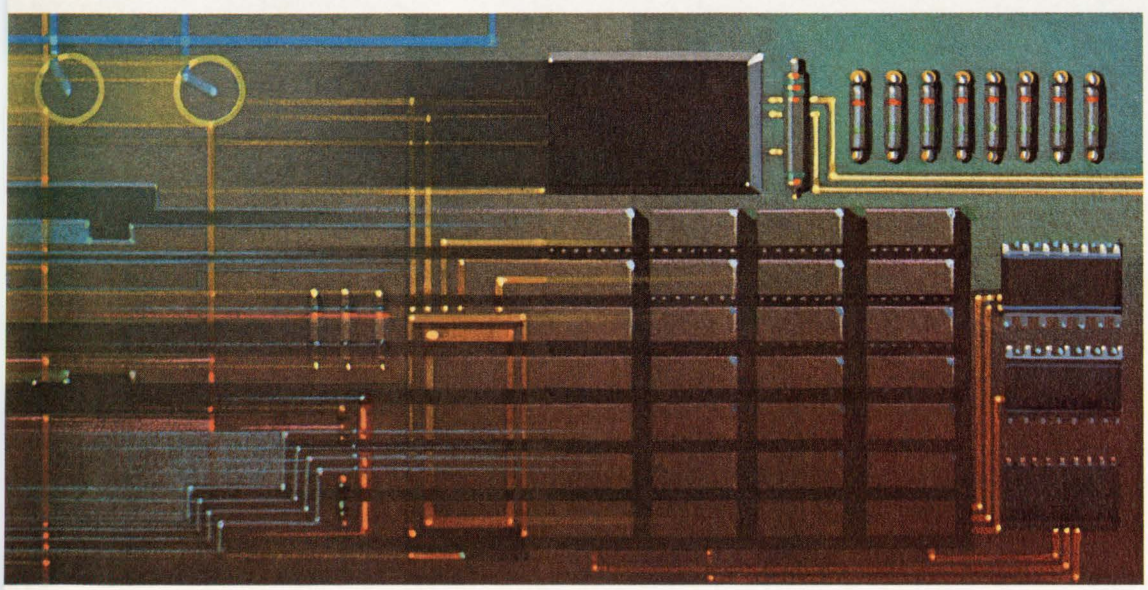

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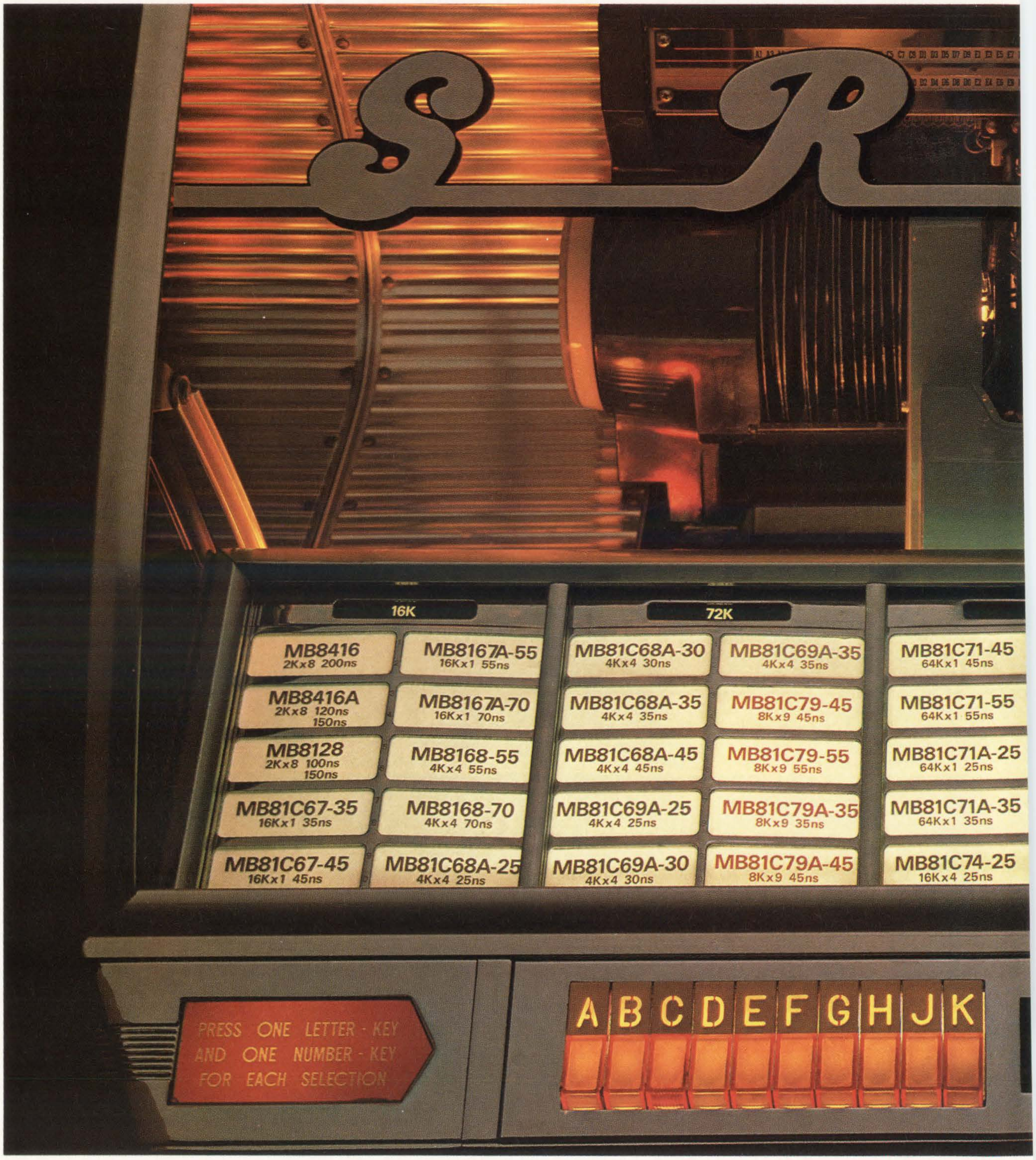

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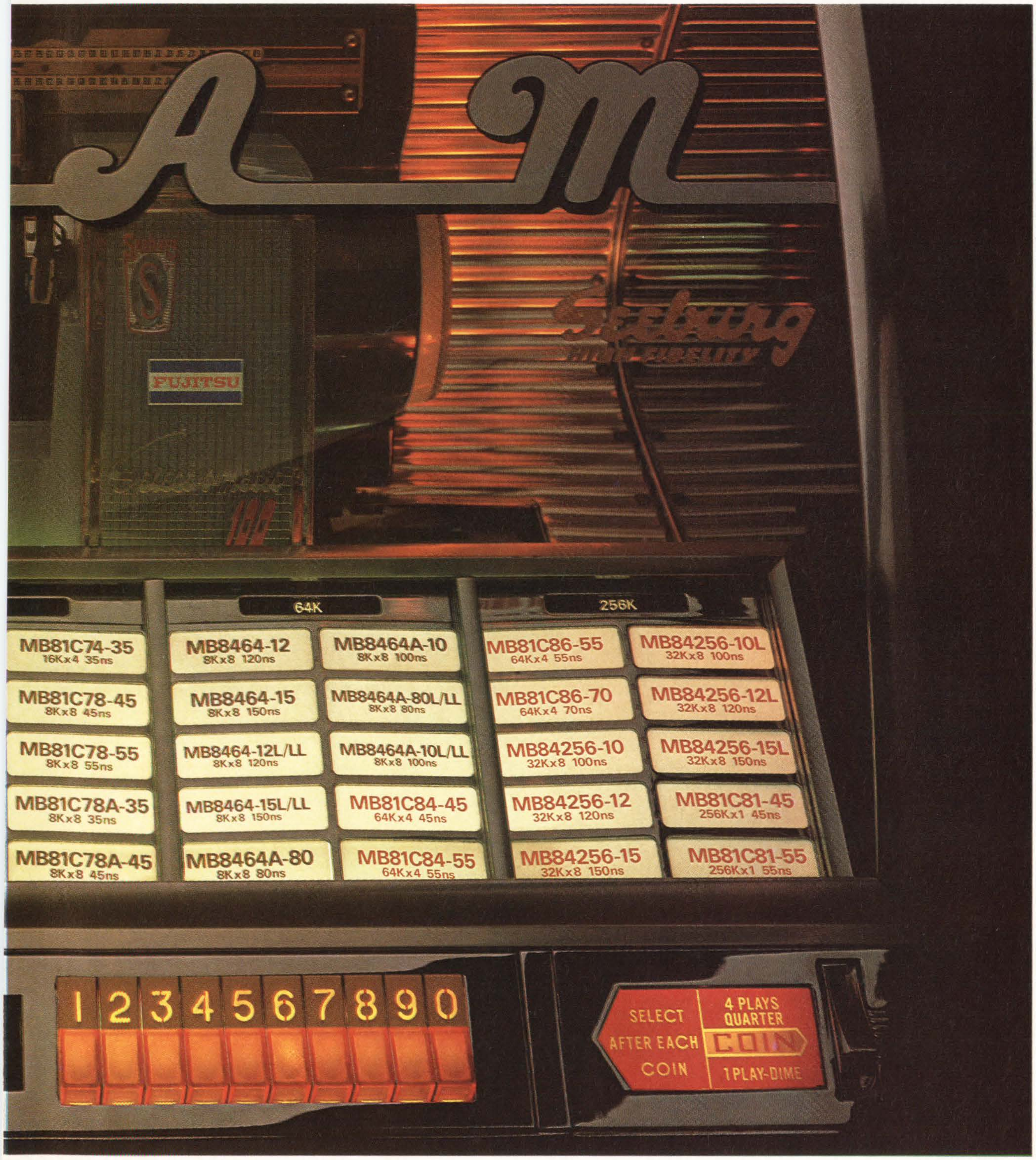

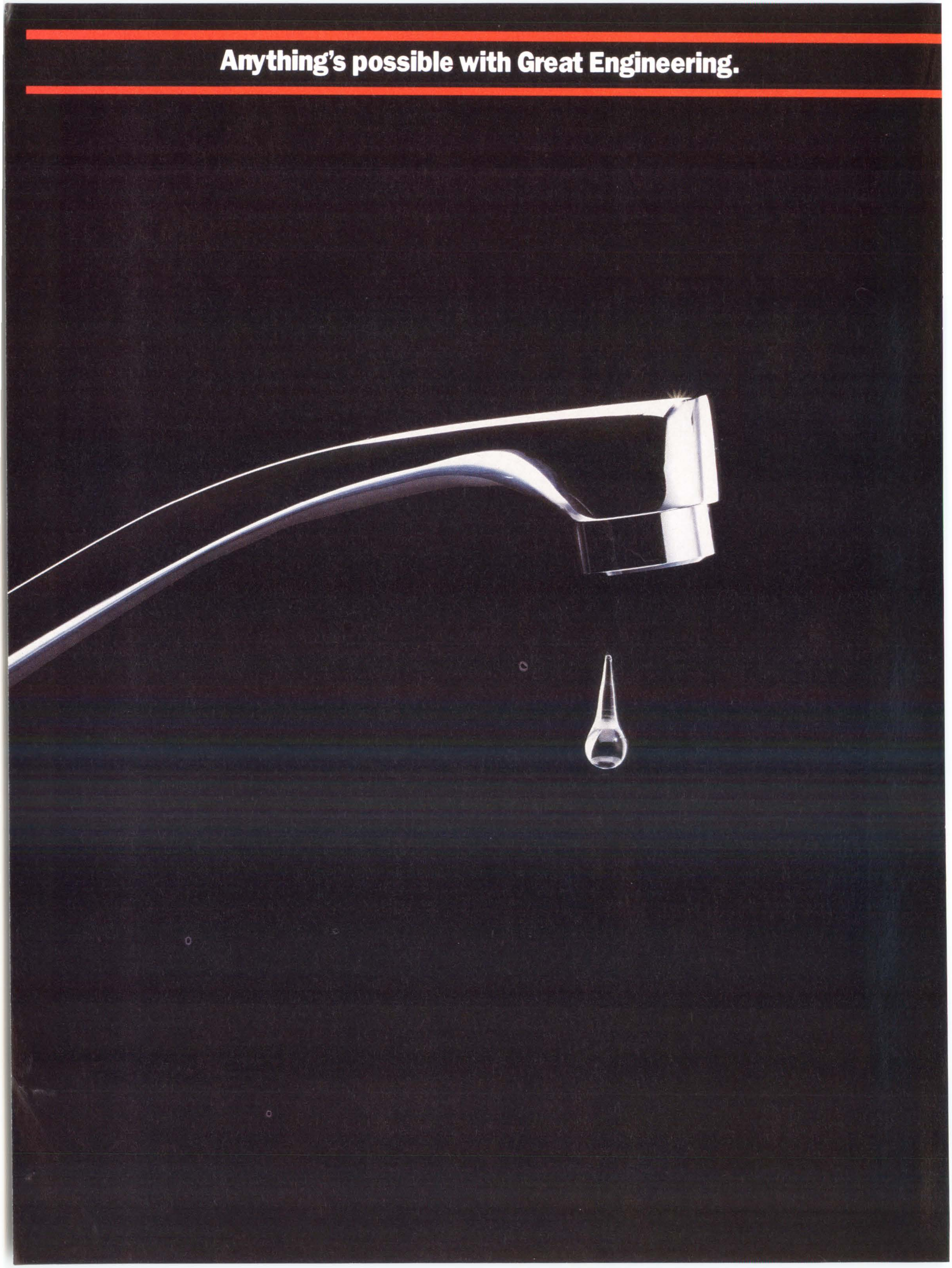
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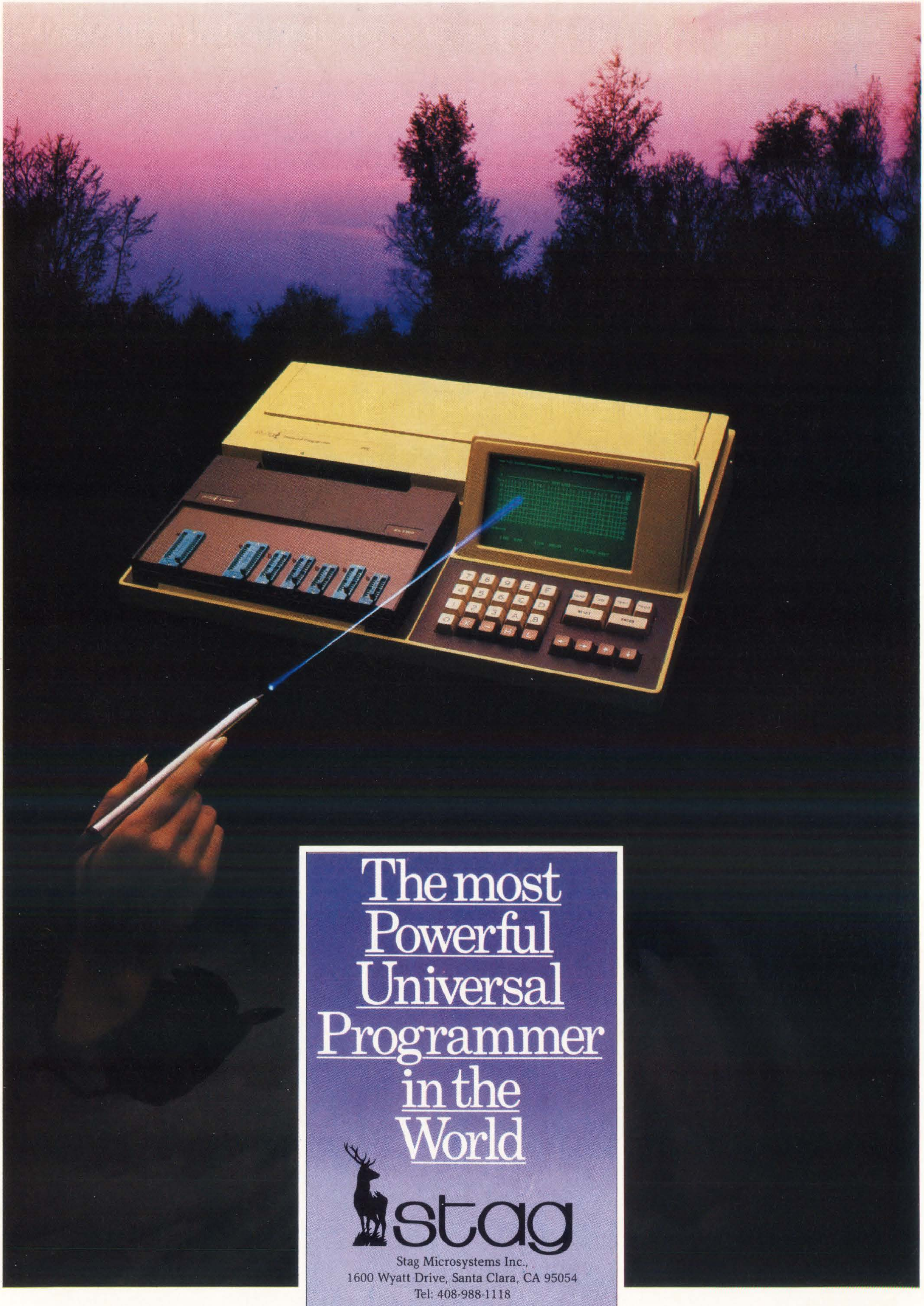
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NEWS BREAKS

EDITED BY JOAN MORROW

IBM PC COPROCESSOR BOARD PROVIDES TERMINAL EMULATION

The PC4100 graphics coprocessor board enables your IBM PC to run software written for the Enhanced Graphics Adapter (EGA) and the Color Graphics Adapter (CGA), as well as the Tektronix 4107 and 4105 color graphics terminals. Based on the programmable TMS34010 graphics engine, the board, from Tektronix Inc (Wilsonville, OR), has a resolution of 640×480 pixels in its initial version; a future version will have a resolution of 1024×768 pixels. In addition to its display memory, the board contains 1M bytes of RAM, which the TMS34010 can use for display list storage. (For more information on graphics engines, see the Special Report starting on pg 112.) The board requires the PLOT 10 PC-07 and PLOT 10 PC-05 software packages to emulate the 4107 and 4105 terminals, respectively. Available at the end of this month, the PC4100 board will cost less than $2000, the PLOT 10 PC-07 will be less than $1000, and the PLOT 10 PC-05 will be less than $500.—Margery S Conner

WINDOWING-STANDARD PROPOSALS EMERGING SLOWLY

On January 15, eleven companies announced support of X Window, a windowing system for multitasking computers developed by MIT. The companies include Adobe Systems Inc (Palo Alto, CA); Apollo Computer Inc (Chelmsford, MA); Data General Inc (Westborough, MA); Digital Equipment Corp (Maynard, MA); Hewlett-Packard Co (Palo Alto, CA); and Masscomp (Westford, MA). The support consists of the companies' promotion of X Window as the industry standard for graphics information display in networked systems; intercompany cooperation on X Window enhancements; pursuit of formal standardization by international standards organizations; and incorporation of X Window into new products. MIT supplies source code for the price of the media; X Window is an open, nonproprietary specification.

Sun Microsystems (Mountain View, CA), which introduced its News (network extensible window system) windowing specification for multitasking screen displays last year, plans to license source code to commercial vendors for $25,000 starting this month. Like X Window and the company's NFS file-interchange specification, Sun has placed the News specification in the public domain. Any company can implement News with proprietary software without paying a license fee. News, based on a subset of Adobe Systems' Postscript graphics description language, currently runs on Sun's 3/200 Series workstations, as does X Window. The company claims that News is a superset of X Window and that News therefore can run X Window-compatible applications.—Steven H Leibson

IN-PACKAGE TRIM TECHNIQUE IMPROVES OFFSET-VOLTAGE SPECS

A proprietary in-package trim technique allows Motorola (Tempe, AZ) to adjust the offset voltage of a quad op amp to 10 μV. The op amps are trimmed at the final test stage after they are packaged, thus, claims Motorola, avoiding the degradation in the offset spec commonly associated with the packaging process. The technique involves applying a current pulse to the trim resistors, which diffuses metal into the dielectric material of the IC and consequently reduces the resistance of the trim.—Jim Wiegand

STD BUS-BASED PERSONAL COMPUTER IS IBM PC/XT COMPATIBLE

The STD Bus-based System 2 from Pro-Log Corp (Monterey, CA, (408) 372-4593) offers IBM PC compatibility at the operating-system, BIOS, and chip-hardware levels. For example, some communication software written for the IBM PC will only work with a serial port implemented with an 8250; the System 2 employs this UART. The personal computer runs Microsoft's MS-DOS version 3.2, and it is rugged enough for industrial applications. You can also purchase the Model 7350 graphics/keyboard card that offers IBM PC-compatible CGA (Color Graphics Adapter), EGA (Enhanced Graphics Adapter), and monochrome operating modes. It interfaces to the standard IBM PC keyboard. With one 3½-in. floppy-disk drive, the NEC V20 μP, and 128k bytes of CMOS static RAM, the system sells for $1595.—Maury Wright

2400-BPS MODEMS SPORT ADAPTIVE ECHO CANCELLATION

Both internal (IBM PC bus) and external versions of Bizcomp Corp's (Sunnyvale, CA) 2400-bps Intellimodem 2400 cost $599. They provide adaptive echo cancellation, a feature the company claims improves sensitivity by a factor of four over competing adaptive equalization designs. Rather than relying on band-splitting filters to remove echos from the telephone line, the Intellimodem 2400 predicts the echo, inverts the predicted signal, and injects the resulting waveform into the line, thus cancelling the predicted echo signal through destructive interference. The modems also feature Hayes-compatible command sets and an internal expansion bus for future hardware enhancements.—Steven H Leibson

CMOS CONTROLLER CHIP HANDLES X.25 PACKET SWITCHING

The MK5025 from Thomson Components-Mostek Corp (Carrollton, TX, (214) 466-6000) uses on-chip DMA control with buffer management to transmit and receive X.25 packets through separate circulator queues, thus offloading your host CPU of all link-level operations. The device lets you achieve data rates to 7M bps. Manufactured in a 1.5-μm CMOS double-level metal process, the 5025 provides link-level data-communication control, a self-test feature, and loop-back test facilities. The chip includes programmable timers and counters and handles HDLC frame formatting—including zero-bit insertion and deletion, FCS generation and detection, and frame delimiting by flags. You can select the FCS as either 16 or 32 bits. A programmable option lets you manipulate XID, TEST, and UI frames. Packaged in a 48-pin DIP, the 5025 costs $55 (1000).—J D Mosley

MAP MODEM CARD PLUGS INTO IBM PC BUS

Compatible with existing Manufacturing Automation Protocol (MAP)/IEEE-802.4 network controllers, the M8024-P modem from Fairchild Data Corp (Scottsdale, AZ) plugs directly into an IBM PC or compatible computer's card slot and attaches to the MAP network through a rear-panel F connector. You can obtain the modem with either a standard, 40-pin connector compatible with network controllers from Industrial Networking Inc (Santa Clara, CA), or a 37-pin connector compatible with network controllers from Concord Data Systems (Waltham, MA). Beta-site units of the M8024-P will be available in June, and production is slated for August.—Steven H Leibson

BiCMOS 16k-BIT TTL-COMPATIBLE STATIC RAMs NOW AVAILABLE

The SSM6167 16k×1-bit and SSM6116 2k×8-bit BiCMOS static RAMs from Saratoga Semiconductor (Cupertino, CA, (408) 973-0945) are both available in two versions. You can order either IC in a standard power version with fast chip select, or in a power-down version that draws 20 mA in standby mode. Both devices come in 20-, 25-, and 35-nsec address access times. The SSM6167 specs 60-mA active power consumption and comes in a 20-pin DIP. The SSM6116 consumes 120 mA when active and comes in a 24-pin DIP. Prices range from $8.60 to $38.50 (100).—J D Mosley

CIRCLE NO 58

X-Y PLOTTER FURNISHES 17.7-IPS PLOTTING SPEED

The SPL-800 from Sekonic Co Ltd (Tokyo, TLX J34376) is an 8-pen X-Y plotter with a 17.7-ips plotting speed in each axis. The 32.3×12.5×41.3-in. device weighs 45 lbs, comes with both RS-232C and IEEE-488 interfaces, and provides 0.001-in. resolution. It also features 18k bytes of storage capacity and software compatibility with HP-GL commands. The plotter costs approximately $5000.—Joan Morrow

VOICE SCRAMBLER SECURES NETZ-C SPEECH TRANSMISSIONS

Meeting the requirements of the West German NETZ-C cellular-radio standard, the FX304 audio processor from Consumer Microcircuits Ltd (Witham, UK, TLX 99382) allows you to scramble speech transmissions by frequency inversion of the audio band. The IC has two identical channels, which you can use to scramble and unscramble transmitted and received speech signals respectively, permitting full-duplex operation. Each channel has separate control inputs to inhibit the frequency inversion and to disable the channel's output.

Based on switched-capacitor filters and balanced modulators, the device is clocked from a low-cost 4.43-MHz crystal. Unwanted modulation products and baseband breakthrough are at a level of better than −40 dB. The FX304 costs around £8 (1000).—Peter Harold

TWO-CHIP SET SUITS 1553B BUS CONTROLLER/TERMINAL APPLICATIONS

You can configure the MA3690 transceiver and the MA3691 terminal controller ICs from Marconi Electronic Devices Ltd (Lincoln, UK, TLX 56380) to operate together as a bus controller, a remote terminal, or a passive bus monitor in dual-redundant 1553B bus systems. The terminal controller features two modes of operation. In single-shot mode, you can control 1553B bus activity directly from the subsystem's processor; in table-driven mode, the terminal controller has sufficient intelligence to execute a sequence of bus control instructions contained in external ROM or RAM.

The terminal controller also features an extendable no-response timeout and an automatic retry facility to cope with bus errors. Programmable options that modify message sequences, redefine status bits, and alter the way flags are set and cleared allow you to tailor the chip set to suit different interpretations of 1553B bus protocol. Samples of the £890 (100) CMOS SOS chip set, approved to MIL-STD-883C, will be available in the second quarter of this year.—Peter Harold

KYOCERA TO MARKET AIDA's CAE TOOLS IN JAPAN

Kyocera Corp's LSI Design Div (Tokyo) and Aida Corp (Santa Clara, CA) have entered into a distribution agreement that licenses the Japanese company to market Aida's CAE workstation tools. Kyocera will offer design support and system-level simulation and testability tools. The products will be available in the Tokyo and Osaka design centers.—Joan Morrow

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	W424 4040 4X40	W424 105D 1X5D	W424 105B 1X5B	W424 1058	W424 1053	W424 1051
Polling Capability/Real Time Clock	●	●				
Enclosed in Metal Housing	●	●	●			
NEMA 12 or 4X Stainless Steel Bezel	●	●	●			
115/230 Volt Power Supply Included	●	●	●			
12 Volt Power Supply Required				●	●	●
Four Line x 24 Character Readout	●					
Single Line Readout (24 Characters)		●	●	●	●	●
64 Canned Messages in EPROM				●		
256 Canned Messages in CMOS RAM	●	●				
1/2" Characters Utilizing Gas Plasma Technology	●	●	●	●	●	●
RS232/RS422 and 20mA Outputs	●	●				
Full and Half Duplex Communication					●	
Accepts RS422 Serial ASCII Input	●	●	●			
Accepts RS232 & 20mA Serial ASCII Input	●	●	●		●	●
PC Software Available for Message Programming	●	●				
Accepts Parallel ASCII Input (TTL Logic Levels)	●	●	●		●	●
Recall Message with +5 to +30VDC Logic	●	●				

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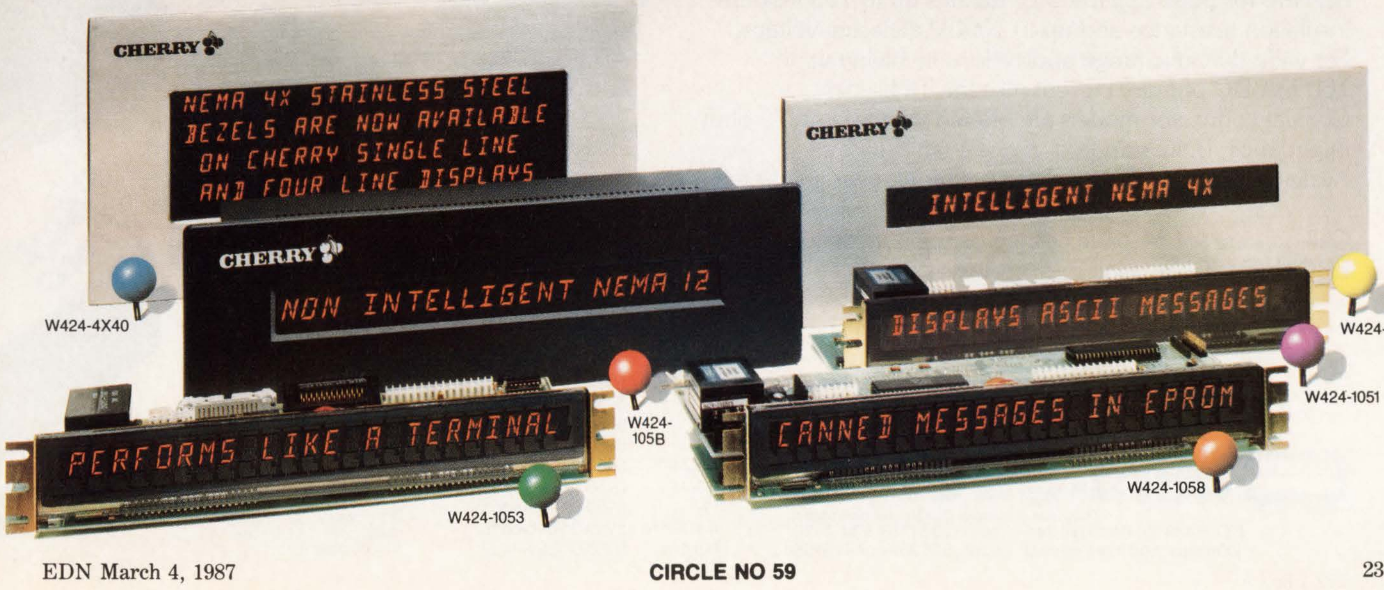
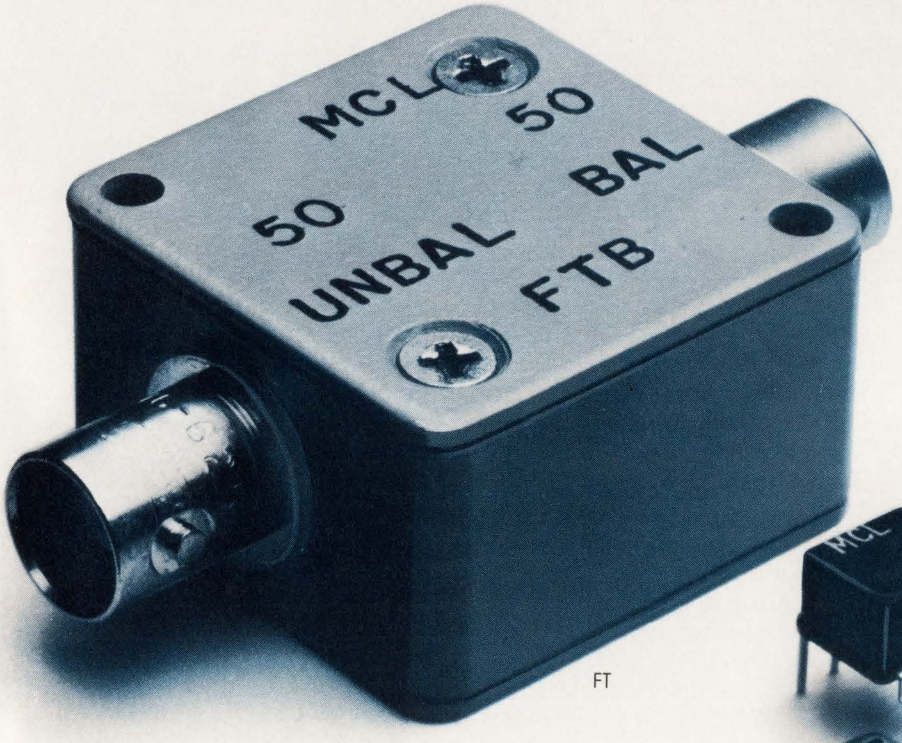


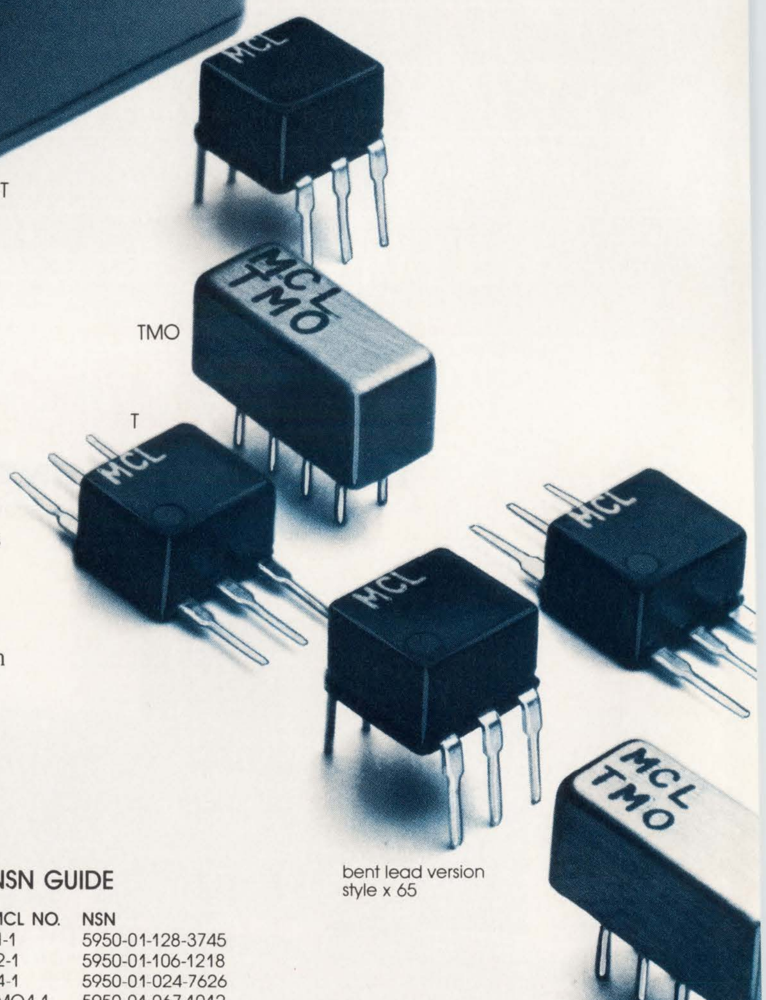
CIRCLE NO 59

RF trans

over 50 off-the-shelf models...



FT



TMO

T

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*units are not QPL listed

bent lead version
style x 65

NSN GUIDE

MCL NO.	NSN
T1-1	5950-01-128-3745
T2-1	5950-01-106-1218
T4-1	5950-01-024-7626
TMO4-1	5950-01-067-1012
TMO4-2	5950-01-091-3553
T9-1	5950-01-105-8153
TMO9-1A	5950-01-098-6315
T16-1	5950-01-094-7439

case styles

T, TH, case W 38, X65 Bent Lead Version
TMO, case A 11, † case B13
FT, FTB, case H 16

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C72-1 Rev. A

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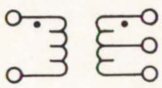
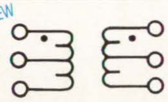
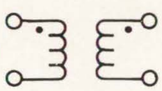
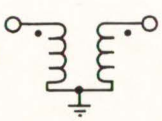
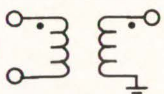
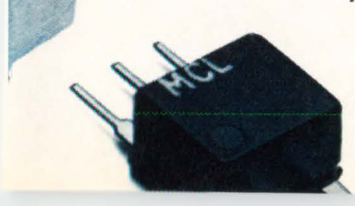
case style number see opposite page.		MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS 3dB MHz	2dB MHz	1dB MHz	PRICE $ Ea.	Qty.
A* PRI  SEC	T	T1-1T	1	.05-200	.05-200	.08-150	.2-80	3.95	(10-49)
		T1-6T NEW	1	.003-300	.003-300	.01-150	.02-50	5.95	(10-49)
		T2-1T	2	.07-200	.07-200	.1-100	.5-50	4.25	(10-49)
		T2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	4.25	(10-49)
		T3-1T	3	.05-250	.05-250	.1-200	.5-70	3.95	(10-49)
		T4-1	4	.2-350	.2-350	.35-300	2-100	2.95	(10-49)
		T4-6T	4	.02-250	.02-250	.05-150	0.1-100	3.95	(10-49)
		T5-1T	5	.3-300	.3-300	.6-200	.5-100	4.25	(10-49)
		T8-1T	8	.03-140	.03-140	.10-90	1-60	6.95	(10-49)
		T13-1T	13	.3-120	.3-120	.7-80	5-20	4.25	(10-49)
		T16-6T NEW	16	.03-75	.03-75	.06-30	.1-20	4.95	(10-49)
	TH	T4-1H	4	8-350	8-350	15-300	25-200	4.95	(10-49)
	TMO	TMO1-1T	1	.05-200	.05-200	.08-150	.2-80	6.45	(10-49)
		TMO2-1T	2	.07-200	.07-200	.1-100	.5-50	6.75	(10-49)
		† TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	6.75	(10-49)
		† TMO3-1T	3	.05-250	.05-250	.1-200	.5-70	6.45	(10-49)
		TMO4-1	4	.2-350	.2-350	.35-300	2-100	4.95	(10-49)
		TMO5-1T	5	.3-300	.3-300	.6-200	5-100	6.75	(10-49)
		TMO13-1T	13	.3-120	.3-120	.7-80	5-20	6.75	(10-49)
B* NEW PRI  SEC	TT	TT1-6	1	.004-500	.004-500	.02-200	.1-50	5.95	(10-49)
		TT1.5-1	1.5	.075-500	.075-500	.2-100	.1-50	4.95	(10-49)
		TT2.5-6	2.5	.01-50	.01-50	.025-25	.05-10	5.25	(10-49)
		TT4-1	4	.05-200	.05-200	.02-50	1-30	4.95	(10-49)
		TT25-1	25	.02-30	.02-30	.05-20	.1-10	7.95	(10-49)
	TTMO	TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	10.95	(10-49)
C PRI  SEC	T	T1-1	1	.15-400	.15-400	.35-200	2-50	2.95	(10-49)
		T1-6 NEW	1	.01-150	.01-150	.02-100	.05-50	4.95	(10-49)
		T1.5-1	1.5	.1-300	.1-300	.2-150	.5-80	3.95	(10-49)
		T1.5-6 NEW	1.5	.02-100	.02-100	.05-50	0.1-25	4.95	(10-49)
		T2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	3.95	(10-49)
		T4-6	4	.02-200	.02-200	.05-150	.1-100	3.95	(10-49)
		T9-1	9	.15-200	.15-200	.3-150	2-40	3.45	(10-49)
		T16-1	16	.3-120	.3-120	.7-80	.5-20	3.95	(10-49)
		T36-1	36	.03-20	.03-20	.05-10	.1-5	5.95	(10-49)
	TH	T1-1H	1	8-300	8-300	10-200	25-100	4.95	(10-49)
		T9-1H	9	2-90	2-90	3-75	6-50	5.45	(10-49)
		T16-1H	16	7-85	7-85	10-65	15-40	5.95	(10-49)
	TMO	TMO1-1	1	.15-400	.15-400	.35-200	2-50	4.95	(10-49)
		TMO1.5-1	1.5	.1-300	.1-300	.2-150	.5-80	6.75	(10-49)
		† TMO2.5-6	2.5	.01-100	.01-100	.02-50	.05.20	6.45	(10-49)
		† TMO4-6	4	.02-200	.02-200	.05-150	.1-100	6.45	(10-49)
		TMO6-1	6	.3-200	.3-200	.5-150	5-50	6.45	(10-49)
		TMO9-1	9	.15-200	.15-200	.3-150	2-40	6.45	(10-49)
		TMO1.6-1	16	.3-120	.3-120	.7-80	5-20	6.45	(10-49)
D PRI  SEC	T	T2-1	2	.025-600	.025-600	.05-400	.5-200	3.45	(10-49)
		T3-1	3	.5-800	.5-800	.2-400	—	4.25	(10-49)
		T4-2	4	.2-600	.2-600	.5-500	.2-250	3.45	(10-49)
		T8-1	8	.15-250	.15-250	25-200	2-100	3.45	(10-49)
		T14-1	14	.2-150	.2-150	.5-100	2-50	4.25	(10-49)
	TMO	TMO2-1	2	.025-600	.025-600	.05-400	.5-200	5.95	(10-49)
		TMO3-1	3	.5-800	.5-800	2-400	—	6.95	(10-49)
		TMO4-2	4	.2-600	.2-600	.5-500	2-250	5.95	(10-49)
		TMO8-1	8	.15-250	.15-250	.25-200	2-100	5.95	(10-49)
		TMO14-1	14	.2-150	.2-150	.5-100	2-50	6.75	(10-49)
E PRI  SEC	FT	FT1.5-1	1.5	.1-400	.1-400	.5-200	1-100	29.95	(1-4)
	FTB	FTB1-1	1	.2-500	.2-500	.5-300	10-100	29.95	(1-4)
		FTB1-6	1	.01-125	.01-125	.05-50	.1-25	29.95	(1-4)
		■ FTB1-1-75	1	.5-500	.5-500	5-300	10-100	29.95	(1-4)



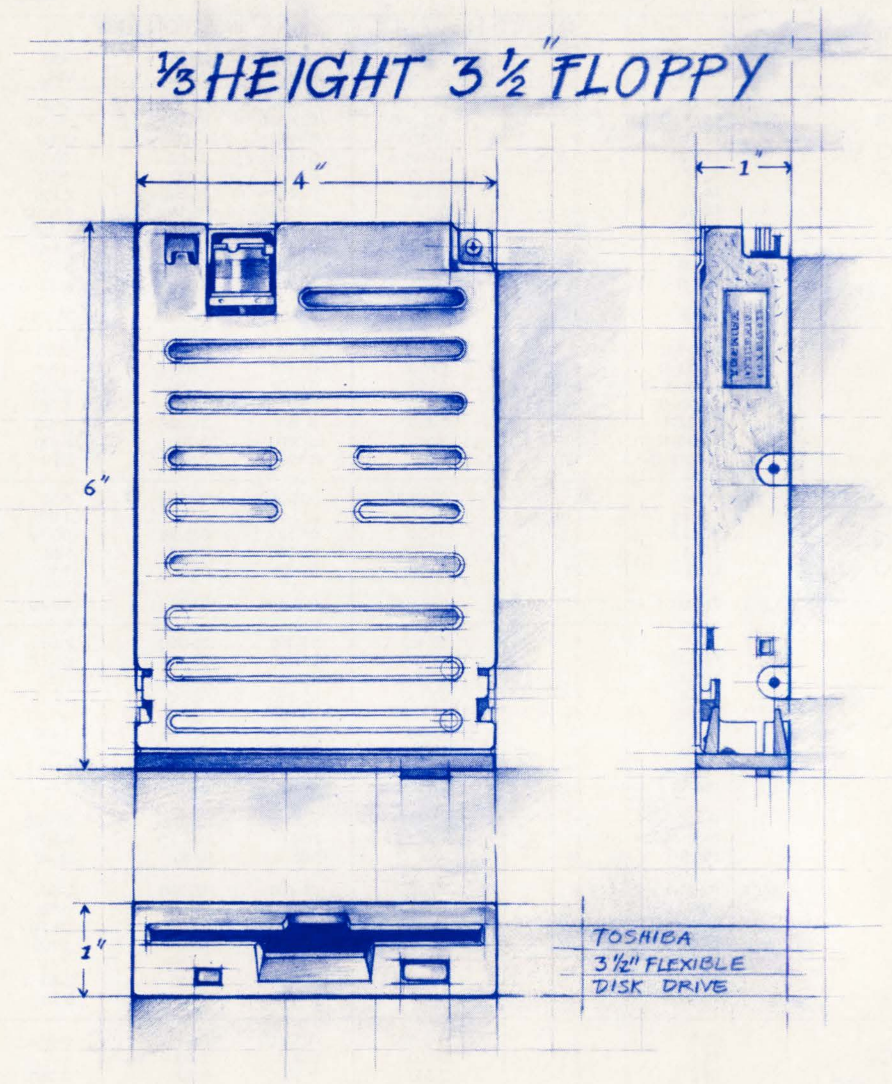
■ Denotes 75 ohm models

* Maximum Amplitude Unbalance
0.1 dB over 1 dB frequency range
0.5 dB over entire frequency range

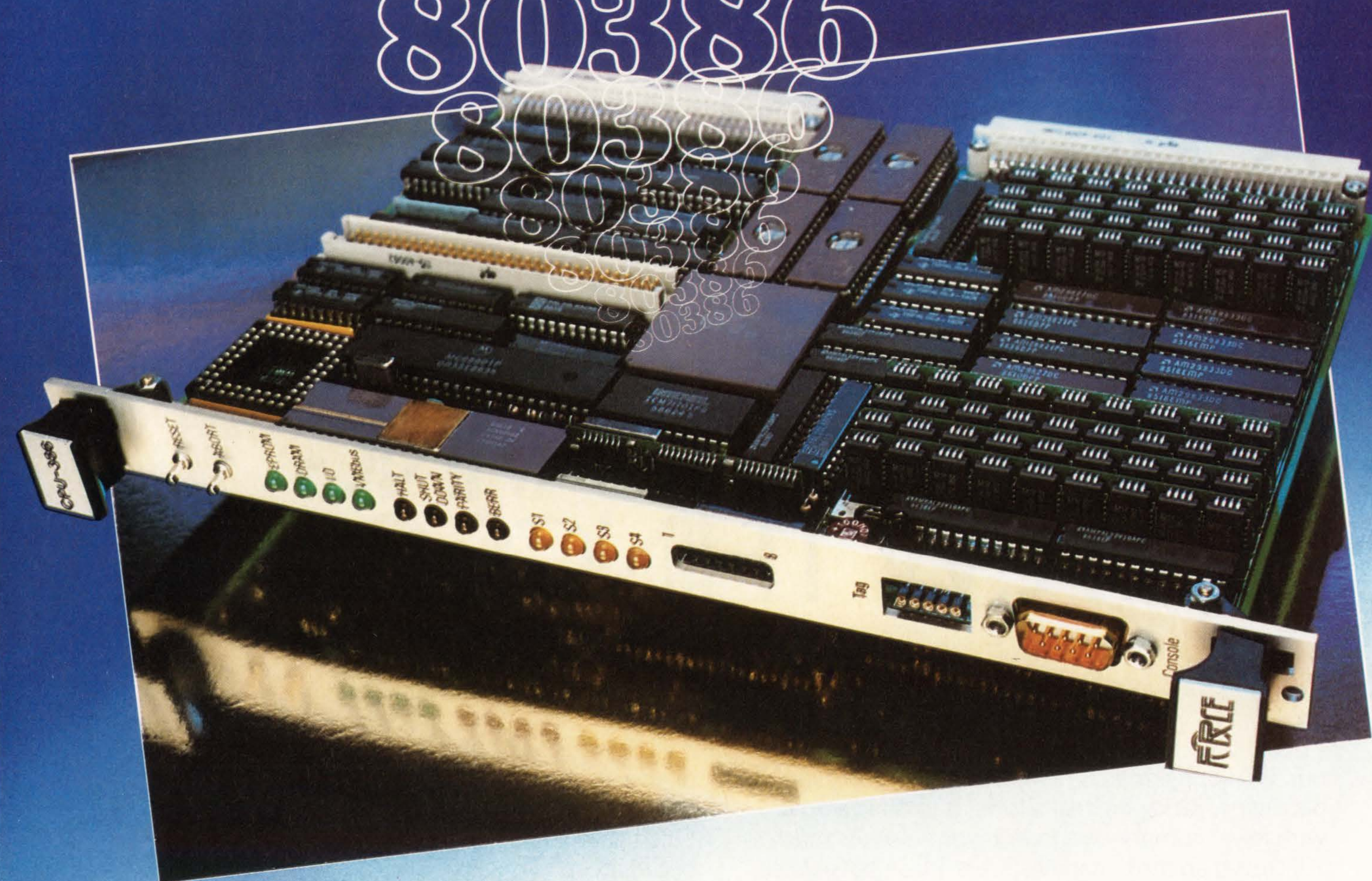
* Maximum Phase Unbalance
1.0° over 1 dB frequency range
5.0° over entire frequency range

CIRCLE NO 92

C72-2 Rev. A


⅓ HEIGHT 3½" FLOPPY
4"
1"
6"
1"
TOSHIBA
3½" FLEXIBLE
DISK DRIVE

80386 or



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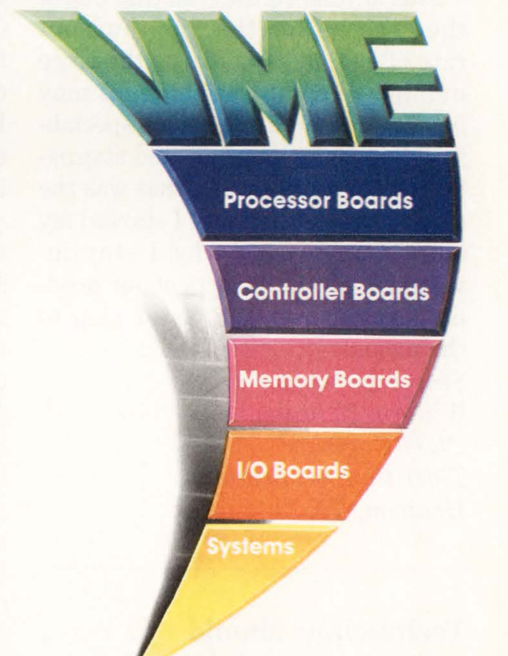
Force 32 bit CPU Availability

	CPU-20	CPU-21	CPU-24	CPU-25	CPU-386A	CPU-386B
Processor	68020*	68020*	68020*	68020*	80386*	80386*
Available frequencies	12.5/16.7/20/25	12.5/16.7/20/25	12.5/16.7/20	12.5/16.7/20	12/16/20	12/16/20
Number of wait states	0	0	1	1	0 (1 at 20 MHz)	
FPU	no	yes	no	yes	no	yes
MMU	no	no	yes	yes	yes	yes
Memory capacity	0.5 to 4 MB SRAM		0.5 to 4 MB SRAM		2 to 8 MB DRAM	
EPROM capacity	512 KB	512 KB	64 KB	64 KB	256 KB	256 KB
Serial I/O channels	3	3	3	3	3	3

68020 ?



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CIRCLE NO 71

SIGNALS & NOISE

High specialization leads to stagnation

Dear Editor:
I say a loud "Amen" to the comments of Philip Mandel and Fred Chitayat (Signals & Noise, EDN, November 13, 1986, pg 33). The walls that seem to exist between analog and digital design are artificial.

One example of the falseness of these walls can be found in the design of high-speed digital circuits, where the lessons of analog RF design (about transmission-line effects, for example) very much come into play.

I do believe that putting people into the little boxes of high specialization is a bad trend: Look what has happened to medicine. After a long drift toward extreme specialization, the medical profession is finally starting to recognize the worth of the general practitioner. I wonder how long it will take the engineering profession to wake up.

Has anyone considered that one of the reasons for the high burnout rate of engineers (and also the large number of company-hoppers) may be that the high degree of specialization leads to boredom and stagnation? I can tell you that that was the case for me. That's why I started my own company and why I stay involved in all the aspects of our product design, from the power plug to the output.

Sincerely yours,
William H Bowen
Chief Engineer
Tiger Communications
Houston, TX

"SURE, BUT THOSE AREN'T MY FIGURES. THEY'RE THE FIGURES OF SOMEONE WHO KNOWS WHAT HE'S TALKING ABOUT."

Technicians should earn associates' degrees

Dear Editor:
Matthew Slate's letter entitled "The technician syndrome" (EDN, November 27, 1986, pg 29) raised some excellent points.

My studies at the University of Texas at Dallas covered the future job market and qualifications for technicians. The main problem is that, in the past, many technicians came from poor training programs in the military or in trade schools. Most firms will no longer accept technicians who received their training only in the military, as an article in *The Wall Street Journal* (October 9, 1985) points out. Further, the book *Career Education in Colleges* (Harris and Grede, Jossey-Bass Publishers, 1977) states that trade-school programs are of very low quality.

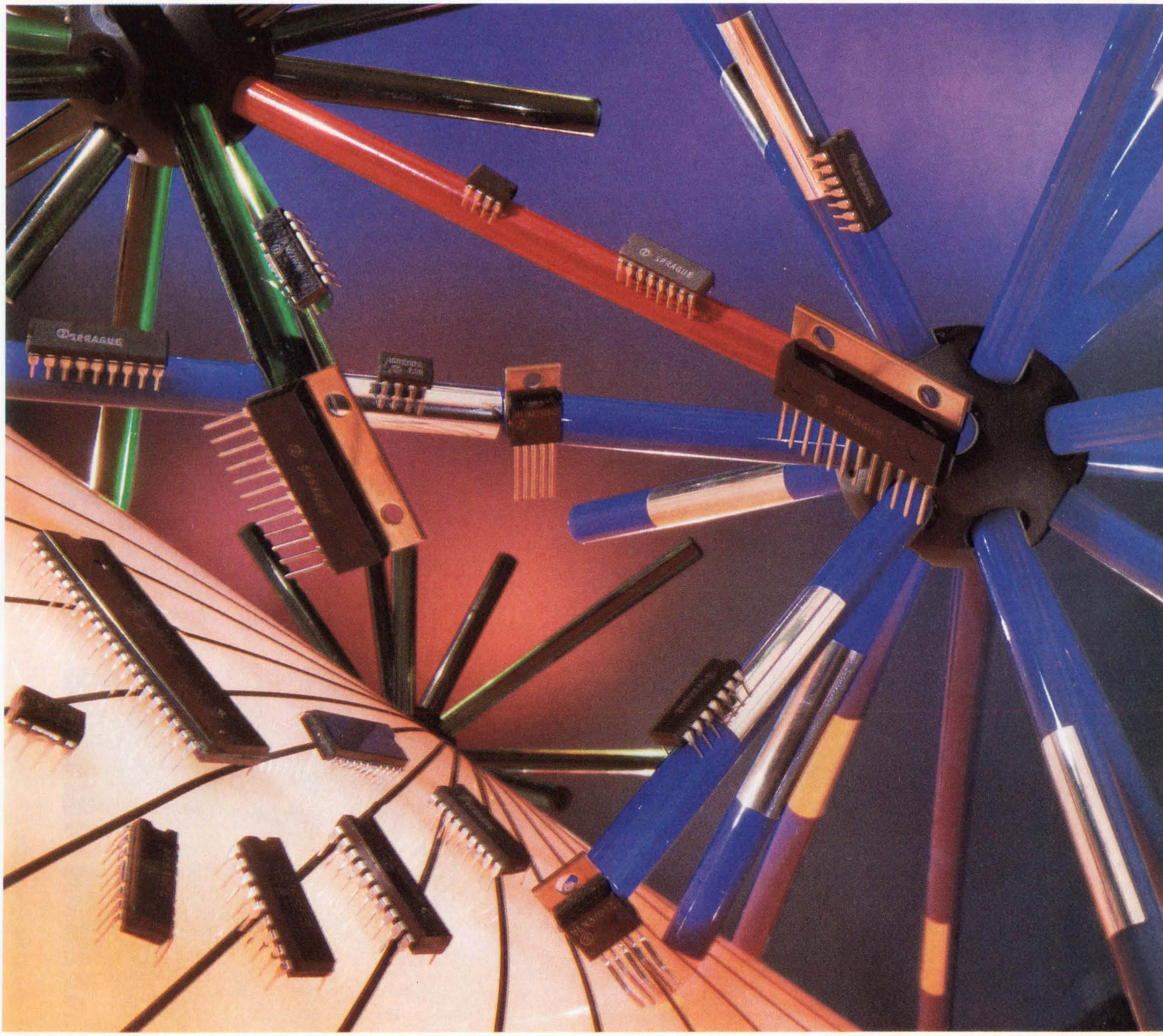
Community colleges now offer associate's degree programs of study in microprocessor systems, laser optics, and robotics. Several studies recommend that firms now require the associate's degree to enter the profession. More technicians should be hired, and their positions should be upgraded to a higher professional level, where their advanced training can be better utilized.

Sincerely yours,
Glen Spielbauer
Dallas, TX

Multiplexer limits 1's-complement data

Dear Editor:
I'd like to correct two errors that

POWER MANAGEMENT.



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Sprague Electric Company, a Penn Central unit, World Hdqtrs., Lexington, MA. For additional information, write for Brochures WR-181, WR-189, WR-195, WR-202, and WR-203 to Technical Literature Service, Sprague Electric Co., 41 Hampden Rd., P.O. Box 9102, Mansfield, MA 02048-9102.

SPRAGUE
THE MARK OF RELIABILITY

CIRCLE NO 5

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Every time.

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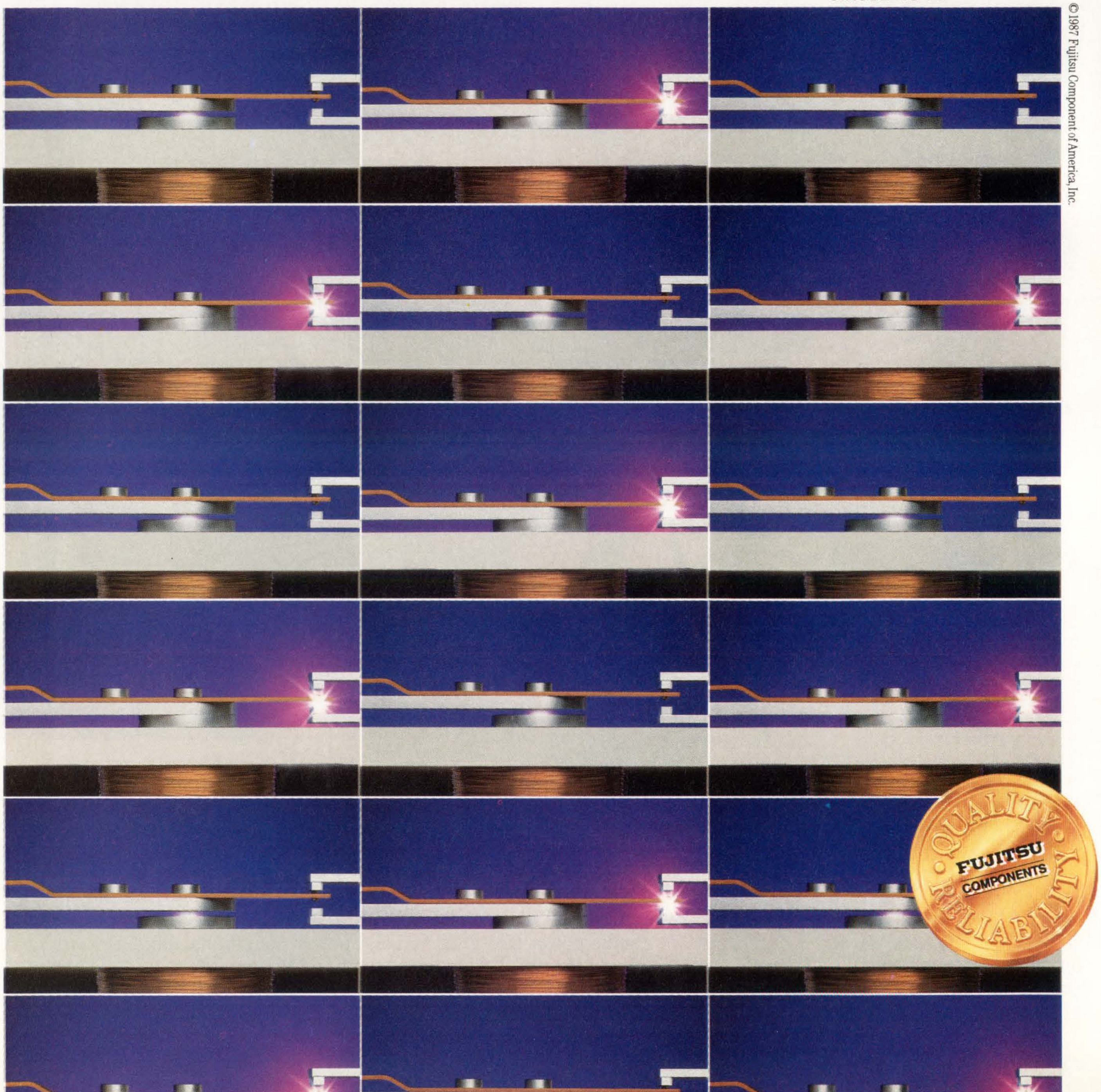
CIRCLE NO 72



crept into the published version of my Design Idea, "Multiplexer limits complement data" (EDN, October 30, 1986, pg 202). First, in an 8-bit, 2's-complement data word, the maximum positive value is only 127, not 128. In the article, therefore, readers should substitute +127 for +128.

Second, **Fig 1**'s circuit works *without any modification* for 1's complement data as well. The modification explained in the last paragraph is for limiting unsigned (straight positive binary) data.

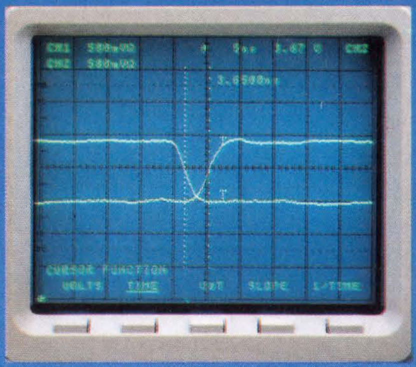
Sincerely yours,
S Murugesan
ISRO Satellite Centre
Department of Space
Government of India
Bangalore, India

Productive software

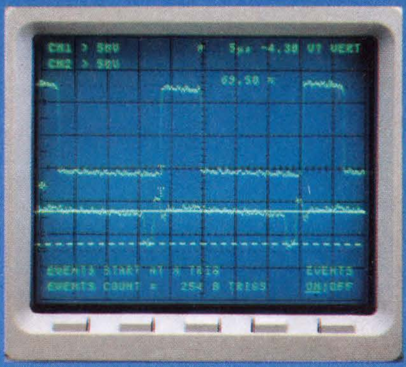
In the paragraph on the Hewlett-Packard DACQ/300 software package in EDN's New Products section (October 2, 1986, pg 267), we erroneously stated that the software can reduce the engineer's program-development time by a factor of 100. Not so. Says H-P: "Would that we could increase our customers' productivity by a factor of 100. Alas, all we can do is reduce the development time by 50%."

YOUR TURN

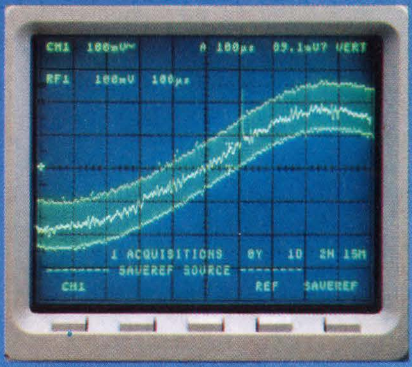
EDN's Signals and Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.



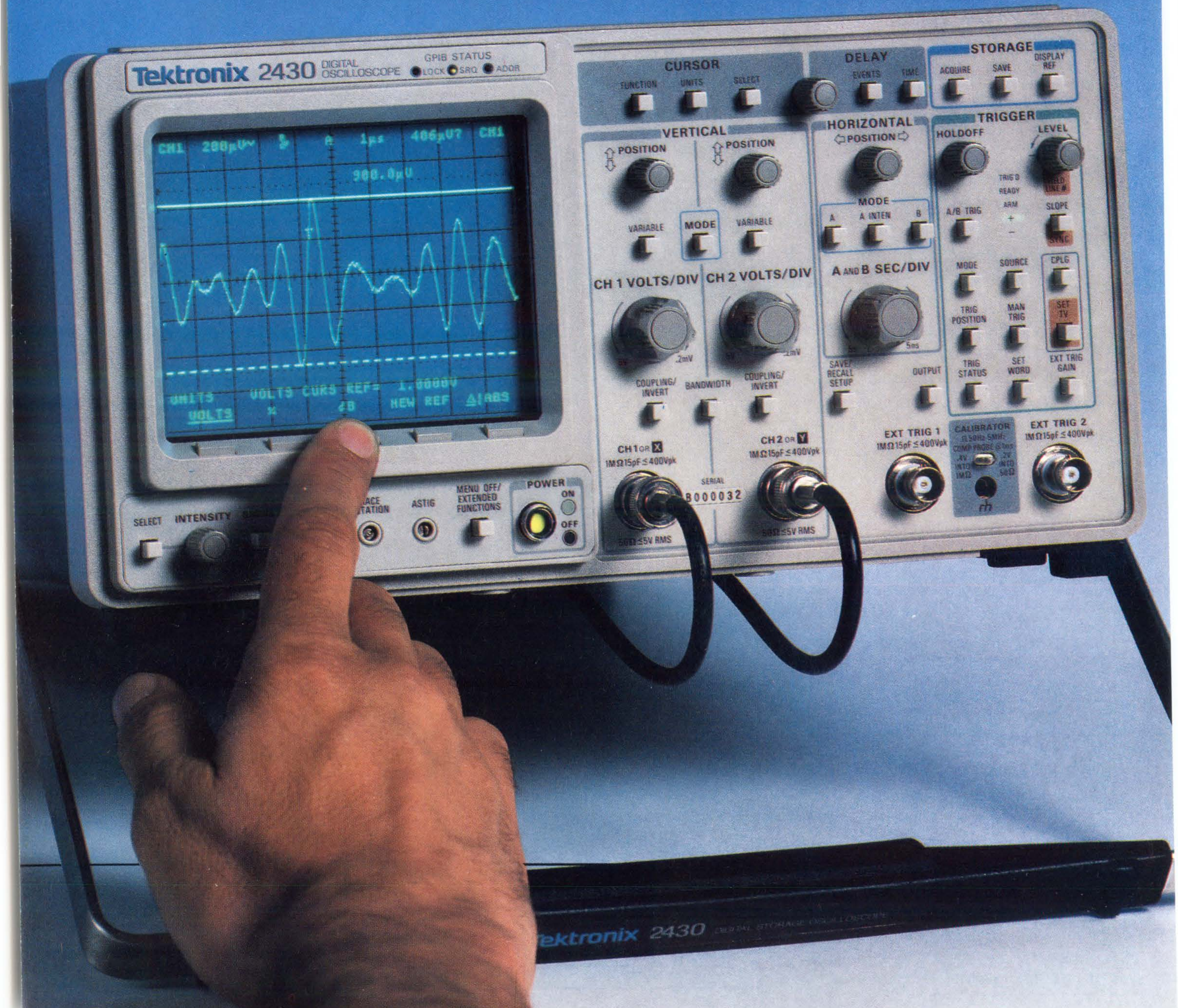
With its 150 MHz bandwidth, 5 ns/div maximum sweep speed and 2-channel simultaneous acquisition, the 2430 displays TTL and ECL signals for risetime and coincidence measurements. (Above) The scope is used in 50 ohm input termination with a 500 ohm probe for an accurate measurement of propagation delay through an ECL inverter.



How long does it take a transformer to reach operating voltage? Using DELAY BY EVENTS, the 2430 lets you select the 254th (or any other) switching event of the pulse-width modulator in a high-efficiency power supply.



A new Tek patented feature, SAVE ON DELTA instructs the 2430 to compare incoming acquisitions against a user defined reference and save it in the event of a difference. You can catch intermittent failures automatically and implement automatic tests with improved repeatability.



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It is also fully programmable via the GPIB. Complete talk/listen capabilities extend the scope's power and make it a valuable systems component for making automatic measurements. You can develop test procedures that can be used later on the manufacturing floor. Plus, the time-consuming task of waveform characterization, analysis and logging is simplified.

In addition, the 2430 can store waveforms and front panel setups in nonvolatile memory.

The 2430 exhibits unusual power as a troubleshooting tool. The patented peak detection circuit lets you capture glitches as narrow as 2 ns at any sweep speed with confidence—a level of performance available until now in only the most expensive instruments.

The 2430's envelope mode, which automatically captures and updates signal minimums and maximums, allows you to conveniently study signal variations such as jitter, drift and stability. It also monitors signal excursions outside user-defined limits.

Plus, a broad range of pretrigger selections available in all modes makes it possible to examine conditions leading up to an event. The crystal-controlled timebase allows you to delay by time and/or events for precise timing measurements in complex triggering modes. You can even trigger on digital words.

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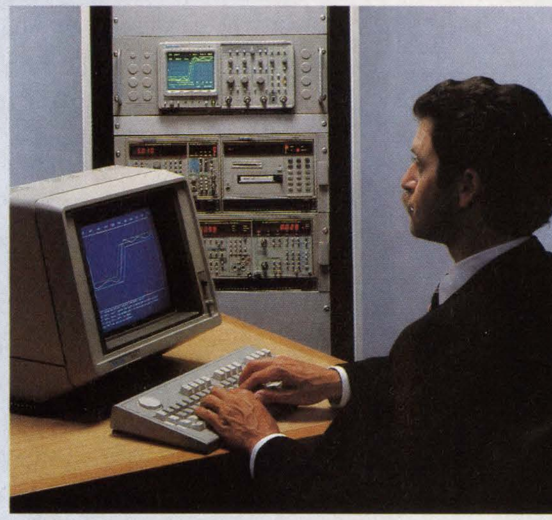

With full programmability you can improve repeatability and throughput—and reduce operator interface requirements.

The enhanced capabilities of the 2430's time and voltage cursors are another convenience, enabling you to make accurate measurements of all essential parameters.

The reliability of the 2430 is underwritten with a 3-year warranty. A variety of low-cost service plans can extend this coverage even further.

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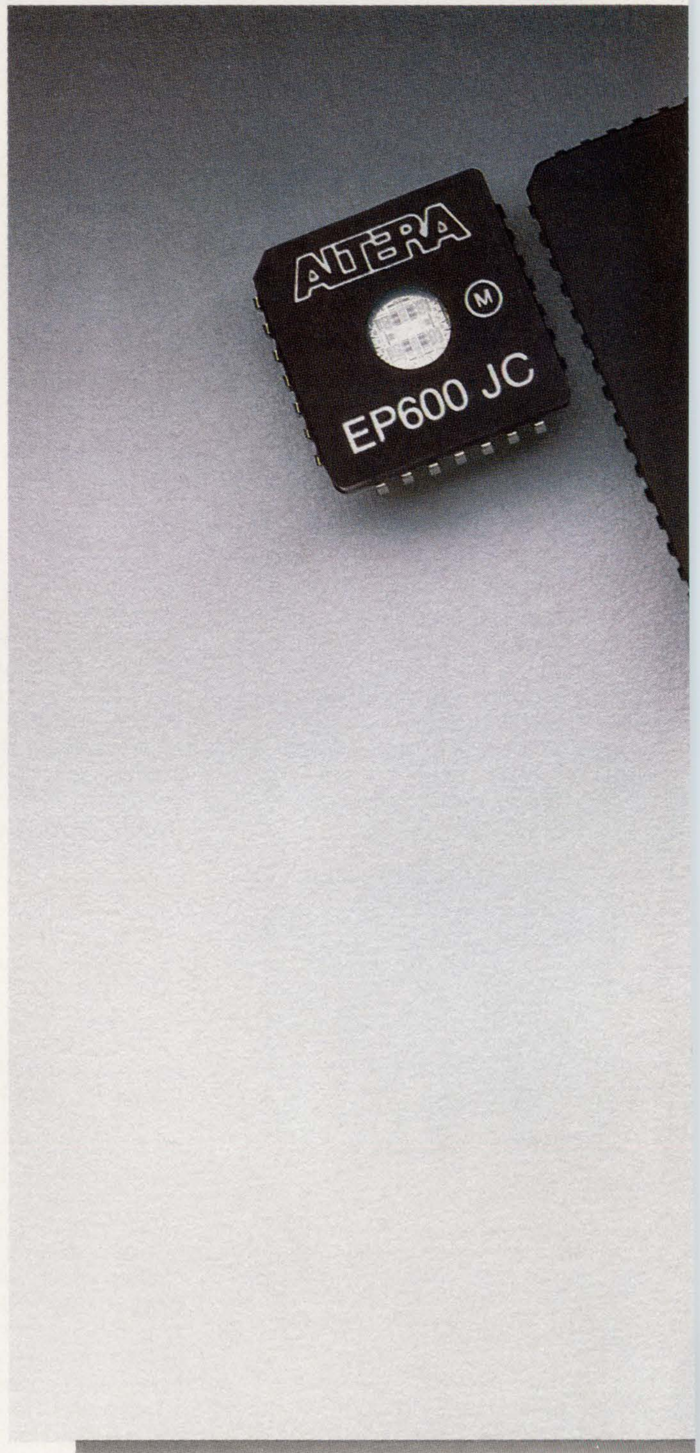

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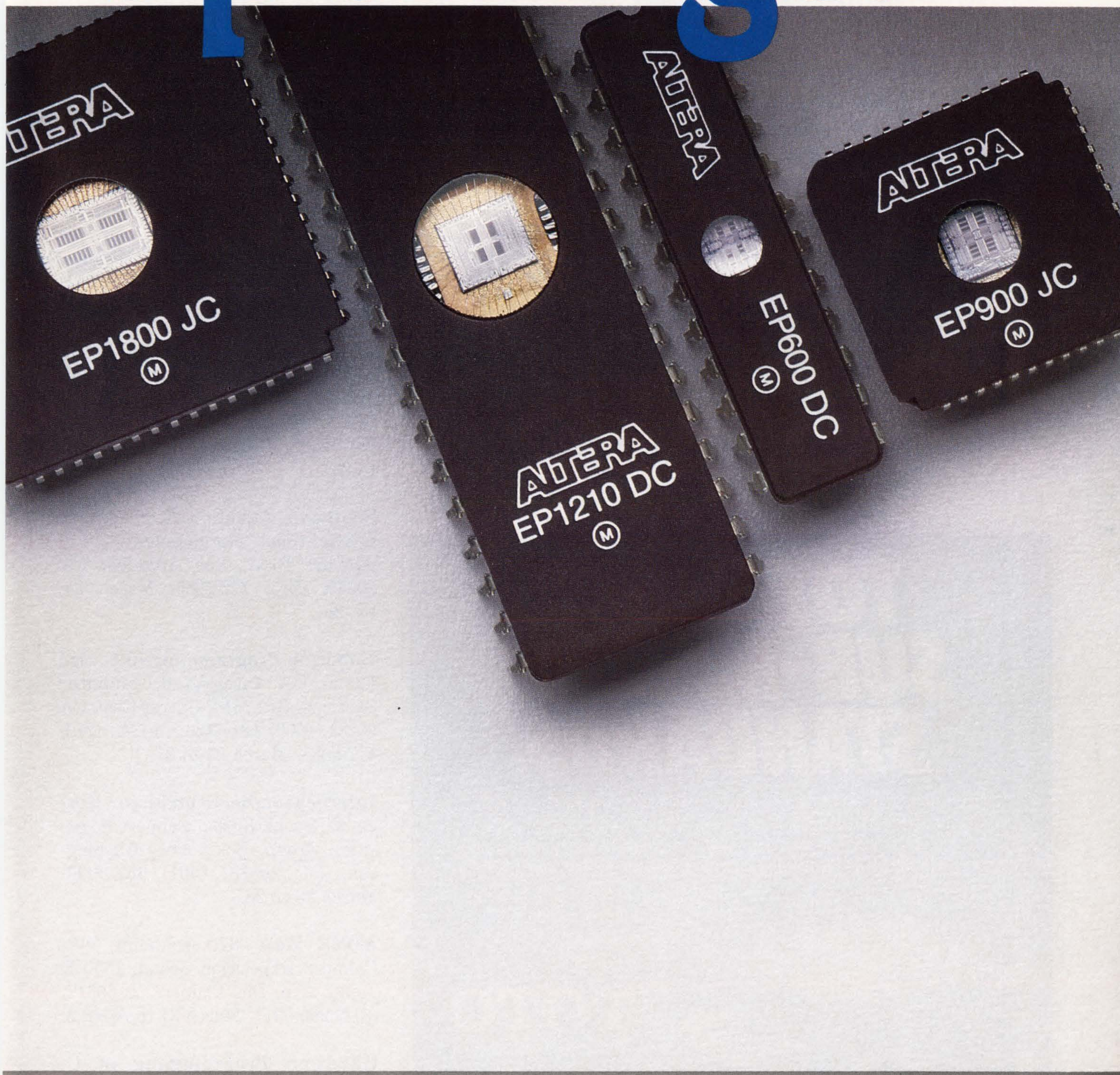
Openings.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Hands-on Programming in C, Boston, MA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. March 17 to 20.

Real-time Operating Systems: A Hands-on Workshop, Palo Alto, CA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. March 17 to 20.

Computer Graphics '87, Philadelphia, PA. National Computer Graphics Association, 2722 Merrilee Dr, Suite 200, Fairfax, VA 22031. (703) 698-9600. March 22 to 26.

IEEE VLSI Test Workshop, Atlantic City, NJ. Wesley Radcliffe, IBM, East Fishkill Facility, Bldg 321-5E1, Dept 277, Hopewell Junction, NY 12533. (914) 894-4346. March 24 to 25.

Southcon, Atlanta, GA. Electronic Conventions Management, 8110 Airport Blvd, Los Angeles, CA 90045. (213) 772-2965. March 24 to 26.

Hands-on Programming in C, San Diego, CA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. March 24 to 27.

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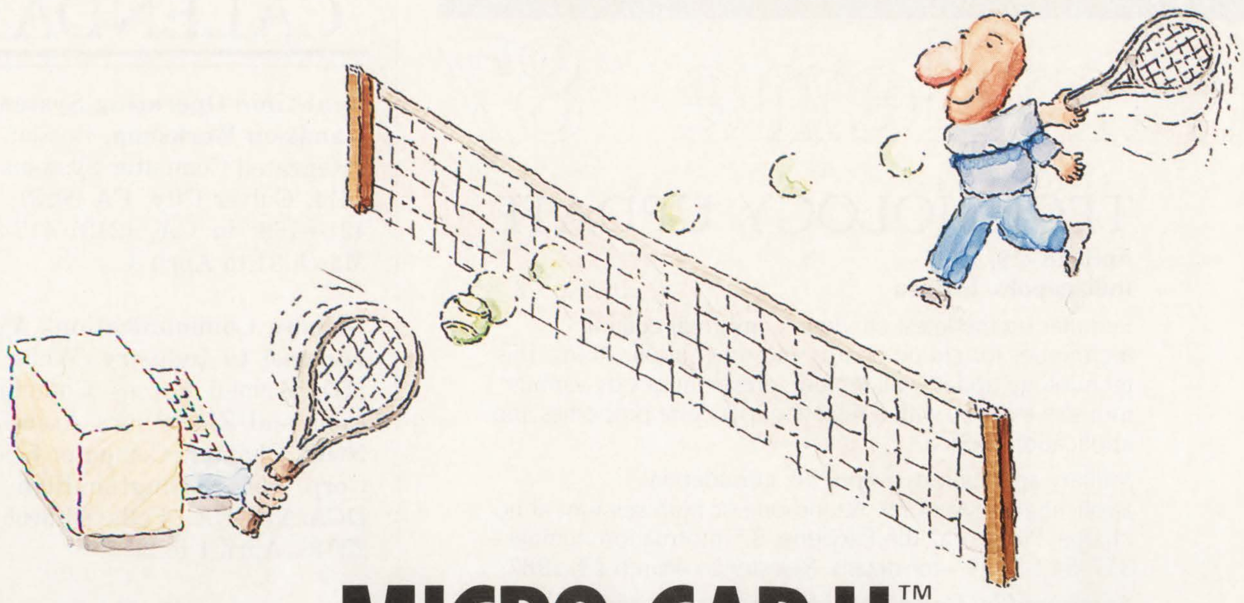
ADEE West '87, Anaheim, CA. Cahners Exposition Group, 1350 E Touhy Ave, Des Plaines, IL 60017. (312) 299-9311. March 31 to April 2.

Hands-on Programming in C, Washington, DC. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. March 31 to April 3.



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CALENDAR

Real-time Operating Systems: A Hands-on Workshop, Boston, MA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. March 31 to April 3.

Defense Communications Agency Forecast to Industry, White Oak, MD. Armed Forces Communications and Electronics Association NOVA Chapter, Computer Sciences Corp, 6565 Arlington Blvd, M/C DCA/AFCEA, Falls Church, VA 22046. April 1 to 2.

Microtronics '87, Hannover, West Germany. Hannover Fairs USA, Box 7066, Princeton, NJ 08540. (609) 987-1202. April 1 to 8.

Invitational Computer Conference, Nashua, NH. B J Johnson & Associates, 3151 Airway Ave, #C-2, Costa Mesa, CA 92626. (714) 957-0171. April 2.

Conference on Human Factors in Computing Systems and Graphics Interface, Toronto, Canada. Wendy Walker, Conference Coordinator, Computer Systems Research Office, University of Toronto, 10 Kings College Rd, Rm 2002, Toronto, Ontario, Canada M5S 1A4. (416) 978-5184. April 5 to 9.

Electro/Mini Micro Northeast, New York, NY. Electronic Conventions Management, 8110 Airport Blvd, Los Angeles, CA 90045. (800) 421-6816; in CA, (800) 262-4208. April 7 to 9.

Nepcon Southeast, Orlando, FL. Cahners Exposition Group, Box 5060, Des Plaines, IL 60017. (312) 299-9311. April 7 to 9.

Annual Electrical Overstress Exposition, San Jose, CA. EOE, 2504 N Tamiami Trail, Nokomis, FL 33555. (813) 966-9521. April 21 to 23.

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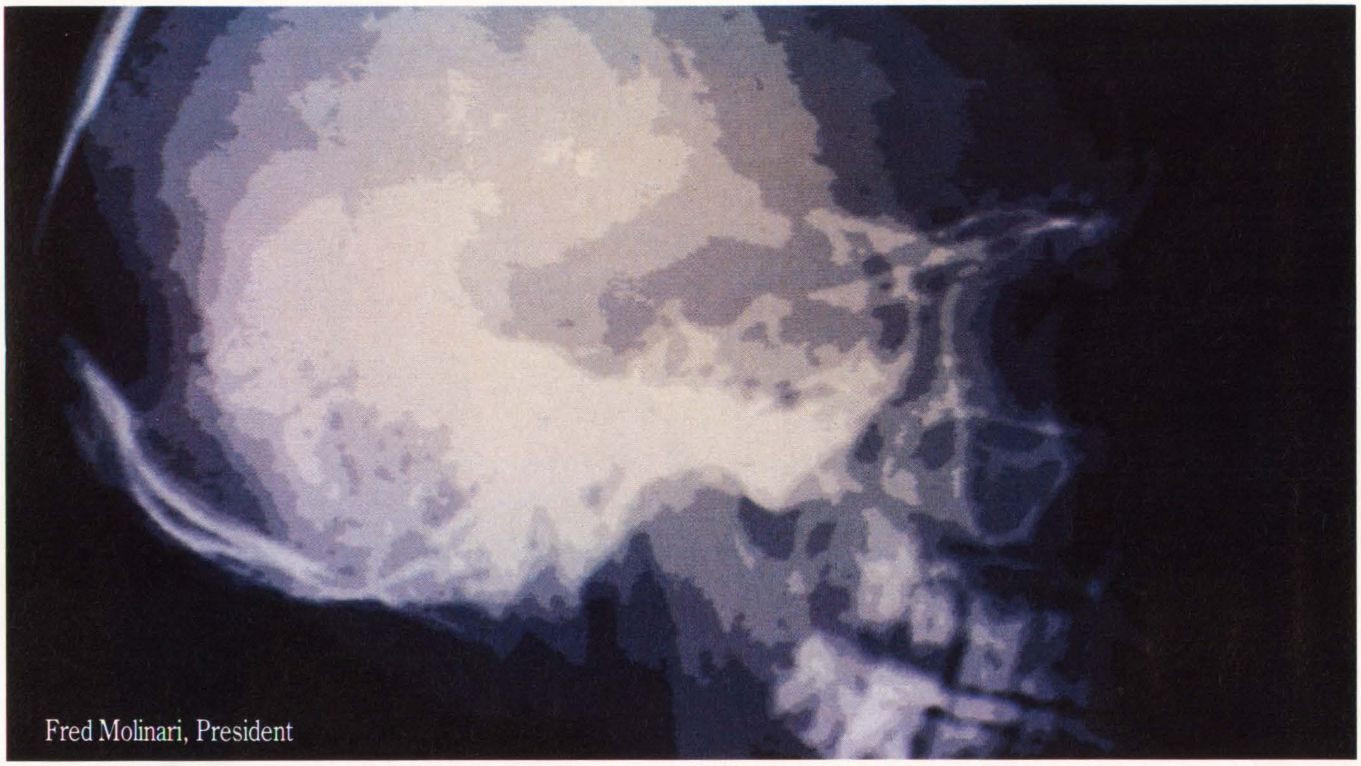

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DT2651 High Res. Frame Grab and DT2658 Aux. Frame Proc.	512x 512	256	✓	✓	✓	4	✓	✓	2 Buffers 512x512x8 (512 KB) and 1 Buffer 512x512x16 (512 KB)	✓	✓	✓	DT-IRIS ($1995)	$2995 $1895

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CIRCLE NO 8

EDITORIAL

We still need the artists

This page has previously contested the suggestion that computers and software can make it unnecessary for humans to master basic writing skills (see EDN, October 16, 1986, pg 53). This issue's cover story, on graphics ICs, makes a similar warning appropriate for graphics-arts skills. No matter how powerful today's graphics engines, the artist must possess the same degree of knowledge and the same planning skills as a writer who uses a word processor, or as an electrical engineer who uses CAE tools.

Consider, for example, this issue's cover. To implement the concept of a winged figure bursting out of a graphics-display controller chip, the cover's designer, David Hamby, required five basic shapes—a torso, leg, wing, head, and chip. Although an illustrator could have roughly sketched each shape in a few minutes, Hamby needed to draw each shape to scale in both front and side views. Each view (some of the digitizing sketches drawn by Hamby are reproduced beginning on pg 112) included 3-dimensional digitizing points accurate to 1/1000th of an inch. The complete design required more than 2400 such points.

You may wonder what advantage lies in generating the illustration with a computer. Although the concept sketch showed the figure in a front view, Hamby thought the front view was a bit boring when he saw the computer display it. By quickly changing software parameters, he was able to rotate the figure and the wings separately from the chip. Likewise, it was fairly easy to change the figure from polished bronze to blued aluminum. At first the wings were orange, which was fine for the bronze figure, but it clashed horribly with the blue. Again, modifying software parameters let Hamby change the color. Hamby was similarly able to adjust the figure to accommodate the wishes of EDN's editorial and art staffs.

Hamby's efforts are something that no computer could duplicate. As Hamby's work shows, a designer's basic skill is a necessary part of using the computer's capabilities.

Margery Conner

Margery Conner
Regional Editor

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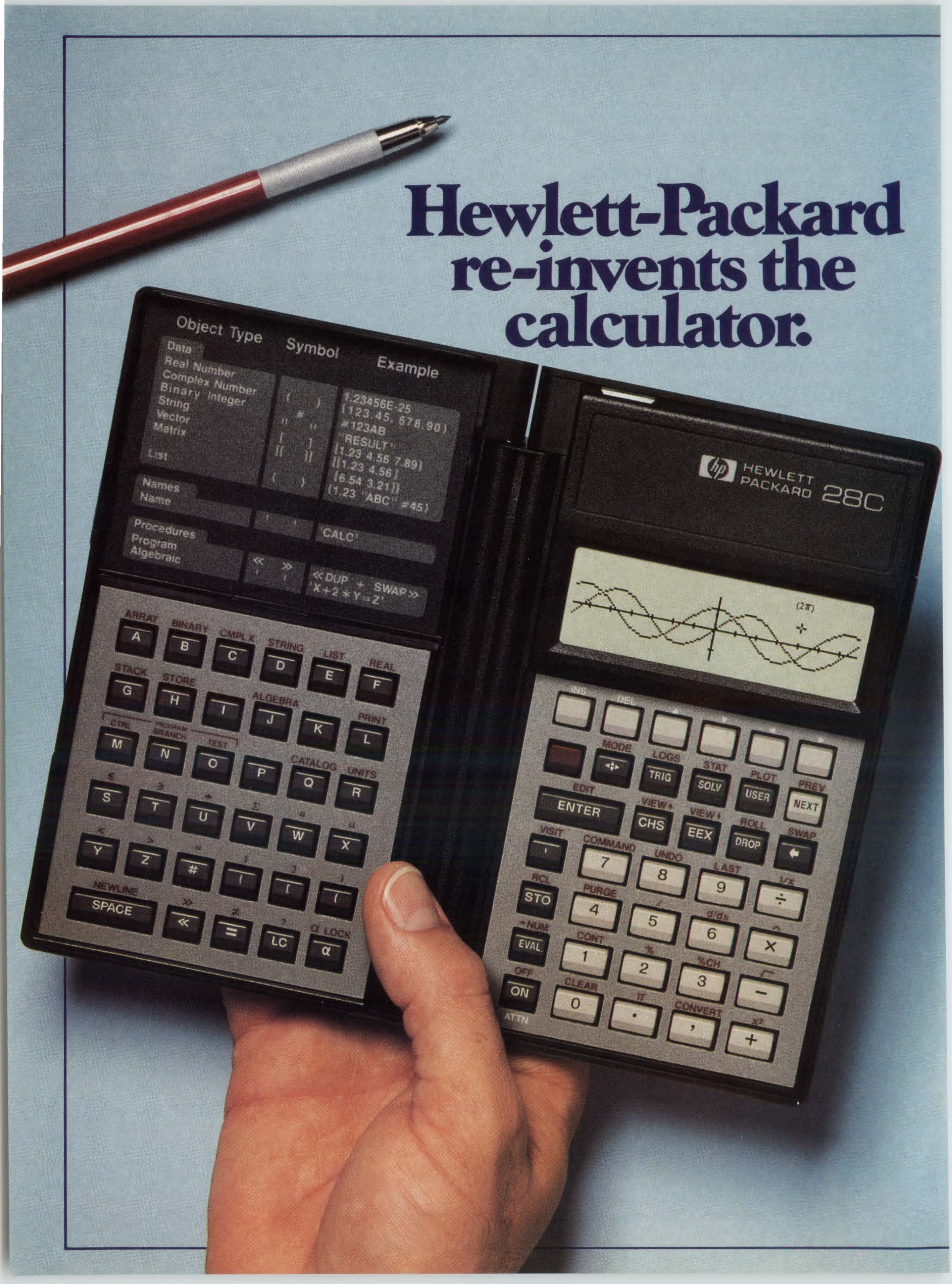
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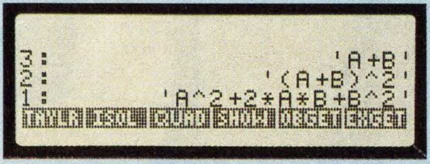

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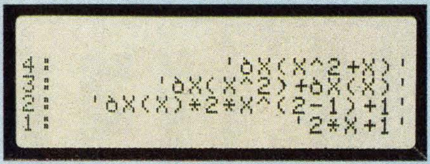

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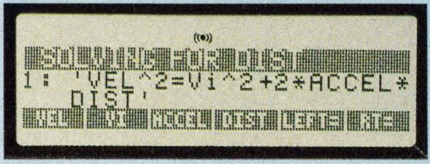

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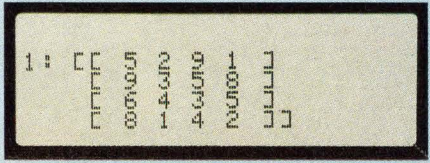

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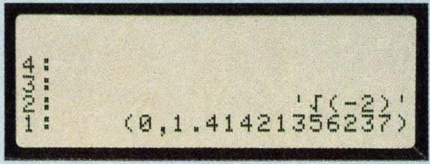

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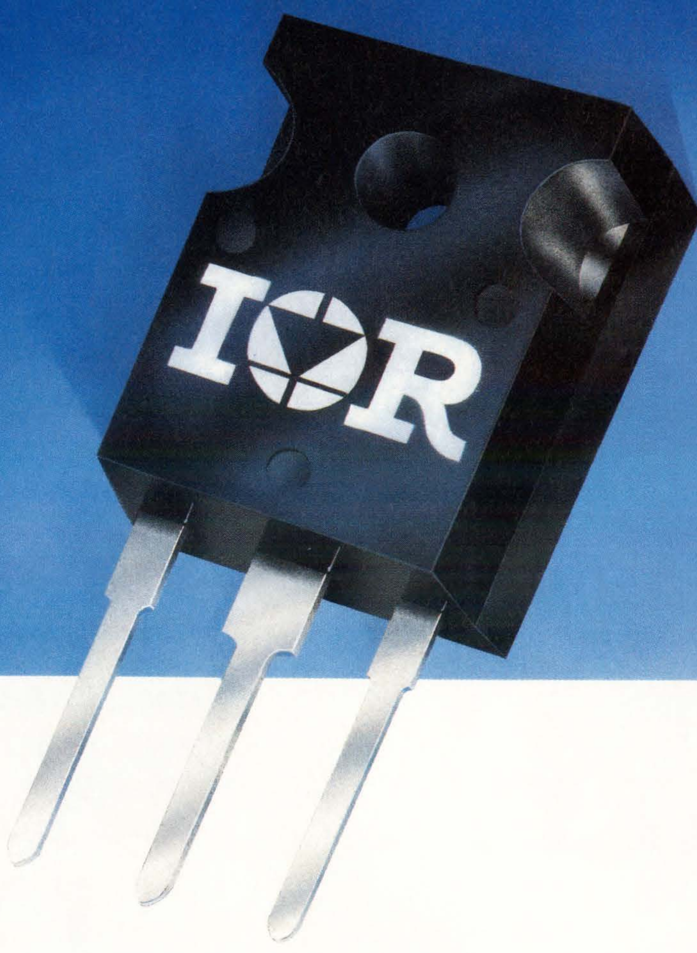

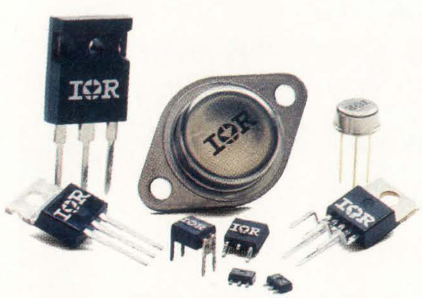

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CIRCLE NO 82

Add-in facsimile boards enable users of PCs to transfer CAE graphics in real time

Chris Terry, *Associate Editor*

With the advent of compression/expansion processor ICs, manufacturers of add-in boards for IBM PCs are now making fax expansion boards that permit you to use your personal computer as a fax machine for sending graphics over the telephone lines.

For more than 10 years, facsimile machines have used compression algorithms that allow the transmission of an 8½×11-in. page of text and images over the PSTN (Public Switched Telephone Network) in less than one minute. These algorithms conform to the CCITT's (Consultative Committee for International Telegraphy and Telephone) set of recommended standards and yield compression ratios between 5:1 and 50:1, depending on image characteristics.

Until recently, though, the hardware capable of performing these image-compression and -expansion algorithms had to be implemented in MSI logic and discrete components. It was complex, expensive, and uneconomical except in dedicated fax machines.

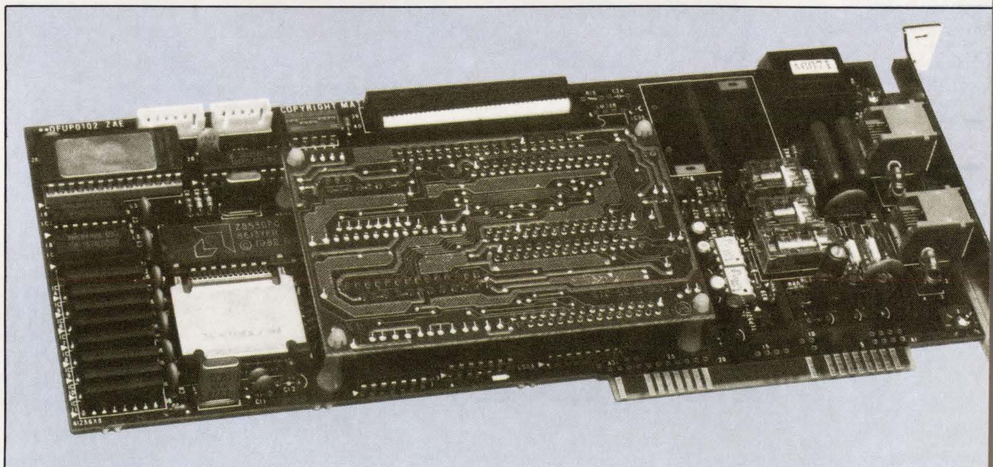
Now, VLSI compression/expansion processors (CEPs) contain all the logic needed to implement the CCITT algorithms in a single chip. All these VLSI CEPs embody CCITT group 3 algorithms, which remove horizontally and (optionally) vertically redundant information and yield a minimum resolution of 100 lines/in. Most CEPs can also perform compression/expansion according to CCITT group 4 algorithms, which provide a 2-D compression mode and a resolution of 400 pixels/in. in both directions.

One-dimensional horizontal compression consists of calculating a line-length value that represents the number of pixels of the same color (black or white) in a scan line across the document. The variable-length Huffman code that the algorithm uses to represent run lengths assumes that each line starts with a white pixel; if, in fact, the line starts with a black pixel, the first code has to be a zero-length line of white pixels.

Two-dimensional compression uses a modified relative-element address-designate (READ) code, based on the relative position of color changes in the previous scan line, which serves as a reference. When a color change lies exactly below the same color change in the reference line, a single bit serves to encode this fact. If the new color change is no more than three pixels to the left or right of the change in the reference line, the offset is represented by the READ code. If the offset is more than three pixels, the algorithm requires that a special code be sent and that the offset distance then be represented as a 1-D Huffman code.

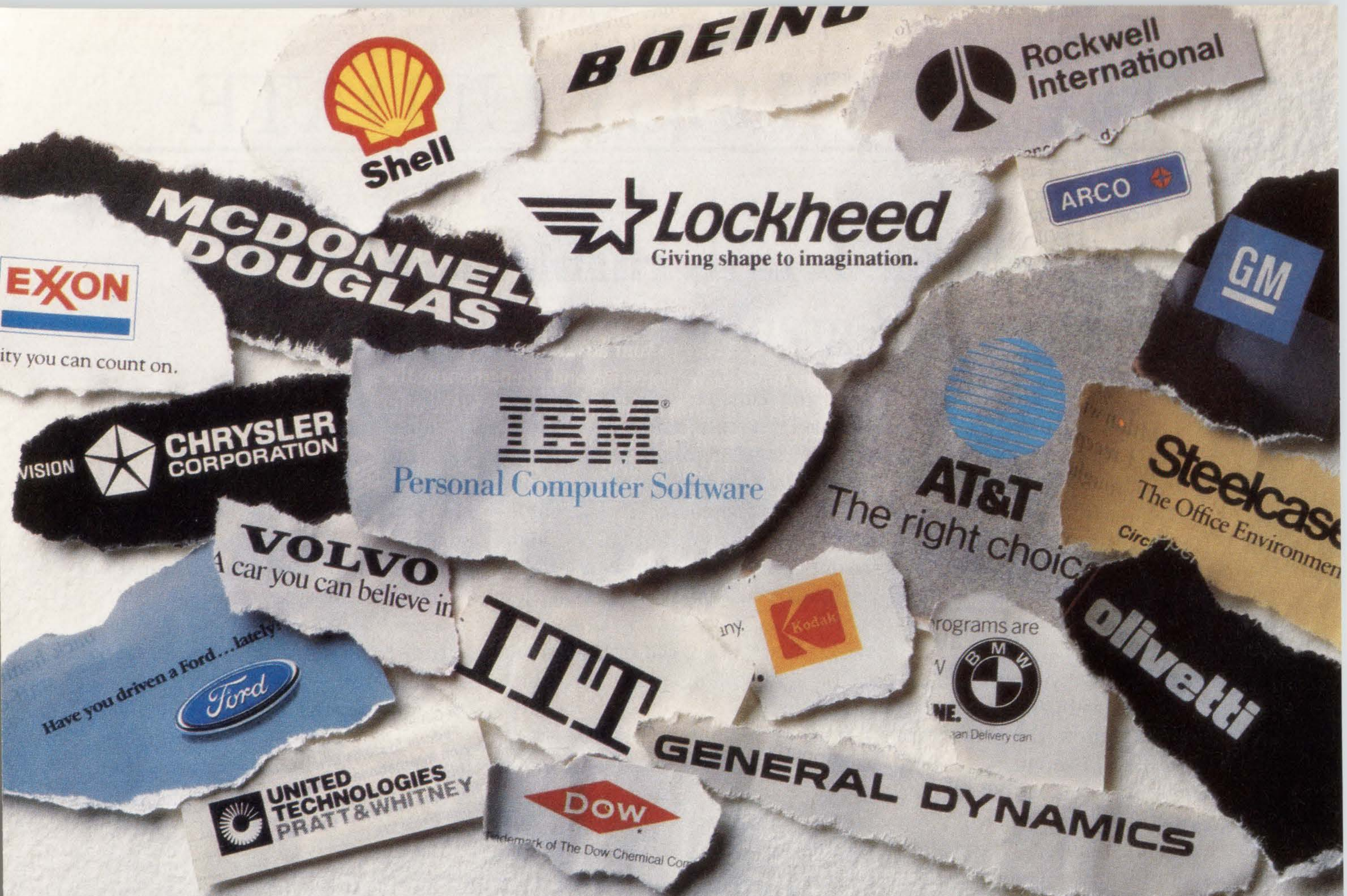
The 2-D algorithm inserts a 1-D Huffman-coded scan line to act as a new reference line at user-specified intervals throughout the document. Thus, if a transmission error occurs in a READ code, its effect is limited to the specified number of scan lines instead of being propagated throughout the document **(Ref 1).**

Several companies are now manufacturing plug-in fax boards based on these CEP ICs for the IBM PC and compatibles. These fax expansion boards allow the PC to emulate a group 3 fax machine. Three such expansion boards are Gammalink's Gammafax, American Data Technology's Smartfax, and Panasonic's FX-BM88.



Model FX-BM88, a plug-in board *from Panasonic Industrial, provides fax hardware and software that lets an IBM PC or compatible emulate a group 3 fax machine and communicate with other fax machines. The communications software lets you establish a directory and send images automatically at times that you specify.*

The $995 Gammafax package comes with software that lets you send and receive images over phone lines at rates as fast as 9600 bps. Actually, effective throughput is somewhat less because the software



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performs extensive error checking, and the hardware continuously adjusts the transmission speed to match the instantaneous capability of the PSTN link. You can expect an average throughput of about 9000 bps between two PC/ATs, or about 4000 bps between two PCs or PC/XTs.

Gammafax's software features allow automatic transmission of documents at a specified time (for example, at night when telephone rates are lower), the inclusion of multiple documents in a single transmission, and the transmission of different combinations of documents to different remote sites.

By the time you read this article, the Smartfax board will be available from American Data Technology at a price between $1000 and $1500. This board operates at 2400, 4800, 7200, or 9600 bps. The software package that comes with it includes a built-in graphics editor that lets you compose new images, enlarge or reduce existing images, rotate all or part of an image, and perform cut-and-paste operations.

The telecommunications routines let you send or receive fax images as a background task while you're running some other application. In addition, they include facilities for automatic dialing, for scheduling drawing-file transfers at specific times, for usage logging, and for looking up the current time associated with area codes throughout the world.

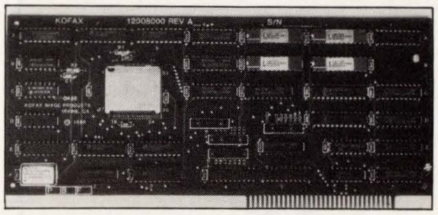
The Panasonic FX-BM88 expansion board ($1000) is intended for use in Panasonic's own IBM-compatible Personal Partner PC, but it also operates in IBM PCs and other compatibles. The board provides group 3 fax transmission of images originating either from an associated flat-bed image scanner or from the PC's disk storage.

Transmission speed may be 9600, 7200, 4800, or 2400 bps, and the hardware provides adaptive equalization, error detection, and automatic retransmission of an erroneous block. The hardware always attempts to operate at 9600 bps, but automatically falls back to the highest speed at which the line (and remote equipment) can maintain error-free communication.

The resident software lets you send or receive fax messages as a background task while you're running another application. You can create, store, and update a fax-machine telephone directory, and the software can use this directory to send one or more fax files to selected destinations at specified times. The software also keeps a history log of all outgoing and incoming fax transmissions, and you can display or print the log at any time.

Board provides disk storage

The Kofax KF-8000 board differs from these other three boards in that it is strictly an image-compression/expansion coprocessor used primarily for efficient storage of images. You can generally store a 1M-byte image in 64k bytes of memory or disk storage. Typical applications include CAE drawing-storage and -retrieval systems, machine-vision systems, and medical imaging systems.



The KF-8000 board *from Kofax compresses and expands bit-mapped images and uses the Am7971 CEP.*

You can create a fax system by using the board's group 3 compression techniques and a separate modem that communicates with any standard fax machine. For maximum resolution, and for PC-to-PC drawing transfers, however, you need to use its more efficient group 4 compression techniques.

The $995 board comes with an easy-to-use MS-DOS device driver. (According to the vendor, it often takes less than one day of programming to interface an application program to the KF-8000.) The board also has a demonstration program that lets you perform disk-file-to-disk-file expansion or compression.

In the very near future, Kofax will be offering its KF-8200 image

Fax boards may raise legal issues

In most states, a document sent by one dedicated fax machine and received by another similar machine is accepted as a legal copy of the original: Dedicated fax machines don't provide any facilities for changing the document. The advent of PC fax expansion boards, however, may cast doubts on the legal acceptability of a faxed document. If you send a document to a PC that emulates a fax machine, the recipient of the document can change its contents by means of the PC's graphics editor.

For this reason, the Portable Office from Medbar Enterprises (Woodside, NY) includes a portable, dedicated facsimile machine. The Portafax weighs only 7½ lbs and attaches to any telephone system by means of an acoustic coupler. The Portafax can communicate with group-2 (analog) or group 3 (digital) facsimile machines.

The other components of the Portable Office are a Data General Model II lap computer with internal or external modem, and an ink-jet printer. The price of the complete system varies from $3939 to $5500, depending on the computer options installed. The facsimile machine is also available separately for $1475.

For more information . . .

For more information on the expansion boards described in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

American Data Technology Inc
Box 3453
Sunnyvale, CA 94088
(408) 732-2400
Circle No 709

Gammalink
2452 Embarcadero Way
Palo Alto, CA 94303
(415) 856-7421
Circle No 710

Kofax Image Products Inc
2691 Richter Ave, #108
Irvine, CA 92714
(714) 474-1933
Circle No 711

Panasonic Industrial Co
1 Panasonic Way
Secaucus, NJ 07094
(201) 348-7000
Circle No 712

compandor (for approximately $2000). This expansion board is similar to the KF-8000 but includes 2M bytes of onboard RAM, a piggyback personality board that matches it to various scanners and laser printers, and a hardware scaling feature that lets you match the drawing size to your video display or printer. As with the KF-8000, the vendor supplies an MS-DOS driver, but you have to write your own interfaces to your application programs.

An on-line alternative exists

One of the principal uses for fax expansion boards is to communicate updated drawings between concerned parties (such as engineers and their customers), but the boards don't permit *interactive* on-line modification of drawings at both ends of a link. To this purpose, American Video Teleconferencing Corp (Farmingdale, NY) offers a RAM-resident software package that permits the operators of two IBM PCs (or compatibles) to call up a drawing or file at both ends and modify it interactively.

Called In-Synch and priced at $149.95, the package's only requirement is that both PCs run the same applications program. Once one party has established a modem link (and preferably a voice link as well), either party can initiate operations that appear simultaneously on both screens. Thus, you can create a new spreadsheet or schematic drawing (or change an existing one), make suggestions about technique or layout, and end up with an identical file at each end—without any difference of opinion between you and your colleague.

You don't incur high connect-time charges for transmitting large files in DIF (data interchange format) or ASCII format because only the concise commands to the application program go over the line; each PC builds or modifies its local file as the result of those commands. Even more important, you can discuss the contents of the file, suggest modifications, and immediately act on them in real time via the modem link. Clearly, this program isn't a complete replacement for all facsimile applications, but just as clearly, it can supplement your PC's fax capability. **EDN**

References

1. Fuchs, Peter M, "Compressing data conserves memory in bit-mapped displays," *EDN*, October 30, 1986, pg 173.

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CY7C149
CY7C130
CY7C170
CY6116
CY7C128
CY7C122
CY7C128
2Kx8 25ns 120/20mA 300 mil
CY6116
2Kx8 35ns 130/20mA
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2Kx8 35ns 120/30mA
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2Kx8 35ns 120/30mA
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16Kx1 25ns 45/60mA
CY7C168
4Kx4 25ns 70/90mA
CY7C169
4Kx4 25ns 70/90mA
CY7C170
4Kx4 25ns 90mA
CY7C171
4Kx4 25ns 70/90mA
CY7C172
4Kx4 25ns 70/90mA
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CY7C149
1Kx4 25ns 90mA
CY7C150
1Kx4 15ns 90mA

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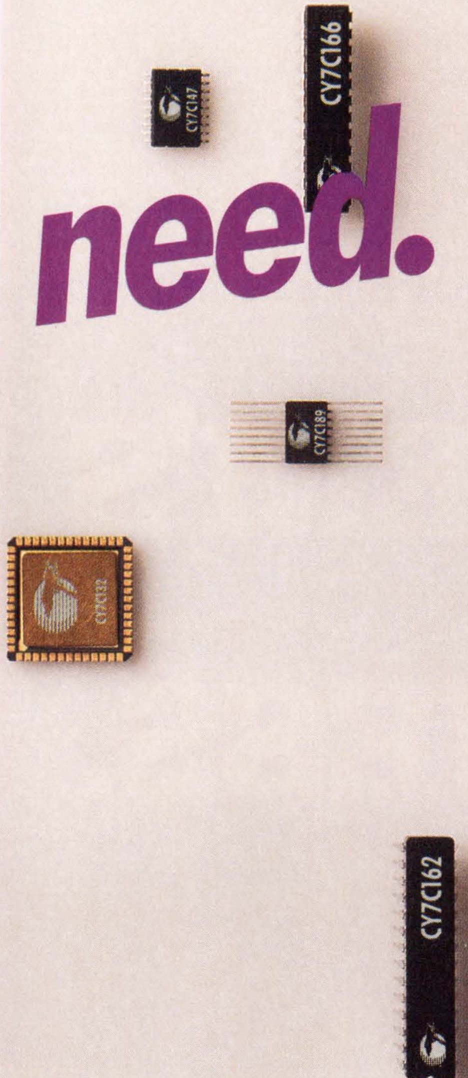

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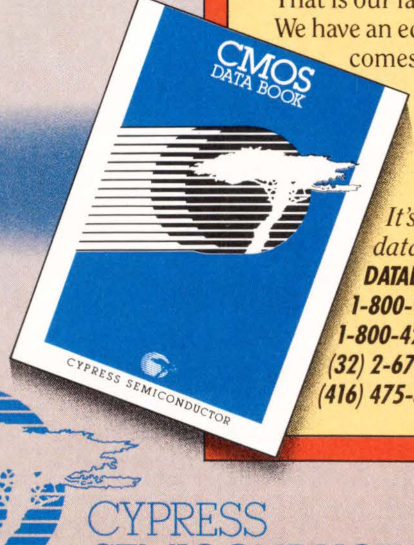

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EF 6803U4	1, 1.25, 1.5	8-Bit ROMless Microcontroller	MC 6803U4 (−1,A)
EF 6809	1, 1.5, 2	High-performance 8-Bit MPU	MC 6809 (A,B)
EF 6809E	1, 1.5, 2	High-performance	MC 6809E (A,B)
16-BIT			
MK 68000	8	16-Bit Microprocessor	MC 68000-8
TS 68000	10, 12.5, 16	16-Bit Microprocessor	MC 68000-10, 12
TS 68008	8, 10, 12.5	16-Bit Microprocessor	MC 68008-8, 10, 12
MK 68200	4, 6	16-Bit ROMless Microcontroller	———

PERIPHERALS

Device	Available Speed (MHz)	Description	Alternate Source
8-BIT			
EF 6821	1, 1.5, 2	Parallel I/O (PIA)	MC 6821 (A,B)
EF 6840	1, 1.5, 2	Programmable Timer (PTM)	MC 6840 (A,B)
EF 6850	1, 1.5, 2	Serial I/O (ACIA)	MC 6850 (A,B)
EF 6854	1, 1.5, 2	ADLC Controller	MC 6854 (A,B)
16-BIT			
MK 68230	8, 10	Parallel I/O and Timer	MC 68230-8, 10
MK 68564	4, 5	Serial I/O	———
MK 68901	4, 5	Multi-Function Peripheral	MC 68901-4
MK 68451	8, 10	MMU	MC 68451-8, 10
TS 68HC901	4, 5, 8	HCMOS Version of 68901	———

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Device	Description
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EF 9367	Graphic 512 x 1024 Pixels
EF 9369	Palette Circuit 16 x 4096
EF 9370	Palette Circuit 16 x 4096
TS 68483	Graphic — Drawing Processor
TS 68493	Enhanced 68483
TS 68494	Palette 256 x 4096

DSP/DATA COMMUNICATION

Device	Description
TS 68930	High-performance Digital Signal Processor
TS 68931	ROMless version of 68930
TS 68950/1/2	Modem Analog Front End Chip Set
MK 68590	Ethernet Controller (LANCE™)
MK 68591/92	Serial Interface for Ethernet

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PRODUCTS

DSP Board Fits IBM PC

GE/Intersil's EVK-128 combines A/D conversion and FIR filtering

JEFF HAIGHT
GE/Intersil Inc.

As digital signal processing becomes simpler, cheaper, and more pervasive, the boundaries between design ideas and design techniques must give way for a more integrated approach to system development. Intersil's EVK-128 board, which occupies one slot in an IBM PC, incorporates analog design and digital signal-processing techniques.

The board works in such applications as PC-based analog or digital data-acquisition and digital filtering systems, finite-impulse-response (FIR) filter design and development systems, or as part of an FIR filter processor for off-line or non-real-time data.

The system (Fig. 1, below) offers an active antialiasing filter, power-supply circuitry, A/D and D/A converters, and digital interfacing and control circuitry. The board also has FIR filtering circuitry and software for FIR design, modification, plotting, and control. Documentation includes itemized parts lists, schematics, timing

continued on page 19

The EVK-128 provides signal-processing hardware and FIR-filter design and modification software. You can copy all or part of the system for use in your own signal processor.

TECHNOLOGY

Power MOSFET Makers Boost Electrical Specs

Manufacturers improve electrical characteristics and offer a host of package types

TAMMI HARBERT
Staff Editor

Recent power-MOSFET introductions offer lower on-resistance, higher voltage, faster switching, and innovations in onboard intelligence. Packaging improvements include greater electrical isolation and an increased availability of plastic and surface-mount parts.

Among the manufacturers of low-on-resistance devices are some companies well known in the power-MOSFET industry: Siliconix, Fairchild, International Rectifier, and General Instrument. Newer manufacturers—IXYS, for example, have also entered the arena.

Low-on-resistance parts
Made for applications requiring low on-resistance, Siliconix's SMM70N05 is built using the company's MOSPower-6 technology, which produces a chip density of 1.6M transistors/in². The device has an 18-mΩ on-resistance with a continuous current rating of 70A. The 50V SMM70N05, a follow on to the company's SMP60N05 and SMM60N05, is available in TO-3 packaging for $10.11 (1000).

Like the SMM70N05, the SMP- and SMM60N05 are 50V MOSPower-6 devices. Unlike the newer device, however,

these parts offer current and on-resistance of 60A and 23 mΩ respectively. Another de-

continued on page 21

CAREERS

The Temptations of Temping

Once confined to the clerical realm, temping grows in popularity among EEs.

RUTH CLOGSTON

Chris Clark, a 30-year-old programming consultant from Hopkinton, MA, has worked as a contractor for six months. He started temping because he wanted freedom and independence—he is developing his own software and needs to avoid the conflicts of interest

continued on page 58

COMPANIES WITH EXPANDED OPTIONS

EEs are increasingly being drawn toward temping.

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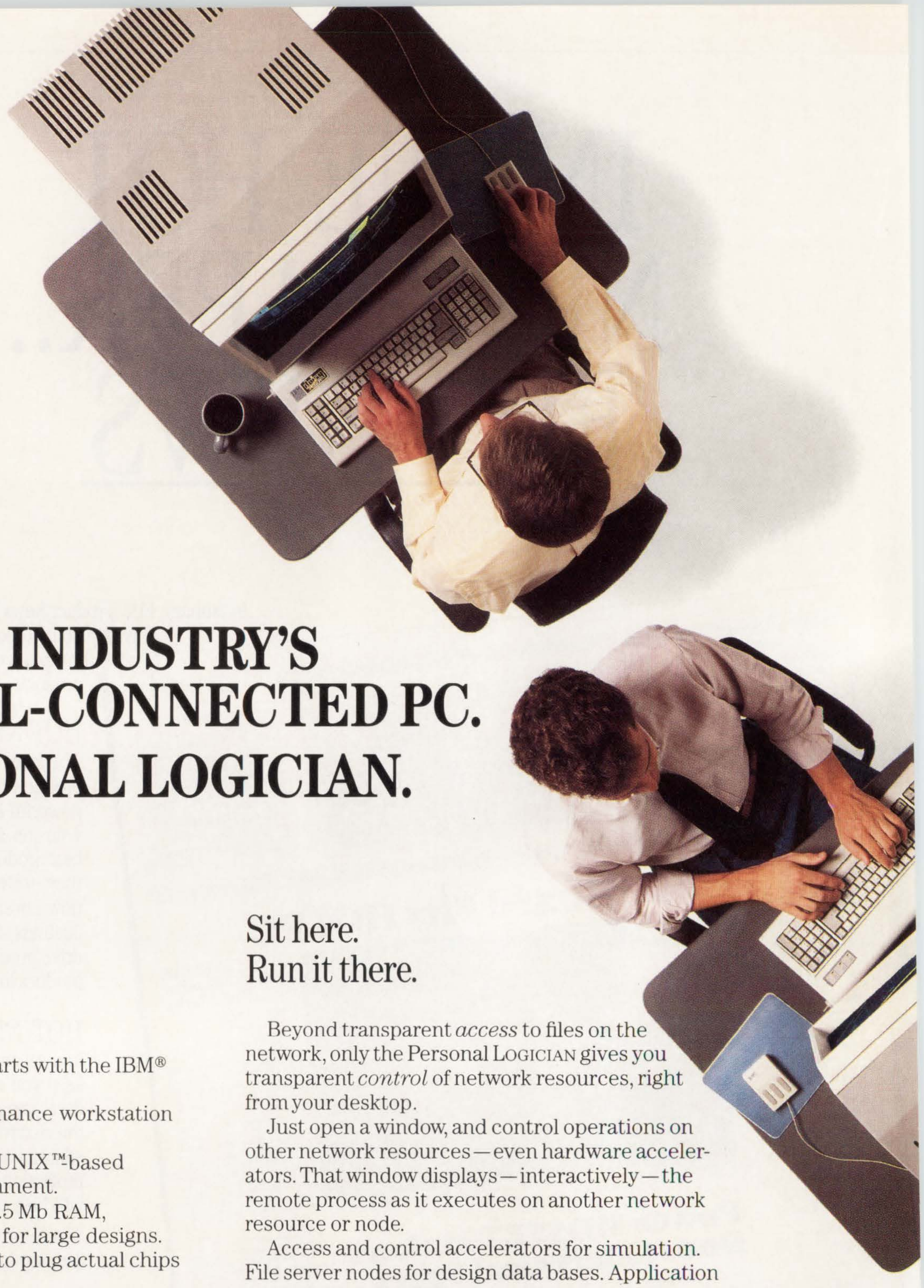

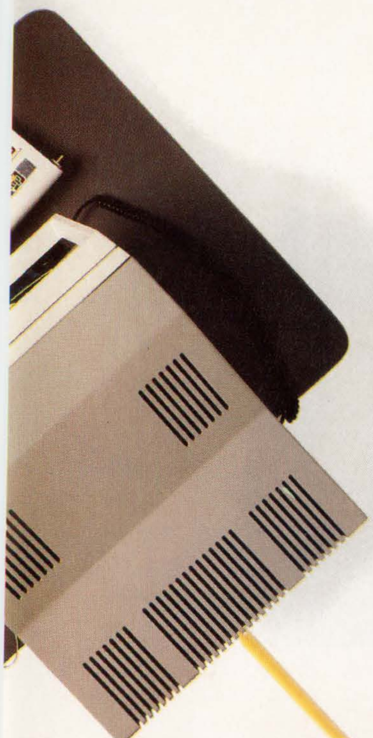


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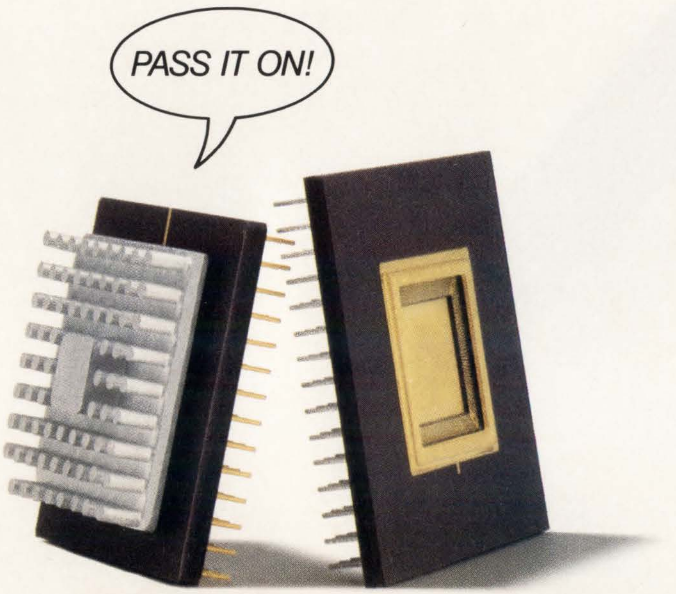

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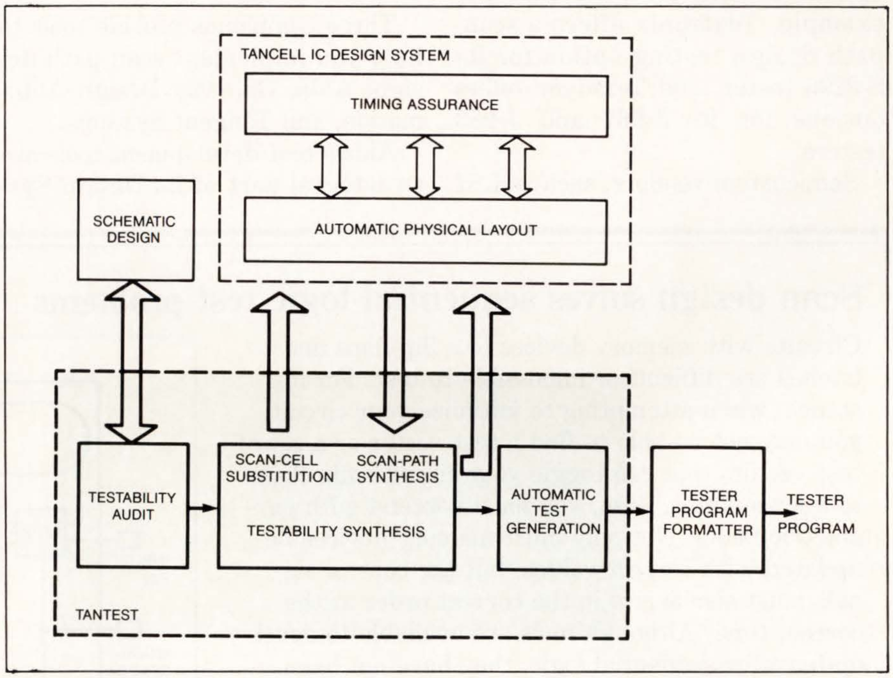
Scan-path tools speed the conversion of your design into a testable chip

Chris Everett, *Regional Editor*

Large chips—those with more than 10,000 to 20,000 gates—are difficult if not impossible to test. It's just not the sheer number of gates that is complicating the testing problem, but also the inclusion of memory devices such as flip-flops and latches.

You could employ a scan-path design methodology to make your chip more testable. But manually designing the additional test logic takes time. Moreover, the additional test logic increases die size and introduces timing delays, which hamper system performance. Automated scan-path design tools, however, can speed the design process while minimizing die size increases and system performance losses.



***Large semicustom ICs** are proving to be difficult if not impossible to test unless you design-in testability. Test-design tools such as Tangent Systems' Tantest suite of tools are integrated with other design-verification tools in a CAE workstation. After design entry, you can check your design for its testability, add needed test logic, verify the design's operation, and automatically generate test vectors.*

The idea of using a scan-path design methodology to make designs testable isn't new. The first published description appeared in 1973. Designers at some companies, including AT&T and NCR, have embraced the concept, expanded it, and incorporated it into their chip-design processes.

Many other designers also tried to use scan-path design technology as well—but they gave up. They found that there were no commercially available tools to help implement scan-path testing. Similarly, the multiplexed flip-flops that the scan-path technique requires were not available as standard parts.

In addition, the available ATE systems did not support scan-path testing. Scan-path testing requires that flip-flops be chained together into a shift register so that test data can be serially shifted into and out of the circuit under test. Hence, each test cycle required application of a test vector one bit wide but tens of bits deep. Testers provided neither the memory depth nor the control needed to shift long strings of test data into the device.

But even had designers gotten over these hurdles, they would have been faced with the penalties of using scan-path design. First, adding multiplexers, mode-select lines, clocking logic, and other test-logic overhead would have made designs larger, which meant larger die sizes and lower manufacturing yields. On scan-path designs that were implemented, die size increases of 10 to 30% were common, with some designs incurring a 50% penalty. Moreover, adding multiplexers also adds time delays, thereby slowing down system speeds.

Thus, many engineers gave up on scan-path techniques and hoped that the test engineering department would find a way to test their designs. But now, you'll find that with chips containing 20,000 or more gates, the test engineering department won't necessarily be able to bail you out. Given enough computer size and time, automatic test-pattern generators and their associated fault simulators can generate tests for combinational logic designs, but there is a theoretical limit on the size of testable sequential-logic designs.

Therefore, to keep test development costs down or even to make testing of your sequential device possible, you must turn to some alternative like scan-path design techniques for test development and accept the penalties.

The hurdles that designers have encountered when they tried to use scan-path design techniques are now disappearing. ATE vendors are supporting scan-path designs with deep memories and scan-path test options on their ATE systems. For example, Tektronix offers a scan-path design testing option for its S-3295 tester, and Teradyne offers options for its J-967 and J-983 testers.

Semicustom vendors, such as LSI Logic, are now offering scannable flip-flops and latches in their device libraries. Hitachi, for example, includes scan-path design testing logic in several of its CMOS and bi-CMOS gate arrays.

Automated tools available

Three companies provide tools to help you implement scan-path design: Aida, Gateway Design Automation, and Tangent Systems.

Aida's test development tools are an integral part of its Design System, which resides on the 32-bit Apollo workstation. To help you design a testable chip, Aida includes a monitor to check that you are adhering to logic-design rules so that the scan-path design circuitry can be easily added to your circuit.

The monitor is called the Logic Design Rules Checker (LDRC), an AI-based system. You can add to it your own design methodology conventions, electrical rules, technology constraints, and parts preferences.

Scan design solves sequential-logic test problems

Circuits with memory devices like flip-flops and latches are difficult or impossible to test. For instance, when attempting to initialize your circuit, you may not be able to find a test vector or a set of test vectors that can toggle your circuit's flip-flops to known states. Also, you must contend with parametric faults. Not only must memory devices be updated with correct values, but the control signals must also arrive in the correct order at the correct time. Although tools are available to develop tests for sequential logic, they have not been totally satisfactory.

Obviously, you can't be asked not to use memory elements in your design. But if the memory elements could be eliminated or masked during test, the test would be reduced to a straightforward one of testing combinational logic. Scan-path testing techniques provide just that capability.

By adding a 2-to-1 multiplexer in front of each flip-flop in your design, you set the stage for scan-path testing **(Fig A)**. One input of each multiplexer connects to your circuit where each flip-flop's input would have been connected, and each flip-flop's input connects to its multiplexer's output. The multiplexers' second inputs are used to serially chain all the flip-flops together. That is, the output of the first flip-flop connects to the second input of the second flip-flop's multiplexer, the second flip-flop's output connects to the second input of the third flip-flop's multiplexer, and so on. The output of the last flip-flop connects to an output pin on your device. The second input of the first flip-flop's multiplexer connects to an input pin, and another input pin serves as the mode-select line, which controls whether the flip-flops operate in the normal mode or in the serial-shift mode.

In the normal operating mode, the flip-flops function as usual (except for some time delay inserted by the inclusion of the multiplexer). In the serial-shift mode, the flip-flops function as a shift register. You can serially shift data into the flip-flops and set them to known states. In effect, you

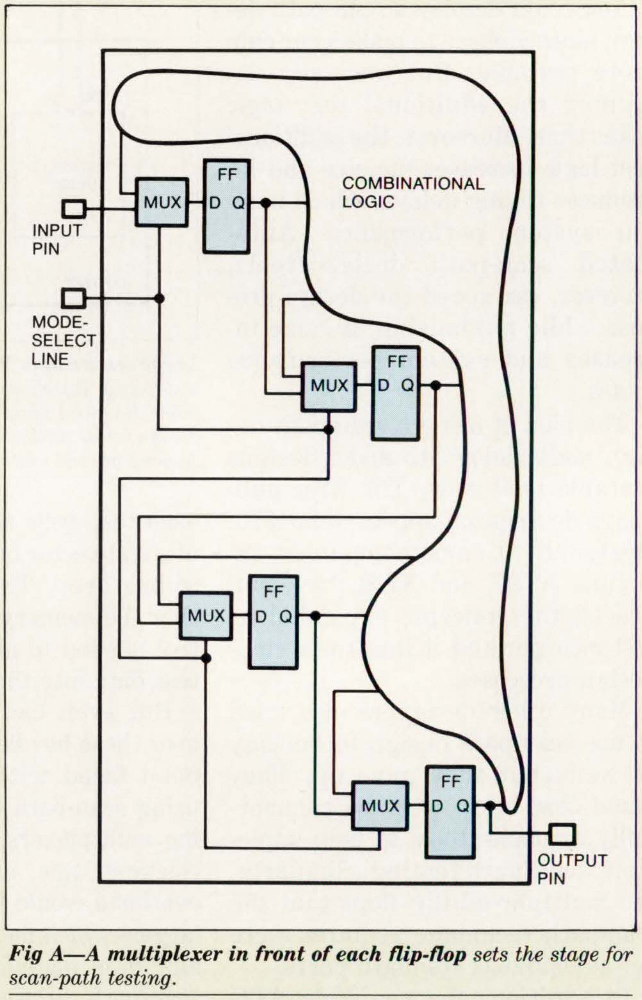


Fig A—A multiplexer in front of each flip-flop *sets the stage for scan-path testing.*

Initially, you load your design onto the Apollo workstation using either Aida's design-entry tools or translators, which can load net lists from Mentor Graphics workstations or workstations that can provide a Tegas-like net list. You then run the LDRC to spot any design considerations, such as feedback loops, that would prohibit you from implementing the scan-path design.

Before using the Scan-ring Generator, you select the number of scan-path chains to be added to your design and determine the order in which the flip-flops are to be connected in each chain.

You can specify the connection of the scan-path logic chains before or after physical layout. Aida suggests that you do so before, because semicustom houses don't usually want to get involved with specifying the scan-path logic after the design has been laid out and simulated. Also if the scan-path logic chains are defined before physical layout, there tends to be less work involved if a layout change is needed. But there is a tradeoff. You may find your design requires a larger die size if the test logic is specified before instead of after the physical layout.

The Scan-ring Generator automatically converts the flip-flops to scannable flip-flops, routes and connects the scan chains, and adds the needed scan-control logic. The Automatic Test-Pattern Generator ($45,000) then develops the patterns for both the normal I/O pins and the scan-path pins. The Fault Simulator

convert the memory elements in your design to pseudo-inputs and pseudo-outputs that can supply vectors to the combinational logic surrounding them. In essence, you increase the visibility into your design by the number of pseudo-inputs and -outputs the scan-path adds to your design. The tester doesn't care whether test vectors are applied at the device's input pins or through the pseudo-inputs created by the scan path, nor does it care where the results are gathered. The only difference between the device's I/O pins and the pseudo-I/O pins is how the tester applies and recovers the test data.

To test a device, the tester first switches the mode-select line to the serial-shift mode. The tester then clocks test data onto the flip-flops via the scan path. After the mode-select line is switched back to the normal operating mode, the tester applies test vectors to the device's input pins. The test clock is exercised, and the tester then collects and evaluates the data at the device's output pins. The tester then again switches the mode-select line to the serial-shift mode and serially shifts out the updated contents of the flip-flops and evaluates the data. While the updated contents of the flip-flops are being shifted out, new test data can be shifted in for the next test cycle.

The use of a multiplexer in front of flip-flops is the first published description of a scan-path test technology, but it has been followed by several other approaches. Currently, four other techniques are receiving attention.

NEC uses a 2-port flip-flop in its designs to implement its scan-path technique. The 2-port flip-flop uses two clock inputs instead of the single clock input and mode-select line used in the traditional multiplexer/flip-flop combination.

Instead of flip-flops, IBM uses latches in its level-sensitive scan-design technique. With this approach, you would design your chip with single-port latches instead of flip-flops and then replace each latch with a 2-port latch. However, the latches cannot be directly chained together to construct the shift register. You would have to add a second single-port latch to each 2-port latch to build the shift register.

The advantage of latches over flip-flops is that latches are hazard free; that is, they are not dependent on the clock's rise and fall times for correct operation. As long as the clock is active, the output of a latch will follow level changes on the input—hence the name "level-sensitive scan design."

To avoid the problem of having to add latches when chaining the system latches, Unisys uses a separate test-data shift register to clock data into and out of the system latches. Although you need more hardware to implement Unisys's scan-set technique, you gain two advantages over the IBM technique. You can clock the contents of the system latches into the test-data shift register during normal system operation, allowing you to take a status check any time you want. Also, data from nodes other than the latch nodes can be clocked into the test-data shift register, thereby increasing the visibility into the design.

Instead of a shift register, Fujitsu/Amdahl uses a multiplexer and a demultiplexer to implement its random-access scan-design technique. You use the multiplexer to clock data out of the system latches and other circuit nodes you want to observe. You use the demultiplexer to set the latches to known states prior to test. Like Unisys's scan-set technique, you can scan the latches during normal operation of your system.

($15,000) grades the resulting patterns using both the Logic Simulator ($50,000) and the Cosimulator Processor ($40,000). The coprocessor is a special-purpose RISC machine that plugs directly into the Apollo workstation. Aida claims a 2.5 to 6.8 times improvement in time to prepare and run a simulation on a 102k-gate design using its coprocessor and simulator versus competitive systems.

The compiled fault simulator uses a variation of the D-algorithm. After propagating and justifying the fault path, the simulator runs the resulting test vector against all the faults remaining in the undetected fault list. Any additional faults detected are then removed from the list.

How much fault coverage is enough?

The ultimate goal of testing is to limit the number of defective parts shipped to customers to an acceptable level. However, the defect level after testing is dependent on not only the number of faults your test vectors will uncover during test (its fault coverage), but also on the yield of your manufacturing process. The equation

$$\text{Defect Level} = 1 - \text{Manufacturing Yield}^{(1-\text{Fault Coverage})}$$

has proven to be an adequate model for many different manufacturing processes. You can use the graph in **Fig A** to visualize the effect that both fault coverage and manufacturing yield have on the percentage of parts shipped that have defects.

If you are manufacturing pc boards with a manufacturing yield of about 95% and have generated a set of test vectors that will uncover 70% of all the potential faults in your boards, then you can expect that about 1% of all the tested boards shipped will have defects. On the other hand, if you use a set of test vectors with 70% fault coverage to test your IC design, then you can expect about 90% of your tested parts to be shipped with defects. Even if your test vector set is expanded or improved to provide 97% fault coverage, you can still expect to ship 10% of your parts with defects.

The higher defect level in ICs shipped results because of the much lower manufacturing yields found in IC manufacturing processes than found in pc-board manufacturing. IC yields of 1 to 10% will force you to use vector sets with greater than 99.90% fault coverage to ensure that you will have less than 0.1% of your tested parts with defects.

How much fault coverage is enough? It depends on your manufacturing yields and what percent of parts shipped that you can afford to be defective. If, however, you find that you do need better than 70% fault coverage, you will probably have to turn to automatic test-pattern generators and their associated fault simulators to generate the required test vectors.

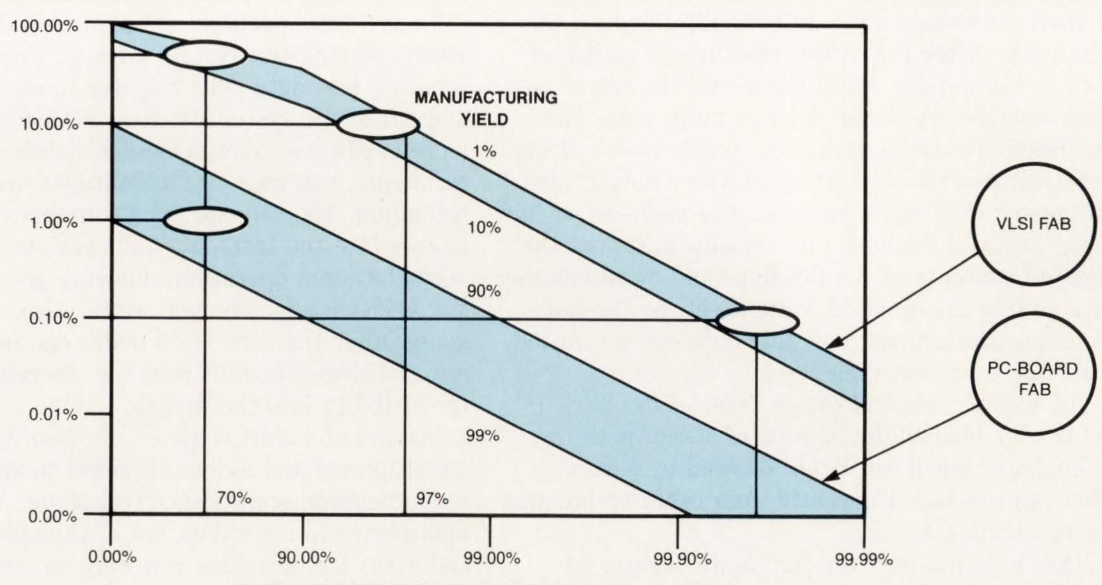
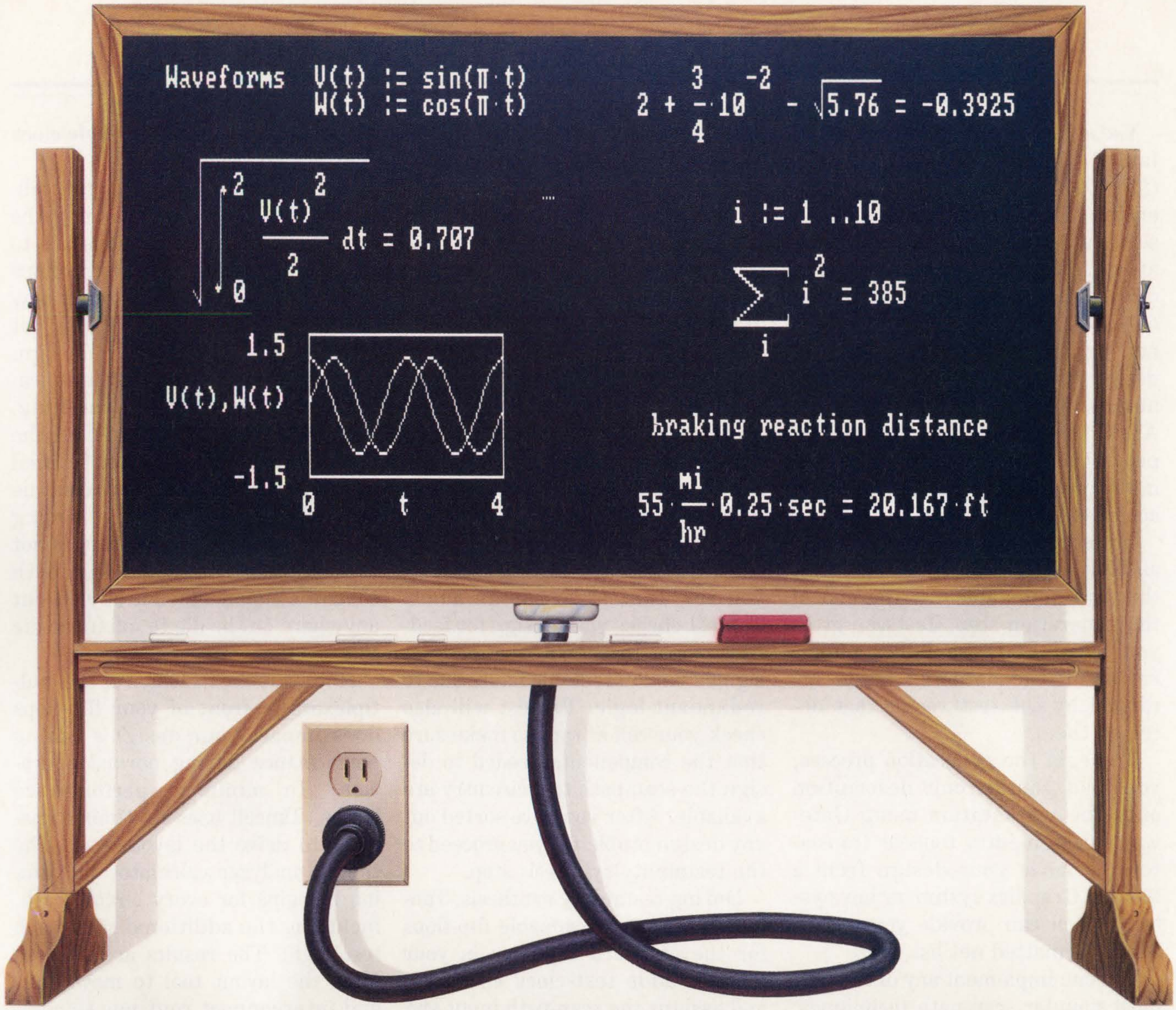


***Fig A—Defect level is dependent** on both the manufacturing yield of its fabrication process and the percentage of potential faults in the products that are tested. Low manufacturing yields, such as found in IC manufacturing, force you to increase test fault coverages to better than 99% in order to keep the percentage of defective devices below 1%.*



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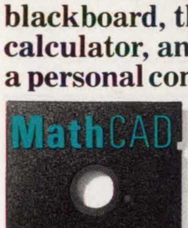

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Gateway Design Automation's fault simulator in its Testscan ($75,000) test-development tool operates in a different manner. Testscan's automatic test-pattern generator (ATPG) first examines your circuit, then generates an initial set of test vectors. The vectors are then run against all the faults in your design and graded according to the number of faults found. Then the ATPG generates a new set and repeats the process until the maximum possible fault coverage is achieved.

Testscan also detects and reports all fault locations in redundant logic that are untestable. At the end of the generation step, Testscan gives you a list of those faults plus a listing of the detected faults arranged by the test vector that detected them.

To begin the generation process, you load your circuit description onto the workstation using Gateway's design-entry tools or translators to move your design from a Mentor Graphics system or any system which can provide you with a Tegas-formatted net list.

You can implement any of the four most popular scan-path techniques: IBM's LSSD, NEC's Scan Path, Fujitsu/Amdahl's Random Access Scan, or the Scan Set design technique developed by Unisys (see **box**, "Scan design solves sequential-logic test problems"). Also, if portions of your design are not to be tested using the scan-path techniques (such as embedded memories), you can have Testscan ignore those portions of your design.

After your design is loaded, Testscan audits the design to check that it conforms to the scan-path design rules. Any errors are listed along with diagnostic messages that tell you where they occur. Then the ATPG automatically completes the process. Typically, Testscan can audit, generate, and grade test vectors for a 2000-gate circuit in less than two minutes.

Testscan operates on a Sun or Apollo workstation, a DEC VAX system, or an IBM mainframe. You can use Testscan to add scan-path design logic and generate test patterns for either chip designs or digital-circuit designs.

Tool waits to minimize silicon

Tangent Systems' Tantest ($55,000) is optimized for standard-cell designs. It's an option on Tangent's Tancell system—a fully automated layout system for cell-based semicustom integrated circuits.

After you enter your net list and cell library onto the workstation, you ask Tantest to run an audit. Tantest checks your design for feedback loops, inaccessible set or reset signals, and untestable faults due to redundant logic. Tantest will also check your cell library to make sure that the components needed to design the scan-path test circuitry are available. After you have sorted out any design problems, you proceed to the testability-synthesis step.

During testability synthesis, Tantest substitutes scannable flip-flops for the standard flip-flops in your design, adds test-clock circuitry, and assigns the scan-path input and output pads. It substitutes edge-triggered flip-flops in your design to support the standard scan-path design technique.

Tantest also locates each clocking network in your design and adds multiplexers so that the networks can all be connected to a single clock source for testing.

Tantest waits until after the cell-layout step before determining the order in which the flip-flops are to be chained together. The flip-flops can later be chained together in any seemingly illogical order and not affect the testability of the design. The ATPG keeps track of their location within your design. By waiting, Tantest therefore does not limit the layout tool's options. Constrained layout options lead to increased die sizes. Also, because the timing within the scan-path circuitry is not critical during test, the scan-path control components can be laid out anywhere on the die to minimize die size.

However, the inclusion of the multiplexers in front of your flip-flops does impact your design's timing performance during normal operation. To minimize performance losses, Tancell uses its timing analyzer to drive the layout tool. The timing analyzer calculates the timing margins for every circuit path, including the additional scan-path test logic. The results are used to force the layout tool to move cells and interconnect routings to compensate for the additional circuit delays caused by the scan-path test logic.

After the cells are laid out, Tantest determines the order in which the flip-flops are connected based on ease of routing and reduced die size

For more information . . .

For more information on the design-for-testability tools described in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

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Circle No 706

Gateway Design Automation Corp
Box 1545
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(617) 486-9701
Circle No 707

Tangent Systems Corp
2840 San Tomas Expressway
Santa Clara, CA 95051
(408) 980-0600
Circle No 708

considerations.

At the completion of the testability synthesis step, the test generation process begins. Tantest uses a deductive fault-simulation process. The ATPG generates an initial test vector sequence to sensitize the signal paths in your design. The simulator then starts at the inputs and deduces what faults were detected and lists them. More vectors are generated and the process is repeated until the fault coverage goal is reached. Tangent Systems' tools are used on DEC Vax systems as well as on Intergraph's Interpro 32 workstation.

It has been said that the primary barrier to the use of scan-path design has been the lack of tools. Robert Blauth, vice president of marketing at Gateway, doesn't agree. "I'm not really sure that it's a lack of tools that is slowing [the use of scan-path testing techniques] down. I really think that the designer is not yet convinced [that he needs a scan-path design]. He feels he has got to design the highest performance or the smallest system, and he's heard horror stories as to overhead taking 20 to 50% of silicon and slowing his machine down 50%. And he's very concerned about those issues." But Blauth adds, "The world is starting to become aware of testability issues and sees the real testability problem facing—especially—ASIC design." **EDN**

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3. Williams, T W, and N C Brown, "Defect Level as a Function of Fault Coverage," *IEEE Transactions on Computing*, Vol C-30, No 12, December 1981.

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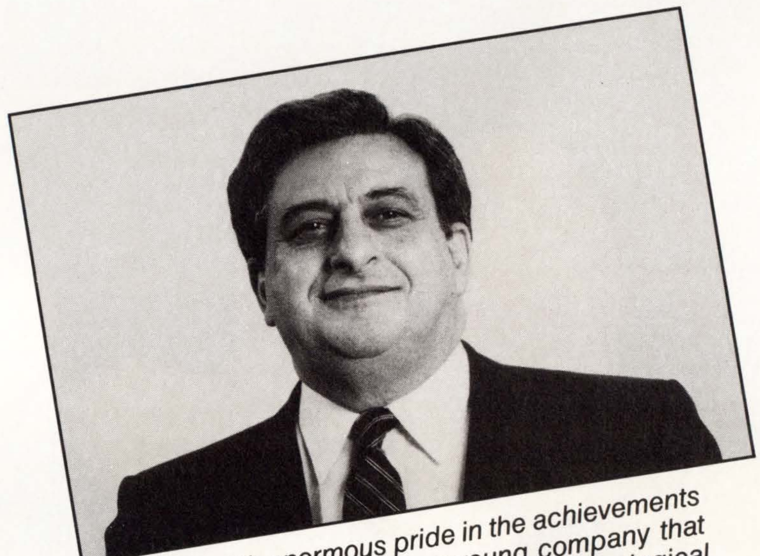

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MC68020 vs. 80386.

How to run apples-to-apples vs. apples-to-oranges benchmarks on these archrival 32-bit MPUs.

Choosing the world's highest-performance 32-bit microprocessor should be as easy as making an apples-to-apples comparison with such industry-standard benchmarks as Whetstone and Dhrystone performance.

How to tell apples from oranges.

When pulling an apples-to-apples comparison, anyone, anywhere, should be able to easily duplicate the comparison factors and results. Repeatably.

Attempt no. 1.

So, when comparing the MC68020 and 80386, the first task is to find one of each.

Motorola shipped over a quarter of a million MC68020s last year, so finding one is easy. Get the fastest available—a 25 MHz—and a 20 MHz Motorola floating-point coprocessor, the MC68881.

Next (things get harder), try to get your hands on a fully functional, bug free 80386 MPU and 80387 floating point.

And now you know why it's so hard to make an apples-to-apples comparison: you can get the Motorola devices, but "comparable" '386 and '387s? No way. You have to settle for the slower '386 and the promise of silicon yet to come on the '387.

Attempt no. 2.

All right, if you can't find the chips, go for readily-available 32-bit systems and compare real, live, '020- and '386-based systems from the commercial market.

Exasperating, isn't it? There are hundreds of choices of commercially-available, '020-based systems. But, finding comparable '386-based systems...?

Attempt no. 3.

Running real benchmarks on real products is the best comparison. We've looked at two questionable comparison attempts. Now it's time to try some industry-standard approaches, such as Whetstone and Dhrystone benchmarking. That should allow an apples-to-apples comparison, shouldn't it? If not, at least it should be apples-to-apples on paper.

Here are currently-available Whetstone and Dhrystone procedures for the MC68020 and the 80386 32-bit processors. To use industry-standard methods of comparison, you'll have to—must—rerun the Whetstones and Dhrystones for the '386 along the same universally-accepted lines as for the '020.

And discover which has the greater potential for being a keystone and which for being a millstone in your new design. The MC68020 is *still* the highest-performance microprocessor no matter how you slice it!

WHETSTONE PERFORMANCE

The Whetstone is a standard double-precision, floating-point benchmark written in FORTRAN.

MC68020/68881

- Execution of standard Whetstone benchmark written in FORTRAN: recognized and run by all leading systems manufacturers (Cray, DEC, IBM, etc.).
- Double-precision floating point: specified by standard Whetstone for high accuracy.
- Complete, 10-loop-count execution: 1 million Whetstone instructions.
- Unary instructions executed: specified by standard Whetstone; single-operand operations.
- Entire Whetstone benchmark procedure was not modified from the original standard: no tricks or tweaks to hype performance.

Result: 1.24 million Whetstones/second with commercially-available silicon (68020, 68881).

80386/80387

- Execution of vendor-modified Whetstone benchmark written in C: nobody else in the industry uses this particular procedure.
- Single-precision floating point: non-standard Whetstone sacrifices accuracy for "performance."
- Incomplete, 2-loop-count execution: only 200,000 Whetstone instructions.
- No unary instructions executed: intentional '386-vendor modifications to Whetstone spec avoids single-operand operations.
- Altered Whetstone benchmark procedure allowed '386 vendor more favorable results: avoided branch control overhead.

Result: Claims that provide no ability for apples-to-apples comparison.

DHRYSTONE PERFORMANCE

The Dhrystone Benchmark measures CPU performance on a typical mix of high-level language statements.

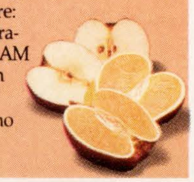
MC68020

- Dhrystone results measured on commercially-available system: Sun Microsystems 3/200 workstation.
- Commercially-available operating system (UNIX®).
- Commercially-available UNIX® C compiler (cc).
- Real-world memory architecture: Dhrystone WRITE operations must pass through to main-memory DRAM.

Result: 6362 Dhrystones with commercially-available, real-world systems.

80386

- Dhrystone results measured on specially-modified "hot box" built by '386 vendor: '386 "starter kit" version not commercially available.
- No operating system used: '386 vendor used own modified debug monitor.
- '386 Vendor used own internal "beta" version of C compiler: not commercially available.
- Utopian memory architecture: zero-wait-state WRITE operations to unlimited cache SRAM —no write through to main memory.



Result: Claims that provide no ability for apples-to-apples comparison.

UNIX is a registered trademark of AT&T.

For an engineer-to-engineer or senior-manager-to-senior-manager update on the real 32-bit system products, call toll-

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free any weekday. If the call can't cover your needs, we'll have the appropriate person get in touch.

For more information on the MC68020, and an apples-to-apples comparison, send the coupon to Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036.

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Magnetic materials provide the final piece to the high-frequency switching-supply puzzle

Charles H Small,
Associate Editor

Driven by the need for physically smaller supplies, power-supply designers are beginning to push beyond the 100-kHz switching speeds of today's switch-mode supplies to frequencies of 1 MHz and higher. The magnetic materials—principally ferrites—used to construct a supply's transformer core are the limiting factor of high-frequency designs, because all the other required components—high-speed power transistors, control chips, and nonmagnetic passive components—can easily handle high frequencies.

Some engineers might wonder why magnetic materials for high-frequency switch-mode power supplies pose problems. After all, the magnetic-materials industry has been supplying ferrite-core transformers of much higher frequencies for applications like local-area networks (LANs). The high-frequency signal-transformer materials have not proved suitable for power applications, however. The problem is simply that these high-frequency ferrites exhibit negative temperature coefficients. Therefore, the signal-transformer materials' inductance values decrease to unusable levels in the 100°C-plus environment of power supplies.

Only the most recent introductions from magnetic-materials makers provide acceptably low losses at moderately high frequencies. Right now, most high-frequency switch-mode power-supply projects are military designs. The smaller size and potentially lower cost of these high-frequency supplies will inevitably—and soon—force commercial engineers to adopt such designs.

For example, AIE Magnetics has introduced a complete transformer assembly for 50W, high-frequency switch-mode power supplies that operate at frequencies to 1.5 MHz. The company designed the transformer to operate with the Unitrode PWM UC 3825 current-mode IC. The company claims that the transformer is 98% efficient at full load. The unit measures 1.25×1.06×0.70 in.

The transformer requires only a 700-nH, air-core output-filter inductor whose coil measures 0.5×0.5 in. The inductor is both cheaper and lighter than ferrite- or iron-core chokes. The transformer costs $13.50, and the choke costs $2.25 (1000).

For engineers who must design their own transformers, selecting a transformer core material for high-

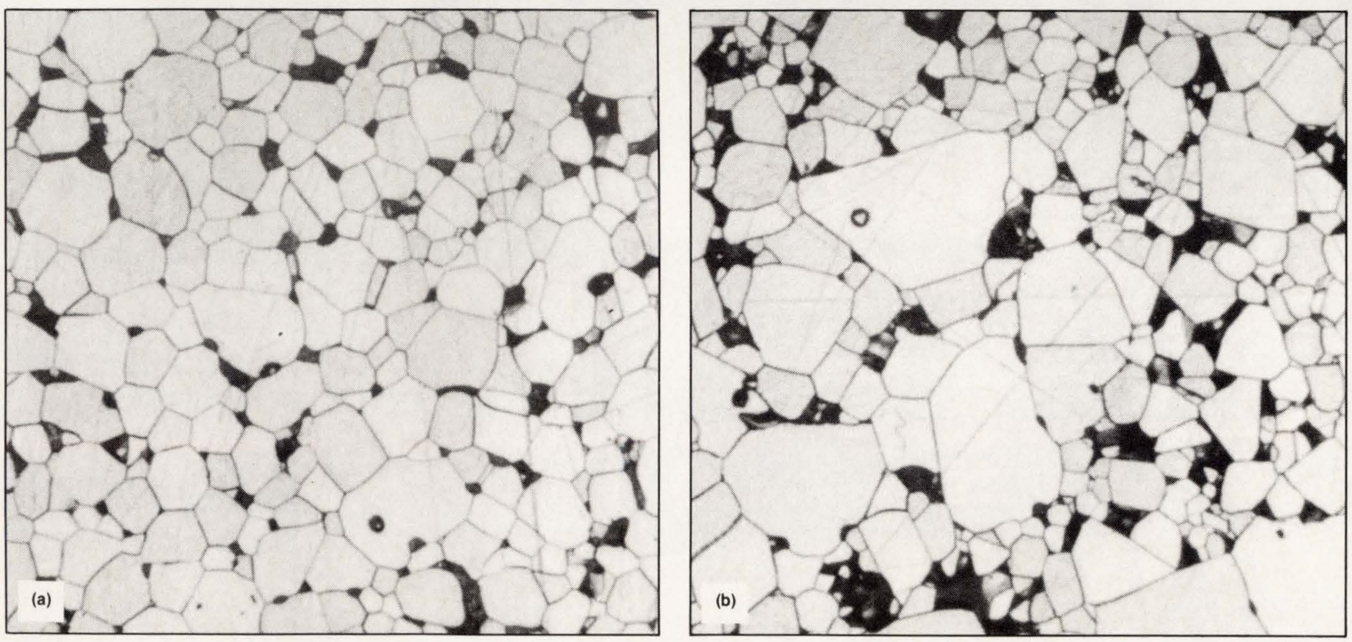

Fig 1—Small differences in ferrite processing *can have a major effect on the material's losses at high frequencies. These microscope photographs (magnified 400×) show two ferrites with exactly the same mix of raw materials. The material with the more uniform grain size **(a)** exhibits one-half the losses at high frequencies that the nonuniform material **(b)** exhibits.*

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frequency switch-mode power supplies is not easy. Manganese zinc (MnZn) and nickel zinc (NiZn) are the two leading candidates for high-frequency switch-mode power supplies, but your choice of either involves your accepting some tradeoffs.

NiZn offers much higher bulk—or volume—resistivity than MnZn. Higher bulk resistivity results in lower eddy-current losses, and eddy-current losses are proportional to the square of the supply's operating frequency. If high-frequency switch-mode power supplies eventually go higher than the 1-MHz operating-frequency region—to speeds of 20 MHz or greater—then NiZn materials will clearly be the best choice.

But MnZn ferrites offer higher initial permeability and will support higher flux densities without saturating than will NiZn. Also, MnZn materials will work over the entire military temperature range, while NiZn materials will not.

The process is the key

Making cores for high-frequency switch-mode power-supply transformers calls for new formulations and exacting process controls on the part of the ferrite manufacturer. Very subtle differences in manufacturing processes can make large differences in core performance at high frequencies, according to Ceramic Magnetics, a manufacturer of custom cores.

Fig 1 shows microscope photographs taken at 400× magnification of the company's standard MN80 ferrite after different processing runs. **Fig 1a** shows small, uniform grains in the material; **Fig 1b**'s ferrite has exactly the same mix of raw materials as that shown in **1a,** but it exhibits twice the loss at high frequencies because of its nonuniform grain. Despite this large difference in performance of the two materials in a circuit, they exhibit the same properties when subjected to standard bulk-resistivity tests.

Decreasing the grain size and obtaining thinner grain boundaries are not the only means of increasing bulk resistivity. This summer, TDK will introduce a 1-MHz MnZn ferrite material that features both lower eddy-current and hysteresis losses. Controlled amounts of impurities and low-temperature sintering help the material achieve twice the bulk resistivity of the company's 500-kHz H7C4 material.

No adequate tests

One curious lag between design principles and actual practice is the lack of instrumentation for testing high-frequency magnetic materials. The industry-standard square-wave tests currently employed for lower-frequency magnetic materials will not work at high frequencies. At high frequencies, magnetic-material users must employ sine-wave stimuli.

In addition, the instrumentation needed to take accurate core-loss measurements at high frequencies currently involves fairly strenuous techniques. Accurate results demand that the engineer dunk the core under test in a Dewar flask filled with nonconductive fluid (that is, in a calorimeter) and measure the core's temperature under load. You can also make less strenuous, but also less accurate, core-loss measurements with an inexpensive RF power meter ("inexpensive" means approximately $3500).

If you have neither a Dewar flask nor an RF power meter, you will have to rely on the manufacturers' published data. Unfortunately, not all magnetic-materials makers specify products in the same fashion.

For example, Ferroxcube conservatively specs its new 3F3 MnZn ferrite material for frequencies to 500 kHz. According to the company, however, the 3F3 material is equal to materials that are specified for 1-MHz operation by other companies. Ferroxcube performs production tests of the 3F3 material at 100 and 400 kHz.

Surprisingly, makers of iron transformer cores are not far behind the ferrite-core makers. For example, the Magnetics Division of Spang and Company (formerly Mag Inc) uses a new cobalt-alloy, amorphous-steel (Metglas) material to make tape-wound cores for magnetic amplifiers (also known as saturable reactors). These mag-amp cores can operate efficiently at switching speeds to 250 kHz, as robust post-regulators for multiple-output

For more information . . .

For more information on the magnetic materials described in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

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Circle No 701

Ceramic Magnetics Inc
87 Fairfield Rd
Fairfield, NJ 07006
(201) 227-4222
Circle No 702

Ferroxcube
Div of Amperex Electronic Corp
5083 Kings Hwy
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(914) 246-2811
Circle No 703

Spang and Company
Magnetics Div
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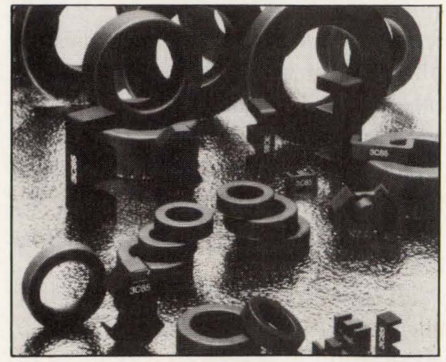

***When fired in a newly designed elevator kiln** instead of an older elevator kiln, Ferroxcube's high-frequency ferrite materials exhibit more uniform specs from batch to batch.*

switchers. The cores cost between $1.34 and $3.70 (100), depending on the size. For designers unfamiliar with mag-amp regulator design, the company can supply several application notes detailing the process.

Of course, obtaining a suitable transformer core isn't the end of the power-supply designer's problems. To a certain extent, the designer is no longer a power engineer so much as an RF engineer. High-frequency switch-mode power supplies change many of a designer's priorities.

Because high-frequency switch-mode power supplies operate at lower flux densities, you need to minimize eddy-current losses rather than reduce hysteresis losses. Also, because the number of turns in the power supply's transformer is small, losses traced to the copper wire become less important at high frequencies. The mechanical layout of the cores and windings are very important, because even very small parasitic capacitances can lead to a significant loss of efficiency at high frequencies. Consequently, engineers are also developing entirely new mechanical configurations for transformers. In short, improved magnetic materials may provide the last piece to the component-choice puzzle, but the design puzzle is just beginning to take shape. **EDN**

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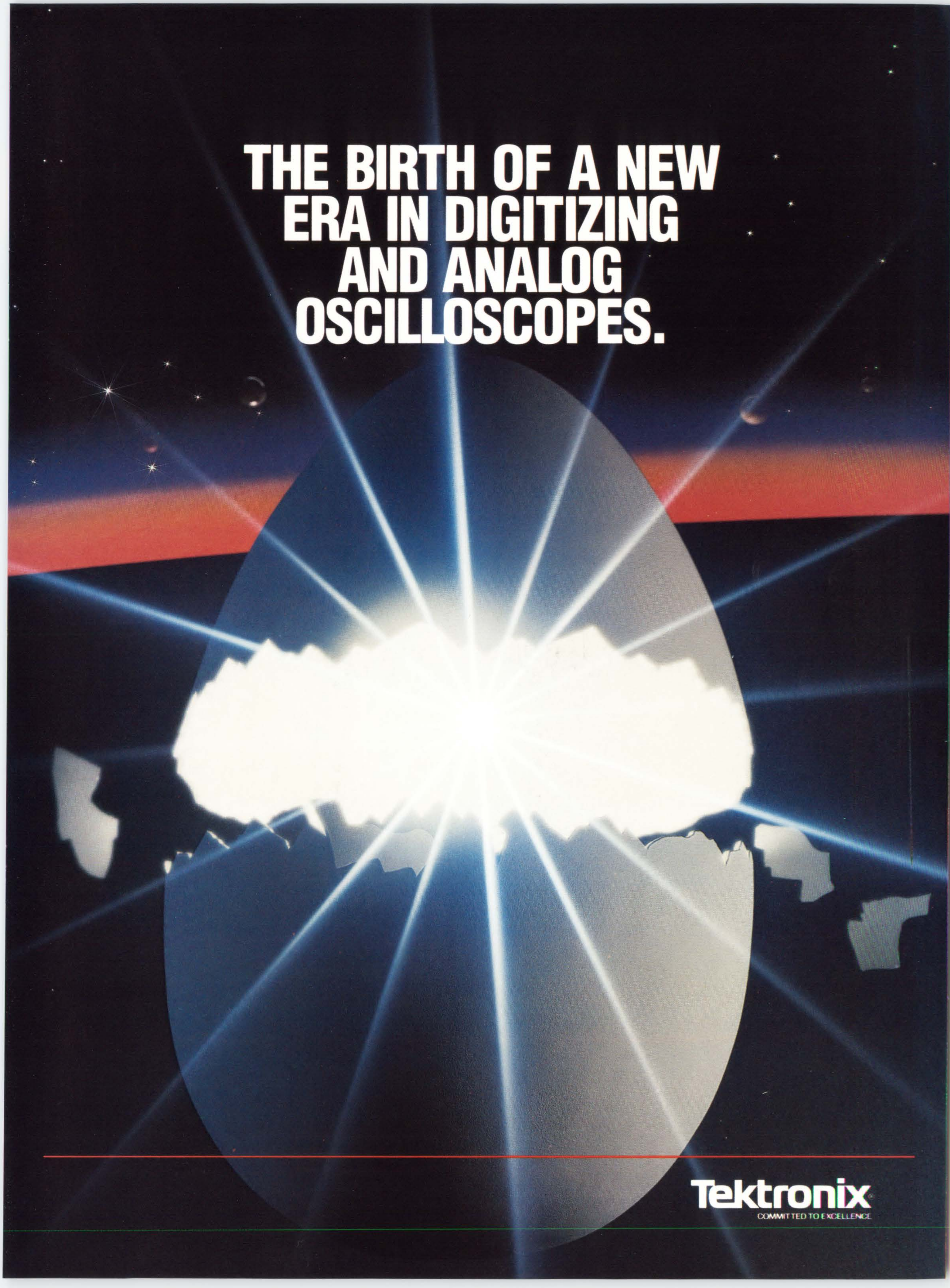
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Vert. Sensitivity[4]	1 mV/div	1mV/div	Vert. Sensitivity[4]	1 mV/div	1 mV/div
Vert. Resolution	10-14 bits[3]	10-14 bits[3]			
Automatic Measurements	Min, Max, Mid, Mean, RMS, Peak-Peak, Rise, Fall, Width, Delay1, Cross, Period, Frequency, Main→Window Trigger, YT Area, YT Energy, Cursors		Automatic Measurements	Peak-Peak, Min, Max, Mid, Frequency, Period, Width, Duty Cycle	
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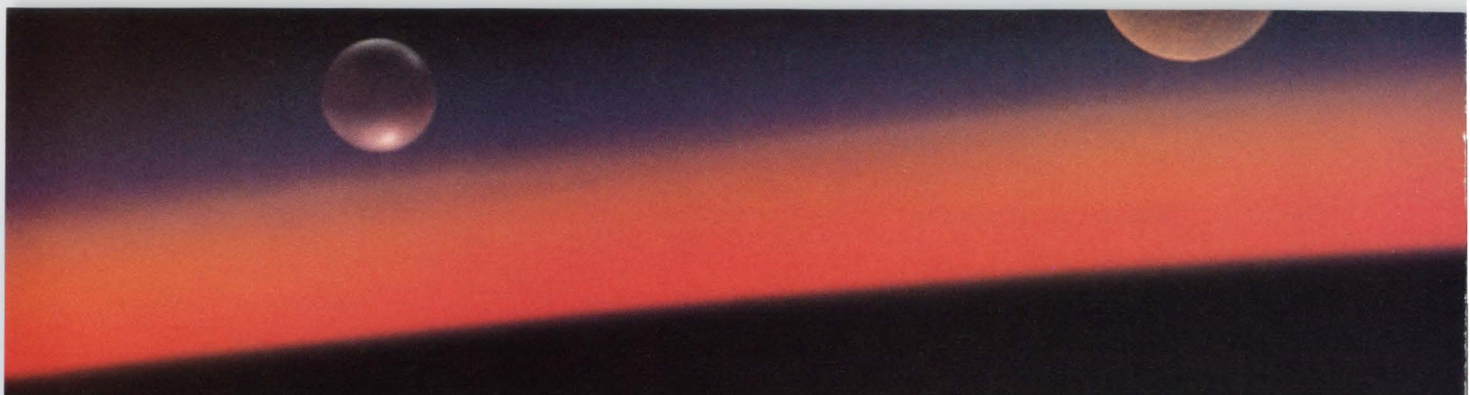
[1]Up to 8 traces may be displayed at once from any of up to 12 input channels.
[2]Absolute DC accuracy with full scale offset or Vc.
[3]14-bit resolution obtained using signal averaging.
[4]Except with 11A71 which has 10mV/div

Demonstrations are now in progress throughout North America. To get in touch with the future of measurement, contact your local Tek sales engineer or call Tektronix at 1-800-547-1512.



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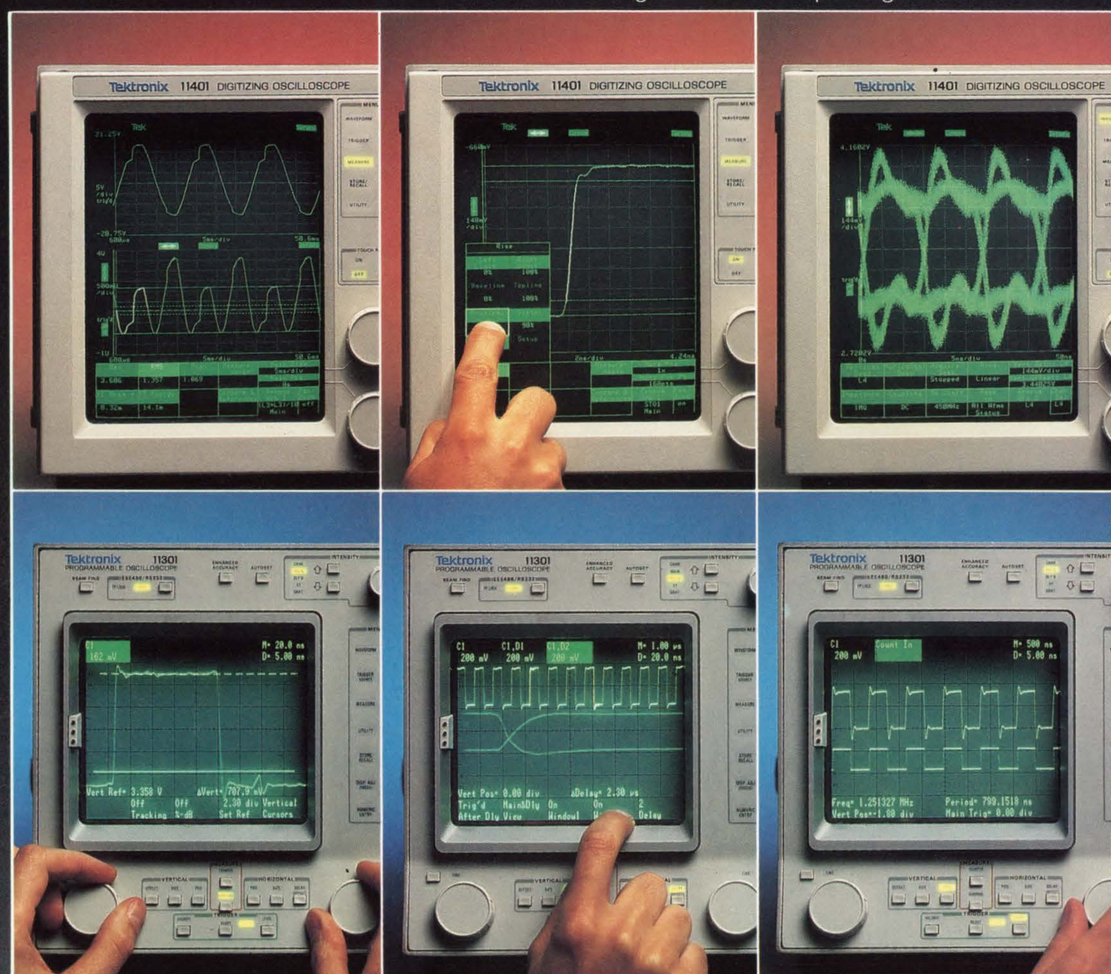

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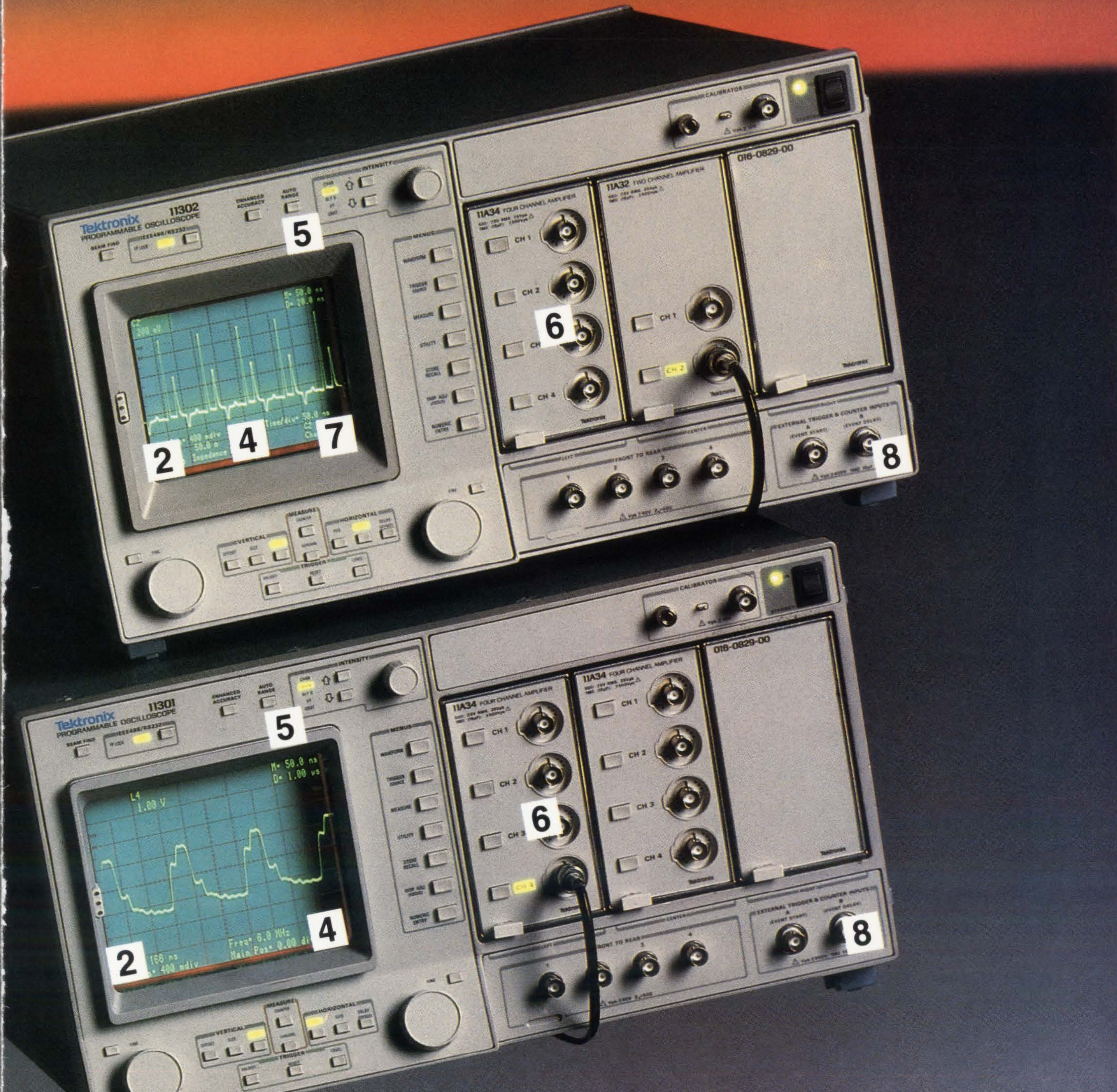

ANALOG

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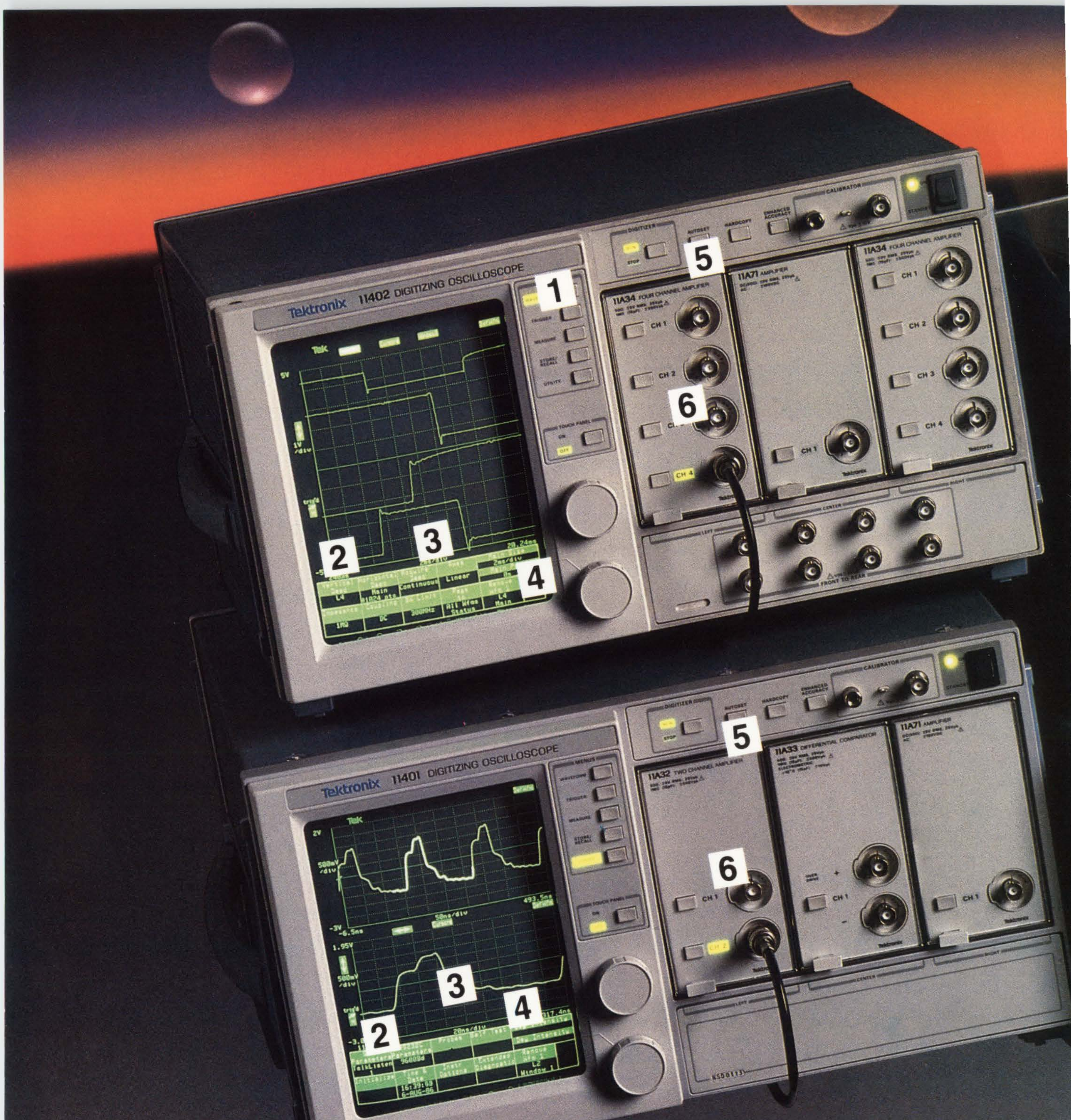

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ADEE West '87 will keep you up to date on chip and system design with CAD/CAE

Joan Morrow,
Assistant Managing Editor

If you need to catch up on developments in computer-aided engineering and design, you won't want to miss the Automated Design and Engineering for Electronics conference. ADEE West '87 takes place from March 31 to April 2 at the Anaheim Convention Center in Anaheim, CA. You can choose among 15 sessions, four short courses, two workshops, and four panel discussions. But leave room on your agen-

ADEE West '87 registration and schedule

The Automated Design and Engineering for Electronics conference—ADEE West '87—will be held on March 31 to April 2 at the Anaheim Convention Center in Anaheim, CA. The conference will include 15 sessions, four short courses, and two workshops. If you plan to attend the courses and workshops, you'll need a separate registration. For more information, you can contact the Show Manager, ADEE West '87, Cahners Exposition Group, 1350 E Touhy Ave, Des Plaines, IL; phone (312) 299-9311. For a preview of the conference sessions, consult the schedule below.

TIME	MONDAY, MARCH 30	TUESDAY, MARCH 31		WEDNESDAY, APRIL 1		THURSDAY, APRIL 2	
9:30 AM	SHORT COURSE 1 CAE/CAD SYSTEMS: SELECTION, JUSTIFICATION AND IMPLEMENTATION PART ONE	SESSION 1	SYSTEM DESIGN AUTOMATION: SIMULATION AND VALIDATION	SESSION 7	EVALUATING THE PAYBACK OF CAE TOOLS	SESSION 13	INTEGRATING DOCUMENTATION INTO THE CAD/CAE ENVIRONMENT
		SESSION 2	PRINTED CIRCUIT DESIGN METHODOLOGIES	SESSION 8	INTERFACING PRINTED CIRCUIT DESIGN WITH MANUFACTURING	SESSION 14	USING FAULT SIMULATION: AN EXAMINATION OF PRACTICAL APPROACHES
	SHORT COURSE 2 AN OVERVIEW OF VLSI ASIC DESIGN AND TECHNOLOGIES PART ONE	SESSION 3	AUTOMATION OF THE ASIC DESIGN PROCESS	SESSION 9	LOGIC SIMULATION	SESSION 15	SILICON COMPILATION USERS' VIEWS
		SHORT COURSE 3	VLSI ASIC DESIGN WORKSHOP PART ONE	SHORT COURSE 4	DESIGNING FOR TESTABILITY: THEORY AND PRACTICE PART ONE	WORKSHOP 2	COMPUTERIZED METHODOLOGIES FOR PCB CAD
1:00 PM	SHORT COURSE 1 CAE/CAD SYSTEMS: SELECTION, JUSTIFICATION AND IMPLEMENTATION PART TWO	SESSION 4	CAD SYSTEM INTEGRATION AND DATA STANDARDS	SESSION 10	CAE FOR SEMI-CUSTOM IC DESIGN		
		SESSION 5	USER STRATEGIES FOR PLACE AND ROUTE IN PRINTED CIRCUIT LAYOUT	SESSION 11	TO CAD OR NOT TO CAD: USERS' EXPERIENCES WITH AUTOMATED ELECTRONIC DESIGN TOOLS		
	SHORT COURSE 2 AN OVERVIEW OF VLSI ASIC DESIGN AND TECHNOLOGIES PART TWO	SESSION 6	SOFTWARE TOOLS FOR ANALOG DESIGN	SESSION 12	ASIC PHYSICAL DESIGN		
		SHORT COURSE 3	VLSI ASIC DESIGN WORKSHOP PART TWO	SHORT COURSE 4	DESIGNING FOR TESTABILITY: THEORY AND PRACTICE PART TWO		
				WORKSHOP 1	SMT DESIGN AND LAYOUT		
3:30 PM		PANEL DISCUSSION 1	BOARD LEVEL SIMULATION: IMPACT AND TRENDS	PANEL DISCUSSION 3	LIBRARY SYMBOL AND MODEL STANDARDIZATION		
		PANEL DISCUSSION 2	THE VIABILITY OF DESKTOP ENGINEERING	PANEL DISCUSSION 4	THE ROLE OF CASE IN ELECTRONIC SYSTEM DEVELOPMENT		

da for evaluating new products—numerous companies will be exhibiting their latest innovations.

New on the docket this year is an exhibit called Circuitpath, which will demonstrate how to ease the integration of CAD/CAE hardware and software from various manufacturers. The exhibit links equipment from such manufacturers as Harris CAD, Gerber Scientific, FutureNet, Digital Equipment Corp, and Valid Logic Systems via a common local-area network using the TCP/IP communications protocol. During the conference, Circuitpath will design a multilayer pc board and a standard-cell IC. At different stations in this exhibit, you'll be able to see everything from circuit design and layout to documentation and plotting.

The conference sessions will mirror what Circuitpath demonstrates. For example, **session 3** will focus on the automation of application-specific IC designs. Speakers from VTC Inc, NCR, Micronix Integrated Systems, and Harris Semiconductor will detail how to combine analog functions, μPs, memory, and other high-level functions on one ASIC. And in **session 12**, speakers will present papers on gate-array layout, cell-based layout, "sea of gates" layout techniques, and management issues.

"CAE for semicustom-IC design" is the topic of **session 10**. During this session, speakers will present papers entitled, "Analog/digital simulation," "ASIC vendor CAE limitations," "CAE for semicustom ECL design," and "AI applications in CAE."

The discussions in **session 2**—"Printed-circuit design methodologies"—will attempt to cover many of the aspects of designing complex boards. Speakers will present five papers: "Bridging the gap (product-design groups vs printed-wiring design)," "Unravelling the routers: finding your way through the maze of placement and routing algorithms," "Gridless and gridded PCB routing," "Rules-based router meets completion/design rule requirements," and "Advanced routing technologies."

Users' viewpoints

At least two of the conference sessions will be devoted to the experience of users. In **session 11**, panelists will describe their experiences using automated-design tools for ICs, pc boards, and board-level systems. In **session 18**, four speakers will describe their trials and tribulations with silicon compliers.

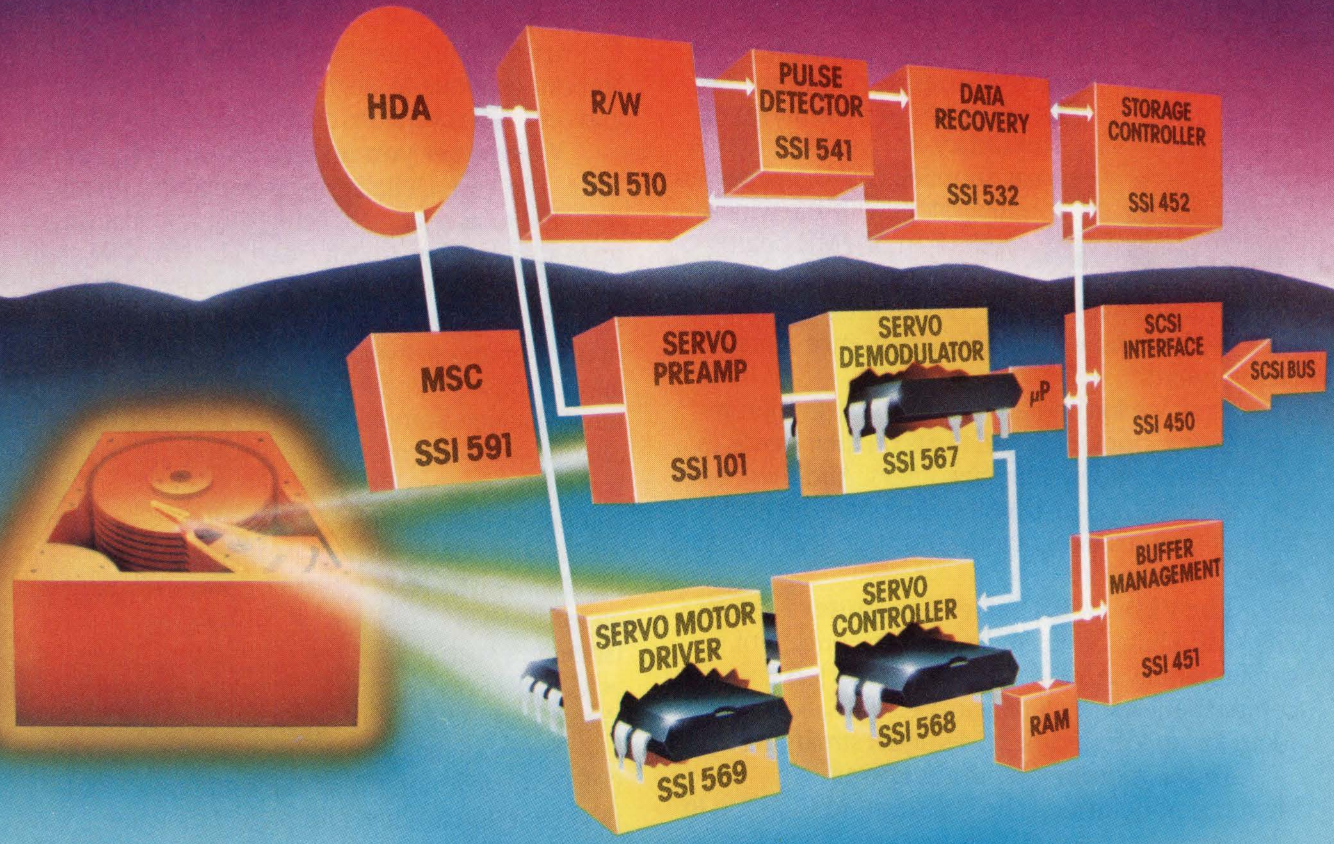
In addition to the 15 sessions, the conference program includes four full-day courses. "CAE/CAD systems: selection, justification, and implementation" and "An overview of VLSI ASIC design and technologies" will be conducted on March 30. The first course, which targets those in charge of selecting a CAD/CAM/CAE system, will cover system requirements, and then show you how to find vendors, screen systems, develop operations, and track productivity. The second course will describe gate arrays and compare them with other technologies and provide an overview of gate-array design.

Short course 3, "VLSI ASIC design workshop," which begins on Tuesday morning, will teach attendees how to anticipate the problems that can occur in each phase of ASIC design. Short course 4, "Design for testability: theory and practice," scheduled for Wednesday morning and afternoon, will cover a variety of design-for-testability methods and show how you can modify a testability technique for your circuits.

Two workshops—one on surface-mount design and layout and the other on methodologies for pc-board CAD—and four panel discussions round out the agenda. **EDN**

Article Interest Quotient
(Circle One)
High 512 Medium 513 Low 514

NEW FROM SILICON SYSTEMS— A SERVO CHIP SET FOR HIGH PERFORMANCE HDD's!



Silicon Systems now introduces the SSI Servo Chip Set. It is a 3-chip servo set for precise head positioning in the new high-performance hard disk drives. This is just the latest development in the company's program for the full integration of disk drive electronics.

The new set consists of the SSI 567 Servo Demodulator, which provides servo demodulation for dedicated-surface servo systems; the SSI 568 Servo Controller, which provides servo control; and the SSI 569 Servo Motor Driver, which is a voice coil servo motor predriver that is compatible with complementary power FETS. The chip set includes all the functional building blocks required in the servo channel, and is easily controlled via the microprocessor interface.

This chip set will break down major barriers to entry into the development of high performance hard disk drives. With its high level of integration, it provides superior performance and features for lower power, reduced board space, and lower cost.

For more information on the new SSI Servo Chip Set and the other exciting product families in the complete ESDI and SCSI Chip Sets for HDD and FDD disk drive electronics, contact Silicon Systems today.

Silicon Systems, 14351 Myford Road, Tustin, CA 92680. Phone: (714) 731-7110, Ext. 575.

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Circle no. 38 for Product Information

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We've taken our to its next logical

Introducing the VME Delta Series™ Computer System: The ultimate in system-level flexibility. For years, Motorola has supplied OEMs and system integrators with the widest selection of VME boards on the market–all based on the most advanced VMEbus technology available.

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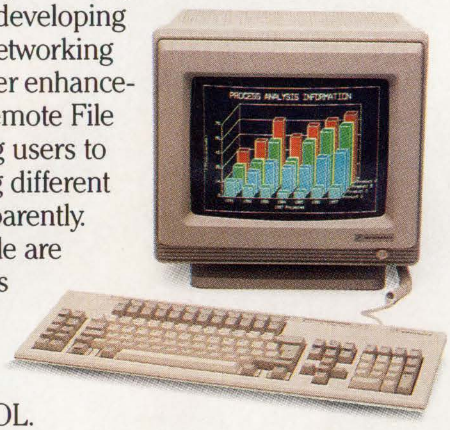
The VME Delta Series Computer System. The VME Delta Series redefines the concept of configurability in VME systems. For starters, take its compact enclosure. It contains 12 VME slots–plus room for up to four disk drives and a streaming tape.

Major memory configurations. Main memory includes both parity and ECC. Up to 1.3 Gigabytes of mass storage is satisfied by a family of ST-506, ESDI and SMD disks. Quarter-inch streaming tape backup and half-inch, 9-track tape drives are available.

Unsurpassed communications with other worlds. Through intelligent communication controllers, the VME Delta Series can handle data from local or remote asynchronous devices. Industry standard communications networks and host computers can be connected using protocols such as SNA, Bisynch and more. For high-speed, local area networking, Ethernet® and TCP/IP controllers are available.

From MC68020 to the next generation–just plug in the board. By adhering to industry-wide standards, the open architecture of the VME Delta Series assures the future viability of your product. Its system CPU uses the popular MC68020 microprocessor. You can continue to upgrade to new generations and even faster versions as they become available.

We can get you up and running in record time. The VME Delta Series is available with all the OEM tools needed to bring your applications up to speed and up to date–fast! The UNIX® System V/68™ Release 3 operating system offers a rich environment for developing multi-user and networking applications. Other enhancements include Remote File Sharing–allowing users to share files among different computers transparently.



Also available are development tools and high-level languages such as C, FORTRAN, Pascal, and COBOL.

Powerful data management software includes UNIFY,® Oracle,® Informix,® color graphics, word processor, spreadsheet and project manager.

The team behind your team: Our Microcomputer Division team can help your OEM team with application and technical support through 100 field offices located world-wide.

We also provide comprehensive support in a wide variety of other areas–software and application update newsletters and a toll-free hotline–such as the one below.

Use it now–to find out more about our new Microcomputer Division in general and more about the VME Delta Series in particular.

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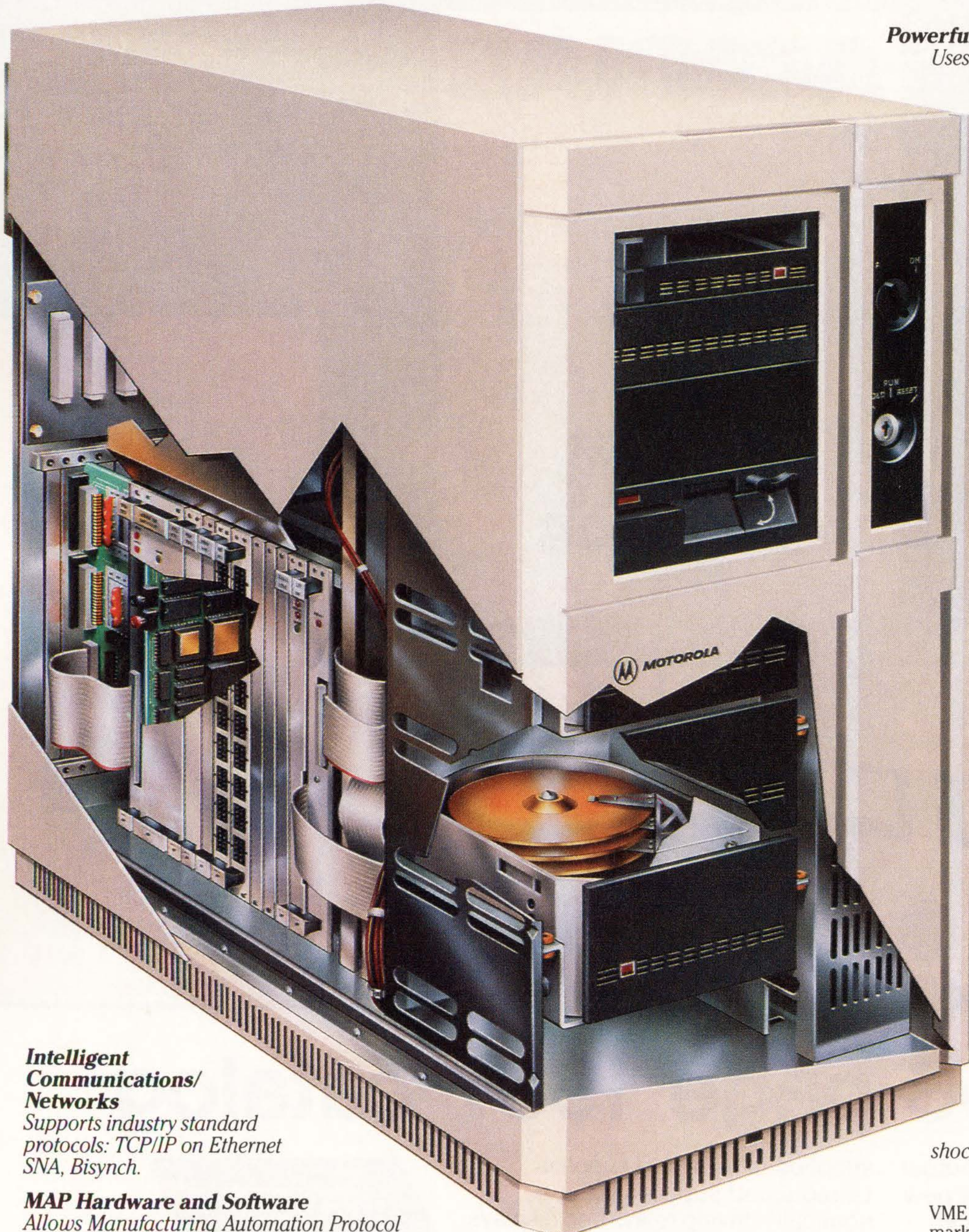
VME experience conclusion.



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Uses 32-bit MC68020 MPU and MC68881 Floating Point co-processor; easy upgrade to next generations.

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Uses SYSTEM V/68–compliant with AT&T's UNIX System V Release 3 with RFS for easy system networking. Real-time executives are available.

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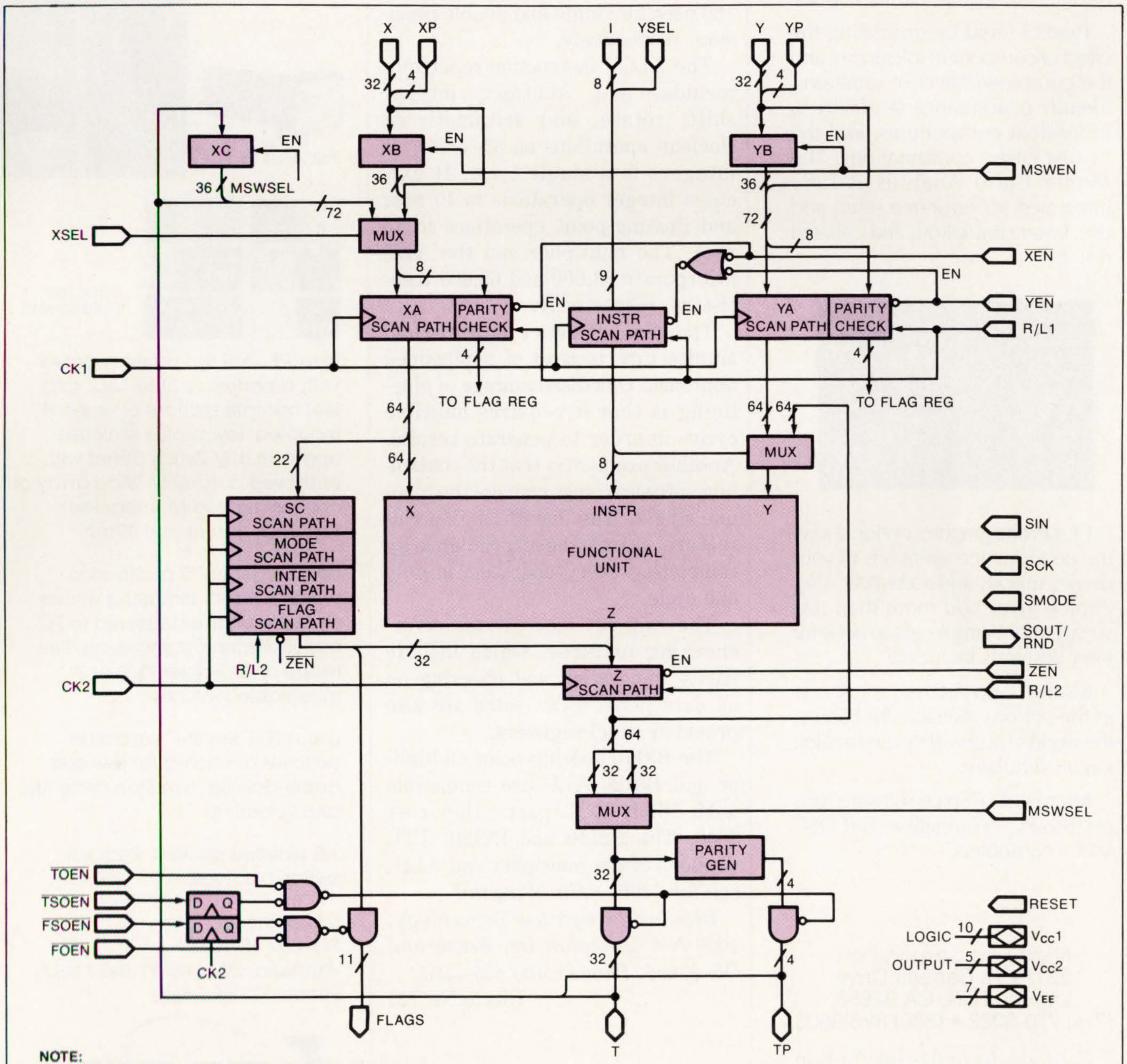
CIRCLE NO 53

Floating-point chip set executes 60M flops, comes in ECL- and TTL-compatible versions

The B3110/B3120 floating-point chip set executes 60M nonpipelined, 64-bit floating-point operations per second. The set comprises a multiplier and an arithmetic logic unit (ALU), and it supports both the IEEE-754 and the DEC F and G floating-point formats.

The multiplier performs single-precision (32-bit) or double-precision (64-bit) floating-point multiplication, division, square-root



Comprising a multiplier and an ALU, *the 10 KH ECL-compatible B3110/B3120 floating-point chip set uses a flow-through architecture that skirts the problems of pipelining by completing every operation in only one cycle.*

UPDATE

calculation, or 32×32-bit integer multiplication in a single cycle. Its division and square-root instructions don't require external seed or look-up-table storage. The chip accomplishes single-precision multiplication in 35 nsec and double-precision multiplication in 45 nsec. It calculates square roots in as little as 170 nsec (single precision) or 325 nsec (double precision). Its worst-case division times are 105 nsec and 180 nsec for single and double precision, respectively.

The ALU's instruction repertoire includes add, subtract, integer shift, rotate, and arithmetic or Boolean operations on 32- or 64-bit integers in a single cycle. It executes integer operations in 10 nsec and floating-point operations in 25 nsec. The multiplier and the ALU incorporate 63,000 and 65,000 transistors, respectively.

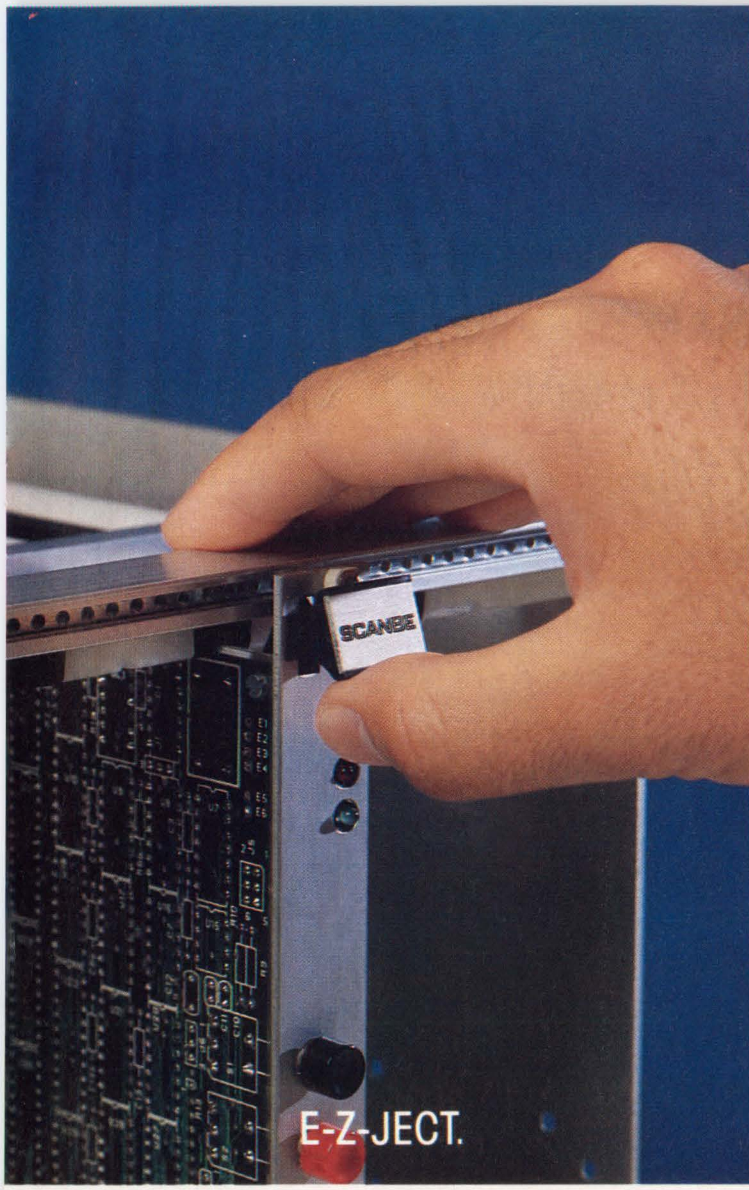
The chip set uses a flow-through architecture instead of a pipelined approach. One disadvantage of pipelining is that it requires multiple cycles in order to generate results. Another problem is that the controlling software must manage the pipeline stages. The flow-through architecture skirts these problems by completing every operation in only one cycle.

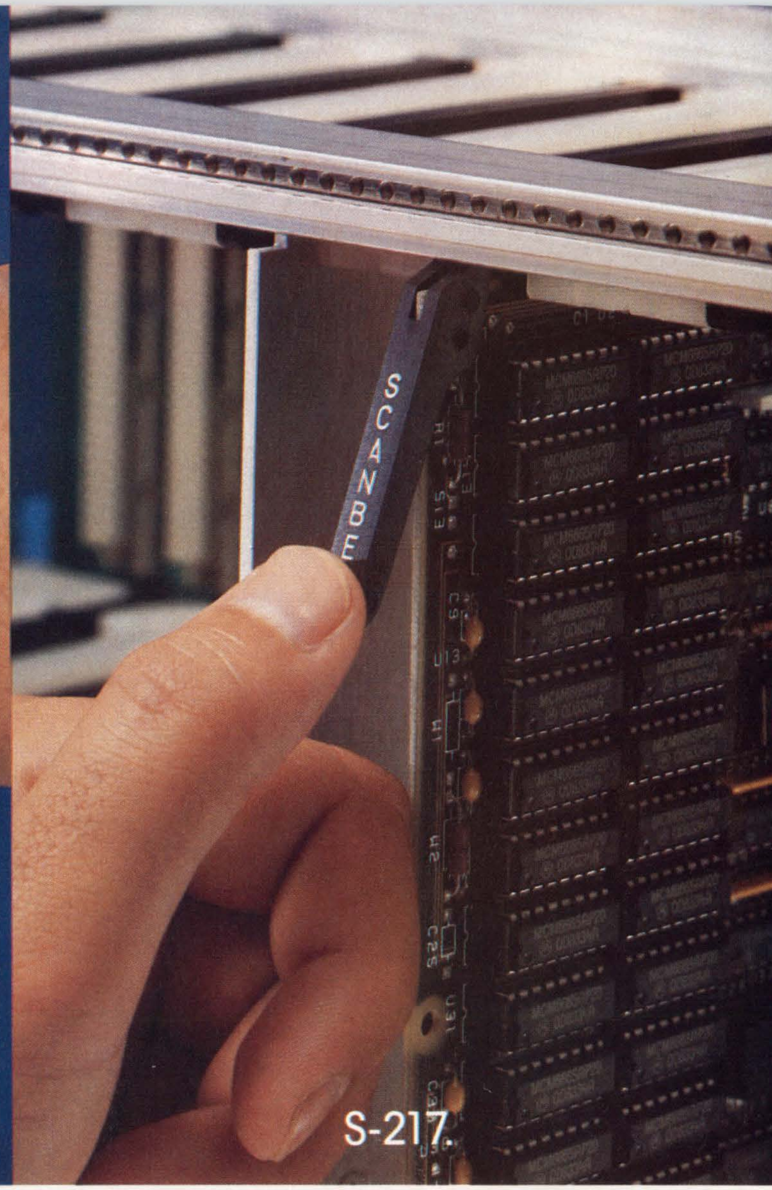
The chip set incorporates error-checking features, which include parity generation and checking on all data ports. Scan paths are also provided on all registers.

The B3110 floating-point multiplier and B3120 ALU are compatible with 10KH ECL parts; they cost $640. The B2110 and B2120, TTL versions of the multiplier and ALU, sell for $490.—***Jim Wiegand***

Bipolar Integrated Technology, 1050 NW Compton Dr, Beaverton, OR 97006. Phone (503) 629-5490.

Circle No 725





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CIRCLE NO 127

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This 5″ x 8″ x 11″ high power-density 1500-Watt unit from Advance Power Supplies provides 3.4 Watts per cubic inch from either 110V or 220V nominal, 47 to 440 Hz input. It's perfect for systems using large amounts of solid-state mass storage.

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Standard features include electronic soft-start; self-diagnostics; overcurrent, overvoltage and overtemperature protection; selectable dual-input voltage; local and remote sensing; and full-cycle holdup. A variety of signal facilities and optional output voltages (2V, 12V, 24V, 48V) make the Powermag A1500 one of the most versatile power supplies available.

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CIRCLE NO 52

703-008

Low-cost, digital pattern generator specs 35-MHz, 64k-bit performance

For $6995 you can buy a 35-MHz digital pattern generator, recorder, and analyzer that handles 16 to 72 64k-bit data channels. The DataSource-8600 is a hardware/software package that plugs into your IBM PC or into a compatible computer to perform real-time data recording, data-stream comparison, and error detection at frequencies ranging from 0.3 Hz to 35 MHz with 0.01% accuracy.

The product's hardware includes a benchtop or rack-mountable chassis that comes with two 8-channel cards and TTL or CMOS probes. You expand the system to the 72-channel limit by adding more cards and probes. Each card provides 64k bits of pattern memory per channel. A half-length expansion card connects the chassis to any IBM PC or compatible computer; you insert it into the PC, and it provides its own bus to handle high-speed data reception. You are therefore not restricted by the slow performance associated with RS-232C and IEEE interfaces, which use the PC bus. You can designate each channel as an input or an output, and you can obtain a printout of generated data patterns.

It's the WaveEdit software, however, that distinguishes this product. Referred to by its developers as "a wordprocessor for waveforms," the program uses pop-up help windows, menus, and interactive color graphics to guide you through waveform-design commands such as counter and clock creation, channel concatenation based on Boolean logic, and waveform inversion.

WaveEdit also lets you copy and move sections of waveforms, much in the way a wordprocessor lets you copy and move sections of text. The display window shows as many as 16 channels; horizontal and vertical scrolling and paging let you scan additional patterns. The software highlights comparison errors between waveforms. You can also name and annotate channels, elect binary or hexadecimal data display, and select horizontal scales ranging from 32 bits to 64k bits.

If speed isn't a critical factor in your waveform analysis, however, you may want to order μSource instead. Priced at $395, this software-driven pattern generator and analyzer offers the same functions as the DataSource-8600, but at frequencies reaching only 50 kHz when used with a 6-MHz 80286-based computer (a standard 8086-based PC performs at approximately 20 kHz). Besides the software (which is 95% compatible with the DataSource version), you receive an interface card and a 16-channel TTL/CMOS probe.

Additional 8-channel card/probe sets for the DataSource-8600 cost $1295 (5). Extra 16-channel μSource probes cost $195. The manufacturer also offers a free demonstration disk that reviews the WaveEdit functions and lets you compose waveforms.—***J D Mosley***

Analytic Instruments Corp, Box 20340, Dallas, TX 75220. Phone (214) 357-3882.

Circle No 726

Boasting a 35-MHz clock rate and the capacity for 72 channels, *the DataSource-8600 turns your computer into a low-cost, high-performance digital pattern generator, recorder, and analyzer.*

Compact magnetic rotary encoder operates in harsh environments

The Model RE10 magnetic rotary encoder bridges the gap between industrial encoders and open-frame kits, offering a useful alternative that combines the best features of both. Instead of relying on electromechanical wiper contacts or optical components, which require a good deal of volume to accommodate alignment and focusing, the RE-10 employs high-density magnetic materials to achieve its compact size—14.3 mm in thickness by 38.5 mm in diameter.

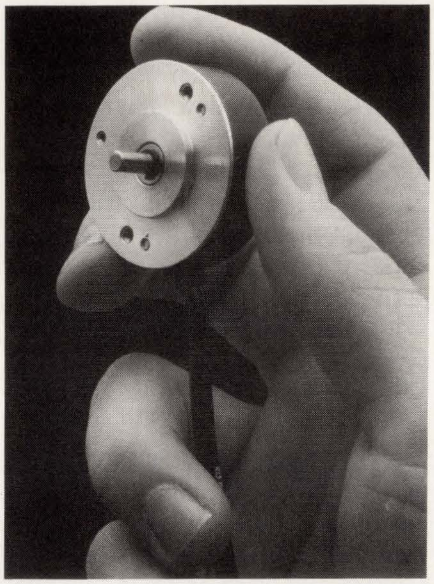
Model RE10 offers a selection of seven angular resolutions ranging to 2048 counts per revolution; the maximum rotational speed is 5000 rpm. The lightweight unit (40 grams) comes in a protective, shielded case; you can design it into tight spaces with little concern for accumulation of dirt, splashes of oil, and other hazards that would degrade the reliability of optical encoders.

Whether the RE10 is operating as a tachometer or as a shaft-position encoder, it connects to the host equipment via an optional universal coupler and rotor shaft. The encoder accommodates radial and axial shaft loads of 1 and 0.5 kg, respectively.

Inside, the 4-mm rotor shaft terminates in a nonferrous aluminum wheel (¾ in. in diameter and ⅛ in. thick). A plastic toroid-shaped magnet, integrated onto the circumference of the wheel, is made up of a rare-earth samarium cobalt magnetic material suspended in a polymer base.

A look inside

The manufacturer records magnetic domains in the circular plastic magnet, at selected pitches that define the encoder's angular resolution. A magneto-resistive read head is positioned tangentially to the wheel's circumference and separated by an air gap of about 0.02 in. The read head is fabricated on a ceramic substrate and comprises a thick-film resistive element that effectively changes its resistance under the influence of an external magnetic field.



A compact, lightweight unit, *the RE-10 magnetic rotary encoder works well in tight spaces, and it's impervious to accumulations of dirt, splashes of oil, and other hazards that would degrade the reliability of an optical encoder.*

A bias current flows in the read head. As encoded domains sweep by the read head, they alternately oppose and aid the bias current's own inherent flux fields, modulating the bias current. Subsequent modulations are directly analagous to the speed and polarity of the magnetic domains as they pass by the read head.

Because of the large air gap separating the wheel from the read head, and because the read head is located at the edge of the wheel rather than at its face, no alignment in the assembly has to be precise. Even under extreme ambient conditions and heavy shaft loading, the encoder operates reliably because there are no critical part tolerances or alignments as in optical encoders.

CMOS hybrid processes outputs

As magnetic domains sweep past the sine and cosine sense elements, they produce two sinusoidal signals (A and B) in quadrature phase. These signals are amplified, squared, processed, and buffered in a 5V CMOS hybrid circuit. Two open-collector npn transistors, each of which can sink 30 mA, send the electrical output to the host circuitry. The CMOS hybrid circuit's metal housing shields against ambient magnetic fields and RFI.

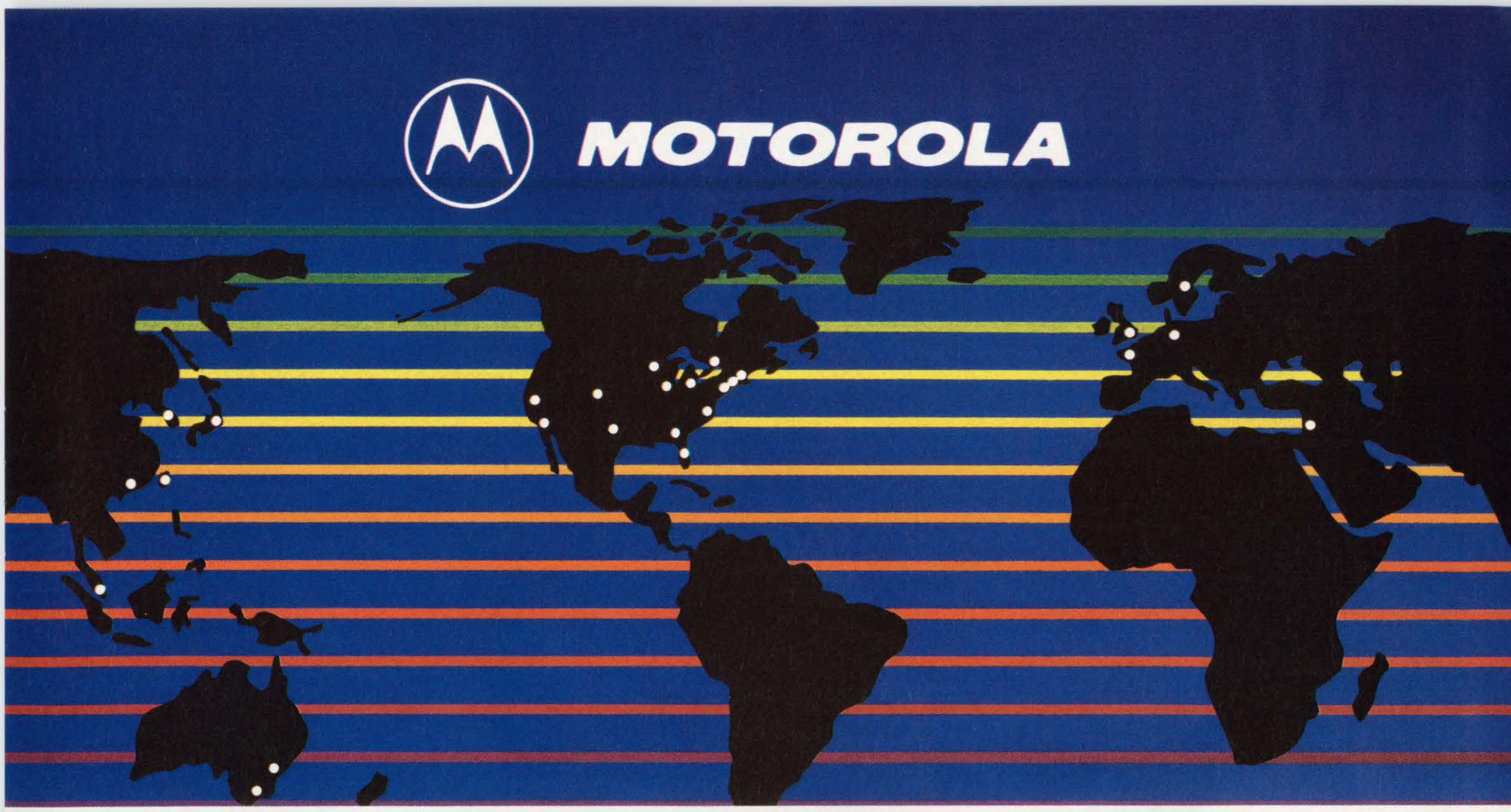
You order the device according to the way the wheel is encoded at the factory. For a resolution of 2048 counts per revolution, you would order the encoder with a -512 suffix. Currently, there are seven suffix numbers available: -512, -500, -400, -360, -256, -200, and -100. The RE10-100 features a resolution of 400 counts per revolution. The maximum output frequency of any of the seven models is 100 kHz.

The units operate from a 5V supply and consume 150 mW max. The operating range spans −10 to +60°C, and the maximum operating humidity equals 95%. The required starting torque is 10 g-cm max; the shaft, wheel, and bearings produce a 2.5 g-cm^2 max moment of inertia. Encoder, $111; coupler, $9.

—Tom Ormond

National Machine Systems Inc, 137 Bristol Lane, Orange, CA 92665. Phone (714) 921-0630.

Circle No 728



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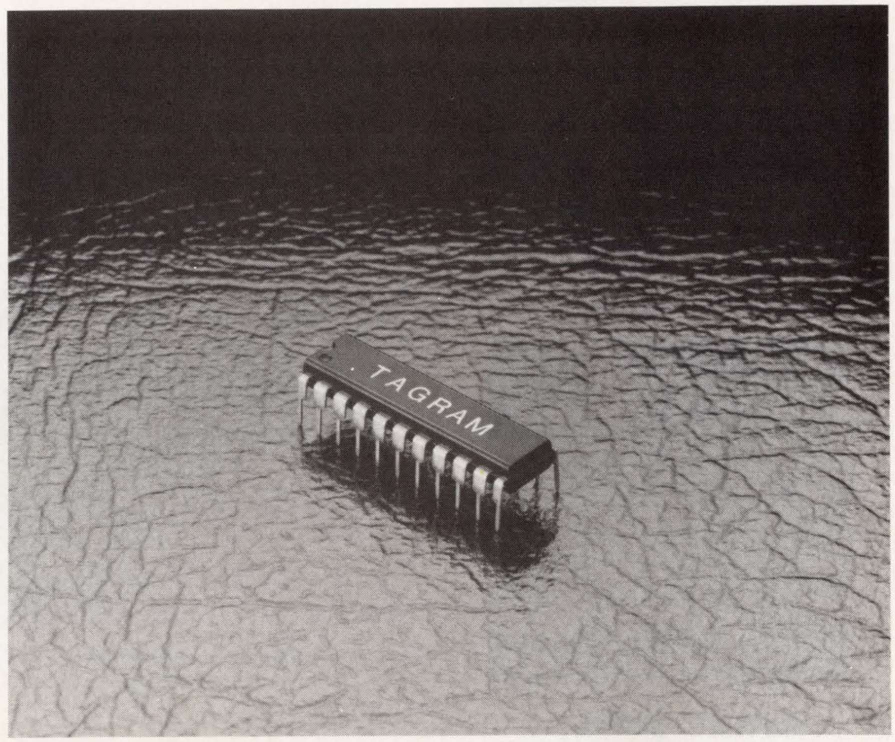
CIRCLE NO 18

20-nsec cache RAM features on-chip comparator



Boasting a 30% improvement in speed *over that of similar RAMs that use external, discrete comparator circuits, the MK41H80 Tagram static RAM also provides a Flash Clear function and full-speed read access.*

Eliminating any need for an external comparator circuit, the MK41H80 Tagram, a 4k×4-bit static RAM, is suitable for use in cache-tag applications. The chip contains a 4-bit comparator that compares RAM contents to current input data in as little as 12 nsec.

The MK41H80 compares the contents of addressed RAM locations to current data inputs. An output of logical one on the chip's Match pin indicates that the input data and the RAM contents match. You can connect the Match pins of several Tagrams to provide Enable or Acknowledge signals to a data cache or μP.

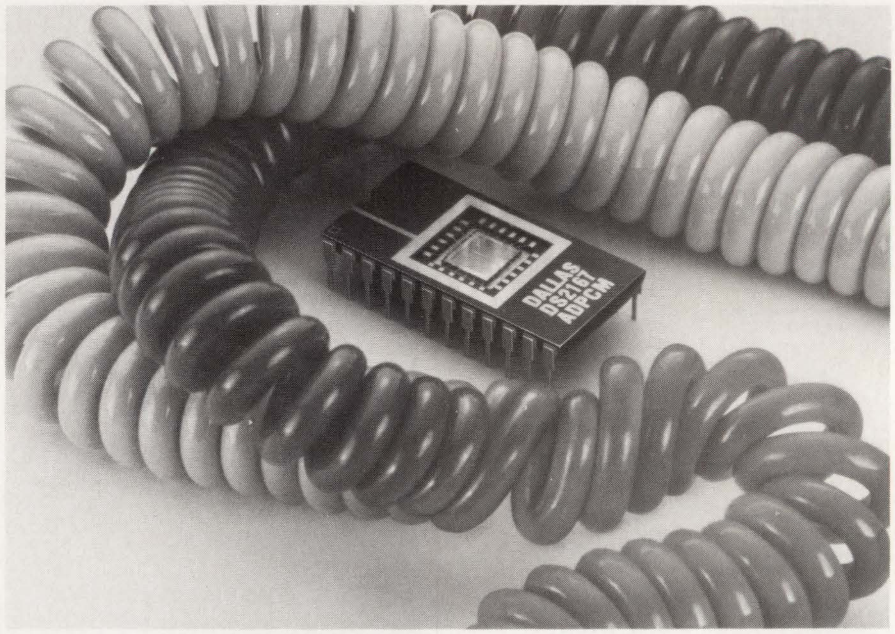
The part's Flash Clear feature lets you clear all RAM bits to logical zero in 40 nsec or less. The Tagram also gives you full-speed read access to the RAM's contents, thus reducing the possibility that the Tagram will induce delays in circuits controlled by high-speed μPs.

You can order the Tagram with an address- and match-access time as low as 20 nsec. Other versions spec 25- and 35-nsec access times. The Tagram operates from a single 5V power supply. Its inputs and outputs are TTL compatible and are protected against static discharge. Available in a 22-pin, 300-mil plastic or ceramic DIP, the Tagram ranges in price from $10.19 to $22.50 (100).—***J D Mosley***

Thomson Components-Mostek Corp, 1310 Electronics Dr, Carrollton, TX 75006. Phone (214) 466-6000. TLX 730643.

Circle No 727

Voice-compression chip doubles T1-line capacity



By compressing the speech bit rate *for telephone voice transmissions from 64k to 32k bps, Dallas Semiconductor's DS2167 ADPCM processor lets you double the capacity of T1 networks.*

The DS2167 combines a digital signal processor (DSP) with an algorithm known as Adaptive Differential Pulse Code Modulation (ADPCM) on a single chip. The result is a voice-transmission rate of 32k bps, which effectively doubles the capacity of 64k-bps full-duplex telephone links.

The ADPCM algorithm allows the DS2167 to conform to the latest CCITT standards while dividing the bit rate for standard speech transmission. The algorithm was developed by CCITT and enhanced by T1Y1 (a North American standards body) to facilitate full-duplex compression and expansion of a voice channel.

In T1 networks, the DS2167 doubles the transmission capability of existing equipment without any need for extensive modification. Thus, you can expand your 24-voice-channel T1 line to accommodate 48 channels by splicing one DS2167 chip per voice channel into each end of the T1 line.

You can also use this chip to integrate voice and data services. The DS2167 offers transmission capabilities that are similar to the Integrated Services Digital Network (ISDN), because the reduced voice-transmission bandwidth lets you combine voice and data transmission on a single line. Such a voice-compression function previously required an entire pc board of electronics. The 24-pin CMOS IC consumes less than 150 mW and costs $39 (1000).—***J D Mosley***

Dallas Semiconductor Inc, 4350 Beltwood Parkway, Dallas, TX 75234. Phone (214) 450-0446.

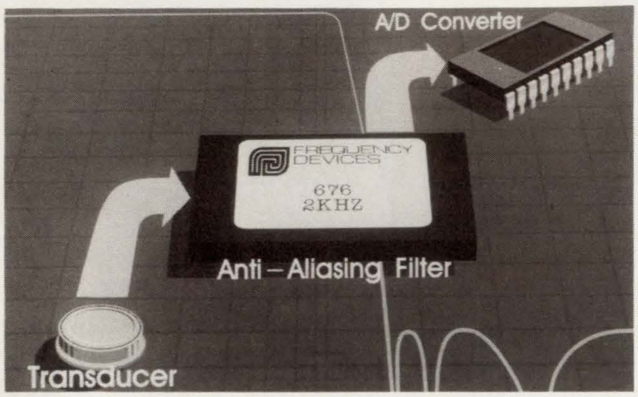
Circle No 729

For more confidence in your scope measurements...

No. 2 in a series from HP.

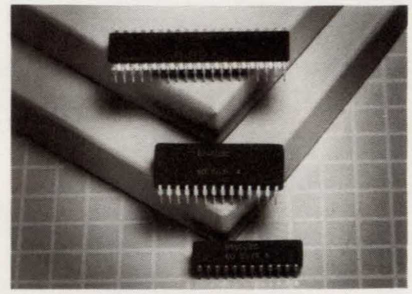
READERS' CHOICE

Of all the new products covered in EDN's **December 25, 1986**, issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, or refer to the indicated pages in our **December 25, 1986**, issue.



▲ ANTIALIASING FILTERS

The 650 and 670 Series antialiasing filters offer close unit-to-unit gain and phase matching; they're designed for use as input filters for 8-, 10-, 12-, and 14-bit A/D converters (pg 133).
Frequency Devices Inc.
Circle No 605

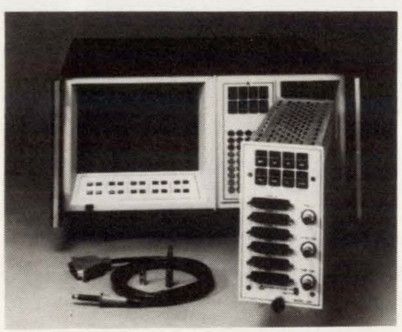


▲VIDEO D/A CONVERTER

The Bt109 triple video D/A converter is an ECL device that suits application in high-resolution (to 2048×1536-pixel) color graphics systems (pg 38).
Brooktree Corp.
Circle No 601

SOLID-STATE EL DISPLAY

Model MD640.200 thin-film electroluminescent display accommodates 25-line, 80-character text and 640×200-pixel graphics for MS-DOS applications (pg 134).
Finlux Inc.
Circle No 606

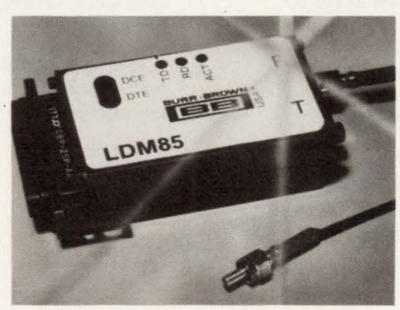


▲ WAVEFORM DIGITIZER

Model 640, a plug-in for the company's Data 6000 mainframe, can capture repetitive signals at frequencies as high as 1 GHz at a resolution of 16 bits (pg 110).
Data Precision.
Circle No 604

CAD FOR PC

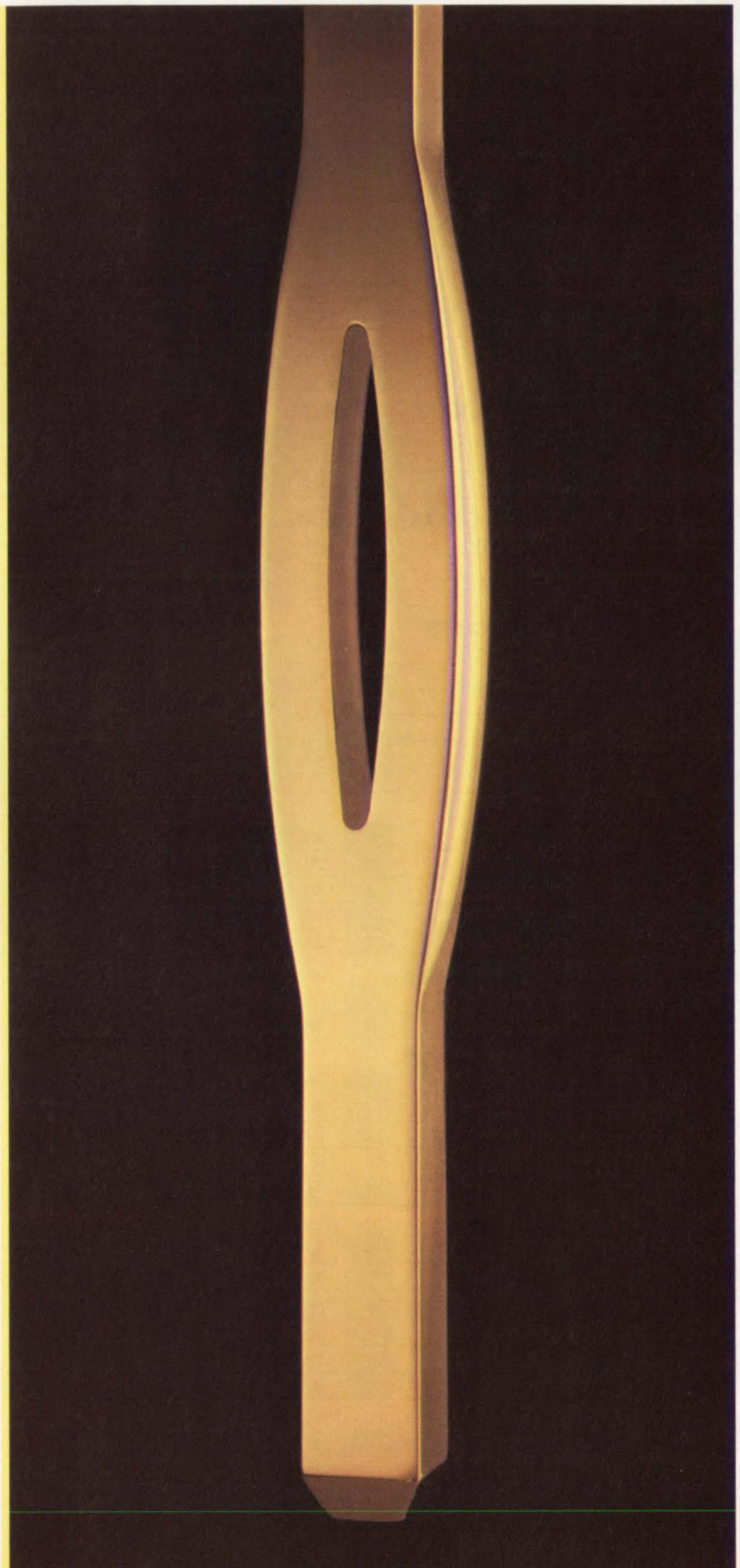
DiaCAD is a CAD software package that runs on the IBM PC and compatible computers having only 256k bytes of memory and one floppy-disk drive (pg 92).
Diacad Associates.
Circle No 603



◀ FIBER-OPTIC MODEM

The LDM85 fiber-optic modem offers multidrop capability: You can connect several stations of the associated data terminal equipment along a single line (pg 61).
Burr-Brown Corp.
Circle No 602

We Have A Fit Over The Competition.

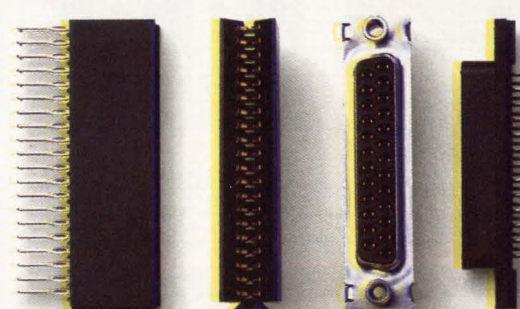


Viking compliant pin connectors will give you a better fit than anyone else's. Our proprietary finishing process produces round, slippery-smooth surfaces on the flexible twin beams of our "eye of the needle" design – on both card-edge and D-subminiature connectors.

This superior process gives you equal insertion and retention forces. And a solid mechanical and electrical fit. It virtually eliminates radial and axial damage to plated thru-holes. In all your printed circuit boards – .062", .093" or .125" thick.

Viking compliant pin connectors help you cut production time and expense and help you produce a higher quality product.

Get complete details on card-edge and D-subminiature compliant pin connectors. Your best contact is Viking Connectors Co., 21001 Nordhoff Street, Chatsworth, CA 91311. Phone (818) 341-4330.



Compliant Pin Connectors

Viking

CIRCLE NO 143

LEADTIME INDEX

Percentage of respondents

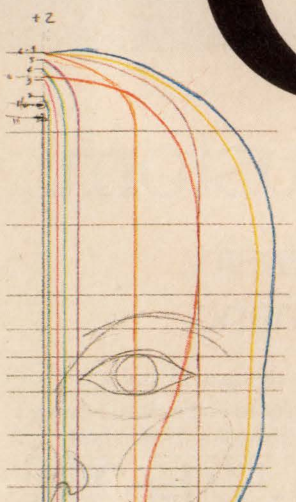
ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	0	9	45	46	0	0	11.0	8.8
Pot-Core	0	13	50	37	0	0	10.2	10.5
Laminate (power)	7	13	47	33	0	0	9.3	8.0
CONNECTORS								
Military panel	0	25	25	25	12	13	13.7	8.8
Flat/Cable	21	47	16	16	0	0	5.1	5.9
Multipin circular	0	27	33	13	13	14	13.1	9.6
PC	0	64	18	18	0	0	6.2	5.7
RF/Coaxial	21	29	36	7	7	0	6.6	5.4
Socket	20	40	27	13	0	0	5.4	4.4
Terminal blocks	12	41	35	12	0	0	5.9	5.6
Edge card	13	33	40	14	0	0	6.3	7.0
Subminiature	20	30	40	10	0	0	5.7	6.4
Rack & panel	0	29	57	14	0	0	7.6	6.2
Power	15	31	39	8	0	7	7.6	7.4
PRINTED CIRCUIT BOARDS								
Single-sided	0	55	40	5	0	0	5.6	4.8
Double-sided	0	38	58	4	0	0	6.4	6.5
Multilayer	0	23	62	15	0	0	8.0	8.9
Prototype	0	79	11	10	0	0	4.8	4.4
RESISTORS								
Carbon film	50	29	21	0	0	0	2.5	4.2
Carbon composition	43	29	10	19	0	0	4.9	3.9
Metal film	44	16	36	4	0	0	4.0	4.5
Metal oxide	30	39	31	0	0	0	3.6	4.3
Wirewound	16	28	56	0	0	0	5.3	2.4
Potentiometers	17	33	38	12	0	0	5.9	5.9
Networks	7	47	33	13	0	0	6.1	6.1
FUSES	29	29	35	7	0	0	4.8	2.4
SWITCHES								
Pushbutton	6	19	63	12	0	0	7.5	4.7
Rotary	5	18	65	12	0	0	7.5	5.7
Rocker	20	13	47	20	0	0	7.2	4.6
Thumbwheel	0	22	45	22	11	0	10.5	5.4
Snap action	20	20	30	20	10	0	8.7	3.5
Momentary	10	20	50	10	10	0	8.7	4.4
Dual in-line	17	33	17	17	16	0	9.2	4.2
WIRE AND CABLE								
Coaxial	43	28	29	0	0	0	3.1	1.8
Flat ribbon	47	20	33	0	0	0	3.3	1.7
Multiconductor	42	17	42	0	0	0	3.8	2.9
Hookup	61	30	9	0	0	0	1.6	1.5
Wire wrap	58	25	17	0	0	0	2.1	1.0
Power cords	36	23	36	5	0	0	4.3	4.3
Other	33	33	17	17	0	0	4.9	5.8
POWER SUPPLIES								
Switching	0	18	46	36	0	0	9.8	6.5
Linear	20	20	50	10	0	0	6.2	4.8
CIRCUIT BREAKERS	20	20	33	27	0	0	7.4	5.7
HEAT SINKS	27	20	47	6	0	0	5.4	3.9

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
RELAYS								
General purpose	28	22	39	11	0	0	5.5	5.2
PC board	0	25	58	17	0	0	8.0	8.1
Dry reed	25	25	37	13	0	0	5.7	6.9
Mercury	0	22	67	11	0	0	7.7	7.6
Solid state	21	36	29	14	0	0	5.6	8.9
DISCRETE SEMICONDUCTORS								
Diode	38	23	31	8	0	0	4.3	4.8
Zener	25	25	30	20	0	0	6.3	5.7
Thyristor	23	39	23	15	0	0	5.4	6.5
Small signal transistor	19	31	31	13	6	0	7.0	5.3
FET, MOS	24	23	18	35	0	0	7.6	7.6
Power, bipolar	25	8	33	34	0	0	8.1	4.8
INTEGRATED CIRCUITS, DIGITAL								
CMOS	10	26	32	32	0	0	8.2	6.4
TTL	31	19	38	12	0	0	5.5	6.5
LS	8	42	42	8	0	0	5.9	5.7
INTEGRATED CIRCUITS, LINEAR								
Communication/circuit	0	14	57	29	0	0	9.4	6.3
OP amplifier	10	20	40	30	0	0	8.5	6.5
Voltage regulator	11	33	39	17	0	0	6.7	6.6
MEMORY CIRCUITS								
RAM 16	37	18	27	18	0	0	5.5	4.0
RAM 64	20	40	30	10	0	0	5.2	4.2
RAM 256	20	20	40	20	0	0	6.9	5.0
ROM/PROM	22	22	45	11	0	0	5.9	5.3
EPROM	14	29	36	21	0	0	7.0	6.9
EEPROM	22	11	45	22	0	0	7.3	8.2
DISPLAYS								
Panel meters	11	45	33	11	0	0	5.7	6.4
Fluorescent	20	20	20	40	0	0	8.4	10.1
Incandescent	0	50	25	25	0	0	7.4	4.3
LED	17	33	33	17	0	0	6.3	5.6
Liquid crystal	0	31	46	23	0	0	8.2	7.2
MICROPROCESSOR ICs								
8-bit	27	9	37	27	0	0	7.4	4.2
16-bit	20	10	50	20	0	0	7.4	2.9
FUNCTION PACKAGES								
Amplifier	25	0	50	12	13	0	9.1	4.9
Converter, analog to digital	0	30	50	20	0	0	8.0	8.6
Converter, digital to analog	0	22	56	22	0	0	8.6	8.5
LINE FILTERS	11	33	34	22	0	0	7.1	6.4
CAPACITORS								
Ceramic	13	39	35	9	4	0	6.4	5.2
Ceramic monolithic	19	19	37	19	6	0	8.1	5.5
Ceramic disc	14	33	29	19	5	0	7.5	5.5
Film	10	30	35	20	5	0	8.1	5.9
Electrolytic	21	25	33	21	0	0	6.6	6.6
Tantalum	13	22	52	13	0	0	6.8	6.6
INDUCTORS	0	18	64	18	0	0	8.5	5.5

Source: *Electronics Purchasing* magazine's survey of buyers


MOTOROLA
68HC05
LATCH
RAM
GLUE LOGIC
OSC
ROM
CRTC

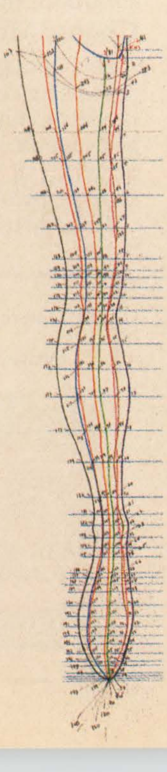
Graphics engines



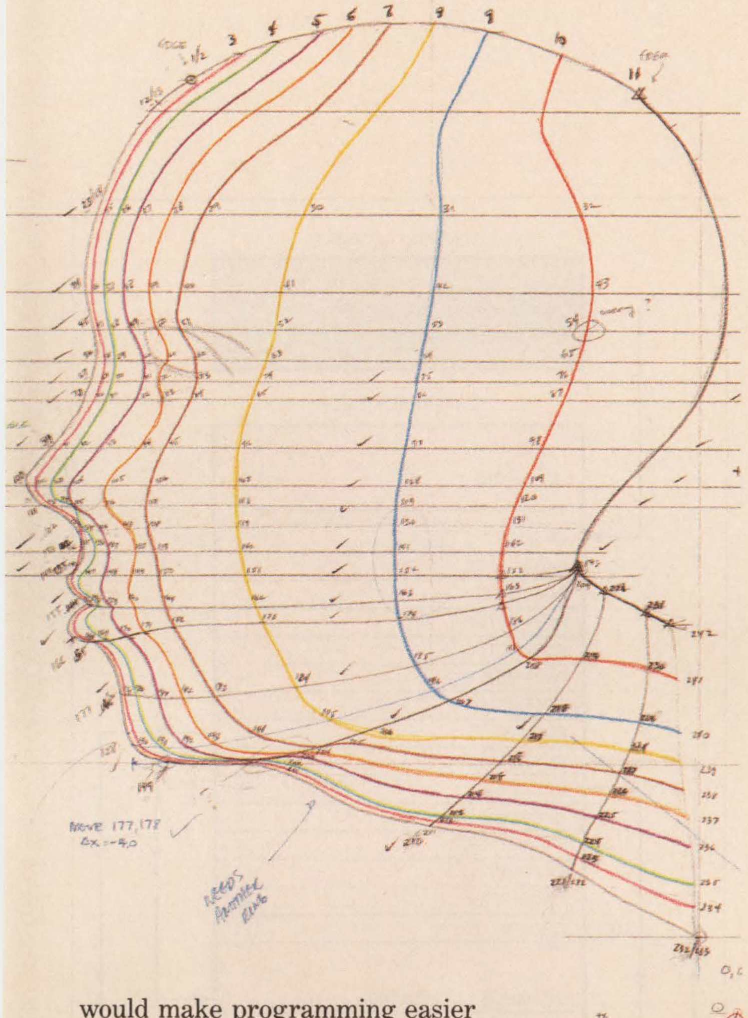
By offloading pixel-manipulation chores from a host CPU, graphics engines can provide higher resolution, more colors, and faster response in your graphics applications. Graphics engines also handle display-memory access and generate CRT control signals.

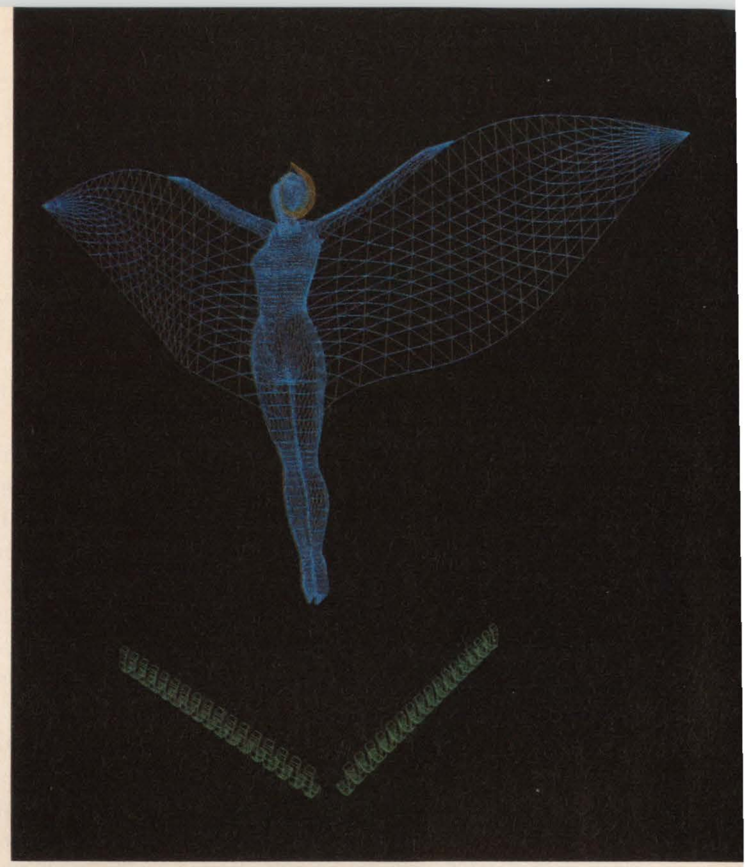
Margery Conner, *Regional Editor*

A graphics engine can free your host CPU, whether it's an 8088 or a VAX 11/70, from such time-intensive graphics-manipulation tasks as object rendering and window management, allowing your application programs to run much faster. Because graphics applications come in such a wide variety—stand-alone workstations, add-in PC graphics boards, instrumentation, and laser printers, for example—no one graphics chip can be optimized for all applications. To find the chip that's right for your application, you need to examine the tradeoffs between two basic factors: the chips' speed and their flexibility.



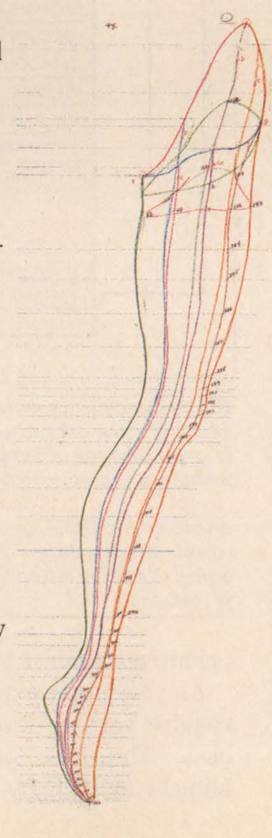
Graphics engines differ from the earlier graphics controllers in that the controllers' only functions were to generate CRT control signals and manage CPU and CRT access to the display memory. The CPU performed all graphic-data manipulation and placed the data in the display memory. Nonintelligent graphics controllers such as the Hitachi 6845 provided only a low-level link to the host processor. For example, in an IBM PC equipped with a Color Graphics Adapter (CGA) card (which contains a Hitachi 6845), the CPU would alter the display by manipulating the CGA card's 6845 register contents. The CPU could also communicate with the display through the BIOS, which





To produce this issue's cover, *artist David Hamby digitized his free-hand sketches of the cover figure's component parts. Then, the Superset Model PGM-2 graphics-processor system, running the artist's proprietary software, performed a B-splined interpolation on the 2400 digitized points to generate the 26,000 nodes necessary to represent the figure in three dimensions. The wire-frame figure results from the high-resolution vector output of the Superset geometry file.*

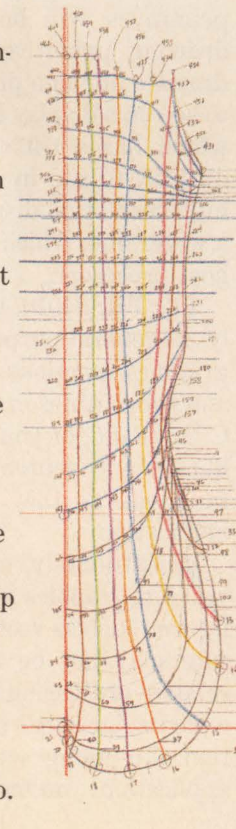
would make programming easier and more transportable but would make the display's response perceptibly slower. Graphics engines remove at least some of the graphics-manipulation chores from the host while still handling display-memory access and generating CRT control signals.



Speed vs flexibility

The speed and flexibility of a graphics engine are determined basically by its degree of programmability. In general, a graphics engine that's highly programmable is flexible—that is, it lets you easily draw any image you wish. A graphics engine that's not programmable can draw any of its standard shapes rapidly, but it's much slower at drawing nonstandard shapes.

A highly programmable graphics engine, such as Texas Instruments' TMS34010 or National Semiconductor's Advanced Graphics Chip Set (AGCS), has a minimal instruction set of hardwired graphics primitives. A nonprogrammable graphics engine, such as AMD's QPDM, Hitachi's ACRTC, Intel's 82786, or NCR's 7300CGC/7301MIC has a large set of hardwired primitives.



Graphics primitives are basic commands that specify the lines, shapes, and characters that make up a picture. These primitive commands are either hardwired into the processor or built into software from assembly-language instructions. The line-drawing primitive for a programmable chip is far more complex than that for a hardwired chip: A software primitive for drawing a standard circle, for instance, would comprise 101 lines of code; the hardwired primitive would have two.

Graphics primitives specify the lines, shapes, and characters in a picture; they can be hardwired into the processor or built into software.

Other common primitives let you draw dots, polygons, and 1-pixel lines.

In general, primitives implemented in hardware run faster than do their software equivalents. However, because primitives have set capabilities, obtaining any function besides the standard ones requires intervention from the host processor. The $21.60 (1000) Hitachi ACRTC graphics engine can rotate a drawing in units of 90° via the Graphics Copy command, or in units of 45° via the Pattern command, but rotating by just one degree requires assistance from the host processor.

Similarly, if you need to draw a picture that you can't define with such primitives as circles, lines, and boxes, the host processor must either draw the figure using the Dot command or else draw it in system memory and then transfer the drawing to the frame-buffer memory. As a rule, when it's executing a standard primitive, a hardwired chip performs the function faster than a programmable chip does, but when the hardwired chip requires intervention from the host CPU, the programmable chip is faster.

Further, keep in mind that the hardwired chips' speed advantage will eventually disappear as graphics technology becomes more sophisticated. As higher-resolution displays become available, the hardwired primitives will be less useful. The hardwired line-drawing primitive of the Intel 82786, for example, draws a line one pixel wide. A 1-pixel-wide line is easy to see on a display like the one provided by IBM's CGA, which has a 640×200-pixel resolution, but it's more difficult to see in a 1024×1024-pixel display. On such high-resolution displays, therefore, you'd want to draw a wider line, which would require intervention from the host processor.

TI's TMS34010, which sells for $50 (25,000), is actually a general-purpose processor that's optimized for graphics functions. You can write your own primitives and subroutines in the graphics processor's assembly or C language, or you can purchase a graphics subroutine library and source code for $10,000. You can use the functions as they are or modify them to suit your application.

Unfortunately, no widely accepted benchmarks exist yet for graphics engines. In any case, broad speed figures such as vectors per second or character-transfer rate may not be an accurate measure of the chips' relative processing power. What's important is how well a particular chip's drawing capabilities fit your application. To judge whether a chip is suitable for your application, you must weigh your need for nonstandard primitives against your need for fast execution.

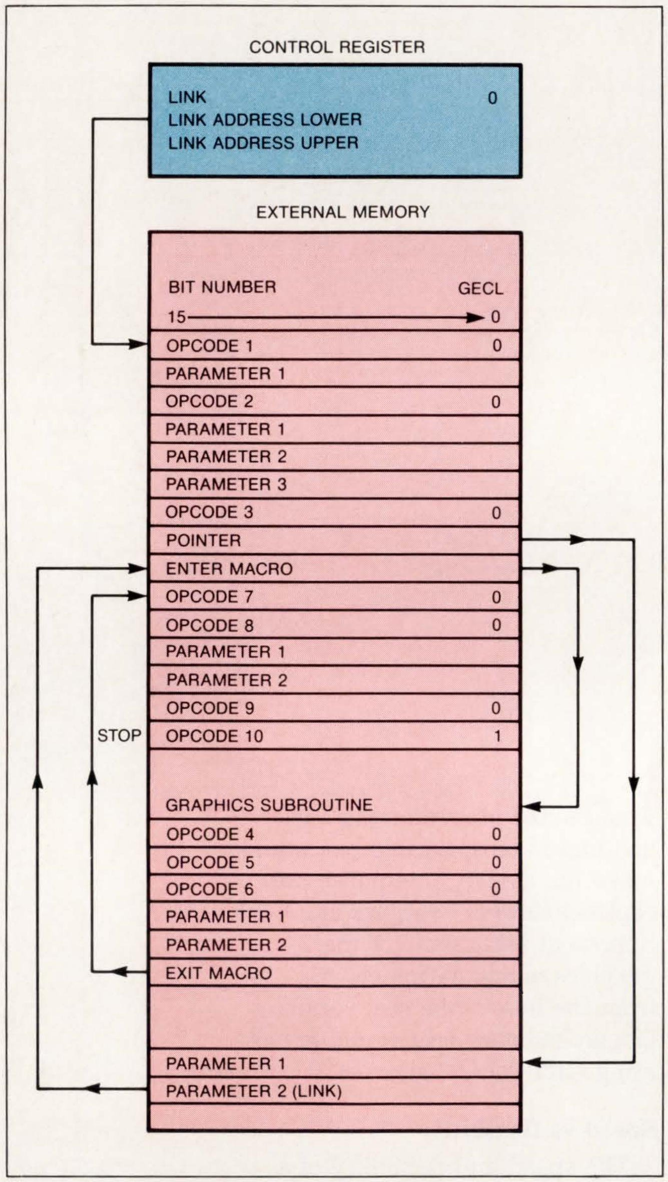


Fig 1—A sequence of instructions resides in memory *in the Intel 82786; it runs only when the application program needs to change bit-map contents or support a special function, such as when you're making menu selections with a mouse. The 82786 tests the GECL (Graphics End of Command List) bit and switches to Poll mode whenever the GECL is 1. Poll mode halts the 82786 until a Link command and address are loaded into the control register. The 82786 begins executing a new linked list of instructions when the GECL bit is reset to 0.*

As you might expect, the different graphics engines require varying levels of processing support from the host. The host processor communicates with the Hitachi ACRTC by loading calls to primitives into the

GRAPHICS ENGINES

MANUFACTURER	CHIP	DISPLAY-MEMORY ARCHITECTURE	MAXIMUM SIZE OF DISPLAY MEMORY	BITS PER PIXEL	HARDWARE WINDOWS*	CHIP PACKAGE	PRICE	PROGRAM-MABILITY
AMD	Am95C60 (QPDM)	PLANAR	4096×4096×4 BITS PER QPDM	4 BITS PER QPDM TO 256 BITS MAX	1 WINDOW WHEN USED WITH THE 8171 CHIP	144-PIN PGA (CMOS)	$250 (100)	HARDWIRED
HITACHI	HD63484 (ACRTC)	PACKED-PIXEL	2M BYTES	1, 2, 4, 8, OR 16	1 WINDOW, 3 HORIZONTALLY SPLIT SCREENS	68-PIN PLCC OR 64-PIN DIP (CMOS)	$21.60 (1000)	HARDWIRED
INTEL	82786	PACKED-PIXEL	4M BYTES	1, 2, 4, OR 8	16 HORIZONTAL, UNLIMITED VERTICALLY	88-PIN PGA OR LCC (CHMOS)	$80 (10,000)	HARDWIRED
NATIONAL SEMICONDUCTOR	AGCS (2 CHIPS: RGP** AND BPU)	PLANAR	16,384×16,384× UNLIMITED PIXEL DEPTH	UNLIMITED	NONE	RGP, 68-PIN PLCC; BPU, 44-PIN PLCC	$140 (100)	PROGRAM-MABLE
NCR	7300CGC AND 7301MIC	PLANAR	1M BYTE	2 BITS PER MIC TO 8 BITS MAX	NONE	7300CGC, 68-PIN PLCC; 7301MIC, 28-PIN PLCC OR DIP	7300CGC, $48 (1000) 7301MIC, $6 (1000)	HARDWIRED
TEXAS INSTRUMENTS	TMS34010	PACKED-PIXEL	128M BYTES	1, 2, 4, 8, OR 16	NONE	68-PIN PLCC	$50 (25,000)	PROGRAM-MABLE

*ALL THE ENGINES SUPPORT SOFTWARE WINDOWS
**RGP WILL BE INTRODUCED IN THE 2ND QTR OF 1987

ACRTC's FIFO instruction port. The other engines can communicate with the host through a display list, allowing the CPU and the graphics engine to be fairly independent of each other.

The $80 (10,000) Intel 82786, for example, fetches graphics calls to primitives from a linked list in memory that the host processor creates and updates. The host loads the list's initial address into a dedicated register in the 82786; each instruction contains the address of the subsequent instruction. The first bit in each instruction, if set, indicates to the 82786 that it should stop and wait for new instructions **(Fig 1).** The host processor can update the display list in the graphics memory through the 82786's dynamic-RAM controller.

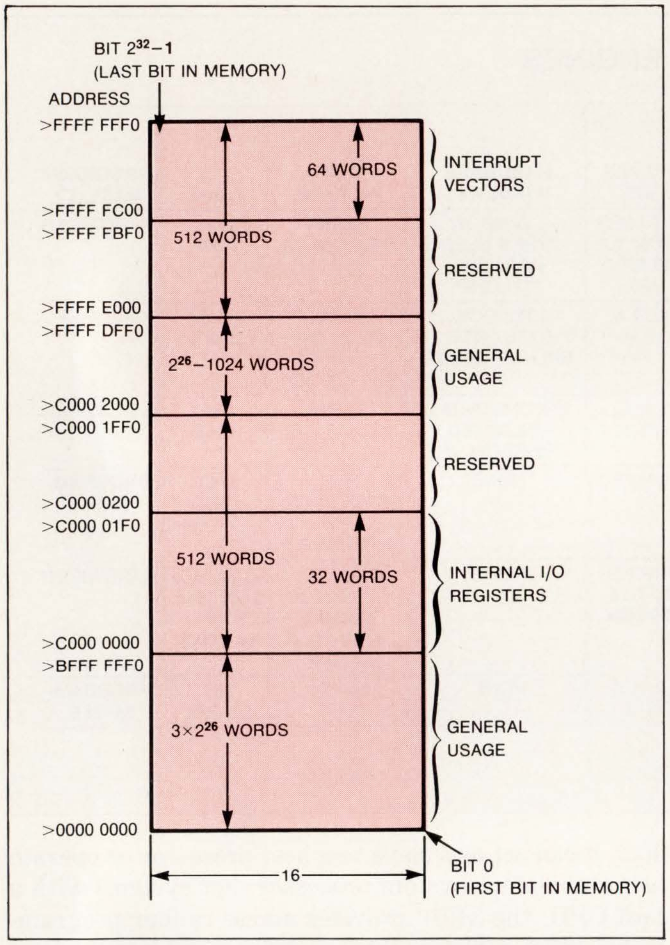
In a low-end system, the host and the 82786 can share a single memory, which the dynamic RAM controller section of the 82786 manages. For higher performance, the system can have both graphics memory and system memory: The host can store character fonts or graphics objects in system memory, which the 82786 can access by using a virtual-mode 80286 or 80386 configuration.

Because the 34010 is based on a stand-alone general-purpose microprocessor core (see EDN's Thirteenth Annual μP/μC Chip Directory, November 27, 1986, pg 102), it can act as a slave to a host processor or operate as a stand-alone system processor. For systems with a host CPU, the 34010 provides access to four programmable 16-bit registers that can be mapped into the host processor's memory or I/O address space, allowing command, status, and data transfer between the 34010 and the host processor. The host doesn't have direct access to the 34010's graphics memory; indirectly, it can perform block moves to the memory through an autoincrementing address register and data port. To eliminate contention with the 34010 for the graphics memory, the host can suspend the 34010's program execution, although the 34010 continues dynamic-RAM- and screen-refresh cycles.

Display-memory architectures

Another basic difference in the architectures of graphics engines lies in the way pixels are stored and accessed in display memory. In a 2-dimensional display memory, each pixel consists of one bit, which can be either on or off, indicating the presence or absence of a dot. Such a display memory supports a monochrome, single-intensity display. In a color display, additional bits at each pixel add color and control the intensity. A

Primitives implemented in hardware generally run faster than do their software equivalents; however, they let you draw only a standard set of lines and shapes.



Data and instructions reside in the same memory space *in the TMS34010 memory architecture, so the chip can theoretically support a maximum display size of 65,536×65,536 pixels.*

4-bit pixel, for instance, can control the CRT's red, green, and blue color guns as well as the pixel's intensity. Each bit within the pixel corresponds to a plane.

Planes can provide information other than color. For example, one plane can show a static picture while another displays an icon that the user can drag around the screen with a mouse. To make objects appear to move, you display their changing position on separate planes. Alternatively, you can use a 1-bit plane to mask certain regions of another plane.

Planar vs packed-pixel display memory

Graphics engines have two basic display-memory architectures: the planar architecture (used by AMD, National Semiconductor, and NCR), and the packed-pixel architecture (used by Hitachi, Intel, and Texas Instruments). A chip's display-memory architecture, like its degree of programmability, affects its speed. In general, the packed-pixel architecture is faster for applications that require the ability to access individual pixels; the planar architecture is faster for applications that require access to large sections of data related to one plane.

In a planar architecture, display memory is divided so that all the bits associated with one plane are stored in the same area of memory (see **Fig 2a**). Each word, therefore, comprises bits associated with only one plane. The display-memory data is accessed a word at a time (a word is usually 16 to 32 bits), so to manipulate one bit within a pixel, the chip accesses at least 15 unnecessary bits.

The planar architecture-based AGCS from National Semiconductor comprises four chips: the raster graphics processor (RGP), the BitBlt processing unit (BPU), a video clock generator, and a video shift register. This modularized approach gives you flexibility in designing or expanding a high-resolution pixel system. In chips based on the packed-pixel architecture, the maximum number of bits per pixel is 16. However, it's common for image-processing applications to require as many as 24 bits.

Because it can support virtually an unlimited number of planes, the AGCS is optimized for use in high-end graphics workstations. Its high price—$140 (100) for one RGP and one BPU—and large chip area make the 4-chip set an unlikely candidate for use on a personal-computer graphics board. To use this chip set, you need one RGP, one video clock generator, and as many BPUs as you have planes (**Fig 3**).

One disadvantage of planar architecture is that it causes difficulty in manipulating individual pixels. Drawing a line, for instance, is a function that planar architecture is not especially suited for. However, the National chip set provides a line-drawing mode that circumvents the problem. In this mode, the BPU can select the individual bits corresponding to a pixel by masking all the other bits. A hardwired algorithm generates the addresses of the line's pixels. The chip operates more slowly in this mode, because each BPU accesses only one bit of a pixel, instead of a 16-bit plane word as it does in its normal mode.

The AMD QPDM also has a planar architecture; like the National chip set, the QPDM lets you add planes (to a maximum of 256) by adding more of the chips; however, unlike National's BPU chip, which supports one plane, each QPDM supports four planes instead of

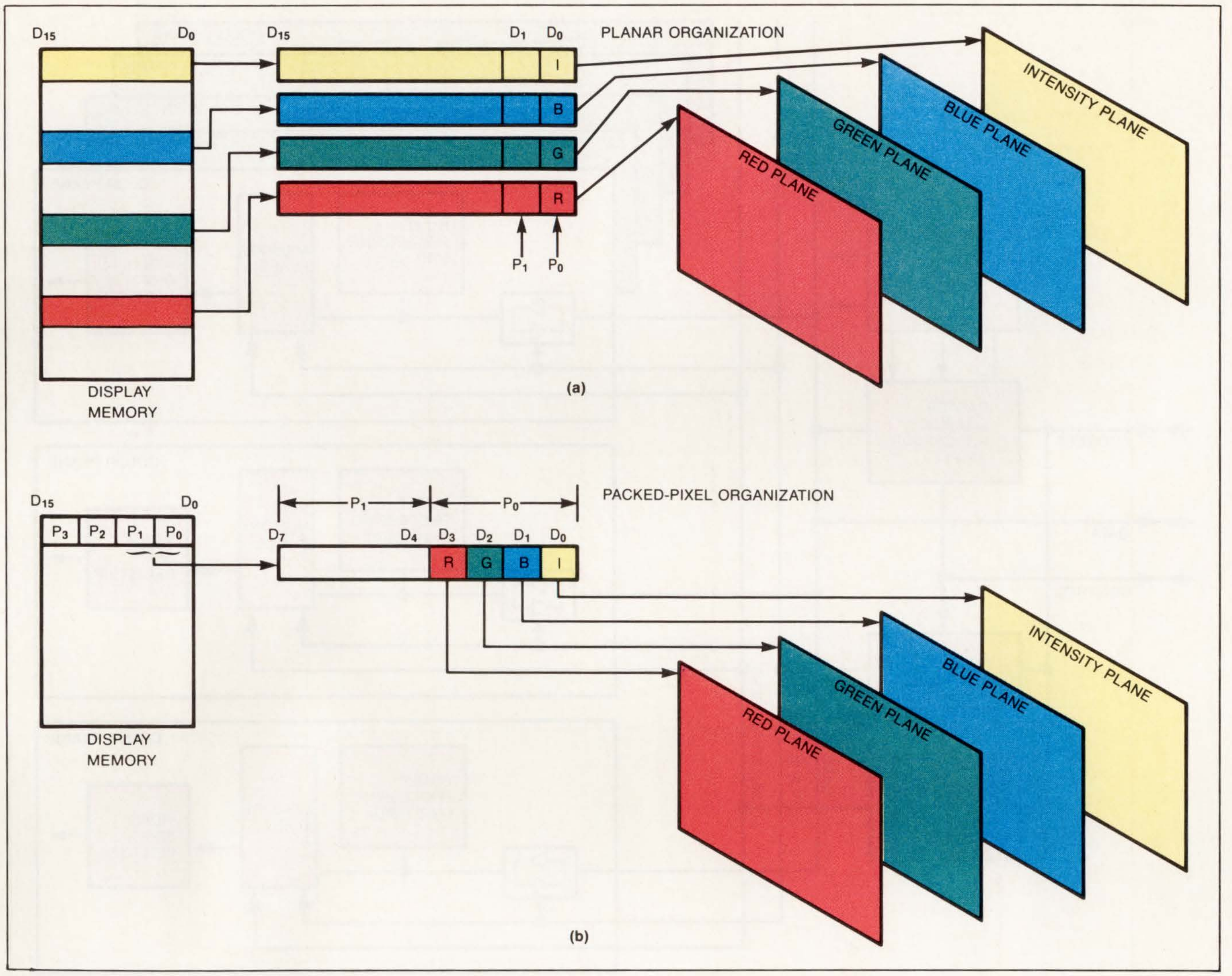


***Fig 2—A graphics engine with a packed-pixel** memory organization **(a)** accesses complete pixels. This architecture optimizes the memory for pixel manipulations such as antialiased line drawing. A graphics engine with a planar organization **(b)** divides display memory so that all the bits associated with one plane are stored in the same area of memory. This architecture is optimum for manipulating planar information, such as performing a masking operation.*

one. The QPDM costs $250 (100).

In a packed-pixel architecture, memory storage is organized so that all the bits in a pixel are contained in the same memory word **(Fig 2b)**. When pixel depth is shorter than word length, multiple pixels can be packed into each word. When the graphics engine accesses a word of display memory, all of a pixel's bits are available simultaneously.

One of the major functions of a graphics chip is to provide software windows; they do so by means of a powerful primitive: the bit-block transfer, or BitBlt (pronounced "bit-blit"). The BitBlt performs a Boolean operation on a source and destination array in one plane of display memory. The graphics engines all implement the BitBlt in hardware. The Intel, AMD, TI, and National chips perform the full set of 16 logical operations; the Hitachi chip performs a subset of the 16 operations.

The TI TMS34010 supports both BitBlts and pixel block transfers, or PixBlts. PixBlts operate on multiple-bit pixels; in color systems, they have a speed advantage over BitBlts because they perform the operation on all planes at once. They can perform logical and arithmetic operation, transparency detection, plane

To judge whether a chip is suitable for your application, you must weigh your need for nonstandard primitives against your need for fast execution.

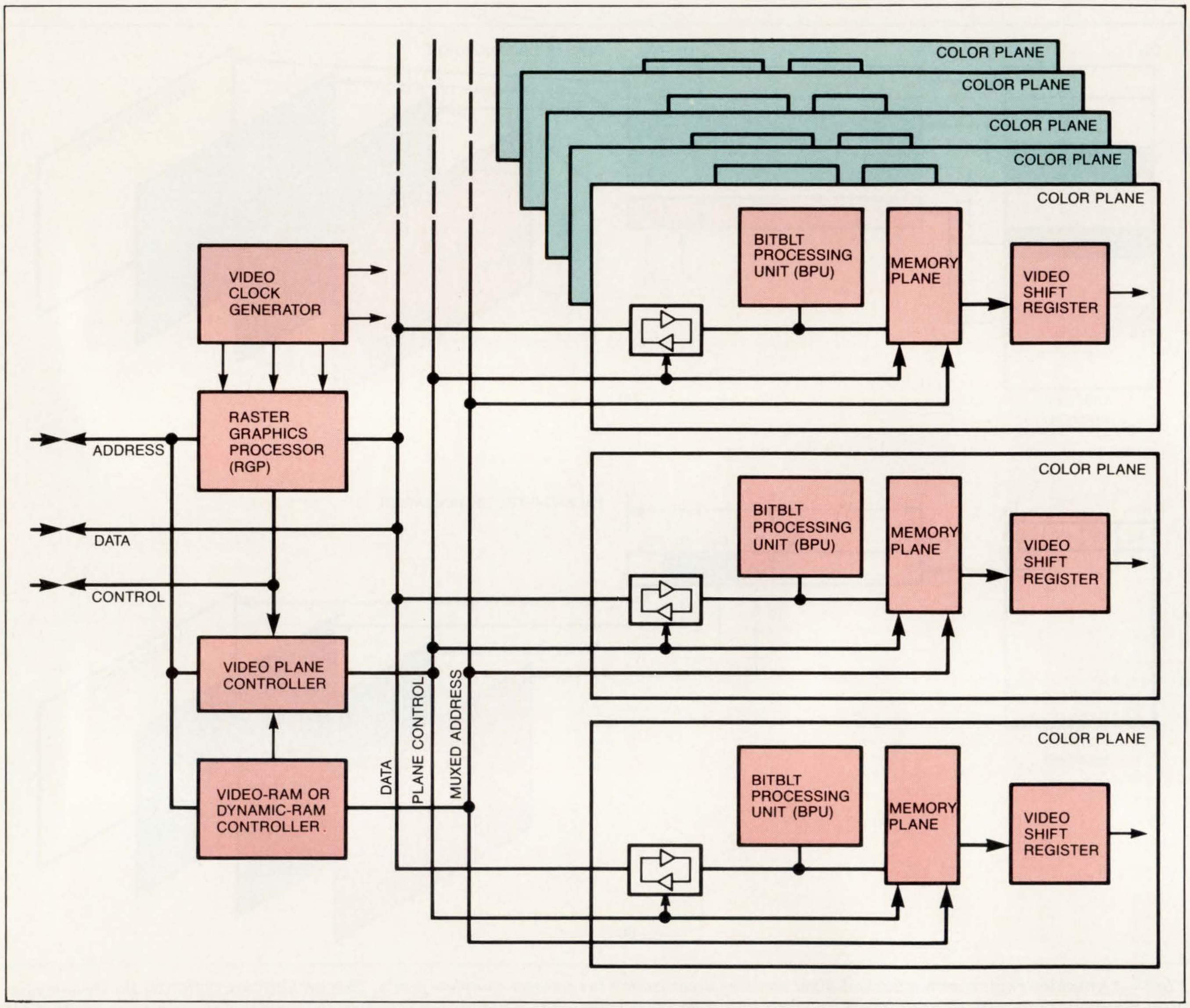


***Fig 3—To allow an almost infinite number** of color planes, the AGCS from National Semiconductor uses a building-block approach. A system needs only one raster graphics processor (to be introduced in the second quarter of 1987); you add one BPU per memory plane.*

masking, and color expansion. Because PixBlts perform arithmetic operations that require the processor to have the ability to handle carries between bits, only a chip with a packed-pixel architecture can perform PixBlts. PixBlts are useful for performing the Bresenham antialiasing algorithm for line-drawing primitives.

BitBlts are useful for creating software windows. For example, you can use the Replace BitBlt command to create a window of text on the screen by specifying the text array as the source array and the windowed area as the destination array. Note that the rectangle of text, although it's in the display memory, is not normally visible on the screen. Because the display memory can be much larger than the actual viewing area, renderings can be stored in areas of the memory outside the viewing area and bit-block-transferred to the screen for rapid display. You don't need to regenerate a drawing each time you need it.

The TMS34010 lets you specify the window's location by loading a register with the XY coordinates of the pixels in two of the window's corners (two corners diagonally across from each other). By specifying the window location in registers, instead of in the primitive, you can keep the basic software extremely flexible;

Broad speed figures such as vectors per second or character-transfer rate may not accurately represent a graphics engine's processing power.

changing the window locations is a matter of changing the register contents once, rather than changing each occurrence of the location in the primitive.

Clipping, including postclipping and preclipping, is a graphics function that permits windowing: It prunes the BitBlt array to fit inside a display window. When a graphics engine performs postclipping, it calculates the positions of all the pixels in a drawing and then discards those pixels that fall outside the window, or "clipping rectangle" **(Fig 4a).** Postclipping generates an accurate line, but the engine wastes time calculating pixels that it never displays.

When a graphics engine performs preclipping, it determines only the portion of the drawing that will fit inside the window; it avoids calculating any part of the picture that falls outside the window **(Fig 4b),** thus saving processing time. When the engine uses an antialiasing algorithm, however, preclipping can produce a less-accurate line (a greater staircase effect) than does postclipping, because the endpoints of a preclipped line lie on the boundary of the window. In other words, a graphics engine calculates an antialiased preclipped line without taking the history of the ideal line into account. Conversely, a chip that uses an antialiasing algorithm to perform postclipping displays the smoothest possible line in the window, because it calculates the position of all the pixels in the ideal line.

The programmable TMS34010, which uses antialiasing algorithms, can perform both postclipping and preclipping. To obtain a smooth preclipped line, you can program the chip to include error-term initialization in its antialiasing algorithm **(Fig 4c).** "Error term" refers to the distance between the calculated pixel and the ideal line. The result is a preclipped line that's as smooth as a postclipped one **(Fig 4d).**

AMD's QPDM, a hardwired chip, can also draw antialiased lines. In color systems, however, the chip works best when you dedicate one QPDM to each color plane, the manufacturer claims.

The clipping rectangle provided by a graphics engine can also support the use of a mouse for making menu selections. In pick mode, when the user points to an icon (which is surrounded by the invisible clipping rectangle) and clicks the mouse, the graphics engine locates the graphics commands that drew the icon's bit map. These commands act as a pointer to the function that the icon represents.

The Intel 82786 offers window control in hardware as well as in software. When it performs hardware windowing, the chip constructs the display image from

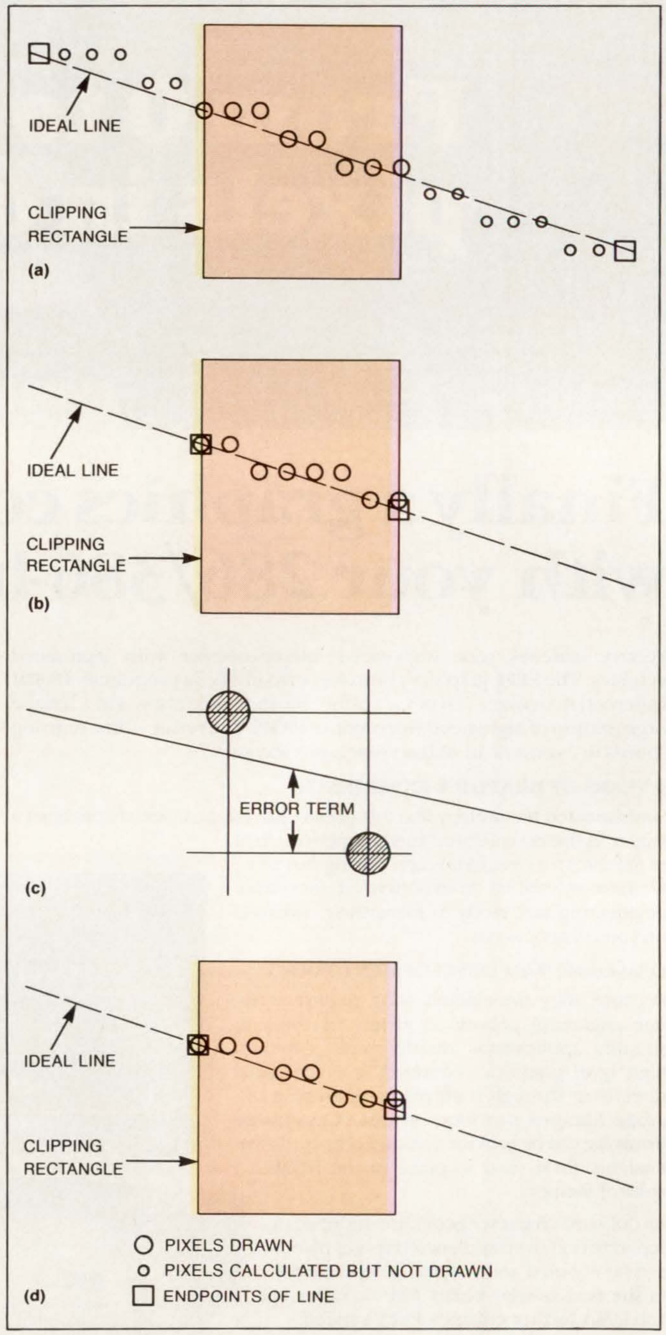


Fig 4—When a graphics engine performs postclipping, *it calculates all the pixels in a line and discards pixels that fall outside the "clipping rectangle," or display window* ***(a).*** *When a chip uses an antialiasing algorithm to perform preclipping, it calculates only pixels that lie inside the clipping rectangle, without taking into account the history of the ideal line* ***(b).*** *To minimize the staircase effect in such a preclipped line, the programmable TMS34010 can include initialization of the error term in the line-drawing algorithm* ***(c).*** *The result is a preclipped line that exactly matches the postclipped line* ***(d).***

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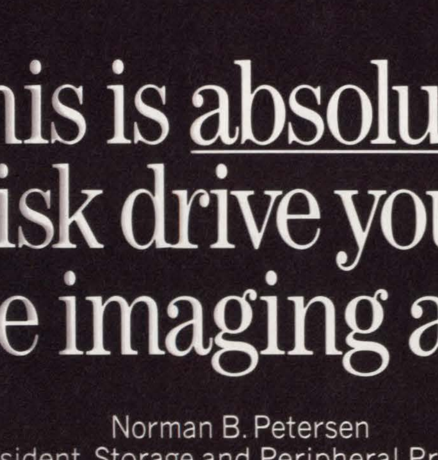

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Implementing windows in hardware is very fast but requires support from your application software.

independent bit maps for each video frame; a pointer keeps track of the section of the bit map being displayed in the window. Software windowing uses BitBlts to copy text or drawings from source arrays into the visible portion of the display memory. The display memory contains the picture in the final form and order in which it will appear on the screen.

The advantage of hardware windowing is speed—it's fast enough, for example, to let you rearrange the screen on every video-frame retrace. Further, once you create the images for a window, you don't need to perform a BitBlt to display memory in order to call the image up on the screen. Instead, you use a pointer to locate the image you want to display; to display a different image, you simply change the contents of the pointer.

When used with dynamic RAMs, the Intel 82786 is limited to 2M bytes of display memory (for example, a 640×480×8- or 1024×1024×2-pixel display). When used with video RAM, its display memory can be as large as 8M bytes (1024×1024×8 pixels). Note, however, that when its display memory is video RAM, the 82786 can't perform hardware windowing, because the chip performs that function by making use of the fast-access modes of dynamic RAM.

Hardware windowing has its drawbacks: For instance, it limits the number of windows you can display. The Intel chip can display a maximum of 16 windows horizontally, the Hitachi ACRTC can display four, and the AMD QPDM (when used with the 8171 video-data-assembly FIFO chip) can display one. To avoid exceeding the limit, you must keep track of the number of windows you have open at a time. What's more, little application software and no software-interface standards (such as MS-Windows) support hardware windowing; in fact, software-interface standards exist to relieve the dependence of application software on graphics hardware.

Some of the graphics-engine manufacturers boast that their chips can work with dynamic RAMs as well as video RAMs, thus saving you money. In the past year, however, the trade restrictions against imported dynamic RAMs have driven their prices up, so they're no longer much less expensive than video RAMs. The 20% premium that you may still have to pay for a video RAM is offset by the ease of interfacing the video RAMs to your graphics hardware; the video RAMs perform parallel-to-serial conversion internally. One possible compromise would be to use video RAMs for onscreen memory and dynamic RAMs for off-screen memory and bit maps.

Support circuitry

Finally, graphics engines require some amount of external circuitry to control the video and memory. Hitachi offers two companion chips for the ACRTC: the HDC63485 Graphics Memory Interface Controller ($10.50) and the HDC63486 Video Attribute Controller ($11.60). The chips implement all the hardware needed for a graphics subsytem (except for RAM and video D/A converters) in less space and at a lower price than any other manufacturer's chips do. With one 63486, the display is limited to a 640×480-pixel resolution and 16 colors; by adding four 63486 chips, you can increase the resolution to 1280×1024 pixels or increase the number of colors to 64k. The three chips are each available in 68-pin PLCCs and 64-pin shrink DIPs. **EDN**

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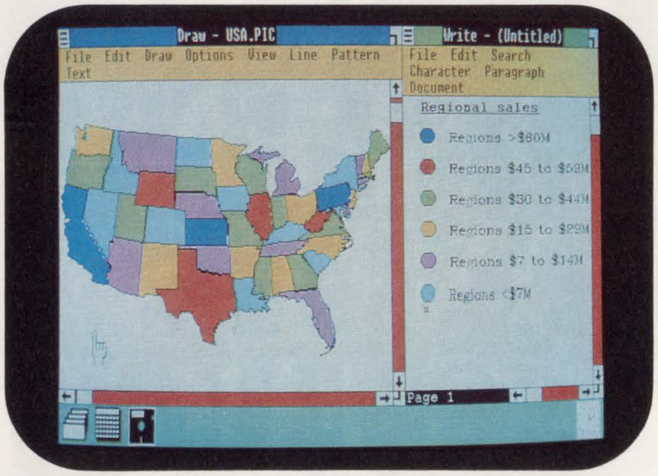

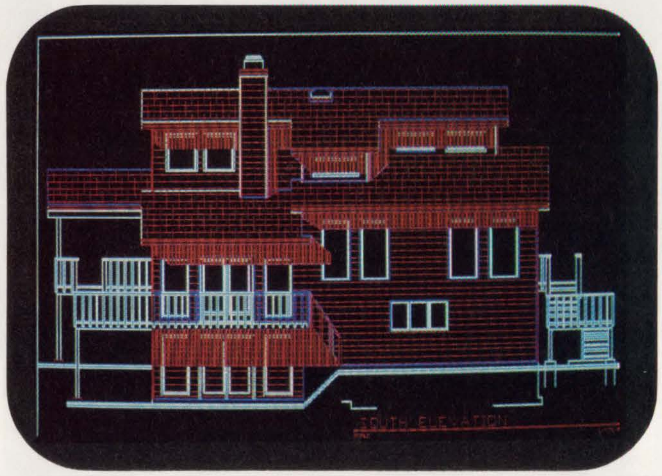

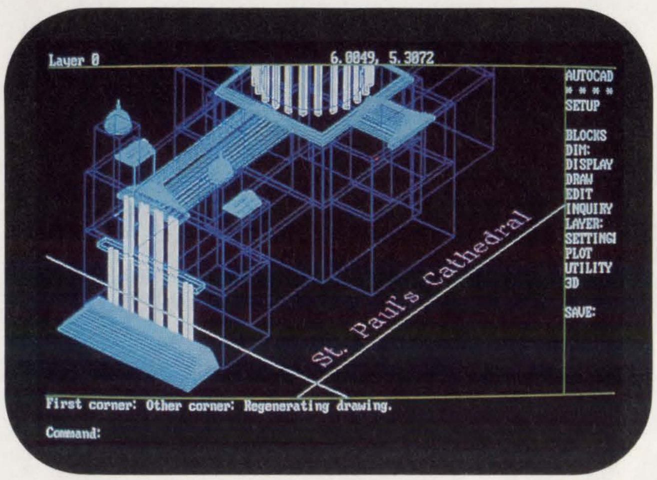

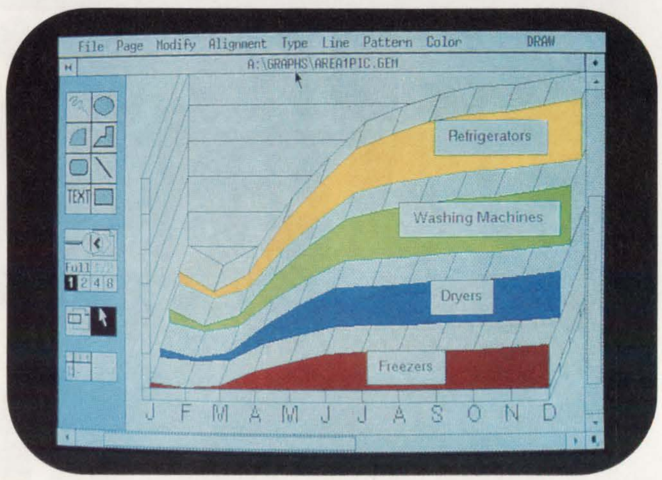

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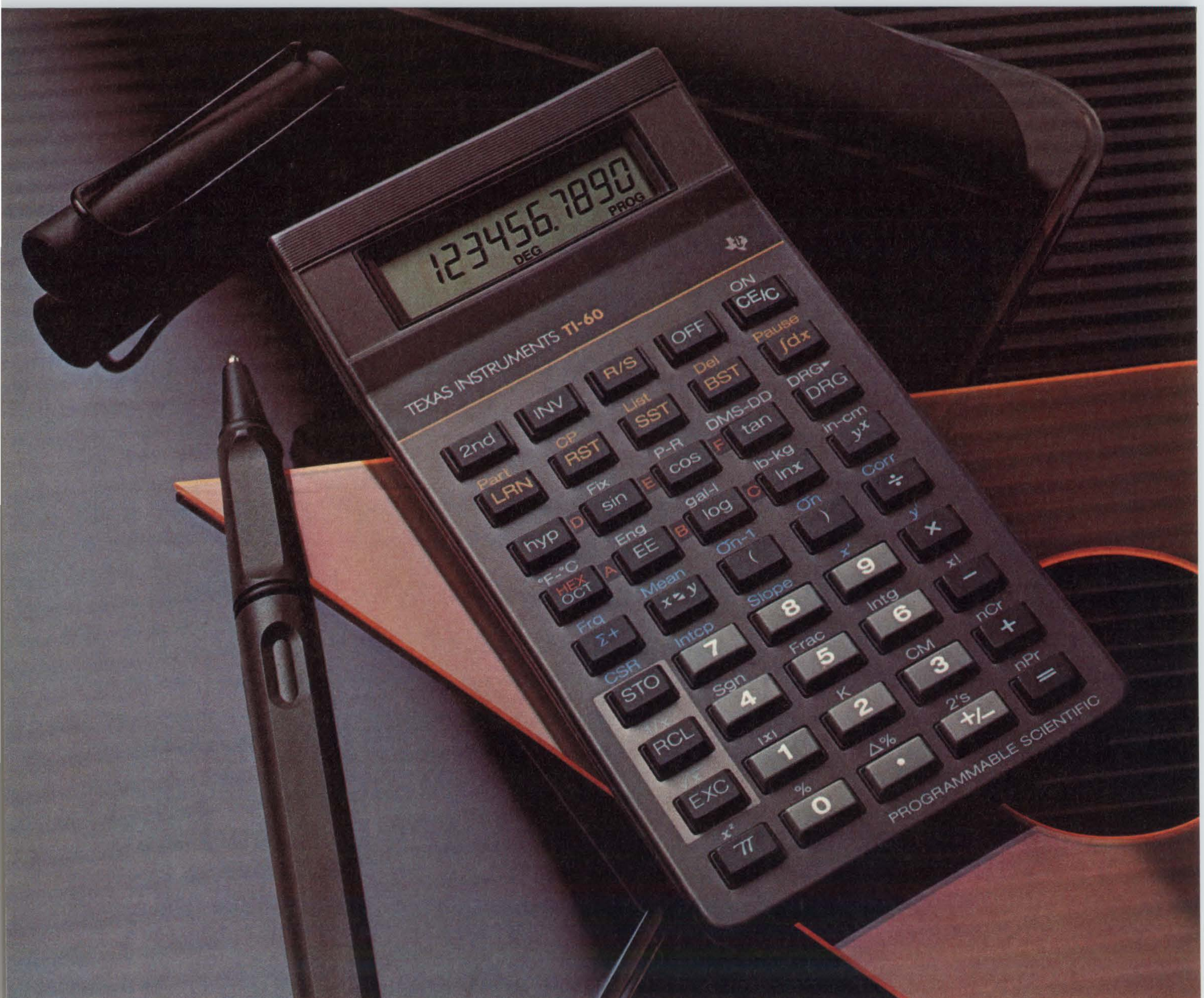

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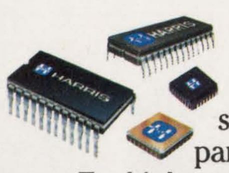

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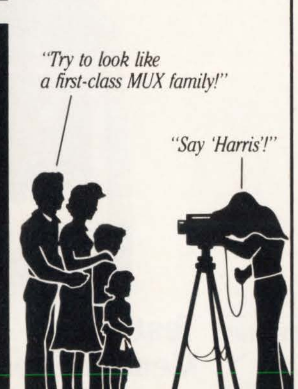

CMOS ADC achieves reliable 12-bit resolution

It's not easy to achieve maximum performance from a 12-bit ADC. Conversion results can be quite misleading if you fail to adjust the converter's endpoints prior to operation. Such adjustments usually require that you calculate the overall converter error budget by combining offset, gain, and linearity errors into a total error spec.

John Reidy and John Wynne, *Analog Devices*

An increasing number of applications require A/D converters with 12 bits of resolution or more. In the past, many designers found that it wasn't easy to work with such converters; achieving true 12-bit performance requires a good deal of bench time (and patience) to trim out offset and gain errors. Luckily, a recently introduced CMOS ADC satisfies a number of high-performance applications while keeping time-consuming design calculations to a minimum.

The AD7578 single-channel device guarantees a total unadjusted error spec of ±1 LSB over its operating range. It converts in 100 μsec and uses an autozeroing technique to reduce offset drifts to less than 100 μV. If your application requires more than one channel, you can use the AD7582, which is identical to the AD7578 except that it accepts four channels.

Converter-to-μP interface is novel

One application in which this converter saves on design time involves interfacing to a microprocessor. When you need to interface an A/D converter to a μP, you'll often find it difficult to ensure that the conversion process is complete before you try to perform a data-read operation. If the conversion hasn't finished by that time, then the converter will reset, or, at the very least, the conversion data will be affected.

To aid in ascertaining when to initiate a read operation, most modern converters have a conversion-in-progress or $\overline{\text{BUSY}}$ output flag, which you can use as an interrupt input for the μP. Using this approach, you command the A/D to start a conversion as the system software continues to run. When the conversion is complete, the $\overline{\text{BUSY}}$ flag forces the μP into a data-read interrupt routine to fetch the data.

Another way to ensure that valid data is available also exists. You simply insert a software delay in the program (longer than the A/D-conversion time) between the conversion-start instruction and the read instruction.

The interface scheme in **Fig 1a** contains elements of

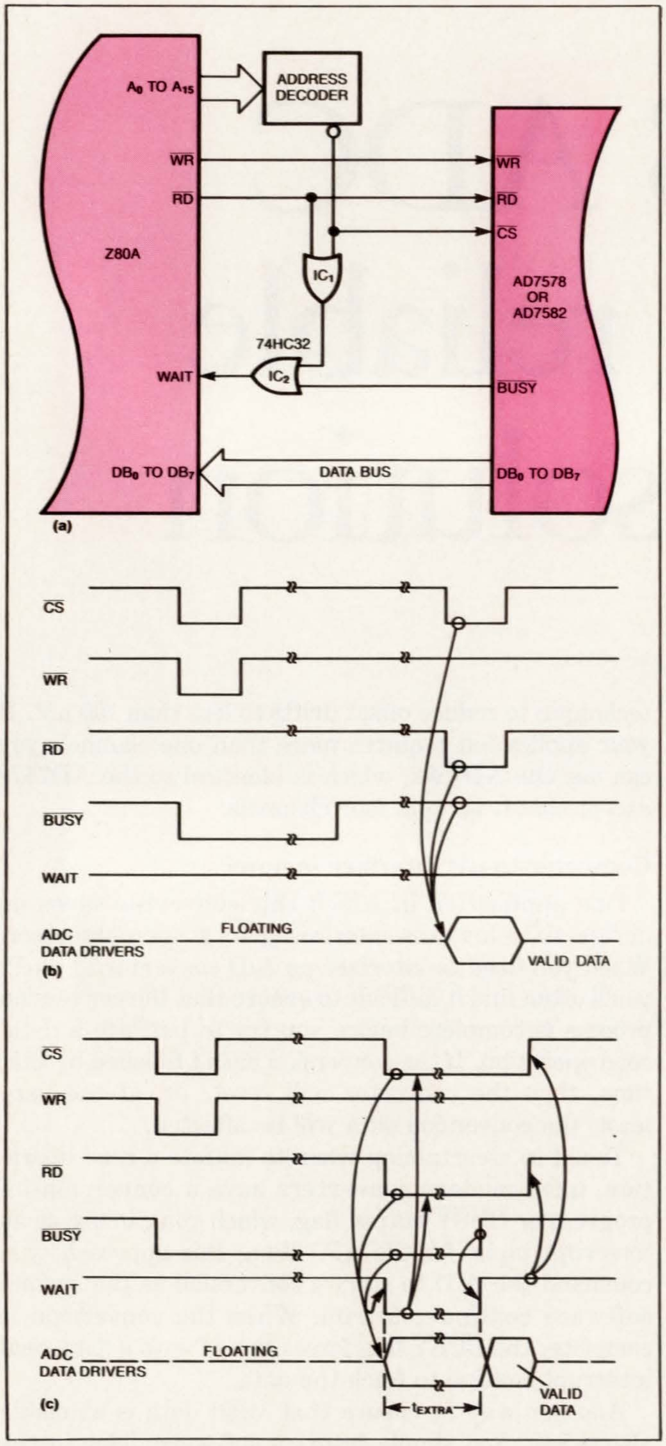

***Fig 1—For this μP-interface application,** you can use a valid read request to gate the converter's $\overline{BUSY}$ flag **(a)**. When the μP executes a read instruction, it has access to the data immediately **(b)** if $\overline{BUSY}$ is high. A low $\overline{BUSY}$ **(c)** puts the μP into a wait mode. When the conversion ends, the read cycle continues until completion.*

both techniques. Here, a valid (low) read request via IC_1 gates the $\overline{BUSY}$ flag (which is low during a conversion) at the input of OR gate IC_2. IC_2's output connects to the Ready or Wait input on the μP. When this input goes low, the μP goes into a wait mode and stays there until the Wait input goes high again. Because the start-conversion command uses a write instruction, IC_2's output remains high after a start-conversion command, and the μP continues to run.

If, at some later time, the μP needs to use the new conversion data for computations, it simply executes a read instruction to the converter to fetch this data. If $\overline{BUSY}$ is high, the conversion is complete and the data is available immediately **(Fig 1b)**. If $\overline{BUSY}$ is low, the conversion is still in progress. The Z80A's Wait input immediately goes low and places the μP in the wait mode, where it stays until the conversion is complete. When the conversion ends, the read cycle continues until it's complete **(Fig 1c)**. Processor wait time can vary from nonexistent (conversion finished when data-read request arrives) to approximately the full conversion time (conversion just started when data-read request arrives). To keep things simple, neither of these timing diagrams includes the BYSL input.

Although **Fig 1a** uses a Z80A, you can use this approach with any μP that allows you to extend its read cycle to 100 μsec max. Of course, you have to modify the circuit slightly to accommodate different processors. With the 8085A, for example, the $\overline{RD}$ signal may occur too late in the read cycle to affect the Ready input and thereby extend the read cycle. To avoid this problem, you should use the 8085A's SO status output as an advanced read signal and connect it to IC_1 in place of $\overline{RD}$.

Simple loop detector works well

Another application for this 12-bit A/D converter is the detection of 4- to 20-mA signals. A popular method involves terminating the loop with a 250Ω resistor and then monitoring the voltage drop across the resistor. Over the full-scale current range, this voltage will range from 1 to 5V.

To comply with this scheme, the monitoring circuitry must meet certain criteria. It must be able to accommodate the 4-mA offset without losing any resolution to the loop. The ability to adjust the zero and the full-scale range independently is also essential. The ability to detect an open-loop circuit condition is another useful capability: Long 4- to 20-mA loops can easily be cut in industrial applications.

Normally, you'd have to trim out offset and gain errors to achieve true 12-bit performance.

Fig 2 shows a circuit that meets these requirements. Rather than directly monitoring a voltage drop across a sense resistor, the circuit bleeds a fraction of the loop current (nominally 25%) into a current mirror based around IC_1. IC_2 then sums the mirrored current with a 1-mA fixed offset current. IC_2's output voltage ranges from 0 to 5V as the loop current changes from 4 to 20 mA. As a result, the dynamic range of the AD7582 matches the dynamic range of the loop current.

Calibration is a 2-step process: The zero-scale range needs adjustment before the full-scale point. For the zero adjustment, you drive a current of zero scale plus 1 LSB (20 mA+3.9 μA) into the loop while the AD7582 continuously converts channel A_{IN0}. As you read the conversion results, adjust R_6 until the AD7582's LSB flickers with all other bits off. You adjust the full-scale point with a loop current of full scale minus 1 LSB (4 mA−3.9 μA) flowing in the loop. Repeatedly converting and reading the A_{IN0} results, you vary R_8 until the AD7582's LSB flickers with all other bits on. The system is now calibrated.

The input structure in **Fig 2** effectively eliminates a phenomenon known as resistor self-heating, a problem that plagues conventional detectors which simply moni-

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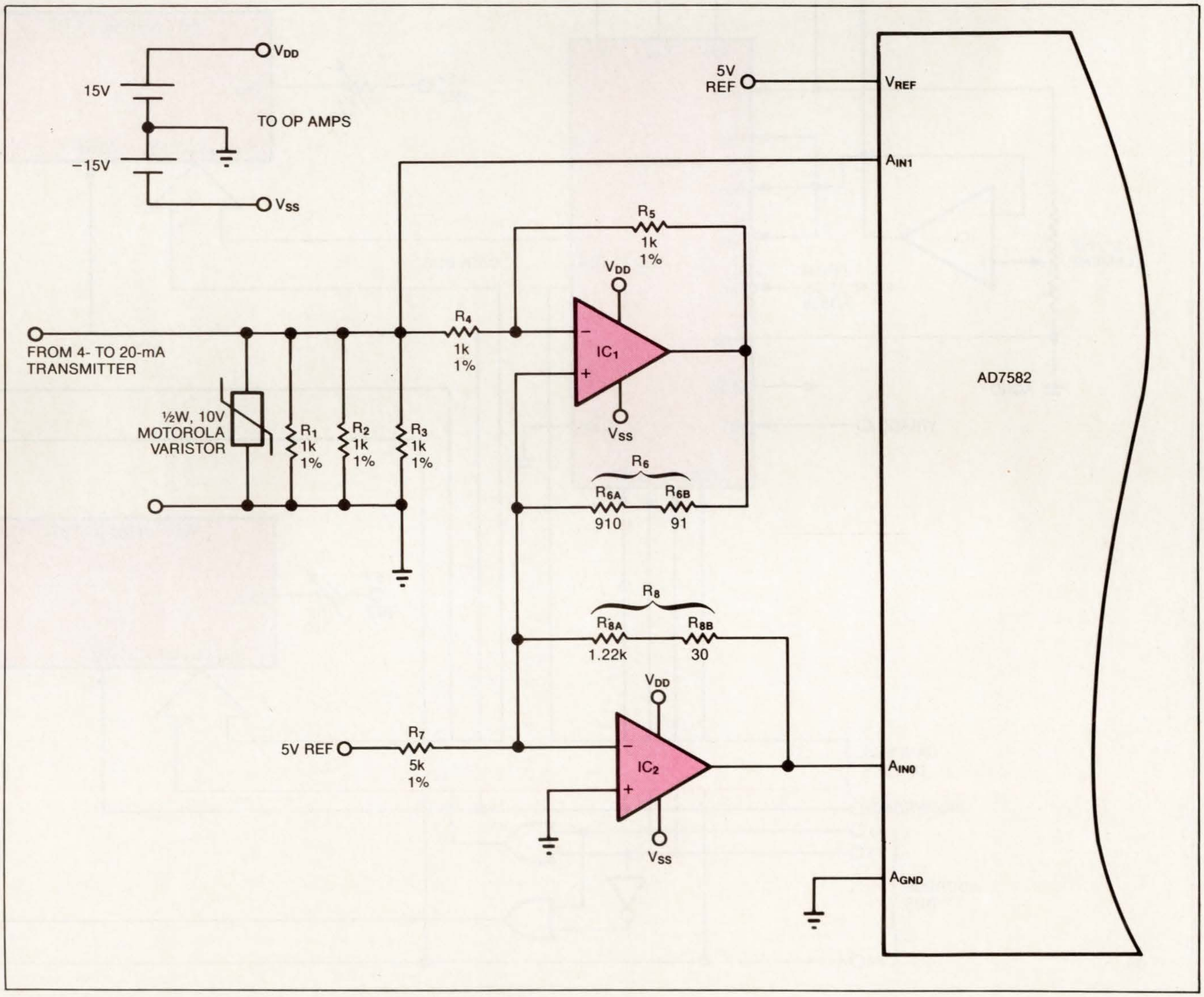


Fig 2—To simplify 4- to 20-mA loop detector monitoring, *this circuit bleeds a fraction of the loop current into a current mirror based around IC_1. IC_2 then sums the mirrored current with a 1-mA fixed offset current.*

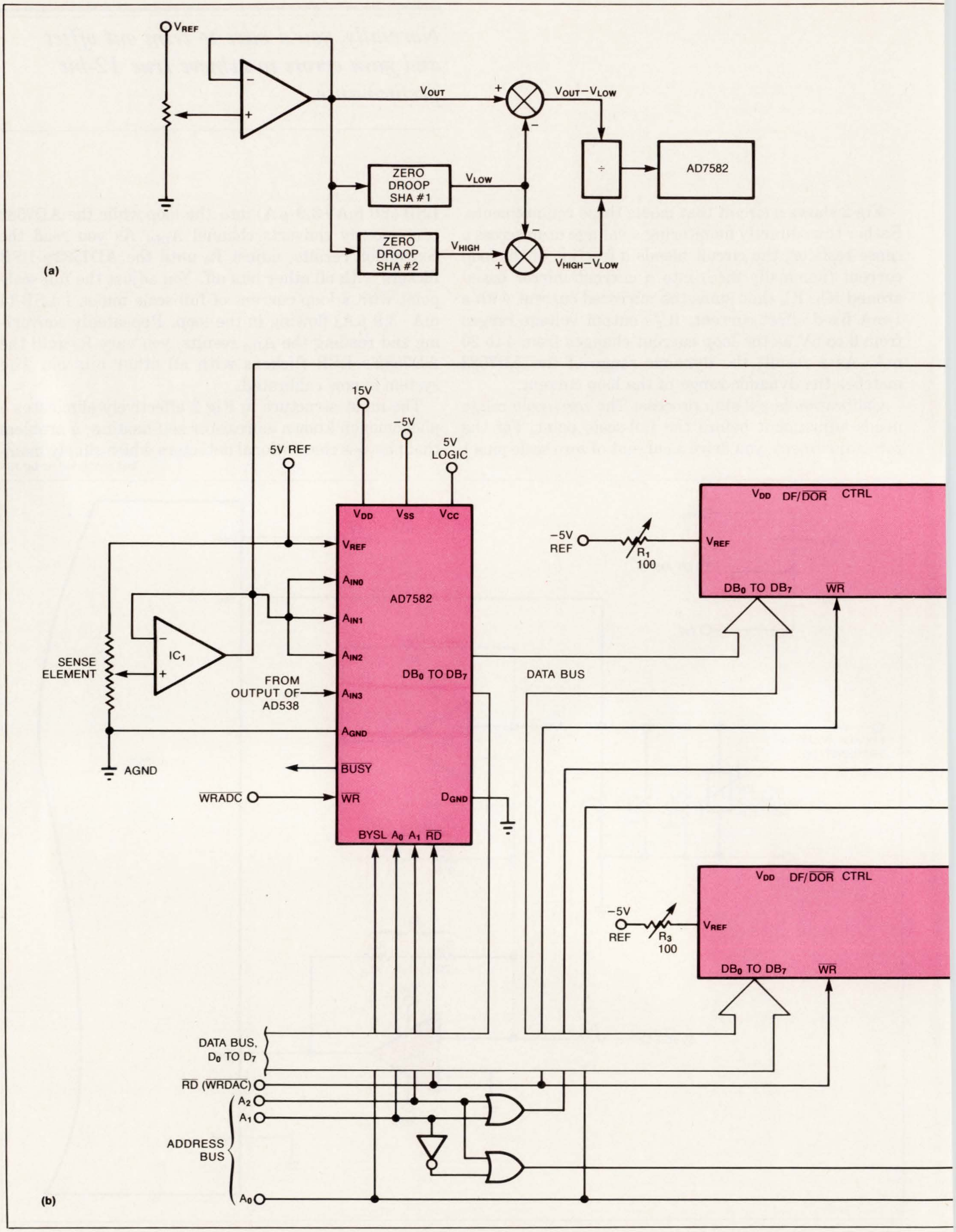
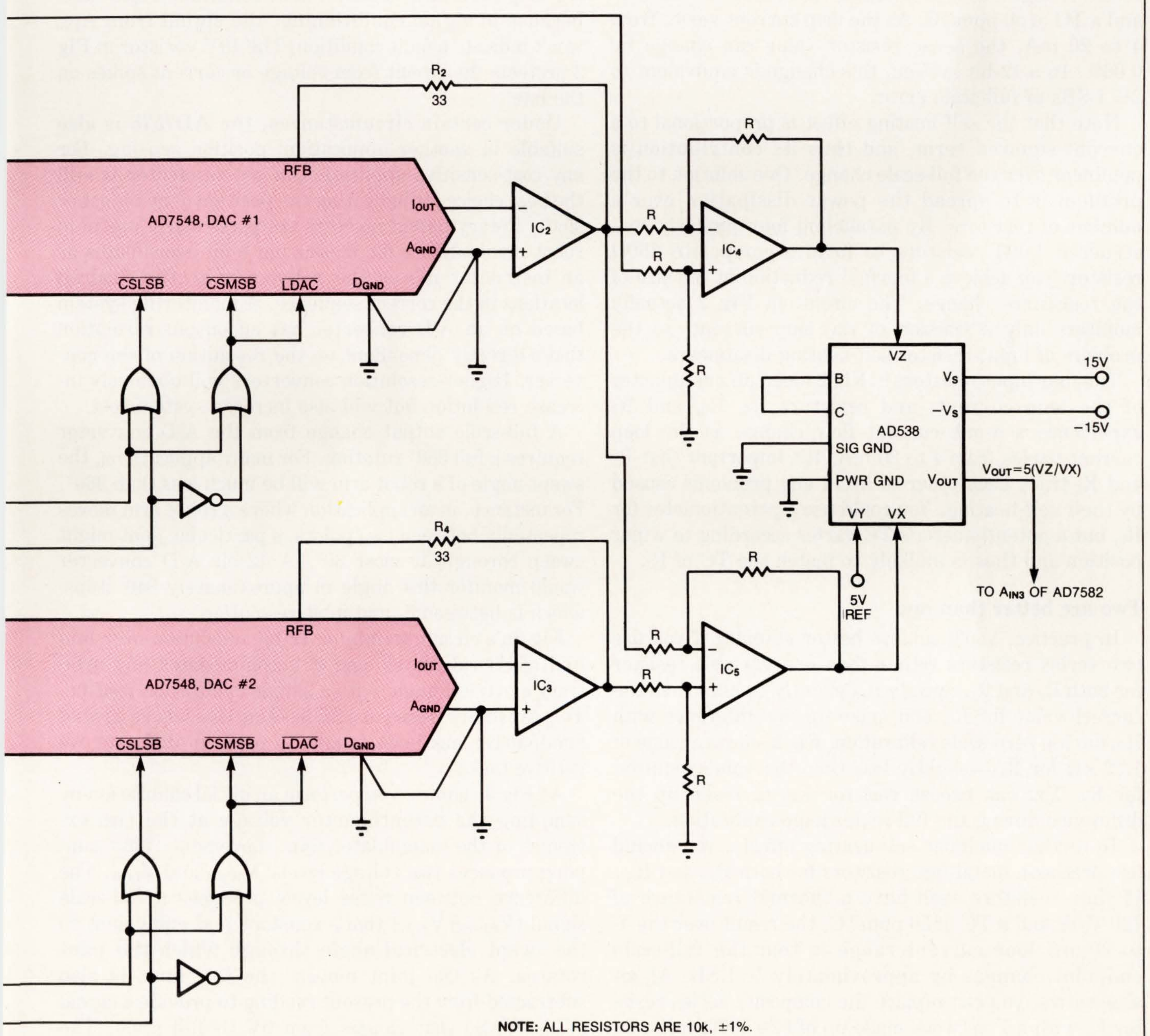


***Fig 3—You can perform an initial calibration** by sampling the potentiometer voltage at the two extremes of the manipulator joint movement **(a)**. The 12-bit D/A converters provide the sample/hold function **(b)**. DAC #1 holds V_{LOW} data, and DAC #2 holds data for V_{HIGH}.*

IC_2	IC_1	CHANNEL SELECTED	MEASUREMENT FUNCTION
0	0	A_{IN0}	SHA, V_{LOW}
0	1	A_{IN1}	SHA, V_{HIGH}
1	0	A_{IN2}	MONITOR, V_{OUT}
1	1	A_{IN3}	RATIOED INPUT



NOTE: ALL RESISTORS ARE 10k, ±1%.

tor the voltage change across a 250Ω resistor. Because every resistor has a finite thermal resistance, its actual value is affected—via its temperature coefficient (TC)—by the heat it dissipates. The greater the thermal resistance and the greater the TC, the greater the problem. For example, a standard ¼W, 250Ω metal-film resistor might have a thermal resistance of 120°C/W and a TC of 50 ppm/°C. As the loop current varies from 4 to 20 mA, the sense resistor value can change by 0.06%. In a 12-bit system, this change is equivalent to 2½ LSBs of full-scale error.

Note that the self-heating effect is proportional to a current-squared term, and thus its contribution is nonlinear over the full-scale change. One solution to the problem is to spread the power dissipation over a number of resistors. By paralleling four similarly constructed 1-kΩ resistors to form a composite 250Ω resistor, you achieve a fourfold reduction in the size of the resistance change. The circuit in **Fig 2** actually monitors only a fraction of the loop current, so the problem of input-resistor self-heating disappears.

The four input resistors in **Fig 2** bleed off one-quarter of the loop current, and resistors R_5, R_6, and R_8 experience a 4-mA current flow change as the loop current varies from 4 to 20 mA. It's important that R_5 and R_6 track each other to avoid any problems caused by their self-heating. You could use a potentiometer for R_6, but a potentiometer's TC varies according to wiper position and thus is unlikely to match the TC of R_5.

Two are better than one

In practice, you'll achieve better stability if you use two series resistors rather than one variable resistor for both R_6 and R_8. Specify R_{6A} slightly smaller than the correct value for R_6, and make up the difference with R_{6B} during zero-scale calibration. **Fig 2** shows a value of 1.22 kΩ for R_{8A}—slightly less than the value required for R_8. You can choose resistor R_{8B} to make up the difference during the full-scale range calibration.

To further minimize self-heating effects, you should use precision metal-film resistors for both R_{8A} and R_{8B}. If your resistors each have a thermal resistance of 120°C/W and a TC of 50 ppm/°C, the result over the 4- to 20-mA loop current range is that the full-scale endpoint changes by approximately ½ LSB. As an alternative, you can replace the composite series resistor R_8 with a T network made up of two 500Ω resistors in series and a 1-kΩ resistor to ground. With the T network, self-heating is negligible.

You can use the A_{IN1} channel of the A/D converter to directly monitor the signal voltage across the composite 250Ω resistor, which is quite helpful for fault-detection purposes. If the loop should open, then A_{IN1} will read 0V. Furthermore, if you're using a thermocouple, the thermocouple conditioner or the 4- to 20-mA transmitter can detect this burnt-out thermocouple and reduce the loop current to 0 mA: a fault condition. Note that, because of signal conditioning, the signal from A_{IN0} won't indicate a fault condition. The 10V varistor in **Fig 2** protects the circuit from voltage or current spikes on the line.

Under certain circumstances, the AD7578 is also suitable in another application: position sensing. For any cost-sensitive application, a potentiometer is still the best choice for indicating the position of an object or shaft. Rotary potentiometers are particularly useful in robot manipulators for measuring joint coordinates as an instructor moves the robot arm to the desired locations in the correct sequence. A monitoring system based on an A/D converter has an output resolution that's directly dependent on the resolution of the converter. Higher-resolution converters will obviously increase resolution but will also increase system cost.

A full-scale output change from the A/D converter requires a full 360° rotation. For many applications, the swept-angle of a robot arm will be much less than 360°. For instance, in an application where a robot arm moves repeatedly between two points, a particular joint might sweep through at most 30°. A 12-bit A/D converter would monitor this angle in approximately 340 steps, which is between 8- and 9-bit resolution.

Fig 3a's circuit maintains 12-bit resolution over limited electrical travel, and it accommodates any arbitrary electrical angle with a simple calibration routine. This capability is very useful in situations where a robot manipulator has been taught to perform different repetitive tasks.

As **Fig 3a** shows, you perform an initial calibration by sampling the potentiometer voltage at the two extremes of the manipulator joint movement. This sampling produces two voltage levels: V_{HIGH} and V_{LOW}. The difference between these levels produces a full-scale signal ($V_{HIGH}-V_{LOW}$) that's constant and equivalent to the swept electrical angle through which the joint rotates. As the joint moves, the low limit is also subtracted from the present reading to provide a signal ($V_{OUT}-V_{LOW}$) that ranges from 0V to full scale. The ratio of these two signals varies from 0 to 100%. When you properly scale the divider block to translate its ratioed output into a 0 to 5V analog signal suitable for

When monitoring 4- to 20-mA loops, you must be able to adjust zero and full-scale range independently.

the AD7582, the system provides 12-bit resolution over the swept angle.

This resolution has a significant impact on circuit performance. For instance, if the 4096 steps of the 12-bit ADC are scaled to cover a swept angle of 45° (one-eighth of the basic 360°), the LSB size will equal 0.01°, which is equivalent to 15-bit resolution. The practicality of this resolution depends on the output smoothness of the potentiometer wiper signal.

Contactless potentiometers, based on a magneto-resistive material, are completely free from sliding noise. When exposed to a magnetic field, the electrical resistance of this material increases. Rotating a permanent magnet, which is attached to a shaft close to two magneto-resistors in series, produces a potentiometric voltage divider. Contactless potentiometers have a number of disadvantages, but they are capable of monitoring movements as small as 1 μm.

ADCs provide S/H functions

In the more detailed diagram of **Fig 3b,** the 12-bit D/A converters, loaded directly from the AD7582, provide the sample/hold-amplifier (SHA) functions. (The A_{IN0} and A_{IN1} channels are dedicated solely to this purpose.) Under μP control, address lines A_1 and A_2 select an SHA channel and the corresponding D/A converter that requires updating. DAC #1 holds data corresponding to V_{LOW}, and DAC #2 holds data for V_{HIGH}. To update an SHA channel, the potentiometer rotates as far as its respective limit will allow, and the $\overline{\text{WRADC}}$ is pulsed low to begin a conversion. When the conversion is complete, the μP executes a read instruction to the same channel.

Because the A/D converter's $\overline{\text{RD}}$ is also the D/A converters' $\overline{\text{WRDAC}}$ signal, the conversion results are transferred from the A/D converter into the respective D/A converter. And, because of the 8+4 format of the A/D-converter data, you need two $\overline{\text{RD}}$ instructions to transfer the full conversion results.

The AD7548 converters are configured to accept the right-hand-justified 8+4 data of the AD7582. The μP's A_0 address line selects and controls the transfer of the low and high byte from the A/D converter to the correct D/A-converter register. Op amps IC_4 and IC_5 perform the subtraction, and the AD538, a monolithic computational circuit capable of providing analog multiplication, division, and exponentiation, performs the precision ratioing. The VY input of the AD538 provides output scaling for the VZ/VX ratioed signal (the A_{IN3} input of the AD7582). The A_{IN3}'s 12-bit conversion result represents the swept angle that the wiper of the precision potentiometer moves through.

Initial system calibration is straightforward. The 100Ω trimming potentiometers (R_1 and R_3) in series with the voltage reference input of each DAC compensate for gain errors in the DACs themselves, as well as any gain errors in the ADC and subtracting amplifiers IC_4 and IC_5. The fact that you can use the DF/$\overline{\text{DOR}}$ and CTRL inputs to override the DAC registers of the AD7548 with all ones or all zeros simplifies the calibration.

To start, you set V_{HIGH}, V_{LOW}, and V_{IN} at full scale and adjust the trimming potentiometers to achieve 0V at the outputs of the subtracting amplifiers. Calibrate the $V_{HIGH}-V_{LOW}$ channel first. For a correct adjustment, V_{LOW} must be exactly 5V full scale. You accomplish adjustment by driving the DF/$\overline{\text{DOR}}$ input of DAC #1 to a logic low and then adjusting R_1 for a 5V output on IC_2. Maintaining these conditions on DAC #1, you now drive the noninverting input of IC_1 with V_{REF}. Carry out a single conversion on A_{IN1} and use a read instruction to transfer the results to DAC #2. You then adjust R_3 until IC_5's output equals 0V.

You calibrate DAC #1 in a similar manner. Carry out a single conversion on A_{IN0} and transfer the results to DAC #1 (data override input DF/$\overline{\text{DOR}}$ is now at a logic high). Then, adjust R_1 until the output of IC_4 is 0V.

The AD538 denominator has a wide 1000:1 dynamic range, and the divider's input offset voltage becomes increasingly important as the denominator gets smaller. If you restrict the dynamic range of the denominator to 10:1, you won't need to do any trimming to achieve a divider accuracy of 0.5%. Under these conditions, the system will accommodate a lower limit of approximately 36° for the swept angle.

Sample/hold amplifier can stand alone

In yet another application with few design headaches, you can use the AD7578 ADC and some additional logic to develop a stand-alone sample/hold system that requires no μP control **(Fig 4a)**. In fact, you need only one control input: the conversion-start signal. You drive the ADC clock input from a 74HC-compatible source at 140 kHz. In **Fig 4a,** the ADC and DAC are both configured for bipolar operation, which allows the circuit to sample and hold over a ±5V input signal range. Because the same 5V reference is applied to both the ADC and DAC, a 1:1 correspondence exists between the input and output in terms of signal magnitude and polarity. The ADC's output code is offset-

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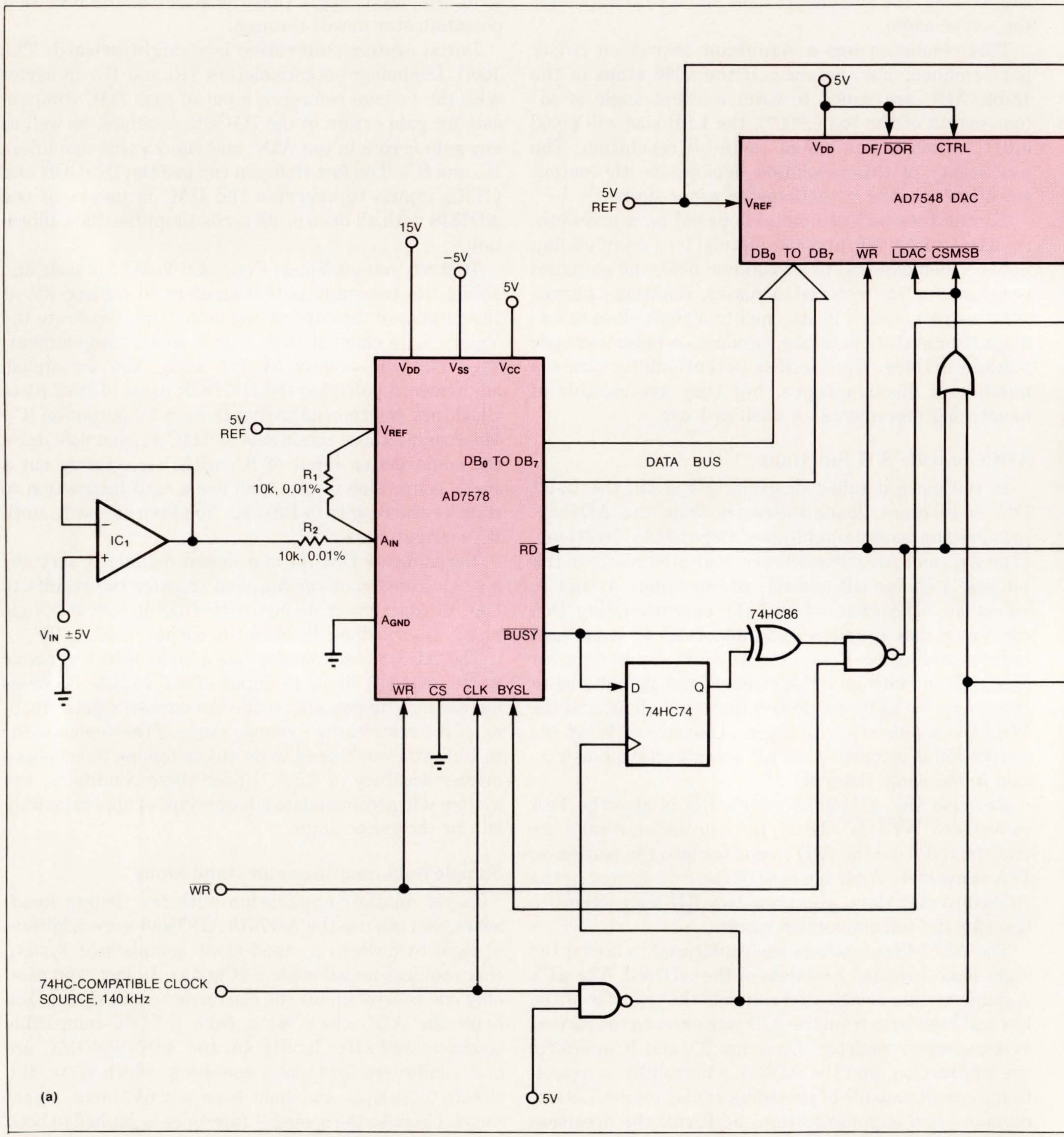
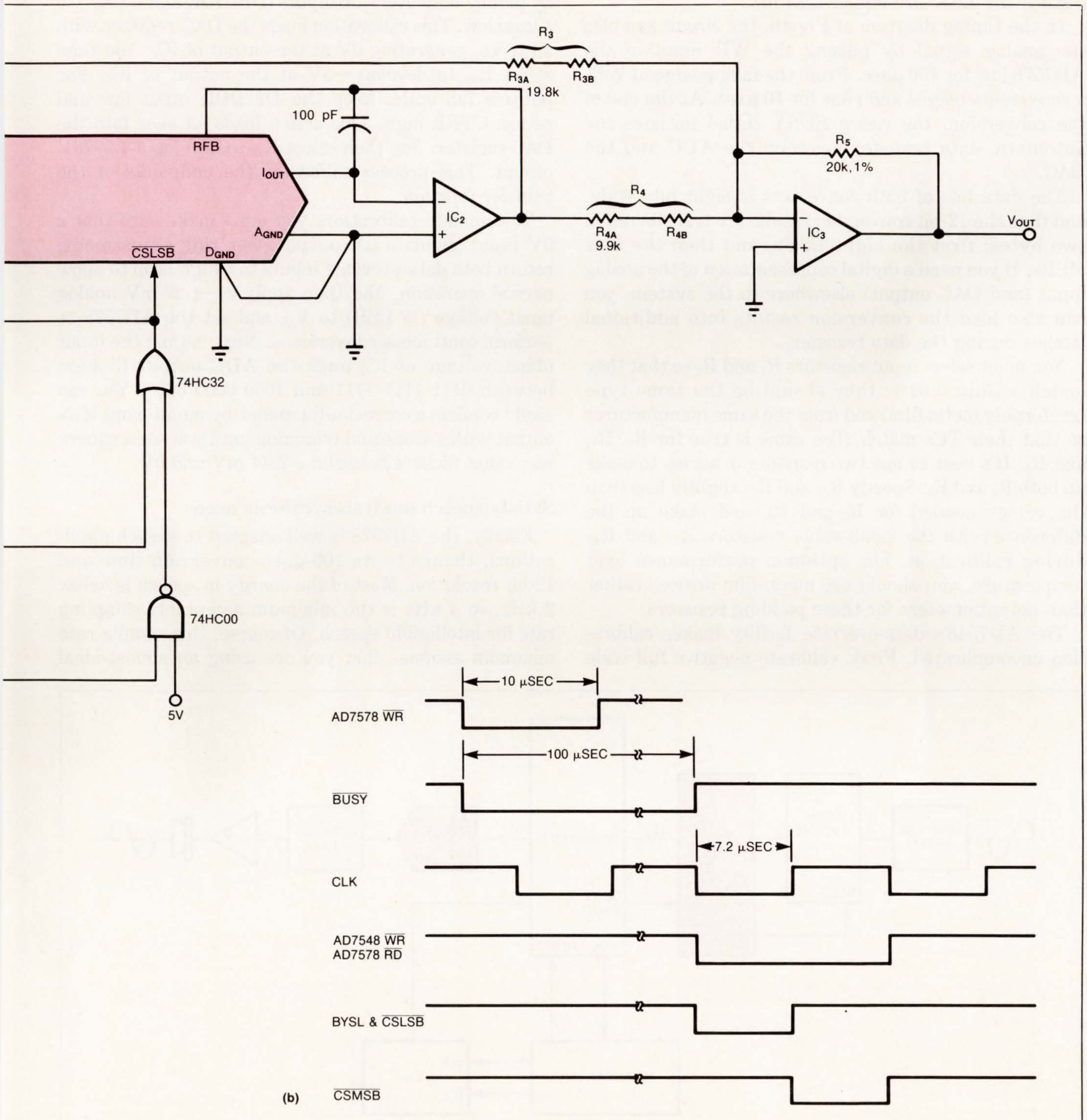


Fig 4—Combining some additional logic with the AD7578, *you can develop a stand-alone sample/hold system that requires no μP control **(a)**. A conversion begins on the falling edge of $\overline{WR}$ **(b)** and runs for 100 μsec. At the end of the conversion, the rising $\overline{BUSY}$ signal initiates an automatic data transfer between the ADC and the DAC.*


R3
R3A
R3B
19.8k
100 pF
RFB
IOUT
IC2
AGND
CSLSB
DGND
R5
20k, 1%
R4
R4A
R4B
9.9k
IC3
VOUT
74HC32
74HC00
5V
10 µSEC
AD7578 WR
100 µSEC
BUSY
7.2 µSEC
CLK
AD7548 WR
AD7578 RD
BYSL & CSLSB
(b)
CSMSB

When cost is crucial, the potentiometer still represents the best solution for position-sensing applications.

binary; the LSB size equals 2.24 mV.

In the timing diagram of **Fig 4b,** the circuit samples the analog signal by pulsing the $\overline{WR}$ input of the AD7578 low for 100 μsec. From the falling edge of $\overline{WR}$, a conversion begins and runs for 10 μsec. At the end of the conversion, the rising $\overline{BUSY}$ signal initiates the automatic data transfer between the ADC and the DAC.

The data bus of both converters is eight bits wide, and thus the 12-bit conversion results are transferred in two bytes: first the eight LSBs, and then the four MSBs. If you need a digital representation of the analog input (and DAC output) elsewhere in the system, you can also load the conversion results into additional latches during the data transfer.

You must select input resistors R_1 and R_2 so that they match within 0.01%; they should be the same type (preferably metal film) and from the same manufacturer so that their TCs match. The same is true for R_3, R_4, and R_5. It's best to use two resistors in series to make up both R_3 and R_4. Specify R_{3A} and R_{4A} slightly less than the values needed for R_3 and R_4, and make up the difference with the small-value resistors R_{3B} and R_{4B} during calibration. For optimum performance over temperature, you should use metal-film devices rather than potentiometers for these padding resistors.

The AD7548's data-override facility makes calibration uncomplicated. First, calibrate negative full scale by pulling both override inputs (DF/$\overline{DOR}$ and CTRL) to a logic low. This calibration loads the DAC register with all zeros, generating 0V at the output of IC_2. You then select R_{3B} to develop −5V at the output of IC_3. For positive full scale, keep the DF/$\overline{DOR}$ input low and return CTRL high. This action loads all ones into the DAC register. You then select R_{4B} to develop a 4.9976V output. This process calibrates the endpoints of the transfer function.

To complete calibration, you must make sure that a 0V input yields a 0V output. For this adjustment, return both data-override inputs to a high level to allow normal operation. You then apply a −1.22-mV analog input voltage (½ LSB) to V_{IN} and set the AD7578 to perform continuous conversions. Next, adjust the input offset voltage of IC_1 until the ADC output flickers between 0111 1111 1111 and 1000 0000 0000. You can easily confirm a correct adjustment by monitoring IC_3's output with a scope and trimming until you see a square wave that flickers between −2.44 mV and 0V.

Satisfy speech analysis/synthesis needs

Finally, the AD7578 is well adapted to speech applications, thanks to its 100-μsec conversion time and 12-bit resolution. Most of the energy in speech is below 2 kHz, so 4 kHz is the minimum acceptable sampling rate for intelligible speech. Of course, this sample rate minimum assumes that you are using an almost-ideal

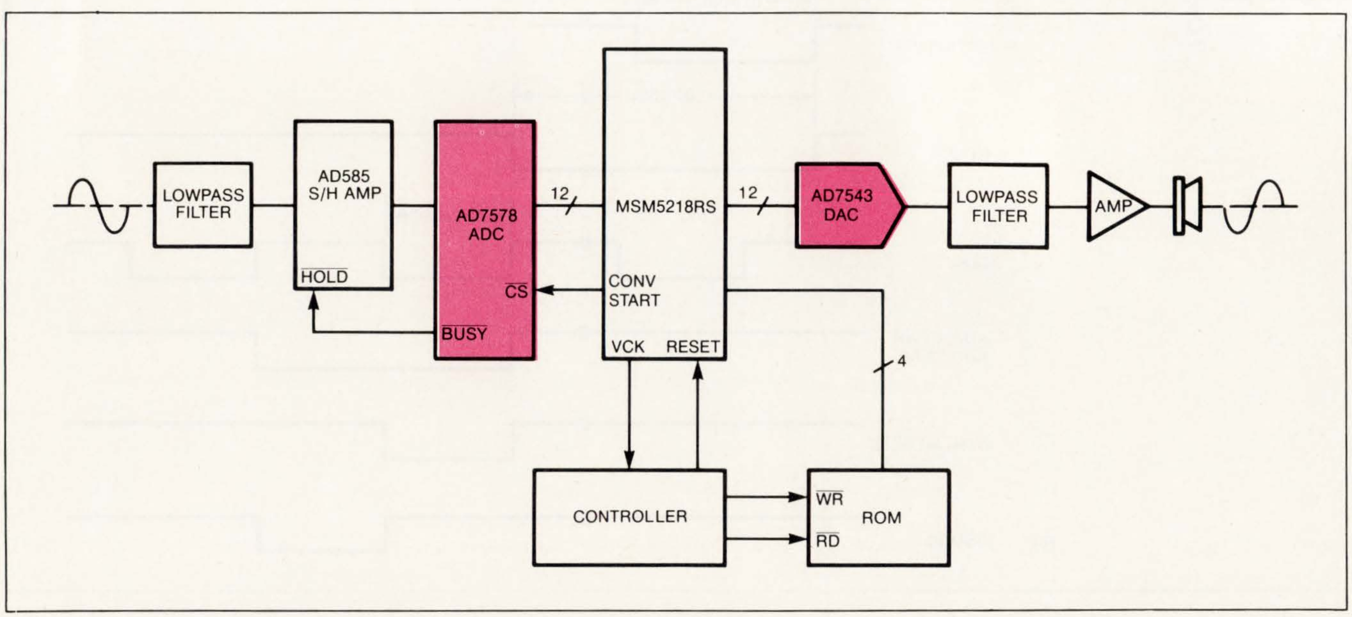


Fig 5—Before being quantized by the AD7578, *the input signal in this speech system goes through some signal-conditioning circuitry and a lowpass filter. The 12-bit data is compressed to four bits for storage in ROM.*

antialiasing filter. To ease filter design and enhance speech quality, most designs employ an 8-kHz sampling frequency.

The ADC's resolution also directly affects speech quality. Insufficient resolution results in too coarse a reproduction, and thus influences intelligibility. More bits means better S/N ratio and better overall fidelity. Ultimately, the amount of memory normally constrains the upper limit. A 12-bit A/D converter, operating at an 8-kHz sampling rate, will fill up 64k bytes of memory in just over five seconds. For an 8-bit A/D converter, it's eight seconds.

Fortunately, voice waveforms contain a lot of redundant information and don't require such high bit rates. Signal-processing routines and dedicated devices introduced in recent years transmit and store voice signals much more efficiently.

One of these, the MSM5218RS speech analysis/synthesis IC from OKI Semiconductor (Sunnyvale, CA), uses an adaptive differential pulse-code modulation (ADPCM) method of data compression. It condenses 12-bit PCM samples into three or four bits. The MSM5218RS also contains a synthesis stage, which expands the 3- or 4-bit ADPCM data to 12-bit PCM data. In addition, it has an onboard 10-bit D/A converter, which you can use to reconstruct the speech signal. You can use an external DAC to provide 12-bit resolution, too.

Taking a slightly more in-depth look at ADPCM will help your understanding. PCM defines the output code of an ADC after quantization. An S/H amp freezes the speech input while an ADC performs the quantizing operation. In differential PCM, the current code is subtracted from the code immediately preceding it, and the result is the new DPCM code. This subtraction significantly reduces the data-transfer rate because, compared with the actual PCM value, the differential PCM value requires fewer bits.

Distortion may occur, though, if the difference between samples is greater than the DPCM encoding value. This difference is called a compliance error. To solve this distortion problem, you must reduce the input-signal bandwidth. ADPCM minimizes the compliance error by adaptively changing the DPCM quantizer step size to suit the waveform being digitized. If the difference between successive samples is great, it increases the step size, and vice-versa, reducing the overall data rate and keeping the compliance error to a minimum. The MSM5218RS uses an ADPCM technique based on the characteristics of speech waveforms. It isn't suitable for triangular waves, square waves, or other such waveforms.

Fig 5 shows a typical speech system. Before being quantized by the AD7578, the input signal goes through some signal-conditioning circuitry and a lowpass filter. The digital data is then compressed from 12 to 4 bits before being stored in ROM. To reproduce the data, the MSM5218RS expands the data, and an AD7543 reconstructs the analog speech input.

To evaluate the system, you can configure the MSM5218RS to operate simultaneously in an analysis/synthesis mode **(Fig 6)**. Except for the ROM storage capabilities, this circuit contains all the necessary components and interface details of a complete digital-speech system. Evaluating a speech system isn't simple because no well-defined tests or instrumentation exist that provide verifiable measurements. You can make a reasonable evaluation by listening to the reproduced speech with an impartial ear. If you've ever carried out such a test, you'll have to agree that eight bits is more than adequate for speech intelligibility.

Nonetheless, increasing the resolution to 12 bits yields a marked improvement in speech quality and naturalness of sound. Because the MSM5218RS's data output rate is the same for 8 and 12 bits, the IC offers these improvements without any memory-capacity penalty. Overall, the system in **Fig 6** provides an efficient means of storing voice inputs, and it reproduces a high-quality speech output that's hard to distinguiush from the original input.

The input signal passes through buffering and lowpass-filtering circuitry before reaching the AD585 S/H amp's input. All the analog stages are ac coupled. Resistor R_3 ensures that the input signal covers the full dynamic analog input range of the AD7578. The MSM5218RS provides timing and control, generating a start conversion (SCON) pulse every 125 μsec. SCON triggers an AD7578 conversion, which the AD7578 acknowledges by bringing its $\overline{\text{BUSY}}$ output low. $\overline{\text{BUSY}}$ asserts the $\overline{\text{HOLD}}$ input of the AD585 S/H amp and freezes the analog input.

In any sampling circuit, it's important that the samples occur at equal intervals. The equidistant $\overline{\text{SCON}}$ pulses, derived from the MSM5218RS clock, ensure such performance. The same clock provides the clock input for the AD7582 via the resonator, which oscillates at 384 kHz. This clock rate is divided by 3 before being applied to the AD7578. The division process increases the conversion time slightly (to 110 μsec), but the 15 μsec available is more than ample time for the circuit to

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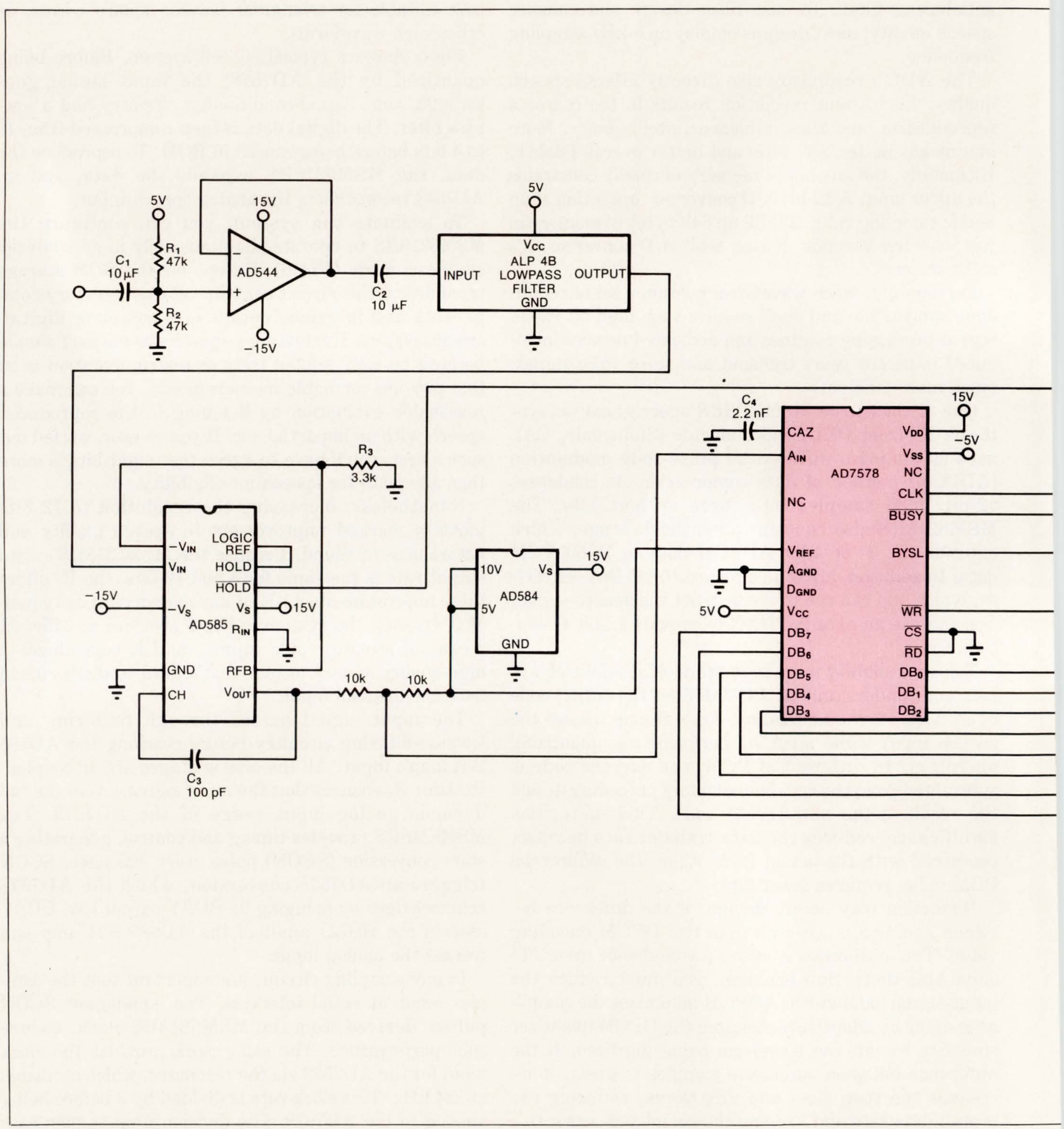
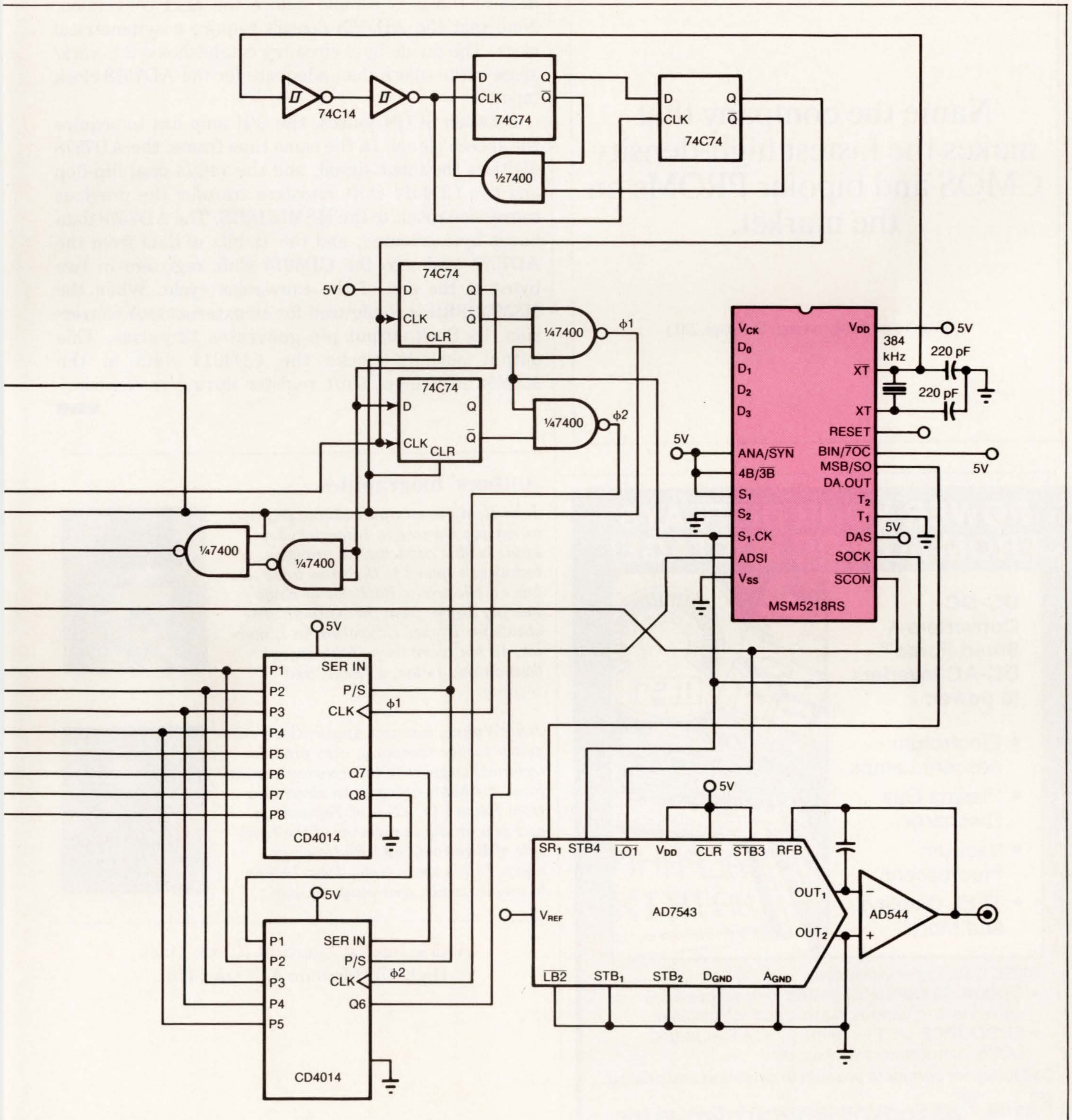


Fig 6—Except for ROM storage accommodations, *this circuit contains all the necessary components of a complete digital speech system. It reproduces a high-quality output hard to distinguish from the original input.*


74C14
74C74
D
CLK
Q
74C74
½7400
5V
¼7400
φ1
φ2
CLR
VCK
D0
D1
D2
D3
ANA/SYN
4B/3B
S1
S2
S1.CK
ADSI
VSS
VDD
XT
RESET
BIN/7OC
MSB/SO
DA.OUT
T2
T1
DAS
SOCK
SCON
MSM5218RS
384 kHz
220 pF
SER IN
P/S
P1
P2
P3
P4
P5
P6
P7
P8
Q7
Q8
Q6
CD4014
SR1
STB4
LO1
CLR
STB3
RFB
VREF
AD7543
OUT1
OUT2
LB2
STB1
STB2
DGND
AGND
AD544

read the A/D-converter data and for the S/H amp to acquire the next sample before the next conversion. Note that the AD7578 doesn't require a symmetrical clock. The divide-by-3 circuitry establishes a 2:1 work/space ratio—more than adequate for the AD7578 clock input.

Between $\overline{\text{SCON}}$ pulses, the S/H amp has to acquire the speech signal. In the same time frame, the AD7578 digitizes the input signal, and the 74C74 dual flip-flop and two CD4014 shift registers transfer the previous conversion result to the MSM5218RS. The AD7578 data bus is byte oriented, and the 12 bits of data from the AD7578 load into the CD4014 shift registers in two bytes at the end of the conversion cycle. When the MSM5218RS is configured for an external D/A conversion, its Sock output pin generates 12 pulses. This output serially clocks the CD4014 data in the MSM5218RS input shift register during conversion.

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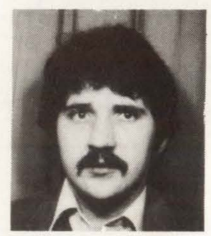
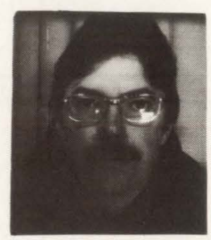
Authors' biographies



John Reidy is an applications engineer at Analog Devices in Limerick, Ireland. In this capacity, he provides technical support to the sales force. He has an Electronic Bachelor of Engineering degree from the National Institute for Higher Education in Limerick. In his spare time, John enjoys badminton, guitar, softball, and reading.



John Wynne, a senior applications engineer for the company, also provides technical support to the division's sales force. He holds a degree in electronics from Kevin St College of Technology and is a graduate member of the Institute of Electronic and Radio Engineers. In his spare time, John listens to music, reads, and plays squash.

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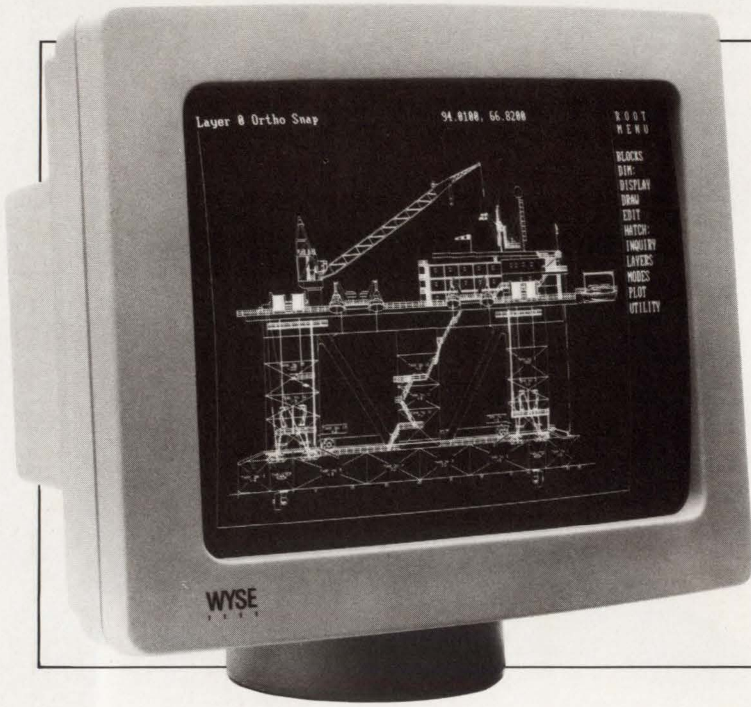

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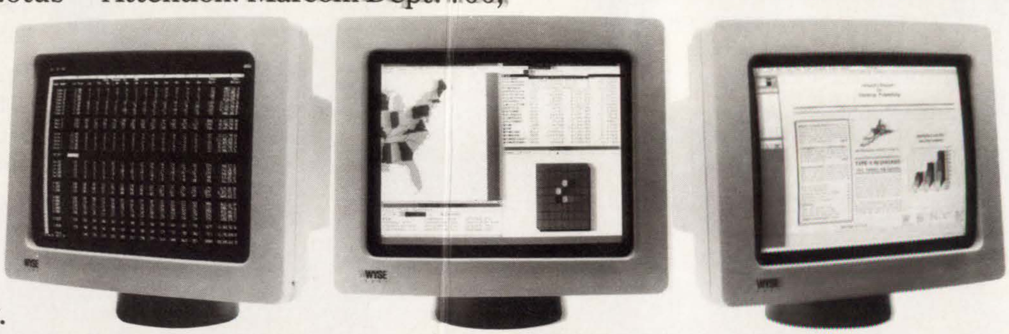


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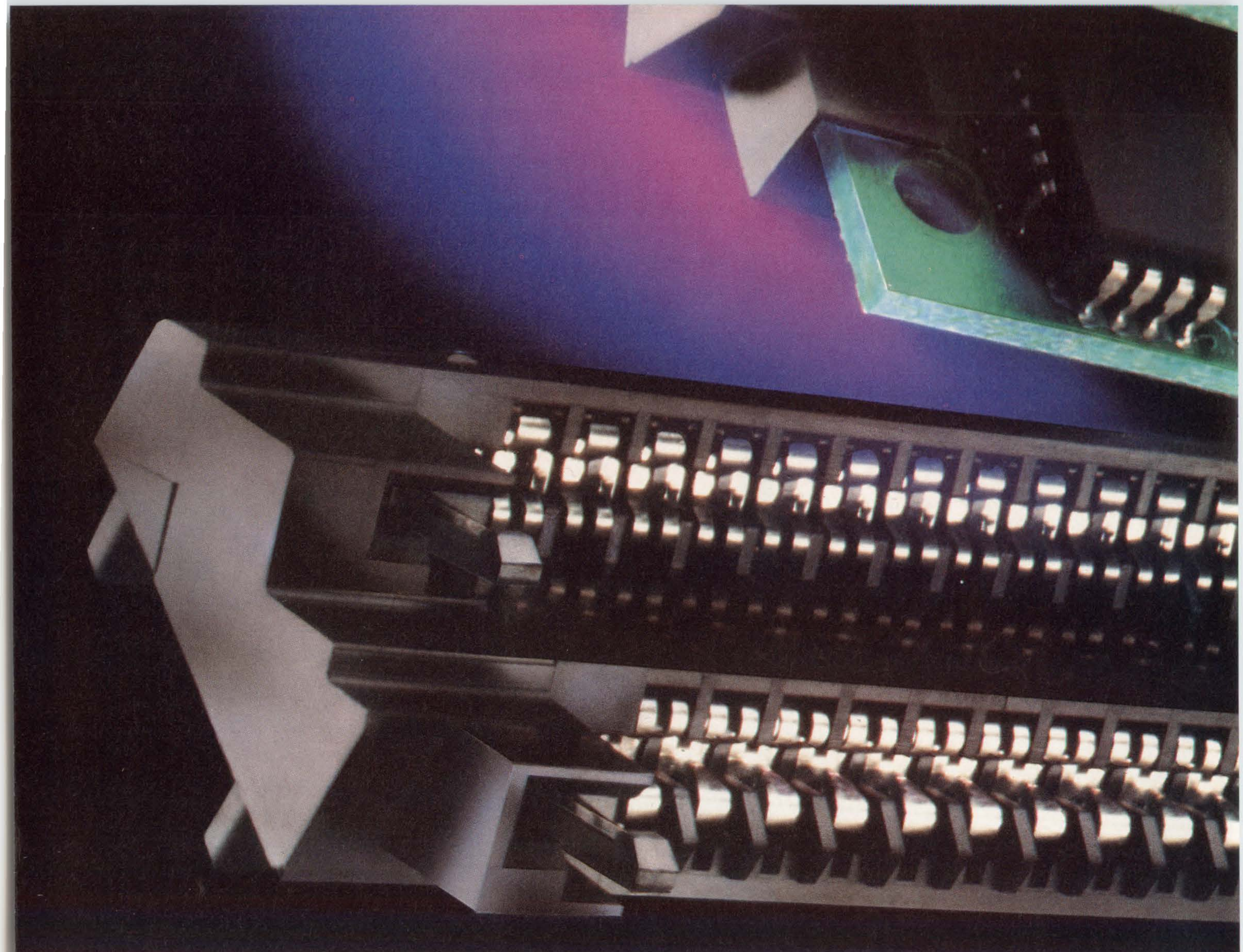

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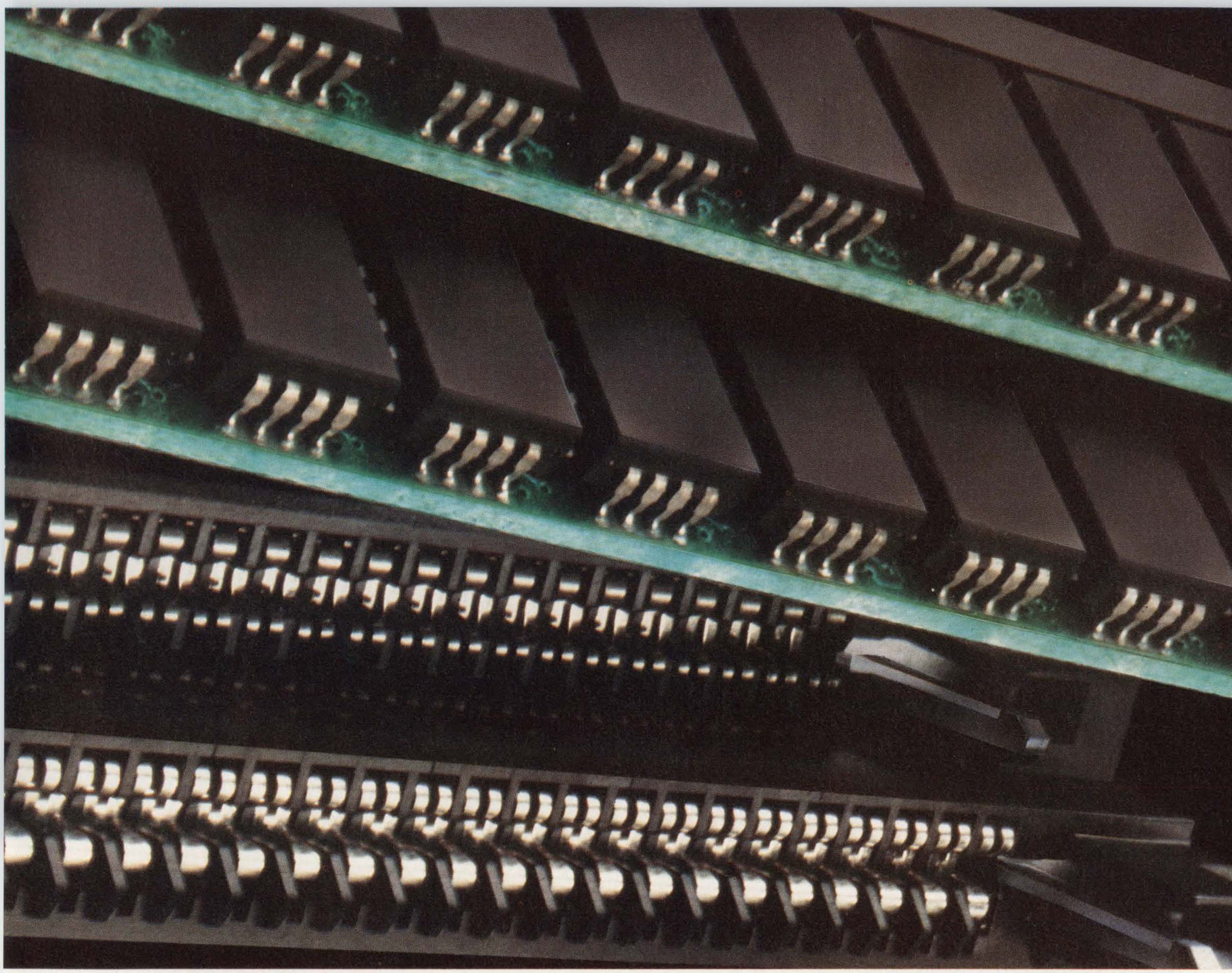

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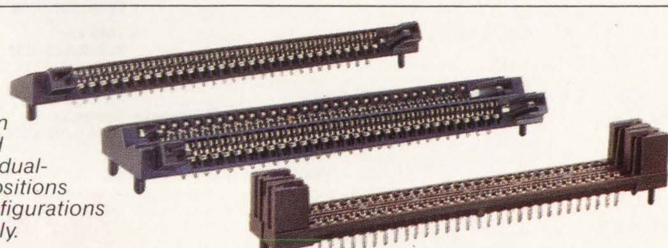

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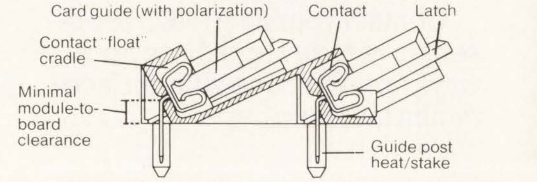

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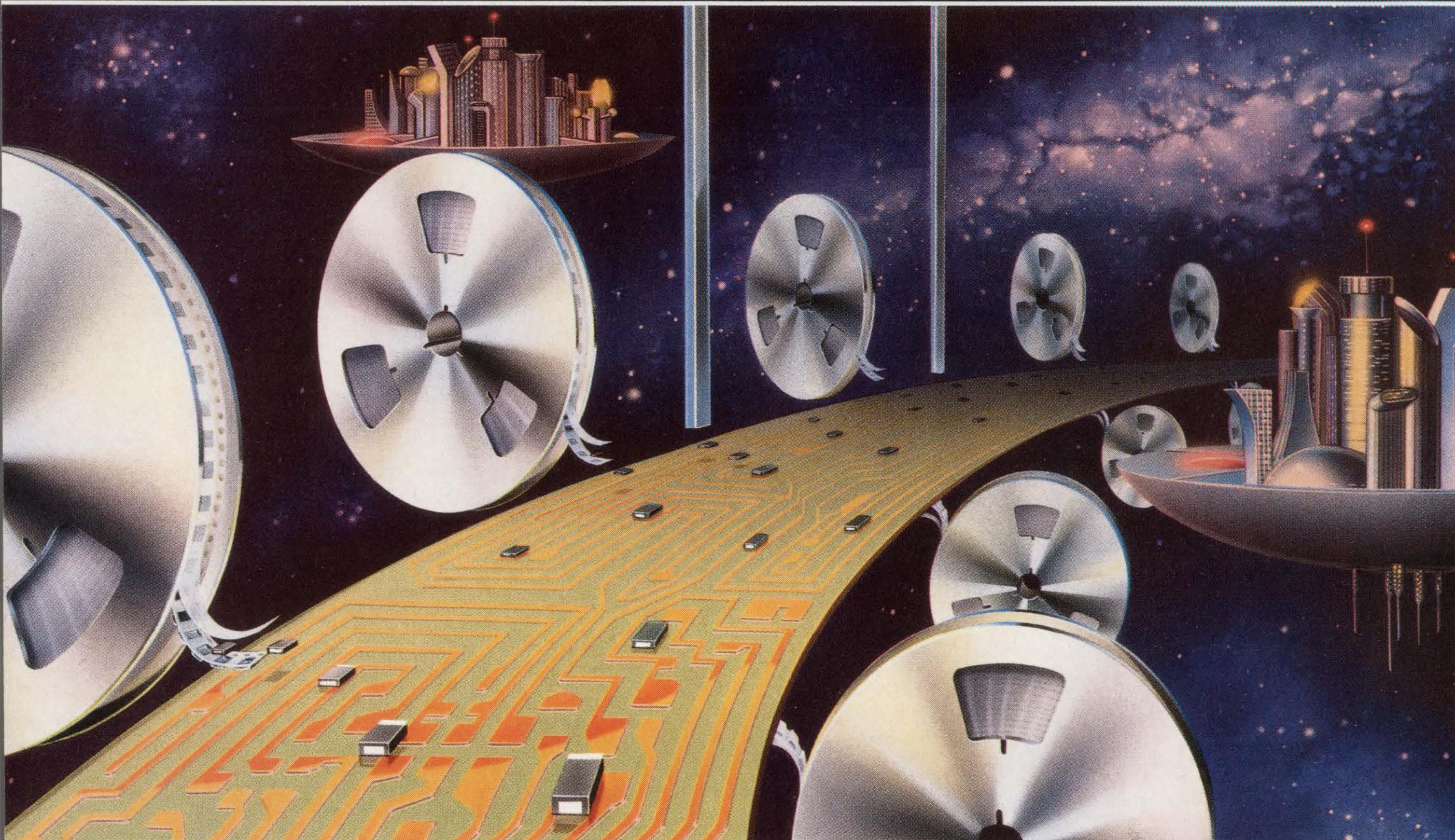

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Interface various IC technologies to CMOS arrays

Many times you have no choice as to what device types your CMOS designs must work with. You need not despair: The key to interfacing devices made from dissimilar technologies lies in a simple analysis of each technology's voltage and current requirements.

Mark Stansberry, *National Semiconductor Corp*

Designs based on CMOS standard and semicustom cells must interact with devices that are fabricated in a wide variety of technologies. In communication systems, for example, high-speed data is often processed using fast bipolar circuitry and then sent on to slower CMOS systems. Old products that have not reached the end of their useful lives often employ TTL and metal-gate technologies, and these systems also must interface with CMOS circuitry. You can handle the interface problem easily by addressing a few simple voltage and current considerations.

The input- and output-voltage switching levels of two distinct technologies must be compatible, the current sourcing and sinking capability of the two technologies must mesh, and absolute voltage and current levels for the technologies must not be exceeded. In addition, you must examine timing requirements very carefully—especially if your design must drive such highly capacitive loads as a 3-state bus.

One important initial consideration with any circuitry is noise—both signal-line and power-line noise. Schmitt trigger inputs, which are available on standard cells, increase immunity to signal-line noise. You can also choose from a variety of output-power options to minimize switching transients that appear on the power lines. These methods of handling noise problems impose no restrictions on your attempts to render compatible the input-voltage switching levels of different technologies.

CMOS-cell arrays present very few problems to other technologies as far as input parameters are concerned. CMOS's input drive requirements are typically on the order of 1 μA for both I_{IH} and I_{IL}. If you decide to include a pullup or pulldown resistor in an input cell, then the input current will increase to approximately 50 μA for I_{IL} (pullup resistor) or I_{IH} (pulldown resistor). Even at 50 μA, devices fabricated in any technology can drive many CMOS devices with ease.

The only major problem you will encounter when you drive CMOS circuitry with devices of another technology is that of matching switching levels. TTL devices typically require V_{IH} to be 2V min, which is unacceptable as a high-level input for CMOS circuitry operating from a 5V supply. You can overcome this incompatibil-

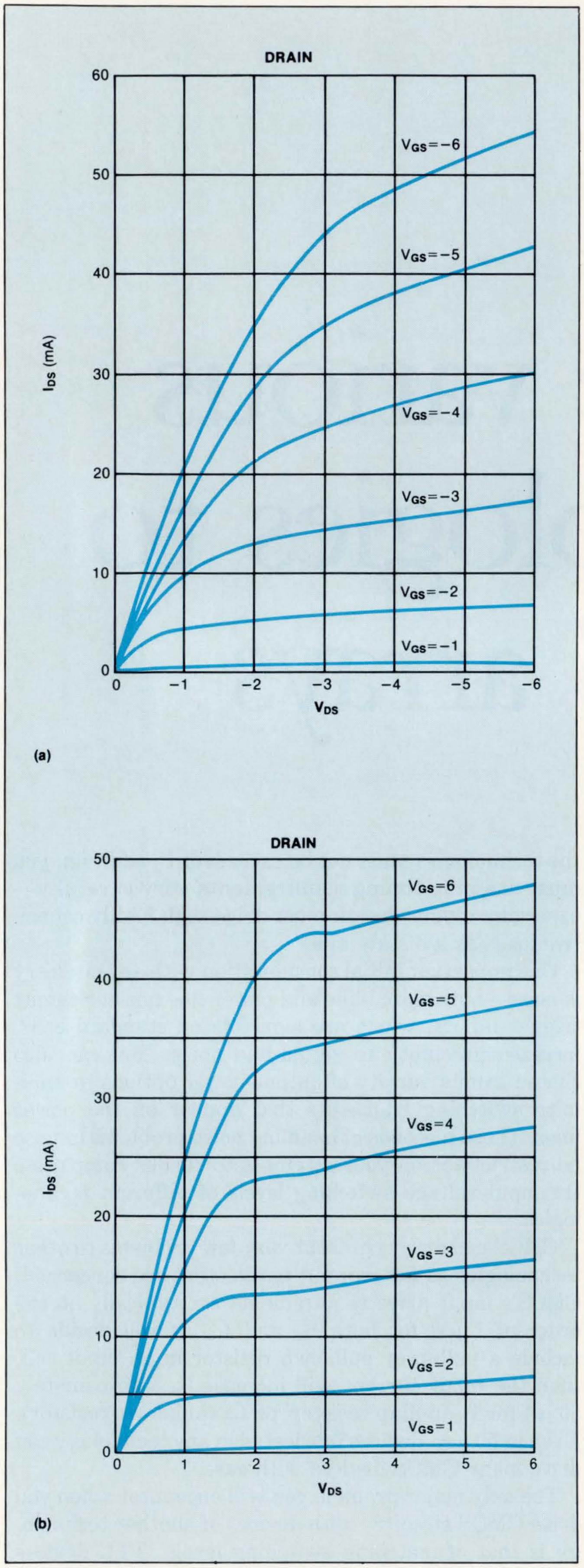

***Fig 1—Voltage and current characteristics** of p-channel **(a)** and n-channel **(b)** transistors reveal the drive capability of output cells and thereby the fan-out associated with the cells.*

ity simply by adding a pullup resistor between the CMOS input and the 5V line, thus driving the input to a higher voltage.

Not only do you need to translate other technologies' logic levels into CMOS levels; you must also make sure that the CMOS inputs are driven higher than 4V and lower than 1V, in order to avoid power-consumption penalties. Between 1 and 4V, the input transistors operate in the linear region and therefore require an inordinate amount of current—2 to 30 mA.

How many outputs can you drive?

Fan-out is a concern in CMOS-cell-based designs only with respect to the output drive capability of the cell array. The input drive current required by an input cell is typically 1.0 μA—low enough that any other logic family would have no trouble driving a multitude of gates. **Fig 1** displays the voltage and current characteristics of n-channnel and p-channel transistors used in the construction of CMOS standard cells. Using these graphs and **Table 1,** you can determine the fan-out that a standard-cell-based design will have when it's interfacing with various technologies.

If, for example, you intend to drive TTL devices with a 4-mA output cell, first look at **Table 1** and determine what the specifications for V_{IH}, V_{IL}, I_{IL}, and I_{IH} are (2V, 0.8V, 1.6 mA, and 40 μA, respectively). Because I_{IL} is orders of magnitude greater than I_{IH}, and the p-channel and n-channel transistors of the cell array can source and sink comparable amounts of current, I_{IL} is the parameter that determines fan-out in this case.

Now look at the voltage and current curves of **Fig 1**; you can see that when the n-channel transistor sinks 16 mA (assuming that V_{GS}=5V), its voltage drop (V_{DS}) is approximately 0.8V. The fan-out in this case is therefore 10 TTL devices, because I_{IL}=1.6 mA, and because V_{DS} must be 0.8V or less (the latter condition follows from the stricture that a valid low input to a TTL gate must be 0.8V or less).

Be mindful of timing requirements

Besides dc considerations, there are, of course, timing concerns related to interfacing various technologies with CMOS. Package, trace, and circuit capacitances of externally driven devices present an ac load to driving devices. Package capacitance is the predominant factor, and if you regard it as the sole contributor to the ac load, you'll obtain a close approximation of the total capacitance. Most packages present between 5 and 15 pF of capacitive load. An output cell driving 10 external

CMOS-cell arrays present very few problems to other technologies as far as input parameters are concerned.

TABLE 1—VOLTAGE AND CURRENT REQUIREMENTS OF VARIOUS IC TECHNOLOGIES

	I_{IH}	I_{IL}	V_{IH}	V_{IL}	V_{OL}	V_{OH}	I_{OL}	I_{OH}
TTL	40 μA	−1.6 mA	2V	0.8V	0.4V	2.4V	1.6 mA	−400 μA
LTTL	10 μA	−0.18 mA	2V	0.7V	0.4V	2.4V	2/3.6 mA	−200 μA
LOW-POWER SCHOTTKY TTL	20 μA	−0.36 mA	2V	0.8V	0.5V	2.5V	4/8 mA	−400 μA
ADVANCED LOW-POWER SCHOTTKY TTL	20 μA	−0.2 mA	2V	0.8V	0.5V	V_{CC} −2V	4/8 mA	−400 μA
SCHOTTKY TTL	50 μA	−0.2 mA	2V	0.8V	0.5V	2.5V	20 mA	−1000 μA
ADVANCED SCHOTTKY TTL	20 mA	−0.5 mA	2V	0.8V	0.5V	V_{CC} −2V	20 mA	−2000 μA
ECL	−400 μA	0.5 μA	−1.95V	−1.63V	−1.63V	−0.92V	—	—
CMOS	1 μA	1 μA	0.7 V_{SS}	0.3 V_{SS}	0.4V	4.6V	1 TO 12 mA	1 TO 12 mA

devices will therefore be driving a minimum of 50 pF.

When you drive capacitive loads, the following rules of thumb will help you determine the delays associated with output cells of different current capability. Expect delays of 0.12 nsec/pF for a 4-mA cell, 0.24 nsec/pF for a 2-mA cell, and 0.48 nsec/pF for a 1-mA cell. Using these numbers, you can see that a 50-pF load will add 6 nsec of delay to a 4-mA driver, 12 nsec to a 2-mA driver, and 24 nsec to a 1-mA driver. These added delays mean that, although a driver may be able to meet your dc current requirements, the delays may not measure up to your timing needs. Take care, then, to match your output cell's current capability with your ac load.

In addition to adhering to the minimum and maximum voltages specified for proper logic levels, you must adhere to the requirements for maximum and minimum safe operational voltages and for maximum allowable currents. The latch-up protection circuitry found on CMOS ICs sets the limit on both positive and negative input voltage swings. If you allow an input signal to exceed the supply voltage by more than 0.7V, or to go below ground by more than 0.7V, the input protection diode will turn on. The protection diode was designed into the IC to turn on in cases such as this, but it's meant to deal only with transient signals. If the diode is on for more than a few microseconds, the circuit may be destroyed. You can add a standard resistor-diode network to the input to limit the current.

CMOS devices that operate simultaneously from different supply voltages present one of the easiest interface obstacles to overcome. You can use open-drain outputs with an external resistor tied to the voltage supply of the component you are attempting to drive. You should use external latch-up circuitry under these circumstances, because an internal latch-up diode will limit the output transition of the output cell to 0.5V above the supply voltage of your standard-cell design. You can also use a 3-state output cell to interface to a circuit that operates from a higher supply voltage; simply use the data to enable the cell or to put it into a high-impedance state. An external pullup resistor connected to the higher supply voltage will pull the signal up to the higher supply level when the cell is in the high-impedance state. The resistor must, in addition, restrict the current flow into the standard cell to a safe level.

The use of TTL parts to drive standard cells poses no special challenge, because CMOS input cells that are TTL compatible are readily available; just specify TTL-compatible input cells and the requirements for V_{IH} and V_{IL} are automatically met. Other means of interfacing TTL to CMOS include the previously mentioned pullup-resistor technique and the use of dual-function level-translator/logic gates.

CMOS's output-voltage levels present no impediment to driving TTL circuitry, but you have to exercise caution with regard to TTL current requirements. Worst-case current requirements for TTL inputs generally restrict the fan-out of CMOS gates that drive TTL gates to 10.

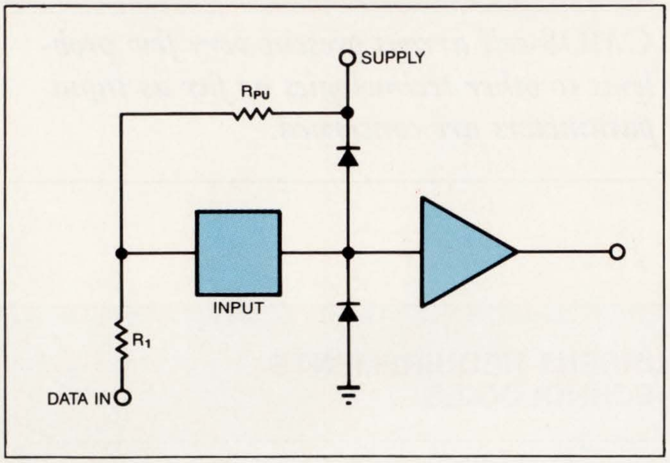

Fig 2—You can interface telecomm signals, *which operate at voltage levels of 0 and −48V, to CMOS arrays using this circuit.*

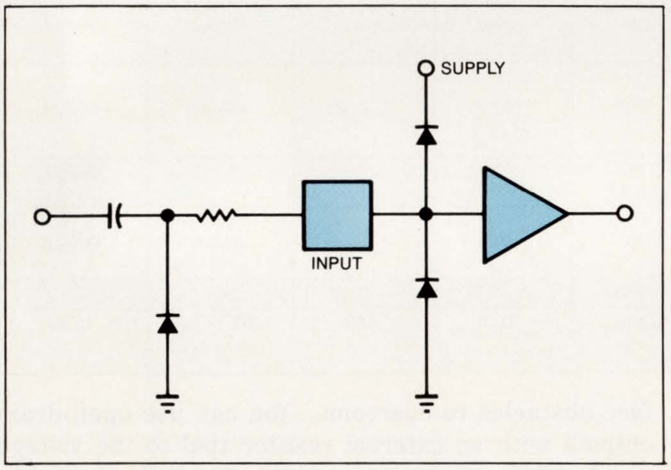

Fig 3—You can use this circuit *to drive 5V CMOS circuitry from 10V logic circuits.*

If you want to interface CMOS to ECL, you can use TTL/ECL and ECL/TTL level translators. Once you have translated an ECL signal to TTL levels, you can tie the signal directly into a TTL-compatible input cell. You can drive a TTL/ECL translator directly from a CMOS output. Once again, though, you need to be aware of the fan-out restrictions associated with this driving configuration.

Telecommunications systems offer yet another interfacing challenge to designers of CMOS-cell-based circuitry (although many of the interfacing techniques described earlier apply here as well). Telecomm equipment often employs fast bipolar circuitry and operates at logic levels of 0 and −48V. **Fig 2** illustrates a resistor-clamping diode network that allows you to interface CMOS devices to telecomm equipment.

When choosing the proper resistor values for this circuit, you must—as noted earlier—take care to prevent latch-up and ensure that the correct switching voltages are attained. To prevent latch-up, you must make sure that the input current to the array doesn't exceed 75 mA and that the interfacing circuit provides the correct switching voltages for a CMOS input—$0.3\times V_{SS}$ and $0.7\times V_{SS}$ for V_{IL} and V_{IH}, respectively. The external pullup resistor (R_{PU}) and the current-limiting resistor (R_1) act in conjunction with internal input protection diodes to accomplish the level translation and input-current protection for the input buffer.

If the input signal is at −48V (logic zero), the input protection diode clamps the voltage at the input of the gate at −0.7V. If the input signal is at 0V (logic one), the input protection diode will pull the gate voltage up towards V_{SS}. R_1 must limit the current to no more than 100 μA. Consequently, the desired value of R_1 is

$$R_1 = \frac{48V - (-0.7)}{100\ \mu A} = 473\ k\Omega .$$

You can determine the value of R_{PU} from

$$V_{IN} = V_{SS} - \frac{R_{PU}(V_{SS} - (-48V))}{R_{PU} + R_1}$$

for a logic zero and from

$$V_{IN} = V_{SS} - \frac{R_{PU}(V_{SS} - 0V)}{R_{PU} + R_1}$$

for a logic one.

For the problem of interfacing the telecomm signal to a CMOS gate, set $V_{IN}=-1V$ for the logic-one state and $V_{IN}=0.7\times V_{SS}$ for the logic-zero state. Substituting these values into the above equations yields $R_{PU}=60\ k\Omega$ and $R_1=470\ k\Omega$. These values provide the level translation and input protection needed.

You can use the circuitry shown in **Fig 3** to interface higher-voltage (10V) signals to 5V CMOS standard cells. The blocking capacitor eliminates the dc component of the incoming signal. Once the capacitor is charged, the driving circuitry pumps no more current into the input. The diodes clamp the input signal, and the resistor serves as a current limiter. **EDN**

Author's biography

Mark C Stansberry is a consultant who, since writing this article, has formed Datahouse Corp (Los Gatos, CA). In addition to conducting market research for the new concern, he does digital-logic-block and ASIC design. Mark acquired his BSEE from San Jose State University. He enjoys skiing, bicycling, wind-surfing, and illustrating in his spare time.

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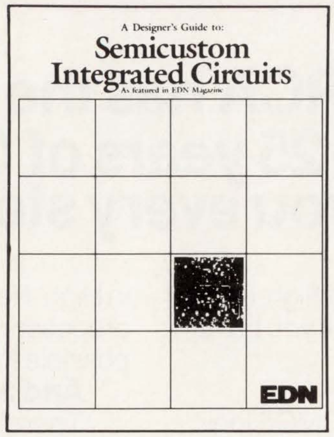

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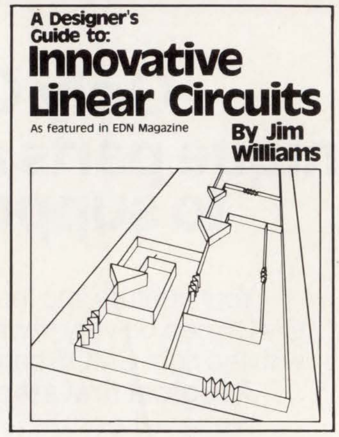

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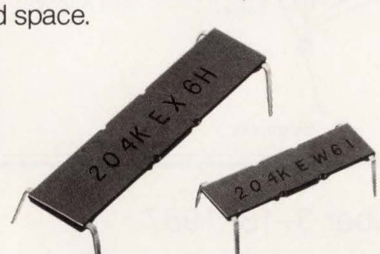

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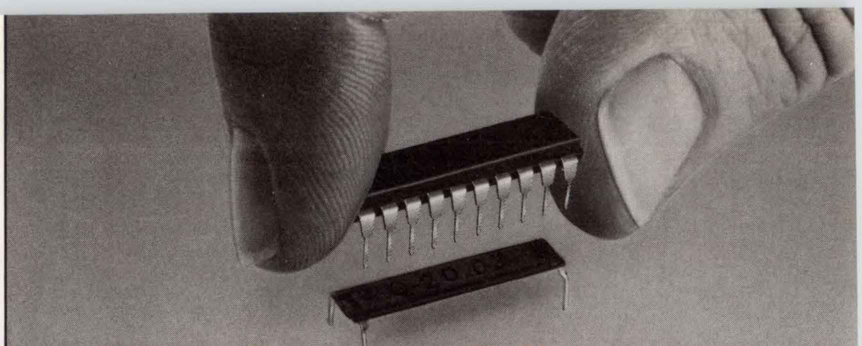

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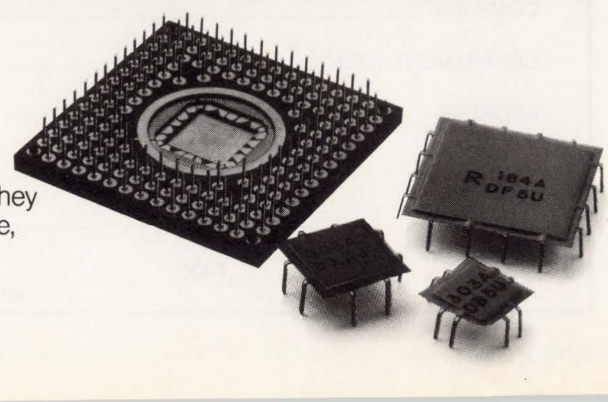

Partition custom ICs along technology lines

Implementing analog circuitry on custom ICs can be a difficult task because such circuitry often uses a wide variety of device technologies. To divide your circuitry into the functional blocks appropriate for each IC technology, you must first know your system's requirements and the strengths and weaknesses of the various technologies.

Karl J Huehne, *United Technologies Microelectronics Center*

The rapid advancements in IC technology have made it possible to consider implementing entire systems on just a few custom or semicustom chips. In such systems, it's easy enough to implement the digital functions; one popular approach is to use gate arrays. However, implementing all the other (mostly analog) circuitry on chip can be much more difficult. Unlike the digital circuits, which generally are fabricated in the same technology, the analog circuitry is often a hodgepodge of components: integrated and discrete, active and passive, MOS and bipolar.

To integrate these analog functions on chip, you must first understand both your system's requirements and the strengths and weaknesses of the various IC technologies. Then you can divide your circuitry into the functional blocks appropriate for each technology. This scheme will let you get the best possible performance out of your IC in the smallest possible space.

Your first task in developing a custom analog IC is to understand the requirements of the system it will operate in. You need to know what the system will demand of your chip, regardless of whether the circuit design is a new one or an existing one. Both these situations can pose difficulties. For example, if your task is to place an existing board-level design on a single chip, you might find that the original requirements were poorly documented and are now lost. If you're designing your chip from scratch, your system requirements will tend to change as the design evolves.

When you start with an existing design, make sure you don't fall into the trap of specifying your IC merely in terms of the existing design's individual components. This approach is the easiest one for a systems house to take, and it can make a proposed design seem like a good risk, but it doesn't take into account the fact that the original circuitry probably consists of many disparate technologies, which will be difficult to integrate on a single chip.

A more serious problem with this approach is that the board designer had access to a number of low-cost, high-performance components, a luxury you won't have when you design your IC. The high-performance components were inexpensive in discrete form, and they took up no extra space. In integrated form, however, these components would use a lot of extra space to implement functions your chip simply doesn't need.

If you're putting an existing board-level design on a chip, don't specify your IC merely in terms of the design's individual components.

Therefore, specifying integrated versions of all the components on the original board would be counterproductive.

A discrete component as mundane as a 741 op amp, for example, offers high input impedance and output short-circuit protection, two features that might not be necessary to your system, yet would require complex circuitry were you to add them to your IC. In a design that calls for a 741, you could prevent this difficulty by specifying lower input impedance for your IC, thereby simplifying the design of the input stage. Alternatively, if the output will not be required to drive anything off chip, you can just avoid including the output short-circuit-protection circuitry.

Define the requirements

Even when you're working on a new design, it's critical for you to define the overall system requirements carefully. In this case, problems can arise when the system requirements are evolving along with the design. At some point during the IC-design process, you'll have to stop and define the system requirements. Your choices of custom-IC vendor, design methodology, and IC process will all depend on the device parameters you specify at this point.

Voltage levels, both normal and maximum, will be one factor in determining what process you'll be able to use. For instance, you'll need to state in your IC specification whether your IC will have to drive high-voltage signals. If it will, you'll need to specify how: You could, for example, use open-drain or open-collector outputs. In each IC, you could incorporate a few output transistors having special characteristics, such as open drains.

Your specification should also include any voltage transients that you expect to see in your circuit. An IC must operate under well-defined bias conditions. When these conditions are violated, normal circuit operation can be disrupted and, in extreme cases, the IC can be destroyed. You can protect your IC from such problems by maintaining isolation between adjacent devices on a bipolar IC. To isolate the devices, make sure that the substrate is at the most negative voltage on the IC.

If you don't provide such external protection, a transient occurring on any IC line could drive a portion of the IC to a level more negative than that of the substrate. This condition, of course, would upset the delicate balance of the biasing scheme, and because parasitic transistors in the substrate could turn on, it could cause enough current flow to destroy the device.

Another factor you must consider is the amount of IC-performance degradation you're willing to tolerate.

IC resistors

The principle behind resistor design is that of a basic electrical parameter known as sheet resistance. The resistance from end to end of a square of material of uniform thickness and resistivity is a constant, independent of the size of the square. The resistance of a material is therefore characterized in terms of ohms per square.

When two of these squares are placed end to end (in series) between electrical contacts, the resistance between the contacts is twice the resistance that would be present if only one square were between the contacts. When two squares are placed side by side (in parallel) between electrical contacts, their resistance is half that of one square.

Approximately, then, the resistor you'll choose depends in part on the number of squares you need to use. If the base-diffusion material has a sheet resistance of 150Ω/square and you

TABLE A—TYPICAL VALUES ASSOCIATED WITH DIFFERENT TYPES OF IC RESISTORS

RESISTOR TYPE	OHMS/SQUARE	TYPICAL TOLERANCE	TC (PPM/°C)
BASE	150	25%	2000
EMITTER	5	30%	1500
E-B PINCH	5000	75%	5000
IMPLANT	1500	25%	3000
METAL	0.030	20%	6000
POLY	60	50%	1500
EPITAXIAL	1500	50%	8500
THIN FILM	1000	20%	200

You'll need to specify whether or not your device will have to operate continuously with unadulterated performance or whether the overall system can withstand some degradation on the part of your IC. If you can't relax your device's performance requirements, you may have to include thin-film or polysilicon resistors in your design. Both types of resistor offer dielectric isolation on the order of a few hundred volts but require extra process steps, which add to the cost of an IC.

Compare device technologies

One of the primary difficulties you face in recasting an existing design in silicon is that functions that aren't performed by the custom or semicustom digital ICs often use different technologies, such as MOS and bipolar technologies. Although you can mix MOS and bipolar technology on an IC, this approach is generally more expensive than using only one technology, and it often presents performance compromises, because it's difficult to optimize a process for both bipolar and MOS device performance. Standard IC products are fabricated around either the npn or the MOS transistor, but not both.

Achieving comparable performance for both device types on the same IC would require a prohibitive number of mask steps. In the mixed-technology pro-

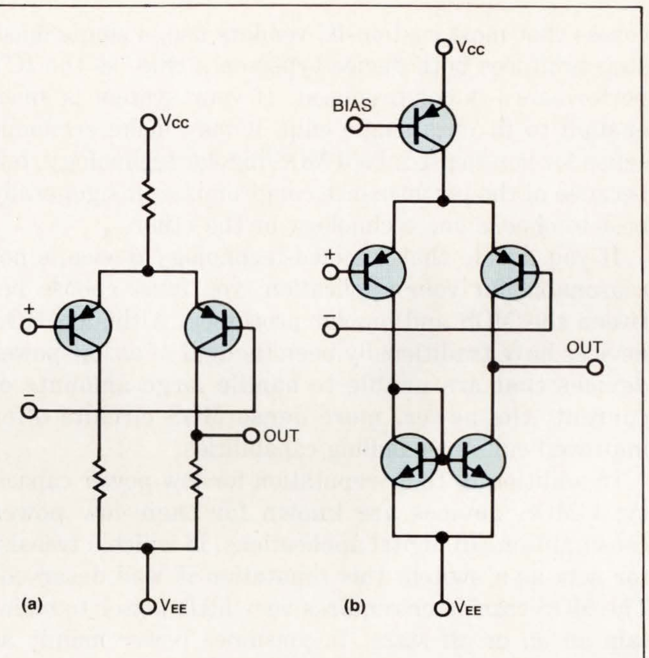

***Fig 1—Two implementations of an op amp's input stage** illustrate how an IC op amp substitutes active circuitry for passive circuitry. The discrete-component implementation **(a)** uses resistors. The integrated version of the circuit **(b)** uses transistors in place of the resistors.*

need a 1.5-kΩ resistor, the resistor will require 10 squares. To obtain a resistance of 15Ω, you'd also require 10 squares of this material, but you'd arrange it in parallel. To keep resistors to a reasonable size, you should limit the resistor values in your design to the range between 1/10 and 10 times the sheet-resistance value of the resistor material you're using.

To obtain a wide range of resistance values, you might be tempted to use a variety of resistor types: base-diffusion, base-pinch, epitaxial, and epitaxial-pinch resistors (see **Table A**). The folly of this approach is that these resistors all use different processes, which will cause undesirable differences in both the resistors' absolute accuracy and their tracking, or matching, characteristics.

The absolute tolerances of IC resistors generally range between 20 and 50%. Absolute tolerance is determined by two primary factors. The first is the sheet resistance of the material, which is determined by the doping concentration and the junction depth. The second factor, the one you have more control over, is the definition of the resistor's length and width. The accuracy of these dimensions is determined by the photolithographic tolerance. This tolerance is a fixed number, which is often on the order of a few microns.

Because the tolerance is a fixed number, you can make it as small as you like by increasing the size of the resistor. The catch is that when you make a resistor 10 times wider, thus improving its accuracy tenfold, it takes up 100 times more space, because you must increase the length by the same ratio in order to maintain the resistor value. As you can see, absolute accuracy exacts a heavy toll in IC area.

If your IC will drive high-voltage signals, you need to specify how: You could use open-drain or open-collector outputs, for example.

cesses that most custom-IC vendors use, a single mask step produces both device types on a chip, so the IC's performance is compromised. If your system is small enough to fit on a single chip, it may make economic sense for you to use mixed MOS/bipolar technology, but because of the performance compromises, it's generally best to choose one technology or the other.

If you decide that a mixed-technology device is not reasonable for your application, you must choose between the MOS and bipolar processes. Although MOS devices have traditionally been thought of as low-power devices that are unable to handle large amounts of current, the newer, more dense MOS circuits offer improved current-handling capabilities.

In addition to their reputation for low power capacity, CMOS devices are known for their low power consumption. In digital applications, in which a transistor acts as a switch, this reputation is well deserved. The MOS transistor requires very little power to maintain an on or off state. It consumes power mainly at intermediate states, when the devices are switching. If your design requires analog circuitry, you may wish to use bipolar technology, because bipolar and CMOS devices consume similar amounts of power at intermediate levels.

Analog switching or multiplexing functions are natural applications for CMOS technology, because MOS devices are inherent switches; the voltage-switching characteristics of bipolar devices aren't as good. On the other hand, bipolar voltage references are much better than MOS voltage references. If you plan on multiplexing analog signals into an A/D converter, for example, and you require an extremely accurate voltage reference, you'll want to use bipolar technology. To determine which process is most suitable for your design, you must carefully specify such switch parameters as speed, settling time, current capability, on-resistance, offset, signal-voltage levels, control-voltage levels, and isolation in the off state.

Important differences also exist between the performance of a circuit implemented in discrete components and the performance you can obtain in an equivalent IC. The designer of a board-level circuit can choose from a great number of transistors. Each of these transistors is optimized for a different characteristic, such as power, voltage, current, low noise, or frequency response. In contrast, you can't tweak an IC to improve it in one spec without making a tradeoff in another. Some variations are available to the IC designer—you can, for example, modify the geometry of a transistor—but the basic limitations of its technology still remain.

Consider the npn transistor. The current-carrying capability of an npn transistor in an IC is limited by the fact that the current is forced to travel vertically through the emitter-base junction and the collector region. Then it must travel horizontally (the buried layer provides a reduction in resistance) and then vertically again through the epitaxial layer to the collector's contact area. However, because you don't have to isolate a discrete npn transistor from other devices, its entire current flow is vertical. Therefore, virtually its entire area is available for conduction, so it can carry much more current than can an integrated npn transistor. Further, the IC transistor has additional capacitance associated with its isolation and substrate junctions, so its frequency response is limited in comparison with that of a discrete transistor.

Although devices on an IC are constrained by the fact that they all operate from the same voltage, have approximately the same operating speed, and are restricted to the same threshold voltages, placing all the devices on the same substrate does have some advantages. Because these devices are produced with the same process steps and with the same material, you can achieve extremely close parametric matching and precise scaling. You can also design multiple-collector pnp and multiple-emitter npn transistors into an IC.

From weakness comes strength

With this knowledge, you can take some of an IC design's weaknesses and turn them into strengths. For example, although the absolute accuracy of a resistor in an IC may be off by as much as 30%, you can match resistor values to a very high degree. Both active and passive devices vary in a very similar fashion in response to environmental changes, so you can take advantage of the resistor matching by designing in differential circuits whenever possible. Differential circuits are little affected by the device-parameter changes that environmental changes cause.

The traditional design philosophy, which emphasizes the use of passive rather than active components, must be completely reversed when you design with ICs. Passive devices take up much more space in silicon than do active devices, so you'll want to favor active devices over passive ones. Indeed, modern IC op amps have a relative dearth of resistors. **Fig 1,** for example, shows a simple, single-stage amplifier designed first in the traditional way, with resistors, and then in the modern way, with transistors in place of the resistors.

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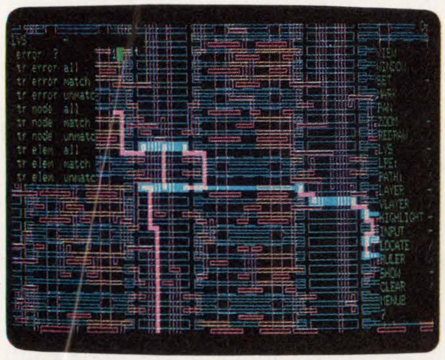

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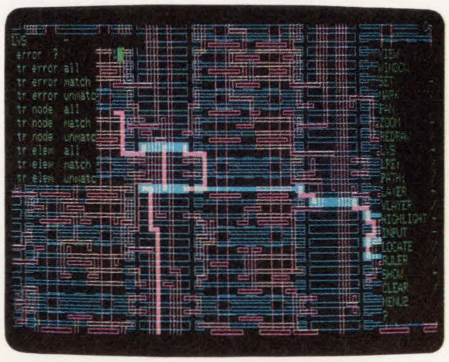

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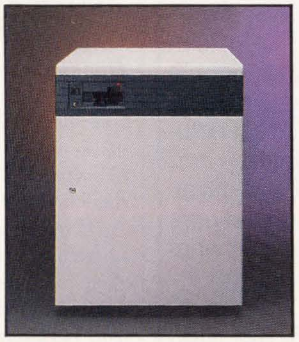

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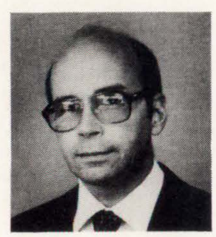
CIRCLE NO 107

Resistors play a key role in many systems. Even systems that employ active devices often have an assortment of external resistors that set threshold, gain, hysteresis, or some other performance factor. For board-level systems, very accurate resistors are readily available. For integrated design, however, the selection of resistors is limited, and the resistance values have very poor accuracies. Fortunately, many applications require only accurate ratio control, an area in which integrated resistors easily outstrip their discrete counterparts (see **box,** "IC resistors").

Just as when you choose a device technology, you face a number of tradeoffs when you choose a design methodology. Custom and semicustom approaches each have their advantages and disadvantages. A custom aproach to implementation can result in the lowest cost per IC, as long as you can amortize the higher initial nonrecurring engineering (NRE) costs of this method over a large volume of chips. Linear arrays offer a lower NRE cost, because they can incorporate some building-block functions, such as op amps. The linear array, though, has not been able to match the utility of a digital gate array, because an analog design can't be reduced to a composition of 2-input-gate equivalent cells.

Standard cells provide higher-level functions than do linear arrays, but if you use these already-defined cells, you'll be making design compromises. Furthermore, analog standard cells, like their digital counterparts, are most often available in CMOS, so the standard-cell approach is geared mainly to applications that contain a lot of digital circuitry and require only limited linear performance. **EDN**

Author's biography



When he wrote this article, Karl J Huehne was design manager of linear and smart power ICs at United Technologies Microelectronics Center. He is currently employed by Motorola Inc (Tempe, AZ), where he is design manager of telecommunications circuits. Karl obtained a BSEE from the University of Illinois and an MSEE from Arizona State University. His interests include astronomy, downhill skiing, and personal computers.

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MSA-0370	4.5	12.5	5.5	10.0	C	16.10
MSA-0420	3.5	8.5	7.0	15.0	D	18.45
MSA-0635	4.0	16.5	3.0	1.5	E	4.85
MSA-0835	6.0	23.5	3.0	12.5	E	7.80
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D) 200 mil BeO E) 100 mil ceramic

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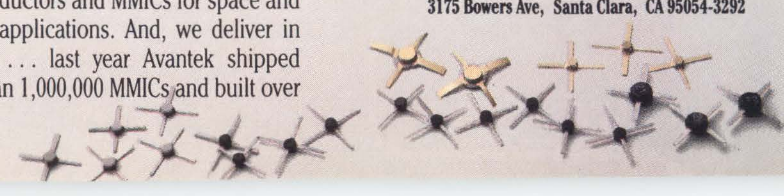

EDIF readers/writers handle data transfer between CAE systems

As you learned in the first three parts of this series, your CAE system can communicate with all CAE systems, ASIC foundries, and testers that can understand the Electronic Design Interchange Format (EDIF) data standard. To create a program that translates your system's data into and out of EDIF, get started with the simple programming steps described here in part 4.

Esther Marx, Hart Switzer, and Mike Waters,
Motorola Inc

Any CAE system can read and write data in the Electronic Design Interchange Format (EDIF)—the growing standard among CAE systems and IC vendors —if you (or the CAE-system vendor) develop the necessary software to translate that data. By using the syntax rules of EDIF, you can create rudimentary EDIF writers and readers quickly. If you need a more sophisticated EDIF writer or reader (for such tasks as silicon compilation), you can add features to the program at a later time.

The first three parts of this series (see **Refs 1, 2,** and 3) described the rules for creating character strings that render your data in EDIF—that is, they described the content of an EDIF file. The reader and writer programs effect the interface between systems that will manipulate that data.

You can write an EDIF reader or writer in any language. For example, you can find EDIF readers and writers in Fortran, Pascal, and C. Furthermore, EDIF readers and writers can run on any computer. EDIF readers and writers have been written for the Commodore 64, the Apple II, Apollo computers, DEC VAXs running VMS or Unix, Symbolics computers, and IBM CMS systems.

The recursive elements of EDIF give some languages an advantage over others. For example, a language like Lisp, which provides built-in recursion features, is easier to use than a language like Fortran. EDIF files resemble Lisp programs, particularly because EDIF and Lisp require extensive use of parentheses.

Several programs that interpret EDIF files are available to the public. (The **box** "For more information . . ." lists software that is either in the public domain or available for license.) However, although you can use one of these programs to help you develop an EDIF reader or writer, you can't simply copy a program and use it on your system. Each CAE system requires its own EDIF reader and writer, which you or your CAE vendor must develop. You should also contact the EDIF user group (below) for the most up-to-date information.

When you develop an EDIF reader, you must begin the program with a step that verifies the version and level of a file. EDIF files must begin with "edifversion" and "ediflevel" statements. The edifversion statement gives the version of EDIF that the file uses (for example, 1 0 0). The ediflevel statement specifies the level of data in a file.

EDIF lets you choose among three levels of data complexity. An ediflevel 0 file provides standard design data. In an ediflevel 1 file, you can associate parameters

You can use a public-domain program to develop an EDIF reader or writer, but you can't simply copy a program.

with your data; this level lets you scale the size of devices in a cell. Ediflevel 2 files accept program statements instead of fixed data or parameters. Because ediflevel 2 provides so much flexibility in device descriptions, you can use this level to transfer designs to and from silicon compilers.

An EDIF reader can always read levels lower than the one you have built into it. However, an EDIF reader can't read a higher level than its built-in level. For example, an ediflevel 1 reader can read ediflevel 0 and ediflevel 1 files, but it can't read ediflevel 2 files.

You can arrange to have an EDIF reader read part of the files that are at a higher level or version than you have built into the reader. To handle more advanced edifversions or ediflevels, the reader must first identify instructions that it can't understand. Then the reader issues a warning statement and saves the unread data. Although the reader can't interpret the complete file, it can usually read most of the file. In many cases, you can translate the unread data manually and create a completely readable file.

EDIF readers and writers add "user" extensions to terms that aren't in the vocabulary of the standard EDIF specification. Words with user extensions form EDIF statements that use standard EDIF syntax but have no meaning within EDIF. The recipient of an EDIF file can understand user extensions only if you make prior data-transfer arrangements. However, even when an EDIF reader can't understand a user extension in a file, it can still preserve the file—that is, it won't garble the non-EDIF content.

Obviously you'll want to be able to transfer EDIF data between incompatible computer systems. Therefore, you can't have as much flexibility in transmitting your files as you could have if you were transferring data between compatible systems. For example, many systems prefix or append characters to their files. EDIF has no control over such extra characters, so you must instruct an EDIF reader to ignore them. The reader must therefore stop translating data after it receives the close parenthesis that matches that in the opening character string, "(EDIF . . .".

Because an EDIF reader must ignore all characters that follow this final parenthesis, you can't transfer two EDIF files as a single file. What's more, an erroneous extra parenthesis will end a file prematurely. Before you transmit an EDIF file, you must verify the syntax of your file. To help prevent syntactical errors, you must include a syntax checker in your reader and writer.

The EDIF file format, which is a character stream, can also create problems for the actual data transmission. Unlike card images or 80-byte records, character streams impose no overhead or restrictions on the content of a file, but unfortunately a character stream is incompatible with some computers. Stream-oriented operating systems, such as Unix, end lines with return characters, line-feed characters, or both. Computers that store data in 80-byte records, for example, will break each stream after every 80 bytes. Most programs assume that this break is the end of a line. Since EDIF uses end-of-line characters, it can't distinguish between the two conditions.

By defining blocks so that they are all the same size, you can arrange to have your EDIF reader recognize the end of a string simply by containing it within that block and adding extra spaces to fill the block. EDIF specifies that all strings be shorter than 256 bytes, so a block greater than or equal to 256 bytes can contain any EDIF string. This technique, however, is extremely wasteful of computer storage; most strings consume much less than 255 bytes, but you must use a whole block for each string.

Instead of setting all blocks to the same length, you can simply instruct your EDIF reader to ignore all record boundaries (such as 80-character records). When translating a CAE system's file into EDIF under such conditions, you specify that your EDIF writer convert all end-of-line characters to blanks. When an EDIF

For more information . . .

For more information on EDIF, for public-copies of EDIF Version 1 1 0, or for copies of public-domain software including parsers written by the University of California at Berkeley and the University of Manchester (UK), contact the EDIF User Group, 2222 S Dobson Rd, Bldg 5, Mesa, AZ 85202.

To obtain an EDIF interpreter licensed by the University of Waterloo, contact Professor M I Elmasry, VLSI Group, Department of Electrical Engineering, University of Waterloo, Waterloo, Ontario, Canada N2L 3G1.

To obtain a public-domain EDIF interpreter developed at the University of Manchester, contact Hilary J Kahn, Department of Computer Science, The University, Manchester, M13 9PL, United Kingdom.

TABLE 1—LIST-HANDLER FUNCTIONS

GENERAL FUNCTION	SPECIFIC TASKS
LIST CONSTRUCTION	CREATE AN ATOM CREATE A LIST COPY PART OR ALL OF A LIST CONCATENATE TWO LISTS
ALTERATION OF EXISTING LIST	APPEND AN ELEMENT TO A LIST DELETE A LIST
RETRIEVAL FUNCTIONS	RETRIEVE A STRING FROM AN ATOM GET AN ELEMENT FROM A LIST GET A SERIES OF ELEMENTS FROM A LIST
QUERY FUNCTIONS	ASK IF AN ELEMENT IS AN ATOM ASK IF AN ELEMENT IS A LIST TEST ATOMS FOR EQUALITY ASK IF AN ELEMENT IS A MEMBER OF A LIST CHECK FOR EMPTY LISTS
AUXILIARY FUNCTIONS	COUNT THE NUMBER OF ELEMENTS IN A LIST COMPARE TWO LISTS DISPLAY THE DIFFERENCES BETWEEN TWO LISTS DELETE AN ATOM READ A LIST WRITE A LIST

reader receives a file, the reader restores the line feeds by converting all blanks to end-of-line characters. It makes no difference to EDIF syntax whether your character strings use line feeds or blanks. Right now, all EDIF readers use the technique of ignoring record boundaries. You can insert an end-of-line character by writing it in ASCII code if required, but as implied above, you don't need an end-of-line character in an EDIF file.

Some computers control files with periods and commas. In serial transmissions, moreover, many systems add extra characters that don't produce printed output. Most computers have a transparent mode, which sends data unchanged, but even transparent modes usually require extra characters for special file-handling procedures. Some high-security systems don't let you transmit binary files. Furthermore, different machines often use different binary codes for the same characters. In short, despite the existence of the ASCII standard, many character codes vary from machine to machine.

What's more, many systems can't read the full ASCII character set. In fact, the only universal characters are the 26 letters of the upper-case alphabet and the 10 digits. Because EDIF must run on all systems in order to be of maximum benefit, the format can use only a subset of the ASCII character set. All modern computer systems understand the subset of ASCII that EDIF does use.

Some older systems, however, can't even handle the EDIF subset of ASCII. You then have to translate one EDIF character into several system characters (such as an underscore to "+U"). As long as you translate each EDIF character into a unique character string, you can use older computer systems. You should assign a printable representation to every EDIF character, so that you can debug your files easily.

Your program must remove all the non-EDIF characters that a computer system adds to a file. While your software is removing the non-EDIF characters, it can also delete extra blanks, tabs, and line feeds.

You should certainly make your EDIF reader as generic as possible to ensure a clean transfer of data between dissimilar systems, but remember that EDIF itself doesn't provide any special capabilities for data transmission. To transfer data via a LAN or modem, you must establish or adopt existing network or file-transfer standards.

Although EDIF doesn't specifically handle data-transmission problems, you can transfer data only if you resolve such problems. For example, EDIF doesn't provide data-error checking or parity checking. If you need these functions, you must add them yourself to your system's protocol-handling facility.

Once you have solved all the problems of structuring an EDIF reader or writer, you can develop the actual code. As you have seen in the earlier articles in this series, EDIF files consist of symbolic expressions enclosed by parentheses. In EDIF, these expressions are called lists. A list handler can simplify an EDIF-file reader or writer.

A list handler insulates users from the data structure and operations of EDIF. For example, a list handler places parentheses around lists, and users shouldn't have to count parentheses. A list handler also takes care of such chores as input, output, data-structure definition, and character-string manipulation.

Table 1 lists the functions that you must include in a list handler. Some of these functions are necessarily only for readers; other functions are specific to writers. A list handler that's a part of a reader only or a writer only doesn't, of course, need to include all of these functions. For example, an EDIF writer's list handler doesn't need the retrieval and logical operations a reader requires. A file reader's list handler, on the other hand, doesn't need the list-building functions a writer uses.

To create a simple list handler for a file writer, for example, you need the functions "create an atom," "create a list," "append an element to a list," and "write a list." Using these functions, your list handler can write such EDIF statements as

```
(DESIGN MOTO2500
    (QUALIFY MOTO2500_LIBRARY MOTO2500_CELL)).
```

This list contains two atoms and another list, which

You can arrange to have an EDIF reader read files that are at a higher level or version than you have built into the reader.

contains three atoms. To create the larger list, your writer must first specify the atoms. These atoms are

```
DESIGN ← CREATE THE ATOM 'DESIGN'
DESIGNAME ← CREATE THE ATOM 'MOTO2500'
QUALIFY ← CREATE THE ATOM 'QUALIFY'
LIBRARYNAME ← CREATE THE ATOM 'MOTO2500_LIBRARY'
CELLNAME ← CREATE THE ATOM 'MOTO2500_CELL'.
```

Next, the list handler must create the "qualify_list":

```
QUALIFY_LIST ← CREATE A LIST.
```

The list handler then appends the keywords "qualify", "libraryname", and "cellname" to the qualify_list. It then creates the "design_list" and appends the remaining atoms to the design_list:

```
APPEND QUALIFY TO QUALIFY_LIST
APPEND LIBRARYNAME TO QUALIFY_LIST
APPEND CELLNAME TO QUALIFY_LIST.

DESIGN_LIST ← CREATE A LIST
APPEND DESIGN TO DESIGN_LIST
APPEND DESIGNAME TO DESIGN_LIST.
```

The list handler completes the statement by appending the qualify_list to the design_list and then writing the file:

```
APPEND QUALIFY_LIST TO DESIGN_LIST
WRITE DESIGN_LIST TO OUTPUT FILE.
```

LISTING 1—INSERTING AN ELEMENT IN A LIST

```
SUBROUTINE INSERT__BEFORE (LIST, ELEMENT, NEW__ELEMENT)
 If ELEMENT is a member of LIST then
    Create NEW__LIST
    N ← 1
    while not ELEMENTS__EQUAL (ELEMENT, Nth element of LIST)
        append Nth element of LIST to NEW__LIST
        N ← N+1
    append NEW ELEMENT to NEW__LIST
    append Nth element of LIST to NEW__LIST
    concatenate NEW__LIST and all elements of LIST after Nth element
    LIST ← NEW__LIST

 else
    print error message


FUNCTION ELEMENTS__EQUAL (ELEMENT1, ELEMENT2)

ELEMENTS__EQUAL ← false
If ELEMENT1 is an atom and ELEMENT2 is an atom
   ELEMENTS__EQUAL ← condition of ELEMENT1 equal to ELEMENT2
If ELEMENT1 is a list and ELEMENT2 is a list
   ELEMENTS__EQUAL ← condition of difference between ELEMENT1
                              and ELEMENT2
```

By creating the atoms before creating the list, the list handler saves storage space. Instead of forming a keyword each time you use it, you can store the keyword and call it as often as you need it.

EDIF readers check syntax and read files

You can develop a list handler for an EDIF reader in the same way that you create a writer. To read the list that you just created, your reader must perform six of the tasks given in **Table 1:** "create an atom," "get an element from a list," "ask if an element is a list," "test atoms for equality," "count the number of elements in a list," and "read a list."

Your reader must first identify the atoms that it's reading. It then verifies that the sequence of atoms in the list obeys EDIF syntactical rules:

```
DESIGN ← CREATE THE ATOM 'DESIGN'
QUALIFY ← CREATE THE ATOM 'QUALIFY'.
```

On the basis of this verification procedure, the reader confirms that it's reading a list:

```
IS_LIST ← TRUE IF A LIST; IF FALSE, ABORT.
```

The reader then checks to see that the design statement contains two atoms and a 3-atom list, as EDIF requires.

```
HEAD_OF_LIST = DESIGN? ← IF FALSE, ABORT
LENGTH_OF_LIST = 3? ← IF FALSE, ABORT
IS_LIST (THIRD ELEMENT)? ← IF FALSE, ABORT
LENGTH_OF_LIST (THIRD ELEMENT) = 3? ← IF FALSE, ABORT.
```

Finally, the EDIF reader reads the statement. The reader looks for "design_name" in the second atom of the design statement, and then it looks for "libraryname" and "cellname" in the third element of the design statement.

You can, of course, add other capabilities to your reader. **Listing 1,** for example, shows the code that enables a reader to insert an element in a list before the *n*th element.

After you complete your EDIF program, you should test it by actually using it. If you can transfer a file to another user and he can interpret the information correctly, then your program works reliably. Wherever possible, you should write both an EDIF reader and an EDIF writer, so you can test your programs against each other for consistency.

To verify your program adequately, you need a

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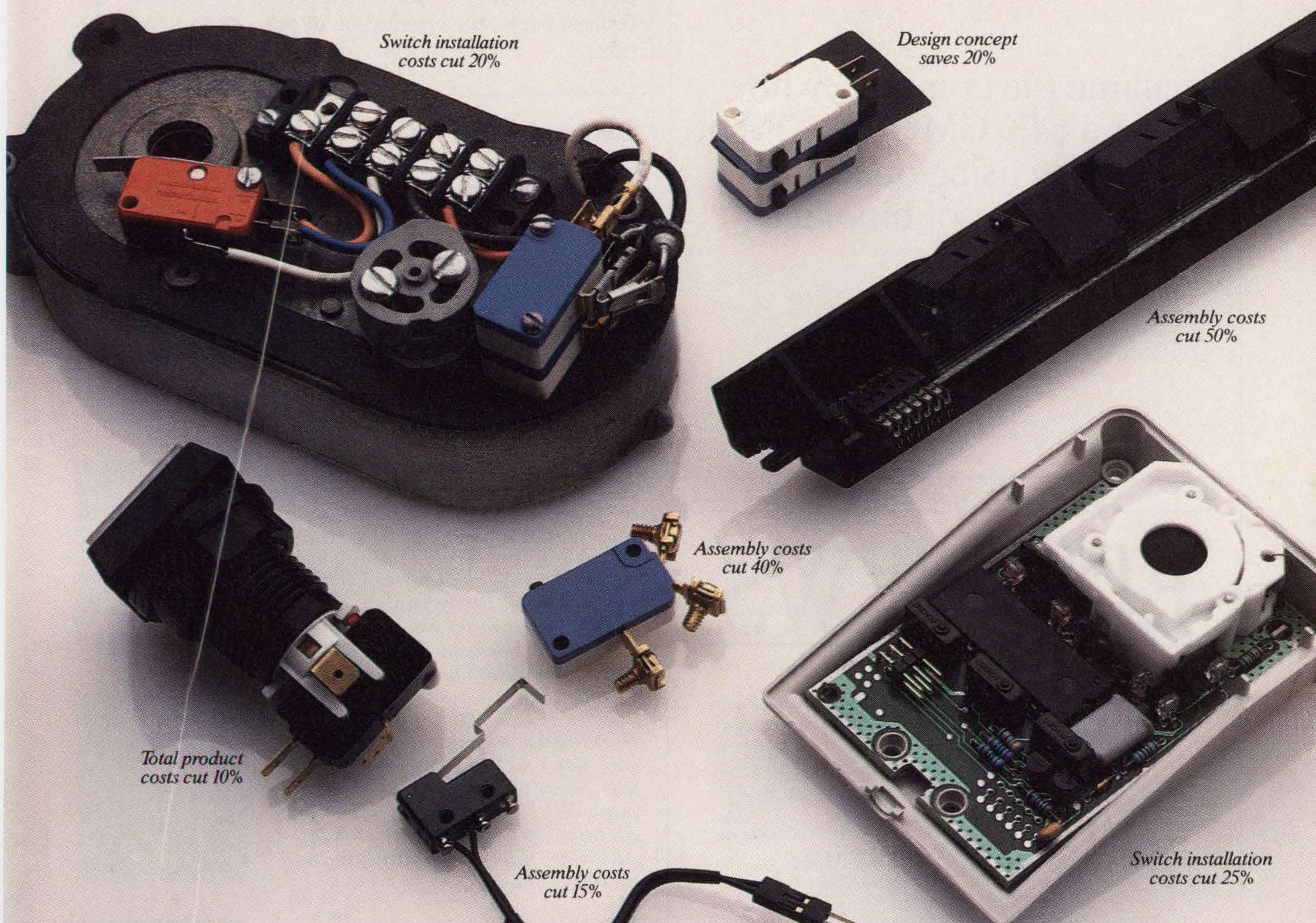

Take the long black strip of switches for example. It was the result of working together with a gaming machine manufacturer who needed to lower the cost of their product.

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(See page 210.)

plotting package that accepts EDIF. The plotting package can be a fairly unsophisticated program, but the program should be able to interpret cell-protection frames, ports, the orientation of cells, and interconnections. **EDN**

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1. Marx, Esther, Hart Switzer, and Mike Waters, "EDIF format brings uniformity to CAE/CAD data," *EDN*, January 22, 1987, pg 153.
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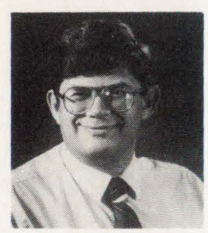
Authors' biographies

Esther Marx is a senior software engineer at Motorola Semiconductor Product Sector's ASIC Division (Mesa, AZ). She received an MS from George Washington University (Washington, DC) and a BA from Oberlin College (Oberlin, OH). Before joining Motorola, Esther served for five years in the Air Force. She enjoys writing science fiction and collecting Star Trek memorabilia.

Hart Switzer is a software engineer with Motorola Semiconductor Products, where she designs and implements EDIF software. She received a BS from Stanford University (Palo Alto, CA). Hart enjoys gardening and collecting antiques.



Mike Waters is a principal engineer and EDIF project manager at Motorola Semiconductor Products. He received a BS in computer science from Regent's College (New York, NY). Mike likes to exchange ideas with other EDN readers via his ham radio (license AA4MW) or his amateur packet radio.

Article Interest Quotient (Circle One)
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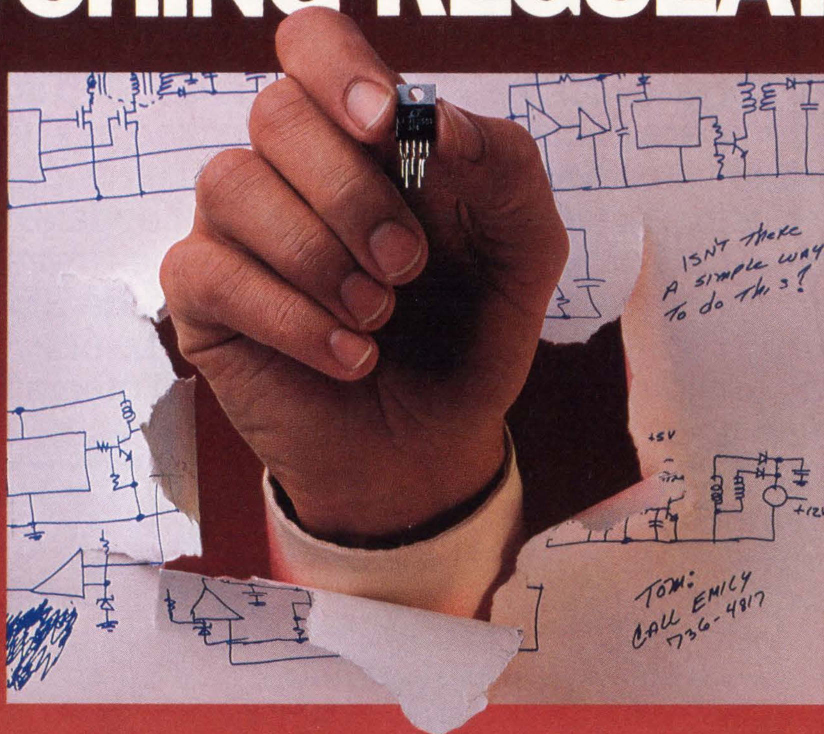
A REAL BREAKTHROUGH IN SWITCHING REGULATORS.



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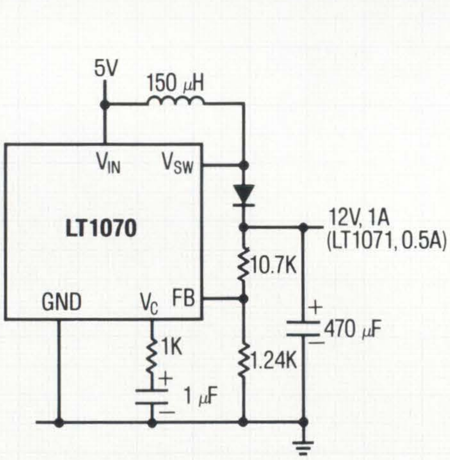

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Take the sweat out of switching regulator design with the new LTC1070/71/72 family. Pricing for LT1070CT is $7.45 each in quantities of 100 (LT1071CT is $5.70 ea./100). The LT1072 will be available in the first quarter of 1987. For additional technical details, contact: LINEAR TECHNOLOGY CORPORATION, 1630 McCarthy Blvd. Milpitas, CA 95035. (408) 942-0810.

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Linear load dissipates constant power

Horace T Jones
Penril Datacomm, Gaithersburg, MD

The **Fig 1** circuit presents a constant-power load to the input voltage V_{IN}. For the component values shown, the circuit provides a 4W load at a nominal V_{IN} of 13V and maintains this power level within ±0.2% for input voltages of 9 to 17V. Potentiometer R_{10} lets you adjust the constant-power level.

Select R_4 and R_5 to produce a voltage $V_{CONTROL}$ of approximately 6V at the inverting input of IC_{1A}. Op amps IC_{1A} and IC_2 form a pulse-width modulator whose output duty cycle (X) is a linear function of V_{IN} (X equals $V_{CONTROL}/V_{CC}$). The modulator's nominal 33-kHz operating frequency (f) decreases as V_{IN} varies above or below its nominal value:

$$f=\frac{X\cdot R_3(1-X)}{R_2R_1C_1}.$$

The modulator's output signal (pin 6 of IC_2) drives the analog switch IC_3, which in turn drives the linear current source formed by op amp IC_{1B} and MOSFET Q_1. Consequently, I_{IN} is inversely proportional to V_{IN}, so the load power P_{IN} is constant:

$$P_{IN}=V_{IN}I_{IN}=\frac{V_{CC}V_{REF}}{R_{11}}\left[1+\frac{R_4}{R_5}\right].$$

Filter components R_8 and C_3 suppress voltage ripple introduced by the switching action of IC_3. This switching action also limits the control loop's 3-dB bandwidth to about 480 Hz. **EDN**

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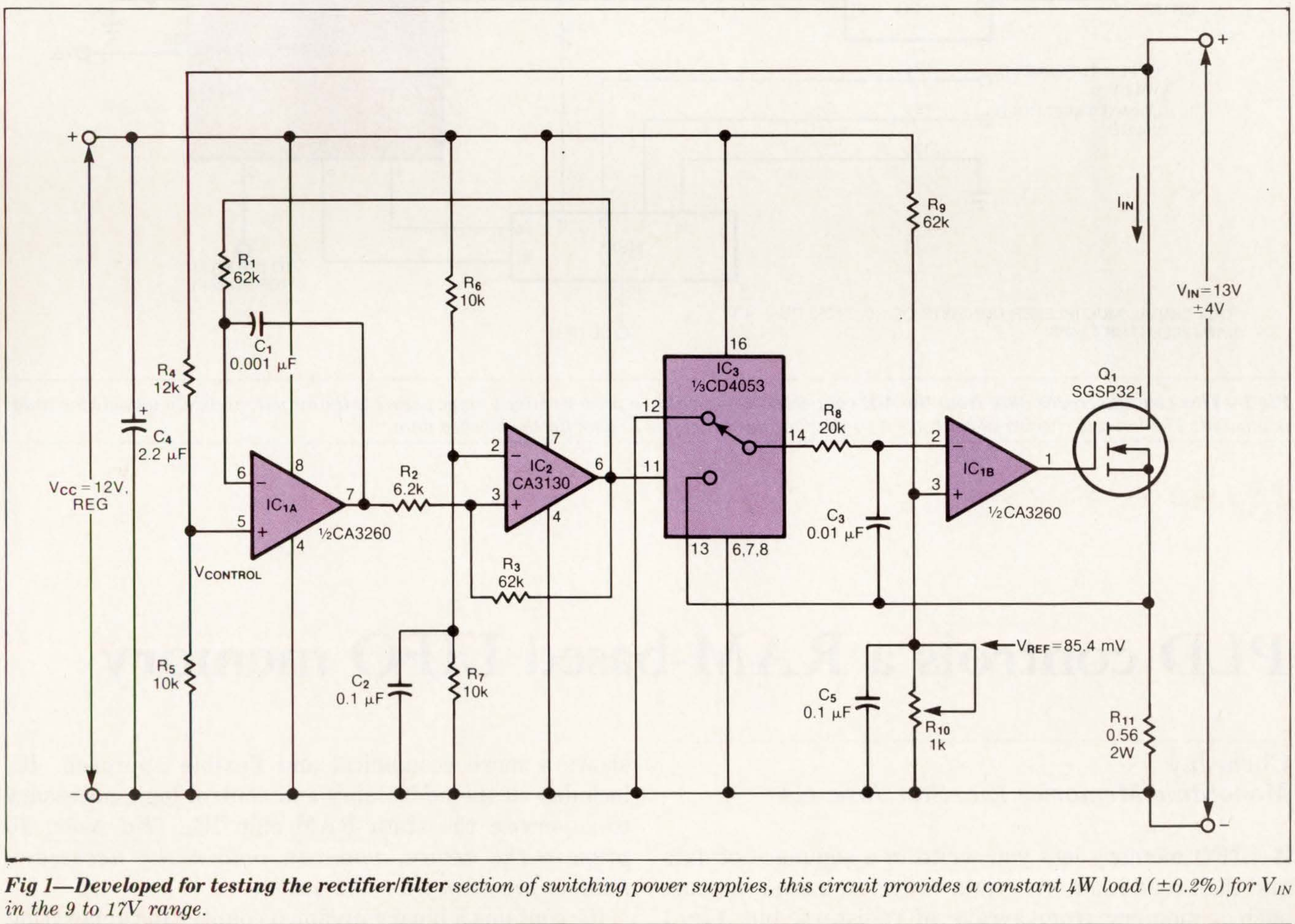


Fig 1—Developed for testing the rectifier/filter section of switching power supplies, this circuit provides a constant 4W load (±0.2%) for V_{IN} in the 9 to 17V range.

Bounds checker has DSP applications

Brian Case
Advanced Micro Devices, Sunnyvale, CA

Fig 1's circuit dynamically limits the range of 12-bit data at the front end of a digital signal-processing system. The bounds checker (IC_2) contains a separate 16-bit register/comparator combination for the upper and lower thresholds. You store the desired values in IC_2 via the data bus; the chip then compares the A/D converter's output D with each threshold.

The outputs CO_L (low when D≤lower threshold) and CO_U (low when D≥upper threshold) control a 12-bit, 4:1 digital multiplexer. Accordingly, the multiplexer passes to its output one of the following values: the lower threshold value, the upper value, or, when D is within bounds, the A/D converter's output. The bounds checker can handle signed or unsigned numbers (pin 28 high or low, respectively). Similarly, different connections to pins 14 and 15 configure the device for various types of threshold comparisons ("greater than" vs "greater than or equal to," for example).

By connecting a counter to IC_2's out-of-bounds output (pin 6), you can tally the number of A/D conversions outside the desired range. By connecting the converter output to several bounds-checker/counter combinations in parallel, you can create a histogram of the converter's output data. **EDN**

To Vote For This Design, Circle No 749

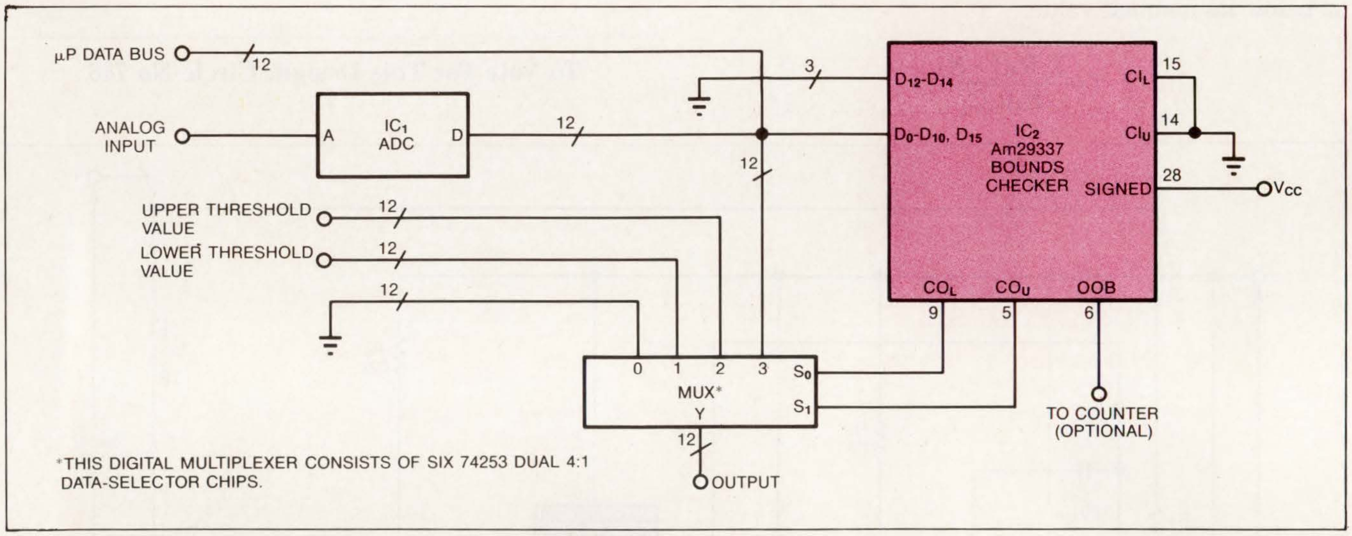


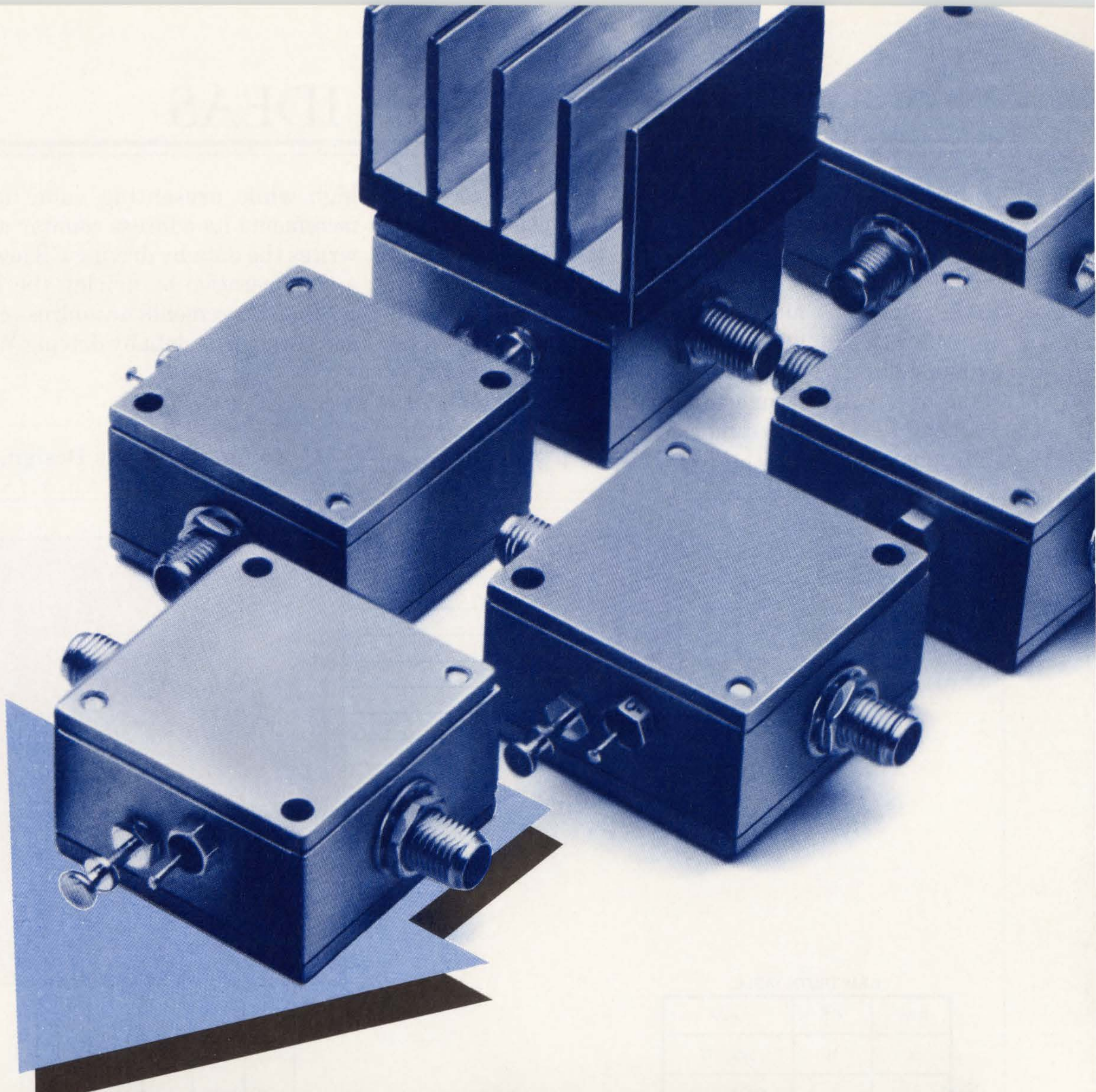
Fig 1—This circuit screens data from the A/D converter. *Data within a predetermined range passes to the output, and data outside the range is blocked. The bounds checker substitutes an upper or lower threshold value for the blocked data.*

PLD controls a RAM-based LIFO memory

Chris Jay
Monolithic Memories Inc, San Jose, CA

A LIFO memory lets you write in a sequence of data and then read it out in reverse order. You can construct such a memory from arrays of registers, but **Fig 1** shows a more economical and flexible approach. IC_1 includes all the addressing and control logic necessary to supervise the static-RAM chip IC_2. *(Ed Note: To prepare the device, you can obtain the necessary Palasm program from the author.)*

IC_1 contains a binary up/down counter for generating



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addresses and a state-machine sequencer for controlling write or read operations during active push (write) or pop (read) cycles. The 2k-byte×8-bit RAM gives you a 2-chip, 128-byte×8-bit LIFO memory, and additional RAM chips in parallel can expand the LIFO memory to 16, 24, or 32 bits wide. Unused address lines should be grounded, but if you want to build a deeper LIFO structure, you can connect those unused address lines to a second device, programmed as a cascadable counter.

To push data onto the LIFO, drive IC_1's Push input high while presenting valid data to the RAM. IC_1 increments its address counter and sets $\overline{WR}$ low, then writes the data by driving $\overline{CS}$ low **(Fig 2a)**. You initiate a pop operation by driving the PAL's Pop input high. IC_1 then decrements its address counter, drives $\overline{CS}$ low, and obtains the data by driving $\overline{WR}$ high **(Fig 2b)**. **EDN**

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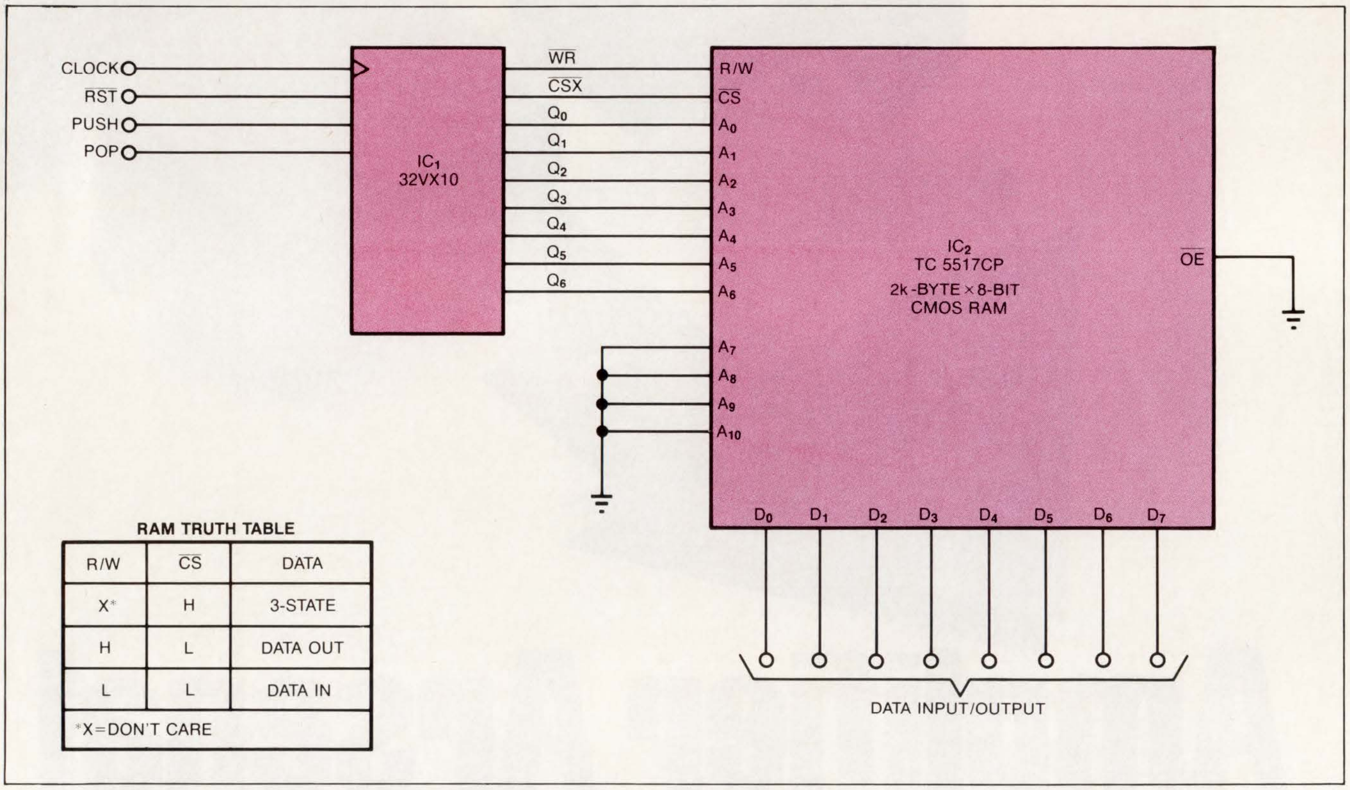

RAM TRUTH TABLE

R/W	$\overline{CS}$	DATA
X*	H	3-STATE
H	L	DATA OUT
L	L	DATA IN

*X=DON'T CARE

Fig 1—This 2-chip, 128-byte×8-bit LIFO memory *consists of just a CMOS RAM chip and a controller chip.*

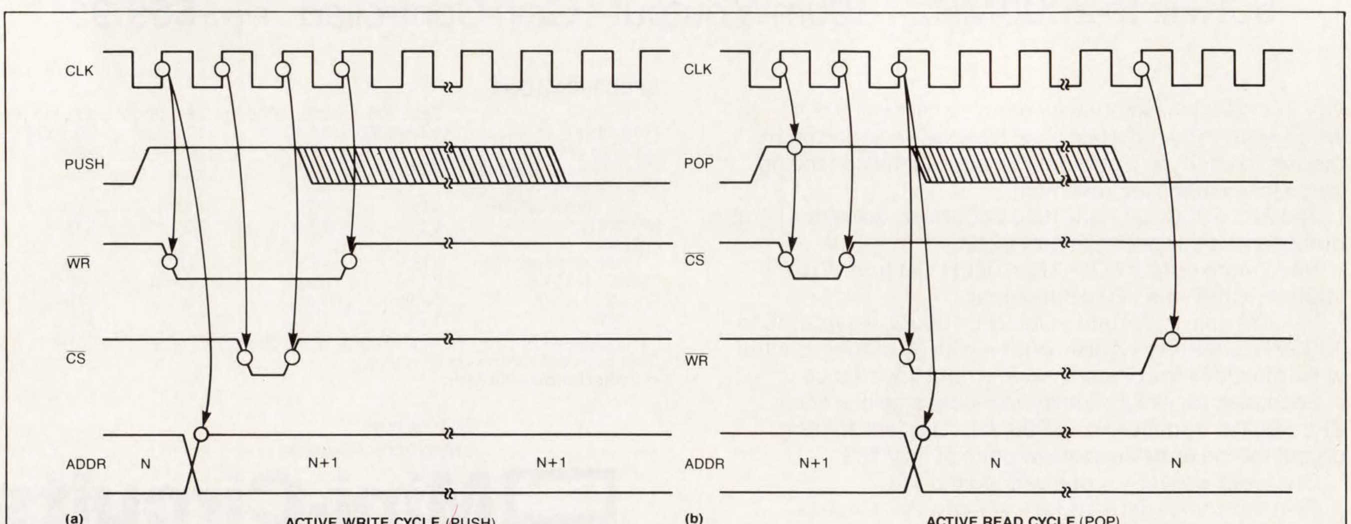

Fig 2—These diagrams illustrate the control-timing *relationships for push and pop operations in the **Fig 1** circuit.*

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Registers	272 byte general-purpose, 53 mode/control	230 byte general-purpose, 26 mode/control	32 byte general-purpose, 26 mode/control, 224 Indirect RAM
External Memory	up to 128K of RAM or ROM	up to 64K of RAM or ROM	up to 64K of RAM or ROM
DMA	Single-channel with 16-bit pointer and count register	None	None
I/O Lines	40 programmable with 2 handshake channels	26 programmable 12 fixed input 2 fixed output	32 programmable
Counter/Timers	3 16-bit: 2 up/down-count with bivalue and capture modes, 1 down count only	2 16-bit up-count only with 4 high-speed input units	3 16-bit up-count only
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Steve Lubs
Department of Defense, Washington, DC

Bypassing the multiplier section of a multiplier-accumulator (MAC) chip lets you form a flexible counter or divider. In this example, the TDC1008J MAC saves circuit-board area by replacing four or five cascaded counters and associated circuitry.

Tie the LSB of one input port (port Y in this example) to logical one, and tie the remaining Y port

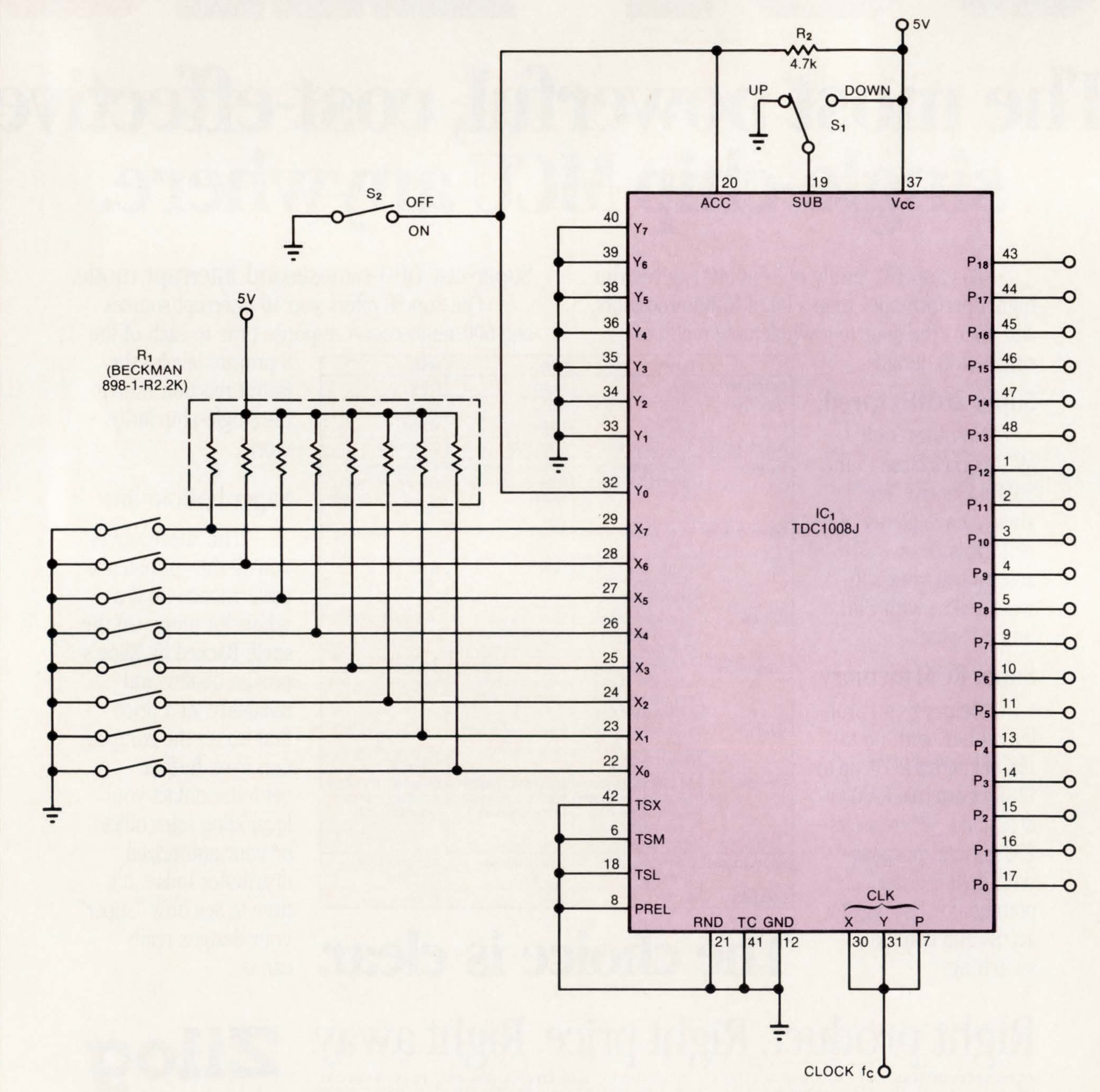

***Fig 1—This multiplier-accumulator chip** can serve as a counter or divider when you bypass its multiplier section.*

You're not gambling with quality when you buy low-cost T70 relays from P&B.

Quality at just 77 cents

UL recognized and CSA certified, Potter & Brumfield's T70 relay switches from 1 milliamp through 10 amps, resistive, on printed circuit boards. All with the same reliability and performance that have made P&B relays the industry standard. And the T70 costs as little as 77 cents in 25,000 piece quantities.

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With 20 different T70 models available from stock at P&B, the unit you need is probably available off-the-shelf. Your P&B distributor or sales representative will gladly help you select the model that's just right for your application. Call toll-free 1-800-255-2550 for the name of an authorized Potter & Brumfield distributor or sales representative serving your area. Or call your P&B regional office.

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Potter & Brumfield Inc., 200 S. Richland Creek Dr., Princeton, IN 47671-0001

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Title

EDN 3487

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Potter & Brumfield A Siemens Company

CIRCLE NO 100

bits to logical zero. Apply an 8-bit digital value M to the other input port (port X in this example). The resulting frequency f_{OUT} on any of the 19 output pins (P_N) is

$$f_{OUT} = \frac{Mf_C}{2^{N+1}}.$$

This circuit accepts values of M from 1 to 255 and f_C to 15 MHz. For higher clock rates, you should select a CMOS MAC. Different combinations of M and P_N provide a wide range of clock frequencies.

Alternatively, you can use all of the output pins or a subset of them as a counter that counts in units of M. Switch S_1 sets the count direction. Note that, following closure of S_2, the chip requires two rising edges of the clock before it loads the output register (**Fig 2**). **EDN**

To Vote For This Design, Circle No 748

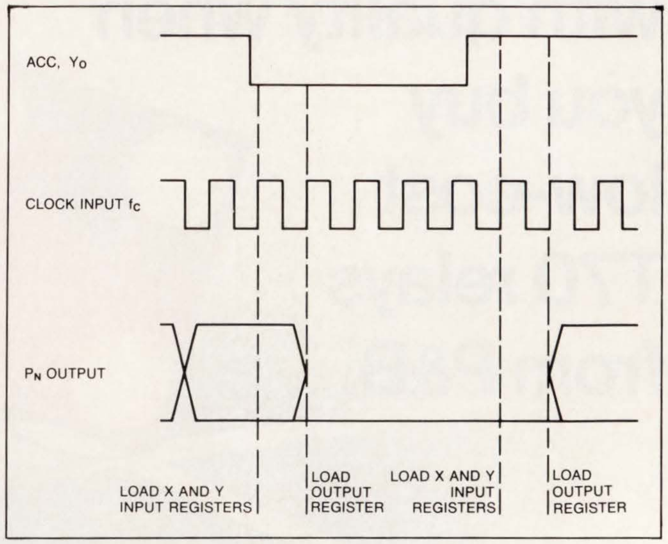

***Fig 2—The multiplier-accumulator chip requires two rising edges of f_C** in order to clear before it loads the output register.*

Pulse-delay circuit has dual-edge trigger

S Murugesan
ISRO Satellite Centre, Bangalore, India

In **Fig 1,** a single monostable multivibrator delays a pulse train by a variable amount; nonetheless, this amount can be no less than the minimum allowed pulse width t_W. This approach simplifies an earlier Design Idea (EDN, June 26, 1986, pg 225) by lowering the parts count.

The exclusive-OR gate IC_1 generates a short pulse following every leading or falling edge of the input waveform. These pulses cause one-shot IC_2 to produce a negative-going pulse with a duration equal to the desired time delay t_D, which you set by adjusting the potentiometer (R). Flip-flop IC_3 then creates a delayed replica of the input pulse by latching the $\overline{Q}_1$ output of IC_2 between positive-going transitions. You can independently control the output-pulse duration by cascading a second one-shot with the first. **EDN**

To Vote For This Design, Circle No 747

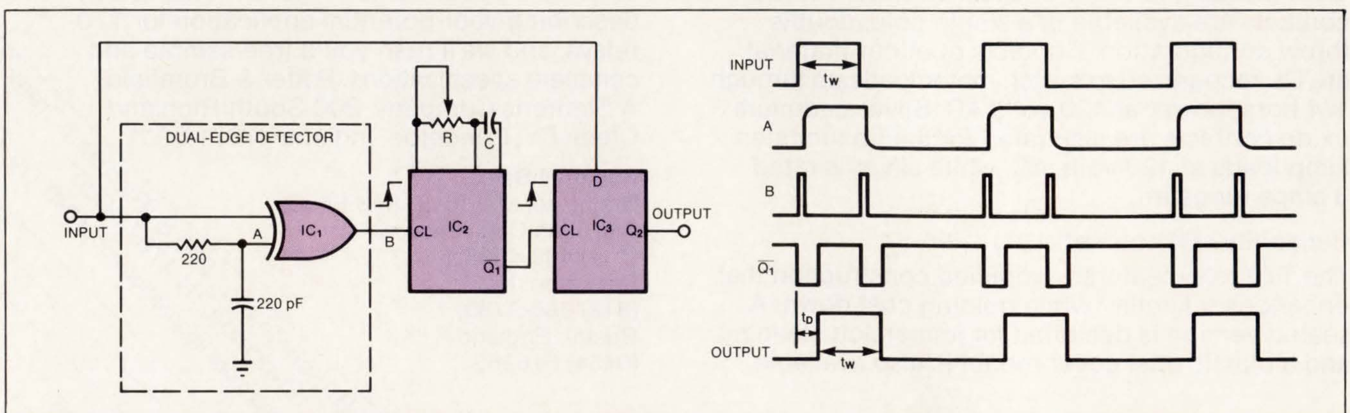

***Fig 1—This circuit delays the input pulse train** by a time interval t_D, which is less than or equal to the minimum pulse width t_W.*

Ah, the big idea. Everyone has one. But not everyone can afford a plotter to plot one on. Which got us thinking. What if there was an HP quality plotter so reasonably priced you could afford to hook one up to every PC CAD workstation in the office?

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The drawing shown below was produced on the HP DraftPro with VersaCAD software.

HEWLETT PACKARD

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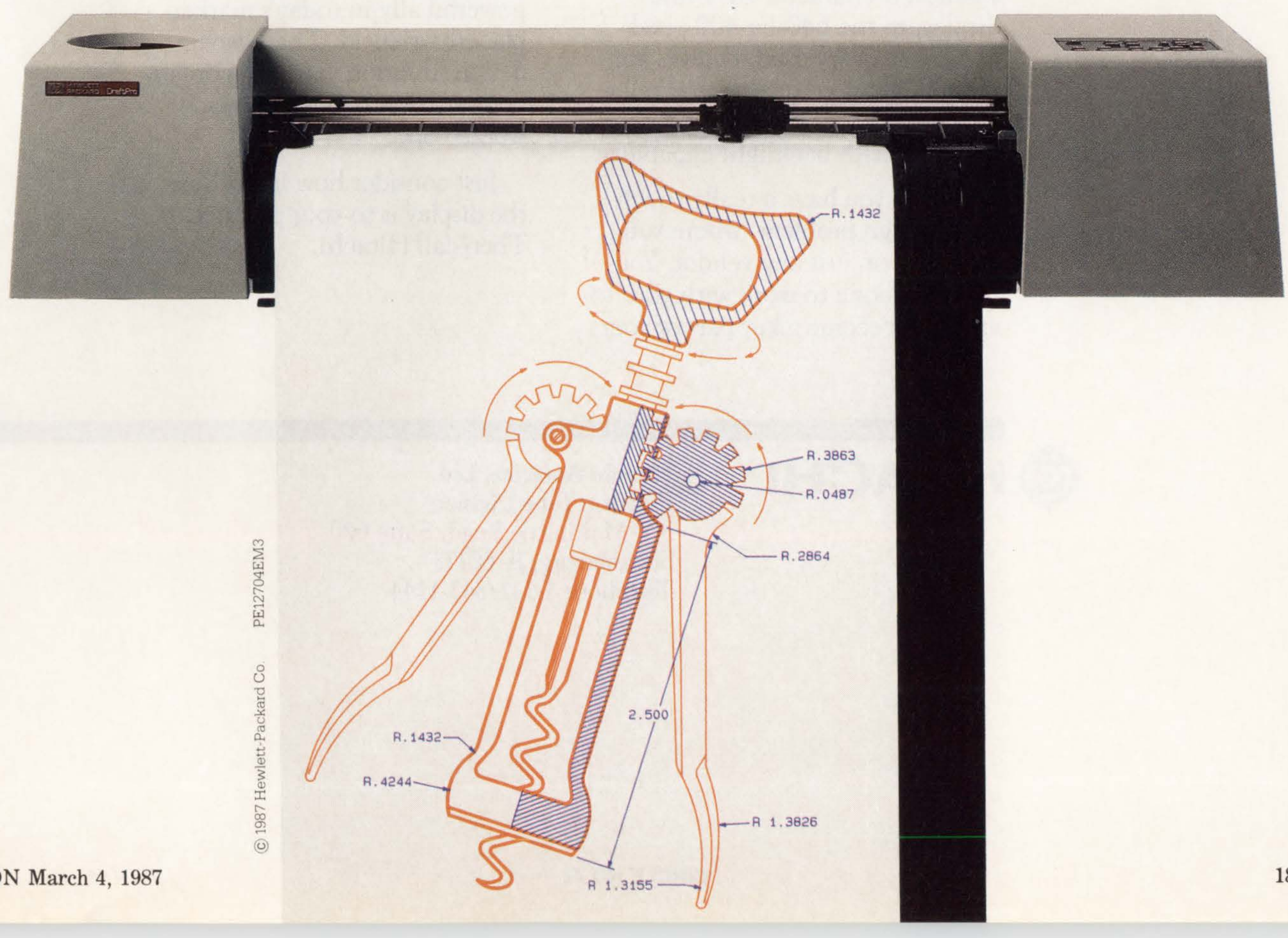
CIRCLE NO 79

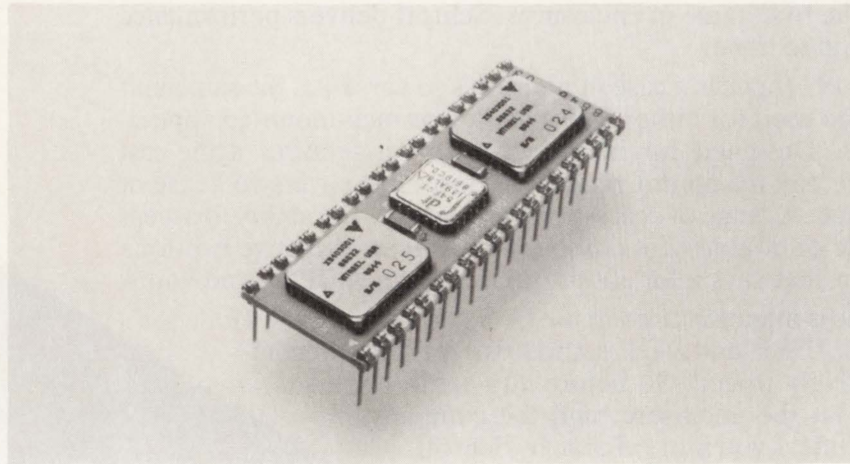
How to pull off a fantastic HP plot for only $5400.



INTEGRATED CIRCUITS

MEMORY MODULE

- *Contains multiple static-RAM chips*
- *100-nsec access time is standard*



Suitable for space-sensitive military applications, the 1M-byte VMS-10A24 memory module comes in commercial and military (MIL-STD-883, Class B and S) versions having access times of 100, 150, or 200 nsec. The device includes four 32k×8-bit static RAMs in DIPs, decoder circuitry, and decoupling capacitors, all of which are mounted on the top and bottom surfaces of a 40-pin ceramic substrate with a standard JEDEC pinout. Normally configured as 64k×16 bits, the module also comes as a 64k×8-bit or a 128k×8-bit device. An EEPROM version is also planned. VMS10A24S-150C, $350; -150B, $510.

Vitarel Microelectronics Inc, 3572 Corporate Ct, San Diego, CA 92123. Phone (619) 292-8353.

Circle No 351

32-BIT μP

- *Has mathematically proven design for enhanced reliability*
- *Automatically halts when internal errors are detected*

The Viper μP is targeted for use in safety-critical applications. Its design is mathematically verifiable at gate level to ensure consistent performance. The processor operates on 32-bit data, and it has 20-bit addressing and an additional control output to divide memory operations from I/O operations. It includes three 32-bit general-purpose registers and a single-bit condition code register. Registers for indexed addressing are automatically checked for overflow beyond the μP's 20-bit address capability. The instruction set is deliberately limited to 16 ALU instructions and 16 comparison operations to avoid ambiguity in the interpretation of each function. An illegal output from the ALU or an invalid address automatically halts the processor. The μP doesn't have any interrupt capability or any support for a hardware stack because both of these are unacceptable sources of program failure in safety-critical systems. Fabricated in 5V CMOS, it costs £250.

Marconi Electronic Devices Ltd, IC Div, Doddington Rd, Lincoln LN6 3LF, UK. Phone (0522) 688121. TLX 56380.

Circle No 352

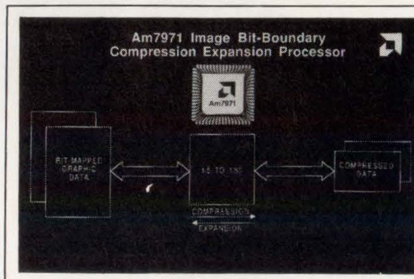
Marconi Electronic Devices Inc, 80 Smith St, Farmingdale, NY 11735. Phone (516) 420-8378.

Circle No 405

COMPANDER IC

- *Processes documents to nearest bit or pixel*
- *Achieves 30:1 compression ratio*

This 1-chip compression/expansion processor allows you to process documents for transmission to the nearest bit or pixel. Model Am7971 is an intelligent processor that achieves typical compression ratios of 30:1. It contains two programmable registers for bit-boundary control. The device compresses and expands 2-tone, bit-mapped documents in ac-



cordance with CCITT recommendations T.4 and T.6 for Groups III and IV facsimile equipment. Its coding options are 1-dimensional modified-Huffman run-length coding, and 2-dimensional modified-Read relative coding. The chip can operate in line-by-line, fractional, and full-page modes. Equipped with an on-chip error-detection mechanism, the device detects all possible data corruptions by checking for illegal codes, negative run lengths, and incorrect line lengths. The IC operates at 5 MHz. Prices for devices in 68-lead PLCCs and LCCs are $119.05 and $142.86 (100), respectively.

Advanced Micro Devices Inc, Box 3453, Sunnyvale, CA 94088. Phone (408) 982-7445.

Circle No 353

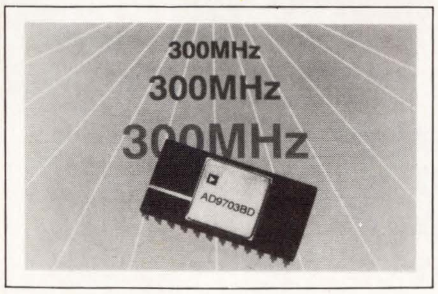
DATA ACQUISITION

- *Data-acquisition system comes in a 40-pin DIP*
- *Includes software-programmable instrumentation amp*

The HS9414 is a self-contained, 12-bit data-acquisition system in a 2.1×0.8-in., 40-pin DIP module. It includes a 4-channel, differential-input multiplexer and an instrumentation amplifier (IA) that has digitally programmable gains of 1, 10, 100, and 500. The module also includes a 10V reference, an S/H amplifier, and a 574-type A/D converter. The system's throughput ranges from 8.2k samples/sec (with 0.02% accuracy) at a gain of 500 to 24k samples/sec (with 0.01% accuracy) at a gain of 1. You can improve the throughput by pipelining the selection of mux channels. The module's power-supply requirements are ±15 and +5V. It dissipates 980 mW typ, 1300 mW max. HS 9414C, $119; HS 9414B, $220. Delivery, six to eight weeks ARO.

Hybrid Systems Corp, 22 Linnell Circle, Suburban Industrial Park, Billerica, MA 01821. Phone (617) 667-8700.

Circle No 354



D/A CONVERTER

- *Offers composite-video control functions*
- *Suitable for 2k×2k-pixel displays*

Offering 300-MHz word rates and a low (45-pV·sec) glitch impulse, the Model AD9703 8-bit video D/A converter is suitable for displays having resolution as high as 2k×2k pixels. The device incorporates blanking, composite-sync, 10% overbright, and reference-white control pins. The settling time to within ±0.4% of full gray-scale output is 6 nsec. Other specs include ±0.2% max integral and differential nonlinearity, ±2-mV max initial offset voltage, and guaranteed monotonicity. The converter's logic inputs are compatible with both 10KH and 100KH ECL systems; the output satisfies the RS-170 video standard and can drive a 75Ω line directly. The AD9703 comes in a 24-pin DIP, operates from a −5.2V ECL supply, and dissipates 1.1W. Nonhermetic BW-grade units operate over −25 to +85°C; hermetic BD- and TD-grade units operate over −55 to +125°C. The three grades cost $42.60, $47.20, and $52.90 (100), respectively.

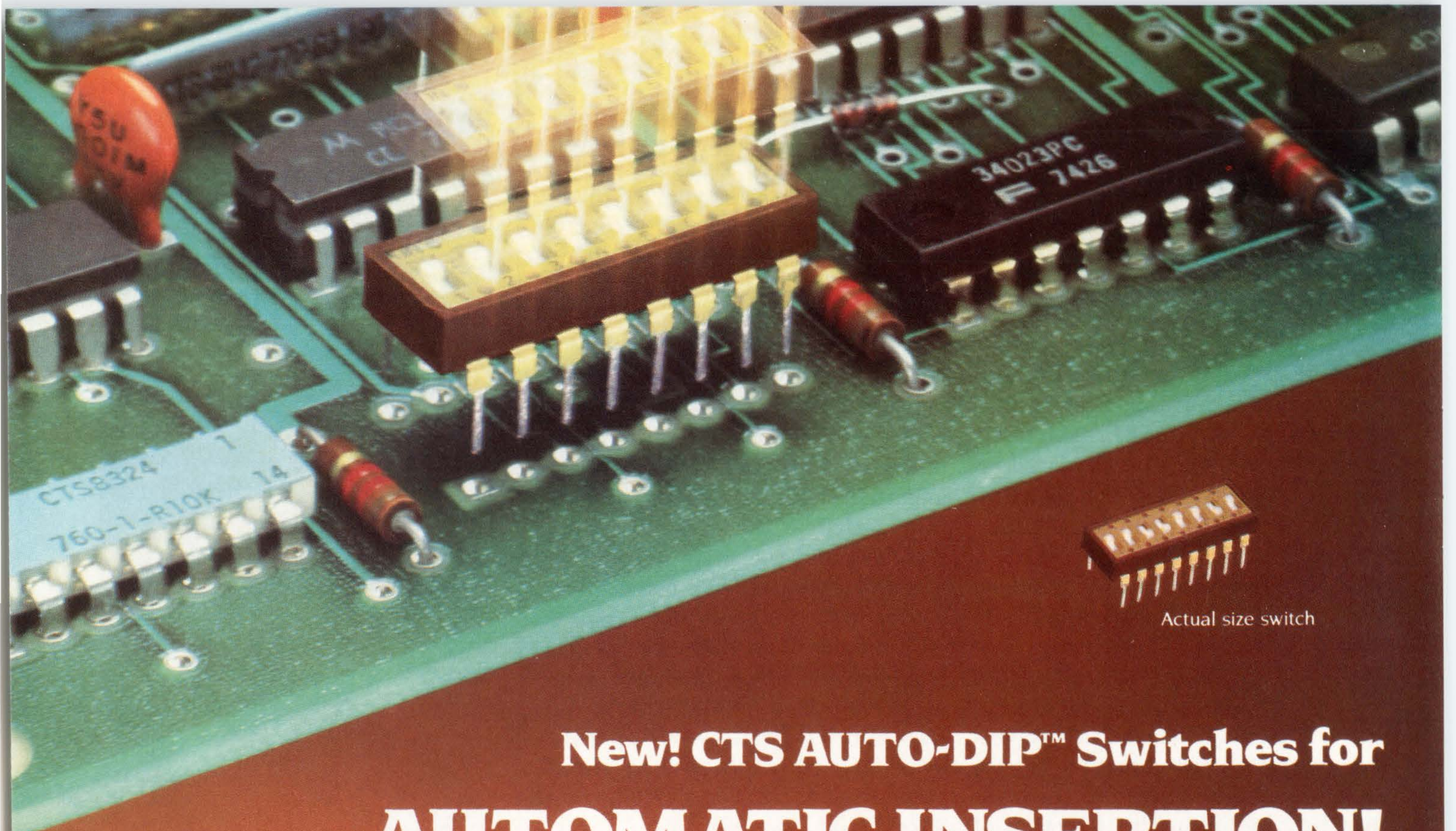
Analog Devices Inc, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 329-4700. TWX 710-394-6577.

Circle No 355

DISCRIMINATOR

- *Couples transducers to digital processors*
- *Identifies and measures motion*

Model THCT2000, an LSI IC, provides an interface between mechanical devices and a data bus. It identifies and measures rotation or linear motion; the circuit determines the direction and displacement of mechanical devices, based on input signals from two transducers connected in quadrature. You can use the IC to measure the duration of a sensor-generated pulse by using a known clock rate, or to measure the frequency of a mechanical event over a known time interval. The discriminator IC also has a 16-bit read/load counter; you can use the counter separately or in cascade to provide accuracy greater than 16 bits. Offering TTL- and CMOS-compatible inputs, the device provides parallel 8-bit 3-state outputs. Clock frequency is 4 MHz max. Packaging



Actual size switch

New! CTS AUTO-DIP™ Switches for AUTOMATIC INSERTION!

You'll realize immediate cost savings in board production with the New CTS Series 207 AUTO-DIP™ Switch.

Because they are the same size as your IC's—these new Series 207 AUTO-DIP™ switches can be used in your automatic insertion equipment right along with IC's...without machine adjustment. You get economical high speed board production. You'll save significant board space as well! This new switch takes only 37% of the volume of a standard DIP switch allowing for closer board stacking and space savings.

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Contact: CTS Corporation,*
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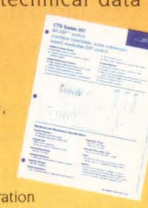
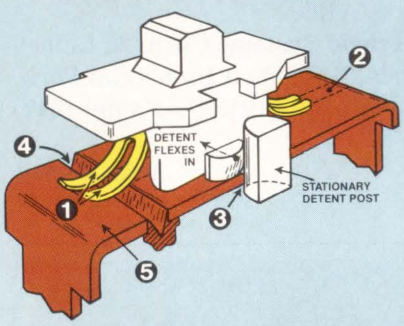
Electromechanical Group,
500 Linne Road,
Paso Robles, CA 93446.
Phone: (805) 239-0427



*In Calif. dba CTS Electronics Corporation

CIRCLE NO 61

Switch reliability that is the best ever!



1. Redundant gold inlaid contacts dramatically enhance contact reliability.
2. Positive wiping contacts assure low and consistent contact resistance. (.050″ travel)
3. Detent function separated from contacts to optimize both designs.
4. Gold contacts never abraded or contaminated by sliding over polymer surfaces. Contacts never touch a nongold surface
5. No contactor deflection for the life of the switch. Constant contact force eliminates overstressing of contacts for greater reliability.

CTS means Reliability

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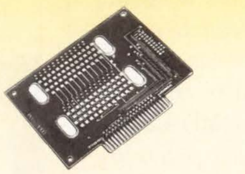
CIRCLE NO 62

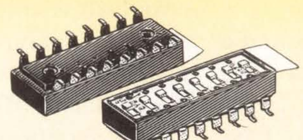
Series CCXO-140 Leadless chip carrier crystal oscillator for surface mounting
Phone: (815) 786-8411

CIRCLE NO 63



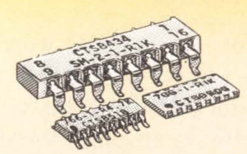
PC Boards Complex double-sided and multilayer.
Phone: (415) 659-1770

CIRCLE NO 64



Surface Mount AUTO-DIP® Switches Process compatible. Series SM 207.
Phone: (805) 238-0350

CIRCLE NO 65

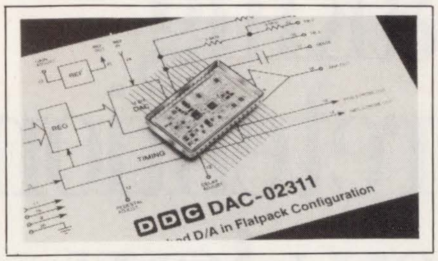


Surface Mount Resistor Networks Numerous package configurations and attachment choices.
Phone: (219) 589-8220

options include a 28-pin plastic or ceramic DIP and a 28-pin PLCC. \$7.20 (1000).

Texas Instruments Inc, Semiconductor Group SC-647, Box 809066, Dallas, TX 75380. Phone (800) 232-3200.

Circle No 356



D/A CONVERTER

- *14-bit deglitched device*
- *Comes in 32-pin flat pack*

The DAC-02311 is a 14-bit, 10-MHz, deglitched D/A converter that comes in a 32-pin flat pack for surface-mount applications. It has a low-impedance voltage output specified for 12- or 13-bit linearity. You program the device's pins for one of five different ranges of output voltage. Using external potentiometers, you can trim the offset, gain, and pedestal errors to zero. The converter operates over the military temperature range and comes in versions screened to MIL-STD-883. \$245. Delivery, stock to eight weeks ARO.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600. TWX 510-228-7324.

Circle No 357

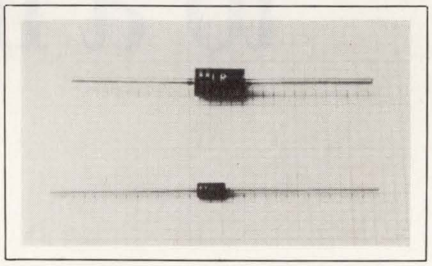
QUAD OP AMP

- *Exceeds precision specs of OP-07*
- *Draws 2.9-mA total supply current*

On a per-amplifier basis, the Model OP-400GP quad op amp consumes less than one-fourth the power used by an OP-07, yet meets or exceeds the precision specs offered by a single OP-07 device. The maximum input-offset voltage and drift are 300 μV and 2.5 μV/°C, respectively. The voltage gain for each amplifier in the OP-400GP is 3,000,000 min. Other specs include a 7-nA max input-bias current, 11-nV/$\sqrt{Hz}$ typ voltage noise, 110-dB min CMR, and 105-dB min PSR. The four op amps can drive capacitive loads as high as 10 nF without oscillation. The device uses the industry-standard pinout for quad op amps. \$5.35 (100).

Precision Monolithics Inc, Box 58020, Santa Clara, CA 95052. Phone (408) 727-9222. TWX 910-338-0218.

Circle No 358



DIODES

- *Feature fast recovery*
- *Rated at 1 and 3A*

The 11DF and 31DF fast-recovery diodes come in axial-lead packages. Rated at 1A and 3A respectively, both the 11DF and 31DF come in 100 and 200V versions (0.98V forward-voltage drop, 35-nsec recovery) and 300 and 400V versions (1.25V forward-voltage drop, 30-nsec recovery). 11DF, \$0.60 (100); 31DF, \$0.68 (100). Delivery, six weeks ARO.

International Rectifier Corp, 233 Kansas St, El Segundo, CA 90245. Phone (213) 607-8837.

Circle No 359

GATE ARRAYS

- *Accommodate Mentor workstations*
- *Use 2-μm CMOS processing*

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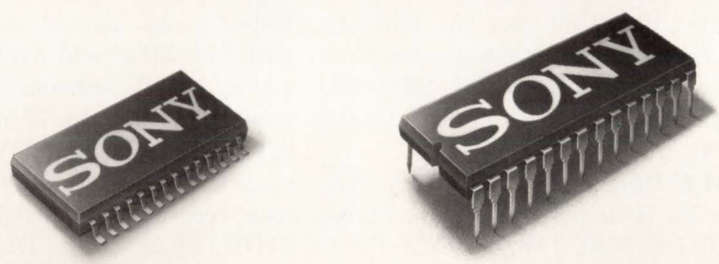
SONY SRAM DEVICES			
PART NUMBER	ORGANIZATION	SPEED (ns)	PACKAGE
CXK5814P—35L/45L/55L	2K x 8	35/45/55	300 mil DIP
CXK5816PN—10L/12L	2K x 8	100/120	600 mil DIP
CXK5816M—10L/12L	2K x 8	100/120	SOP*
CXK5416P—35L/45L/55L	4K x 4	35/45/55	300 mil DIP
CXK5864AP—70L/10L	8K x 8	70/100	600 mil DIP
CXK5864AM—70L/10L	8K x 8	70/100	SOP*
CXK5864PN—12L/15L	8K x 8	120/150	600 mil DIP
CXK5864M—12L/15L	8K x 8	120/150	SOP*
CXK5464P—45L/55L/70L	16K x 4	45/55/70	300 mil DIP
*Small Outline Package			



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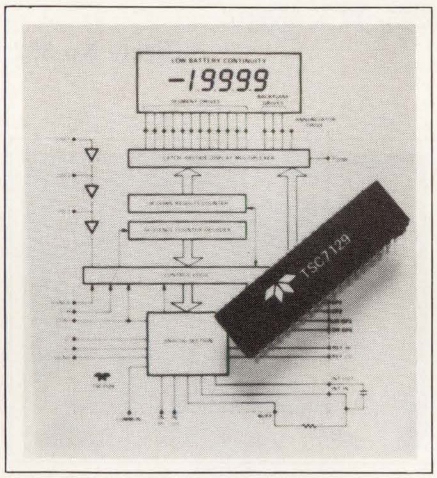
PERFORMANCE OF 32K X 8 SRAM					
PART NUMBER	PROCESS	SPEED (ns)	PACKAGE	DATA RETENTION CURRENT (MAX)	DATA RETENTION CONDITION
CXK58256P—10L/12L	MIX MOS	100/120	600 mil DIP	50 μA	0 to 70°C
CXK58256MF—10L/12L	MIX MOS	100/120	SOP	50 μA	0 to 70°C
CXK58256P—10LL/12LL	MIX MOS	100/120	600 mil DIP	10 μA	0 to 70°C
CXK58255P—45/55/70	FULL CMOS	45/55/70	600 mil DIP	5 μA	−30 to 85°C
CXK58255P—45L/55L/70L	FULL CMOS	45/55/70	600 mil DIP	2.5 μA	−30 to 85°C

SONY®

stations. Three levels of available support span the range from schematic capture to layout and back-annotation of the devices. Using a Mentor Capture workstation, you can draw the schematic design and run a design-check package. With the addition of simulation software and the Mentor Idea workstation, you can perform logic simulation that includes fan-in, fan-out, processing delays, and user-defined resistance delays. Finally, by using Mentor's Gate workstation, you can place and route the design's macro cells. The three levels of support from the gate-array manufacturer cost $1500, $4000, and $27,500, respectively.

Siliconix Inc, 2201 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 988-8000.

Circle No 360



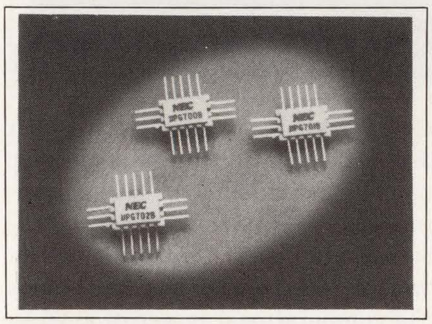
A/D CONVERTER

- *CMOS 4½-digit device*
- *Drives a multiplexed LCD*

The TSC7129 is a CMOS 4½-digit A/D converter that directly drives a multiplexed LCD; you supply only a voltage reference and a few passive components. Package options include a 40-pin plastic or ceramic DIP and a 44-pin plastic leaded chip carrier or flat pack. The converter's successive integration technique provides resolution to 10 μV and a reading accuracy to 0.005% of full scale. The device is pin compatible with the ICL7129 from Intersil, but eliminates the external RC network that's normally required by including phase compensation for the internal integrator amplifier. Drawing 500 μA from a 9V battery, the chip includes circuitry for low-battery detection; overrange, underrange, and change-range outputs (for autoranging); and a latch-and-hold input (for snapshot readings). Chips, $7; packaged parts, from $9.95 (100). Delivery, 8 to 10 weeks ARO.

Teradyne Semiconductor, Box 7267, Mountain View, CA 94039. Phone (415) 968-9241.

Circle No 361



GaAs LOGIC ICs

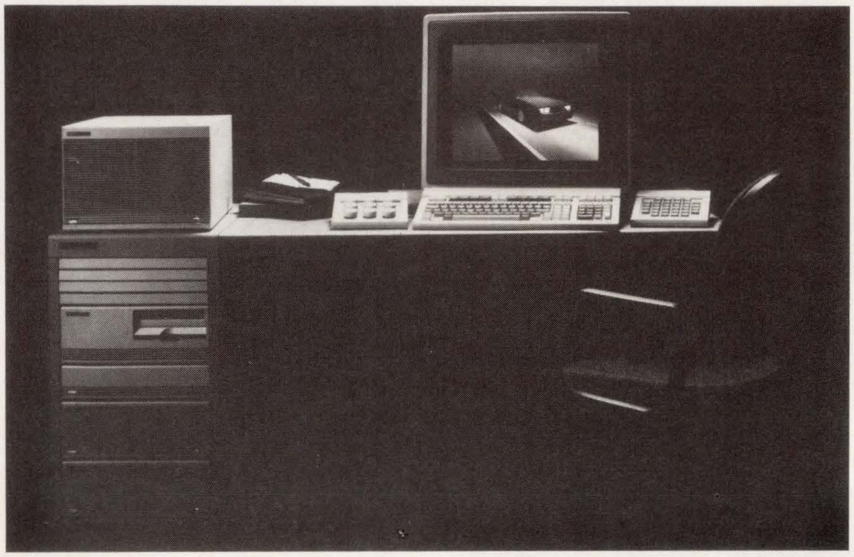
- *Can operate at speeds exceeding 2.4 GHz*
- *Compatible with ECL circuits*

These three GaAs digital ICs can operate at speeds as high as 2.4 GHz. Model μPG700B is a master-slave D-type flip-flop that has set/reset functions. Model μPG701B is a master-slave T-type flip-flop that also offers set/reset functions. Model μPG702B is a 3-input OR/NOR gate. Typical positive-supply current (I_{DD}) for the μPG700B and -702B is 70 mA; the μPG701B's I_{DD} is 80 mA. Models μPG700B and -702B draw a 50-mA negative-supply current (I_{SS}); the μPG701B draws 60 mA. In 16-pin hermetic ceramic packages, $197 (100). Delivery, three months ARO.

California Eastern Laboratories, 3260 Jay St, Santa Clara, CA 95054. Phone (408) 988-3500.

Circle No 362

CAE & SOFTWARE DEVELOPMENT TOOLS



CAE WORKSTATION

- *Uses 25-MHz 68020 and 20-MHz numeric coprocessor*
- *Provides 32k-byte, write-through cache with no wait states*

The HP Series 9000 Model 350, available in six configurations, is based on the 25-MHz 68020 μP, supplemented by the 20-MHz 68881 numeric coprocessor. All configurations come with a 32k-byte, write-through cache that operates with no wait states; 8M bytes of RAM (expandable to 32M bytes); HP-IB (IEEE-488) and RS-232C interfaces; a high-speed disk interface; and a LAN interface conforming to the IEEE 802.3 standard. Configurations include a keyboard, a display, a mouse, and all necessary cabling. The operating system is HP-UX, the vendor's implementation of Unix. At the low end of the line is the 350SPU, a stand-alone unit that can act as a network server or multiuser processor. At the other end is the 350SRX workstation, which provides a graphics resolution of 1280×1024 pixels and is equipped with a 19-in. color display that can have as many as 24 color planes. The 350SRX is capable of executing complex applications such as 3-D mechanical design, molecular modeling, modeling of solids, geophysical engineering, and earth-strata analysis. According to the vendor, this model has four times the computational power of a VAX-11/780. Prices range from $21,900 for the 350SPU to $54,900 for the 350SRX.

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 381

VLSI ANALYSIS

- *Runs on vendor's VLSI-verification systems*
- *Lets you characterize a VLSI device at the prototype stage*

Meta-Shmoo is an enhancement of the operating software of the vendor's Topaz design-verification systems for VLSI devices. It lets you automatically plot the performance of a device by means of a Shmoo (safe modes of operation) plot. You can plot time vs voltage, time vs time, voltage vs time, or voltage vs voltage, both for thorough characterization of a device and for automatic measurement of parameters, such as propagation and setup times. The program lets you select the parameters to be plotted, the pins on which the system will take measurements, maximum and minimum test values, and incremental values at which tests are to be conducted. You can display the test results on the screen or direct them to a dot-matrix printer. During operation, the Topaz system runs the entire vector set at each incremental point on the plot, thereby allowing the program to display the worst-case pass/fail condition for each set of Shmoo parameters. $2500.

HiLevel Technology Inc, 18902 Bardeen, Irvine, CA 92715. Phone (800) 445-3835; in CA, (714) 752-5215. TLX 655316.

Circle No 382

PC-BOARD CAD

- *Enhanced features include zoom, pan, and scroll*
- *Autorouting speed of original product increased by 100%*

Enhancements to the Artworker 3000 pc-board CAD system increase its overall speed by as much as 20% and add high-speed zoom, pan, and scroll facilities. You can zoom in or out of a layout using as many as four different predefined magnification factors. Additional enhancements include a 100% speed improvement in the autorouting operation, with


SIEMENS

some improvement in the quality of the routing. The system allows you to generate schematics incorporating as many as ten 100×100-in. sheets, and to perform interactive placement. The system comes with all necessary hardware and software; prices for the enhanced Artworker 3000 start at approximately £12,000.

Wayne Kerr Datum Ltd, Jenner Rd, Crawley, West Sussex RH10 2GA, UK. Phone (0293) 549011. TLX 87201.

Circle No 383

BASIC INTERPRETER

- *Runs on all Apollo computers*
- *Provides a superset of ANSI Basic X3.60 plus other dialects*

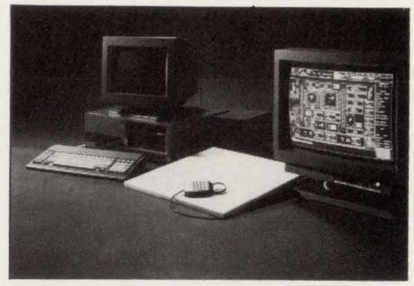
This Basic interpreter, formerly available only for the Apollo DN300 and DN320, now runs on all Apollo computers, including DN3000 machines. The interpreter embodies a superset of ANSI Basic X3.60, plus several existing Basic dialects, which allows it to accept many programs that run on other Basics. It recognizes variable names containing as many as 255 alphanumeric characters, and it allows dynamically evaluated data statements. It also supports user-defined functions; multiple statements per line; and integer, real, and string variables. You can write your Basic program to trap execution errors. The interpreter compiles the program into executable pseudo machine code, and it can operate in both interactive and batch modes. It sells for less than £500 (single-user license).

Lattice Logic Ltd, 9 Wemyss Pl, Edinburgh EH3 6DH, UK. Phone 031-225 3434. TLX 72465.

Circle No 384

Lattice Logic USA, 3333 Bowers Ave, Suite 199, Santa Clara, CA 95954. Phone (408) 748-9797.

Circle No 406



PC-BOARD CAD

- *Based around an IBM PC/AT-compatible computer*
- *Links to Cadat and Spice simulation packages*

The KAD-286 is a CAD workstation that allows you to perform schematic capture, simulation, and layout generation for pc-board or hybrid-component designs. It consists of the company's IBM PC/AT-compatible computer equipped with a graphics processor board (1024×780-pixel resolution), a 20-in. color (or 17-in. monochrome) moni-

(See page 210).

tor, and an 11×11-in. digitizing tablet. The system's graphics editor features menu, function-key, or cursor-controlled data entry. You can organize schematics into as many as 200 pages and produce single-page or global net lists and component listings from them. Selectable net-list formats allow you to pass net-list data to Cadat or Spice simulation software, and you can modify net lists during the simulation or routing phases. Post-layout processing allows you to perform design-rule checks and to compare and verify layout and schematic net lists. Post-layout software is available, including drill-tape generation and plotting capabilities for pen, photo, impact, laser, and thermal plotters. The workstation, including software, sells for around DM 40,000. The software is also available separately.

Kontron Messtechnik, Oskar-von-Miller-Strasse 1, 8057 Eching/Munich, West Germany. Phone (08165) 77551. TLX 526719.

Circle No 385

Kontron Electronic Inc, 630 Clyde Ave, Mountain View, CA 94039. Phone (415) 965-7020.

Circle No 407

CD ROM RETRIEVER

- *Lets you prepare documents for transfer to CD ROM*
- *Lets you use an IBM PC to retrieve data from a CD ROM*

SilverSmith is a document-preparation and indexed-retrieval program that conforms to the Association of American Publishers (Washington, DC) standard for document markup, using the Standard Generalized Markup Language (SGML). The SGML is defined by ISO standard 8879 (available from the American National Standards Institute, New York, NY), and it's currently being considered by the National Information Standards Organization as a candidate for the standard for data interchange on CD ROM media. The complete package consists of a build (preparation) module and a search-and-delivery module. The build module allows you to create an SGML index for a document that you have prepared with your usual word processor and SGML tags. You can use the search-and-retrieval module with floppy disks, hard disks, or optical disks; it lets you perform a search at a speed that is independent of file size, and then retrieve data that meets your search criteria. At the start of a search session, you can set the boundaries for the search (eg, paragraph, chapter, book), and a window displays the SGML tags used in the document. You can select the tags by entering them from the keyboard, or by using the cursor to highlight the desired tags. You can use the Boolean text-search operators AND and NOT in your query. To run either module, you need an IBM PC or compatible equipped with at least 128k bytes of RAM and MS-DOS 2.1 or later. Complete package, $595; search-and-delivery module only, $100.

Taunton Engineering Inc, 505 Middlesex Tpk, Suite 11, Billerica, MA 01821. Phone (617) 663-3667.

Circle No 386

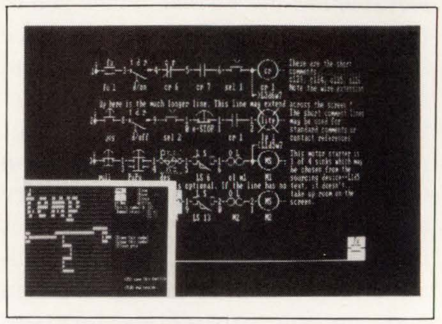
GRAPHICS TOOL KIT

- *Implements the proposed ANSI and ISO extensions to GKS*
- *Lets you add light sources to highlight 3-D images correctly*

Visual:3D is a modular, 3-dimensional graphics library based on the internationally accepted GKS (Graphics Kernel System) standard. The vendor has enhanced the basic GKS standard with extensions required by many 3-D applications. Some of these extensions implement the guidelines set forth in the GKS-3D draft proposal (also known as ISO DP 8805); these include drawing primitives for boxes, spheres, cylinders, cones, prisms, ovals, and rounded rectangles. More advanced extensions include solid shading, facet shading with hidden-surface removal, smooth shading, and global shading by ray tracing. The tool kit provides solid-surface attributes that include multiple light sources of different types, reflectivity and translucency, and antialiasing. The package includes a graphics-device-management system that provides device independence by letting you describe the environment's capabilities and constraints in an ASCII text file. The system analyzes the graphics requirements and produces the required control stream or invokes the appropriate system calls. From $1500 to $8000, depending on the system-hardware configuration.

Visual Engineering Inc, 2150 N First St, Suite 600, San Jose, CA 95131. Phone (408) 922-2800.

Circle No 387



PLC DESIGN

- *Provides predrawn symbols for many ladder-logic devices*
- *Runs on IBM PCs and compatibles*

PLC-Ladder is a drawing tool for

the ladder-logic diagrams used in the design of relay logic and programmable-logic controllers. The program runs on any IBM PC or compatible machine and allows you to call up logic symbols from a library and place them in a cellular grid that accommodates as many as 256 rungs. The package includes a graphics font editor that lets you create nonstandard symbols and store them in the library. You can copy, move, insert, or delete complete rungs by means of simple commands. Wire-management routines automatically handle interrung connections and provide for manual or automatic renumbering of the rungs after an insertion or deletion. Drawings are stored on disk; you can obtain hard copy by directing them to an inexpensive dot-matrix printer. Because the program is dedicated to the creation of ladder diagrams, the vendor claims, it is faster to use for this application than standard CAD programs are. The company also maintains that a user requires less than one hour of self-training time to become competent in the program's use. $495.

Simon Industries Inc, 2901 Hoover St, Orange, CA 92667. Phone (714) 639-9436.

Circle No 388

C COMPILER

- *Runs on PC/AT and compatibles*
- *For 80386 processor*

The C 386 compiler and the RLL 386 relocation, linkage, and library tools package are 80386 software-development tools that run on the IBM PC/AT or compatibles. The C 386 compiler implements the full C language. It generates code that is compatible with the vendor's other 80386 languages, so you can link modules written in different languages on different hosts. The compiler also provides facilities for symbolic debugging. The RLL 386 package consists of a linker, a builder, a mapper, and a librarian. The linker integrates program modules that have been separately compiled on a PC, VAX, or Xenix system into larger files or complete programs. The builder assigns absolute addresses to files created by the linker, to allow these files to be placed in nonvolatile memory. The mapper generates a program memory map to aid in debugging and software documentation. The librarian manages the program modules so that they can easily be accessed by all members of your programming team. C 386 compiler, $900; RLL 386 package, $600.

Intel Corp, Literature Dept, 3065 Bowers Ave, Santa Clara, CA 95052. Phone local office.

Circle No 389

NEW PRODUCTS

COMPUTERS & PERIPHERALS

A/D BOARDS

- *Data-acquisition boards for IBM PC/AT and for Multibus II*
- *Sample rates of 250 kHz available*

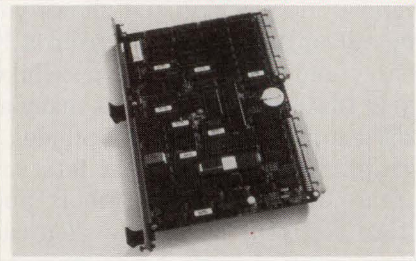
The DT2821-G analog I/O board provides single-board data acquisition for the IBM PC/AT and compatible computers. The DT2401 Series analog I/O boards, on the other hand, are directed at Multibus II applications. The DT2821-G gives you 12-bit resolution for 16 single-ended or eight differential analog inputs, programmable gain, two 12-bit deglitched DACs, a channel-gain list, a programmable clock, and support for interrupts and DMA transfers. The board can acquire data at a sustained rate of 250 kHz. (At present, however, the only PC that can run at this rate is the Compaq 386; other PCs can sustain 180 to 235 kHz, depending on their clock speed.) The DT2401 Series features two 12-bit, 50-kHz D/A converters, 32 lines of digital I/O organized as two 16-bit ports, and an onboard programmable clock that can start A/D conversions or control off-board events. DT2821-G board, $2995; DT2401 Series, $1695 to $2960.

Data Translation, 100 Locke Dr, Marlboro MA 01752. Phone (617) 481-3700. TLX 951646.

Circle No 363

CRT CONTROLLER

- *For VME Bus systems*
- *Available in ruggedized military versions*



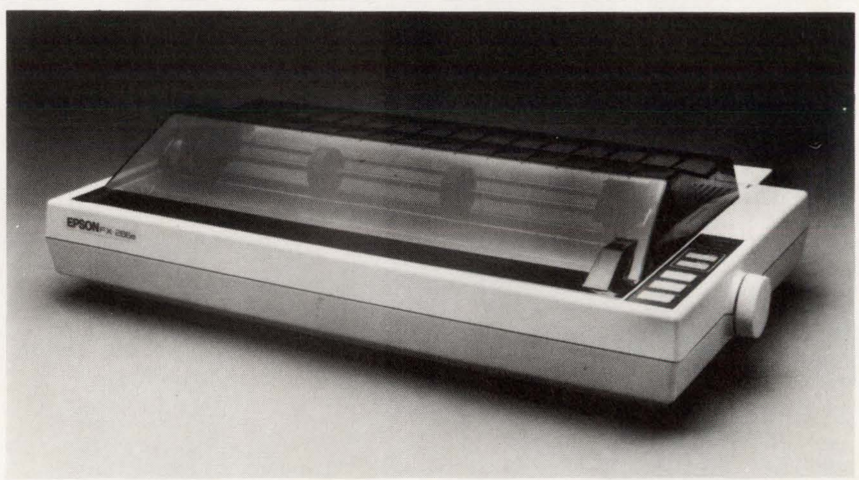
The SVME-676, a VME Bus-compatible alphanumeric CRT controller, offers serial and parallel I/O, a timer, and a real-time clock/calender with battery backup. It provides RS-170-compatible video output with nonserrated vertical synchronization for alphanumeric displays. The board generates the video timing signals and refresh memory addressing. The module has a memory-mapped video refresh memory and attribute memory, the combination of which provides multilevel gray-scale, underline, blink, and reverse video. It also features software-selectable screen formats and programmable cursor-blink rates. The board provides 20 bits of parallel I/O and a 24-bit timer on board. It offers two channels of serial I/O, providing an optional RS-422 or RS-423 interface. Ruggedized military versions are also available. $1690.

DY-4 Systems Inc, Suite 202, 1475 S Bascom Ave, Campbell, CA 95008. Phone (408) 377-9822.

Circle No 364

PRINTERS

- *Two additional models to printer line*
- *Both come with Roman and sans serif NLQ fonts*



The FX-86e (80-column) and FX-286e (136-column) dot-matrix printers are 9-pin dot-matrix printers that provide Roman and sans serif near-letter-quality (NLQ) fonts as standard features. The printers support pica, elite, proportional, italic, and condensed printing modes. Double-height and double-width characters are also available. You can select draft or NLQ and normal or condensed modes via front-panel buttons. Automatic single-sheet feed is standard on both models. In draft mode, both units print at 240 cps and 12 characters per inch (cpi); in NLQ mode, they print at 48 cps and 12 cpi. Each printer operates either in conjunction with Epson's standard code for printers (ESC/P) or in IBM printer emulation mode. Optional accessories for the printers include a single-bin sheet feeder, a 32k-byte data buffer, and the company's 81xx Series of serial interface boards. FX-86e, $549; FX-286e, $799.

Epson America Inc, 2780 Lomita Blvd, Torrance, CA 90505. Phone (213) 539-9140.

Circle No 365

NEED HELP WITH COOLING DESIGN PROBLEMS?

At Torin Engineered Blowers, we specialize in providing creative solutions to air-moving application problems.

Comprehensive test-laboratory facilities, and over 40 years of design experience have established our reputation for technical leadership in custom blower design for the electronics cooling, business machine, aerospace and military markets.

Our quality product line includes custom-designed single, dual and multi-stage centrifugal blowers, transverse-flow blowers, mixed-flow blowers, cabinet blowers and vane-axial fans.

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CIRCLE NO 133

DISPLAY CONTROLLER

- *Supports a variety of monitors*
- *Video-output section is on a piggyback module*

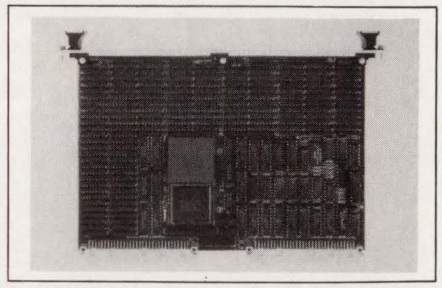
The Intelligent Graphics Controller (IGC) is a modular graphics-controller board with which you can program your own graphics primitives. The board is designed around the TI34010, a 32-bit graphics-controller chip that uses software to form graphics primitives. Compatible with the IBM PC, the board supports 640×480- to 1280×1024-pixel monitors. You can choose the appropriate video-output stage for your application from three piggyback modules, which address low, medium, and high levels of monitor performance. You can display 16 to 256 colors from palettes of 4096 or 16.8 million colors. The board provides 512k bytes of RAM for storing command software for the graphics system's processor. The Direct Graphics Interface Specification (DGIS) is the standard interface for the IGC. Model 10 comes with 512k bytes of video RAM; 640×480-, 960×720-, and 1024×768-pixel resolution; and 16 available colors from a palette of 4096. Model 20 comes with 1M byte of video RAM; 640×480-, 960×720-, and 1024×768-pixel resolution; and 256 available colors from a palette of 4096. Model 30 comes with 1M byte of video RAM; 1024×1024- and 1280×1024-pixel resolution; and 256 available colors from a palette of 16.8 million. Model 10, $1499; Model 20, $1999; Model 30, $2499.

Emulex Corp, Persyst Div, Box 6725, Costa Mesa, CA 92626. Phone (714) 662-5600.

Circle No 366

VME RAM BOARD

- *Board can be configured with 2M or 4M bytes of RAM*
- *Error detection and correction corrects single-bit errors*



The DRAM-5 board offers a choice of 2M or 4M bytes of dynamic RAM for VME Bus applications and is corrected for all single-bit errors. The DRAM-5 also detects and reports to the host all double-bit errors. LEDs on the front panel signal all detected errors. Both versions of the board use ZIP 256k×1-bit RAMs for space savings. The boards are 32 bits wide in both data path and address path, and they employ a 64-bit-wide internal cache that enhances access time for sequential read operations. Read-access time is 140 nsec with a cache hit. Worst-case access time of 280 nsec occurs when read access misses the cache. Write time for the boards is 120 nsec. The DRAM-5 contains a control and status register, implements all VME Bus data-transfer modes, and provides support for unaligned and read-modify-write transfers. For 24- or 32-bit-address operation, you can access memory in 64k-byte blocks in conjunction with a mode jumper. DRAM-5A (2M bytes), $2095; DRAM-5B (4M bytes), $2895.

Force Computers Inc, 727 University Ave, Los Gatos, CA 95030. Phone (408) 354-3410.

Circle No 367

RLL CONTROLLER

- *Run-length-limited controller for 3½-in. disk drive*
- *Attaches to two ST506/412 or two ST412R drives*

The OMTI 3127 3½-in. disk-drive controller incorporates run-length-limited (RLL) encoding and attaches as many as two ST506/412- or two ST412R-compatible fixed or removable Winchester drives to computer systems using the SCSI host


ON
OFF

interface. The drive supports 1:1 interleaving and a buffering scheme that helps to generate a 7.5M-bps data-transfer rate. The RLL algorithm can increase the storage capacity of the disks by as much as 50%. A 48-bit polynomial is used for error detection and correction. The drive consumes 0.75A. $129 (OEM qty).

Scientific Micro Systems Inc, 339 N Bernardo Ave, Mountain View, CA 94043. Phone (415) 964-5700.

Circle No 368

PROTOTYPING BOARD

- *Allows you to prototype an intelligent VME Bus slave board*
- *Communicates with other bus processors via shared memory*

The TSVME431 prototyping card for the VME Bus features a 68010 10-MHz μP and a VME Bus interface that occupy one-half of the double-Eurocard card, which is adjacent to the VME Bus P1 connector. The other half of the board, adjacent to the P2 connector, has a 110×160-mm, 0.1-in.-pitch wire-wrapping area and provision for the installation of a P2 connector. The wire-wrapping board detaches from the processor section via a 96-pin DIN-41612 connector, which carries a buffered extension of the 68010's data and address bus. It also carries interrupt and interrupt-acknowledge lines, control lines, and a decoded address line that indicates the internal memory space reserved for the user. The μP has 60k bytes of onboard, dual-ported RAM, 4k bytes of local memory, two sockets for a maximum of 128k bytes of EPROM, two sockets for RAM/EPROM/EEPROM, and two RS-232C interfaces. Approximately Fr fr 8000.

Thomson Semiconducteurs, 45 Ave de l'Europe, 78140 Velizy, France. Phone (1) 39469719. TLX 204780.

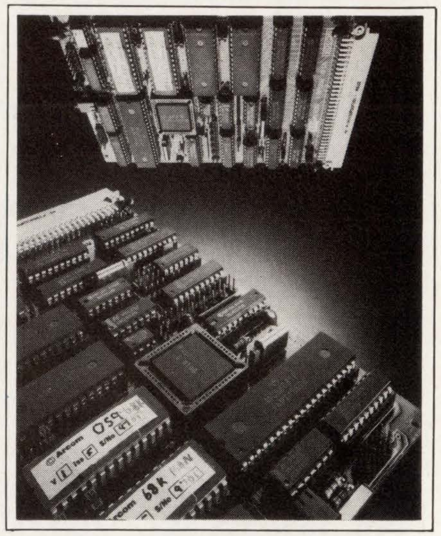
Circle No 369

Thomson Components-Mostek Corp, 7950 E Redfield Rd, Scottsdale, AZ 85260. Phone (602) 951-2900.

Circle No 370

CPU CARD

- *OS9/68000 operating system provides support*
- *Based on an 8-MHz 68008 μP*



Supported by the OS9/68000 OS, the SC008 CPU card for STE Bus systems suits real-time or operating-system environments. The board runs an 8-MHz 68008 μP and has 16k bytes of RAM, four memory sockets for RAM or EPROM, two serial I/O ports, and a counter-timer/real-time clock. The CPU can operate as a single STE Bus master, or it can provide bus-access arbitration alongside other STE Bus CPUs. It supports nonvectored-interrupt handling for the STE Bus and one interrupt for onboard devices. The CPU can access the full 1M-byte STE Bus address space as well as 4k bytes of I/O space. £275.

Arcom Control Systems Ltd, Unit 8, Clifton Rd, Cambridge CB1 4WH, UK. Phone (0223) 242224. TLX 817114.

Circle No 371

Dow Corning Presents

A Design Digest of Electronic Reliability

Designing a high-performance electronic product is only half the battle. Protecting it is the other half. Demand our high-reliability protective materials and you have won. Here is what we mean:

New thermally-conductive elastomer conducive to many uses.

For thermal dissipation that protects perfomance, choose new SYLGARD® Q3-6605 thermally-conductive elastomer. It is especially useful as a thermally-conductive adhesive to bond ceramic hybrid circuit packages to heat sinks. Other uses include bonding or potting power supplies, coils, heavy-duty relays, and similar units. Primerless, too.

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When you encapsulate components in a silicone gel, you protect them against hostile environments, temperatures as low as −80°C and more. DOW CORNING® silicone gels also cushion components against stress and vibration. We offer a broad choice of one component and two component materials, for room temperature and heat cure processes.

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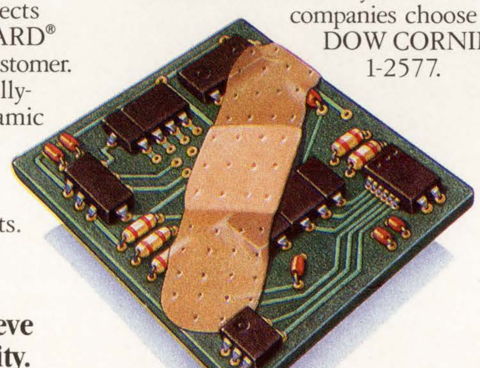
A PC board coating simply has to be reliable. And with DOW CORNING® 1-2577 conformal coating you get more: easy repairability when components need replacing. Add superior protection in extreme environments, versatile processing with dipping or spraying, and you have all the reasons major automotive and military electronics companies choose DOW CORNING 1-2577.



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OPTIGARD® optical fiber coating UV-cures in just 0.3 seconds—5 to 20 times faster than thermal-curing coatings. And it protects against moisture and "micro-bends" better than acrylate coatings. It's part of the OPTIGARD family which includes fiber optics grade $SiCl_4$ core and cladding and OPTIGARD cable filler.

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Stress. Moisture. Ion contamination. Voltage linkage. Alpha particles. All are killers of your devices, robbers of reliability. Now you have a defense against them. HIPEC® coatings protect semiconductors and hybrids through a wide range of temperatures and environments. They're available in a variety of forms from gel to firm elastomer and resins. And HIPEC coatings are easier to process than other high-performance materials.

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Write Department 7013, Midland, MI 48686-0994.

DOW CORNING®

STEPPING MOTORS

- *Torque ratings to 142 oz-in.*
- *Class B insulation standard*

The 1.8° full-step angle motors in the D34D62-22 Series of stepping motors operate at 200 steps/revolution and provide holding torque ratings ranging from 26 to 142 oz-in. Phase-current ratings range from 1 to 4.7A in unipolar operation, and from 0.33 to 6.6A in bipolar operation. Rotor inertia ratings range from 0.28 to 1.8 oz-in^2, and detent-torque ratings spec at 4 to 14 oz-in. Bipolar models have four AWG-22 leads that are 12 in. long; the six models that run in both bipolar and unipolar modes have eight leads. Standard insulation for these motors is Class B. The motors operate over a −20 to +50°C ambient range; the recommended case temperature is 100°C max. From $69.

Stock Drive Products, 2101 Jericho Tpk, New Hyde Park, NY 11040. Phone (516) 328-3330.

Circle No 372

MOSFETs

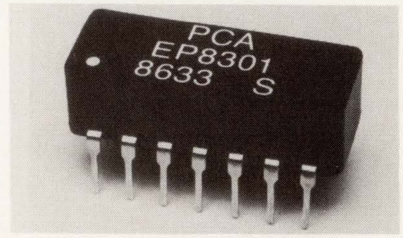
- *Qualified to MIL-STD-19500/543B*
- *Power dissipation equals 150W*

The 2N6768 and 2N6770 military-qualified MOSFETs are rated for 400 and 500V, respectively. The two devices are qualified to MIL-STD-19500/543B and listed under QPL-19500 for JANTX and JANTXV levels. The 6768 is a 15A unit with an on-state resistance of 0.3Ω. The 6770 is rated for 12A and has a 0.4Ω on-state resistance. The units are available in TO-204AA metal packages and operate over −55 to +150°C. The total power dissipation at 25°C is 150W. $20 to $45.

Fairchild Semiconductor Corp, 4300 Redwood Hwy, San Rafael, CA 94903. Phone (800) 554-4443; in CA, (415) 499-4416.

Circle No 373

DELAY LINES

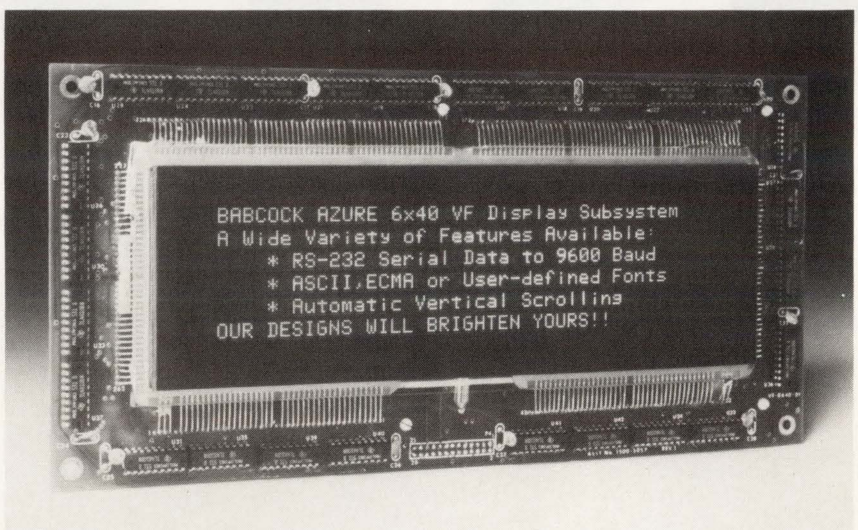


- *Delay times range as high as 1000 nsec*
- *Buffered input and outputs*

EP8300 Series TTL-compatible active delay lines provide 10 equally spaced output delays. The 28 units in the family offer total delay times of 50 to 1000 nsec, ±5% or 2 nsec, whichever is greater. The delay-line input and the 10 output taps are buffered by a Schottky TTL inverter. The rise time specs at 4 nsec max for 50- to 500-nsec delay models, and 5 nsec max for 550- to 1000-nsec models. In a 14-pin DIP, the lines are compatible with automatic-insertion equipment. The operating range spans 0 to 70°C. EP8301 50-nsec model, $4 (1000). Delivery, stock to six weeks ARO.

PCA Electronics Inc, 16799 Schoenborn St, Sepulveda, CA 91343. Phone (818) 892-0761.

Circle No 374



DISPLAY SYSTEM

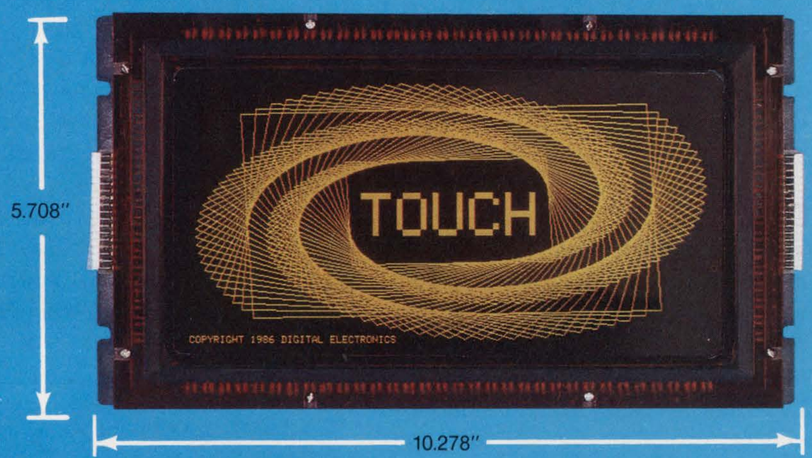
- *Offers 1200 to 9600 baud rates*
- *100,000-hour display life*

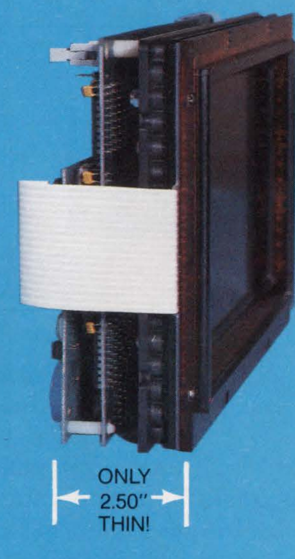
The VF-0640-01 is a 6-line×40-character vacuum-fluorescent display subsystem that features 0.2-in.-high characters. The display brightness specs at 175 fL, and data rates range from 1200 to 9600 baud. The unit displays several fonts: 96-character standard ASCII, ECMA, Katakana, scientific, European, and custom. Built-in software features include dimming, scrolling modes, and blinking characters. The system accepts both TTL-level parallel or serial ASCII input data. Operation spans 0 to 55°C, and the viewing angle is 130°. The display life specs at 100,000 hours. High refresh and data-entry rates prevent flickering.

SEALTOUCH™

PATENT PENDING

A **SEALED** I/R TOUCH DISPLAY MODULE SO FAR ADVANCED YOU HAVE TO SEE IT TO BELIEVE IT!





FULLY INTEGRATED 512x256 MATRIX EL DISPLAY MODULE INCLUDES I/R SEALTOUCH AND GRAPHICS/TEXT TERMINAL CONTROLLER.

- One-piece molded I/R frame and integral bezel/filter.
  - Flush mounts in your front panel cutout.
  - Sealable from moisture and dirt — antiglare, scratch-resistant, polarized filter included.
- Low power requirement — 20 Watts typical, requires only +5, +12 vdc input.
- Minimum footprint, compact cube.
  - I/R touch frame fits within display panel frame outline.
  - Ultra-compact module occupies minimum space. See dimensions above.
  - Flat display screen and flat touch plane eliminates parallax.

ENHANCED OPERATIONAL FEATURES ASSURE MAXIMUM PERFORMANCE AND DESIGNER EASE!

- **NEW "FTS" GRAPHICS:**
  - Dual processor architecture gives highest graphics performance in the industry.
  - Fast — 2400 vectors/sec., 4 million pixels/sec. (block fill).
  - Convenient interfaces — serial, parallel, raster, DMA, keyboard.
  - ASCII encoded.
- **VT100* TERMINAL EMULATION:**
  - VT100* based text capability.
  - No hand-shaking required at 19.2K baud.
- **EXPANDED TOUCH SOFTWARE:**
  - High resolution.
  - Automatic button draw and button pages.
  - Pop-up menus.
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  - Software compatible with earlier DeeCO systems.
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*VT100 is a Trademark of Digital Equipment Co.

CIRCLE NO 70

The display comes with an onboard μP controller; an RS-232C input is available as an option. $776 (99).

Babcock Display Products Inc, 1051 S East St, Anaheim, CA 92805. Phone (714) 491-5116.

Circle No 375

PANEL METER

- *1-μV/count resolution*
- *Serial BCD output optional*

Model 2002-S is a 4½-digit panel meter designed for strain-gauge, load-cell, and torque-monitoring applications. Standard features include a jumper-programmable differential preamp, which provides resolution down to 1 μV/count; an adjustable, electrically floating 10 to 24V dc bridge-excitation supply; and independent bridge-balance, zero, and span adjustments for direct readout in engineering units. The display spans ±19,999 counts with 99.98% accuracy. The 2002-S fits a standard ⅛-DIN panel cutout. Options include serial BCD output and a splash-proof lens cover that conforms to NEMA-12 requirements. $279.

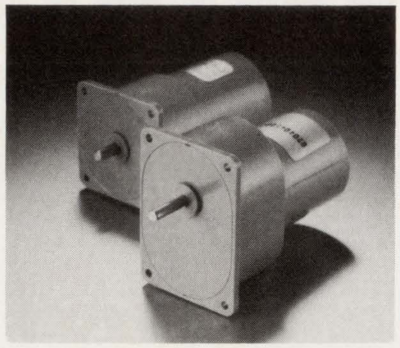
Newport Electronics Inc, 630 E Young St, Santa Ana, CA 92705. Phone (714) 540-4914. TWX 910-595-1787.

Circle No 376

DC MOTORS

- *Feature integral shaft-tachometer or -encoder fixture*
- *Ironless rotors for low inductance*

These cylindrical-collector, ironless-rotor dc motors now offer a choice of



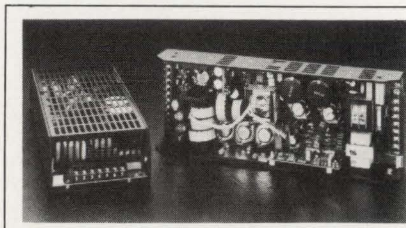
a dc tachometer, a frequency tachometer, or a fixture that accepts a shaft encoder. These options make them suitable for variable-speed, constant-speed, and position-control applications, respectively. The 66-mm-diameter motors are available with supply voltages of 12 or 30V nominal. They operate at approximately 2000 rpm, have a torque of 120 mNm (milli-Newton-meters), and feature a mechanical time constant of 17 msec. The sample price is around $46. Delivery, 12 weeks ARO.

Philips Elcoma, Box 523, 5600 AM Eindhoven, The Netherlands. Phone (040) 757005. TLX 51573.

Circle No 377

Airpax, Cheshire Industrial Park, Cheshire, CT 06410. Phone (203) 272-0301.

Circle No 378



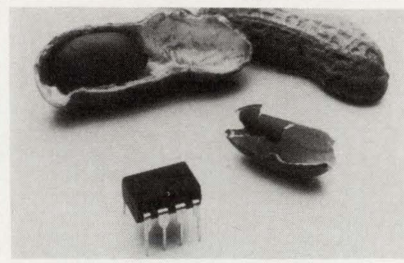
SWITCHING SUPPLIES

- *Typical efficiency equals 75%*
- *Meet FCC/VDC, level A specs for EMI*

The QX Series of switching power supplies includes units that have output capabilities of 250 to 325W, with as many as five outputs, including a 50A main output. All models have fully regulated outputs for reduced soft-error rates, jumper-programmable input-voltage range selection, and input surge-current limiting; protective features include brownout, overload, overvoltage, and reverse voltage. The typical efficiency is 75%. Standard features include a 20-msec holdup time, remote sensing, and remote inhibition. Options include a power-fail signal, an EMI safety cover, remote on/off, and thermal-shutdown switches. The supplies have UL, CSA, and TUV approvals and meet FCC/VDC, level A specifications for EMI. $299 to $338 (100).

Cherokee International Inc, 8 Autry, Irvine, CA 92718. Phone (714) 951-9679. TWX 510-101-0493.

Circle No 379



FET DRIVER

- *Patented photovoltaic IC provides fast turn-off*
- *Housed in an 8-pin DIP*

Offering a significant reduction in drive-circuit complexity, board space consumed, and cost, the FDA200 converts a TTL- or CMOS-level current input into a 12 or 14V output that drives discrete MOSFETs. This driver incorporates a patented photovoltaic IC that includes a gate-clamping circuit for fast turn-off. You can operate the unit's two optically isolated outputs in series, in parallel, or independently; this operation drives ac or dc loads. The driver performs over a −40 to +85°C range and comes in a standard 8-pin DIP. $4.20 (1000).

Theta-J Corp, 107 Audubon Rd, Wakefield, MA 01880. Phone (617) 246-4000.

Circle No 380

Anritsu Presents Spectrum Analysis That's Simply Unforgettable

MS710C Spectrum Analyzer

No more writing down results. No more sketching waveforms on paper. No more grease pencil graphics on the CRT grid. Why?

Because Anritsu's new MS710-series Spectrum Analyzers actually *remember* display screens for you – up to nine of them, in fact. Each one complete with waveforms and comprehensive alphanumeric information such as frequency, level, etc. Each one ready for recall to the CRT at the push of a button. Check and recheck, contrast one with another, even compare the current real-time waveform to a standard in memory. It's like having a file of waveform information always at your fingertips. Frequency range is wide, too; for instance, our new MS710C covers the range from 10kHz to 23GHz (or up to 140GHz with an external mixer). It offers signal search functions, along with an ergonomic front panel that puts every control right where it's needed. A special display lists key functions right on the screen: it's virtually a built-in operator's manual!

Can't get the MS710C out of your mind? Contact Anritsu for further details.

Spectrum Analyzer	Frequency Range	Frequency Stability (6.5GHz)	Frequency Range with External Mixer
MS710C	10kHz~30MHz, 100kHz~23GHz	30kHz	18~140GHz
MS710D	100kHz~23GHz	1MHz	18~140GHz
MS710E	100kHz~23GHz	30kHz	–
MS710F	100kHz~23GHz	1MHz	–

Anritsu

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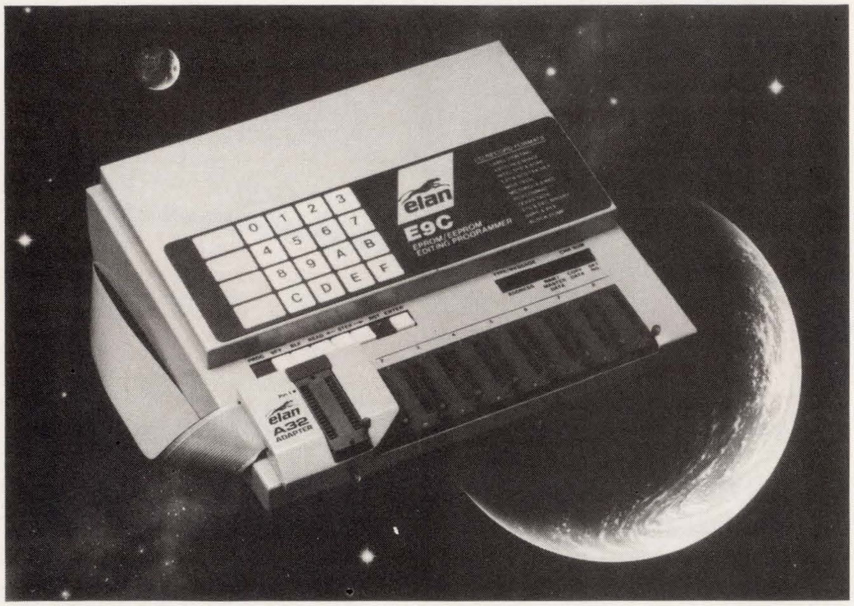
CIRCLE NO 51

TEST & MEASUREMENT INSTRUMENTS



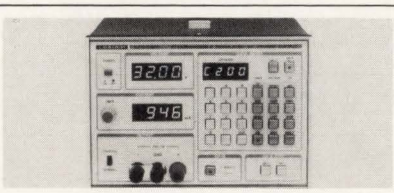
PROGRAMMERS

- *Program 1M-bit and one-time-programmable devices*
- *Implement EPROM manufacturer's recommended algorithms*

These EPROM/EEPROM programmers, Models E8B, E9C, E12B, and C41, are now capable of programming 28- and 32-pin 1M-bit devices. They can now also program Intel one-time-programmable devices using Intel's Quick-Pulse Programming algorithm. Using the E8B or E9C, you can now program as many as eight 27512, 27513, or 27011 EPROMs while still performing automatic access-time testing of the devices. Also available is the A32, a 28- to 32-pin adapter that allows programmers with 28-pin sockets to program and verify the 32-pin 27010, 27C001, and 27C101 1M-bit devices. Upgrades start at £150.

Elan Digital Systems Ltd, 16-20 Kelvin Way, Crawley, West Sussex RH10 2TS, UK. Phone (0293) 510448. TLX 877314.

Circle No 390



DC POWER SUPPLY

- *Stores 200 settings internally*
- *Supplies 0 to 32V at 1A*

The LPS-2801 programmable dc power source supplies 0 to 32V at 1A. You can program output-voltage changes in 10-mV increments over time periods ranging from 10 msec to 99.99 sec. The device's slew rate ranges from 100 μV/sec to 3200V/sec. You can control the device manually or over the IEEE-488 bus. The source stores as many as 200 settings internally; you can program each setting to produce either a steady dc voltage or a ramp. $1940.

Leader Instruments Corp, 380 Oser Ave, Hauppauge, NY 11788. Phone (800) 645-5104; in NY, (516) 231-6900. TWX 510-227-9669.

Circle No 391

EMULATORS

- *Plug into IBM PC*
- *Versions available for 8- and 16-bit μPs*

The ERX Series μP emulators each comprise a board set and a personality module for a specific μP. The board set consists of either two boards for 8-bit μPs or three boards for 16-bit μPs. The boards plug into IBM PC slots or slots in the company's Boxer computer. Personality modules are currently available for the Hitachi 6301 and 64180 and the Zilog Z80. An 8-bit board set costs $2995; each personality module is $2995.

Zax Corp, 2572 White Rd, Irvine, CA 92714. Phone (800) 421-0982; in CA, (714) 474-1170.

Circle No 392

CALIBRATOR

- *Handheld instrument weighs 14 oz*
- *Unit generates stimulus and measures output*

The CL-2241 frequency calibrator is a handheld unit. It generates test signals having frequencies ranging from 0.3 to 163 Hz. The instrument also measures signals ranging from 0.1 Hz to 200 kHz, 4 cpm (cycles per minute) to 2k cpm, and 20 cph (cy-

cles per hour) to 20k cph. The unit measures 6×3×2 in. and weighs 14 oz. It operates from a 9V battery or an ac adapter. $475.

Rochester Instrument Systems Inc, 255 N Union St, Rochester, NY 14605. Phone (716) 263-7700.

Circle No 393

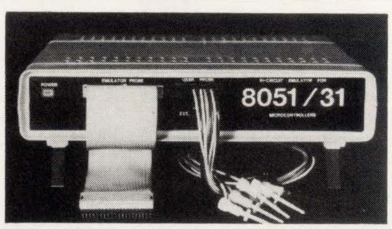
RS-232C ANALYZER

- *Converts baud rates*
- *Captures message streams to 32k bytes*

The Datamon portable RS-232C analyzer weighs 7 lbs, including accessories and a standard carrying case. You can record message streams as long as 32k bytes and view them in several formats on a dumb terminal. The device provides status LEDs for RS-232C lines and baud-rate conversion. $795.

Standard Logic Inc, Box 2319, Corona, CA 91720. Phone (714) 735-8610.

Circle No 394



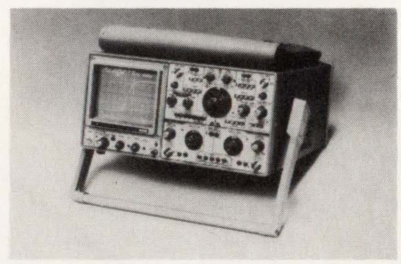
8051 EMULATOR

- *Emulator runs at a 12-MHz clock speed*
- *Qualifies breakpoints by address range, data, and cycle*

The 8051/31 in-circuit emulator for 8051-family single-chip μPs runs at clock rates as high as 12 MHz. It works with either a dumb terminal or an IBM PC. The emulator has 128k address breakpoints, a 2k-sample trace buffer, and 64k bytes of mappable program memory. The emulator also has an 11-bit event counter, an external-trigger input, and an internal-trigger output. The emulator's command monitor provides single stepping, in-line assembly and disassembly, and control of the μP's internal registers. You can qualify breakpoints by address or address range, data, program-cycle type, and external inputs. $3195.

IAM, Bóx 2545, Fair Oaks, CA 95628. Phone (916) 961-8082.

Circle No 395



PORTABLE SCOPES

- *Display four traces*
- *Accept references for ratiometric measurements*

The SS-6122 100-MHz and SS-6611 60-MHz portable oscilloscopes each have a 6-digit reciprocal counter. Each of the 4-channel scopes also has four on-screen cursors. The cursors can automatically track the 10 to 90% excursions of a waveform. Besides displaying the usual measurement readouts, the screen can show comments, such as the measurement setup, the contents, and the operator's name. The comments can be as long as 80 characters. The screens also show the date and time. The scopes can display ratiometric measurements referenced to previously entered voltage and time values. SS-6122, $2295; SS-6611, $1795.

Iwatsu Instruments Inc, 430 Commerce Blvd, Carlstadt, NJ 07072. Phone (201) 935-5220.

Circle No 396

Precision High Voltage Resistors and Resistor Networks from CADDOCK for high performance, high voltage systems.

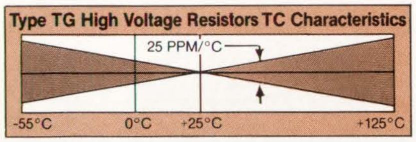
Type TG Low TC Precision High Voltage Resistors with a TC of 25 PPM/°C from -55°C to +125°C and resistance values to 1,000 Meg.

Constructed with Caddock's Tetrinox® resistance films to achieve exceptional temperature and loadlife stability, the Type TG high voltage resistors are ideal for the precision circuitry of TWT power supplies, electron microscopes, X-ray systems, high resolution CRT displays and geophysical instruments.

The Type TG resistors deliver this outstanding combination of performance specifications:

- Temperature Coefficient of 25 PPM/°C from -55°C to +125°C.

Type TG High Voltage Resistors TC Characteristics



- Resistance range from 1 Meg. to 1000 Meg.
- Resistance Tolerances from 1.0% to 0.1%.
- Loadlife Stability of 0.25% per 1000 hours.
- Voltage ratings up to 48,000 volts.
- Max. Continuous Operating Temp. of +225°C.
- Exclusive Non-Inductive Performance.

plus - Matched Resistor Sets with Low Ratio Temperature Coefficient Tracking Performance.

The Type TG resistors can be used in combination with the low TC of Caddock's Type TK Low TC Precision Radial-Lead Resistors to achieve 30 PPM/°C Ratio TC without special matching.

With special matching, a Ratio TC of 10 PPM/°C can be achieved.

- **For Type TG data, circle Number 101.**

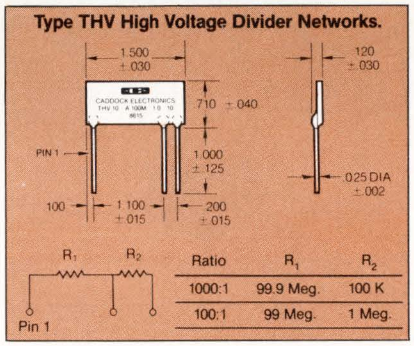
Type THV Thin-Profile 10 KVDC Precision Resistor Voltage Divider Networks with Ratio TCs to 10 PPM/°C from -55°C to +125°C.

Caddock's advanced high voltage resistor technology combines our high stability Tetrinox® resistance films with laser-generated V-Notch Geometry (Pat. Pend.) to produce this compact high voltage divider network.

The performance of these high stability networks includes these special features:

- Standard Input Resistance of 100 Megohm with custom resistances available.
- Standard Voltage Division Ratios of 1,000:1 or 100:1 with custom ratios available.
- Ratio Tolerances of 0.25%, 0.5%, 1.0% or 2.0% at 10 KVDC.
- Ratio Temperature Coefficients of either 10 PPM/°C or 25 PPM/°C from -55°C to +125°C.
- Non-Inductive Performance.
- Thermal coupling between the resistors in this single-substrate network provides excellent Ratio Temperature Coefficient stability.

Type THV High Voltage Divider Networks.



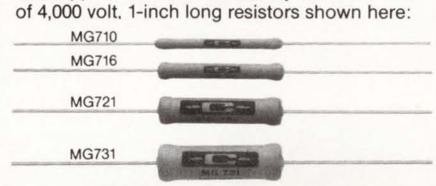
Ratio	R_1	R_2
1000:1	99.9 Meg.	100 K
100:1	99 Meg.	1 Meg.

- The thin-profile and 1.5 inch body length provides for easy packaging in space-sensitive designs.

- **For Type THV data, circle Number 102.**

Type MG Precision High Voltage Resistors with extended resistance range to 10,000 Megohm and a TC of 80 PPM/°C.

For greater **design flexibility**, Caddock's 'family' of Type MG resistors has been expanded with additional models and now includes 23 models that permit designers to select the optimum resistor size, power rating and voltage rating for each application, as illustrated by the four models of 4,000 volt, 1-inch long resistors shown here:



The Type MG high voltage, high stability resistors include all of these performance specifications:

- Standard Temperature Coefficient of 80 PPM/°C.
- Resistance values to 10,000 Megohm.
- Resistance Tolerances from 1.0% to 0.1%.
- Loadlife Stability better than 0.8% per 1000 hours.
- Voltage ratings up to 48,000 volts.
- Max. Continuous Operating Temp. of +225°C.
- Exclusive Non-Inductive Performance.

Most models of these high voltage resistors are manufactured with Caddock's Exclusive Non-Inductive Design for improved performance in high frequency, pulse and wide-band circuits.

- **For Type MG data, circle Number 103.**

Caddock's new 28-page General Catalog describes over 200 models of standard and custom precision and ultra-precision resistors and resistor networks. For your personal copy, call or write our main offices at -

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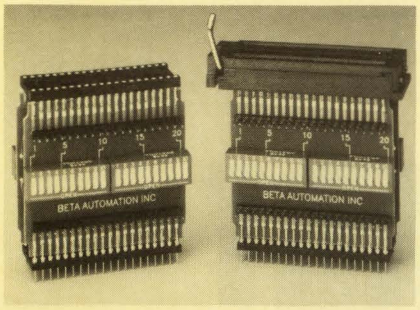

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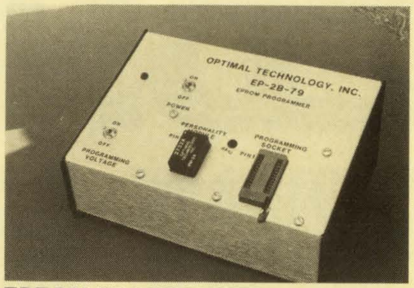
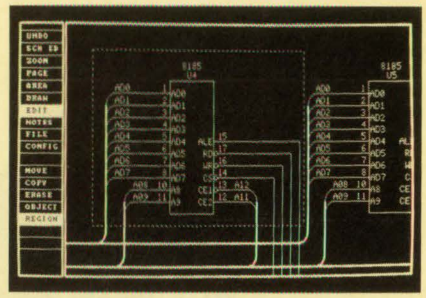


EPROM PROGRAMMER

MODEL EP-2B-79 with software MS-DOS, CP/M, Apple, Atari Pet, AIM-65, SYM-1, VIC-20, C-64, H-8, H-89, SS-50, TRS-80 (1&3), and S-100. Programs 2708, 2716, TMS2716, 2732, 2732A, 2532, 2764, 2564, 27128, 27128A, 27256, 27512 and MCM68764 EPROMs; 2816A, 2864A, EEPROM; 8751, 38E70 8748 MPU Price $179 with personality modules $17 to $35, Software $21 to $40.

Optimal Technology
Earlysville, VA 22936
804-973-5482

CIRCLE NO 332



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CIRCLE NO 334

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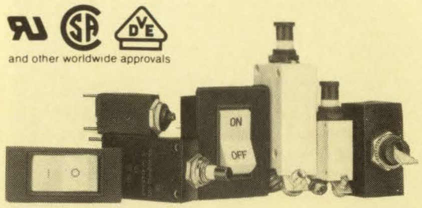
and other worldwide approvals



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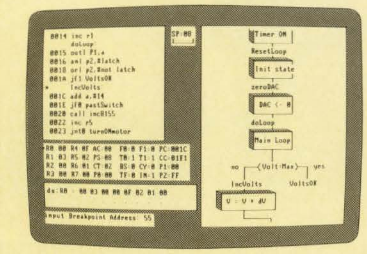
Simulator/Debugger for IBM-PC for 8048 - 8051 - 8096 μCs



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	8048	8051	8096	7000	
X-Assembler	✓	✓	✓	✓	$295
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Simulator*	✓	✓	✓	✓	$595

Demo disk and manual for simulator only $39.50

*8096 Simulator — $995

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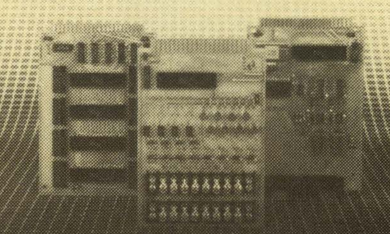
(415) 726-3000 • Telex 171-135 Attn: Cybernetics

CIRCLE NO 337

6800/6809 Micro Modules



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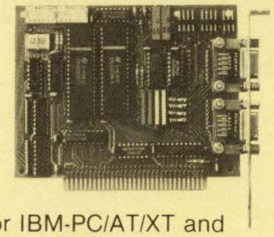

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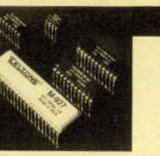

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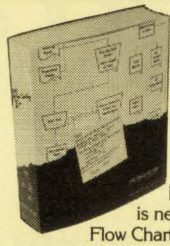

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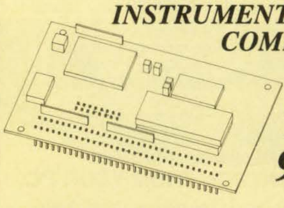

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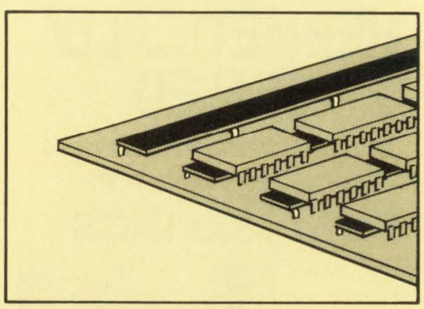

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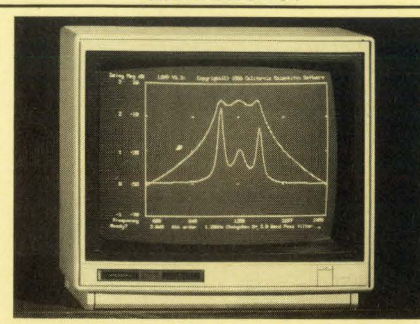

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Datagraf Inc, 8305 Highway 71 West, Austin, TX 78735.

Circle No 397

Guide to Macintosh software

The winter edition of *MacGuide* contains an up-to-date listing of more than 2000 programs that are available for the Apple Macintosh. For each software package, the publication includes product name, vendor name, suggested retail price, and program description. $4.95; $1 for shipping and handling.

Menu, 1520 S College Ave, Fort Collins, CO 80524.

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Wall chart depicts PLDs

This wall chart provides a convenient reference to all types of programmable semiconductor devices. It's divided into sections that tabulate all PLDs, EPLDs, GALs, bipolar and CMOS PROMs, EPROMs, EEPROMs, and microprocessors. The information listed includes programmable-array size, the number of pins, and the company's identifier code for each device.

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Data sheet details fault-tolerant computers

This preliminary data sheet covers 200/400XR Series fault-tolerant computers and how they bring fault tolerance into the supermicrocomputer and minicomputer price range. Along with block diagrams and a black-and-white photo, the 6-pg publication gives an overview of system operation, lists optional communications interfaces, describes the different configurations, and devotes an entire page to complete specifications.

Parallel Computers Inc, 3004 Mission St, Santa Cruz, CA 95060.

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Catalog presents interconnect devices

This 84-pg catalog features the company's line of interconnection products. The sockets and adapters are available in SIPs, DIPs, zig-zag configurations, and over 150 low-insertion-force, pin-grid-array footprints. In addition, you can order them with standard glass-filled molded polyester, high-temperature Rynite, and FR-4 fiberglass epoxy; you can order the Peel-A-Way terminal carriers in Mylar or Kapton. The catalog covers such new products as hybrid sockets with surface-mounted components, single- and dual-beam connectors, multilayer wire-wrapped boards, and surface-mount decoupling capacitor sockets. Request *Catalog #7*.

Advanced Interconnections, 5 Energy Way, West Warwick, RI 02893.

Circle No 401

Test-and-measurement accessories cataloged

Publication No 5954-0193D describes this company's test and measurement accessories that are available in the US by phone order for same- or next-day shipment. The catalog is organized into four sections: accessories and cables, rack mounts and cabinets, supplies, and instruments. It lists products alphabetically, numerically, and by equipment reference. The catalog also contains selection guides, flow diagrams, and compatibility charts to help you find the right products for a particular application.

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303.

Circle No 402

Directory for software

A group of software publishers have cooperated in putting together this 16-pg newspaper. It describes each business-oriented software package with enough detail to make a purchasing decision. Participants include the following companies: Turner Hall Publishing, Software Concepts, Polytron, Rocky Mountain Software Systems, Spectre Technologies, North Edge Software, Permar & Associates, DGH Software, Bruce & James, Olympus Software, and Maxthink.

Cooperative Software Catalog, 1641 S Lansing St, Aurora, CO 80012.

Circle No 403

Newsletter covers μP development system

A quarterly newsletter discusses topics of interest to users of microprocesser development systems (MDSs) for 64180, 6301, and 8051 μP projects. This 6-pg issue features an article comparing the cost and performance of PC-based MDS tools vs traditional mainframe MDSs. In addition to including selected application notes, the paper lists and briefly describes other application notes available upon request.

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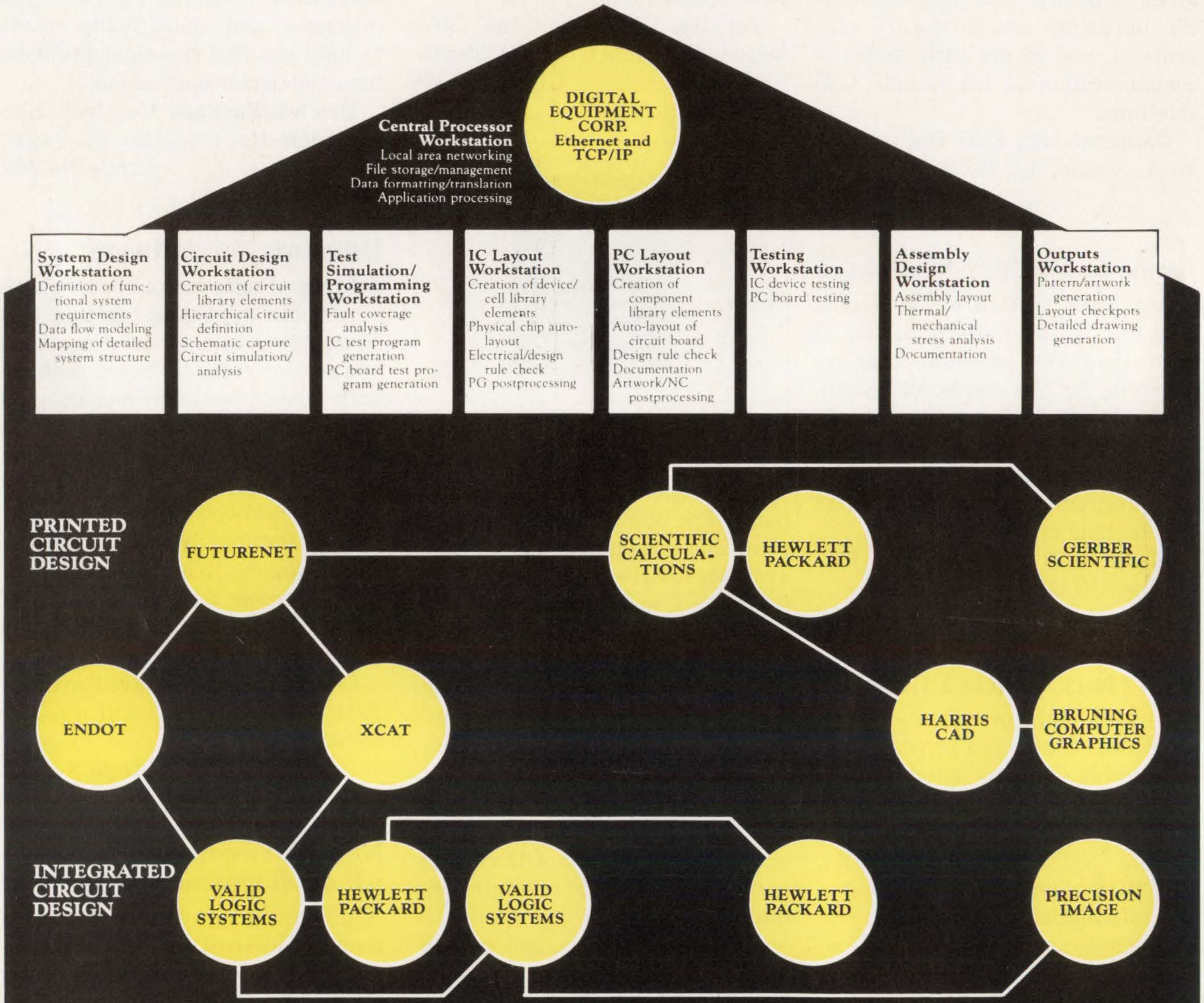

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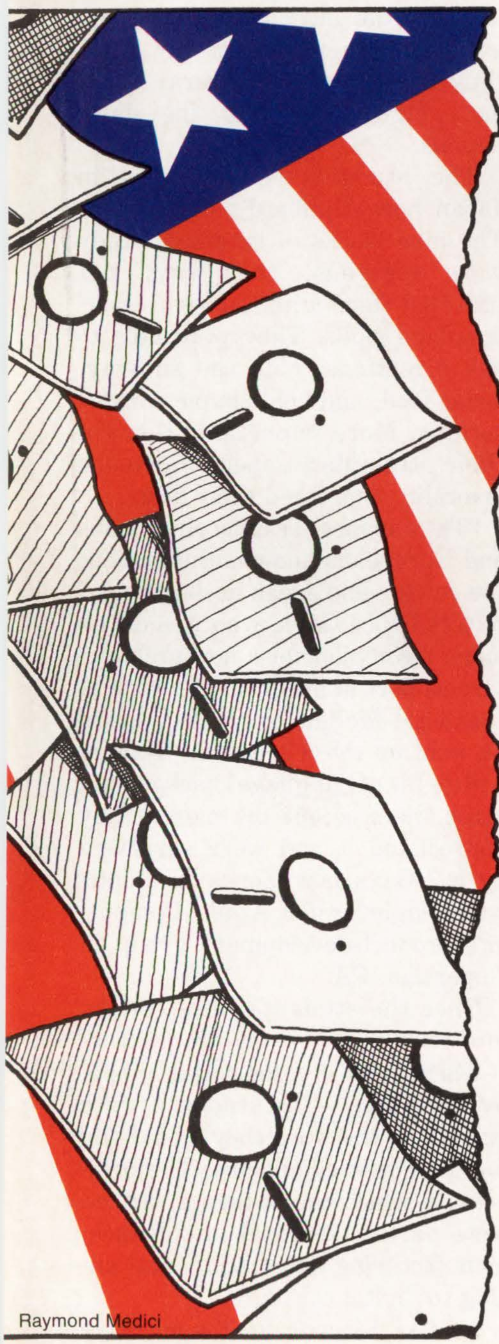
A study in contrasts: US engineers recall their visit to Japan

Deborah Asbrand, *Associate Editor*


Raymond Medici

While on a fellowship in Tokyo, Anderson Howard, a US graduate student in electrical engineering, attended a conference of Japan's Institute of Electrical and Communications Engineers. He expected it to be similar to large American technical conferences that he had attended. But what Howard found at the Japanese conference surprised him. Instead of presenting a program of about 200 presentations, each lasting 30 to 45 minutes, the Japanese conference featured 2800 presentations, each lasting 15 minutes.

The goal of Japanese professional societies at their technical conferences, Howard discovered, is to give attendees a broad sample of ongoing technical research. American conferences, on the other hand, generally cover a narrower range of technology in greater detail.

This dissimilarity between the American and Japanese engineering communities was just one of the differences Howard noted during his stay in Japan three years ago. Howard's 8-month visit was sponsored by the American Electronics Association's Japan Fellowship Program, a 3-year-old venture that sends American students to work for Japanese companies. With few other programs offering similar opportunities, the AEA fellows who subsequently enter the US electronics workforce become members of a small group: US engineers with firsthand knowledge of Japanese engineering practices.

The members of the first AEA-sponsored contingent, which included Howard and five others, currently work for such American electronics concerns as Hewlett-Packard, Apple Computer, Daisy Systems, and Westinghouse Electric. Having now worked two years for their US employers, they can attest to differences between the two countries' engineering education, industry training, and job responsibilities. But the greater distinctions, they say, lie in each country's cultural nuances.

What prompted the AEA to initiate the program was not a need to explore cultural nuances, but a need to address serious economic problems between the US and Japan, and to offer a way to ease the resulting tensions. In 1983, with trade between the US and Japan climbing to record imbalances in Japan's favor, concern about the trade deficit was increasing among US electronics companies. The AEA, which represents more than 2800 US electronics companies, decided that a cooperative venture between US and Japanese companies would be a welcome gesture towards smoother relations between the US and Japan, says Pat Hill Hubbard, the AEA vice president of engineering and management education.

A deficit of another kind also was a factor in the association's decision to sponsor a fellowship program. "The Japanese were sending about 400 engineering students each year to study in US universities, while the US was sending about seven students to study in Japan," Hubbard says. "They were learning all about us and we weren't learning anything about them." The real goal of the fellowship program, Hubbard says, became one of introducing more US engineering students to Japanese culture.

An important aspect of learning about Japan's culture, Hubbard believed, included studying the complex Japanese language. Hubbard says that some supporters of the program chafed at this proposal, noting that the study of English is a requirement in Japanese schools, and that, as a result, most Japanese workers have at least a passing familiarity with the English language. Consequently, the AEA fellows would be able to communicate with their Japanese counterparts well enough to get by with no special training. Hubbard, however, disagreed.

"As we began to research the program, one of the problems we saw was the differences in the cultures. Culture is reflected in language. We wanted the students to establish long-term relationships with their coworkers that would be above trade politics." Hubbard's persistence has paid off: Before leaving for their Japanese assignments, AEA fellows spend nine weeks in an intensive Japanese-language class at Cornell University. There, they spend six hours each day listening to native Japanese speakers, participating in conversation drills, and learning the intricacies of the language. To keep up with the class, they usually spend several hours each night reviewing the day's lessons.

The students' experiences in Japan bore Hubbard's theory out. The nine weeks of language study were rigorous, they say, but provided them with "survival level" language skills. They were able to ask directions, ride the subway, order food, and hold simple conversations. More important, though, their attempts to speak Japanese favorably impressed their hosts.

"The Japanese assume Americans and Europeans know nothing about the culture and speak no Japanese," recalls Bruce Gaya, who was developing a compiler for a new architecture as part of his graduate work at Carnegie-Mellon University when he went on the fellowship. "Having a little bit of [language] background made them accept me more. They appreciated it and were surprised by it." Gaya now works as a software engineer for Apple Computer's product-development group in Cupertino, CA.

Once the students were settled into their Japanese living quarters —which in most cases was a company dormitory—the students were briefed on the work they'd be doing for their host companies. The projects on which the students worked were varied: artificial intelligence, manufacturing automation, and analog-to-digital conversion.

At Oki Electric in Tokyo, Gaya

How the Japan Fellowship Program operates

The American Electronics Association Japan Fellowship Program has sponsored 26 students since its inception in 1984. The program is open to all US graduate students in electrical and computer engineering or computer science. Once selected as fellows, the students are matched with Japanese host companies based on mutual technical interests. Students work for their Japanese hosts for nine months to one year.

The program is jointly funded by American and Japanese electronics companies. American companies' contributions pay for the students' tuition and expenses while enrolled in an intensive 9-week language class at Cornell University. The Japanese host companies, which have included Sony Corp, Fujitsu, Hitachi, and Oki Electric, pay for the students' travel, housing, food, books, and research materials, and they offer a monthly stipend. In addition, a grant from the National Science Foundation matches contributions from US supporters.

worked with Japanese engineers on an artificial-intelligence research project. Gaya's colleagues were intent on learning more about software, an area to which they ceded American superiority. "They felt that in the area of chips and hardware, Japan was better," he says. "But they felt American software and artificial intelligence were far superior. They wanted to work hard to catch up and develop an artificial-intelligence capability at Oki."

Education and training

The engineers with whom Gaya worked were technically astute, he says, but their training differed from that of most American engineers. "My group wasn't trained as engineers," he says. "They were trained as scientists, and they came to Oki and learned [engineering] there. [My coworkers'] software skills weren't that great. Japan as a whole is lacking good software."

Because of their scientific backgrounds, Japanese engineers are less specialized than American engineers, says Jeff Funk, a senior engineer at Westinghouse Electric's research and development laboratory in Pittsburgh, PA. "In Japan, the university education is generalized. When they join a company, Japanese engineers receive a great deal of training. Their responsibilities are broader than American engineers'. When Japanese engineers design a product, for example, they're forced to talk to manufacturing people when they're designing." Funk traveled to Japan upon completion of his doctorate degree in engineering and public policy at Carnegie-Mellon University in Pittsburgh. In Japan, he studied factory automation and visited the factories of 15 companies.

Anderson Howard's association with Japanese engineers dispelled for him the notion that Japanese technology is secondhand. "Before I went over, I had the impression that the Japanese just copy Americans and don't do basic research," he says. "But it's apparent that they conduct a lot of basic research now. They're sensitive to the feeling that their technology is inferior, and they hate being thought of as copycats. They want to be thought of as world-class leaders in technology."

Howard adds that competition among Japanese companies is intense. A likely cause of such rivalries is the nation's seemingly tireless interest in electronics, evident in the akihabara, the section of Tokyo where hundreds of consumer-electronics vendors line the storefronts. Howard, too, succumbed to the excitement of the district, purchasing a pair of stereo speakers and a Walkman radio while he was there.

Japanese engineers "felt that in the area of chips and hardware, Japan was better. But they felt American software and artificial intelligence was far superior."

Mastering Japanese etiquette

The greatest differences between American and Japanese engineers, the men noted, were in their relationships with their respective employers. In Japan, the boundaries of acceptable and unacceptable behavior are rigid by comparison with US standards.

Gaya inadvertently discovered the importance of remaining within those boundaries. Interested in extending his stay in Japan, he began negotiating with his supervisors at Oki Electric. He soon found that, among his engineering peers, his engagement in a time-honored American custom—haggling over salary—was a faux pas by Japanese standards.

"I had one colleague come up and say 'How could you ask for more money? This is terrible!'" Gaya remembers. "There's a whole feeling that the company is like your mom and dad. If the company says something, you do it. They feel they must serve the employer. Your own desires and wishes are nothing compared to what's good for the company." Now working in Silicon Valley, Gaya marvels at the different credo he finds among the valley's workers: "Here, people stay with the job as long as it's good for them. There's little loyalty to the company, only to yourself."

At NEC, where Howard worked while in Japan, the work environment combined a measure of flexibility with rigid guidelines. To help employees better accommodate their family's schedules, the company allows them the choice of beginning work each day at 8:30, 9:00, or 9:30 am. Yet arriving even one minute late exacts a stiff penalty upon employees: They owe the company one half hour of overtime as compensation. As a result, Howard says, "It wasn't uncommon to see people running from the train station in their suits to arrive at work on time."

Japanese Bandstand

Company-sponsored festivities, however, were common. To strengthen the family-like bonds between the company and its employees, attendance at company parties is limited to employees—no family members are welcome. Invited to one such party after working at NEC for just one month, Howard was asked to make a speech and sing before the 50 celebrators in attendance. He was reluctant to address the crowd but aware that the invitation was an honor and not to be declined. Gamely, he gave a short speech and then sang "Yesterday" by the Beatles. When his coworkers called for an encore, he followed with a rendition of a song

ISSUES

popular with many Japanese, "I Left My Heart in San Francisco."

Now employed by Hewlett-Packard as a development engineer, Howard continues to correspond with Japanese friends, and last year he was visited by three NEC researchers. To maintain his language skills, he watches a local Japanese television news broadcast each night. He has given talks on his experiences in Japan for Hewlett-Packard and for the AEA. In his talks, he says, "I've helped to open people's eyes about what Japan is like. I've encouraged them to study the language."

> *The Japanese are "sensitive to the feeling that their technology is inferior, and they hate being thought of as copycats. They want to be thought of as world-class leaders in technology."*

Indeed, his study of the language has provided him with a distinct professional advantage: Now able to read Japanese, he can explore Japanese electronics journals for research and development information. And it's this type of reciprocation that may bring a greater understanding between the two cultures: Gaya reports that the Japanese engineering community has long recognized the importance of reading English. At Oki Semiconductor, his engineering group had two translators whose only job, he says, was to "search through American journals and cut out articles for the engineers to read." Turnabout is fair play. **EDN**

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1987 Editorial Calendar and Planning Guide

EDN

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Apr. 30	Apr. 9	Communications Special Issue; ASICs; Test & Measurement
May 14	Apr. 23	Analog Technology Special Issue; ICs; Test & Measurement
May 28	May 7	Computer Peripherals; Software; Power Sources/Devices
June 11	May 21	Math ICs; CAE; Computers
June 25	June 4	ASIC (Semicustom ICs) Directory; Analog ICs; Surface-Mount Technology
July 9	June 18	Product Showcase-Volume 1; ICs & Semiconductors; Software
July 23	July 2	Product Showcase-Volume II; Computers & Peripherals; Test & Measurement Instruments
Aug. 6	July 16	Computer Boards; Digital Signal Processing; Test & Measurement; Top Ten Reader Vote Contest
Aug. 20	July 30	Military Electronics Special Issue; Fiberoptics; Software

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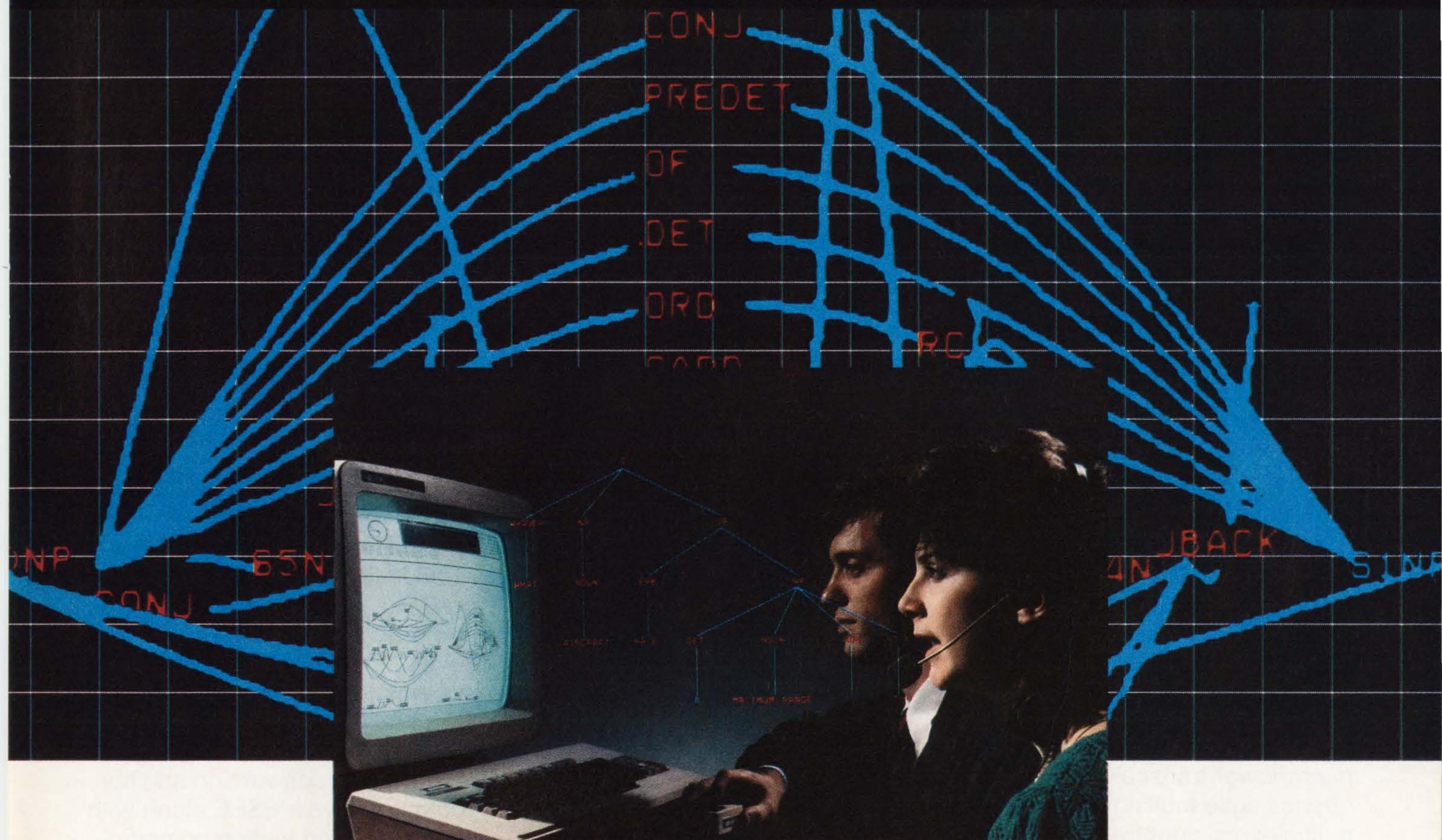

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PRODUCTS

DSP Board Fits IBM PC

GE/Intersil's EVK-128 combines A/D conversion and FIR filtering

JEFF HAIGHT
GE/Intersil Inc.

As digital signal processing becomes simpler, cheaper, and more pervasive, the boundaries between design ideas and design techniques must give way for a more integrated approach to system development. Intersil's EVK-128 board, which occupies one slot in an IBM PC, incorporates analog design and digital signal-processing techniques.

The board works in such applications as PC-based analog or digital data-acquisition and digital filtering systems, finite-impulse-response (FIR) filter design and development systems, or as part of an FIR filter processor for off-line or non-real-time data.

The EVK-128 provides signal-processing hardware and FIR-filter design and modification software. You can copy all or part of the system for use in your own signal processor.

TECHNOLOGY

Power MOSFET Mak...

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The focus of EDN News is on hot products that will have the most powerful impact on the way you do your job. EDN News covers the best products on the market, how they evolved, and why. Plus, it now covers the industry events that drive product technology and hence product introductions.

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In a separate section, EDN News keeps you abreast of professional developments and job openings in the electronics field. It carries editorial aimed at your career and professional growth. Editorial that will help you find a job and keep it.

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Annual growth rate is 10.2% for rectifier market

The US market for diode rectifiers, a market valued at $521.7 million in 1985, is expected to grow at an average annual rate of 10.2% for the next five years, according to the market-research company Venture Development Corp (VDC) of Natick, MA. By 1991, the value of US shipments of these products will be $932.7 million. VDC cautions, however, that this market growth is contingent upon improvements in diode-rectifier technology.

Specifically, manufacturers are focusing on improvements in packaging. The performance levels of many rectifier products—particularly standard and fast-recovery types—are essentially similar and meet the needs of large OEMs. Ease of mounting, power dissipation, reliability, size, spacing, thermal characteristics, hermeticity, total device cost—all these factors are predominantly determined by the package.

Plastic packages are most popular in low- and medium-current applications, and, in 1985, rectifiers housed in plastic or epoxy packages accounted for 45% of all rectifier sales. These packages often cost less, consume less board space, and are easier to mount than other package types. Manufacturers are continuing to improve the reliability and power dissipation of plastic, and VDC expects rectifiers in plastic packages to continue making gains in market share through the rest of the decade.

Glass-packaged axial-lead rectifiers offer greater current-carrying capacity than plastic axial-lead types, and metal-packaged stud-mounted rectifiers dissipate more power and are more reliable. The former will see healthy growth into the next decade, though cost is an important limiting factor. The latter are bulky and difficult to mount, and growth in that market segment will be sluggish.

MILESTONES IN THE DEVELOPMENT OF MOLECULAR ELECTRONIC TECHNOLOGY

1990	DEMONSTRATION OF MOLECULAR-SCALE SWITCHES AND MEMORY ELEMENTS. COMPUTER MODELING OF MOLECULAR-SCALE CIRCUITS.
1991	DEVELOPMENT OF TECHNIQUES FOR PREDICTING THE 3-DIMENSIONAL STRUCTURE NEEDED TO MAKE MOLECULAR-SCALE DEVICES USING A POLYPEPTIDE SEQUENCE FOR A SPECIFIC FUNCTION.
1994	SOLUTION OF THE CONNECTOR PROBLEM (LINKING A KEYBOARD TO AN INDIVIDUAL MOLECULE).
1998	CONSTRUCTION OF A MOLECULAR-SCALE ELECTRONIC CHIP OR 3-DIMENSIONAL ARRAY.
2000	INITIAL SALES OF MOLECULAR ELECTRONIC DEVICES AND COMPUTERS.
2010	SALES OF MOLECULAR ELECTRONIC DEVICES AND COMPUTERS REACH $1 MILLION.
2020	SALES OF MOLECULAR ELECTRONIC DEVICES AND COMPUTERS CONSTITUTE 1% OF THE TOTAL COMPUTER MARKET.
2050	SALES OF MOLECULAR ELECTRONIC DEVICES AND COMPUTERS CONSTITUTE 10% OF THE TOTAL COMPUTER MARKET.

(SOURCE: SEAI TECHNICAL PUBLICATIONS)

Molecular electronic devices to be commercial by 2000

According to several experts in molecular electronic technology, the development of that technology will yield computer modeling of molecular-scale circuits by 1990 and commercially available devices by the year 2000. The survey responses, collected and analyzed by Professor M Todd Jarvis of the Mississippi State University Department of Engineering and published by SEAI Technical Publishing (Madison, GA), also include predictions that sales of molecular electronic devices and computers will constitute approximately 1% of the total computer market by 2020.

Researchers in molecular electronics are seeking ways to significantly improve both computational densities and speeds. Some investigators believe that proposed chromophore chains for molecular chips could attain spacing improvements above the upper limits of silicon by a factor of 40. Other researchers see molecular electronics as issuing a new breed of analog computers for such applications as pattern recognition, correlations, and context-dependent decisions. Another potential approach combines molecular technology with biosensors for such medical applications as bionic implantations.

Scientists are investigating two principal approaches to the construction of molecular electronic circuitry. One approach would employ synthetic materials, such as polymers or charge-transfer salts. The other approach would use biological polymers—primarily proteins. Whichever approach proves more feasible, the experts polled seemed to think, molecular-scale ICs would be available at a much lower cost per element than today's ICs.

The actual device structures proposed thus far look astonishingly like their counterparts rendered now in silicon. Beyond the visual similarities, however, the construction of molecular-scale electronic devices poses some special challenges and difficulties: In one area, for example, scientists will have to face problems associated with the use of different materials, and in another, they may even have to consider new methods of signal transport.

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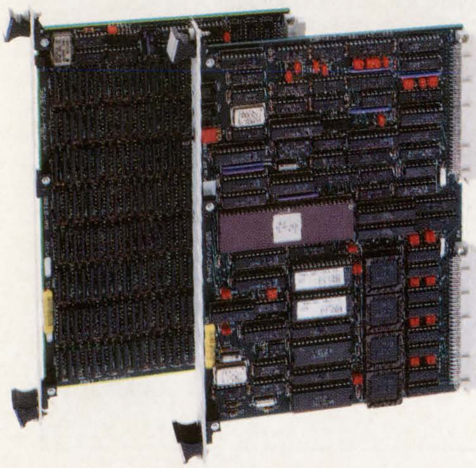

"VMEbus boards are just too damned expensive."
Tom Andersen
CEO, SBE, Inc.

New price/performance for VME. If you're building VMEbus systems, or thinking about moving up to VMEbus systems, this is good news: SBE is entering the VMEbus marketplace with two new boards. And new price/performance standards for the industry.

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SBE VMEM-4. 4 Megabytes of dynamic RAM for VME. At a price that's more than simply competitive. This new VME memory board from SBE works equally well with 16-bit and 32-bit processors and supports 8-bit, 16-bit and 32-bit aligned transfers. Plus, 32-bit unaligned transfers that free programmers from boundary alignments, greatly simplifying program design. **A note on price:** Presently, 256K RAM prices are extremely volatile. We're quoting stable bare-board prices plus RAM at our lowest spot price. Call for quotes.

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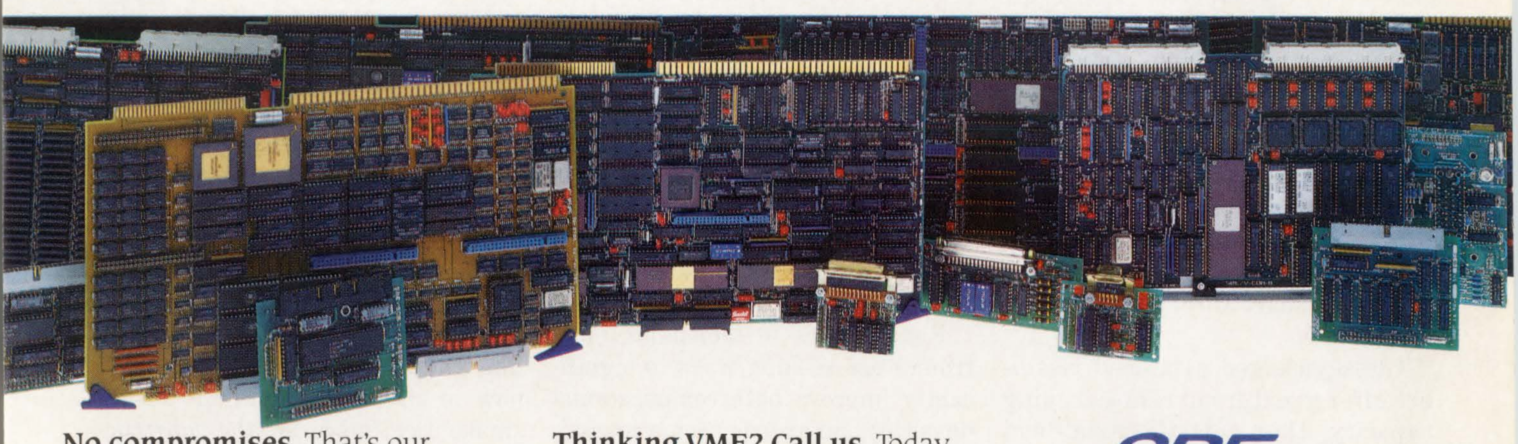

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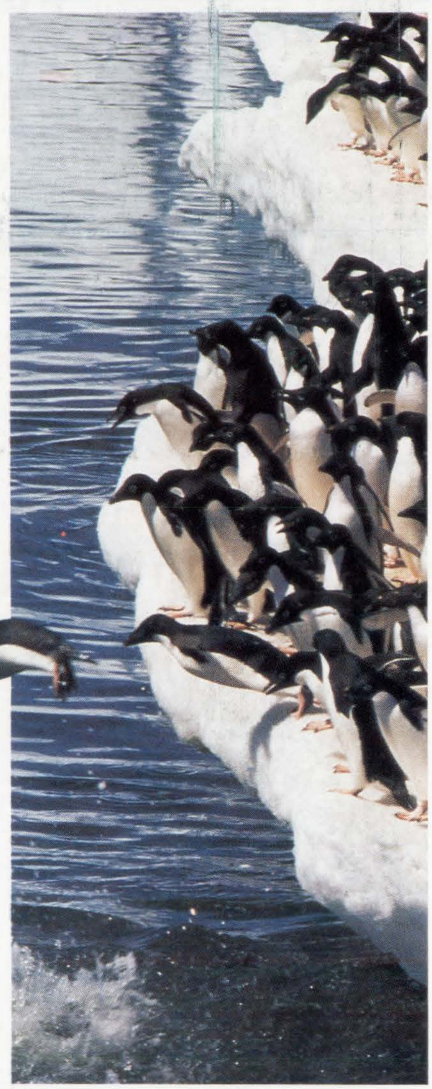

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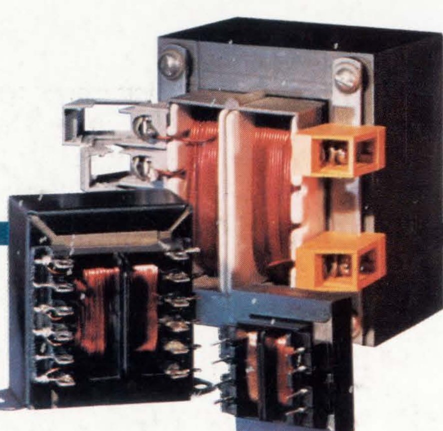

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