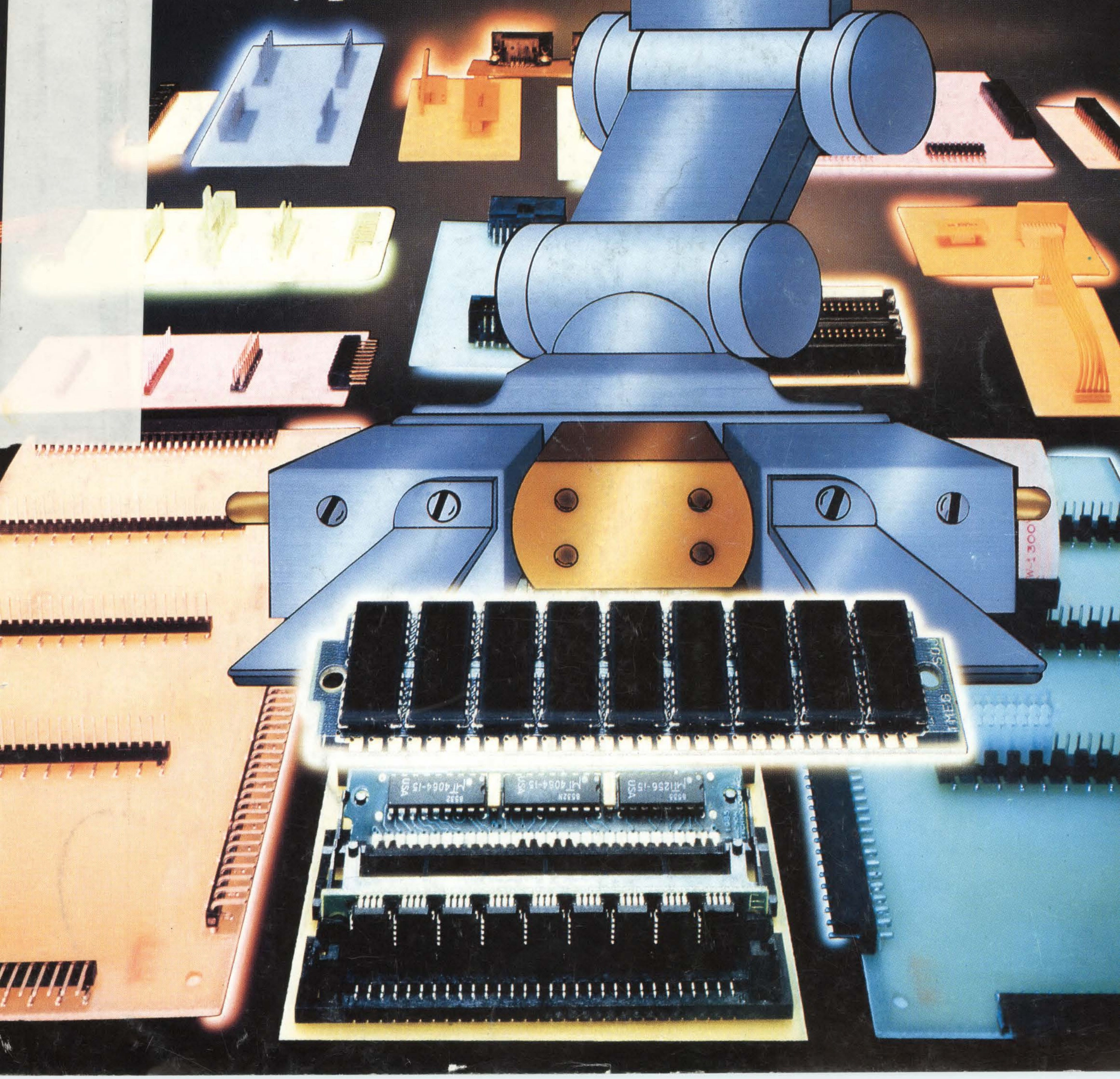
A CAHNERS PUBLICATION
FEBRUARY 18, 1988

EDN®

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Innovations in hardware ease assembly process



PUNCH UP YOUR FLASH A/D PERFORMANCE.

FREEZE VIDEO SIGNALS WITH A SAMPLE & HOLD AMP LIKE THIS.

Introducing the VA730 High-Speed Sample & Hold Amplifier . . . the only monolithic IC of its kind that operates in the 50MHz range.

The only one that's available in surface-mount packaging, and in both commercial and military grades.

And the only one that's designed specifically to operate with 8-bit flash converters.

Best of all, not only is it less costly than expensive hybrids, it's priced well below competing Japanese monolithics.

The VA730 has an A/D converter reference power supply, a sample & hold function, and an ECL clock output section operating to a frequency of 50MHz.

It's available in a 14-pin cerdip package, in a 20-pin ceramic leadless chip carrier (LCC), and in die form.

The VA730 Sample & Hold Amp is just part of VTC's broad line of Linear Signal Processing (LSP) ICs, which includes *Op Amps* to 500MHz gain bandwidth . . . precision, high-speed, and fast settling, plus dual and quad . . . with no sacrifice in performance.

A/D Converters to 12 bits, 1µsec conversion.

Flash Converters to 8 bits, 250MHz.

DACs to 12 bits, 100nsec settling time.

A family of ECL and TTL *High-Speed Comparators* to 1.5GHz.

Video Amps and *Unity Gain Amps* to 2000V/µsec, 300MHz.

And *Operational Transconductance Amplifiers* to 50V/µsec, 75MHz.

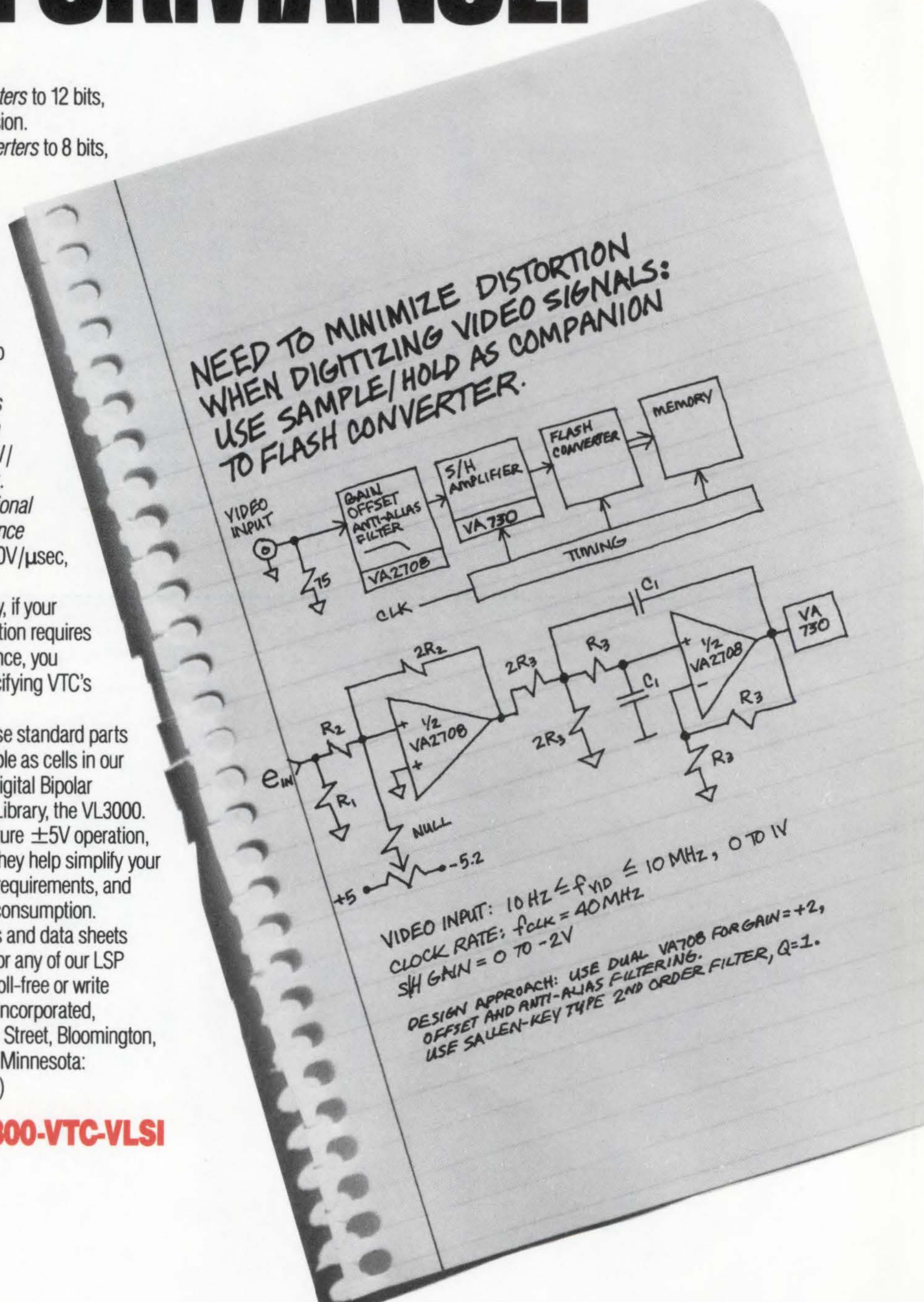
Quite simply, if your analog application requires high performance, you should be specifying VTC's LSP ICs!

Most of these standard parts are also available as cells in our 6GHz Linear/Digital Bipolar Standard Cell Library, the VL3000.

They all feature ±5V operation, which means they help simplify your system power requirements, and reduce power consumption.

For samples and data sheets on the VA730, or any of our LSP products, call toll-free or write us today: VTC Incorporated, 2401 East 86th Street, Bloomington, MN 55420. (In Minnesota: 612/851-5200.)

CALL 1-800-VTC-VLSI



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Performance, Pure & Simple.™

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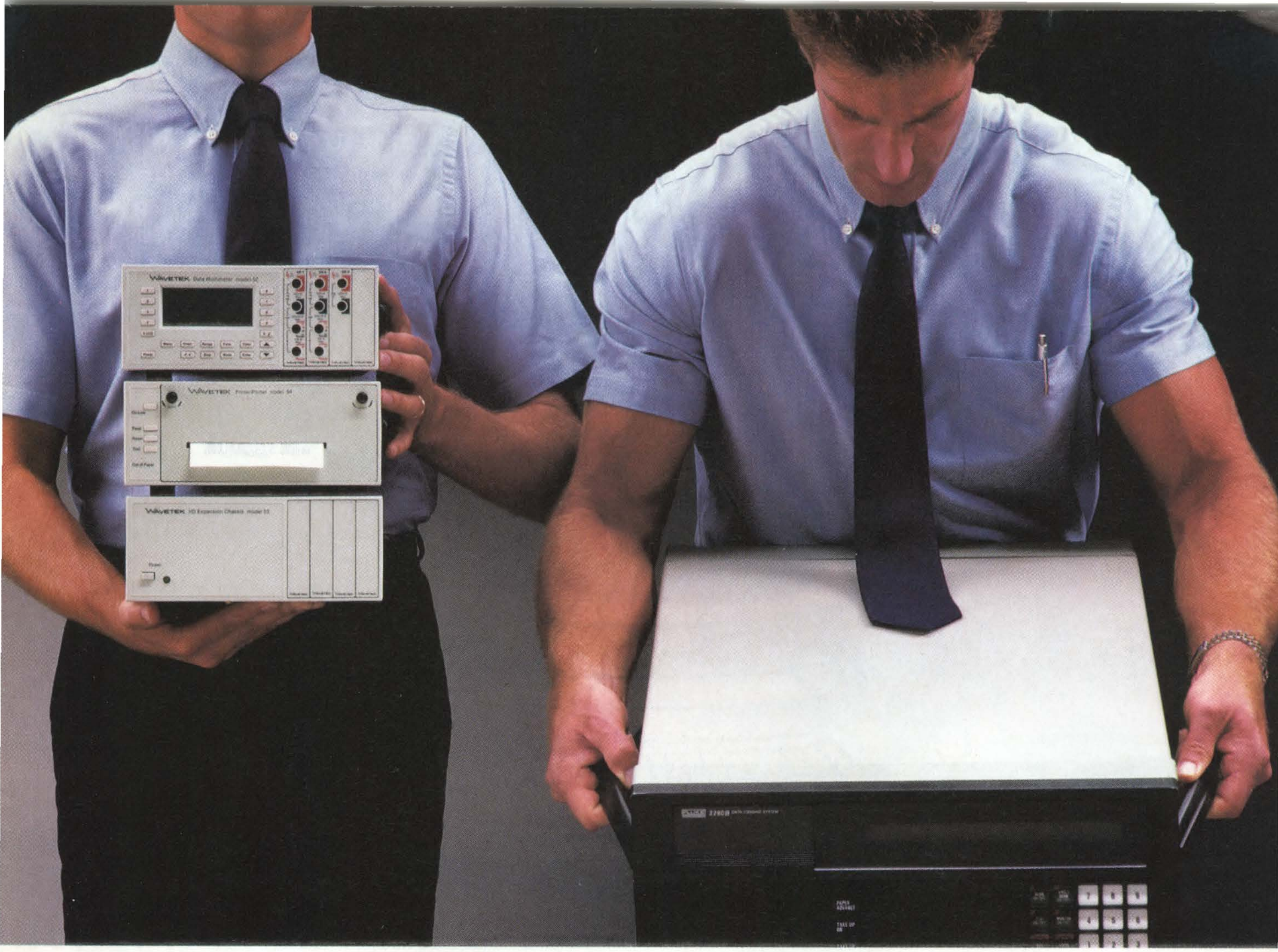


Side by side comparison of our data logger and theirs.

Wavetek has brought an exciting new dimension to data logging—small. Our Series 50 Data Logger is a fraction the size and considerably less expensive than the one on the right. And our data logger is light enough to be easily carried by mere mortals. When you compare the rest of the features, the competition drops right out of sight.

For instance, the Series 50 Data Logger scans 260 channels, provides digital and stripchart printouts and can operate on its internal battery for days, storing up to 100,000 readings in non-volatile memory.

Even more amazing is what the Series 50 measures, including:

- **DC Volts and true RMS AC Volts**
- **Temperatures, 6 Thermocouple Types, °C, °F, °K**
- **AC/DC Current**
- **DC Watts, AC Volt-Amperes**
- **dBw, dBm**
- **Frequency and Period**
- **Pulse Width, Time Interval**
- **Events (Counter)**
- **Resistance and Continuity**
- **Diode Junction Voltage**

All are STANDARD FEATURES, not options! In addition, there are four independent A/D converters, so you can make four different types of measurements simultaneously.

We could go on for pages, but rather than weigh you down with specifications, we'd rather show you how Series 50 will make your job easier. Please call, or write for our brochure. Wavetek San Diego, Inc., P.O. Box 85265, San Diego, CA 92138. Tel. (619) 279-2200; TWX 910-335-2007.

Circle 3 for literature

Circle 42 for demonstration

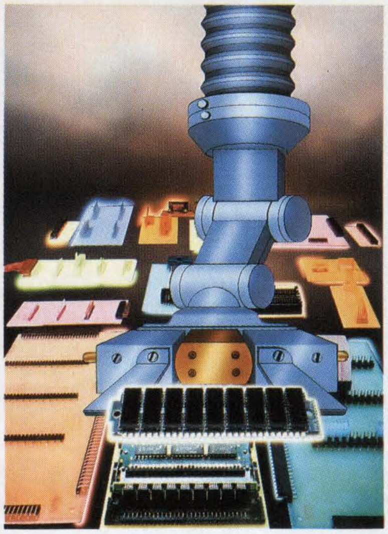
WAVETEK

Volume 33, Number 4

EDN

February 18, 1988

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *Advances in materials and hardware can ease your design through the production phase of the product-development cycle. See pg 148. (Photo courtesy Molex Inc)*

DESIGN FEATURES

Continued on page 7

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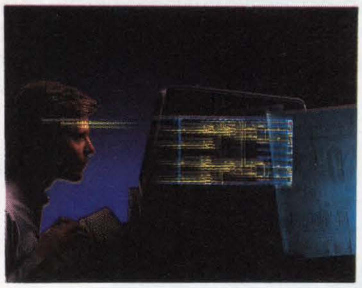
Continued from page 5



For help in designing with multiple PLDs, you can turn to a variety of recent software packages, which range from the simple to the very powerful (pg 61).

TECHNOLOGY UPDATE

PRODUCT UPDATE

DESIGN IDEAS

Continued on page 9

EDN magazine now offers Express Request, a convenient way to retrieve product information by phone. See the Reader Service Card in the front for details on how to use this free service.

Express Request

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4 The Gate Array WorkSystem™ Makes Layout As Easy As Pushing A Button.

IN A SERIES

Tektronix Aided Engineering

Now logic designers can control the entire physical layout of gate array designs. From a single schematic entry environment. Just by pushing a button.

Developed by Tektronix as part of Tektronix Aided Engineering, the Gate Array WorkSystem eliminates the need for IC layout expertise. Because it gives you everything you need to quickly develop ASIC vendor-certified layouts.

And since you're controlling the layout from the schematic, you can tune your design using iterations of simulation and automatic layout to achieve your performance requirements.

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Tektronix®
COMMITTED TO EXCELLENCE

Continued from page 7

EDN

February 18, 1988

EDITORIAL

Before making assignments, be sure everyone has the proper tools and understanding to complete the jobs. Otherwise the assignments may be worthless.

NEW PRODUCTS

PROFESSIONAL ISSUES

Change is coming for performance reviews, but it's slow and painful.—*Deborah Asbrand, Associate Editor*

LOOKING AHEAD

Parallel processing spurs high-end-computer growth . . . EMI/RFI market to exceed $8 billion by 1993.

DEPARTMENTS

Only Mentor Graphics has brought a billion gates to light.

In just 5 years, over a billion gates have flowed through our IDEA Series™ design automation systems. And that's a very conservative estimate.

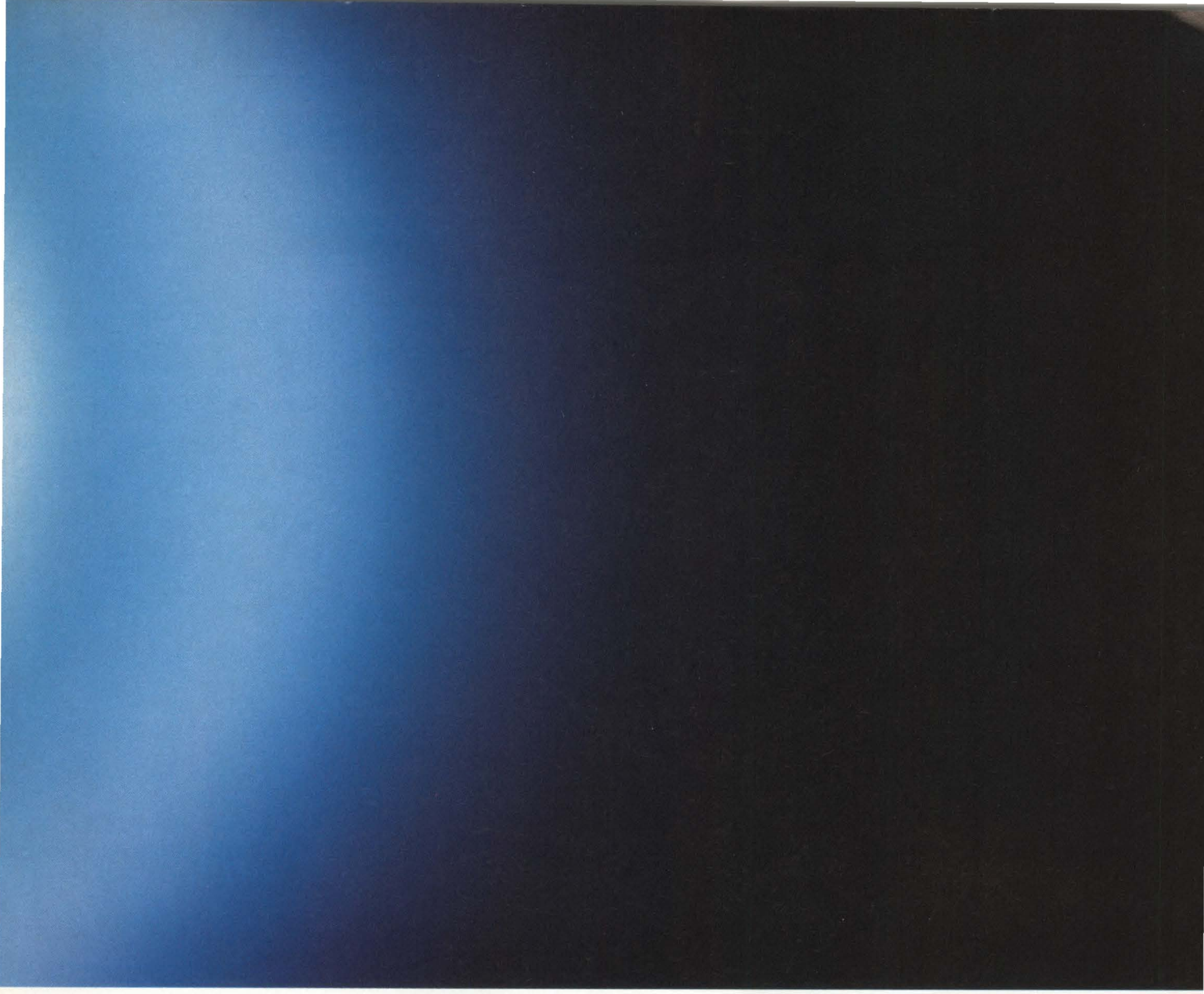
Which makes it seem all the more incredible that, before we came along, almost all electronic circuits were drafted and breadboarded by hand.

Since then, our schematic capture and simulation tools have produced more circuits for more products than any other electronic design automation vendor.

A claim only Mentor Graphics can make.

Along the way, we've pioneered schematic capture and simulation tools that are now industry standard. Like hierarchical design entry, which allows efficient management of even the largest designs. And MSPICE,™ which brings real interactivity and a graphics-oriented interface to analog simulation.

At the same time, we've provided the depth and power required to work with very large designs. A macro language allows you to build a highly customized interface, one suited specifi-



cally to your particular productivity needs. And "case frames" allow very complex circuit patterns to be expressed in just a few keystrokes.

For simulation, our QUICKSIM™ family brings you logic, timing, and fault simulation in a single, integrated package. Plus the ability to use a mixture of modeling techniques, including chip-based modeling with our Hardware Modeling Library.™ And you can call upon our Compute Engine™ general-purpose accelerator to enhance standard workstation performance.

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As we head toward our next billion gates, we'd like to make some of them yours. It's all part of a vision unique to Mentor Graphics, the leader in electronic design automation. Let us show you where this vision can take you.

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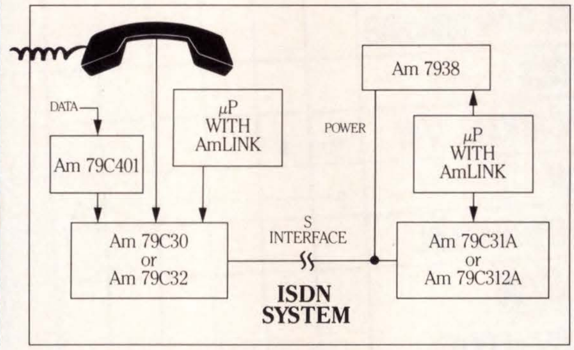
Starting with ISDN is one thing. Finishing is something else.

It's possible to put together your own ISDN chip set. Subscriber controller here, power supply there, line card device from somewhere else.

But why? Advanced Micro Devices can deliver the whole connection.

The ISDN chip set that's made for each other.

With AMD's five chip set, everything is included. All designed to work together. And to conform to the CCITT recommendations.



The set is so highly integrated, you won't need extra chips for things like dialing and ringing.

Each of AMD's chips was designed to take advantage of the most efficient technology for its function, including bipolar and CMOS. The set consists of the Am79C30 Digital Subscriber Controller, the Am79C31A/312A Digital Exchange Controller, the Am79C32 ISDN Data Controller, and the Am7938 Quad Exchange Power Controller which works with the Am79C31A/312A. And it won't be long before we'll have protocol devices like the Am79C401 Integrated Data Protocol Controller.

Software made for our chip set.

Once you've got hardware, you'll probably be needing some software. That's easy. AMD has everything from low level device drivers to AmLINK, our LAPD software.

AmLINK implements software interfaces defined in the CCITT Q.921/931 recommendations. AmLINK is modular and it's independent of the operating system, giving you added flexibility. And, because you need it, source code is available.

We also provide well documented development boards that come complete with demonstration software. Understanding the capabilities, flexibility and functionality of complex ISDN chips has never been easier.

Field trial proven.

There's one more good reason why you should pick AMD. Our ISDN chips are in field trials with Illinois Bell, Mountain Bell, the Deutsche Bundespost and others. The chips were certified in field trial test beds. And they're still in use today.

Get in touch with AMD for more information. Then get your product off to a great start. And finish.

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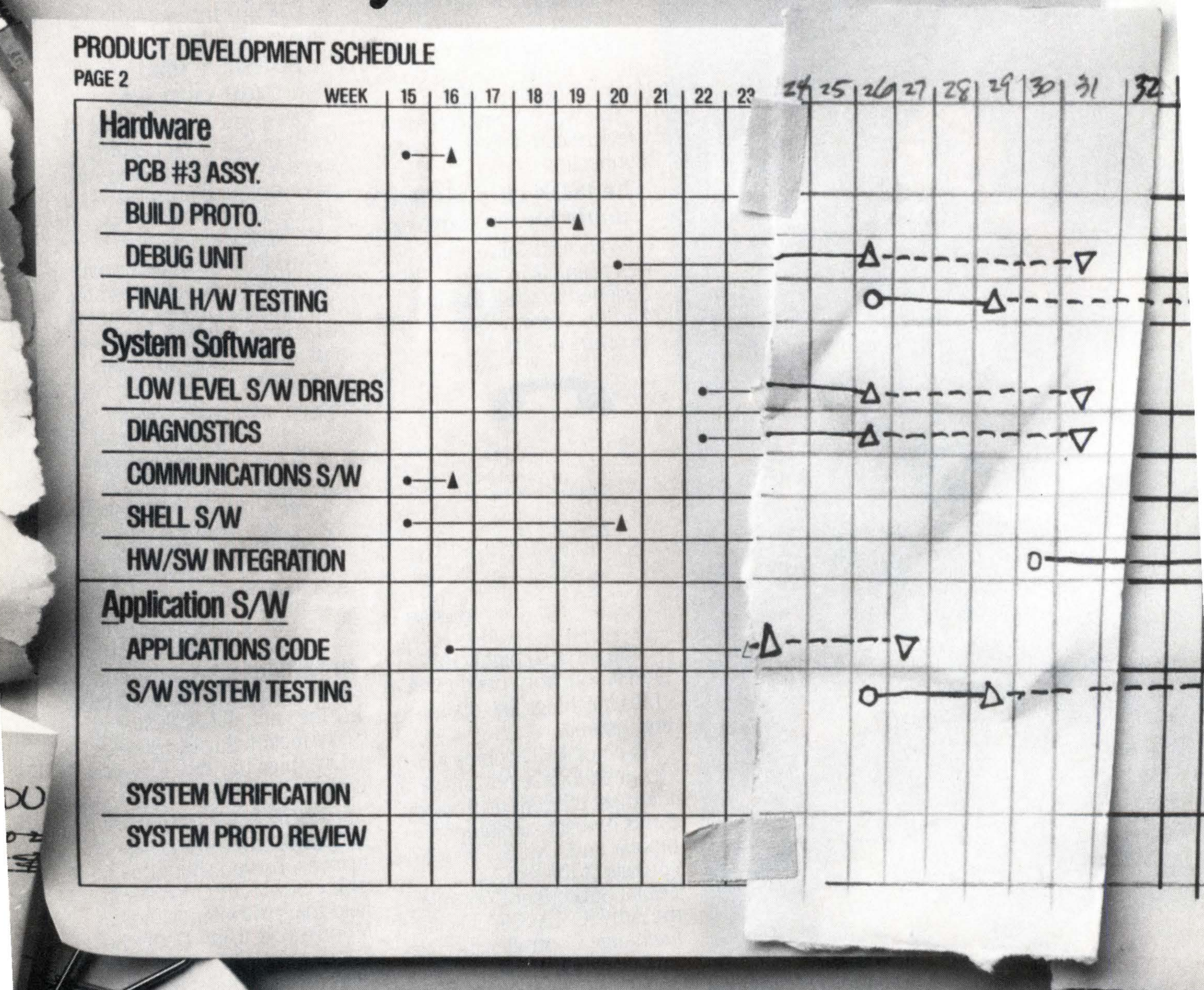

Let's face it. Slipped development schedules and budget overruns can mean lost opportunities. Yet many traps that seriously delay a development schedule are quite complex, especially when they are compounded by problems that arise in cross development work.

Like not knowing whether the errors you are getting from your prototype processor are real. Or losing bugs in the cracks between your development system and the prototype.

Fortunately, the answer to these complex problems is simpler than you might think. Because now Applied Microsystems offers what we call performance packages: complete, fully integrated development solutions, designed to meet your development requirements and to detect even subtle problems quickly.

Performance Packages that Live Up to Their Name.

Each package includes a powerful in-circuit emulator, the only tool that can successfully bridge the gap between host computer and prototype. With features like complex triggering, reliable memory, built-in target diagnostics, I/O simulation, and special interrupt handling.

And to complement the power of our emulators, we provide software tools that work with a variety of platforms and languages.

Whichever package you choose, you're getting the highest performanc

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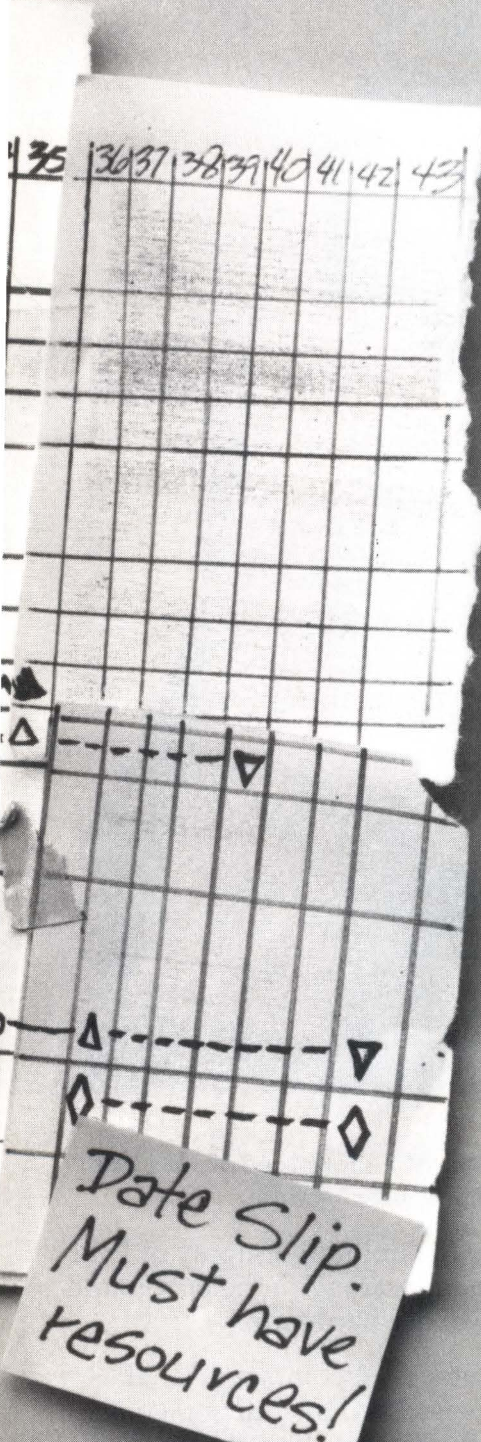
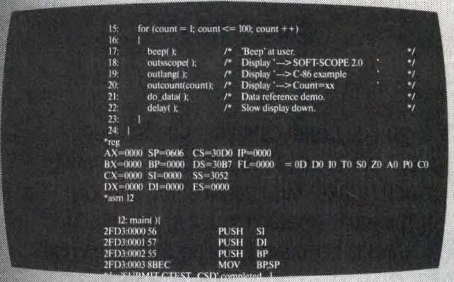


development tools available.

Source Level Debugging for Intel Microprocessors

Our VALIDATE/Soft-Scope and VALIDATE/Soft-Scope 286 packages are designed for any language producing complete Intel OMF information.

A PC-based, in-circuit source level debugger and simulator are closely cou-

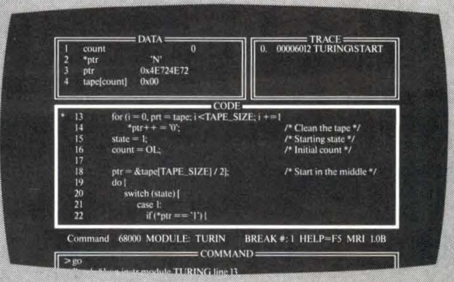


pled with our ES 1800 emulator. You can use commands to examine variables on the fly, check contents of registers, and determine current position in code. And real-time trace is displayed as source level statements, machine instructions or bus cycles.

The packages also include a logic state analyzer probe, and provide up to 2 Megabytes of overlay memory plus full protect mode support for the 80286.

Source Level Debugging for Motorola Microprocessors

The window-oriented VALIDATE/XEL package combines our XEI source-level debugger, a simulator and the MCC68K compiler with our ES 1800

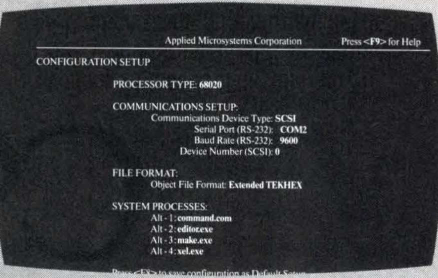


emulator. The package also includes a logic state analyzer probe and our well-known SCSI interface option, that significantly decreases download time.

In addition to up to 2 Megabytes of overlay memory, you get target control from your source code; powerful "C" language macros for code patching, remote control and simulation of I/O; plus user-definable windows for viewing registers, stacks and variables

High-speed Symbolic Debugging for Intel, Motorola and Zilog Microprocessors

Our VALIDATE/ES DRIVER package includes easy-to-use (menu-driven and remote control) software that smoothly links the host functions to the ES 1800 emulator. This allows the upload and download of programs, symbol tables and command files.



Also included are a logic state analyzer probe; the SCSI option for increasing download speeds by up to 30 times; plus up to 2 Megabytes of overlay memory.

To find out more about 8, 16 or 32-bit development solutions that save money in the long run, write Applied Microsystems Corp., P.O. Box 97002, Redmond, WA 98073-9702. Or call 1-800-426-3925 (In Washington, call 206-882-2000).

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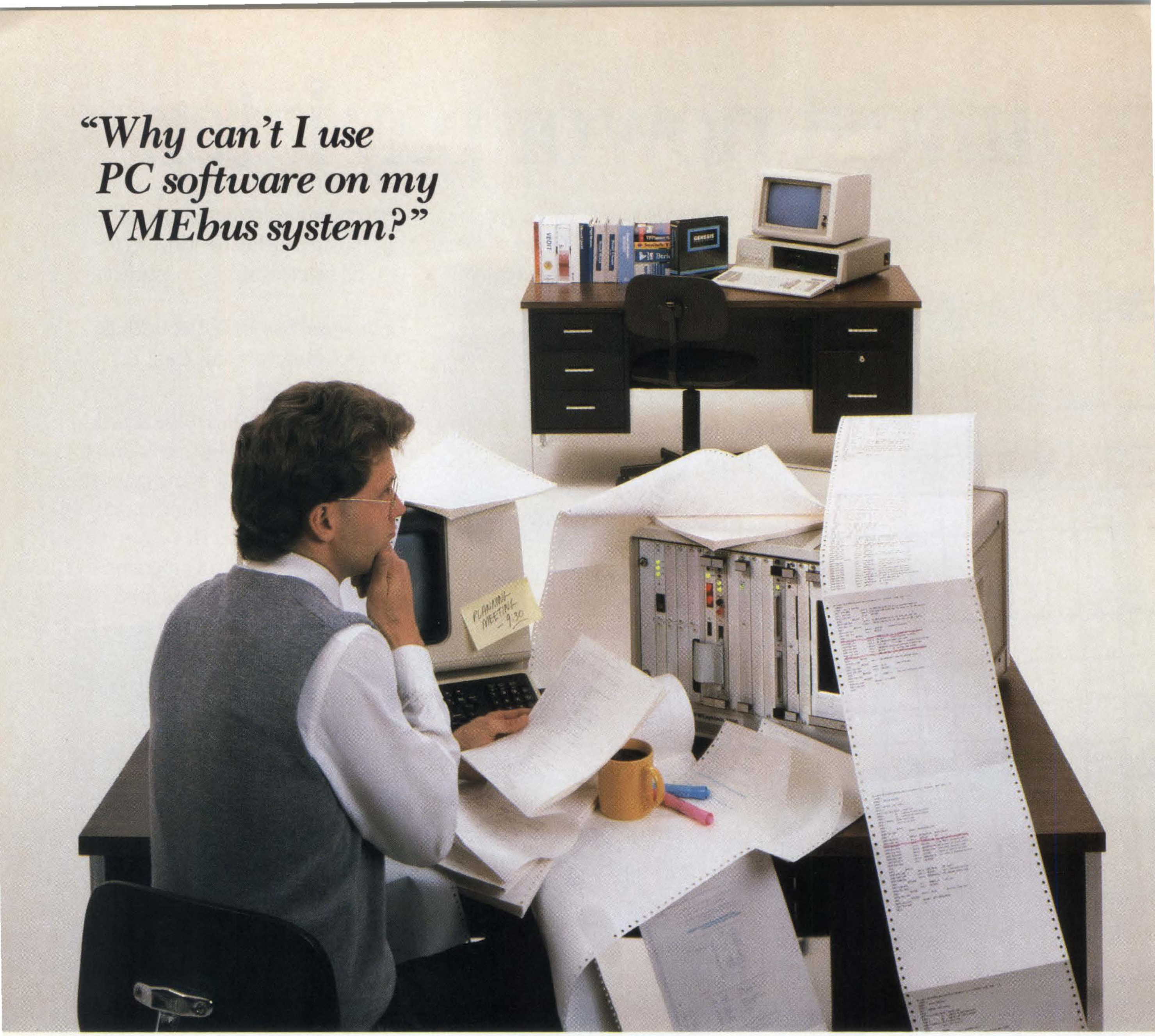
"Why can't I use PC software on my VMEbus system?"



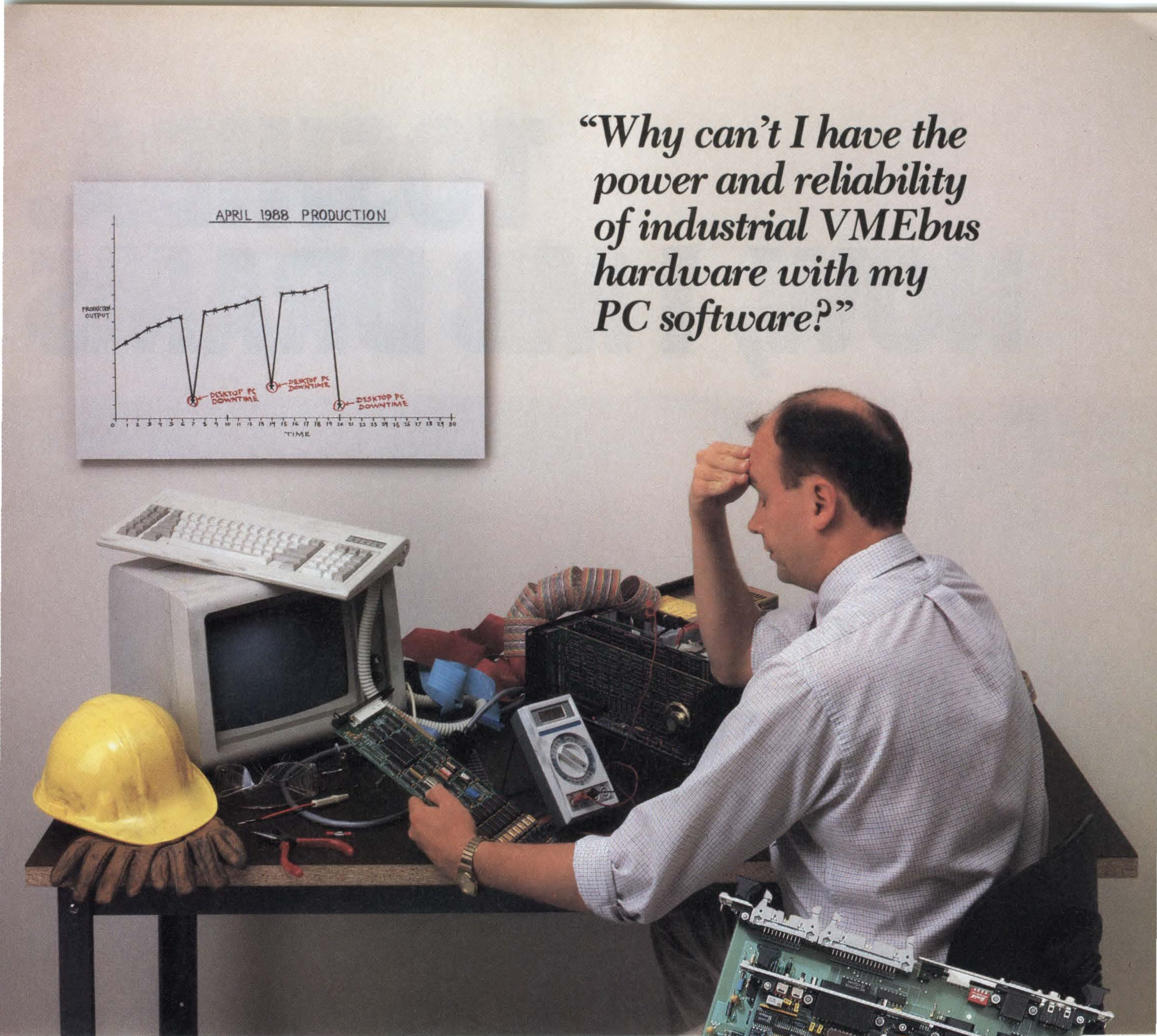
You Can!

Xycom's new processor now marries PC/AT software to VMEbus hardware.

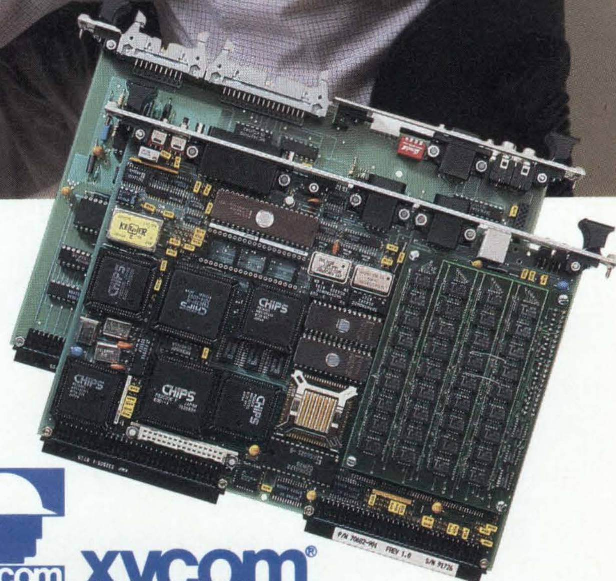
The new XVME-682 PC/AT Processor. It's the perfect industrial computer system.

It lets you combine the unlimited supply of IBM PC/AT-compatible software with the power and performance of VMEbus hardware.

Consider the advantages! A complete PC/AT computer on a two-card set, including memory, disk controller, and color graphics. A standardized operating system with off-the-shelf software



available for: industrial control, spreadsheets, communications, word processing, graphics, and more. Plus the rugged, high performance of VMEbus hardware— with multiprocessing, I/O, and faster throughput capabilities.



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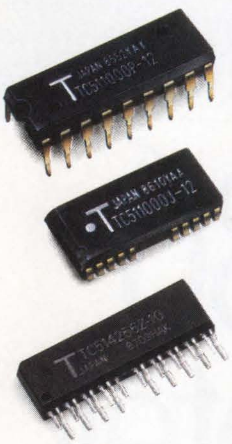

Toshiba, world production leader in CMOS, is delivering 1MB DRAMs. In three different access modes. With speeds of 85, 100 and 120 ns. You have a choice of fast page mode, static column or nibble mode, as well as DIP, SOJ and ZIP packages.

TOSHIBA 1 Mb DRAMs					
Part Number	Organization	Process	Speed	Mode	Package
TC511000 - 85	1 Mb x 1	CMOS	85 ns	Fast Page	18 pin
TC511000 - 10	1 Mb x 1	CMOS	100 ns	Fast Page	18 pin
TC511000 - 12	1 Mb x 1	CMOS	120 ns	Fast Page	18 pin
TC511001 - 85	1 Mb x 1	CMOS	85 ns	Nibble	18 pin
TC511001 - 10	1 Mb x 1	CMOS	100 ns	Nibble	18 pin
TC511001 - 12	1 Mb x 1	CMOS	120 ns	Nibble	18 pin
TC511002 - 85	1 Mb x 1	CMOS	85 ns	Static Column	18 pin
TC511002 - 10	1 Mb x 1	CMOS	100 ns	Static Column	18 pin
TC511002 - 12	1 Mb x 1	CMOS	120 ns	Static Column	18 pin
TC514256 - 85	256K x 4	CMOS	85 ns	Fast Page	20 pin
TC514256 - 10	256K x 4	CMOS	100 ns	Fast Page	20 pin
TC514256 - 12	256K x 4	CMOS	120 ns	Fast Page	20 pin
TC514258 - 85	256K x 4	CMOS	85 ns	Static Column	20 pin
TC514258 - 10	256K x 4	CMOS	100 ns	Static Column	20 pin
TC514258 - 12	256K x 4	CMOS	120 ns	Static Column	20 pin

256K CMOS STATIC RAM

Toshiba's product development leadership continues. We were first with 16K CMOS RAMs. First with 64K CMOS RAMs. And now first again—with 256K CMOS static RAMs. This 32K x 8 device features the lowest power consumption available today—only 5mA/MHz. Lower than any competitive product. And we offer speeds to 85 ns.

TOSHIBA 256K CRAMs					
Part Number	Organization	Process	Speed	Standby Power	Package
TC55257AF-85	32K x 8	CMOS	85 ns	100μA MAX	28 pin
TC55257L-10	32K x 8	CMOS	100 ns	100μA MAX	28 pin
TC55257AL-12	32K x 8	CMOS	120 ns	100μA MAX	28 pin
TC55257AL-85L	32K x 8	CMOS	85 ns	30μA MAX	28 pin
TC55257AL-10L	32K x 8	CMOS	100 ns	30μA MAX	28 pin
TC55257AL-12L	32K x 8	CMOS	120 ns	30μA MAX	28 pin

(Now available in Plastic Flat Pack.)

ULTRA LEADERSHIP

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NEWS BREAKS

EDITED BY JOANNE CLAY

SOFTWARE TOOL SIMPLIFIES SILICON-COMPILER-BASED DESIGNS

The ChipCrafter design software from Seattle Silicon (Bellevue, WA, (206) 828-4422) provides mainstream ASIC designers with the advantages of process-independent silicon compilers. Designing for silicon compilers usually requires a custom-IC-design background that most electronics engineers and electronics companies don't have. According to the vendor, the ChipCrafter tools allow any engineer who can design a standard-cell ASIC to design a compiler-based ASIC. Compiler-based designs let you select from a variety of foundries and processes in order to optimize speed, power, and cost considerations. The software package allows you to design at the standard-cell level or lower. It also lets you create state machines and complex control circuitry from behavioral inputs. The software provides automatic placement and routing of all elements, dividing standard cells where necessary for efficient design. Because all the design elements—including the standard cells—are compiler based, you can optimize the elements on an individual basis. For example, you can adjust the size of output transistors to meet drive requirements. The package supports scan-path testing; it automatically connects all flip-flops, registers, and counters. ChipCrafter is currently in Beta-site testing; delivery of production quantities will begin in May. The package costs $59,000.—Doug Conner

PARALLEL-PROCESSING COMPUTER FEATURES OPEN ARCHITECTURE

Based on a distributed-memory, message-passing communications network, the Series 2010 parallel-processing computer from Ametek (Monrovia, CA, (818) 359-2835) lets you interface any processing node to standard VME Bus-compatible devices and local disk drives. Each node contains a 25-MHz 68020 μP, a 68881 floating-point unit, 1M byte of local memory that's expandable to 8M bytes, and a VME Bus interface. Message passing is controlled among the nodes by automatic-message-routing devices (AMRDs) that contain five parallel channels and transfer data at speeds exceeding 20M bytes/sec. The languages available for the Series 2010 include C, Fortran 77, Unix, and Concurrent Lisp. The system uses a Sun-3 workstation as the front-end host. Pricing for the Series 2010 starts at $45,000 for a 4-node system. Each additional node you add to the system raises the performance spec by 4 MIPS.—J D Mosley

DMM IC OFFERS IMPROVED CURRENT RESOLUTION

Besides using the TSC816 digital-multimeter IC in handheld multimeters, you can use it for dedicated conversion and display of voltage, current, and resistance outputs from sensors and transducers. The DMM IC, from Teledyne Semiconductor (Mountain View, CA, (415) 968-9241), is an improvement over the earlier TSC815; it provides a 2-mA current range with 1-μA resolution. The device has 24 operating ranges covering voltage, current, and resistance measurements. Autoranging is provided for voltage and resistance measurements. The IC has on-chip liquid-crystal-display drivers and is available in a 68-pin plastic leaded chip carrier (PLCC) for $13.20 (100).—Doug Conner

LOW-COST ERASABLE-LOGIC DEVELOPMENT TOOL IS PC BASED

The $795 PET100 erasable-logic development system from Pistohl Electronic Tool Co (Cupertino, CA, (408) 255-2422) combines the company's $295 erasable-logic assembler and $495 erasable-logic programmer with a test-vector-generation language and an EPROM programmer. The assembler generates JEDEC fuse maps from your Boolean equations; a 50-rule expert system finds logic errors, suggests corrections, and pops up a WordStar-compatible editor with the cursor positioned at the error. The erasable-logic programmer comprises programming hardware and the company's high-level test language, WIOS. The system supports EEPLDs from Altera, Atmel, Cypress, AMI/Gould, ICT, and Monolithic Memories.—Margery S Conner

SIGNAL PROCESSOR COMES IN 10- AND 12.5-MHz VERSIONS

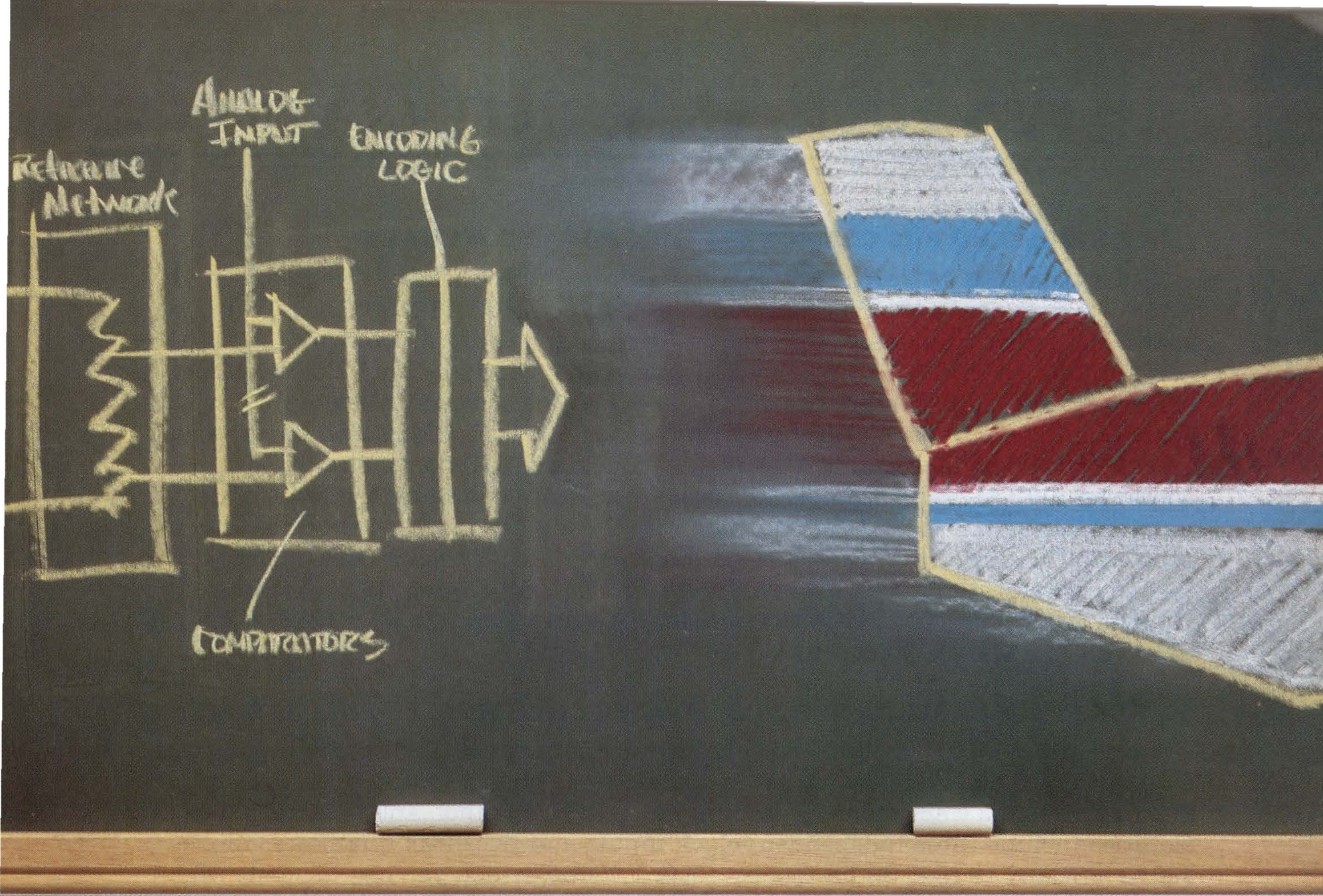
The ADSP-2100 digital-signal processor from Analog Devices (Norwood, MA, (617) 461-3881) is now available in 10- and 12.5-MHz versions (the ADSP-2100AJ and -2100AK, respectively). The vendor claims the product's speed and architectural efficiency make it the industry's fastest general-purpose DSP chip. According to the company, the ADSP-2100A can compute an in-place, complex 1024-point FFT in 3.0 msec, a speed comparable to that of dedicated FFT chips. The -2100AJ and -2100AK are code and pin compatible with the company's earlier 6- and 8-MHz (-2100J and -2100K) versions of the chip, and are available in 100-lead pin-grid arrays and 100-lead PLCCs. The 10- and 12-MHz chips, in PLCCs, cost $103 and $133 (1000), respectively; samples are available from stock. The vendor plans to introduce a military-temperature version of the 10-MHz chip in the fourth quarter of 1988. The company also offers a C compiler that generates source assembly code for the 2100 and 2100A chips. The compiler conforms to the ANSI X3J11 draft, and it comes in MS-DOS, VAX/VMS, and Unix BSD 4.2 versions. Emulators and evaluation boards for the -2100A chips will be available in the second quarter of 1988.—Joanne Clay

INEXPENSIVE DIGITAL-FILTERING SOFTWARE RUNS ON YOUR PC

You can now purchase an integrated data-acquisition, -storage, and -analysis software package that also provides four types of digital filters: lowpass, highpass, bandpass, and band reject. The $1185 package includes a data-acquisition program called Snapshot Storage Scope, the Snap-Calc analysis and monitoring program, and the new Snap-Filter program. The software was developed by HEM Data Corp (Southfield, MI, (313) 559-5607). If you already have the Snap-Calc and Snapshot Storage Scope programs, you can buy Snap-Filter for $395. Snap-Filter lets you specify any filter as a finite-impulse-response or infinite-impulse-response filter. To order a demonstration disk, contact Andrea Tomaszewski at the above number.—J D Mosley

OPTION BOOSTS LASER-PROCESSING SYSTEM'S THROUGHPUT BY 15%

By adding the H844 vision-processing option to the M218 Laser Processing System from Teradyne's Industrial Consumer Div (Boston, MA, (617) 482-2700, TWX 710-321-1055), you can boost the system's throughput by 15% and improve its wafer-alignment success rate to better than 99.99%, the vendor claims. With the H844 option, the M218 system performs high-speed wafer alignment by using proprietary vision algorithms. The H844's user interface includes software windows, a mouse, pull-down menus, and graphics tools. The H844 is also available with an optical-character-recognition feature, which reads alphanumeric characters printed on the wafer in standard fonts. The M218 system incorporates a Unix-based Sun workstation, a digital-signal processor, an automatic-calibration facility, and an Ethernet interface. It performs precise link-cutting operations on a variety of silicon devices, including dynamic and static RAMs and gallium arsenide ICs. The H844 vision-processing option costs $40,000; the optional optical-character-recognition feature is $20,000. Delivery is 16 weeks ARO.—Joanne Clay



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NEWS BREAKS: INTERNATIONAL

SINGLE-BOARD Q BUS COMPUTERS RUN PDP-11 SOFTWARE

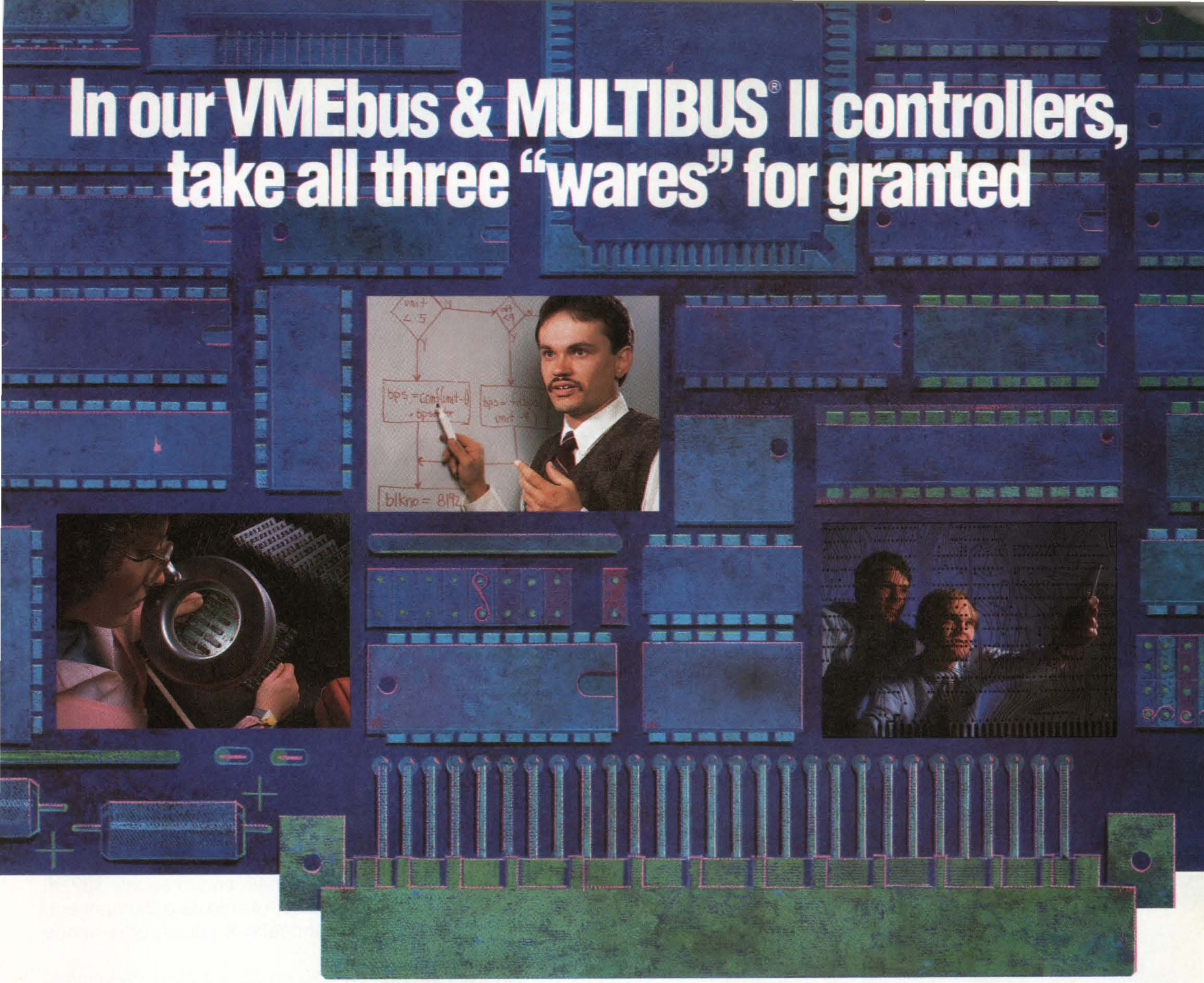
Featuring a DEC J-11 processor that has zero-wait-state access to as much as 4M bytes of parity-checked onboard dynamic RAM, the M80 and M90 quad Q Bus single-board computers from Mentec Computer Systems Ltd (Dublin, Ireland, TLX 93309) can run unmodified DEC PDP-11 operating systems and software. The M80's 15-MHz processor provides a 30% improvement in speed over the company's earlier M70 single-board computer; the M90's 18.5-MHz processor provides a 60% speed improvement over the M70. The M80 and M90 each offer four serial-I/O ports, 32k bytes of bootstrap EPROM, and an EEPROM that allows you to configure the board. The software-configurable boot program can step through as many as six different bootstrap calls, allowing you to use the board as a host processor in a variety of system configurations. The M80 will be available in OEM quantities by March 1988; a 1M-byte version costs £2500 (50). The M90 will be available by May 1988. A 4M-byte version of the M90 sells for £5150 (50).—Peter Harold

LOW-COST LOGIC ANALYZER PROVIDES 32-CHANNEL, 25-MHz OPERATION

Priced at £1790, the TA1000 logic analyzer from Thandar Electronics Ltd (St Ives, UK, TLX 32250) provides you with 32 state/timing channels that operate at 25 MHz. The instrument's trace memory amounts to 1k bits/channel, and its external clock facilities include three independent clock inputs and five clock qualifiers. You can define as many as four 32-bit trigger/restart words, which you can logically OR together in each step of a 4-step trigger sequencer. Each step of the trigger sequencer also includes a 1- to 256-event counter. You can display timing or variable-format state information on the analyzer's 7-in. CRT, and you can analyze the information by using the instrument's trace-expansion facilities, its two screen cursors, and its reference memory. You can also perform automatic trace/reference-memory comparisons on any portion of the traced data. An optional feature lets you stop trace acquisition on trace/reference equality or inequality, or count the occurrences of these conditions. The instrument's price includes IEEE-488 and RS-232C control interfaces. Variable-threshold input pods and disassemblers for 8- and 16-bit μPs are available as options.—Peter Harold

FIRMS PRODUCE FIRST TRON-BASED 32-BIT μP AND PERIPHERALS

Hitachi, Fujitsu, and Mitsubishi have developed the first 32-bit microprocessor and peripheral chips based on the Tron architecture proposed by professor Ken Sakamura of Tokyo University. The chips are the result of the three firms' agreement to develop Tron μPs and peripheral circuits in three stages. Hitachi's development is the GMicro/200 32-bit μP, which runs at 20 MHz and can perform 6 MIPS. The chip has sixteen 32-bit registers and can manage as much as 4G bytes of data. Hitachi manufactures the chip with a 1-μm CMOS double-layer-aluminum process. The device measures 14×14 mm and incorporates approximately 730,000 transistors. Samples of the chip will be available this spring; Hitachi will begin mass production of the device in the fall of 1988. Fujitsu plans to develop a 12- to 20-MIPS version of the GMicro/200 by the end of 1988, and Mitsubishi is scheduled to develop a 4.5- to 10-MIPS version by the first half of 1989. Fujitsu has also developed three peripheral ICs for the 32-bit μP: They include a DMA controller that can receive and send data at 27M bytes/sec without using the μP, a tag memory with a 27-nsec readout speed, and an interrupt controller.—Joanne Clay



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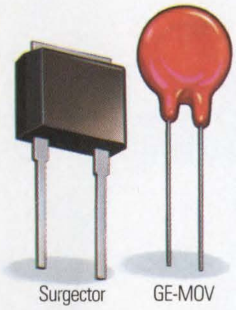

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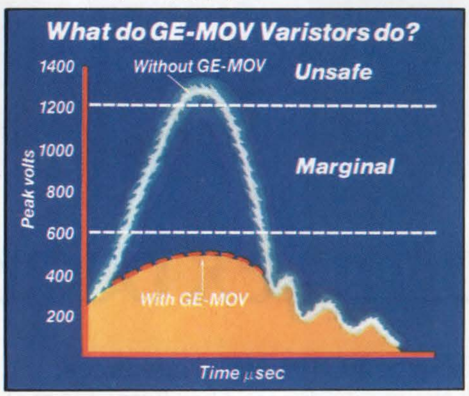

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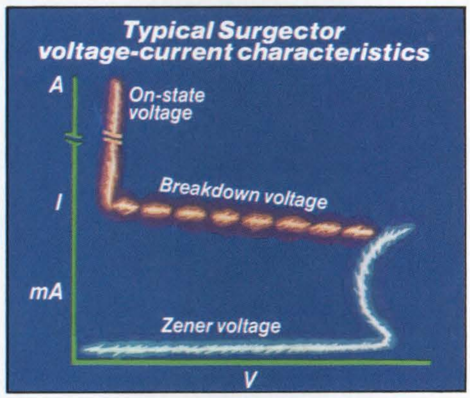

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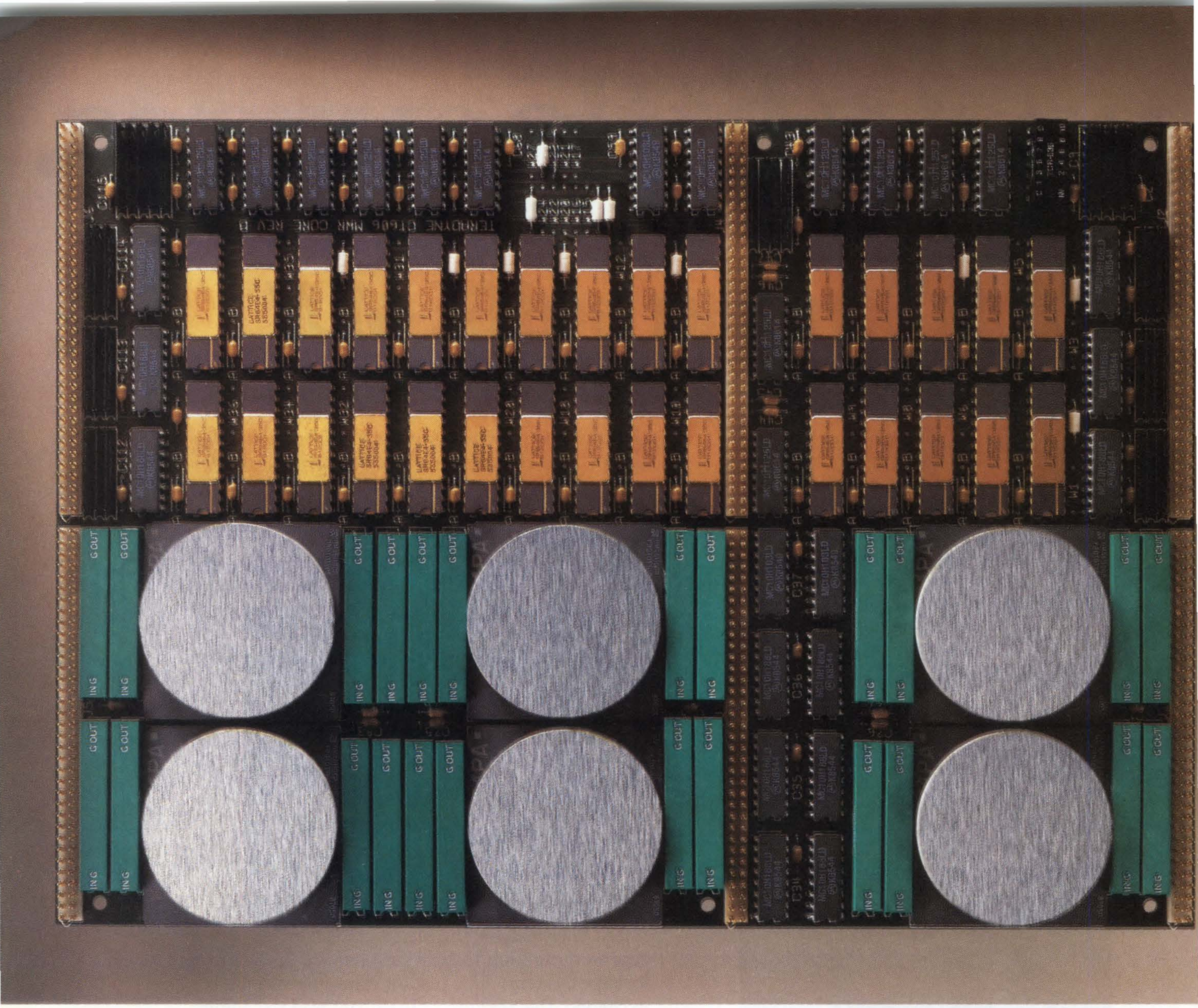

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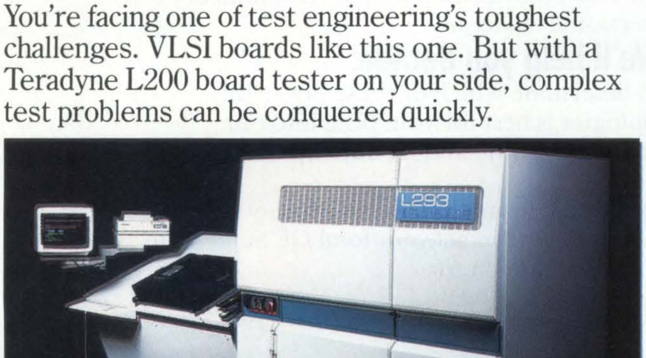

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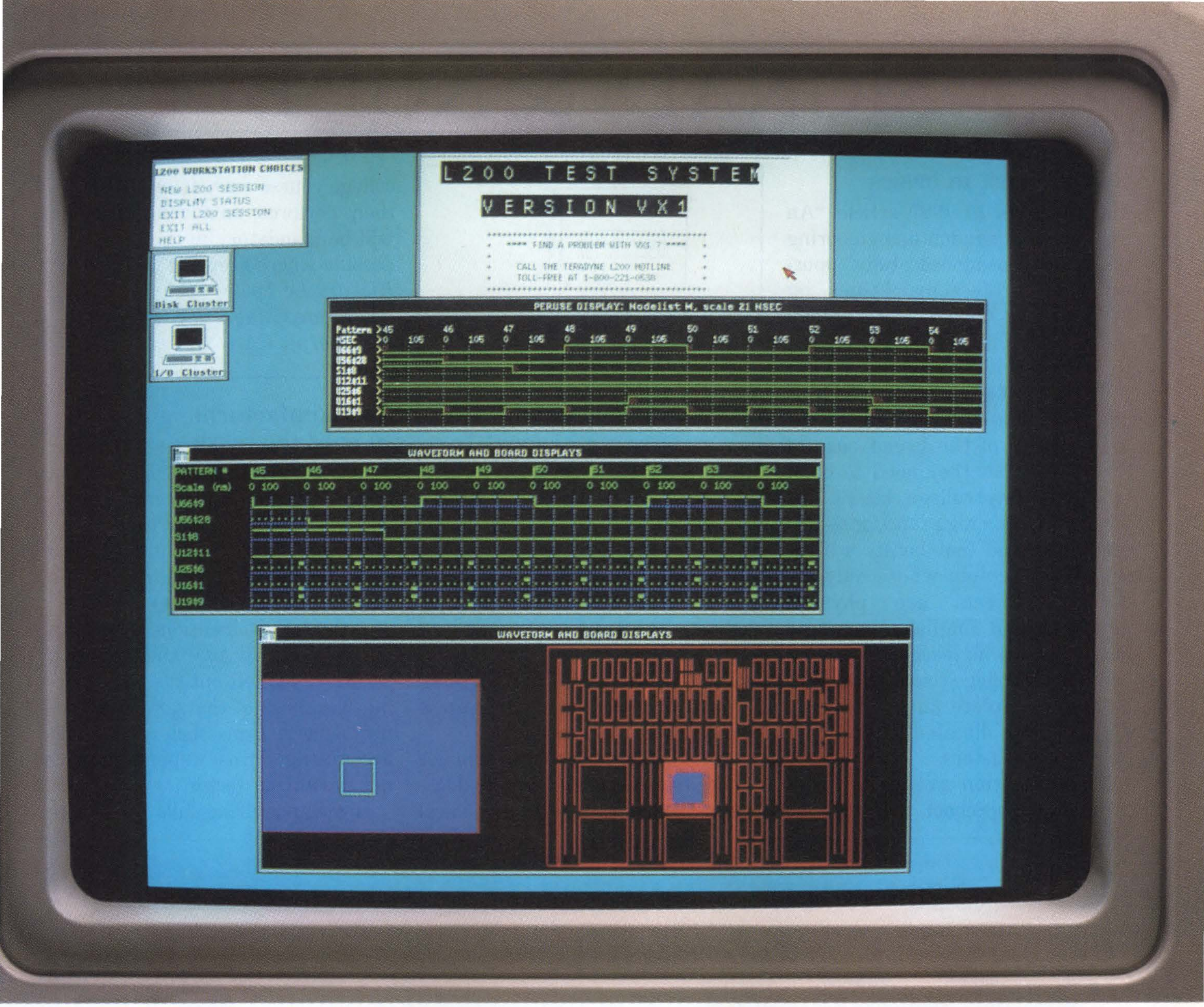

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Programmers will appreciate clustered VAX workstations. Graphics, like waveforms and shmoo plots, make heavy debug and analysis light work.

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L293	576	80 MHz	±1.5 ns
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SIGNALS & NOISE

Getting back to basics

The December 10, 1987, article, "An experimental graduate-engineering program opens up new study opportunities" (Professional Issues, pg 363), brings up another problem that is contributory to the one that concerns Daniel Sternlicht.

The level of education available to average high-school students deprives them of the broad base of knowledge that they need to build on in lower-level college classes. In a state that has a high functional-illiteracy rate and that boasts a high-school curriculum whose only required subjects are physical education and English, there's no chance that a high-school graduate can carry a college course load sufficient to complete an engineering degree in the allocated four years of 16-credit semesters.

The education available to me (Central High School, Philadelphia, PA, class of 1941) can't be duplicated now in any public school system dedicated to passing substandard students through a watered-down system where baseball is more important than biology, and Latin is passed over for linebackers.

If it takes two years in a junior college to achieve the level of education sufficient to tackle a technical college course such as engineering, then, perforce, an advanced degree will be mandatory in that area, especially where licensing is required.

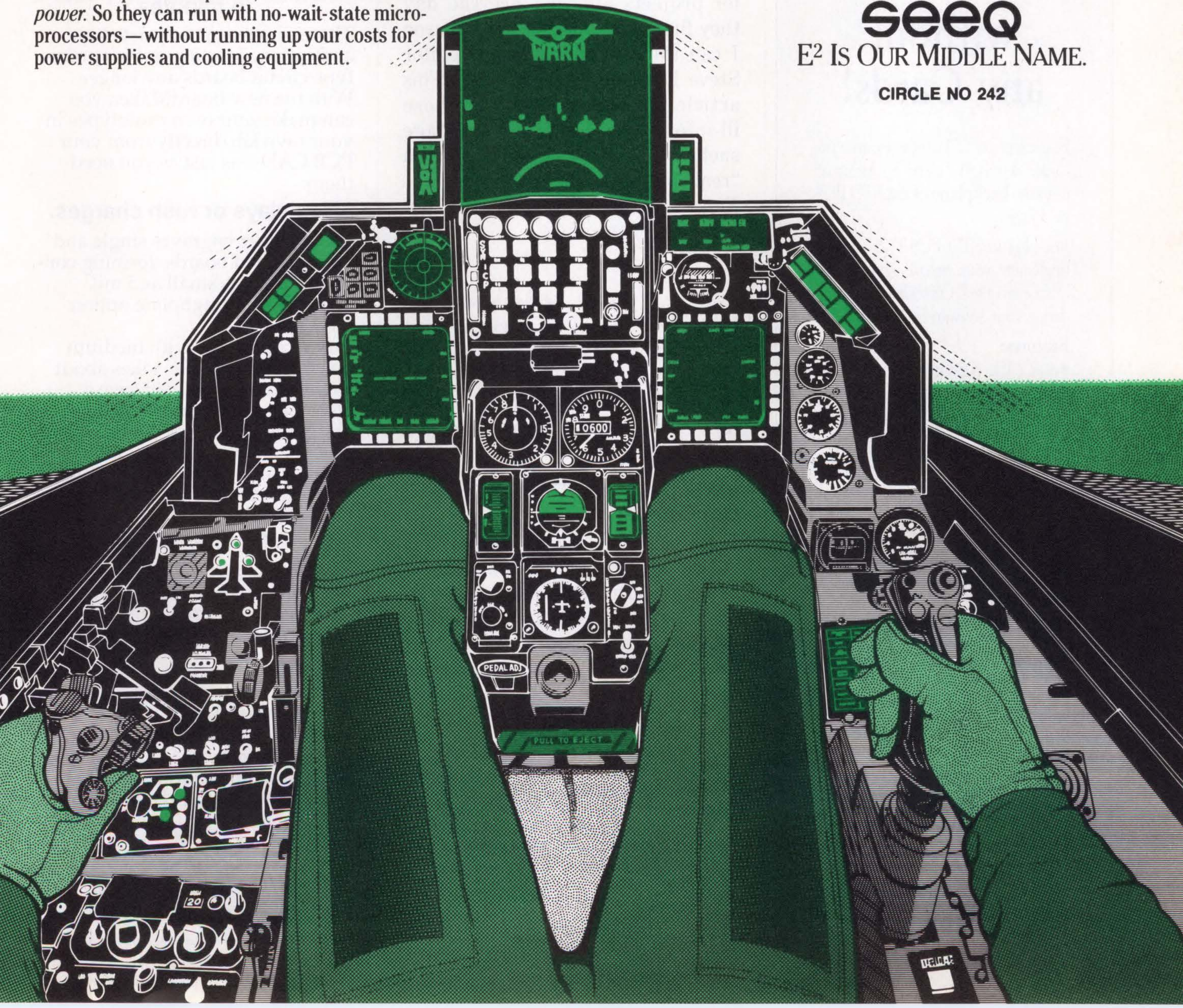
Richard La Porte
Engineered Magnetics Inc
Hawthorne, CA

As manufacturing goes, so goes the service sector?

Your December 10, 1987, editorial (pg 53) on the service-economy myth was excellent. Other articles show economists are now beginning to realize that service firms are not the salvation for this country.

Although you mentioned the service sector's low pay and poor job security, you left out the most glaring weakness of the service economy: Service firms such as law and accounting firms depend on the manufacturing sector.

If manufacturing falls flat on its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face, service firms will come tumbling down. When service firms automate with computers to the extent that manufacturers already have, the layoffs that manufacturers are famous for will be nothing compared to the bloodbath we can expect in the service sector.
Glen Spielbauer,
Dallas, TX

MLL: Medium-level language

The article entitled "HLL cross compilers speed 1-chip-μC software development" (EDN, December 24, 1987, pg 126) omitted all mention of Forth. Forth has been the high-level language of choice for microcontroller projects almost since the day they first came out. The only reason I can think of that regional editor Steve Leibson left Forth out of his article is that he is one of those ill-informed computer-language snobs who doesn't consider Forth a "real" high-level language.
Robert Johnson
Friedhoff Control Co
Duluth, MN

(Ed Note: Steve Leibson says he isn't an ill-informed computer-language snob. His research for the article uncovered no Forth languages for a single-chip computer. He'd like to hear from readers who know of any.)

Correction

In the schematic for the Design Idea "Circuit protects solenoids in dot printer" (EDN, December 10, 1987, pg 325), IC_{6A} pins 1 and 2 should be connected to ground.

WRITE IN

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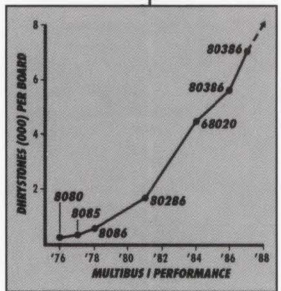

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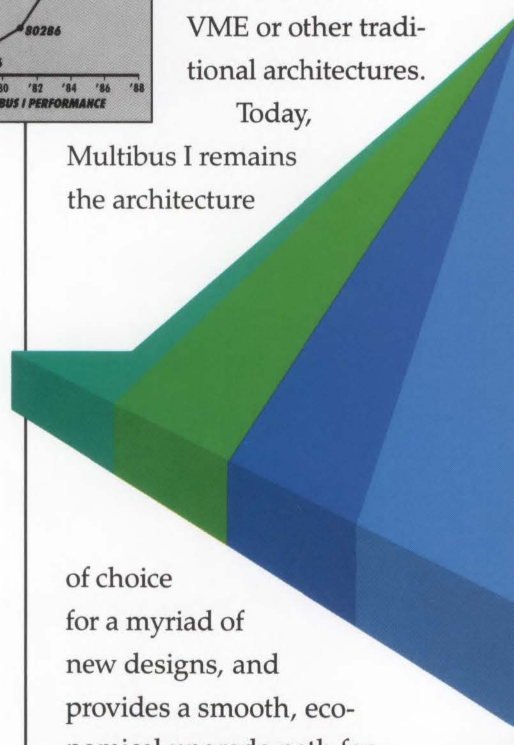

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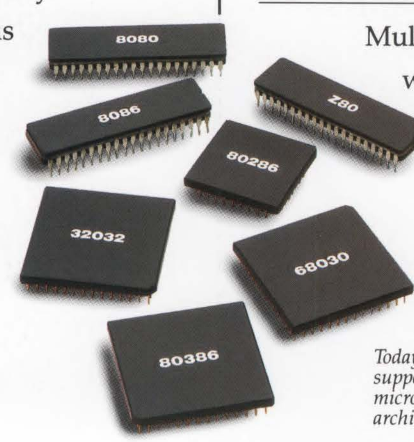
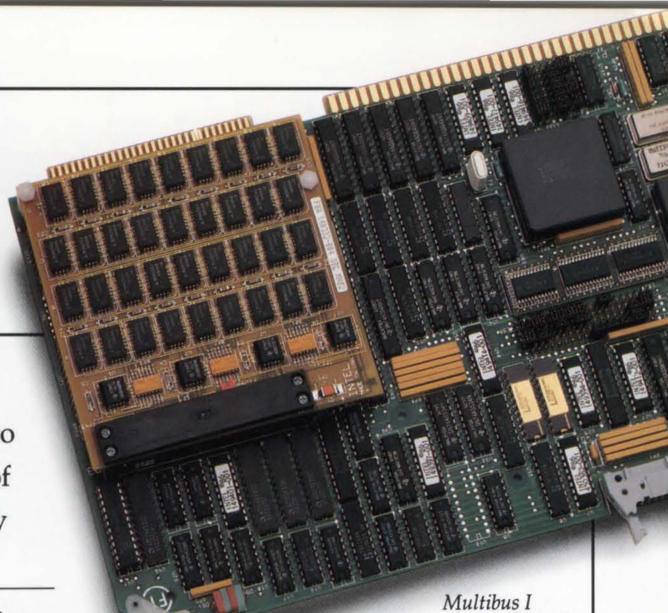
KEEPING PACE WITH TECHNOLOGY, WITHOUT COMPROMISING COMPATIBILITY.

Multibus I has done what no other architecture



Today's Multibus I supports every major microprocessor architecture.

FASTER, MORE THAN EVER BEFORE.



Multibus I provides 84 sq. in. of board space, large enough for high functionality, yet small enough to be economical in low density designs. The LBX and SBX bus extensions add low-cost memory expansion and I/O customization.

in history has been able to do: successfully absorb more than a decade of rapid technological advancement without compromising compatibility. From one generation of products to the next.

And from one vendor to the next.

In part this is due to the architecture itself, refined over the years by IEEE committees. In part it is due to the series of bus extensions that have helped Multibus I keep pace with the performance of newer buses.

But, mostly, Multibus I's success can be attributed to more than 240 manufacturers who have added their ingenuity to develop over 2,000 different Multibus I products to solve a wider range of applications than any other bus. Period.

WHAT'S NEW ON MULTIBUS I TODAY?

Today's Multibus I is loaded with exciting new products incorporating the latest VLSI and specialized technologies. You can use it to solve new applications efficiently and economically. And breathe new life into existing Multibus I applications.

Without expensive redesigns. And, without abandoning the comfort and security of the bus that's supported more success stories than we can even count.

THE BEST IS YET TO COME.

Recent months have seen many important new Multibus I hardware and software products. For the full story, circle the reader service number or contact the Multibus Manufacturers Group.

Each of the companies on the back of this ad will send you complete technical data on their latest offerings. Plus timely announcements of future new products.

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So don't delay. Find out what's new on Multibus I. And discover why the most successful commercial bus architecture in history is stronger, faster, more powerful, and more popular than ever!

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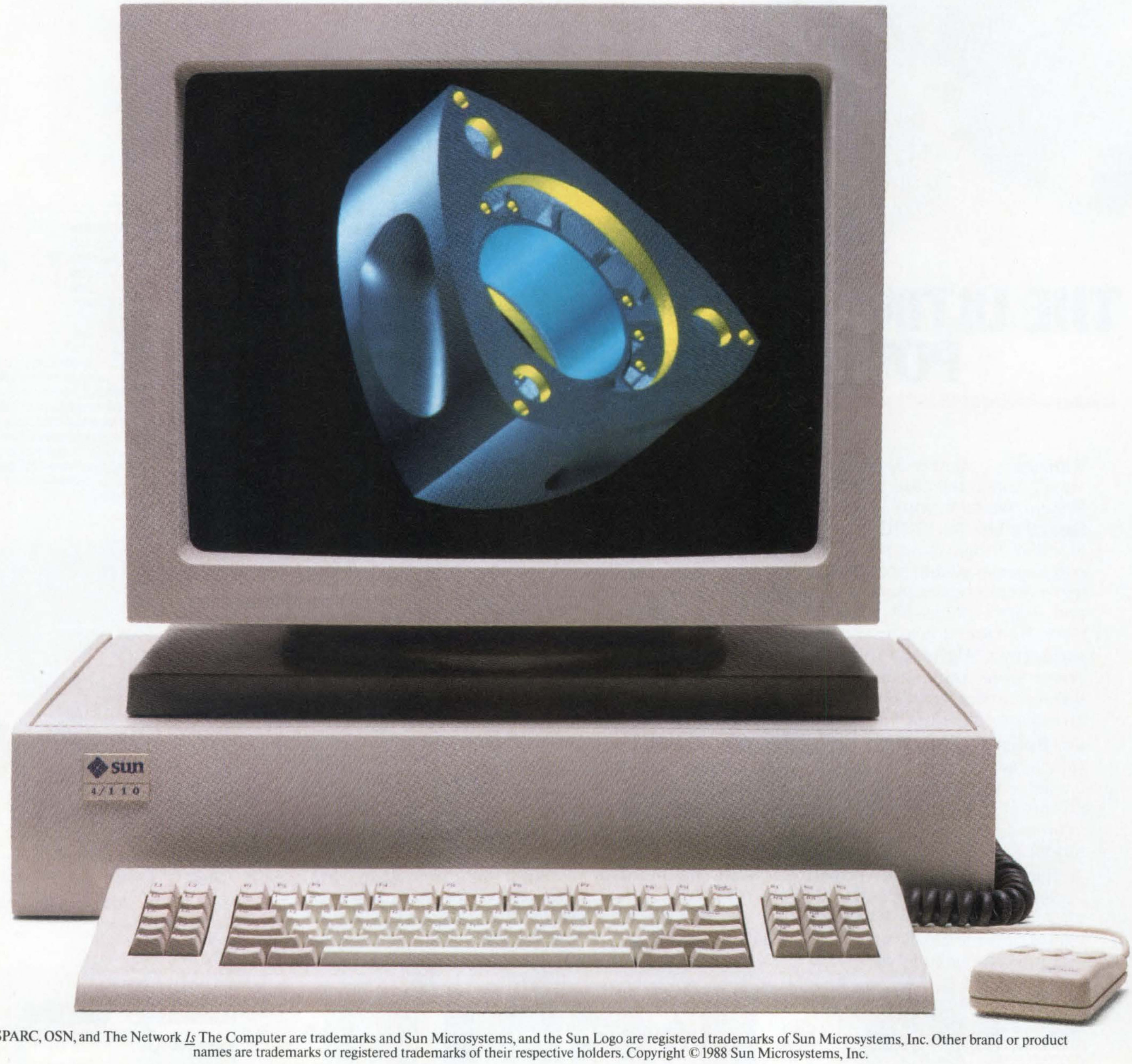

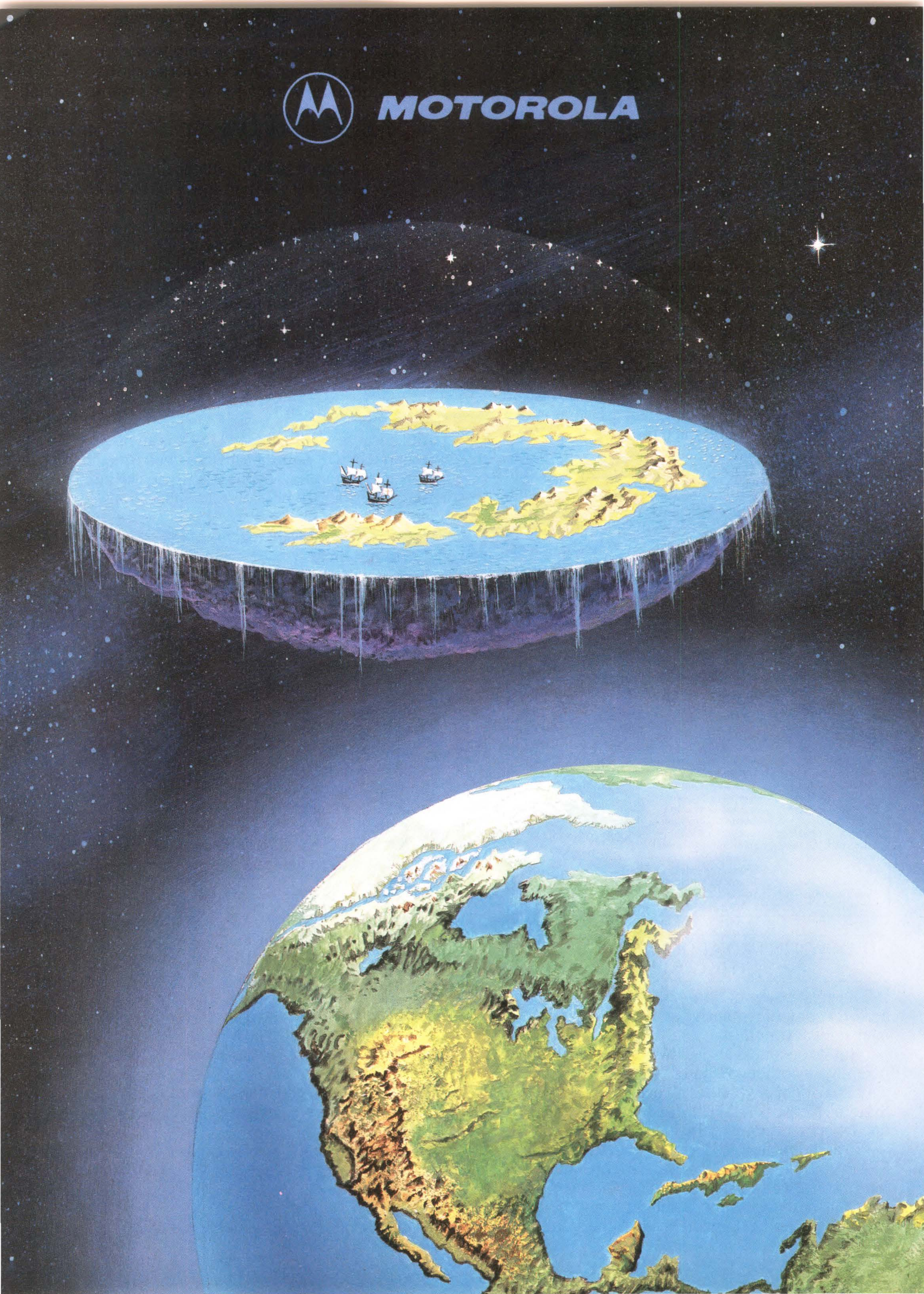
MOTOROLA

CALENDAR

Microwave IC Technology (seminar), Fullerton, CA. California State University, Office of Extended Education, Fullerton, CA 92634. (714) 773-3080. March 4.

Personal Computer Interfacing for Scientific Instrumentation Automation (short course), Blacksburg, VA. Linda Leffel, CEC, Virginia Tech, Blacksburg, VA 24061. (703) 961-4848. March 10 to 12.

Modern Electronic Packaging (seminar), San Diego, CA. Technology Seminars, Box 487, Lutherville, MD 21093. (301) 269-4102. March 15 to 17.

Microelectronic Packaging and Surface Mounting (seminar), Fullerton, CA. California State University, Office of Extended Education, Fullerton, CA 92634. (714) 773-3080. March 18.

10th Annual Conference for Inventors and Entrepreneurs, Denver, CO. Rocky Mountain Inventors Congress, Box 4365, Denver, CO 80204. (303) 443-3818. March 18 to 19.

Neural Networks for Artificial Intelligence, Arlington, VA. Technology Transfer Institute, 741 10th St, Santa Monica, CA 90402. (213) 394-8305. March 21 to 23.

Digital Signal Microprocessor and Microcomputer Chips and Development Systems (seminar), Cambridge, MA. Amnon Aliphas, DSP Associates, 18 Peregrine Rd, Newton, MA 02159. (617) 964-3817. April 4 to 6.

Microcircuit Interconnections and Assembly Methods (seminar), Fullerton, CA. California State University, Office of Extended Education, Fullerton, CA 92634. (714) 773-3080. April 7.

Electrostatic Discharge (ESD): Concern or Over-concern? (semi-

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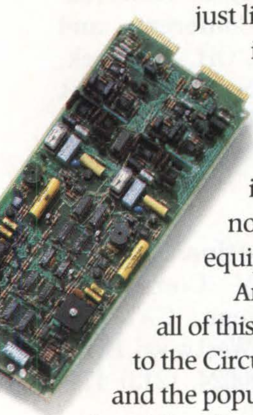

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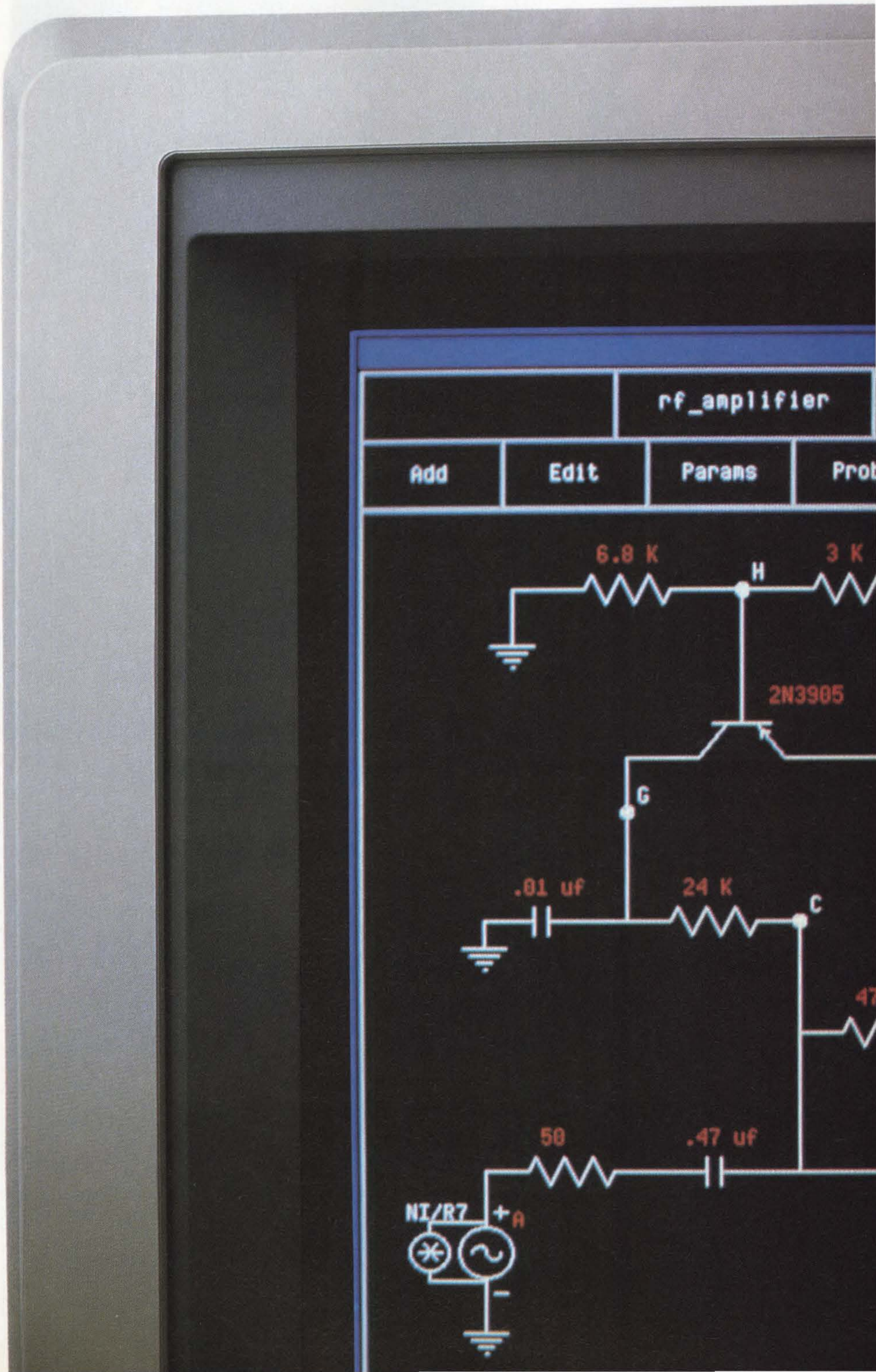

CALENDAR

nar), Fullerton, CA. California State University, Office of Extended Education, Fullerton, CA 92634. (714) 773-3080. April 12.

Hybrid Microcircuit Technology (seminar), Fullerton, CA. California State University, Office of Extended Education, Fullerton, CA 92634. (714) 773-3080. April 18.

American Power Conference, Chicago, IL. Robert Porter, Chicago Institute of Technology, Chicago, IL 60618. (312) 567-3202. April 18 to 20.

Instrument Society of America/IEEE Columbus Conference and Exhibit, Columbus, OH. Sol Black, AT&T Network Systems, Dept 11CB123430, 6200 E Broad St, Columbus, OH 43213. (614) 860-5605. April 19 to 20.

IEEE Instrumentation/Measurement Technology Conference (IMtc/88), San Diego, CA. Bob Myers, IMtc, 1700 Westwood Blvd, Los Angeles, CA 90024. (213) 475-4571. April 19 to 22.

Modern Electronic Packaging (seminar), Raleigh, NC. Technology Seminars, Box 487, Lutherville, MD 21093. (301) 269-4102. April 20 to 22.

Modern Microwave Techniques (short course), Los Angeles, CA. UCLA Extension, 10995 Le Conte Ave, Los Angeles, CA 90024. (213) 825-3344. April 25 to 28.

Pittsburgh Conference on Modeling and Simulation, Pittsburgh, PA. William Vogt or Marlin Mickle, 348 Benedum Engineering Hall, University of Pittsburgh, Pittsburgh, PA 15261. May 5 to 6.

EMC Expo, Washington, DC. Karen Smith, EMC Expo, Box D, Gainesville, VA 22065. (703) 347-0030. May 10 to 12.

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Besides speed, our new TTL SRAMs have a lot going for them.

Fast static RAMs have been disappearing fast lately. Some, by going up in a cloud of vapor. Others, like our new 64Ks, by breaking speed barriers.

They're taking off fast for good reason. Because for one thing, our new SRAM family is the only one being made in BiCMOS by a U.S. manufacturer. So you get *both* the high speed of bipolar *and* the low power of CMOS. Putting the technology of tomorrow into your products today.

Old memories are going, going, gone.

No matter what memory technology you're now using, our BiCMOS parts can replace it directly. They're pin-for-pin compatible with all industry-standard SRAMs. So you can go on working with the design rules you know. Yet get the advantages of next-generation process technology.

Advantages like a choice of 20-, 25-, 35-, or 45-nsec speeds. Yet these SRAMs draw no more current than conventional CMOS parts, while delivering twice the output drive. And they come in by-8 and by-4 organizations, with all the popular packaging options. In both commercial and military temperature ranges.

Order some to go today.

All your SRAM systems can be "go" today, with Saratoga's BiCMOS parts. Besides our 64K TTL line, we're shipping volume orders of our 4K and 16K TTL families, plus ECL SRAMs in 4K and 16K densities. These parts feature speeds as fast as 8 nsec, and full military temperature range operation.

So if you're not sure whether those other fast SRAMs are coming or going, check Saratoga. Call (408) 864-0500 today, or write Saratoga Semiconductor, 10500 Ridgeview Court, Cupertino, CA 95014.

At 20nsec, they're going fast.

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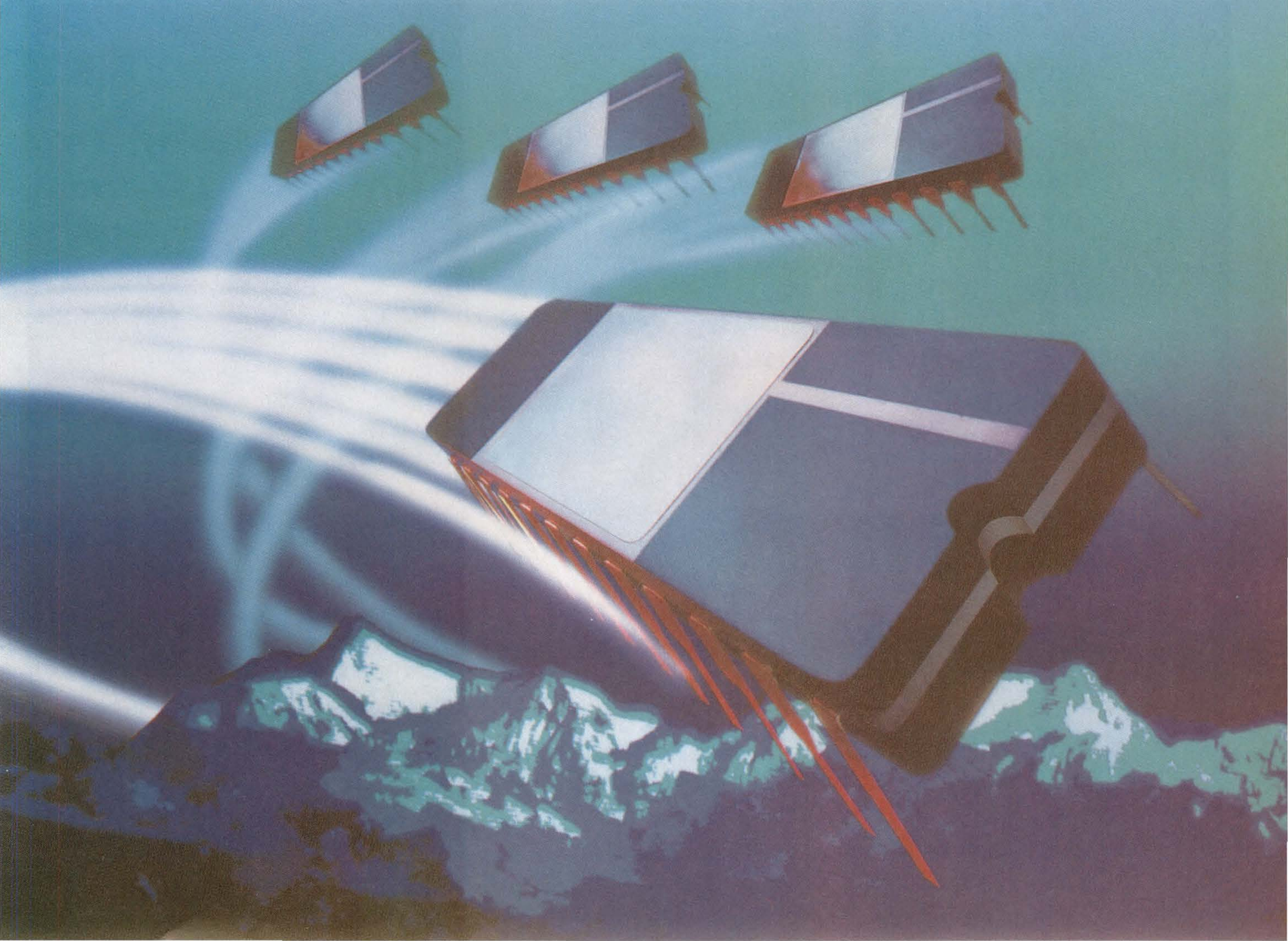

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BOARDMASTER's rules-driven methodology guides the most advanced set of layout tools available anywhere. Like 100% autorouting, with separate rip-up/reroute and manufacturing passes to increase board yields and reduce per unit costs.

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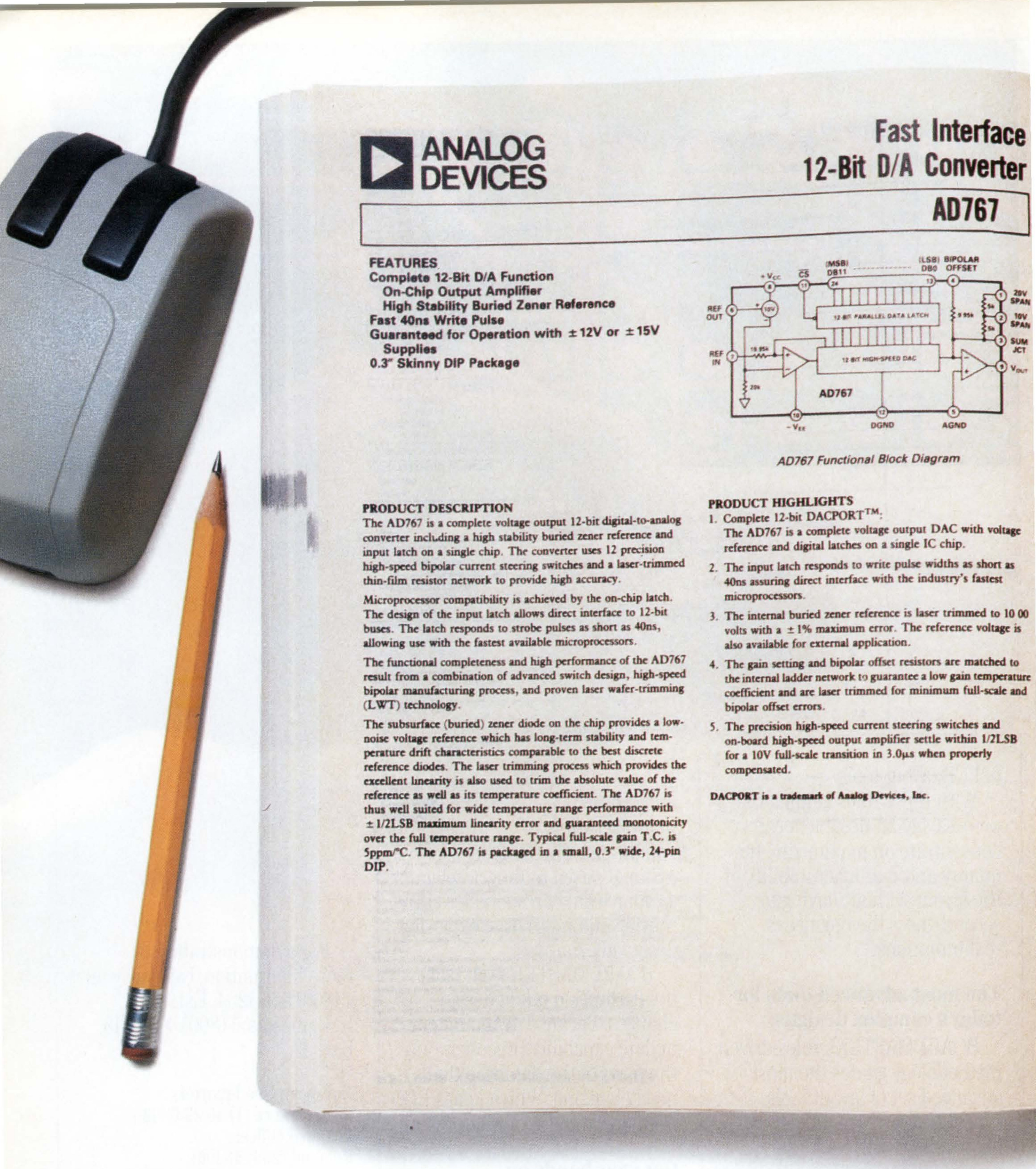

ANALOG DEVICES

Fast Interface 12-Bit D/A Converter

AD767

FEATURES
Complete 12-Bit D/A Function
On-Chip Output Amplifier
High Stability Buried Zener Reference
Fast 40ns Write Pulse
Guaranteed for Operation with ±12V or ±15V Supplies
0.3" Skinny DIP Package

AD767 Functional Block Diagram

PRODUCT DESCRIPTION

The AD767 is a complete voltage output 12-bit digital-to-analog converter including a high stability buried zener reference and input latch on a single chip. The converter uses 12 precision high-speed bipolar current steering switches and a laser-trimmed thin-film resistor network to provide high accuracy.

Microprocessor compatibility is achieved by the on-chip latch. The design of the input latch allows direct interface to 12-bit buses. The latch responds to strobe pulses as short as 40ns, allowing use with the fastest available microprocessors.

The functional completeness and high performance of the AD767 result from a combination of advanced switch design, high-speed bipolar manufacturing process, and proven laser wafer-trimming (LWT) technology.

The subsurface (buried) zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity is also used to trim the absolute value of the reference as well as its temperature coefficient. The AD767 is thus well suited for wide temperature range performance with ±1/2LSB maximum linearity error and guaranteed monotonicity over the full temperature range. Typical full-scale gain T.C. is 5ppm/°C. The AD767 is packaged in a small, 0.3" wide, 24-pin DIP.

PRODUCT HIGHLIGHTS

1. Complete 12-bit DACPORT™:
   The AD767 is a complete voltage output DAC with voltage reference and digital latches on a single IC chip.
2. The input latch responds to write pulse widths as short as 40ns assuring direct interface with the industry's fastest microprocessors.
3. The internal buried zener reference is laser trimmed to 10.00 volts with a ±1% maximum error. The reference voltage is also available for external application.
4. The gain setting and bipolar offset resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser trimmed for minimum full-scale and bipolar offset errors.
5. The precision high-speed current steering switches and on-board high-speed output amplifier settle within 1/2LSB for a 10V full-scale transition in 3.0μs when properly compensated.

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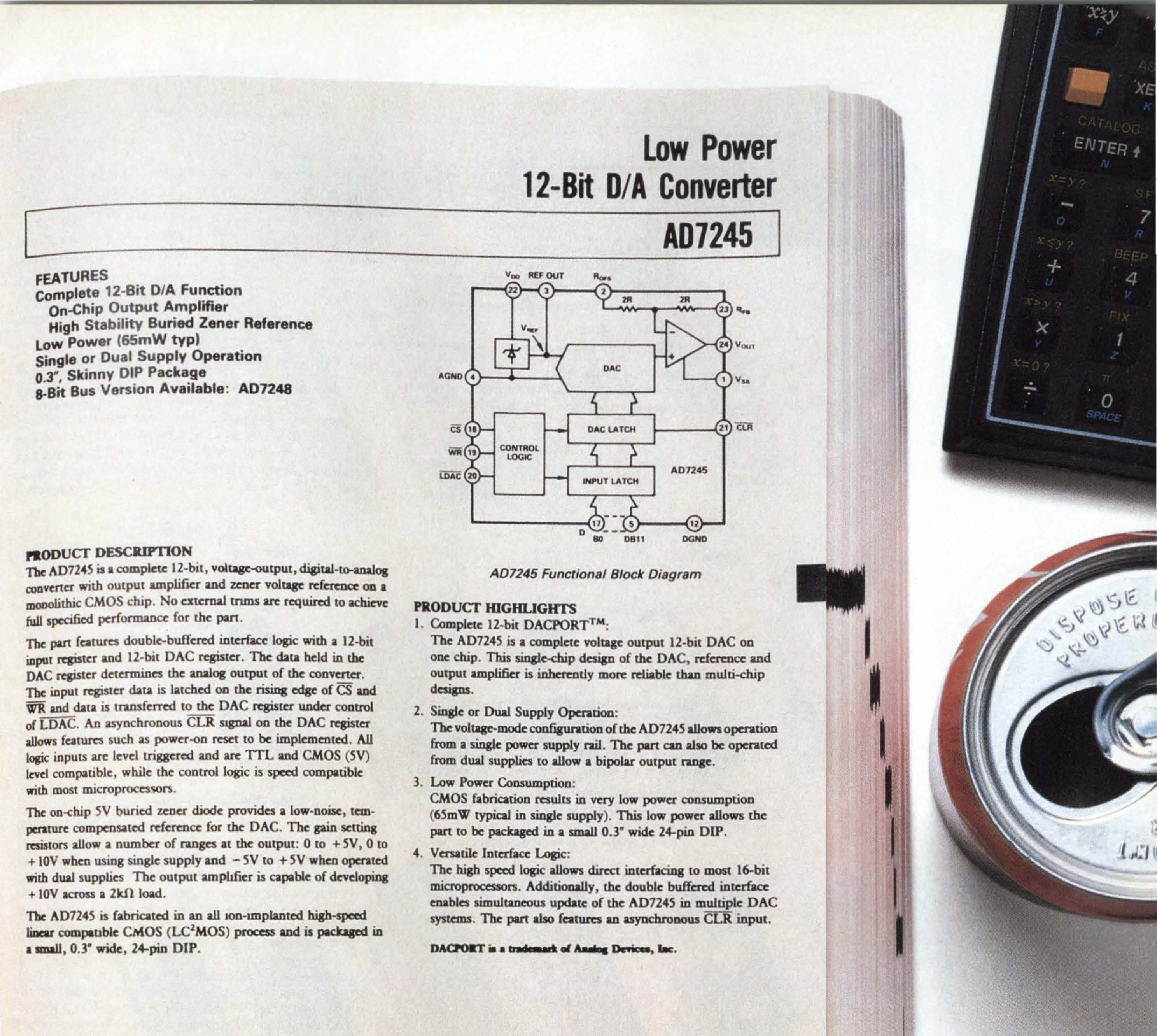
Bringing complete 12-bit DAC functionality and performance to your designs no longer requires having to deal with all the problems associated with external components. Instead, it simply requires specifying our new AD767 or AD7245.

Both the AD767 and AD7245 feature an on-chip stable buried Zener reference, output amplifier and microprocessor interface logic. And these complete functions come packed into skinny 0.3" DIPs. All this means you no longer have to deal with error budgets, product characterizations, or space constraints related to external components.

If digital interface speed is what you're after, the AD767 responds to pulse widths as short as 40ns, allowing it to be used with today's fastest processors. On the other hand, if low power dissipation is critical to your application, the LC²MOS AD7245 consumes only 65mW. There's also



FINALLY, THE COMPLETE STORY ON COMPLETE 12-BIT DACs.

an 8-bit bus version of the AD7245 (the AD7248) that loads in two bytes. Whether your need is determined by speed or power dissipation, it doesn't have to be limited by price. Our DACs come complete for as little as $8.40 (1000s).

To find out how the AD767 and AD7245 can tend to your complete 12-bit DAC needs, call Applications Engineering at (617) 935-5565 Ext. 2628 or 2629. Or write to Analog Devices, P.O. Box 9106, Norwood, MA 02062-9106.

ANALOG DEVICES

Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106; Headquarters: (617) 329-4700; California: (714) 641-9391, (619) 268-4621, (408) 559-2037; Colorado: (303) 590-9952; Maryland: (301) 992-1994; Ohio: (614) 764-8795; Pennsylvania: (215) 643-7790; Texas: (214) 231-5094; Washington: (206) 251-9550; Austria: (222) 885504; Belgium: (3) 237 1672; Denmark: (2) 845800; France: (1) 4687-34-11; Holland: (1620) 81500; Israel: (052) 28995; Italy: (2) 6883831, (2) 6883832, (2) 6883833; Japan: (3) 263-6826; Sweden: (8) 282740; Switzerland: (22) 31 57 60; United Kingdom: (932) 232222; West Germany: (89) 570050

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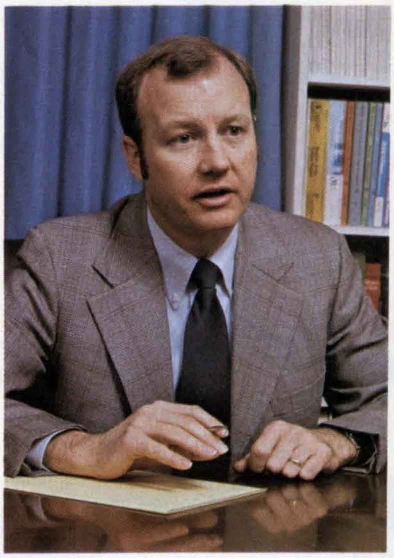
EDITORIAL

Building bridges



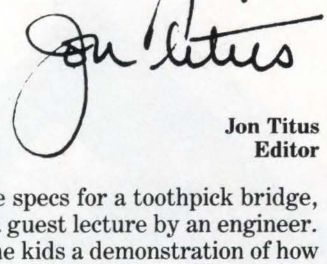
How many EE students could we expect to graduate if university professors were to tell each freshman engineering student the day before Spring break, "Go to Radio Shack, buy components, and build a working 10-GHz FM receiver." Assume, for example, that the professors give the students no explanation and no background information, only a list of specifications. After vacation, the faculty tests the designs, but never explains why one or two work and the others don't. Instead, it's back to simple dc circuits. Probably you couldn't find a better way to sour students on electrical engineering.

A ridiculous scenario? Maybe. But equally absurd situations do happen. During the past Christmas vacation, my son—an eighth grader—had to build a bridge out of toothpicks. The assignment included strict specifications for the length, width, and height of the span as well as the requirement that the bridge be able to support a 5-lb brick. Someone with a bit of mechanical know-how might be able to build a reasonable bridge, but most 13-year-olds don't have the vaguest idea of how forces act on bridges or on toothpick structures. The brick smashed most of the models and the teacher probably said, "Too bad, yours was a poor design."

Prior to vacation there was no preparation and no explanation of how bridges work. Likewise, after the bridges were tested there was no discussion of the lessons learned from the winning designs. Because the kids were never taught about structures and forces, they could have built 50 different bridge models, none of which could withstand the brick's force. The first thing most kids learn from the bridge-building experiment is that they hate building toothpick structures.

Also, because the teacher set a lofty goal that the kids couldn't reach without proper preparation, he taught them a subtle lesson: They are stupid. By diminishing our kids' self-esteem and their interest in new ideas, we destroy a precious resource—open, inquisitive minds.

The bridge-building assignment turns into an annoyance for the kids, who rebel against it, put it off until the last day of vacation, and give it as little attention as possible. Their reaction is easy to understand. Sometimes work assignments are a lot like toothpick bridges. I'm sure I've given people jobs to do without giving them the proper tools or without being sure they have the background and the skills to do the job. It's easy to assume that coworkers and subordinates share my enthusiasm and my goals, and that they have the same overall view of a project as I do. But it's not always so. When I make my next assignments, I'll try to remember the toothpick bridges.



Jon Titus
Editor

P S: If one of your youngsters brings home specs for a toothpick bridge, drop the teacher a note and suggest instead a guest lecture by an engineer. Also, you might find someone who can give the kids a demonstration of how a mechanical-CAD system evaluates simple structures.

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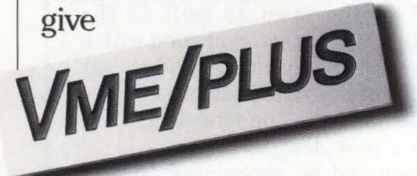


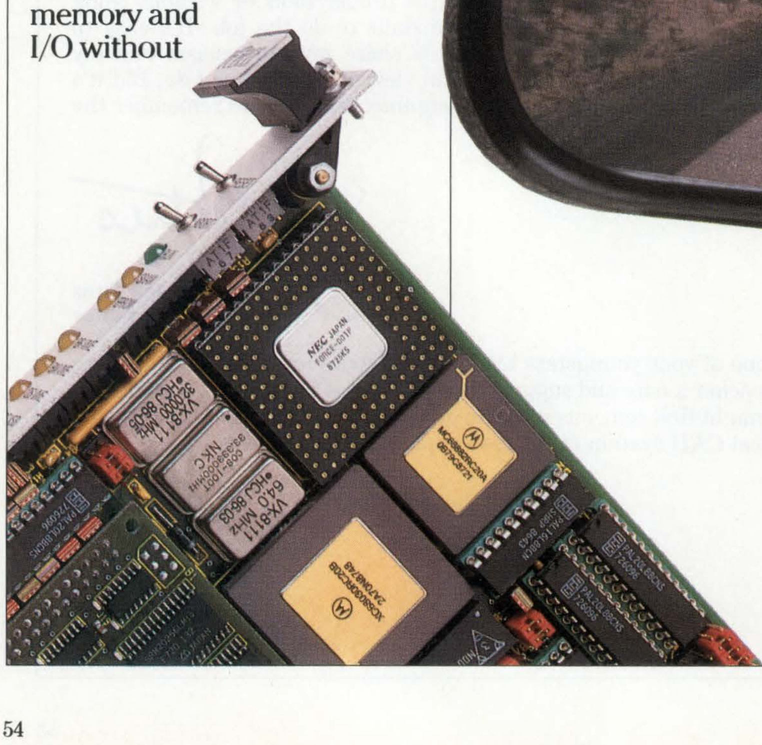
your project the kind of performance you've only dreamed about.

VME/PLUS gives you a choice of microprocessors, including a 68030 running at 25MHz without wait states. Complemented by 1MB of local memory. There's also a new VSB interface on P2. Which lets you add lots of local memory and I/O without increasing bus overhead. You also get two serial ports and up to 4MB of EPROM.

The result is system throughput that's way ahead of anything else in the VME world.

Think about the possibilities for real-time applications. For the first time, you can squeeze every ounce of performance from every processor. With no wasted overhead. And no stalls.

But that's only the beginning. The newest



you a different competition.

member of the VME/PLUS family, CPU-32, comes with a powerful new real-time, multitasking monitor called VMEPROM. It's resident in EPROM, so there's no license required and no extra charge.

CPU-32 also includes full support for real-time operating systems and UNIX 5.3.

CPU-32 CHARACTERISTICS	
PROCESSOR	68030/16.7 TO 25 MHz
CO-PROCESSOR	68882/16.7 TO 25 MHz
ZERO-WAIT-STATE SRAM	1MB
VMEPROM	REAL-TIME, MULTITASKING MONITOR
EPROM	UP TO 4MB @ 1 WAIT-STATE
SERIAL I/O	2 RS-232 CHANNELS
SECONDARY BUS SUPPORT	VSB

What this new technology means for you is unprecedented levels of speed and system throughput, exceptional reliability and – here's the best part – lower total system cost.

And if that's not enough, we also offer a full set of off-the-shelf peripheral boards and software. All VMEbus compatible. And guaranteed to cut the wait states out of your design cycle.

So if you're looking for the best way to stay ahead of your competition and your deadline, take a close look at VME/PLUS.

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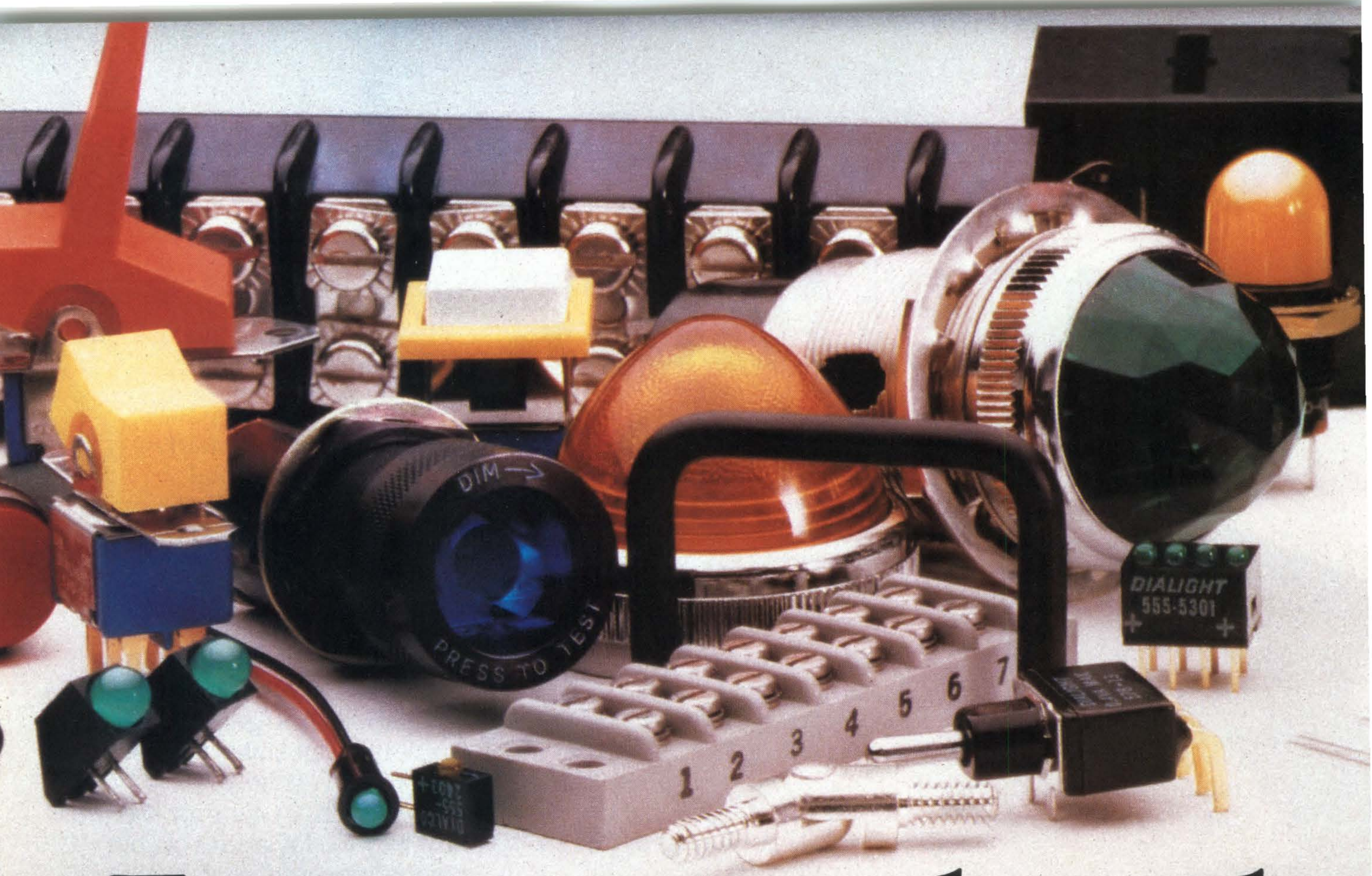

Engineering is the only

It's widely held that if you've seen one LED, you've seen them all. The same goes for things like terminal blocks and switches. A myth at times perpetuated by the very companies that make and market these products. With one notable exception.

Dialight Company.

Passive components, actively engineered.

We believe that passive components are no less important than integrated circuits. An attitude that's reflected in the way we go about our work.

Our design team is constantly assessing the manufacturing techniques of OEMs in every important technology. Anticipating ways to make our products easier and more economical to design-in and install (our invention, the Circuit Board Indicator is a good example).

They'll spend months developing a new compound for our sealed switches. Or devising a reliable way of testing each and every one of our Circuit Board Indicators and LEDs. They'll lose sleep over milliohms of contact resistance, or a fraction of an inch clearance on our switch terminals.

It's an attitude that's ultimately reflected in the products we sell.

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A product concept we pioneered over fifteen years ago to facilitate fast, reliable circuit board installation of LEDs, the Dialight Circuit Board Indicator is designed to insert and wave solder in up to one fourth the time at up to one fourth the cost of non-packaged LEDs.

All 100% tested and available in hundreds of standard and custom designs including the latest super-bright gallium aluminum arsenide units.

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No one makes more indicator lights for more applications than Dialight. Over a million designs accrued through fifty years of innovation. Incandescent, neon and LED units available in commercial and even the latest military configurations to meet MIL-L-85762A night vision requirements.

Dialight Switches

More than 100,000 designs that include illuminated pushbuttons, rockers, toggles and levers in a wide range of terminations, contact

commodity we sell.

ratings and mounting styles. All 100% tested. All customized to meet any application need.

Even sealed switches specifically engineered for board-mounted solvent washing with sealed O-rings to prevent seepage.

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Molded from special aggregates that in some models, withstand temperatures in excess of 155°C. Making Kulka the only manufacturer to meet B, F and HT requirements of MIL-T-55164C.

Standard features include solid brass, nickel-plated screws, molded-in contacts and special plates that prevent overtorquing and breakage. All readily engineered into any conceivable custom or special order.

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Dialight, Kulka and HHSmith products that speak of rigorous quality control, exhaustive testing and the Company philosophy of design and engineering: the word passive may be used to describe our components, but never the way we build them.

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In addition to basic kernel functions, it has reprogrammability, a human interface and on-target development.

iRMX 286 and the iRMK kernel are the latest developments in an operating system family we've been refining since real-time began for microprocessors. Currently, there are over half a million CPUs running iRMX, making it the most popular real-time O/S family in the world.

You'll also be glad to know that iRMX operating systems are solidly in touch with the rest of the real-time world. Our OpenNET™ Network connects it to VAX/VMS and even PC DOS compatibles.

REAL TIME COMPARISON			
	Interrupt Latency	Development Host	Regions
iRMK	10 μsec.	PC-DOS	yes
iRMX 286	13 μsec.	self hosted	yes
VAXELN	33 μsec.	VAX/VMS	no

What's more, iRMK and iRMX are easy to get started with. Because they run on our industry standard family of open system MULTIBUS hardware. Including our new 20 MHz 80386 MULTIBUS I and II boards. We even offer complete systems for OEMs like our new 80386-based System 320.

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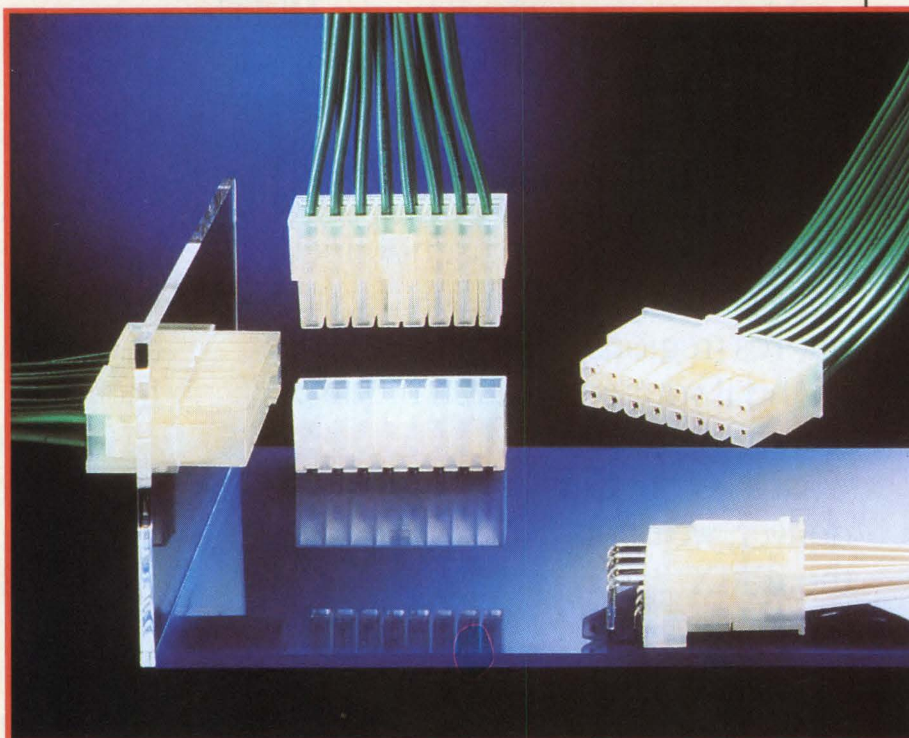

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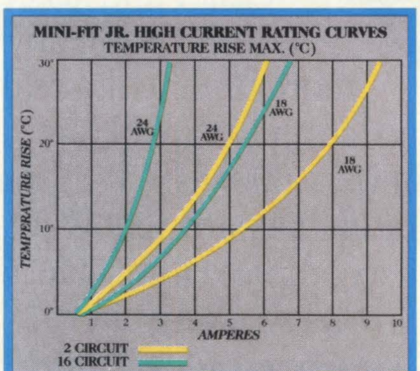

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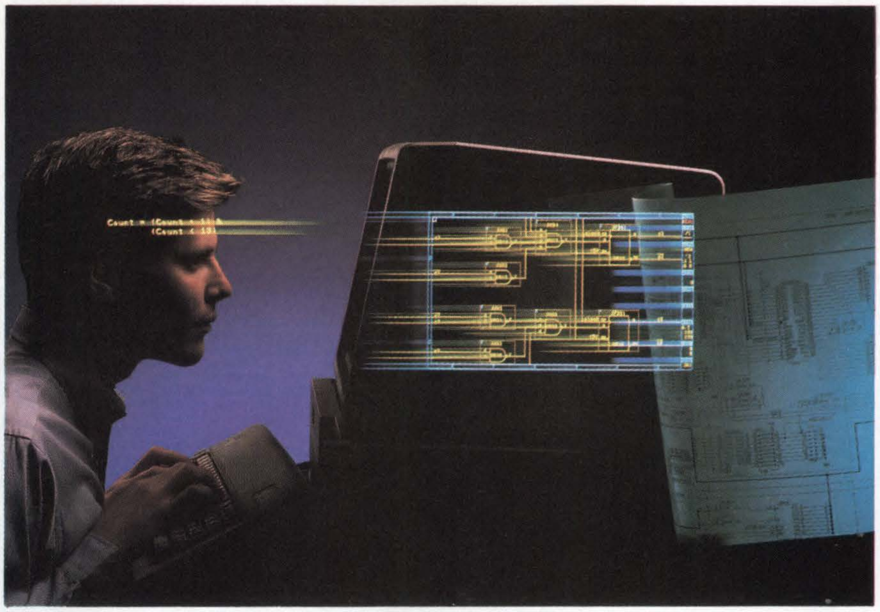
PLD-design software meets the challenge of multiple-device PLD applications

Charles H Small,
Associate Editor



Providing a semiautomatic logic partitioner, *Data I/O Futurenet's Futuredesigner can fit your logic designs into multiple PLDs or a gate array.*

Until recently, engineers have tried to implement as many logic functions as they could in a single programmable-logic device (PLD) in order to use as much as possible of the device's internal circuitry. Now, however, designers are realizing logic functions that are so complex that they must be mapped over several PLDs. This trend is particularly apparent for large state machines (see box, "Extending the classical state machine"), and it's straining the capabilities of many first-generation PLD-design software packages, which were designed to handle only one device at a time.

For aid in designing with multiple PLDs, you can turn to one of a number of more recent software packages. These packages range from simple, design-entry systems to very powerful packages that can select devices for you and partition designs semiautomatically or automatically.

You may be aware that multiple PLDs aren't the only solution to the problem of realizing extensive logic functions; you could employ one of the newer, very large PLDs instead. The manufacturers of these PLDs make available custom software packages that can handle logic specifications commensurate with the capacities of their devices. However, these large PLDs are not as fast as the fastest smaller PLDs, and many companies' inventory practices don't accommodate them, so you may, in some cases, still choose to gang several 20- or 24-pin PLDs rather than adopt one of the more commodious architectures.

Multiple PLDs also make sense for designers who use PLD designs only as an interim step, choosing to play it safe by prototyping large logic functions in PLDs before they realize the designs with gate arrays. For this kind of application, you might as well select the least expensive, most familiar parts.

Low-cost multiple simulation

Whatever your reason for developing a multiple-PLD design, you can choose from a fairly large assortment of design aids that range from simple to very powerful and come with prices ranging from nothing to tens of thousands of dollars. The lowest-cost package for multiple-PLD design is Signetics' Amaze—it's free to qualified customers. Amaze works with the firm's PLA (programmable-logic array) and PML (programmable macro logic) devices. When you use Amaze, you must manually partition and optimize your logic design. But once you've done this work, you can submit several compiled logic specifications to Amaze's simulator simultaneously to verify your multiple-PLD design automatically.

If you wish to design with PALs instead of PLAs, you can combine MMI's Palasm 2 and Royal Electronic's Logicsim ($79). Like Amaze, Palasm 2 has an unbeatable cost/performance ratio (it's free and it works) and it handles all of MMI's and AMD's programmable-logic devices. Palasm 2 is also like Amaze in that it requires you to partition your logic design manually. After you've derived the sets of Boolean equations for your partitioned design, you must submit your equations to Logicsim, because Palasm 2's simulator can handle only one device specification at a time.

Logicsim is a simple register-transfer logic (RTL) simulator that can handle several PLD specifications simultaneously as long as all the devices' signal names are consistent. In fact, it can work with *any* PLD-design software that produces

Boolean equations. (Most PLD-design systems offer an option that lets you print out reduced Boolean equations no matter which design-entry format you use—truth-table, schematic-capture, state-machine, state-diagram, or waveform.) You'll probably have to do some minor editing on the file of Boolean equations to put them in the right format for Logicsim.

As anyone who's ever attempted the task will testify, partitioning a logic function over several PLDs is a difficult task. The architecture of the devices you select greatly influences the choices you can make in partitioning your design. A designer must also juggle such factors as device cost, device speed, power consumption, and alternate sourcing.

In general, there's no closed solution to the problem of selecting devices and partitioning and minimizing logic designs—especially for designs that use several asynchronous clocks or asynchronous preset and clear inputs. Given enough time and talent, a designer can massage the equations of almost any design so that they'll fit into a particular device. Therefore, optimizing a logic design is an iterative process. Iterative processes, by their very nature, consume a lot of time, whether it's the designer's time or computer time.

If your budget can stand some greater expenditures, you can get more computer assistance: Futuredesigner from Data I/O Futurenet and LOG/iC from Kontron (Isdata in Europe) offer help in two different areas.

Extending the classical state machine

The theory of classical state machines predates digital electronics. Now that you can obtain PLDs that have computer-like features such as subroutine stacks and microprogrammed architectures, you'll need to extend the classical state machine to take full advantage of these devices' features and to employ modern hierarchical-design methods.

Theoretically, the most compact and abstract description of a Mealy state machine is the mathematician's 5-tuple:

$$(\mathbf{I}, \mathbf{Z}, \mathbf{Q}, \omega, \delta),$$

where vector **I** is the set of inputs to the state machine, vector **Z** is the set of states, vector **Q** is the set of outputs, and ω and δ are a pair of functions that relate inputs to next states and inputs to outputs, respectively.

Although the mathematical representation of a state machine serves to focus attention on the machine's elements, engineers do not find this mathematical representation particularly illuminating. They prefer, instead, to use a For-Next table (**Fig Aa**). In a For-Next table, each row of the table corresponds to a state of the state machine. The column headings correspond to the machine's inputs. At each intersection of a row and column are two elements: the output that the machine makes in response to the input and the next state of the machine.

But the more abstract, mathematical representation of a state machine does serve neatly as a starting point for describing state-machine extensions formally. Engineers have, for some time, employed an ad hoc, undocumented extension to the classical state machine by allowing for both registered, state-dependent outputs and asynchronous outputs (which are not accounted for in the mathematician's 5-tuple).

You can further extend the classical state machine in two ways: first, by replacing the input vector **(I)** with a more flexible menu vector **(M)**, and second, by replacing the output vector **(Q)** with a more powerful action vector **(A)**. The menu

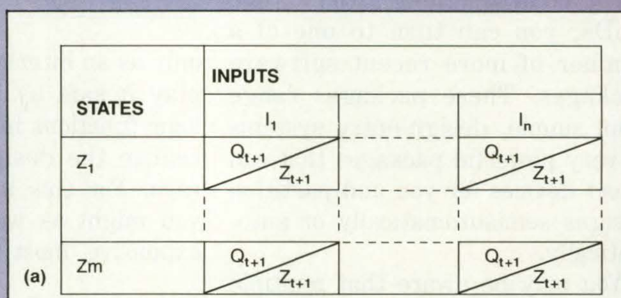


Fig A—You can extend the classical Mealy state machine (a) in two ways to accommodate new PLDs having microprogrammed architectures and return stacks. As b shows, you can first substitute a set of menu choices appropriate to each state for the fixed array of inputs in a and then expand the notion of the output vector (Q) in a into the action vector (A) in b. The action vector allows the state machine to emit a sequence of outputs as well as jumps to and from submachines.

Futuredesigner is, among other things, a semiautomatic logic partitioner. It derives partitioned logic equations for a multiple-PLD design if you first select the devices and then specify which logical output will be assigned to which PLD's output pin. Depending on the options you buy, Futuredesigner can also simulate multiple-PLD designs. Futuredesigner's pricing is complex: $7990 for logic-equation, state-machine, and truth-table design entry (the price includes an IBM PC coprocessor board); $3990 for schematic capture; and $5500 for a Cadat simulator plus $800 for PLD/Cadat translation software.

Kontron's LOG/iC, on the other hand, can automatically select devices and partition your design, but only if you use PLAs; if you use other devices, you must perform device selection and partitioning manually. The PLA package is $1995; packages for other devices and simulators cost more.

Besides LOG/iC, a number of other experimental automatic device-selection, minimization, and partitioning programs also prefer to work with the more flexible devices such as PLAs, or PLDs having programmable macrocells (the 22V10 or GAL (generic array logic) devices, for instance), rather than PALs, which have a more rigid architecture. Two recently announced software packages carry PLD-design automation a step further, however: They work with all PLDs, not just the flexible ones.

Hewlett-Packard's HP PLD design system, for example, runs on HP 9000 Series 300 workstations; it

vector (**M**) is itself a set of vectors, each vector being the set of allowable inputs for a given state. The action vector (**A**) includes the classical output vector (**Q**) but also allows the state machine to enter or exit other state machines, perform a series of actions, or emit asynchronous outputs. The expanded state machine becomes, therefore:

$$(\mathbf{M}, \mathbf{Z}, \mathbf{A}, \omega, \delta).$$

To understand why you need a menu vector for complex systems, consider, for example, electrical-drafting programs. These programs can have more than 800 commands. To represent something as complex as a state machine, you would need a For-Next table having more than 800 columns, which is clearly far too cumbersome. Therefore, when you model a large state machine having many inputs, instead of having all the inputs active all the time and ranging them across the top of the For-Next table, you recast the For-Next table so that only the allowable inputs for each state—or each line of the table—are entered right above each action/next-state entry (**Fig Ab**). Note that with this menu-like representation, your For-Next table no longer needs to be rectangular; each state has only as many entries in the table as it has allowable inputs.

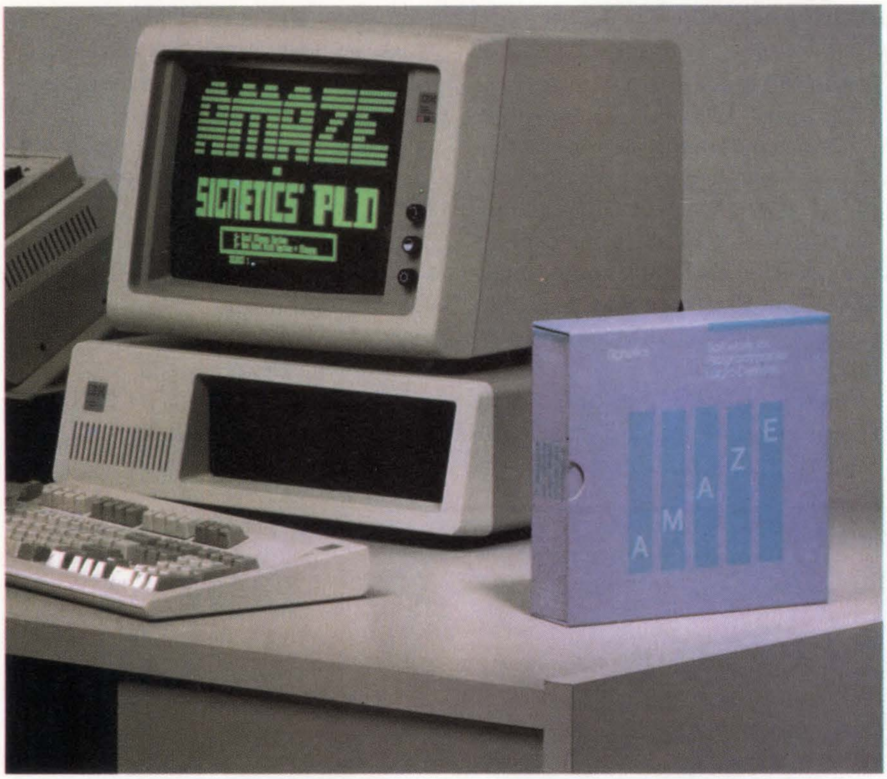
Meanwhile, the output vector (**Q**) is replaced with the action vector (**A**). The action vector (**A**) allows you to break a large state machine up into a hierarchical design and to take advantage of newer PLDs' return stacks and microprogrammed architectures.

In response to an input, the expanded state machine's action vector (**A**) can emit the classical state machine's single output (**Q**) as well as a series of outputs (assuming you have chosen a microprogrammed architecture to implement your state machine) or emit asynchronous outputs.

Additionally, the expanded state machine can invoke (or Enter) a lower-level state machine. Naturally, the action vector, **A**, also allows a corresponding Exit operation to leave a lower-level state machine and return control to the higher-level state machine. The term for a lower-level state machine is "submachine."

The classical state machine has no memory. It doesn't know where it came from; it knows only where it's going. To see how the concept of the submachine proves useful, consider a simple tape recorder. The recorder has buttons for stop, play, record, rewind, fast forward, and pause. The recorder's specification accepts the pause button as an allowable input when the recorder is playing, recording, rewinding, or fast forwarding. Further, the spec also states that pressing the pause button a second time should return the recorder to its previous state.

To model the operation of this tape recorder, a classical state machine would need four pause states—one each for the play, record, rewind, and fast-forward states. Modeling the recorder with an expanded state machine would involve only a single pause submachine. Pressing the pause button, in any allowable state, would cause the recorder state machine to invoke (or Enter) the pause submachine. The only allowable input to the pause submachine is the pause button. Pressing the pause button again causes the pause submachine to execute an Exit and return control to the recorder state machine.



***Even a low-cost PLD design system such as Amaze** (from Signetics) can help you with multiple-PLD designs if its simulator can at least verify a multiple-PLD specification.*

costs from \$8000 to \$14,500. (With the exception of HP PLD, all the software packages mentioned here run on IBM PCs; an IBM PC/XT or PC/AT with a hard disk is just about mandatory for these programs because of their extensive device libraries and user screens.) When you use HP PLD, you first enter your logic design without worrying about device selection. The program then automatically selects devices and partitions your design over several devices, if necessary.

Similarly, Minc's Logic Designer (\$4500) allows you to enter your logic design in a variety of design-entry formats without first selecting a device. Logic Designer, too, searches its library of device types for the best fit for your logic specification. In contrast, older programs force you to try to compile your design into a given device; if your design won't fit, you have no choice but to resubmit the logic equations after choosing a different part. This hit-or-miss method can prove to be time consuming and frustrating.

HP's HP PLD and Minc's Logic Designer take into consideration such device-specific factors as power consumption, pricing, and inventory restrictions when making an automatic device selection. Also, both packages have a new method of logic-design entry—waveform entry. Both packages allow you to employ a graphics editor to draw input and output waveforms from which the programs deduce logic equations. You could, for example, copy a μP's I/O signals from its hardware manual and combine the μP's signals with the waveforms from a peripheral IC's spec sheet. The programs then could automatically design a PLD that would serve as an interface between the μP and the peripheral IC—all without your having to write a single Boolean equation.

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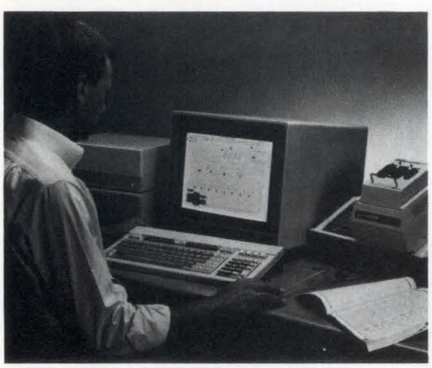

***The HP PLD software package automatically** selects devices and fits complex PLD designs into multiple devices as necessary.*

For more information . . .

For more information on the PLD-design software described in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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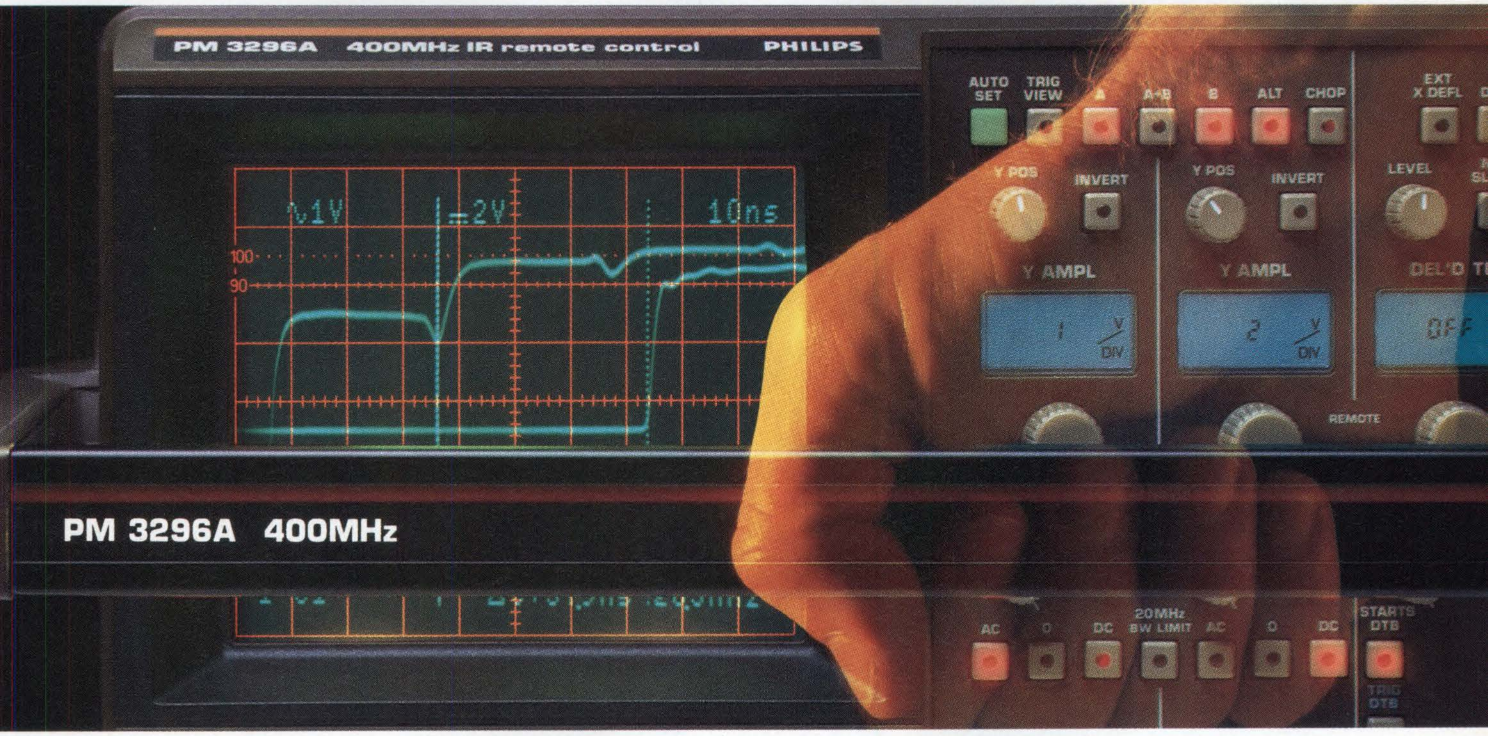

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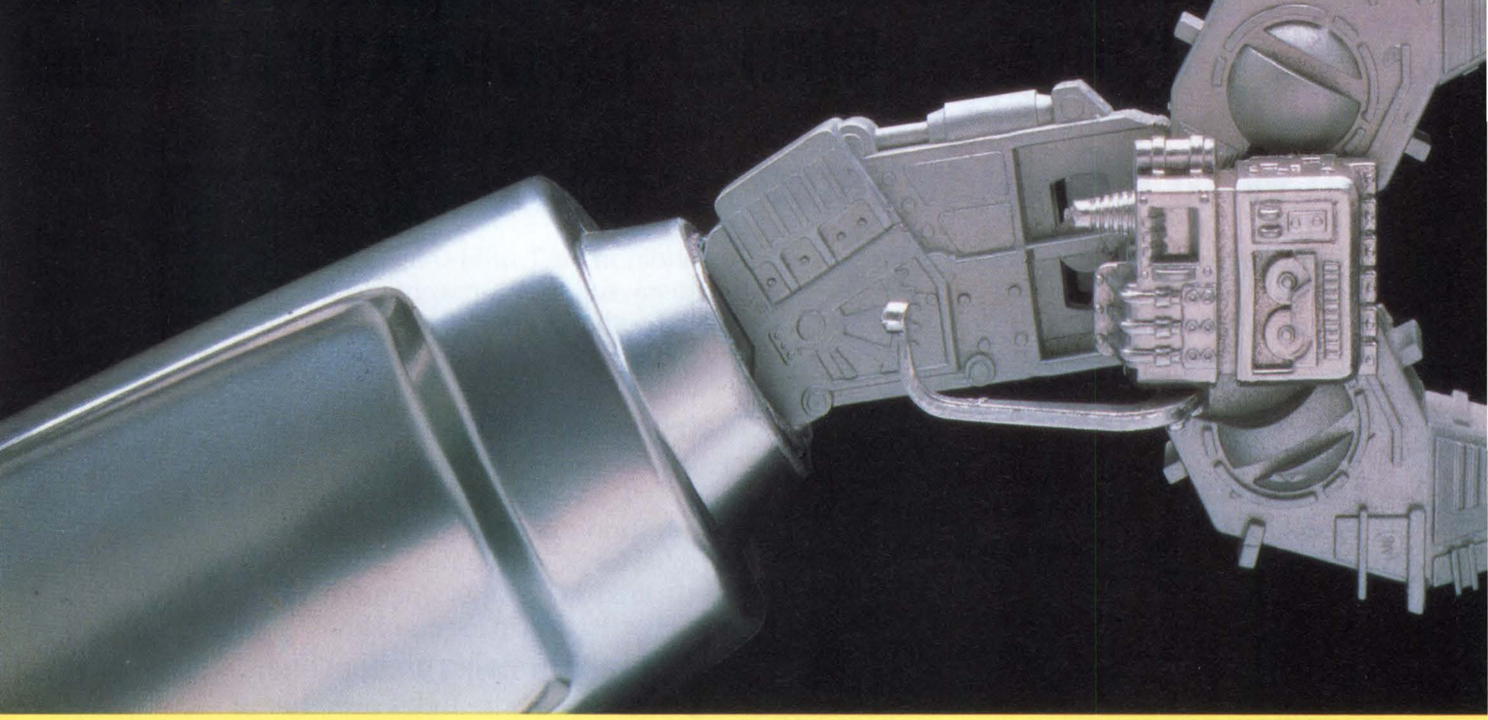

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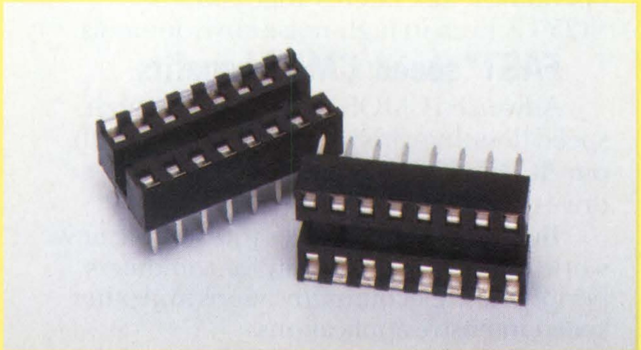

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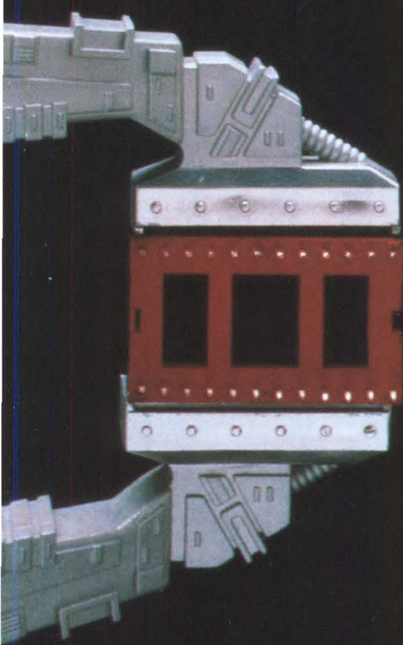

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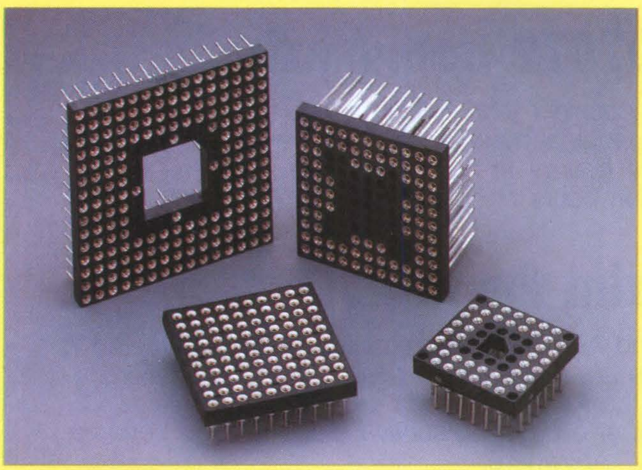

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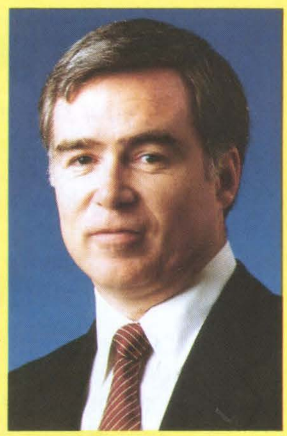

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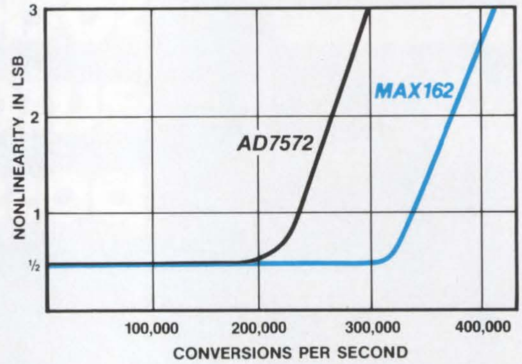

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* Maxim Reliability Report RR-IC 1987.

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Growing array of 1-chip dc/dc converters provides power for diverse applications

Dave Pryce, *Associate Editor*

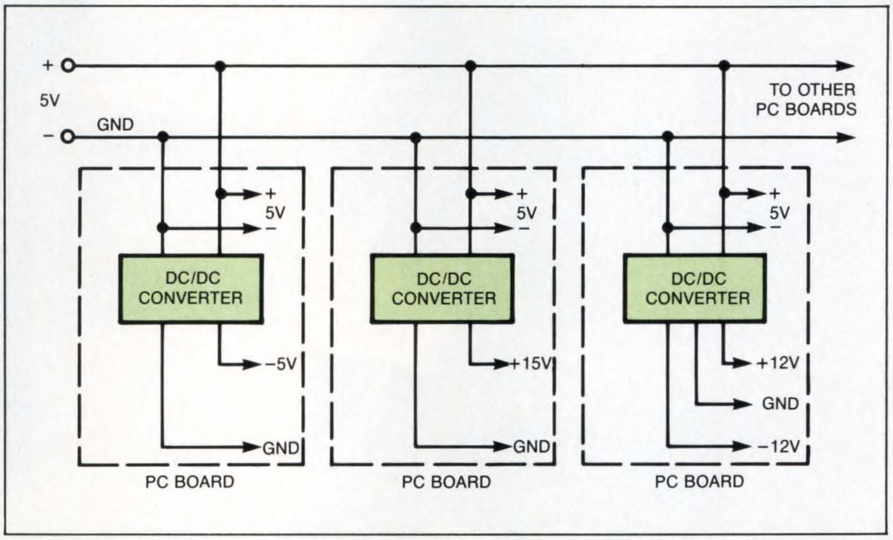

Fig 1—Monolithic dc/dc converters provide easy solutions *to the need for different voltages throughout a system. Shown here are three converters, operating from a 5V bus, that step up the bus voltage and/or invert its polarity.*

The increasing variety of chip-level dc/dc converters is not only changing the way system designers structure conventional power supplies, but is also providing solutions to applications problems that were previously satisfied only by more costly and cumbersome approaches. A single, low-power monolithic IC can supply the exact amount of voltage needed for specific pc-board functions, and high-power types can simplify the design and reduce the component count of many power supplies.

The conventional way to obtain multiple dc outputs is to generate them in the main power supply and then bus them to the needed points throughout the system. An alternative approach, and one that is becoming increasingly popular, is to use the power supply's main dc output (typically 5V for computer systems) and distribute it to the various boards throughout the system for conversion to a different voltage by a small, monolithic dc/dc converter. An example of this approach is shown in **Fig 1,** where three board-level converters generate −5, 15, and ±12V from a standard 5V bus.

Distributed power has advantages

Using a distributed approach gives you several advantages: It reduces the size and complexity of the main power supply, allows the local generation of the different voltages needed by analog circuits, and simplifies any subsequent design modifications. Not so obvious, but perhaps equally important, is that the distributed approach reduces regulation problems associated with voltage drops across lengthy wire runs (paricularly those carrying high current). Further, the local-converter approach minimizes decoupling problems.

Monolithic dc/dc converters are also useful for generating higher voltages when operated from low-voltage battery supplies such as 1.5 and 3V. Some of the new CMOS converters are particularly efficient for low- to medium-power applications. Conversely, other dc/dc converters are specifically designed to convert a high input voltage, such as the −48V from a telephone line, to a lower voltage for powering digital and/or analog systems.

Most monolithic dc/dc converters are essentially switching-regulator circuits that include the output switch, but not the usual bells and whistles associated with the typical PWM switch-mode control circuit. With the possible exception of some types that are capable of handling high voltages, dc/dc converters are designed for ease of use and low end-system cost; any required housekeeping features are usually built into the devices.

Converters take three forms

Depending on their input-voltage range and the output voltage (or voltages) they deliver, dc/dc converters take one of three basic forms:

- Boost (or step-up) converter **(Fig 2a)**—In this converter, the output voltage is higher than the input voltage. The higher output voltage is a result of the voltage developed across the inductor, which stores energy as a function of the switching frequency and the duty cycle.
- Buck (or step-down) converter **(Fig 2b)**—This converter's voltage is lower than its input voltage. The converter chops the input voltage into a pulse train. The switching duty cycle determines the output voltage, but the inductor voltage does not add to the input

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voltage as is the case with the boost converter.

- Buck-boost (or step-up/step-down) converter **(Fig 2c)**—This converter's output voltage can be either higher or lower than its input voltage, depending on the duty cycle of the switching. This type of converter inverts the polarity of the output with respect to the input.

Typical examples of the currently available crop of low-power CMOS converters are two devices from Maxim Integrated Products. The MAX632 and MAX636 **(Fig 3)** are complementary in nature; both operate from an input voltage of 5V, but the MAX632 provides a positive 12V output, and the MAX636 provides a negative 12V output. Each device comes in an 8-pin plastic DIP.

These converter types are ideal for powering low-power analog circuits from a 5V digital bus. They're relatively inexpensive and require very few external components. The MAX632 even includes a built-in diode, although you can use an external diode for greater efficiency, if you wish. For best results, the external diode should be a switching type such as the 1N4148 or the 1N5817 (Schottky).

Standard rectifier diodes designed to work at 60-Hz line frequency don't function very well at switching frequencies in the 40-kHz range. When used as shown in **Fig 3**, the MAX632 provides an output of 12V at 25 mA (with about 85% efficiency) and the MAX636 provides an output of −12V at 15 mA (with about 75% efficiency) **(Ref 1)**.

Model LM3578 from National Semiconductor is a versatile bipolar device that you can use as a step-up (boost) converter, a step-down (buck) converter, or (with the aid of an external transistor) a polarity-inverting, step-up/step-down (buck-boost) converter. **Fig 4** shows the internal functions of the device, which has some unusual features. The input comparator stage has both inverting and noninverting inputs that simplify circuit design, and you can reference the external current-limit circuitry to either ground or the V_S pin.

Depending on the chosen configuration, you can take the output from either the collector or the emitter of the output transistor. The LM3578 operates from any dc voltage in the 2 to 40V range and can supply output currents as high as 750 mA. The oscillator frequency is adjustable to 100 kHz, and duty cycles to 90% are possible. As is the case with many low- to medium-power dc/dc converters, the LM3578 comes in an 8-pin DIP.

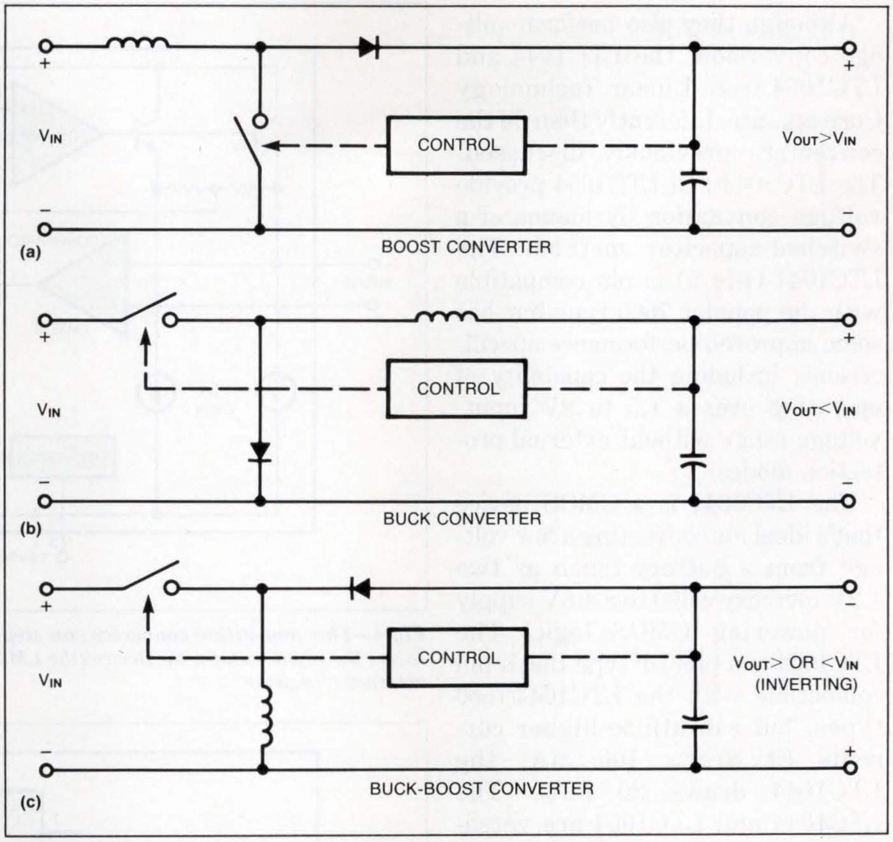

*Fig 2—**A dc/dc converter can take one of three basic forms.** The boost converter **(a)** steps up the input voltage, the buck converter **(b)** steps down the input voltage, and the buck-boost converter **(c)** can either step up or step down the input voltage while inverting its polarity.*

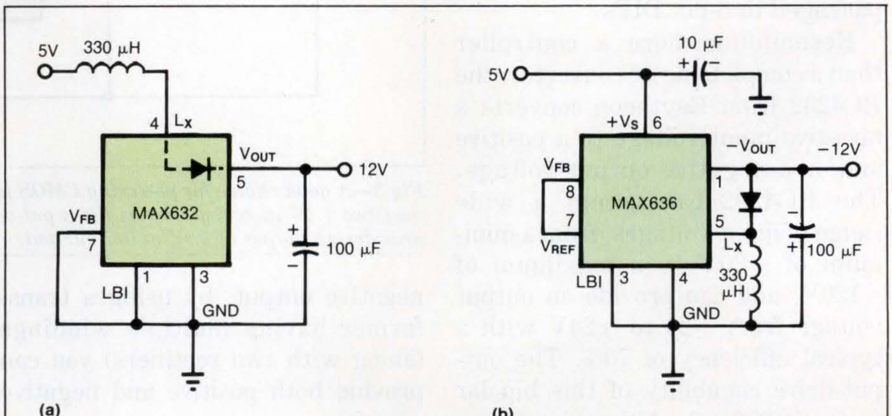

*Fig 3—**Low-power CMOS converters** are ideal for providing the unique voltage requirements of analog circuits from a 5V digital bus. Here, two different models provide 12V **(a)** and −12V **(b)** for different applications.*

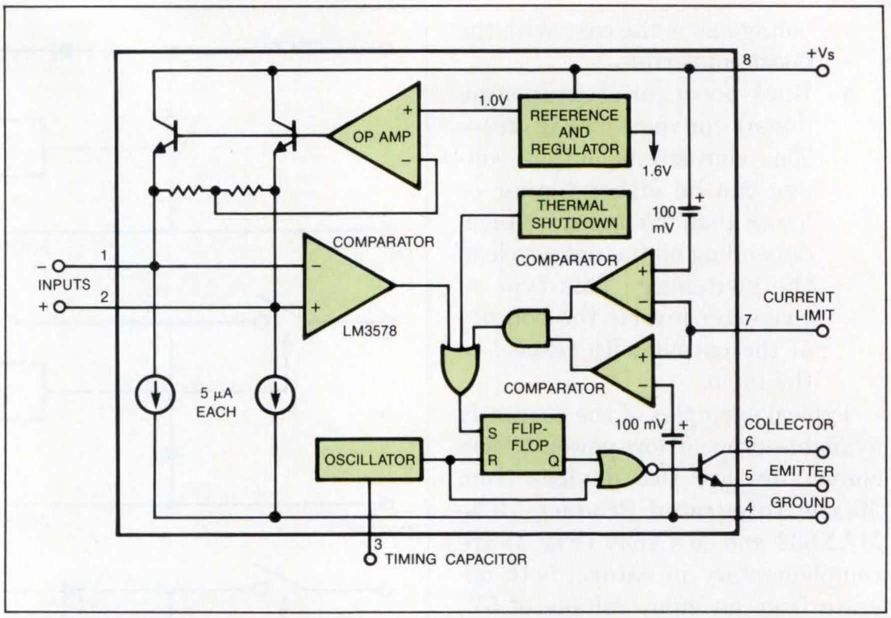

Fig 4—This monolithic converter can step up, step down, or invert the input voltage. To invert the input voltage, the device (the LM3578 from National Semiconductor) requires an external transistor.

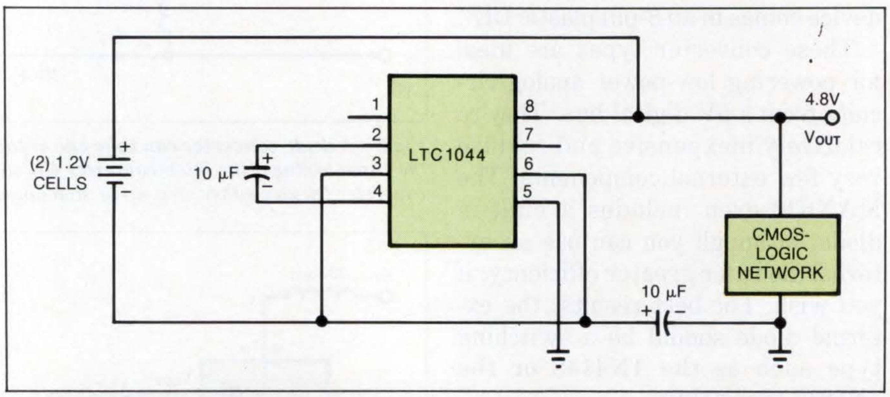

Fig 5—A good choice for powering CMOS logic, the LTC1044 from Linear Technology Corp uses two 1.2V mercury cells as the input-voltage source in this application. The converter provides an output of 4.8V at low current.

Although they also perform voltage conversion, the LTC1044 and LTC1054 from Linear Technology Corp operate differently than do the converters previously discussed. The LTC1044 and LTC1054 provide voltage conversion by means of a switched-capacitor method. The LTC1044 (**Fig 5**) is pin compatible with the popular 7660 type but has some improved performance specifications, including the capability of operating over a 1.5 to 9V input-voltage range without external protection diodes.

The LTC1044 is a CMOS device that's ideal for converting a low voltage from a battery (such as two 1.2V mercury cells) to a 4.8V supply for powering CMOS logic. The LTC1054 is a bipolar type that's pin compatible with the LTC1044/7660 types, but can utilize higher currents (it draws 100 mA; the LTC1044 draws 20 mA). The LTC1044 and LTC1054 are versatile, low-power devices. You can use them to double, halve, or invert an input voltage. Both converters are packaged in 8-pin DIPs.

Resembling more a controller than a complete dc/dc converter, the RC4292 from Raytheon converts a negative input voltage to a positive and/or a negative output voltage. The RC4292 can accept a wide range of input voltages, from a minimum of −20V to a maximum of −120V, and can provide an output voltage from −24 to +24V with a typical efficiency of 70%. The output-drive capability of this bipolar device is 350 mA. Although you can use the IC on a stand-alone basis, most applications of the RC4292 incorporate an external power transistor and a transformer.

One such application is shown in **Fig 6**, in which the RC4292 converts the off-hook telephone-line voltage of −48V to a 5V output suitable for powering digital circuits. The external power MOSFET drives the transformer, which steps down the supply voltage. By rearranging the output rectifier, you can provide a negative output; by using a transformer having multiple windings (along with two rectifiers) you can provide both positive and negative outputs.

Similar to the Raytheon RC4292 in their ability to handle high input voltages are the Si9100 and Si9102 from Siliconix. These D/CMOS types, however, include the power switch on chip and offer a somewhat more versatile architecture. These more-complex devices therefore require a 14-pin DIP rather than the 8-pin DIP of the RC4292. The Si9100 has an input-voltage range of 10 to 70V and can supply 350 mA of output current. The Si9102 has an input-voltage range of 10 to 120V and an output-current rating of 250 mA.

Although you can use them without a transformer for nonisolated applications, the Si9100/9102 find principal use in transformer-coupled flyback- and forward-converter applications. Such applications include ISDN and PBX equipment, modems, and distributed-power systems. Thanks to their high input-voltage ratings, you can operate these devices directly from the −48V telephone line. The 120V-rated Si9102 can operate from −96V double-battery telecommunications power supplies.

Climbing to the high-power rung of the dc/dc-converter ladder, you can find types from Linear Technology Corp, Lambda, and SGS that are capable of providing output currents from 1.5 to 10A.

The LT1070 from Linear Technology Corp has an input-voltage range of 3 to 60V and can deliver 5A output current; it's available in either a 5-pin TO-3 package or a 5-pin TO-220 package. The LT1070 is a current-mode control chip. This operating mode offers the advantages of pulse-by-pulse current limiting and the reduction of the 90° phase shift in the inductor **(Ref 2).**

Several high-power dc/dc converters are available from Lambda Semiconductors. The LSH6300 Series includes devices that have cur-

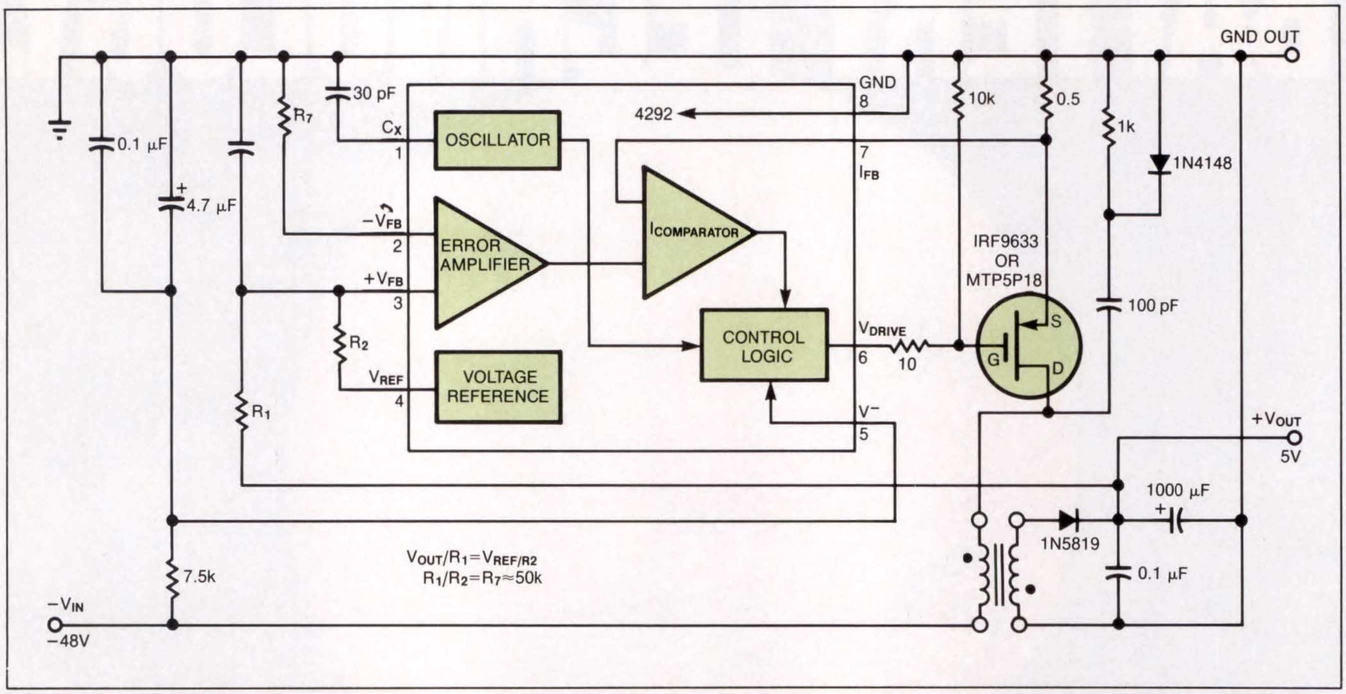

*Fig 6—**Useful in telecomm applications,** this circuit uses the RC4292 from Raytheon to convert the off-hook telephone-line voltage of −48V to a 5V output suitable for powering digital circuits.*

REPRESENTATIVE MONOLITHIC DC/DC CONVERTERS

VENDOR	PART NUMBER	INPUT VOLTAGE (V)	OUTPUT VOLTAGE (V)	OUTPUT CURRENT (A)	OPERATING FREQUENCY (kHz)	PROCESS TECHNOLOGY	PACKAGE	PRICE
LAMBDA	LSH6325P	12 TO 35	5 TO 27	2	70	BIPOLAR	5-PIN TO-200	$11.22 (100)
LINEAR TECHNOLOGY CORP	LT1070	3 TO 60	CIRCUIT-DEPENDENT	5	40	BIPOLAR	5-PIN TO-3 5-PIN TO-220	$9.60 (100) $7.45 (100)
	LTC1044	1.5 TO 9	V_{OUT} = 2V_{IN}	0.020	10	CMOS	8-PIN DIP	$1.95 (100)
	LT1054	3.5 TO 15	V_{OUT} = V_{IN}/2 V_{OUT} = −V_{IN}	0.100	35	BIPOLAR	8-PIN DIP	$2.95 (100)
MAXIM INTEGRATED PRODUCTS	MAX630	2 TO 16.5	$V_{OUT} > V_{IN}$	0.375	75	CMOS	8-PIN DIP	$3.50 (100)
	MAX638	3 TO 16.5	$V_{OUT} < V_{IN}$	0.375	65	CMOS	8-PIN DIP	$3.32 (100)
	MAX632	2 TO 12.6	12	0.325	50	CMOS	8-PIN DIP	$3.50 (100)
	MAX636	2 TO 16.5	−12	0.375	50	CMOS	8-PIN DIP	$3.32 (100)
	MAX680	2 TO 6	4 TO 12 −4 TO −12	0.010	8	CMOS	8-PIN DIP	$2.16 (100)
NATIONAL	LM3578	2 TO 40	$V_{OUT} > V_{IN}$ $V_{OUT} < V_{IN}$	0.750	100	BIPOLAR	8-PIN DIP	$1.40 (1000)
RAYTHEON	RC4292	−20 TO −120	−24 TO 24	0.350	100	BIPOLAR	8-PIN DIP	$2.65 (1000)
SGS	L4962	9 TO 46	5 TO 40	1.5	150	BIPOLAR	16-PIN POWER DIP	$1.50 (10,000)
	L4970	15 TO 50	5 TO 40	10	500	BCD	15-PIN MULTIWATT	$4.50 (10,000)
SILICONIX	Si9100	10 TO 70	$V_{OUT} < V_{IN}$	0.350	120	D/CMOS	14-PIN DIP	$5.43 (100)
	Si9102	10 TO 120	$V_{OUT} < V_{IN}$	0.250	120	D/CMOS	14-PIN DIP	$5.97 (100)

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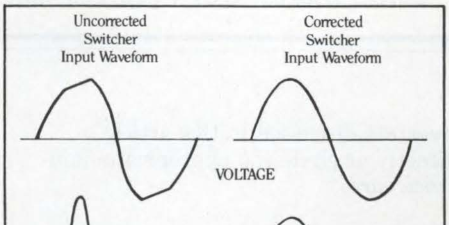
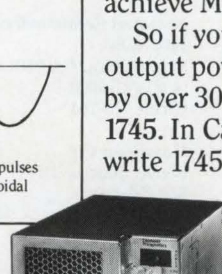


Power factor correction converts the high current pulses characteristically drawn by a switcher into a sinusoidal waveform, in-phase with the line voltage.



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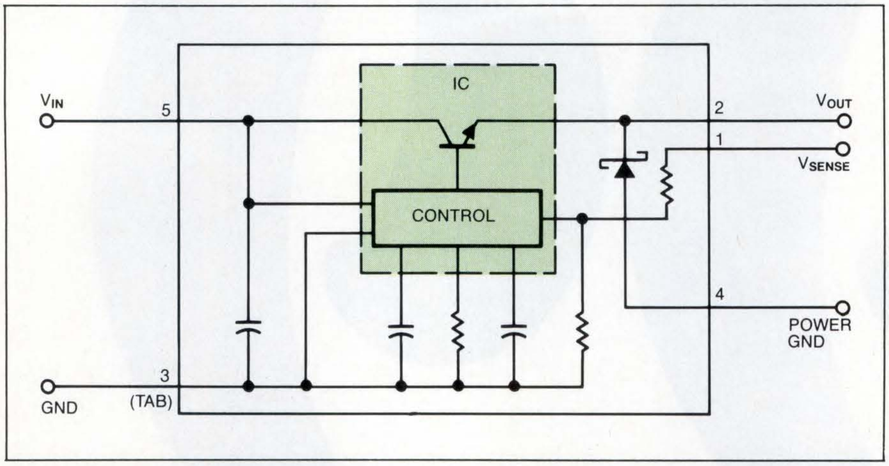

Fig 7—This hybrid 2A dc/dc converter *from Lambda integrates a monolithic control/power chip with a Schottky diode, thick-film resistors, and chip capacitors on a single substrate.*

rent ratings of 2, 3, and 5A. The LSH6300 types **(Fig 7)** are actually miniature hybrids packaged in a TO-220 case. In each of these devices, however, the monolithic section is the heart of the converter: It contains the regulator, error amplifier, comparator, oscillator, current-limit circuitry, logic circuits, and output switching transistor.

The monolithic chip—along with a Schottky diode, thick-film resistors, and chip capacitors—is mounted on a ceramic substrate. You need to add only an external inductor and one or two capacitors to form a complete step-down dc/dc converter. The LSH6300 converters are normally set for a 5V output, but you can program each device for higher voltages by adding a resistor between the output pin and the sense pin.

Finally, two more excellent examples of high-power dc/dc converters are the L4962 and L4970 from SGS Semiconductor. The L4962 is a bipolar device that has an input-voltage range of 9 to 46V, an output-current rating of 1.5A, and a maximum operating frequency of 150 kHz. The L4962 is housed in a 16-pin power DIP. For high-power applications, the L4970 has an input-voltage range of 15 to 50V and an output-current rating of 10A. The L4970 is fabricated in a bipolar-CMOS-DMOS (BCD) process that allows you to operate the device at frequencies as high as 500 kHz. Because of its high-current and high-power capabilities, the L4970 comes in a rugged 15-pin package (called "Multiwatt") that has a long metal tab that aids in dissipating heat.

Although your present designs may not need the assistance of a dc/dc converter, chances are that future ones will. The use of a single system-supply voltage (usually 5V) is increasing in popularity, and it's a simple matter to provide the required on-card voltages for analog circuits by using a small, monolithic dc/dc converter that can step up or invert the bused voltage.

Monolithic converters can also simplify the design of your system power supply by combining several functions on a single chip. Although manufacturers of ICs are responding to the need for single-supply components by introducing new op amps, comparators, A/D converters, and other analog circuits, the use of the traditional dual-supply analog circuit will probably dominate most applications for an extended period. Whatever your application's needs, it's likely that one of the available dc/dc converters will satisy them. **EDN**

For more information . . .

For more information on the dc/dc converters discussed in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

Lambda Semiconductors
121 International Dr
Corpus Christi, TX 78410
1-800-255-9606
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Linear Technology Corp
1630 McCarthy Blvd
Milpitas, CA 95035
(408) 432-1900
Circle No 702

Maxim Integrated Products
510 N Pastoria Ave
Sunnyvale, CA 94086
(408) 737-7600
Circle No 703

National Semiconductor Corp
Box 58090,
Santa Clara, CA 95052
(408) 721-5000
Circle No 704

Raytheon Co
Semiconductor Div
350 Ellis St
Mountain View, CA 94043
(415) 968-9211
Circle No 705

SGS Semiconductor Corp
1000 E Bell Rd
Phoenix, AZ 85022
(602) 867-6100
Circle No 706

Siliconix Inc
2201 Laurelwood Rd
Santa Clara, CA 95054
(408) 988-8000
Circle No 707

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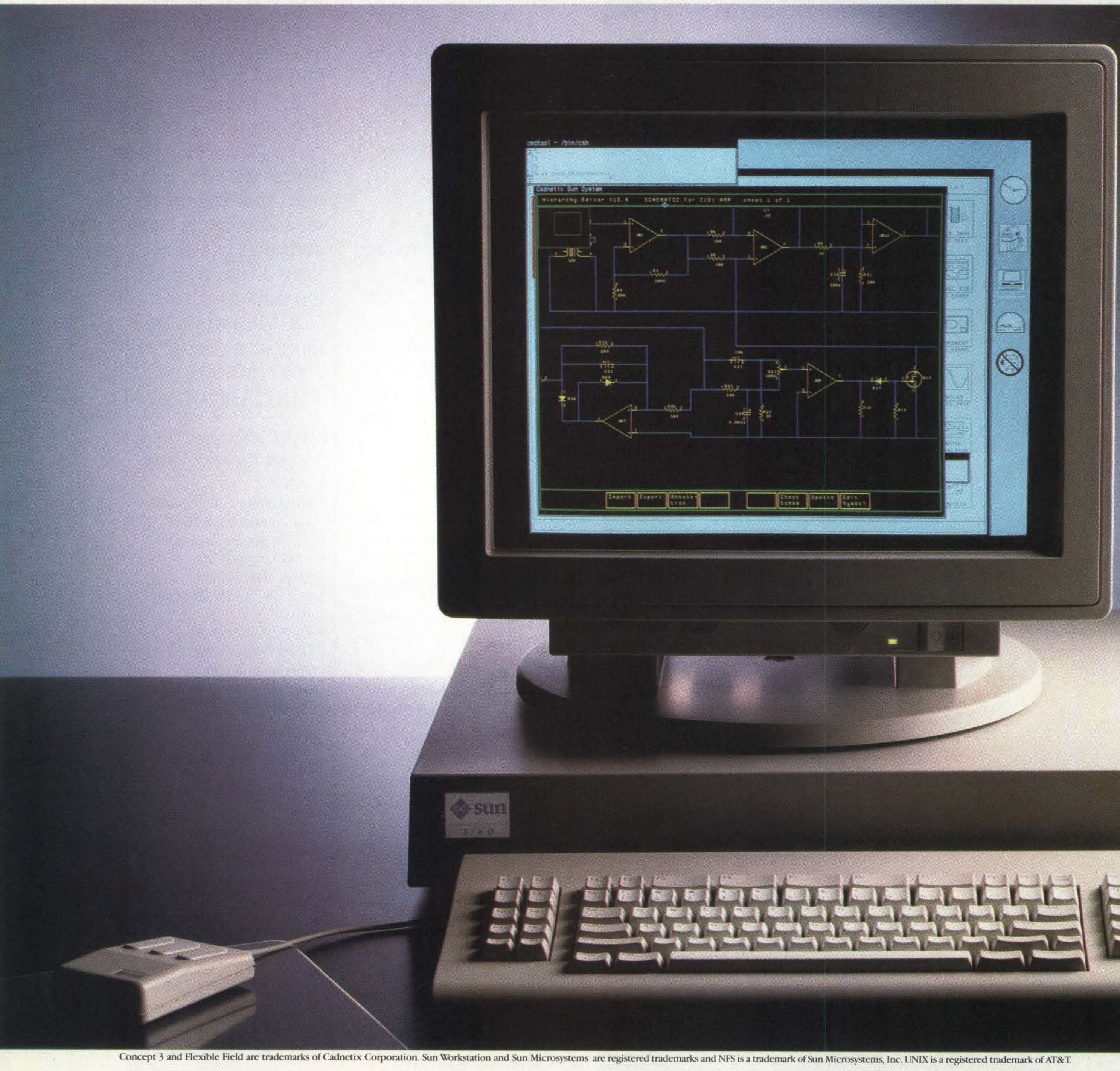

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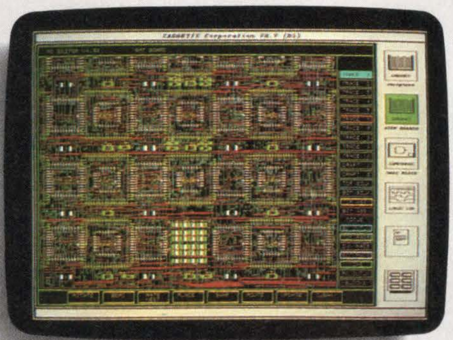

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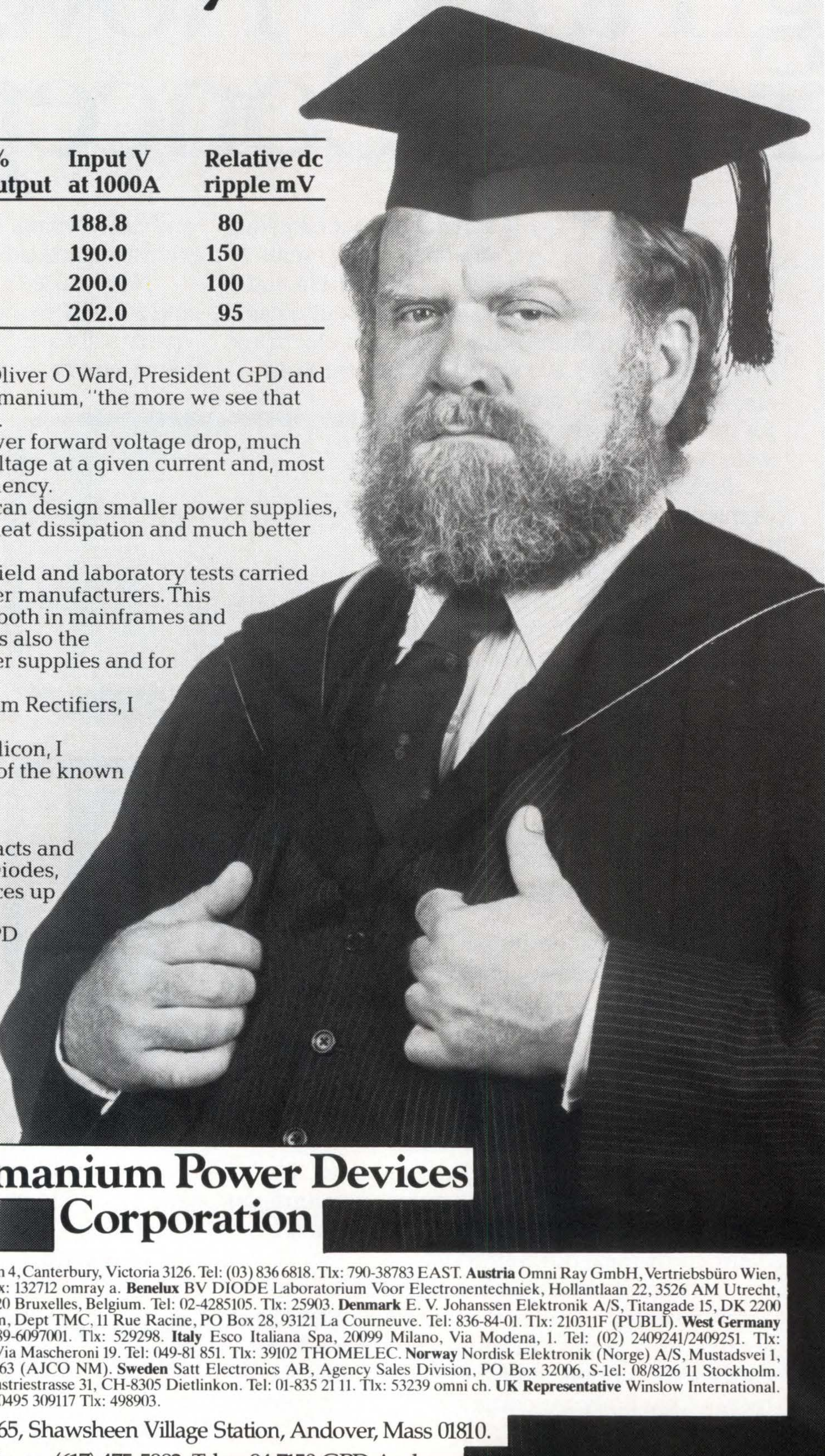

Device	Peak Vf at 1000A	Rel. Eff. % at 5kW output	Input V at 1000A	Relative dc ripple mV
Germanium	0.60	86.5	188.8	80
Schottky	1.00	85.0	190.0	150
Silicon A	1.20	76.0	200.0	100
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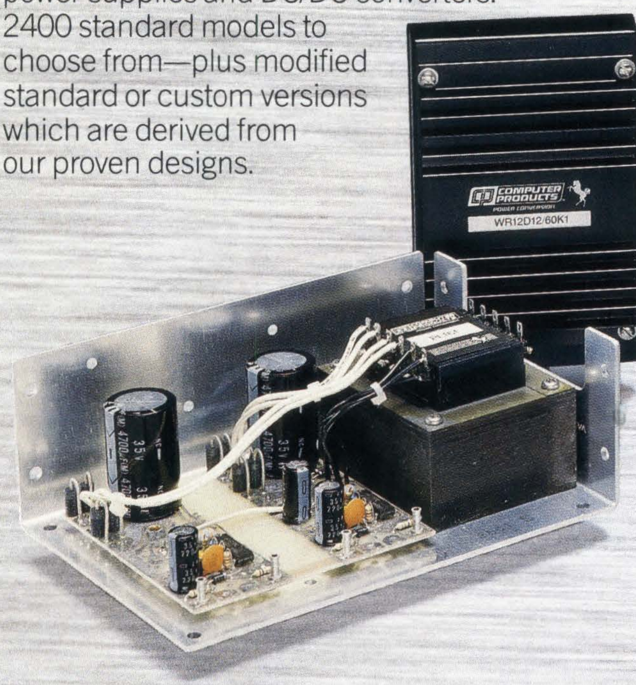

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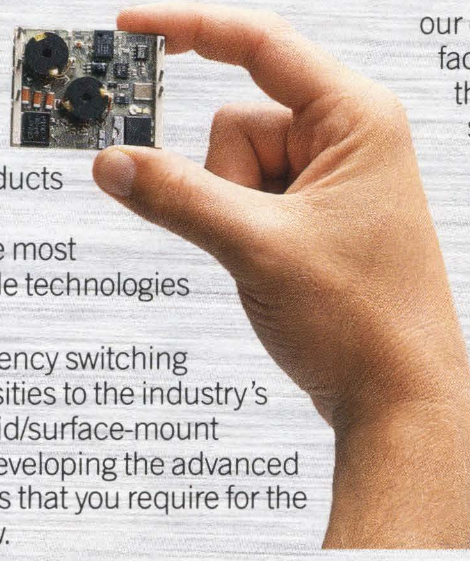

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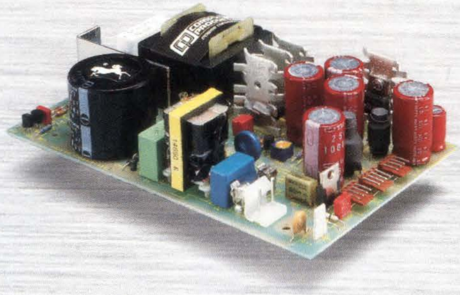

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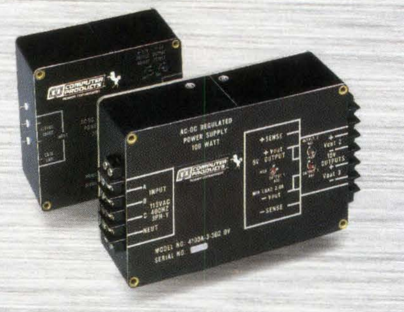

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New software tools run IBM PC software on a variety of 32-bit μPs

Robert H Cushman,
Special Features Editor

Multiple MS-DOS-based programs can run on workstations. *The SoftPC program Insignia Solutions supplies pictorial representations of the IBM PC's monitor that indicate which programs are running. The screen shows Digital Research's GEM (including the calculator), as well as Lotus 1-2-3, Wordstar 2000, Sidekick, and Flight Simulator. Unix uses the window in the lower right corner of the screen to note its operations.*

Most industry observers agree that the vast wealth of MS-DOS-based software is what gives the 8086 μP family such a decided advantage over other μPs. That situation is changing, though: Several software packages now let your MS-DOS-based software run on non-8086-family μPs. (The 8086 family includes the 8088, 80186, 80188, 80286, and 80386 chips.)

By today's reckoning, the value of readily available MS-DOS software is approaching $10 billion. Most of it has been developed as a direct response by third-party software developers to the availability of the 8088-based IBM PC. Thus, most of that software exists as 8088 or 8086 assembly-language instructions, which makes it unusable with other μPs (see **box,** "The IBM PC aberration").

Such a lopsided software situation couldn't go unnoticed, so it's no surprise that enterprising software developers now offer the means for running your MS-DOS-based software on other popular—or promising—μP chips. Three new software packages don't involve the older and more obvious technique of inserting an 8086-based CPU board into a computer. The non-8086 target μP of first choice is probably Motorola's 68020, but there is growing interest in other μPs, particularly those that promise extremely high-speed operation.

Two such software solutions are Phoenix Technologies' Software Co-Processor and Insignia Solutions' SoftPC. These packages simulate the IBM PC's hardware and software configuration within a non-8086-based system. They also translate the 8086 instructions so that the MS-DOS-based program will operate properly. (Although the programs provide simulation as well as instruction-interpretation or -translation functions, you can call them translation programs for simplicity's sake.)

First, you must load the translation software into your target computer, then you can load and run an MS-DOS-based application program. The Phoenix and Insignia programs interpret each 8086 instruction as the target computer fetches it from memory; the software traps and decodes each instruction and remaps I/O and memory operations to suit the target system's configuration. The translation software simulates the IBM PC's resources, which include the MS-DOS code, the basic input-output system (BIOS) code, pertinent I/O devices, and possibly a graphics display. The software cannot simply interpret the MS-DOS-based program instruction by instruction, because the interpretation process would be too slow. Therefore sophisticated programming techniques—some possibly patentable—speed instruction processing.

For example, when the Software Co-Processor sees repetitive program structures, such as loops, it decodes their instructions only once. Thus, the translation software doesn't have to reinterpret the instructions when it encounters the loop again in the MS-DOS software.

As a result, the software requires the target computer to run through only about eight to 10 target μP instructions to interpret each 8086 instruction.

The third software solution is Hunter Systems' XDOS, which is now undergoing final debugging. Rather than interpreting or translating 8086 instructions, the XDOS program converts the 8086's instructions to equivalent instructions for the target μP. Thus, before you run an MS-DOS-based program on your target computer, XDOS performs a binary-to-binary conversion that compiles the 8086 instructions into your target μP's instructions. Industry experts agree that the conversion approach is a very difficult challenge, but because the computer spends no time interpreting instructions as the application program runs, MS-DOS-based application programs should run faster than they would under SoftPC or Software Co-Processor. However, keep in mind that each 8086 instruction compiles into an average of one and a half to two of the target computer's instructions. The compilation doesn't yield a 1-to-1 op-code-to-op-code translation ratio.

32 bits are a must

To be practical, all three software solutions require the processing speeds and memory capacities that today's 32-bit μPs furnish. With anything less than a 32-bit μP in your target computer, execution speeds for converted or interpreted MS-DOS programs will drag when you compare their execution speed to what you'd expect from an IBM PC/XT, PC/AT, or a compatible computer. The translation programs require 32-bit-wide memory simply to hold their simulation software efficiently. For example, Insignia's software needs 3.5M bytes of memory in your target computer system.

Even the XDOS program requires about 100k bytes. Although it converts the 8086 instructions prior to running the program, it still must simulate the IBM PC's MS-DOS configuration for the program's use. Trials show that because XDOS requires a relatively small amount of memory, you can run it on powerful 16-bit μPs, such as Motorola's 68010.

Cost is nominal

Fortunately, the cost of adopting these software techniques isn't high, at least not when compared with the $5000 to $50,000 necessary for a typical 32-bit Unix-based workstation or computer. Likewise, they're less expensive than plug-in boards that simulate the IBM PC's hardware.

The IBM PC aberration

In the ideal 32-bit computer world, there would be no need for software-translation programs. Unix would be the universal standard operating system, and all programs would be written in C so that you could run them on any Unix system. Thus all μPs would only be given a Unix operating system and a C compiler, and they would all be equal from the standpoint of software support.

But today the Intel 80386 μP has an advantage over all other 32-bit μPs, because it enjoys the heritage of what some call the IBM PC aberration. Just as the 16-bit members of the 8086 family gained an overwhelming dominance in the 16-bit arena because of the PC's popularity, so could the 80386 become dominant in the world of 32-bit computers. The basis for the dominance is the 50,000-or-so programs written by third-party software developers for the IBM PC. If you want to view the magnitude of the software-development effect, just look on the shelves in your local software store or in the advertisements in personal-computer magazines. If you are concerned with designing embedded systems, just look at the many varied libraries of specialized MS-DOS-based software for industrial and scientific applications.

Most of these MS-DOS programs were written in 8086 or 8088 assembly language so you can use them only on computers equipped with 8086-family μPs. Typically, when such programs have been written in a high-level language, the supplier will not release the high-level-language source code. That leaves you without an easy conversion route to another μP family.

You can argue that the ideal Unix- and C-based 32-bit world has indeed arrived. There are as many Unix-based personal computers now as any Unix visionary could have ever wished for. But the MS-DOS-software market dwarfs efforts on Unix's behalf. That in itself might not be a problem if it weren't for the third-party software developers who tend to write software for computers with a large market share. The software on the retail shelves bears this out. Buyers follow suit, buying software for the most popular computers.

So, because the software-translation techniques let other μPs share MS-DOS-based software, they may get OEM designers past the IBM PC aberration. Now designers can choose μP hardware based on its own technical merits and suitability for an application while still maintaining compatibility with the MS-DOS software world.

Insignia plans to sell its SoftPC packages through distributors for \$595. The SoftPC package runs on either a SUN-3 or on an Apple MAC-II computer, both of which use the 68020 μP. Hunter Systems and Phoenix plan to work with OEMs, but both say that their packages will cost about the same as Insignia's software. In some cases you won't have to buy the translation software. NCR (Dayton, OH) is considering bundling such programs with its 68020/30-based Tower computer system.

These software-translation packages also have other advantages. For example, when you run MS-DOS-based software on a Unix-based computer system, the MS-DOS software can capitalize on the Unix system's resources. Thus, not only is extensive multitasking possible, but so are multiuser and file-sharing operations. Also, such Unix-based systems are often ahead of the IBM PC when it comes to providing user-friendly mouse and graphics interfaces.

However, the layered Unix software can slow your computer. The interpretive approaches to converting MS-DOS-based software, while fine for single-user computers, may bring multiuser-Unix systems to a halt. Performance depends to a great extent on the target system's μP. **Table 1** provides a preliminary look at the reported and projected performances of these systems in terms of the Dhrystone benchmark. Use the results with much caution. More accurate data will emerge as more users adopt these software-translation techniques.

First, to provide a basis of comparison, **Table 1** lists benchmark values for the 8088, 80286, and 80386 μPs in familiar computers. The original IBM PC and the later PC/XT use 8088s that run at 4.77 MHz. An Intel representative says that the company's benchmark tests yield about 400 to 500 Dhrystones for both computers.

The IBM PC/AT yields a wide range of Dhrystone rates because a wide range of clock speeds is now used in PC/AT and compatible computers. There are two sets of Dhrystone values for the 80386. The first, 6000 to 7000 Dhrystones, results from running 16-bit 8086 code on the 80386. The second set, 9000 to 10,000 Dhrystones, arises when the 80386 runs full 32-bit code. The 80386 can run either type of code directly because the instruction bit patterns are identical. Keep in mind that, when the 80386 runs 8086 code from within the 80386's protected mode, there is an additional 20% or so degradation in performance because the 80386 must trap the 8086's memory and I/O instructions to protect the system.

Table 1 also supplies Dhrystone values for non-8086-family target μPs as they run the Dhrystone program—in both target μP code and in 8086 code that runs through a translation program. The non-8086 μPs fall into two categories: reduced-instruction-set computers (RISCs) and complex-instruction-set computers (CISCs).

When a 68020 (16 MHz) runs an MS-DOS Dhrystone program for an 8086 μP by way of the Phoenix or the Insignia translation method, you reap about the same performance as you would from a PC/XT: 500 Dhrystones. A 68030 (25 MHz)

TABLE 1—ROUGH BENCHMARK COMPARISONS FOR SOFTWARE-TRANSLATION TECHNIQUE

μP	CLOCK FREQUENCY (MHz)	OPERATING SYSTEM	COMPUTER	TRANSLATION TECHNIQUE	8086 CODE (DHRYSTONES)[1]	NATIVE CODE (DHRYSTONES)[1]
8088	4.77	MS-DOS 2.3	PC/XT	NONE	400 TO 500	400 TO 500
80286	6 TO 12	MS-DOS	PC/AT[2]	NONE	1000 TO 2000	1000 TO 2000
80386[3]	20	MS-DOS 3.3	COMPAQ DESKPRO	NONE	6000 TO 7000	9000 TO 10,000
68020 68030	16 25	UNIX	SUN-3	SOFTWARE CO-PROCESSOR SOFTPC	500 TO 2000	6000 TO 8000
68020 68030	16 25	UNIX	SUN-3	XDOS	2000 TO 3000	6000 TO 8000
32532	20 TO 30	UNIX	GENERIC ADD-IN CPU BOARD	SOFTWARE CO-PROCESSOR	1000 TO 4000[4]	9000 TO 16,000
CLIPPER (C-100 AND C-300)	33 TO 50	UNIX V.3	INTERPRO SERIES	SOFTPC	1000 TO 3000[4]	8000 TO 16,000
CLIPPER (C-100 AND C-300)	30 TO 50	UNIX V.3	INTERPRO-200	XDOS	5000 TO 10,000[4]	8000 TO 16,000
MIPS R2000		UMIPS/UNIX	M/1000	SOFTPC	3000 TO 5000[4]	24,000

NOTES:
1. USE BENCHMARKS WITH CAUTION.
2. PC/AT SPEEDS DEPEND ON COMPUTER MODEL AND MANUFACTURER.
3. EXPECT A 20% DEGRADATION WHEN USING THE 80386 IN PROTECTED MODE.
4. TENTATIVE VALUES BASED ON MANUFACTURERS' PROJECTIONS.

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should operate at about 2000 Dhrystones—the performance of today's PC/AT.

Preliminary tests indicate that when the same 68020-based computers use the XDOS translation software, they should reach or exceed PC/AT performance. Typically, a 68020 μP would be running under Unix in a computer such as the SUN-3 workstation.

One of the fastest CISC μP's is National Semiconductor's 32532. The company claims that the device reaches an operating clock frequency of 30 MHz. Based on that clock frequency, Phoenix's Software Co-Processor should run MS-DOS-based software at about twice the speed of a PC/AT. **Table 1** also provides some speculative estimates of performance levels for two RISC μPs: Intergraph's Clipper and MIPS's R2000. The estimates include SoftPC estimates for both RISC μPs and an XDOS estimate for the Clipper. The technical marketing staffs at both Intergraph and MIPS helped prepare the estimates.

Assuming that future performance matches that which the RISC suppliers promise—they talk of reaching 50 MIPS by the early 1990s—it may be that RISC μPs will be attractive for running MS-DOS-based programs that can benefit from high execution speeds. But keep in mind that by definition RISC machines tend to use more instructions than do CISCs. So although they operate faster, they require more instructions. Also, you can assume that Intel will continue expanding the capabilities of its 8086 family. Intel has broadly hinted that the future 80486 μP will offer faster, more RISC-like instructions. Thus, instead of the 80386's average 4.4 clock cycles per instruction, the 80486 may require just two clock cycles.

So, at least, these software-trans-

For more information . . .

For more information on the software packages discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

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Circle No 716

Insignia Solutions Inc
1255 Post St
Suite 625
San Francisco, CA 94109
(415) 885-4455
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Phoenix Technologies Ltd
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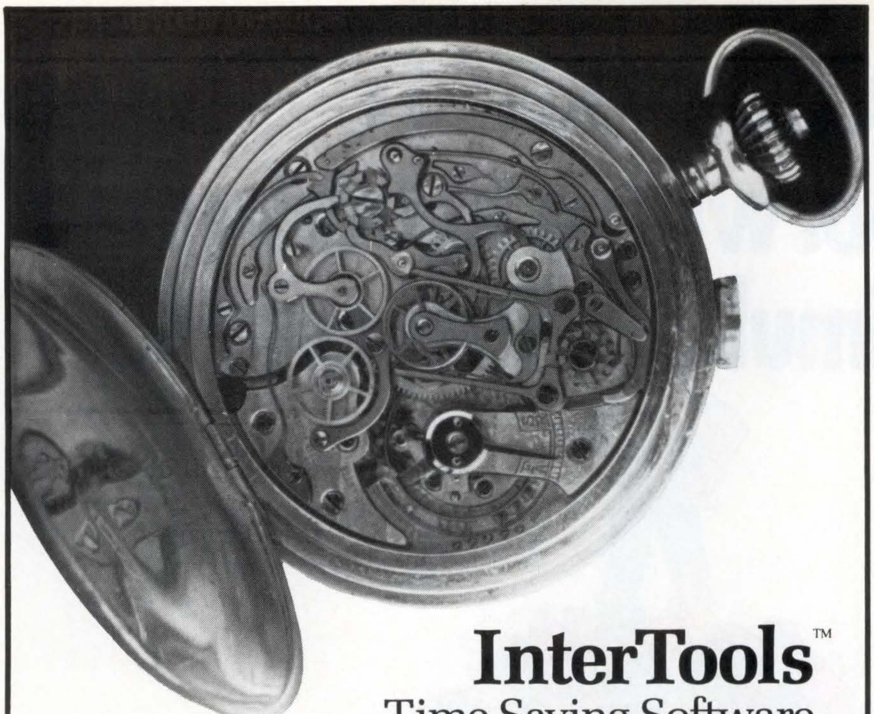

lation techniques will run MS-DOS-based 8086 code on 32-bit computers as fast as it runs on IBM PCs and PC/XTs. At most, the techniques promise to run MS-DOS-based programs much faster than they run on present, or will run on near-future 8086-family μPs. But no one expects these techniques to upset the 8086; as Intel points out, these imitators will always be behind the 8086 family when it comes to software timeliness. After all, the MS-DOS-based software is really meant for use on 1981-vintage hardware, says Intel. What will soon count in the 32-bit computer world is how well the computers run 32-bit software, not how well they run old 16-bit programs.

However, the software-translation techniques can add immediate value to new RISC μPs such as AMD's 29000. New μP-chip manufacturers cannot offer libraries of software products as soon as their chips are available. So, the ability to run existing MS-DOS-based programs can help such chips survive while their supporters build up a repertoire of 32-bit software.

Remember embedded systems

At first glance, these software-translation approaches appear to benefit only desktop workstations and similar large computers. Designers of embedded systems will also find them useful, particularly the XDOS binary-translation approach, because it demands little additional memory. One example is when an OEM designer wants to place a specialized MS-DOS-based program for laboratory-data analysis into an embedded controller as an option for customers. Being able to select an MS-DOS-based program for a non-8086-family computer opens a world of possibilities.

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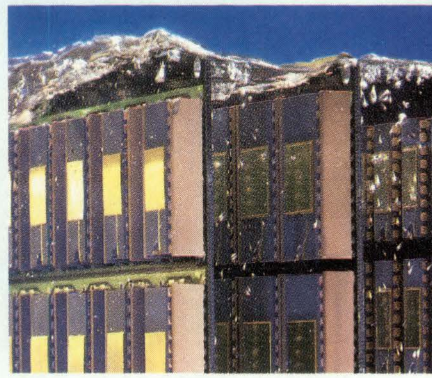

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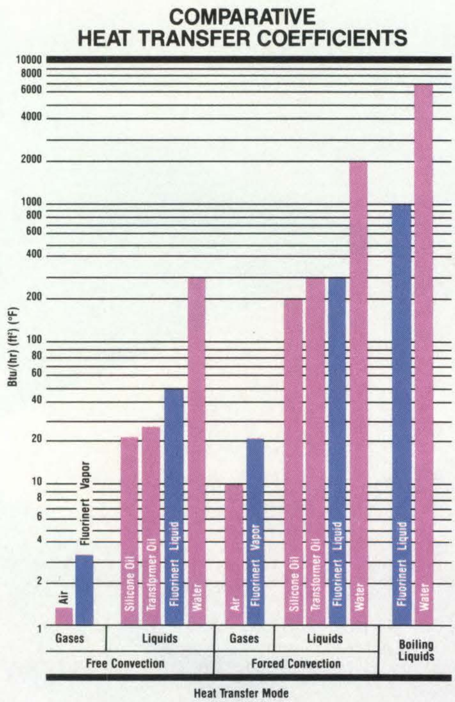

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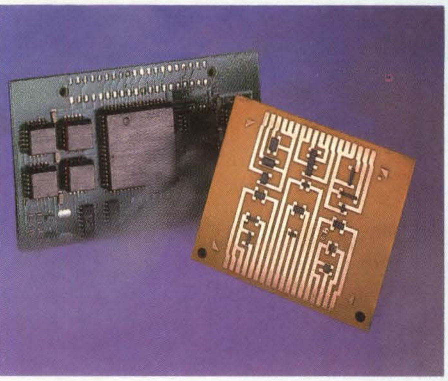

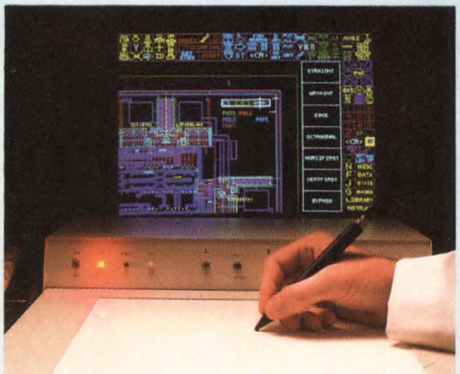

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THERMAL SHOCK TEST CONDITIONS

Military Standard 883-1011			Military Approved Fluorinert Liquids	
Test Condition	**Hot Test Step 1**	**Cold Test Step 2**	**Hot Test Step 1**	**Cold Test Step 2**
A	100°C	− 0°C	Water, FC-40	Water, FC-40, FC-77
B	125°C	− 55°C	FC-40, FC-70, FC-5311	FC-77
C	150°C	− 65°C	FC-40, FC-70, FC-5311	FC-77
D	200°C	− 65°C	FC-70, FC-5311	FC-77
E	150°C	− 195°C	FC-40, FC-70, FC-5311	Liq. N_2
F	200°C	− 195°C	FC-70, FC-5311	Liq. N_2

GROSS LEAK TEST CONDITIONS

	Military Approved Fluorinert Liquids		
Military Standards	**Indicator Fluids**	**Detector Fluids**	**Absorption Fluids**
MIL-STD 883-1014	FC-40, FC-43	FC-72, FC-84	Do not apply
MIL-STD 750-1071	FC-40, FC-43	FC-72, FC-84	FC-43, FC-75, FC-77
MIL-STD 202-112	FC-40, FC-43	FC-72, FC-84	Do not apply

Discover higher yields in vapor phase soldering

Fluorinert Liquids have been the industry's fluid of choice since the vapor phase reflow soldering (VPS) process was introduced in 1975. There are a number of good reasons for this universal acceptance. VPS with Fluorinert Liquids produces highly reliable solder joints. The system reduces reject rates, increases production, and lowers production costs. With Fluorinert Liquids, you can be assured that your products will never be exposed to a temperature higher than the selected liquid's boiling point. (See above)

You'll avoid those problems usually associated with other systems — shadowing, uneven heating, and overheating. The liquids are non-flammable. Their low surface tension helps them evaporate quickly from the work pieces without leaving a residue.

VPS with Fluorinert Liquids is especially suited for boards with high mass or complex geometries. The liquid vapors completely surround the assembly and penetrate remote recesses to heat all surfaces evenly. The vapors are 15 to 20 times heavier than air so they can be contained easily within the work area. The system offers an oxygen-free, non-corrosive environment to minimize rejects from oxidation contamination.

Some typical applications using Fluorinert Liquids in VPS include surface mounted leaded or leadless components, through-hole leads and wire-wrap pins, lead frame attachment, reflow of electroplated solder or tin and miscellaneous metal joining.

VPS SELECTION GUIDE

Fluorinert Liquid	Boiling Point	Typical Solders
FC-43	174°C/345°F	70 Sn/18 Pb/12 In 100 In 58 Sn/42 In 58 Bi/42 Sn
FC-70, FC-5311 FC-5312	215°C/419°F	63 Sn/37 Pb 60 Sn/40 Pb 62 Sn/36 Pb/2 Ag
FC-71	253°C/487°F	100 Sn 95 Sn/5 Ag 60 Pb/40 Sn

Discover the unique cooling benefits of Fluorinert™ Liquids

As the package size decreases, your need for more efficient heat dissipation increases in proportion. 3M Fluorinert Liquids are very efficient as a direct contact heat transfer medium, with the added advantage of having the high dielectric characteristics needed to meet stringent demands of the diversified electronics industry. We offer 11 liquids with boiling points that range from 56°C to 253°C.

These stable liquids allow you to maximize power density and miniaturize your package. Yet they reduce failure rates and increase reliability.

Fluorinert Liquids are used in such demanding applications as:

- Radar transmitters • Power supplies
- High voltage transformers • Lasers
- Radar klystrons • Computer modules
- Computer memories • Fuel cells

Typical properties of Fluorinert Liquids used in cooling are:

Fluorinert Liquid FC-77 (English Units)	Liquid		Vapor
	Room Temp. (77°F)	**Boiling Point (207°F)**	**Boiling Point 207°F @/ATM**
Density lb./ft³	111	100	0.85
Thermal Conductivity Btu/(hr) (ft²) (°F/ft)	0.037	0.033	0.008
Specific Heat Btu/(lb.) (°F)	0.25	0.28	0.23
Viscosity c.p.	1.42	0.46	0.02
Coefficient of Thermal Expansion ft³/(ft³) (°F)	0.0008	0.0009	0.0015

Discover heating/curing with Fluorinert™ Liquids

Because they maintain their vapor temperature with absolute precision, Fluorinert Liquids can be used in many heating and/or curing operations. They serve as heat transfer media in solder mask and polymer thick film applications and for polymer processing. The non-corrosive vapors will not support oxidation. Ideal where solvent flash-off is a problem.

SEE US AT NEPCON-WEST, BOOTH 241

3M

Buscon/88 West offers technical programs, seminars, and presentations galore

All computer-bus users should put Buscon/88 West high on the list of shows and conferences they plan to attend. As in the past, the Buscon program offers training seminars and technical presentations, as well as commercial exhibits. Running from February 22 to 25 at the Disneyland Hotel in Anaheim, CA, Buscon has eight seminars for you to choose from. Four of the seminars run for a full day, but the other four are only a half day each.

One of Monday's full-day seminars is entitled "A technical look at bus structures and applications," and will give you a working knowledge of general bus structures in addition to an overview of today's popular buses and emerging bus technologies for future use.

If you'd rather spend your time taking a closer look at the Nubus, however, then attending "The Nubus; and a special Macintosh II-Nubus workshop" may be a day well spent. The morning portion of the seminar covers technical aspects of the Nubus's architecture. You'll learn about the bus's performance, its processor and architecture orientation, and how the bus supports multiprocessor operations. In the afternoon session, you'll learn about Apple's Mac II computer and how it implements the Nubus's architecture. Seminar leaders will also discuss the market for Mac II-compatible hardware.

For Multibus II users and Multibus II OEMs, another Monday seminar, "Designing with the message-passing coprocessor," will supply information about how to design with and use the chip. During the discussions of message-passing coprocessor applications, the seminar leader will also discuss topics ranging from bus basics to hardware and software development.

However, if you're already firmly in the VME Bus camp, "Choosing and using the new generation of VME Bus interface chips" may be more to your liking. The Monday-afternoon seminar will present the similarities and differences between the VME Bus interface chips that will soon make their debut. In this session, you'll also hear about guidelines that can help you determine which chip approach is best for your application. The seminar will include examples of pc-board designs that include the new VME Bus interface chips.

Another Monday-afternoon seminar will discuss the problems of designing a compatible product for IBM's Micro Channel architecture. Monday's technical seminars wind up with an afternoon session devoted to the VSB—a subset of the VME Bus. The VSB (VME Subsystem Bus) provides an alternative for data-transfer operations between multiple processors in a VME Bus computer system.

The seminar sessions also include two nontechnical programs. Monday's fourth all-day session affords you the chance to learn about selecting a manufacturer's representative, and Tuesday's schedule includes an all-day program devoted to partnership opportunities for US and Japanese companies.

Aside from the seminars, you can also attend technical programs on Tuesday, Wednesday, and Thursday at the Disneyland Hotel. The technical programs offer topics that will interest most bus users. You'll get a choice of hardware and software presentations ranging from interface designs and bus structures to real-time operating systems and multiprocessing applications.

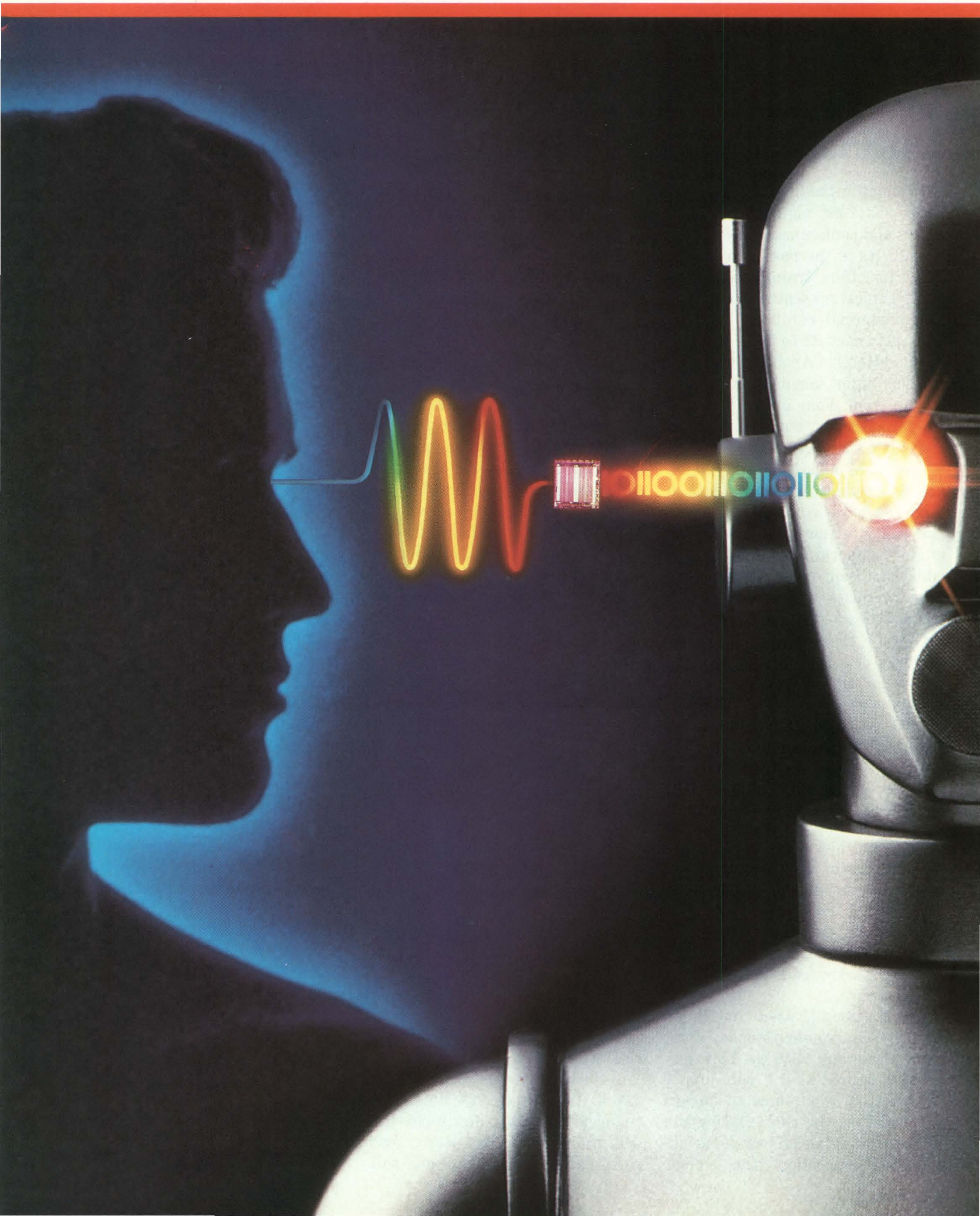
If you'd rather peruse the bus manufacturers' latest hardware and software products, Buscon won't disappoint you. The show has reservations for over 200 booth spaces in the Disneyland Hotel's exhibit area. The exhibits will be open on February 24th between 11 am and 5:30 pm, and also on the 25th between 11 am and 4:30 pm.

As in the past, Buscon's organizers (CMC, Norwalk, CT, (203) 852-0500 or (714) 669-1201) plan a traditional Buscon party on the exhibit floor. Billed as the "all-aboard" industry reception, the get-together starts at 5:30 pm on Wednesday. Attendance is by invitation only, but the Buscon committee has a loose interpretation of what constitutes an invitation. No other show offers such an opportunity to visit with company marketing, sales, and technical people in such a relaxed, informal setting.

At the last Buscon show in the Boston area, the conferences, seminars, and exhibits drew approximately 2000 people. This winter, Buscon's organizers project attendance of at least 3000 participants. The Buscon show is small when you compare it to Wescon, Electro, or Comdex, but there's no better place to meet other bus users and industry experts.—*EDN Staff* **EDN**

Article Interest Quotient
(Circle One)
High 506 Medium 507 Low 508

High-resolution conversion



in the blink of an eye.

Get video speed, low power consumption, high resolution and superior price/performance with our new CMOS data converters.

We've expanded our line to include more CMOS flash ADC's, a charge balancing ADC, an SPI ADC and a DAC. All featuring single 5V supply operation.

We also offer a new high-speed op amp especially well-suited to driving ADC's or video cables.

4, 6 and 8-bit CMOS flash ADC's.

Choose from 4, 6 and 8-bit ADC's. All operate at video speeds, with clocking speed and input bandwidth specified at 5V. What makes these flash ADC's special is silicon-on-sapphire construction, resulting in low cost, high speed, very low input capacitance, low power consumption and inherent latch-up resistance.

10-bit CMOS charge balancing ADC.

This 10-bit successive approximation ADC captures fast moving signals, providing excellent resolution.

It features a built-in fast track and hold, with conversion rates of 150 KHz and an input bandwidth of 1.5 MHz. Even at the maximum rate, power consumption is less than 20 mW.

10-bit CMOS serial ADC.

The CDP68HC68A2 is selectable for either 8- or 10-bit resolution and has an 8-channel multiplexer allowing up to 8 channels of inputs. The device can be used directly with our CDP68HC05C4, C8 or D2 microprocessors or other similar SPI (Serial Peripheral Interface) buses.

8-bit CMOS R-2R video-speed DAC's.

These CMOS/SOS digital-to-analog converters operate from a single 5V supply at video speeds and can produce "rail-to-rail" output swings. Typical update rate is 50 MHz. Settling is fast (20 ns typical) to 1/2 LSB. "Glitch" energy is minimized by segmenting and bar graph decoding of upper 3 bits.

High-speed op amp.

Specially designed for use with data converters, the CA3450 op amp has excellent speed and transmission line driving capabilities.

For 10-bit accuracy, it settles to within 1/2 LSB in 40 ns with a 2V input signal. And it can drive up to four 50 ohm transmission lines.

ADC's	*Res. Bits*	*Conv. Rate Hz*	*Power Diss. (MW)*	*Pkg. Leads*	*1K Price*
CA3304E	4	20M	30	16	2.95
CA3304AE	4	25M	35	16	4.50
CA3306CE	6	10M	65	18	5.50
CA3306E/3306AE	6	15M	70	18	6.25/11.25
CA3318E/3318CE	8	15M	150	24	38.50/24.00
CA3310E/3310AE	10	150K	15	24	6.00/8.00
CDP68HC68A2E	10	10K	15	16	3.75
DAC's					
CA3338E/3338AE	8	50M	100	16	6.00/8.40
OP AMP	*UGBW Hz*	*Slew Rate (X10)*	*I_{OUT} MA*	*Pkg Leads*	*1K Price*
CA3450E	200M	300V/µSec	±75	16	2.70

Data in a flash.

For data sheets of these new products, call toll-free 800-443-7364, extension 19. Or contact your local GE Solid State sales office or distributor.

In Europe, call: Brussels, (2) 246-21-11; Paris, (1) 39-46-57-99; London, 0276-685911; Milano, (2) 82-291; Munich, (89) 63813-0.

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These three leading brands are now one leading-edge company.
Together, we have the resources—and the commitment—
to help you conquer new worlds.

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NEW SMD catalog with easy-to-use selection guide available now. Call (714) 781-5050 or the local office for your FREE COPY!

Surface mount technology has assumed a strategic role in electronics.

To survive in the marketplace, more and more products need the cost savings, space efficiency and high performance of the surface mounted designs you're creating today.

When your circuits call for surface mounted trimming potentiometers and resistor networks, the answer is Bourns. Survival gear.

Customerized Technology: The Bourns Advantage

Bourns—more than any other resistive component manufacturer—has taken surface mount technology and optimized it to your manufacturing processes. We call it "customerized technology" and it means that you can be sure our components will work smoothly with your onsertion equipment; that it will stand up to the new—and hotter—SMD soldering techniques; and, that they will survive vigorous boardwashing. Customerized technology means that before we design our product we even take into consideration how you test the board.

There's No Equivalent

Today you can select from more than 15 styles from Bourns Trimpot including the new 3304, the first 4mm model that's both SMD compatible and automation friendly.

Bourns has also developed an extensive line of surface mount resistor networks. Included in the line are both molded PCC, SOIC, and now SOJ styles in standard JEDEC packages. All in all, nobody serves up SMD technology in so many ways.

Bourns always makes the extra effort. There's no equivalent.

NOW! Anti-Tombstoning Chip Resistors

BOURNS®

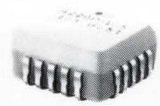
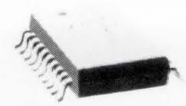
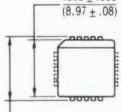
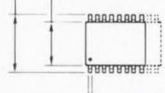
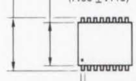
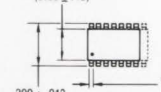
BOURNS TRIMPOT
BOURNS NETWORKS

After 40 years, there's still no equivalent.

Bourns, Inc., 1200 Columbia Avenue, Riverside, California 92507; (714) 781-5050; TLX: 676-423; TWX: 910-332-1252; FAX: 714-781-5700. European Headquarters: Zugerstrasse 74, 6340 Baar, **Switzerland:** 042-333333; TLX: 868722; FAX: 042-319017. **Benelux:** 070-874400; TLX: 32023. **France:** 01-40033604; FAX: 01-40033614. **Germany:** 0711-22930; FAX: 0711-291568. **Ireland:** 021-357001; FAX: 021-357443. **United Kingdom:** 0276-692392; FAX: 0276-691037. Asia Pacific Headquarters: 1401 Citicorp Centre, 14th Floor, 18 Whitfield Road, **Hong Kong:** (852) 5-702171; TLX: 82953 BAPHK HX; FAX: 852-5-664341; CBL: BOURNSASPA HONGKONG. **Singapore:** (65) 339-3331; FAX: (65) 339-1116.

CIRCLE NO 13

Cut along dotted line to remove and save.

BOURNS Resistor Networks	Molded PCC  **MODEL 4200P**	Molded SOL  **MODEL 4400P**	Molded SOL-J  **MODEL 4400J**	SOM  **MODEL 4800P**
Board Space				
Style	Leaded Chip Carrier	Wide Body Gull Wing	Wide Body "J" Lead	Medium Body Gull Wing
Pin Counts	10 and 20	16 and 20	16 and 20	14 and 16
Packaging	Plastic tubes, tape and reel	Plastic tubes, tape and reel	Plastic tubes, tape and reel	Plastic tubes, tape and reel
Standard Resistance Range (Ohms)	10Ω to 1 Megohm	10Ω to 1 Megohm	10Ω to 1 Megohm	10Ω to 1 Megohm
Maximum Operating Voltage	50V	50V	50V	50V
Temperature Coefficient of Resistance	±100ppm/°C ±250ppm/°C for values less than 50Ω	±100ppm/°C ±250ppm/°C for values less than 50Ω	±100ppm/°C ±250ppm/°C for values less than 50Ω	±100ppm/°C ±250ppm/°C for values less than 50Ω
Operating Temperature	−55°C to +125°C	−55°C to +125°C	−55°C to +125°C	−55°C to +125°C
Power Rating	Derate to zero power +70°C to +125°C	Derate to zero power +70°C to +125°C	Derate to zero power +70°C to +125°C	Derate to zero power +70°C to +125°C
Power Dissipation	4210P .... 0.160 watt/resistor 1.50 watts/package 4220P.......0.115 to .160 watt/resistor 2.00 watts/package	4420P......0.115 to .200 watt/resistor 2.0 watts/package 4416P......0.115 to .200 watt/resistor 1.6 watts/package	4420J.....0.115 to .200 watt/resistor 2.0 watts/package 4416J.....0.115 to .200 watt/resistor 1.6 watts/package	4814P.....0.080 to .200 watt/resistor 1.12 watts/package 4816P.....0.080 to .200 watt/resistor 1.28 watts/package
Short Time Overload (ΔR Max.)	±0.25%	±0.25%	±0.25%	±0.25%
Load Life (ΔR Max.)	±1.00%	±1.00%	±1.00%	±1.00%
Mechanical Shock (ΔR Max.)	±0.25%	±0.25%	±0.25%	±0.25%
Moisture Resistance (ΔR Max.)	±0.50%	±0.50%	±0.50%	±0.50%
Resistance to Soldering Heat (ΔR Max.)	±0.25%	±0.25%	±0.25%	±0.25%
Body Materials	Epoxy resin/novolac	Epoxy resin/novolac	Epoxy resin/novolac	Epoxy resin/novolac
Schematics	Isolated, Bussed, Dual Terminators	Isolated, Bussed, Dual Terminators	Isolated, Bussed, Dual Terminators	Isolated, Bussed, Dual Terminators

Bourns, Inc., 1200 Columbia Ave., Riverside, CA 92507; (714) 781-5500; TLX: 676-423; TWX: 910-332-1252; FAX: 714-359-5162

CIRCLE NO 10

BOURNS **Trimming Potentiometers**	4mm Square Sealed Single-Turn  **MODEL 3314**	4mm Square Open Style Single-Turn  **MODEL 3304**	1/4" Square Sealed Multiturn  **MODEL 3269**	.350" Square Sealed Multiturn  **MODEL 3272**
Board Space	.175 (4.45)	.150 (3.8)	.250 (6.35)	.35 (8.89)
Configuration	J-Hook, Gull Wing	Leadless Chip	Gull Wing	Gull Wing
Adjustments	Top	Top	Top, Side	Side
Packaging	Embossed Tape	Embossed Tape	Plastic Tubes	Plastic Tubes (Embossed Tape Optional)
Body Dimensions	.244"x.197"x.100"	.15"x.18"x.094"	.25"x.25"x.28"	.35"x.35"x.20"
Standard Resistance Range (Ohms)	10Ω to 2 Megohms	500Ω to 1 Megohm	10Ω to 1 Megohm	100Ω to 1 Megohm
Resistance Tolerance (Std.)	±20%	±25%	±10%	±10%
Absolute Minimum Resistance (Max.)	1% or 2Ω (whichever is greater)	5%	1% or 1Ω (whichever is greater)	1% or 1Ω (whichever is greater)
Contact Resistance Variation (Max.)	1% or 3Ω (whichever is greater)	5%	3% or 3Ω (whichever is greater)	1% or 3Ω (whichever is greater)
Voltage Adjustability			±0.02%	±0.02%
Resistance Adjustability			±0.05%	±0.05%
Resolution	Infinite	Infinite	Infinite	Infinite
Insulation Resistance	200 vdc. 100 Megohms min.		500 vdc. 1,000 Megohms min.	500 vdc. 1,000 Megohms min.
Effective Travel			12 Turns nominal	12 Turns nominal
Maximum Exposure (Temperature/Time)	215°C/3 minutes 265°C/30 seconds 300°C/3 seconds	265°C/30 seconds	215°C/3 minutes	215°C/3 minutes
Power Rating	300 Volts max. 70°C.....0.25 watt 125°C.......0 watt	50 Volts max. 70°C......0.2 watt	300 Volts max. 85°C.....0.25 watt 150°C.......0 watt	300 Volts max. 85°C.....0.25 watt 150°C.......0 watt
Temperature Range	−55°C to +125°C	−55°C to +125°C	−65°C to +150°C	−65°C to +150°C
Temperature Coefficient	+100ppm/°C	±200ppm/°C nom.	±100ppm/°C max.	±100ppm/°C max.
Seal Test	85°C Fluorinert*		85°C Fluorinert*	85°C Fluorinert*
Mechanical Angle	240° nominal	Continuous	16 Turns nominal	16 Turns nominal
Torque	100G-CM max.	3.0 oz-in. max.	3.0 oz-in. max.	3.0 oz-in. max.
Terminals	Hot solder dipped copper		Solderable pins	Solderable pins
Weight	Approx. 0.01 oz.		0.015 oz.	0.02 oz.

*Fluorinert is a registered trademark of 3M Company.

CIRCLE NO 11

EDN
SURFACE-MOUNT TECHNOLOGY

This Designer's Ready Reference chart provides a check list that you can use when you have completed your electronic design and are ready to pass the design on to a circuit-board engineer. Because there are many decisions you must make before a board can be laid out, you can use this check list to help prepare necessary design information.

DESIGN RULES

Type of design:
- SMT only
- Mixed SMT and through-hole components

Mounting:
- Component-side only
- SMT solder-side only
- Both sides

DESIGN RULES FOR SMT COMPONENTS

CONFIGURATION	SPACING (IN.) TYP	MIN
SOIC (SIDE TO SIDE)	0.100	—
SOIC (END TO END)	—	0.025
SOIC (SIDE TO CHIP)	0.050	—
SOIC (END TO CHIP)	0.050	0.025
PCC TO PCC	0.100	—
PCC TO CHIP	0.050	—
CHIP TO SOT	0.050	0.025
CHIP TO CHIP	0.050	0.025
LAND TO TRACE	0.008	—
TRACE TO TRACE	0.008	—
PAD TO TRACE	0.008	—
TRACE WIDTH INTO LAND	≤0.015	0.008
VIA PAD DIAMETER	0.037	0.025
VIA HOLE DIAMETER	0.020	0.013
PCC SOCKET CLEARANCE	0.200	—
LAND TO SILKSCREEN	—	0.010
TRACE TO BOARD EDGE	0.050	0.025
LAND TO WIDE TRACE	0.025	0.0125
TRACE WIDTH	0.008	—
VIA TO UNRELATED LAND	0.025	0.008

DESIGN RULES FOR MIXED TECHNOLOGY

CONFIGURATION	MIN SPACING (IN.)
CHIP TO AXIAL LEAD	0.075
CHIP TO AXIAL BODY	0.050
SOIC TO DIP	0.100
AXIAL SIDE TO DIP SIDE	0.100
AXIAL END TO DIP END	0.200
DIP END TO DIP END	0.200
DIP SIDE TO DIP SIDE	0.100
SOIC SIDE TO DIP SIDE	0.100
PCC TO DIP SIDE	0.125
PCC TO AXIAL BODY	0.100

DESIGN REQUIREMENTS FOR TEST

All test pads should be accessible from the same side of the board; usually the bottom.
The test pads should be at least 0.035 in. in diameter.
As many of the test pads as possible should be put on 0.100-in. centers.
The minimum space between test pads cannot be less than 0.050 in.
If the board tester supplies power to your circuit through test pins, use at least one test pad for each ampere of power. Thus, 5V at 1A requires one test pad for the power and one for the ground connection.
All interconnect networks should have a test pad.
Determine whether you need access to unconnected or disconnected IC pins for testing purposes.
Test pads must be separated from the component lands.

MANUFACTURING

Identify the types and models of the machines used for pick-and-place operations.
Which solder-reflow method will be used?
- Infrared
- Hand solder
- Laser
- Wave solder
- Vapor phase
- Hot air

Which type of cleaner will you use?
- Aqueous
- Spray
- Solvent
- Manual

Can selected components withstand manufacturing-process stresses?
What is the panel or board size you require?
Can you use a standard board or panel size?
What are the tooling specifications for assembly machines?
What will be the board's orientation?
What are the component orientations?
Are there any autoinsert or autoplace guidelines?
What are the edge clearances for wave soldering and for autoinsertion?

LAYOUT DETAILS

What is the maximum acceptable number of layers?
Do all components have designators and pins assigned to them?
Has the power-and-ground table been completed?
Have the critical-signal paths been identified?
Have the components that dissipate more than 1W been identified?
Where must the power-supply bypass capacitors be placed?

BILL-OF-MATERIAL INFORMATION

Are all designators, part numbers, and quantities included?
- Are capacitor values listed in μF or pF units?
- Are the capacitor's working voltages specified?
- Are the capacitor's tolerances specified?
- Are the capacitor's dielectric materials specified?
- Are all resistor wattages specified?
- Are all resistor tolerances specified?
- Can multiresistor packages be split into individual resistors?
- Are inductor values, tolerances, and voltages specified?
- Are shielded and unshielded inductors clearly marked?
- Are connector specs included?
- Are connector pin assignments clearly identified?
- Are any ICs to be butt mounted?
- Can multidevice ICs be repackaged?
- Are all socket-mounted items clearly identified?
- Are crystals to be grounded?
- Are specifications included for all nonstandard parts?
- Have you included specs for hardware items?

TESTING

What is the minimum space needed between components for testing purposes?
What is the minimum test-pad size?
Are you using single- or double-side testing?
Will you be probing the top or bottom side of the board?
If bareboard testing is required, what is the grid spacing?
What bareboard test fixture will you use?
Is in-circuit testing required?
- If so, what is the grid spacing?
- Will the design use lands or separate pads for test?
- Must you probe disconnected pins on ICs?
- What in-circuit test fixture will be used?

Do you require functional testing?

CIRCUIT-BOARD FABRICATION

How many layers will the board have?
Are there power and ground planes?
What is the board material's thickness; .030 in., .047 in., .062 in., or other?
Is a silkscreen required?
- What size letters are necessary?
- Which board sides will require silkscreen legends?

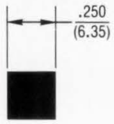
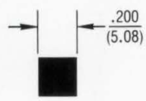
What is the copper-plating process?
- Solder mask over bare copper (smobc)
- Smobc with tin plate
- Solder mask over tin plate

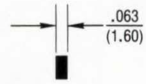
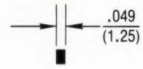
What is the solder-mask process?
- Wet or dry film
- Color mask

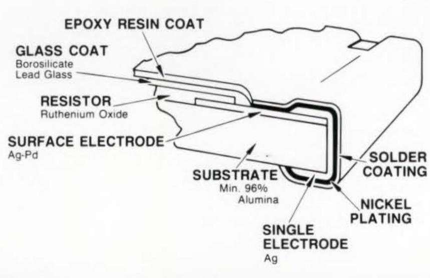
If gold plating is required, what is the plating's thickness?
Is partial gold plating required?

MECHANICAL

What is the board's size?
Are there any irregular cutouts?
Mechanical-drawing information:
- Are edge connectors shown?
- Is a pin-1 designation clearly noted for each connector?
- Are tooling holes located by dimensions or are they located on a panel?
- Is panelization required? If so, what size panel do you need?
- Is palletization required? If so, what size pallet do you need?
- How many tooling holes are required and what are their dimensions (in inches)?

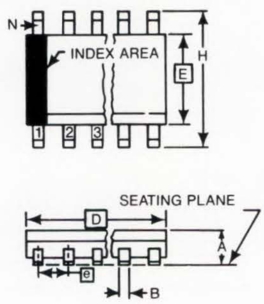
1/4" Square Sealed Single-Turn	5mm Square Sealed Single-Turn
 **MODEL 3325**	 **MODEL 3335**
	
"J" Leads, Gull Wing	"J" Leads, Gull Wing, Through-Hole
Top, Side	Top
Plastic Tubes	Embossed Tape
.35"x.26"x.22"	.20"x.20"x.16"
10Ω to 1 Megohm	10Ω to 500KΩ
±10%	±20%
1% or 2Ω (whichever is greater)	1% or 2Ω (whichever is greater)
1% or 3Ω (whichever is greater)	3% or 3Ω (whichever is greater)
±0.05%	±0.05%
±0.15%	±0.15%
Infinite	Infinite
500 vdc. 1,000 Megohms min.	500 vdc. 1,000 Megohms min.
215°C/3 minutes	215°C/3 minutes
300 Volts max. 85°C......0.5 watt 150°C.......0 watt	100 Volts max. 85°C......0.2 watt 150°C.......0 watt
−55°C to +150°C	−55°C to +150°C
±100ppm/°C max.	±100ppm/°C max.
85°C Fluorinert*	85°C Fluorinert*
260° nominal	270° nominal
3.0 oz-in. max.	3.0 oz-in. max.
Solderable pins	Solderable pins
0.02 oz.	0.02 oz.

BOURNS **Chip Resistors**	1/8 Watt  **MODEL CR1206**	1/10 Watt  **MODEL CR0805**
Board Space		
Resistance Range (Ohms), Tolerance and Temperature Coefficient	100Ω to 1 Megohm ±1%, 100ppm/°C 47Ω to 1 Megohm ±5%, 200ppm/°C 10Ω to 47Ω ±5%, 300ppm/°C	47Ω to 1 Megohm ±5%, ±200ppm°C 10Ω to 47Ω ±5%, ±300ppm/°C
Power Rating	0.125 watt	0.100 watt
Maximum Operating Voltage (at 70°C)	200 Volts	100 Volts
Maximum Ambient Temperature	125°C	125°C
Temperature Range	−55°C to +125°C	−55°C to +125°C
Thermal Shock (Method)	±0.5% (MIL-R-55342, Para. 4.7.3)	
Low Temperature Operation (Method)	±0.5% (MIL-R-55342, Para. 4.7.4/IS-30 Para. 3.6)	
Short Term Overload (Method)	±0.5% (MIL-R-55342 Para. 4.7.5/IS-30 Para. 3.7)	
High Temperature Exposure (Method)	±0.5% (MIL-R-55342 Para. 4.7.6/IS-30 Para. 3.8)	
Body Materials		



EDN SURFACE-MOUNT TECHNOLOGY
JEDEC PACKAGE SHAPES AND DIMENSIONS

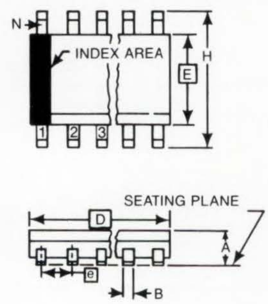
SMALL OUTLINE (SO)—0.50 IN. WIDE



SYMBOL	DIMENSIONS (IN.) MIN	MAX
A	0.532	0.0688
B	0.0138	0.0192
E	0.1497	0.1574
e	0.050	0.050
H	0.2284	0.2440

NO OF PINS	D LENGTH (IN.) MIN	MAX
8	0.1890	0.1968
14	0.3367	0.3444
16	0.3859	0.3937

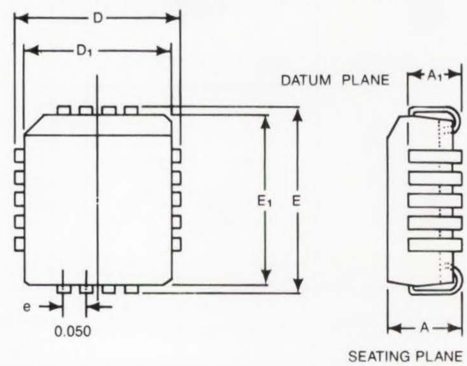
SMALL OUTLINE (SO)—0.300 IN. WIDE



SYMBOL	DIMENSIONS (IN.) MIN	MAX
A	0.0926	0.1043
B	0.0138	0.0192
E	0.2914	0.2992
e	0.050	0.050
H	0.394	0.419

NO OF PINS	D LENGTH (IN.) MIN	MAX
16	0.3977	0.4133
18	0.4469	0.4625
20	0.4961	0.5118
24	0.5985	0.6141
28	0.6969	0.7125

PLASTIC CHIP CARRIER (PCC), RECTANGULAR

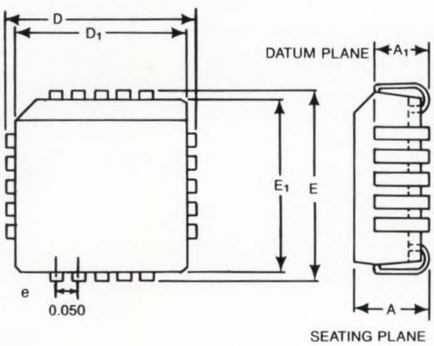


PACKAGE DIMENSIONS

SYMBOL	18 PINS MIN	18 PINS MAX	18 PINS MIN	18 PINS MAX	22 PINS MIN	22 PINS MAX	28 PINS MIN	28 PINS MAX	32 PINS MIN	32 PINS MAX
A	0.100	0.140	0.100	0.140	0.100	0.140	0.100	0.140	0.100	0.140
D	0.317	0.327	0.320	0.335	0.320	0.335	0.385	0.395	0.485	0.495
D_1	0.282	0.288	0.287	0.293	0.283	0.293	0.347	0.353	0.447	0.453
E	0.457	0.467	0.520	0.535	0.520	0.535	0.585	0.595	0.585	0.595
E_1	0.422	0.428	0.487	0.493	0.487	0.493	0.547	0.553	0.547	0.553

NOTE:
ALL DIMENSIONS ARE GIVEN IN INCHES.

PLASTIC CHIP CARRIER (PCC), SQUARE



PACKAGE DIMENSIONS

SYMBOL	20 PINS MIN	20 PINS MAX	28 PINS MIN	28 PINS MAX	44 PINS MIN	44 PINS MAX	52 PINS MIN	52 PINS MAX	68 PINS MIN	68 PINS MAX	84 PINS MIN	84 PINS MAX	100 PINS MIN	100 PINS MAX	124 PINS MIN	124 PINS MAX
A	0.165	0.180	0.165	0.180	0.165	0.180	0.165	0.200	0.165	0.200	0.165	0.200	0.165	0.200	0.165	0.200
D AND E	0.385	0.395	0.485	0.495	0.685	0.695	0.785	0.795	0.985	0.995	1.185	1.195	1.385	1.395	1.685	1.695
D_1 AND E_1	0.350	0.356	0.450	0.456	0.650	0.656	0.750	0.756	0.950	0.958	1.150	1.158	1.350	1.358	1.650	1.658

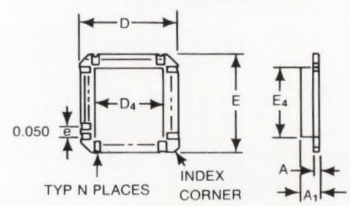
NOTE:
ALL DIMENSIONS ARE GIVEN IN INCHES.

PACKAGE DIMENSIONS

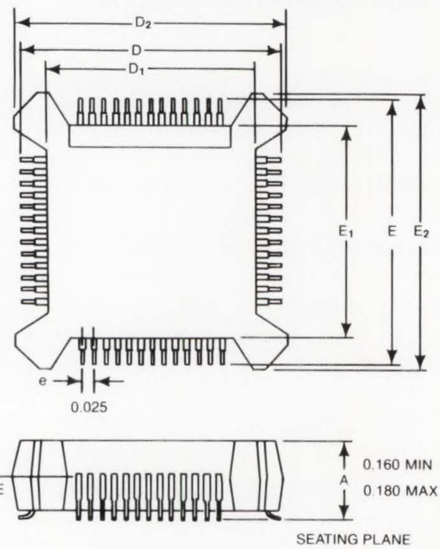
SYMBOL	16 PINS MIN	16 PINS MAX	20 PINS MIN	20 PINS MAX	28 PINS MIN	28 PINS MAX	44 PINS MIN	44 PINS MAX	52 PINS MIN	52 PINS MAX	68 PINS MIN	68 PINS MAX	84 PINS MIN	84 PINS MAX	24 PINS MIN	24 PINS MAX
A	0.017	0.088	0.017	0.088	0.017	0.088	0.037	0.088	0.037	0.088	0.037	0.088	0.037	0.088	0.017	0.088
A_1	0.064	0.100	0.064	0.100	0.064	0.100	0.069	0.120	0.082	0.120	0.082	0.120	0.082	0.120	0.064	0.100
D AND E	0.292	0.308	0.342	0.358	0.442	0.458	0.640	0.660	0.739	0.761	0.938	0.962	1.135	1.165	0.395	0.410
D_4 AND E_4	0.257	0.308	0.307	0.358	0.406	0.458	0.495	0.560	0.495	0.560	0.495	0.862	0.495	1.065	0.352	0.408

NOTE:
ALL DIMENSIONS ARE GIVEN IN INCHES

LEADLESS CHIP CARRIER (LCC)



PLASTIC QUAD FLAT PACK (PQFP)



PACKAGE DIMENSIONS

SYMBOL	52 PINS MIN	52 PINS MAX	68 PINS MIN	68 PINS MAX	84 PINS MIN	84 PINS MAX	100 PINS MIN	100 PINS MAX	132 PINS MIN	132 PINS MAX	164 PINS MIN	164 PINS MAX	196 PINS MIN	196 PINS MAX	244 PINS MIN	244 PINS MAX
D AND E	0.575	0.585	0.675	0.685	0.775	0.785	0.875	0.885	1.075	1.085	1.275	1.285	1.475	1.485	1.775	1.785
D_1 AND E_1	0.447	0.453	0.547	0.553	0.647	0.653	0.747	0.753	0.947	0.953	1.147	1.153	1.347	1.353	1.647	1.653
D_2 AND E_2	0.597	0.603	0.697	0.703	0.797	0.803	0.897	0.903	1.097	1.103	1.297	1.303	1.497	1.503	1.797	1.803

NOTE:
ALL DIMENSIONS ARE GIVEN IN INCHES.

ADVERTORIAL

Multibus I Architecture Supports 32-Bit Transfers

32-bit transfers across the Multibus*I Architecture with a 256Mbytes physical address space, (increased from 16Mbytes), and a 20Mbyte bandwidth within the IEEE 796 specification. "TRU-32" © defines the reserve lines in the P-2 backplane, giving a full 32-bit data width to all 23 slots in the Multibus I specification. As faster, more powerful CPU designs emerge, the costs for todays newer technology in open-architecture buses have sky-rocketed. Migration reluctance from embedded, well established buses is understandable when faced with the reality of: costly hardware changes, timely software learning curves, and off-the-shelf incompatibility among the new buses. This new scheme will benefit those who develop, design or manufacture around the best supported and well defined open-architecture in the world.

CIRCLE NO 129

80386 SBC Executes "Tru-32" Specifications

The ZENDEX ZX-386 single-board computer incorporates the "TRU-32" specification with downward compatibility to all 16-bit and 8-bit Multibus I boards. A full function 32-bit SBC, the ZX-386 can be used in present Multibus I systems executing standard 16-bit data width or Zendex will make available the "P-32" backplane, (4 to 23 slots), supporting the TRU-32 specification for 32-bit applications. The board features a 16MHz 80386 processor; 80387 numeric coprocessor; 82380 DMA controller; 8Mbytes dual ported one wait state DRAM; 4 EPROM sockets; two serial ports; 4Mbyte per second SCSI interface; and two SBX connectors. "TRU-32 Development Kits" are available and include Interface scheme, PAL equations, and license for $100.00. ZENDEX CORPORATION (415) 828-3000

CIRCLE NO 130

Intelligent Multibus I Extender Board

A most useful tool to assist test technicians and engineers in trouble shooting Multibus I products has been designed and released by Zendex Corporation. The ZX-611 has sixteen LED's displaying buffered bus functions for 16-bit, 8-bit and the new 32-bit Multibus I specification. Two on board switches control: 1) systems reset and 2) local power for insertion and extraction of boards in extension without removing system power. Support arms relieve connector pressure and contact problems inherent to the weight of bus boards on extension. In addition, terminal pins for +5v and ground are mounted on the board for oscilloscope and probe attachment along with plated thru holes on P1 for user selective test points. ZENDEX CORPORATION (415) 828-3000

CIRCLE NO 131

Modular I/O Flexibility Through SBX

As the ever increasing need for modular I/O intensifies a broad range of SBX Expansion Modules for the SBX specification have been developed. Expanding virtually any system with standard or custom designs, ZENDEX CORPORATION manufactures the largest selection of modules available. SCSI, Cmos SCSI, IEEE 488, HDLC, Modem, Servo controller, Stepper Motor controller, Encoder, Clock/Calendar, Disk controller, Dual Serial, A/D D/A Converter, and more. The ZENDEX ZX-564 mother board supports 6 SBX modules simultaneously, 8/16 bit transfers, 4 channels of DMA with user definable applications such as: Multiple Serial I/O, Industrial Control, Data Acquisition, and many more. ZENDEX CORPORATION (415) 828-3000

CIRCLE NO 132

CIRCLE NO 133

Launch your design with a 40MHz FIFO that can be accessed in 15ns.

Make waves with your design. Launch it with the MK4505 BiPORT™ FIFO from SGS-THOMSON Microelectronics, the Winning Team.

At 15ns, the MK4505 is one of the fastest single-chip FIFOs in the world.

The MK 4505 enables you to go full speed ahead now—without extra registers, extra buffers or extra costs.

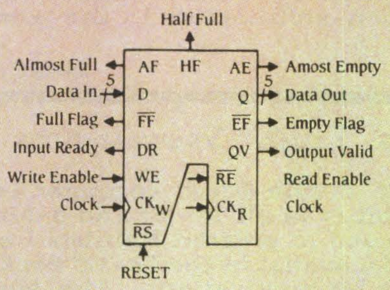
Our FIFO's blazing 15ns access speed and 25ns cycle time come from a unique combination of advancements including: 1.2μ full-CMOS technology, an eight-transistor BiPORT™ memory cell and 1K x 5 pipelined architecture.

Separate rising edge-triggered read and write clocks assure transfer of data between two totally asynchronous systems.

A full complement of status flags lets you know how much is—or isn't—available, before it's too late.

	MK4505-25
Cycle time	40 MHz
Access time	15ns
Almost full & Almost empty status flags	Yes
Free-running clock inputs	Yes
Separate read & write enable inputs	Yes
Depth	1024
Width	5-bit
Width & depth expandable with no support logic	Yes
Fully authorized second sourcing	Yes

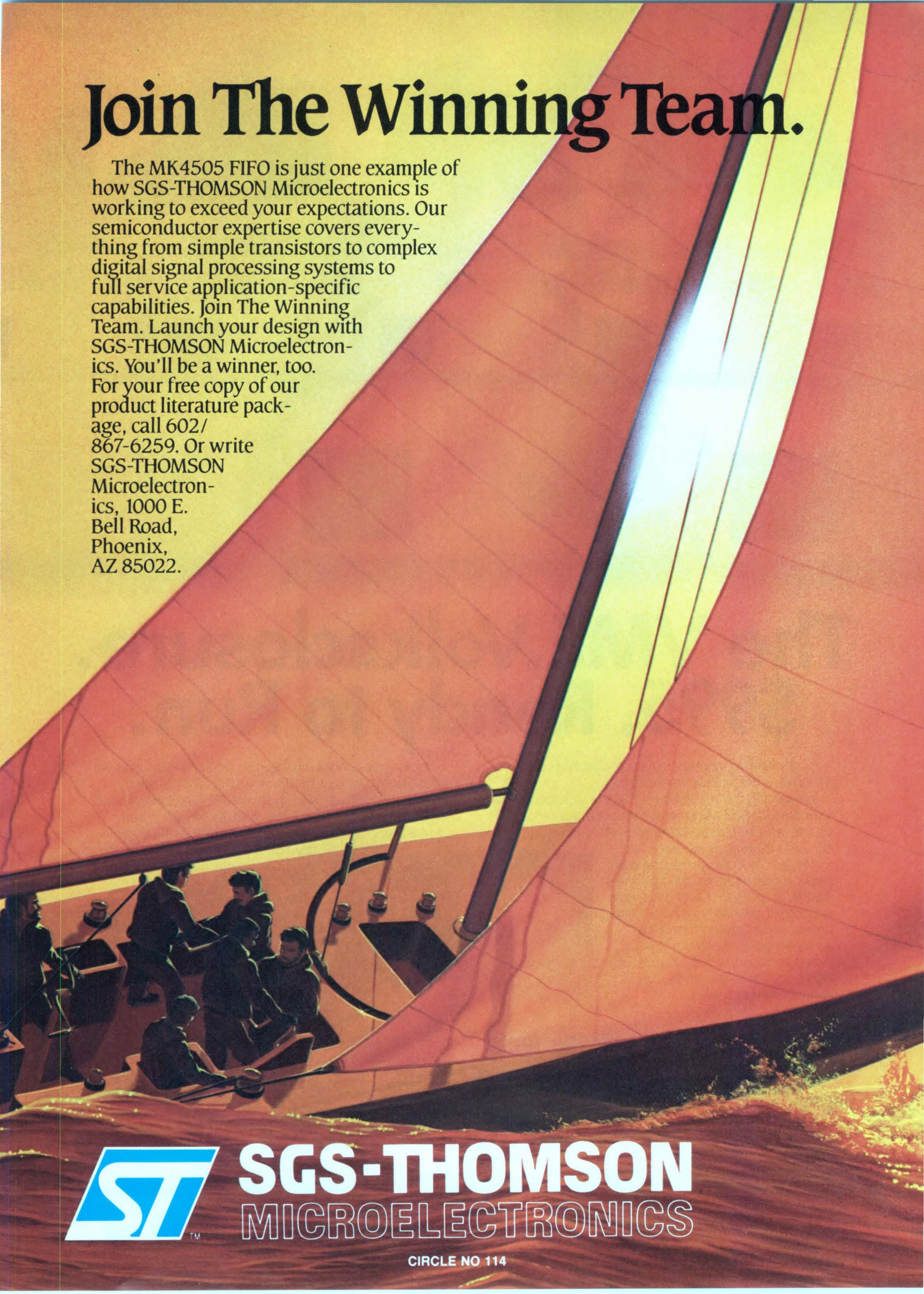
Unrivalled speed and performance capabilities, coupled with ultrathin 300 mil DIP packaging make the MK4505 BiPORT FIFO the logical design-in choice for applications like digitized video and audio, image processing, high performance graphics, microwave and FDDI, RADAR return sampling and cache write buffering.



Two models are available: a Master (MK4505M) and a Slave (MK4505S). The MK4505M gives you all the control signals necessary for reliable, full speed width and/or depth expansion without adding extra logic.

Get your design right on course, right from the start with the MK4505, just one member of our complete family of FIFOs. Join the Winning Team—SGS-THOMSON Microelectronics.

Call or write for more information: 1000 E. Bell Road, Phoenix, Arizona 85022. 602/867-6259.


Join The Winning Team.
The MK4505 FIFO is just one example of how SGS-THOMSON Microelectronics is working to exceed your expectations. Our semiconductor expertise covers everything from simple transistors to complex digital signal processing systems to full service application-specific capabilities. Join The Winning Team. Launch your design with SGS-THOMSON Microelectronics. You'll be a winner, too. For your free copy of our product literature package, call 602/867-6259. Or write SGS-THOMSON Microelectronics, 1000 E. Bell Road, Phoenix, AZ 85022.
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CIRCLE NO 114

The VME Volksclosure. $995. Ready to Run.

Finally. The economies of mass production catch up with VME and Multibus II enclosures.

Introducing the Volksclosure, Electronic Solutions' economy model enclosure with turbo performance. All you do is add cards and peripherals for a complete, attractive desktop computer.

With the Volksclosure (also known as our Model One) everything comes standard: six VME or Multibus II slots, space for three half-height 5¼″ disk drives, and a high-performance six-layer backplane all in a highly tooled enclosure with our handsome front panel that hides those ugly connectors and cables.

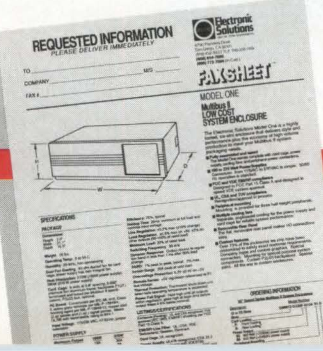
You do get a choice between two multiple-output power supplies: 190 Watts with 19A at +5V or 270 Watts with 30A at +5V. You can also choose a J2 backplane for VME extended addressing or iLBX II for a Multibus II system.

Most important, while the Volksclosure costs less, you don't get less. It fully reflects Electronic Solutions' commitment to quality and performance. For example, it meets UL and CSA safety standards and FCC Class A EMI/RFI specs to the letter.

THREE YEAR 3 LIMITED WARRANTY

The New Volksclosure. How to get a lot more mileage from your packaging budget. Call right now for complete details.

We'll FAX you the facts



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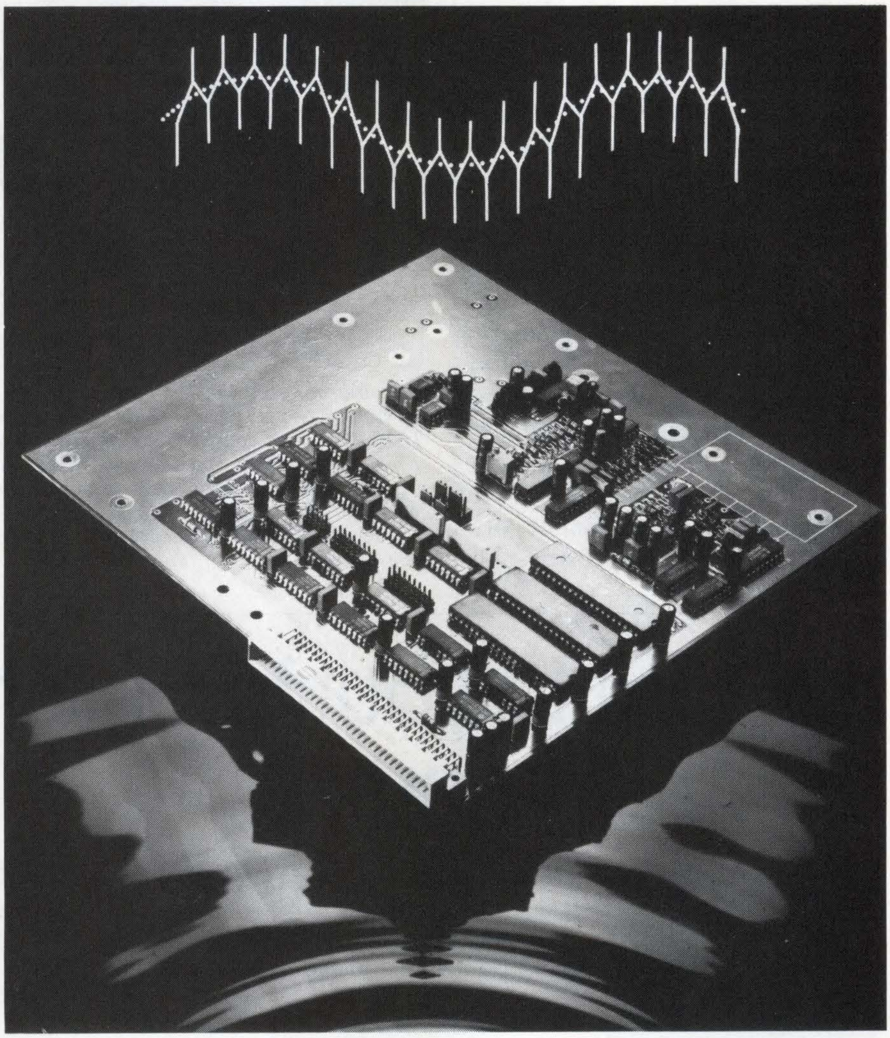
CIRCLE NO 178

Ripple-and-noise test module uses voltage-comparison technique

This ripple-and-noise test module, intended for use in testing switching-regulated power supplies, plugs into the vendor's 6500 modular automatic power-supply test system. The difficulty of reproducing switching-supply ripple-and-noise measurements has caused friction between power-supply vendors and their customers. The manufacturer claims to have solved that problem by replacing more conventional noise-measurement techniques with a method based on voltage-level and duty-factor sensing.

Peak-to-peak measurements of switching-supply noise are notoriously difficult to reproduce because of their extraordinary sensitivity to the bandwidth of the measurement instrumentation's peak-detection circuits. To overcome this problem and to pinpoint whether noise is associated with a supply's switching action or its conversion of line-frequency ac to dc, a common noise-measurement technique uses filters to separate switching-frequency noise from line-frequency-related ripple, and it uses an rms-to-dc converter to measure the filters' output. (A lowpass filter allows you to measure line-related noise components; a highpass filter passes the switching-frequency-related components.)



This power-supply ripple-and-noise test module *achieves improved measurement repeatability by using an unusual A/D-conversion technique in place of the more common filtering and rms-to-dc conversion methods.*

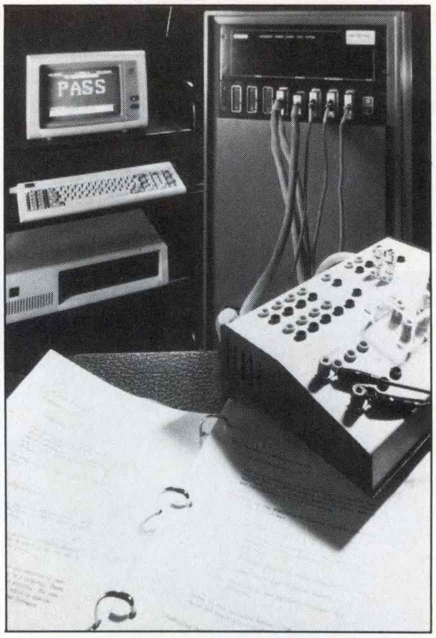
Because the supply's switching frequency is hundreds of times as high as the line frequency, it may seem as though you don't need filters with an especially sharp cutoff. However, only about 5½ octaves separate the seventh harmonic of the 60-Hz power line from the most common switching-regulator frequency, 20 kHz. If, for example, you use a single-pole lowpass filter to eliminate switching-frequency voltages, you'll find that a filter that attenuates by only a little more than 33 dB (that is, <50×) at 20 kHz still produces a greater-than-desired 3 dB of attenuation of voltages at the seventh line-frequency harmonic.

If you attempt to improve the rejection of switching-frequency noise by lowering the filter's cutoff frequency, you further attenuate ripple components at harmonics of the line frequency. If, instead, you increase the sharpness of the filter's cutoff characteristic, you can introduce peaks into the filter's passband response, which, even with careful selection of the cutoff frequency, may affect measurements of line-frequency-related ripple. At the very least, you'll probably find it tricky to design filters that yield measurements someone else can reproduce.

Although it appears that the

trend toward higher switching-regulator operating frequencies will make it easier to obtain accurate ripple-and-noise measurements by using conventional techniques, remember that power-supply switching-noise waveforms contain a significant amount of energy at harmonics of the switching frequency higher than the 33rd. Slew-rate and bandwidth limitations in most rms-to-dc converters cause errors in measuring waveforms with such high-frequency components, and these errors worsen as the switching frequency increases.

The manufacturer's test module makes reproducible ripple-and-noise measurements by eliminating filters and rms-to-dc converters entirely. The module, which achieves a 30-MHz bandwidth, uses an unusual A/D-conversion technique and takes advantage of the fact that the switching-spike component of a power supply's ripple-and-noise waveform normally has a low duty factor. The module adjusts a voltage comparator's reference input signal until its value is less than the ripple and noise under examination for a programmable, and normally small, fraction of the total time. By adjusting the fraction until the reference-signal value begins to increase rapidly, you determine the noise-pulse duty factor. The module then reports the value of the reference signal—a value proportional to the ripple component of the ripple and noise. A 3-channel module costs \$3800; a 7-channel module sells for \$4500. Prices for the 6500 system range from \$30,000 to \$500,000; most configurations cost less than \$100,000.—***Dan Strassberg***



You can configure the 6500 automatic power-supply test system *in many ways. An IBM PC/XT or compatible computer is a popular controller. You can choose voltage sources, dynamic loads, and measurement modules of several types. A 16-slot backplane allows you to match system capabilities to your needs.*

Intepro Systems Inc, 450 Bedford St, Lexington, MA 02173. Phone (617) 863-9500. TLX 510-601-8053.

Circle No 720

Z I L O G

Z280

The highest performance and highest integration, ever. Together on a single 16-bit chip.

The Z280™ gives you a more powerful CPU and higher performance peripherals than you've ever seen on a 16-bit chip. Think of it as a complete microsystem on a chip.

Unmatched performance...

Start with the most powerful 16-bit engine available, add on-board Cache, MMU and Burst Mode memory support — and you'll begin to understand the Z280's power and potential.

...powerful on-board peripherals...

Imagine the savings in cost and board size when you have peripherals like 4 DMA channels that'll give you transfers at 6.6 Mbytes/sec, and a full-duplex UART.

...and the glue to tie it all together.

With a DRAM Controller to support up to 1 MBit DRAMs and Programmable Wait State Logic — on board — you're really looking at significant glue reduction.

	Z280™	80186	68070
Package	68-pin PLCC/CMOS	68-pin LCC/NMOS	84-pin PLCC/CHMOS
Typical Power	375 mW	2 W	800 mW (est)
Speed	10-25 MHz	8-12.5 MHz	10 MHz
Memory Support	16 Mb Physical Paged	1 Mb Physical Segmented	16 Mb Physical 8 or 128 Segments
16-bit Registers	12 General	8 General	15 Dedicated
Instruction Pre-fetch	256-Byte Assoc. Cache; Burst Mode	6-Byte Queue	None
Multiprocessor Support	Local or Global	Local only	Local only
Wait Logic	Programmable	Programmable	Hardwire
DMA	4 Channels, 6.6 Mb/s @ 10 MHz	2 Channels 2 Mb/s @ 8 MHz	2 Channels, 3.2 Mb/s @ 10 MHz
Counter/Timers	3 16-bit	3 16-bit	2 16-bit
Serial I/O	1 Full-Duplex UART	None	1 Full-Duplex UART
DRAM Controller	10-bit Refresh	None	None
Price (100)	$33	$43	$50

The choice is clear.

Z280: Truly a microsystem.

The Z280 gives you a lot more performance. In a lot less board space. All off the shelf and backed by Zilog's proven quality and reliability. Plus, it's binary code-compatible with the Z80,® and priced to rival 8-bit chips. And all the development support tools you need are available from industry leaders. Contact your local Zilog sales office or your authorized distributor today. Seeing is believing. Zilog, Inc., 210 Hacienda Ave., Campbell, CA 95008 (408) 370-8000.

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CIRCLE NO 179

Systems DMM lets you choose 8½-digit resolution or 100,000 readings/sec

Designed to be at home in a reference lab, on an engineer's bench, or in a test-equipment rack, the $5900 Model 3458A digital multimeter offers a range of measurement speeds and resolutions that allow the instrument to tackle a wide variety of jobs. At its highest resolution, the DMM provides 8½-digit measurements; at its fastest speed, the multimeter takes 100,000 readings/sec. In addition, a precise timebase and a switchable, high-speed, track-and-hold input path allow the instrument to digitize repetitive waveforms to 15 MHz.

For situations requiring high-throughput measurement, the DMM can take 100,000 readings/sec with 4½ digits of resolution. The instrument's standard acquisition memory holds 10,000 readings, and a $500 option adds storage capacity for an additional 64,000 readings. To allow for additional storage capacity or for data analysis, the multimeter can pump readings out through an IEEE-488 port to a computer at the full 100,000-reading/sec rate. The company supplies a $1000 control-and-analysis software package for the DMM; the package runs on the vendor's Model 9000 workstations.

For applications that don't require the DMM's full measurement speed but that could make use of additional resolution, the instrument can take 50,000 5½-digit, 5000 6½-digit, or 60 7½-digit readings/sec. It performs 5 readings/sec when set to its maximum resolution of 8½ digits.

The instrument's internal input path incorporates an integrator with a 160-kHz bandwidth. You can digitize repetitive signals with frequencies to 15 MHz by switching the input path to a track-and-hold

You can choose to take 100,000 4½-digit measurements/sec or five 8½-digit measurements/sec with the Model 3485A DMM.

circuit and using the DMM's subsampling feature. The subsampling measurement technique takes a series of samples, one per cycle of the signal it's measuring. Following a trigger event that occurs once each cycle, the DMM waits longer (the increment is programmable) than it did during the previous cycle and then takes a sample. Over several cycles, the instrument builds a detailed picture of the signal's waveform. The DMM's sampling clock can operate at frequencies as high as 100 MHz, and it features less than 100 psec of jitter.

Automated test systems can readily use the DMM's flexible tradeoff between resolution and speed. The company claims that digital multimeters in automated test systems perform a large percentage of the measurements, so a faster DMM in such a test system will probably greatly improve overall system throughput. In addition to the ability to take measurements quickly, the 3458A multimeter can perform as many as 200 function or range changes/sec and can take 250 autoranged measurements/sec.

To aid in making rapid range and function changes in a test environment, a program memory in the instrument stores measurement sequences that can be activated by the transfer of only a few bytes over the IEEE-488 interface. This program memory allows the DMM to make as many as 1000 limit checks/sec. You can calibrate the multimeter from its front panel (so it can remain in its system rack) with just two references—a 10-kΩ resistor and a 10V reference source—and a short circuit.

The company, which incorporated its proprietary multimeter language (HPML, also used in its earlier 3457A DMM) in the instrument, asserts that its future DMMs will also

UPDATE

support this language to ease future software changes. You can issue all of the HPML commands from the DMM's front panel as well as enter them through the instrument's IEEE-488 port.

The multimeter's accuracy specifications make it well suited for work in a reference laboratory. The company rates the instrument's dc-voltage accuracy at 0.5 ppm over 24 hours and 8 ppm over one year. An $800 high-stability option improves that annual accuracy rating to 4 ppm. The linearity spec is 0.1 ppm over 24 hours and has been measured as being within 0.05 ppm of 10V against the Josephson-Junction Array voltage standard developed by the National Bureau of Standards in Boulder, CO. You can command the DMM to perform an automatic calibration against its internal reference standards, which have known drift and temperature coefficients.

Because the DMM can measure both ac and dc voltage and current, resistance, frequency, and period, it's likely to find a home on the test benches of engineers who need a high-precision, full-featured multimeter. Its dc-voltage measurements include five ranges from 0.1 to 1000V with a maximum sensitivity of 10 nV, and its resistance ranges can measure impedances from 10Ω to 1 GΩ (full scale) with 2-ppm accuracy. The ac-voltage scales, frequency counter, and period measurement accommodate signals with frequencies of 1 Hz to 10 MHz. The 3458A is available eight weeks ARO. A $160 option extends the instrument's warranty period from one year to three years.

— Steven H Leibson

Hewlett-Packard Co, 3495 Deer Creek Rd, Palo Alto, CA 94304. Phone local office.

A FIRST FROM TEKTRONIX

TURN BACK THE CLOCK ON MICROPROCESSOR PROBLEMS!

Now see what your hardware and software are really doing, in real time, without waiting for problems to repeat. Nothing else comes close to tools like these in Tek's DAS9200 Digital Analysis System:

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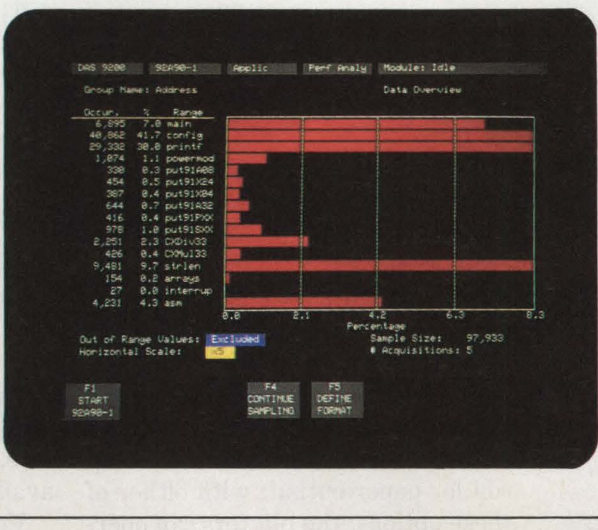

Monitor and integrate up to six 8-, 16- or 32-bit micros at once! That's just one of many other ways the DAS9200 helps you beat the clock in system design. To learn more, contact your local Tek representative. Or call:

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Electrostatic plotters produce prints at 1 ips

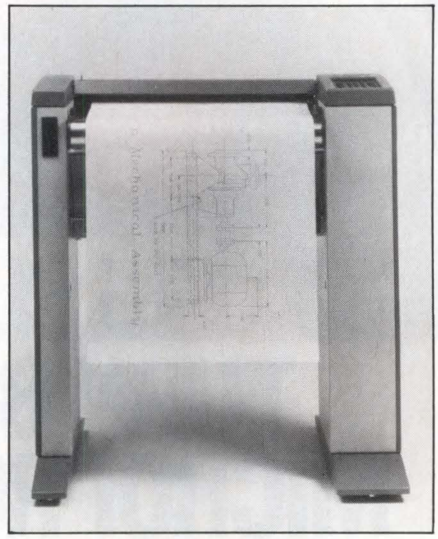
Electrostatic raster-printing technology gives the 8500 Series monochrome plotters a plotting speed of 1-ips. You can use the 24- and 36-in.-wide plotters as a department or network resource because of their fast output speed. Yet the devices are priced in the $20,000 range, so they're affordable for use with a single workstation or personal computer.

Electrostatic plotters use a linear array of wire nibs to place images on the medium. The wire nibs selectively conduct an electrical charge that discharges dots on the dielectric surface of the coated medium. The medium then passes through a toner bath, and toner particles are fused to the selected charged dots forming the image. The wire nibs of the 8500 Series plotters produce a resolution of 200 dots/in.

Although electrostatic plotters are raster devices, the 8500 Series includes a controller that performs a vector-to-raster conversion. The controller accepts input in the HPGL (Hewlett-Packard Graphics Language) and Calcomp 906/907 vector data formats. The plotters include a Centronics parallel interface and an RS-232C serial interface that operates at speeds as high as 38.4k baud.

The plotters use roll-feed media, and they can produce more than 100 plots with a single roll. You can choose among various types of media, including opaque, translucent, and vellum paper and clear and matte polyester films. The plotters each include a manual cutter for the media. The company also offers an automatic cutter and a take-up roll for paper output; with either of these options, the plotters can operate unattended.

The Model 8524 plots on 24-in.-wide media and costs $19,900, and the Model 8536 uses 36-in.-wide media and sells for $24,900. The 8536 can produce an E-size drawing in 45 sec, and either machine can plot a D-size drawing in 36 sec. The plot time does not vary with image complexity. However, the controller must rasterize a full graphics image before plotting begins.



***HPGL and 906/907 vector data inputs** drive the rasterizing controllers of the 8500 Series plotters, allowing the plotters to operate with most popular graphics-software packages.*

The plotters can print multiple copies of an image at the 1 ips plotting speed. You simply select as many as 999 copies at the control panel. The control panel also allows you to choose a line thickness ranging from 3 to 90 mils. Further, it lets you scale or rotate a drawing, create a mirror image, and change a drawing's point of origin. Each plotter includes a floppy-disk drive that you can use to store and retrieve various plotter setups. The vendor offers OEM discounts on the plotters, and production quantities are available now.—***Maury Wright***

Versatec, 2710 Walsh Ave, Santa Clara, CA 95051. Phone (408) 988-2800. TWX 910-338-0243.

Circle No 719

IF YOU'RE DESIGNING DISK DRIVES AND HAVE ONLY USED OUR READ/WRITE CIRCUITS– THIS CHART IS FOR YOU.

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If you're designing disk drives, you're probably already familiar with Silicon Systems. Chances are good that you are presently using one or more of Silicon Systems' Read/Write amplifier IC's in your HDD designs. But maybe you don't know that we also offer the industry's most extensive line of mass storage ASIC's.

The adjacent chart illustrates that Silicon Systems can also provide more than a score of circuits for pulse detection, data recovery, head positioning, spindle motor control, and controller electronics. And the list continues to grow.

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With Silicon Systems growing families of IC's for all the electronic functions in hard disk drives, many leading HDD designers are finding they can now easily mix-and-match SSi products to implement their specific design features. This powerful design approach allows them to reduce board area, eliminate external passives, and lower costs by simplifying their designs.

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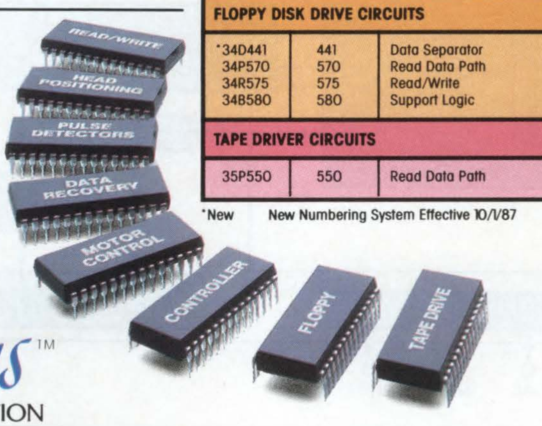
MICROPERIPHERAL IC SELECTION CHART

SSI Device Numbers New	Old	Head Type	# of Channels	Max Input Noise nV/√Hz	Max Input Capacitance (pf)	Read Gain (typ)	Write Current Range (mA)	Power Supplies	Read/Write Data Port(s)
HDD READ/WRITE AMPLIFIERS									
32R104B	104	Ferrite	4	2.4	23	35	15 to 45	+6V, −4V	Differential, Bi-directional
32R104BLN	104L	Ferrite	4	1.7	23	35	15 to 45	+6V, −4V	Differential, Bi-directional
32R114	114	Thin Film	4	1.1	65	123	55 to 110	±5V	Differential/Differential
32R115	115	Ferrite	2, 4, 5	1.8	20	40	30 to 50	±5V	Differential, Bi-directional
32R117	117	Ferrite	2, 4, 6	2.1	23	100	10 to 50	+5V, +12V	Differential/TTL
32R117A	117A	Ferrite	2, 4, 6	1.7	20	100	10 to 50	+5V, +12V	Differential/TTL
32R188	188	Ferrite	4	2.4	18	43	35 to 70	+6V, −5V	Differential, Bi-directional
32R501	501	Ferrite	4, 6, 8	1.5	23	100	10 to 50	+5V, +12V	Differential/TTL
*32R510A	510A	Ferrite	2, 4, 6	1.5	20	100	10 to 40	+5V, +12V	Differential/TTL
*32R511	511	Ferrite	4, 6, 8	1.5	20	100	10 to 40	+5V, +12V	Differential/TTL
*32R512	512	Thin Film	8	0.9	32	150	10 to 40	+5V, +12V	Differential/TTL
*32R514	514	Ferrite	2, 4, 6	1.5	20	150	10 to 40	+5V, +12V	Differential/TTL
32R520	520	Thin Film	4	0.9	65	123	30 to 75	±5V	Differential/Differential
32R521	521	Thin Film	6	0.9	65	100	20 to 70	+5V, +12V	Differential/TTL
*32R522	522	Thin Film	4, 6	1.0	32	100	6 to 35	+5V, +12V	Differential/TTL

SSI Device Numbers New	Old	Circuit Function	Features
HDD PULSE DETECTION			
32P540	540	Read Data Processor	Time Domain Filter
32P541	541	Read Data Processor	AGC, Amplitude & Time Pulse Qualification, RLL Compatible
HDD DATA RECOVERY			
32D531	531	Data Synchronizer	Data Synchronizer/Write Precompensation
*32D532	532	Data Separator	Data Synchronizer/2, 7 RLL ENDEC
*32D533	533	Data Synchronizer	Data Synchronizer/Write Precompensation
*32D534	534	Data Separator	Data Synchronizer/MFM ENDEC/Write Precompensation
*32D535	535	Data Separator	Data Synchronizer/2, 7 RLL ENDEC/Write Precompensation
HDD HEAD POSITIONING			
32H101A	101A	Preamplifier-Ferrite Head	AV = 93, BW = 10MHz, e_n = 7.0nV/√Hz
32H116	116	Preamplifier-Thin Film Head	AV = 250, BW = 20MHz, e_n = 0.94nV/√Hz
*32H567	567	Servo Demodulator	Di-bit Quadrature Servo Pattern: PLL Synchronization
*32H568	568	Servo Controller	Track & Seek Mode Operation; Microprocessor Interface
*32H569	569	Servo Motor Driver	Head Parking, Spindle Motor Braking
HDD SPINDLE MOTOR CONTROL			
32M590	590	2-Phase Motor Speed Control	±0.035% Speed Accuracy; Unipolar Operation
32M591	591	3-Phase Motor Speed Control	±0.05% Speed Accuracy; Unipolar Operation
*32M593	593	3-Phase Motor Speed Control	±0.037% Speed Accuracy; Bipolar Operation
HDD CONTROLLER/INTERFACE			
*32B450A	450A	SCSI Controller	Async transfer to 2MBPS; Initiate/Target Modes; Internal Drivers; CMOS
*32C452	452	Storage Controller	20Mbits/sec; CMOS; Programmable; AIC-010 Compatible
*32C453	453	Buffer Controller	Non-mux addressing to 16K; CMOS; AIC-300 Compatible
32B545	545	Support Logic	Includes ST506 Bus Drivers/Receivers
FLOPPY DISK DRIVE CIRCUITS			
*34D441	441	Data Separator	High Performance Analog Data Separator, NEC 765 Compatible
34P570	570	Read Data Path	2 Channel Read/Write With Read Data Path
34R575	575	Read/Write	2, 4 Channel Read/Write Circuit
34B580	580	Support Logic	Port Expander, Includes SA400 Interface Drivers/Receivers
TAPE DRIVER CIRCUITS			
35P550	550	Read Data Path	4 Channel Read/Write With Read Data Path

*New New Numbering System Effective 10/1/87



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Monolithic A/D converter delivers 1-MHz, 12-bit performance at low cost

For designs that require a high-speed, 12-bit sampling A/D converter, consider using the CSZ5412-JC1, a monolithic 1-MHz A/D converter. This IC offers speed and accuracy that matches or exceeds the performance of hybrid alternatives while consuming a third of the power—700 mW—and selling for only $180 (100). This price includes the sample-and-hold circuitry that you must add to many competing hybrid devices.

Using a 2-step flash A/D conversion to achieve its high speed and accuracy, the CSZ5412 incorporates self-calibrating circuitry, pipelined acquisition and settling times, and overlapped conversion cycles. The 2-step technique requires a track-and-hold amplifier, a 6-bit flash A/D converter, a 6-bit D/A converter, and a differential amplifier—all of which are provided on the chip's monolithic substrate.

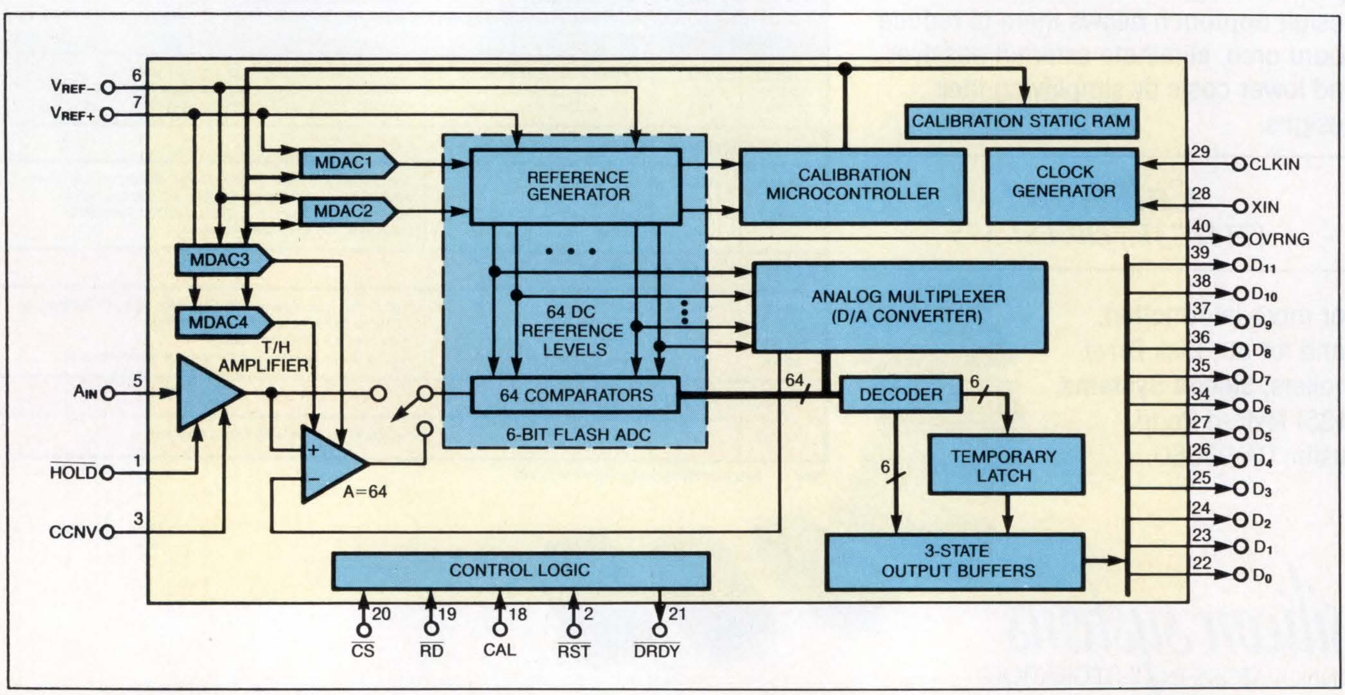
The device's pipelined settling times, which are used in both the sampling and the conversion processes, give the converter its 1-MHz throughput rate. The device can actually begin a conversion cycle while it's still operating on the previous sample. This process of overlapping the conversion cycles by using a pair of track-and-hold amplifiers results in a throughput time that's shorter than the device's conversion time.

The CSZ5412 uses several calibration techniques to ensure 12-bit accuracy over time and temperature. For example, it has a reference-generating circuit that provides 64 graduated reference levels; the circuit continually adjusts the levels to 12-bit accuracy. Further, an on-chip μC provides digital correction that calibrates the device's gain and offset and minimizes linearity errors at the 64 segment boundaries.

You can connect the converter directly to a μP's data and control buses because it comes with an overrange output, 3-state output buffers, and a flexible control interface. Alternatively, the device can operate in stand-alone mode, independently of microprocessor control. The converter specs a 3V analog-input range. The device's total harmonic-distortion spec is 0.02%, and its dynamic range is 72 dB. You can also order a similar device, the CSZ5412-JC2, which has a 500-kHz conversion rate and costs $115 (100).—***J D Mosley***

Crystal Semiconductor Corp, Box 17847, Austin, TX 78760. Phone (512) 445-7222. TWX 910-874-1352.

Circle No 721



This 40-pin monolithic CMOS A/D converter *is a low-power, low-cost, self-calibrating device that provides a 12-bit representation of an analog input signal at sampling rates as fast as 1 MHz.*

Rack-mountable, 5½-digit programmable multimeter features 8-channel scanner

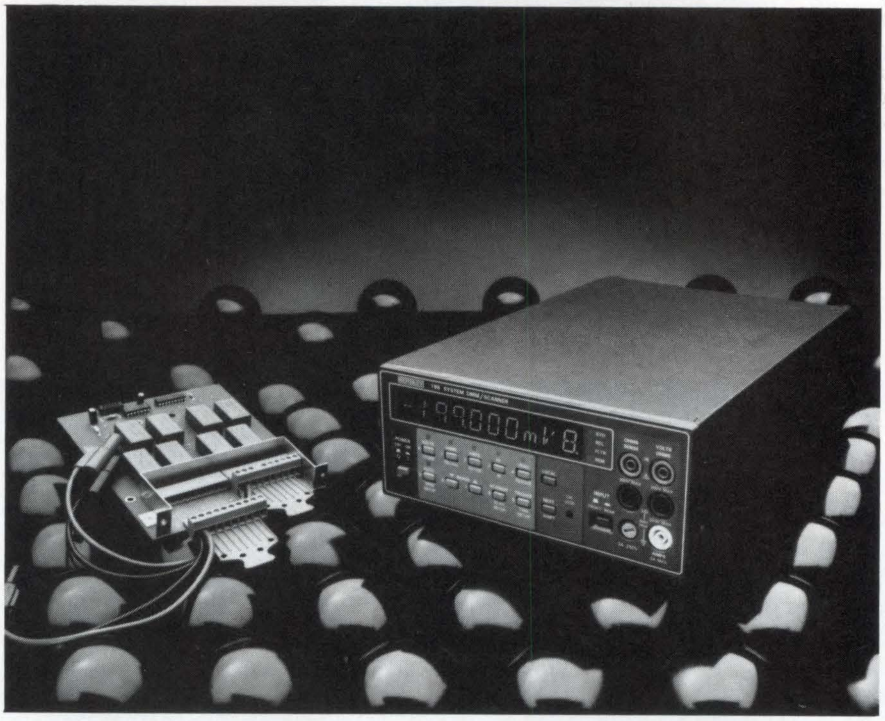
Combining two instruments in one half-rack-size enclosure, the Model 199 systems digital multimeter and scanner is a $1395 instrument that provides $3000 of functionality: Purchased separately, the devices would cost $3000. You can order the Model 199 without its scanner option for $995—a price lower than that of most other 5½-digital multimeters on the market.

The multimeter's mainframe features microprocessor control, which allows the instrument to control a switching module. The multimeter alone measures dc and ac voltage, dc and ac amps, ohms, and decibels. By adding the 8-channel scanner option, you transform the instrument into a complete multichannel measurement system.

The instrument's sensitivity specs are 1 μV, 1 mΩ, and 100 nA, and its best 1-year dc-voltage accuracy is 0.007% of reading. You can take 150 readings/sec at a resolution of 4½ digits and store them in an internal buffer. You can trigger the readings externally.

The optional scanner, which you can install at your site, offers a switching speed of 400 channels/sec (including measurement time), 2-pole and 4-pole switching, and less than 1-μV thermal offset in switch contacts. The low thermal offset lets the Model 199 accurately switch and measure low signal levels. Further, the scanner's 4-pole switching mode provides Kelvin-type (4-wire) resistance measurements.

The unit can switch and take measurements across 40 channels/sec. The manufacturer specifies a 25-msec internal delay between channel changes; this delay includes switch settling time as well as the time it takes to process a reading.



Combining an IEEE-488 digital multimeter and an 8-channel scanner *in a single enclosure, the Model 199 offers 5½-digit precision and costs $1395. Its Translator software lets you easily convert the code of your existing test programs for use on the 199.*

The multimeter, which you can program via its IEEE-488 bus, houses 500 memory locations. By using internal memory to store readings, the unit can reach its maximum speed of 150 readings/sec.

By adding the scanner, you can use the Model 199 as an 8-channel data logger that operates either under computer control or as a stand-alone instrument. The data logger can take readings at intervals varying from 16 msec to 16.6 minutes, or it can take readings asynchronously, at the command of external control equipment. With the scanner, the multimeter can also subtract, divide, and compute the ratio of two values.

The multimeter comes with Translator, a program that lets you add the Model 199 to your existing automated-test system, yet make only minimal changes to any test software you've already written. Translator replaces lengthy IEEE-488 device-dependent program code with short, mnemonic commands. It allows the multimeter to execute a program written for another multimeter or scanner when you place special translation statements at the beginning of your test program. The Translator software codes reside in the DMM's nonvolatile memory.

—J D Mosley

Keithley Instruments Inc, 28775 Aurora Rd, Cleveland, OH 44139. Phone (216) 248-0400. TLX 985469.

Circle No 722

Achiever:

START WITH a complete, full performance, 5½-digit system DMM. And then...

Over Achiever:

INSTALL the 8-channel switching option for an integrated system—in one package. For datalogging and more applications...

The Model 199 System DMM/Scanner

KEITHLEY

Put a complete DMM in your measurement system.

Satisfy your measurement needs with the Model 199's 5½-digit resolution and 6-function performance: DC and AC volts, , DC and AC amps, ohms (2- and 4-wire), and dB (for AC volts and amps). All standard—and so is the IEEE-488 interface.

You also get excellent Keithley sensitivity (1μV, 1mΩ, 100nA), with 60ppm accuracy*. And the 199 gives you the extras, like a 500-reading internal memory, to help get the most from your most essential measurement instrument. Use the 199 on your bench or in a system—it's cost-effective and convenient in both situations.

*DC volts, 90 days.

Fast—Where It Counts. The Model 199 isn't just fast, it's fast where it counts—in your high performance test system. You can synchronize the 199 to your system and achieve a rate of 150 readings per second, with 4½-digit resolution. Storing readings in the 500-point memory frees your system controller for other work.

Stand-Alone Data Logging. Use the Model 199 to track drift or other trends. Under front panel control, the 199 can be programmed to automatically store up to 500 readings at intervals from 15ms to 16.6 minutes (over 5 days of data), or at any externally-triggered time interval.

More Performance, Maximum Utility.

- Enable a 30-reading running average filter to measure noisy signals.
- Use the ZERO function to subtract offsets or make measurements referenced to a user-defined baseline
- Display messages to prompt an operator in a semi-automated system.
- Save your DMM setup to avoid reprogramming the Model 199 on power-up.
- Automatically calibrate the Model 199 from the IEEE-488 bus on either front or rear inputs. Seal the front panel calibration lock switch for security.
- Reduce programming time—use the 199's non-volatile TRANSLATOR software to reduce the length of transmitted command strings, or to emulate the commands of an older DMM.

MAXIMUM READING RATES (Readings/Second)[1]

DCV, DCA, ACV, ACA

RESOLUTION	Continuous Into Memory MUX: OFF	Continuous Into Memory MUX: ON	External Trigger Into Memory MUX: OFF	External Trigger Into Memory MUX: ON	Triggered Via IEEE-488 Bus[2] MUX: OFF	Triggered Via IEEE-488 Bus[2] MUX: ON
4½-Digit	65	65	150	62	80	49
5½-Digit	35 (29)	9 (7.5)	40 (33)	9 (7.5)	34 (29)	9 (7.5)

OHMS

RESOLUTION	Continuous Into Memory MUX: OFF	Continuous Into Memory MUX: ON	External Trigger Into Memory MUX: OFF	External Trigger Into Memory MUX: ON	Triggered Via IEEE-488 Bus[2] MUX: OFF	Triggered Via IEEE-488 Bus[2] MUX: ON
4½-Digit	43	20	47	20	30	18
5½-Digit	16 (13)	9 (7.5)	18 (15)	9 (7.5)	15 (12.5)	9 (7.5)

[1]Reading rates are for fixed range readings with filters off, for 3V, 3kΩ, and 30mA ranges. 5½-digit rate is for 60Hz operation. Values in parentheses are for 50Hz operation.
[2]One shot on TALK.

STORAGE & SCANNING CAPABILITIES

500-Reading Memory: Stores reading, range, and scanner channel.

Trigger: One shot or continuous from front panel, IEEE-488 bus, and rear panel BNC.

Programmable Reading Interval: 15ms to 999.999s.

Programmable Trigger Delay: 1ms to 999.999s.

WITH MODEL 1992 8-CHANNEL SCANNER

Programmable Configuration: 2- or 4-pole.

Programmable Channel Limit: 1 to 8.

Programmable Scanning Modes: Manual, step, and scan.

Ratio: Channels 2 through 8 referenced to Channel 1.

IEEE-488 BUS IMPLEMENTATION

MULTILINE COMMANDS: DCL, LLO, SDC, GET, GTL, UNT, UNL, SPE, SPD.

UNILINE COMMANDS: IFC, REN, EOI, SRQ, ATN.

INTERFACE FUNCTIONS: SH1, AH1, T6, TE0, L4, LE0, SR1, RL1, PP0, DC1, DT1, C0, E1.

All front panel functions and programs are available over the IEEE-488 bus, in addition to Status, Service Request, Output Format, EOI, Trigger, Terminator, Display Message, and Non-Volatile TRANSLATOR.

IEEE-488 address is programmable from the front panel.

MODEL 1992 SCANNER OPTION

CONTACT CONFIGURATION: 8-channel 2-pole, or 4-channel 4-pole.

CONTACT POTENTIAL: $<1\mu V$ per contact pair.

MAXIMUM SWITCHING RATE: 40 channels/second, including Model 199 4½-digit DCV reading time.

CONNECTOR TYPE: Quick disconnect screw terminals, #14 AWG maximum wire size.

MAXIMUM SIGNAL LEVEL: 200V peak, 100mA, resistive load.

CONTACT LIFE: $>10^6$ operations (at maximum signal level); $>10^8$ operations (cold switching).

CONTACT RESISTANCE: $<1\Omega$.

ISOLATION BETWEEN ANY TWO TERMINALS: $>10^9\Omega$, <75pF.

ISOLATION BETWEEN ANY TERMINAL AND EARTH: $>10^9\Omega$, <150pF.

COMMON MODE VOLTAGE: 350V peak between any terminal and earth.

MAXIMUM VOLTAGE BETWEEN ANY TWO TERMINALS: 200V peak.

MAXIMUM VOLTAGE BETWEEN ANY TERMINAL AND MODEL 199 INPUT LO: 200V peak.

DIMENSIONS, WEIGHT: 25mm high × 130mm wide × 170mm deep (⅞ in. × 5 in. × 6½ in.). Adds 0.3kg (8 oz.) to Model 199.

GENERAL

MAXIMUM READING: 302,999 counts in 5½-digit mode.

CONNECTORS: Measurement: Switch selectable front or rear, safety jacks. **Digital:** TRIGGER input and METER COMPLETE output on rear panel, BNCs.

WARMUP: 2 hours to rated accuracy.

TEMPERATURE COEFFICIENT (0°-18°C & 28°-50°C): $<\pm(0.1 \times$ applicable accuracy specification)/°C.

ISOLATION: Input LO to IEEE LO or power line ground: 500V peak. 5×10^5 V•Hz maximum. $>10^9\Omega$ paralleled by 400pF.

OPERATING ENVIRONMENT: 0°-50°C, 80% relative humidity up to 35°C; linearly derate 3% RH/°C, 35°-50°C (0%-60% RH up to 28°C on 300MΩ range).

STORAGE ENVIRONMENT: −25° to +65°C.

POWER: 105-125V or 210-250V, rear panel switch selected, 50Hz or 60Hz, 20VA maximum. 90-110V and 180-220V versions available upon request.

DIMENSIONS, WEIGHT: 90mm high × 220mm wide × 330mm deep (3½ in. × 8⅝ in. × 12⅞ in.). Net weight 3kg (6 lbs., 8 oz.).

ACCESSORIES SUPPLIED: Model 1751 Safety Test Leads, Instruction Manual.

ACCESSORIES AVAILABLE:

Model 1992:	8-Channel Scanner	$395.00
Model 1993:	Quick Disconnect Scanner Connector Kit	45.00
Model 1998-1:	Single Fixed Rack Mounting Kit	40.00
Model 1998-2:	Dual Fixed Rack Mounting Kit	65.00
Model 1651:	50-Ampere Shunt	55.00
Model 1681:	Clip-On Test Lead Set	15.00
Model 1682A:	RF Probe	69.00
Model 1685:	Clamp-On Current Probe	105.00
Model 1751:	General Purpose Test Leads	15.00
Model 1754:	Universal Test Lead Kit	25.00
Model 5806:	Kelvin Clip Leads	195.00
Model 7007-1:	Shielded IEEE-488 Cable, 1m	89.00
Model 7007-2:	Shielded IEEE-488 Cable, 2m	99.00
Model 7008-3:	IEEE-488 Cable, 0.9m (3 ft.)	77.00
Model 7008-6:	IEEE-488 Cable, 1.8m (6 ft.)	85.00

MODEL 199 SYSTEM DMM/SCANNER $995.00

MODEL 199/1992 SYSTEM DMM/SCANNER with 8-Channel Scanner Option $1390.00

Prices and specifications subject to change without notice.

DC VOLTS (5½ Digits)

RANGE	RESOLUTION	INPUT RESISTANCE	ACCURACY[1] ±(%rdg + counts) 24 Hours[2] 23°±1°C	90 Days 18°-28°C	1 Year 18°-28°C
300 mV	1 µV	>1 GΩ	0.004 + 3[3]	0.009 + 3[3]	0.012 + 3[3]
3 V	10 µV	>1 GΩ	0.003 + 2	0.006 + 2	0.007 + 2
30 V	100 µV	11 MΩ	0.004 + 2	0.008 + 2	0.009 + 2
300 V	1 mV	10 MΩ	0.004 + 2	0.008 + 2	0.009 + 2

[1]For 4½-digit accuracy, count error is 5 (except 15 on 300mV range).
[2]Relative to calibration standards.
[3]When properly zeroed.

CMRR: >120dB at dc, 50Hz or 60Hz (±0.05%) with 1kΩ in either lead.

NMRR: >60dB at 50Hz or 60Hz (±0.05%).

MAXIMUM ALLOWABLE INPUT: 300V rms or 425V peak, whichever is less.

TRMS AC VOLTS (5½ Digits)

RANGE	RESOLUTION	ACCURACY[1] ±(%rdg + counts) 1 Year, 18°-28°C: 20 Hz - 50 Hz[2]	50 Hz - 200 Hz[2]	200 Hz - 20 kHz[2]	20 kHz - 100 kHz[3]
300 mV	1 µV	2 + 100	0.35 + 100	0.15 + 200	2.0 + 300
3 V	10 µV	2 + 100	0.35 + 100	0.15 + 200	1.5 + 300
30 V	100 µV	2 + 100	0.35 + 100	0.15 + 200	1.5 + 300
300 V	1 mV	2 + 100	0.35 + 100	0.15 + 200	1.5 + 300

[1]For 4½-digit accuracy, divide count error by 10; 4½-digit specifications apply for inputs >200Hz.
[2]Sinewave inputs >2000 counts.
[3]Sinewave inputs >20,000 counts.

RESPONSE: True root mean square, ac coupled.

CREST FACTOR (ratio of peak to rms): Up to 3:1 allowable.

NON-SINUSOIDAL INPUTS (>20,000 counts):
For rectified sine wave, add 0.3% of reading to above specifications for fundamental frequencies <20kHz.
For pulse waveforms, add 0.3% of reading for fundamental frequencies <1kHz, or 3.5% for frequencies <10kHz.

INPUT IMPEDANCE: 1MΩ shunted by <100pF.

MAXIMUM ALLOWABLE INPUT: 300V rms or 425V peak, 10^7V•Hz, whichever is less.

CMRR: >60dB at 50Hz or 60Hz (±0.05%) with 1kΩ in either lead.

SETTLING TIME: 1 second to within 0.1% of change in reading.

dB (ref = 1V):

INPUT	RESOLUTION	ACCURACY ±dB 1 Year, 18°-28°C: 20 Hz-20 kHz	20 kHz-100 kHz
−34 to +49 dB (20 mV to 300 V)	0.01 dB	0.2	0.4
−54 to −34 dB (2 mV to 20 mV)	0.01 dB	1.1	—

OHMS (5½ Digits)

RANGE	RESOLUTION	NOMINAL I-SHORT	ACCURACY[1] ±(%rdg + counts) 24 Hours[4] 23° ±1°C	90 Days 18°-28°C	1 Year 18°-28°C
300 Ω[2]	1 mΩ	1.7 mA	0.005 + 4[3]	0.009 + 4[3]	0.012 + 4[3]
3 kΩ[2]	10 mΩ	1.7 mA	0.004 + 2	0.008 + 3	0.009 + 3
30 kΩ[2]	100 mΩ	160 µA	0.004 + 2	0.008 + 3	0.009 + 3
300 kΩ	1 Ω	50 µA	0.014 + 2	0.024 + 3	0.026 + 3
3 MΩ	10 Ω	5 µA	0.02 + 2	0.03 + 3	0.03 + 3
30 MΩ	100 Ω	0.5 µA	0.1 + 5	0.12 + 5	0.12 + 5
300 MΩ	1 kΩ	0.5 µA	2.0 + 5	2.0 + 5	2.0 + 5

[1]For 4½-digit accuracy, count error is 5 (except 15 on 300Ω range).
[2]4-wire accuracy, 300Ω-30kΩ ranges.
[3]When properly zeroed.
[4]Relative to calibration standards.

CONFIGURATION: Automatic 2- or 4-wire.

MAXIMUM ALLOWABLE INPUT: 300V rms or 425V peak, whichever is less.

OPEN CIRCUIT VOLTAGE: <5.5V.

DC AMPS (5½ Digits)

RANGE	RESOLUTION	ACCURACY[1] ±(%rdg + counts) 1 Year, 18°-28°C	MAXIMUM VOLTAGE BURDEN
30 mA	100 nA	0.05 + 15	0.4 V
3 A	10 µA	0.1 + 15	2 V

[1]For 4½-digit accuracy, count error is 20.

MAXIMUM ALLOWABLE INPUT: 3A. Protected with 3A, 250V fuse accessible from front panel.

TRMS AC AMPS (5½ Digits)

RANGE	RESOLUTION	ACCURACY[1] ±(%rdg + counts) 1 Year, 18°-28°C: 20 Hz-45 Hz	45 Hz-10 kHz	MAXIMUM VOLTAGE BURDEN
30 mA	100 nA	2 + 100	0.6 + 100	0.4 V
3 A	10 µA	2 + 100	0.6 + 100	2 V

[1]Inputs >2000 counts. For 4½-digit accuracy, divide count error by 10; 4½-digit specifications apply for inputs >200Hz.

RESPONSE: True root mean square, ac coupled.

CREST FACTOR (ratio of peak to rms): Up to 3:1 allowable at ⅔ full range.

NON-SINUSOIDAL INPUTS: Specified accuracy for fundamental frequencies <1kHz.

MAXIMUM ALLOWABLE INPUT: 3A. Protected with 3A, 250V fuse accessible from front panel.

SETTLING TIME: 1 second to within 0.1% of final reading.

dB (ref = 1mA):

INPUT	RESOLUTION	ACCURACY ±dB 1 Year, 18°-28°C 20 Hz-10 kHz
−14 to +69 dB (200 µA to 3 A)	0.01 dB	0.6

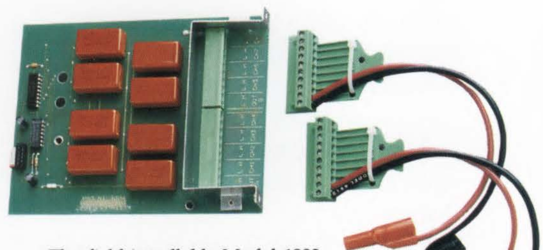
Add the 1992 Scanner option to make the 199 an integrated, 8-channel measurement system.

Put a complete measurement system in your DMM.

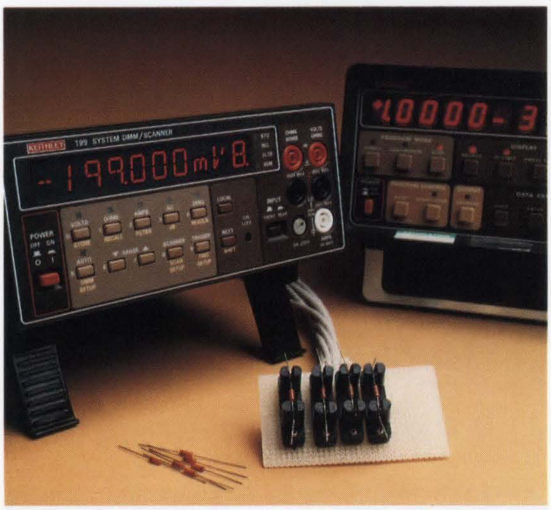
The Model 199 DMM/Scanner combination can switch and measure up to 40 channels per second. And the sensitivity of the 199 is accessible through the scanner—each set of contacts creates less than 1μV contact error. You can also make low level resistance measurements—the scanner can make 4-wire measurements on 4 channels or 2-pole measurements on 8 channels. Directly display Ratio for testing components to specific tolerances.

$$\text{Ratio} = \frac{\text{Channel } n}{\text{Channel } 1}$$

$(n = 2, \ldots 8)$



The field-installable Model 1992 8-Channel Scanner Option comes with two quick disconnect scanner connectors and test lead sets. You can order extra sets of connectors and leads (Model 1993 Quick Disconnect Scanner Connector Kit) to save different wiring setups.

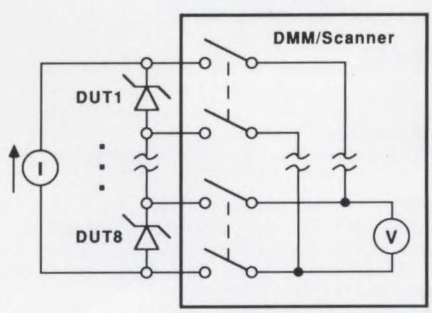


Use the Model 199 DMM/Scanner to evaluate multiple components, such as zener diodes, in a single test. Use the scanner in three different ways:

Manual: Operate channels individually.

Step: Automatically increment through each channel at a defined interval.

Scan: Automatically scan a set of channels at a defined interval.



Savings Through Integration

By combining two instruments in one, Keithley saves you:

- *Valuable rack space:* The 199 comes in a new, compact package.
- *Learning time:* Start up quickly by learning one instrument instead of two.
- *Controller time:* Reduced IEEE-488 bus handshake time.
- *One IEEE-488 address.* Access a single location.
- *Cost:* Use the Model 199 DMM/Scanner instead of up to 8 DMMs, a DMM and separate scanner, or an 8-channel datalogger.

Complete Confidence For Your Complete System.

Keithley recognizes your need for incorporating reliable instrumentation into your system. The high-reliability design and 2-year warranty of the Model 199 DMM/Scanner make it an excellent value. Order your Model 199 now on a 30-day money-back guarantee.

$995 DMM

$1390 DMM + scanner

1-800-552-1115

Model 196: Extended system performance.

When even smaller changes must be measured, the 6½-digit Model 196 System DMM provides the necessary extended performance. The 196 resolves changes as small as 1 part in 3,000,000, and with excellent sensitivity. You can make these measurements with confidence: the 196 is accurate to 30ppm (DC volts, 90 days). In addition, offset compensated ohms eliminates errors caused by thermal contact potentials.

When high speed is your main concern, the Model 196 can take 3½-digit readings at 1000 per second into its 500-reading memory.

With front/rear inputs, Voltmeter Complete and External Trigger signals, and IEEE-488 interface, the Model 196 provides full-rack systems capability—in a half rack case, at a half rack price.

$1395

	Sensitivity	Maximum Reading	Basic Accuracy
DCV	100nV	300V	0.003%
ACV	1μV	300V	0.15%
Ohms	100$\mu\Omega$	300MΩ	0.005%
DCA, ACA	1nA	3A	0.05% 0.6%

FRONT PANEL PROGRAMS	
Menu	Set Hi/Lo Limits
Display Resolution	Digital Calibration
mX+b	Reset to factory default conditions
Hi/Lo/Pass	Offset Compensation
Multiplex On/Off	Zero Modify
Save Setup	Filter Constants
IEEE-488 Address	dB Reference
Line Frequency	
Self Test	
Set m,B Constants	

Complete Support For Your Application. Our full line of precision sources, scanners, and measurement instruments enables you to build a complete system of compatible Keithley components for your application. Incorporate powerful software packages such as ASYST and DADiSP to handle your data acquisition and analysis needs.

Our Application Engineers are available to discuss your difficult measurement requirements with you. We do more than just tell you how to operate our instruments—we offer suggestions to help you solve your measurement problems. Contact our Information Center to discuss your requirements with an Application Specialist.

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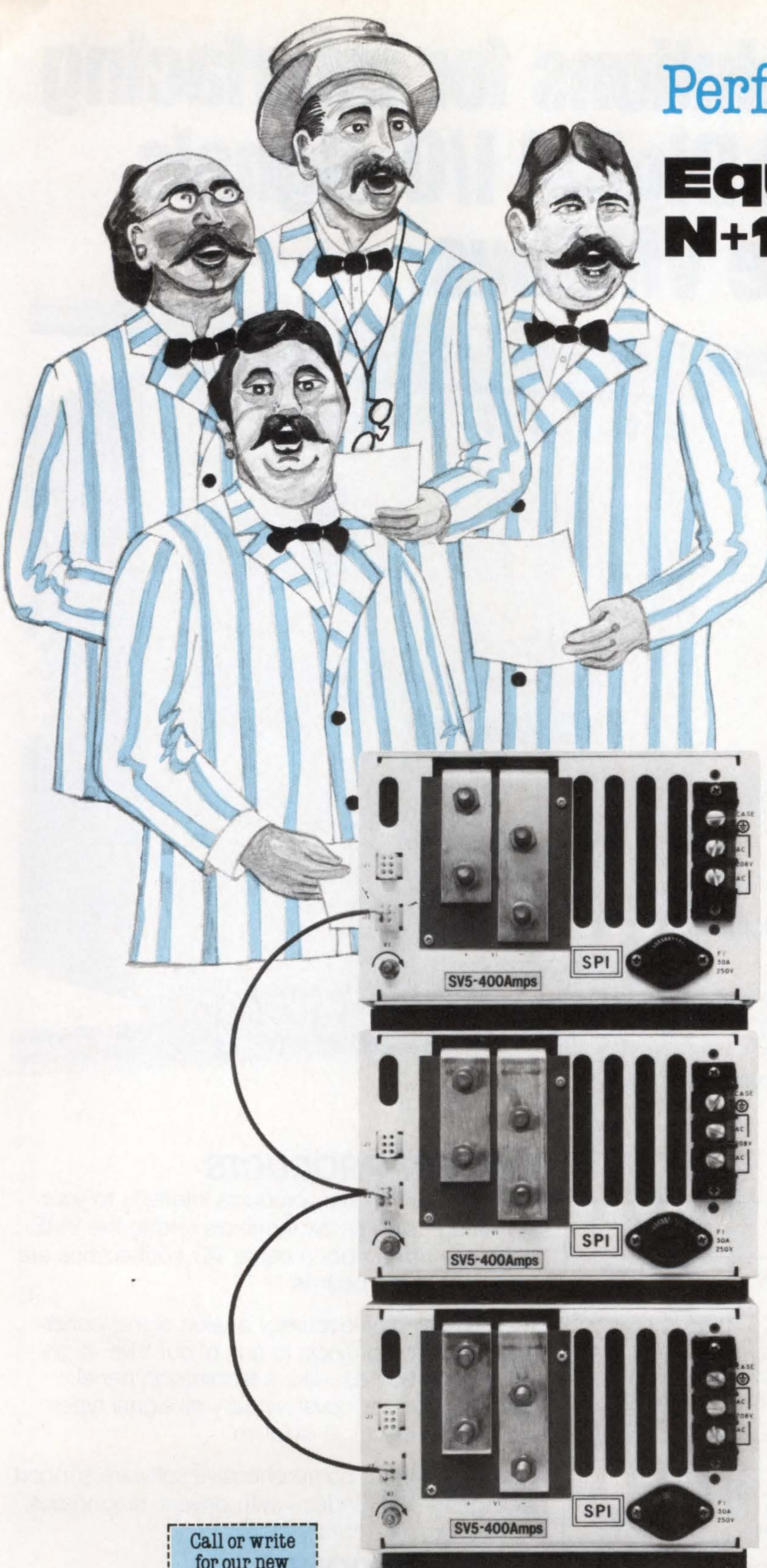

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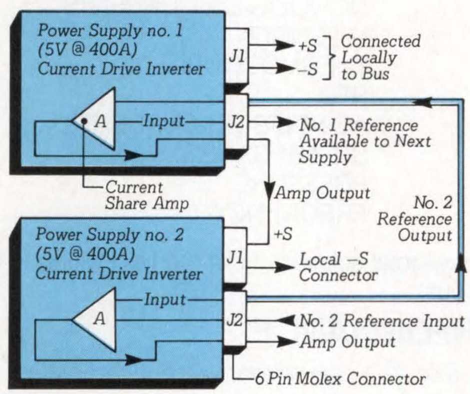

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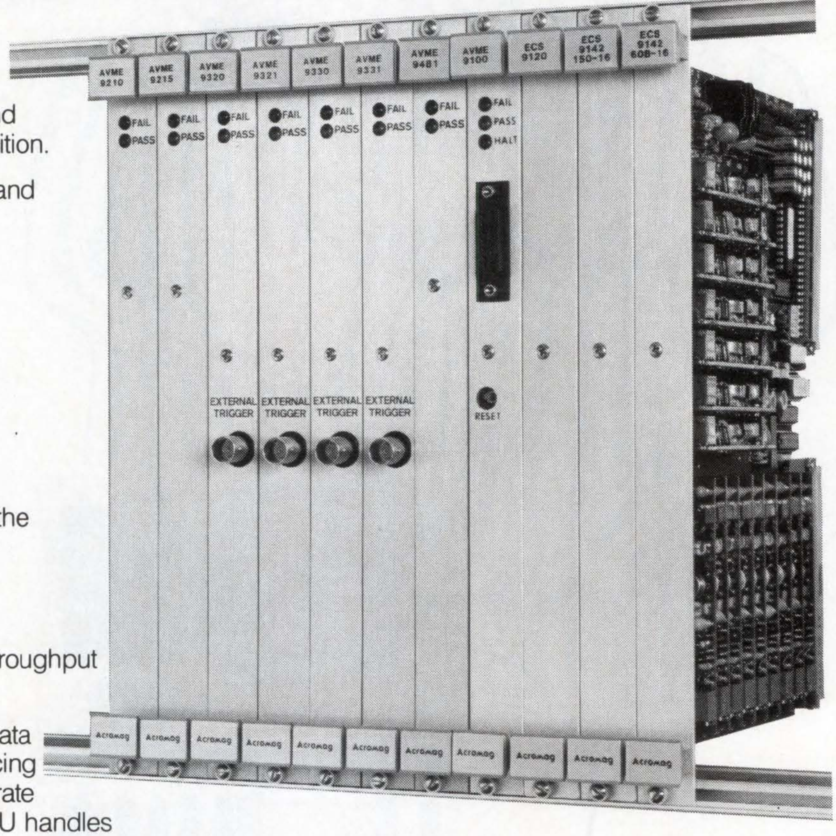
CIRCLE NO 180

Acromag has solutions for interfacing A/D, D/A and Digital I/O signals to the VMEbus.



Our extensive line of VMEbus-based products handles your interfacing applications for test and measurement, industrial control, or data acquisition.

If you need to interface with industrial sensors and industry standard field signals:

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RTD
AC VOLTS OR CURRENTS
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FREQUENCY

We have total solutions from the field wiring to the VMEbus.

PERFORMANCE

For basic A/D conversion, we've incorporated many operational features to improve overall throughput to your host processor.

For more advanced applications, Acromag's Data Acquisition Subsystem simplifies sensor interfacing and reduces host activity. So you can concentrate on processing the data while our on-board CPU handles routine tasks.

Function	In/Out	Max Signal Range**	Features	Product
High-Speed Analog I/O	16D/32SE*in 2 out, opt.	±10 in/out	12 Bit A/D, 67K chan/sec throughput 12 Bit D/A	AVME9320 AVME 9321
High-Res. Analog I/O	16D/32SE in 2 out, opt.	±10 V in/out	14 Bit A/D, 33K chan/sec throughput 12 Bit D/A	AVME 9330 AVME 9331
Analog Out	8 out	±10V, Vout 4-20mA, Iout	12 Bit D/A, 6 μ sec Vout, 25 μ sec Iout, throughput	AVME9210 AVME 9215
Data Acq. Controller	16D/32SE in, opt.	±10V	14 Bit A/D, 256 in, scans, linearizes, limit checks	AVME9100 AVME9110
Subsystem Expanders	16D/32SE in	±10V	High level expander	ECS9120
	16D in	±10V	Filtered inputs	ECS9121
	8D/16D in	−6 to +60mV −15 to +150mV Thermocouple	250V isolation, interface for TC, RTD, and Pressure with termination panels	ECS9142-60 ECS9142-150 ECS9142-60B
Digital I/O	64 in/out	0-30V in/out	8 in with latch and interrupt	AVME9480 AVME9481

*SE - Single ended D - Differential
**Most inputs and outputs have programmable ranges.

SUPPORT PRODUCTS

Acromag's termination products interface to your field wiring using screw terminals and to the VME backplane using ribbon cable. I/O connections are at the rear of the boards.

The modular, high-accuracy analog signal conditioning system connects to any of our VME high-level analog boards—like a termination panel. Available modules cover virtually all signal types and provide electrical isolation.

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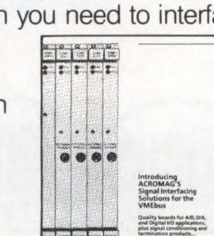

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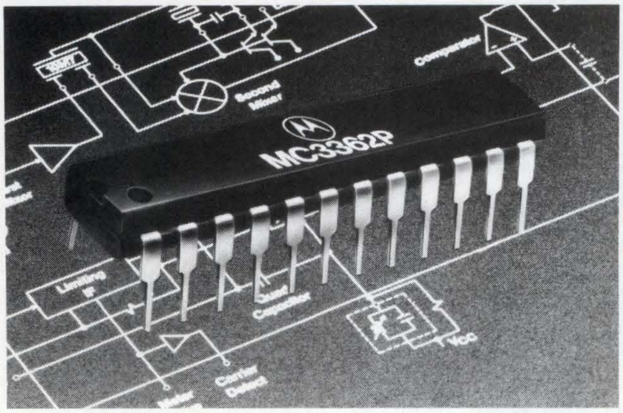
CIRCLE NO 175

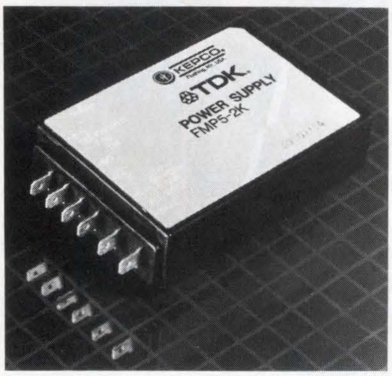
READERS' CHOICE

Of all the new products covered in EDN's **December 10, 1987,** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, or refer to the indicated pages in our **December 10, 1987,** issue.



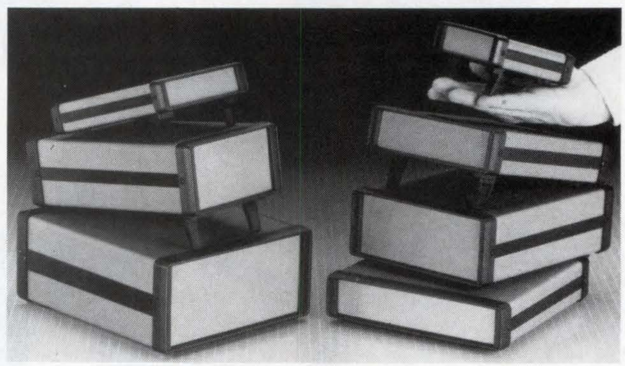
◄ FM RECEIVER

The MC3362 IC is a narrowband-FM, dual-conversion low-voltage (2V) receiver that incorporates all essential VHF-receiver functions, from the antenna input to the audio preamp output (pg 304).
Motorola Inc.
Circle No 605



▲ SWITCHING MODULES

FMP Series single-output switching modules come in low-profile, plastic-encased packages (pg 205).
Kepco Inc.
Circle No 604

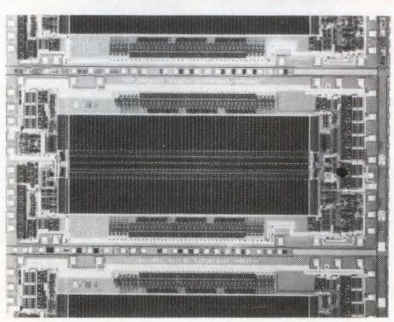


▲ ALUMINUM ENCLOSURES

The SL Series consists of seven small aluminum enclosures that provide EMI shielding and help to dissipate heat (pg 115).
Tracewell Enclosures.
Circle No 602

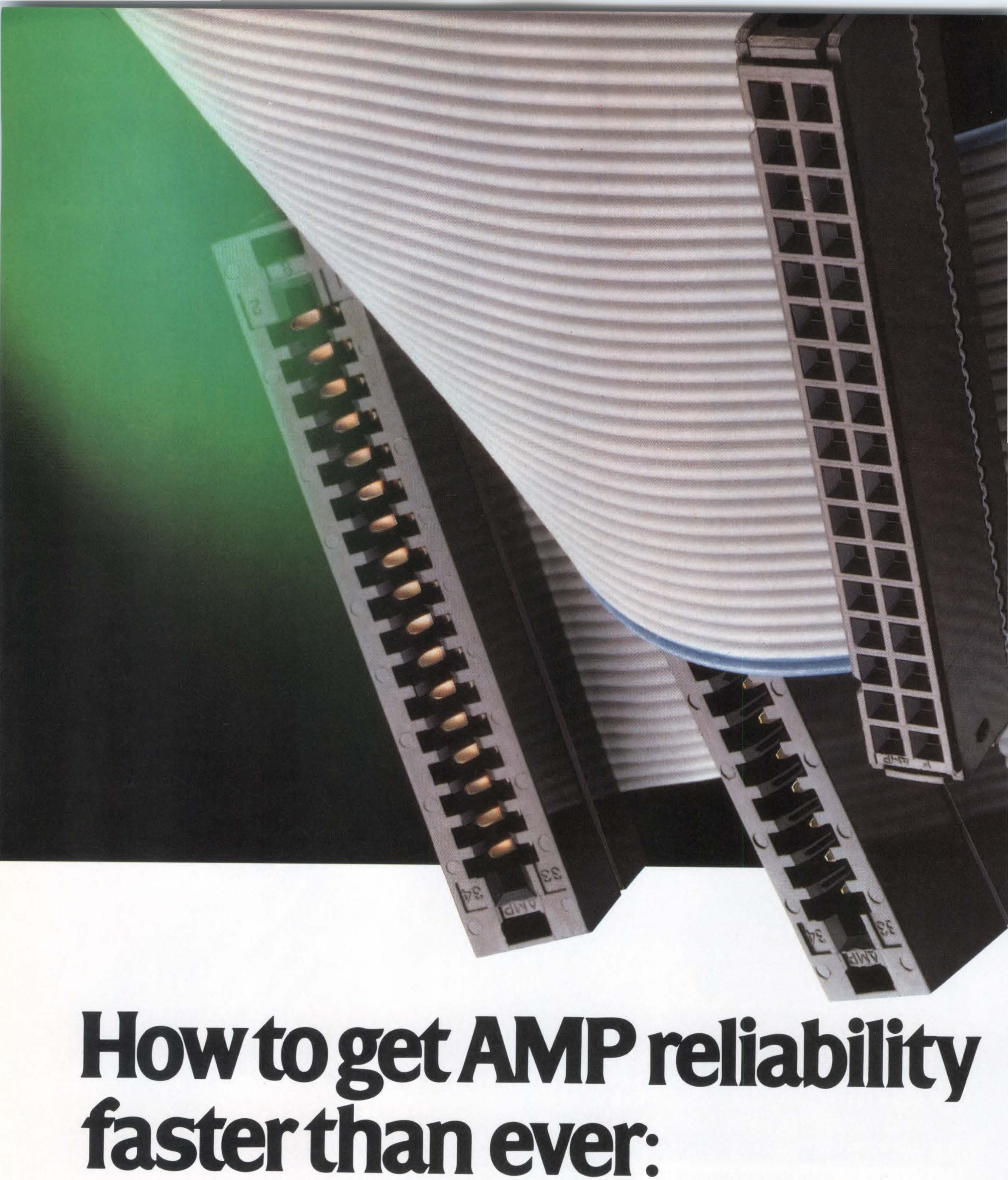
C COMPILER

Turbo C is a C editor, compiler, and linker that runs on the IBM PC and compatibles (pg 179).
Borland International.
Circle No 603



◄ CMOS FIFO

The MK4505 is an edge-triggered, latched, expandable, and cascadable FIFO buffer that offers a 15-nsec access time (pg 59).
Thomson Components-Mostek Corp.
Circle No 601



How to get AMP reliability faster than ever: more sources than ever.

LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	8	58	17	17	0	0	5.7	9.3
Pot-Core	0	50	25	17	8	0	8.2	9.4
Laminate (power)	6	39	33	17	5	0	7.8	8.7
CONNECTORS								
Military panel	0	0	67	17	16	0	12.2	11.5
Flat/Cable	17	44	28	11	0	0	5.3	6.6
Multi-pin circular	10	40	20	20	10	0	8.0	10.0
PC (2-piece)	0	33	45	22	0	0	8.0	7.3
RF/Coaxial	13	40	13	27	7	0	8.1	6.4
Socket	6	67	11	11	5	0	6.0	5.3
Terminal blocks	25	45	15	10	5	0	5.4	5.6
Edge card	19	44	19	12	6	0	6.3	6.3
D-Subminiature	13	40	33	7	7	0	6.6	6.2
Rack & panel	0	45	33	11	11	0	8.6	6.8
Power	0	29	29	28	14	0	11.2	7.2
PRINTED CIRCUIT BOARDS								
Single-sided	0	74	21	5	0	0	4.7	5.1
Double-sided	0	46	50	4	0	0	6.0	6.9
Multi-layer	0	23	69	8	0	0	7.4	7.9
Prototype	5	85	10	0	0	0	3.4	3.5
RESISTORS								
Carbon film	35	45	20	0	0	0	3.0	3.6
Carbon composition	28	43	19	10	0	0	4.3	3.1
Metal film	15	50	35	0	0	0	4.3	4.4
Metal oxide	11	56	22	11	0	0	5.2	4.8
Wirewound	4	46	32	14	4	0	7.2	7.2
Potentiometers	7	55	31	7	0	0	5.2	6.4
Networks	16	37	32	10	5	0	6.6	4.7
FUSES	54	38	8	0	0	0	1.8	3.8
SWITCHES								
Pushbutton	11	72	11	6	0	0	3.9	6.0
Rotary	5	67	11	17	0	0	5.5	7.3
Rocker	6	59	23	12	0	0	5.5	5.7
Thumbwheel	0	69	15	16	0	0	5.7	8.4
Snap action	0	64	29	7	0	0	5.3	5.6
Momentary	7	60	26	7	0	0	5.0	5.6
Dual in-line	0	50	20	30	0	0	7.8	6.4
WIRE AND CABLE								
Coaxial	23	68	9	0	0	0	2.8	3.3
Flat ribbon	26	42	32	0	0	0	3.8	4.0
Multiconductor	25	50	25	0	0	0	3.5	4.6
Hookup	23	65	12	0	0	0	2.9	3.1
Wire wrap	38	54	8	0	0	0	2.2	4.8
Power cords	28	56	12	4	0	0	10.8	4.5
POWER SUPPLIES								
Switcher	6	41	29	24	0	0	7.2	10.1
Linear	0	55	27	18	0	0	6.6	9.5
CIRCUIT BREAKERS	7	33	27	33	0	0	8.3	8.2
HEAT SINKS	17	46	33	4	0	0	4.7	6.2
RELAYS								
General purpose	13	67	12	8	0	0	4.3	6.9
PC board	0	79	0	21	0	0	5.7	8.5

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
RELAYS								
Dry reed	0	40	40	20	0	0	7.5	8.9
Mercury	20	40	40	20	0	0	4.4	8.8
Solid state	0	54	31	15	0	0	6.5	7.5
DISCRETE SEMICONDUCTORS								
Diode	32	42	19	7	0	0	3.8	7.8
Zener	35	35	15	15	0	0	4.7	8.8
Thyristor	8	38	31	23	0	0	7.2	9.5
Small signal transistor	37	32	21	10	0	0	4.3	8.8
MOSFET	6	44	28	22	0	0	7.0	8.0
Power, bipolar	15	31	39	15	0	0	6.4	7.5
INTEGRATED CIRCUITS, DIGITAL								
Advanced CMOS	0	50	33	17	0	0	6.8	9.3
CMOS	10	38	38	14	0	0	6.4	8.7
TTL	21	42	16	21	0	0	5.8	5.7
LS	19	48	19	14	0	0	5.2	5.9
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	8	42	33	17	0	0	6.5	8.9
OP amplifier	17	33	22	28	0	0	7.1	7.8
Voltage regulator	11	42	26	21	0	0	6.6	6.8
MEMORY CIRCUITS								
RAM 16k	0	46	27	27	0	0	7.8	7.3
RAM 64k	0	47	27	26	0	0	7.7	7.7
RAM 256k	0	20	47	33	0	0	9.5	10.0
RAM 1M-bit	0	20	30	40	10	0	11.8	11.1
ROM/PROM	9	36	18	37	0	0	8.2	8.7
EPROM 64k	0	36	43	21	0	0	7.8	8.5
EPROM 256k	0	36	36	28	0	0	8.4	9.7
EPROM 1M-bit	0	22	45	33	0	0	9.4	13.5
EEPROM 16k	0	40	30	30	0	0	8.3	9.4
EEPROM 64k	0	36	37	27	0	0	8.3	9.6
DISPLAYS								
Panel meters	8	38	46	8	0	0	6.0	7.2
Fluorescent	0	12	38	50	0	0	11.1	13.0
Incandescent	0	33	34	33	0	0	8.8	8.9
LED	18	32	41	9	0	0	5.6	6.8
Liquid crystal	0	10	40	50	0	0	11.3	9.8
MICROPROCESSOR ICs								
8-bit	28	27	18	27	0	0	6.5	7.8
16-bit	8	50	17	25	0	0	6.7	9.1
32-bit	8	42	25	25	0	0	7.1	8.9
FUNCTION PACKAGES								
Amplifier	0	50	38	12	0	0	6.4	10.2
Converter, analog to digital	0	31	46	23	0	0	8.2	9.8
Converter, digital to analog	0	43	29	28	0	0	8.0	10.7
LINE FILTERS	0	63	12	25	0	0	6.8	7.6
CAPACITORS								
Ceramic monolithic	21	32	37	10	0	0	5.5	6.3
Ceramic disc	26	30	29	15	0	0	5.6	6.5
Film	9	45	32	14	0	0	6.0	7.5
Aluminum electrolytic	12	42	27	19	0	0	6.4	7.2
Tantalum	15	41	29	15	0	0	5.9	7.1
INDUCTORS	0	44	31	25	0	0	7.7	7.6

Source: *Electronics Purchasing* magazine's survey of buyers

There are many AC sources available today... but only 3H offers the

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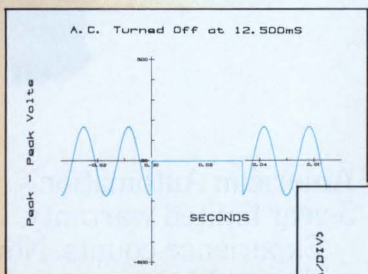
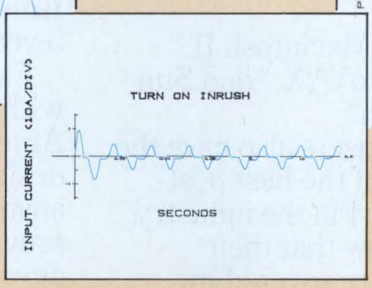
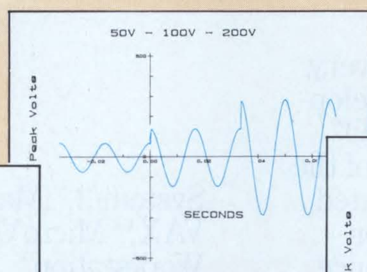


Power break with programmable control of phase and duration

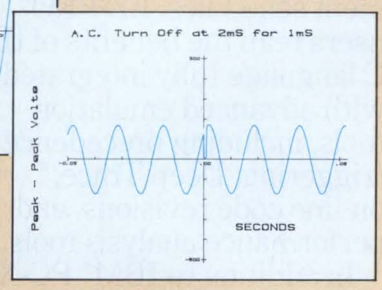


Up to 100A of peak inrush current in a single unit

Instantaneous application of programmed three-wave sequence



Notch removal for testing ride through



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- Full measurement function including rms voltage, rms current, true average power, power factor, positive and negative peak current, and inrush current
- Three pre-programmed waves available for continuous operation
- Programmable instantaneous three-wave amplitude sequencing (for transient applications)
- Programmable current limit
- Programmable Maximum RMS & Peak Current (to protect both the product being tested and the AC source)
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8086	8035	68HC11A2	6801	6301X	6504	1806	Z80H
8088	8039	68HC11A8	6802	6301Y	6505	CDP6805C4	Z180
80186	8344		68B02	6303R	6506	CDP6805C8	Z8001
80188	8048	68000	146805E2	6305V	6507	CDP6805D2	Z8002
80286	8049	68008	6803	63705	6512	CDP6805E3	
	8050	68010	6808	6309	6513	**Harris:** 80C86	**NEC:** V20 V40
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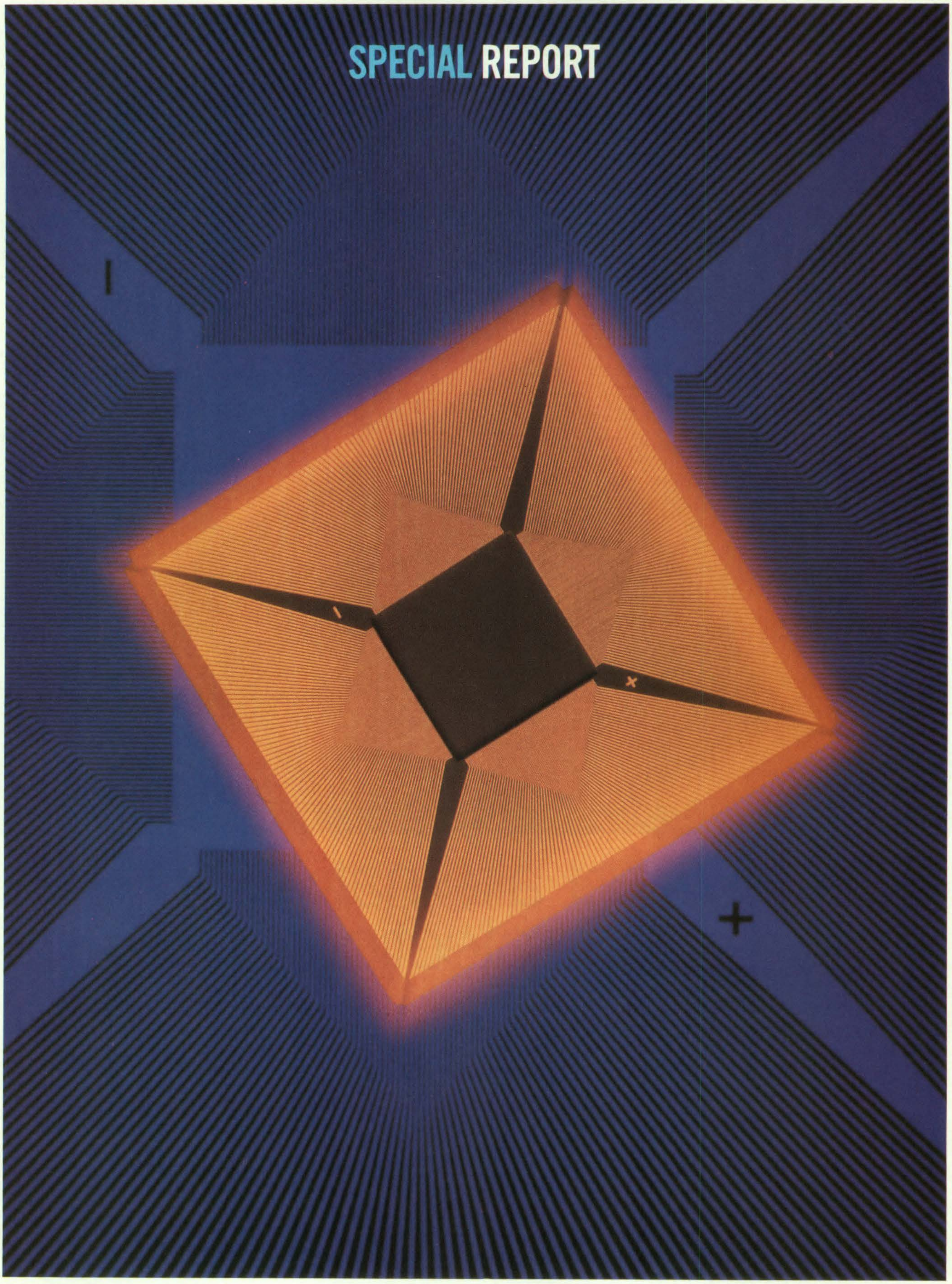
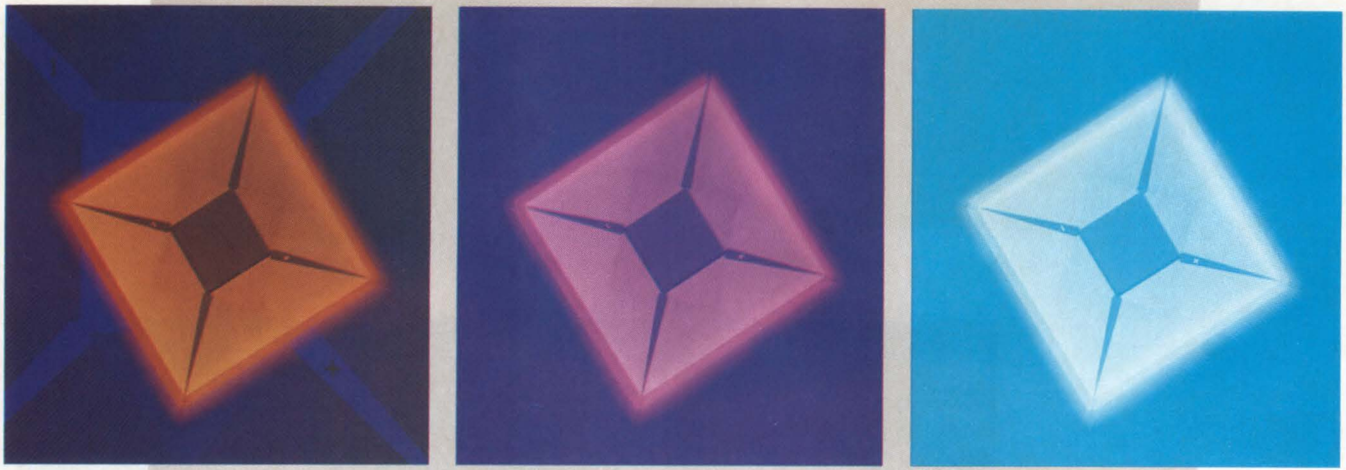


With new processing technologies, *you can realize the high-density packaging required to develop today's electronic systems. (Photo courtesy DuPont)*



MATERIALS AND HARDWARE

Tom Ormond, *Senior Editor*

High density and performance are goals for today's VLSI- and SMT-based designs. Fortunately, advances in materials other than silicon are keeping pace with advances in integrated circuits. Innovative hardware is making it easy to mount, cool, interconnect, and shield VLSI- and SMD-populated assemblies.

VLSI devices are achieving increasingly high levels of performance, and surface-mount technology makes possible significant increases in circuit densities. Equally important, however, are the advances in material and hardware areas. These advances are converting the promises of VLSI and SMT into manufacturable, cost-effective products.

This report will highlight innovations in six nuts-and-bolts areas of system design:

- Fabrication processes, which are yielding improved resistance materials for high-resolution, low-current trimmers, and which are offering improved packaging techniques for microwave circuits (pg 150).
- Wired circuit boards, which can operate at gigahertz frequencies (pg 151).
- Molding technology, which yields not only unique pc-board configurations but also enclosures that you can tailor to your application (pg 152).
- Thermal-management technology, which can help you remove heat from dense, high-performance circuits (pg 154).
- Connectors (both fiber optic and electrically conductive), which are easing the interface to high-density circuits (pg 155).
- Shielding, which can help you ensure electromagnetic compatibility at the enclosure or component level (pg 158).

Designed to efficiently transfer heat from pc-board components, *thermal planes from Aavid are particularly well suited for use in sealed card cages that contain closely spaced boards.*

Although such areas rarely receive their just due when it comes to press coverage, they are critical if you hope to successfully guide your design through the production phase of the product-development cycle.

• Fabrication processes

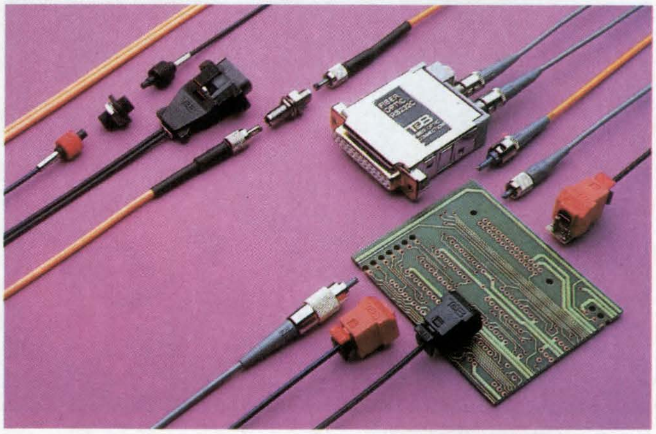
Today's variable-resistance devices (trimmers) typically include wirewound, bulk-metal, or cermet-film resistive elements. Devices from this last category have traditionally served applications requiring high resolution: Cermet-film elements offer essentially infinite resolution. In contrast, wirewound and bulk-metal elements both exhibit step-type resolution characteristics—because of the discrete windings around a mandrel in the former case and, in the latter case, because the photoetching process used to produce bulk-metal elements generally yields a serpentine pattern.

Cermet has exhibited a drawback, however. Oxidation can plague thick-film cermet trimmers when they're exposed to low-microampere (dry-circuit) currents. Cermet is essentially a metal-oxide ink: Dry-circuit current levels cannot break down the oxidation layer (which forms at the junction of the wiper and the resistive element), and as a result, long-term cermet-trimmer stability degrades.

To better adapt cermet to dry-circuit applications, Bourns has developed what it calls Palirium technology, in which islands of precious metal (usually a low-resistance gold compound) are deposited on a thick-film cermet element and cured at high temperatures. A wire wiper makes contact with the metal pads on the cermet resistance element. The wiper, made up of multiple contact points, reduces contact resistance by creating parallel current paths across adjacent islands.

The Bourns Trimpot II HPS trimmers are the first devices to employ this new technology. Their resistance values range from 0.5 to 100 kΩ with a tolerance of $\pm 10\%$, and their resolution ranges from 0.15 to 0.35%. In company tests for contact-resistance variation, which were run at a current level of 5 μA on nominally 2-kΩ elements at 125°C over 2000 hours, drift was less than 0.5%. These results represent a greater than 300%

In applications involving dry-circuit current levels, oxidation layers seriously degrade the long-term stability of conventional cermet trimmers.



***Although simple termination and easy maintenance are key features** of the Pre-Cap fiber-optic connectors from Thomas & Betts, they are also high-performance devices. Their mean insertion loss equals 0.12 dB; the standard loss deviation measures 0.016 dB.*

performance improvement over conventional cermet variable-resistance elements. Indeed, these specs compare favorably to those of the more costly bulk-metal trimmers.

Handling microwave circuit needs

Other advances in film-deposition techniques are benefiting multilayer microwave circuits. DuPont has developed four proprietary technologies—PCM, PCS, LCM, and PPM-β—which it uses to fabricate microwave modules that accommodate surface-mount devices and thick-film resistors. The modules feature ceramic construction. DuPont uses photoforming techniques to provide conductor lines with square edges and smooth surfaces.

PCM (photoformed ceramic module) technology is a copper-based multilayer technology designed to provide excellent conductivity and via geometry. Resolution for lines and spaces equals 2 and 3 mils, respectively, and vias can have 4-mil diameters.

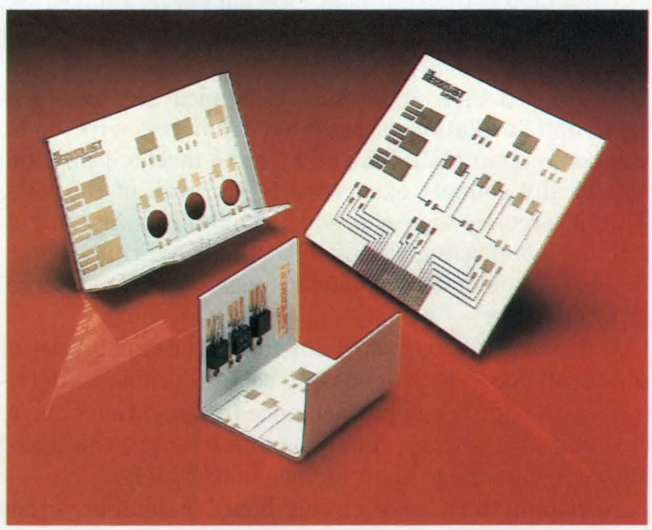
PCS (photoformed ceramic substrate) technology, which is compatible with PCM, provides thin-film accuracy and control without the costs associated with conventional single-layer processes. PCS produces very-fine-line conductor traces using a polymer emulsion that becomes tacky when exposed to light. In the PCS process, the tacky area is toned using a conductor or oxide powder and then fired to set the pattern. PCS resolution approaches or exceeds that of thin-film technology: Resolution for lines and spaces equals 2 mils.

LCM (laminated ceramic module) technology is a low-temperature co-fired ceramic technology that uses a proprietary dielectric film and specially formulated gold, silver, silver/palladium, or copper compositions. The technology provides a cost advantage vs thick-film multilayer schemes, and it outperforms high-temperature co-fired ceramics. LCM technology produces a dense hermetic structure that you can personalize by using existing thick-film or PCM technology.

Finally, the PPM-β (photoformed plastic module) technology, which is compatible with either rigid or flexible circuitry, produces 5-mil lines and 25-mil pads on a variety of substrates (as large as 12×18 in.) with as many as four layers. In the fabrication cycle, a proprietary process plasma-etches a dielectric material to form blind and buried vias. These vias are more tolerant of thermal cycling than plated vias are, so PPM-β technology minimizes the problems that can occur when wave-soldering surface-mounted components. PPM-β's polyimide dielectric offers a low dielectric constant and its bulk copper foil produces high conductivity.

• Wired circuit boards

The increasing number of high-speed designs employing ECL, advanced Schottky logic, high-speed CMOS, and even gallium arsenide are producing new challenges in the areas of circuit density and signal propagation. Kollmorgen Corp's Multiwire Div has developed a discrete wiring technology that offers



***Featuring electrical characteristics that match those of ceramic materials,** Thermal-Clad substrates from Berquist can serve as isolated mounting media for either packaged or unpackaged heat-generating devices. The substrates feature three laminated layers: a base plate (usually copper or aluminum) bonded with an epoxy-based, thermally conductive dielectric to a circuit layer (either copper or aluminum foil).*

Photoforming techniques are beginning to bridge the gap between the accuracy of thin film and the cost advantages of thick film.

solutions to many of the challenges that designers face when striving to realize high-speed circuits.

The Multiwire circuit boards feature a customized pattern of wires (4 or 6 mils) laid down on an adhesive-coated substrate. Polyimide insulation on the wires lets them cross without shorting (and eliminates the need for vias in internal layers), thereby increasing packaging density: A Multiwire board with one or two layers of wiring can readily replace a more expensive multilayer board.

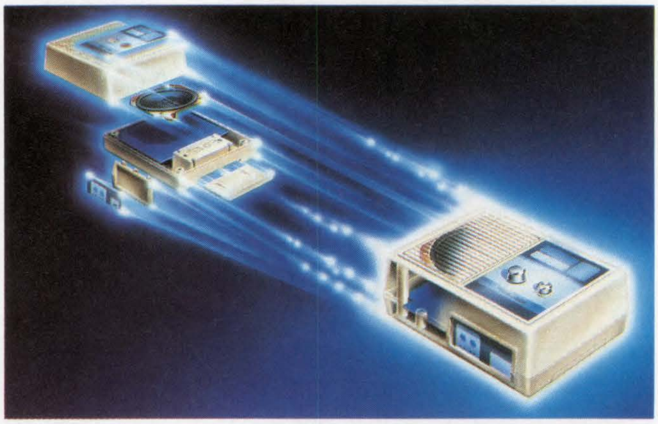
The Multiwire board-fabrication process begins with a standard, copper-clad FR-4 base material. The copper-clad base laminate is then imaged and etched according to a format drawing. The format determines both the ground planes for power distribution and the board's controlled impedance. Adhesive material applied to the board provides a base for the placement of wires. The adhesive insulates the power and ground planes and serves as a foundation for the permanent interconnections.

A computer-driven numerically controlled wiring machine then writes insulated wires in a predetermined, repeatable pattern in accordance with the customer's net list. Each wire begins and ends at a hole location. Next, the wires are pressed into the adhesive and encapsulated by a cover layer of epoxy glass. This process locks every wire securely in place. Holes drilled at each plated-through-hole location serve a dual role, providing a junction for each wire as well as mounting holes for components.

The board then undergoes a chemical cleaning process, and insulation is removed from the wire ends. Copper is then plated in the holes to mechanically and electrically connect each wire to the wall of the hole. This interconnection exceeds IPC and military standards for bond strength and withstands multiple soldering and desoldering without damage to the hole barrel or interconnect.

Multiwire's Coaxe board illustrates the capabilities of the technology. By eliminating several problems detrimental to high-speed performance (propagation delays, crosstalk, reflections, and ground currents), the board allows designers to achieve speeds to 20 GHz.

Although the Coaxe circuit board resembles other Multiwire boards in appearance, its performance at gigahertz frequencies is quite different. Its characteristic impedance is exactly matched to application requirements. Time delay can be reduced to 1.2 nsec/ft. The boards' 2×10^{-4} dissipation factor results in attenuations as low as 4.9 dB/ft at 1 GHz.



The flexibility available with molding techniques *allows Amerex to provide standard enclosures with custom molded options.*

The Coaxe board combines the best features of coaxial cables and the packaging simplicity of pc boards. It features a coaxial wire that's small enough to be built into the board. As a result, it offers true 50Ω coaxial interconnections between circuit components. The 50Ω coaxial lead is embedded in the ground plane; you can specify coaxial wires for every interconnect on the board. Embedding the shielded leads in the ground plane minimizes return currents. The ground plane also serves as a heat sink for mounted chips. The Coaxe board accommodates either through-hole or surface-mounted components.

• Molding technology

Traditional pc boards have one primary mission—to mechanically support and electrically interconnect components on a 2-dimensional surface. Designers have had to use other components and structural elements to connect the pc board to the rest of the system. Now, molded circuit interconnects offer a new approach for packaging electronic components. These interconnects employ injection-molded thermoplastic parts that are selectively metallized. They can incorporate pc boards, connectors, chip carriers, and mechanical and structural elements.

Molded circuit interconnects are made from engineering-grade thermoplastics such as polysulfone, polyethersulfone, polyetherimide, and polyarylsulfone. The characteristics of these resins provide maximum continuous run temperatures as high as 180°C and heat-deflection temperatures to 210°C. Electrical parameters are also impressive: Resistivity is 10^{+10} Ω-cm, and in the gigahertz frequency range the dielectric constant is approximately 2.8.

With permeabilities ranging to 350,000, Bomco's MμShield material is designed for applications in which EMI could be catastrophic to sensitive instruments.

With molded boards, thickness control is far superior to that of epoxy-fiber-glass laminates and is uniform over the entire board surface—tolerances reach ±0.001 in. Molded-in holes are clean and free of drilling debris. Hole diameters can be as small as 0.3 mm (12 mils) with tolerances of ±0.013 mm (±0.5 mil). The molding process places no limit on the form of holes and cutouts.

However, because of the flow characteristics of available resins and the molding pressure required to fill the molds, board sizes are currently limited to about 150 in^2. Moreover, the technology is most economical in high-volume applications (typically, more than 40,000 pieces) where you can amortize the cost of making the mold over the lifetime of the part. In addition, molded circuits are not very forgiving when it comes to engineering changes: Changes in circuit layout, for example, require changes in the mold. Finally, molded circuits are not compatible with multilayer constructions.

Bringing the technology to market

Triquest and Elite Circuits are two companies working together to develop molded circuit boards. Triquest builds the molds and produces the substrate boards; Elite provides the metallization and other finishing procedures.

Another molding-technology company is Pathtek; it is involved in volume production of a molded LED holder and interconnect for an electronic typewriter. The molded device uses the company's Mold-n-Plate process (a 2-shot imaging and selective-metallization system) to form circuit patterns on molded structures. The part aligns four LEDs in a molded holder, which serves as a mounting mechanism. By incorporating 2-sided, plated-through-hole circuitry into the plastic molding, this device replaces a single-sided circuit board and consolidates three components into one package.

Although the molded part and its conventional equivalent function identically, the molded part offers advantages in weight reduction and overall assembly costs. Weight, parts count, and subassembly labor operations for the molded and conventional implementations are 9.9g vs 11.5g, six parts vs eight parts, and three operations vs six operations.

An inside look at today's enclosures

Molding technology doesn't stop with boards. It's also finding application in the enclosure market, where modularity and versatility are key driving forces. A casual observer might miss most of the innovations in enclosure design because many of the advances are quite subtle.

The past few years have seen minimal alterations in basic enclosure design. Portable molded enclosures still come in two basic styles: the 1- or 2-piece clam-shell style, wherein users typically interface through the top surface; and the front/rear panel design, in which interfacing normally takes place through the panel sections. When you look beyond the basic styles, howev-

The high-speed active devices available today pose a number of problems for pc-board designers.

er, you'll find that vendors are offering a variety of enclosure features that are designed to let users more effectively package their products.

One development has been the introduction of specialty enclosures that include battery compartments. More recent innovations, from companies like Amerex, include display-window enclosures, speaker-grill enclosures, and low-profile enclosures. All of these off-the-shelf specialty units incorporate molded-in features that can make your product look like it's enclosed in a custom housing.

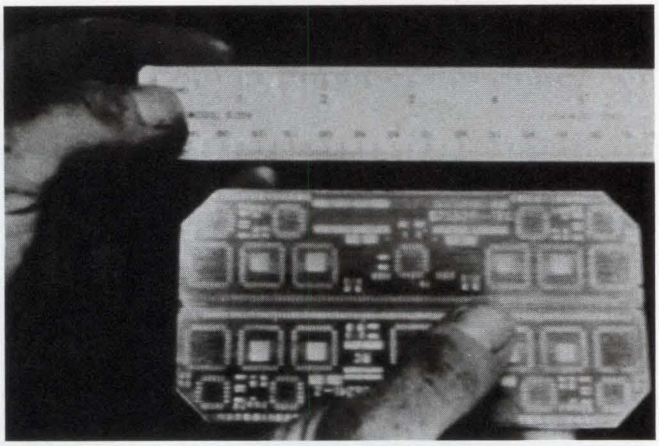
• Thermal management

Board-level thermal management has been a major design consideration for many years. Today, though, designers are striving to cram more and more circuitry into smaller and smaller packages, and the resulting increase in power densities is making effective thermal management even more critical. Indeed, heat dissipation can reach levels that standard pc-board materials cannot handle effectively. Fortunately, vendors of substrate materials are addressing these dissipation problems.

Thermo-Clad substrates from Berquist serve as an isolated mounting medium for either packaged or unpackaged heat-generating devices. The substrates feature three laminated layers: a base plate (usually copper or aluminum) bonded with an epoxy-based, thermally conductive dielectric to a circuit layer (either copper or aluminum foil). This combination provides several important features in demanding surface-mount applications. It has electrical characteristics that match those of ceramic or epoxy-glass materials, but the composite substrate has much better thermal and physical characteristics than either material. Surface resistivity equals 7×10^9 MΩ, and thermal conductivity measures 0.0136 W/cm/°K. In addition, TCE (thermal coefficient of expansion) ranges from 8 to 25 ppm/°C over an operating range of −36 to +100°C.

The dielectric layer holds the key to Thermal-Clad substrate performance. It rapidly transfers heat from the metal etched-circuit layer to the metal base plate while it simultaneously electrically isolates the two layers. The dielectric withstands processing temperatures as high as 400°C and features good breakdown performance—2000V for a 2-mil-thick layer.

The design flexibility of Thermal-Clad substrates is especially useful in die-mounted assemblies. Substrate dimensions can range from less than 1 in^2 to 10×16 in. To satisfy special requirements, Berquist can also alter performance characteristics by thickening a layer or changing layer materials. You can, for example, specify substrates that feature a heavy copper circuit layer to handle high currents and provide better thermal spreading characteristics. You can also request a substrate whose dielectric layer withstands 4000V. In addition, Berquist can provide special base materials to optimize thermal expansion characteristics, for example.



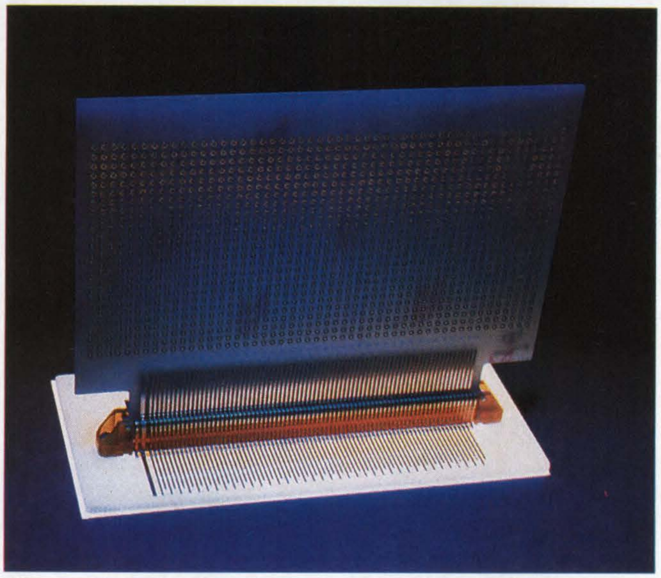
***High density and reliability** are possible with custom, multilayer ceramic substrates from DuPont. The Aegis part, suitable for multichip control boards, permits greater design freedom without sacrificing reliability.*

Aavid Engineering takes a more traditional approach to solving thermal-management problems with its pc-board thermal planes. These planes are designed to efficiently transfer heat from pc-board components to the cold wall of a card cage and are particularly well suited for use in sealed card cages that contain closely spaced boards.

Made of aluminum or copper in thicknesses from 0.02 to 0.1 in., the thermal planes are fabricated on numerically controlled equipment to achieve maximum hole-to-hole layout density. It's possible, for example, to achieve 0.09-in. holes on 0.1-in. centers—a pattern that's particularly useful for chip carriers, for which heat dissipation from central pins can often be a problem.

The thermal planes are available with a number of different finishes. Aluminum planes can be black-anodized or finished with gold chromate. Copper planes are available with tin or nickel electroplating, black oxide, or a special high-emissivity dielectric coating that also has high thermal conductivity.

In addition to the basic thermal planes, Aavid also offers prepregnated sheets that let you bond the thermal planes to the pc board. The planes are also available



Based on a design employing shape-memory alloys, *these impedance-matched, high-density connectors from Beta Phase offer a combination of zero insertion force and high contact force. In addition, you can actuate the devices electrically.*

with epoxy-lined through holes to provide electrical insulation. The planes work with pc boards that have all kinds of through-hole components—ICs, transistors, resistors, diodes, rectifiers, and bridges.

The thermal planes add rigidity to the board and help to resist shock and vibration. Aavid provides complete design support for custom thermal-plane products. Using CAD equipment to analyze your board's thermal characteristics, the company can provide a plane that is optimum for an individual application.

• Connectors

Manufacturers of electrical connectors are offering devices with contact spacings in the millimeter range to help you get signals into and out of high-density boards. Fiber-optic-connector manufacturers are offering devices that are easy to terminate but that don't sacrifice performance. In addition, some manufacturers are taking a systems approach to product design and development.

Molex is one connector manufacturer that's emphasizing the systems approach. To reduce customers' costs, Molex is currently using robots to interconnect connectors to pc-board headers, to insert single-in-line modules into its SIMM sockets, and to insert daughter boards into edge connectors.

Increasing circuit densities are driving the trend toward metric center-to-center pin spacings. Although the incremental difference between connectors with 1.25-mm and 0.050-in. contact spacings might seem trivial (the standard 0.050-in. center-to-center connector requires about one mil more space per position than the 1.25-mm connector does), the space savings can be significant for a 30- or 40-position connector.

Molex has developed a 1.25-mm board-to-board hinged connector—a 2-piece system with a mated height and width of 10.3×6.7 mm. Aside from helping designers maximize circuit-board density, the connector facilitates pc-board maintenance by allowing you to easily access the board surface. The connector mates on the coplanar (or board-edge to board-edge) axis, allowing you to rotate the board by as much as 90°. The connector also mates in the reverse direction to accommodate boards that are mounted in parallel.

The connector is basically designed for use on pc boards that house components requiring adjustments (potentiometers or trimmer capacitors) as the boards pass down an assembly line. The hinged connector uses a reliable, high-pressure tuning-fork-type contact system. The connectors feature plated phosphor bronze contact terminals. Solder tails are arranged in a staggered pattern to simplify the soldering process and to improve the connector's mechanical stability. Kinks in the solder tails keep the connectors properly positioned during soldering.

Mating and rotation lifetimes for these hinged connectors are 30 and 50 cycles, respectively. The connectors are available in 4- to 20-position sizes (even numbers only). The polyester housings have a 94V-0 UL flammability rating. Contacts are rated for 125V at 1A.

Pre-Cap Series connectors from Thomas & Betts are compatible with SMA, ST, and FC fiber-optic-connector designs. Although simple termination and easy maintenance are key features of the connectors, they are high-performance devices nevertheless. Mean insertion loss equals 0.12 dB, and standard loss deviation measures 0.016 dB.

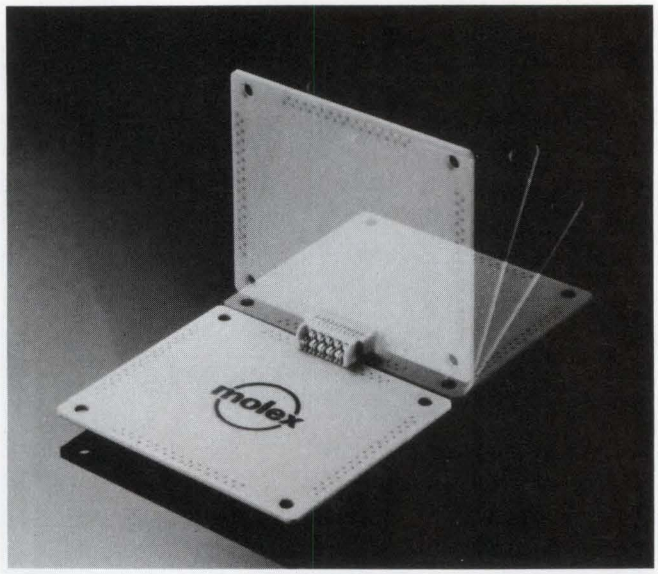
The connectors consist of a precision injection-molded ferrule assembly, a bayonet-type nut, a compression spring, and a retaining coupler ring. The ferrule is keyed and spring-loaded into the coupler to provide repeatable connector performance. The ferrule features a borosilicate-glass capillary, a zinc die-casted insert, and an injection-molded, self-reinforced thermotropic liquid-crystal polymer. The capillary measures 1×10 mm, has a 128-μm-diameter center hole (with a +1/−0-μm tolerance), and features a beveled entry on one end to ease fiber insertion. The connector manufac-

Molded circuits offer designers an easy way to upgrade the packing density of a pc board.

turing process positions the capillary and the zinc insert within the molding die; the polymer is then injected to form the finished ferrule assembly.

Connector installation is quite simple. After preparing the cable's end, you simply place a small amount of medium-viscosity epoxy on the fiber and buffer and inject a low-viscosity epoxy into the ferrule. You then insert the fiber into the connector body and hold the cable in place by crimping the cable strength members. Next, you apply epoxy to the cavity of the strain-relief boot and then slide the boot onto the connector. After the epoxy cures, you scribe and break the fiber and then polish the interface.

The polishing operation produces a mirror-like finish on the fiber and the glass capillary. The polishing process removes only glass (rather than glass and ceramic, as is typical of many other connector-polishing operations), so there's no need to constantly monitor for fiber wear. The result is shorter termination time. Moreover, it's almost impossible to overpolish the ferrule tip.



Featuring a 1.25-mm contact-to-contact spacing, *these hinged connectors from Molex use a high-pressure tuning-fork-type contact system and a polyester housing that has a 94V-0 flammability rating.*

A connector that never forgets

Miracle wire and wonder wire are just a few of the names given to a group of alloys whose potential for commercial applications is yet to be realized. Known as shape-memory alloys (SMAs), these metals have a physical structure that, through the application of heat, can be unlocked, rearranged, and programmed to take on new shapes. Forces exerted during the reshaping transition can be tremendous—as much as 50,000 psi.

Although SMAs were introduced more than 20 years ago, their inherent advantages were not fully exploited because of fabrication difficulties: The metals often popped back into their original shape during the manufacturing process, breaking equipment. In addition, batch-to-batch consistency was poor. In the last few years, however, manufacturers have overcome these problems, making it possible to economically realize the commercial potential of the metals.

About 20 alloys have shape-memory properties, but only a few—copper zinc aluminum, copper zinc nickel, and nickel titanium—are practical for commercial applications. The nickel titanium alloys are the most promising because they offer the best overall performance characteristics. They have twice the memory and are far more resistant to corrosion and cracking than are other SMAs, and they are lightweight and nearly as elastic as rubber (depending on the nickel titanium combination).

Beta Phase offers a line of pc-board connectors that use this nickel titanium alloy. These connectors offer a combination of impedance-matched, high-density contacts, zero insertion force (ZIF), and high contact force. They allow you to make ZIF connections on three edges of a pc board. In addition, you can remotely or locally actuate the devices electrically—there's no need to physically access the connector. The connector can also function as a card guide and stiffener, providing good mechanical support for the board.

The connector consists of three basic parts—a shape-memory element, a closing spring, and flexible-film circuitry that includes the contact pattern and a built-in heater. When you trigger the heater, the shape-memory element moves toward its original flat shape, engaging and opening the contact-closing spring. After inserting the board, you remove power from the heater. The shape-memory element closes, engaging the contacts with high normal forces—100g/contact in a typical connector. The polyimide-film flexible circuitry meets military standards.

Beta Phase's connectors offer a number of features. The use of flexible circuitry allows for 0.01-in. contact-trace spacings, and it's also possible to mix trace widths and center spacings to accommodate signal, power, and grounding needs. The connectors are also compatible with surface-mount applications. Because plastic molded bodies are not required for strength or support, each connector's profile, size, and weight are low. The use of shape-memory alloys also makes it easy to tailor

Board-level thermal management has been a prime design consideration for many years, and SMT is increasing its importance.

the connectors for specific applications. For an application involving −55 to +125°C operation, for example, the connector would employ an alloy that triggers above 125°C.

• Shielding

Given the complexity of today's electronic circuitry, electromagnetic compatibility is a critical design consideration. EMI and RFI can propagate along a conducting medium or radiate through space. In either case, the electromagnetic energy can cause undesirable interference and degrade the operation of a receiving system.

The FCC has established limitations on radiated and conducted interference levels for all computer and peripheral devices according to the class of product. Class A devices include those found in commercial, industrial, or business applications. FCC Docket No 20780 states that, depending on frequency, emanations from a Class A device shall not exceed specific field-strength levels at 30 meters. Over frequency ranges of 30 to 88, 88 to 216, and 216 to 1000 MHz, the field-strength limitations are 30, 50, and 70 μV/m, respectively.

Although the FCC specifies maximum permissible interference levels from a system, the commission does not tell enclosure manufacturers or system designers how to reduce emissions, and a battle is raging over how best to minimize radiation problems. Some see metal enclosures as the ideal solution for reducing EMI/RFI problems, though manufacturers of molded plastic enclosures contend that their products can provide acceptable electromagnetic compatibility.

The ideal EMI/RFI enclosure is a box (of metal or conductively coated plastic) without any seams or openings. Realistically, an effective cabinet is one that approaches these ideal qualities and provides access to internal components. The seams around all access points are crucial for maintaining good EMI/RFI integrity. The mating surfaces of all seams must be electrically connected, so you must use gaskets that feature high surface conductivity as well as good shielding properties. If different conductive materials are involved, they must be galvanically compatible to prevent a buildup of corrosion that can degrade gasket performance.

Instrument Specialties offers an extensive line of beryllium copper shielding strips for gasketing enclosure seams and openings. Beryllium copper does not absorb moisture or support fungus growth, and it isn't bothered by severe weather. It has excellent thermal

For more information . . .

For more information on the material and hardware products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

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Product introductions indicate that connector manufacturers are striving to help designers cope with production problems.

and electrical conductivity properties; it does not set under compression; and it is not affected by ozone, ultraviolet or nuclear radiation, EMP, or solvents.

The company's latest introduction is the Snap-tite clip-on shielding strip. The strips feature high holding power coupled with high electrical conductivity. They are well suited for high-vibration applications or situations where the available spring pressure cannot keep a gasket mounted securely. D-shaped lances clip into predrilled or prepunched holes, locking the gasket in place. Because Snap-tite gaskets require no friction for adherence, they are compatible with any type of surface. The strips come with various corrosion-resistant and high-conductivity plated finishes in standard or custom lengths.

Rather than implementing shielding yourself, you can buy enclosures that are already shielded. Manufacturers of plastic molded enclosures currently use two methods to control EMI/RFI. Most offer enclosures that are shielded with a conductive paint, a technique that's quite effective. Depending on the quantity of product involved, however, it can be an expensive solution. Amerex uses a second approach to shield its Unibox line of plastic enclosures. The company employs a family of die-cut Mylar and foil-laminated inserts, which slip into standard enclosures. These board shields are available in small quantities, and you can easily modify them to fit specific applications.

Conductive plastic materials hold great promise for shielding, but currently available materials cannot meet the cosmetic requirements of many applications. Material manufacturers are making progress in this area, however.

Meanwhile, Emcor has a line of metal enclosures that provide a good combination of shielding and accessibility. Designed to both contain and exclude radiated interference by reflecting and absorbing incident electromagnetic radiation, the enclosures feature a cabinet frame with 14-gauge, 1.75-in.-wide multiformed corner channels that are fully welded.

These frames support a static load of more than 3500 lbs without failing or permanently deflecting. The rugged construction is necessary to obtain and maintain the close-tolerance access openings required for proper EMI/RFI gasket sealing. The frames, along with all optional bolt-on components, are zinc-plated per MIL SPEC QQ-Z-325, Type II, Class 3. A highly conductive, galvanically compatible wire-mesh gasket, in combination with the optional components, provides EMI/RFI shielding around all openings.

The enclosures come in different styles and sizes. Both vertical and slope-front frames are available in 19- and 24-in. widths with depths of 25⅝ and 31⁹⁄₁₆ in. The vertical frames come in 40 sizes, each in five different configurations. The slope-front units are available in eight sizes, each in four configurations. All emission-control side panels are removable from the inside and flush-mount within the frame's side channels. Top and closure panels are constructed of 16-gauge, cold-rolled steel. All can accommodate adhesive-backed, foam-wire-mesh gasketing.

Shielding at the board level

You don't have to wait until you get to the enclosure level to address magnetic interference problems. Bomco's MμShield material can prevent interference problems at the component level by diverting magnetic flux around sensitive circuitry. MμShield's permeability figures range from 200 to 350,000 (relative to the free-space permeability rating of 1).

Shielding applications fall into two categories: those where the shield must prevent fields from radiating, and those where the shield serves to prevent magnetic-field penetration. Bomco stocks three general types of MμShield material—high permeability, medium permeability, and high saturation—each of which can handle either application category.

High-permeability MμShield material has a minimum permeability of 80,000. Maximum permeability equals 350,000, and the saturation point is approximately 7500 gauss after treatment. Medium MμShield material is normally used in conjunction with high-permeability material. It has a permeability of 12,500 to 150,000 with a saturation point of approximately 15,500 gauss. Permeability for high-saturation material ranges from 200 to 50,000 with saturation points of 18,000 to 21,000 gauss.

Bomco heat-treats all MμShield material during manufacturing to ensure maximum permeability and low shock sensitivity. Should your shielding needs ever change, you can return the MμShield product for special heat treating. In addition, if you'd prefer to design your own shields, Bomco provides MμShield material in coil, sheet, and tubing form. **EDN**

Article Interest Quotient (Circle One)
High 485 Medium 486 Low 487

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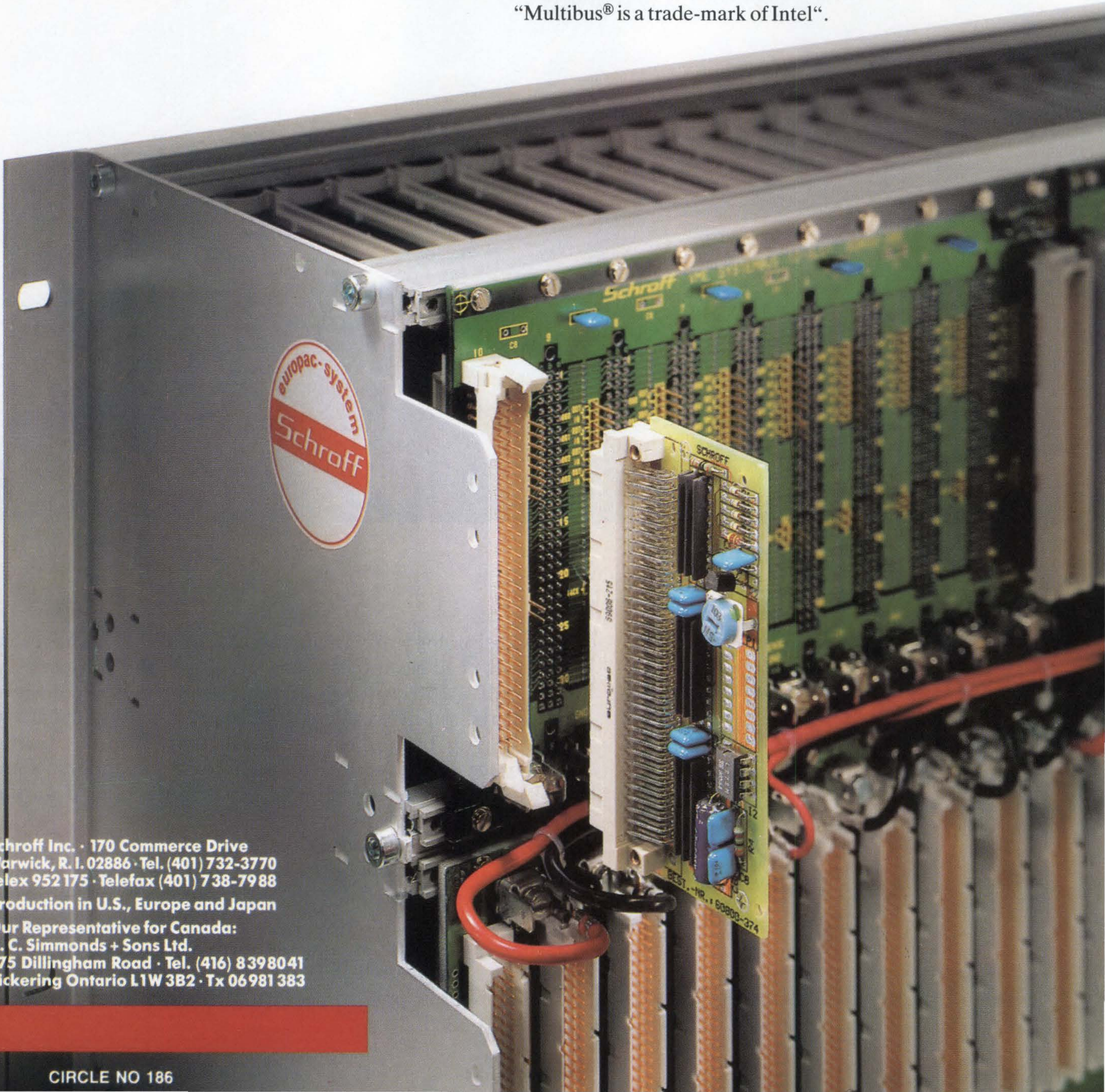

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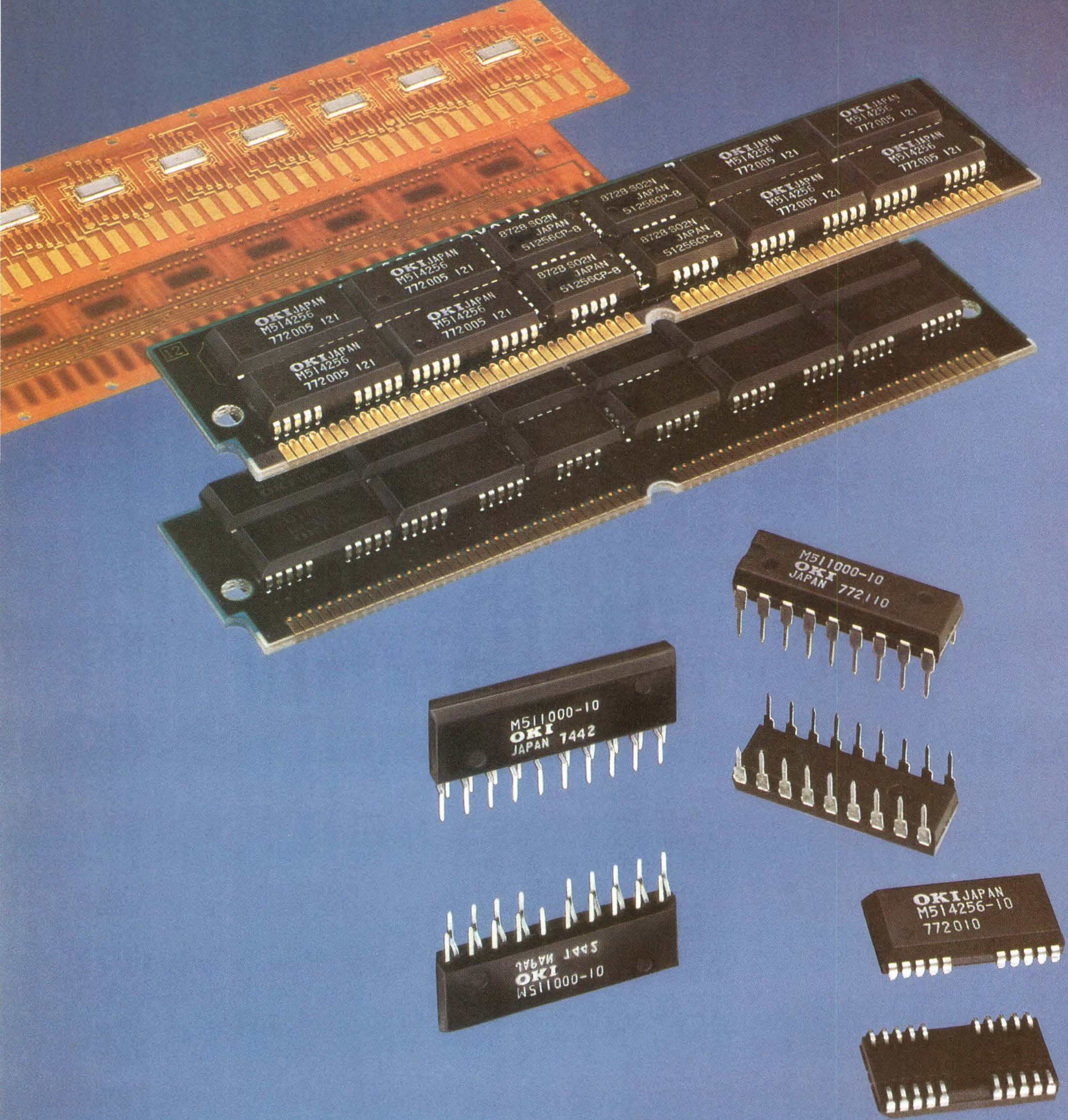

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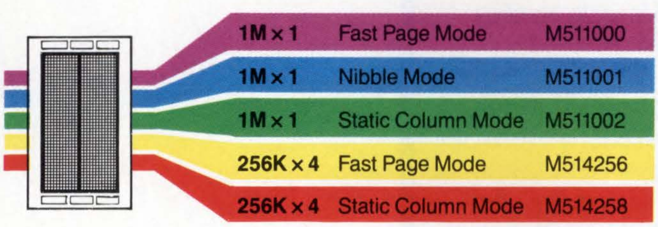

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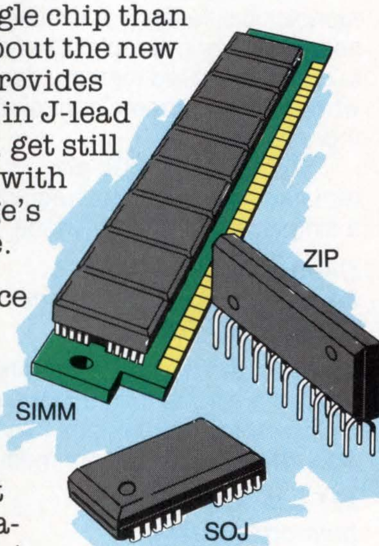

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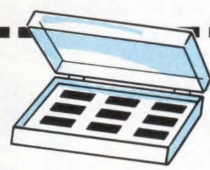

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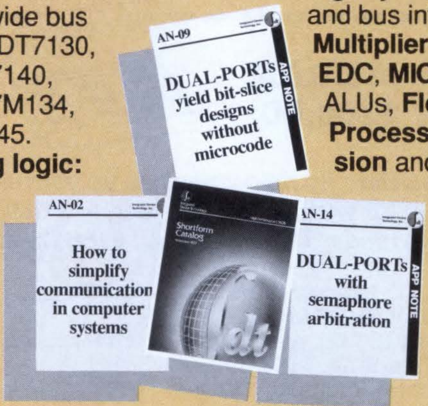

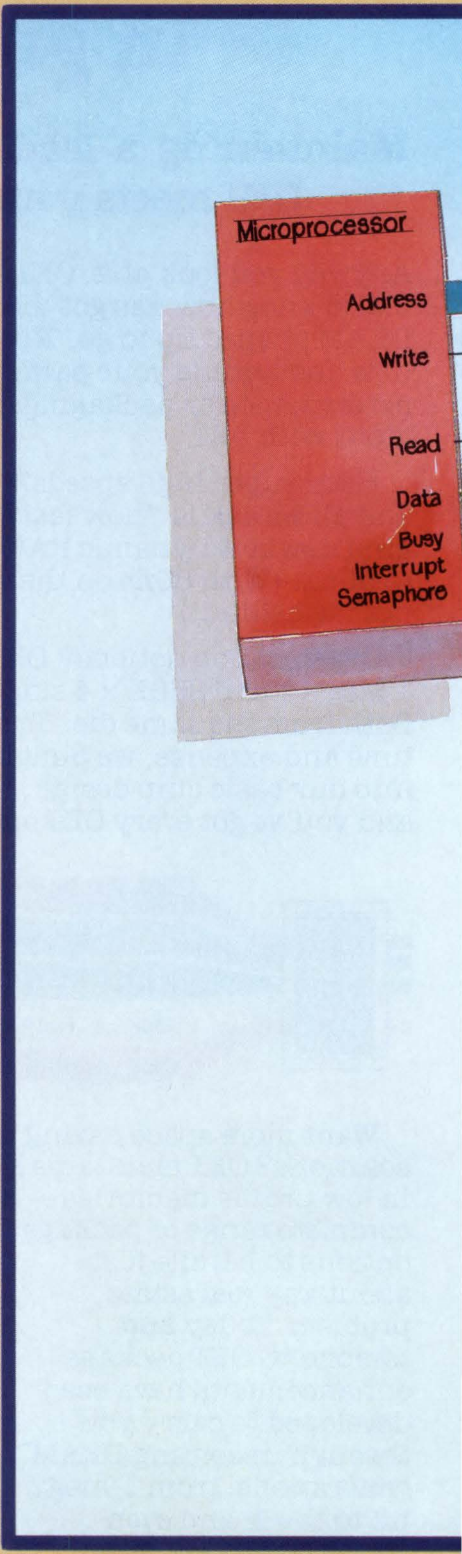

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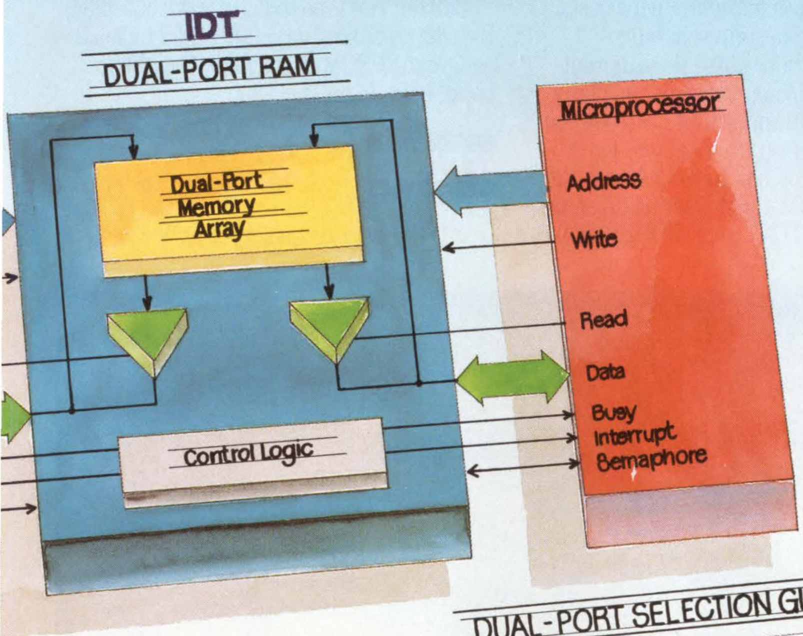
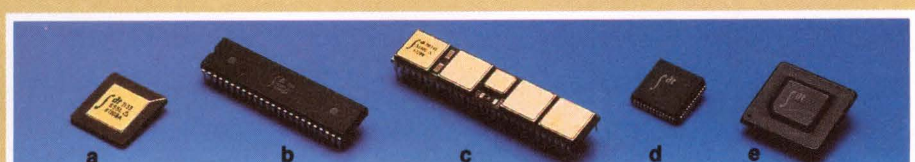


DUAL-PORT SELECTION GUIDE

Description	Part Number	Access Time	Expandability	Control Logic: Interrupt	Control Logic: Busy Logic		Control Logic: Semaphores
1Kx8	IDT 7130	35 ns	✓	x	MASTER		
"	IDT 7140	35 ns	✓	x		SLAVE	
2Kx8	IDT 7132	35 ns	✓		MASTER		
"	IDT 7142	35 ns	✓			SLAVE	
"	IDT 71321	35 ns	✓	x	MASTER		
"	IDT 71421	35 ns	✓	x		SLAVE	
"	IDT 71322	45 ns	✓				x
2Kx16	IDT 7133	55 ns	✓		MASTER		
"	IDT 7143	55 ns	✓			SLAVE	
4Kx8	IDT 7134	45 ns	✓				
"	IDT 71342	45 ns	✓				x
8Kx8 Module	IDT 7M134	50 ns	✓		MASTER		
"	IDT 7M144	50 ns	✓			SLAVE	
16Kx8 Module	IDT 7M135	50 ns	✓		MASTER		
"	IDT 7M145	50 ns	✓			SLAVE	
32Kx8 Module	IDT 7M137	60 ns	✓				

(a) Hermetic LCC
(b) Plastic and hermetic DIP
(c) Standard and custom modules
(d) Plastic PLCC
(e) Plastic and hermetic PGA



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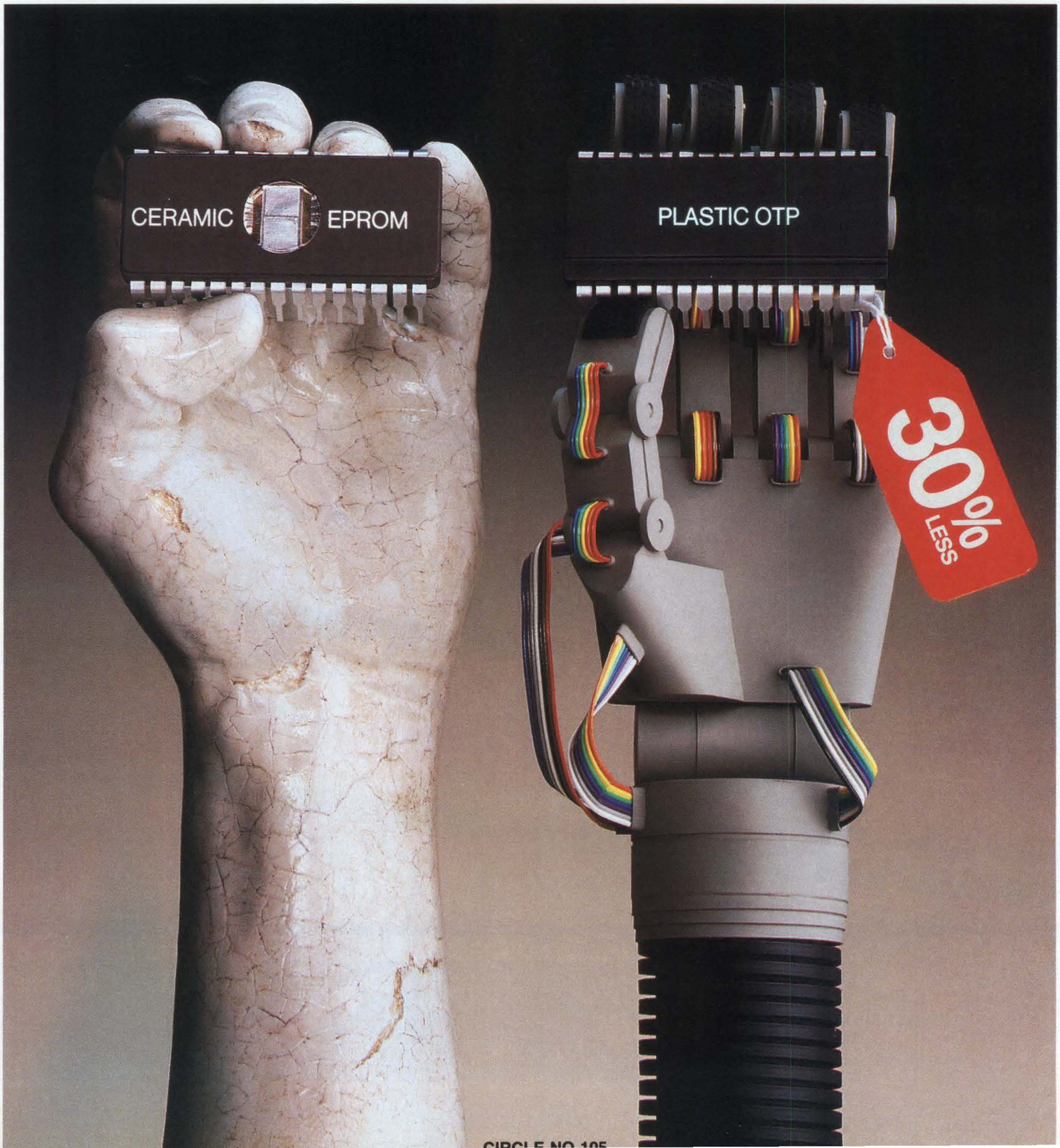

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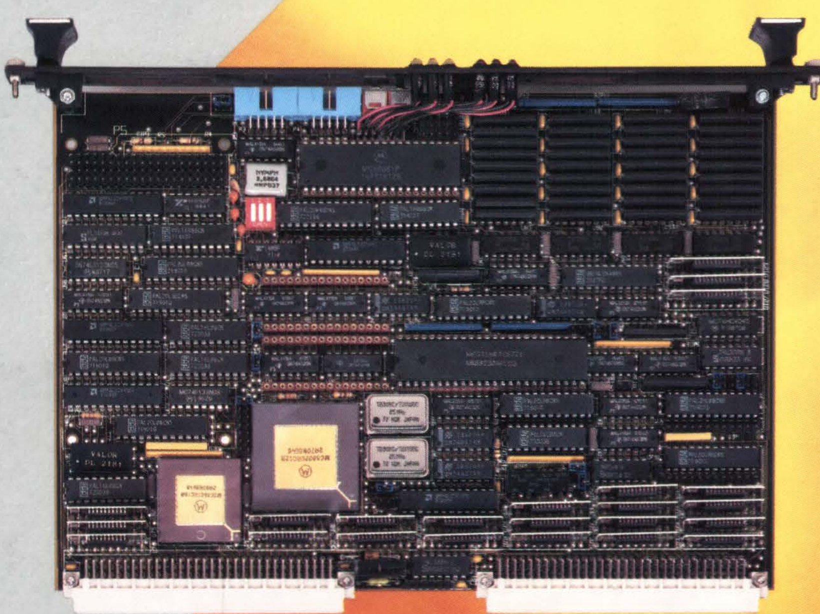

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In addition to its modular I/O, the OB68K/VSBC20 comes standard with 2 RS232C async serial ports and a 16-bit parallel port. The OMNIMODULE and on board serial I/O is brought out to your choice of front panel or P2 connector. On board parallel I/O is brought out to the P2 connector only.

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CIRCLE NO. 119

Programmable array serves as a controller for dynamic RAMs

Large memory systems that use dynamic RAMs often have varying requirements for control. A programmable gate array can offer the flexibility to meet the needs of various memory-system applications. In addition to integrating refresh circuitry, it contains sufficient logic to allow you to implement error detection and correction.

Thomas Waugh, *Xilinx Inc*

To produce cost-effective products with large amounts of memory, designers often prefer to use low-cost, high-density dynamic RAMs instead of the comparatively more expensive and less dense static RAMs. However, dynamic RAMs require control circuitry that static RAMs don't. To implement that circuitry in a single chip, you can use a programmable gate array. Such a device can provide refresh signals (the capacitor that makes up each dynamic memory cell must be recharged, or refreshed, typically once every two to four milliseconds), and it can provide the error detection and correction that can alleviate the headaches that the dynamic RAMs' susceptibility to soft errors can cause (see **box,** "Soft errors can cause hard problems").

You'll find several options available to you for dynamic-RAM controller designs. The simplest option is an off-the-shelf standard LSI memory controller. The manufacturers of these parts combine μP interface logic with memory-access and memory-refresh circuitry on one chip. However, each memory system has unique timing and protocol requirements, so standard parts can't accommodate every system. Even though some manufacturers include some degree of programmability in their parts, designers must often employ glue logic, in the form of extra SSI or MSI packages, to meet system requirements.

Custom gate arrays provide a highly integrated solution. However, nonrecurring engineering costs, testing and simulation costs, inventory risk, and the long design cycle make the custom gate array unattractive for many designs.

The Logic Cell Array (LCA) device can overcome some of these difficulties. Its programmability gives the designer freedom to tailor the dynamic-RAM controller to the exact specifications of a memory system without external glue logic (see **box,** "LCA devices offer flexibility"). You can configure the LCAs to meet unique system requirements without the loss in integration posed by the SSI/MSI solution and without the costs and risks associated with the custom gate-array solution.

The 2000-gate XC3020 LCA device is well suited for designing a dynamic-RAM controller. Not only does a single XC3020 incorporate dynamic-RAM control functions and error detection and correction, but the CMOS device also consumes less power than standard programmable controllers, which are typically imple-

A nuisance associated with dynamic RAMs is their susceptibility to soft errors.

mented in NMOS or bipolar technologies.

Consider a design example based on an 8-MHz 8086 μP that directly addresses 1M bytes of memory made up of 32 256k-bit dynamic-RAM chips. A single LCA serves both as a dynamic-RAM controller and an error checker/corrector (ECC). The dynamic-RAM controller uses a 16-MHz clock synchronized to the μP's clock and resides between the 8086 μP (along with its 8288 bus controller) and the system memory **(Fig 1)**. Two '245-type octal bus transceivers determine the communication direction (that is, whether the 8086 will read from or write to the dynamic RAM). The 8288 bus controller supervises the transceivers and can isolate the μP from the dynamic-RAM data bus by placing the transceivers

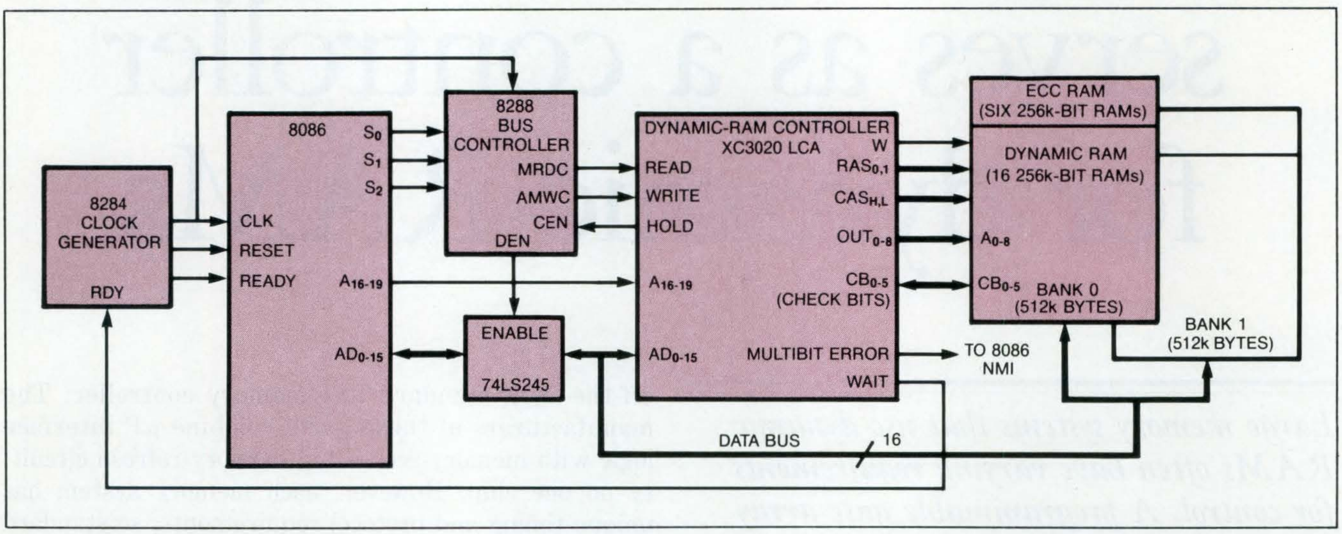

***Fig 1—The 2000 logic gates** in an XC3020 allow it to incorporate control and error-correction and -detection circuitry for an 8086-based system.*

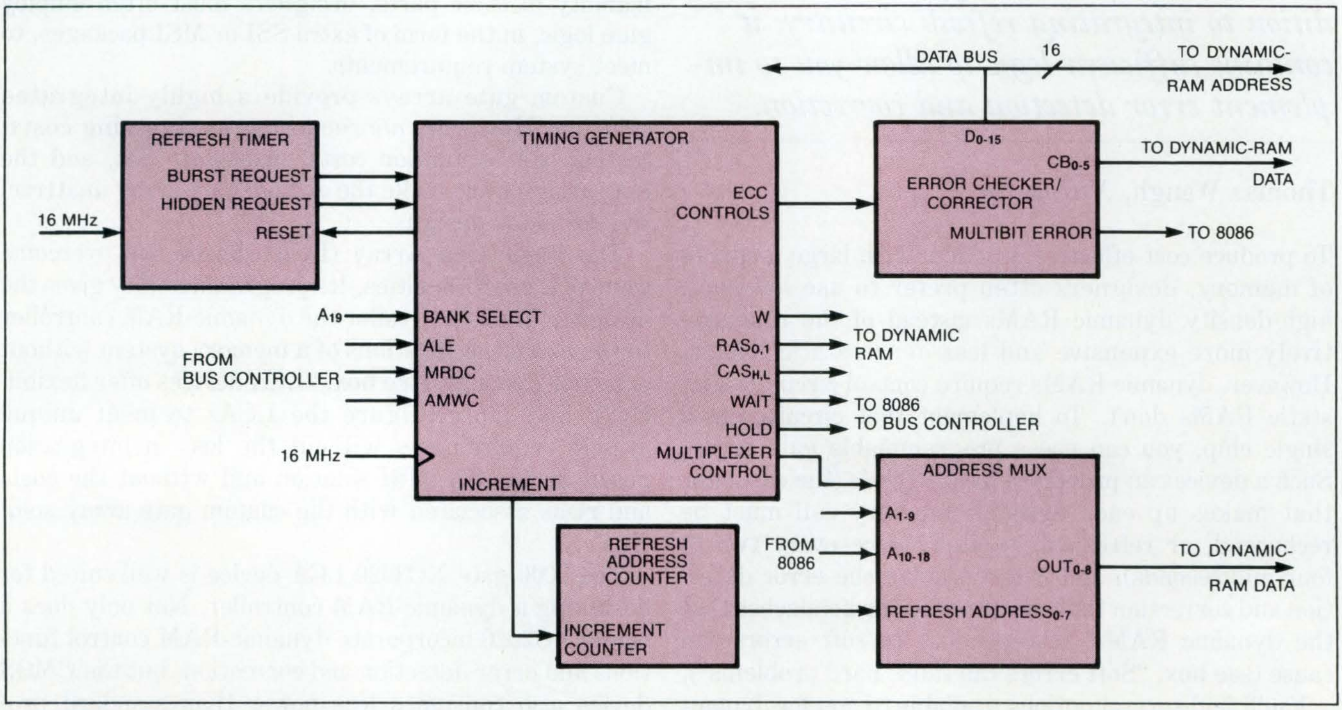

***Fig 2—You can view the dynamic-RAM controller** as consisting of the five basic blocks shown here.*

in a high-impedance condition via the enable (EN) command.

The 8288 bus controller also decodes the µP status lines (S_2, S_1, and S_0) and informs the dynamic-RAM controller whether it should perform a read or write operation. The dynamic-RAM controller then performs the appropriate operation, issuing a row-access strobe (RAS), a column-access strobe (CAS), and a write (W) signal, if necessary. The controller generates error-correction bits on each write operation, and it checks and corrects errors on each read operation. The controller also informs the µP if a memory access requires a wait state or if the controller has detected an error that it can't correct.

Fig 2 is a block diagram of the dynamic-RAM controller and error checker/corrector that reside in the LCA. The refresh timer uses a 16-MHz clock to furnish a signal that informs the dynamic-RAM controller when to refresh the memory. Each of the 256 rows of memory in this system needs refreshing every 4 msec. The refreshing technique employed provides a combination of hidden and burst refreshes. The controller refreshes eight rows every 125 µsec, which corresponds to 4 msec÷125 µsec=32 sets of eight refreshes during the

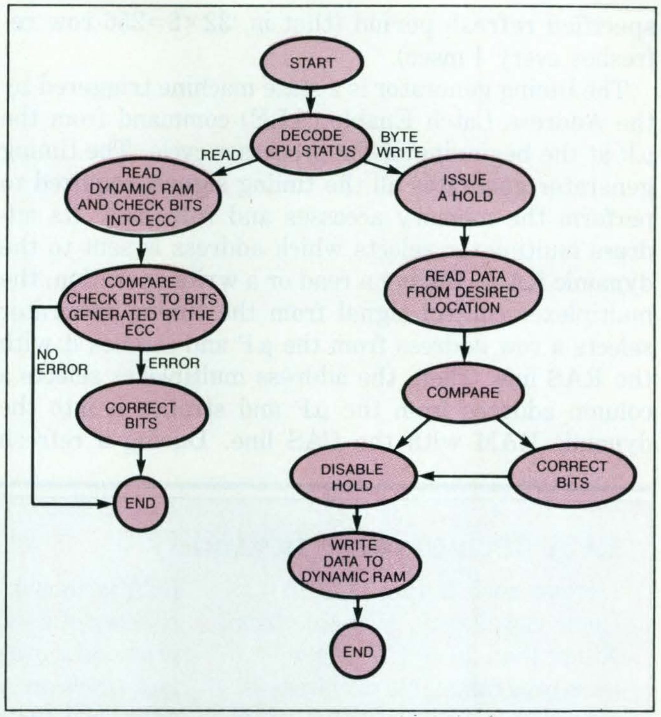

Fig 3—The modified Hamming code *that the error checker/detector in **Fig 2** uses conforms to this state diagram.*

Soft errors can cause hard problems

Dynamic RAMs are much more susceptible to soft errors than static RAMs are. A soft error is the loss of data in a memory cell that is not permanently damaged. Rewriting the data in the cell corrects the error. This type of error is different from a hard error, which results when a memory cell is permanently damaged.

Usually alpha particles (helium nuclei) cause soft errors in dynamic RAMs. Alpha particles are normally present in the atmosphere, but the ones responsible for most soft errors are emitted by radioactive impurities in the IC package of the dynamic RAMs themselves. If an alpha particle hits a memory cell, it can corrupt the cell's charge, causing a data-bit error.

Many people are under the impression that the likelihood of such an error is so slight that it can be safely ignored. Although this belief might have been true for the smaller memory systems of the past, it is no longer so. The size of memory systems today makes soft errors unacceptably likely.

A typical error rate for NMOS dynamic RAMs is about 0.12% per 1000 hours, which translates to an MTBF (mean time between failures) of 1000 hours/0.0012=833,333 hours, or a little over 95 years. However, this spec is for only one RAM chip. The original IBM PC had 64k bytes of RAM, comprising thirty-six 16k-bit dynamic RAMs. The MTBF of such a memory is about 833,333 hours/36 dynamic RAMs=23,148 hours, or just over 2½ years. This value is still probably acceptable. However, the 16M-byte memories in common use today comprise 512 25k-byte dynamic RAMs and have an MTBF of less than 10 weeks. This value is too low for many applications. Device and packaging improvements can reduce the probability of a soft error. However, the most effective means of minimizing such errors is to incorporate error detection and correction into the dynamic-RAM controller.

During a write cycle, the ECC circuitry generates six check bits, using a modified Hamming code, for a 16-bit data word.

specified refresh period (that is, 32×8=256 row refreshes every 4 msec).

The timing generator is a state machine triggered by the Address Latch Enable (ALE) command from the μP at the beginning of the processor cycle. The timing generator generates all the timing signals required to perform the memory accesses and refreshes. Its address multiplexer selects which address is sent to the dynamic RAM. During a read or a write operation, the multiplexer control signal from the timing generator selects a row address from the μP and strobes it with the RAS line. Then, the address multiplexer selects a column address from the μP and strobes it into the dynamic RAM with the CAS line. During a refresh operation, a refresh address counter generates an 8-bit address, which is selected by the address multiplexer. The RAS line strobes the refresh address into the dynamic RAM.

During a write cycle the ECC circuitry generates six check bits, using a modified Hamming code, for a 16-bit data word. The standard Hamming code requires five bits to provide single-bit error detection and correction. The added sixth bit (which is used for a parity check of the data and five check bits) allows the modified Hamming code to provide single-bit error correction and double-bit error detection. **Fig 3** shows a state diagram for the ECC circuit.

During a read cycle, the ECC circuitry generates a

LCA devices offer flexibility

Devices such as the XC3020 Logic Cell Array, available from Xilinx (San Jose, CA), have user-programmable architectures, and consist of three types of configurable elements on a chip: a perimeter of I/O blocks (IOBs), a core array of configurable logic blocks (CLBs), and resources for interconnection.

The general structure of an LCA is shown in **Fig A.** The perimeter of configurable IOBs provides a programmable interface between the internal logic array and the device package's pins. The array of CLBs performs user-specified logic functions. The interconnect resources—which are analogous to pc-board traces—carry logic signals among the blocks.

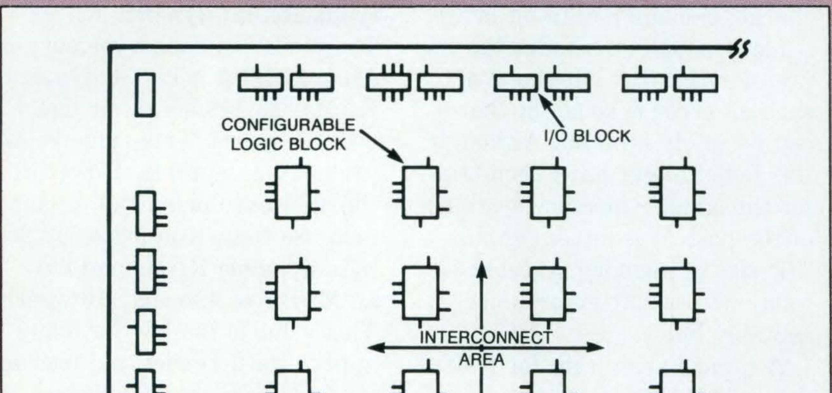

***Fig A—An LCA device** consists of an array of interconnected logic blocks surrounded on the periphery by I/O blocks.*

A configuration program stored in internal static memory cells determines the user-defined logic functions and interconnections. The program is loaded when the power is turned on or when a program mode is enabled. The program data resides externally in an EEPROM, EPROM, ROM, or on a floppy or hard disk. The configuration is determined by an XACT development system, which operates in an IBM PC/AT or compatible with 640k bytes of internal RAM, 1.5M bytes of extended memory, color graphics, a mouse, and DOS 3.0 or higher. The development system provides interactive design and editing along with logic and timing simulation.

The XC3020 has 2000 usable gates for logic functions. The internal static memory has a capacity for as many as 14,815 data bits, which control 64 configurable logic blocks and 58 I/O blocks. In addition, 3-state internal buses facilitate wide wire-AND functions.

new set of check bits from the data that's read from memory. The ECC circuitry compares these check bits with the check bits that were stored in memory to see if an error has occurred. If the comparison yields a correctable error, the ECC circuitry corrects it. When it detects a noncorrectable double-bit error, the ECC circuitry flags the μP.

Memory cycles' timing requirements vary

The timing requirements for different memory cycles are shown in **Fig 4. Fig 4a** shows a memory cycle that requires that a word be written to memory with no wait states. After asserting a row and column address and strobing the dynamic RAM with the respective RAS and CAS lines, the controller asserts the W line to write the 16-bit data word and the six generated check bits to the dynamic RAM.

A memory cycle that requires that a single byte be written to memory is more complicated **(Fig 4b).** First, the controller must read the word resident in the desired memory location and check it for errors. Then the controller inserts the new byte into the appropriate byte of the word. The ECC circuit generates a new set of check bits, and the newly formed combination of word and check bits is written to memory when the controller asserts the W line. This operation involves inserting two wait states and isolating the controller from the μP data bus to perform the read from memory. The controller issues a Hold command to the 8288 bus controller, which disables the '245 transceiver to isolate the controller from the data bus. **Fig 5** shows a state diagram for the Hold and Wait logic circuitry.

Memory cycles that require a read from memory are shown in **Fig 4c** and **Fig 4d.** A read operation requires a minimum of one wait state—the penalty for implementing error correction and detection. The insertion of a wait state is unavoidable because of the time required to detect an error. If the ECC circuitry detects an error, two wait states must be inserted to allow time to correct the error. The corrected data along with the check bits are written back into memory when the controller asserts the W line.

A hidden refresh can occur when the μP is reading from or writing to some device other than memory, such as an I/O port. The address multiplexer selects a refresh address from the refresh address counter and applies it to the dynamic RAM. The timing generator issues an RAS command to execute the refresh.

A burst refresh **(Fig 4e)** occurs only if the refresh timer indicates that the required eight refreshes have

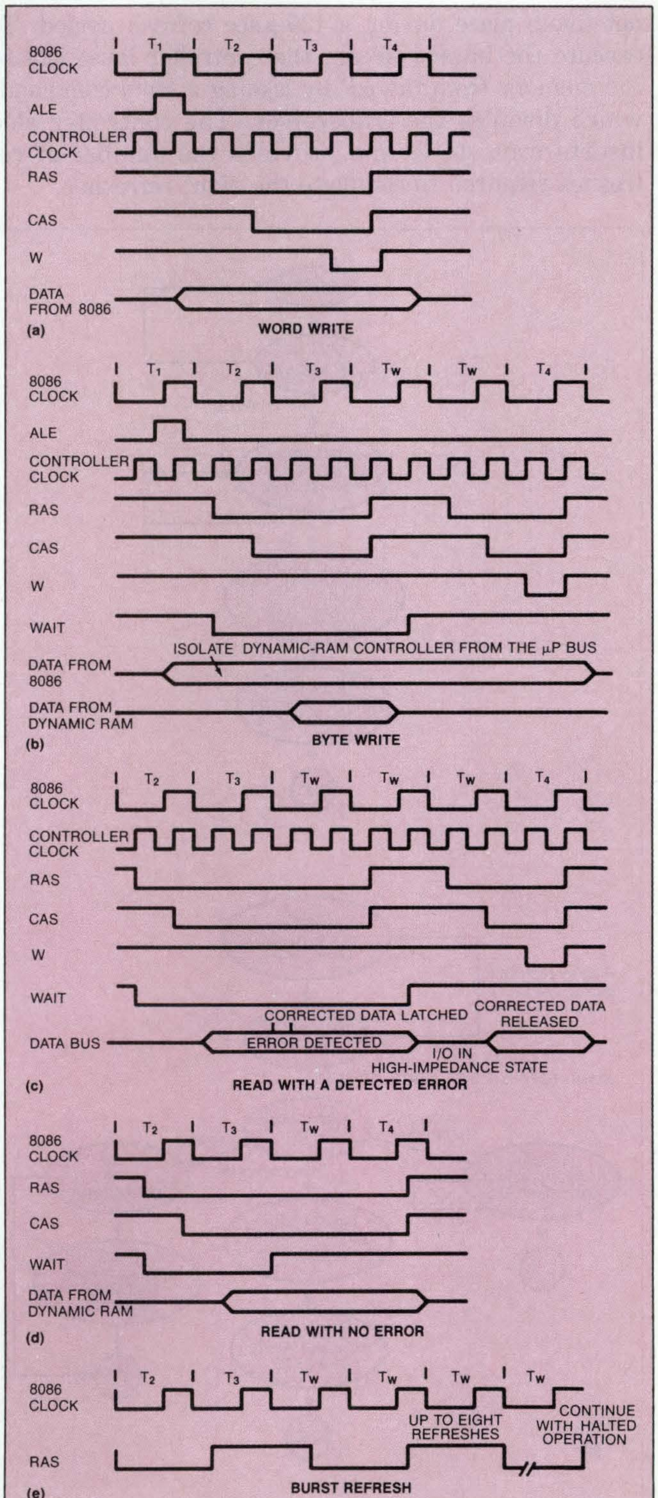

Fig 4—When performing the various read, write, or refresh *operations, the controller's logic circuitry must provide the appropriate timing.*

The dynamic-RAM controller takes advantage of the internal buses on the LCA.

not taken place during a 125-μsec refresh period. To execute the burst refresh, the controller must isolate the memory from the μP by issuing a Hold command, which disables the transceiver. The controller also inserts wait states and provides the number of refreshes required to complete the eight refreshes.

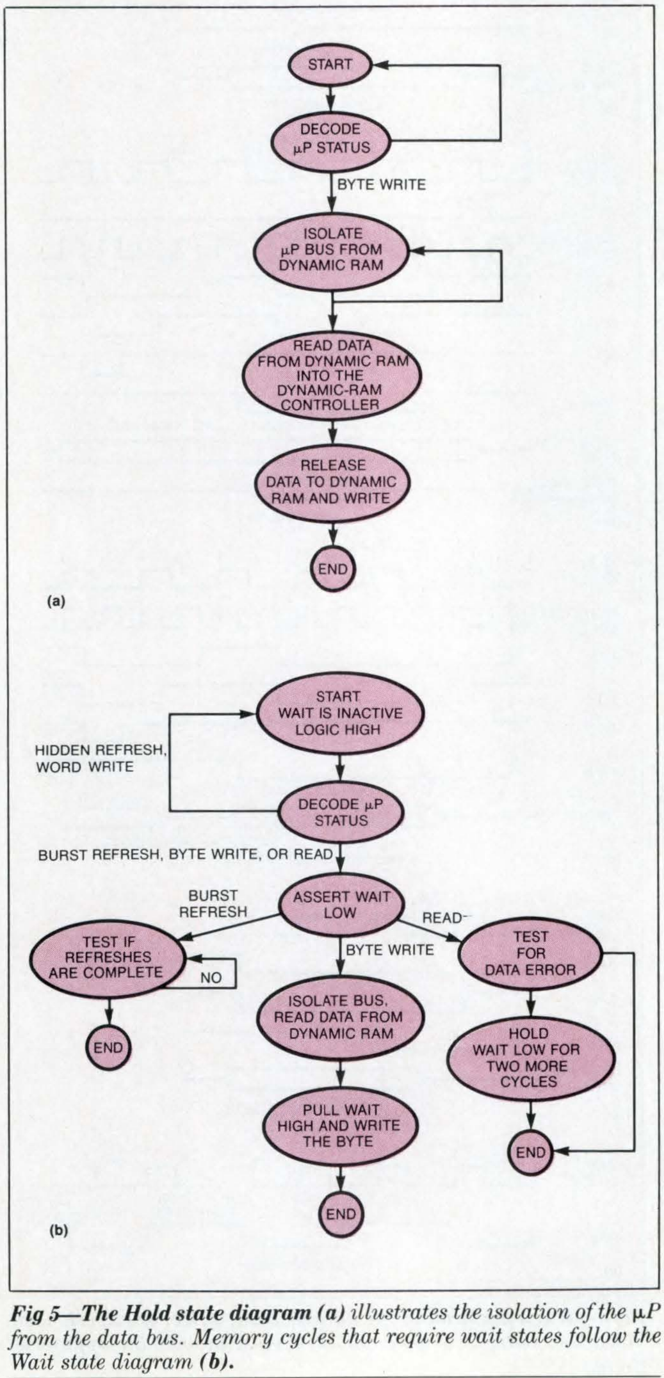

Fig 5—The Hold state diagram (a) *illustrates the isolation of the μP from the data bus. Memory cycles that require wait states follow the Wait state diagram **(b)**.*

Some features of the 3000 family LCA architecture aid the design of the dynamic-RAM controller. **Fig 6** shows a bit-sliced view of one of the address and data IOBs (input/output blocks) located inside the LCA. The IOB provides two paths to the CLBs (configurable logic blocks) on the chip. One is direct and the other is through a storage element, which you can configure as an edge-sensitive flip-flop or as a level-sensitive transparent latch. This circuit arrangement lets you latch addresses and data on a multiplexed bus, such as that used by an 8086 μP, into the LCA device. The ALE command from the 8086 latches the addresses into the dynamic-RAM controller. Data from the μP enters the same input pin and goes directly to the ECC circuit through the IOB's direct path. No external latches are necessary.

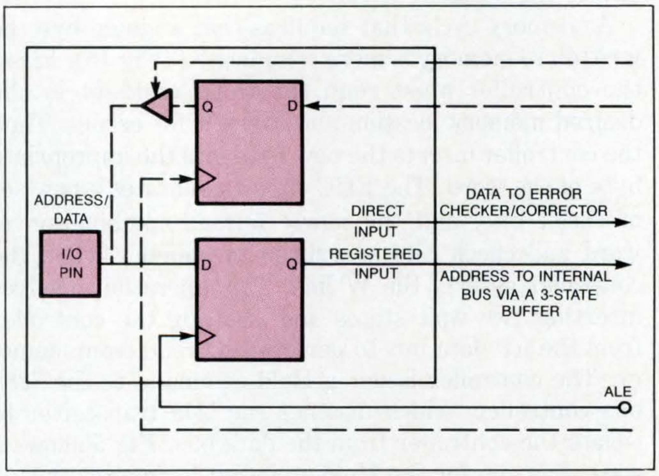

Fig 6—Data at an I/O pin *on the XC3020 can be either latched into the device or passed directly to a CLB.*

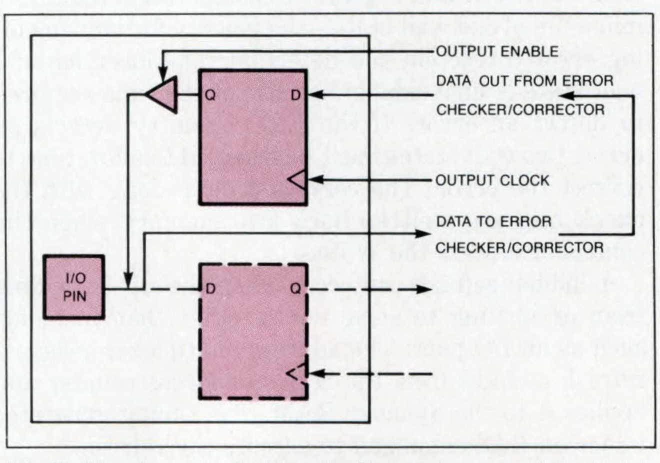

Fig 7—The dynamic-RAM controller *makes use of the 3-state buffers placed on the XC3020's output registers.*

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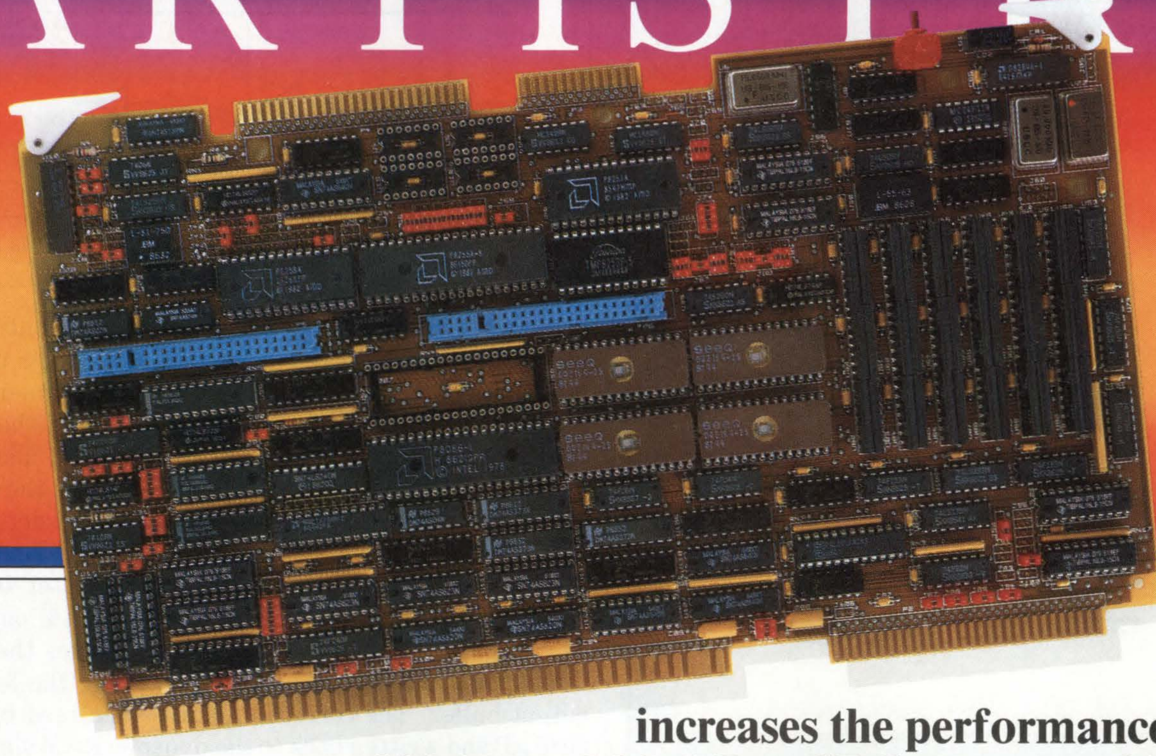

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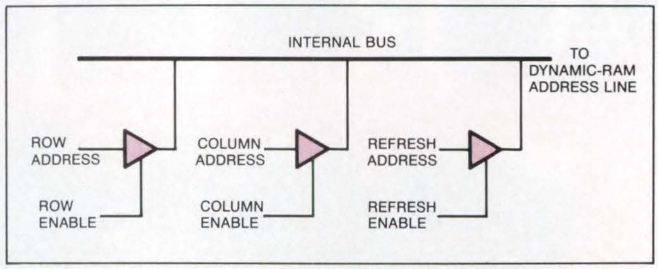
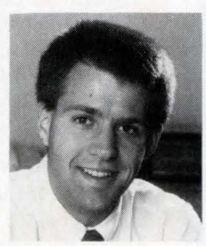


Fig 8—The 3-state drivers attached to the internal bus on the XC3020 allow the multiplexing of addresses onto one line.

The ECC circuit in the dynamic-RAM controller utilizes the 3-state buffer placed on the outputs of the output register of an IOB **(Fig 7)**. During a memory-read cycle, for example, the controller puts the IOB output in a high-impedance condition, thereby allowing dynamic-RAM data on the data bus to enter the ECC circuit via the direct input path. If the ECC detects a data-bit error, it will correct the error and latch the corrected data word into the output register of the IOBs. The controller forces the dynamic-RAM outputs to a high-impedance condition and releases the corrected data onto the data bus by enabling the 3-state output buffer. The corrected data is then read by the 8086 μP and written back to the dynamic RAM simultaneously.

The dynamic-RAM controller also takes advantage of the internal buses on the LCA device. Because the drivers to the horizontal bus can be placed in high-impedance conditions, all of the row addresses, column addresses, and refresh addresses are multiplexed onto the same bus **(Fig 8)**. The dynamic RAMs have access to this bus when the data is latched into the output registers of the IOBs. Enabling the correct 3-state bus drivers forces the proper sequence of addresses. **EDN**

Author's biography



Thomas Waugh is an applications engineer with Xilinx Inc (San Jose, CA). His duties include application design and technical support. He previously worked at Johns Hopkins University's Applied Physics Lab. He received a BSEE degree from Stanford University and is a member of the IEEE. In his spare time he enjoys reading, swimming, and traveling.

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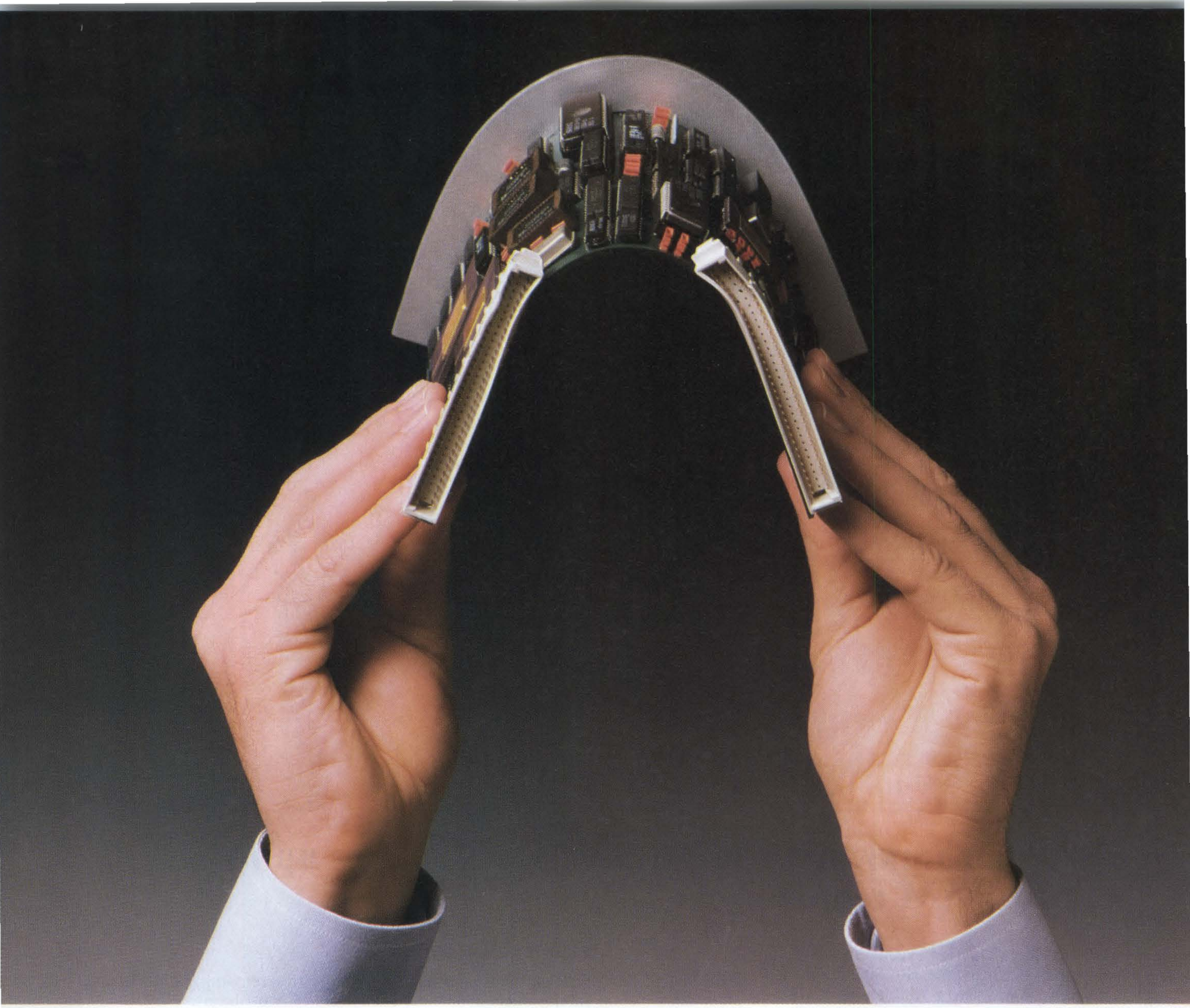

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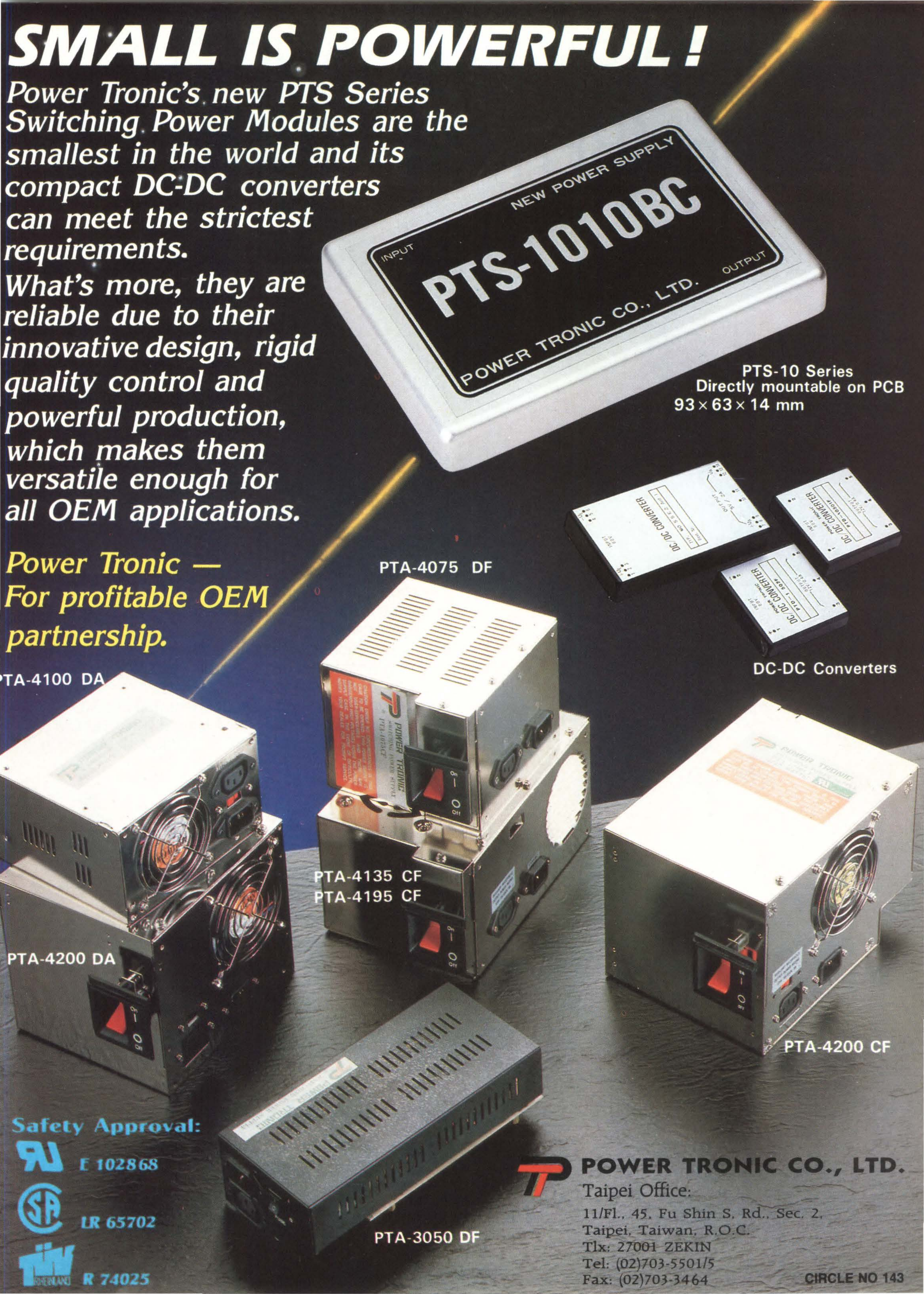
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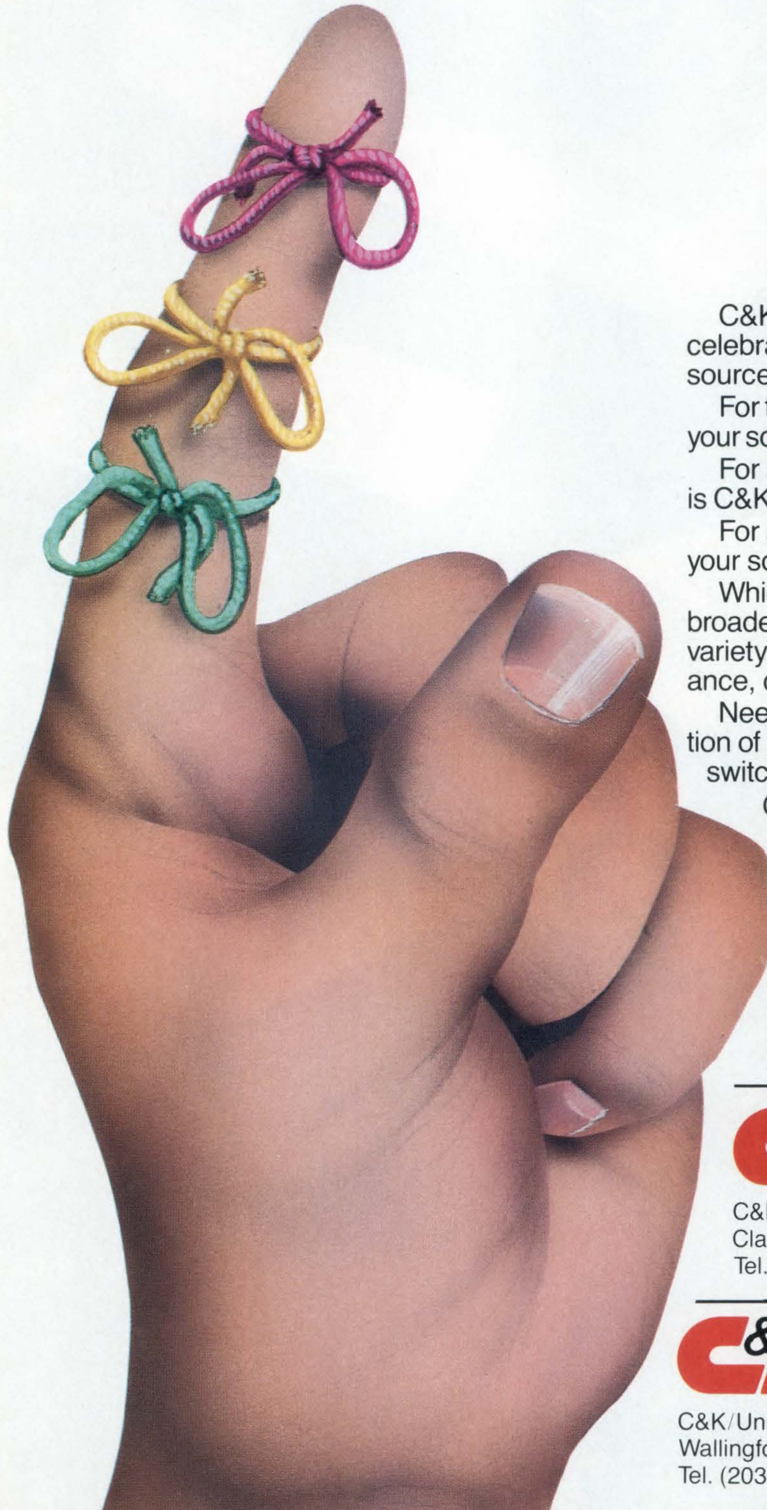

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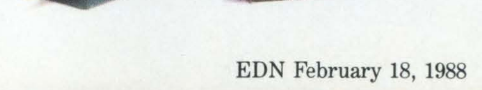

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Selection criteria assist in choice of optimum reference

It's not always easy to select the most suitable precision voltage reference for your application. These devices often require parametric and economic tradeoffs. Further, parameters that are crucial in some systems are missing from or presented unclearly in many data sheets. An overview of selection criteria can help you make the choice.

Ron Knapp, *Maxim Integrated Products*

In choosing a precision voltage reference, you should look beyond initial accuracy, temperature coefficient (TC), and cost. Other factors that determine the suitability of a reference for your application are the device's power dissipation, noise, long-term stability, package size, ease of use, TC linearity, and the manufacturer's definition of TC. Familiarity with these selection criteria will help you avoid unpleasant surprises when you characterize your prototype system.

Before going into the details of the various selection factors, it's useful to briefly review the different types of references available and to explain the principles of operation of each type. The overview will give you some insight concerning the performance you can expect from the various references. Reference circuits comprise three categories: bandgap cells, zener-diode-based references, and heated-substrate types. Most voltage references fall into the first two categories and derive their fixed output from a bandgap cell or a zener diode. The third type of reference obtains additional stability by mounting the bandgap or zener circuit on a heated substrate.

Bandgap references depend on the behavior of diodes (or the equivalent base-emitter junctions of transistors). The following equation predicts the operation of such junctions with a high degree of precision.

$$V_{BE} = V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{T}{T_0}\right) + \frac{nkT}{q}\ln\left(\frac{T_0}{T}\right) + \frac{kT}{q}\ln\left(\frac{I_C}{I_{C0}}\right),$$

where

- V_{G0}=the extrapolated bandgap voltage (about 1.2V) at 0°K
- n=process-dependent constant; value 1.5 to 3
- q=charge of an electron
- k=Boltzmann's constant
- T=temperature in °K
- I_C=collector current
- T_0=reference temperature for V_{BE0} and I_{C0}
- I_{C0}=reverse saturation current at T_0
- V_{BE0}=V_{BE} value for the conditions T_0 and I_{C0}.

The diode's temperature coefficient is large but predictable and repeatable (−2 mV/°C or −3100 ppm/°C). Thus, you can achieve stability by balancing the diode's

The V_{BE} equation's third and fourth nonlinear terms limit the performance of bandgap references by making a flat voltage/temperature response impossible.

TC with a TC of equal magnitude and opposite sign. Such a TC exists for the *difference* between the forward voltages of two diode junctions operating at different current densities. Because the ratio of mismatch governs the TC's value, the bandgap circuit is compatible with good IC design—parameter values should depend on accurate ratios based on layout geometry, rather than on absolute quantities that are difficult to control.

You can calculate the desired difference voltage (ΔV_{BE}) with high predictability, directly from the diode equation

$$\Delta V_{BE} = \frac{kT}{q} \ln\left(\frac{J_1}{J_2}\right),$$

where J_1/J_2 is the ratio of current densities. To obtain zero TC, you add the expression for V_{BE} to the one for ΔV_{BE}, differentiate the sum with respect to temperature (T), and set this quantity equal to zero. The result is

$$V_{G0} = V_{BE0} + \frac{kT}{q} \ln\left(\frac{J_1}{J_2}\right).$$

Solving this equation for the J_1/J_2 ratio tells you that an approximate 8:1 ratio gives the best result (a near zero TC). Scaling the transistor areas gives an IC designer accurate control of this ratio.

In a basic bandgap circuit **(Fig 1)**, V_{BE} is the base-emitter voltage of Q_1, and ΔV_{BE} appears across R_2. The ratio of R_1 and R_2 scale ΔV_{BE} to a voltage (V_1) whose TC cancels the TC of V_{BE}. The amplifier then raises the 1.2V sum of V_1 and V_{BE} (the bandgap-cell voltage) to a higher level at V_{OUT}: usually 2.5 to 10V. Unfortunately, the amplifier multiplies noise as well. A 10V scaled output, for example, increases the bandgap cell's noise voltage by an approximate factor of 8 (10÷1.2).

Commonly available bandgap-reference voltages are 10, 5, 2.5V, and the bandgap-cell voltage itself, 1.23V. Typical TCs range from 5 to 50 ppm/°C. The V_{BE} equation's higher-order, logarithmic third and fourth terms limit the performance of these references by making a flat voltage-temperature response impossible. What's more, some of the equation's coefficients are process-dependent—particularly n, which is related to the carrier mobility of dopant in the silicon. The quantity n poses a problem because you cannot easily determine its value by making electrical measurements during production.

Because most bandgap references are constructed in silicon monolithic form, they are relatively inexpensive ($3 to $20). Many designs employ curvature correction to compensate for the logarithmic nonlinearity in the TC, but none offer an exact cancellation.

Zeners have rock-bottom TCs

The second type of voltage reference—based on a zener diode—achieves TCs as low as ±1 ppm/°C. Zener diodes have a positive or negative TC, depending pri-

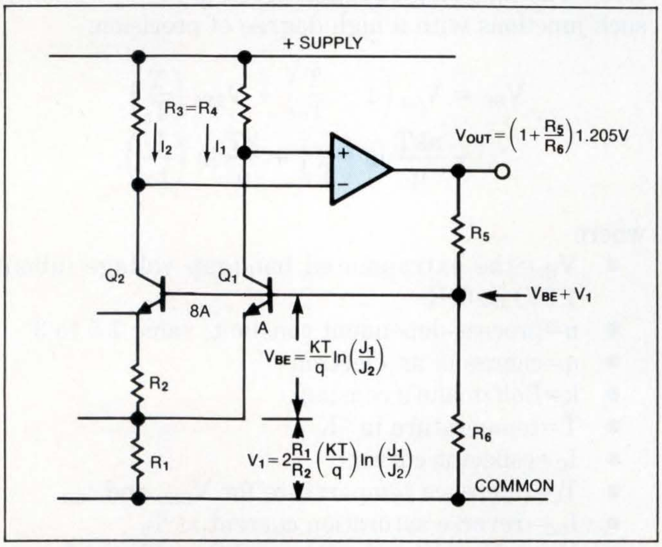


Fig 1—A bandgap voltage reference *generates the sum ($V_{BE}+V_1$), in which the two voltages have equal and opposite temperature coefficients. The amplifier then raises the sum to a more convenient voltage level.*

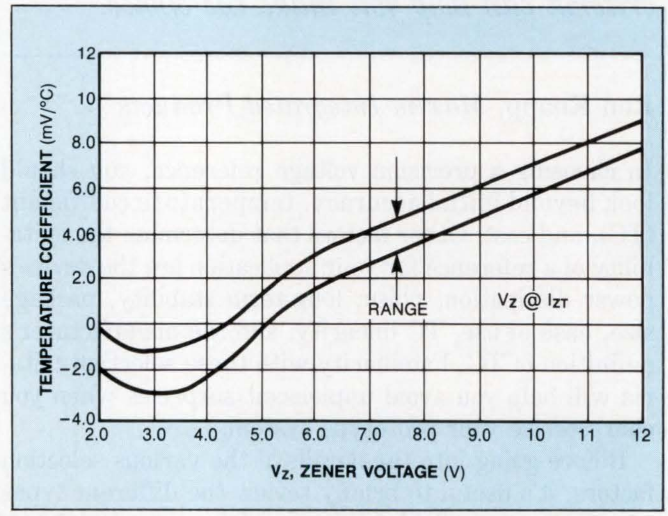


Fig 2—Zener diodes produce a zero-TC voltage *near 5V—the level for which the mechanisms of negative-TC field-emission breakdown and positive-TC avalanche breakdown are in balance. However, the zero-TC ideal is difficult to achieve on a production basis.*

marily on the breakdown-voltage value and to a lesser degree on the operating current. The zener breakdown involves two mechanisms: field-emission breakdown, which dominates below 5V and produces a negative TC, and avalanche breakdown, which occurs above 5V and yields a positive TC. Although complex and difficult to quantify, these breakdown mechanisms should be in balance at approximately 5V, yielding a near-zero TC. Tests corroborate this contention **(Fig 2)**.

Unfortunately, 5V zener diodes exhibiting the utopian zero TC are difficult to produce. The problem is that the negative TC breakdown mechanism is flukey and difficult to reproduce consistently in production. The positive TC breakdown, on the other hand, is predictable and eminently repeatable for devices using routine semiconductor-production processes. Another characteristic that's predictable and repeatable is the negative-slope temperature characteristic of a forward-biased diode.

Because of the difficulty of producing a zero-TC zener diode that depends purely on breakdown mechanisms, it's evident that the TC of a zener-diode reference should not depend solely on the absolute zener breakdown voltage. A class of zener diodes, called TC zeners, takes a compensatory approach by balancing the negative TC of a forward-biased diode (−2 mV/°C) with the equal and opposite TC of a 5.6V zener diode. The output voltage is therefore 6.3V (0.7V+5.6V). These references offer 5- to 100-ppm/°C TCs and require operating currents from 0.5 to 7.5 mA. You must maintain the specified operating current to obtain the guaranteed TC.

Precision references need laser trimming

To achieve accuracies as tight as ±0.01% in precision references, manufacturers use laser-trimmed thin-film resistors. Diffused resistors embedded within silicon exhibit not only hysteresis, but also high TC, poor TC matching, large voltage coefficients, and poor stability. Thin-film resistors, deposited on the chip's surface, are found in such voltage references as the REF01, AD581, AD2700, and the MAX670.

The secret to the precision references' accuracy is to trim the thin-film resistors by laser before attaching a lid to the package. This critical operation determines a reference's initial accuracy and its long-term stability. Fuse-link blowing and resistor-link trimming are alternative schemes for trimming the absolute voltage, but the chip area required with these methods makes them prohibitively expensive for tight-tolerance adjustments.

Thick-film resistors have insufficient stability for use in precision references; therefore, hybrid products such as the MAX670, AD2700, and AD2710 include TaN (tantalum nitride) or NiCr (nichrome) thin-film resistors, sputtered on a ceramic substrate of 99.6% alumina (Al_2O_3). Before trimming each lot of references, the manufacturer determines the optimum settings for laser power and focus by executing a test matrix of experimental laser cuts.

For each power setting, the system makes a staircase trim pattern in which each right-angle turn marks an additional increment of focus **(Fig A)**. After completion of the focusing and system-calibration steps, quality-control personnel inspect the trim process every 30 minutes to ensure uniform cuts throughout the manufacturing lot. The system achieves extremely clean trims in this way **(Fig B)**. To prove its stability, each device must maintain initial accuracy after trim during a 48-hour, 150°C burn-in operation.

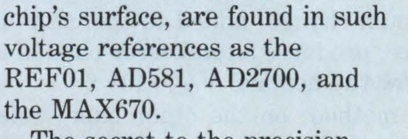


Fig A—A staircase test matrix helps to optimize focus and power levels *in a laser system used for trimming precision thin-film resistors.*

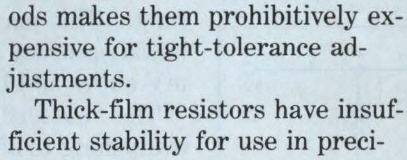


Fig B—After calibration, a laser-trim system cuts cleanly *through a thin-film resistor. The calibration depends on the staircase setup technique of* ***Fig A.***

You can easily achieve a 1-ppm/° C TC by mounting a zener-reference circuit of reasonably low TC on a heated substrate.

The AD2700 and MAX670 series of hybrid references, for example, use a 1N827 zener diode—chosen for low noise, low dynamic impedance (10Ω max), and good TC linearity. (Why use a hybrid? Fabrication of these TC zener references involves a specialized process, involving extra steps not always available in a standard bipolar process.) The products' initial 10-ppm/°C TC is that of the zener diode. Active laser trimming then lowers the TC by adjusting the zener-diode current, thereby creating additional 3- and 1-ppm/°C product grades (see **box,** "Precision references need laser trimming").

The manufacturer calculates the required zener current using actual TC values, obtained through oven tests on unsealed devices. Note that the amplifier in **Fig 3** supplies current to the zener, which in turn supplies an input voltage to the amplifier. To ensure circuit startup, R_4 supplies current to the zener and the amplifier uses ground as its negative supply, thereby eliminating $V_{OUT}=0V$ as an unwanted stable state. Note that the amplifier in a zener reference contributes less output noise than does the amplifier in a bandgap reference, because the zener voltage requires less amplification.

Heater trades P_D for stability

The third type of reference, based on either a bandgap or zener voltage, uses a local heater to maintain the substrate at a constant temperature, usually 10 or 15 degrees above the upper limit of the operating range. If the circuit's TC is reasonably low (20 to 30 ppm/°C), such a reference can easily achieve a TC of 1 ppm/°C. The disadvantage is power dissipation—an LM199 at −55°C, for example, requires as much as 28 mA at 15V for the heater alone.

Also, the LM199's output voltage stabilizes at 1 ppm/°C but the initial accuracy is only ±5%. To meet the ±0.1% or ±0.01% tolerances required in data-converter applications, therefore, you must add a precision op amp and scaling resistors and then cope with these components' additional cost and error contributions. The proper evaluation of a reference application involves these issues as well as many of the following ones, which are not always covered explicitly in the data sheet.

Confusion surrounding the specification of temperature coefficient, for instance, is partly a matter of definition. Two definitions are popular. In the "box" method, V_{OUT} for an in-spec device must remain within a rectangle formed by T_{MIN}, T_{MAX}, and the maximum specified ΔV_{OUT} **(Fig 4).** ΔV_{OUT} is the product of the nominal output voltage (V_{NOM}), the specified TC, and the operating-temperature range. For the AD2700L,

$$\begin{aligned}\Delta V_{OUT} &= V_{NOM}\,(TC)\,(T_{MAX} - T_{MIN})\\ &= 10V(3\ ppm/°C)\,[85-(-25)°C]\\ &= 3.3\ mV.\end{aligned}$$

In other words, V_{OUT} will change no more than ±3.3 mV between any two temperatures in the operating range. This maximum change, added to the ±2.5-mV initial-accuracy spec, produces a total error band of 5.8 mV above and below the nominal V_{OUT} (10V).

The "butterfly" method, on the other hand, refers everything to 25°C and allows the manufacturer to use

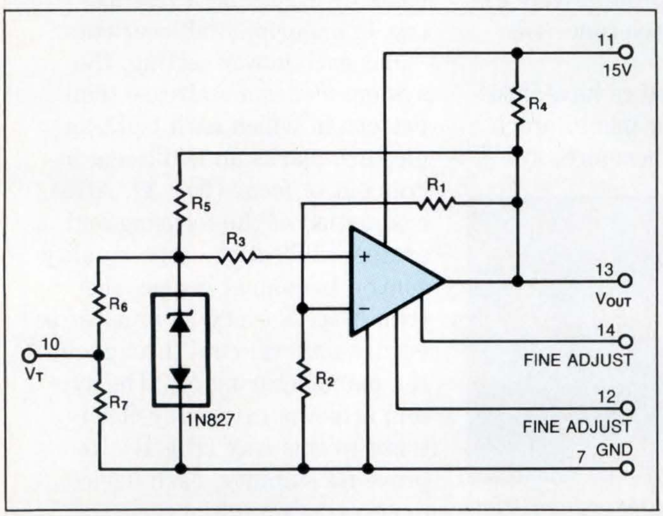


Fig 3—The amplifier in this zener-diode reference *bootstraps the zener voltage by delivering current to the zener while the zener delivers voltage to the amplifier. R_4 provides start-up current to the zener.*

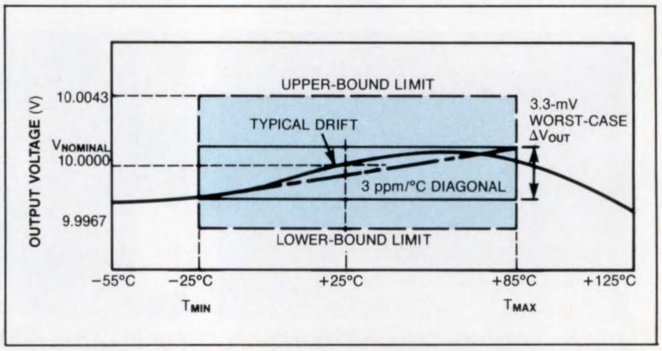


Fig 4—In the "box method" of specifying TC, *the operating-temperature range and the maximum allowed change in V_{OUT} form the sides of a rectangle, and the slope of the rectangle's diagonal becomes the TC.*

different TCs in determining the error bands at temperatures above and below 25°C (**Fig 5**). The AD2710K, for example, specs a change of ±0.9 mV over the 25 to 70°C range (10V×2 ppm/°C×(70−25)°C). You must add to this the initial tolerance of ±1 mV at 25°C, resulting in a maximum possible error of ±1.9 mV at T_{MAX} (70°C).

Such systems as DVMs and data-acquisition instrumentation often use the box method for specifying total error, because users aren't likely to calculate accuracy using the TC specs. This approach has a disadvantage —the whole 3.3-mV error change in the example of **Fig 4** could occur between, say, 25 and 70°C, yielding an effective TC of 7.33 ppm/°C, which exceeds the maximum specified TC (3 ppm/°C). A worst-case analysis over temperature, however, must allow for this much change anyway, regardless of where it occurs in the operating-temperature range.

Because temperature testing plus the reading and recording of data are costly, manufacturers usually base TC specs on only a few data points. These should include at least 25°C and the endpoints (T_{MIN} and T_{MAX}). Using the endpoints alone, for example, can make the reference appear better than it actually is if the TC curve is symmetrical and parabolic.

You should avoid using "typical" specs for TC and absolute accuracy; only tested and guaranteed limits for minimum and maximum have meaning. A data sheet should also identify the temperatures used in the calculation of the device's TC. The AD2700L data sheet, for instance, lists 25°C plus the endpoints (−25 and 85°C). The AD2700U data sheet lists these three as well as the extended endpoints of −55 and 125°C.

Correction yields S curve

Although voltage-reference data sheets seldom specify TC linearity, the characteristic curves for V_{OUT} over temperature contain the most useful TC-linearity information that a manufacturer can provide. For bandgap references these curves are parabolic or S-shaped (**Fig 6**), depending, among other factors, on whether the device includes a linearity-correction circuit. The TC linearity of zener-based references depends mainly on the zener diode, and the reference will include one of two diode types, depending on the intended temperature range and the desired linearity (see **box**, "Zener diodes determine TC linearity").

Another important specification is noise, which appears on most data sheets as a typical value but seldom has a guaranteed limit. Because noise testing is difficult, manufacturers usually guarantee maximum values by performing sample testing only, if that. What's more, because a designer can easily filter or band-limit the higher frequencies by adding capacitors, noise specs cover the 0.1- to 10-Hz range in nearly all cases. (The suppression of low-frequency 1/f noise, however, requires impractically large capacitor values.)

Data sheets usually specify noise in terms of $nV/\sqrt{Hz}$, an expression that allows you to calculate output noise for the bandwidth of interest. At the same time, you usually convert this quantity to the more useful μV p-p, especially for converter applications:

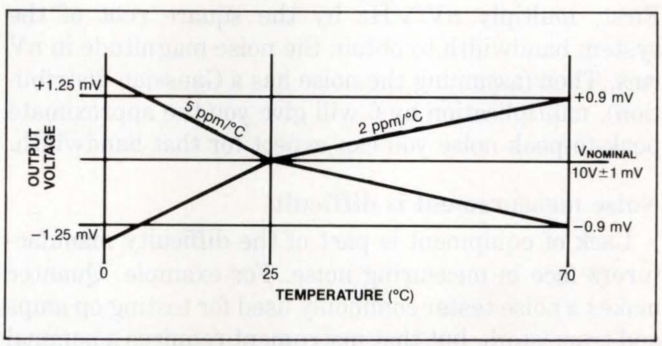


***Fig 5—The "butterfly" method of TC specification** normalizes the variation of V_{OUT} with respect to 25°C. You then extend wing-shaped error bands to the operating-temperature extremes.*

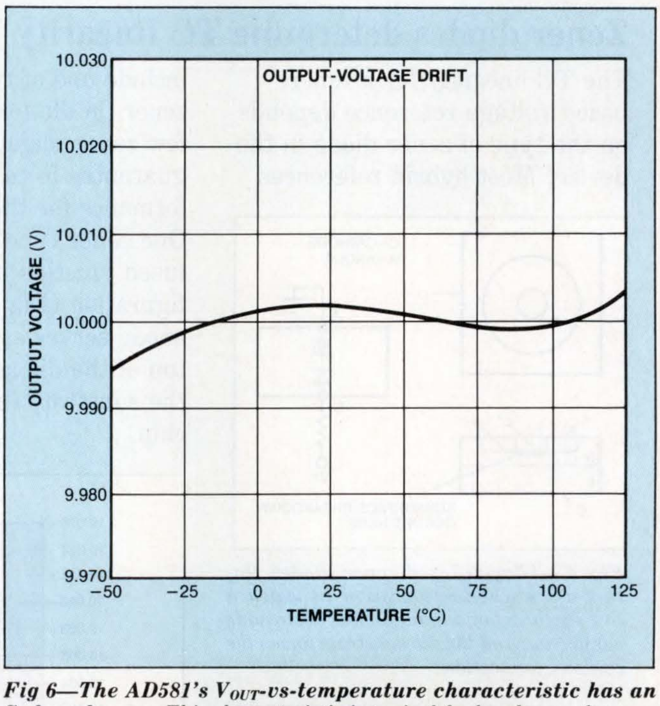


***Fig 6—The AD581's V_{OUT}-vs-temperature characteristic has an S-shaped curve.** This characteristic is typical for bandgap references that include correction circuits for TC linearity.*

Bandgap references usually have a parabolic TC characteristic that assumes an S shape if the device includes circuitry to effect linearity correction.

First, multiply nV/√Hz by the square root of the system bandwidth to obtain the noise magnitude in nV rms. Then (assuming the noise has a Gaussian distribution), multiplication by 6 will give you the approximate peak-to-peak noise you can expect for that bandwidth.

Noise measurement is difficult

Lack of equipment is part of the difficulty manufacturers face in measuring noise. For example, Quantec makes a noise tester commonly used for testing op amps and transistors, but that instrument requires a nominal 0V bias for the circuit node under test. Spectrum analyzers make good noise testers, but not many have the dynamic range and the low noise floor necessary to measure, say, 10-μV signals riding on 10V dc. Frequency range is another complication. Spectrum analyzers come in high- or low-frequency models (above or below 100 kHz), so one model doesn't cover the measurement range needed for many applications—0.1 Hz to several megahertz.

You can measure noise directly using a Tektronix storage oscilloscope with a 7A22 plug-in amplifier, which has 10-μV/div sensitivity and selectable lowpass and highpass filters that cover 0.1 Hz to 1 MHz. The

Zener diodes determine TC linearity

The TC linearity for a zener-based voltage reference depends on the type of zener diode in the device. Most hybrid references include one of two types of TC zener (in die form), and only a few zener manufacturers can guarantee 5- to 10-ppm/°C performance for these products. One zener type has an alloy-diffused junction in a vertical configuration **(Fig A),** wherein the anode serves as a bond pad on top of the die and the cathode as the substrate (backside) of the chip.

The other type of zener features an ion implant and lateral geometry **(Fig B),** and has both connections on top of the chip. For this type, the substrate must float unconnected, because the substrate is the junction of two zener diodes—one operating as a zener in the breakdown mode, and the other operating as an ordinary forward-biased diode. The zener voltage is 5.6V,

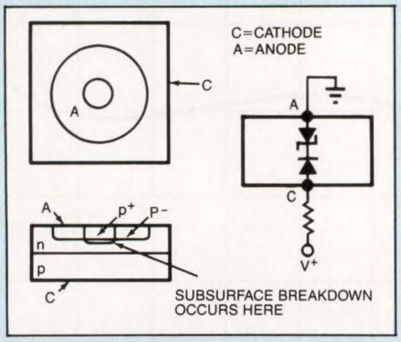


***Fig A—Alloy-diffused zener diodes** feature a vertical configuration in which a top-surface bond pad forms the anode connection and the die substrate forms the cathode connection.*

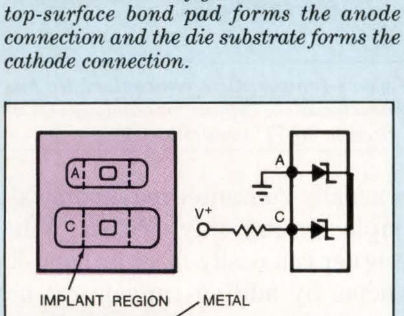


***Fig B—The lateral geometry of ion-implanted zener diodes** places both diode connections on the top surface of the chip.*

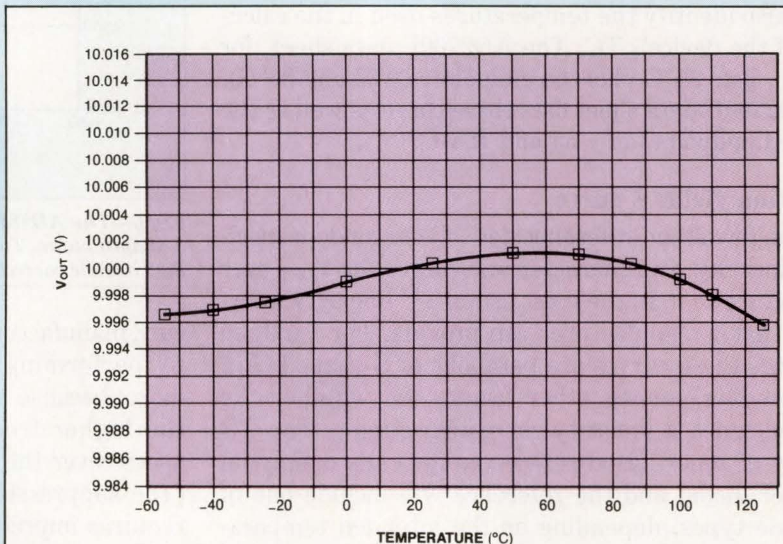


***Fig C—An ion-implanted-zener reference** such as the AD2700 exhibits a concave-down TC characteristic and better overall linearity than does a diffused-zener type for the range −55 to +125°C.*

lowpass settings don't include 10 Hz, however, and the amplifier's input-voltage limitation may require that you ac-couple the signal. The coupling capacitor then forms a highpass filter of a few hertz that precludes the use of the 0.1-Hz highpass setting.

For a more convenient method of noise testing with a storage oscilloscope, you use a low-noise op amp configured for a gain of 100, a 0.1-Hz highpass input filter, and a 10-Hz lowpass output filter **(Fig 7).** The gain boosts 10-μV signals to 1 mV—within the range of most oscilloscopes—and allows use of an OP07A (whose 0.6-μV p-p max noise contributes less than 60 μV p-p noise at the output).

To measure noise, set the scope amplifier's vertical-input coupling to dc. Allow the filter to settle and the reference to warm up (about 30 sec in most cases). Clear the screen in storage mode and set the time base for single-trigger mode at 1 sec/div. Set the scope to save mode or maximum screen persistence and measure the peak-to-peak noise for 10 sec. (Observation for 10 seconds is the accepted method, even though the time constant for 0.1 Hz is only 1.6 sec.) A scope photo based on this technique **(Fig 8)** shows about 20-μV p-p noise for the AD581—typical for most bandgap references—

and when operated at the proper current, it produces a TC of 2 mV/°C—a TC equal to and opposite that of the forward-biased diode. For this reason, nearly all temperature-compensated zener diodes have a total voltage of 6.3V (5.6+0.7V). You can create a higher output voltage by connecting multiple forward-biased diodes in series with a higher-voltage zener diode.

Both TC-zener types specify V_{OUT} as 6.3V±5%, but the actual tolerance for ion-implanted types is tighter (typically ±40 mV, or ±0.6%), vs ±300 mV (±4.7%) for alloy-diffused types. The tighter tolerance of ion-implanted zener diodes allows the reference manufacturer to target gain-resistor values more closely, do less laser trimming, and thereby provide better V_{OUT} stability.

TC linearity is the most noticeable difference between the two zener types. The implanted zener's concave-down curve exhibits better overall linearity from −55 to 125°C **(Fig C),** but the diffused zener has better TC linearity from 0 to 70°C **(Fig D).** Both the forward-biased diode and the zener diode contribute to the nonlinearity, and these effects increase at low current.

Accordingly, most TC zeners have operating currents in the 0.5- to 7.5-mA range, which is an order of magnitude higher than that of zeners normally found in an IC. High current (sufficiently beyond the value at the zener's breakdown voltage) also ensures low noise.

Though it's a tedious procedure, you can always characterize the reference over temperature and then compensate for the TC nonlinearity by using a temperature sensor, A/D converter, and software lookup table. The well-controlled ion-implant process offers a compromise solution, however—the use of zener diodes in which the TC curves and 25°C voltages are repeatable from lot to lot.

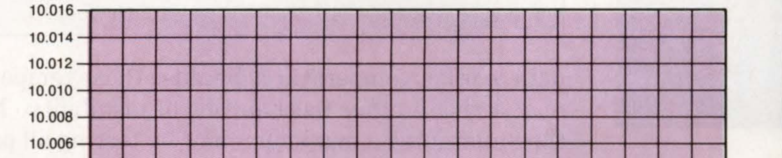


***Fig D—The output of a diffused-zener reference** such as the AD2710 provides excellent TC linearity from 0 to 70°C, but suffers in linearity outside that range.*

Often, the statistical data taken by the manufacturer on life-test samples is the best stability information you can obtain about a reference.

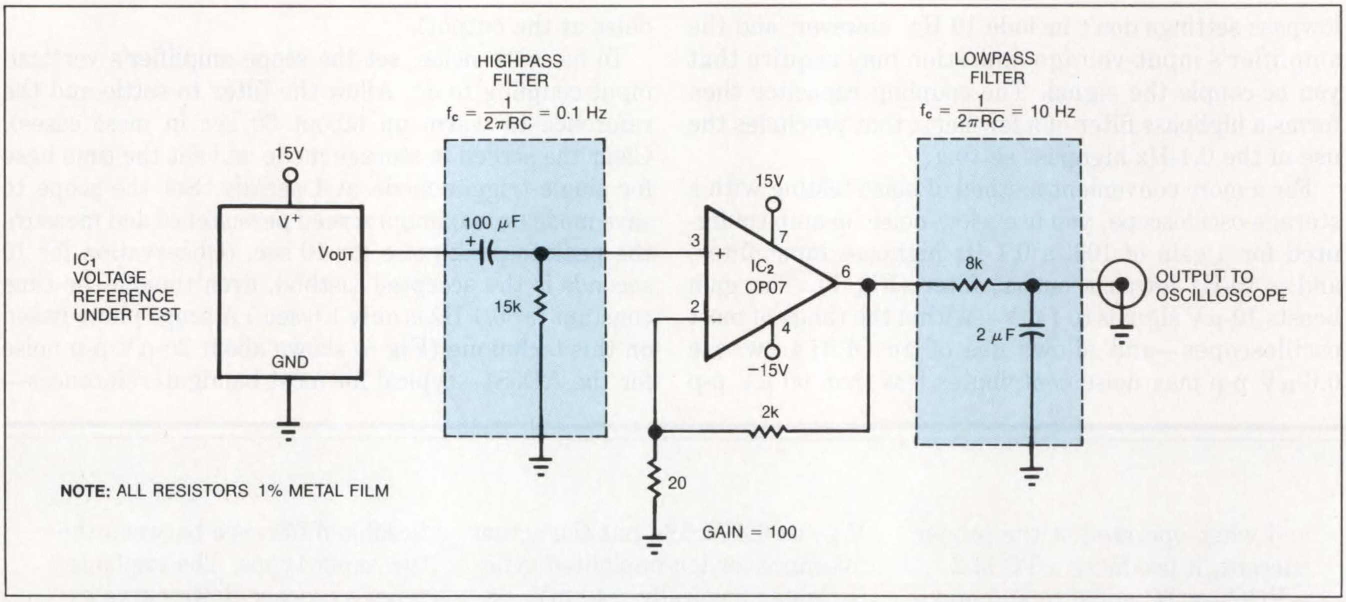


*Fig 7—**Introducing highpass and lowpass filters** and a low-noise op amp lets you measure voltage-reference noise using a storage oscilloscope.*

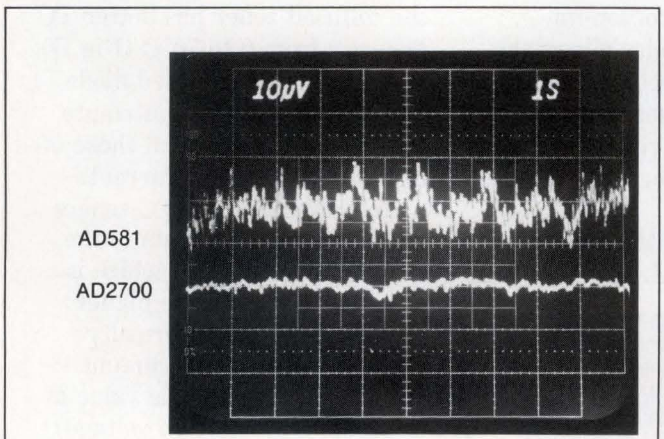


*Fig 8—**This scope photo shows the noise levels** typical for a bandgap reference (upper trace) and a zener-based reference (lower trace). The scale is 10 μV/vertical div; 1 sec/horizontal div.*

TABLE 1—REFERENCE-NOISE COMPARISON

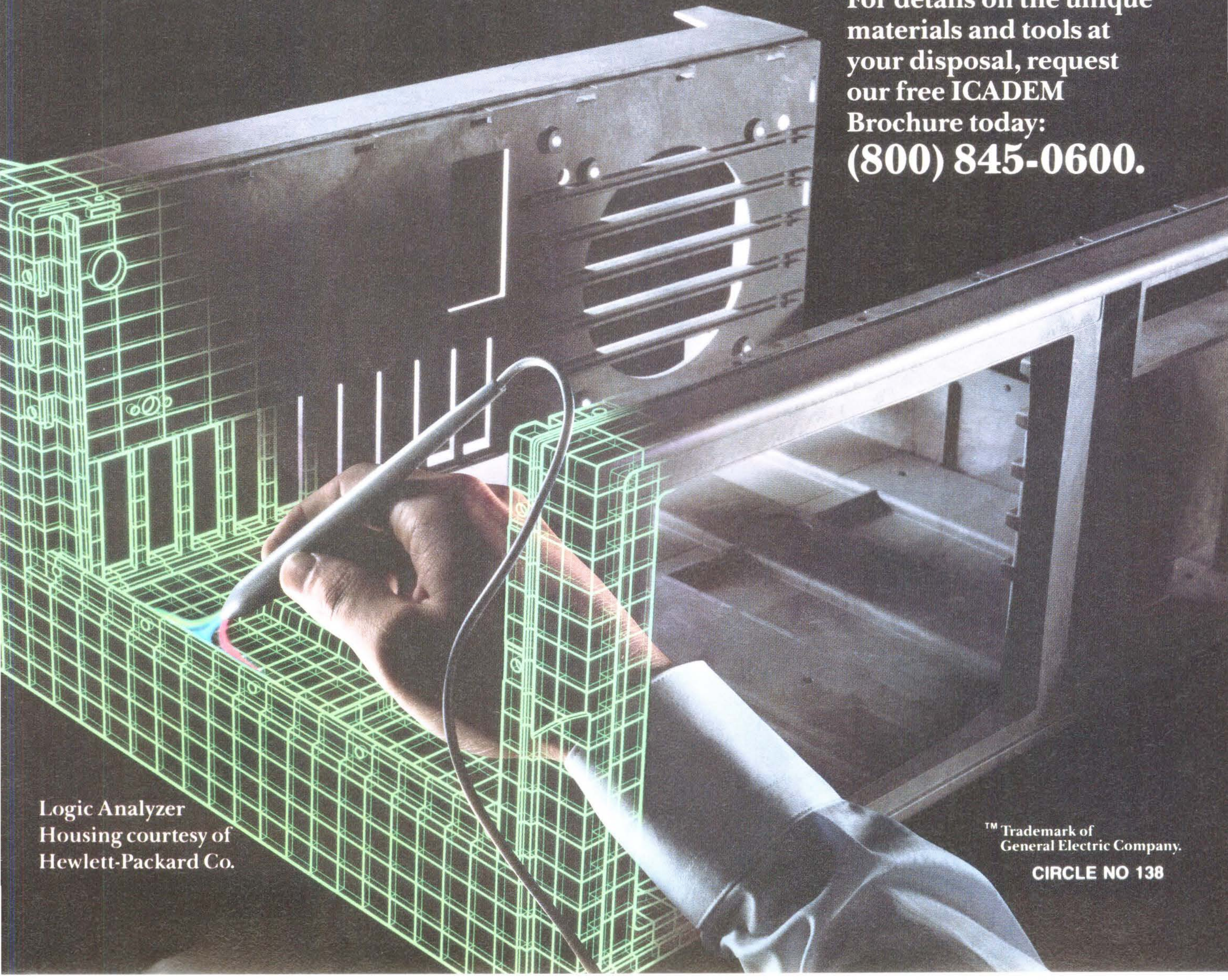
BANDWIDTH	NOISE (μV p-p) AD581 (BANDGAP)	AD2700 (ZENER)
0.1 TO 10 Hz	20	5
1 TO 100 Hz	50	8
1 Hz TO 3 kHz	220	30
1 Hz TO 300 kHz	600	200

and about 5 μV p-p for the AD2700 zener reference. **Table 1** compares noise for these devices over different bandwidths.

Long-term stability

Long-term stability can be the most important spec in a reference application, but—as in the case of noise—this parameter seldom receives a thorough characterization in the data sheet. Most manufacturers specify stability as 25 to 100 ppm (typ) per thousand hours at 125°C. They cannot accurately extrapolate this stability data to other temperatures because those temperatures may activate other mechanisms of instability. Nor can they guarantee a maximum limit by testing all parts for 1000 hours, because 100% burn-in testing costs too much. (And in any case, the manufacturer cannot guarantee a reference's stability for the second 1000 hours.) The solution, therefore, is to either test samples only or to guarantee this spec "by design" (in other words, the manufacturer will replace customer parts that fail).

Often, the best reference-stability information that a customer can obtain is the statistical data taken by the manufacturer on life-test samples. Maxim, for example, records long-term stability for a set of sample devices operating continuously for several thousand hours at 55°C (a realistic operating temperature that is higher than the room ambient temperature but lower than T_{MAX}). Such data (**Fig 9**) for the AD2700, for instance,



Output-current specs are misleading unless they specify V_{OUT} limits such as those in the spec for load regulation.

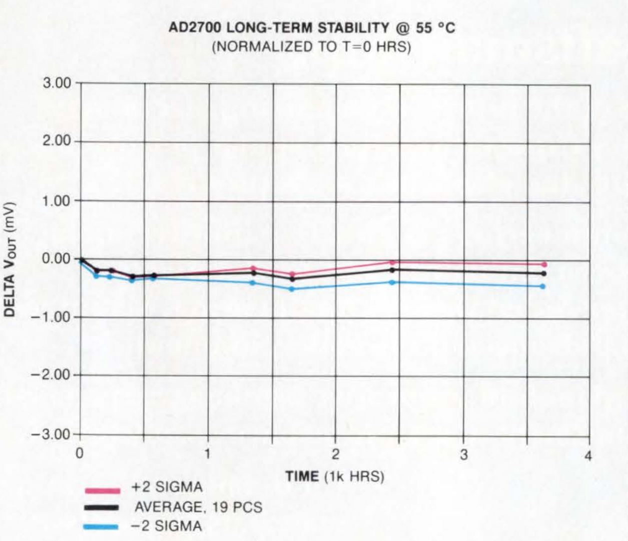


Fig 9—The average stability of AD2700 voltage references over 3600 hours *at 55°C appears in the center curve. The upper and lower curves denote 2-sigma boundaries that encompass 90% of the 19 units tested.*

shows that V_{OUT} drifts about 250 μV negative and then remains within ±50 μV of that level. The center curve represents typical performance; the upper and lower "2-sigma" curves encompass 90% of the devices, based on the standard deviation of measured values.

I_{OUT} specs can be misleading

Output-current specs are misleading unless they specify V_{OUT} limits such as those included in the spec for load regulation. Note how this parameter reveals important differences in several reference devices. The AD2700, for example, has a 741-type output circuit that can sink and source current equally well within a range of ±10 mA. V_{OUT} changes 0.5 mV max for a 0- to 10-mA change in output current, resulting in a load regulation of 50 μV/mA max.

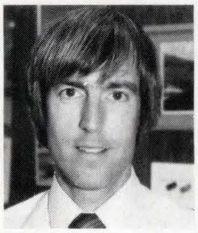
The MAX671 has Kelvin outputs that provide load regulation of 10 μV/mA max. The 10V REF01 monolithic reference, on the other hand, has a simple emitter-follower output that can only source current (to ground); its load regulation is 1 mV/mA max over 0 to 10 mA. For the AD580, this same 1-mV/mA limit represents lower performance because V_{OUT} is only 2.5V. The 10V references AD581 and AD584 can source as much as 10 mA at 25°C but specify the load regulation (500 μV/mA max) to only 5 mA. These two devices have limited current-sinking capability over the MIL temperature range. They guarantee 5-mA source current over the full operating-temperature range.

Measure V_{OUT} vs V_{SUPPLY}

Line regulation and power-supply rejection ratio (PSRR) are two other important parameters for voltage references. They represent the change in V_{OUT} that results from fluctuations in supply voltage. Line regulation is a dc test whose results are usually expressed in μV/V or mV/V. PSRR can be a dc test, but usually the test conditions for this parameter include a range of frequencies or a specific frequency. The line-regulation spec has the advantage that self-heating effects are included in the output-voltage change. PSRR, on the other hand, has more realistic test conditions. At 60 Hz in particular, self-heating effects average out but the power supply may offer poor regulation, degrading the stability of V_{OUT}.

Finally, consider the implications of temperature hysteresis in your application. A reference output V_{OUT1} at temperature T_1 should return to V_{OUT1} after you cycle the device to T_2 and back to T_1. If not, the output exhibits hysteresis. The cause is thermal stress within the IC, which in turn causes expansion of the silicon with temperature—and this effect is aggravated by the contact of dissimilar packaging materials that have different coefficients of expansion. With the exception of that for the LT1021 (Linear Technology Corp, Milpitas, CA), voltage-reference data sheets rarely mention hysteresis. **EDN**

Author's biography



Ron Knapp is a senior member of the technical staff at Maxim Integrated Products (Sunnyvale, CA). He holds a BS in systems engineering from Boston University, an MSEE from Worcester Polytechnic Institute, and is vice president of the Northern California Chapter of The International Society for Hybrid Microelectronics (ISHM). In his spare time, Ron enjoys flying and sailing.

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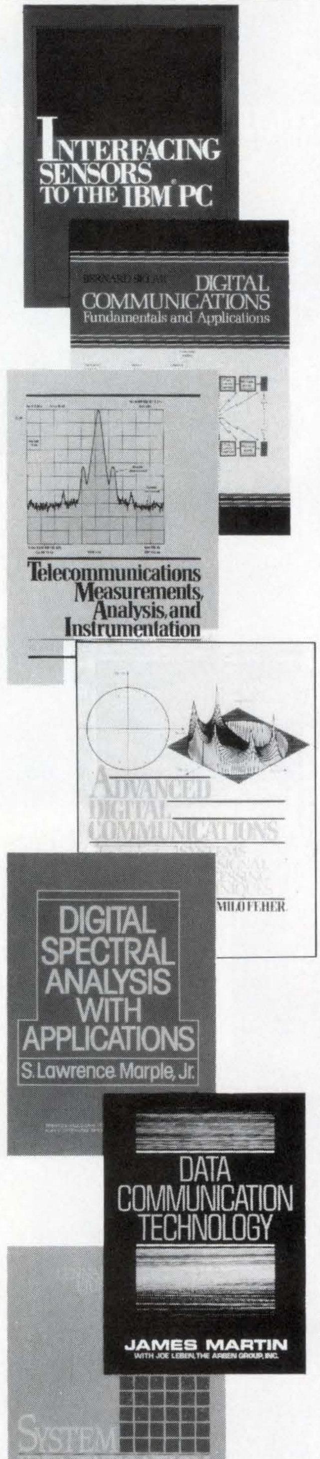

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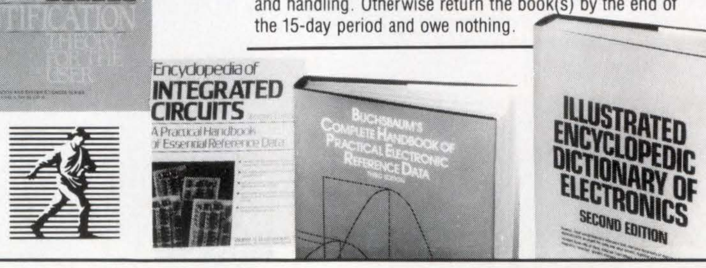

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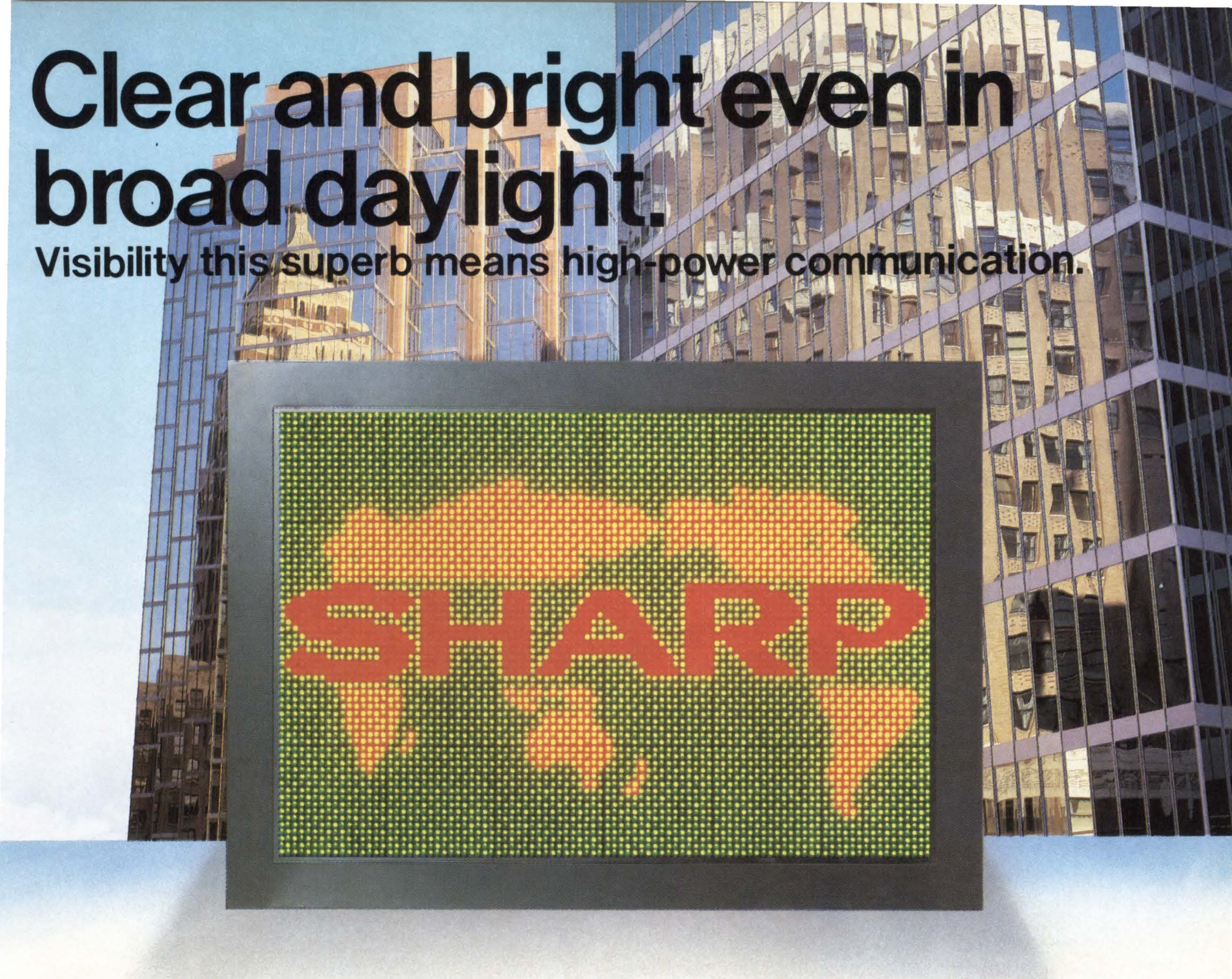

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		Colored diffusion	Colored transparency	Colorless transparency		Min	Typ	
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				○	GL5UR2K1	1400	2000	
			○		GL5UR3K	2400	3000	
				○	GL5UR3K1	2400	3000	
			○		GL5UR46	250	400	
				○	GL5UR2K6	1400	2000	
	7.5φ			○	LT9550L	200	400	Red
		○			LT9552L	80	200	
	7.5φ *1 (Dichromatic LED lamp)			○	LT9550EL	120	250	Red
						80	120	Yellow-green
				○	*2 LT9555EL	TBD	60	Red
							40	Yellow-green
	10φ			○	LT9512U	4000	5000	Red
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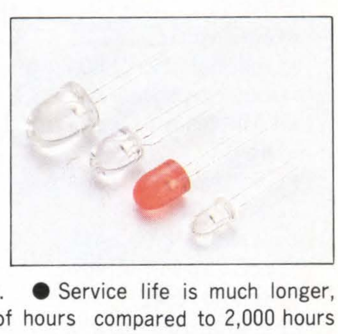

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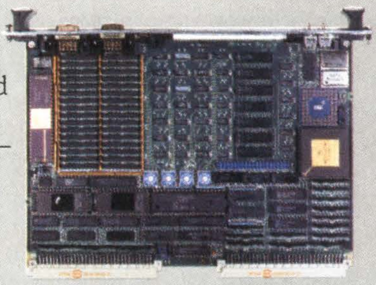

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CIRCLE NO 134

Serial techniques expand your options for μC peripherals

The Serial Peripheral Interface (SPI) bus of the MC68HC11 microcomputer is flexible enough to let you attach devices designed for other serial buses—Signetics' IIC peripherals, for instance, or ITT's IM family.

Naji Naufel, *Motorola Inc*

Designers usually assume that basing a system upon a particular single-chip microcomputer unit (MCU) will restrict their choice of peripherals to those for which interface functions are available on the MCU or on subsystem chips of the same family. Unfortunately, peripheral family members may not be adequate to meet the needs of your application. For a system based on the Motorola MC68HC11, however, you can expand your options by attaching serial devices to the MC68HC11's SPI bus. This bus is adaptable enough to work with serial devices designed for other buses, such as the Signetics family of Inter-Integrated-Circuit (IIC) peripherals and the ITT family of Intermetall (IM) peripherals.

Although devices in the Signetics and ITT families aren't directly compatible with the MC68HC11 microcomputer, it's not difficult to attach them, as slave devices, to the Motorola SPI bus. You'll find it fairly straightforward, for instance, to connect two relatively simple devices, a clock/timer from the IIC family and an EEPROM from the IM family, to the MC68HC11's bus. If you want to attach more complex devices from either family, you'll probably need to study the source documentation **(Refs 1, 2, and 3)**, but the schematics and software routines that follow will be adequate as a starting point. For additional information about the registers to which the software routines refer, see **box,** "Three registers control the SPI."

Interbus connections are simple

The SPI consists of little more than an 8-bit shift register with separate lines for incoming and outgoing data, and a third line that carries the shift clock. The protocol is simple; you set the interface for a read or a write operation and generate eight clock pulses to shift the data in or out, sending the most significant bit (MSB) first.

The IIC bus has a single, bidirectional data line and a clock line, but the transmission protocol is a little more complex; it requires both a start and a stop condition. In addition, the clock sequence consists of nine pulses; eight of these pulses shift the data bits in or out (MSB first), and the ninth allows a slave device to acknowledge receipt of the data byte.

The IM bus also has a bidirectional data line and a clock line, but in addition it requires an IDENT line that distinguishes between an address and a data byte.

Because you can configure the SPI lines as open-drain circuits, you can connect both the serial-input and serial-output lines to the bidirectional data line of a peripheral.

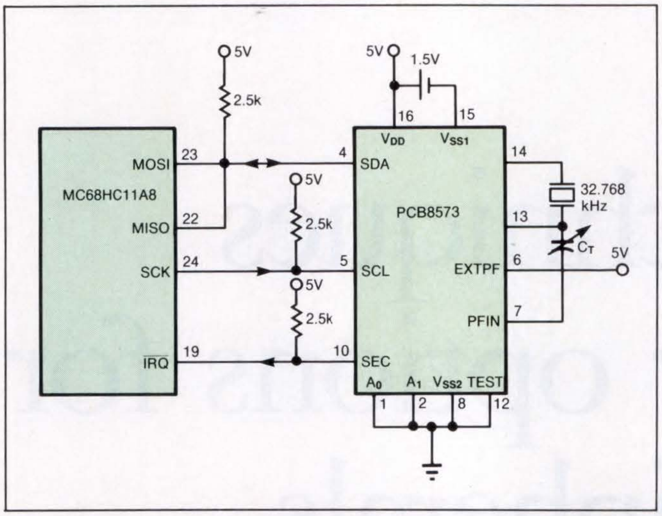

Fig 1—You need only three lines to connect the PCB8573 clock/timer *from the Signetics IIC family to the SPI bus of an MC68HC11A8 microcontroller.*

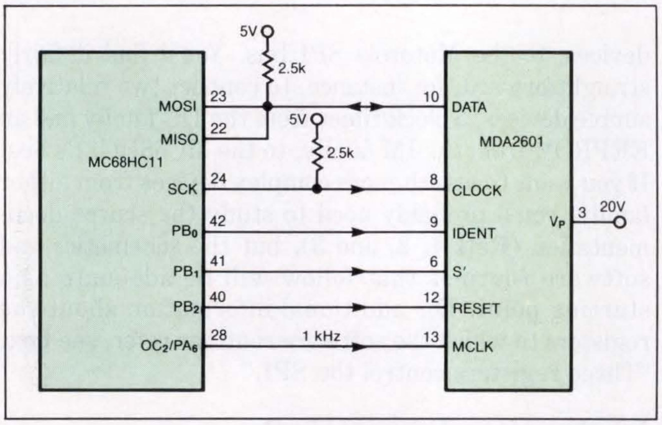

Fig 2—Serial peripherals of the ITT Intermetall family, *such as the MDA2601 EEPROM, need part of a parallel port for control purposes, as well as the SPI, for data transmission.*

Unlike the other two buses, IM devices send the least significant bit (LSB) first. Therefore, if you're interfacing the SPI to an IM device, you must provide a software routine to reverse the bit order before sending and after receiving a data byte.

Fig 1 shows how to connect an IIC clock/timer chip to the SPI bus, and **Fig 2** shows the connections for an IM EEPROM. In both cases, you have to connect the MOSI (master out, slave in) pins of the 68HC11 microcomputer to the MISO (master in, slave out) pins and to the bidirectional data pin of the peripheral device. Because the MOSI pin is part of an internal open-drain circuit, you need a pullup resistor on the line.

For this type of configuration, you send data to the peripheral merely by writing the data byte to the shift register (SPDR). To receive data from the peripheral, you generate receive shift-clock pulses by writing FF_{HEX} to the transmit register as if you were sending it. Again, because the MOSI line is part of an open-drain circuit, incoming data bits that are set to 1 don't affect the MOSI/MISO line status (which defaults to high because of the FF_{HEX} in the transmit register); incoming bits that are set to 0, however, can pull the line low without difficulty.

IIC software uses only port D

The software that lets you emulate the IIC protocol takes advantage of the MC68HC11's ability to use its port D pins either as SPI pins (when the SPI is enabled) or as general-purpose, independent I/O pins (when the SPI is disabled). The sample software of **Listing 1** (pg 203) makes use of this feature to generate the timing shown in **Fig 3.**

To initialize the interface, turn off the SPI (SPE=0) and set bits 3 and 4 of port D high to generate the idle

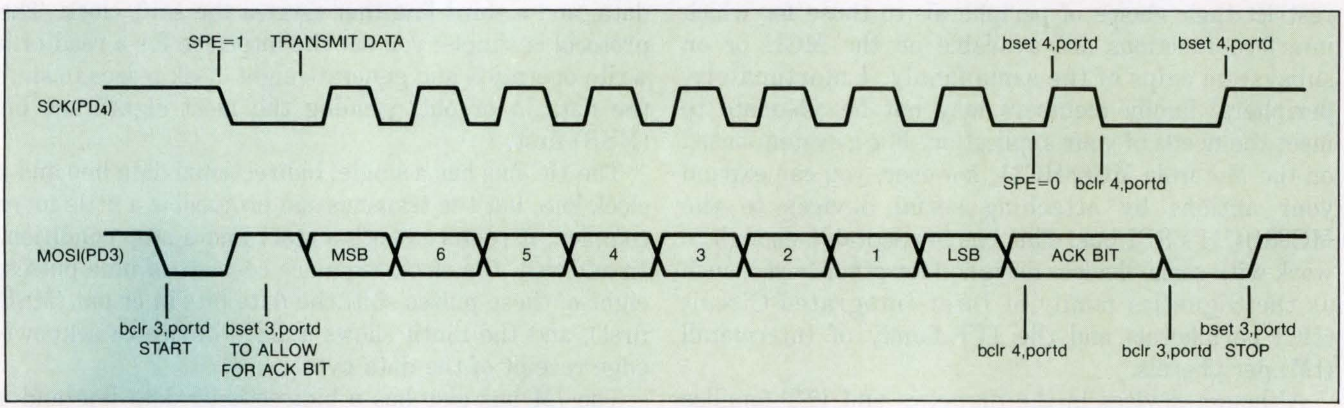

Fig 3—By turning off the SPI, you can use its pins as independent I/O lines. *Thus, you can interface the MC68HC11 MCU to IIC peripherals without using any other ports, as this timing diagram shows.*

condition of the MOSI and SCK lines. To send a byte to the peripheral, you first load the byte into the B accumulator and then generate a start condition by clearing bit 3 of port D while leaving bit 4 high. Next, you turn on the SPI; this action forces the SCK line low and the MOSI line high (CPOL=CPHA=0) and causes the MCU to transmit the eight data bits.

When all the data bits have been shifted out, you clear bit 4 of port D, then turn off the SPI and generate the acknowledge clock pulse by first setting, then clearing, bit 4 of port D. Finally, after the last byte has been sent, you call the Stop subroutine to generate a stop condition by setting bit 3 of port D high while bit 4 (the clock line) is in the idle (high) state.

Devices that use the IM bus examine the IDENT line; because this line must be held low throughout the

Three registers control the SPI

The SPI (Serial Peripheral Interface) allows you to use the MC68HC11 microcomputer's I/O port D to communicate with a peripheral device over a simple serial link. The three main registers are the SPI control register (SPCR), the SPI data register (SPDR), and the SPI status register (SPSR) **(Fig A).**

The SPCR stores control words sent by the processor via the microcomputer's internal data bus. The SPE bit enables or disables the SPI; the CPOL bit determines the polarity (high or low) of the SCK clock line in the idle condition; the CPHA bit determines which edge of the SCK clock latches data into or out of the shift register; the MSTR bit determines whether the SPI will act as a master or as a slave; and the two SPR bits select the shift-clock rate. The DWOM bit, when set to 0, configures the six port D pins as normal CMOS outputs; when set to 1, it configures these pins as open-drain outputs.

The SPDR consists of a read-data buffer and a shift register. To write data to a peripheral, you load the shift register directly; a second write instruction, issued before the current byte has been completely transmitted, will be ignored. During a read operation, however, an incoming byte is automatically transferred to the buffer as soon as the last bit has been clocked into the shift register; therefore you have one byte-time in which to fetch the byte, while the next byte is filling the shift register.

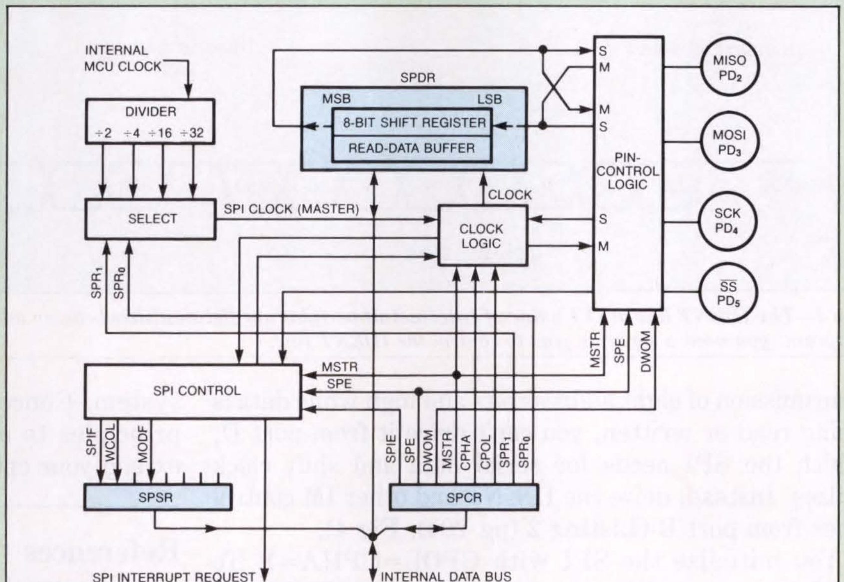

Fig A—The SPCR, SPDR, and SPSR registers provide control of the SPI, transmit/receive facilities, and status information.

In the SPSR, the completion of a data transfer between the MCU (microcomputer unit) and the peripheral device, in either direction, sets the SPIF bit (transfer-complete flag). To clear the SPIF, you must first read the SPSR and then read or write the SPDR. When the SPIF is set, failure to read the SPSR will inhibit any attempt to write to the SPDR. Attempting to write to the SPDR while a data transfer is in progress will set the WCOL bit (write-collision flag) and inhibit the write operation. To clear the WCOL bit, you must first read the SPSR and then write the data byte to the SPDR.

To communicate with the IM bus, you must reverse the bit order of each byte before sending it or after receiving it.

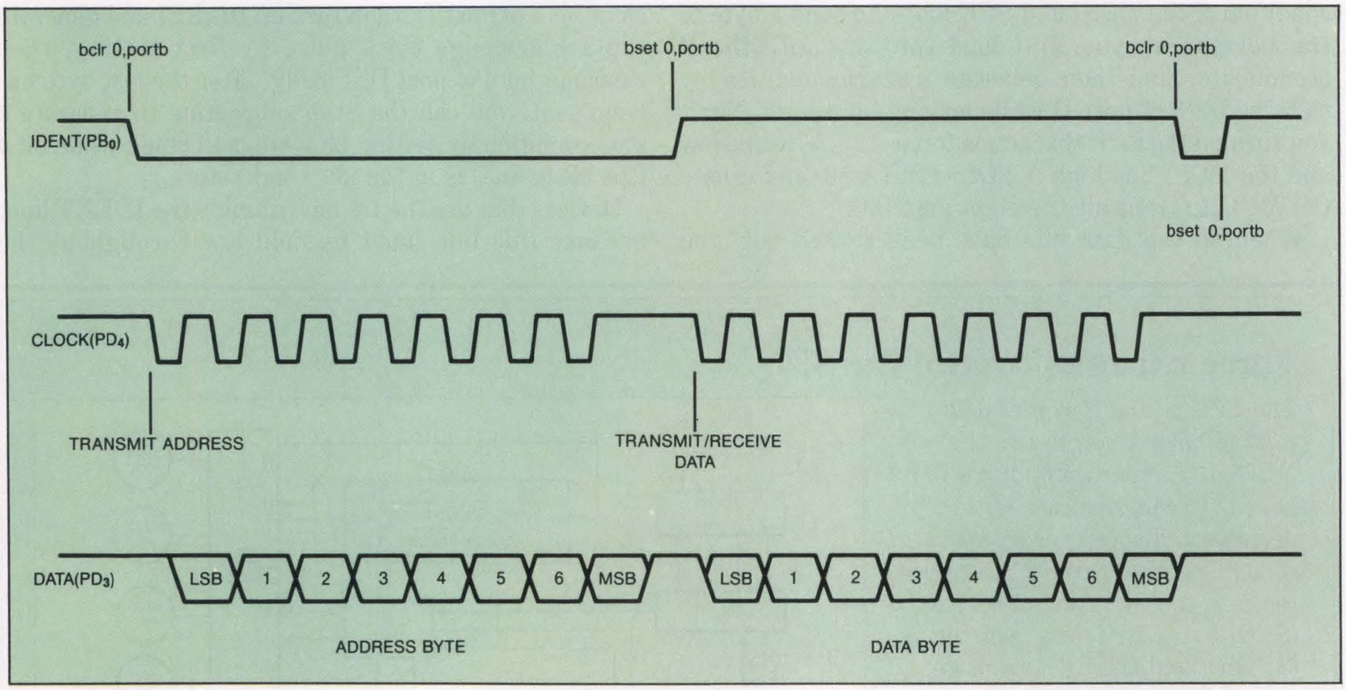

Fig 4—The IDENT line of ITT's line of Intermetall peripherals distinguishes *between addresses and data. As you can see from this timing diagram, you need a separate port to control the IDENT line.*

transmission of eight address bits and high while data is being read or written, you can't drive it from port D, which the SPI needs for serial data and shift clock pulses. Instead, drive the IDENT and other IM control lines from port B (**Listing 2** (pg 204), **Fig 4**).

You initialize the SPI with CPOL=CPHA=1. To send data to a peripheral, you force the IDENT line low and transmit the 8-bit peripheral address. Then, while holding IDENT high, you send (or read) the eight data bits. When all the address and data pairs have been sent, you drive IDENT low and then high again to create a short pulse, which generates a stop condition.

As with the IIC bus, you transmit FF_{HEX} to generate shift-clock pulses for a read operation; the resultant high on the MOSI line doesn't interfere with incoming data bits. Remember, too, that the IM bus requires that you transmit the LSB first, whereas the SPI requires the transmittal of the MSB first; to meet this condition, the "flip" subroutine of **Listing 2** reverses the bit order before you load a byte into the transmit shift register and after a complete byte has been assembled in the receive shift register.

Although the preceding diagrams and subroutine listings relate to specific peripherals, you can easily adapt the basic techniques to connect any peripheral of the IIC or IM families to the SPI bus of a 68HC11-based system. Conceivably, you can even apply the same principles to other families of serial peripherals to extend your options still further. **EDN**

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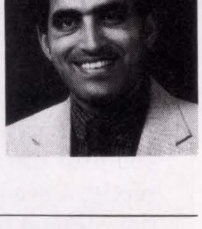
1. *MC68HC11A8 HCMOS Single-Chip Microcomputer, Technical Data Sheet MC68HC11A8/D*, Motorola Literature Distribution Ctr, Box 20912, Phoenix, AZ 85036.
2. Fenger, Carl K, "Bus links peripherals, multiple masters in low-speed network," *EDN*, April 3, 1986, pg 153.
3. *CCU 2000/2030 microcontroller data sheet*, ITT Corp.

Author's biography



At the time he wrote this article, Naji Naufel was an MCU applications engineer with Motorola (Austin, TX); since then he has become a product engineer responsible for testing 8-bit MCUs and improving yields. Naji holds a BSEE from the University of Texas. In his spare time, he enjoys tennis, photography, and flying radio-controlled model aircraft.

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LISTING 1—ICC BUS SUBROUTINE

```
*****************************************************************************
* This subroutine transfers a byte from the HC11's SPI to the IIC
*peripheral. Upon entry, data is in Acc B.
*w_start is the entry point for sending a start bit.
*nostart is the entry point for transferring data without a
*start condition.
*****************************************************************************
*
w_start        equ     *
               bclr    portd,x $08    start condition (bclr 3, portd)
nostart        equ     *
               ldaa    spcr,x
               oraa    #$40           enable SPI (SPE=1)
               staa    spcr,x
               bset    portd,x $08    return PD3 to idle state (bset 3,portd)
               stab    spdr,x         write data
wait           ldaa    spsr,x         wait for ewnd of transmission
               bpl     wait           SPIF not set, wait.
*
               bclr    portd,x $10    bclr 4,portd to leave SCLK (PD4) low
               ldaa    spcr,x         create ACK clock pulse
               anda    #$bf           clear SPE, disable SPI
               staa    spcr,x         causes PD4 to go high
*
               tst     ack            test acknowledge falg
               bne     hi_ack         keep ACK high
lo_ack         bclr    portd,x $08    else, clear ACK bit (bclr 3,portd)
               bsr     hi_ack         generate ACK clock
               bset    portd,x $08    bring ACK bit high (beset 3,portd)
               rts                    return to caller
*
hi_ack         bset    portd,x $10    generate ACK clock (bset 4,portd)
               brn     hi_ack         ensure clock-pulsse width
               bclr    portd,x $10    bclr 4,portd
               rts                    return to caller


*****************************************************************************
*This subroutine creates a stop condition
*****************************************************************************
*
stop           equ     *
               bclr    portd,x $08    bring SDA low (bclr 3,portd)
               bset    portd,x $10    bring SCL high (bset 4,portd)
               bset    portd,x $08    bring SDA high (bset 3,portd)
               rts                    return to caller
*****************************************************************************
* This subroutine sends an address byte, followed by a control
* byte in CONTROL
*****************************************************************************
*
addrcntl       equ     *
               ldab    #waddr         r/w=0
               bsr     w_start        send address with start condition
               ldab    control
               bsr     nostart        send control byte without start
               rts                    return to caller


*****************************************************************************
* This subroutine reads a data byte
*****************************************************************************
*
read           equ     *
               ldaa    #$00
               staa    control
               inca
               staa    ack            high ack bit (ack nonzero)
```

Listings continued on pg 204

LISTING 1—ICC BUS SUBROUTINE *(Continued)*

```
                jsr     addrcntl        send address/control bytes
                jsr     stop
                ldab    #raddr          r/w=1
                bsr     w_start         send address with start condition
                clr     ack             low ACK bit
                ldab    #$ff            and read 4 data bytes
                bsr     nostart         keep MOSI open-drain high
                ldaa    spdr,x          get received data
                staa    ram+2           HOURS
                ldab    #$ff
                bsr     nostart
                ldaa    spdr,x
                staa    ram+3           MINUTES
                ldab    #$ff
                bsr     nostart
                ldaa    spdr,x
                staa    ram+1           DAYS
                inc     ack             high ACK bit for last byte received
                ldab    #$ff
                jsr     nostart
                jsr     stop            end session
                lda     spdr,x
                staa    ram             MONTHS
                rts                     return to caller

*               END OF LISTING 1
****************************************************************************
```

LISTING 2—IM BUS SUBROUTINE

```
****************************************************************************
* This subroutine reverses the order of the bits in a byte. The input
* data is in Acc A, and the output is returned in Acc B. The action
* shifts the data out of the MSB side of Acc A into the MSB side of Acc B.
****************************************************************************
*
flip            equ     *
                ldab    #$08            do it 8 times
                stab    temp
again           asla
                rorb
                dec     temp
                bne     again
                rts

****************************************************************************
* This subroutine sends two bytes to the IM peripheral; the first byte
* is in ADDR, the second byte is in DATA.
****************************************************************************
*
im_send         equ     *
                ldx     #$1000          point X to register base address
                lda     ADDR            address register
                bsr     flip            reverse the bit order
                bclr    portb,x %00000001 clear IDENT (PB0)
                stab    spdr,x          send byte (address register)
                ldaa    DATA            get address
                bsr     flip
                brclr   spsr,x %10000000  wait for SP]I flag
                bset    portb,x %00000001 set IDENT (PB0)
                stab    spdr,x          send word
                brclr   spsr,x %10000000  wait for SPI flag
                bclr    portb,x %00000001
                bset    portb,x %00000001 toggle IDENT (PB0)
                rts                     return to caller

*               END OF LISTING 2
****************************************************************************
```

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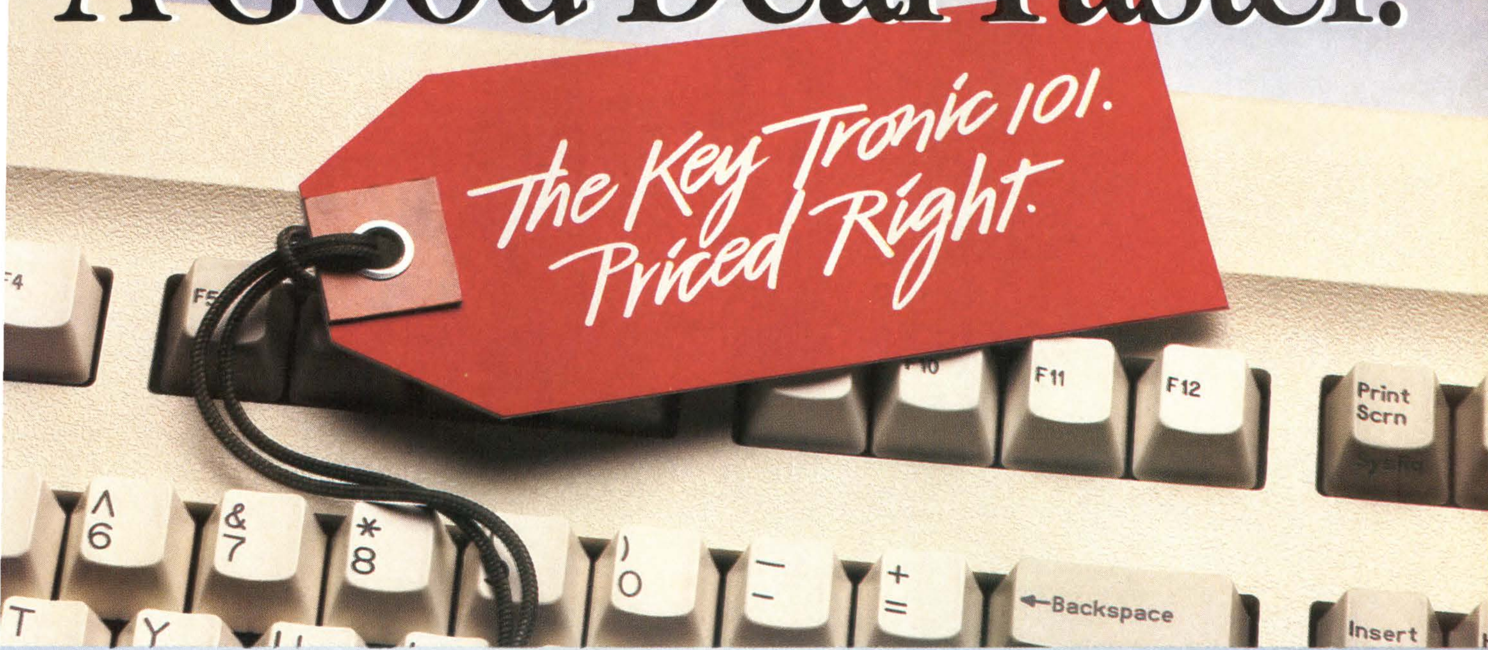

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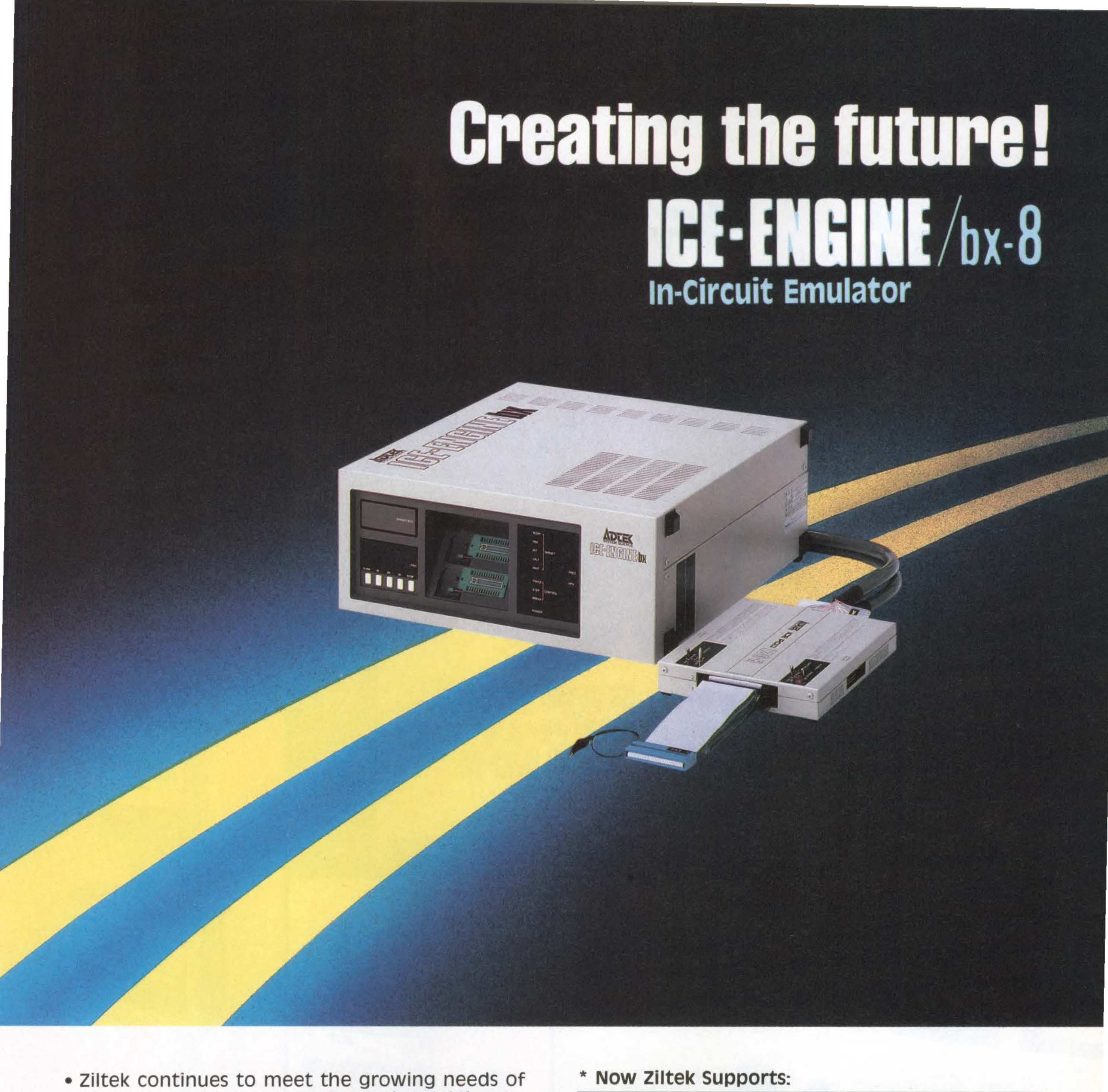
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Programmable-delay ICs control system timing

Low cost, low power, and small package size extend the application of digital-to-time converters in system timing applications. By exploiting the programmability features of these devices, you can both simplify timing-system design and gain greater control of timing parameters than you can by using analog time-delaying methods.

Craven Hilton and Jeff Barrow,
Analog Devices Inc

Accurate control of pulse timing is extremely important in digital electronic systems in those applications where system requirements dictate digital control of delays. Until now, you've had to use an analog method, employing a high-speed comparator to detect the incremental delays on a linear ramp, and a D/A converter to set the threshold level of the comparator. This design uses as much as one watt of power; now, however, monolithic digital-to-time converters (DTCs), such as the AD9500, accomplish the same function while only dissipating 300 mW. You can use the AD9500 to control time delays having intervals as small as 10 psec in a full-scale span of 2.5 nsec min.

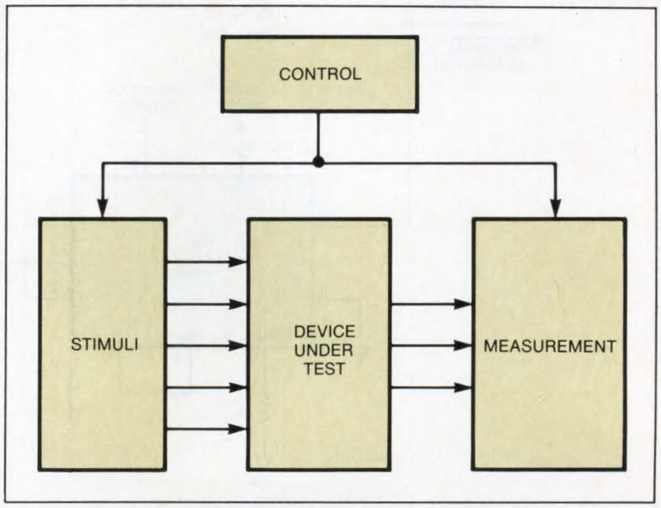

Fig 1—This test configuration, typical of virtually all electronic measurement systems, *comprises four blocks: stimuli, control, measurement, and the device under test.*

Some circuit examples illustrate the benefits of using a monolithic DTC in such applications as LSI and VLSI automatic test systems, which present significant challenges in pulse generation and distribution. For instance, although you can achieve repeatable delays of less than 100 psec by using an analog technique with an RC time reference, this method will not provide you with *variable* delays having such short intervals. The key to the flexibility of the monolithic DTC is the device's programmability.

Fig 1 is a generic block diagram of virtually all

By exploiting a DTC's programmability, you can simplify timing-system design and gain more precise control of timing parameters.

electronic measuring systems. Such a system can evaluate any device (the device under test, or DUT) for virtually any performance criteria if you apply the proper stimuli and use the appropriate measurement circuits. This electronic measuring system will serve as a model for the timing circuits throughout the remainder of the text.

One way to exploit the programmability of the DTC is to use two DTCs triggered from the same clock to program both the leading and trailing edges of an output pulse. This application is illustrated in **Fig 2a.** The first DTC (IC_1), which produces the leading edge of the output pulse, drives the clock input of IC_3, a D-type flip-flop whose D input is tied to a logic one. After IC_1

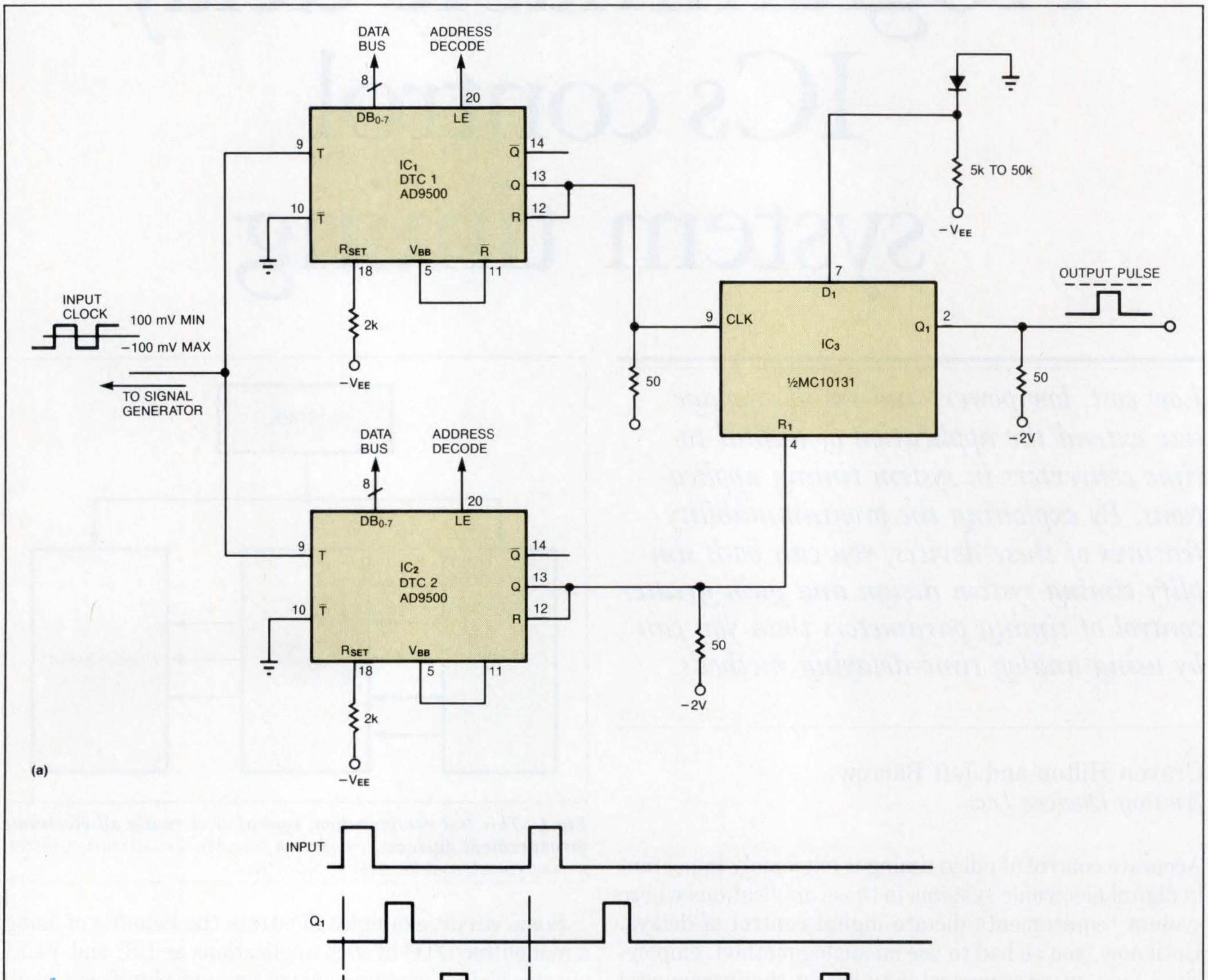

Fig 2—Two DTCs control the output's leading and trailing edges *in this digitally controlled pulse generator. The timing diagram in **b** brings out the fact that the leading edge of the output pulse, Q_O, occurs after an interval equal to the propagation delay plus the programmed delay.*

clocks the one through the flip-flop, the second DTC (IC_2) resets the flip-flop, thereby producing the falling edge.

At a time equal to the propagation delay plus the programmed delay of the first DTC (**Fig 2b**), the flip-flop produces the leading edge of the output pulse. Because the propagation delays of the two DTCs cancel each other, the width of the output pulse is exactly the difference between the programmed delays of the two DTCs. You can determine the programmed delay of each DTC from

$$t_D = t_{PD} + \frac{XX_{16}}{FF_{16}} (R_{SET}\ C_{SET}).$$

The circuit of **Fig 3** provides precise delay matching for those applications in which you need to distribute a

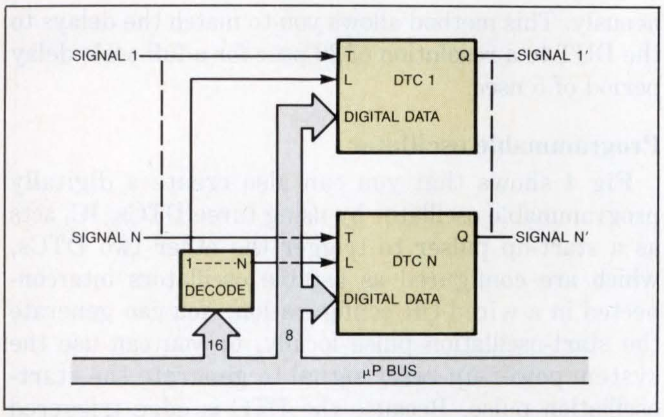

Fig 3—Providing precise delay matching in critical applications, *this circuit uses multiple DTCs to compensate for differences in the delays inherent in different signal paths. The closed-loop circuit provides a deskewing function.*

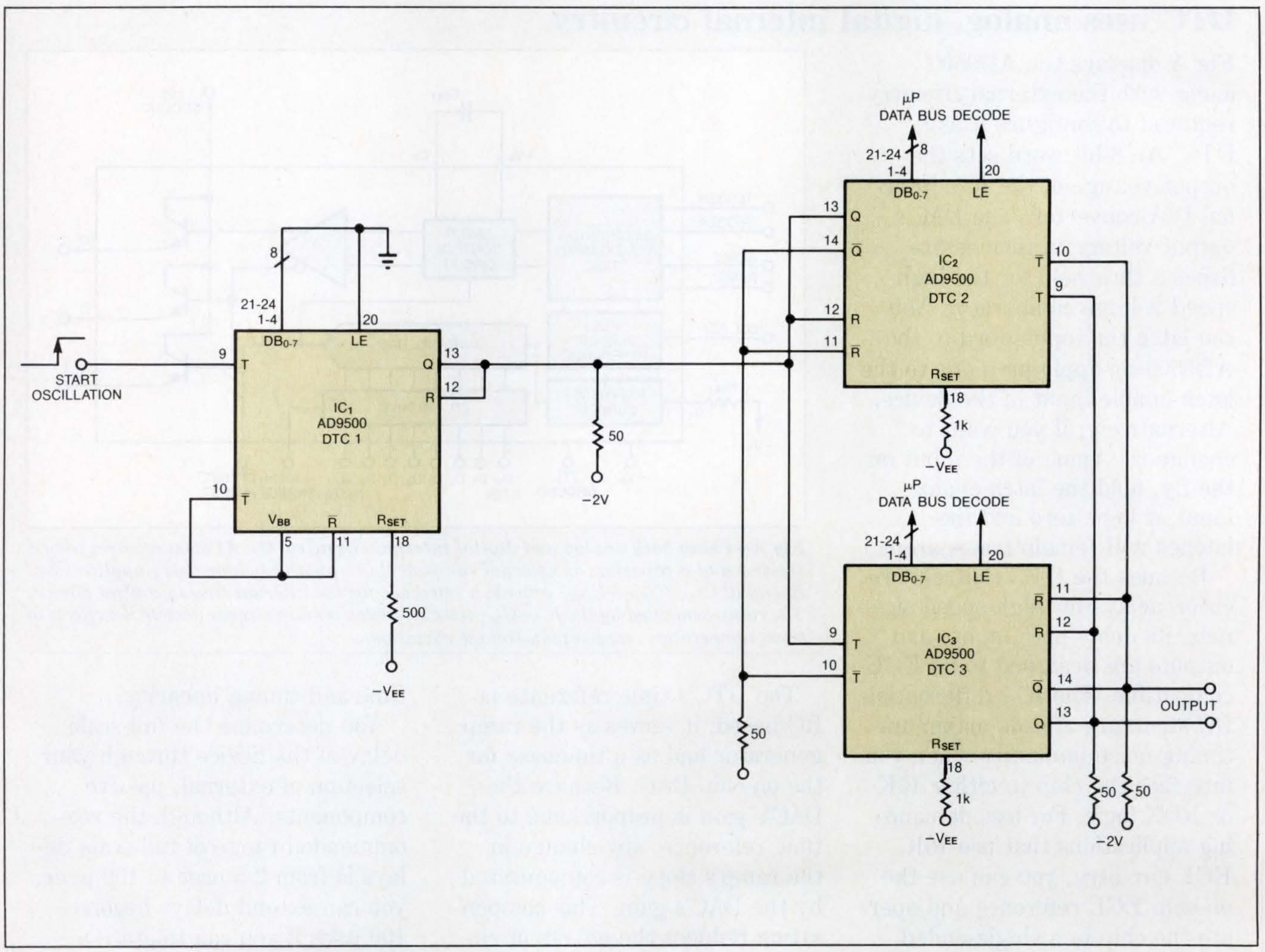

Fig 4—Using DTCs configured to start and stop the oscillation, *this digitally programmable oscillator gives you complete control over the start-up, shutdown, and frequency of oscillation.*

You can use multiple digital-to-time converters to construct oscillators, deskewing circuits, and accurate delay-measurement systems.

number of pulses and maintain good coherence between those pulses. Because individual test circuits may have extraneous delays in the signal paths to the DUTs, close matching in the initial tester delays will not be sufficient to guarantee close matching between the delivered pulses. The combination of programmable deskewing circuitry and the closed-loop calibration scheme of **Fig 3** allows you to compensate for the timing variations in the circuit paths during your test-system setup cycle.

During the setup cycle, the closed-loop system measures the delay to each input pin of the DUT. It then modifies the delay values stored in each of the DTCs until the input pulses arrive at the DUT's pins simultaneously. This method allows you to match the delays to the DUT to a resolution of 20 psec for a full-scale delay period of 5 nsec.

Programmable oscillator

Fig 4 shows that you can also create a digitally programmable oscillator by using three DTCs. IC_1 acts as a start-up pulser to trigger the other two DTCs, which are configured as astable oscillators interconnected in a wired-OR configuration. You can generate the start-oscillation pulse locally, or you can use the system power-up-reset signal to generate the start-oscillation pulse. Because the DTC is edge triggered and the oscillator is stable in either the oscillating or

DTC uses analog, digital internal circuitry

Fig A displays the AD9500 along with the external circuitry required to configure it as a DTC. An 8-bit word sets the output voltage of the IC's internal D/A converter. The DAC's output voltage in turn establishes a threshold for the high-speed voltage comparator. You can latch the input word to the AD9500 by applying a one to the latch-enable input of the device. Alternatively, if you want to change the value of the input on the fly, hold the latch-enable input at logic zero and the latches will remain transparent.

Because the DTC controls precision delays for high-speed signals, its delay-path inputs and outputs are designed to be ECL compatible. The IC's differential-I/O structure affords maximum timing-noise immunity when you interface the chip to either 10K or 100K logic. For less demanding applications that use 10K ECL circuitry, you can use the on-chip ECL reference and operate the chip in a single-ended mode.

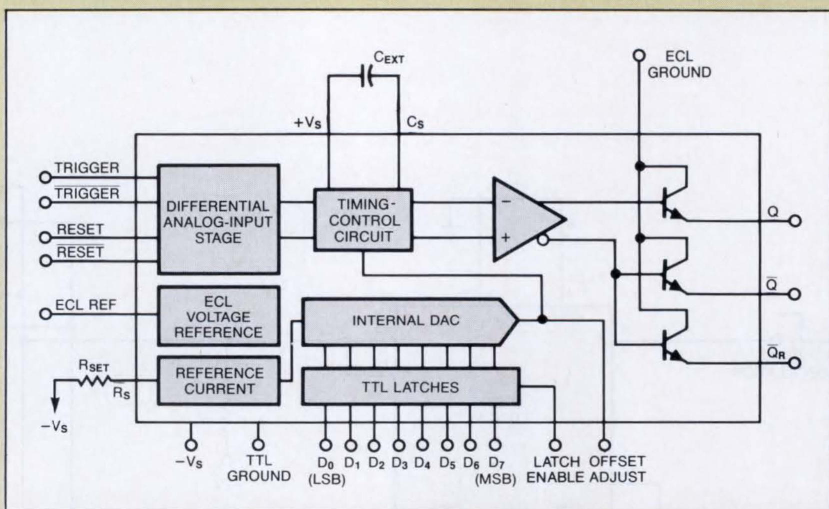

*Fig A—**Using both analog and digital internal circuitry,** the AD9500 requires only a resistor and a capacitor as external components in programmable-delay applications. R_{SET} and C_{SET} ($C_{EXT}+C_{INT}$) provide a reference for the internal timing-control circuit. The ramp generated by the R_{SET}/C_{SET} time reference remains linear despite the effects of time, temperature, and supply-voltage variations.*

The DTC's time reference is RC based; it serves as the ramp generator and as a timebase for the on-chip DAC. Because the DAC's gain is proportional to the time reference, any change in the ramp's slope is compensated by the DAC's gain. This compensation reduces the effects of environmental changes on full-scale time and timing linearity.

You determine the full-scale delay of the device through your selection of external, passive components. Although the recommended range of full-scale delays is from 2.5 nsec to 100 μsec, you can extend delays beyond 100 μsec if you can tolerate a degradation of the linearity and nonoscillating mode, a single pulse from IC_1 will start the oscillation. By grounding the trigger input on either IC_2 or IC_3, you can stop the oscillation.

As **Fig 4** shows, each DTC resets itself as it triggers the alternate DTC. The programmed delay of each device is determined by the equation given earlier. This delay, in turn, determines the output frequency of the oscillator, which is simply the reciprocal of the sum of the two propagation delays plus the two programmed delays.

When you need to measure a time delay, you can use two DTCs in conjunction with two comparators, a D-type flip-flop, and a successive-approximation register (SAR) as illustrated in **Fig 5a.** Flip-flop IC_3 serves as a coincidence detector. The first DTC (IC_1) varies the delay of the pulse applied to the D input of the flip-flop. The coincidence detector serves as a time comparator, whose function is analogous to that of a voltage comparator in a successive-approximation A/D converter.

The clock input to the flip-flop is delayed by a period equal to the unknown ECL delay. The circuit compares the first cycle of the 1-MHz clock with the unknown delay and checks to see if the delay is greater than half-scale. Then it checks for one-quarter or three-quarters scale, one-eighth or seven-eighths scale, and so on. At the end of the test process, then, the output of the SAR provides an 8-bit representation of the delay through the DUT. To measure TTL-circuit delays, you

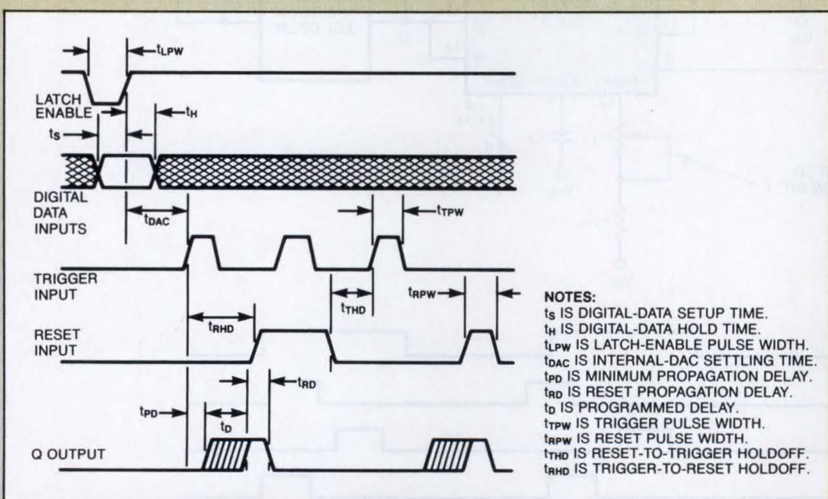

Fig B—Timing characteristics for the digital-to-time converter *are shown in this timing diagram. The illustration shows the relationship between the digital delay-coefficient data and the latch-enable strobe. The text delineates the limits you should observe for the various inputs, in order to obtain proper operation of the DTC.*

repeatability of the delay. At the other end of the spectrum, if you choose a full-scale range of 2.5 nsec, then the smallest incremental delay available to you is 10 psec.

The maximum delay trigger rate is 100 MHz, but an offset adjustment in the device allows you to operate two DTCs in a ping-pong fashion to double the trigger rate. The IC's maximum differential nonlinearity is $\pm\frac{1}{2}$ LSB at 25°C and ± 1 LSB over the operating-temperature range. Maximum integral nonlinearity for the device is ± 1.25 LSB for full-scale delays of 100 nsec or more over the operating-temperature range.

The timing characteristics of the AD9500 are illustrated in **Fig B.** Lines 1 and 2 show the timing relationship between digital-delay coefficient data and the latch-enable strobe. The minimum latch-enable pulse width is 2 nsec. The data setup time for the input latch is a maximum of 2.5 nsec, and the hold time is a minimum of 4.5 nsec. You must allow at least 25 nsec from the rising edge of the latch-enable pulse before you trigger an event, otherwise the internal DAC might not have time to settle.

Lines 3, 4, and 5 of **Fig B** show the relationship of the output to the reset and trigger events. The total delay through the DTC is the sum of the propagation delay and the programmed delay. The propagation delay equals the delay through the differential input stage, the comparator, and the delay attributable to ignoring the first, nonlinear portion of the ramp. The last of these components increases with full-scale delay.

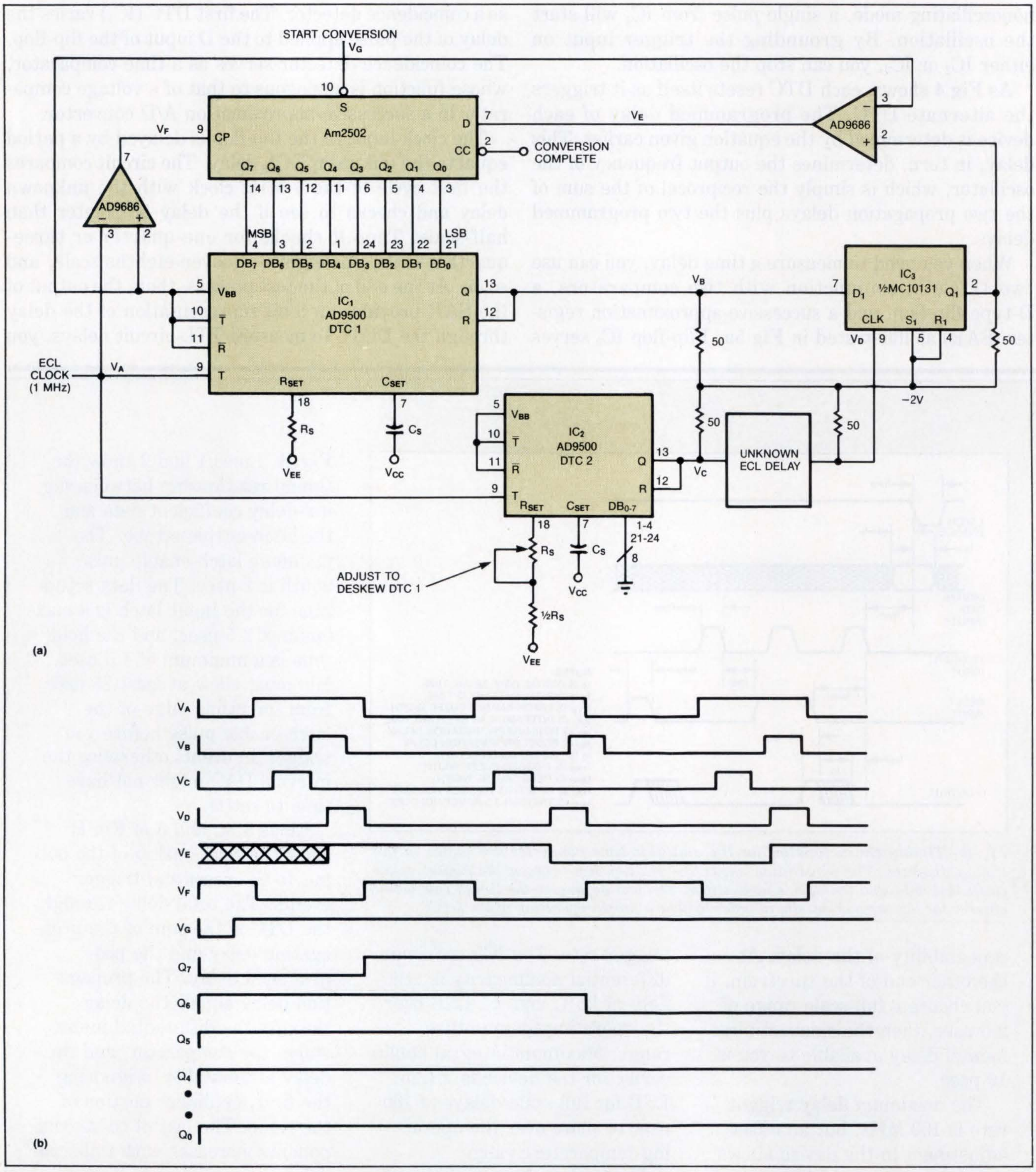

Fig 5—Operating in similar fashion to a successive-approximation A/D converter, *this circuit allows you to make precise delay measurements. The circuit in* ***a*** *handles ultrafast ECL circuitry; you can easily modify it to accommodate TTL circuits. The timing diagram in* ***b*** *illustrates the timing characteristics at various points in the circuit.*

A successive-approximation process in the time domain, similar to that commonly used in the voltage domain in ADCs, yields an accurate delay-measuring system.

add an AD9686 comparator between the Q output of the second DTC (IC_2) and the input to the unknown-delay circuit, and an AD96685 comparator between the output of the unknown-delay circuit and the flip-flop.

To calibrate the circuit of **Fig 5b,** you insert a shorting strap in place of the unknown-delay circuit to eliminate extraneous circuit delays and the flip-flop's setup time. To null the circuit, apply a digital code of 00_{16} to IC_2 and adjust potentiometer R_S. This adjustment varies the propagation delay through IC_2. The calibration is complete when the output of the SAR is also 00_{16}. You must apply start-conversion pulses during the calibration. This calibration procedure is equally valid for the modified, TTL-delay configuration. **Fig 5b** shows the timing for a typical conversion cycle.

You can use the circuit of **Fig 6a** to measure the settling time of analog signals—for example, the output of a D/A converter. The operation of this circuit is similar to the operation of the digital delay detector, but it uses a voltage-input window comparator in place

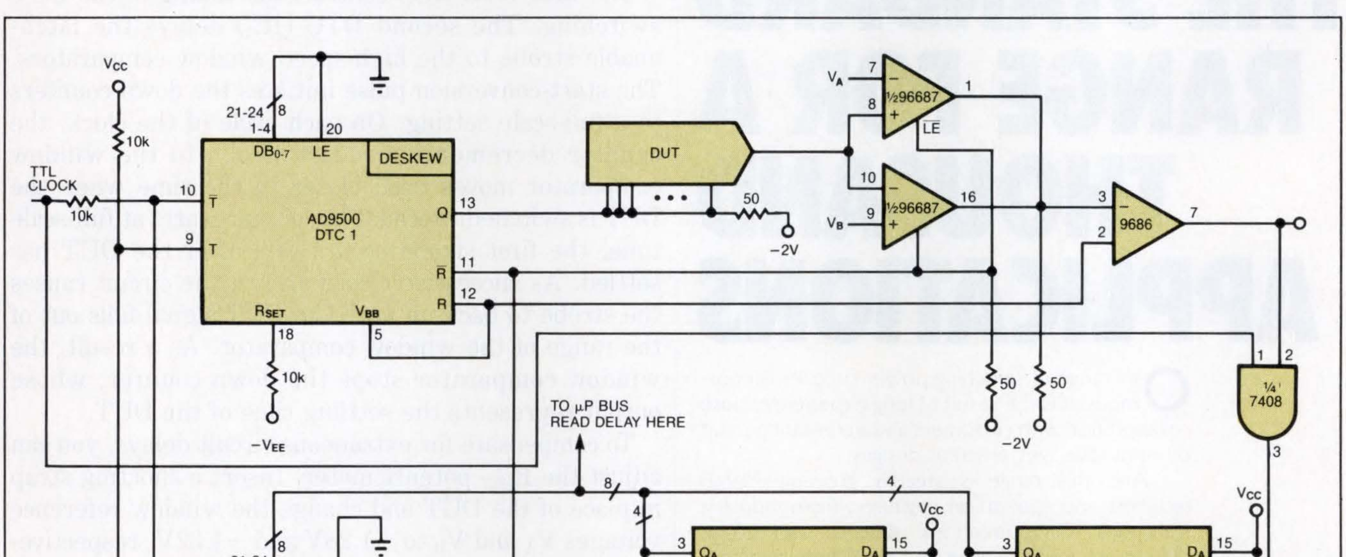

Fig 6—You can measure the settling time of analog signals by using the circuit in a. The operation of this circuit is similar to that of the digital delay detector in Fig 5a. A typical analog voltage-settling waveform is illustrated in b.

of the coincidence detector, and down counters in place of the SAR.

Fig 6b shows a typical analog voltage-settling waveform, as well as the output of a window comparator that uses a constant high-frequency strobe. This continuous-clock method produces ambiguous results because the signal comes into the error-band window during three clock periods. The circuit of **Fig 6a,** however, produces a single strobe per cycle of the analog signal and homes in on the correct measurement in the following manner.

The first DTC (IC_1) controls the timing of the DUT switching. The second DTC (IC_2) delays the latch-enable strobe to the high-speed window comparators. The start-conversion pulse initiates the down counters to a full-scale setting. On each cycle of the clock, the counter decrements and the strobe to the window comparator moves back closer to the time when the DUT is switched. Because the circuit starts at full-scale time, the first strobe occurs well after the DUT has settled. As successive clocks arrive, the circuit causes the strobe to back up until the DUT signal falls out of the range of the window comparator. As a result, the window comparator stops the down counter, whose output represents the settling time of the DUT.

To compensate for extraneous circuit delays, you can adjust the R_{SET} potentiometer. Insert a shorting strap in place of the DUT and change the window reference voltages V_A and V_B to $-1.28V$ and $-1.32V$, respectively. Then adjust R_{SET} until you receive a zero output from the down counters. When you reset the voltages for the window around the DUT's output and the conversion takes place, the output of the down counter will represent the propagation delay plus the settling time of the DUT. **EDN**

Authors' biographies

Craven Hilton is a marketing engineer at Analog Devices Inc's Computer Labs Div (Greensboro, NC). An AAS graduate of the Technical College of Alamance, he's worked at ADI for 11 years. Craven's spare-time activities include golf and aquatic sports.

Jeff Barrow is a senior design engineer in charge of designing high-speed analog ICs at ADI's Computer Labs Div. A 6-year employee at ADI, he obtained a BSEE from the University of Arizona. Jeff is a member of IEEE and Tau Beta Pi. His hobbies include astronomy, mathematics, and woodworking.

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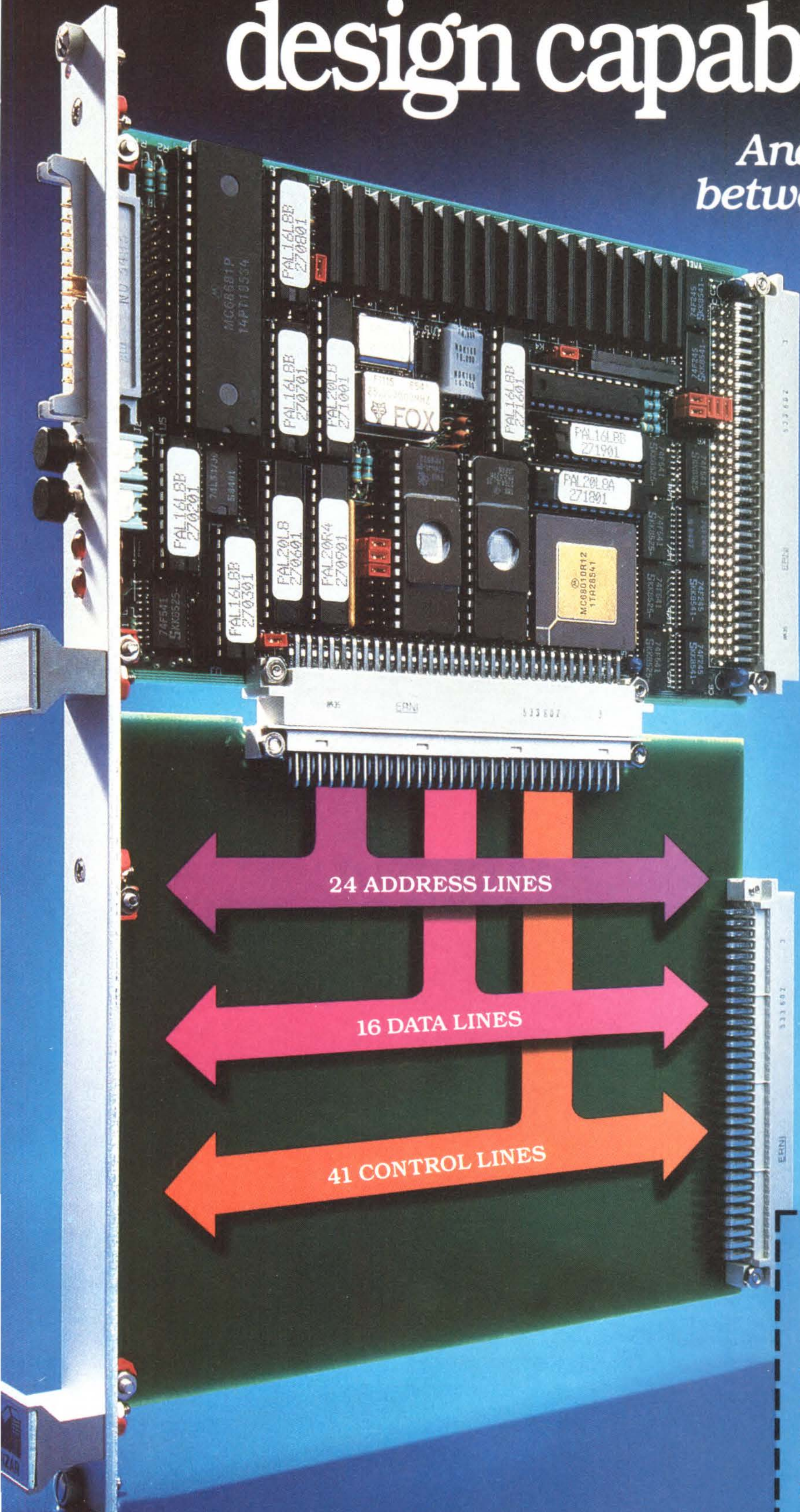

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Precision comparators ease oscillator and data-converter design

To simplify the task of designing high-performance circuits such as a crystal oscillator, V/F converters, A/D converters, and an ATE pin receiver, you can use a comparator that combines low bias current, high gain, high speed, and 3-state outputs.

John Dutra and Barry Harvey, *Elantec Inc*

Over the years, analog designers have come to regard voltage comparators much as in the old saying about persons of the opposite gender: "You can't live with them, but you can't live without them." Comparators have a well-deserved reputation for being temperamental. For example, most comparators have a tendency to oscillate, which can cause them to yield meaningless results. One way to defend your products from the effects of such unseemly behavior is to lavish exquisite care on the comparators, both in analyzing and designing the circuits that use them and in laying out the pc boards that house them. For instance, you must drive the comparators from low-impedance sources, and you must be careful to connect bypass capacitors to the proper circuit-ground point.

To simplify the task of obtaining valid comparisons at high speed in such demanding applications as data converters and oscillators, you can employ fast, low-bias-current comparators such as the EL2018 and EL2019. These comparators don't require the lavish care that their more temperamental counterparts do, and you can use them effectively in such applications as

- A crystal oscillator
- A pair of V/F converters, each having 0.01% of full-scale rms nonlinearity relative to the best-fit straight line, and a maximum output frequency you can set higher than 10 MHz
- Two 12-bit successive-approximation A/D converters, one of which has 1.5-μsec total conversion time
- A high-voltage pin receiver with output multiplexing, such as those found in some automatic test systems.

Fig 1 shows a crystal oscillator that oscillates at the crystal's 20-kHz to 20-MHz series-resonant frequency. It uses the EL2018 as a high-gain, wideband linear

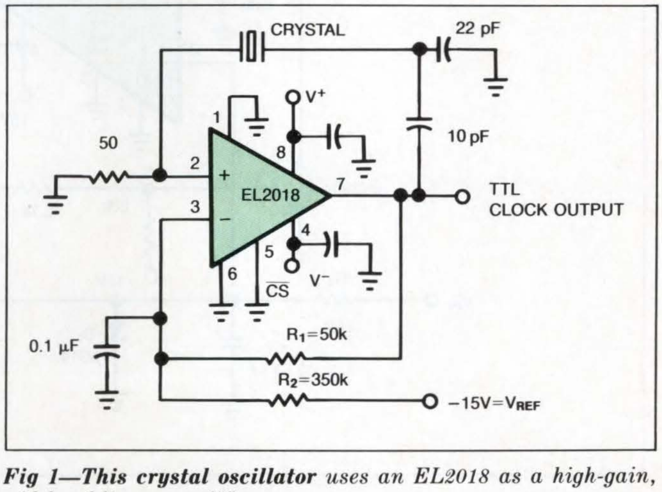


***Fig 1—This crystal oscillator** uses an EL2018 as a high-gain, wideband linear amplifier.*

Most comparators have a tendency to oscillate, which can cause them to yield meaningless results.

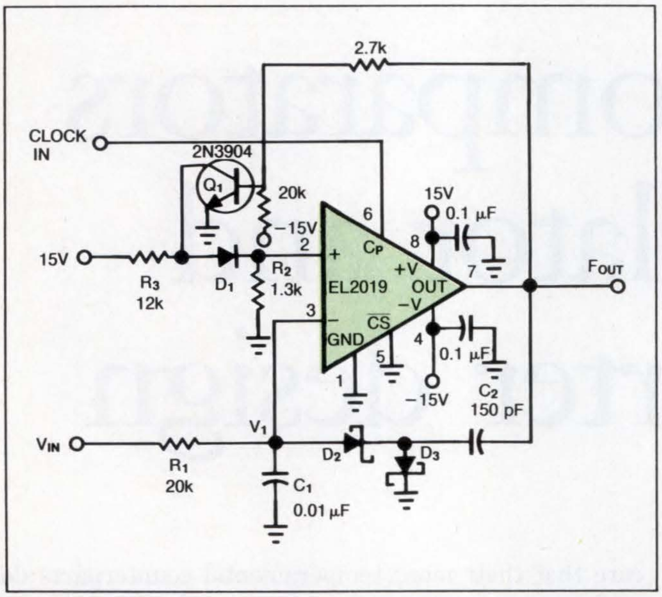


***Fig 2—This simple V/F converter** is based on the charge-balancing principle. The converter uses only one IC—an EL2019 comparator.*

amplifier. Compared with simpler oscillators, this circuit provides superior immunity to load and power-supply variations. It loads the crystal with 50Ω in series with 32 pF, the preferred values for many crystals. DC feedback via R_1 and R_2 holds the comparator's negative input at 0V. By adjusting R_1, R_2, or V_{REF}, you can maintain the required voltage at the comparator's negative input while causing a small variation in the output duty cycle. If you choose R_1, R_2, or V_{REF} incorrectly, the circuit may oscillate at a subharmonic of the desired frequency.

V/F converter's clock input can reach 25 MHz

The circuit shown in **Fig 2** is a charge-balancing V/F converter whose output is a pulse train with a repetition rate proportional to the input voltage. Although you can control the output frequency, you can't control the shape of the output pulses. Except as a second-order effect, the frequency of the circuit's clock input does not affect the V/F-conversion scale factor; the

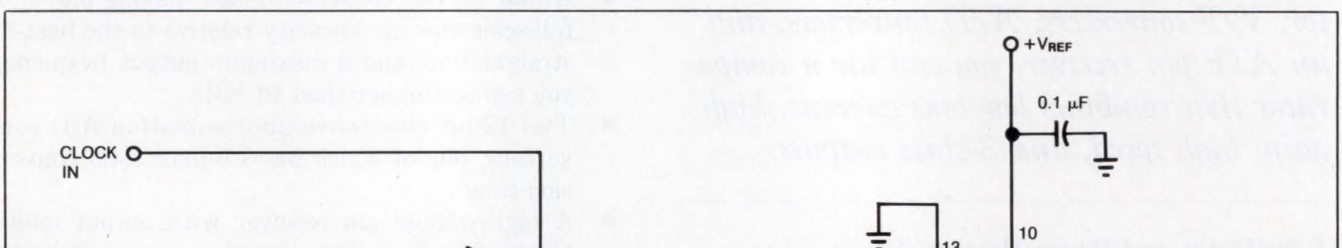


***Fig 3—Adding an analog switch** to Fig 2's V/F converter improves the circuit's temperature sensitivity.*

clock frequency does establish an upper limit for the output pulse rate—the maximum output rate is half the clock frequency. You can use a clock whose frequency is as high as 25 MHz, and the circuit will make conversions with 0.01% of full-scale rms nonlinearity relative to the best-fit straight line.

The EL2019's output can change state only at positive-going clock edges. Normally, the comparator's output is in the high state, V_{OH}, and Q_1 is saturated, so no current flows in D_1. The comparator's positive input is, therefore, essentially at ground potential, and the comparator compares the voltage at its negative input (the summing node, V_1) to ground. If you apply a positive input, node V_1 goes positive, causing the comparator output to drop to the low state, V_{OL}, at the next positive-going clock edge. The low comparator output turns Q_1 off and allows the voltage at the comparator's positive input to rise to approximately 1.4V. In no event can the summing node become as positive as 1.4V, because Schottky diodes D_2 and D_3 will clamp it at a lower voltage. Therefore, the differential voltage at the comparator input will cause the comparator output to return to V_{OH} at the next positive-going clock edge.

Charge-balancing action occurs when the comparator output drops from V_{OH} to V_{OL}. When the comparator output is at V_{OH}, C_2 charges to $V_{OH}-V_{D3}$. When the comparator output drops to V_{OL}, current flows through C_1, D_2, C_2, and the comparator's output stage, causing charge to redistribute itself between C_1 and C_2. Because C_1 is much larger than C_2, the change in voltage across C_1 will be much smaller than the change in voltage across C_2.

When a charge is delivered through D_2, the initial current is on the order of several milliamps, but it sags within tens of nanoseconds and continues to decay thereafter. Short clock pulses limit the time for charge to transfer fully to C_1, thus making the scale factor slightly clock-rate dependent at high frequencies.

Diode drops cause temperature sensitivity

The output frequency is given by the equation:

$$F=V_{IN}\div[R_1C_2(V_{OH}-V_{OL}-V_{D3}-V_{D2})]$$

where R is in ohms, C is in farads, and F is in hertz. Note that although C_1 doesn't appear in the equation, you don't have complete freedom in selecting it. C_1 must be much larger than C_2, but it must not be so large that the change in voltage across C_1 during a single clock cycle (which is approximately equal to the change in voltage across C_2 multiplied by C_2/C_1) is small compared to the comparator's noise level. The tradeoff in C_1's value is that it should not be so large that it takes too much time to count and average the output pulses, but it should not be so small that it causes excessive output frequency jitter. If the input signal is so large (or C_1 is so small) that in a single clock period C_1 charges to the point where D_2 and D_3 conduct, the output will not latch. The pulse rate will rise to its maximum possible value—half the clock frequency.

The clock frequency can be as high as 25 MHz for V/F linearity of 0.01% of full scale. The voltage-to-frequency conversion remains linear for output frequencies about as high as 45% of the clock frequency. The circuit's input-offset voltage is predominantly that of the EL2019. The V/F scale factor is reasonably constant over temperature, because of the constant logic levels at the EL2019 output and the low voltage drop across the Schottky diodes, D_2 and D_3. These diodes are the major source of calibration sensitivity to f_{CLOCK}.

Use analog switch to improve stability

Fig 3 shows an improved version of the V/F-converter circuit. In **Fig 3**'s circuit, a DG303A analog switch is used as a dpdt switch to connect C_2 either from V_{REF} to ground or from ground to the summing node. For **Fig 3**,

$$SF\approx V_{REF}\times R_1\times C_2.$$

Charge transfer between the drive and signal portions of the analog switch is the major error source in this circuit. Note that **Fig 3**'s scale-factor expression, unlike that of **Fig 1**, contains no temperature-dependent terms.

Fig 4a shows the schematic of a 12-bit successive-approximation A/D converter. The 25HCT04 is faster than the traditional 2504 successive-approximation register, and the AD565A D/A converter provides a typical 150-nsec settling time at the summing junction. The EL2018 provides a 20-nsec typ response time and draws only 0.2 LSB of bias current. The required output swing of 0.8 to 2.0V, divided by the voltage gain of 40,000, yields an input uncertainty of only 0.02 LSB, which is less than the system noise and the comparator's thermal noise. A breadboard of this circuit had only about 0.1 LSB of noise, peak to peak.

Fig 4b shows that the maximum delay times of the components yield a 4-μsec worst-case conversion time. In practice, the breadboard version of this circuit achieves its specified accuracy at a conversion time as

One way to defend your circuits from comparators' unseemly behavior is to lavish exquisite care on the comparators.

short as 2.5 μsec with no resistance at the summing junction, and 1.8 μsec with 3.9 kΩ from summing junction to ground; the circuit's noise is still acceptable.

Star grounds don't work at these speeds, so the breadboard employs a copper ground plane with all wires draped physically close to the plane. The analog

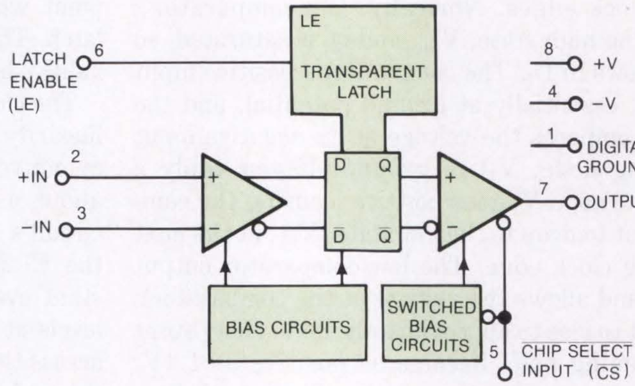
Flip-flop succeeds where latch often failed

You can model the EL2018 as an input comparator followed by a simple logic latch that's followed in turn by an output 3-state TTL buffer **(Fig A).** The EL2019 replaces the latch with a full master/slave flip-flop—the input and output stages are the same as those in the EL2018 **(Fig B).**

High-speed comparators have traditionally had output latches. The latches aren't just for data storage; their purpose is to help suppress oscillations. Clearly, when a comparator's latch is set to latch mode, no coupling from output to input can ever cause sustained oscillation. Generally, you need to hold the latch in transparent mode for only a short time (in comparison with the time it would take a signal to propagate through the comparator IC.) Thus, a quick pulse on the latch-enable pin allows the latch to capture new data without connecting the output to the input long enough for the comparator to build up an oscillation.

A significant problem with the latch enable is that it can influence the comparator's decision no matter what you do to prevent such influence—it is, after all, an analog input to an analog circuit element. Even though you just want it to strobe the output, it does more—all too often it affects the accuracy of the comparisons.

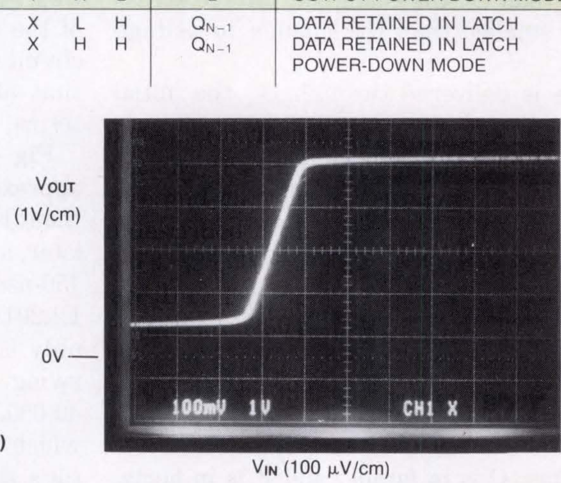
A master/slave flip-flop, as in the EL2019, solves the problem



(a)

FUNCTION TABLE

INPUTS (TIME N−1)				INTERNAL Q	NOTES	OUTPUT
+IN	−IN	$\overline{CS}$	LE			
+	−	L	L	H	NORMAL COMPARATOR OPERATION	H
−	+	L	L	L		L
+	−	H	L	H	INTERNAL NORMAL COMPARATOR OPERATION	HIGH Z
−	+	H	L	L	OUTPUT POWER-DOWN MODE	HIGH Z
X	X	L	H	Q_{N-1}	DATA RETAINED IN LATCH	Q_{N-1}
X	X	H	H	Q_{N-1}	DATA RETAINED IN LATCH POWER-DOWN MODE	HIGH Z



(b)

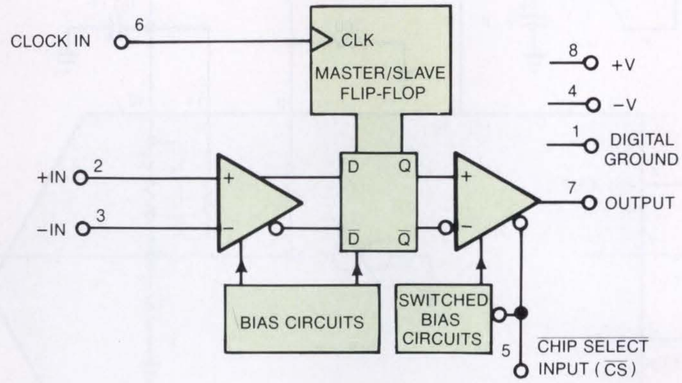
Fig A—The EL2018 comparator ***(a)*** *has three major sections—an input comparator followed by a simple logic latch, which is followed in turn by an output 3-state TTL buffer. The transfer function of the comparator* ***(b)*** *shows that an input voltage change of approximately 100 μV causes an output change of approximately 4V, which is a voltage gain of approximately 40,000.*

circuitry is located in one compact region away from all digital lines, and the comparator output is routed with rigid coaxial cable to prevent noise feedback. During the conversion, the current drawn from the signal source by the A/D input varies rapidly. To prevent these current fluctuations from destroying the conver-

altogether. At no condition of the clock input can an analog signal pass through the device. Rather, a comparison of the inputs propagates to the output only after a positive-going clock edge; the analog input is completely quantized as the digital output.

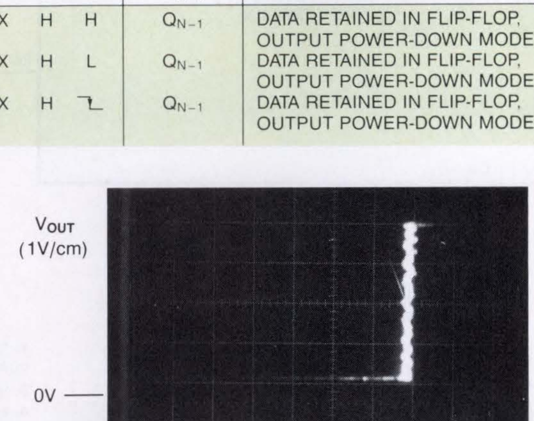
The master/slave configuration offers other benefits as well. Because the analog input requires about 4 nsec of input setup time before the clock edge, the clock edge itself can't influence the analog comparison. That is, the clock edge has a zero setup time and the comparator ignores it because it doesn't meet the setup requirement. Latched comparators, in contrast, allow both clock edges to influence the analog output.

The master/slave flip-flop gives the comparator virtually infinite gain; that is, a very small input can determine a full logic-output swing. In fact, the small input noise of the EL2019 ($5\ nV/\sqrt{Hz}$ yields $30\ \mu V$ rms thermal noise) is greater than any measured gain error. You can say that the EL2019 has only offset and thermal noise errors, which is a boon to A/D conversion. Finally, in many comparator applications, such as delta modulators, an external flip-flop follows the comparator; in such circuits, the EL2019 saves external components.



FUNCTION TABLE

INPUTS (TIME N−1)				INTERNAL Q (TIME N)	NOTES	OUTPUT (TIME N)
+IN	−IN	$\overline{CS}$	CLK			
+	−	L	↑	H	NORMAL COMPARATOR OPERATION WITH D FLIP-FLOP	H
−	+	L	↑	L		L
+	−	H	↑	H	NORMAL COMPARATOR OPERATION WITH D FLIP-FLOP; POWER-DOWN MODE	HIGH Z
−	+	H	↑	L		HIGH Z
X	X	L	H	Q_{N-1}	DATA RETAINED IN FLIP-FLOP	Q_{N-1}
X	X	L	L	Q_{N-1}	DATA RETAINED IN FLIP-FLOP	Q_{N-1}
X	X	L	↓	Q_{N-1}	DATA RETAINED IN FLIP-FLOP	Q_{N-1}
X	X	H	H	Q_{N-1}	DATA RETAINED IN FLIP-FLOP, OUTPUT POWER-DOWN MODE	HIGH Z
X	X	H	L	Q_{N-1}	DATA RETAINED IN FLIP-FLOP, OUTPUT POWER-DOWN MODE	HIGH Z
X	X	H	↓	Q_{N-1}	DATA RETAINED IN FLIP-FLOP, OUTPUT POWER-DOWN MODE	HIGH Z



(b)

Fig B—The EL2019 (a) is similar to the EL2018, except that it replaces the EL2018's latch with a full master/slave flip-flop. The transfer function of the EL2019 (b) exhibits essentially infinite voltage gain because of the EL2019's master/slave flip-flop.

Fast, low-bias-current comparators can simplify the task of obtaining valid comparisons at high speed in demanding applications.

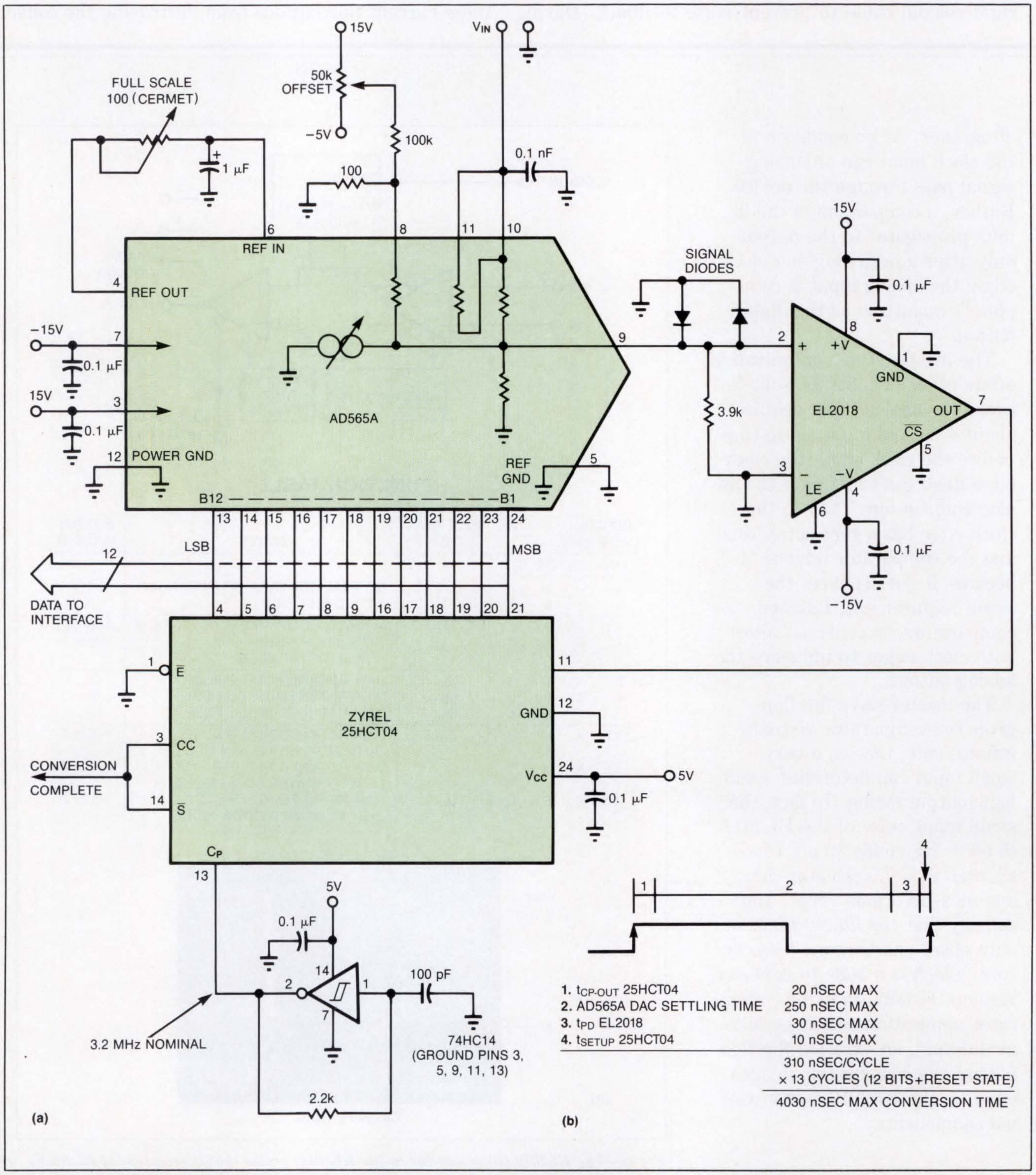


***Fig 4—A 12-bit successive-approximation A/D converter (a)** that uses the EL2018 and an AD565 D/A converter achieves a 4-μsec total conversion time. The timing diagram for this circuit **(b)** shows that D/A-converter settling consumes approximately 80% of the total time.*

sion accuracy, the signal source must maintain a constant output level, so the signal source must have low ac output impedance and must be local to the analog section. Incidentally, it's not at all necessary or useful to clamp the D/A output with Schottky diodes; inexpensive 1N914s perform quite satisfactorily.

The A/D converter of **Fig 5a** uses the TRW TDC1012, one of the fastest monolithic TTL-input, 12-bit D/A converters available. The converter's output current is 0 to −40 mA. Few practical amplifiers can support 12-bit accuracies with 40 mA of load current; therefore, a 25Ω load resistor converts the current to a −1V signal, which fits comfortably within the DAC's output compliance. When the DAC's full-scale output is

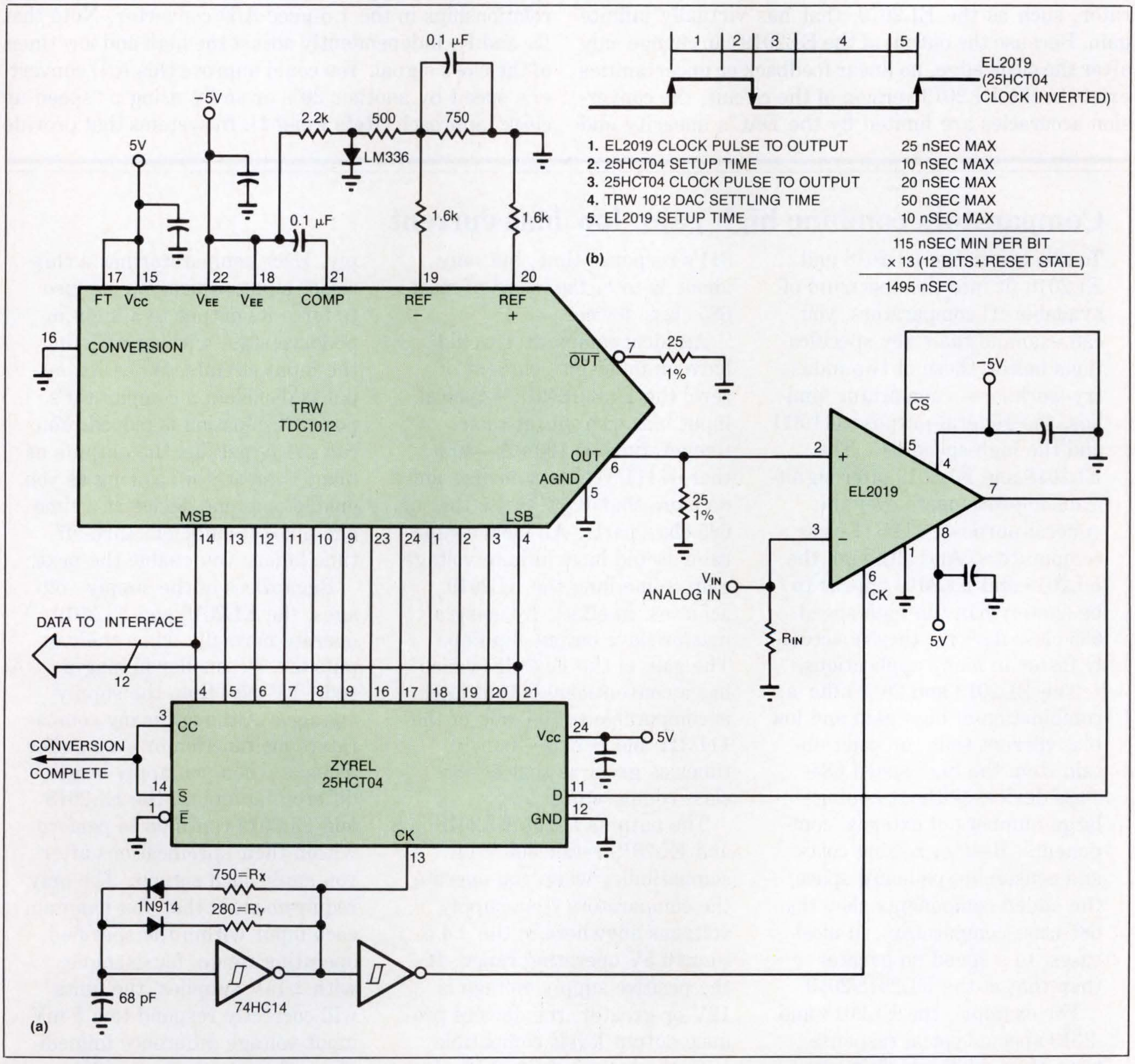


Fig 5—You can design an A/D converter (a) *capable of performing a complete 12-bit conversion in 1.5 μsec by using an EL2019 comparator, a TDC1012 D/A converter, and a high-speed successive-approximation register. The timing diagram* ***(b)*** *shows that the 1.5-μsec converter's settling time is only approximately 40% of the total.*

You can use fast, low-bias-current comparators in such applications as a crystal oscillator, data converters, and a high-voltage pin receiver.

1V, the LSB value is 244 μV, which is clearly a very small signal for the comparator to resolve. When an EL2018 with its latch permanently enabled is substituted for the EL2019 in this design, the small signals drive the EL2018 output into its linear operating output range, and code feedback causes errors of several LSBs.

You can overcome these difficulties by using a comparator, such as the EL2019, that has virtually infinite gain. Because the output of the EL2019 can change only after the clock edge, no linear feedback or uncertainties exist. In the EL2019 version of the circuit, the conversion accuracies are limited by the DAC's linearity and the noise of the EL2019's front end. Further, because of the EL2019's master/slave flip-flop, the circuit's timing relationships are precisely defined and synchronous clock noise is eliminated (see **box,** "Flip-flop succeeds where latch often failed").

The clock of the 1.5-μsec A/D converter has an unusual duty cycle. You can see the need for this duty cycle by referring to **Fig 5b**, which shows the timing relationships in the 1.5-μsec A/D converter. Note that R_X and R_Y independently adjust the high and low times of the clock signal. You could improve this A/D converter's speed by another 20% or so by using a "speed-up clock" approach **(Refs 1** and **2).** In systems that provide

Comparators combine high gain, low bias current

To see where the EL2018 and EL2019 fit into the spectrum of available IC comparators, you can examine their key specifications beside those of two industry-workhorse comparator families, the general-purpose 111/311 and the high-speed 685. The EL2018 and EL2019 offer significant improvements over the general-purpose, 111/311-class comparators. And although the EL2018 and EL2019 appear to be slower than the high-speed, 685-class devices, they're actually faster in many applications.

The EL2018 and 2019 offer a combination of high gain and low bias current that you can't obtain from the high-speed 685-class devices without adding large numbers of external components. Besides raising costs and consuming pc-board space, the added components slow the 685-class comparators, in most cases, to a speed no greater than that of the EL2018/2019.

For example, the EL2018 and -2019 spec a typical response time of 20 nsec, which is approximately 10 times as fast as the 311's response time, but only about ½ to ¼ the speed of most 685-class devices.

An ideal comparator would have an input bias current of zero; the EL2018/2019's typical input bias current (at room temperature) is 100 nA—40% that of 111/311-class devices and no more than 0.5% to 1% that of 685-class parts. An ideal comparator would have infinite voltage gain, something the EL2019 achieves, in effect, by using a master/slave output flip-flop. The gain of the EL2018, which has a conventional output latch, is comparable to the gain of the 111/311 and is more than 10 times as great as that of 685-class comparators.

The outputs of the EL2018 and EL2019 retain full TTL compatibility when you operate the comparators from supply voltages anywhere in the ±4.5 to ±16.5V operating range. If the positive supply voltage is 12V or greater, the devices produce output levels compatible with the inputs of CMOS logic devices operating from a 5V supply. Each comparator has a chip-select input, which you can use to force its output to a high-impedance state without affecting the input circuits. When its output is disabled, a comparator's power dissipation is halved. You can safely parallel the outputs of many comparators as long as you enable only one device at a time and allow it sufficient turn-off time before you enable the next.

Regardless of the supply voltages, the EL2018 and EL2019 operate normally when their inputs are 3V smaller in magnitude (2V typ) than the supply voltages. Although many comparators malfunction or even suffer damage when you apply large differential inputs, the EL2018 and EL2019 continue to perform within their specifications after you apply such signals. The only requirement is that you maintain each input within the specified operating range; for example, with ±15V supplies, the units will correctly respond to a 5-mV input-voltage difference immediately after you remove a 24V (26V typ) differential input.


AUGAT

A crystal oscillator that uses the EL2018 comparator as a high-gain, wideband linear amplifier can provide superior immunity to load and supply variations.

higher analog input voltages, the comparator would let you extend the circuit's resolution to 16 bits.

Some unusual properties of the EL2018 and EL2019 can prove useful in such applications as a pin receiver for automatic test equipment **(Fig 6)**. For example, the comparators' input stages can handle signals as large as ±12V in any combination, and the comparators have 3-state output capability, which can halve the device's power dissipation while maintaining input circuits in the active mode. (See **box,** "Comparators combine high gain, low bias current.")

In **Fig 7**'s circuit, when $\overline{CS}$ (pin 5) is at V_{IH}, the device's output impedance is high and the supply current is 50% of its active-output value, yet the input stage and latch continue to function, allowing you to clock multiple comparators simultaneously and read the outputs sequentially. The ability to capture data on many lines at a time and read it back sequentially is useful in large test systems, which may have as many as 1000 comparators, only 10% of which are active at one time.

The 50Ω resistors in series with the outputs of each comparator limit the fault currents, which can flow because the output stage of the comparator turns on faster than it turns off. Without the current-limiting resistors, the aforementioned output-stage characteristic could cause momentary short circuits across the comparator's power-supply lines. You can clock the input latch at speeds as high as 30 MHz, and you can scan the outputs at a 5-MHz rate. **EDN**

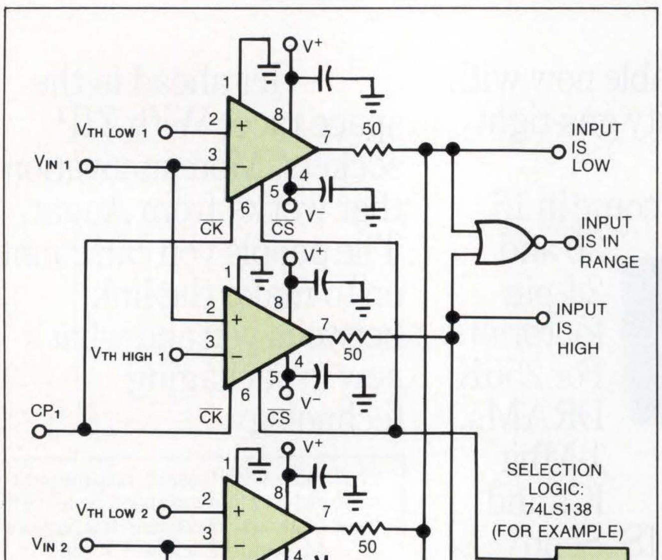


***Fig 6—This multiplexed ATE pin receiver** takes advantage of the comparators' 3-state outputs to capture the states of many analog signals simultaneously and read them back sequentially.*

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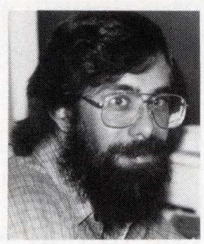
Authors' biographies

Jon Dutra is currently applications manager at Elantec (Milpitas, CA). He holds a BSEE from California State Polytechnic University at San Luis Obispo, an MSEE from the University of California at Davis, and an MBA from the University of California at Berkeley. In his spare time he enjoys amateur radio, flying, and teaching his new son old tricks.



Barry Harvey is a senior design engineer for high-speed analog ICs at Elantec. He previously worked for Precision Monolithics, Siliconix, and AMD. He holds an MSEE from Stanford University and has been granted two patents. In his spare time, he enjoys running, playing guitar and mandolin, and programming his personal computer.

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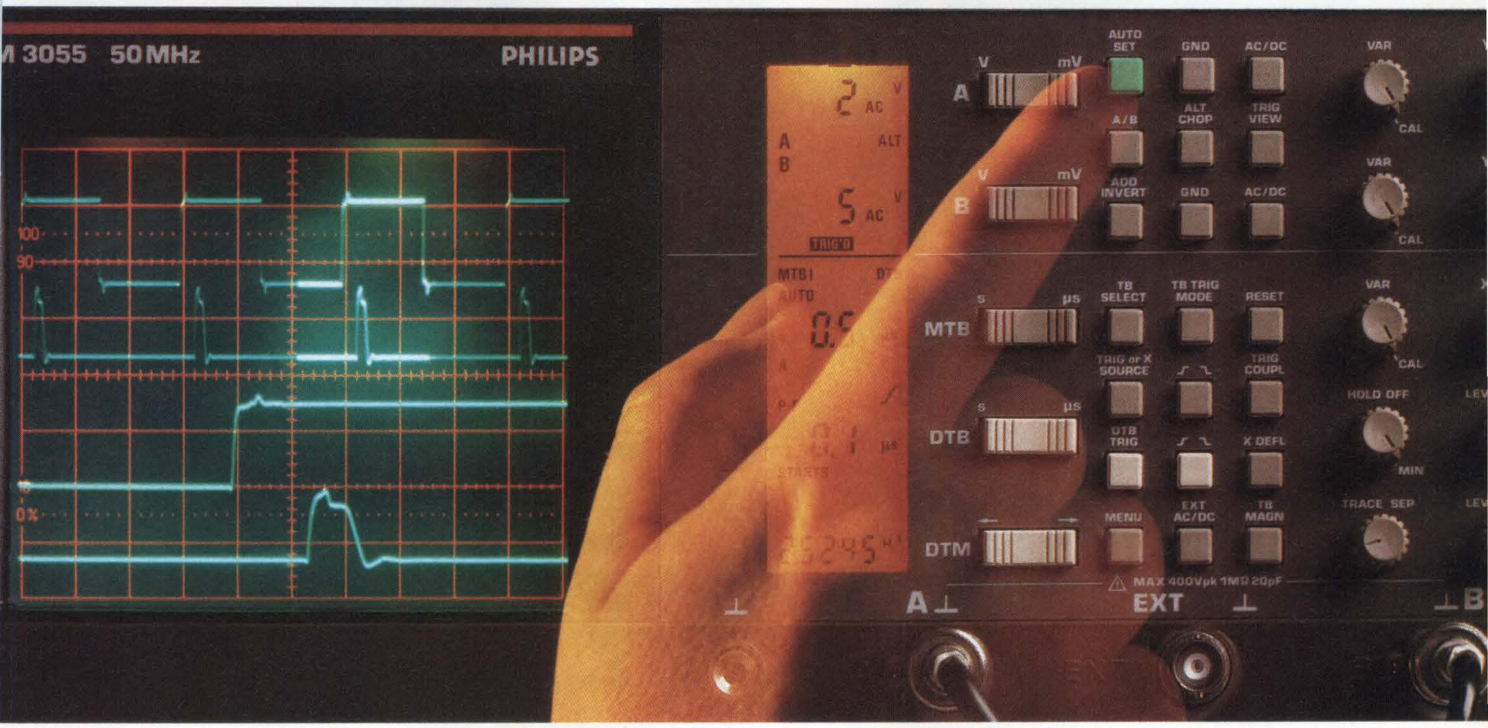

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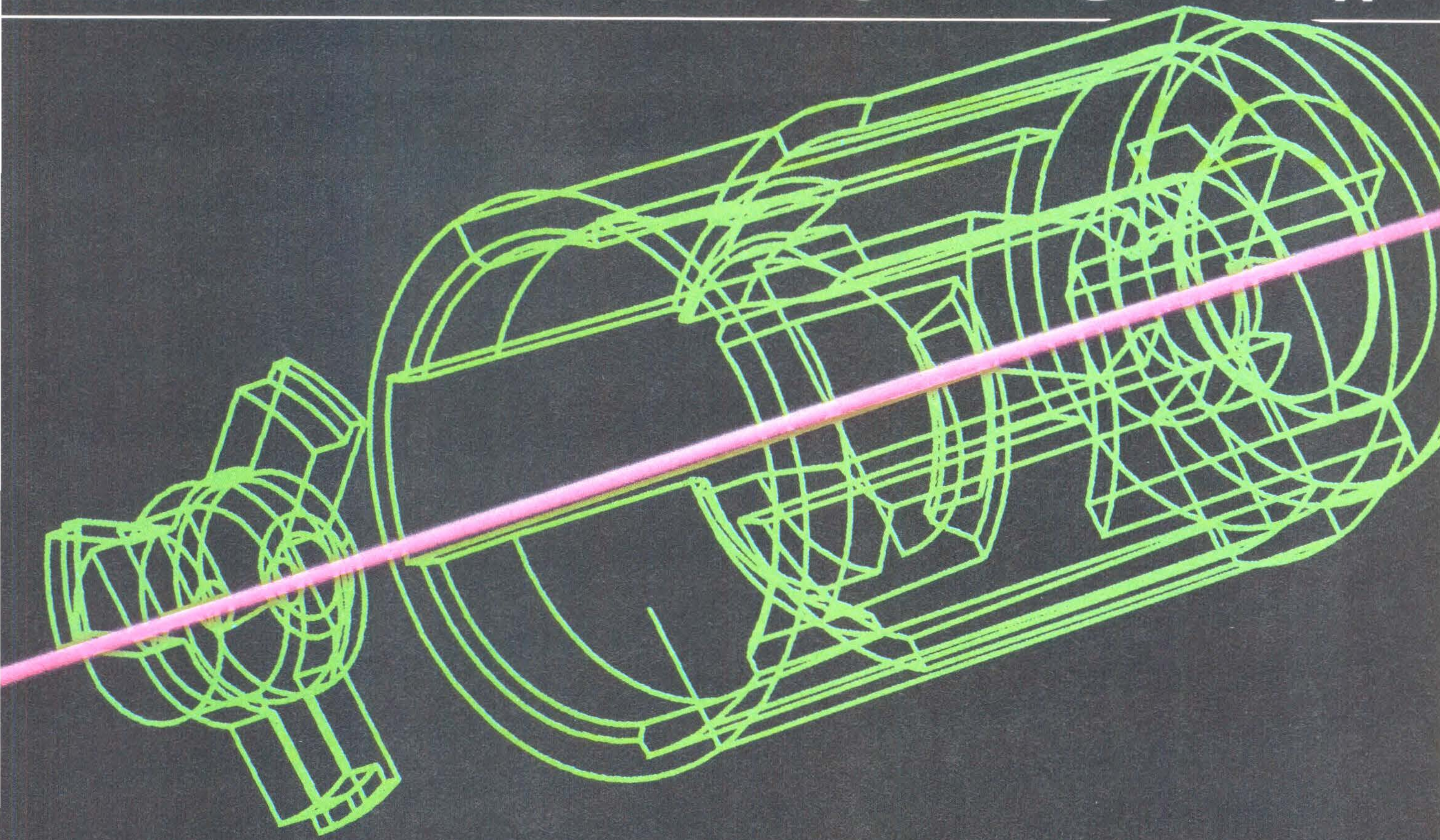

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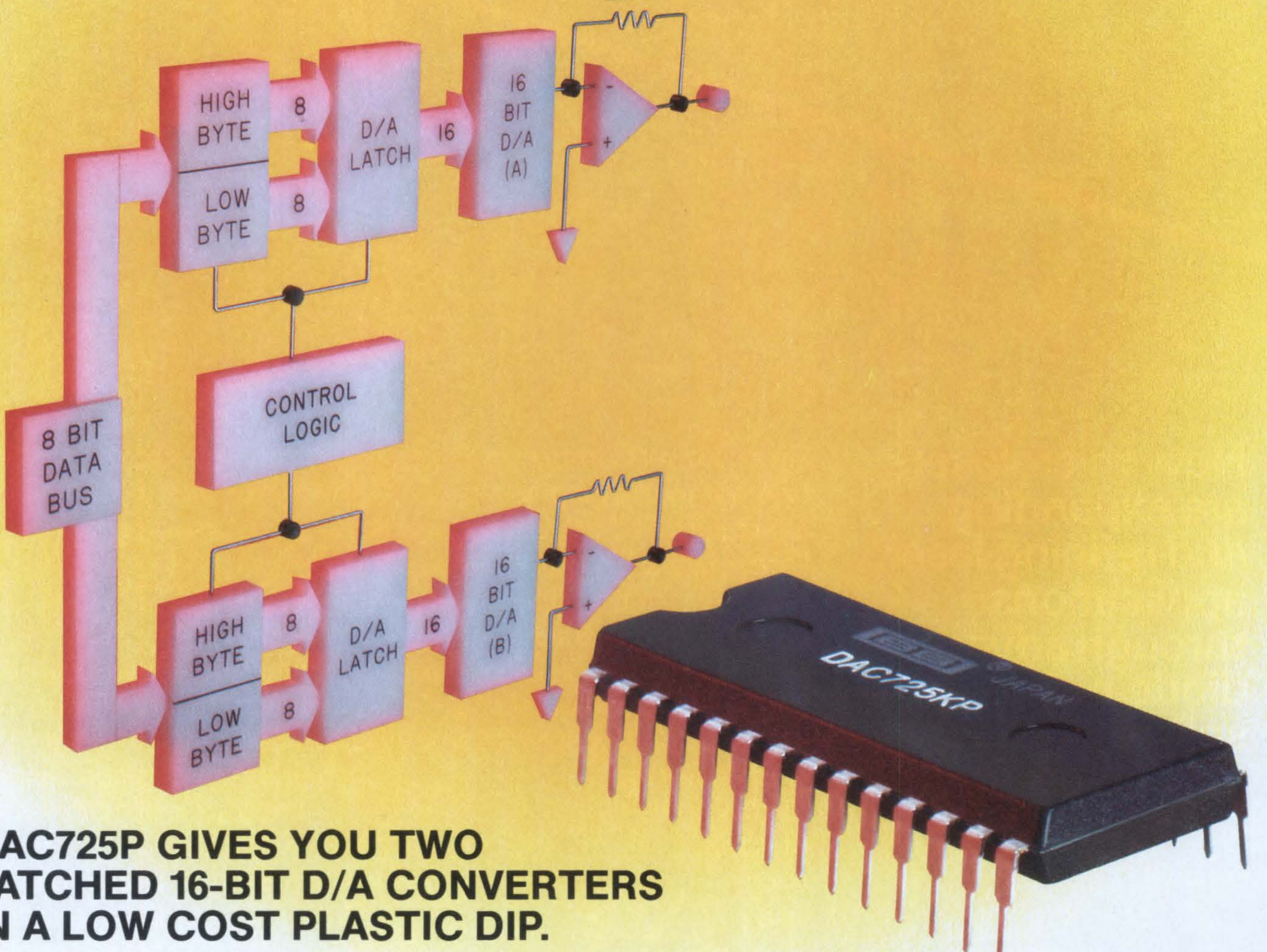

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LINEAR TECHNOLOGY

DESIGN NOTES

Number 7 in a series from Linear Technology Corporation *February, 1988*

DC Accurate Filter Eases PLL Design

Nello Sevastopoulos
Philip Karantzalis

The LTC1062 is a versatile, DC accurate, instrumentation lowpass filter with gain and phase that closely approximate a 5th order Butterworth filter. The LTC1062 is quite different from presently available lowpass switched capacitor filters because it uses an external (R, C) to isolate the IC from the input signal DC path, thus providing DC accuracy. The DC accurate output, pin 7 of Figure 1, is buffered by an internal op amp from the switched capacitor network. The output of the switched capacitor network drives the bottom of C1. The input and output appear across an external resistor and, the IC part of the overall filter handles only the AC path of the signal. A buffered output is also provided (Figure 1) and its maximum guaranteed offset voltage over temperature is 20mV. Typically the buffered output offset is 0-5mV and drift is 1μV/°C. The use of an input (R, C) also provides other advantages, such as lower noise and antialiasing.

With commercially available PLLs, the loop filter is designed by the user to optimize the loop performance. For a variety of applications, a 1st or 2nd order lowpass passive or active R, C filter will do the job. When minimum output jitter and good transient response are required simultaneously, the design of the loop filter becomes more sophisticated. For instance, a fast transient response implies wide filter bandwidth and a reduced VCO output jitter implies minimum ripple at the VCO input. This is achieved by high outband attenuation of the lowpass filter. The LTC1062 provides the above requirements as well as economy and cutoff frequency programmability to be used advantageously in PLL designs.

The circuit of Figure 2 illustrates the use of the LTC1062 as a loop filter. The power supplies for the circuit are a single 5V

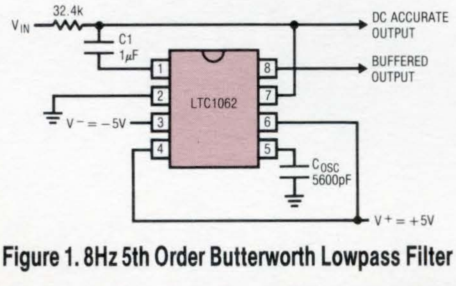


Figure 1. 8Hz 5th Order Butterworth Lowpass Filter

for the PLL and ±5V for the LTC1062. The CMOS PLL is a CD4046B. The LTC1062 can also be used with a single 5V with some additional level shifting (see AN20). Phase detector #2 drives a diode-resistor limiter combination to make the voltage at input R of the LTC1062 swing from one diode above ground to one diode below the 5V supply. Additionally, the two 5k resistors establish a maximum AC impedance to keep the LTC1062 in its operating region and to bias the VCO input at its mid point when phase detector #2 switches into a three-state mode.

An empirical design procedure for input frequencies less than 5kHz ($f_{IN} \le 5$kHz, Figure 2) is illustrated below:

- Given the minimum input frequency value, the cutoff frequency, f_C, of the LTC1062 should be chosen as:

  $$1/6\,(f_{IN(MIN)}) \le f_C \le 1/4\,(f_{IN(MIN)})$$

  The internal (or external) clock frequency of the LTC1062 should be 150 to 250 times the desired cutoff frequency, f_C.

- The capacitor C_{OSC} setting the LTC1062's internal oscillator should be chosen by:

  $$C_{OSC} = \left(\frac{130\text{kHz}}{250 \times f_C} - 1\right) \times 33\text{pF}$$

  By further decreasing the value of C_{OSC}, the internal clock frequency of the LTC1062 increases and the damping of the loop also increases.

- By letting the value of $C = 0.047\mu$F, the LTC1062 input resistor R should be:

  $$R \simeq \frac{5500\text{k}\Omega}{f_C\,(\text{Hz})}$$

  Note: For this application, the loop filter is not required to be maximum flat and, therefore, the (R, C) values of the LTC1062 can be within ±5% tolerance.

To illustrate the performance difference between a lowpass passive R, C loop filter and the LTC1062, the circuit of Figure 2 was tested for a PLL with a 60Hz ±10% input fre-

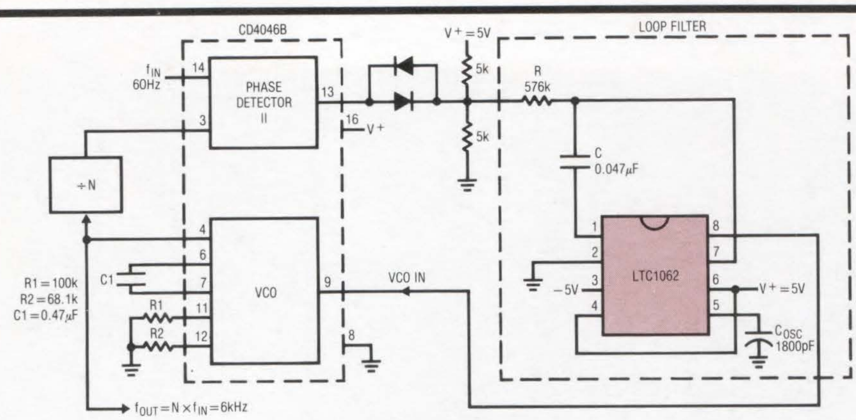
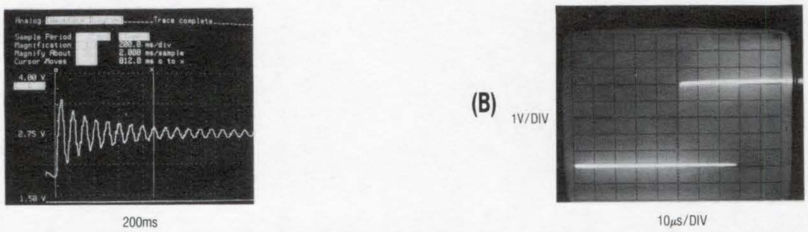


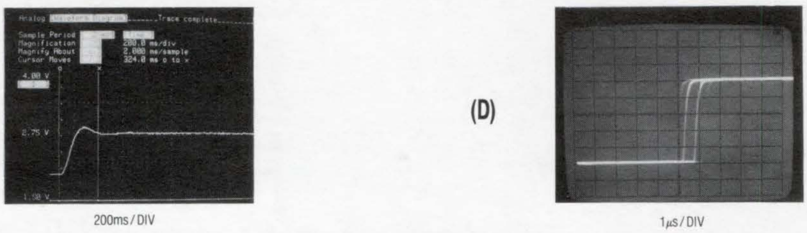
Figure 2

(A) (B)



Transient response (A) and jitter (B) of the PLL with a passive R, C loop filter. The output frequency of the VCO is 6kHz and the ÷ N = 100.

(C) (D)



Transient response (C) and jitter (D) of the PLL with the LTC1062 used as a loop filter. The VCO output frequency is 6kHz and the ÷ N = 100. The jitter is reduced to the internal jitter of the VCO.

Figure 3

quency range and with ÷ N = 100. Then, the PLL's VCO output could be used to drive the clock input of a precision switched capacitor filter, such as an LTC1060A set up in a 100:1 clock to center ratio, and configured as a 60Hz sharp notch or bandpass filter. Figure 3A shows the transient response of the loop when a passive R,C loop filter, Figure 4, is used. The input frequency is shifted from 54Hz to 60Hz and the loop takes 820ms to settle within 5% of its steady stable value. The corner frequency of the R, C passive filter is 22Hz. The natural frequency of the loop is approximately 10Hz and the damping factor less than 0.1. Figure 3B shows the jitter at the VCO output under the above conditions. A 30μs jitter with $f_{OUT} = 6kHz$ corresponds to 18% instantaneous frequency inaccuracy. This makes the PLL VCO output unusable as a

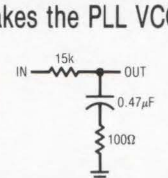


Figure 4. Lowpass R, C Filters used for PLL Example

clock generator for a tracking switched capacitor filter. A small improvement in the VCO output jitter could be achieved by further decreasing the filter's cutoff frequency; this, however, would further penalize the circuit's settling time.

Figures 3C and 3D show the PLL performance when an LTC1062 is used as a loop filter. The corner frequency f_c of the LTC1062 was set at 9.5Hz ($\simeq$ 1/6 f_{IN}) and its internal clock was set for 2.4kHz ($\simeq 252 \times f_c$). The settling time of the loop was 320ms and the damping factor was optimally set to 0.7. The 1μs VCO output jitter, $f_{OUT} = 6kHz$, was measured over 5 periods and it is attributed to the inherited jitter of the VCO internal circuitry. With the LTC1062 used as a loop filter, the circuit's jitter corresponds to 0.12% frequency error. This is quite adequate to drive the clock input of 0.3% accurate switched capacitor filters, such as LTC1059A or LTC1060A.

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Comparator circuit monitors window events

T G Barnett
London Hospital Medical College, London, UK

The **Fig 1** circuit is a window comparator that generates an output pulse for each event that occurs within a specified window. That is, each output pulse signifies an input voltage pulse or level change that exceeds $V_{REF\ LOW}$ but not $V_{REF\ HIGH}$.

The monostable multivibrators IC_{2A} and IC_{2B} produce a 10-µsec pulse at their Q output in response to a rising edge at their A input **(Fig 2)**. Comparator IC_{1B} produces a rising edge when the input exceeds $V_{REF\ LOW}$, and comparator IC_{2A} produces a rising edge when the input exceeds $V_{REF\ HIGH}$.

NOR gates IC_{3A} and IC_{3B} form a bistable latch whose Q output (when low) disables IC_4. IC_4 (unless disabled) produces output pulses in response to falling edges at the IC_{1B} comparator output. You set the width of these pulses by selecting the C_3 capacitor value. As shown, the circuit can handle an input waveform containing 0 to 2V amplitudes and 10-Hz to 10-kHz frequency components. The supply voltage is 5V. **EDN**

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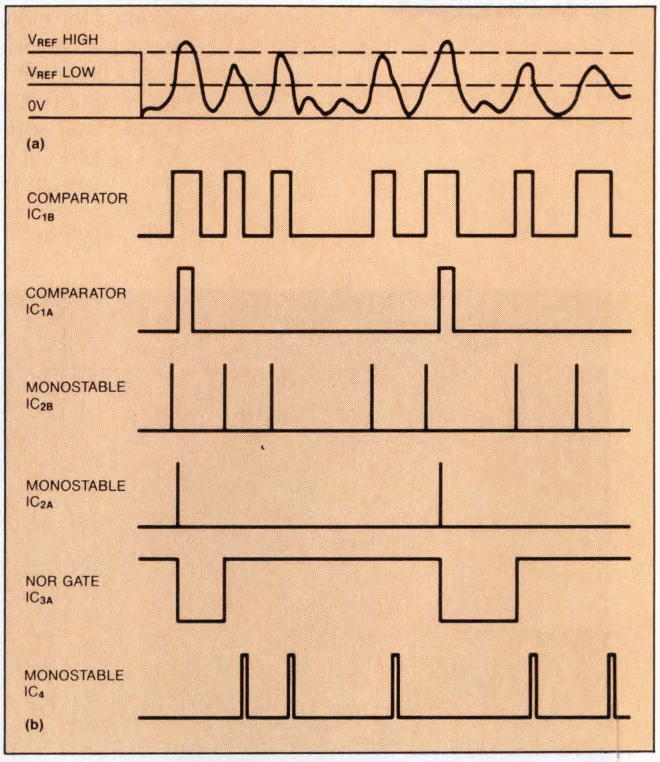

***Fig 2—In response to an input signal (a), the Fig 1** circuit's ICs produce outputs **(b)** that depend on the input's relationship to high and low reference voltages.*

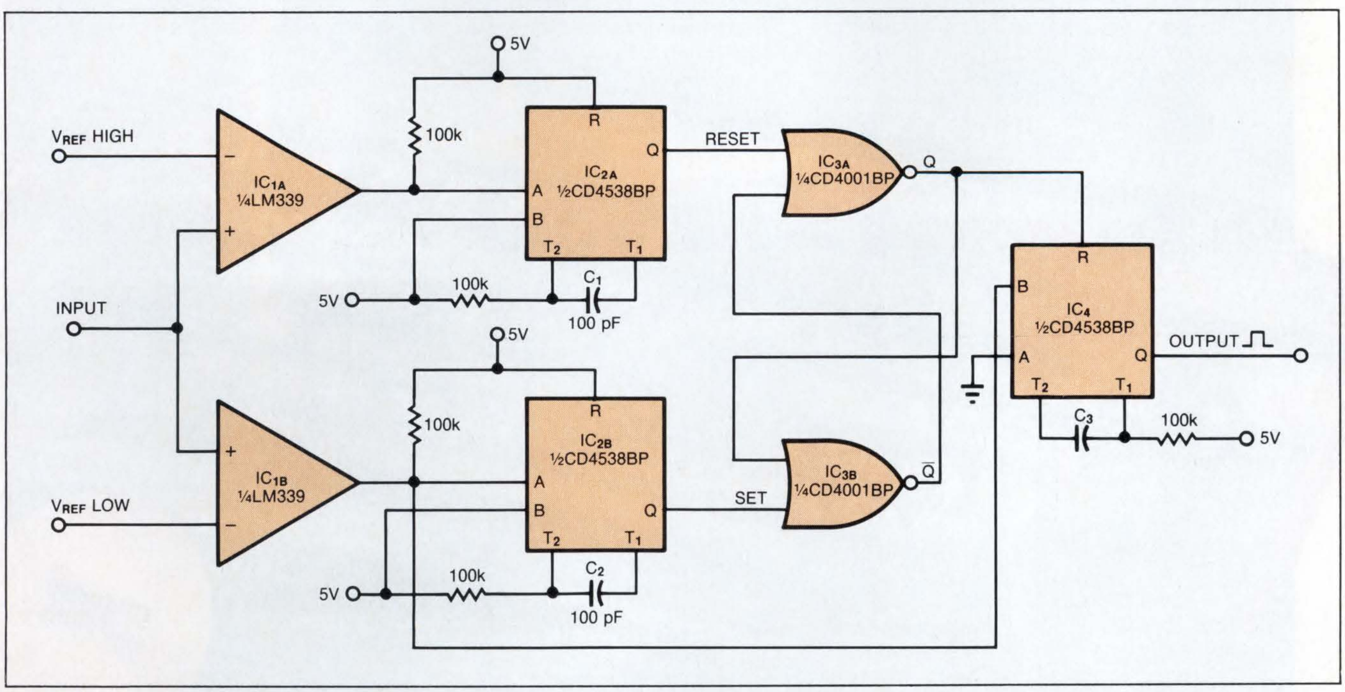

***Fig 1—This window comparator** can serve as a pulse-height discriminator—the circuit generates an output pulse for each input-pulse height between $V_{REF\ LOW}$ and $V_{REF\ HIGH}$.*

MOSFETs provide low-loss rectification

William Chater
The Aerospace Corp, Los Angeles, CA

Rectifiers strongly affect the efficiency of a low-voltage power supply. Silicon diodes, for example, carry a 0.7V forward-voltage penalty. You can avoid much of the power dissipation and heat burden associated with diode rectifiers by using the high-efficiency MOSFET rectifiers shown in **Fig 1.** This approach is especially useful in vacuum work, where the lack of convection cooling limits the allowable power dissipation.

The secondary of the transformer shown in **Fig 1** maintains opposite-polarity V_{DS} voltages across the MOSFETs Q_1 and Q_2; it reverses these polarities once per input cycle. With each change of polarity, the secondary voltage also toggles the MOSFETs' on/off states by causing the output of each comparator (IC_{1A} and IC_{1B}) to switch between the comparators' supply rails. As a result, a unidirectional and nearly constant current flows from the transformer's center tap through the load and back through each MOSFET in turn.

In **Fig 2,** note how an IRFF110 MOSFET's familiar first-quadrant curves extend into the less familiar third quadrant. In particular, note that the channel is off for V_{GS} less than 3V (first quadrant) and fully on for V_{GS} in the 4 to 6V range (third quadrant). Thus, by switching the V_{GS} level you can simulate a diode with very low on-resistance and low forward bias. What's more, this approach avoids activating the MOSFET's parasitic diodes, which usually prevent the application of MOSFETs as rectifiers.

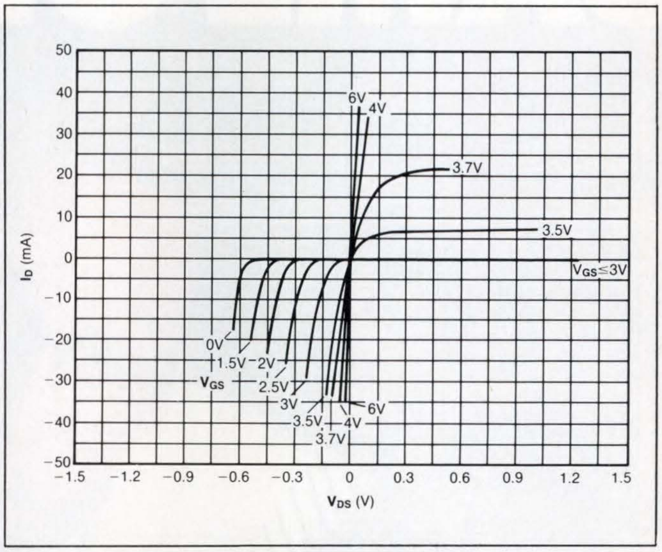

Fig 2—These characteristic curves for an IRFF110 *MOSFET show how it can simulate a nearly ideal diode when you simultaneously switch its V_{DS} and V_{GS} voltages.*

In the circuit shown in **Fig 1,** the comparators' open-collector outputs provide a rapid transition to the

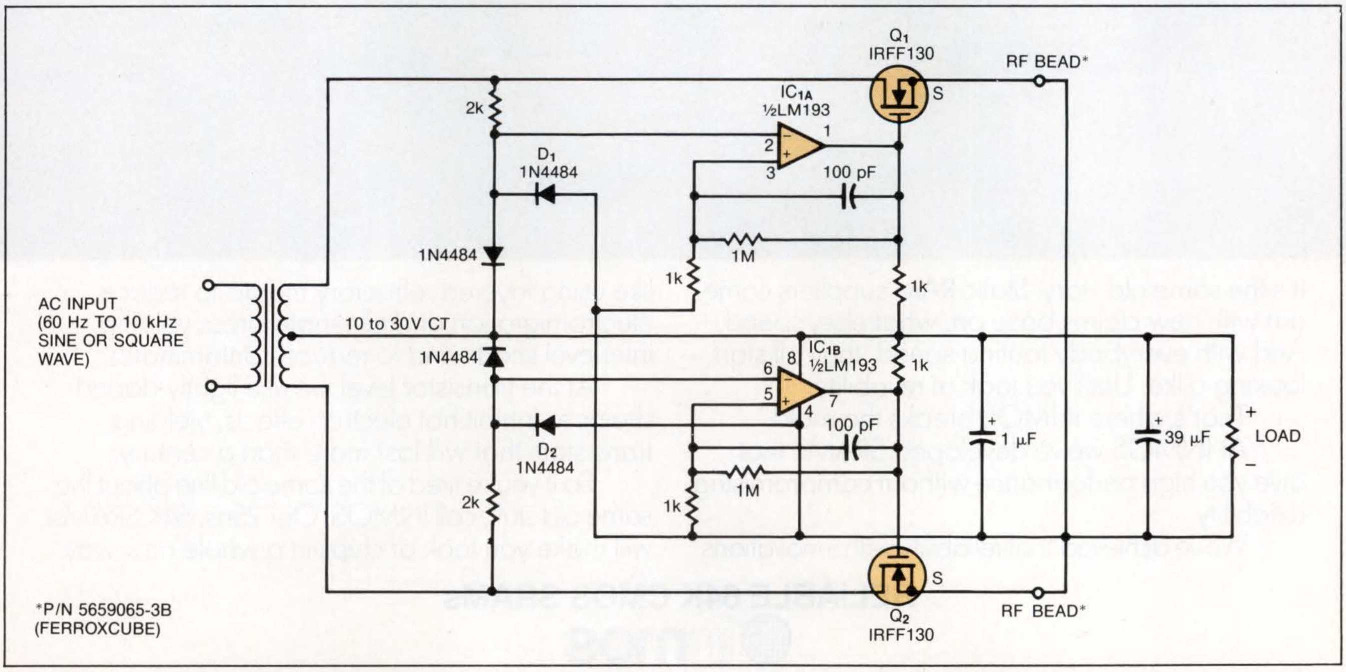

Fig 1—Using MOSFET switches *in place of diode rectifiers, this full-wave rectifier circuit produces a 5V, 1A output at 97% efficiency.*

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CIRCLE NO 193

low state, but the 1-kΩ pullup resistors produce a slower transition to the high level. The MOSFETs thus avoid conduction overlap by turning off rapidly and turning on slowly. Diodes D_1 and D_2 offer protection by clamping the comparators' inverting-input voltages with respect to the negative supply voltage (pin 4). These diodes are normally superfluous, however, because the MOSFETs' low forward drop won't allow the diodes to turn on.

Using a square-wave input, this circuit can produce a 5V, 1A output with 97% efficiency (resistive losses are 60 mW, and each transistor dissipates another 60 mW). For even lower losses, you can parallel two MOSFETs for each switch. Using diode rectifiers, the efficiency would be about 90%. The use of a sine-wave input also lowers the circuit efficiency but not to the level of a diode-rectifier version: The duty cycle of the switches in **Fig 1** goes from almost 50% with a square-wave input to about 20% with a sine-wave input. Consequently, the switches deliver greater-amplitude current pulses to the load filter, which increases the power dissipation. **EDN**

To Vote For This Design, Circle No 746

Temperature sensor has 4- to 20-mA output

Art Kapoor
Precision Monolithics Inc, Santa Clara, CA

The **Fig 1** circuit's current-transmitter output (4 to 20 mA) is proportional to temperature. The transmitter accepts an 8 to 40V supply voltage, exhibits a PSR better than 0.0003%/V, and provides ±1% accuracy over the −50 to +150°C temperature range after calibration. IC_1's temperature-proportional output V_{TEMP} lets the chip serve as a temperature sensor as well as a 2.5V reference. V_{TEMP} equals 0.55V at 25°C and has a temperature coefficient of 1.9 mV/°C.

The micropower, single-supply op amp IC_2 buffers the current drain on V_{TEMP}, which can supply no more than 50 nA. The second op amp (IC_3) regulates I_{OUT} as illustrated by the equation for current summation at the op amp's noninverting input:

$$I_{OUT} = \frac{V_{TEMP}(R_6 + R_7)}{R_2R_8} - \frac{V_{SET}\,(R_2 + R_6 + R_7)}{R_2R_8}.$$

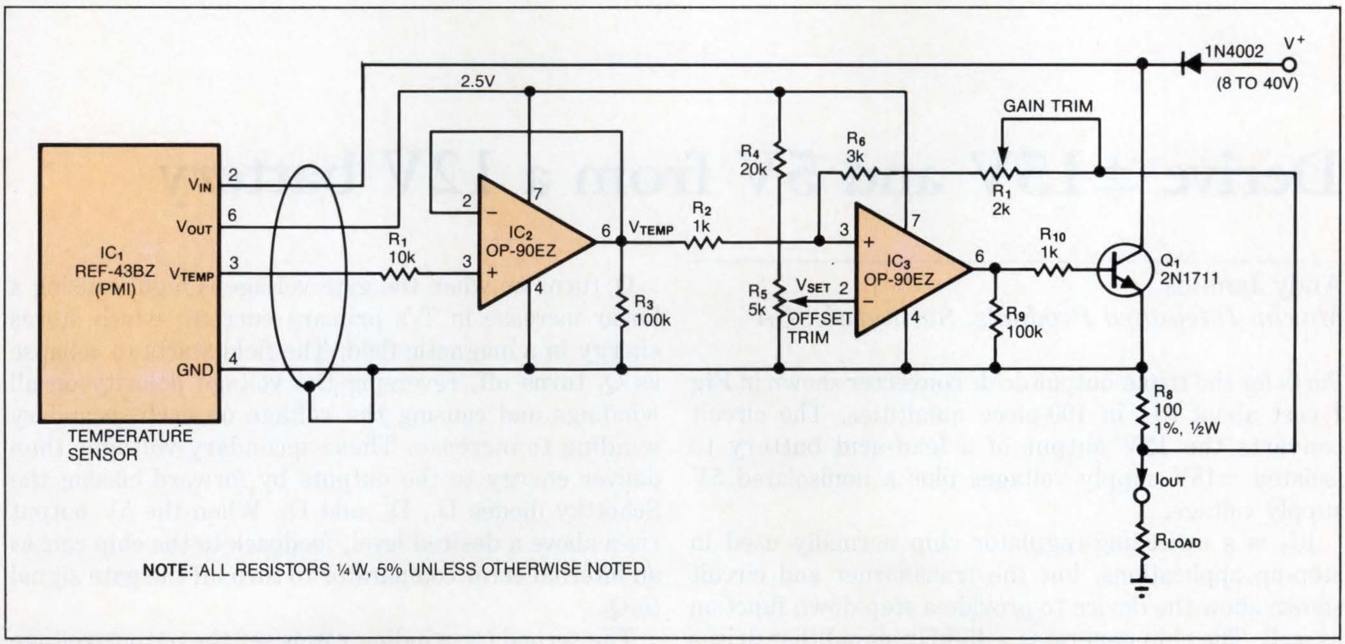

***Fig 1—This circuit generates a 4- to 20-mA** current output that is proportional to temperature. Gain and offset trims do not interact.*

You obtain the variation of I_{OUT} with temperature by differentiating the transfer function:

$$\frac{\Delta I_{OUT}}{\Delta T} = \frac{\frac{\Delta V_{TEMP}}{\Delta T}(R_6 + R_7)}{R_2R_8}.$$

The formulas show that the gain and offset trims do not interact if you trim the gain first. To trim the gain, first place the sensor (IC_1) in an ice-water bath (0°C) and, if necessary, adjust the offset-trim potentiometer (R_5) so that I_{OUT} is greater than 4 mA. Record I_{OUT}. Next, place the sensor in boiling water (100°C). Adjust the gain-trim resistance (R_6+R_7) so that I_{OUT} produces the desired mA/°C ratio:

$$\text{OUTPUT RATIO} = \frac{\Delta I_{OUT}}{\Delta T_{OPERATING}} = \frac{16\text{ mA}}{\Delta T_{OPERATING}}.$$

If the transmitter is to operate over −50 to 150°C, for example, then

$$\text{OUTPUT RATIO} = \frac{16\text{ mA}}{150°\text{C} - (-50°\text{C})} = \frac{16\text{ mA}}{200°\text{C}} = 0.08\text{ mA/°C}.$$

Suppose the I_{OUT} value that corresponds to 0°C is 6.3 mA. Then at 100°C,

$$I_{OUT\,(100°C)} = I_{OUT\,(0°C)} + 100°\text{C}\,(0.08\text{ mA/°C}) = 6.3\text{ mA} + 8\text{ mA} = 14.3\text{ mA}.$$

TABLE 1—GAIN-TRIM VALUES

TEMPERATURE RANGE	R_6 (FIXED)	R_7 (VARIABLE)
0°C TO 70°C	10 kΩ	5 kΩ
−15°C TO 85°C	6 kΩ	3 kΩ
−50°C TO 150°C	3 kΩ	2 kΩ

Therefore, you should adjust R_6 so that I_{OUT}=14.3 mA while the sensor is at 100°C.

Finally, you can adjust the offset at any temperature $T_{AMBIENT}$ without affecting the gain trim:

$$I_{OUT} = \frac{16\text{ mA}\,(T_{AMBIENT} - T_{MIN})}{\Delta T_{OPERATING}} + 4\text{ mA}.$$

At 20°C in the above example,

$$I_{OUT} = \frac{16\text{ mA}}{200°\text{C}}(20°\text{C} - (-50°\text{C})) + 4\text{ mA} = 9.6\text{ mA}.$$

Table 1 shows the R_6 and R_7 values required for various temperature ranges. **EDN**

To Vote For This Design, Circle No 748

Derive ±15V and 5V from a 12V battery

Andy Jenkins
Maxim Integrated Products, Sunnyvale, CA

Parts for the triple-output dc/dc converter shown in **Fig 1** cost about $11 in 100-piece quantities. The circuit converts the 12V output of a lead-acid battery to isolated ±15V supply voltages plus a nonisolated 5V supply voltage.

IC_1 is a switching-regulator chip normally used in step-up applications, but the transformer and circuit shown allow the device to provide a step-down function as well. The chip generates a 45-kHz signal that drives the gate of MOSFET Q_1.

Q_1 turns on when the gate voltage is high, causing a linear increase in T_1's primary current, which stores energy in a magnetic field. The field starts to collapse as Q_1 turns off, reversing the voltage polarity on all windings and causing the voltage on each secondary winding to increase. These secondary voltages then deliver energy to the outputs by forward-biasing the Schottky diodes D_1, D_2, and D_3. When the 5V output rises above a desired level, feedback to the chip causes an internal error comparator to turn off the gate signal to Q_1.

The secondary-winding ratios set the output-voltage levels, and close coupling between the trifilar windings

assures good load regulation for the ±15V supplies (regulation is about 2% for a 10 to 100% load change). For better regulation, you can set the output voltage higher and add linear regulators. The inductors L_1 and L_2 block high-frequency ringing from the transformer that would otherwise boost the ±15V outputs out of spec when lightly loaded. For best regulation, you should provide minimum loads of 10% for the 15V supplies and 20% for the 5V supply.

The circuit can accommodate the 8 to 16V range associated with the terminals of a lead-acid battery. What's more, the protection network made up of resistor R_1 and zener diode D_4 allows the circuit to withstand 50V for 1 msec—a classic overvoltage test that simulates the load dump of an automobile's alternator when you turn off the ignition. For an input change of 8 to 16V, the 5V output's line regulation is typically 0.2%.

Battery current is about 600 mA for nominal operation, but current peaks in the primary winding can be 4A or more. Therefore, you should provide good-quality ground connections and short, low-impedance connections to the transformer and the MOSFET. Close decoupling using ceramic and electrolytic capacitors also reduces output noise. With proper circuit layout, the output noise is about 50 mV at the 5V output and 30 mV at the 15V outputs.

The transformer, constructed with a ferrite pot core that offers low loss and minimal magnetic leakage, has a primary inductance of about 21 μH for the power levels shown. You must choose a core size and material that will handle the 4A peak currents without saturation. The 15V secondaries have 2.9:1 turns ratios, which provide the desired 3:1 voltage ratio after covering the rectifier losses. Actual turns are as follows: the primary, 11½ turns; the 15V secondaries, 11½ turns each; the 5V secondary, four turns. High circuit efficiency (about 75% at full load with a 12V input) eliminates any need for a heat sink on the MOSFET. **EDN**

To Vote For This Design, Circle No 747

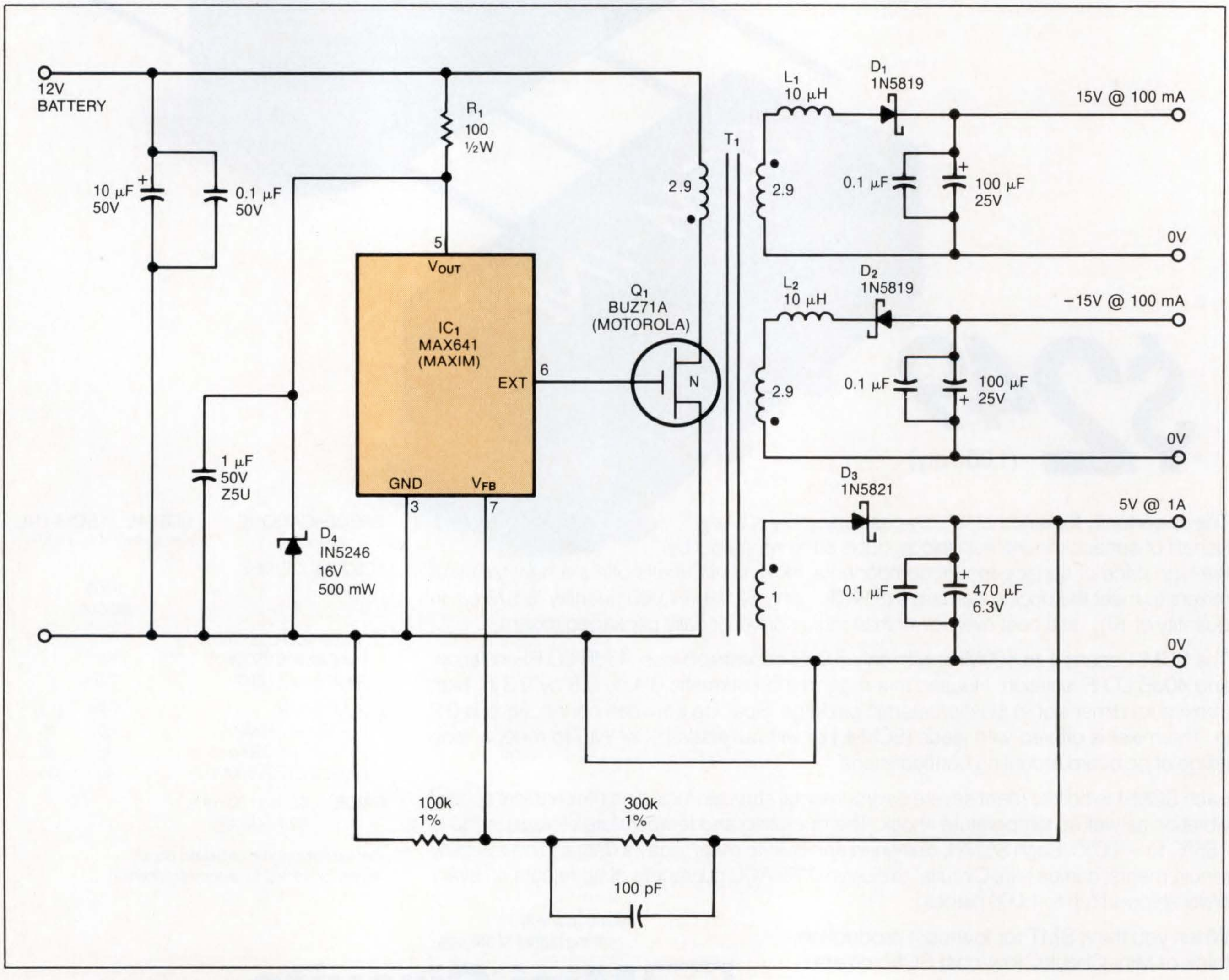

***Fig 1—This triple-output dc/dc converter** requires only one IC.*

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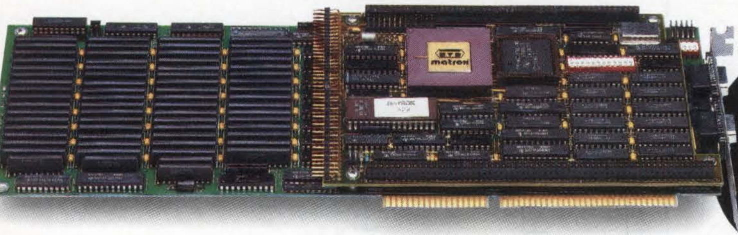

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CIRCLE NO 192

ISSUE WINNER

The winning Design Idea for the November 12, 1987, issue is entitled "Step-up converter produces 5V from 1.5V," submitted by Gerald Grady of Maxim Integrated Products (Sunnyvale, CA).

Switch debouncer uses few parts

Bill McClelland
Stahl Research, Port Chester, NY

When debouncing is important, designers often use an spdt switch for an spst function (*EDN*, October 29, 1987, pg 252). You can debounce an spst switch, however, using a single Schmitt-trigger inverter **(Fig 1).**

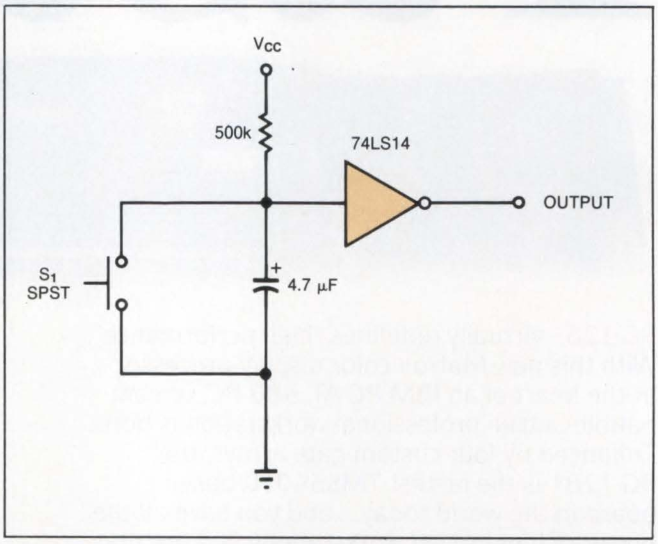

Fig 1—This simple spst switch debouncer *relies on the inverter's internal pullup resistor. An external resistor allows use of a CMOS gate.*

The TTL inverter (74LS14) has an internal 16-kΩ pullup resistor that pulls the gate input high when the switch is open. As you close the switch, the 4.7-µF capacitor discharges on the first contact; if the switch contacts bounce open, the internal resistor limits the capacitor's recharge to a rate sufficiently slow to prevent an undesired gate transition before the contacts again close. Note that the circuit correctly debounces the switch for both opening and closing. If you add an external pullup resistor (dotted lines), you can use a CMOS Schmitt-trigger gate (74HC14) and a smaller (0.1 µF) capacitor. **EDN**

To Vote For This Design, Circle No 750

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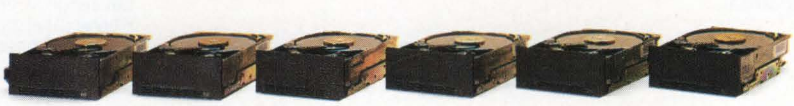

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CIRCLE NO 200

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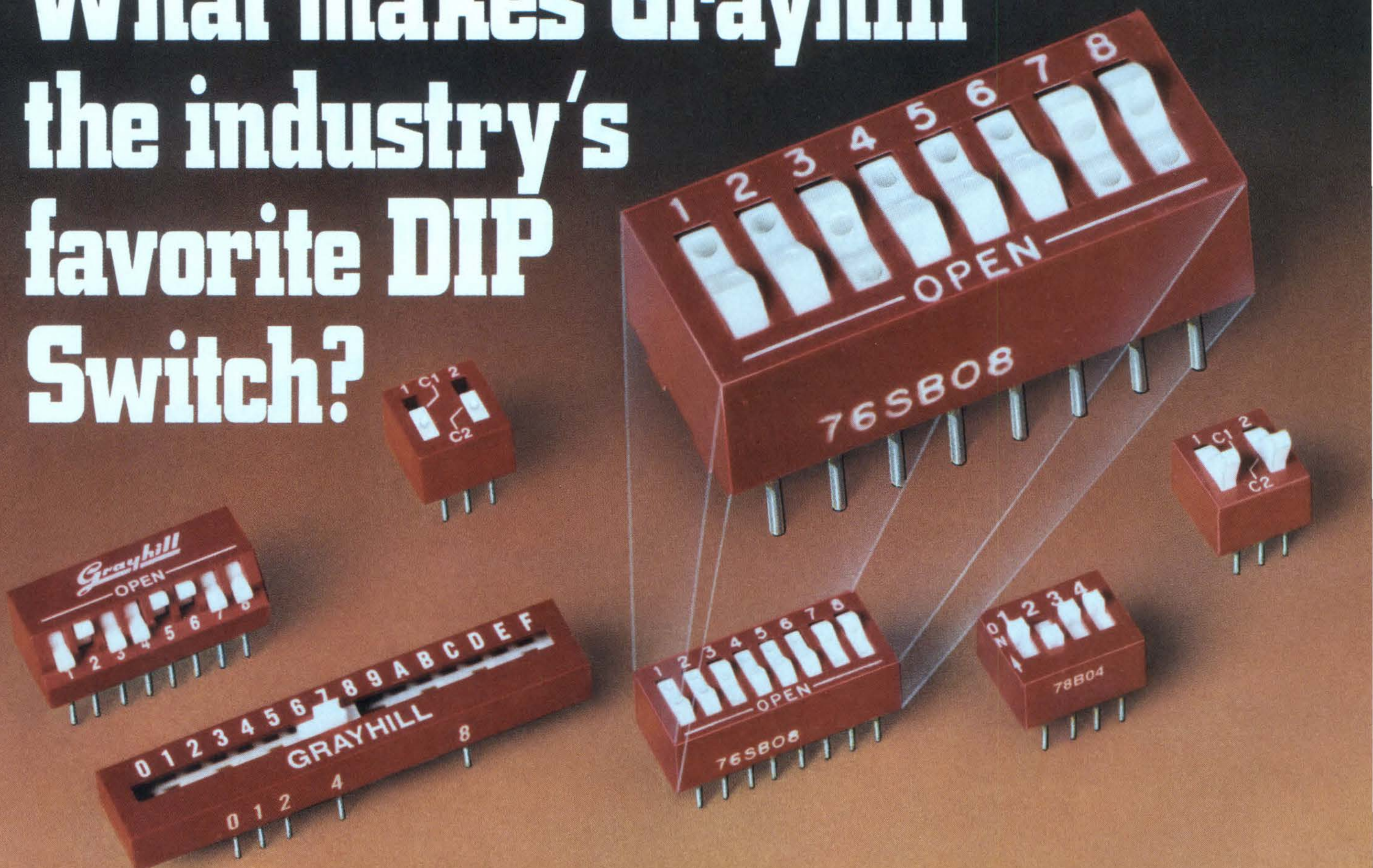

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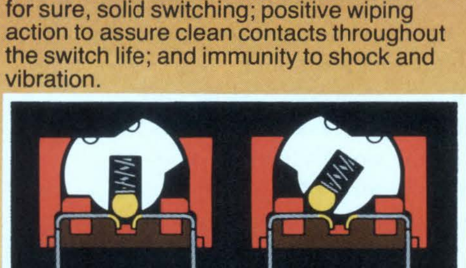

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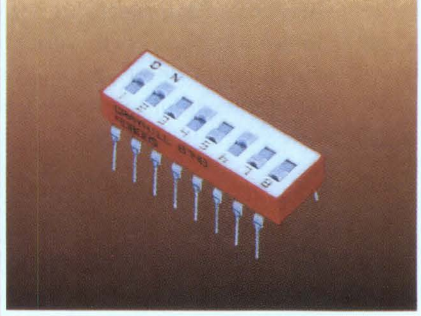

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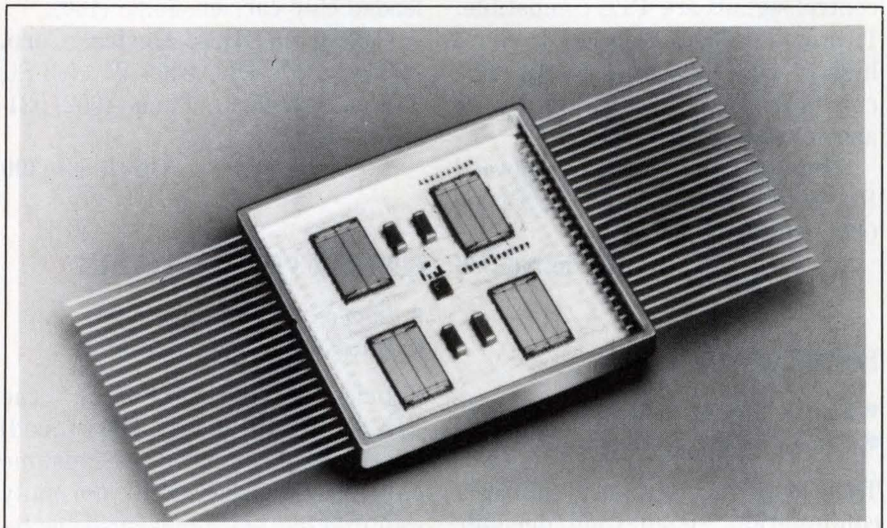

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- *Provides 1M-bit memory*
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The MEM-84000 hybrid IC comes in a 1.25×1.25×0.15-in. hermetic flatpack and uses four TTL-compatible 32k×8-bit RAM chips to implement its 1M-bit memory. The unit's 100-nsec access time, 64k×16-bit memory organization, and −55 to +125°C operating temperature range suit it for use with 16- or 32-bit CPUs in military processor applications. Data transfers to the device are made using 16 address lines, 16 data lines, and standard read, write, and enable lines. You can use external decoding to expand the unit's memory to any width or depth. The unit operates from a 5V supply. Its low-power CMOS construction allows battery backup, which prevents data loss in the event of power failure. The unit retains data even when operating on battery voltages as low as 2V. $750. Delivery, stock to 90 days ARO.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600. TWX 310-685-2203.

Circle No 385

MICROCONTROLLER

- *Has three more ports than the 87C51 microcontroller*
- *Features 56 I/O pins*

The 7-port EPROM-based SC87C451 microcontroller has all the features of the industry-standard 87C51 and three more 8-bit, bidirectional ports. The three ports provide 24 additional I/O pins, which you can use in telemetry, printer, process-control, and disk-drive applications; you can also use the unit to advantage in distributed-processing applications. You can program one of the three ports for 3-state control. Using four handshaking pins, you can load the unit via a μP system as you would a RAM. The microcontroller stores its control program in 4k bytes of EPROM; you can quickly test various prototype control programs by erasing the control program in the EPROM through the microcontroller's quartz window and loading a new control program. In a 68-pin PLCC, $95; in a 64-pin ceramic DIP, $85 (100).

Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94088. Phone (408) 991-2000.

Circle No 386

VIDEO MULTIPLEXER

- *Features eight channels*
- *Has 300-MHz bandwidth*

The DG538 8-channel video multiplexer has low drive requirements and provides TTL compatibility, address-latch data readback, a 300-MHz bandwidth, and −97-dB crosstalk at 5 MHz. The unit's analog signal range allows ±5V signal swings, eliminating the need for a bias circuit and coupling capacitors at the multiplexer's input and output. All of the monolithic IC's signal lines are fully isolated from adjacent signal lines, and the unit features 55Ω on-resistance and 8-pF max drain capacitance. Applications for the unit include high-quality video systems, wideband information-distribution systems, cable and studio TV equipment, and medical imaging systems. In a 28-pin DIP, $11.52; in a PLCC, $13.01 (100).

Siliconix Inc, 2201 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 988-8000.

Circle No 387

A/D CONVERTER

- *Offers 10-bit resolution*
- *Provides 20M-samples/sec*

According to the manufacturer, the TDC1020 is the first monolithic flash A/D converter to offer 10-bit resolution at a guaranteed 20M-sample/sec rate. Its target applications include radar and studio-quality video systems. The device is also suitable for use in medical-imaging applications and for high-speed data conversion. The converter operates over the commercial temperature range and comes in a 64-pin DIP. $295 (1000).

TRW LSI Products, Box 2472, La Jolla, CA 92038. Phone (619) 457-1000.

Circle No 388

SHIFT REGISTER

- *Multiplexes and demultiplexes 8-bit data streams*
- *Offers ECL-compatible inputs*

The SDA-8020 is a 4/8-bit shift register for use as an interface between high-speed A/D or D/A converters and the memories in a data-acquisition system. Featuring ECL-compatible signal inputs, the device can demultiplex an 8-bit data stream having a clock speed as high as 100 kHz into four parallel 8-bit TTL data channels having a clock speed 25% less than that of the serial clock. Conversely, a multiplexing mode can reverse this action. The cascadable shift register has two clock outputs, and all its external control signals are TTL compatible. It provides special signals to drive high-speed CMOS static RAMs. The chip is packaged in a 68-pin PLCC and consumes 1.5W. $70 (100).

Siemens Corp, 2191 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 980-4577.

Circle No 389

DTMF RECEIVER

- *Detects all 16 DTMF tone pairs*
- *Combination decoder and filter*

The G8870 receiver on a chip is a combination Touch-Tone decoder and filter. It detects all 16 DTMF tone pairs and converts them to code. It can also distinguish sound frequencies that approximate DTMF signals from actual DTMF signals, selectively passing only the latter to the output bus. The device consumes 35 mW max. It comes in an 18-pin DIP or a 20-pin plastic leaded chip carrier. $5.25 (100).

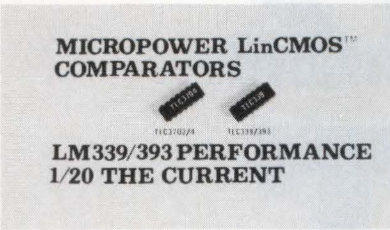
California Micro Devices Corp, Microcircuits Div, 2000 W 14th St, Tempe, AZ 85281. Phone (602) 921-4540.

Circle No 390

CMOS COMPARATORS

- *Low current consumption*
- *Duals and quads available*

Fabricated in LinCMOS, the TLC393 (dual) and TLC339 (quad) micropower comparators consume only 5% of the current normally required by their pin-compatible bipolar counterparts, the LM393 and LM339. When the micropower comparators are operating from a 5V supply, the typical power dissipation of each independent compara-



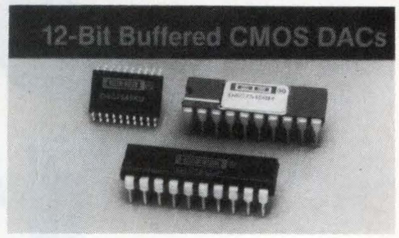
tor in the micropower chips is only 50 μW; the response time is typically 2.5 μsec at 5 mV of overdrive. The TLC393 and TLC339, like the LM393 dual and LM339 quad, have open-drain outputs that can interface to a variety of loads and supplies and to logic functions. In contrast to the 393 and 339 types, two other LinCMOS types, the TLC3702 dual and the TLC3704 quad have push-pull outputs that eliminate the need for external pullup resistors for driving capacitive loads. All four micropower LinCMOS comparators operate from single-supply voltages of 3 to 16V for versions in the commercial and industrial temperature ranges or 4 to 16V for versions in the military temperature range. A variety of DIP and SO packages are available. Plastic-DIP commercial devices, from $0.52 to $0.73 (100).

Texas Instruments Inc, Semiconductor Group (SC-764), Box 809066, Dallas, TX 75380. Phone (800) 232-3200, ext 700.

Circle No 391

CMOS 12-BIT DAC

- *Performs 4-quadrant multiplication*
- *Features TTL/CMOS-logic compatibility*



The DAC7545 buffered, 12-bit multiplying D/A converter is a pin-compatible replacement for industry standards such as the AD7545 and PMI7545. The device features 12-bit μP-interface logic and loads data as 12-bit data words. It processes data when the Chip Select and Write pins are both at logic lows. Because it is a multiplying DAC, it supplies output that is the product of the digital input code and an external analog reference signal. The DAC's reference input can vary between ±20V; with the addition of external op amps at its output, the device can perform 4-quadrant multiplication. The converter features 10-nA max output leakage and 70-pF max output capacitance. In a plastic DIP, $8; in a small outline package, $9.20; in a ceramic DIP, $9.50 (100).

Burr-Brown, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491.

Circle No 392

Continued on pg 253

CIRCLE NO 201

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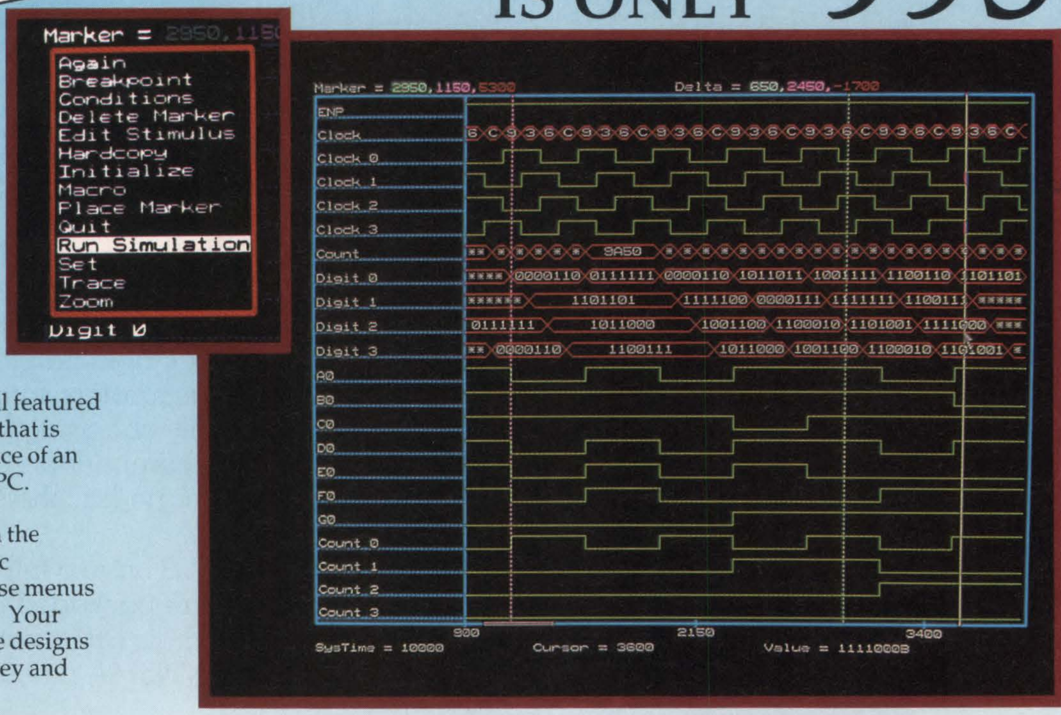

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Elcor Associates, Inc.
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Advanced Digital Group
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15. CT, RI, MA, VT, NH, ME
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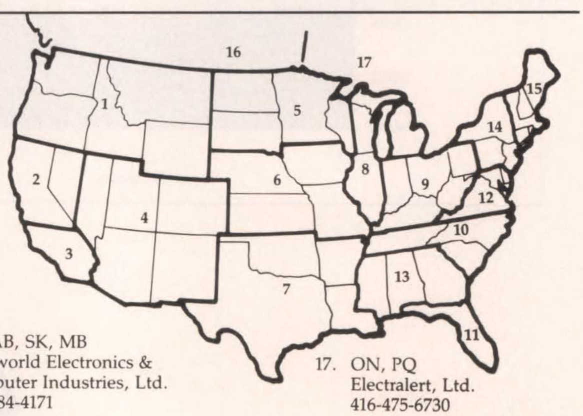
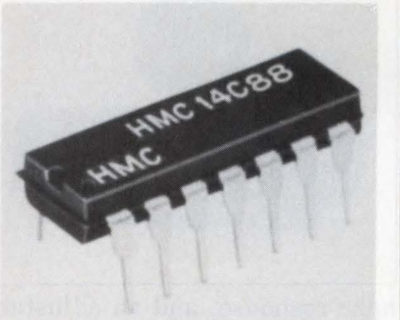
16. BC, AB, SK, MB
Interworld Electronics & Computer Industries, Ltd.
604-984-4171



17. ON, PQ
Electralert, Ltd.
416-475-6730

OR 8746



QUAD LINE DRIVER

- *CMOS device operates from supply voltages of 4.5 to 15V*
- *Conforms to RS-232C and CCITT V.24/V.28 specifications*

The CMOS HMC14C88 is a replacement for the TTL 1488 bipolar quad line driver. The inputs are compatible with both TTL and CMOS levels and are nominally centered to switch at 1.4V. The outputs switch to within 75% of the supply rails while driving RS-232C line loads of 3 to 7 kΩ. The outputs are also short-circuit protected, provide a minimum power-down output impedance of 300Ω, and have a propagation delay of less than 2 µsec. $0.72 (1000).

HMC, 1235 Walt Whitman Rd, Melville, NY 11747. Phone (516) 673-6505.

Circle No 393

QUAD POWER DRIVER

- *Output current to 2.5A*
- *Output voltages to 60V*

The SG3645 quad driver for stepper motors comes in a 16-pin Batwing package. Each of its four open-collector Darlington outputs has a breakdown voltage rating of 60V and a current rating of 2.5A. A common enable signal can enable or disable all four outputs simultaneously. Each of the device's four channels have TTL-compatible inputs and integral transient-suppression diodes in the outputs. The circuit has a thermal shutdown feature. The SG3645 is specified for operation at junction temperatures from 0 to 125°C. Samples are available from stock. $2.65 (100). Delivery, 60 days ARO.

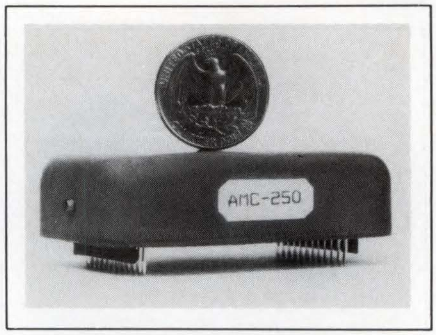
Silicon General, 11861 Western Ave, Garden Grove, CA 92641. Phone (714) 898-8121. TWX 910-596-1804.

Circle No 394

SERVO AMPLIFIER

- *250W capability*
- *30-kHz PWM frequency*

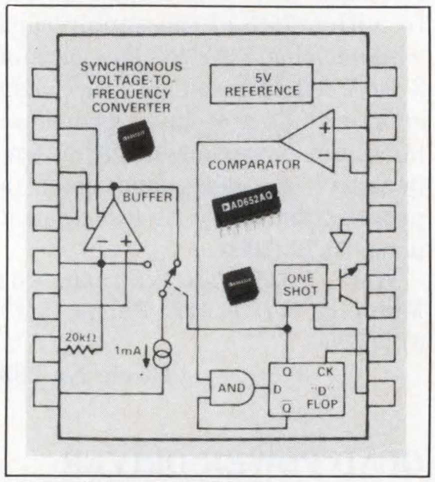
The AMC-250 contains a complete dc velocity servo amplifier that provides protection against output short circuits, overheating, and overvoltage. The device also has a compensation adjustment to opti-



mize response, and an adjustable current limit. The device doesn't require an external heat sink or forced-air cooling for most duty cycles, even at its maximum output of ±50V at ±5A. The device operates at any supply voltage from 20 to 50V and measures 1.62×2.75×0.75 in. $149.

Advanced Motion Controls, 15921 Haynes St, Van Nuys, CA 91406. Phone (818) 989-4480.

Circle No 395



V/F CONVERTER

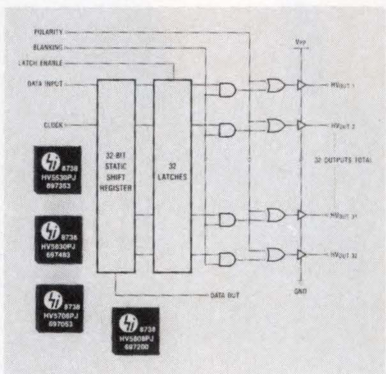
- *Full-scale frequency of 2 MHz*
- *Maximum nonlinearity of ±0.005%*

The AD652 can perform a V/F conversion to 14-bit accuracy (16-bit resolution) in 32.77 msec at 2 MHz. The internal 5V reference can supply 10 mA to an external load. You can apply an external clock to the device, in synchronous mode, to set its full-scale frequency. The AD652 is pin compatible with the AD651 and VFC100 synchronous V/F converters. The device operates from a

12 to 18V supply for unipolar operation or from a ±6 to ±18V supply for bipolar applications. The packaging options include a 20-terminal PLCC or a 16-pin ceramic DIP. The device is available in three temperature ranges and two accuracy grades. $6.95 to $13.65 (100).

Analog Devices, Literature Ctr, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 935-5565. TWX 710-394-6577.

Circle No 396



DRIVERS

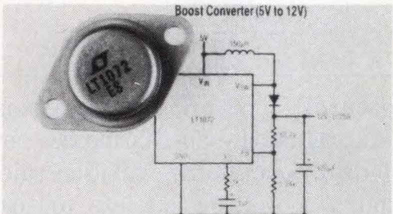
- *Provide 32 channels*
- *Feature 80 and 300V ratings*

The HV55 and HV56 300V drivers and the HV57 and HV58 80V drivers combine high-speed, low-power CMOS logic with high-voltage DMOS outputs. The HV55 and its reverse-shift complement, the HV56, have 32 open-drain, 300V N-channel outputs, each of which can sink 100 mA. A built-in, 8-MHz shift register controls the outputs and offers polarity and blanking control. The combination of the two control features provides flexibility for driving flat-panel displays. The HV57 and its reverse-shift complement, the HV58, have 32 push-pull, 80V outputs, each of which can source or sink 20 mA. You can use these units to drive nonimpact printers and electroluminescent, plasma, and liquid-crystal displays. The devices come in 44-pin PLCC J-lead packages. From $6.34 (1000).

Delivery, six to eight weeks ARO.

Supertex Inc, 1225 Bordeaux Dr, Box 3607, Sunnyvale, CA 94088. Phone (408) 744-0100. TWX 310-683-9143.

Circle No 397



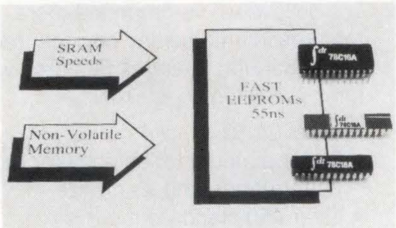
SMPS REGULATOR

- *Features on-chip 1.25A switch*
- *Operates from 3 to 60V*

The LT1072 regulator IC includes an on-chip 1.25A output switch and comes in either a 5-pin TO-3 or TO-220 package. The SMPS (switch-mode power supply) unit operates over a 3-to-60V input voltage range, and you can synchronize it with a system clock that operates from 48 to 70 kHz. The regulator uses an adaptive antisaturation switch drive that permits a wide range of load currents at low-saturation voltage and high operating efficiency. The IC operates in all standard switching configurations, including the buck, boost, flyback, and forward configurations. Designers with little experience in switch-regulator applications will find the chip easy to use: It features a built-in oscillator; integral control and protection circuitry; and built-in circuitry for producing a fully isolated flyback regulator, thus eliminating the need for optocouplers or extra transformer windings. A shutdown mode, which you activate externally, reduces total standby-operation current to 50 μA typ. In a TO-220 package, $4.25 (100).

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (800) 637-5545; in CA, (408) 432-1900.

Circle No 398



CMOS EEPROMs

- *55-nsec read access time*
- *Serial programming I/O channel*

The IDT78C16 is a 16k-bit EEPROM featuring a 55-nsec access time; it's pin compatible with slower (150-nsec) types. Along with the 55-nsec access time, the IDT78C18 features a serial-I/O channel that allows rewrites independently of the target system's µP. Additionally, you can write to both devices in the customary, parallel manner. Both devices have onboard charge pumps for generating programming supervoltages from a single 5V supply. The IDT78C16 and IDT78C18 are available in a variety of ceramic DIP and LCC packages. From $15 (100).

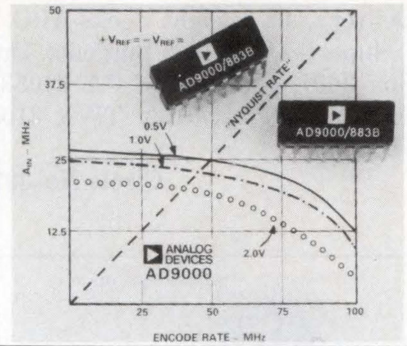
Integrated Device Technology Inc, Box 58015, Santa Clara, CA 95052. Phone (408) 727-6116. TWX 910-338-2070.

Circle No 399

6-BIT ADC

- *Features 75M-sample/sec encode rate with no missing codes*
- *Processed to MIL-STD-883B rev C*

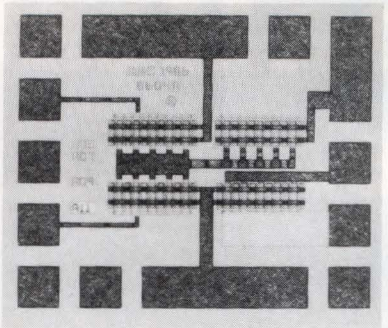
The AD9000 flash A/D converter guarantees a minimum encode rate of 75M sample/sec. You can use it in telecommunications, electronic-warfare-systems, and radar-guidance applications. The device features dc specifications of ±1-LSB max differential and integral nonlinearity, and ±1.5-LSB max initial offset error. Its dynamic linearity specs at ±0.5 LSB typ, when measured with a 15-MHz input signal. It



features a 42-dB signal-to-noise ratio, 44-dB in-band harmonics, and 46-dB 2-tone intermodulation rejection. An overflow bit lets you cascade converters to achieve higher resolution without reducing the sampling rate. AD9000SD/883B rev C, in a 16-pin DIP, $110; AD9000SE/883B rev C, in a 28-pin LCC, $120 (100).

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 935-5565. TWX 710-394-6577.

Circle No 400



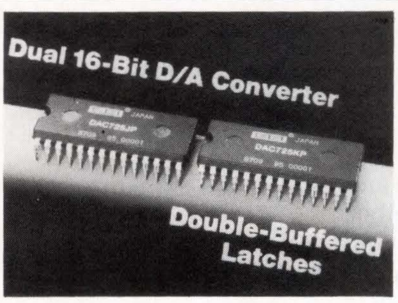
LASER-DIODE DRIVER

- *GaAs laser-diode current modulator*
- *Minimum bandwidth of 1.5 GHz*

The LDCM 1500A is a monolithic laser (or LED) driver for use in analog or digital fiber-optic systems. The device offers a minimum bandwidth of 1.5 GHz and a frequency response as high as 2.5 GHz. You can configure the input as either single-ended or differential. The bias current and the modulation current are both rated at 70 mA, and both are adjustable. The LDCM 1501A comes in a 10-pin surface-mount package. LDCM 1500A chip, $33 (100). Delivery for prototypes, four to eight weeks ARO.

Microwave Semiconductor Corp, 100 School House Rd, Somerset, NJ 08873. Phone (201) 563-6530.

Circle No 401



DUAL 16-BIT DAC

- *Double-buffered input register*
- *14-bit monotonicity*

The DAC725 is a dual, 16-bit DAC that incorporates dual, double-buffered data latches, a precision internal buried-zener voltage reference,

INTRODUCING 2AG FUSES

The world's smallest glass fuse.

Actual size: 0.177″ diameter x 0.58″ long;
Slo-blo® and fast-acting types, rated: ¼ ~ 7A, 250V or less.

Now you can get 3AG reliability and performance in a new economical subminiature size. Our Slo-blo® and fast-acting fuses are perfect for p.c. board and other limited space applications. Order them in bulk, or on tape and reel for high speed automatic insertion. New mating 2AG p.c. board fuse clips are also available.

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and output op amps. The device provides 16-bit resolution and 14-bit monotonicity over temperature. The output range is ±10V, and the settling time for a full-scale step is 4 μsec. Integral linearity error is ±0.003% of full scale. The design employs two DACs and two CMOS gate-array latch chips. The device loads data in two 8-bit bytes and provides separate lines for functions such as chip select, latch control, and clear. The device comes in a 28-pin plastic DIP. $34.90 (100).

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491.

Circle No 402

DUAL-POWER OP AMPs

- *Deliver output currents as high as 2.5A*
- *Protected against dc short circuits to supply rails*

The TCA2465 consists of dual-power op amps housed in a 9-pin power single in-line package. Each op amp within the device is internally compensated and can supply peak output currents as high as 2.5A. They operate from supply voltages between ±3V and ±20V. The op amps are internally protected against output short circuits to either supply rail and against thermal overloads. Operating from ±10V supplies, the op amps have a minimum open-loop gain of 70 dB at 100 Hz, a minimum common-mode input voltage range from −10 to +7V, and a typical slew rate of 2V/μsec. Under the same conditions, the output voltage can typically slew to ±8.5V at 1 kHz for a 4Ω load. The short-circuit current is typically 1A. The permissible differential input voltage ranges from the negative to the positive supply rail. TCA2465, $2.90; TCA2465A, a 16-pin DIP requiring external compensation, $2.40 (1000).

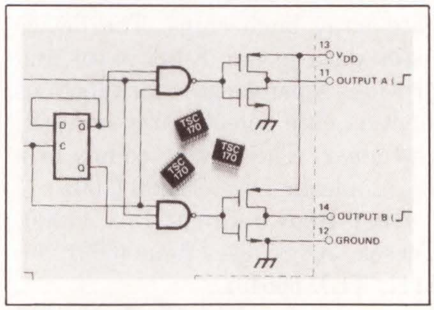
Siemens AG, Zentralstelle für Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089)

2340. TLX 5210025.

Circle No 403

Siemens Components Inc, 2191 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 980-4500.

Circle No 404



CONTROLLER

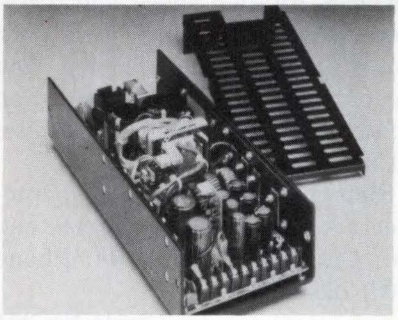
- *Features 3.8-mA max quiescent current*
- *Has dual totem-pole outputs*

TSC170/171 CMOS switching regulator ICs run at one-fifth the quiescent supply current of the equivalent, bipolar UC3846/3847. The lower supply current eliminates the need for high-wattage power resistors in off-line switching topologies. You can employ the current-mode control to parallel two or more power supplies for higher-power applications. The controller's dual totem-pole outputs can directly drive power MOSFETs or bipolar transistors. The units' output voltage swing equals the supply voltage, and each output's 50-nsec rise and fall times (1000-pF capacitive load) minimize power dissipation in the MOSFET switches. Each unit also features an internal voltage reference and undervoltage-lockout and soft-start capability. When in the off state, the TSC170 has low outputs and the TSC171 has high outputs. In a 16-pin plastic DIP, \$4; in a 16-pin wide-body small outline package, \$4.25 (100).

Teledyne Semiconductor, 1300 Terra Bella Ave, Mountain View, CA 94039. Phone (415) 968-9241. TWX 910-379-6494.

Circle No 405

COMPONENTS & POWER SUPPLIES



POWER SUPPLY

- *Has isolated, fully regulated outputs*
- *Features a 5V/40A main output*

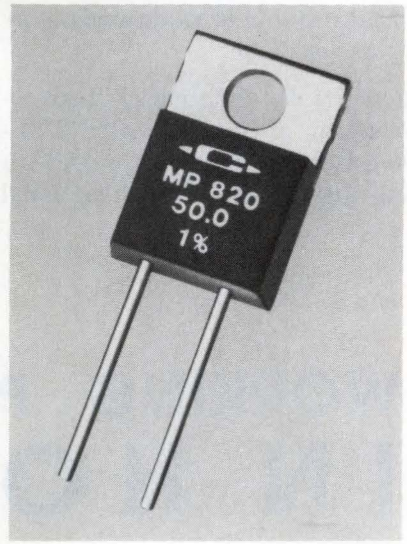
The 300W Model NQF 300 features four fully isolated and regulated outputs that have better than ±1% line, load, and cross regulation. Its transient recovery time equals 500 μsec for 50% load steps, and its main output is preset to 5V/40A. You can specify any combination of 5, 12, 15, or 24V for the three auxiliary outputs; the current can range to 10A pk on output 2, and 5A on outputs 3 and 4. Each output has full overload and short-circuit protection. You can select input ranges of 90 to 132 or 180 to 246V ac, 47 to 440 Hz. The supply meets UL, CSA, VDE, IEC, and BS safety standards and contains VDE standard RFI line filters. $345 (50).

Intelligence Power Technology Inc, 2111 Howell Ave, Anaheim, CA 92806. Phone (714) 937-1301.

Circle No 351

POWER RESISTOR

- *Housed in TO-220 power package*
- *Features ±1% standard tolerance*



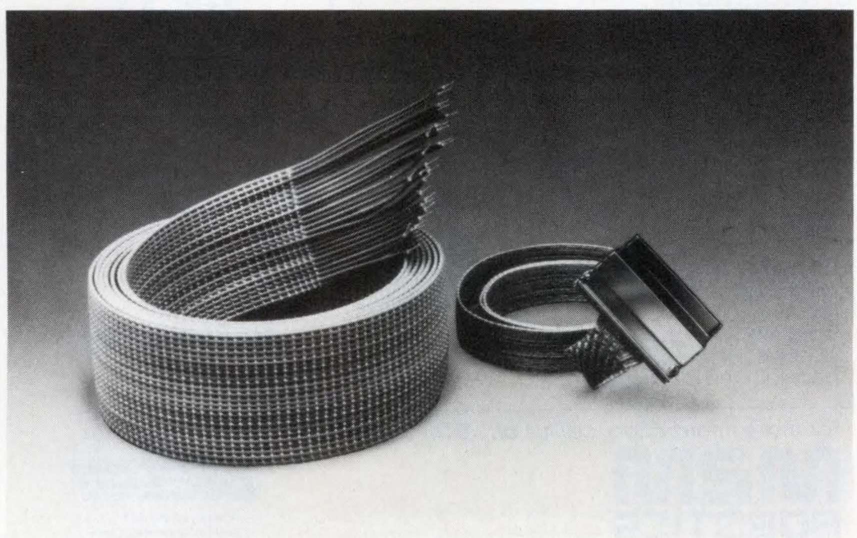
Housed in a TO-220 power package, the MP820 Kool-Tab device is a 20W heat-sink-mountable power resistor. The resistor employs a noninductive design that makes it suitable for high-frequency and power-switching circuitry. Its resistance values range from 10Ω to 1 kΩ and its standard tolerance equals ±1%. The resistor features a silicone case, which protects it from the environment, and a low profile, which permits you to fit it into tight spots. Its single-screw mounting design simplifies the task of attaching it to a heat sink. $1.90 (1000) for a 50Ω device. Delivery, six weeks ARO.

Caddock Electronics, 1717 Chicago Ave, Riverside, CA 92507. Phone (714) 788-1700. TWX 910-332-6108.

Circle No 352

COAXIAL CABLE

- *Highly flexible for easy bending, routing, and stowing*
- *Available with six to 64 signal conductors*



This subminiature ribbon coaxial cable is highly flexible. You can fold the cable upon itself, bundle it in rectangular or round sections, or group it with other cable for routing. To terminate each signal set, you secure the signal conductor and companion drain wire to the appropriate connector terminals. The vendor can provide custom-designed multilayer paddle cards or pc boards to eliminate impedance mismatch. You can order the cable in varying lengths, with six to 64 signal conductors, single or dual drain wires, and impedances of 50 to 130Ω. $1.25/ft (100 ft).

Woven Electronics, Box 667850, Charlotte, NC 28266. Phone (803) 963-5131.

Circle No 353

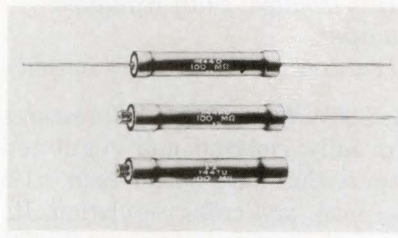
INTERRUPTER MODULE

- *Consists of a GaAlAs emitter and a hybrid photodetector*
- *Features a built-in daylight-suppression filter*

The SFH 910 differential photo interrupter module contains TTL-compatible circuitry that provides a counting pulse and a directional pulse that let you detect the direction of motion. The unit consists of a GaAlAs IR emitter and a hybrid photodetector. The photodetector encompasses a split photodiode with amplifiers, Schmitt triggers, and evaluation logic; the module also features a built-in daylight-suppression filter. Both the counting-pulse and directional-recognition signals are npn open-collector outputs compatible with TTL circuitry. You can use the module to encode mechanical-shaft rotation speed and direction. It accepts code wheels with slot widths as small as 0.85 mm. You can obtain a 96-slot code wheel as an option. SFH 910, $5.60 (1000); disc, $0.73.

Siemens Components Inc, Optoelectronics Div, 19000 Homestead Rd, Cupertino, CA 95014. Phone (408) 725-3520.

Circle No 354



RESISTORS

- *Withstand 50 kV in air or 100 kV in oil*
- *Are available in 1, 2, or 5% tolerance levels*

Produced by depositing a ruthenium oxide thick film onto a high-purity ceramic base, T40 Series high-voltage resistors can withstand a dc voltage as high as 50 kV in air or 100 kV when immersed in oil. The series includes three types with resistance values ranging from 1 kΩ to 4 GΩ, 1 kΩ to 15 GΩ, and 1 kΩ to 45 GΩ, respectively. The resistances are available with tolerances of ±1, ±2, or ±5% and temperature coefficients of ±25, ±50, or ±100 ppm/°C. A sleeve over the resistor protects it from mechanical damage and provides electrical insulation. From £3 to £10 (1000).

Welwyn Electronics, Bedlington, Northumberland NE22 7AA, UK. Phone (0670) 822181. TLX 53514.

Circle No 355

IRC Inc, Box 1860, Boone, NC 28607. Phone (704) 264-8861. TLX 469902.

Circle No 356

Mallory-brand Aluminum Electrolytics

Selecting this outstanding capacitor line just became an even wiser decision.

Because the company that makes them is now easier to work with. When RTE bought Mallory's aluminum electrolytic business, they didn't change a great product. It's still made on the same production lines by the same skilled work force.

What did change was the level of customer service — at the plant and in the field — to make it easier for you to get specifications, samples or engineering help, and check delivery schedules. Now when we give you a shipping date, we meet it or beat it 99% of the time!

How has all this been accomplished?

At the plant, by adding seasoned specialists, an in-house CAD-assisted engineering department, and a computerized order entry/customer service expediting system.

In the field, by assigning all Aerovox M aluminum electrolytics to the service-driven rep and distributor organization of our sister RTE company, Aerovox Inc., one of the world's largest capacitor makers, and a leading supplier of EMI filters.

So, next time you need aluminum electrolytics, call your Aerovox rep, or us, direct... because our product is still outstanding. And now, so is our service!

Now we're Aerovox MALLORY*

Send for our new Aerovox M technical bulletins today.

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CIRCLE NO 212

COMPONENTS & POWER SUPPLIES

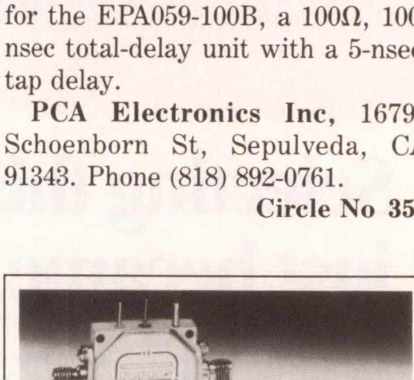
DELAY LINES

- *Available with a variety of impedance values*
- *Feature delays as long as 1000 nsec*

Housed in 24-pin DIPs, the EPA059, EPA060, and EPA061 Series 20-tap delay lines provide 20- to 1000-nsec delays. Each unit has four 50Ω lines with 20- to 200-nsec delays, six 100Ω units with 20- to 1000-nsec delays, and five 200Ω devices with 20- to 1000-nsec delays. Nominal tap-to-tap delays for all three series are 1, 2.5, 5, and 10 nsec for 50Ω lines; 1, 2.5, 5, 10, 25, and 50 nsec for 100Ω lines; and 1, 2.5, 5, 25, and 50 nsec for 200Ω lines. Maximum output rise times range from 3 to 20 nsec for 50Ω units and 3 to 100 nsec for the 100 and 200Ω lines. All lines have their outputs on pin 23. Inputs are on pin 1 for the EPA060 units and on pin 2 for EPA059 and EPA061 Series devices. $5.82 (1000) for the EPA059-100B, a 100Ω, 100-nsec total-delay unit with a 5-nsec/tap delay.

PCA Electronics Inc, 16799 Schoenborn St, Sepulveda, CA 91343. Phone (818) 892-0761.

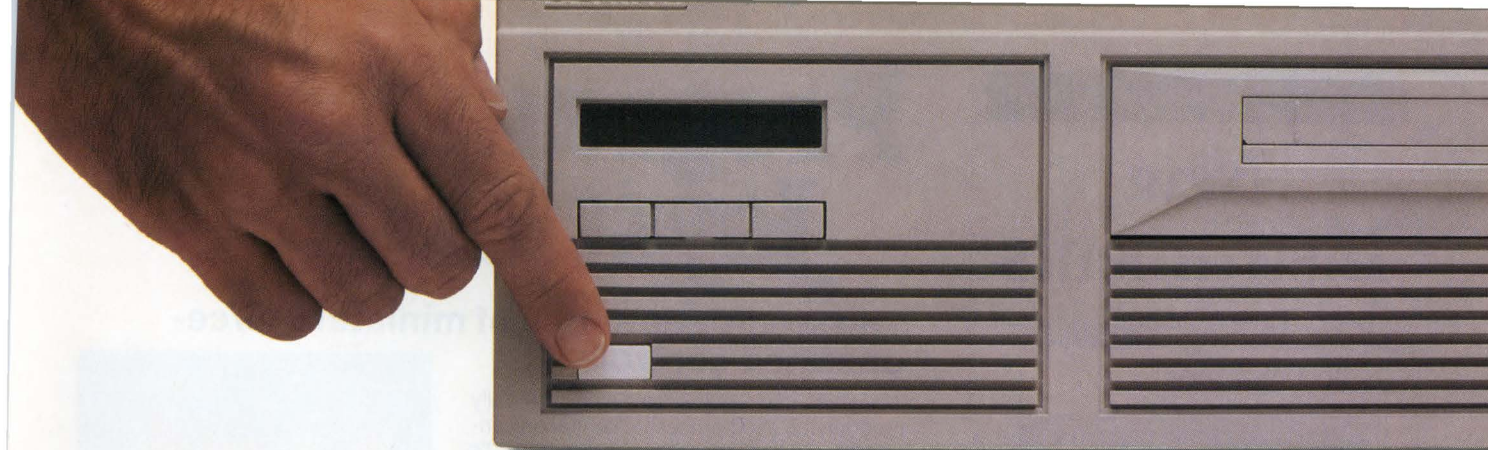
Circle No 357



MIXER

- *Operates over 2- to 26-GHz range*
- *Housing has removable SMA connectors*

The Model DBL2-26 biasable mixer operates over the 2- to 26-GHz range and provides IF signals from 1 to 500 MHz. It utilizes a self-adjusting bias arrangement in which the dc-bias level is reduced as the LO (local-oscillator) power is in-



Push button backup.

Low-cost backup
for HP9000 users.

For all the times you've wanted a simpler, smarter, more reliable way to backup your data, Bering has the answer.

Introducing ECHO. Automatic tape backup you can count on time after time after time.

Our ECHO 40MB tape backup drive is compatible with all HP9000 Series 200/300/500 users. It incorporates the kind of sophisticated features you'd expect from an expensive drive. Yet it's priced at about *half* the price of comparable systems.

ECHO doesn't sacrifice quality, either. It's extremely reliable, with built-in error corrections that let you rest assured you're not missing anything.

At the push of a button, your ECHO drive can copy 40MB of data from your hard disk, creating a "mirror image" of your

files. Other features like off-line operation let you perform backup or restore without a CPU. ECHO's timed-backup lets you automatically backup a project without being present. Menu-driven selections and LCD displays make operation easier. And at 2.4MB per minute, ECHO's backup is *very* fast.

Last, but not least, ECHO uses the latest space-saving 3M DC2000 mini tape cartridges–a tidy little addition to over-crowded work areas.

For a data sheet or more information, call us at **800 BERING 1.**
Bering Industries, 240 Hacienda Ave., Campbell, CA 95008.

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CIRCLE NO 211

creased. It has a usable LO power range of 10 dBm. The typical conversion loss is 9 dB with 0 dBm LO power. The mixer requires a bias dc of 12V at 8 mA. It's also available for use at 15V. The mixer is supplied in a drop-in housing that features removable SMA connectors. The housing measures 1×1×0.375 in. $1195. Delivery, 90 days ARO.

RHG Electronics Laboratory Inc, 161 E Industry Ct, Deer Park, NY 11729. Phone (516) 242-1100. TWX 510-227-6083.

Circle No 358

TRIMMERS

- *Rated for 500 mW at 70°C*
- *Feature 1000-hour full-load life*

The adjustable screw design of each CT-9 Series 18-turn trimmer resistor permits actuation of a worm gear that turns a wiper assembly around the trimmer's circular resistive element. The trimmers' resistance values range from 10Ω to 5 MΩ. Their multicontact precious-metal wipers have low 1% contact-resistance variations. The trimmers are rated for 500-mW at 70°C and are derated to 0W at 125°C. Their other specs include a 300V dc max voltage rating, a 200-cycle rotational life, and a 360-g-cm shaft torque rating. Sealed with O-rings, the trimmers pass leak tests at 85°C and can withstand soldering temperatures of 350°C for as long as 3 sec. Their operating range spans −55 to +125°C. $0.79 (5000).

Mepcopal, 11468 Sorrento Valley Rd, San Diego, CA 92121. Phone (619) 453-0332.

Circle No 359

PRESSURE SENSOR

- *Interfaces with most harsh media*
- *Temperature compensation over 0 to 50°C*

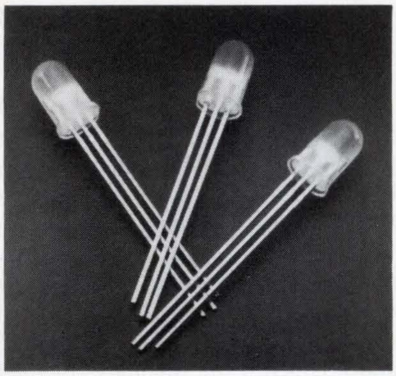
The Model 84 pressure sensor is available in gauge and sealed-gauge

ranges from 5 to 300 psi and in absolute ranges from 5 to 50 psi. Its accuracy is ±0.5%. The unit has a stainless-steel housing, which uses silicone oil to couple a diffused piezoresistive sensor to a convoluted, flush, stainless-steel diaphragm. The diaphragm interfaces with most harsh media. Integral laser-trimmed resistors provide tempera-

ture compensation and calibration over 0 to 50°C. For a 1.5-mA supply current, the nominal output span equals 100 mV. The device is ±1% interchangeable. $50 (OEM qty). Delivery, stock to six weeks ARO.

IC Sensors Inc, 1701 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 432-1800.

Circle No 360



2-COLOR LEDs

- *Combine red and green LEDs in one package*
- *Luminous intensities range to 8 mcd*

Housed in a 3-lead, industry-standard T-1¾ package, HLMP-4000 bicolor LED lamps contain a red chip and a green chip. The leads are spaced on 0.05-in. centers, with the center lead providing the common-cathode connection. The viewing angle is 65°. The typical luminous intensity, at a 10-mA forward current, measures 5 mcd for the red chip and 8 mcd for the green chip. $0.46 (10,000).

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 361

TRANSISTORS

- *Have collector breakdown voltages as high as 300V*
- *Maintain gain at high collector currents*

The ZTX-554, -555, -556, and -557 are high-voltage medium-power pnp transistors. The ZTX-554 and -555 have collector-emitter breakdown voltages of 125 and 150V, respectively; both have a gain of 50 to 300 at a collector current of 300 mA. Their maximum collector current equals 1A, and their power rating specs at 1W. The ZTX-556 and -557 have collector-emitter breakdown voltages of 200 and 300V, respectively; both have a gain of 50 to 300 at a collector current of 50 mA. You can obtain all the devices in TO-92 cases. You can also order the ZTX-555 and ZTX-557 transistors in surface-mount packages that come on 16-mm tape for use with automatic placement equipment. $0.17 to $0.20 (1000).

Ferranti Electronics Ltd, Fields

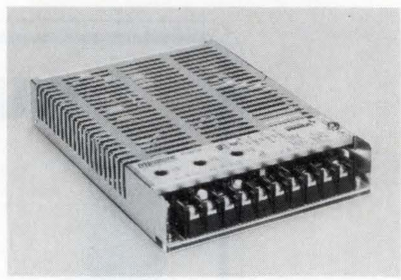
COMPONENTS & POWER SUPPLIES

New Rd, Chadderton, Oldham, Lancashire OL9 8NP, UK. Phone 061-624 0515. TLX 668038.

Circle No 362

Ferranti Electric Inc, 87 Modular Ave, Commack, NY 11725. Phone (516) 543-0200. TLX 6852104.

Circle No 363



POWER SUPPLIES

- *Offer power levels of 25 to 150W*
- *Feature 20-msec min holdup time*

Housed in enclosures that are UL recognized and CSA certified, the 34 models in the Mustang series of switching power supplies provide output powers of 25, 50, 70/80, 100, and 150W. All models feature an input EMI filter, inrush-current limiting, output-voltage adjustment, built-in overload protection, and typical operating efficiencies of 70 to 75%. Low-line to high-line regulation equals 0.4% and no-load to full-load regulation equals 0.8%. All models have a 20-msec min hold-up time. From $59.50 (1000).

Computer Products Inc, 2900 Gateway Dr, Pompano Beach, FL 33069. Phone (305) 974-5500. TWX 510-956-3098.

Circle No 364

PRESSURE SENSORS

- *Designed for hostile media in harsh environments*
- *Can sense from 15 to 300 psig*

ST2000G Series pressure transducers are suitable for measurement of hostile media in harsh environments. Encased in rugged stainless-

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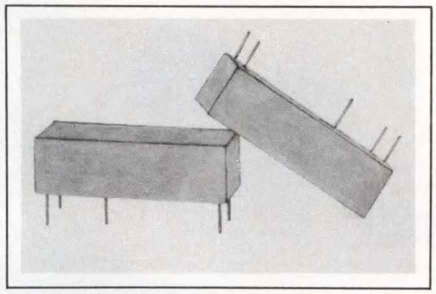
MICRO SWITCH
a Honeywell Division

CIRCLE NO 218

steel packages, the transducers each feature an IC sensor element and signal-conditioning circuitry. They have pressure-sensing capability that ranges from 15 to 300 psig (pressure per square inch of gravity). You can obtain the tranducers with either 1 to 6V dc or 2.5 to 12.5V dc for each pressure range. Their sensor output options include full-scale spans of 5V±200 mV, and zero-pressure offsets, trimmed to within ±100 mV, that allow you to interchange transducers without recalibrating. All the transducers feature temperature compensation to within ±0.02%/°C. The sensors are optimized for 0 to 70°C operation but will operate from −40 to +85°C. The transducers' operating voltage ranges from 12 to 30V dc. $125.

Sensym Inc, 1255 Reamwood Ave, Sunnyvale, CA 94089. Phone (408) 744-1500.

Circle No 365



FILTERS

- *150- to 200-MHz frequency range*
- *Ripple is 1 dB max*

The units in this line of LC filters feature a 4-pole response with a nominal frequency range of 150 to 200 MHz. Typical 3-dB bandwidths of ±10 MHz are available; units are also available with a 50-dB bandwidth of ±60 MHz. The operating range spans −35 to +85°C. The filters have 1 dB max ripple and 4 dB max insertion loss. The standard source and load impedance is 50Ω. From $115.

Piezo Technology Inc, Box 7859, Orlando, FL 32854. Phone (305) 298-2000. TWX 810-850-4136.

Circle No 366

ANALOG LINK

- *10,000-ft transmission capability*
- *0.3% min accuracy*

This fiber-optic module transmits 4- to 20-mA or 0 to 10V dc analog signals. Its transmission range is 10,000 ft. The optical encoding of data is based on signal frequency and is therefore not subject to error

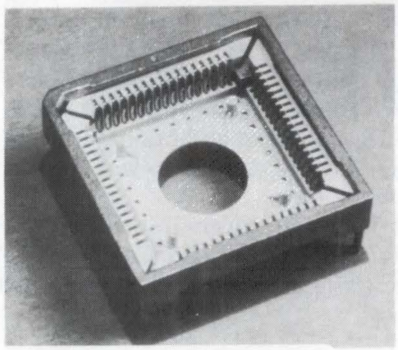
caused by fluctuations in the received optical power. The link has a minimum accuracy of 0.3% and a response time of 2 msec max. The transmitters have LED indicators for power, overrange, and underrange signals. The receivers have LEDs and open-collector outputs to indicate overrange and lock conditions; the lock condition indicates that the receiver is accepting valid signals. $900/pair.

EOTec Corp, 420 Frontage Rd, West Haven, CT 06516. Phone (203) 934-7961.

Circle No 367

BURN-IN SOCKETS

- *Available in 20- to 68-position versions*
- *Feature housings rated for 200°C operation*



These low-insertion-force, burn-in sockets come in 20- to 68-position versions. They accept square, plastic chip carriers with J leads on 0.05-in. centers. The units feature liquid crystal polymer housings rated for continuous operation at 200°C. You can obtain them with three types of contacts: beryllium copper rated to 200°C, beryllium copper rated to 150°C, and phosphor bronze rated to 125°C. The contacts feature nickel-boron platings. The sockets have metal-locking frames that reduce insertion forces, and positive ejection systems that facilitate manual or automatic loading and unloading and that also improve heat exchange. Their insertion life specs at 5000 cycles min. From $8, depending on model and quantity.

Mark Eyelet Inc, 63 Wakelee Rd, Wolcott, CT 06716. Phone (203) 756-8847. TWX 510-600-7291.

Circle No 368

SUPPRESSORS

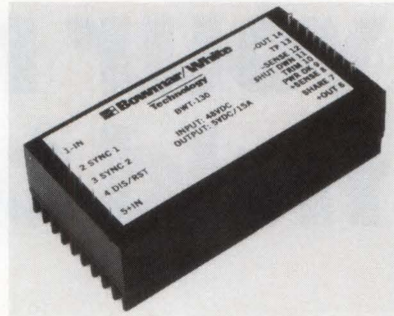
- *Designed primarily for field installation*
- *Feature a short-circuit failure mode*

420E2 Series transient voltage suppressors are suited for field installation on equipment that has inadequate levels of transient protection. Each model has two pairs of circuits with line-to-line and line-to-ground protection. The family includes de-

vices with operating line voltages of ±12, ±25, ±28, ±36, ±50, and ±60V max; the maximum clamping voltages (at 2000A) spec at 22, 44, 46, 60, 80, and 95V, respectively. You can make electrical connections easily, using two screws for line connections and three fork terminals for equipment connections. The suppressors feature a short-circuit failure mode. Their maximum standby current equals 5 μA and their line throughput resistance specs at 12Ω. All the suppressors operate from −55 to +100°C. From $24 (100).

General Semiconductor Industries Inc, 2001 W Tenth Pl, Tempe, AZ 85281. Phone (602) 968-3101.

Circle No 369



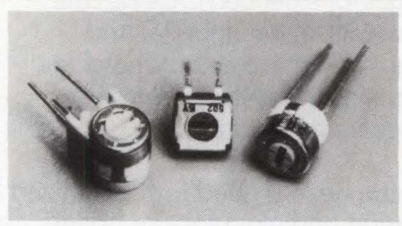
DC/DC CONVERTER

- *Delivers 5V at 15A*
- *400-kHz switching frequency*

The Model BWT-130 switch-mode dc/dc converter converts an unregulated 48V dc input to a regulated 5V output at currents ranging to 15A. The converter has a 5.7 W/in.^{3} power density and an 80% min efficiency. The fixed-frequency operation is 400 kHz, and the noise is less than 0.5% p-p from dc to 20 MHz. Other features include a 0.2% max load regulation, 0.1% max line regulation, overvoltage protection, current limiting to 18.8 A, 2000V dc min input-output isolation, and a typical no-load power consumption spec of 0.5W. The operating range, with natural convection, spans −20 to +60°C. $300.

Bowmar/White Technology Inc, 4246 E Wood St, Phoenix, AZ 85040. Phone (602) 437-1520.

Circle No 370



TRIMMERS

- *Designed for high-density applications*
- *Sealed to withstand board-washing processes*

The RJ-4 and ST-4C are single-turn, cermet trimmers. The RJ-4 is housed in a TO-18-type package, which measures 0.193×0.177 in. It

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Choosing the right fan for your application is easy, when you choose PAPST. Simply because PAPST offers the broadest line of AC and DC tubeaxial fans in the world.

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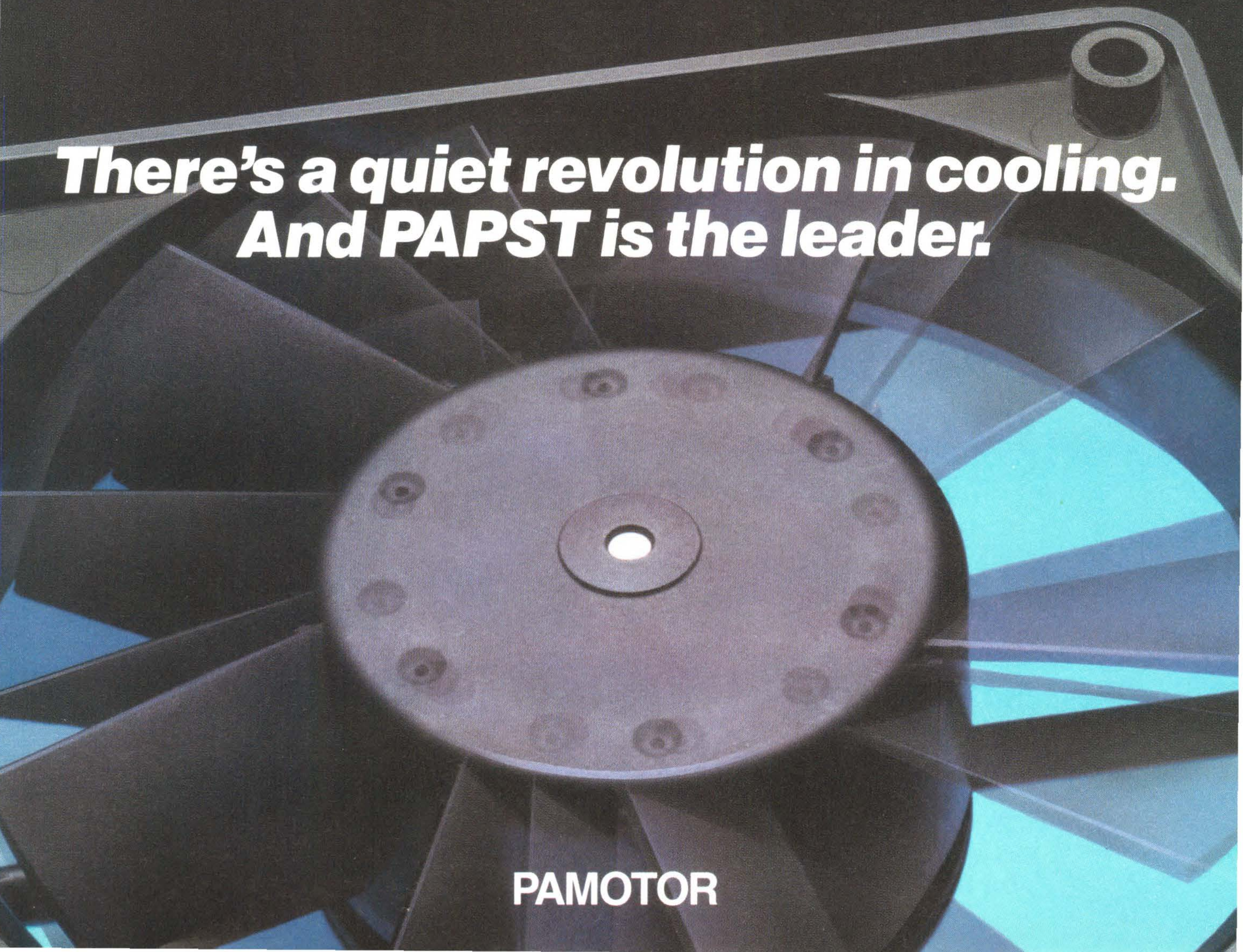
1-800-262-5226 (MA only)

CIRCLE NO 207



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Score the MS-DOS-Compatible System On a Chip from NEC

Now you can score on your next round of systems designs *and* parlay your MS-DOS investment. Simply use our CMOS V25™ Whole in One™ — the new 16-bit microcomputer on a chip from NEC.

It lets you tee off with features like a 16-bit ALU, two full-duplex UARTs, true STOP and HALT modes, and a whole lot more.

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Check out the V25's real strengths. Full support, for one. It's here now with hardware and software tools including EPROM/OTP parts. And you're supported by regional design centers with an increasing number of application engineers.

Stand-alone ICE and PC-based mini-ICE use our relocatable assembler and C compiler to provide powerful development capability for system designers.

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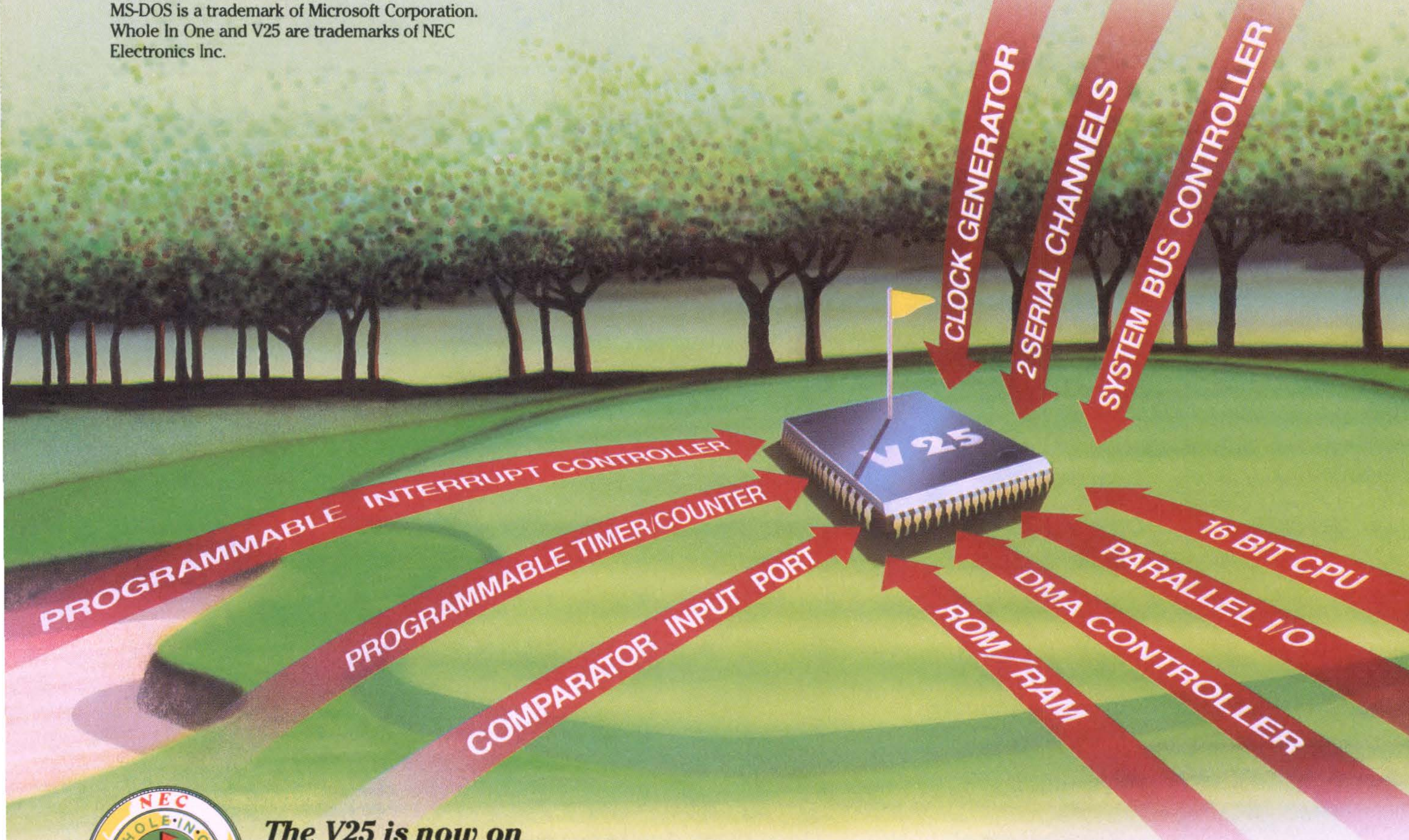
NEC Electronics Inc.
401 Ellis Street, P.O. Box 7241
Mountain View, CA 94039



The V25 is now on distributor shelves for immediate delivery

NEC

CIRCLE NO 219

has a power rating of 500 mW and is available in top- or side-adjust configurations. The ST-4C measures 0.177×0.197×0.091 in. It's available with top adjustment. Both trimmers have a resistance range of 10Ω to 2 MΩ and a standard tolerance of 20% (10% tolerance is available). Both of them also have a 1% max CRV (contact-resistance variation) and are sealed with an O-ring, which enables them to withstand a variety of board-washing procedures. RJ-4, $1.10; ST-4C, $0.77 (1000).

Mepcopal Co, 11468 Sorrento Valley Rd, San Diego, CA 92121. Phone (619) 453-0332.

Circle No 371

KEYBOARDS

- *Feature an optional remote bar-code reader*
- *Come bundled with an enhanced version of Smartkey*

G80-2000 Series keyboards have an identical layout to the IBM 3270 keyboard, with 24 function keys along the top and 10 keys on the left. Normally, only software written for the 3270 recognizes the extra function keys. However, the vendor's keyboards come bundled with an enhanced version of Smartkey so that users of IBM PC/XT, PC/AT, or compatible computers can take advantage of the extra keys. You can obtain N-key rollover, LED actuation-indicators, and programmable autorepeat as options. You can order the keyboards with a low-profile housing that conforms to DIN standards. All the keyboards come with US/International, French, and German character layouts. You can also obtain custom versions of the keyboard that offer other layouts. $900 with all options.

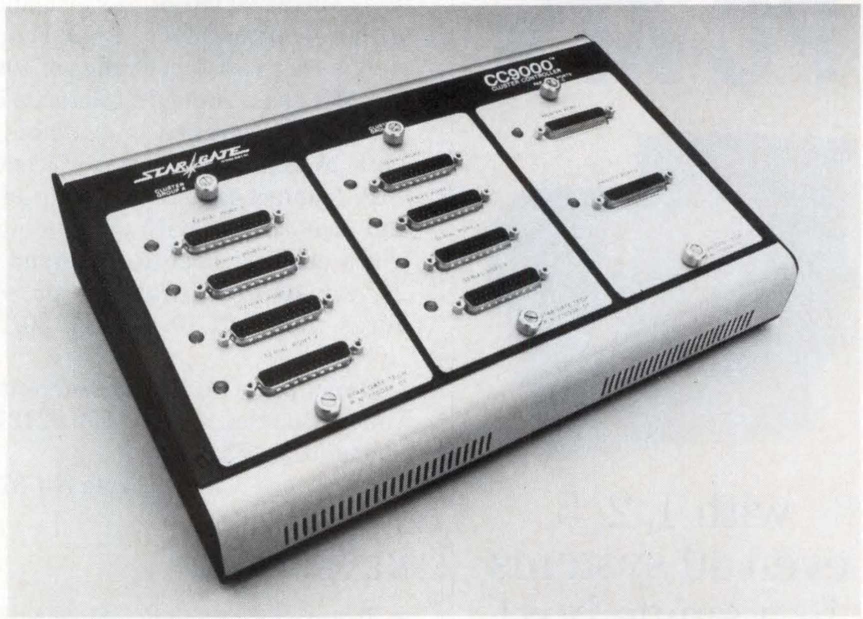
Cherry Electrical Products, 3600 Sunset Ave, Waukegan, IL 60687. Phone (312) 360-3500.

Circle No 372

COMPUTERS & PERIPHERALS

CLUSTER CONTROLLER

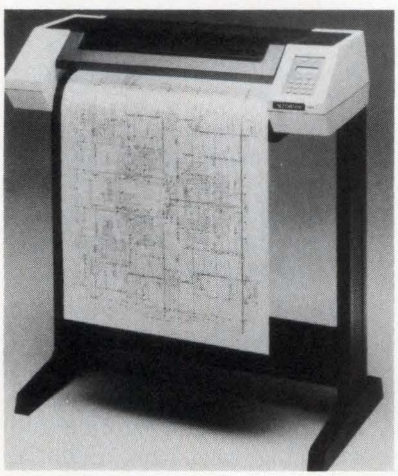
- *Can control 10 devices 800 ft from a PC*
- *An 80186 offloads I/O tasks from the host CPU*



The CC9000 is an 80186-based communications control device. It provides eight serial and two parallel ports and can control devices located as far as 800 ft from the host PC. Since the host connection is compatible with a StarLAN interface, you can connect each unit to the host via a StarLAN hub or minihub interface card. The unit handles full-duplex operations and programmable baud rates from 50 to 38.4k baud. The host connection takes place via inexpensive, unshielded twisted-pair telephone wire. Using its µP, 512k bytes of RAM, and proprietary system software, the unit offloads some of the I/O tasks from the host. It supports PCs and terminals running the MS-DOS-compatible PCMOS/386 multiuser operating system from Software Link. 8-port unit, $1295; upgradable 4-port unit, $1295.

Star Gate Technologies Inc, 33,800 Curtis Blvd, Eastlake, OH 44094. Phone (800) 782-4283; in OH, (216) 951-5922.

Circle No 407



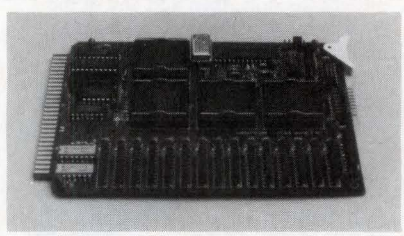
PEN PLOTTER

- *Organizes plot data to minimize pen movements*
- *Plots at 30 ips on axis at a 2g acceleration rate*

The 1023 pen plotter provides a plotting speed of 30 ips on axis at a 2g acceleration rate; its diagonal plotting speed is 42 ips diagonally at a 2.8g acceleration rate. A look-ahead feature keeps the pen moving at high speed when a line changes direction by <45°. One of its two 68000 µPs controls servo motion and linear pen motion, and the other controls data communications and management. Communications take place via an RS-232C interface with speeds to 19.2k baud. A data-management algorithm organizes plot data to minimize pen movements and pen changes. The algorithm searches the data structures stored in memory to plot the vector closest to the current pen position. An 8-pen rotating turret gives you a choice of eight colors or pen types. An optical sensor determines the type of pen selected and automatically adjusts pen force and velocity. Adjustable pinch rollers can handle media sizes from 8.5×11 in. to 25×36 in. The plotter also has an MTBF of 3000 hours. $4895.

CalComp, 2411 W La Palma Ave, Anaheim, CA 92801. Phone (714) 821-2142.

Circle No 408



GRAPHICS BOARD

- *Color graphics board for STD bus has an ACRTC processor*
- *Board attains drawing speeds of 2 million pixels/sec*

The HRG-1000 is a color graphics board for the STD bus that features a Hitachi ACRTC graphics processor. The board can attain draw-

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2. MULTIPIN WITH 8-200 AMP CONTACTS

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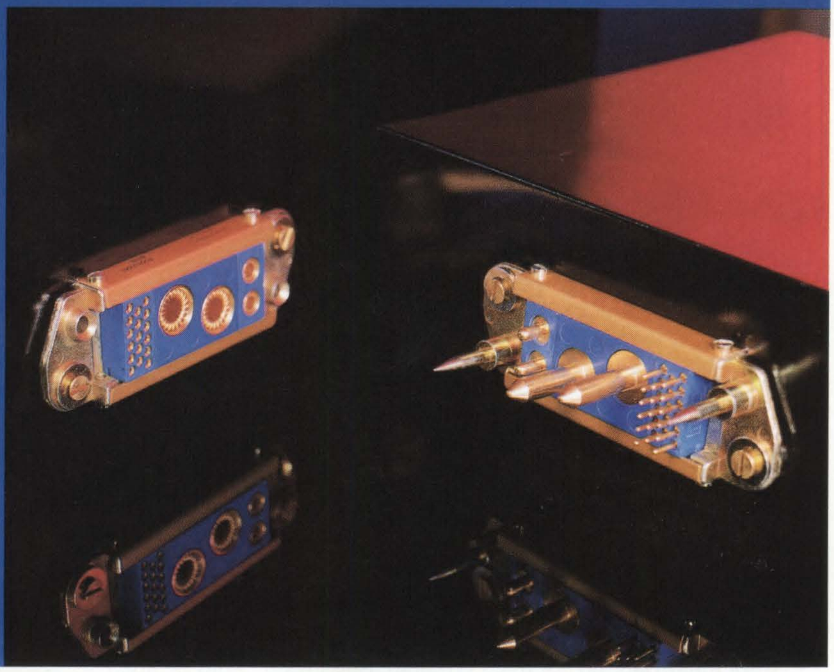

Only Hypertronics ends the compromise in power supply connectors for backplane subassemblies—in military, computer and other electronic systems—by combining Low Insertion Force (LIF) power, signal and MIL spec reliability in a single rack & panel connector.

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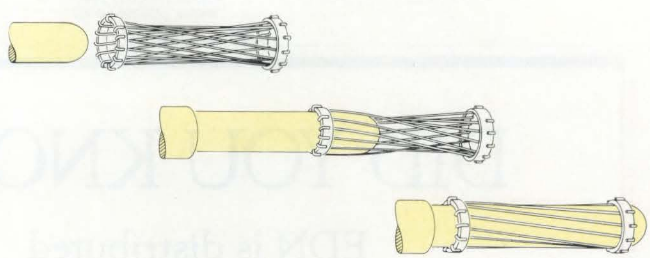

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"New Horizons in Connectors"

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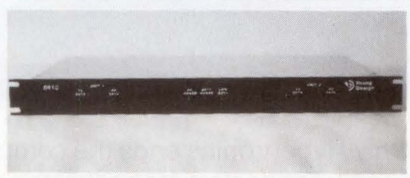
CIRCLE NO 206

ing speeds of 2 million pixels/sec. When used with an analog monitor, it can provide 16 simultaneous colors from a palette of 4096 colors. The board also works with TTL RGB input color monitors that have resolutions ranging from 320×200 pixels to more than 800×600 pixels. It includes 25-MHz and 32-MHz video output clocks and is programmable for the number of horizontal pixels, the number of lines, and synchronization rates. The board supports multiple screens, panning, zooming, windows, clipping, and more than 20 high-level drawing commands including lines, rectangles, polylines, polygons, circles, ellipses, and arcs. The board occupies an 8-byte block in the I/O or expanded I/O space. It requires 5V at 2.2A typ. $664.

Cobra Systems, 14,700 Main St, Suite 3, Bellevue, WA 98007. Phone (206) 641-2759.

Circle No 409



JITTER REMOVER

- *Removes jitter on data from a master port*
- *Distributes reconditioned data to four ports*

The DR-10 removes jitter from asynchronous data present on a master port and redistributes it to four auxiliary ports. It also removes jitter on data received from any of the four auxiliary ports prior to sending the data to the master port. All ports are RS-232C compatible and the redistributed data is time delayed by one byte. The unit operates full duplex at data rates from 300 to 9600 bps. The master port is configured as DCE (data communications equipment) and the auxiliary ports are configured as DTE

(data terminal equipment) to allow transparent insertion of the device in an RS-232C line. You can install one or two independent channels in a 1¾-in. standard 19-in. rack enclosure. The unit also has a battery backup option that powers the unit for more than 10 hours when ac power is removed. Single-channel unit, $1195; dual-channel unit, $1695.

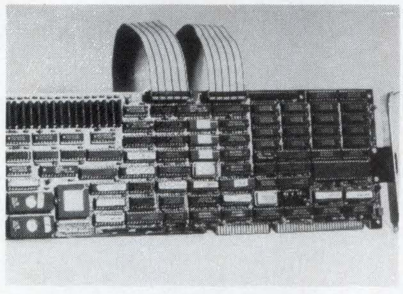
Young Design Inc, 7882 Tyson Oaks Circle, Vienna, VA 22180. Phone (703) 448-8939.

Circle No 410

FRAME STORE

- *1024×2048-pixel logical resolution*
- *Provides onboard color-image processing*

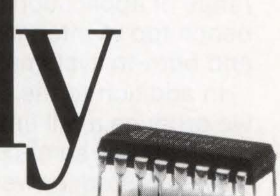
The FS1000 Frame Store board provides IBM PC/ATs and compatible computers with image-processing

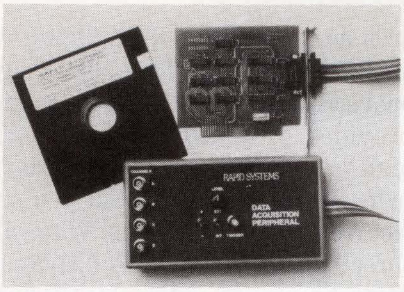


capabilities. The board is based on a 68010 μP; it has 2M bytes of video RAM and a Brooktree Bt453 color palette IC that provides as many as three overlay colors and displays as many as 256 colors from a palette of 16M colors in the video image. Onboard image-processing capabilities include image compression, zoom, and scrolling. The device sends the image to a standard RGB color monitor. Address mapping in the video RAM allows you to position single or multiple images anywhere on the screen. The text/graphics overlay facility allows you to add information to the screen without destroying the video-image information. A software library of image-processing routines is available for the board. To expand the board's image-processing capabilities, you can link it to a Data Translation (Marlborough, MA) DT7020 32-bit floating-point array processor, via the Data Translation DT-connect bus. This connection lets you avoid using the PC/AT bus to transfer information between the two boards. The vendor is developing a piggyback frame grabber for the board. The FS1000 comes in two versions: one for use with NTSC color signals, one for use with PAL color signals. It costs $4995, including a manual and sample programs.

Camtrel Computer Systems Ltd, Unit 101, Cambridge Science Park, Milton Rd, Cambridge CB4 4FY, UK. Phone (0223) 61506. TLX 94012250

Circle No 411





PERIPHERAL DEVICE

- *Offers 4-channel data acquisition for IBM PC or compatibles*
- *Acquires data at 1- to 500-kHz sample rates*

The R414 peripheral device for the IBM PC provides four data-acquisition channels. Its sampling rates range from 1 to 500 kHz, and its 8-bit A/D converter triggers on an internal or external analog signal. You can adjust the unit's gain so that the analog-input-voltage range spans 10 mV to 320V p-p. All of the unit's inputs have diode protection. The unit comes with user programs and subroutines written in C, Turbo Pascal, or Basic. You can obtain software that lets you operate the unit as a digital oscilloscope or spectrum analyzer; digital-signal-processing hardware is also available. $295.

Rapid Systems, 433 N 34th St, Seattle, WA 98103. Phone (206) 547-8311. TLX 265017.

Circle No 412

COLOR MONITOR

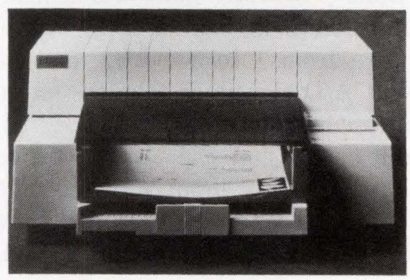
- *Has automatic frequency scanning*
- *Provides graphics resolution to 800×600 pixels*

The Spectrasync 1437 is a color monitor with automatic frequency scanning from 15.5 to 37 kHz horizontally and from 50 to 90 Hz vertically. The monitor automatically adjusts the aspect ratio (the horizontal

and vertical dimensions and positions) to preset values. This adjustment allows the monitor to maintain the image on the screen at the desired size regardless of the scanning frequency. The monitor can be used with the IBM PS/2; the IBM PC, PC/XT, PC/AT, and compatibles; and the Apple Macintosh II. It supports IBM's CGA, EGA, PGA, VGA, and MCGA graphics standards and can accept TTL digital or analog video inputs. The 14-in. diagonal screen has a 0.31-mm pitch and provides graphics resolutions as high as 800×600 pixels. Three front-panel RGB pushbuttons let you select from seven text colors. When all three buttons are off, the display is monochrome. An optional tilt/swivel base is available. $849. Tilt/swivel option, $29.

Idek America Inc, 204 S Olive St, Rolla, MO 65401. Phone (314) 364-7500.

Circle No 413



PRINTER

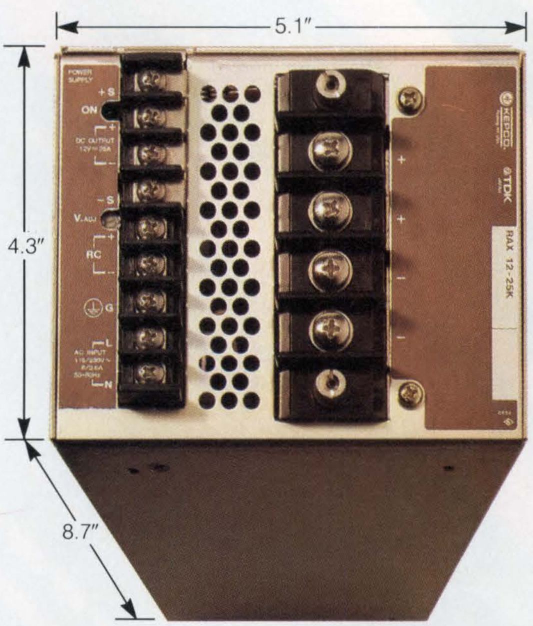
- *Provides laser-quality output for $995*
- *Prints text at speeds of 120 cps*

The DeskJet is a personal printer with laser-quality output. It employs inkjet technology, but prints high-resolution text and full-page graphics at 300 dots/in. It prints text at speeds of 120 cps for laser-quality text and 240 cps for draft quality. The printer features an automatic cut-sheet feeder (to 100 sheets) and a front-loading design for quick reloading of paper. It can accommodate US letter, legal, and European A4 paper sizes, as well as manually fed #10 business envelopes. The printer has Courier, Courier Bold, and Courier Compressed fonts built in. Two accessory-cartridge ports extend the available font types. These ports also provide memory expansion (to 256k bytes of RAM) for soft fonts and provide an interface for an FX-80 printer emulation cartridge. The printer has a 16k-byte buffer and

New 150KHz switcher.
4.3 inches high.
50 to 1500 Watts.
SELV.
And loaded.

- 8mm primary-secondary and 4mm primary-ground spacings for a SELV (**S**afety **E**xtra **L**ow **V**oltage) power supply per IEC 380/VDE 0806. UL recognized, CSA certified. VDE/IEC certified by TÜV Rheinland.
- On-board dual-choke filter meets FCC Class A.
- MIL STD 810D certified.
- 75-80% efficiency.
- Soft start.
- Power on LED.
- Remote on/off, optically isolated.
- Remote error sensing.
- Voltage adj +10, −30%.
- Overvoltage protection.
- 115/230V a-c selectable input.
- 300V d-c input.
- Current share (1500W).
- The 300W and 1500W models have undervoltage protection.
- Holding time: 20msec. min, 30msec typ.
- Supplied fully enclosed for industrial applications.

All built-in. No extra cost.*



Shown:
300-Watt Model
RAX 12-25K
(Output 12V/25A).

***Price complete:**
50W — $199
100W — $289
175W — $380
300W — $520
1500W — $1450
Quantity discounts available.

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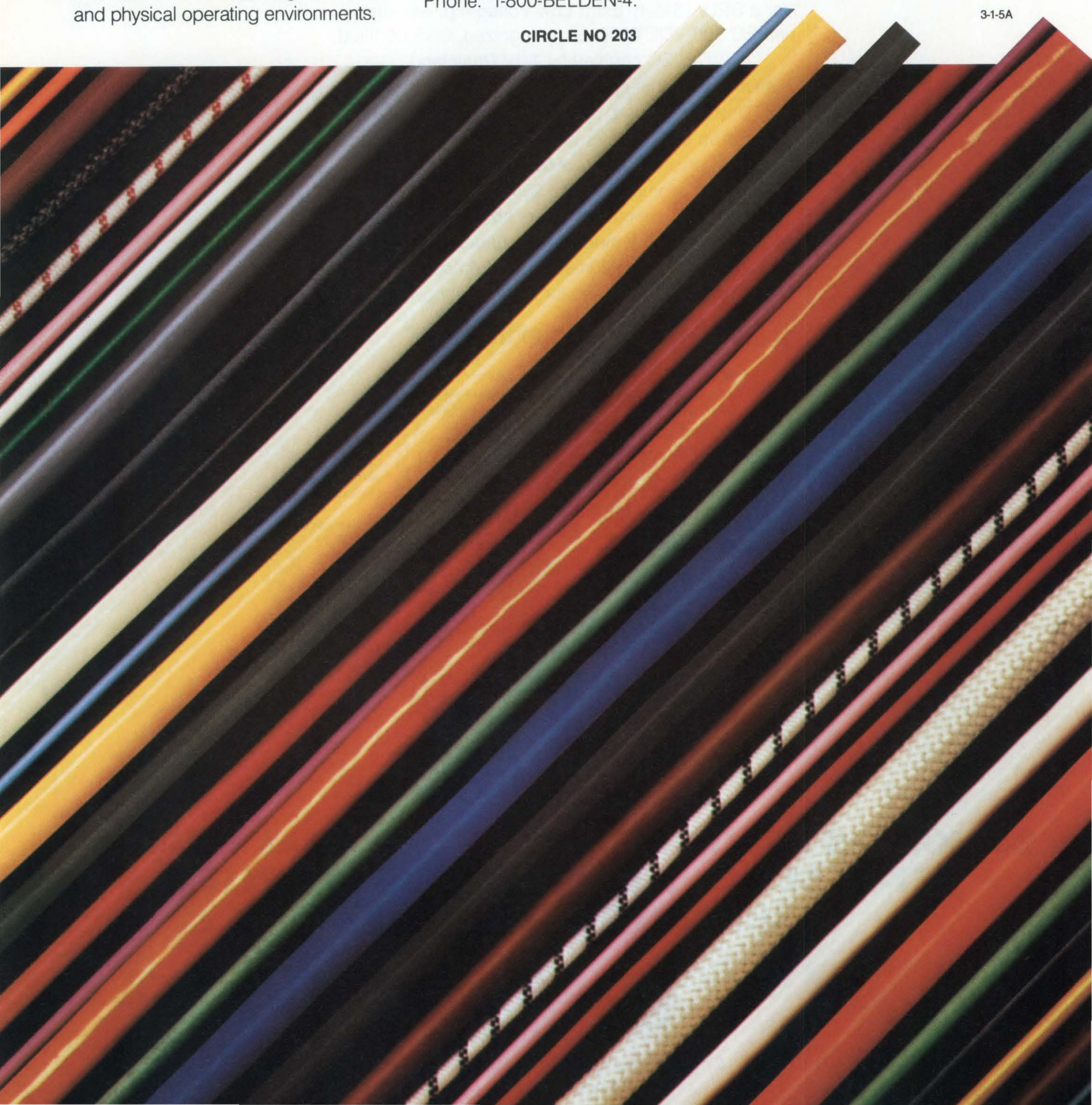
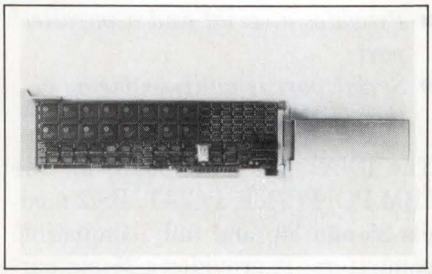


employs the company's PCL printer language. Either an RS-232C or a Centronics parallel port serves as the computer interface. $995.

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 414



COMMUNICATION BOARDS

- *Provide either eight or 16 serial ports for the IBM PS/2*
- *Feature communications for multiuser operating systems*

PS-COM/X Series boards for the IBM PS/2 models 50, 60, and 80 feature either eight or 16 asynchronous serial communications ports per board. You can mount as many as four of these 16-channel boards on the PS/2 Bus to provide 64 serial ports. You can select data-transfer rates from 50 to 56k baud for each port. The boards use high-speed 16450 UARTs and are compatible with the DOS, OS/2, Xenix, Unix, Theos, Pick, QNX, and PC-MOS operating systems. Each port provides full modem control. You can mount as many as 16 RJ-45 connectors in a compact, shielded extension that mounts on the faceplate connector extending from the board. The connector allows you to use multiple boards in a system that has either RJ-45 or RJ-11 cabling. COMware software allows DOS to access as many as 64 COM ports. 8-port version, $895; 16-port version, $1295.

DigiBoard Inc, 6751 Oxford St, Saint Louis Park, MN 55426. Phone (800) 344-4273; in MN, (212) 922-8055.

Circle No 415

RAM BOARD

- *Provides 4M bytes of iLBX-II memory for Multibus II systems*
- *Has a refresh mode suited to video acquisition*

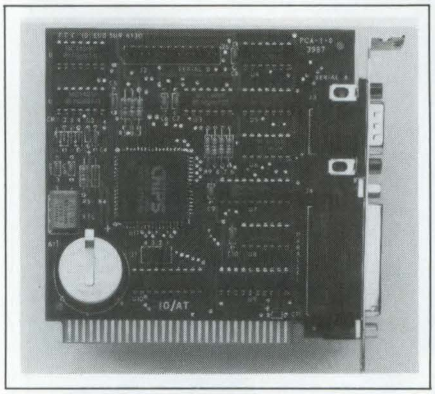
The FAB104 Multibus II-compatible memory board provides 4M bytes of parity-checked dynamic RAM, which is sent to an iLBX-II bus on its P2 connector. The board supports 8-, 16-, 24-, and 32-bit data transfers, and 26-bit addressing on the iLBX-II bus. It has a read-access time of 375 nsec and a write-access time of 250 nsec. You can program a variety of board parameters—including its base-address and refresh modes—via the Multibus-II interconnect space, which is supported on the iLBX-II bus. One of the board's refresh modes is designed to allow the board to acquire video information and support image-processing operations in real time. The board typically draws 3.5A from its 5V supply. FrFr 34,200.

Centralp Automatismes, 16 rue Gabriel Peri, 92120 Montrouge, France. Phone (1) 42533617. TLX 632380.

Circle No 416

I/O BOARD

- *Provides a serial and a parallel port*
- *Serial port is addressable as either COM1 or COM2*



The IO/AT is an I/O board for the IBM PC, PC/XT, PC/AT, PS/2 models 25 and 30, and fully compatible computers. It provides a 25-pin parallel port, which you can address as LPT1, LPT2, or a user-selectable port. It also provides a 9-pin serial port that you can address as COM1, COM2, or a user-selectable port. An NS16450 UART chip provides the interface to the serial port. An optional 25-pin serial port is also available. You can access the additional serial port by connecting a ribbon-cable assembly to the board. If you install four of the boards, each with the optional serial port, in your PC, the PC will be able to communicate with as many as eight serial devices. The board has no switches or jumpers to set, so a particular configuration is completely software controlled. Once the address selections have been made, they are stored on the board in static RAM that's pow-

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VI-200's deliver as much as 200W from 5.5 In.³

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VICOR Corporation, 23 Frontage Road, Andover, MA 01810 Tel: 617-470-2900, TWX: 910-380-5144, FAX: 617-475-6715

CIRCLE NO 220

ered by a lithium battery. The boards measure 4.3×4.2 in. and are FCC Class B certified. IO/AT board with one serial and one parallel port, $119; with two serial and one parallel ports, $139.

Boca Research Inc, 6401 Congress Ave, Boca Raton, FL 33487. Phone (305) 997-6227. TLX 990135.

Circle No 417

HANDHELD TERMINAL

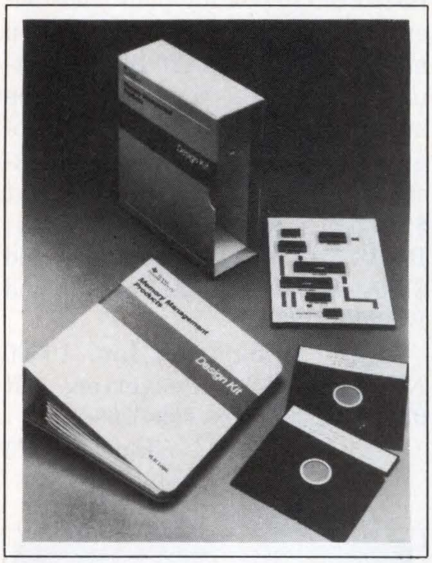
- *Contains DTMF communications circuit*
- *Features 2-line, 32-character display*

The MultiPortable pocket-size data terminal uses an 8-bit μP that features communication circuits for DTMF (dual-tone multifrequency) and tone transmission. The μP also provides audio-tone monitoring and pulse-width timing for tone detection. The terminal has 64k bytes of internal memory, an 8-bit parallel port, an RS-232C port, and three I/O and control ports. The package includes a 66-character qwerty keyboard and a 2-line, 32-character liquid-crystal display. An optional 1200-bps modem transfers data via two RJ-11 telephone-jack interfaces. When functioning as a voice terminal and "smart" telephone, the unit stores names, addresses, and numbers in a directory that enables it to perform automatic dialing. One edge of the terminal contains a Memocard access port. This port can transfer and accept data from a credit-card-size memory card containing an EEPROM. The unit measures 6½×3¾×1¼ in. and weighs about 12 oz. Terminal with optional modem, $650; 2k-byte Memocard, $79; 8k-byte Memocard, $139.

Multimil Inc, 670 International Parkway, Suite 190, Richardson, TX 75081. Phone (214) 644-7724. TLX 286258.

Circle No 418

CAE & SOFTWARE DEVELOPMENT TOOLS



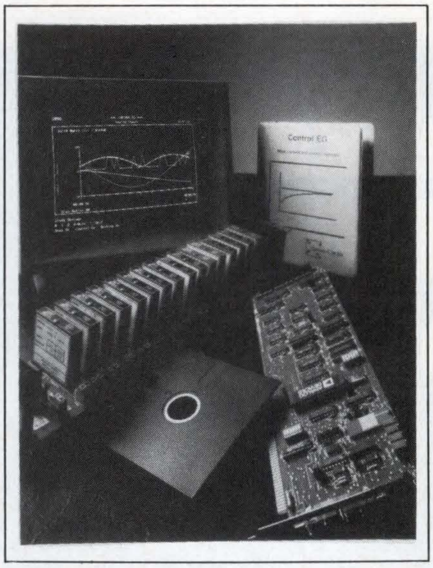
DESIGN KIT

- *Lets you evaluate memory-management performance*
- *Includes graphics-symbol libraries*

Memory-management design kit SN74MMDK01 consists of technical data, application information, libraries of schematic-capture graphics symbols, and samples of the vendor's memory-management ICs. The documentation includes data sheets for each of the sample devices and related products, and the vendor's *Memory-Management Applications Handbook*. You can use the symbol libraries, which are from Logic Automation and FutureNet, on the FutureNet and Mentor Graphics CAE systems; Logic Automation also supplies behavioral-simulation models for the memory-management devices in the kit. These devices include dynamic-RAM controllers, cache-address comparators, error-detection and -correction circuits, and memory drivers. You can use the kit either to shorten the design time of a memory system or to evaluate performance improvements gained by using the vendor's devices. $149.

Texas Instruments Inc, Semiconductor Group (SC-780), Box 809066, Dallas, TX 75380. Phone (800) 232-3200, ext 700.

Circle No 373



CONTROL SOFTWARE

- *Monitors as many as 128 analog inputs*
- *Drives as many as 32 analog outputs*

Contro EG is a menu-driven, data-acquisition, process-control software package that can monitor as many as 128 analog inputs and control as many as 32 analog outputs. It can also display bar graphs, annunciators, and history stripcharts of all channels. The program runs on an IBM PC or a compatible computer and works with the vendor's RTI-800 Series of analog and digital plug-in boards. Tables built into the software automatically provide thermocouple linearization and input scaling. You can save the setup conditions and recall them later as needed; once you have specified the configuration of I/O boards and signal-conditioning modules, the program makes the I/O interface transparent to you. You can automate all aspects of a process, and you can change system parameters (such as alarm limits) while collecting data. The typical scanning rate on an IBM PC/AT is 64 channels/sec. $500.

Analog Devices Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 461-3359. TWX (710) 394-6577.

Circle No 374

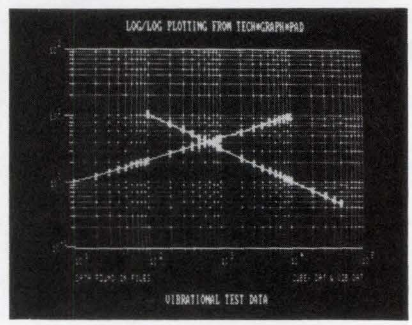
IC-SIMULATION MODEL

- *Lets you simulate a board using BIT components*
- *Works with popular CAE programs*

You can order SmartModel logic-simulation models for four components manufactured by BIT (Bipolar Integrated Technology Inc): the B3018A/B2018 16×16-bit fixed-point multiplier; the B3011/B2011 multiplier-accumulator; the B3210/B2210 5-port register file; and the B3110/B2110 floating-point multiplier. The vendor will soon offer a model for BIT's B3120/B2120 floating-point ALU. You can use the models with most popular CAE programs and with a variety of workstations. Workstation licenses cost $950 each for the B3011/B2011, B3018/B2018, and B3210/B2210, and $1800 each for the B3110/B2110 and B3120/B2120.

Logic Automation Inc, 19500 NW Gibbs Dr, Beaverton, OR 97006. Phone (503) 690-6900.

Circle No 375



DATA PLOTTER

- *Lets you process and plot data from a variety of sources*
- *Works with files and data-acquisition software*

Tech*Graph*Pad is a tool for plotting data that you've collected from laboratory experiments, prototype tests, or engineering analyses. It accepts data directly from data-acquisition software, from files generated by spreadsheets, from text editors (ASCII format only), or from its own built-in editor. The program can generate linear, log, and R-Theta plots; perform polynomial curve-fitting; and do spline, Bezier, and Savitsky-Golay data smoothing. You can direct the output to the screen for display by a Hercules or compatible monochrome-graphics adapter, or by an IBM CGA, EGA, or compatible color-graphics adapter. You

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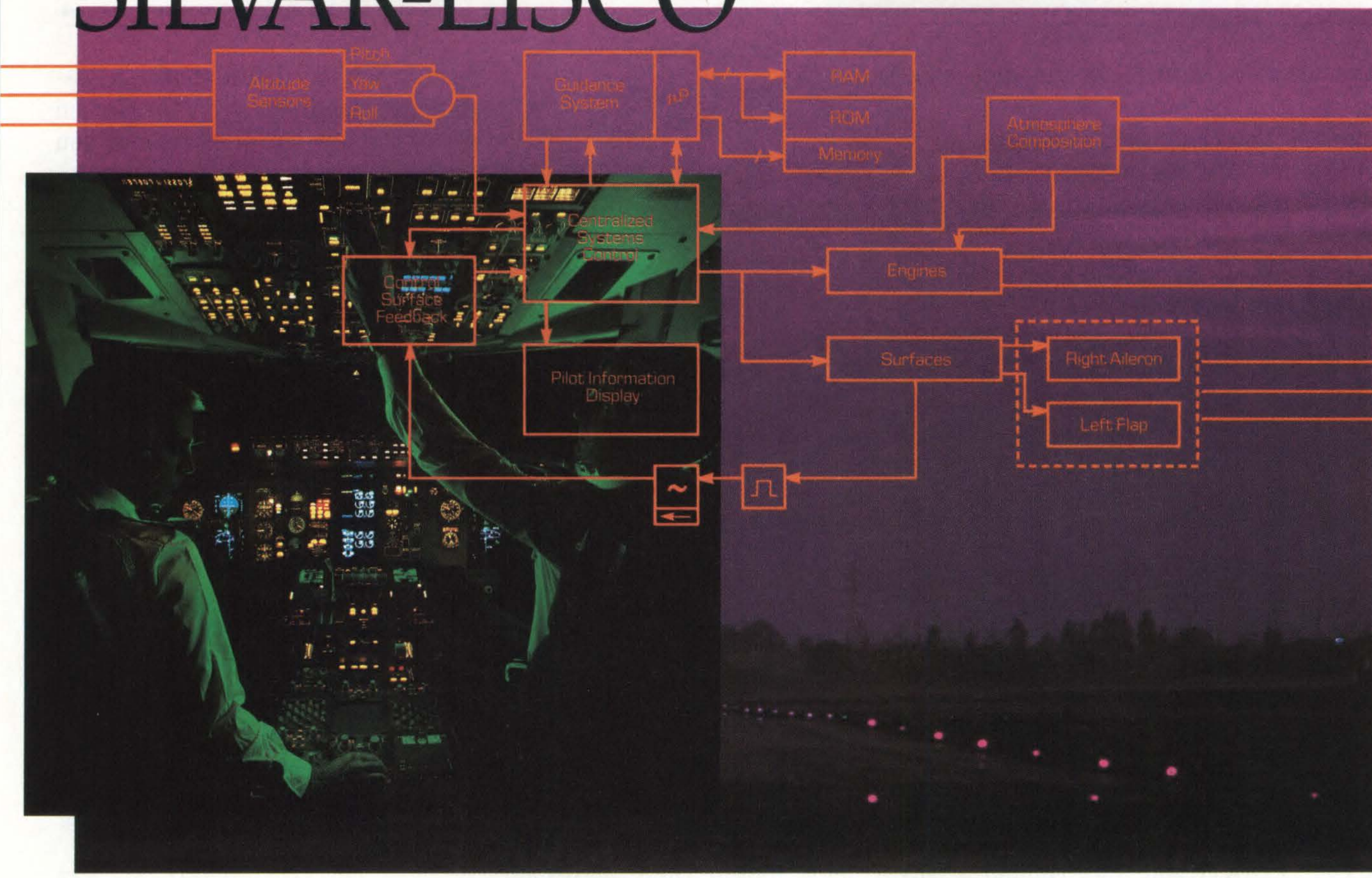

For complex designs, HELIX™ is the "what if" simulator!

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CAE Software products for electronic design.

CIRCLE NO 230

have complete control over the scaling and the placement of axes, labels, and notations. For hard copy, you can use a wide variety of plotters and dot-matrix printers. To run the program, you'll need an IBM PC, PC/XT, PC/AT, or a compatible computer that's equipped with at least 512k bytes of RAM and runs MS-DOS version 2.0 or later. $275.

Binary Engineering, 100 Fifth Ave, Waltham, MA 02154. Phone (617) 890-1812.

Circle No 376

WAVE-SOLDER CONTROL

- *Allows off-line programming of wave-soldering machines*
- *Lets you write parameters to EPROM*

The ElectroSave software package—which runs on the IBM PC, PC/XT, PC/AT, and fully compatible computers—allows you to perform off-line programming of the vendor's µP-controlled Econopak II wave-soldering system. By following the program's menu selections and prompts, you can create a file containing a complete set of operating parameters for the production run of a given board type; the parameters include preheat temperature, flux density, solder temperature, wave height, and conveyor speed. You can later recall the parameters for display on the screen or on the system printer, and you can change any or all parameters. When you are satisfied with the values, you can download the file, via an RS-232C link, to the Econopak II machine for execution of a soldering run. You can also upload parameters stored in the machine for archival storage in an EPROM. To run the program, you'll need an IBM PC or compatible computer that's equipped with the IBM Monochrome Display and Printer Adapter (or equivalent) and an Epson-compatible dot-matrix printer. The package comes with a ribbon cable to connect the Econopak machine to the PC's serial port; it also comes with EPROM chips, and a program disk with a backup copy. $1195.

Electrovert USA Corp, 4330 Beltway Pl, Arlington, TX 76018. Phone (817) 468-5171.

Circle No 377

SOFTWARE TOOL

- *Program development for µCs without in-circuit emulation*
- *Runs on an IBM PC*

This version of the chipForth software-development environment allows you to write and debug software for Intel's 8051/8031 family of microcontrollers without using an in-circuit emulator. Instead, chipForth provides interactive program development, using only the on-chip RAM of the µC and a ROM emulator. You can write programs that use only the on-chip RAM and ROM of the µC or programs that use the 8051's 64k bytes of external data and program space. You can also implement systems with overlapping data and program space. The development environment uses the Forth programming language combined with an editor, an assembler, and a compiler. This development software runs on an IBM PC, PC/XT, PC/AT, or a compatible computer linked to the target system via a serial port. The Forth multitasking kernel that is supplied uses as few as 40 bytes/task. It imposes no overhead on the µC's interrupt handling and does not affect its bit-handling capabilities. £1800.

Computer Solutions Ltd, Canada Rd, Byfleet, Surrey KT14 7HQ, UK. Phone (09323) 52744. TLX 946240 (Request ref 19012265).

Circle No 378

TERMINAL EMULATOR

- *Allows IBM PCs to emulate 3270 workstations*
- *Includes a communications card for the PC*

The PC70 hardware/software package allows one or two IBM PC, PC/XT, PC/AT, or compatible computers to operate as IBM-3270 BSC (binary synchronous communications) workstations. The package includes a full-length add-in card that you can configure as the PC's COM1 or COM2 port, and terminal-control software that performs the 3270 emulation. You can link the card both to the host and to another PC, enabling each to operate as a 3270 workstation. Both workstations can use their own printers. If you don't use the second workstation facility, you can employ the second port on the card to drive a line printer directly. You can link the package to the host system via a null modem or via a modem/line driver connected to a leased line. £850.

Sipher Designs (Electronics) Ltd, Unit 14, St George's Industrial Estate, White Lion Rd, Amersham, Bucks HP7 9JQ, UK. Phone (02404) 5335. TLX 83293.

Circle No 379

CAE & SOFTWARE

MICROWAVE SIMULATOR

- *Simulates nonlinear microwave circuits*
- *Harmonic-balance techniques for nonlinear aspects*

Microwave Harmonica is a general-purpose software package for the design and simulation of nonlinear microwave circuits that operate in a time-periodic or quasiperiodic steady-state mode. The program can simulate amplifiers, passive and active frequency multipliers, mixers, and voltage-controlled oscillators; it can also analyze 2-tone intermodulation distortion in microwave circuits. For the linear portions of the circuit, the program uses a frequency-domain description that allows you to model passive microwave components and to introduce experimental information as needed. A set of generalized parametric equations can describe nonlinear devices in the time domain; for simulation purposes, the state variables are described by means of their spectral components (harmonics), which represent the true unknowns. The voltage and current harmonics are then described by 1- or 2-dimensional FFTs. $25,000.

Compact Software Inc, 483 McLean Blvd, Paterson, NJ 07504. Phone (201) 881-1200.

Circle No 380

ASIC EXPERT SYSTEM

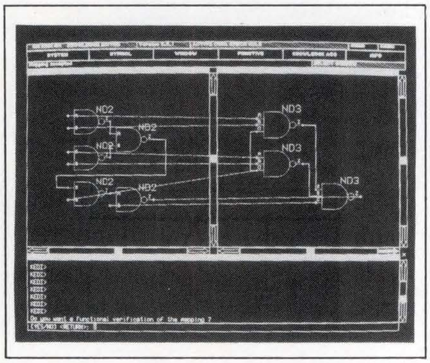
- *Lets you capture your ASIC design expertise*
- *Builds knowledge base for optimizing ASIC designs*

Knowledge Consultant is a software tool that lets you graphically capture your design expertise in a knowledge base. The vendor's Logic Consultant expert system can use the knowledge base to optimize your ASIC logic designs by reducing propagation delays and decreasing the gate count. Using the built-in graphics editor, you first draw an antecedent circuit using foundry-

specific component-library symbols; then you draw the consequent circuit, a less obvious but more efficient circuit that provides the same functionality. You also define the port, mapping between the two circuits. The knowledge compiler then verifies that the two circuits are logically identical and determines the speed and area factors for each of the circuits. If the knowledge you are adding is already in the knowledge base, the program so informs you; otherwise it compiles the knowledge into the knowledge base. The system runs on a Mentor Graphics (Beaverton, OR) workstation. $49,500.

Trimeter Technologies Corp, 200 Hightower Blvd, Suite 100, Pittsburgh, PA 15205. Phone (412) 787-8630. TWX 510-601-3773.

Circle No 381



IC DESIGN TOOL

- *Provides a common user interface for design tools*
- *Allows foundry-independent IC design*

The Spirit IC design environment provides you with a stable user interface through which you can access a variety of proprietary or commercial IC design tools. The user interface remains the same even if you add to or change the set of design tools, so you don't need to learn a new user interface for each tool. In addition to the user interface, the tool set has a design manager, a design database, and a foundry interface that allow you to meet the requirements of different silicon foundries. System-management software allows the system administrator to create and change information about users, projects, foundries, libraries, and process parameters. Spirit targets fully custom IC design teams and is available for use on the Apollo Domain 3000 workstation, HP-9000 Series 300 and 500 computers, and the PCS Cadmus computer. Approximately gld 175,000 (including a tool set).

Integrated Circuit Design BV, Box 3132, 7500 DC Enschede, The Netherlands. Phone (053) 306455. TLX 72280.

Circle No 382

 CIRCLE NO 80

WAIT

THE WAIT FOR ABSOLUTE FLEXIBILITY IN HIGH POWER IS OVER

WAIT UNTIL YOU READ THIS You can have up to 5 outputs with unlimited flexibility of output voltage and current combinations with acdc electronics' NEW 1600W power supply. That's UNLIMITED combinations! Check the chart below.

DON'T WAIT . . . SEE— THE SMALLEST 1600W PACKAGE acdc electronics has packaged 1600 W into a 5″ × 8″ × 13″ profile. That makes acdc's JFM Series the SMALLEST 1600W multi output switch mode power supply available. Anywhere!

THE WAIT FOR INDEPENDENT AUXILIARY OUTPUTS IS OVER Each JFM auxiliary output is an independent, switch mode power supply which eliminates all cross regulation problems. Additional standard features—never before offered on a high power multi—include: remote sense, margining and inhibit . . . on each auxiliary output.

And, to troubleshoot your system, independent LED's indicate output out-of-tolerance and identify the faulty output.

WAIT NOT Don't wait for the power supply you need. Any output voltage combination listed in the model selection chart will be delivered in two weeks!

WAIT UNTIL YOU TEST THESE SPECIFICATIONS

- Internal EMI Filter meets FCC & VDE Class A
- All outputs are floating
- No minimum load required on any output
- Single-wire paralleling (main output)
- Current monitor
- 30 Ms holdover storage

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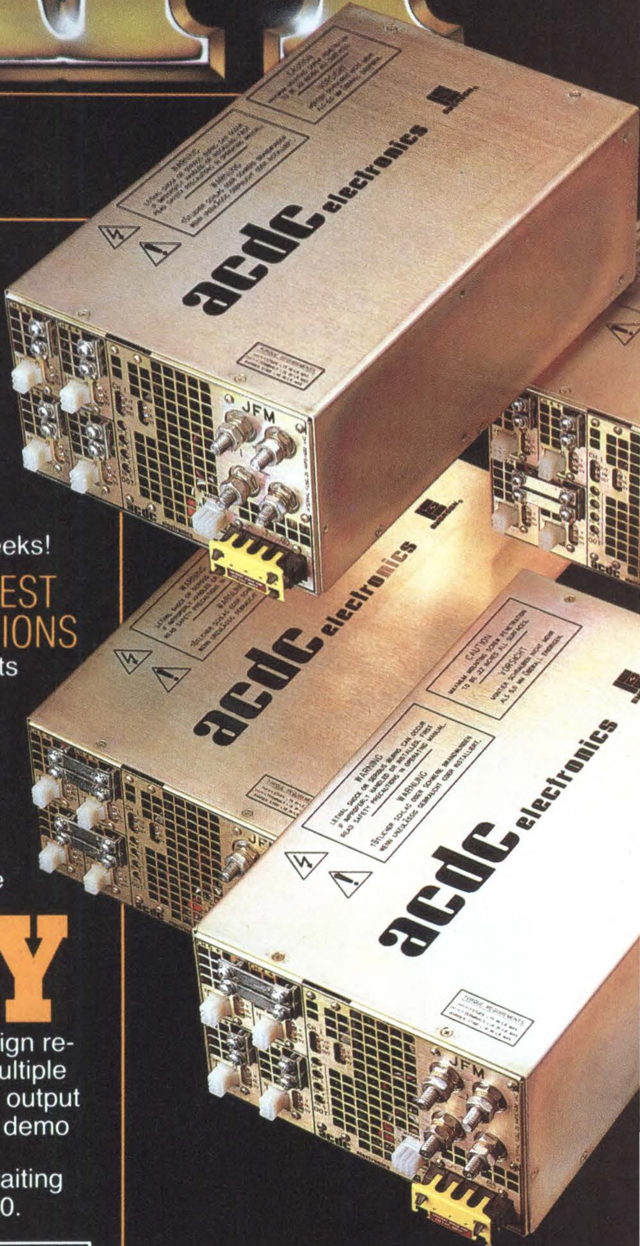

1600W MULTI

MAIN OUT	CH2	CH3	CH4	CH5
5V/200A	TABLE A or B	TABLE A or B		
5V/200A	TABLE A or B	TABLE B	TABLE A or B	
5V/200A	TABLE B	TABLE B	TABLE B	TABLE B

TABLE A AUX's	TABLE B AUX's
5V/60A	5V/30A
12V/30A	12V/15A
15V/24A	15V/12A
24V/15A	24V/7.5A

1500w 800w 500w 300w 175w 70w 15w
1600w 1000w 750w 400w 220w 135w 40w

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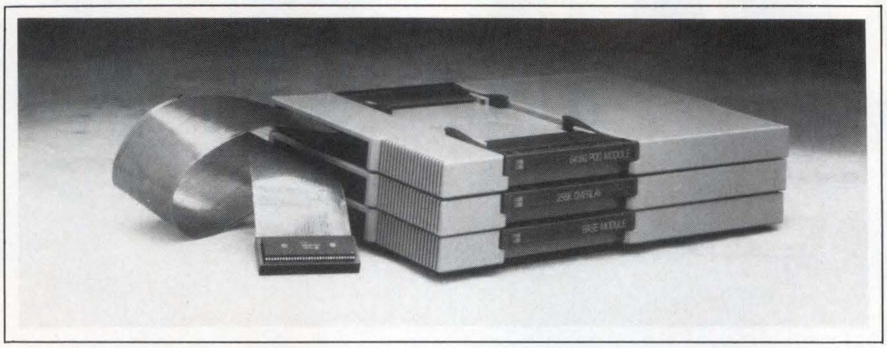


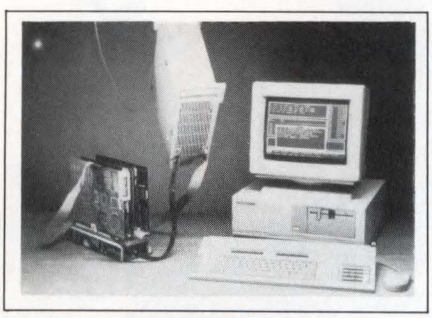
Z80/64180 EMULATOR

- *Emulates Z80H at full speed with no wait states*
- *Provides 8k×48-bit words of high-speed trace memory*

The EL 800 in-circuit emulator performs zero-wait-state emulation of the Z80H μP at 8 MHz and the HD64180 at 6 MHz without preempting any interrupts. To minimize propagation delays, the device uses a hybrid circuit rather than the more common passive connection. The emulator plugs into the target μP socket and drives the 16-in. cable back to the emulator. The emulator itself is packaged as a group of 8.5×11×0.85-in. modules that stack on top of one another and snap together to make electrical as well as mechanical connections. A single power supply energizes all of the units. You need to purchase only one module; you add features—for example, 64k to 256k bytes of overlay memory with optional battery backup—by adding modules. Your personal computer (running MS-DOS 3.0 or higher and having 640k bytes of RAM) acts as host; you connect the emulator to either the COM1 or COM2 port. You can display the 8k×48-bit words of trace memory in several ways: for example, you can restrict the display of write instructions to those that write to data space. $4850.

Applied Microsystems Corp, Box 97002, Redmond, WA 98073. Phone (206) 882-2000. TLX 185196.

Circle No 420



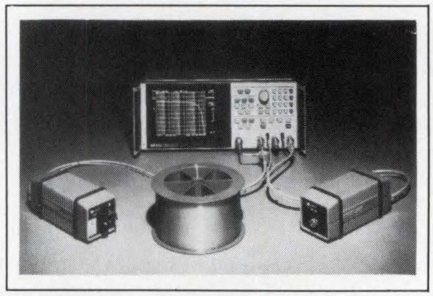
IN-CIRCUIT EMULATOR

- *Emulates Z80, 68000, 80186, and 80188 μPs*
- *Optional state and timing analyzer*

Hosted by an ASCII terminal or a computer, the HP 64700 Series emulator/analyzer performs transparent, real-time emulation and analysis of systems based on the Z80, 68000, 80186, and 80188 μPs. Optional versions can also perform 16-channel logic-state analysis at 25 MHz and timing analysis at 100 MHz. You can trigger the logic analyzer without breaking the emulated processor's program execution. All units include an emulation analyzer with which you can trace the code flow. Using the analyzer, you can prestore and time-tag instructions and qualify the trace specifications with sequences of as many as eight system states. The hardware includes a code-coverage analyzer; it provides a history of the memory addresses that the μP reads from or writes to during program execution. 8-bit μP without logic analyzer, $8900 to $12,500; 16-bit μP, $11,300 to $14,650.

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 421



PHOTONIC ANALYZER

- *Includes light source and receiver*
- *Handles modulation frequencies as high as 3 GHz*

The HP 8702A photonic analyzer system is a design and analysis tool for high-bandwidth (that is, high-bit-rate) optoelectronic components. Such components include transmitters, receivers, couplers, and fibers used in long-haul fiber-optic communications systems. The analyzer extends microwave-network analysis techniques (and, optionally, time-domain analysis techniques) to equipment that modulates and transmits light waves. The system, which can include both a lightwave source and a lightwave receiver, measures modulation bandwidth, responsivity, modulation and detection sensitivity, dynamic range, linearity, attenuation, and delay. A synthesized 300-kHz to 3-GHz RF source provides the modulating signals, and a calibrated 3-channel receiver measures the magnitude and phase of demodulated signals. The time-domain option enables the ana-

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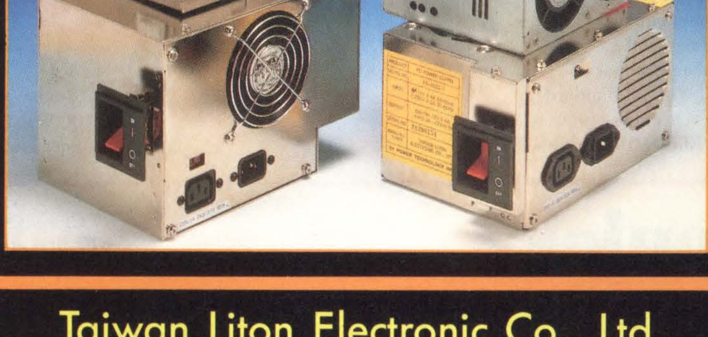

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CIRCLE NO 227

lyzer to make pulse-dispersion measurements. Analyzer, $28,000; time-domain option, $4800; single-mode or multimode light source, $12,700; lightwave receiver, $5000. Delivery, eight weeks ARO.

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 422

Z280 EMULATOR

- *Supports 16M-byte address space*
- *Handles the μP's 8- and 16-bit buses*

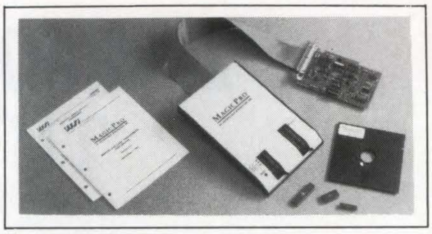
The Z280 IceAlyzer is an in-circuit emulator for Zilog's Z280 μP. With the addition of an RS-232C-interfaced ASCII terminal, the system supports the Z280's 10-MHz maximum clock rate, 16M-byte address space, memory manager, extended I/O addressing, and both the 8- and 16-bit buses. You can set 32,000 hardware breakpoints so that they take effect individually or in regions and on read, write, or fetch cycles. To debug ROM-based systems, you can overlay 256k bytes of RAM anywhere in the Z280's address space. The unit has built-in tests for common target-system hardware faults. It also performs software-performance analysis. $7995.

Softaid Inc, 8930 Rte 108, Columbia, MD 21045. Phone (800) 433-8812; in MD, (301) 964-8455.

Circle No 423

PROGRAMMER

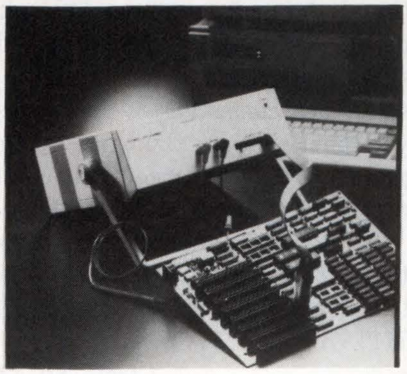
- *Programs small lots during development*
- *Supports vendor's programmable-device line*



The MagicPro memory and logic programmer runs on a PC bus-based personal computer and is suited to programming small quantities of the vendor's devices. It provides 20 lines that address 1M bytes and has 16-bit-wide I/O. A cable connects the PC Bus short card to a pair of ZIF (zero insertion force) sockets that, without adapters, accommodate DIP devices having 24, 28, 32, and 40 pins in rows on 0.3- and 0.6-in. centers. Socket adapters enable the programmer to handle LCC and PGA (pin-grid-array) packages. The product's support software comes on a 5¼-in. disk. $995.

Waferscale Integration Inc, 47280 Kato Rd, Fremont, CA 94538. Phone (415) 656-5400. TLX 289255.

Circle No 424



PC-BOARD TESTER

- *Locates defective components*
- *Learns and stores signatures of device and board pins*

The portable Board Wizard locates defective components on pc boards. It can learn and store characteristic signatures at each pin of known-good boards and devices such as ASICs and PLDs. The tester compares the stored signatures against signatures measured on the board under test. The unit can also conduct comparisons by referring to a library of signatures for 74-series TTL devices. $3495.

Suan Technologies (USA) Inc, 18437 Saticoy St, Suite 8, Reseda, CA 91335. Phone (818) 996-1386.

Circle No 425

COUNTERS

- *Count at 200- and 520-MHz rates*
- *Display uses eight 0.56-in.-high LEDs*

The 712 is a 200-MHz counter; the 713 is virtually identical, but it handles frequencies to 520 MHz. The 712 has two channels, the 713 three. Besides indicating a signal's frequency, both units totalize from 10 Hz to 10 MHz, and measure period and frequency ratios from 10 Hz to 2.5 MHz and time intervals from 0.5 μsec to 0.2 sec. Their time bases spec ±5 ppm/yr aging and ±10 ppm temperature stability from 0 to 50°C. The instruments include 1-MHz lowpass filters with selectable attenuation; in the self-check mode, each instrument displays the frequency of its 10-MHz internal timebase. The counters' 8-digit displays use 0.56-in.-high LEDs and provide overflow, gate, microsecond, and kilohertz indicators. Model 712, $525; Model 713, $675.

Simpson Electric Co, 853 Dundee Ave, Elgin, IL 60120. Phone (312) 697-2260. TLX 722416.

Circle No 426

VHSIC VERIFIER

- *Operates at 100 MHz*
- *Accommodates 448 channels*

The Logic Master XL 100 prototype verification system supports 100-MHz clock and data rates. The vendor claims that this speed exceeds the test requirements of VHSIC-Phase-II parts and that the system's 100-psec edge placement, 125-psec frequency resolution, and 448-channel capability are appropriate for at-speed verification of ECL and GaAs ASICs. The system comes with an automatic tool for speeding fixture fabrication, reducing wiring errors, and maintaining a 50Ω device environment. The system, which can contain 16 to 224 bidirectional channels or 32 to 448 split pattern-generation and data-acquisition channels, provides 12 timing sets, each consisting of two edges; you can assign any timing set to any pin. With 128 bidirectional channels, $250,000.

Integrated Measurement Systems, 9525 SW Gemini Dr, Beaverton, OR 97005. Phone (503) 626-7117.

Circle No 427

AUTOMATED BRIDGE

- *Measures series and parallel capacitance and loss*
- *Shows loss as Q, resistance, conductance, or dissipation*

The 7600 μP-controlled automated bridge makes 3-terminal measurements of series and parallel capacitance and loss. The bridge operates at 1 MHz, and it lets you add programmable external bias voltages of ±100V or ±200V. It makes as many as 70 readings/sec and can display losses as resistance, conductance, dissipation, or Q. The bridge can display the actual measured capacitance or it can display the difference between the measured value and a user-entered nominal value either as a percentage of the nominal or as a difference. The bridge can automatically select full-scale capacitance ranges of 1.9900 pF through 1990.0 pF, or you can choose the range manually. When making remote measurements, the bridge automatically compensates for capacitance of cables of selectable length. The instrument features a real-time clock for time and date stamping of hard-copy records, and three interfaces: Centronics parallel, RS-232C serial, and IEEE-488 high-speed parallel. $12,500. Delivery, 16 weeks ARO.

Boonton Electronics Corp, 791 Rte 10, Randolph, NJ 07869. Phone (201) 584-1077.

Circle No 428

LINEAR IC TESTER

- *Performs go/no-go tests and measures parameters*
- *Tests more than 150 op amps and voltage comparators*

The Model 750 μP-based benchtop linear IC tester tests more than 150 types of single, dual, triple, and quad op amps and voltage comparators. It performs both go/no-go and parametric tests on such devices. When performing go/no-go tests on an op amp, the tester first verifies that the device is closed-loop stable. The tester then ascertains whether the device's output can swing to at least 75% of the supply voltage. Next, it measures the device's gain-bandwidth product and compares this measurement against a predetermined limit. When operating in the parametric-measurement mode, the tester can perform 10 types of tests and provide quantitative data; it can run the tests in sequence and can hold the data on its display until you issue a command for it to proceed to the next test. $2495.

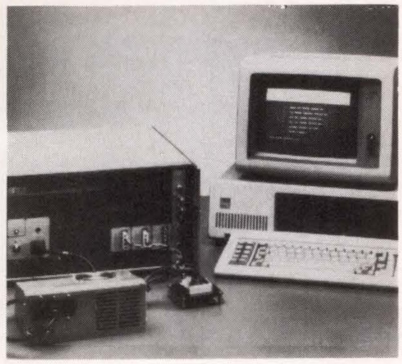
Information Scan Technology Inc, 487 Gianni St, Santa Clara, CA 95054. Phone (408) 988-1908.

Circle No 429

SUPPLY TESTER

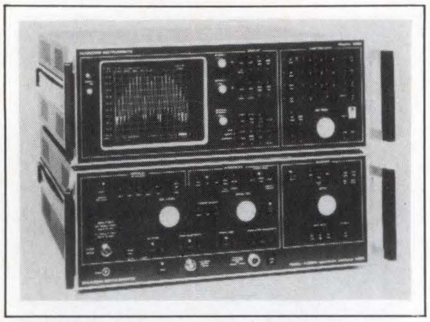
- *Hosted by MS-DOS-based PC*
- *Has Basic-language software that supports 14 tests*

The Model 701 power-supply tester can reside on a desktop. It utilizes an MS-DOS-based IBM PC-compatible computer as a controller. The software supports 14 tests, which include current-limit and voltage adjustments, a p-p noise test, combined line- and load-regulation measurements, and, for multiple-output supplies, cross-regulation measurements. The programming language is Microsoft Basic. Including computer, $11,950.



Condor Inc, 2311 Statham Parkway, Oxnard, CA 93033. Phone (805) 486-4565.

Circle No 430



SPECTRUM ANALYZER

- *Covers 100 Hz to 4.2 GHz*
- *Can resolve 3-Hz bandwidth*

The 2383 spectrum analyzer covers the frequency range from 100 Hz to 4.2 GHz and can display a full-bandwidth sweep on a single screen. Its minimum resolution bandwidth is 3 Hz and its high-level accuracy is ±1.5 dB with any control settings and at any specified operating temperature, even at 4.2 GHz. Its built-in tracking generator eliminates frequency-drift-induced impairment of swept-frequency synchronous measurements. The instrument's intermodulation is better than −90 dBc, and its residual responses are below −110 dBm. An optional active probe permits you to take high-level measurements with minimal loading at frequencies as high as 1.25 GHz. The IEEE-488 interface permits a high-speed dump of the screen display to a host controller. $41,950. Delivery, 60 days ARO.

Marconi Instruments, 3 Pearl Ct, Allendale, NJ 07401. Phone (201) 934-9050.

Circle No 431

PLD PROGRAMMER

- *Operates with an MS-DOS-computer host*
- *Programs 20- and 24-pin devices*

The Avpal PLD programmer accepts JEDEC files created by CUPL and other PLD-programming languages. It permits you to load files directly from disk into a buffer, edit the files, check PLDs to make sure they are blank, program PLDs from the buffer, read a chip into the buffer, and save the buffer contents to disk. The programmer also lets you read the status of a PLD's security fuse; blow the fuse to prevent unauthorized copying of the device; and display, print, or modify the device's fuse map. The unit consists of a card, which plugs into IBM PCs and compatible machines, and a remote head, which contains a zero-insertion-force socket and connects to the card via a cable. The MS-DOS-based software is menu driven. The programmer handles 20- and 24-pin PLDs made by Monolithic Memories, National Semiconductor, and Texas Instruments. $395.

Avocet Systems Inc, Box 490, Rockport, ME 04856. Phone (800) 448-8500; in ME, (207) 236-9055. TLX 467210.

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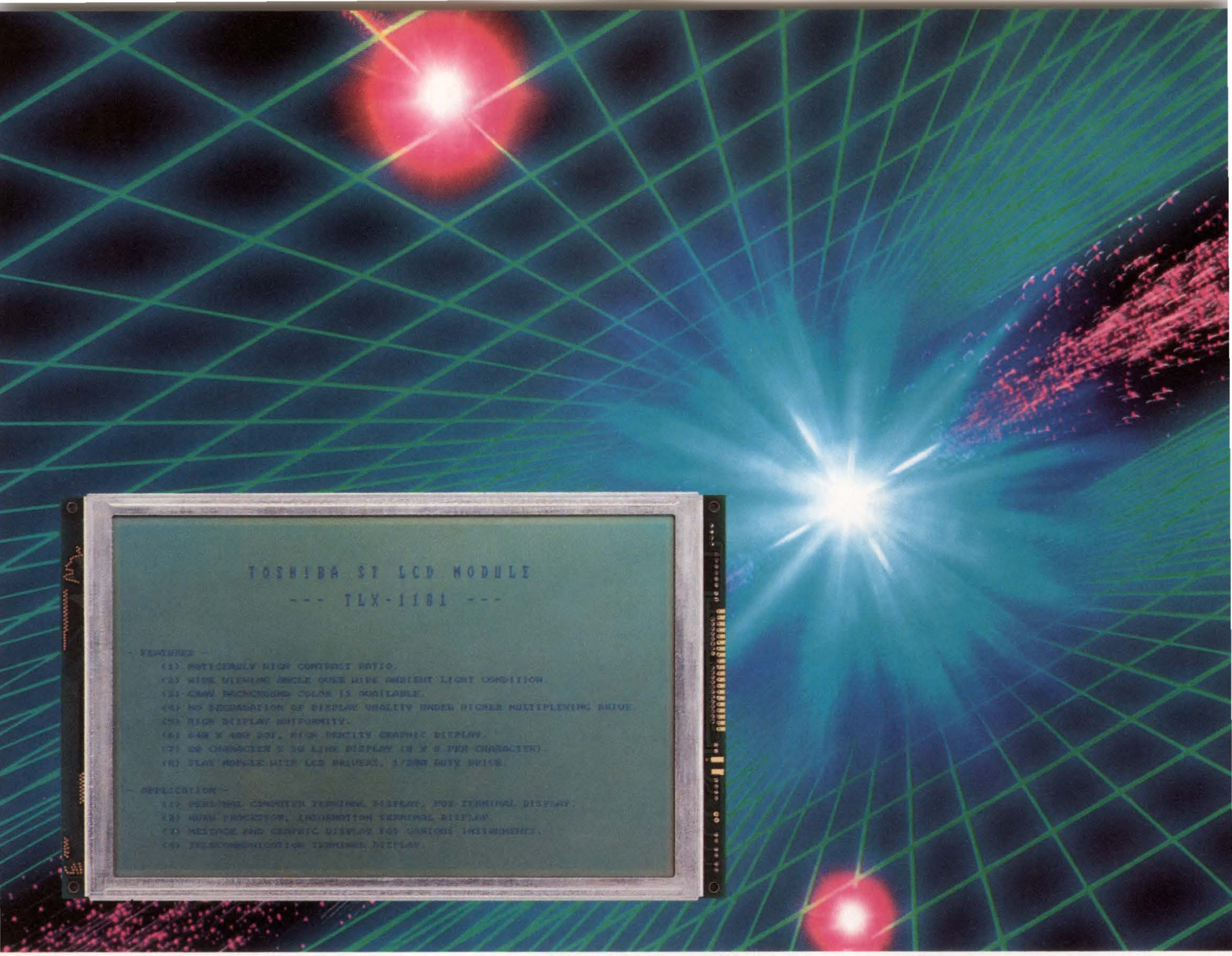

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TLX-932	640 × 200	1/200	0.375 × 0.375	293 × 97.6 × 14	No	T7779
TLX-561	640 × 200	1/200	0.35 × 0.49	275 × 126 × 14	Yes	T7779
TLX-711A*	240 × 64	1/64	0.53 × 0.53	180 × 65 × 12	Yes	T6963C**
TLX-341AK*	128 × 128	1/64	0.45 × 0.45	93.2 × 86.6 × 12	No	T6963C

*Under development, **Built-in controller

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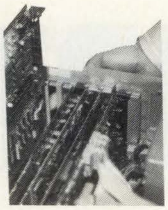

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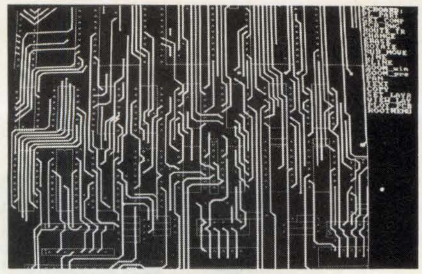

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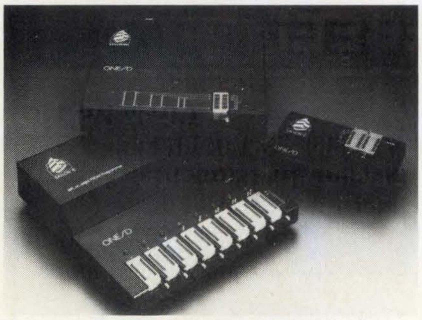

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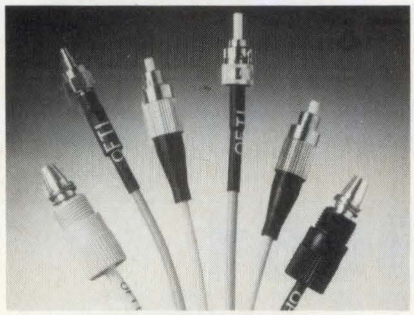

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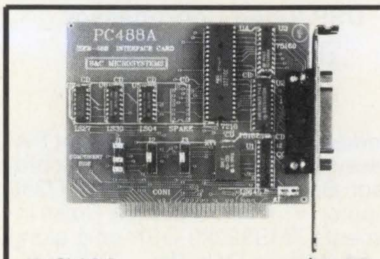

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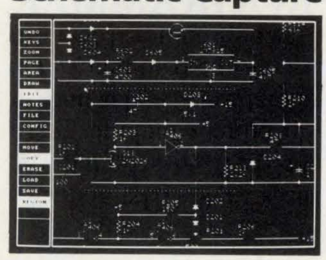

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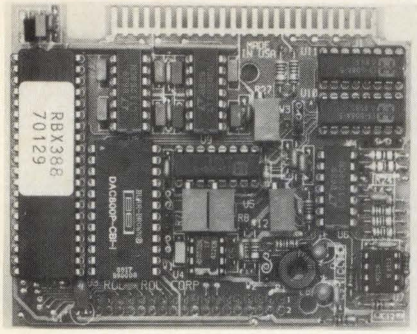

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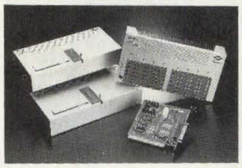

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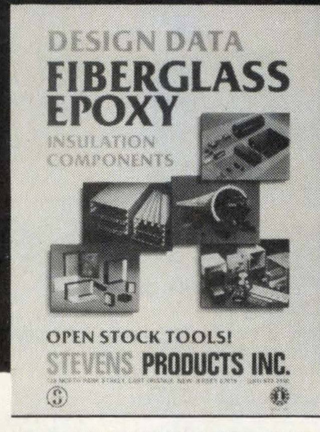

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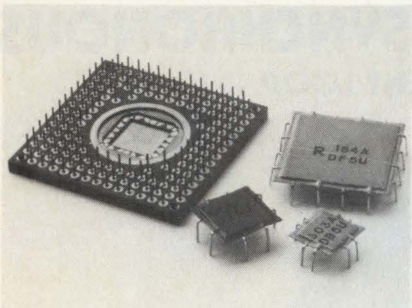

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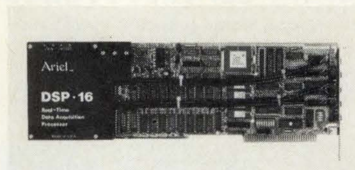

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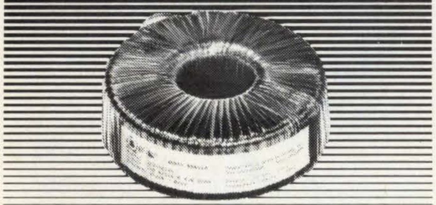

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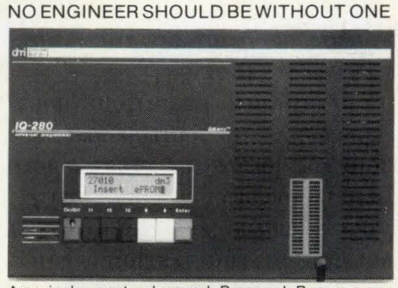

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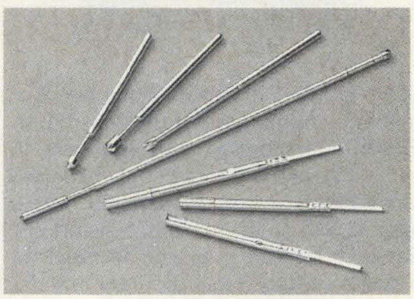

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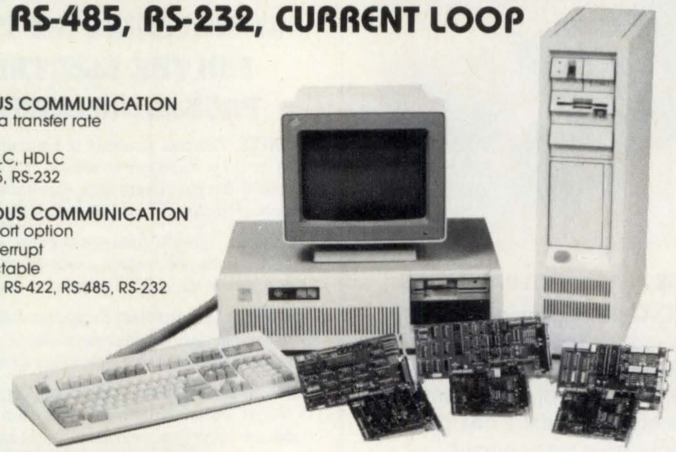

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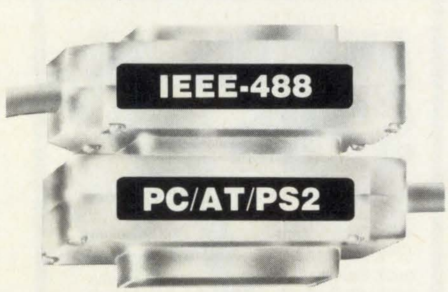

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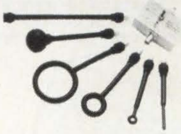

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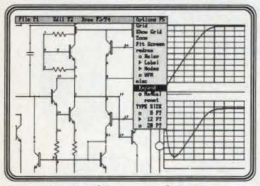

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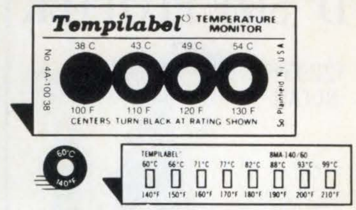

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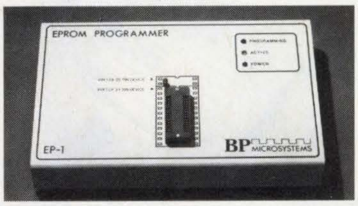

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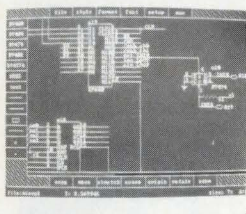

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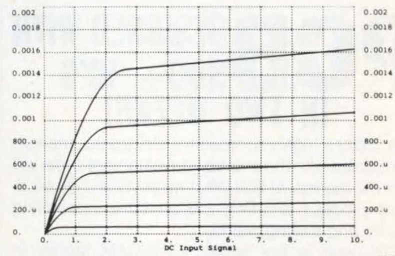

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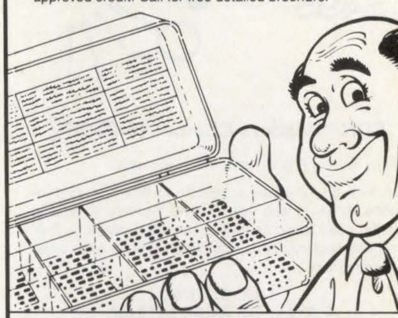

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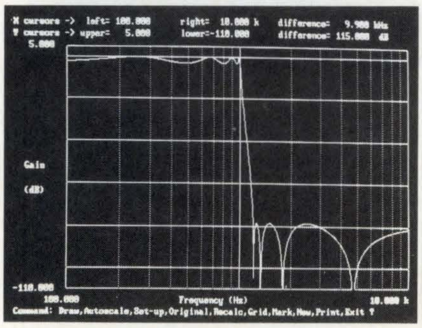

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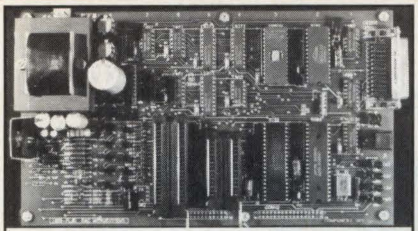

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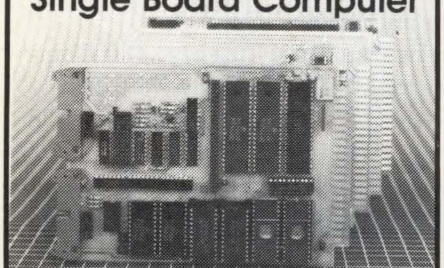

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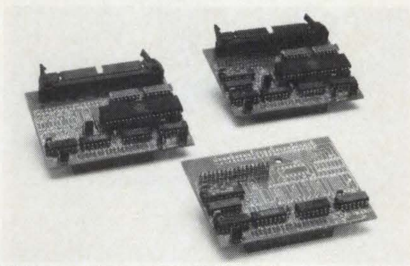

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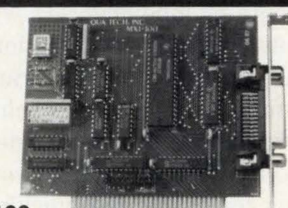

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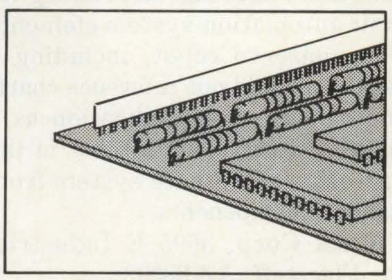

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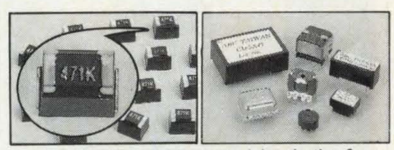

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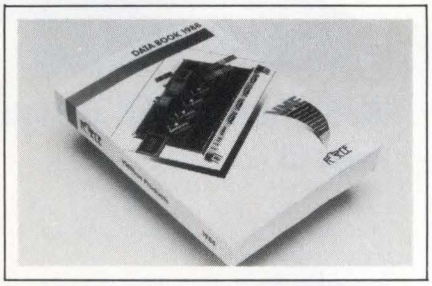

Publications feature VME Bus and VME/Plus

The 560-pg *VME Data Book 1988* is the vendor's second edition of its data book on VME Bus products. Published simultaneously, the technical brochure on VME/Plus examines several growth-oriented architectural features. The data book contains nine chapters with numerous photos and illustrations. A product-selection matrix arranged in columns introduces each chapter. Further, a product guide helps you to locate the products you are looking for easily and quickly. The brochure features the most recent VME/Plus 32-bit devices. It also contains previews of products in the design stage, which are scheduled for release this year.

Force Computers Inc, 3165 Winchester Blvd, Campbell, CA 95008.

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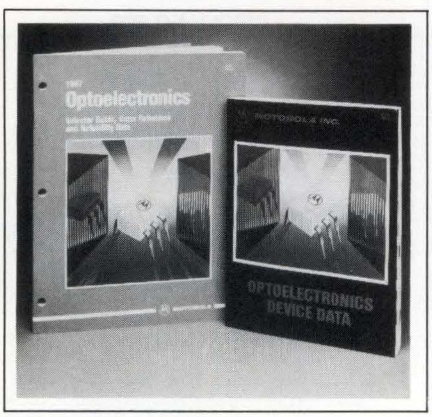

Optoelectronics guide and data book

The two publications, Optoelectronics Selector Guide (SG87/D) and Optoelectronics Data Book (DL118/D), are divided into product sections: emitters/detectors, isolators, slotted switches, and fiber-optic components. The data book contains 65 new products and their applications and includes a new section on optoelectronic chips or die. Both books contain an industry cross reference and a reliability section.

Motorola Inc, Technical Information Center, Box 52073, Phoenix, AZ 85072.

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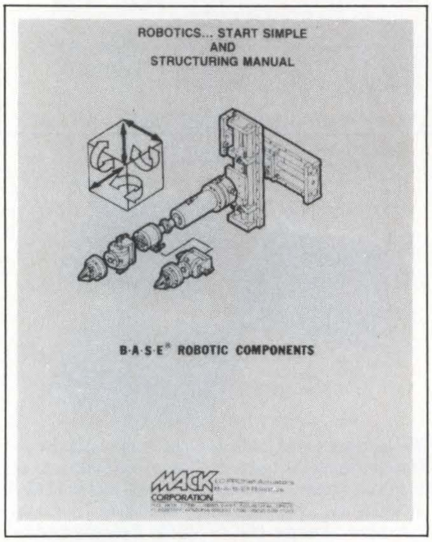


Document describes robotics

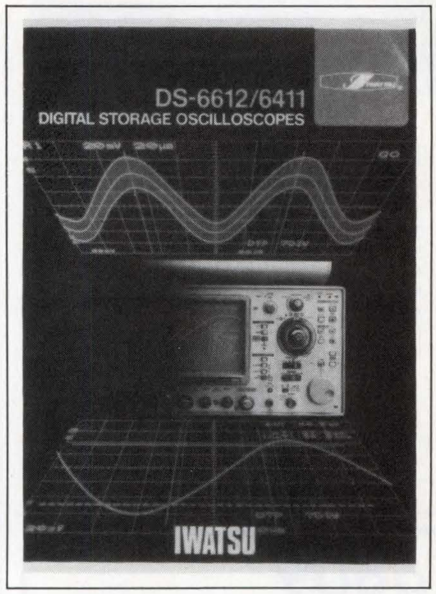
The 110-pg booklet *Robotics...Start Simple, and Structuring Manual* comprises three main sections: the fundamentals of robotics; applications and ideas; and structuring for basic automation-system elements of a nonservo robot, including a back-cover fold-out reference chart. You can use the publication as a guide to structuring a robot in the Cartesian coordinate system from standard components.

Mack Corp, 3695 E Industrial Dr, Flagstaff, AZ 86002.

Circle No 437

Digital storage oscilloscopes presented

This 6-pg, 4-color fold-out provides information about two of the vendor's digital storage oscilloscopes, the DS-6612 and DS-6411. The brochure describes each instruments' control panel in detail and lists features and specifications. Ample illustrations are included.



Iwatsu Instruments, 430 Commerce Blvd, Carlstadt, NJ 07072.

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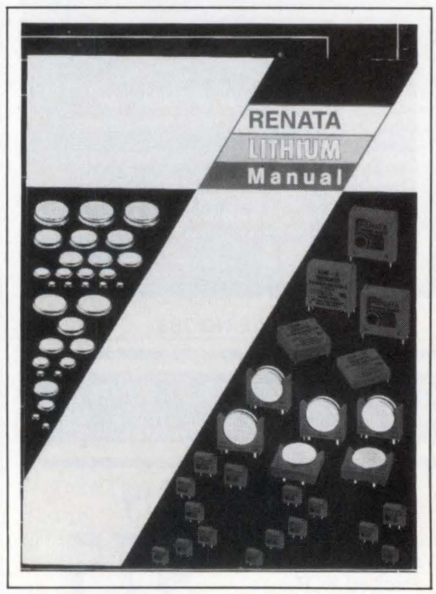

Booklet covers lithium products

This 28-pg manual deals with lithium batteries and power modules. Besides summarizing information on the vendor's complete line of products, the publication focuses on applications, and environmental, safety, and quality data. Its array of products and procedures includes industry-standard button cells for low-cost consumer and computer

LITERATURE

memory backup applications, as well as applications in process control, data acquisition, portable equipment, and factory automation.

International Power Sources Inc, 10 Cochituate St, Natick, MA 01760.

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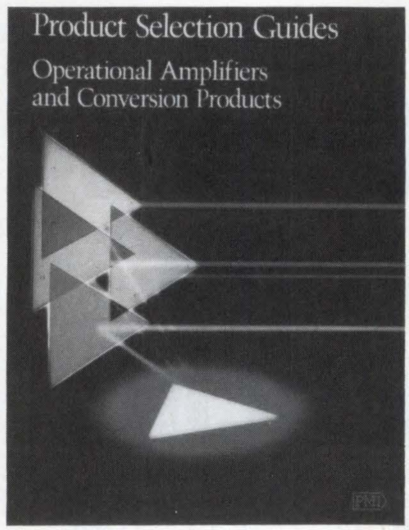

Choosing op amps and data-conversion products

The 8-pg *Product Selection Guide* features more than 80 operational amplifiers and data-conversion products. It provides information about single, dual, and quad op amps; and low-offset-voltage, low-power, low-bias-current, low-noise, high-slew-rate, and wideband amplifiers. The booklet's specification listings for 8-, 10-, and 12-bit-resolution ADCs and DACs simplify the selection of converter products.

Precision Monolithics Inc, Box 58020, Santa Clara, CA 95052.

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Safety-device options

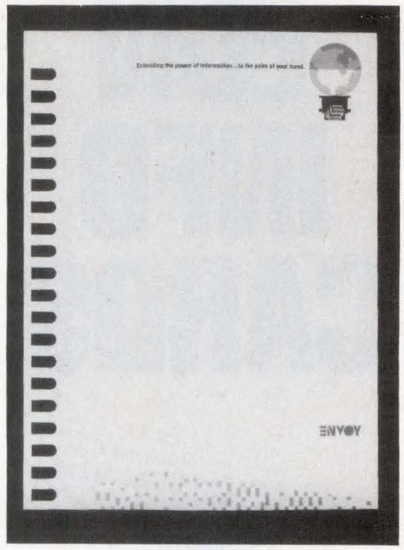
This 4-pg brochure deals with the company's safe interface controls for intrinsically safe circuits and lists specifications for the vendor's Series 17, 27, and recent Series 37 controls. It reviews applications, operational modes, and FM-, UL-, and CSA-approved models. The pamphlet also provides an abbreviated version of the National Electric Code from the National Fire Protection Association (Quincy, MA). To help you locate the areas where intrinsically safe controls are needed, it highlights hazardous location Classes I, II, and III.

Warrick Controls Inc, Box 460, Royal Oak, MI 48068.

Circle No 441

Coverage of memory cards in credit-card format

This brochure discusses the Envoy family of microchip memory cards, which features EEPROM, EPROM, and ROM memory in a credit-card format. It provides overall specifications, EPROM/CMOS/OTP Series and EEPROM/CMOS Series specifications, a product guide, and connector specifications. The card cutouts are pocketed in the back cover of the brochure for easy accessibility.



General Instrument Microelectronics, 2355 W Chandler Blvd, Chandler, AZ 85224.

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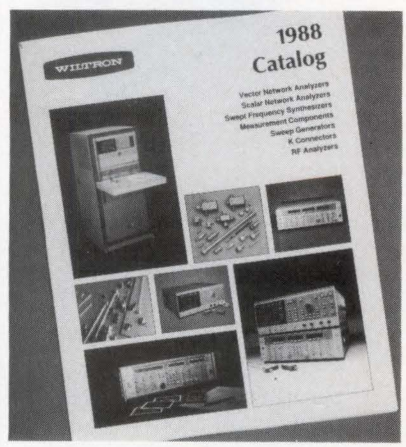

A catalog of microwave products

The vendor's 1988 92-pg, 4-color catalog highlights microwave measurement components, instruments, and systems in the dc to 60-GHz range. General information before each major product group helps you to make the best choice for your particular needs. The book also features complete specifications for precision measurement components; the K Connector coaxial product line, operates to 46 GHz; and a new line of 40-GHz fixed attenuators. Other new products include vector network analyzers, scalar network analyzers, swept-frequency synthesizers, sweep generators, and RF analyzers.

Wiltron Co, 490 Jarvis Dr, Morgan Hill, CA 95037.

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Static RAMs and programmable logic devices

The company's 102-pg catalog provides specifications for its complete line of high-performance PLDs and memory devices. It includes detailed information about advancements in E²CMOS PLD technology, the GAL (generic array logic) 39V18, and the GAL 16Z8, as well as specifications for the E²CMOS GAL and high-speed static RAM devices. Further, the publication features application notes and a sales office directory.

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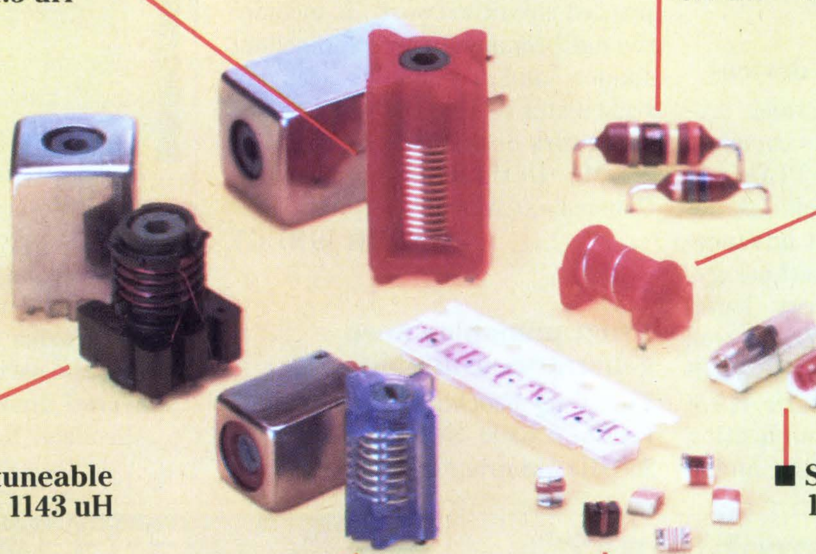

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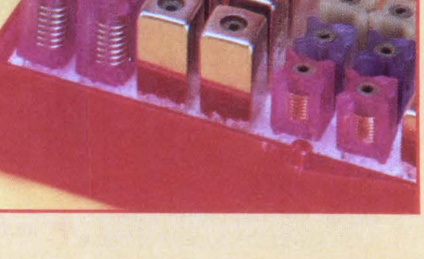

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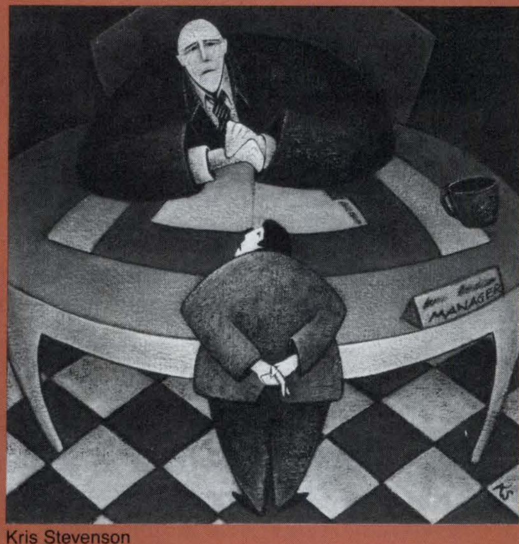

Kris Stevenson

Change is coming for performance reviews, but it's slow and painful

Deborah Asbrand,
Associate Editor

The good news about performance appraisals is that companies are finally starting to take them seriously. The bad news is that the review process is still so dreaded and steeped in misunderstanding that improvements are minimal.

"Performance appraisal is a no-win situation," concedes Bob Glen of the Naval Weapons Center at China Lake (CA). Glen recently managed a project that involved revamping the performance-appraisal system used for 5000 employees at the China Lake and San Diego naval bases. Conducting an evaluation and being evaluated, Glen said at the IEEE's 1987 conference on engineering careers, are "probably the most stressful things you can do. But there's no way around them."

It's small wonder, then, that for most employees, annual reviews entail the strained nervousness of a superpower summit conference. Employees step into their manager's office and wait to hear the category or label—unsatisfactory, satisfactory, or above average—to which the year's 50-odd weeks of work have been reduced. But subordinates aren't the only ones who shudder at the thought of yearly assessments. Managers report that they feel just as much, and maybe more, tension.

The problem with performance appraisals is that many businesses pay them only lip service. Instead of serving as an opportunity for a manager and subordinate to meet and constructively discuss the latter's professional strengths and weaknesses, the annual event is, by design, an exercise in paperwork by which the employer substantiates salary increases and promotions. For most workers, reviews are empty rites of the workplace: Employees need feedback on their performance every day, not just one day a year. And since few managers are trained to provide such support, companies are left with the task of salvaging some usefulness from a system of infrequent reviews.

Human-resource professionals gamely try to help. Performance appraisal is a favorite topic among training professionals, says Patricia Galagan of the American Society of Training and Development (Alexandria, VA). The organization's monthly magazine, *Training and*

Appraise (ə-praz): **1.** To set a value on, estimate the amount of **2.** To evaluate the worth, significance, or status of; *especially,* to give an expert judgment of the value or merit of
—*Webster's Ninth New Collegiate Dictionary*

Development Journal, runs several articles each year on implementing and improving performance-appraisal systems. Galagan, the magazine's editor, says the publication's 50,000 readers are hungry for information on the topic because "professionally, they believe it's important." But fueling their interest, she adds, are "the companies they work for," many of which are looking to improve their review systems.

Indeed, after years of viewing employee evaluations as a necessary evil, more American businesses are waking up to the advantages they can derive from a well-planned performance-appraisal system. Until recently, human resources was the stepchild of corporate culture, says Gary Latham, chairman of the University of Washington's management and organization department. But currently, he says, "there's the realization that we've put maximum efforts into finance and technology, and that we now have to put as much emphasis on our internal systems."

Many corporations, too, are seeking to eliminate cost-of-living salary increases and adopt a pay-for-performance system. Implementing merit pay, though, leads many businesses back to their appraisal processes. "Companies are finding that they can't begin to pay for performance until they're able to define what good performance is," says Audrey Ellison, marketing manager for Organizational Dynamics, a Burlington, MA management-training and consulting firm.

Also attracting employers' interest is the important role that review documents play in lawsuits that employees file against former employers—and the large sums that courts have been awarding employees for damages. For example, nine laid-off employees of Miles Inc, the maker of Alka Seltzer, sued the company for age discrimination. They claimed that they were given pink slips because of their ages, not their job performance; Miles countered that only the workers who performed most poorly were dismissed in the company-wide layoff. Miles lost the suit and in August 1986 was ordered to pay the workers $1.63 million in damages. Key to the fired employees' victory were copies of their performance reviews, which contained glowing descriptions of their abilities.

The paper chase

Parting with time-honored systems, though, is not easy. Many companies, for example, believe that revamping their evaluation forms can bring substantive change to their review systems. Studies, however, show that the arrangement of evaluation-form questions or the way they're phrased has little bearing on a review system's effectiveness. "Generally, all of the tools seem to work if the people using them believe in them," says Pat Gallegos, personnel director for Evans and Sutherland Computer Corp, a Salt Lake City, UT maker of high-end graphics terminals. "Whether you use a blank sheet of paper or a ranking system doesn't really matter."

> For most employees, annual reviews entail the strained nervousness of a superpower summit conference.

Relinquishing old attitudes about performance appraisal is even more difficult. The review process is an emotional mine field for managers and employees alike. "There's a lot of fear surrounding the process on both sides," says Richard Swanson, director of the University of Minnesota's training and development research center. "Supervisors don't feel comfortable being in a godlike position and judging people. So they avoid it."

Newly promoted or ill-trained managers are often unprepared for the hurt feelings and deflated egos that result from poorly conducted reviews. Don Wilson says that on first becoming a manager at Bell Laboratories in the 1960s, he expected to conduct performance reviews in the workmanlike fashion that he performed his other responsibilities. He quickly recognized his mistake. "I didn't think about how I was shaping the person on the other end of the process," he says. "It was only when I saw people were hurt that I realized how devastating [the performance review] can be to self-esteem."

Performance appraisals bring "a great deal of trauma to both parties," says Wilson, now a telecommunications researcher for Bell Communications Research in Morristown, NJ. Thirty-five years of reviewing and being reviewed have convinced Wilson of the futility of ranking, rating, and categorizing employees. "We're spending a lot of energy trying to measure very small differences between people and placing a great deal of importance on those differences."

Engineers, in particular, scoff at the quirks of the review process, so much of which hinges on the skills—and idiosyncracies—of the manager conducting the evaluation. Few performance-appraisal problems are occupation-specific, but consultants and researchers agree that engineers, whose field is so precise, chafe at the personal and subjective process of job reviews. "People in engineering always say that performance appraisals aren't objective or measurable enough," says Norman Smallwood, a partner of Novations Group Inc, a Provo, UT, consulting firm. "But the simple truth is that [judging] performance is always subjective."

The chief obstacle to achieving more communication and less measurement is management's reluctance to abandon the once-yearly review system. Feedback needs to occur regularly, human-resource officials say, not one day each year. Latham points to sports as the best example of how frequent discussions benefit performance: Coaches "don't wait until the end of the season to let people know what they're doing wrong."

Once-a-year reviews attempt to accomplish too much in too little time. In addition to covering an employee's job performance and rating, the review discussion often includes pay increases, possible promotion, and career guidance. As a result, employees leave their manager's office shell-shocked. "People are told that they're average performers, [and] they start to stew," says Smallwood. "Then they're told about a salary increase—which, because they're still stewing, they may not even notice—and then the manager says 'Now let's talk about your career.'"

Yet persuading companies to dismantle a system of annual reviews is difficult because most can't envision a replacement for it. "Companies want to part with it because it's not working, but the question they ask is 'how?'" says Ellison.

Experts agree that the first step to solving review-process problems is to conduct performance appraisals several times a year. Often, appraisals constitute the only opportunity employees have of receiving feedback on their work, and "they need to be done at least quarterly to do any good," says Latham. "Think about the surprise quizzes that you took in school. When you arrived in class, the teacher announced the quiz and instructed you to place your books under your seat. You hated it, but, boy, did you study for that class. Performance is at a maximum in that kind of class."

At the very least, says Latham, salary and promotion reviews should be conducted independently of performance reviews, particularly if employees are asked to perform self-evaluations. "Self-evaluations are worthwhile so long as money and promotion opportunities aren't tied to them," Latham says. "Then it's like asking the person to testify against himself."

The next task is helping managers to kick their dependence on the paperwork of the process and learn the art of constructive conversation. "Managers need to learn to explain their position," Gallegos says, "not defend it."

Feel like a number

The good news for employees is that the authors of human-resource studies are now turning their attention from the tools of appraisal to the targets of those tools—the employees. Researchers are examining how people respond to interviews and the ways in which they can disagree without feeling defensive.

A more humane system of appraisal, however, seems a long way off. The June 1987 issue of *Training and Development Journal* contained a monograph entitled "An uneasy look at performance appraisal," which has been widely cited by training professionals. In the article, the late Douglas MacGregor criticized the cold, assembly-line-like quality of most review systems. "As far as the assumptions of the conventional appraisal process are concerned," MacGregor wrote, "we still have what is practically identical with a program for product inspection."

MacGregor's theories are not controversial. Indeed, they are in close agreement with those of other industry experts. So, why has his monograph generated so much commentary? Because it's 30 years old, a reprint from a 1957 issue of the *Harvard Business Review.* **EDN**

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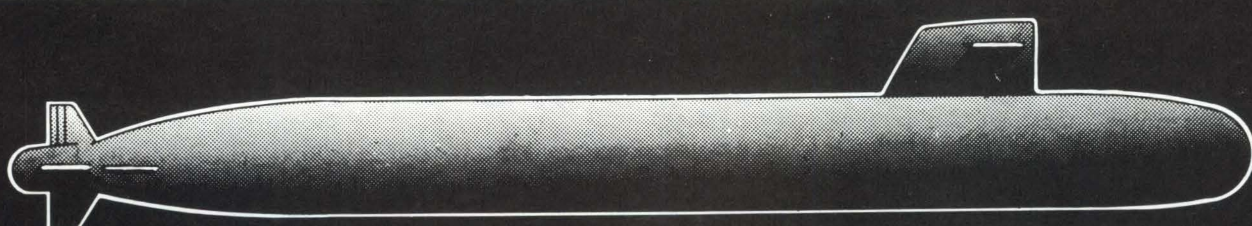

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Challenge your expertise in high-speed logic design and/or microprocessor system design using flow charts and timing diagrams for digital design and detailed design analysis. Your experience should include vendor libraries, test vendor generation, simulation checkout, and TTL emulators for gate array standard cell design. Familiarity with CAE systems used in logic design, test vector generation, simulation checkout, and documentation is also necessary. You must have five years' related experience plus a BSEE or equivalent degree; an MSEE degree is preferred.

Systems Software Engineers:

Evaluate, design, and develop firmware, operating systems, device drivers, and utility software for PC systems. You'll need a BSCS, BSEE or equivalent degree with four years' related experience in PC software development, 8086/286/386 Assembly/"C" language programming in MS-DOS, OS/2, and/or UNIX/XENIX operating systems.

Systems Architects:

Design new products by investigating and evaluating system compatibility and performance of design alternatives and new technologies. You'll develop hardware compatibility tests and performance analysis tools.

Qualify with a BSEE, MSEE preferred, and three years' hardware background with a knowledge of microprocessor-based systems software. In addition, experience with CPUs/memory/bus architecture, numeric co-processors, file subsystems, network/communications, graphic subsystems, and state machines is required.

Graphics Display Manager:

Coordinate and manage the definition, development and procurement of display subsystems. You'll provide compatible systems and develop high resolution products for engineering workstations, desktop publishing, and related applications.

You must have a BSEE or BS in Physics; an MS is preferred. Eight years' experience in electronics design engineering and management, including five years in design of computer equipment is necessary, as well as the ability to manage technical professionals in an engineering development environment.

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We currently have opportunities available in the areas listed below for individuals with a technical degree or the equivalent combination of formal education and related experience. Government or aerospace industry background is preferred. If you are interested in one or more of these areas, please send your resume to: Professional Staffing, GENERAL DYNAMICS SPACE SYSTEMS DIVISION, MZ C2-7143-I155, P.O. Box 85990, San Diego, CA 92138. (Opportunities also exist in Huntsville, AL and Harlingen, TX.)

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- Fairings
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- Pre-Design
- Liaison

FLUID SYSTEMS DESIGN
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- Hydraulic
- Propulsion
- Cryogenics

THERMAL/FLUIDS ANALYSIS
- Systems Modeling
- Space Environments
- Propulsion
- Cryogenics

AVIONICS
- EMI/EMC
- Electrical Power
- Instrumentation
- RF Systems
- Parts Engineering
- Harness Design/Installation
- Liaison
- Analog/Digital Circuit Design
- Avionics Systems
- Mechanical Packaging
- Control Systems
- Guidance & Navigation

SYSTEMS
- Systems Requirements
- Systems Safety

DYNAMICS/ANALYSIS
- Launch Vehicle Transient Load
- Environmental Dynamics
- Acoustics
- Jettison Trajectory
- IRAD & CRAD
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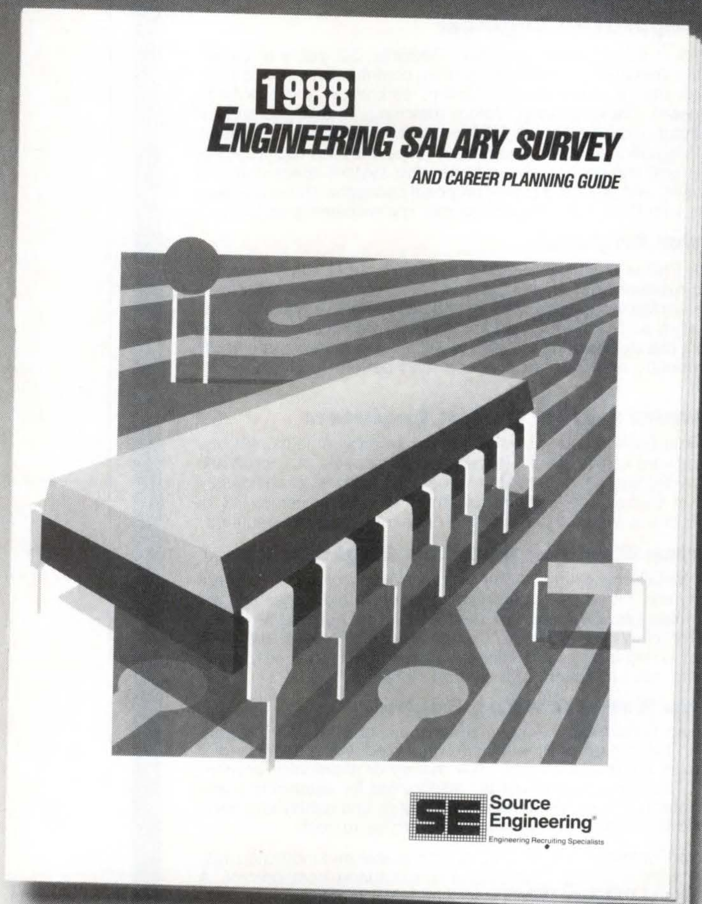

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Senior Engineer

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Avionics System Design Engineers

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Group Manufacturing Engineer

Qualified candidates will have a minimum of 5-10 years experience in the design or manufacture of printed wiring board and/or electronic chassis, preferably in a military or electronics environment. This new position will be responsible for establishing and coordinating a team to interface with design and quality engineering and to insure product design producibility to cost.

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This position is responsible for the programming, set-up and operation of automatic pick-and-place equipment and for troubleshooting the mechanical and electrical problems that occur with these systems. Also responsible for training maintenance personnel and recommending layout and artwork changes to products in order to improve their manufacturability.

A BSME and a demonstrated understanding of electro-mechanical principles in automatic component placement systems required.

INDUSTRIAL ENGINEERING SECTION MANAGER

Reporting to the Manager of PCB Assembly, this position is responsible for directing the activities of the Industrial Engineering Group who support all the major product lines in this microcircuit manufacturing facility. Included is the development, modification and documentation of the process. flow diagrams, visual line aids for the assembly operations and labor rate standards and line balance audit. Also responsible for reviewing equipment capacity and performing operational analysis time studies.

Experience in the fabrication of conventional and SMD PC Board assembly is required. Familiarity with polymer, thick film or chip and wire microcircuits would be beneficial. BSIE required.

QUALITY ASSURANCE ENGINEER

This individual will establish the measurements and process controls necessary to detect entry of any factors that might adversely affect product quality or reliability. Also, this position will develop and implement quality levels and appropriate defect classification for quality rating of assembled products.

A BSEE or equivalent along with 2 years experience in the setting-up and usage of statistical process controls is required.

TEST EQUIPMENT SECTION MANAGER

Reporting to the Plant Manufacturing Engineering Manager, this position will be responsible for developing and implementing test systems and production equipment improvements which will result in improved reliability and overall performance. This individual will also manage test systems maintenance, spare parts inventory and upgrades to existing equipment.

Requirements include a BSEE and practical experience with the programming and maintenance of integrated manufacturing line test equipment (i.e., Everett Charles, Zehntel, H.P., Gen Rad and Teradyne systems).

ELECTRICAL ENGINEER

Laser Systems

Position involves maintaining equipment for optimum performance of laser systems, which will include development of laser trim programs, and training personnel in set-up and operations.

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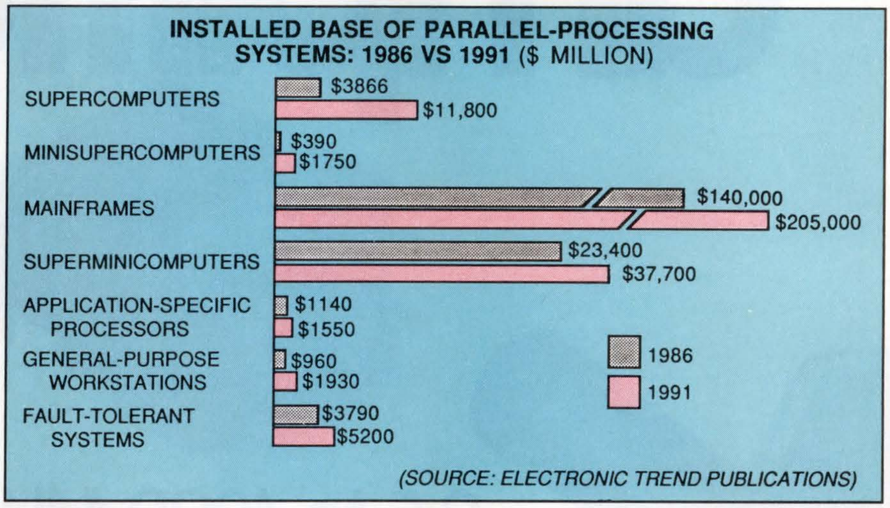
LOOKING AHEAD

EDITED BY CYNTHIA B RETTIG

Parallel processing spurs high-end-computer growth



Parallel-processing architectures will account for 26% of the growth in the worldwide high-performance computer market from 1986 to 1991, according to a report by Electronic Trend Publications (ETP) of Saratoga, CA. In 1985, total revenues from systems shipped in this market equaled $20 billion. In 1990, revenues will be $39.6 billion, and 48% of all systems shipped will incorporate some form of parallel-processing design. Although mainframes and superminicomputers will represent 87% of the 1990 market's dollar value, a new class of computers—including minisupercomputers, data processors, array processors, and symbol processors—will account for more than $1 billion of the market's value. The value of the total installed base of parallel-processing machines, which was $173.5 million in 1986, will rise to $264.9 million by 1991.

In the early stages of the market's growth, the demand for parallel-processing machines will come primarily from the scientific and technical fields. However, as 1990 approaches, the drawbacks of alternative processing methods will augment the growth of parallel-processing systems. ETP's report points out a number of these drawbacks. In the first place, single-processor-based architectures are reaching their theoretical limits in terms of speed. Further, I/O linkages in application-specific array processors and networks can be slow. Finally, general-purpose minicomputers and mainframes will simply prove unsuitable for high-performance computing, for which application-specific systems will prove necessary.

Because parallel processing uses multiple arrays of CPUs simultaneously, it can achieve speeds 10 to 100 times faster than can the older, uniprocessor systems. Hardware or hardware-related issues crucial to parallel processing include VLSI circuitry, gallium arsenide ICs, megabit-memory-chip development, improved internal channel speeds, hybrid optoelectronic circuitry, and better technology for cooling circuitry. All of these key elements are either under development or already available.

Software development for parallel-processing systems is proceeding more slowly, however. ETP identifies three major stumbling blocks in this area: the design of operating systems specifically geared for parallel operation, confusion about a standard for higher-level languages, and the problem of designing appropriate language compilers.

EMI/RFI market to exceed $8 billion by 1993

From 1983 to 1986, the market for EMI-shielding equipment and facilities grew from $540 million to more than $1 billion. By 1993, the market will exceed $8 billion, according to MIRC (Market Intelligence Research Co) of Mountain View, CA. Increased demand from government, military, and industrial sectors will drive this healthy growth rate.

The sophistication of modern electronic equipment and a heightened awareness of security needs have made EMI a critical issue. Industry in general has become more concerned about how EMI influences product performance, and the government and military sectors are placing increasing emphasis on protection from security leaks. At the same time, EMI-shielding products are steadily growing more dependable, more attractive in price, and better looking.

MIRC divides the market for EMI-shielding equipment and facilities into two major segments: architectural shielding structures and shielding for electronic equipment. Suppliers of architectural shielding structures are striving to provide turnkey services to customers. Among their products are windows with such features as wire mesh and transparent conductive coatings; room enclosures, which include both welded stand-alone and modular products; doors and walls; and building materials and related services. Suppliers of electronic-equipment shielding offer such products as paint; zinc arc spray; plating; conductive plastics; and minor products such as conductive foils, tapes, gaskets, and sealants.

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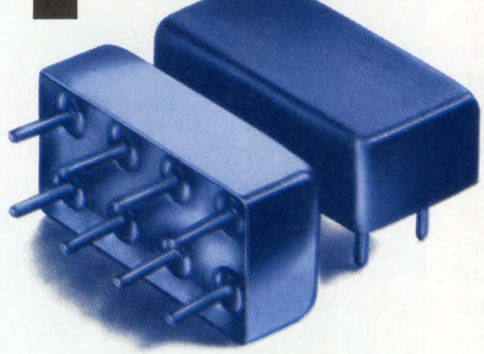

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MAN-1LN	0.5-500	28	1.0	8	2.8	60	15.95
◇MAN-1HLN	10-500	10	0.8	15	3.7	70	15.95

††Midband $10f_L$ to $f_{u/2}$, ± 0.5dB †1dB Gain Compression ◇Case Height 0.3 In.
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