A CAHNERS PUBLICATION

MARCH 14, 1991

EDN®

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Special Report:

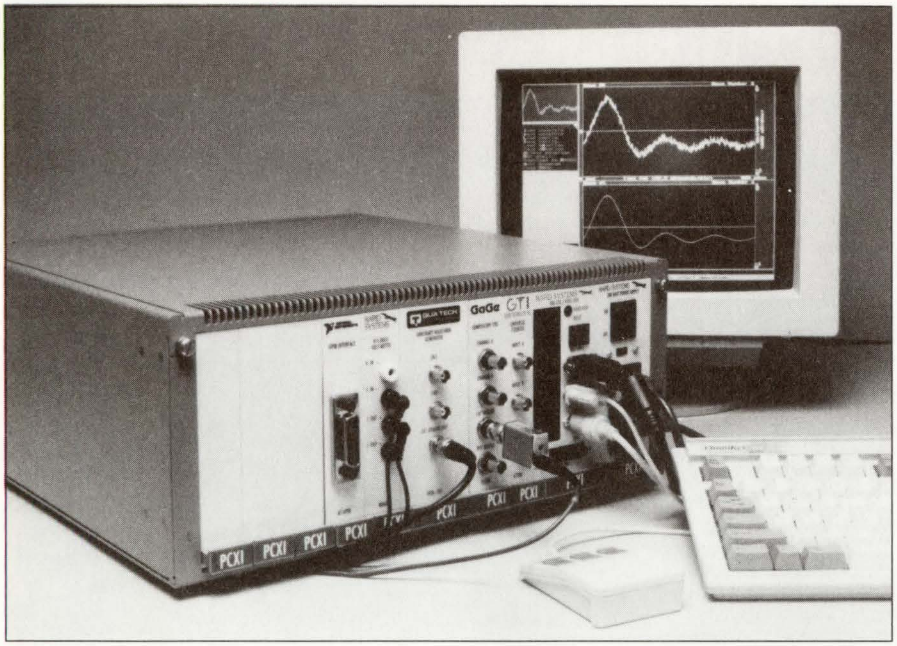
Instrumentation amps extract elusive signals in common-mode noise

pg 82

Presenting the three rules of BiCMOS design.

Lead, follow, or get out of the way.

It's Everything a PC Isn't.



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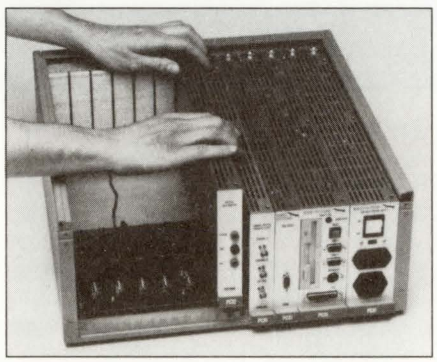

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But for all those thousand and one other jobs, well, PCXI is a lot like VXI. VXI is modular and upgradeable, so is PCXI. They primarily use a 286/386 CPU, so do we (except we can also offer you a 486). VXI has quite a few instrumentation and function modules from manufacturers, so does PCXI (except there are thousands of modules, off-the-shelf, from hundreds of manufacturers). We even look alike.

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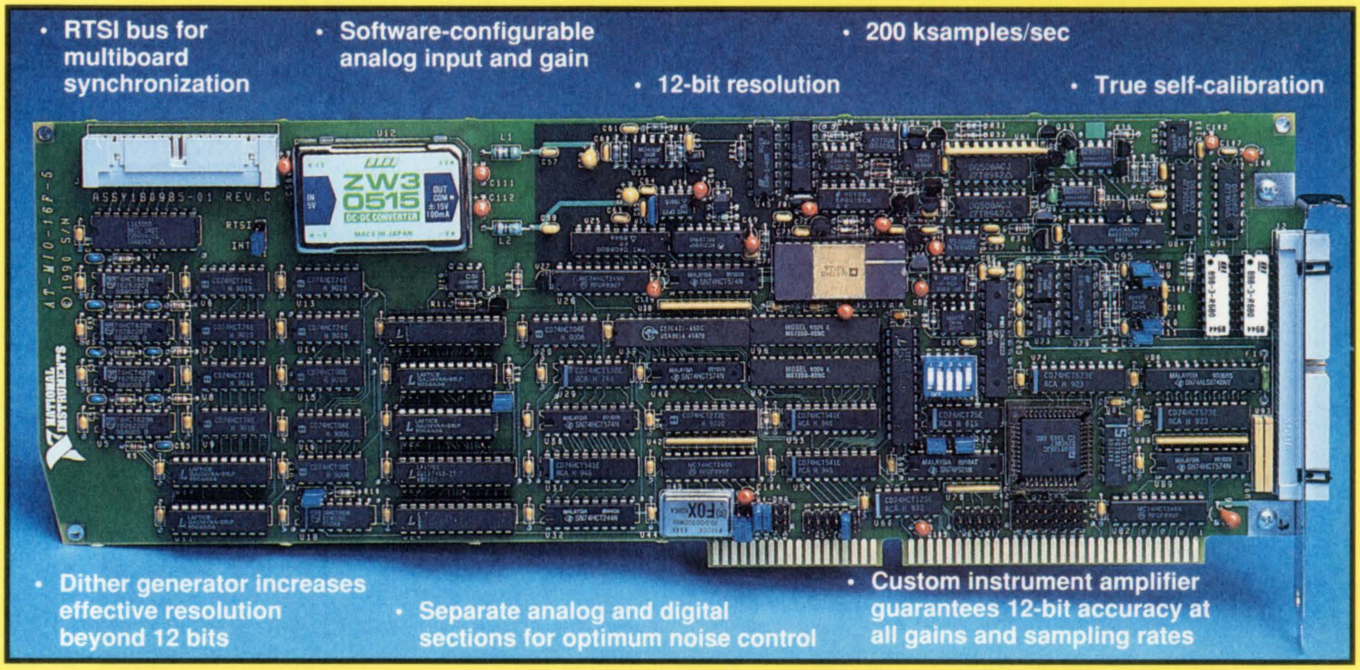

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AT-MIO-16F-5	AT	16 SE 8 DI	200,000	12	±5, 0 to 10	0.5, 1, 2, 5, 10, 20, 50, 100	2	12	8	3	√	√				
AT-MIO-16H-9 AT-MIO-16H-15 AT-MIO-16H-25	AT	16 SE 8 DI	100,000	12	±10, ±5, 0 to 10	1, 2, 4, 8	2	12	8	3	√ √ √	√ √ √		√ √ √		√ √ √
AT-MIO-16L-9 AT-MIO-16L-15 AT-MIO-16L-25	AT	16 SE 8 DI	100,000	12	±10, ±5, 0 to 10	1, 10, 100, 500	2	12	8	3	√ √ √	√ √ √		√ √ √		√ √ √
Lab-PC	XT	8 SE	62,500	12	±5, 0 to 10	1, 2, 5, 10, 20, 50, 100	2	12	24	3	√	√	√	√		√
PC-LPM-16	XT	16 SE	50,000	12	±5, 0 to 10 ±2.5, 0 to 5	1	–	–	16†	3	√	√	√			
AT-DIO-32F	AT	–	–	–	–	–	–	–	32	–	√	√				√
PC-DIO-96	XT	–	–	–	–	–	–	–	96	–	√	√	√			
PC-DIO-24	XT	–	–	–	–	–	–	–	24	–	√	√	√			√
PC-TIO-10	XT	–	–	–	–	–	–	–	16	10	√	√	√			
EISA-A2000	EISA	4 SE SS	1,000,000	12	±5	1	–	–	–	–	√	√			√	

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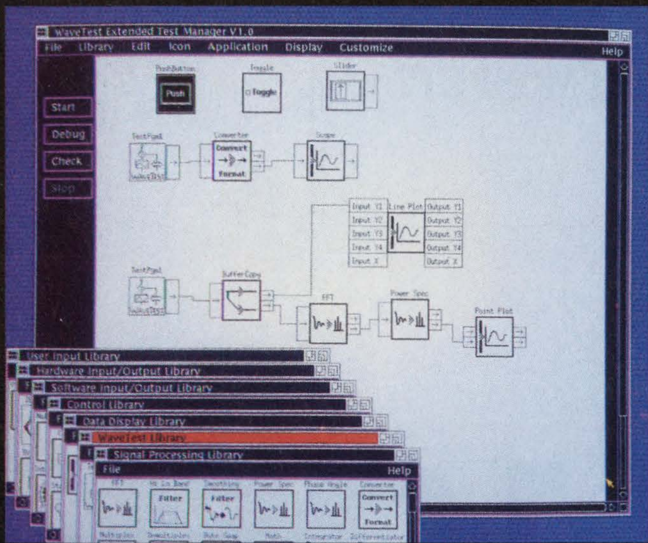
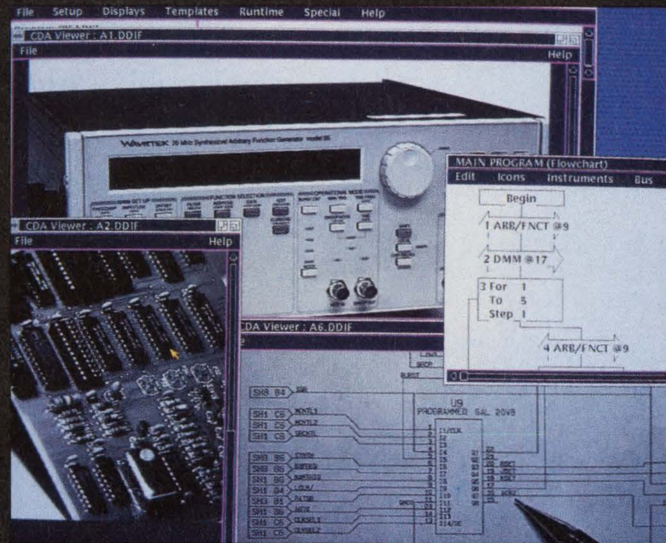


Just select and move icons to build a complete ATE test and data management program.



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Circle 11 for Literature

Circle 12 for Demonstration

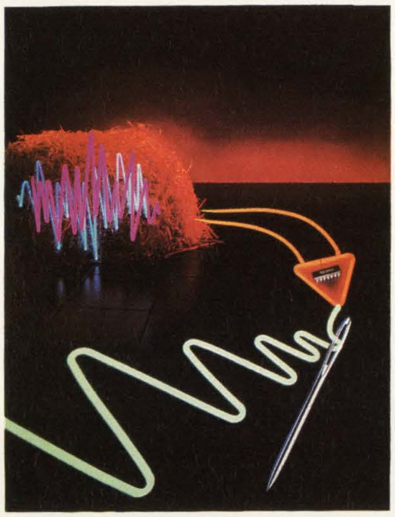
WAVETEK®

Volume 36, Number 6

EDN Magazine Edition®

March 14, 1991

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *If your amplifier has too much inherent noise, your signal can get lost and become indiscernible. Today's monolithic instrumentation amplifiers, however, offer an economical and accurate alternative to identifying even weak signals. See our Special Report beginning on pg 82. (Photo courtesy Burr-Brown Corp)*

SPECIAL REPORT

DESIGN FEATURES

TECHNOLOGY UPDATES

Continued on page 7

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BPA ABP

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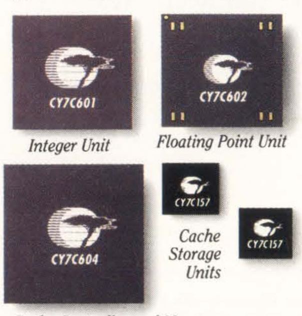
The new SPARCstation™2 from Sun Microsystems delivers almost twice the CPU performance of previous generations – the highest performance in its class.



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Continued from page 5

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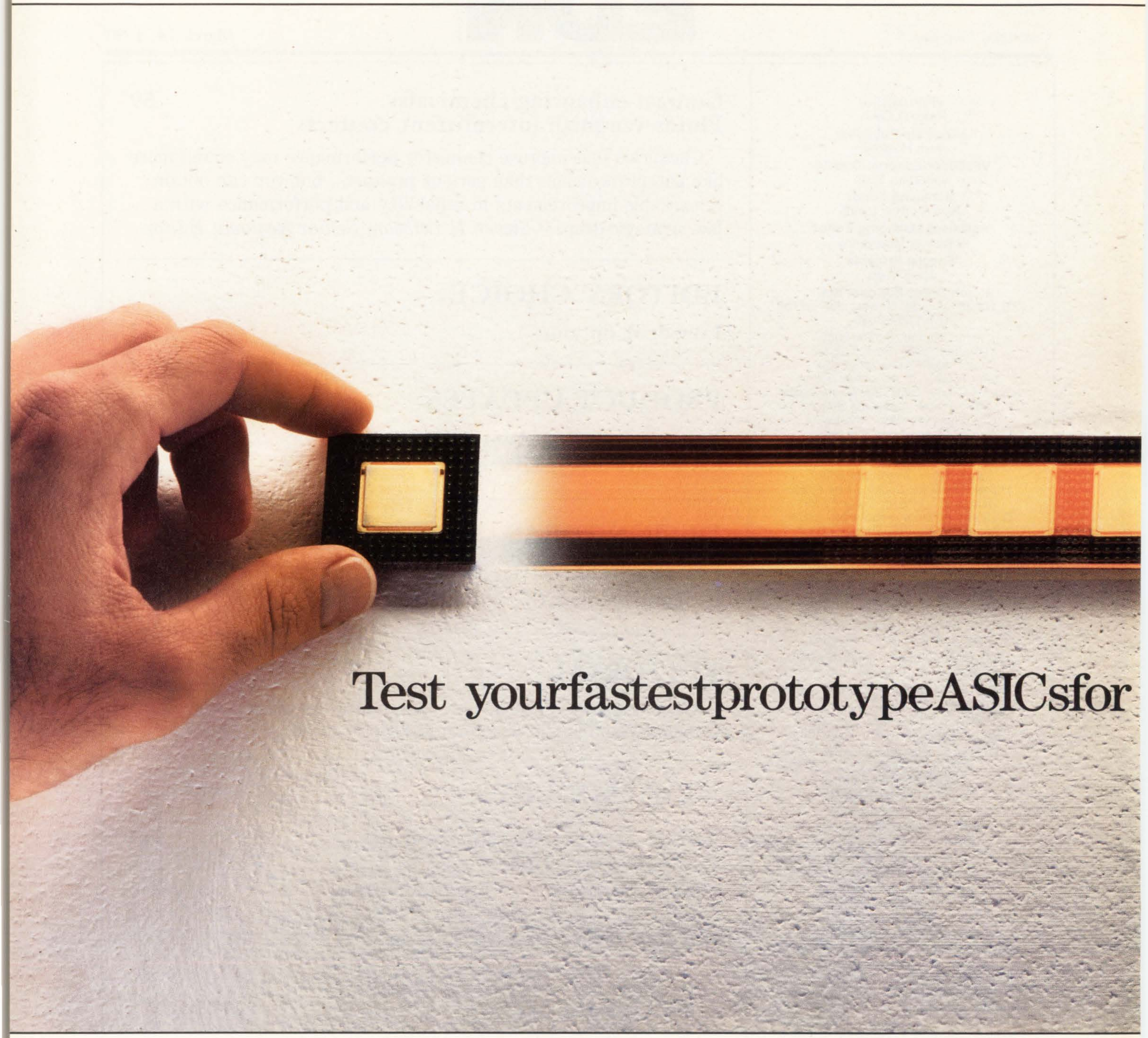

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Before you send those fast ASIC designs off to production, make sure they'll handle the stress of real-world operating conditions.

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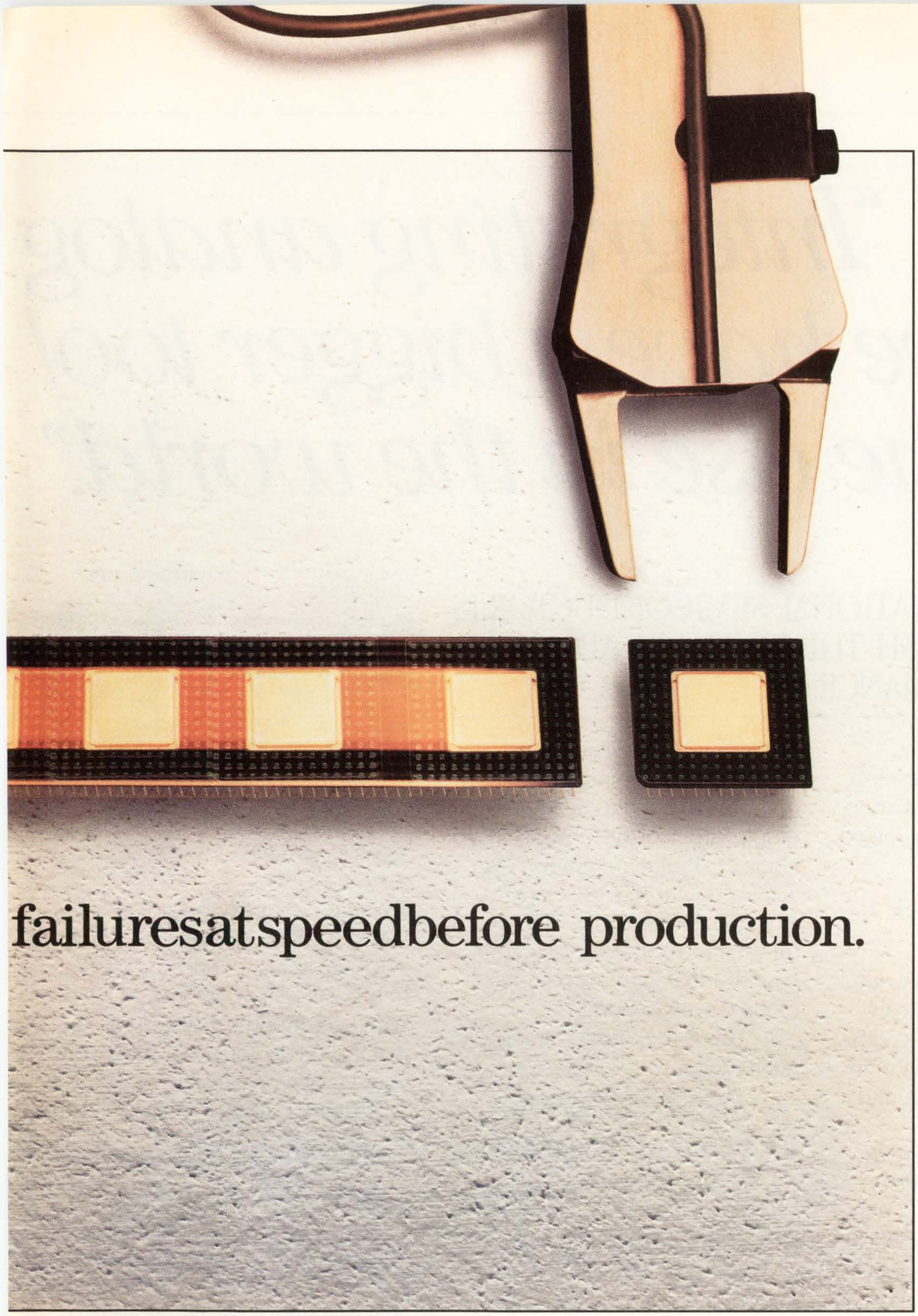

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CIRCLE NO. 69

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"Our first Futurebus+ chipset contains five devices, and they employ some of the most advanced analog+digital integration ever achieved. Our BTL drivers, for example, let the digital CPU send information to the digital memory over the analog bus at peak rates of 2-3 Gbytes/second!

"This is the future — and we've got it today."

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"Another great example is CLASIC, our powerful Custom Linear ASIC family.

"To reach system-on-chip performance, you've got to integrate analog and digital functions onto the same substrate.

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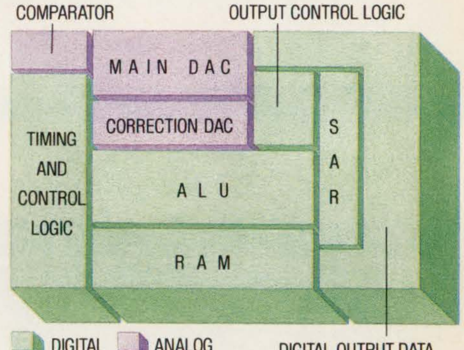

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"Our new ADC1251 takes a quantum leap in integration. It's powered by a sophisticated digital controller and is totally self-calibrating, so it will maintain linearity over time, temperature, and supply voltage.

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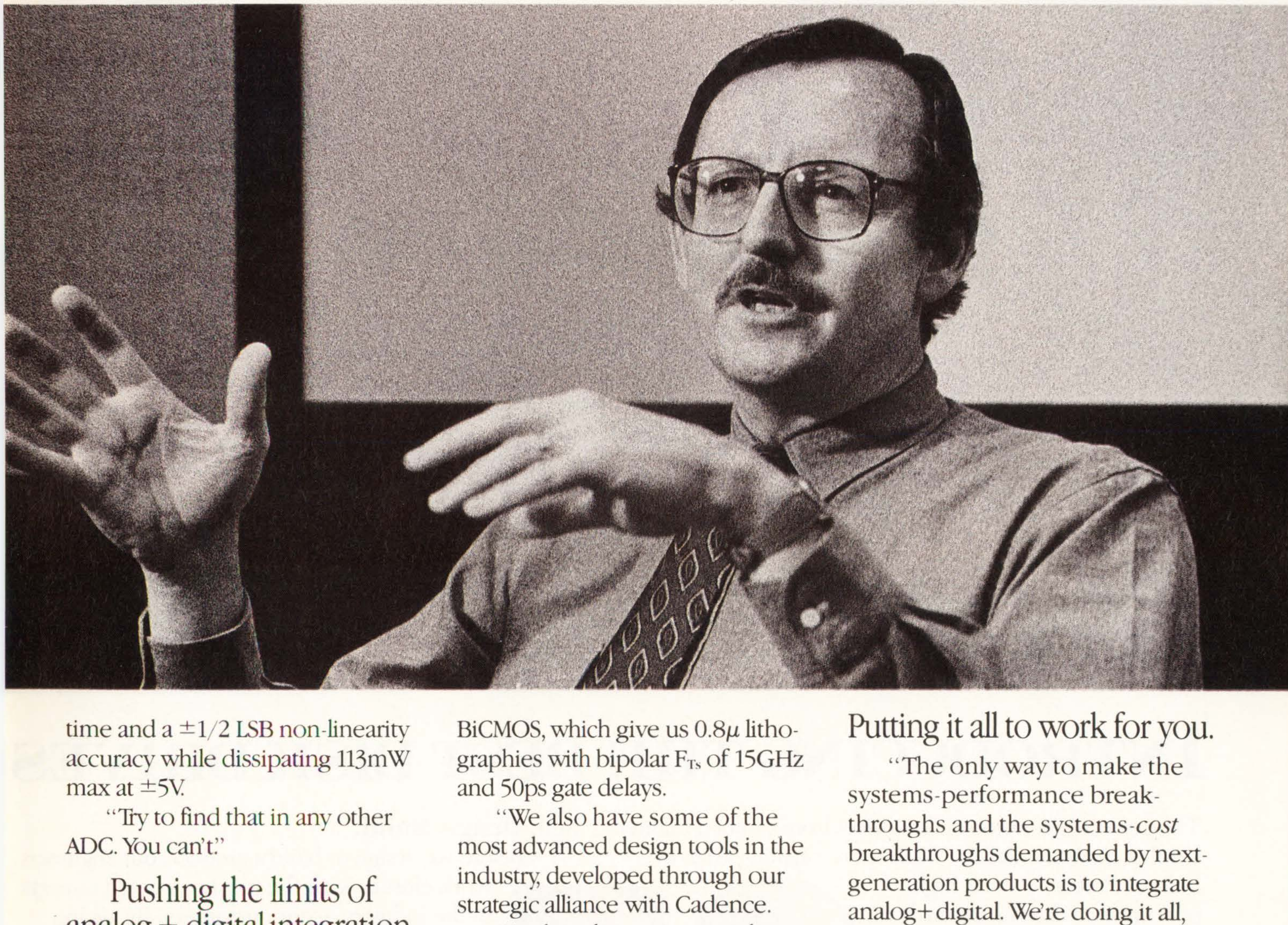

time and a $\pm 1/2$ LSB non-linearity accuracy while dissipating 113mW max at $\pm 5V$.

"Try to find that in any other ADC. You can't."

Pushing the limits of analog + digital integration.

"To achieve these levels of integration, you need powerful tools in the hands of experienced designers.

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Putting it all to work for you.

"The only way to make the systems-performance breakthroughs and the systems-*cost* breakthroughs demanded by next-generation products is to integrate analog+digital. We're doing it all, right now. So if I were a designer, I'd call us. Soon."

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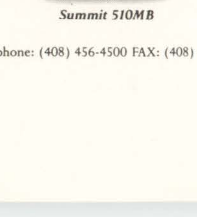
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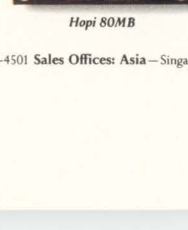
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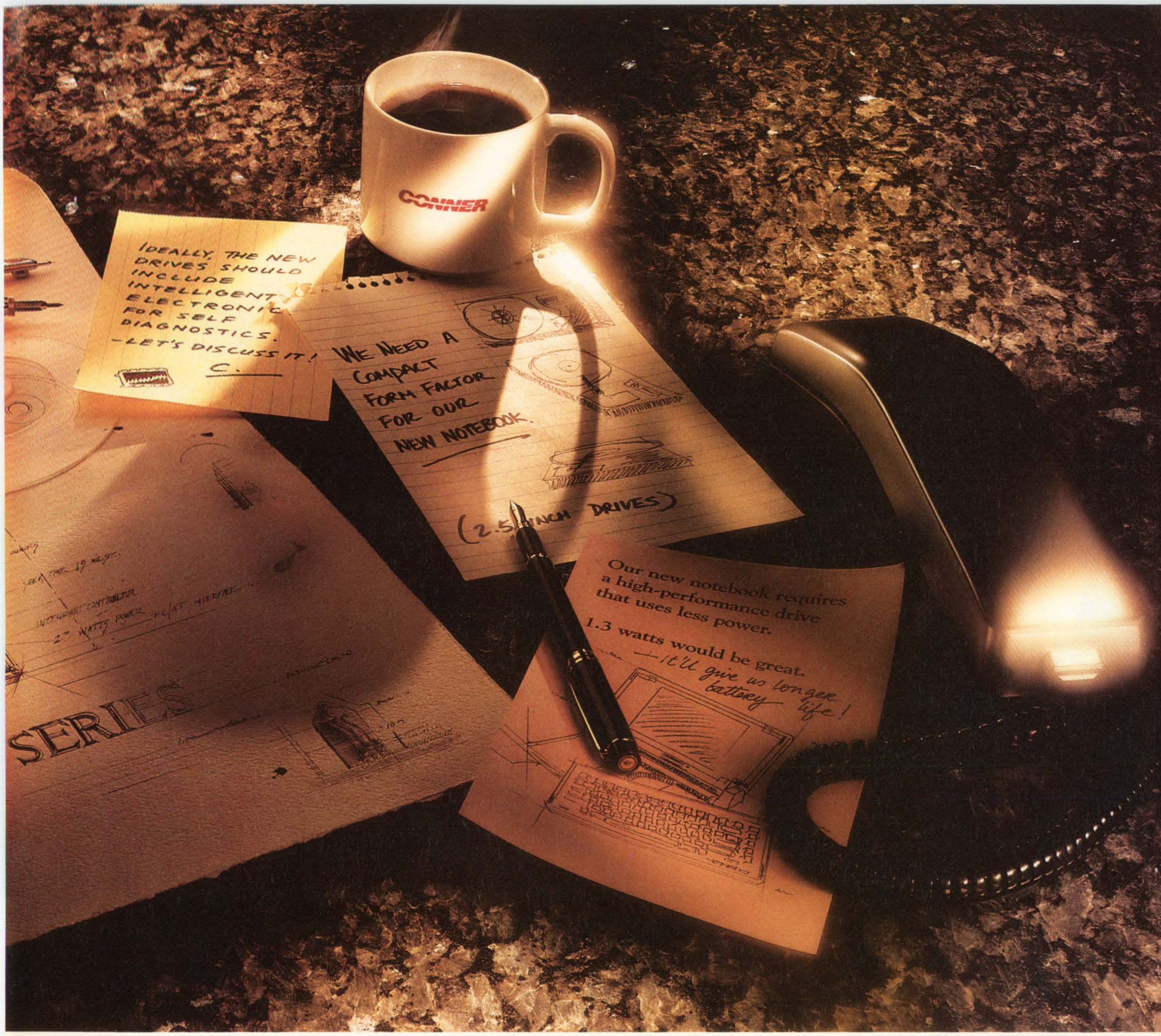

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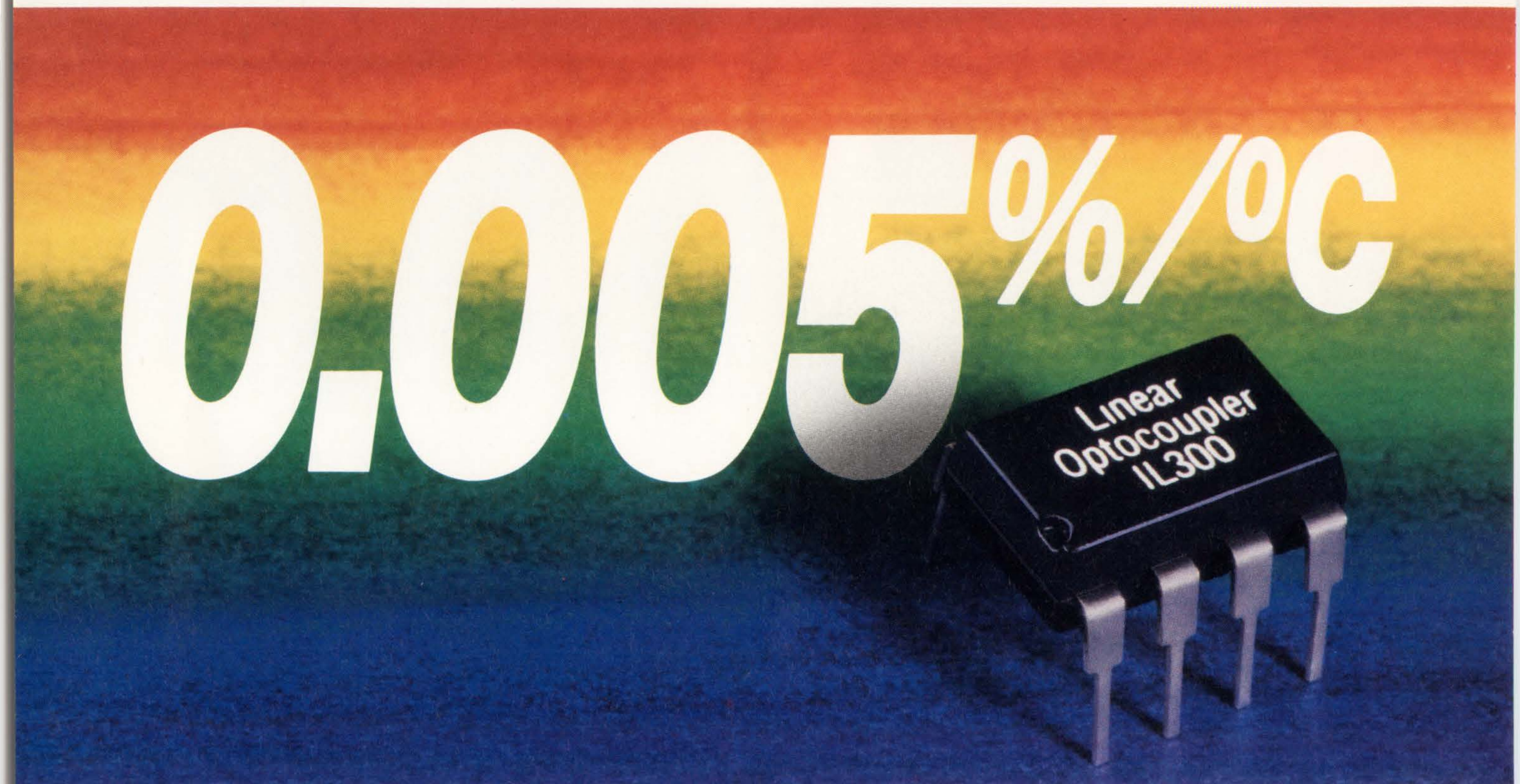


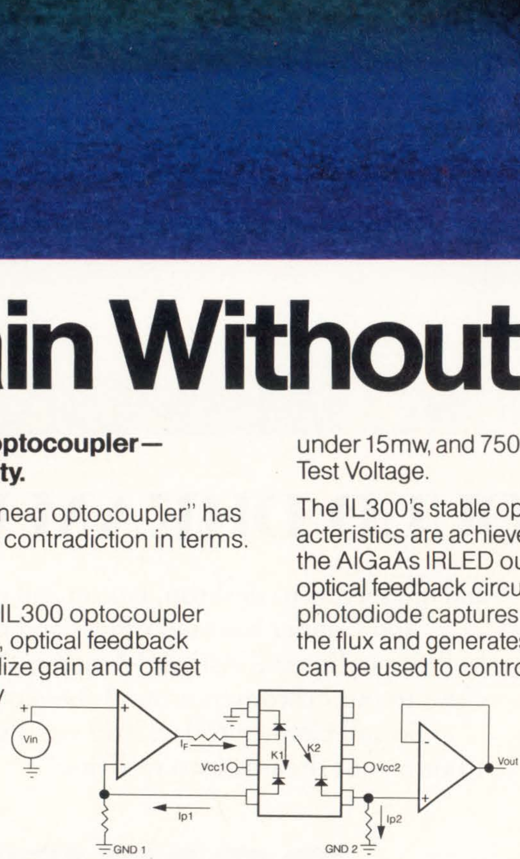
Gain Without Pain.

New linear optocoupler— Rx for stability.

The phrase "linear optocoupler" has always been a contradiction in terms.

Until now.

Siemens new IL300 optocoupler uses a unique, optical feedback loop to neutralize gain and offset drift caused by temperature and LED degradation. The results will change the way you think about optocouplers: DC gain stability of ±0.005%/°C, ±0.01% servo linearity, a wide (>200KHz) bandwidth, power consumption under 15mw, and 7500 VAC Withstand Test Voltage.



The IL300's stable operational characteristics are achieved by controlling the AlGaAs IRLED output flux with an optical feedback circuit. The servo PIN photodiode captures a percentage of the flux and generates a signal that can be used to control the LED drive current. This compensates for the LED's inherent non-linear, time, and temperature characteristics.

The IL300's stability and excellent isolation characteristics make it ideal for power supply regulation, medical sensor isolation, audio signal interfacing, digital telephone isolation, and many other applications.

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CIRCLE NO. 88

NEWS BREAKS

EDITED BY SUSAN ROSE

SOLID-STATE STORAGE DEVICE REPLACES DISK DRIVES

Winsystems' $325 MCM-RSSD IC memory-card drive can replace a floppy-disk drive in STD Bus applications. It replaces conventional rotating-disk memories in harsh environments where computers are subject to extreme temperatures, magnetic fields, vibration, dirt, and fumes. The drive uses ESD-resistant RAM data cartridges that store as much as 2M bytes of data. The drive has an operating temperature range of 0 to 65°C and comes with a card ejector, vibration-resistant front-panel latch, and a front-panel status display. The host STD Bus microcomputer identifies the drive as an I/O-mapped card. A bootable BIOS extension for this unit costs $50. The CMOS version of the drive, the LPM-RSSD, is $335. Winsystems Inc, Arlington, TX, (817) 274-7553, FAX (817) 548-1358.—J D Mosley

S/H-AMPLIFIER ARCHITECTURE OPTIMIZES DYNAMIC SPECS

The AD9100 S/H amplifier from Analog Devices integrates a closed-loop input amplifier with a switching network that reduces distortion but maintains the slew rate of traditional open-loop S/H-amplifier designs. The acquisition time to a 2V step is typically 16 nsec to 0.01% accuracy, which translates to 12-bit accuracy at clock rates of 30M samples/sec. The amplifier's hold-mode distortion is guaranteed to be less than −81 dB (full scale) for frequencies as high as 12 MHz and −74 dB for frequencies as high as 20 MHz. The amplifier can drive capacitive loads as high as 100 pF, making it a good match for 8- and 10-bit flash converters that operate as high as 60M samples/sec.

The amplifier requires ±5V supplies. It has an internal hold capacitor and internal decoupling capacitors. The differential ECL encode clock reduces jitter to less than 1 psec, and the device internally clamps the analog input to prevent damage from voltage transients. The amplifier's spectral noise density is 3.3 $nV\sqrt{Hz}$, and feedthrough rejection is 83 dB at 20 MHz. The device is available in a 20-pin ceramic DIP specified for commercial, industrial, or military temperature ranges. The commercial temperature version costs $79 (100). Analog Devices Inc, Greensboro, NC, (919) 668-9511, FAX (919) 668-0101.—Anne Watson Swager

HANDHELD TESTERS SPOT LAN CABLE PROBLEMS

Cabling problems crash networks. The HP J2181A, HP J2177A, and HP J2187A handheld testers from Hewlett-Packard can help you find such problems quickly. Two of the testers incorporate time-domain reflectometers that isolate and identify faults in LAN cables: The $1495 HP J2181A cable scanner locates faults in coaxial and simple twisted-pair cables, and the $2495 HP J2177A pair scanner performs the same task for more complex twisted-pair systems. The $995 HP J2187A quick scanner performs LAN diagnostic tests. All three testers incorporate 2-line LCD displays for presenting setup and diagnostic messages. Hewlett-Packard Co, Palo Alto, CA, phone or fax the local office.—Steven H Leibson

MICROCONTROLLER HOUSES EPROM, EEPROM, AND ADC

The single-chip ST90E40 8-bit CMOS microcontroller from SGS-Thomson combines 16k bytes of EPROM for program storage with 512 bytes of EEPROM and 256 bytes of RAM mapped into data space. Also on chip are an 8-bit ADC, eight channels, sample-and-hold. The chip also has a conversion time of 11 μsec. The chip has two 16-bit programmable timers and a 375k-baud serial communications interface. Seven 8-bit I/O ports carry the address and data bus, status and timing signals, analog inputs, interrupts, and serial or parallel data. The 12-MHz ST9-series core processor has a 128k-byte address range, 256-byte register file, and DMA control. The ST90E40 in a 68-pin ceramic leaded chip-carrier package is $50 (1000). The 1-time-programmable ST90T40 in a plastic leaded chip carrier, expected by the third quarter of 1991, will cost $20 (10,000). The ST9040 with 16k bytes of maskable ROM in place of EPROM, due at the end 1991, will cost $8 (100,000). SGS-Thomson Microelectronics, Agrate, Italy, (39) 60351, FAX (39) 6035700.—Brian Kerridge

PERIPHERAL IC MAKES μP CRASH PROOF

The Micro Softener IC from Dallas Semiconductor lets an assortment of μPs resume operation after a power outage by retaining calibration, program, and data information. The chip acts as a power monitor, a watchdog timer, a nonvolatile controller, an address decoder, a bootstrap ROM, and dual-port register file. It has its own uninterruptable lithium-battery power supply. The chip lets you make software updates or changes via an on-chip serial port for the 6303, 68HC11, 80C196, and the 8086-compatible V40 μPs, thus eliminating any need to open the system to access the IC. The chip's on-chip bootstrap loader automatically initializes the μP with application code you can download from any IBM PC. Therefore, you don't need to add a boot EPROM to your circuit. The chip also provides additional I/O capabilities for sensors and pushbuttons with its 32 parallel-port pins. Prices for the chip range from $7 to $9.20 (1000), depending upon the μP. Dallas Semiconductor, Dallas, TX, (214) 450-0448, FAX (214) 450-0470.—J D Mosley

ADA COMPILER TRIPLES PREDECESSORS' SPEED

The latest version of the Ada Software Development Environment for 80486-based IBM PCs running DOS creates code that runs three times faster than that of its predecessor. The $4995 package includes an optimizing compiler and runtime executive, binder, multiple libraries, symbolic source-level debugger, program viewer, cross-reference generator, a make utility, source-code reformatter, and a math package. The package operates the Intel 80486 μP in its 32-bit mode, which circumvents the operating system's 640k-byte RAM limits and the constraints of segmented architecture imposed by the μP's antecedents. The package requires 4M bytes of extended memory. Alsys Inc, Burlington, MA, (617) 270-0030, FAX (617) 270-6882.
—Steven H Leibson

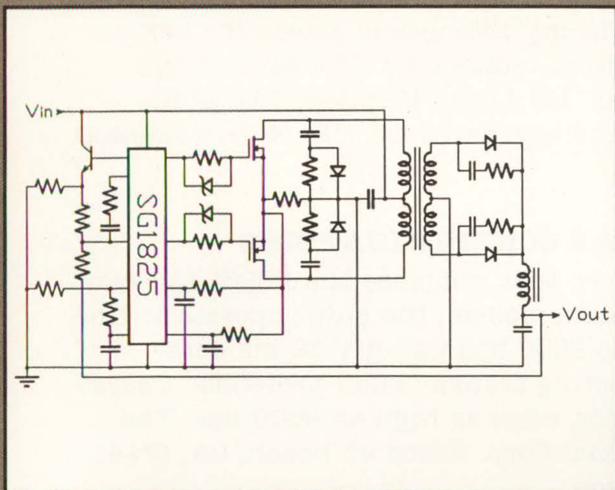
DIFFERENTIAL INPUTS QUIET CONVERSION

The TLC1225 from Texas Instruments uses differential inputs to reduce system errors created by common-mode noise. For single 5V supply operation, the input common-mode voltage range is 0 to 5V. The converter suits industrial control and data communications and is compatible with most μPs and DSPs. The device features a 12-μsec conversion period. The device's self-calibration eliminates factory laser trimming and offset adjustments in the field. You initiate calibration, which takes 300 clock cycles to complete, by issuing a command word to the data bus. The TLC is available in a plastic DIP characterized over a temperature range of −40 to +85°C and costs $16.74 (1000). The TLC1125, an 11-bit linear device similar in all other respects to the TLC1225, costs $11.17 (1000). Texas Instruments Inc, Dallas, TX, (800) 336-5236, FAX (214) 995-4360.—Anne Watson Swager

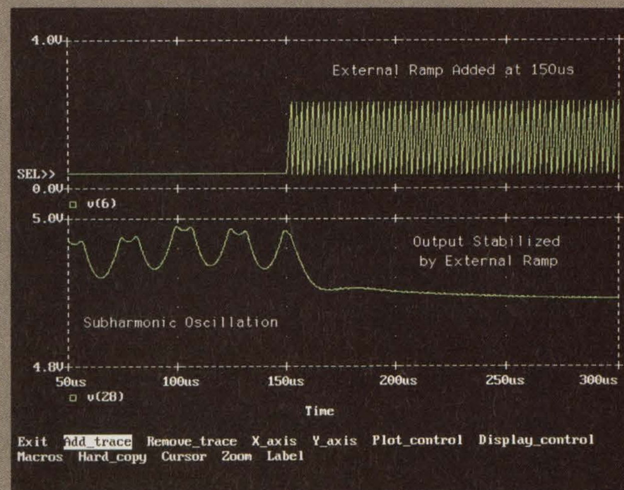
PSpice

MicroSim Corporation

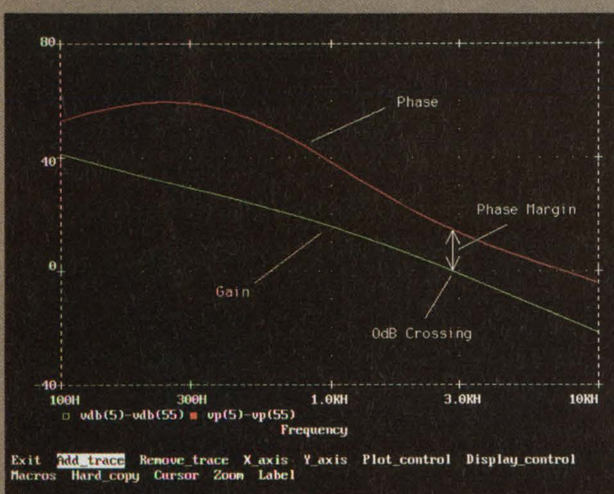
The Standard for Circuit Simulation Switch-Mode Power Supply Design



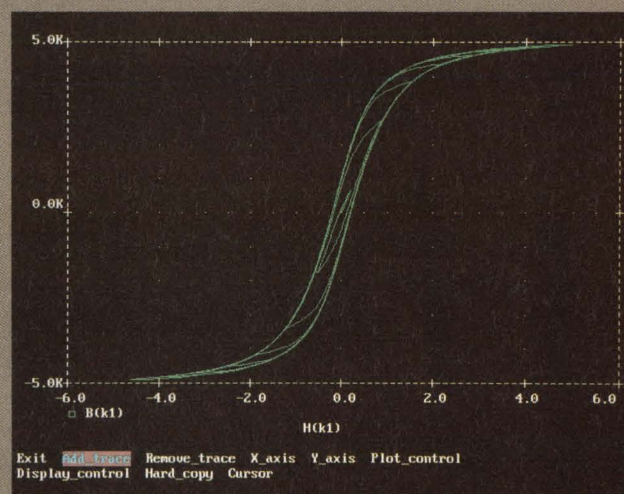
Current mode power supply schematic.



Power supply simulated using mixed analog/digital simulation. Plot shows subharmonic oscillation being suppressed by external ramp.



Simulation using the Vorperian switch model to examine the stability of a power supply.



Hysteresis curve of transformer.

A cycle by cycle simulation of switch-mode power supplies is recognized as a difficult simulation task for SPICE-based simulators, which must cope with timings that can span 4 orders of magnitude. This problem invariably results in very long simulation times, but is improved considerably by MicroSim's approach of building the controller macromodel chips so that a significant section is simulated in the digital domain. PSpice's behavioral modeling and mixed analog/digital simulation capability makes this possible.

PSpice is available on the IBM-PC (running DOS or OS/2); Macintosh II; Sun 3, Sun 4, and SPARCstation; DECstation 2100, 3100, and 5000; and the VAX/VMS families. In addition to the PWM macromodels, the PSpice library contains over 3,500 analog and 1,500 digital parts which can be used in a variety of applications. Our technical staff has over 150 years of combined experience in CAD/CAE, and our software is supported by the engineers who wrote it.

For further information about the PSpice family of products, call us at (714) 770-3022, or toll free at (800) 245-3022. Find out for yourself why PSpice has become the standard for circuit simulation.

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CIRCLE NO. 85

GATE ARRAY INCLUDES BUILT-IN TEST NETWORK

LSI Logic's LFT150XXX series family of gate arrays uses the built-in test technology developed by Crosscheck Technology Inc. The technology allows you to read every node in your completed design, thus simplifying test vector creation.

The family has four initial members, offering between 270 and 410 I/O lines. Their sizes range from 86k to 190k available gates, offering 43% usable gates. The arrays use the company's 1μm HCMOS LCA100K gate-array technology. The gate arrays start at $120 (10,000) for 160-pin quad flatpacks. LSI Logic, Milpitas, CA, (408) 433-4554, FAX (408) 433-7241. Crosscheck Technology, San Jose, CA, (408) 432-9200, FAX (408) 452-0734.—Richard A Quinnell

TWO-CHIP-MODEM IC SUPPORTS DATA, FAX COMMUNICATIONS

The two chips from Rockwell International Corp that comprise the RC9624AC can create an integrated data and fax modem. As a data modem, the chips operate at line speeds to 2400 bps and will deliver data rates to 9600 bps using V.42 bis data compression. The chips also execute error-correcting transmission protocols. Operating as a fax modem, the chips attain transmission rates as high as 9600 bps. The chip set costs $35 (10,000). Rockwell International Corp, Newport Beach, CA, (714) 833-4600, FAX (714) 833-4078.—Steven H Leibson

A/D CONVERTERS COME IN A NEW PACKAGE

Burr-Brown Corp's ADC574A and ADC774 A/D converters now come in 28-lead plastic leaded chip-carrier packages. The successive-approximation converters include a 10V reference, an internal clock, TTL-compatible 3-state output buffers, and a microprocessor interface. The converters have either 8- or 12-bit resolution, depending on external programming. The ADC574A converts 12 bits in 25 μsec max and 8 bits in 17 μsec. The ADC774's 12-bit conversion takes a maximum of 8.5 μsec and its 8-bit conversion takes 5.3 μsec. Both devices have a 150-nsec bus-access time. Missing codes are not guaranteed for either device over their 0 to 75°C specified temperature range. Versions of the ADC574 with ±1-LSB and ±1/2-LSB linearity cost $19.20 and $25.20 (OEM qty), respectively. The two linearity versions of the ADC774 cost $25.20 and $52.30, respectively. Burr-Brown Corp, Tucson, AZ, (800) 548-6132, FAX (602) 889-1510.—Anne Watson Swager

PACKET OF PAPERS DESCRIBES THE VXIBUS

You'll find a broad range of VXIbus topics covered in a packet of papers compiled by Hewlett-Packard and offered at no charge. Topics include an overview of the VXIbus, hints on applying the architecture, information on designing VXIbus instruments, and configuration hints. Hewlett-Packard Co, Palo Alto, CA, phone or fax your local office.—Steven H Leibson

REAL-TIME OPERATING SYSTEM FOR FIXED-POINT DSPs

Ready Systems's VRTX32/56000 real-time operating system works with Motorola's 56000 family of 24-bit fixed-point DSPs. The operating system provides synchronization mechanisms, priority-based scheduling, and intertask communication. Development licenses start at $6000. Production licenses start at $235 (100). Ready Systems, Sunnyvale, CA, (800) 228-1249, FAX (408) 736-3400.—Doug Conner

CIRCLE NO. 78

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lowpass, highpass, bandpass, narrowband IF

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- 5-section, 30dB/octave rolloff • VSWR less than 1.7 (typ) • meets MIL-STD-202 tests
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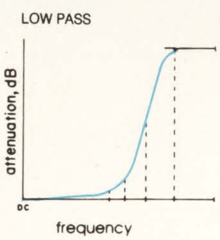
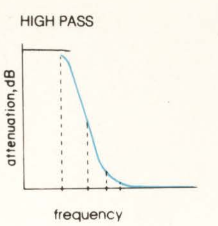
- surface-mount • over 100 off-the-shelf models • immediate delivery

low pass dc to 1200MHz



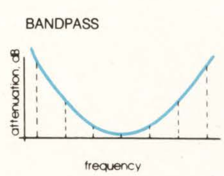
MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	(loss>40dB) Max.	Min.	VSWR pass-band typ.	stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45

high pass dc to 2500MHz



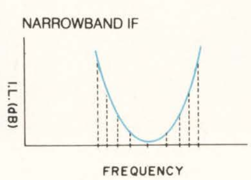
MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Min.	(loss>40dB) Min.	VSWR pass-band typ.	stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95

bandpass 20 to 70MHz



MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB) Max. F1	Min. F2	STOP BAND, MHz (loss > 10 dB) Min. F3	Max. F4	(loss > 20 dB) Min. F5	Max. F6	VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95

narrowband IF



MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	F6	STOP BAND, MHz I.L. > 35dB F7	F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

CIRCLE NO. 97

Mini-Circuits

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F132-2 REV. ORIG.

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It's really what's inside that co

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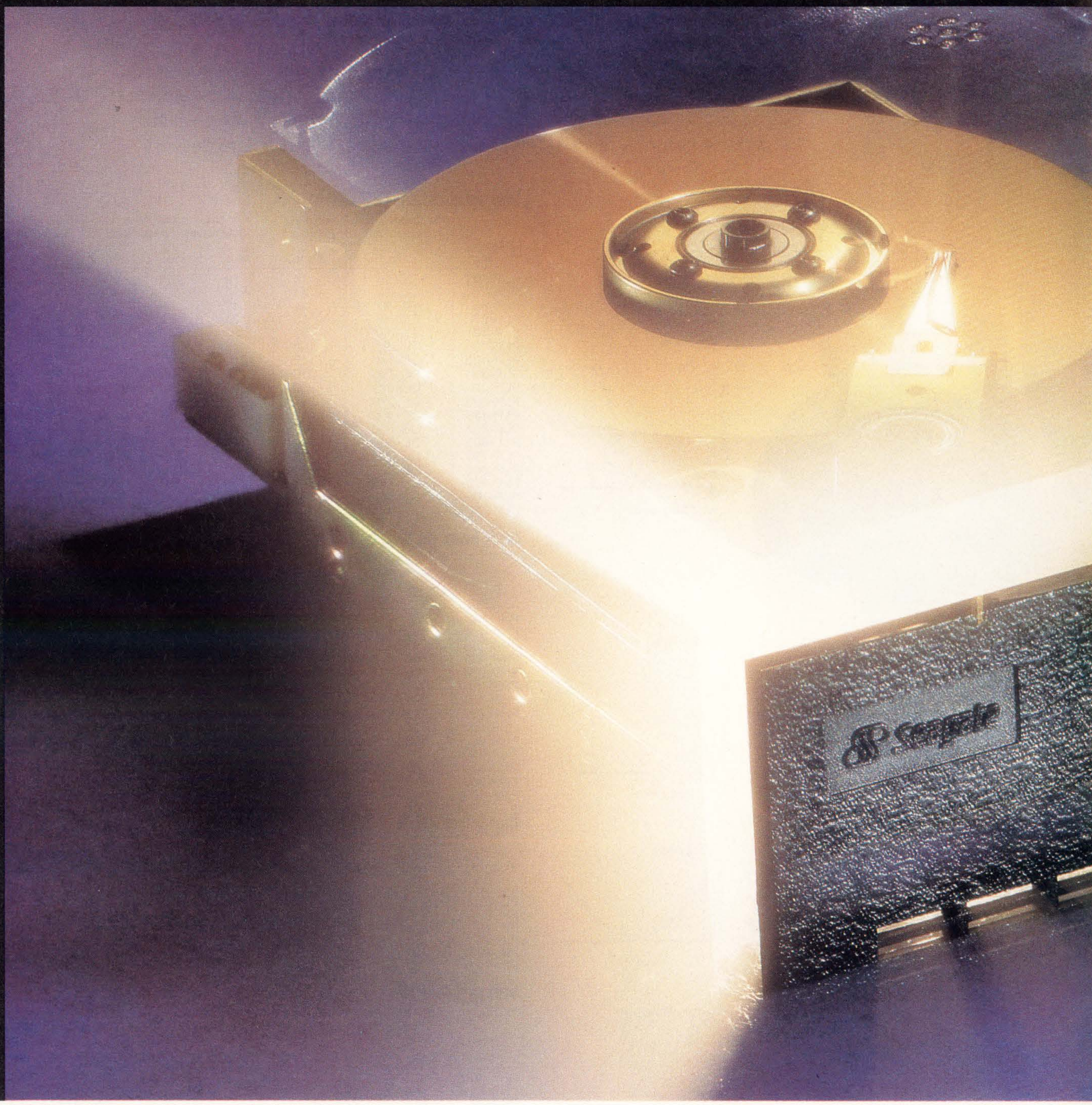

he same.
unts.

Apart from our nameplate, a Seagate disc drive looks much like any other when viewed from the outside. But it's the tangible and intangible elements we put inside that make a Seagate drive really shine.

If you could see inside you'd find the best components available. Many of them—such as discs, motors, semiconductors and thin-film heads—we design and build ourselves, allowing us to control their quality, cost and availability. Most of what we don't manufacture is obtained from a select group of vendors who must meet our strict Supplier Certification Program criteria. This guarantees consistently high quality and continual conformance to our customers' requirements.

H N O L O G Y

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The third major factor that sets Seagate drives apart is our commitment. You see it in the inspired dedication of our employees: like our engineers, who apply the latest technology advances to our current models. In our assemblers and technicians, who are committed to producing defect-free products. And in our sales, customer service and technical support groups, who continually go the extra mile to ensure complete customer satisfaction.

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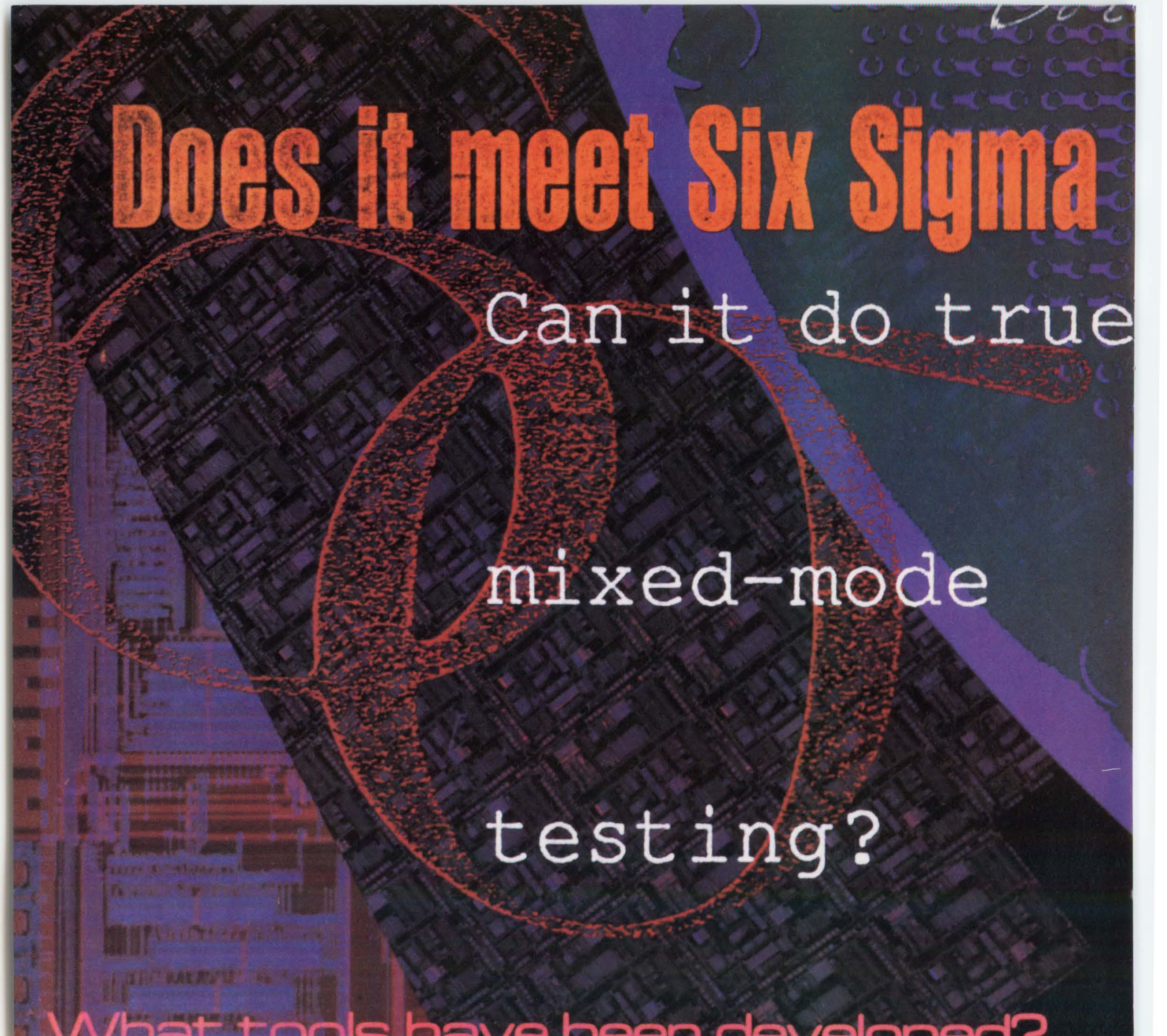
A COMMITMENT TO QUALITY Seagate

Seagate

The first name in disc drives



Before the A500 started testing Motorola's mixed-

"Motorola has adopted a Six Sigma initiative which focuses attention on approaching zero-defect performance in everything we do, including our test systems. Our purchase of the Teradyne A500 test system supports our Six Sigma initiative and our competitive leadership challenge."

Director of Marketing

Motorola knows you can't have a Six Sigma process unless you can test to Six Sigma standards. That's why Motorola's MOS Digital-Analog Integrated Circuits Division chose the Teradyne A500 Analog VLSI Test System. Because, in addition to proving the A500 could handle the complex technical requirements of Motorola's advanced ISDN interfaces, we also demonstrated that we could perform to Motorola's stringent quality levels.

"Can it do scan testing? Digitize high-frequency waveforms? Do true mixed-mode testing? Does it have a flexible architecture? Can you give us the support for a Six Sigma process? Applications expertise? Complete documentation? The right tools? In each case, Teradyne answered yes."

Manager, Advanced Test Technology

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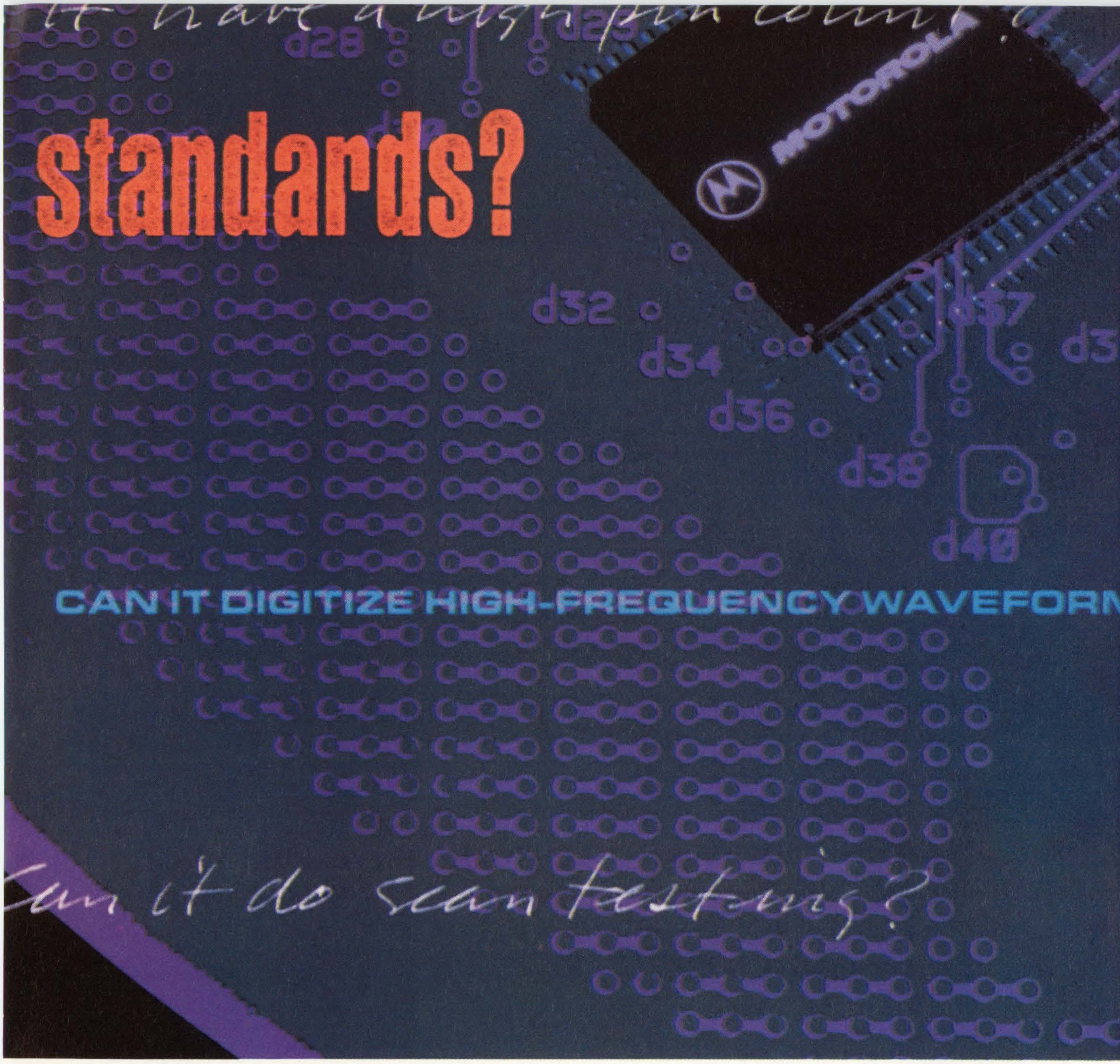


signal technology, Teradyne had to pass a few tests.

With the A500, Motorola had the ability to digitize waveforms at 20 MHz, plus the high pin count necessary to guarantee that their ISDN U-Interface worked the way it was supposed to.

Best of all, the A500's full tester simulation and powerful IMAGE™ software provided the design flexibility and rapid debugging Motorola needed to deliver defect-free parts on time.

"The A500 gave us the resources we needed, in one place, to be able to have a functioning test program very quickly – at least two to three times faster than any other test system. This type of support is just what we need to get our complex circuits, such as the U-Interface transceiver, to the marketplace ahead of the competition."

Operations Manager

To Motorola, delivering Six Sigma quality is not just a promise. It's a way of doing business. And it's a test that must be passed by suppliers as well.

To see how our A500 family of test systems can help you deliver quality, call Beth Sulak at (617) 482-2700, ext. 2746.

Or call your nearest Teradyne sales office, or write: Teradyne, Inc., 321 Harrison Ave., Boston, MA 02118.

TERADYNE

CIRCLE NO. 75

SIGNALS & NOISE

Reader swears by the Mac

Gosh, isn't it wonderful that Jon Titus has joined the 1990s (EDN, October 11, 1990, pg 49)? He has discovered that people want to be able to use a computer, not hack with it. He's all blown away to find that the PC community, with the introduction of the painfully slow Windows 3.0, is almost to the stage where Macintosh was in 1984.

One very worthwhile thing to come from the introduction of Windows 3.0 is that it has forced Apple to introduce lower-cost versions of the Mac. Note, though, that the lowest priced Mac has all the operating features of a PC with Windows, without the extra cost of a monitor, VGA card, and mouse. All these are included in the Mac price. I started using DOS-based machines and cursed the awkward interface. Then I found the Mac and have never looked back. Go for the real thing.

J Thomas Baylor, PE
San Diego, CA

(Ed Note: I would have been more impressed if Apple had made a commitment to an open bus and had encouraged more engineering and scientific applications.)

Engineers' salaries should be "professional"

There has been a lot of talk about engineers' salaries. I've always thought of an engineer as a professional that society puts in the same class as lawyers and doctors. Society believes that professionals (lawyers, doctors, and engineers) are paid the most, but this is not the case.

Perhaps the engineering profession has been stepped on through ignorance. Engineers' salaries cannot even approach lawyers' and doctors' salaries. Even some grade-school teachers with 5 years' experience are making more money than an average engineer with 5 years' experience (and engineers have to work all year long).

You'd think that the hard work that engineers do in obtaining their education and keeping up with the pace of technology would be rewarded with a generous salary. The people who design a product (and who are essentially responsible for it) should be paid the most, not a salesman who goofed off through the college years (and landed his job because of his personality).

Salesmen, in fact, can generally set their own hours and adjust their schedules as they see fit, yet they still earn a higher dollar amount through commissions and sales than the average engineer. Shouldn't the engineer who designed the features of the product get a part of this commission? Actors and singers get royalties from their work for years after—why shouldn't engineers?

I think it's time to think of the importance of attracting good engineers by rewarding them with more than just a pat on the head for a job well done.

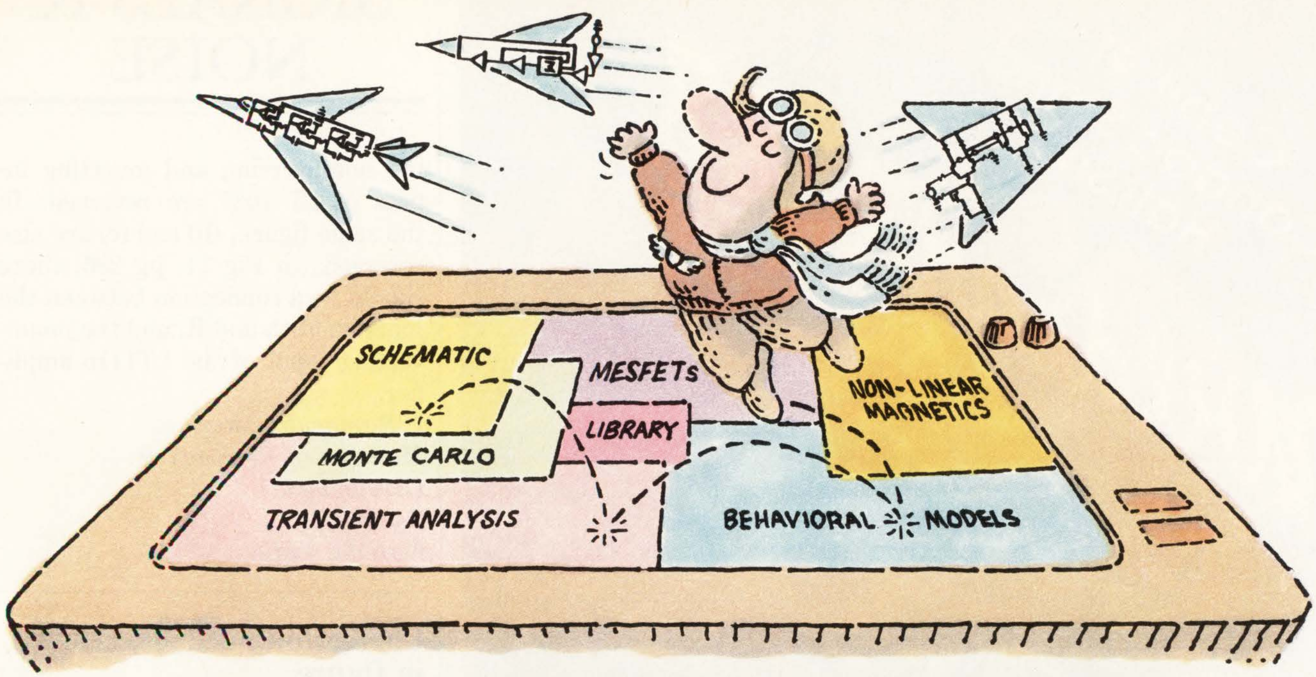
Name withheld by request
Aiken, SC

TMW also sponsors "Test Engineer" award

In Dan Strassberg's editorial "Support your local test engineer" (EDN, January 21, 1991, pg 57), he inadvertently overlooked Test & Measurement World's (TMW's) role as an ongoing co-sponsor of the Test Engineer of the Year award, along with John Fluke Mfg Co Inc. EDN, which is a sister publication of TMW magazine, apologizes for the oversight.

Reader catches errors and omissions

I'd like to bring to your notice some mistakes in illustrations for the article, "AC-driven bridge circuits suit specific applications" (EDN, November 8, 1990, pg 235). In Fig Ab,



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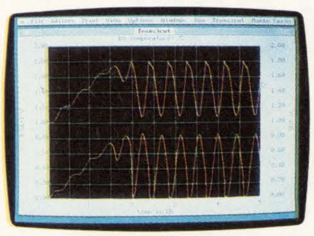
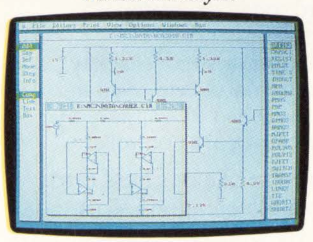
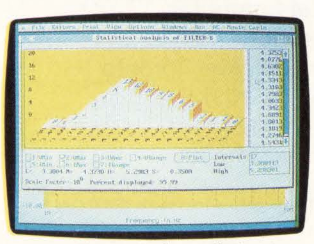


Transient analysis



Schematic editor



Monte Carlo analysis

And don't forget MICRO-CAP III's extended routine list—from impedance, Nyquist diagrams and BH plots to Monte Carlo for statistical analysis of production yield. The algebraic formula parsers for plotting virtually any function. The support for Hercules, CGA, MCGA, EGA and VGA displays. Output for plotters and laser printers.

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SIGNALS & NOISE

the noninverting and inverting inputs of LT 1037 are reversed. In the same figure, (b) and (c) are also reversed. In Fig 11, pg 236, there should be a connection between the junction of C_1 and R_1 and the noninverting input of the LT1115 amplifier.

V Ramasubramaniam
Manager of Research & Development
Systronics
Naroda, India

Correction needed in figure

I generally don't write about things in magazines, but just can't help pointing out an error in Fig A (EDN, November 8, 1990, pg 235). The pentode vacuum tubes are actually shown in (c), not (b), as indicated. Maybe it was the use of the tube symbol that caught my eye.

Robert A Judd
Design Engineer
Watlow Controls
Winona, MN

IT'S EASY TO HAVE YOUR SAY

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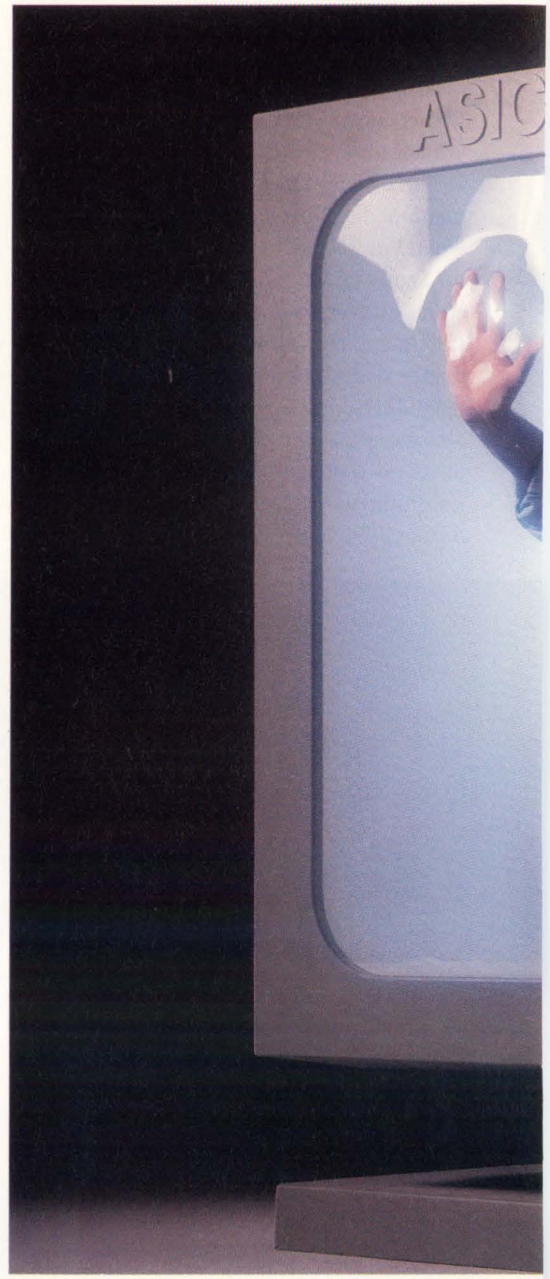

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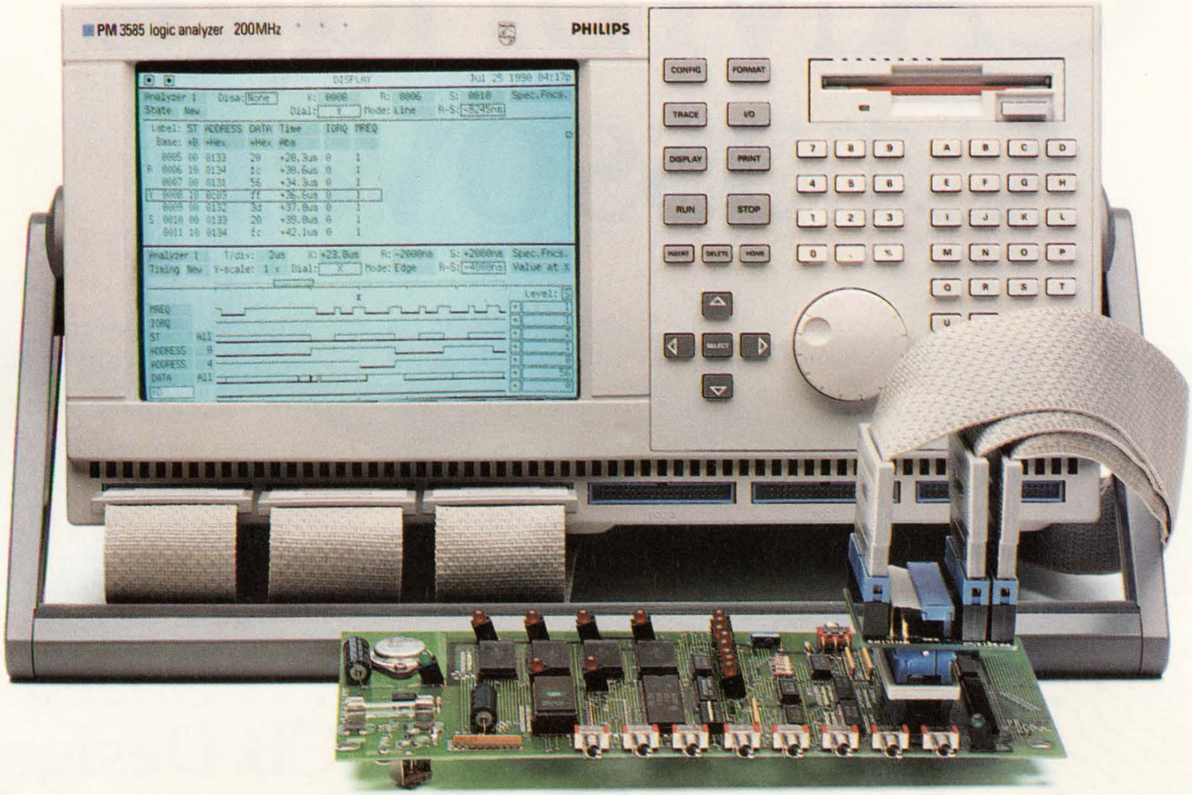

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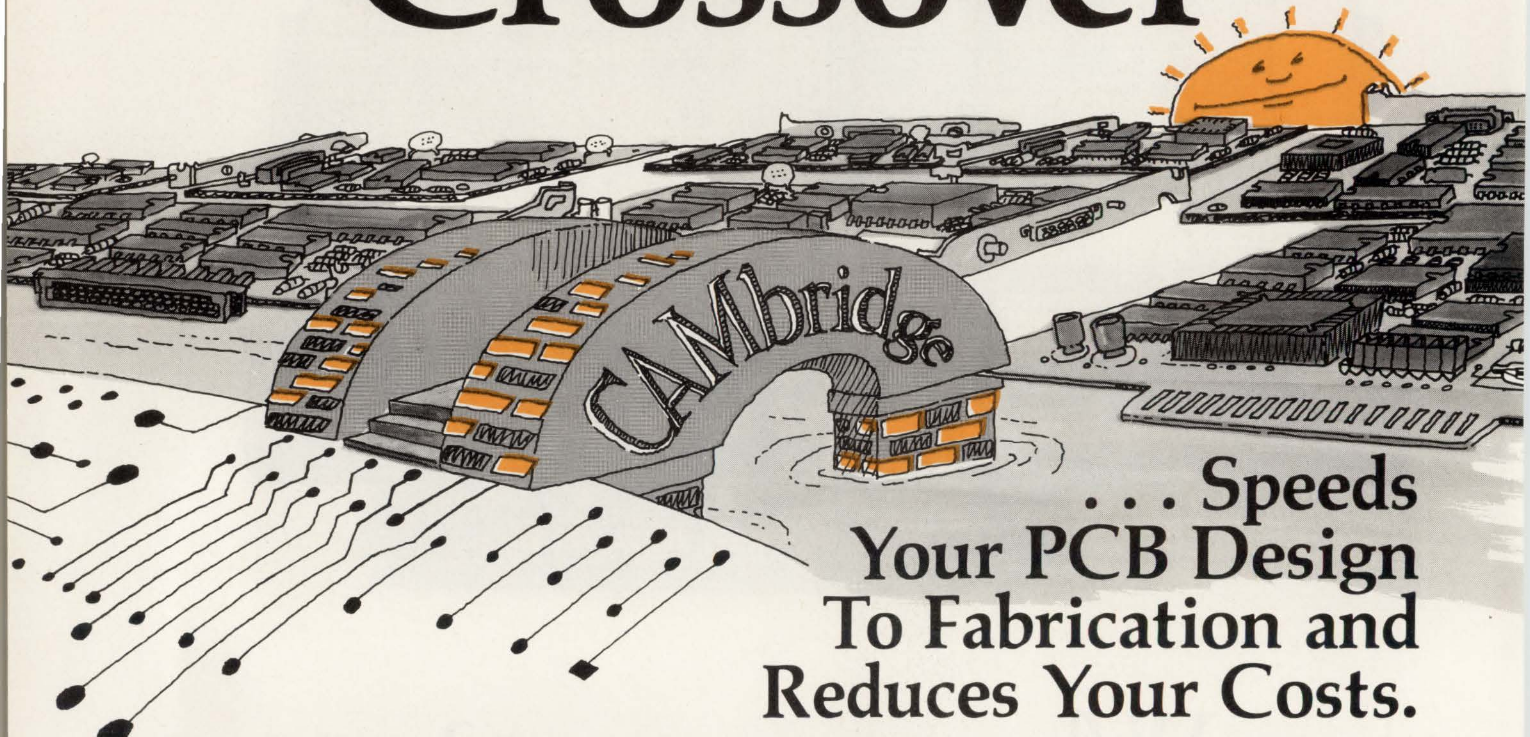

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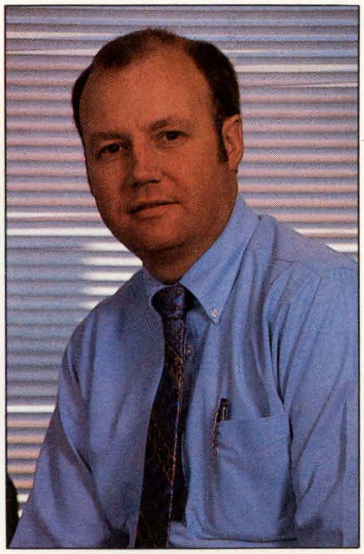
Smart weapons, smart lessons



As a member of the electronics industry, I'm particularly pleased that intelligent weapons such as the Tomahawk cruise missile, Patriot air-defense missile, and laser-guided bombs worked well at the start of the UN-coalition war against Iraq. For years, many of these smart weapons have been under scrutiny in the US Congress and the Pentagon. Unfortunately, few legislators have an engineer's perspective on thorough design or test. Congress should be on the lookout for weapons that are poorly designed and tested. Following, I've listed a few guidelines that might help. There are some lessons for all of us here:

1. Test your product under realistic and uncontrived conditions. Have disinterested people test it. Several extremely complex military weapons such as the Aegis cruisers have yet to be tested under realistically simulated battle conditions. Testing some systems involves "practice tests" that let the testers predict a system's expected performance. These test simulations are bogus, yet this testing mentality often prevails in the military. *Engineers never say, "Hey, if it works in this lab, it will work anywhere. After all, they're not going to give one of these to just any maintenance jockey."*

2. Adapt off-the-shelf products with care. They're not necessarily adaptable to all designs. When the US Army designed the Sgt York division air-defense (DIVAD) system several years ago, it specified many off-the-shelf electronic systems. Despite the fact that some of the off-the-shelf radar equipment was originally used in aircraft, it was thought that using it in the DIVAD system would save money and avoid the time needed for a new design. Unfortunately, the off-the-shelf equipment wasn't suitable for the tasks at hand. *An engineering manager would never say, "It took a lot of money to design the custom-built power supply in our El-Cheapo clone computers, so it'll work in our new line of medical instruments, too."*

3. Don't try to duplicate your competitors' successes. The DIVAD system essentially mimicked the Soviet Union's older ZSU-23/4 air-defense system which *was* effective years ago in Middle East combat. Times change and so do aircraft characteristics. However, as the US military designed the DIVAD system, it could never keep up with advancing aircraft maneuverability, thus defeating the system. Luckily it was canceled. *Engineers are too smart to be taken in by, "This idea will make your company into the next Apple Computer..."*

4. Put money in your budget to give your managers and sales people realistic training. Many weapons are so expensive that the troops that control them almost never have the opportunity to test fire them—even under controlled conditions. One Army outfit I knew of sponsored an annual competition to see which *one* gunner got to fire an antitank missile. *An engineering-group leader would never say, "Ok, ok, we'll send one engineer for an afternoon course on the new 250-MHz logic analyzer, then at lunch she can tell the rest of you how to use it."*

5. Don't needlessly endanger the people who use your product. Few of us would consider putting a 1000V power-supply contact on the front panel of a tester or exposing people to other avoidable hazards. I pity the troops who fire the US's TOW antitank missiles. The soldiers must remain exposed from the time they sight the missile on a target until the missile reaches its target. The blast from launching a TOW missile is a glaring target for enemy gunners. Our NATO allies have a more effective antitank system that protects the gunners. After all, if they miss their targets, they should be alive to try again. *As engineers, we've never heard, "No one would ever be stupid enough to put a screwdriver in . . . ZAP."*

Jon Titus
Editor

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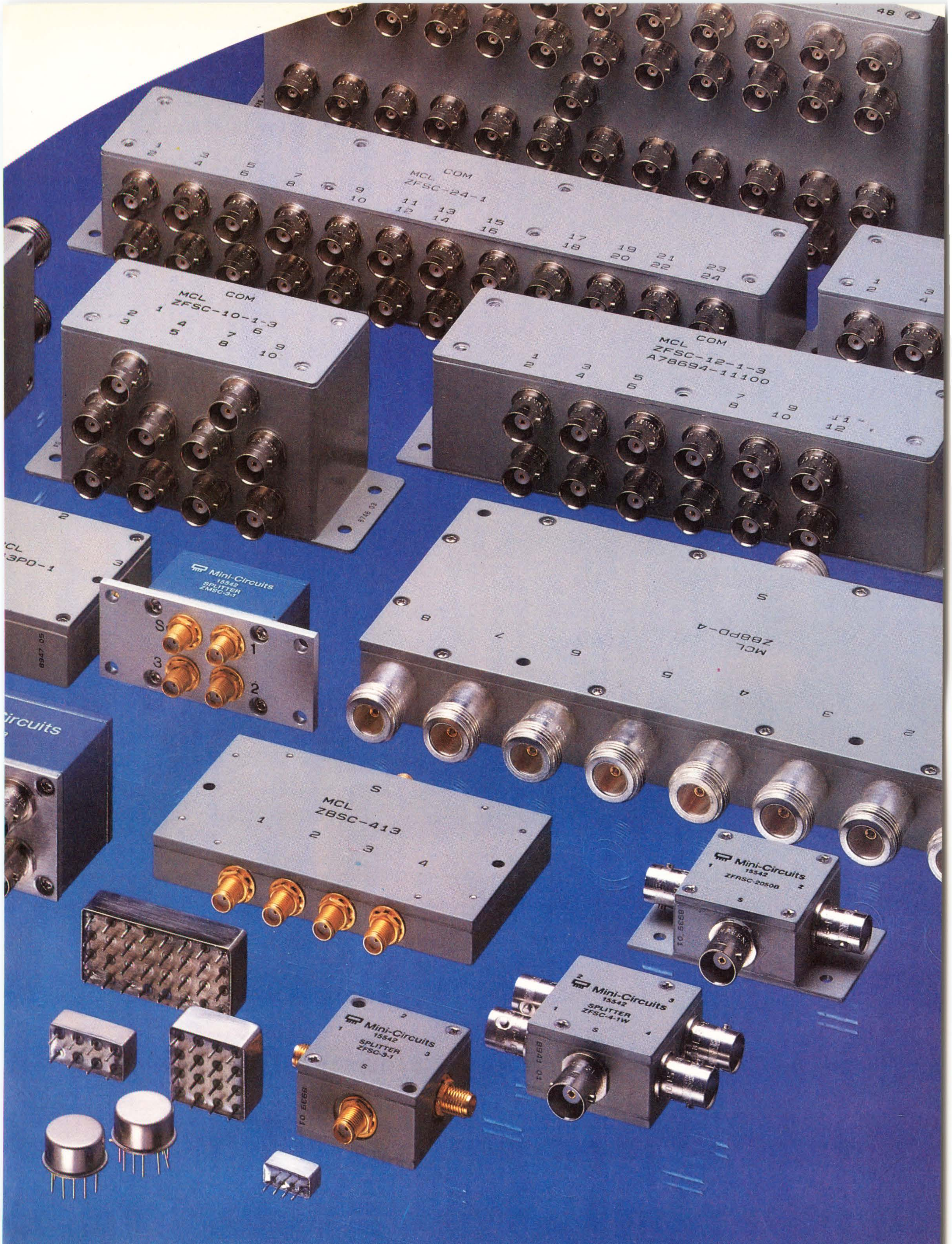

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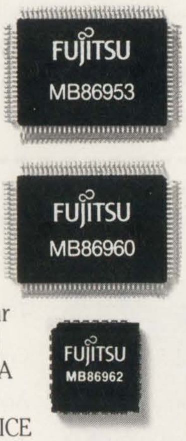

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CACHE-COHERENCY PROTOCOLS

Protocols keep data consistent

Maintaining data consistency in numerous cache RAMs operating on a shared-memory bus can give a system designer a headache. Some well-defined cache-coherency protocols can keep these headaches from becoming migraines.

John Gallant,
Associate Editor

Interconnecting multiple processors on a shared-memory bus poses the problem of cache coherency. Because any self-respecting processor has its own cache memory these days, the designer must ensure that multiple caches and the global memory residing on the same bus have a common perception of the data at a particular memory location. This issue has spawned a variety of hardware-based schemes to maintain consistent data when more than one processor requires access to the same database. These schemes include the write-through, MOESI, MESI, and central-directory cache-coherency protocols.

IBM introduced the cache memory in the 3070 mainframe computer in 1973. A cache is much smaller and faster than main memory and temporarily holds replicas of certain main-memory addresses. Caches are essentially a compromise way of obtaining an inexpensive zero-wait-state memory when the main memory is slower than the CPU. Since 1973, μP design has concentrated on attaining faster operating speeds; dynamic-RAM design has concentrated primarily on achieving higher densities.

Because the speed gap between the μP and main memory continues to widen, a local cache RAM has become practically a necessity in high-performance systems. In fact, many highly integrated μPs, such as Motorola's 68030 and 68040 and Intel's 80486 and i860, incorporate a cache controller and a cache RAM on chip.

A cache miss causes problems

Fig 1 shows a typical multiprocessor system that is tightly coupled to a shared global memory via a high-speed bus. Most of the time, each CPU operates on the data in its local cache. How-

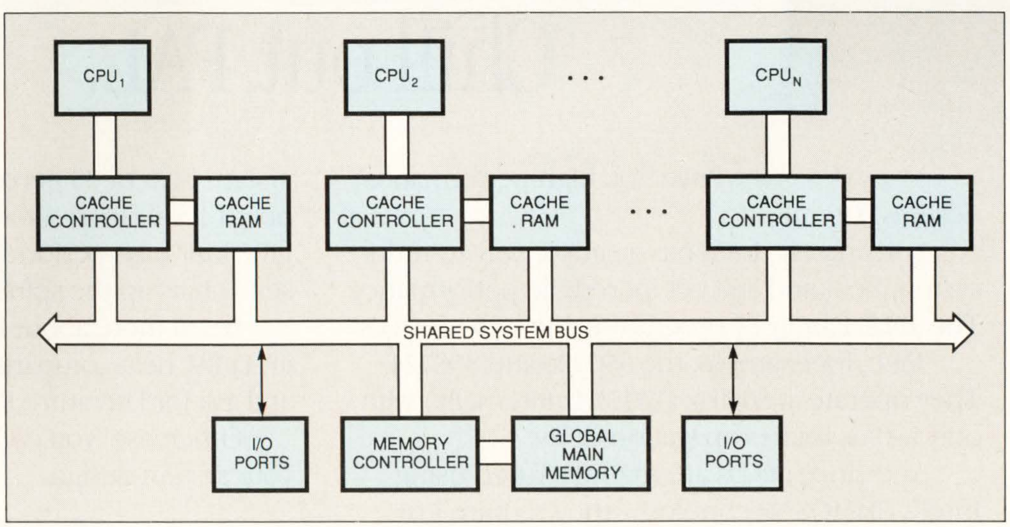
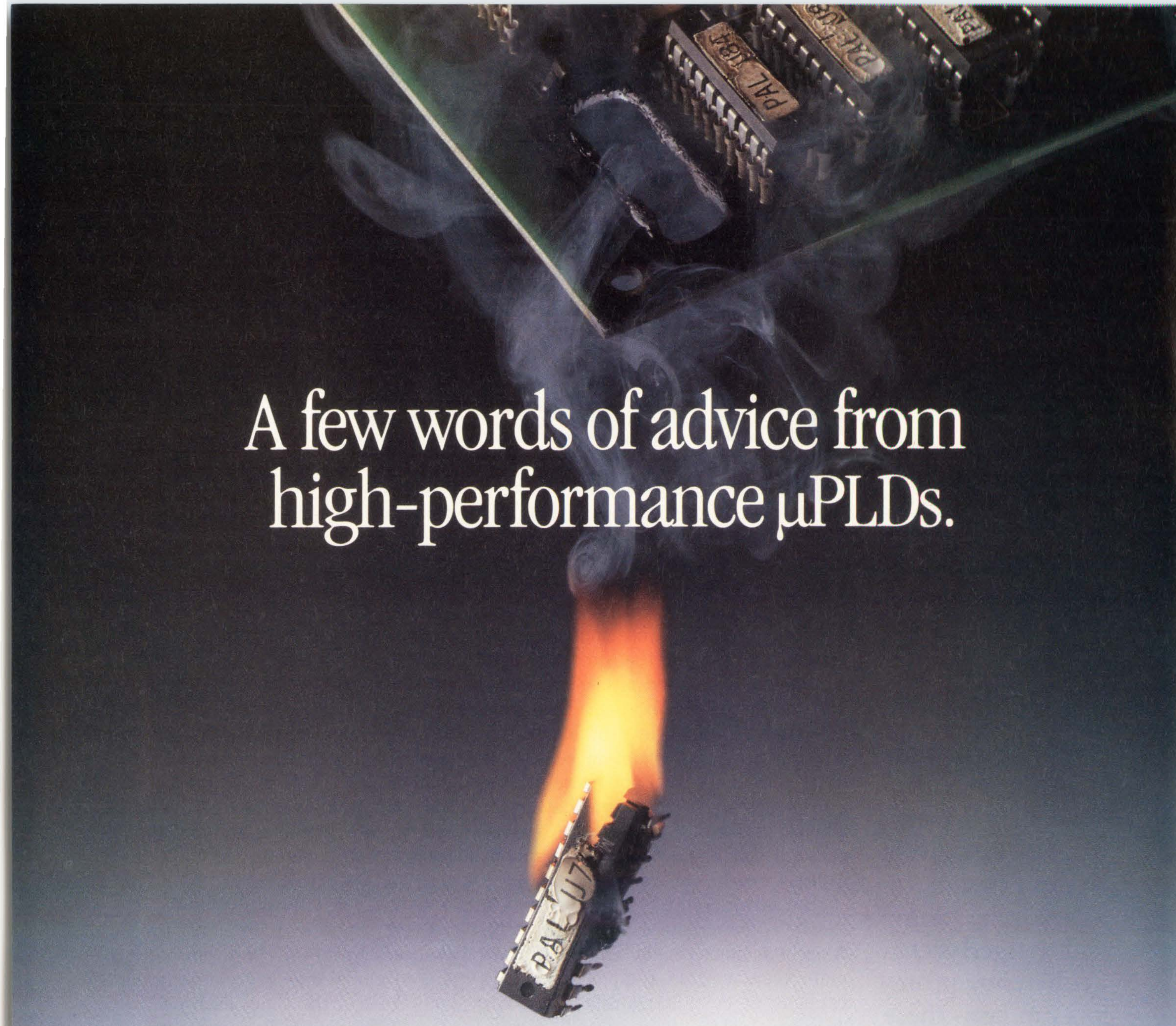


***Fig 1—A tightly coupled multiprocessor connects n CPUs** and their local cache RAMs to the global main memory via a wide-bandwidth system bus.*



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ever, when a CPU attempts a read or a write to an address that isn't in its local cache—an occurrence called a cache miss—the CPU's arbitration logic must arbitrate for control of the bus so the cache RAM can access the data from the main memory.

A problem arises when several copies of the data at that address exist in the local caches of different CPUs at the same time. Because any CPU can modify the data in its local cache RAM, the main memory may not contain the most up-to-date copy of the data. A trivial method of ensuring that the requesting CPU obtains the most-recent data is to have sections of memory that more than one CPU share reside in main memory only—not in any of the local caches. Although implementing this method is simple, system designers generally don't employ the method because it results in inefficient multiprocessing.

A write-through cache-coherency protocol is also relatively simple to implement but can be effective when only a few medium-performance CPUs, such as 68010 or 80286 μPs, are on a wide-bandwidth bus. Note that in this article, a policy refers to the method a cache controller employs to update main memory whenever the CPU modifies data in the local cache RAM. A protocol refers to a procedure a system uses to maintain consistent data in the caches and the main memory. Note also that there are both a write-through policy and a write-through protocol.

The write-through protocol requires that the cache controller assign a 1-bit attribute to each line in its local cache RAM. A line is a block of data having contiguous addresses; the attribute identifies whether the line is valid or invalid. If a line is valid, a CPU can read or write to that line; if a line is invalid, the CPU must access the main memory.

In the write-through policy, which works in conjunction with the write-through protocol, the cache controller transfers a line to its local cache RAM from main memory whenever a cache miss occurs on a read operation. A cache controller updates its local cache on a valid cache hit and the main memory every time a CPU issues a write command. The memory controller queues the write requests, which lets the CPU continue without waiting for the end of the write cycle.

For the write-through protocol to work, each cache controller must monitor the address bus whenever a CPU writes to main memory. If the cache controller determines that the write address corresponds to an address in its local cache RAM, the controller must invalidate the line containing that address. Thus, only the cache RAM containing a line with a valid attribute and the main memory contain up-to-date copies of the data. A cache with an invalid line must access main memory to obtain a valid copy of the data.

Because the write-through policy generates lots of bus traffic, a system bus using the write-through protocol can easily become saturated when multiple high-performance μPs share a memory bus with-

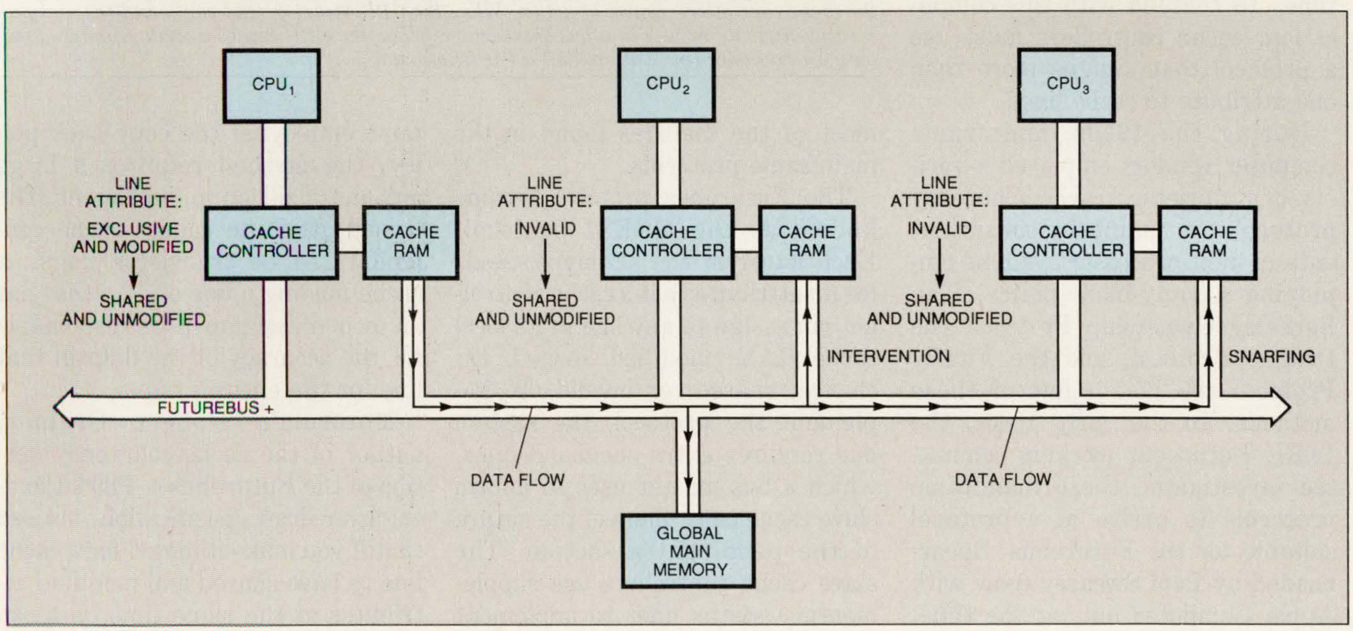

Fig 2—The Futurebus+ MESI protocols minimize system bus traffic. *Here, CPU_2 issues a read to an invalid line in its local cache. Because CPU_1's local cache has an exclusive and modified copy of the line, CPU_1 intervenes in the transaction. At the same time, CPU_3's cache snarfs the data to obtain a shared and unmodified copy of the line.*

Cache-coherency protocols

out sufficient bandwidth. In fact, the 40M-byte/sec VMEbus, which can implement the write-through protocol using its location monitor, saturates when just two 68030s having 64k-byte second-level local cache RAMs have common access to the bus's main memory, according to Motorola's Robert Greiner.

Cache controllers that implement a copy-back policy can significantly reduce bus traffic in a multiprocessor system. In the copy-back policy (also known as the write-back policy), a CPU writes only to its local cache RAM and not to the main memory, unless the cache is full. The controller flags the modified data in the cache RAM as dirty. The controller updates the main memory when it replaces a line in the cache RAM because of a read miss.

Although the copy-back policy reduces bus traffic, it complicates the cache-coherency issue. Because any CPU can write data into its local cache RAM without informing the system, many modified copies of the data can exist at any particular time. To contend with this complication, cache controllers must use a protocol that assigns more than one attribute to cache lines.

During the 1970s, mainframe computer vendors employed a variety of proprietary cache-coherency protocols to maintain consistent data in multiprocessor systems employing a copy-back policy. The Berkeley Ownership Protocol, the Dragon Protocol, and the Firefly Protocol are just a few of these methods. In the early 1980s, the IEEE Futurebus working committee investigated these mainframe protocols to arrive at a protocol suitable for the Futurebus. Spearheaded by Paul Sweazey (now with Apple Computer but, at the time, with National Semiconductor), the committee defined an open cache-coherency protocol that contains

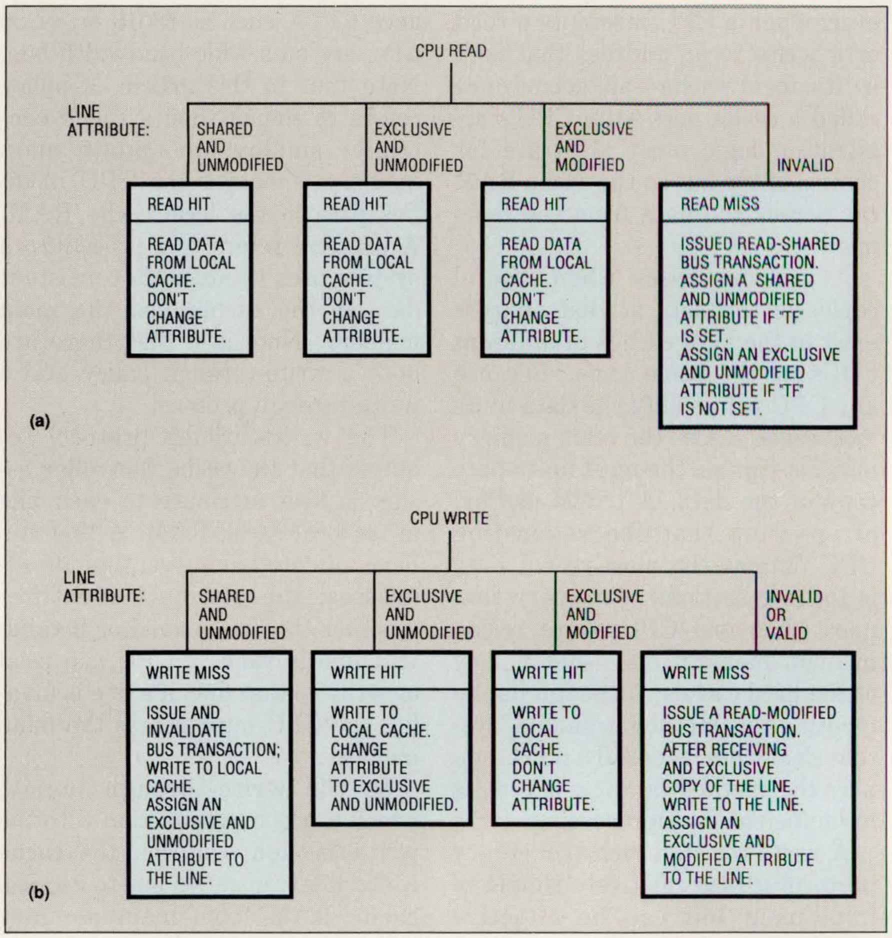

Fig 3—In the Futurebus+ implementation of the MESI protocol, *line attributes determine the cache controllers' course of action. When the CPU issues a read command* ***(a)****, only an invalid attribute results in a bus transaction. When the CPU issues a write command* ***(b)****, only an exclusive line can prohibit a bus transaction.*

most of the features found in the mainframe protocols.

The Futurebus protocol became known as the MOESI protocol. Each letter in the acronym stands for an attribute that a cache controller can assign to any line in its local cache RAM: modified, owned, exclusive, shared, or invalid. To implement the protocol, the system bus requires extra command lines, which a bus master uses to inform slave cache controllers of the nature of the pending transaction. The slave cache controllers use supplementary status lines to implement the protocol.

Although the MOESI protocol guarantees data consistency in systems employing the copy-back policy, the method requires a large amount of silicon to implement. The owned attribute causes cache controllers to be transistor hogs. A cache holding a line of data that has an owned assignment is responsible for the accuracy of the data in that line for the entire system.

Motorola's Robert Greiner, author of the cache-coherency section of the Futurebus+ P896.1 logical-layer draft specification, noticed that if you make it illegal for a cache line to have shared and modified attributes at the same time, you can eliminate the owned attribute from the MOESI protocol. The shared attribute indicates that another cache

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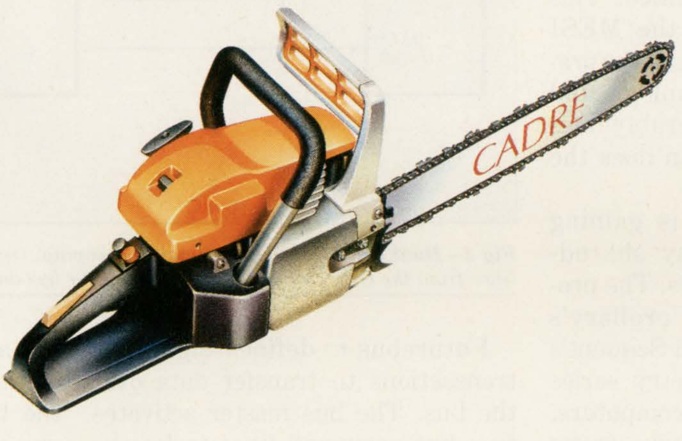

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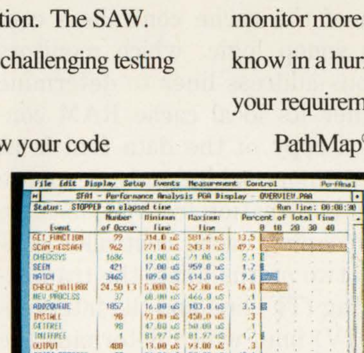

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on the bus shares a copy of the line; the modified attribute indicates that the cache line supersedes the copy in main memory because the local CPU has written data to the line.

Essentially, a slight change to the MOESI protocol makes a line having a shared attribute valid only when the line is unmodified. This modification results in the MESI protocol, which the current Futurebus+ specification employs and which requires considerably less silicon to implement than does the MOESI protocol.

The MESI protocol is gaining popularity among many shared-memory system designers. The protocol is employed in Corollary's (Irvine, CA) 486/smp and Sequent's (Beaverton, OR) Symmetry series of shared-memory bus computers. The IEEE Nubus working group has submitted a draft specification for sponsor ballot that supports the MESI protocol. The revised Nubus standard, known as Nubus90, defines three new command lines and a status line to realize the protocol. The Nubus MESI protocol supports cache line sizes of 4, 8, 16, 32, and 64 bytes.

Although many ways to implement the MESI protocol exist, exploring the Futurebus+ implementation is possible because Futurebus+ is an open architecture. Each cache controller on the bus assigns a 2-bit attribute to each line in its local cache RAM. The attribute indicates whether the line is valid or invalid, shared and unmodified, exclusive and unmodified, or exclusive and modified. An exclusive attribute means that no other cache RAM has a copy of the line; a shared attribute means that another cache RAM has a copy of the line. The local CPU can read a valid line privately. A modified line must always be exclusive, and an exclusive line is always valid.

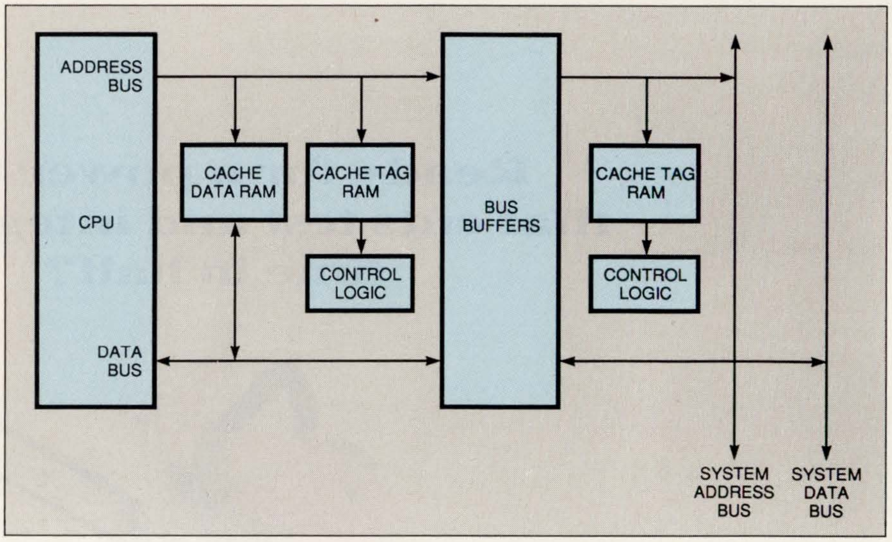

Fig 4—Dual cache-tag RAMs simplify snooping. *One of the RAMs can snoop the address lines from the CPU, while the other snoops the bus address lines.*

Futurebus+ defines eight bus transactions to transfer data over the bus. The bus master activates four bus command lines to let the other cache controllers, or slaves, know which of the eight possible transactions is about to occur. The master informs the other bus modules of the affected memory address by activating the bus address lines. Each of the cache controllers contains snoop logic, which monitors the bus address lines to determine whether its local cache RAM contains a copy of the data that is at that memory address. In response to the information from the master, the snooping cache controller activates two status lines, the transaction-flag (TF) line and the intervention (IV) line, which determine the action of the master and the slaves during the transaction.

A slave's snoop controller activates the wire-ORed TF status line when its local cache has a shared copy of the data. A slave's snoop controller activates the IV status line when the slave wishes to intervene in a transaction. A slave must intervene in a transaction if the master is attempting a read from the shared memory, and the slave has an exclusive and modified copy of the data. This intervention lets the bus transfer a valid line from one cache to another.

Snoop before snarfing

Futurebus+ permits any cache controller or the memory controller to capture a copy of a line when other modules on the bus are exchanging that line during a transaction. The controller captures the data—an action called snarfing—by converting the transaction to a broadcast operation. Snarfing conserves bus traffic by preventing the controller from initiating a redundant bus transaction to get the same data. When a cache controller snarfs a line, it assigns a shared and unmodified attribute to that line in its local cache RAM, as **Fig 2** shows. Note that after any bus transaction, the local cache controller must reassign attributes to the affected line.

You can implement the MESI protocol using only four of the eight Futurebus+ transactions: read shared, read modified, invalidate, and copy back. When a CPU issues a read to an address in a line that has a shared and unmodified, exclu-

sive and unmodified, or exclusive and modified cache attribute, the operation is a read hit, and no bus transaction is necessary **(Fig 3a)**.

However, if the line has an invalid attribute, the operation is a read miss, and the CPU arbitrates for the bus to issue a read-shared transaction. If a second controller sets the TF status line, the CPU's controller assigns a shared and unmodified attribute to the cache line after its local cache RAM receives a copy of the data from the bus. If the TF status line isn't set, the cache controller assigns an exclusive unmodified attribute to the line.

When a CPU issues a write command to an address in a line that has an exclusive attribute, the operation is a write hit, and no bus transaction is necessary **(Fig 3b)**. If the line isn't exclusive, the operation is a write miss—even if the line is valid. If the CPU's cache RAM has a copy of the data in a shared and unmodified line, the local cache controller writes to the cache RAM and assigns an exclusive and modified attribute to the line. The controller must then issue an invalidate bus transaction. When the other cache controllers detect the invalidate bus transaction, they must assign an invalid attribute to their copies of the line.

If a write miss occurs and the local cache RAM doesn't contain a copy of the data in a shared and unmodified line, the CPU's controller issues a read-modified transaction. The read-modified transaction lets the requesting cache controller obtain an exclusive copy of the line in order to modify it. The controller's cache RAM can obtain the line from either an intervening cache controller's cache RAM or the main memory. Other cache controllers must invalidate shared copies of the line. Once the requesting controller's cache RAM receives the exclusive line, the local CPU writes to the line, and the controller assigns an exclusive and modified attribute to it.

The MESI protocol allows a cache controller to use a transaction to allocate empty space in its cache RAM to service cache misses. The controller can flush a line in its cache RAM that is not exclusive and modified. If the line is exclusive and modified, the cache controller must transfer it to main memory before the location can be reused.

You can't currently buy any silicon that implements the MESI protocol.

A cache controller also uses a bus transaction when data must be restored in main memory. **Ref 2** contains a more detailed description of all the Futurebus+ transactions as well as some concrete examples of the MESI protocol in action.

Although the MESI protocol is gaining adherents as the cache-coherency protocol for shared-memory bus systems, you can't currently buy any silicon that implements the technique. However, a number of chip vendors are actively developing chip sets for this purpose. Texas Instruments (Dallas, TX) is developing a chip set that will implement the Futurebus+ version of the MESI protocol, and S-MOS (San Jose, CA) is developing silicon that will integrate the cache-controller and memory-controller functions on a single chip.

Because on-chip cache controllers in today's highly integrated μPs only execute a write-through policy, designers place a second cache between the system bus and the CPU when employing these μPs in a shared-memory bus system. The on-chip cache is called the primary cache; the off-chip cache is called the secondary cache. The secondary cache translates the primary cache's write-through policy to a copy-back policy to use the MESI protocols on the system bus.

Systems employing this hierarchical caching scheme often incorporate a rule called the principle of inclusion. The principle of inclusion always requires the secondary cache RAM to have a superset of the data in the primary cache RAM. You implement the principle of inclusion using two basic precepts:

1. Any data the cache controller writes into the primary cache RAM, it must also write into the secondary cache RAM.
2. Any data the cache controller removes from the secondary cache RAM it must also force out of the primary cache RAM.

The principle of inclusion lets the secondary cache screen invalidation transactions on the system bus and thereby limit the number of invalidation transactions sent to the primary cache controller. Because the CPU must stop during an invalidation cycle, this screening reduces the number of unnecessary CPU wait states.

Two tags are better that one

Snooping cache controllers, such as those that implement the MESI protocol, often use dual cache-tag RAMs for each CPU to determine whether a memory location resides in the local cache **(Fig 4)**. The cache-tag RAM contains the upper address bits, or tags, for each stored location as well as a com-

parator that matches the upper address bits of a pending transaction to signal a cache hit. A single cache-tag RAM would require a multiplexer to switch between tags generated by the CPU and tags on the system bus. By employing dual cache-tag RAMs—one that snoops the tags from the local CPU and one that snoops the tags on the system bus—matching tags is faster.

Although snooping bus schemes such as the MESI protocol are popular in shared-memory bus systems, they aren't the only way to maintain cache coherency. For example, in a central-directory technique, the memory controller maintains tables that contain critical information on the status of each cache in the system.

Chips and Technologies Inc (San Jose, CA) employs this technique in the M/PAX chip set, which can maintain data consistency for as many as six cache RAMs. A central data-coherency unit invalidates lines that contain shared data when a cache controller requests exclusive ownership of a line. The unit also transfers ownership of a line when another cache controller requests an exclusive copy. Because the central-directory technique doesn't require snooping or cross interrogation between cache controllers, it simplifies the implementation of hierarchical bus structures.

Maintaining cache coherency on a shared-memory system bus of any sort is a complex issue. Implementing a write-through cache-coherency protocol is relatively easy, but the protocol is only effective when the system bus has sufficient bandwidth to handle the traffic that more than one CPU generates. Today's faster CPUs, however, are pushing the bandwidth limits of system buses. Snooping protocols based on a copy-back policy, such as the MESI protocol, are gaining adherents to preserve available bandwidth.

Hierarchical bus structures that have caches on more than one bus present further difficulties. Because a central-directory protocol eliminates cross interrogation between caches, it can simplify matters. However, directory-based schemes require lots of silicon to maintain status tables for every cache in the system. Perhaps a combination of a snooping protocol and a directory protocol is a compromise solution for hierarchical bus structures.

Some board vendors circumvent the problem of cache coherency by creating a cluster of multiprocessing CPUs on a single bus module. The module usually contains two to four CPUs, each operating from its own local cache, and a large portion of main memory. A cache-coherency protocol is only necessary for the cluster, so the module can communicate with the system bus via a dual-port RAM. EDN

Acknowledgments

Although the author takes responsibility for the accuracy of this article, he is grateful to Motorola's Robert Greiner, Intel's John Hyde, and Integrated Device Technology's Jim Handy for their helpful comments and suggestions in its preparation.

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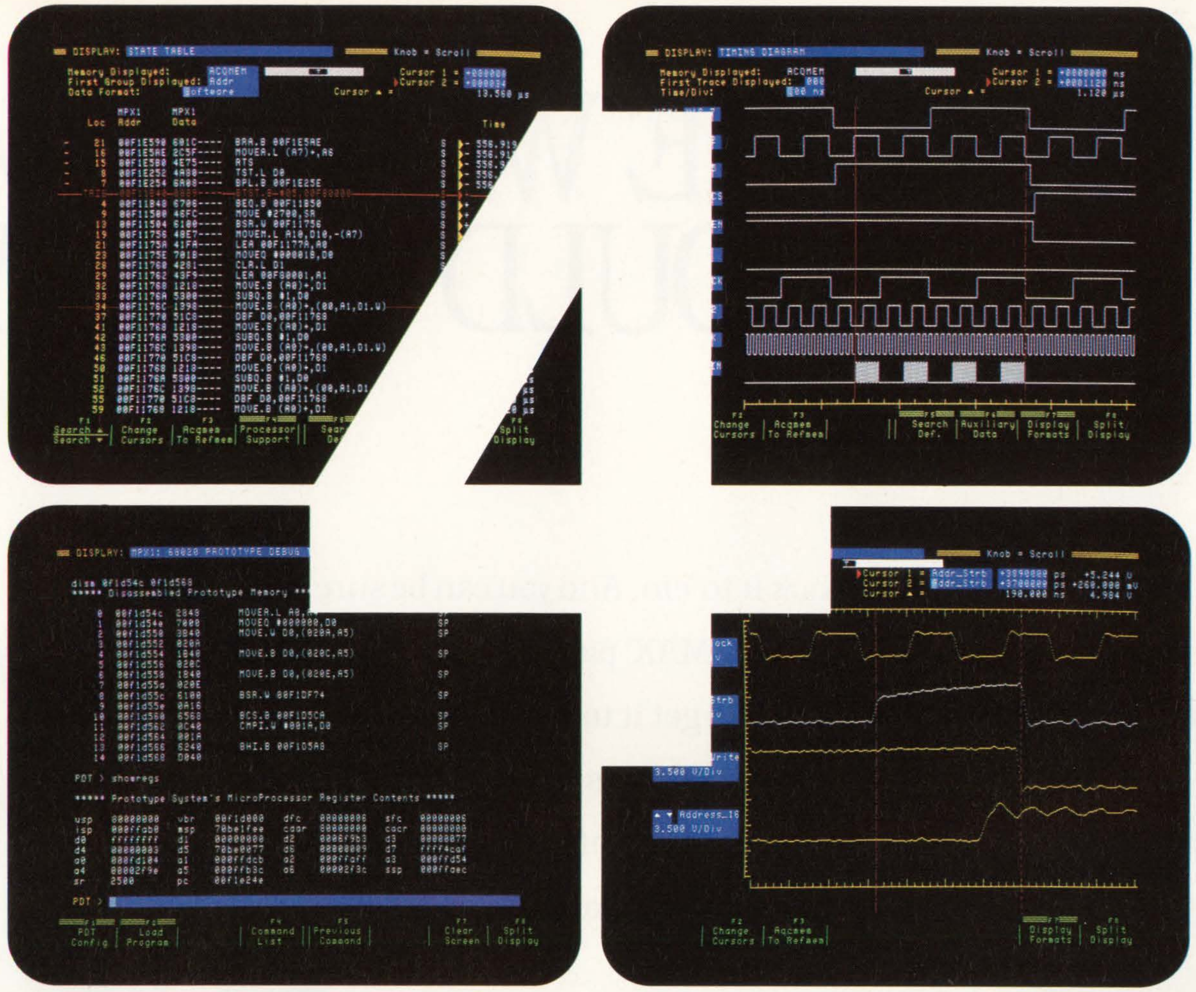

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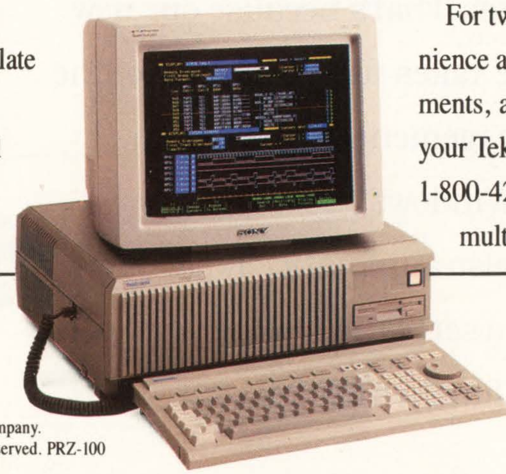

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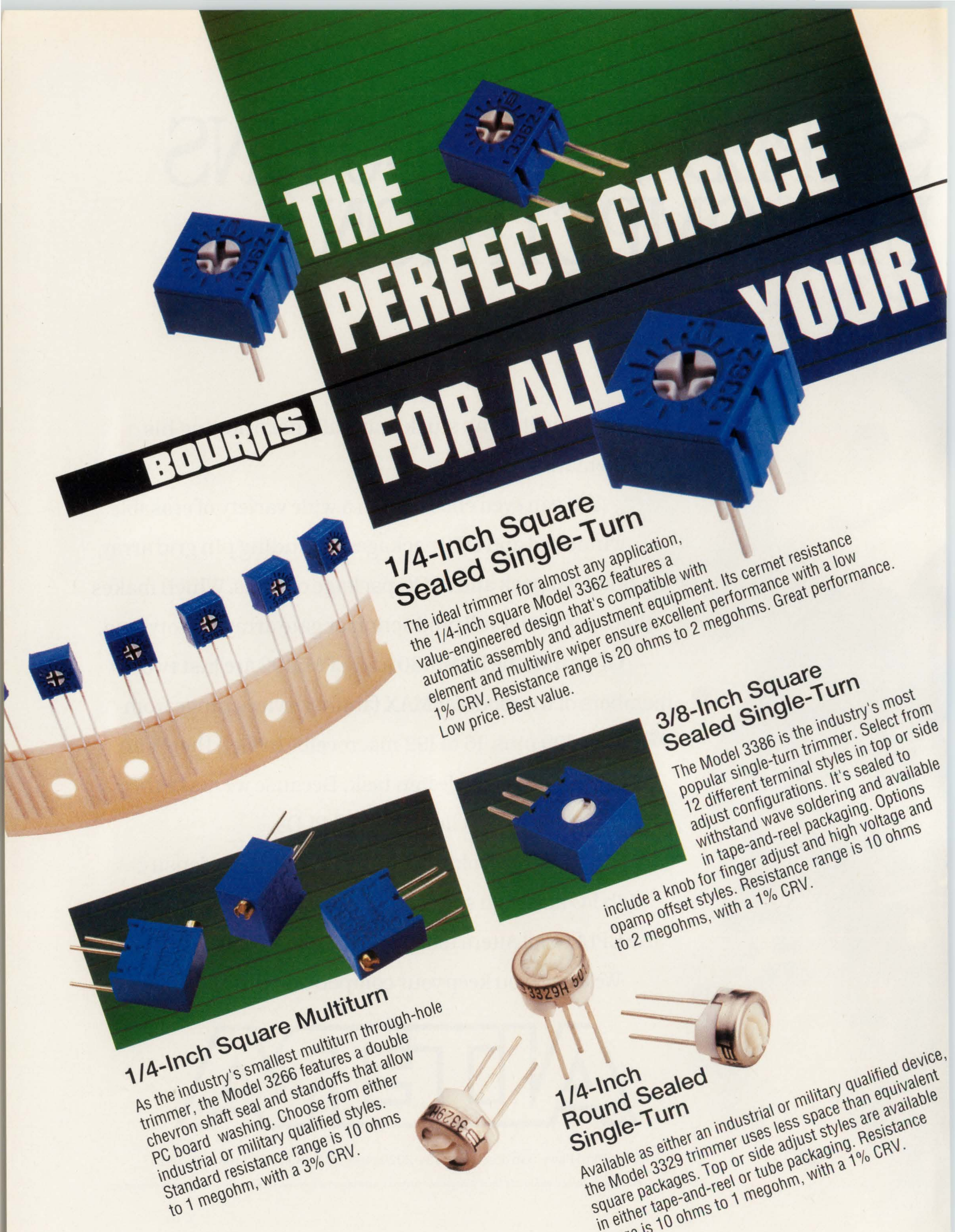
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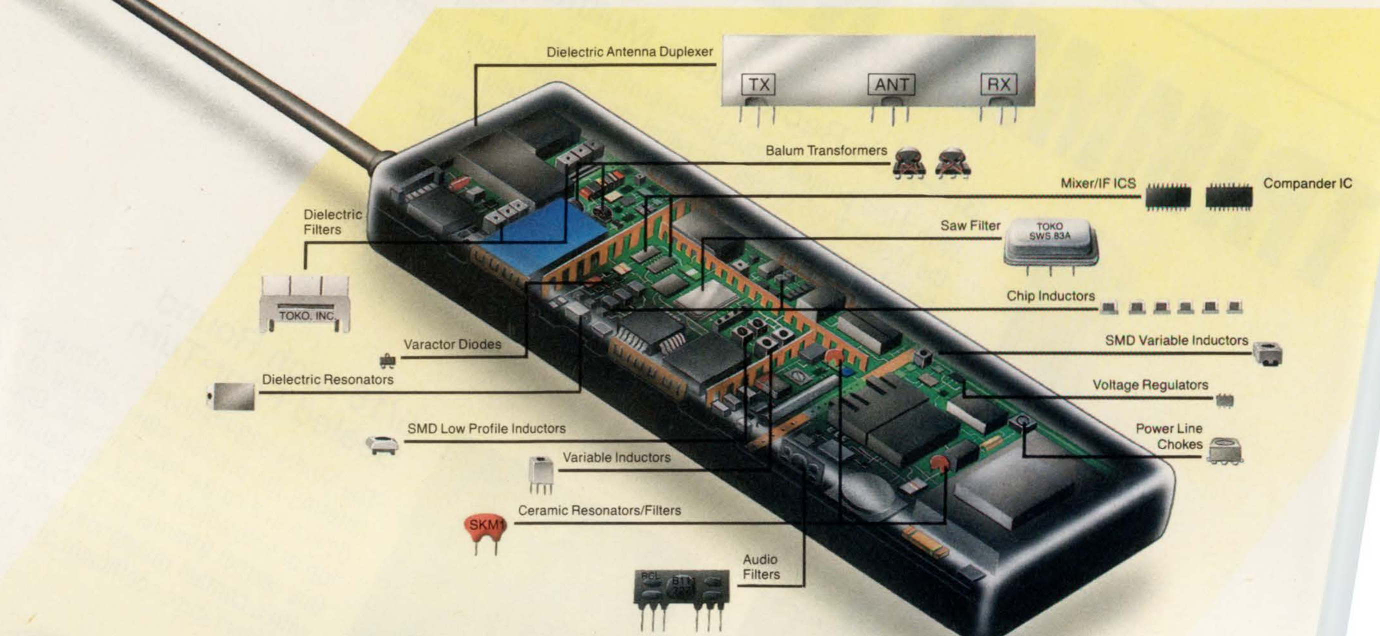

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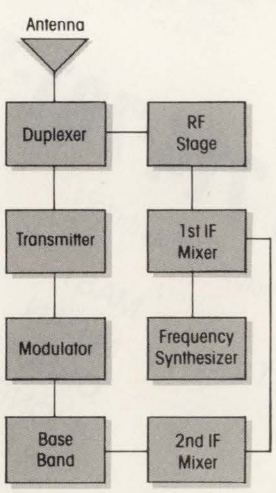

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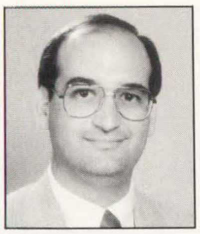
CONTACT-ENHANCING CHEMICALS

Fluids vanquish intermittent contacts



Chemicals that improve connector performance may sound more like patent medicines than serious products, but you can obtain remarkable improvements in reliability and performance with a few strategic drops.

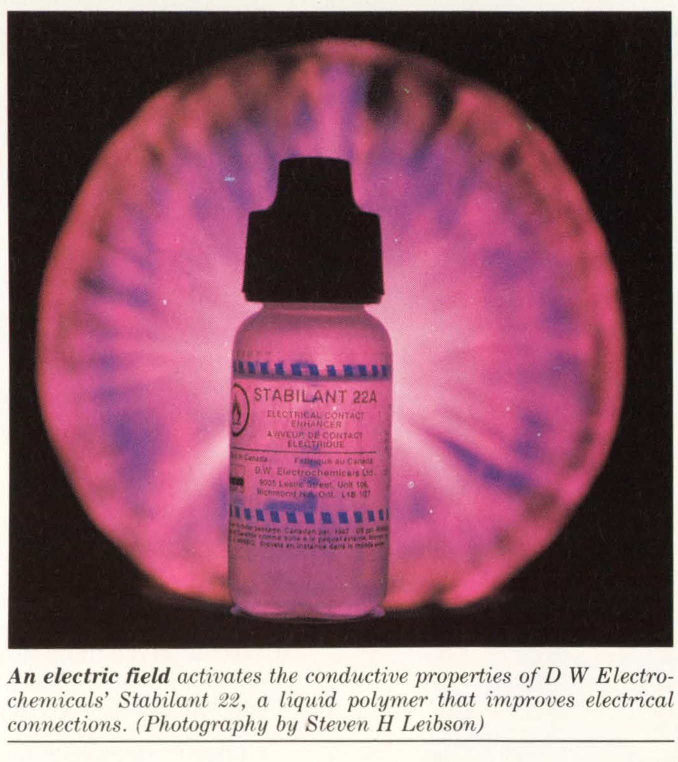
Steven H Leibson, Senior Regional Editor

Despite their best efforts, socket and connector vendors cannot deliver faultless parts. Airborne contaminants, corrosive environments, and a naturally oxidizing planetary atmosphere all conspire to degrade a connection's performance. As the quality of other electronic components continues to improve, the relative unreliability of a product's sockets and connectors emerges as a major cause of product failure. Fortunately, chemical solutions exist for these problems. If you have no experience with such products, you may consider them to be more like snake oil than a remedy for product failures, but many engineers think these chemicals are a godsend.

The shiny finish of a quality connector's contacts looks as though it should work well without help. Despite appearances, however, the contacts of even the best sockets and connectors aren't smooth. Their metallic surfaces have microscopic peaks and valleys. When two parts of a mating connector meet, they actually touch through myriad contact points. A sufficient number of these contacts makes a good electrical connection. However, dirt and corrosion reduce the number of contact points and restrict the flow of current across the joint.

Oxygen in the atmosphere corrodes contact surfaces that lack gold plating. (Because gold is a noble metal, it doesn't readily react with other substances.) Connector vendors may use gold plating to boost a contact's performance, but the corrosive gases found in many industrial environments can degrade even gold-plated contacts. Plated gold is porous, so contaminants can pass through the gold to attack the metal underneath the plating. Over several months, a sufficiently corrosive environment can strip the gold plating from a connector.

When mated together with a high normal force, tin-plated contacts can form gas-tight connections that exclude oxidation and corrosion. Like a gold-plated



***An electric field** activates the conductive properties of D W Electrochemicals' Stabilant 22, a liquid polymer that improves electrical connections. (Photography by Steven H Leibson)*

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connection, a gas-tight joint reduces the problems caused by oxidation, corrosion, and contaminants. However, mechanical vibrations and expansion and contraction from thermal cycling can cause even gas-tight connections to make and break. Each time a connection breaks, oxidation and corrosion take place at the newly exposed contact site. The process is called fretting corrosion **(Ref 1)**.

Fretting corrosion can cause intermittent failures—one of the worst problems to find and solve. These intermittent failures will often disappear, temporarily, if you unplug and then reconnect the failing contacts. A formerly gas-tight connection can open permanently when a layer of insulating film composed of corrosion products builds in a contact joint. Even if the connection doesn't open, its resistance can increase from milliohms to ohms over long time periods as more and more contact points open.

Insulating films in contact junctions form Schottky diodes that distort low-level signals while conducting larger signals. Analog circuits that depend on such a connection may completely fail because of the resistance increase and distortion. Even digital signals can experience significant degradation in rise and fall times.

You can fight oxidation and corrosion. A lubricant applied to mating connectors will seal that connection and prevent airborne contaminants and reactive gases from reaching the contact area. Mineral oil mixed with microcrystalline wax appears to be an adequate contact lubricant for new, uncontaminated surfaces **(Ref 2)**.

If you're fresh out of microcrystalline wax, or if you're treating sockets and connectors that have been in service for a while, you may want to use a prepared product to strip off the existing contamination and provide a barrier to corrosion. If so, consider the Cramolin family of chemicals from Caig Laboratories.

For more information . . .

For more information on the contact-enhancing chemicals discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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Caig makes two types of Cramolin: red and blue. Red Cramolin cleans contacts by dissolving corrosion. After using the red variant, you wipe away the residue and use the blue Cramolin to protect the cleaned contacts. Two-ounce bottles of red and blue Cramolin liquid cost \$15.75 and \$16.25, respectively; 6-oz spray cans of red and blue Cramolin cost \$8.95 and \$9.25, respectively. Caig also sells several forms of Cramolin paste for contacts that carry currents of hundreds or thousands of amperes. The company will soon introduce Cramolin Gold for protecting gold-plated contacts.

Ben Poehland detailed seven years of experience with Cramolin products in one of his columns, "The 8-Bit Alchemist," which appears in *Current Notes*, a magazine for Atari computer users **(Ref 3)**. Poehland described using the chemicals on cable connectors, plugs, jacks, sockets, and particularly on dirty switches. He used red Cramolin to quiet a switch that was injecting noise into a video display after a few week's use. A misbehaving disk-drive selector switch responded similarly.

Poehland also explained how he mixes preparations based on Cramolin products; he doesn't use them straight. He mixes each 2-dram bottle with sufficient trichloroethane to make three ounces of solution. He blends the mixtures in travel-sized, glass mouthwash bottles after carefully relabeling the bottles. Poehland states that thinner Cramolin films work better.

Fill in the gaps

Cleaners and lubricants such as Cramolin enable connectors to perform as designed. However, these chemicals do not conduct electricity; they rely on the connector's contact points to carry current. Stabilant 22 from D W Electrochemicals is a concentrated liquid polymer that fills gaps between mated contacts and conducts current under an applied electric field. Consequently, the company claims that the substance enhances a contact's conductivity. A 15-ml bottle of Stabilant 22 costs \$102.

D W Electrochemicals also sells a dilute version of the product, Stabilant 22a, which consists of 4 parts isopropyl alcohol and 1 part Stabilant 22. This thinner mixture easily flows into small spaces, such as between an IC's pins and its socket contacts. Thus, you can apply Stabilant 22a to connections without separating the contacts, and capil-

Contact-enhancing chemicals

lary action will transport the fluid into the gaps. A 15-ml bottle of Stabilant 22a costs $36. You can get Stabilant 22 in an 8:1 dilution from Sumiko (Berkeley, CA, (415) 843-4500), an importer of high-end audio equipment. Sumiko calls its mixture Tweek. A 7-ml bottle of Tweek costs $18.

Like Cramolin, Stabilant 22 has its advocates. Bill Loughman, a programmer at Childrens' Hospital in Oakland, CA, rejuvenated an ailing, 15-year-old Processor Technology Sol computer using the product. (Processor Technology met its demise years ago, but its computers continue to work.) Loughman added a 5M-byte hard-disk drive to his computer, and the drive had become less reliable over the years. However, Loughman felt he had invested too much of his time and money in the old CP/M machine to retire it.

Hard-disk errors and system crashes occurred with increasing and irritating frequency. Loughman tried replacing cables and connectors but accomplished nothing. Finally, he bought a bottle of Stabilant 22a from Personal Computing Tools (Los Gatos, CA, (800) 767-6728) and treated every connector and IC socket in the system. The computer, which had been failing almost hourly, worked for months without a problem. By coating its edge connector with the liquid, Loughman also refurbished a Sol plug-in personality card that had never worked right.

Personal Computing Tools, a catalog sales outfit, sells a 50-ml bottle of Stabilant 22a for $76. The company's president, Leon Hamner, says that he has heard several success stories like Loughman's. He has also learned of similar successes at computer manufacturers who prefer to keep their use of the liquid quiet. Hamner says he knows the chemical must be a good product because he has sold approximately 500 bottles and has had less than 2% returned. He says that return rate is very low for products sold through a catalog.

Quantitative evidence

The lack of meaningful performance specifications for these chemicals leaves you with little useful information about their effectiveness except for qualitative anecdotal evidence. However, D W Electrochemicals has performed some experiments that produced quantitative information (**Refs** 4 and 5). In one experiment, the company used a distortion analyzer and a spectrum analyzer to measure the performance of 10 sets of 100 gold-plated edge-connector fingers wired in series.

As you can see from the graph in **Fig 1,** the total harmonic distortion generated by the new (at least newly acquired) contacts rose to about 0.004% at low signal levels. The company hypothesizes that thin oxidation films on the contacts created Schottky diodes that rectified low-level signals and created the distortion.

After aging these connectors on an electronics-manufacturing-shop floor for 31 days unmated, and then 31 more days mated, the edge-connector contacts introduced more than twice the harmonic distortion than they did when new. Applying Stabilant 22 dropped the distortion well below the when-new levels. After this test, another 62 days of aging produced no distortion increases.

In a second experiment, the company treated an old and unreliable S − 100 Bus memory board. After measuring the rise times of control signals at 10 of the memory chips' pins, the company applied Stabilant 22 to the board's ICs and sockets. The chemical improved the rise times of the observed signals by an average of 40% and produced a 70% improvement in one instance. Further, the formerly unreliable board worked dependably. The company theorizes that the IC socket's contacts had been exhibiting high contact resistance caused by oxidation.

Because MOS memory chips have

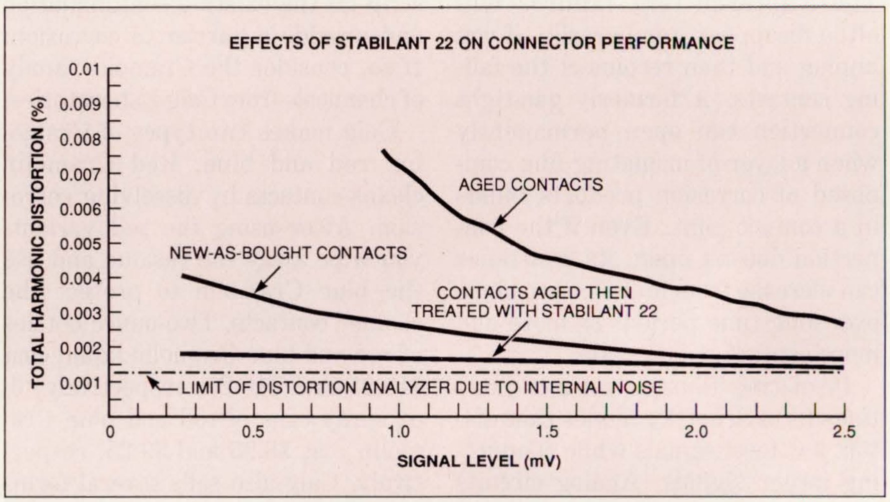

Fig 1—Aging in the relatively benign atmosphere *of an electronics-manufacturing-shop floor more than doubled the distortion introduced by a series circuit of 100 edge-connector contacts. Subsequently coating the connectors with Stabilant 22 dropped the distortion below its original value.*

Contact-enhancing chemicals

high-impedance inputs, the memory ICs on the S-100 Bus board could continue to operate even if the junction impedances between the ICs' pins and the socket contacts were several ohms. A high contact resistance between the socket contacts and the IC pins combined with the ICs' input capacitance could degrade signal rise times and induce failures. Reducing that contact resistance thus improved the rise times.

Even with these stories of miraculous cures, you should be skeptical. Don't let this anecdotal evidence convince you that contact-enhancing chemicals are a cure for all your electrical problems. You cannot remedy fundamental design problems such as timing violations or noisy circuits through the promiscuous use of a spray can or a goop-laden brush. However, the evidence does indicate that these products can conquer oxidation, corrosion, dirt, and intermittent contacts. Because the chemicals are inexpensive, you can afford to evaluate the vendors' claims yourself without incurring much risk. The possibility that you might greatly reduce field failures warrants such investigation. EDN

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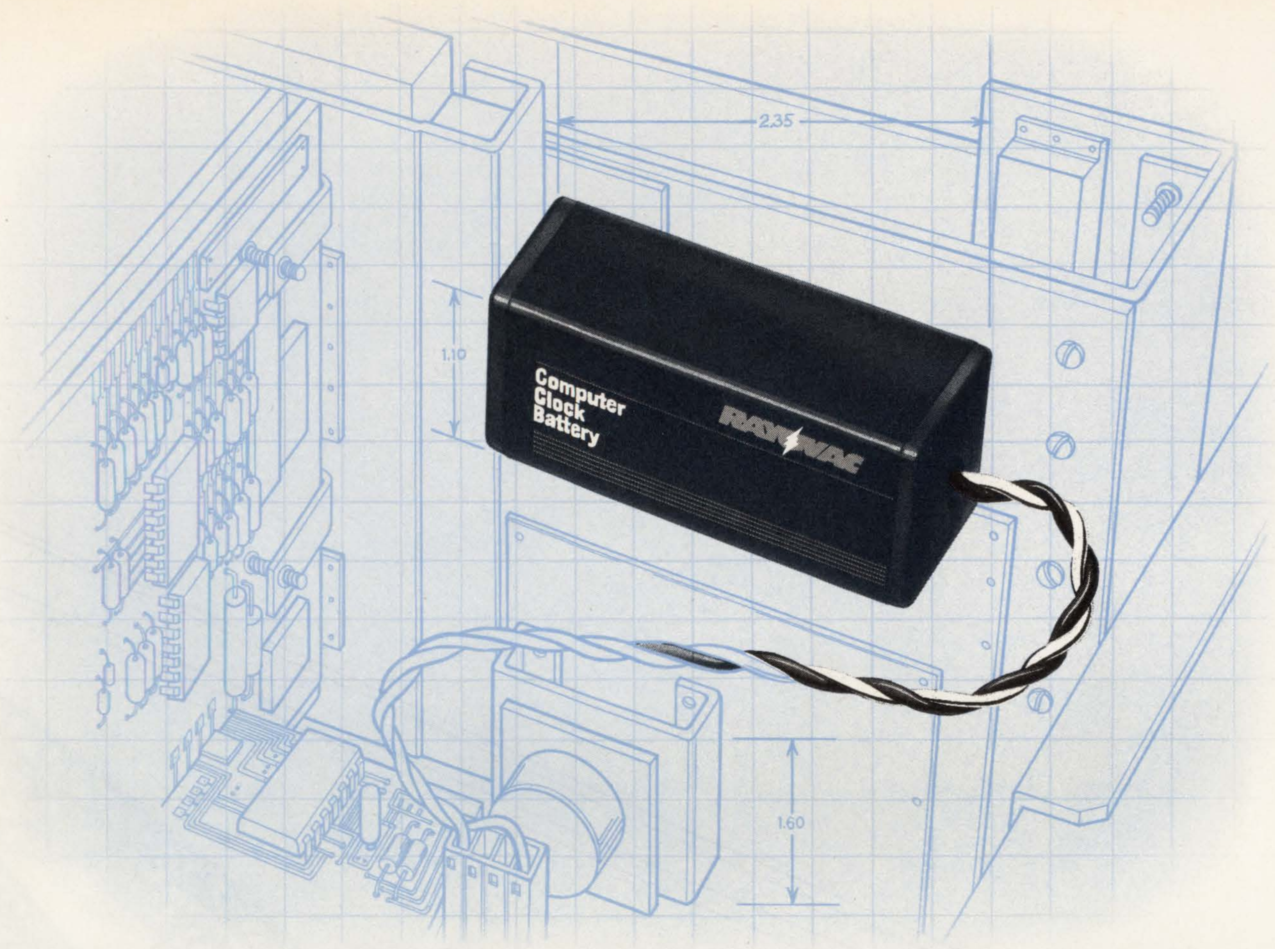

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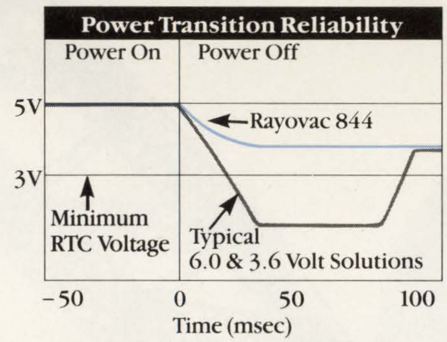
Maintaining voltage is just one way the Rayovac 844 delivers superior reliability. It also offers long life, a 3-5 year span, plus safety no lithium battery can match.



The 844 ensures IC voltage above the critical 3.0V level maintaining clock stability and configuration file memory.

The 844 is compatible with industry standard chip sets: Chips & Technology; VLSI Technology; Western Digital; Zymos and Intel. And it's made in the U.S.A., with on-time delivery available around the world.

So plug added reliability and service into your design. Specify a Rayovac 844. Call Rayovac's Technical Sales & Marketing Department for complete information and battery specifications at 608-275-4694.

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CIRCLE NO. 41

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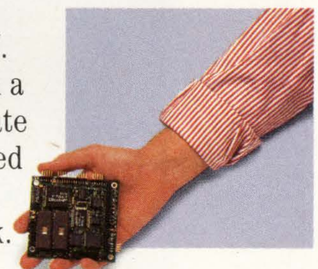
Remember the challenge of constructing "engineering marvels" with your Erector® set? That red metal box held a complete set of interlocking pieces — all that was needed to assemble just about anything. Your imagination was the only limitation.

That's the idea behind Ampro's new way for OEMs to build embedded control applications. Put your application together, simply and quickly, using Ampro Embedded System Modules



Our CoreModule™ family packs ready-made full PC- or AT-compatible intelligence into 3.6″ x 3.8″ x 0.6″. Just plug one into your circuit board — like plugging in a chip — to easily interface to your own logic. They operate over 0 to 70°C, and include a CMOS CPU, RAM, extended BIOS, Solid State Disk, serial and parallel I/O ports, keyboard and speaker interfaces, and a real-time clock.

Stack a CoreModule unit together with one or more of our expansion MiniModule™ peripherals (no backplanes or card cages needed). MiniModule products, also 3.6″ x 3.8″, can be used to add display controllers, more Solid State Disk capacity, network controllers, modem and facsimile features, additional I/O, and much more.

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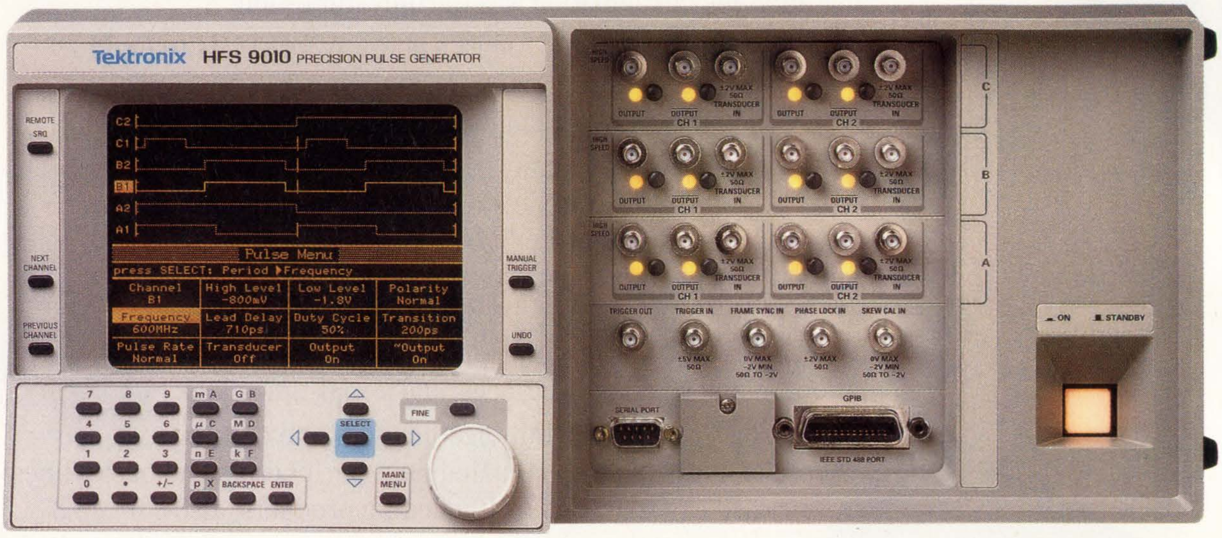
CIRCLE NO. 45

Making



You're looking at the biggest news in signal sources in years: two new families of pulse generators from Tektronix.

You can already see one reason why Tek's new pulse generators are stirring up so much interest: their what-you-see-is-what-you-get user interface vastly simplifies your life.

Now you can stop piecing the big picture together from one-line LEDs, blinking error lights and trial-and-error iteration. Tek's new scope-like display lets you set up and modify a whole set of parameters at once, with a true representation of your pulses and instant, visual feedback.

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Add to all this our popular pulse generator plug-ins from Tek TM500/

CIRCLE NO. 73

MEGA MEMORY.

SONY HIGH-DENSITY SRAMS				
MODEL	CONFIG.	SPEED (ns)	PACKAGING	DATA RETENTION
CXK581000P*	128K x 8	100/120	DIP 600 mil	L, LL
CXK581000M*	128K x 8	100/120	SOP 525 mil	L, LL
CXK581100TM*	128K x 8	100/120	TSOP	L, LL
CXK581100YM*	128K x 8	100/120	TSOP (reverse)	L, LL
CXK581001P	128K x 8	70/85	DIP 600 mil	L
CXK581001M	128K x 8	70/85	SOP 525 mil	L
CXK581020SP	128K x 8	35/45/55	SDIP 400 mil	
CXK581020J	128K x 8	35/45/55	SOJ 400 mil	

***Extended temperature range available.** **L = Low power. LL = Low, low power.**

MEGA COMMITMENT.

As you can see, Sony's more committed than ever to meeting your high-density SRAM needs.

Just consider the enhancements we've made in a few short months: TSOP and TSOP-reverse packaging. Low data retention current. And extended temperature range.

All based on our unique 0.8-micron CMOS technology, and available in 32-pin DIP and surface-mount plastic packages.

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Sony high-density SRAMS are shipping now, complete with competitive pricing. So call (714) 229-4190 today. Or write Sony Corporation Of America, Component Products Company, 10833 Valley View St., Cypress, CA 90630, Attention: Semiconductor sales. FAX (714) 229-4285.

SONY®

CIRCLE NO. 90

Low-drift op amps incorporate switching input stage and DAC-controlled autozero loop

Max425 and Max426 CMOS op amps ($9.50 (100) in 8-pin plastic DIPs) employ a novel internal architecture that allows them to equal or surpass the low-drift performance characteristics of bipolar and chopper-input alternatives. The maximum specifications for input-offset voltage are V_{io} of 5 μV, V_{io} TC of 0.05 μV/°C, and input bias current (I_B) of 200 pA. V_{io} noise in a 0.1-to 10-Hz bandwidth is typically 0.25 μV p-p, which represents a fivefold improvement on similar specs for the best choppers.

Both amps have 140-dB min open-loop voltage gain and common-mode and power-supply rejection ratios of 120 dB min. Internal compensation yields gain-bandwidth products of 350 kHz and 15 MHz, for the Max425 and Max426, respectively. The amps consist of three amplifier stages under control of on-chip logic circuitry. The essential parts appear in the block diagram of **Fig 1**.

The op amps achieve low-drift performance by using two independent and programmable on-chip nulling techniques. The first is an autozero loop, and the second is a commutating input stage.

The autozero loop operates by shorting the input switch and nulling the first two stages of the op amp. The loop operates until the voltage at the comparator equals the level immediately prior to commencement of the autozero cycle. Digital memory in the control logic stores the correction factor and maintains the null via DACs. One cycle of this autozero loop typically reduces a 50-μV V_{io} to 0.5 μV.

You can program the autozero loop to operate either on command or automatically once every minute. While the autozero loop is in action, the op amps' output stage operates as a S/H circuit and maintains output at a constant voltage. The down side of this technique is the 50 msec it takes for one cycle of autozero operation to execute, even on the faster Max426.

The input stage commutates at a default frequency of 300 Hz, although external frequency control is possible. When the switches operate, the op amps' V_{io} and 1/f noise alternately add to and subtract from the external signal source. The effective input is the signal source, amplitude modulated at 300 Hz by the op amps' input offset and noise. A similar waveshape appears at the op amps' output, with an average value of the signal source multiplied by the closed-loop gain.

You have a choice of programming both, either, or neither nulling method for operation. There are performance tradeoffs, however. Without programming the commutating switch, no cancellation of 1/f noise results. In addition, without an occasional cycle of autozero-loop operation, the op amps' output signal may contain an increasing level of 300-Hz ripple.

Basic applications include use of the op amps as thermocouple-sensor and strain-gauge-bridge amplifiers. Judicious programming of the nulling techniques, however, allows you to use the amplifiers for other applications. For example, with the commutating switch off, I_B max reduces to 10 pA, opening up possible use in high-impedance circuits. In data-acquisition systems where continuous or burst readings demand minimal interruption, you can hold off operation of the autozero loop until a convenient time slot is available.—***Brian Kerridge***

Maxim Integrated Products, 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600. FAX (408) 737-7194.

Circle No. 732

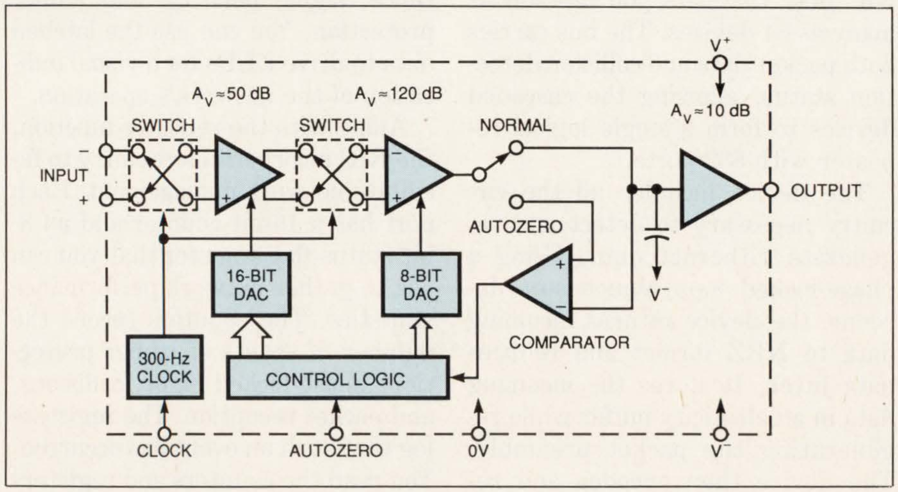
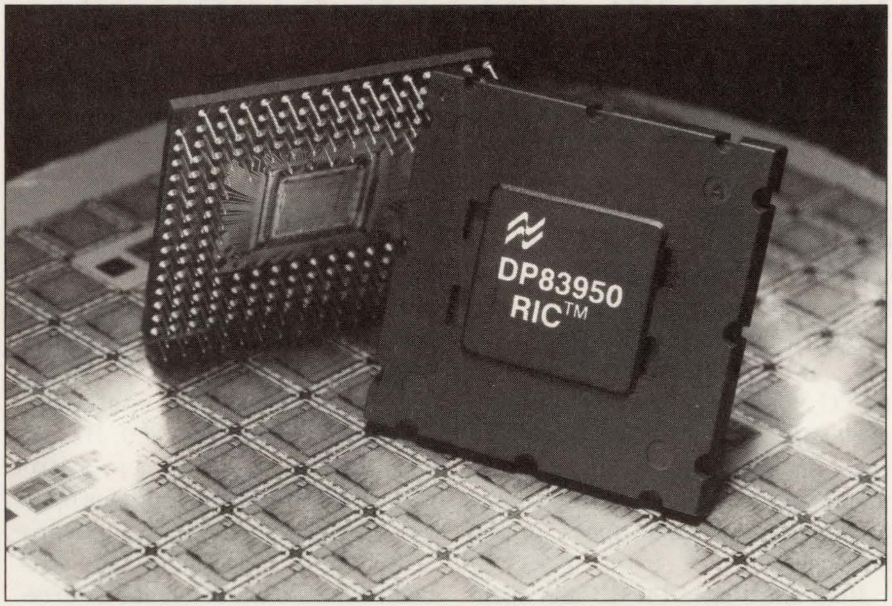


Fig 1—Two independent on-chip nulling techniques *in Max425 and Max426 op amps allow you to tailor low-drift performance to a variety of applications.*

Repeater IC offers 12 10Base-T ports with network management capability



Combining both repeater and network-management functions, *the DP83950 helps you build managed and nonmanaged IEEE-802.3 Ethernet hubs.*

The DP83950 repeater interface controller (RIC) simplifies the design of managed Ethernet hubs by combining, in a single IC, both repeater circuits and logic for gathering network-management data. The IC contains transceivers, PLL-based Manchester encoding and decoding circuits, and an elasticity buffer for receiving and regenerating data packets. It also contains a variety of event counters, status registers, and interface circuits for handling the network data.

The RIC has 13 Ethernet ports. One port contains an attachment unit interface (AUI) for connecting to AUI-compatible transceiver boxes and cable. The remaining 12 ports contain on-chip 10Base-T transceivers, allowing you to connect the port to twisted-pair wiring with an additional 74ALSXXX driver and a transformer filter. Or, you can bypass the on-chip transceivers and use external transceivers for connection to other media.

You are not limited to 13 ports in your hub, however. The RIC offers a set of signals, called the inter-RIC bus, that lets you cascade as many as 64 devices. The bus carries both packet data and collision detection status, allowing the cascaded devices to form a single logical repeater with 832 ports.

The device includes all the circuitry necessary to detect and regenerate Ethernet data. Using a phase-locked loop Manchester decoder, the device returns incoming data to NRZ format and reduces data jitter. It stores the incoming data in an elasticity buffer while regenerating the packet preamble. The device then encodes and retransmits the stored data.

You control the RIC's operation via an 8-bit microprocessor interface port that serves a dual purpose. In addition to interacting with the host processor, the port can address and drive status display latches. These latches provide 5 bits of information on each port, including link integrity, collision occurrence, signal polarity, and jabber protection. You can use the latched data to drive LEDs for a visual indication of the network's operation.

Along with the repeater function, the RIC incorporates circuitry to facilitate network management. Each port has a 16-bit counter and an 8-bit status-flag register that you can use to gather network performance statistics. The counters record the number of events of jabber protection, phase-locked error, collisions, and packet reception. The registers log that such an event has occurred. You read the counters and registers through the RIC's microprocessor interface.

The RIC also facilitates network management by creating a hub-management status packet. The device can duplicate and transfer an incoming packet to another port and to an Ethernet controller connected to the hub-management interface. The device then appends 7 bytes of status information to the packet sent to the controller. The status information includes the receiving port's address, the timing of any collisions, the time between packets, and the event counter status flags, allowing the controller to analyze the network's performance on a per-packet basis.

The RIC is a 5V CMOS device housed in a 160-pin plastic pin-grid array package. It is available in sample quantities and costs $145 (100).—***Richard A Quinnell***

National Semiconductor, Box 58090, Santa Clara, CA 95052. Phone (408) 721-7020 or local office.

Circle No. 731

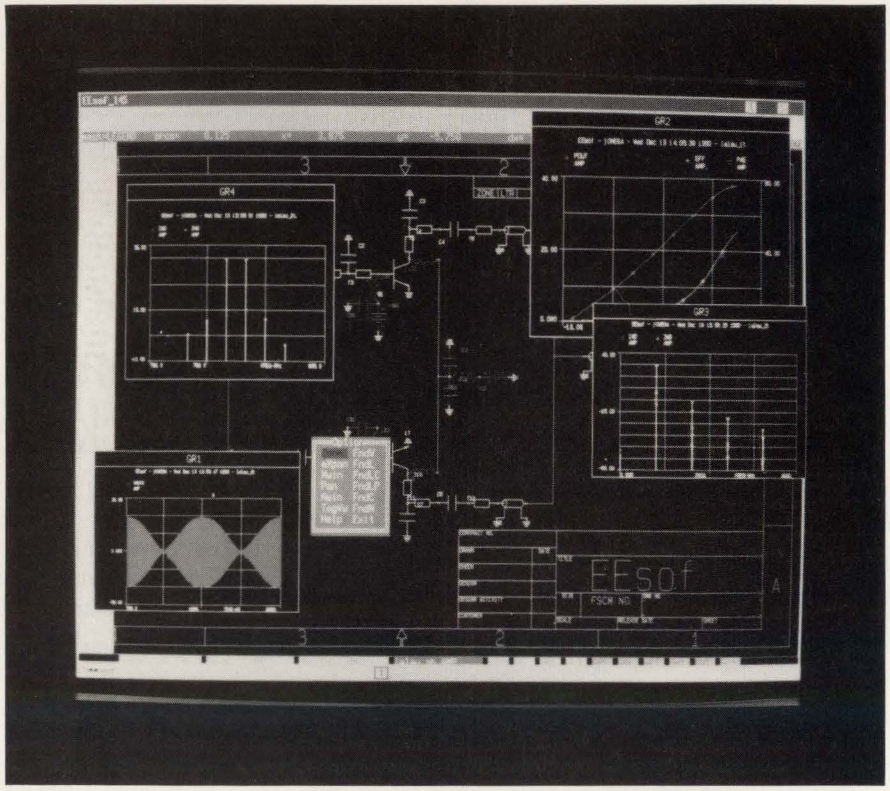
Simulator analyzes and optimizes high-frequency circuits

A CAE package called jOmega simulates circuits operating at 30 to 3000 MHz. A harmonic-balance simulator that partitions the design into linear and nonlinear portions facilitates such high circuit-speed analysis. For the nonlinear section, the simulator represents currents and voltages by harmonic-series time-domain waveforms. The simulator uses the FFT to convert the waveforms to the frequency domain. Frequency-domain equations allow the simulator to determine the boundary conditions and iterative analysis provides the internal circuit analysis.

The simulator's ability to optimize both linear and nonlinear circuits and to use lossy and dispersive transmission-line RF circuit models are among the advantages of harmonic balance over such classical simulation algorithms as Spice.

The package's statistical-analysis capability provides two optimization routines. The first allows you to simulate and tune your circuit to meet tight performance specifications. Nonlinear tuning offers the ability to gain insight into your circuit's operation via circuit tradeoffs. This tuning capability can assist you in securing optimum conditions for amplifier output, mixer conversion loss, and oscillator-output spectral purity. The other routine performs yield optimization, letting you trade off component cost, reliability, and performance.

In addition, jOmega features a schematic editor and a library of approximately 50 RF, package-level circuit models and standard BJT (bipolar junction transistor) models that you can customize. File management and documentation tools are also part of the tool set.



A harmonic-balance algorithm *in jOmega analyzes and optimizes operating characteristics such as power saturation, power-added efficiency, and intermodulation distortion.*

An option to the software adds floor planning and the ability to mix physical layout and electrical simulation. Using the floor planner, you can verify that all components will fit on your board. With this feature, you can predict and fix proximity and parasitics problems before you draft a layout of the board.

The jOmega floor-planning tools augment—rather than replace—more powerful board-layout tools. The package's software communicates with other layout software via Gerber, IGES (Initial Graphics Exchange Specification), and neutral mask output file standards.

The software runs on IBM PCs under OS/2 and on Sun, HP/Apollo, and IBM workstations. Available in the second quarter of 1991, the software costs $24,500; the final price depends on the system, configurations, and options you choose. The floor planner costs $5000.

—Michael C Markowitz

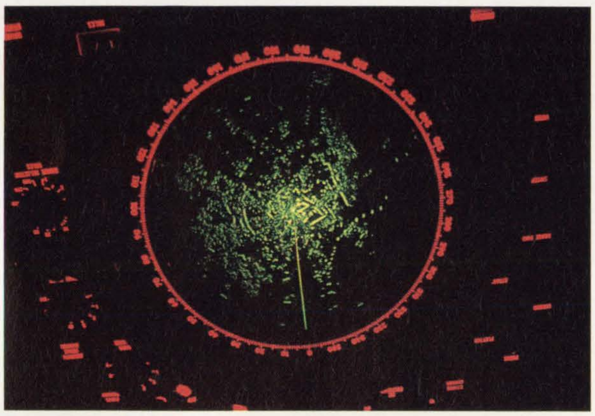
EEsof Inc, 5601 Lindero Canyon Rd, Westlake Village, CA 91362. Phone (818) 991-7530. FAX (818) 991-7109. TLX 384809.

Circle No. 730

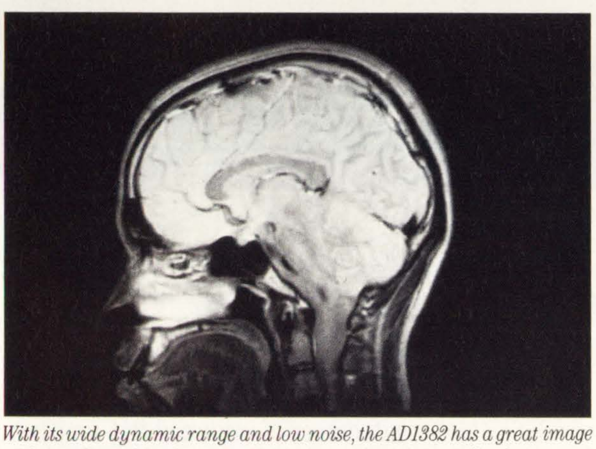
The only 16-bit, 500 kSPS SADC with guaranteed dynamic performance.

For the competition, that's not a pretty picture.

If you're working in spectral imaging applications, our new AD1382 presents a very pretty picture indeed. Because it's the first 16-bit, 500 kSPS single-package sampling A/D converter to offer guaranteed ac performance.



The use of the AD1382 is soaring in radar applications, thanks to its higher level of integration and guaranteed dynamic performance.



With its wide dynamic range and low noise, the AD1382 has a great image with people working in magnetic resonance imaging applications.

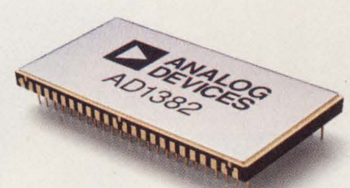
The AD1382 delivers guaranteed 100% production tested SNR, THD and peak distortion performance at three input frequencies and over two input ranges – testing that gives you the confidence to design for the best possible noise performance in your system.

You can also feel confident about the cost-effectiveness of the AD1382. It offers a higher level of integration with on-board track/hold and reference.

And since it's a single package, it's easier to design in and uses less board space than more expensive modular or multipackage solutions.

For a better picture of what the AD1382 can do for you, contact Analog Devices at 1-800-262-5643. Or write to Analog Devices, P.O. Box 9106, Norwood, MA 02062-9106.

AD1382



A 16-bit 500 kSPS SADC, the AD1382 provides excellent dynamic and static performance in a dual inline ceramic package.

Guaranteed (@25°C, ± 5 V input range):

SNR
- **5 kHz 90 dB min**
- **100 kHz 90 dB min**
- **200 kHz 88 dB min**

THD & Peak Distortion
- **5 kHz – 90 dB min**
- **100 kHz – 88 dB min**
- **200 kHz – 74 dB min**

DC specifications include:
0.0015% FSR INL, 0.0006% FSR DNL and NMC guaranteed to 16-bits

Other features include:
Zero offset autocalibration
± 5 V, ± 10 V Bipolar input range

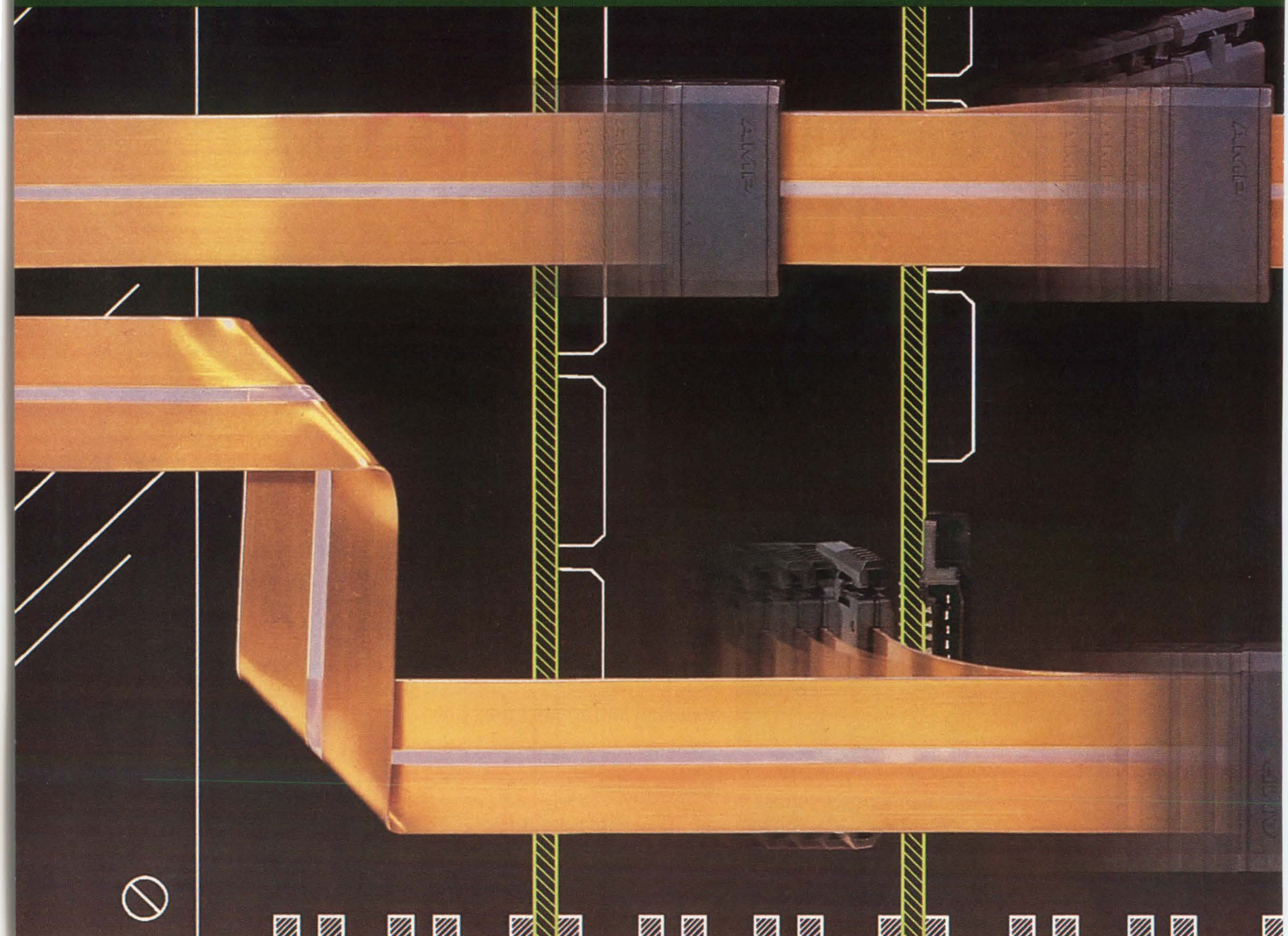
An evaluation board for the AD1382 is available.

ANALOG DEVICES

Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106. Offices and applications support available worldwide.

CIRCLE NO. 67

Putting high-performance power distribution on the fast track.

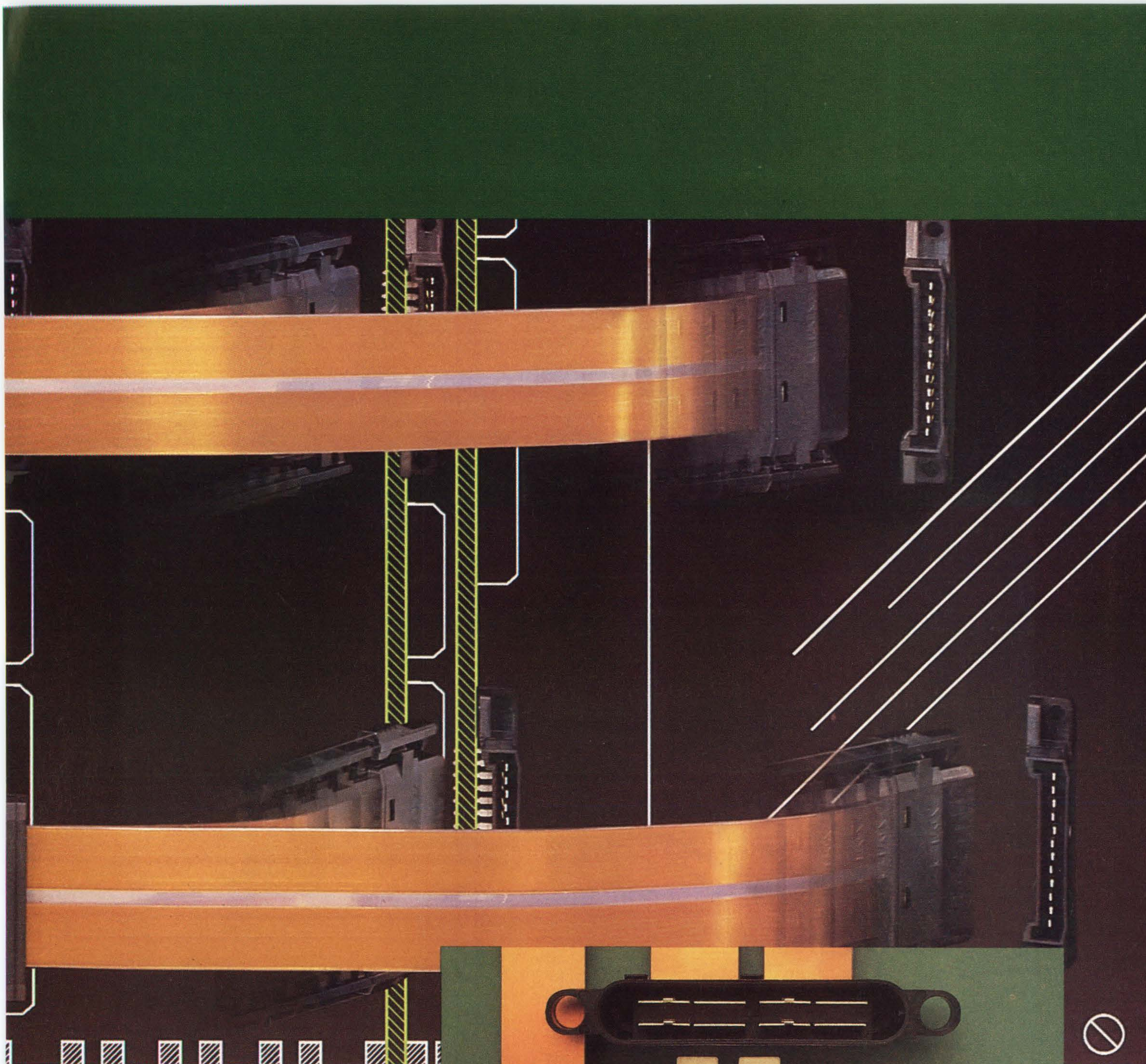


THIS IS AMP TODAY.

Designers of today's high-performance power distribution systems (PDSs) need a practical way to take advantage of the compact size, thermal efficiency, and low inductance of insulated flat copper power cable.

Our newest invention not only makes flat conductors practical, it adds powerful new options to the way you can design your 'flat power' PDS.

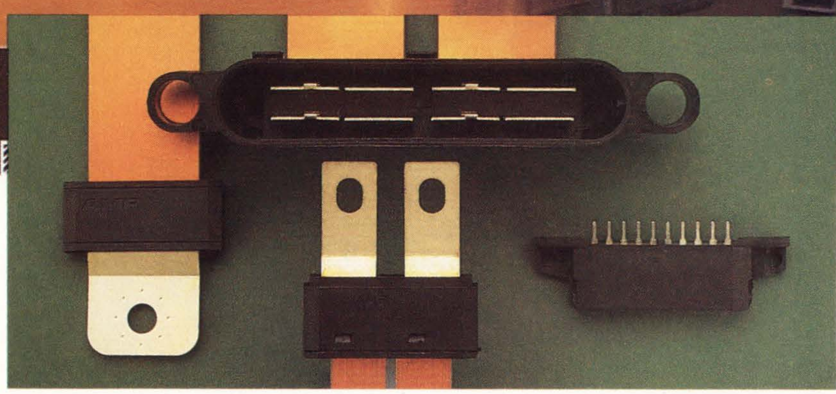
AMPOWER Wave Crimp



Assemblies let you specify direct taps on flat cable wherever you'd like, for efficient branching. And they give you a true modular approach to power—with separable printed circuit board connectors and sequenced Blind Mate drawer connectors—for fast assembly, and easy service and upgrade.

The exclusive crimp termination contacts an area 50% greater in cross section than the conductor itself. Result: no thermal penalties, no current restrictions, no compromise in the inherent low-noise properties of flat conductors. Electrical characteristics are consistently predictable.

To realize all the new opportunity in flat power right now, call 1-800-522-6752 (fax 717-561-6110) and ask about AMPOWER Wave Crimp Assemblies. In Canada call 416-475-6222. AMP Incorporated, Harrisburg, PA 17105-3608.



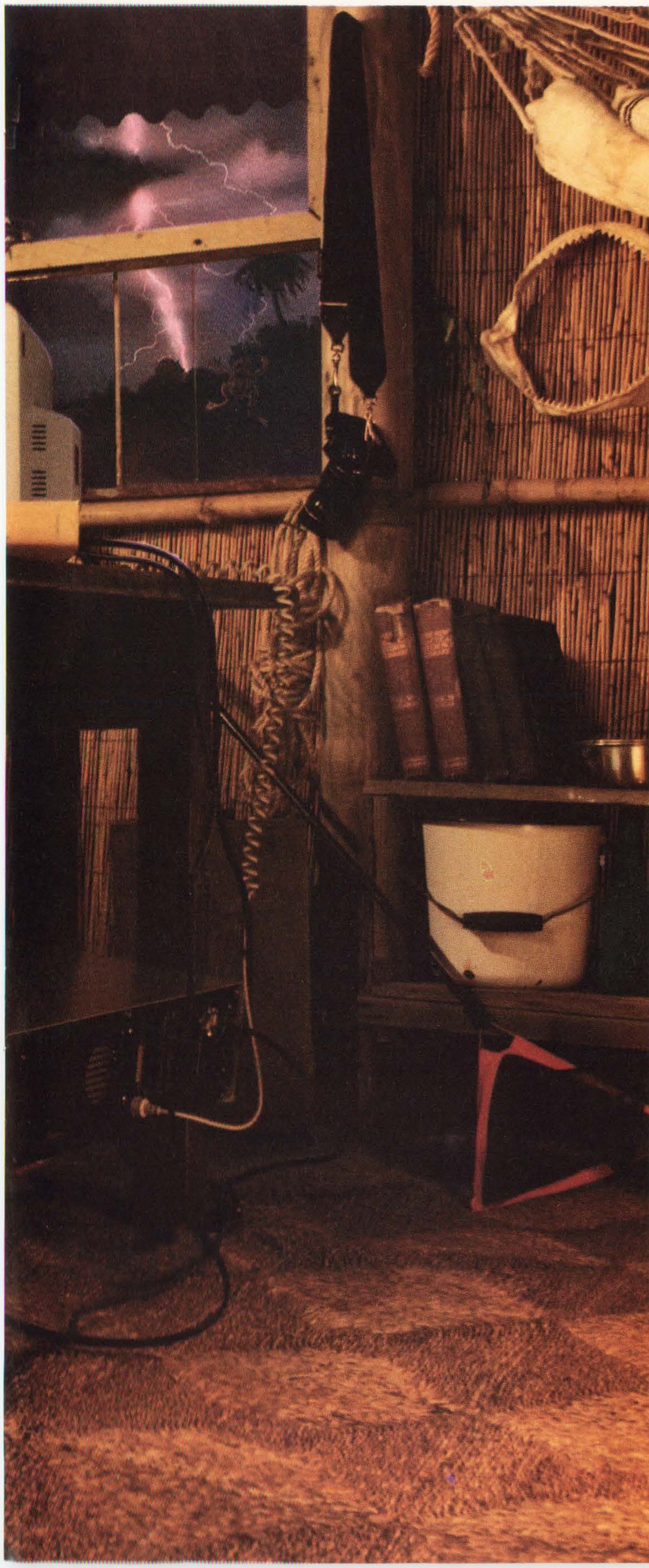
Flat conductor PDS made practical.

CIRCLE NO. 94

AMP

From Outer Space to Your Place,

We're Your Best Defense.



By putting our military experience to work in high-volume, low-cost applications, we're giving new meaning to the term *National Defense*. Our Power Supply Supervisory Chips are a good example.

These Raytheon Linear Arrays *(RLAs)* act as a computer's early warning system. They monitor internal voltage levels to 0.3% accuracy—and signal a shut down before power surges can fry the system.

It's "Defense Technology" with a peaceful purpose. And it's helping take computers into places they've never been.

Our RLAs have business benefits, too. If you can't decide between a custom or semicustom device, don't. Our *Win-Win* program lets you get to market quickly with a semicustom array, then shift to full custom as sales increase.

Win-Win is fast, flexible, and makes good business sense because it eliminates the risk of getting into a full custom array before you're really ready.

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CIRCLE NO. 72

Raytheon

Where quality starts with fundamentals

EDN SPECIAL REPORT

Monolithic instrumentation amplifiers

As they become cheaper and more versatile, monolithic instrumentation amplifiers are growing more attractive for high-accuracy circuit applications. The days of discrete designs' dominance may be numbered.

Doug Conner,
Regional Editor

Although you can design your own instrumentation amplifier from an op amp and four resistors, you'll find it difficult to maintain accuracy for resolution beyond 12 bits. Monolithic instrumentation amplifiers offer a high-performance alternative.

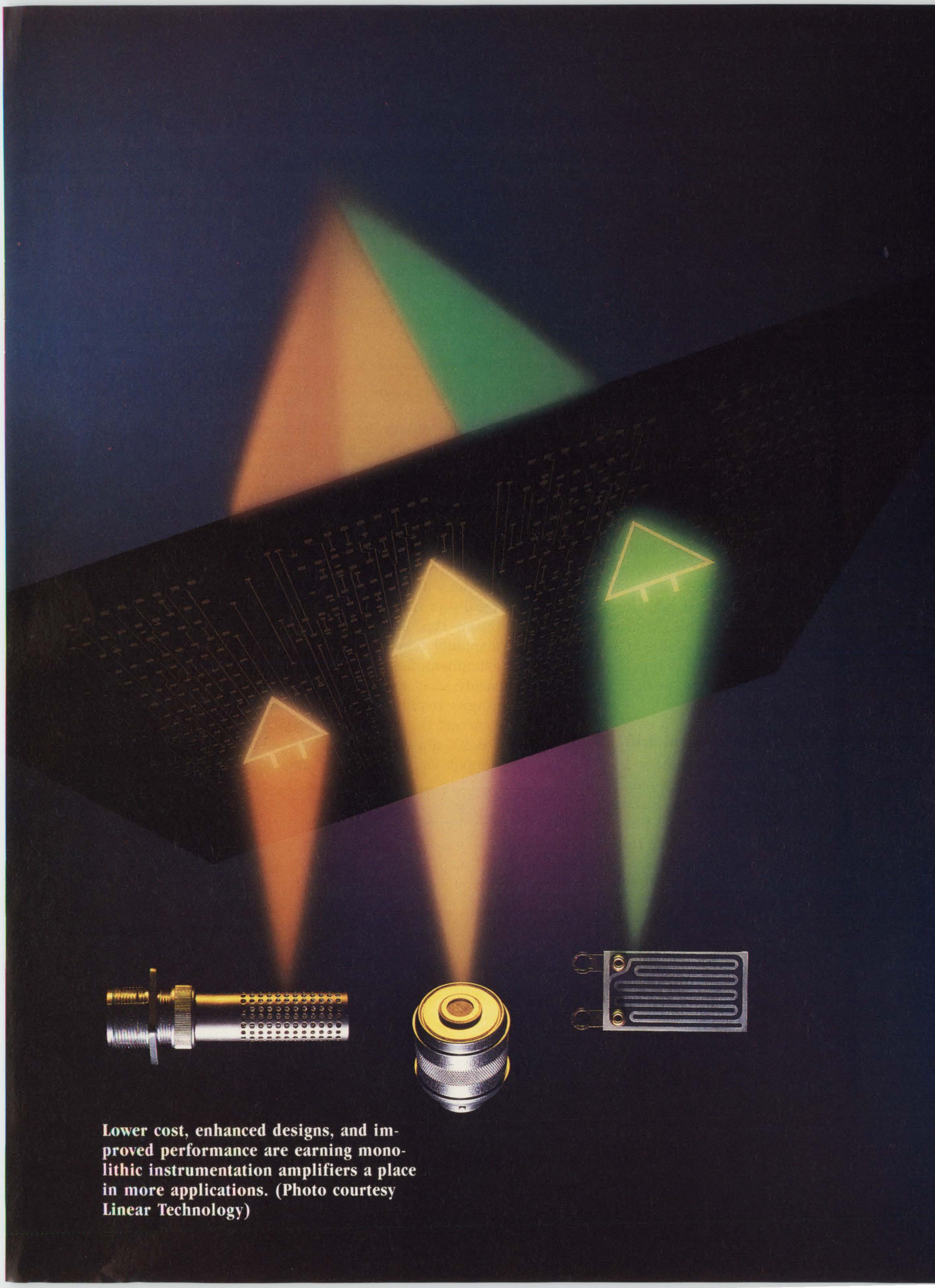
An instrumentation amplifier differs from an ordinary op amp in that it is a committed differential-input gain block with a fixed or easily set gain. Instrumentation amplifiers accept a differential input signal, multiply it by a gain, and output a single-ended signal referenced to a local analog ground. Because input signals are often of low amplitude, many instrumentation amplifiers let you amplify the signal by gains of 1000 or more.

The differential input signal to an instrumentation amplifier may have an amplitude of only a few millivolts riding on top of a common-mode signal of several volts. For cases where common-mode voltages are large, a high common-mode rejection ratio (CMRR), defined as the ratio of differential gain to common-mode gain, is important. The high CMRR keeps the common-mode voltage fluctuations from causing errors in the output.

The low-frequency CMRR for monolithic instrumentation amplifiers typically ranges from around 75 dB for a gain of 1 to 120 dB for a gain of 1000 (**Table 1**). The CMRR depends on frequency, diminishing as the frequency increases. Instrumentation-amplifier data sheets provide graphs showing the degradation of CMRR with increasing frequency.

Some other traits common to instrumentation amplifiers are a matched high-input impedance and a low input-bias current. A low input-bias current is important when signal sources have a high output impedance or when you're coupling the input through a large series resistance. You may need to include large series resistors on the inputs of an instrumentation amplifier for overvoltage protection or as part of a low-pass RC filter.

You needn't purchase a ready-made instrumentation amplifier. You can construct your own inexpensive device as shown in **Fig 1**. This configura-



Lower cost, enhanced designs, and improved performance are earning monolithic instrumentation amplifiers a place in more applications. (Photo courtesy Linear Technology)

Instrumentation amplifiers often have separate input and output offset-voltage specifications.

tion is the simplest form of differential amplifier—adequate for 8-bit resolution applications. It offers neither matched nor high input impedance. Linearity, drift, and CMRR specifications will depend on the components used.

You can also construct 2- and 3-amplifier devices for better performance; however, you may not be able to justify using them. As you add amplifiers, the component cost and pc-board space begin to add up to the point where a monolithic instrumentation amplifier would be more economical and offer higher performance. Pricing for monolithic instrumentation amplifiers starts at approximately $5 (100). In addition, more-compact monolithic instrumentation amplifiers, available in 8-pin DIPs and surface-mount packages, consume even less pc-board space.

Monolithic designs control drift

Monolithic designs offer other advantages over do-it-yourself amplifiers. Because monolithic instrumentation amplifiers keep all internal resistors close to the same temperature, drift specifications are typically quite good. Although off-chip matched-resistor networks can also provide stable resistance ratios, thermocouple effects between the resistor network and the op amp can cause specifications to drift with temperature changes.

Instrumentation amplifiers usually amplify low-level signals, where the range of the differential input may be only tens of millivolts. When dealing with these low-level signals, voltage offsets caused by the instrumentation amplifier are critical. Unlike operational amplifiers, whose data sheets typically specify voltage offsets as an input offset voltage, instrumentation amplifiers often have two specifications for offset voltages: one for input offset voltage and one for output offset voltage.

The reason for separating the voltage offset specification is that the input and output stages of the amplifier contribute separately to the total voltage offset. The total offset voltage is

$$V_{OFFSET} = V_{INPUT\ OFFSET} \times Gain + V_{OUTPUT\ OFFSET}.$$

The total dc offset voltage for instrumentation amplifiers ranges typically from 10 μV to a few millivolts. You can trim amplifiers with high dc offset voltages for high-accuracy dc applications if the offset is stable enough over time and temperature.

Instrumentation-amplifier manufacturers typically provide application information that includes a method of manually trimming the dc offset. Instrumentation amplifiers with separate input and output dc offset voltages require two adjustments to correct the offset completely. You don't always need to correct both input and output offsets. For high-gain values, the input offset voltage dominates the error term, so you can usually obtain acceptable results by correcting only the input offset.

Another approach manufacturers offer is an auto-zeroing method which lets you periodically measure and correct the output of the instrumentation amplifier. Auto-zeroing typically involves shorting the two inputs of the instrumentation amplifier and adjusting the output to zero in software or hardware.

The easiest way to get an amplifier with low dc offset voltage is to buy one. Linear Technology broke new ground in instrumentation amplifiers by offering the first chopper-stabilized instrumentation amplifier, the LTC 1100, with a 10 μV total offset.

Gain considerations

DC offset isn't the only issue to consider when evaluating the dc accuracy of an instrumentation amplifier; gain accuracy is also important. The nominal gain error on monolithic instrumentation amplifiers typically ranges between 0.01% and 1%, depending on both the amplifier model and the gain you select. If

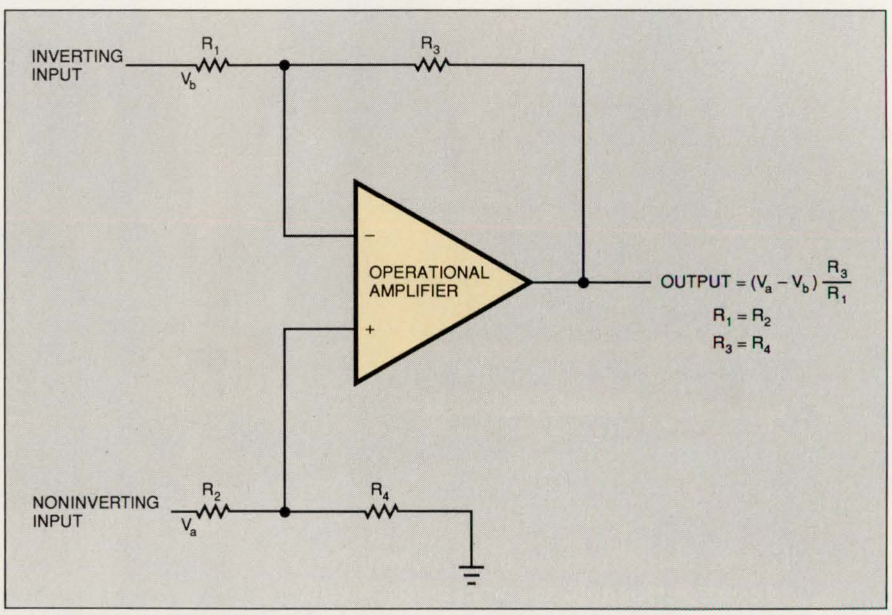


Fig 1—An op amp and four resistors make a differential amplifier of limited capability. This low-cost circuit is normally adequate for 8-bit applications.

the nominal-gain-error contribution is too large, you can trim the gain for higher accuracy.

Other sources of gain error are difficult or impossible to trim. The gain nonlinearity error can range from almost nothing (0.0007%) to 0.1%. Gain drift accompanying temperature changes can add errors ranging from 4 ppm/°C to 100 ppm/°C. An error of 100 ppm/°C may not sound like much, but if your amplifier must operate over a relatively large temperature range, such as 70°C, you're looking at a potential 0.7% error.

You should watch for potential drift problems, but the selection of gains available, and how you select them, may be just as important. You can use three common methods to set the gain of instrumentation amplifiers: adding resistors, selecting with pins, and selecting with software.

Programming gains with resistors gives you the most flexibility, typically allowing you to select gains from 1 to 10,000. Using one or two resistors having the right values, you can set any desired gain value. Of course, the resistors must be precision resistors with low drift characteristics. However precise initially, resistor-programmed gains carry the potential disadvantage of increased drift with temperature changes.

Instrumentation amplifiers that let you use pin- or software-programmable gains fully specify the drift in their product data sheets. Gains available on these products are usually limited to powers of 10 or powers of 2. Pin-programmable instrumentation amplifiers require you to connect the appropriate signals and pins to select the gain. Software-programmable instrumentation amplifiers let you select among the possible gains by applying a digital word to the inputs.

The advantage of pin- and software-programmable instrumentation amplifiers is that no precision resistor is needed to program the gain. The disadvantage is in limiting you to the built-in gains.

Adjust gain with fixed-gain amps

If you want a gain that isn't available on a pin- or software-programmable instrumentation amplifier,

Table 1—Representative monolithic instrumentation amplifiers

Manufacturer	Product	Gain	Gain select method	Gain error (% max at 25°C)[1]	DC input offset (± μV max at 25°C)[1]	DC output offset (± μV max at 25°C)[1]	Input bias current (nA max at 25°C)[1]	Unit price[2] (100)	Notes
Analog Devices	AD365	1, 10, 100, 500	Digital	0.05 to 0.1	200	5000	50	$65.10	Includes track-and-hold.
	AD522	1 to 10,000	Resistor	0.05 to 1.0	200 to 400	0	25	$37.80	
	AD524	1, 10, 100, 1000	Pin	0.02 to 2.0	50 to 250	2000 to 5000	15 to 50	$9.90	
	AD526	1, 2, 4, 8, 16	Digital	0.01 to 0.15	250 to 700	0	0.15	$8.25	
	AD624	1, 100, 200, 500, 1000	Pin	0.02 to 1.0	25 to 200	2000 to 5000	15 to 50	$11.90	
	AD625	1 to 10,000	Resistor	0.02 to 0.05	25 to 200	2000 to 5000	15 to 50	$9.50	
	AD626	20	Fixed	0.2	NA	NA	NA	$3.00	Gains from 1 to 160 are possible; single supply.
	AMP-01	0.1 to 10,000	Resistor	0.6 to 0.8	50 to 100	3000 to 6000	4 to 6	$9.90	
	AMP-02	1 to 10,000	Resistor	0.02 to 0.7	100 to 200	4000 to 8000	10 to 20	$4.75	
	AMP-05	0.1 to 2,000	Resistor	0.5 to 1.0	1000 to 2000	15,000 to 25,000	0.05 to 0.1	$9.90	
	SSM-2017	1 to 1000	Resistor	0.13 to 3.5 typ	220 typ	47 typ	6700 typ	$1.80	THD + Noise < 0.01% for gain = 100, from 20 Hz to 20 kHz; 850 pV√Hz Noise.
Burr-Brown	PGA202	1, 10, 100, 1000	Digital	0.15 to 1.0	500 to 1000	5000 to 20,000	0.050	$6.95	
	PGA203	1, 2, 4, 8	Digital	0.15 to 0.25	500 to 1000	5000 to 20,000	0.050	$6.95	
	INA102	1, 10, 100, 1000	Pin	0.05 to 0.9	100 to 500	200 to 300	30 to 50	$5.65	
	INA103	1, 100	Pin	0.01 to 0.25	50 to 100	2000 to 5000	8000 to 12,000	$6.90	THD + Noise ≤ 0.0009% for gain = 1000, at 1 kHz.
	INA120	1, 10, 100, 1000	Pin	0.05 to 1.0	25 to 200	600 to 2000	20 to 50	$5.90	
Linear Technology	LTC1100	10, 100	Pin	0.04 to 0.075	10	0	0.05	$6.45	Chopper stabilized; single supply.
	LTC1101	10, 100	Pin	0.04 to 0.06	160 to 220	0	8 to 10	$4.95	Single supply.
	LTC1102	10, 100	Pin	0.05 to 0.07	600 to 900	0	0.04 to 0.06	$4.95	
National Semiconductor	LM363	10, 100, 1000	Pin	0.5	100 to 2000	0	10	$8.35	

Notes: NA = Specification not available at press time.
1. Range of maximum values is for different versions and gain settings.
2. Amount is for lowest priced version.

Even for low-frequency signals, you may have bandwidth concerns if you are multiplexing signals.

you essentially have three choices. First, you can use a resistor-programmable instrumentation amplifier. Also, some pin- and software-programmable instrumentation amplifiers let you use resistors for setting nonstandard gains.

Second, you can add a conventional op-amp gain stage after the instrumentation amplifier. Because the output of the instrumentation amplifier provides a signal with low impedance that is referenced to ground (single-ended), setting the gain with an op amp is relatively easy. But the additional gain stage provides another source of gain error and drift. If you need to trim the circuit to correct gain error, then you can trim both the instrumentation amplifier's contribution and that of the op-amp gain stage with one adjustment.

In this case, the gain drift with temperature will remain an important consideration unless you'll be using the circuit for a relatively narrow temperature range. Adding periodic automatic gain calibration to the circuit, similar to auto-zeroing for offset, would also eliminate this concern.

The third choice is to perform final gain scaling in software. For certain applications, you'll often convert the analog output to a digital word and send it to a computer. Initial scaling usually is necessary only to set the correct order of magnitude for the signal. This adjustment is sufficient to satisfy electrical considerations such as the acceptable voltage range for the A/D converter. Once the analog signal is converted to digital, you can perform the final scaling in software.

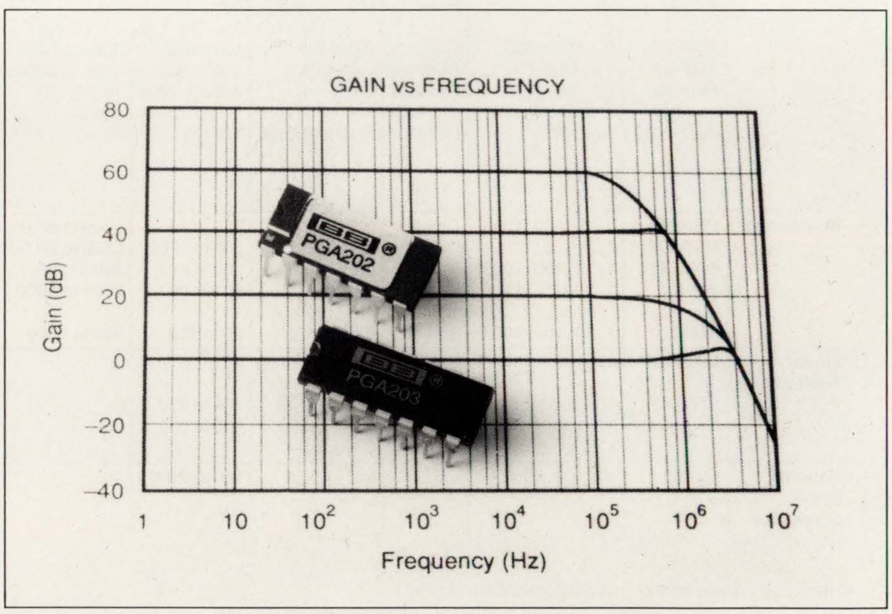
If you need an instrumentation amplifier for a high-accuracy application, you need an accurate output voltage at the load, not just on the output pin of the amplifier. Instrumentation amplifiers typically have an output-drive-current capability of several milliamperes. However, when dealing with high-accuracy circuits, you sometimes need to deliver an accurate voltage to a node through some resistive series connection.

Even a 0.1Ω series resistance will cause a 100-μV offset when you drive 1 mA through it. To avoid this offset, some instrumentation amplifiers provide an output sense line in addition to the output force line. The sense line feeds back the output voltage measured at the load, allowing the amplifier to compensate for any voltage drop between the amplifier and the load. If you keep the instrumentation amplifier and associated circuitry close together, you can probably avoid both voltage drops because of series resistance and the need for a sense line. But if you can't keep the amp and circuitry close, a sense line can save components and reduce offset when the voltage drops are unavoidable.

Another feature showing up on instrumentation amplifiers is single-supply operation. Although you can use a single supply plus ground to power any instrumentation amplifier, the qualities that define useful single-supply operation are usually operation at 5V or less and the ability of the inputs and output to swing very close to the supply and ground.

At least three instrumentation amplifiers—the LTC1100 and LTC1101 from Linear Technology and the AD626 from Analog Devices—now offer single-supply operation. The LTC1101 operates down to ground with the lowest supply current requirement of any instrumentation amplifier—120 μV. The AD626 has a midscale offset feature that allows it to accept bipolar signals with a single supply. Input signals can exceed the range of the supply rails.

The amplifiers discussed so far have been instrumentation amplifiers for dc applications. Yet these amplifiers often end up in applications where the frequencies are between dc and 10 Hz. For these low-frequency applications, dc performance is of primary importance, but ac performance may also require attention.



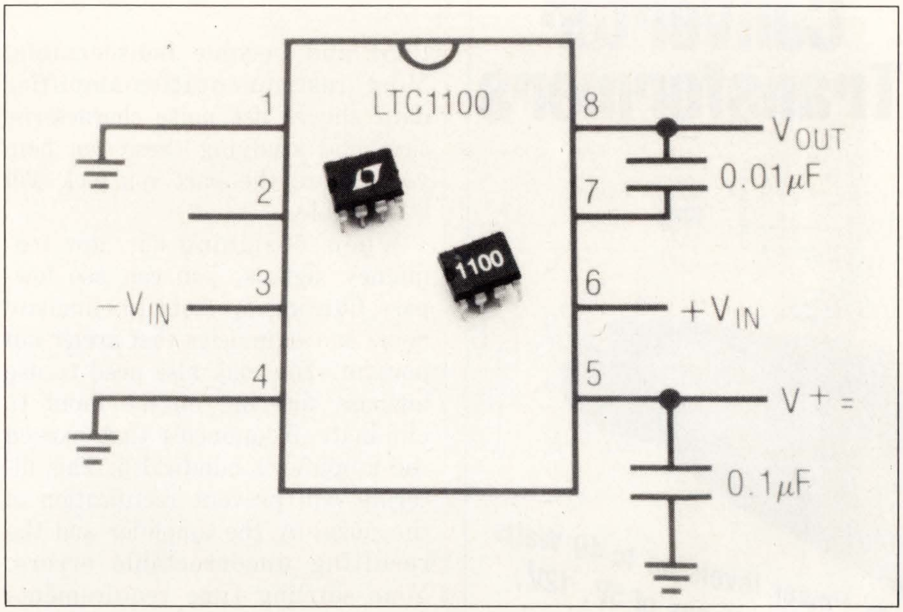
Select among gains of 1, 10, 100, and 1000 with a 2-bit digital word on Burr-Brown's PGA202. The PGA203 provides gains of 1, 2, 4, and 8.

Though your application may use only signals below 10 Hz, if you will be multiplexing different signals through an instrumentation amplifier, you may need a higher-bandwidth amplifier. Each time you switch the multiplexer to a different signal, you need to wait for the instrumentation amplifier's output to settle before you can take a reading. You must make sure the settling time of the amplifier is compatible with the time you'll spend on each signal. Higher-bandwidth amplifiers often have the faster settling time you'll need.

Instrumentation amplifiers are also useful in audio and other applications where frequencies of interest are above 10 Hz. In these higher-frequency cases, the ac performance becomes critical, and the dc performance often becomes secondary.

For audio applications, you may want to consider instrumentation amplifiers designed specifically for audio frequencies. You'll find these amplifiers characterized for specs important to audio, such as total harmonic distortion (THD). For example, Burr-Brown's INA103 has a typical THD plus noise of 0.0009% at 1 kHz and a gain of 100. PMI's (a division of Analog Devices) SSM2017 has a THD of less than 0.01% for audio frequencies while operating at a gain of 1000.

If you're amplifying low-amplitude signals such as soft musical passages, you'll often be concerned with the amplifier's noise. If the amplifier has too much inherent noise, your signal can sink into the noise



A maximum total offset of 10 μV makes the chopper-stabilized LTC1100 from Linear Technology a good candidate for high-accuracy applications. The 8-pin DIP version has a fixed gain of 100. The 16-pin surface-mount version offers gains of 10 and 100.

Put guards to work on sensitive signals

When working with low-frequency signals, you may elect to use a grounded shield around the input lines to reduce the noise pickup. The grounded shield causes a significant capacitive coupling of the signal-to-ground and low-pass signal filtering, especially if the signal source has a high output impedance. To reduce the signal's capacitance to ground, a guard driver can buffer the input signal to drive the shield (**Fig A**). Although the guard does nothing to reduce the capacitance to the shield, the signal and shield swing together, eliminating the voltage changes across the capacitance.

Note that the guard need not be the same voltage as the signal as long as the offset remains constant. The guard drivers provided on some instrumentation amplifiers are a diode drop away from the signal voltage.

Guards can provide another benefit, particularly on the surface of a pc board, by reducing leakage currents. A pc board that has become dirty provides leakage paths between nearby signals. If you surround the input signals to the instrumentation amplifier by a guard line at the same voltage as the inputs, all leakage will be between the guard and surrounding signals, having no effect on the input signal.

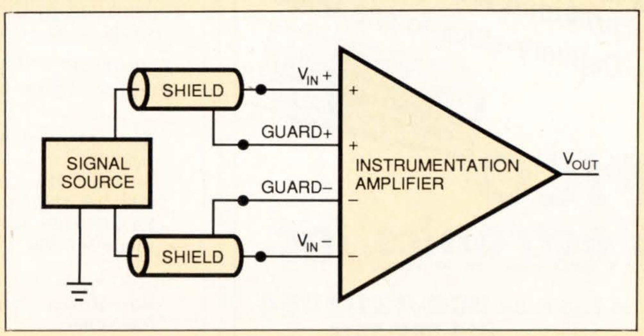


Fig A—Guard drivers available on some instrumentation amplifiers let you shield the inputs from noise yet avoid paying a penalty on input bandwidth due to capacitive coupling with ground.

floor and become indiscernible. Most instrumentation-amplifier data sheets list noise characteristics, and studying these can help you ensure the part you pick will be suitable.

When designing for low-frequency signals, you can use lowpass filtering up front to eliminate noise at frequencies that aren't important. You may also need to use lowpass filtering on the input to eliminate frequencies that exceed the amplifier's bandwidth. This filtering will prevent rectification of the noise by the amplifier and the resulting uncorrectable errors. Your settling time requirements will often dictate how low you can make the pass frequency.

Instrumentation amplifiers find use in amplifying differential signals, especially when common-mode voltages are present or you need to change the reference ground voltage to another ground. For instrumentation amplifiers, the grounds typically need to be within 10 to 30V of each other. When you need to change ground references, where potential differences are greater, you can use isolation amplifiers. Isolation amplifiers are hybrid circuits and more expensive than instrumentation amplifiers. However, they can operate with potential differences of hundreds or even thousands of volts.

Although instrumentation amplifier prices are just beginning to drop below the $5 level, the devices are still too expensive for many applications where they would otherwise be ideal. For example, when measuring current through a resistor, an instrumentation amplifier provides a simple way to obtain a voltage proportional to current, even when neither end of the resistor is at ground potential.

You can expect to see performance improvements in the future. Meanwhile, prices should continue to drop on new instrumentation amplifiers, so you'll be able to use them for all the applications where you need a differential input gain device. For high-performance applications, you can expect to see offsets improve, so you won't always need to trim them. EDN

Article Interest Quotient
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Manufacturers of monolithic instrumentation amplifiers

For more information on monolithic instrumentation amplifiers such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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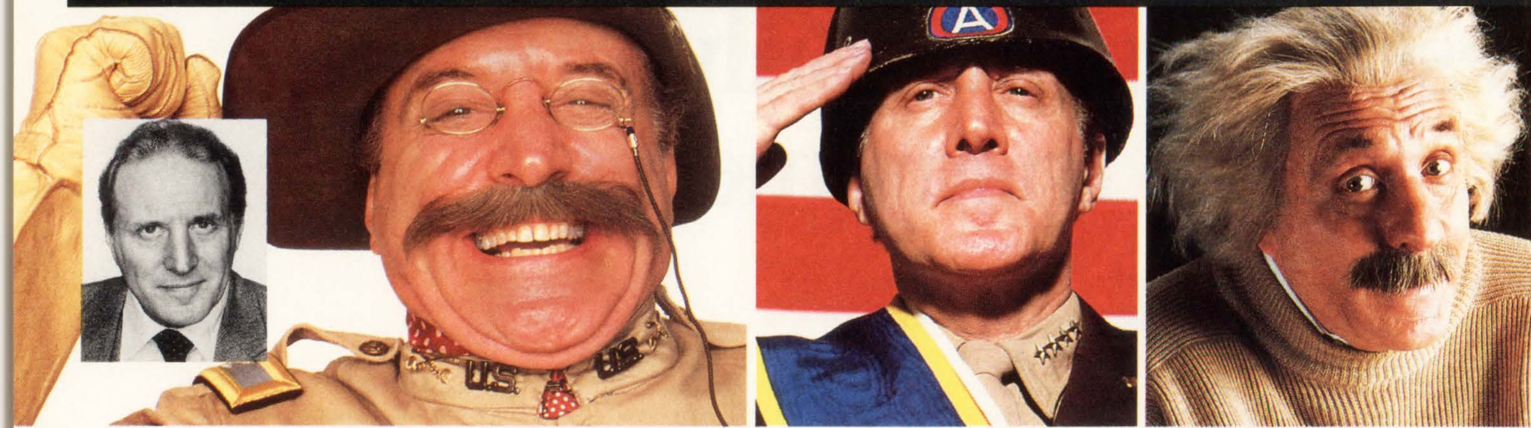
CIRCLE NO. 59

Multi Roles. One actor, many faces...



One power supply, many applications.

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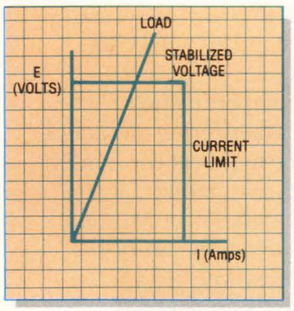
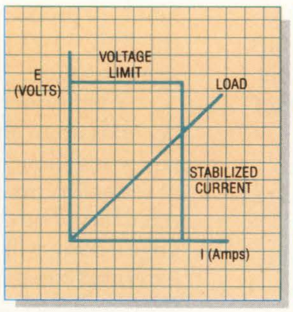
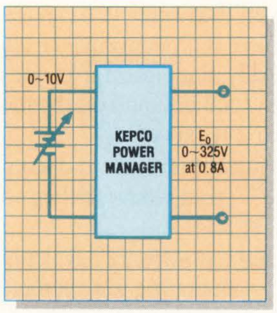


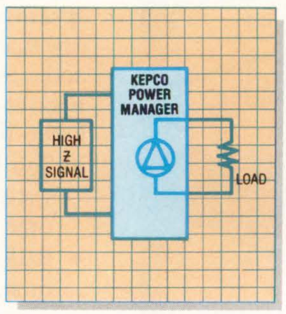
....SUPPLY STABILIZED VOLTAGE
0.001% voltage stabilizer



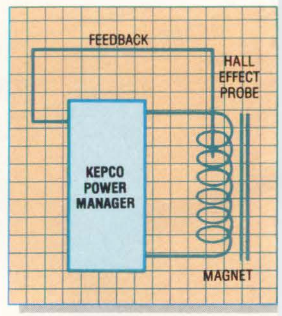
AND CURRENT.
0.005% current stabilizer



THEY'RE PROGRAMMABLE IN VOLTAGE MODE.
A voltage stabilizer controlled by a 0-10V d-c signal



THEY'RE PROGRAMMABLE IN CURRENT MODE.
A current stabilizer controlled by a high impedance source



THEY'LL ACCEPT FEEDBACK.
A magnetic field stabilizer controlled by a Hall-effect sensor

Model ATE 325-0.8M

The actor/model is *Jan Leighton*, whose face has been photographed as everyone from Patton to MacArthur to Lincoln. One face, many roles. More than 3,372 historical notables according to his fact sheet!

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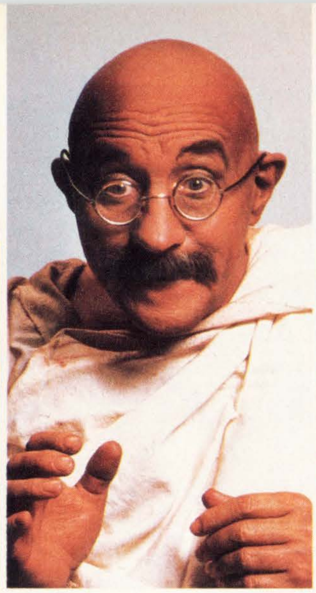
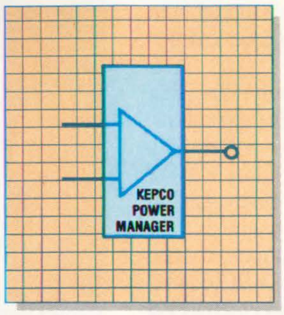
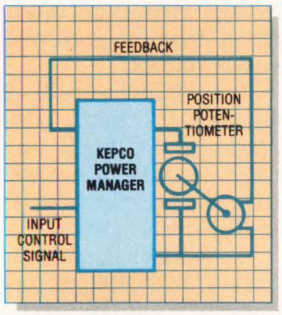
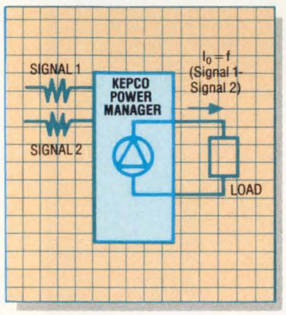




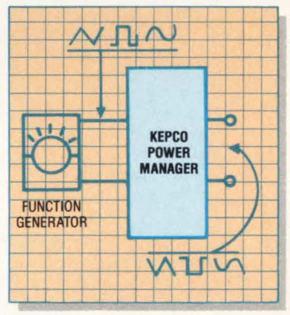
THEY'LL FUNCTION AS AN AMPLIFIER...
A self-powered oversized op-amp



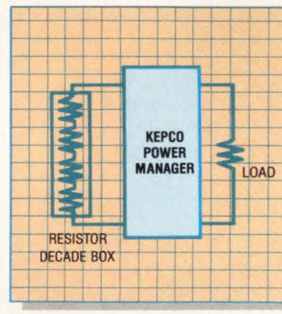
OR CONTROL A MACHINE.
A servo amplifier to drive a positioning motor



ATE CAN SUM INPUT CONTROL SIGNALS
A current stabilizer controlled by the difference between two signals



...BE DRIVEN BY AN ANALOG FUNCTION
A voltage stabilizer controlled by a signal generator



OR INTERFACE TO THE DIGITAL WORLD
A voltage stabilizer controlled by a passive resistance decade box

ATE are made in 5 power ranges, 50 to 1000W (voltage ranges 0-6V to 0-325V) to afford:

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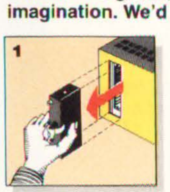
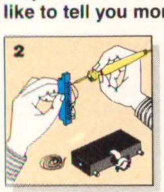
Most important... ATE's linear design supports a fast-programming mode which — for your control signals — allows a wide bandwidth response ... 16KHz in our 0-6V, 100 Ampere model, allowing roles ordinary power supplies cannot imagine.

- ☐ *Fast Recovery* current stabilizer
- ☐ *Wide band* power amplifier
- ☐ *Rapid response* to sequenced programs

Like Jan Leighton, Kepco's 41 different ATE models are capable of many roles, limited mainly by your imagination. We'd like to tell you more. ATE's unique user port allows you access to the principal control points. A simple 3-step procedure allows you to configure your ATE for whatever role you require.





By appropriate wiring of the mating plug, your ATE easily assumes a variety of roles: voltage/current controller, resistance programmed, voltage programmed, digitally programmed, power amplifier, servo amplifier, integrator.

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Create signals having optimum resolution, response, and noise

Simultaneously achieving fine frequency resolution, fast switching speed, and low phase noise is the hallmark of the signal-generation technique known as direct digital synthesis.

Earl McCune Jr, *Digital RF Solutions Corp*

Direct digital synthesis (DDS), also known as direct digital frequency synthesis (DDFS), is a newcomer to the toolbox of engineers who develop hardware for generating signals and waveforms. Because of component tolerances, value variations with time, and manufacturing inconsistencies, traditional analog techniques can only approximate a desired signal. In contrast, DDS calculates the signal directly.

DDS is known as a numeric—rather than a digital—technique. Two concerns account for this categorization: one technical, the other more marketing oriented. The technical reason stems from the direct calculations; the signal is actually generated by manipulating numbers. Although "digital" can have the same meaning as "numeric," digital can also refer to signals having (usually) two fixed amplitude levels. DDS does use techniques that are digital in both senses, but the two most important aspects of DDS are the numeric means it uses to represent quantities and the inherent precision that results from its use of numbers.

The marketing-oriented reason for calling DDS a numeric technique relates to the constraints imposed by traditional analog design. To maintain waveform inaccuracies of 0.1% or less (60-dB dynamic range), designers have avoided digital circuits. Such circuits have a reputation for generating noise currents that degrade signal purity in sensitive analog circuits nearby. With DDS, the digital circuits actually generate the analog signals. Using "numeric" rather than "digital" as the descriptor helps to dissociate DDS from digital circuits' unsavory reputation.

You can view DDS as an extension of digital signal processing (DSP) in accordance with the ideas presented in **Fig 1**. DSP has been around for many years. It is often used for filtering signals after an analog-to-digital conversion. DSP is also used to transform such digitized signals. For example, DSP techniques such as the FFT can transform a time-domain signal into an equivalent frequency-domain signal. These uses are

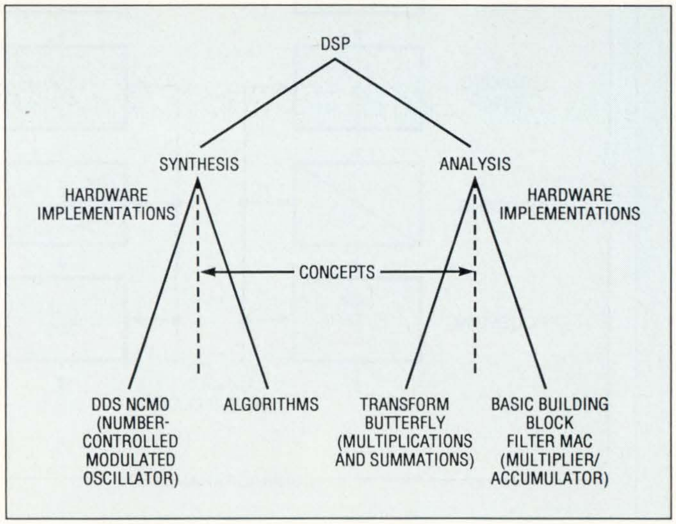

Fig 1—You can view DDS *as closely parallel to DSP. Both subject areas have sets of mathematical and hardware tools whose functions are intimately related.*

What is really important about DDS is the numeric means it uses to represent quantities and the inherent precision that results from its use of numbers.

analytical; they take an existing signal and change it.

Signal synthesis doesn't begin with an existing signal. DDS takes a small set of parameters (numbers) that describe the desired signal and generates a number sequence that represents the signal. This number sequence usually undergoes a digital-to-analog conversion to finally produce an analog signal. (See **box**, "The sampling theorem backwards.")

A major motivation for the development of DDS is achieving high accuracy at moderate cost. Calculators selling for $9.95 are accurate to 12 digits, whereas analog systems must incur large costs to maintain 0.1% accuracy—equivalent to three digits. By maximizing the use of digital techniques, DDS generates accurate analog signals inexpensively.

There are several ways to implement DDS. Where generating high frequencies is unnecessary—for example, in the voice band—you can implement DDS with general-purpose microprocessors. Low- and medium-speed phone-line modems have been built this way for years. As the required signal frequency increases above the audio range, the computing overhead for signal generation increases proportionally. Somewhere in the low RF (radio-frequency) range, the computing requirements become prohibitive even for modern, high-speed general-purpose μPs. At these higher signal frequencies, you should consider implementing DDS with dedicated hardware.

Dedicated DDS devices are optimized for signal synthesis. Their inputs are the signal parameters; their output is the desired signal. The control processor only needs to keep up with the signal parameters, not with the complete signal. The DDS device acts as a peripheral, freeing the main processor for other tasks.

Fig 2 shows the basic block diagram of a direct digital synthesizer. The DDS has three main blocks: the digi-

The sampling theorem backwards

Direct Digital Synthesis (DDS) obviously belongs to the synthesis side of Digital Signal Processing (DSP). There is no signal to be sampled or processed; rather, there is a sampled signal to be used. In this respect, DDS operates the sampling theorem in the reverse of the usual direction.

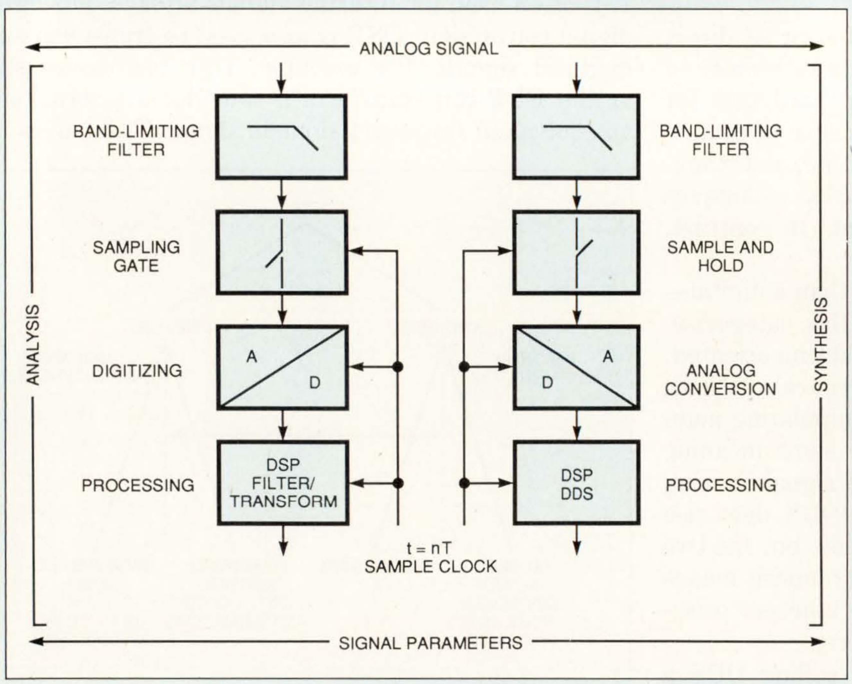

Fig A—Waveform analysis *using DSP and waveform synthesis using DDS involve similar operations. But DSP and DDS reverse the order of the operations.*

The left side of **Fig A** shows the sampling process as you would conventionally apply it in DSP. You must first band-limit the input signal with an anti-aliasing filter, after which the signal is sampled and digitized. The digitizer provides a number sequence that can be further processed to identify characteristic parameters.

With DDS, the characteristic parameters exist first. The number sequence is generated from these parameters and then converted into an analog waveform. The alias signals characteristic of a sampled signal are then removed with a band-limiting filter. The math is the same; the order of performing the operations is different.

tal accumulator, a waveform map, and the digital-to-analog converter. The input parameters are the signal frequency, represented by a number, and the timebase clock. The whole assembly is often called a number-controlled oscillator (NCO).

The objective of the NCO is to produce a signal s(t) according to the basic signal equation

$$s(t)=A\cos(2\pi\cdot f\cdot t). \tag{1}$$

To the NCO, f is the signal-frequency-number input parameter, and t is the time reference provided by the clock. The waveform map provides the sinusoidal cosine waveform and the digital-to-analog conversion sets the output-signal amplitude, A.

The argument of the cosine is the signal phase, which, for a fixed output frequency, must be a linear ramp. The digital accumulator generates this ramp. At every cycle of the clock, a phase increment corresponding to the desired output frequency is added to the existing phase value. At a particular output frequency, this increment will be fixed, and its repeated accumulation results in the desired ramp.

The accumulator is not a counter. The step size of a counter is fixed, usually at unity. For the digital accumulator, the step size corresponds to the signal-frequency number, f. This distinction will become important shortly in deriving the DDS tuning relationship.

Waveform map

If an NCO's output waveform is fixed as a cosine, a fixed ROM can implement the waveform map. Addresses in the ROM will represent the phase position within the output-signal cycle, and the data stored at each address will be the corresponding cosine amplitude.

Note that the waveform mapping is general. Maps can be made for disk read/write-head waveforms, nonlinear-phase signals, and even noise waveforms. A particularly special case is the operation of two waveform maps in parallel, one with a cosine and the other with a sine waveform. This technique provides absolute quadrature signals, which are required by many signal-processing and DSP applications.

The waveform map must operate at the full clock speed. Because the map follows the digital accumulator, each clock pulse provides different information to the map, and the map must settle completely within each clock period. If it doesn't do so, it will incorrectly convert the phase information from the digital accumulator to the corresponding amplitude value. For example, a 10-MHz clock requires the waveform map to have a cycle time of less than 100 nsec.

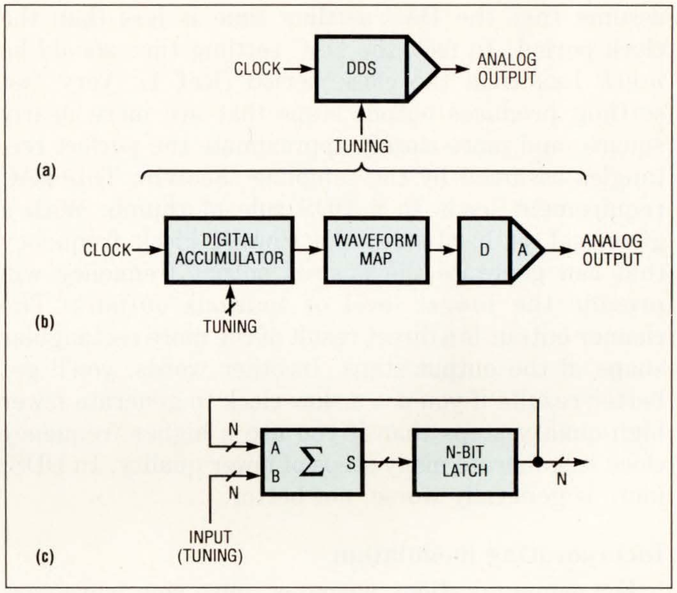

Fig 2—You can think of a DDS *as a single block* ***(a)*** *with digital and tuning inputs and an analog output. The more complex representation* ***(b)*** *more closely approximates the real nature of the DDS, and the 2-block representation of the digital accumulator in* ***c*** *suggests that the accumulator is more than a simple counter.*

The analog-conversion block takes the amplitude number sequence from the waveform map and converts it into a single analog signal. Today, a single-chip DAC usually performs this operation. Because the amplitude number sequence represents the actual, real-time samples that an accurate ADC would have generated from the desired signal, had the signal existed, the DAC output signal is the (re)constructed waveform of the desired signal.

In general, DAC devices are not designed for use in DDS (**Ref 1**). High-quality DDS output signals demand that the DAC not only have good static linearity, but also that its dynamic characteristics (slewing and settling) be well matched and controlled. A common fix for a DAC with unsatisfactory dynamic characteristics is to follow it with a sample-and-hold (S/H) circuit. Doing so replaces the DAC's dynamic characteristics with those of the S/H circuit, which are generally better. As the DAC manufacturers improve their products to meet the needs of high-quality DDS outputs, the use of S/H circuits in DDS will diminish.

Discussions of DACs in DDS applications generally

DDS takes a small set of parameters (numbers) that describe the desired signal and generates a number sequence that represents the signal.

assume that the DAC settling time is less than the clock period. In fact, the DAC settling time should be *much* less than the clock period (**Ref 1**). Very fast settling produces output steps that are more nearly square, and more closely approximate the perfect rectangles assumed by the sampling theorem. This DAC requirement leads to a DDS rule of thumb: With a given set of hardware, the slowest clock frequency that can generate the desired output frequency will provide the lowest level of spurious outputs. The cleaner output is a direct result of the more rectangular shape of the output steps. In other words, you'll get better results if you use a slow clock to generate fewer high-quality steps than if you use a higher frequency clock to generate many steps of lower quality. In DDS, more is generally worse, not better.

Incorporating modulation

For communications purposes, pure sine waves are essentially useless. To pass information along, you must modulate the sine wave in some way. A sine wave has three characteristics capable of modulation: amplitude, frequency, and phase. Including them in the general signal, **Eq 1** gives the general communications signal:

$$s(t)=A(t)\cos(2\pi\cdot(f+f_m(t))t+p(t)).$$

$A(t)$ represents amplitude modulation (AM), $f_m(t)$ represents frequency modulation (FM), and $p(t)$ represents phase modulation (PM). A DDS device that includes modulation capabilities is called a modulated NCO, an NCMO for number-controlled modulated oscillator, or an MNCO for modulated, number-controlled oscillator.

Interest in using continuous-phase signals to conserve output bandwidth is growing. A signal that does not have phase continuity will be discontinuous at its first derivative. Rapid changes in a waveform produce high-frequency sidebands, and a signal whose first derivative is discontinuous can have high-frequency sidebands that contain significant energy. The more of the signal's high-order derivatives that are continuous, the smaller the waveform's high-frequency content will be.

DDS is inherently a continuous-phase technique; its output-waveform calculation always proceeds from the present point, whether or not any parameter changes. Therefore, DDS completely eliminates switching transients, overshoot, and undershoot. By definition, phase modulation can produce phase discontinuities, but a modulated NCO can only approximate them. The modulated NCO approximates phase discontinuities by performing a large number of small phase steps in quick succession. Ideally, one of these steps should occur in every DDS clock cycle. You can purchase devices and hardware that phase-modulate at this rate (**Refs 2, 3,** and **4**).

Developing DDS designs

Frequency resolution is one of the primary issues of any synthesized-signal design. For DDS, you find the output frequency f_o from the relationship

$$f_o=(f_{clk}/K)\cdot M \text{ Hz}, \qquad (2)$$

where f_{clk} is the applied clock frequency, in Hz, M is the tuning number applied to the DDS, and K is the operating modulus of the DDS digital accumulator.

The clock frequency sets the DDS's sampling rate, which is the rate at which the DDS updates the signal-amplitude samples. In almost all cases, the sampling rate is equal to the frequency of the applied clock. The design of the DDS device determines the operating modulus, K, which equals the number of states that the accumulator can take on. Since most devices use binary circuits, K is usually a power of two such as 2^{24} or 2^{32}. When DDS devices use decimal circuits, K is a power of ten such as 10^6 or 10^8. A new technique called variable resolution (VR) lets you set K to any number between 1 and the digital accumulator's maximum intrinsic number of states.

The tuning number, M, is an integer between zero and K/2. The upper bound is called the Nyquist limit, a requirement from the sampling theorem to guarantee a unique output frequency. When $M=0$, **Eq 2** shows that the output frequency will also go to zero. Therefore DDS designs include dc within their tuning bandwidth. The frequency resolution of the DDS is the derivative of **Eq 2** with respect to M. This calculation gives the DDS resolution (f_{res}) as

$$f_{res}=f_{clk}/K. \qquad (3)$$

The frequency resolution is identical to the output frequency when $M=1$. Because M must be an integer, all output frequencies will be harmonics of the resolution given in **Eq 3**. For this reason, this resolution is occasionally called the DDS quantization frequency.

DDS frequency resolutions can be very small. As an example, consider a 24-bit binary DDS device operating with a 10-MHz clock. The 24-bit accumulator sets K to 16,777,216 and yields a frequency resolution of 10,000,000/16,777,216 = 0.59 Hz. Ease of achieving fine frequency resolution is a fundamental characteristic of the DDS. More bits give even finer steps.

Several applications require an exact frequency resolution, and have a single, high-precision reference frequency for the DDS clock. For these designs, a simple algebraic shift of **Eq 3** would be useful:

$$K = f_{clk}/f_{res}. \quad (4)$$

Such an approach would set the DDS modulus and the desired resolution exactly. The Variable Resolution (VR) technique accomplishes these objectives. If a design requires precise resolution, such as 2.85714 Hz or 0.100000 Hz, it must either supply a special clock frequency to the DDS according to

$$f_{clk} = K \cdot f_{res},$$

or use VR technology, according to **Eq 4**.

Synthesizer output bandwidth

As mentioned before, there is a maximum output frequency at which the tuning relationship of **Eq 2** holds. This frequency (the Nyquist frequency) is equal to one half of the applied clock frequency. As with most real designs, the practical upper limit is lower than the theoretical limit. For DDS, the practical upper limit lies around 40 to 45% of the clock frequency. This limitation holds not only for the tuned output frequency, but also includes the sum of any and all modulation sidebands above the carrier.

Output settling-time performance

The first D in DDS stands for direct, which means DDS designs do not use feedback to ensure output-frequency accuracy. This approach differs from the PLL approach, which depends on feedback to achieve output-frequency accuracy. The PLL must stabilize its feedback loop to effect any frequency change. Hence, changing the frequency of a PLL takes longer than the reciprocal of the PLL's bandwidth.

As soon as you change the applied-frequency number, M, a DDS starts using the new M value in its calculations. The DDS' pipeline depth (number of calculation stages) establishes the time required for the output signal to reflect this frequency change. If, for example, a DDS has a 10-MHz clock and 32 stages, it will require 3.2 microseconds. More efficient designs, using fewer stages, switch proportionally faster: With the same clock, a 6-stage DDS will settle in 600 nanoseconds. Hardware is readily available with 5 stages of registers from the applied tuning number to the DAC output. With a 10-MHz clock, such a design exhibits the same frequency agility (settling time) as a 32-stage design operating at 64 MHz.

Dealing with output alias signals

Because it is a sampled system, a DDS has a multiple-signal output spectrum. In addition to the desired output signal at f_o, there are output signals at each harmonic of the clock plus f_o. The output spectrum is therefore f_o, $f_{clk}+f_o$, $2 \cdot f_{clk}+f_o$, $3 \cdot f_{clk}+f_o$, etc. The additional signals, often referred to as alias signals, are mixing products of the output signal with the clock and all of its harmonics. These signals must be removed by lowpass filtering to leave only the desired f_o signal. This filtering is the reverse of the antialias filtering used ahead of ADCs.

To make the output filter realizable, the upper output frequency is nominally 40% of the clock frequency. As the upper output frequency approaches the Nyquist frequency from below, the alias frequency at $f_{clk}-f_o$ approaches the Nyquist frequency from above. The closer the upper output and alias frequencies get to each other, the more complex the output lowpass filter must become. If you try to make the output frequency exceed 40% of the clock frequency, the output filter quickly becomes impractical. For example, achieving 60 dB of alias rejection when the output frequency is 42% of the clock requires a Chebyshev lowpass filter with more than 20 sections. Realizing any analog filter of seven sections or more requires special care, but producing a filter with 20 sections is almost impossible.

At the output of the lowpass filter, analog signal (re)construction is complete. The signal can then be used directly, or additionally processed by such conventional analog techniques as amplification, mixing, limiting, and multiplication.

Determining output-signal quality

The cosine is a transcendental function, which the waveform map cannot quantize precisely. The quantization errors that inevitably exist produce signals in addition to the main signal and the alias terms. These nonharmonic extra signals are called DDS spurs. In a good DDS design, these spurs will be relatively low in amplitude—at least 60 dB below the main output.

There are three main blocks: the digital accumulator, a waveform map, and the digital-to-analog conversion.

In the best DDS designs, the spurs are 70 to 80 dB below the main output. If required, under some conditions, you can reduce the spurs even further.

When you tune the main signal, the DDS spurs generally move around much faster than the main signal does. You can predict the location of the spurs by modifying a technique used in analog systems with mixers (**Ref**s **5** and **6**). Near output frequencies that are integral submultiples of the clock ($1/3$, $1/4$, $1/10$, etc.), the spurs all "gather around" the main output. At exact integral submultiples of the clock, the spurs all cross over the main output. You can quickly check a DDS design's degree of spur generation by tuning the DDS to near the $1/3$- and $1/4$-clock-frequency crossovers. You can then directly evaluate the output spectrum quality from plots similar to those of **Fig** 3.

Construction hints for success

A DDS, by nature, uses digital circuits to perform analog functions. The absence of noise generation is essential for a successful design. High-frequency construction techniques are necessary. Clock frequencies are typically 10 to 50 MHz. On a standard pc board made from G-10 or FR-4 laminates, the shortest wavelength is about 270 cm. Transmission-line effects are not important here, because a typical DDS design covers 10 to 20 cm—under $1/10$ of a wavelength.

Loop currents are another matter. The DDS's digital circuits have edge speeds of less than 10 nsec. The currents these circuits produce have significant energy at 500 MHz or more. The signal current must flow from the driving IC's dc supply pin, through its output transistor(s), to the receiving IC's input pin, and back to the supply through the ground. **Fig 4** shows this current path.

Any signal transfer from one IC to another has three loop currents. The driving IC draws current from its supply pin to turn on an output-pin driver. Some of this current flows into the interconnection as signal current. The rest flows out the driving IC's ground pin to return to the supply.

The signal current flows to the receiving IC and draws a matching current from the IC as required to conserve charge. (Basic physics strikes again!) This return signal current flows from the receiving IC's ground pin, underneath the signal trace (if there is a ground plane there), and back to the driving IC to return to the supply.

A third loop current results from the effects of the signal on the receiving IC. The receiving IC will draw current from its own supply pin in response to the stimulus. This current will flow out of the IC's ground pin and will return to the power supply.

Good low-noise construction will guarantee that all of these currents flow in the smallest possible area. Radiation and other interference increases in direct proportion to the area enclosed by the conductors carrying these currents. Also, if more than one current flows in a conductor, the currents can interact. Careful layout of the pc board is essential to minimize signal-loop sizes and impedances common to several loops.

Current loops around each IC are a slightly different

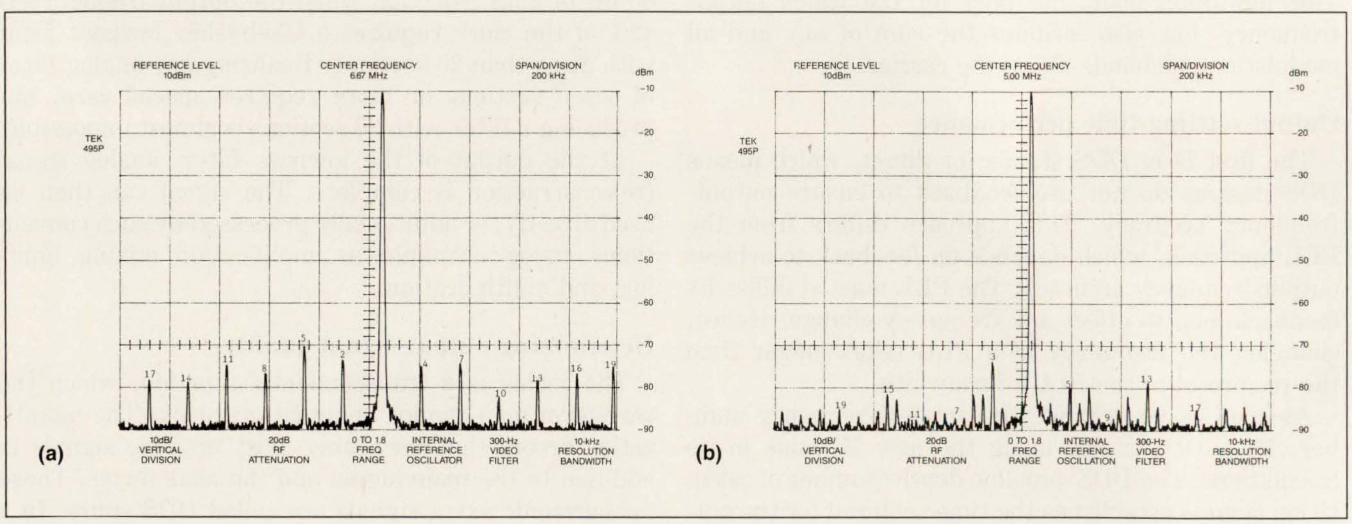

Fig 3—You can quickly check a DDS *design's degree of spur generation by tuning the DDS to near the $1/3$-* ***(a)*** *and $1/4$-clock-frequency* ***(b)*** *crossovers. Spectral plots such as these then readily reveal the spurs.*

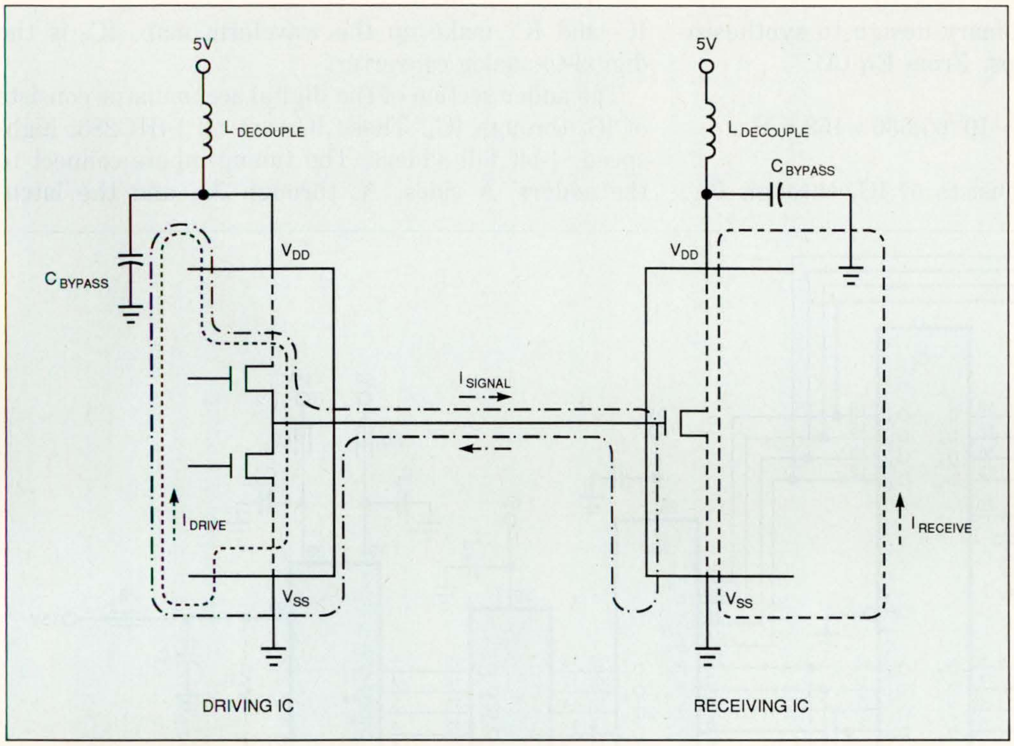

Fig 4—When one IC sends a signal to another, the currents that flow create electromagnetic fields. Understanding the current paths in signal leads and ground planes helps you to minimize the spurious signals generated by the changing fields.

matter. The bias component of the switching currents should never flow far from the IC—this is the idea behind the use of bypass capacitors. If the impedance of the bypass capacitor is lower than that of the power supply as seen by the IC power pin, the switching current will come from and return to the bypass capacitor (hence the name). Between switching transients, the bypass capacitor will recharge from the higher impedance supply. If there is no bypass capacitor, the IC will be forced to draw power from the power supply during the transient. Because power supplies are rarely right next to their loads, the loop-current path will enclose a large area. Radiation and interference will be severe.

Multilayer PC boards and surface-mounted components are a significant help in controlling these currents. A ground-plane layer immediately below the signal traces minimizes the signal-current path length. Surface-mounted bypass capacitors have lower lead inductances than do through-hole-mounted capacitors. Mounting these devices on the back of a pc board further reduces the length of the current path. Nevertheless, these modern components and construction techniques are mixed blessings. Besides costing more, they can cause problems with power distribution.

A bypass capacitor will work when its impedance, as seen by the IC's power pin, is lower than that of the power supply. By design, a power plane, like a ground plane, has a very low impedance. For the bypassing to control the transient loop current, there must be some impedance between the point where the IC draws current from the power plane and the junction of the IC's power pin and the bypass capacitor. This impedance can take the form of a ferrite bead or, if the dc current is low enough, a smaller chip inductor. A 470-nH inductance is a good value for this application. Without the series inductance, the bypassing is ineffective; the ICs draw energy directly from the low-impedance power and ground planes in a manner that makes control essentially impossible.

Fig 5 shows a simple DDS design using standard components. This synthesizer, which is useful as a general-purpose signal generator covering the audio and low-RF ranges, has the following specifications:

Output Frequency Range	0 to 4 MHz
Frequency Resolution	152.6 Hz
Spurious Signal Suppression	50 dB below carrier
Frequency Switching Time	<500 nsec

A 10-MHz crystal-reference frequency drives this sample design.

With a given set of hardware, the slowest clock frequency that can generate the desired output frequency will provide the lowest level of spurious outputs.

The DDS uses a 16-bit binary design to synthesize the required frequency steps. From **Eq (3)**

$$f_{res} = f_{clk}/K = 10\ \text{MHz}/2^{16} = 10^7/65{,}536 = 152.6\ \text{Hz}.$$

The digital accumulator consists of IC_1 through IC_6. IC_7 and IC_8 make up the waveform map. IC_9 is the digital-to-analog converter.

The adder section of the digital accumulator consists of IC_1 through IC_4. These ICs are all 74HC283, high-speed, 4-bit full adders. The tuning inputs connect to the adders' A sides, A_0 through A_3, and the latch-

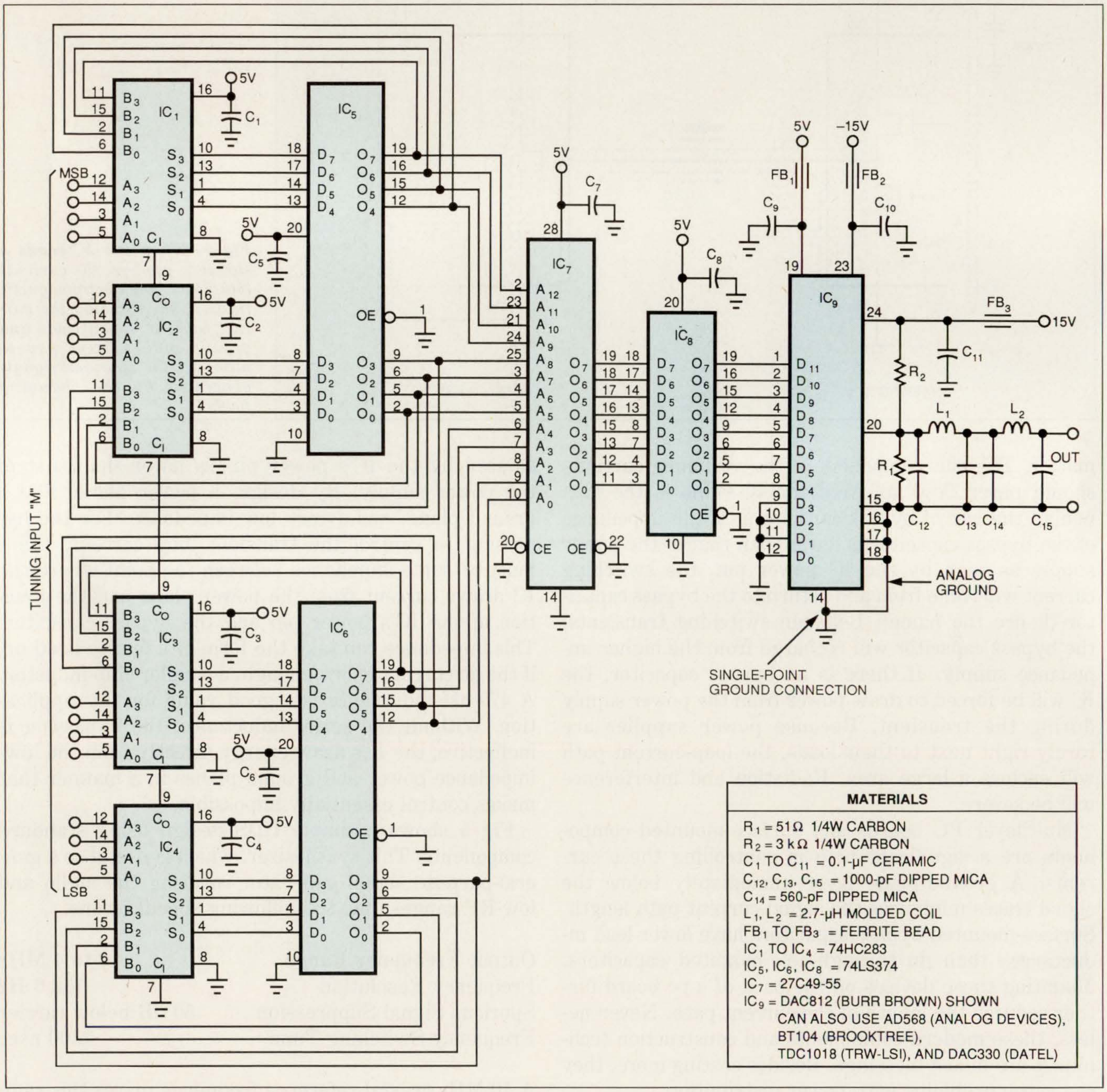

Fig 5—This 0- to 4-MHz DDS *uses nine readily available ICs. All of the other components are passive.*

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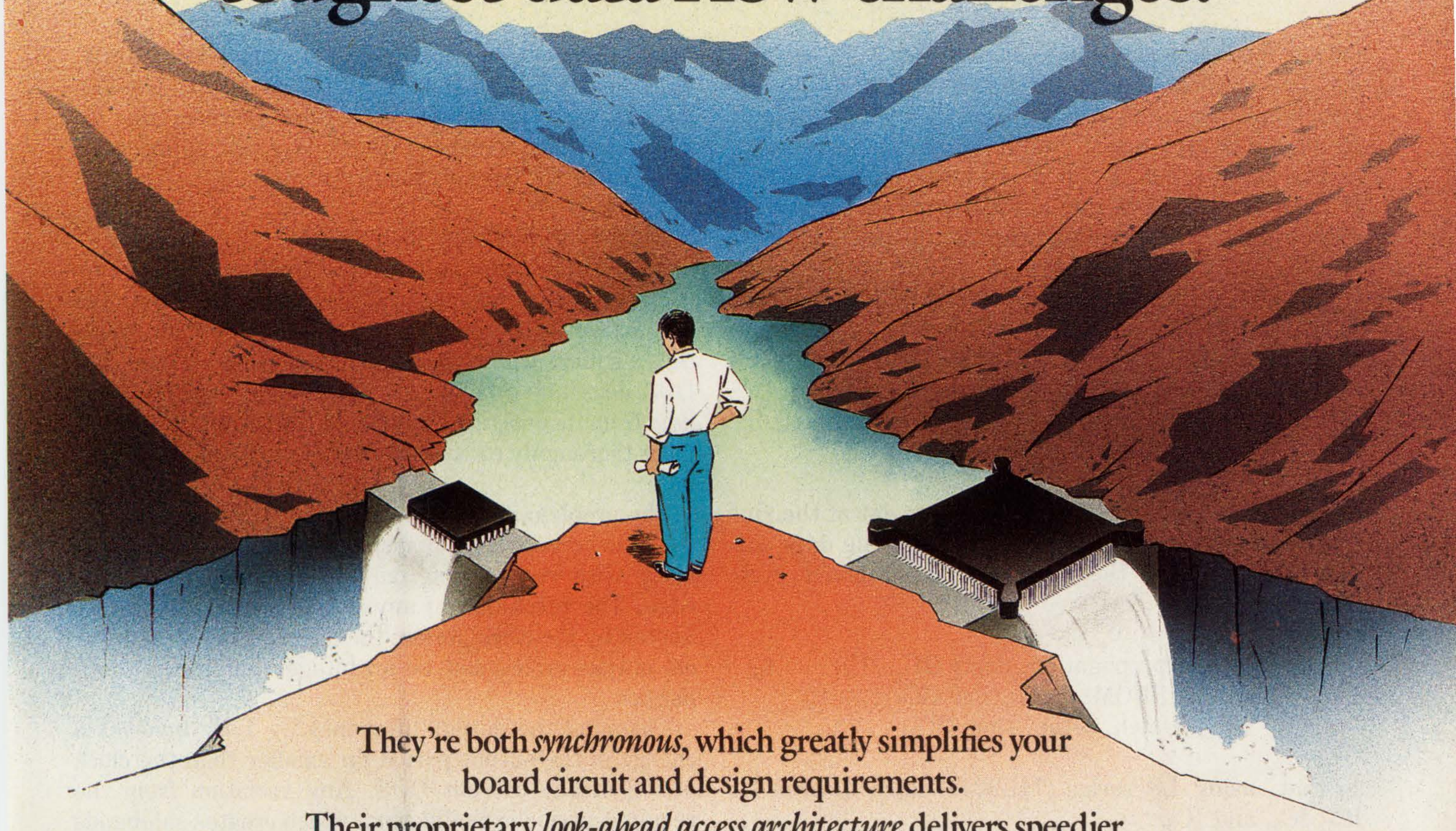

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The LH5492 4K x 9 clocked FIFO comes in a 32-pin PLCC. It is available with access times of 20 ns, 25 ns and 35 ns, and cycle times of 25 ns, 35 ns and 50 ns, respectively.

Introducing: The LH5420 256 x 36 x 2 Bidirectional FIFO.

Sharp's new LH5420 is actually two 256 x 36-bit FIFOs in one. Operating in parallel but opposite directions to provide bidirectional data buffering that would normally require multiple independent devices.

Its 36-bit word width is an industry first. And ideal for interfacing with new generation higher-speed 32/36-bit and 64/72-bit microprocessors and buses. Moreover, a choice of 9, 18, or 36-bit word widths on Port B means efficient word width matching.

Programmable Almost Empty and Almost Full status flags on each port—in addition to Full, Half Full and Empty flags—allow you to either leave the flags set at their initialized setting of 8, or program them over the entire FIFO depth.

The LH5420 comes in a 132-pin plastic QFP package. It is available with access times of 15 ns, 20 ns and 25 ns, and cycle times of 25 ns, 30 ns and 35 ns, respectively.

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DDS designs do not use feedback to ensure output-frequency accuracy. A PLL depends on feedback to achieve output-frequency accuracy.

output feedback connects to their B sides, B_0 through B_3. This arrangement is arbitrary, but it is easy to remember. To configure the four devices as a single 16-bit adder, the carry output of one stage connects to the carry input of the next-higher stage. Latches IC_5 and IC_6 complete the digital accumulator. The adder outputs drive the latch inputs: IC_1 and IC_2 drive IC_5; IC_3 and IC_4 drive IC_6.

The waveform map consists of PROM IC_7 and latch IC_8. The PROM contains 8k (2^{13}) bytes, so there are 13 address bits. The PROM contains a full sine wave calculated from

$$\text{data} = 127 \cdot (\sin(2\pi \cdot \text{address}/8192) + 1),$$

where 0<address<8191, and the argument of the sine function is in radians. Latch IC_8 retimes the data output. You can find the required PROM-device cycle time from

$$\begin{aligned}\text{clock\_period} = {} & \text{propagation\_delay } (IC_5, IC_6) \ldots t_{pd} \\ & + \text{PROM\_cycle\_time } (IC_7) \ldots t_{cy} \\ & + \text{latch\_setup\_time } (IC_8) \ldots t_{su},\end{aligned}$$

so that, using LS series (74LS374) latch devices for IC_5, IC_6, and IC_8,

$$\begin{aligned} t_{cy} & < T_C - t_{pd} - t_{su} \\ & < 100 - 25 - 20 \text{ nsec} \\ & < 55 \text{ nsec.}\end{aligned}$$

Faster latch devices will allow correspondingly longer PROM cycle times. For this example, a PROM device of type 27C49 through 27C55, or a similar part, permits 10-MHz operation.

IC_9 performs digital-to-analog conversion. Several devices meet the requirements of this function; the Burr-Brown DAC812 is shown. This device settles to 12-bit accuracy in less than 50 nsec, about half of the clock period. R_1 converts the 0- to 10-mA DAC output current to a voltage and also sets the output impedance of the DAC. A resistance of 50Ω matches the conventional line impedance of RF circuitry. Resistor R_2 injects a 5-mA current into the DAC output node to center the DAC output range around zero.

The 5-section LC, lowpass filter removes the output-signal alias terms. The component values produce a Chebyshev filter with 0.1 dB of passband ripple and a cutoff frequency of 4 MHz in a 50Ω system.

Thus, designing the filter completes the synthesizer's design. The output signal power is nominally 0.5 mW, which is 5 dB less than 1 mW (−5 dBm). The frequency-switching time is two clock periods, that is, 200 nsec. The measured spurious-signal suppression is −52 dBc (52 dB less than carrier level).

Square-wave time-base generator

Many applications do not require sine waves. In timing applications, square waves are all you need. Because DDS is a digital technique, you would expect that a square-wave output would be natural. Alas, the DDS does not produce a square wave without some help from its designer. The reasoning, which is covered more thoroughly elsewhere (**Ref 7**), is only summarized here.

The problem stems from the fact that a DDS design is a synchronous digital system. Its state will change, along with any output, only in response to a clock edge. The resolution of any output cycle is therefore limited by the clock period: the duration of any individual output cycle must be an integer number of clock periods.

Changing the output frequency by 1 Hz involves a change in the output period far smaller than the clock period of any current DDS. Any variation from the required period is modulation, which creates sidebands and spurs. Because the time quantization is too coarse to achieve the necessary signal quality, interpolation is necessary. The DDS output lowpass filter (LPF) performs the interpolation. Because the LPF is built from fixed components, it qualifies as an LTI (linear, time-invariant) network—a concept from early circuit-analysis classes. LTI networks have a "natural frequency" which is sinusoidal; you obtain the highest quality output signals by driving the filter with sinusoidal signals. This purpose underlies the cosine waveform map and the DAC. To effectively filter the phase information, you must make the LPF as "happy" as possible. The LPF will then perform the required time interpolation and yield a clean signal. But it is a sine wave. To make it square, you must employ amplitude limiting, usually with a comparator of some sort.

Fig 6 shows a wideband clock generator built with DDS. Note that this design creates a square wave by limiting a sine wave's amplitude. From a 50-MHz clock, this generator will provide a direct square-wave output from dc to the limit of the LPF, probably around 20 MHz.

At low output frequencies, the jitter on the DDS square-wave output is less objectionable than it is at

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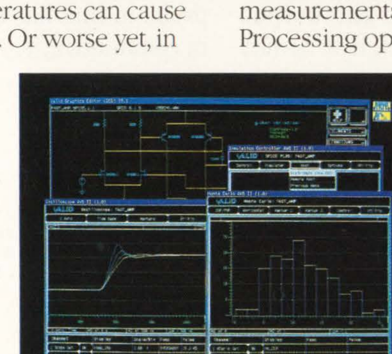

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If you try to make the output frequency exceed 40% of the clock frequency, the output filter quickly becomes impractical.

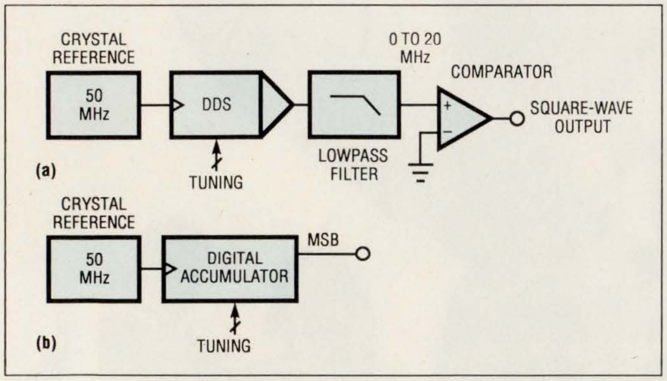

***Fig 6—To obtain a high-quality** square wave over a broad range of frequencies, you must have the DDS generate a sine wave. Then you must filter out the harmonics and limit the sine wave's amplitude, as in **a**. But if you are interested only in low-frequency square waves and you can tolerate moderate jitter, the DDS's digital accumulator alone may suffice, **(b)**.*

high frequencies. If you need only a low-frequency output, you need not generate a sine wave and limit its amplitude to produce a square wave. **Fig 6b** shows an implementation that dispenses with sine-wave generation and amplitude limiting. With a strict limitation on its bandwidth, the direct output exhibits tolerable jitter, according to:

$$f_{max}, \text{ direct square wave} = f_{clk} \cdot \%\_\text{jitter}/2.$$

This example uses a 50-MHz clock. Square waves with 0.1% jitter are directly obtainable from dc to 25 kHz. If you increase the jitter tolerance to 1%, the output bandwidth can increase to 250 kHz. Though it is not very efficient as square-wave generators go, this DDS design would be small and exceedingly stable.

Arbitrary output waveforms are possible, as mentioned earlier, by changing the information in the waveform map. **Fig 7** shows two common ways to change this information; real-time map changes are possible. Through the use of a dual-port RAM, a computer can insert changes to the waveform as the DDS operates. A generator with such an architecture can produce high-quality speech and is suited to any application that requires a large number of waveforms.

If the number of different waveform types is relatively small, a single PROM can hold them all. An external processor can select the desired waveform with the upper address bits. A typical application of this type is in testing of disk-drive read circuits. The PROM holds proper waveforms for positive and negative flux transitions as well as several types of problem waveforms for each transition direction. The processor can supply the circuit under test with normal waveforms, occasionally insert a particular error, and then return to normal operation. Digital buses and communications links are testable in a similar way.

Direct Digital Synthesis is a real technology, well beyond the experimental stage. DDS devices and subassemblies are available today from several manufacturers. Because DDS does not rely on feedback, it can simultaneously realize small frequency steps, fast frequency switching, and low phase noise. Careful construction techniques have solved the spurious-signal problem that has traditionally limited DDS applications in communications systems. Hence, the doors are open

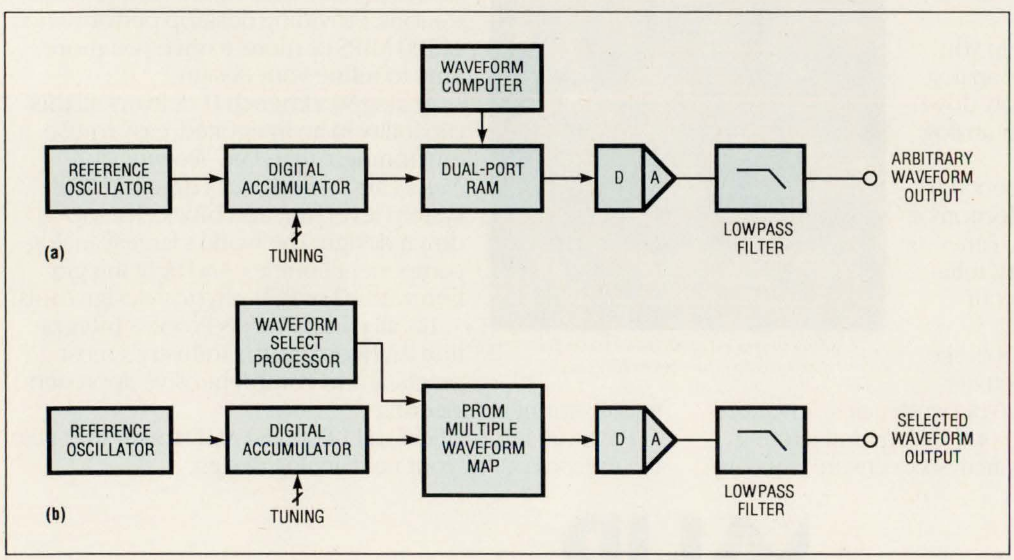

***Fig 7—Obtaining arbitrary waveforms** from a DDS can involve using a dual-ported memory and feeding it new waveform maps on the fly, **(a)**. For less demanding applications, a ROM can store several waveform maps, **(b)**, and the MSBs of the ROM address can determine which waveform the DDS produces.*

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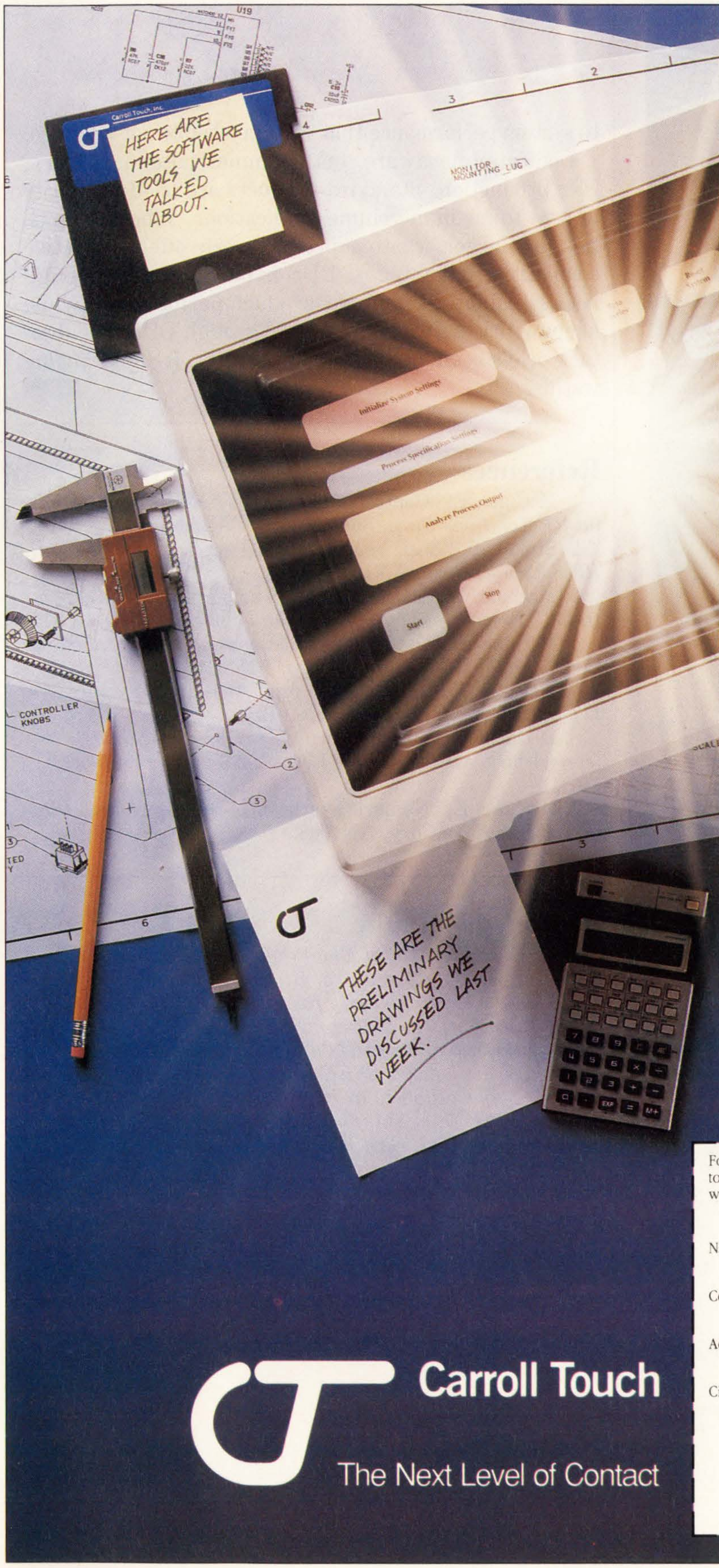

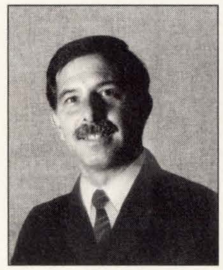

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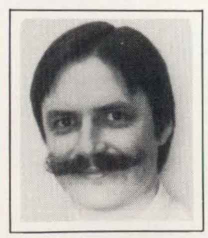
Author's biography



Earl McCune Jr is VP of Engineering at Digital RF Solutions Corp. He has been with the firm for nearly five years and has developed module- and board-level synthesizers using DDS and other techniques. He holds a BSEE from the University of California at Berkeley and an MSEE from Stanford University (Stanford, CA). Earl is a member of IEEE. His leisure activities include hiking, bicycling, and working with model aircraft.

Article Interest Quotient (Circle One)
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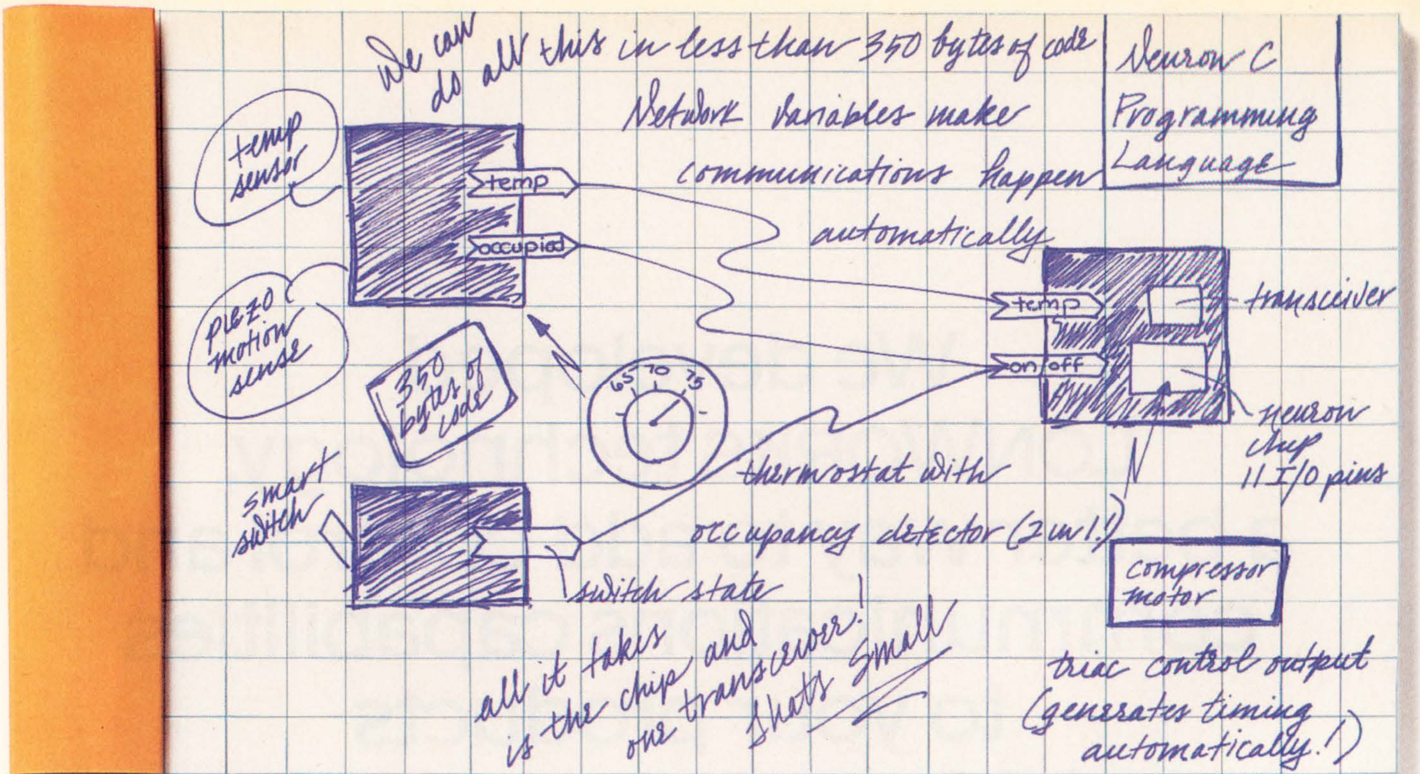
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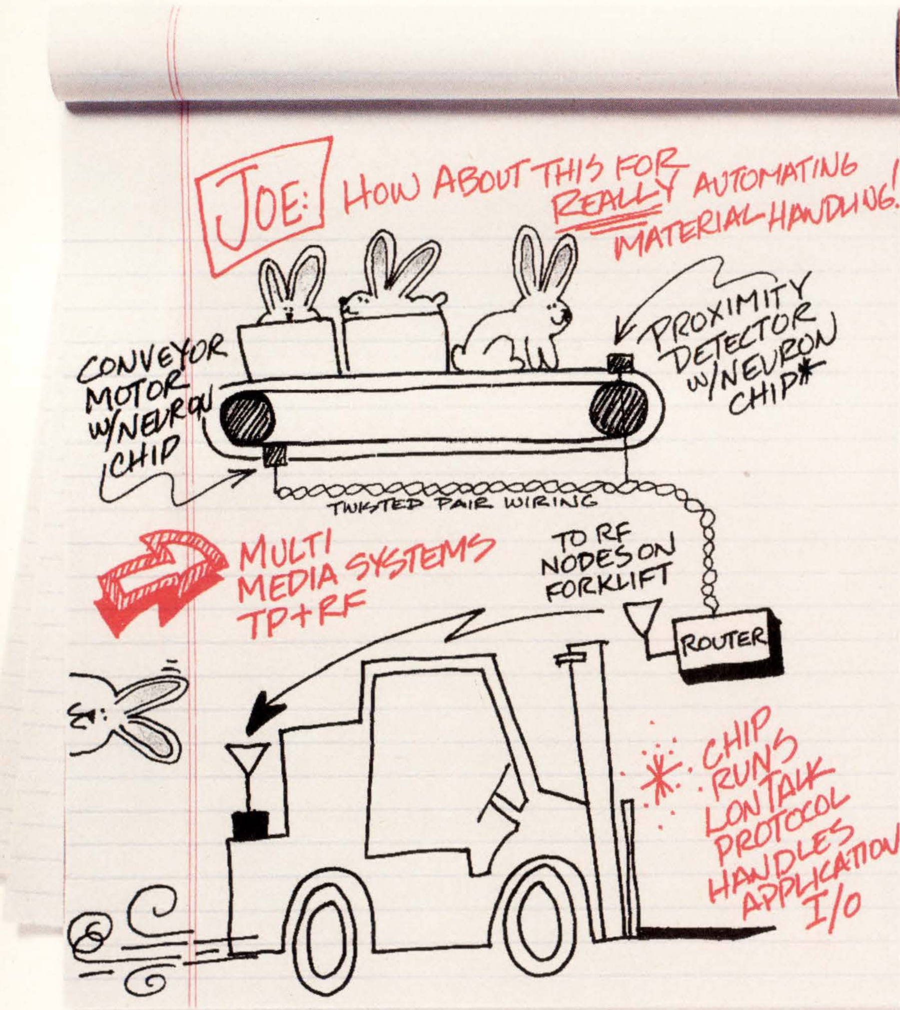
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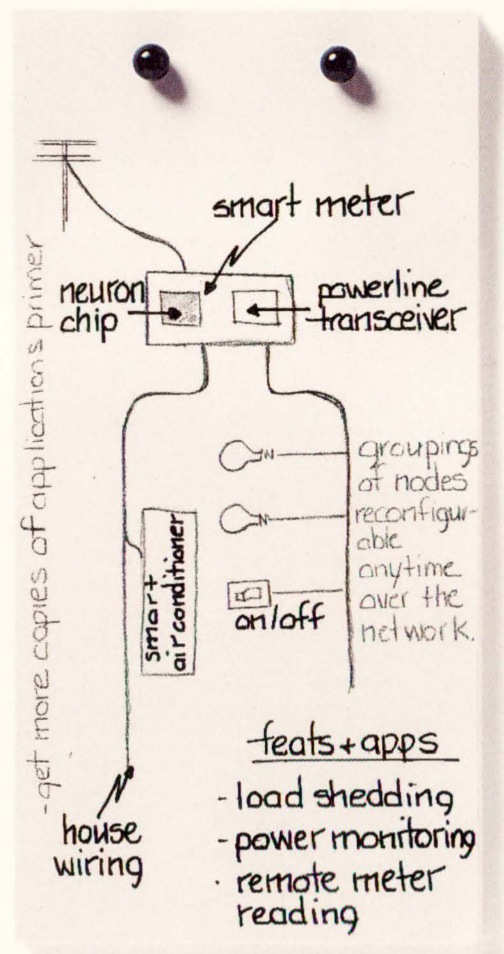
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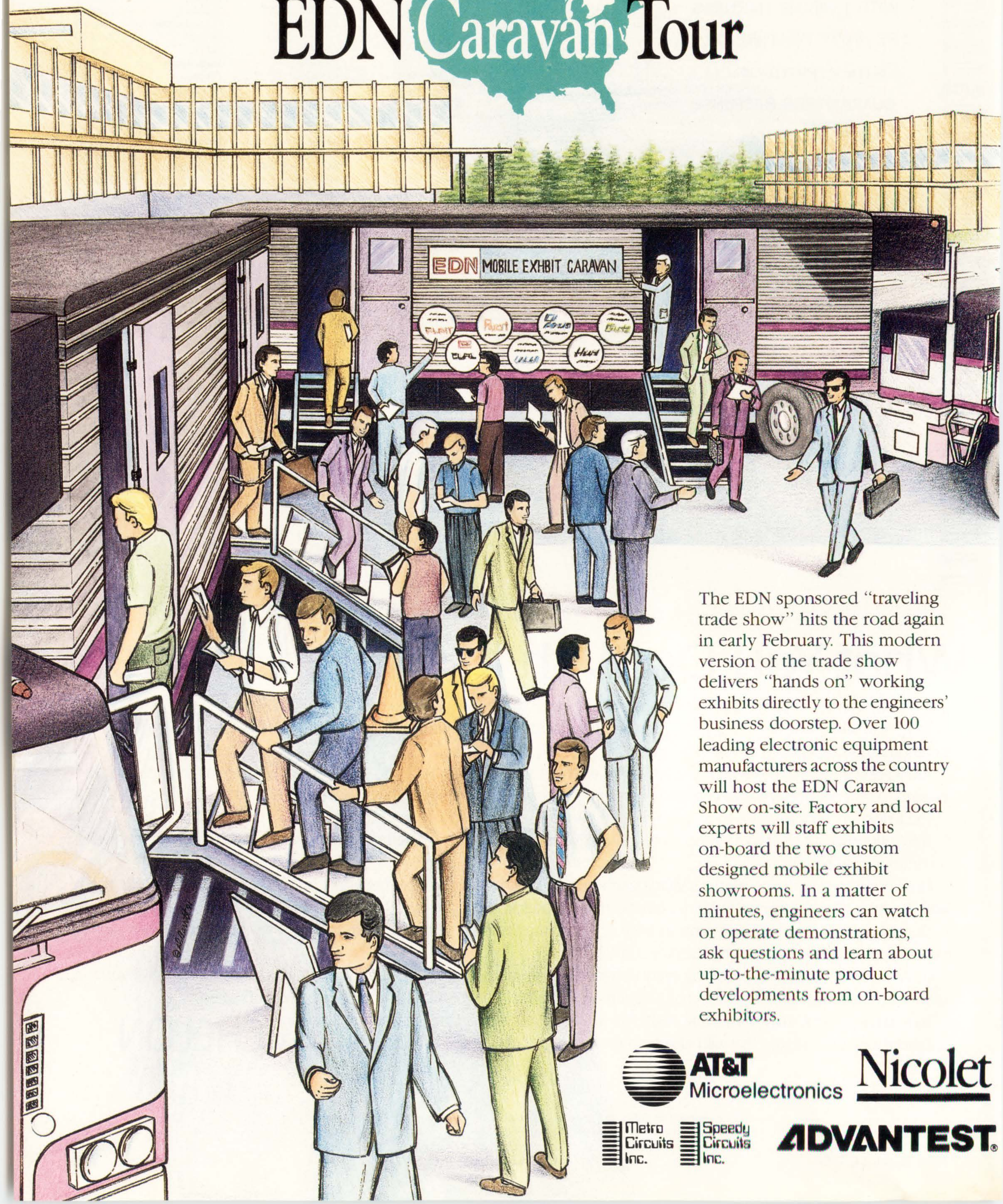

The EDN sponsored "traveling trade show" hits the road again in early February. This modern version of the trade show delivers "hands on" working exhibits directly to the engineers' business doorstep. Over 100 leading electronic equipment manufacturers across the country will host the EDN Caravan Show on-site. Factory and local experts will staff exhibits on-board the two custom designed mobile exhibit showrooms. In a matter of minutes, engineers can watch or operate demonstrations, ask questions and learn about up-to-the-minute product developments from on-board exhibitors.

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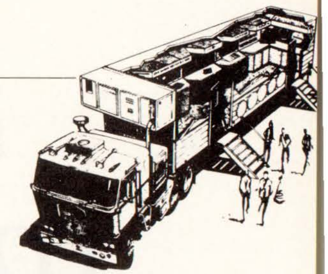

DATE	TIME	SITE
4/1 Monday	9:00-12:00 AM	SANDIA NATIONAL LABORATORIES Kirkland Air Force Base, Albuquerque, NM
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4/2 Tuesday	9:00-12:00 AM	LOS ALAMOS NATIONAL LABORATORIES Albuquerque, NM
4/3 Wednesday	9:00-11:30 AM	DIGITAL EQUIPMENT CORPORATION 301 Rockrimmon Blvd., So., Colorado Springs, CO
4/3 Wednesday	2:00-3:30 PM	METRUM INFORMATION SYSTEMS 4800 East Dry Creek Road, Littleton, CO
4/4 Thursday	9:00-11:30 AM	AT&T BELL LABORATORIES 11900 N. Pecos St., Denver, CO
4/4 Thursday	1:30-4:00 PM	BALL CORPORATION 1950 33rd St., Boulder Ind. Park, Boulder, CO
4/5 Friday	8:00-4:00 AM-PM	MARTIN MARIETTA ASTRONAUTICS (three sites) 12250 So. Highway 75, Denver, CO
4/8 Monday	9:00-11:00 AM	BEECH AIRCRAFT CORPORATION 9709 E. Central, Wichita, KS
4/9 Tuesday	9:00-11:30 AM	SEAGATE TECHNOLOGY 10323 W. Reno Avenue, Oklahoma City, OK
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4/10 Thursday	1:30-3:30 AM	TEXAS INSTRUMENTS, INC. Forest Lane, Dallas, TX
4/11 Thursday	9:00-11:30 AM	ROCKWELL INTERNATIONAL Shiloh & Renner Rd., Richardson, TX
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4/12 Friday	8:30-11:00 AM	E-SYSTEMS INC. 1570 Farm Road, Greenville, TX
4/12 Friday	12:30-3:30 PM	E-SYSTEMS INC. 1200 Jupiter Road, Garland, TX
4/15 Monday	9:00-12:00 AM	COMPAQ COMPUTER CORPORATION 20555 FM 149, Houston, TX
4/15 Monday	1:30-3:30 PM	COMPAQ COMPUTER CORPORATION 20555 FM 149, Houston, TX
4/16 Tuesday	9:00-11:30 AM	IBM CORPORATION 11400 Burnet Road, Austin, TX
4/16 Tuesday	1:00-3:00 PM	TEXAS INSTRUMENTS, INC. 12501 Research Blvd., Austin, TX
4/17 Wednesday	9:00-11:30 AM	DELL COMPUTER CORPORATION 9505 Arboretum Blvd., Austin, TX
4/17 Wednesday	1:00-3:00 PM	TRACOR, INC. 6500 Tracor Lane, Austin, TX
4/18 Thursday	9:00-11:00 AM	ELECTROSPACE SYSTEMS INC. 1301 E. Collins Road, Richardson, TX
4/18 Thursday	12:00-1:30 PM	CONVEX COMPUTER CORPORATION 701 N. Plano Road, Richardson, TX
4/18 Thursday	2:30-4:00 PM	DSC COMMUNICATIONS 1000 Coit Road, Plano, TX
4/19 Friday	9:00-11:30 AM	TEXAS INSTRUMENTS, INC. 2501 W. University, McKinney, TX
4/19 Friday	1:00-3:00 PM	TEXAS INSTRUMENTS, INC. 6500 Chase Oaks Blvd., Plano, TX
4/22 Monday	9:00-11:30 AM	BENDIX KING CORP. 400 N. Rogers Road, Olathe, KS
4/22 Monday	12:30-2:30 PM	ALLIED SIGNAL AEROSPACE 2000 E. 95th Street, Kansas City, MO
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4/23 Tuesday	11:30-1:00 AM-PM	EMERSON ELECTRONICS & SPACE 8100 W. Florissant Ave., St. Louis, MO
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4/25 Thursday	9:00-11:30 AM	NORTHROP CORPORATION, Defense Systems 600 Hicks Road, Rolling Meadows, IL
4/25 Thursday	12:30-3:00 PM	MOTOROLA, INC., Cellular Group 1501 W. Shure Drive, Arlington Heights, IL
4/26 Friday	8:30-11:00 AM	ZENITH ELECTRONIC SYSTEMS 1000 Milwaukee Avenue, Glenview, IL
4/26 Friday	12:30-2:30 PM	MOTOROLA, INC., Automotive & Industrial Elex. 4000 Commercial Avenue, Northbrook, IL
4/29 Monday	9:00-11:30 AM	ROCKWELL INTL', Commercial Avionics 400 Collins Road N.E., Cedar Rapids, IA
4/29 Monday	12:00-1:30 PM	ROCKWELL INTL', Collins Defense Communications 855 35th Street N.E., Cedar Rapids, IA
4/29 Monday	2:15-3:30 PM	ROCKWELL INTL', Collins Defense Communications Collins Road — Bldg. 153, Cedar Rapids, IA
4/30 Tuesday	9:00-11:30 AM	IBM CORPORATION Highway 52 So. & NW 37th St., Rochester, MN
4/30 Tuesday	2:00-4:45 PM	ROSEMOUNT, INC. 12001 Technology Drive, Eden Prairie, MN
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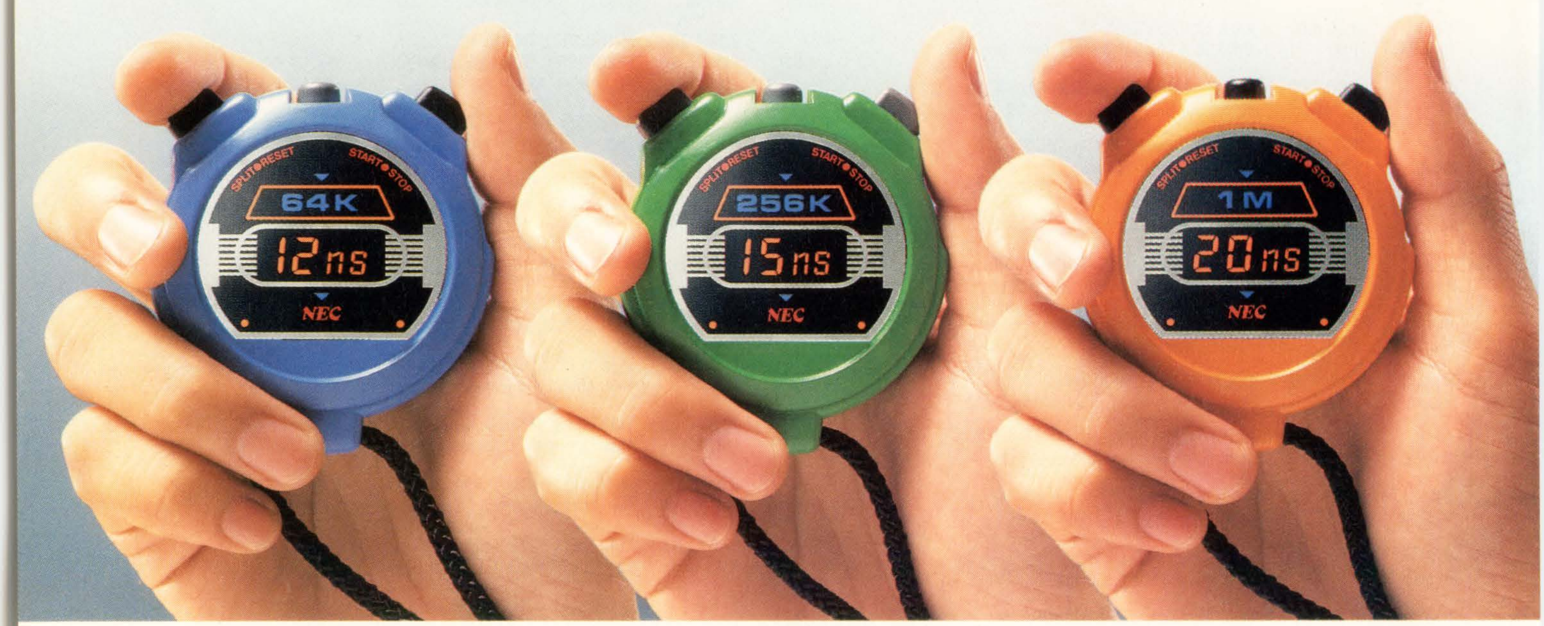

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72K	4369	8K x 9	15/20	DIP/SOJ
256K	43251B	256K x 1	15/20/25	DIP/SOJ
	43254B	64K x 4	15/20/25	DIP/SOJ
	43253B	64K x 4 OE	15/20/25	DIP/SOJ
	43258A	32K x 8	15/20/25	DIP/SOJ
	43250A	32K x 8 (with parity check)	15/20/25	DIP/SOJ
288K	43259A	32K x 9	15/20/25	DIP/SOJ
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CIRCLE NO. 50

Choose PC software or scientific calculators to tame tough math

For less than $400 you can get a top-of-the-line scientific calculator or an IBM PC software package that will solve a wide range of your engineering math problems. The calculators are more portable; the programs are more powerful. All have a lot of capability.

Richard E Douglass, *Consultant*

For engineering computations from basic trig to matrix math and more, you can turn to a variety of software packages and engineering/scientific calculators for assistance. I recently compared some typical computational tools—four software programs and four calculators—that provide many of the features an electronics engineer might want. The calculators and software aren't direct competitors, but they illustrate the capabilities that are now available for a modest amount of money. All of the tools reviewed have a list price of less than $400.

The four calculators I chose are the Hewlett-Packard HP 48SX, the Texas Instruments TI-81, the Sharp PC-E500, and the Casio fx-8000G. All are their manufacturers' top-of-the-line models. The Sharp and the HP are actually small computers, but I call them calculators to emphasize their portability.

The software packages I chose are SoftWarehouse's Derive (Release 1.58), Universal Technical Systems Inc's TK Solver Plus (Release 1.1), MathSoft Inc's MathCad 2.5, and Borland International's Eureka 1.0. All the programs run on IBM and compatible PCs under MS-DOS. Selection criteria for this review included a less-than-$400 list price; other packages are available that are more expensive and perhaps more capable.

(Ed note: After this review was prepared, SoftWarehouse released a new version of Derive. Derive 2.0 has expanded and extended capabilities for programming, equation solving, matrix operations, calculus, numerical methods, plotting, and user interfaces. The program's documentation was substantially improved. We regret that this review could not cover these recent additions.)

It is still generally true that calculators are more portable than computers and better suited for immediate calculations that might be required in meetings or while traveling. Computers generally provide more computational power than calculators. Nevertheless, the gap between calculators and computers becomes smaller every year; therefore, I've attempted to evaluate calculators and software packages on the same features; those useful to a working engineer.

The types of features covered in the comparison ta-

Calculators are more portable, but computers provide more options. The differences become smaller every year.

bles (**Tables 1** through **19**) indicate the range of capabilities of these tools. These features include

- scientific calculator functions
- data storage and recall
- user-defined functions
- complex mathematics
- vector mathematics
- matrix mathematics
- statistical calculations
- numerical solution of equations
- symbolic algebra and calculus
- reference formulas and constants
- unit conversions
- graphics and graphical analysis
- programming features
- text entry and edit
- clock functions
- printer interface
- mass-storage interface
- computer interface.

"Report Card" shows grades

Table 1 lists a very brief summary of the tools, including price information and grades (from A to F, as in school) for overall capabilities and ease of use. The grades summarize my opinions about the quality of the tools. Therefore, there is, of course, a degree of subjectivity involved.

A very important factor in ease of use is the "intuitiveness" of the command structure. You can use some of the tools, at least for simple tasks, without reading the documentation. Others are difficult to use even after studying the manuals.

Other ease-of-use factors are the number of keystrokes required to accomplish a given job and the availability of on-line help. Finally, and probably most important to ease of use, is the quality of the documentation package.

As I began reading the calculators' and programs' documentation, I was surprised at how difficult it was to determine which tools have which features. In many cases, I found myself experimenting with a tool just to determine if a particular feature was available. So I apologize if I've failed to list some products' features, but if a feature isn't listed in a tool's documentation index, then the tool's manufacturer must share the blame with me.

Several factors contribute to the ease or difficulty in using these tools' documentation (**Table 2**). Two inseparable ones are the completeness of the description of operations and the completeness of the index. A tutorial section that groups operations by function is helpful, as is a reference section that lists operations in alphabetical order.

The Casio calculator's documentation doesn't contain an index. I am immediately turned off by a manual without an index, no matter how complete the table of contents is. On calculators as powerful and complex as those reviewed here, each key typically serves multiple functions. It is important that the documentation make these functions clear.

Table 3 summarizes the tools' most basic features. All of the tools can perform the functions of a simple scientific calculator. All the tools use algebraic data entry, except the HP calculator, which uses Reverse Polish (except for symbolic equations). (As an aside, I prefer Reverse Polish, but I find algebraic entry much more acceptable on a multiline screen.)

The number of memory cells addressable by calculator commands of the type STO A (to store a value in memory register A) varies among the tools. The Sharp calculator provides substantial additional memory that certain functions can address. The HP calculator and the four software packages assign variable names to values (for example, NUM=4). The number of storage locations is limited by total available memory. I found the HP method quite clumsy (it required too many key strokes) compared to the others.

I had difficulty determining the arithmetic precision used by most of the tools for internal computations; the table entries are my best guesses after gleaning the documentation.

Menus or marked keys

Intrinsic functions (**Table 4**) are those frequently provided by special function keys on a scientific calculator, or are otherwise built into the tool. The TI and HP calculators provide math menus, as opposed to special function keys, for some functions. Math menus require a few more key strokes and are, therefore, a little less convenient to use. The computer programs typically access these functions by direct commands, such as Y=sin(30), followed by a SOLVE or PRINT Y command.

The ability to define and analyze functions is one of the most important capabilities of these tools, second only to the basic calculation functions. All the tools let you define functions of one or more independent variables for subsequent graphing, numerical evaluation, and analysis. The tools differ in the types of mathemati-

Math tools in summary

The four calculators and the four PC software packages that I examined are all capable tools for solving engineering math problems. There are substantial differences among the tools, however, so your own needs will determine which one is best for you.

The Casio fx-8000G is a compact and fairly conventional programmable scientific calculator that is augmented by function-definition and graphing features. Access to its scientific functions is via function keys (as opposed to a menu), so access is fast, but the keyboard is crowded and hard to read. The Casio's text editing and storage features are handy for phone lists.

The TI-81, like the Casio, is compact, fairly conventional, and has function-definition and graphing features. Its graphical analysis capabilities are somewhat more powerful than the Casio's. Because you access some of its scientific functions via a menu, the TI has a less cluttered keyboard, but requires more keystrokes. It has no text editing and storage capabilities. I found the TI the easiest of the calculators to learn and use.

The Sharp PC-E500 is a little less compact than the Casio and TI calculators, but substantially more powerful. It is really a combination of a scientific calculator and a Basic-language computer. As a calculator, it was almost as easy to use as the TI. With its QWERTY keyboard and built-in Basic, it was far and away the easiest for me to learn to program. Its special function-definition mode was easy to learn and use. Unfortunately, its graphics-analysis mode was the least powerful of the calculators.

The HP 48SX is the most powerful of the four calculators. It has an amazing number of features. However, the limited space for control keys means that each key must serve three or four functions, and the command structure was not very "intuitive." I found it very difficult to learn and use.

The four computer programs all have better equation-solving capabilities than any of the calculators. Eureka is the least expensive and least powerful, but I found it easiest to use. If you don't need this kind of tool very often, the ease-of-use factor becomes very important. I plan to keep Eureka around as the first tool to try for solving equations.

Because of the flexibility of its command structure (or programming language), TK Solver Plus is in some sense the most powerful of the programs. I found it the most difficult to use, however. It would probably be most useful with an applications library.

Although MathCad has equation-solving capabilities, its strong point is its enhanced function-definition, analysis, and graphing capabilities. Once you get used to the mathematical editor (which took me some time), you can define, evaluate, and plot complicated functions (including complex variables, vectors, derivatives, and integrals) very quickly. The program's supplier advertises it as a mathematical scratchpad; I found it serves very well in that capacity.

Derive is a strange beast, but it can be very useful. Even though I've used the program a number of times over the last year or so, I still find it hard to use. Nevertheless, if I have a substantial amount of algebra (or an algebraically complex series expansion or derivative) to do, the first thing I do is unlimber Derive. If I can get Derive to solve the problem (or pieces of the problem), I usually feel the time spent struggling with the program has been worthwhile. If Derive can solve the problem at all, it gives a correct answer; if I solve the problem by hand, I usually have to do it several times to ensure I haven't made a careless mistake. Also, Derive will save its answers in a text file that I can import directly into my Fortran programs. I also use Derive's extended numerical accuracy to obtain results that I can compare with those from my programs.

cal operations you can include in a function and the types of analyses you can perform. **Table 5** indicates features available for user-defined functions containing only simple variables; **Tables 7**, **8**, **9**, and **17** cover complex variables, vectors, matrices, and graphical analysis features.

All of the programs and calculators provide some capability for solving user-defined equations, but the capabilities vary widely. At a minimum, you can determine the roots of a user-defined function by graphical means. The more capable tools will solve a set of nonlinear equations, subject to constraints (including inequalities), by sophisticated numerical-analysis techniques. **Table 6** lists the capabilities. I didn't have time to experiment with equation solving as much as I would have liked, so the entries in the table are based largely on documentation.

The capabilities for performing complex-number, vector, and matrix operations also vary widely among the tools. Some of the tools offer no such capabilities; others treat complex values, vectors, and matrices in virtually the same way as real numbers and functions. The best complex-math features (**Table 7**) come with the HP calculator and with the Eureka, MathCad, and Derive programs.

As indicated in **Table 8**, the HP calculator, MathCad, *Two of the tools—the Derive software package and the HP 48SX calculator, perform symbolic mathematical operations.*

and Derive have the best vector-math features. I found using the vector-analysis features of the HP a little tedious, primarily because of the small, cluttered keyboard. I've owned versions of MathCad and Derive for some time and have found them both useful and easy to use in solving vector math problems.

None of the tools I reviewed provide the complete set of matrix-analysis features that you find in special-purpose matrix-analysis software for IBM-compatible (and other) computers. Nevertheless, some of them offer capabilities that are sufficient for most needs (**Table 9**). The Sharp and HP calculators and the MathCad and Derive programs are the strongest in this area. TK Solver has good capabilities, but in my opinion is less convenient to use.

My observation about statistical-analysis features is the same as for matrix-analysis features: None of the tools provide the complete set of statistical-analysis features offered by special-purpose statistical-analysis software. All the tools except Eureka provide some capability for statistical operations on tabulated data; some offer capabilities that are sufficient for most needs (**Table 10**). Once again, the Sharp and HP calculators and the MathCad and Derive software packages are the strongest in this area; TK Solver has good capabilities, but is less convenient to use. The Sharp and HP calculators and the TK Solver library provide programs for computing the most common probability functions (**Table 11**).

Symbolic algebra and calculus

Derive and the HP 48SX perform symbolic mathematical operations. (See **Table 12** for symbolic algebra features and **Table 13** for symbolic calculus.) For example, given the equation

$$a*x\hat{}2+b*x+c=0,$$

the tools will provide the solution

$$x=[-b\pm\sqrt{(b\hat{}2-4*a*c)}\,/\,(2*a).$$

Derive is somewhat more powerful than the HP calculator. I found the HP's symbolic capabilities more useful for reference to math formulas (common integrals, series expansions, and so forth) than for solving symbolic equations.

I have owned Derive (and its predecessor, MuMath) for several years, and I have found it helpful in several applications. Generally, I've used it for such tasks as simplifying algebraic expressions and expanding expressions in Taylor's series. There are more powerful symbolic-math programs than Derive, but not in the same price range.

Several of the tools provide reference formulas, tables of mathematical constants, and tables of physical constants. (See **Table 14** for details.) The volume of reference data in the Sharp calculator particularly impressed me; for the HP calculator, an optional HP Solve Equation card—which was included in the unit I reviewed—offers capabilities similar to the Sharp's.

As shown in **Table 15**, some of the tools can convert among different sets of units (for example, inches and centimeters) and will test dimensional consistency of variables used in arithmetic calculations. (In other words, they won't let you add apples to oranges.) The units-checking feature is handy, but I find it a little tedious to enter units with variables in equations, so I probably would make little use of it.

Graphics and graphical analysis

Graphing user-defined functions is possible with all the programs and calculators. I found this capability one of the tools' most useful features (**Table 16**). With a suitable output device, some of the tools can produce report-quality graphs.

Some of the tools can also be used to analyze graphical displays of user-defined functions (**Table 17**). At a minimum, you can use a cursor to move cross-hairs on a display and get a read-out of cursor position. Some of the tools offer greater analysis capabilities, such as numerical integration of the area between two plotted curves.

One of the main purposes of these computational tools is to eliminate the need for programming. Nevertheless, there are at least two reasons for including some programming features: batch processing of operations (putting the operations in a queue for later execution) and the need to perform computations that the tools don't provide directly. Programming capabilities of the tools vary widely (**Table 18**).

The Casio and TI calculators use a keystroke-entry type of programming language similar to that found in most earlier generations of scientific calculators. The Sharp has a modified version of the interpreter Basic used in most personal computers. The HP language is different from anything I have ever seen; it is a mix of keystroke-entry commands, high-level-language constructs (for example, *if-then-else-end*), and stack-object manipulation commands. I found the HP difficult to

For more information . . .

For more information about the calculators and software packages reviewed in this article, circle the appropriate numbers on the Information Retrieval Service Card or use EDN's Express Request Service. When you contact any of the following companies directly, please let them know you saw their products in EDN.

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program, the Sharp quick and easy (since I already knew Basic), and the Casio and TI fairly easy, but tedious.

With the software packages, you enter equations much as you would write them on a sheet of paper. Eureka, TK Solver, and MathCad allow sort of a free-form entry—you use the program's built-in editor to steer a cursor around the screen and make changes to equations much as you would with your favorite text editor. Derive's entry and editing capabilities are much more limited and difficult to use. You enter each equation or expression on a numbered line; once entered, the line is not easy to edit.

Eureka, TK Solver, and Derive can import text and equations from ASCII disk files. The equations are of a form typically used by high-level languages—for example, f(x)=x 2+sin(x). With MathCad, you have to use the program's editor to create program statements and equations appear in a true math format. You can save the statements in disk files for later recall and editing, but you can't use an ASCII editor on them.

TK Solver is the only one of the computer programs with a programming language that has full provisions for subroutines with local variables, IF-THEN-ELSE constructs, DO loops, and so forth. Although this language gives TK Solver a great deal of power, I found it hard to harness that power because of the way the software partitions various kinds of program specifications into sheets and sub sheets. These include

- a rules sheet for specifying the main equations defining your problem,
- a variables sheet for specifying such things as the type and status (input, output, guess, list variable) of variables in the equations,
- variables sub sheets (to specify units), and more.

Even though TK provides some help in negotiating the sheets, I found programming the sheets and maneuvering among them tedious. On the positive side, the sheet approach does force you to use a modular program structure, declare variables, and do other things that constitute good programming practice.

Hardware interfaces and options

Most of the calculators provide interfaces to personal computers, hard-copy devices, and mass storage (**Table 19**), although these interfaces are usually extra-cost options. The software packages, of course, use your computer's hardware facilities.

The HP and Sharp calculators have built-in serial ports, although the Sharp's connector is nonstandard. The Casio has an optional Centronics port. The HP, Sharp, and Casio calculators connect to optional printer/plotters. Add-in memory modules are available for the HP and the Sharp. Application software libraries come with the TK Solver, MathCad, and Derive software packages and optional libraries are also available. The HP calculator, as mentioned earlier, has optional application libraries on plug-in cards.

While computational speed is probably not the most important factor in determining the utility of these tools, it can nevertheless be important. To provide some information about relative speed, I devised a test computation that all the tools could handle. The computer I used for the tests is an Everex Step 25 with a 25-MHz 80386 CPU and an 80387 numeric coprocessor. For other computers with numeric coprocessors, speed results should scale roughly with clock speed.

The computation I used for the speed test is a summation of a geometric series for which there is also an analytical solution. The series is

$$S=\sum_{n=0}^{N} x^n,$$

None of the tools provide the complete set of matrix-analysis features that you find in special-purpose matrix-analysis software.

which can be summed analytically to give

$$\frac{1-x^{N+1}}{1-x}.$$

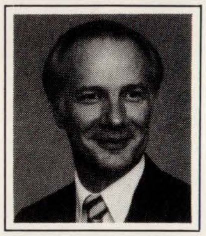
Timing the calculations with a stop watch, I used each tool to evaluate the sum for $x=0.99$ and $N=500$. All the tools gave the correct answer (99.34295221788) to the number of significant figures that they could display. The elapsed times were

Casio fx-8000G	13.1 sec
TI-81	13.0 sec
Sharp PC-E500 (single precision)	6.5 sec
Sharp PC-E500 (double precision)	9.0 sec
HP 48SX	41.6 sec
Eureka	0.4 sec
TK Solver Plus	0.2 sec
MathCad	0.5 sec
Derive	0.1 sec

I was surprised at how long the HP took to perform the calculation. It may well be that the code I wrote was not the most efficient method for this calculator.

Overall, I am impressed with all the tools; I believe they all provide a lot of power for not much money. There are substantial differences among them, however, and the information provided here should help you evaluate the tools for your own needs. EDN

Author's biography



Richard E Douglass is an independent consultant specializing in analytical tools for sonar systems design. He has a PhD in mechanical engineering from the University of Texas and is a member of the Acoustical Society of America.

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Table 1—"Report card"

	Casio fx-8000G	TI-81	Sharp PC-E500	HP 48 SX	Eureka	TK Solver Plus	MathCAD	Derive
List price	$120	$110	$229	$350	$167	$395	$349	$200
Ease-of-use grade (A–F)	C	A	A	D	B	C	B	D
Capability (A–F)	C	C	B	A	C	A	A	A

Table 2—Documentation

	Casio fx-8000G	TI-81	Sharp PC-E500	HP 48 SX	Eureka	TK Solver Plus	MathCAD	Derive
On-line help	No	No	No	No	Yes	Yes	Yes	Yes[1]
Table of contents	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Index (grade A–F)	No	C	C	B	C	C	B	D
Organization (grade A–F)	C	C	B	B	C	B	D	C
Tutorial section (commands grouped by function)	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Alphabetical command reference section	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
Examples (grade A–F)	C	B	B	C	D[2]	B[3]	B	D
Clarity of explanatory text (grade A–F)	C	B	B	C	C	B	B	D

Notes: 1. On-line help often refers only to a page in the user's manual.
2. Examples and command descriptions are in separate sections.
3. No examples for the library routines, which supply a large part of the software's power, are provided.

Table 3—Basic operations and data

	Casio fx-8000G	TI-81	Sharp PC-E500	HP 48 SX	Eureka	TK Solver Plus	MathCAD	Derive
Algebraic (A) or Reverse Polish (RP) data entry	A	A	A	RP[1]	A	A	A	A
Number of memory cells for basic storage	26[2]	27[3]	26[3]	NA	NA	NA	NA	NA
Number of screen text lines	8×16	8×16	4×40	4×20	25×80	25×80	25×80	25×80
Significant figures for calculations	13	13	10[4]	15[5]	13[5]	15[5]	15[5]	∞[6]
Fixed number of decimal places displayed	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Scientific notation	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Engineering notation	Yes	Yes	Yes	Yes	No	Yes	No	No

Notes: NA = Not applicable because partition of memory between data and program instructions is under system control.

1. Uses algebraic notation for symbolic equations.
2. Memory can be repartitioned for more data and less program storage.
3. Additional variable memory for Basic programs and special operations, such as matrix analysis, available.
4. 20 significant figures in double-precision mode are available for most operations. In both single and double precision, some internal calculations use greater significance (for example, 12 significant figures for single precision, 24 for double).
5. Number of significant figures is not clear from documentation.
6. The user specifies the significance of numeric data. Significance apparently is limited only by available memory.

Table 4—Intrinsic built-in functions

	Casio fx-8000G	TI-81	Sharp PC-E500	HP 48 SX	Eureka	TK Solver Plus	MathCAD	Derive
+, −, •, ÷	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
π, e^x, ln(x)	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
10^x, $\log_{10}$	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
y^x	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Sin, Cos, Tan	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Sin^{-1}, Cos^{-1}, Tan^{-1}	Yes	Yes	Yes	Yes	Tan^{-1} only	Yes	Yes	Yes
Deg (D), Rad (R), Grad (G) angle modes	D, R, G	D, R	D, R, G	D, R, G	R	D, R	R	R
Sinh, Cosh, Tanh	Yes	Yes[1]	Yes	Yes[1]	Yes	Yes	Yes	Yes
Sinh^{-1}, Cosh^{-1}, Tanh^{-1}	Yes	Yes[1]	Yes	Yes[1]	No	Yes	Yes	Yes
n!	Yes	Yes[1]	Yes	Yes[1]	Yes	Yes[2]	Yes	Yes
Γ(x)	No	No	Yes[1]	No	No	Yes[2]	Yes	Yes
Bessel functions	No	No	No	No	No	Yes[2]	Yes	Yes[2]
Financial functions (present value, etc.)	No	No	No	No	Yes	Yes[2]	No	Yes
Decimal < − > hours.minutes.seconds	Yes	No	Yes	Yes[1]	No	No	No	No
Absolute value of x	Yes	Yes	Yes[3]	Yes[1]	Yes	Yes	Yes	Yes
Integer part (next smaller, larger)	Yes	Yes[1]	Yes[3]	Yes[1]	Yes	Yes	Yes	No
Fractional part of x	Yes	Yes[1]	No	Yes[1]	Yes	No	No	No
Mantissa, exponent of x	No	No	No	Yes	No	No	No	No
Round x to n significant figures	No	Yes	No	Yes[1]	No	Yes	Yes	No
Truncate x to n significant figures	No	No	No	Yes	No	No	No	No
Sign of x	No	No	Yes[3]	Yes[1]	Yes	Yes	No	Yes
Remainder (Modulo x with respect to y)	No	No	No	Yes[1]	No	Yes	Yes	No
Minimum, maximum of {x, y, . . . }	No	No	No	Yes[1]	No	Yes	Yes	Yes
Set value according to test (eg, Value=x>y)	No	Yes[1]	Yes[3]	Yes[1]	No	Yes	Yes	No
Prime factors of number	No	No	Yes[4]	No	No	Yes[2]	No	Yes
Greatest and least common multiples of number	No	No	Yes[4]	No	No	Yes[2]	No	No
Logic operations (eg, AND, OR, XOR)	Yes	No	Yes[3]	Yes[1]	No	Yes[2]	No	No

Notes:
1. Function available via math menu, not function key.
2. Function is in library that comes with the software.
3. Available in Basic's immediate mode. Not available on function keys.
4. Function is in built-in program library.

Table 5—Evaluation and analysis of user-defined functions

	Casio fx-8000G	TI-81	Sharp PC-E500	HP 48 SX	Eureka	TK Solver Plus	MathCAD	Derive
Simple define/edit mode	Yes[1]	Yes[2]	Yes	Yes[3]	Yes	Yes	Yes[3]	Yes
Nesting of user functions	No	No	Yes	Yes	Yes	Yes	Yes	Yes
Numerical evaluation of function	Yes[4]	Yes[4]	Yes	Yes	Yes	Yes	Yes	Yes
Roots of function by search methods	Yes[4]	Yes[4]	Yes[5]	Yes[5]	Yes	Yes	Yes	Yes
Roots of polynomials (all complex roots)	No	No	Yes[6]	Yes[7]	Yes	Yes[8]	No	Yes
Numerical differentiation of function	No	Yes	No	No	Yes	Yes[8]	Yes	Yes
Numerical integration of function	No	No	Yes[9]	Yes	Yes	Yes[8]	Yes	Yes
Numerical integration of differential equation	No	No	No	No	Yes	Yes[8]	No	No
Max/min of function	No	No	No	No	Yes	Yes[8]	No	No
Fourier transform of function	No	No	No	No	No	Yes[8]	No	Yes[10]
Sums, series definition of function	No	No	No	Yes	Yes	Yes	Yes	Yes
Product-form definition of function	No	No	No	No	No	No	Yes	Yes
Continued-fraction definition of function	No	No	No	No	No	No	No	No

Notes: 1. Function definition is by entry of an algebraic keystroke sequence, such as those used for calculator math operations. Subsequent functions can be superimposed on plot, but only last function remains in memory.
2. Function definition is by entry of an algebraic keystroke sequence, such as those used for calculator math operations. You can enter as many as four functions and superimpose their plots.
3. Equation editor displays equations in true mathematical format.
4. Evaluating functions and locating roots involves manually moving cursor and reading ordinate value.
5. Numerical root-search methods are in built-in program libraries.
6. Built-in cubic-polynomial solver.
7. Built-in quadratic-polynomial solver.
8. Function is in library that comes with the software.
9. Numerical-integration procedure is in a built-in program library.
10. Fourier-transform procedure is in a library that comes with the software.

Table 6—Numerical solution of simultaneous equations

	Casio fx-8000G	TI-81	Sharp PC-E500	HP 48 SX	Eureka	TK Solver Plus	MathCAD	Derive
Sets of linear equations	No	Yes[1]	Yes	Yes	Yes	Yes	Yes	Yes
Sets of nonlinear equations	No	No	No	No[2]	Yes	Yes	Yes	No
Optimization (maximize function with constraints)	No	No	No	No	Yes	Yes[3]	Yes[4]	No

Notes: 1. Linear-equation solver requires user interaction to apply matrix row operations.
2. Multiple-equation solutions available, but you must sequence the equations so that the first equation has only 1 unknown, the second has only 2 unknowns (including the unknown in the first equation), and so on.
3. Function is in library that comes with the software.
4. Built-in procedure for minimizing error subject to constraint equations.

Table 7—Complex mathematics

	Casio fx-8000G	TI-81	Sharp PC-E500	HP 48 SX	Eureka	TK Solver Plus	MathCAD	Derive
$+, -, \cdot, \div$	No	No	Yes[1]	Yes	Yes	Yes[2]	Yes	Yes
y^x	No	No	No	Yes	Yes	Yes[3]	Yes	Yes
Sin, Cos, Tan	No	No	No	Yes	Yes	Yes[4]	Yes	Yes
Sin^{-1}, Cos^{-1}, Tan^{-1}	No	No	No	Yes	Tan^{-1} only	Yes[4]	Yes	Yes
e^x, ln(x)	No	No	No	Yes	Yes	Yes[4]	Yes	Yes
Absolute value	No	No	Yes[1]	Yes	Yes	No	Yes	Yes
Argument (phase)	No	No	Yes[1]	Yes	Yes	No	Yes	Yes
Conjugate	No	No	No	Yes	No	Yes[2]	Yes	Yes
Real part, imaginary part extraction	No	No	No	Yes	Yes	Yes[2]	Yes	Yes
Combine real x, y into x + i*y	No	No	No	Yes	Yes	Yes[2]	Yes	Yes

Notes: 1. Built-in program for elementary complex operations.
2. Requires complex values to be in the form (a, b). Mixing real and complex numbers in arithmetic operations not allowed.
3. Built-in function for raising a complex value to a real power.
4. Function is in library that comes with the software.

Table 8—Vector mathematics

	Casio fx-8000G	TI-81	Sharp PC-E500	HP 48 SX	Eureka	TK Solver Plus	MathCAD	Derive
Cylindrical coordinate mode (2D, 3D)	No	No	No	Yes	No	No	No	No
Spherical coordinate mode (for 3D)	No	No	No	Yes	No	No	No	No
Conversion between modes	No	No	No	Yes	No	No	No	No
Assemble, extract components	No	No	No	Yes	No	Yes[1]	Yes	Yes
Complex elements	No	No	No	Yes	No	No	Yes	Yes
Add, subtract	No	No	No	Yes	No	Yes[1]	Yes	Yes
Multiply by constant	No	No	No	Yes	No	Yes[1]	Yes	Yes
Dot product	No	No	No	Yes	No	Yes[1]	Yes	Yes
Cross product	No	No	No	Yes	No	No	Yes	Yes
Magnitude	No	No	No	Yes	No	No	Yes	No

Note: 1. Treats vectors as special "lists" and provides list operations equivalent to these vector operations.

Table 9—Matrix mathematics

	Casio fx-8000G	TI-81	Sharp PC-E500	HP 48 SX	Eureka	TK Solver Plus	MathCAD	Derive
Convenient data entry/edit	No	Yes[1]	Yes[2]	Yes[3]	No	Yes[4]	Yes	Yes
Identity matrix generation	No	No	No	Yes	No	No	Yes	Yes
Other special form matrix generation	No	No	No	Yes[5]	No	Yes[4]	Yes[6]	Yes[7]
Complex elements	No	No	No	Yes	No	No	Yes	Yes
Add, subtract	No	Yes	Yes	Yes	No	Yes	Yes	Yes
Transpose	No	Yes	Yes	Yes	No	Yes[8]	Yes	Yes
Multiply	No	Yes	Yes	Yes	No	Yes[8]	Yes	Yes
Determinant	No	Yes	Yes	Yes	No	Yes[8]	Yes	Yes
Trace	No	No	No	No	No	No	Yes	Yes
Maximum, minimum element	No	No	No	Yes[9]	No	No	Yes	No
Sort elements	No	No	No	No	No	No	Yes	No
Absolute value (Euclidean norm)	No	No	No	No	No	No	Yes	No
Row, column norms	No	No	No	Yes	No	No	No	No
Inverse	No	Yes	Yes	Yes	No	Yes	Yes	Yes
Eigenvalues	No	No	No	No	No	Yes[8]	No	Yes
Eigenvectors	No	No	No	No	No	Yes[8]	No	No

Notes: 1. Handles as many as three 6×6 matrices.
2. Handles as many as 29 matrices. Maximum size, with sufficient memory installed, is 256×256.
3. Special editor for matrix data entry provided.
4. Treats matrices as special "lists" and provides list operations equivalent to these matrix operations.
5. Can generate a matrix with elements all the same value.
6. Can define elements using its list-creation ("range variable").
7. Can define elements as functions of indices.
8. Function is in library that comes with the software.
9. Provided as statistical function.

Table 10—Statistical calculations and data analysis

	Casio fx-8000G	TI-81	Sharp PC-E500	HP 48 SX	Eureka	TK Solver Plus	MathCAD	Derive
Convenient data entry/edit	No[1]	Yes[2]	Yes[3]	Yes[4]	No	Yes[5]	Yes[6]	Yes[7]
Total of values	Yes	Yes	Yes	Yes	No	Yes[8]	No	No
Maximum, minimum	No	No	No	Yes	No	Yes[8]	Yes	No
Mean, variance, standard deviation	Yes	Yes	Yes	Yes	No	Yes[8]	Yes	Yes
Covariance and/or correlation (paired tables)	Yes	Yes	Yes	Yes	No	Yes[8]	Yes	No
Linear regression	Yes	Yes	Yes	Yes	No	Yes[8]	Yes	Yes[9]

Notes: 1. Statistical analysis uses special data-entry mode with limited editing. After running an analysis, you cannot edit data and repeat analysis.
2. Has data-table editor that allows editing data between analyses.
3. You can use Basic to create statistical data. Basic data and statistical-analysis data reside in same area.
4. Enter and edit data in a special statistics mode or in the matrix editor mode.
5. You use a list sheet to enter statistical data.
6. Treats statistical data as vector elements.
7. Statistical functions operate only on vector and matrix elements.
8. Function is in library that comes with the software.
9. Generalized function-fit capability for regression provided.
10. Other types of regression are only possible indirectly (for example, by taking log of independent variable).
11. Plots histogram data but does not provide tabular output.

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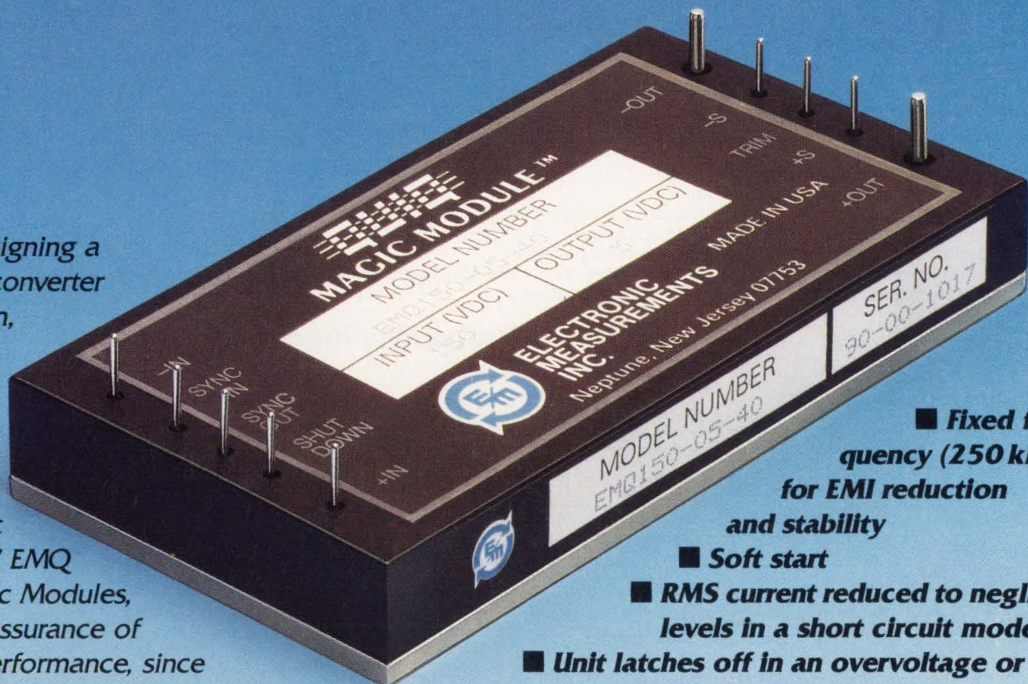

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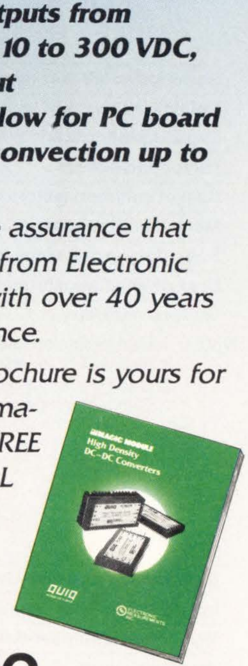

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Table 10—Statistical calculations and data analysis *(continued)*

	Casio fx-8000G	TI-81	Sharp PC-E500	HP 48 SX	Eureka	TK Solver Plus	MathCAD	Derive
Other types of regression (eg, Log fit)	No	Yes	No[10]	Yes	No	Yes[8]	No	Yes[9]
Linear interpolation on data table	No	No	No	No	No	Yes	Yes	No
Higher-order interpolation on data table	No	Yes	No	No	No	Yes	Yes	No
Sort data	No	Yes	Yes[10]	No	No	Yes[8]	Yes	No
Histogram (density function)	Yes[11]	Yes[11]	No	Yes	No	Yes[8]	Yes	Yes
Generate uniform distribution random numbers	Yes	Yes	Yes	Yes	No	Yes[8]	Yes	No
Generate normal distribution random numbers	No	No	No	No	No	Yes[8]	No	No

Notes: 1. Statistical analysis uses special data-entry mode with limited editing. After running an analysis, you cannot edit data and repeat analysis.
2. Has data-table editor that allows editing data between analyses.
3. You can use Basic to create statistical data. Basic data and statistical-analysis data reside in same area.
4. Enter and edit data in a special statistics mode or in the matrix editor mode.
5. You use a list sheet to enter statistical data.
6. Treats statistical data as vector elements.
7. Statistical functions operate only on vector and matrix elements.
8. Function is in library that comes with the software.
9. Generalized function-fit capability for regression provided.
10. Other types of regression are only possible indirectly (for example, by taking log of independent variable).
11. Plots histogram data but does not provide tabular output.

Table 11—Probability functions

	Casio fx-8000G	TI-81	Sharp PC-E500	HP 48 SX	Eureka	TK Solver Plus	MathCAD	Derive
Binomial coefficient	No	No	No	No	No	Yes[1]	No	No
Number of permutations, combinations	No	Yes[2]	Yes[3]	Yes[2]	No	Yes[1]	No	No
Calculate normal (Gauss) probability	No	No	Yes[4]	Yes	Yes	Yes[1]	Yes	Yes
Calculate Chi-square probability	No	No	Yes[4]	Yes	No	Yes[1]	No	No
Calculate T probability	No	No	Yes[4]	Yes	No	Yes[1]	No	No
Calculate F probability	No	No	Yes[4]	Yes	No	Yes[1]	No	No

Notes: 1. Function is in library that comes with the software.
2. Function available via math menu, not function key.
3. Available as intrinsic function in calculator Basic mode.
4. Built-in programs for these functions provided.

Table 12—Symbolic algebra

	Casio fx-8000G	TI-81	Sharp PC-E500	HP 48 SX	Eureka	TK Solver Plus	MathCAD	Derive
Solve for variable in equation	No	No	No	Yes[1]	No	No	No	Yes[2]
Collect like terms in expression	No	No	No	Yes	No	No	No	Yes
Expand products and powers in expression	No	No	No	Yes	No	No	No	Yes
Factor polynomial	No	No	No	Yes[3]	No	No	No	Yes[4]
Cancel common factors in ratio of polynomials	No	No	No	No	No	No	No	Yes
Manual rearrangement of elements of expression	No	No	No	Yes	No	No	No	Yes
Substitute expressions for variables	No	No	No	No	No	No	No	Yes
User-defined transformations	No	No	No	No	No	No	No	Yes
Vectors, matrices	No	No	No	No	No	No	No	Yes

Notes: 1. Can isolate or solve for a variable in an equation if the variable appears only once and if the equation is sufficiently simple.
2. Can isolate, or solve for, a variable in an equation if the equation is sufficiently simple.
3. Can only factor quadratics.
4. Can factor a polynomial of arbitrary degree if the equation is sufficiently simple.

Table 13—Symbolic calculus

	Casio fx-8000G	TI-81	Sharp PC-E500	HP 48 SX	Eureka	TK Solver Plus	MathCAD	Derive
Differentiation of user-defined function	No	No	No	Yes[1]	No	No	No	Yes[1]
Integration of user-defined function	No	No	No	Yes[1]	No	No	No	Yes[1]
Taylor series for user-defined function	No	No	No	Yes[1,2]	No	No	No	Yes[1]
Vector calculus	No	No	No	No	No	No	No	Yes[3]

Notes: 1. Operation possible if the function is sufficiently simple.
2. Maclaurin series expansion (about the origin) in the expansion variable provided.
3. Can form gradient, divergence, and Laplacian vector operators.

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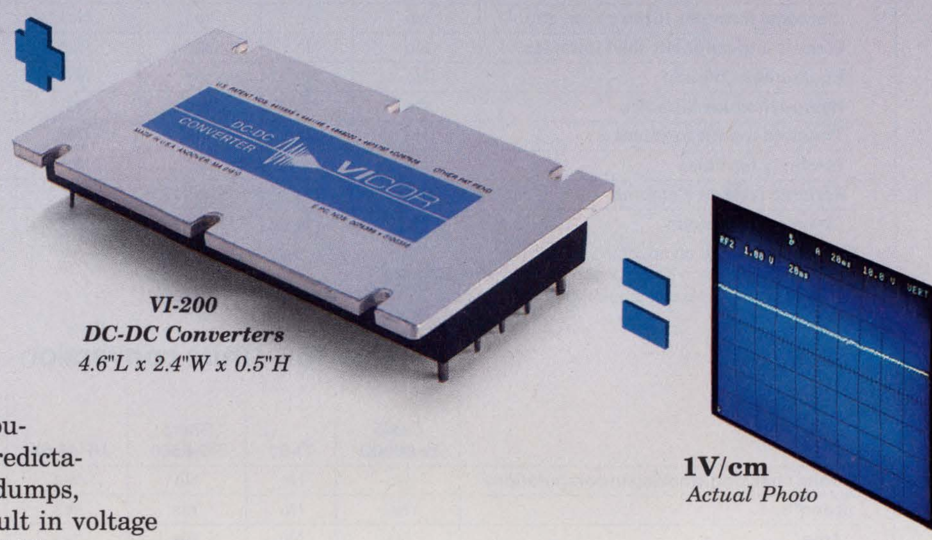

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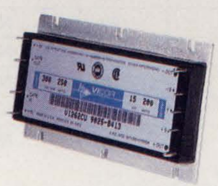

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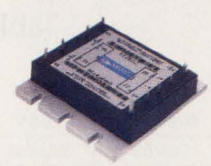

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Table 14—Reference formulas and constants

	Casio fx-8000G	TI-81	Sharp PC-E500	HP 48 SX	Eureka	TK Solver Plus	MathCAD	Derive
Physical constants	No	No	Yes	No[1]	No	No	No	Yes[2]
Algebraic identities (factorization, etc)	No	No	Yes	No[3]	No	No	No	No[3]
Trigonometric identities	No	No	Yes	No[3]	No	No	No	No[3]
Table of integrals	No	No	Yes	No[3]	No	No	No	No[3]
Table of Laplace transforms	No	No	Yes	No	No	No	No	No
Electrical formulas (Ohm's Law, etc)	No	No	Yes	No[1]	No	No	No	No
Electric and magnetic field formulas	No	No	Yes	No[1]	No	No	No	No
Equations of motion	No	No	Yes	No[1]	No	No	No	No
Hydrodynamics formulas	No	No	Yes	No[1]	No	No	No	No
Thermodynamic formulas	No	No	Yes	No[1]	No	No	No	No
Elasticity formulas	No	No	Yes	No[1]	No	No	No	No
Periodic table of elements	No	No	Yes	No[1]	No	No	No	No
Chemistry formulas	No	No	Yes	No[1]	No	No	No	No

Notes: 1. Available on optional library card.
2. Available in library that comes with the software.
3. Not provided in tabular form, but resident in symbolic-manipulation rules.

Table 15—Units conversion

	Casio fx-8000G	TI-81	Sharp PC-E500	HP 48 SX	Eureka	TK Solver Plus	MathCAD	Derive
Units checking/tracking in computations	No	No	No	Yes	No	Yes[1]	Yes[1]	No
Length	No	No	Yes	Yes	No	No	No	Yes[2]
Area	No	No	Yes	Yes	No	No	No	Yes[2]
Volume	No	No	Yes	Yes	No	No	No	Yes[2]
Angle	No	No	No	Yes	No	No	No	Yes[2]
Time	No	No	No	Yes	No	No	No	Yes[2]
Speed	No	No	Yes[3]	Yes	No	No	No	No
Acceleration	No	No	No	No	No	No	No	No
Mass	No	No	Yes	Yes	No	No	No	No
Force	No	No	Yes[3]	Yes	No	No	No	Yes[2]
Energy	No	No	Yes	Yes	No	No	No	Yes[2]
Power	No	No	No	Yes	No	No	No	Yes[2]
Pressure	No	No	No	Yes	No	No	No	No
Electric charge	No	No	No	Yes	No	No	No	Yes[2]
Temperature	No	No	No	Yes	No	No	No	No
Light	No	No	No	Yes	No	No	No	No
Prefixes (micro, etc)	No	No	No	Yes	No	No	No	Yes[2]

Notes: 1. Allows user-defined conversions.
2. Available in library that comes with the software.
3. Provides some of these conversions.

Table 16—Graphics

	Casio fx-8000G	TI-81	Sharp PC-E500	HP 48 SX	Eureka	TK Solver Plus	MathCAD	Derive
Display resolution (pixels)	95×63	96×64	240×32[1]	130×55	EGA[2]	VGA	VGA	VGA
Plot tabulated data	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Auto plotting (scaling, sampling)	Yes	Yes	Yes	Yes	Yes	No[3]	Yes	Yes
X, Y plots	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Log, log-log	No	No	No	No	No	Yes	Yes	No
Parametric X, Y	No	Yes	No	Yes	No	Yes	Yes	Yes
Conic (two branches)	No	No	No	Yes	No	No	No	No

Notes: 1. Uses only 140 of the 240 pixels across in its built-in graphics program.
2. Default display is text mode. Selecting the zoom feature switches to one of your computer's graphics modes, presumably the highest resolution available. On the author's computer, however, Eureka selected the EGA mode, even though VGA was available.
3. Makes you set up a data table to plot a function.
4. Available in library that comes with the software.
5. Plots surfaces, but without hidden lines.
6. Lets you annotate plots by placing text in regions near graphics.

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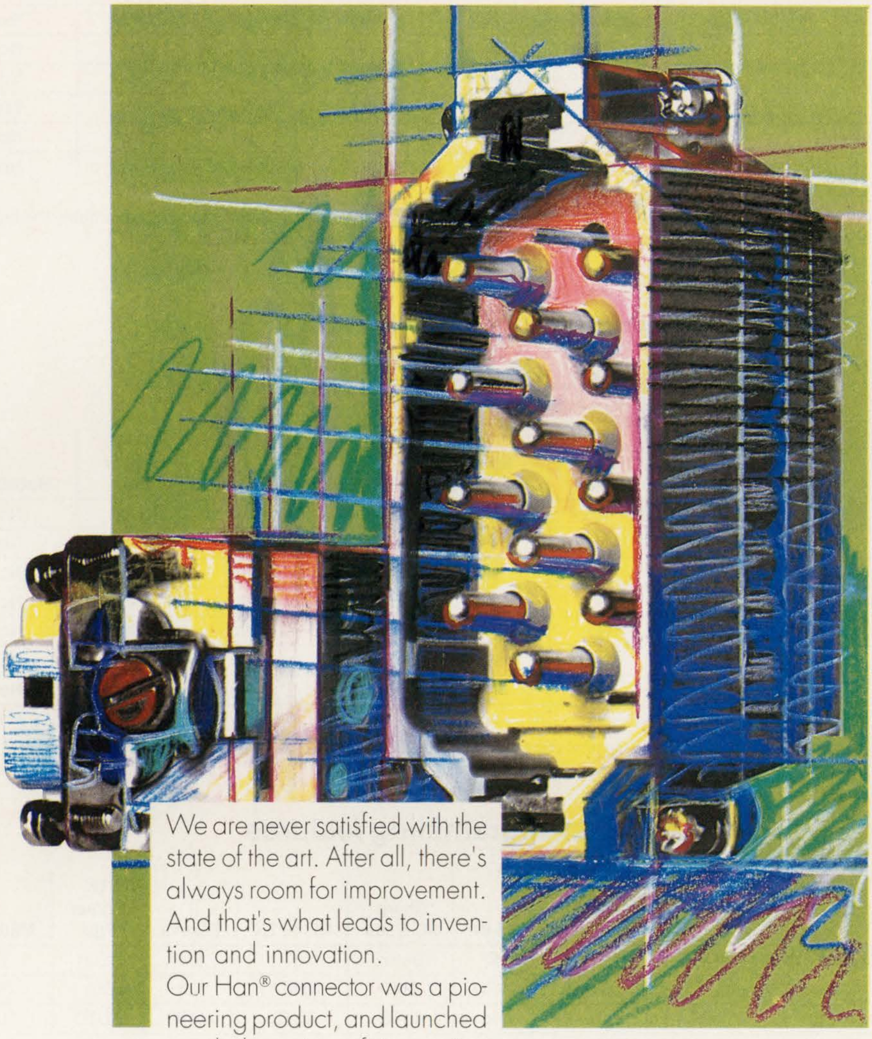

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CIRCLE NO. 54

Table 16—Graphics *(continued)*

	Casio fx-8000G	TI-81	Sharp PC-E500	HP 48 SX	Eureka	TK Solver Plus	MathCAD	Derive
Polar plots	No	Yes	No	Yes	No	No	No	Yes
Contour plots	No	No	No	No	No	Yes[4]	No	No
3-D (surface) plots	No	No	No	No	No	Yes[4,5]	Yes	Yes
Bar charts	Yes	Yes	No	Yes	No	Yes	No	Yes
Pie charts	No	No	No	No	No	Yes	No	No
Error bars	No	No	No	No	No	No	Yes	No
Multiple curves/plot	Yes	Yes	No	Yes	No	Yes	Yes	Yes
Multiple line types	No	No	No	No	No	No	No	No
Axis labels	No	No	No	Yes	No	Yes	No	No
Text/titles	No	No	No	No	No	Yes	Yes[6]	No
Drawing capability (lines, curves)	Yes	Yes	No	Yes	No	No	No	No
Zoom capability	Yes	Yes	No	Yes	No	No	No	Yes

Notes: 1. Uses only 140 of the 240 pixels across in its built-in graphics program.
2. Default display is text mode. Selecting the zoom feature switches to one of your computer's graphics modes, presumably the highest resolution available. On the author's computer, however, Eureka selected the EGA mode, even though VGA was available.
3. Makes you set up a data table to plot a function.
4. Available in library that comes with the software.
5. Plots surfaces, but without hidden lines.
6. Lets you annotate plots by placing text in regions near graphics.

Table 17—Graphical analysis

	Casio fx-8000G	TI-81	Sharp PC-E500	HP 48 SX	Eureka	TK Solver Plus	MathCAD	Derive
Cursor readout	Yes[1]	Yes	No	Yes	No	No	No	Yes
Trace function	Yes	Yes	No	No	No	No	No	No
Evaluate plotted function at cursor	Yes	Yes	No	Yes	No	No	No	No
Root location (automated search)	No	No	No	Yes	No	No	No	No
Slope calculation	No	No	No	Yes	No	No	No	No
Area calculation	No	No	No	Yes	No	No	No	No
Extremum calculation	No	No	No	Yes	No	No	No	No
Plot derivative	No	No	No	Yes	No	No	No	No

Note: 1. Does not allow concurrent control of horizontal and vertical cursor position. You use arrow keys for horizontal and vertical control, but you must hit a key to toggle between the two.

Table 18—Programming features

	Casio fx-8000G	TI-81	Sharp PC-E500	HP 48 SX	Eureka	TK Solver Plus	MathCAD	Derive
Type of programming (keystroke (K) equation (EQ))	K[1]	K[1]	Basic	K[2]	EQ[3]	EQ[3]	EQ[3]	EQ[3]
Memory available	1446[4]	2400	28K[5]	28K[5]	NA	NA	NA	NA
Data, program instruction partition	Yes[6]	No	AUTO	AUTO	AUTO	AUTO	AUTO	AUTO
Directories	No	No	No	Yes	Yes	Yes	Yes	Yes
Editor for command entry	Yes	Yes	Yes	Yes	Yes[7]	Yes[7]	Yes[8]	Yes[7]
Subroutines	Yes	Yes	Yes	Yes	Yes	Yes	No	No
Functions	No	No	Yes	Yes	No	Yes	Yes	Yes

Notes: NA = Not applicable.
1. Programming language is calculator-keystroke queue type.
2. Language is a combination of calculator-keystroke commands and high-level-language commands.
3. Equation-statement types of commands.
4. 1446 "steps" provided. A keystroke command uses either one or two steps.
5. Additional memory is available at extra cost.
6. Lets you partition 206 "steps" of memory between program and data. One data cell is equivalent to 8 program steps.
7. You can create command sequences with built-in editor, or import sequences created with another editor. Expression of equations is in a high-level-language notation similar to Basic.
8. You can only create and edit command sequences using the built-in editor, which displays equations in mathematical notation rather than a high-level-language notation.
9. Provides only a conditional jump past the next statement line.
10. Has a primitive 1-line IF test for function definition. For example, f(x)=IF(x>0, 1, −1) indicates that f(x) is 1 for x greater than 0 and −1 for x less than or equal to 0.
11. "Range variables" provide most of the computational power of Do loops.
12. Data files are treated as "objects."
13. Accesses data tables using its peculiar list-function save and load.

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Table 18—Programming features *(continued)*

	Casio fx-8000G	TI-81	Sharp PC-E500	HP 48 SX	Eureka	TK Solver Plus	MathCAD	Derive
Local variables in subroutines/functions	No	No	No	Yes	No	Yes	No	No
String variables	No	No	Yes	Yes	No	No	No	No
Logical variables	No	No	No	Yes	No	Yes	No	No
***If-then-else* branching**	No[9]	No[9]	Yes	Yes	No	Yes	Yes[10]	No
Do loops	No	No	Yes	Yes	No	Yes	Yes[11]	No
Formatted print of computed data	No	Yes	Yes	Yes	No	Yes	Yes	No
Prompt and wait for user input	Yes	Yes	Yes	Yes	No	No	No	No
Test keyboard and proceed if no entry	No	No	Yes	Yes	No	No	No	No
Graphics commands	Yes	Yes	Yes	Yes	No	No	Yes	No
Device control (eg, printer port)	No	No	Yes	No	No	No	No	No
Time/date functions	No	No	No	Yes	No	No	No	No
Error trapping	No	No	Yes	Yes	No	No	No	No
Single-step debugging capability	No	No	Yes	Yes	No	No	No	No
Set breakpoint debugging capability	No	Yes	Yes	Yes	No	Yes	No	No
Examine variables debugging capability	No	No	Yes	Yes	No	Yes	No	No
Data file access	No	No	Yes	Yes[12]	No	Yes[13]	Yes	No

Notes: NA = Not applicable.

1. Programming language is calculator-keystroke queue type.
2. Language is a combination of calculator-keystroke commands and high-level-language commands.
3. Equation-statement types of commands.
4. 1446 "steps" provided. A keystroke command uses either one or two steps.
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11. "Range variables" provide most of the computational power of Do loops.
12. Data files are treated as "objects."
13. Accesses data tables using its peculiar list-function save and load.

Table 19—Hardware interfaces and options

	Casio fx-8000G	TI-81	Sharp PC-E500	HP 48 SX	Eureka	TK Solver Plus	MathCAD	Derive
Computer interface	No	No	Yes	Yes	NA	NA	NA	NA
Printer/plotter interface	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes
Mass storage interface	Yes	No	Yes	Yes	NA	NA	NA	NA
Memory	No	No	Yes	Yes	NA	NA	NA	NA
Libraries	No	No	No	Yes	No	Yes	Yes	Yes

Note: NA = Not applicable.

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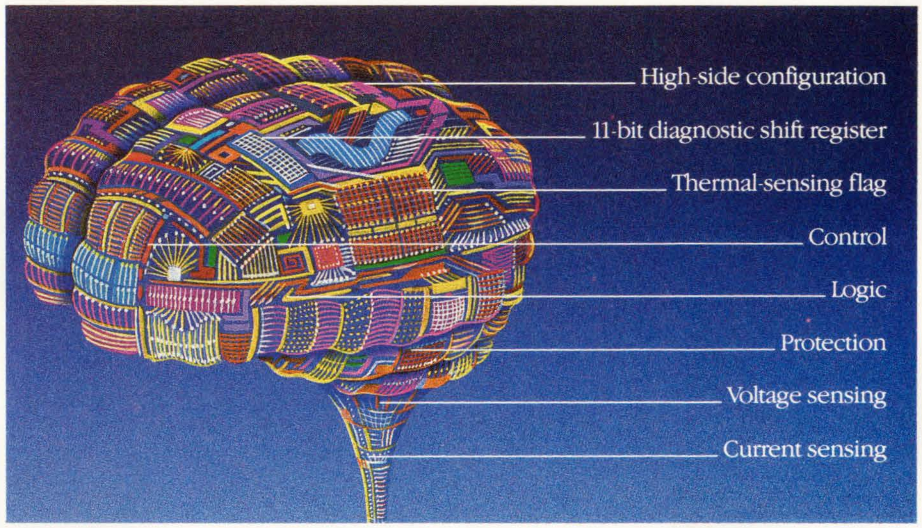

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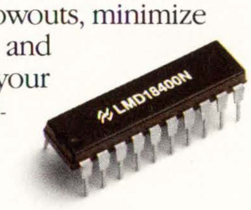

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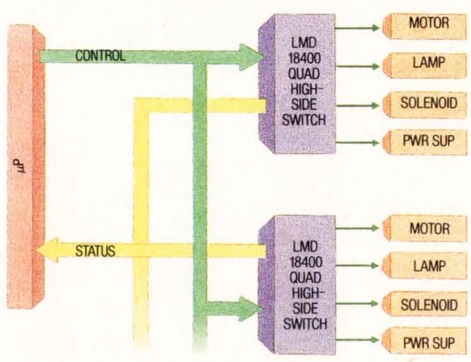

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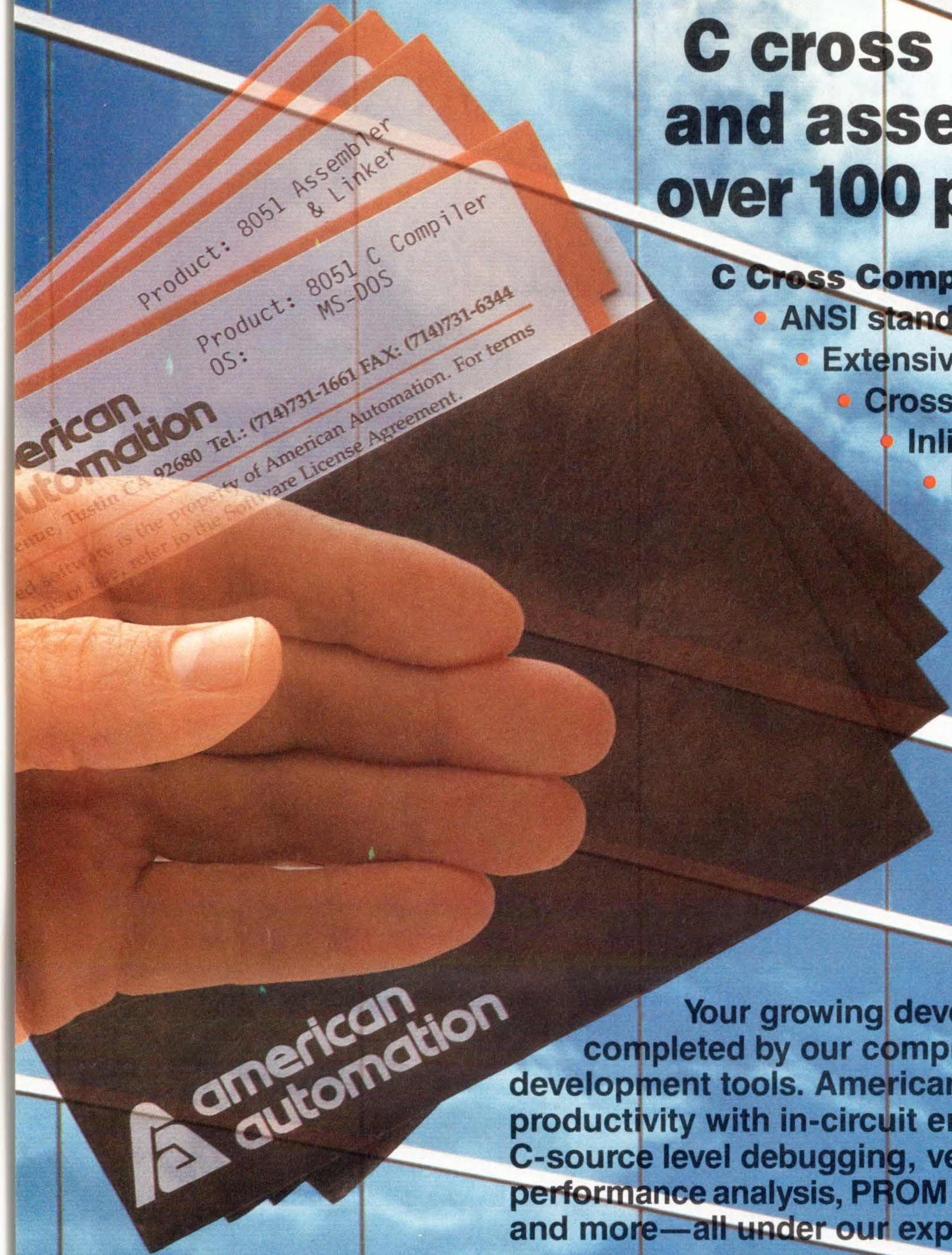

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CIRCLE NO. 56

DESIGN NOTES

Number 45 in a series from Linear Technology Corporation March, 1991

Signal Conditioning for Platinum Temperature Transducers

Jim Williams

High accuracy, stability, and wide operating range make platinum RTDs (resistance temperature detectors) popular temperature transducers. Signal conditioning these devices requires care to utilize their desirable characteristics. Figure 1's bridge based circuit is highly accurate and features a ground referred RTD. The ground connection is often desirable for noise rejection. The bridges RTD leg is driven by a current source while the opposing bridge branch is voltage biased. The current drive allows the voltage across the RTD to vary directly with its temperature induced resistance shift. The difference between this potential and that of the opposing bridge leg forms the bridges output.

A1A and instrumentation amplifier A2 form a voltage controlled current source. A1A, biased by the LT1009 reference, drives current through the 88.7Ω resistor and the RTD. A2, sensing differentially across the 88.7Ω resistor, closes a loop back to A1A. The 2k-0.1µF combination sets amplifier rolloff, and the configuration is stable. Because A1A's loop forces a fixed voltage across the 88.7Ω resistor, the current through Rp is constant. A1's operating point is primarily fixed by the 2.5V LT1009 voltage reference.

The RTD's constant current forces the voltage across it to vary with its resistance, which has a nearly linear positive temperature coefficient. The non-linearity could cause several degrees of error over the circuit's 0°C-400°C operating range. The bridges output is fed to instrumentation amplifier A3, which provides differential gain while simultaneously supplying non-linearity

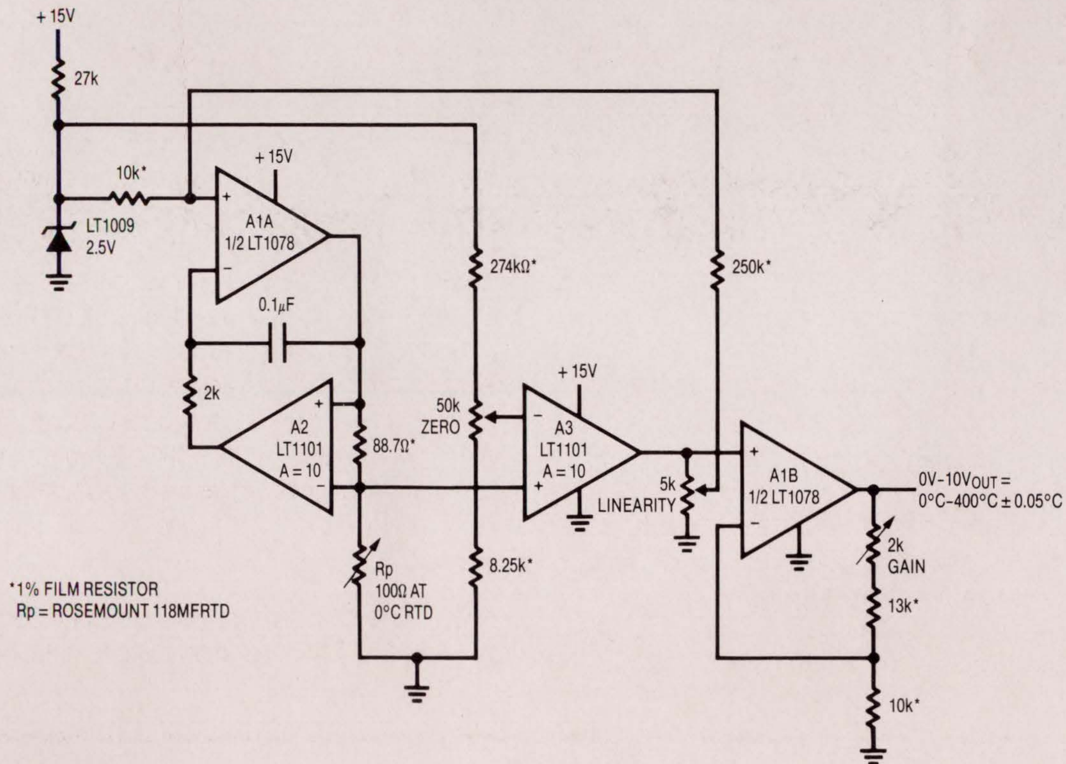

Figure 1. Linearized Platinum RTD Bridge. Feedback to Bridge from A3 Linearizes the Circuit.

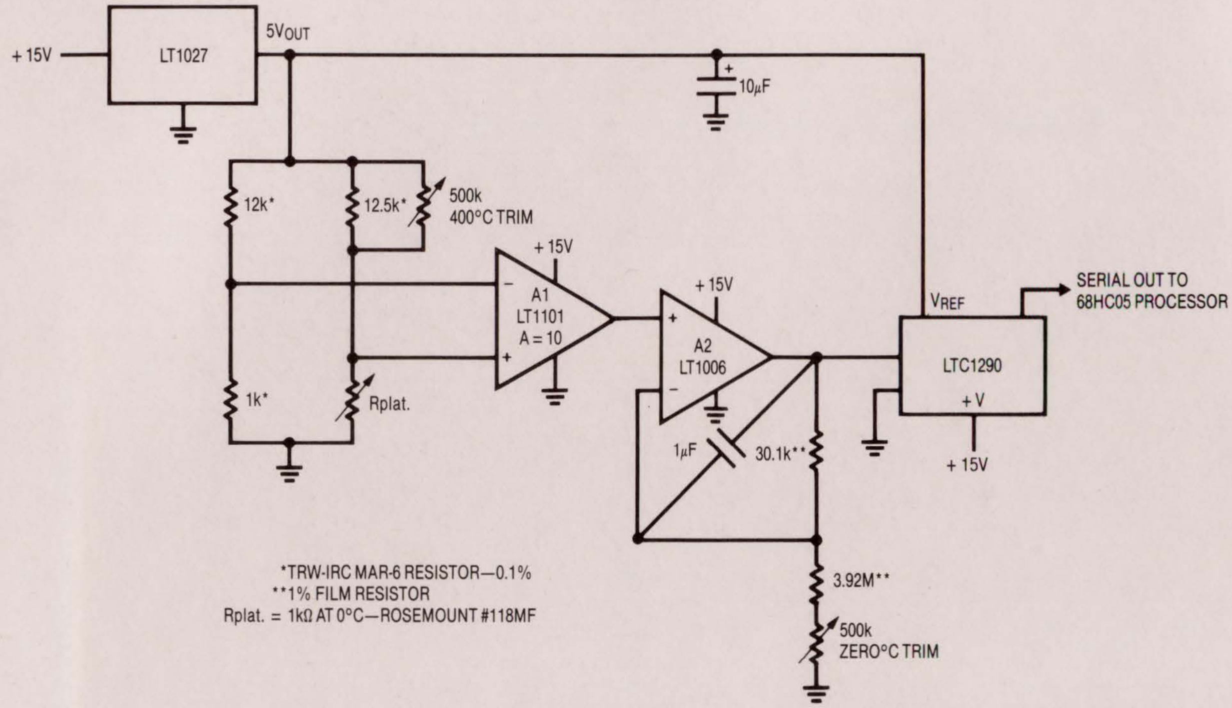

Figure 2. Digitally Linearized Platinum RTD Signal Conditioner

correction. The correction is implemented by feeding a portion of A3's output back to A1's input via the 10k-250k divider. This causes the current supplied to Rp to slightly shift with its operating point, compensating sensor non-linearity to within ±0.05°C. A1B, providing additional scaled gain, furnishes the circuit output.

To calibrate this circuit, substitute a precision decade box (e.g., General Radio 1432k) for Rp. Set the box to the 0°C value (100.00Ω) and adjust the zero trim for a 0.00V output. Next, set the decade box for a 140°C output (154.26Ω) and adjust the gain trim for a 3.500V output reading. Finally, set the box to 249.0Ω (400.00°C) and trim the linearity adjustment for a 10.000V output. Repeat this sequence until all three points are fixed. Total error over the entire range will be within ±0.05°C. The resistance values given are for a nominal 100.00Ω (0°C) sensor. Sensors deviating from this nominal value can be used by factoring in the deviation from 100.00Ω. This deviation, which is manufacturer specified for each individual sensor, is an offset term due to winding tolerances during fabrication of the RTD. The gain slope of the platinum is primarily fixed by the purity of the material and has a very small error term.

The previous example relies on analog techniques to achieve a precise, linear output from the platinum RTD bridge. Figure 2 uses digital corrections to obtain similar results. A processor is used to correct residual RTD non-linearities. The bridges inherent non-linear output is also accommodated by the processor.

The LT1027 drives the bridge with 5V. The bridge differential output is extracted by instrumentation amplifier A1. A1's output, via gain scaling stage A2, is fed to the LTC1290 12-bit A-D. The LTC1290's raw output codes reflect the bridges non-linear output versus temperature. The processor corrects the A-D output and presents linearized, calibrated data out. RTD and resistor tolerances mandate zero and full scale trims, but no linearity correction is necessary. A2's analog output is available for feedback control applications. The complete software code for the 68HC05 processor, developed by Guy M. Hoover, appears in Application Note 43.

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DESIGN IDEAS

EDITED BY ANNE WATSON SWAGER

One coax cable carries video and power

Jeff Kirsten and Charlie Allen
Maxim Integrated Products, Sunnyvale, CA

In **Fig 1**'s video system, a single coaxial cable carries power to a remote location, selects one of eight video channels, and returns the selected signal. The system can choose one of several remote surveillance-camera signals, for example, and can display the picture on a monitor near the interface box.

The interface box **(Fig 2)** encodes a desired channel with three bits via the switch settings of S_1 through S_3. You can modify the circuit to read an applied digital

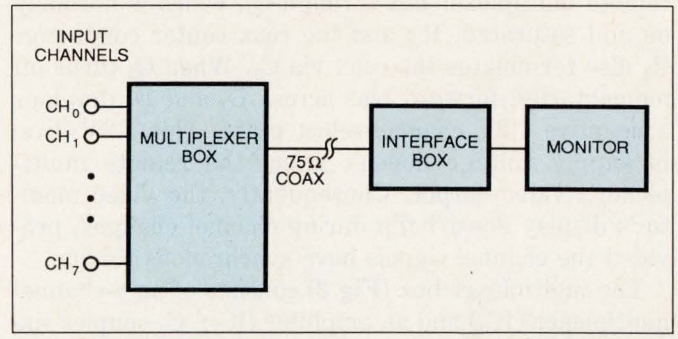


Fig 1—This 1-cable system carries *composite video (NTSC, PAL, or SECAM), power, and channel-select signals.*

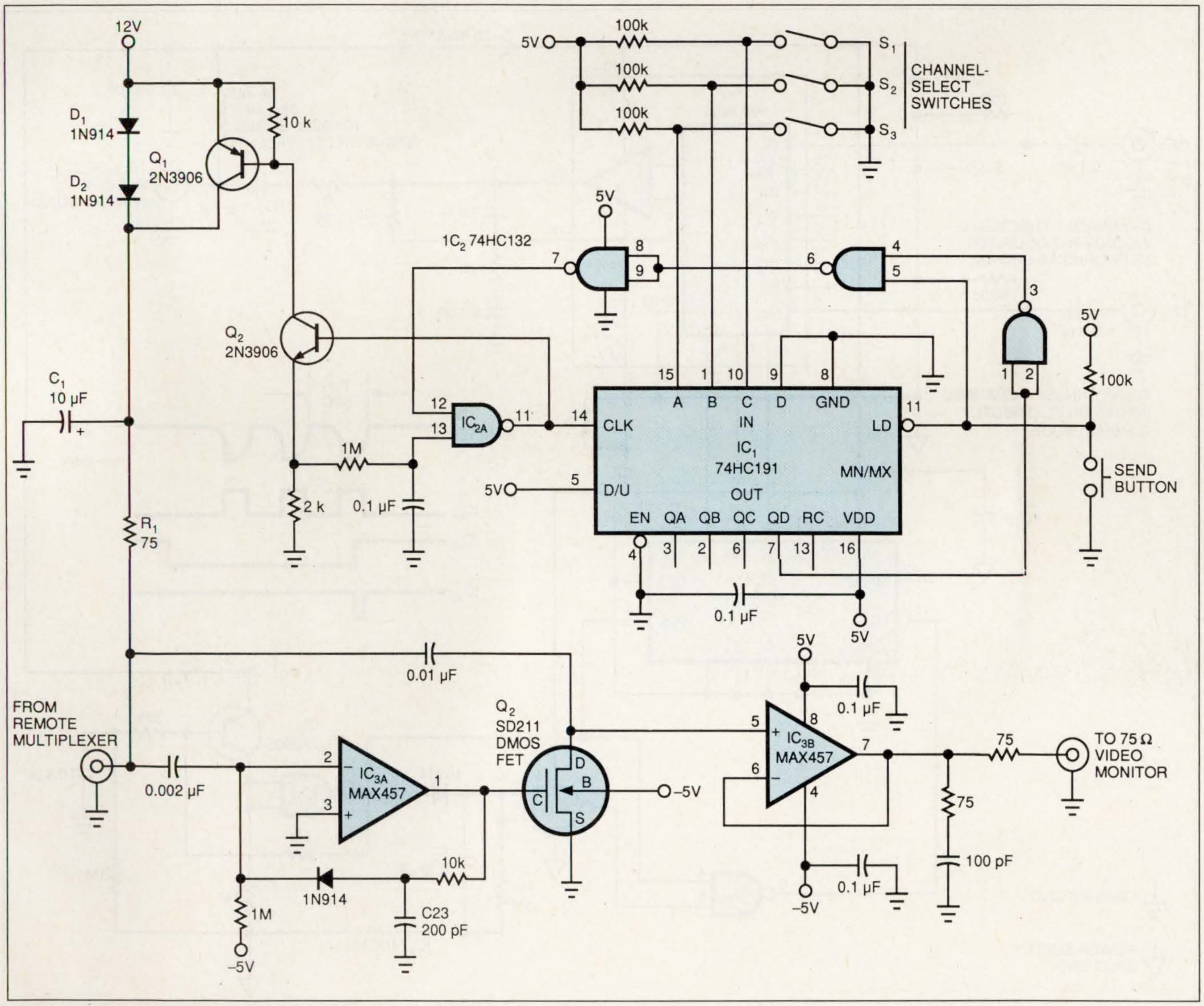


***Fig 2—The interface end of Fig 1**'s circuit delivers 10V down the cable, pulses the supply voltage to transmit channel-change commands, and buffers the received video signal.*

input. Momentary depression of the send button triggers down-counter IC_1 and gate oscillator IC_{2A}, which respond by initiating a channel-selection burst.

Supply current flows from the interface box to the remote multiplexer box through Q_1, which is normally on and saturated; R_1; and the coax center conductor. R_1 also terminates the coax via C_1. When Q_1 turns off momentarily, forward bias across D_1 and D_2 develops a negative 1.2V channel-select pulse. This 1.2V drop in supply voltage doesn't affect the remote multiplexer's video output. Consequently, the video monitor's display doesn't flip during channel changes, provided the channel signals have synchronous timing.

The multiplexer box (**Fig 3**) consists of an 8-channel multiplexer (IC_1) and an amplifier (IC_2). C_1 couples the multiplexer's baseband video output to the cable, and L_1 decouples the video from dc power arriving on the same line. The power, approximately 30 mA at 10V, drives all circuitry in the multiplexer box.

Channel-select input signals generated at the interface box—1 pulse for channel 0, 8 pulses for channel 7—pulse the circuit in **Fig 3**'s 10V supply to 8.8V and back at a 10-Hz rate. Q_1 and its associated components convert these pulses to 5V-logic levels that clock the 4-bit counter, IC_2. The counter in turn selects the desired multiplexer channel. The first pulse of a burst selects channel 0. Subsequent pulses that arrive before discharge of the timeout network R_2 and C_2 each advance IC_2 by one count. Thus, channel 0 appears almost instantly, and channel 7, when selected, appears near the end of a 0.8-sec burst.

The short time constant associated with coupling video to the cable—C_1 and R_1 in the multiplexer box in **Fig 3**, R_1 in the interface box in **Fig 2**—enables you

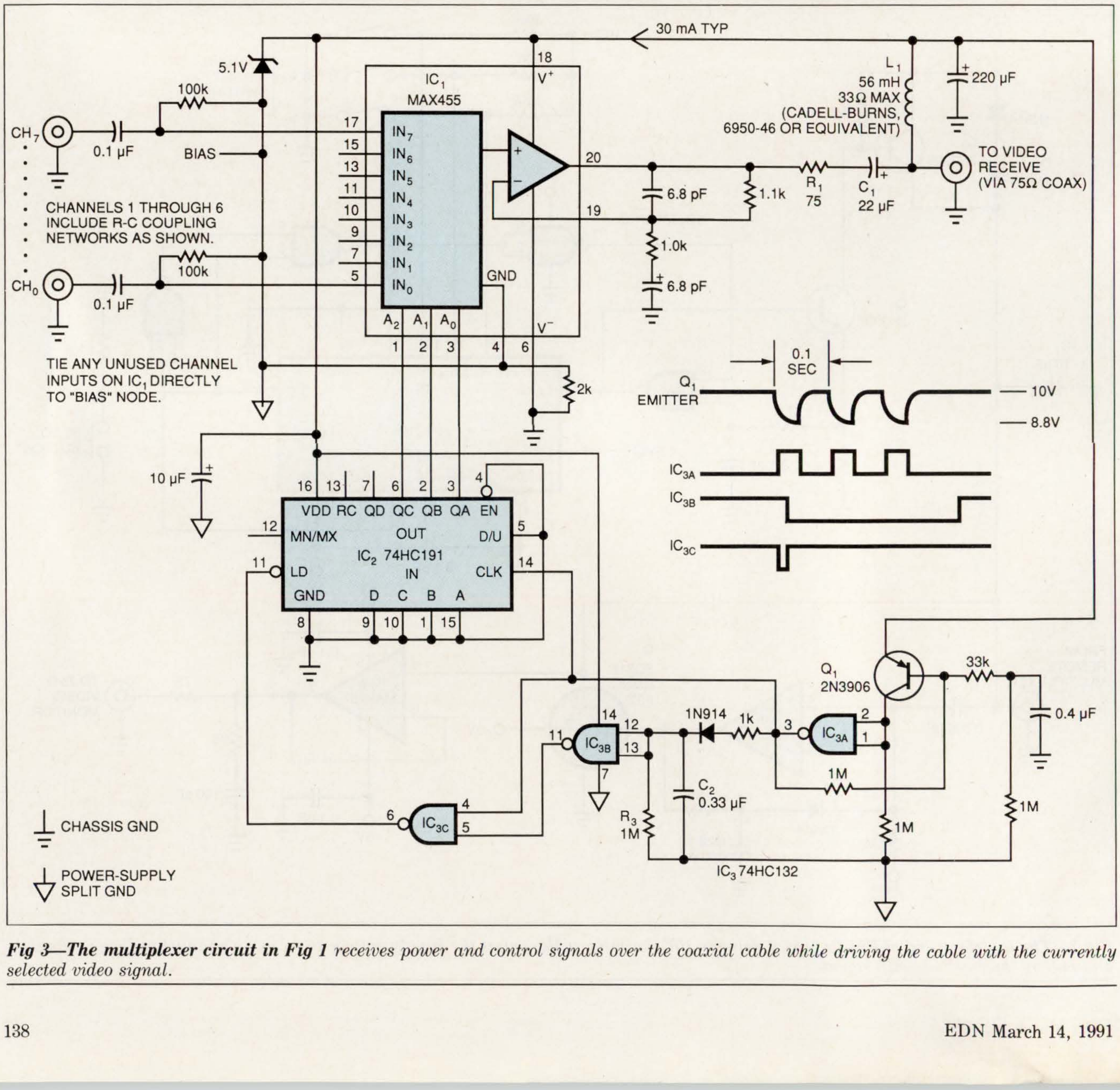


Fig 3—The multiplexer circuit in Fig 1 receives power and control signals over the coaxial cable while driving the cable with the currently selected video signal.

to select any channel in less than one second. But it also allows the composite video's synch-pulse baseline to shift with picture content. To counter this shift and its effect on the monitor's video synchronization, peak detector IC_{3A} drives DMOS FET Q_2, which applies dc restoration ahead of the video buffer IC_{3B} (**Fig 2**). During each negative sync pulse, Q_3 turns on just long enough to clamp the pulse tip at 0V.
(EDN BBS /DI_SIG #938) EDN

To Vote For This Design, Circle No. 748

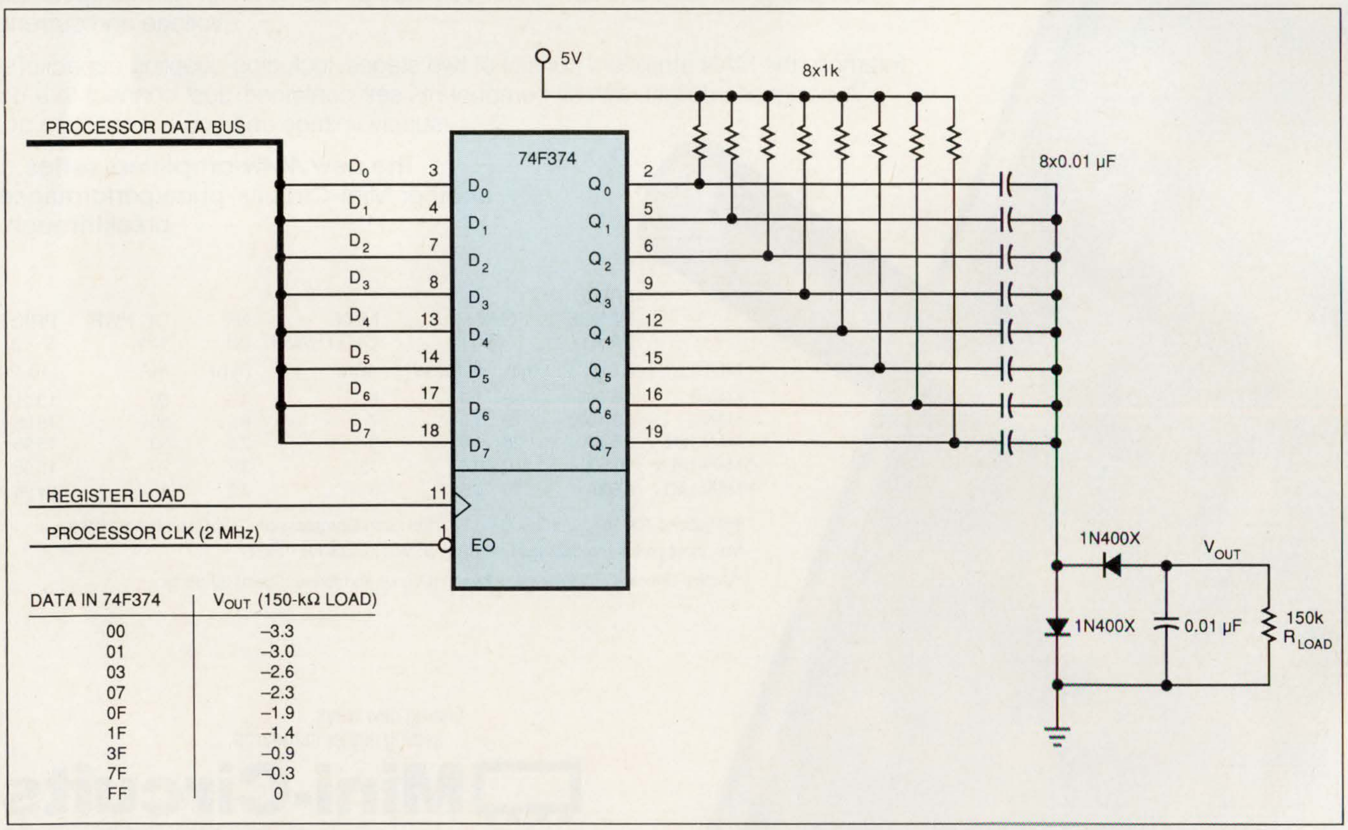
µP controls negative-voltage converter

Dan Kuechle
Network Systems Corp, Minneapolis, MN

The dc/dc converter in **Fig 1** produces a variable negative voltage using no coil or transformer. The circuit was designed to drive the contrast pin on an LCD display in a system without a negative supply. The LCD display needs a few microamps of negative voltage and has to be user-adjustable.

A 74F374 octal 3-state flip-flop register generates a square wave that the circuit ac-couples to the rectifier diodes and to the load. By controlling the number of zeros written into the flip-flop, the processor can control how many flip-flops are actively driving the load, and thus, how high the output voltage will be. The **figure** includes a table of approximate input words and output voltages. (**EDN BBS /DI_SIG #939**) EDN

To Vote For This Design, Circle No. 749



DATA IN 74F374	V_{OUT} (150-kΩ LOAD)
00	–3.3
01	–3.0
03	–2.6
07	–2.3
0F	–1.9
1F	–1.4
3F	–0.9
7F	–0.3
FF	0

Fig 1—The processor's data bus controls *the state of eight flip-flops that ultimately control the level of this negative voltage converter's* V_{OUT}.

Looking
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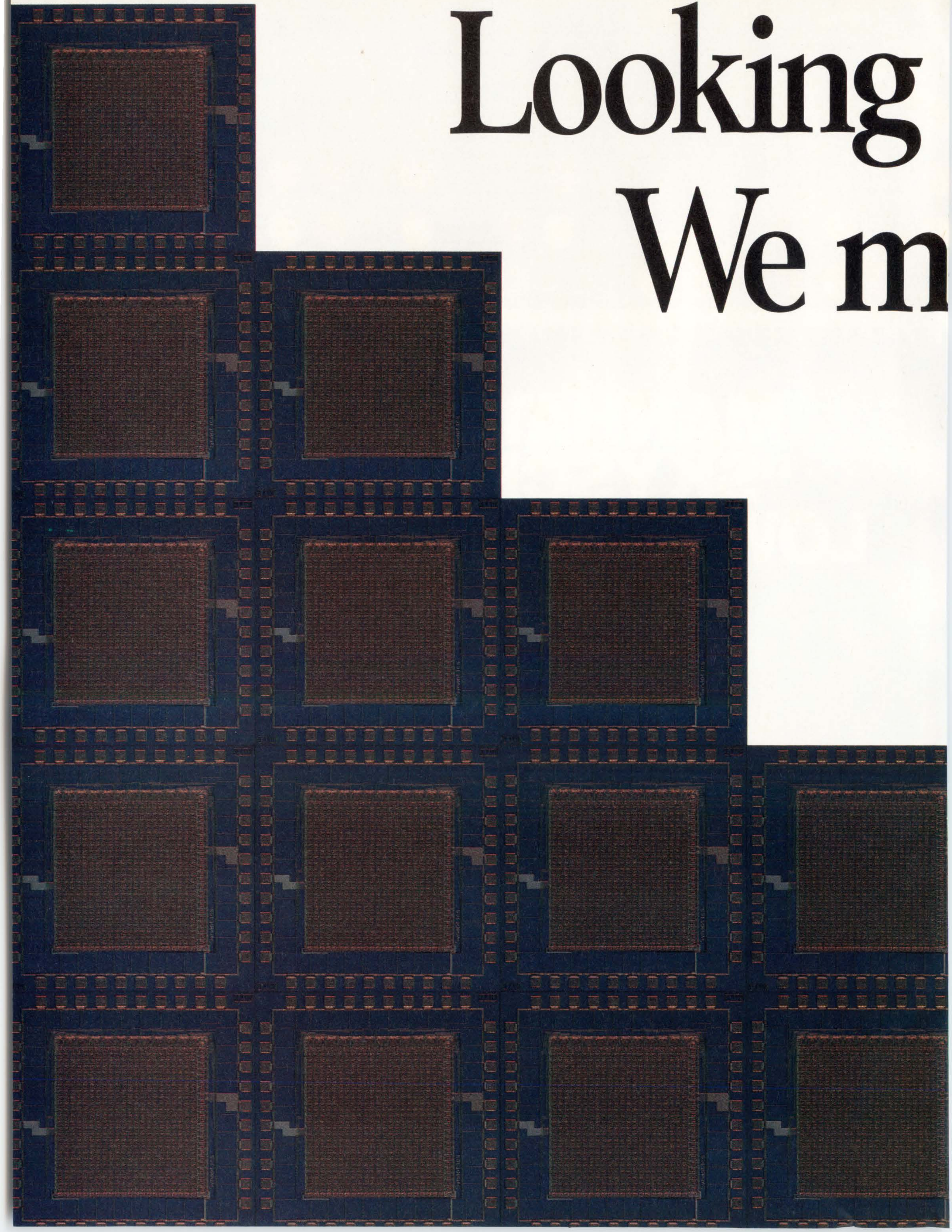

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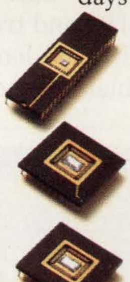

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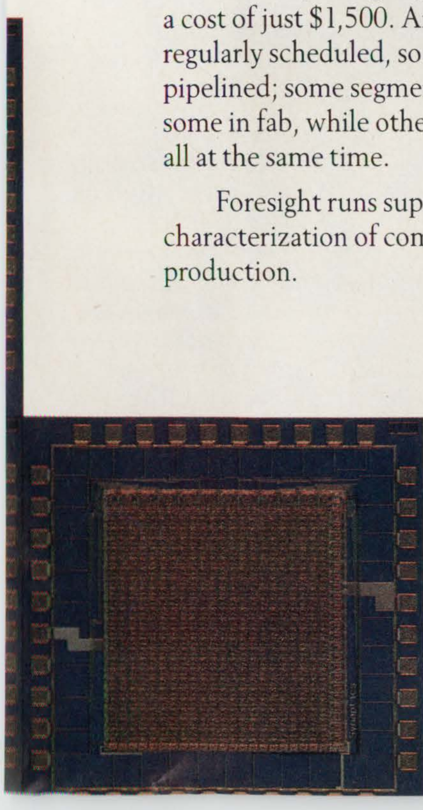

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CIRCLE NO. 71

TEST & MEASUREMENT INSTRUMENTS

Portable 500-Hz Oscillographic Recorder

- *Can have two or four channels*
- *Accepts plug-in signal conditioners*

The Easygraf is a 22-lb portable oscillographic recorder with 500-Hz frequency response. It accepts plug-in signal conditioners and uses fixed thermal elements to print one, two, or four analog traces; the chart grid; event markers; and alphanumeric annotation on 4-in.-wide, fanfolded paper. Resolution is 200 dpi. The analog traces can appear superimposed or side by side. The recorder samples each channel 5000 times/sec. Chart speed is variable from 0.01 to 100 mm/sec. The basic unit accommodates two plug-in signal conditioners from a new family called the 6600 series. Four-channel operation requires a companion case to hold the third and fourth conditioners. $3995; signal conditioners from $315.

Gould Inc, 8333 Rockside Rd, Valley View, OH 44125. Phone (216) 328-7264. FAX (216) 328-7400.

Circle No. 351

Factory Data-Collection Terminal

- *You can connect 160 terminals on an RS-485 loop*
- *Includes 64k bytes of nonvolatile memory*

The MEC-51 preprogrammed factory-data terminal automatically collects and processes data from production machinery; receives information that machine operators enter on its sealed hexadecimal keypad; displays data on an 8-digit LED display; and transmits data on a 2-wire RS-485 loop. As many as 160 terminals connect on a single 2-wire loop. The unit's inputs are optically isolated. The µP that controls the terminal has 64k bytes of nonvolatile RAM. Lotus Development Corp's 1-2-3/@Factory software helps you create reports from the data collected by the terminal. $895.

Manufacturing Technology, 578 Post Rd E, Suite 621, Westport, CT 06880. Phone (203) 454-8730.

Circle No. 352

RS-232C Tester

- *Performs eight functions*
- *Weighs 2.6 lb; uses three 9V batteries*

The DataTool 5500 is a 2.6-lb unit that receives power from three 9V batteries. It performs the following functions on RS-232C signals: data monitoring, bit error-rate testing, data trapping, device exercising,

and device simulation. It also operates as a breakout box, a pulse-level voltmeter, and a cable tester; it detects power dropouts during error-rate tests. The unit configures itself automatically to match the characteristics of the monitored data stream. You can download test setups and error messages to the tester; it stores this information in nonvolatile memory. It simultaneously analyzes the received and transmitted data streams and prints test data during tests. $1295.

Datacom Technologies Inc, 11001 31st Pl W, Everett, WA 98024. Phone (206) 355-0590. FAX (206) 353-9252. **Circle No. 353**

Multichannel Filter/Amplifier

- *Can have 64 channels*
- *Plug-ins let you program their gain and filter response*

The 9064 is a multichannel filter/amplifier. You can mount the 7-in.-high chassis in an EIA rack. The chassis, which accepts 16 plug-in cards, includes a power supply, a fan, a digital controller with battery-backed memory, a common bus for monitoring individual channels, and RS-232C and IEEE-488 ports. Plug-in cards contain two or four channels. The channels can be filters with fixed or programmable response and amplifiers with fixed or programmable gain. Lowpass filters can have 8-pole, Bessel, Butterworth, elliptic, or constant-delay response. Highpass filters can have 8-pole elliptic or Butterworth response. Programmable and fixed corner frequencies range from 1 Hz to 51.2 kHz ±2%. Unit-to-unit amplitude response tracks to ±0.05 dB; phase to 0.5°. Chassis, $4000; cards from $400. Delivery, six to eight weeks ARO.

Frequency Devices Inc, 25 Locust St, Haverhill, MA 01832. Phone (508) 374-0761. FAX (508) 521-1839. **Circle No. 354**

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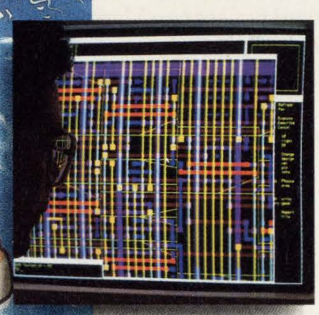

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MAS-90-035

CIRCLE NO. 74

COMPUTERS & PERIPHERALS

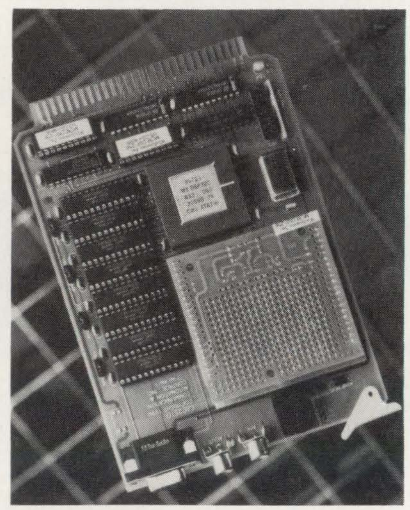
Optical Character Reader

- *Recognizes typeset fonts and bar codes*
- *Reads text from typewriters and dot-matrix printers*

The Datasweep 2 handheld optical character reader reads font sizes having from 6 to 20 points. It contains a database of common office fonts and special fonts such as OCR-A, OCR-B, and E13B. An option lets the unit read bar codes. The reader operates with IBM PCs or 100% compatible computers, running DOS 3.0 or higher and having a minimum of 256k bytes of memory. The software requires approximately 35k bytes of memory. The unit requires a full-sized expansion slot and can read from 25 to 30 cps. It can read data that is underlined or located within boxes with an accuracy >99.9%. Print quality the unit reads ranges from typewriter or laser-printer quality to dot-matrix draft mode. An RS-232C port is part of the unit. $1795.

Soricon Corp, 4725 Walnut St, Boulder, CO 80306. Phone (303) 440-2800. FAX (303) 442-2438.

Circle No. 367



DSP Board

- *Uses 50-MHz DSP32C chip for the STD bus*
- *Comes with either 64k or 256k bytes of zero-wait-state RAM*

The MCM-DSP32C DSP board for the STD bus features a 50-MHz AT&T DSP32C DSP chip that delivers 25M flops. It contains either 64k or 256k bytes of zero-wait-state RAM that has a 32-bit-wide data path. Benchmarks include executing a 1024-point complex FFT in 3.3 msec; multiplying a 4×4 matrix in 6.16 μsec; and calculating a complex adaptive FIR filter having 80 nsec/tap. The host can transfer data to the board as fast as 3.5M bytes/sec using programmed I/O transfers. Data transfer is independent of the

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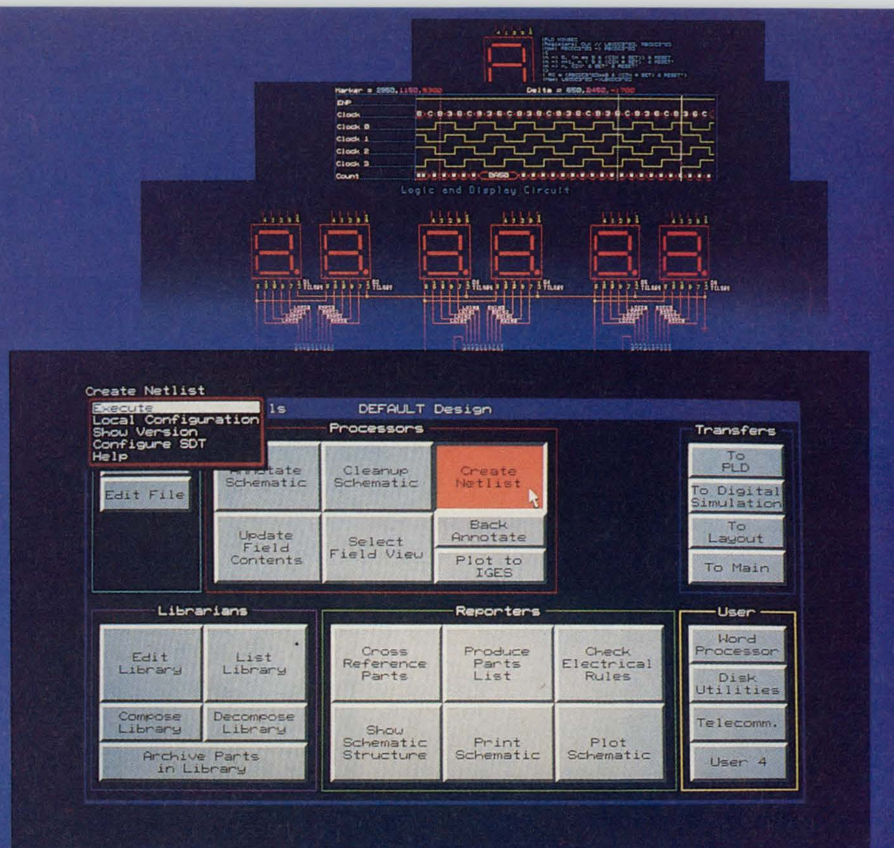
Release IV



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CIRCLE NO. 86

DSP's execution of a program. The DSP board can perform 8- or 16-bit data transfers on the STD bus. You have the option of adding a daughter board to provide serial I/O, a Codec, a 16-bit ADC, or prototyping space. $1495.

Winsystems Inc, 715 Stadium Dr, Suite 100, Arlington, TX 76011. Phone (817) 274-7553. FAX (817) 548-1358. **Circle No. 368**

Multibus II Adapter

- *Drives 32-bit devices using the HSD protocol*
- *Has data-transfer rate >3.5M bytes/sec*

The MBHSD adapter board for the Multibus II provides a bidirectional link to a 32-bit external device using the Gould/Encore HSD protocol. It can also connect the Multibus II system to a Gould/Encore HSD board or another MBHSD. The data-transfer rate is >3.5M bytes/sec. During data transfers, the board can reformat the words by byte swapping, word swapping, or word and byte swapping. The 6U board supports data transfers via the LBX bus or PSB interface. All features are software selectable. Board, documentation, and 20-ft ribbon cables, $4750.

Applied Data Sciences Inc, Box 814209, Dallas, TX 75381. Phone (214) 243-0113. FAX (214) 243-0217. **Circle No. 369**

Memory Cards

- *Available in full- and half-card formats*
- *Feature EEPROM or EPROM to transport data*

The Courier, a line of portable memory cards, features a selection of read/write EEPROM and one-time-programmable EPROM memories. The densities range from 256k to 1024k bits. Operating as in-circuit memory, the cards provide random access to data as fast as 300

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- Cost efficiency

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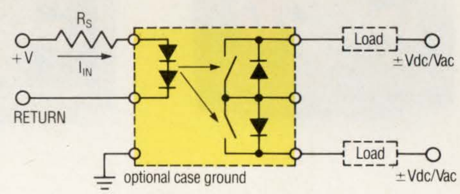
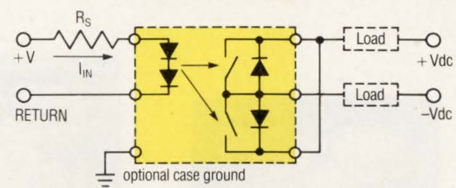
INPUT ELECTRICAL CHARACTERISTICS (−55° to +105° unless otherwise noted)			
	Min	Max	Units
Continuous Input Current (I_{IN})	10	50	mA_{DC}
Input Current (Guaranteed On)	10		mA_{DC}
Input Current (Guaranteed Off)		100	μA_{DC}
Input Voltage Drop at (I_{IN}) = 25mA		3.25	V_{DC}

OUTPUT ELECTRICAL CHARACTERISTICS (−55° to +105° unless otherwise noted)				
Part Number	**FB00CD**	**FB00FC**	**FB00KB**	**Units**
Bidirectional Load Current (I_{LOAD})	±1.0	±0.50	±0.25	A_{DC}/A_{PK}
DC Load Current (I_{LOAD})	2.0	1.0	0.5	A_{DC}
Bidirectional Load Voltage (V_{LOAD})	±80	±180	±350	V_{DC}/V_{PK}
DC Load Voltage (V_{LOAD})	80	180	350	V_{DC}
ON-Resistance (R_{ON}) at (I_{LOAD}) max.	0.72	1.8	12.9	Ohms
Turn-On Time (T_{ON})	800	800	500	µs
Turn-Off Time (T_{OFF})	300	600	500	µs

Notes: 1. A series resistor is required to limit continuous input current to 50mA (peak current can be higher).
2. Rated input current is 25mA for all tests.
3. Loads may be connected to any output terminal.
4. ON resistance shown is for the bidirectional configuration. The DC ON resistance is ¼ of these values.



B-directional and ac configuration



DC configuration

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CIRCLE NO. 95

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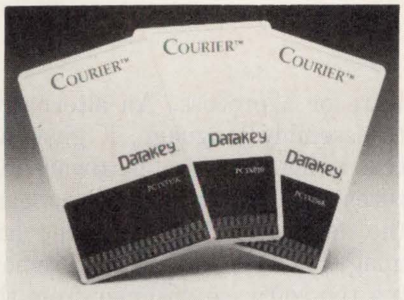
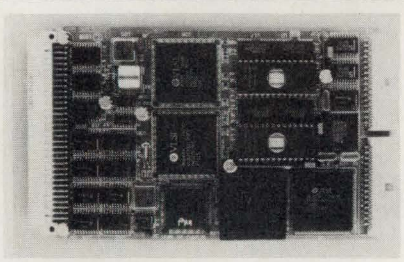
SII Seiko Instruments



nsec. The cards are well suited for use in compact systems where they serve as an alternative to disk or tape drives. Both full- and half-card formats are available. The cards attach to the host system via a 38-pin connector. The contacts are gold plated and have a rating of 10,000 insertion-removal cycles. The nonvolatile memories retain data for a minimum of 10 years; they require a 5V supply. Three EPROM cards have the following data formats: 32k × 8 bits, 64k × 8 bits, and 128k × 8 bits. An EEPROM card has a 32k × 8-bit format. $18 to $130.

Datakey Inc, 407 W Travelers Trail, Burnsville, MN 55337. Phone (612) 890-6850. **Circle No. 370**



Single-Board Computer

- *Uses an 80386-SX for the G-64/96 bus*
- *IBM PC/AT compatible*

The GESMPU-38 single-board computer for the G-64/96 bus comes on a 100 × 160-mm Eurocard. It uses an 80386-SX μP and 80387-SX coprocessor, running at either 16 or 20 MHz. The board is IBM PC/AT compatible and comes with 1M, 2M, 4M, or 8M bytes of dynamic RAM arranged in one, two, or four banks. The board has hardware support for the LIM EMS 4.0 extended memory standard as well as ROMBIOS and VideoBIOS. Other features include a page-address register, a timer, an interrupt controller, port B logic, a real-time clock calendar with 114 bytes of battery-backed CMOS RAM, a DMA controller, and a PC/AT-compatible keyboard controller. Two serial ports, a bidirectional parallel-printer port (LPT1), a 37C65B floppy-disk controller, and an IDE hard-disk port also come with the board. $2195 with 1M byte of RAM.

Gespac Inc, 50 W Hoover Ave, Mesa, AZ 85210. Phone (602) 962-5559. **Circle No. 371**

CAE & SOFTWARE DEVELOPMENT TOOLS

CAE Routing Tool

- *Automatic and interactive routing*
- *Postscript and HP Laserjet outputs*

Version 2.0 of Pads-2000 includes many features that, according to the manufacturer, are superior to those in more expensive workstation-based CAE systems. A major enhancement is T-Routing, the ability to route from any track within a net to any other pin, via, or track segment within the same net. You can start from or tie into a track using a "T" without having to finish at a component pin. If you "T" into another track and your operation results in an excessive track length on your board, the T-Routing feature automatically cleans up and removes the excess track. The feature also works in interactive mode. The tool allows micro vias in addition to existing through vias and blind/buried vias. Text and graphics symbols can rotate 360° in 0.1° increments. $5995.

CAD Software Inc, 119 Russell St, Suite 6, Littleton, MA 01460. Phone (508) 486-9521. FAX (508) 486-8217. **Circle No. 372**

Software Tool For Machine-Level Coding

- *An alternative to using an assembler*
- *Prompts for inputs and checks for syntax errors*

M-Code Personal, a software tool that runs on PCs, lets engineers, technicians, and scientists who write small programs control hardware or a process. An alternative to assembly language, it gives access to machine-level hardware features and doesn't force you to learn the details of a programming language. In fact, rather than removing the software designer from the hardware as languages try to do, M-Code takes you to the hardware and helps automate coding for it. Interactive prompts and syntax checking help you create code; no edit/assemble/link sequence is necessary. You simply create your code, save it to disk, rename it as a COM file, and run it. As an alternative, you can develop code for PROM-based remote target systems. The tool allows programs as large as 64k bytes and comes with a small library of routines. An optional source-code package includes

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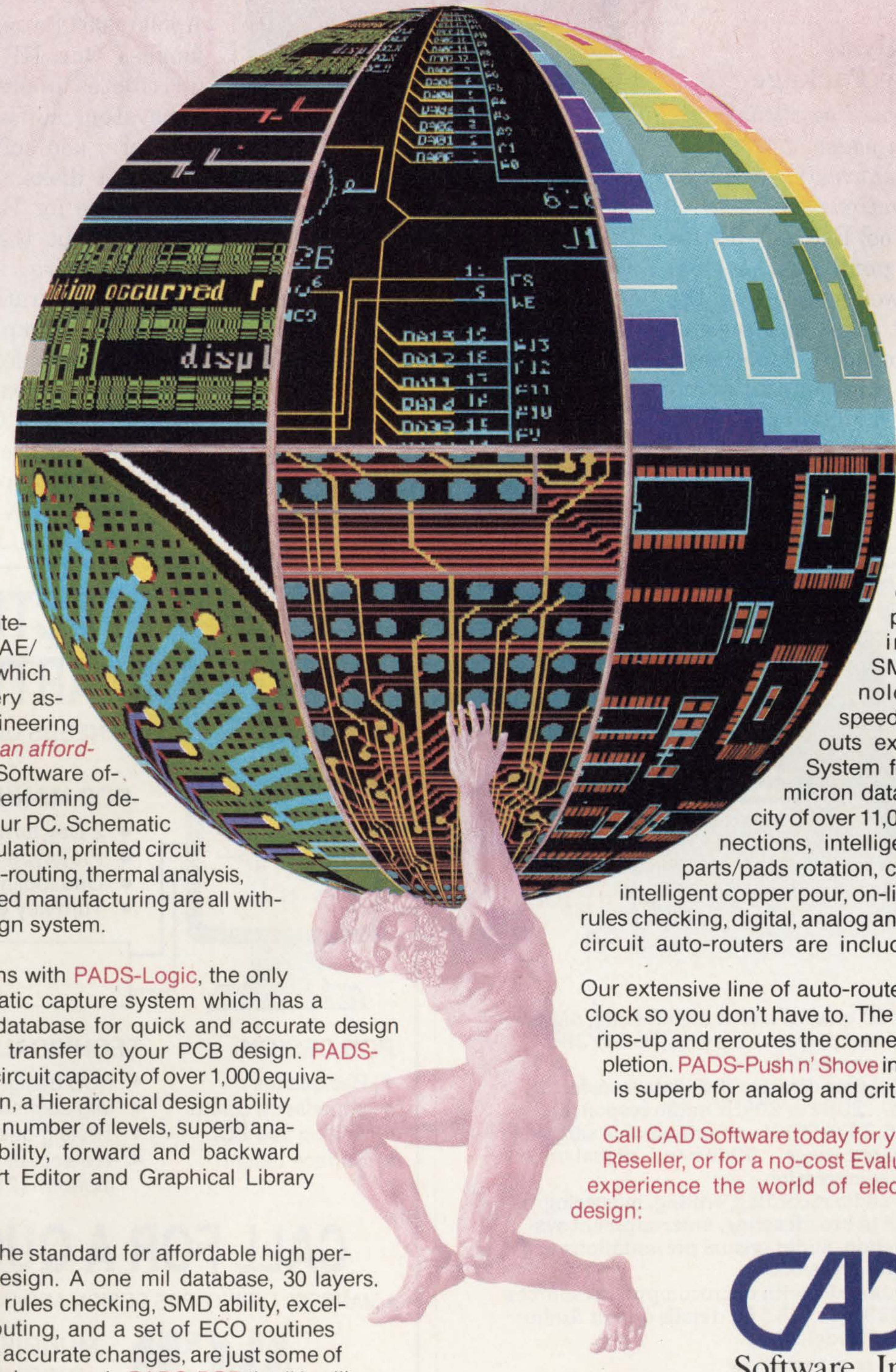

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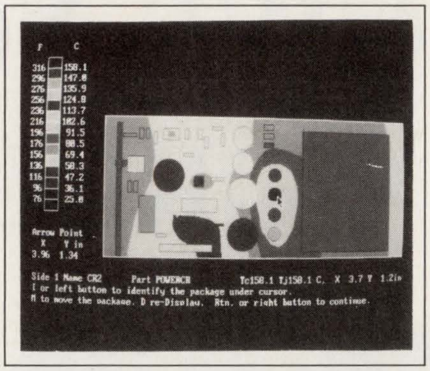
routines for keyboard, display, and ASCII conversion. M-Code Personal, $99.95; source-code package, $29.95.

DOSystems Inc, Box 4601, Carmel, CA 93921. Phone (408) 625-9016. **Circle No. 373**

Thermal-Analysis Power-Supply Package

- *Performs thermal analysis during design phase*
- *Used for transformers, capacitors, and resistors*

CAE software tool Betasoft-R runs on a PC and performs thermal analyses of power supplies in the design stage. It takes into account various transformers, capacitors, and resistors in addition to the microelectronics of a supply. The power supply can be at any elevation, under natural or forced-air cooling, and with various heat sinks



or heat-spread planes attached. The software can model 3-D flow and thermal fields and can interface with CAE products from Mentor, Valid, P-CAD, AutoCAD, OrCAD, RPP, and Relex. The tool runs on DOS-based PCs that have 640k bytes of memory and an EGA display. $1995.

Dynamic Soft Analysis Inc, 213 Guyasuta Rd, Pittsburgh, PA 15215. Phone (412) 781-3016. FAX (412) 781-3098. **Circle No. 374**

Software On CD-ROM

- *Replaces magnetic tape and printed documentation*
- *Allows keyword search of documentation*

Two types of software are now available on CD-ROM for users of the HP 9000 Series 300 and the HP Apollo 9000 Series 400 workstation families. One, HP Laser-release/UX distributes operating-system and subsystem software, application software, and software updates on CD-ROM disks. The other, Software Store for HP, contains information about third-party applications software, including promotions, demonstrations, on-line documentation, company information, and ordering information. Updates to HP Laser-release/UX go to users monthly on CD-ROM disks; updates to Software Store for HP are quarterly. Software provided with HP Laser-release/UX includes the HP-

UX 8.0 operating system, select HP application software, the OSF/Motif graphical user interface, and subsystem modules that include compilers, network software, and graphics software. A full-text-retrieval software package based on OSF/Motif allows users to search the software's documentation for keywords. With Software Store for HP, users can choose a point-and-click procedure to review a variety of applications software. A printed buyers' guide also comes with each CD-ROM disk. The supplier also sells CD-ROM hardware for all of its systems running HP-UX. HP Laser-release/UX, from $495; Software Store for HP is free.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.
Circle No. 375

Line- And Bus-Design Software

- *For high-bit-rate data transmission on strip lines*
- *Calculates transmission-line matrices*

K G Line Design, a CAE program, performs design calculations for low-crosstalk, high-bit-rate data transmission on multiwire lines and buses. The program calculates the impedance-matching (no crosstalk, no reflection) network elements from the line's geometry; it also calculates the crosstalk due to mismatch for any termination network as well as the crosstalk that develops as a pulse propagates along the line. It can also calculate the gains for an unscrambler-decoder (to "undo" the crosstalk) if it appears to be the best solution. The software runs on IBM PCs and compatible computers. Regular 45-wire version, $475; demo 3-wire version, $5.

Kenneth D Granzow Consultant, 1079 Haverhill Pl, Colorado Springs, CO 80919. Phone (719) 528-6784. **Circle No. 376**

Here's where the barricades start to come down in the mixed signal revolution.

North American Locations & Dates

Cedar Rapids, IA March 18
Cleveland, OH March 19
Pittsburgh, PA March 20
Atlanta, GA March 25
Clearwater, FL March 26
Orlando, FL March 27
Huntsville, AL March 28
Waltham, MA April 1
Saddlebrook, NJ April 2
Westchester, NY April 3
Smithtown, NY April 4
Cromwell, CT April 5
Santa Clara, CA April 8
Costa Mesa, CA April 9
Los Angeles, CA April 10
Woodland Hills, CA April 11
San Diego, CA April 12
McLean, VA May 6
Baltimore, MD May 7
Cherry Hill, NJ May 8
Fort Washington, PA May 9
Raleigh, NC May 10
Toronto, Canada May 13
Santa Clara, CA May 14
Pleasanton, CA May 15
Bellevue, WA May 16
Beaverton, OR May 17
Woburn, MA May 20
Montreal, Canada May 21
Bloomington, MN May 22
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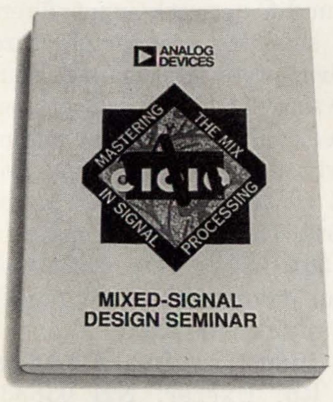

With the revolution in mixed signal technology, digital designers now need to know about analog. And the analog guys can no longer turn their backs on digital.

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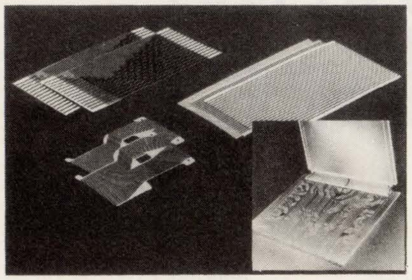


Flexible Connectors

- *Available with carbon or carbon-silver traces*
- *Designed for pc-board applications*

J-Type flexible connectors are designed for board-to-LCD or board-to-board applications. The line consists of units with carbon (JC Type) or carbon-silver (JS Type) traces screened to a polyester substrate. An anisotropic conductive thermoplastic is then applied over either the bonding-interface surface or the entire surface. The polyester material is typically 0.025 mm thick, but other thicknesses are available. JS-Type devices have a trace pitch as small as 0.3 mm using 0.15-mm trace widths. JC units have a minimum pitch of 0.5 mm and use trace widths of 0.25 mm. JC connector measuring 30×49 mm with 27 traces on 1-mm centers, $0.10 (1000).

Shin-Etsu Polymer America, 34135 7th St, Union City, CA 94587. Phone (415) 475-9000. FAX (415) 475-0613. **Circle No. 361**

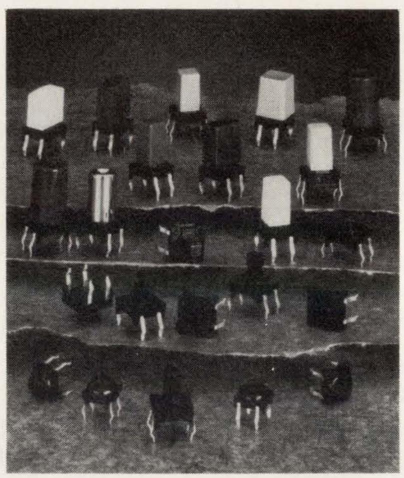
Optical Encoder

- *Housed in a 2-in.-diameter package*
- *Has a fully sealed design*

The H20 rugged industrial optical encoder is housed in a 2-in.-diameter package. It features an 80-lb load bearing, and an aluminum housing that is fully sealed against oil and water splash. An unbreakable code disk provides as many as 600 cycles/turn (2400 counts/turn) on two quadrature channels. Zero index is also available. The unit operates from a supply of 5 to 24V and employs a single LED source. Hollow- and through-shaft versions are also available. Additional options include tethered mounting arrangements, sealed cable or environmental connectors, and a variety of mounting configurations. $100 (OEM qty).

BEI Motion Systems Co, Industrial Encoder Div, 7230 Hollister Ave, Goleta, CA 93117. Phone (800) 350-2727; in CA, (805) 968-0782. FAX (805) 968-3154.

Circle No. 362



Miniature Keyswitches

- *Designed for logic-level switching applications*
- *Measure only 7 mm square*

CDS710 and CDS720 Series miniature keyswitches measure only 9 and 7 mm square, respectively. Both lines are designed for analog or digital logic-level switching and are TTL and MOS compatible. The snap-dome construction provides a positive tactile feedback and an audible response. The switches will handle loads of 1 to 20V dc. Terminations on the 710 are designed for pc-board mounting on a 0.1-in. grid. Switch housing material is polycarbonate, and the contact/dome spring is made of silver-plated phosphor bronze. Terminals are brass plated to enhance solderability. All units meet IEC 68, UL 94V-0, UN-D 1119, and UN-L 1152 test standards. CDS710, $0.219; CDS720, $0.145 (10,000).

CRL Components Inc, Highway 20 West, Fort Dodge, IA 50501. Phone (515) 573-1300. FAX (515) 573-1342. **Circle No. 363**

DC/DC Converters

- *Feature a wide input range*
- *Develop a 30W output*

SIW dc/dc converters accept inputs of 9 to 36V and 20 to 72V and develop single, dual, or triple outputs of 5 to 48V in 15 or 30W versions. Standard converter features include an LC-network input filter, 6-sided shielding, overtemperature shutdown, protection against input voltage surges, short-circuit protection via current limiting, and intrinsic reverse-polarity protection. Typical converter efficiency measures 85%. The units are housed in a 3×2.56×0.84-in. case which features an industry-standard pinout configuration. $100 (25).

Wall Industries Inc, 5 Watson Brook Rd, Exeter, NH 03833. Phone (800) 321-9255; in NH, (603) 778-2300. **Circle No. 364**

VME Chassis

- *Can accommodate two drives*
- *Comes with a power supply*

The VCV-11/Model 38 chassis includes a 3-slot card cage, which accommodates 6U×160 VME cards, a J1 backplane, and mounting and power wiring for two half-height drives. If the application requires it, a J2 backplane is available. The chassis features a function-control panel, which includes Reset and

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	MP7541/A	MP7542
	MP7543,	MP7542G
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	MP7645,	MP7623
		MP7680/A
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16-bit	MP7616,	MP7626/36A
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Micro Power Systems

3100 Alfred St., Santa Clara, CA 95054

CIRCLE NO. 84

Abort switches and Sysfail and DC-ok indicators. The unit comes with a 300W power supply and two fans that have 75-cfm moving capabilities. Airflow is side to side through the card cage. The chassis is designed for mounting in a 19-in. RETMA rack, but a decorative cover is available for desk-top applications. $1000. Delivery, four to six weeks ARO.

Zoltech Corp, 7023 Valjean Ave, Van Nuys, CA 91406. Phone (818) 780-1800. FAX (818) 780-1978.

Circle No. 365

Motor Control

- *Handles 10-hp motors*
- *Regulates speed within ±2%*

The 2745-10 controls the speed and direction of dc motors as large as 10 hp. The units have an isolated μP/TTL-compatible (10-bit parallel input) speed input or an isolated analog voltage (±5V) speed input. The control features 1500V dc isolation between signal inputs and motor/power line outputs. A failsafe circuit brings the motor to a full stop if the control signal is not present, preventing unsafe or uncontrolled operation. The unit regulates motor speed within ±2% against line and load variations. All controls are set at the factory for use with 180V dc motors. The unit is packaged on an open-frame heatsink bracket. Built-in forced-air cooling fans are included. Plug-in boards for acceleration and deceleration control, encoder feedback, and electronic braking are available. $574 (100). Delivery, stock to 10 weeks ARO.

Powr-Ups Corp, 1 Roned Rd, Shirley, NY 11967. Phone (516) 345-5700. FAX (516) 345-3106.

Circle No. 366

NEW PRODUCTS

INTEGRATED CIRCUITS

Current-Feedback Op Amp

- *Has 150-MHz bandwidth*
- *Operates from ±5V supply*

The EL2171 current-feedback op amp provides a bandwidth of 150 MHz at a gain of 20. The device, which is stable at gains beyond ±7, has a typical phase deviation of 0.2° at 50 MHz. Current drain with a ±5V supply is only 15 mA. Rise and fall times are 2.5 nsec for a 2V step, and settling time to 0.1% is 10 nsec. The company also offers the EL2071, which is identical to the EL2171 except for the addition of a disable pin that turns the amplifier on and off in 200 nsec. Samples are available now in 8-pin DIP and SO packages. EL2171, from $8.45; EL2071, $8.70 (100).

Elantec, 1996 Tarob Ct, Milpitas, CA 95035. Phone (408) 945-1323. FAX (408) 945-9305. TWX 910-997-0649. **Circle No. 355**

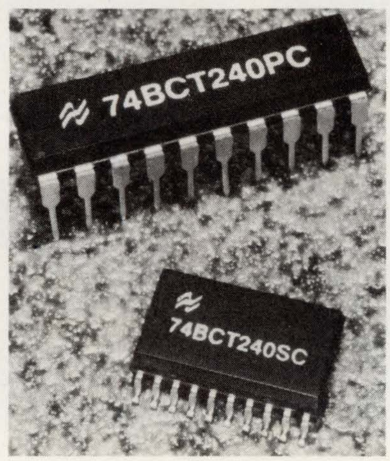
Micropower Op Amp

- *Operates at 1.2 μA*
- *Offset voltage is 0.5 mV*

Designed for low-voltage, battery-powered applications, the MAX406 op amp needs only 1.2 μA max of supply current. The amplifier operates from a single supply of 2.4 to 10V or from dual supplies of ±1.2 to ±5V. The ultralow quiescent current extends the operating life of a battery to its shelf life. When powered from a 9V battery, the op amp's output can source 2 mA. The output voltage swings rail-to-rail while the input-voltage range extends down to the negative supply rail. An input bias current of 0.1 pA typ and an input offset voltage of 0.5 mV max minimize errors when amplifying low-level signals. Two pin-selectable operating modes optimize stability and speed for a range of designs. In the unity-gain mode, which is optimized for stability, the gain-bandwidth product is typically 8 kHz, and slew rate is 5V/msec. In the high-speed mode, the gain-bandwidth product is typically 40 kHz, and slew rate is 20V/msec with the device remaining stable at gains of two or more. The MAX406 is available in 8-pin DIP and SO packages. From $3 (1000).

Maxim Integrated Products, 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No. 356



BiCMOS Logic Family

- *Can drive heavily loaded buses*
- *Can source 15 mA, sink 64 mA*

When fully released, the 54/74BCT family of BiCMOS logic devices will include more than 60 logic functions. The first two are the 74BCT240, an inverting octal buffer/line driver with 3-state outputs, and the 74BCT2240 octal buffer/line driver with a 25Ω series output termination. With a source/sink-current capability of 15/64-mA, all BCT devices can drive heavily loaded capacitive buses. The devices have a typical propagation delay of 2.5 nsec. In the case of multiple output drivers, the devices also feature a guaranteed skew of less than 1.5 nsec between drivers. The logic devices are available in plastic DIP and SOIC packages. The 74BCT240, $1.50; the 74BCT2240, $1.92 (100).

National Semiconductor, Box 58090, Santa Clara, CA 95052. Phone (207) 775-8868.

Circle No. 357

4M-Bit EPROM In PLCC Package

- *Organized 256k×16 bits*
- *Access times are 150 or 200 nsec*

Organized as 256k×16 bits, the 27C240 4M-bit EPROM is available in both 40-pin ceramic DIPs and 44-pin PLCCs (plastic leaded chip carriers). According to the company, the PLCC version has the smallest footprint of any 4M-bit EPROM currently available. The chip's 16-bit width makes it useful in 16- and 32-bit systems. Key specifications include access times of 150 nsec or 200 nsec, and a standby current drain of 100 μA. The EPROM accommodates a minimum of 50 programming cycles and provides 10 years of data retention. 150-nsec version in a PLCC package, $62.75; in a ceramic DIP, $67 (100).

Philips Components-Signetics, Box 3409, Sunnyvale, CA 94088. Phone (408) 991-2000.

Circle No. 358

Smart-Power, 3-Phase High-Voltage Bridge

- *Rated at 600V and 30A*
- *Can operate from a 270V bus*

Designed for driving high-power motors, the PWR-82333 features a maximum continuous current rating of 30A. The smart-power hybrid IC contains six insulated-gate bipolar transistors (IGBTs) and six antiparallel fast-recovery diodes connected in a 3-phase bridge arrangement. Each IGBT is driven from an internal level translator, which has programmable logic inputs of 0 to 5V and 0 to 15V. Internal protection

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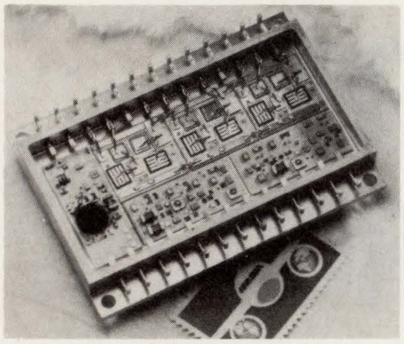


circuitry prevents in-line transistors from simultaneous conduction. An external shut-down input provides fast turn-off of the output drive stage. Digital input circuits provide compatibility for all types of motor controllers. The hybrid also has a constant-voltage drive stage, which provides uninterrupted performance even in a stalled-motor situation. Housed in a $3.0 \times 2.1 \times 0.39$-in. copper package, the PWR-8233 offers a low thermal resistance of 0.85°C/W. Unit pricing, from $1250. Delivery, stock to 12 weeks ARO.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600, ext 420. FAX (516) 567-7358. **Circle No. 359**

T1/E1 Transceivers

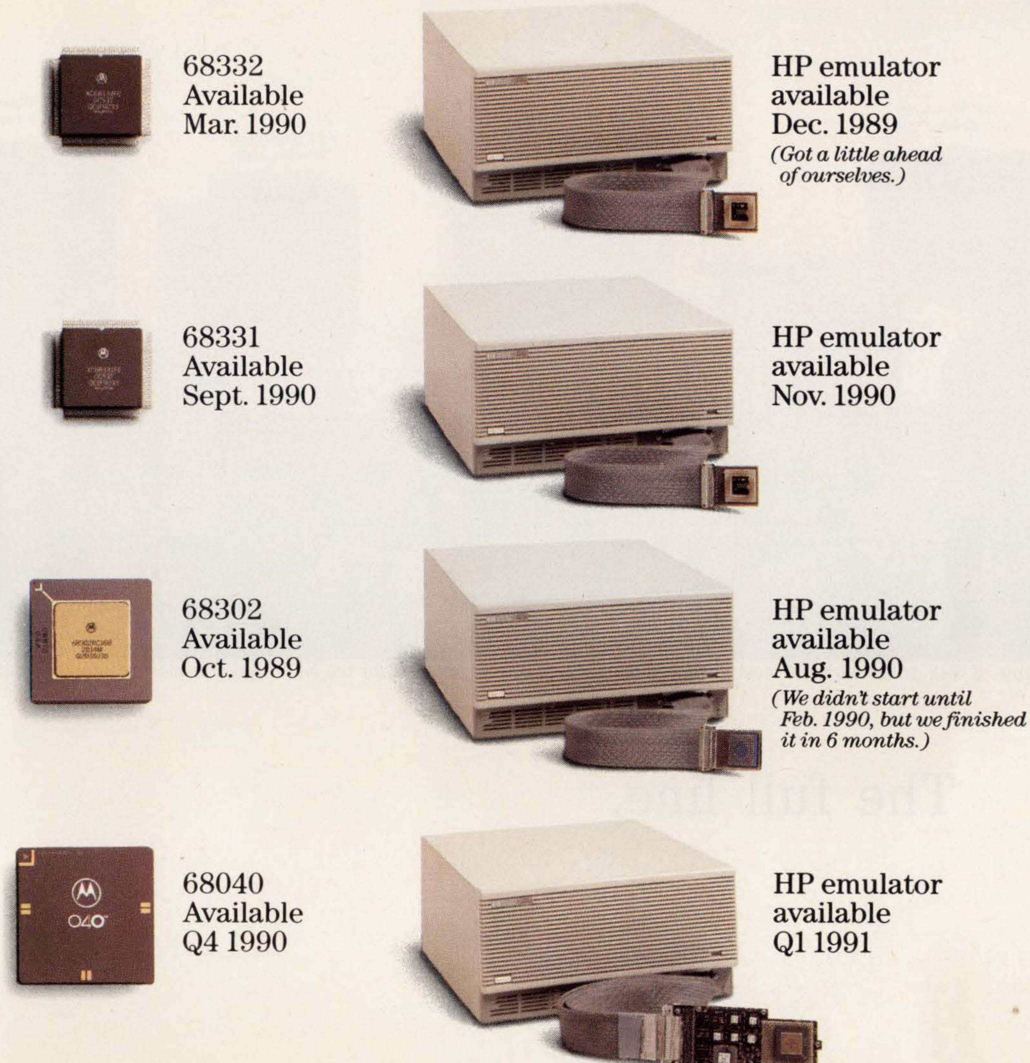
- *Operate at low power*
- *Provide jitter attenuation*

The LXT304A and LXT305A are T1/E1 PCM baseband transceivers for use in the design of T1/E1 multiplexers, SONET equipment, and PCM channel banks. The transceivers' low power requirement of 400 mW permits higher densities in applications with fixed power budgets, such as remote switching units. The LTX304A, which provides jitter attenuation on the receiver side, offers diagnostic features including transmit/receive signal monitoring.

Transmit pulse shapes are programmable for various line lengths and cable types. The LXT305A is a similar device, except that it provides jitter attenuation on the transmit side. The devices, which work over a temperature range of −40 to 85°C, are available in 28-pin DIP and 28-pin PLCC (plastic leaded chip carrier) packages. From $15.75 (1000).

Level One Communications, 105 Lake Forest Way, Folsom, CA 95630. Phone (916) 985-3670.

Circle No. 360



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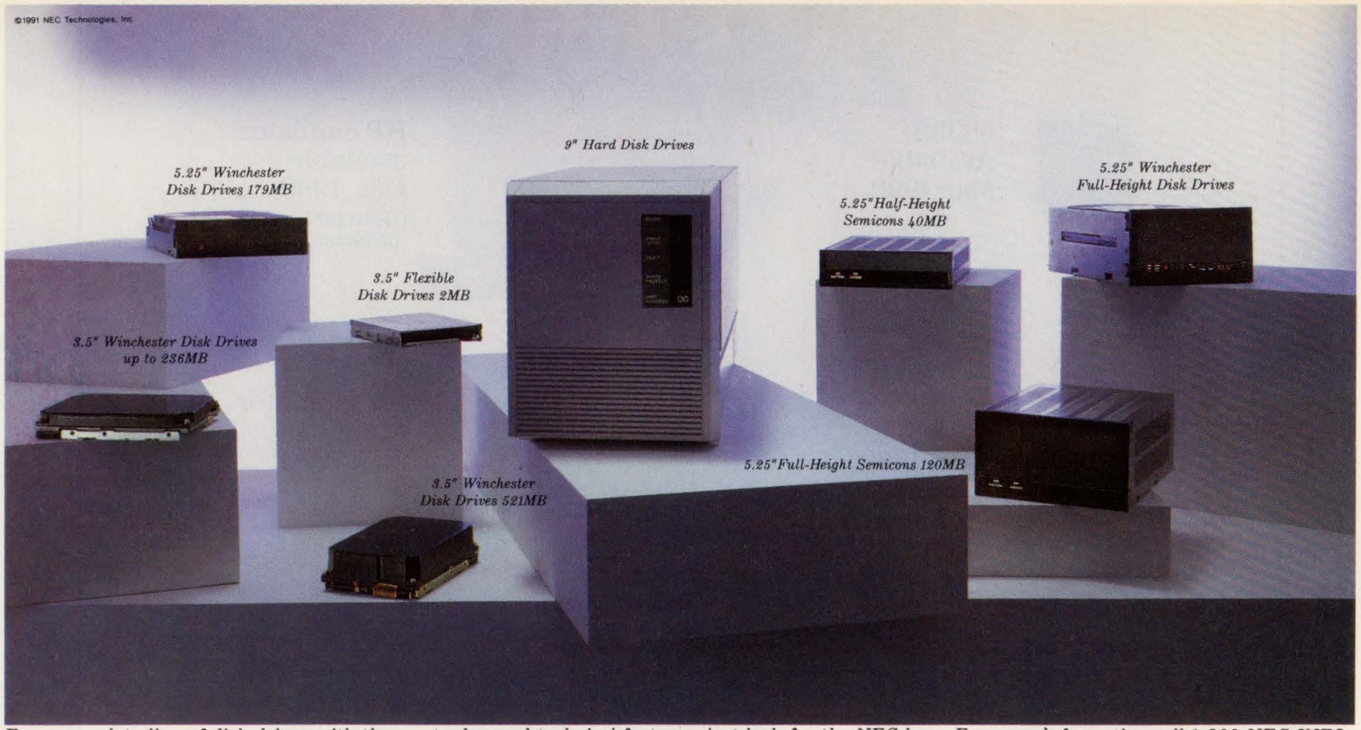

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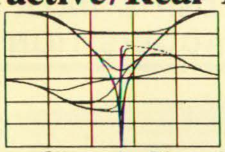

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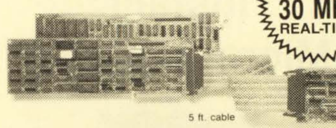

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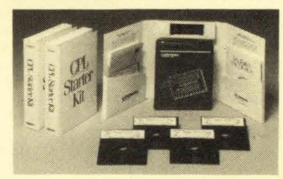

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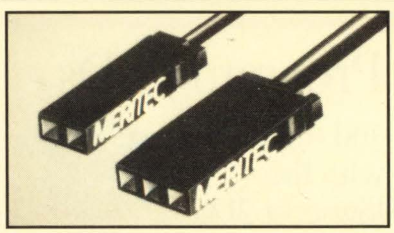

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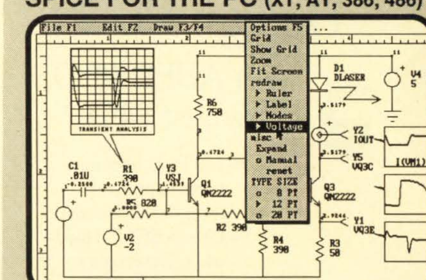

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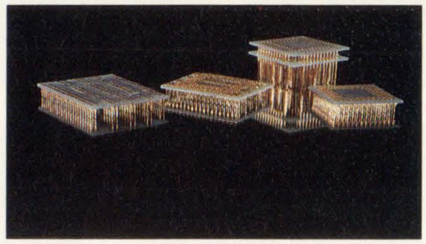

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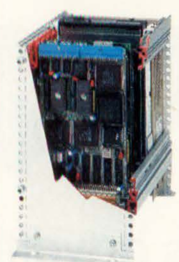

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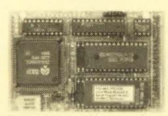

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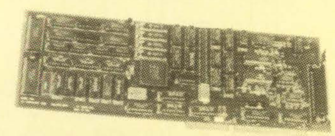

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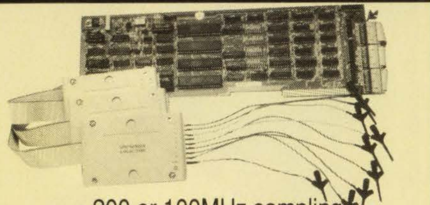

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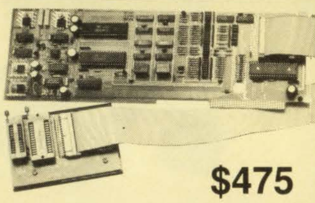

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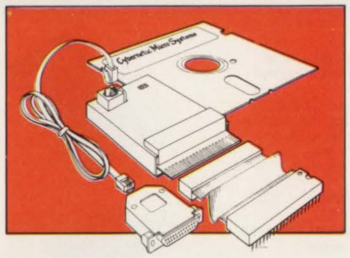

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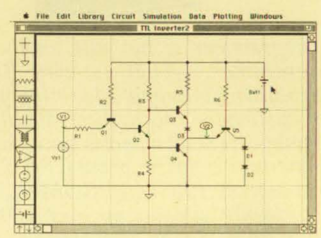

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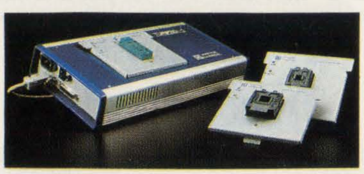

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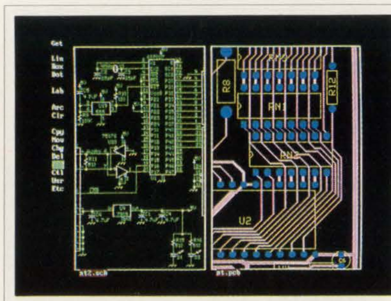

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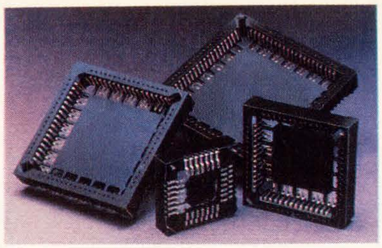

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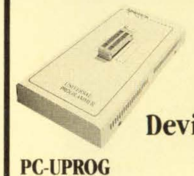

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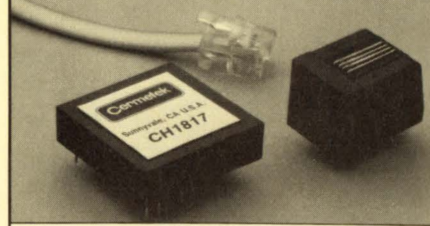

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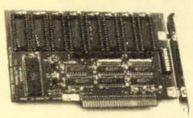

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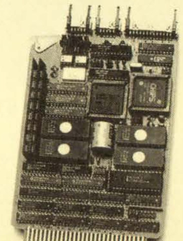

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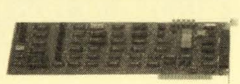

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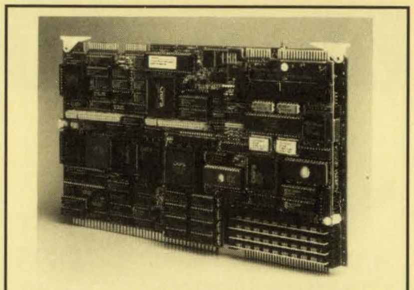

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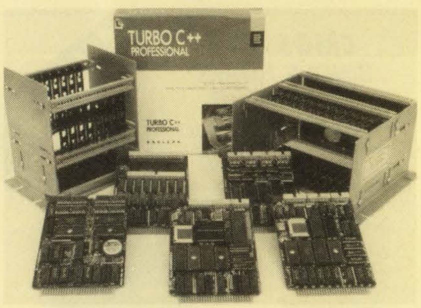

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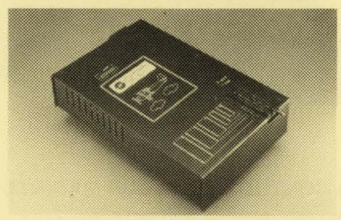

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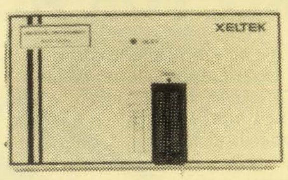

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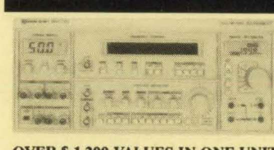

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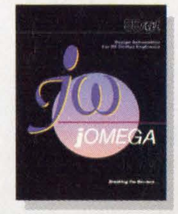

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