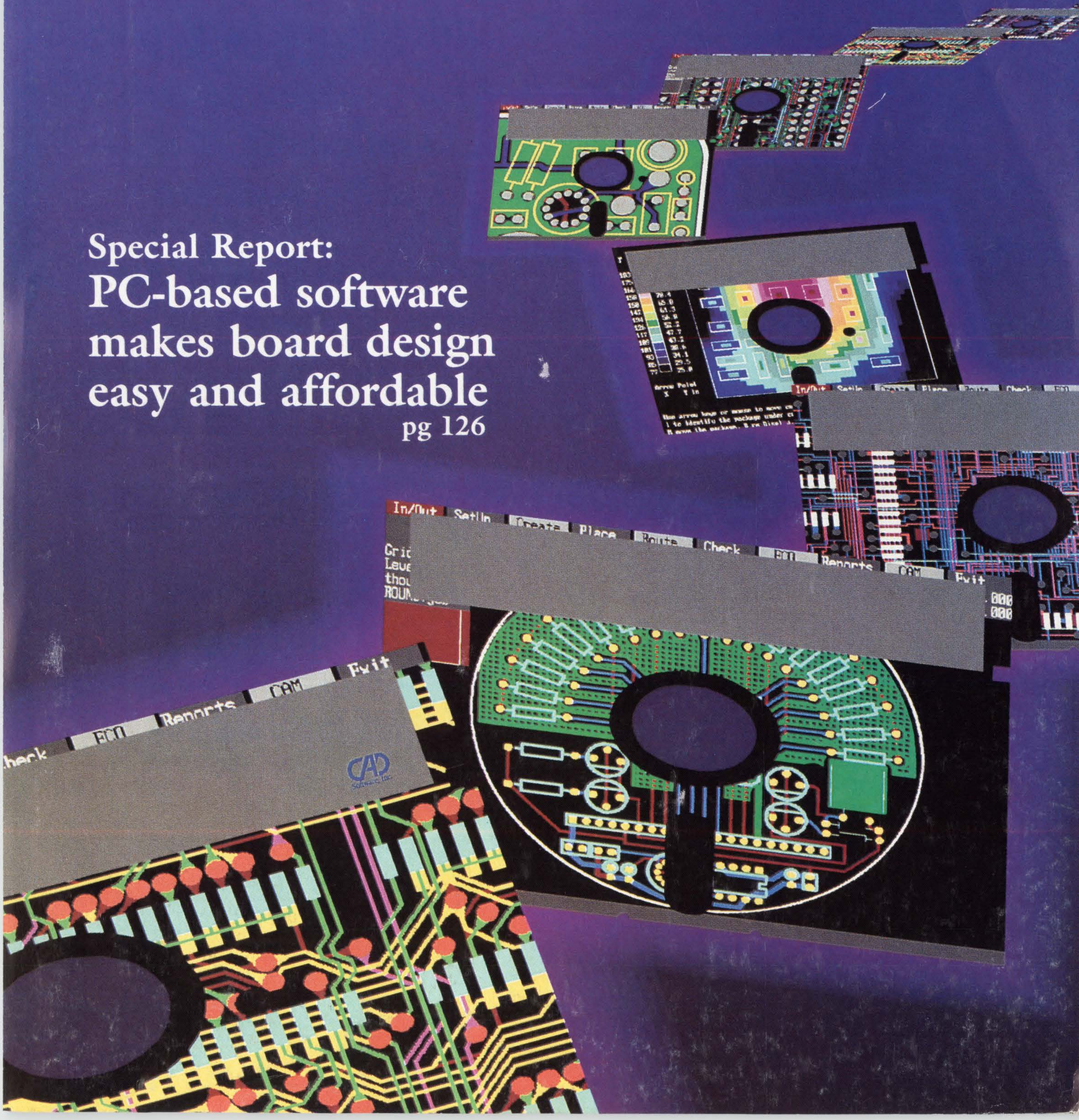
A CAHNERS PUBLICATION
JUNE 6, 1991

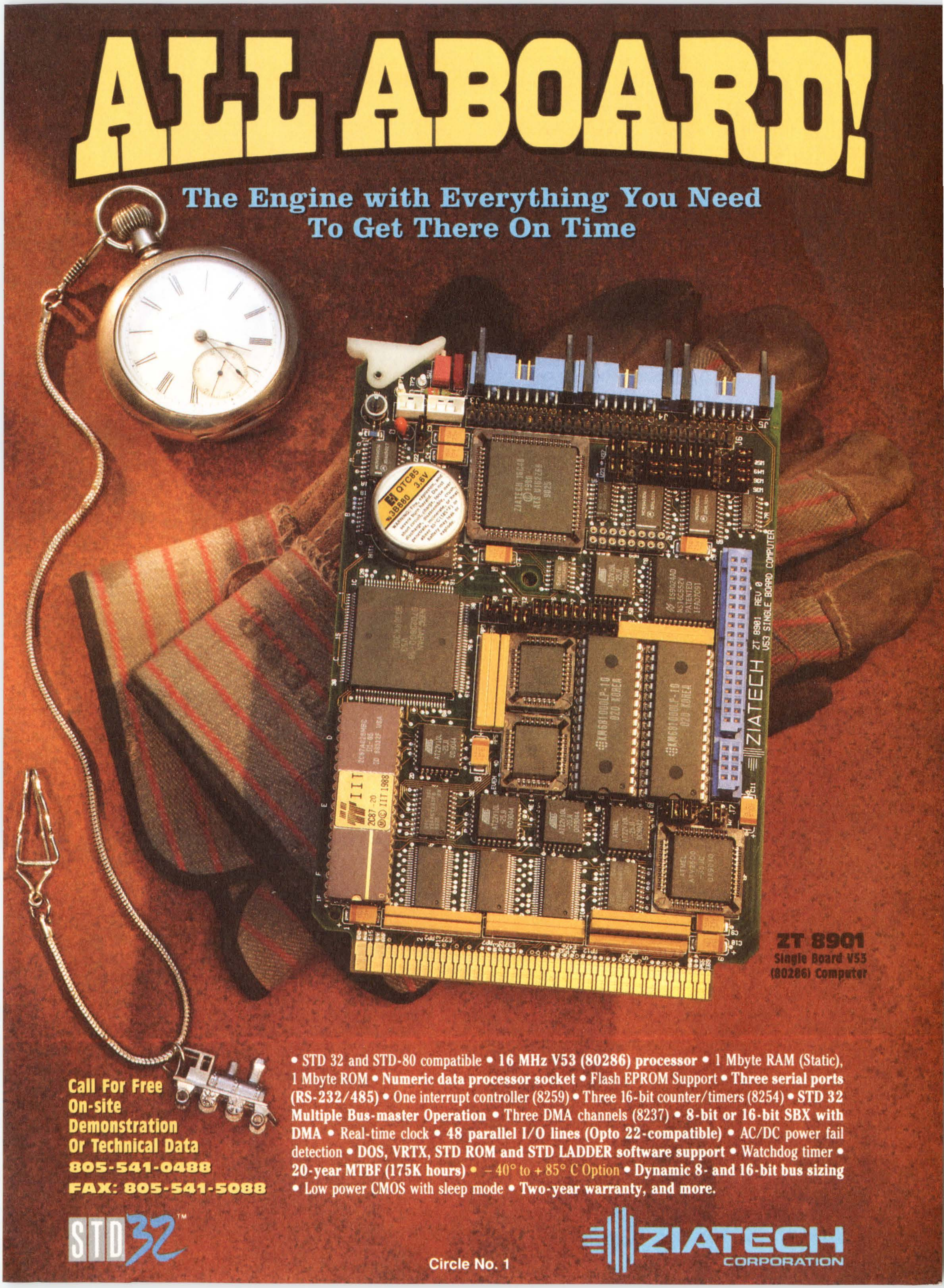
EDN®

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Special Report: PC-based software makes board design easy and affordable

pg 126

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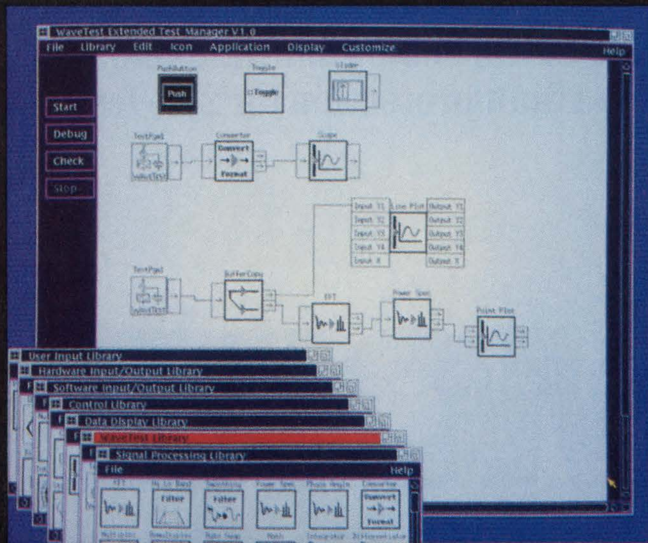
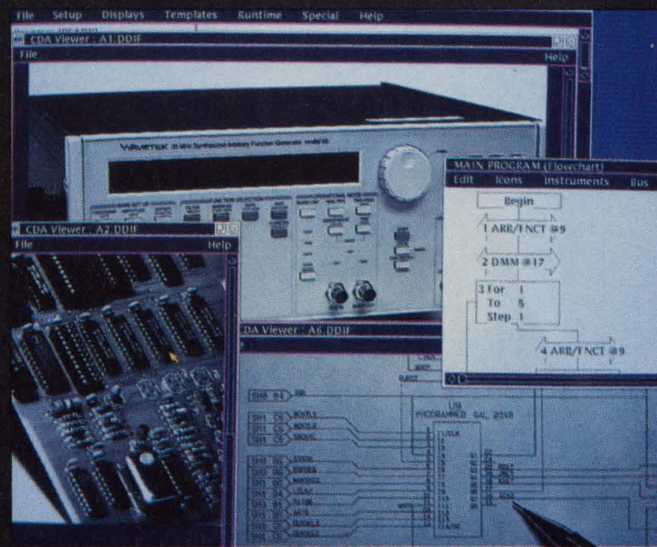


Just select and move icons to build a complete ATE test and data management program.



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WaveTest XTM (Extended Test Manager) is the software solution test designers have dreamed about, when they had time to sleep. It combines the fun and efficiency of iconic test generation with the power of VMS and ULTRIX workstation environments. You can collect, analyze and distribute test data with the flick of a mouse.

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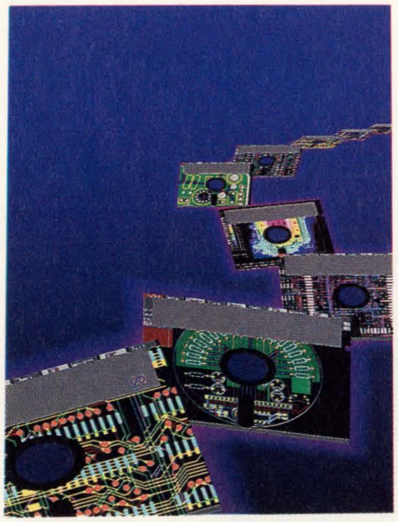
EDN Magazine Edition ®

Volume 36, Number 12

June 6, 1991

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *For less than $5000, engineers who design their own boards or occasionally design prototype boards can buy pc-board design packages that have a surprising number of capabilities. See our Special Report on pg 126. (Photo courtesy CAD Software)*

SPECIAL REPORT

DESIGN FEATURES

Continued on page 7

EDN® (ISSN 0012-7515, GST Reg. #123397457) is published 48 times a year (biweekly with 2 additional issues a month, except for February, which has 3 additional issues and July and December which have 1 additional issue) by Cahners Publishing Company, A Division of Reed Publishing USA, 275 Washington Street, Newton, MA 02158-1630. Terrence M McDermott, President; Frank Sibley, Executive Vice President; Jerry D Neth, Senior Vice President/Publishing Operations; J J Walsh, Senior Vice President/Finance; Thomas J Dellamaria, Senior Vice President/Production and Manufacturing; Ralph Knupp, Vice President/Human Resources. EDN® is a registered trademark of Reed Properties Inc., used under license. Circulation records are maintained at Cahners Publishing Company, 44 Cook Street, Denver, CO 80206-5800. Telephone: (303) 388-4511. Second-class postage paid at Denver, CO 80206-5800 and additional mailing offices. **POSTMASTER: Send address corrections to EDN®, PO Box 173377, Denver, CO 80217-3377.** EDN® copyright 1991 by Reed Publishing USA; Ronald G Segel, Chairman and Chief Executive Officer; Robert L Krakoff, President and Chief Operating Officer; William M Platt, Senior Vice President. Annual subscription rates for nonqualified people: USA, $119.95/year; Mexico, $169.95/year; Canada, $181.85/year; all other nations, $209.95/year for surface mail and $329.95/year for air mail. Single copies are available for $15. Please address all subscription mail to Ellen Porter, 44 Cook Street, Denver, CO 80206-5800.

Continued from page 5

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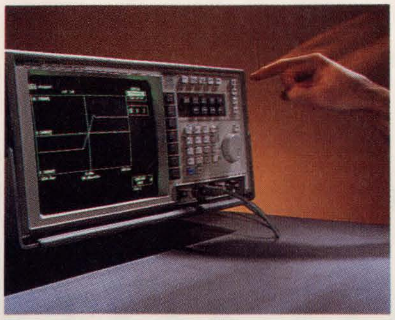
June 6, 1991



***Frequency and time-interval analyzers** make and store long series of measurements with little or no dead time between readings. The units help spot problems you can't find with coventional counters by letting you visualize the measurements (pg 79).*

TECHNOLOGY UPDATES

INNOVATION™ Driving Electronic Technology Into The Next Century

PRODUCT UPDATES

Continued on page 9

EDN magazine now offers Express Request, a convenient way to retrieve product information by phone. See the Reader Service Card in the front for details on how to use this free service.

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New 512K CMOS PROMs optimize performance.

As embedded control microprocessors shift into high gear, you need memory solutions that won't jam up system performance.

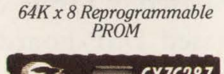
With access times as low as 20 ns, our 512K PROMs with fast column access let your microprocessor read right from PROM. For applications from communications and networking to peripherals and avionics, these high-performance, high-density, low-power, CMOS PROMs move embedded control performance into the fast lane.

Choose the CY7C285 or CY7C289 for a 64-byte page and WAIT signal that eliminates invalid data. Address latches in the CY7C289 give you the speed you need to support high-speed RISC or CISC microprocessors. Pick the CY7C286 for the highest overall performance available at 50 ns. The CY7C287 offers registered outputs and synchronous operation.

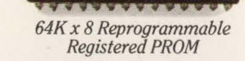
You get higher performance than bipolar PROMs, but the power savings of CMOS.

64K x 8 Reprogrammable Fast Column Access PROM, 20 ns

64K x 8 Reprogrammable PROM



64K x 8 Reprogrammable Registered PROM



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Continued from page 7

EDN Magazine Edition®

June 6, 1991

DESIGN IDEAS

EDITORIAL

Don't expect much from the Advanced Computing Environment alliance. Such groups do little to further competition or innovation.

NEW PRODUCTS

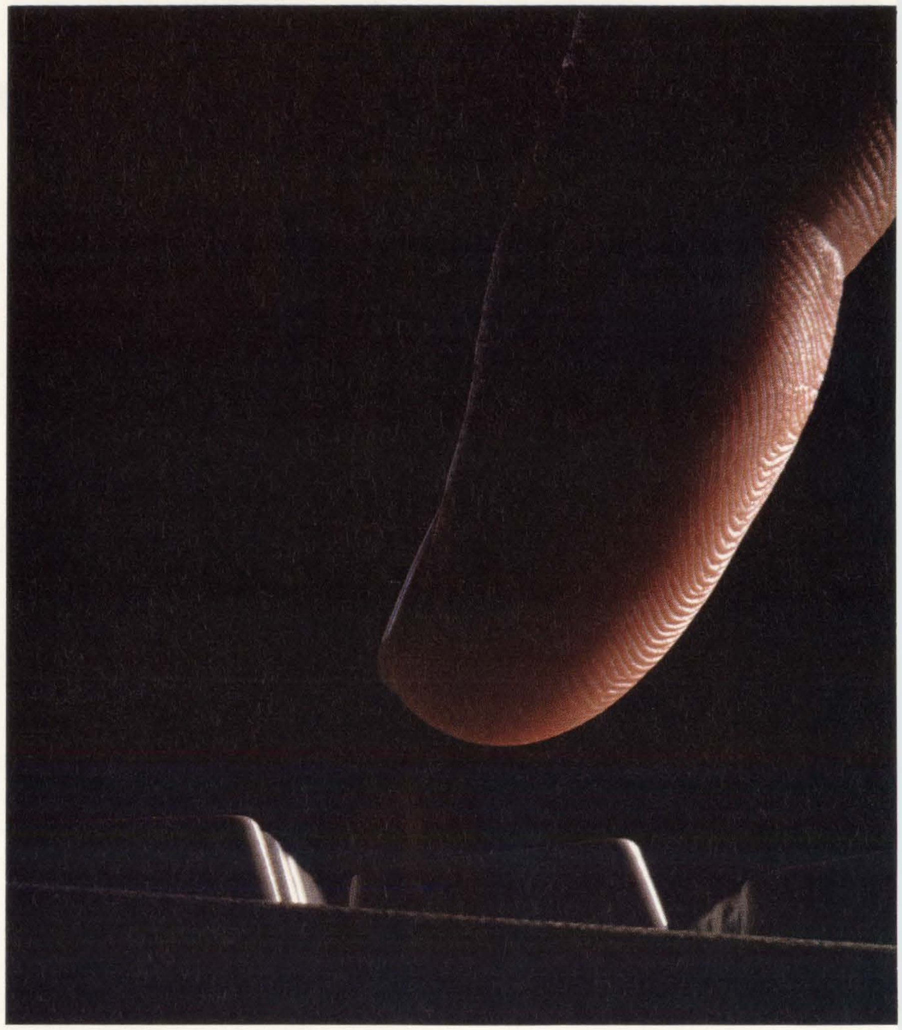
PROFESSIONAL ISSUES

Engineering graduate schools face a difficult decade

Enrollments are declining, and a serious faculty shortage may lie ahead.—*Jay Fraser, Associate Editor*

DEPARTMENTS

IN THE TIME IT TAKES
COULD ROUTE THE WO



Our new push-button software makes programming other logic devices seem positively tedious.

Believe it or not, it only takes about 150 seconds to place and route a Xilinx FPGA.

Chances are: it'll take you longer to read this ad.

THE FIRST AND STILL THE FASTEST.

At Xilinx we invented the FPGA. And we've led the industry ever since.

With the fastest, highest performance FPGAs available anywhere.

Today, we offer system clock speeds of 60 MHz.

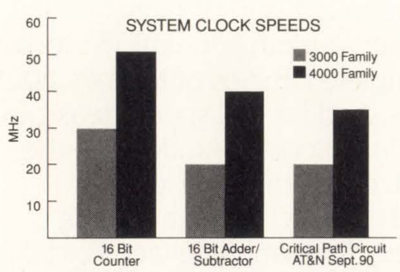
We're also the first programmable logic company to offer you on-board RAM.

Making our newest FPGAs ideal for everything from FIFOs to register stacks.

What's more, we're the only programmable logic company that provides you with on-chip wide decode.

And that's just the beginning.

Because as formidable as our hardware may seem, it's only half the story.



As measured by typical design benchmarks, the XC3000 family is the industry's fastest FPGA. Or at least it was until we introduced the 4000 family.

NEW ENHANCED SOFTWARE PROVIDES PUSH BUTTON SOLUTION.

Device speed alone doesn't determine the fastest, highest-performance logic device.

When you're designing, the clock on the wall is every bit as important as the clock speed of the chip.

So to make Xilinx FPGAs even faster and easier to program, we've redesigned our software.

This is no mere upgrade. It's a major rewrite.

Our new version of XACT now comes with 200 soft macros. And fifty hard macros.

Providing automatic placing and routing for virtually all designs.

With greater than 90% gate utilization.

If you've worked with Xilinx FPGAs before, you'll see improvements even before you start to place and route your design.

If you've never worked with Xilinx FPGAs before, you'll find every other logic device to be positively tedious by comparison.

WHEN IT COMES TO SYSTEM TESTING, WE PASS WITH FLYING COLORS.

Our newest FPGAs offer you yet another competitive advantage that's exclusive to Xilinx.

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RLD'S FASTEST FPGA.

The industry's first on-chip JTAG boundary scan for easy testing of PC boards and device I/Os.

This unique Xilinx offering improves overall system testability and dramatically reduces board test costs. It's a major boost for those designing high-density, surface mount systems or complex, multi-layer PC boards.

We told you we'd save you time and money.

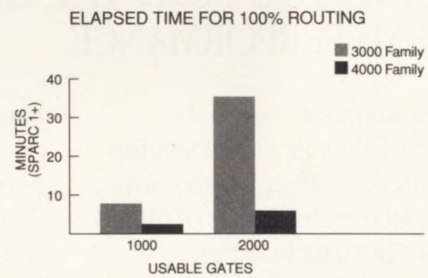
IF AT FIRST YOU DON'T SUCCEED, IT'S EASY TO TRY AGAIN.

As you well know, when you're designing a system, changes keep coming fast and furious.

Which is why Xilinx FPGAs are designed to be reprogrammed quickly an unlimited number of times.

And not only do our FPGAs save you an enormous amount of time early on, they also save you time later when you need to make those "last minute" enhancements.

It's one more way we make it easier for you to get your product to market as fast as possible. First time. Every time.



New algorithms have reduced place and route times by a factor of four.

GETTING AN EDGE OVER YOUR COMPETITORS IS JUST A PHONE CALL AWAY.

If you've read this far, you could have already placed and routed one of our FPGAs.

So don't delay. No other programmable logic company can offer you the many exclusive features of Xilinx FPGAs.

Call 1-800-255-7778. Or in California, 408-559-7778. And we'll send you more information on how our FPGAs can give you the competitive edge.

But you'd better hurry.

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HOW NATIONAL SEMICONDUCTOR IS HELPING YOU PUSH THE LIMITS OF ADVANCED SYSTEMS PERFORMANCE.

Tom Redfern, National's Director of New Product Development, Interface/Peripherals Group, talks about the challenges of mixed analog+digital technology.

Making Futurebus+ a reality.

"Traditional bus protocols are starting to hit the wall. They can't accommodate the wide data paths and high transfer rates demanded of the next generation of 32- and 64-bit microprocessors.

"That's why we've been an active participant on the IEEE's Futurebus+ committee since its founding in 1979. And that's why we invented the Backplane Transceiver Logic (BTL) that makes Futurebus+ a reality today.

"Our first Futurebus+ chipset contains five devices, and they employ some of the most advanced analog+digital integration ever achieved. Our BTL drivers, for example, let the digital CPU send information to the digital memory over the analog bus at peak rates of 2-3 Gbytes/second!

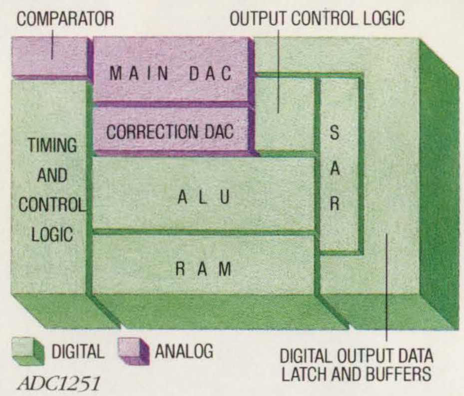
"This is the future— and we've got it today."

Setting the pace in system-level integration.

"Another great example is CLASIC, our powerful Custom Linear ASIC family.

"To reach system-on-chip performance, you've got to integrate analog and digital functions onto the same substrate.

"Well, CLASIC does that.



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"It's that simple."

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ADC1251 A/D Converter

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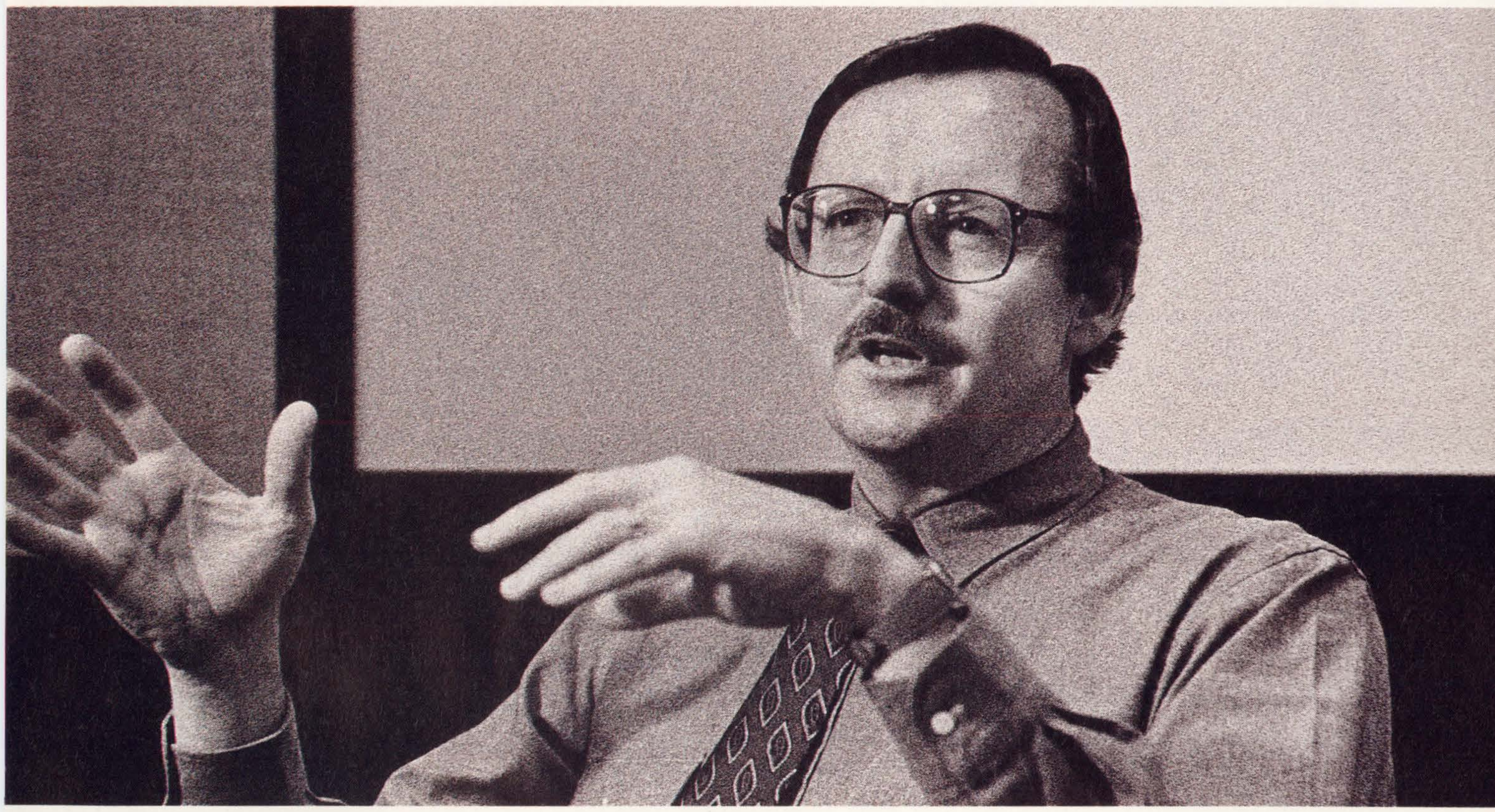

time and a ±1/2 LSB non-linearity accuracy while dissipating 113mW max at ±5V.

"Try to find that in any other ADC. You can't."

Pushing the limits of analog + digital integration.

"To achieve these levels of integration, you need powerful tools in the hands of experienced designers.

"We've got them. A full range of process technologies, including fourth-generation bipolar ECL and BiCMOS, which give us 0.8μ lithographies with bipolar F_{Ts} of 15GHz and 50ps gate delays.

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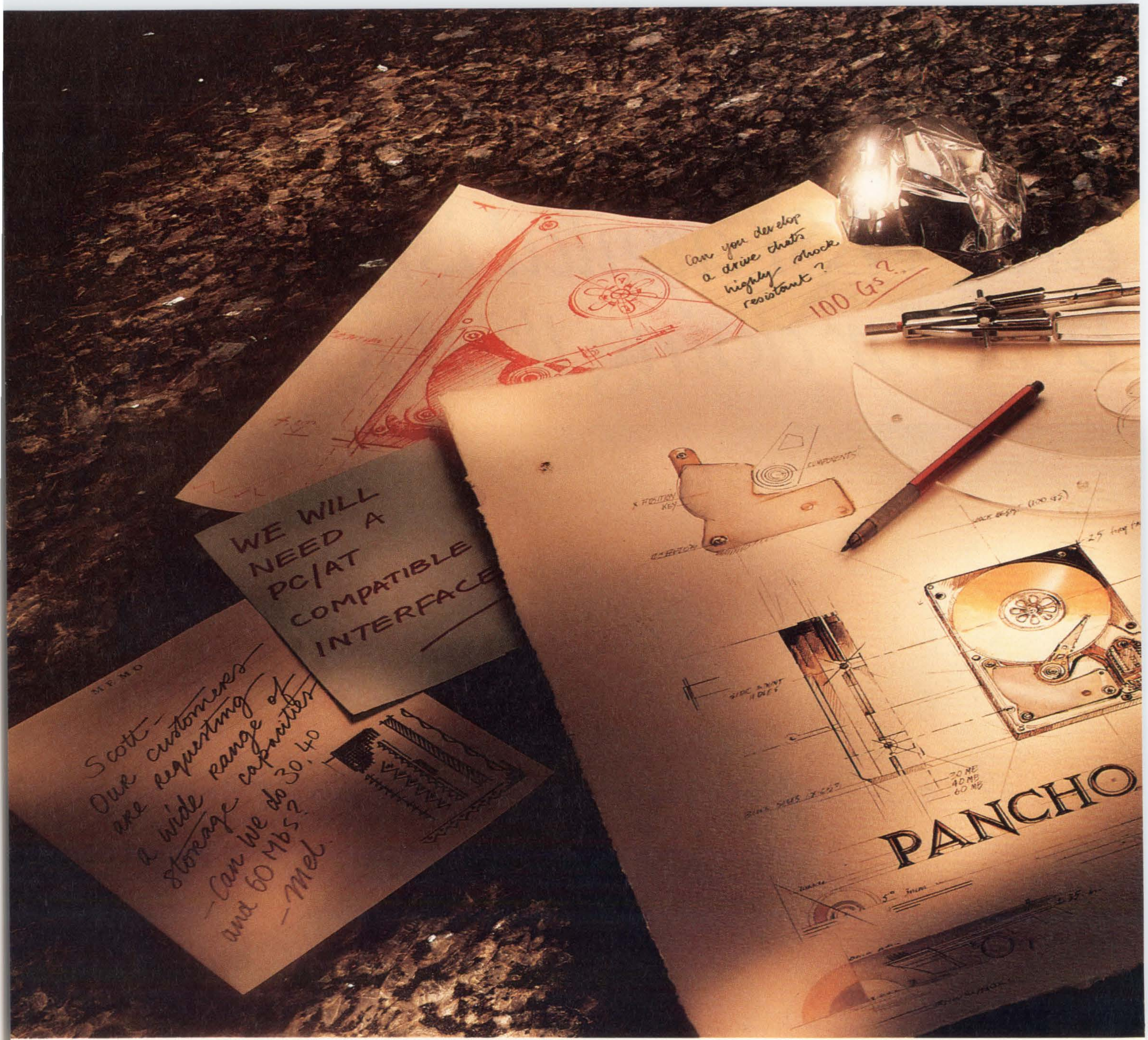

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EDITED BY SUSAN ROSE

16-BIT S/H AMPLIFIER ACQUIRES IN 500 nSEC

The SHM-945 from Datel Inc features a 500-nsec-max acquisition time to ±0.00076% (±1/2 LSB at 16 bits) for a 10V full-scale step, and it features a maximum acquisition time of 350 nsec to ±0.003% (±1/2 LSB at 14 bits) for a 10V step. A differential input section allows rejection of common-mode noise that arises from grounding and layout issues, which often prevent the final design from attaining 16-bit performance. The manufacturer laser trims the offset, pedestal, and gain errors, and no external adjustments are required. A range pin allows you to select gains of −0.5, −1, and −2. Other specifications include feedthrough rejection of typically 100 dB, typical hold-mode noise of 60 μV rms, typical aperture uncertainty of 10 psec, and a typical small-signal bandwidth of 16 MHz. The device requires ±15 and 5V supplies, and dissipates 385 mW max. 24-pin DIP, 0 to 70°C and −55 to +125°C devices are available for $79 and $87 (OEM qty), respectively. Datel Inc, Mansfield, MA, (508) 339-3000, FAX (508) 339-6356.—Anne Watson Swager

GIVE YOUR MAC A MATH COPROCESSOR

For $249 you can plug the Apex 16-MHz math coprocessor board from Second Wave Inc into your Apple Macintosh LC computer's processor-direct slot. The coprocessor accelerates math-intensive tasks such as CAD, graphics, and spreadsheets by five to ten times. Second Wave Inc, Austin, TX, (512) 343-9661, FAX (512) 343-9663. —JD Mosley

CALLING FOR DSP-CONFERENCE PAPERS

DSP Associates has issued a call for papers for its International Digital Signal Processing Applications and Technology Conference and Exhibition. The Conference, which will take place October 28 to 31 in Berlin, Germany, is focused entirely on the development needs and application challenges facing international DSP-product designers. Authors should concentrate on recent DSP-based developments and new products in telecommunications, speech processing, image processing/recognition, control systems, automotive engineering, VLSI and DSP architectures, geophysics, underwater and radar detection, consumer electronics, and other applications. Send (via mail or fax) 100-word abstracts to the company by June 30. Contact the company for more information about display booth space reservations, costs, and other details. DSP Associates, Newton Centre, MA, (617) 964-3817, FAX (617) 969-6689, contact Jim Buhrendorf; Antwerp, Belgium, 32 (3) 237-1677, FAX 32 (3) 248-1694, contact Lina Van Meerbeeck.—Susan Rose

PUBLICATION OPENS PC'S KEYBOARD PORT FOR EXPLOITATION

The keyboard port on IBM PC and compatible computers can provide a handy interface port if you know how to use it. "PC Keyboard Design," a $249 book-and-disk publication, provides detailed information on both the IBM PC/XT and PC/AT keyboard ports with suggestions for possible peripheral devices you might design to use these ports. The accompanying disk includes source code for managing the PC's keyboard controller. Annabooks, San Diego, CA, (619) 271-9526, FAX (619) 592-0061.—Steven H Leibson

MATH COPROCESSORS HIT HIGH AND LOW LIMITS

The $1075 Fasmath 83D87-40 math coprocessor from Cyrix Corp has an operational clock rate of 40 MHz and 5.5M-flops peak performance. For 80286-based computers, you can buy a $238 25-MHz coprocessor, the 82S87-25, that has power-management functions for battery-powered applications. When idle, the 25-MHz coprocessor consumes less than 100 μW of power. By stopping the clock and control input signals you can reduce the power consumption to less than 100 μW. Cyrix Corp, Richardson, TX, (214) 234-8387, FAX (214) 234-8397.—JD Mosley

MACINTOSH OS TIGHTENS APPLICATIONS TIES

Apple Computer Inc is now shipping its System 7 operating system (OS) for the Macintosh personal computer family. The OS supports multitasking as standard procedure, allows the use of virtual memory, and supports 32-bit addressing. The OS also features several tools that simplify interaction between applications packages, including the ability to "publish" data created with one program and "subscribe" to that data with other programs. Published data maintains a link to its source, ensuring that subscribers automatically receive updates when the data changes.

By the end of summer, all new Macintosh computers will come with the new OS factory-installed on the hard disk. Current Macintosh owners on maintenance programs will receive free upgrades. Other users can purchase a personal upgrade kit for $99 or a network upgrade kit, allowing you to update all network nodes simultaneously, for $349. The upgrade kits include the OS, tutorials, manuals, technical support, and a preinstallation tool that checks your programs and data for compatibility with the OS. If the tool finds problems, it provides a telephone number you can call for technical help. Apple Computer Inc, Cupertino, CA, (408) 996-1010.
—Richard A Quinnell

ANIMATE CAD DRAWINGS FOR LIVELY DEMONSTRATIONS

Autodesk's $795 Animator Pro offers a simple way to animate designs. The software can produce and display animations at resolutions as great as 1024×768 pixels. It can also read AutoCAD .DXF files and process a 2-D image using any of five different animation techniques. Your audience doesn't need a copy of the software to play the resulting animation; all they need is an 80386-based computer that runs DOS. Autodesk Inc, Sausalito, CA, (415) 332-2344, FAX (415) 331-8093.—J D Mosley

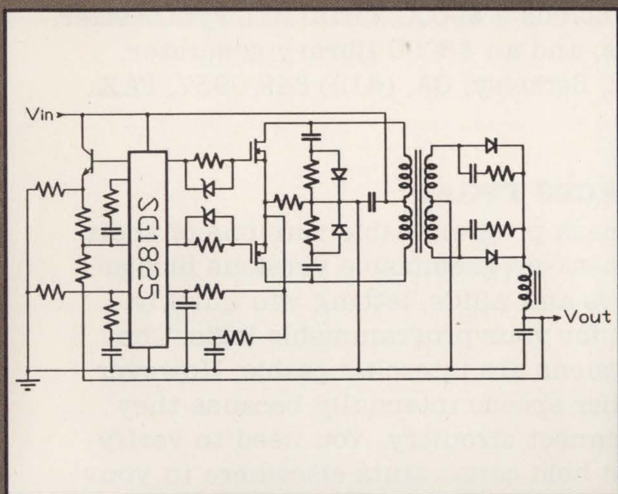
OPTIMIZE FPGA DESIGNS IN NATIVE ARCHITECTURE

Exemplar's Release 1.0 software tools combine synthesis, speed and area optimization, and mapping of field-programmable gate arrays (FPGAs) in one package. Most software packages that synthesize and optimize FPGAs don't work at the architectural level, which slows the design process. The software reads inputs from ABEL, CUPL, Palasm 2 equations, PLA truth tables, and EDIF 2.0.0 netlists. You can also use VHDL (VHSIC hardware description language) RTL (register transfer level) synthesis to create designs. The software outputs a design mapped in the FPGA building blocks, requiring you to use the chip vendor's tools for place and route. Libraries are available for Xilinx and Actel FPGA families, LSI Logic LCA10000, NEC CMOS5,

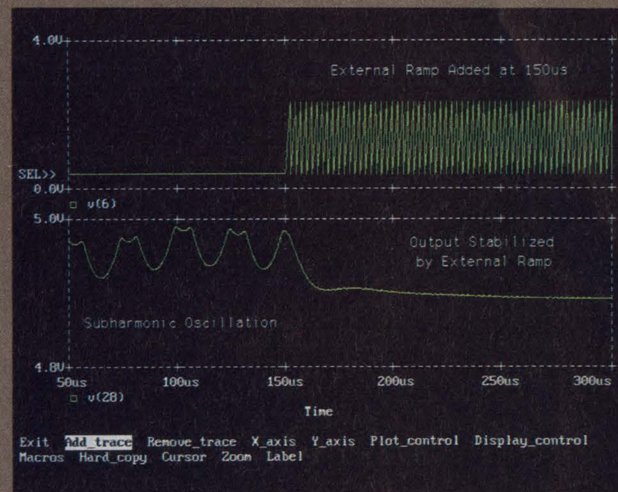
PSpice

MicroSim Corporation

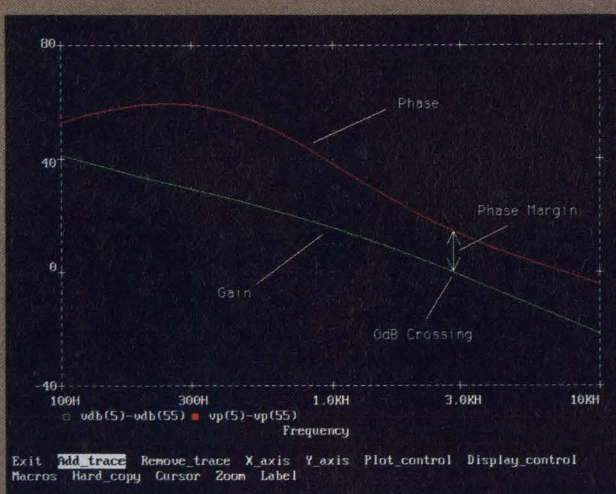
The Standard for Circuit Simulation Switch-Mode Power Supply Design



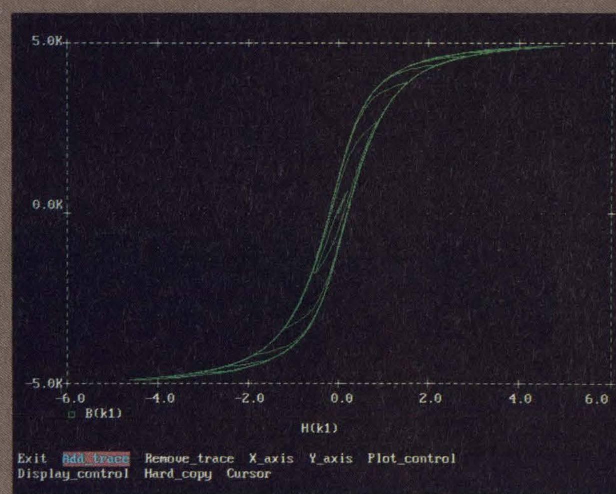
Current mode power supply schematic.



Power supply simulated using mixed analog/digital simulation. Plot shows subharmonic oscillation being suppressed by external ramp.



Simulation using the Vorperian switch model to examine the stability of a power supply.



Hysteresis curve of transformer.

A cycle by cycle simulation of switch-mode power supplies is recognized as a difficult simulation task for SPICE-based simulators, which must cope with timings that can span 4 orders of magnitude. This problem invariably results in very long simulation times, but is improved considerably by MicroSim's approach of building the controller macromodel chips so that a significant section is simulated in the digital domain. PSpice's behavioral modeling and mixed analog/digital simulation capability makes this possible.

PSpice is available on the IBM-PC (running DOS or OS/2); Macintosh II; Sun 3, Sun 4, and SPARCstation; DECstation 2100, 3100, and 5000; and the VAX/VMS families. In addition to the PWM macromodels, the PSpice library contains over 3,500 analog and 1,500 digital parts which can be used in a variety of applications. Our technical staff has over 150 years of combined experience in CAD/CAE, and our software is supported by the engineers who wrote it.

For further information about the PSpice family of products, call us at (714) 770-3022, or toll free at (800) 245-3022. Find out for yourself why PSpice has become the standard for circuit simulation.

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Toshiba 120g, and VLSI VGT200 gate arrays. The price for the architectural analyzer, one vendor-specific library, and an X-Window graphical user interface is $10,000 per seat for Unix and $6000 for DOS. Options include a $9000 VHDL RTL synthesizer, an $8000 schematic generator for EDIF netlists, and an $8000 library generator. Additional libraries are $5000. Exemplar Logic, Berkeley, CA, (415) 849-0937, FAX (415) 849-9935.—Doug Conner

LOW-COST MASK PROGRAMMING REPLACES FPGAs

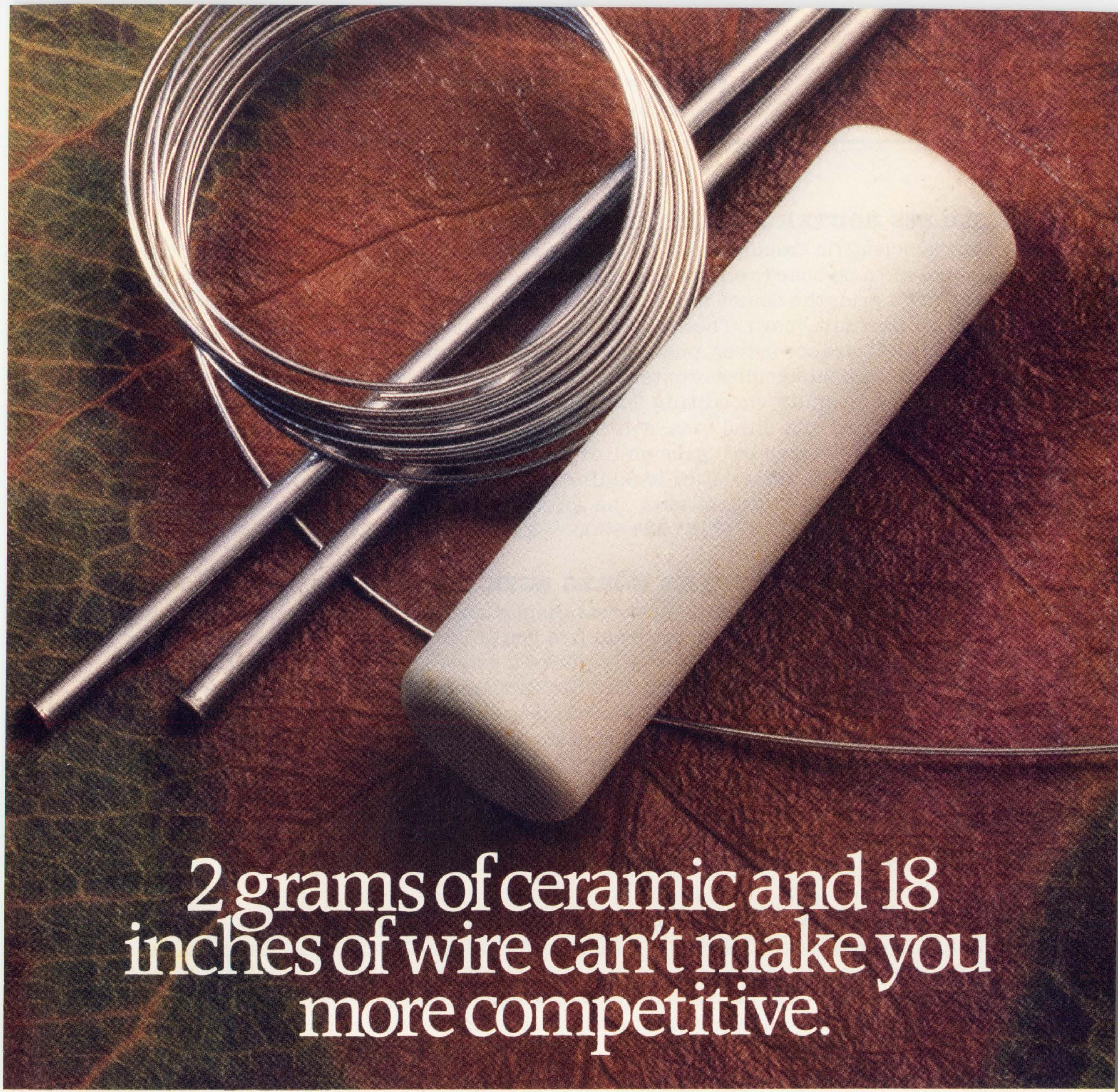
Both Xilinx Inc and Altera Corp now have mask-programmable versions of their field-programmable gate arrays (FPGAs). The mask-programmable versions bridge the price gap between programmable gate arrays and ASICs, letting you quickly create a lower-cost pin-compatible replacement for your programmable logic. The field-programmable and mask-programmed versions are interchangeable. However, the mask-programmed versions operate at higher speeds internally because they use metal to replace the programmable interconnect circuitry. You need to verify that the higher speed doesn't violate setup and hold constraints elsewhere in your design.

The Xilinx devices replace members of the XC3000 FPGA family. The $9 XC3330, $13 XC3342, and $25 (10,000) XC3390 cost 50 to 70% less than the programmable versions. The 100-MHz devices are pin and function compatible with the programmable devices, including emulation of the configuration logic associated with device programming. You can disable the emulation and skip the delay associated with initializing the programmable devices. The NRE charges range from $5000 to $9000, including test program generation, with prototypes available in three weeks.

The Altera devices replace the Max 5000 and EP1810 families. The NRE charge is $15,000, and prototypes can be ready in five weeks. Unit costs vary with package and design sizes. The typical price for an EPM5128 in a 68-lead plastic leaded chip carrier is $10 (5000). Xilinx Inc, San Jose, CA, (408) 559-7778, FAX (408) 559-7114. Altera Corp, San Jose, CA, (408) 984-2800.—Richard A Quinnell

FLASH MEMORY EMBEDS PROGRAM AND ERASE COMMANDS

The Am28F020 2M-bit flash memory from Advanced Micro Devices contains embedded code that automatically erases and programs the memory device. The embedded algorithms save you from writing and debugging the programming routines themselves. When you send the erase command to the chip, the device automatically preprograms, erases, and verifies the entire memory for an all-zero data pattern. The embedded erase algorithm terminates when the chip reaches an adequate erase margin, thereby preventing overerasure. The device doesn't require any controls or timing during these operations. The device indicates to the system when it's ready for reprogramming, during which the chip indicates its readiness for new data on a byte-by-byte basis. The devices comes in four speed grades, with access times of 90, 120, 150, and 200 nsec. Organized as 256k × 8 bits, the IC is available in a 32-pin PLCC (plastic leaded chip carrier) and a 32-pin plastic or ceramic DIP. The 200-nsec version in the PLCC package costs $44 (100). Advanced Micro Devices, Sunnyvale, CA, (800) 222-9323, (408) 740-5703, FAX (408) 749-3240.—Anne Watson Swager



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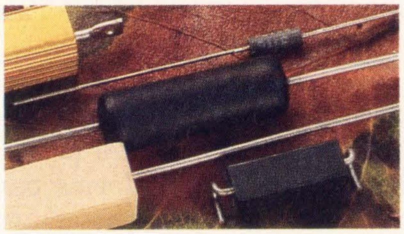

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CIRCLE NO. 193

NEWS BREAKS

GRIDLESS ROUTER REALLY ELIMINATES GRID

Harris Scientific Calculations' Freestyle pc-board router is a true gridless router (as opposed to pc-board routers that reduce the size of the grid to seem gridless). Instead of a grid, the device is a shape-based router that starts with routing obstacles placed on a circuit board. These obstacles include the board edges and component pads. Using clearance-driven push-and-shove and ripup-and-retry algorithms, the company claims this gridless router has yet to meet a board it couldn't route to completion. Among its via editing features, the router allows stacked, staggered, and spiral buried and blind vias, coincident via rules and via tap-in under surface-mount pads. The router performs on-line design-rule checks based on rules that you can set by many characteristics including layer, class, net, and boundaries. Running on both Sun and DEC workstations, the software costs $29,950. Harris Scientific Calculations, Fishers, NY, (716) 924-9303.—Michael C Markowitz

DATA-ANALYSIS SOFTWARE WORKS WITH IEEE-488 DIGITIZER

IOtech's $1695 Turbolab graphical data display and analysis program calculates a 4096-point FFT in 1.5 sec. The program lets you collect data from as many as 16 analog channels and send it directly to your PC's memory or disk. The software performs IIR-filter and FFT calculations for as many as 16,384 points and transparently uses your PC's hard disk as a virtual memory when an operation requires additional RAM. In this way you can acquire, display, and manipulate waveforms of virtually any length. For seamless data acquisition, you can interface the software directly to the manufacturer's $1795 ADC488 100-kHz, 16-bit IEEE-488 digitizer. The program comes with a module that automatically determines the memory and channel configuration of the ADC488 during startup. IOtech Inc, Cleveland, OH, (216) 439-4091, FAX (216) 439-4093.—J D Mosley

HANDHELD DMMs MEASURE CAPACITANCE AND FREQUENCY

John Fluke Mfg Co's 70 Series II handheld digital multimeters (DMMs) consists of eight models at list prices ranging from $69 to $185. The flagship models 79 and 29 make all of the basic measurements with 4000-count resolution and 0.3% accuracy for dc volts. They also measure frequency to 20 kHz and capacitance to 9999 μF. John Fluke Mfg Co Inc, Everett, WA, (206) 347-6100.—Dan Strassberg

IC VERIFICATION SOFTWARE DISTRIBUTES TASK

Silvar-Lisco's suite of IC-design tools, called SL-Verify, operate faster by distributing electrical- and design-rule checks and mask-data preparation across your entire network of available workstations. The software performs layout vs layout, schematic vs schematic, and layout vs schematic consistency checks. To facilitate making runset changes, the software lets you specify rules with variable limits. (The runset is the command file that defines what checks are to be performed and what rules each check shall use.) The $100,000 suite includes four tools: a block-based design-rule checker, an electrical-rule checker that performs parameter extraction, a mask-data preparation tool that includes E-beam and pattern-generation fracturing algorithms, and a manufacturing yield-analysis tool. A rule-set translator lets you use existing Dracula runsets. Silvar-Lisco, Sunnyvale, CA, (408) 991-6000, FAX (408) 737-9979.—Michael C Markowitz

FILTERS

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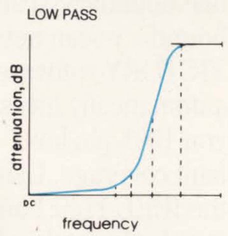
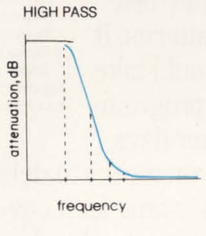


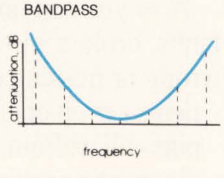
low pass dc to 1200MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	STOP BAND, MHz (loss>40dB) Max.	Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45



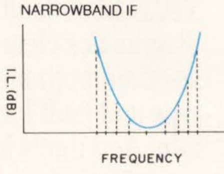
high pass dc to 2500MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Min.	STOP BAND, MHz (loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95



bandpass 20 to 70MHz

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB) Max. F1	Min. F2	STOP BAND, MHz (loss > 10 dB) Min. F3	Max. F4	STOP BAND, MHz (loss > 20 dB) Min. F5	Max. F6	VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95



narrowband IF

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	F6	STOP BAND, MHz I.L. > 35dB F7	F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

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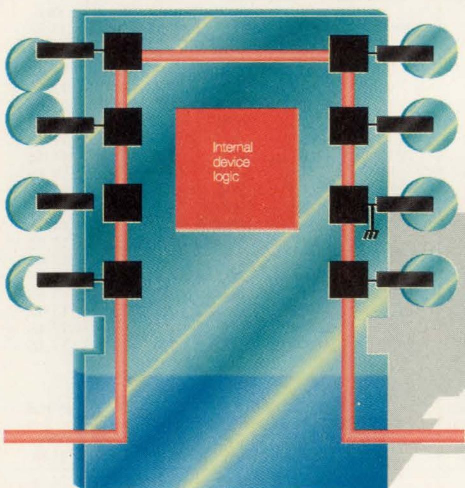
People say boundary in low cost, high quality Now you can test that



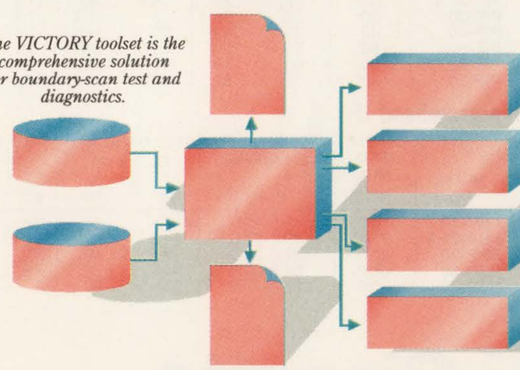
Find common manufacturing faults without test patterns libraries or physical test access with boundary-scan design and VICTORY software.

Increasing device complexity. Rising pattern development costs. High density packaging. Disappearing nodal access. These are the board test problems boundary scan was created to solve. Which is fine in theory. Only problem is there hasn't been any way to put boundary scan to the test. Until now.

VICTORY – the first software to automate boundary-scan testing.

Introducing VICTORY™ from Teradyne: the only software toolset ready to help you turn boundary-scan theory into a practical advantage. From the moment your first boundary-scan device is designed in, VICTORY starts to simplify the testing of complex digital boards. And the more boundary-scan parts you have, the more time and money you save.

The VICTORY toolset is the comprehensive solution for boundary-scan test and diagnostics.

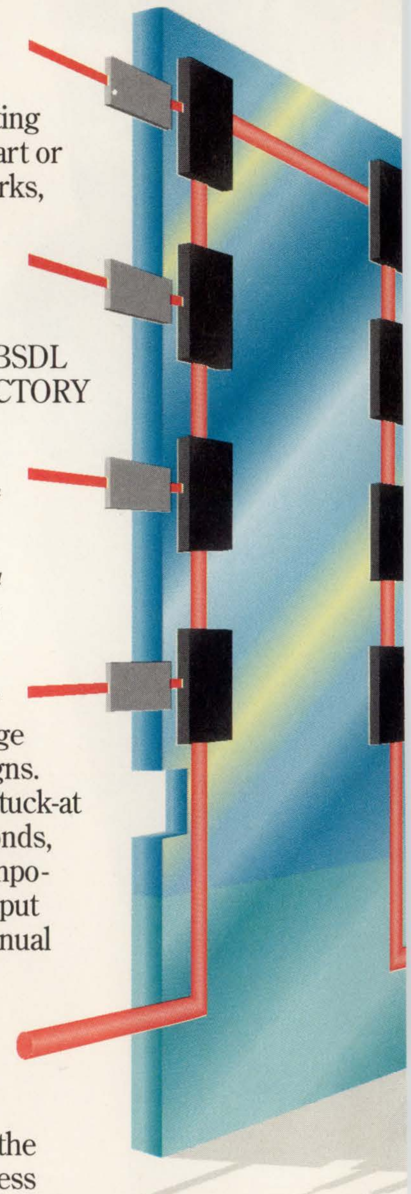


Delivers high fault-coverage.

Whether you're testing one boundary-scan part or boundary-scan networks, VICTORY software automatically gives you 100% pin-level fault coverage. Using the IEEE 1149.1 and BSDL standards, it takes VICTORY only a minute or two to generate test patterns. It would take a programmer days, even weeks to deliver the same fault coverage for conventional designs.

Concurrent engineering takes on new meaning when you use VICTORY's Access Analyzer to optimize board layout for testability and cost-efficiency.

Now you can find stuck-at faults, broken wire bonds, wrong or missing components – even open input pins – all without manual diagnostic probing. VICTORY's fault diagnostics clearly spell out both fault type and fault location. And that's just the manufacturing process

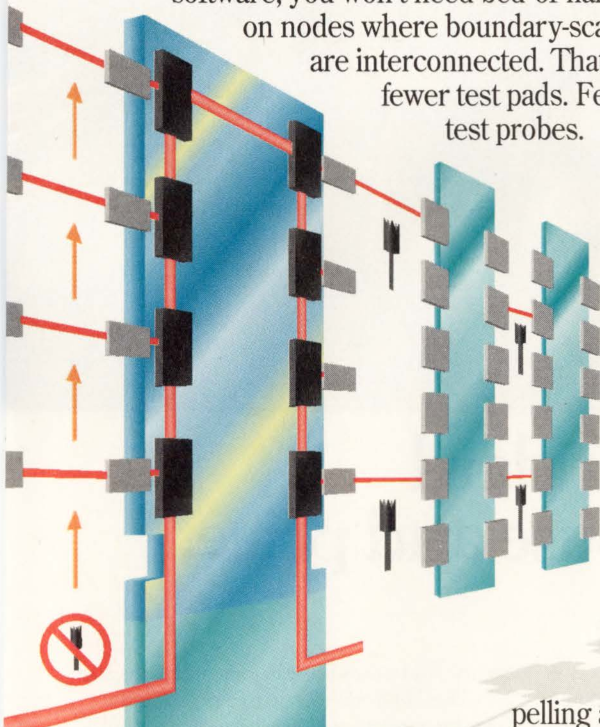


scan is a breakthrough board testing. theory.

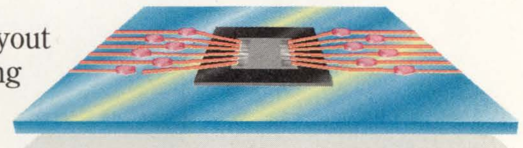
feedback you need to eliminate defects where it's most cost-effective–at the source.

Helps solve the test access problem.

With boundary-scan design and VICTORY software, you won't need bed-of-nails access on nodes where boundary-scan parts are interconnected. That means fewer test pads. Fewer test probes.



That's a compelling advantage to board designers. Which is why VICTORY's Access Analyzer was developed. With this concurrent engineering tool, designers get testability information early in the design process. They can easily see where test points are required for visibility and where they can be dropped, for optimized board layout without lowering fault coverage.



Boundary-Scan Intelligent Diagnostics identify faults by type and location without physical probing – even on high-density SMT assemblies

Good for the bottom line.

Shorter test programming time. Higher fault coverage. Lower PC board and test fixture costs. The bottom line on VICTORY is how positively it will affect your bottom line. And because VICTORY works with all Teradyne board testers, you're free to tailor a test process that's cost-effective for both your boundary-scan and non-scan boards. No matter what your test objectives. For example, with our new Z1800VP-series testers, a complete solution for in-circuit and boundary-scan testing starts at well under $100,000.

Get high fault coverage at low cost when you test boundary-scan boards with our new Z1800VP system and VICTORY software.

Make the next logical move. Call today.

Boundary scan is the design-for-test breakthrough that promises lower cost, higher quality board testing. But don't take our word for it. Call Daryl Layzer at (800) 225-2699, ext. 3808. We'll show you how, with VICTORY software and Teradyne board testers, you can test this theory for yourself.

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SIGNALS & NOISE

Precision op amp guarantees spec

In the Technology Update, "Precision parts demand kid-glove treatment" (EDN, February 18, 1991, pg 99), Bob Dobkin of Linear Technology Corp doubts that anyone can ship a bipolar amplifier with an offset drift of less than 0.1 μV/°C. Because this comment appears immediately following Analog Devices' (PMI Div) OP-177E TC specification of 0.1 μV/°C, it seems to imply that our product does not meet its published specification.

Bob says ". . . you can measure performance at this level five times and get five different answers." True, there is some variation in measured values for all automatic testing; the goal is to refine the testing to a point where all five answers are very close together and then guardband for these test variations. The TC of the OP-177E is tested to a 0.1 μV/°C limit and is typically much better than that.

Derek Bowers
VP Engineering
Steve Sockolov
Linear Marketing Manager
Analog Devices
Santa Clara, CA

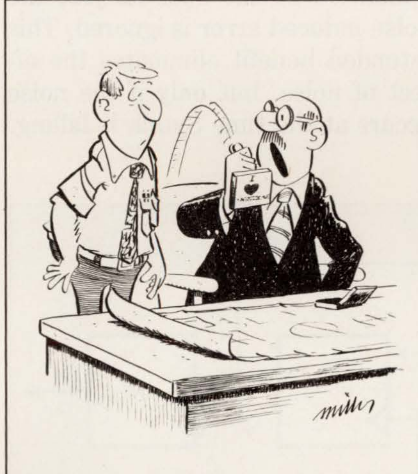
This recession's job market is "less friendly"

Julie Anne Schofield's article, "The Job Hunting Blues" (EDN, January 21, 1990, pg 230) is right on the mark.

As a 1971 graduate of Cal Tech who has had experience in many areas of electronics and applied physics, I've found the present job market much less friendly and much more competitive than when I was last job hunting in 1979. While cleaning out old magazines, I noticed that there were four or five times more job opportunities listed in EDN two or three years ago than in the current issues.

Julie writes, "Don't even mention the purported engineer shortage to an engineer. . ." That's for sure. I'm seriously considering leaving engineering to teach physics and astronomy. (I'm much less seriously considering going into music, but because only 20% of Juilliard graduates have music as their prime source of income, this seems less realistic.)

Craig McCluskey
Colorado Springs, CO



"What do you mean you don't get any recognition? This is your third 'I love engineering' this week!"

He eschews computer worship, be it Mac or PC

I'll take the liberty of paraphrasing J Thomas Baylor's letter about the Mac versus the PC in EDN, March 14, 1991, pg 26. He wrote ". . . people want to be able to use a computer, not hack with it." My version: "People want to be able to use a computer, not worship it."

I've been using MS-DOS-based PCs since about 1983, and I've never once lamented the lack of wastebaskets, file cabinets, and such on my screen. Worse yet in the eyes of "power users," I never once felt the compulsion to switch instantly from one program to the other, and I never felt unbearably lonely as the result of being a non-multiuser.

I agree with the Editor's comment about Apple's arrogance vis-a-vis an open bus and applications encouragement. I'll add to this the company's monopolistic, sole-source pricing philosophy, which has finally come around to bite Apple in the derriere, as witness the recent move to more reasonable prices.

Bill Travis
International Sales & Marketing Manager
Micro Networks
Worcester, MA

Frequency-synthesis technique questioned

The article, "Nonlinear division synthesizes multiple clock frequencies" (EDN, February 18, 1991, pg 169) by Sid Ghosh, is interesting in regard to the resulting phase jitter produced by dithering the divider between d and (d+1). The tabulated clock frequencies in Table 2 are all related multiples of 8 kHz including the T1 rate of 1544 kHz.

A PLL loop can synthesize all these frequencies mentioned in the first paragraph. The conventional analog VCO can be eliminated and a complete digital PLL can be implemented with the Signetics 74HC/HCT297 and a couple of programmable divide-by-N counters such as the 74HC/HCT40103.

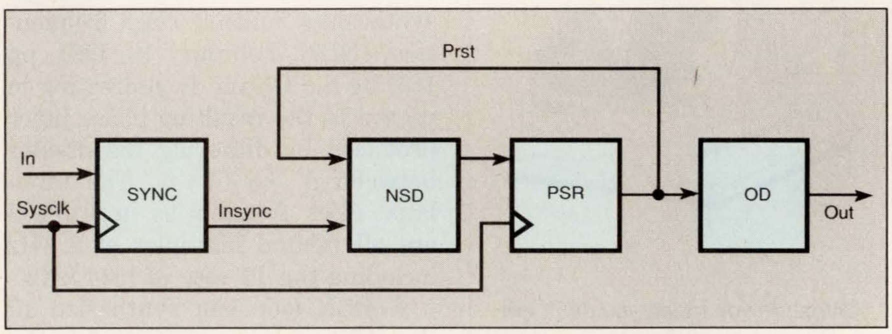
Richard L Panosh, President
Vista Medical and Electronic Engineering
Lisle, IL

A promise of more reliability and less noise

Ricardo Rabinovich's article "State-machine design curbs illegal states and transitions" (EDN, February 4, 1991, pg 95) promises novel ideas that might improve the reliability of the synchronous state machines I design. However, the proposed method of adding next-state-validation logic is likely to decrease, rather than increase, the reliability of such state machines.

Ricardo discusses several approaches to improved reliability. However, it might be prudent to add another flip-flop at the input stage of the synchronizer so that the exclusive-OR gate input is not taken from the potentially metastable output of the first flip-flop.

The article discusses the implementation of a state machine that includes next-state-validation circuitry. I believe this implementation is less reliable than the equivalent conventional implementation with input synchronization of such state machines shown in the **figure** below:



The remainder of either state machine operates entirely on synchronous signals. In such a machine, errors are due to design error, circuit element failure, or unexpected 1-shot events, such as noise. However, if the next-state-validation logic is derived from the same equations as the next-state-generation logic, then errors in the state-machine specification will be present in both parts of the state machine, and it will do exactly what the designer (wrongly) tells it to do.

Because the proposed circuit has more components than a more conventional implementation, it will experience circuit-element failures more often and be less reliable.

Finally, Ricardo's circuit is supposed to be resistant to illegal transitions caused by noise. I will assume that an error occurs when, due to noise, the present-state register (PSR) is loaded with an inappropriate or illegal value.

If noise is the problem, the conventional state machine will present incorrect values to the PSR only if the noise occurs during setup and hold around the Sysclk edge.

In contrast, noise can affect the article's circuit in other ways:

1. NSD outputs are wrong around the edge of $\overline{\text{Sysclk}}$. In this case the NSR is loaded with an incorrect value and, if the next-state-validation circuit does its job, the noise-induced error is ignored. This intended benefit eliminates the effect of noise, but only if the noise occurs at the time Sysclk is falling. Noise occurring at this time cannot affect the conventional implementation because it samples the NSD output only at the rising edge of Sysclk.

2. NSD outputs are wrong around the edge of Sysclk. In this case Ricardo's implementation will not notice the error until after it has been loaded into the PSR and causes an illegal transition. The conventional implementation requires that the NSD include logic to deal with illegal states, but avoids the NSVAL (next-state-validation) burden.

3. NSVAL output is wrong around the edge of Sysclk. The next-state-validation circuit is also subject to noise. Noise causes a valid state transition to be ignored, an invalid state transition to be taken, or worst of all, the multiplexer to take some bits from the present state and some from the next state.

4. Multiplexer output is wrong around the edge of Sysclk. The multiplexer inputs, outputs, and circuits themselves are subject to noise, which may produce an illegal state transition.

Mechanism 2 (above) is the same mechanism that causes illegal transitions in a conventional state machine and would be expected to occur with a similar frequency in both implementations. Mechanisms 3 and 4 are unique to the proposed implementation and would make it less reliable than a conventional implementation.

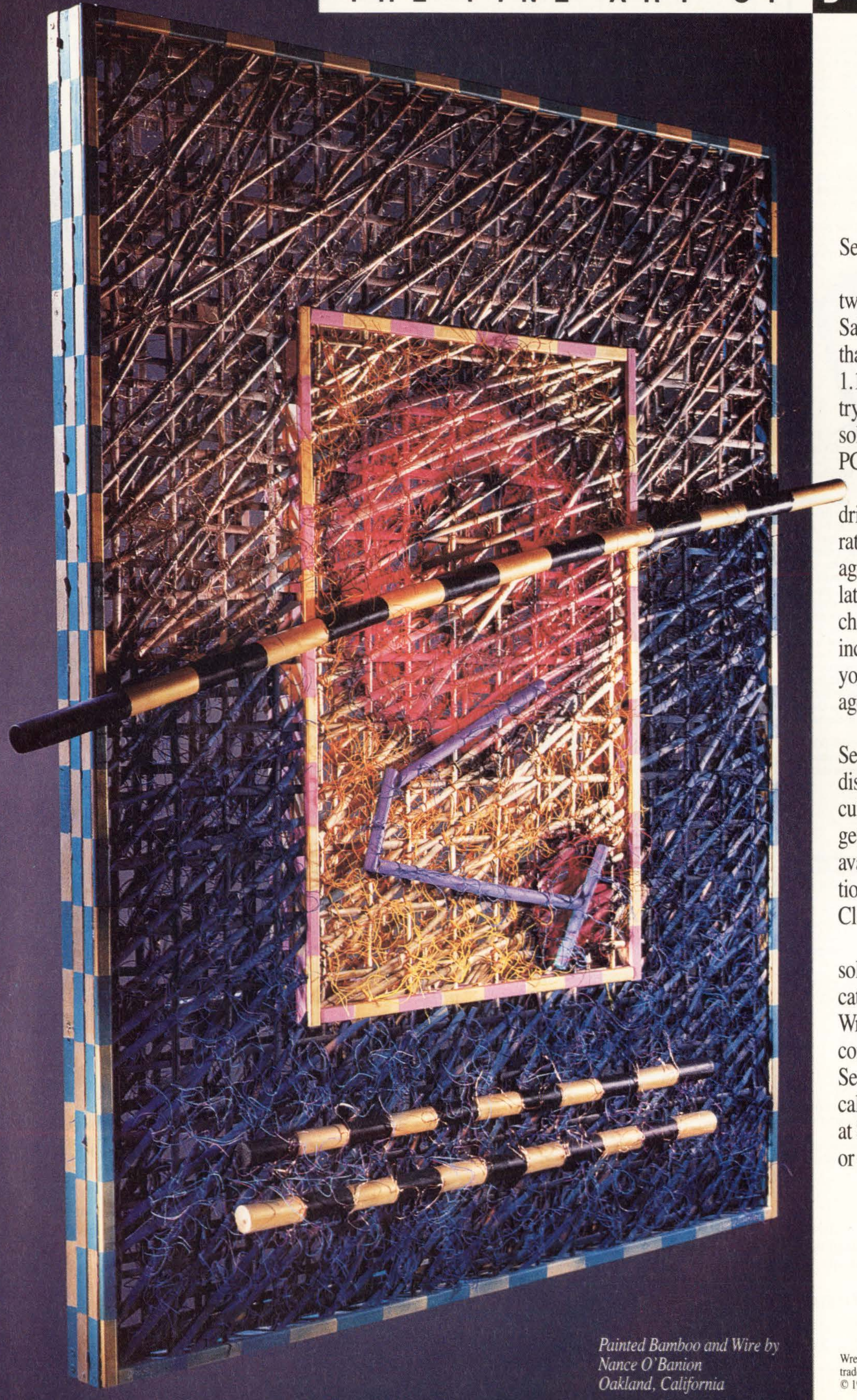
Ricardo makes many good points about synchronization, decoupling, and timing analysis to ensure the most reliable state machine possible. But by adding more logic to try to detect illegal transition, he has made the circuit more vulnerable to noise.

Allen E Tracht
Principal Engineer
IOtech Inc
Cleveland, OH

(The author's reply: Some of the points that Allen Tracht has raised make sense, but others are debatable.

The synchronizer circuit does not require an additional flip-flop because the output of the exclusive-OR gate is connected via the multiplexer to a flip-flop input. All three flip-flops of the input are synchronized by the same clock; therefore, a potential metastable condition in the first flip-flop will not propagate to the last flip-flop unless the metastable condition lasts longer than the clock cycle. An additional flip-flop at the input would be vulnerable to the same problem.

A circuit like the one in my article could require additional parts in a discrete implementation. This addition might be detrimental to system reliability due to the parts count. However, the additional



Painted Bamboo and Wire by
Nance O'Banion
Oakland, California

SIGNALS & NOISE

supervisory function could improve the overall reliability of the system. The kinds of techniques presented in my article are oriented toward ASIC implementations where the number of additional gates required for self-checking might not significantly jeopardize the overall reliability of the circuit.

I have not claimed 100% noise immunity for the self-checking circuit; rather, this circuit increases overall circuit-noise immunity.

Illegal states or transitions would be almost unavoidable if this circuit were to operate in a noisy environment. My article focuses on recovering from random noise. Redundant circuitry provides a recovery mechanism when an isolated fault occurs in either circuit, but not in both.

In a conventional state-machine architecture, a noise glitch will almost certainly put the state machine in an undesired state. The self-checking circuit (NSR/NSVAL/MUX) does not let the machine transit to a wrong state. Adding components for the additional circuit increases the possibility of catching more noise. However, noise in the self-checking circuit would not create erroneous state transition, but at worst, a 1-clock delay to a valid one.

A conventional state machine with an input deglitcher is also vulnerable to noise of duration wider than the deglitcher can filter out. The state machine with a self-checking circuit can detect and solve for illegal input combinations, thereby preventing illegal transitions.

This technique will build "forgiveness" in the circuit, but it will not replace good design practices.)

The measure of a solar cell's thickness

Jay Fraser's article, "Who cares about power?" (Professional Issues, EDN, November 8, 1990, pg 381), is well written, but I question the statement on page 382 that reads: "...solar cells...have to be relatively thick, 25 to 50 mm." Unless I'm missing something, any solar cell, no matter how transparent, won't let light penetrate more than a quarter of an inch or so. The intended measurement was probably 25 to 50 *mils*, which is thick for silicon wafers, but not as thick as the numbers given.

James L Rieger, PE/PTBW
Ridgecrest, CA

(The author's reply: James Rieger is indeed correct. The measurement of solar cells should be 25 to 50 mils thick.)

Correction

The News Break "A/D converters come in a new package" (EDN, March 14, 1991, pg 18) contains an error. The edited statement, "Missing codes are not guaranteed," changes the meaning; the statement should read "No missing codes are guaranteed."

Mea culpa

In the Technology Update on the STD Bus CPU board (EDN, March 28, 1991, pg 51), the Computer Dynamics Sales Inc listing in Table 1 got botched. The entry listed for "Sales Inc" is actually part of the Computer Dynamics Sales Inc data. EDN apologizes for the error.

HAVE YOUR SAY

Send your letters to Signals & Noise Editor, EDN Magazine, 275 Washington St, Newton, MA 02158. Or, send us a message via MCI mail at EDNBOS or via EDN's bulletin-board system at (617) 558-4241 and leave a letter in the EDITORS Special Interest Group. You'll need a 2400-bps or less modem and a communications program that is set for eight data bits, no parity, and one stop bit, or 1200/2400, 8N1 in shorthand.

EDN

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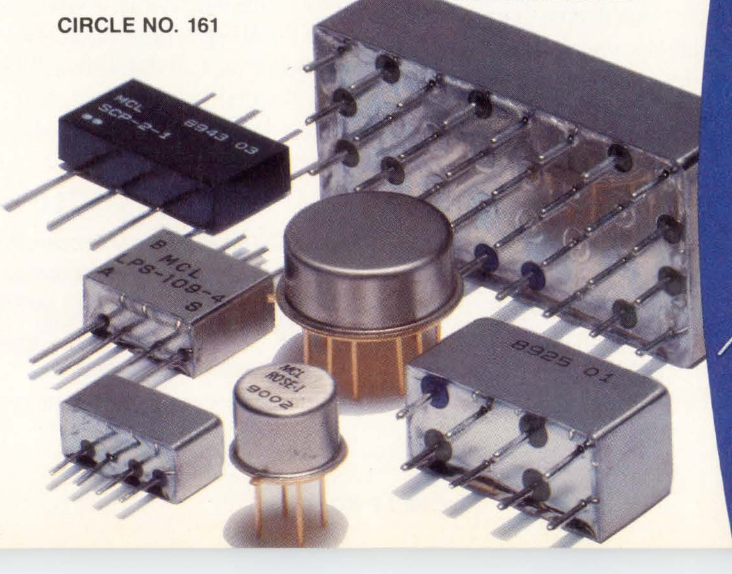

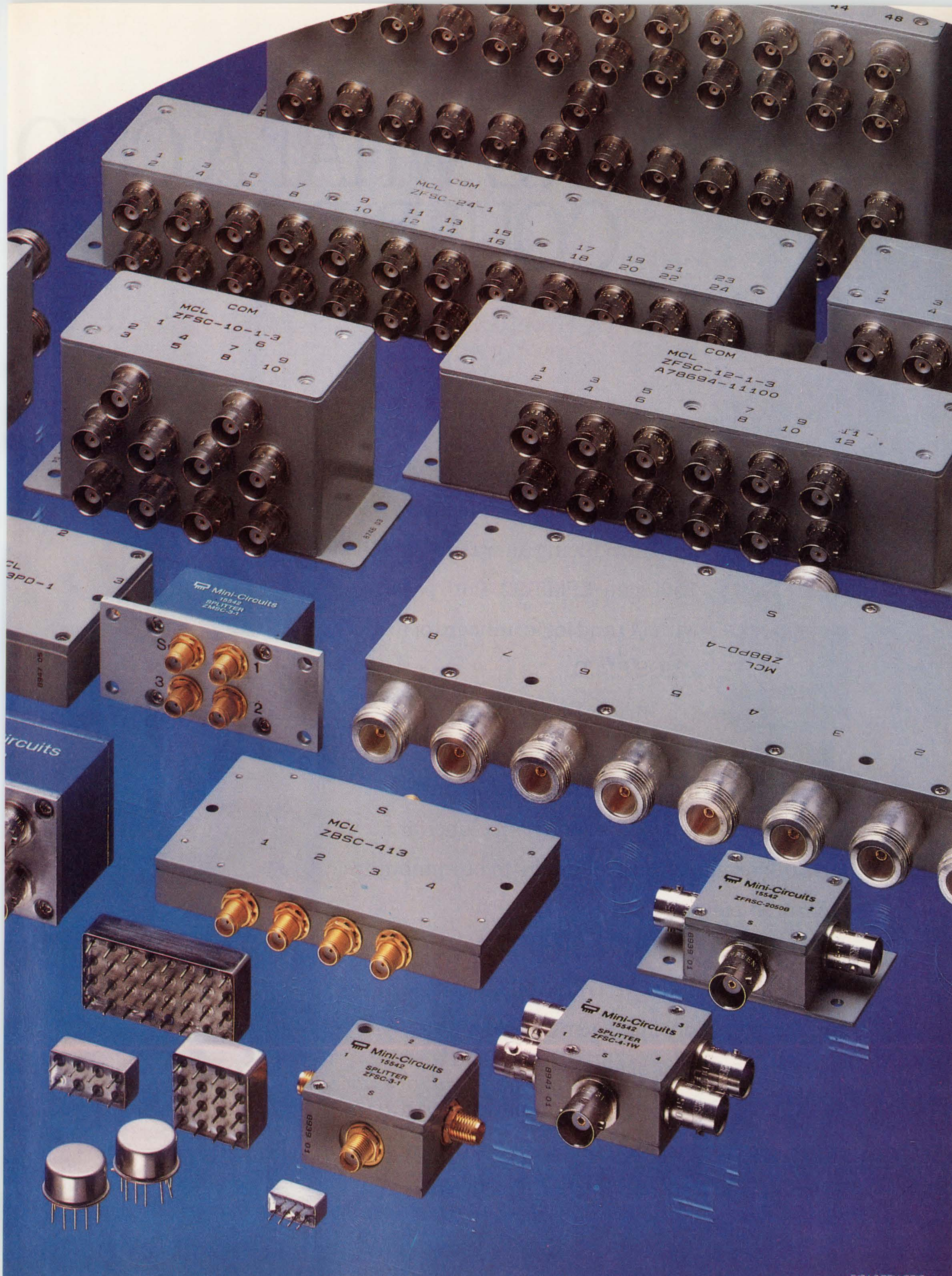
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MCL COM ZFSC-10-1-3
MCL COM ZFSC-12-1-3 A78694-11100
Mini-Circuits 15542 SPLITTER ZMSC-3-1
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ASK EDN

EDITED BY JULIE ANNE SCHOFIELD

Single-board computer needs VGA driver board

Does anyone out there know of a simple and cheap driver board to give VGA output from a single-board computer? We sell a 4×3-in. CMOS single-board Forth computer card, and a customer wants to drive a Hitachi 6-in. VGA color LCD. Any ideas?
The Saelig Co
Victor, NY

We know of three companies that make driver boards that meet your requirements:

Ampro Computers Inc
990 Almanor Ave
Sunnyvale, CA 94086
(408) 522-2100
FAX (408) 720-1305

Cybernetics Microsystems
Box 3000
San Gregorio, CA 94074
(415) 726-3000
FAX (415) 726-3003

Micromint Inc
4 Park St
Vernon, CT 06066
(203) 871-6170
FAX (203) 872-2204

Second sources sought

We would like to find sources for the following parts: the Western Digital WD92C32 phase-locked-loop disk data separator and the NEC μPB9201C floppy-disk interface. The manufacturers no longer make these parts and our buyer has bought all he could find. If you don't know of a source, perhaps you could appeal to the EDN readers.
Margaret Motamed
Principal Member
Engineering Staff
Xerox Corp
El Segundo, CA

We checked with the Cahners CAPS system, and apparently Western Digital is the only company to have manufactured the 92C32. We were unable to locate a second source for the NEC floppy-disk interface. If any EDN reader knows of a source for either of these parts, please contact ASK EDN.

Big problem solved

I have a big problem: Who is the manufacturer of the TP3054 chip? Please tell me the company from which I can order this chip.
Joe Müller
Manager of Product Planning
John Lay Electronics
Littau, Switzerland

The CAPS system, which is available from Cahners Technical Information Services, lists two TP3054 manufacturers:

National Semiconductor Corp
Box 58090
Santa Clara, CA 95052
(408) 721-5000
FAX (408) 730-0764

Texas Instruments Inc
Microprocessor & Microcontroller Products Div
Box 809066
Dallas, TX 75380
(800) 232-3200.

Reader wants to reduce noise of heartbeat signal

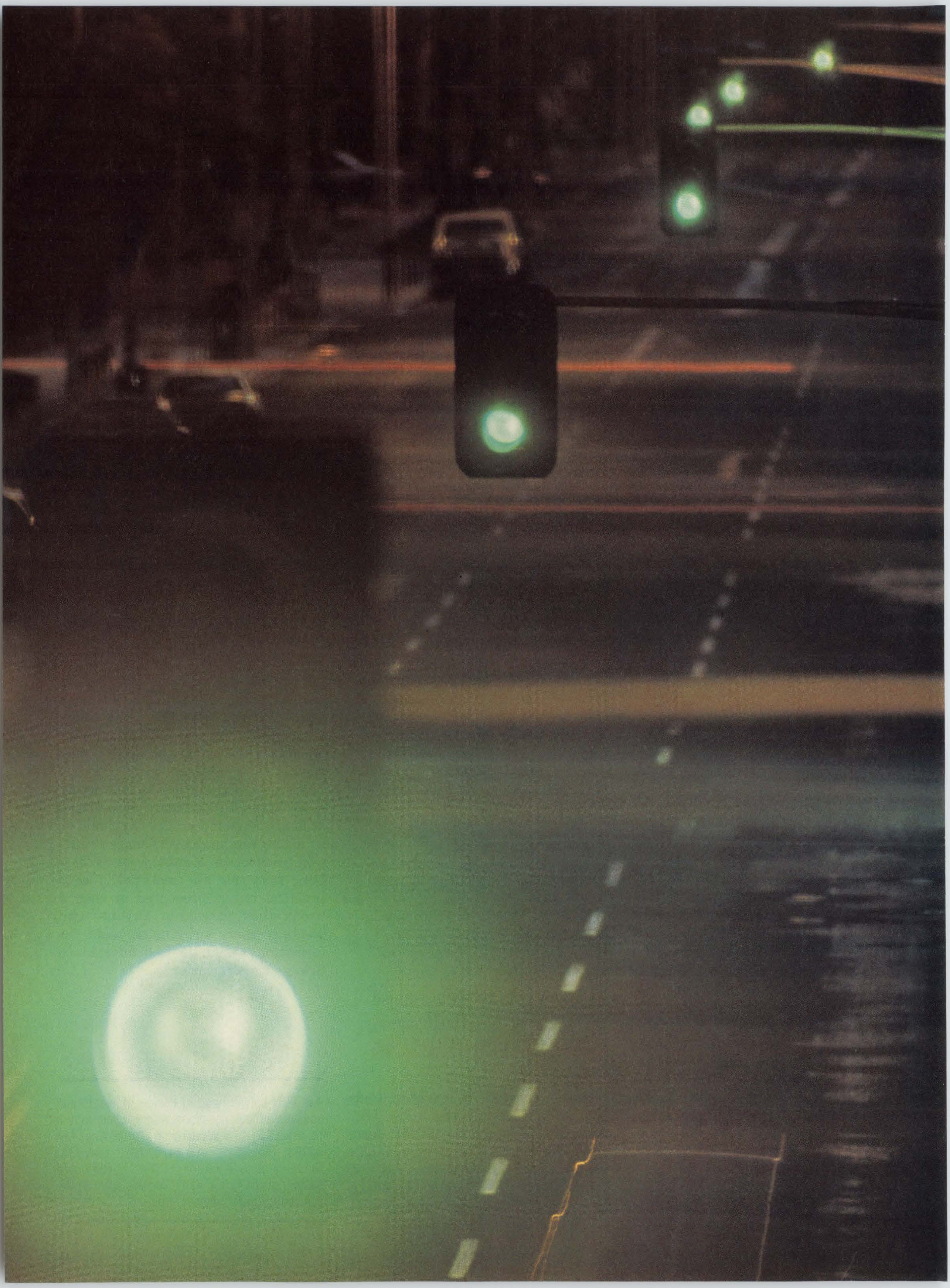
I am interested in learning techniques to decouple the noisy IBM power supply from my circuit cards that plug into the bus. Such a technique would let me work with very small signals such as EKG heartbeats and recording-studio-quality signals. Using op amps and trying to process signals in the millivolt and microvolt ranges, I get a lot of common-mode noise and such being fed in by the very noisy IBM power supply. Also, as programs are executed, the noise increases, so I need a way to make the 5, 12, −5, and −12V power supplies clean while the data fly all over the place.

As you've probably guessed, I've tried a wide range of capacitors, resistors, and inductors without success. I suspect that besides the noise I can see on a 20-MHz scope, there is even more outside this band. If someone could provide techniques to work with signals like this, it would open the door for better-quality products. I look forward to any light you can shed on this subject.
John Bercik
Covox Inc
Eugene, OR

No short reply in Ask EDN will solve your problem. Over the years, however, EDN has run a good number of contributed articles on noise reduction.

Also, Analog Devices is conducting a series of DSP seminars at locations around the country. The last hour or so of the seminar covers noise reduction. Associate Editor Dan Strassberg says that the material is very practical but is presented at such a break-neck pace that anyone who wants to carry away much useful information would be well advised to bring a tape recorder.

Ask EDN solves nagging design problems and answers difficult questions. Address your letters to Ask EDN, 275 Washington St, Newton, MA 02158. FAX (617) 558-4470; MCI: EDNBOS. Or send us a letter on EDN's bulletin-board system at (617) 558-4241; leave a letter in the ask_edn Special Interest Group.



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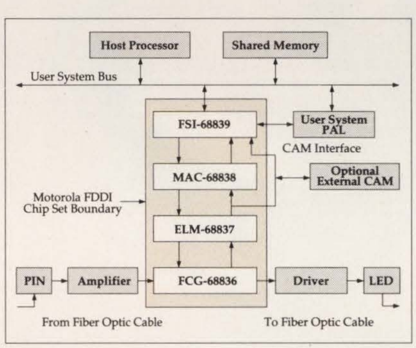

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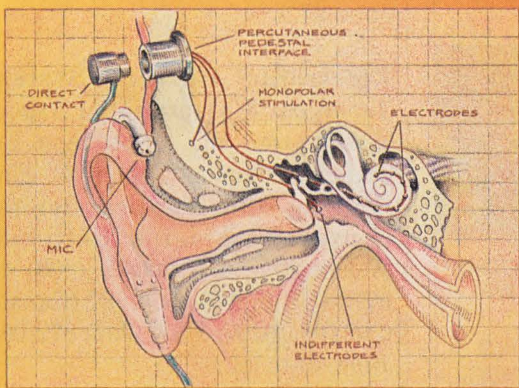

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Gain Bandwidth Product: 3.0 MHz typ.
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CIRCLE NO. 141

CALENDAR

Embedded Processor Design Seminar, Various Cities. Intel Corp, 5000 W Chandler Blvd, Chandler, AZ 85226. (800) 548-4725; in AZ, (602) 941-3000. May 21 to June 27.

Electronic Warfare Systems: Technical & Operational Aspects, Washington, DC. Continuing Education Program, School of Engineering and Applied Science, George Washington University, Washington, DC 20052. (800) 424-9773 (US); (800) 535-4567 (Canada); (202) 994-6106. FAX (202) 872-0645. June 10 to 14.

Usenix Technical Conference and Exhibition, Nashville, TN. Usenix Conference Office, 22672 Lambert St, Suite 613, El Toro, CA 92630. (714) 588-8649. FAX (714) 588-9706. June 10 to 14.

IEEE MTT-S International Microwave Symposium, Boston, MA. LRW Associates, 1218 Balfour Dr, Arnold, MD 21012. (301) 647-1591. FAX (301) 647-5136. June 11 to 14.

EMC-91 Product Compliance First Principles Colloquium, Santa Clara, CA. Ghery Pettit, Apple Computer Co. (408) 285-2528. June 12 to 13.

University, Government, and Industry Microelectronics (UGIM) Symposium, Melbourne, FL. Thomas Sanders, Dept of Engineering, Florida Institute of Technology, 150 W University Blvd, Melbourne, FL 32901. (407) 768-8000, ext 8769. June 12 to 14.

Reliability: The Next Generation (short course), Washington, DC. George Washington University, School of Engineering & Applied Science, Washington, DC 20052. (800) 424-9773; in DC, (202) 994-6106; in Canada, (800) 535-4567. June 17 to 21.

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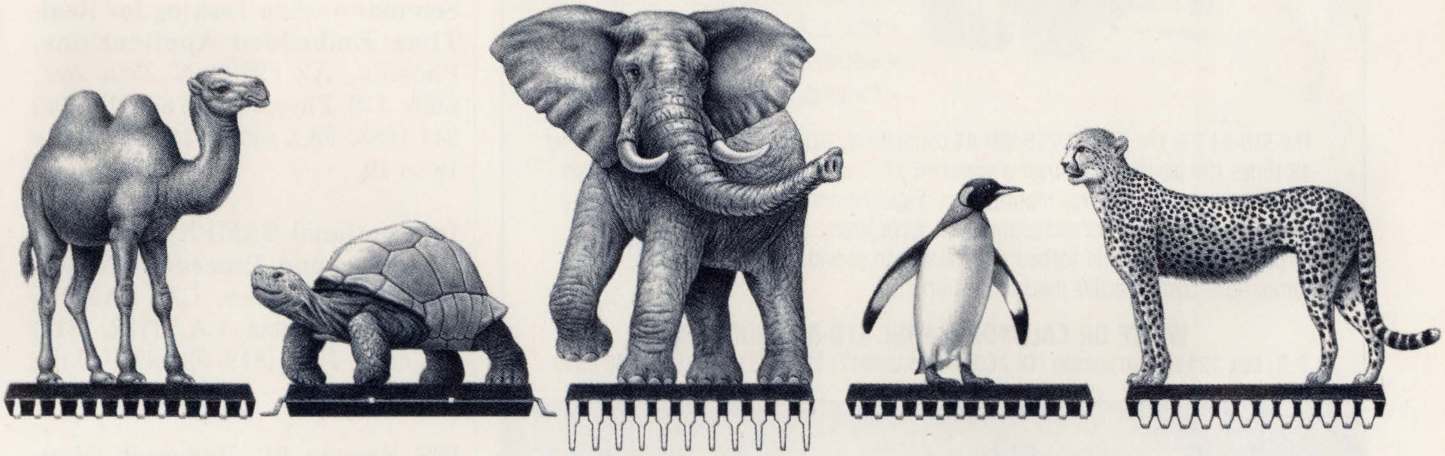

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	CXK581000M	100/120	SOP 525mil	L/LL	B/X	Now
	CXK581100TM	100/120	TSOP (normal)	L/LL	B/X	Now
	CXK581100YM	100/120	TSOP (reverse)	L/LL	B/X	Now
	CXK581001P	70/85	DIP 600mil	L/LL		Now
	CXK581001M	70/85	SOP 525mil	L/LL		Now
	CXK581020SP	35/45/55	SDIP 400mil			Now
	CXK581020J	35/45/55	SOJ 400mil			Now
128Kx9	CXK77910J	17/20	SOJ 400mil		Sync ASM	3/Q '91
256Kx4	CXK541000J	25/30/35	SOJ 400mil			3/Q '91

L = Low LL = Low,Low B = 3 Volt X = Extended Temperature

SONY

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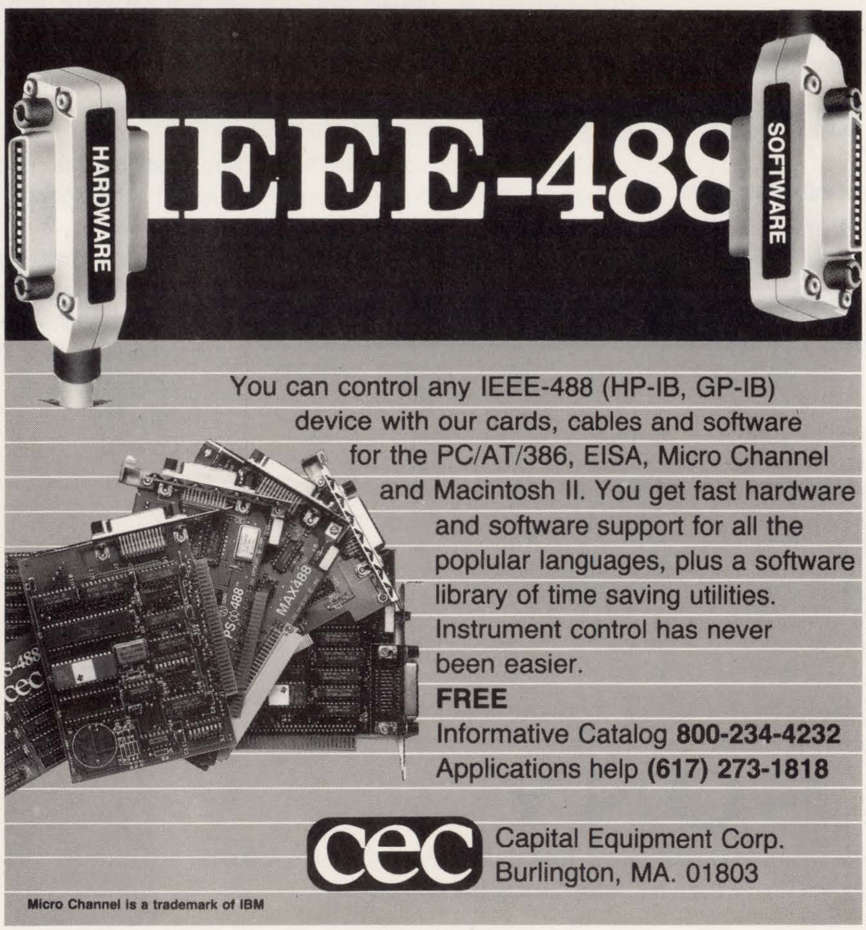
Sony Canada, 411 Gordon Baker Rd., Willowdale, Ontario M2H 256

CIRCLE NO. 44



CIRCLE NO. 45

CALENDAR

Design Automation Conference, San Francisco, CA. Alfred Dunlop, Program Chair, 28th DAC, MP Associates Inc, 7490 Clubhouse Rd, Suite 102, Boulder, CO 80301. (303) 530-4333. June 17 to 21.

Seminar on Ada Tasking for Real-Time Embedded Applications, Phoenix, AZ. 9630 N 25th Ave, Suite 118, Phoenix, AZ 85021. (602) 944-1883. FAX (602) 944-3253. June 18 to 19.

International SAMPE Electronic Materials and Processes Conference, Los Angeles, CA. SAMPE, Box 2459, Covina, CA 91722. (818) 331-0616. FAX (818) 332-8929. June 18 to 20.

ISS Europe 91, Budapest, Hungary. SEMI, 805 E Middlefield Rd, Mountain View, CA 94043. (415) 964-5111; (415) 940-6901. June 19 to 21.

Supercomputing USA/Pacific 91, Santa Clara, CA. Meridian Pacific Group Inc, 116 E Blithedale Ave, Suite 2, Mill Valley, CA 94941. (415) 381-2255. FAX (415) 381-1451. June 19 to 21.

SEMICON/Kansai-Kyoto 91, Kyoto, Japan. SEMI, 805 E Middlefield Rd, Mountain View, CA 94043. (415) 940-6901; (415) 964-5111. June 19 to 22.

CFC Alternatives Conference, Burlingame, CA. Angela Hoyte, Miller Freeman Expositions, 600 Harrison St, San Francisco, CA 94107. (415) 905-2354. FAX (415) 905-2239. June 24 to 26.

Test Engineering Conference, Atlanta, GA. Miller Freeman Expositions, Test Engineering Conference, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. June 24 to 27.

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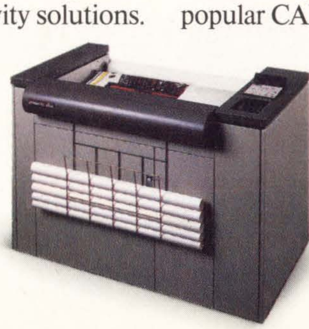

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CIRCLE NO. 143

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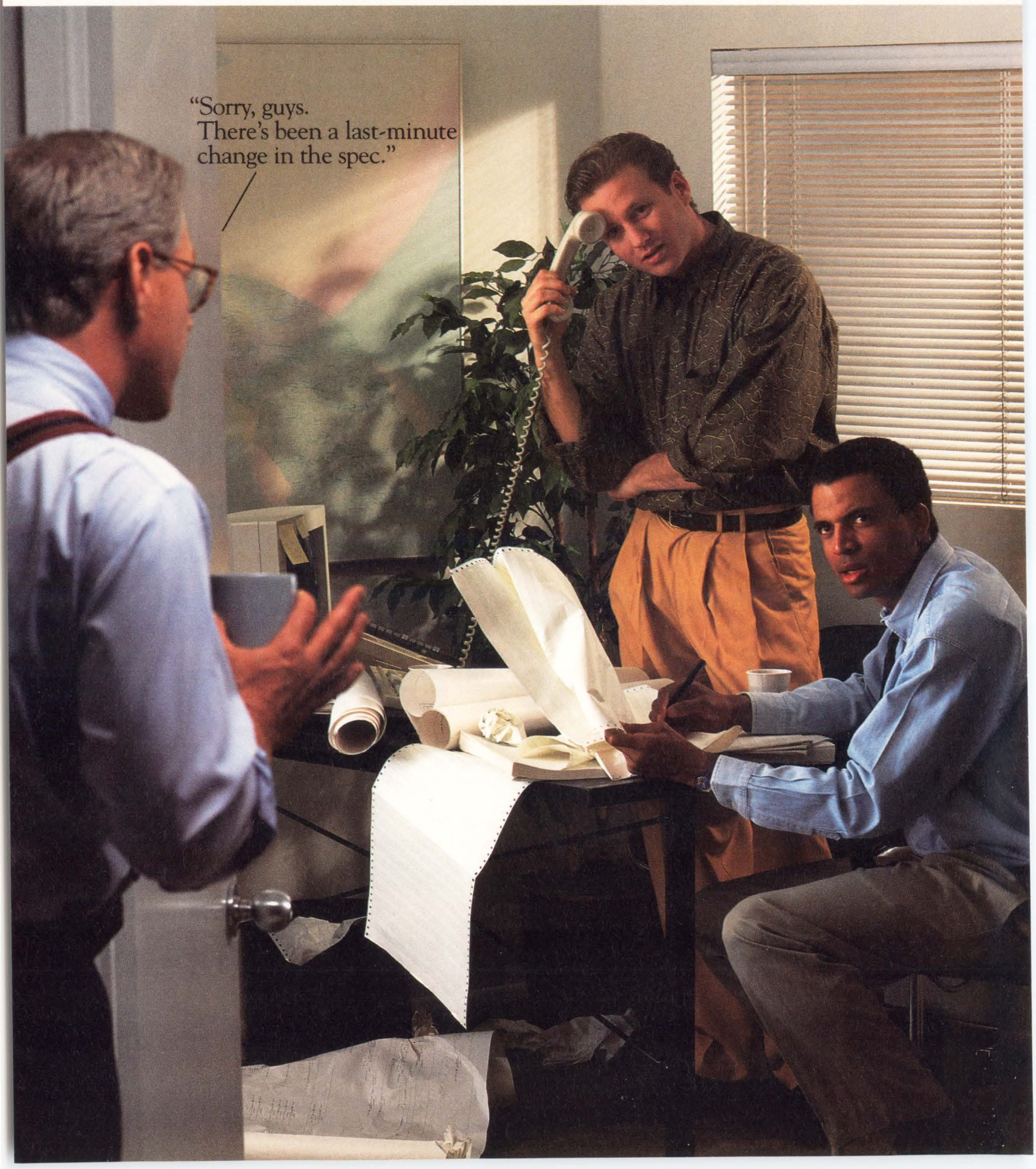

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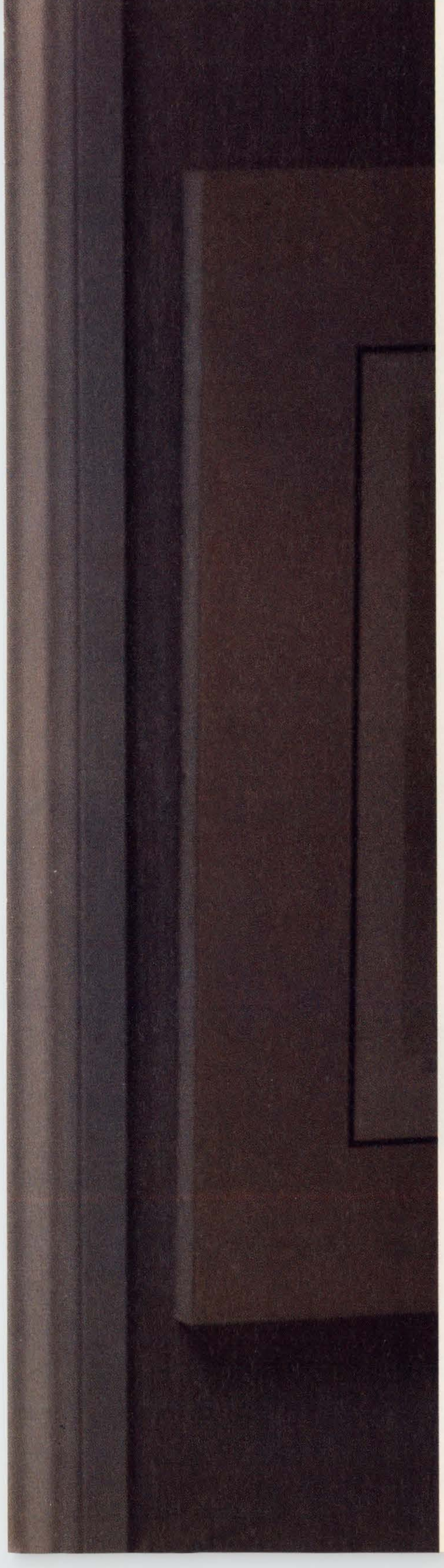

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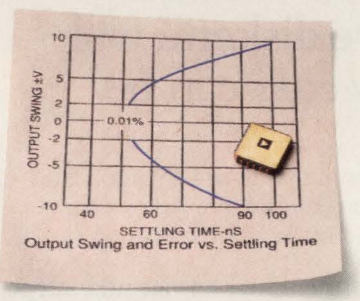

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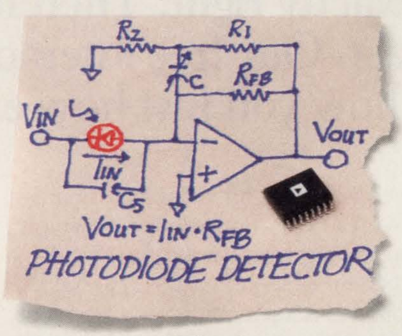

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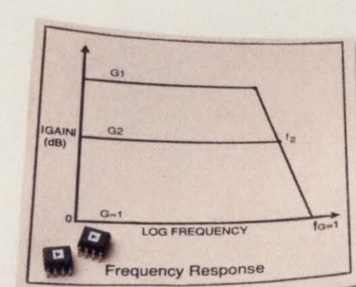

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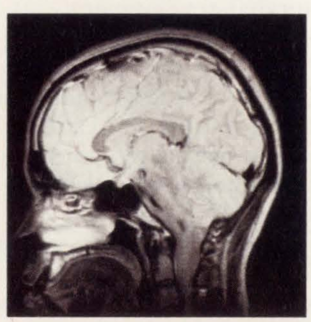

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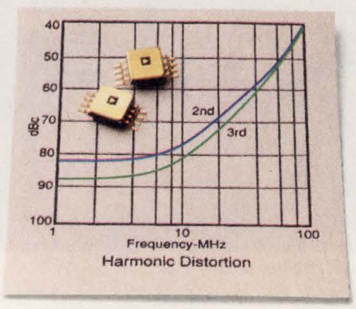

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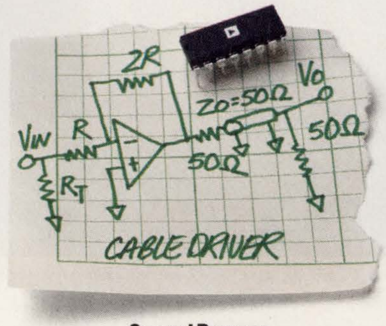

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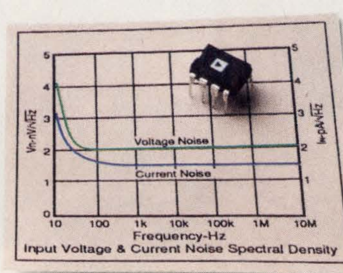

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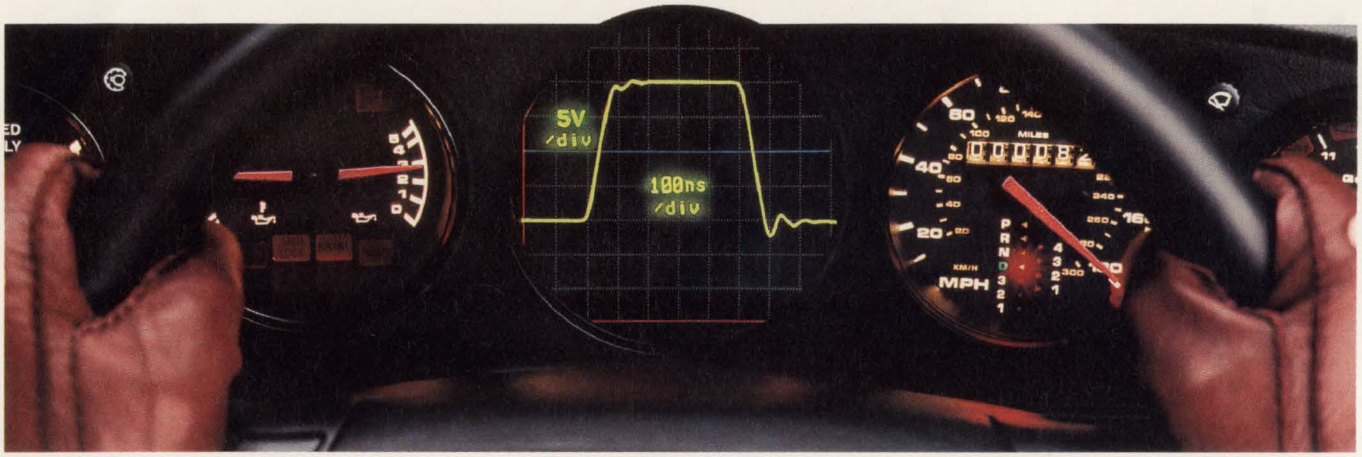

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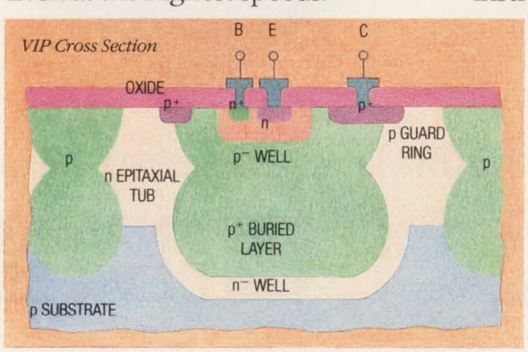

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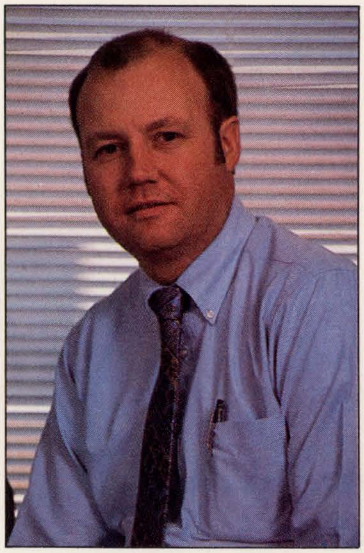
EDITORIAL

Good luck, ACE



Several weeks ago, Compaq Computer Corp announced the Advanced Computing Environment (ACE) consortium, a group established to bring standardized RISC technology to personal computers. If the ACE plan bears fruit, personal computers in the mid-90s will have the power of industry-standard RISC systems, and users will be able to take advantage of standard PC software. To meet these goals, consortium members must develop standard hardware and software based on Mips Computing Systems' RISC microprocessors.

Although the consortium's plans call for each company to build on its own strengths, we're not holding our breath while we wait for advanced-RISC-computing (ARC) hardware and software products to reach users. In fact, the group's ARC specifications won't be available to non-ACE companies until the first ARC systems are sold. So much for an open and competitive market. If you think you've heard a similar story, you may be thinking of the consortium that Compaq led to adopt the Extended Industry Standard Architecture (EISA) several years ago. The member companies laid down grand plans for EISA to challenge IBM's Micro Channel Architecture. Today, you'll have difficulty finding an EISA PC or EISA add-in cards. The invisible hand of the market left EISA behind.

A similar scenario may loom ahead for the ACE companies: Because they're "cooperating," they're not competing. As is typical of such uncompetitive consortia, nothing in the ACE announcement suggests anything innovative in the group's approach to developing hardware or software. If anything, the consortium stifles innovation by adopting a broad plan for a so-called standard computer architecture and for operating systems arrived at by committee decision. I doubt that the ACE companies asked their customers what sort of mediocre committee "standard" they wanted vendors to foist on them.

Whenever a large number of companies forms a consortium to tackle a fast-moving market they let slip by them, mediocrity results. If the ACE members are serious about catching IBM and Sun Microsystems in the workstation and high-performance-PC market, they and we would be better off having the members act as competitors. By forcing each other to do better, they might come up with new products that would leave their rivals behind. After all, it has happened before. Just ask Sun and IBM.

Jon Titus
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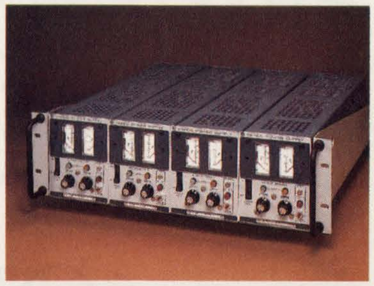

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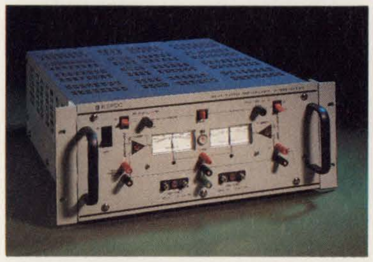

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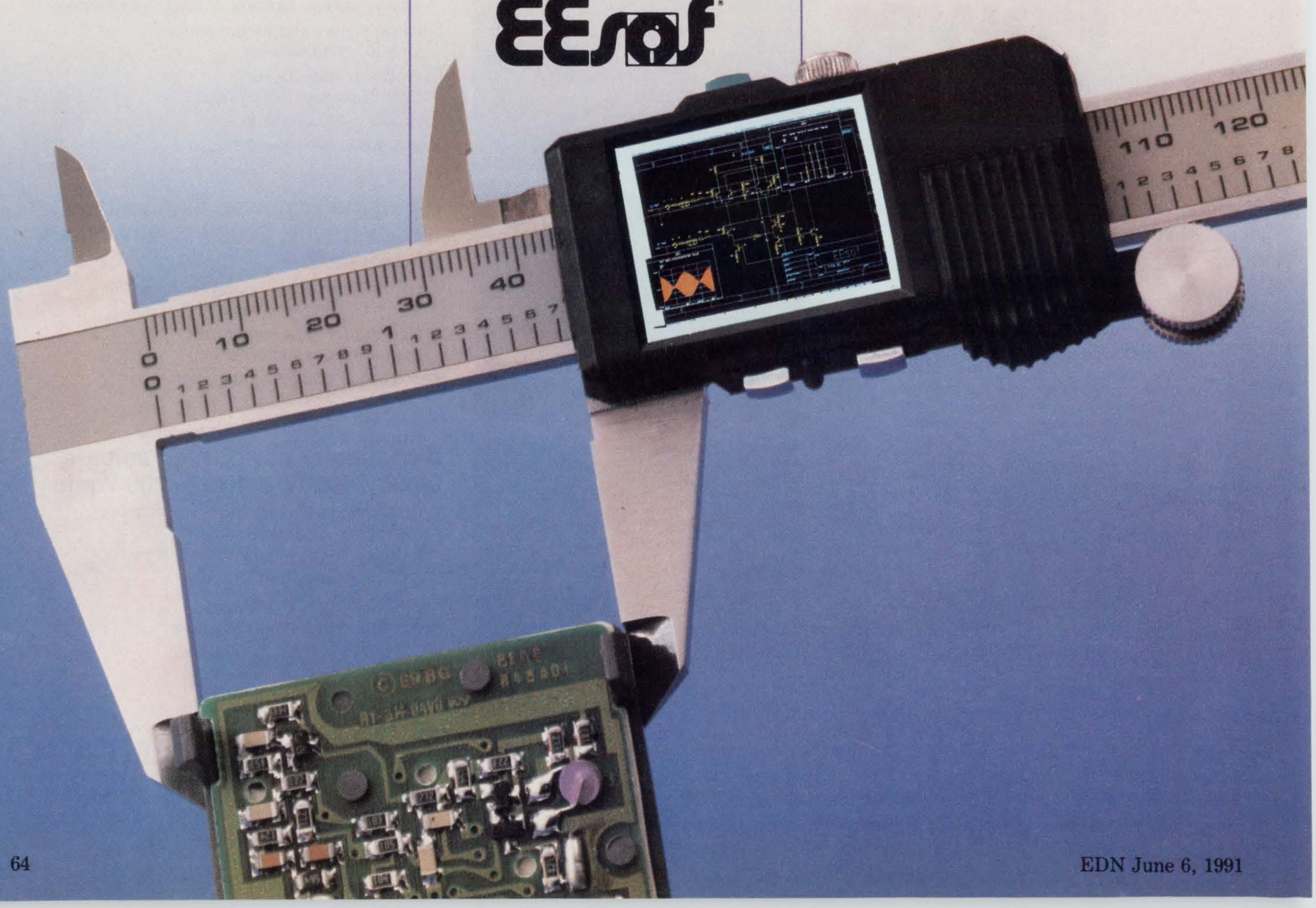


MIXED-SIGNAL DESIGNS

Concurrency, circuitry foster testability

You can add circuitry to the analog part of your mixed-signal design, but the best way to ensure your design's testability is to coordinate with your test engineers.

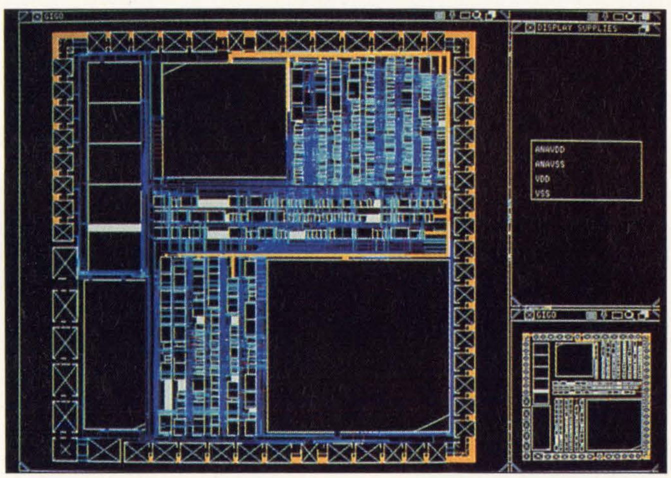
Michael C Markowitz,
Associate Editor

Digital circuit designers have a wealth of well-documented design techniques to guide them toward high circuit testability. Unfortunately, as they incorporate more analog circuitry in their ICs, designers sail further into uncharted waters. And these uncharted waters are rough on your budget; mixed-signal vendors estimate testing eats up 25 to 50% of NRE (nonrecurring-engineering-cost) dollars. Worse, test-program development can take from one to three months for a mixed-signal design versus a day or two for a digital design.

Mixed-signal circuits don't have a checklist of "rules" of testability. "Checklists create too many questions" for you to use them on mixed-signal designs, according to Brice Baker, CAE Manager at Gould AMI. You can't blindly start adding scan, partitioning, multiplexing, and built-in self-test functions. Blind adherence to added test-logic functions will likely cause your circuit to fall out of specification—though the added circuitry will enable you to measure how far. When you're designing a mixed-signal circuit, you must carefully take account of the impact of each added function.

In some regards, mixed-signal circuits are like strictly digital designs. The secret to high testability is providing access to internal nodes for control and observation. The two design types differ, though, in the performance cost of such access. Whereas the parasitic effects of extra signal lines on a digital node may degrade performance by hundreds of picoseconds, the effect of extra signal lines on analog circuit components can be devastating.

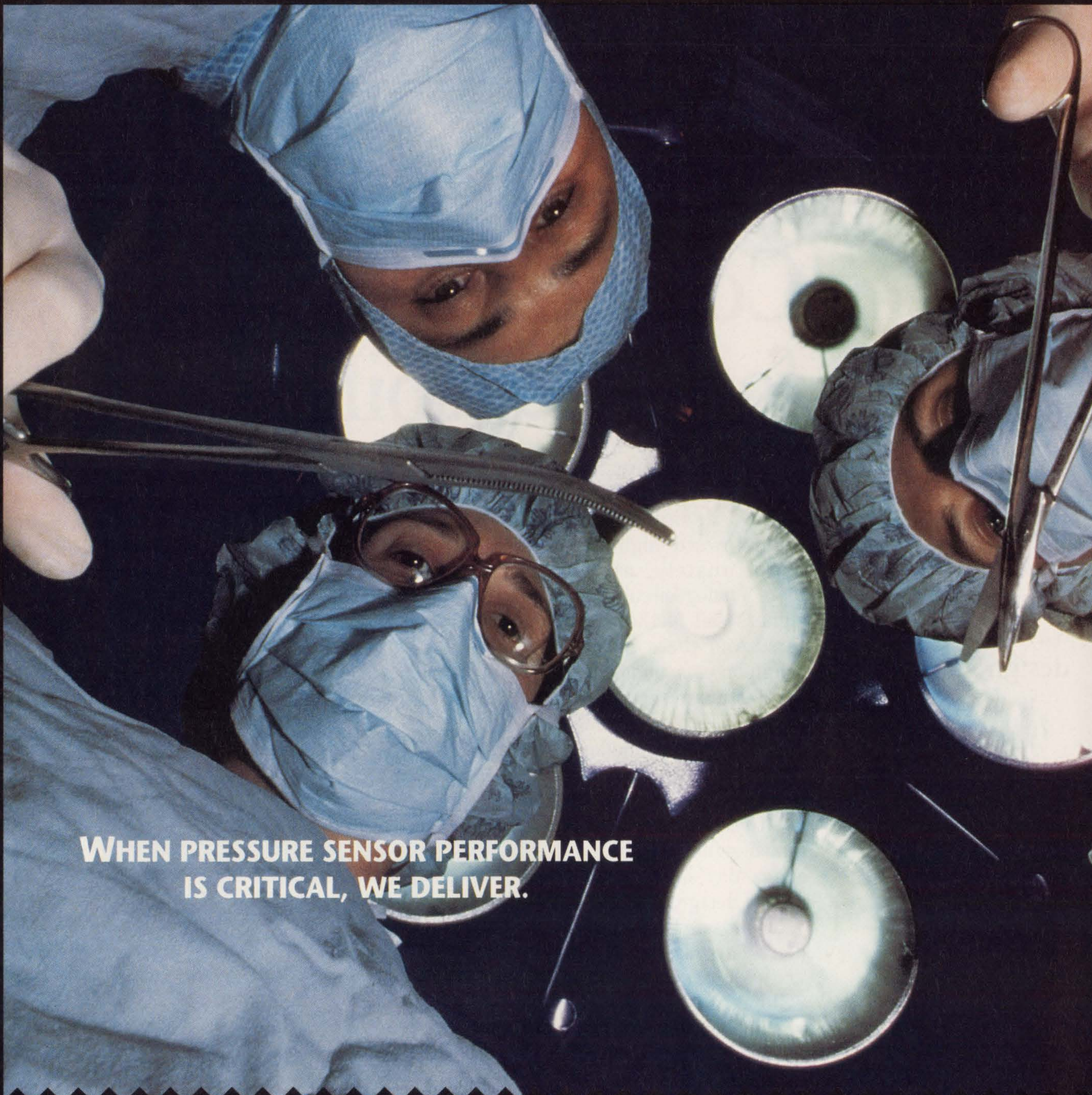
The difficulty stems from the difference in what you're trying to measure.



Partitioning the analog and digital subcircuits makes each more testable. *Paying careful attention to the layout and placement of the power and clock lines makes the circuit more resistant to noise. (Photo courtesy Silvar Lisco)*

You evaluate digital logic by simply measuring voltage (high/low) and sometimes current. Analog measurements, on the other hand, include circuit response in the time and frequency domain, temperature variations, offset voltages, leakage currents, and stability conditions. And measuring these levels requires such additional tools as Bode plots, according to Randeep Soin, technology specialist at Genrad Ltd.

Solving the mixed-signal test problem


WHEN PRESSURE SENSOR PERFORMANCE
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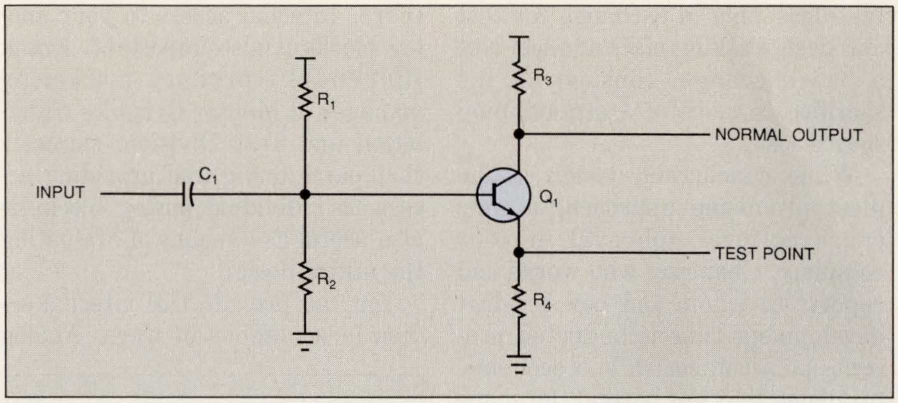
isn't easy. CAE tools for analog and mixed-signal design lag behind those for digital design, and even if the tools were comparable, metrics for measuring the test coverage of analog circuits are imprecise. High fault coverage, the digital benchmark, has little meaning in the analog domain.

The most promising approach to making testable mixed-signal circuits involves concurrent engineering. Standard sequential design styles have you design the part and pass it to the test engineer. The test engineer then writes the test program and hands it to the manufacturing engineer. Manufacturing builds the tooling and uses the test program to test the part. Often in mixed-signal design, this sequential flow is further complicated because different designers create the analog and digital logic.

The flaw in this development flow is that design decisions that cause test escapes and manufacturing difficulties aren't usually identified until after you've finished creating the circuit. As a result, the cost of a redesign is weighed against test and manufacturing kluges. Too often the kluges win.

Using sequential development, even if the analog and digital designers communicate well, there is little feedback from test or manufacturing to design. Concurrent engineering attempts to guarantee feedback between departments and to guarantee that such feedback will come when it will do the most good—before the design is finished. According to Mani Soma, Associate Professor in Electrical Engineering at the University of Washington, test structures can't be added as an afterthought. Test planning must be an integral part of the design phase of the mixed-signal circuit.



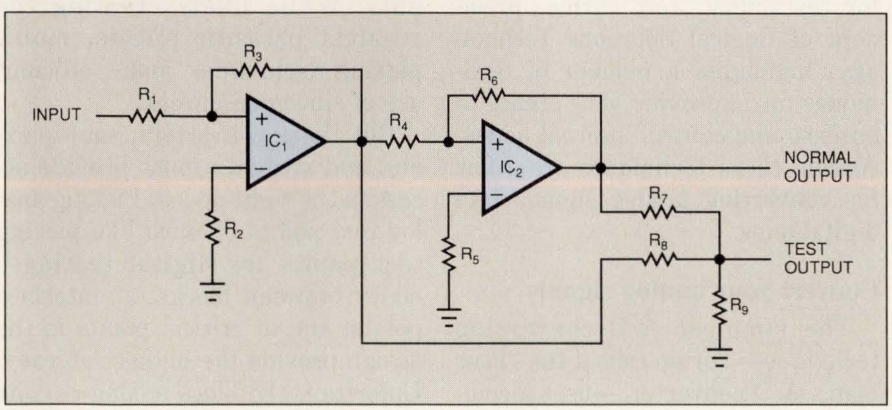
Among the best places for an analog test point in a discrete amplifier circuit *is at the top of the emitter resistor (R_4). Because this point is generally a low-impedance point, connecting high-impedance test equipment won't seriously impair performance. (Redrawn from "Testability Practices in the 1990s")*

Everyone works together

Concurrent engineering merges all of the distinct development efforts into a joint effort. Not that you, as designers, develop test programs and marketing plans; rather, that you better understand the problems and issues of the other disciplines and weigh their impact on your design. As a result, the test engineer can recommend locations for you to insert test points while you are creating your design rather than asking you to kluge them in after you've simulated and debugged your circuit.

The need for concurrent engineering is acute because designers often have limited knowledge of test limitations and capabilities, according to Tom Quan, director of analog IC tools at Cadence Design Systems. Generally, you don't know enough about such issues as DUT (device under test) boards, tester cabling, load boards, power supplies, and the parasitic capacitance and resistance of the test equipment. This lack of knowledge can translate into testing complications when you begin to use sequential engineering.

Though mixed-signal test development will still take longer than digital, that time will shrink due to the productive interaction of design engineers, test engineers, and manufacturing engineers. Better, development efforts will overlap rather than occur in a progression. So conception to production will



You can often combine test points *by judiciously choosing a resistor network. (Redrawn from "Testability Practices in the 1990s")* take less time in exchange for test and design taking place at once. Not a bad exchange, considering the sacrifice is more of a streamlining than a loss.

While concurrent design is the most promising approach, it may cause cultural upheaval in your company. Changing who works and reports to whom and how product development time is budgeted presents political, social, and economic problems that are beyond the scope of this article. Regardless of these cultural difficulties, talking to your test engineers while you design will help you identify and avoid potential test pitfalls. There are also some tricks that, used judiciously and coupled with careful analysis, can improve the testability of your mixed-signal design.

Partition the design

First, since the digital and analog sub-blocks are often designed separately, partitioning the design and ensuring testability on either side of the interface is important. On the digital side, you can use structured approaches such as scan chains and built-in self-test. On the analog side, ad hoc approaches such as partitioning, providing internal access to individual blocks, and converting analog signals to digital can improve your designs.

The critical part of a mixed-signal design is the interface between the digital and analog circuits, according to Mark Ashton, product marketing manager for scan-based products at Schlumberger Technologies. If you can provide scan-chain access to the interface, you've got control and observation points into and out of both the analog and digital circuits.

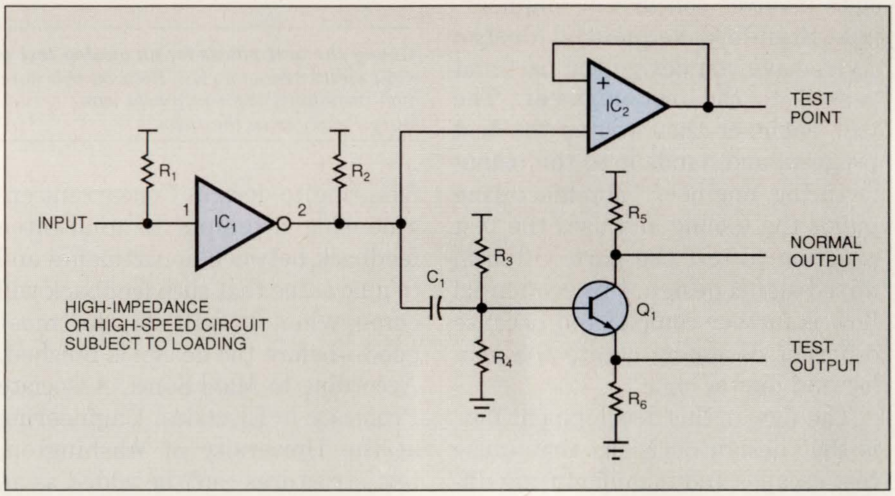
Certainly, having easy access to your analog circuitry at the analog-digital boundary is likely to improve testability, but you shouldn't stop there. Internal access to your analog blocks is also important. Frank Binnendyk, product marketing manager at Mentor Graphics' Simulation and Test Division, suggests that partitioning and providing access to individual analog blocks is also useful as a means of evaluating the entire design.

You can provide this internal access in a number of ways. Analog multiplexers and switches are relatively low-cost—both in performance and silicon—means of measuring and forcing internal voltages and currents.

In a course he teaches on design for testability, Jon Turino, president of Logical Solutions Technology, highlights a number of techniques for improving your ability to observe and control internal nodes. Among these techniques are a few for converting analog signals into digital ones.

Convert your analog signals

The simplest A/D conversion technique—Turino calls it the "Poor man's A/D converter"—uses a comparator to compare a voltage from the analog circuit to an on- or off-chip reference. He also notes an extension to this technique that buffers analog circuitry with DACs on the inputs and ADCs on the outputs. Die-size and pin-count considerations might preclude this technique's practicability. Similarly, you can use voltage-to-frequency and frequency-to-voltage converters to measure digital values from inherently analog circuits.



Buffering a circuit with a voltage-follower operational amplifier *or with an emitter-follower discrete transistor allows you to measure internal signals with minimal impact. (Redrawn from "Testability Practices in the 1990s")*

To maximize silicon utilization, you can share these comparators and converters internally using analog multiplexers and FET switches. These multiplexers and switches can select between numerous inputs. While likely creating the greatest parasitic effects, multiplexing techniques make efficient use of silicon resources.

But these converters, multiplexers, and switches must provide access to the right nodes. Picking analog test points is much like picking test points for digital testing—nodes between blocks, at interface points, and at critical points in the design provide the highest efficacy. Unfortunately, since analog circuits are more sensitive than digital circuits, you must consider potential

Mixed-signal designs

loading problems in your choice of test points. If connecting test equipment to particular nodes might disturb your circuit, add buffers between the node and the test point to isolate the node. Consider using impedance-matching networks when testing high-frequency circuits. Finally, as with your digital circuits, feedback loops greatly complicate testing; use analog switches to break automatic gain and frequency control loops wherever possible.

Jon Turino identifies two other important, common-sense considerations for analog testability. First, make sure the voltage or current levels you're trying to measure are well above the noise of your test equipment. You'll surely get more accurate and reproducible results measuring the 100-mV output of an operational amplifier rather than the 1-mV input.

Make test circuits testable

The second consideration is to remember that if you add circuitry to make your designs testable, these new circuits must also be testable. Test-logic evidence that your internal circuits are bad is only conclusive if you know the test logic is good.

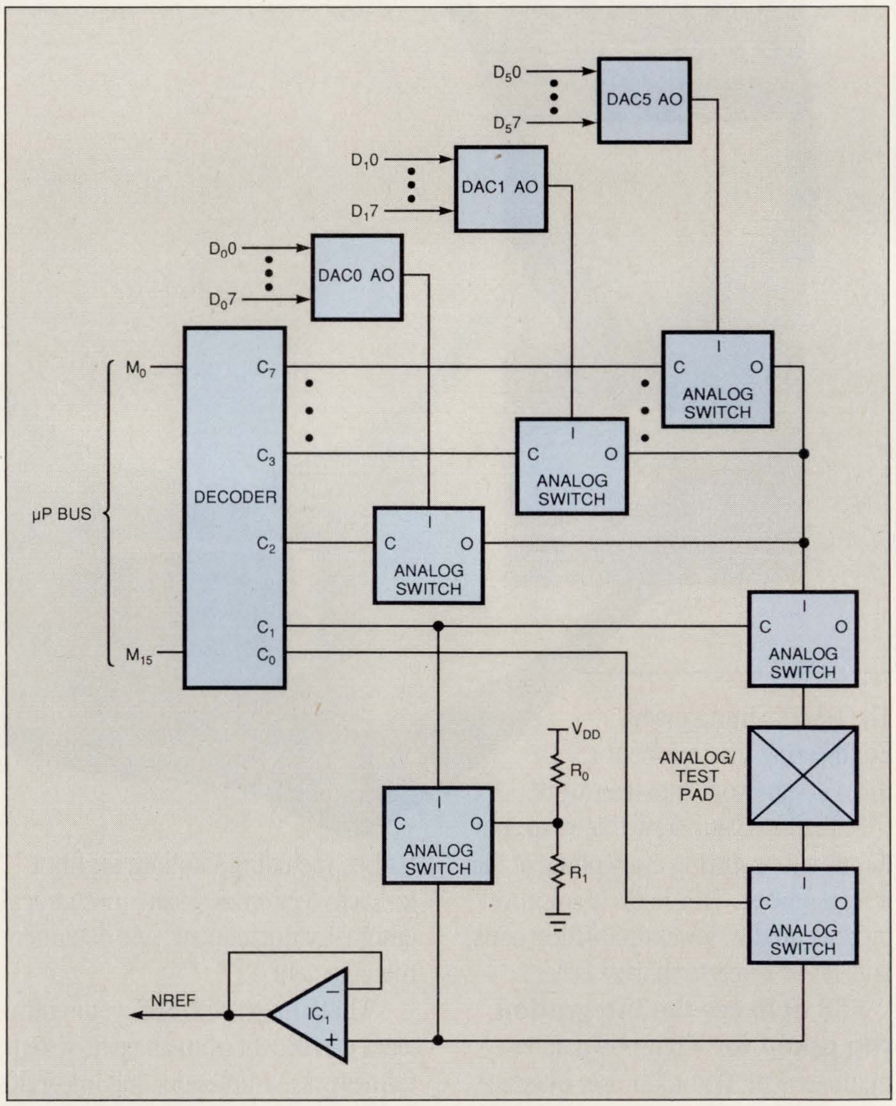
Although the analog side constitutes the major sticking point in testing mixed-signal circuits, enhancements on the digital side, such as scan chains, can help. Scan chains are shift registers whose storage elements are shared with your sequential logic. Under normal circuit operation, you disable the shifting mechanism and the storage elements function as your design requires. In test mode, the storage elements serially shift data through the design. By alternating test and operating modes, you can preset and capture circuit values at embedded points in your design.

Many different versions of scan testability exist. These versions vary clocking schemes and the types of storage elements they allow. (For a more detailed discussion of how to use scan, see **Ref's 1, 2,** and 3.)

Kent Koenig, test manager at NCR, recommends that if your digital circuitry includes a microprocessor bus, you can add an extra register for testing. Using this extra register, you can switch between internal and external references and control the multiplexers and switches.

Concurring with Koenig, Teradyne's Manager of Test Applications, Randy Kramer, also suggests using a microprocessor bus when available. Because digital sections often have higher pin counts than the analog sections, Kramer also finds multiplexing an analog signal onto a digital pin in test mode a convenient and low-impact means of increasing your analog circuit observability.

On the other hand, many CAE



Using a decoder and analog switches in a multiplexing scheme, you might be able to drive an internal analog level as well as test internal analog signals if you've got an appropriately placed I/O pad. (Suggestion courtesy NCR Corp)

Mixed-signal designs

methods for making digital circuits testable require minimal design interference. Such techniques as Crosscheck's embedding test logic; logic-synthesis tools from Dassault Electronique, Racal-Redac, Synopsys, Teradyne EDA, and VLSI Technology/Compass Design Automation inserting scan chains automatically; and Expertest's capacity for creating test patterns for all digital logic almost make digital test a noninvasive operation.

When you've discussed testability considerations and you're ready to lay out your mixed-signal design, Silvar Lisco Product Marketing Manager, Paul DeBelder reminds you to consider where you place digital clock and power lines. These are very noisy and could seriously affect your analog circuitry. You'll also have to provide proper shielding between the analog and digital

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sections. Just as important, make sure you recheck your circuit's behavior with RC data extracted from the circuit layout.

Of course, one complaint of adding testability to designs is its impact on circuit performance. An effort is underway to help you quantify this impact. A number of vendors, including Genrad, Harris, Sierra, and Valid, are building macromodels of specific pieces of test equipment. Last year, Wavetek introduced its XTM integrated into the Digital Equipment Corp Real-Time Test Integrator—a comprehensive set of models that allows you to emulate a complete test setup. These models allow you to build and simulate a model of your circuit, connect it to the appropriate simulated test equipment, and measure its performance.

If you're looking for testability help from your silicon vendor, be aware that the vendor's expertise and interaction with your design efforts vary widely. At one extreme, Analog Devices takes your specification and returns a piece of silicon; they do the design and ensure its testability using many of the techniques discussed herein.

At the other extreme, Orbit Semiconductor doesn't provide design help. You are responsible for creating the design. Its testability is completely dependent on your skill, creativity, and expertise. Orbit provides you with process parameters that you incorporate into your models. The company offers fast (4- to 5-week turnaround), inexpensive (as low as $1500) foundry service, and they suggest that you prototype functional blocks within the design. During fabrication, the company monitors their process, so if a design fails, they can determine whether their fabrication was within specifications.

Many other companies, among them Gould AMI, NCR, and Sierra, assign and provide you with access to their applications and test engineers. These engineers generally have a good understanding of how their organizations test mixed-signal designs. Therefore, they can tell you what they need to test your circuits. They can often help you weigh the impact of testability on your design. EDN

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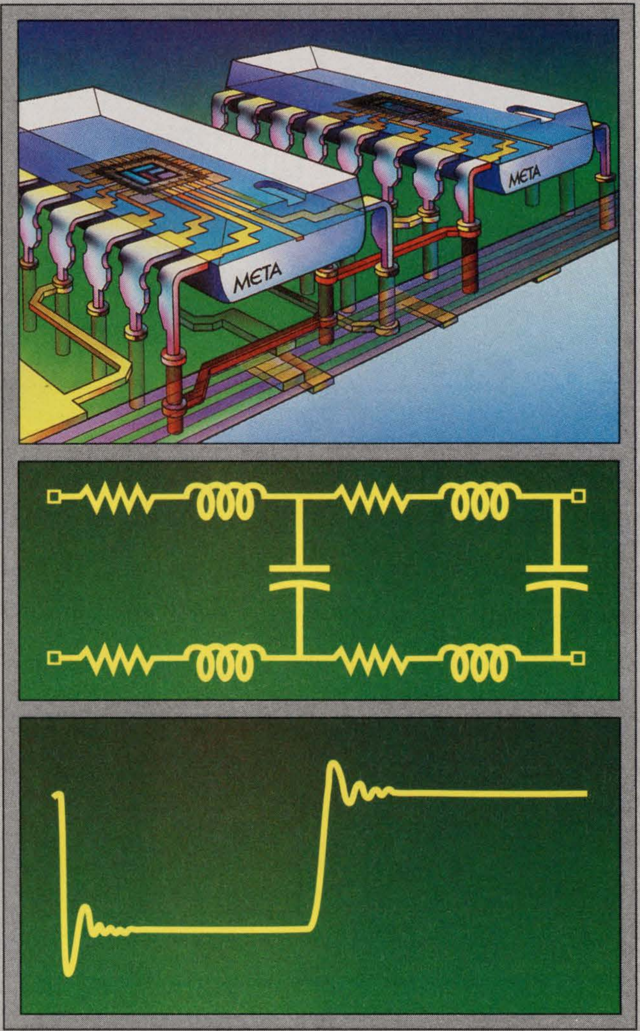

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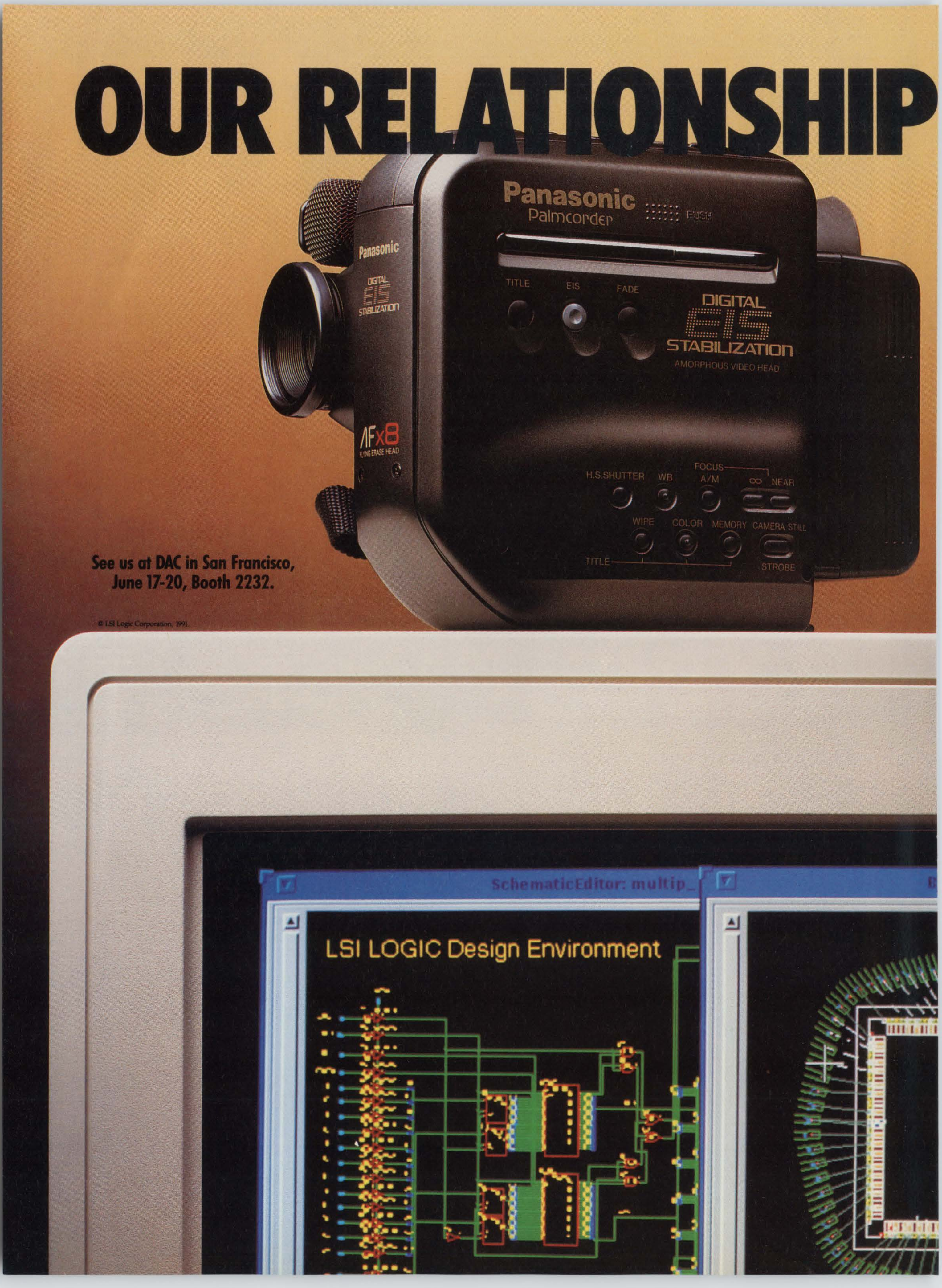
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FREQUENCY AND TIME-INTERVAL ANALYZERS

Units provide insights classic counters can't

Time-measurement instruments aren't restricted to counters and timers anymore. Analyzers that let you visualize long series of measurements can help you troubleshoot problems for which you would never dream of using a conventional counter.

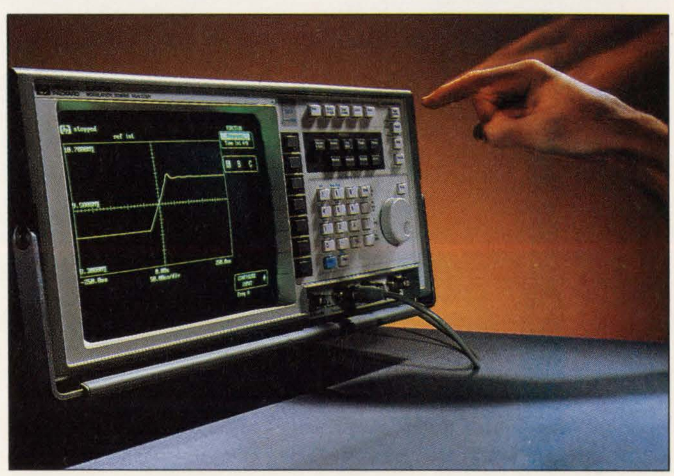
Dan Strassberg, Associate Editor

Time-interval analyzers (TIAs) and frequency and time-interval analyzers (or modulation-domain analyzers) make and store large numbers of measurements with little or no dead time between readings. They then present the measurements in numeric or graphics form, either statistically or in the original time-ordered sequence. Such products first appeared more than a decade ago, but only within the last four years have they been widely promoted. Although they may at first seem to be a cure for a nonexistent disease, the analyzers are, in fact, useful—so useful that many engineering departments, even some that don't own conventional counters, should consider acquiring them.

A related type of product, the time-to-voltage converter (TVC) continuously converts short time intervals to voltage levels that you can monitor on an oscilloscope. The TVC concept is decades old. But, like time-interval analyzers, in the past TVCs were usually specialized devices. For example, some heart-rate monitors used in hospital intensive-care units are based on TVCs. Recently however, Tektronix introduced a TVC designed from the ground up as a general-purpose instrument. This TVC competes with TIAs and frequency-domain analyzers. At $2500, this unit is far and away the lowest-priced continuous-measurement device (**Table 1**). It does need a scope for display and a power supply/enclosure, however.

Another instrument, which at first glance appears to be a conventional counter (in concept, if not in packaging), is actually quite unusual. The IBM PC-based GT-2210S Modulation/Time-Interval Analyzer from Guide Technology can make more than 2000 meaningful measurements per sec. This rate is as much as 200 times the maximum rate of classical counter/timers. So, although the Guide product doesn't make continuous measurements, it makes enough measurements so that you can use it to track rapid changes in frequency or interval duration.

One difficulty that manufacturers of these products have is getting potential users to think about their measurement problems and the instruments' capabili-



What you see on the screen *of this modulation-domain analyzer from HP is not a voltage ramp; it is the change in output frequency of a synthesizer simulating a step change in frequency as best it can.*

ties in appropriate terms. To address that issue, Hewlett-Packard devised the concept of the modulation domain, represented pictorially as follows: Envision a space defined by three axes. Along the X axis is time; along Y is voltage; and along Z is frequency. An oscilloscope is a time-domain instrument; it measures voltage vs time. A spectrum analyzer—a frequency-domain instrument—measures voltage vs frequency. Many TIAs, including HP's frequency and time-interval analyzers, can measure frequency vs time. HP calls the frequency-time (X-Z) plane the modulation domain.

The idea of displaying frequency vs time bothers some people because frequency is defined *in terms of* time, and you can't measure frequency in zero time. Even more vexing is the idea of measuring time intervals vs time. In fact, though, when you compare the values of the dependent variables these instruments record (intervals or waveform periods), with those of the independent variable (time), the de-

Table 1—Representative frequency and time-interval analyzers and time-to-voltage converters[1]

		Maximum frequency		Number of inputs	Timebase stability						Time-ordered readings stored	
					standard		optional					
Vendor	Model	basic unit	with prescaler	(standard/ maximum)	(ppm/ month)	(ppm from 0 to 50°C)	(ppm/ month)	Jitter	Maximum readings (per sec)	Maximum histogram bins	standard	optional
Guide Technology	GT2210S	100 MHz	1.3 GHz	2/2	0.2	5 (0 to 40°C)	0.1	100 psec rms	2300 resolving 100 psec	Via host-PC software	30,000 (640k-byte PC)	See comment
Hewlett-Packard	53310A	200 MHz	2.5 GHz (see comment)	2/3	0.3	8	0.005/	125 psec rms typical	2.5M	450	8000	32,000
	5372A 5373A	500 MHz	2 GHz (see comment)	2/3	0.0005 /day	Oven reference standard	None	150 psec rms	13.3M	2000	8191	N/A
	5371A	500 MHz	See comment	2/2	0.0005 /day	Oven reference standard	None	150 psec rms	10M	125	4096	N/A
International Test Instruments	DTA8850	200 MHz sampled, 20 MHz direct	None	3/3 (2 data; 1 for arming)	1 ppm/ year	0.1	None	As little as 50 psec	1M in 2 sec; 10M in 6 sec	130,000	262,000 periods 131,000 pulse	Double standard memory
Odetics	2001A	25 MHz	None	4/4 (2 data; 1 enable; 1 arming)	100/ year	2/°C	None	1.4 nsec rms 2 nsec p-p	833k at 10-bit resolution	1000	N/A	N/A
	3100	100 MHz	None	5/5 (2 data; 2 control 1 clock)	5/ year	0.025/°C	None	150 psec rms 200 psec p-p	1.3M at 12 bits	4000	N/A	N/A
	4625 CTime	250 MHz	None	2 data; 2 control; gate; clock	0.5/ year	0.01°C	None	88 psec rms 125 psec p-p	30M at 19 bits	4000	16k	64k (Fall '91)
Racal-Dana	2351 2351EMD	250 MHz	None	2/2	1	10 (0 to 60°C)	None	100 psec rms	5M with 200-psec resolution	Depends on software	8191	N/A
Stanford Research Systems	SR620	300 MHz	1.3 GHz	2/2	Note 2	1	Note 3	25 psec rms	Takes 800 μsec + measured interval for one reading	250	250	N/A
Tektronix	TVC 501	2.5 MHz	100 MHz built-in, 1.3 GHz (DP 501)	2/2	25[4]	25[4]	None	30 nsec p-p	2.5M	N/A	N/A	N/A

Notes:
N/A = Not applicable
1. All units from HP, International Test Instruments, and Odetics have built-in graphic displays. The others require external displays. The Stanford Research SR620 can operate as a stand-alone counter, however.
2. Allan variance: $2 \cdot 10^{-10}$ per sec.
3. Allan variance: $5 \cdot 10^{-11}$ per sec; temperature effects: 0.005 ppm from 0 to 50 C.

pendent-variable values are much smaller. Because of these scale differences, the instruments can legitimately plot frequency and time intervals vs time.

Time-interval analyzers had their beginnings in evaluation of spaceborne magnetic-tape data recorders. TIAs are still used extensively for testing of magnetic recording devices (for example, hard-disk drives). The first TIAs, made in the late 1970s by what was then the Kode Division of Odetics, did not maintain a time-ordered record of measurement results; they kept track only of statistical distributions. By keeping track of just the statistics, a TIA could store the results of many more measurements in much less memory at much lower cost than could an instrument that stored time-ordered measurement sequences. Moreover, the statistics provided all of the information the application demanded.

The nearly unrelenting downward spiral of memory prices has played a major role in the growing popularity of TIAs that retain time-ordered measurements. As you might expect, though, such instruments are not gaining acceptance simply because they have become practical. TIAs that store and display time-ordered measurements have many more potential applications than those that only present statistics.

But a time-ordered display is not essential for testing of magnetic recording devices. When testing a device such as a data tape recorder, you can predict its error rate from the width of the distribution of a large number of measurements of the time from a clock edge to the recovery of a 1 or a 0. If the recorder must maintain low error rates under demanding environmental conditions, you can predict its performance by monitoring how the time-interval distributions shift or widen as you vary the ambient temperature or as you subject the recorder to shock and vibration.

Another point in favor of statistical data recording is that by using it, a TIA can accumulate data for much longer than it can record in the time-ordered mode. When an instrument stores time-ordered readings, it places each reading in a separate memory location. The number of such locations is finite, so the analyzer must periodically stop recording to transfer its measurements to a host computer or a mass-storage device. The higher the acquisition rate, the sooner recording must stop.

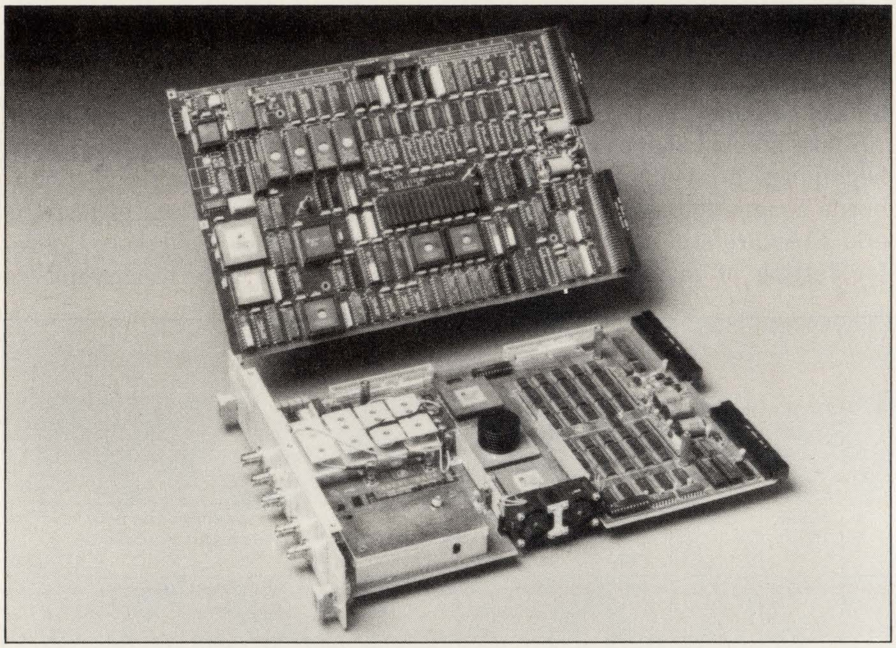
To store data in histogram form, a TIA needs only one location for

US list prices				
base unit	time-base option	extra memory	prescaler	Comments
$2995	$200	Uses host RAM	Included	Plug-in card for IBM PC. Can use more than 640k bytes if present. Makes 1400 measurements/sec at 6-digit resolution.
$9500	$1600	$500	$1450 (2.5 GHz)	All listed H-P analyzers can handle 18 GHz with 5364A prescaler. All measure with zero dead time in all modes.
$30,000 $32,000	Oven standard	N/A	$2150	5372A and 5373A are similar; 5373A makes additional measurements—for example pulse repetition interval and duty cycle.
$24,500	Oven standard	N/A	N/A	As with all the HP analyzers, an IEEE-488 interface is standard on the 5371A.
$25,000	N/A	$3960	N/A	By plugging in a keyboard, you can use the analyzer as an 80286-based PC.
$15,000	N/A	N/A	N/A	Has 10 timebases from 1 nsec to 1 μsec. Sample size selectable from 10^4 to 10^9. Built-in randomizer. See story.
$18,850	N/A	N/A	N/A	Built-in autocalibration. 16 ranges—400 nsec to 4 msec. Trigger delay 4.4 μsec to 440 msec in 16 ranges. Sample size: 1 to 10^{10}.
$15,000	N/A	$2500	N/A	Features similar to 3100, though ranges differ. Memory divides into as many as 128 separately armed, 1-sample to 16k-sample records. Software-selected input impedance.
$14,950 $16,995	N/A	N/A	N/A	C-size VXIbus module. EMD version performs DSP using its own μP and math coprocessor. Transfers data to host at 4M bytes/sec.
$4500	$950	N/A	Standard on both inputs	Finds mean, minimum, maximum, standard deviation, and Allan variance. Has RS-232C parallel, and IEEE-488 ports. Transfers 1400 binary or 150 ASCII responses/sec. D/A outputs permit graphic displays on scopes and chart recorders.
$2500[5]	N/A	N/A	N/A	Time-to-voltage converter. Can use a scope or other graphic device to present output. Because it does not store readings, memory depth does not affect its performance.

4. Timebase stability is specified as 25 ppm as a function of time and temperature but neither the duration nor the temperature range are indicated.
5. Modular unit requires an enclosure/power supply. Prices range from $395 to $795. 1.3 GHz prescaler, $995.

each "bucket" or "bin." Each time a measurement falls in a particular bin, the TIA increments the count in that bin. If the word length of the bins is great enough, a TIA in statistical mode can go on indefinitely making continuous or nearly continuous measurements.

Tektronix emphasizes that because its TVC doesn't *store* readings, it can present time-ordered measurement sequences indefinitely. Although that statement is true, the scope on which you view the TVC's output can display only limited numbers of measurements during its sweep interval; it will miss events that occur during its retrace interval. If you slow the sweep to accommodate more measurements, you will eventually miss transient phenomena of short duration.



A virtue of VXI modules *is their compactness. Thanks to Racal-Dana's 2351, high-resolution frequency and time-interval analysis is part of the repertoire of functions available to system designers working with the compact modular format.*

Newer TIAs generally have extremely high maximum measurement rates: Odetics specifies its 4625 CTime at 30M measurements/sec, and Hewlett-Packard specifies its 5372A and 5373A at 13.3M. However, when time intervals occur in rapid succession as they do in a magnetic recorder, a TIA may not be able to make continuous measurements.

When the analyzer must leave gaps between measurements, a problem akin to aliasing in more conventional sampled-data systems can arise: the analyzer can lock onto measuring intervals of roughly equal duration and thus give an erroneously optimistic picture of the measurement distribution. To prevent this situation, some analyzers incorporate a randomizer, which de-

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Frequency and time-interval analyzers

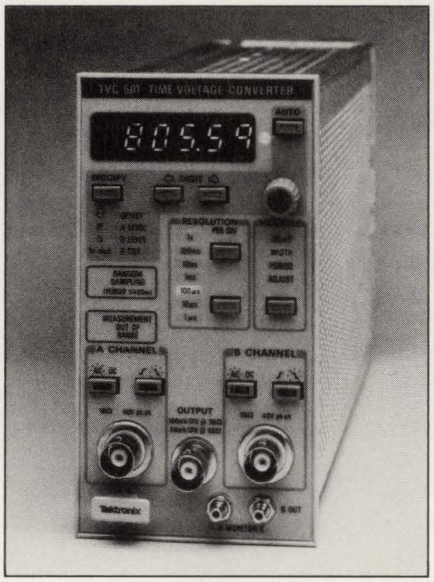
lays the earliest start of successive measurements by a randomly distributed amount.

Word length not the whole story

Most modern TIAs (Odetics' are an exception) show their counter/timer heritage in their long word length. Like nearly all counter/timers, these instruments can make measurements with nominally very high resolution. However, word length is not a good measure of a time-measuring instrument's resolution—especially not its ability to time single-shot events.

Odetics' longest word-length TIA has a 19-bit word, whose least-significant bit is equivalent to 2 ppm of full scale—two counts in the least-significant digit of a 6-digit decimal number. To make up for this relatively short word length, the firm's TIAs have more measurement ranges than most others. Odetics' literature sometimes refers to these ranges as timebases; selecting a different timebase accomplishes much the same thing as changing the sweep speed (timebase) of an oscilloscope. Moreover, just like scopes with a delayed sweep, Odetics analyzers let you delay the start of an interval measurement after a trigger event. The delay can be much longer than the interval represented by a full-scale count.

Don't let the number of digits in a TIA's word length mislead you. When determining the instrument's resolution, the same considerations apply as for counter/timers. The uncertainty in an individual measurement is the result of a rather involved calculation based on various noise sources in the instrument. If



You can use a conventional scope *to display how time intervals vary as a function of time. Tektronix's TVC 501 time-to-voltage converter makes such displays possible. The small module is part of the firm's TM 500 family.*

you insist on a single number to express the repeatability of a time-measurement instrument's readings, look at the jitter spec. However, you ought to carefully read all of the footnotes in the data sheet and learn how to calculate the uncertainty of real measurements.

The best jitter spec quoted for any instrument in **Table 1** is 25 psec rms, for Stanford Research Systems SR620 counter/timer. (Though the SR620 is not a TIA, it is included because of its built-in ability to produce histograms.)

In fact, jitter in TIA readings can often be more significant than jitter in measurements you make with a counter/timer. The reason is that if a counter/timer's readings aren't repeatable enough, you can usually improve the situation by asking the instrument to average a large number of readings. With a TIA, the variations among readings often represent exactly what you are trying to measure. You'd really like the TIA's own uncertainty to be insignificant compared with the variations attributable to the system under test.

In the eye of the beholder

A TIA's method of presenting its acquired data is an important aspect of its operation. Analyzers from HP, International Test Instruments (ITI), and Odetics are stand-alone instruments that don't require additional equipment. These units incorporate displays—CRTs in the HP products, an electroluminescent (EL) panel in the ITI product, and, depending on the model, either a CRT or an EL panel in the Odetics products. The displays can present data in graphical and numeric form. The stand-alone analyzers can also send data to a host computer via IEEE-488 interfaces, RS-232C ports, or both. The ITI unit offers an additional benefit; you can use the instrument as an 80286-based PC.

The other products require external displays. The Tektronix TVC works with any scope. The Guide Technology unit, which is based on an IBM PC bus I/O board, uses the computer's display. The Racal Dana units are C-size plug-ins for the VXIbus; they use the host computer's display. The Stanford Research unit is a stand-alone counter. It can send its graphics output to a scope, a plotter, or a chart recorder. You need such an external device to take advantage of the instrument's TIA-like qualities, though you need no external equipment to use it as a counter.

TIAs, particularly those with a time-ordered presentation, are wonderful general-purpose instruments. Several vendors have compiled stacks of application notes describing the diverse ways in which you can use these products. For example, HP has a 2-in.-thick stack of more than two dozen notes covering applications in fields as varied as disk-drive testing; development of secure-communications, cellular-radio and radar systems; and design of motion-control systems. Tektronix publishes a book (**Ref 1**) that describes more than a score of uses for its TVC, including several in embedded-system debugging.

TIAs in embedded-system debug

Space limitations don't permit detailed descriptions of many of these applications. Tektronix's embedded-system debugging examples, however, show that the ways in which you can use a TIA are limited mainly by your imagination. As you might expect from the supplier of an instrument that produces a time-ordered display, Tektronix has chosen examples that emphasize the value of such a presentation over a statistical one.

A problem frequently encountered in embedded real-time systems is unpredictable interrupt-response time, or interrupt latency. There are many ways to look at interrupt latency, but a TVC or a TIA that produces a time-ordered display allows you to quickly see how interrupt latency varies with time. The instrument measures the time from the falling edge of the processor's interrupt-request (IRQ) line to the appearance on the address bus of the starting address of the interrupt-service routine. A word-recognizer probe generates a trigger when it senses the desired address. (For even greater rigor, you can further qualify the address with the trailing edge of the memory-read strobe.)

If the interrupt latency sometimes exceeds specifications, you can try to correlate the failures with such events as the line-voltage zero crossing. In this example, you can display the line voltage on an unused scope channel.

Time-interval analyzers and modulation-domain analyzers will ultimately change the way engineers view the measurement of frequency and time. In this ever more digital world, frequency and time are growing in importance as measures of system performance. In an increasingly fast-paced environment, these variables are not static. In a sense, conventional counters and timers have failed to keep pace with the dynamic nature of the quantities they measure. Instruments of the types discussed here have corrected that anachronism. In the months and years ahead, you can expect new and intensified competition among vendors of these units. With it, not surprisingly, will come higher performance and lower prices. EDN

Reference

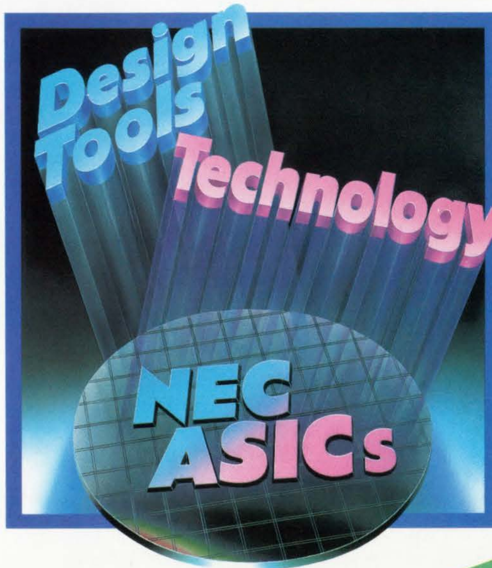
1. Tektronix Inc, *"TVC 501 applications brochure and data sheet,"* Beaverton, OR, 1990.

Article Interest Quotient
(Circle One)
High 500 Medium 501 Low 502

C&C Computers and Communications

CB-C7

High Integration Level Cell-Based ASIC Technology



Systems on Silicon

Fast Turnaround Options

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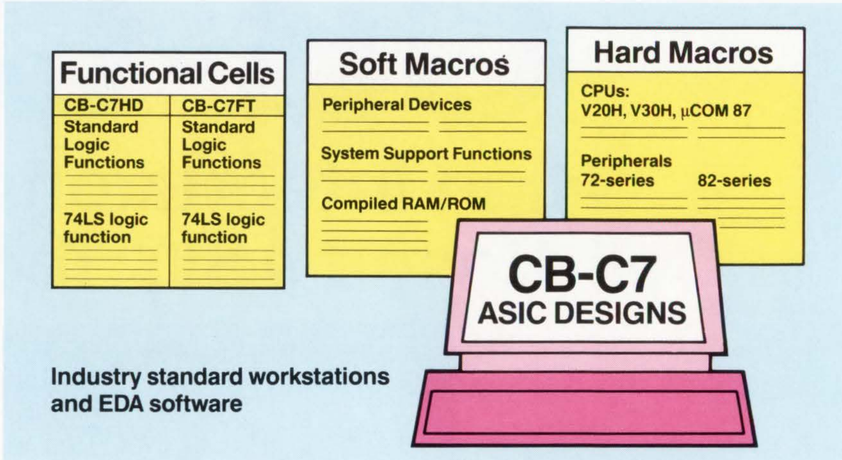

Mega function block Libraries - key to system integration

NEC's CB-C7 megafunction block-libraries cover all your likely integration requirements – from the simple logic elements which glue your system together, right up to the high-level functions which provide your designs with on-chip intelligence.

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CB-C7 ASICs utilize an advanced CMOS process technology which features 0.8μm gate lengths. This technology achieves internal gate delays of only 0.44 nsec and power gate delays of 0.34 nsec (fan-out = 2, wire length = 2mm)

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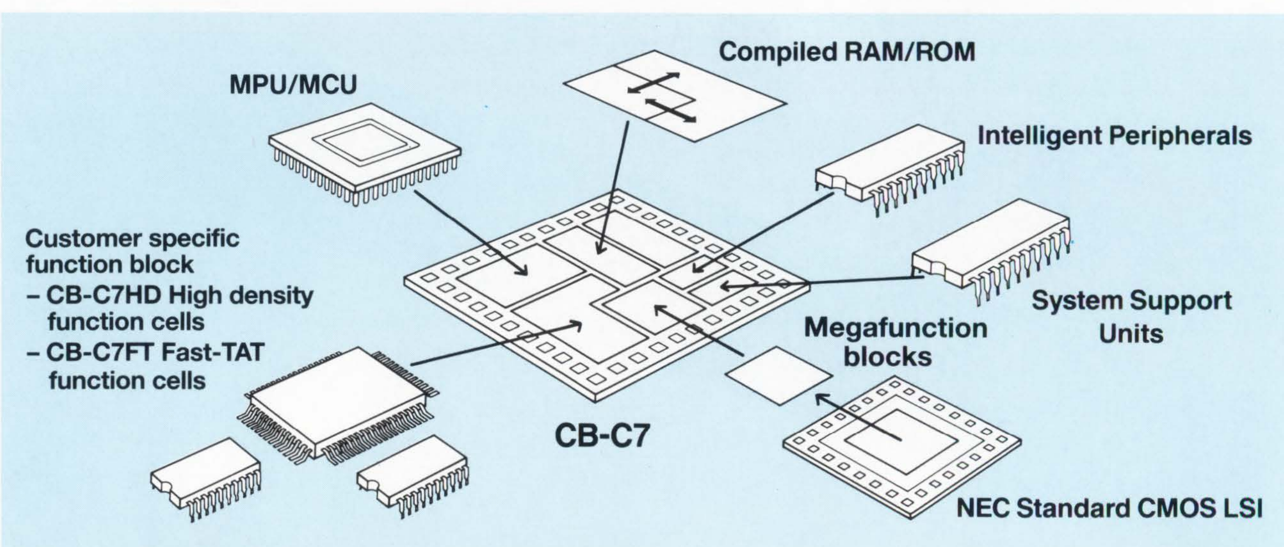

Solving Cost/Turnaround Trade-offs

Fast turnaround and low unit price are often conflicting requirements when it comes to implementing your ASIC designs – the first suggesting the use of a gate array solution, and the second dictating a standard cell approach. NEC's CB-C7 ASIC technology solves these cost/turnaround trade-offs – with combined gate-array/standard-cell solutions for fast turnaround, and full standard-cell implementations for low unit cost.

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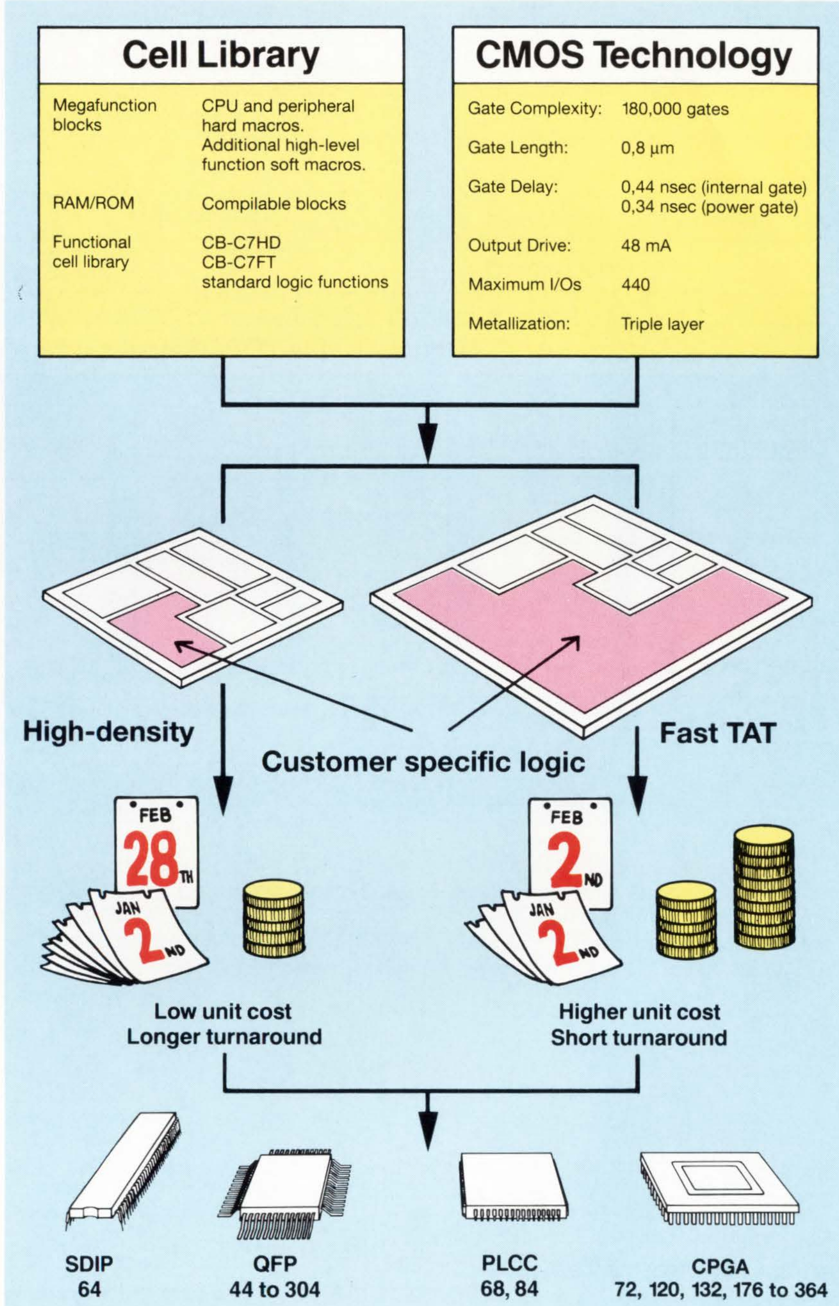

High Performance ASICs and Packages

Both the fast turnaround and low unit cost versions of CB-C7 ASICs feature the same high performance - so there are no compromises with either solution.

To match this performance, we have an equally impressive range of packages in which to house them. You can choose between conventional plastic DIPs, quad flat-packs, PLCCs and high pin-count plastic or ceramic pin-grid arrays. NEC's state-of-the-art packaging technology provides CB-C7 ASICs with maximum protection from their environment, ensuring their long-term reliability.

OpenCAD – flexibility in design

NEC OpenCAD gives you maximum freedom in the CB-C7 design process. Freedom to perform schematic capture using popular EDA software such as DAZIX, Mentor, Valid and VIEWlogic, on industry standard workstations from DEC, HP-Apollo, IBM and SUN.

After schematic capture, your design is completed by compiling RAM/ROM blocks and optimizing user-defined logic. It is then floor-planned using ChipPlan, simulated with System Hilo or Verilog, and placed and routed using Cell-3 Ensemble. After post-layout simulation and design-rule checks, we pass pattern generation data to one of our wafer fabrication facilities in Japan, the USA or Europe.

To simplify your design task, logic optimization, simulation, and chip layout are normally carried out by a NEC ASIC design center on their SUN or DEC workstations. Providing access to NEC's Unified Design Environment – a suite of ASIC design tools which operate under DEC PowerFrame system management software – these workstations ensure a simple user interface and smooth data flow from one design process to the next.

However, OpenCAD also gives you the flexibility to install part or all of the NEC Unified Design Environment on your own system, so that you can perform as much, or as little, of the CB-C7 design process as you choose.

NEC Unified Design Environment - A Framework for Right-First-Time Designs

To handle the complexity of CB-C7 ASICs, and that of our next generation of ASIC technologies, we have taken some of the best ASIC design packages in the industry – such as VIEWlogic schematic capture software, Synopsys HDL compilers and logic synthesizers, Genrad System Hilo, and Cadence simulation, layout and routing software – and integrated them into the NEC Unified Design Environment.

At the heart of this design system lies the NEC Central Unified ASIC Database – a technology independent database which allows us to automatically generate new simulation models as new process technologies are introduced.

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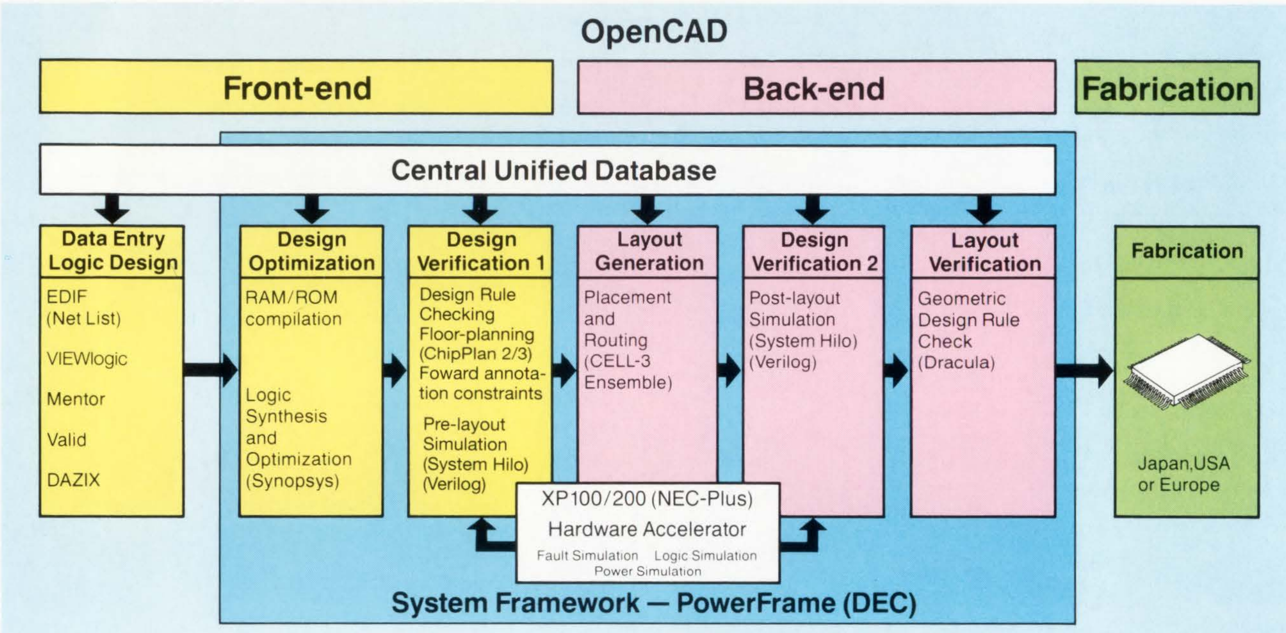

Wherever you are in the world, there is a NEC design center close enough to support you in CB-C7 ASIC design. If you are already using industry standard workstations and EDA software to design ASICs, you probably have all the hardware and software design tools you will need. Simply install the CB-C7 ASIC libraries, and you can start on a CB-C7 design tomorrow.

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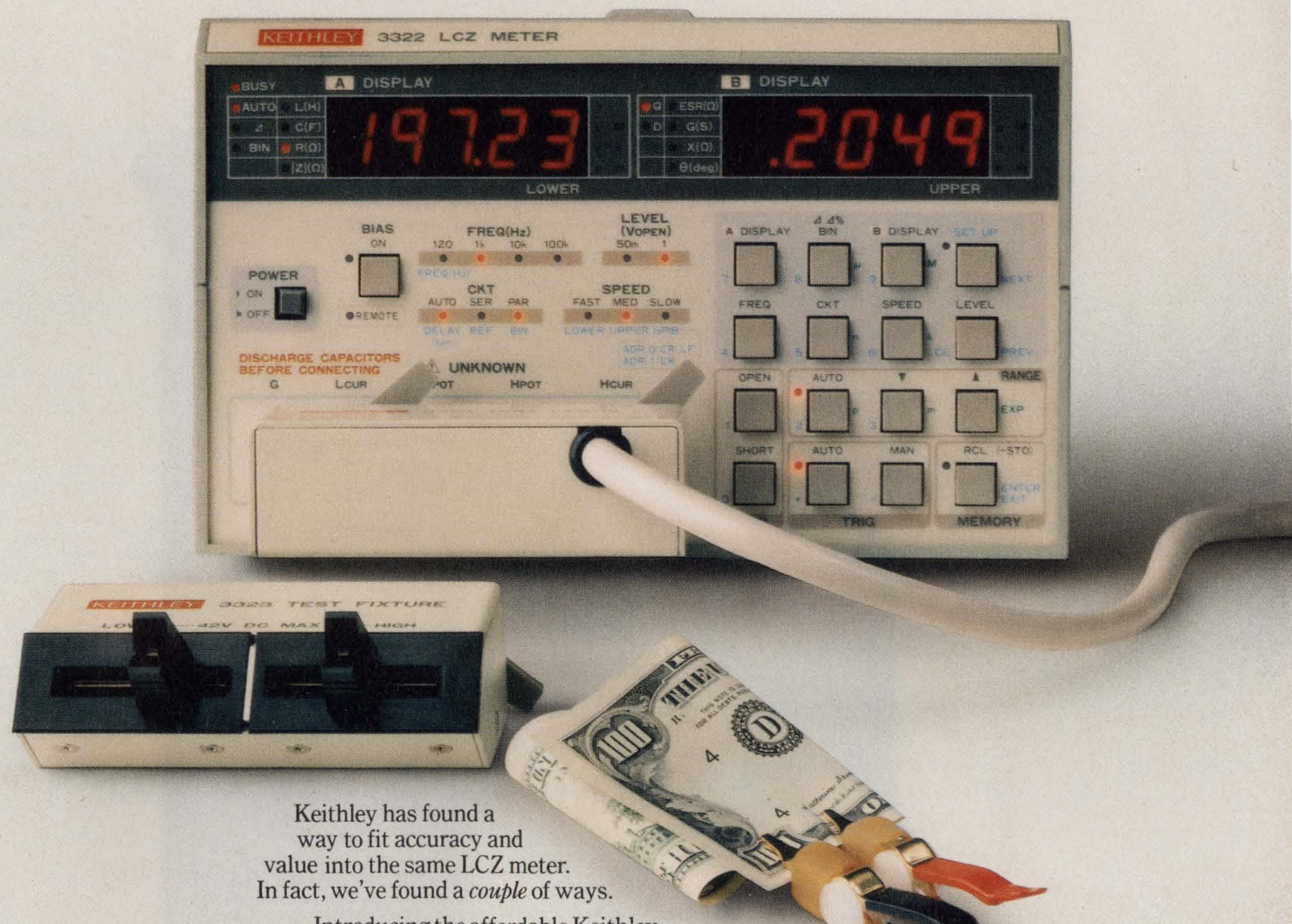

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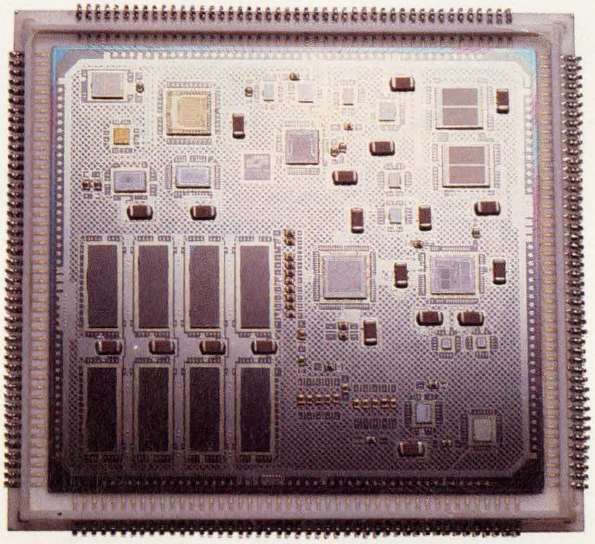

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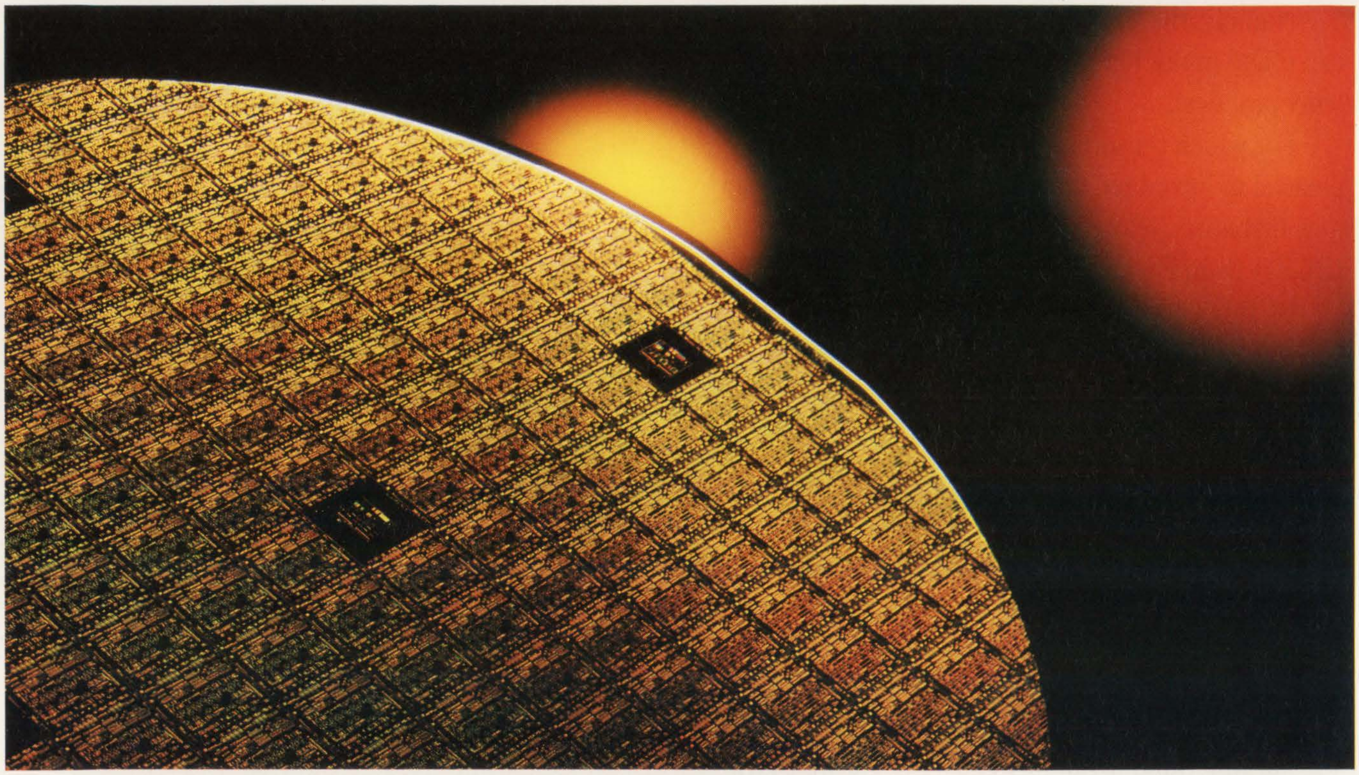


LEARNING ADA

Class provides fast track to understanding

Given enough time and the right motivation, most engineers can learn to use the Ada programming language on their own. However, a training class will hasten language proficiency.

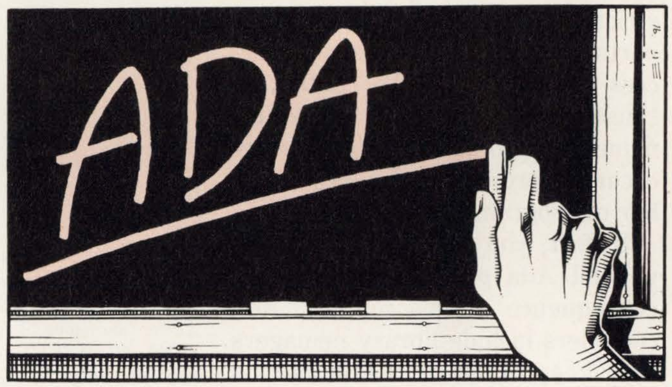
Steven H Leibson,
Senior Regional Editor

If you work on military projects for the Department of Defense, your time has just run out. The US government's fiscal year 1991 budget states that "After June 1, 1991, where cost effective, all Department of Defense software shall be written in the programming language Ada." Thus, you must now prove that another language would be cheaper to use if you wish to avoid using Ada for a military programming project.

Ada's features suit the language for complex programming projects, but its reputation of being hard to learn discourages many engineers from learning it. To find out just how hard learning Ada really is, I attended a 5-day real-time Ada programming class at Alsys in Burlington, MA. (Alsys is not the only compiler vendor to offer classes in Ada programming. I selected this class because its timing suited my needs.) I discovered that learning Ada as a second language isn't as tough as people say. Although Ada is a complex language, it isn't impossibly difficult to learn. In fact, the language actually eases the job of writing programs for multitasking systems.

Although I'd never programmed in Ada before, I have assimilated many other programming languages including Algol 68 (a structured language and a predecessor of Ada that nearly drove me away from computers forever), Basic, HPL (a proprietary Hewlett-Packard programming language for desktop computers), and several microprocessor assembly languages. My familiarity with these programming languages matches the experiences of many engineers who know the general concepts of computer programming but lack specific Ada knowledge.

Dr Benjamin M Brosgol taught the class. His 3-part series on real-time Ada programming appeared in EDN last year (**Refs 1, 2, and 3**). He was a member of one of the four teams that competed on the original Ada specification.



Eli Gerber

Brosgol taught not only Ada's syntax, but imparted the reasoning behind the language's features. That kind of information helps you make better use of a programming language, especially one as complex as Ada.

The first part of the class focused on the structure of an Ada program. An Ada program consists of many "program units." The main program, one such unit, is a procedure that uses the services of "subprograms," which can be functions or procedures. Subprograms are also program units. Each program unit comprises two parts. The first part, the optional "specification," declares the elements of the program unit that are visible to other units. The second part is the body code.

Divide and conquer

Ada's definition requires that an Ada compiler be able to compile a program unit consisting of just a specification. Thus, you can write a specification for a program unit in Ada, compile it so that other subprograms can use it, and postpone implementing that module until a later time. You can then write and compile the code that performs the subprogram's real work separately.

This compartmentalization lets you conceal a subprogram's implementation, its "body," from the other subprograms. This characteristic thus limits the number of details a programmer must remember at any one time by severely restricting access to and from other parts of the program. Restricted access also prevents the conflicting reuse of variables and procedure names—a problem that frequently occurs on projects with a large number of programmers.

In fact, you can separately compile all Ada program units. As a consequence of this feature, Ada compilers include library managers that keep track of the numerous program units, variables (which Ada calls objects), and procedure names that make up a complete program. **Fig 1** gives you a glimpse of the complexity you can expect from even small programs. Ada programs don't have to be so complex. **Fig 2** demonstrates that an Ada program can be as short as five lines.

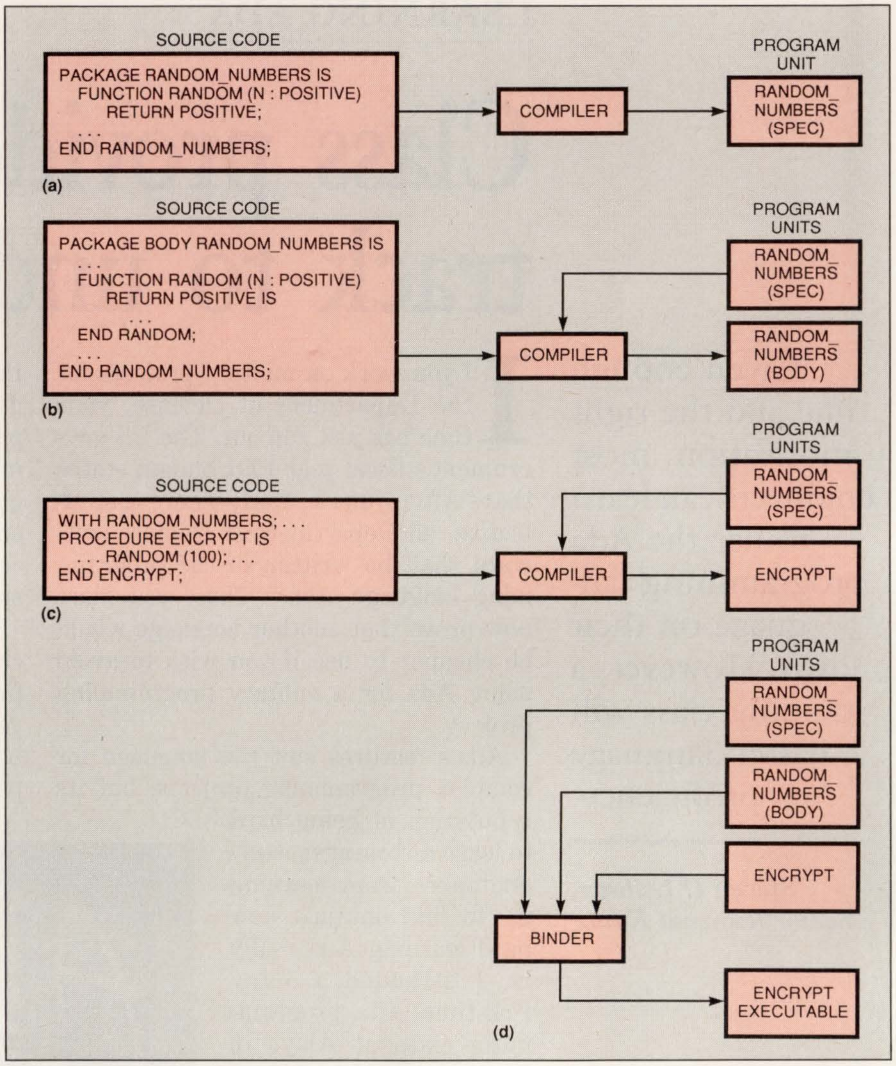


Fig 1—You can construct an Ada program *by using several modules, or program units, which the Ada development environment saves in a library. In this example, the Ada package RANDOM_NUMBERS consists of distinct specification units and body program units. These two types of units are compiled separately in **a** and **b**. The compiler uses the RANDOM_NUMBERS spec unit to compile the RANDOM_NUMBERS body in **b**. The compiler requires only the RANDOM_NUMBERS spec to compile the main program, ENCRYPT, in **c**. The binder (a linker and librarian rolled into one tool) uses all three compiled program units to create an executable file **(d)**.*

I found the idea of a program comprising tens or hundreds of program units somewhat daunting. All the languages I know well don't allow separate compilation, so this concept was somewhat new to me. As I grew more familiar with Ada, I became accustomed to this programming style and now understand why many vendors stress the abilities of their products' library-management tools. Such tools are essential if you want to take full advantage of Ada's features.

From generalities, the class moved on to the specifics of writing an Ada program. As a first step, you declare all the objects you plan to use. You can declare objects in both the specification and the body of a program. Because Ada has strong typing and constraint checking, you must declare all objects before you use them. Other subprograms can use the objects you declare in the specification unless you declare those objects private. If you declare an object in a subprogram's body, it is private to that unit.

When you declare an object, you must also declare its "type." For example, if you are going to use an object called DAY to hold the day of the month in your program, you might declare DAY to be an integer. However, the day of the month can never be negative, and if DAY somehow became negative during your program's execution, that situation would constitute an error. Instead, declare DAY as a "positive," which is a predefined subset of the integer type that includes the set of integers greater than zero.

Using constraint

To make full use of Ada's error-checking abilities, you could use Ada's user-defined subtype declaration to further limit DAY's value to the integers 1 through 31 inclusive. If you defined DAY as such a subtype, then every time you assigned a value to DAY, Ada would check to make sure that the assigned value fell within the limits of that object's definition. This continual constraint checking is one of the strongest of Ada's type-checking abilities because it enhances a program's reliability.

Further, you cannot use sleazy programming tricks, such as assigning the value of a floating-point number to an integer type, because Ada doesn't allow such shenanigans. Other languages may allow such "cheating" and their programming styles may sometimes produce more-efficient-looking code, but such languages exact a penalty from anyone trying to maintain your program.

Ada provides explicit ways to convert a floating-point number to an integer. Because the conversion must be explicit, anyone reading your program will be able to see what you are doing. Remember, Ada's designers were building a language for large projects and big programming teams. They always opted for stylistic clarity and shunned obscurity.

```
with TEXT_IO; use TEXT_IO;

procedure TEST1 is

begin

   PUT_LINE("Hello, world!");  -- this is the traditional first program

end TEST1;
```

Fig 2—A simple Ada program *need not look complex, as this 5-line listing demonstrates.*

For the remainder of the first day's lessons, we looked at simple Ada statements such as assignments, *if* statements, *case* statements, and loop structures. We also studied the two types of subprograms: functions and procedures. Functions return an explicit value. Procedures do not return a value to the caller but may indirectly return values by changing the value of global objects.

As part of its emphasis on constrained programming, Ada also places limitations on subprograms' parameters. Parameter modes help you limit vulnerability to inadvertent modification. You can define the mode of a passed parameter as *in*, *out*, or *in out*. A subprogram can read the value of an *in* parameter but cannot change that parameter's value. A subprogram can change the value of an *out* parameter but cannot read its value. And a subprogram can both read and change a parameter you define as *in out*.

Struggling through day one

I was overwhelmed by the time the instructor turned us loose on our PCs for the first day's workshop problems. The concepts I had to simultaneously assimilate included Ada terminology, the quirky syntax, several unfamiliar program and data structures, and the language's stylistic philosophy. I was also learning to use Ada tools, including an editor, verifier, compiler, binder (a linker and librarian rolled into one tool), and a debugger.

Had I realized the sheer volume of information I would need to assimilate that first day of class, I might have studied Ada before class started. The text for the course **(Ref 4)** would have been a helpful study aid. Of course, if I had the time to read that book, I might not have felt the need to take the course in the first place.

The second day of class was less of a struggle. I began to recognize proper Ada syntax and found reading program listings easier. We started the day by looking at "generics," Ada's rough equivalent to programming macros. Generics are templates for creating subprograms. One example of a useful Ada generic is the sort routine.

Suppose you develop an efficient algorithm to sort objects. Instead of writing separate subprograms to sort lists of integers, fixed-point numbers, floating-point numbers, and strings, you can write one generic for that algorithm that sorts objects of an unspecified type. Later, you can specify the object type to be sorted when you instantiate the generic. This Ada feature helps you reuse the code you write.

Next, we studied complex objects: arrays and records. Arrays are homogeneous collections of objects; records are collections of heterogeneous objects. Most programming languages have similar kinds of data structures. Ada allows "discriminated" records that have variable fields. You can use a record's discriminator field to determine the number and types of fields in the rest of the record (**Fig 3**). This feature is a great way to efficiently organize the memory a program uses for records.

Ada's access types may seem somewhat foreign unless you're familiar with the C programming language's pointers. Access types point to objects and thus contain the address of the object to which they point. However, you generally don't use access types to work directly with machine addresses. Instead, you use an access type to manipulate an object's component parts by tacking the object's component names onto the access-type designator.

An example helps clear up the confusing terminology and illustrate the reasons for using access types. Suppose you declare a designator REF as an access type for record R, which has two components: objects VALUE and NEXT. The VALUE component holds a numeric value; NEXT holds a pointer to the next record. You typically use this kind of data structure to create linked lists. If you want to manipulate a linked list of these records using many different Ada subprograms, you could have problems.

Without access types, Ada's scoping rules (the rules that define which objects a subprogram can use) might cause the Ada runtime system to pass the entire linked list to each relevant subprogram. That operation would create a new copy of the set of records somewhere in memory for every subprogram that uses the records in the list. If the objects you're working with are large, multiple copies could cause your system to run out of memory and abort the program.

An access designator such as REF lets the subprogram manipulate the original set of objects or, in this case, records. Using Ada's "dot notation," the subprogram can manipulate a record's value component using the designation REF.VALUE. The subprogram finds the next record on the list by reading REF.NEXT.

Note that this scheme preserves Ada's type-checking feature because REF.VALUE has the same type as VALUE, and REF.NEXT is the same type as NEXT. Access types for complex objects can get pretty involved, and I can't say that I fully understand them yet, but the class certainly gave me a good start on the subject.

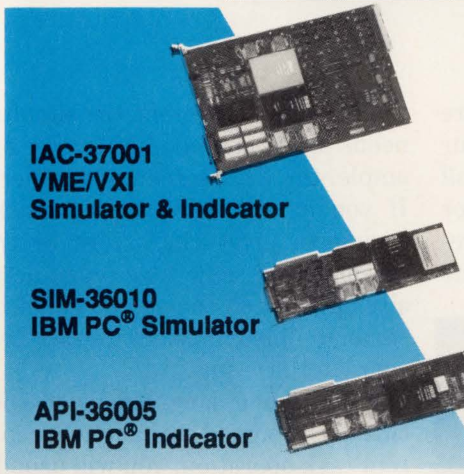
I hit a brick wall during the discussion of recursion in Ada not because of Ada but because I'm just not conversant enough with the basic concepts of recursion. As another class member said, "My mind doesn't work that way." I did learn enough to know that if I ever figure out how to effectively use recursion in any programming language, I'll be able to use Ada to write recursive programs.

At the end of the day's lecture, we studied storage management, because access types make allocating memory difficult for the runtime system. Temporary objects exist only as long as the tasks using them exist. If you use access types to reference temporary objects, the runtime system may not be able to determine when you no longer need those objects and therefore might be unable to reclaim the memory the objects use. You can explicitly reclaim that memory by using Ada's "unchecked deallocation" feature. Through unchecked deallocation,

```
package RESERVATIONS_DATABASE is

   subtype SMALL_NATURAL is NATURAL range 1..3;

   type CLASS_TYPE is (FIRST_CLASS, COACH);

   type SPECIAL_SERVICE_TYPE is (MASSAGE, HOT_TUB);

   type MEAL_TYPE is (SNAKE_SURPRISE, UNKNOWN_DEAD_ANIMAL, FILET_OF_SHOE);

   type PASSENGER_TYPE ( NAME_LENGTH : SMALL_NATURAL := 0;
                 CLASS         : CLASS_TYPE    := COACH ) is
     record

     NAME : STRING(1..NAME_LENGTH);
     case CLASS is

        when FIRST_CLASS =>
           FIRST_CLASS_ROW_NUMBER  : INTEGER range 1..3;
           FIRST_CLASS_SEAT_NUMBER : INTEGER range 1..10;
           SPECIAL_SERVICE         : SPECIAL_SERVICE_TYPE;

        when COACH =>
           COACH_ROW_NUMBER  : INTEGER range 4..30;
           COACH_SEAT_NUMBER : INTEGER range 1..10;
           MEAL              : MEAL_TYPE;

     end case;

     end record;

end RESERVATIONS_DATABASE;
```

Fig 3—Discriminated records let you compact *the fields in a record. The discriminating field CLASS specifies whether the remaining portion of the record contains row-number, seat-number, and special-service fields or row-number, seat-number, and meal-type fields. Ada's constraint checking will generate an exception if your program tries to assign a first-class row number to a coach-class field.*

SYNCHRO PRODUCT UPDATE



New Generation Instruments on Cards Offer both Angle Indicator and Simulator Functions

IAC-37001 is a VME/VXI register based Synchro/Resolver Angle Indicator and Simulator on a single size "C" Card. The card performs separate S/D and D/S operations simultaneously.

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API-36005 is a full size IBM PC® card containing a single-channel, wideband, instrumentation grade Synchro/Resolver Angle Position Indicator. Offering programmable resolution of 16 or 20 bits, accuracy of 18 arc seconds and an operating frequency range of 360 to 5000Hz, it is ideal as a stand alone Indicator in an engineering lab or PC based Automatic Test Equipment (ATE).

SIM-36010 is a full size IBM PC® card containing a single-channel, wideband, high-accuracy Synchro/Resolver Simulator. The instrument accepts an external reference and provides an output signal of 11.8, 26, or 90V L-L with a drive capability of 1.5VA. The SIM-36010 also includes a programmable dynamic rate feature.

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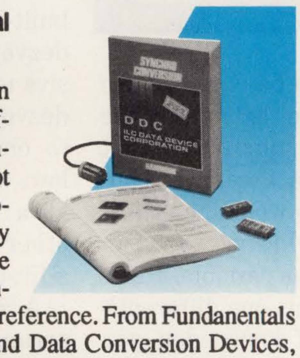
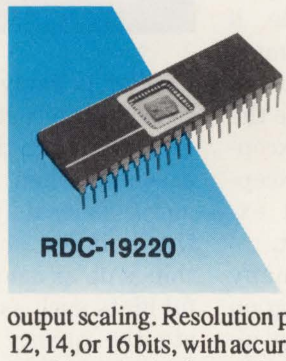
DDC Handbook Offers Tutorial on Synchro Conversion



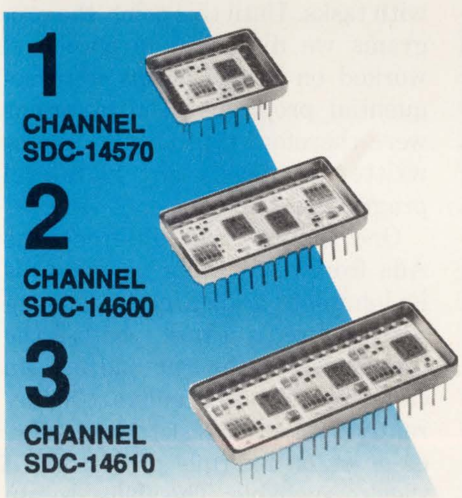
DDC's "Synchro Conversion Handbook" is once again being offered, free of charge, to design engineers. The handbook covers not only DDC's approach on the subject but also all the other generally accepted techniques in use throughout the industry. It continues to be a popular treatise and reference. From Fundanentals of Angle-Sensing Transducers and Data Conversion Devices, through Theory of Operation, Measuring and Computing Performance Parameters, and concluding with Design Constraints and Selection Criteria for Typical Applications, the Handbook is thorough in presenting a wealth of useful, factual information.

Programmable 16 Bit Monolithic R/D Converter



The RDC-19220 series are low-cost, versatile, programmable monolithic Resolver-(and LVDT)-to-Digital Converters. These converters are available in small 28 pin DDIP, 40 pin DDIP, or 44 pin PLCC packages and offer programmable features such as resolution, bandwidth, and velocity output scaling. Resolution programming allows selection of 10, 12, 14, or 16 bits, with accuracies of 2.3 arc minutes. This feature combines the high tracking rate of a 10 bit converter with the precision of a 16 bit device in a single package. Typical applications include motor control, robotics, machine tool, and process control.

New Generation S/D Converters with Tach-Quality Velocity Output



A new generation of one, two, and three channel Synchro- or Resolver-to-Digital converters lead the way based on a single-chip monolithic. These completely self-contained synchro converters are housed in hermetically sealed packages with an area requirement as low as 0.5 square inches per channel.

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Circle 126 for Sales Contact   CIRCLE NO. 118   Circle 127 for Literature you can explicitly force the Ada runtime executive to delete an object from memory.

I found the second day's workshop problems on discriminated records and unchecked deallocation to be fairly easy. I skipped the problems that demonstrated recursion.

Making exceptions

We started the third day of class by looking at exception handling. An Ada runtime system can raise several exceptions while your program is running. For example, if an assignment statement attempts to assign an improper value to an object, that operation will cause the runtime system to raise an exception. If you do not write an exception-handling routine for that exception, your program will halt.

Halting may not cause many problems for a program running on a PC or workstation—you can always restart the program. But real-time, embedded programs generally can't afford to halt because some sort of physical damage may result. If your Ada program is managing control surfaces on an aircraft, you don't want that program to halt on its own.

You can generate user-defined exceptions from within a program by using Ada's *raise* statement. The *raise* statement causes program execution to jump to the named exception-handling routine. You should not use the *raise* statement for normal program branching, however, because the program cannot return to the point at which the exception was raised. Exceptions in Ada are just that: exceptional situations. You should use them only when you need to abort one instruction sequence and immediately start another.

The instructor also discussed "exception etiquette," which included tips that help programs stay operational even when exceptions occur. For example, if a hardware failure or storage exception occurs, your exception handler should close all open files and reclaim storage for objects no longer needed before relinquishing program control. The handler is likely to be closer to the scope of the routine that caused the exception than the subprogram that executes when the exception handler finishes its job would be. Thus, the handler should try to clean things up as much as possible. Helpful hints such as this one differentiate the quality of knowledge you can get in a class from what you can read on your own.

Ada's continual checking of an objects' constraints enchances a program's reliability.

After a more involved look at generics, we moved on to the real-time aspects of Ada. We started with tasks. Until this point, the programs we discussed in class and worked on in workshops were sequential programs. The programs were therefore typical of programs written in nearly any high-level programming language.

One feature that differentiates Ada from many other languages is its inherent parallelism. By labeling a procedure as a task, you tell the compiler that the runtime system can run that procedure concurrently with other tasks on one processor or on multiple processors, if they're available. The ability to run subprograms concurrently resides in the Ada runtime executive supplied with the compiler.

If you're already familiar with multitasking environments, you know that one of the biggest problems to solve in multitasking systems is how to prevent the simultaneous use of shared objects. For example, the CRT screen is an object. If you have two concurrent tasks trying to print characters to the screen at the same time, what actually appears on the screen could be some jumbled mixture of the two character streams.

When using languages not specifically designed to handle concurrent task operation, you will usually create a semaphore to control access to shared objects. Ada has a built-in mechanism called the "rendezvous" to ensure mutually exclusive use of shared objects. The rendezvous uses a simple mechanism to ensure mutual exclusion: It allows only one caller to be served at a time. The server serves all other calling tasks one at a time on a first-come, first-served basis.

A rendezvous is an asymmetric arrangement between the calling and called tasks. The calling (or client) tasks issue a call to the task with which they wish to rendezvous. The called (or server) task has an *accept* statement that creates an "entry" for the clients. If the client task issues a call before the server task executes its *accept* statement, the Ada runtime executive suspends the caller until the rendezvous occurs. Similarly, if the server task executes an *accept* statement first, the runtime executive suspends the server until a client issues a call. Note that *accept* statements are not caller specific, whereas clients issue server-specific calls.

When at least one client and the server are ready, the rendezvous occurs. A rendezvous situation in which multiple clients call one server causes an implicit semaphore. The semaphore occurs because the server accepts only one call at a time and will not service another client until the server executes another *accept* statement.

If you write your program so that

the server task alone can manipulate a protected object, then all other subprograms (and programmers) must observe the implicit semaphore of the rendezvous. Misused semaphores, a problem in many multitasking programs, are thus rare when using Ada.

The rendezvous does have one potential drawback: execution speed. Depending on the compiler, the μP, and the clock rate, a rendezvous may take tens or hundreds of microseconds to execute—even when both the client and server tasks are ready. A compiler vendor can tell you how long a rendezvous takes using that company's compiler and a particular hardware configuration. You must then decide if your application can afford that much time. For many real-time applications, even a 100-μsec rendezvous isn't too long. However, some applications can't afford to waste that amount of time.

We investigated Ada tasking during the third day's workshop problems. One problem created two tasks that sent characters to the PC's screen simultaneously. Without using a rendezvous to protect the screen, we did indeed observe jumbled output. By adding a screen-server task to provide mutual exclusion for other tasks, we produced more orderly behavior. Despite Ada's reputation as a verbose language, I found that I could create programs that demonstrated complex Ada concepts with a page or two of code. For example, the three program units for the screen-printing task appear in **Fig 4.**

On the fourth day, the instructor discussed more-advanced methods for using tasks. For example, conditional, or "guarded," *accept* statements let you control which rendezvous calls a server task will accept. For example, a guarded *accept* statement might be available for rendezvous calls only if parameter x equals zero. Server tasks can have multiple *accept* statements, and you can guard all or just some of them.

When executing, your program will evaluate the guarded statements first and then ignore all *accept* statements with closed guards.

(a)

```
package LINE_PCKG is
   procedure PUT_UC_LINE (ITEM : in STRING);
   procedure PUT_LC_LINE (ITEM : in STRING);
end LINE_PCKG;
```

(b)

```
with TEXT_IO;
use TEXT_IO;
package body LINE_PCKG is

   task MONITOR is
      entry PUT_UC_LINE(ITEM: in STRING);
      entry PUT_LC_LINE(ITEM: in STRING);
   end MONITOR;

   task body MONITOR is

      MAX_LENGTH : constant := 80;
      LINE  : STRING(1..MAX_LENGTH);
      INDEX : NATURAL;
      CHAR_CODE, UC_CHAR_CODE, LC_CHAR_CODE : NATURAL;

      procedure MOVE (FROM: in STRING; TO : out STRING; LAST : out NATURAL) is
      LOCAL_LAST : NATURAL;
      begin
         if FROM'LENGTH <= TO'LENGTH then
            TO := (TO'RANGE => ' ');
            LOCAL_LAST := TO'FIRST+FROM'LENGTH-1;
            TO(TO'FIRST..LOCAL_LAST) := FROM;
      else
            TO := FROM(FROM'FIRST..FROM'FIRST+TO'LENGTH-1);
            LOCAL_LAST := TO'LAST;
      end if;
      LAST := LOCAL_LAST;
      end MOVE;

   begin
      loop
      select
         accept PUT_UC_LINE(ITEM: in STRING) do
           MOVE(FROM=> ITEM, TO=> LINE, LAST => INDEX);
         end PUT_UC_LINE;
            for I in LINE'FIRST..INDEX loop
               if LINE (I) not in 'a' .. 'z' then
            PUT (LINE (I)); -- no conversion needed
            else
                  CHAR_CODE := CHARACTER'POS (LINE (I));
            UC_CHAR_CODE := CHAR_CODE - 32;
                  PUT (CHARACTER'VAL (UC_CHAR_CODE));
            end if;
         end loop;
         NEW_LINE;
      or
         accept PUT_LC_LINE(ITEM: in STRING) do
           MOVE(FROM=> ITEM, TO=> LINE, LAST => INDEX);
         end PUT_LC_LINE;
           for I in LINE'FIRST..INDEX loop
              if LINE (I) not in 'A' .. 'Z' then
            PUT (LINE (I)); -- no conversion needed
            else
                  CHAR_CODE := CHARACTER'POS (LINE (I));
            LC_CHAR_CODE := CHAR_CODE + 32;
                  PUT (CHARACTER'VAL (LC_CHAR_CODE));
            end if;
         end loop;
         NEW_LINE;
      end select;
      end loop;
   end MONITOR;

   procedure PUT_UC_LINE (ITEM : in STRING) is
   begin
      MONITOR.PUT_UC_LINE(ITEM);
   end PUT_UC_LINE;

   procedure PUT_LC_LINE (ITEM : in STRING) is
   begin
      MONITOR.PUT_LC_LINE(ITEM);
   end PUT_LC_LINE;
end LINE_PCKG;
```

(c)

```
with LINE_PCKG;
use LINE_PCKG;
procedure SYNMON is
   task T1;
   task T2;

   task body T1 is
   begin
      for I in 1 .. 200 loop
         PUT_UC_LINE ("abcdefghijklm01234");
      end loop;
   end T1;

   task body T2 is
   begin
      for I in 1 .. 200 loop
         PUT_LC_LINE ("NOPQRSTUVWXYZ56789");
      end loop;
   end T2;
begin
   null;
end SYNMON;
```

Fig 4—A server task can provide mutually exclusive access *to protected objects. The task MONITOR prevents the lines of characters that tasks T1 and T2 generate from intermixing on a display screen.*

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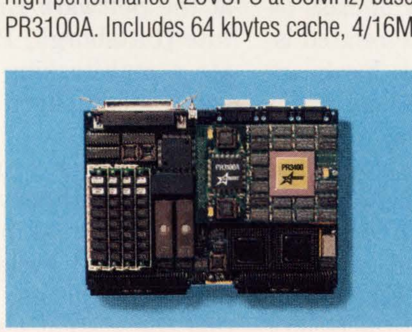

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CIRCLE NO. 131

Learning Ada

The remaining open-guarded and unguarded *accept* statements are available for rendezvous calls. After one such rendezvous is accepted and completed, the program will reevaluate the guards.

When writing the code for a server task, you need to take care to minimize the amount of suspension time for the calling tasks. You can place a server task's code within the rendezvous, where it is protected, or outside the rendezvous. Placing as much of the server task's code outside the rendezvous as possible minimizes the duration of the rendezvous and thus reduces the amount of time the calling task will be suspended.

Complex structures such as rendezvous calls make Ada seem very much removed from the underlying hardware, but the language also has features that let you directly manipulate the hardware. For example, representation clauses let you specify how the compiler should organize objects at the bit level. If you need to specify the addresses and the exact bit-by-bit definition of a peripheral chip's control and status registers, you use representation clauses.

The fifth and last day of class focused on more hardware-related issues. Ada lets you link hardware interrupts to tasks. The interrupt works like a call to a server task from a client task, but has higher priority than any other Ada task. Because Ada is a high-level language, you may not find Ada-level routines to be the best solution for servicing interrupts, but the facility exists. Ada compilers from different vendors handle interrupts differently, so you need to study the technical specifications to discover how each compiler handles interrupts.

Because Ada handles interrupts as if they were task-entry calls, you can test interrupt-handling tasks without using hardware interrupts. Another task can just as easily rendezvous with the interrupt-handler's entry. You may find this feature handy for testing your interrupt code before you have target hardware or if you do not have enough hardware test beds for all of your programmers.

Ada has a built-in mechanism called the "rendezvous" to ensure mutually exclusive use of shared objects.

You can also use interrupts to simulate interrupt situations that may be too difficult or dangerous to test otherwise. For example, if you want to see how your reactor-control software responds to a coolant-leak interrupt, you probably won't want to actually create such a leak for your test during the early stages of software development.

We spent most of the last day discussing rate-monotonic scheduling theory. (**Ref** 5). This theory, most recently developed by Lui Sha at the Software Engineering Institute (Pittsburgh, PA), lets you create a multitasking system that always meets hard periodic deadlines.

Essentially, rate-monotonic scheduling theory states that if your multitasking system has enough CPU cycles to service all periodic requests, you can assure that the system services all the requests in the time required by assigning the highest priority to the task with the shortest period and the lowest priority to the task with the longest period. Tasks with intermediate periods receive intermediate priorities inversely proportional to their periods.

The discussion of rate-monotonic scheduling concluded the real-time Ada course. Five days of immersion in the language have not made me an expert Ada programmer. However, I did not attend this class to become an expert on Ada's syntax. Instead, I wanted to know why the language incorporated some of its unique features and how to best exploit these features in real-time systems. I now have an excellent foundation to further develop my Ada programming skills. EDN

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Acknowledgment

For more information about this class, contact Alsys Inc at 67 S Bedford St, Burlington, MA 01803, phone (617) 270-0030, FAX (617) 270-6882.

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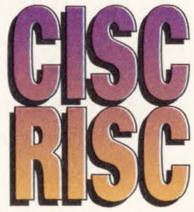

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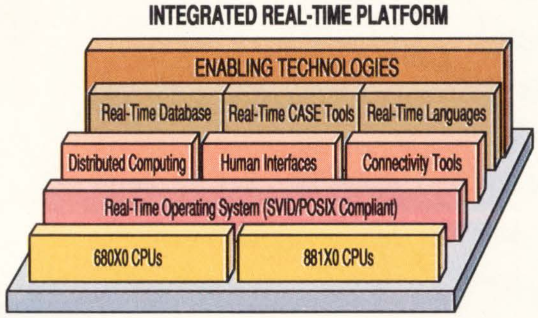

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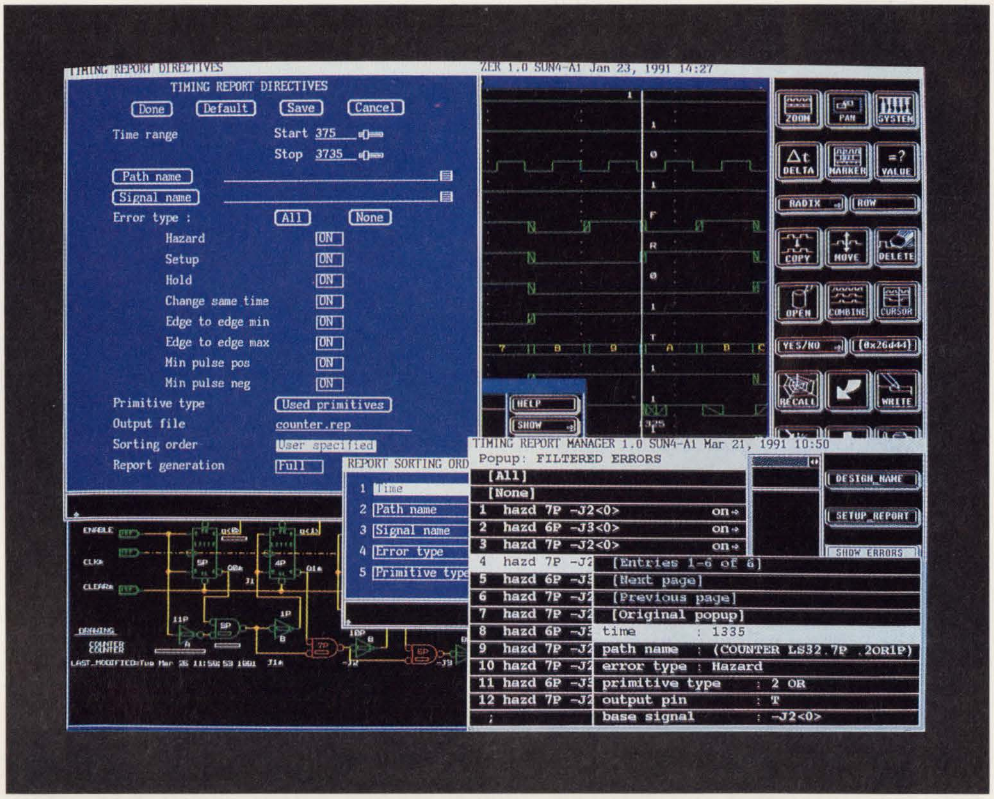
The performance of devices on the same integrated circuit generally correlate with temperature, voltage, and process. As a result, it is unlikely that the propagation delays through one gate on an IC will be at its maximum while the delay through another gate on the same IC will be at its minimum. The Rapidtime simulator allows you to "package" devices in your timing simulation so their performance correlates.



__Because the dynamic timing analyzer__ and schematic-capture tools are tightly integrated, you can use the analysis output to graphically locate timing violations on the schematic.

Without this correlation, timing results wouldn't be realistic. Designing your circuit to account for one path through a string of gates operating at minimum specification while another path operates at maximum specification would be too conservative.

The dynamic timing analyzer uses the same simulation patterns that you use to drive the Rapidsim logic simulator. As a member of the vendor's simulation tool suite, the analyzer shares libraries and a user interface with both the logic simulator and a fault simulator. Integration within the suite also allows you to back-annotate layout-dependent timing information from the vendor's own Allegro pc board and Compose and Construct IC layout tools.

The vendor's claim that each member of the tool suite uses the same "simulator engine" is misleading. Each tool uses its own independent event queue and algorithm to perform logic, timing, and fault analysis. Where the tools do converge is in reading the same netlist, eliminating the need for translating data between tools.

The results-file output from the timing analyzer, like the other tools, is also linked to the front-end schematic-capture tools. Rather than sorting through a mountain of confusing error or timing-violation logs, the timing analyzer gives you the option of highlighting errors within your schematic, though this option doesn't extend to VHDL source code. This graphical capability aids debugging. You can also sort the violations by time of occurrence, error type (setup, hold time, pulse width), signal name, or path name.

The simulation suite offers 140 ASIC-vendor-supplied design libraries whose models include all the information for timing analysis. Within Rapidtime, you can scale the timing data in the models to experiment with different design margins. You can also use the LM1000 hardware-modeling system within the simulation runs.

The software runs on Sun, DEC, and IBM workstations as a network sharable resource and costs \$20,000. The Logic Workbench costs \$7000.

—Michael C Markowitz

Valid Logic Systems, 2820 Orchard Pkwy, San Jose, CA 95134. Phone (408) 432-9400. FAX (408) 432-9430. TLX 3719004.

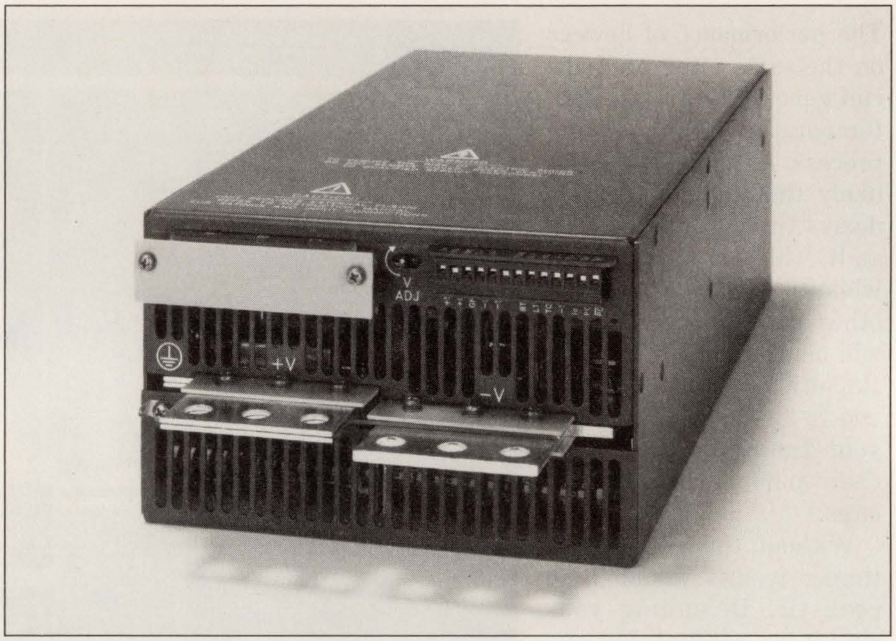
Circle No. 732

Modular switching power supply develops an 1100 A output

Housed in a package measuring 5×8×16 in., LFS-52 Series switching power supplies range to 1100A. The units employ a modular design consisting of three full-bridge circuits that switch at 100 kHz. A 1.22-MHz crystal oscillator provides the logic-level timing signals that switch the three modules 120° out of phase. The series includes three models—the LFS-52-2, which has an output of 1.8 to 3.3V at 1100A, the LFS-52-5, which has an output of 4.5 to 6V at 1000A, and the LFS-52-8, which has 5.5 to 8V at 800A output. These output values equate to a power density of 10W/in^3.

Each of the modules in the LFS-52 series supplies is wired in a redundant configuration. If one driver fails, the supply will continue to deliver two-thirds of its rated output power indefinitely. To further ensure full internal redundancy, each module has separate fuses; these fuses guarantee that any defective module will be invisible to the remaining modules. The 2V models have a guaranteed minimum efficiency of 70%; minimum efficiency figures for the 5 and 8V models are 75 and 80%, respectively.

Control circuitry in the supplies is referenced to the secondary side of the supply. This design removes the isolation boundary from the feedback loop. The supplies employ an average-current control scheme, allowing for accurate load sharing from supply to supply. A transformer-coupled gate-drive scheme switches the high-power MOSFETs that are incorporated in the inverter modules. Supply input is 3-phase and does not require bulk-storage capacitors. As a result, the units have a 0.9 minimum power factor.



Featuring a 10 W/in.^{3} power density, *the LFS-52 Series of switching power supplies comprises three models, each model measuring 5×8×16 in.*

The supplies feature a 2-stage differential filter on the output. Individual module output chokes feed into a common capacitor assembly and through a second-stage filter. To address common-mode considerations, the supplies include free-standing input-rectifier and inverter-switch heat sinks to minimize capacitance-to-chassis figures. A shield located between the primary and secondary windings of the main transformer has a low-inductive connection to the input film capacitors, which shorts out the primary-to-secondary interwinding capacitance. The first-stage output-filter chokes are located on the negative leg of the output bus structure. This design holds the output bus assembly at a fixed potential relative to ground, thus keeping secondary-to-chassis currents to a minimum.

Supply-line regulation equals 0.1% for line variations of 170 to 265V ac. Load regulation measures 0.1% for 0-to-100% load variations. Transient response time equals 4 msec, and thermal coefficient is 0.03%/°C. The units feature an air-flow sensor that provides thermal protection in the event of inadequate air velocity. Fixed-electronic-current limiting clamps output current to 107% of 40°C rated current. Overvoltage protection is standard on all units. When the preset voltage level is exceeded, the protection circuitry removes the inverter drive. A dc-power-good indicator LED goes off to indicate that a power failure has occurred. The LFS-52 Series is priced from $2800.—***Tom Ormond***

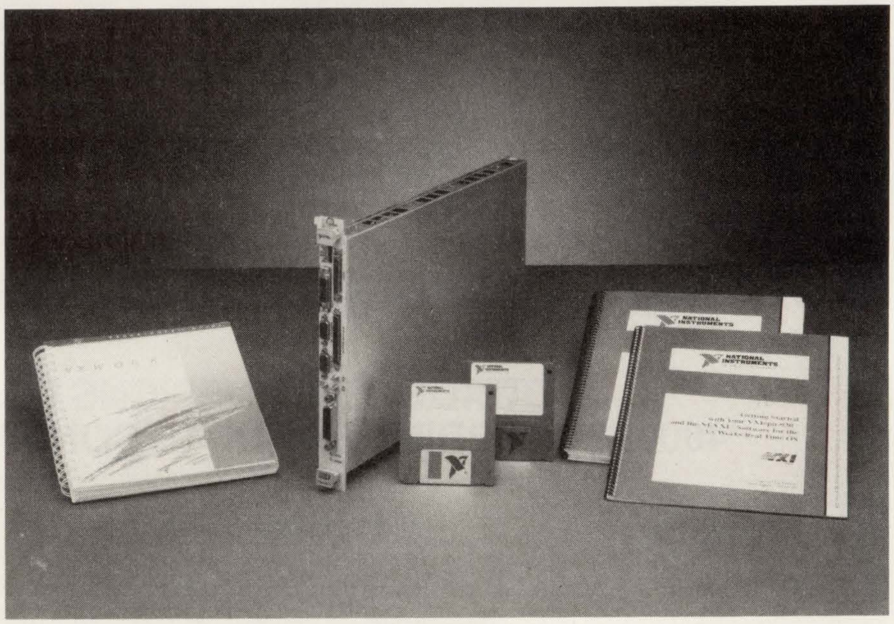
Lambda Electronics Inc, 515 Broad Hollow Rd, Melville, NY 11747. Phone (516) 694-4200. FAX (516) 293-0519.

Circle No. 730

68030-based VXIbus controller offers real-time, distributed operation

The VXIcpu-030 C-size 68030-based board comes with VXI and IEEE-488 drivers and an integrated Ethernet connector; it's suitable for real-time embedded applications that require VXIbus control. Using this Slot-0 controller board, you can build distributed VXIbus systems that network VXIbus mainframes with workstations, PCs, file servers, and terminals. This single-slot board gives you direct control of VXIbus registers, memory, interrupts, and triggers. You can also configure the board for non-Slot-0 operation.

A SCSI port, an IEEE-488 connector, and two serial ports are standard features on the board. Options include eight additional serial ports, an internal hard-disk drive, and a 68882 floating-point coprocessor. The heart of the controller is a Motorola MVME147 single-board VME computer with a 25-MHz 68030 µP. You can populate the MVME147 with as much as 16M bytes of RAM and 4M bytes of ROM.



***Complete with Ethernet, SCSI, VXIbus, and IEEE-488 ports,** the VXIcpu-030 controller board from National Instruments lets you develop embedded applications that can network VXIbus mainframes with other computers and terminals.*

The controller is also a fully functioning VXI message-based commander with complete Resource-Manager capability and direct access to all VXI address spaces. You can use it to perform 8-, 16-, and 32-bit data transfers. Onboard RAM is dual-ported to the VXIbus for direct shared-memory communication.

Wind River Systems sells a version of its Vxworks real-time operating system that has been optimized for use with the controller. Using its built-in X-Window server facilities, this operating system lets you use a Unix workstation or a PC as a high-level software development platform; the platform generates real-time code that executes on the controller's target processor.

Development tools that come with Vxworks include libraries for both VXIbus and IEEE-488 instrument control. The VXI driver software includes a resource manager; functions for word serial communications; direct access to the VXI bus; interrupt and signal handling; and trigger handling.

You can edit, compile, link, and debug your real-time application software on your Unix host computer via a local terminal on the controller itself. By downloading portions of your application code to the embedded processor, you can interactively set breakpoints to trace program execution. This software also lets you examine variables, memory, and register locations.

Pricing for the controller board begins at $5995 for a base unit with 2M bytes of RAM. You'll pay an additional $1595 for National Instruments' software-development libraries and $400 for a runtime license. The Vxworks development system for the controller board sells for $20,000; its runtime license costs $600.—***JD Mosley***

National Instruments, 6504 Bridge Point Pkwy, Austin, TX 78730. Phone in US and Canada, (800) 433-3488; in TX, (512) 794-0100. FAX (512) 794-8411.

Circle No. 733

Wind River Systems Inc, 1010 Atlantic Ave, Alameda, CA 94501. Phone (800) 545-9463; in CA, (415) 748-4100. FAX (415) 814-2011.

Circle No. 734

SBus-based DSP board performs 33M flops

The TMS320C30-based Spirit-30 DSP board adds 33M-flops math performance to SBus-based computers from Sun Microsystems and other manufacturers. You can use the board in applications such as image processing, communications, and vibration analysis. The board can transfer data to or from the host computer as fast as 25M bytes/sec and can interrupt the host via any one of the seven SBus interrupts.

An SBus-based host computer can reset, interrupt, enable, disable, and read status information from the Spirit-30. The board can accommodate 256k to 2M bytes of zero-wait-state static RAM that is mapped into the host computer's address space. An additional 32k bytes of static RAM connect directly to the expansion bus of the TMS320C30. You can use this private memory to store frequently accessed coefficients.

Dual proprietary parallel ports interface the math board to additional memory and peripheral devices. The first port, dubbed ASM-Peripheral Port, supports 32M-byte/sec transfer rates to data-acquisition devices such as frame grabbers. The second port, the ASM-Main Port, transfers data as fast as 66M bytes/sec. You can use the ASM-Main Port to expand memory to 64M bytes and to link multiple boards in a daisy-chain fashion.

The board also includes two serial ports that can operate as fast as 8M bits/sec. You can connect standard RS-232C devices to the ports. And, the company can supply a number of data-acquisition modules that connect via the serial ports. You can choose from modules with 12- to 16-bit resolution and sampling rates ranging from 8 to 400 kHz. The board also offers compatibility with the industry-standard DT-Connect expansion bus.

You can choose from an array of software-development tools for the board, including an optimizing ANSI-C compiler, assembler, and linker. The company also offers a C-language source-level debugger, a simulator, and a DSPL library of DSP algorithms. You can buy the Spox OS real-time operating system for the board.

A Spirit-30 board configured with 256k bytes of static RAM costs $3995. The SBus board is compatible with Spirit-30 products for other types of computers, such as IBM-compatible PCs. You can port software to any of the boards by recompiling and relinking the source code.—***Maury Wright***

Sonitech International Inc, 14 Mica Ln, Suite 208, Wellesley, MA 02181. Phone (617) 235-6824. FAX (617) 235-2531. **Circle No. 731**

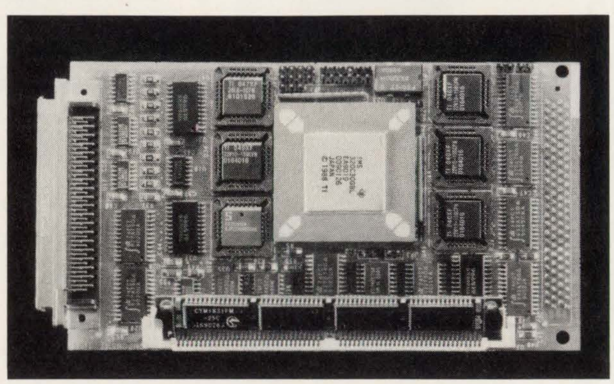


Image-processing, vibration-analysis, radar, and other DSP application programs *execute at 33M flops on Sun SPARCstations and other SBus-based systems equipped with a Spirit-30 board.*

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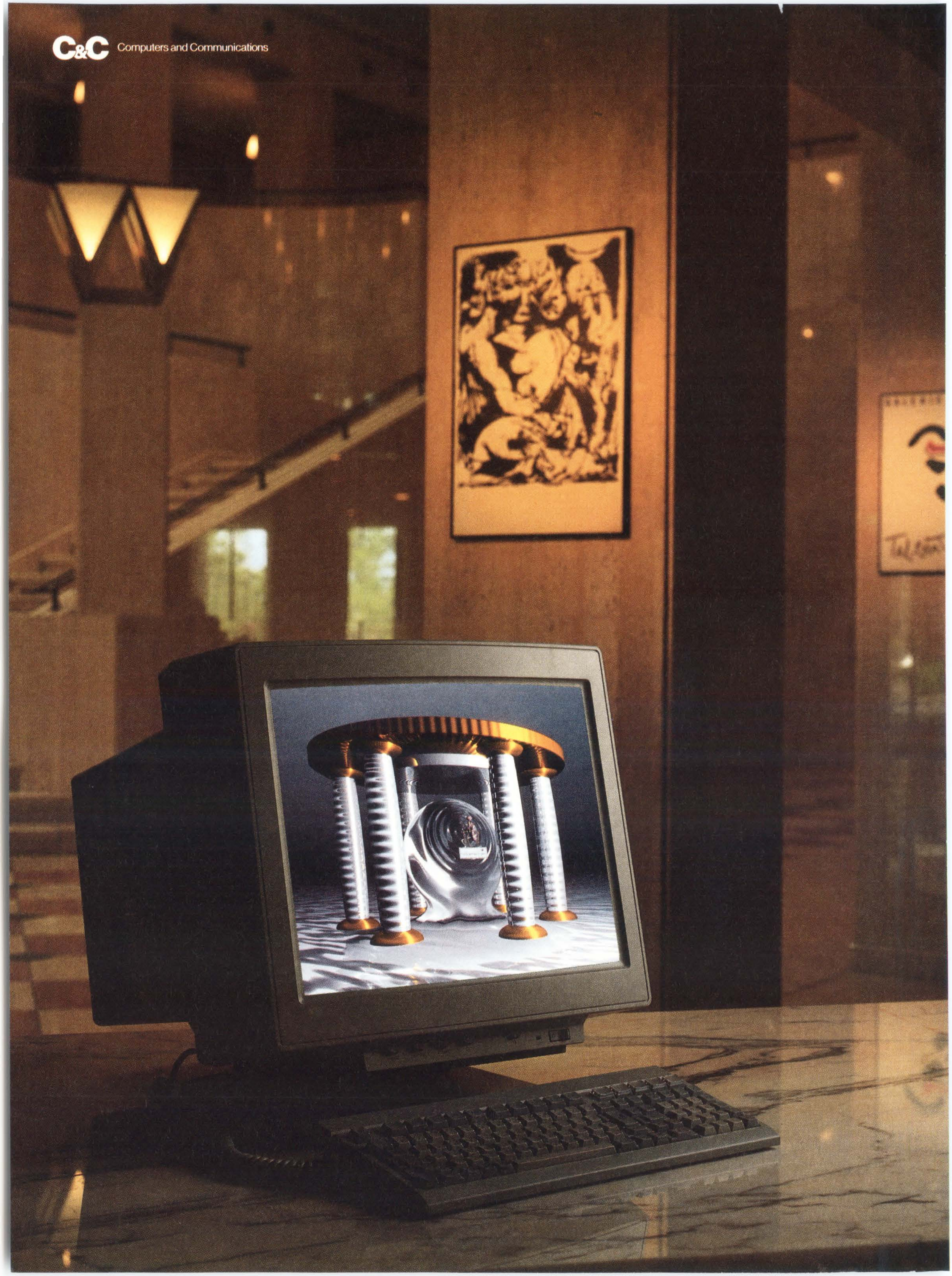
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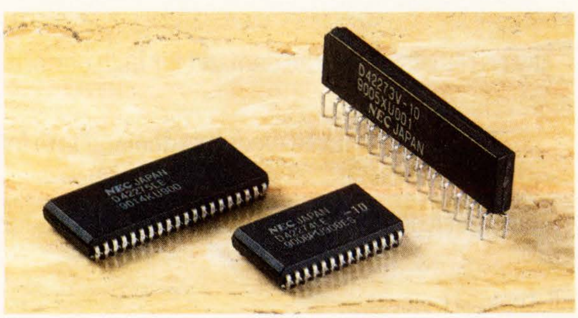

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Part Number	μPD42273	μPD42274	μPD42275
Organization			
256K x 4	○	○	
128K x 8			○
Special Features			
Fast Page Mode	○	○	○
Flash Write		○	○
Split Buffer			○
Block Write			○
Persistent Write Per Bit			○
Packages			
SOJ	○	○	○
ZIP	○	○	

Major Characteristics	μPD4227X—80	—10	—12
RAS Access Time (Max)	80ns	100ns	120ns
CAS Access Time (Max)	20	25	30
Fast Page Mode Cycle Time (Min)	50	60	70
Serial Access Time ((Max)	25	30	40
Serial Cycle Time (Min)	25	30	40

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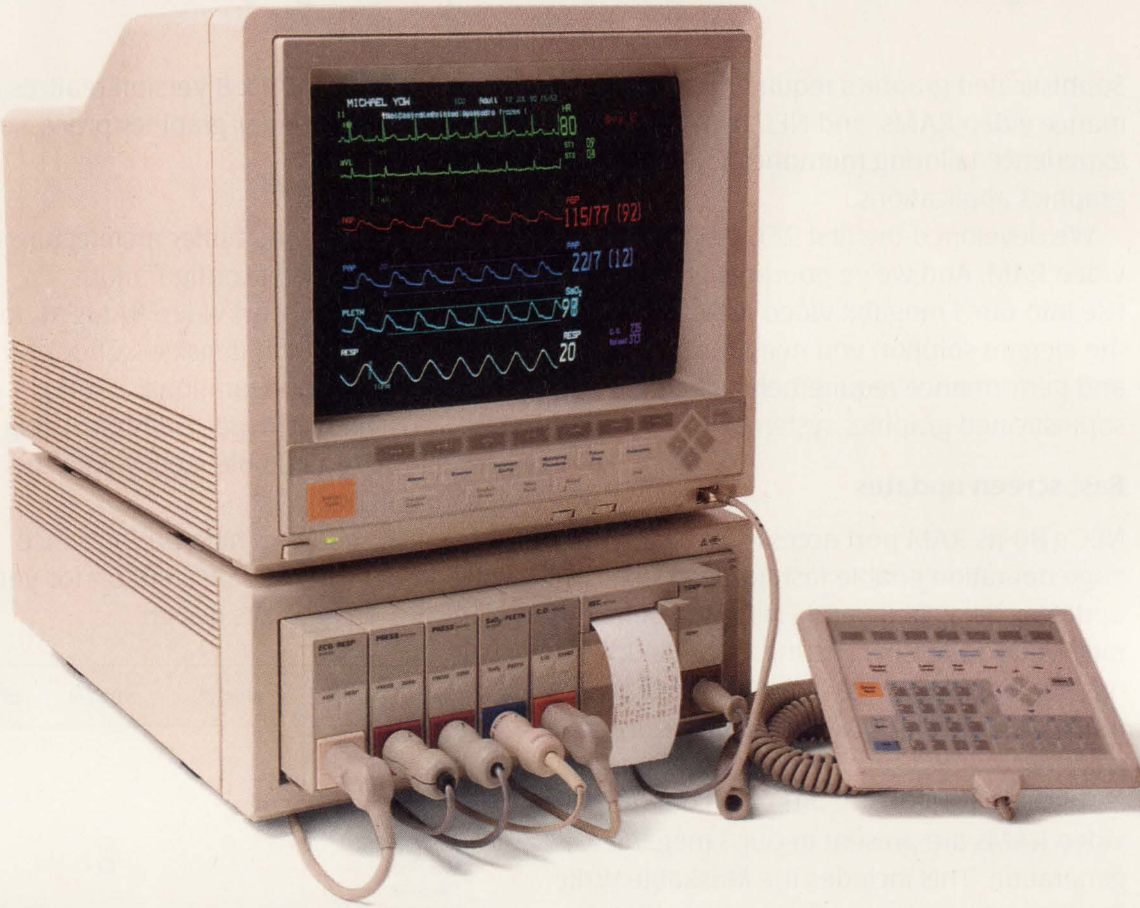

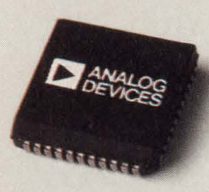

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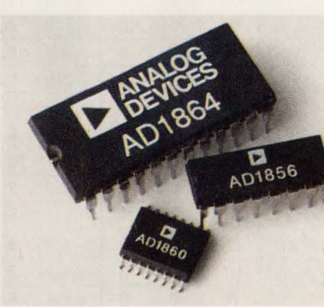

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ANALOG DEVICES

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LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	0	15	71	14	0	0	8.2	7.5
Pot-Core	0	60	20	20	0	0	6.4	8.7
Laminate (power)	0	29	71	0	0	0	6.5	8.3
CONNECTORS								
Military panel	0	0	100	0	0	0	7.9	10.4
Flat/Cable	17	33	50	0	0	0	4.9	3.6
Multi-pin circular	0	40	40	20	0	0	7.4	6.3
PC (2-piece)	25	25	50	0	0	0	4.7	4.5
RF/Coaxial	25	25	25	25	0	0	6.6	5.1
Socket	38	13	49	0	0	0	4.3	4.6
Terminal blocks	17	17	49	17	0	0	7.0	4.8
Edge card	17	33	50	0	0	0	4.9	4.1
D-Subminiature	13	25	49	13	0	0	6.6	5.0
Rack & panel	0	33	67	0	0	0	6.3	5.9
Power	0	33	67	0	0	0	6.3	3.9
PRINTED CIRCUIT BOARDS								
Single sided	0	78	22	0	0	0	4.0	5.1
Double sided	0	82	18	0	0	0	3.8	4.7
Multi-layer	0	75	25	0	0	0	4.2	6.4
Prototype	0	100	0	0	0	0	2.9	3.1
RESISTORS								
Carbon film	27	45	28	0	0	0	3.5	4.8
Carbon composition	33	12	44	11	0	0	5.5	4.3
Metal film	14	64	14	8	0	0	4.2	3.8
Metal oxide	14	29	43	14	0	0	6.4	4.3
Wirewound	0	33	56	11	0	0	7.1	6.4
Potentiometers	23	31	38	8	0	0	5.2	5.4
Networks	20	40	40	0	0	0	4.3	5.1
FUSES	38	36	13	13	0	0	4.1	2.9
SWITCHES								
Pushbutton	17	50	33	0	0	0	4.1	5.8
Rotary	0	38	49	13	0	0	7.0	7.0
Rocker	0	56	33	11	0	0	6.0	6.7
Thumbwheel	0	40	20	40	0	0	8.9	8.7
Snap action	0	43	43	14	0	0	6.8	8.0
Momentary	25	37	38	0	0	0	4.1	5.8
Dual-in-line	0	50	33	17	0	0	6.7	5.2
WIRE AND CABLE								
Coaxial	20	40	20	20	0	0	5.8	3.4
Flat ribbon	27	36	27	10	0	0	4.7	3.3
Multiconductor	22	44	22	12	0	0	4.9	3.3
Hookup	50	42	8	0	0	0	1.8	2.0
Wirewrap	29	57	14	0	0	0	2.8	2.3
Power cords	40	20	10	30	0	0	6.0	5.3
POWER SUPPLIES								
Switcher	0	17	0	83	0	0	13.3	7.9
Linear	17	17	17	49	0	0	9.4	9.6
CIRCUIT BREAKERS	14	29	43	14	0	0	6.4	7.6
HEAT SINKS	14	57	29	0	0	0	4.0	4.7
BATTERIES								
Lithium coin cells	20	40	40	0	0	0	4.3	3.7
9V alkaline	60	40	0	0	0	0	1.1	3.4
Real-time clock back-up	0	100	0	0	0	0	2.9	5.2
RELAYS								
General purpose	27	27	36	10	0	0	5.2	7.1
PC board	0	60	30	10	0	0	5.7	6.5

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
Dry reed	0	33	67	0	0	0	6.3	8.4
Mercury	0	50	50	0	0	0	5.4	5.4
Solid state	0	50	50	0	0	0	5.4	8.7
DISCRETE SEMICONDUCTORS								
Diode	36	21	36	7	0	0	4.5	4.9
Zener	23	46	23	8	0	0	4.4	4.9
Thyristor	13	37	37	13	0	0	6.0	5.6
Small signal transistor	29	29	42	0	0	0	4.2	4.2
MOSFET	17	17	33	33	0	0	8.2	6.5
Power, bipolar	0	50	50	0	0	0	5.4	4.8
INTEGRATED CIRCUITS, DIGITAL								
Advanced CMOS	0	14	57	29	0	0	9.4	5.7
CMOS	9	28	36	27	0	0	7.9	4.3
TTL	13	25	62	0	0	0	5.7	3.4
LS	22	22	56	0	0	0	5.1	4.2
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	50	0	50	0	0	0	3.9	3.8
OP amplifier	18	36	36	10	0	0	5.5	5.0
Voltage regulator	45	18	27	10	0	0	4.2	3.5
MEMORY CIRCUITS								
DRAM 16K	0	0	0	100	0	0	15.5	8.7
DRAM 64K	0	67	0	33	0	0	7.1	7.0
DRAM 256K	0	75	25	0	0	0	4.2	7.4
DRAM 1M-bit	0	67	33	0	0	0	4.6	7.4
SRAM 4K × 4	0	0	100	0	0	0	7.9	10.4
SRAM 8K × 8	0	33	50	17	0	0	7.6	5.6
SRAM 2K × 8	0	0	75	25	0	0	9.8	8.3
ROM/PROM	0	50	25	25	0	0	7.3	7.4
EPROM 64K	20	40	20	20	0	0	5.8	7.1
EPROM 256K	17	33	17	33	0	0	7.4	6.7
EPROM 1M-bit	0	50	0	50	0	0	9.2	6.6
EEPROM 16K	0	0	50	50	0	0	11.7	8.4
EEPROM 64K	0	0	50	50	0	0	11.7	8.4
DISPLAYS								
Panel meters	0	0	100	0	0	0	7.9	11.7
Fluorescent	0	0	0	100	0	0	15.5	11.5
CRT 12-in. mono	50	0	0	50	0	0	7.7	9.3
LED	27	18	45	10	0	0	5.6	5.1
Liquid crystal	0	0	40	60	0	0	12.5	8.4
MICROPROCESSOR ICs								
8-bit	0	29	57	14	0	0	7.5	5.0
16-bit	0	34	33	33	0	0	8.7	10.4
32-bit	0	34	33	33	0	0	8.7	7.4
FUNCTION PACKAGES								
Amplifier	25	0	50	25	0	0	7.8	4.9
Converter, A/D	33	0	0	67	0	0	10.3	5.4
Converter, D/A	25	0	0	75	0	0	11.6	6.8
LINE FILTERS	0	50	0	50	0	0	9.2	7.2
CAPACITORS								
Ceramic monolithic	21	64	8	7	0	0	3.6	4.8
Ceramic disc	27	45	18	10	0	0	4.3	5.5
Film	9	45	27	19	0	0	6.4	6.0
Aluminum electrolytic	9	55	27	9	0	0	5.2	4.9
Tantalum	7	43	29	21	0	0	6.8	5.4
INDUCTORS	0	37	38	25	0	0	8.0	4.2

Source: Electronics Purchasing Magazine's survey of buyers.

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Data Acquisition & Control

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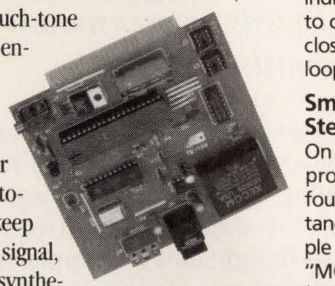
TE-158: $190.00



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AD-142: $142

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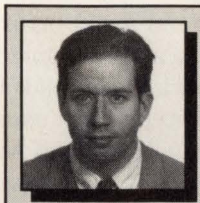
IN-141: $65



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Kevin Tschudi *Engineer, Alpha Products*

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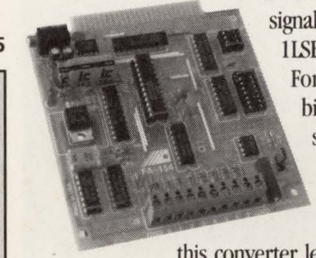

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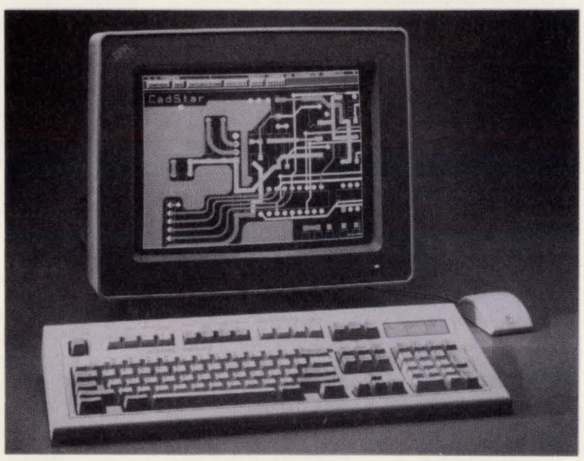
Low-cost pc-board design tools

Low-cost pc-board design software packages that run on personal computers are easy to use and have many of the capabilities of more expensive packages. They are a smart choice for engineers who design their own boards or occasionally design prototype boards.

Doug Conner, *Regional Editor*

Low-cost pc-board design software has a surprising number of the same capabilities you'll find in software packages costing much more. For less than $5000—often much less—you can obtain software that supports all the steps—design entry, component placement, routing, and design-rule checking—you need to generate artwork for fabricating a board from a schematic design. The ease of use of these packages makes them suitable for both dedicated pc-board designers and engineers needing quick turnaround and tight control over pc boards for prototype and other development applications. **Table 1** lists the capabilities of representative low-cost pc-board design software packages.

The first step in using any pc-board design system is having a schematic of the circuit you want to build. Although pc-board design systems let you design from scratch using a schematic drawn on the back of an envelope, you'll save time and avoid errors if the schematic is in an electronic format that the software can read. PC-board design systems are usually compatible with a variety of schematic-entry programs. The system typically needs two lists of information from the schematic: the netlist and the component list. Once the software has this information, you can start designing the board.

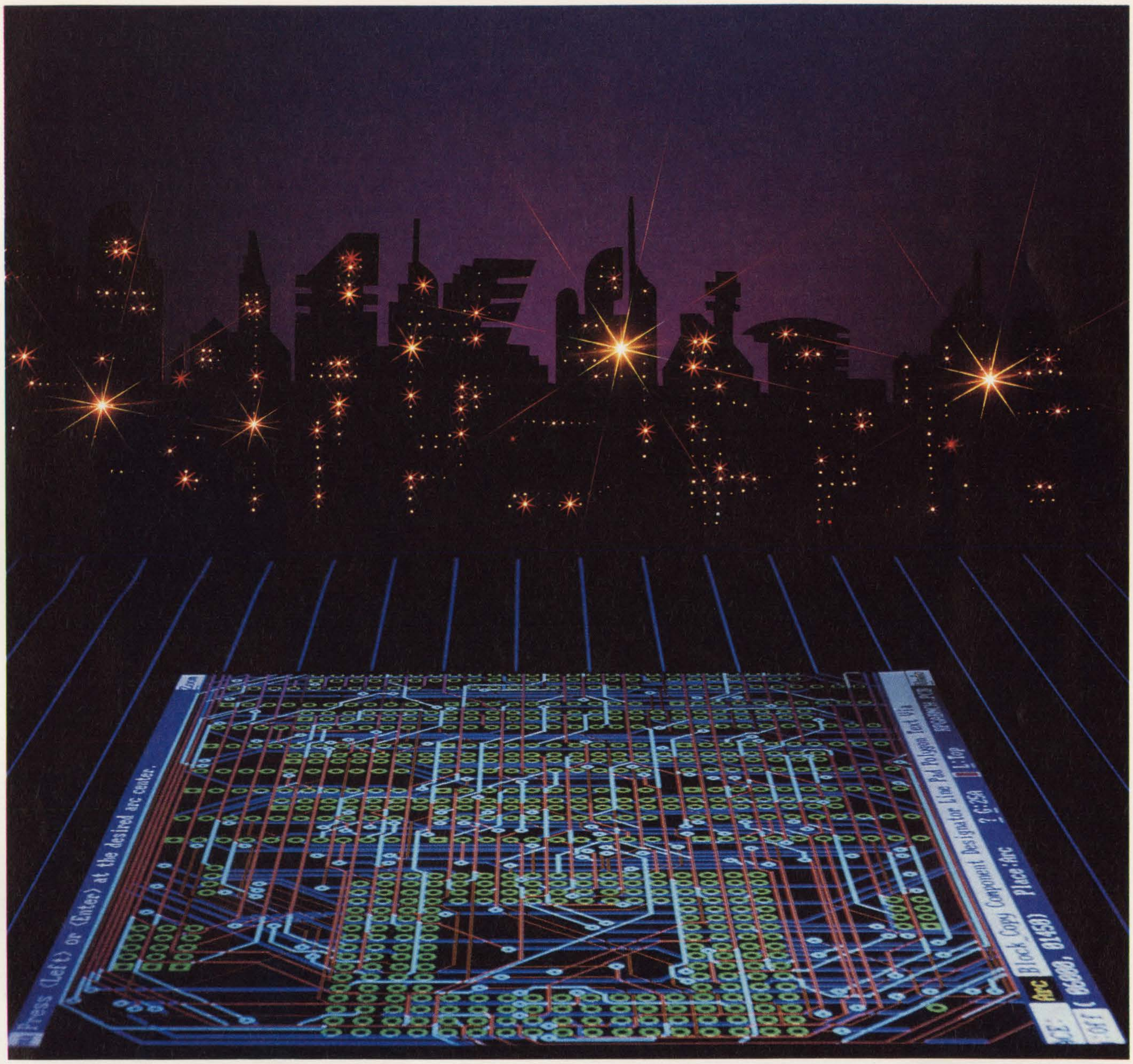


You can draw curved traces using some of the low-cost pc-board design packages, such as Cadstar from Racal-Redac Inc.

In addition to the initial electronic transfer of a design from the schematic to the pc-board design tools, some packages offer forward and back annotation. Both functions help keep the data matched between the pc-board design and the schematic.

Back annotation automatically transfers data back to the schematic after you have designed the pc board. Data typically back annotated are component identifiers and IC pin numbers. After layout, you automatically or interactively assign component identifiers in a logical sequence such as from left to right and top to bottom of the pc board. Back annotation updates the schematic to match the new component identifiers.

During layout, you or your software may have to reassign the logic blocks of ICs such as NAND gates or flip-flops that have multiple logic blocks to improve



PC-board design software that costs less than $5000 lets you perform on a personal computer many tasks that once required the power of a workstation. These tasks include forward and back annotation, autorouting, and design-rule checking. (Photo courtesy Accel Technologies)

the layout and shorten connections. By automatically back annotating these identifier and pin changes to the schematic after you've completed the layout, you'll have a schematic that accurately matches the pc board. Keeping the schematic and pc-board layout consistent is difficult to do if you back annotate interactively or manually.

Forward annotation is most useful when you need to add engineering changes to an existing design. When you need to change a pc board because of errors in the schematic or a change in requirements, you'll often correct the schematic first. Forward annotation makes the component additions or deletions on the layout and adds or removes the corresponding logical connections. You'll still need to place any new components and change the logical connections to physical tracks.

PC-board design software packages sometimes communicate better with the software vendor's own schematic-entry software than with schematic-entry software from another supplier. You should look into this issue if you are trying to match a pc-board design package with another company's schematic-entry software.

To take advantage of the netlist connection information and the parts list from a schematic-entry program, you need to have a component library that has all the components of your design. You have two alternatives: make or buy. Most design packages offer component libraries either as options or standard with the package. Purchasing a large component library can save you considerable work compared with creating your own, but you can't assume that a purchased library will fit your exact requirements.

Design software that uses the netlist's connection information should prevent you from connecting a trace to the wrong component pin.

If your company has developed its own component footprints to match its particular manufacturing methods, you can't assume the library you buy will match. For example, the lead spacing allowance for a quarter-watt resistor may vary from one company to the next.

Once you've obtained component models that include the components' physical footprints and have created a board outline drawing that includes connectors, the

Table 1—Representative low-cost pc-board design packages

Manufacturer	Product	Price (Basic package)	Component placement: Back annotation	Gate and pin swap	Components on both sides for SMT	Connection-length listing	Force vectors	Routing: Through-hole and SMT	Blind and buried vias	Design-rule checking, on-line	Design-rule checking, batch	System: Minimum grid size for manual routing (mils)	Maximum signal layers	Maximum power and ground layers	Maximum number of nets	Maximum pc-board dimensions (in.)
Accel Technologies Inc	Tango	$595 to $1695	✓		✓		✓	✓			✓	1	10	2	5000	32 × 32
Advanced Microcomputer Systems Inc	PC-Pro	$250	✓	✓	✓	✓		✓			✓	1	256	U	U	32 × 32
	EZ-Board	$695	✓	✓	✓	✓		✓			✓	1	256	U	U	32 × 32
Aptos Systems	Criterion	$995	✓	✓	✓	✓	✓	✓	✓	✓	✓	1 micron	50	50	2000	64 × 64
	RGraph	$3995	✓	✓	✓	✓	✓	✓	✓	✓	✓	1 micron	50	50	10,000	64 × 64
CAD Software Inc	PADS-PCB	$975	✓	✓	✓	✓		✓	✓		✓	1	30	U	4511	33 × 33
Cadisys Corp	Auto PCB	$995	✓	✓	✓	✓	✓	✓	✓	✓	✓	U	50	16	10,000	200 × 200
Design Computation Inc	DC/CAD	$495	✓		✓			✓	✓	✓	✓	1	32	8	7500	32 × 32
Douglas Electronics Inc	Douglas CAD/CAM	$1500			✓			✓	✓			1	U	U	>4000	32 × 32
The Great SoftWestern Co Inc	Autoboard	$295 to $4000	✓	L	✓	✓		✓	✓			U	16	16	U	25 × 25
Interactive CAD Systems	Procad	$695 to $1595	✓	✓	✓	✓		✓	✓	✓	✓	1 micron	80	6	2000	64 × 64
Number One Systems Ltd	Easy-PC	$195			✓			✓				2	8	8	U	17 × 17
Omation Inc	Schema-PCB	$975	✓	✓	✓	✓		✓	✓		✓	1	30	U	2000	32 × 32
OrCAD	PCB	$1495	✓		✓	✓	✓	✓	✓	✓	✓	1	16	16	U	32 × 32
PMS Instruments Ltd	Eagle	235 £	✓	✓	✓			✓			✓	1	2	255	U	64 × 64
Racal-Redac Inc	Maxi/PC	$995	✓	✓	✓	✓		✓			✓	1	16	16	3500	32 × 32
	Cadstar	$4850	✓	✓	✓	✓		✓	✓		✓	1	16	16	5400	32 × 32
Rubow Systems	Cadon	$795			✓			✓	✓		✓	1	U	U	>5000	32 × 32
Teradyne Inc	Vanguard PCB	$5000	✓	✓	✓			✓	✓	✓	✓	1	200	200	U	64 × 64
TSien Ltd	Boardmaker 2	$795	✓		✓			✓		✓	✓	2	8	8	800	17 × 17
Ultimate Technology Corp	Ultiboard	$4475	✓	✓	✓	✓	✓	✓	✓	✓	✓	1/1200 in.	32	32	1400	50 × 50
Visionics Corp	EE Designer III	$495	✓	✓	✓	✓	✓	✓	✓	✓	✓	1	16	10	64,000	64 × 64
Wintek Corp	Smartwork	$495									✓	50	3	0	U	10 × 16
	Hiwire II	$995 to $1695			✓	✓		✓	✓		✓	1	255	32	U	60 × 60

Note: NS = Not specified, U = Unlimited, R = Recommended, L = Limited capability.

next step is placing the components on the board. Component placement is one of the most critical steps in board design. Whether you'll be routing the board interactively or using an autorouter, a good component placement will determine how easy routing will be.

limitations			
Minimum angular rotation increment (degrees)	Computer types supported	System memory (bytes minimum/maximum)	Comments
90	IBM	640k/32M	Windows-like user interface.
90	IBM	256k/NS	
90	IBM	640k/2M(R)	Windows 3.0 compatible.
0.1	IBM	640k/NS	Both packages include schematic, pc board, hybrid, and IC design tools. Curved traces.
0.1	IBM	640k/4M	
90	IBM	640k/4M	Single parts library. Checks for thermal pads. Forward annotation.
0.01	IBM 386/486	4M/32M	Signal-specific clearance rules.
1.0	IBM	640k/NS	Includes schematic capture.
1.0	Apple Macintosh	2M/NS	Flexible pad design.
90	IBM	640k/NS	AutoCAD compatible.
1.0	IBM	640k/8M	Integrated schematic capture; 2-D mechanical drafting package.
90	IBM	512k/NS	Very easy to learn.
90	IBM	640k/NS	Forward annotation.
1.0	IBM	640k/32M	Integrated with schematic capture.
90	IBM	640k/NS	Libraries included.
90	IBM	640k/1M	
90	IBM	640k/2.2M	Motif-style user interface.
U	IBM	640k/16M	Runs under AutoCAD.
90	IBM	2M/16M	Multiwindow graphic framework. Version available for workstations.
90	IBM	640k/NS	Net-based design rules.
1/1200	IBM	2M/NS	Easy to learn.
90	IBM	640k/2M	Integrated schematic capture, forward annotation.
90	IBM	512k/NS	
90	IBM	640k/32M	Multiple windows.

Automatic placement tools do exist, but they can't perform the complete placement task. You should expect an automatic placement tool to give you an intelligent initial placement. At that point, you'll have to move components around to get an optimum placement.

Tools exist that can help you with manual component placement, and many of them are available with low-cost pc-board design software. The rat's nest display is a feature of almost all pc-board design packages and is probably the most useful tool. A rat's nest display shows network connections as straight point-to-point connections between component pins. The connections in a rat's nest display are typically rubber banded: When you move a displayed component, the display maintains the point-to-point connection by lengthening or shortening the connection and changing the angle. Using a rat's nest display, you can see immediately how well a particular placement groups interconnecting components.

Because the rat's nest display is sometimes confusing on dense pc boards with many connections, some software packages also offer alternatives. Some let you look at only a portion of the rat's nest at a time. By showing only the connections for a selected component, you can see how well the component is placed relative to the components connected to it.

Force vectors are another tool that aids in component placement. A force vector is an arrow attached to each component. The vector's direction and length indicate the average direction and length of all the connections to a component. Force vectors simplify the display, but they also eliminate connection information.

Another placement aid displays the density of connections on the pc board. By finding where the number of connections is likely to exceed the space available for tracks, placement-evaluation tools can help you avoid a component placement that would be difficult or impossible to route.

Keep connection lengths short

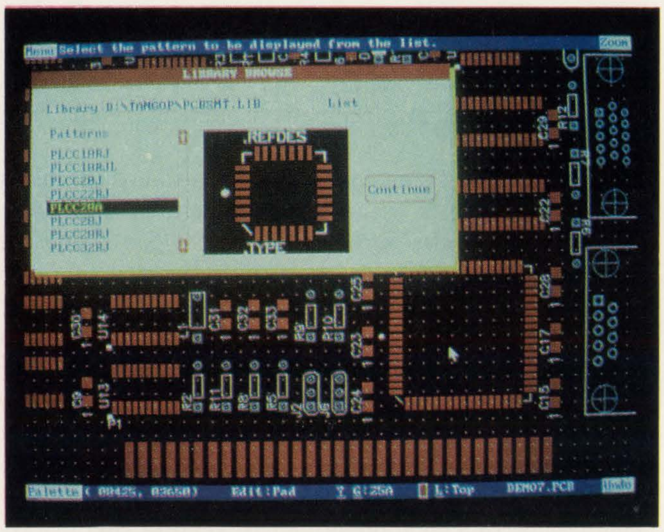
A good placement not only makes routing easy, but it should also minimize connection lengths. A measure of a layout's efficiency is the average connection length. The design software usually measures connection lengths by assuming that all tracks must run horizontally or vertically to connect two points. This type of connection length is sometimes called the Manhattan connection length. A layout that reduces connection lengths may be an improvement if it does not create areas where connection densities are too high for you to effectively route the board.

The best autorouters for personal computers typically cost $4000 and more, which pushes the system cost above the $5000 low-cost limit.

One way to minimize connection lengths is to reorder connections on a net after you've placed the components. If a net includes more than two nodes, reordering the connections will sometimes result in shorter connection lengths. Some software can reorder nets automatically.

Part of the placement task is making the pin and gate swaps necessary to minimize connection lengths and ease routing. Some software packages perform the function automatically; others offer interactive pin and gate swapping.

Component placement is a highly interactive process. You need to be able to move components quickly and easily. PC boards for surface-mount designs might require placing components on both sides of the pc board.



Component placement is one of the most critical steps in board design. The photo shows placement in progress using the Tango software package from Accel Technologies Inc.

Not all software packages let you do so. When evaluating a pc-board design system, you'll want to make sure the software and your computer can move and rotate components quickly and pan or zoom quickly.

Count on interactive routing

After developing a good component placement, you'll move on to routing the pc board. Even if you expect to use an autorouter, you should still count on spending considerable time using the interactive routing tools. You may need to do interactive routing for special analog or digital requirements or for cleaning up areas that the autorouter didn't do to your liking or wasn't able to complete. Although most pc-board design tools all perform the same operations in the interactive routing mode, the ease with which they do so varies.

For example, if the design tool takes advantage of the netlist and component information, you won't need to look for component identifiers and count to the correct pin on an IC. The software will use rubber-banded connections or some other method to show you the track or tracks you need to create for each net. Software that uses the netlist connection information should also prevent you from connecting traces to the wrong component pin.

When routing long traces, you might view a zoomed-in display of the area around the source of a signal and find that the destination is not visible on the screen. You'll find that having the display indicate the direction of the signal's destination is a helpful feature. Rubber banding a track as you lay it down from its start to its destination is an easy-to-follow method that works whether the destination is inside or outside the viewing area.

In addition to clearly showing which pads you must connect, the software should make creating the physical connections easy. The pc-board design software should let you quickly add tracks, vias, and change layers. Software that automatically adds a via when you select a different pc-board layer simplifies design. Another timesaver is being able to move a portion of a track from one layer to another.

Interactive routing usually requires some backtracking. You should be able to easily move or delete tracks or track segments. Software that can automatically and simultaneously remove tracks and vias will save you time. Modifying a route rather than removing and rerouting the net is another timesaver.

Satisfy special routing requirements

For complex pc boards, being able to quickly alter a track's width while you're routing is important. Track-width changes are sometimes necessary on analog designs and when routing through narrow spaces on surface-mount pc boards.

If you need to create a large irregular copper area on a board, you can do so on just about any system by adding wide traces until you fill the area with copper. Creating an outline of the area and using an area-fill command to create the partial copper plane is an easier method and is available on some systems.

As pc-board density and complexity increase, software support for more-complex manufacturing techniques becomes necessary. For example, you may need to use blind and buried vias, which many low-cost pc-board design packages support. Try an evaluation package before you buy to see whether support means possible but difficult, or easy enough for you to use the tool to quickly perform common functions for your type of design work.

Periodically as you design, you'll need to perform a display redraw to fill in the display in areas where you have deleted objects. A fast display redraw helps keep you from losing your concentration.

To keep screen redraws fast, some software packages display only the centerline of a trace and not its actual width. Some packages leave out other physical details around pads. This display method speeds display redraws, but you also need the option of seeing the true copper shapes of traces and pads.

Many pc boards use power and ground planes, and most design packages let you design these planes. Such software automatically connects power and ground pins to the correct planes. The software also adds clearance areas around vias and pads that do not connect to the plane.

The right autorouter may save time

Interactive routing, even with the most efficient pc-board design tools, can take days or even weeks for large or dense designs. Autorouters are another option. Although you can buy pc-board design software including autorouters for less than $5000, you'll spend more for a package that includes a high-performance autorouter.

Selecting an autorouter is not easy for either low-cost or high-performance design packages. Autorouters use different routing methods and have capabilities that are difficult to quantify. Furthermore, designers use them on a wide variety of pc-board designs.

An autorouter that does an excellent job on TTL designs might not be of any value on ECL designs because it would be unable to put termination resistors near destinations and follow other ECL routing requirements. The presence of analog circuitry in a design provides further challenges to autorouters. You don't want digital tracks crossing sensitive analog areas, and the autorouter would have to follow an endless variety of other special requirements common to analog designs. Surface-mount designs add yet more specialized manufacturing requirements for autorouters, including the directions for traces to enter pads.

A through-hole TTL design that has plenty of space between components and a good component placement may be successfully routed by a variety of autorouters. Poor component placement can stump the best autorouter.

Keeping in mind the difficulty of making generalizations about autorouters, a few comments might keep expectations in order and provide some thoughts for evaluating these tools.

The best autorouters for personal computers typi-

High-priced pc-board design packages

Some of the same companies that offer low-cost pc-board design packages also offer higher-cost tools with higher-performance capabilities. Often these tools can accept larger designs and operate more efficiently by taking advantage of the 32-bit mode of 386-and 486-class computers. Also, if you have more than $5000 to spend, you can afford the extra $4000 to $7000 you'll need to buy one of the best autorouters available for personal computers. You can usually upgrade a low-cost system by buying a high-priced autorouter later with little or no price penalty.

As you move up to workstation-based software packages, you'll find capabilities that extend beyond those of today's personal-computer-based products, at least in some areas. For example, you probably can't find a personal-computer-based autorouter that intelligently handles ECL, but you can find such a workstation-based product. ECL autorouters are more common as workstation products not because of any inherent limitations of personal computers, but because workstation-based CAE companies have more customers who need ECL tools.

In fact, personal-computer software for pc-board design is making the jump to 32-bit processing, putting the software limitations of personal computers on a par with the limitations of workstations. Although most of today's pc-board design software is still written in 16-bit code, within the next year you'll probably see many design packages that are written in 32-bit code.

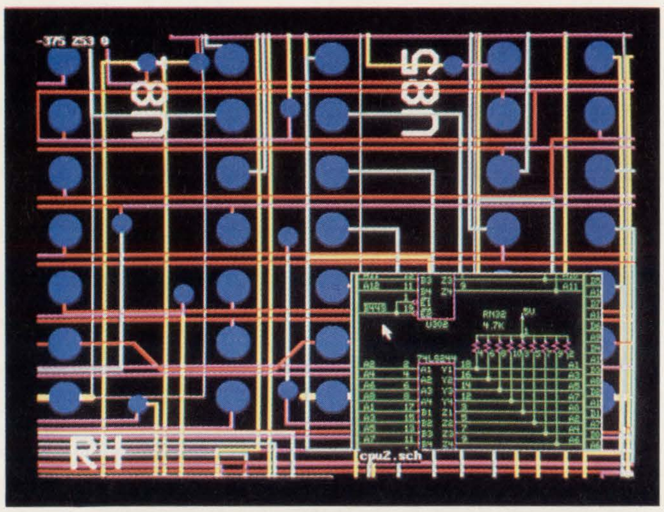
Even though 486-based personal computers offer impressive processing power, high-performance workstation-based systems continue to offer superior processing speed for autorouting large designs.

Workstation-based design systems also offer a robustness that comes from their creators' having worked on pc-board design problems longer. Considerations such as support for military-standard documentation and release control, which prevents you from using the wrong design revision, are common on workstation systems. One thing you probably won't get on workstation-based systems, however, is ease of use.

cally cost $4000 and more, which pushes the system cost above the arbitrary $5000 low-cost limit. Autorouters are often options available with basic pc-board design packages, so you can always add them later.

The best justification for using an autorouter is that the tool will save you money compared with the time you would otherwise spend routing boards. A good autorouter can pay for itself quickly, even if it costs $10,000. Unfortunately, an inexpensive autorouter with limited capability won't be cost effective even if you need to design only a few boards.

An autorouter that completes 85% of the routes on a pc board is probably not going to save you any time because it forces you to move many tracks—probably every single one—to route the remaining 15%. A router that completes more than 95% of the routes might be worth looking into, but you really want a tool that routes more than 98%.



User-defined windows for viewing the schematic and pc-board design simultaneously are available with some software packages, such as Hiwire II from Wintek Corp.

Don't be fooled by an autorouter that achieves a high routing completion by using an excessive number of routing layers. The autorouter has to be routing in the same number of layers you'd use for an interactive design, or it's wasting your money on extra pc-board layers. That waste will continue for the life of the design.

Autorouters require you to set several control parameters, depending on the complexity of the router. For example, many autorouters let you trade connection length for vias to help reduce the production cost of boards.

Autorouters have variations in what level of interactive use they support. Some autorouters are reentrant. You can autoroute, stop, make some manual routes or changes to routes, and then resume autorouting the remaining nets. Others tools don't let you interrupt and restart them. Sometimes routers that aren't re-entrant let you preroute signals. You can route critical signals yourself before you start the autorouter.

A feature typically found on the more expensive pc-board routers is a push-and-shove capability. When a designer working interactively needs to add a track where there is no space, the autorouter will push tracks over, if possible, and make slight changes to avoid clearance violations. Autorouters with the push-and-shove capability sometimes support interactive operation in a semiautomatic mode. You designate where you want the new track to go, and the router pushes other tracks out of the path.

Editing a pc-board design after an autorouter has finished with it is not an easy task. A designer has a much easier time editing a board he or she has personally designed than a board someone else has designed. Autorouters definitely count as someone else.

Let the software look for violations

Periodically as you route a pc board, you need to verify that you have not created any design-rule violations. Although autorouters automatically satisfy the design rules, when you work interactively, you might create a design-rule violation. Design-rule checking is a design-software feature that can save considerable time compared with manually checking a layout, and it's more accurate. Design-rule checking can guarantee that the pc-board connections match the schematic and can verify that you've routed the board with proper clearances.

The basic function of design-rule checking is verifying clearances between copper areas. Depending on the software, you may be able to designate different pad-to-pad, pad-to-trace, and trace-to-trace clearances. Some systems allow additional clearance specifications for vias and solid copper areas. Others use the pad clearance for vias.

One concern should be that design-rule checking verifies the spacing between the actual copper areas. For example, if the checker assumes the pads are circular, and they are in fact rectangular, a diagonal trace running close to a rectangular pad might touch it.

Design-rule checking is available on line or in batch mode. You run batch checkers periodically during the design to find and correct errors. Some design tools offer both batch and on-line checkers. On-line checking sounds great in theory because it prevents you from creating a design violation. In practice, it is sometimes a nuisance.

While interactively routing, you'll often want to

move an existing route to open up space for a new route. In the process, you might temporarily leave a track touching a pad belonging to another net. After entering the new track, you'd go back and clean up the temporary violation. With on-line design-rule checking, you are unable to leave any temporary violations. Designers accustomed to leaving temporary violations will find on-line checking unnatural and inefficient.

When you are routing signals in a design that has different design rules for different signals, the on-line checker is helpful. Rather than keeping track of the design rules for each signal, the on-line checker makes sure you are following the correct design rules for each net. To use design-rule checking in this fashion you need a signal-specific checker, a feature of some pc-board design tools.

Speed is another issue for design-rule checking. Whether the checker is on-line or runs as a batch job, it shouldn't hinder design. Some systems let you restrict the checker to the area on the screen to boost speed.

Manufacturers of low-cost pc-board design tools

For more information on low-cost pc-board design tools such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

Accel Technologies Inc
6825 Flanders Dr
San Diego, CA 92121
(800) 488-0680
FAX (619) 554-1019
Earl Therrien
Circle No. 650

Advanced Microcomputer Systems Inc
1321 NW 65th Pl
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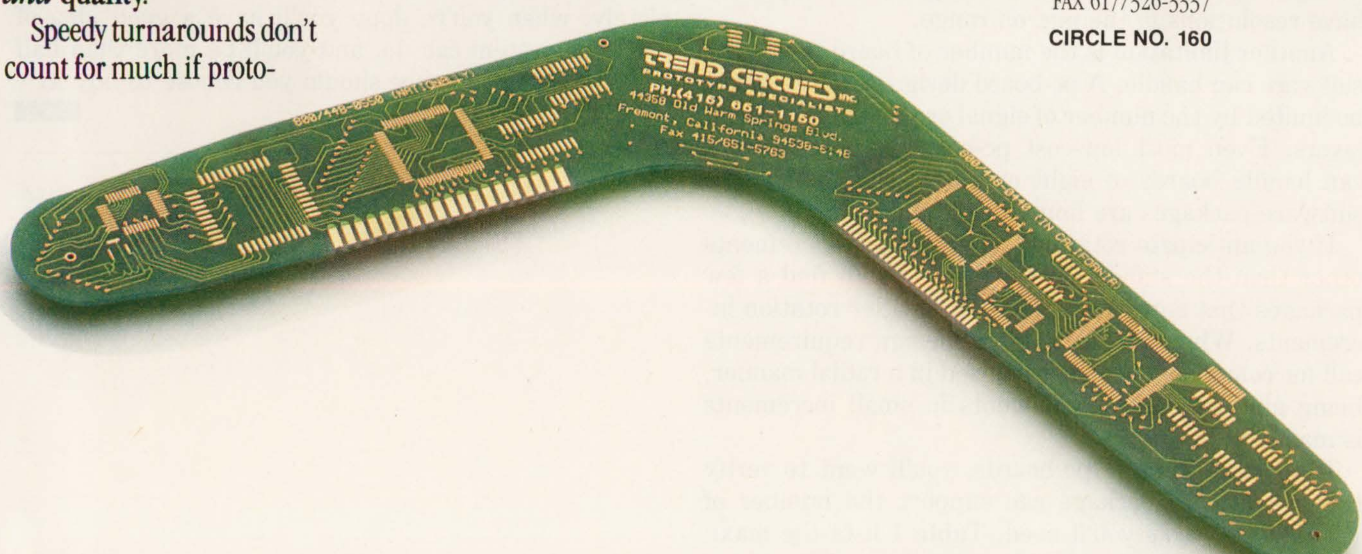

Satisfying the design rules isn't always the end of the design task. You may need to satisfy special requirements, usually for manufacturing, to finish the job.

If you've designed the pc board interactively, you may have incorporated most of the manufacturing requirements as you routed the board. Some changes, however, are easier to make after you've routed the complete pc board. For example, removing vias when a track doesn't need to change layers is usually easiest to do after you've routed all the nets. Autorouters typically make a manufacturing pass after routing to reduce vias, miter corners, and make other improvements.

After you've completed a pc-board design and are ready to have it fabricated, you'll need to make films. Most pc-board design packages provide standard outputs for photoplotters and drill tapes, although—incredibly—these outputs are sometimes options. Before you make expensive photoplots, you may want to examine a printout of the actual copper areas. Software available with many of the design packages lets you make printouts for visual checks.

System limitations to check

Most low-cost pc-board design systems can accommodate many different design types, but there are some absolute limitations that may prevent you from creating a particular design. **Table 1** lists some of these limitations. In most cases, the limitations won't be a problem.

For example, most systems have a minimum grid resolution of 1 mil for manual routing. This minimum shouldn't be a limitation for pc-board design, although it might be an issue for hybrid designs. A few systems have resolutions in the micron range.

Another limitation is the number of board layers the software can handle. A pc-board design package might be limited by the number of signal or power and ground layers. Even most low-cost pc-board design systems can handle boards of eight or more layers, but some software packages are limited to fewer layers.

If you anticipate rotating components in increments other than the standard 90 degrees, you'll find a few packages that support 1-degree or smaller rotation increments. When special pc-board design requirements call for components to be organized in a radial manner, being able to rotate components in small increments is mandatory.

If you design large pc boards, you'll want to verify that a software package can support the number of ICs and networks you'll need. **Table 1** lists the maximum number of networks the software packages support. Some packages do not have a strict limit and assign memory as needed, sharing it with other functions. In these cases, the manufacturer may not specify the number of nets the software will let you use.

Another indication of the capacity of a design tool is how much memory it can use. Software packages for IBM and compatible personal-computer systems are sometimes limited to 640k bytes of memory and designs of a few hundred ICs. Those systems that take advantage of extended or expanded memory can accommodate designs of several thousand ICs.

As the size of your design increases, so does the need for computing power. Although you can easily design a pc board with fewer than 100 ICs on an IBM PC/AT or compatible computer, designs of several hundred ICs call for 386- or 486-based systems. The computing power is especially important if you plan to use a high-performance autorouter. Even on a 386 or 486 system, a high-performance autorouter may spend more than 12 hours working on a large board that has many components. Evaluate pc-board design software on a system with the same processing speed and memory you expect to be using.

Given the many low-cost pc-board design packages available, choosing the one that best fits your needs is difficult. Even if only one looks like the right package for you, definitely try the evaluation package that most companies offer.

Evaluation packages are relatively complete and are not canned demonstrations. Usually you can perform all the pc-board design functions the complete system offers, but the evaluation software limits you by not saving or printing your design. Although you might need a few days to exercise an evaluation package completely, when you're done you'll have a good idea of what the system can do, and you'll be more than half trained on the software should you choose to buy it. **EDN**

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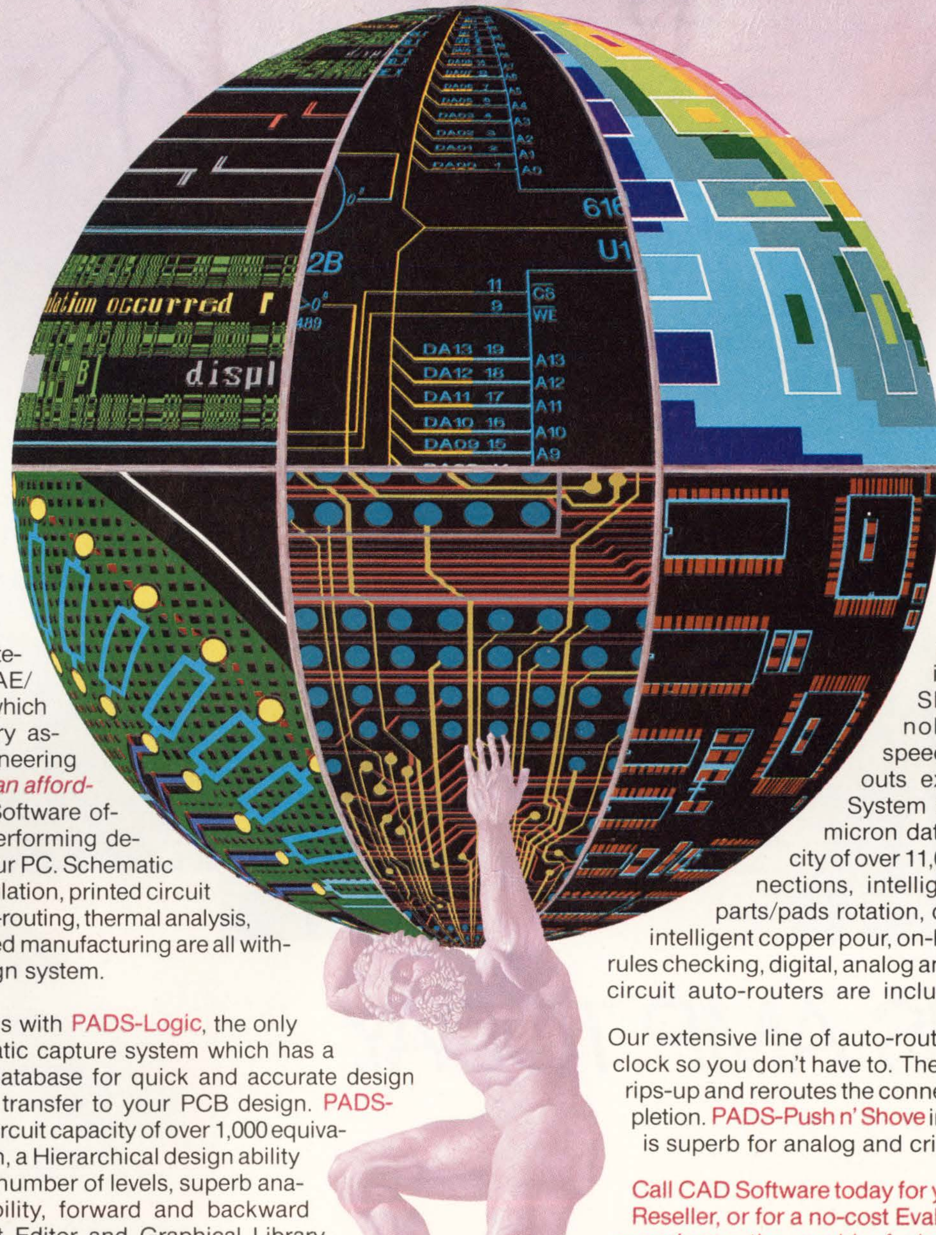

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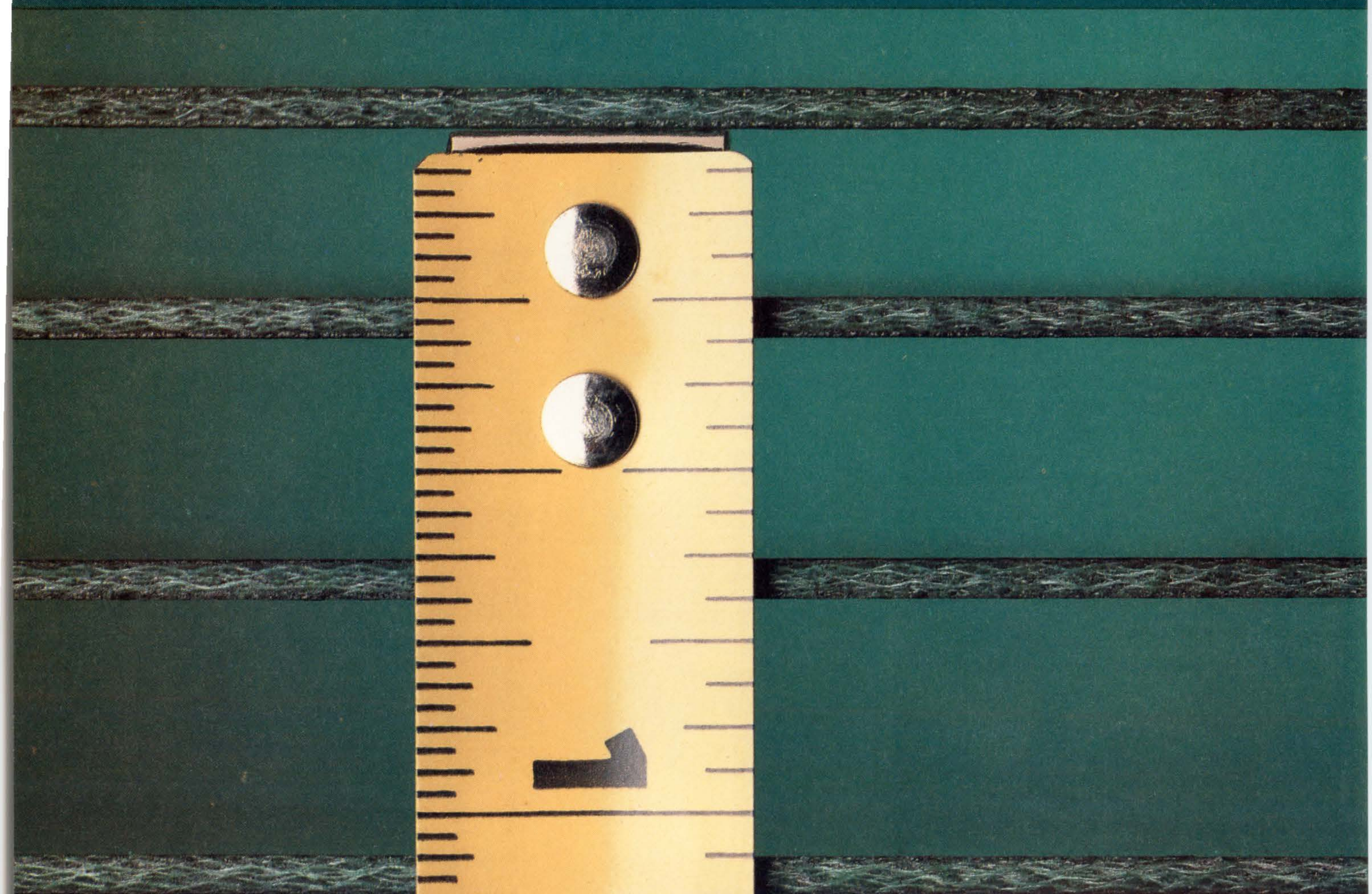

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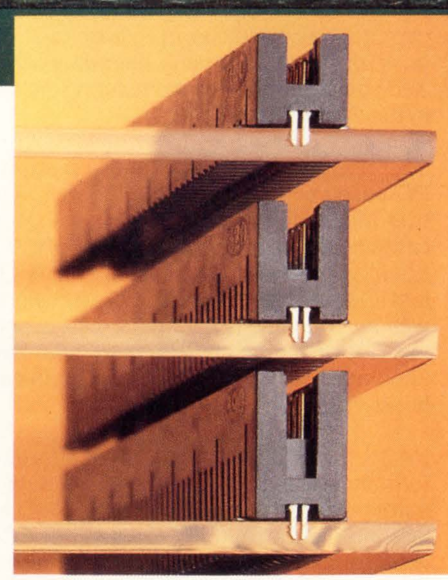

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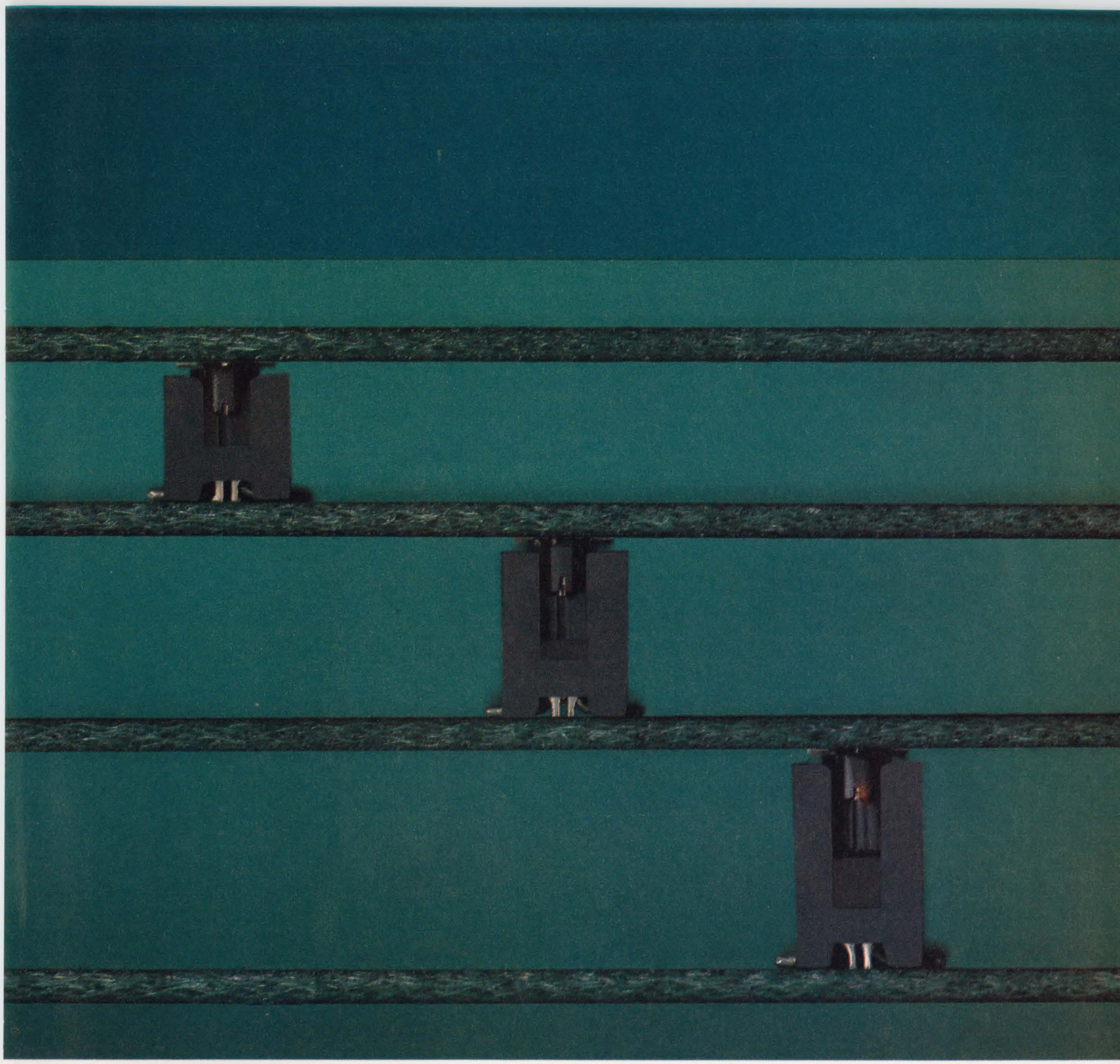

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RAID 5 architecture provides economical failsafe disk storage

Traditional methods used to back up critical data can be expensive and slow. A parity-based disk-array architecture offers an alternative that attacks these drawbacks.

Michael Anderson, *Micropolis Corp*

Redundant Arrays of Inexpensive Disks (RAID) **(Ref 1)** is a hardware and data architecture for mass data storage. Currently there are six variants, or levels, of the RAID architecture, ranging from RAID 0 to RAID 5. Each level describes an arrangement of data on an array of disk drives that increases your storage capacity and provides data redundancy in the event of a drive failure. RAID 5 is the most versatile of the RAID variants. RAID 5 provides fast data access and an inexpensive means to achieve fault tolerance that challenges traditional backup techniques.

Many of today's top-quality disk drives boast MTBFs greater than 150,000 hours. However, this MTBF translates to a 6% yearly failure rate, which can be catastrophic for many critical applications. Therefore, system designers must provide other assurances that critical data won't be lost. Traditionally, system designers have relied on two approaches to achieve fault-tolerance. The first approach, tape backup, suffers from mechanical limitations; restoring the data onto a high-capacity disk drive can often take hours because of the tape drive's slow access time.

The second approach is to record critical data simultaneously on two separate disk drives—a technique known as disk mirroring. Should one of the disk drives fail, the data on the alternate disk drive is immediately available. Disk mirroring reduces the probability of total data loss to the unlikely probability that the alternate disk drive will fail before you can replace the failed disk and restore the data onto a new disk.

Although disk mirroring is a fast and reliable method for achieving data redundancy, it's expensive. You must employ twice as many disk drives to back up the data completely. RAID 5 provides a less expensive alternative to disk mirroring while maintaining a similar low probability of total data loss.

RAID 5 is mathematically simple

The mathematics supporting the RAID 5 architecture employ the basic algebra postulate that states "If $A+B=C$, then $C-B=A$ and $C-A=B$." RAID 5 uses this same postulate but employs modulo-2 addition. In modulo-2 addition, an exclusive-OR (XOR) operation generates the arithmetic sum of the A and B terms, which is also known as odd parity. The postulate lets you reconstruct data on a single drive in the array using data stored on the remaining drives.

A simple example demonstrates how the RAID 5 technique works. Consider an array of three disk drives that store data in single bytes (8 bits). Two of the drives contain actual data, whereas the third drive contains the modulo-2 arithmetic sum of the data on the other two disk drives—odd parity. If one data drive

RAID 5 can employ the host CPU to generate parity or reconstruct data for a failed drive without incurring additional hardware cost.

contains the binary value 00110000, and the other data drive contains 00000011, the parity drive contains 00110011. **Table 1** shows how you can reconstruct the data on any of the disk drives by generating the XOR function for the data on the remaining drives.

The money you save when you use RAID 5 rather than disk mirroring to achieve fault tolerance increases as the required capacity increases. If an array requires n disk drives to attain the required capacity, disk mirroring requires $2 \times n \times$ cost/drive. In contrast, RAID 5 requires $(n+1) \times$ cost/drive to achieve the same degree of reliability. For an array containing two data drives, disk mirroring costs $4 \times$ cost/drive where RAID 5 costs $3 \times$ cost/drive. The extra cost to achieve fault tolerance using RAID 5 asymptotically approaches the cost of an array without backup as the number of drives in the array increases. The additional cost for RAID 5 is $(n+1)/n$ times the cost of an array without backup. If an array has 5 data drives, RAID 5 costs you $(5+1)/5=1.2$ times cost/drive to add fault tolerance.

Disk-drive costs don't quite complete the expenditure necessary to implement RAID 5. However, the additional hardware costs are minimal. Two additional cost factors complete the picture: the cost of the additional hardware required to control redundant data storage and the hardware cost to generate parity.

Disk drives containing a SCSI disk controller are the most efficient building blocks for the RAID 5 architecture. To employ SCSI, the host computer needs a SCSI-to-host adapter board. The board lets the host control as many as seven SCSI disk drives simultaneously. SCSI-to-host adapter boards currently cost from \$50 to \$200.

For most applications, the additional cost to generate parity can be zero. Practically all of today's file servers contain fast RISC (reduced-instruction-set computer) or CISC (complex-instruction-set computer) CPUs that have 32-bit data paths. These CPUs can execute an XOR instruction, which generates parity, in a shorter time than the time to transfer data to a disc drive. For example, a 33-MHz Intel 80386 μP can generate parity at a rate exceeding 8M bytes/sec, which is four to eight times faster than the typical SCSI transaction rate. Therefore, a basic implementation of RAID 5 can employ the host CPU to generate parity or reconstruct data for a failed drive without additional hardware cost.

Table 1—Reconstructing the data for a failed disk drive

	00110000	Drive 1 (data drive)			
XOR	00000011	Drive 2 (data drive)			

	00110011	Drive 3 (parity drive)			
	00110000	Drive 1		00000011	Drive 2
XOR	00110011	Parity drive	XOR	00110011	Parity drive
	--------			--------	
	00000011	Drive 2		00110000	Drive 1

Table 2—Calculating new parity using strategy 1

	00110011	Drive 3 (old parity)
XOR	00110000	Drive 1 (old data)

	00000011	(Old parity with old data removed)
XOR	11000000	(New data)

	11000011	(New parity)

Three strategies manage the data

RAID 5 not only offers fault-tolerance at a lower cost than traditional disk mirroring, but the architecture also efficiently distributes and manages the data on the disk drives. RAID 5 offers three data-management strategies. To write new data to a disk drive using strategy 1, called read-before-write, the host first reads the old data and the old parity bytes from their respective disk drives. The host then removes the effect of the old data on the old parity byte before generating a new parity byte using the new data (**Table 2**). The host can then write the new data and the new parity to their respective disk drives.

Strategy 2, read-what-you-don't-have, writes data to a disk drive in a different manner. First, the host reads data from a disk drive whose data isn't being modified. The host generates a new parity byte by taking the XOR of this data with the new data to be written (**Table 3**). The host then writes the new data and the new parity byte to their respective disk drives.

RAID 5 employs strategy 3, read-nothing, when modifying all of the data drives simultaneously. For example, in a 3-drive array, when the host must simultaneously modify both data drives, there isn't a need to read old data or the old parity byte. The host simply generates a new parity byte from the two new data bytes and stores both the data bytes and the new parity byte on their respective disk drives.

RAID 5's three data-management strategies offer different advantages depending on the number of blocks that you need to modify. If you need to modify

Table 3—Calculating new parity using strategy 2

	00000011	Drive 2 (Not being modified)
XOR	11000000	Drive 1 (New data to be written)

	11000011	New parity

only one block of data, strategy 1 is the most effective. If you need to modify data on more than one half of the disk drives, you should employ strategy 2 because there is less data for the host to read before modifying the blocks. If you must modify the data on all of the drives, strategy 3 is the most efficient since it doesn't require the host to read data from any drive.

RAID 5 distributes data and parity

You've probably noticed that all three strategies for modifying a data drive also require the host to modify the stored parity byte. If you store parity information on a single disk drive, as some variants of the RAID architecture suggest, each time the host modifies data in the array, it must also access the parity disk drive. Therefore, an array architecture having a single parity disk drive creates a bottleneck because the host can only modify data sequentially.

RAID 5 overcomes this potential bottleneck by distributing the parity information over all of the drives in the array. Because each drive in the RAID 5 architecture contains a mixture of data and parity, the host can issue read and write commands in parallel. **Table 4** shows a typical RAID 5 implementation for an array containing 4 disk drives. In this implementation, block 1 data resides on drive 1 and block 6 data resides on drive 2. The parity information for these two blocks is on drives 4 and 3, respectively. Therefore, the host must access drives 1 and 4 to modify block 1 data using strategy 1. Similarly, the host must access drives 2 and 3 to modify block 6 using strategy 1. Because the drives are independent, the host can modify both blocks of data in parallel.

Satisfying multiple disk transfer requests in parallel increases the system's transaction rate. A high transaction rate is important for image processors and virtual-memory systems that swap large amounts of data in solid-state memory to and from disk. The data distribution shown in **Table 4** locates sequential blocks of data on successive disk drives in the array. This arrangement lets the host queue four read requests, for example, from blocks 5, 10, 3, and 12. The queued requests

Table 4—Raid 5 data and parity distribution

	Drive 1	Drive 2	Drive 3	Drive 4
Address 1	Block 1	Block 2	Block 3	*P(1-2-3)
Address 2	Block 5	Block 6	*P(4-5-6)	Block 4
Address 3	Block 9	*P(7-8-9)	Block 7	Block 8
Address 4	*P(10-11-12)	Block 10	Block 11	Block 12
Address 5	Block 13	Block 14	Block 15	*P(13-14-15)

*Parity

permit the four independent disk drives to access the correct track and sector for the blocks in parallel and thereby proportionally reduce the disk access time.

Many operating systems, including PC-DOS, generate disk requests of varying length. For example, when the operating system loads a program into memory it can generate a large disk request ranging from 64 to 128 blocks of data. On the other hand, when the host accesses a file directory or updates a database, the operating system generates a small disk request ranging from 1 to 4 blocks. The RAID 5 architecture can efficiently handle both types of request and provide inexpensive failsafe storage as well. EDN

Reference

1. Patterson, David A, Garth Gibson, and Randy Katz, "A Case for Redundant Arrays of Inexpensive Disks (RAID)," Report UCB/CSD87/391, Computer Science Div, (EECS), The University of California, Berkeley, CA, 1987.

Author's biography

Michael Anderson is the director of software engineering for Micropolis Corp. For the past 2 years he has managed an engineering and support staff, participated in market planning, and defined future products. He has also contributed to the development of 360M-, 760M-, and 1.2G-byte disk storage products. Michael majored in computer science at the University of Nebraska and is married with 3 children. He lists parallel arrays, processors, and storage as personal interests.

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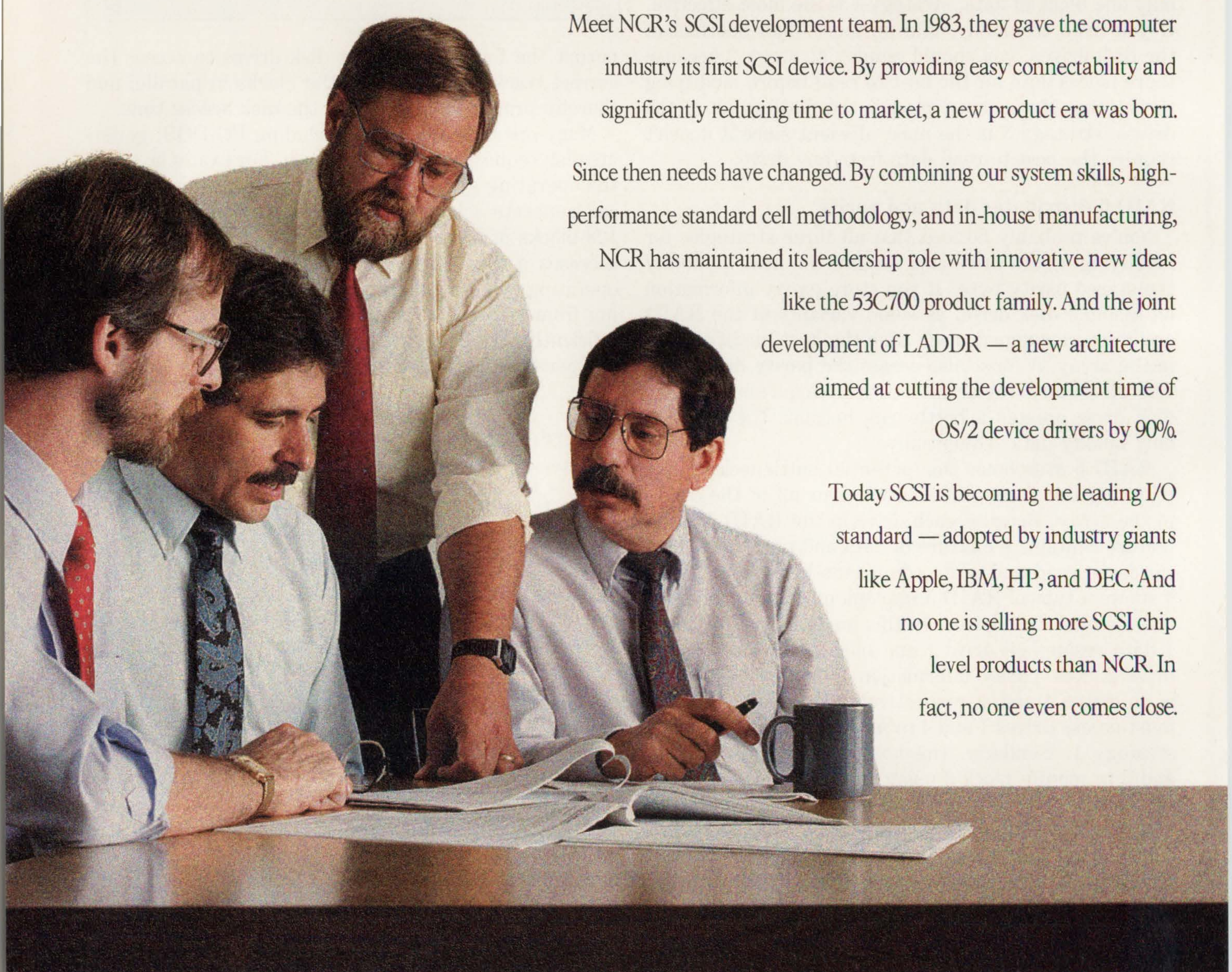

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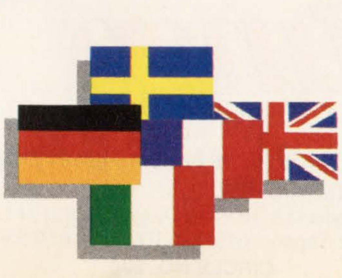

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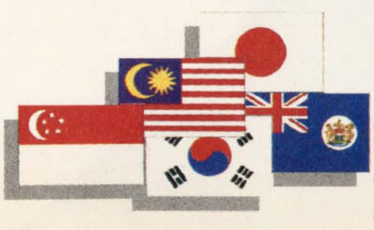

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Careful inductor selection optimizes dc/dc converters

Higher output power levels and faster switching speeds have complicated the selection of inductors for small dc/dc converters. However, if you check circuit waveforms for anomalies and review key electrical parameters during the design phase, you can simplify the development of an optimized dc/dc converter.

Bruce D Moore, *Maxim Integrated Products*

Battery-operated systems and distributed-power-system concepts have greatly increased the use of low-power dc/dc converters and their associated magnetic components. Designers typically use transformers in dc/dc converter designs. However, unless transformer isolation is required, an inductor makes sense for a low-power switching-converter applications. This is especially true if the circuit must be more efficient than a capacitor-based charge-pump circuit. Compared with transformers, inductors are easier to specify, procure, and mount. Single-transistor-driver schemes are more effective with inductors than with transformers. Best of all, there's a variety of inductor types available, each in a range of inductance values.

Because standard inductors suit most applications, you can usually avoid expensive custom-magnetics development. Selecting the optimum inductor requires some knowledge of the available inductor geometries and core materials, however. (Note that for some unknown reason, inductor data sheets are often cagey about the product's core-material type.)

In the context of designing dc/dc converters that have an output power capability of 10 watts or less, a boost regulator serves as a general example. The boost regulator used as an example, also called a flyback regulator, features pulse-frequency modulation (PFM) to first establish its L value and then calculate its maximum ratings. By examining the inductor further, you can find certain specifications and characteristics that are a function of its shape and materials.

Fig 1 illustrates the three basic topologies for single-inductor switching regulators—the buck (or step-down), the boost (or step-up), and buck-boost (or inverting) topologies. Low-power regulator applications generally combine one of these topologies with a PFM or PWM (pulse-width-modulation) controller circuit. The different combinations of topology and controller place similar demands on the inductor. However, you must take extra care in calculating the inductance value in pulse skipping controllers.

When selecting an inductor for a simple buck-regulator circuit, you must take several factors into account—inductance value, saturation current, dielectric strength, dc resistance, EMI, and stray capacitance.

The converter's switching frequency and the voltage drop across the inductor determine the correct induc-

Because standard inductors suit most applications, you can usually avoid expensive custom-magnetics development.

tance value. Both factors affect the inductor current's rate of change in any given application. Erroneous inductor values can generate excessive current in the switching transistor or lower the inductor's energy storage performance. Insufficient energy storage, in turn, slows both converter start-up- and transient-response times. In clocked-PFM regulators, insufficient energy storage will also degrade load regulation.

Economic considerations also provide a strong incentive to reduce inductor values: lower values require less wire and smaller cores. As a rule, you should select an inductor whose value is as low as possible, and yet does not introduce excessive-current, inefficiency, component stress, and high-ripple problems.

Pulse-skipping PFM regulators, such as the boost circuit in **Fig 2**, are a good choice for battery-powered applications because the design draws minimal quiescent current and requires few external components. Here, however, you must be especially careful when selecting the inductor, to avoid load-regulation problems. Studying the regulator's switching waveforms (**Fig 3**) provides some clues about the factors that influence a PFM regulator's output.

Supply voltage and inductance value determine the slope of an inductors' current waveform. Because the regulators in question operate in a discontinuous-current mode (the current returns to zero on every cycle), the regulator's average load current is directly proportional to the peak inductor current. Peak current depends on slope, and the slope depends on the inductor's value. An inductor with an excessive L value, therefore, cannot transfer adequate energy on each oscillator cycle.

Peak inductor current can be expressed in terms of the voltage boost ratio and the load current as

$$I_{PK} = (4I_{LOAD})(V_{OUT} + V_D - V_{IN})/(V_{IN} - V_{SW}),$$

where the factor of 4 is a constant resulting from the 50% duty cycle. Values for I_{PK} and the switch transistors' on time (t_{ON}) let you calculate the optimum inductor value as

$$L = (t_{ON})(V_{IN} - V_{SW})/I_{PK},$$

where V_{OUT} equals output voltage, V_{IN} equals supply voltage, V_{SW} equals saturation voltage of the switch transistor, and V_D equals the forward voltage of the rectifier diode.

Coil inductance must not be so low that peak cur-

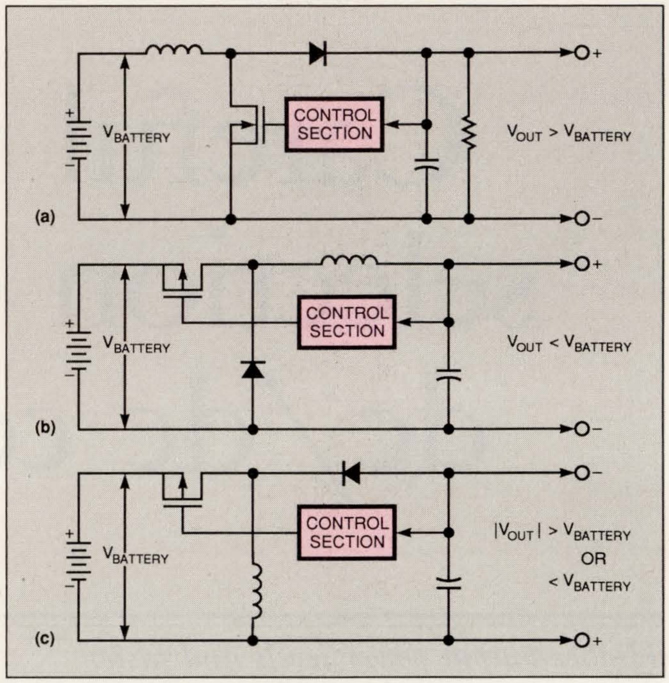

Fig 1—By arranging the same basic components *in different topologies, you can obtain a boost* ***(a)****, a buck* ***(b)****, or a buck-boost* ***(c)*** *dc/dc regulator.*

rents saturate the core or overstress the switching transistor. This rule applies to both PFM and PWM regulators. Excessive inductor current causes many odd symptoms, including low efficiency, rattling heat sinks, whining coils, and increased output ripple. Very low inductance can lead to burned windings and shattered, smoking transistors and ICs. The worst-case I_{PK} in the previous PFM-regulator calculations occurs when load current, supply voltage, and the diode's forward voltage are all maximum values while inductance, switch on-resistance, winding resistance, and switching frequency are all minimum values.

As you strive to extract higher output current from a PFM regulator, the minimum- and maximum-allowable inductor values tend to converge. An actual convergence indicates the need for a power transistor capable of higher currents. But excessive peak currents can result from the discontinuous-current mode in which the inductor operates. This I_{PK} limitation makes clocked-PFM regulators impractical for power levels exceeding 10W.

The following example uses earlier equations for I_{PK} and L to convert an input of 5V (±10%) to an output of 15V using a 1N5817 diode and a MAX641 regulator IC. The IC has a ±10% tolerance on its 50-kHz oscilla-

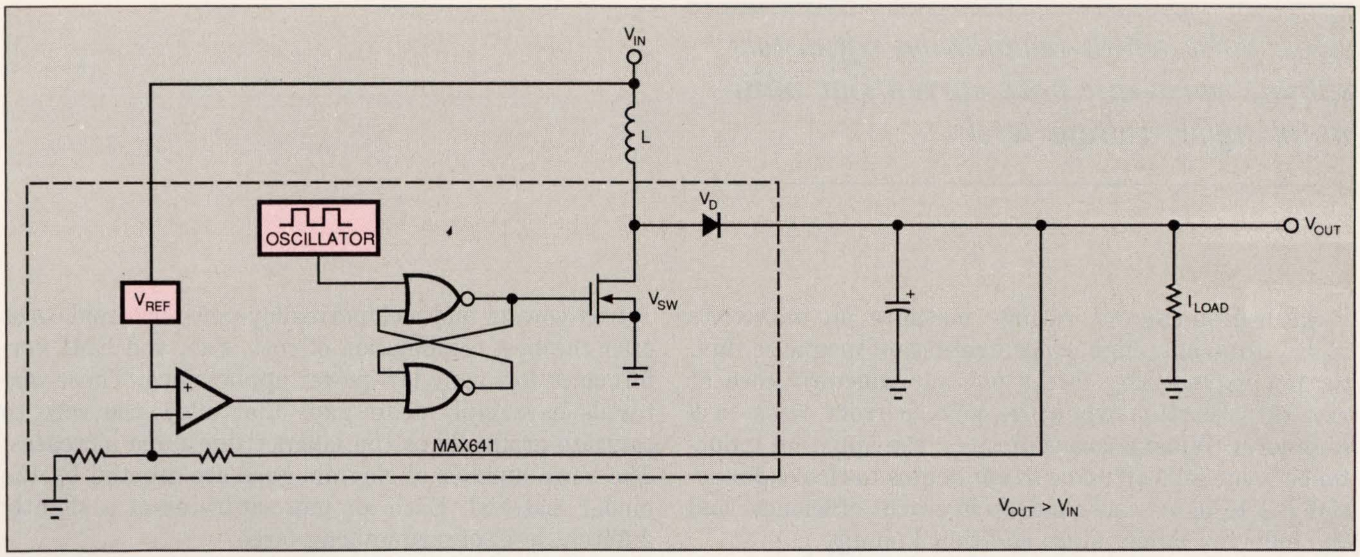

Fig 2—To regulate the output voltage, the MAX641 boost regulator employs clocked pulse-frequency modulation or pulse-skipping techniques.

tor frequency. The output-current capability must be 15 mA. First, calculate the maximum-allowable inductor value using the equation

$$I_{PK} = 4(15\text{ mA})(15V + 0.4V - 4.5V)/(4.5 - 0.75) = 174\text{ mA}$$
$$L = (9\ \mu\text{sec})(4.5V - 0.75V)/174\text{ mA} = 194\ \mu\text{H}.$$

Next, you must calculate the minimum-allowable inductor value. Here, let I_{PK} equal 450 mA—the maximum current rating for the switch transistor in the IC. With those criterion,

$$L = (11\ \mu\text{sec})(5.5V - 0.25V)/450\text{ mA} = 128\ \mu\text{H}.$$

From off-the-shelf inductors, you can choose a standard value like 150 μH—a value which lies between the calculated minimum and maximum values.

Selecting the inductor for PWM regulators

Unlike pulse-skipping PFM regulators, most PWM regulators exhibit worst-case peak currents at minimum supply voltages. Because PWM regulators generally operate in a continuous-current mode at high duty cycles, their inductance values are limited only by winding constraints and the need for reasonable start-up and transient-response times.

In continuous-current mode, the inductor current fluctuates, but never returns to zero. Because the current may increase in staircase fashion over a period of several cycles, its rate of increase (determined by the inductance value) does not constrain the maximum level attained by the inductor current or the average load current. Thus, PWM regulator designs do not impose a hard limit on the maximum inductance value. The minimum value depends on the inductor's I^2R loss and the switching transistors' current capability.

The exact inductance value is seldom critical for regulation in a PWM circuit, but some control schemes require a particular value for other reasons. The

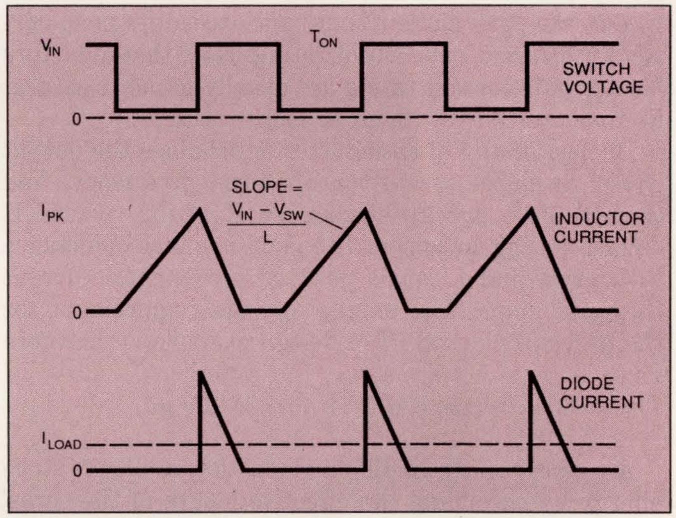

Fig 3—To ensure ac stability, the inductor current in Fig 1's pulse-frequency-modulation regulator must return to zero during each switching cycle.

MAX743 dual-output regulator IC, for example, which features current-mode feedback control, achieves ac stability by compensating the inductor current's rate of change, or slope. To ensure ac-stable operation, which is free from subharmonic noise, you must tailor the slope compensation to a given supply voltage and inductance value.

Don't overlook saturation effects

In some specialized circuits the design deliberately saturates the magnetic core (for example, Royer-type self-oscillating transformer-drive schemes and saturable magnetic reactors that provide regulation in multiple-output, transformer-based power supplies). In most applications, however, you select the inductance and the core material (using air gaps in the core if necessary) to avoid saturation. For PWM regulators in particular, you must take care to avoid magnetic saturation.

Most pulse-width-modulation regulators exhibit worst-case peak currents at minimum supply-voltage levels.

Saturation-current ratings measure an inductor's ability to handle high concentrations of magnetic flux. Strong magnetizing forces put an inductors' core at risk of saturation when the peak current rises to a high level. When a core saturates, the apparent inductance value falls off and current begins to rise exponentially. I^2R losses cause a drop in circuit efficiency, and the inductor cannot store additional energy.

High-current spikes resulting from saturation can endanger power transistors and cause noise and efficiency problems. To avoid saturation, the inductors' worst-case peak current must not exceed its peak current or incremental-current rating. Note that inductors lacking a dc-current rating are usually prone to saturation, as are those with an ac amps rating.

Energy stored in an inductor determines the output power available at a given operating frequency. You can calculate energy storage as $E = LI^2/2$, where E equals energy in joules, L equals nominal inductance in henrys, and I equals peak or incremental current rating in amps. The energy storage requirement for the previous clocked-PFM design example is therefore

$$E = (194\ \mu H)(174\ mA)/2 = 2.9\ \mu J.$$

Air gaps greatly amplify an inductors' ability to store energy by extending the effective length of the cores' magnetic path. Air can store a tremendous amount of energy. A small air gap, whether built into the material or created by grinding or machining operations, can more than double the power output from a given core by preventing saturation at high current levels.

Ferrite and other highly permeable core materials are very susceptible to saturation, and you must treat them accordingly. The closed magnetic path of a ferrite toroid, for instance, is extremely good for containing EMI. However, the short path combined with the ferrite's high permeability make toroids prone to saturation. Ferrite toroids make good transformer cores, but they are less suited to simple boost regulators featuring large dc-offset currents.

For applications of 5W or lower, powder-type cores with distributed air gaps are often a better choice than ferrite toroids or pot cores. After cutting an air-gap slot in the core of a ferrite toroid, the machining costs and EMI level will be so high that you may have been better off choosing a ferrite bobbin, with its large inherent air gap, in the first place. Pot cores, though self-shielding, are more expensive because they require more manufacturing steps than the other types.

Iron-powder and molypermalloy-powder toroid cores offer the best combination of cost, size, and EMI performance for many low-power applications. These materials have built-in air gaps that allow the core to saturate gradually as the magnetizing force increases. The large number of tiny air gaps are created by the binder material. Each air gap saturates at a slightly different level of magnetizing force.

The cylindrical or bobbin-core geometry, although noisy, is best for low-power ferrite applications because such shapes are easy to wind, and are therefore inexpensive to manufacture. Ferrite pot cores are preferable for applications higher than 5W. The pot core's low EMI emissions are a benefit in applications that involve high levels of current and magnetic field strength.

A look at core-material tradeoffs

There are no clear cut best-choice winners when you look at today's available core materials; each has a distinct advantage in certain areas (**Table 1**). Ferrites are attractive because they combine low cost with high volumetric resistivity, which minimizes eddy-current losses. Ferrites are the only choice for switching frequencies of 500 kHz and higher. On the other hand, ferrites' high permeability usually calls for an air gap and the associated complications: high EMI for bobbins and extra assembly steps for pot cores.

Molypermalloy powder (MPP), the Porsche of powder core materials, combines good saturation characteristics with low hysteresis losses. MPP is expensive, however; it contains scarce ingredients (nickel) and requires many processing steps. Iron powder and silicon-steel tape, despite their tendencies to sustain eddy-current and hysteresis losses, are inexpensive materials also suited to general-purpose applications.

For small size combined with good EMI performance, it's hard to beat high-flux MPP toroid cores. Standard MPP cores, formulated for RF applications, contain 80% nickel, plus iron and molybdenum. The high-flux variety contains 50% nickel and doesn't work as well for RF applications. However, high-flux MPP cores provide tremendous flux-handling that is useful in switching-regulator circuits.

For comparison, ferrite and standard MPP materials handle flux densities of 4500 and 7500 gauss, and the high-flux MPP material is good for 15,000 gauss. High-flux cores can handle switching frequencies ranging to 300 or 400 kHz before eddy-current losses become excessive. Like all MPP cores, the high-flux types are

Table 1—Common inductors that suit dc/dc converters

Type	EMI	Comments
Ferrite bobbin	high	Makes compact, low cost, axial-lead (cylindrical) inductors. Low core losses support high efficiency.
Ferrite bobbin with ferrite shield	low	Efficient but prone to saturation.
Ferrite pot core	low	Efficient. Easily gapped to the correct value. Best for high-current or high-frequency applications.
Molded (low cost)	high	OK for light loads. Prone to saturation and often inefficient. Observe current ratings carefully.
Silicon-steel toroid	low	Tape wound; similar to iron powder. Use thinner tape for higher frequencies.
Ferrite toroid	low	Prone to saturation.
Molypermalloy-powder toroid	low	Best available for frequencies less than 400 kHz. Low EMI, low losses, compact, and expensive. Use high-flux type.
Iron-powder toroid	low	Specify core material carefully to achieve low losses.

expensive. For low-power miniaturized applications, however, the high-flux MPP cores are often more cost-effective than ferrite types because they eliminate the need for precision gapping.

Size reduction is possible with high-flux core materials, as can be seen by comparing two prototype boards for the MAX743 switching regulator. Both boards generate 3W at ± 15V from a 5V source. However, the surface-mount version uses a high-flux core material to achieve a much higher power density—18W/in.^{3} vs 2W/in^3.

The core material affects the power level for a given inductor size, but dc resistance in the windings will waste some of that power. In the step-up circuit of **Fig 2**, the approximate average inductor current is given as

$$I_{AVE} = I_{LOAD}((V_{OUT} + V_D - V_{IN})/(V_{IN} - V_{SW}) + 1).$$

High winding resistance produces an L/R effect in the inductor-current waveform. The resulting I^2R losses degrade circuit efficiency and cause the core temperature to rise.

For pulse-skipping PFM-type regulators, the dc-winding resistance can have the same effect as an overly high inductance value. By limiting I_{PK}, dc resistance limits the available output current. Note that the calculation for maximum inductance value does not account for dc resistance. This dc resistance is significant for battery-powered and low-voltage applications of 3V or less. In these cases, the inductance values must be low enough to achieve an acceptable slope for the inductor-charging current. Ideally, this slope is determined by the input voltage and the inductance value or $I(t) = V_{IN}(t)/L$. The peak current is therefore a function of t_{ON}, or $I_{PK} = V_{IN}t_{ON}/L$. Finally, dc-winding resistance (R_{DC}) limits inductor current as the inductance value approaches zero, as given by the expression

$$I_{PK} = (V_{IN}/R_{DC})\ (1 - e^{(-R_{DC}t_{ON})})/L.$$

Another current-related topic to consider is temperature rise. Inductor specifications generally include two current ratings—continuous (or rms) and dc saturation, which is sometimes referred to as peak or incremental current. A continuous rating accounts for the temperature rise caused by winding resistance, the inductor's operating temperature range, and its insulation or potting-material properties. The continuous rating is usually higher than the dc-saturation rating. Often, however, just the opposite is true for higher-valued inductors. As a rule of thumb, make sure that the inductors' average current is less than its continuous current rating. In high-frequency applications, be sure to include a safety margin for additional temperature rise due to core losses.

High-frequency losses consist of three major components—losses due to hysteresis, losses due to eddy currents in the core, and losses due to eddy currents in the wire. Legg's equation defines losses within the core as

$$R_{AC}/L\mu = Xf + YB_m f + Zf^2,$$

where R_{AC} equals the equivalent loss resistance in ohms, L equals inductance in henries, μ equals magnetic permeability, X equals residual-loss coefficient, f equals frequency, Y equals hysteresis-loss coefficient, B_m equals maximum flux level in gauss, and Z equals eddy-current-loss coefficient.

Magnetic hysteresis, which occurs as flux density nears its saturation point, becomes a problem in iron-powder cores at switching frequencies of 100 kHz or lower. A simple cure for this problem is to enlarge the core volume, which will reduce the peak flux density at high currents. Larger cores, however, exacerbate the eddy-current problem by providing more low-resistance paths for current. Eddy current in the core is a function of f^2, and rapidly becomes a problem as

Gap spacings in powdered-material cores are so small that EMI is seldom a problem as long as the core is a toroid.

the frequency approaches 300 to 400 kHz. To combat the eddy-current problem, consider switching to another core material rather than changing the core size.

Eddy current in the windings (circulating currents within the wire) can also be a problem at frequencies of 500 kHz and higher. The solution here is to select a wire thickness equal to the skin depth of copper—a value determined by the switching frequency. Litz wire (ultra-thin, multistranded wire) or windings made from pc-board traces can help reduce eddy current. Positioning these windings within the core as far as possible from the air gap also helps.

Eddy currents appear in cores that have low volumetric resistivity. Low-resistance paths in the core cause the core to behave like a length of metal in a changing magnetic field. Circulating currents in the low-resistance path dissipate power. High switching frequencies (above 100 kHz) can develop significant eddy currents in iron-powder and steel-tape cores and these currents generate a core-temperature rise (**Table 2**). Because the regulator may appear to be operating correctly, the problem can be difficult to detect.

You should settle EMI issues early in the design process, before they can affect the pc layout and component placement. Shielded inductors, for example, tend to be larger, more expensive, and more difficult to mount than unshielded types.

Electronic circuitry can often tolerate moderate levels of EMI. This is particularly true for digital circuits. Even analog circuits, if they involve general-purpose ICs such as the LM324 op amp, can often weather the noise associated with unshielded inductors. In these cases, it's worth the effort to try an unshielded bobbin-type inductor in place of a pot-core or toroid inductor. The bobbin-type unit will cost half as much and be twice as small as an electrically equivalent pot-core or toroid inductor. Bobbin inductors generate their highest magnetic fields near the ends along the axis, so point them away from sensitive nodes and mount them at 90° angles to other magnetic components.

Another point to consider when selecting inductors is the problem of EMI. The air-gap spacings in powdered-material cores are so small that EMI is seldom a problem as long as the core is a toroid or has a geometry that features a closed magnetic path. Fringe fields are much greater for core geometries that include a cut, or have a large inherent gap such as that between the ends of a bobbin inductor wound on a cylindrical core. Pot cores and other clever mechanical designs make it possible to have air gaps in the ferrite material while keeping the EMI problem minimized.

Table 2—Frequency limits for standard core materials

Frequency	Core Material
To 100 kHz	Standard iron powders and steel tape
To 200 kHz	Low-permeability, high-frequency iron powders
To 400 kHz	High-flux molypermalloy powders
To 500 kHz	Standard molypermalloy powders
To 1 MHz	Manganese-zinc ferrite
To 10 MHz	Nickel-zinc ferrite

The final problem area present is the stray interwinding capacitance in inductors with values of several millihenries and larger. This capacitance combines with the coils' inductance to form a tank circuit, which rings at the inductors' self-resonant frequency (SRF). In low-SRF coils, a sudden jump of coil current, which occurs when the power switching transistor turns on, precedes the normal linear ramp of current. Large values of stray capacitance, therefore, cause switching losses that lower the regulator circuits' efficiency.

To avoid this problem, set the SRF at least five to ten times the oscillator frequency, thereby minimizing the interwinding capacitance. You can minimize this capacitance during the toroidal-winding phase by overlapping the ends of the winding somewhat, or by leaving a gap between the winding ends rather than ending the winding with one full layer. EDN

Author's biography

Bruce D Moore is a senior member of the technical staff at Maxim Integrated Products in Sunnyvale, CA and has been with the company for the past year. Bruce defines new product needs, writes application notes, resolves customer problems, and is involved with company seminars. He holds an EET degree from Heald Engineering College (San Francisco, CA). In his spare time, Bruce enjoys chess, skiing, motorcycle road racing, and military history.

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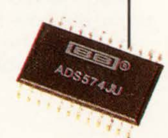

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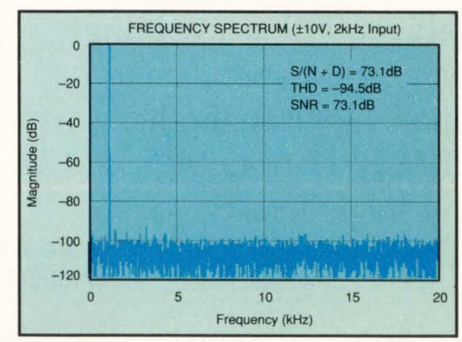

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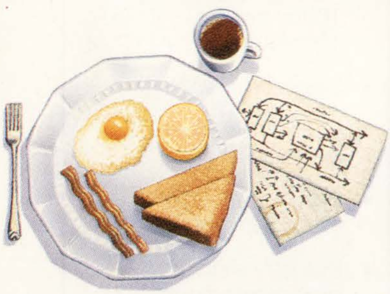

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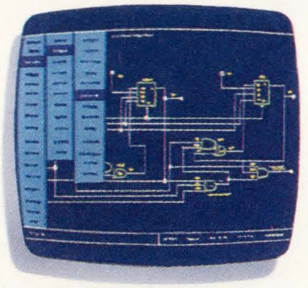

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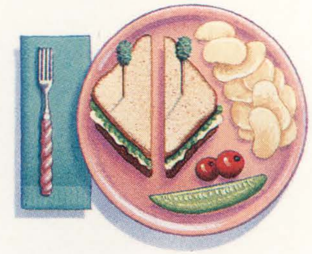

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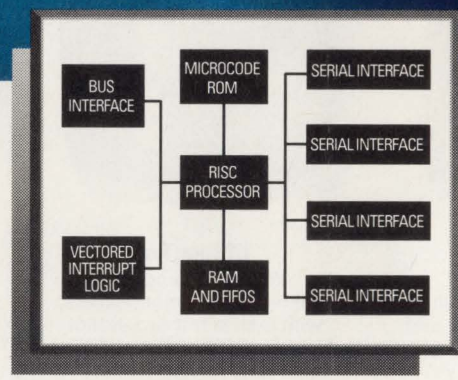

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C L O S I N G T H E G A P

An object-oriented show and tell

Chris Terry, *Associate Editor*

"Object oriented" was *the* marketing buzzword a year ago and *The Wall Street Journal* dubbed it "the computer industry's equivalent of oat bran." The term has moved beyond that to become the description of an approach to software design that is serious, important, and, above all, *practical*.

Many principles of object-oriented programming (OOP) have been around for a long time. Encapsulation, for example, has for many years meant you can hide the details of how a routine works from other routines that don't need to know (and should not be able to change) those details. Michel Floyd, manager of CAE product development at Integrated Systems Inc, comments that languages such as Modula-2 permit the encapsulation of procedures but rarely encapsulate data with those procedures, because the data has to be available to many different procedures.

When it comes time to choose an object-oriented language, you have two options: A pure language that is a complete development system you must learn, or a hybrid language that links with the system you already have.

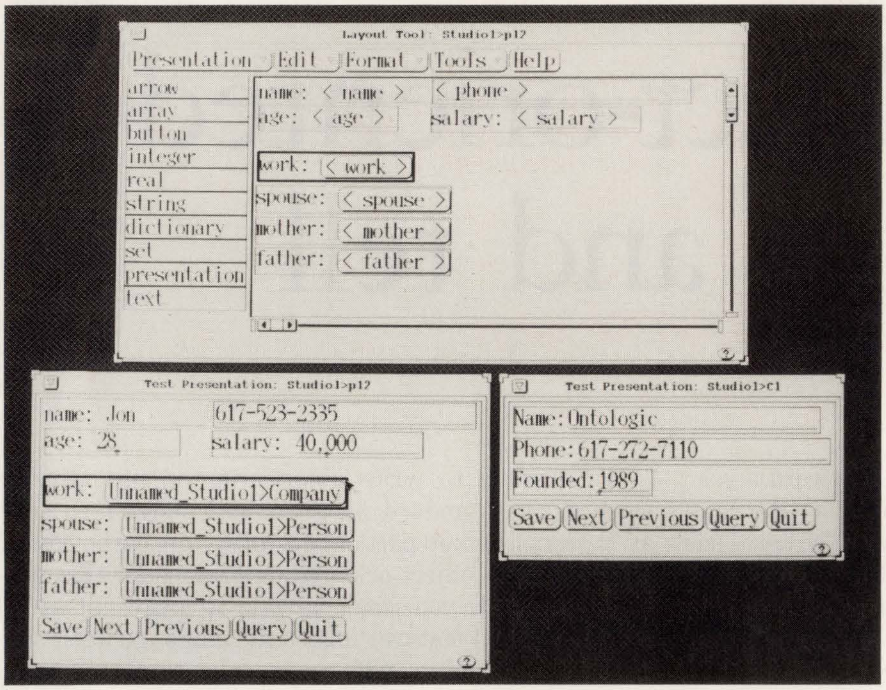
OOP demands a radically different way of thinking, however. Object A can request object B to perform some action (such as drawing itself on the screen) without object A's knowing anything about how the action will be performed. Further, you can group objects that share all or most of their attributes into a class. Floyd comments that in the fields of simulation and modeling, object-oriented principles make it relatively easy to mimic objects and phenomena of the real world, and that these principles enforce clarity of thought. Floyd cautions, however, that it takes most people six to eight months to learn to think in object-oriented terms.

It's possible to write object-oriented programs in some of the standard programming languages such as C, which is not particularly easy, or Turbo Pascal 5.5, which has object-oriented extensions for that purpose. However, you won't be able to make full use of object-oriented features unless the language itself supports them. Purists will recommend that you use a "pure" object-oriented language, such as Smalltalk/V or Eiffel. These complete development systems include an editor, a syntax checker, a browser, and a class library. The class library contains most of the objects and classes that you're likely to need for general application programs. The editor and syntax checker and, indeed, the nature of the languages themselves, combine to guide you into good OOP practices and signal any gross violations of OOP principles. Thus, they are very helpful to the novice.

These integrated systems have several disadvantages, however. One of them is the need to learn a new programming language; another is the general opinion that Smalltalk is better suited to small projects than to large ones. Further, Smalltalk does not make it particularly easy for you to interface to programs that were written in another language. Eiffel does have some facilities for interfacing to other languages, but they are not as comprehensive as the facilities of C++.

OOP purists tend to sneer at hybrid languages, such as C++ and Turbo Pascal with Objects. Nevertheless, hybrids have the advantage of a relatively simple tran-

Object-oriented programming has become an approach to software design that is serious, important, and above all, practical.



You can interactively develop screens *for presenting Ontos database information with Ontos Studio from Ontologic. Screens are objects, and therefore, you can reuse a screen in many applications.*

sition from the standard languages (C or Pascal) to the object-oriented extensions—at least as far as syntax is concerned. Further, the hybrids have the advantage of easy and standard links to programs in other languages, and they are less restrictive than pure OOP languages.

Jeff Kantor, manager of advanced applications development at Iconix Inc, points out that every application needs interfaces to other languages or to programs running on other machines. In cross-development systems, you need to be able to optimize some code for the development system and other code for the target system; often this requires access to the low-level routines that drive the hardware. C and C++ give you these interfaces and links very easily. Smalltalk, on the other hand, deals in higher-level abstractions and therefore encourages isolation from the hardware.

Some vendors of software-development tools for object-oriented software take no stance on the choice of language, but provide tools for both Smalltalk and C++. Parcplace Systems, for example, offers both Objectworks/Smalltalk and Objectworks/C++. Objectworks can help you create color-graphics applications for heterogeneous networks running under standard windowing systems. This integrated development system adheres to the standard conventions of Smalltalk, but has features that make it easier to create larger systems than you could do with the Smalltalk/V development tools. Also, for each version of Objectworks, Parcplace provides a set of class libraries that is available as a separate item.

But the winner is . . .

Just as C is currently the language of choice for programmers who use standard structured-analysis and structured-design methods to design all kinds of systems and application programs, so C++ is well on the way to becoming the language of choice for people who design object-oriented systems and applications.

A few months ago, you might have thought that far more development systems and tools were available for Smalltalk than for C++; this is no longer the case. **Table 1** lists almost twice as many compilers, libraries, and add-on tools for C++ as for other object-oriented languages. Although a few items on both sides may have been inadvertently omitted, the 2:1 ratio is likely to change even more heavily toward C++ during the next few months.

The significant change is in the increase of class libraries for C++. Because Smalltalk has been around for nearly 15 years, the class library that comes with Smalltalk/V is huge. However, for C++ there were, until a few months ago, only the somewhat limited AT&T Standard class library and the C++ class library produced by the National Institute of Health.

Text continued on pg 166

Manufacturers of object-oriented software-development tools

For more information on object-oriented software-development tools such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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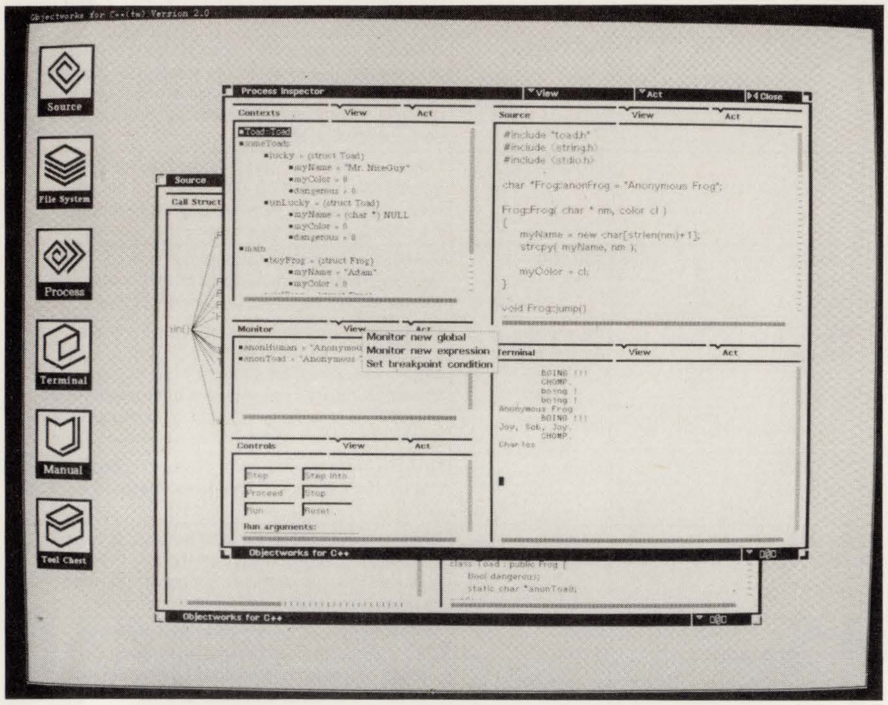
Table 1—Representative development tools for object-oriented languages

Manufacturer	Product	Host	Price	Comments
Abraxas	Code Check 2.0	MS-DOS OS/2 Mac-OS Unix	\$495 \$695 \$495 \$995	Analyzes C and C++ source code according to a set of user-defined rules.
Artifact	Class library for Smalltalk/V Mac and Presentation Manager	DOS-286, OS/2 Presentation Manager, Mac-OS	\$99.95 each volume	Each volume contains 40 to 50 classes with applications and examples. Current volumes are Magnitudes and Math; Data Structures; Graphics and Drawing; Artificial Intelligence.
Borland International	Turbo C++ Professional	MS-DOS	\$299.95	Complete development system with compiler, debugger, profiler, assembler, multifile editor, and object-oriented memory manager for expanded or extended memory.
Code Farms	Persistent Data	MS-DOS Unix	\$295 \$1195	Tool for creating object-oriented databases. Comes with interactive data browser, and royalty-free class library that includes dynamic arrays, ER models, and hash tables. Most classes supplied in source code.
Comeau Computing	Comeau C++	MS-DOS Unix	\$250 \$250	Compiler conforms to AT&T spec version 2.1. Comes with stream and iostream class libraries.
Computer Innovations	C++	80386/486 Unix systems	\$495	Conforms to AT&T spec 2.1. Comes with integrated C compiler, linker, debugger driver, SID++, source-level debugger, standard AT&T C++ class library.
Digitalk	Smalltalk/V	MS-DOS Presentation Manager Windows Mac-OS	\$499.95 \$499.95 \$499.95	Integrated development system that includes an editor, browsers, inspectors, and a large class library.
Digitalk	Add-on tools: communications extension kit; EGA/VGA color extension kit; Goodies #1 through #3 (tools and applications)	MS-DOS and 80286	\$49.95 each kit	Class libraries, inference engine, spelling checker, character-recognition neural network, and other aids.
Dyad	M++	MS-DOS OS/2 Windows Unix	\$725; with source code, \$1075	Class library for mathematical operations of all kinds, including multidimensional-array, vector, and tensor operations. Indexing facility operates on rows, planes, and large groupings.
Glockenspiel	Glockenspiel C++	MS-DOS Unix	\$495	Conforms to AT&T spec 2.0. In US, write to Imagesoft for DOS version and to Oasys for Unix version.
Hewlett-Packard Corp	C++ Softbench	HP/UX	From \$9950 per seat	Development system for object-oriented design and program development.
Iconix	Power Tools	Mac-OS	\$4995	CASE tool for Macintosh computers; handles object-oriented analysis in addition to most other CASE methodologies.
Intek	Intek C++	MS-DOS Unix/386	\$495	Conforms to AT&T spec 2.0; DOS version runs in protected mode. Compatible with a large variety of C compilers.
Intellicorp	Kappa PC	Windows	\$3500	Development system for object-oriented application programs. You can write your programs in ANSI C or in Kappa Application Language.
IDE	Software through pictures	Many systems	\$995	CASE tool that provides an Object-Oriented Structured Design notation. Supports all of the features of C++. Also provides interface to programs developed using ISE's Eiffel object-oriented development system.
ISE	Eiffel	Unix/386	From \$495	Development system for object-oriented software using the Eiffel object-oriented language. Includes class and system compilers, class libraries, browsers, debugger, and cross-development and -testing facilities.
Microtec	CCC68K cross-compiler	680×0 Unix systems	From \$6600	Cross-development system for object-oriented embedded applications written in C++. The compiler conforms to AT&T spec 2.1 and comes with XRAY68K C++ source-level debugger; ASM68K assembler, linker, and librarian; symbol-name inspection tool; and C++ class libraries for iostreams, complex arithmetic, and real-time operating systems.

Manufacturer	Product	Host	Price	Comments
Microway	NDP C ++ 386	MS-DOS	$995	Native compiler; conforms to AT&T spec 2.0. Supports Intel, Weitek, and Cyrix math coprocessors. Provides links to NDP C, Fortran, and Pascal.
Mind's Eye	Mind's Eye	MS-DOS	From $695	Object-based software package that can link text, graphics, and data to evaluate the relationships between various aspects of any project, process, or problem. Can also be used as software-design tool.
Object Design	Objectstore	Unix	From $2000	Object-oreinted Database Management System for applications written in C or C ++. Lets you create applications to share objects among multiple users on a heterogeneous network.
Objectivity	Objectivity/DB	Sun-OS Unix	$30,000	Development system for object-oriented database management systems on networked workstations from multiple vendors.
Object Technology International	Envy/Developer	MS-DOS Netware	$12,000 for 3-user system	Development system for embedded systems written in Smalltalk/V. Allows a project team to work concurrently on different parts of the same projects. Library systems track both source and object code and protect completed classes and applications from accidental changes.
Objectvision	Objectvision	MS-DOS	$399	CASE tool for the design of object-oriented programs. Generates C ++ or Turbo Pascal 5.5 code.
Ontologic	Ontos 2.0	Sun-OS OS/2	$9950 for 1-user system	Development system for distributed database applications. A graphical design tool automatically generates C ++ header files and database schemata.
Oregon Software	Oregon C ++	80386 Unix and Sun-3	$895 $1700	Native compiler that compiles directly from C ++ source without translation to ANSI C. Comes with source-level debugger compatible with C ++, ANSI C, and K&R C.
Parcplace Systems	Objectworks\C ++ and Objectworks\Smalltalk	Sun-OS, Windows	$3500 $3500	Integrated development system to help C ++ designers. Conforms to AT&T spec 2.1. Comes with a graphical source browser and visual debugger; allows you to use traditional Unix tools as well as the optional Objectkit\C ++ class libraries.
PMI	Data ++ Windows	MS-DOS	$189	Library containing more than 160 classes for development of user interfaces. Works with a variety of C ++ compilers.
Saber Software	Saber C ++	Unix	$3995 for single user	Compiler conforms to AT&T spec 2.1. Comes with source-level debugger and class, cross-reference, data, and program browsers, Can be used with IDE's Software through Pictures.
Servio Corp	Facets	Sun-OS	$1000	Collection of object-oriented tools to help programmers in the development of Objectworks/Smalltalk applications. Includes complete source code and an on-line, context-sensitive help system. Includes schema designer, forms designer, report writer, and menu builder.
Zinc Software	Zinc Interface Library	MS-DOS OS/2 Windows	$200	Class library for C ++ applications. Provides event-manager and window-manager classes, together with complete help and error systems.
Zortech	Zortech C ++	MS-DOS Unix	$450	Native compiler for 80386-based computers running MS-DOS or Unix. Conforms to AT&T spec 2.1. Developer's edition includes C and C ++ compilers, C ++ debugger, C ++ Tools, and source code for the class library.

Object-oriented programming demands a radically different way of thinking—it takes most people six to eight months to learn to think in object-oriented terms.



This process inspector provides five views *(in separate windows) of your C++ code and classes. With Objectworks/C++, you can resize any or all of the windows.*

The picture is quite different today because there now are not only C++ class libraries organized along the lines of the Smalltalk library but also some useful specialist class libraries (**Ref 1**).

The predominance of C++ is further confirmed by the fact that several major CASE tool vendors have announced plans to integrate existing or upcoming C++ development systems into their CASE tool frameworks. For example, Interactive Development Environments is forming an alliance with Saber Software so that Software through Pictures will support not only Saber C but also Saber C++. Cadre, too, is allying itself with Saber so that the Teamwork tools will facilitate the design of object-oriented systems that will be implemented with the aid of the Saber C++ development tools.

Not to be outdone, Hewlett-Packard is offering a C++ version of its Softbench framework that will support object-oriented design and program development on all HP computers that run under HP/UX (HP's version of Unix). The C++ Softbench package consists of Framework LSI (a tool that allows diverse third-party tools to work together on a heterogeneous network), Encapsulator (for adapting individual tools to the Softbench framework), a class and object builder, a browser for finding and examining classes, a static analysis tool, and a graphics editor.

Another indication of the trend toward C++ is that several object-oriented database managers not only provide an interface to related application programs written in C++, but are themselves written in that language. Objectdesign's Objectstore is a typical example of such ODBMS (object-oriented database management system) packages. It can handle persistent data as fast as transient data, and it provides a DML (data manipulation language) preprocessor that is based on the AT&T *cfront* C++ preprocessor. Objectdesign has signed a strategic alliance with Saber Software to integrate Objectstore with both Saber C and Saber C++.

Objectdesign's DML preprocessor supports parameterized types—that is, a system of templates designed by AT&T's Bjarne Stroustrup for defining container classes. These templates make it easier to design libraries of safe and reusable code—an important step toward wider use of standard software libraries. The ANSI X3J16 subcommittee has decreed that parameterized types will be part of the initial C++ standard. Also, AT&T has announced that it has licensed Objectdesign's implementation of parameterized types for inclusion in C++ Release 3.0. This inclusion of a ready-made mechanism in the compiler will help to accelerate wide distribution of the technology throughout the C++ community.

Another vote for C++ was cast at the OOPSLA

There seems to be no lack of proposed notations for object-oriented design. The trouble is that few of them agree with each other.

1990 conference, when Objectivity Inc announced that its Objectivity/DB engineering-database management system would support Hewlett-Packard's C++/Softbench for the development of applications to run on HP 9000 workstations.

And finally, Ontologic's Ontos 2.0 ODBMS, which runs on Sun, Apollo, DEC, and high-end 80386-based computers, is written in C++, supports multiple inheritance, and supports data distribution across networks. The package includes a development tool that automatically generates both C++ header files and database schemata, and a graphical browser that allows you to perform interactive inspection and maintenance of the database.

Just in CASE . . .

Although most modern CASE tools let you use a variety of methodologies, each with its own conventions for graphical notation, no standard notation has yet emerged for object-oriented design. You can use one of the standard notations, such as Yourdon/DeMarco, Hatley/Pirbhai structured design for real-time systems, or Chen Entity Relationship diagrams for databases. But these do not always entirely meet your object-oriented needs.

There seems to be no lack of *proposed* notations for object-oriented design. The trouble is that few of them agree with each other. Fewer still have powerful enough backing to ensure widespread adoption. Meilir Page-Jones began a recent article (**Ref 2**): "Last week we went to an object-oriented symposium . . . where we met a most unusual software engineer. He didn't have his own object-oriented design notation!"

However, there are two proposals from sources prestigious enough to ensure serious attention: one comes from Meilir Page-Jones, Larry Constantine, and Steven Weiss (**Ref 2**); the other from Anthony J Wasserman and his colleagues at IDE (**Ref 3**). It's very doubtful if either of these notations (or any other, for that matter) will become the sole standard. Most likely, several notations will eventually obtain sufficient acceptance to be regarded as de facto standards for particular types of applications. This will duplicate the situation in the structured-analysis/design field, in which engineers and organizations adopt the methodology and notation that best suits their ways of thinking and the kind of work they are doing.

Meanwhile, more and more engineers keep coming up with ideas (some half-baked, others very mature and practical). A good sign for the maturation of object-oriented technology was the formation of the Object Management Group (OMG), quartered in Framingham, MA. This organization now has more than 80 members drawn from systems vendors, software developers, and software users. November 1990 saw the publication of OMG's Object Management Architecture Guide, which provides a complete architectural overview of an object-oriented environment and the major interfaces necessary to facilitate interoperability and extensibility. The guide includes a glossary of the terms used. Because this guide was the collaborative effort of many OMG members, there is hope that OMG will have a screening and stabilizing influence that may lead to the development of common ways of looking at objects and common ways of implementing methods. Until there is wide acceptance of relatively standard approaches, there is little hope of achieving any large body of genuinely machine-independent and reusable code. **EDN**

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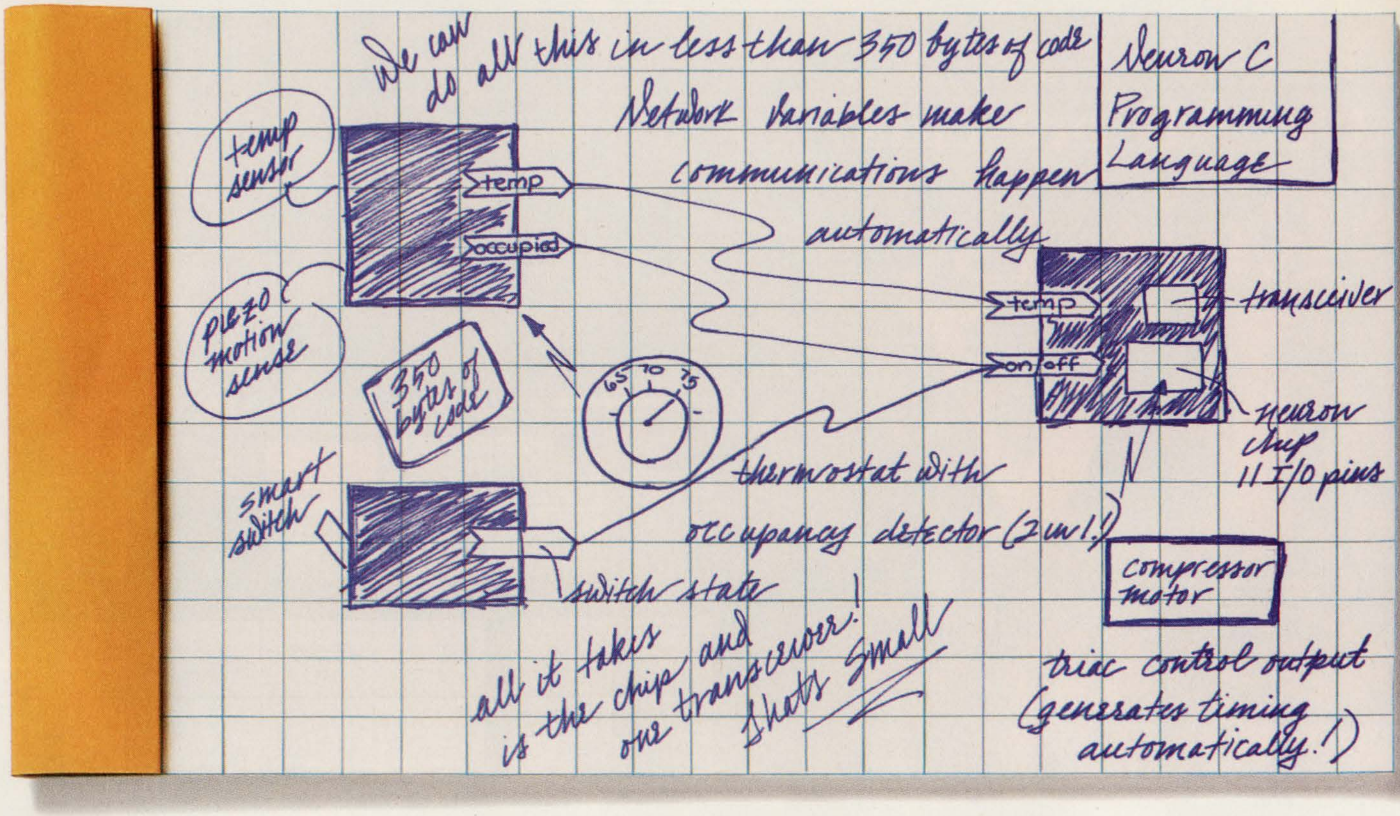
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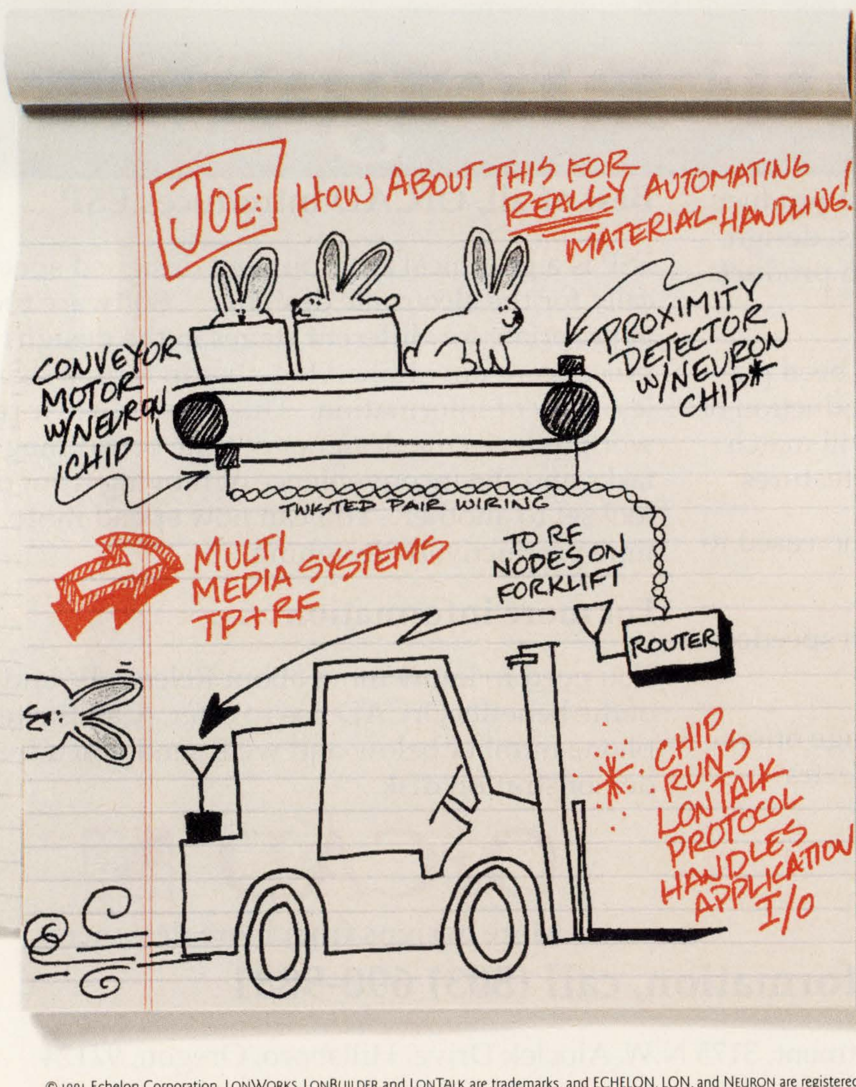
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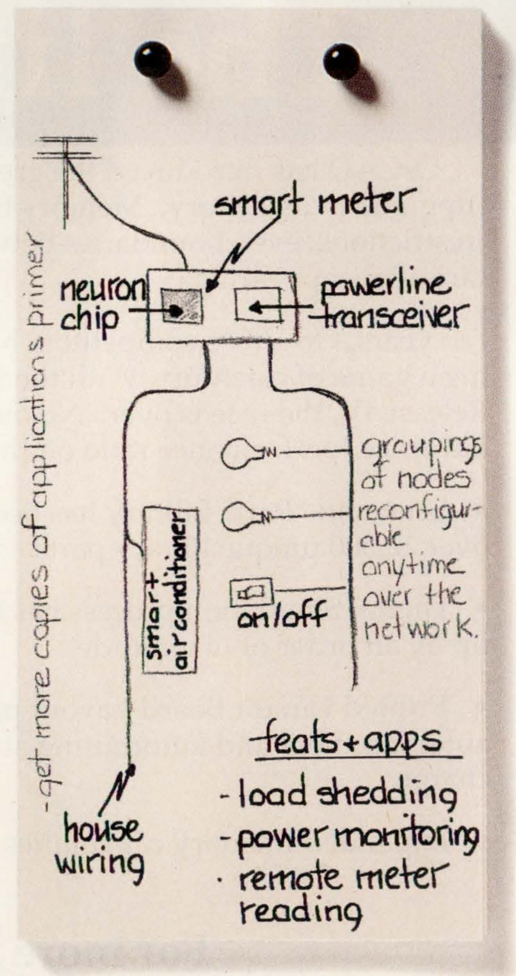
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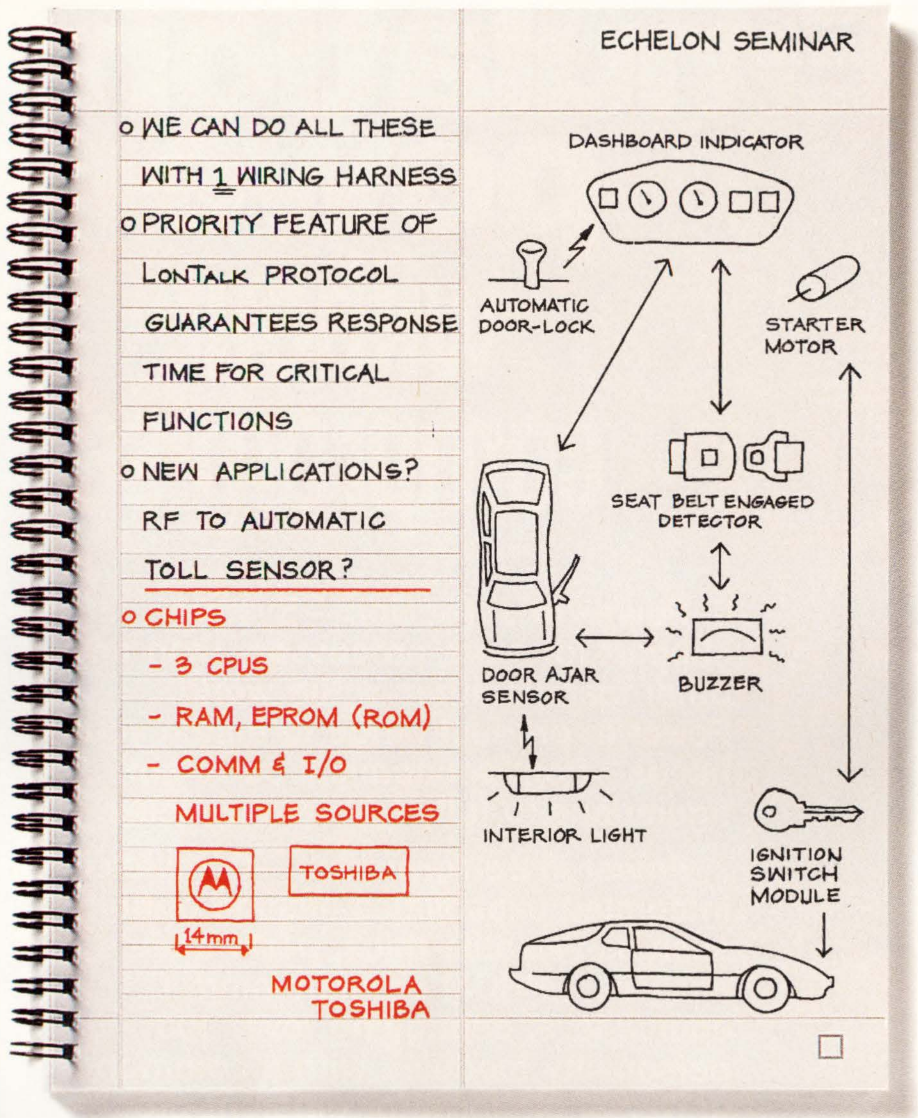

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CIRCLE NO. 206

EDITED BY ANNE WATSON SWAGER

Multiplier lowers impedance

Ian Hickman
Ian Hickman Partners, Waterlooville, UK

The Cockcroft-Waton voltage multiplier (**Fig 1a**) can produce a large negative voltage—hundreds of kilovolts—where the peak voltage across each diode and capacitor equals the p-p input voltage. However, for lower voltage applications—as low as a hundred volts—some disadvantages predominate. **Fig 1a**'s circuit exhibits a high-output impedance due to the small effective capacitance of the series-connected capacitors, and it exhibits considerable voltage loss due to all of the diode drops. Further, this circuit requires 2n diodes and 2n capacitors to produce a dc output voltage approximately n times the rail voltage.

Fig 1b's circuit multiplies more effectively using fewer diodes and capacitors. The parallel arrangement of the capacitors lets you use smaller capacitors than those required in **Fig 1a**. Alternatively, when using the same capacitor values of **Fig 1a**, the output impedance will be lower. Second, whereas the clock source directly drives only one of the two strings of capacitors in **Fig 1a**, **Fig 1b**'s clock drives both strings with opposite phases. This drive scheme doubles the voltage per stage of two diodes. A final diode is necessary to pick off the dc output voltage because both strings of capacitors now carry the p-p ac input-voltage waveform. The ICL7667 dual-FET driver accepts a TTL drive swing and provides a low-impedance push-pull drive to the diode string. This low impedance is particularly helpful when using a long string to raise output voltage to more than 100V starting from a low rail voltage.

Fig 1b requires n+1 diodes and n+1 capacitors to output a nominal voltage equal to n times the rail voltage. Using a rail voltage of 5V, **Fig 1b** requires less than half the number of **Fig 1a**'s diodes and capacitors because of the improved circuit's increased output per stage resulting from fewer numbers of diode forward-voltage drops in the circuit. To use **Fig 1b** to produce a positive output, reverse the polarities of the capacitors and diodes and tie the anode of D_1 to the positive rail. Such a positive-output circuit can produce 45V from a 15V input using three capacitors and three diodes—n=2. **(EDN BBS /DI_SIG #966)** EDN

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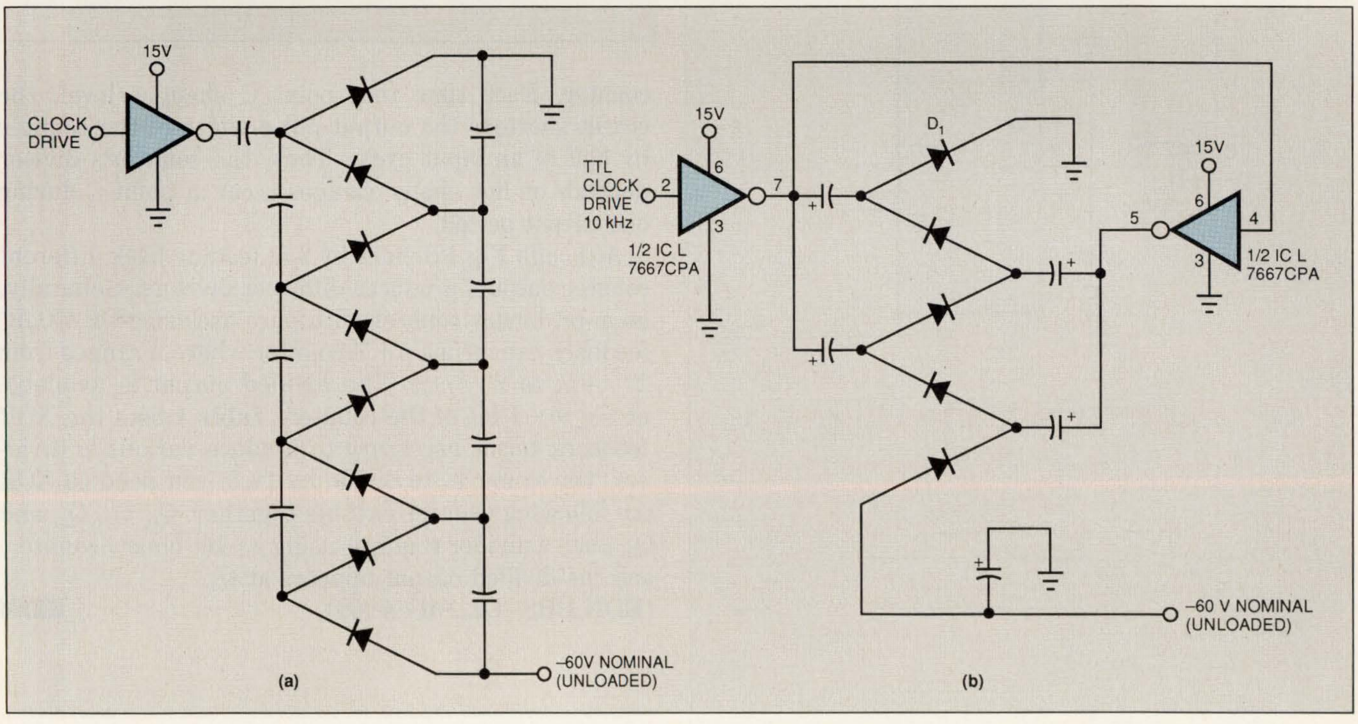

***Fig 1—The multiplier in b improves** upon the conventional circuit in **a** by exhibiting lower impedance and by requiring fewer capacitors—or alternatively, smaller valued capacitors—and fewer diodes.*

Divider splits the divisor

Yongping Zia
Department of Electrical Engineering, West Virginia University, Morgantown, WV

Fig 1 is yet another variant of a standard digital divider. This circuit, instead of dividing by an integer, divides the input signal by n + ½. With the feedback connections exactly as **Fig 1** shows, the circuit divides by 3.5. Point C in **Fig 1** ultimately controls when the input clocks the 74HC161 4-bit counter. When C = 0, the positive edge of the input triggers the counter. If C = 1, the negative edge of the input triggers the counter. Each time that point C changes level, the circuit shortens the output pulse width of the counter by half of an input cycle. Thus, the counter's divisor depends on how many changes occur at point C during one output period.

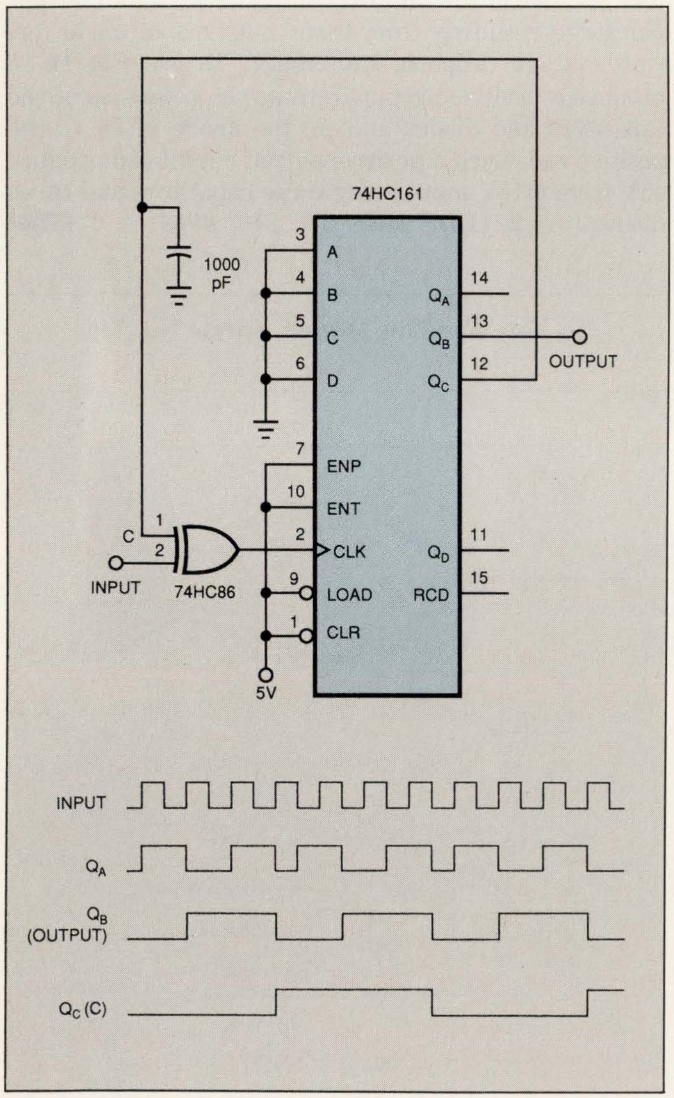

***Fig 1—Feeding back counter outputs** and XORing them with the input produces a counter that divides by n + ½.*

Table 1—XOR feedback signals for N + ½ divider

Divide number	Feedback signal(s)			
N = 1.5	Q_1			
N = 2.5	Q_0	Q_2		
N = 3.5	Q_2			
N = 4.5	Q_0	Q_3		
N = 5.5	Q_0	Q_1	Q_3	
N = 6.5	Q_1	Q_3		
N = 7.5	Q_3			
N = 8.5	Q_0	Q_4		
N = 9.5	Q_0	Q_2	Q_4	
N = 10.5	Q_0	Q_1	Q_2	Q_4
N = 11.5	Q_0	Q_1	Q_4	
N = 12.5	Q_1	Q_4		
N = 13.5	Q_1	Q_2	Q_4	
N = 14.5	Q_2	Q_4		
N = 15.5	Q_4			
N = 16.5	Q_0	Q_5		
N = 17.5	Q_0	Q_3	Q_5	
N = 18.5	Q_0	Q_2	Q_3	Q_5
N = 19.5	Q_0	Q_2	Q_5	
N = 20.5	Q_0	Q_1	Q_2	Q_5

Although **Fig 1** divides by 3.5, feeding back different counter outputs produces different divisors. Generally, an m-bit binary counter with pure exclusive-OR (XOR) feedback can form a n + ½ counter where n ranges from $2^{m-2} + ½$ to $2^{m-1} - ½$. The divided output is available at the m − 1 bit of the counter. **Table 1** lists the XOR feedback terms necessary to produce various ½ dividers. For example, to divide by 18.5, you need to XOR the following counter outputs together: Q_0, Q_2, Q_3, and Q_5. Such a divider requires using a 6-bit binary counter, and the divided output appears at Q_4.

(EDN BBS /DI_SIG #968) EDN

To Vote For This Design, Circle No. 747

8051 μC converses with dual-port RAM

Brady Barnes
Inter-Tel Inc, Chandler, AZ

Interfacing an 8051 microcontroller to a dual-port RAM poses some problems that a small amount of glue logic can solve (**Fig 1**). The main problem has to do with the busy signal, $\overline{\text{DPR\_BZ}}$, that the dual-port RAM generates. When the 8051 attempts to access a location in the RAM that is currently being accessed by another processor, the RAM asserts the $\overline{\text{DPR\_BZ}}$ signal to alert the 8051 that it must wait until the other processor's access is complete. Unfortunately, the 8051 can't wait because it doesn't provide for asynchronous bus control. External gating (**Fig 1**) and some extra software are necessary for proper communication between the two devices. The 8051's RAM-access code is simple (**Listing 1**). The 8051 software checks the status of the busy signal, and if the RAM is busy, the software tries again to access the location.

Listing 1—8051 to dual-port RAM interface code

```
LOOP1  MOVX  @DPTR, A        Write a byte of data to the
       JB    P3.1, LOOP1     DPR. Was the DPR busy? If it
                             was busy, try again.

LOOP2  MOVX  A, @DPTR        Read a byte of data from the
       JB    P3.1, LOOP2     DPR. Was the DPR busy? If it
                             was busy, try again.
```

The new circuitry and software must meet two objectives. When the RAM asserts the busy signal, the 8051 must first recognize the busy signal, and then not write to the RAM accidentally. The busy signal generated by the RAM is not a latched signal. Thus, depending on the timing of the two processors that access the RAM, the busy signal can last from ten or

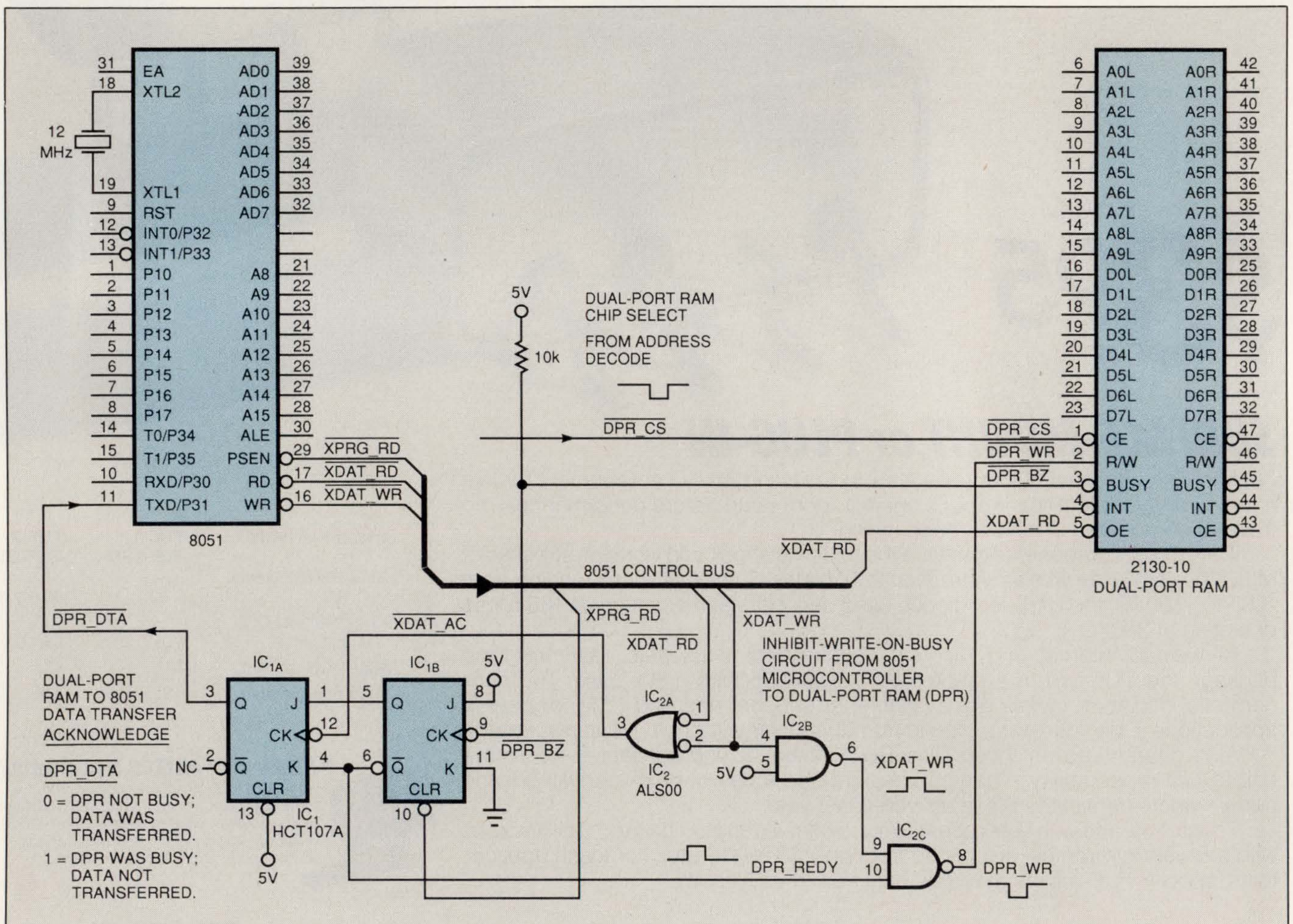

***Fig 1—Glue logic and software enable** an 8051 microcontroller to interface with a dual-port RAM properly.*

LINEAR TECHNOLOGY
DESIGN NOTES

Gain Trimming In Instrumentation Amplifier Based Systems – Design Note 51

Jim Williams

Gain trimming is almost always required in instrumentation amplifier based systems. Gain uncertainties, most notable in transducers, necessitate such a trim.

Figure 1, a conceptual system, shows several points as candidates for the trim. In practice, only one of these must actually be used. The appropriate trim location varies with the individual application.

Figure 2 approaches gain trimming by altering transducer excitation. The gain trim adjustment results in changes in the LT1010's output. The LT1027 reference and LT1097 ensure output stability. Transducer output varies with excitation, making this a viable approach. It is important to consider that gain "lost" by reducing transducer drive translates into reduced signal-to-noise ratio. As such, gain reduction by this method is usually limited to small trims, e.g. 5-10%. Similarly, too much gain introduced by this method can cause excessive transducer drive, degrading accuracy. The transducer manufacturer's data sheet should list the maximum permissible drive for rated accuracy.

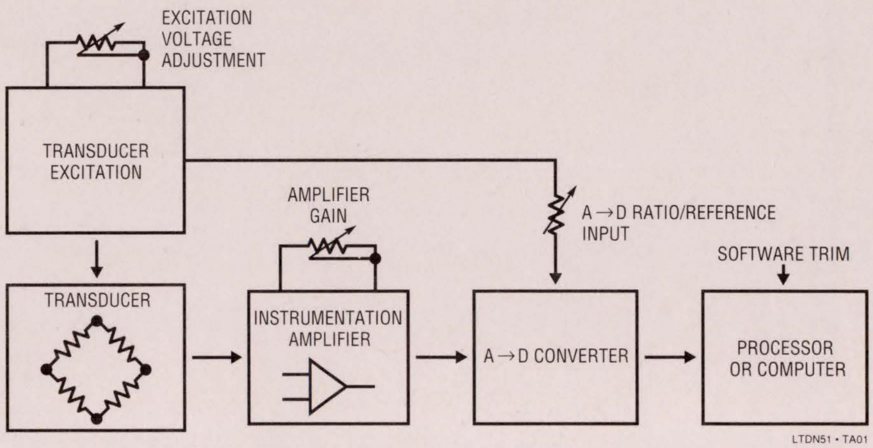

Figure 1. Conceptual Transducer Signal Conditioning Path Showing Gain Trimming Possibilities. In Practice, Only One Adjustment Is Required.

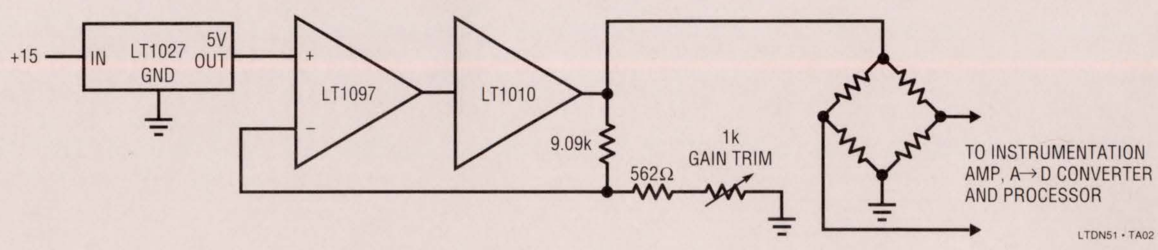

Figure 2. Gain Trimming by Adjustment of Transducer Excitation. This Method is Useable for Small (5-10%) Trims. Large Trims Will Cause Excessive Transducer Power Dissipation or "Starved" Outputs.

Figure 3 adjusts gain in the instrumentation amplifier stage. The fixed gain LT1101 instrumentation amplifier feeds a second amplifier where the trim occurs. As both cases show, the gain trim may be up or down. A secondary benefit of this trim scheme is that it permits optional offset summing and filtering. Note that either the inverter or follower may be set up for gain addition or reduction. The sole limitation is the signal polarity reversal imposed by the inverter case. This may be corrected by reversing the instrumentation amplifiers' inputs.

A final hardware based gain trim is shown in Figure 4. Here, the A→D reference input is scaled to the appropriate voltage by the op amp and associated components. The op amp input is usually the transducer excitation voltage or, in cases where this is not possible, a reference.

One final way to trim gain is in software. If a processor is involved in the system this is a viable alternative. The software trim does a simple code conversion on the A→D output. When using this approach utilize as much of the analog components' dynamic range as possible to avoid signal-to-noise degradation.

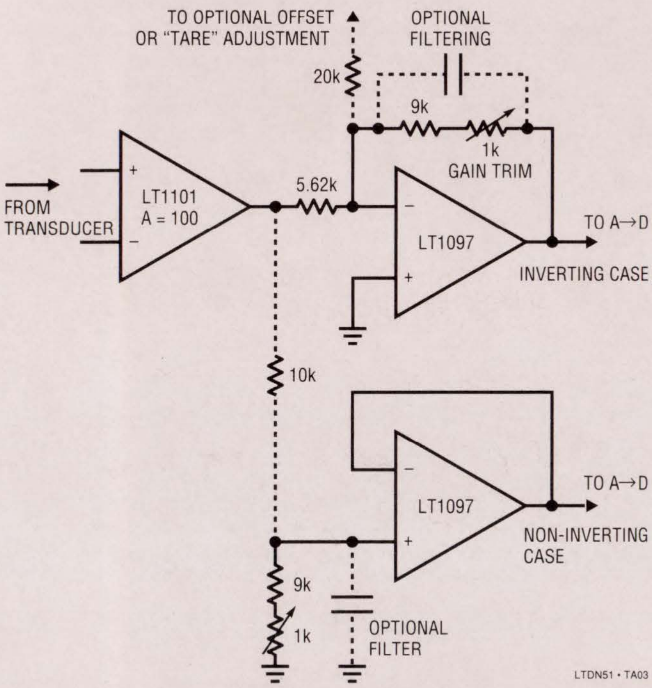

Figure 3. Gain Trimming at the Instrumentation Amplifier. A Second Stage Permits Trimming Gain Up or Down, and Allows Filtering and Offsets to Be Summed In.

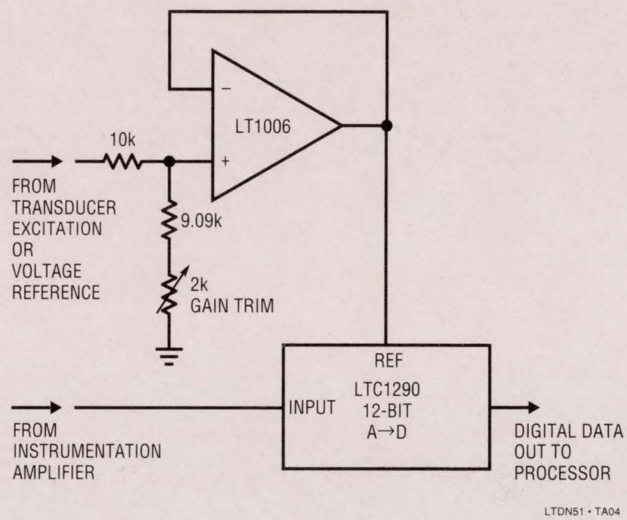

Figure 4. Gain Trimming By Adjustment of the A→D Reference Input Voltage

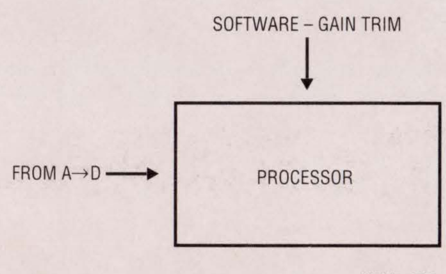

Figure 5. Software Based Trimming

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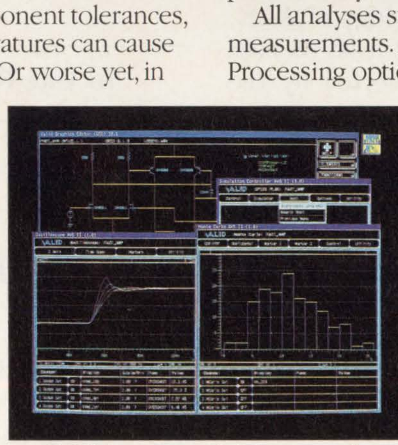
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twenty to as long as hundreds of nanoseconds. The busy signal's active time will never be the same for each access contention.

The interface circuit must latch this busy signal. The flip flop, IC_{1B}, serves this purpose. To simplify the software and make accesses to the RAM as fast as possible for the 8051, the μC must clear IC_{1B} just prior to accessing the RAM. To accomplish this task, the 8051 must fetch an opcode from external memory, which causes the 8051's PSEN to strobe low. (PSEN is equivalent to $\overline{\mathrm{XPRG\_RD}}$ in the glue-logic circuit. The mnemonic, XPRG_RD, stands for external program memory read.) Strobing PSEN low clears the flip flop, which is now armed and waiting for the busy signal to assert itself.

Once IC_{1B} clears, the 8051 can access the RAM, which to the controller looks like external data memory. This access causes the address decoder to assert the chip-enable signal, $\overline{\mathrm{DPR\_CS}}$. After $\overline{\mathrm{DPR\_CS}}$ goes low, the RAM will assert $\overline{\mathrm{DPR\_BZ}}$ within 50 nsec if there is contention for the memory location.

If contention occurs, the busy signal immediately sets IC_{1B}. Because $\overline{\mathrm{DPR\_CS}}$ depends solely on address decoding, the time between recognition of a valid address and the busy-signal assertion is $103+50=153$ nsec. Allowing for another 54 nsec for the signal to propagate through the flip flop, the output of that IC_{1B} will then respond within 207 nsec after the RAM's address becomes valid.

The address is valid 43 nsec before the negative edge of ALE. Thus, the output of IC_{1B} when clocked by $\overline{\mathrm{DPR\_BZ}}$ will be valid within 164 nsec ($207-43$ nsec) after the negative edge of ALE. The $\overline{\mathrm{XDAT\_WR}}$ and $\overline{\mathrm{XDAT\_RD}}$ signals from the 8051 aren't asserted for at least 200 nsec after the negative edge of ALE. Thus, the output of IC_{1B} will be valid at least 36 nsec *before* $\overline{\mathrm{XDT\_RD}}$ or $\overline{\mathrm{XDAT\_WR}}$ are asserted by the 8051. It is important that IC_{1B}'s output be valid before these two XDAT signals become active for two reasons: Together, they form the clock signal that transfers IC_{1B}'s state to IC_{1A} and they work to inhibit a write command to the RAM if the busy signal is active.

The circuit transfers the state of IC_{1B} to IC_{1A} on the negative edge of either XDAT signal. This transfer of the busy status is necessary because $\overline{\mathrm{XPRG\_RD}}$ clears IC_{1B} shortly after $\overline{\mathrm{DPR\_CS}}$ goes high. The busy status can now be read by the 8051 through one of its ports.

To prevent an accidental write to the RAM, the 8051 must first access the write location *without* asserting the $\overline{\mathrm{DPR\_WR}}$ signal by asserting only the $\overline{\mathrm{DPR\_CS}}$ signal. If the RAM asserts the busy signal at this point, the output of IC_{1B} will block the $\overline{\mathrm{DPR\_WR}}$ signal via NAND gate IC_{2C}, and thereby prevent a write to the RAM.

If the RAM isn't busy, the $\overline{\mathrm{DPR\_WR}}$ signal must *not* experience a delay of more than 33 nsec in order to meet the data hold time of the RAM. The hold time of the 8051 is 33 nsec, and the required hold time of the RAM is 0 nsec. Thus, the circuit can have up to a 33-nsec delay of $\overline{\mathrm{XDAT\_WR}}$ and $\overline{\mathrm{DPR\_WR}}$ and still meet the hold time of the RAM. The $\overline{\mathrm{WR\_}}$ signal passes through two levels of NAND gates. The circuit uses ALS logic to meet the write timing requirement. Using HC or HCT logic will not meet the 33-nsec delay requirement. However, either FAST, ACT, or ALS logic is fast enough.

Note that because this interface circuit uses the external-program-read signal from the 8051, the 8051 code that accesses the dual-port RAM must reside in external memory. **(EDN BBS /DI_SIG #969)** **EDN**

To Vote For This Design, Circle No. 748

Duty-cycle chopper controls lamp

Ronald Doctors
GMI Inc, Santa Barbara, CA

Fig 1's high-intensity-lamp dimmer emulates a rheostat; the circuit has only two leads. To maximize the battery-powered circuit's operation time between charges, the circuit employs a PWM system. A system with duty cycles between 20 and 95% provides the necessary brightness range. **Fig 1**'s component values set the maximum duty cycle close to 100% and the minimum around 20%. The circuit is useful for applications in which the minimum duty cycle allows for energy storage, and in which efficiency is important (solar-powered lamps and motors, for example). To maximize efficiency, C_1 charges during the off time and stores enough energy to drive Q_1 and keep IC_1 operating. Because the dimmer-control circuit is in series with the lamp, all the current passes through the lamp, which improves efficiency.

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some passive components implement the PWM circuit. One half of the TLC556, R_1, R_2, and C_2 form a free-running, 1-kHz oscillator that has a very low duty cycle. This signal triggers a one-shot comprising the other half of the TLC556, R_3, R_4, the 100k potentiometer, and C_3. Q_1 and Q_2 provide the saturated output drive. These transistors can carry 1A with a V_{CE}(SAT) of 0.25V. Thus, no heat sinking is required. D_1 prevents Q_2 from dumping charge onto C_1 when Q_2 is on. **(EDN BBS /DI_SIG #967)**

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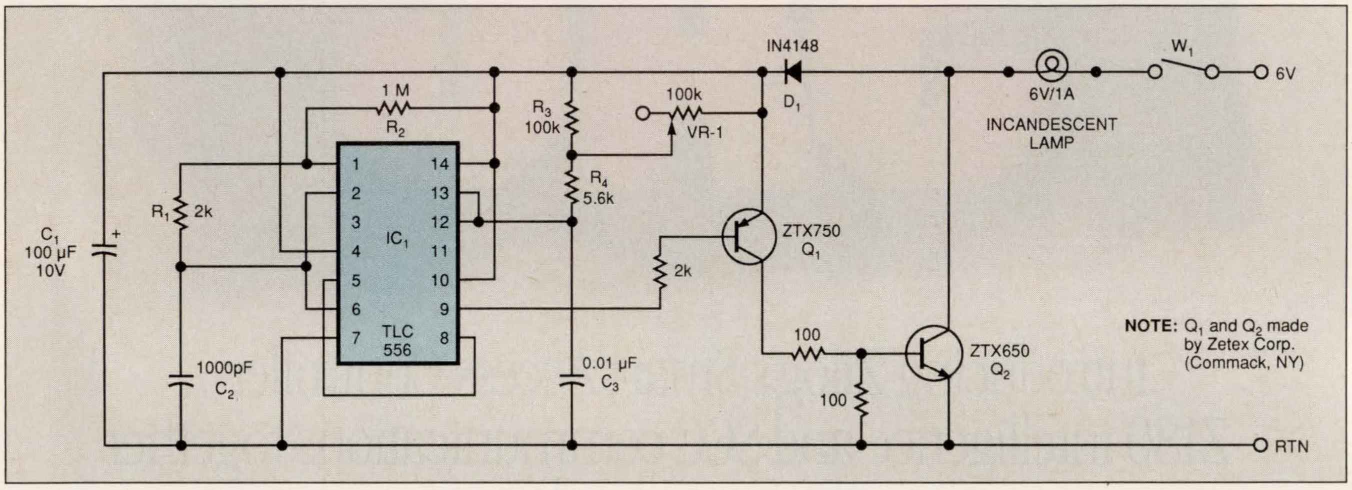

Fig 1—IC_1, a CMOS 555 timer, and associated components form a PWM circuit that adjusts the duty cycle of this lamp dimmer between 20 and 100%.

Current source scrounges parts

Philip Leong
Department of Electrical Engineering, University of Sydney, Sydney, Australia

Fig 1 uses readily available parts to implement a 0-to 200-nA current source. The circuit borrows a PMOS transistor from the input stage of a CD4007A, a device easier to obtain than a discrete PMOS transistor. The CA3130 op amp operates as a follower so that its positive input sets the current that flows through R_2. The MOSFET input stage of this op amp exhibits low-input current. The op amp must be able to produce an output voltage high enough to turn the CD4007A's internal FET off. Thus, the op amp requires a positive supply voltage of 5V. The circuit presents an output voltage from 0 to 3V, and R_1 controls the amount of output current. **(EDN BBS /DI_SIG #970)**

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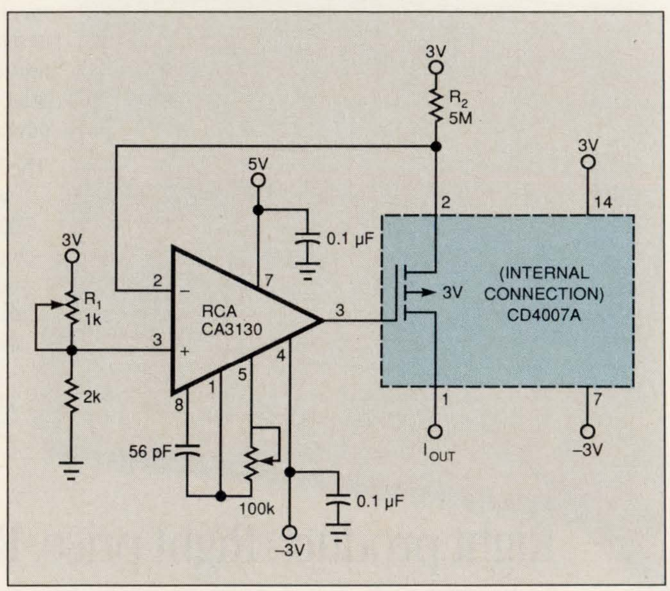

Fig 1—This low-drift current source makes use of an input PMOS transistor inside a readily available CD4007A.

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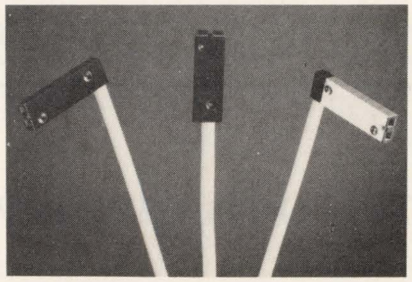

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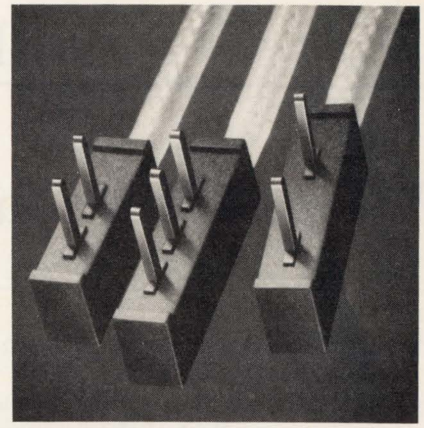

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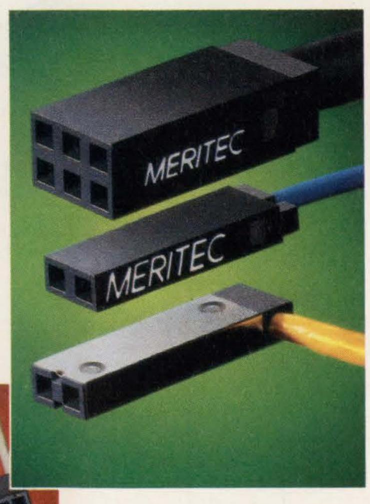

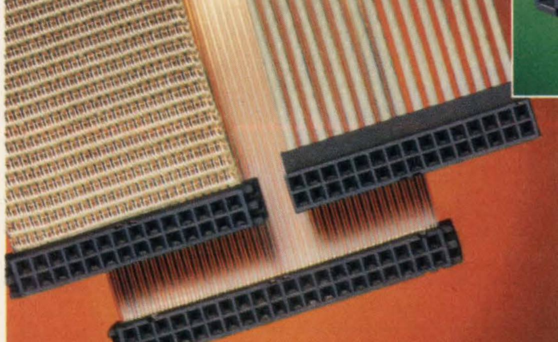

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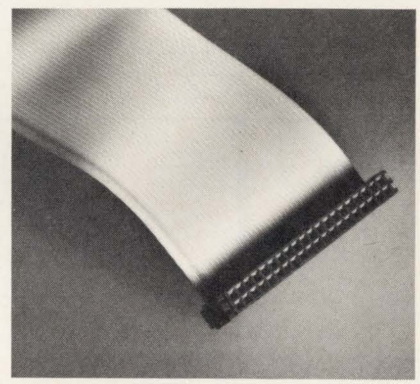

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- *High strength molded terminations*
- *Controlled impedance*

Meritec's Multi-Signal Interconnects (MSI™) can be terminated to FEP, PTFE or Filatex™ textile cable. Precision, high strength molded terminations assure high reliability in critical applications. The assemblies offer controlled impedance and low crosstalk. Standard impedances are available from 50 to 95Ω. EMI/RFI shielding is optional. The connectors are compatible with latch and eject headers and are available in high or low profile configurations. The high profile configuration is available with pull tabs.

CIRCLE NO. 173

Phase shifter adapts to frequency changes

Ion Constantinescu
B&C Microsystems Inc, Sunnyvale, CA

Fig 1's circuit adds 120 degrees of phase shift to a 50- or 60-Hz input regardless of the frequency and amplitude fluctuations of that input. The circuit configures a 2N4093 JFET as a voltage-controlled resistor whose value is proportional to the phase difference between the input and the output. The values of C_1, R_1 and r_{DS} determine the amount of phase shift, 120° in **Fig 1**'s case.

A 555 timer implements a phase detector whose two inputs are related to the input and output. The input and output, respectively, drive IC_{1B} and IC_{1C}, which operate as zero-crossing detectors. D_1 and D_2 limit the positive-going pulses at the 555 inputs. Thus, the falling edges of IC_{1B} and IC_{1C}'s outputs control the 555 timer. The timer's output signal stays low for a time proportional to the phase shift between the circuit's input and output.

The average value of the timer's output and an offsetting voltage drive IC_{1D}. R_2 and C_2 filter IC_{1D}'s output. The resultant signal controls the JFET. The potentiometer sets the control at a value for which the phase shift between input and output is equal to 120 degrees when the input signal frequency is 50 or 60 Hz. Any differences between the input and output changes the 555 output's average value, thus ultimately modifying the control voltage and the JFET's resistance.

To calibrate the circuit, apply a 50-Hz sine wave with an amplitude less than $1V_{p\text{-}p}$ to the input and adjust the potentiometer until the phase shift reads 120° on a digital phase meter. For input frequency variations between 40 and 60 Hz, the phase shift changed by a maximum of ±0.17%, which is equivalent to an offset of only 0.02 °/Hz. The average value at IC_{1D}'s noninverting input is 3.864V.

(EDN BBS /DI_SIG #959) EDN

To Vote For This Design, Circle No. 745

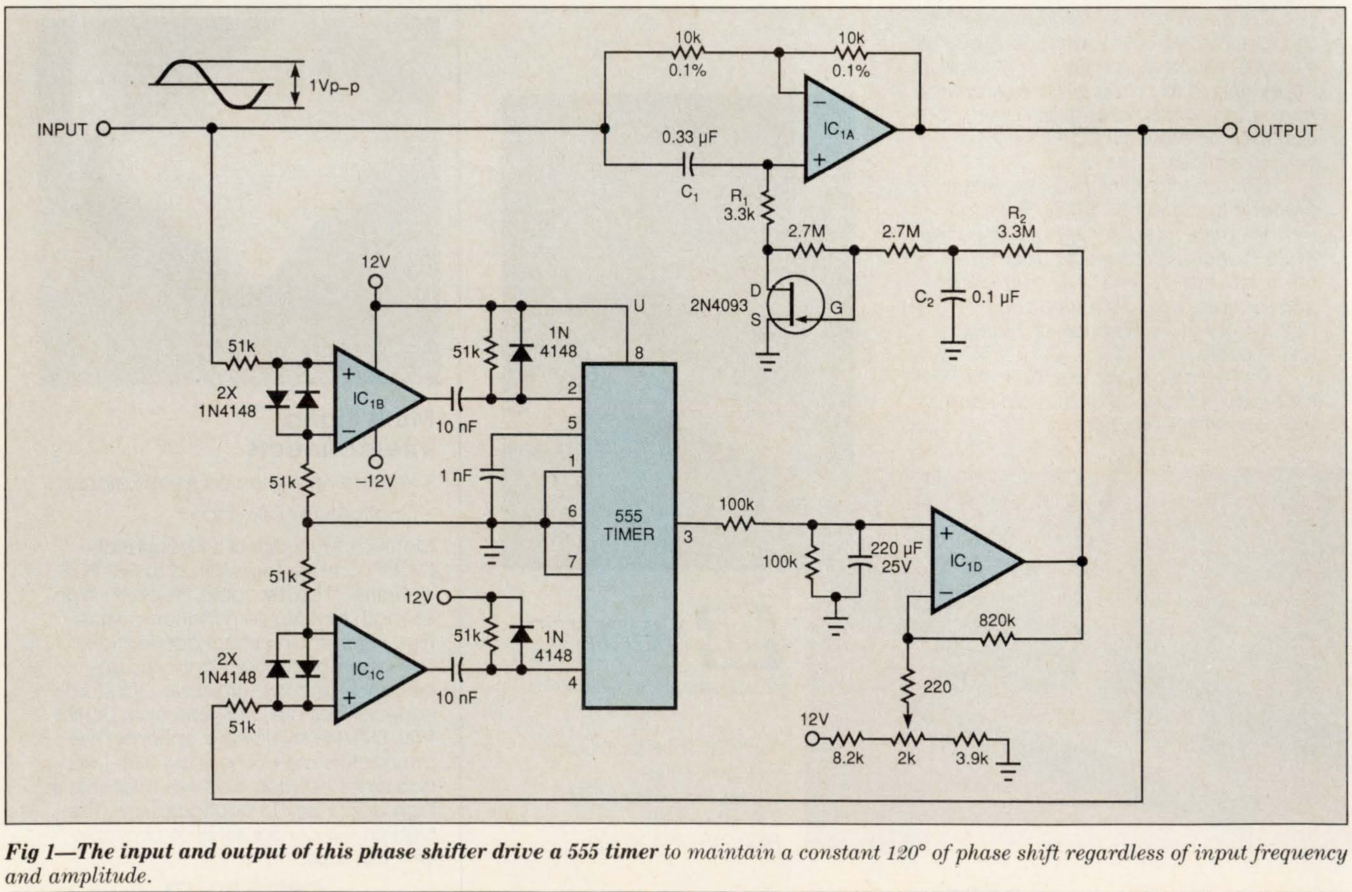

*Fig 1—**The input and output of this phase shifter drive a 555 timer** to maintain a constant 120° of phase shift regardless of input frequency and amplitude.*

Design Entry Blank

$100 Cash Award for all entries selected by editors. An additional $100 Cash Award for the winning design of each issue, determined by vote of readers. Additional $1500 Cash Award for annual Grand Prize Design, selected among biweekly winners by vote of editors.

To: Design Ideas Editor, EDN Magazine
Cahners Publishing Co
275 Washington St., Newton, MA 02158

I hereby submit my Design Ideas entry.

Name ______________________

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Company ______________________

Division (if any) ______________________

Street ______________________

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Country ______________ Zip __________

Design Title ______________________

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Social Security Number ______________
(Must accompany all Design Ideas submitted by US authors)

Entry blank must accompany all entries. Design entered must be submitted exclusively to EDN, must not be patented, and must have no patent pending. Design must be original with author(s), must not have been previously published (limited-distribution house organs excepted), and must have been constructed and tested. Please submit software listings and all other computer-readable documentation on a 5¼-in. IBM PC disk.

Exclusive publishing rights remain with Cahners Publishing Co unless entry is returned to author or editor gives written permission for publication elsewhere.

In submitting my entry, I agree to abide by the rules of the Design Ideas Program.

Signed ______________________

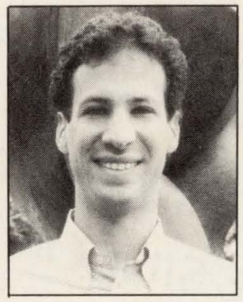
Date ______________________

ISSUE WINNER

The winning Design Idea for the March 1, 1991 issue is entitled "Amplifier scheme lowers drift and noise," submitted by Jim Williams of Linear Technology Corp (Milpitas, CA).

Your vote determines this issue's winner. All designs published win $100 cash. All issue winners receive an additional $100 and become eligible for the annual $1500 Grand Prize. **Vote now**, by circling the appropriate number on the reader inquiry card.

Three ICs produce a grand prize



For Bruce Saldinger of Los Angeles, "Three ICs produce pure sine waves" produced the 1990 Design Idea of the Year. Saldinger's October 25 Design Idea was his first submission. "I'm still in shock" he said, one week after being notified of the $1500 prize.

In Saldinger's circuit, a TTL counter, an 8-channel analog multiplexer, and a fourth-order lowpass filter generate 1- to 25-kHz sine waves with a THD better than −80 dB. The circuit cascades two second-order, continuous-time Sallen-Key filters to implement the fourth-order lowpass filter. Two resistive dividers provide bipolar dc inputs to the multiplexer. The multiplexer produces an eight-times oversampled staircase approximation of a sine wave. Eight-times oversampling greatly simplifies the smoothing requirements of the lowpass filter by pushing the first significant harmonic out to seven times the fundamental.

The three-IC sine wave idea first came to him when he was a co-op student working at IBM in Manassas, VA. It can also be traced back to all the engineering communications-related classes he took. He says the circuit is an example of a practical solution to a principle learned in school. Saldinger says the three-IC idea also fit in well with his work at Maxim Integrated Products.

Saldinger is currently earning his MBA from UCLA. An MBA will, he says, allow him to "explore other avenues." Saldinger has a BSEE from UC Berkeley, where he was a member of Eta Kappa Nu, a National honor society for electrical engineers. After graduating, he worked for Monolithic Memories, now Advanced Micro Devices. He wanted to work with a smaller company, so he joined Maxim to design analog ICs. Now he's back in school full time. Saldinger says he didn't reach a career plateau, but that he "saw it coming." This summer he's off to Tokyo for an internship with Sony. For prospective EE students, he recommends getting a broad background, cautioning that specialization could hold them back.

Saldinger's main "hobby" is studying for final exams. When not studying for finals or whipping up winning circuit designs, he indulges in wind surfing and squash.—*Brian Tobey*

EDN

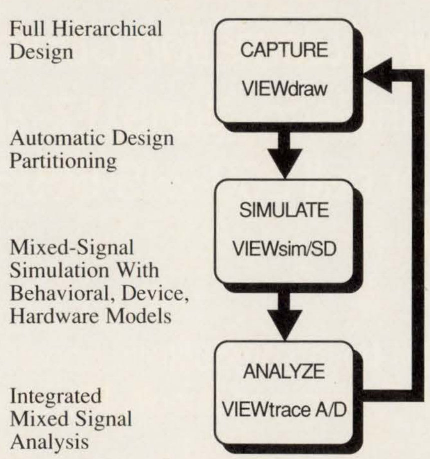
For Most People, It Was Just Another Warm September Day.

For design engineers, it was the day mixed analog/digital design came of age.
The event was the mixed-signal design demonstration at the IEEE Bipolar Circuits and Technology Meeting (BCTM). The goal was to give credence to mixed-signal simulation and to benchmark companies in the marketplace. The results were conclusive.

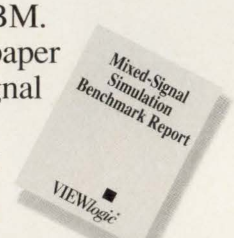
Viewlogic came up with the right answer first.
But more to the point, what we did at BCTM in September, we can do for you now. We're the only company with a proven technology and a three year track record of success. The only one that integrates design capture, simulation and analysis.

But that's just the beginning.

Performance and Flexibility available nowhere else.
With VIEWsim/SD, you'll get the choices you need. You'll be able to mix behavioral models with gates and SPICE primitives. Choose from leading analog simulators like PSPICE and HSPICE. Include physical hardware models for devices when software models are not available. Use the most popular platforms from SUN, DEC and IBM.



Our white paper "Mixed-Signal Simulation Benchmark Report" proves the point. **Call us at 1-800-422-4660, Ext. 102.** You'll like the climate we're creating for mixed-signal design.



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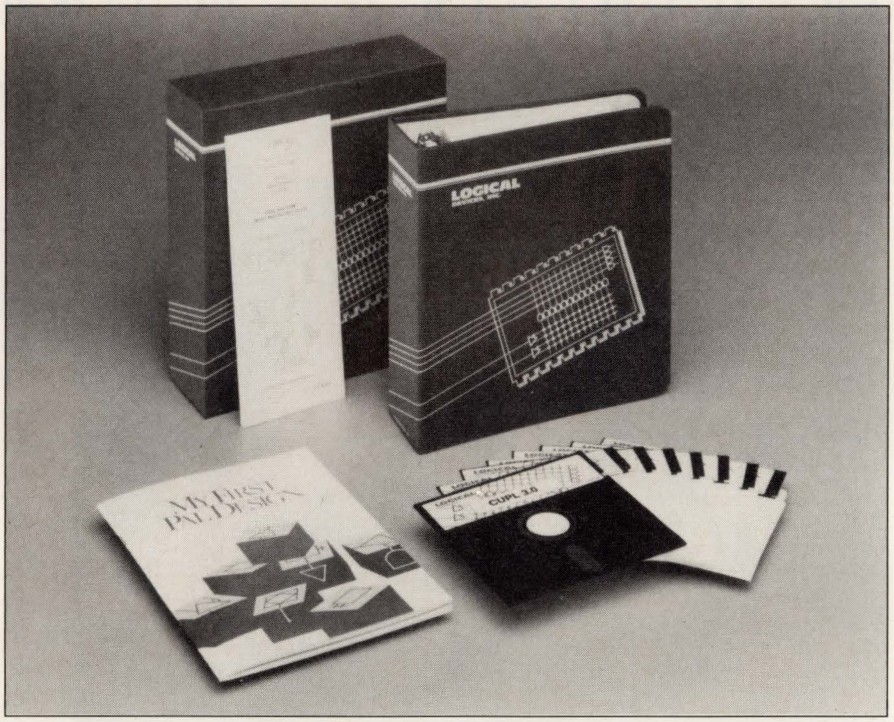
CAE & SOFTWARE DEVELOPMENT TOOLS

PLD Compiler

- *Now available for DECstations*
- *Supports most PLD device types*



CUPL is a PLD Compiler and simulator that lets you enter designs without first specifying a device or pin number. The program supports devices from Altera, AMD/MMI, Intel, Lattice, National Semiconductor, Signetics, Texas Instruments, and Toshiba, as well as Xilinx gate arrays. In addition, the program provides on-line help for all valid extensions at the end of variable names; these extensions indicate specific functions assigned to major nodes that you can program within the PLD. You can include arithmetic expressions within loops; the preprocessor loop index has a maximum value of 1024. The program can also handle PLCC (plastic-leaded-chip-carrier) versions of PLDs; the chip-diagram section of the .DOC output file shows the correct PLCC package with the signal names already placed on the pins. The program accepts Boolean-equation, state-machine, schematic, and truth-table inputs, and optimizes and simulates the design to verify proper operation before programming. Integrated with DEC's Power Frame framework, CUPL supports the DECwindows interface, which incorporates the X-Window system; it runs under Ultrix, VMS, Apollo NCS, SunOS, and Sunview operating systems. For DECstation, Apollo 3000/4000, Sun-3, Sun-4, and SPARCstation workstations, from $2295.

Logical Devices Inc, 1201 NW 65th Pl, Fort Lauderdale, FL 33309. Phone (305) 974-0967.

Circle No. 351

C Communications Library

- *Provides uniform applications interface*
- *Includes routines that work like C++ virtual functions*

Commlib Level 2 version 3.1 provides a set of routines that works like C++ virtual functions and supports six device drivers. These routines provide a uniform API (applications-program interface) for programming asynchronous data communications. The library includes Xmodem, Ymodem, Zmodem, Kermit, and ASCII file-transfer protocols with Xon/Xoff, RTS/CTS, or DTR/DSR flow-control handshaking. Other routines can control 16550 FIFO-mode UARTS or modems that use the Hayes AT command set, with flexible interrupt-driven support for an unlimited number of serial ports. You can use standard PC COM1 . . . COM8 ports with a choice of three low-level drivers; intelligent Digiboards; six makes of nonintelligent multiport boards; Fossil drivers to support Fido/Opus/Seadog BBS systems; or Fresh Technology's Modem Assist to provide modem access across a network. Other new functions include a diagnostic function call that displays the status of all significant ports on the screen, and a fast driver that can solve the problem of lost interrupts in some high data-rate situations. You can use the library with C compilers from Microsoft, Borland, Watcom and Topspeed, or C++ compilers from Zortech and Borland. $359.

Greenleaf Software Inc, Bent Tree Tower Two, Suite 570, 16479 Dallas Pkwy, Dallas, TX 75248. Phone (800) 523-9830; in TX, (214) 248-2561. FAX (214) 248-7830.

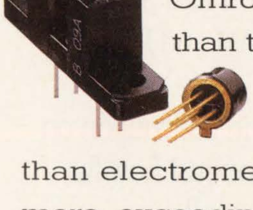
Circle No. 352

Enhanced PC-Board Design Software

- *Provides new parts library*
- *Checking feature reduces errors*

Version 4.0 of Pads-PCB is a major upgrade of this widely used pc-board design software. The vendor

IMAGINE BLINKING A MILLION TIMES A DAY FOR TWENTY YEARS, AND YOU'LL BEGIN TO UNDERSTAND THE DURABILITY OF OUR OPTICAL SWITCHES.



Omron optical switches keep an eye on innovation. They work by sight rather than touch. Which means they won't wear out like electromechanical switches in tough applications such as duplicating, fax machines and computer peripherals. In fact, our optical switches operate thousands of times faster than electromechanical switches. And, they perform reliably for up to twenty years or more, exceeding the lifetime of the product itself.

Omron's optical switches dramatically improve the reliability of your end product by virtually eliminating switch failure. Take a closer look at Omron optical switches. There are over 50 standard types to choose from. Or ask us about the more than 100,000 different types of control components we produce. You can reach us at 1-800-62-OMRON.

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WE HAVE THE FUTURE IN CONTROL.

CIRCLE NO. 176

has integrated its CAE and PCB libraries into a single common library that serves both the schematic-capture and pc-board design tools. A library manager gives you rapid access to, and graphical browsing through parts contained in the library. The human interface now provides a "fill-in-the-form" screen format for entering alphanumeric data such as padstacks, tracks, clearance, and other database-setup information. This format simplifies data entry and reduces the number of input errors. Other enhancements include checking for the presence of thermal pads on power and ground planes, graphics-card drivers for most 1024×728 high-resolution cards, and facilities for output to a laser printer. Pads users with annual support receive the new version at no charge; users without annual support, $350; new users, $975.

CAD Software Inc, 119 Russell St, Suite 6, Littleton, MA 01460. Phone (800) 255-7814; in MA, (508) 486-9521. FAX (508) 486-8217.

Circle No. 353

CAE Optimization Tool For Diverse Technologies

- *Can optimize a design within its existing technology*
- *Can remap the design to a different technology and optimize it*

Retargeter is a CAE tool that can optimize single- or multiple-gate net lists and PLD JEDEC files for the original technology (such as TTL standard parts or FPGAs), or can remap the design to a different technology (such as CMOS or gate arrays) and then optimize the design for the new technology. The optimization algorithms break a large design into small groups and synthesize each group individually. The tool reads an existing wire file and produces a new wire file containing optimized logic; another tool, Viewgen, lets you use the new file to generate a schematic for a gate-level simulation. Retargeting does not necessarily produce a one-to-one exchange of cells from one technology to another; the optimization may add or delete cells from the original design in order to optimize performance in the new technology. Version for a Unix host computer, $30,000.

Viewlogic Systems, 293 Boston Post Rd W, Marlboro, MA 01752. Phone (508) 480-0881.

Circle No. 354

Object-Oriented Database-Management System

- *Provides interactive query facility*
- *Portability library isolates machine-specific code*

Objectstore release 1.1 includes feature and performance enhancements and is available for IBM's RS/6000 under AIX 3.1, for DECstations running Ultrix 4.1, and for other workstations running Unix System V release 4, as well as Sun-3 and SPARCstation computers. New features include an interactive query facility that gives you real-time access to information, and a new portability library that isolates machine-specific code and facilitates the porting of Objectstore to Unix-based and non-Unix-based systems. Performance improvements include local-mode processing in which the client and server run on the same machine; faster short transactions; and a faster collections class library. The new API (application programming interface) is based on C and C++ libraries so that you can use the object-oriented, database management system with a variety of third-party compilers. Depending on the number of seats and sites for which licenses are provided, $2000 to $6000/seat.

Object Design Inc, 1 New England Executive Park, Burlington, MA 01803. Phone (617) 270-9797. FAX (617) 270-3509.

Circle No. 355

Translator For Simulating Data Files

- *Converts flat-vector stimulus files to other formats*
- *Handles high-level constructs found in Mentor Force files*

Vtran is a program that loads the state/time information of simulation stimulus files and reformats the data for use by any of more than 20 widely used simulators. Version 1.5 adds new simulator interfaces for Cadat, Lasar, VLSI Technology, Toshiba, and Lsim, and new "Format String" features enhance the program's ability to read differently formatted files. You can customize the format descriptors to describe both the input-data format and the output-data format. After loading the data, the program can perform some optional processing on the data before generating the output file. It can change the pin list, pin order, pin timing, and other parameters; the modifications may affect as many as 1024 pins. Vtran is available for Sun, Apollo, Intergraph, and IBM PC/AT computers. Single-node license, $3495.

Source III Inc, 4960 Almaden Expressway, Suite 147, San Jose, CA 95118. Phone (408) 997-2575.

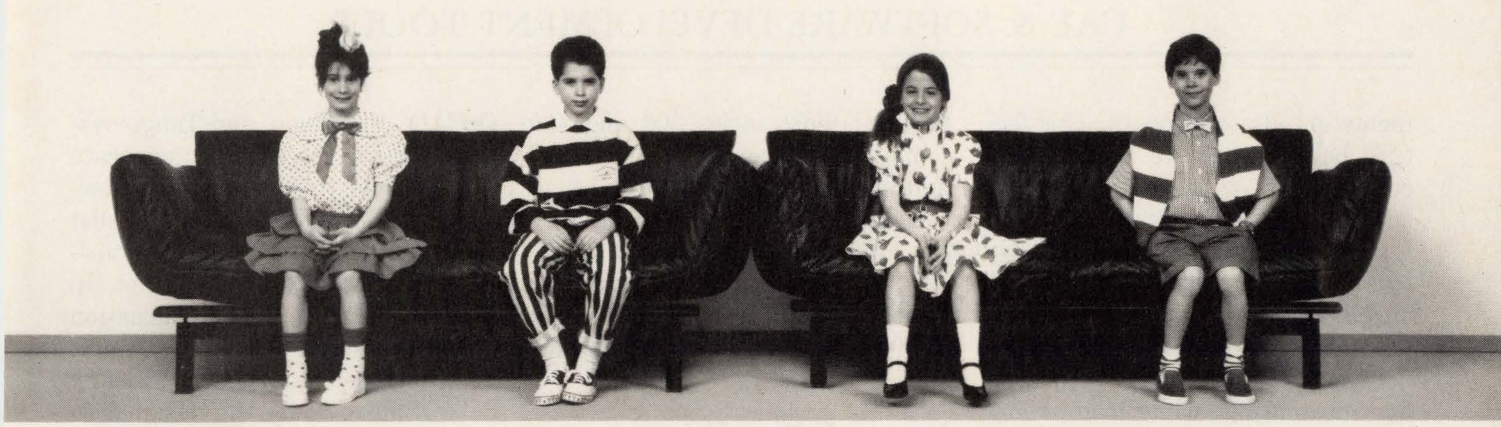
Circle No. 356

Autorouter For High-Speed Printed-Circuit Boards

- *Provides table-driven crosstalk controls*
- *Automatically balances pair routing*

Specctra SP50 is an autorouter for the layout of high-speed pc boards. The program lets you construct a table of parallel rules that emulate a curve of gap versus parallel length allowed between two segments; you can use different tables for segments on the same layer and seg-

Their way.



Our way.

Here's how to turn a relay with 2 changeover contacts into one with 4.

The MT4, our new relay with 4 changeover contacts, hardly occupies more board space than the MT2, our relay with 2 changeover contacts.

So if you need 6 twin changeover contacts on your board, simply install an MT2 and an MT4. Two relays of virtually identical size.

And the expensive space you formerly needed for a third MT2 is now free for other important functions.

Plus: less testing, less component cost, less assembly effort, greater reliability.

What more can you want?

(The new MT4: Power consumption at 20 °C 300 mW. Temperature range −55 °C to 85 °C. Space occupied per contact 12 M^2.)

I'm interested in the new MT4 relay. Please send me your literature.

Company ______________________

Name ______________________

Address ______________________

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EDN 6/6/91

Alcatel STR AG
CH-8055 Zurich/Switzerland, Friesenbergstrasse 75

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Dr. Juchli 1000 STR

ments on adjacent layers. This feature helps to achieve high routing completion with little or no crosstalk. For very fast dual-polarity ECL circuits, you normally have to route both polarities as a balanced pair and then fix them in place; this autorouter makes such nets subject to ripup and retry during autorouting, while maintaining conformance to all design rules. Delay considerations may require minimum lengths for some nets and maximum lengths for other. You can specify minimum or maximum lengths for individual connection, nets, or net classes, and the autorouter will observe these constraints. The features reduce the amount of manual editing required during layout and correspondingly reduce the total design time. The program runs on the Sun SPARC family of workstations, the IBM RISC 6000, and the Hewlett-Packard 9000 series 300 and 400 computers. Depending on host configuration, from $45,000.

Cooper & Chyan Technology Inc, 1601 Saratoga-Sunnyvale Rd, Suite 255, Cupertino, CA 94014. Phone (408) 366-6966. FAX (408) 252-9565. **Circle No. 357**

Layout Editor For Standard-Cell Autorouting

- *Provides padframe generation and routing*
- *Performs all angle editing*

L-Edit version 3 is an IC-design tool that runs on IBM PCs and compatibles. New features include built-in standard-cell placement and routing; automatic padframe generation; and padframe routing. The editor now allows you to automatically route a standard-cell ASIC, complete with padframe generation and routing, on your PC. Users of OrCAD, Viewlogic, and Tango systems can use the editor to generate ASICs from their schematic; however, you'll need the Gatesim netlist tool kit and SCMOSscmap to translate and simulate your design in schematic form. When translation and simulation are complete, L-edit uses the standard-cell library SCMOSlib to route the design into a layout-level description. In six to seven weeks, Mosis (Marina del Rey, CA) can fabricate prototypes of chips routed by L-edit for $500; several silicon foundries (including Hewlett-Packard, Orbit, and VLSI Technology) can fabricate intermediate and high-volume quantities. L-edit version 3, $995; SCMOSscmap and SCMOSlib, $295 each; Gatesim, $1295.

Tanner Research Inc, 444 N Altadena Dr, Pasadena, CA 91107. Phone (818) 795-1696. FAX (818) 795-7937. **Circle No. 413**

CIRCLE NO. 177

Design Kit For Text-Screen Creation

- *TSR program reports row/column coordinates*
- *Screen-design form lets you draw preliminary sketch*

Screen Design Kit is a combination of software and accessories that helps you design and maintain text screens for application programs. You can pop up a TSR (terminate-and-stay-resident) program from within any application in order to see the column/row coordinates and attribute byte of any position on the screen; the report shows foreground and background colors in decimal, binary, programming codes, dBase color codes, and English. A color palette displays all of the available color combinations. These reports help you define the characteristics of your screen design very precisely. The accessories include a pad of 50 screen-design forms; these forms let you sketch out your design using exact row/column coordinates; a row/column ruler; a laminated conversion chart showing the ASCII, decimal, hex, octal, and binary codes of every available character or symbol (including box-drawing combinations). $99.95.

Butler Computer Systems, Box 5306, Walnut Creek, CA 94596. Phone (415) 256-8401.

Circle No. 358

Interactive Digital Simulator

- *Performs functional simulation and timing analysis*
- *Runs in protected mode on 80386/486-based systems*

Ultisim is an interactive digital simulator that runs in 32-bit protected mode on 80386/486-based systems with a performance comparable to that of simulators running on Unix-based workstations. The 28-state simulator provides save and restore capability, a logic analyzer-like display, and a digital waveform processor. The program comes with model libraries for TTL 54 and 74 series, ECL, CD4000, and PLD devices. The Viewtrace option, developed with Viewlogic Systems (Marlboro, MA), can perform graphical manipulation, Fourier transforms, and analog waveform processing. Three versions are available. Entry System, with a design capacity of 50 14-pin ICs, $1295; Advanced System, with a design capacity of 200 14-pin ICs, $3275; Professional System, with unlimited design capacity, $7375; Viewtrace option, $1995.

Ultimate Technology, 1725 Montgomery St, San Francisco, CA 94111. Phone (415) 391-2433. FAX (415) 391-0669. **Circle No. 359**

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We've expanded our line of rugged microcomputers into a full team of products, all built rugged from the ground up. These are full rugged systems, versatile enough for military applications, and tough enough for the harshest environments.

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700 KMS Place, Ann Arbor MI 48106-1868

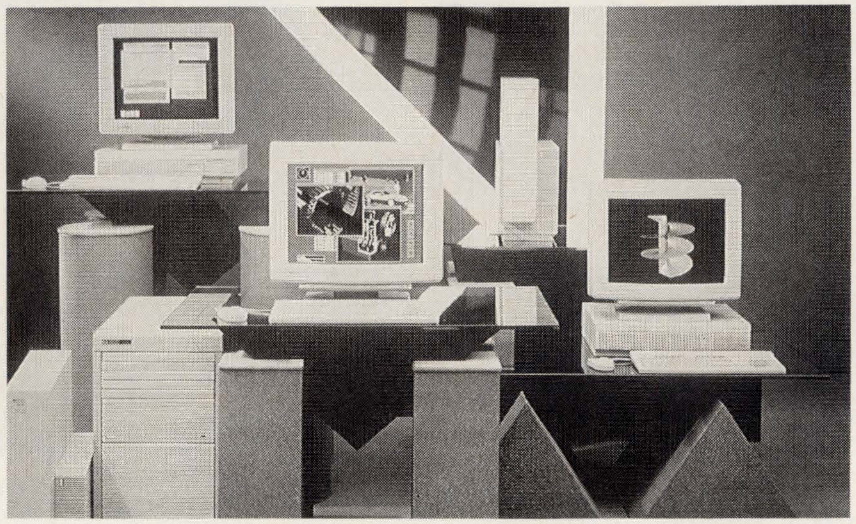
CIRCLE NO. 174

NEW PRODUCTS

COMPUTERS & PERIPHERALS

RISC Workstations

- *Three models use the PA-RISC processor*
- *Two models deliver 76 MIPS and 72.2 Specmarks*



The 9000 Series 700 consists of three models of workstations that use the company's PA-RISC (Precision-Architecture Reduced-Instruction-Set-Computer) processor. The entry-level desktop Model 720 runs at 50 MHz and delivers 57 MIPS, 55.5 Specmarks, and 17M flops. The desktop Model 730 and the desk-side Model 750 run at 66 MHz and deliver 76 MIPS, 72.2 SPECmarks, and 22M flops. Both desktop models have 128k-byte instruction and 256k-byte data caches and as much as 64M bytes of RAM with error-correction code (ECC). In addition, the desktop models have as much as 840M bytes of internal disk storage and accommodate 10G bytes of disk capacity. The desk-side Model 750 has 512k bytes of cache and as much as 192M bytes of ECC RAM. The Model 750 has as much as 2.6G bytes of internal disk drive and accommodates 40G bytes of disk capacity. The Model 720 and 730 each have one EISA slot, and the Model 750 has four EISA slots. Model 720 with a 400M-byte disk, from $15,990; Model 730 with two 400M-byte disks, from $23,990; Model 750 with 660M-byte disk, from $39,690.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

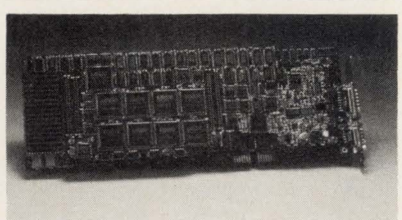
Circle No. 360

Image Processor

- *Three parallel 25-MHz processors achieve 75-MHz rate*
- *Averages as many as 256 frames in real time*

The DT2867 frame grabber and frame processor on a single 16-bit ISA bus board contains three parallel 25-MHz processors, each containing its own ALU and multiplier. The combination achieves a 75-MHz pixel-processing speed. Because the board can process three pixels simultaneously, it performs a 3×3 convolution on a 640×480-pixel image in less than 1/15 sec. The ALUs have 16-bit accuracy and a 1M-byte processing buffer, which allows the board to average as many as 256 frames in 1/30 sec. In addition, the processor executes histograms in 1/30 sec and can store as many as four separate histograms. The board digitizes images from video cameras and VCRs and stores the images in one of two 512k-byte frame buffers. $6995. A Windows 3.0 software package, called Global Lab Image, will be available in September for $2495.

Data Translation, 100 Locke Dr, Marlboro, MA 01752. Phone (508) 481-3700. **Circle No. 361**



VGA To Video Board

- *Converts VGA output to NTSC or PAL video signals*
- *Runs independent of the host*

The Tapecaster 8-bit ISA bus board converts a VGA output signal to either NTSC or PAL video-formatted signals. A hardware design that doesn't require software lets you simultaneously view the data on a VGA-compatible monitor while recording data on a videotape. The board uses crystal-controlled frequency sources, which provide a precise NTSC or PAL output frequency. The board also has a Super VHS output. By converting all VGA modes having a maximum resolution of 640×480 pixels, the board allows VGA video windows and color to be faithfully reproduced. The video quality is limited only by the NTSC and PAL standards. $750.

Redlake Corp, 15005 Concord Circle, Morgan Hill, CA 95037. Phone (800) 543-6563; in CA, (408) 779-6464. FAX (408) 778-6256.

Circle No. 362

SUPER CIRCUIT BOARDS FROM HITACHI CHEMICAL, OF COURSE.

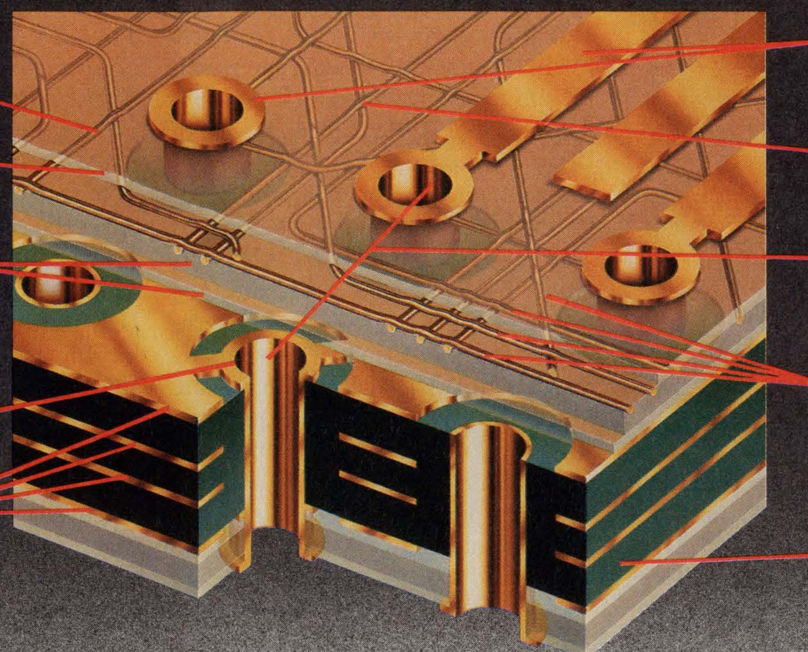
INSULATED WIRES
Insulated 0,1mm (4 mil) diameter copper wires are routinely used for high wiring densities.

OVERLAY
A cover layer of epoxy glass cloth is used to encapsulate the board and to securely affix the wires in place.

ADHESIVE + UNDERLAY
The wires are securely bonded to an adhesive material, and additionally insulated from the format board with underlay pre-preg material.

THROUGH HOLE PLATING
Copper plated through holes interconnect each wire both mechanically as well as electrically to inner layer power and ground planes.

INNER LAYER FORMAT BOARD
Multilayer format board can be used for power and ground sources.



PADS
Electroplated pad configurations are used for surface mount technology.

WIRE CROSSOVER
Polyimide insulated wires having a dielectric break down voltage greater than 500VDC permit crossover wiring.

BASIC GRID 2.54 mm (0.1 inch)
Basic grid is standard at 2.54 mm (0.100 inch), however, 1.91 mm (0.075 inch) and 1.27 mm (0.050 inch) are also possible.

3 WIRES BETWEEN IC PINS & DIAGONAL WIRING
Concurrent wire routing can easily accommodate 3 wires between IC pins plus diagonal wiring to minimize crosstalk.

GLASS EPOXY BASE MATERIAL
Base material is an epoxy glass cloth FR-4 material. Plating catalysts are impregnated within the material to insure good platability.

Smaller Denser Faster. This is Super Circuit sophistication at its finest, and is a prime reason you should consider SMT combined with Multiwire® Interconnection Technology. In this day of higher density silicon chip integration and higher speeds, circuit boards need to become an active extension of the component. Multiwire Boards (MWB®) are the next logical step. Using uniform 0.1mm diameter insulated copper wire for signal interconnection, MWB can routinely accommodate super high wiring densities and high signal speeds. This allows transmission line performance characteristics while offering critical wire length and precisely controlled impedance levels. Concurrent Routing, a uniquely developed wiring technique, permits a high degree of design flexibility while achieving enhanced electrical performance, especially where high signal speeds and crosstalk management are critical.

At Hitachi Chemical we offer total, one vendor responsibility to the circuit board industry, and we manufacture 100% of all materials used in our highly complex products. We are the *only* circuit board manufacturer providing 21st century products as well as producing the specialized materials to achieve these designs. Our space age interconnection technology provides clear epoxy films for improved insulation resistance, polyimide laminate boards for high heat characteristics, low dielectric laminate materials to facilitate high speed signal transfer, flexible and rigid-flex MWB, printed circuit boards, ceramic boards and multilayer boards.

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Santa Clara, CA 95051
(408) 244-2570

2102 Business Center Dr.
Suite 130
Irvine, CA 92715
(714) 253-5790

CIRCLE NO. 10

80486 EISA Computers

- *Contain 4M bytes of RAM expandable to 32M bytes*
- *Have one 8-bit ISA and seven EISA slots in AMI's BIOS*

The ME 486-EISA/25 and ME 486-EISA/33 are EISA bus computers containing 25- and 33-MHz 80486 μPs, respectively. Standard configurations include 4M bytes of RAM; 128k bytes of external cache RAM; an extended VGA card and a color monitor capable of 1024× 768-pixel resolution with 256 colors; a 150M-byte ESDI hard-disk drive; an EISA disk controller with cache; 1.44M-byte, 3½-in. and 1.2M-byte, 5¼-in. floppy-disk drives; one parallel and two serial ports; either DOS 3.3 or DOS 4.01; and a choice of three keyboards. You can expand the memory on the mother board, in 4M-byte increments, to a maximum of 32M bytes. The RAM chips have 70-nsec access times and are arranged in a page mode for zero-wait-state operation. The computers use an AMI BIOS and have one 8-bit and seven EISA expansion slots. ME 486-EISA/25, $4999; ME 486-EISA/33, $5499.

Micro Express, 1801 Carnegie Ave, Santa Ana, CA 92705. Phone (714) 852-1400. FAX (714) 852-1225.

Circle No. 363

80386SX Single-Board Computer

- *Executes IBM PC-compatible software on the VMEbus*
- *Runs at 20 MHz and has 1M, 4M, or 8M bytes of RAM*

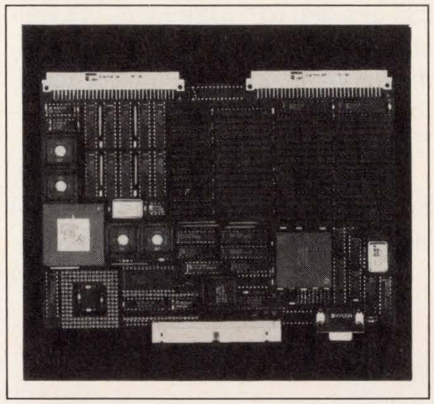
The XVME-686 PC/AT single-board computer (SBC) for the VMEbus uses a 20-MHz 80386SX μP and 1M, 4M, or 8M bytes of RAM. It executes IBM PC-compatible software. Its operating temperature ranges from 0 to 65°C. The board contains both a VMEbus and an ISA bus hardware interface; an IDE hard-disk controller; a controller for two floppy disks; a 16-bit VGA graphics controller; a socket for an 80387SX coprocessor; two serial ports; a Centronics parallel port; and a watchdog timer. Other features include VMEbus Slot 1 functions and a VME interrupter and interrupt handler. The board can access the short I/O, standard, or extended address space. The hardware byte-swapping feature handles byte-ordering differences between conventional VMEbus 680xx CPUs and the 80386SX μP. From $3500.

Xycom Inc, 750 N Maple Rd, Saline, MI 48176. Phone (800) 367-7300; in MI, (313) 429-4971. FAX (313) 429-1010. **Circle No. 364**

Graphics Controller Board

- *Uses TMS34020 chip and displays 1024 × 1024 pixels*
- *Provides from 15.7 to 63 kHz*

The VCF-V graphics controller board for the VMEbus uses TI's TMS34020 graphics chip to display 1024 × 1024 pixels; the display has a depth of 8 bits. The 6U board also provides an overlay of 1024 × 1024 pixels having a depth of 4 bits. The number of addressable pixels is expandable to 2048 × 2048 pixels,



which can produce multiple-page displays. A write-mask register write protects individual bit planes. You can expand the standard display memory from 1M to 8M bytes, and you can opt for a TMS34082 floating-point unit. Both the graphics chip and the host processor have access to the dual-port video RAM, which the board uses for display memory. The board also handles interrupts from the host, an onboard SCSI controller, and a serial I/O port. $1900.

Peritek Corp, 5550 Redwood Rd, Oakland, CA 94619. Phone (415) 531-6500. FAX (415) 530-8563. **Circle No. 365**

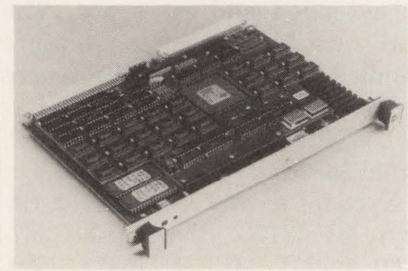
DSP Evaluation Module

- *Operates as fast as 40 MHz for TI's TMS320C51 chip*
- *Lets you develop, debug, and benchmark algorithms*

The EVM320C5X DSP evaluation module for TI's TMS320C51 chip operates at 40 MHz and executes 20 MIPS. It has 16k bytes of zero-wait-state RAM for data and for programs, respectively. Both RAMs are expandable to 64k bytes. A 96-pin DIN expansion connector provides access to all of the DSP signals. The connector is an interface to a series of companion modules that aids hardware and software development. One companion module contains TI's TLC3204X analog interface circuit. In addition, a prototype module lets you develop custom circuitry. The stand-alone evaluation module communicates with an IBM PC-compatible symbolic debugger via an RS-232C port. The PC must have either a 286 or a 386 μP, 512k bytes of available RAM, a hard-disk drive, a 5¼-in. floppy-disk drive, a color-monitor adapter, and either PC- or MS-DOS 3.0 or higher. $1495.

Spectrum Digital Inc, Box 1559, Sugar Land, TX 77487. Phone (713) 561-6952. FAX (713) 561-6037.

Circle No. 366



Graphics Controller Board

- *Uses a TI TMS34020 chip to draw 4M pixels/sec*
- *Meets Mil-Specs for military applications*

The PMV 68 GDP-1 VMEbus graphics controller board meets Mil-Specs for shipboard, ground mobile, and airborne applications. It uses TI's TMS34020 chip to draw 4M pixels/sec, and it generates fill patterns and vectors. The board comes with as much as 3M bytes of dual-port video RAM for display memory. An additional 1M byte of dual-ported RAM provides the interface between the VMEbus and the TMS34020 chip. The board can display either 768×574 or 1280×1024 pixels. An 8-bit-deep display buffer provides 256 simultaneous colors from a palette of 16.7M colors. The board also accepts composite-video signals from an external source, such as an FLIR sensor, to overlay the signals on its local graphics and display the superimposed image. $6920. Delivery, eight weeks ARO.

Radstone Technology Corp, 20 Craig Rd, Montvale, NJ 07645. Phone (800) 368-2738; in NJ, (201) 391-2700. **Circle No. 367**

DSP Boards

- *Use TI TMS320C50 or TMS320C51 DSP chip*
- *Have 16k×16-bit RAM*

The TMS320C50 system and processor boards are DSP boards for the 16-bit ISA bus; they use either a 40-MHz TMS320C50 or TMS320C51 DSP chip. The boards contain a 16k×16-bit program and a 16k×16-

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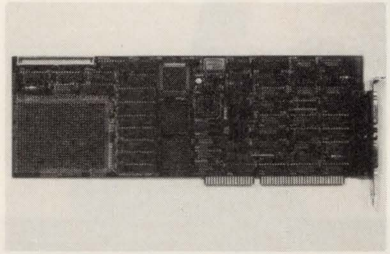
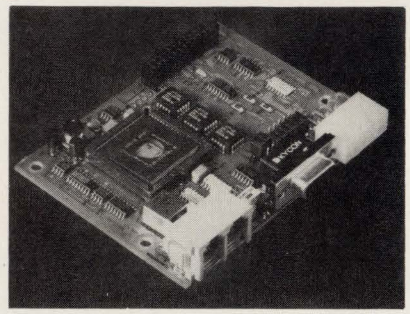
Japan 81-45-543-7185 (FAX 81-45-545-1499)
Korea 82-2-868-0147 (FAX 82-2-868-6600)
Singapore 65-353-8312 (FAX 65-353-8315)

bit data RAM. Both RAMs are expandable to 64k×16 bits. The system board comes with dual onboard 16-bit sigma-delta A/D and D/A converters for analog I/O. Both boards have a prototyping area that lets you build custom interfaces or peripheral circuits. The company's DSP-Link expansion interface is a 50-pin connector that permits high-speed 16-bit parallel data transfers. Both boards contain TI's test bus controller chip, which enables JTAG (Joint Test Action Group) boundary scanning. System board, $3495; processor board, $2495.



Spectrum Signal Processing Inc, Suite 301, 3700 Gilmore Way, Burnaby, BC Canada V5G 4M1. Phone (604) 438-7266. FAX (604) 438-3046. **Circle No. 368**



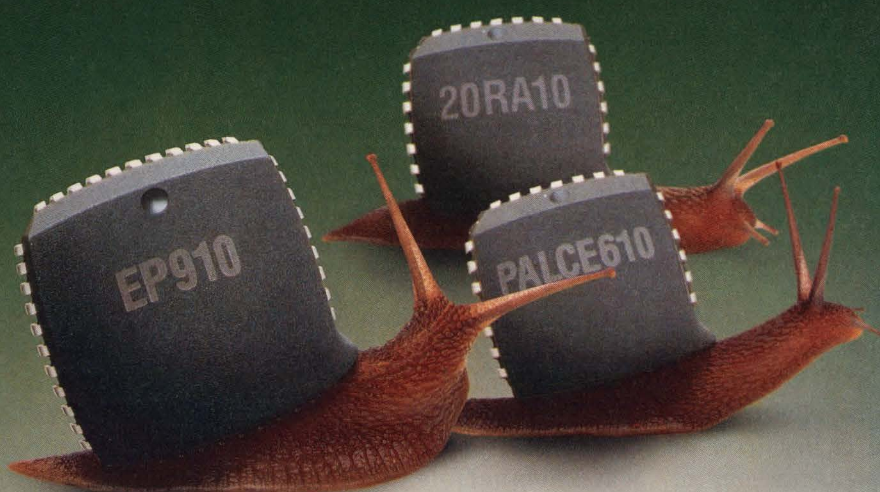
Motor Controllers

- *Let a host control as many as 31 motors on a network*
- *Host communicates with multiple drives over an RS-485 link*

The TR Node peripheral board controls a servo or variable speed motor. As many as 31 boards operate as nodes on a TR Network that uses a host computer for intelligence. The host computer runs a motion-control program to communicate with the nodes over an RS-485 serial link at a user-selectable rate of 115.2 or 38.4k baud. Each node on the TR network responds to a move-on-demand command set. Each node can interpolate points on a motion profile and synchronize the motor's speed and position to other motors on the network. The 3.94×3-in. control boards accept TTL inputs from an incremental encoder either as a stream of pulses or as quadrature signals. Board and L-bracket mount, $371 (100).

Teknic Inc, 214 Andrews St, Rochester, NY 14604. Phone (716) 546-3212. **Circle No. 369**

A question for designers who aren't yet using high-performance μPLDs.



Why the big delay?

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PLD	t_{PD}*
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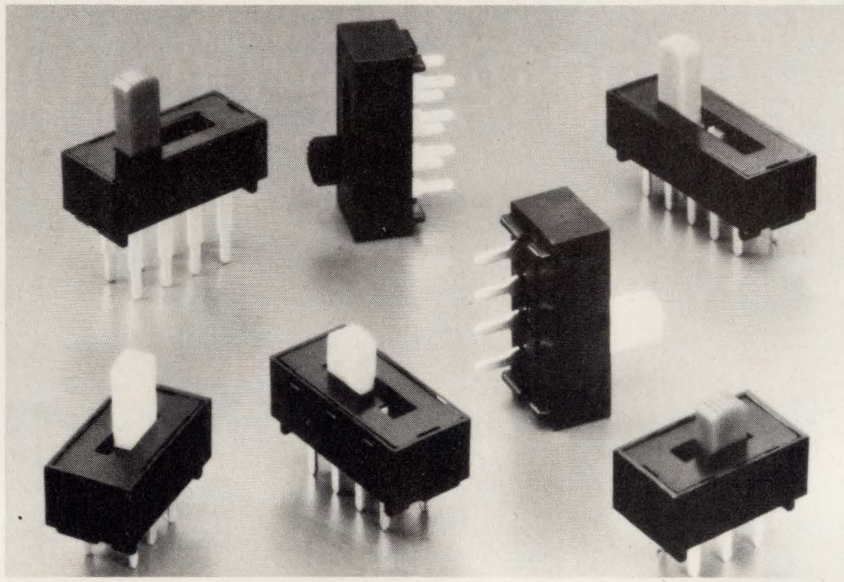
CIRCLE NO. 180

Slide Switches

- *Rated for 4A*
- *Available in single- and double-pole versions*

L Series miniature slide switches feature an all-enclosed plastic construction. Power-rated models are UL recognized and CSA certified, and have ratings ranging to 4A at 125V ac. The line also includes versions that are designed for low-level switching applications. Single- and double-pole versions are available in 2-, 3-, and 4-switch configurations. Housing material is 6/6 nylon, which has a 94V-2 UL rating. The switches feature a built-in positive-detent mechanism. They're available with gold-plated contacts for low-level switching applications and with silver-plated contacts for power service. Electrical life measures 10,000 make-break cycles at full load. Insulation and dielectric strength equal $10^9\Omega$ min and 1000V rms, respectively. Single-pole models, \$0.52; double-pole versions, \$0.74 (1000).



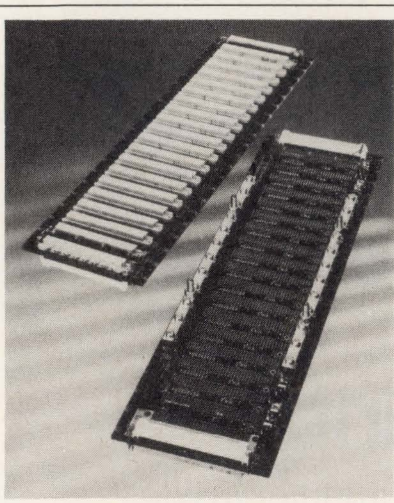
C&K Components Inc, 15 Riverdale Ave, Newton, MA 02158. Phone (617) 964-6400.

Circle No. 370

VMEbus Backplane

- *Accommodates 100-MHz system speeds*
- *Utilizes 11-layer construction*

This J1 backplane is designed to support 16-bit implementations in VMEbus applications. The device can accommodate 100-MHz system operating speeds. Although the unit has only a 3U height, it features all the capabilities normally found on a 6U monolithic backplane. It utilizes 11-layer stripline construction and is designed to be fully backward-compatible with existing VME backplane designs. The device is also fully compliant VMEbus specification IEEE P1014, draft 3.0, revision D. \$590.



Bicc-Vero Electronics Inc, 1000 Sherman Ave, Hamden, CT 06514. Phone (203) 288-8001. FAX (203) 287-0062. **Circle No. 371**

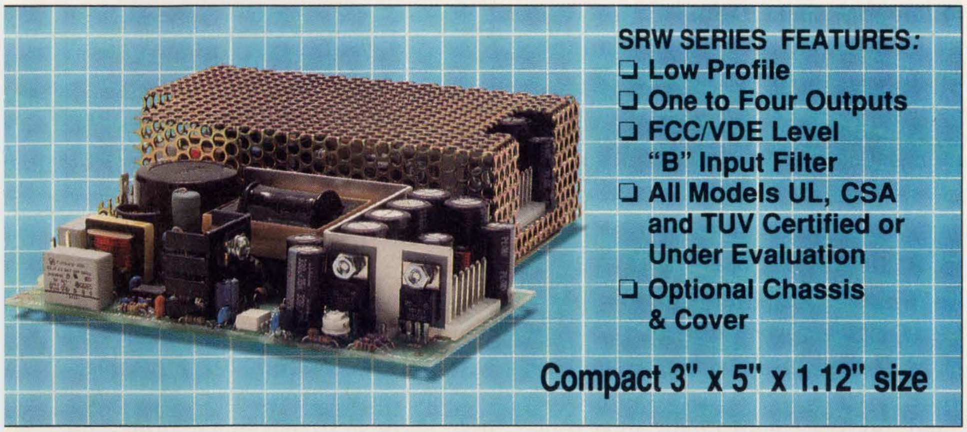
Servoamplifier

- *Develops a ±12A at ±75V peak output*
- *Has 95% efficiency*

The Model 303 PWM servoamplifier is designed for fractional horsepower motion-control applications. It operates from a single-polarity supply (16 to 80V) and develops a 4-quadrant continuous output of ±6A at 75V; for applications involving fast motor acceleration, the unit can develop a peak output of ±12A. The amplifier's 22-kHz switching frequency puts motor-hum noise beyond the human hearing range. The 3-kHz bandwidth maximizes servo accuracy, and the 95% efficiency simplifies cooling requirements and expands mounting options. The amplifier features a user-configurable gain-bandwidth response; users can tailor the response with a single resistor. The unit can function as a current or voltage source. Measuring 6.7×4×1.1 in., the amplifier can be mounted on pc boards, on equipment bulkheads, or edgewise in bookshelf fashion. The device is also compatible with Eurocard assembly requirements. \$275.

Copley Controls Corp, 410 University Ave, Westwood, MA 02090. Phone (617) 329-8200. FAX (617) 329-4055. **Circle No. 372**

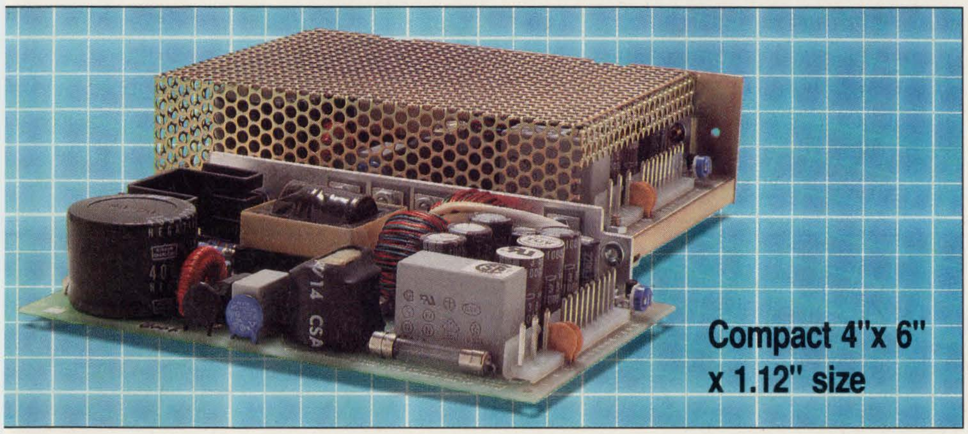
Universal 85-270v Input AC/DC Power Supplies



45 watt — SRW-45

	Model No.	Output 1	Output 2	Output 3	Output 4
QUADS	SRW-45-4001	+5V@5A	-5V@2A	+12V@0.7A	-12V@0.7A
	SRW-45-4002	+5V@5A	-5V@2A	+15V@0.7A	-15V@0.7A
	SRW-45-4003	+5V@5A	+24V@1A	+12V@0.7A	-12V@0.7A
	SRW-45-4004	+5V@5A	+24V@1A	+15V@0.7A	-15V@0.7A
	SRW-45-4005	+5V@5A	+24V@1A	-12V@0.7A	-5V@0.7A
TRIPLES	SRW-45-3001	+5V@5A	+12V@3A		-12V@0.7A
	SRW-45-3002	+5V@5A	+15V@2A		-15V@0.7A
	SRW-45-3003	+5V@5A	+24V@1.5A		-12V@0.7A
DUALS	SRW-45-2001	+5V@5A	+12V@3A		
	SRW-45-2002	+5V@5A	-5V@4A		
	SRW-45-2003	+5V@5A	+24V@1.5A		
	SRW-45-2004	+12V@3A	-12V@2A		
	SRW-45-2005	+15V@2.5A	-15V@2A		
SINGLES	SRW-45-1001	+5V@9A			
	SRW-45-1002	+12V@3.75A			
	SRW-45-1003	+15V@3A			
	SRW-45-1004	+24V@1.9A			

Other output combinations available, please consult factory



65 watt — SRW-65

	Model No.	Output 1	Output 2	Output 3	Output 4
QUADS	SRW-65-4001	+5V@5A	-5V@3A	+12V@2A	-12V@2A
	SRW-65-4002	+5V@5A	+12V@1A	+12V@2A	-12V@2A
	SRW-65-4003	+5V@5A	+24V@1A	+12V@2A	-12V@2A
	SRW-65-4004	+5V@5A	-5V@3A	+15V@2A	-15V@2A
	SRW-65-4005	+5V@5A	+24V@1A	+12V@2A	-5V@2A
	SRW-65-4006	+5V@5A	+24V@1A	+15V@2A	-15V@2A
TRIPLES	SRW-65-3001	+5V@5A		+12V@3A	-12V@1A
	SRW-65-3002	+5V@7A		+12V@2A	-12V@2A
	SRW-65-3003	+5V@7A		+15V@2A	-15V@2A
	SRW-65-3004	+5V@5A	-5V@4A	+12V@2A	
	SRW-65-3005	+5V@5A	-5V@4A	+24V@1A	
DUALS	SRW-65-2001	+5V@7A			-5V@5A
	SRW-65-2002	+5V@7A		+12V@3A	
	SRW-65-2003	+12V@3A			-12V@2.5A
	SRW-65-2004	+15V@2.5A			-15V@2A
	SRW-65-2005	+5V@7A		+24V@1.5A	
SINGLES	SRW-65-1001	+5V@13A			
	SRW-65-1002	+12V@5.4A			
	SRW-65-1003	+15V@4.3A			
	SRW-65-1004	+24V@2.7A			

Other output combinations available, please consult factory

115 watt — SRW-115

	Model No.	Output 1	Output 2	Output 3	Output 4
QUADS	SRW-115-4001	+5V@12A	-5V@4A	+12V@4A (6Apk)	-12V@2A
	SRW-115-4002	+5V@12A	+24V@1A	+12V@4A (6Apk)	-12V@2A
	SRW-115-4003	+5V@12A	-5V@4A	+15V@3A (4Apk)	-15V@2A
	SRW-115-4004	+5V@12A	+24V@1A	+15V@3A (4Apk)	-15V@2A
	SRW-115-4005	+5V@12A	+12V@1A	+24V@3A	-12V@1A
TRIPLES	SRW-115-3001	+5V@12A		+12V@4A (6Apk)	-12V@2A
	SRW-115-3002	+5V@12A		+15V@4A (6Apk)	-15V@2A
DUALS	SRW-115-2001	+5V@12A		+24V@3A	
	SRW-115-2002	+12V@5A			-12V@5A
	SRW-115-2003	+15V@5A			-15V@5A

Other output combinations available, please consult factory

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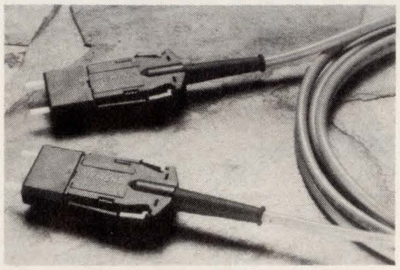
9C Princess Road Lawrenceville, New Jersey 08648 Phone: (609) 896-2122 Fax: (609) 895-1738



Fiber-Optic Jumpers

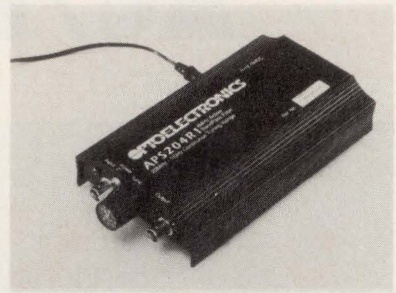
- *Available in 3-km lengths*
- *Have a 0.2-dB insertion loss*

These fiber-optic duplex jumpers are designed to fit the company's Escon-compatible transmitter-receiver shell assembly. The units are available in lengths ranging from 3 to 3000m. The terminating connectors have a retractable shroud that provides additional ferrule protection and eases access for cleaning. A typical duplex jumper has a mean insertion loss of 0.2 dB with a standard deviation of 0.09 dB. The jumpers use a cable that features fibers with 62.5-μm cores. The units are designed to withstand pull forces of approximately 67 lbs. 3m jumpers, $250 (1000).

Siemens Fiber Optic Components, 3846-A First Ave, Evansville, IN 47710. Phone (800) 827-3334; in IN, (812) 422-2322. FAX (812) 422-2339. **Circle No. 373**

Bandpass Filter

- *Has 4-MHz bandwidth*
- *Operates over 6 octaves*



The Model APS-204 bandpass filter has a constant 4-MHz bandwidth and features continuous electronic tuning over the six octaves from 20 to 1000 MHz. The unit is an active filter and has no insertion loss. The device uses a 4-pole resonant cavity filter, which has a Q of 325, to maintain the passband width at 4 MHz, regardless of center frequency. The filter operates on 12V dc for mobile convenience and consumes just 6W. It is housed in an aluminum case, which includes an on-off switch and a 10-turn potentiometer for selecting the center frequency. Noise figure equals 10 dB max, and the third-order intercept is specified at 15 dB typ. $995.

Optoelectronics Inc, 5821 NE 14th Ave, Fort Lauderdale, FL 33334. Phone (800) 327-5912; in FL, (305) 771-2050. FAX (305) 771-2052. **Circle No. 374**

Optical Encoders

- *Designed for price-sensitive applications*
- *Feature a GaAlAs light source*

Containing only a light source and integral sensor, MOD900 and MOD910 Series optical encoders are designed for highly price-sensitive applications. The units utilize a collimated GaAlAs LED light source and a sensing element that consists of an integrated photodiode—a phased-array optical IC. The encoder requires no interrupter masks normally associated with optical encoders—disk resolution is duplicated in diode-array format on the optical IC. Features include resolutions of 200, 500, 512, 1000, and 1024 pulses/revolution and a 100-kHz frequency response. Operating range spans −40 to +80°C, and MBTF exceeds 100,000 hours. Encoder outputs are TTL and CMOS compatible. An index output is available as an option. $15 (OEM qty).

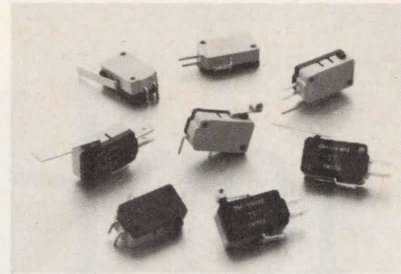
BEI Motion Systems Co, 1755-B La Costa Meadows Dr, San Marcos, CA 92069. Phone (619) 471-2600. FAX (619) 471-2675.

Circle No. 375

Snap-Acting Switches

- *Operate with 15g force*
- *Rated for 5A*

TF-CC and CD Series precision snap-acting switches operate with forces as low as 15g. Designed to meet UL, CSA, and VDE requirements, the units are available in spst and spdt models that are rated to switch 1, 3, or 5A. Units are available with a variety of actuators including standard-pin plungers, wide-pin plungers, levers, lever rollers, and simulated rollers. Termination options include a choice of solder terminals, standard quick-connect, offset quick-connect, screw terminals, and pc-board terminals. From $1 (OEM qty). Delivery, eight weeks ARO.



Unimax, Box 152, Wallingford, CT 06492. Phone (203) 269-8701.

Circle No. 376

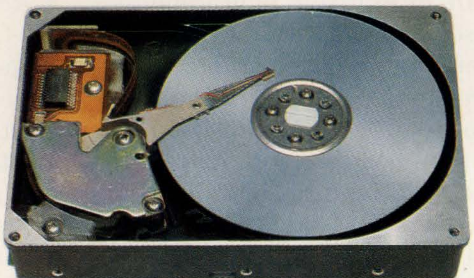
DC/DC Converters

- *Have 200W output*
- *Meet military temperature-operating-range requirements*

MFL Series dc/dc converters provide a 200W output-power capabil-

CIRCLE NO. 58

Specs for Hard Drivers.



Maxtor 7080

Simplicity of design makes Maxtor's Cheyenne Series inch-high 80MB 7080 disk drive the most reliable in its class. Compare Maxtor's four-head, two-platter design to Seagate's six-head, three-platter design. Fewer moving parts make Maxtor's drives inherently more dependable.

Power consumption is a very low 2.8 watts, making it one of the lowest in the 80MB class. The 7080 is also Novell Labs certified, and is available with either SCSI or AT interface, giving you flexibility for a winning system.

Exceptionally fast 17ms seek time and 32K cache buffer in the new generation inch-high form factor give Maxtor faster data throughput than the competition.

Call and ask about our entire Cheyenne family of disk drives with capacities from 40MB to 130MB. Don't fall for the off-the-wall claims. Give us a shot and we'll prove Maxtor specs can't be matched. **Call your nearest Authorized Maxtor Distributor.**

3.5-inch Disk Drive Spec.	Maxtor 7080A	Seagate 1102A
Seek Time	**17 Msec.**	19 Msec.
Standard Buffer Size	**32K**	8K
Form Factor	**3.5" x 1"**	3.5" x 1.6"
Heads-Disks	**4/2**	6/3
Avg. Power Consumption	**2.8 watts**	9 watts

We Drive Harder.

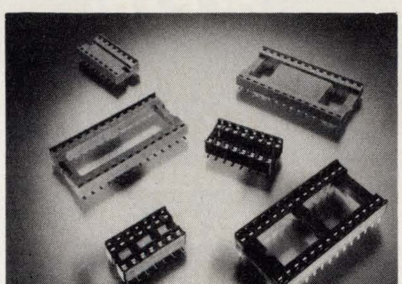
Maxtor®

CIRCLE NO. 207

ity in a true military/aerospace grade device. The parts meet the −55 to +125°C military operating-range requirement and are designed to pass constant acceleration, random vibration, thermal shock, and extended high-temperature life tests. The converters operate with either 28 or 270V inputs and provide outputs of 5, 12, 15, 28, ±12, or ±15V at power levels ranging to 65W/unit. As many as three converters can operate in a current-sharing mode. Other converter parameters include an 85% typical efficiency, 50-dB-max audio rejection, and 15-mV line and load regulation figures. Operating with no external components, the converters meet MIL-STD-461C CS01 and CS02 susceptibility requirements. Operating with companion EMI filters, the converters meet MIL-STD-461C CE03 emission limits. $690 (100).

Interpoint Corp, Box 97005, Redmond, WA 98073. Phone (206) 882-3100. FAX (206) 882-1990.

Circle No. 377



Surface-Mount Sockets

- *Available with tin- or gold-plated contacts*
- *Feature gull-wing terminals*

Diplomate surface-mount DIP sockets are available in dual- and single-leaf versions. They feature gull-wing solder tails and high-temperature-tolerant insulators that can withstand vapor-phase-reflow and infrared-soldering temperatures. Dual-leaf versions feature face-wiping contacts with either tin or gold plating over phosphor bronze. The insulators have a closed-bottom design to prevent solder wicking. Single-leaf sockets come with tin-plated phosphor bronze or beryllium copper contacts. These devices also resist wicking and bridging and have a closed-top design to prevent contact damage. The dual-leaf sockets are available in 16- or 32-position versions; single-leaf units have 28 positions. $1.45 (1000) for the 28-position unit.

AMP Inc, Box 3608, Harrisburg, PA 17105. Phone (800) 522-6752.

Circle No. 378

Latching Solenoid

- *Requires no power to remain pulled in*
- *Operates from a single supply*

The M82 solenoid can pull in and latch when power is applied to the coil. A magnet then holds the plunger in the closed position after the power is removed. The unit can operate with only a 50- to 100-msec pulse of power. Once closed, the unit can withstand a force of 76 to 160 oz. A short-duration 1W pulse, applied in reverse polarity, will cancel the permanent magnetic field and release the plunger. The solenoid operates with a supply of 12, 24, or 110V dc. The continuous standard power rating is 7W, and the intermittent-duty power rating is 20W. $13. Delivery, six to eight weeks ARO.

Liberty Controls Inc, 500 Brookforest Ave, Shorewood, IL 60435. Phone (815) 725-2241. FAX (815) 725-6571. **Circle No. 379**

Connector Kits

- *Evaluate epoxyless optical connectors*
- *Available for single- and multimode fibers*

EK100X kits allow users to evaluate XTC Series epoxyless fiber-optic connectors. Each kit contains 25 connectors, a specially designed crimp tool, a sapphire scribe, and easy-to-follow instructions in a handy carrying case. The kits are available for single- and multimode (50/125 and 62.5/125 μm) fibers. The 2.5-mm connectors in the kit are functionally form- and fit-compatible with the popular ST connector. When terminating a single-mode fiber, the connector demonstrates a 0.16-dB insertion loss over an operating range of −40 to +65°C. EK1001 multimode kit, $444; EK1000 single-mode version, $520.

Ofti, 2 Lyberty Way, Westford, MA 01886. Phone (508) 692-6606.

Circle No. 380

Prototyping Converter

- *Requires no soldering*
- *Accepts plastic quad flatpack sockets*

The 160QF100-R00-M prototyping socket converter accepts both 160- and 144-pin hinged-lid, ZIF plastic quad flatpack (PQFP) sockets and converts the footprints to a standard 100-mil matrix. You can then mount the converter assembly on standard prototyping boards. The female pins on the top of the converter accept the socket, allowing for easy insertion and removal with no need for soldering. The converter can remain in place on the prototyping board; when any changes are necessary, you simply unplug the socket and replace it with whatever is required for the task at hand. Two converter sizes are available. The minimum-footprint version is only slightly larger than the size of the PQFP socket. The test-pin unit has two rows of test posts/side to facilitate signal monitoring. $166.

EDI Corp, Box 366, Patterson, CA 95363. Phone (209) 892-3270.

Circle No. 381

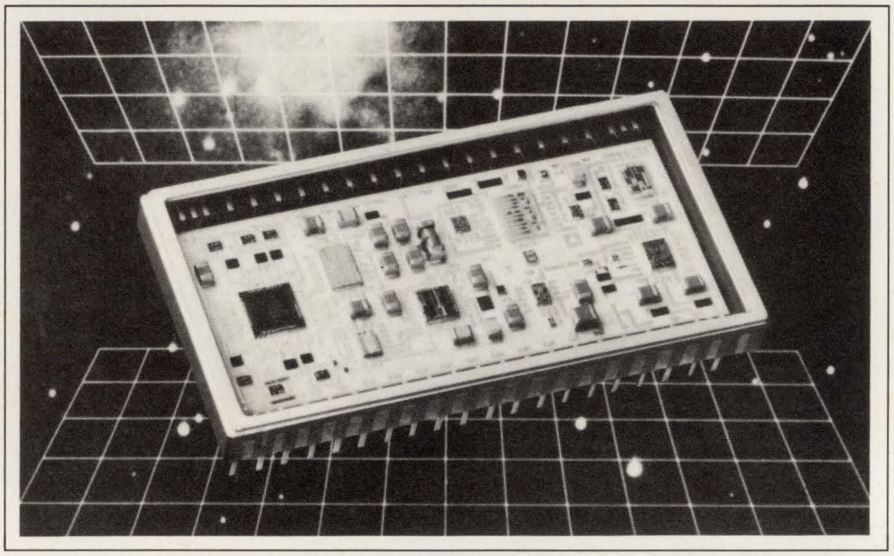
NEW PRODUCTS

INTEGRATED CIRCUITS

14-Bit Hybrid ADC

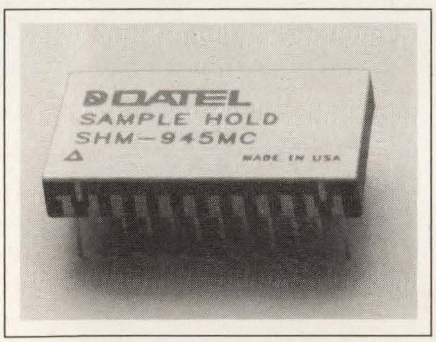
- *Contains T/H circuit*
- *Conversion speed is 5 MHz*

Packaged in a hermetic 40-pin TDIP, the ADC-00145 contains a 14-bit A/D converter, a 200-nsec track/hold circuit, 3-state output buffers, and timing circuits. Capable of converting at a 5-MHz rate, the device uses a 2-step conversion algorithm. A pulse input to the encode-command pin initiates the conversion cycle. After the T/H circuit samples and stores the analog input, a flash ADC generates a coarse encode of the sampled voltage and stores its 8 bits in the MSB register. At the same time, a high-speed DAC converts the 8 bits to an analog voltage, which is subtracted from the original input. The flash ADC then generates a fine encode of the subtracted voltage and stores



these 8 bits in the LSB register. Digital error correction combines the coarse and fine data to yield a 14-bit output. The ADC-00145 operates over −55 to 125°C. From $1200. Delivery, 8 to 12 weeks ARO.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600, ext 419. FAX (516) 567-7358. **Circle No. 382**



High-Speed S/H Amplifier

- *Delivers 16-bit accuracy*
- *Acquisition time is 500 nsec*

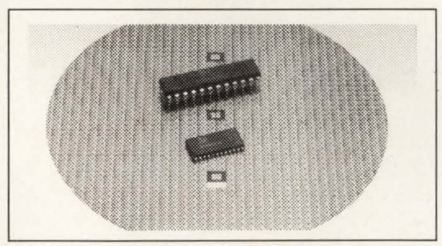
The SHM-945 is a high-speed S/H amplifier characterized for both 16-bit and 14-bit applications. At 16-bit resolution, the hybrid circuit features a maximum acquisition time of 500 nsec to ±0.00076% (±½ LSB) for a 10V full-scale step. At 14-bits, the device has a maximum acquisition time of 350 nsec to ±0.003% (±½ LSB). The amplifier features a differential input, which provides rejection of common-mode noise. Other specifications include feedthrough rejection of 100 dB, hold-mode rms noise of only 60 μV, aperture uncertainty of 10 psec, and a bandwidth of 16 MHz. The device operates from 5 and ±15V supplies. Packaged in a 24-pin DDIP, the SHM-945, in commercial and military temperature ranges, $79 and $87, respectively (OEM qty).

Datel Inc, 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000. FAX (508) 339-6356. TLX 174388. **Circle No. 383**

Sampling A/D Converter

- *12-bit resolution*
- *333-kHz throughput*

The SP7800 sampling A/D converter features a 333-kHz throughput at 12-bit accuracy and resolution. In addition to a 12-bit ADC, the monolithic device contains an internal S/H circuit, a reference, a clock, a microprocessor interface, and 3-state outputs. Dynamic performance includes a S/N ratio of 72



dB, a spurious-free dynamic range of 80 dB, and THD of −80 dB. The device supports standard input ranges of ±5 and ±10V. The SP7800 is available in a 28-pin plastic DIP, 28-pin side-brazed ceramic DIP, and 24-pin SOIC packages. Commercial grade parts, from $23 (100).

Sipex Corp, 6 Fortune Dr, Billerica, MA 01821. Phone (508) 663-9691. **Circle No. 384**

BiCMOS Decoder PLDs

- *Have 6- or 7-nsec propagation delay*
- *Support system clock rates to 50 MHz*

Optimized for address-decoder ap-

plications, the 12-input, 8-output fuse-programmable BiCMOS PLDs feature propagation delays of 6 or 7 nsec. The 336 and 337 models of this series have registered inputs; the 338 and 339 have output latches. The 336 and 338 have two product terms per output; the 337 and 339 have four product terms per output. The chips with registered inputs accommodate most RISC (reduced-instruction-set computer) processors, including SPARC and Mips, which assert addresses for only a short period around the clock edges. The chips with output latches accommodate processors that do not issue an address with every clock cycle and that remove addresses and data before the end of the clock cycle, a behavior that is typical of CISC (complex-instruction-set-computer) processors such as the 80486 and 680x0. The decoder PLDs come in a variety of packages including DIP, SOJ, LCC, and PLCC (plastic leaded chip carrier) types. $14.30 to $16.35 (100).

Cypress Semiconductor, 3901 N First St, San Jose, CA 95134. Phone (408) 943-2600.

Circle No. 385

Color-Palette D/A Converters

- *Compatible with RS-170*
- *Data rates from 35 to 110 MHz*

The TMC0171 and TMC0176 color-palette D/A converters contain three 6-bit DACs, a 256-word × 18-bit RAM look-up table, and a standard MPU interface for writing and reading the RAM. An 8-bit data input addresses the RAM, selecting one of the 256 18-bit words that determine the specific 6-bit levels of red, green, and blue colors. The devices, which cover data (pixel) rates from 35 to 110 MHz, are compatible with the RS-170A standard and directly drive the red, green, and blue analog inputs to CRT monitors. The TMC0171 is available in speed grades of 35 and 40 MHz. The TMC0176, which includes a power-down control for use in battery-operated systems, is available in speed grades of 40, 50, 66, 80 and 110 MHz. Package options include 28-pin DIPs and 44-lead PLCC's (plastic leaded chip carrier). Depending on type and speed grade, $3.38 to $6.82 (100).

TRW LSI Products Inc, Box 2472, La Jolla, CA 92038. Phone (619) 457-1000. FAX (619) 455-6314.

Circle No. 386

Resolver-To-Digital Converter

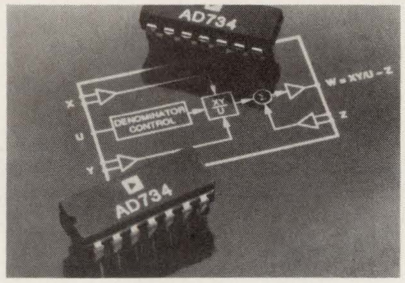
- *Replaces optical encoder*
- *Has 1.3 arc-minute accuracy*

Designed to replace optical encod-

ers in high-resolution military applications, the 16-bit HRD1416 resolver-to-digital converter comes in a 1-in.-square, hermetically sealed, 32-pin package. The Type-II tracking converter operates from a single 5V supply and consumes only 75 mW of power. Compatible with both 8- and 16-bit microprocessors, the converter features an accuracy of 1.3 arc-minutes. An internal 0.5 or 1.0V-rms reference signal generates as much as 10 mA of drive, allowing direct connection to most resolvers. An anti-180° false-lock-up circuit prevents the converter from locking into an angle 180° from the true angle. A transparent latch with 3-state outputs, configured as two independently enabled 8-bit bytes, eases the transfer of data from the converter. A built-in test feature provides a logic "1" when the tracking error exceeds ±1°. The HRD1416 is built using MIL-STD-883B processing. From $525. Delivery, 16 weeks ARO.

Natel Engineering Co Inc, 4550 Runway St, Simi Valley, CA 93063. Phone (805) 581-3950. FAX (805) 584-4357. TWX 910-494-1959.

Circle No. 387

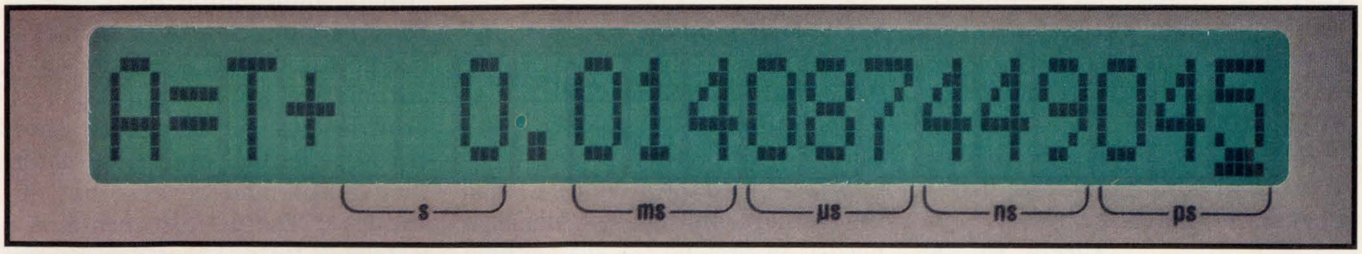


Analog Multiplier/Divider

- *Bandwidth is 10 MHz*
- *Slew rate is 450V/μsec*

Operating with a full-power bandwidth of 10 MHz, the AD734 multiplier/divider offers a slew rate of 450V/μsec, a S/N ratio of 94 dB, and a guaranteed conversion accuracy of 0.25%. The device performs the mathematical function W=XY/U, where X, Y and U are fully differential analog-input signals. Connected as a four-quadrant multiplier, the device can function as an oscillator, filter, or voltage-controlled amplifier. Connected as a 2-quadrant divider, the device can function as an automatic-gain-control (AGC) amplifier or an rms-to-dc converter. A direct-divide mode allows users to optimize the dynamic range for varying input-signal spans. Because of its 40-MHz input bandwidth, you can also use the device as a demodulator or mixer in heterodyne receivers. The third-order intercept point is 43 dBm, and the 1-dB compression point is 18.6 dBm for an 8.46V signal across 1 kΩ. Third-order intermodulation distortion (IMD) is −75 dB. The

Go ahead ... add 5 psec



Picoseconds are no problem for the DG535 Precision Pulse & Delay Generator.

The DG535 provides 4 edge (delay) and 2 pulse (delay and width) outputs, all with 5 ps resolution, 1000 sec range, 50 ps rms jitter, and adjustable output levels. The outputs drive 50 Ohms or high impedances to 4 Volts with a slew rate of 1 V/ns - just right for driving TTL or ECL or even high speed analog circuits. Throw in the 35 Volt output option and you can trigger almost anything. For even greater accuracy and stability, add the 1 ppm optional timebase .

Top it off with the intelligent menu-based front panel and standard GPIB interface, and the DG535 is probably the most versatile timing generator you can find.

On the bench or in a test environment, the DG535 has the accuracy, stability, precision, and reliability you need to solve your tough timing problems - all at a price you can afford. Call SRS for more information on the DG535, even if you don't need picosecond resolution.

DG535	**$3500**

- 4 delay, 2 pulse channels
- 5 ps delay resolution
- 50 ps rms jitter from trigger
- Adjustable output levels to 4 Volts
- 0 to 1000 sec delay range
- Internal/external trigger to 1 MHz
- Internal/external timebase
- 9 location set-up memory
- GPIB interface standard
- ±35 Volt output option
- 1 ppm timebase option
- 100 ps rise/fall time option

SRS **STANFORD RESEARCH SYSTEMS**

1290 D Reamwood Avenue, Sunnyvale, CA 94089 TEL (408) 744-9040 FAX 4087449049 TLX 706891 SRS UD

AD734 is available in a 14-pin ceramic package, two temperature grades, and three accuracy grades. AD734AQ, with 0.1% accuracy, $10.55 (100).

Analog Devices Inc, 181 Ballardvale St, Wilmington, MA 01887. Phone (617) 937-1428.

Circle No. 388

Bus Driver/Receiver IC

- *For analog multiplex-bus networks*
- *Designed for automotive applications*

The CS-8425 bus-driver/receiver IC interfaces with the system's μP and the sensors and control elements needed to provide the system with specific information or functions. Designed for class-A multiplexed bus networks such as those used in automotive applications, the IC provides protection against short circuits, thermal overload, voltage transients, and reverse-battery voltages. The IC also contains a watchdog feature that you can use to disable the power-output stage. Two operating modes are available. The polling mode provides synchronous access to each of 30 possible sensors on the bus. The command mode allows random access to any of 32 control elements on the bus. Each mode relies on the IC to interpret digital input information and then communicate with the system by placing analog signals on the bus. CS-8425, in 16-pin DIP and 20-pin SOIC packages, $1.60 and $1.70 (1000), respectively.

Cherry Semiconductor Corp, 2000 South County Trail, East Greenwich, RI 02818. Phone (401) 885-3600. **Circle No. 389**

64k-Bit Nonvolatile Smart RAM

- *Includes real-time clock*
- *Organized 8k × 8 bits*

The MK48T08 and MK48T18 Smart RAMs each contain a low-power 8k × 8-bit CMOS static RAM (SRAM), a CMOS clock and power-fail detection circuits, a crystal, and a lithium battery. The devices, which provide time and data retention without need of external power, have access times of 100 and 150 nsec. The devices operate with a standard SRAM memory access, without need for any special write-timing requirements and without limitations on the number of write cycles. Integral power-fail circuitry automatically provides chip deselect and write protection whenever V_{cc} falls below 4.75V (MK48T08) or 4.5V (MK48T18). Both devices also provide two chip-enable inputs and a power-fail output signal. Using a 24-hour BCD format, the clock func-

tions include year, month, date, day, hour, minute, and second. A control register lets you set, stop, restart, or calibrate the clock. They come in 28-pin plastic DIPs. From $22.50 (1000).

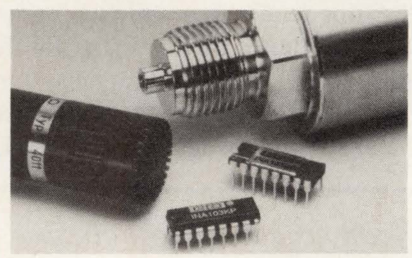
SGS-Thomson Microelectronics, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. FAX (602) 867-6290. **Circle No. 390**

Dual-Port Memory Module

- *Features 512k-bit density*
- *Has 16k × 32-bit organization*

Designed for high-performance applications employing 32-bit CISC (complex-instruction-set computer) or RISC (reduced-instruction-set computer) processors, the IDT7M1002 memory module features 512k-bit density and a 16k × 32-bit organization. The module, which mounts four IDT7006 16k × 8-bit dual-port devices on a 121-pin PGA package, is 1.8 in^2. To meet varying customer requirements, the dual-port module is available in access-time ratings of 40, 45, 50, 55, 65, 80, and 100 nsec. The vendor tests each module at the pin level as if it were a single monolithic component, using guardbanded ac and dc parametric tests over the operating temperature range. IDT7M1002, from $447.50 (100).

Integrated Device Technology, Box 58015, Santa Clara, CA 95052. Phone (408) 727-6116. FAX (408) 492-8674. **Circle No. 391**



Instrumentation Amplifier

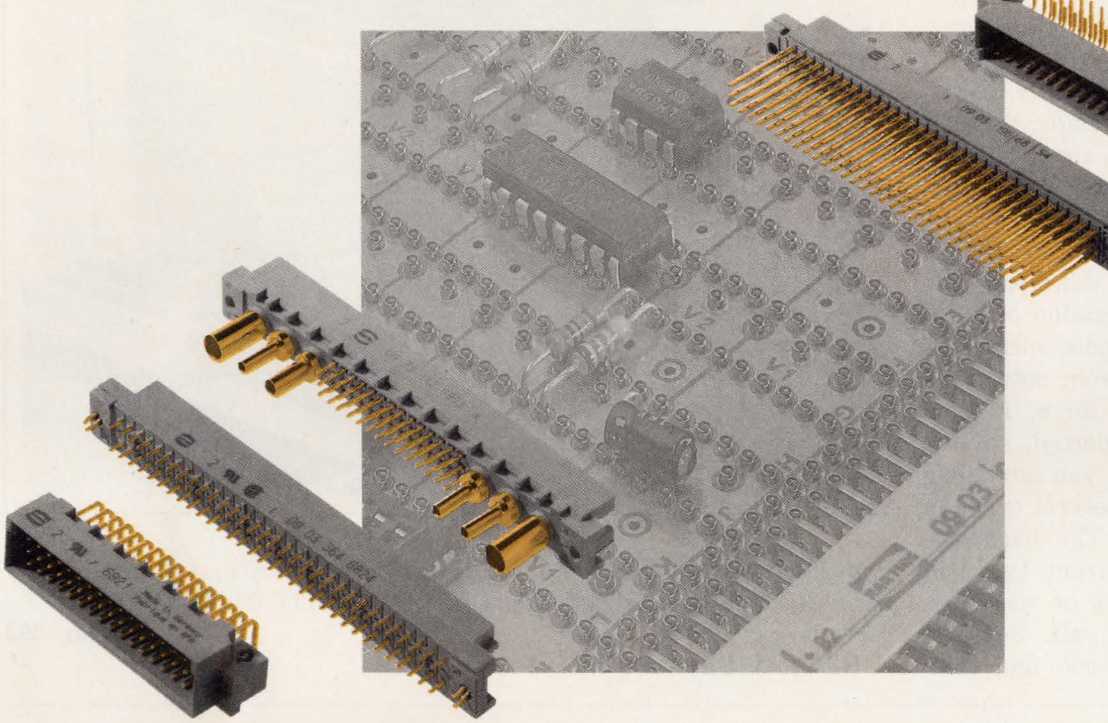
- *Noise is 1 nV/$\sqrt{Hz}$*
- *THD + N is 0.0009% at 1 kHz*

Designed primarily for use with low-source-impedance transducers, the INA103 instrumentation amplifier features a noise specification of only 1 nV/$\sqrt{\text{Hz}}$. The monolithic device incorporates a distortion-canceling input stage, which reduces THD + N to 0.0009% at 1 kHz. The device also includes gain-setting resistors for gains of 1 and 1000; external resistors can set the gain anywhere in the 1 to 1000 range. At a gain of 1000, offset voltage is 52 μV max, and drift is 1.25 μV/°C max. The INA103 comes in a 16-pin DIP and is available in commercial and military temperature grades. From $4.85 (1000).

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (800) 548-6132; in AZ, (602) 746-1111. FAX (602) 889-1510. **Circle No. 392**

Gds A DIN connectors

Efficient



HARTING is a hallmark of innovation and reliability worldwide – throughout the electronics industry and in the switchgear sector.

With the Gds A standard DIN 41612 printed circuit connectors, HARTING not only meets top requirements in terms of precision and quality but also makes a contribution to progress in the field of automation. The Gds A connector is mounted and fixed to the PC board in a single procedure. Components, solder pins and the fastening clips of the connector can thus be soldered in a single process.

With a comprehensive range of connectors, HARTING offers perfect solutions for all applications.

Connectors from HARTING – the quality connection

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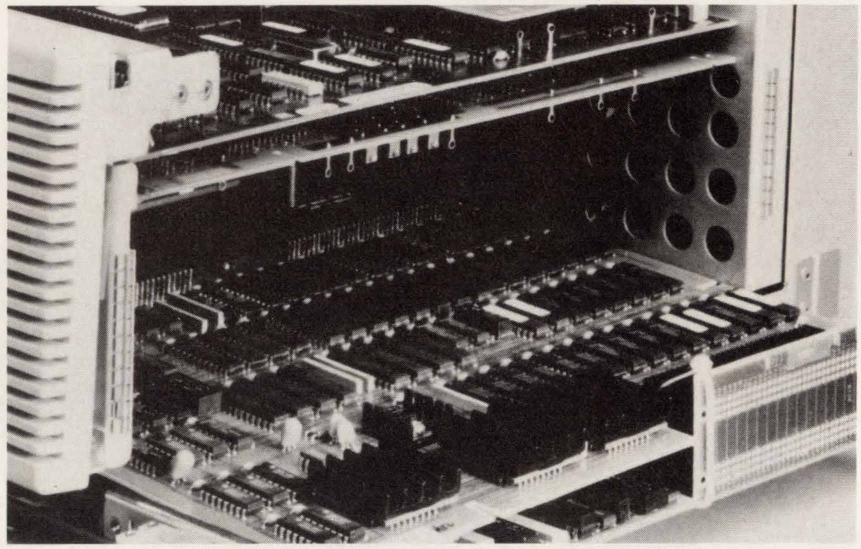
CIRCLE NO. 171

LAN Support For μP Development System

- *Consists of card cage, interface, and EPROM card*
- *Supports 8, 16, and 32-bit μPs*



The 67400A card cage, 67401A LAN interface card, and a companion EPROM card let you interface the vendor's μP development systems to local-area networks. Hence, you can upload and download code and control the operation of hardware development tools, such as in-circuit emulators, from networked workstations. Tools for 8, 16, and 32-bit μPs are supported, so that on a single network, you can debug systems based on several types of target processors. The hardware connects with different types of LANs either directly or via an attachment interface unit. Some of these LANs are thick- and thin-wire Ethernet, and StarLAN. Card cage, $6000; LAN card, $2500; flash EPROM card, $500.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

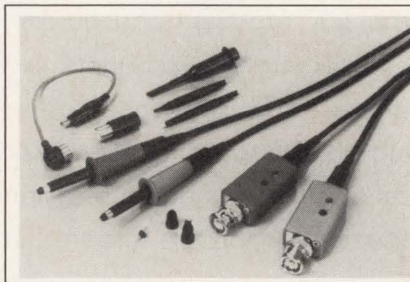
Circle No. 393

MS Windows-Based Data-Acquisition Drivers

- *Provide more than 70 services for creating tasks*
- *Let you take advantage of your hardware's speed*

The Driverlinx series family of language-independent dynamic-link libraries supports several vendors' data-acquisition boards under MS Windows V3.0's real, standard, and enhanced modes. Supported boards come from Keithley Metrabyte, Computer Boards, Soltec, and Advantech. The libraries provide developers with more than 70 services for creating foreground and background data-acquisition tasks. Such tasks include analog and digital I/O; frequency, period, and time measurement; and event and pulse counting. Applications communicate with the drivers by passing service requests that contain the specifications of the required task. Speed of operation is usually that of the hardware. C source code for the libraries' interactive demonstration program is included. $400.

Scientific Software Tools Inc, 30 E Swedesford Rd, Malvern, PA 19355. Phone (215) 889-1354. FAX (215) 889-1334. **Circle No. 394**



Differential Probe Set

- *Have 250-MHz bandwidth*
- *Permit adjustment of resistance and ac response*

The MD12F differential probe set lets you precisely match oscilloscope channels for accurate differential measurements. The probes work with signals from dc to 250 MHz. One of the probes in the pair lets you precisely adjust its attenuation at dc. Coarse and fine controls let you adjust the frequency response. The probe set has an attenuation of 10:1 and a rise time of 1.4 nsec. The probe set works with scopes whose input capacitance is from 10 to 60 pF. $340.

Test Probes Inc, 9178 Brown Deer Rd, San Diego, CA 92121. Phone (800) 368-5719.

Circle No. 395

80386SX Preprocessor For HP Logic Analyzers

- *Includes clip for contacting PQFP IC*
- *Also includes disassembly and configuration software*

The 386SX preprocessor works with HP 1650A/B, HP 1652A/B, HP 1654A/B, and HP 16510A/B logic analyzers. It has a software disassembler, configuration software, and a passive clip that facilitates connect-

SUPER
UNIVERSAL PROGRAMMER

SUPERPRO

Devices Programmed

- E(E)PROMS, FLASH EPROMS
- PALS, FPLS, PEELS, GALS
- EPLDS, EEPLDS
- MICRO CONTROLLERS
- BIPOLAR PROMS

ICs Tested

- TTL/CMOS, LOGIC ICS
- DYNAMIC/STATIC MEMORY DEVICES

Circle # 220

$795

SUPERPRO is a software controlled 40 - pin universal device programming workstation designed to meet all of your programming needs for different types of programmable devices.

A unique library - operating software structure provides the great flexibility to program most recent devices as well as many future devices. Integrated with IBM PC or compatibles via high speed parallel interface, SUPERPRO becomes the most high performance and cost effective programming solution in the market.

SUPERPRO's universal pin driven technology provides you with the utlimate device upgrade flexibility. Its 40 - pin GOLD ZIF socket and built - in protection for short circuit and over current make the SUPERPRO virtually indestructible.

GENERAL FEATURE

- Interfaces with IBM PC/XT/AT/386 or compatibles
- Reliable and fast programming w/Normal, Intelligent, Interactive and Quick Pulse algorithms
- Accepts standard file formats : JEDEC, INTEL Extended HEX, Motorola S, Tektronix HEX, and Binary formats
- Manages 16, and 32 - bit Word split
- Supports most compilers in JEDEC format such as ABEL, CUPL, PALASM, Tango PLD, OrCAD PLD, MINC PLD, and ISDATA
- Includes Test Vector capability and Multi - array Fuse Map Editor
- Tests TTL/CMOS Logic ICs & Dynamic/Static RAMs with user definable patterns

Optional Device Libray Generator

Optional Library Generator allows the user to update the software library by typing in the necessary data specifications and algorithms. This makes the LOPS software unlimited in terms of programming. Library Generator for SUPERPRO(SUPER - LG) contains a C - like programming language with a compiler.

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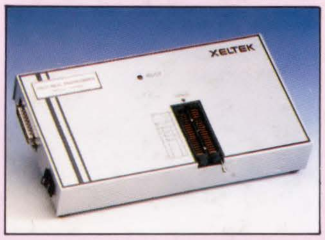
UNIPRO is a low-cost 40pin universal programmer. It contains most of general features from SUPOERPRO.

DEVICE SUPPORT
- PROM : All E(E)PROMs and Flash EPROMs of 24/28/32 pins up to 4 MBits
- Bipolar PROM : Signetics(82S···), (87S···), AMD/MMI(27S···, 63S···)
- PLD : PALs, EPLDs, GALs, and more
- Micro Controller : INTEL 87··· to Signetics 87C··· (Wide range of adaptors are available)
- IC TESTER : TTL(74 series), CMOS(40/45 series) logic, DRAM(4164, 41464···), SRAM(2114, 6116···)
- 32bit WORDSPLIT with 4 GANG adaptor
- PLASM2/CUPL/ABEL/TANGO/OrCAD JEDEC files
- PLA verification using test vector
- GAL electronic signature recognition



Circle # 221

OIPTIONS
- ADAPTORs for PLCC, LCC, SOIC, FLATPAK-type ICs
- 4 Socket Adaptor for E(E)PROM.
- Socket Adaptors for Micro Controllers.
- Package includes software, programming module, high speed interface card, & cable.

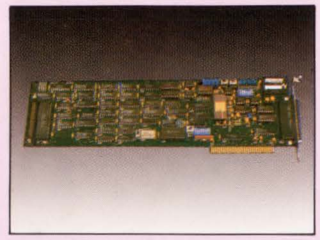
MCP-550

ADVANCED DATA ACQUISITION CARD

The MCP-550 is the ideal single-board solution for many data acquisition and control applications.

It is a high performance data acquisition card for IBM PC/XT/AT, integrated with A/D, D/A, D/I, D/C, and Timer/Counter functions. A built in Direct Memory Access circuit makes it possible to transfer data in high speed.

The MCP-550 is supported by a variety of vendor softwares which makes it ideal for wide range of industrial and laboratory applicatiions, such as Process Control, Automatic testing, Factory Automation, and Data Aquisition. Furthermore, it can be integrated with a PC and softwares to emulate many electronic devices. For example, Digital Oscilloscope, X-Y Recorder, Data Logger, and Programmable Controller are just a few on the list.



Circle # 224

- Multi functions in one card : A/D, D/A, D/I, D/O
- 16 single-ended or 8 differential analog input channel.
- A/D Sample Rate : 60KHz normal or 100 KHz max.
- 24 TTL compatible D/I & D/O channels
- Two 12-bit monolithic multiplying D/A channel

MFI-421

MULTIFUNCTION IN ONE INSTRUMENT

One Instrument With Four Test and Measuring System.
- Power Supply,
- Function Generator
- Digital Multimeter
- Frequency Counter

- Full Overload Protection
- Range : 1Hz ~ 100MHz
- Sensitivity : 1Hz ~ 60MHz : 15mV
  60MHz ~ 100MHz : 25mV
- Accuracy
  ± (1Hz + 1 dgt + Time Base Error)
- Output Waveform:
  Sine, Square, Triangle, Scewed Sine, Ramp, Pulse, TTL Level Square
- Frequency : 0.02Hz~2MHz
- Output : 0.1 Vpp ~ 20 Vpp
- Auto Ranging
  DCV, ACV, Ω, DCA, ACA
- Basic Accuracy : ± (0.5% + 2 dgts)

Circle # 222

- 3 1/2 Digit LCD Display of Voltage and Current
- Triple Output
  - Output # 1 : 0 ~ 50V, 0.5A max
  - Output # 2 : 15V, 1A(Fixed)
  - Output # 3 : 5V, 2A(Fixed)
- Ripple
  - Output # 1 : 1mV max
  - Output # 2, # 3 : 2mV max
- Load Regulation
  - Output # 1 : 0.01%+5mV
  - Output # 2, # 3 : Less than 35mV

MCP-520

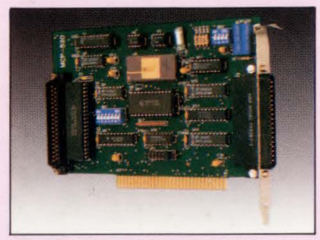
LOW-COST DATA ACQUISITION CARD

The MCP-520 is a cost effective single-board solution for many data acquisition and control applications.

It is a multi-function card for IBM PC/XT/AT or compatible computers, integrated with A/D, D/I, D/O functions on a single board.

In order for users to minimize their efforts for developing application softwares, a utility software diskette is provided, which includes drivers and sample programs.

- Multifuncations in one card : A/D, D/I, D/O
- Eight single-ended analog input channels
- Industry standard 12 bit resolution with sunccessive approximation



Circle # 225

- 24 TTL compatible Digital input/Digital output channels
- High speed analog to digital conversion with 60,000 samples/sec(15 sec)
- DMA and interrupt handling
- Signal Analysis
- Data logging and process control
- Monitoring and Controlling process
- Programmable signal generator
- Industrial ON/OFF control
- Contact closure monitoring

DDM-901

DIGITAL MULTIMETER TESTER

Autorange DMM With bar graph

- A/D convertor : 3 & 3/4 DIGIT CMOS LSI with auto range & auto polarity
- Display : LCD(Liquid Crystal Display), Max. indication 3999 or -3999
- Measuring Ranges : AC/DC Voltage & current, Resistance, Capacitor, Hfe, Frequency and Diode
- Range
  - CDV : 400mV, 4V, 40V, 400V, 1000V
  - ACV : 40V, 400V, 750V
  - OHM : 4KΩ, 40KΩ, 400KΩ, 4MΩ
  - DCA : 4mA, 40mA, 400mA, 2A, 10A
  - ACA : 400mA, 2A, 10A
  - CAPACITANCE : 10nF, 100nF, 1 μF, 5 μF,
  - FREQUENCY : DC to 400KHz> 400KHz(unspecified)
- Bar graph ZOOM and NULL function

Circle # 223

- Autopower cutoff
- Relative data Value display data hold by DMM
- Designed according to protection class II IEC 348
- Operating
  - Temperature : 0C to 40C (32F to 104F)
  - Humidity : 0% to 90% (0C to 35C), 0% to 70% (35C to 55C)

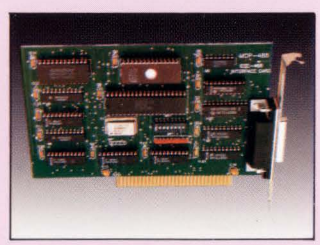
MCP-488

IEEE-488 INTERFACE CARD

The MCP-488 interface card complies with IEEE-488 standards, which is the most popular international standard for transferring information between electronic devices.

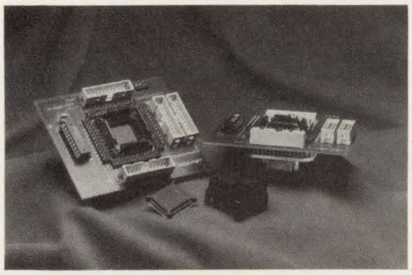
Comunication between PC and IEEE bus devices is possible because the MCP-488 interface card provides hardware and software. The firmware manifests its competance and handiness with programming languages or operating systems.

Interfaces ought to deal with hardwere book-keeping and timing while maintaining compatibility between a computer and peripherals. The MCP-488 handles IEEE-488 interface standards smoothly.



Circle # 226

- Complete compliance with IEEE-488 standards
- The software provides flexible and handy IEEE-488 language extentions for high level languages and operating systems.
- The printer port of IBM PC/XT/AT can be programed to a port for IEEE-488 devices
- Dierect memory access for high speed data transmission



ing to the 386SX μP in its surface-mounted, plastic quad flatpack. (HP refers to the disassembler as an inverse assembler.) Preprocessor, and four termination adapters, $1565.

Emulation Technology Inc, 2344 Walsh Ave, Santa Clara, CA 95051. Phone (408) 982-0660. FAX (408) 982-0664. **Circle No. 396**

Handheld DMMs

- *Include eight models*
- *Some measure capacitance to 9999 μF*

The 70 Series II consists of eight handheld digital multimeters; three of them are in bright yellow safety cases. The flagship models 79 and 29 make basic measurements with a resolution of 4000 counts and an accuracy of 0.3% for dc volts. They also measure frequency to 20 kHz and capacitance to 9999 μF. Convenience features, such as Touch Hold, simplify use. With this feature actuated, when you touch a probe to a voltage, the meter will hold its reading until you tell it to make another measurement. Therefore, you can watch where you're probing instead of watching the meter. $69 to $185.

John Fluke Mfg Co Inc, Box 9090, Everett, WA 98206. Phone (206) 347-6100. FAX (206) 345-5116. TLX 185102. **Circle No. 397**

High-Speed Pattern Generator

- *Provides eight channels at 680 MHz; four at 1.36 GHz*
- *Stores 16k or 32k states/channel*

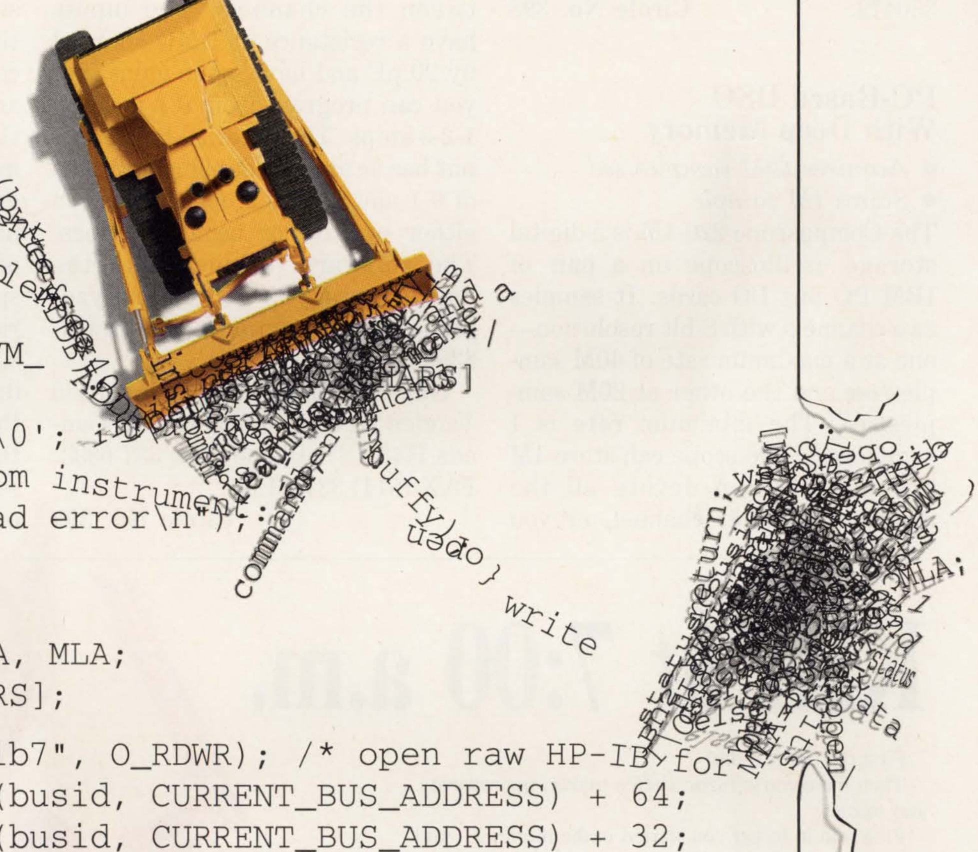
The PG-1400 high-speed pattern generator can produce an 8-channel output at 680 MHz or a 4-channel output at 1.36 GHz. In the 8-channel mode, it stores patterns 16k-states deep; in the 4-channel mode, it stores 32k-state patterns. You can connect as many as eight units together to produce 64-channel patterns at 680 MHz or 32-channel patterns at 1.36 GHz. As its host, the

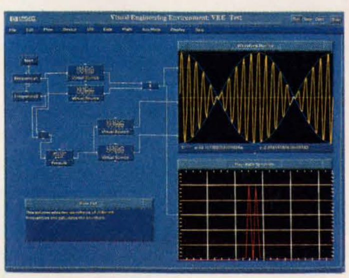
Finally, engineering software that clears the way to problem solving without programming.

```
void service(eid)
int eid;
{ int stat, byte;
/*serial poll
byte=hpib_spoll(eid
if ( (byte<0)||! (b
   printf("SRQ Prob
  return; }
stat=my_read(eid, DVM_
if (stat>0) {
   buffy[stat] = '\0'; i
   printf("Data from instrument:
else printf("I/O read error\n");
return; }

main() {
int busid, stat, MTA, MLA;
char command[MAXCHARS];

busid=open("/dev/hpib7", O_RDWR); /* open raw HP-IB for
MTA=hpib_bus_status(busid, CURRENT_BUS_ADDRESS) + 64;
MLA=hpib_bus_status(busid, CURRENT_BUS_ADDRESS) + 32;
stat = BUTTON_BIT ;
sprintf(command, "KM%02o", stat); /* 2 octal digits */
```





With HP VEE, you simply link the icons.

Computers are great for problem solving, if only programming didn't get in the way and slow you down. And now, it doesn't have to. Because the HP visual engineering environment (HP VEE) lets you solve problems without programming.

With HP VEE, you explore solutions visually by arranging and linking icons on the CRT. Each icon represents and executes a specific function for data collection, analysis —from simple mathematics to complex algorithms—and presentation. You don't have to write a single line of code.

There are two HP VEE software packages for prototyping, experimentation, and problem modeling. HP VEE-Engine, at $995*, is a general-purpose tool for analysis and presentation of existing data. HP VEE-Test includes HP VEE-Engine and adds extensive I/O capability, including soft panels and device I/O objects for $5,000*.

So, if programming is keeping you from finding solutions, call **1-800-752-0900.** Ask for **Ext. 2380**, and find out how HP VEE clears the way.

* U.S. list prices.

There is a better way.

HEWLETT PACKARD

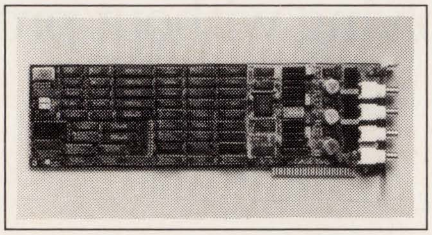
generator requires an IBM PC/AT or equivalent computer with a high-resolution color display and 10M bytes of free space on its hard disk. $38,500. Delivery, six weeks ARO.

Outlook Technology Inc, 200 E Hacienda Ave, Campbell, CA 95008. Phone (408) 374-2990. TLX 350479. **Circle No. 398**

PC-Based DSO With Deep Memory

- *Acquires 40M samples/sec*
- *Stores 1M sample*

The Compuscope 220-1M is a digital storage oscilloscope on a pair of IBM PC bus I/O cards. It samples two channels with 8-bit resolution—one at a maximum rate of 40M samples/sec and the other at 20M samples/sec. The minimum rate is 1 sample/sec. The scope can store 1M sample. You can devote all the memory to either channel, or you



can divide the memory equally between the channels. The inputs have a resistance of 1 MΩ shunted by 20 pF and have seven gains that you can program from 0.1 to 10 in 1-2-5 steps. The external-trigger input has ac and dc coupling and gains of 0.1 and 1. The scope triggers on either positive or negative slopes. The software included with the boards lets you store, analyze, print, and communicate data. $3900.

Gage Applied Sciences Inc, 5465 Vanden Abeele, Montreal, PQ Canada H4S 1S1. Phone (514) 337-6893. FAX (514) 337-8411.

Circle No. 399

Code-Generation Software For Data Acquisition

- *Queries you about your application*
- *Creates analog, digital, and counter/timer I/O routines*

Smartcoder software works with the firm's PCI-20026S-1 data-acquisition software drivers. This operation allows Quickbasic to create code that controls analog, digital, and counter/timer I/O functions on the firm's IBM PC-based instrumentation boards. The code-generation software frees you from having to know operational details of the boards and drivers. By responding to application-related queries displayed in menu form, you supply information needed by the drivers to initialize and configure the boards correctly. Depending on the speed of your computer, the software produced by the code generator can perform as many as

CIRCLE NO. 214

5000 read/write operations/sec. $95.

Intelligent Instrumentation/ Burr-Brown, 1141 W Grant Rd, MS 131, Tucson, AZ 85705. Phone (602) 623-9801. FAX (602) 623-8965.

Circle No. 400

Handheld 2- to 8-GHz Signal Generator

- *Provides at least 10 dBm*
- *Accepts TTL remote programming*

The Model 8001 signal generator produces an output of at least 10 dBm over the range of 2 to 8 GHz. The 2.52×5.57×7.45-in. handheld unit uses less than 10W of ac power and is programmable via a TTL interface. Frequency resolution is 1 MHz; accuracy is ±15 MHz. In normal mode, the generator can switch frequencies across the full band in less than 350 msec; in fast mode, switching takes less than 20 msec. At 20 kHz from the carrier, single-sideband phase noise is 80 dB below carrier level (−80 dBc). Second-harmonic output is at least −8 dBc, third-harmonic output is typically −14 dBc, and spurious outputs are −50 dBc. You can frequency-modulate the unit (40-MHz carrier deviation) with dc- to 200-kHz signals. $3750. Delivery, three to five weeks ARO.

April Instrument, Box 62046, Sunnyvale, CA 94088. Phone (415) 964-8379. FAX (415) 965-3711.

Circle No. 401

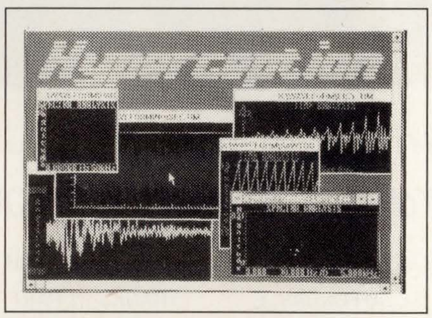
CIRCLE NO. 215

DSP Software

- *Usable for filter design and system analysis*
- *Handles both fixed- and floating-point implementations*

Version 2.0 of Monarch DSP software runs on IBM PCs and PS/2 series machines. The software helps you design FIR and IIR digital filters and perform signal and system analysis. It can calculate FFTs and inverse FFTs to 4k points. It supports fixed-point and floating-point realizations. It displays 2-D and 3-D graphics, and prints them out on more than 300 types of hard-copy devices. Version 2.0 software, $595; adaptive-filter module, $399; code generators for TI, AT&T, and Motorola DSP μPs, $99 each.

The Athena Group Inc, 3424 NW 31st St, Gainesville, FL 32605. Phone (904) 371-2567. FAX (904) 373-5182. **Circle No. 402**



MS Windows-Based DSP Software

- *Performs on-line and post processing*
- *Supports plug-in acquisition cards*

Hypersignal-Windows DSP software runs under MS Windows version 3.0. Some versions perform post processing of previously acquired data. Other versions support plug-in data-acquisition cards. These versions operate on data in real time as you acquire them. Among the functions you can perform are gap-free logging of data to a hard disk. You can obtain source code for the acquisition-card interfaces. Having access to this code simplifies the task of writing applications that use the hardware. The software provides "hooks" for coupling such user-written applications. $795 to $1995.

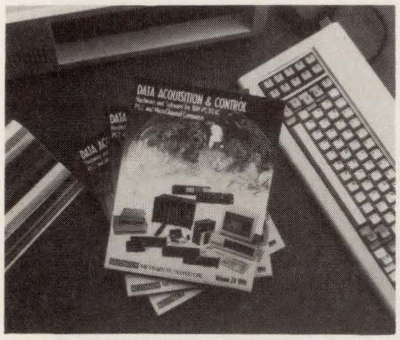
Hyperception, 9550 Skillman, LB 125, Dallas, TX 75243. Phone (214) 343-8525. FAX (214) 343-3457. **Circle No. 403**

Low-Power STD Bus Analog I/O Board

- *Provides 32 single-ended inputs and 2 outputs*
- *Auto-zeroing holds offset to 100 μV*

The LPM-AIO STD bus board has 32 single-ended analog-input channels and two analog outputs. It uses low-power CMOS devices; it consumes less than 820 mW. The board operates from −25 to +85°C and works with all CMOS STD bus processors whose clock speeds do not exceed 8 MHz. Overvoltage protection guards the inputs against damage from signals whose levels exceed the supply voltage by ±10V. An amplifier with software-programmable gains of 1, 10, and 100 conditions the input signals. An auto-zero cycle precedes each A/D conversion and typically holds offsets to 100 μV. The ADC converts with 12-bit resolution in 125 μsec. $525.

Winsystems Inc, Box 121361, Arlington, TX 76012. Phone (817) 274-7553. FAX (817) 548-1358. **Circle No. 404**



Near Plethora Of Products For 1991

The 1991 product handbook provides a comprehensive listing of data-acquisition, industrial-control and monitoring, signal-conditioning, personal instrumentation and communications products for IBM PCs, PS/2s, and Apple Macintosh microcomputers and compatibles. The 272-pg book also describes the Workhorse and Metrabus families of high-speed industrial control and monitoring products. Selection guides can help you find products you need to locate.

Keithley Metrabyte, 440 Myles Standish Blvd, Taunton, MA 02780.

Circle No. 405

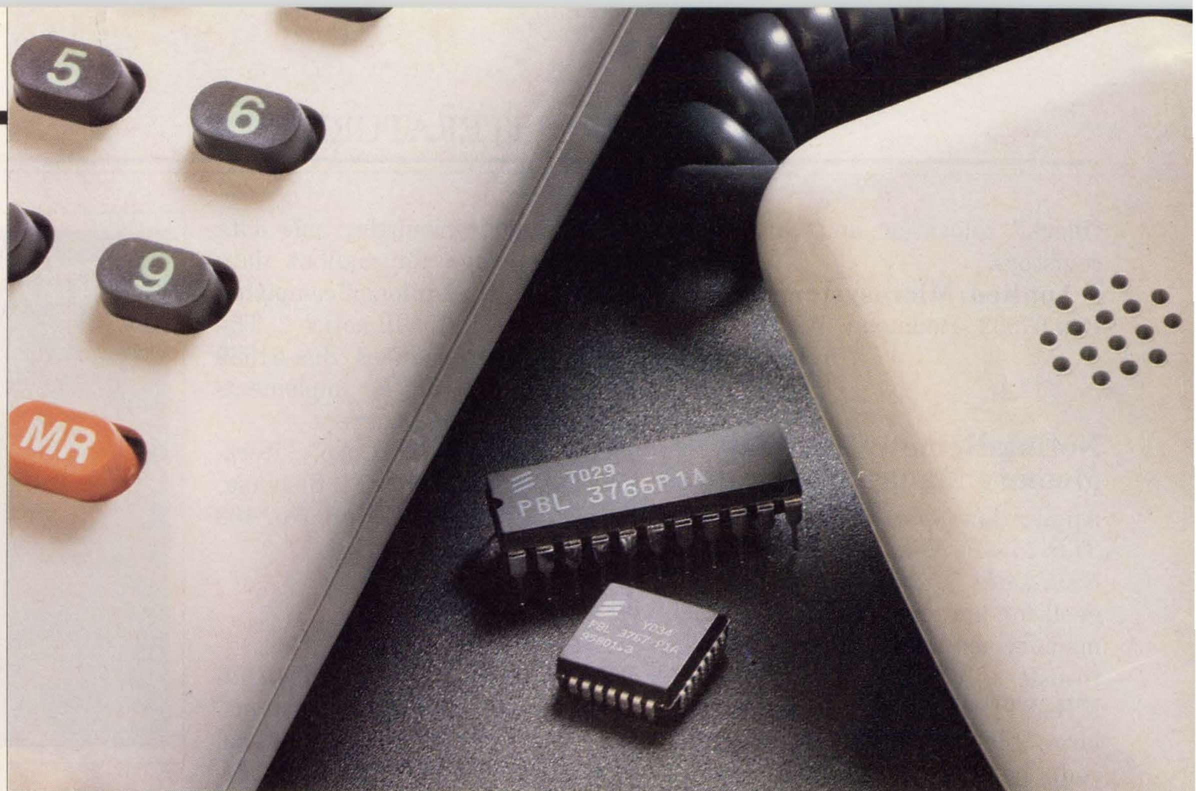
Brochure Surveys Applications For DSP

The subject of this 8-pg brochure is DSP-based solutions for high-end signal-analysis applications in military/SIGINT (signal intelligence), research physics, and satellite communications. Application notes explain pulsed radar, FSK, and other measurements. A description of the VMEbus-based analysis system includes comparing amplitude and frequency; spectrogram; and phase and view limits of color displays.

Tektronix Federal Systems Inc, Box 4545, MS 38-386, Beaverton, OR 97076. **Circle No. 406**

App Notes Discuss Embedded Systems

The Basics of High Speed Design explains how to design a reliable and functional high-speed digital system, delving into ground bounce, crosstalk, transmission lines, ground planes, and pc-board stack-up. *Networked Embedded Design Development Systems* discusses how to develop well-designed networks. *Transparent Connections for Embedded Microprocessor Systems Design Tools* deals with five types of transparency. It explains how you can build the five types of transparency (communications, execution, logical, electrical and mechanical) into an emulation system. *Event Monitor System for ES 1800 Emulators* covers the benefits and features of such a system. *Programming the 8018X/80C18X Peripheral Control Block* gives examples of how to set the



New SLICs cut the cost of on-premises/PBX subscriber lines

Lower cost chips that need fewer external components are the latest Subscriber Line Interface Circuit offerings from Ericsson.

Designed for cost sensitive applications such as general purpose PBX/Key systems, they give you three other major advantages over alternative solutions: wide supply voltage operation from -24 V to -58 V dc, on-hook transmission and a very low on-hook power dissipation of just 35 mW with -48 V dc supply or 20 mW when running from a -24 V dc supply.

So you can reduce the cost of your power supply circuit too!

Each SLIC includes loop current and ring trip detection, together with a ring relay driver. And they work with either a conventional or programmable CODEC/filter, all of which simplifies design.

Equally important, the new circuits are available in two versions: the PBL 3766 with a programmable constant loop current, and the PBL 3767 with programmable resistive battery feed and loop current limitation for short lines.

Both come in a choice of 22-pin plastic DIP or 28-pin PLCC packages with compliant 'j' leads.

Simply call us for full technical data or clip the coupon.

Please send me your latest PBL 3766 and PBL 3767 datasheets — **EDN 6/6/91**

Name

Company

Job Title

Address

Telephone

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403 International Parkway, Richardson TX 75081
Tel: 214 - 669 - 9900 Fax: 214 - 680 - 1059

Representatives: Alabama (205)880-8050. Arizona (602) 991-6300. California (408) 253-1960, (619) 292- 1771, (714) 891-4621. Colorado (303) 758-4884. Connecticut (203) 243-9343. Florida (407) 352-3755. Georgia (404) 448-1215. Illinois (312) 968-0118. Indiana (317) 577-9950. Iowa (319) 354-8894. Massachusetts (508) 692-2500. New Jersey (201) 525-8000. New York (516) 929-5756, (716) 586-0777, (518) 383-2239. N.Carolina (919) 847-8800. S. Carolina (803) 233-4637. Texas (214) 553-1200, (512) 834-8374, (713) 370-8177. Washington (206) 882-0962, (206) 254-4572. Wisconsin (414) 781-1730.

ERICSSON

"block" relocation and chip-select registers.

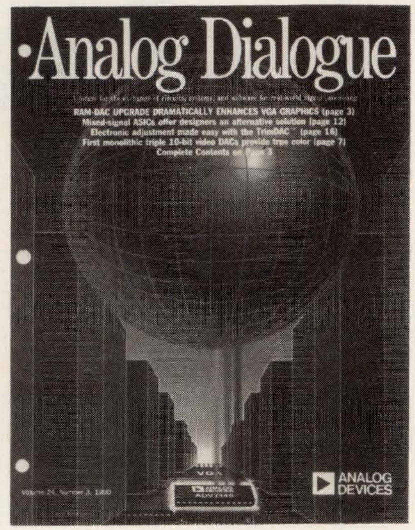
Applied Microsystems Corp, Box 97002, Redmond, WA 98073.
Circle No. 407

Noting Remote-Terminal Memory Management

Application Note AN/B-18, *A MIL-STD-1553B Notice 2 Solution For Bulk-Data Transfers*, explains the need for improved remote-terminal memory management in bulk data transfers. It discusses the use of the MIL-STD-1553 bus for transferring large blocks of data or program code between intelligent subsystems. Listing useful attributes for improved memory management, the note mentions the processing of multiple messages to the same transmit/receive subaddress without host-processor intervention; capacity for at least 64k words; receiving and transmitting bulk data blocks; storage for mailbox data blocks; and the option of complying with MIL-STD-1553B notice 2. The publication introduces Bus-61559 Aim Hy'er hybrids for implementing multimessage transfers.

ILC Data Device Corp, Literature Dept, 105 Wilbur Pl, Bohemia, NY 11716. **Circle No. 408**

Journal Reports On Circuits And Systems



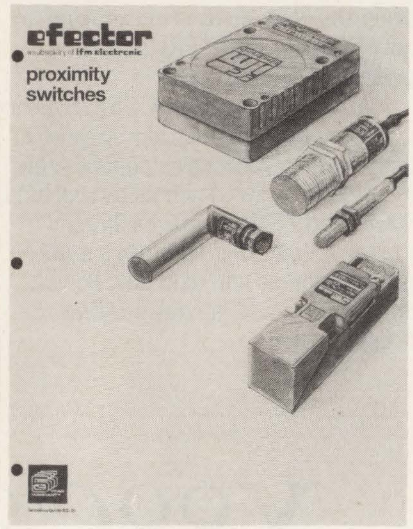
The quarterly journal, *Analog Dialogue,* focuses on circuits, systems, and software for real-world signal processing. The 28-pg Volume 24, No. 3 features three RAM D/A converters that enhance VGA graphics. It also covers a monolithic current transmitter, enhancements for DSP (IC processors and development tools), and two precision dual op-amp families. The regular feature, Ask the Applications Engineer, continues a discussion on op amps; the Worth Reading column provides a listing of app notes.

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. **Circle No. 409**

Source Book Illuminates Computer Systems

The Computer Systems Edition of the 1991 Industrial Computer Source Book reports on more than 500 related products. It sums up industrial-computer-system, data-acquisition, industrial-control, and communications products for IBM PCs, PC/XTs, PC/ATs, and compatibles. The expanded presentation includes 20-, 15-, and 10-slot rack and bench-top chassis, 8- and 15-slot chassis, and the Labtech Notebook with Iconview.

Industrial Computer Source, 4837 Mercury St, San Diego, CA 92111. **Circle No. 410**



Guide To Inductive And Capacitive Switches

This selection guide offers a line of inductive and capacitive proximity switches. An overview allows you to scan products by mechanical configuration, sensing range, or any of 15 other product parameters. The publication provides prices, dimension drawings, wiring diagrams, and electrical and mechanical specifications. Also included is information about mounting hardware and other accessories to simplify installation for position-sensing and level-detection applications.

Efector Inc, 805 Springdale Dr, Exton, PA 19341. **Circle No. 411**

Catalog Focuses On Measurement System

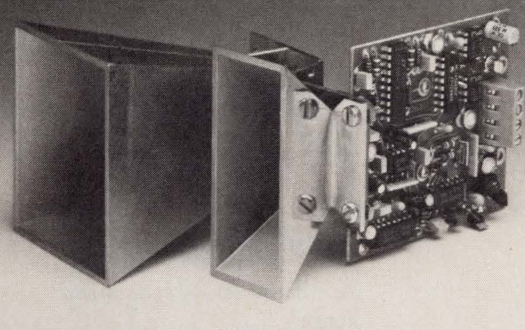
The catalog lists the company's modular measurement systems (MMSs) as well as systems from other vendors. It specifies more than 40 MMS components including modules, instruments, mainframes, and displays. The 160-pg publication describes resources and tools that simplify configuring the system, building custom modules, and ordering custom systems.

Hewlett-Packard Co, 19310 Pruneridge Ave, MS 49AM, Cupertino, CA 95014. **Circle No. 412**

Measure...

Displacement Proximity Level

With ALPHASENSORS' Microwave Sensor Technology



Microwave Sensors Offer:

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- Low Cost/High Performance

Put our **ALPHASENSORS'** microwave technology to the test—order our MSM 10200 Motion Sensor Evaluation Kit–$195, delivered from stock. For more information, call or write:

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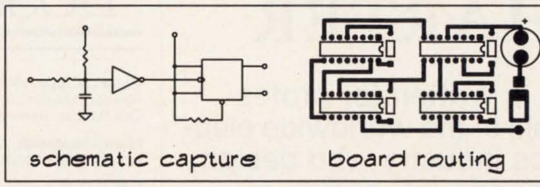
CIRCLE NO. 108

From schematics to printed circuit boards,



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will deliver high-quality, cost effective, turn-key assembled printed circuit boards from:

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- CAD GENERATED SCHEMATICS
- NETLISTS (most formats supported)
- HAND TAPED ARTWORK
- GERBER FILES
- or POSTSCRIPT FILES

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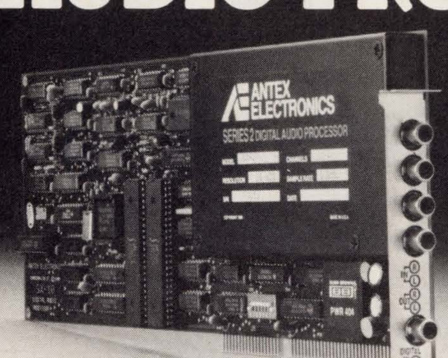
CIRCLE NO. 109

AUDIO PRO



Introducing... CD quality, stereo high fidelity, digital audio you record and playback on your PC-AT/286/386/Model 30 or compatible.

Featuring... real time direct to disk data transfer... 16-bit resolution... 20Hz to 20kHz audio response... 0.005% THD... 6.25 to 50kHz programmable sample rate... 92dB dynamic range... 90db s/n... digital input ... 4 to 1 ADPCM compression.

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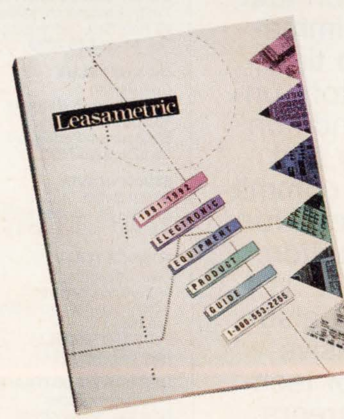
CIRCLE NO. 111

It's Here.

It's Free.

The 1991/92 Electronic Equipment Product Guide



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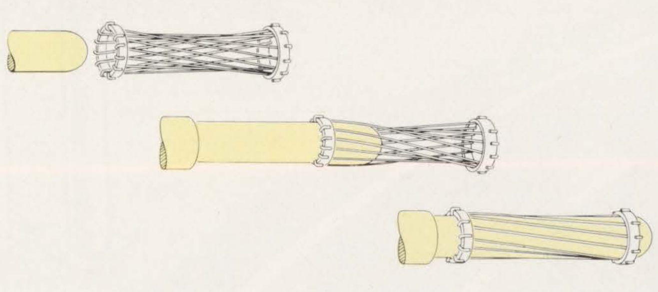

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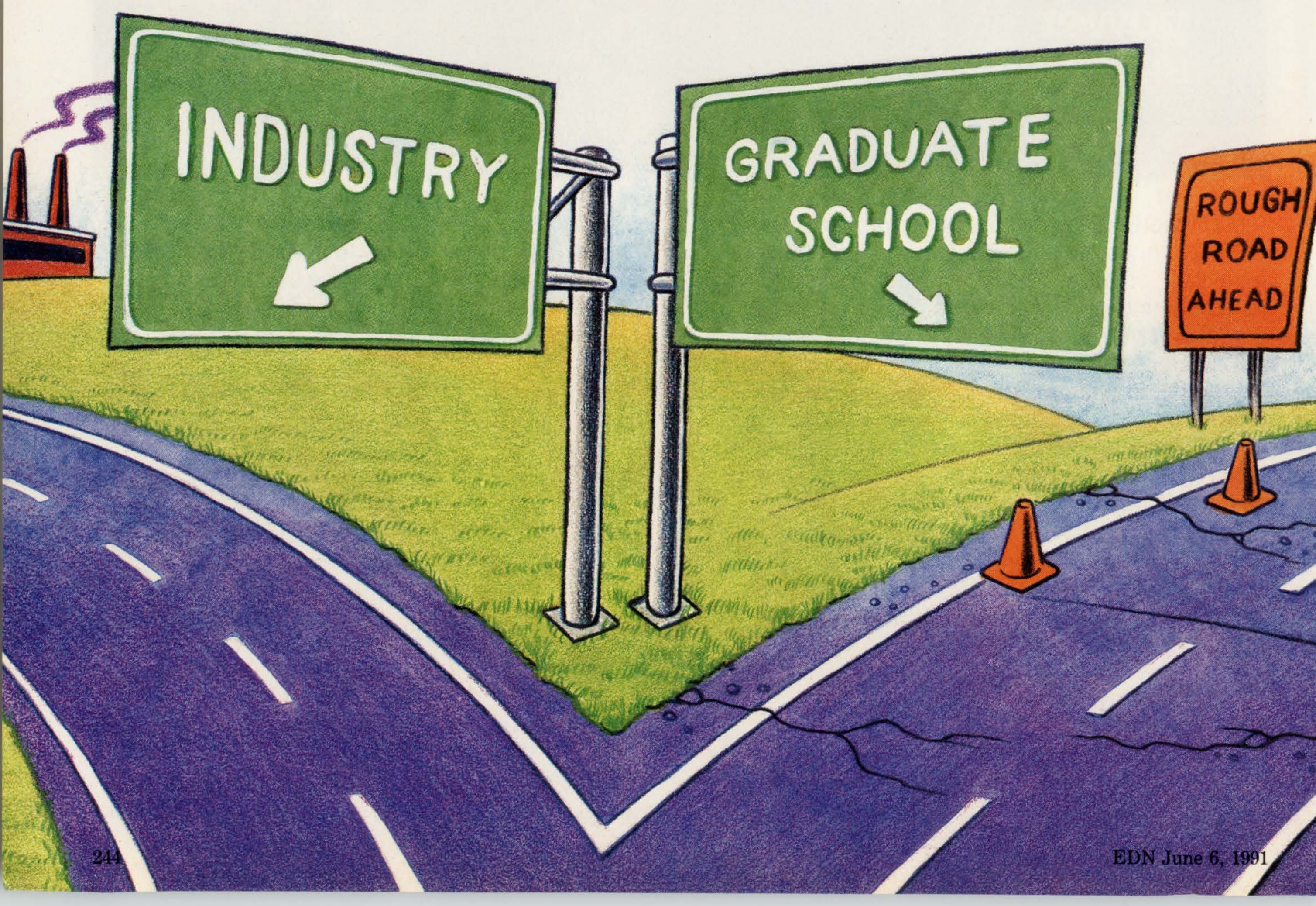
Engineering graduate schools

Jay Fraser, *Associate Editor*

Enrollments are declining, and a serious faculty shortage may lie ahead.

Americans make up approximately 95% of all students who receive bachelor's degrees in engineering from US schools, but less than 50% of those who go on to earn a PhD. Today more than half of the teaching assistants, research assistants, and faculty under 35 years old in our engineering schools are foreign nationals. Behind those statistics from the National Science Foundation lies a complex of interlocking factors—financial, psychological, academic, even ethnic—that may mean serious problems in the future for graduate-level engineering education and the engineering profession in this country.

The most overpowering reason why the majority of American students don't go on to graduate school is financial. More than half of all undergraduates now need some sort of financial assistance to pay for their educations. Because of current federal policy, they usually receive this assistance in the form of student loans. So going to graduate school would only sink them further into debt. In addition, some students, as soon as they graduate, are expected to help support their families or to help put a younger brother or sister through college. The pressure is very strong on many people to leave school after earning their



face a difficult decade

BS degree and start earning money as soon as possible.

This situation isn't helped by the low stipends that many schools pay their teaching and research assistants. A full professor with tenure may earn as much as an engineer of equal age and experience working in industry. Teaching and research assistants, on the other hand, usually receive only one-third to one-fourth the salary of someone with a BS and an entry-level job at a high-tech company.

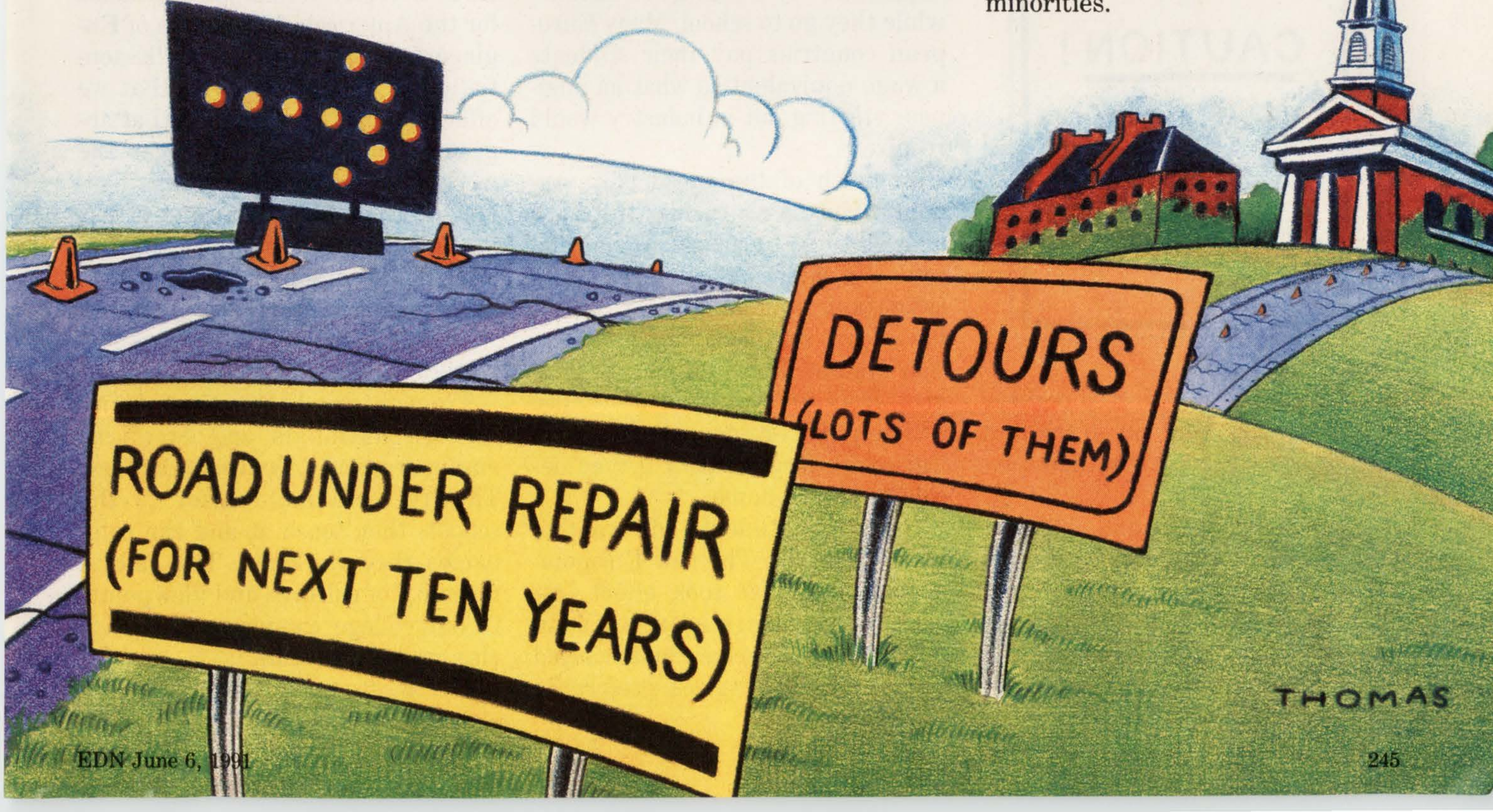
Another reason for the low number of Americans who go on for a master's degree or a PhD is that many students simply become tired of going to school. After grinding away for four or five years, a large number of students want to get out of academia and do something practical. They think of advanced degrees as being important for a career in teaching, but not really necessary for a career in industry, where they will gain knowledge through hands-on experience.

J Ray Bowen, Dean of Engineering at the University of Washington (Seattle, WA), points out that in graduate schools the courses too often aren't aimed at students who are seeking practical knowledge. "Some of those educational experiences that are designed to prepare students for advanced degrees are not necessarily applicable [to industry]," he says. "We have to enhance the design training in the advanced degree programs. We also need to introduce some courses related to engineering management and the management of technologies. We need to get more into the design of complex systems."

Educators believe that one way to raise the number of Americans enrolled in graduate engineering programs is to put more effort into recruiting people from those groups that have been traditionally underrepresented in the profession—women and minorities. In recent years engineering schools have worked to attract and retain women and minority students through increasing the number of scholarships available, setting up support groups, and providing academic counseling.

These efforts have shown positive but small results so far. According to the National Action Council for Minorities in Engineering, the number of African-American, American-Indian, and Hispanic freshmen has risen in the last five years. Members of these groups now make up 6.5% of all engineering graduates. However, only about 1% of the faculty of engineering schools are members of minorities.

Illustrations by Rod Thomas



Although the number of women enrolled in engineering programs has leveled off in recent years at approximately 15%, it too rose during the last decade. Women currently make up about 3% of engineering faculty members.

Women and minority students are, of course, subject to the same financial pressures and the same desire to leave school for industry as other students, but educators point to an additional reason why many women and minorities have not become faculty members until now. The fact that there have been so few women and minority instructors and professors in engineering schools means that students have lacked role models and mentors.

Another reason for low student interest in an academic career may underlie all the others. As Bowen puts it, "There's been a sort of malaise in many institutions about the attractiveness of a faculty career,

and that has been reflected perhaps in a poor marketing job on the part of university faculty for their profession."

At many colleges and universities, the road to tenure is through research and writing, not teaching. This emphasis discourages students who are interested in teaching, and hinders teachers from working more closely with students. Some professors only teach the bare minimum—one course per semester—so they can devote themselves to their research. Students perceive that a desire to teach could actually be dangerous to a faculty career. On many campuses you can still hear the old joke: "He was the best teacher I ever had. Don't tell the tenure committee."

All these reasons conspire to prevent American students from pursuing advanced degrees. According to the American Society for Engineering Education (ASEE), the number of Americans who received PhDs in engineering last year was about half of what it was in 1970. A much higher percentage of foreign-born students go on to graduate schools, not because they have a more pronounced taste for the academic life, but because many of the pressures American students live under don't affect them.

Some foreign graduate students don't feel the same financial pinch that Americans do because they're supported by their governments while they go to school. Many European countries pay their students a wage equivalent to what an engineer starting out in industry would receive.

In much of the world only students who pass grueling tests are allowed to go to college. Honor and pride, in addition to financial considerations, compel them to go as far as they can in the higher education system. Plus, an advanced degree from an American university will help them command more prestige and a larger salary if they decide to return home.

But many students will want to stay in the US. The new US immigration law that took effect last year gives foreign students an additional incentive to earn an advanced degree. The law gives preference to skilled and educated individuals. A PhD greatly increases a student's chances of becoming a permanent resident or a US citizen.

The result of this combination of factors is that foreign nationals now

make up more than half of all recipients of PhDs and more than half of all the faculty members under 35 years old in American engineering schools.

Some people see this as a cause for alarm, and some don't. Richard Ellis, Director of Manpower Studies for the American Association of Engineering Societies, says, "Essentially, we should be proud that we offer an educational system that appeals to people from all over the world. Our schools are clearly leaders internationally. It's one of the few places where Americans are still in a position of technological mastery and leadership."

Problems in the classroom

There's no doubt that many foreign nationals are excellent engineers and talented teachers. They're a valuable asset to the schools they teach at and the companies they work for. They add a diversity of cultures and viewpoints to our college campuses. But they also create problems.

The most obvious problem con-

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cerns language. Many foreign nationals speak less than perfect English, and this can make communication difficult. "There's some truth to that," says Ellis. "But at the same time, we caution people to be very careful about stereotypes. There are many foreign nationals in the schools whose English is better than yours or mine."

Another problem is cultural differences. Some foreign-born teachers come from countries where women are not treated as first-class citizens. In a survey of female graduate students conducted at MIT in 1987, the respondents indicated that they faced difficulties ranging from being left out of classroom discussions to being assigned less challenging assistantships. However, the women also said that it was not always foreign-born instructors who caused these problems.

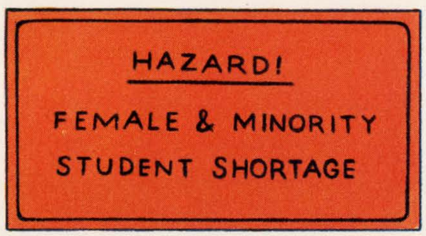
Looming on the horizon may be another problem that has far-reaching implications for US graduate schools and high-tech firms: The number of foreign-born engineering students and faculty members could decrease sharply at any time.

Recent events in the People's Republic of China are a good example of what might happen elsewhere. After the massacre in Tiananmen Square in June of 1989, the Chinese government cut back severely on the number of students allowed to study abroad and made it much more difficult for those who were permitted to leave. Now, before Chinese students travel overseas they must, in effect, post bond for themselves.

The number of foreign graduate students and faculty members may also decrease if the American economy continues to weaken. If foreign nationals feel there are better opportunities for them in their native countries, then more and more of them will return home. That will leave gaps in the student and faculty populations of US engineering schools as well as in high-tech companies.

A potential faculty shortage

Another problem is fast approaching that will exacerbate all the others. A 1989 report by the ASEE Task Force on the Engineering Pipeline estimates that by 1995,



25% of the engineering faculty in this country will reach retirement age. A large number of students enrolled in engineering programs in the late 1950s during the defense buildup of those years and the beginning of the space race, and consequently joined engineering faculties. As these people retire over the next decade, engineering schools will have to increase their efforts to fill faculty positions just to maintain their current levels of staffing.

Maintaining the quality of graduate schools of engineering in this country is extremely important, and the US can't depend on a constant number of foreign nationals to fill its teaching positions. It must assure itself of a reliable supply of first-rate American students who want to pursue advanced degrees in engineering and go on to faculty careers. Educators and professional organizations have analyzed the problems besetting US engineering schools and have come up with a number of recommendations.

The first place many people look for help is the federal government. It could aid graduate schools by creating more fellowships and increasing the amount of money it distributes as research grants. In addition, when government agencies are evaluating research proposals they should take into account not just the technical goals of the projects, but also the number of students who would be involved in them. However, with the trend these days toward cutting government spending, more federal funding may be hard to come by.

Industry can help in some of the same ways government can—providing more fellowships and sponsoring more research on campus. Many companies already have tuition reimbursement plans, and many engineers are willing to go back to school for an advanced degree if their companies will pay for it. However, they're put off by how long it will take if they have to go part time. Companies should try to make it possible for their employees to attend graduate school full time.

But engineering schools can't count on outside institutions to

solve their problems for them. First of all, they should take steps to ease the financial burden on students by increasing stipends for teaching and research assistants so that they equal the average starting salary in industry for someone with a BS.

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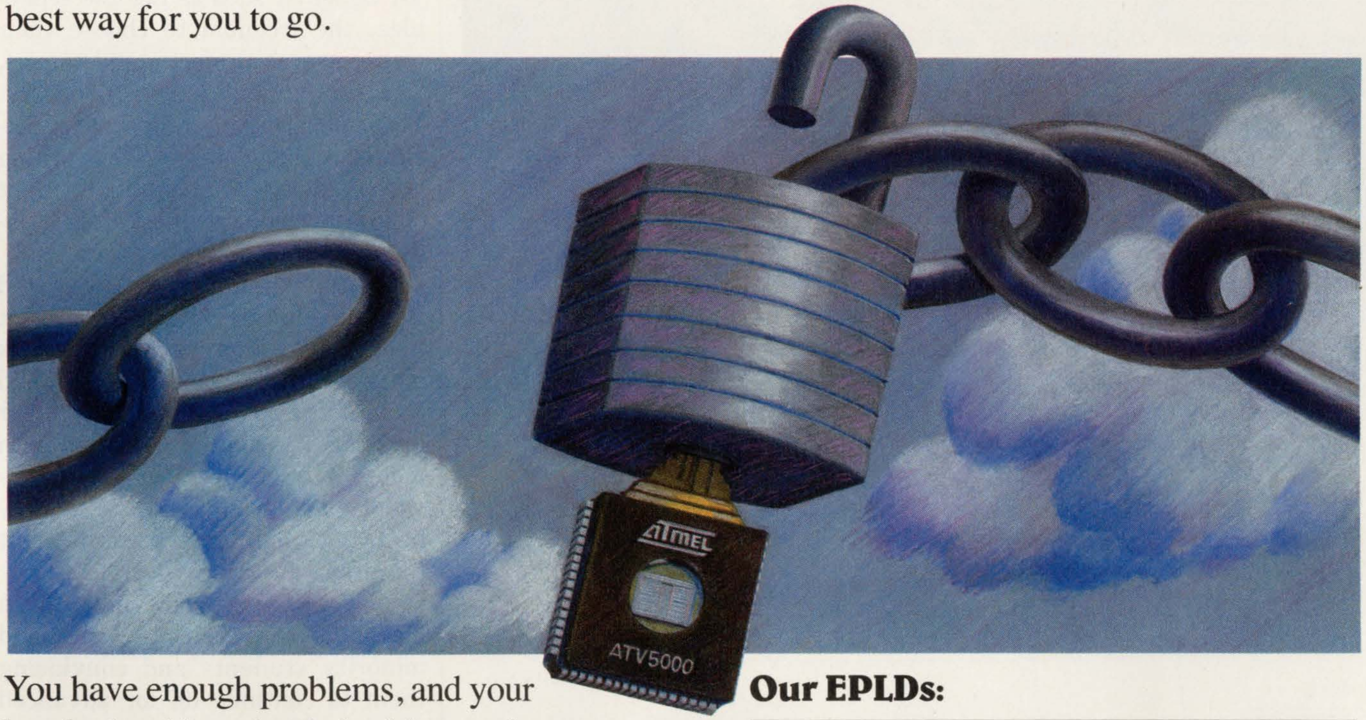

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PROFESSIONAL ISSUES

Educators should do more to encourage students to consider an academic career. Faculty members enjoy benefits, such as flexible schedules, the freedom to choose their own research projects, and tenure, that simply don't exist in industry. Teachers also get the personal satisfaction that comes from working with students. More students might choose a faculty career if they understood its rewards better.

For those students not interested in academic careers, but who want more thorough preparation to work in industry, graduate schools should include more courses that offer practical information and deal with real-world problems. Students won't go to graduate school if they believe it's only for those who want to pursue abstract research.

Engineering schools must do a better job of recruiting women and minority students and convincing them to continue on for advanced degrees. This is necessary not just to keep educating a sufficient number of engineers, but also to provide role models for younger students. With more role models visible, more women and minority students may enroll in engineering programs, and this problem might eventually solve itself.

In brief, if engineering graduate schools want to head off the problems they'll face in the decade ahead, they must make it much more attractive for students to go after advanced degrees. They're going to have to recruit students for faculty careers as aggressively as high tech firms recruit them for industry. EDN

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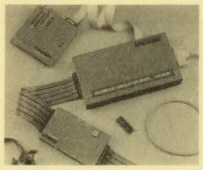

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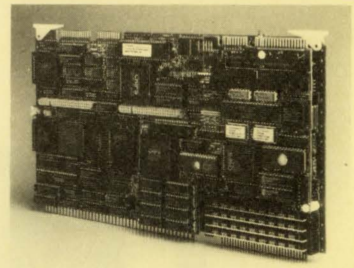

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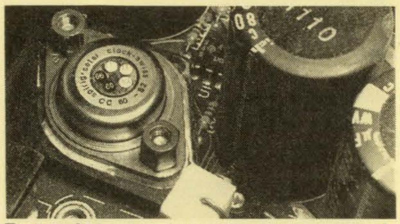

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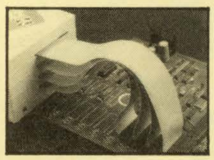

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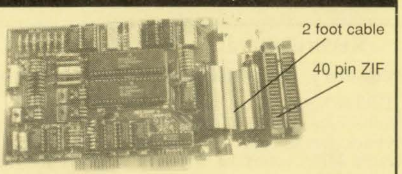

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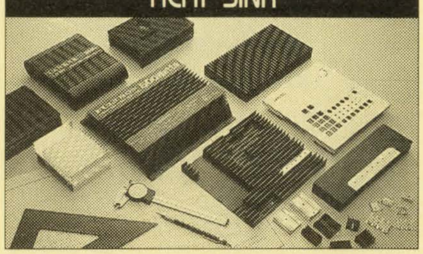

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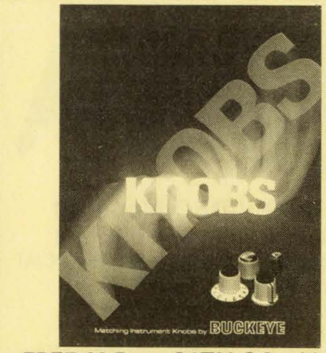

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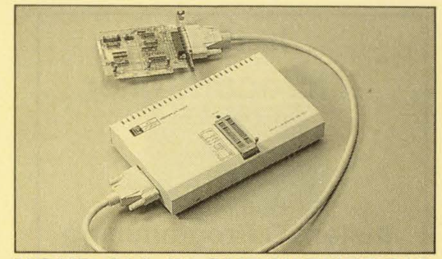

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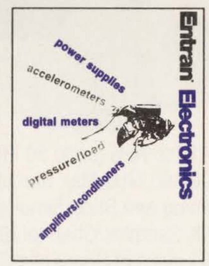

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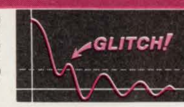

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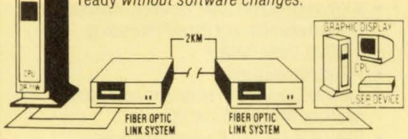

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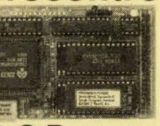

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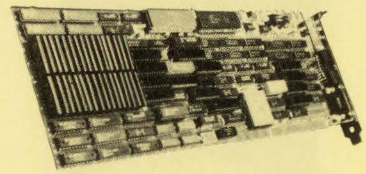

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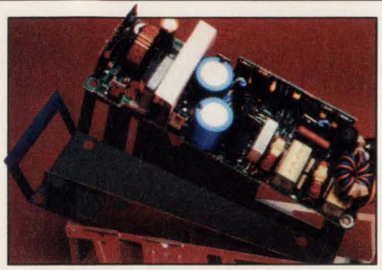

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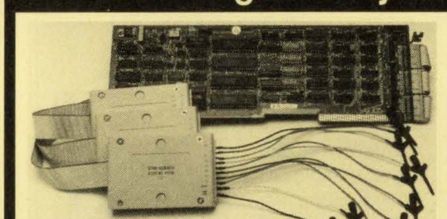

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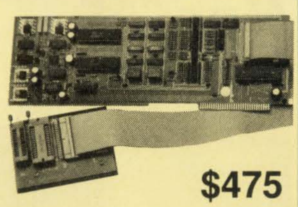

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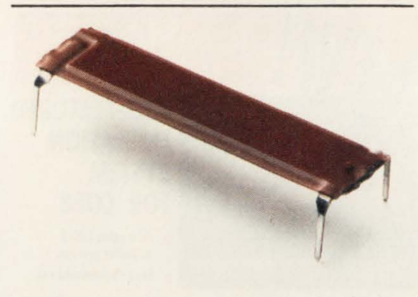

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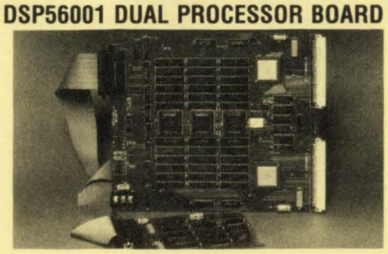

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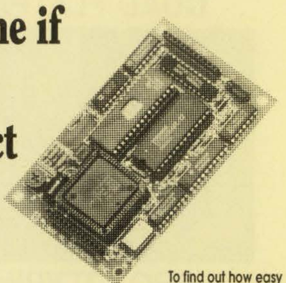

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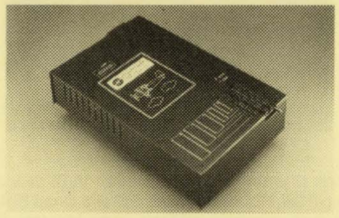

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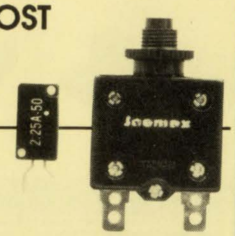

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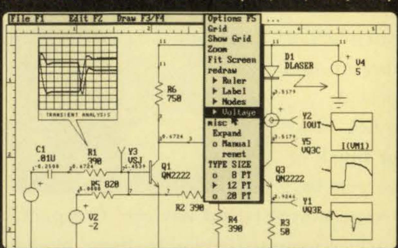

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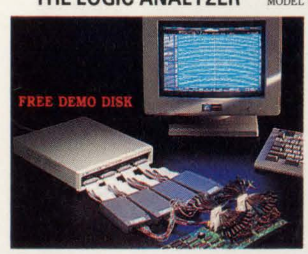

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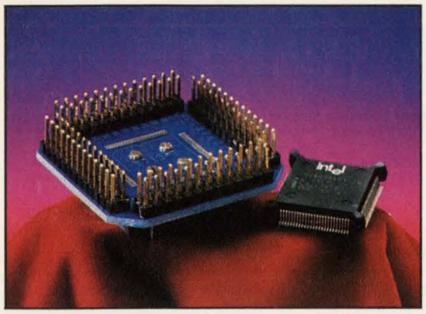

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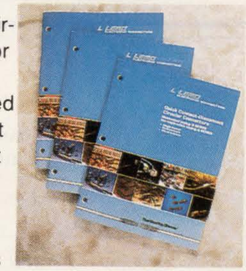

LEMO's new circular connector catalog highlights expanded shell and insert designs. Insert configurations are available in single, multi or mixed designs including signal, coaxial, triaxial, high voltage, fiber optic and fluidic/pneumatic. Shell styles are available in standard chrome plated brass, anodized aluminum or stainless steel.

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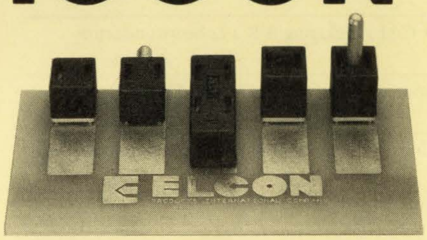

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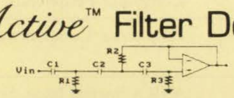

Val.	Calculated		Standard	units
R1	36.224	-->	33.000	kOhm
R2	9.913	-->	8.200	kOhm
R3	324.243	-->	300.000	kOhm
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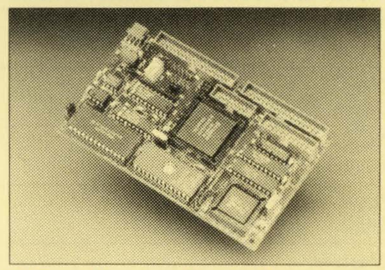

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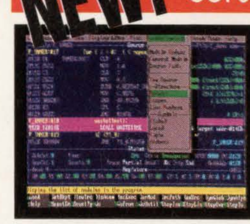

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Issue	Issue Date	Ad Deadline	Editorial Emphasis
News Edition	June 27	June 7	ICs & Semiconductors, RISC**, Regional Profile: So. California**
Magazine Edition	July 4	June 13	Product Showcase—Volume I • Interconnects, ICs & Semiconductors • Neural Networks • Power Sources, Software
Magazine Edition	July 18	June 26	Product Showcase—Volume II • Test & Measurement, Computer Peripherals • Components, CAE/ASICs •
News Edition	July 25	July 5	ICs & Semiconductors, Peripherals**, Regional Profile: Massachusetts**
Magazine Edition	Aug. 5	July 11	CAE • ASICs, Test & Measurement • Computers & Peripherals • Technical Article Database
News Edition	Aug. 8	July 19	CAE, Datacom**
Magazine Edition	Aug. 19	July 25	Military Electronics Special Issue, Image Processing • Ultra High Speed ICs/ASICs • Computer Peripherals, Software •
News Edition	Aug. 22	Aug. 2	Peripherals/Components, Test & Measurement**, Regional Profile: Idaho, Colorado, Utah**
Magazine Edition	Sept. 2	Aug. 8	ASICs Special Issue, Semicustom ICs • CAE, Packaging • ICs & Semiconductors Data Converters
News Edition	Sept. 5	Aug. 16	Military Electronics Special Issue, Computer Architectures, Defense Electronics**
Magazine Edition	Sept. 16	Aug. 21	DSP/Microprocessors, ICs & Semiconductors, CAE/ASICs, Environmental Engineering • Software
News Edition	Sept. 19	Aug. 29	RISC/ICs, Computers**, Regional Profile: Florida**
Magazine Edition	Oct. 1	Sept. 5	Computers & Peripherals/Networks, DSP Chip Directory • ICs & Semiconductors/ Memory Technology, Instrumentation
News Edition	Oct. 3	Sept. 13	ICs & Semiconductors, Multimedia**
Magazine Edition	Oct. 10	Sept. 19	Test & Measurement Special Issue, Oscilloscopes, VXI Board Directory • CAE/ASICs, Sensors & Transducers •
News Edition	Oct. 17	Sept. 27	ATE/Board & IC Testing, Artificial Intelligence**, Regional Profile: New Mexico & Arizona**
Magazine Edition	Oct. 24	Oct. 3	Telecommunications ICs, Graphics & Video Circuits, Computers & Peripherals, Software, Wescon Preview Issue
Magazine Edition	Nov. 7	Oct. 17	High Performance DSPs • CAE/ASICs, Computers & Peripherals/Communications, Software, Wescon Show Issue
News Edition	Nov. 14	Oct. 25	Telecommunications**, Wescon Show Issue
Magazine Edition	Nov. 21	Oct. 31	18th Annual Microprocessor Directory • Test & Measurement, CAE/ASICs, ICs & Semiconductors
News Edition	Nov. 28	Nov. 8	PC Cards, Board Level**, Regional Profile: Wisconsin, Illinois, Michigan**, EDN's Innovator/Innovation Awards Coverage •
Magazine Edition	Dec. 5	Nov. 14	Product Showcase—Volume I • ICs & Semiconductors, Microprocessors, Power Sources, Hardware & Interconnect, Software
News Edition	Dec. 12	Nov. 20	DSP**, Regional profile: DC, Maryland, Virginia**
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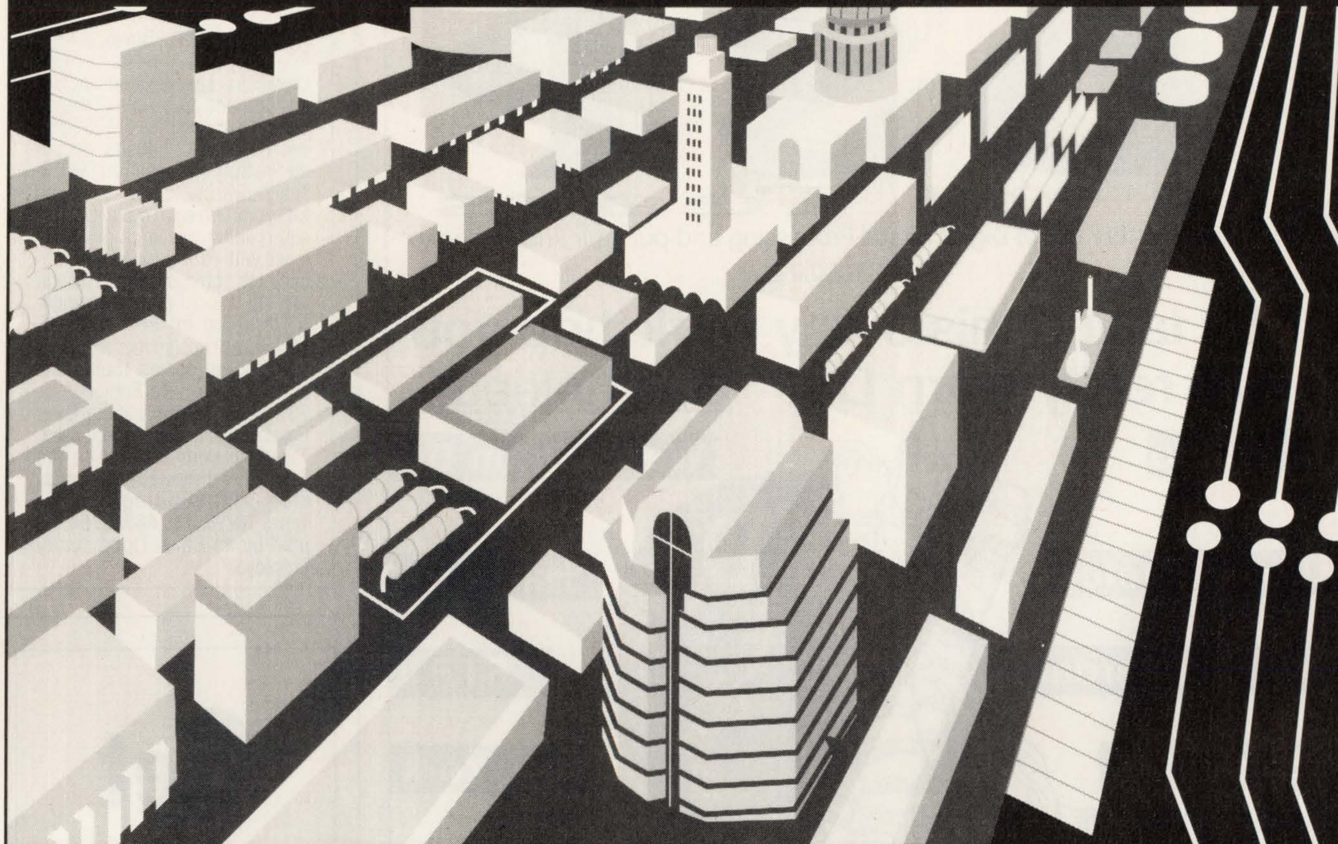

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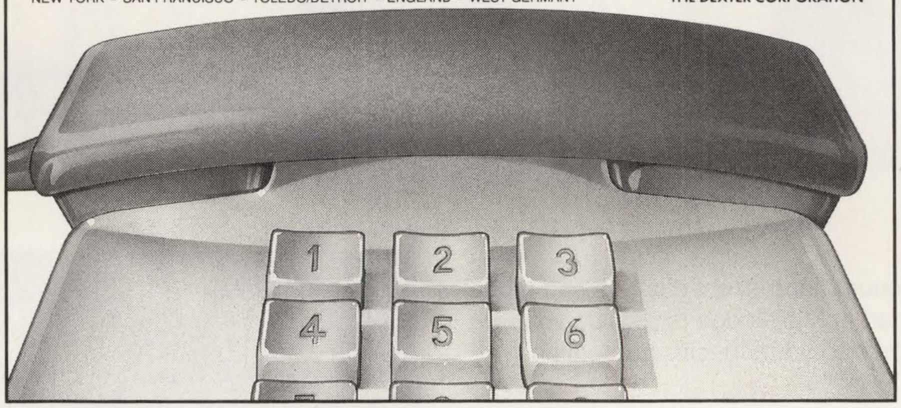

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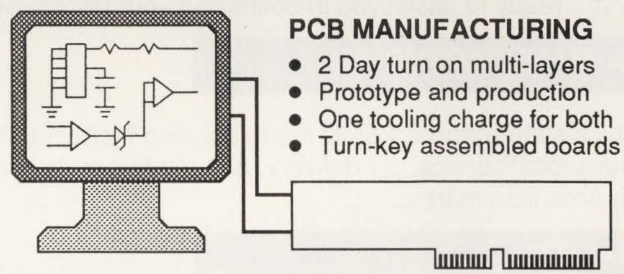

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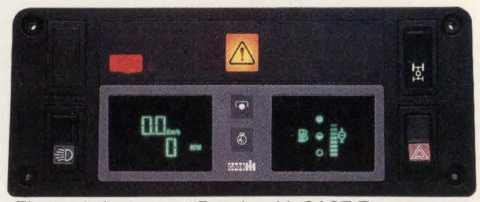

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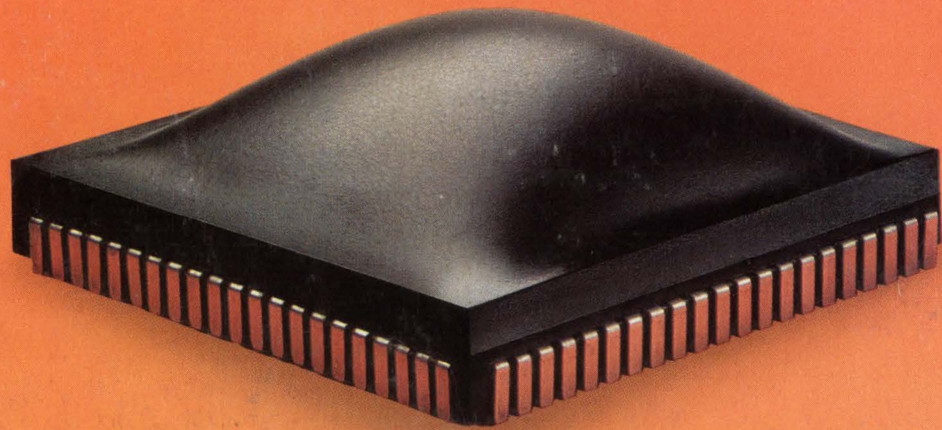

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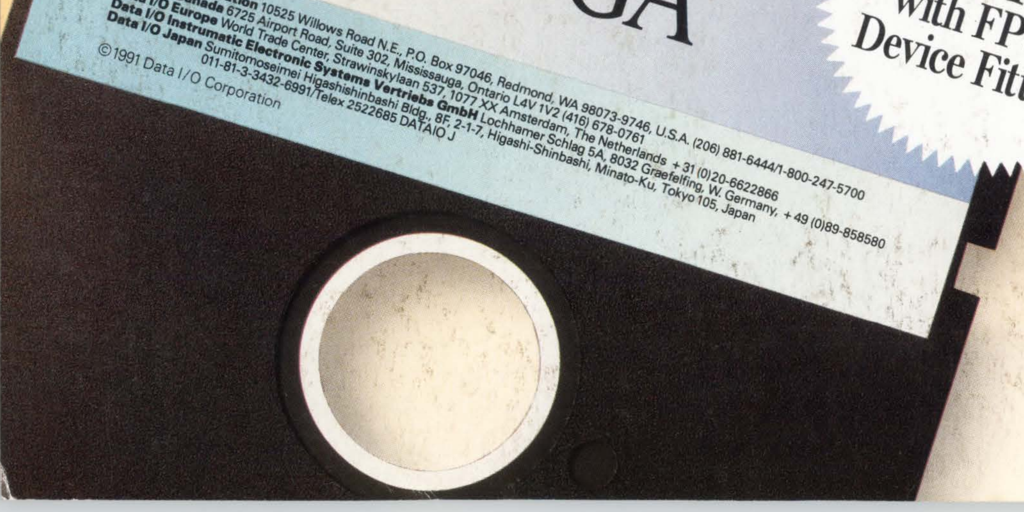

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