INTERNATIONAL EDITION

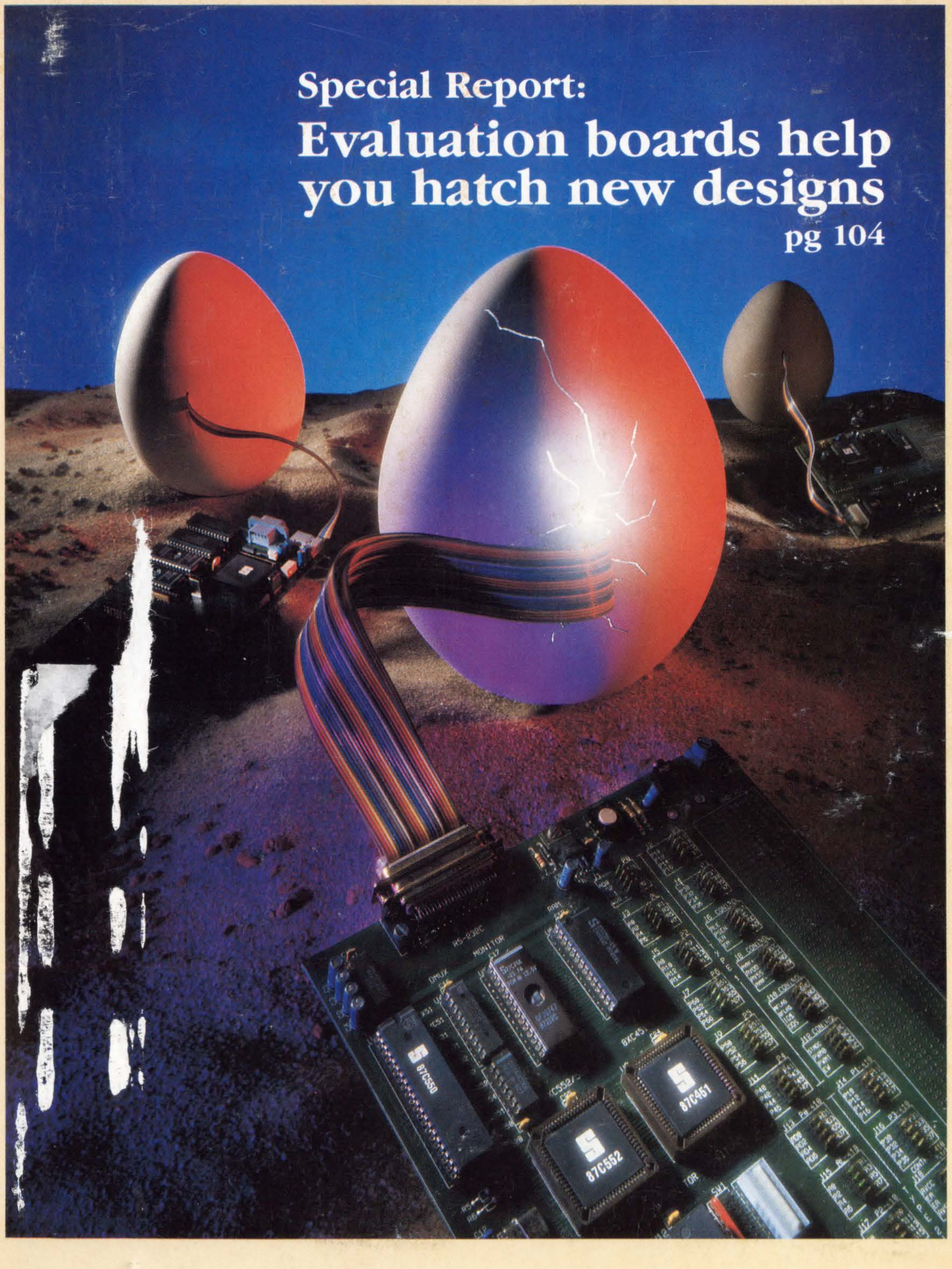
EDN®

PROCESSOR UPDATE PG 93

A CAHNERS PUBLICATION
January 20, 1992

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

Special Report:
Evaluation boards help you hatch new designs
pg 104



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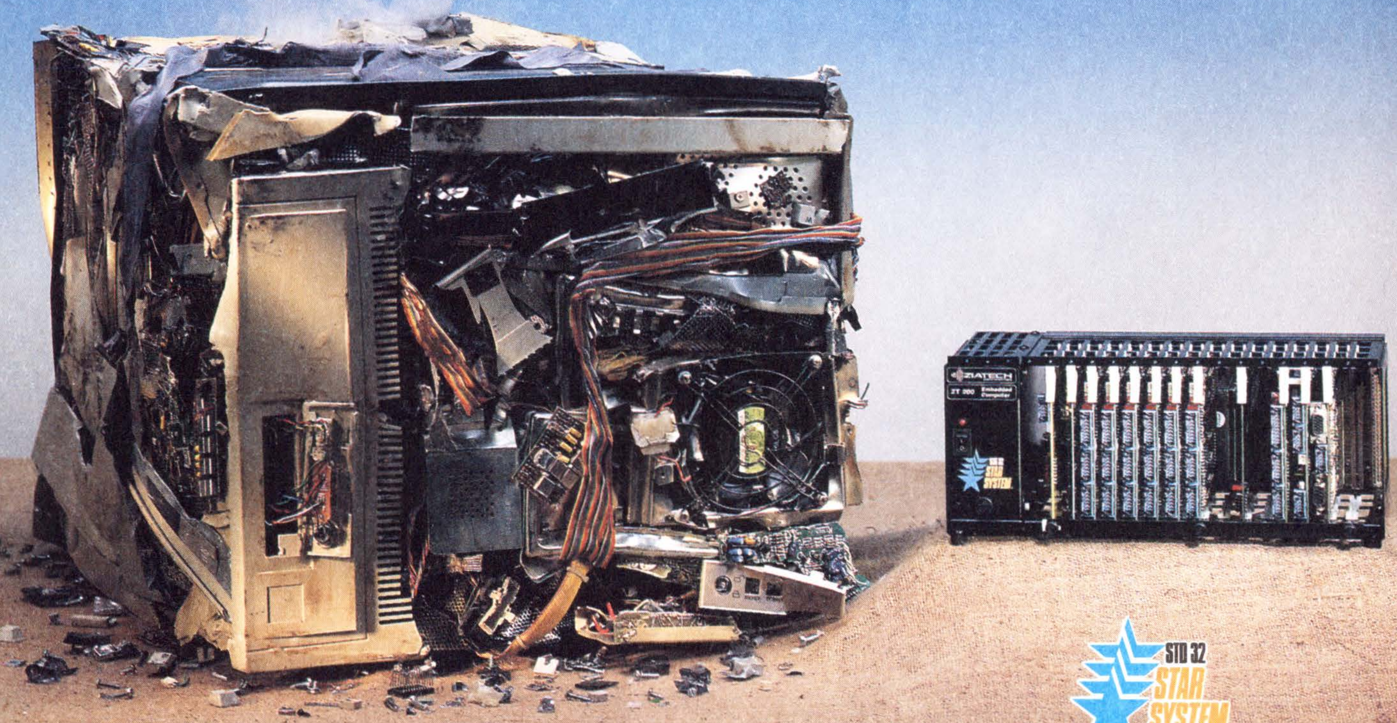

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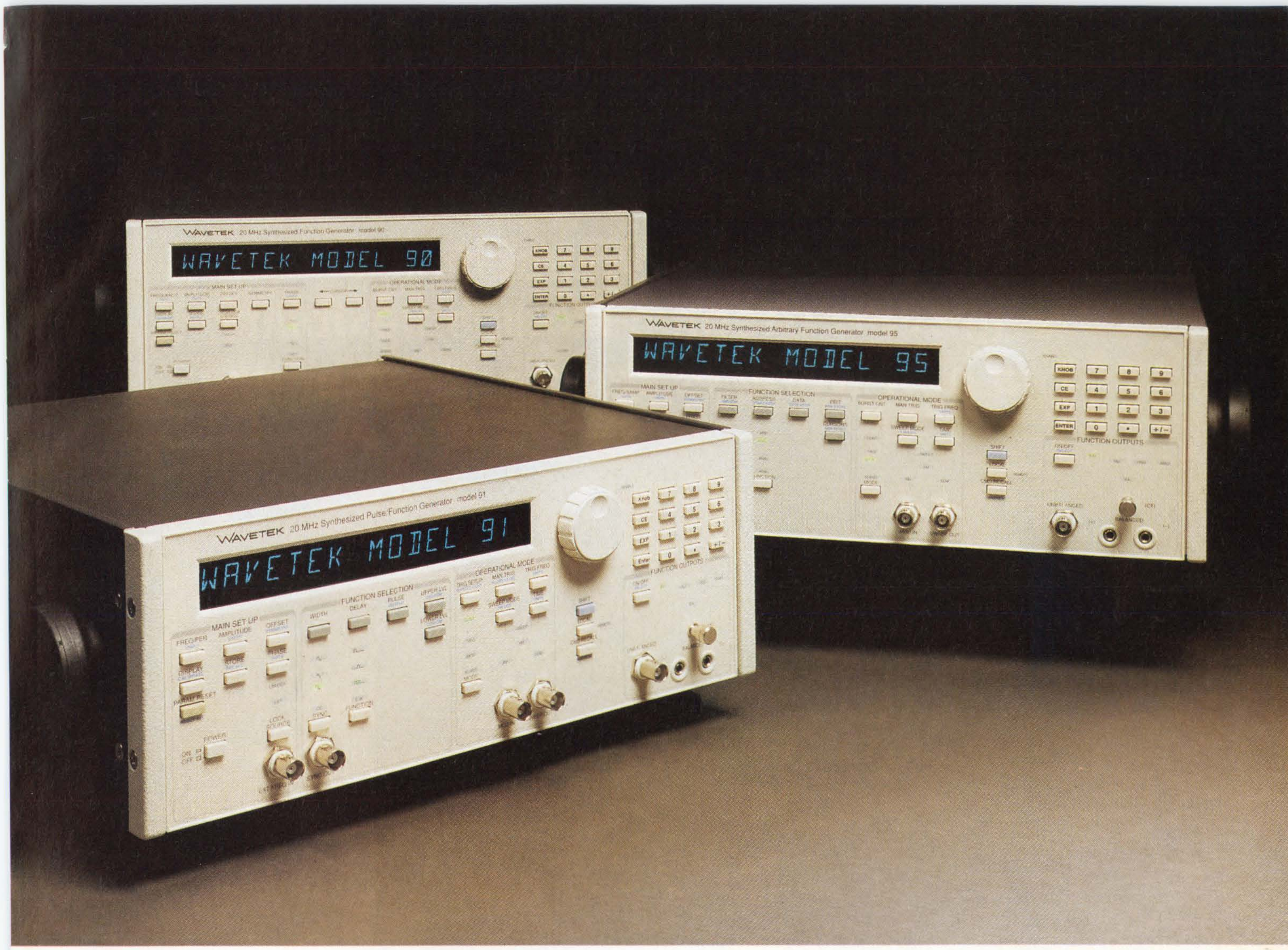

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CIRCLE NO. 5

EDN®
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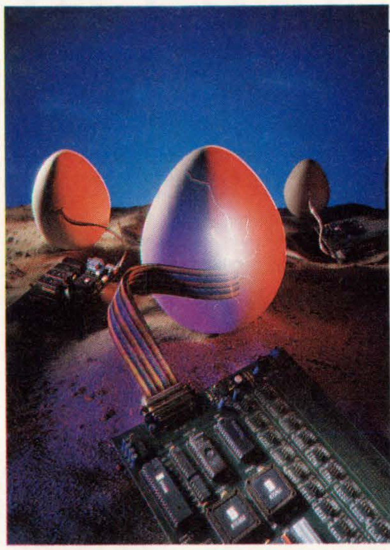
ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE



On the cover: Evaluation boards give you the luxury of experimenting with different 8-bit microcontrollers before cutting the cord on your old standby. Photo courtesy Signetics, Philips Semiconductors; photographer, Geoffrey Nelson; art director, Ottip Ramos. . . . . **PAGE 104**

High-resolution systems get a boost from autocalibrating A/D converters . . . . **PAGE 53**

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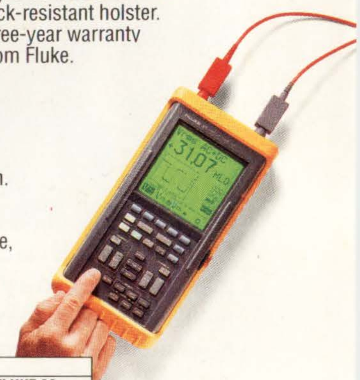

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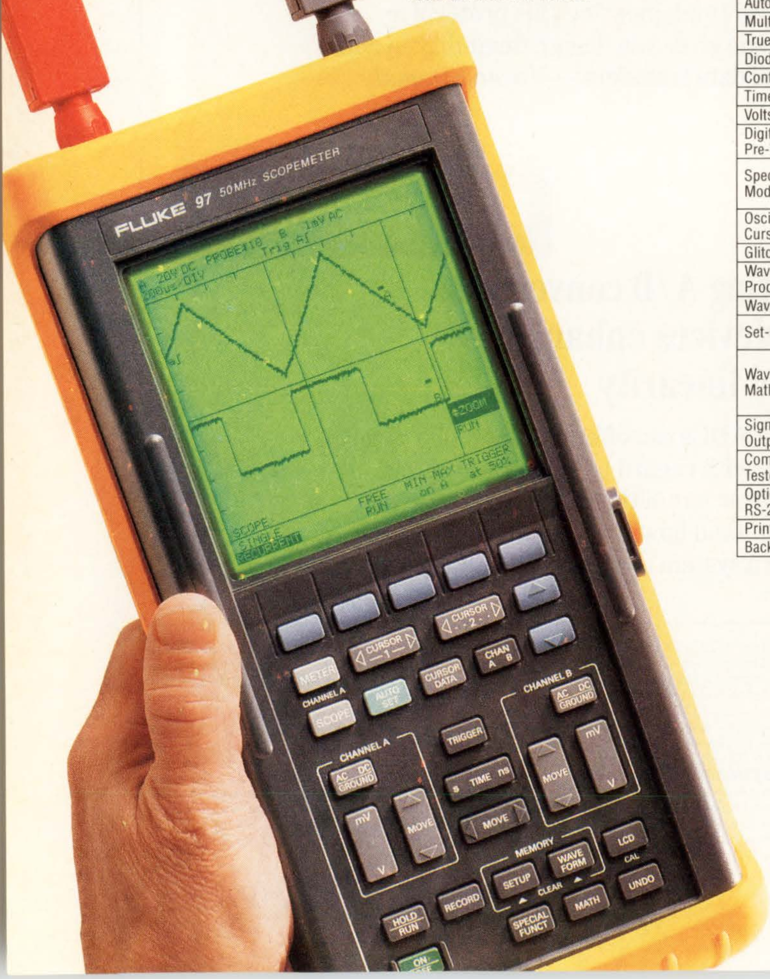

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<tr><th colspan="4">FLUKE 90 SERIES SCOPEMETER SELECTION GUIDE</th></tr>
<tr><th></th><th>FLUKE 97</th><th>FLUKE 95</th><th>FLUKE 93</th></tr>
<tr><td>Suggested List Price</td><td>$1795</td><td>$1495</td><td>$1195</td></tr>
<tr><td>Bandwidth</td><td colspan="3">50 MHz Dual Channel</td></tr>
<tr><td>Sample Rate</td><td colspan="3">25 Megasamples/second</td></tr>
<tr><td>Autoset</td><td colspan="3">Automatically sets Voltage, Time and Trigger</td></tr>
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<tr><td>True RMS Volts</td><td colspan="3">AC or AC+DC up to 600V (1700V Pk–Pk)</td></tr>
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<tr><td>Continuity Beeper</td><td colspan="3">Yes</td></tr>
<tr><td>Time/Division</td><td colspan="3">10 ns/div to 60 sec/div</td></tr>
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<tr><td>Backlit Display</td><td>Electroluminescent</td><td></td><td></td></tr>
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CIRCLE NO. 6

EDN
MAGAZINE EDITION

JANUARY 20, 1992

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In our new Hands On! section, EDN's editors review books, software, music, and more.. **PAGE 189**

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EDITORS' CHOICE

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PROCESSOR UPDATES

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JANUARY 20, 1992

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DESIGN IDEAS

EDITORIAL

NEW PRODUCTS

DEPARTMENTS

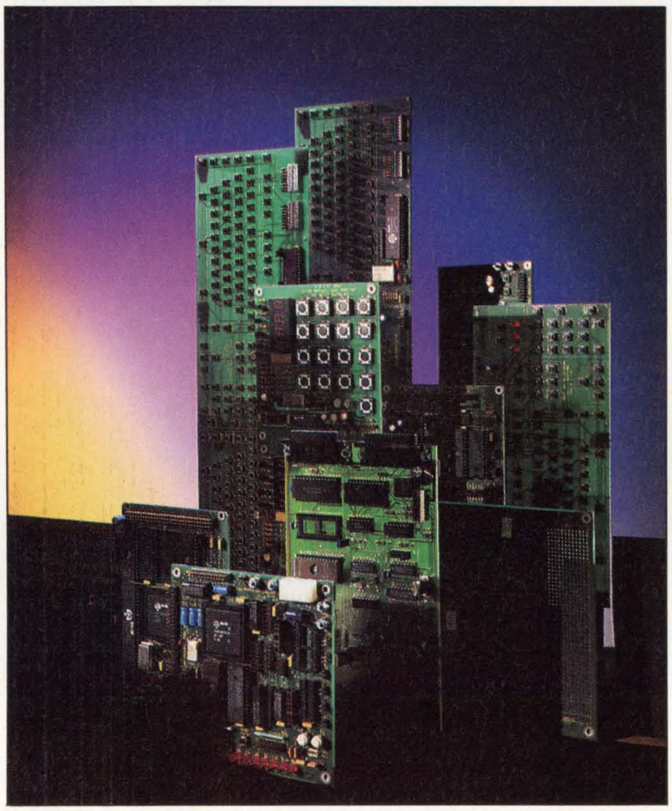
NEW

A summary and analysis of articles in this issue

Welcome to the enhanced EDN. By now, you've probably noticed that we've made some changes to the magazine, starting with the cover. We've spent the last three years talking to you, our readers, to find out how we could better serve your needs. The enhancements we've made to EDN's magazine and news editions represent the fruits of that research.

All of the changes you see are enhancements. In other words, we didn't omit any of the parts of EDN magazine you already enjoy. We'll continue to cover the critical topics of the electronics industry, and we're continuing our in-depth coverage of products and technology. The enhancements are designed to make it easier for you to read EDN and to provide you with even more of the information you need to do your work.

For example, the cover of EDN's magazine edition now carries much more information about the articles inside to help you find the stories that interest you. You'll find that the article titles are consistent from the cover, to the table of contents, and on to the article itself. You'll also see colored title bars at the top of each editorial page to help you keep track of where you are in the magazine. We think the consistent title treatment and the title bars will eliminate any problems you may have had finding articles in EDN.



This issue's Special Report covers 8-bit μC evaluation boards.

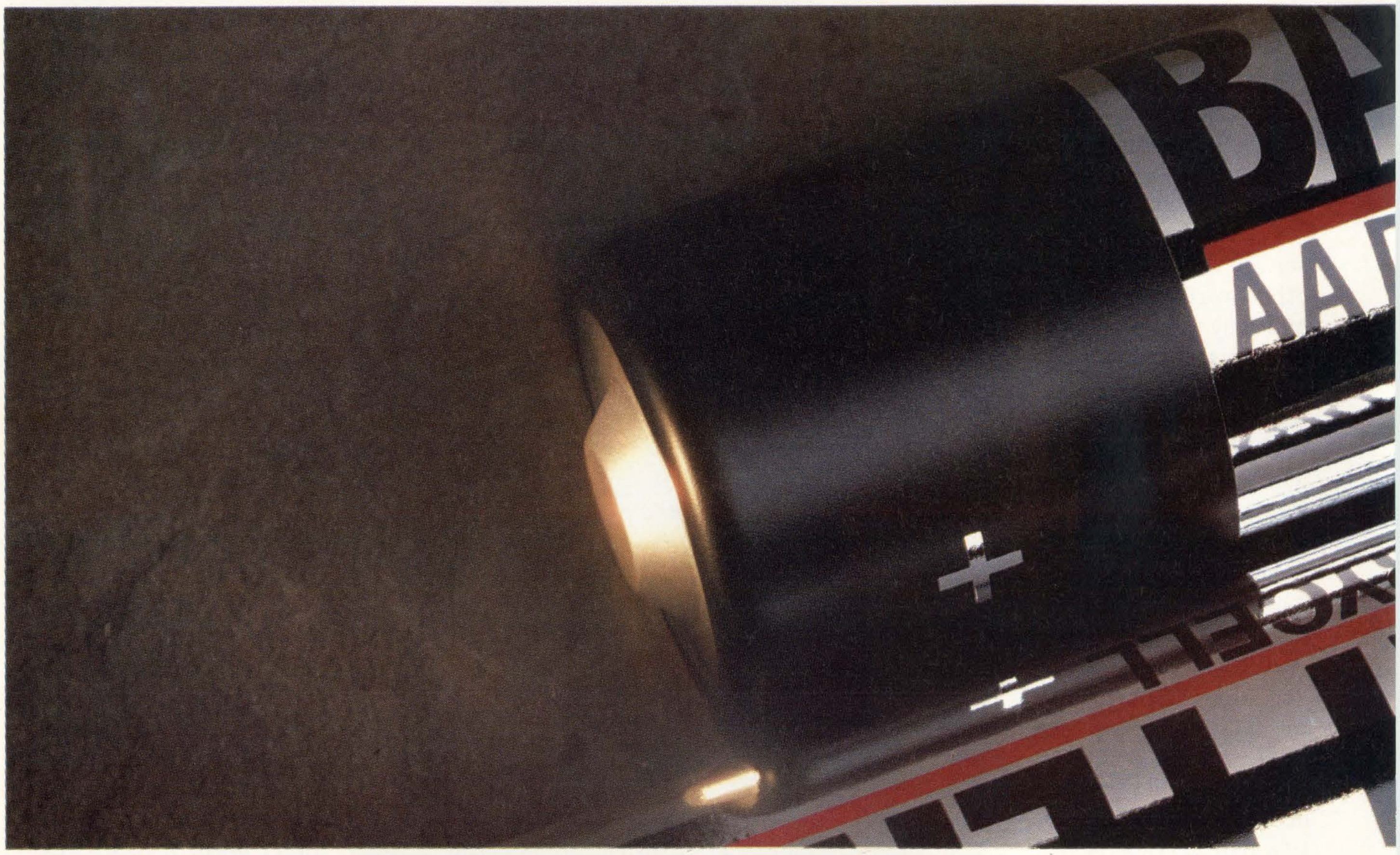
However, the enhancements to EDN go far beyond these cosmetic changes. We've reorganized the News Breaks and short products sections so that we can provide you with even more of the information you want. We've also added several new sections we think you'll like. Because EDN has always been the industry leader in μP coverage, we're introducing a Processor Update section, starting with this issue. In this section, we plan to introduce every new μP, μC, and all related development tools. We're starting this section with a bang. You'll find five Processor Updates in this issue.

In the back of the magazine, you'll find our new "Hands On!" review section. EDN has undertaken several hands-on projects over the years, and we are committed to giving you as much first-hand exposure to new products as we can. Our editors, who are also engineers, will use this section to give you personal advice about products they've tried. Further, we thought we'd have some fun with this section, so you'll find reviews of engineering-related recreational products mixed in with the reviews of software and development products.

The section you're reading right now, "Inside EDN," is also new. We plan to use this page to give you some added insight into each issue's articles. For example, in this issue's Special Report, Ray Weiss looks at development boards for 8-bit processors. These boards help you quickly evaluate competing processor architectures by giving you ready-made, operational platforms for your test software. You don't need to waste any time designing hardware for processors you ultimately won't use in a final product. Ray says he had a blast trying out all of these evaluation boards and their associated software tools. He tells you about his experiences starting on page 104. Ray continues his narrative in our next issue by looking at boards for 16-bit processors.

Steven H Leibson
Executive Editor

Soon, Eight Ho
Computing Will



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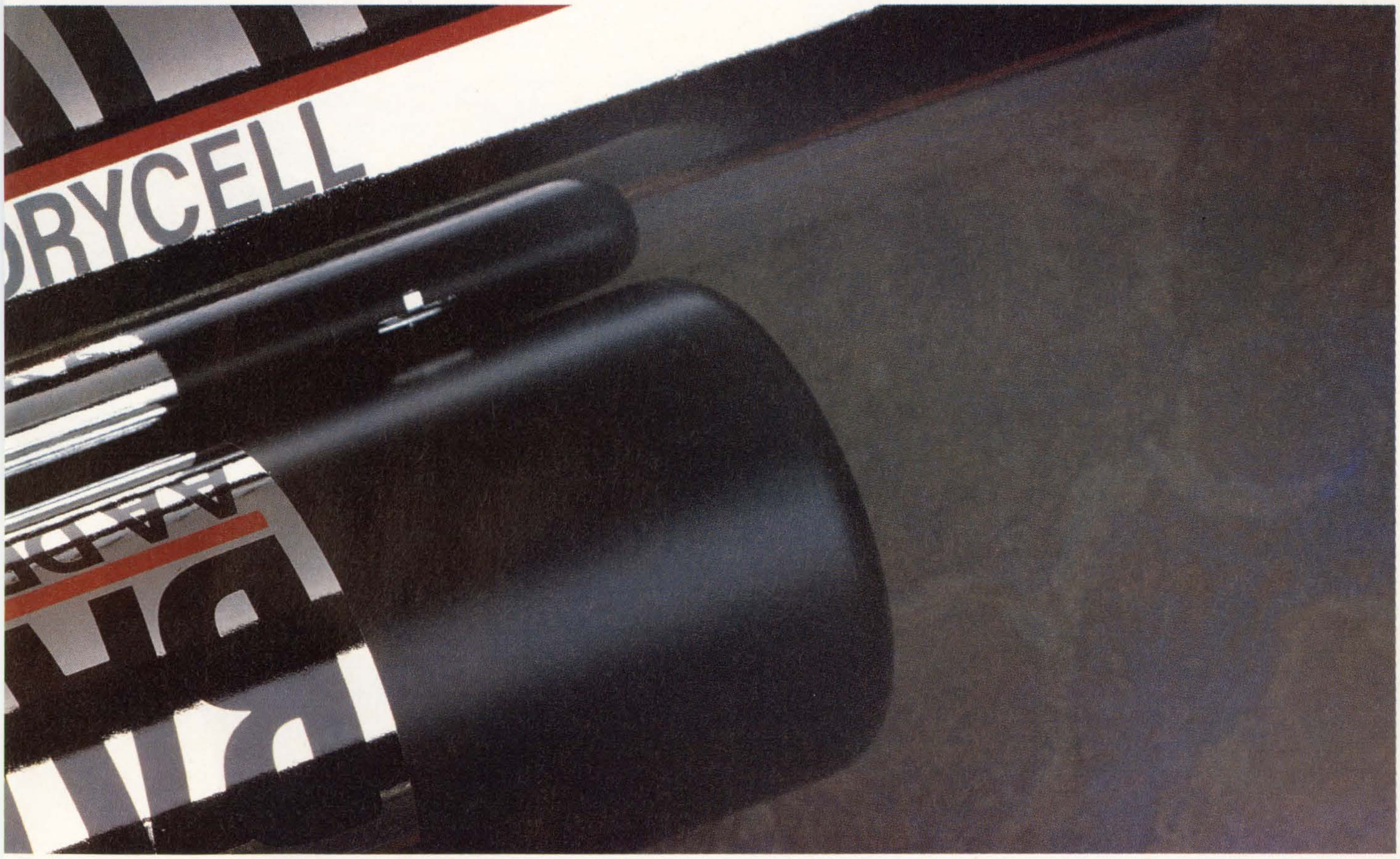

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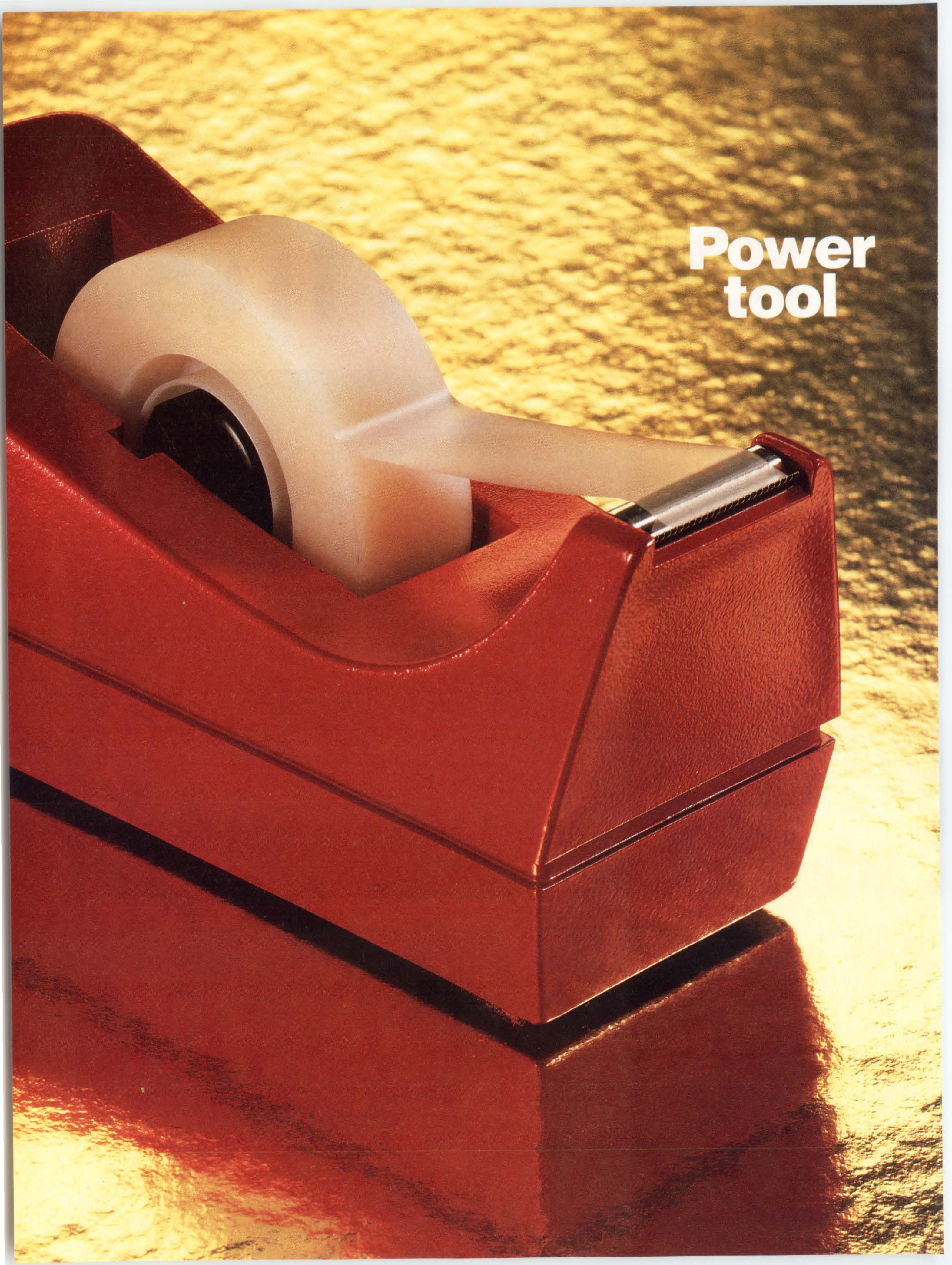
Power tool



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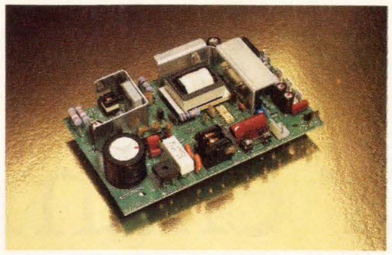

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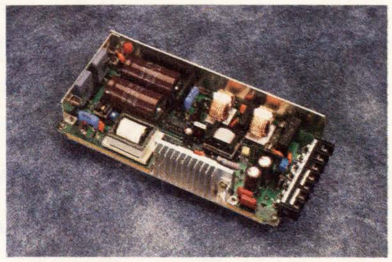
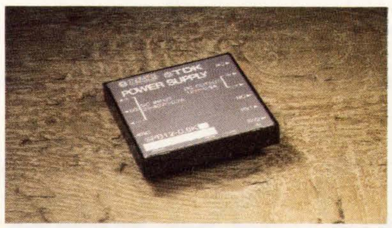


ac to dc power, single output 15W, 25W, 50W, 100W, 150W

- ☐ 5V to 48V output
- ☐ Wide range 85-264V ac input
- ☐ UL/CSA/TÜV certified to international safety standards

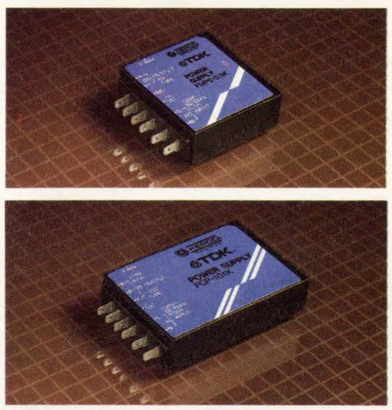
Kepco Group FAW Power Supplies



dc to dc power, single output 5W, 10W, 50W, 100W

- ☐ 5V to 24V output
- ☐ 12-150V dc input
- ☐ UL/CSA

Kepco Group FPD Power Supplies



ac to dc power single output/dual output 3W, 10W

- ☐ 5V to 24V output
- ☐ ±12V, ±15V output
- ☐ 85-132V ac input
- ☐ UL/CSA

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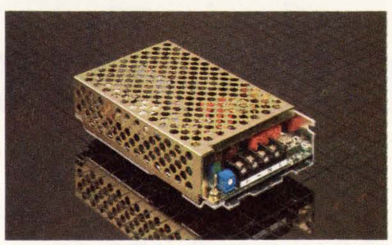
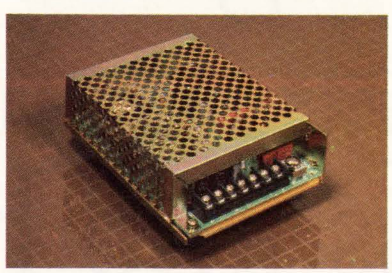


ac to dc power, single output 15W, 25W, 50W

- ☐ 5V to 24V output
- ☐ 85-132V ac input
- ☐ UL/CSA

Kepco Group FAK Power Supplies



ac to dc power, triple outputs 16W

- ☐ +5V, ±12V and ±15V output
- ☐ 85-132V ac input
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to 20,000 usable gates. An
PLD family. Bye-bye mas
dense as it gets. Well, there
old college roommate. 30-
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inch neck, crushed
ou know the type."

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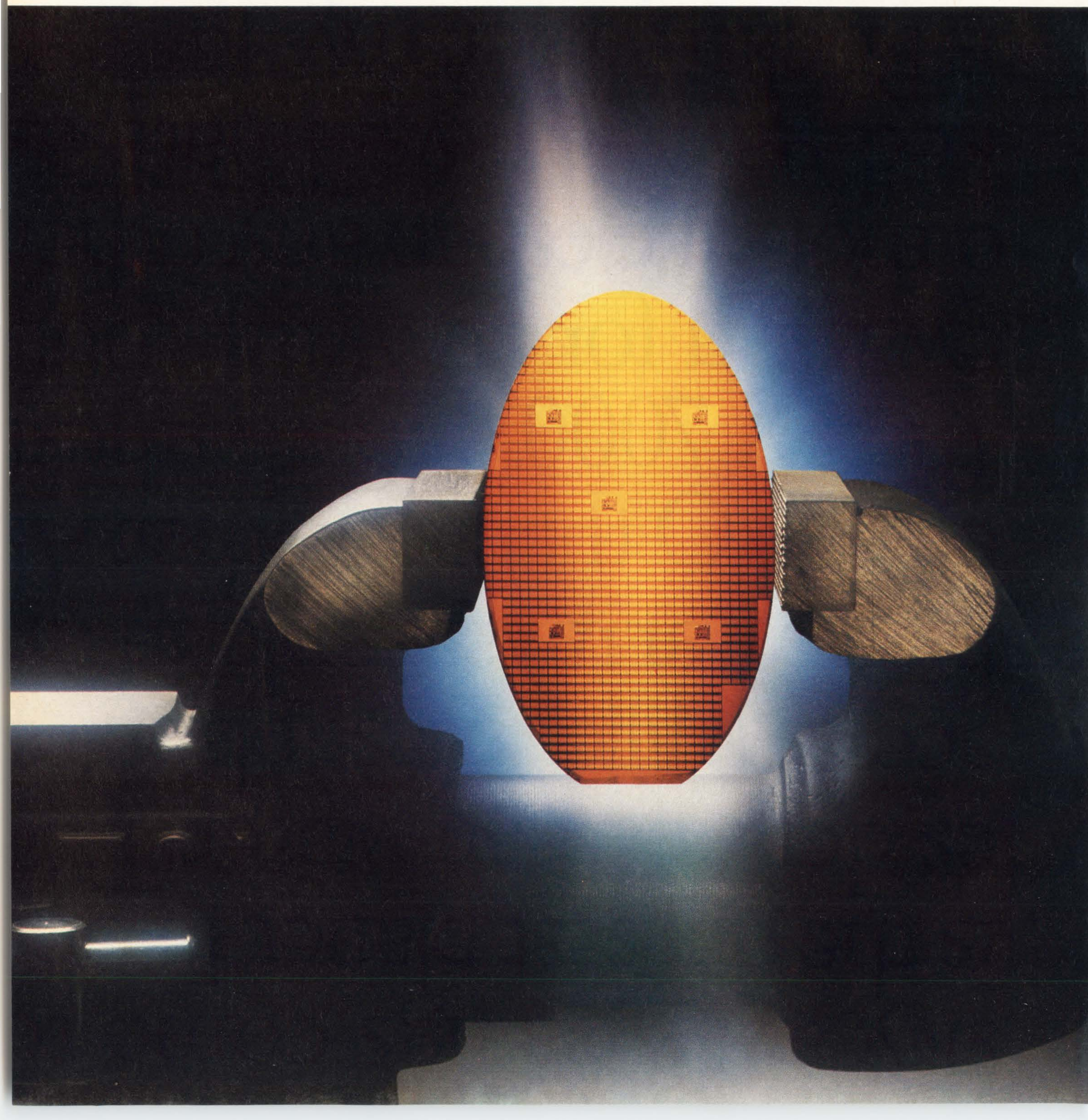
CIRCLE NO. 10

IN THE ERA OF MegaChip™ TECHNOLOGIES

We've squeezed more ABT Widebus as fast



speed from our logic.
as 4.1 ns!

With our new Advanced BiCMOS interface logic (ABT) family, you get the speed, drive and low power you need to optimize the performance of processors operating at 33 MHz and above.

Fabricated in our 0.8-micron BiCMOS process, this new family delivers maximum speeds down to 4.1 ns over recommended operating conditions. Typical performance of the devices is in the 2.5- to 3.0-ns range.

Other critical performance parameters are as impressive. Drive capability is 32 to 64 mA. Static power consumption is typically 2 mA (I_{CCH}, I_{CCZ}) and 30 mA (I_{CCL}). Ground bounce is less than 800 mV typ.

All this in Widebus

Our ABT family, a second-generation advance of our leadership BiCMOS (BCT) family, includes versions of our 16-, 18- and 20-bit-width Widebus™ functions.

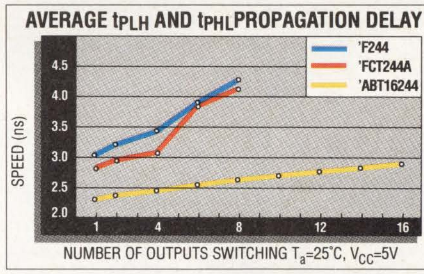
Among the many ABT Widebus functions released is the 'ABT16244, a 16-bit buffer and line driver. It exhibits much greater stability of propagation delay *(see chart)*, which results in a lower derating factor across the number of outputs switched.

Also in volume production are the Widebus 'ABT16245 16-bit bidirectional bus transceiver and the 'ABT16543 and 'ABT16952 16-bit bidirectional registered bus transceivers.

As in our successful Advanced CMOS Logic (ACL) Widebus family, these devices come in our leadership surface-mount shrink small-outline package (SSOP) that gives you twice the number of I/Os as a standard small-outline package in the same space.

Unique additions included

There are also new devices in our ABT Widebus family featuring greater density and functionality. Our 'ABT16500A is a good example. An 18-bit registered transceiver, it combines D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes.



TI's speed advantage: *In a one-to-one comparison, a TI 'ABT16244 16-bit Advanced BiCMOS driver proves to be much faster and more stable than Advanced Bipolar and standard CMOS octal drivers.*

To complement our full line of Widebus products, our ABT family will include at least 39 octal buffers/drivers, flip-flops, transceivers and registered transceivers.

Squeeze more out of your system with a free sample 'ABT16500A: Call 1-800-336-5236, ext. 3009

To learn firsthand how our new ABT family can boost the performance of your bus-interface designs, get a free 'ABT16500A transceiver and data sheet. Just complete and mail the return card or call the number above.

TEXAS INSTRUMENTS

08-1139

2-state op amp sleeps or wakes up on demand

Increasing numbers of low-power applications benefit from component features such as shutdown pins and sleep-mode states. Each independent amplifier in Motorola's dual MC33102 op amp takes these features one step further by requiring no additional external components or device pins. The op amps don't require any active shutdown command. Instead, they operate in a sleep mode that consumes just enough power to detect incoming signals and automatically shift to a higher performance mode when the load's current exceeds a certain threshold. The company is applying this sleep-mode concept to other ICs for low-power applications. In sleep mode, the amplifier is active and waiting for an input signal.

In this state, each op amp operates with a current drain of 45 μA per amplifier and features a slew rate of 0.16V/μsec, gain bandwidth of 0.33 MHz, and output current of 0.15 mA. If an input signal causes either amplifier's output to source or sink 160 μA (when operating from ±15V supplies), that amplifier automatically switches to the awake mode. In this mode, the amplifiers exhibit a slew rate, gain bandwidth, and output drive of 1.7V/μsec, 4.6 MHz, and 50 mA, respectively. Current drain in this higher-performance state is typically 750 μA. The amplifiers automatically return to sleep mode when output current drops below 142 μA. A delay circuit contains a capacitor with a 1-sec discharge time that prevents unwanted returns to the sleep mode. Applying this device requires some care because the output's switching threshold voltage will depend on the load resistance. Samples of the $1.60 (10,000) device are available for commercial applications in both 8-pin plastic DIPs and SOICs. The specifications hold over −40 to +85°C. Quantity delivery is from stock to 6 weeks. Motorola Inc, Tempe, AZ, (602) 897-3615, FAX (602) 897-4193.—Anne Watson Swager

SRAM-based FPGAs run at 50 MHz

Concurrent Logic's static-RAM-based FPGAs (field-programmable gate arrays) are capable of clocking counters at rates as high as 70 MHz. The CLi6000 family has equivalent gate densities ranging from 1200 to 10,000 gates with 64 to 160 I/Os. The FPGAs use internal RAM to program routing connections. The architecture is like a

Text continued on pg 24

Silicon microvalve has proportional flow control

IC Sensors has produced an electrically activated, normally closed valve on a silicon chip using micromachining techniques. The valve has a silicon diaphragm with diffused-in heating resistors. The diaphragm is part of a bimetallic structure that moves when heated. By controlling the power dissipated in the resistors you can control gas flow over the range of 0 to 150 cc/minute at pressures as high as 50 psi. IC Sensors, Milpitas, CA, (408) 432-1800, FAX (408) 432-7322.
—Richard A Quinnell

Transistor demonstrates 20-GHz peak f_T

At the International Electron Devices Meeting in Washington, DC last month, IBM researchers described a silicon-on-insulator (SOI), lateral-bipolar transistor with a maximum switching speed of 20 GHz. Unlike most previous lateral-bipolar devices, which have a wide base region or high base resistance, the IBM device features a narrow base and emitter. As a result, the transistor offers minimal resistance—emitter resistance is 8Ω—and junction capacitances are less than 33 fF.

Although commercial applications are several years off, the transistor offers promise in areas such as high-speed, low-power applications. In addition, because SOI protects circuits from Cosmic-radiation-induced soft-errors, the transistor offers pro-mise in space and hostile environment applications. IBM Research Div, Yorktown Heights, NY, (914) 945-2885
—Michael C Markowitz

Logic family includes boundary scan

National Semiconductor introduced a family of logic devices that incorporates the IEEE 1149.1 (JTAG) boundary scan test circuits. The Scan18xxx series' initial issue has five parts, four 18-bit transceivers, and a serial-to-parallel test access-port converter.

The devices are based on National's Fact-QS CMOS technology and offer TTL-like output swings and drive. They come in both DIP and surface-mount packages. Samples are available now; production is scheduled for the second quarter. Logic devices cost $5.75 (100); the converter costs $9.95. National Semiconductor, Santa Clara, CA, (408) 721-5000.
—Richard A Quinnell

Continued from pg 23

gate array in that it comprises a large matrix of small, fine-grain, logic cells. A 10,000-gate equivalent part will have 64,000 logic cells. These cells consist of a multiplexer, bus logic, and a flip-flop. The FPGAs have a matrix of 8 × 8 elements with special block routing resources. The FPGA has global routing resources for signals and clocks. These resources link into the blocks via signal repeaters. Chip clock skew is held to less than 1 nsec across a chip. Gate delays are on the order of 2.1 nsec, with 2- and 0-nsec setup and holds.

These FPGAs suit register-intensive designs: They have 576 to 64,000 logic cells, each with one flip-flop. Toggle rates are as high as 150 MHz, and the FPGAs can run sequential logic at 50 MHz. The family has a set of design tools, including schematic capture, synthesis, schematic regeneration, automatic place and route, and post-layout timing and functional verification. These tools run on the View-logic tool set and include the Viewlogic schematic capture and simulator. The 5000-equivalent-gate CLi6005 is avail-able now and costs $108 in volume. The CLi6002 and CLi6003 are available in sample quantity from $58. Concurrent Logic Inc, Sunnyvale, CA, (408) 522-8700, FAX (408) 732-2765.—Ray Weiss

Flat-panel VGA controller offers interface choices

The 65520 flat-panel VGA controller from Chips and Technologies gives you a range of interface choices. The device has separate I/O ports for ISA, Micro Channel Architecture, or 386SL peripheral interface buses. It will work with two or four memory devices and either volatile or dynamic RAM, which lets you choose between cost and performance. The device handles LCD, electroluminescent, and plasma flat panels, and drives flat-panel and CRT displays simultaneously. It supports 1024 × 768-pixel resolution on both displays with 16 colors on the CRT. At 640 × 480 resolution, the device provides 64 gray levels on flat panels and 256 colors on CRTs.

The controller offers backward compatibility with all older graphics standards. It uses horizontal compensation to center lower-resolution images on the panel and vertical compensation to expand low-resolution images to fill a 480-line display. The vertical compensation methods include centering, line replication, and blank-line insertion. The $45 (1000) controller is available in sample quantities now and will be in production in April. Chips and Technologies Inc, San Jose, CA, (408) 434-0600.—Richard A Quinnell

Chip set handles serial link at 1.25 Gbit/sec

The GaAs Taxi chip set lets you replace a parallel data link with a high-speed serial link over coaxial cable or optical fibers. The 4-chip set, based on AMD's Taxi chip set, includes a multiplexer, a demultiplexer, a transmitter, and a receiver. The devices work in teams to convert a 32- or 40-bit parallel-data bus into a 1.25 Gbit/sec serial link. The transmitter's output signal will drive a coaxial cable directly, or drive a fiber-optic transmitter. The bus interface devices have TTL-compatible interfaces, but require both 5 and 2V supplies. The set costs $995 in sample quantities and $603 (1000). Sets are available now, as are development boards. Vitesse Semiconductor,Camarillo, CA, (805) 388-3700, FAX (805) 987-5896. —Richard A Quinnell

Making math work for you

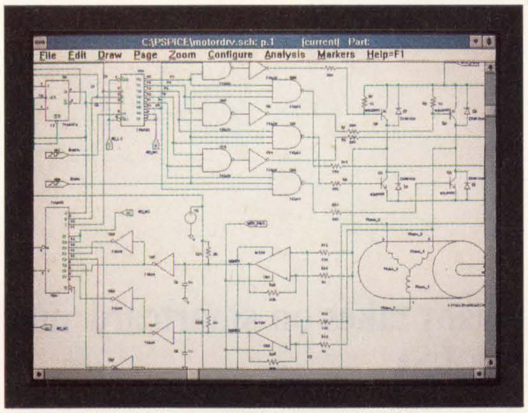
Mastering the algebra for an analysis derivation is a vexing problem for some engineers. To master the math, you can attend a 3-day, $995 course taught by Dr R D Middlebrook of the California Institute of Technology. The course, Structured Analog Design, teaches how to get design value out of the formal methods you already know—and with much less work. The insights gained will help you to obtain maximum benefit from CAD programs. The course is offered February 19 to 21 in Santa Clara, CA, and September 9 to 11 in Boston, MA. Part 2, a workshop in the techniques covered in part 1 plus additional material is offered March 4 to 6 in Los Angeles, CA, and September 14 to 16 in Boston, MA. Ardem Associates, (714) 592-0317, FAX (714) 592-0698. —Susan Rose

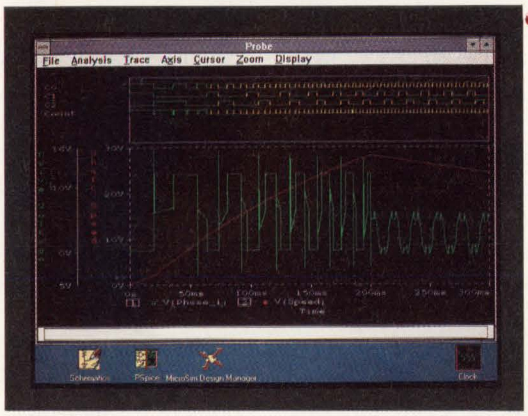
Technique provides fast Spice analysis

The AWE (Asymptotic Waveform Evaluation) technique provides Spice-like accuracy with simulations that are orders-of-magnitude faster. Professors Lawrence Pilage of the University of Texas (Austin, TX) and Ronald R Roher of Carnegie Mellon University (Pittsburgh, PA) developed the technique. The technique uses a frequency-domain analysis based on an RLC interconnect model to approximate circuit performance.

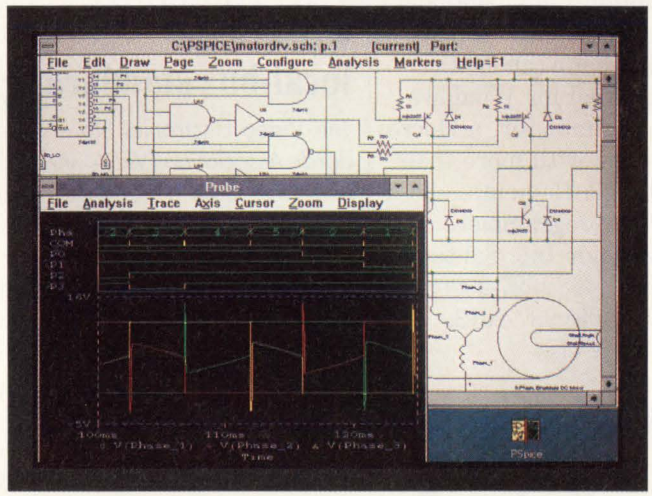
Currently, Quicklogic Corp's upgraded pASIC FPGA (field programma-

Text continued on pg 26





Where would you go to answer all of your analog and digital circuit design questions?



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CIRCLE NO. 12

Text continued from pg 24

ble gate array) design kit uses the analysis technique for fast Spice simulation. Results are within 10% of a Spice simulation's results. The $3995 tool kit's logic synthesizer creates FPGA circuits from VHDL (VHSIC Hardware Description Language) and Boolean equation forms. It also has a schematic entry tool for Windows 3.0, a simulator, a Macro Library with more than 200 logic elements, and a device programmer. Quicklogic Inc, Santa Clara, (408) 987-2000, FAX (408) 987-2012.
—Ray Weiss

Light sensor connects directly to μPs

A single TSL220 light-to-frequency converter reduces the number of external components necessary to detect and measure minute changes in light intensity. Because the device itself comprises a large-area photodiode and a patented BiMOS current-to-frequency converter, it replaces a discrete photodiode, amplifier, and A/D converter. You can directly connect the sensor to a μP or a digital-control circuit. The device features a dynamic range of 118 dB and a linearity of 2% over the full-scale range and can detect intensity changes of 0.01% over the full-scale range. The $4.61 (1000) device comes in a clear plastic 8-pin DIP. Texas Instruments Inc, Semiconductor Group, Dallas, TX, (800) 336-5236, ext 700, (214) 995-6611, ext 700.
—Anne Watson Swager

VESA committee will create local-bus standard

The Video Electronics Standards Association (VESA) intends to create a standard for a graphics local bus. A technical committee will define a bus for graphics peripherals that connects directly to the host's CPU via a 32-bit data bus. The standard will ensure compatibility between third-party peripherals for high-performance graphics. The Local Bus Committee includes Appian Technology, Binar Graphics, Chips and Technology, Cirrus Logic, Desktop Electronics, Everex Systems, Headland Technology, Integrated Information Technologies, Micronics Computer, Media Vision, National Semiconductor, Orchid Technology, Panacea, Tseng Labs, and Weitek. The committee chairman is Ron McCabe, Graphics Product Manager at Everex Systems. The committee plans to submit a proposal to the VESA general membership at VESA's August, 1992, General Meeting. VESA, San Jose, CA, (408) 435-0333, FAX (408) 435-8225.
—John Gallant.

Company takes on smartcard market in the USA

SGS Thomson has expanded its ST16XYZ family of smartcards with two microcontrollers for applications requiring effective data security. The ST16623 and ST16301 have 8-bit CPUs with 6 and 3 kbytes of ROM, 224 and 128 bytes of RAM, and 3 and 1 kbytes of EEPROM, respectively, on board. These memory capacities are combined with built-in hardware and software security features. A non-maskable security interrupt that is generated whenever an unauthorized access is attempted lets the devices restrict data accesses across the RAM/ROM/EEPROM area. Other features include compliance with ISO standards, 5-MHz operation, 100,000 write/erase cycles, and a 10-year data retention. The devices come in die or micromodule form. In micromodule form, the chips cost $2.78 and $3.28 (5000), respectively.

The company has been active in smartcard development for more than 10 years. The recent formation of the Smartcard Products Business Unit marks an effort to take more control of smartcard applications in the US. SGS Thomson Microelectronics, Carrollton, TX, (214) 466-7210.
—Susan Rose

Synthesize waveforms at 2 nsec/point

The Flexstar 7000 can step through waveforms at 2 nsec per point, letting you generate high-speed waveforms. You program the first half of the waveform with as many as 128 data points, and the instrument generates a mirror image of the second half automatically. You can also disable the second half of the waveform. The instrument lets you create arbitrary waveform patterns (waveform present or no waveform) to one-million waveforms long. The $20,000 instrument generates waveforms by consecutively summing the outputs of 128 DACs. Resolution for each DAC is 8 bits plus sign, and the overall resolution is approximately 12 bits for a full-scale waveform. Because the instrument creates the waveform using a summing method, it automatically generates the overlapping waveform effects of pulse crowding when you make the period shorter than the pulse length. Flexstar, San Jose, CA, (408) 433-0770, FAX (408) 433-1766.—Doug Conner

PROFILES IN PARTNERING

Raytheon and Dale®

PRODUCTS: Metal film and wirewound resistors.

OBJECTIVE: Develop efficient systems for supplying and procuring MIL-style components.

UNITS INVOLVED: Raytheon and Dale Electronics, Inc.

For more than two decades, Raytheon and Dale® have developed a strong manufacturer/vendor relationship focused on close communication and a common goal to continually improve quality.

Today, Dale works closely with other Vishay companies (including Angstrohm and Ultronix) in supplying established reliability resistors used in the *Patriot, Sparrow* and other programs of the Raytheon Missile Division. Military specifications involved include: MIL-R-39005, MIL-R-39007, MIL-R-39009, MIL-R-39017, MIL-R-55182, MIL-R-55342 and MIL-R-83401.

In helping Raytheon meet the exacting requirements of these programs, Dale, in 1984, became the first OEM vendor to Raytheon to install an on-line computer terminal, allowing direct-order capability with several Dale plants.

Since then, this system has been tailored to allow Raytheon purchasing locations to obtain a wide range of information on orders to Dale including everything from price, to production status, to a shipping date.

A COMPANY OF VISHAY

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"In essence," a Dale spokesperson commented, "Raytheon can access anything we can in relation to any or all of their orders. More recently, Dale helped Raytheon pioneer their first system for electronic data interchange (EDI)."

Quality, also, has played a big part in the relationship. With a history of tens of millions of parts shipped to Raytheon, Dale has maintained exceptionally high quality levels. This is why Raytheon has chosen Dale for several quality and service awards over the last few years.

For more information on how Dale's commitment to effective partnering can benefit your operation, please contact Joe Matejka, Vice President, Quality Assurance, Dale Electronics, Inc., 1122 23rd Street, Columbus, Nebraska 68601-3647. Phone 402-563-6511. Fax 402-563-6418.

CIRCLE NO. 13

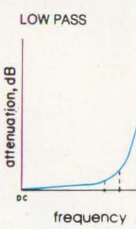
FILTERS

dc to 3GHz from $11.45

lowpass, highpass, bandpass

• less than 1dB insertion loss • greater than 40dB stopband rejection • surface-mount • BNC, Type N, SMA available • 5-section, 30dB/octave rolloff • VSWR less than 1.7 (typ) • rugged hermetically-sealed pin models • constant phase • meets MIL-STD-202 tests • over 100 off-the-shelf models • immediate delivery

low pass, Plug-in, dc to 1200MHz



Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB	Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB
PLP-5	DC-5	8-10	10-200	PLP-250	DC-225	320-400	400-1200
PLP-10.7	DC-11	19-24	24-200	PLP-300	DC-270	410-550	550-1200
PLP-21.4	DC-22	32-41	41-200	PLP-450	DC-400	580-750	750-1800
PLP-30	DC-32	47-61	61-200	PLP-550	DC-520	750-920	920-2000
PLP-50	DC-48	70-90	90-200	PLP-600	DC-680	840-1120	1120-2000
PLP-70	DC-60	90-117	117-300	PLP-750	DC-700	1000-1300	1300-2000
PLP-90	DC-81	121-137	167-400	PLP-800	DC-720	1080-1400	1400-2000
PLP-100	DC-98	146-189	189-400	PLP-850	DC-760	1100-1400	1400-2000
PLP-150	DC-140	210-300	300-600	PLP-1000	DC-900	1340-1750	1750-2000
PLP-200	DC-190	290-390	390-800	PLP-1200	DC-1000	1620-2100	2100-2500

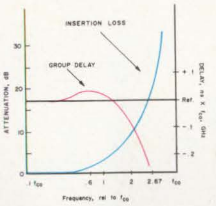
Price, (1-9 qty), all models: plug-in $14.95, BNC $32.95, SMA $34.95. Type N $35.95

Surface-mount, dc to 570MHz

SCLF-21.4	DC-22	32-41	41-200	SCLF-190	DC-190	290-390	390-800
SCLF-30	DC-30	47-61	61-200	SCLF-380	DC-380	580-750	750-1800
SCLF-45	DC-45	70-90	90-200	SCLF-420	DC-420	750-920	920-2000
SCLF-135	DC-135	210-300	300-600				

Price, (1-9 qty), all models: $11.45

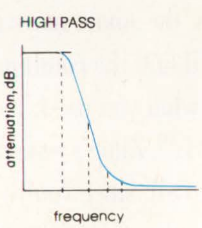
Flat Time Delay, dc to 1870MHz



Model No.	Passband MHz loss < 1.2dB	Stopband MHz loss > 10dB	Stopband MHz loss > 20dB	VSWR Freq. Range, DC thru 0.2fco X̄	VSWR Freq. Range, DC thru 0.6fco X̄	Group Delay Variations, ns Freq. Range, DC thru fco X̄	Group Delay Variations, ns 2fco X̄	Group Delay Variations, ns 2.67fco X̄
PBLP-39	DC-23	78-117	117	1.3:1	2.3:1	0.7	4.0	5.0
PBLP-117	DC-65	234-312	312	1.3:1	2.4:1	0.35	1.4	1.9
PBLP-156	DC-94	312-416	416	0.3:1	1.1:1	0.3	1.1	1.5
PBLP-200	DC-120	400-534	534	1.6:1	1.9:1	0.4	1.3	1.6
PBLP-300	DC-180	600-801	801	1.25:1	2.2:1	0.2	0.6	0.8
PBLP-467	DC-280	934-1246	1246	1.25:1	2.2:1	0.15	0.4	0.55
▲BLP-933	DC-560	1866-2490	2490	1.3:1	2.2:1	0.09	0.2	0.28
▲BLP-1870	DC-850	3740-6000	5000	1.45:1	2.9:1	0.05	0.1	0.15

Price, (1-9 qty), all models: plug-in $19.95, BNC $36.95, SMA $38.95, Type N $39.95
NOTE: ▲: -933 and -1870 only with connectors, at additional $2 above other connector models.

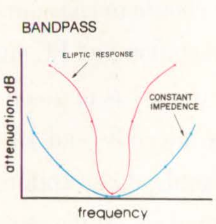
high pass, Plug-in, 27.5 to 2200MHz



Model No.	Stopband MHz loss < 40dB	Stopband MHz loss < 20dB	Passband MHz loss < 1dB	VSWR Pass-band Typ.	Model No.	Stopband MHz loss < 40dB	Stopband MHz loss < 20dB	Passband MHz loss < 1dB	VSWR Pass-band Typ.
PHP-25	DC-13	13-19	27.5-200	1.8:1	PHP-400	DC-210	210-290	395-1600	1.7:1
PHP-50	DC-20	20-26	41-200	1.5:1	PHP-500	DC-280	280-365	500-1600	1.8:1
PHP-100	DC-40	40-55	90-400	1.8:1	PHP-600	DC-350	350-440	600-1600	2.0:1
PHP-150	DC-70	70-95	133-600	1.8:1	PHP-700	DC-400	400-520	700-1800	1.6:1
PHP-175	DC-70	70-105	160-800	1.5:1	PHP-800	DC-445	445-570	780-2000	2.1:1
PHP-200	DC-90	90-116	185-800	1.6:1	PHP-900	DC-520	520-660	910-2100	1.8:1
PHP-250	DC-100	100-150	225-1200	1.3:1	PHP-1000	DC-550	550-720	1000-2200	1.9:1
PHP-300	DC-145	145-170	290-1200	1.7:1					

Price, (1-9 qty), all models: plug-in $14.95, BNC $36.95, SMA $38.95, Type N $39.95

bandpass, Elliptic Response, 10.7 to 70MHz



Model No.	Center Freq. (MHz)	Passband I.L. 1.5 dB Max. (MHz)	3 dB Bandwidth Typ. (MHz)	Stopbands I.L. > 20dB at MHz	Stopbands I.L. > 35dB at MHz
PBP-10.7	10.7	9.6-11.5	8.9-12.7	7.5 & 15	0.6 & 50-1000
PBP-21.4	21.4	19.2-23.6	17.9-25.3	15.5 & 29	3.0 & 80-1000
PBP-30	30.0	27.0-33.0	25-35	22 & 40	3.2 & 99-1000
PBP-60	60.0	55.0-67.0	49.5-70.5	44 & 79	4.6 & 190-1000
PBP-70	70.0	63.0-77.0	68.0-82.0	51 & 94	6.0 & 193-1000

Price, (1-9 qty), all models: plug-in $18.95, BNC $40.95, SMA $42.95, Type N $43.95

Constant Impedance, 21.4 to 70MHz

Model No.	Center Freq. MHz	Passband MHz loss < 1dB	Stopband loss > 20dB at MHz	VSWR 1.3:1 Total Band MHz
PIF-21.4	21.4	18-25	1.3 & 150	DC-220
PIF-30	30	25-35	1.9 & 210	DC-330
PIF-40	42	35-49	2.6 & 300	DC-400
PIF-50	50	41-58	3.1 & 350	DC-440
PIF-60	60	50-70	3.8 & 400	DC-500
PIF-70	70	58-82	4.4 & 490	DC-550

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F132-2 REV. A

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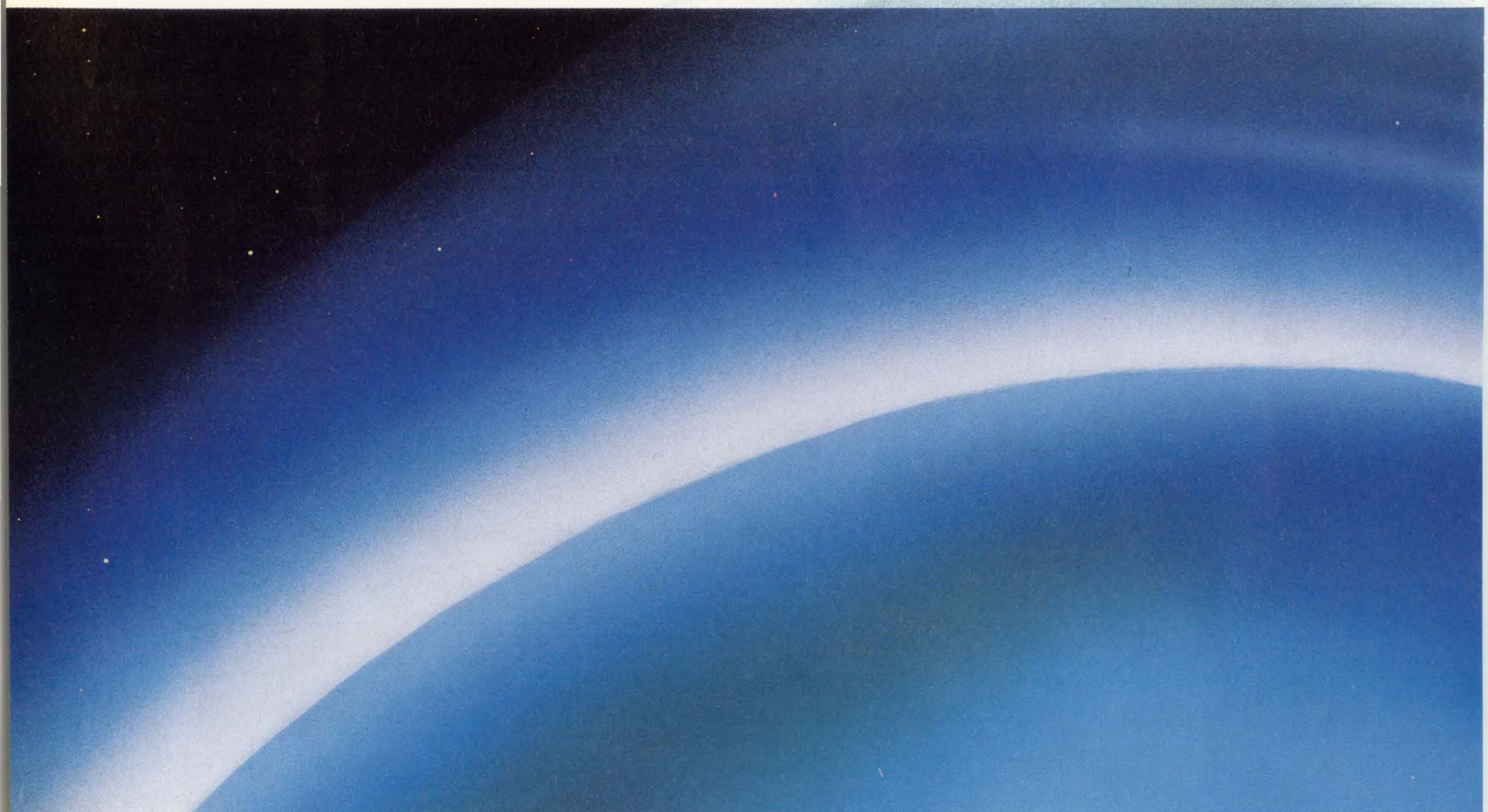

Zilog's Z80® MPU Family: It's the smartest way to add impressive performance and innovation without having to spend time learning and writing new code.

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So if you're looking for a way to upgrade an existing design, or for the extra performance you need for something entirely new, the smart move is to look to the Z80 MPU family. You'll find the combinations of features that will give you just what you need, including the high-performance Z181,™ Zilog's Smart Access (SAC™) Controller. And best of all, since you're already familiar with the Z80 code, the migration path couldn't be quicker.

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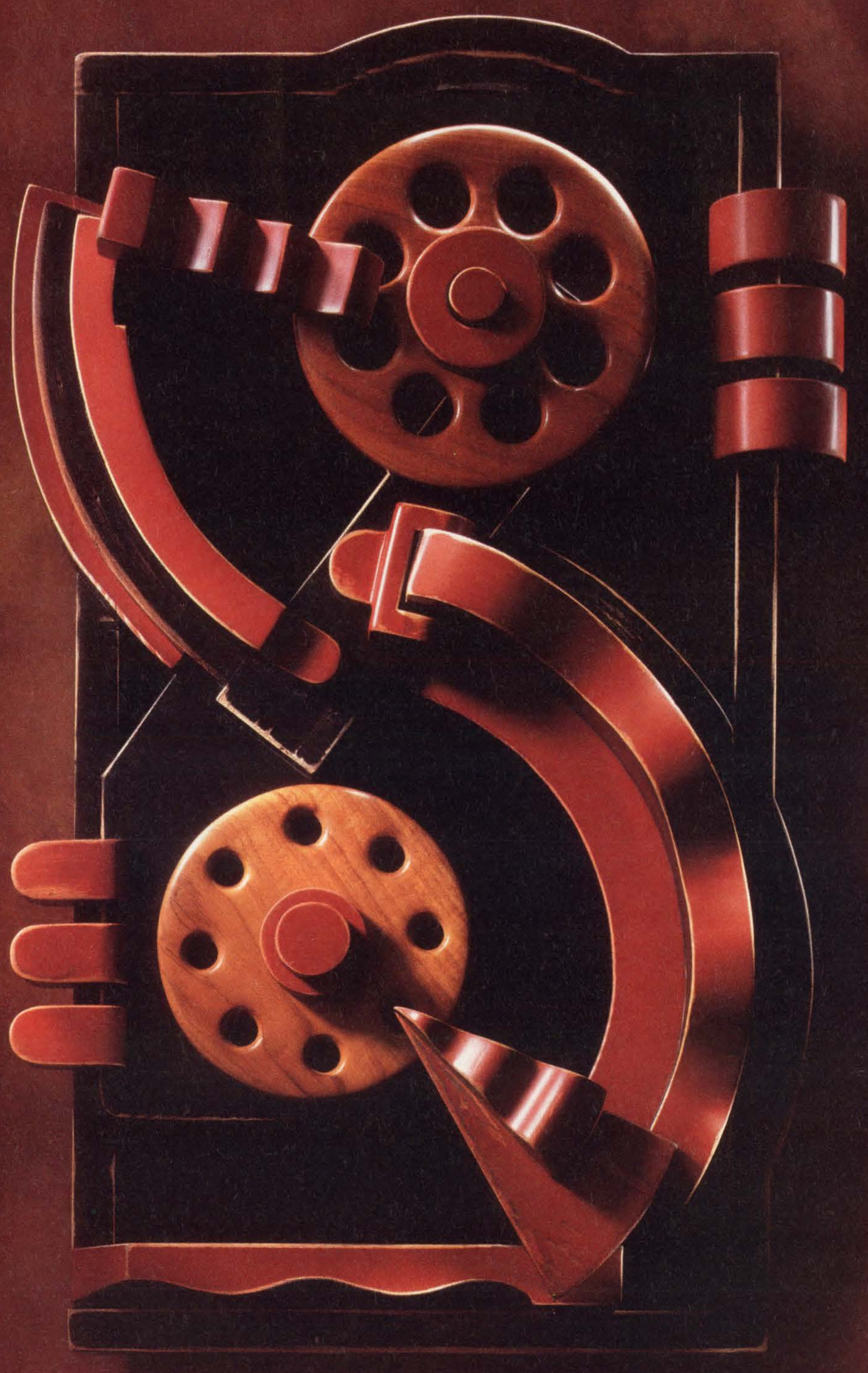

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Company notes new phone area code in New Jersey

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Questions raised by "PLD metastability" article

Several points need to be made about the article "Determine PLD metastability to derive ample MTBFs" (EDN, August 5, 1991, pg 147). To begin with, a more accurate and faster way to measure metastability is to use a digital scope with histogram capability. Signetics uses the HP 54120; the Tektronix CSA 803 is another scope that will work. You don't need a specially designed test-fixture circuit and the associated costs to build and use it.

If we want to measure state-of-the-art parts, we are dealing with products that have t_{SW}s of 115 psec. The number of metastability data points drops by a factor of 6000 with a 1-nsec change of t_R. This problem makes data collection very time consuming and inaccurate if it's done by the method demonstrated in the article.

The asynchronous data is a problem because data leading the clock at the device by a hair's breadth often causes dramatically different metastability readings than the data lagging the clock. Either one or the other of these cases always occurs if both the clock and the data are produced by pulse generators at fixed frequencies.

The t_{SW} will vary rather dramatically over temperature, perhaps 40% from 0 to 70°C. A 40% change in t_{SW} will have an explosive—that is, exponential—effect on MTBF. (It's unlikely that the part you are interested in will be operating at room temperature in your system.) It's difficult to set up a test with a home-made board and still be able to change temperatures. In addition, the parts begin to heat up significantly at higher frequencies, causing the t_{SW} to change. To rely on your measurements, the part under test should be measured in a controlled environment.

Finally, some parts do not respond in a classical manner, and the best way to determine this is by viewing a metastability histogram with incremental steps smaller than the part's t_{SW}.

One further note on the last page of the article, a formula for a 2-stage synchronizer was given as:

$$MTBF=\frac{e^{\left(\frac{t_R}{t_{SW}}\right)^2}}{W\ f_C f_D}.$$

Although this formula has appeared in other papers, it is in error and will calculate extremely optimistic MTBFs that don't represent real-life failure rates. A more reasonable formula is

$$MTBF=\frac{e^{\left(\frac{t_R+t_C-t_P}{t_{SW}}\right)}}{W\ f_C f_D}.$$

where t_C is the clock period and t_P is the normal propagation delay through the device.

Charles Dike
Senior Design Engineer
Signetics Corp

Comments about EMC Law and its effects

In reference to Brian Kerridge's article about the EMC (Electromagnetic Compatibility) Law (EDN, September 16, 1991, pg 57), my impression of his understanding of this law is that he regards it as a new obstacle to free trade. I think this is untrue.

First, in densely populated Europe, there is an urgent need for strict EMC rules.

Second, for the many manufacturers in the US that are not as multilingual as they should be for exporting, it will be easier [for them] to qualify because qualifying in just one European country is sufficient to qualify throughout the EEC (European Economic Community). So, no more language barrier.

In the Editor's Note to Berlin reader, Guido Körber (EDN, June 20, 1991, pg 31), the Editor asked "Which side of the Wall were you on?" In Memoriam to the Cold War situation: In the eastern part of this city, possession of EDN could have led to troubles; in the western part, the transfer of EDN to the eastern part could have caused "COCOM" (Coordinating Committee for Multilateral Export Controls) troubles.
Friedrich Widmann
Berlin, Germany

Reader extols editorial

Charles Small's editorial, "Make FPGA design easier" (EDN, October 10, 1991, pg 49), is the best editorial for quite a long time. As a designer and user from early 1983, I completely agree with him. And what [should we] say about the problems of teaching in the schools?
P Aviolat
Aviolat Electronique
CH-1056 Epalinges, France

HAVE YOUR SAY

EDN's Signals & Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. Send your letters to Signals & Noise Editor, EDN Magazine, 275 Washington St, Newton, MA 02158, or leave a note via MCI mail at EDNBOS. Or use EDN's bulletin-board system at (617) 558-4241: From the Main System Menu, enter SS/SOAPBOX, then W to write us a letter. You'll need a 2400-bps or less modem and a communications program set for 8,N,1.

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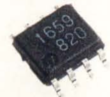

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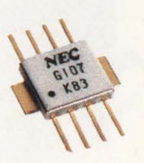

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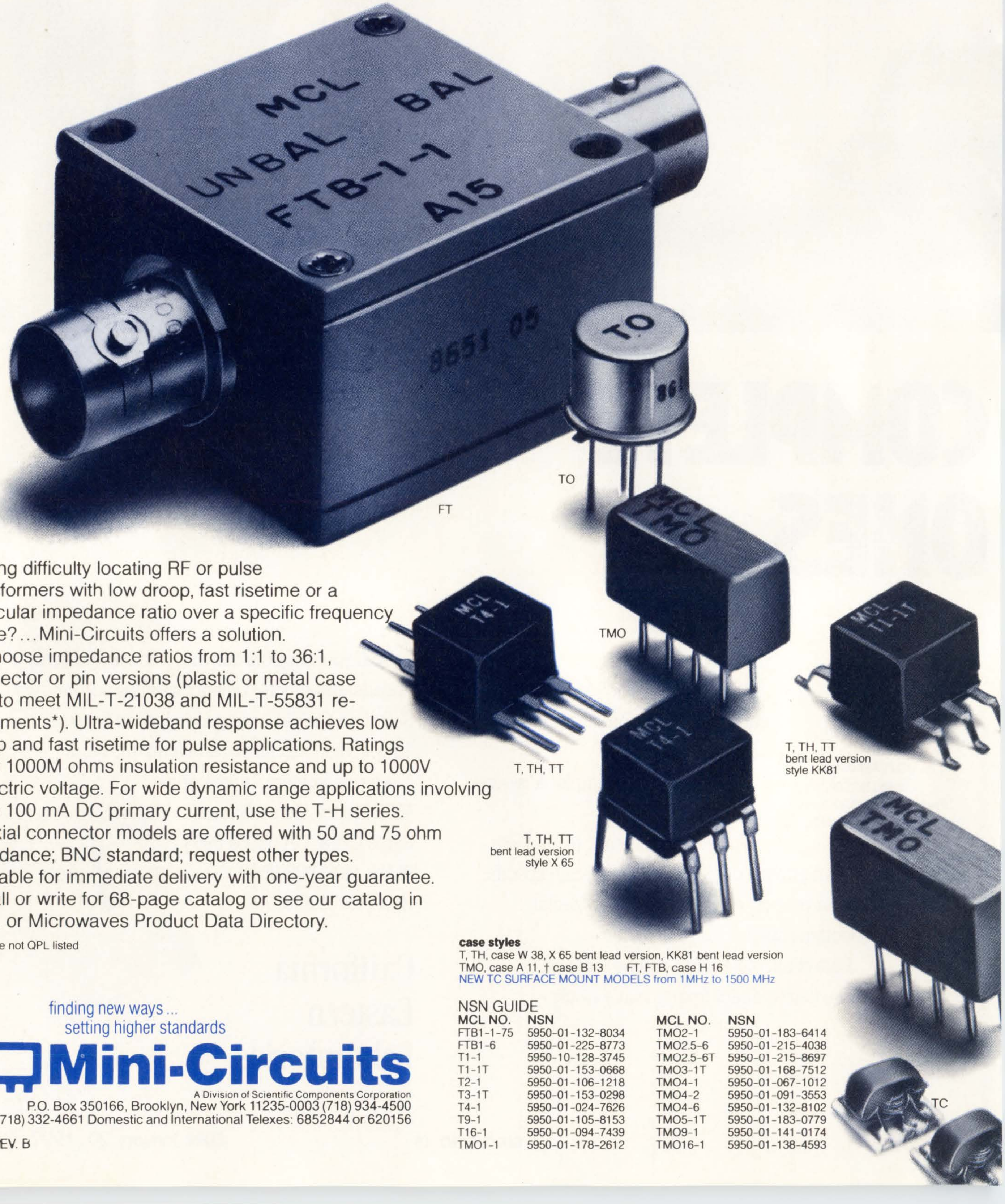

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MCL NO.	NSN	MCL NO.	NSN
FTB1-1-75	5950-01-132-8034	TMO2-1	5950-01-183-6414
FTB1-6	5950-01-225-8773	TMO2.5-6	5950-01-215-4038
T1-1	5950-10-128-3745	TMO2.5-6T	5950-01-215-8697
T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
T16-1	5950-01-094-7439	TMO9-1	5950-01-141-0174
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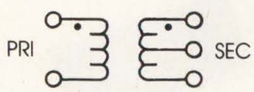
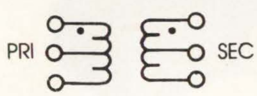
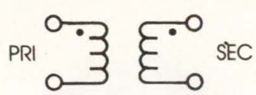
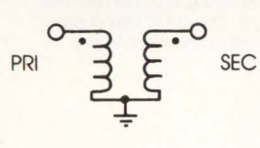
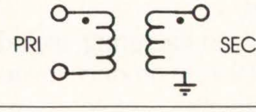
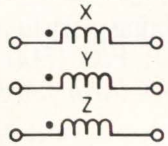
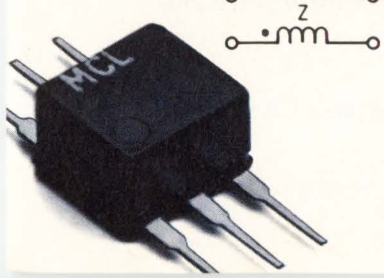
case style number see opposite page		MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS 3dB MHz	2dB MHz	1dB MHz	PRICE $ Qty. (1-9)
A* 	T	T1-1T	1	.05-200	.05-200	.08-150	.2-80	4.45
		T1-6T	1	.003-300	.003-300	.01-150	.02-50	6.95
		T2-1T	2	.07-200	.07-200	.1-100	.5-50	4.95
		T2.5-6T	2.5	.01-100	.01-100	.02-50	.50-20	4.95
		T3-1T	3	.05-250	.05-200	.1-200	.5-70	4.95
		T4-1	4	.2-350	.2-350	.35-300	2-100	3.25
		T4-6T	4	.02-250	.02-250	.05-150	0.1-100	4.45
		T5-1T	5	.3-300	.3-300	.6-200	.5-100	4.95
		T8-1T	8	.03-140	.03-140	.10-90	1-60	7.95
		T13-1T	13	.3-120	.3-120	.7-80	5-20	4.95
		T16-6T	16	.03-75	.03-75	.06-30	.1-20	5.65
	TH	T4-1H	4	10-350	10-350	15-300	25-200	5.95
	TMO	TMO1-1T	1	05-200	.05-200	.08-150	.2-80	7.95
		TMO2-1T	2	.07-200	.07-200	.1-100	.5-50	8.45
		†TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	8.45
		†TMO3-1T	3	.05-250	.05-250	.1-200	.5-70	7.95
		TMO4-1	4	.2-350	.2-350	.35-300	2-100	6.25
		TMO5-1T	5	.3-300	.3-300	.6-200	5-100	8.45
		TMO13-1T	13	.3-120	.3-120	.7-80	5-20	8.45
B* 	TT	TT1-6	1	.004-500	.004-500	.02-200	.1-50	6.95
		TT1.5-1	1.5	.075-500	.075-500	.2-100	1-50	5.95
		TT2.5-6	2.5	.01-50	.01-50	.025-25	.05-10	6.45
		TT4-1	3	.05-200	.2-50	.2-50	1-30	5.95
		TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95
		TT25-1	25	.02-30	.02-30	.05-20	.1-10	9.95
	TTMO	TTMO25-1	25	.02-30	.02-30	.05-20	.1-10	11.95
		TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	11.45
		TTMO4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	13.95
C 	T	T1-1	1	.15-400	.15-400	.35-200	2-50	3.25
		T1.18-3	1.18	0.01-250	0.01-250	0.02-200	0.03-50	5.65
		T1-6	1	.01-150	.01-150	.02-100	.05-50	5.65
		T1.5-1	1.5	.1-300	.1-300	.2-150	.5-80	4.45
		T1.5-6	1.5	.02-100	.02-100	.05-50	0.1-25	5.65
		T2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	4.45
		T4-6	4	.02-200	.02-200	.05-150	.1-100	4.45
		T9-1	9	.15-200	.15-200	.3-150	2-40	3.95
		T16-1	16	.3-120	.3-120	.7-80	5-20	4.45
		T36-1	36	.03-20	.03-20	.05-10	.1-5	6.95
	TO	TO-75	1	10-500	—	10-500	40-250	6.95
	TH	T1-1H	1	8-300	8-300	10-200	25-100	5.95
		T9-1H	9	2-90	2-90	3-75	6-50	6.45
		T16-H	16	7-85	7-85	10-65	15-40	6.45
	TMO	TMO1-02	1	1-800	1-800	2-500	—	9.45
		TMO1-1	1	.15-400	.15-400	.35-200	2-50	6.25
		TMO1.5-1	1.5	.1-300	.1-300	.2-150	.5-8	8.45
		†TMO2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	7.95
		†TMO4-6	4	.02-200	.02-200	.05-150	.1-100	7.95
		TMO6-1	6	.3-200	.3-200	.5-150	5-50	7.95
		TMO9-1	9	.15-200	.15-200	.3-150	2-40	7.95
		TMO16-1	16	.3-120	.3-120	.7-80	5-20	7.95
D 	T	T2-1	2	.050-600	.050-600	.1-400	.5-200	3.95
		T3-1	3	.5-800	.5-800	2-400	—	4.45
		T4-2	4	.2-600	.2-600	.5-500	2-250	3.95
		T8-1	8	.15-250	.15-250	.25-200	2-100	3.95
		T14-1	14	.2-150	.2-150	.5-100	2-50	4.95
	TMO	TMO2-1	2	.050-600	.050-600	.1-400	.5-200	7.95
		TMO3-1	3	.5-800	.5-800	2-400	—	8.45
		TMO4-2	4	.2-600	.2-600	.5-500	2-250	7.95
		TMO8-1	8	.15-250	.15-250	.25-200	2-100	7.95
		TMO14-1	14	.2-150	.2-150	.5-100	2-50	8.45
	FT	FT1.22-1	1.22	.005-100	.005-100	.01-50	.05-25	35.95
		FT1.5-1	1.5	.1-400	.1-400	5-200	1-100	35.95
E 	FTB	FTB-1	1	.2-500	.2-500	.5-300	1-100	36.95
		FTB1-6	1	.01-125	.01-125	.05-50	.1-25	36.95
		■FTB-1-75	1	.5-500	.5-500	5-300	10-100	36.95
F 	T	T-622	1	0.1-200	0.1-200	0.5-100	5-80	3.25
		T626	1	0.01-10	0.01-10	0.2-5	.04-2	3.95



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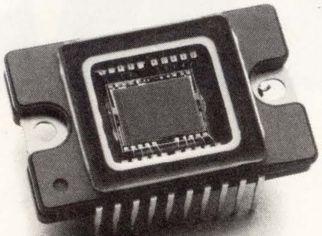
C72-2 REV. B

No guts.



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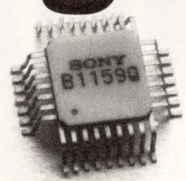

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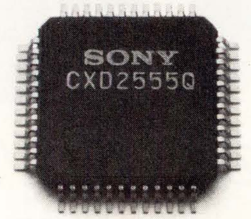

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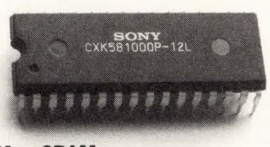

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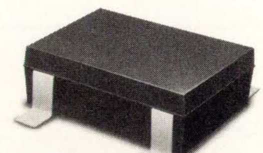

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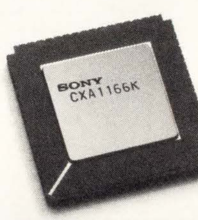

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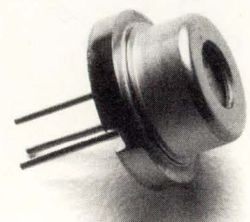

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CIRCLE NO. 20

EDITED BY JULIE ANNE SCHOFIELD

How damp is damp?

We have developed a product that measures relative humidity for our custom control system and require a reliable humidity-sensor element. The initial design used a Minicap2 from Panametrics (Waltham, MA), but the device did not meet specifications and is now unavailable in Australia. The sensor measured 5 to 95% relative humidity with a linear change in capacitance (200 pF ±15% at 33% RH).

Unfortunately, the only alternative device obtainable here is the Philips H1, which is capacitive but is also nonlinear. Can you please advise us of any known sources for humidity-sensor elements—not those built into modules—in the US?
Stuart White
EMS Control Systems
Osborne Park, Australia

Three companies that sell relative-humidity sensors are

General Eastern Instruments
20 Commerce Way
Woburn, MA 01801
(617) 938-7070
FAX (617) 938-1071

Newport Scientific Inc
Hygrodynamics Div
8246-E Sandy Ct
Jessup, MD 20794
(301) 498-6700
FAX (301) 490-2313

Ohmic Instruments Co
508 August St
Easton, MD 21601
(301) 820-5111
FAX (301) 822-9633

Gone, but not forgotten

In the August 19, 1991, issue you ran a question about pc-board layout. You suggested the 3-part Designers' Guide to Transmission Lines and Interconnections published in the June 23, 1988, issue. How can I obtain this article or back issue?
Dan Cavaliere
Tempustech Inc
Naples, FL

To get a copy of an article, contact University Microfilm. The charge is $11.75 per article, regardless of the article's length.

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For a back issue published within the past 10 years, contact EDN's Helen Benedict at our Newton, MA, address (phone (617) 558-4681, FAX (617) 558-4470). Back issues cost $10 each and must be prepaid.

Nerd stumps editors

Since you answer "nagging questions," here are several real naggers. What's worse, I get the idea that I'm supposed to know the answers because they're so obvious, but no one seems to know what the numbers are or where to look.

1. Devices connected to the dial-up telephone network are specified as to their "ringer equivalency," an indication that the load is the same as that many bells. Should the load be an impedance, probably all real, at a particular frequency (such as 8 kΩ at 40 Hz) or an RLC combination for the frequency-selective ringing (not used on single-party lines) like 10,000Ω and 20 µF at 5Hz.

2. Telecommunications devices for the deaf have been around for a long time and operate half duplex (one transmits at a time, both ends receive at all times) through the phone lines. The code used is Baudot (although now they sometimes also use ASCII). But what are the mark and space tone frequencies? How do these devices compare to a 300-baud asynchronous modem, which uses two frequency pairs? What is the bit rate? The phone-company people who deal with the stuff don't know and can't tell me who to ask. I'd like to make my computer and modem operate this way, and I'm sure others who either are hearing impaired or communicate with those who are would too.

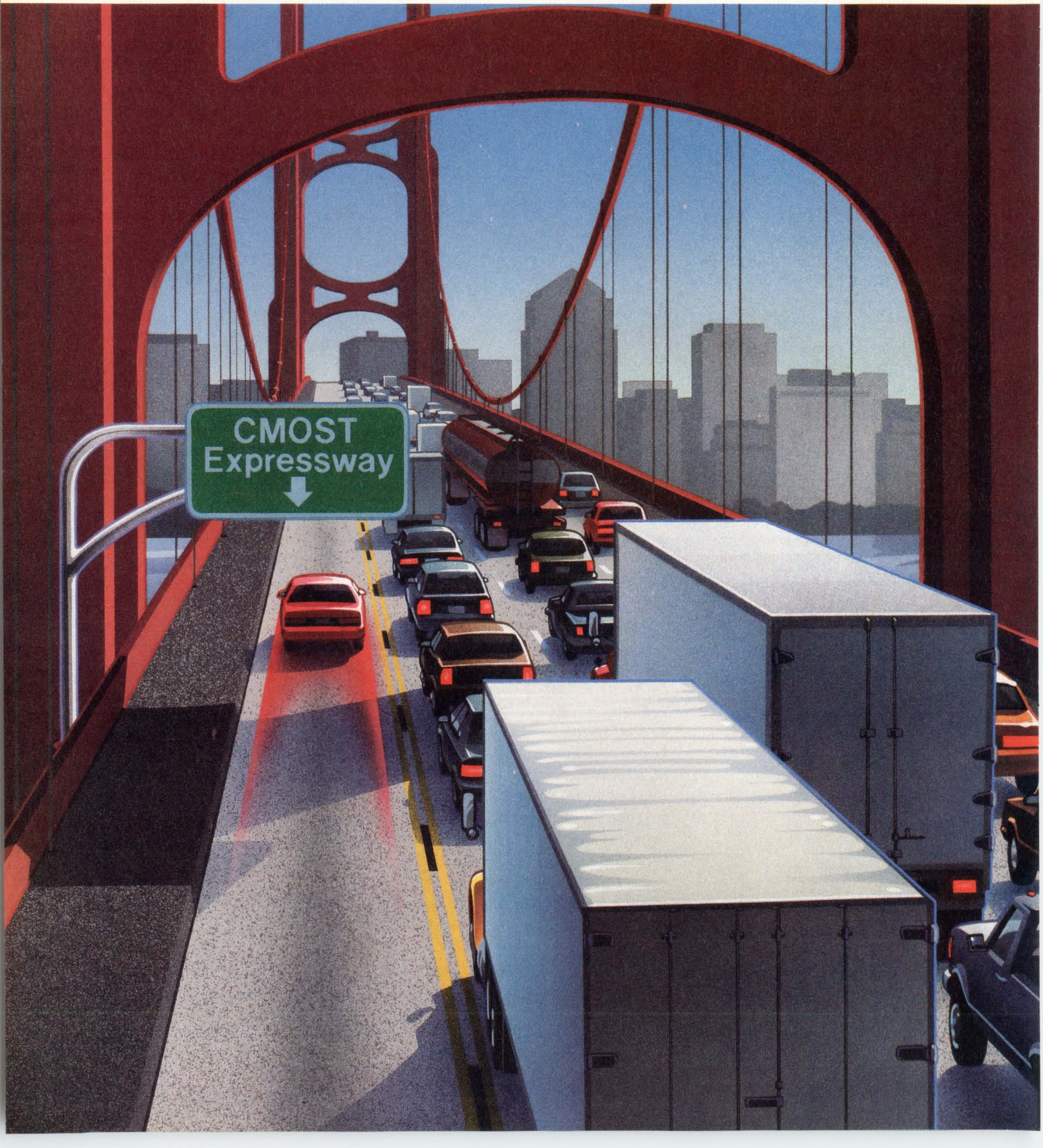
3. What is the carrier deviation for transmission of a satellite-relayed television signal? Since the television waveform is asymmetrical, what is the position of blanking with regard to the band edges of the channel? Does white cause a positive deviation of the carrier frequency or a negative one?

Since I am a nerd (a term that, as far as I'm concerned, isn't negative but simply informational), I worry about these questions while trying to get to sleep nights, so any information you could provide would be appreciated.
James Rieger
Telemetry Div
Naval Weapons Center
China Lake, CA

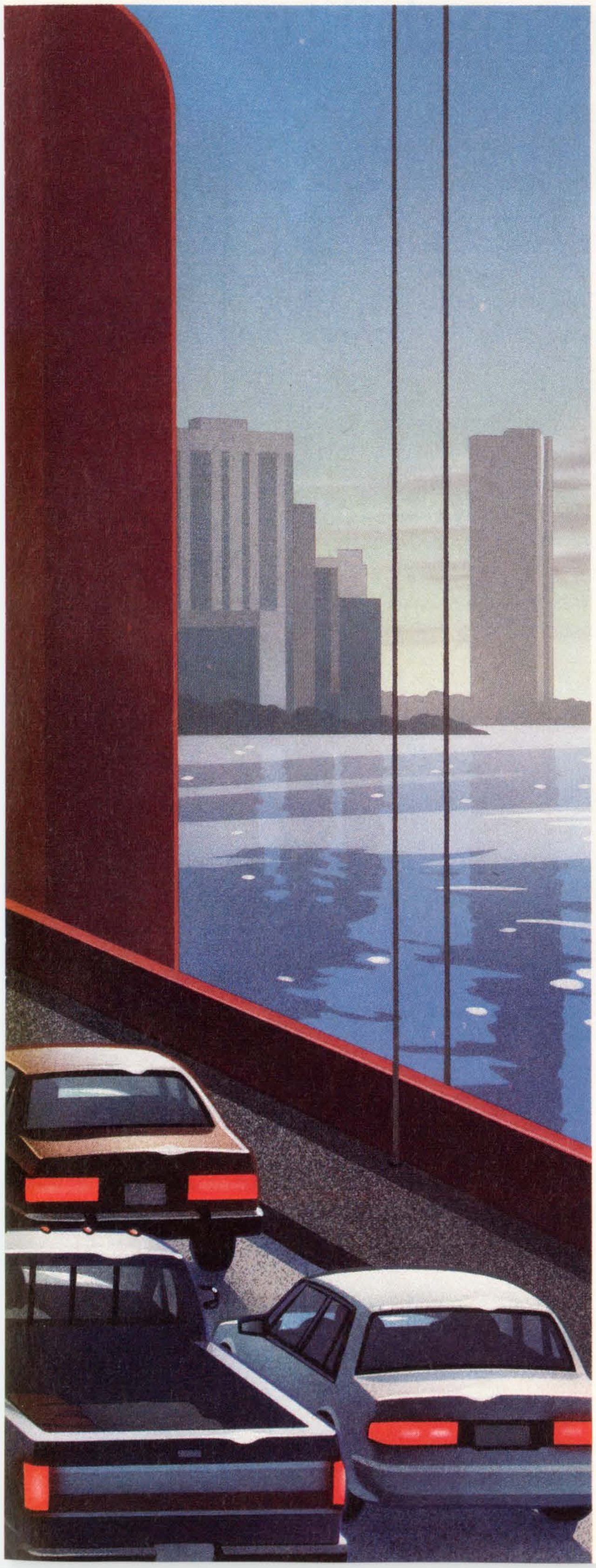
We hate to shake your faith in us, but the EDN editors are stumped and believe that the answers to your three questions are lost in the mists of time. Ask EDN urges any reader who has any information at all about the topics keeping Mr Rieger up nights to contact us at once.

Ask EDN solves nagging design problems and answers difficult questions. Address your letters to Ask EDN, 275 Washington St, Newton, MA 02158. FAX (617) 558-4470; MCI: EDNBOS. Or send us a letter on EDN's bulletin-board system at (617) 558-4241: From the Main System Menu, enter SS/ASK_EDN and select W to write us a letter.

Toshiba SRAMs Move Yo



u Into The Fastest Lane.



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CIRCLE NO. 21

Winds of change blow strong

The winds of change continue to blow. Events throughout the world show that change is continuous, whether it's revolutionary or evolutionary. Even small changes force us to do things differently. But most of us don't like change, and we resist it until we either adapt to it or get swept away by it.

Changes can be big, too, and the break-up of the Soviet Union's satellite countries is one of the best recent examples. At the time that Eastern Europe was in the midst of its turbulent changes, many people here in the US couldn't understand why the people involved didn't welcome the changes. Let's not get too smug. Here in the US we're still going through a big change—the break up of the Bell Telephone System into regional operating companies, or "baby Bells"—and people are still resisting it.

I've heard people talking about which long-distance phone company they should choose, which phone sets they should buy, what they can wire up themselves, and how to get phone equipment repaired. Life was so much simpler when the Bell System answered all our phone needs. Many people would like to abandon the competitiveness of today's communications industry for the peaceful time when one company provided for all their communications needs. It's no wonder that the telephone company became known as "Ma Bell." The change to a competitive market forces us to adapt and to make choices, not all of which are clear or easy.

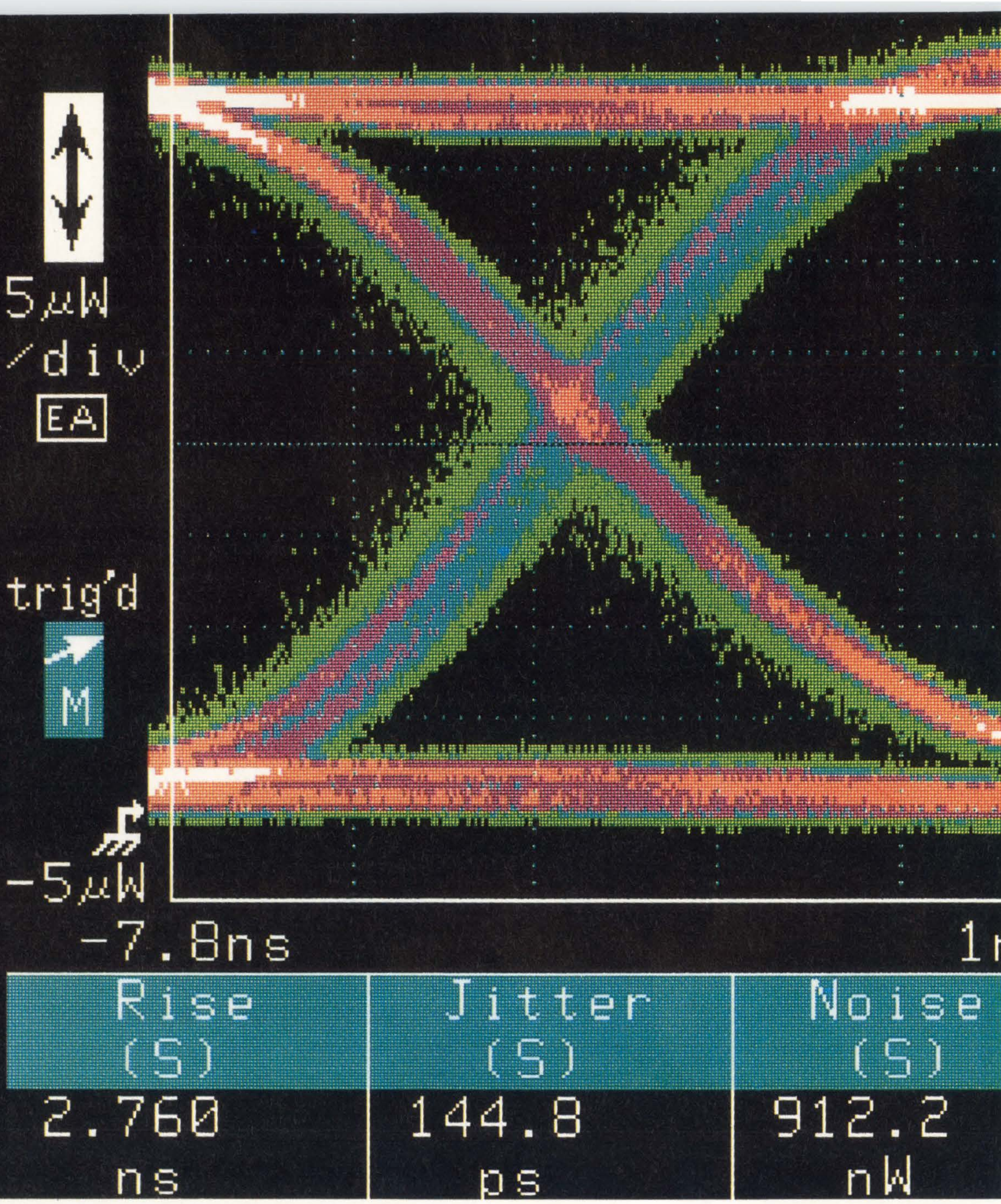
What is clear is that the US Congress should stop meddling in the telecommunications industry and stop telling the telephone companies what they can and cannot do. If these companies want to sell computer equipment, database services, and even access to cable-TV programs, let them. Yes, there are inequities among telecommunications companies, and yes, competition may favor some Bell companies. But it has always been this way. Some companies are always stronger and more competitive than others. No new industry starts with all the competitors on equal footings. It's time for the telecommunications industry to grow up, to welcome all entrants, and to let companies compete freely. As a friend of mine used to say, "Adapt or die." So it should be among telecommunications companies.

Jon Titus
Editor

Jesse H. Neal
Editorial Achievement Awards
1990 Certificate, Best Editorial
1990 Certificate, Best Series
1987, 1981 (2), 1978 (2),
1977, 1976, 1975

American Society of
Business Press Editors Award
1991, 1990, 1988, 1983, 1981

Send me your comments via FAX at (617) 558-4470, or on the EDN Bulletin Board System at (617) 558-4241 300/1200/2400, 8, N, 1.



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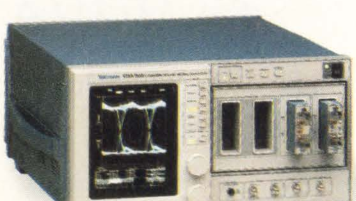

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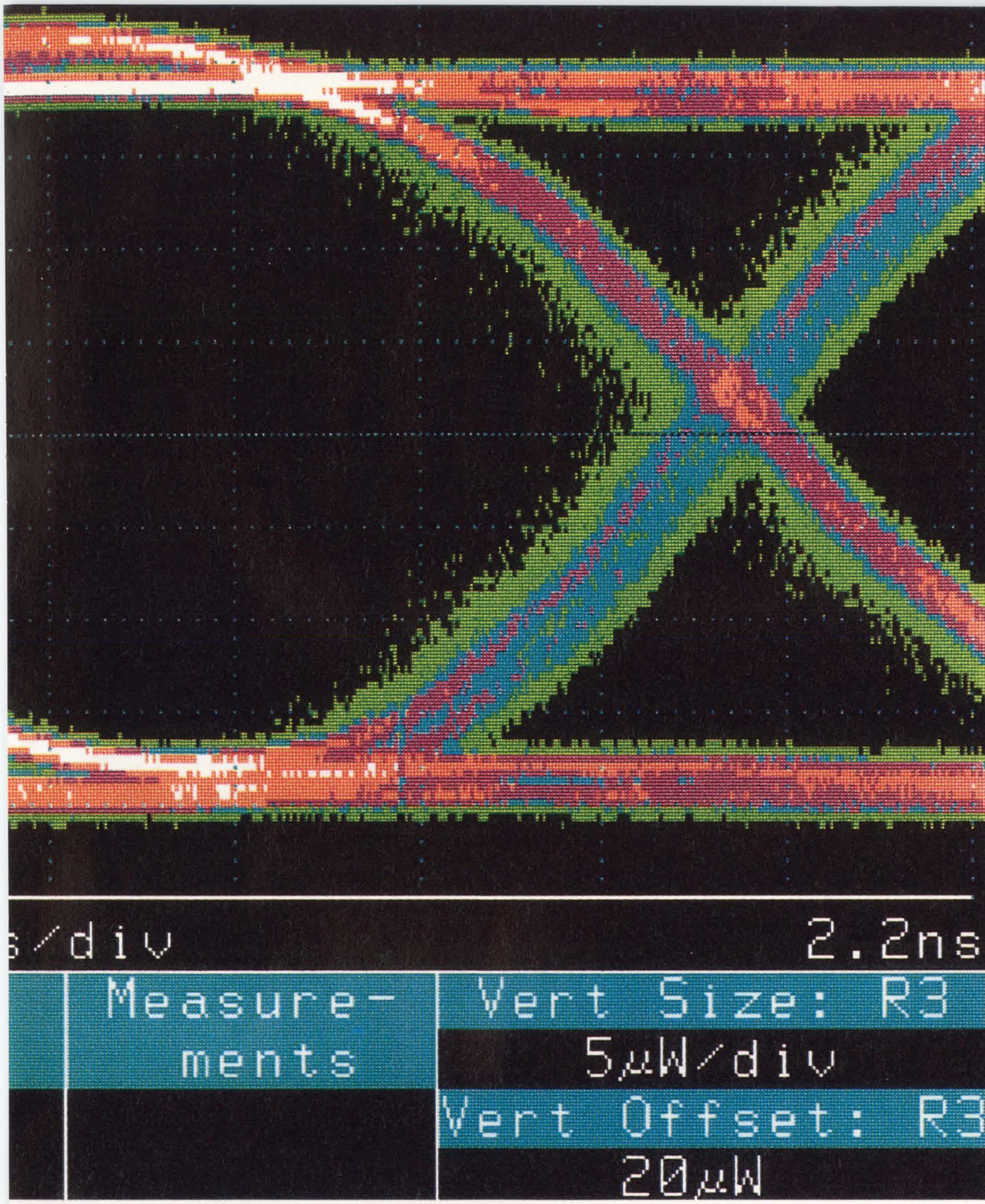
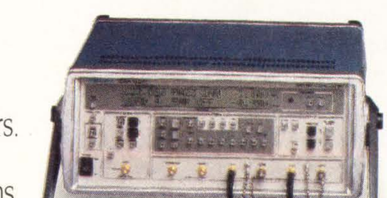


THE JITTERS.



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SELF-CALIBRATING A/D CONVERTERS

Monolithic devices enhance accuracy and linearity

DAVE PRYCE, Technical Editor

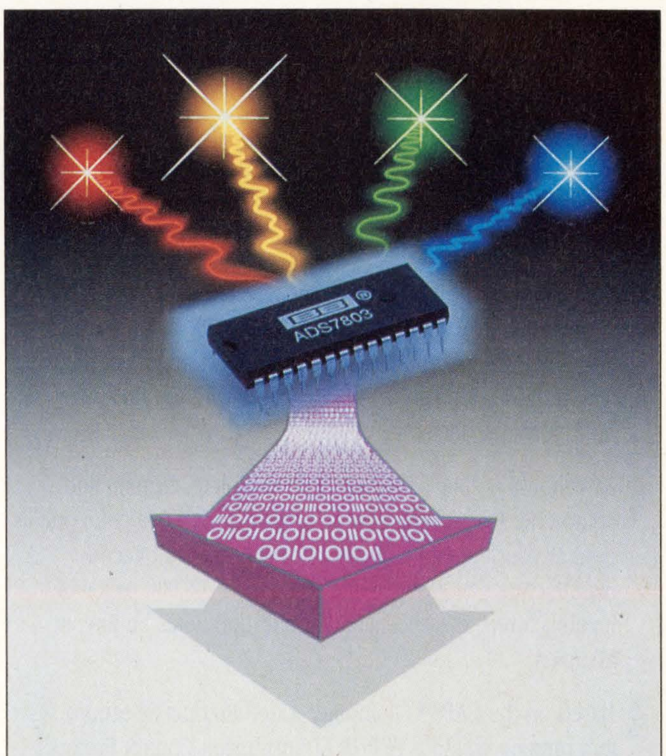
Self-calibrating ADCs can offer outstanding performance, particularly with regard to linearity specifications. To get the most out of these devices, however, you need to understand how they work and what they can actually do in a system application.

Although self-calibrating (autocalibrating) A/D converters are establishing a presence in many high-resolution applications, they don't necessarily constitute a panacea for all of the ills that can afflict a complete data-conversion system. For example, a monolithic self-calibrating ADC does not usually correct for external gain and offset errors—and most gain and offset errors arise from other elements in the system such as op amps or instrumentation amplifiers. Nevertheless, autocalibrating ADCs can greatly enhance the performance of systems having 12-bit or greater resolution, particularly in terms of accuracy and linearity.

For an in-depth view of device characteristics and system considerations from a manufacturer's viewpoint, see "Autocalibration—fact and fiction."

Analog Devices, a company that makes both monolithic and hybrid ADCs, claims there is no real need for autocalibration at resolutions less than 12 bits. The characteristics of the A/D conversion process support this contention. A converter has 2^n states, where n equals the number of bits of resolution. A 12-bit converter has only 4096 states, but a 16-bit converter has 65,536 states. The accuracy of a converter depends on the bit weight—the least significant bit (LSB)—and is equal to $1/2^n$. For a 12-bit converter, the LSB is equal to 0.0244% of the full-scale range (FSR), but for a 16-bit converter, the LSB is only 0.0015%. For a 10V FSR, the LSB of a 12-bit converter is equal to 2.441 mV; for a 16-bit converter it is only 152.588 μV.

Achieving the required accuracy gets increasingly difficult for higher-resolution converters and for lower full-scale ranges. For example, the LSB of a 20-bit converter with a FSR of 5V is less than 5 μV. Analog Devices states that, even with precise laser trimming of the



This 12-bit self-calibrating ADC, the ADS7803, is available from Burr-Brown. The low-power device can sample to 100 kHz and features a 4-channel multiplexer.

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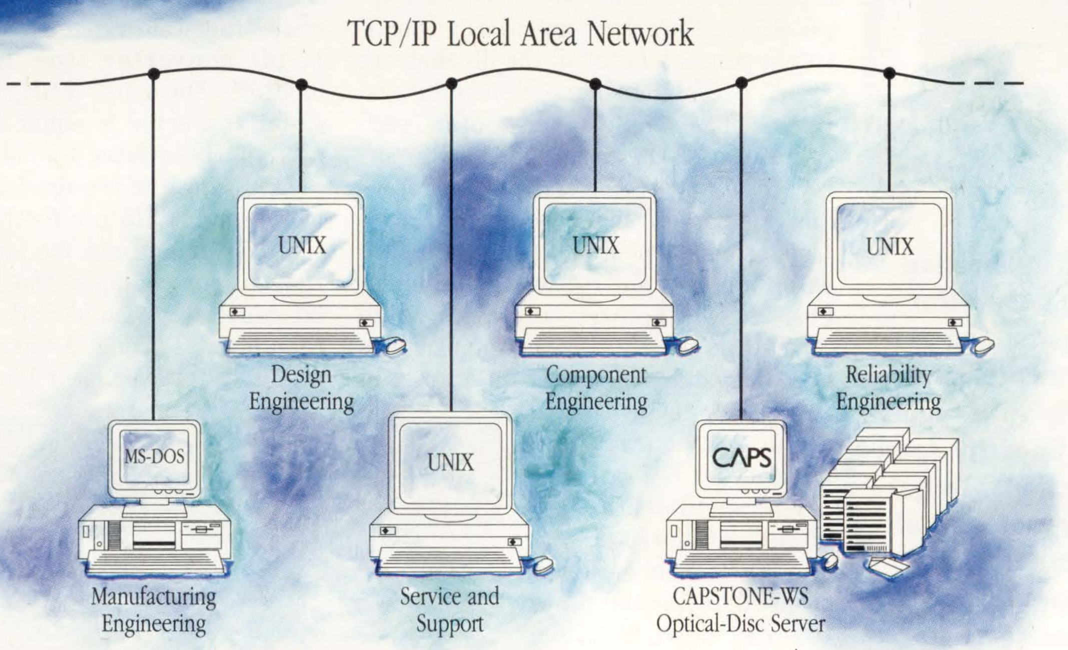

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CIRCLE NO. 24

resistors on its monolithic chips, problems arise at 16-bit resolutions because of changes in transistor and resistor characteristics following package assembly.

Laser trimming also adds complexity to the design and manufacture of resistor-based ADCs. The trimming requires accurate real-time control and constant monitoring of resistance values. Moreover, the equipment needed for laser trimming is expensive and requires skilled operators. These factors can add cost to the product and a degree of uncertainty to product yield. Of equal importance is the problem that once a laser-trimmed device is packaged, you can't make further adjustments to the device to compensate for changes that might occur over time.

ICs eliminate laser trimming

These considerations and the previously mentioned accuracy problem have spurred a few manufacturers to develop self-calibrating ADCs that do not rely on laser-trimmed resistors. Instead of using resistors to set the initial accuracy, self-calibrating chips use capacitors implemented in a CMOS process that features a switched-capacitor DAC architecture to maintain continuous accuracy.

Crystal Semiconductor was the first company to introduce a self-calibrating ADC based on capacitor-DAC CMOS technology and is a major supplier of monolithic chips to hybrid manufacturers. Other companies, such as Analog Devices, Burr-Brown, Harris Semiconductor, National Semiconductor, and Texas Instruments, offer devices that employ similar architectures.

The capacitor-DAC architecture used by Analog Devices in its 16-bit AD1876/AD676 series is typical of most self-calibrating A/D converters that digitally correct for nonlinearities. To accomplish the calibration, the device includes a 9-bit capacitor array and 11 16-bit words of on-chip RAM. **Fig 1** illustrates the basic circuitry of the front end of the AD1876 in the sample configuration.

In this configuration, V_{IN} charges all of the capacitors in CapDAC except the most-significant-bit (MSB). The MSB capacitor charges to V_{REF}, introducing a bipolar offset. To take the sample, the top-plate switches are opened, trapping the charge on the CapDAC. The device switches the sample/convert switch to analog ground and runs a successive-approximation algorithm on the nine capacitor switches, testing the top-plate voltage with respect to ground on each cycle. SubDAC is a resistor-string DAC that obtains the bottom 7 bits. The CalDAC corrects for errors in the CapDAC, using codes determined during the calibration operation. To isolate the input and reference from initial charging currents, the buffer switches insert a buffer between the inputs and the capacitors each time the capacitor configuration changes. The Dummy DAC balances the input to the comparator to ensure low offset and provide a remote ground sense.

The AD1876 and AD676 are members of a family of four devices that provide options for ac and dc specifications, output configuration, and package choices. The AD1876, which comes in a 16-pin DIP, is specified only for ac parameters and has a serial output. The AD676 comes in a 28-pin DIP, is specified for both ac and dc parameters, and has a 16-bit parallel output. Both

Text continued on pg 58

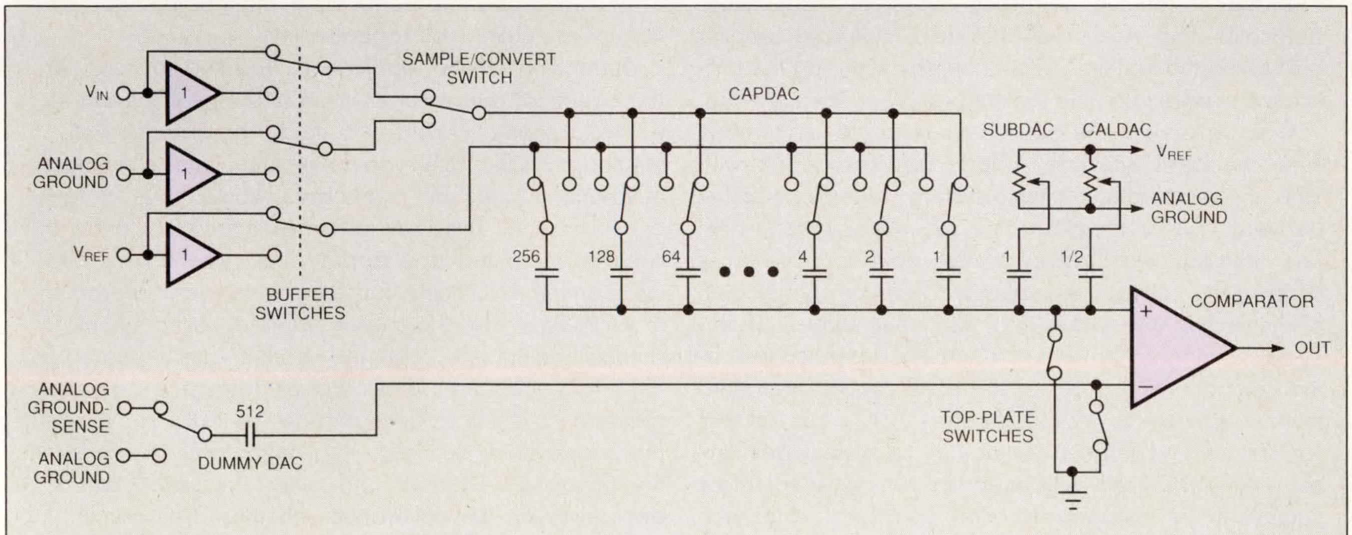

Fig 1—This capacitor-DAC architecture is typical of self-calibrating A/D converters that digitally correct for nonlinearities. Shown here is the 16-bit AD1876 from Analog Devices, which uses a 9-bit capacitor array and 11 16-bit words of on-chip RAM to accomplish the calibration.

Autocalibration—fact and fiction

GEORGE HILL, Burr-Brown Corp

Autocalibrating ADCs can offer outstanding specifications, with linearity foremost. However, as with other new techniques, autocalibrating's advantages can be oversold. The key to extracting real advantages from the hype is to understand what autocalibration does and why manufacturers use it. Autocalibrating ADCs can be the right choice in many applications, but a user experienced with conventional ADCs needs to consider the characteristics of calibration to get the most out of autocalibrated converters.

Although the data-sheet specifications for autocalibrating ADCs may show great linearity and low offset and gain errors, the use of these devices will not always eliminate the need to calibrate the complete system. For example, op amps or instrumentation amplifiers usually dominate the system's offset, and the voltage reference—typically external to the ADC—dominates the gain error. As a result, most precision applications need a system-calibration cycle to achieve overall accuracy.

To calibrate a system's offset, you need circuitry that grounds the input as close to the signal source as possible. This action should produce a 0V input to the ADC. By converting with the input of the system grounded, the output of the ADC represents all of the offsets contributed by the system. The system processor can store this data and later subtract it during normal operation to remove the effects of system offset. Future autocalibrating ADCs will include circuitry to simplify calibrating the system's offset, thereby reducing the calibration overhead on the system processor and software.

Gain error is more difficult to calibrate accurately. Even the best available voltage references drift with time and temperature, limiting system gain-error stability between visits to the calibration lab. Also, if the system has any gain, calibrating system gain error requires dividing the value of the voltage reference by the gain and injecting the result into the input stages of the system during calibration. Fortunately, signal-conditioning components in front of the ADC usually contribute minimal gain error. Autocalibrating ADCs can correct for the second largest contributor to system gain error—the ADC itself. Still, they do not adjust for error sources in the voltage reference, so a good reference remains important in any system whose absolute accuracy is critical.

One of the major features of autocalibration, according to data sheets and other press, is that the ADCs can recalibrate themselves to remove errors at any temperature. This capability raises several questions that are not always clearly answered in the data sheets. First, how often must the ADC recalibrate to maintain a certain accuracy? The answer depends on how stable the ADC is over time and with changes in temperature. Most autocalibrated ADCs have excellent linearity stability, which is fortunate because linearity is the second most difficult error to remove by means of a system-level calibration routine (after voltage-reference error), and system-linearity error comes mostly from the ADC. Typically, it isn't necessary to recalibrate linearity more often than every few days, unless the ambient temperature changes more than 30 to 40°C. Linearity is a specification where autocalibration really can approach—or even exceed—the levels commonly available with conventional ADCs.

Autocalibration accuracy and repeatability

A related question concerns what happens if an ADC is recalibrated several times at any given temperature. How much can the accuracy change from calibration to calibration? A ±0.5-LSB calibrated-accuracy specification means that the accuracy of the ADC can change as much as 1 LSB between calibrations, depending on the calibration resolution and its immunity to noise in the system. A system built using a 16-bit ADC with a ±0.5-LSB accuracy could thus yield a system with only 1-LSB repeatability. Unfortunately, most data sheets do not specify calibration repeatability.

Depending on the application, you should consider the effects of autocalibration on differential linearity in particular. Early versions of some autocalibrating ADCs yielded parts that achieved no-missing-codes after most calibration cycles but sometimes would have a few codes missing. This type of performance could be a problem in control-loop applications, where a missing code on the ADC could cause the loop to cycle around the missing code and never stabilize. Although most autocalibrating ADCs on the market can repeatedly achieve no-missing-codes, this performance can depend on system conditions outside the ADC. For example, system noise during the calibration cycle can affect the differential linearity and other calibrated errors, depending on the calibration scheme. The source of this noise is often the voltage reference, but noise can also come from digital clocks, changing levels on the bus, and fluctuating ground currents.

Another question designers must face is how to absorb the overhead downtime in the system when the ADC is recalibrating. At a minimum, the system requires this delay each time it powers up. To get maximum results from an autocalibrating ADC, other components of the system, particularly the voltage reference and the power supplies, must be sufficiently stable during calibration to achieve the required system accuracy. Because of this need for stability, calibration is not usually done until some time after system turn-on, and you need to include appropriate circuitry, or software, in the system to generate the delayed calibration command. In most systems, the extra milliseconds are usually no problem at power-on.

If an autocalibrating ADC needs periodic recalibration during normal operation or needs recalibration after temperature changes to meet system-accuracy requirements, you need to take this additional downtime into account when designing and specifying the system. This downtime is critical where you need to do conversions continually or where some external event triggers the conversions. Where conversions must be done continually over long periods of time, the stability of the initial calibration is of major importance. In signal-analysis applications, a series of samples is taken periodically, after which the data is analyzed. In these cases, it may make sense to run a calibration cycle after each set of samples, if there is enough time available. In systems where an external event triggers conversions, either the stability of the ADC after power-up must be good enough to maintain accuracy until the system is powered-down, or the system must be specified for limits on how often trigger events can come, to leave time for recalibration.

In applications where the total power consumption of the system is important, you need to include the calibration time in determining the system's power requirements. Unlike many conventional ADCs, self-calibrating ADCs can't be simply turned off between conversions to save power, although some of the newer parts have power-down modes that retain the calibration data while drawing very little supply current between conversions.

Avoiding laser trimming's trimmings

Also, remember that manufacturers choose autocalibrating architectures for reasons beyond what they promote in the data sheets. Some start-up firms have chosen the autocalibrating approach in part to avoid having to develop methods to trim the thin-film resistors often used in conventional architectures, perhaps because digital-logic designers are easier to find than laser-trim experts. The alternative is to use digital logic on chip to trim linearity. The start-ups accept larger die sizes, more complex design tools and more expensive fabrication; they plan to offset these higher costs by eliminating trim times, the equipment needed to deposit the resistors and trim them, and the costs of developing the thin-film experience base.

A manufacturer's decision to use autocalibration logic to avoid thin-film resistors has a direct impact on system designers. The elimination of thin-film resistors means that these converters can't easily handle most of the standard industrial analog-input ranges, because of the digital CMOS processes used for the ADCs. In many industrial applications, analog signals pass between various equipment in 0 to 5V, 0 to 10V, ±5V and ±10V ranges, in part to improve system noise immunity compared with lower voltages. The problem occurs when the supply to the autocalibrating ADC is below the voltage level of the input signal. Even for a 0-to-5V analog input range, there is a problem if an external part transmits a full-scale 5V signal to the ADC when its power supply has fallen to 4.5V or 4.75V. In this case, the system must divide down the input signals before they get to the ADC. Thus, in many applications, removing the resistors from the ADC means the system designer will have to use them externally to attenuate the standard industrial voltage ranges to the level the autocalibrating ADC can tolerate.

Autocalibrating ADCs will be increasingly valuable alternatives as their calibration capabilities are extended to include adjustment for system offset and gain errors, providing full system calibration in more applications. Manufacturers are starting to offer these features on some newer, very-low-speed ADCs, but not on the autocalibrating ADCs now on the market. However, in the general-purpose range of 12 to 16 bits and 1- to 100-μsec conversion rates, autocalibrated ADCs allow a new approach to providing excellent linearity.

George Hill is strategic marketing engineer for Burr-Brown in Tucson, AZ.

devices feature a sampling rate of 100 ksamples/sec, total harmonic distortion (THD) of 0.002%, a S/N ratio of 90 dB, and a full-power input bandwidth of 1 MHz. To optimize performance, Analog Devices partitions these devices into two monolithic chips, a digital control chip fabricated in CMOS and an analog ADC chip fabricated in BiMOS.

Device minimizes all errors

Taking self-calibration to a higher level is National's ADC1241, a 12-bit + sign converter that minimizes errors in gain, linearity, and offset. The ADC performs a conversion in 8.7 μsec and produces all 13 bits in parallel. A S/H circuit simplifies the analog interface. The internal self-calibration system reduces linearity errors to less than ±0.5 LSB, and gain and offset errors to less than 1 LSB.

The block diagram in **Fig 2** shows the converter's main components. In addition to the main DAC, the converter includes a linearity-correction DAC and an offset-cancellation DAC that connect to the comparator. During a conversion, the successive-approximation register (SAR) controls the output of these DACs, which correct the output of the main DAC for gain and linearity errors and cancel the comparator's offset voltage. Under microprocessor control, the converter can initiate a calibration procedure at any time to correct for errors.

During normal operation, switch S_1 connects the comparator to the analog input, and switch S_2 connects the comparator to the main DAC. To enable the offset-correction system and perform an auto-zero routine, S_1 and S_2 are switched to ground, disconnecting the analog input and the main DAC from the comparator's input. The SAR then controls the offset-DAC's output. A successive-approximation algorithm (similar to the one used to control the main DAC during a conversion) finds the offset-DAC input code that results in the lowest offset error and stores this code in the offset register. A complete offset-correction cycle requires 13 μsec.

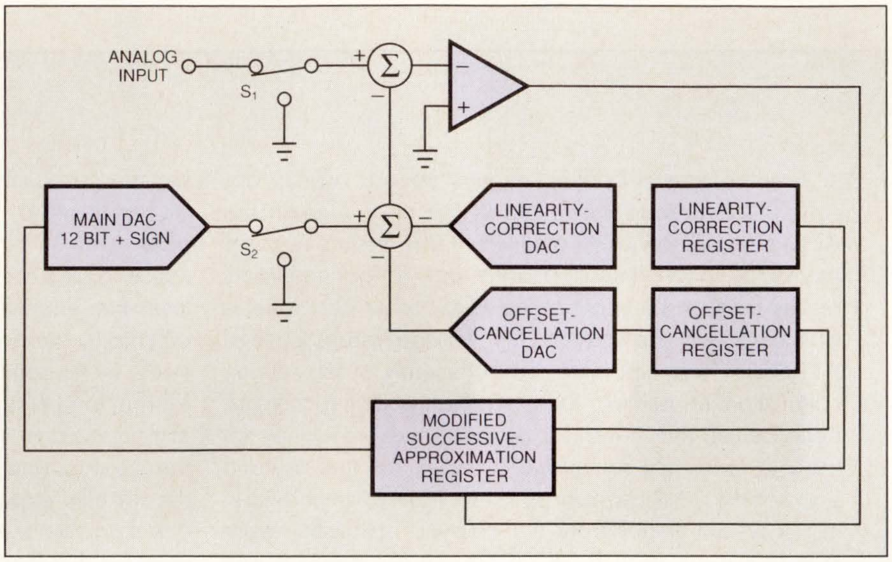

Fig 2—A linearity-correction DAC and an offset-cancellation DAC both connected to a comparator are main components of National Semiconductor's 12-bit ADC1241. During a conversion, the successive-approximation register (SAR) controls the output of these DACs, which correct the output of the main DAC for gain and linearity errors and cancel the comparator's offset voltage.

To eliminate linearity errors, the ADC1241 uses a more complex procedure than the one just described for offset correction. As a simplified example, consider a 3-bit A/D conversion. To perform the correction routine, S_1 is switched to ground and the main DAC is given an input code of 010. Because capacitive DACs allow subtraction of the result of one code from that of another on successive clock cycles, the circuitry applies a second code, 001, to the DAC and subtracts its output from the output produced by the first code. If the DAC has no errors, the difference between the two output voltages (in this case the mismatch between the MSB and all of the less significant bits) will be 1 LSB. Any mismatch will cause an error voltage.

The linearity-correction DAC then follows a successive-approximation routine to find a correction voltage that will cancel this error. The procedure repeats for each bit until it finds all of the necessary correction factors. For this 3-bit example, the next test will be 100 − 011. The correction codes are stored in the correction register for use during subsequent conversions. A complete linearity error-correction cycle requires 698 μsec.

Most monolithic self-calibrating ADCs operate in a similar fashion. Another common feature is their lack of an on-chip reference. Manufacturers cite various reasons for the absence of a reference, including process incompatibilities and noise constraints—particularly at the 16-bit level. Digital CMOS technology, for example, does not lend itself to the fabrication of an accurate, low-drift reference. In some cases, the need for an additional pin to bring out the reference restricts packaging choices. **Fig 3** shows the typical block diagrams of the functions in a traditional ADC **(a)**, a self-calibrating ADC **(b)**, and a delta-sigma ADC **(c)**.

In the traditional ADC, the reference is typically on chip, but other

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SELF-CALIBRATING A/D CONVERTERS

functions are not—although many devices now include the track and hold circuitry. Calibration circuitry is done in software. In the self-calibrating ADC, the reference is off chip for reasons previously cited. In the delta-sigma converter, the calibration circuitry adjusts only for offset and full-scale errors; there is no capacitor-DAC to compensate for linearity errors. The reference may, or may not be on chip, depending on whether the converter is designed for signal-processing or dc-accurate applications. Of course, for hybrid circuits the manufacturer has essentially complete freedom as to what to include.

With some exceptions, monolithic self-calibrating ADCs have successive-approximation architectures and provide resolutions in the 12- to 16-bit range. These general-purpose types have conversion rates in the 20- to 100-kHz range. Crystal Semiconductor, for example, makes several self-calibrating ADCs that use a successive-approximation architecture and fit into the general-purpose category. It also offers specialized types such as the CS5412, a 12-bit 2-step flash converter that features a 1-MHz sample rate, and the CS5501/CS5503 16/20-bit devices that use a delta-sigma architecture.

Designed for accurate dc measurements, the CS5501 and CS5503 feature a 6-pole, lowpass Gaussian filter with an adjustable corner frequency from 0.1 to 10 Hz. The 16-bit CS5501 features a maximum linearity error of ±0.0015% and offset and full-scale errors of ±0.5 LSB. The differential nonlinearity of a 16-bit, no-missing-codes performance is ±0.125 LSB.

The 20-bit CS5503 has higher offset and full-scale errors of ±4 LSB but offers greater dynamic range, often eliminating the need for external gain scaling. The typical linearity error is ±0.0003%. For both the CS5501 and CS5503, you can initiate the on-chip, self-calibration circuitry at any time or temperature to ensure the specified offset and full-scale errors. You can also use these devices in system-calibration schemes to null offset and gain errors in the input channel.

Burr-Brown offers a pair of 12-bit self-calibrating ADCs, the ADC7802 and the ADS7803. These devices are actually Siemens parts SDA0812 and SDA1812, respectively. Because of its expertise and penetration in the ADC and DAC market, Burr-Brown has an agreement with Siemens to market and sell these devices. Both the ADC7802 and ADS7803 feature multiplexed 4-channel analog inputs and can convert in 8.5 μsec for a 117-kHz throughput rate. Although identical in architecture and pin-out (both devices come in 28-pin packages), their respective performance characteristics show some subtle and not-so-subtle differences.

For example, the ADC7802 is optimized for dc precision and can handle input-signal frequencies only to 500 Hz. Conversely, the ADS7803

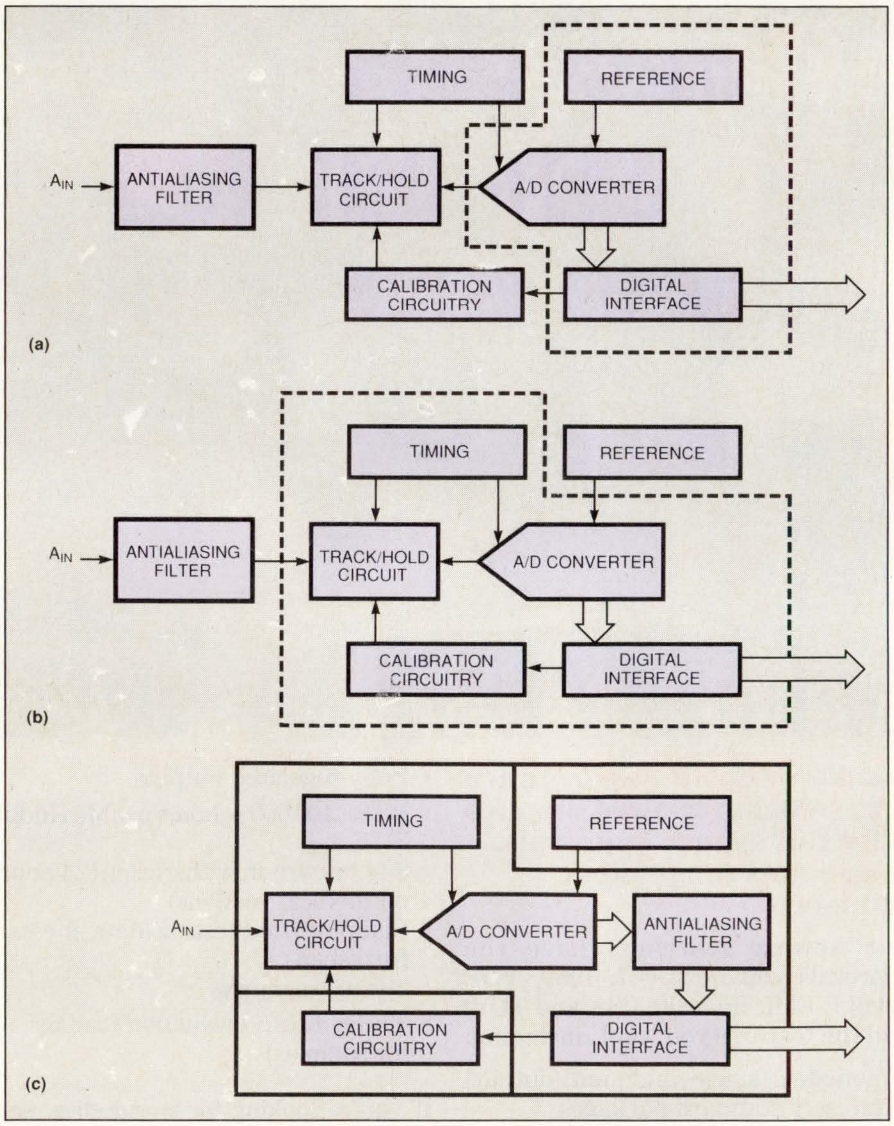

Fig 3—The partitioning of A/D converter architectures varies widely. Shown here are the traditional approach (a), a self-calibrating device (b), and a delta-sigma converter (c). The Reference in c may or may not be on chip.

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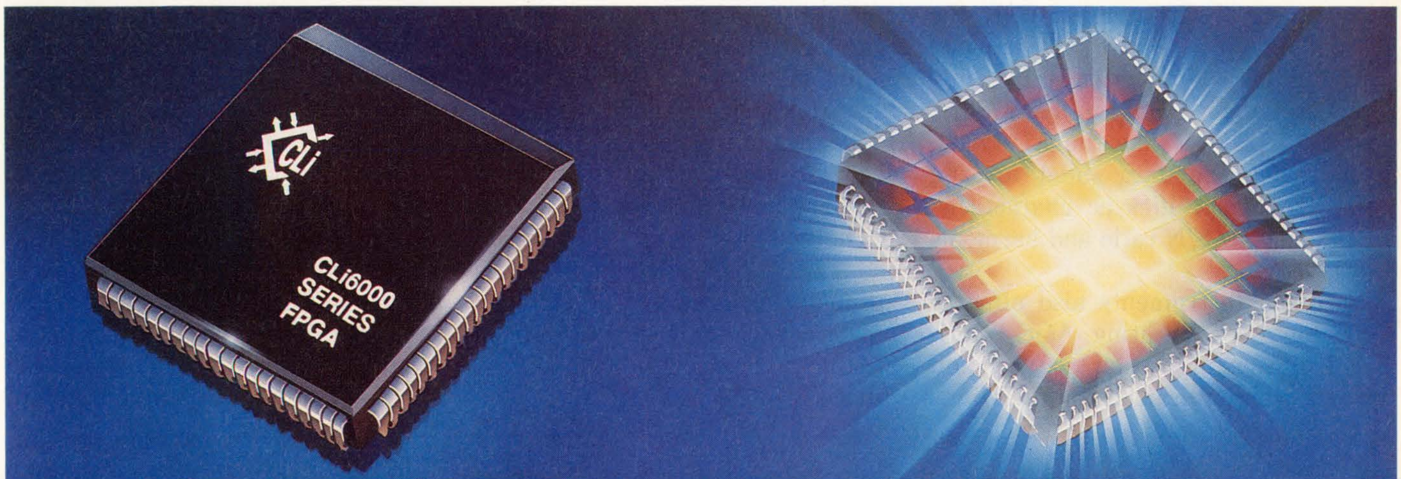

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is optimized for dynamic performance and can handle input-signal frequencies to and beyond 50 kHz. Although both devices operate from a 5V supply and have a typical power consumption of 10 mW, the ADS7803 adds a power-down mode that reduces consumption to 50 μW—a desirable feature for portable equipment. Also, although both devices feature input-channel matching to within ±0.25 LSB, the total unadjusted error (all channels) of the ADC7802 is ±0.5 LSB, somewhat better than the ADS7803's ±0.75 LSB. Unlike the ADC7802, however, the data sheet for the ADS7803 specifies ac characteristics such as S/N ratio and harmonic distortion.

Texas Instruments also offers a 12-bit self-calibrating ADC. Optimized for industrial control and data-communications applications that require minimum system noise, the TLC1225 features differential inputs that reduce system error created by common-mode noise. The ADC is compatible with most microprocessors and digital signal processors (DSPs), including the company's TMS320 family. The TLC1225 accommodates both unipolar and bipolar operations, outputs data in a parallel word, and interfaces directly to a 16-bit data bus. Output code for bipolar conversion is in 2's-complement format, which facilitates numerical computations by DSPs and microprocessors. Output code for unipolar conversion is in standard binary format.

The self-calibration technique of the TLC1225 affords simultaneous automatic calibration of seven internal capacitors in the A/D conversion circuitry. This calibration occurs during a nonconversion cycle and requires 300 clock cycles to complete. A conversion period requires only 24 clock cycles, and the ADC initiates either cycle at any time by writing a command to the data bus. The chip's self calibration produces a typical integral nonlinearity error of ±1 LSB, a maximum offset error of ±1.5 LSB, and unadjusted positive and negative full-scale error of ±2 LSB.

Somewhat out of the mainstream of most monolithic self-calibrating converters is the HI-7159A from Harris Semiconductor. Designed for use in laboratory instruments, industrial process control, and weight and part-counting scales, this 5½-digit ADC uses a dual-slope integrating technique that enables it to resolve input changes as small as 1 part in 200,000 (10 μV for a 2V full-scale reading). This degree of resolution is nearly equivalent to

Table 1—Representative self-calibrating A/D converters

Manufacturer	Part number	Resolution (bits)	Conversion rate (kHz)	Input bandwidth	Linearity error (±LSB)	S/N ratio (dB)	THD (dB)	Output data format	Comments	Cost
Analog Devices	AD676	16	100	1 MHz	1.0	88	−95	16-bit parallel	Characterized for ac and dc.	$38 (100)
	AD1876	16	100	1 MHz	1.0	90	−95	Serial	Characterized for ac only.	$33 (100)
Burr-Brown	ADC7802	12	117	500 Hz	0.5	NS	NS	Two 8-bit bytes	Optimized for dc precision, has 4-channel multiplexer.	$18.95 (100)
	ADS7803	12	117	50 kHz	0.75	71	−75	Two 8-bit bytes	Optimized for ac performance, has 4-channel multiplexer.	$19.95 (100)
Crystal Semiconductor	CS5012A	12	100	NS	0.5	73	−82	Parallel, serial	3-state I/O	$19.50 (1000)
	CS5412	12	1000	4 MHz	0.75	70	−74	Parallel	2-step flash, 3-state I/O.	$60 (1000)
	CS5501	16	4	10 Hz	0.125	NS	NS	Serial	Delta-sigma type, 6-pole filter.	$13.60 (1000)
Harris Semiconductor	HI-7159A	≈18	15 or 60 conversions/sec	NS	Digital auto-zero	NS	NS	Parallel, Serial, UART	Dual-slope integrating type, has 200,000-count resolution, 5½ digit.	$15 (100)
Micro Networks	MN6450	16	50	NS	1.0	88	−98	16-bit parallel	Hybrid IC includes reference, analog input buffer, control logic, μP interface.	$175 (100)
National Semiconductor	ADC1241	12+sign	55	25 kHz	0.5	76	NS	13-bit parallel	1-LSB gain and offset error.	$15.90 (100)
	ADC12451	12+sign	83	25 kHz	0.5	76	−82	Two bytes	Characterized for ac and dc.	$14.90 (100)
Texas Instruments	TLC1225	12+sign	83	NS	1.0	NS	NS	13-bit parallel	Differential or single-ended inputs, compatible with TMS320 DSP family.	$16.74 (1000)

Note: NS = Not specified

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18-bit accuracy. The ADC's auto zeroing features virtually eliminate zero-drift with temperature changes, and its integrating architecture minimizes the long settling times commonly seen in delta-sigma converters.

To enhance microprocessor compatibility, the HI-7159A includes four interface options: 8-bit parallel, UART serial, 32-device UART serial, and synchronous serial. The UART serial modes are user programmable for baud rates to 19,200. The 32-device serial mode permits connection and individual addressing of as many as 32 devices on a 2-wire serial line. The host may direct the ADC to measure and report the internal offset voltage, the input voltage plus the offset voltage, or the default. In the default mode, the ADC measures the internal offset and input voltages and subtracts the offset voltage from the input voltage. The HI-7159A's resolution is switchable between a high-resolution 200,000-count (5½-digit) mode and a high-speed 20,000-count (4½-digit) mode.

Manufacturers of hybrid ADCs are free to include other circuit functions in addition to the commonly used monolithic self-calibrating chip. For example, Micro Networks' MN6450 16-bit A/D converter includes an analog input buffer, a 4.5V reference, timing, and control logic, a microprocessor interface, and 3-state output buffers that provide a 16-bit-wide data output. The hybrid circuit provides true 16-bit performance, including no missing codes and 0.0015% integral linearity. The MN6450 features a 50-kHz sampling rate, an 88-dB S/N ratio, and −98-dB harmonics and spurious noise. As with most high-performance hybrid devices, the MN6450 is available in several temperature and performance grades, including MIL-STD-883. EDN

References

1. Linear Applications Seminar Handbook, 1989 and 1991, National Semiconductor, Santa Clara, CA.
2. Analog/Digital Conversion Data Book, Crystal Semiconductor, Austin, TX.

Article Interest Quotient
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High 476 Medium 477 Low 478

For more information . . .

For more information on the self-calibrating ADCs discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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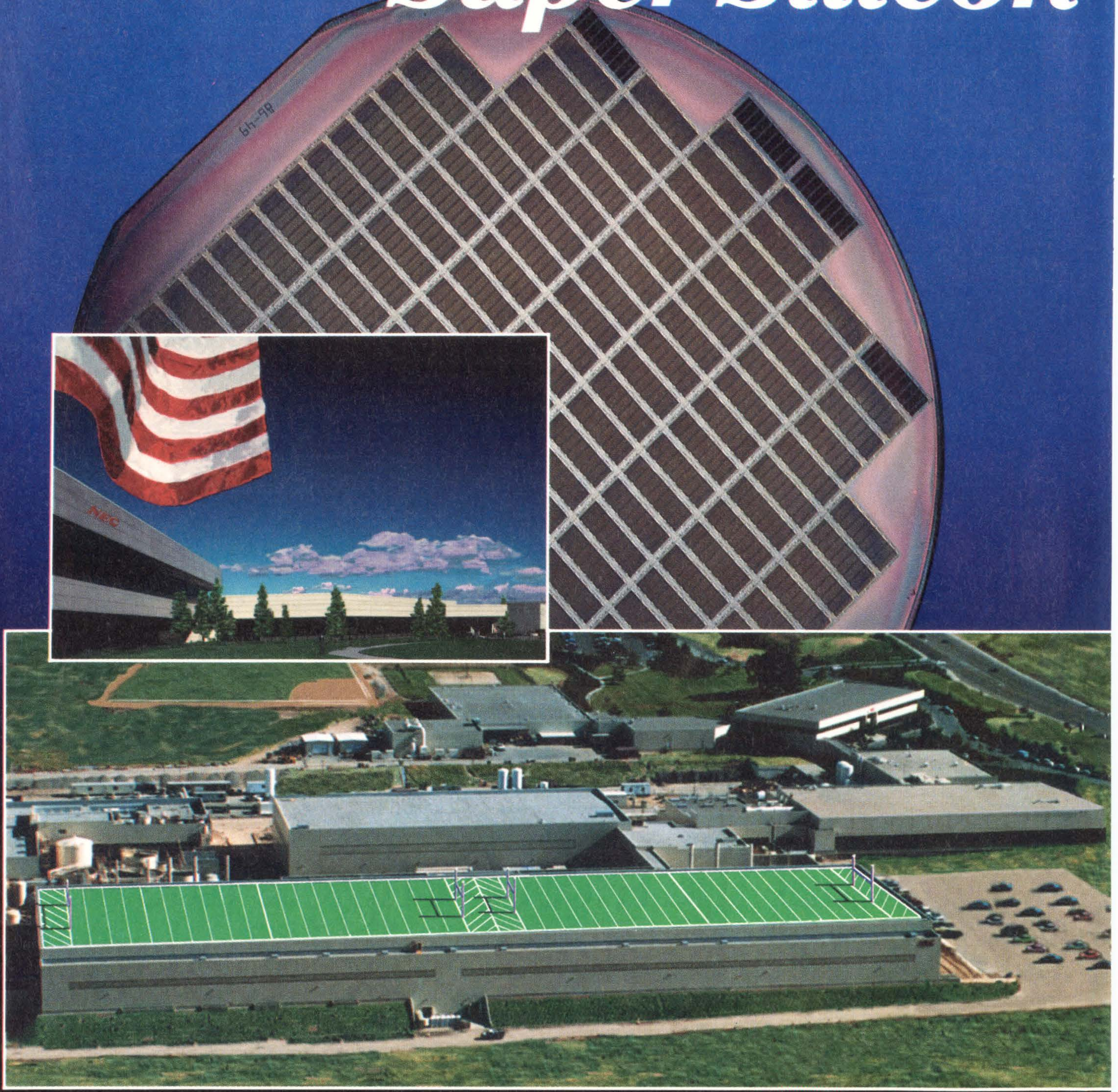

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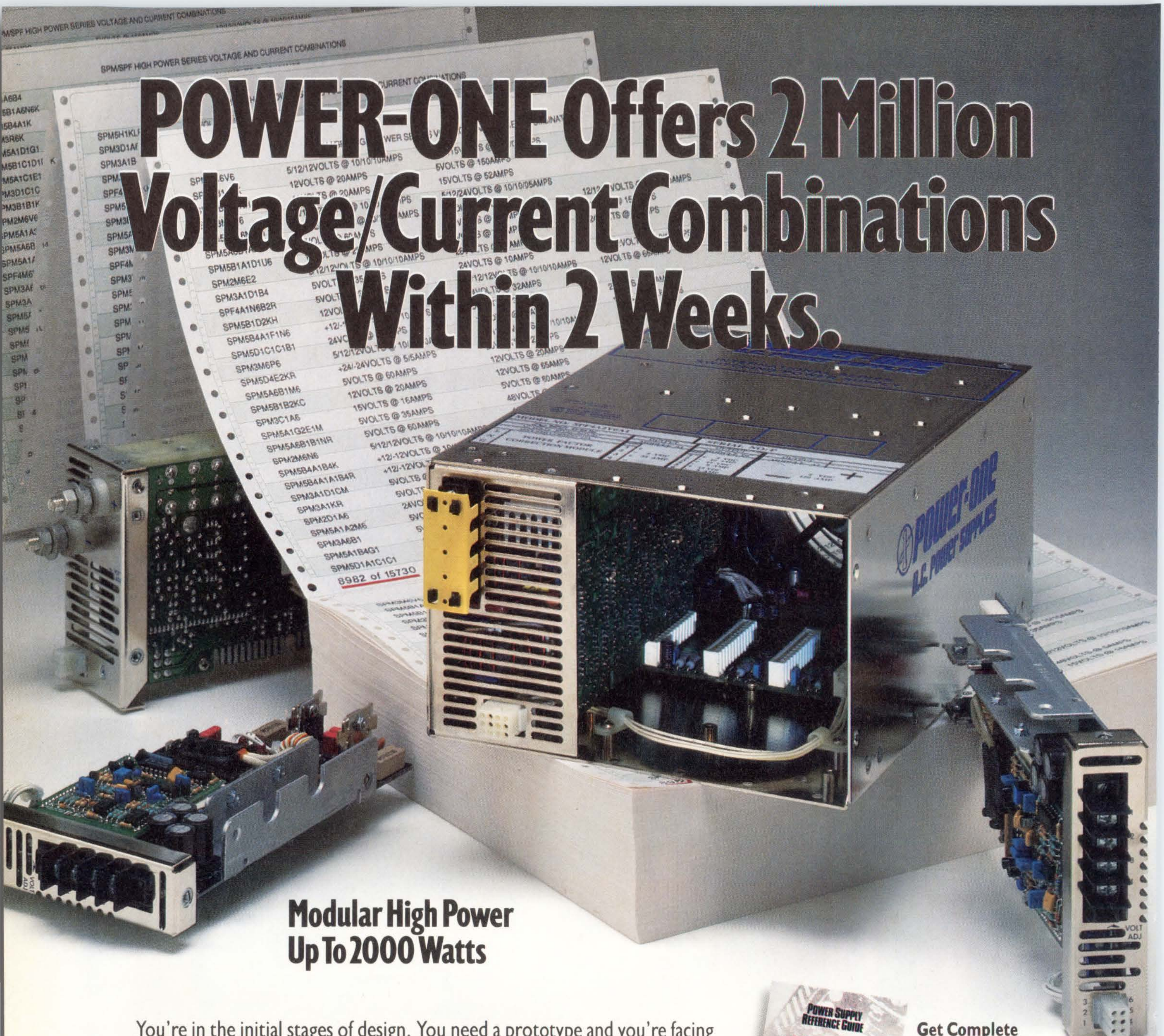

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Surface-mount sockets expand design options

TOM ORMOND, Senior Technical Editor

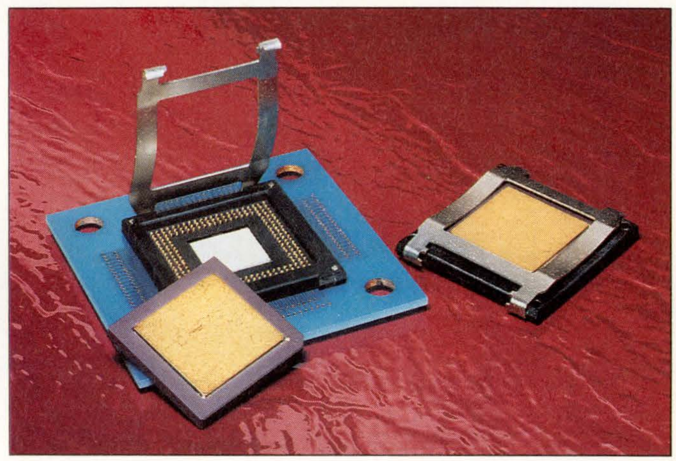
Surface-mount sockets ease package replacement and system expansion, protect ICs from temperature damage during soldering, and make test points readily available.

SMT-socket manufacturers are making pin geometries tighter to accommodate the latest generation of complex ICs. They're also using high-performance engineering plastics to let socket housings withstand harsh board soldering and cleaning, and have developed a class of solderless surface-mount sockets. Land-grid-array (LGA) sockets employ compression-mount techniques to provide the socket-to-board interface. The lack of hidden solder joints greatly eases inspecting and repairing or replacing such sockets.

Selecting an SMT socket means considering about half a dozen factors. Some of these factors—such as heat resistance, lead coplanarity, and mounting technology—are unique to surface-mount technology. Other factors such as size, solder-joint reliability, ease of assembly, and contact quality are not. However, these last factors are more critical in applications involving surface-mount sockets than those using through-hole sockets.

Conventional glass-filled polyesters are more than adequate for socket-housing service as long as the sockets are going to go through a wave-soldering system during board assembly. These materials cannot handle the rigors of IR or vapor-phase reflow soldering, the processes more common for SMT assembly. During wave soldering, only the leads are raised to a temperature that exceeds the solder's melting point; during reflow soldering, the entire socket assembly is heated.

Surface-mount sockets should be able to handle 230°C temperatures for at least 30 seconds and 260°C for 10 seconds in extreme cases. Deviating from these figures to any marked degree is a mistake. Extending the time spent above the solder melting point can damage the board as well as other sensitive components. Also, increasing the time or temperature can cause intermetallic compounds to form in the solder joint. These compounds can lead to premature solder-joint failure.



Designed specifically for Intel's 80386 μP, Cinch Connector's land-grid-array (LGA) socket interfaces the processor to a pc board without using solder.

Today, most surface-mount sockets use high-performance engineering plastics for the housing material. Polyphenylene sulfide (PPS), one of these plastics, is a high-strength thermoplastic compatible with surface-mount assembly operations. It has a heat-deflection temperature in excess of 260°F, good chemical resistance, and high dimensional stability—all key parameters for surface-mount sockets.

Lead coplanarity is a second consideration in surface-mount assembly

operations. The quest for flat pc boards faces all designers involved with surface-mount technology (SMT). Mirror-flat boards represent the ideal, but the physics of real-world materials is such that board warping and twisting is a fact of life.

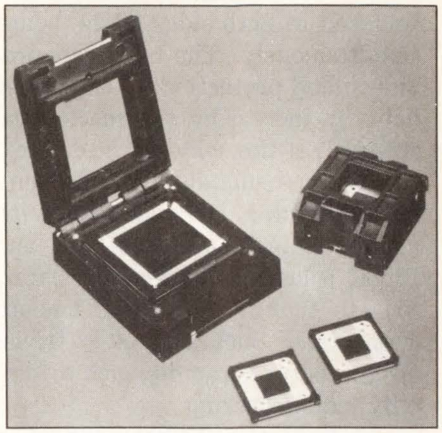
Through-hole sockets are forgiving of lead-length variations—you can always bend the leads enough to get them through the holes in the board. Not so with surface-mount sockets. Ideally, the tips of all the socket leads should lie on the same plane. Open solder joints can result if a single lead is significantly higher or lower than this plane. Unfortunately, you'll rarely find coplanarity specifications on data sheets. The best way to realize a successful design and minimize problems is to maintain stringent control of solder-paste application, component placement, and solder-reflow operations.

A socket's overall size is another important selection consideration. One of the prime reasons for going the SMT route in the first place is high packing density. If a socket housing a DIP device with row-to-row spacing of 0.3 in. measures 0.5 in. wide, the real-estate increase for using the socket is a significant 40%.

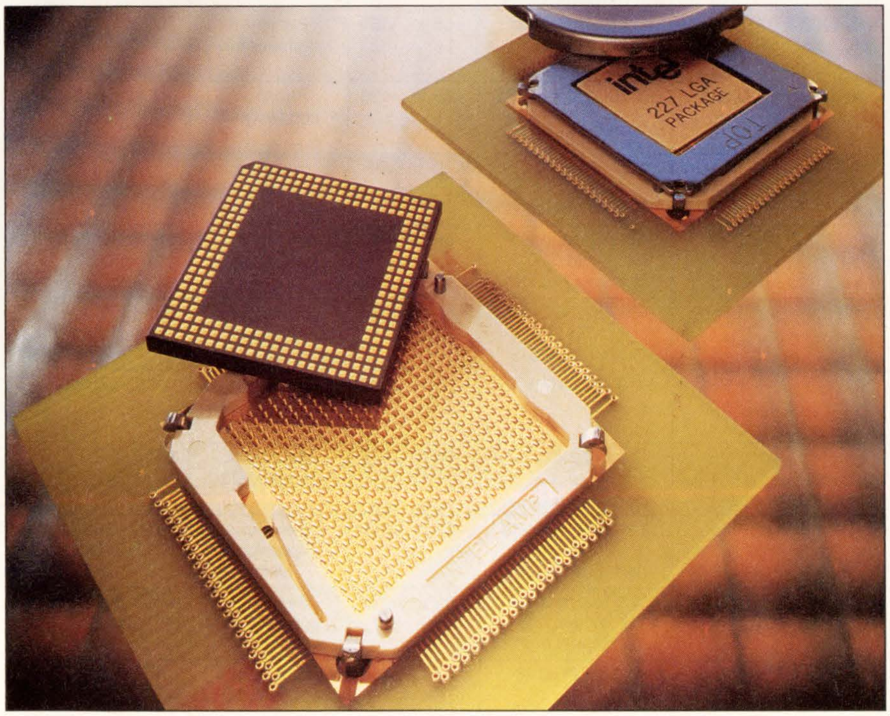
Some ICs are available in more than one surface-mount package. Your task is to select the package that is going to maximize socket packing density. Also consider socket height, especially in applications involving boards racked-mounted on 0.5-in. centers. SMT assemblies can have components mounted on both sides of the board, so you can't assume that a socket less than 0.5 in. high will cause no problems.

Solder joints can fail

In most cases, the weakest link in a surface-mount system is the solder joint between the lead and the board. This interface deserves special attention with sockets because these devices must accommodate extreme stress levels even in normal usage. In addition to lead coplanarity, lead configuration plays a major role in establishing solder-joint reliability.



Suitable for automated surface-mount assembly, Series 550/560 sockets from CTI Technologies meet all JEDEC specifications. The sockets have an open-body design, which maximizes air flow across the IC under test.



Featuring an above-board profile of 0.2 in., AMP's LGA socket assembly accommodates packages having as many as 484 pins spaced on a 0.05-in. centerline grid.

Designers have several lead-configuration options, including gull wing, J lead, and butt. The gull-wing option is the popular choice for reliability. Gull-wing leads can be formed on standard and fine pitches, have a low profile, and tend to self-align during soldering. Gull-wing leads are also easy to clean and can simplify solder-joint inspection. On the negative side of the ledger, gull-wing leads require more board space than the other types. As is the case in many areas of electronics, you have to make a tradeoff between solder-joint reliability and board packing density.

When it comes time to select surface-mount sockets, also keep assembly needs in mind. Several seemingly mundane socket features can greatly simplify manufacturing. For example, look for sockets whose body design exposes the lead-pad interface. Such a socket can simplify board cleaning and solder-joint inspection and also reduce the effects of IR shadowing.

Some sockets have locking clips that hold them to the board prior to soldering. This feature is especially useful in high-vibration assembly and when components are soldered to both sides of the board simultaneously. The clips can provide added protection for the solder joint by increasing the mechanical strength of the soldered interface.

If you're using automated assembly, consider DIP sockets with molded-in pick-and-place pads and PLCC (plastic leaded chip carrier) sockets that feature large smooth open areas. Such seemingly trivial design features can do much to simplify manufacturing.

The final point to consider when choosing SMT sockets is contact quality. **Table 1** lists some typical parameters for a representative sampling of surface-mount sockets. As you can see, most vendors employ beryllium copper or phosphor bronze as the contact material.

Beryllium copper contacts have the best spring characteristics over the widest temperature range (−65 to +125°C), so they are well suited for military and computer applications. Phosphor bronze contacts suit industrial applications; they feature good spring characteristics over a moderate temperature range—−65 to +105°C—and they're less expensive than beryllium copper contacts.

As the data in **Table 1** illustrate, surface-mount sockets accommodate a variety of IC package styles including DIPs, SOICs, LCCs, PLCCs, and PQFPs (plastic quad flatpacks). Most of the sockets in **Table 1** are designed to be soldered to the pc board. However, another class of surface-mount sockets is rapidly gaining popularity—the land-grid-array (LGA) socket, which employs compression-mount techniques to provide the socket-to-board interface.

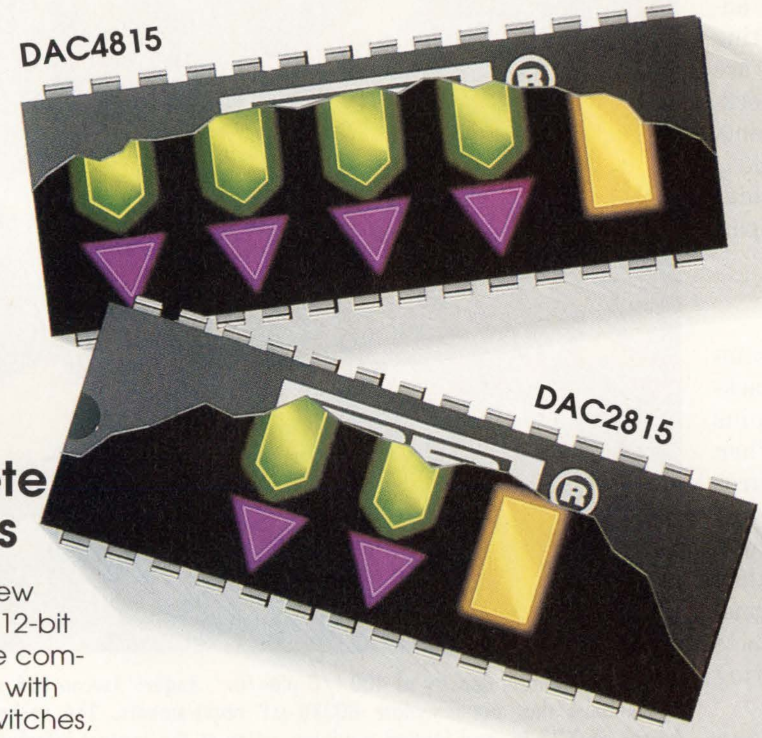
These sockets mechanically fasten to the pc board, usually with screws or plastic studs. A cover

Table 1—Representative surface-mount sockets

Manufacturer	Model	Type[1]	Pin count	Insulator[2]	Size (in.)	Operating range (°C)	Contact (material/plating)	Price
Advanced Interconnections	2819	PLCC	28, 44, 52, 68, 84, 100, 124	PPS	0.5×0.5×0.2 to 1.8×11.8×0.2	−60 to +220	Beryllium copper/tin lead	$16.38 for 68-pin unit
AMP Inc	Dip-lomate	DIP	8, 14, 16, 20, 24, 28, 40	PCT	0.395×0.394×0.21 to 1.995×0.694×0.21	−25 to +105	Phosphor bronze/tin or gold	$1.45 (1000) for 28-pin unit
Aries Electronics Inc	Series 518	DIP	6 through 64	PET	0.3×0.4×0.165 to 3.2×1×0.165	−30 to +140	Beryllium copper/gold	$0.46 to $0.81 for 14-pin unit
Augat Inc	PSU Series	PLCC	20, 28, 32, 44, 52, 68, 84	PPS	0.613×0.613×0.175 to 1.413×1.413×0.175	−55 to +105	Beryllium copper/gold	$2.34 (1000) for 68-pin unit
CTI Technologies Inc	550/560 Series	PLCC	128, 168, 192, 248, 256, 328	PPS	1.89×1.5×0.92 to 2.84×2.31×1.02	−55 to +150	Beryllium copper/gold	$56.36 (250) for 128-pin unit
Emulation Technology Inc	SOR/SOL Series	SOIC	8, 14, 16, 20, 24, 28	Ultem	0.275×0.425×0.225 to 0.79×0.525×0.26	−55 to +125	Beryllium copper/gold	From $4.80
Hirose Electric USA Inc	DL3 Series	SOIC	28, 32	PPS	0.59×0.957×0.196 to 0.59×1.05×0.196	−55 to +85	Phosphor bronze/tin lead	$4.07 for 32-pin unit
Kycon Inc Cable & Connector	SMP Series	PLCC	20, 28, 32, 44, 52, 68, 84	PPS	0.62×0.62×0.177 to 1.42×1.42×0.177	−55 to +125	Phosphor bronze/tin	$1.68 (1000) for 32-pin unit
McKenzie Technology	ADP Series	PLCC	44, 52, 68, 84	PPS	0.665×0.665×0.282 to 1.17×1.17×0.282	Not specified	Phosphor bronze/gold	$15 (500) for a 68-pin unit
Methode Electronics Inc	Low profile SM	PLCC	32	PPS	0.7×0.8×0.15	−50 to +125	Beryllium copper/tin lead	$1.33 (10,000)
Mill-Max Manufacturing Corp	Series 110	DIP	4 through 64	PPS	0.4×0.2×0.22 to 1×3.2×0.22	−50 to +150	Beryllium copper/gold	$0.73 (2500) for 20-pin unit
Nepenthe	NEP Series	LCC	32, 44	Ryton	0.612×0.713×0.213 to 0.813×0.813×0.23	−65 to +200	Beryllium copper/gold or tin	$3.22 (1000) for 32-pin unit
Samtec Inc	ICF Series	DIP	8 through 48	LCP	0.375×0.8×0.195 to 0.675×4.8×0.195	−65 to +125	Beryllium copper/gold	From $0.11 per pin
3M Co	Type B	LCC	68	PPS	1.21×1.21×0.36	−55 to +105	Beryllium copper/gold	$6.78 (5000)

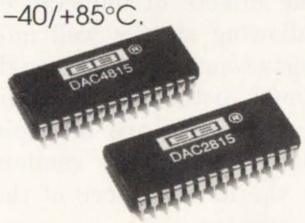
Notes: 1. LCC=Leadless chip carrier; PLCC=plastic leaded chip carrier.
2. LCP=Liquid-crystal polymer; PCT=polycyclohexane terephthalate; PET=polyethylene terephthalate; PPS=polyphenylene sulfide.

New Family of 12-Bit Dual and Quad DACs



Complete Solutions

Burr-Brown's new generation of 12-bit multi-DACs are complete solutions with CMOS logic switches, high performance buried-zener reference, and low-noise bipolar output amplifiers in cost-saving plastic packages. All are fully specified and monotonic over the extended industrial temp range of –40/+85°C.



Save Space, Cut Costs

You save space and money with these complete, compact multi-DACs. They're ideal for applications requiring more than one DAC…ATE pin drivers, medical diagnostic and lab instrumentation, industrial control, and general purpose circuits.

Interface Options

Choose a high speed serial interface (10MHz clock) or a 2-byte (8+4) double-buffered interface. All models feature an asynchronous CLEAR control for power-on-reset or system calibration purposes.

Free Samples, Selection Guide

Sample the best DAC for your application. And, ask for a copy of our *High Performance D/A Converters* guide with key specs, performance diagrams, and applications information on our newest DACs. Just contact your local Burr-Brown sales office, or call for immediate assistance, **1-800-548-6132.**

Model	Function	Digital Interface	Output Range
DAC2814	Dual	Serial Port	–10V to +10V, 0 to +10V, 0 to –10V
DAC2815	Dual	8-bit Port	–10V to +10V, 0 to +10V, 0 to –10V
DAC4814	Quad	Serial Port	–10V to +10V, 0 to +10V, 0 to –10V
DAC4815	Quad	8-bit Port	–10V to +10V

Duals from $16.95. Quads from $24.95. *U.S. OEM prices, in 100s.*

Burr-Brown Corp.
P.O. Box 11400
Tucson, AZ 85734

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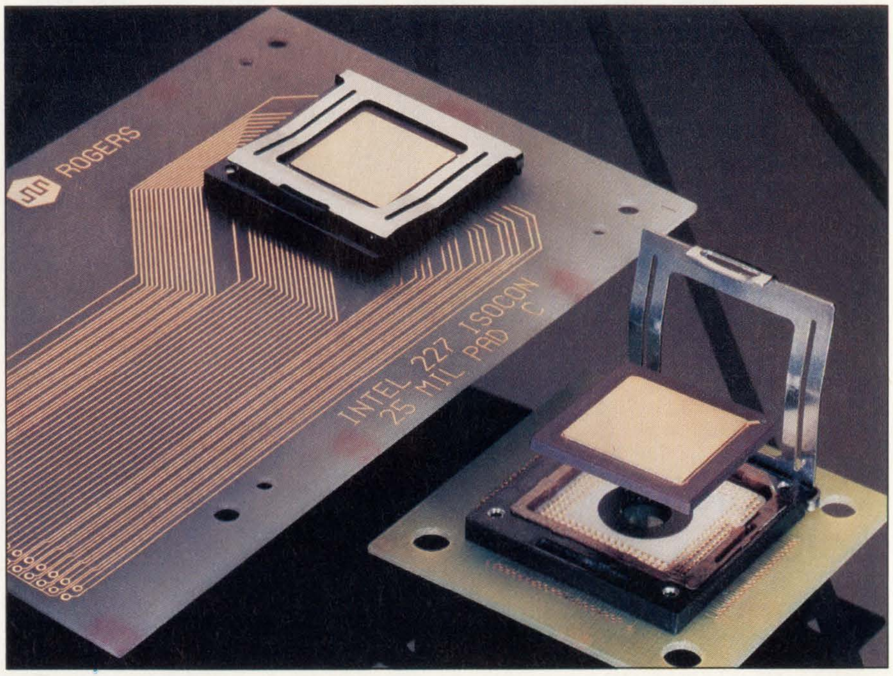
CIRCLE NO. 33

SURFACE-MOUNT SOCKETS

plate clamps down the IC. The advantages of compression mounting as opposed to solder mounting are twofold. Compression-mount sockets result in no hidden solder joints and are easier to replace should a repair be necessary. With solder connections, inspection and repair tasks are almost impossible.



Offering a contact density of 400 I/O pins/in.^{2}, Rogers' Isocon LGA sockets are available in versions that accommodate 80386-µP requirements. The sockets have a mounted height of 0.23 in. and feature a wiping action at the contact interface.

Solderless sockets

The Ampflat LGA socket assembly from AMP accommodates packages with as many as 484 pins spaced on 0.05-in. centers. When mounted, the assembly measures 0.2 in. above the board. The contact array is 0.009-in. high when fully compressed and provides less than 10-psec delay and 200°C/W thermal resistance per contact. The contacts provide 0.006 in. of wipe during mating.

The socket assembly comprises a heat clamp/pressure plate, a chip-carrier nest that holds the LGA package, the contact array, and an insulator/spacer, all of which are sandwiched between a cover plate and a base plate. The thickness of the insulator corresponds to the thickness of the pc board for a given assembly. Thus, the resultant thickness of the assembly yields the required normal force under compression.

The clamping cover of the assembly is a single piece that you can install and remove with an ordinary screwdriver. Both the top and bottom plates are made of stainless steel. The bottom plate insulator is assembled with adhesive on its top and bottom surfaces so that the bottom plate is permanently attached to the pc board after initial socket assembly. The socket transfers heat from the carrier package to the pc board.

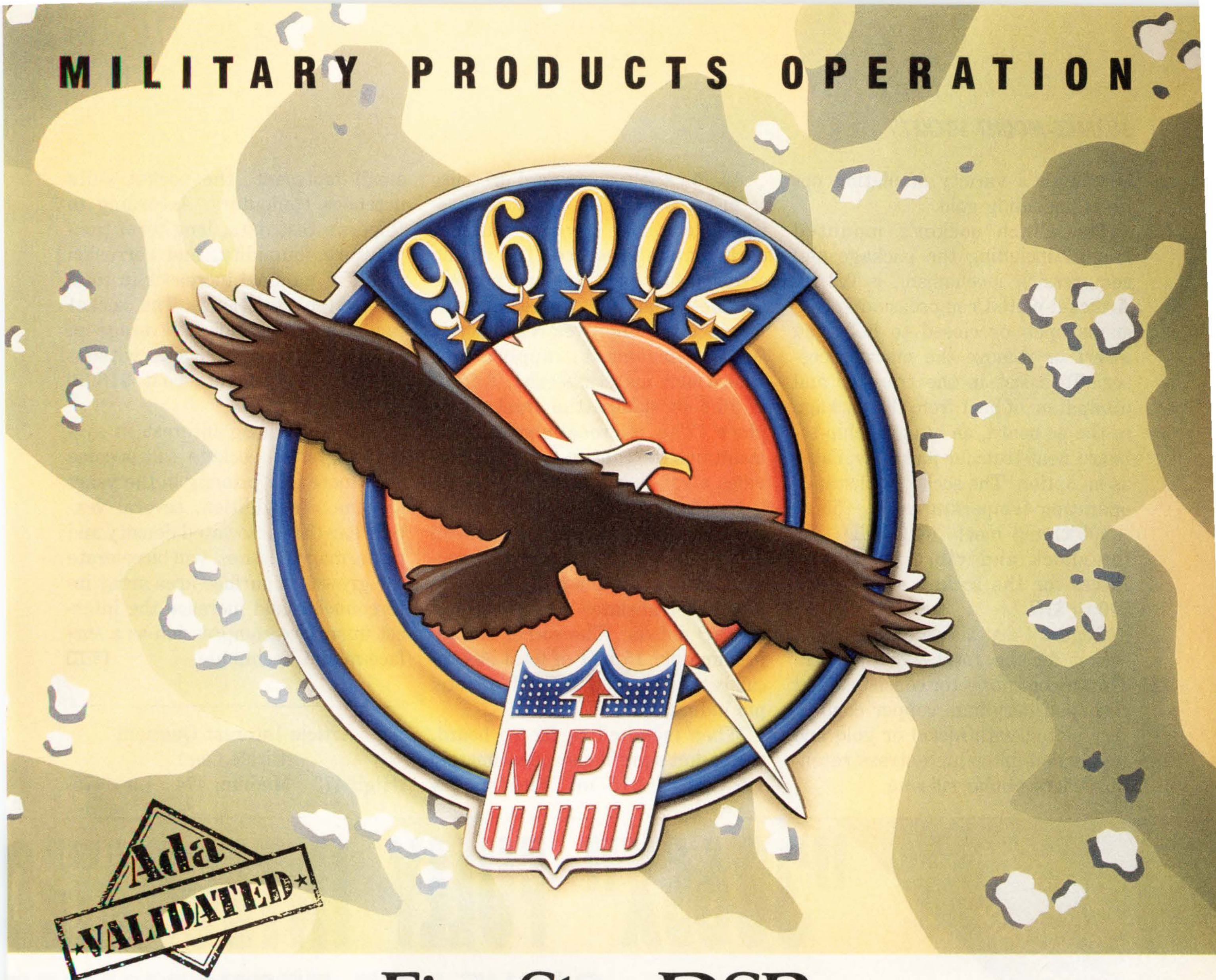
At $20 to $26, the Ampflat socket assembly is an economical interconnect device. The devices feature easy field replacement of the chip without special tools, low-cost replacement of the contact array, and the choice of gold or tin contact interfaces.

Cinch has developed an LGA socket specifically for the Intel 80386 µP. You attach the socket to the board with conventional mounting hardware or with plastic studs that are an integral part of the socket body. The socket is available in two sizes: one uses the Intel-recommended mounting footprint; the second has a smaller footprint for applications in which board space is at a premium.

The socket's button contacts are single strands of randomly bent wire that resemble cylindrical Brillo pads. The nature of the wire formation yields a number of mechanical and electrical advantages. Mechanically, the wire structure comprises many spring segments, all of which share the stress of the contacts' deflection during mating cycles. The random structure also provides redundant points of contact at the mating surface. Compressing the button contact axially causes the spring segments to move laterally at the mating surface. This motion results in a wiping action, which improves the reliability of the contact.

Electrically, the nature of the wire formation creates a structure particularly well suited for transmitting high-speed signals. Unlike a coil spring, the random structure cancels the effects of inductance, thereby allowing signals well into the gigahertz range to pass through with minimal distortion. In addition, because there are multiple contact points within the random structure, the dc resistance of the contact is very low.

The button contacts are available in two diameters—0.04 in. for placement on straight or staggered patterns in which the spacing between contacts is 0.075 in. or greater, and 0.02 in. for placement on patterns with spacings of 0.04 in. or greater. The contacts come in a variety of materials and can accommodate a range of applications in which temperature ranges from 200°C down to the cryogenic temperature of liquid nitrogen. The contacts are avail-



Five Star DSP

DSPs don't come any better than Motorola's high-performance Military 96002. It's our premier 96-bit floating-point digital signal processor, ideally suited for array processing and intense digital signal processor applications such as radar and communications.

Electrical samples of this single-chip, dual-port, low-power HCMOS general purpose IEEE DSP will be available third quarter 1991, with the MIL-STD-833 and SMD versions slated for introduction in early 1992.

Ada Supported

Motorola understands the unique demands placed upon Military systems and works closely with software vendors to ensure that its products are fully supported.

Now Available

Available *now* in the "Pin Grid Array" (PGA) and "Ceramic Leaded Chip Carrier" (CLCC) is the Military 56001 HCMOS, low power, general purpose DSP in full MIL-883 and SMD versions. For price and delivery information and Brochure #BR912/D, contact your local sales office.

For more information on the 96002, order our DSP Brochure #BR1402/D by calling toll-free 1-800-441-2447.

Or complete and return the coupon below to Motorola, P.O. Box 20912, Phoenix, AZ 85036.

Malcolm Baldrige National Quality Award Winner 1988

To: Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036

Please send me Motorola's DSP Brochure # BR1402/D.

507EDN012092

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Company ________________

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MOTOROLA

able with a variety of plating options, including gold.

The Cinch socket's mounted height, including the package and compression mechanism, is 0.2 in. A nickel-plated compression spring snaps open or closed to help you insert or remove the microprocessor. To assist in the transfer and dissipation of heat from the package to the pc board, an integral chip-to-board heat-transfer pad is available as an option. The socket withstands operating temperatures of −55 to +100°C and meets MIL-STD 1344 for shock and vibration levels. Prices for the sockets range from $10 to $15.

Rogers Corp also offers an LGA socket for the Intel 80386 SL μP. The Isocon connector consists of flat S-shaped beryllium copper conductors plated with nickel or gold and suspended in a high-stress-retention microcellular silicone.

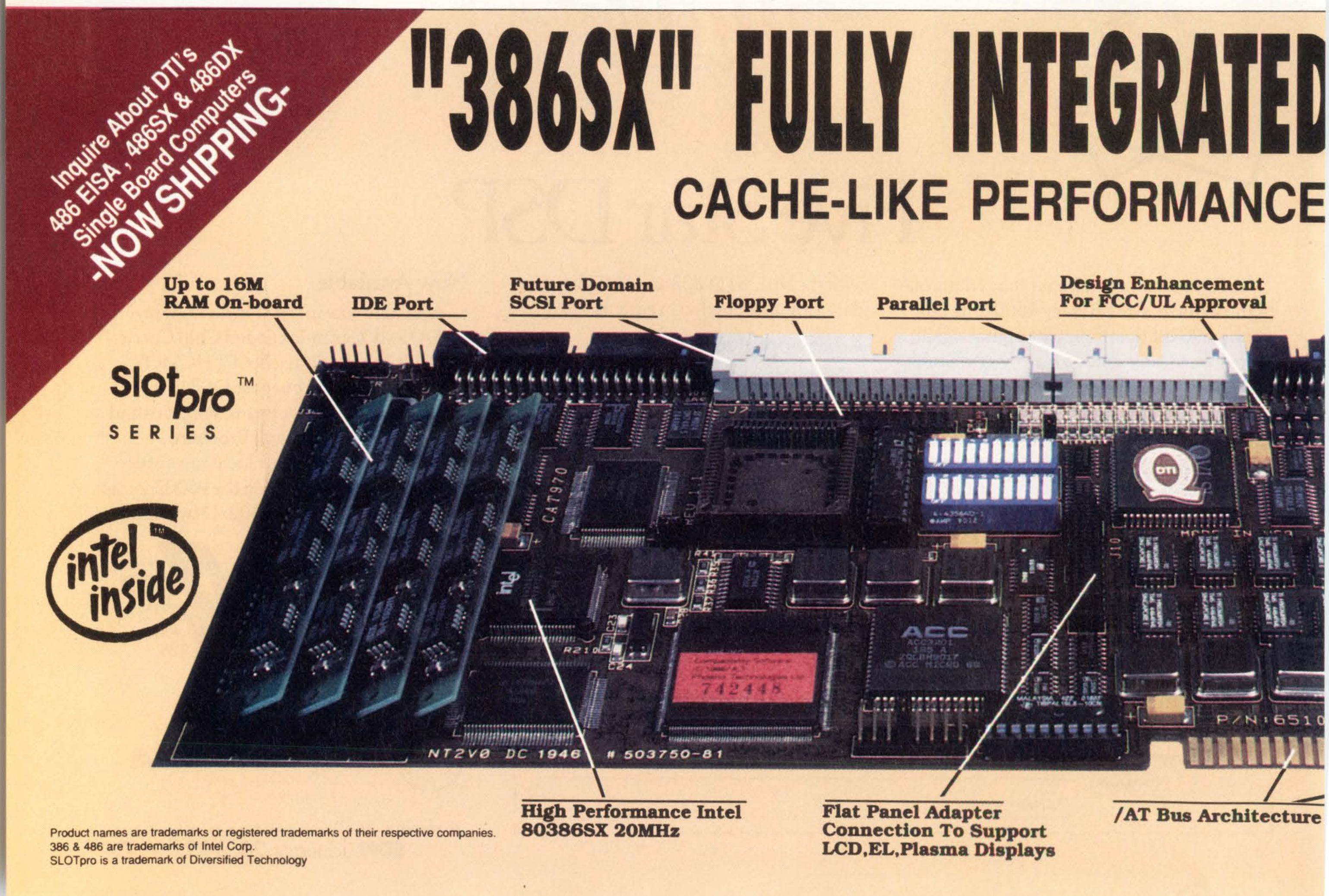
As you apply downward pressure to insert a chip, the conductors rotate and provide a wiping action at each contact interface. The wiping scrapes dust particles and nonconductive oxides from the contact surfaces, which improves reliability in field-replacement applications where such materials exist. A force of 15.6 lb clamps the Intel μP in place. The microcellular silicone maintains the contact force and provides a gas-tight seal.

Key features of the Isocon socket include conductor pitches between 0.1 and 0.05 in. and variable conductor location within a grid. The 0.05-in. pitch translates to a density of 400 I/O pins/in^2. The socket has approximately 15 mΩ of total electrical resistance and 0.5 nH of total pin inductance.

When mounted to the pc board, the socket's profile is approximately $1.6 \times 1.6 \times 0.215$ in. With such a small footprint, the socket suits notebook computers. According to Rogers's test data, long-term temperature, humidity, and corrosion result in minimal increases in total connection resistance. The socket can also withstand an average of 10,000 mate-unmate cycles without failure. The sockets cost $16.90 (1000).

With increasing interest in system upgrades, sockets will become even more of a priority in the years to come. In addition, several venders say that associated density and performance issues will accelerate the growth of surface-area array interconnects and increase the interest in surface compression as a surface-mount technique. EDN

Article Interest Quotient
(Circle One)
High 473 Medium 474 Low 475



For more information . . .

For more information on the surface-mount IC sockets discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

Advanced Interconnections
Box 1342
West Warwick, RI 02893
(401) 823-5200
FAX (401) 823-8723
Circle No. 700

AMP Inc
Box 3608
Harrisburg, PA 17105
(800) 522-6752
Circle No. 701

Aries Electronics Inc
Box 130
Frenchtown, NJ 08825
(908) 996-6841
FAX (908) 996-3891
Circle No. 702

Augat Inc
Interconnection Products Div
Box 779
Attleboro, MA 02703
(508) 222-2202
FAX (508) 222-0693
Circle No. 703

Cinch Connectors
1500 Morse Ave
Elk Grove Village, IL 60007
(708) 981-6000
FAX (708) 981-4266
Circle No. 704

CTI Technologies Inc
7855 E Evans Rd
Suite A
Scottsdale, AZ 85260
(602) 998-1484
FAX (602) 483-2731
Circle No. 705

Emulation Technology Inc
2344 Walsh Ave
Bldg F
Santa Clara, CA 95051
(408) 982-0660
FAX (408) 982-0664
Circle No. 706

Hirose Electric USA Inc
2685-C Park Center Dr
Simi Valley, CA 93065
(805) 522-7958
FAX (805) 522-3217
Circle No. 707

Kycon Cable & Connector Inc
1772 Little Orchard St
San Jose, CA 95125
(408) 295-1110
FAX (408) 295-8054
Circle No. 708

McKenzie Technology
44370 Old Warm Springs Blvd
Fremont, CA 94538
(510) 651-2700
FAX (510) 651-1020
Circle No. 709

Methode Electronics Inc
Interconnect Products Div
1700 Hicks Rd
Rolling Meadows, IL 60008
(708) 392-3500
FAX (708) 392-9404
Circle No. 710

Mill-Max Manufacturing Corp
Box 300
Oyster Bay, NY 11771
(516) 922-6000
FAX (516) 922-9253
Circle No. 711

Nepenthe
2479 E Bayshore Rd
Suite 800
Palo Alto, CA 94303
(415) 496-6666
FAX (415) 856-8650
Circle No. 712

Rogers Corp
Circuit Components Div
2400 S Roosevelt St
Tempe, AZ 85282
(602) 967-0624
FAX (602) 967-9385
Circle No. 713

Samtec Inc
Box 1147
New Albany, IN 47150
(812) 944-6733
FAX (812) 948-5047
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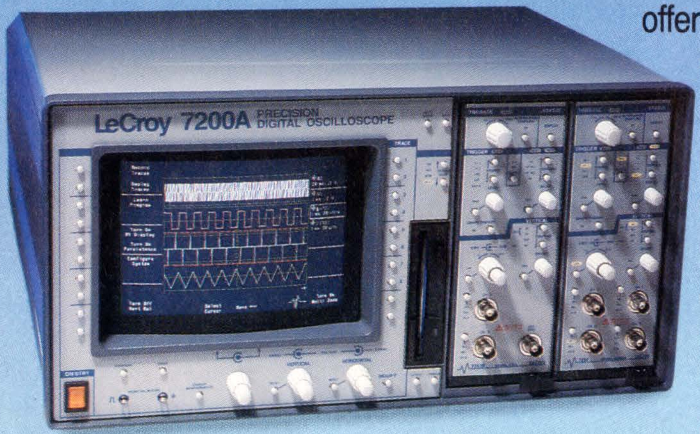
Circle No. 715

We Increased The Memory To One Megaword, So You Can Increase The Bandwidth.

LeCroy's one megaword acquisition memory means higher sampling rates over most time base settings. The results: greater useable bandwidth and increased aliasing protection. *These are the kind of facts the competition can no longer ignore...or match.*

Whether you choose our new 300 MHz 9300 Series or the 2 GS/sec 7200A Series, both offer you the world's longest memories and are available in 2 and 4 channel configurations.



The new 7200A Series, our high performance line with high resolution color display, features 500 MHz bandwidth at 2 GS/s with 200k memory standard and 1 Meg/channel optional. Modular architecture allows the user to choose 2, 4 or even 8 channels, all with super-long memory. Floppy and hard disk drives are standard features.

LeCroy DSOs offer the best displays in the business: bigger – crisper – more pixels, and now – color! These large, bright, easy-to-view displays eliminate text and signal overlap and, at the same time, allow multiple grids for simultaneous viewing of traces and their expansions.

Equally impressive is the fact that LeCroy DSOs give you answers, not just data. And the reasons are simple: LeCroy DSOs incorporate massive multiprocessor power, resulting in live-updating waveform parameters, time zooming, frequency analysis (FFT), fast averaging, arithmetic, histogramming, and PASS/FAIL testing. All this...over multiple

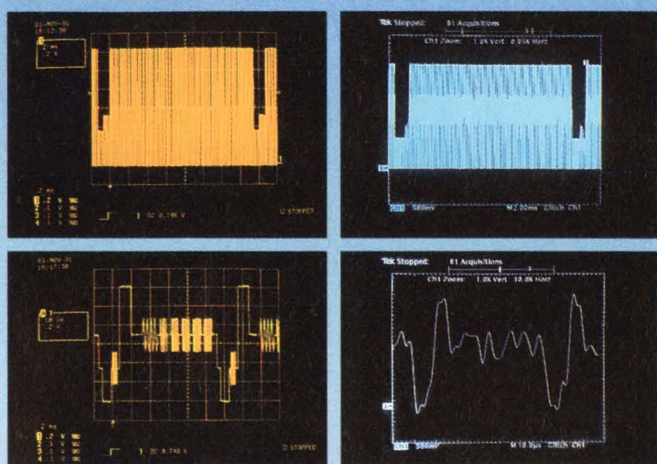
Taking DSO Memor

channels simultaneously and...without ever losing precious source data.

PC compatibility is yet another LeCroy advantage. Whether you're using memory cards (9300 Series), or floppies (7200A Series), you can dump your waveforms and other data directly into your PC or word processor, or personalize your instrument for your dedicated measurements.

The new 9300 Series offers 300 MHz bandwidth and 100 MS/s per channel, with memories from 10k to 1 Meg/channel. All versions feature DOS compatible memory cards and automatic PASS/FAIL testing. Prices start below $5,000.

LeCroy **Competition**



In many applications, there's no substitute for a really long memory. The screens above show a complete TV field captured at 2 ms per division. The benefits of the long memory are shown when the waveform is expanded to view a single TV line.

For a copy of our new information guide, or a demonstration of LeCroy digital oscilloscopes, call 1-800-5-LeCroy; fax (914) 578-5985.

LeCroy Corporation – Dept. A
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Chestnut Ridge, NY 10977-6499

CIRCLE NO. 35

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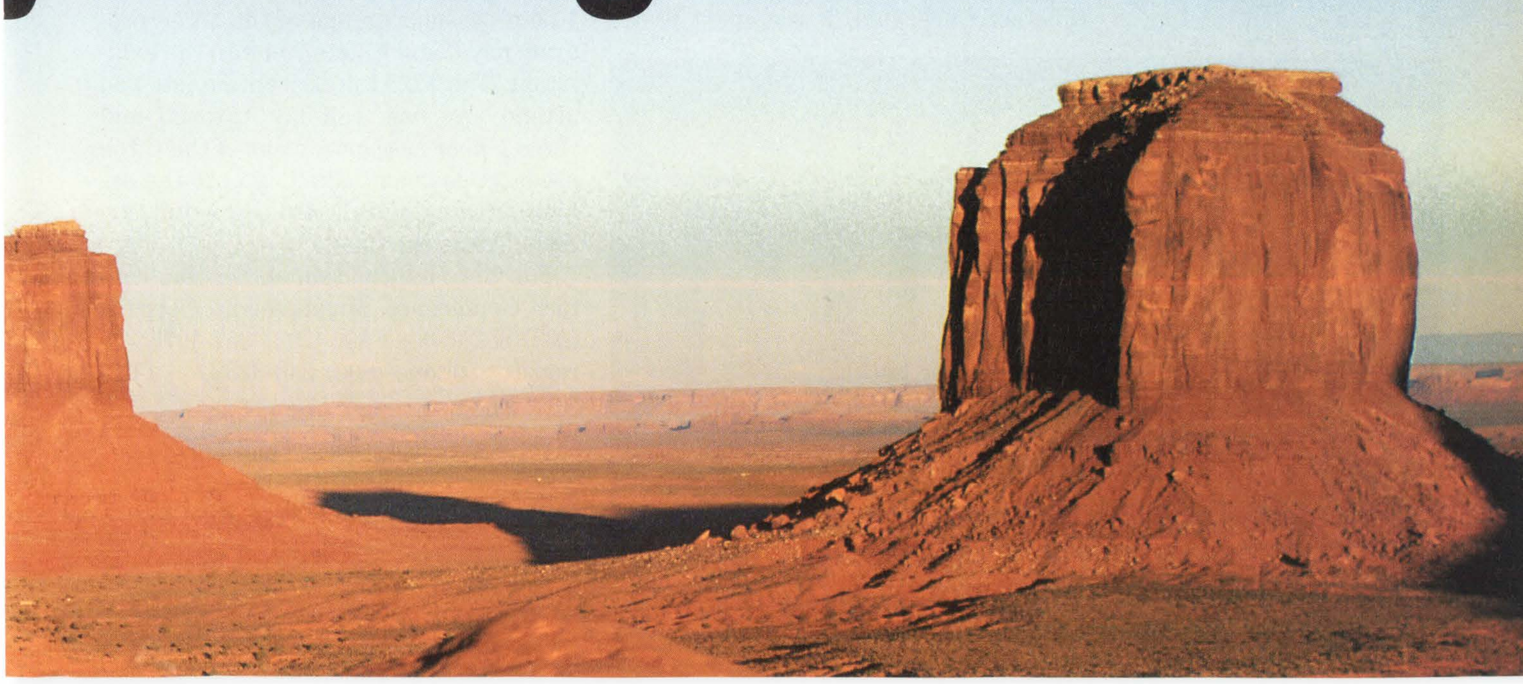
The Digital Scope Specialists

y To A Higher Plane.



Buscon beefs up technical program

JULIE ANNE SCHOFIELD, Associate Editor

Buscon West now features more than 60 technical sessions and tutorials.

This year's Buscon West features a much-expanded technical program and more than 100 exhibitors showing their latest products. The show will be held from Tuesday, February 4, to Thursday, February 6, at the Long Beach, CA, Convention Center.

As with last year's Buscon West, an all-day Futurebus+ workshop will be held Monday, February 3—the day before the official opening of the show. The session will present a complete engineering discussion of the architectural and protocol design concepts behind Futurebus+, the physics of backplane transmission, a study of bus acquisition (arbitration and allocation), the parallel protocol, cache coherency, and message passing.

The rest of the technical program comprises 3-hour tutorials and 1-hour lectures. The tutorial topics are the Sbus, the VMEbus and VME64 (a proposed addition to the VMEbus spec), Multibus enhancements, the Micro Channel Architecture, LAN communications strategies, and the Scalable Coherent Interface (SCI) high-speed bus architecture. Lecture topics include the major bus architectures, CPUs, real-time software, and development issues of concern to designers working with backplane buses.

More than 100 exhibitors will occupy 30,000 square feet of floor space. These exhibitors will show off the latest bus technology, boards, components, systems software, and development tools. Exhibit-hall hours are 10 am to 6 pm Tuesday and Wednesday and 10 am to 4 pm on Thursday.

Your Buscon badge will get you into the Buscon Bash, which organizers herald as the "Mother of All Industry Parties." The Bash will happen Wednesday, February 5, from 5:30 to 7 pm.

You can register for Buscon in several ways. Passport #1 costs $695 and lets you attend the preconference Futurebus+ workshop as well as any of the sessions and half-day tutorials on all three program days. You'll also get a copy of the official conference proceedings and admission to the exhibition and the Buscon Bash. Passport #2, $545, doesn't gain you admission to the Futurebus+ workshop but otherwise allows you the same privileges as passport #1.

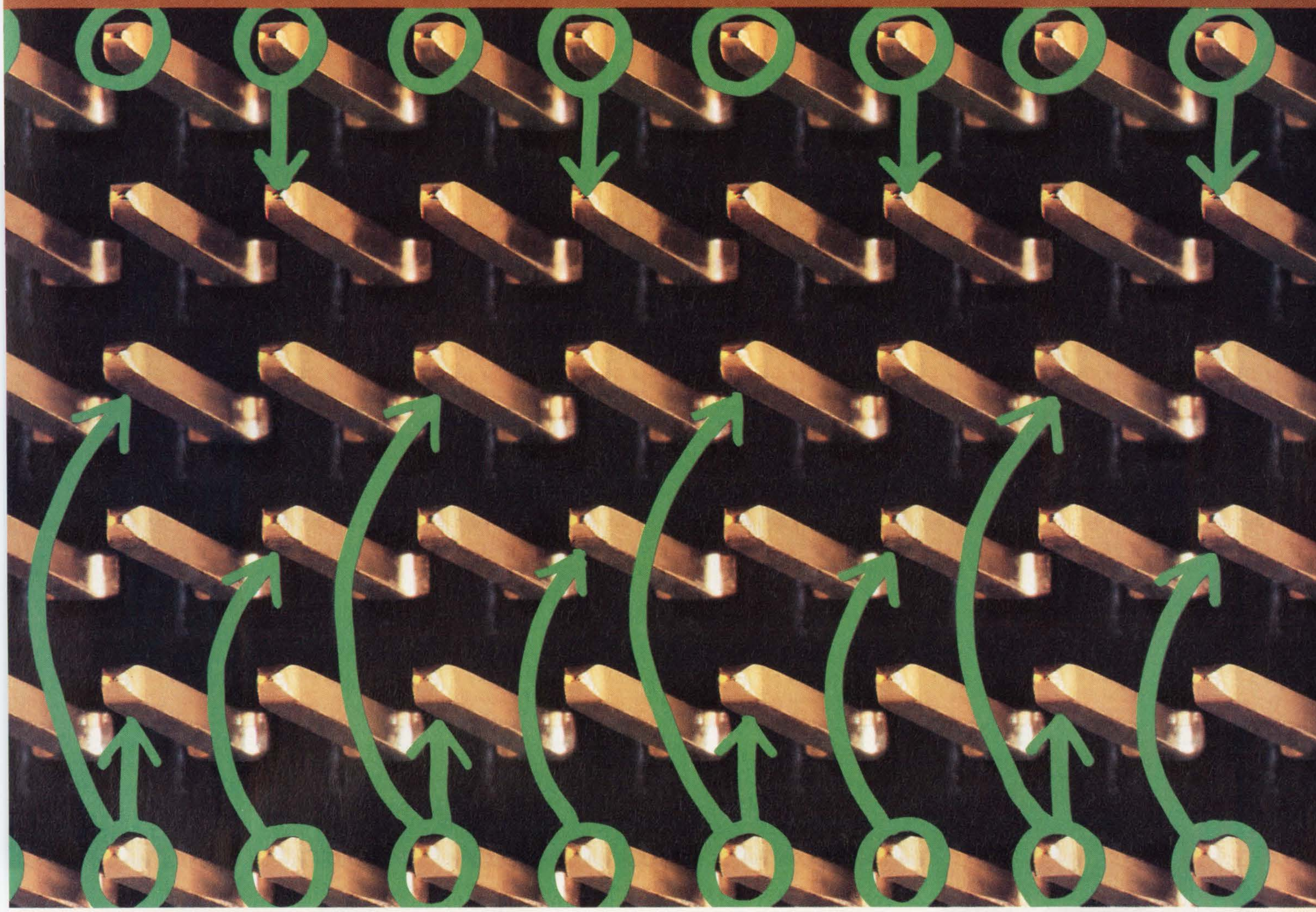
The $145 half-day option lets you attend one half-day tutorial or any four 1-hour sessions on one of the three program days, and it gets you into the exhibition. The $225 full-day option lets you attend any one half-day tutorial and three 1-hour sessions on one of the three program days and admits you to the exhibition. Registering for the exhibition costs $10 at the door.

For more information on Buscon, contact Conference Management Corp at (203) 852-0500; FAX (203) 857-4075. To register, phone (800) 243-3238. EDN

Article Interest Quotient
(Circle One)
High 470 Medium 471 Low 472

Table 1—Buscon/West '92 program schedule

Day	8:30 to 9:30 am	9:45 to 10:45 am	11 am to 12 pm	12:15 to 1:15 pm	2:45 to 3:45 pm	4 to 5 pm	5:15 to 6:15 pm
Mon Feb 3	**PCW** Preconference Futurebus+ workshop 8:30 am to 6 pm						
Tues Feb 4	**101** Technical aspects of SBus 8:30 am to 12:30 pm				**501** Factors in choosing external buses for high-speed data capture and processing	**601** Bus-interface solutions utilizing fine-pitch SMT packages and advanced semiconductor processes	**701** Bridging Futurebus+ I/O to high-performance multiprocessor systems
	102 VME64 and VMEbus 8:30 am to 12:30 pm				**502** Imaging and graphics—the technologies combined	**602** VXIbus in high-performance data-acquisition applications	**702** Design and integration of mixed-bus systems on high-performance HP-UX W/S
	103 SCSI-2 on the SPARCstation SBus	**201** Overwhelming case for a single-piece thermal plane for conduction-cooled models	**301** Futurebus+ implementations	**401** Mezzanine bus implementation in full military specification boards	**503** Live insertion in Futurebus+ design	**603** Graphical interfaces in real-time programming	**703** Implementing a SCSI LAN protocol: SCSINet
	104 Multiple DOS processors for industrial control	**202** SCSI design—A chip perspective	**302** Software development, testing, and integration issues for real-time multitasking systems	**402** Overcoming "Gotchas" in VMEbus multiprocessor design	**504** Frequency-domain filtering and 2-D FFT image processing	**604** Trident, 3-pronged attack on VMEbus system bottlenecks	**704** Considerations for remote device drivers in a real-time environment
Wed Feb 5	**801** Enhancements to Multibus 8:30 am to 12:30 pm				**1201** An integrated Ada environment for the '90s	**1301** Advanced hardware process synchronization primitives for VMEbus systems	**1401** Developing control applications without programming
	802 Micro Channel Architecture 8:30 am to 12:30 pm				**1202** Upcoming multiprocessing support in Unix System V	**1302** Open Boot/Forth	**1402** High-performance DSP-based image classifier
	803 Unix vs kernels for real time	**901** Using Windows DDE to provide GUI for real-time VMEbus applications	**1001** Designing for worst case: The impact of real-time O/S performance on real-world embedded systems	**1101** Utilizing a new standard: EISA-based PCXI vs VXI for testing	**1203** Strategies for testing and monitoring VMEbus systems	**1303** The I/O bus in Futurebus+	**1403** Token Ring networking
	804 SSBLT—The next VME performance push	**902** Chip vs board vs software decisions on Futurebus+	**1002** Busless computing environment	**1102** Bus analyzers solve system-development needs	**1204** Benchmarking real-time systems	**1304** Closely coupled UNIX in real-time systems	**1404** Advanced networking
Thurs Feb 6	**1501** Communications strategies 8:30 am to 12:30 pm				**1901** Porting RTOS to the MIPS R3000	**2001** Real-time RISC factors	**2101** VMEbus and computer automation
	1502 SCI (Scalable Coherent Interface) 8:30 am to 12:30 pm				**1902** Serial channel extends VMEbus, adding additional 400 Mbyte/sec transfers	**2002** High-speed serial communications and WANs	**2102** Practical considerations in the implementation of VME64
	1503 Futurebus+/VME bridge	**1601** FDDI gives bus-based systems new opportunities	**1701** DRAM control in high-performance systems	**1801** Designing FDDI adapter cards	**1903** Embedded firmware using hierarchies of message-driven state machines	**2003** Distributed micro-kernel technology in a real-time Unix environment	**2103** Futurebus+ electrical considerations for high performance
	1504 A real-time multiprocessor interface using the buffered pipe protocol	**1602** A comparative anatomy of RISC processors for real time	**1702** P1212.1: IEEE standard for using shared memory	**1802** Architectural and performance considerations of SCSI-2 peripheral interfaces, controllers, and I/O boards	**1904** DSP + processor technology—optimized for mixed media	**2004** Hard metric mezzanine board standard	**2104** Futurebus+ from a perch in Texas

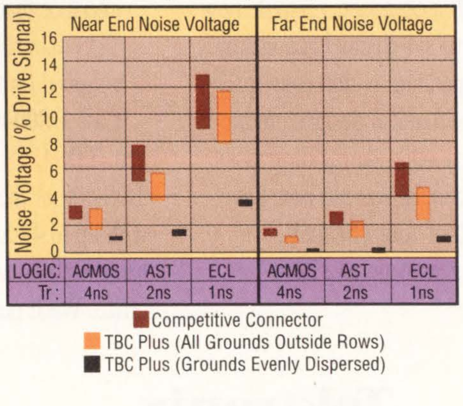


AMP TBC Plus connectors give you complete freedom in ground and signal assignment, so you can write your own 'ground rules' for outstanding electrical performance in high-speed, high-density backplane applications.

Because they are true 6-row connectors and you assign ground where you need it, near end and far end noise voltage figures in the <10 ns risetime range are far below connectors that limit ground to the outer rows or 'planes' (TBC Plus performance is even better when configured the same way!).

Our economical twin-beam receptacle design is unique in offering greatly reduced inductance in the outermost 'long' row of pins, and matched propagation delay in all lines.

Note performance of AMP TBC Plus connectors with evenly dispersed 'checkerboard' grounding: some competitive styles don't allow this.



Capacitance is a mere 2pf, max, line-to-line.

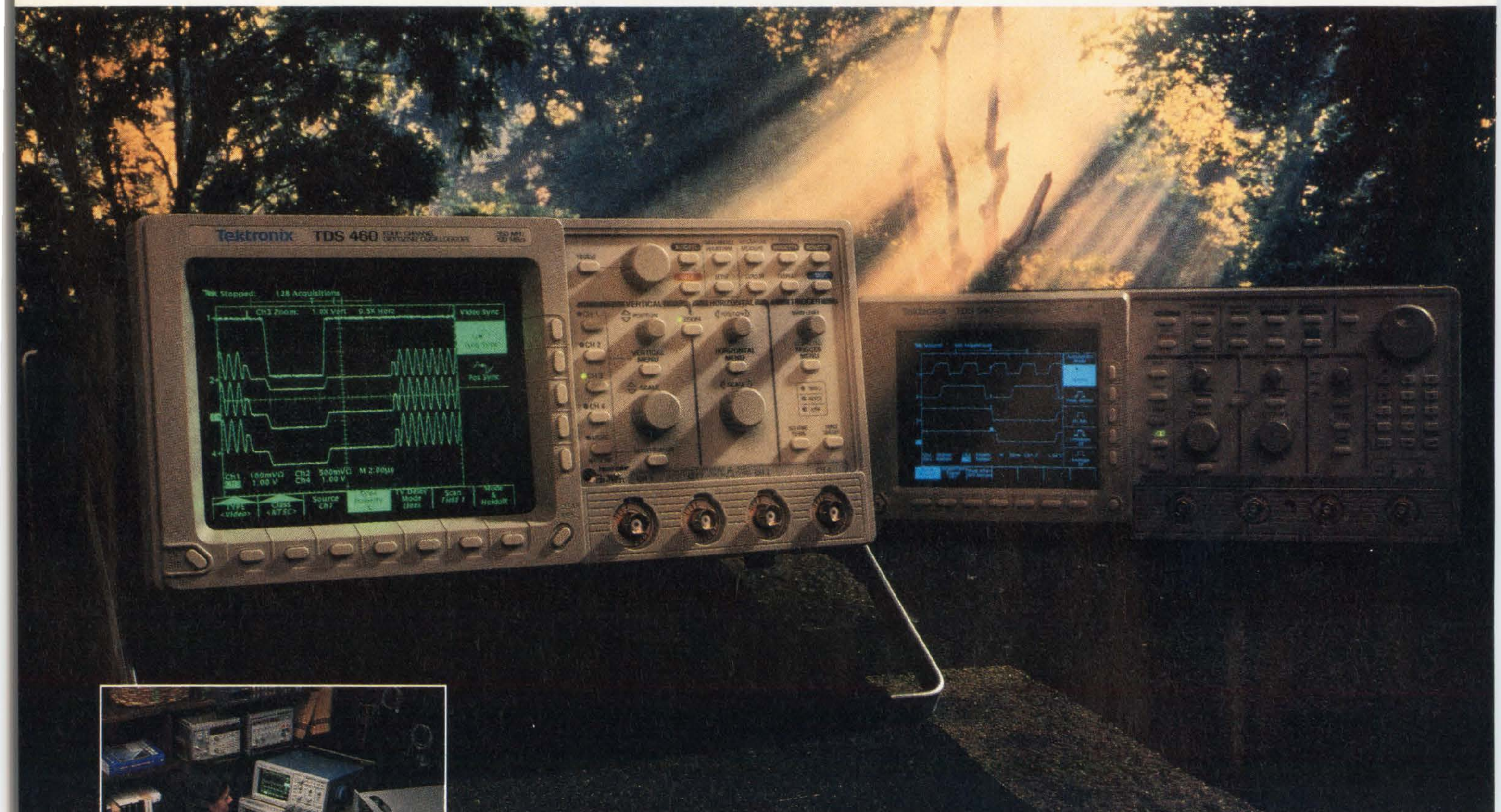
Modular configuration (90- and 120-position sections) provides 'building block' flexibility, with applications to 810 positions or more. Header posts in staggered heights allow four-level sequenced mating.

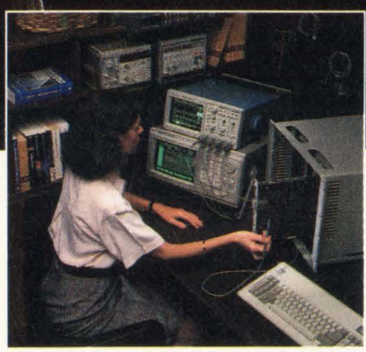
For the Plus in high-speed performance, call our Product Information Center at 1-800-522-6752 (fax 717-986-7575). AMP Incorporated, Harrisburg, PA 17105-3608. In Canada call 416-475-6222. For design assistance in characterized back-plane assemblies, contact AMP Packaging Systems, 512-244-5100.

AMP

CIRCLE NO. 36

Tek's new encore TDS 400. Extraordinary 4-channel power. Ordinary 2-channel price.





Tek's new TDS 400 Series oscilloscopes make TDS performance from 150 MHz to 350 MHz more portable and affordable than ever.

Now you can pick up where Tek's breakthrough TDS 500 Series left off — with a compact, versatile new series that puts the TDS platform's 4-channel acquisition, multiprocessing and intuitive operation within easy reach of digital, analog and electro-mechanical design, production test, field service, and many other demanding tasks.

For the usual price of *two* channels, you can now have:

- 100 MS/s sampling on each of four channels.
- On-the-fly signal processing with up to 12-bit vertical resolution.
- Record lengths to 30,000 points.
- Video trigger option with back-porch clamp and dial-up line/field selection.
- 22 time-saving automatic measurements.
- The unique graphical user interface that lets most TDS manuals stay shrink-wrapped on the shelf.

Call 1-800-426-2200 Ext. TDS4, for more information on either the new TDS 400 or the recently-announced TDS 500 Series — with up to 4 channels, 1 GS/s sampling and 500 MHz bandwidth — and for the number of your nearest Tek sales office. We'll put you through to all the right channels, fast!

Tektronix

Test and Measurement

CIRCLE NO. 37

3GA-188087-0

Controller quickly charges NiCd batteries using current pulses and time derivatives

Quickly charging a NiCd battery requires controlled application of charging current and careful monitoring of the cell's condition. The ICS1700 rapid-charge controller meets these two requirements by using a pulsed current to charge the cell and by calculating the first derivative of the battery voltage to assess the cell's state of charge.

The controller's use of both techniques allows you to charge NiCd batteries safely in approximately 20 minutes by preventing undue build-up of pressure and temperature within the battery. The controller can charge NiCd cells at ½, 1, 2, and 4C. (The C rate is defined as the current-flow rate that is equal to the rated battery capacity. For example, applying a 2A charge to a 1 Ahr battery is a 2C rate.) When charging at a 4C rate, the approximate charge time is 20 minutes.

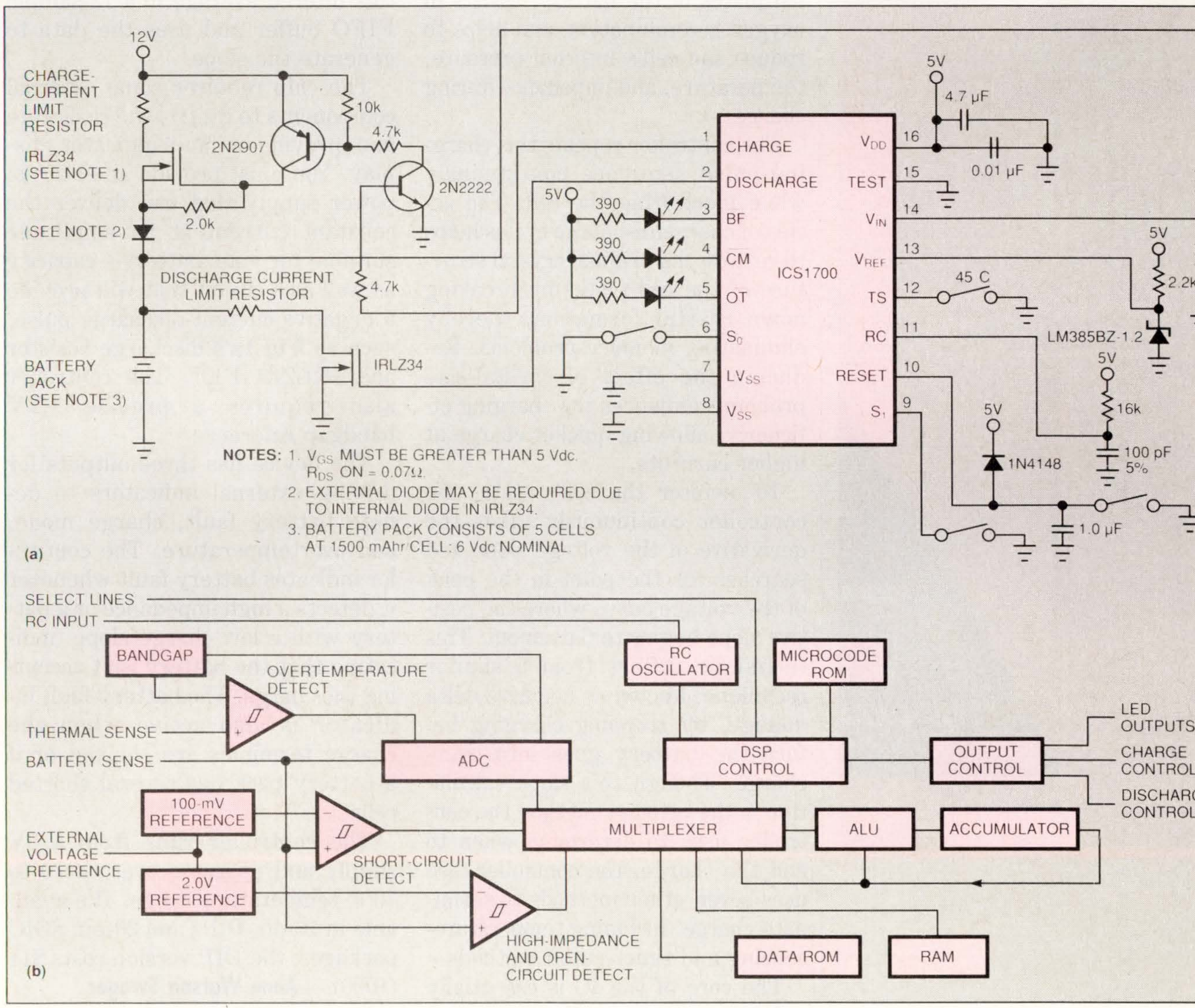
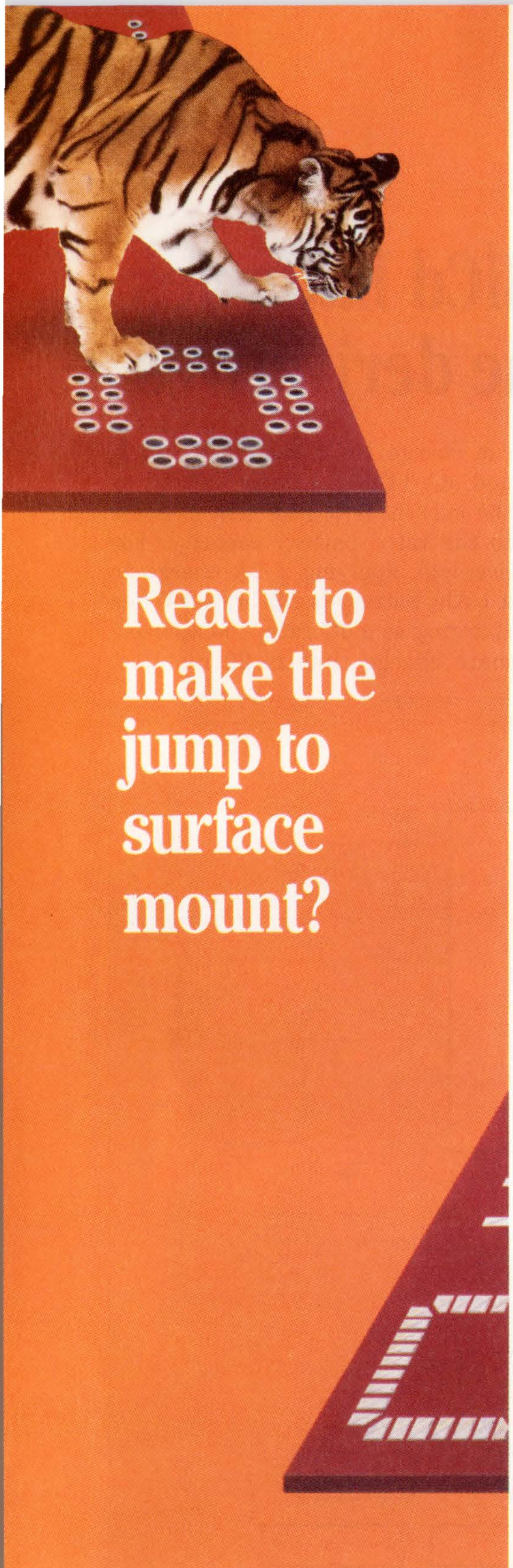


Fig 1—In a typical application, the ICS1700 quickly charges NiCd batteries working in conjunction with other circuitry (a), such as a power supply, discharge FET, and simple transistor switches. The IC itself (b) consists of an ADC to read in the battery state and a controller optimized for the efficient numerical calculations necessary to derive the linear regression slope and determine the correct charge-termination point.



Note that not all batteries can handle 4C charging rates, so you must select an appropriate battery.

The controller works in tandem with a power supply to implement a patented pulse-current technique that consists of a positive-current charging pulse followed by a high-current, short-duration discharge pulse. (The company licenses the patented reflex charging pulse from Christie Electric Corp, Gardena, CA.) This short pulse prevents the build-up of gas bubbles on the internal plates of the battery, assists in oxygen recombination, and helps to reduce the cell's internal pressure, temperature, and impedance during charge.

The controller repeats this charging-pulse sequence continuously while monitoring the cell. The series of charge/discharge cycles helps to restore the original crystal structure of the cell plates by breaking down crystal formation, thereby eliminating memory problems. Reducing the effect of crystal-size problems enhances the charging efficiency, allowing quicker charge at higher currents.

To monitor the cell's state, the controller continuously takes the derivative of the voltage slope and searches for the point in the peak of the voltage curve where the positive slope begins to flatten out. This technique differs from a similar technique, known as negative delta voltage, by stopping charging before the battery goes into overcharge. Though this slope calculation is the primary method the controller uses to determine when to end the charge, the controller also uses seven other methods to terminate charge, including temperature-sensing and timer-cutoff methods.

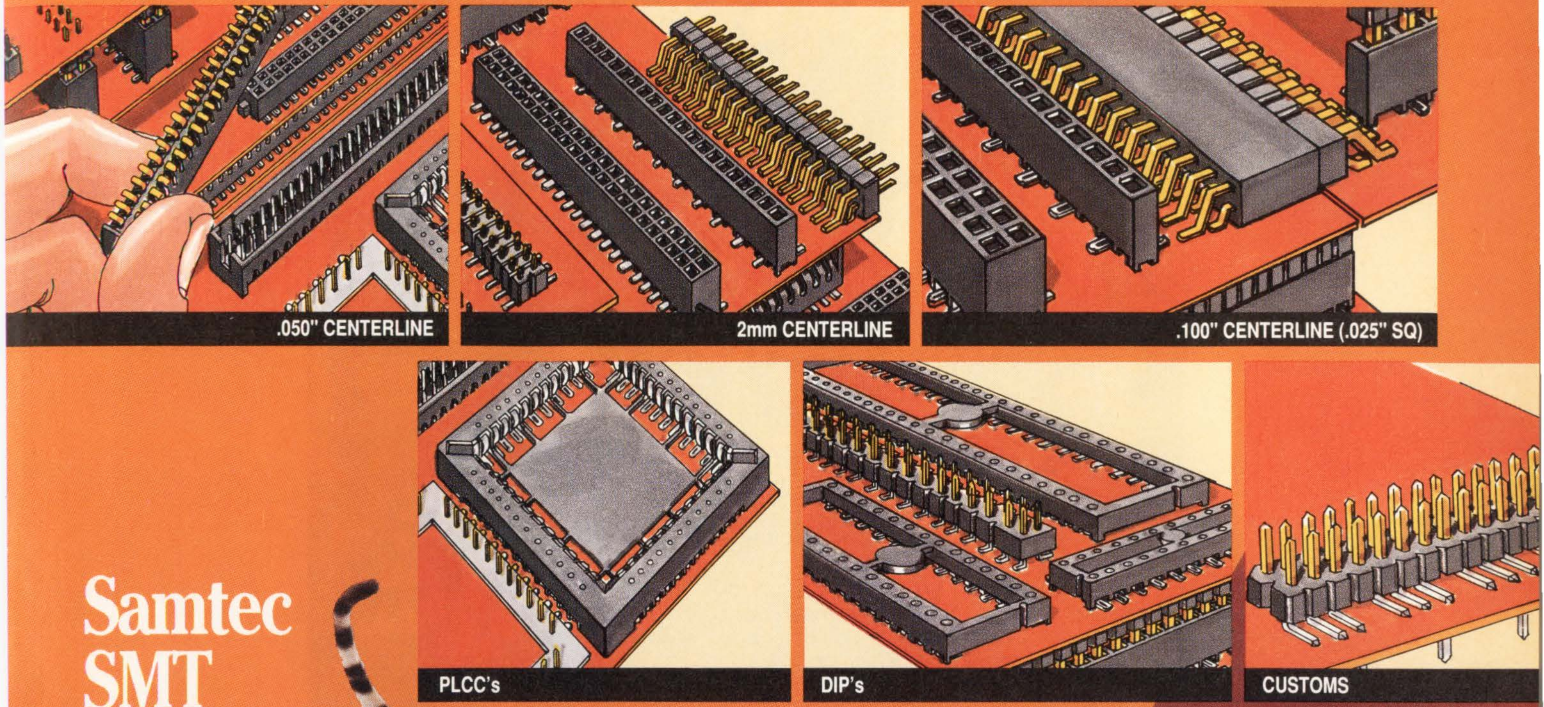
The core of the IC is essentially a RISC microcontroller optimized for the efficient numerical calculations needed to derive the linear regression slope and determine the correct charge-termination point. The controller uses a 10-bit successive-approximation ADC to sample the analog voltage of the battery. The IC averages the result of successive conversions to limit the effect of voltage jumps caused by battery and ADC noise. The number of successive voltage samples that the controller averages depends on the charge rate. An IIR filter weights the averaged voltage to filter out any large aberrations in the cell-voltage curve. The IC stores this filtered average in a 12-sample FIFO buffer and uses the data to generate the slope.

The chip requires some external components to control the clock rate and provide a fault-indicator display. You must provide an external power supply that can deliver the constant current at an amplitude suitable for your battery's capacity as well as a circuit that will provide a negative current-discharge pulse, such as **Fig 1a**'s discharge resistor and IRLZ34 FET. The controller also requires a precise 1.2V bandgap reference.

The device has three outputs for driving external indicators to denote battery fault, charge mode, and overtemperature. The controller indicates battery fault whenever it detects a high impedance or a battery with a low charge slope, indicating that the battery isn't accepting the charge. The battery-fault indicator is also active when the charge terminals are shorted or if a battery pack has several shorted cells.

The controller runs from a 5V supply and operates over the 0 to 70°C temperature range. It's available in 16-pin DIPs and 20-pin SOIC packages; the DIP version costs $11 (1000).—**Anne Watson Swager**

Integrated Circuit Systems Inc, 2626 Van Buren Ave, Valley Forge, PA 19482. Phone (215) 666-1900. FAX (215) 666-1099. **Circle No. 731**



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CIRCLE NO. 38

Workstation brood adds low-end machine and servers

An entry-level workstation, four servers, and two high-end, 24-plane graphics boards expand the utility of the HP 9000 Series 700 family of PA-RISC-based workstations. The Series 700 Model 710 has an entry-level price of $7490 and delivers 49.7 SPECmarks, 57.9 MIPS, and 12.2 Mflops from its 50-MHz CPU. These metrics contrast with the $11,990 Model 720, whose performance of 59.5 SPECmarks, 57.9 MIPS, and 17.9 Mflops represents a compiler-enhancement-based improvement from its introductory numbers. Two mechanisms that reduce price and improve performance of the Model 710 workstation are the smaller caches: the 32-kbyte instruction cache and 64-kbyte data cache are from one-quarter to one-half the size of those of the other family members.

The base machine comes diskless, with 16 Mbytes of memory, graphics supporting eight image planes, and a 19-in., 1280×1024-pixel-resolution gray-scale monitor. Graphics options allow you to configure the machine with color monitors: a 16-in. 1024×768-pixel monitor ($4000) or a 19-in. 1280×1024-pixel monitor ($6500). All three graphics options are integrated into the CPU and utilize hard-coded graphics primitives to achieve 7292 X11 performance and 950,000 2- or 3-D vectors/sec. Integration onto the CPU is another cost-saving feature.

You can add as much as 840 Mbytes of internal disk storage in four half-height slots or 9.4 Gbytes using external disk arrays. The low-end workstation also supports 1.44-Mbyte, 3½-in. floppy-disk drives, CD-ROM storage, or 2-Gbytes of 3.5-in. DDS (direct-digital-synthesizer) tape. You can also increase your main memory from 16 Mbytes to as much as 64 Mbytes, using error-correction code SIMMs.

The four servers come in four configurations ranging in price from $23,440 to $87,638. The servers enhance network capacity via an internal disk capacity of as much as 2.6 Gbytes and an external capacity of 236 Gbytes. All servers offer two 8-Gbyte, 4-mm DAT (digital-audio-tape) drives and a 600-Mbyte CD-ROM. You can stuff the main memory with 32 to 384 Mbytes of RAM.

The existing workstation family previously offered three graphics choices. These choices featured circuit boards with 8-plane gray-scale or color and a board with as many as four i860 CPUs.

Two new boards for the higher-end 720, 730, and 750 workstations are called the CRX-24 and CRX-24Z. They provide a 24-plane single buffer or 12+12-plane double buffer and offer eight overlay planes for additional storage. The CRX-24Z supplements the features of the CRX-24 with a hardware Z-buffer, accelerated shading, and antialiasing.

Because both boards operate at greater than 30 frames/sec, they both support video. These two graphics options range in price from $13,500 to $21,500. A $2000 software product called Power Shade adds shading capabilities to the existing graphics products or to the new CRX-24; it comes with the CRX-24Z.

In contrast to the relative dearth of software vendors committed to the Series 700 at introduction, HP announces that almost 2000 applications are possible on the workstations today.

Prices are not yet firm and could be lower than quoted. All products are available except for the graphics boards, whose delivery takes four to eight weeks ARO.

—Michael C Markowitz

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900. **Circle No. 732**

Extending the low end of its RISC-based workstation line, Hewlett-Packard's Series 9000 Model 710 runs at almost 50 SPECmarks.

NEW

8-bit 68HC05K microcontroller minimizes cost and fits in 16-pin DIPs and SOICs

Engineers who need to watch their design pennies will like a low-end version of the Motorola 68HC05 8-bit microcontroller (μC). The 68HC05K series brings the μC's architecture down to a 16-pin DIP, the smallest pin package for any 8-bit μC. In large OEM volumes, these μCs' cost will fall to less than $0.90. In addition, the μC's design minimizes the need for extra components.

Motorola's 68HC05 is a simple μC with a single accumulator and index register. It comes with limited on-chip ROM or EPROM and RAM, typically with 2 to 4 kbytes of ROM and 176 bytes of RAM. It has no provisions for accessing off-chip memory and has four 8-bit I/O ports and a counter/timer system.

The series takes the 68HC05 architecture down another level. Although it has the standard 6805 processor core, the 68HC05K's peripherals have been cut back. It has two I/O ports—one has eight and one has two I/O lines. On-chip memory has been reduced to a 1-kbyte address space, with 504 bytes of ROM or EPROM (including eight interrupt vectors) and 32 bytes of RAM. A new μC option is a 64-bit personality EPROM, which holds version or design data.

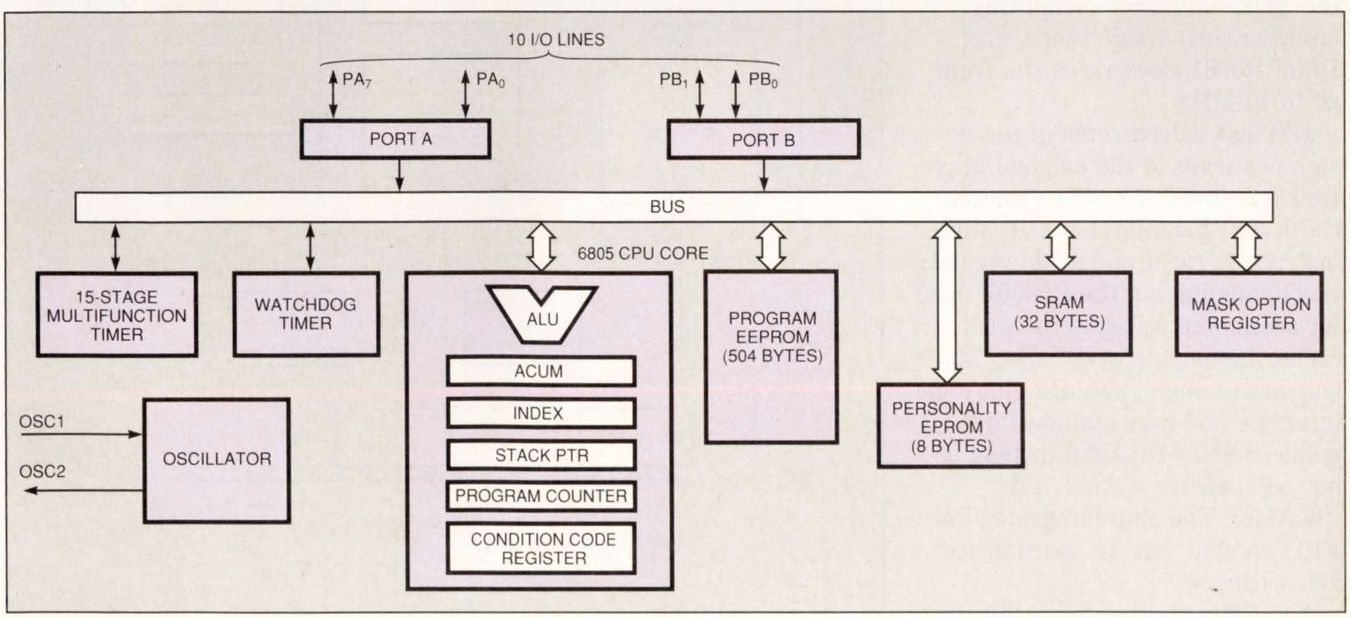
Reduced stack-pointer size is a result of the series' limited addressing space. The μCs have a reduced, multifunction 15-stage timer. A programmable watchdog timer catches runaway software. Both watchdog-timeout and timer-overflow conditions trigger interrupts.

The μCs feature the standard IRQ external-interrupt line as well as a programmable option for four I/O lines. The I/O lines can be ORed to IRQ, creating five external-interrupt sources. The μC series runs with a 4-MHz external oscillator or clock; internal clocks are 2 MHz divided down from the rate.

Three new μCs enlarge the 68HC05K family: the base level 68HC05K0; the 68HC05K1 with personality EPROM; and a one-time-programmable 68HC705K1 with EPROM.

To save external components, four of the I/O lines can sink 4 mA to drive LEDs directly, eliminating drivers. Port I/O pins have software-programmable pull-down resistors (100 μA), eliminating external pull-down resistors.

Shortly, the company will introduce a new PC-based integrated-development-software package for the 68HC05K. Developed by P&E Microsystems (Woburn, MA), the package includes a macro assembler, an editor, a simulator, and a



This low-end, 8-bit μC family, the 68HC05K microprocessor series, has a 1-kbyte address range with 504 bytes of ROM or EPROM and 32 bytes of RAM. The series also has a reduced set of peripherals and 10 I/O pins.

windowed source-code debugger, all combined in an integrated environment.

The low-end 68HC05 parts cost $1.20 for the 68HC05K0, $1.85 for the 68HC05K1, and $2.75 for the one-time-programmable 68HC705K1 (10,000). Samples of the chips are available now.

—**Ray Weiss**

Motorola Inc, Microprocessor Products Group, 6501 William Cannon Dr, Austin, TX 78735. Phone (512) 891-3434. **Circle No. 733**

MIPS-based chip in 84-pin package runs to 40 MHz

The MIPS-architecture-based ACE, a RISC alternative to PCs, may not have to wait for the Mips R4000 superpipelined RISC (reduced-instruction-set computer) chip. The R3081, a MIPS-based chip, is a high-end version of IDT's R3051/2 family of embedded RISC CPUs. The R3081 is compatible with the Mips R3000 and can run the emerging Microsoft Windows/NT operating system, the core of the ACE (advanced-computing environment) architecture, and Unix. R3081 clock rates run from 20 to 40 MHz.

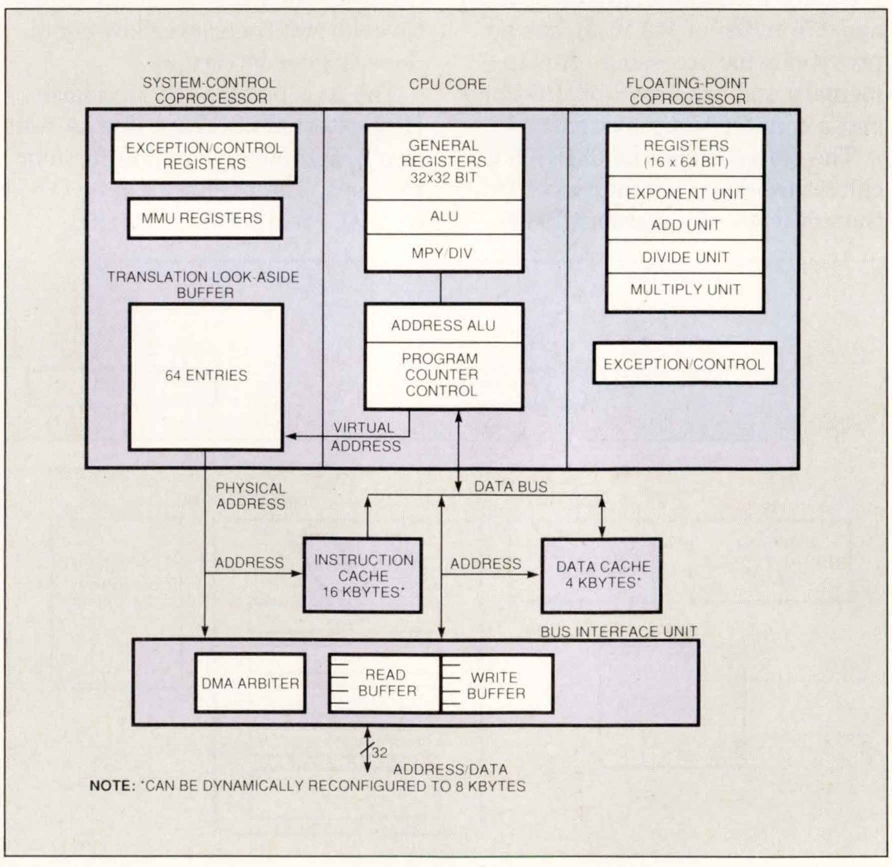
IDT has solved some of the design obstacles of the original Mips R3000 architecture. For example, the R3081 incorporates a 16-kbyte instruction cache and a 4-kbyte data cache, eliminating the R3000's need for sequential accesses to two caches in a single cycle. Also, the chip has a simple, minimal glue logic interface and uses standard dynamic RAMs (DRAMs) instead of more-expensive static RAMs (SRAMs). The chip integrates an FPU on chip, saving board space and wiring.

The R3081 is pin compatible with earlier R3051 CPUs; existing designs can be upgraded without redesign. The R3081 has one of the largest instruction caches among RISC processors. The R3081's caches can be dynamically modified to an 8-kbyte instruction and data cache configuration, creating a more-balanced configuration. Thus, the operating system can configure the hardware for large-scale applications; the only limitation is that the caches must be flushed before reconfiguring them.

The R3081 caches are direct mapped (only one cached item per address) and are physically, rather than virtually, addressed. This relieves the requirement that virtual caches be flushed on a process context switch. The instruction cache has a 4-word, 16-byte line size (smallest cached element is four words). The data cache has a word or 4-byte line size. The R3081 has a write-through cache policy—writes to the cache are also written through to main memory. For cache coherency, DMA writes from the cache can be programmed to invalidate the cache lines written, eliminating potential data conflicts (the main memory data now is the valid data).

Like the R3051, the R3081 CPU uses a multiplexed address and data bus to help minimize pin count. This approach does not markedly hamper CPU-memory performance: It shifts from address to data in ½ a clock cycle and has read/write buffering. With fast enough DRAMs, reads can take two memory cycles, and writes two or three cycles, depending on decode-logic times. The multiplexed bus does, however, require external logic to latch the address and hold it during the data-presentation phase of a memory cycle.

IDT designers improved CPU



The latest IDT revision of the MIPS RISC architecture, the R3081 combines large on-chip cache with an FPU and a multiplex bus, fitting a small-package IC.

WORLD'S SMALLEST 8th-ORDER LOWPASS FILTERS - $2.95*

Butterworth & Bessel with No External Parts

Maxim's new MAX291/MAX295† (Butterworth) and MAX292/MAX296† (Bessel), 8th-order low-pass switched-capacitor filters, come in space-saving small-outline 8-pin miniDIP and SO packages. And to save even more space and design time, no external resistors or capacitors are needed.

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  100:1 Clock to Corner Ratio
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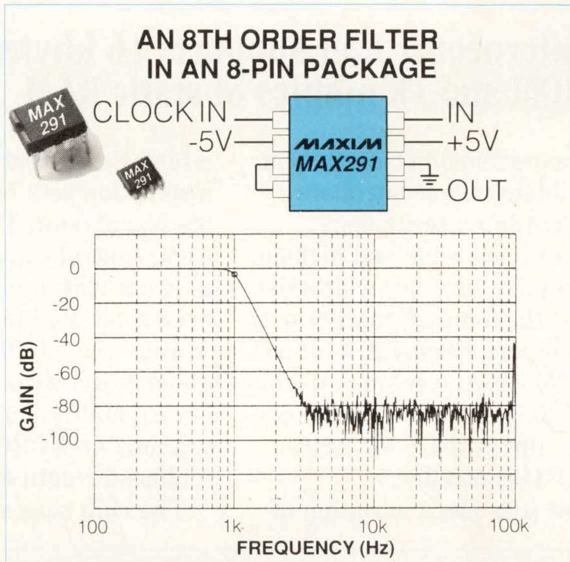
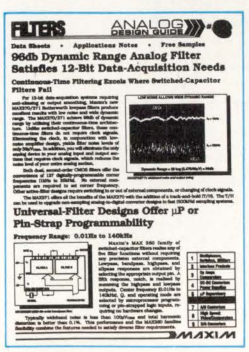
  50:1 Clock to Corner Ratio
- ♦ **THD + Noise: -70dB Typ.**
- ♦ **+5V or ±5V Supply Operation**
- ♦ **Cascadable for Higher Orders**



MAX291's 8th-order Butterworth response has 48dB/octave rolloff with no passband ripple.



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* 1000-up FOB, USA suggested resale.
† MAX295/MAX296 will be available after February, 1992.

CIRCLE NO. 41

performance by adding read and write buffers. These 4-word-deep read and write buffers allow the CPU to continue processing: Writes are buffered for later execution and burst or block reads can be picked up independently of the CPU.

In addition, the R3051 and R3081 support DMA for peripherals (the DMA takes over the CPU's external bus). Also, the bus interface has been improved with a higher drive, clock output, a half-frequency bus operation option (to have memory bus speeds relative to the CPU bus rates), and a slow bus turnaround feature that eliminates 3-state contention problems for external memory reads followed by writes. The 20-, 33-, and 40-MHz parts cost $98, $146, and $196, respectively, (10,000). Samples of the R3081 will be available in March.—**Ray Weiss**

Integrated Device Technology Inc, 3236 Scott Blvd, Santa Clara, CA 95052. Phone (408) 727-6116. FAX (408) 492-8674. **Circle No. 734**

4-bit microcontroller supports 16 kbytes of EPROM and 1k nibbles of static RAM

Engineers shouldn't treat 4-bit (1-nibble) microcontrollers (μCs) as outdated technology. Four-bit μCs are alive and kicking. In fact, they're busy attacking the low end of the 8-bit μC market with specialized peripherals. A 4-bit μC, the μPD75P316A, combines 16 kbytes of EPROM with low power consumption, direct drive for LEDs, and an LCD controller.

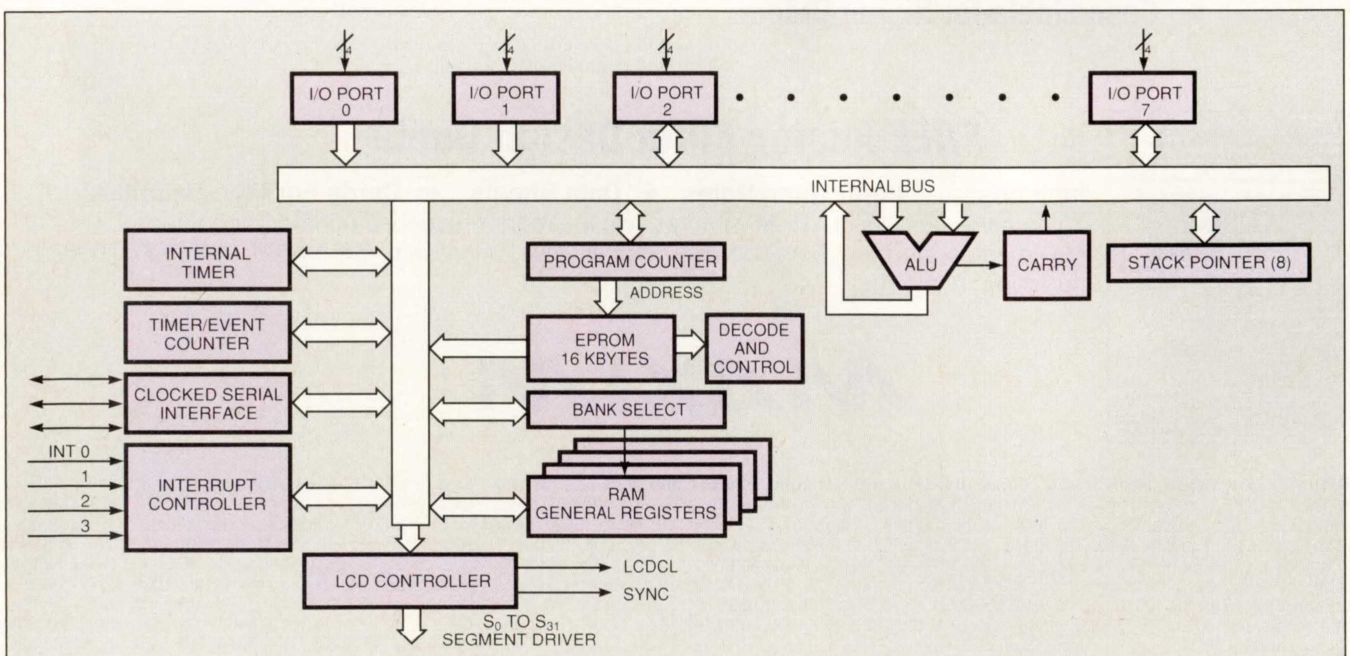
Four-bit μCs are a variation of 8-bit μCs, in that they sport 8-bit instruction sets but use 4-bit arithmetic and data. Thus, they have the same control capabilities of 8-bit μCs but suit applications that don't need 8-bit arithmetic or long data words. The μUPD75P316A, a single-chip μC with no external memory capability, has 16 kbytes of programmable EPROM on chip and 1k nibbles for data storage.

The chip runs with a 4.19-MHz clock and has an execution cycle of 0.95 μsec. The CPU has a set of general-purpose registers, eight 4-bit registers, or four 8-bit registers. These are not minimal processors; they have more than 100 instructions, including bit manipulation and table-reference operators. Six data-addressing modes comprise 1-, 4-, and 8-bit direct; 4-bit register indirect and 8-bit register indirect; and bit-manipulation addressing.

This chip is an extension of an existing 4-bit μC, the μPD75P316. The new chip has doubled data memory and additional EPROM. Both chips can run at low voltages, minimizing operating power dissipation: Voltage ranges are 2.7 to 6V.

RAM is organized into four banks of 256 nibbles each. The first bank is for CPU registers, interrupt vectors, and the program stack. The μC peripherals are memory mapped and are in memory bank 15.

The μPD75P316A chip comes with peripherals that include an LCD controller, a watchdog timer, an 8-bit binary counter with comparator and count register, a serial bus for interfacing with other processors, and three 4-bit I/O ports.



This 4-bit μC, the NEC μPD75P316A, is a full-fledged microcontroller with sophisticated peripherals, including an LCD controller.

QUAD VOLTAGE-OUTPUT 12-BIT DACS REPLACE 4 OP AMPS AND 4 DACS!

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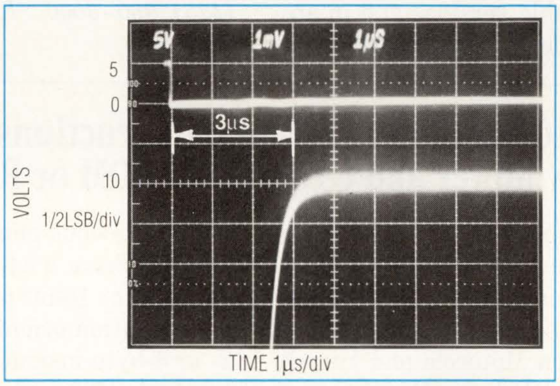
Maxim's new MAX526 quad voltage-output A/D converter replaces 4 digital-to-analog converters (DACs) and 4 op-amps with a single CMOS monolithic IC! The new DAC delivers performance you'd expect from hybrid and module quad DACs. Maxim guarantees monotonic 12-bit performance with 1/2LSB relative accuracy over temperature for all 4 outputs, and 1LSB total unadjusted error with no zero- or full-scale adjustments. And, 10V outputs settle to 1/2LSB in 5μs.

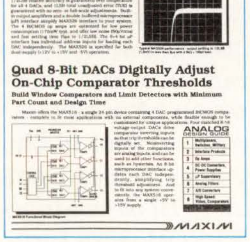
- ♦ **Four 12-Bit DACs in One Package**
- ♦ **Buffered Voltage Output**
- ♦ **1LSB Total Unadjusted Error**
- ♦ **Double-Buffered Logic Inputs**
- ♦ **24-pin DIP and SO Packages**
- ♦ **Parallel μP Interface**



Typical MAX526 performance-output settling to 1/2LSB (1.2mV) in less than 3μs with a 5kΩ + 100pF load.

Input Double Buffering & Output Amplifiers Simplify Design

The MAX526's double-buffered 8-bit parallel interface simplifies digital connections by eliminating "glue" logic. The analog interface is also simplified by built-in output amplifiers, eliminating external op-amps and providing the speed and drive needed for most applications.



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CIRCLE NO. 42

To save on component costs, the I/O-port pins have programmable pullup resistors. Three ports can drive LEDs directly, eliminating the cost of drivers or buffers.

The on-chip LCD controller has four modes, which drive 32, 64, 96, or 128 LCD segments. The controller saves the LCD data in the upper 32 nibbles of RAM bank 1. The controller has built-in timer functions (using the μC timer) to refresh the LCD displays automatically. Signals coordinate multiple μCs acting as LCD controllers.

The μPD75P316A comes in an 80-pin quad flatpack for one-time-programmable versions and in an 80-pin leadless chip carrier with a window for reprogramming. To program the EPROM, 12.5V are needed. The chips meet commercial −40 to +85°C temperature ranges.

Development support for the 4-bit μC includes a structured assembler preprocessor, which incorporates high-level control constructs into assembly code, making it easier to structure a program.

The μPD75P316A costs $27.95 (10,000) for the one-time-programmable part and $65 for the reprogrammable part (small qty).

—**Ray Weiss**

NEC Electronics Inc, 401 Ellis St, Mountain View, CA 94039. Phone (415) 960-6000. FAX (800) 729-9288. **Circle No. 735**

16-bit μC combines 200-nsec instructions with low power and 64-kbyte EPROM or ROM

American engineers can now design in Hitachi's 16-bit, high-end microcontroller (μC) H8/500 series. Because a patent-infringement suit between Motorola and Hitachi has been settled, the H8/500 is now available in the United States. The H8/500 is a 16-bit μC having a 200-nsec basic instruction cycle backed up with as much as 62 kbytes of on-chip EPROM or ROM and 2 kbytes of static RAM.

The previous-generation 300 series μCs have a 64-kbyte address space, 8- or 16-bit registers, a register operation orientation, and fixed 2- or 4-byte instructions. In contrast, the 500 series can address 16 Mbytes using paged addressing. The series also features an orthogonal instruction set, a 32-bit-long word for 32-bit processing, and a peripheral set.

The H8/500 μCs support a single address space—with as much as 16 Mbytes of external memory—using memory pages. The CPU works within a 64-kbyte page, which is defined by page registers. The three major memory modes of the chip include Expanded Minimum, which addresses 64 kbytes of external memory; Expanded Maximum, which addresses 1 Mbyte of external memory (16 pages); and Single Chip, which addresses on-chip memory only. The μCs have an 8- or 16-bit external memory bus. Internal-memory accesses take two internal clock cycles, and external-memory accesses take three cycles.

The series has eight general-purpose 16-bit registers—two of which are dedicated as stack and frame pointers. Running at 10 MHz, the μCs deliver a 200-nsec add, a 1.6-μsec multiply, and a 2.6-μsec divide. The series has a variable instruction length with 63 instructions. The μCs' seven addressing modes include a register indirect with an increment/decrement option, which is effective for optimized table-entry processing. The instruction set also includes bit manipulation and test instructions.

The instruction-processing rate increases by laying out instruction object code in reverse order in memory. Instead of having the op code as the leading byte for an instruction, it is presented last, trailing the effective address information. This reversal speeds execution because the effective address fetches can parallel instruction decoding.

The μCs have as much as 62 kbytes of on-chip program memory, which is the largest amount of on-chip memory for any commercial 16-bit μC. This factory-programmed memory is either mask ROM or one-time-programmable EPROM (zero turnaround time) for fast delivery and prototyping. For program development, windowed reprogrammable EPROM parts will be available in 80-pin, plastic-leaded-chip-carrier versions of standard 84-pin, zero-

Table 1—Hitachi H8/500 Series Microcontrollers

H8 Version	Features	Price (quantity)
Common to all	Seven or more ports, duplex serial channel, 10-bit A/D converter (13.8 μsec) watchdog timer, 9 external interrupts, DMA controller, wait-state controller, 8-bit multifunction timer, 2 or more 16-bit timers, 3V power versions	NA
510	ROMless controller 16-bit external bus, on-chip DRAM refresh 112-pin quad flatpack	$11.85 (5000)
520	Low-end controller 64-pin package 16-kbyte ROM/EPROM, 512 bytes of RAM	$11.45 ROM (10,000) $22.22 EPROM (1000)
532/534	Midrange controller, 3 PWM timers, extra 16-bit timer, 32-kbyte ROM/EPROM, 1- to 2-kbyte RAM 84-pin plastic leaded chip carrier or 80-pin quad flatpack	$14.20 ROM (10,000) $25.80 EPROM
536	High-end controller, 3 PWM timers, extra 16-bit timer, 62-kbyte EPROM/ROM	$19.40 ROM (10,000) $34.10 EPROM (1000)

Note: NA=Not applicable.

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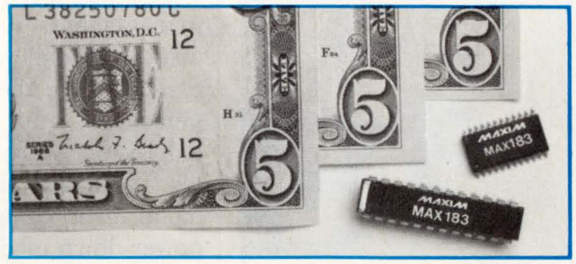

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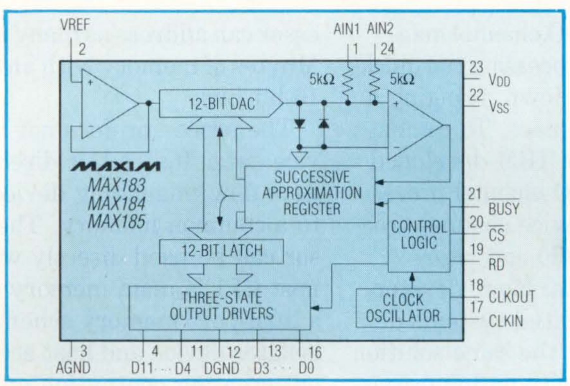
The MAX183 reduces design complexity and time with flexible +5V, +10V, or ±5V input ranges and an internal reference buffer that allows one system reference to drive multiple ADCs. The A/D works with an external voltage reference, so you can choose the optimum one for each application.



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CIRCLE NO. 43

turnaround-time parts. These devices can be programmed in a standard 27256-type EPROM programmer.

These 16-bit μCs also have a large set of on-chip peripherals, which include two or three 16-bit timers, an 8-bit free-running timer, a DMA controller, seven to nine I/O ports, an interrupt controller, a 10-bit A/D converter, a serial communications interface (duplex), and a watchdog timer.

The μCs have built-in power management. You can choose three programmable power-down states: Sleep, where the clock and support peripherals run, but the CPU is halted; Software Standby; or Hardware Standby—in both standby modes everything is halted. In all power-down modes, RAM and register values are held. Recovery is triggered by combinations of interrupts and special pin inputs. Typical current dissipation is 30 mA running, and 20 mA and 0.01 μA, respectively, for sleep and standby modes.

Software tools are available for the μC series: two C compilers from Avocet Systems Inc (Rockport, ME) and Software Environments Ltd (Dallas, TX), as well as a Forth system, and a Fuzzy-Logic compiler from Togai Infralogic (Irvine, CA). In-circuit emulators are also available from a number of vendors.

—**Ray Weiss**

Hitachi America Ltd, Semiconductor and IC Div, 2000 Sierra Point Pkwy, Brisbane, CA 94005. Phone (415) 589-8300. FAX (415) 583-4207. **Circle No. 736**

Programmable I/O processor services device interrupts

Device and I/O channel management processing can quickly load a system down, bringing a host CPU to its knees. To combat this, in the 1960s, IBM developed programmable I/O channel processors to offload device channel processing from the 360 and later-version host CPUs. Now, desktop, server, and dedicated-systems designers can apply the same solution to their designs with an I/O processor chip, the Signetics SC26C460.

When a device needs service, it triggers a request line; the SC26C460 processor will then queue these requests, servicing them by assigned priority. The chip can interrupt the host CPU to pass data or request service.

The chip is a dedicated I/O processor that can handle as many as 32 device channels, directing and controlling their I/O data streams. The chip is programmable, with 15 instructions; the processor offloads the host CPU by fielding device interrupts and managing the device data transfers between the peripherals and main memory. The processor can address as many as 16 Mbytes of memory with an 8- or 16-bit bus.

The processor does not buffer device data. Instead, it directs the data flow, managing device access to a common memory. The processor can be used directly with the host CPU's main memory or with a dual-port memory scheme, which isolates device and host access without creating contention on the host memory bus.

The processor stores separate memory addresses and buffer lengths for each device channel; each device channel has a separate channel program-entry point. The processor can interrogate and check device status, read and write a peripheral, and branch to a different processing stream. It can also translate device code via decision tables.

The SC26C460 I/O processor comes in a 68-pin plastic leaded chip carrier and costs $18.50 (1000).—**Ray Weiss**

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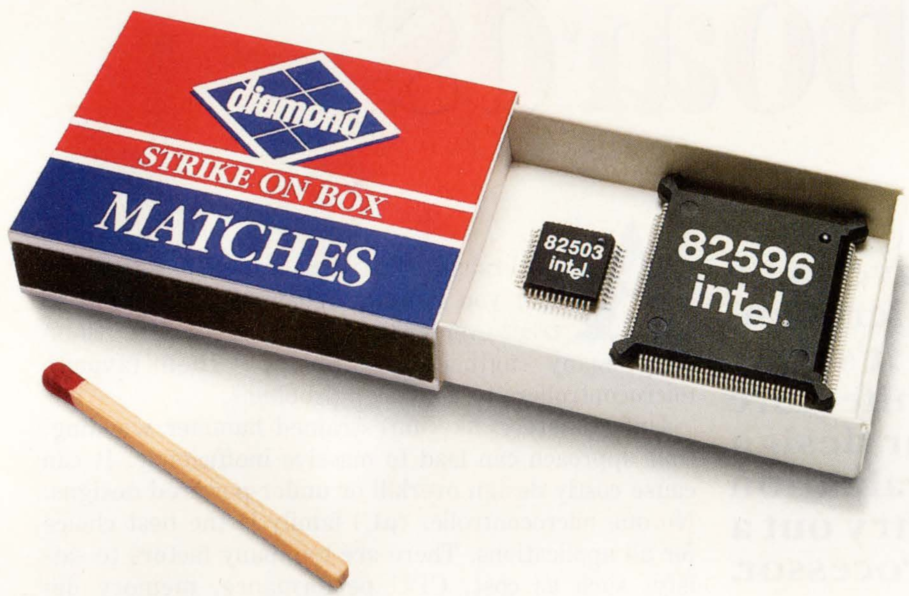

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8-bit μC evaluation boards

You no longer have to be tied to a single microcontroller (μC) family. It's easy to try another architecture to fill out your design tool kit. Pick an evaluation board and try out a new processor.

RAY WEISS, Technical Editor

As Abraham Maslow noted, "When the only tool you have is a hammer, you tend to treat everything as if it were a nail." Similarly, many engineers try to apply their favorite microcontrollers to all design problems.

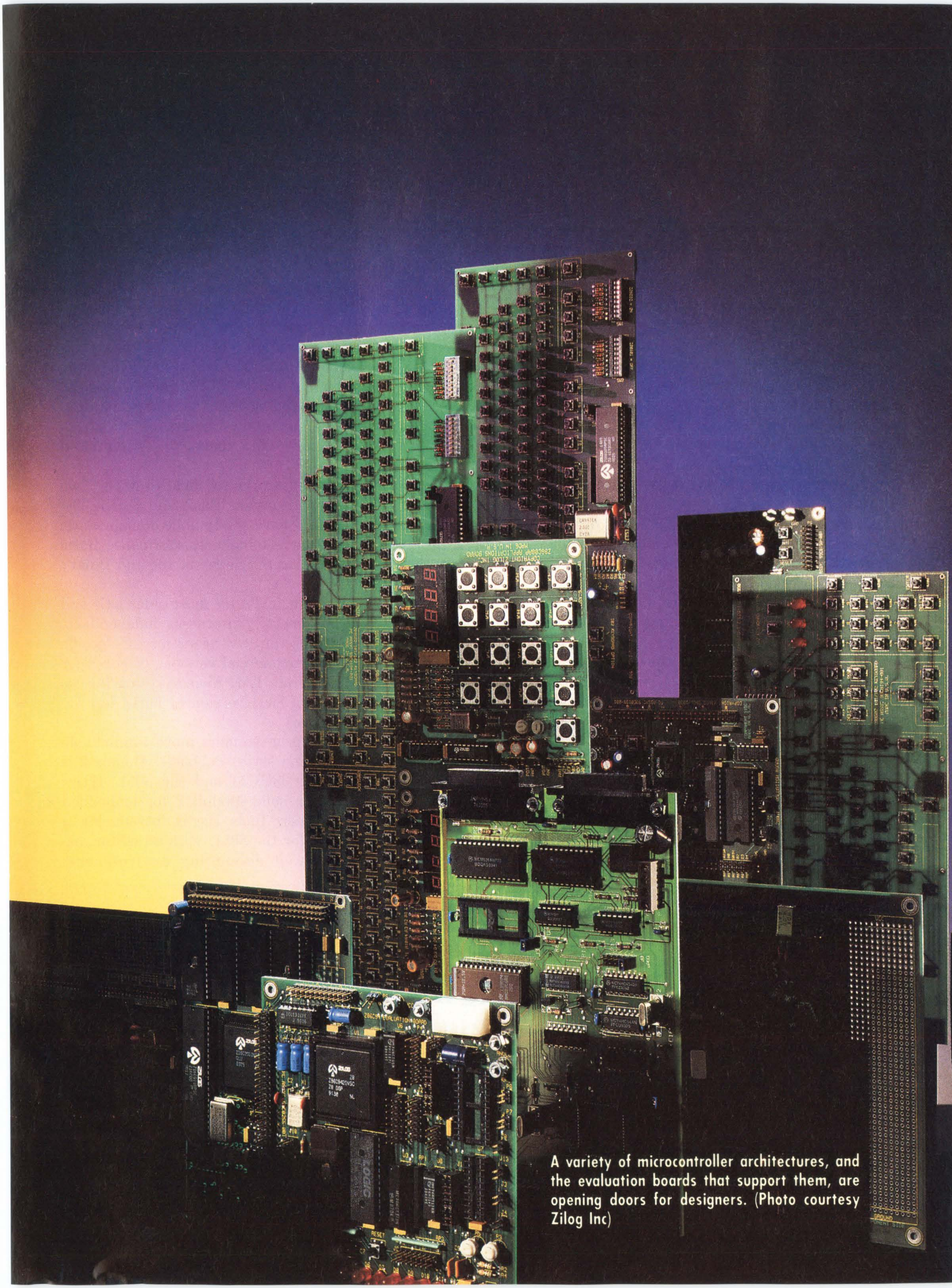
Unfortunately, like unrestrained hammer wielding, that approach can lead to massive inefficiency. It can cause costly design overkill or under-powered designs. No one microcontroller (μC) family is the best choice for all applications. There are too many factors to satisfy, such as cost, CPU performance, memory demands, peripheral needs, and board space. Even so, many engineers are reluctant to try new μCs, to go through the painful process of integrating a new CPU and software into their design environment.

However, today it's easy to try out a new μC. There's a variety of choices, ranging from small, low-cost, minimal-pin-count μCs to fast, high-memory density μCs loaded with peripherals. And, today's μCs have far better documentation and software.

Low-cost evaluation boards and software also put trying out a new system within any engineer's grasp. Most evaluation sets cost less than $500. Almost all are below a lab manager's sign-off limits.

New μCs = PCs + Software

These days it's far easier to add a new μC family to your design stable. A major enabling factor is the IBM PC, which provides a common base for μC development tools. PCs and clones also provide a common



A variety of microcontroller architectures, and the evaluation boards that support them, are opening doors for designers. (Photo courtesy Zilog Inc) operating methodology for tools, unlike years ago in the age of "blue boxes," where each chip vendor had their own proprietary development stations.

Most evaluation boards link to a PC via its serial port. Users on the PC host interact with the target board through terminal emulator software. Typically, the target μC runs a target monitor, a software kernel that controls the μC and links to the host. Through a terminal emulator, users link to the monitor and interactively start, stop, set breakpoints, and interrogate the target μC processor. They can also read or set memory and registers.

These monitors provide ICE (in-circuit emulator)-like capabilities for debugging. Monitors are not free: The penalty for monitor use is that they take up program memory and are intrusive—taking CPU cycles to run.

Easing the transition to new μCs is a new generation of development software—assemblers, compilers, and utilities. Much improved over early generations, these tools have increased reliability and usability. PC-based, many tools are taking on common interfaces and operating characteristics, making it easier to add new tools.

In addition, many tool kits now incorporate μC instruction-set simulators. These simulators let engineers play with a new architecture in a highly controlled simulation environment before tackling the hardware. With a simulator you can interactively monitor your running code.

One advantage of evaluation boards is that they can also serve as low-cost pseudo ICEs. For example, the Motorola evaluation modules also serve as low-cost ICEs for target μCs running in single-chip mode. They come with a cable that plugs into a target board's μC socket. Programs running under monitor control on the evaluation-module μC can drive a target board via the cable.

Languages make it easier

Another major factor opening up μC use is an increasing use of high-level languages for embedded applications. C is the new de facto high-level language for embedded systems. High-quality C compilers are available for embedded μCs such as the 8051, the 68HC11, and even the 68HC05. With C, users can move algorithms and large blocks of code between μCs. However, there are portability problems with μC-specific code, especially with memory segmentation and peripherals.

C, however, doesn't have the μC field to itself. Two major language competitors are Basic and Forth. The 8051, 68HC11, and Z80 have solid public-domain Basic interpreters. There are also higher-performance Basic compilers for the 8051 from Systronix Inc and Binary Technology Inc.

Forth implementations exist for most older μCs and μPs. Forth code is generally processor independent, with special word (procedure) versions for μC-specific hardware. There are commercial versions of Forth for the Z80 and 68HC11 from LMI Microsystems Inc, as well as a public-domain 8051 version of Forth (on the Signetics bulletin board).

For those 8-bit μC programmers more comfortable with a Pascal-like coding style, PC-based Modula-2 is available for both the 68HC11 and the 8051. Introl Corporation supplies a solid Modula-2 for embedded applications. Vail Silicon Tools Inc is introducing a Modula-2/51 compiler for the 8051, with an editor, assembler, and windowed debugging environment.

Getting started easily

Getting started on a new microcontroller (μC) has some barriers to overcome. These include learning its architecture, a new instruction set, and the μC peripherals and how to use them. Databooks are notoriously dense reading. Here are some books for a quick start:

The 8051 Microcontroller: Architecture, Programming, and Applications by Kenneth J Ayala, West Publishing, Minneapolis, MN, 1991. $49.

This is an excellent professional introduction to the 8051 μC. The book discusses simple hardware and software applications with sample code. Applications include Keypads, LCDs, D/A, A/D, and serial communications. A limited 8051 simulator/debugger and an assembler come with the book, letting you try out 8051 programs without hardware.

Single- and Multiple-Chip Microcomputer Interfacing by GJ Lipovski, Prentice Hall, Englewood Cliffs, NJ, 1988. The book costs $34.90, and the laboratory manual costs $12.70. Both are available either directly from Motorola or from bookstores.

This set is a beginning class text for μC applications with some elementary material. The book may be for beginners, but it includes excellent code and logic-design examples. It provides a fast start-up for the 68HC11 μC.

Modula-2 code generally matches 8051 C efficiencies.

But languages are only a means to effectively use the underlying μC hardware. Engineers must analyze the different microcontroller architectures for specific applications. Evaluation boards give them a chance to try out a μC before actually building hardware and coding full applications.

At the low end with the 68HC05

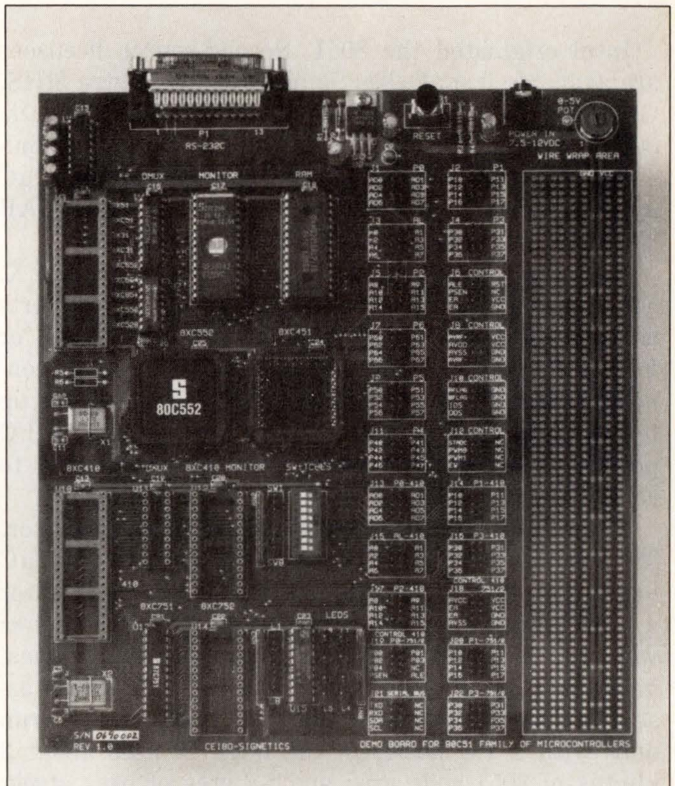
The Motorola 68HC05 is considered by many to be the leading 8-bit μC. It's a minimal architecture with only two active registers (A and X), supplemented by control registers. It is self contained with a minimal pin count: there's no external memory. On-chip memory runs from 2 kbytes to 15,936 bytes of ROM, EPROM, or EEPROM, with 176 bytes of static RAM (SRAM).

The basic 68HC05C4 μC features four I/O ports, a programmable timer (with compares), and two specialized serial-communications ports. Motorola uses the 6805 core in custom ASICs, many of which have become standard parts. Consequently, there are more than 100 variations on the 6805. Chip pin counts for the 68HC05 run from 24 to 40.

Motorola has evaluation boards and modules for the 68HC05: The modules are equipped with a programmer for writing the μC's EPROM. Motorola's 68HC05EVM is built around a 68HC05C9, which has 15,936 bytes of on-chip EPROM. The evaluation module simulates the single-chip mode (on-chip memory) of operation using external memory. User code and data are downloaded into the evaluation module's RAM or pseudo ROM from a host PC or terminal. The μC's ROM is simulated using write-protected, evaluation-module RAM. The μC switches back and forth between the monitor and the user-address maps during execution. There are 16 kbytes of evaluation-module RAM available for each space. Motorola is moving to evaluation systems, 2-board equivalents to evaluation modules, with a personality daughter board for each 6805 μC.

With the evaluation modules, Motorola supplies a terminal emulator, a target monitor for debugging, and a macroassembler. P&E Microsystems Inc supplies these tools. Motorola will soon supply an integrated tool set that combines these packages into a single development environment for the 68HC05. This tool set includes an editor, a debugger, a simulator and a communications link to a monitor-based target system. The debugging interface is the same for both the simulator's and the evaluation module's μC.

Surprisingly, even for a such a simple μC, there's a first-class C compiler: C6805 from Byte Craft. By relying on three built-in expert systems to optimize code, the Byte Craft compiler approaches hand-coded code efficiency. It is a very clean and easy-to-use compiler. C6805 comes with a development environment—E6805 Symbolic Host Support. It is compatible with the evaluation module-based P&E tools.



In addition to a limited assembler/disassembler and symbolic debugger, the DB51 development board has a large prototyping area and easy to reach test points. The board also supports a raft of Signetics 8051 derivative chips.

The 8051 still lives

The 8051 is one of the more popular microcontrollers. It is still a powerful 8-bit architecture with four memory-based memory banks (8 registers per bank), special bit operations (with a dedicated memory area), and a dual-memory space with as much as 64 kbytes each for data and external memory. I/O and peripherals are memory mapped and addressed as Special Function Registers.

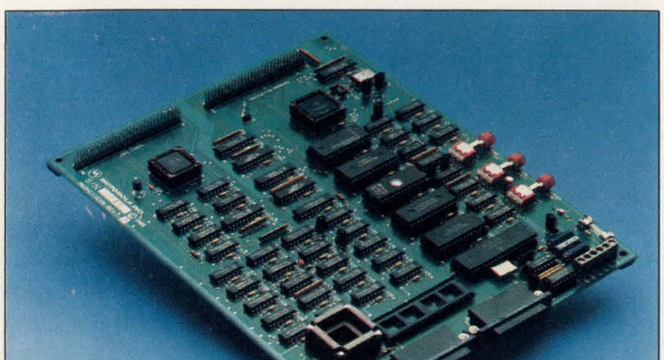
The 8051's instruction set is fairly easy to learn. It has complex addressing, including register indirection, indexing, and immediate forms. External memory references, however, cost an additional instruction cycle, need register indirection, and pass through the accumulator (A).

Intel originated the 8051. Second-source licensees are available from Dallas Semiconductor, Matra MHS, Oki Semiconductor, Siemens, and Philips/Signetics. 8051 applications range from low-end μCs using minimal-pin-count ICs from Signetics to high-end, 8-bit μC applications using advanced 8051s, like the SAB 80C517 from Siemens with a 16/32-bit math unit.

Intel supplies an evaluation board, the EV80C51FX. The board is built around an 80C51FA and supports as much as 64 kbytes of external memory, RAM, or EPROM. Also on board are 10 LEDs which are connected directly to μC output ports and can be lit up to test the I/O-port lines. There are two serial I/O ports, one to link to the host PC and the other to connect to the 80C51FA's UART.

The board comes with an embedded-control monitor. This monitor lets a PC host-based user control μC execution on the evaluation board. With the monitor a user can set as many as 16 software breakpoints as well as read and set registers and memory values, including bits. The software includes a single-line assembler/disassembler. The monitor is designed to run only with a PC host. On the 8051, it uses about 3 kbytes of 8051 code area and 8 bytes of user stack. Signetics sells a range of 8051s, including minimal pin configurations. The Signetics DB-51 development board supports 16 or more 8051 variations, including μCs with the I^2C serial bus. The board comes with a host debugger.

If you want to try the high end of 8051 processing, you can get the EMOD-C517 evaluation board from Siemens. This board is built around the Siemens 80C537 ROMless version of the 80C517. This is an 8051 heavyweight with a 32/16-bit math processor, eight 16-bit pointers, seven I/O ports, and a full collection of timers. The board comes with Franklin Software's ROM monitor, Monitor 51, and a terminal emulation program. Franklin C has been ported to this processor and board. The board furnishes 32 kbytes each for program and external data.



You can directly program or run the Motorola 68HC11EVB μC with on board EPROM and RAM. The evaluation board includes an on board programmer.

The 8051 has solid C compilers. Franklin makes a C development system that delivers efficient code. It comes with a source code debugger, an assembler, and monitor. Commercial simulators and macroassemblers are available from Archimedes and others.

An interesting 8051 evaluation system is Dallas Semiconductor's DS5000KT. Dallas took a new tack, incorporating an 8051 core in a hybrid chip, along with μC peripherals, SRAM (static RAM) for program and data memory, and a battery. The DS5000 chip is a self-contained unit. The chip is easy to program and debug because it uses SRAM—you can just change your code without having to program an EPROM or EEPROM.

The DS5000KT is built around the DS5000 chip. It connects to the host via a phone cable and has a DIP plug for target systems. It runs either stand-alone or as a target board μC. Systronix has ported its BCI51-compiled Basic for the DS5000KT. This compiled Basic is fast and eliminates a lot of μC bookkeeping, such as initialization. It makes a potent development combination with the DS5000KT.

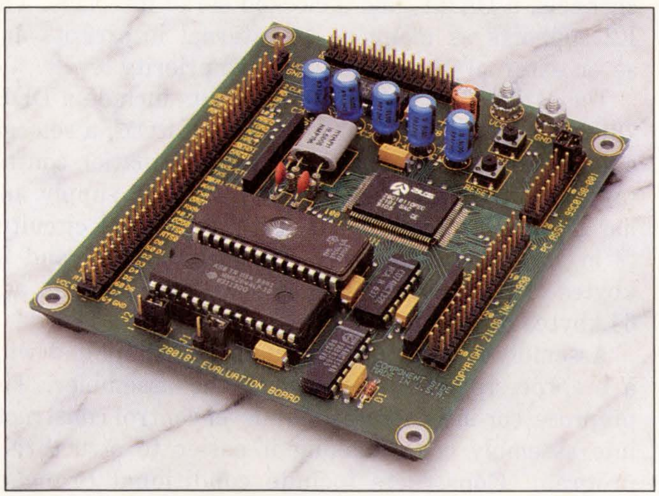
Industrial-strength 8 bits: the 68HC11

Like the 6805, the Motorola 68HC11 is a descendant of the pioneer 6801 μC. It's more complex than the lean 6805 and has a raft of peripherals for industrial control. These peripherals include five 8-bit I/O ports, an A/D converter, a timer system (with a watchdog timeout), and two serial interfaces. The 68HC11 acts as a single-chip μC or accesses as much as 64 kbytes of external memory. However, the 68HC11K4 bank switches out to 1 Mbyte of external memory. Like the 8051, an external pin shifts addressing to external memory, making it easy to build RAM- or EPROM-based debugging systems. Unlike the 8051, there's no penalty for off-chip memory accesses.

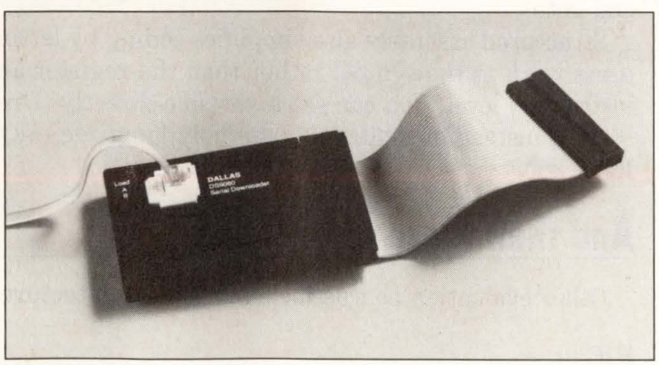
The 68HC11 is a straightforward CPU architecture that has two 8-bit accumulators and four 16-bit registers (X and Y index, SP stack pointer, and a program counter). Two 16-bit index registers ease 64-kbyte addressing for the 8-bit CPU. On chip, the 68HC11 supports as much as 24 kbytes of ROM or EPROM, 640 bytes of RAM, and 1 kbyte of data EEPROM.

Motorola ships evaluation boards and modules for the 68HC11. The modules incorporate programmers to program on-chip EPROM. There are boards and modules for different 68HC11 versions. The 68HC11EVM is built around a 68HC11A1FN chip with an EVBbug monitor EPROM, 16 kbytes of SRAM for user ROM, and 8 kbytes of SRAM for the monitor scratch pad or user EEPROM. The evaluation module links to a PC host for monitor-based debugging. The target-board µC can run in single-chip mode with internal memory or in expanded mode using on board memory. The board accommodates 48-pin DIPs or 52-pin plastic leaded chip carriers (PLCCs).

The evaluation module comes with the Buffalo Monitor and IASM, an integrated debugger, editor, and cross-assembler. IASM, which P&E wrote, is a windowed environment for source-code debugging—monitoring and controlling µC execution. P&E also sells a 68HC11 simulator. The company is integrating



This evaluation board can ring Zilog's Z80181 through its paces. The board holds 32 kbytes of RAM and ROM for the processor. A ROM monitor links control to a PC host.



This evaluation board is a complete system. The Dallas DS5000KT has an 8051 µC, 32 kbytes SRAM, and a backup battery. Systronix Basic or Franklin C can be used for higher-level languages.

IASM and the simulator into a single development environment, which will be supplied with Motorola evaluation modules. With the new tool set, developers will be able to easily shift from simulation to direct execution in the same environment. They can test code in the simulator and then run it directly in the 68HC11 in the same test environment.

A number of C compilers are available for the 68HC11, including one from Motorola. Archimedes Software (San Francisco, CA) has an ANSI C compiler. This compiler is similar to Archimedes 8051 and Z80 versions, making it easy to shift code between the µCs. Archimedes C is very easy to use and has good documentation. Other 68HC11 C compiler vendors include American Automation, Franklin Software, Introl Corp, and Intermetrics.

Visiting an old friend: the Z80

The Z80 is an old engineering favorite and is heavily used in communications and control applications. Zilog has created a set of embedded Z80-based controllers. These include the Z8 and the super Z8 µCs. Second-source Z80 licensees include Hitachi, Goldstar, NEC, SGS Thompson, Sharp, and Toshiba.

Hitachi and Zilog have upped the original 64-kbyte Z80 address space to 1 Mbyte by adding a bank-switching memory-management unit (MMU). The Hitachi HD64180 and the Zilog Z80180 µCs have built-in MMUs and are heavily used in high-level embedded systems. Both rely on off-chip program memory, and have two DMA channels, two UARTs, two 16-bit timers, and a clocked serial port. Zilog further extended the architecture with the Z80180 for communications applications with the Z80180. It is a complete Z80180 with additional peripherals: 16 I/O pins, a counter-timer-controller, and a multiprotocol serial communications channel (like the Z85C30 chip).

The core Z80 architecture is surprisingly robust, with a complex instruction set that puts a lot of capability in the engineer's hands. There are more than 155 instructions, including block moves and memory data searches. The Z80 has a duplicate set of program registers: there are two sets of eight 8-bit registers (A, flag, and six general). The CPU also has four 16-bit registers: two index, a stack pointer and a program counter. These registers simplify 16-bit addressing for the 8-bit CPU.

There are lots of evaluation boards for the Z80 family. One is Zilog's Z80181 evaluation board, which contains a Z80181 µC, 32 kbytes of ROM with the ROM monitor, and 32 kbytes of RAM. Zilog furnishes a terminal-emulator program to control the board. The company also furnishes an assembler and linker/loader for the µC. You can relocate the code to map into the board RAM.

Because of the Z80's popularity, there are numerous software tools, including C compilers, Forth systems, and assemblers. One is the Archimedes' ANSI Z80/Z181C compiler, which includes an assembler, linker/loader, and librarian.

Zilog also fields a highly innovative package for Zilog communications µCs. The Electronic Programmers Manual eliminates a major problem—configuring and using µC peripherals. Using it, you can set up and use the µC peripherals directly without having to get into the details of setting the memory-mapped peripheral-control registers. The manual is implemented in an easy to use, windowed environment. It generates a set of C functions or assembler tables for application code.

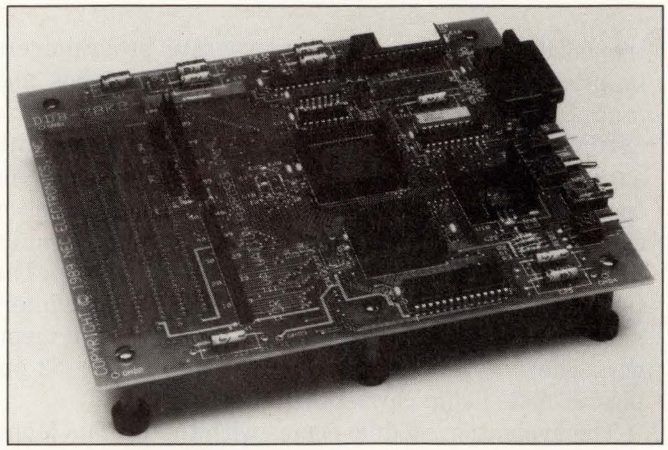
Many keyboard controllers use the Z80. The Z8602 µC is designed for keyboard control and comes with code for PC 101/102 keyboards. If you want to play with keyboard control, the ZD86D2 Keyboard Kit evaluation board holds the Z86602, ROM code, and a set of keyboard keys.

NEC K2: The next generation

The 78K2 series is NEC's second generation of 8-bit microcontrollers. A high-end 8-bit µC, the 78K82xx's CPU can address as much as 1 Mbyte of data memory and 64 kbytes of program memory. K2 µCs hold as much as 32 kbytes of ROM, EPROM, or one-time programmable memory, and as much as 1 kbyte of RAM. The external access bus is similar to an 8085, but with separate spaces for data and program. Some versions hold as much as 512 bytes of EEPROM for program and data constants. With a 12-MHz clock, minimal instruction execution is 333 nsec. The µC packages range from 64-pin DIPs to 74-pin plastic quad flatpacks.

The K2 has an innovative Peripheral Management Unit. A programmer can program the unit to service peripherals directly. In peripheral-management mode, flagged peripheral interrupts don't interrupt program flow or require coding. Instead, the peripheral is serviced as defined by structured tables. The processing is automatic, stealing cycles from the CPU. The macroservice routines transfer data directly between memory and the peripherals independent of program execution.

The K2 has as many as 71 I/O pins. Its peripherals include an A/D converter (8 bits, 16 channels), D/A converter (8 bits, 2 channels), a 16-bit timer, as many as three 8-bit timer/counters, as many as four PWM



This board comes with a ROM monitor, EPROM, and 32 kbytes each of EPROM or ROM and user SRAM. The board holds an additional 64 kbytes of user data ROM. The DDB-78K2 evaluation board supports the NEC K2 8-bit µC.

channels, a UART, and a clocked serial interface. The K2 supports as many as 14 internal interrupts and seven external interrupts with two priority levels.

The NEC µPD782xx evaluation kits include a DDB-78K2-2xx evaluation board, a monitor ROM, a relocatable/structured assembler, and a PC emulation control program. The board comes with a power supply and has a small prototyping area for additional circuitry (9 in.^{2}). The board holds 32 kbytes of ROM and 32 kbytes of RAM. For larger applications, you can add 64 kbytes of data RAM.

Assembly-language programming is simplified with a preprocessor that comes with the assembler. The preprocessor incorporates high-level control constructs into assembly code, making it easier to structure a program. Constructs include conditional branches (if_elseif_endif, if_bit_elseif_endif, and switch_case), loop control (for_next, while_endw, repeat_until, and repeat_until_bit), and loop breaks (break, continue, and goto).

Structured assembly also simplifies coding by letting users work at the symbol rather than the register and instruction level. You can set a variable directly (Drek = #7), instead of coding K2 assembly language (MOV Drek,#7).

And then there were more

Other evaluation boards include these architectures:

PIC

Microchip Technology's PIC 16C5x 8-bit µC is a third-generation, low-end µC. The PIC architecture traded simpler internal structures—pipelining, Har-

Table 1—Representative 8-bit evaluation boards

Vendor	Microcontroller (μC)	Hardware	Software	Price	Comments	Circle number[3]
Dallas Semiconductor	DS5000	DS5000KI		$160	The DS5000 chip is a system with 32-kbyte SRAM and battery backup. It comes with an emulation plug, and you can plug it into the target system and control it with a monitor.	662
4350 Beltwood Pkwy Dallas, TX 75244 (214) 450-0400 FAX (214) 450-0470	12 MHz 32-kbyte SRAM[1] on-chip battery	Emulation plug ZIF socket	Host loader (loads, interrogates μC) basic compiler (optional)			
Echelon Corp	Neuron 3150	Lonbuilder Starter Kit		$17,995	This is a hardware/software development environment for the Neuron distributed control chips made by Toshiba and Motorola. The company offers a lease/rental program.	663
4015 Miranda Ave Palo Alto, CA 94304 (415) 856-6153	10 MHz 10-kbyte ROM 2-kbyte RAM 512-byte EEPROM[2]	64-kbyte RAM 64-kbyte control RAM 2 ICEs 2 nodes	Assembler Neuron-C linker/loader source debugger network manager protocol analyzer			
Intel Corp	80C51FC	EV80C51FX		$260	iRiSM-integrated monitor and host interface.	664
Embedded Processor Group 5000 W Chandler Blvd Chandler, AZ 85226 (602) 554-2649	16 MHz 32-kbyte ROM 256-byte RAM	32-kbyte SRAM configurable board programmable LED sensor	Line assembler/disassembler symbolic debugger iRiSM-monitor/terminal emulator			
Microchip Technology Inc	PIC17C42	EDP-17		$395	3-digit LED display for test. 16-bit instruction word, 8-bit registers/ALU (250-nsec instruction cycle).	665
2355 W Chandler Blvd Chandler, AZ 85224 (602) 963-7373 FAX (602) 899-9210	16 MHz 4-kbyte EPROM 232-byte RAM	64k×16-bit SRAM or EPROM EPROM Programmer Wrapped-wire area	Linker/loader assembler			
Motorola	68HC05C4	M68HC05EVM		$500	Can use as a pseudo ICE. Software package from P&E integrates the assembler/editor/simulator/debugger. Onboard programmer accommodates 40-pin DIPs, 44- and 52-lead PLCCs.	666
Microprocessor Products Group 6501 William Cannon Dr W Austin, TX 78735 (512) 440-2000	4 MHz 4-kbyte ROM 176-byte RAM	16-kbyte monitor EPROM 8/16-kbyte user pseudo ROM programmer emulation pod	Integrated communications/ assembler/editor source-code debugger monitor			
	68HC11A8	M68HC11EVM		$500	Can use as a pseudo ICE. Software package from P&E integrates the assembler/editor/debugger/simulator. Onboard programmer handles 48-pin DIPs, 52-lead PLCCs.	667
	4 MHz 8-kbyte ROM 256-byte RAM 512-byte EEPROM	8-kbyte monitor EPROM 8/16-kbyte user pseudo ROM programmer emulation pod	Integrated communications/ assembler/editor source-code debugger monitor C compiler (optional)			
National Semiconductor Corp	COP800	COP800 Designers Kit		$295	First pass kit with assembler and simulator.	668
2900 Semiconductor Dr Santa Clara, CA 95051 (408) 721-5000 FAX (408) 730-0764	10 MHz 4-kbyte ROM 128-byte RAM	(Simulation kit)	Assembler simulator symbolic debugger			
NEC Electronics Inc	μPD78213	DDB-78K2-21X		$295	Wrapped-wire area. Can add 64-kbyte ROM. Comes with ac/dc power supply.	669
401 Ellis St Mountain View, CA 94039 (415) 960-6000 FAX (800) 729-9288	12 MHz 16-kbyte EPROM or ROM 512-byte RAM	96-kbyte ROM 32-kbyte RAM	Assembler link/loader monitor symbolic debugger C compiler (optional)			
Oki Semiconductor Inc	65511	EVA65K		$300	16 programmable LEDs 8 assignable DIP switches assignable potentiometer μC is redesign of 8051. Has 400-nsec instruction cycle and 64-kbyte address spaces.	670
650 N Mary Ave Sunnyvale, CA 94086 (408) 720-1900	10 MHz 4-kbyte ROM 128-byte RAM	32-kbyte SRAM 16 programmable LEDs assignable DIP switches potentiometer	Line assembler/disassembler monitor			
SGS-Thompson Microelectronics Inc	ST-6220	ST-6 Starter Kit		$195	Elegant μC programming system with a simulator to try code. Comes with four μCs.	671
1000 E Bell Rd Phoenix, AZ 85002 (602) 867-6259	8 MHz 3876-byte ROM 64-byte RAM	μC EPROM programmer only	Assembler linker/loader source-code debugger simulator			

Notes: 1. SRAM=Static RAM
2. EEPROM=Electrically erasable PROM
3. For more information on 8-bit evaluation boards such as those described in this table, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request Service.

Table continued

vard architecture, load/store, and fixed-length instructions—for faster instruction execution. It has a 2-stage pipeline with only 33 instructions. Programs are held in on-chip EPROM of 512 to 2k 12-bit words. And there are as many as 80 bytes of on-chip RAM. PIC peripherals include an 8-bit counter, watchdog timer, and as many as 20 I/O pins. Pin counts run from 18 to 28 pins.

Microchip has brought out a higher-level PIC, the PIC17C42. It is a 16/8-bit μC, with 16-bit instructions (as many as 64k words) and 8-bit data (as much as 64 kbytes). On-chip memory is 2k words of EPROM and 256 kbytes of data SRAM. It has 55 instructions.

The PICPAK-17 is an evaluation board and programmer for the PIC17C42. It provides two external EEPROMs to hold program memory. These EEPROMs hold the object code to program the μC's internal EPROM. You can use SRAMs on the board as well. The board has a small prototyping area, as well as a 3-digit, 7-segment display for testing I/O.

TI TMS370

TI's TMS370 is a simplified architecture for low- to mid-size applications. It has a 64-kbyte address space, with as much as 16 kbytes of on-chip program ROM or EPROM, and as much as 512 bytes of RAM. Also, it has as much as 512 bytes of EEPROM for data constants. The TMS370 has three external interrupts for real-time applications.

Table 1—Representative 8-bit evaluation boards *(continued)*

Vendor	Microcontroller (μC)	Hardware	Software	Price	Comments	Circle number[3]
Siemens Components Inc Semiconductor Group 2191 Laurelwood Rd Santa Clara, CA 95054	80C517 12 MHz 32-kbyte EPROM or ROM 2-kbyte RAM	EMOD-C517: 16-kbyte EPROM 32-kbyte RAM (+ optional 32 kbytes)	Terminal emulator line assembler	$250	Can test high-end 8051—with 16/32-bit math unit, eight 16-bit pointers and seven I/O ports.	672
Signetics 811 E Arques Ave Sunnyvale, CA 94088 (408) 991-2000 FAX (408) 991-2311	8051 family 12 MHz 4-kbyte ROM 256-byte RAM	Ceibo BD-51: 32-kbyte RAM 32-kbyte EPROM potentiometer programmable LED bank 8 switch bank for I/O	Loader symbolic debugger monitor	$320	8-pin plastic leaded chip carrier. Supports Signetics 8051 family. Serves 24-, 48-, 40-pin DIPs and 68-pin plastic-leaded-chip carrier wrapped-wire area.	673
Texas Intruments Inc Box 1443, MS 719 Houston, TX 77251 (713) 274-2000 FAX (713) 274-2445	TMS370C356 20 MHz 16-kbyte ROM or EPROM 512-byte RAM 512-byte EEPROM	TMS370 Design Kit: 16-kbyte ROM 512-byte RAM 512-byte EEPROM programmer	Terminal emulator symbolic/source debugger	$370	Handles all TMS370 devices.	674
	TMS7000 6 MHz 4-kbyte ROM 256-byte RAM	TMS 700 EVM: 32-kbyte RAM 24-kbyte EPROM programmer	Assembler terminal emulator symbolic/source debugger	$795	Simple 2-register μC architecture. Low- to mid-range μC, 1.25-μsec minimum instruction cycle at 6 MHz.	675
Toshiba America Inc Semiconductor Products Div 9775 Toledo Way Irvine, CA 92718 (714) 455-2000	TLCS-90 12.5 MHz 32-kbyte ROM 1-kbyte RAM	EDB-90: 256-kbyte EPROM 256-kbyte RAM Darlington drivers for stepper motors Analog bus for A/D converter	Assembler source-code debugger linker/loader C compiler monitor	$400	The TLCS-90 series comprises high-end μCs. The μCs are register oriented, with a 320-nsec minimum instruction cycle. 64-kbyte instruction and 1-Mbyte data-address space. Wrapped-wire area, 13 programmable LEDs.	676
Zilog Inc 210 Hacienda Ave Campbell, CA 95008 (408) 370-8000	Z80181 12.5 MHz MMU (to 1 Mbyte memory) no on-chip memory	Z8018100ZC0: 32-kbyte EPROM 8-kbyte SRAM	Assembler link/loader monitor (in EPROM, + source code)	$150	Z80181 smart access controller for communications. Board header for expansion software to set up peripherals.	677
	Z08602 4 MHz 2-kbyte ROM 124-byte RAM	Z0860200ZC0: Three LEDs two 8-position-DIP software	Assembler link/loader monitor keyboard-control code	$231	Keyboard controller. Comes with software (EPROM and source code). Board has miniature keyboard on it. Models 101/102 are PC keyboards.	678

Notes: 1. SRAM=static RAM
2. EEPROM=Electrically erasable PROM
3. For more information on 8-bit evaluation boards such as those described in this table, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request Service.

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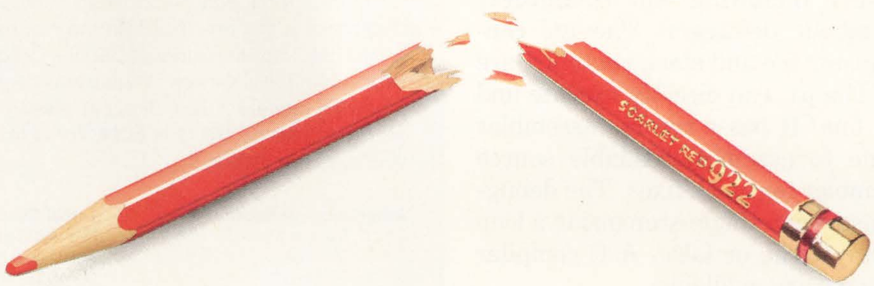

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The TMS370 application board uses two TMS370 μCs: a master controller for the host interface, and a slave as the target interface. The board takes one of three different slave μCs (28-pin DIP, 28-pin PLCC, or 68-pin PLCC). It supports both EEPROM and ultraviolet EPROM memories, as well as RAM for code and data. You can directly program the EEPROMs and EPROMs. There is also a wrapped-wire prototyping area for additional circuitry.

The board comes with a PC-based, window-oriented development tool set, including an assembler, disassembler, and symbolic debugger. The μC contents, including its register file and stack contents, are visible via a monitor. The μC can directly execute and define expressions on line. It has a reverse assembler to convert object code to assembly-readable source code, and a patch assembler for quick fixes. The debugger is sophisticated—users can single-step inside a loop while an expression stays true or false. A C compiler and source code debugger are available.

ST6

The SGS ST6 is a low-end, single-chip μC, with as little as 20 pins. The μC holds 2 to 4 kbytes of on-chip EPROM or ROM and 64 bytes of RAM. The μC has no off-chip memory bus. It's a simple, minimal register architecture with an accumulator, four memory registers, and a 12-bit PC. The μC supports as many as 21 external interrupts. Peripherals include an A/D with as many as 16 input channels, one or two 8-bit timers, a watchdog timer, and LCD drive capability. Running at 8 MHz, an average instruction takes 13 clocks for execution.

SGS doesn't make an evaluation board. Instead, they furnish a low-cost programmer, complete with PC-based development software. The ST6 starter kit includes a programmer board and three windowed EPROM ST6 μCs. The board links to a PC for downloading code into a μC. The development software includes a 1-pass, macroassembler, a loader, and a simulator.

National COP800

The National COP800 family consists of low-end μCs. Pin counts range from 20 to 44 pins and have 39 I/O lines. Running at 10 MHz, the minimum instruction execution time is 1 μsec. The COP800 is built around a minimal register set—A, B, and index—along with Stack Pointer, Control, and Program-Status Word registers. The COP800 has a Harvard architecture with a single, 32-kbyte address space. The μC has 1 to 8 kbytes of ROM or EPROM and 64 to 256 bytes of SRAM on chip. Versions with as much as 4 kbytes of program EEPROM are also available. The μC family includes a programmable UART, PWM timers, a watchdog timer, an 8-bit A/D converter, and a proprietary serial I/O scheme. The device supports as many as 16 interrupts.

For initial evaluation, National furnishes a COP800 Designer's Tool Kit. This kit includes an assembler

For more information . . .

For more information on software such as the programs described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN. For a listing of hardware vendors, see **Table 1**.

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Byte Craft Ltd
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FAX (519) 746-6751
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Franklin Software Inc
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San Jose, CA 95129
(408) 296-8051
FAX (408) 296-8061
Circle No. 654

Hitachi America Ltd
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FAX (415) 583-4207
Circle No. 655

Intermetrics Microsystems Software Inc
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Cambridge, MA 02138
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Milwaukee, WI 53204
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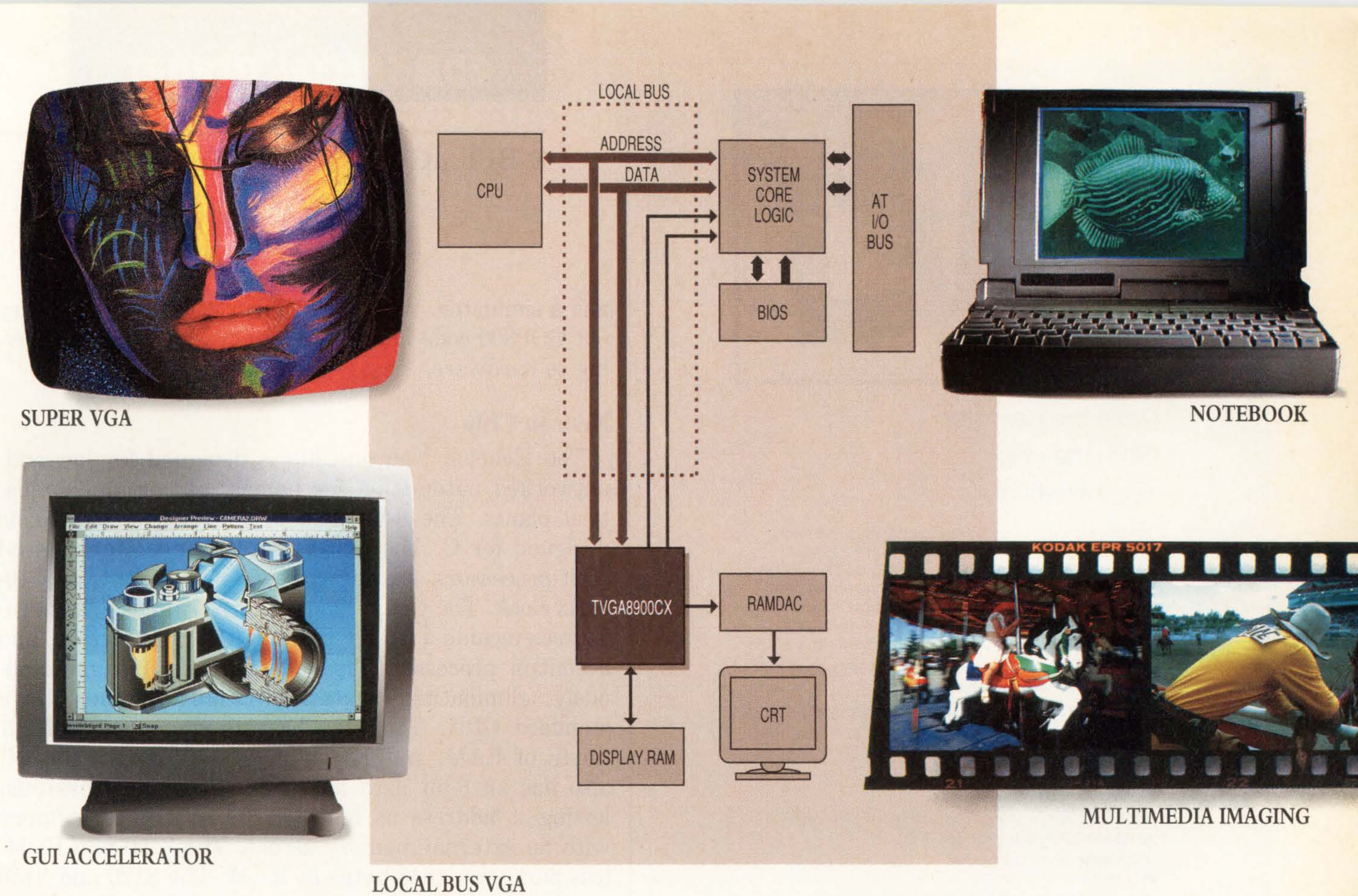

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and a simulator. With the simulator, engineers can try out COP800 code in a secure environment before moving to hardware.

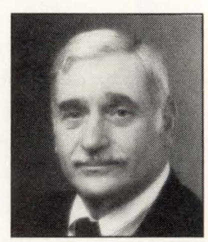
Neuron Chip

The Echelon Neuron-Chip is designed for low-end, networked automation for homes, offices, and industrial plants. The 8-bit chip is one of the first to be designed for C. The μC consists of three interleaved 8-bit processors, sharing common resources with a 10-MHz clock. The CPUs time-share resources. These resources include a main CPU, a network processor, and a control processor. Three tasks can run simultaneously, eliminating the task-switching overhead in a standard CPU. The 3120 has 10 kbytes of ROM, 1 kbyte of RAM, and 412 bytes of EEPROM. The μC also has an 8-bit data bus and a 16-bit address bus, letting it address as much as 64 kbytes of memory with no external memory access. The 3150 is a ROM-less part with 2048 bytes of RAM. The 3120 and 3150 are built by Motorola and Toshiba as Echelon licensees.

Echelon's Neuron C is an extended C for programming Neuron chips. Neuron C has built-in functions and scheduling for network communications and control I/O. Echelon is fielding a complete development environment, Lonbuilder's Developers Workbench, for network-control applications. The environment includes PC-host software with a Neuron C and a source-code debugger, a network manager, a protocol analyzer, and two emulators. Lonbuilder can support as many as 32,000 nodes. Echelon has transceivers for twisted pair, RF, and power-line media. EDN

Author's biography

Ray Weiss, one of EDN's West Coast Technical Editors, can be reached at (818) 704-9454.



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5x5x11.5"	1000W	5V/120A	5-15V/20A	5-15V/20A	5-24V/5A	5-24V/5A
5x8x11"	1000W	5V/150A	5-15V/20A	5-15V/20A	5-24V/10A	5-24V/10A
5x8x11.5"	1500W	5V/200A	5-15V/20A	5-15V/20A	5-24V/10A	5-24V/10A
5x8x13.75"	2500W	5V/400A	5-15V/20A	5-15V/20A	5-24V/10A	5-24V/10A

Single Output Models *(Partial Listing)*

Size	Total	Output Voltage Range/Max. Amps (select one)				
(HxWxL)	Watts	2-4VDC	4-6VDC	7-12VDC	12-28VDC	28-56VDC
5x6.5x10"	750W	2-4V/187A	4-6V/150A	7-12V/63A	12-28V/27A	28-56V/14A
5x5x11.5"	1000W	2-4V/250A	4-6V/200A	7-12V/84A	12-28V/36A	28-56V/18A
5x8x11.5"	1500W	2-4V/375A	4-6V/300A	7-12V/125A	12-28V/54A	28-56V/27A
5x8x11.5"	2000W	2-4V/400A	4-6V/400A	7-12V/167A	12-28V/72A	28-56V/36A
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CIRCLE NO. 55

Programmable device masters the art of high-speed data transfers

Vinita Singhal, Altera Corp

The Micro Channel Architecture defines a high-speed data-transfer protocol for moving data between a bus master and a slave. Implementing this protocol in programmable logic gives you design flexibility in addition to high-speed data transfers.

Recent enhancements to the Micro Channel Architecture bus have created a system that supports independent bus masters. One of the main enhancements is the streaming-data procedure (SDP), which allows faster data transfer. Implementing this protocol needn't greatly complicate your design. You can generate essential signals for a bus-master adapter with SDP capability using an EPLD-based design. (Check the EDN BBS for an Altera Hardware Description Language state-machine description of this circuit.)

Streaming is a high-speed data-transfer mode for data (bytes, words, or double words) that reside at consecutive address locations. An SDP cycle needs only the starting address; the protocol assumes subsequent data packets are at sequential addresses. One streaming-data cycle consists of multiple 16-, 32-, or 64-bit sequential data transfers. The cycle time for each packet transfer is half (100 nsec) that of the default (zero-wait-state, 200-nsec) cycle. The streaming-data procedure is transparent to devices that do not use or transmit the data. Streaming-data participants must support basic transfer to operate with nonstreaming-data participants.

The SDP increases data-transfer rates by a factor of 2, 4, or even 8 over the 5 Mbyte/sec baseline bus throughput (which assumes 8-bit transfers). Any bit in the POS (programmable-option-select) register space can enable SDP. Data streaming can occur only by mutual consent between a master and a slave device and requires several signals. These signals are:

Signal	Description
-SDR(0)	Streaming-data request bit 0; input to MCA_BM_EPLD
-SDR(1)	Streaming-data request bit 1; input to MCA_BM_EPLD
-MSDR	Multiplexed streaming-data request; for 64-bit SDP using address and data buses
-SD STROBE	Streaming-data strobe; MCA_BM_EPLD output
CD CHRDY	Card channel ready; from slave adapter to MCA bus
CHRDYRTN	Card channel ready return; input to MCA_BM_EPLD (generated by the system as a logical AND of all adapter CD CHRDY signals)
-CD DS 16	Card acknowledge, 16-bit data stream
-CD DS 32	Card acknowledge, 32-bit data stream

The following streaming-data-signal combinations (X is "Don't Care") are valid:

-SDR0	-SDR1	-CD DS 16	-CD DS 32	-MSDR	Description
0	0	X	X	X	Reserved
0	1	0	0	0	64-bit SDP
0	1	0	0	1	32-bit SDP
0	1	0	1	1	16-bit SDP
1	0	X	X	X	Reserved
1	1	X	X	X	Basic transfer

The software listings in this article are available on EDN's computer bulletin-board system (BBS). Phone (617) 558-4241 with modem settings 300/1200/2400,8,N,1. Access */freeware* SIG and specify *(r)ead* option followed by *(k)eyword* search for "MS #346."

Although the Micro Channel Architecture specification permits data transfers between unequal bus widths, it does not direct unequal bit-width data through the data-byte lanes during the SDP; the master or slave must implement this control. In general, the wider side of the transfer controls where the data end up. For example, in the case of a 16-bit master executing streaming-data transfers with a 32-bit slave, the slave provides steering control.

Five signals control the bus

Once a bus master gains control of the bus, it drives all bus-control signals and the address and data buses. On the Micro Channel Architecture bus, a bus master must drive five bus-control signals. These signals are the -S0 and -S1 status signals; the -ADL address decode latch; the -CMD command strobe; and the M/-IO memory or I/O-cycle indicator.

Fig 1 illustrates a complete interface to the Micro Channel Architecture bus using three major functional blocks: An I/O or memory slave interface, an arbitration-controller block (both available from Altera and several other sources), and the MCA_BM_EPLD (Altera's Micro Channel Architecture Bus Master Erasable Programmable Logic Device), which implements bus-master control logic having SDP capability.

When the arbitration controller signals to the MCA_BM_EPLD, using -BUSGNT, that the EPLD has won the bus, the EPLD drives the bus-control signals. If you enable streaming-data capability (via a POS register bit), the MCA_BM_EPLD determines whether the slave can perform streaming operations. If so, the MCA_BM_EPLD generates the -SD STROBE (streaming-data strobe) signal. If the slave introduces wait states (CD CHRDY = low), -SD STROBE continues to strobe; however, the master maintains data on the bus until the slave activates CD CHRDY.

The MCA_BM_EPLD is a synchronous state machine that runs off a 20-MHz clock (CLK_20) and gen-

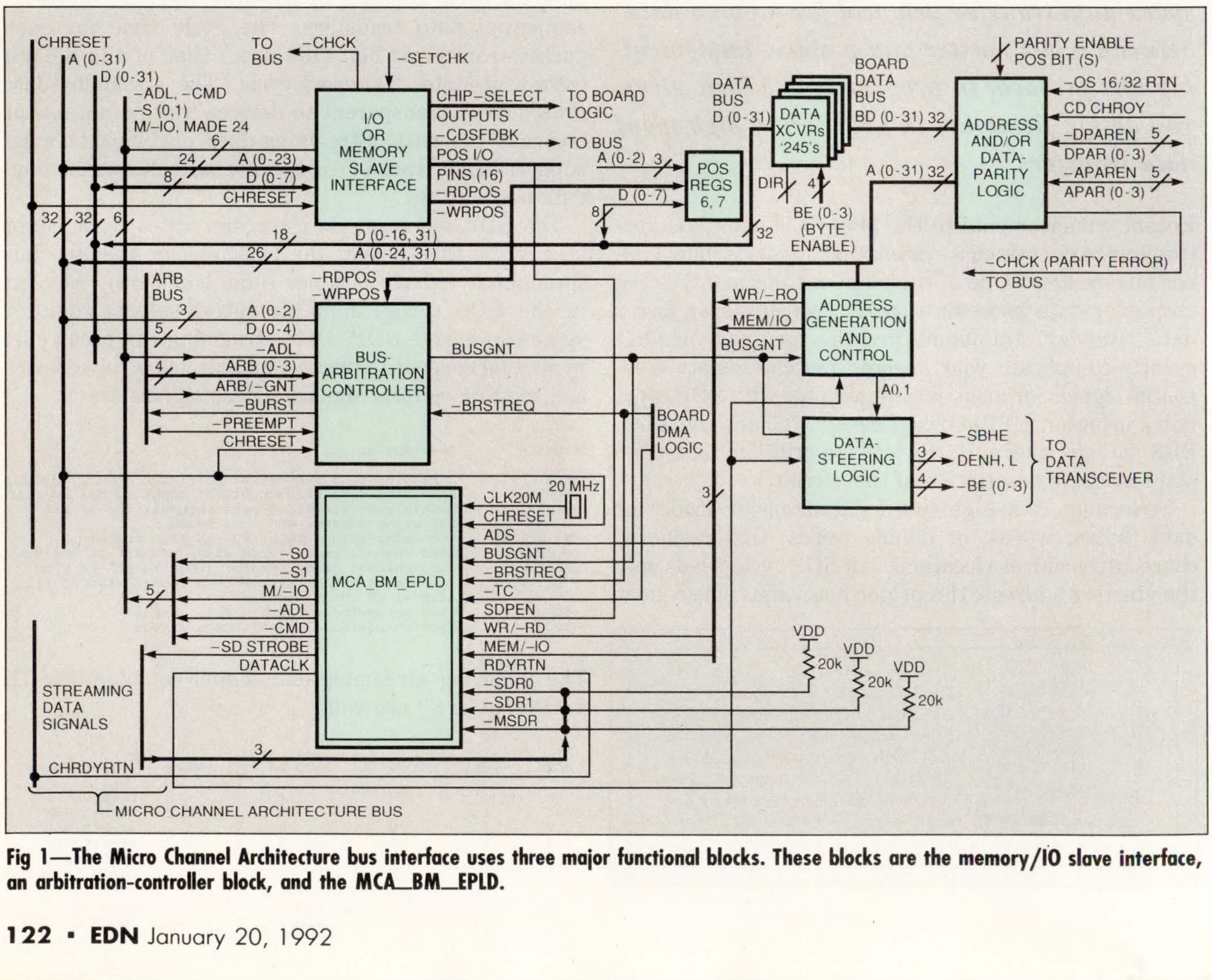

Fig 1—The Micro Channel Architecture bus interface uses three major functional blocks. These blocks are the memory/IO slave interface, an arbitration-controller block, and the MCA_BM_EPLD.

erates the signals necessary for a bus master with streaming-data-transfer capability. These signals are:

Signal	I/O	Description
-ADL	O	Micro Channel Architecture address-decode latch
-CMD	O	Micro Channel Architecture command strobe
-S0	O	Micro Channel Architecture status signal bit 0
-S1	O	Micro Channel Architecture status signal bit 1
M/-IO	O	Micro Channel Architecture memory I/O signal
-SD STROBE	O	Micro Channel Architecture streaming-data strobe
DATA_CLK	O	Master internal clock; to board logic
-ADS	I	Address stable; from CPU or controller or address-generator logic
BUSGNT	I	Bus arbitration controller output; signals bus won
-BRSTREQ	I	Board logic; burst request
-TC	I	Board logic/Micro Channel Architecture; terminal count
CHRESET	I	Micro Channel Architecture channel reset
CLK_20M	I	20-MHz synchronizing clock
WR/-RD	I	Write/read from CPU/controller or address-generator logic
MEM/-IO	I	Memory or I/O cycle; generated by CPU or DMA controller or address generator
-SDR0	I	Micro Channel Architecture streaming-data request bit 0
-SDR1	I	Micro Channel Architecture streaming-data request bit 1
-MSDR	I	Micro Channel Architecture multiplexed streaming-data request (64-bit streaming-data transfers)
RDYRTN	I	Micro Channel Architecture CD CHRDYRTN
SDPEN	I	From any user-defined POS bit

Within an SDP cycle, the -SD STROBE clock times each transfer. SDP cycles are of several types that depend on the conditions under which the SDP commences and whether the slave introduces wait states. These types are deferred cycle, where the SDP start is delayed; data pacing, where wait states are inserted in SDP cycles; and combined deferred cycle and data pacing. Additional SDP qualification depends on how the cycle is terminated. Termination can be requested by the master, the slave, or by the master because the slave isn't ready. The MCA_BM_EPLD supports all variations of the SDP cycles.

The MCA_BM_EPLD's outputs are decoded as a function of the present state. The next state results from the present state and the inputs. The main states of the MCA_BM_EPLD state machine **(Fig 2)** are:

State	Description
IDLE	Idle; wait for cycle start
STATUS	Cycle start; drive status signals
ADLTCH	Generate address-decode latch
BXFER	Distinguish the cycle to be nonstreaming
WAIT	Determine synchronous or asynchronous extended
CMDCLK1	Default cycle timing state
SYNEXT	Synchronous-extended cycle
SYNEXT1	Synchronous-extended cycle timing state
ASYNEXT	Asynchronous-extended cycle
SDDEFCYC	Deferred start for SD cycle
SD STROBE	Streaming-data strobe (active low)
STRBHI	Streaming-data strobe (high)
MTERM	Master-terminated SD cycle
STERM	Slave-terminated SD cycle
MSTERM	Master-terminated SD cycle; slave not ready
MSTRBHI	Streaming-data strobe (high; slave not ready)
CMDTR1	Trailing edge of -CMD
EBC	End of basic transfer cycle
ESDC	End of streaming-data-transfer cycle

Several details of the state-transition diagram in **Fig 2** are worth emphasizing.

The signals -BUSGNT and -BRSTREQ tell the

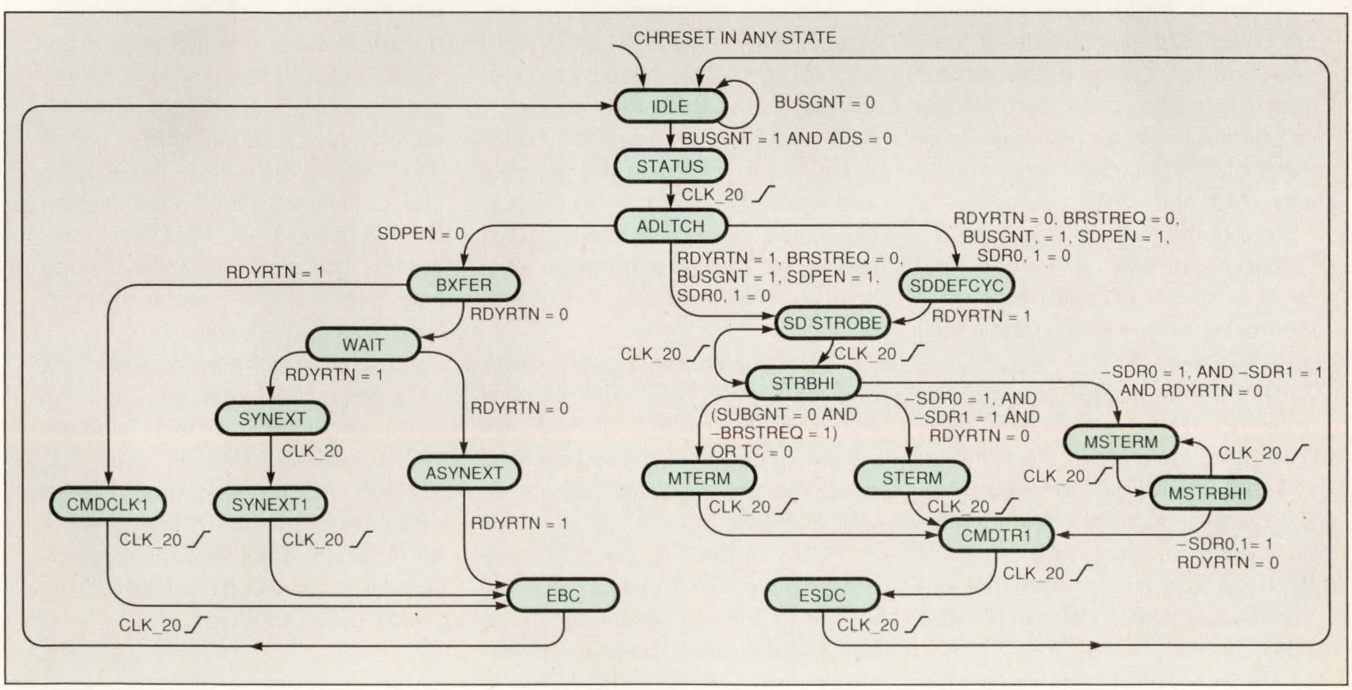

Fig 2—The bus-master state machine contains 19 states that perform streaming- and nonstreaming-data transfers.

MCA_BM_EPLD when it is the bus master for block (burst) transfers. -BUSGNT is an output from the Micro Channel Architecture bus-arbitration controller logic signaling that the EPLD has won the bus. The -BRSTREQ input to the arbitration controller indicates an active -BURST transfer request.

-ADS starts the transfer cycle

The -ADS input to the EPLD **(Fig 1)** indicates a valid address on the address bus. Functionally, -ADS is similar to the -ADS signal on the 80386 processor. This signal indicates the start of a data-transfer cycle and the MCA_BM_EPLD device uses it to latch the state of the WR/-RD and MEM/-IO signals. Subsequently, the MCA_BM_EPLD drives the status and control signals. The EPLD decodes the status signals (-S0 and -S1) and M/-IO from the state of the write/read signal (WR/-RD) and MEM/-IO inputs, respectively. One cautionary note, the Micro Channel Architecture bus doesn't provide pullup resistors for the streaming-data-related signals (-SDR0, -SDR1, -MSDR, and -SD STROBE). As a result, adapters that receive these signals must provide pullup resistors for each signal. The Micro Channel Architecture specification recommends a minimum of 20-kΩ pullup to 5V dc.

The DATA_CLK output on the MCA_BM_EPLD device provides stretched-out -SD STROBE pulses by tracking the status of the CHRDYRTN signal. The address and byte-count increment logic can use DATA_CLK directly. However, when -MSDR is low, indicating 64-bit data streaming, the Micro Channel Architecture specification (and hence, the MCA_BM_EPLD) does not support data pacing. In this case, the DATA_CLK output is identical to the -SD STROBE output.

The bus-master transfer controller indicates termination of the SDP cycle to the MCA_BM_EPLD device by either of two conditions. One condition is the deactivation of BUSGNT followed by deactivation of the -BRSTREQ signal. If the master is -PREEMPTed or no longer needs the bus, the bus-arbitration controller deactivates BUSGNT. If another device

Designer's do's and don'ts

The following design pointers highlight important information gleaned from Micro Channel-related literature. They are summarized here for your convenience.

1. When a master gains control of the channel, it must initiate at least one transfer cycle. If the master must abort the cycle, it activates -S0 and -S1 with the minimum pulse width of 85 nsec and does not activate -ADL and -CMD.
2. To exit the inactive state, the arbitration controller of the bus master must sense -PREEMPT high after the trailing edge of the status line(s) goes inactive.
3. The system master can perform data transfers, and system logic can perform refresh operations, while ARB/-GNT is in the ARB state. Selected slaves must respond independently of the state of ARB-/GNT. A bus master must not run cycles when ARB/-GNT is in the ARB state.
4. Status-signal timing during streaming-data transfers is completely different from nonstreaming-data transfers. So don't use status signals -S0 and -S1 to hold CD CHRDY low.
5. Because programmable-option-select (POS) register 2, bit 0 (card enable) can be modified by the system, don't use it for device reset.
6. If possible, don't use the Fixed-Resources keyword in the adapter description file. Contrary to the purpose of POS, the keyword indicates resources that the adapter must have, such as hardwired INT or ARB levels.
7. The byte-enable signals -SBHE and -BE0, -BE1, -BE2, and -BE3 are not mutually exclusive. A 32-bit master talking to a 16-bit slave must drive the byte-enable signals as well as -SBHE.
8. POS's register space is I/O address space XXX0 to XXX7 (hex).
9. The T79 timing parameter specifies the maximum time length for streaming-data transfers. For a master-terminated cycle, the master must de-assert -S0 and -S1, to indicate end of cycle, within 7.8 μsec (max) from -CMD active (start of cycle). Therefore, the master must signal termination of the streaming-data transfer within 7.8 μsec from -CMD active. However, the Notes section in the Micro Channel Architecture specification adds that if -PREEMPT goes active, the master can continue to hold the channel for 7.8 μsec from -PREEMPT, indicating that basic transfer cycles may continue after streaming-data transfers are complete.
10. The Micro Channel bus doesn't provide pull-up resistors for the streaming-data-related signals -SDR0, -SDR1, -MSDR, and -SD STROBE. Adapters receiving these signals must provide a pullup resistor for each signal. The MCA specification recommends a minimum of 20-kΩ pullup to 5V dc.

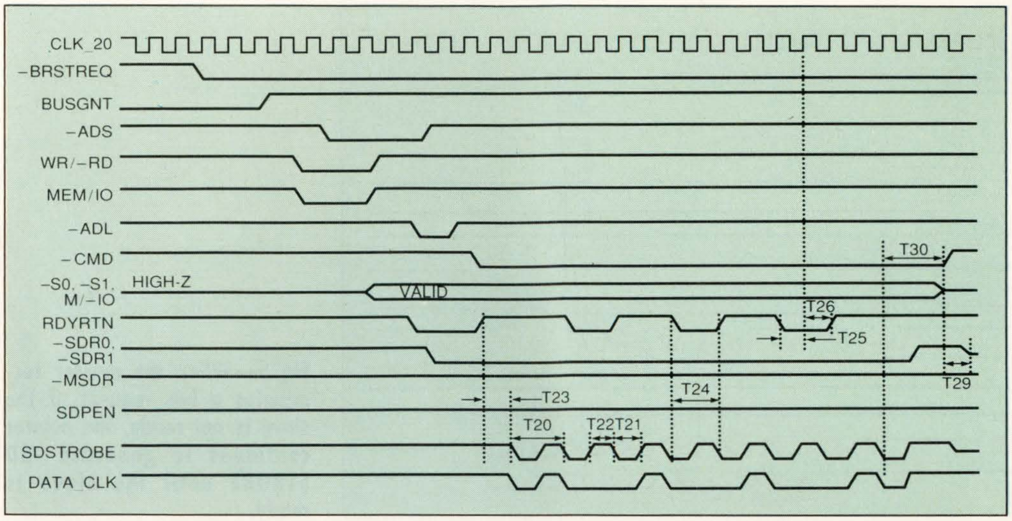

Fig 3—This diagram illustrates the timing of a 16- to 32-bit streaming-data transfer, with deferred start and data pacing, terminated by the slave.

-PREEMPTs the bus master, the adapter has up to 7.8 μsec to complete transfers. Under -PREEMPTion, the arbitration controller de-asserts BUSGNT but may continue to assert -BURST on the Micro Channel bus. You can use the falling edge of BUSGNT to start a 7.8-μsec timer to monitor the requesting device's de-assertion of its bus request (-BRSTREQ). To maximize bus throughput, the MCA_BM_EPLD uses BUSGNT inactive and -BRSTREQ inactive to terminate the cycle. The second termination condition is an active low pulse on the -TC input pin. The local-transfer controller generates this active-low, terminal-count signal to indicate the last streaming-data-transfer cycle.

According to the Micro Channel specification, a slave that introduces wait states during SDP should not de-assert -SDR0 and -SDR1 while CD CHRDY is inactive. Following an active CD CHRDY, the slave may de-assert the -SDR0 and -SDR1 signals. This restriction leads to the "Master-terminated, slave-not-ready" special case of a master-terminated streaming-data cycle.

The timing diagrams in **Fig 3, 4,** and **5** illustrate the bus cycles the chip supports along with all relevant timing parameters. Several of these timing parameters are dictated by the Micro Channel specification. They are not specific to the MCA_BM_EPLD; their inclusion makes the interface timing description complete and easy to understand. For cross-referencing, **Table 1** contains the Micro Channel Architecture streaming-data timing parameter numbers.

Fig 3, 4, and **5** illustrate timing parameters for SDP cycles. For a deferred SDP cycle, the Micro Channel Architecture specification does not have a maximum number (minimum specification = 0 nsec) for the first active -SD STROBE pulse after CHRDYRTN becomes active. The timing of -SD STROBE after CHRDYRTN is MCA_BM_EPLD's T23 (**Fig 3**). T24 refers to a Micro Channel Architecture specification that the slave wait-state logic must adhere to for CHRDYRTN tim-

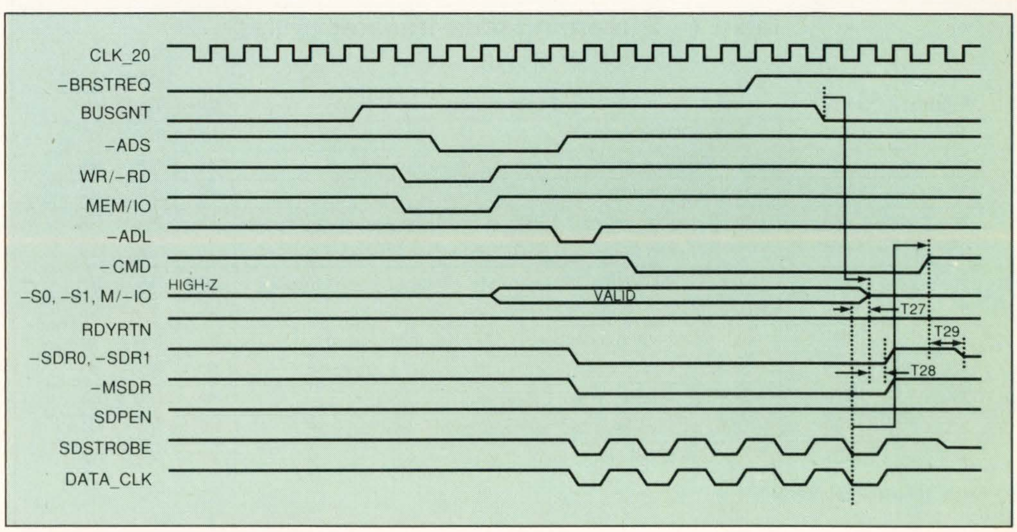

Fig 4—The bus master forcing -BRSTREQ high terminates a streaming-data transfer.

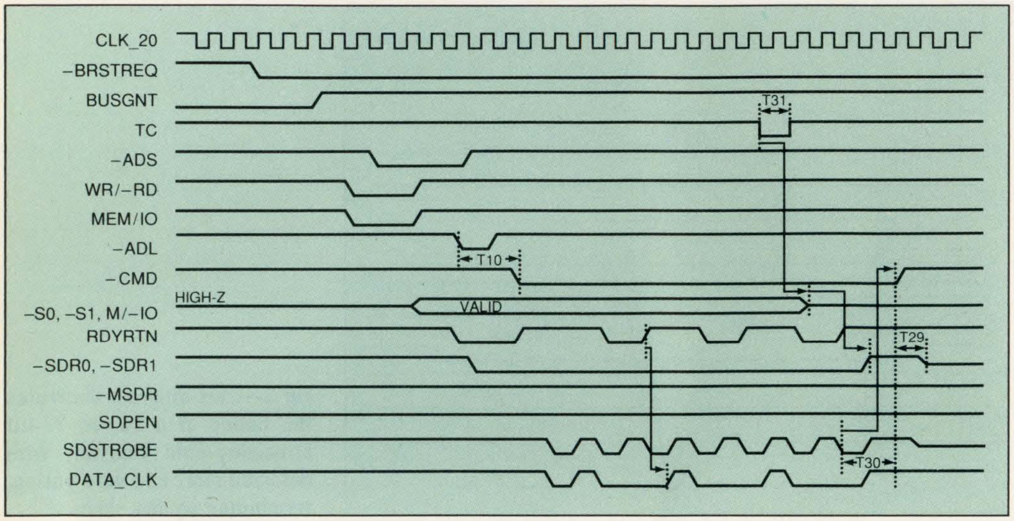

Fig 5—When the master terminates a bus request, if the slave is not ready, the master continues to generate -SD STROBE until the slave is ready.

ing. Timing parameters T25 and T26 specify setup and hold times for the slave wait-state logic for data-pacing, that is, introducing wait states during SDP cycles.

In a slave-terminated SDP cycle, the slave indicates the end of the SDP transfer by de-asserting -SDR0, -SDR1, and -MSDR. In response, the bus master de-asserts status signals -S0 and -S1 and the -CMD strobe. MCA_BM_EPLD's T30 timing parameter adheres to the Micro Channel Architecture specification stating that -CMD inactive from the last falling edge of -SD STROBE should be 100 nsec minimum. T30 also applies to the case when the master terminates the cycle but the slave is not ready, which is illustrated in **Fig 5.**

In a master-terminated SDP cycle **(Fig 4)**, the SDP transfer ends when the master deactivates -S0 and -S1. T27 refers to a Micro Channel Architecture specification that states -S0 and -S1 should be de-asserted within 10 nsec of the last -SD STROBE pulse. This parameter makes it necessary for the transfer controller on the bus-master adapter to signal the end of SDP transfer (by de-asserting the BUSGNT signal) more than one CLK_20 period (50 nsec + EPLD-register setup time) before the last -SD STROBE pulse.

Timing parameter T28 is a Micro Channel Architecture specification for the slave adapter to de-assert -SDR0, -SDR1, and -MSDR signals within 40 nsec of the bus-master adapter's de-assertion of the -S0, -S1 status signal. T29 is a parameter common to all of the SDP cycles. This parameter refers to a Micro Channel Architecture specification that states after the -SDR0 and -SDR1 signals are de-asserted, the slave must drive the -SDR0 and -SDR1 signal to a high-impedance state within 40 nsec from the trailing edge of the -CMD strobe. The timing parameter T31 specifies the minimum required pulse width for -TC, the terminal-count signal that indicates the end of the SDP transfer, to

Table 1—Streaming data-transfer cycles

Figure	Parameter	Explanation	Timing Min	Timing Typ	Timing Max
3	T20	–SD STROBE period	NA	100	NA
3	T21	–SD STROBE active	50	NA	NA
3	T22	–SD STROBE inactive	50	NA	NA
3	T23	RDYRTN active to –SD STROBE falling edge (deferred cycle)	78	NA	NA
3	T24	RDYRTN valid from –SD STROBE low for data pricing	3	NA	45
3	T25	RDYRTN inactive low setup to CLK_20 high	9	NA	NA
3	T26	RDYRTN inactive low hold from CLK_20 high	9	NA	NA
4	T27	–S0, 1 inactive from last –SD STROBE falling edge	NA	NA	10
4	T28	–SDR0, 1 and –MSDR inactive from –S0, 1 inactive	NA	NA	40
3,4,5	T29	–SDR0, 1 3-state from –CMD	NA	NA	40
3,5	T30	–CMD inactive from last falling edge of –SD STROBE	100	NA	NA
5	T31	–TC pulse width	60	NA	NA

Note: NA = Not applicable.

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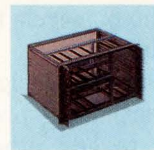
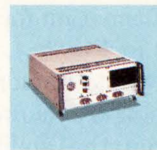

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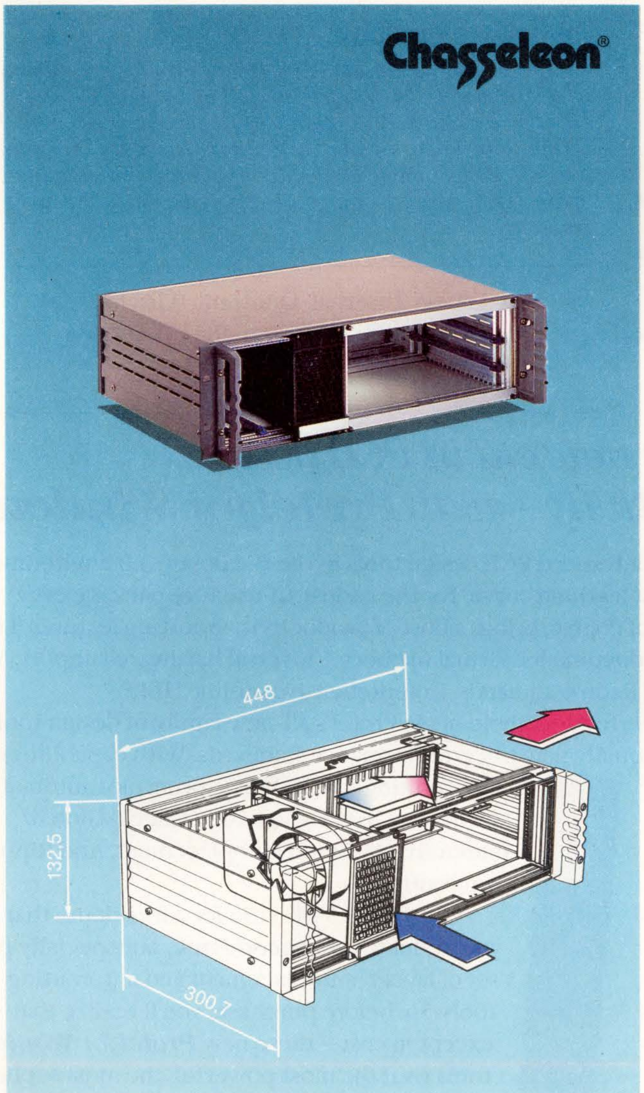

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CIRCLE NO. 54

be 60 nsec minimum. **Table 1** gives device-specific timing information for the bus-cycle timing diagrams illustrated in **Fig 3, 4,** and **5.**

You could implement this design in several different technologies. However, using programmable logic offers you the ability to add other functions, remove unnecessary features, or modify parts of the design to meet your design needs. EDN

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Author's biography

Vinita Singhal is an MPLD Design Manager at Altera Corp who supervises the design group that transfers designs from EPLDs to Mask-Programmed Logic Devices. She has a BTech with honors from the Indian Institute of Technology and an MSEE from Pennsylvania State University. In her spare time, Vinita enjoys reading, technical writing, and traveling.

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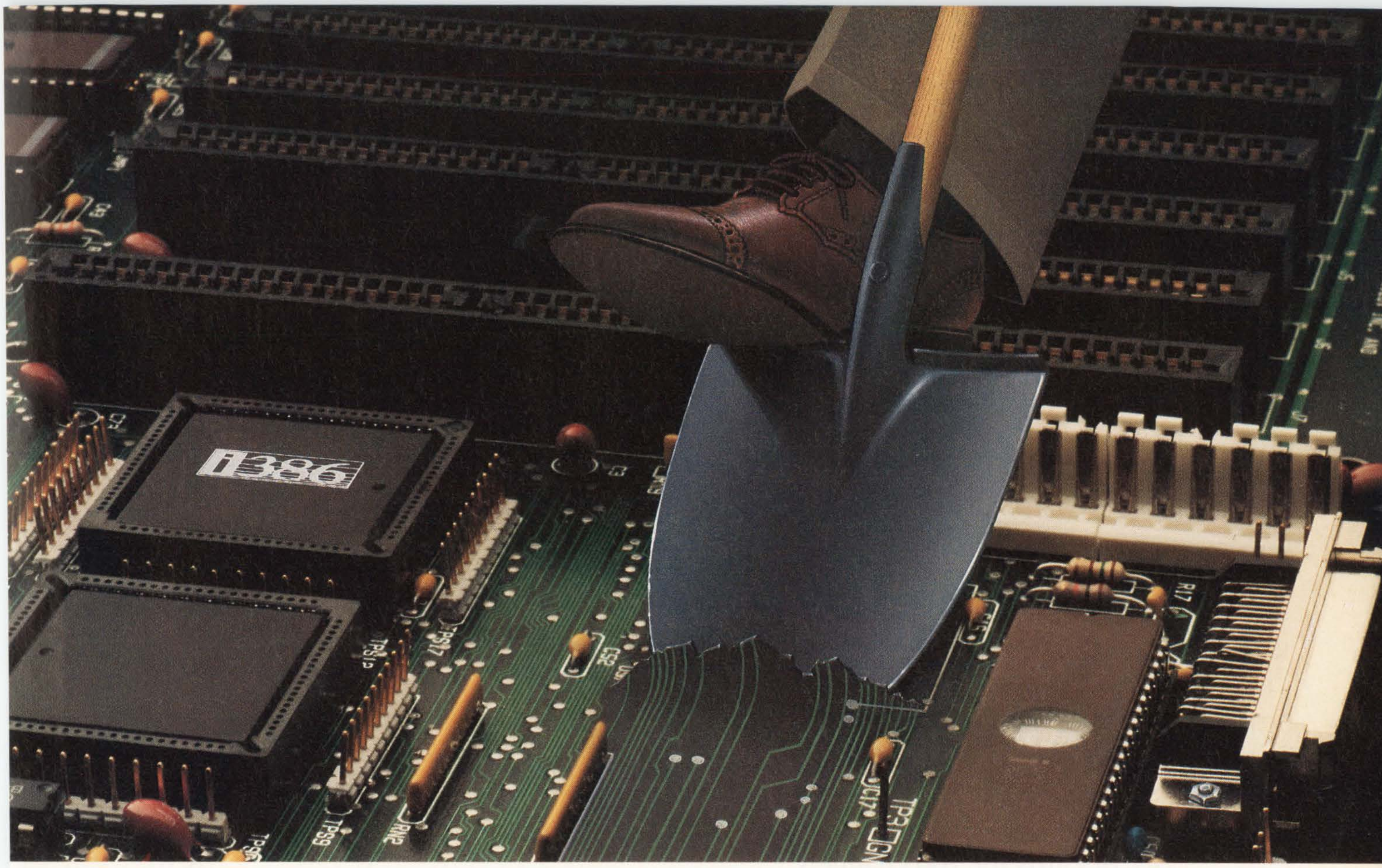

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The LT1190 is a family of high speed amplifiers optimized for video performance on ±5V or single +5V supplies. The family includes three voltage feedback op amps and two video difference amplifiers. All amplifiers slew at 450V/μs, and deliver ±50mA output current for driving cables. The LT1193 video difference amplifier features uncommitted high input impedance (+) and (–) inputs, and can be used in differential or single-ended configurations. In addition, the LT1193 has an adjustable gain of two or greater, with a –3dB bandwidth of 80MHz.

Wideband Voltage Controlled Amplifier

The LT1193 video difference amplifier combined with an MC1496 balanced modulator make a low cost 50MHz Voltage Controlled Amplifier (VCA), shown in Figure 1. The input signal of the MC1496 at pin 1 is multiplied by the Control Voltage on pin 10, and appears as a differential output current at pins 6 and 12. The LT1193 acts to level shift the differential signal and convert it to a single-ended output. Resistor R_B is used to set the bias current in the MC1496 to 1mA in each 200Ω R_L, while R_{CM} is used to shift the differential output into the common mode range of the LT1193. Resistors R1 through R4 bias the MC1496 inputs so that the Control Voltage V_C can be referenced to 0V. Positive V_C causes positive gain; negative V_C gives a phase inversion ($-A_V$), while 0V on V_C gives maximum attenuation (within the V_{OS} of the MC1496 control inputs). The value of R_e is chosen by knowing the maximum input signal:

$$R_e = (V_{IN}\ max)/1mA$$

For the example shown the maximum input signal is 100mV peak, therefore, R_e = 100Ω. At this maximum input signal there is significant distortion from the r_e modulation of the input pair. Linearity can be improved by increasing R_e at the expense of gain. The maximum voltage gain of the VCA is:

$$\frac{V_O}{V_i} = \left(A_V \text{ of LT1193}\right)\left(\frac{2R_L}{R_e + 2r_e}\right)$$

$$V_O/V_{IN} = 2(2\times200)/(100+52) = 5.26 = 14.42dB$$

Figures 2 and 3, show the frequency response and harmonic distortion of the VCA.

The voltage gain of the VCA can be increased at the expense of bandwidth by changing the value of load

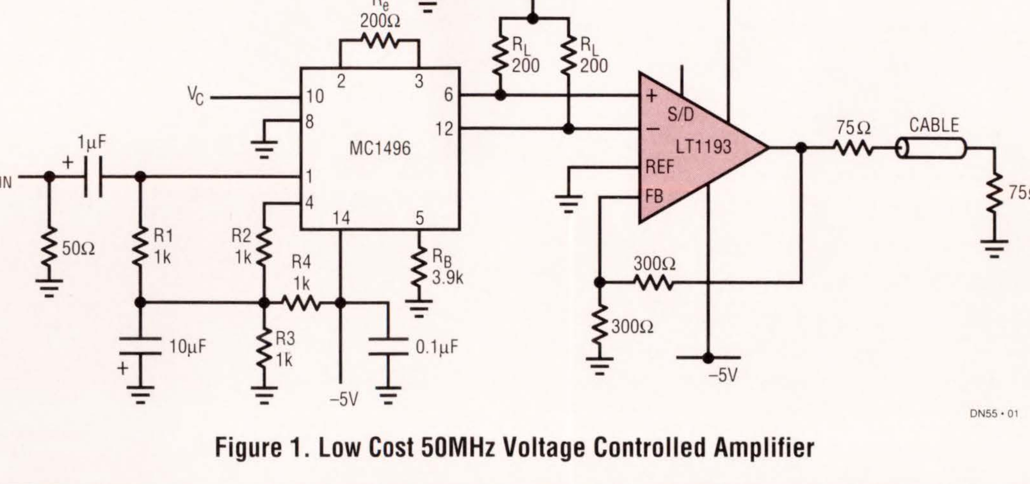

Figure 1. Low Cost 50MHz Voltage Controlled Amplifier

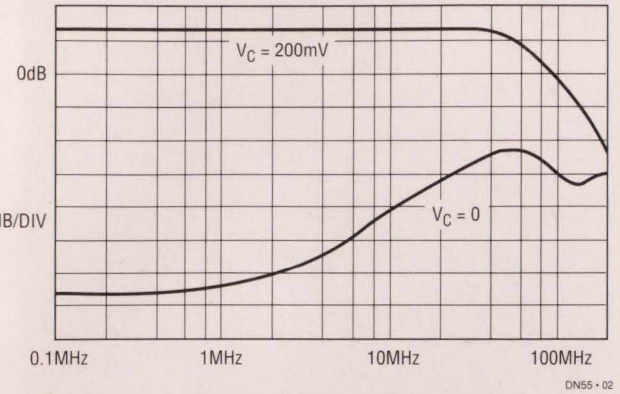

Figure 2. Gain and Attenuation of VCA

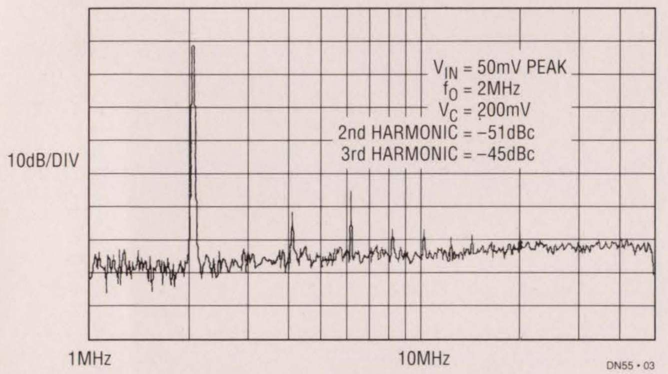

Figure 3. VCA Output Spectrum

resistors R_L. Shorting R_{CM} and increasing R_L to 2k will increase the maximum gain by 20dB and the –3dB bandwidth will drop to approximately 10MHz.

The LT1193 has a shutdown feature that reduces its power dissipation to only 15mW and forces a three-state output. The three-state output occurs when pin 5 is taken to V^-. The high Z state, dominated by the impedance of the feedback network, is useful for multiplexing several amplifiers on the same cable. The impedance of the feedback resistors should not be raised above 1kΩ because stray capacitance on the (–) input can cause instability.

Extending the Input Range on the LT1193

Figure 4 shows a simplified schematic of the LT1193. In normal operation the REF pin 1 is grounded or taken to a DC offset control voltage, while differential signals are applied between pins 2 and 3. The LT1193 has been optimized for gains of 2 or greater, and this means the input stage must handle fairly large input signals. The maximum input signal occurs when the input differential amplifier is tilted over hard in one direction, and 1.2mA flows through the 1kΩ R_e. The maximum input swing is therefore 1.2Vp or 2.4Vp-p. The second differential pair is running at slightly larger current so that when the first input stage limits, the second stage remains biased to maintain the feedback.

Occasionally it is necessary to handle signals larger than 2.4Vp-p at the input. The LT1193 input stage can be tricked to handle up to 4.8Vp-p. To do this, it is necessary to ground pin 3 and apply the differential input signal between pin 1 and 2. The input signal is now applied across two 1k resistors in series. Since the input signal is applied to both input pairs, the first pair will run out of bias current before the second pair, causing the amplifier to go open loop. This effect is shown in Figure 5 for the amplifier operating in a closed loop gain of 1. The LT1193 has a unity gain phase margin of only 40 degrees, so when operating at unity gain, care must be taken to avoid instability.

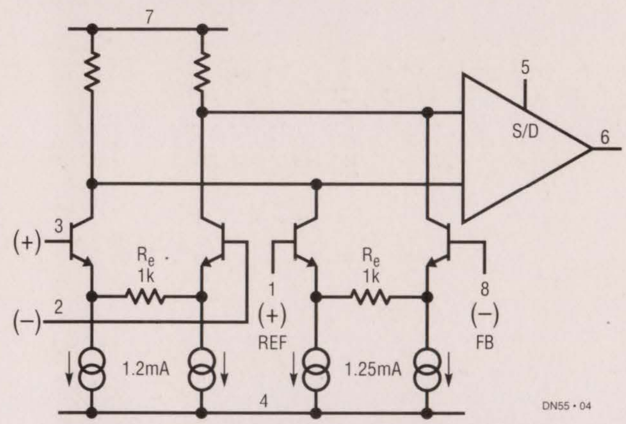

Figure 4. LT1193 Simplified Schematic

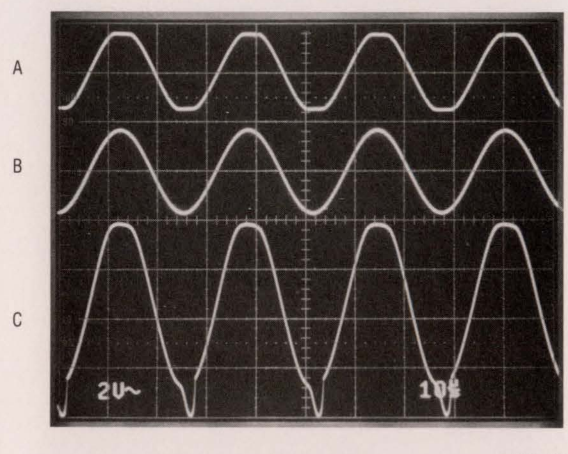

Figure 5. LT1193 in Unity Gain
(A) Standard Inputs, Pins 2 to 3, V_{IN} = 3.6Vp-p
(B) Extended Inputs, Pins 1 to 2, V_{IN} = 3.6Vp-p
(C) Extended Inputs, Pins 1 to 2, V_{IN} = 7.0Vp-p

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EDITED BY CHARLES H SMALL & ANNE WATSON SWAGER

Battery-powered microprocessor turns itself off

Carl Hallman, Network Systems Corp, Brooklyn Park, MN

Combining a 3-terminal micropower regulator with a simple 2-transistor switch yields a very low-leakage, auto-power-off circuit for a battery-powered μP (**Fig 1**). This circuit requires about 10 mA of additional battery current to operate when power is on. However, the circuit extends the battery life for short power-on cycles by reducing the leakage current when power is off to a minimum.

The LP2950/LP2951 regulators from National Semiconductor are 3- and 8-pin micropower regulators, respectively, that are suited for battery-powered devices. The 8-pin version has a shutdown pin that would be very useful except for its relatively high leakage current that will drain a 9V battery in about six months with no use. This shutdown pin also requires an active-high signal. This circuit uses the 3-pin version with a 2-transistor switch in front of the regulator. This switch results in virtually no measurable leakage currents and features an active-low shutdown pin.

The circuit uses a momentary-contact switch to force Q_2, which powers the LP2950 regulator, to conduct. Once powered up, one of the μP's initial instructions sets an output pin to a logic high. This pin connects to the base of Q_1. Q_1 then starts conducting and keeps Q_2 turned on after the momentary-contact switch is released. The μP's program keeps the level of the output pin high for a predetermined length of time. When this power-on time expires, the μP forces the power on this pin low. This low logic level shuts off Q_1, which lets the base of Q_2 rise to the emitter voltage. Shutting off Q_2 removes the power to the regulator and shuts down the μP. **EDN BBS /DI_SIG #1076** EDN

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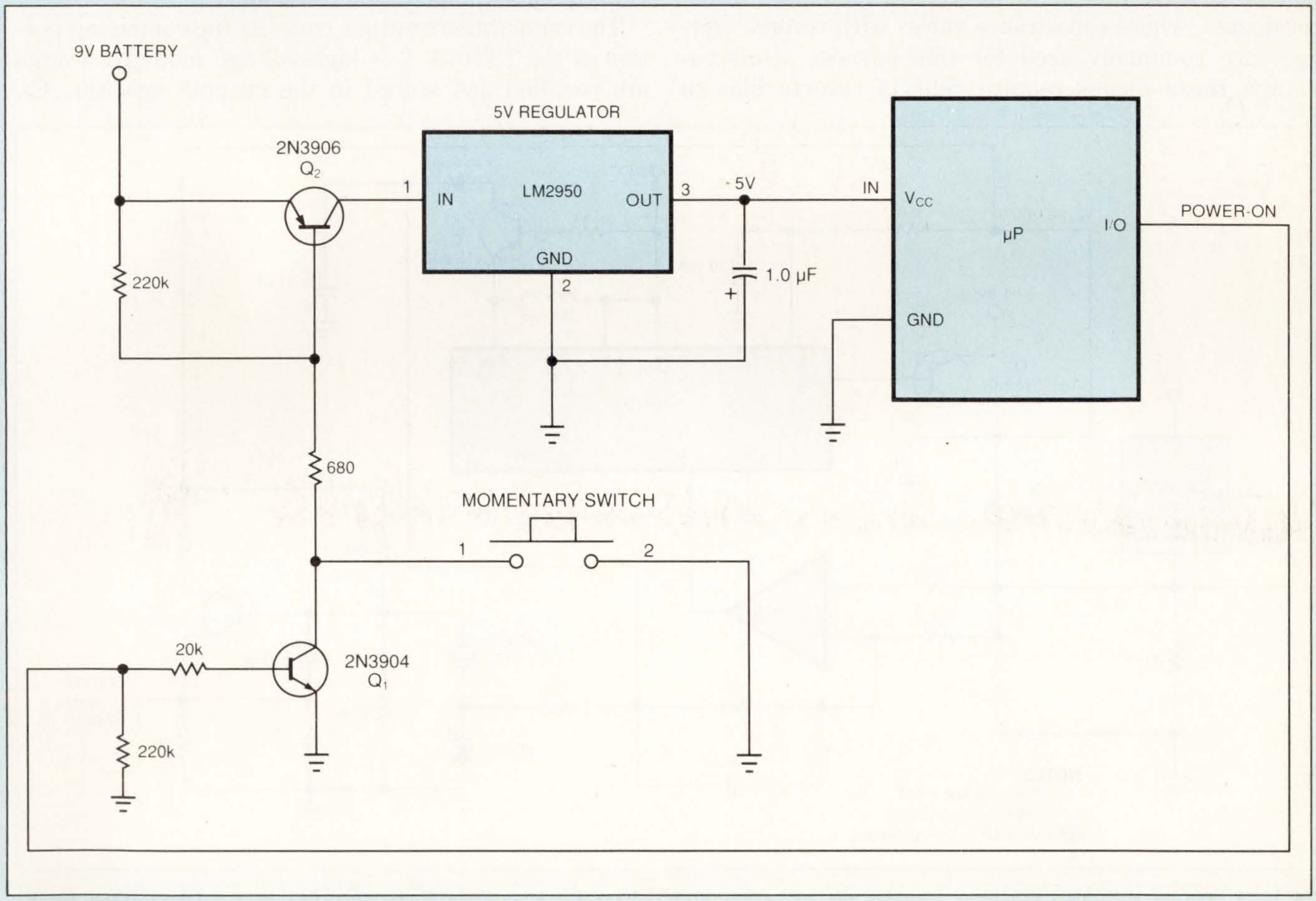


Fig 1—Using a low-leakage regulator with an active-low shutdown pin, this battery-powered μP with transistor switches extends battery life for applications that require only short power-on periods by preventing leakage when the power is off.

Single 1.5V cell powers crystal oscillator

Jim Williams, Linear Technology Corp, Milpitas, CA

Many single-cell systems require a stable clock source. Such applications include portable high-accuracy clocks, survival radios, and secure communications. Crystal oscillators that run from 1.5V are relatively easy to construct. However, designing one with good stability over temperature is much more difficult. Ovenizing the crystal is one approach, but power consumption is excessive.

Fig 1's circuit presents an alternate method that provides frequency-correcting bias to the oscillator. The circuit improves the temperature stability of a 1.5V-powered crystal oscillator by a factor of 20 by slightly tuning the crystal's resonance as ambient temperature varies. The bias value is determined by absolute temperature and corrects for the oscillator's repeatable thermal drift. The simplest way to correct for the drift is by slightly varying the crystal's resonance point with a variable shunt or series impedance. Varactor diodes, whose capacitance varies with reverse voltage, are commonly used for this purpose. Unfortunately, these diodes require volts of reverse bias to generate significant capacitance shift, making direct 1.5V-powered operation impossible. **Fig 1** uses an LT1073 configured as a step-up switching regulator to derive the necessary bias from 1.5V.

Q_1 and its associated components form a 1-MHz Colpitts oscillator, which normally has a temperature coefficient of about 1 ppm/°C. The remainder of the circuit implements the temperature correction. The LM134 adjustable current source senses ambient temperature, converting it to a current that then flows through the 30.1-kΩ resistor. The LT1017 comparator subtracts this resistor's voltage from a reference potential. The stable subtraction voltage is derived from the LT1073's internal 212-mV reference via Q_2 and the 73.2- and 27.4-kΩ resistors. Feedback from Q_2's collector to the LT1073's auxiliary-amplifier output, AO, closes the reference loop, which also powers the Colpitts oscillator. C_1 frequency-compensates the loop.

The comparator's output controls the remaining portion of the LT1073. L_1's high-voltage inductive events are rectified and stored in the output capacitor, C_2,

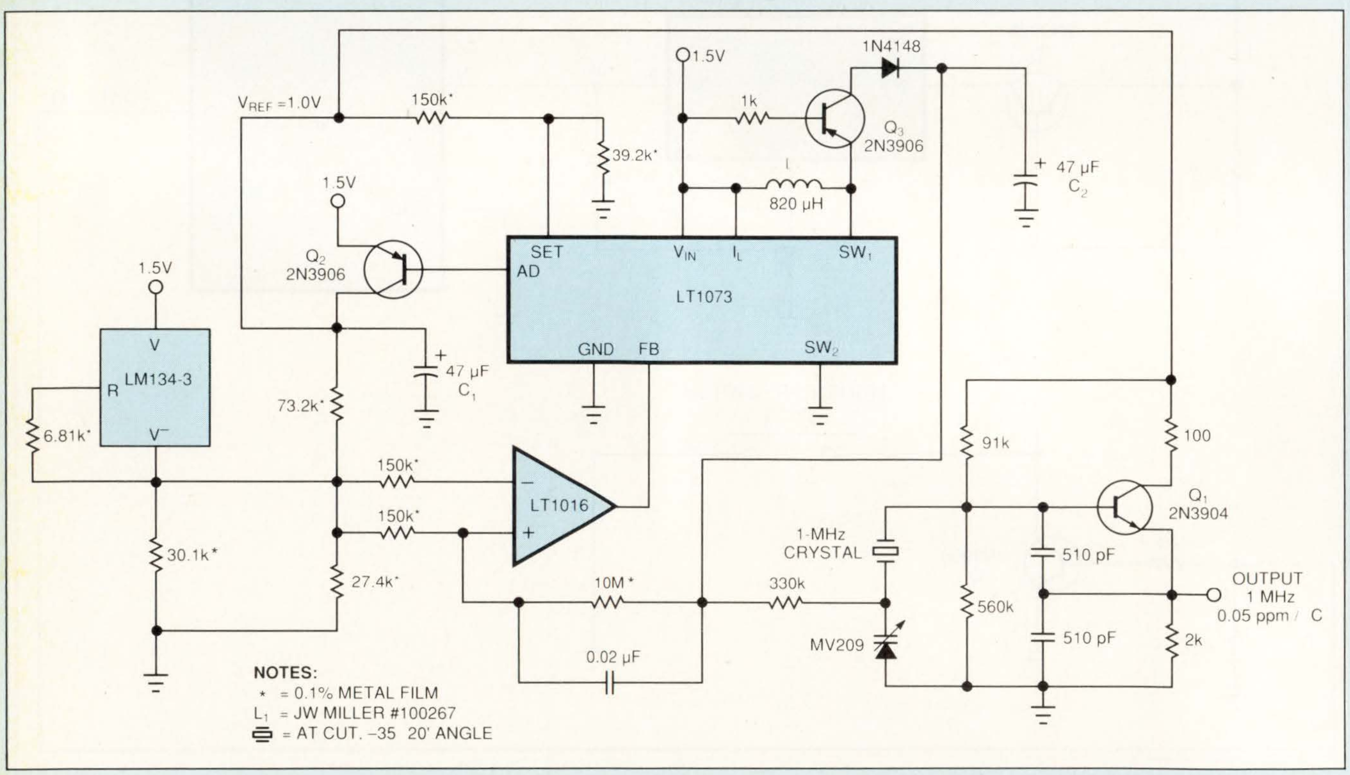
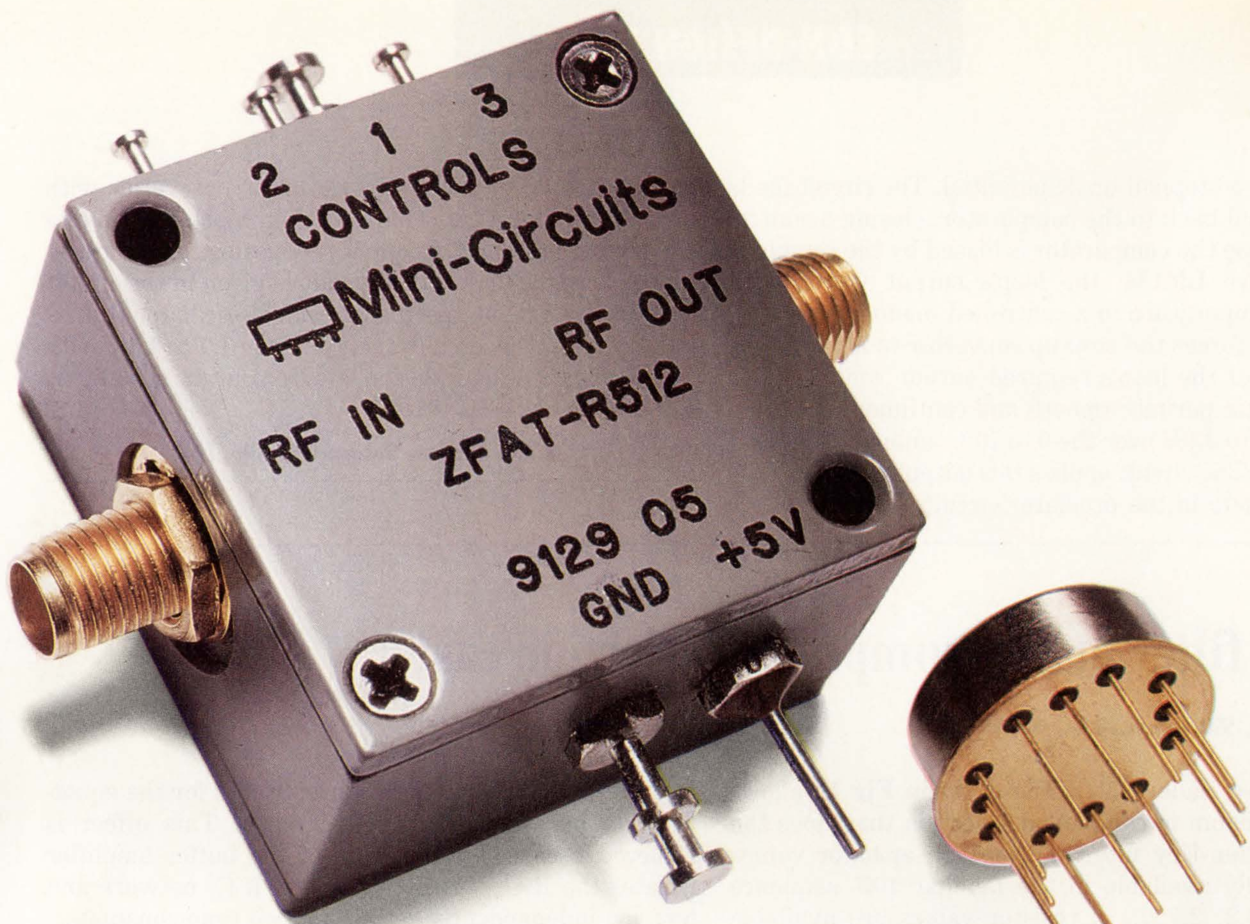


Fig 1—A step-up switching regulator provides the necessary bias voltage for a varactor diode operating in a 1.5V-powered circuit. The varactor diode's change in capacitance, controlled by a feedback loop including a temperature-sensing LM134 current source, opposes the crystal's drift with temperature to provide for an output that changes 0.05 ppm/°C.



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resulting in a stepped-up dc potential. The circuit feeds this potential back to the comparator, closing a control loop. Because the comparator is biased by the temperature-sensitive LM134, the loop's output varies with ambient temperature in a controlled manner.

Q_3's drop forces the step-up converter to always run, regardless of the loop's required output voltage. This characteristic permits smooth and continuous varactor bias from 0 to 3.9V over the 0 to 70°C ambient temperature range. The circuit applies this output to the MV209 varactor diode in the oscillator circuit. The varactor's capacitance, a function of its dc bias, thus varies with ambient temperature. This change in capacitance shifts the crystal's resonant frequency, opposing temperature-induced crystal drift. For the values given in the circuit and the crystal cut specified, residual oscillator drift is 0.05 ppm/°C. The circuit functions from 1.7 to 1.1V with no specification degradation. Current drain is 230 μA. **EDN BBS /DI_SIG #1077**

To Vote For This Design, Circle No. 747

Active filter makes component selection easier

Michael Wyatt, SSO Honeywell Inc, Clearwater, FL

The modified Sallen-Key active filter in **Fig 1b** allows greater freedom in component selection than does the original Sallen-Key filter of **Fig 1a**. Capacitor values are generally available in the familiar 10% sequence of 1, 1.5, 2.2, 2.7, . . . ; resistor values are available in the 1% sequences of 1, 1.02, 1.05, ... Sallen-Key filter designs based on equal capacitor values rather than the more common equal resistor values would benefit from better fidelity and lower cost. However, the original filter in **Fig 1a** is restricted when using equal capacitors to damping factors greater than or equal to 1. This restriction limits the filter's usefulness for practical designs. In the more common equal-resistor case, the damping is unrestricted and equals $\sqrt{C_2/C_1}$. However, capacitor values that fit this equation may not be available at reasonable costs.

Fig 1b's modification lifts those component-value restrictions. Filter damping is unrestricted for the equal-capacitor or the equal-resistor case. This effect is achieved because the addition of the buffer amplifier isolates the R_1C_1 network from the R_2C_2 network and lets you independently select the two time constants.

You design the filter by selecting a standard value for C_1 and C_2, then computing the ratio R_2/R_1, and finally solving for R_2 and R_1 from the natural frequency equation. For example, to design a second-order low-pass Butterworth filter with a corner frequency of 1 kHz, first choose convenient values of 0.01 μF for C_1 and C_2. Then compute the ratio of $R_2/R_1=2$ for damping of 0.707. Now solve for $R_1=11.25$ kΩ and $R_2=22.50$ kΩ from the equation for natural frequency ($\omega_N=2\pi f$) included in **Fig 1b**. **EDN BBS /DI_SIG #1075**

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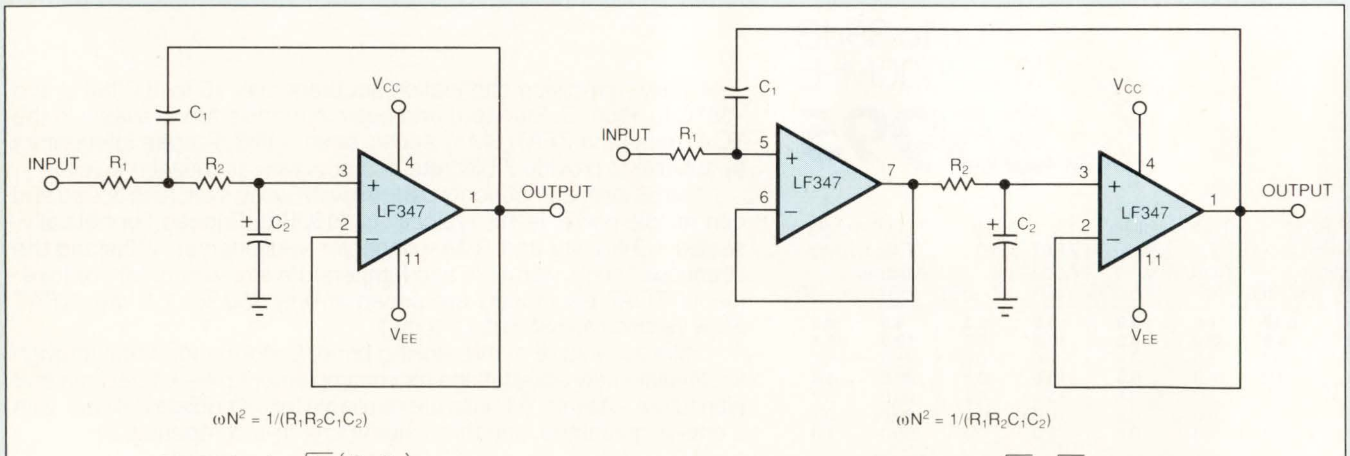

(a) $\omega_N^2 = 1/(R_1R_2C_1C_2)$

$$\text{DAMPING FACTOR} = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}\left(\frac{R_1+R_2}{\sqrt{R_1R_2}}\right)$$

(b) $\omega_N^2 = 1/(R_1R_2C_1C_2)$

$$\text{DAMPING FACTOR} = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}\sqrt{\frac{R_2}{R_1}}$$

Fig 1—Adding a buffer to the original Sallen-Key filter in (a) removes component-selection restrictions. The filter in (b) lets you choose either equal resistor or equal capacitor values for any desired filter-damping factor.

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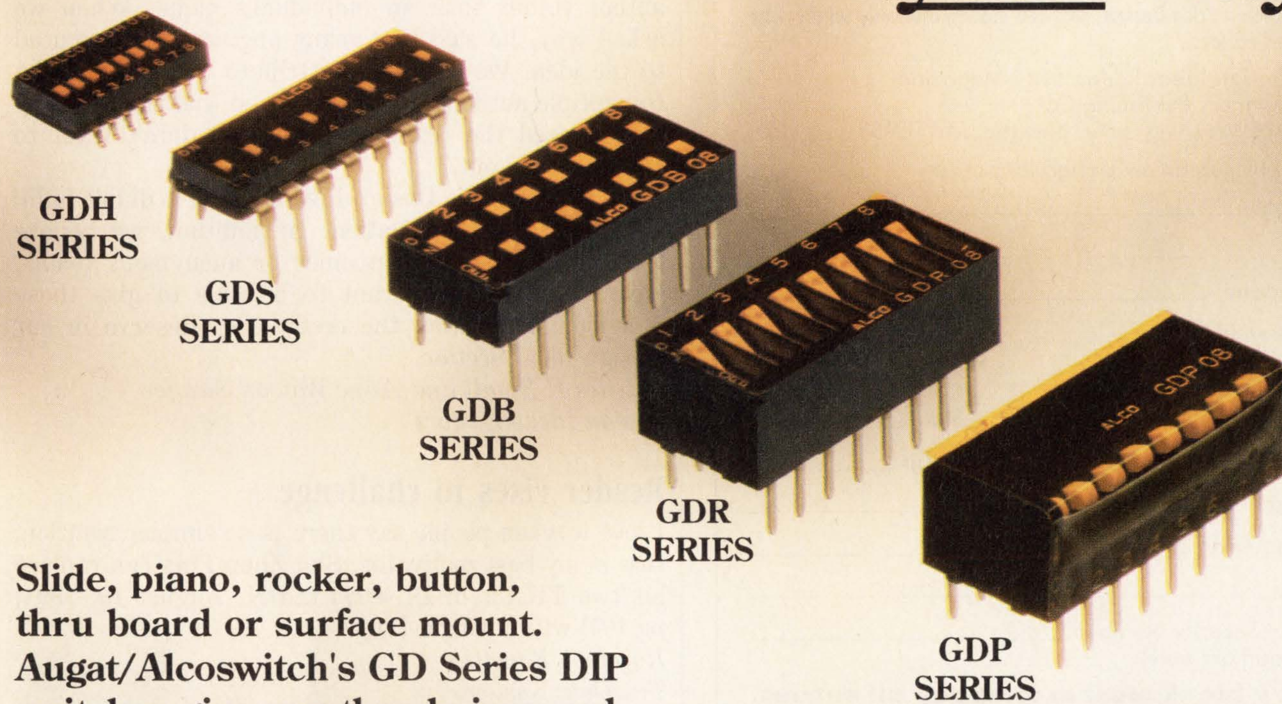

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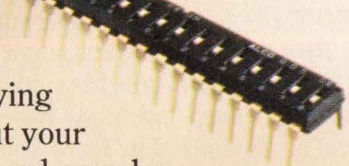

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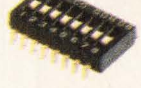

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The winning Design Idea for the October 1, 1991, issue is entitled "High-frequency VCOs top 100 MHz," submitted by Di Paolo Franco of Ericsson Fatme (Rome, Italy).

ISSUE WINNER

The winning Design Idea for the October 10, 1991, issue is entitled "PC printer port performs I/O," submitted by D Fletcher of IDS Inc (Dallas, TX).

Credit individuals, not companies

A spokesman for an electronics company recently submitted a Design Idea and neglected to include a signed entry blank. When we called him, he stated that his company wanted the company's name to appear as the author rather than an individual's name. When we asked why, he said that many engineers contributed to the idea. We offered to attribute the Design Idea to multiple authors. He then replied that his company "emphasized the team approach and didn't want to single anyone out."

We rejected this Design Idea because it didn't fulfill our criteria for publication. In addition, we believe that engineers, not companies or anonymous teams, have ideas. And we want to be able to give these individual innovators the credit they deserve in our Design Ideas section.

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Design Ideas Editors

Reader rises to challenge

I love it when people say there is no simpler solution; that is my best motivator. Shu Zhen Ping can replace his two TIL13s in DI #994 (EDN, August 19, 1991, pg 164) with a single H1AA4.

Robert A Bonetti
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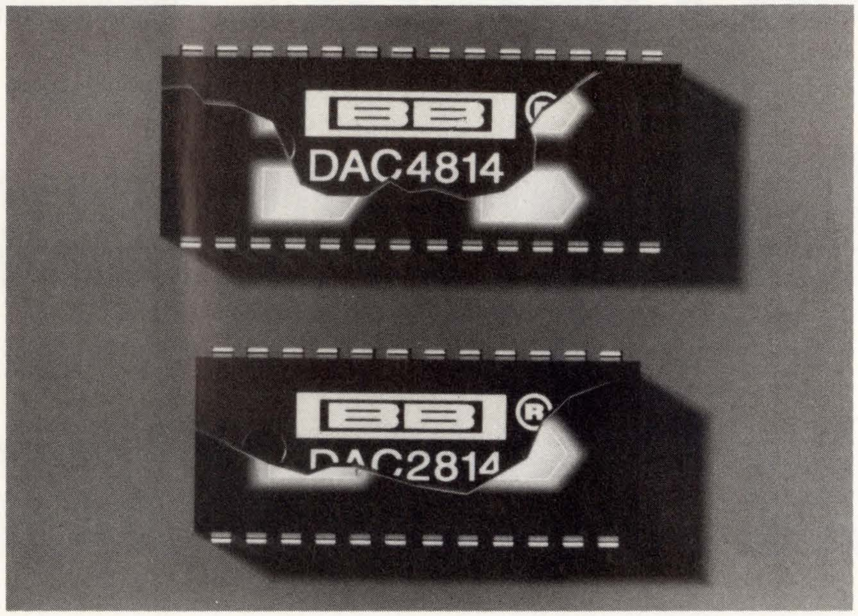

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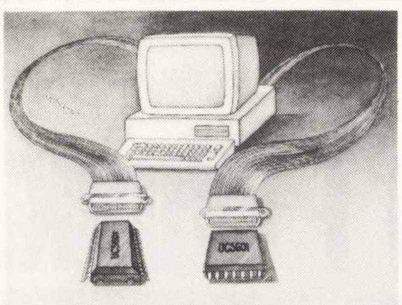

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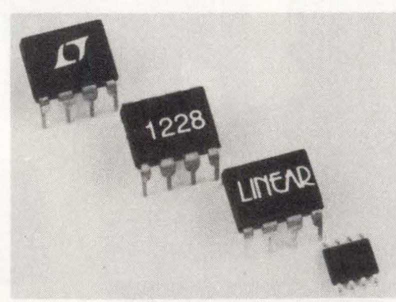
Unitrode Integrated Circuits Corp, 7 Continental Blvd, Merrimack, NH 03054. Phone (603) 424-2410. **Circle No. 375**

Variable-Gain Amplifier

- *Has 75-MHz bandwidth*
- *Control range is 60 dB*

The LT1228 combines a 100-MHz current-feedback amplifier with a 75-MHz gain-controlled, differential-input amplifier. The 60-dB control range is set by an external resistor. The amplifier, which has an output-drive capability of 30 mA, is specified for operation from ±2 to ±18V supplies. The differential



gain and phase of the current-feedback amplifier are 0.04% and 0.1° while driving a 75Ω cable. Rise time is 3.5 nsec. LT1228, in 8-pin DIP and SO packages, from $3.95 (100).

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (800) 637-5545; (408) 432-1900. FAX (408) 434-0507. **Circle No. 376**

Text continued on pg 143

8-bit CMOS ADC. The HI-5700 features a conversion rate of 20 Msamples/sec. A parallel architecture provides high speed and eliminates the need for an external sample-and-hold circuit. An overflow bit allows series connection of two converters for 9-bit resolution. The device operates from a 5V supply and consumes 550 mW. The HI-5700 comes in a 28-pin plastic DIP. Commercial or industrial temperature grades, $13 and $16.90 (100), respectively. **Harris Semiconductor,** Box 883, Melbourne, FL 32901. Phone (800) 442-7747, ext 1096. **Circle No. 377**

Low-power GAL. The GAL16V8S-15E is an electrically erasable PLD that can emulate most types of 20-pin PLDs. The GAL device features an input-to-output propagation delay of 15 nsec and a maximum supply current of 27 mA. The company guarantees a 100% field-programming yield, data retention of 20 years, and 100 erase/write cycles. The PLD comes in 20-pin DIPs and plastic leaded chip carriers. 15-nsec version, $2.72; 25-nsec version, $1.84 (5000). **SGS-Thomson,** 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. FAX (602) 867-6290. **Circle No. 378**

T1 frequency translator. The PLXO (phased-locked crystal oscillator) provides frequency translation between telephone-standard reference clocks and North American DS1 (1.544 MHz) and DS1C (3.152 MHz) transmission rates and Europe's CEPT1x2 (4.096 MHz) transmission rate. The PLXO provides a loss-of-lock signal, which the designer can use as a system warning. Pricing varies according to the frequency range. The 1.544- to 4.096-MHz version, $21 (10,000). **AT&T Microelectronics,** Dept 52AL040420, 555 Union Blvd, Allentown, PA 18103. Phone (800) 372-2447, ext 819; in Canada, (800) 553-2448, ext 819. **Circle No. 379**

Modem chip set. The 4-chip SQ6987 modem enables voice, facsimile, and data transmission and can detect DTMF tones during voice transmission. The chip set can transmit and receive facsimile information at 9600 bps and data communications at 2400 bps. The modem supports V.21, V,29, V.27ter, and V.27 signaling for facsimile operation and includes MNP-5 and V.42bis error correction and data compression. The SQ6987 operates from ±5V supplies and comes in plastic leaded chip carriers, DIPs, and quad flatpacks. $45 (10,000). **Sierra Semiconductor,** 2075 N Capitol Ave, San Jose, CA 95132. Phone (408) 263-9300. FAX (408) 263-3337. TLX 384467. **Circle No. 380**

SCSI disk-drive controller. The CL-SH450 supports 40-MHz NRZ disk-transfer data rates and the 10-Mbyte/sec SCSI-2 standard. An intelligent buffer manager decreases access times between the host and disk interfaces by allowing the transfer of noncontiguous blocks of data. A proprietary split-data-field technique allows zone recording formats and 88-bit Reed-Solomon error correction. In a 100-pin quad flatpack, $30 (100). **Cirrus Logic Inc,** 1463 Centre Pointe Dr, Milpitas, CA 95035. Phone (408) 945-8300. FAX (408) 263-5682. TLX 171918. **Circle No. 381**

Programmable-gain D/A converters. This series of 8-bit D/A converters features a programmable gain to any one of four levels. The chips, which operate from a 4.5 to 13.2V supply, have a settling time of 2.5 µsec within 1V of V_{cc} and analog ground. The output range extends from 0 to V_{cc}. Edge-triggered latches have 30-nsec write times and 0-nsec hold times. The ML2340 (single latch) and ML2341 (double latch) have a programmable reference of 4.5 or 2.25V. The ML2350 (single latch) and ML2351 (double latch) have a programmable reference of 5 or 2.5V. The devices come in 18- and 20-pin packages. From $3.75 (100). **Micro Linear Corp,** 2092 Concourse Dr, San Jose, CA 95131. Phone (408) 433-5200. **Circle No. 382**

12-bit D/A converters. The MAX507 and MAX508 are 12-bit voltage-output converters that combine a laser-trimmed DAC with a 10V-drive-capable output amplifier and a buried zener reference. The DACs have double-buffered logic inputs and acquire data in 12-bit-wide (MAX507) or 8+4-bit-wide (MAX 508) format. The devices have a settling time of 5 µsec to ±0.5 LSB and a slew rate of 2V/µsec. Package options include 20- and 24-pin DIPs and wide SO packages. From $7.55 (1000). **Maxim Integrated Products,** 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600. **Circle No. 383**

Low-power 20-pin PAL. Especially useful in portable-computer applications, the PLC18V8Z-25 universal PAL device has a 25-nsec (max) propagation delay and a current drain of less than 100 µA. The device includes 10 inputs, 74 AND gates, and 8 output macrocells. Input-transition-detection circuitry automatically adjusts the device's current consumption to the presence or absence of an input signal. From $3.75 (1000). **Signetics/Philips,** Box 3409, Sunnyvale, CA 94088. Phone (408) 991-2000. **Circle No. 384**

Synchro-to-digital converter. Featuring a 14-bit or programmable 14- or 16-bit resolution, the SDC-14575 synchro/resolver-to-digital converter comes in a 1.0×0.8-in. package. The converter's velocity output provides a 4V dc signal that is linear to 1%. The device is available in 4- or 8-arc-minute accuracy grades. For resolver use, the SDC-14575 accommodates inputs of 2 and 11V rms. For synchro inputs, a solid-state Scott-T transformer accepts signal levels of 11.8 or 90V rms. The frequency range is 47 Hz to 5 kHz, and the closed-loop bandwidth is 103 kHz. From $365. **ILC Data Device Corp,** 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600, ext 383. FAX (516) 567-7358. **Circle No. 385**

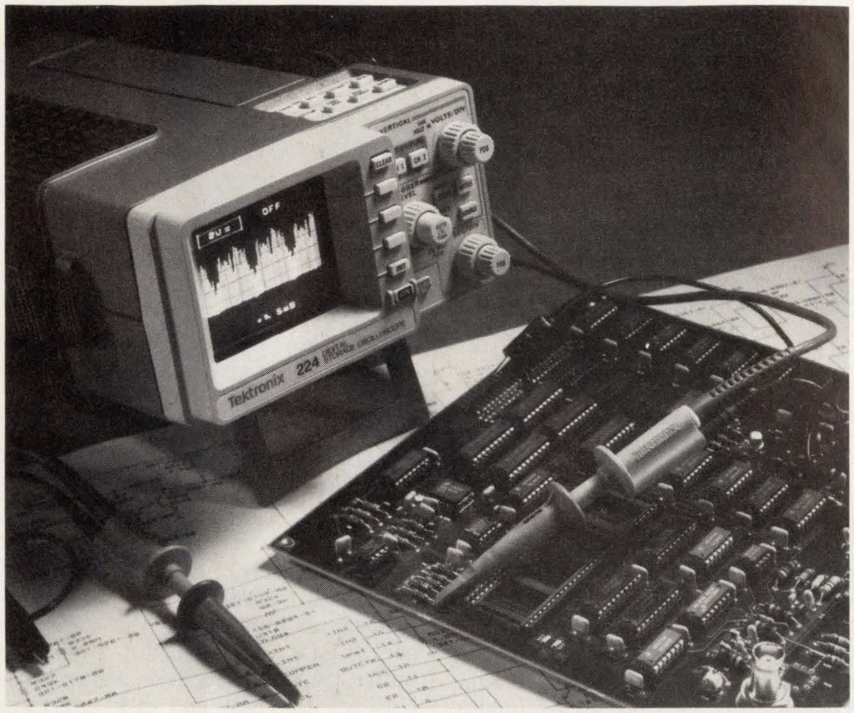
12-bit, 3-MHz A/D converter. Featuring a 3-MHz (330 nsec) sampling speed, the HI-5800 12-bit converter contains a 2-step subranging 7-bit flash ADC, a 7-bit DAC with digital error correction, an on-chip voltage reference, and a sample-and-hold circuit. Key specifications include differential nonlinearity of 0.5 LSB, a 71-dB S/N ratio, −72-dB THD, and a 74-dB spurious-free dynamic range. The HI-5800, in a 40-pin ceramic DIP, $110 (100). **Harris Semiconductor,** Box 883, Melbourne, FL 32901. Phone (800) 442-7747, ext 1139. **Circle No. 386**

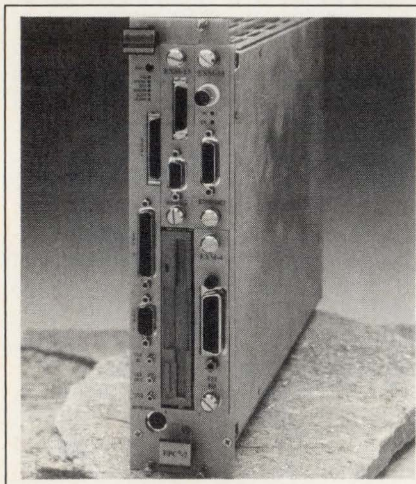
60-MHz Handheld DSO

- *Weighs 4.4 lb.*
- *Runs for 3 hours from rechargeable batteries*

Model 224 2-channel, 60-MHz-bandwidth handheld digital storage oscilloscope weighs 4.4 lb and meets the shock and vibration requirements of MIL standard T28800D. It operates for 3 hours from a pair of rechargeable batteries and features ohmic isolation to 600V rms between each channel and the chassis. The scope has automatic trigger settings and stores four front-panel setups for later recall. You can control the scope through its RS-232C port. The vendor's CAT200 virtual-instrument software lets you use a PC for this purpose. $2750.

Tektronix Inc, Box 1520, Pittsfield, MA 01202. Phone (800) 426-2200. **Circle No. 387**





i486-Based VXI Controller

- *Occupies two C-size slots*
- *Includes hard disk that stores as much as 240 Mbytes*

The EPC-7 VXIbus controller uses an i486 μP as its CPU, running at either 33 or 50 MHz. The 2-slot C-size module optionally contains a 3½-in. floppy-disk drive and a hard disk that can store as much as 240 Mbytes. In addition, the controller includes four EXMbus slots. The EXMbus is similar to the 16-bit ISA bus except that EXMbus cards support a module-identification sequence when you power them up. Although it can't take advantage of the module IDs, software for ISA bus cards works with EXMbus cards. An adapter lets you plug a full-length ISA bus card into the controller. 33-MHz, 2-Mbyte RAM, 52-Mbyte hard-disk and floppy-disk drive, and runtime software, $6995; 640 × 480-pixel graphics controller, $450.

Radisys Corp, 19545 NW Von Neumann Dr, Beaverton, OR 97006. Phone (800) 950-0044; (503) 690-1229. **Circle No. 388**

6½-Digit DMM

- *Basic dc accuracy is 15 ppm for 24 hours*
- *Takes 1000 readings/sec*

The HP 34401A 6½-digit multimeter works as a stand-alone or a computer-controlled instrument. Both IEEE-488 and RS-232C ports are included. The meter can take a reading in 1 msec, change its range in 20 msec, and respond to the standard commands for programmable instruments (SCPI). Programs written for the HP 3478A and the Fluke 8840A meters work without modification. The unit's basic dc accuracy is 15 ppm for 24 hours. In addition to dc measurements, the meter measures wideband ac. Other functions include measuring decibels, and testing diodes and continuity. $995.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900. **Circle No. 389**

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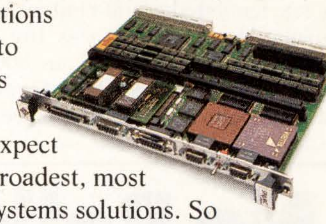

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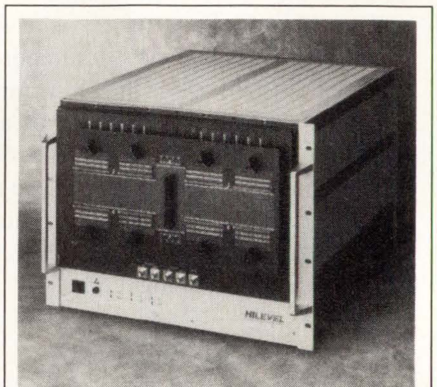
CIRCLE NO. 62

IEEE-488 digital-control interface. The Digital488/80A 80-channel digital I/O interface communicates with the controlling computer via the IEEE-488 bus. The unit, which you can mount in an equipment rack, divides its inputs into 40-channel groups, each of which has six handshake and control lines. A nonvolatile memory stores the power-up state of all lines and an 8000-byte buffer captures 1000 80-bit readings, thus relieving the bus interface of the need to poll the unit constantly. $995; high-voltage option for handshake and control signals, $295. **IOtech Inc,** 25971 Cannon Rd, Cleveland, OH 44146. Phone (216) 439-4091. FAX (216) 439-4093. **Circle No. 390**

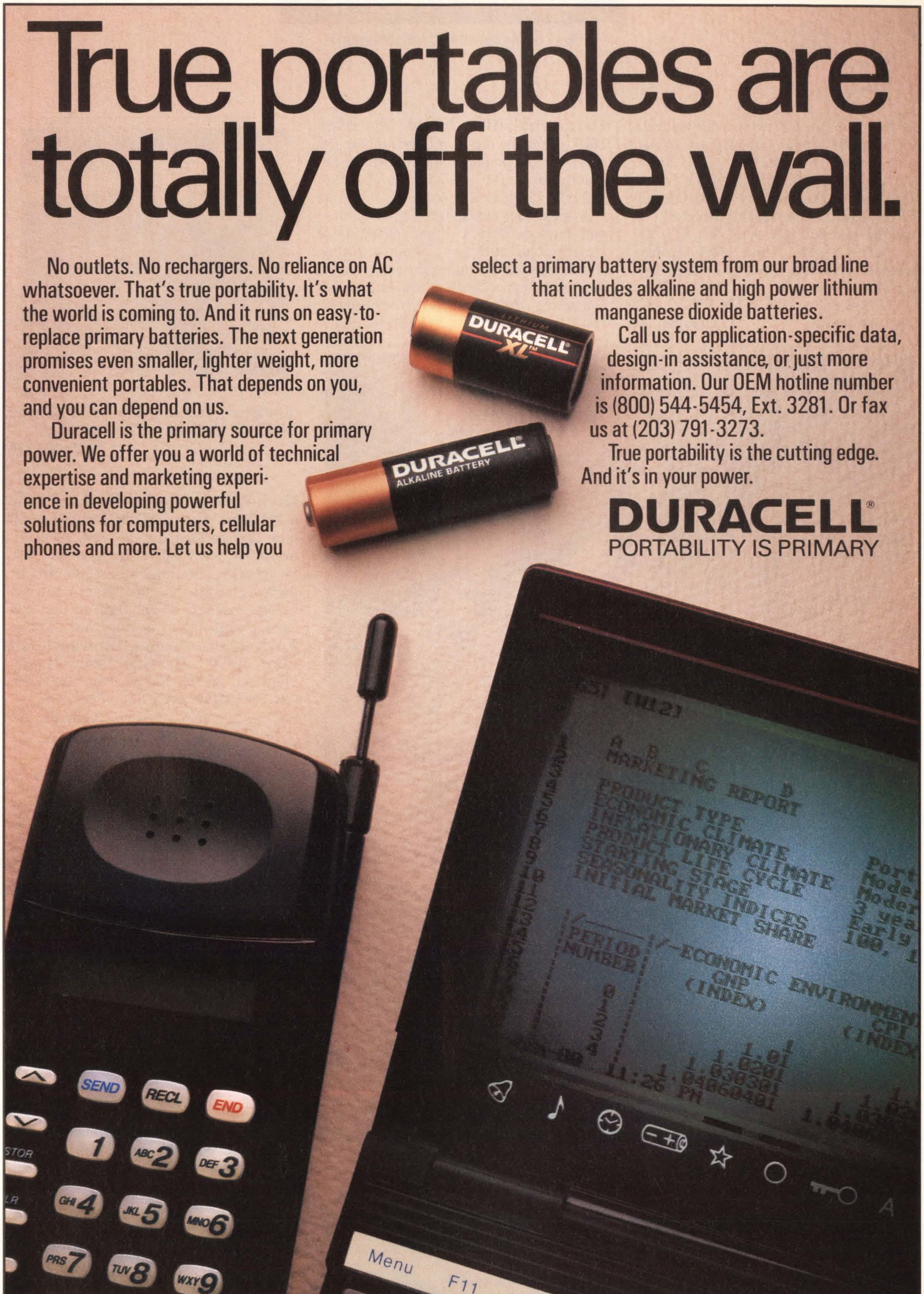
ISA bus audio-input boards. The AT-A2150 series uses delta-sigma A/D conversion to achieve a 93-dB S/N ratio and −95-dB total harmonic distortion. There are two versions; one for general audio work (flat within ±0.015 dB to 20 kHz); the other for voice measurements (flat within ±0.015 dB to 4 kHz). $1995. **National Instruments Corp,** 6504 Bridge Point Pkwy, Austin, TX 78730. Phone in US and Canada, (800) 433-3488; (512) 794-0100. FAX (512) 794-8411. **Circle No. 391**



Benchtop ASIC tester. The ETS370 provides as many as 512 pins and features a 25-MHz bidirectional data rate, a 50-MHz clock, and programmable timing generators with 500-psec resolution and per-pin programmability. The unit's device and user interfaces conform to those of the vendor's ETS and Topaz families. A 256-pin system with 16 timing generators and a 33-MHz i486-based PC controller sells for less than $95,000. **Hilevel Technology Inc,** 31 Technology Dr, Irvine, CA 92718. Phone (714) 727-2100. FAX (714) 727-2101. TLX 655316. **Circle No. 392**

DSP and audio I/O board for 16-bit ISA bus. The AT-DSP-2200 provides 25 Mflops of computation capability via a WEDSP32C DSP μP. The board also includes two channels of 16-bit delta-sigma A/D conversion with a S/N ratio of 92 dB and total harmonic distortion of −95 dB. Two analog-output channels incorporate 8× oversampling filters. $2495. **National Instruments Corp,** 6504 Bridge Point Pkwy, Austin, TX 78730. Phone in US and Canada, (800) 433-3488; (512) 794-0100. FAX (512) 794-8411. **Circle No. 393**

Half-size ISA bus digital I/O boards. These 5.512×3.9-in. boards use 5V dc power only; no 12V supplies are needed, so they work in several laptop PCs. Each board has 32 channels configured as four 8-bit ports. Two mod-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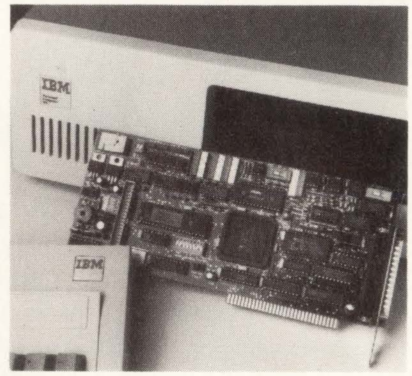
els provide inputs; two provide outputs; and two mix inputs and outputs. In each pair, one unit works with TTL levels, and the other unit provides 5-kV isolation and works with 12 to 24V levels. TTL outputs sink 40 mA; isolated outputs handle 200 mA. Unit for TTL levels, $225; isolation unit, $295. **Contec Microelectronics USA Inc,** 2188 Bering Ave, San Jose, CA 95131. Phone (800) 888-8884; (408) 434-6767. FAX (408) 434-6884. **Circle No. 394**

Data-acquisition board. The DAS-1600 digitizes eight differential or 16 single-ended analog inputs with 12-bit resolution at 100 kHz. It also provides a pair of 12-bit analog outputs, 24 digital I/O lines, four dedicated digital inputs, and four dedicated digital outputs. A pacer clock and two 16-bit counter-timers facilitate triggering conversions and counting events. $899; advanced software, $200. **Keithley Instruments** Data Acquisition Div, 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3000. FAX (508) 880-0179. **Circle No. 395**



High-voltage digital I/O board for VMEbus. The VMIVME-2128 has 16 8-bit bidirectional digital ports, each addressable via a pair of bytes on 8-, 16-, or 32-byte boundaries. The output driver circuits handle 990-mA surges before shutting down. Built-in test circuits isolate faults in real time. $1295. **VME Microsystems International Corp,** 12090 S Memorial Pkwy, Huntsville, AL 35803. Phone (800) 322-3616; (205) 880-0444. FAX (205) 882-0859. **Circle No. 396**

80186EB emulator. You can use the 186EB in-circuit emulator for firmware development of the 80186EB and 80188EB single-chip μPs. The emulator, which supports 131,072 hardware breakpoints and allows read, write, and fetch protection of specified areas of memory, comes with a source-level debugger for C and PL/M. $7500. **Softaid Inc,** 8300 Guilford Rd, Columbia, MD 21046. Phone (800) 433-8812; (410) 290-7760. FAX (410) 381-3253. **Circle No. 397**

Event-timing controller/monitor. The GT401 controller/monitor plugs into the 16-bit ISA bus. It includes a real-time clock with 1-μsec resolution, four I/O channels, and three 16-bit timer/counters. You can instruct the I/O channels to output specific numbers of pulses at predetermined real times or to time-stamp the edges of the input signals with a resolution of 400-nsec. The unit places the time stamps in dual-ported RAM that can be read from the ISA bus. $995. **Guide Technology Inc,** 920 Saratoga Ave, Suite 215, San Jose, CA 95129. Phone (800) 288-4843; (408) 246-9905. FAX (408) 246-0924. **Circle No. 398**

Ariel V-C40 Hydra Breaks the BOPS Barrier

1.1 billion operations per second sets the record for 6U VMEbus coprocessor cards

Only Ariel's Hydra combines four TI TMS320C40 DSPs to deliver twice the processing speed and four times the I/O bandwidth of any 6U VMEbus coprocessor card. It's the only choice for the most compute-intensive multiprocessor applications.

The V-C40 packs up to 64 Mbytes of DRAM as well as up to 5 Mbytes of SRAM in eight banks—two per processor. Each DSP has direct access to memory via dual 32-bit memory buses, as well as six parallel I/O ports and a high-speed six-channel programmable DMA controller. All six channels can transfer data simultaneously without interrupting program execution.

Hydra also includes a 24-bit parallel ADbus that lets you access a wide range of high-speed data acquisition cards. Development support includes an ANSI C compiler and the first PC-based XDS510 in-circuit emulator to support parallel processing. And of course, with Ariel's legendary technical support, you'll never work alone.

To learn more about the V-C40 Hydra, or any of Ariel's DSP products for ISA/EISA, VMEbus, SBus, Hewlett-Packard, NeXT, or Macintosh computers, send us a fax, leave us a message on the BBS or E-mail, or just give us a call.

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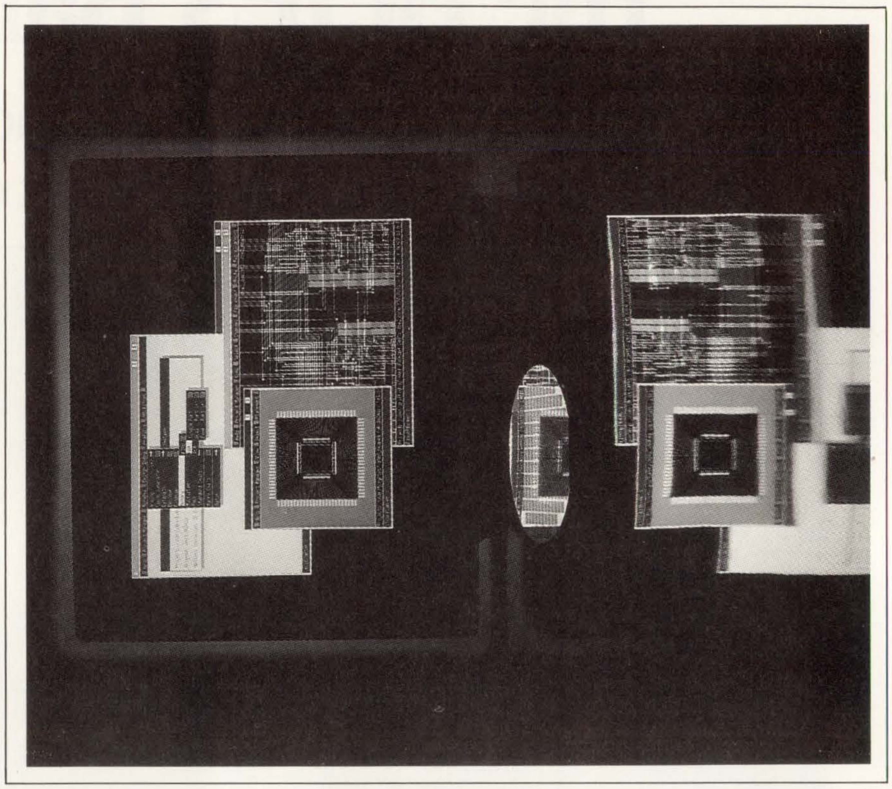
CIRCLE NO. 65

Migration Path For IC Silicon Compiler

- *Migrate Genesil designs to IC silicon compiler*
- *Features module libraries and IC place-and-route tools*



The Chipcrafter IC design software provides a migration path for users of Genesil, for which Mentor Graphics has announced it will discontinue support. The Chipcrafter software is an IC-design software tool set that features module libraries (standard cells, memories, and data-path elements), logic synthesis for glue logic (including finite state machines), and automated IC place-and-route tools. The libraries are technology and design-rule independent. The function-block library includes SSI standard cells and complex, high-performance data-path elements such as memories and analog functions. Users can modify these blocks for specific design needs and add the modified blocks to the library as new elements. The automatic place-and-route tools are user interactive. Users set the performance constraints to drive the tools and can interactively hand route. The tools also handle I/O buffer sizing, clock distribution, and power-rail sizing, all of which users can override for hand intervention. The tool set features a static timing analyzer and interfaces with Mentor Graphics and Valid Logic CAE tools for schematic capture and simulation. Chipcrafter modules, from $25,000; system, from $59,000. Until March 31, 1992, Genesil users can trade in their Genesil software to get a 45% discount for a special Chipcrafter package.

Cascade Design Automation, 3650 131st Ave, Suite 650, Bellevue, WA 98006. Phone (206) 643-0200. **Circle No. 399**

Bus-Design Timing-Analysis Tool

- *Generates detailed timing diagrams for signal analysis*
- *User selects bus-cycle type*

Busdesigner/AT reduces the hundreds of stringent timing specifications of the IBM AT, ISA, and EISA bus standards into a small group of requirements. The software lets a designer rapidly check a variety of architectures during a board's design stage. Once the designer settles on an architecture, the tool automatically generates timing diagrams complete with all timing margins for each type of bus cycle. Timing models include I/O, memory with wait states, DMA cycle, memory refresh, and bus-master arbitration. The tool flags and highlights all timing violations, thus providing a design check before you build actual circuits or run complex simulations. You can change specific components and analyze the effects on the bus interface. Busdesigner runs on top of the company's Timingdesigner graphical, interactive signal analyzer, which runs on PCs. Busdesigner/AT, $695; Timingdesigner for Windows, $995.

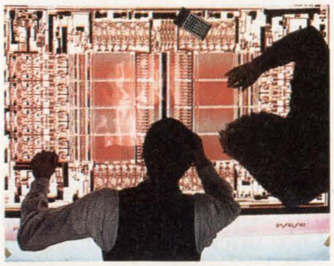
Chronology Corp, 2721 152 Ave NE, Redmond, WA 98052. Phone (206) 869-4227. **Circle No. 400**

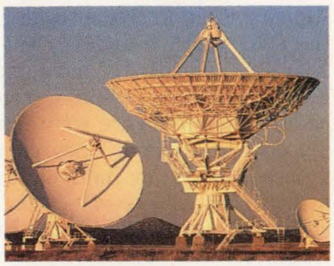
C-Compiler Package

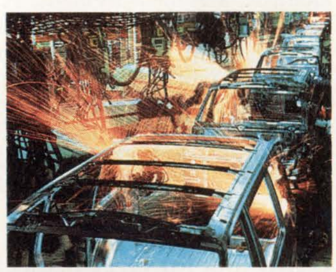
- *For 68000 series*
- *Offers increased compilation speed*

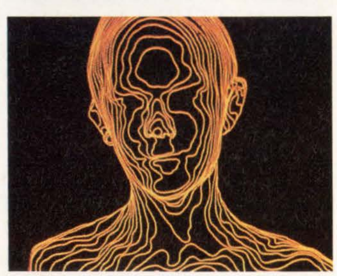
Version 5.1 of the Crosscode C compiler for the 68000 family of processors runs on IBM PC and Unix systems. It includes the Freeform source-code debugger and runtime utilities. Version 5.1's optimization techniques can provide a 40% speed up. IBM PC version, from $1995.

Software Development Systems Inc, 4248 Belle Aire Lane, Downers Grove, IL 60515. Phone (800) 448-7733; (708) 971-8170. FAX (708) 971-8513. **Circle No. 401**









PC-board design package. The PADS-2000 pc-board design package, Version 3.0 supports curved design tracks. You can define an arced or beveled miter at each route corner for curved tracks. This feature allows you to define as many as seven different mitering radii to meet line-curve requirements. The design package also provides improved copper handling for pour islands, pad-stack modification for individual components, and drill-hole checking. $6995. **CAD Software Inc,** 119 Russell St, Suite #6, Littleton, MA 01460. Phone (800) 255-7814; (508) 486-9521. FAX (508) 486-8217. **Circle No. 402**

Cross-development tools for MIPS architecture. The vendor has ported its C development tools for the MIPS architecture to other platforms. The R3000 RISC microprocessor software-development tools are now available on Sun-4 workstations and DEC VAX systems running the VMS operating system. The R3000 RISCross-development tool set, including C compiler, architecture (instruction-set) simulator, cache-memory simulator, and development utilities, $40,000. **Mips Computer Systems Inc,** 950 DeGuigne Dr, Sunnyvale, CA 94086. Phone (408) 720-1700. FAX (408) 524-7950. **Circle No. 403**

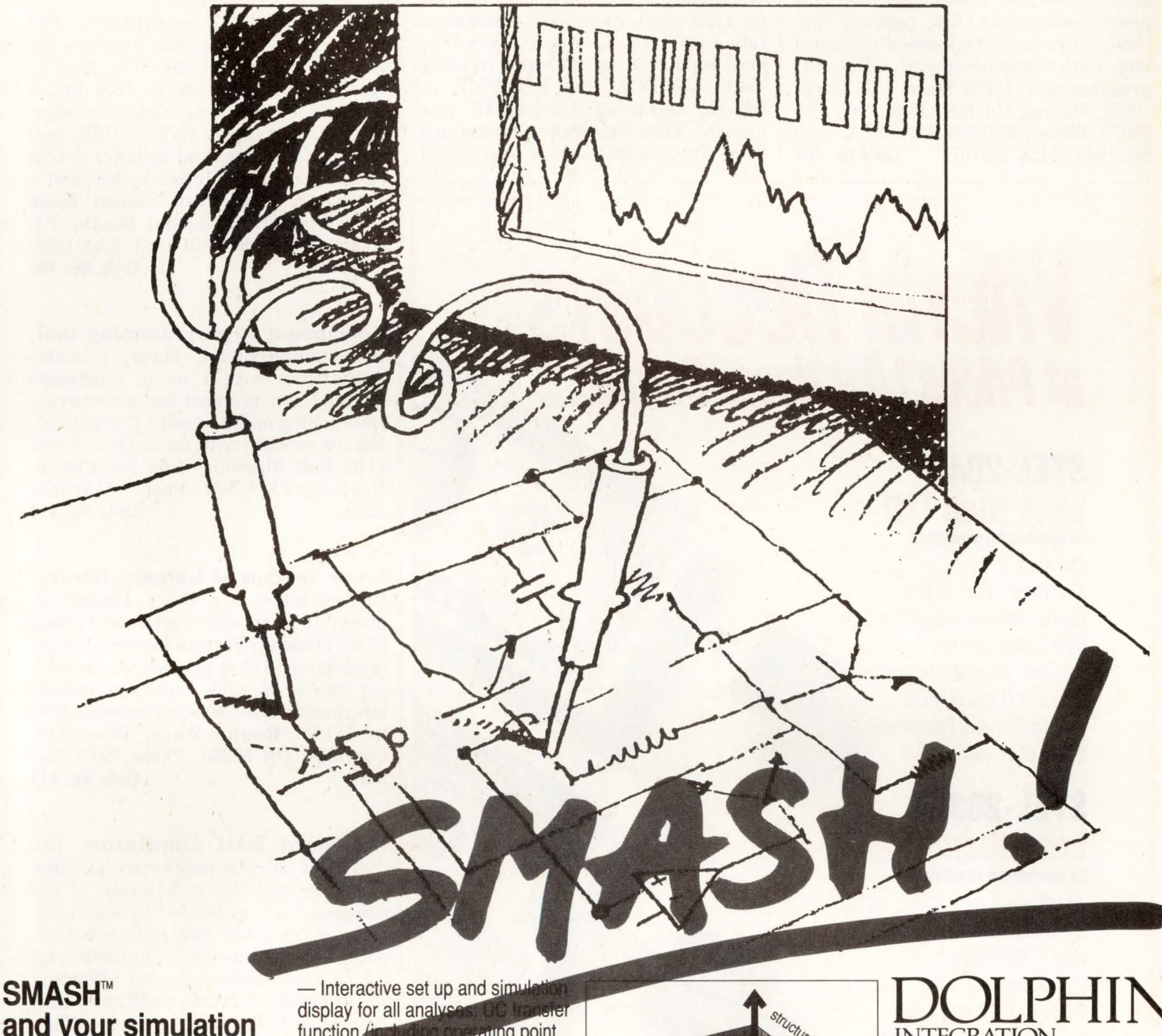
Optimized cross-assemblers for 8-bit microcontrollers. The Professional Optimized Cross-Assemblers support 8-bit microcontrollers such as the 8051, 6805, 68HC11, 8080/85, 6800, X80/180, and others, including the 16-bit 68000. These 2-pass, relocatable, macro assemblers are written in assembly code for speed. They come with a 2-pass linker, an independent locate utility that allows relocating without relinking, and a librarian. From $99. **Logisoft,** Box 61929, Sunnyvale, CA 94086. Phone (408) 773-8465. FAX (408) 773-8466. **Circle No. 404**

DSP application development tools for DSP 56001/96002. Hypersignal, an algorithm development package for the Motorola DSP56001 and DSP96002 DSP processors, supports real-time DSP algorithm development, analysis, and measurement. It provides spectrum analysis, a digital oscilloscope, frequency-domain displays, waveform editing, and real-time signal filtering. From $989. **Signalogic Inc,** 9704 Skillman #111, Dallas, TX 75243. Phone (214) 343-0069. FAX (214) 343-0163. **Circle No. 405**

CASE tool for large projects. Cohesion ASD/SEE (Aerospace-Defense/Software Engineering Environment) is a CASE (computer-aided software engineering) tool for large software-engineering projects. It includes a set of integrated CASE tools and services. Designed for large Ada projects, it supports DoD standards for configuration management and documentation. The system spans the entire product life cycle from specification to maintenance. From $25,000/seat. **Digital Equipment Corp,** Maynard, MA 01754. Phone (508) 467-5164. **Circle No. 406**

PLD programmer software. The PROMlink-6 software package for programming and editing PLD/FPGA programming data drives a device pro-

Simulator Multi-degree Analog-Structural Hierarchical on your personal workstation



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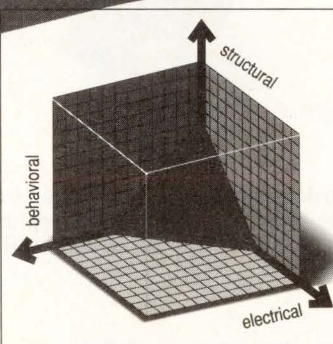
— Available on your personal computer (Mac, PC) and UNIX workstation (SUN...).

CIRCLE NO. 68



SMASH™ processes simultaneously 12000 gates, 250 transistors and 12000 steps or events.

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3333 Bowers Avenue
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Fax: (408) 727 - 2541

D01-1191A

grammer. Running under DOS, the software provides a windowed, easy-to-use interface. Users can select device types, download programming data, log errors, configure design files, and edit programming data. The package supports a 15k-baud, high-speed download link. $695; if purchased with a Data I/O programmer, $595. **Data I/O Corp,** 10525 Willows Rd NE, Redmond, WA 98073. Phone (206) 881-6444. FAX (206) 882-1043. TLX 152167. **Circle No. 407**

Software JPEG image-compression package. The Alice-DOS software package for software image compression compresses and decompresses JPEG images, both color and grayscale, for DOS applications. The compression ratio is 25:1 typ. The software handles most popular image file types, including Targa, Tiff, PCX, VIA, EPS, BMP, and DIB, as well as RGB and CYMK pixel formats. $195. **Telephoto Communications Inc,** 11722 Sorrento Valley Rd, Suite D, San Diego, CA 92121. Phone (619) 452-0903. FAX (619) 792-0075. **Circle No. 408**

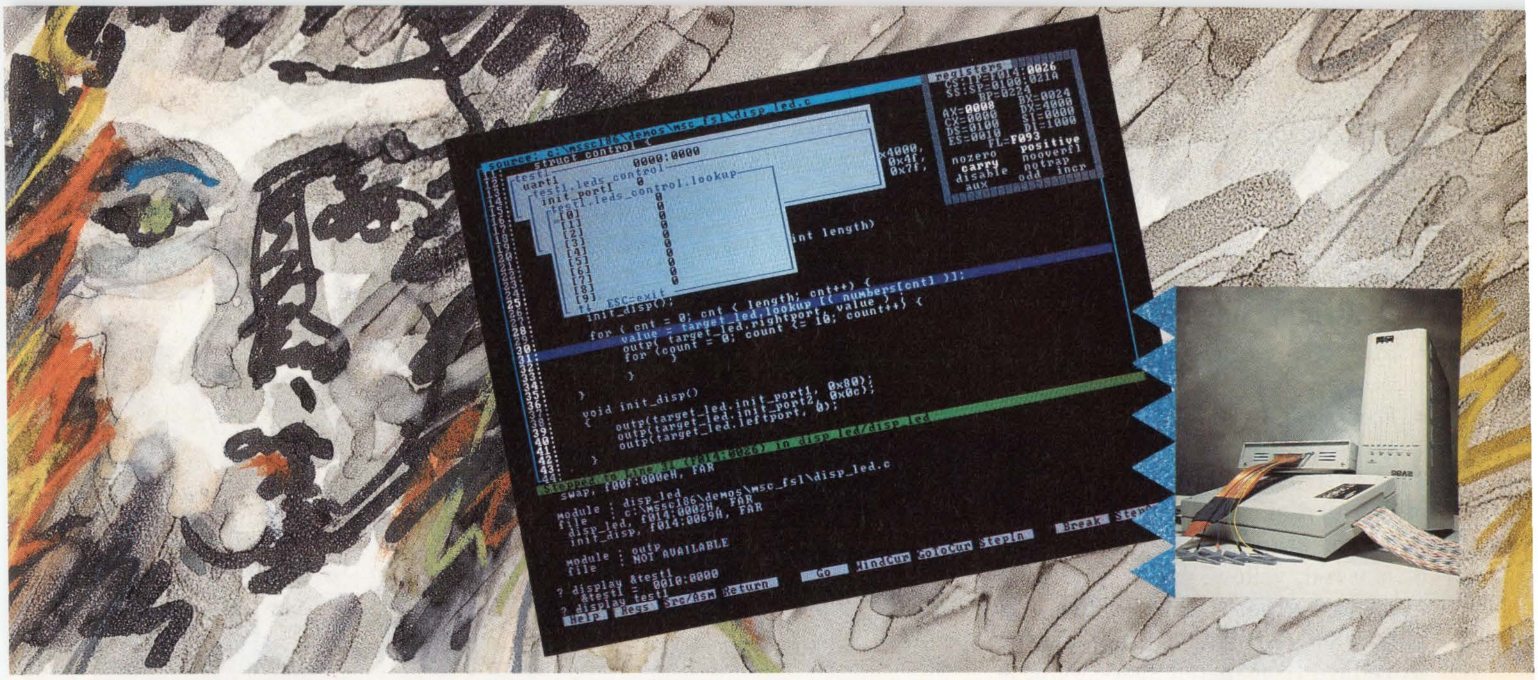
8051 Modula 2 compiler. The Modula 2 compiler is now available for the 8051 microcontroller. The Mod 51 cross-compiler runs on an IBM PC or compatible and is a single-pass compiler. It generates INTEL.HEX and INTEL.OBJ files, and includes a text editor, assembler, linker/loader, and a simulator. $1495. **Vail Silicon Tools Inc,** Box 165, Pompano Beach, FL 33069. Phone (305) 491-7443. FAX (305) 974-8531. **Circle No. 409**

Concurrent C programming tool. The Counterpoint C library provides applications with a set of constructs (parallel and process) for constructing and running multithreaded C programs. Future versions will run on Unix. From $149. **Soft Machines Inc,** Box 270806, Houston, TX 77277. Phone (713) 660-0269. **Circle No. 410**

C++ version of Linpack library. Linpack.h++ is a C++ Linpack library. It is an object-oriented version of the standard Fortran Linpack library procedures. These procedures for solving sets of multiple equations include incremental least-squares solvers. $299 to $1195. **Rogue Wave,** Box 2328, Corvallis, OR 97330. Phone (503) 754-2311. **Circle No. 411**

PC-board EMI simulator. The Swiftrad electromagnetic-emission simulator provides a 3-D map of the emission levels generated by board signals, an emission spectrum, error reports for excessive emission levels, and color-coded highlighting of offending track layouts. $35,000. **Swiftlogic Ltd,** Badenheath Pl, Cumbernauld, Glasgow, G68 9HX, Scotland. (0236) 720748. FAX (0236) 730983. **Circle No. 412**

Test synthesis compiler. Test Compiler, a logic-synthesis tool, builds in test for synthesized logic. Version 2.2 outputs test patterns for HDL (hardware-description-language) simulators. Optimizing and reducing test patterns saves test time. Test coverage is 99.5%. From $40,000. **Synopsys Inc,** 700 E Middlefield Rd, Mountain View, CA 94043. Phone (415) 962-50000. FAX (415) 965-8637. **Circle No. 413**



Power Debugging

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68020	20 MHz
NEC	
V20/V30	16 MHz
V40/V50	10 MHz
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V33	16 MHz
V53	16 MHz
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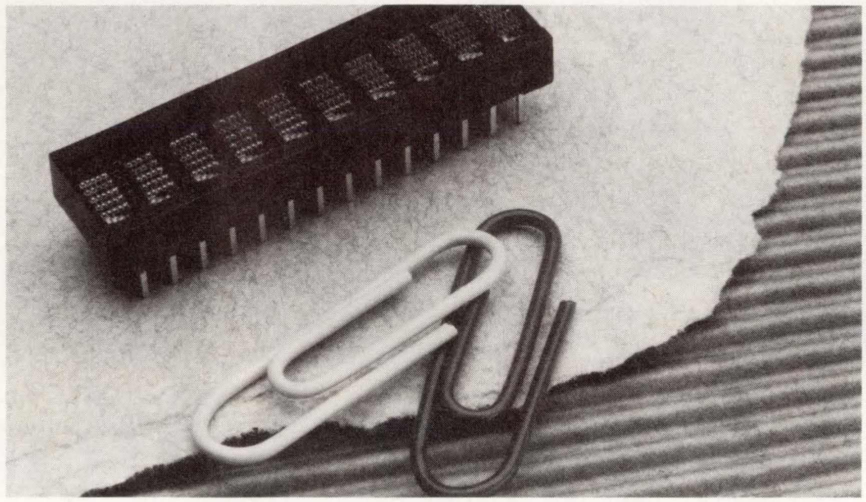
Sophia Systems Co., Ltd., Shinjuku NS Bldg. 8F, 2-4-1 Nishishinjuku, Shinjuku-ku, Tokyo 163, Japan, TEL: (03) 3348-7000 FAX: (03) 3348-2446

LED Display Modules

- *Capable of 10-character serial input*
- *Feature a 5×5 dot-matrix display*



The SCD558X 8-digit and SCD-5510X 10-digit LED display modules come in standard red, high-efficiency red, yellow, green, and high-efficiency green. The displays employ 5×5 dot-matrix LED arrays to reduce front-panel space by 60% and power consumption by 30% compared with figures for standard 5×7 dot-matrix displays. They work with the serial peripheral interface ports of most μPs. The units feature a 200-bit RAM to generate user-defined characters. The displays are X-Y stackable. The display modules feature a power-down mode that requires less than 250 mW. The units incorporate onboard intelligence, which includes column and row drivers that are easy to access through the serial interface. Operating range spans −40 to +85°C. Both displays are housed in 28-pin plastic DIPs. 8-digit model, $23.70 to $26.60; 10-digit model, $29.60 to $33.25 (100).

Siemens Components, Optoelectronics Div, 19000 Homestead Rd, Cupertino, CA 95014. Phone (408) 725-3423. **Circle No. 356**

Ethernet Transceivers

- *Meet IEEE standards*
- *Receiver has 58-dB dynamic range*

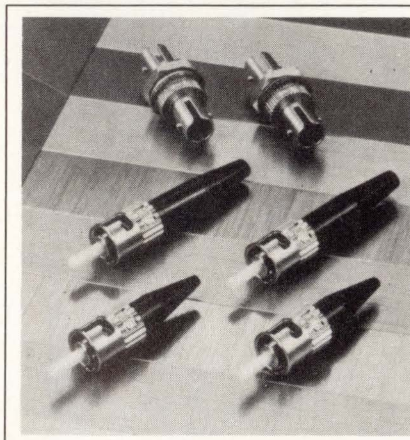
The AT-MX25F/MX26F Series Ethernet fiber-optic transceivers provide fiber-optic inter-repeater link (FOIRL) functions in accordance with IEEE standards. The receiver section has a 58-dB dynamic range at the optical input port. The unit automatically handles any transmission distance over a 0 to 1000m range without the need for any power-setting adjustments. Five diagnostic indicators continuously update unit status—LEDs indicate data-packet transmit and receive activities, collisions, timer expiration, and valid data links. A link monitor indicates low light-level transmissions. The transceivers are housed in a package that's less than 4 in.^{3} in size and weighs less than 3 oz. Electrical connections and power are supplied via a 15-pin D subminiature connector; the MX25F and MX26F units have SMA- and ST-type optical connectors, respectively. $495.

Allied Telesis Inc, 575 E Middlefield Rd, Mountain View, CA 94043. Phone (415) 964-2771. FAX (415) 964-0944. **Circle No. 357**

Optical Connectors

- *Are ST compatible*
- *Designed for field termination*

SLP Type II Series ST-compatible fiber-optic connectors consist of three pieces—housing, crimp ring, and boot. The units are designed for field termination and accommodate either multi- or single-mode fibers. The devices employ a zirconia ceramic ferrule to maximize ferrule hole concentricity. Connector insertion loss is specified at 0.2 dB typical for either type of fiber. Return losses are better than 40 dB. The housing incorporates a wraparound shell design that protects the adapter sleeve from dirt contamination. The connectors are available with either a 3-mm black boot or a 0.9-mm black boot; they can also be



ordered in a kit that contains both boots. The connector is compatible with industry-standard tooling. $6.50 (100).

Seiko Instruments USA Inc, Electronic Components Div, 2990 W Lomita Blvd, Torrance, CA 90505. Phone (213) 517-7786. FAX (213) 517-7792. **Circle No. 358**

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"meeting your needs"
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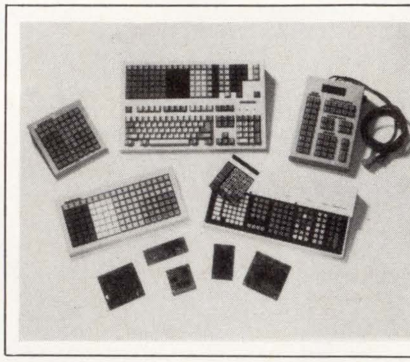
CIRCLE NO. 40



Modular keyboards. These POS (point of sale) keyboards are available in standard configurations of 8×8, 18×7, and 16×8 keys; however, you can specify units with positions ranging from a few keys to hundreds of keys. Each of the keyboards shares the same software, allowing for complete reprogrammability of each key and easy modification and upgrading. The base configuration features full-travel key switches rated for 20 million operations. Clear snap-on keytops allow easy insertion of user-created legends. $200 to approximately $500. **Genovation Inc,** 17741 Mitchell N, Irvine, CA 92714. Phone (714) 833-3355. FAX (714) 833-0322. **Circle No. 359**

Insulation displacement connectors. These 50-position D subminiature connectors are available in male and female versions. They accept 0.05-in. pitch cable. The connectors are rated for 1 to 1.5A per contact depending on wire size. Operating range spans −50 to +105°C. Contacts are beryllium copper with gold plating, and the polyester housing has a UL 94V-0 rating. $5.53 and $5.35 (1000) for male and female versions, respectively. **ODU USA,** 4620 Calle Quetzal, Camarillo, CA 93012. Phone (805) 484-0981. FAX (805) 484-7458. **Circle No. 360**

Wirewound surface-mount inductors. Series 1010 molded inductors are available in the standard 1010 EIA envelope size. Inductance values range from 0.01 to 0.1 μH for parts with phenolic cores and from 0.12 to 27 μH for parts with ferrite cores. Standard tolerance is 10%. Terminations are solder-coated copper per MIL-STD-202. $0.70 (1000). Delivery, four to six weeks ARO. **American Precision Industries,** 270 Quaker Rd, East Aurora, NY 14052. Phone (716) 652-3600. **Circle No. 361**

Actual Size

Which One Has More Chips In It?

If you guessed the TDK Multilayer Chip LC Filter on the right, you're correct.

This unique device integrates 7 capacitors, 2 inductors, and 2 transformers for a total of 11 chips into a single band pass filter.

How do we do it? Multilayers of ferrite material, dielectric ceramic material, conductive material and internal electrode are all woven together and sintered simultaneously.

Only TDK has the thick film composition know-how needed to manufacture chip LC Filters, Transformers, IFTs and other multi-layer components that save valuable design space while they increase overall product reliability.

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CIRCLE NO. 74

3M Reduces Solvents Used In Electrical Tape Manufacturing

Reduction of solvent usage assures users of future tape availability as worldwide environmental concerns heighten

AUSTIN, Tex. — The 3M Electrical Specialties Division is implementing solvent reduction processes in the manufacture of OEM insulating electrical tapes. The established goal is to reduce solvent purchases and usage by 80 percent.

Customers incorporating these insulating tapes in present products, re-designs and new products will be assured of a reliable source well into the 21st Century.

New sixteen page brochure describes over 50 Scotch electrical tapes for OEM applications, and other electrical insulation products.

3M is also taking a holistic view of its efforts to achieve a cleaner environment, believing that it is important to examine the full scope of a product's impact on the environment – beginning with product design and the manufacturing process, and extending to product usage, packaging and disposal.

The tapes are designed for use in OEM electrical applications to insulate, hold, protect and identify electrical conductors, components and circuits. Solvent reduction processes will be extended to as many OEM electrical tapes as possible. The following tapes with a thermosetting rubber-resin adhesive have already been released:

No. 2 and 38 Crepe Paper
No. 27 Glass Cloth
No. 46, MR 98 Polyester Film/ Glass Filament
No. 44, 55, 1174, MR 93, MR 93B, MR 94, MR 94B Polyester Film/MAT
MR 96 Polyester Film

For more information, contact a 3M Electrical Specialties Division representative or authorized distributor, or call 1-800-233-3636.

3M Electrical Specialties Division
6801 River Place Boulevard
Austin, Texas 78726-9000

3M

CIRCLE NO. 75

Components & Power Supplies

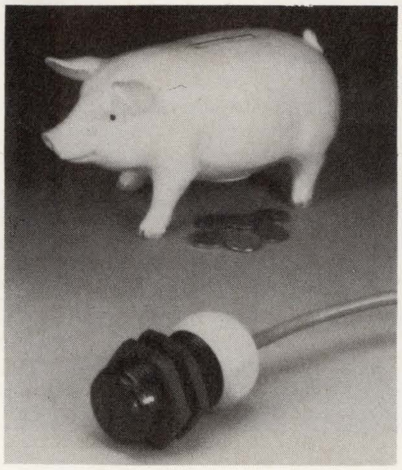
Monolithic MOSFETs. TopFET devices feature a host of built-in protection features. They include overtemperature protection for junction temperature above 150°C, short-circuit load protection, overvoltage clamping for inductive loads, input ESD protection, and reverse battery protection. Maximum on-state resistance ranges from 28 to 100 mΩ, and maximum continuous drain-source voltage equals 50V. $2.25 (1000). Delivery, 12 to 16 weeks ARO. **Philips Components,** 2001 W Blue Heron Blvd, Riviera Beach, FL 33404. Phone (800) 447-3762; (407) 881-3342. **Circle No. 362**

PGA sockets. The PZA447H509B5-39C-R socket is designed for the Mips R4000 processor. Contact area is gold plated. The units are available with either FR4 and PPS thermoplastic housings. Both of these versions are compatible with vapor-phase and infrared soldering systems. $35.18 (1000). **McKenzie Technology,** 44370 Old Warm Springs Blvd, Fremont, CA 94538. Phone (510) 651-2700. FAX (510) 651-1020. **Circle No. 363**

Coaxial adapters. Model PE9342 type BNC female to type mini-UHF coaxial adapters feature low loss over a range of dc to 4 GHz. The 50Ω units have brass nickel-plated bodies and utilize Teflon insulators. The contact is gold plated. The adapters operate over a −65 to +165°C range. $5.95. **Pasternack Enterprises,** Box 16759, Irvine, CA 92713. Phone (714) 261-1920. FAX (714) 261-7451. **Circle No. 364**

Power amplifiers. The solid-state Class AB linear amplifiers in the PA900 Series cover an 850- to 900-MHz frequency band. They operate from a supply voltage of 25V. Output power values range to 100W, and gain figures range from 19 to 45 dB. $1010 to $1230 (10). Delivery, 16 weeks ARO. **Motorola RF Products Div,** 325 Maple Ave, Torrance, CA 90503. Phone (213) 783-5785. FAX (213) 783-5790. **Circle No. 365**

Transient-voltage suppressors and filters. PQI Series interfaces combine voltage suppression and RFI filtering in a single package. The units feature a 205V pk clamping level, 95J energy dissipation, less than 1-nsec single-stage response time, and a 3000A surge withstand capability. The units are housed in an ABS plastic package and come with a line cord. $75 to $229. **Superior Electric,** 383 Middle St, Bristol, CT 06010. Phone (203) 582-9561. **Circle No. 366**



Photoelectric sensor. C30 Series infrared sensors operate in a retroreflective mode and have a 16-ft sensing range. The units are self-contained and operate from a 10V dc source. A red LED indicates the presence of a sensor output. The sensors are sealed against moisture and carry a NEMA 6 rating. The sensors are available for either light or dark operation. $36. **Banner Engineering Corp,** Box 9414, Minneapolis, MN 55440. Phone (612) 544-3164. **Circle No. 367**

Metal film resistors. Type ELR-07 metal film resistors, with values ranging to 22 MΩ, are rated for 250 mW, are available in tolerances of ±2, ±5, and ±10%, and have a temperature coefficient of ±350 ppm/°C. $0.51 (1000) for a 22 MΩ, ±2% model. Delivery, 11 to 12 weeks ARO. **Dale Electronics Inc,** Box 609, Columbus, NE 68602. Phone (402) 371-0080. **Circle No. 368**

Bus connector. This Semconn connector is designed for the Access.bus link. The 71565 Series receptacle is available in through-hole and surface-mount versions with either full or partial shielding. Series 71564 plugs ground the cable shield to the plug shield to ensure a stable ground path. Receptacle, $1992 to $2775; plug, $1409 (1000). **Molex Inc,** 2222 Wellington Ct, Lisle, IL 60532. Phone (708) 969-4550. FAX (708) 969-1352. **Circle No. 369**

Optical switch. The EE-SA105 optical switch operates without a contact mechanism. It activates with a 15g operating force and has a 0.059-in. pretravel. The LED operates with 50-mA forward current and develops an output of 0.5 mA min. The switch output is high when the actuator is in the rest position and has a dark current of 200 nA max when the plunger reaches the end-of-travel position. From $0.99 (5000). **Omron Electronics Inc,** 1 E Commerce Dr, Schaumburg, IL 60173. Phone (708) 843-7900. FAX (708) 843-7787. **Circle No. 370**

Circular connectors. These MIL-C-5015-style plastic circular connectors mate with metal-shell MIL-C-5015 style connectors in shell sizes 20-14 and 18-10. They feature a housing design that prevents mating when insert arrangements are incompatible. The pin and socket contacts are available in reel-mounted strip form as well as in loose-piece form connectors and are compatible with panel or cable applications. $11 to $16. Delivery, six weeks ARO. **AMP Inc,** Box 3608, Harrisburg, PA 17105. Phone (800) 522-6752. **Circle No. 371**

Pin-grid-array sockets. GSM Series PGA sockets are surface mountable. They are available in standard footprints ranging from 8×8 to 20×20. The butt-style terminals are available with tin-lead plating and the FR-4 insulator meets the temperature requirements of vapor-phase soldering systems. $0.030 per pin (1000). Delivery, four to six weeks ARO. **Augat Inc,** 452 John Dietsch Blvd, Attleboro Falls, MA 02763. Phone (508) 699-9800. FAX (508) 699-6717. **Circle No. 372**

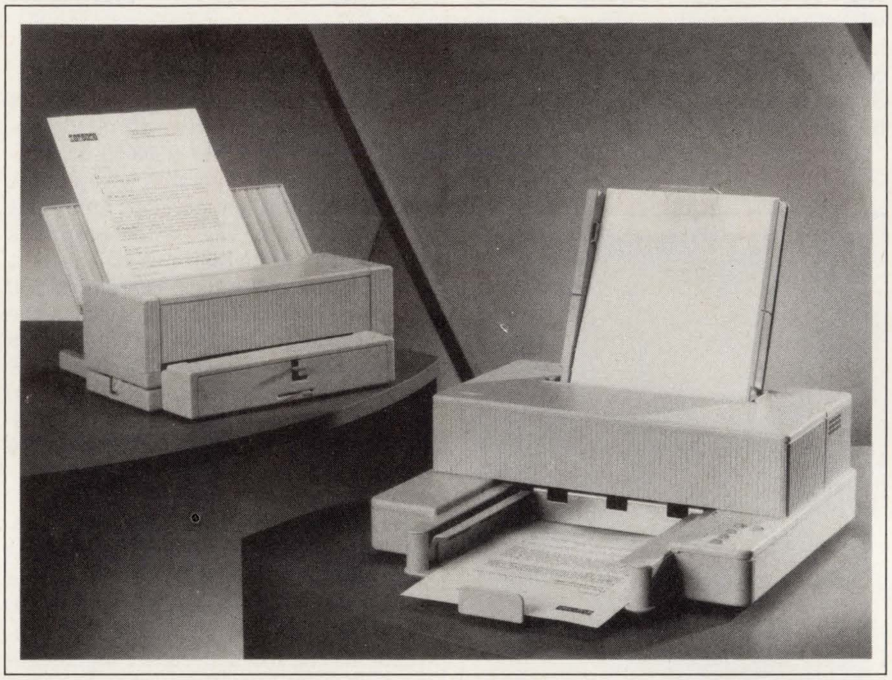
High-current connectors. EX5-R and IL-AG5 Series connectors are rated for 8 and 3A per contact, respectively. They feature nylon housings that have a UL 94V-2 rating. Additional specifications include an 1800V ac withstanding voltage, 109Ω insulation resistance, and a 10 mΩ contact resistance. Less than $1 (1000). **JAE Electronics,** 142 Technology Dr, Bldg 100, Irvine, CA 92718. Phone (800) 523-7278 (except in CA and AK); (714) 753-2600. FAX (714) 753-2699. **Circle No. 373**

Computers & Peripherals

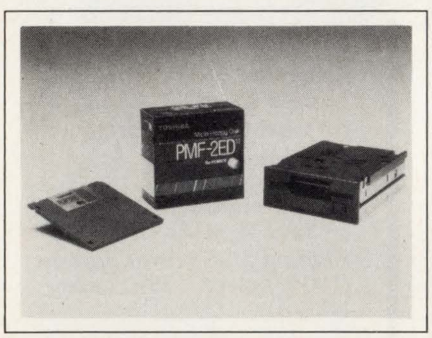
Ink-Jet Printer

- *Prints monochrome graphics at 300 dpi*
- *Prints at 360 cps in draft- and 120 cps in letter-quality modes*

The DECjet is a monochrome ink-jet printer for DOS-compatible computers. The unit prints graphics at 30×300 dpi. The unit also prints four resident and seven optional fonts at 600×300 dpi. The four resident fonts are Courier, Landscape Courier, Letter Gothic, and Times Roman. The printer comes standard with a 150-pg sheet feeder, and you can opt for an additional 150-pg sheet feeder. Three modes print at 360 cps for high-speed draft, 240 cps for draft, and 120 cps for letter quality. The printer has a Centronics parallel port and emulates an HP Deskjet Plus printer (HP-PCL 3). Other features include 44-dBA operation and replaceable print head/ink supply cartridge, as well as envelope, selected transparencies, letter, and A4 paper printing. $795.



Digital Equipment Corp, Maynard, MA 01754. Phone (508) 635-8290. **Circle No. 414**



3½-in. Floppy-Disk Drive

- *Has 4-Mbyte capacity and 1-Mbps transfer rate*
- *Drive consumes 1.8W and resists 1.0g vibration while operating*

The ND-3571 is a 3½-in., 4-Mbyte floppy-disk drive. The drive uses the company's patented perpendicular-recording technology. The technology uses barium ferrite particles for the recording media, which permits the particles to be magnetized vertically. Vertical magnetization permits higher bit density than conventional horizontal magnetization. The drive has a 3-msec track-to-track access time and transfers data at 1 Mbps. The drive consumes 1.8W and can withstand 1g vibration while operating. The unit measures 1×4×6-in. and weighs 1 lb. $100 (OEM); $160 with installation kit.

Toshiba America Information Systems Inc, Disk Products Div, 9740 Irvine Blvd, Irvine, CA 92718. Phone (714) 583-3000. **Circle No. 415**

Dual-Channel Ethernet Boards

- *Communicate with two subnetworks simultaneously*
- *EISA bus master boards come with Netware v3.1 drivers*

The 3032/EISA dual-channel Ethernet boards communicate with two subnetworks simultaneously. The 2-channel design conserves expansion slots and costs less than two single-channel boards. The boards have dual transceivers that connect to twisted-pair or thin coaxial cable. An attached unit interface provides a connection to other media. The boards can automatically switch between bus-master burst mode (when transferring large blocks of data) and slave I/O mode (when transferring small blocks of data). Each channel has a 64-kbyte buffer, which permits double buffering of transmission packets during burst mode. The boards come with Netware v3.1 drivers and have automatic configuration and diagnostic-test programs. 10Base-T or coaxial model, $945.

Standard Microsystems Corp, 80 Arkay Dr, Hauppauge, NY 11788. Phone (800) 762-4968; (516) 273-3100, ext 5317. **Circle No. 416**

Text continued on pg 170

What's to get excited about in a power supply?

Ple

Auto-selectable AC input.

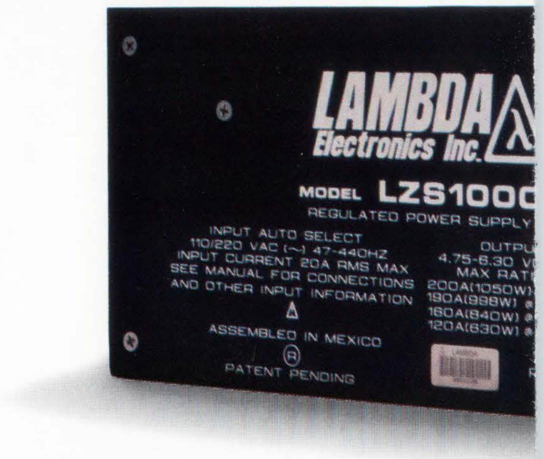
AC power fail signal.

DC overvoltage signal.

DC undervoltage signal.

Inverter good signal.

Overtemperature protection.



Lambda introduc

REGULATED VOLTAGE
Line: 0.1% from 85 to 132VAC or 170 to 265VAC.
Load: 0.1% from no load to full load.
Ripple and noise:
10mV RMS, 35mV pk-pk on LZS-1000-1;
10mV RMS, 50mV pk-pk on LZS-1000-2.
15mV RMS, 100mV pk-pk on LZS-1000-3.
Temp. coeff.: 0.025%/°C.

INPUT POWER
AC: 85-132VAC/170-265VAC auto selectable single phase, 47-440 Hz.
DC: 220-375VDC.

EFFICIENCY
75% typical.

OPERATING TEMPERATURE RANGE
-30°C to +71°C with suitable derating above 40°C.

OVERTEMPERATURE PROTECTION
Via internal thermostat.

FUSING
Externally accessible.

OVERVOLTAGE PROTECTION
Adjustable.

OVERLOAD PROTECTION
External overload protection, automatic electronic current limiting limits the output to a preset value thereby protecting the load as well as the power supply.

COOLING
Integral fan.

IN-RUSH CURRENT LIMITING
Not to exceed 45A for 85 to 132VAC; 78A for 170 to 265VAC.

CURRENT SHARING
Single wire connection.

REMOTE SENSING
Compensation for 0.5VDC drop in output load cables.

REMOTE ON/OFF
Logic "0" open or short = Off.
Logic "1" = On.

REMOTE PROGRAMMING
Resistive: 1000Ω/V.
Voltage: Volt per volt.

enty.

Current sharing.

-30°C to +71°C.

EMI compliance to FCC, VDE 0871, Class B.

UL/CSA/TUV/SELV compliant.

5 year guarantee.

ces the LZ Series.

POWER FAILURE
"-1" model will remain within regulation limits for at least 16.7 msec. after loss of AC power when Vout ≤ 5.25, Vin ≥100VAC.

INDICATORS
Overvoltage/overtemperature LED and output voltage good LED.

ENVIRONMENTAL SPECIFICATIONS
Per MIL-STD-810D.

EMI
FCC Class B; VDE 0871Class B; MIL-STD-461A, Part7, CE04.

INPUT LINE DISTURBANCES
IEEE-587 Category A, VDE 0160.

PHYSICAL DATA
Dimensions: 4.75 x 5.63 x 10.50 inches.
Weight: 15 lbs.

SAFETY AGENCY APPROVALS
Under evaluation for UL, CSA, TUV.

GUARANTEE
Five year guarantee includes labor as well as parts. Lambda Grade 1 design.

Model	Output Voltage Adj. Range (VDC)	Max Current (Output Power) at Operating Temperature Of				Price*		
		40°C	50°C	60°C	71°C	Qty. 1	Qty. 10	Qty. 25
LZS-1000-1	4.75 - 6.30	200.0 (1050)	190.0 (998)	160.0 (840)	120.0 (630)	$1130	$1075	$1025
LZS-1000-2	11.40 - 15.75	83.0 (1050)	80.0 (998)	67.0 (840)	50.0 (630)	$1130	$1075	$1025
LZS-1000-3	19.0 - 29.4	50.0 (1050)	48.0 (998)	40.0 (840)	30.0 (630)	$1130	$1075	$1025

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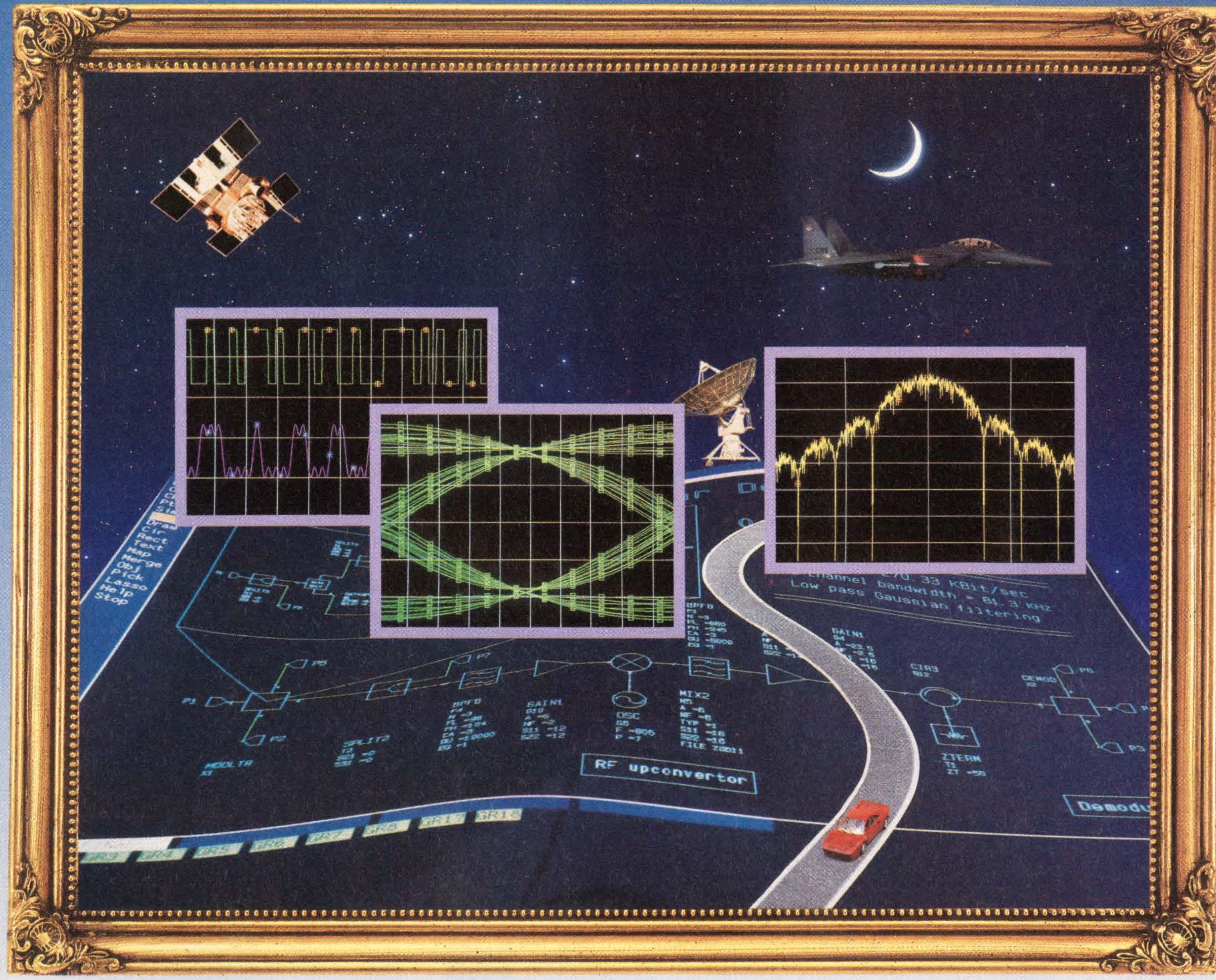

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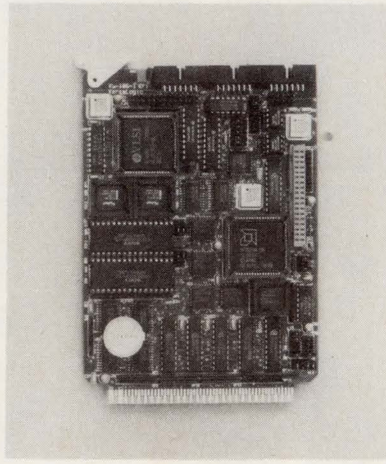
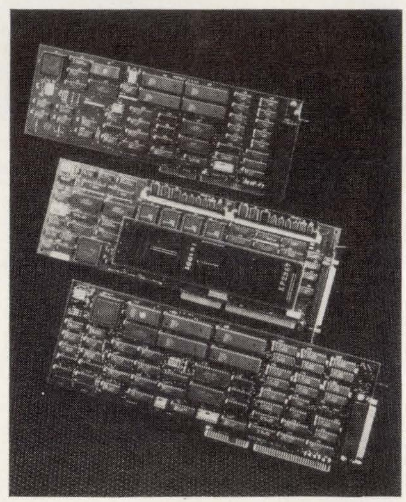
STD bus CPU board. The VL-186-1 transfers 16-bit data in an STD 80- or STD 32-compatible system. The board features a 16-MHz 80C186 µP, as much as 1 Mbyte of EPROM or 256 kbytes of Flash EEPROM, and as much as 1 Mbyte of static RAM with battery backup. Other features include two COM ports, a parallel printer port, three 16-bit timer/counters, two programmable DMA channels, a watchdog timer, and an SBX expansion connector. $645. **Versalogic Corp,** 3888 Stewart Rd, Eugene, OR 97402. Phone (800) 824-3163. FAX (503) 485-5712. **Circle No. 418**





Multiport serial boards. The ACL II+, ACL IIR+, and ACL 16+ multiport serial boards use communication chips that can transfer and receive asynchronous data as fast as 115 kbaud. ISA, EISA, and Micro Channel boards are available. The ACL II+ has eight programmable ports and an RS-232C connector. $1125 to $1195. The ACL IIR+ has eight programmable ports and RJ-12 connectors. $725 to $795. The ACL 16+ has 16 programmable ports and three handshake options. $1495 to $1995. **Star Gate Technologies Inc,** 29300 Aurora Rd, Solon, OH 44139. Phone (800) 782-7428; (216) 349-1860. FAX (216) 349-2056. **Circle No. 419**

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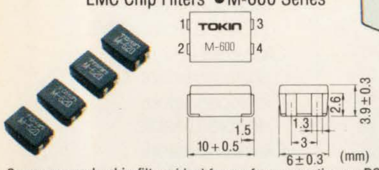

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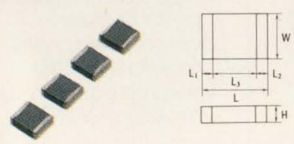

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C505 (SE)	5.0±0.4	5.6±0.5	3.0 max.	0.3~2.5	0.3 min.
C408 (SA)	4.0±0.4	8.0±0.5	3.2 max.	0.3~2.5	0.3 min.
C610 (SB)	6.3±0.4	10.0±0.5	4.5 max.	0.3~2.5	0.3 min.
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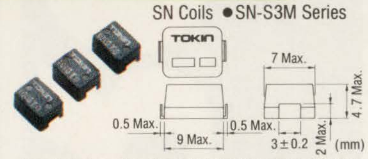

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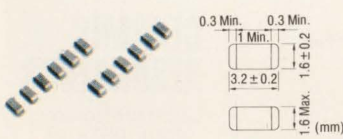

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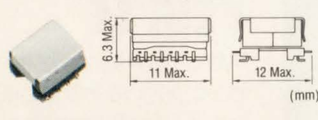

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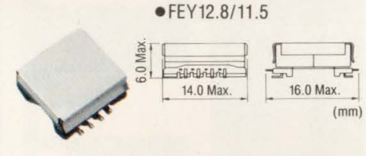

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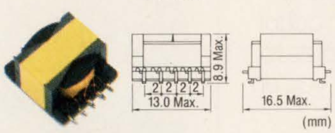

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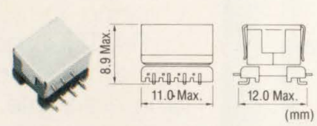

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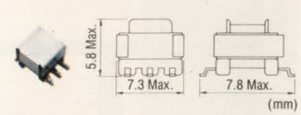

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Software and hardware catalog. This 1992 catalog offers an abundance of software and hardware products for developing instrumentation systems. It features five color-coded sections—Application Software, IEEE-488, Data Acquisition, VXI/MXI, and Training. The first four sections of the 544-pg publication provide tutorials on IEEE.488.2, SCPI (standard commands for programmable instruments), plug-in data-acquisition systems, VXI, and MXI. The tutorials deal with applications for instrument control, data acquisition, test and measurement, and similar applications. **National Instruments,** 6504 Bridge Point Pkwy, Austin, TX 78730. **Circle No. 351**

Listing of DSP development tools. This "line card" for DSP development tools complements a DSP-processor line card that the company published previously. The card summarizes the software and hardware development tools that the vendor or third parties offer for fixed- and floating-point DSP families. Included in the listing are assemblers, linkers, simulators, C compilers, debuggers, evaluation boards, emulators, PC plug-in boards, signal-processing software, filter design software, and a real-time kernel/operating system. **Analog Devices,** Box 9106, Norwood, MA 02062. **Circle No. 352**

Step-down-switching app note. The application note, *AN35: Step Down Switching,* explores high-efficiency switching-regulator designs for stepping down the primary power supply of a system. Schematics with comments and advice for more than 20 power-supply systems show sources for the inductors used in the designs. Useful advice helps experienced—as well as inexperienced—power-supply designers to design pc boards, add-on cards, or system modules. **Linear Technology Corp,** 1630 McCarthy Blvd, Milpitas, CA 95035. **Circle No. 353**

Calibration and instrumentation listings. Representing the TE Product Line, this catalog includes resistance and capacitance decade boxes, portable thermocouple simulators, and 11 different voltage and current-calibrator models. It also details the range of programmable IEEE-488 Bus test equipment that is available. The publication provides specifications, illustrations, and features of each product listed. **Zi-Tech Instrument Corp,** Box 51845, Palo Alto, CA 94303. **Circle No. 354**

Catalog of distributor products. This 20-pg catalog provides information and photos for handheld and benchtop multimeters and digital thermometers and accessories. It also specifies Philips' timers and counters, frequency counters, and DMMs. **John Fluke Mfg Co Inc,** Box 9090, Everett, WA 98206. **Circle No. 355**

Acronyms and abbreviations chronicled. The 209-pg *Dictionary of Information Technology and Computer Acronyms, Initials, and Abbreviations* targets a plethora of potential users. Hardcover, $24.95; paperback, $12.95. **McGraw-Hill Inc,** Professional Book Group, 11 W 19th St, New York, NY 10011. **INQUIRE DIRECT**

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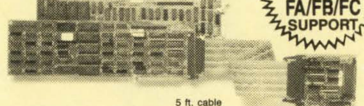

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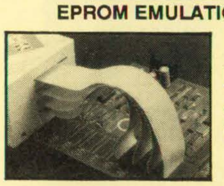

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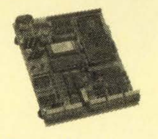

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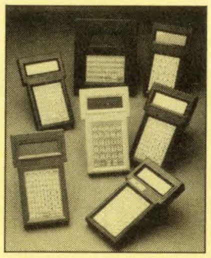

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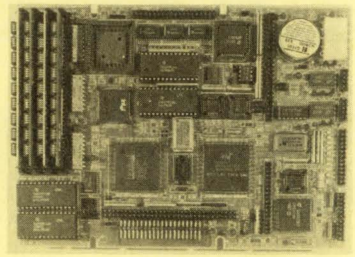

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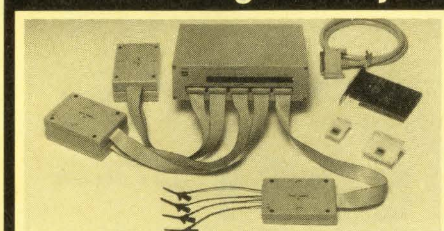

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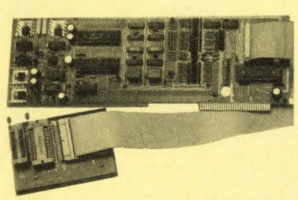

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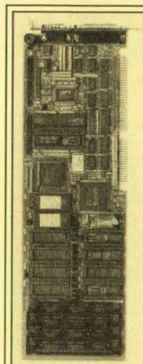

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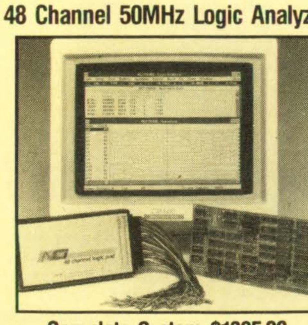

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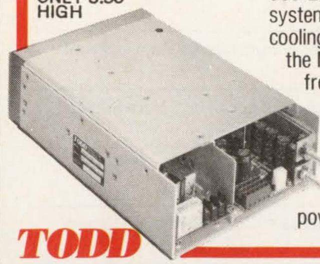

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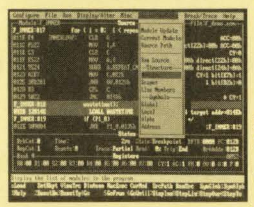

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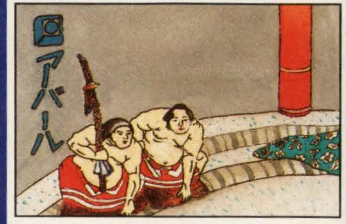

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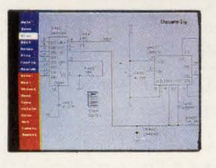

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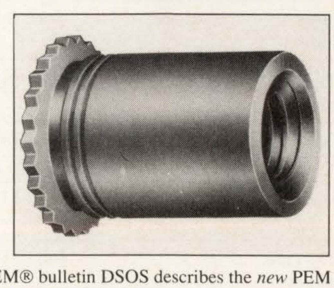

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1992 Recruitment Editorial Calendar

Issue	Issue Date	Ad Deadline	Editorial Emphasis
News Edition	Feb. 6	Jan. 23, '92	STATE OF ENGINEERING Special Supplement • Computers & Peripherals • Communications Technology • Annual Salary Survey
Magazine Edition	Feb. 17	Jan. 23	EDN's 35th Anniversary Issue • ASICs • ICs & Semiconductors • Test & Measurement • Manufacturing Issues
News Edition	Feb. 20	Feb. 6	ICs & Semiconductors • ISSCC Hot Products • Computers & Peripherals • Regional Profile: Colorado, Utah, Idaho
Magazine Edition	Mar. 2	Feb. 6	COMMUNICATIONS SPECIAL ISSUE • Test & Measurement • Local-area Networks • Microprocessors • Memory Technology
News Edition	Mar. 5	Feb. 20	Memory Technology • CPU Boards • Computers & Peripherals • Diversity Special Series
Magazine Edition	Mar. 16	Feb. 20	COMPUTER & PERIPHERAL SPECIAL ISSUE • Multimedia • Components • Memory Technology • Computer Peripherals • International Technology Update—Japan
News Edition	Mar. 19	Mar. 5	DSP Software • Communications • Regional Profile: New York, New Jersey, Pennsylvania
Magazine Edition	Mar. 30	Mar. 5	Microprocessors • Analog Circuits • CAE • Test & Measurement
SOFTWARE ISSUE	Mar. 30	Mar. 5	SOFTWARE ENGINEERING SPECIAL ISSUE • (To be polybagged with the March 30th Magazine Edition issue)
News Edition	Apr. 2	Mar. 19	ICs & Semiconductors • Multimedia Software/Development Tools • Engineering Management Special Series
Magazine Edition	Apr. 9	Mar. 19	CAE • EDN Hands-on Special Project—Part I: Field-programmable Gate Arrays • Software • Memory Technology
Magazine Edition	Apr. 23	Apr. 2	Portable Computer Design • EDN Hands-on Special Project—Part II: Field-programmable Gate Arrays • Electromechanical Devices • Computer Peripherals
News Edition	Apr. 30	Apr. 16	ASICs SPECIAL ISSUE • FPGAs and EPLDs • CICC Hot Products • ASICs • Regional Profile: Northern California
Magazine Edition	May 7	Apr. 16	Communications/Networks • Test & Measurement • Surface-Mount Components • Power Sources • Electro Show & Products Issue
ELECTRO SHOWGUIDE & PRODUCT SPOTLIGHT		Apr. 3	A free page available to all advertisers running a full page in 2 out of 3 Electro issues
News Edition	May 14	Apr. 30	Graphics Technology • Computers & Peripherals
Magazine Edition	May 21	Apr. 30	Analog ICs • Analog CAE • PC Board CAE Tools • Programmable-Logic Devices
News Edition	May 28	May 14	Communication ICs • CAE Software • Regional Profile: Texas, Oklahoma, Kansas
Magazine Edition	June 4	May 14	ASICs/PLDs • DSP Software • CAE/Software/Interoperability • Digital ICs & Semiconductors
News Edition	June 8	May 21	CAE SPECIAL ISSUE • EDA/CASE Supplement • DAC Hot Products • Software Engineering • Diversity Special Series
Magazine Edition	June 18	May 28	Microprocessors • Electromechanical Devices • ICs & Semiconductors
SOFTWARE ISSUE	June 18	May 28	SOFTWARE ENGINEERING SPECIAL ISSUE (To be polybagged with the June 18th Magazine Edition issue)
News Edition	June 25	June 11	MILITARY ELECTRONICS SPECIAL ISSUE • DSP Hardware • Military Electronics • Regional Profile: Florida, Alabama
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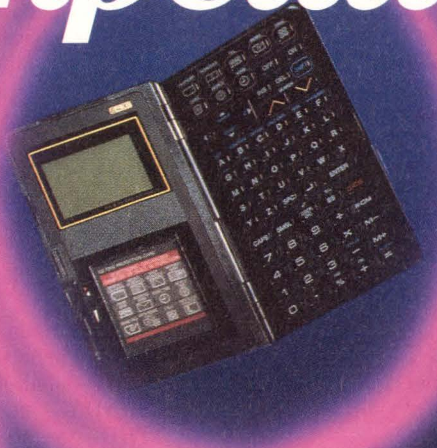

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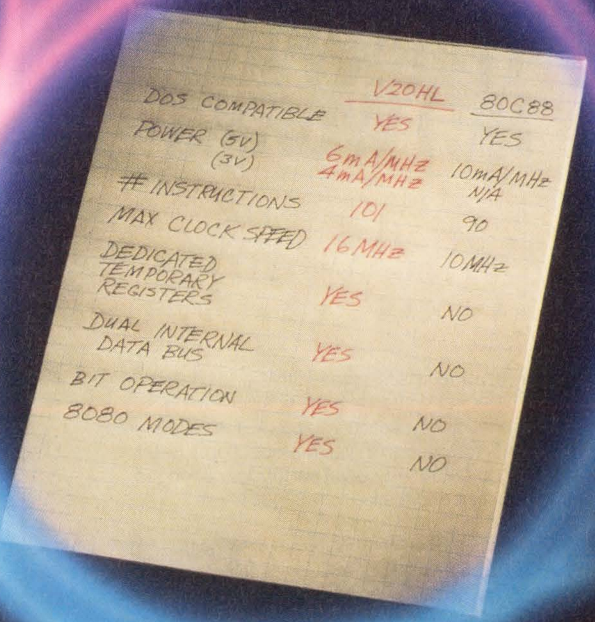

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EDN-ACRONYMS & ABBREVIATIONS

ADC—analog-to-digital converter
ALU—arithmetic and logic unit
ASIC—application-specific integrated circuit
BiMOS—bipolar metal-oxide semiconductor
CALDAC—calibration DAC
CAPDAC—capacitor DAC
CMOS—complementary metal-oxide semiconductor
CPU—central processing unit
DAC—digital-to-analog converter
DIP—dual in-line package
DMA—direct memory access
DSP—digital signal processor
EEPROM—electrically erasable programmable read-only memory
EPLD—erasable programmable logic device
EPROM—erasable programmable read-only memory
FSR—full-scale range
ICE—in-circuit emulator
JEDEC—Joint Electron Device Engineering Council
LAN—local-area network
LCC—leadless chip carrier
LCD—liquid-crystal display
LCP—liquid-crystal polymer
LED—light-emitting diode
LGA—land grid array
LSB—least significant bit
MMU—memory-management unit
MSB—most significant bit
PC—personal computer
PCT—polycyclohexane terephthalate
PET—polyethylene terephthalate
PLCC—plastic leaded chip carrier
POS—programmable option select
PPS—polyphenylene sulfide
PQFP—plastic quad flatpack
PROM—programmable read-only memory
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RAM—random-access memory
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SDP—streaming-data procedure
SMT—surface-mount technology
SOIC—small-outline integrated circuit
SUBDAC—resistor DAC
THD—total harmonic distortion
UART—universal asynchronous receiver transmitter
VMEbus—32-bit data bus that has a theoretical maximum data-transfer rate of 40 Mbytes/sec
VME64—a proposed addition to the VMEbus standard that will allow 64-bit data transfers

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The pluses of C

You're a C programmer but you've been postponing a foray into the realm of C++. *The World of C++*—a package of two 1-hour VHS videotapes, an instruction manual, a workbook, and program disks—could be a good place to start. The tapes provide 21 lessons that correspond to chapters in the workbook. The programs on the disks let you test the principles learned from the taped lessons and book.

The video lessons move so quickly that it's easy to get left behind. Keep your VCR control handy so you can freeze the program frames and examine the listings. Put the lesson book aside and watch and listen to the taped lessons. You'll probably want to rewind and review each lesson more than once before you tackle the written problems and explore the solutions. The book also provides plenty of hands-on exercises and points you to solutions on the accompanying disks—the package supplies both 3½- and 5¼-in. disks. Don't look for extra tutorial materials in the book—you'll get that from the tapes.

Unless you're a fairly knowledgeable C programmer and are already familiar with C++ concepts, you might want to start by reading some or all of an introductory book on object-oriented programming. Two books of particular note are *Object-Oriented Technology, A Manager's Guide*, by David A Taylor (Servio Corp, Alameda, CA) and *Object-Oriented Design with Applications*, by Grady Brooch (Benjamin/Cummings Publishing, Redwood City, CA). If you're not a C programmer, this package could confuse you. Get some experience using C before you tackle it.

The disks that accompany the package supply compressed files of the exercise programs. An installation program unzips the files for you and puts them on your hard disk. It should be obvious that the programs run with the manufacturer's Borland C++ or Turbo C++ compliers. As in any package such as this, you'll learn most by tinkering and experimenting with the provided programs rather than by just running the sample programs. You can adapt the programs to other C++ compliers, but in doing so you may find you're learning more about subtle complier differences than about object-oriented programming. In sum, the package is worth the price, and you'll find it available at a discount from many mail-order software companies.
—Jon Titus

The World of C++, Borland, Scotts Valley, CA 95066, 1991, $199.95.

Adventures in analog

If you do *any* analog circuit design, buy this book! But don't expect a reference work that's going to answer the kind of nagging questions that arise again and again on your job. This book may indeed provide enough answers to warrant your classifying it as a reference, but that really isn't its main function. And don't shell out the cash for this book because you're looking for a definitive treatment of a narrow and arcane subject. You will certainly find several chapters that are thorough treatments of highly specialized topics, but such treatments aren't the book's main function either.

In fact, this volume defies characterization. It combines insights into little-understood technical areas with a look into the thought processes of some genuinely talented (even great) engineers. Then it spices this material with narratives of technical adventures that are every bit as entertaining and suspenseful as many mystery novels. I can't think of the last time I read an electrical-engineering book wondering how it was going to turn out! This book is what literary folk call a page turner.

Jim Williams has brought together 22 well-known analog designers; 23, if you count George Philbrick. (Philbrick died years ago, but because many regard him as the father of analog electronics; a bit of his work is included.) Each of these authors has his own interests and style. Each has his own agenda and biases. Each contributed one or more chapters. There were very few rules or constraints. Williams observes that the concept for the book was a formula for chaos. It's a tribute to the authors and editors that what emerged is not chaotic at all.

The well-indexed volume contains much useful information and provides a picture of analog design, in all its diversity, as a way of thinking and a way of approaching problems. What sets the book apart is that it brings to life the individualism and eclecticism of analog designers. Moreover, it demonstrates that, beyond their common practice of the analog art, what brings these designers together is their inquisitiveness, their open-mindedness, and their willingness—in fact, their *eagerness*—to look at problems in unconventional ways.

Those with no real appreciation for analog design often deride its practitioners as engaging in a black art. Yet everything that goes on in analog circuits (as in *all* circuits) has a foundation in science. Those who seek to understand the lessons their circuits are trying to teach them are the ones who possess the stuff of which great designers are made. In a larger sense, engineers who pursue disciplines far removed from analog design—even disciplines far removed from electronics—are likely to find valuable lessons in Williams's book. So, even if you never do analog design, if you are an engineer, buy this book!
—**Dan Strassberg**

Analog Circuit Design: Art, Science, and Personalities; Jim Williams, editor; ISBN 0-7506-9166-2; 389 pgs; $44.95; Butterworth-Heinemann Publishing; Boston, MA, 1991.

Advantages outweigh flaws in C pointer book

You might think that a topic that appears to be narrow wouldn't deserve a book of its own. However, don't be deceived by the title of the book *Mastering C Pointers*—it's a bigger subject than you might think. Because pointers play such an important part in complex programs, it's gratifying to find a book devoted to the subject.

Author Robert J Traister assumes that you know a bit of C, and he builds on that basic knowledge as he clearly explains new concepts that you may have heard about but may not understand clearly. The examples are simple and straightforward, clear and concise. The short examples are easy to type into your computer and test. Unlike other authors of books on C, Traister avoids the temptation to show off his programming skills, an approach that usually discourages readers.

Traister spends a great deal of time on character and string pointers, not because string operations are so important on their own, but because character or byte operations are an integral part of most real-world applications. In addition, you'll find chapters on memory access, memory allocation, pointers and functions, and pointers to other objects.

Although I recommend this book highly, it does have a few flaws. The author's use of little men with knapsacks to explain how pointers locate information seems silly in a professional-level book. I would have rather seen clear diagrams that show how information is stored and how pointers locate it from within programs. There isn't a diagram in the book. By comparison, several of my favorite C programming books are replete with diagrams that show bit maps, structures, unions, and other C arrangements of information.

Traister ends the programming portion of his book with a chapter on pointers to other structures, but he doesn't go far enough. One of my reasons for reading the book was to prepare for learning more about data structures such as linked lists and trees, and about sorting algorithms. Handling an introduction to these topics as clearly as he introduced basic pointer principles would have made the book invaluable. All in all, I recommend the book, particularly to C programmers who are just getting the hang of the language.
—**Jon Titus**

Mastering C Pointers, Robert J Traister, Academic Press, San Diego, CA, 1990, 182 pgs, $34.95.

Designer music

Very little techie humor is recorded commercially. That's why I snatched up *The Funniest Computer Songs* at the Computer Literacy Bookshop in San Jose, CA ((408) 435-1118). This audio cassette contains some of the most hilarious songs about electronic technology I've ever heard.

Even the song titles elicit a chuckle. Try to keep a straight face while thinking about songs with titles such as "Please, Mr Compatibility," "I'm A Mainframe, Baby," or "Uncle Ernie's Used Computers' Babbage's Birthday Bargain Bash."

Here are a few lyrics from the "Engineer's Rap" sung by the group Run GMC:

We all calculate,
and do design,
test that box,
and deliver it on time.

Back from lunch,
I need a rest,
but we're just in time,
for acceptance test.

Tweak the knob,
Turn the dial,
Hit return,
And wait for awhile ...

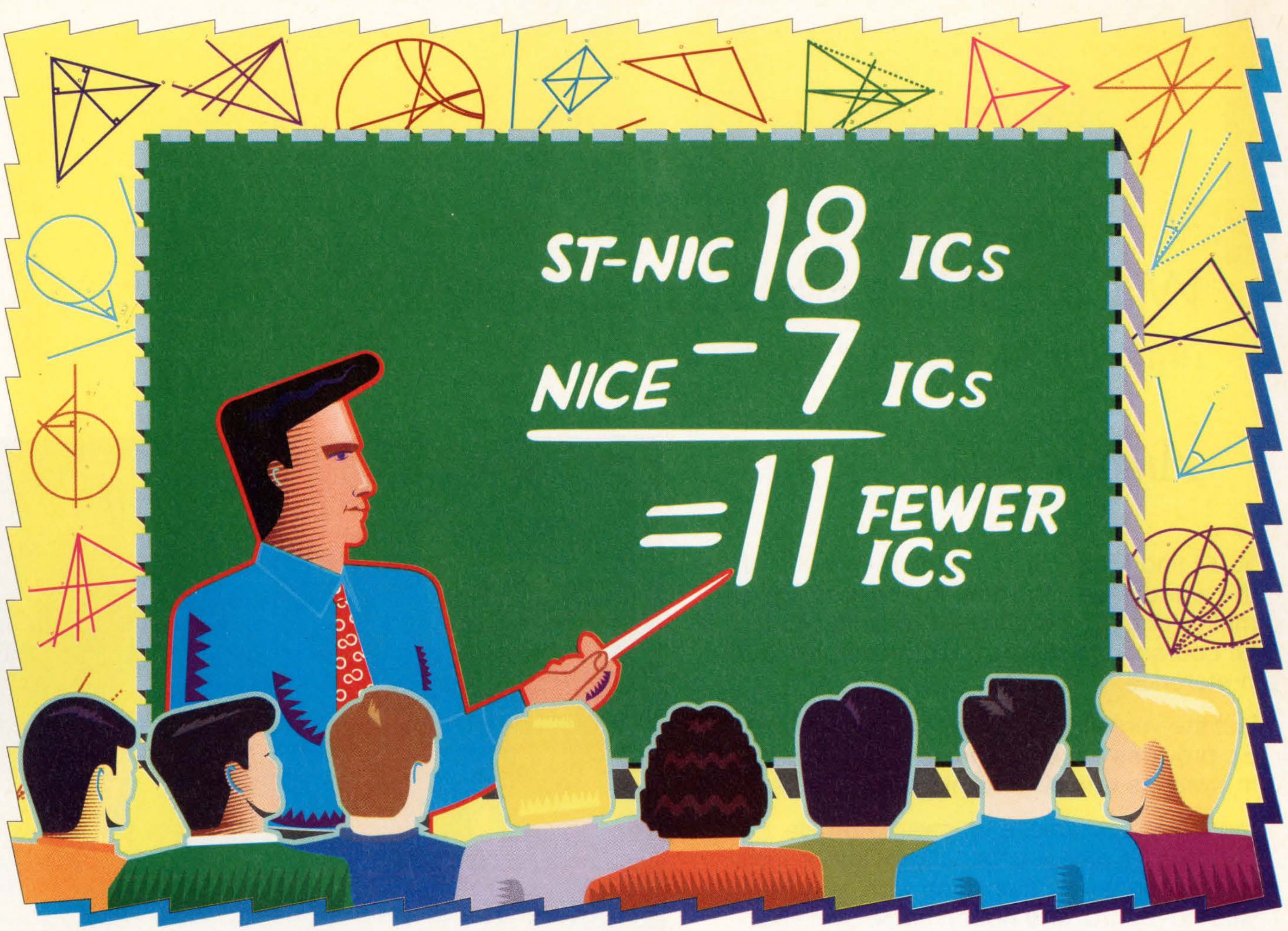
And wait for awhile ...
(hey, what's going on here)
And wait for awhile ...

It's, it's, it's usually much faster
than this.

Sometimes you need a big dose of humor to help you make it through the day. Keep this tape handy for the next time you smoke a chip or download the wrong code revision.—**Steven H Leibson**

The Funniest Computer Songs, $8.98 (plus $1 postage), Vince Emery Productions, Box 460279, San Francisco, CA 94146.

EDN



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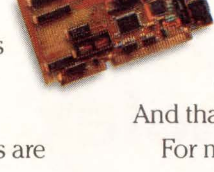
It doesn't take a mathematical wizard to see the superiority of the NICE® Ethernet solution from the Advanced Products Division of Fujitsu Microelectronics. We think the numbers speak for themselves.

Our NICE solution, for example, requires far fewer ICs than ST-NIC's™ so-called single-chip solution—7 vs. 18.* And that means fewer passive components as well. Making Ethernet LAN board design easier. Faster. And more cost effective than ever before.



Then, add on another factor—that NICE products are competitively priced—and systems designers clearly have a proven formula.

What's more, the fewer the parts, the smaller the size—and the lower the power consumption. All of paramount importance for motherboard applications.

Plus, because NICE is a highly automated controller, it offers substantially greater system performance for user applications—by freeing CPU and memory bandwidth. Fact is, benchmarks and customers report up to 33% higher performance over competitors' controllers. Quite an edifying statistic, don't you think?

And, unlike other available solutions, NICE has been designed to *fully* comply with Ethernet standards—ensuring international interoperability. And that's no myth.

For more enlightening facts, here's one more NICE number: **1-800-866-8608.** Or call your local sales office for our NICE Designer Kits. And discover the world's most advanced, highly-integrated, cost-effective Ethernet solution—the NICE family of high-performance products from Fujitsu. Because all it takes to expose a little myth is a little math.

FUJITSU

Delivering the Creative Advantage.

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CIRCLE NO. 91

With our SL™ connector system, design flexibility and cost savings are yours.

Automatically.

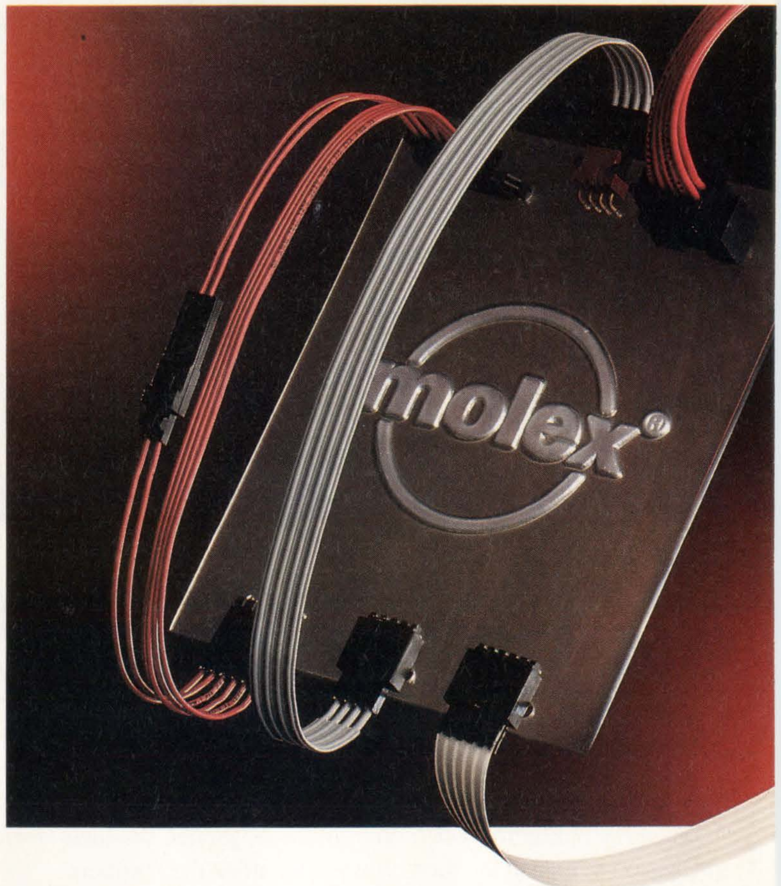
You'll find Molex SL connectors in some of the world's leading—and most dependable—makes of electrical and electronic equipment. Of course, reliability is a big reason for this preference.

But the versatility and lower applied cost that SL provides are critical factors, too, especially in systems with several interconnections.

Modular, stackable, and lower in profile, SL connectors give you virtually unlimited flexibility when you're designing wire-to-wire, wire-to-board, and ribbon cable systems.

The single-piece IDT connectors feature, pre-assembled terminals in the housings, and interconnects with locking shrouded headers. In short, they're ideal for high-speed, high-efficiency automated assembly.

Ask your Molex representative about SL connectors, and learn how they can multiply design options and automate assembly.



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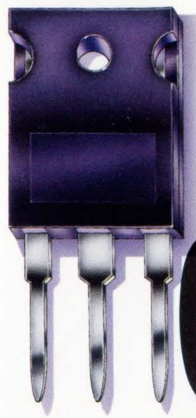
CIRCLE NO. 92



oney.

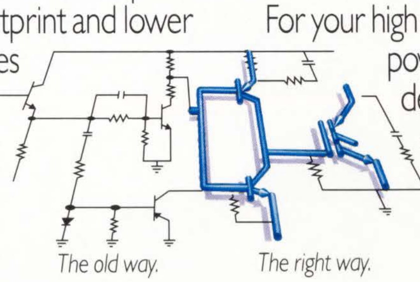
Why is everyone switching from bipolar to IR IGBTs?

Ask three design engineers why they're switching to IR IGBTs and you may get three different answers: <u>Performance.</u> IR IGBTs switch faster, generate less heat, and operate at higher frequencies than bipolars.

<u>Simplicity.</u> Our IGBT's MOS gate makes it much simpler to drive than a bipolar.

<u>Size.</u> Its smaller footprint and lower component count saves a lot of board space.

But all three answers add up to one: <u>Cost effectiveness.</u> Any way you look at it, the price/performance ratio improves. Or, the bottom line is the bottom line.



The old way. *The right way.*

For your high voltage, high current power transistor circuit designs, remember, cost efficiency has four initials: IGBT. Make that six. IR IGBT.

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