EDN®

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

A CAHNERS PUBLICATION
April 9, 1992

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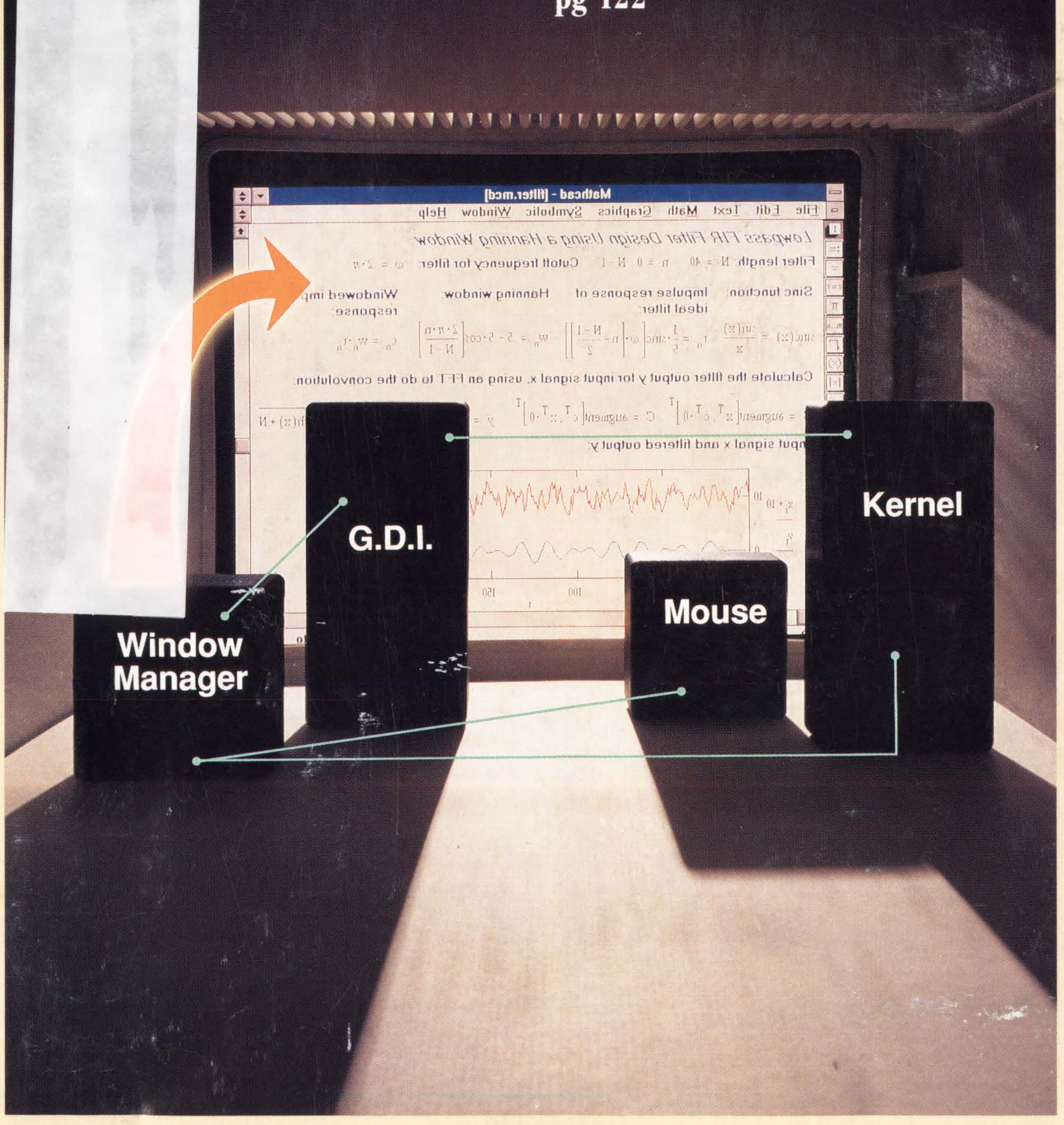

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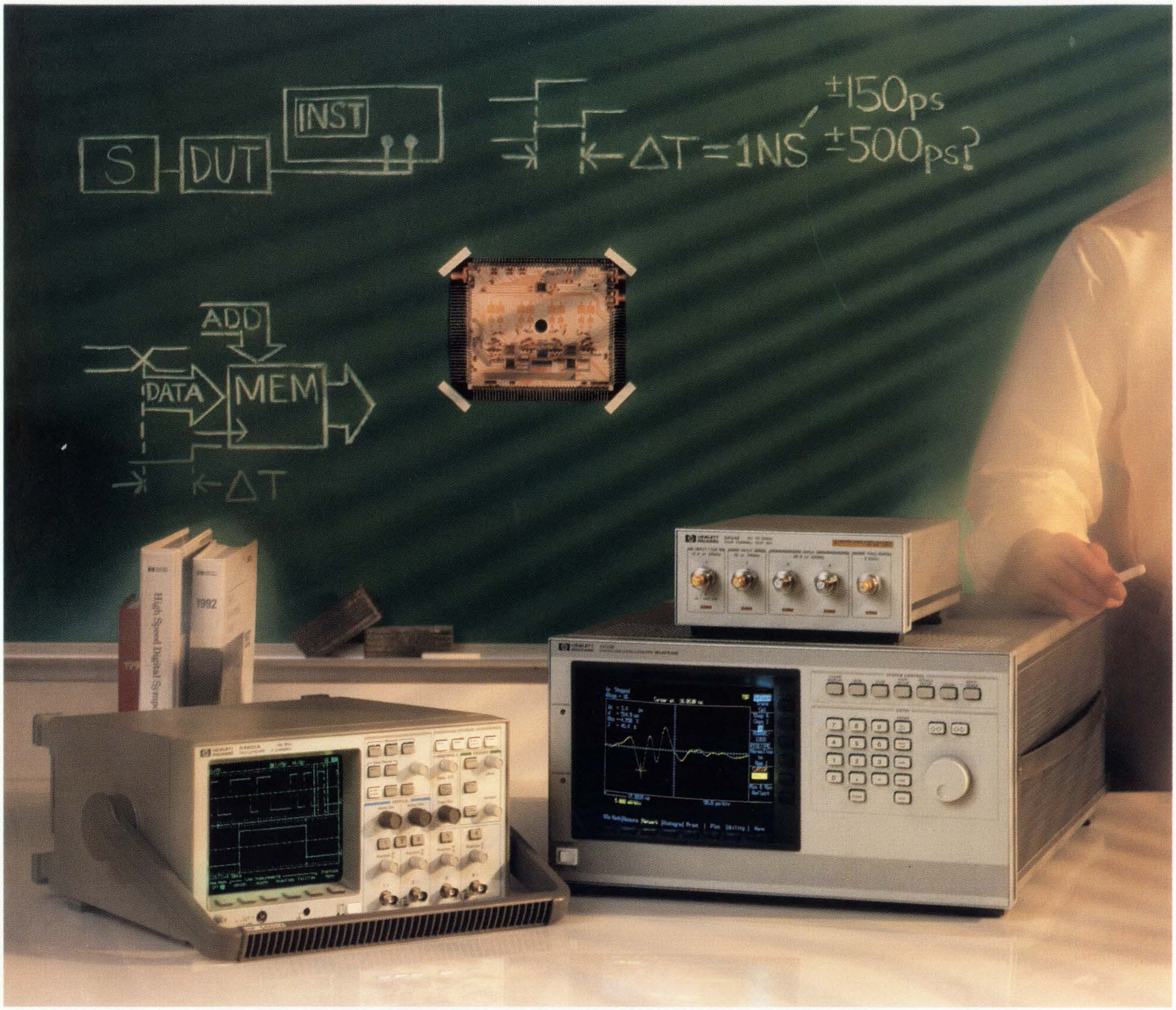
HP scopes make digital designs easier to understand.



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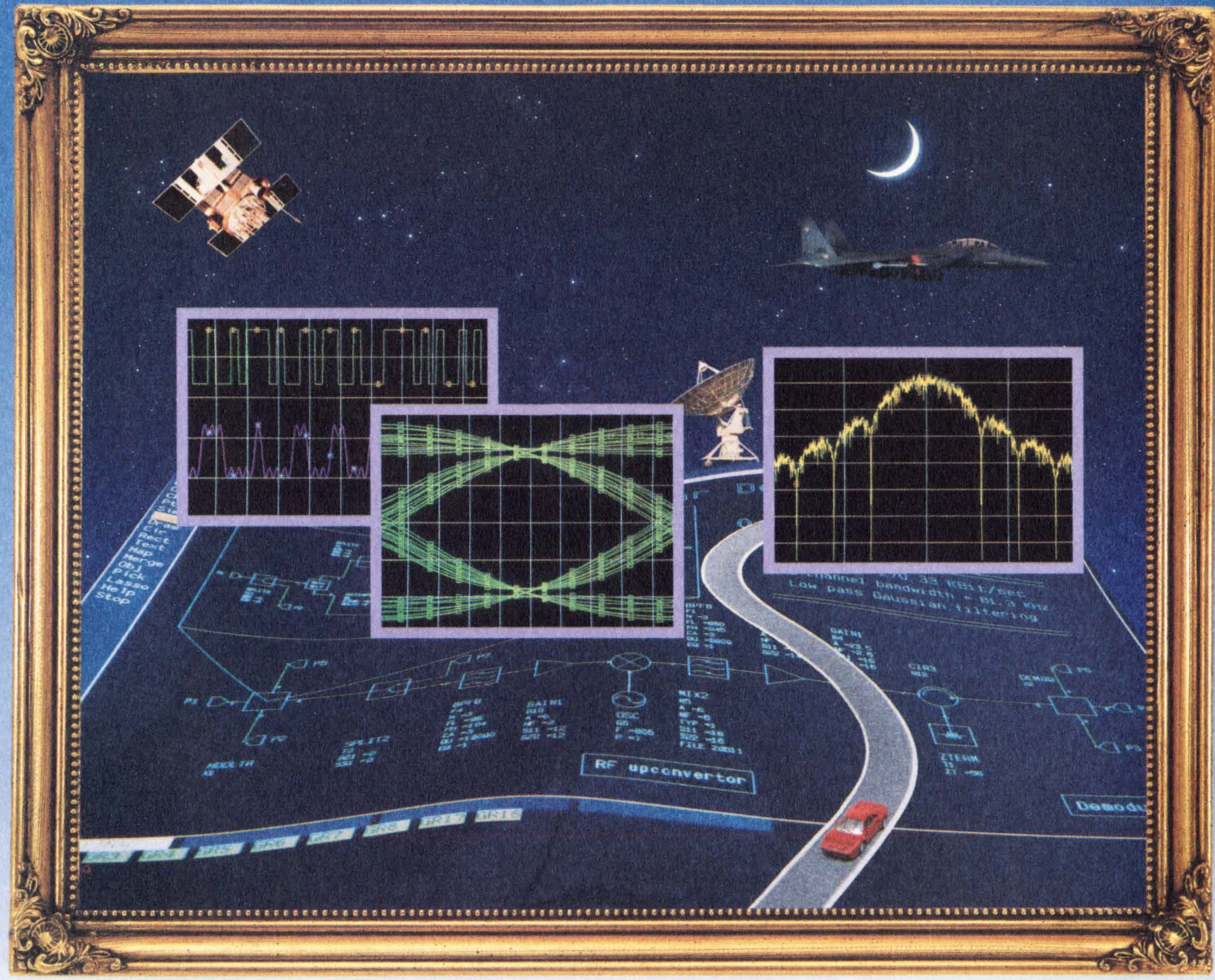

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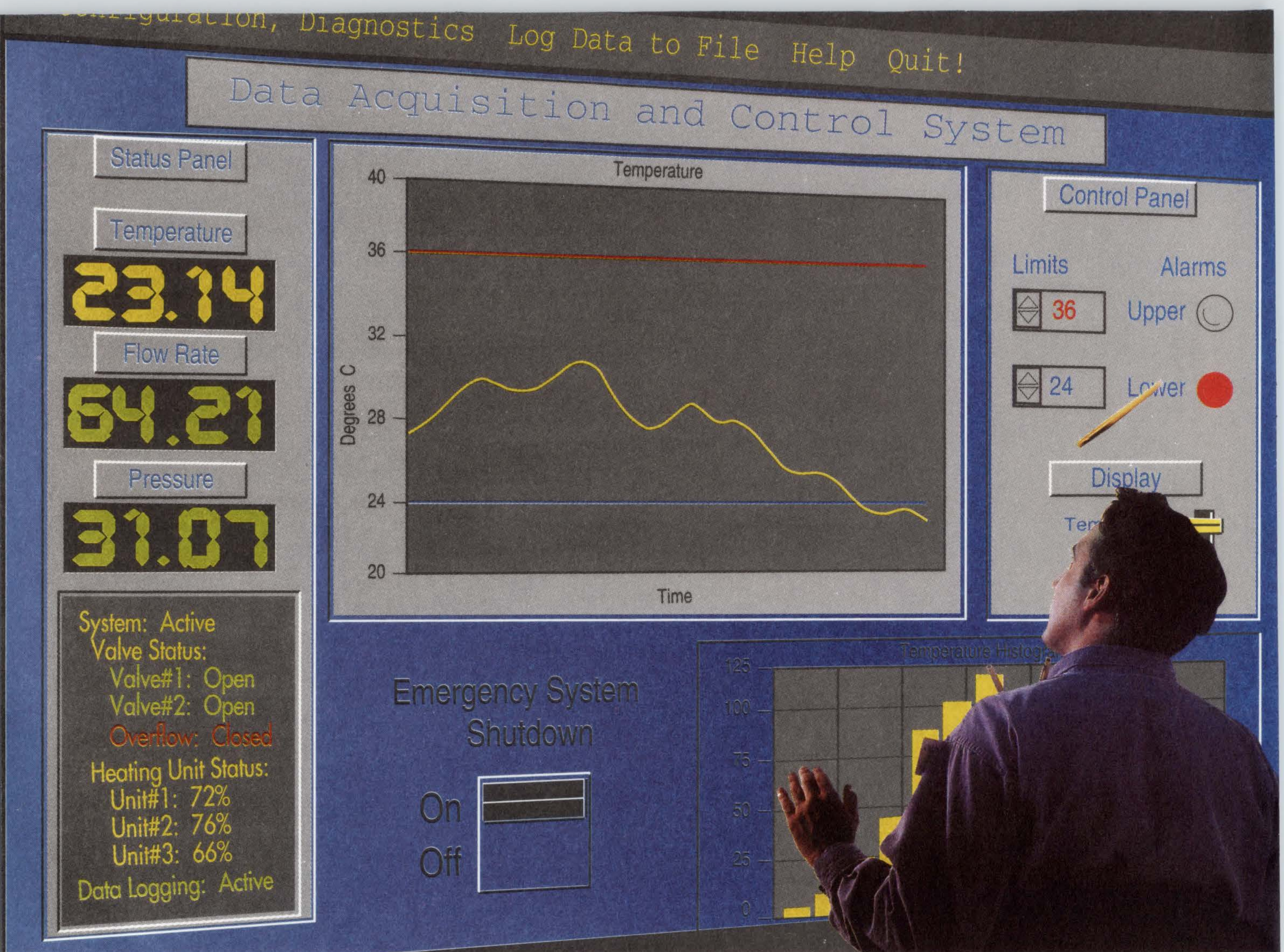

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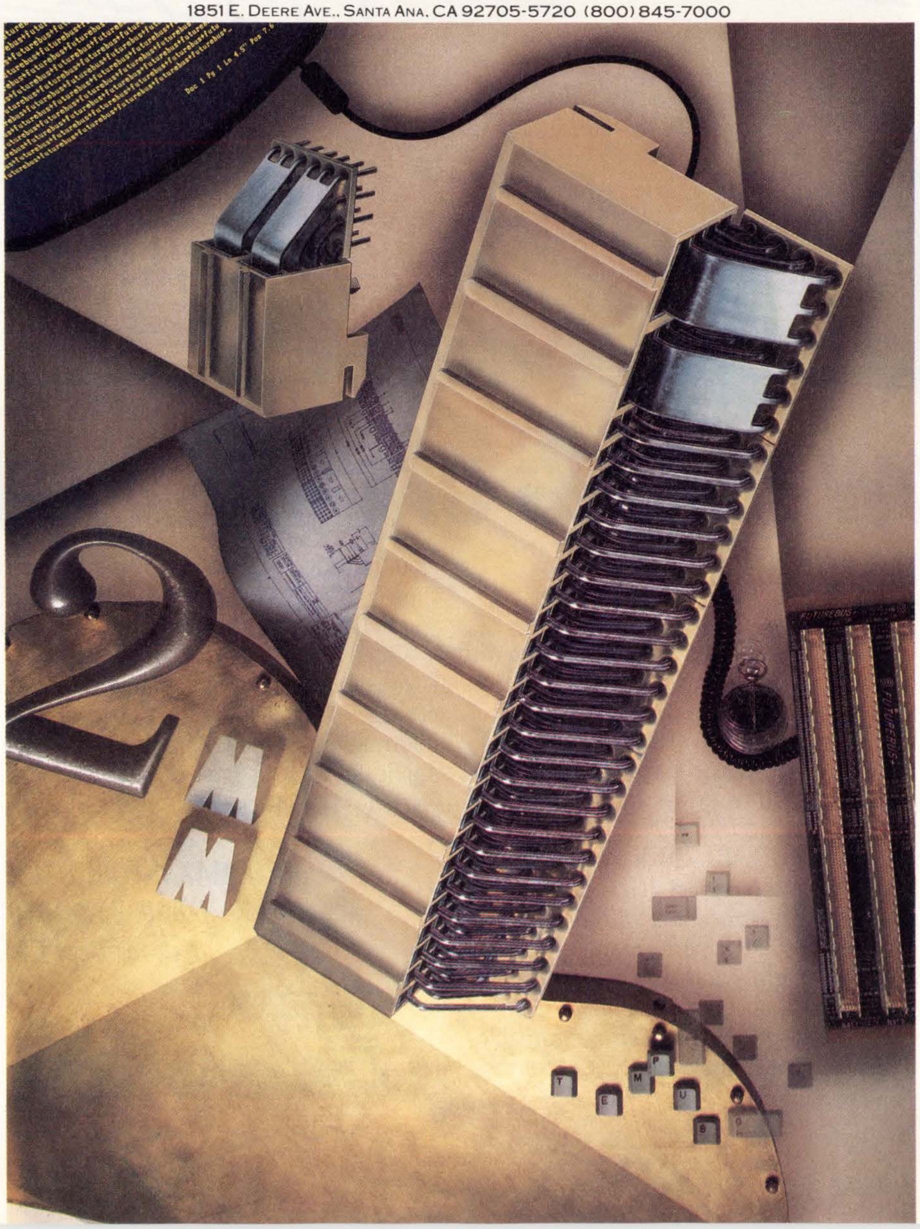

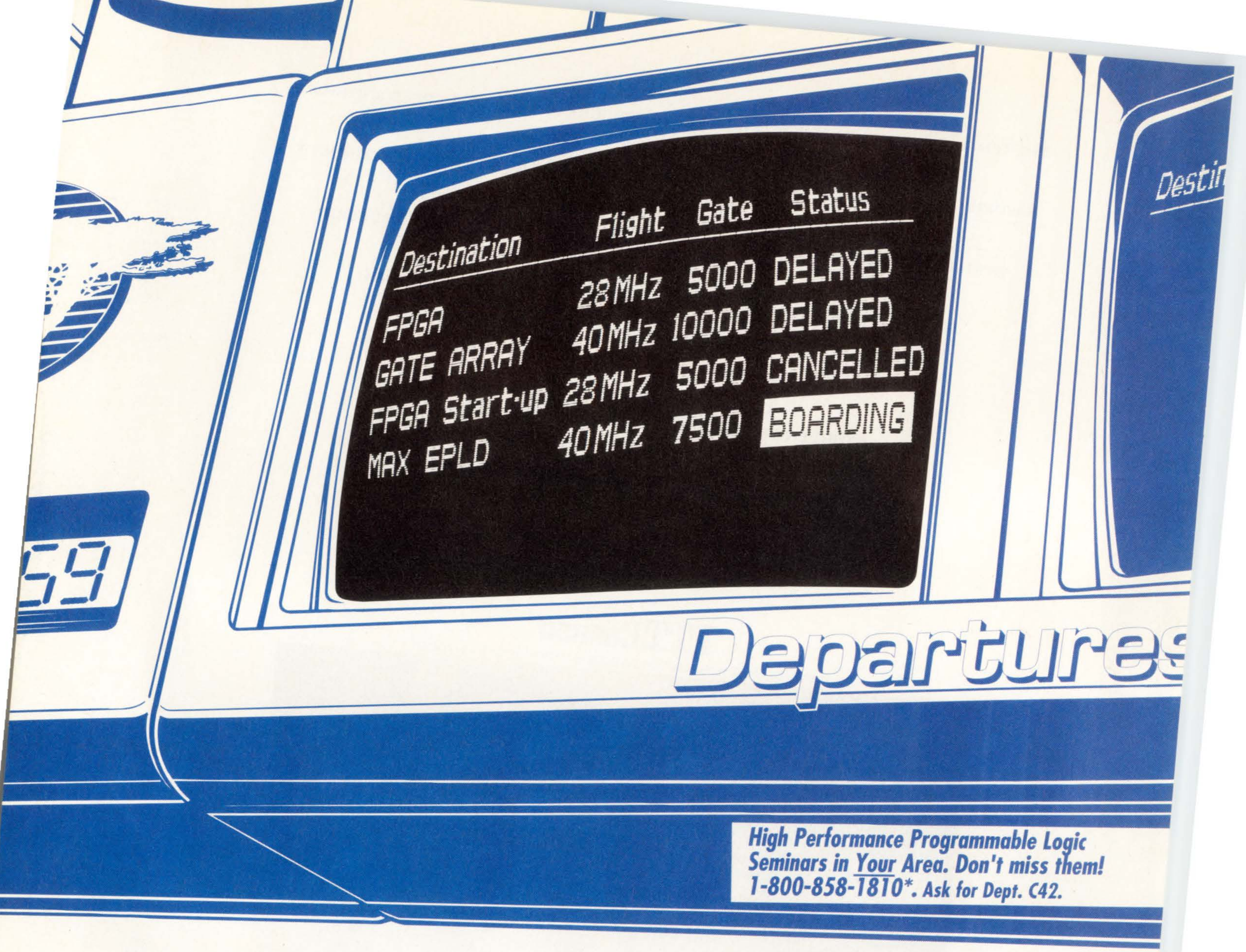

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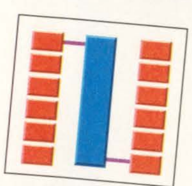

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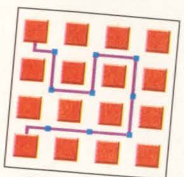

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EDN

MAGAZINE EDITION

APRIL 9, 1992 VOLUME 37, NUMBER 8

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

On the cover: When you talk about Windows, what often comes to mind is its user interface. A look at Windows' internal mechanisms, however, reveals an equally important perspective from which to weigh its pros and cons for use with engineering software. (Photo courtesy Mathsoft; design by Liz Schweber; photography by Peter Jones, Advanced Photographics, Custom Laboratory Services) . . . . **PAGE 122**

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Express Request

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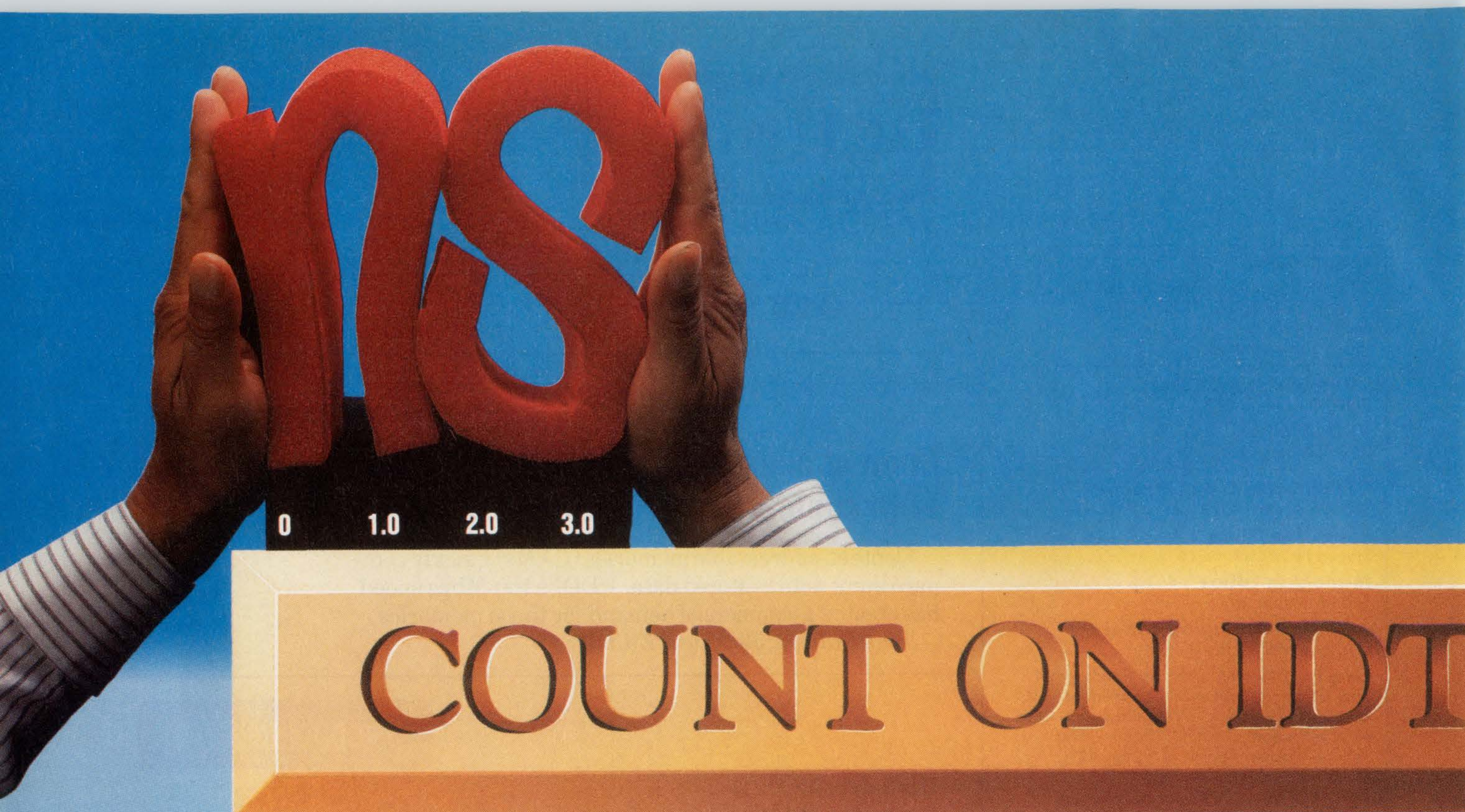

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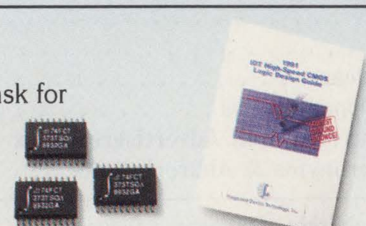

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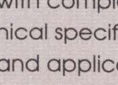

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A summary and analysis of articles in this issue

The editors of EDN Magazine edition did a lot of poking, prodding, and tire kicking to bring you the stories in this issue. For starters, you'll find the first installment of Technical Editor Doug Conner's 2-part, hands-on FPGA series. As with most of EDN's hands-on series, this article blossomed from Conner's curiosity about some aspect of design; in this case, FPGA design. Rather than just telling you

about the available design tools or interviewing some existing users, Conner wanted to let you know—first hand—just how easy or difficult it is for an experienced design engineer to learn how to use FPGA development tools.

He started just where you would, by defining a product that he wanted to design. Then he designed and built it using an FPGA as a key component. Along the way he took a class that taught him how to design with FPGAs, he learned how a simulator can prevent you from venturing down blind alleys, and he faced that moment of truth when the power is first turned on. All told, he had a lot of fun.

In this issue's Special Report, Senior Technical Editor Charles Small looks under the hood of Microsoft Windows to gauge its suitability for engineering applications. Small also interviewed several software vendors and found them divided on their intentions regarding Windows. Some are converting their applications programs, others aren't. As part of his investigation, Small became one of the 12,000 beta sites for Windows version 3.1.

Technical Editor Anne Watson Swager also tried out some software for her Technical Update on filter-design packages. She discovered that most of these packages create designs for either switched-capacitor or continuous-time filters but not both types. Consequently, these software products are most helpful when you already know the type of filter you want to use. They'll save you time by automating the filter equations so you can leave the filter textbooks on your bookshelf. However, if you need help in deciding between filter types, or if you're trying to create an unusual filter, you might not be satisfied with most filter-design packages.

Finally, Technical Editor John A Gallant discovered a recent innovation while researching his Technical Update on content-addressable memories (CAMs). A lone inventor in Boulder, CO, has developed a method that makes CAMs out of conventional RAMs through a decidedly unconventional architecture. See the sidebar in Gallant's Technical Update for more details.

Steven H Leibson
Executive Editor

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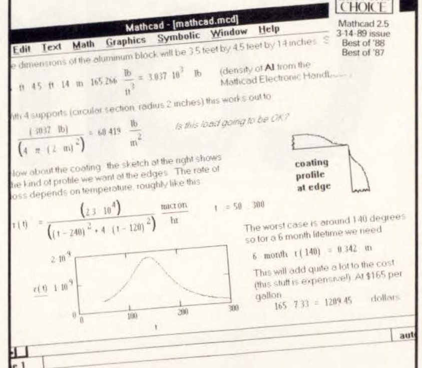

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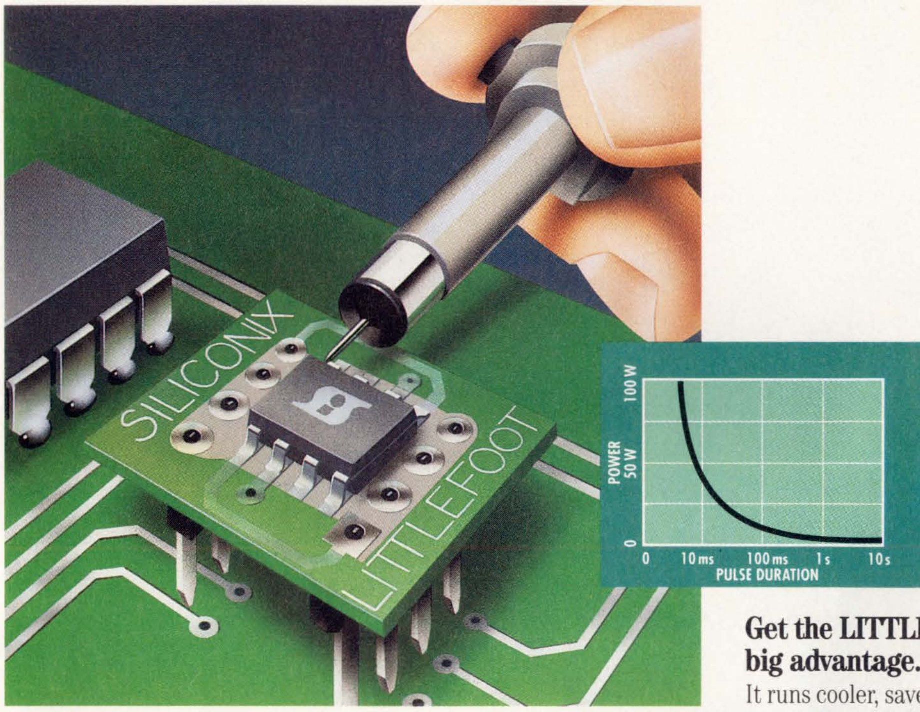

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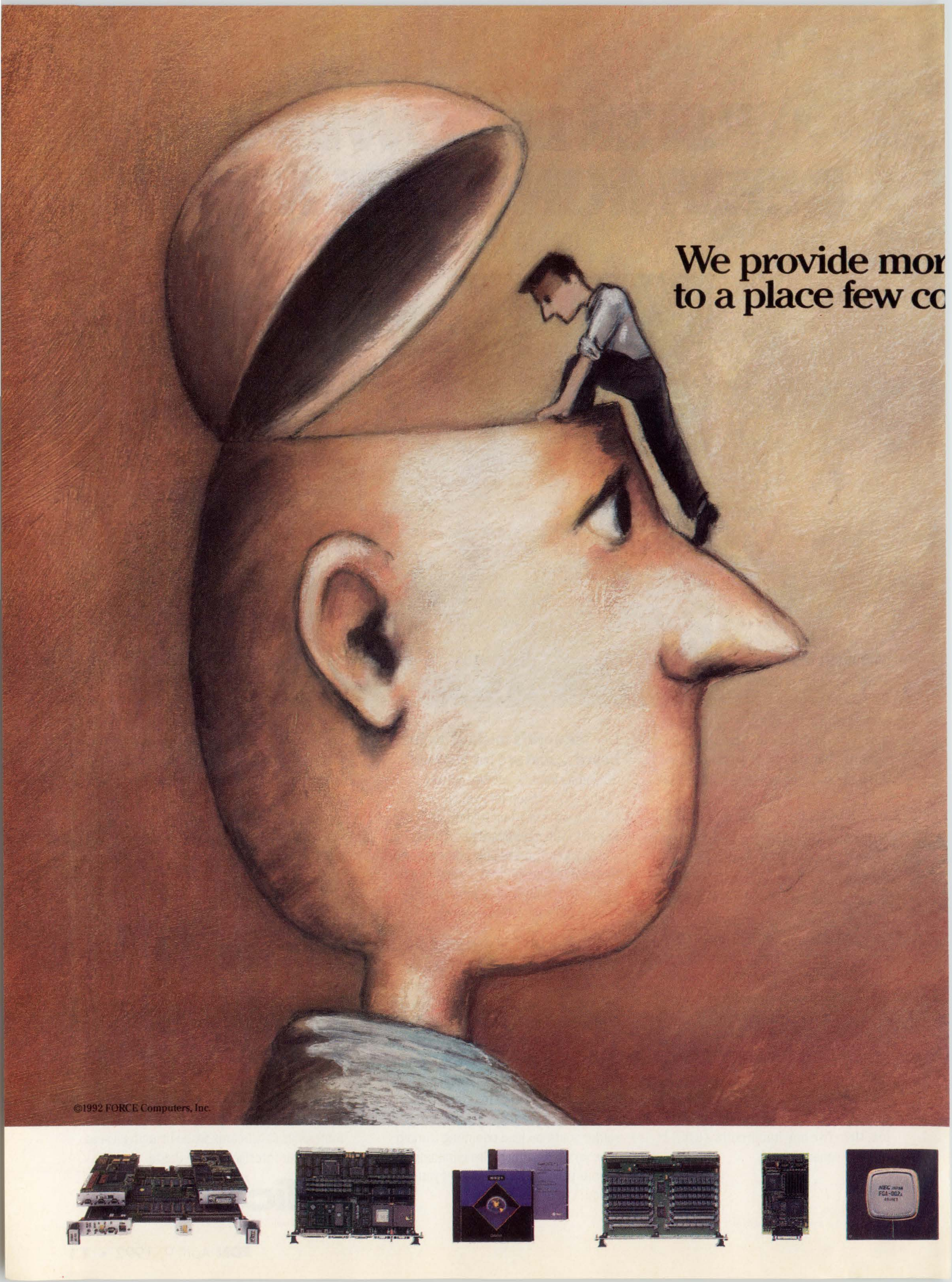
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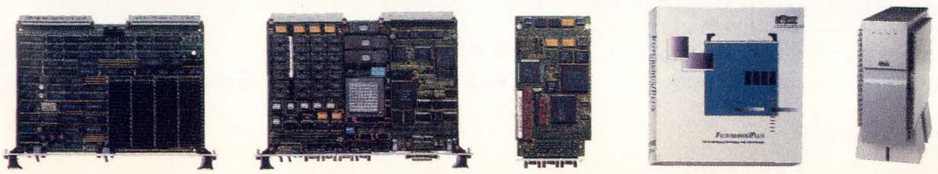

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CIRCLE NO. 8

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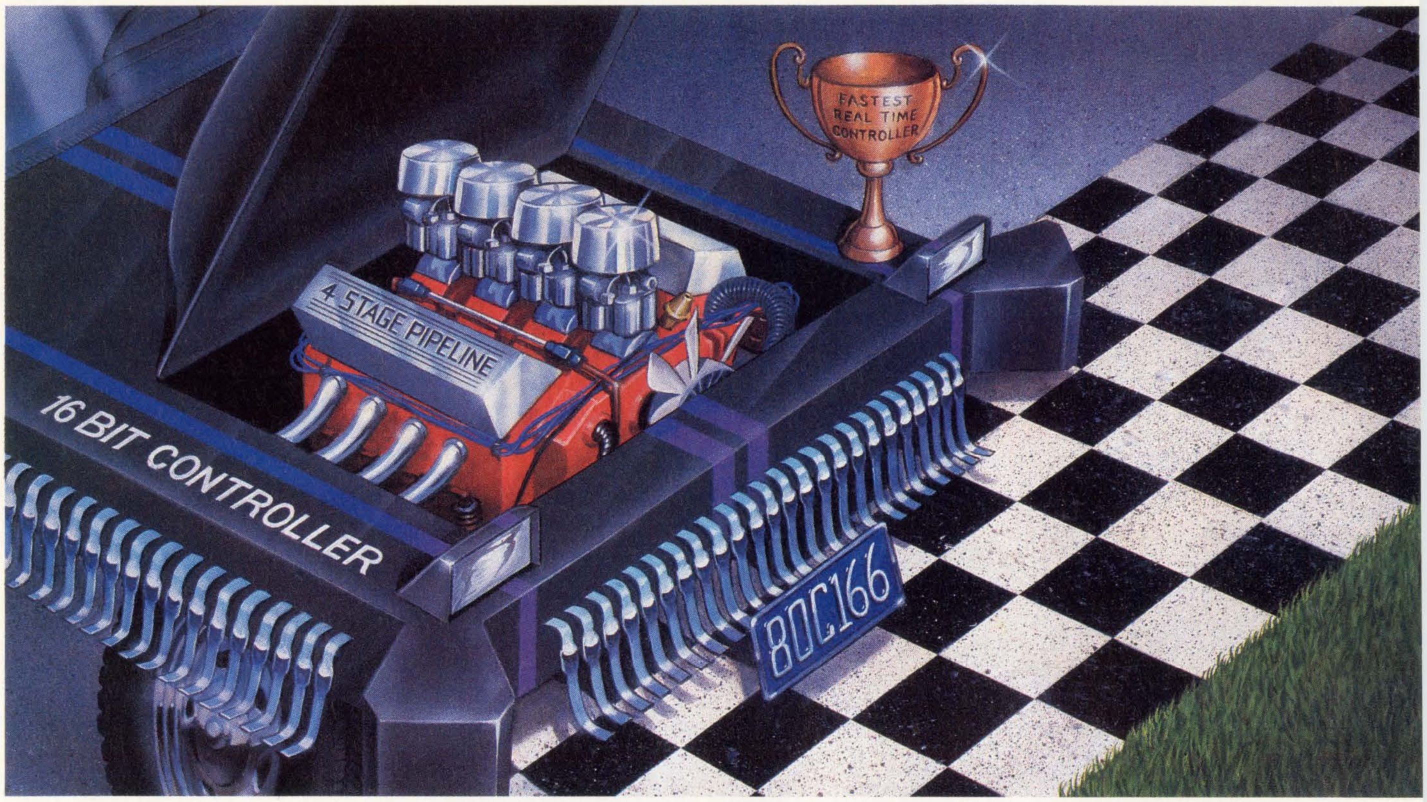

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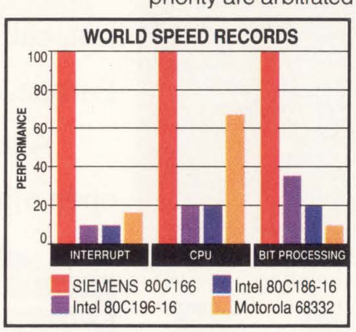

The 80C166 also gives you the most effective interrupt performance anywhere, with speeds as fast as 250 ns because the 64 levels of priority are arbitrated each machine cycle. The fully vectored interrupt system allows the fastest identification of interrupt sources. Plus, through the use of a Peripheral Event Controller, which 'steals' just one machine cycle from the CPU, it lets you service peripherals without going through a standard interrupt procedure.

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With the Siemens SAB80C517A, we've also brought this high-performance to the 8-bit microcontroller. It offers 10-bit A/D conversion, 32K ROM, 2.2K onboard RAM, and 32- and 16-bit arithmetic functions, while still retaining 8051 software compatibility. And it has 8 data pointers and 68 ports—more than any competitor.

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CIRCLE NO. 9

EDITED BY SUSAN ROSE

Multiple sources for ISA bus—in two senses

Programmable dc sources are common building blocks in automatic test equipment (ATE). They differ from D/A converters by providing higher output currents (and sometimes, higher output voltages) and by offering outputs isolated from the system chassis. Some also operate in four quadrants; they source or sink positive or negative voltage or current, and they can absorb current from a positive-voltage load, and they can supply current to a negative-voltage load. Until about a year ago, when the first ISA bus plug-in programmable dc source appeared, if you were building PC-based ATE, your dc sources had to be external units, controlled via IEEE-488 or RS-232C.

Now Datel is offering a programmable dc source, the PC 462. It has four outputs totaling 22W, offers 200-μsec transient response, and is unconditionally stable under all load conditions. Although lacking 4-quadrant capability, the $1195 unit, which plugs into the 16-bit, PC/AT version of the ISA bus, provides dedicated positive and negative outputs; one pair is rated at ±20.475V at 250 mA each, the other at ±6.1425V at 1A each.

The board also includes an isolated 16-channel ADC that you can use to monitor the output voltages and load currents, two digital inputs, and two high-power digital outputs rated at 300V and 100 mA. The board's analog inputs and outputs have 12-bit resolution. A $95 program provides a virtual-instrument interface under MS Windows V3.0. Datel Inc, Mansfield, MA, (508) 339-3000, FAX (508) 339-6356.—Dan Strassberg

DIP-size devices take the pain out of antialiasing

Until now, if you wanted a filter you could just drop onto a pc board and pretty much forget, you had to choose between very expensive programmable hybrid circuits or rather large modules built from discrete devices. Now, a family of small, moderately priced lowpass filters requires no external components, exhibits low noise, and requires little specialized knowledge to apply. The D70 series includes 4-, 6-, and 8-pole models with Butterworth and Bessel characteristics and fixed user-specified, cut-off frequencies from 500 Hz to 50 kHz (2% tolerance). The filters are housed in 0.625×0.3-in. dual-in-line packages that measure 0.5-in. long in the 4-pole version (0.825-in. long in the 6- and 8-pole versions). The 8-pole devices are priced at $49 (1). A 4-pole device costs $19 (10,000). Even though the filters are made to order, delivery is four to six weeks ARO. Frequency Devices Inc, Haverhill, MA, (508) 374-0761.—Dan Strassberg

Intel gives away PLD/EPLD software

Intel is offering free copies of its PLDshell Plus software. The software includes a device compiler, a logic minimizer, a simulator, and a decompiler. The decompiler accepts JEDEC fuse maps. The compiler targets the company's 20- and 24-pin PLDs and EPLDs that are second-sourced from Altera. The compiler also swallows PALASM files. To receive the free software, call the Intel Literature Center at (800) 548-4725, or call your local Intel office and ask for Intel Packet #IB75.

—Charles H Small

FPGA combines 100-MHz clock rate with 2000-gate density

Quicklogic's QLI2x16 FPGA (field programmable gate array) is designed for high-speed counter operation: The logic supports 100-MHz (min) clock rates for 16-bit binary counters and as much as 150 MHz for Johnson counters with simple front-end control logic (the raw toggle rate is 180 MHz). The chip is the second in the pASIC FPGA family. Refinement of the basic circuit design and the addition of dedicated clock inputs and drivers with through-chip skip held to 1 nsec has improved performance by 15%.

The chip is built around a 10×12 matrix of interconnected logic cells. Each cell consists of six AND functions, three multiplexers, and a D flip-flop, all of which are the equivalent of 20 or more virtual gates. This organization gives the FPGA an equivalent gate count of 2000 (min) logic gates. Unlike other FPGAs, this logic core is designed for logic control functions. It has 14 inputs folding into six ANDs with multiplex control and a dedicated D flip-flop. In addition, two gate outputs and two multiplex outputs directly exit the cell, supplementing the flip-flop output.

The chip comes in an 84-pin plastic leaded chip carrier with 68 bidirectional inputs and eight dedicated inputs. $98 (100). Quicklogic Corp, Santa Clara, CA, (408) 987-2000.

—Ray Weiss

Ethernet connects data-acquisition system to Sun workstations

When you connect an externally mounted data-acquisition subsystem to a workstation, the two most common interfaces are IEEE-488 and RS-232C. However, workstations have Ethernet interfaces; using one of the other types of interfaces usually requires adding hardware. Moreover, Ethernet has the potential of 10-Mbps transmission (albeit with nondeterministic response). RS-232C is orders of magnitude slower; IEEE-488, which has comparable speed, has cable-length limitations that are restrictive in many data-acquisition applications—

Logic families operate fast on low-voltage supplies

Two logic CMOS IC families from Philips Semiconductor operate with V_{CC} in the 1.2 to 3.6V range. The first family, known as HLL (High-speed, Low-power, Low-voltage), exhibits a typical propagation gate delay of 2.5 nsec on a 3.3V supply. It uses 0.25 mW in an idle condition and 0.9 mW when switching at 1 MHz. The HLL family withstands 5.5V inputs, and you can interface inputs and outputs directly to TTL logic levels in mixed 3 and 5V logic systems. The second family, LV-HCMOS, features similar speed performance to Philips' established 5V HCMOS range of logic products. The new family is also pin- and function-compatible with HCMOS products, letting you replicate 5V logic designs on 3.3V supplies, resulting in approximately a 70% power savings.

The first products to appear in each range are 3-state octal inverting line drivers. At 25°C and with 3 V_{CC}, the 74HL33240 exhibits a maximum propagation delay of 3 nsec and a 3-state enable time of 3.6 nsec. Equivalent figures for the 74LV244 under the same conditions are 17 and 20 nsec, respectively. The 74HL33240, in a 24-pin plastic small-outline package, costs $1.50 (100); the 74LV244, in a 20-pin plastic small-outline package, costs $0.42 (100). The company forecasts 20 parts and shrink small-outline packages for each family by the fourth quarter of 1992. Philips Semiconductor, Eindhoven, The Netherlands, 40-722091, FAX 40-724825. In the US, Signetics Corp, Sunnyvale, CA, (800) 227-1817, FAX (408) 991-3581.—Brian Kerridge

particularly those in factories.

Strawberry Tree's I/O Station 464 is a data-acquisition unit housed in a 4.25×17×16.88-in. enclosure. You can mount the enclosure under a Sun workstation's monitor or at a distance from the workstation. In either case, you connect the unit to the workstation via 10Base-2, 10Base-5, or 10Base-T Ethernet. The unit holds four of the vendor's data-acquisition boards; eight types are available. The initial offering is intended for relatively low-speed applications (0.5 to 2 msec/point). A CPU in the enclosure linearizes the data and scales it in engineering units before placing it on the network. The unit's pricing begins at $3995. Strawberry Tree Inc, Sunnyvale, CA, (408) 736-8800, FAX (408) 736-1041.

—Dan Strassberg

Logic emulator runs at 8 MHz without tweaks

Pie Design Systems' Mars II series modular logic emulators let you emulate a large PLD, FPGA (field programmable gate array), or ASIC without programming a part or incurring a mask charge. Mars stands for modular, automatic, retargetable, and scalable. The modularity arises from the division between the debugging circuitry and the emulation circuitry. Automatic refers to the emulator's ability to partition a logic design automatically and map it onto the emulation hardware. The company claims that its automatic partitioning software can produce emulations that operate at clock speeds to 8 MHz by identifying critical timing paths and treating these paths accordingly. Retargetable and scalable refer to the company's belief that the emulation architecture can immediately benefit from speed and density improvements made to the underlying FPGA technology used for the emulation circuitry.

The system's debugging module includes a 576-channel logic analyzer, a functional tester, and an emulation server that links the emulation modules to a host computer. The emulation module, called a logic-block module, contains the dynamically configured FPGAs that actually perform the logic emulation. Any number of emulation modules can share one debugging module.

Software for the system includes on object-oriented database manager that controls all of the emulation system's data files, a compiler that transforms EDIF-logic netlists into emulation files, functional test software that ensures that the emulation configuration matches the original logic design, and the logic-analyzer control software. A system that can emulate 50,000-gate designs costs from $208,000 to $227,000. Additional emulation modules cost $54,000 and provide 25,000-gate emulation per module. Pie Design Systems Inc, Sunnyvale, CA, (408) 738-8899, FAX (408) 738-8853.

—Steven H Leibson

Choose interface and form factor for your drives

You can choose an IDE (Integrated Drive Electronics) or a PCMCIA (Personal Computer Memory Card Industry Association) interface with disk drives from Ministor's 1.8-in. Miniport family. Most small disk drives include an IDE interface, but the Miniport models are among the first to also include compatibility with the PCMCIA standard, originally developed as a memory expansion bus for notebook computers. The series includes drives with 32- and 64-Mbyte capacities priced at $280 and $380, respectively (OEM qty). The drives feature 18-msec average seek times, an average latency of 6.67 msec, and a 256-kbyte buffer. A 5V supply powers the drives that consume 2.5W of power during read/write operations. The units feature a 2-level sleep mode that lowers power consumption to 0.1 or 0.005W. The drives can operate through a 20g shock and can withstand 200g of shock when not operating. Minístor Peripherals Corp, San Jose, CA, (408) 937-0165.—Maury Wright

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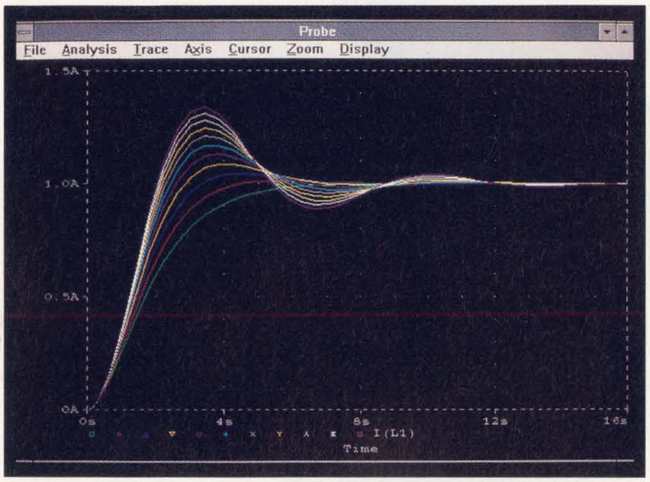
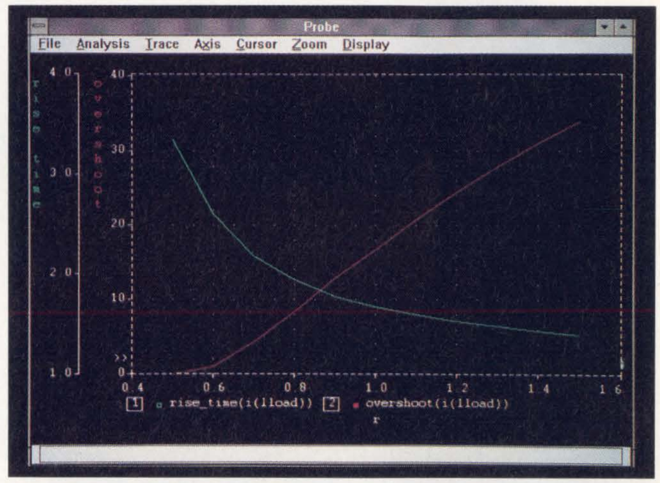
Using the Design Center's Performance Analysis Feature



Current through an inductor with stepped resistance



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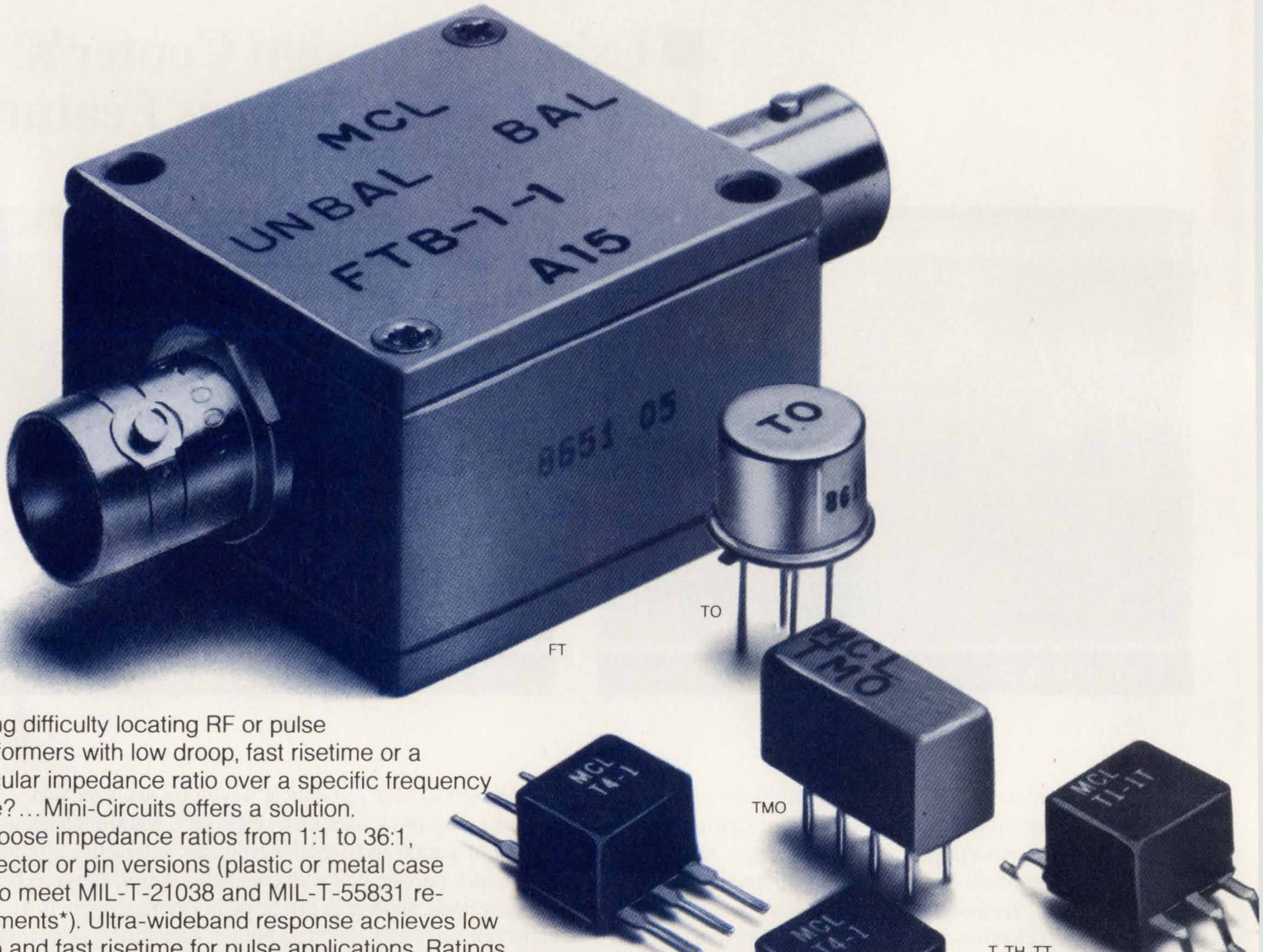

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T1-1	5950-10-128-3745	TMO2.5-6T	5950-01-215-8697
T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
T16-1	5950-01-094-7439	TMO9-1	5950-01-141-0174
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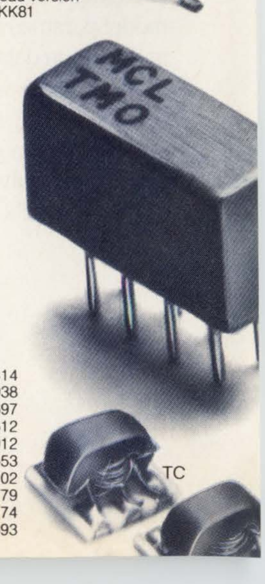

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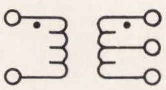
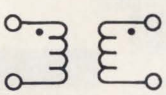
A* PRI  SEC	T	T1-1T	1	.05-200	.05-200	.08-150	.2-80	4.45
		T1-6T	1	.003-300	.003-300	.01-150	.02-50	6.95
		T2-1T	2	.07-200	.07-200	.1-100	.5-50	4.95
		T2.5-6T	2.5	.01-100	.01-100	.02-50	.50-20	4.95
		T3-1T	3	.05-250	.05-200	.1-200	.5-70	4.95
		T4-1	4	.2-350	.2-350	.35-300	2-100	3.25
		T4-6T	4	.02-250	.02-250	.05-150	0.1-100	4.45
		T5-1T	5	.3-300	.3-300	.6-200	.5-100	4.95
		T8-1T	8	.03-140	.03-140	.10-90	1-60	7.95
		T13-1T	13	.3-120	.3-120	.7-80	5-20	4.95
		T16-6T	16	.03-75	.03-75	.06-30	.1-20	5.65
	TH	T4-1H	4	10-350	10-350	15-300	25-200	5.95
	TMO	TMO1-1T	1	05-200	.05-200	.08-150	.2-80	7.95
		TMO2-1T	2	.07-200	.07-200	.1-100	.5-50	8.45
		†TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	8.45
		†TMO3-1T	3	.05-250	.05-250	.1-200	.5-70	7.95
		TMO4-1	4	.2-350	.2-350	.35-300	2-100	6.25
		TMO5-1T	5	.3-300	.3-300	.6-200	5-100	8.45
		TMO13-1T	13	.3-120	.3-120	.7-80	5-20	8.45
B* PRI  SEC	TT	TT1-6	1	.004-500	.004-500	.02-200	.1-50	6.95
		TT1.5-1	1.5	.075-500	.075-500	.2-100	1-50	5.95
		TT2.5-6	2.5	.01-50	.01-50	.025-25	.05-10	6.45
		TT4-1	3	.05-200	.2-50	.2-50	1-30	5.95
		TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95
		TT25-1	25	.02-30	.02-30	.05-20	.1-10	9.95
	TTMO	TTMO25-1	25	.02-30	.02-30	.05-20	.1-10	11.95
		TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	11.45
		TTMO4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	13.95
C PRI  SEC	T	T1-1	1	.15-400	.15-400	.35-200	2-50	3.25
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		T1-6	1	.01-150	.01-150	.02-100	.05-50	5.65
		T1.5-1	1.5	.1-300	.1-300	.2-150	.5-80	4.45
		T1.5-6	1.5	.02-100	.02-100	.05-50	0.1-25	5.65
		T2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	4.45
		T4-6	4	.02-200	.02-200	.05-150	.1-100	4.45
		T9-1	9	.15-200	.15-200	.3-150	2-40	3.95
		T16-1	16	.3-120	.3-120	.7-80	5-20	4.45
		T36-1	36	.03-20	.03-20	.05-10	.1-5	6.95
	TO	TO-75	1	10-500	—	10-500	40-250	6.95
	TH	T1-1H	1	8-300	8-300	10-200	25-100	5.95
		T9-1H	9	2-90	2-90	3-75	6-50	6.45
		T16-H	16	7-85	7-85	10-65	15-40	6.45
	TMO	TMO1-02	1	1-800	1-800	2-500	—	9.45
		TMO1-1	1	.15-400	.15-400	.35-200	2-50	6.25
		TMO1.5-1	1.5	.1-300	.1-300	.2-150	.5-8	8.45
		†TMO2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	7.95
		†TMO4-6	4	.02-200	.02-200	.05-150	.1-100	7.95
		TMO6-1	6	.3-200	.3-200	.5-150	5-50	7.95
		TMO9-1	9	.15-200	.15-200	.3-150	2-40	7.95
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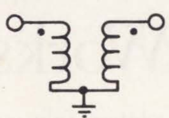
D PRI  SEC	T	T2-1	2	.050-600	.050-600	.1-400	.5-200	3.95
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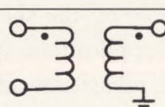
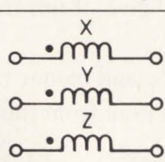
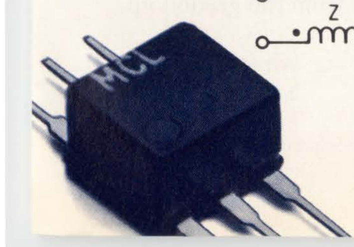
		T8-1	8	.15-250	.15-250	.25-200	2-100	3.95
		T14-1	14	.2-150	.2-150	.5-100	2-50	4.95
	TMO	TMO2-1	2	.050-600	.050-600	.1-400	.5-200	7.95
		TMO3-1	3	.5-800	.5-800	2-400	—	8.45
		TMO4-2	4	.2-600	.2-600	.5-500	2-250	7.95
		TMO8-1	8	.15-250	.15-250	.25-200	2-100	7.95
		TMO14-1	14	.2-150	.2-150	.5-100	2-50	8.45
	FT	FT1.22-1	1.22	.005-100	.005-100	.01-50	.05-25	35.95
		FT1.5-1	1.5	.1-400	.1-400	5-200	1-100	35.95
E PRI  SEC	FTB	FTB-1	1	.2-500	.2-500	.5-300	1-100	36.95
		FTB1-6	1	.01-125	.01-125	.05-50	.1-25	36.95
		■FTB-1-75	1	.5-500	.5-500	5-300	10-100	36.95
F 	T	T-622	1	0.1-200	0.1-200	0.5-100	5-80	3.25
		T626	1	0.01-10	0.01-10	0.2-5	.04-2	3.95



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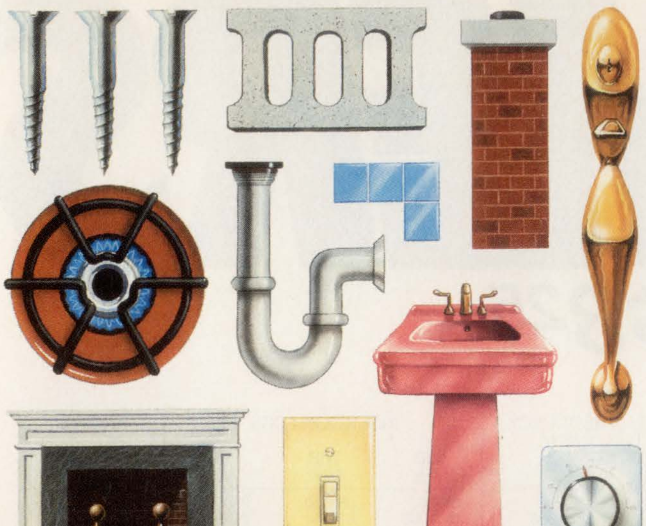
CIRCLE NO. 18



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CIRCLE NO. 19

How different people perceive the world

I remember talking with Charles Small about how different people perceive the world. I've worked as both a writer and visual artist, and it was fascinating to hear about the various modes of perception and expression.

At my workplace, a lot of thought and work is going into the development of practical user interfaces. Designing in-circuit emulators involves both engineering and programming skills, obviously. It strikes me that this development work is a new frontier.

Kathy Madison
Pentica Systems Inc
Cambridge, MA 02139.

(Ed Note: Essential reading is "The Visual Display of Quantitative Information" by Edward Tufte. Tufte, a statistician, rates graphics by an engineer as the greatest graphics ever produced. He has nothing good to say about art directors and computerized graphing programs.)

Switching from a PC to a workstation

In reference to Steven Leibson's editorial "Friendliness by the pound" (EDN, August 19, 1991, pg 55), I'd like to make a few points based on my experience transferring from a PC to a workstation.

[At our workplace] we operate a CAE program for analysis and design of electronic circuits in communications systems. We have been successfully utilizing the program on a PC for about five years. Toward the end of this period it became obvious that the PC was inadequate for our needs and that the software itself was being limited by operating under DOS, even with memory extension techniques like an LIM-compatible (Lotus-Intel-Microsoft) above-board and memory-management system.

At this point, the software house offered us a few choices:

1. Stay on a PC under DOS and use existing software (forever).
2. Stay on a PC, use OS/2, and get new hardware (extra memory, 386 machine).
3. Move to a workstation and use Unix.

Obviously (1) was not a valid long-term solution so we looked at (2) and (3). I attended shows and meetings on operating systems and learned a few key facts. The most important of these was if your application software runs better on one system than another (assuming similar hardware cost), ignore the OS and go for the best performance. With workstation prices falling and the proven track record for Unix, we went for option (3).

We got a shelf full of manuals (13 volumes), but we also got a condensed set of references similar in weight to the DOS manuals. So far, these have covered almost all we've needed to know. We also got good support from our software house. Our new workstation is a valuable addition to our development resources.

It's obviously more difficult to manage a workstation than a PC, but the extra effort to overcome teething problems is well rewarded. With regard to the technical editor, where was his software support? The Golden Rule here is to always make sure your system software is established on your platform and see it demonstrated before you decide. Workstations may not be necessary for the bit-time market yet, but their time will come.

Chris Vernon
Racal Communications Systems Ltd
Bracknell, Berkshire, RG12 1RG, UK

NEXT IN EDN

EDN's month-long exploration of FPGAs continues with the second part of Doug Conner's hands-on FPGA project, which will appear in EDN Magazine's April 23 issue. We wrap up our look at these devices in EDN News Edition's April 30 issue with a look at the hot new products in this field.

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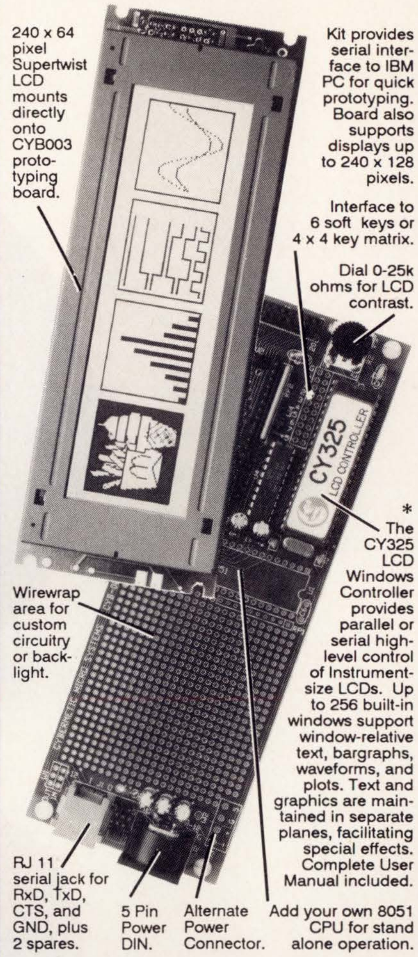

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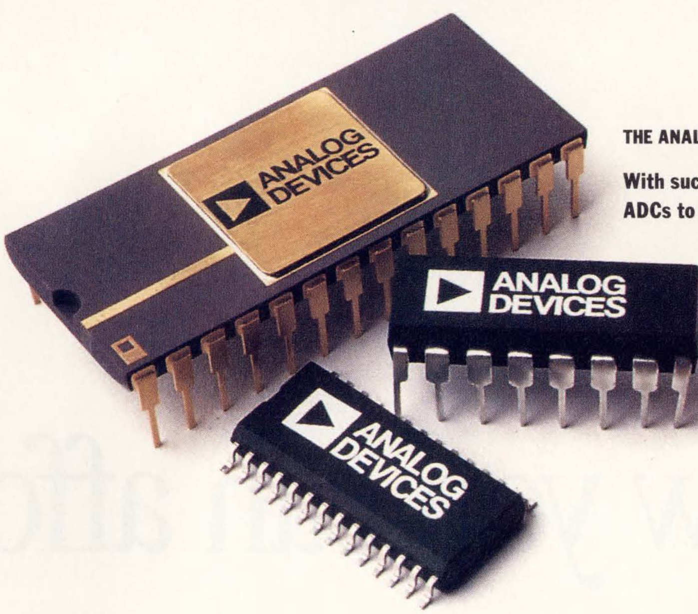

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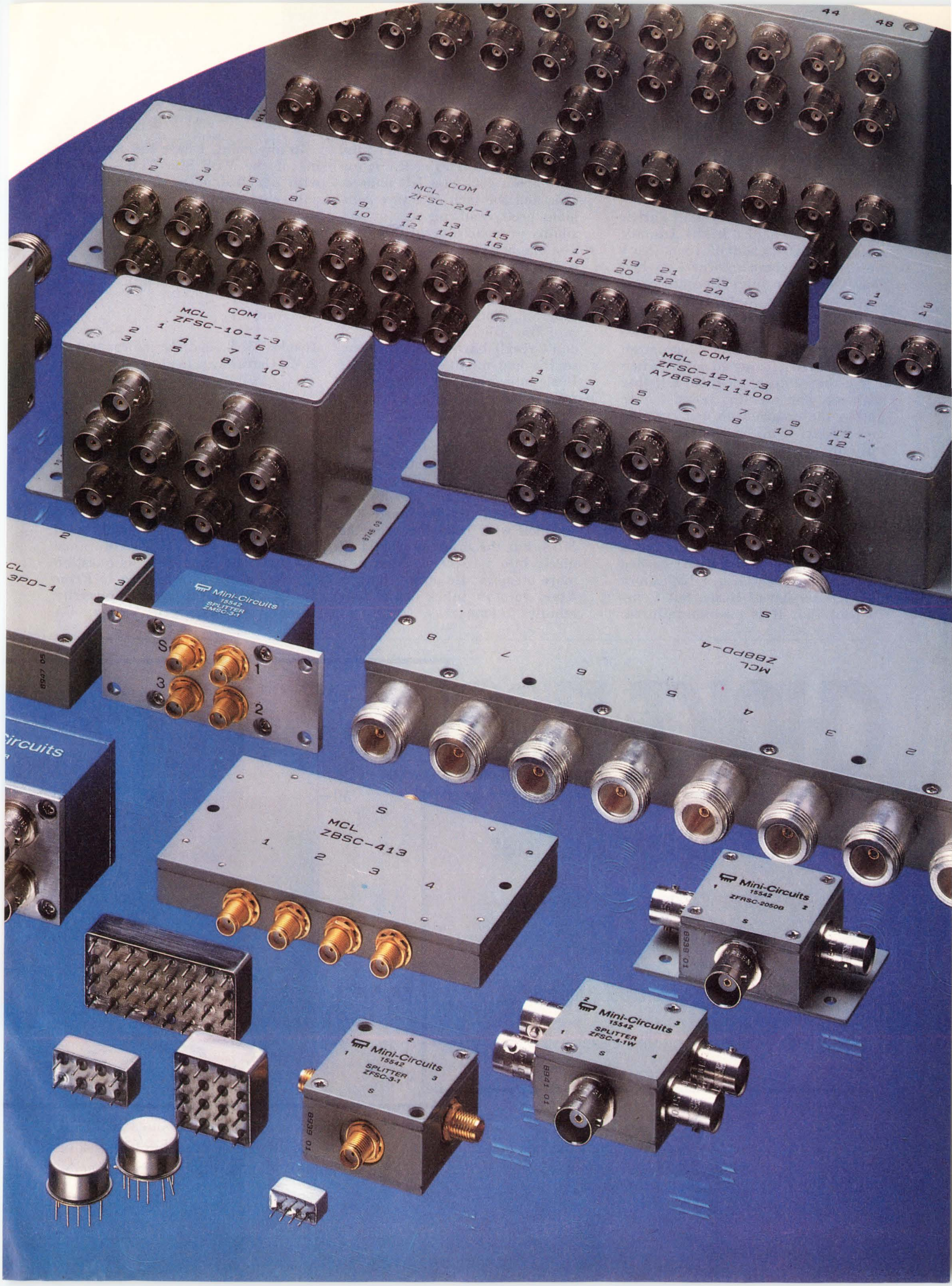
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EDITED BY JULIE ANNE SCHOFIELD

Ferengis, Romulans, and the Borg, beware

In reply to the request for information about Star Trek V2.0 in the January 2 issue of EDN, about 10 years ago I worked for a company where we had Star Trek on an Intel Microprocessor Development System (MDS). We spent a lot of lunch hours and spare time playing with it. As a result, we learned quite a bit about the program and produced a listing on paper. When I left the company, I took a listing with me, and over the years, I have gotten the program up and running on an Atari 520ST and worked intermittently on translating the program to C. What I've learned is:

- The program is written in Basic and is about 2000 lines long. The listing runs to 30 pages and has no PEEKs or POKEs.
- The object file on disk contains a Basic interpreter and an encoded version of the source. I don't know what version of Basic, but I suspect that it is custom tailored. When you load this into an Intel MDS with 64 kbytes of RAM, you have about 400 bytes left unused. This and the lack of a save command pretty well rule out any possibility of modifying the program.
- The one bug that I remember was a tendency for certain input combinations—I don't remember exactly which ones—to crash the program. Since I put the program into the Atari with ST Basic, I don't recall having this problem, so the bug might well be in the Basic interpreter.
- At one point I tried putting Star Trek into another 8-bit system with 64 kbytes of memory using a commercially available Basic interpreter. I got about three quarters of the program in (by typing it) and ran out of memory. I don't believe you would have much better luck with Intel Basic on the MDS, but the program should fit nicely into a 16-bit machine with more memory. Be aware that my Atari version takes about four minutes to load.

In any event, I have the paper listing of the MDS Star Trek—covered with penciled notes, but still readable—and would be happy to send a copy to Ask EDN. Or, if you have access to an Atari 520ST, I could send a disk with the source code for the ST version and the text file of an expanded instruction manual.

Ken Bartlett
San Jose, CA

Thanks. We'll send the information on to M J Garraway in the United Kingdom.

The how and why behind root-sum-squared calculations

In the February 3 edition of EDN, Gary Altman requested a theoretical justification for the commonly used root-sum-squared (RSS) tolerance analysis. The answer to his question is given in *An Introduction to Error Analysis* by John R Taylor, University Science Books, Mill Valley, CA

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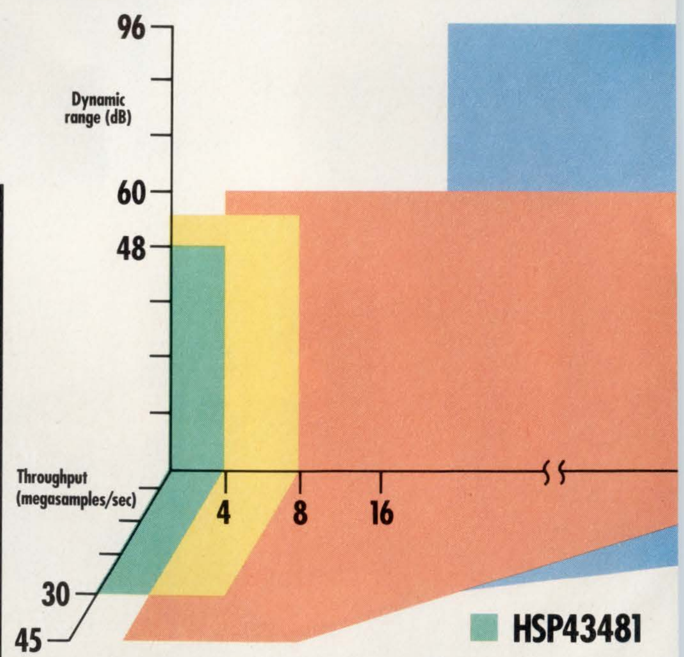

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($19.50 paperback, $24 hardbound). Chapter three develops tolerance equations suitable for electronic circuits. The inside cover summarizes the formulas. Every design engineer should read and understand this book.

Mr Altman has good reason to suspect the simplistic RSS approach; it is seldom correct. A dimensional check alone should set off a warning alarm. What could justify combining resistor tolerance, transistor gain tolerance, and offset voltage limits in this manner? Clearly, these diverse quantities need some conversion before they represent error contributions.

Begin the analysis with an algebraic equation for the observable properties of the design (voltage, current, force) in terms of component parameters. Parameters include resistance, capacitance, gain, offset, and leakage. Find a parameter's contribution to the observable properties' tolerance by taking the partial derivative of the equation with respect to that parameter. The result is an algebraic coefficient times the symbolic differential of the parameter. This coefficient does the appropriate scaling and dimensional conversion; the differential is going to accept something related to the parameter's tolerance.

Next, assume the tolerances have a Gaussian (normal random) distribution around the mean value. Deduce each parameter's standard deviation from specifications or from measurements. (The standard deviation provides a more informative measure of tolerance.) Multiply each parameter's standard deviation by the associated algebraic coefficient to obtain a corresponding standard deviation for the observable properties. The individual tolerance contributions (standard deviations) combine as the RSS when the statistics are Gaussian, as we have assumed.

Combining simple tolerances in the RSS manner is only valid when all the algebraic coefficients are 1 after numerical evaluation. Such is the case for serial propagation delays in digital circuits and for similar cascaded contributions. In most cases, however, the RSS of tolerances is meaningless.

If any readers need further help, Intrel Service Co offers production tolerance analysis and design reviews at reasonable cost.

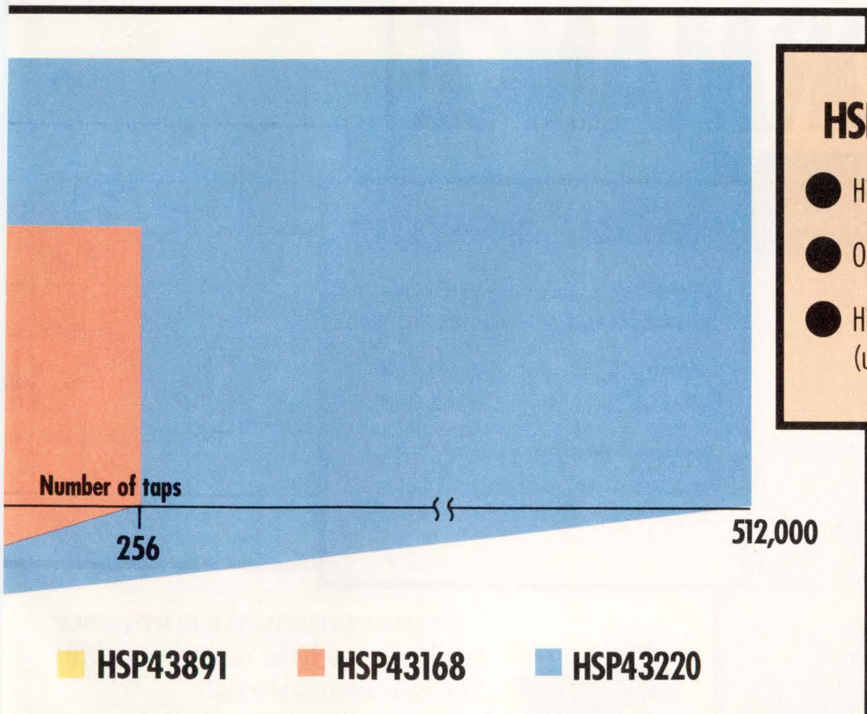
James A Kuzdrall, PE
President
Intrel Service Co
Nashua, NH

We received more than a dozen letters justifying root-sum-squared tolerance analysis, and yours said it best. Thanks.

Readers respond to Rieger's naggers

In the January 20, 1992, Ask EDN (pg 43), James Rieger posed three questions. The first question was about the ringer equivalence of devices hooked up to the dial-up telephone network. The second was about the characteristics of telecommunications devices for the deaf.

Approximately a dozen readers answered the first two questions. The best answers are printed here. The third



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CIRCLE NO. 25

question, about the carrier deviation for transmission of a satellite-relayed television signal, is still up for grabs.

Regulations define ringer equivalence

I can assist with Mr Rieger's query regarding ringer equivalency.

The definition of ringer equivalency is in the US Code of Federal Regulations, Title 47 (Telecommunication), Part 68 (Connection of Terminal Equipment to the Telephone Network), section 68.312 (On-Hook Impedance Limitations), paragraph d. This definition is implemented in the FCC Instructions to Form 730 (Application for Part 68 Registration). The purpose of 47 CFR 68, known in the industry as FCC Part 68, is the protection of the telephone network.

Two major types of ringers, A and B, are manufactured depending on the desired frequency coverage. The ringer load is not necessarily all real. To determine the ringer equivalence number (REN), first measure the impedance of the ringer of a product as indicated: Type A ringer, 20 and 30 Hz; Type B, 15.3 through 68 Hz. The lowest impedance measured is used as the denominator. The numerator comes from FCC Part 68 based on the historical impedances of ringers: Type A, 7000 for 20 Hz; 5000 for 30 Hz; Type B, 8000. An example of this calculation is REN7000÷Z for a Type A ringer driven at 20 Hz.

FCC rules state that telephones and other equipment may be connected to a telephone line (called a loop) as long as the sum of their RENs is equal to or less than 5.0. There are two reasons for this requirement: (1) a ringing signal from a telephone central office contains sufficient energy to ring only so many loop-powered telephones of average design; and (2) if a telephone's ringing were not answered, telephone-company equipment would be tied up unnecessarily, generating excessive trouble reports. This last situation would cause impairment of service to other customers.

Because complex impedance is not included in the definition of REN, and complex impedance affects the ability of the central office to deliver ringing energy, many telephone companies state in their tariffs that they will provide sufficient energy to cause ringing of equipment having a sum REN less than or equal to 4.0.

FCC Part 68 is being reviewed for possible updating by the Regulatory Issues Subcommittee of the Telecommunications Industry Association Engineering Committee. C L Berestecky of AT&T is chair of the subcommittee. The instructions to FCC Form 730, Application for Part 68 registration, are administered by William von Alven of the FCC Staff, Industry Administrative ad hoc Advisory Committee, Mr Ronald G Provost of Bell Communications Research, Chair.

Clifford E Chamney
Member of Technical Staff
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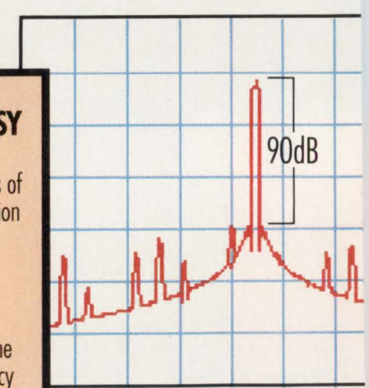

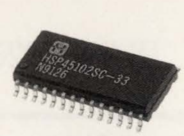

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Address for TDD information

I have an address that might help James Rieger find out more about telecommunications for the deaf (TDD):

Telecommunications for the Deaf Inc
8719 Colesville Rd, Suite 300
Silver Spring, MD 20910
(301) 589-3786.

Kourosh Derakhshani
Transistor Devices Inc
Randolph, NJ

Frequency pairs for TDDs

In answer to Mr Rieger's question about telecommunications devices for the deaf, I think I can shed some light on the subject.

The original teleprinters used on the National Deaf Phone TTY/TDD Network ran 60 wpm, or 45 baud, Baudot Code in compliance with the Weitbrect FSK standards of 1400-Hz mark and 1800-Hz space frequencies. These early TTYs (teletypewriter units) did operate at half duplex, and the go-ahead characters were typed at the end of each message to keep the operators from stepping on each other's fingers. All the early modems used acoustic coupling, but as phone regulations softened up, modems started appearing with both direct and acoustical coupling. Portable telecommunications devices also came out with Bell 103 standards and ASCII with 110/300-baud capabilities. The 103A3 frequency pairs are

Mode	Frequency	Mark frequency (Hz)	Space frequency (Hz)
Originate	T f1	1270	1070
Originate	R f2	2225	2025
Answer	T f2	2225	2025
Answer	R f1	1270	1070

I hope this answer helps Jim get some sleep. I'm sorry, but I don't feel qualified to answer his third question.

Mike Phillips
Dartech Engineering
Winston, OR

Still stumped by third nagger

James Rieger's third question was "What is the carrier deviation for transmission of a satellite-relayed television signal? Because the television waveform is asymmetrical, what is the position of blanking with regard to the band edges of the channel? Does white cause a positive deviation of the carrier frequency of a negative one?" Please contact Ask EDN if you can put this one to rest.

Ask EDN solves nagging design problems and answers difficult questions. Address your letters to Ask EDN, 275 Washington St, Newton, MA 02158. FAX (617) 558-4470; MCI: EDNBOS. Or send us a letter on EDN's bulletin-board system at (617) 558-4241: From the Main System Menu, enter SS/ASK_EDN and select W to write us a letter.

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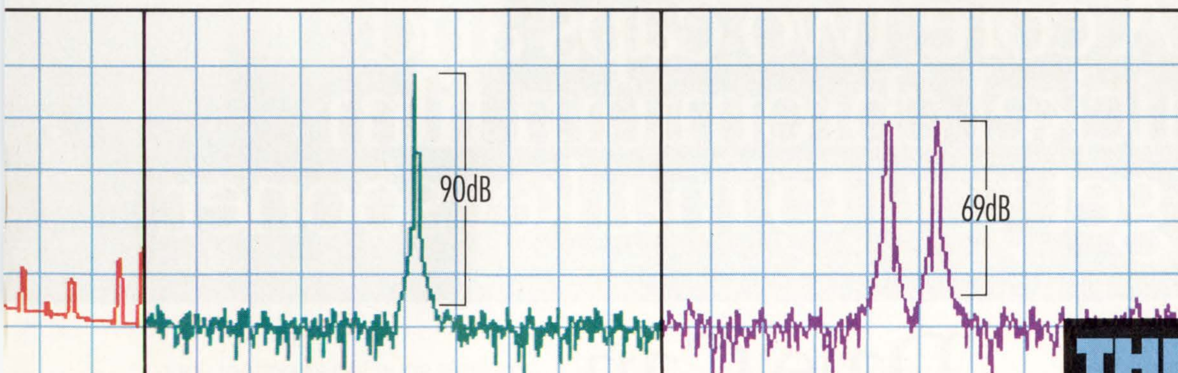

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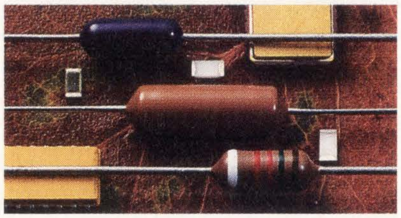

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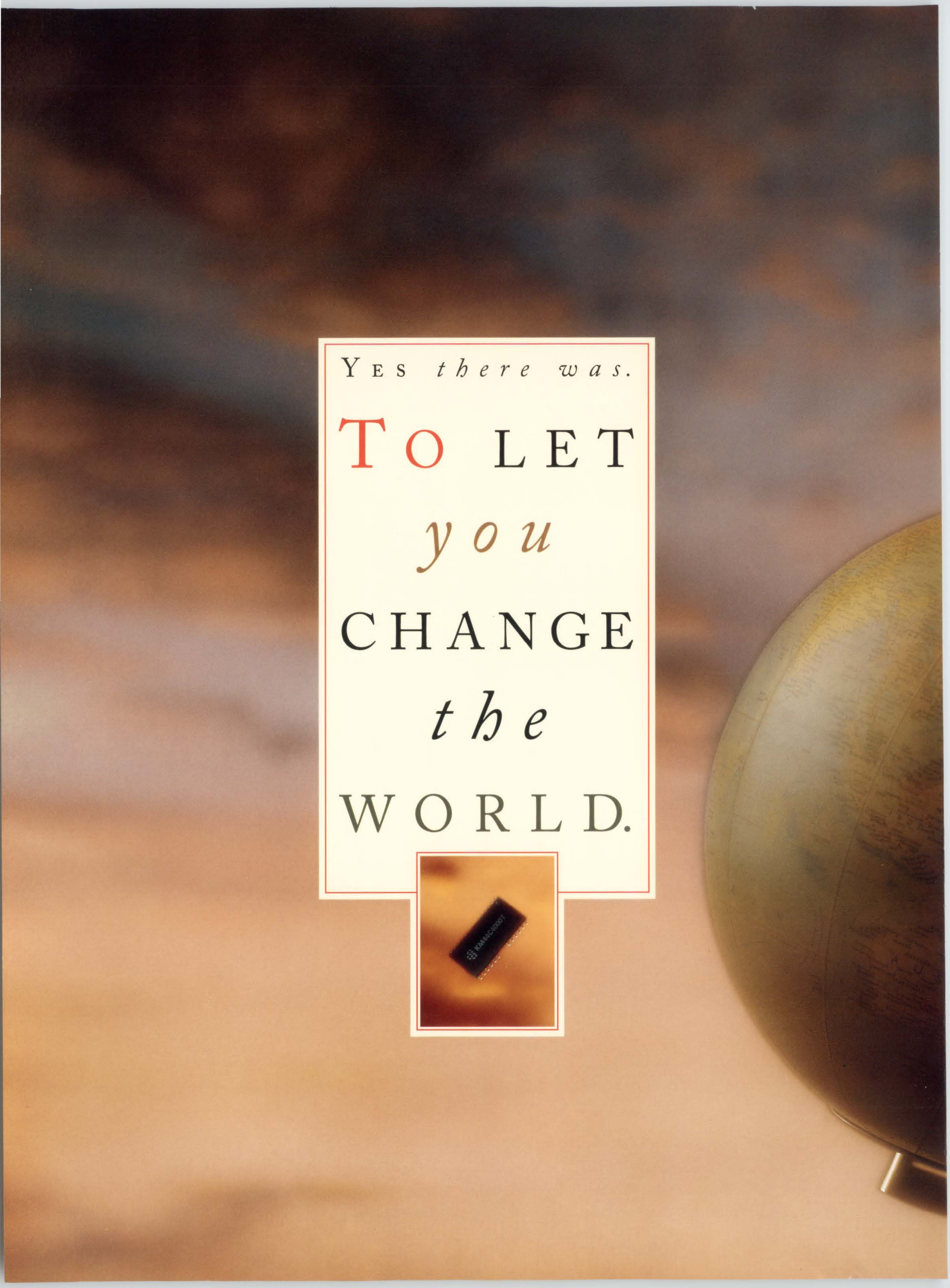
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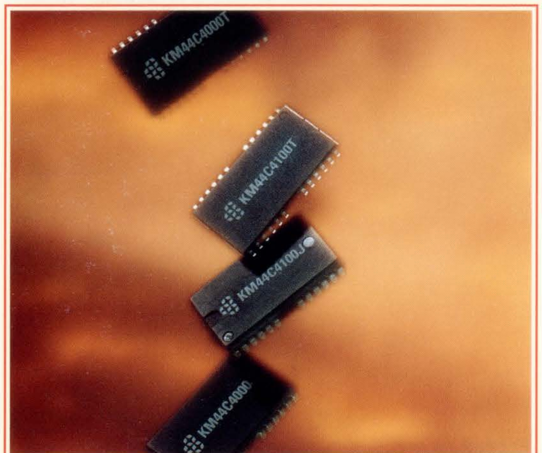

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Don't tread on me

For some reason, we in the US seem to think that government interference is a good thing, even when it runs contrary to common sense. Two recent issues in the news prove the point: high salaries for company presidents and re-regulation of the cable-TV business.

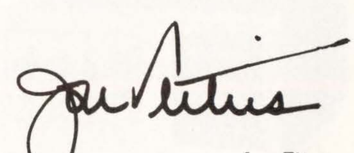
In mid 1991, *Forbes* magazine reported that Steven J Ross of Time Warner Inc received more than $78 million in compensation. No wonder Japanese executives complain that US companies pay their executives too much. Comments from the Japanese and reports in the press set off a storm of protest in Washington. Legislators have proposed rules and regulations that would limit executive pay and compensation. This is a wrong-headed approach. Frankly, executive pay is an irrelevant issue.

Most of us agree that performance should be rewarded and that many executives are overpaid for what they do. However it probably doesn't matter to you and me. So what if Apple Computer's John Sculley earns $16 million per year? He has to do something with that money. It goes back into the economy, being spent and invested in many ways. It doesn't disappear.

Sculley's high salary expenditure may mean that Apple has less to spend on basic research, but it's up to the company's board of directors and its stockholders to determine that. I own no Apple stock, so whether Apple pays Sculley one dollar or $16 million is irrelevant to me. If Apple loses its competitive edge because it pays its executives too much, it's the investors who will lose. A more competitive computer company that spends its money better will take Apple's place.

Competition and risk are important concepts, often beyond legislators' understanding. Stripped of many regulations, the cable industry has become more competitive as investors have risked money on new ventures. As always, competition spawns variety. Here in the US, I can watch programs that range from religious services to first-run movies, and from rock-music videos to 24-hour newscasts. However, the increasing costs of cable-TV services have sparked Congress to consider re-regulating cable TV. Our legislators fear that networks will take over cable channels and will charge for broadcast programs that they provide for free today.

Today's innovative technologies mean that there will be more competition in the television arena, not less. Fiber-optic cables will broaden the spectrum of services, and small, start-up program suppliers will have easy access to our TV sets. It's unlikely that today's TV-program and network giants will obtain a stranglehold on our viewing habits. Even if they could, their monopoly would only be temporary. In the meantime, we could always turn off the TV and read a book . . . or a magazine.



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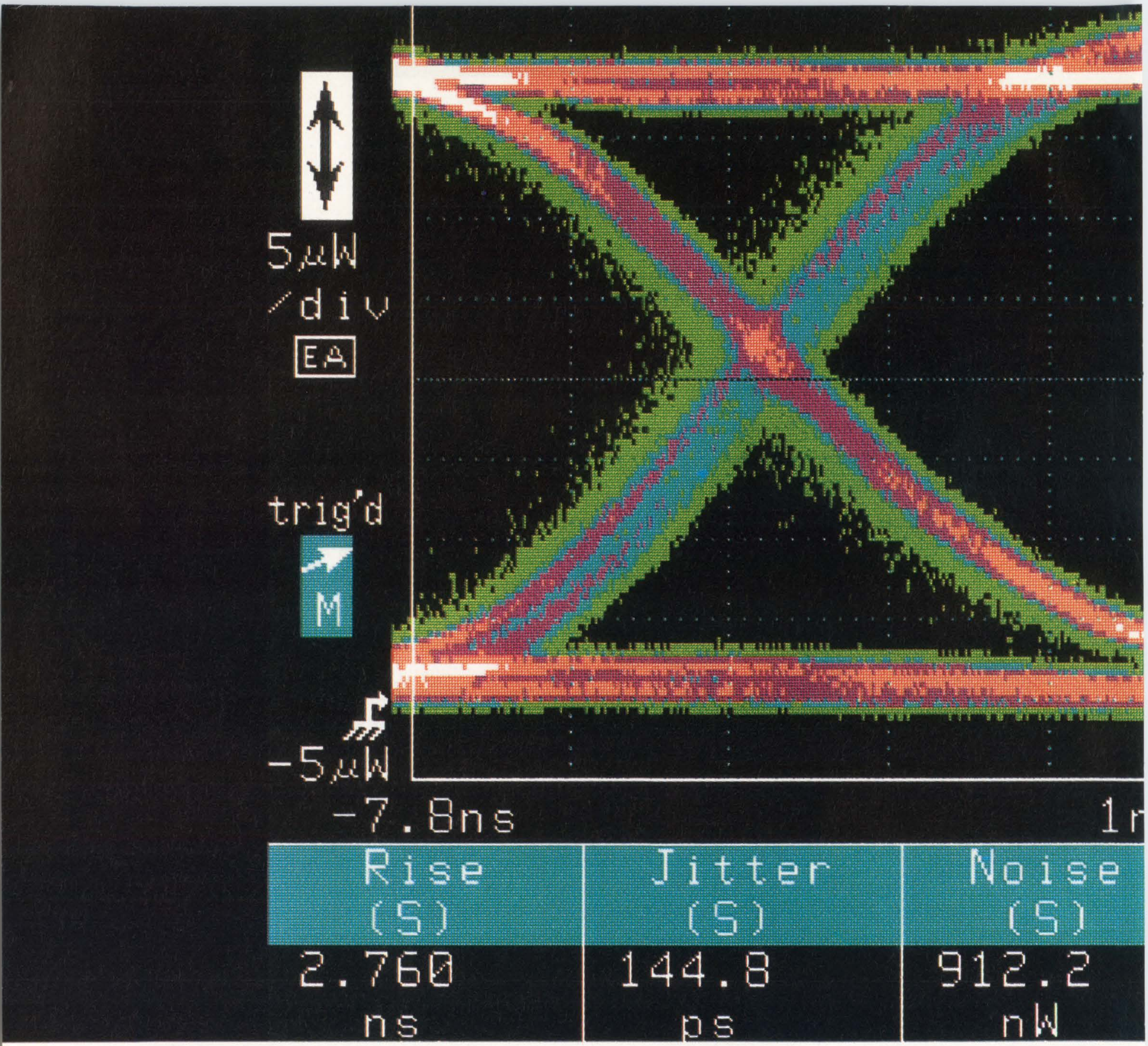

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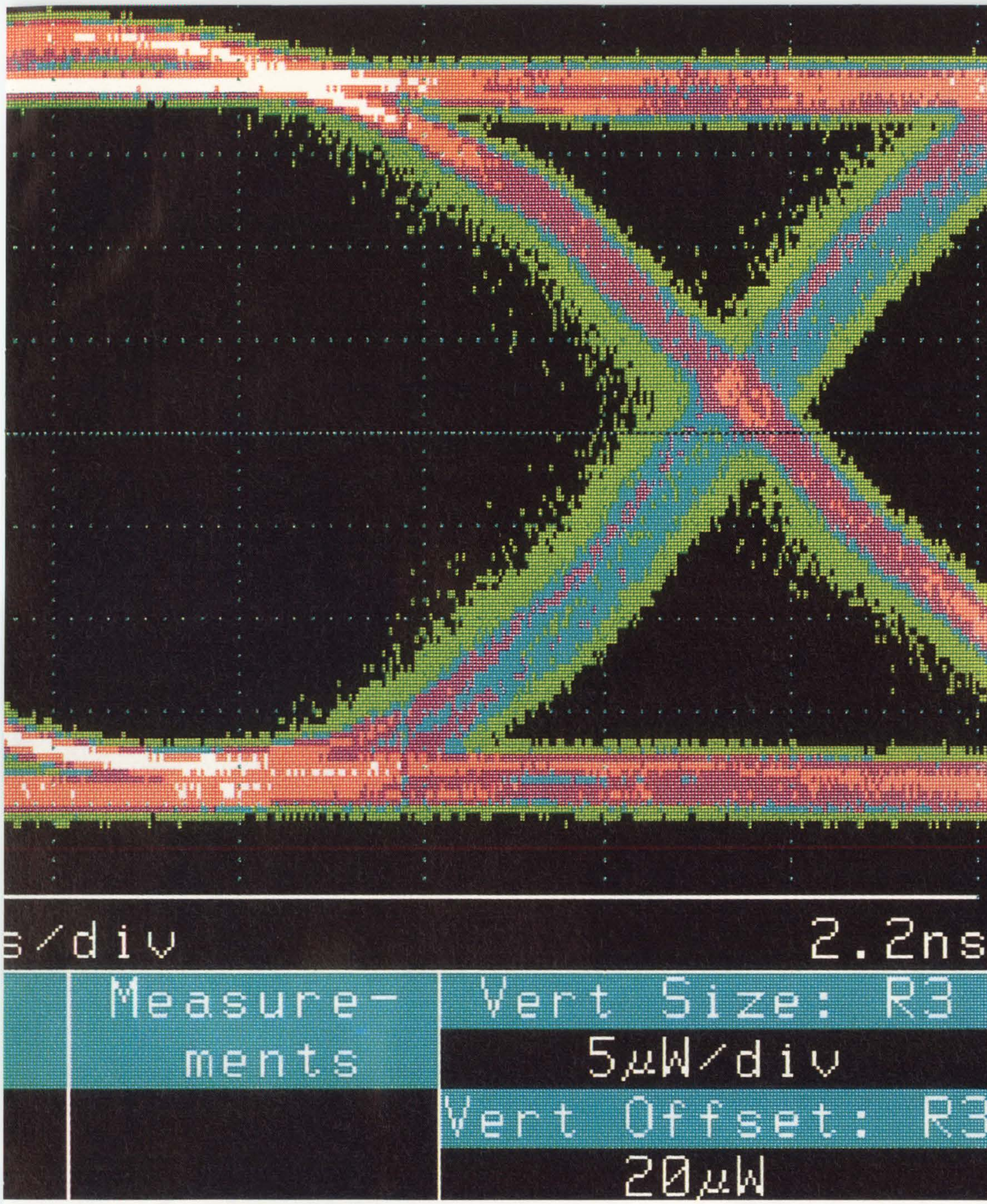

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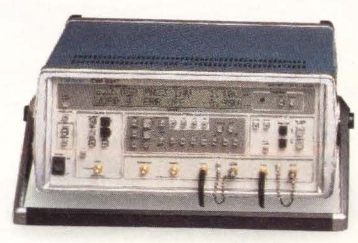

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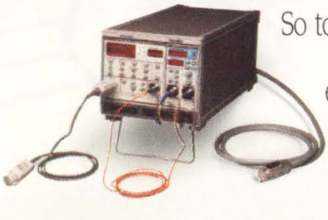

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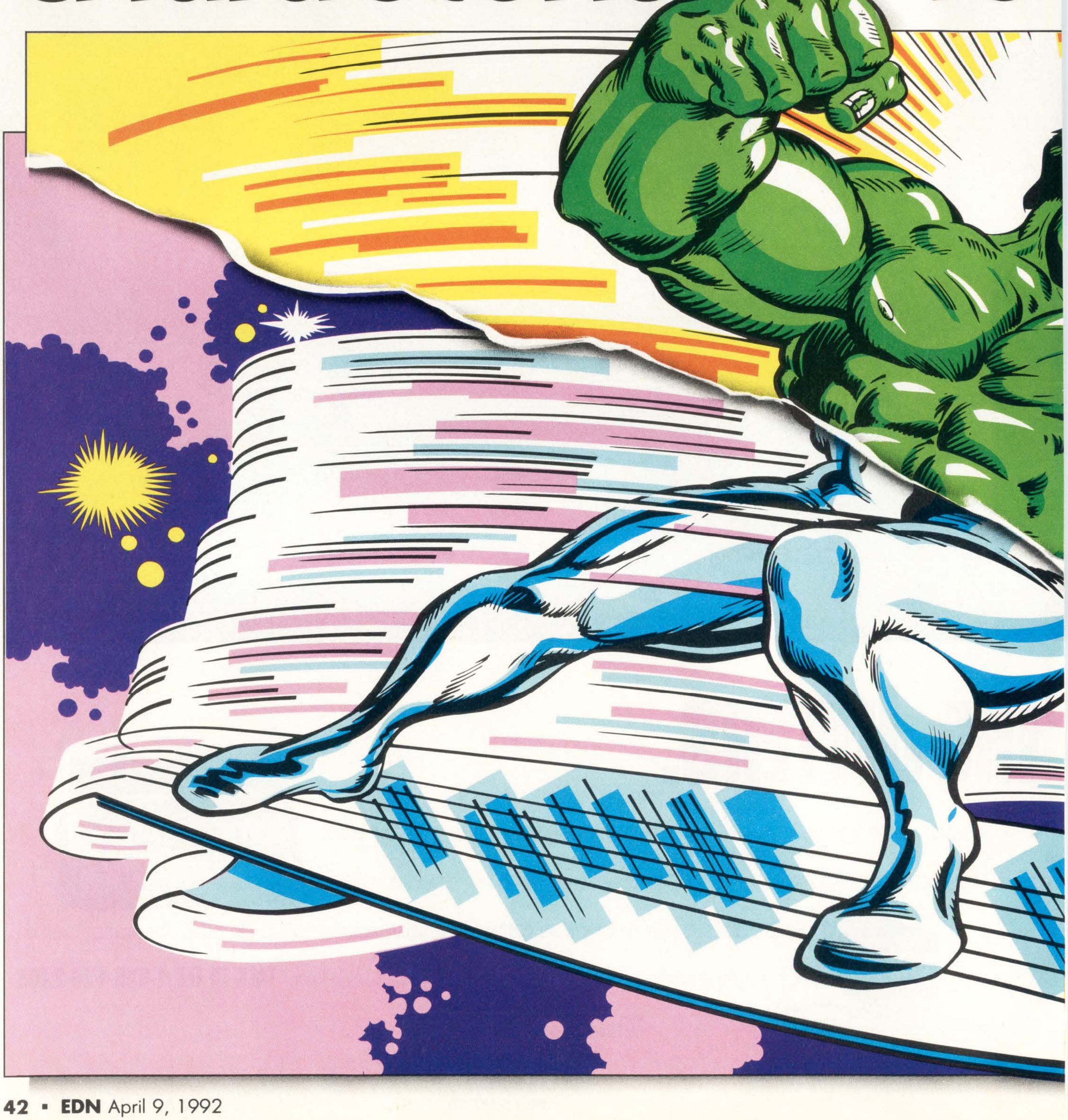

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CIRCLE NO. 29

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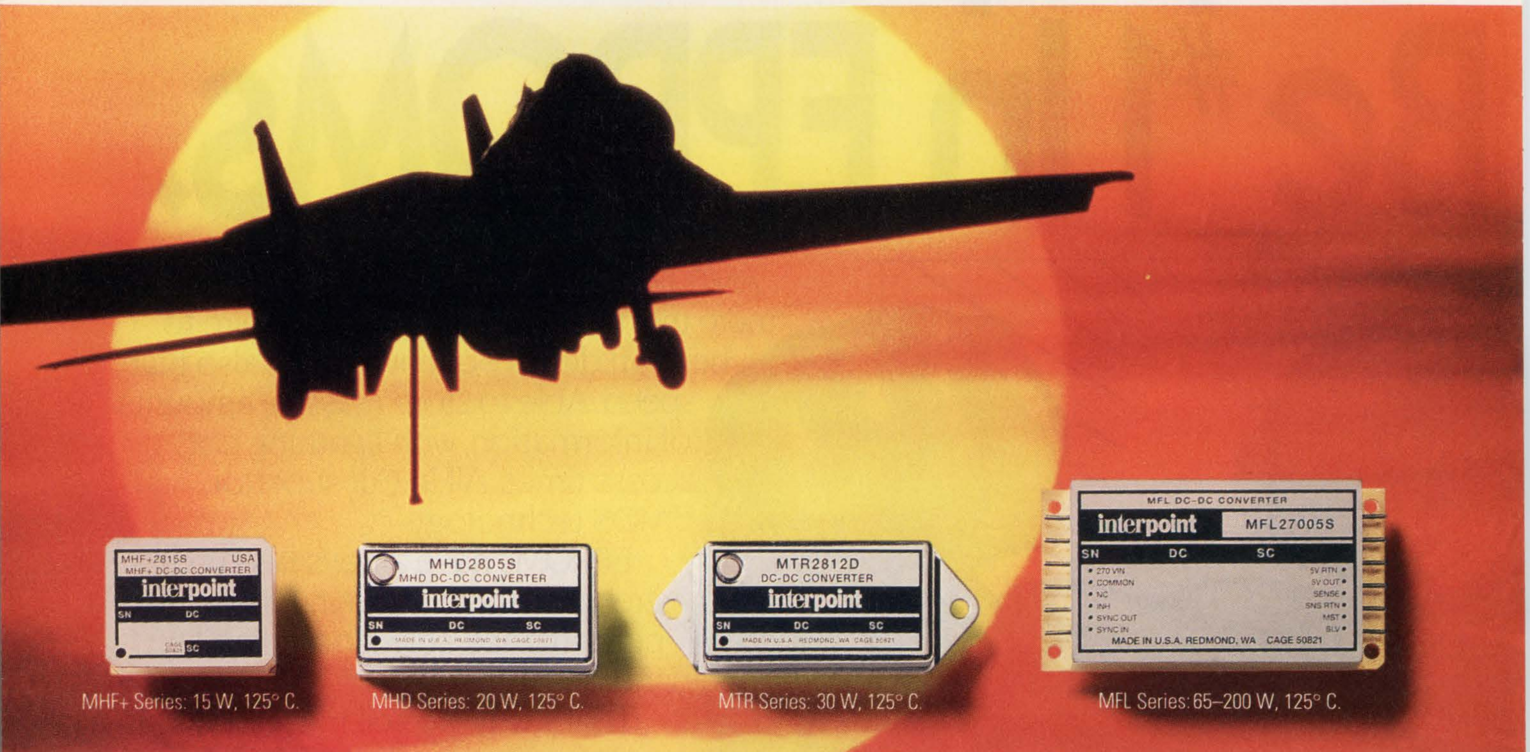

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CIRCLE NO. 57

Design software links active-filter performance with real devices

ANNE WATSON SWAGER, Technical Editor

Analog filter-design software helps to not only perform filter designs' obligatory math quickly, but some programs can also select the right active and passive components to implement the filter. First, be sure the software supports the filter ICs that best match your overall system requirements.

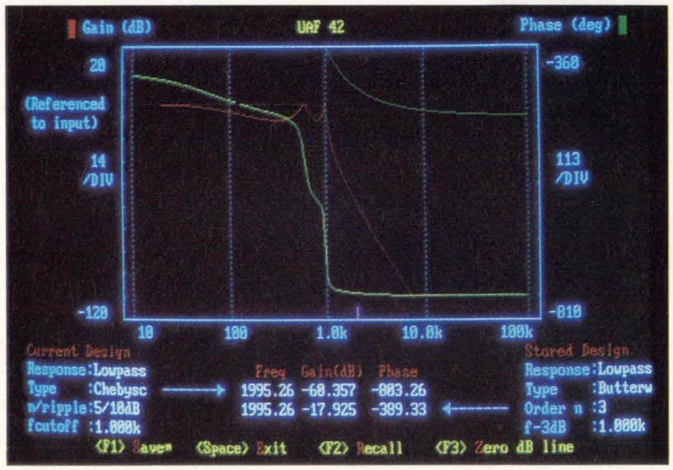
Active-filter design software takes the tedium out of a mathematically intensive job. Because equations so closely predict an analog filter's performance, software that solves those equations is obviously a useful tool. Without performing the math, it'd be virtually impossible to design any filter with predefined characteristics. "You can't hack filters on the bench," points out Jim Williams of Linear Technology. Software is also the best candidate to perform the numerous iterations required to optimize the filter for a particular characteristic.

Tremendous numbers of active-filter design packages exist (**Ref 1**), and are available from software vendors, IC vendors, and shareware-program vendors (such as those you'll find posted on EDN's Bulletin Board in the CAE special interest group—do a key word search for "filter"). IC vendor programs are either free or cost as much as $40. Shareware vendors generally ask a registration fee of around $30. Software vendors offer software starting above $500.

The packages listed in **Table 1** comprise a subset of all filter-design software that not only calculate a filter's parameters from filter specifications, but also provide a way for you to implement that filter. As a group, these software packages offer easy-to-use tools that span a range of features and prices. It's very easy to pick up any one of these packages and go to work designing filters.

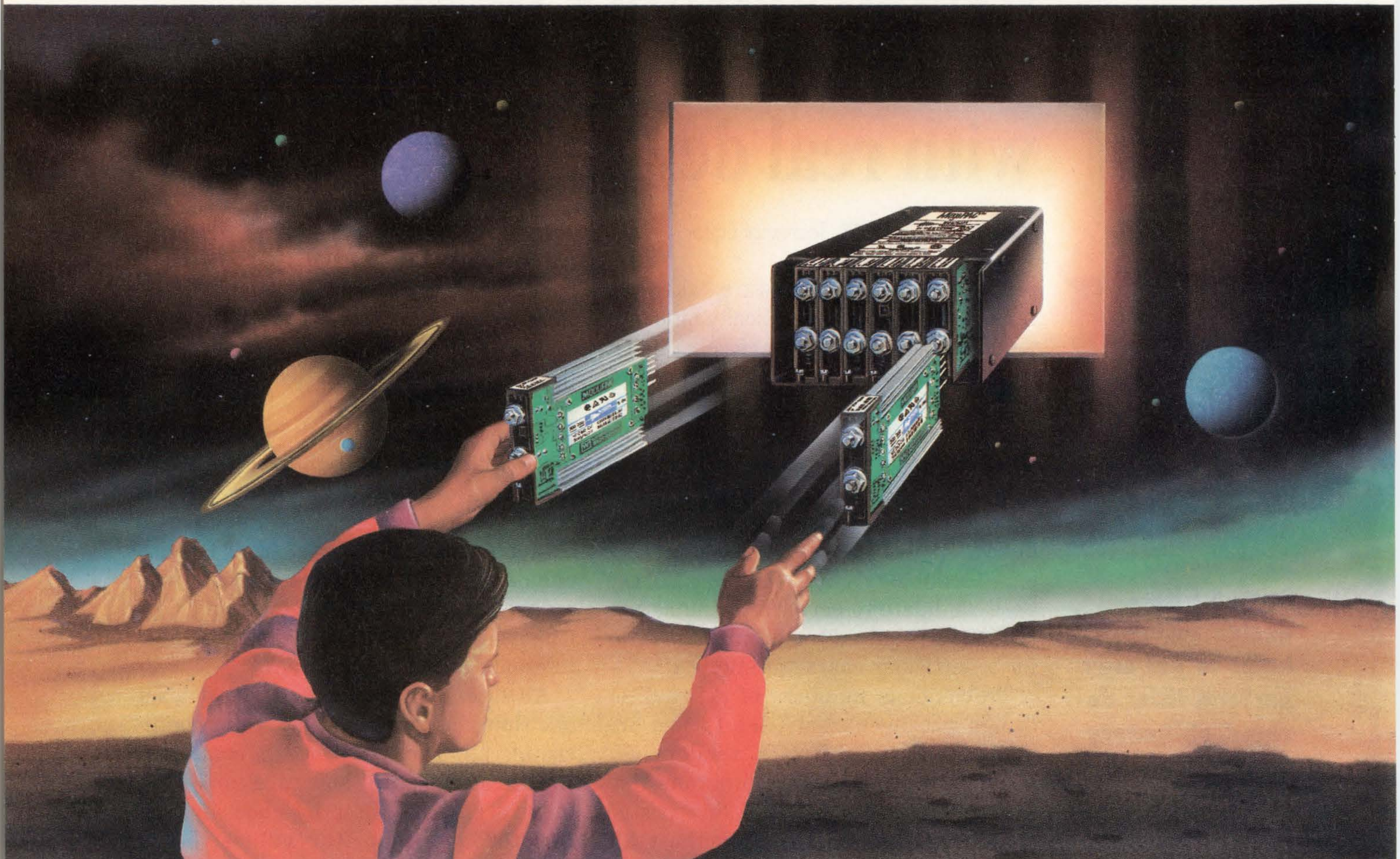
However, the package that will ultimately make the most of your filter-design time depends on the proposed filter. No design software will make you an expert, and most of the packages require that you know quite a bit about the filter you want to design. What are the required frequency *and* time-domain characteristics? Does your filter fit with one of the classical filter-response characteristics, such as Butterworth or Chebyshev, or will you need to be able to create a custom function?

All filter-design packages do at least one thing for you—calculate filter coefficients, f_ns, and Qs. Once it completes the calculations, the software can implement a physical filter by choosing real resistor and capacitor values. Some packages are intended for continuous-time filters only, others for switched-capacitor filters only. Of those that can



IC vendors' software offers useful help for a bargain. The Filter42 portion of Burr-Brown Corps Filterpro, which the company provides for free, features on-screen prompts and graphical displays to guide the user through the selection of the filter type and active RC circuit values.

POWER To Configure



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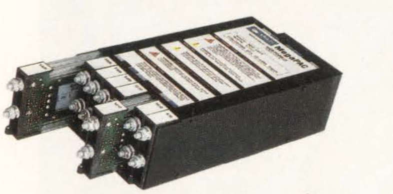

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Component Solutions For Your Power System

CIRCLE NO. 31

select passive component values for continuous-time filters, the software doesn't necessarily support a wide range of the numerous circuit topologies.

The starting point

So, before even using the software, it's a good idea to briefly review the various types of active filters and their pros and cons. Two basic types of active filters exist: continuous time—typically those composed of op amps, resistors, and capacitors known as active RC—and switched-capacitor filters.

As their name suggests, continuous-time filters work from continuous streams of analog data. Switched-capacitor filters use a switched-capacitor network to emulate a resistor, thereby replacing most of the resistors in an active RC filter with switches and capacitors (**Ref 2**). Since a clock drives the switched-capacitor network, these filters are a type of sampled-data system.

The biggest differences between active and switched-capacitor filters are size, noise, and ease of use. Switched-capacitor filters generally require much fewer parts than continuous-time types, for which op amps, resistors, and capacitors add up quickly as you increase the number of poles.

However, continuous-time vendors, such as Burr-Brown and Maxim, continue to develop filters with higher integration. Burr-Brown's UAF42 ($6.95 (100)) contains three op amps that can implement a 2-pole filter. Maxim's MAX275 ($3.75 (1000)) and MAX274 ($4.95 (1000)) have built-in op amps and capacitors that, together with external resistors, can create fourth- and eighth-order filters in 20- and 24-pin packages, respectively.

Continuous-time filters have a leg up on switched-capacitor types when it comes to very low noise requirements. The noise of the current generation of switched-capacitor filters is much lower than earlier devices. However, continuous time filters are still a better choice if signals are in the millivolt range.

Another way of expressing the noise issue is that continuous time filters have a wider dynamic range than switched-capacitor types. If you're looking for 100 dB of dynamic range, you'd be hard pressed to find a switched-capacitor filter to meet this requirement. A typical switched-capacitor filter exhibits noise on the order of 150 μV of noise, making it impossible to achieve 100 dB of dynamic range. Such a filter could provide 80 dB, however.

Switched-capacitor filters can be easier to use than continuous-time filters because they don't require tuning adjustments to compensate for component tolerances. The

Table 1—Representative IC filter-design software

Vendor	Program	Filter implementation	Filter topology(s)	Filter type(s)	Filter response(s)	Commercial ICs supported	Price	Comments
Burr-Brown Corp	Filterpro (Filter 1, '2)	Active RC	Sallen-Key and multiple feedback	Lowpass	Butterworth, Chebyshev, and Bessel	Suggested op amps	Free	
	Filterpro (Filter 42)	Active RC with URF42 filter IC	Any state-variable filter pole pair.	Lowpass, highpass, bandpass, notch	Butterworth, Inverse Chebyshev, and Bessel	UAF42 only	Free	
International Microelectronic Products Inc	IMP42011 Filter Synthesis Tool Set	Continuous-time, programmable	Integrated biquad cells	Lowpass, allpass	Bessel, Equiripple	IMP42C55	$995	Includes evaluation-system hardware.
Linear Technology Corp	FilterCAD	Switched capacitor	State variable	Lowpass, highpass, bandpass, notch	Butterworth, Chebyshev, and Elliptic	LIC1059, 1068, 1061, 1064, and 1164	$40	You can obtain Bessel responses by manually entering pole and zero valves.
Maxim Integrated Products	MAX274 Evaluation Kit	Continuous time	State variable	Lowpass, highpass, bandpass, notch, and allpass	Butterworth, Chebyshev, and Bessel	MAX274	$20	Evaluation kit includes design software, evaluation board, and MAX274 IC.
Microsim Corp	Filter Designer (Standard and Advanced)	Active RC and switched capacitor	Active RC biquads (12 types), switched-capacitor biquads (5 types)	Lowpass, highpass, bandpass, and notch	Butterworth, Chebyshev, Inverse Chebyshev, and Elliptic	IMP's lowpass, programmable, linear-phase, continuous-time filters and Linear Technology's switched-capacitor filters.	$600 (standard) $1800 (advanced)	Macintosh versions also available.
National Semiconductor Corp	Switched Capacitor Filter Software Design Tools	Switched capacitor	State variable	Lowpass, highpass, bandpass, and notch	Butterworth, Chebyshev, and Elliptic	MF10, MF5, MF8, LMF100	Free	

switched-capacitor filter depends entirely on capacitor value ratios and not on absolute values, thereby removing any need to tune the filter other than setting the switching frequency. Also because a switched-capacitor filter doesn't rely on component tolerance, it can achieve somewhat higher Q values.

A switched-capacitor filter has the added elegant feature that the filter's cutoff frequency scales with the clock frequency. So, by changing the clock, you can modify the filter on the fly.

Switched-capacitor filters have been known to suffer from artifacts such as clock feedthrough and aliasing. Both of these effects have been reduced by IC designer's efforts. Putting a simple RC filter at the output of a switched-capacitor filter is sufficient to remove any clock-feedthrough artifacts and prevent aliasing.

Choose the architecture

These characteristics are all general distinctions between continuous-time and switched-capacitor filters. But within each type there are choices to be made. IC manufacturers generally implement switched-capacitor filters in a state-variable form. However, this general form is but one possible type of active filter architecture (**Fig 1**). Depending on the arrangement of the resistors and capacitors around the components, numerous combinations are possible (look in any filter textbook for examples).

These numerous combinations exhibit different filter characteristics, such as low or high sensitivity and wide or narrow range of Qs. Biquadratic filters, those whose transfer functions contain complete quadratic equations in both the numerator and denominator, can implement lowpass, highpass, and notch filters. A state-variable filter is one type of a biquad filter. Each filter architecture has its pros and cons, the discussion of which already fills up volumes. **Ref 3** is one place to start to learn more about the specifics of practical filter architectures.

It's all in the application

The next step after deciding on the filter topology is choosing a filter response, such as Butterworth, Chebyshev, Inverse Chebyshev, Bessel, and Elliptic, or choosing some nonclassical filter response. These classic filter responses and their characteristics are very well documented in textbooks and vendors' application literature. Which response is best is purely a system-level decision. **Fig 2** gives a very quick overview of the frequency and time-domain responses of the classical filters. A filter that has the desired frequency response can exhibit undesirable time-domain effects, such as excessive ringing.

With the filter topology and desired response in hand, filter-design software programs can not only calculate the filter coefficients, but go through the tedium of choosing passive component values for you

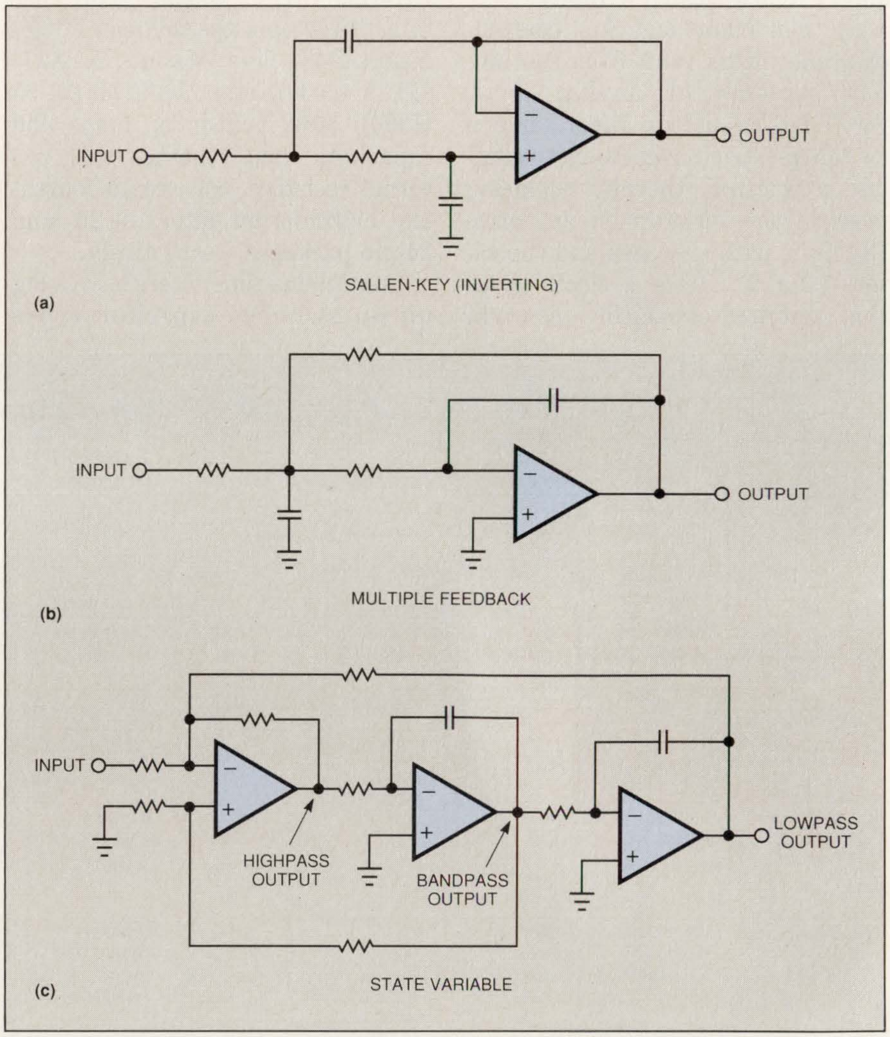

Fig 1—Different filter architectures have inherently different characteristics. For example, the sensitivities of a multiple feedback filter (a) are lower than that of a Sallen-Key (b). Also, unlike Sallen-Key and multiple-feedback filters shown, state variable filters (c) are a type of biquadratic filter, which means they can implement any filter type including lowpass, highpass, and bandpass. (Note that this figure only shows active RC implementations of the filters.)

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CIRCLE NO. 32

IC FILTER-DESIGN SOFTWARE

as well. The software included in **Table 1**—by no means a compilation of all the software available—goes one step further by connecting the desired filter performance to real devices. Most of these packages are design tools provided by vendors to help make it easier to use their filter ICs.

However, Microsim's Filter Designer also includes information on International Microelectronic Products' continuous-time filters and Linear Technology's switched-capacitor ICs. Filter Designer clearly provides the widest choice of filter topology. After specifying the filter and determining the coefficients, you can choose between active-RC and switched-capacitor biquadratic filter architectures and several popular commercial IC filters.

Don't expect the moon

National Semiconductor was the first of the filter IC vendors to come out with a filter-design package in 1987. Since then, Burr-Brown, Maxim, and Linear Technology have joined in. These packages' interfaces are somewhat more glitzy than National's program, which just asks you a series of filter-specification questions, but ultimately these packages perform the same steps. The software first calculates mathematical filter parameters, and then implements a filter and chooses passive component values using one of their devices.

The abilities of these programs do have limits, however. Note that not all the software listed in **Table 1** can compute values for all filter response characteristics. All of the software packages do Butterworth and Chebyshev, but not necessarily Inverse Chebyshev, Bessel, and Elliptic. And, even though Maxim's software can calculate poles, zeros, and Qs for highpass and notch filters, the MAX275 can't implement filters that include zeros.

Most of the packages place limits on filter order. National's program can handle tenth-order lowpass and highpass filters and twentieth-order bandpass and notch designs. Burr-Brown's programs, for example, can go as high as eight poles. In some cases, you must specify the filter order. In others, the software determines the necessary order depending on the filter specifications.

The programs also have limitations on resistor accuracy. Many of the packages have just two options for resistor values: 1% or exact. National's program for the MF10 allows either 1% or 5% resistors. With Microsim's Filter Designer, resistor tolerances can be 1, 5, or 10%; capacitors can only be 5%. Burr-Brown's programs let you input real capacitance values if you choose to actually measure them.

Despite these various limitations, the packages are easy to use and have convenient user interfaces. For example, Maxim's software works like a spreadsheet, calculating new filter values as you move cursors and change filter specifica-

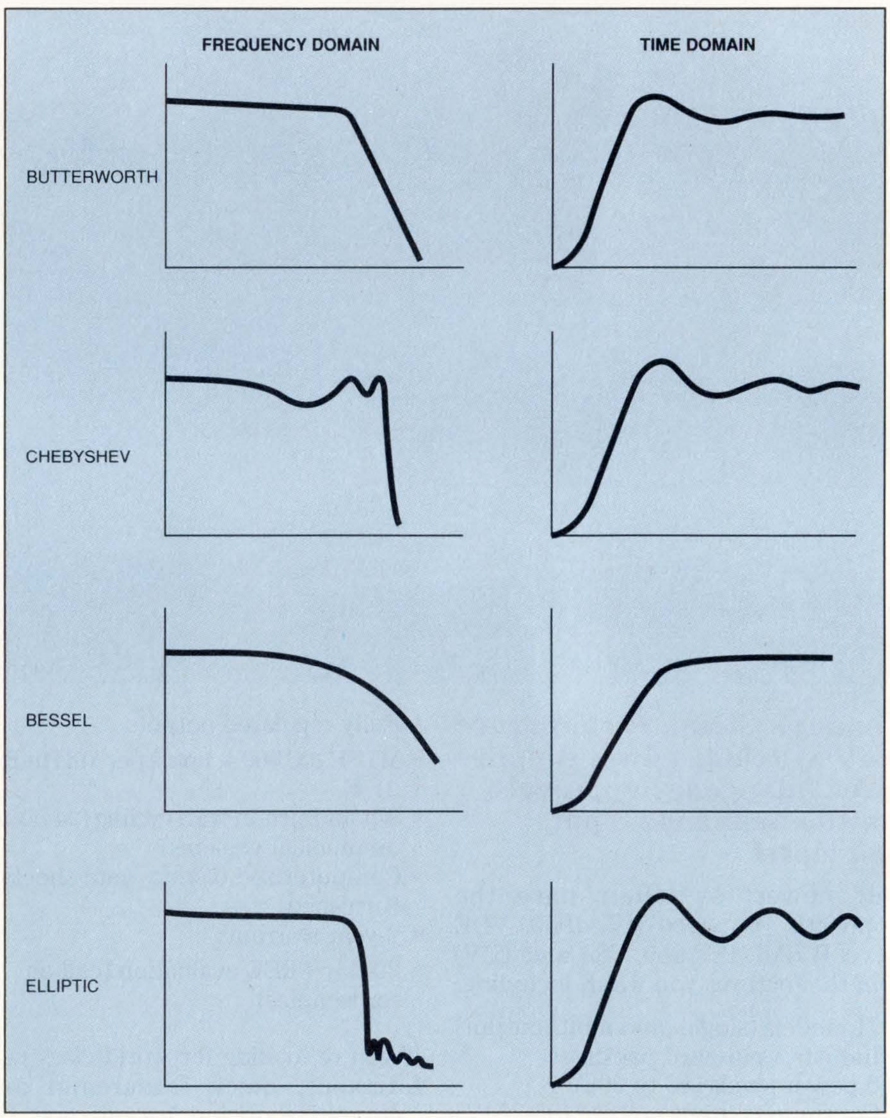

Fig 2—The classic filter-response types have pronounced differences in their frequency and time-domain characteristics.

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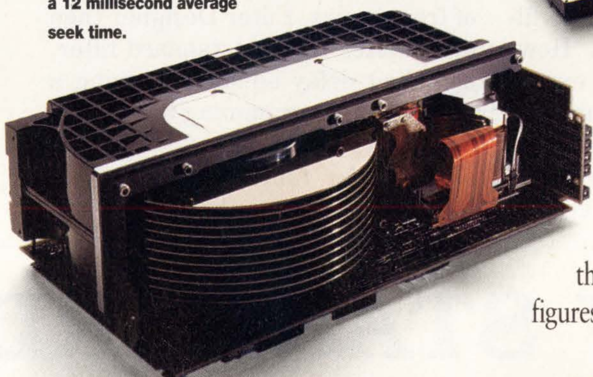

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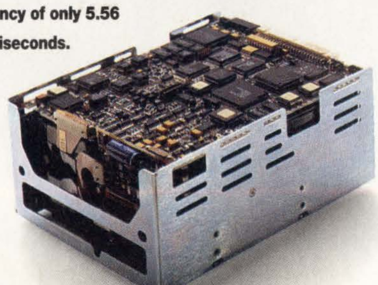

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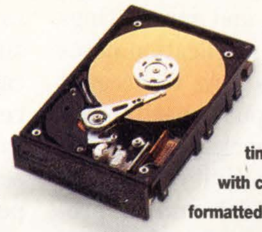

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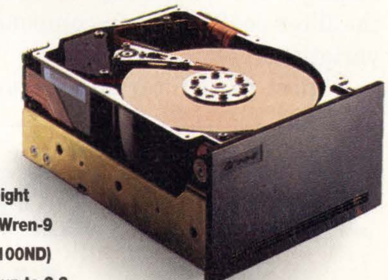

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The 3.5", half-height ST11200 family, with up to 1.2 gigabytes of storage, boasts a 256 kilobyte multi-segmented cache buffer and an average seek time of 10.5 milliseconds.

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tions. Burr-Brown's software screen provides basic but useful tutorial information as you make your filter selections. Calculations are done automatically as you change parameters. The accompanying application notes provide useful information on how to choose op amps based on the designed filter's Qs, center frequencies, and gain settings of each stage. The application notes also instruct users how to account for an op amp's input capacitance.

Many of these packages perform some sort of sensitivity analysis. Burr-Brown's Filter1 and '2 programs display sensitivity of natural frequency and Q to component-value changes in 1% increments. Filter Designer's sensitivity menu displays the sensitivity of each of the filter coefficients to components variations.

A first-pass filter design using any of these packages takes only minutes. But in many cases, you'll want to optimize your design. Maxim's software and Microsim's Filter Designer both provide for gain optimization of continuous-time filters. They let you reorder stages and adjust gain setting to maximize the filter's dynamic range. Plots of the output of each successive cascaded-filter section can reveal excessive peaking that results in clipping and reduced range. Adjusting stages and gain settings can reduce the unwanted peaking.

Such reordering and gain optimization doesn't change the basic filter coefficients themselves. However, two programs will let expert designers either fine-tune their designs by modifying coefficients or design custom filters from scratch.

Linear Technology's FilterCAD has a custom feature to help create filters that don't fit any of the classical response types. This custom feature either lets you modify previously designed filters or create filters with custom responses from scratch. By alternately graphing the resulting response and modifying frequency and Q values, you can iteratively arrive at almost any kind of response.

The advanced version of Microsim's Filter Designer also has a nonstandard functions menu. You define the nonstandard function by specifying minimum and maximum transfer-function limits at a number of frequencies. Filter Designer then synthesizes this nonstandard filter, including delay equalizers, using a nonlinear programming numerical optimizer. In minutes, you can create transfer functions that might take weeks manually because no

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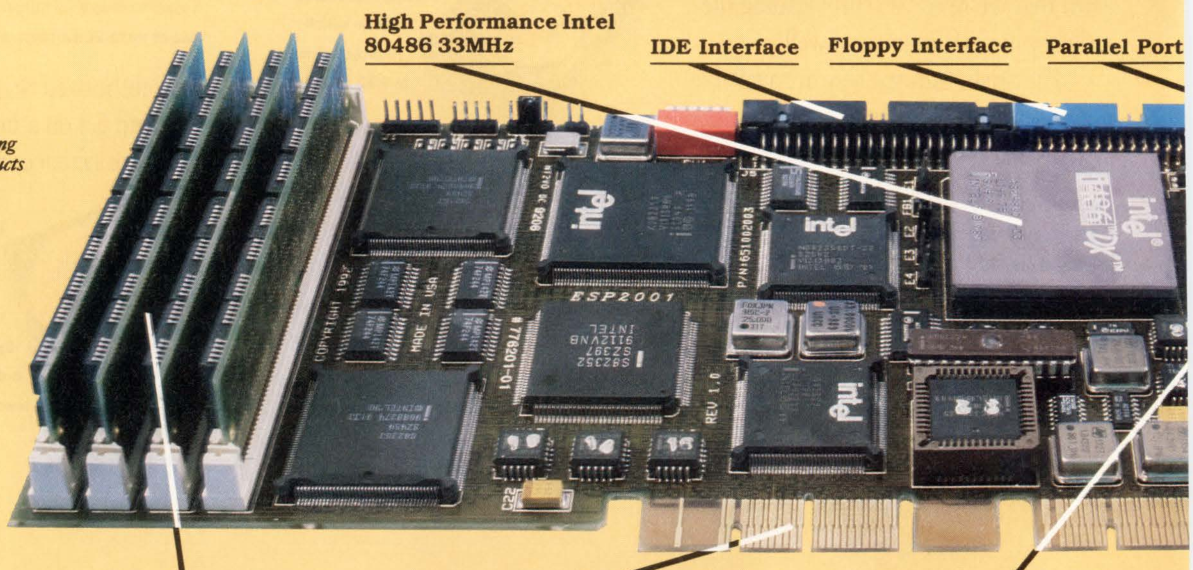

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systematic derivation theory exists.

The numerical optimizer sets Filter Designer apart from the IC vendors' software packages. Also, the IC vendors' packages are less comprehensive—they include fewer topologies and options. So, if you have a variety of filter-design requirements, spending the money on a comprehensive filter-design package may be well worth it. If you just need a good tool for designing specific classical active filters—either continuous-time or switched-capacitor—the IC vendors' packages are a tremendous bargain. EDN

For more information . . .

For more information on the filter-design software discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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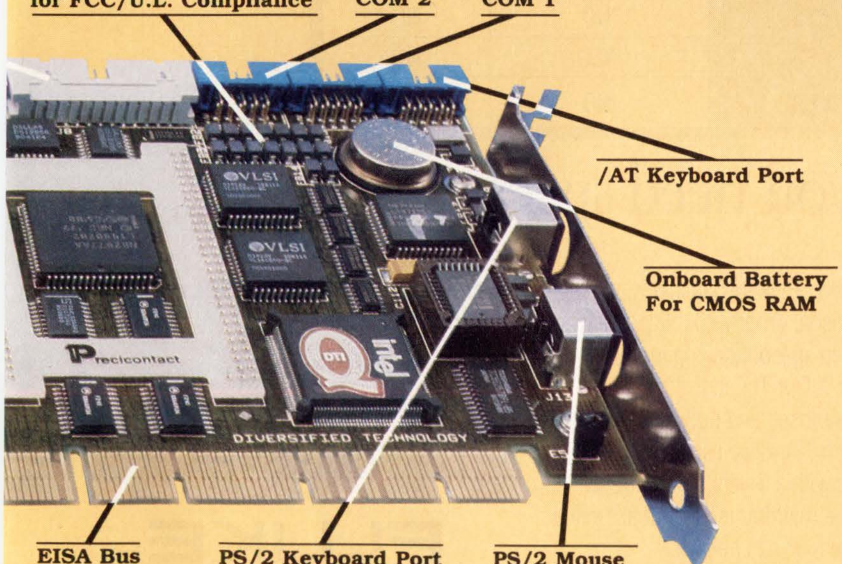

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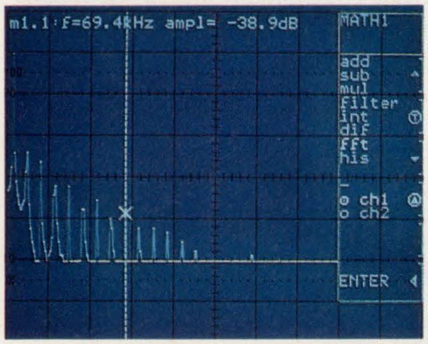

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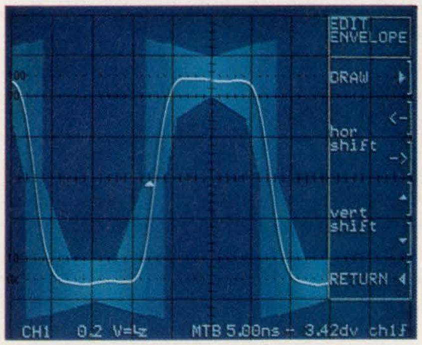

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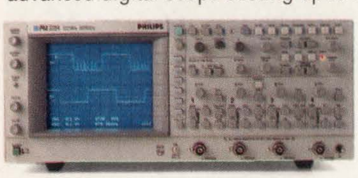

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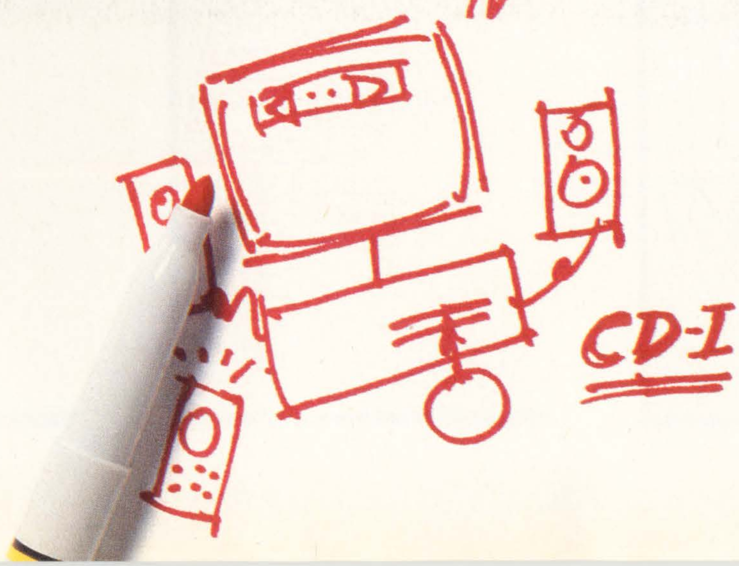

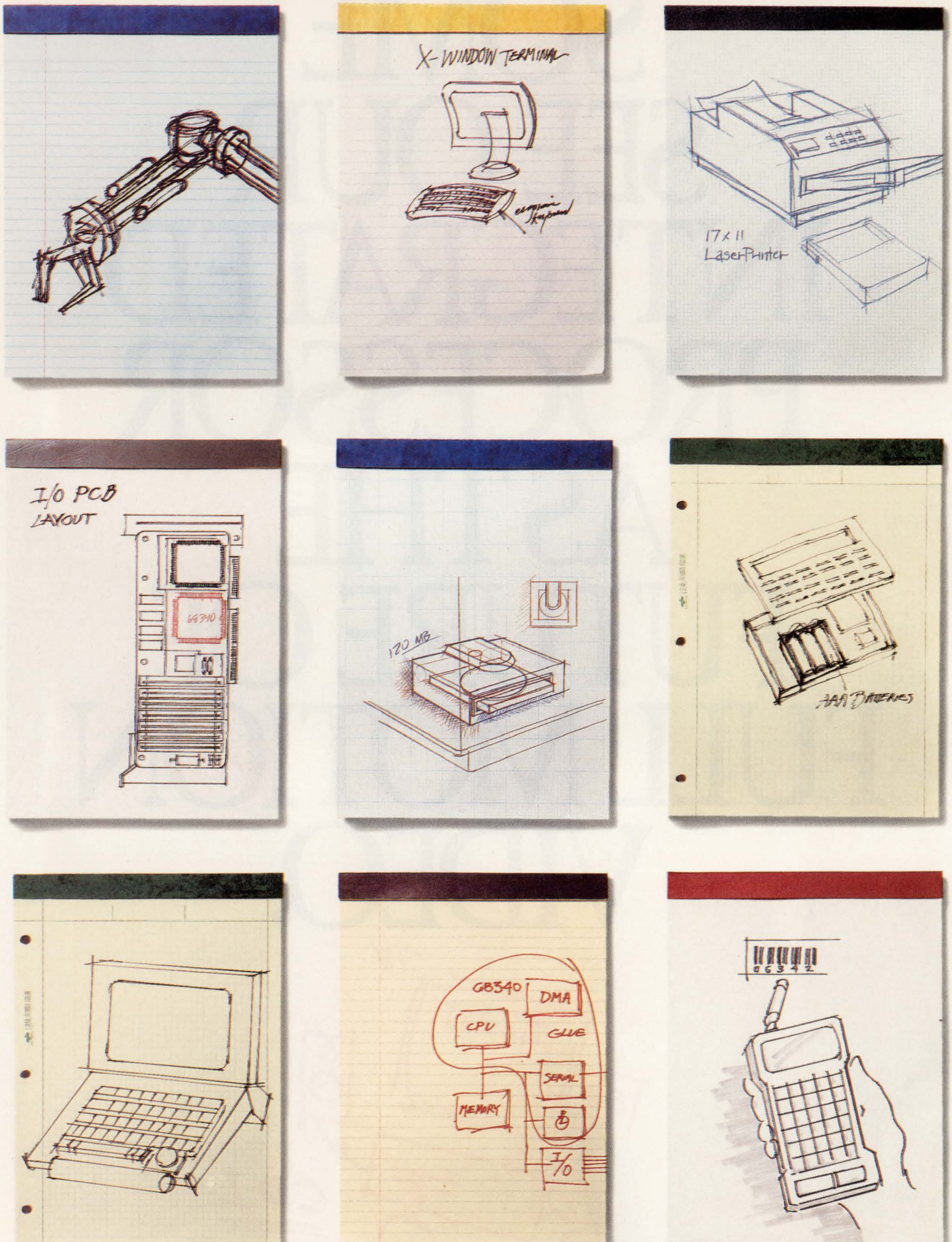
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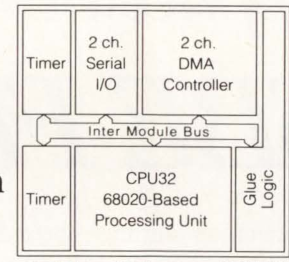

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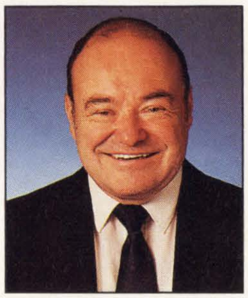
CONTENT-ADDRESSABLE MEMORIES

FDDI routers and bridges create niche for memories

JOHN GALLANT, Technical Editor



Content-addressable memories (CAMs) quickly compare input data to stored data. FDDI's 100-Mbps speed has created a commercial demand for these memories, whose steep prices had confined them to supercomputers and research projects.

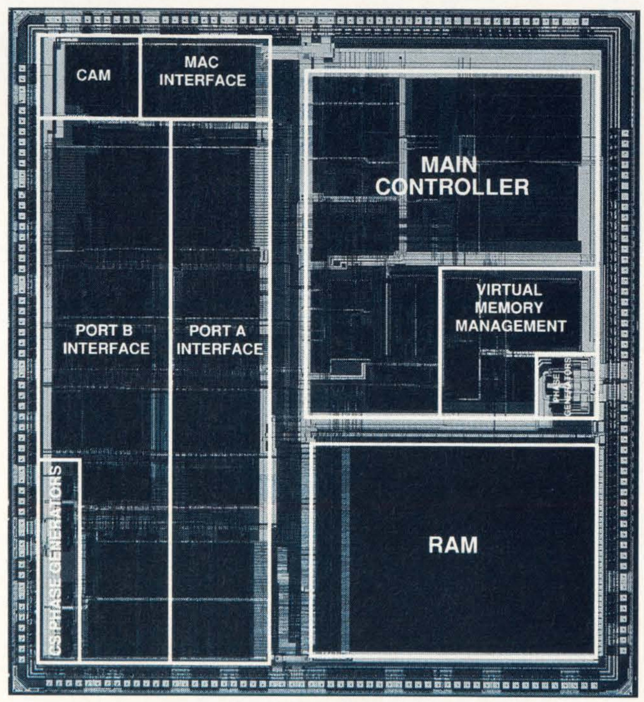
The Von Neumann computer architecture has conditioned most of us to envision a memory device as a collection of data you index via an address. This presumption is natural because most of today's computers access all instruction sequences, constants, and data in exactly this manner. However, high-speed data comparison—such as the address filtering an FDDI bridge or router does—requires a memory device that indicates its contents based on a data set rather than an address. A content-addressable memory (CAM) is best suited for this task.

In fact, almost from the creation of digital computers, designers have needed a device that could quickly determine whether a particular data value matches a stored data value. If a match occurs, the logic needs to know the address where the data is stored and the value of any conditional-branch pointers stored with the data. If the database is large, finding the data using search-and-sort software routines can be like looking for a needle in a haystack.

The generic CAM architecture has a comparator for each array location. When an input data word matches a stored data word, "Bingo," the comparator issues a hit command and reports all the data stored at that location and its address. If multiple matches occur, a priority encoder establishes the output data sequence.

Because they have multiple comparators, CAMs are inherently expensive devices. Thus far, defining a CAM architecture that would suit a range of applications has not produced cost-competitive products. So designers have often compromised speed for cost by instead using a static or dynamic RAM along with search logic and a single comparator for data comparison. In fact, the most cost-effective way to do data comparison is to sort the data in software using hashing algorithms.

In LANs, bridges and routers, which connect multiple networks via the data-link and network layers of the OSI model, must quickly filter many destination addresses before forwarding a



Because LAN address-filtering applications currently provide the widest market opportunity, it seems natural to incorporate a CAM into a LAN chip set. The MC68839 chip in Motorola's FDDI 4-chip set includes a 32 × 48-bit CAM array.

matched address to another attached network. CPU speeds have been fast enough to do this address filtering via hashing algorithms at 10-Mbps Ethernet and 16-Mbps Token Ring speeds. But FDDI (Fiber Distributed Data Interface) networks chug along at 100 Mbps, and only CAMs can handle address filtering at that speed.

An FDDI bridge must identify a message's destination or source address in a fraction of the message time interval. The destination or source address field in the FDDI message format is a minimum of 2 bytes (16 bits) or a maximum of 6 bytes (48 bits). A minimum of 4 bytes must be in the message's data field. For a message of minimum length, a bridge must identify a message's source address in less than 800 nsec before receiving another message **(Fig 1)**. Commercially available CAMs can identify addresses in less than 200 nsec.

Other applications that could benefit from the speed of CAMs include parallel computing architectures, which compare computational results with destination information to determine the data flow to other processing elements. An-

Fully associative memory uses off-the-shelf parts

Designers have searched long and hard for an economical content-addressable or fully associative memory device that would quickly determine whether a piece of data resides in main memory. So far, the high cost associated with such memory devices has limited their use to supercomputers; most other computers employ lower-cost set-associative memory products. Now, a patent-pending fully associative memory that uses off-the-shelf components may make these memories affordable enough for the masses. The device is called the data-addressable memory (DAM).

The DAM employs three standard RAMs for each set of data **(Fig A)**. While the DAM is storing data, a log (for log book) RAM stores the data in the standard fashion by using sequential input addresses to point to successive data locations. In parallel with the log RAM, a twist RAM reverses the roles of the input address and data words. In the data-addressable twist RAM, the input data stores the log RAM's address word. When identical data occur at different addresses in the storing sequence, the second address overwrites the previous address in the twist RAM.

To recover overwritten addresses, a linked-list RAM stores the sequence of previous addresses stored in the twist RAM. Before identical data stores a new address word into the twist RAM, the DAM stores the previous twist-RAM address into a linked-list RAM. The new address in the twist RAM points to the location in the linked-list RAM where the previous address is stored. Because the DAM uses addresses to find data in the log RAM and addresses in the linked-list RAM, the words in both these RAMs can never be overwritten. Although the linked-list RAM may contain many identical address sequences, all of the sequences have unique locations.

To read the data, the DAM circuitry employs an

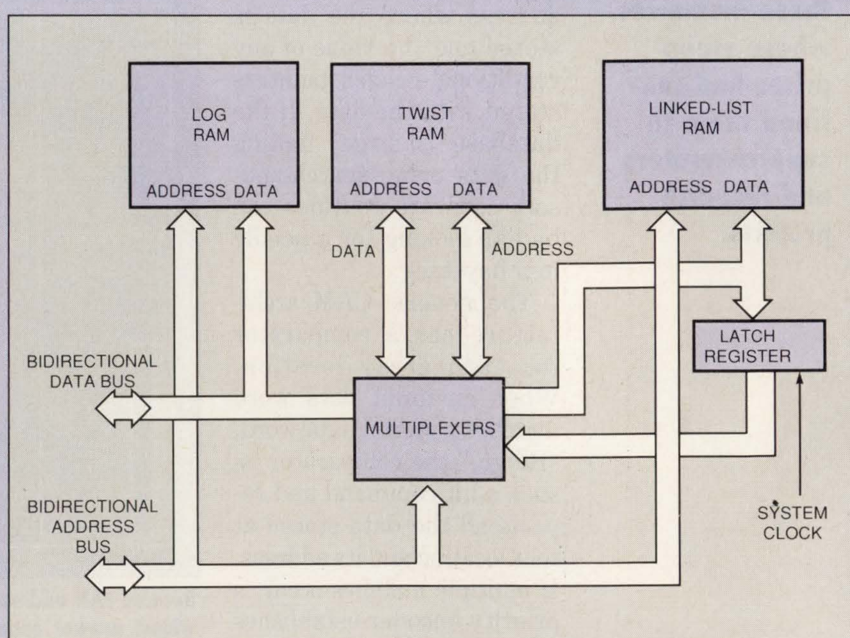


Fig A—The patent-pending DAM employs three standard RAMs—a log RAM, twist RAM, and linked-list RAM. A register reads out the stored address sequence in the linked-list RAM in reverse order. You can increase the DAM array by adding groups of three RAMs.

other application is voice and pattern recognition in which an algorithm compares input data to stored templates in an array.

Speeding up the search for data in a relational database or a fully associative cache is another application that could benefit from CAMs. In fact, translation look-aside buffers (TLBs) are actually special-purpose CAMs for virtual memory systems. In virtual memory systems, a TLB quickly checks a virtual address issued by a CPU against addresses in a look-up table to see whether a physical address resides in local RAM.

Commercially available CAMs are still few and far between. Most vendors of specialty memories have found the volume demand for CAMs to be so low that it isn't worth the investment cost, according to Micron Technologies' (Boise, ID) Gene Cloud, vice president of semiconductor marketing. Currently, the only commercial application that has started actively using CAMs is bridges in FDDI LANs. As these high-speed LANs proliferate, they could fuel the demand for CAMs in other applications and possibly drive down prices.

external register that latches the output address words from the linked-list RAM using the system clock. To query the DAM, you direct a specific data word to the twist RAM to see if a stored address matches. If the twist RAM doesn't contain an address word for the specified data, a 0 address word appears on the address bus via the multiplexer. A 0 address on the address bus indicates a miss. If the twist RAM does contain an address word, the address on the address bus points to a location in the log RAM where the data resides and to a location in the linked-list RAM to see if that RAM has a previous address for the data.

If the linked-list RAM doesn't contain a previous address, the next system clock latches a 0 address word from the linked-list RAM into the external register. A latched 0 address word indicates that the log RAM contains no additional copies of the data. If the linked-list RAM does contain a previous address, the next system clock latches the stored address from the linked-list RAM into the register.

The control circuitry multiplexes the stored address onto the address bus, which points to the location in the log RAM where duplicate data resides and also to the location in the linked-list RAM where the next previous address in the sequence resides. Each succeeding clock latches the address word from the linked-list RAM into the register until a 0 address word appears. The 0 address word indicates that all previous locations have been identified.

In the conceptual block diagram in **Fig A,** the DAM reads the sequence of data in reverse order from which the data were stored in the log RAM. In a variation of the DAM, the device reads data in order. You can stack multiple log, twist, and linked-list RAMs in parallel to address multiple sets of data. The bidirectional data and address buses connect to the RAMs for all the other data sets to retrieve associated data from their respective log RAMs. Reading the contents at specific data values in one or more sets will identify all associated data in the other DAM sets. For example, consider that the DAM contains the following data for three parallel sets P, Q, and R:

Address	Set P	Set Q	Set R
1	7	2	1
2	5	3	5
3	8	2	9
4	9	7	4
5	5	2	4
6	2	3	3
7	3	2	7
8	2	7	5

A query for identifying all data values in the other sets that belong to a value of 3 in set P, 2 in set Q, or 5 in set R produces the following output sequences:

Sequence of data belonging to P=3:

Address	Set P	Set Q	Set R
7	3	2	7
	0	0	0

Sequence of data belonging to Q=2:

Address	Set P	Set Q	Set R
7	3	2	7
5	5	2	4
3	8	2	8
1	7	2	1
	0	0	0

Sequence of data belonging to R=5:

Address	Set P	Set Q	Set R
8	2	7	5
2	5	3	5
	0	0	0

For further information contact Larry Dillard, Box 18238, Boulder, CO 80308. Phone (303) 494-8244.

CONTENT-ADDRESSABLE MEMORIES

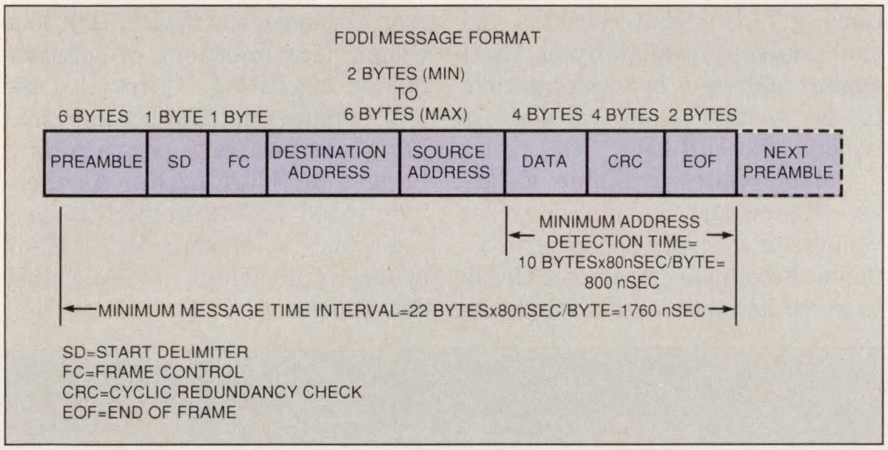


Fig 1—The CAM is the only practical device for filtering destination or source addresses in the FDDI message format. The worst-case minimum address-detection time is 800 nsec. CAMs can do the job in 200 nsec or less.

Testing the waters of the LAN bridge market, Advanced Micro Devices (AMD) introduced the first commercially available, single-chip CAM in late 1988—the 12-kbit CMOS Am99C10. The two chip versions have 100- and 70-nsec read/write cycle times, and each costs $21 (100). The chip suits LAN bridges and routers that filter addresses as fast as 200 Mbps. The chip's architecture also suits it for LAN group addressing. In group addressing, a sender transmits a message to every member of a group that belongs to associative sets of data in a look-up table.

The Am99C10 CAM holds 256 words, each consisting of a 48-bit register and a 48-bit comparator (**Fig 2**). You transfer data to and from the CAM via a 16-bit bidirectional bus. An internal 2-bit segment counter loads 48-bit data into an internal comparand register 16 bits at a time.

After the counter loads the 48-bit data into the comparand register, all comparators simultaneously check the comparand data with their associated storage-register data within one clock cycle. If a match occurs, the CAM activates an external $\overline{\text{MTCH}}$ signal, and a priority encoder generates an 8-bit match-word address. This address appears in a 16-bit status register to identify the location of the data in the CAM.

If multiple matches occur, the CAM activates a bit in the status register, and the priority-encoder generates the lowest match-word address. A mask register lets you selectively mask any of the bits in the comparand register before data comparison. You can also selectively mask the bits in the storage registers before data comparison.

Each of the 256 words in the CAM has two associated data bits: a skip bit and an empty bit. The actual width of the array locations is therefore 50 bits (48+2). Both the skip and empty bits can keep their words from being compared with the input data. The skip bit lets you detect words other than the highest-priority word. The empty bit indicates an empty slot in the array.

You can program the Am99C10 to read and write to any of its storage registers. Each CAM register can contain data or be empty so that the register doesn't participate in a comparison. You can set all of the array contents to empty in a single

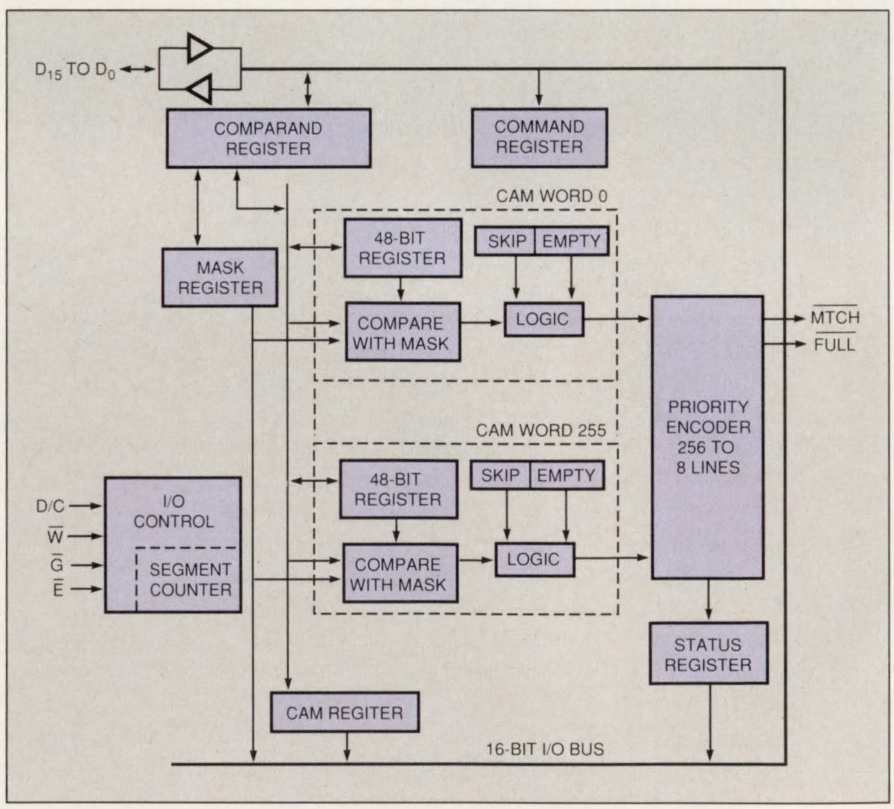


Fig 2—The first commercially available CAM was Advanced Micro Devices' Am99C10. The chip simultaneously matches input data to stored data in a 256 × 48-bit array using separate comparators for each stored word.

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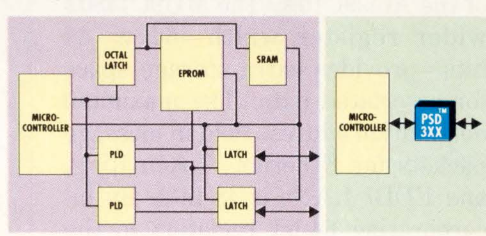

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CONTENT-ADDRESSABLE MEMORIES

clock cycle. The CAM activates an external $\overline{\text{FULL}}$ signal when all locations in the array are full.

You can expand the capacity of a CAM array by connecting multiple Am99C10A chips in parallel. The largest possible CAM array is 64k×48 bits and consists of 256 chips. To extend the capacity of the CAM array you also need external PALs to decode the $\overline{\text{MTCH}}$ and $\overline{\text{FULL}}$ signals from the multiple Am99C10A chips.

The newcomer on the block

The only other commercially available, single-chip CAM is the MU9C1480 from Music Semiconductors. (The part sells for $65 in a 28-pin DIP and $60 (1000) in a 44-pin plastic leaded chip carrier.) After recognizing some limitations to the Am99C10, the company introduced the MU9C1480 in June 1991. The chip essentially is an enhanced version of the Am99C10 architecture and is also aimed at address-filtering applications in LAN bridges and routers. GEC Plessey Semiconductors is a second source for the part.

The MU9C1480's array is 1k×64 bits, which is four times the density of the Am99C10A. The MU9C1480's wider register width—64 vs 48 bits—provides extra storage space for associated data. The maximum destination address field in message packets for Ethernet, Token Ring, and FDDI LANs is 48 bits. By incorporating 64-bit registers in the array, the MU9C1480 can append 16 bits of associated data to each stored address.

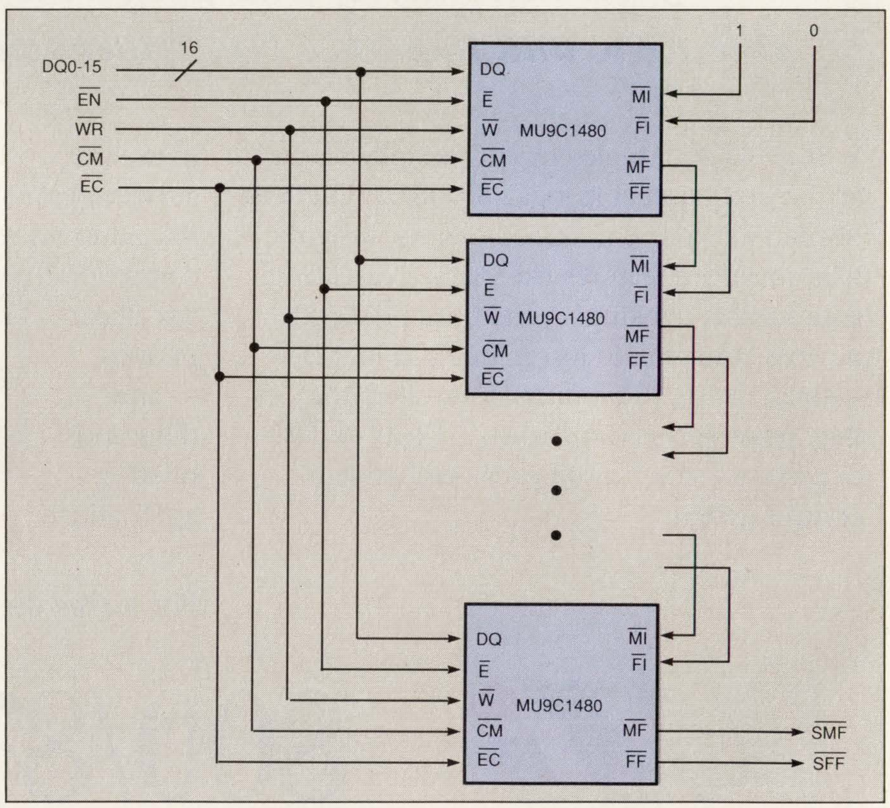
The 16-bit associated-data field can store bits for algorithms that purge node addresses that have not been active within a certain elapsed time interval. The field also lets you append a port address to the node address. And you can perform data comparisons on masked bits in the field.

The MU9C1480 comes in versions having 120- and 150-nsec read/write cycle times. You transfer data to and from the chip via a 16-bit bidirectional bus. An on-chip 1-to-4-line multiplexer directs the data to an internal 64-bit bus, which feeds the comparand register and the CAM array. The chip has dual 64-bit mask registers, which let you mask bits for both data writes and compares. When multiple matches occur, a priority encoder generates the highest priority 10-bit address. The address appears in a 16-bit status register.

The MU9C1480 has several features that simplify address filtering. These features include programmable translation between Ethernet and Token Ring address formats; an associative writing mode that expedites the storing of data by automatically writing to the next free address; and an up-down address counter that speeds memory writes and reads using DMA. The chip can also partition the 64-bit words into 16-bit sections, which the chip can allocate as CAM or RAM.

Perhaps the most attractive feature of the MU9C1480 is the straightforward way you can connect multiple chips in parallel to expand a CAM array. The chip doesn't require extensive external logic to decode the match and full lines, as AMD's Am99C10 does. Instead, the MU9C1480 has two input lines, a match input and a full input, that connect to the match-output and full-output signals of its parallel neighbor. This arrangement lets you cascade an unlimited number of MU9C1480s in a daisy-chain manner that is similar to chip expansion for FIFO memories.

The most widespread use of commercial CAM devices is for filtering addresses in high-speed LANs, so some LAN-interface-chip vendors



You can cascade an unlimited number of Music Semiconductor's MU9C1480 chips to expand a CAM array. The chip contains a match-input and a match-full line that directly connect to the match-output and full-output lines of its neighbor.

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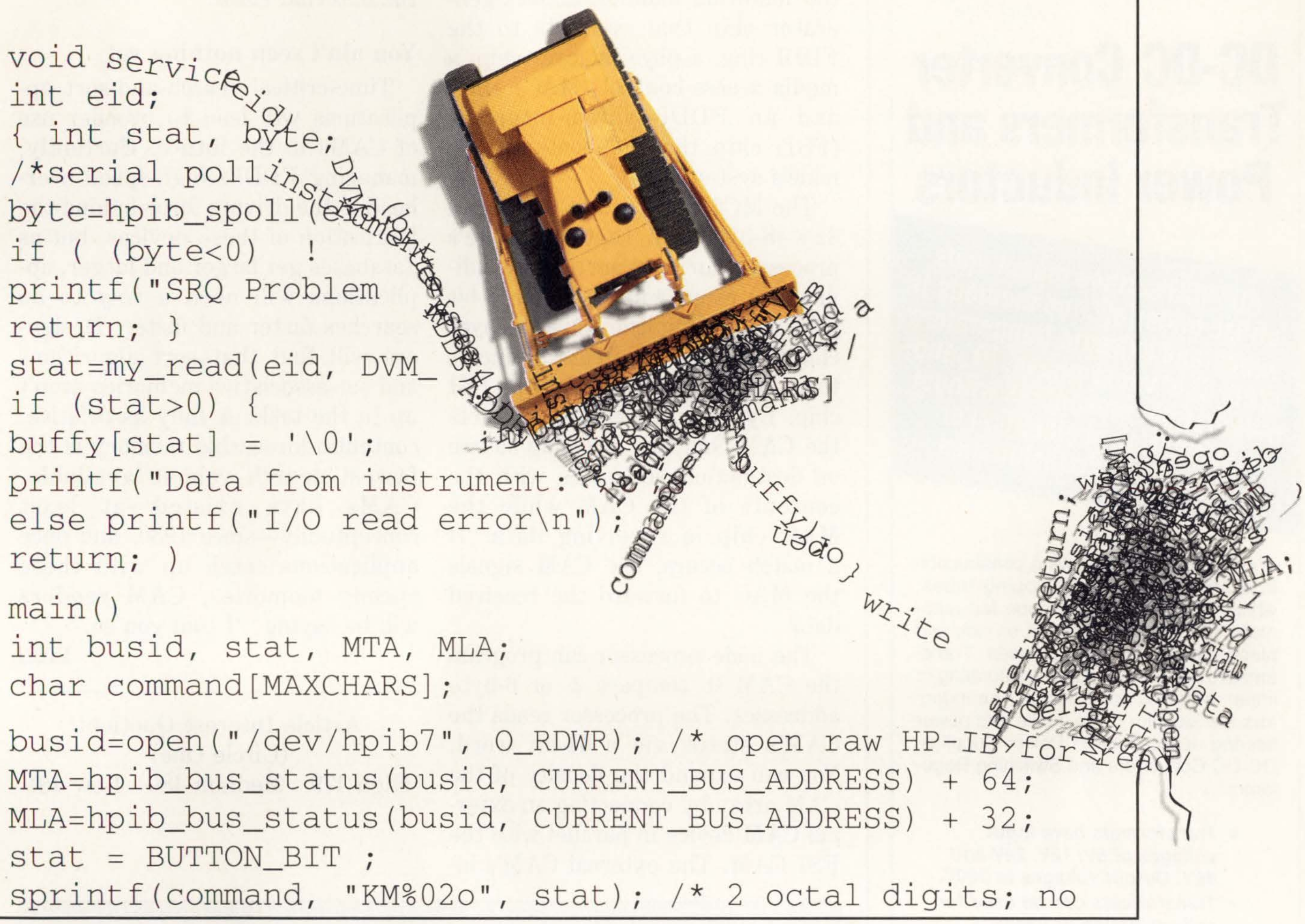

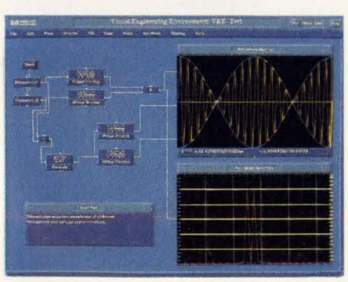

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CIRCLE NO. 38

CONTENT-ADDRESSABLE MEMORIES

are including a CAM in their chip sets. Motorola has included a CAM—albeit a small one—in its FDDI chip set. The $186 (1000) set comprises four chips connected in the following manner: a clock-generator chip that connects to the FDDI ring, a physical-layer chip, a media-access-control (MAC) chip, and an FDDI-system-interface (FSI) chip that connects to the node's system bus.

The MC6889 FSI chip contains a 32×48-bit CAM that the node's processor can program to store individual or group addresses. The 8-bit port connecting the physical-layer chip to the MAC chip also connects to a CAM-interface port on the FSI chip. Bypassing the MAC chip lets the CAM compare incoming source or destination addresses with the contents of the CAM while the MAC chip is receiving data. If a match occurs, the CAM signals the MAC to forward the received data.

The node processor can program the CAM to compare 2- or 6-byte addresses. The processor reads the CAM's status via a 64-bit word. You can expand the density of the CAM array by connecting an external CAM device in parallel with the FSI CAM. The external CAM's input port connects directly to the FSI chip's CAM-interface port. The 64-bit word has a user-defined bit you can use to signify whether a match occurs in the FSI CAM or the external CAM.

You ain't seen nothing yet

Time-critical search-and-sort applications will lead to broader use of CAMs in the future. Currently, managing FDDI's high-speed overhead is the driving force behind the fabrication of these devices, but as databases get larger and larger, applications will need a way to do searches faster and faster. Designers will find that sort algorithms and set-associative memories aren't up to the task. A fully associative, content-addressable memory is the fastest search vehicle available. CAMs have existed—at least conceptually—since 1950, and once applications catch up with these speedy memories, CAM vendors will be saying, "I told you so." EDN

Article Interest Quotient
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For more information . . .

For more information on the content-addressable-memory products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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Motorola Inc
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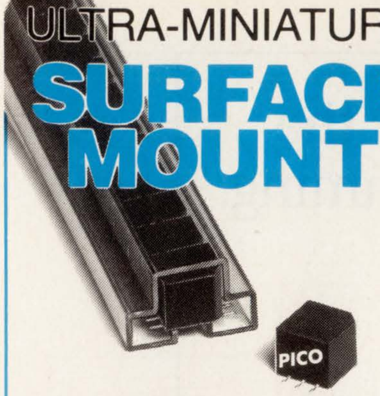

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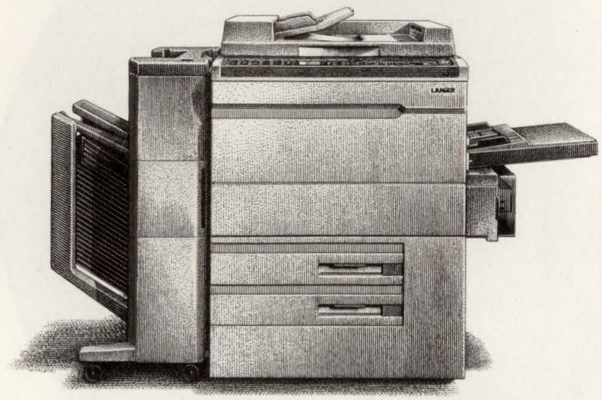

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CIRCLE NO. 42

High-density PLD offers speed and in-system programmability

The PLSI 1032 and ISPLSI 1032 are the first two members of a high-density programmable-logic-device (PLD) family based on electrically erasable CMOS. The base technology allows the ISPLSI device to be in-system programmable.

The basic logical unit of the devices is a logic block, offering 20 product terms. The terms can use the true and complemented forms of as many as 16 internally generated signals and have access to two additional signals from dedicated I/O pins.

Each logic block has two 4-, one 5-, and one 7-input OR circuits. You can combine the output signals of these OR circuits if you need additional width or bypass the combinatorial circuitry if you need top speed with only a few terms. You can also Exclusive-OR the OR output signal with one of the product terms.

The four output signals from the logic block either pass through or bypass output registers. The registers are configurable as D-, JK-, or T-type registers with a choice of four clocks and two reset signals. Three of the clocks and one reset signal are common to all the logic blocks; the remaining signals are product terms from the block. The devices offer one register for each OR gate, but the registers are not dedicated to the gates.

Although all logic-block output signals are available internally to the product terms, signals destined for the outside world must pass through an output routing pool before reaching I/O cells. The devices group eight logic blocks together on each device edge, with each group having its own output routing pool and 16 I/O cells.

The routing pool gives you flexibility in I/O pin selection. Each of the 32 logic-block output signals in the group has a choice of four I/O cells. As with the combinatorial circuitry in the logic blocks, you can bypass the routing pool for greater speed but no choice in I/O pin.

You can configure the I/O cells as input ports, output ports, or bidirectional ports, with each port type offering options. Input ports can simply buffer signals, latch them, or register them. Output ports can buffer signals, either with or without inverting them. They can also provide 3-state buffers, with the enable signal coming from a product term. Bidirectional ports can simply buffer, or buffer the output signal while registering the input signal.

If you use all the bypass options, a signal can propagate through either device in 15 nsec. Because of the wide combinatorial terms available, your design may not need to use feedback. If it does, however, the feedback term can add from 9 to 16 nsec, depending on fanout of the term internally.

The device family comes in two nearly identical forms. The ISPLSI device, however, has an additional attribute. Four of the device's I/O pins serve double duty as programming pins, allowing you to clock in and load a serial programming pattern while the device is in a system. This in-system programmability lets you build your system, even your prototype, without sockets for the PLD, thus decreasing noise and increasing system speed.

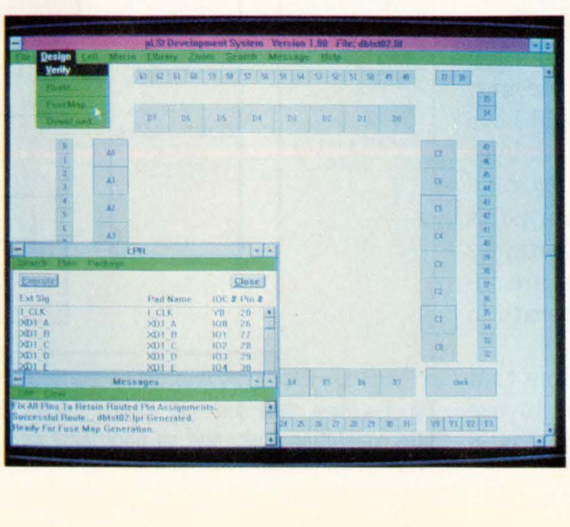
The company supports its devices with an array of programming tools. The basic software runs on a DOS-based computer under Windows and allows schematic and Boolean design entry. It comes with a library of 240 macro functions that include most common TTL functions. You can also edit these macros or create your own. If you already have a design entry system, the software can serve as back-end, place-and-route software. The company also offers an engineering kit for the ISPLSI device.

The PLSI 1032 ranges from $49 to $81 (1000). The ISPLSI device costs $142 (100). Software costs $995, and the engineering kit is $395. The devices come in 84-pin plastic-leaded-chip-carrier packages.

—Richard A Quinnell

Lattice Semiconductor Corp, 5555 NE Moore Ct, Hillsboro, OR 97124. Phone (503) 681-0118. FAX (503) 681-0347. TLX 277338.

Circle No. 732



The PLSI and ISPLSI programmable logic devices offer combinatorial logic blocks with flexible I/O pin mapping. They are supported by Windows-based design, place, and routing software.

Cache tag RAMs offer 12-nsec validated match with extras

The CY7B180 and CY7B181 cache tag RAMs not only offer 4k × 16-bit tag memory, they include functions such as chip-select decoding and the logic needed for validating matches. They also include two status bits for each memory location and an additional data port to speed copy-back cache designs.

The devices' base structure is 4k × 18 bits. Each word location stores a 16-bit tag and two status bits. You use the devices for storing the lower-order address bits for the memory you have copied into cache. When the processor addresses a memory location, the tag RAMs respond with a match signal within 12 nsec if that address has been cached.

Several built-in functions can simplify your cache design. You can read from and write to the tag data and status bits independently. This operation allows you to update status without having to do a read-modify-write on a combined tag and status word. Another function allows automatic generation of a write output signal to the cache RAM when the tag RAMs detect a valid write hit.

A design-simplifying attribute comprises two separate ports: one for tag data and one for the address-match comparison data. The latter port provides the contents of a tag RAM whenever a match occurs. With a single port, you would have to multiplex address and data lines to the tag RAM in order to read back tag data. The separate ports eliminate that need. All ports, as well as the command lines, are internally latched and can operate in latch or clocked mode.

When replacing a cache line that has "dirty" data, you need to use the tag data to find the address in main memory that needs changing. Having that data available automatically when the tag RAM is addressed, rather than having to read it back through the match-comparison port, speeds the copy-back process.

The tag-RAM array (**Fig 1**) includes status bits for each tag location. The CY7B180, intended for use in a multiprocessing application, uses the two bits to code the corresponding tag data's status as modified, exclusive, shared, or invalid. The CY7B181, intended for use in a uniprocessing application, uses one status bit to represent whether or not the tag data is valid. It uses the other status bit to let you know whether the data is "dirty,"—that is, modified but not yet updated in main memory. The device automatically sets the "dirty" bit if it detects a write hit.

The 181's on-chip valid bit allows it to perform validated matches. When you present the address in question to the RAM, it will respond by indicating whether that location has been tagged and whether the tag is valid. You can clear individual valid bits in a memory cycle or clear all valid bits simultaneously in two memory cycles.

The devices have four chip-select lines—two low-true and two high-true. When the device is not selected, all of its outputs switch to high impedance. This combination of features allows you to cascade as many as four devices, forming a 16k-word RAM array, without suffering a speed penalty. Simply use the two most significant address bits to drive the appropriate chip selects and wire-OR the output signals.

The CY7B180 and CY7B181 come in 68-pin plastic leaded chip carriers and cost $72.05 (100).

—**Richard A Quinnell**

Cypress Semiconductor, 3901 N First St, San Jose, CA 95134. Phone (408) 943-2600. FAX (408) 943-2741. **Circle No. 730**

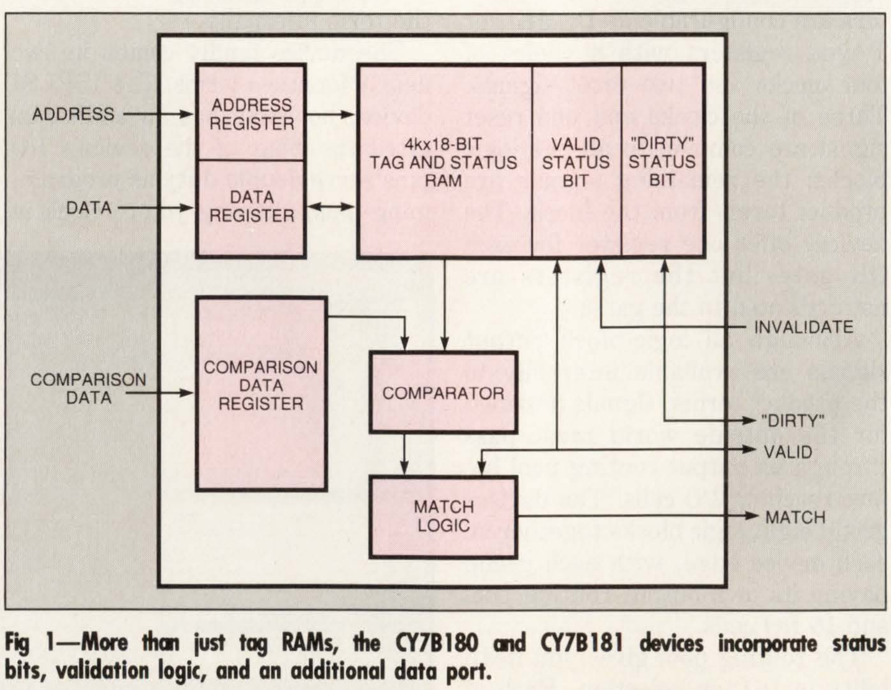


Fig 1—More than just tag RAMs, the CY7B180 and CY7B181 devices incorporate status bits, validation logic, and an additional data port.

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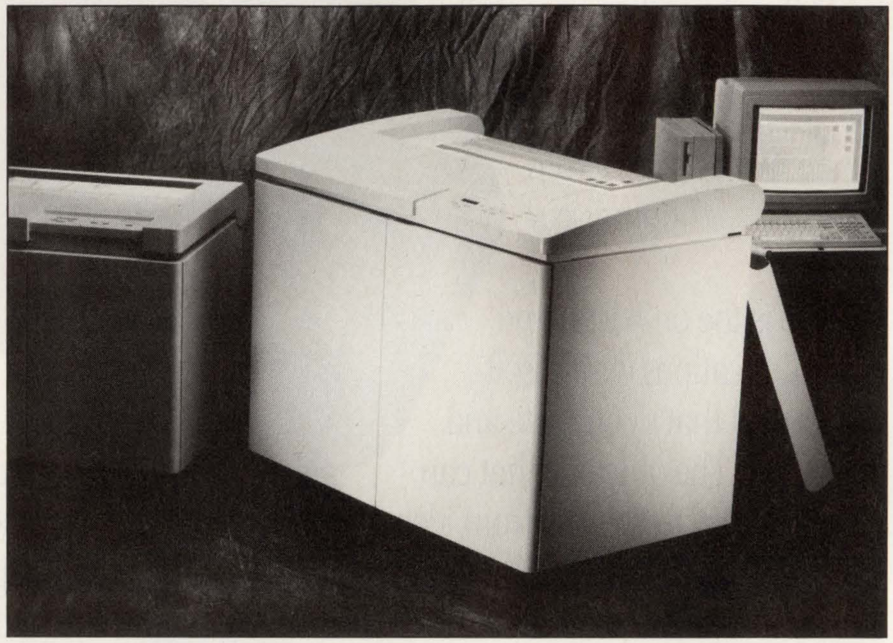
CIRCLE NO. 43

Electrostatic plotter makes E-size drawings at 6 ips

The Colorstation 400X family of electrostatic plotters produces color or monochrome, E-size (36×50-in. cut-sheet) or D-size (24×36-in. cut-sheet), drawings. The series consists of four models: the Colorstation 436CX for E-Size color drawings; the Colorstation 424CX for D-size color drawings; the Colorstation 436MX for E-Size monochrome drawings; and the 424MX for D-size monochrome drawings. The plotters boast a writing speed of 6 ips—considerably faster than competitive models that write between 0.8 and 2 ips.

The plotters achieve their high plot speed by employing a patented Silicon Imaging Bar writing head. Conventional electrostatic plotters employ a multiplexed writing head to transfer electrical charge to the media. A multiplexer transfers charge from a common source to multiple nibs. The Silicon Imaging Bar writing head consists of a dedicated driver for each nib. Because a multiplexed driver necessitates a time delay before applying charge to subsequent nibs, it is slower than these dedicated drivers.

In addition, the Colorstation Series can accurately register the location of dithered color dots. Conventional electrostatic plotters employ a multipass reel-to-reel media-transport system, which rewinds on each pass to deposit the four primary colors. On the first pass, reel-to-reel systems place registration marks on the edge of the media to provide servo information for subsequent passes. However, during the toning process, any paper stretching can distort this registered information.



Providing switch-selectable 200- or 400-dpi resolution, the Colorstation 400X Series color and monochrome electrostatic plotters produce plots at 6 ips.

The Colorstation Series locks the cut-sheet media onto a belt using a vacuum. Registration marks are fixed on the vacuum-locked belt, which rotates past the nibs on each color pass. Because the media cannot shift or stretch while locked to the belt, the vacuum-locked system ensures registration from one color application to the next. The Colorstation series has an overall plot-accuracy specification of 0.05%.

For a print controller, the Colorstation Series plotters employ an Intel 80960CA RISC μP that delivers 66 MIPS peak. The plotters also offer 200-dpi plots for quick drafts and 400-dpi plots for fine detail. You switch between modes with the press of a button. Competitive models offer only one of these resolutions. In 200-dpi mode, the 436CX can produce a full-color, E-size plot in less than 3 minutes.

A plot-nesting feature places A- through E-size drawings on a single sheet. For example, an E-size model can plot 16 A-size, 8 B-size, 4 C-size, 2 D-size, or a combination of these sizes on a single E-size sheet. A plot-tiling feature lets you plot large panels by automatically splitting a drawing into several images and plotting the im-

Table 1—Electrostatic plotter prices

	Hard-drive capacity		
Model	42 Mbytes	100 Mbytes	234 Mbytes
424MX	$22,895	$23,895	$24,895
424CX	$34,895	$35,895	$36,895
436MX	NA	$28,895	$29,895
436CX	NA	$44,895	$45,895

NA = Not available

XEROX

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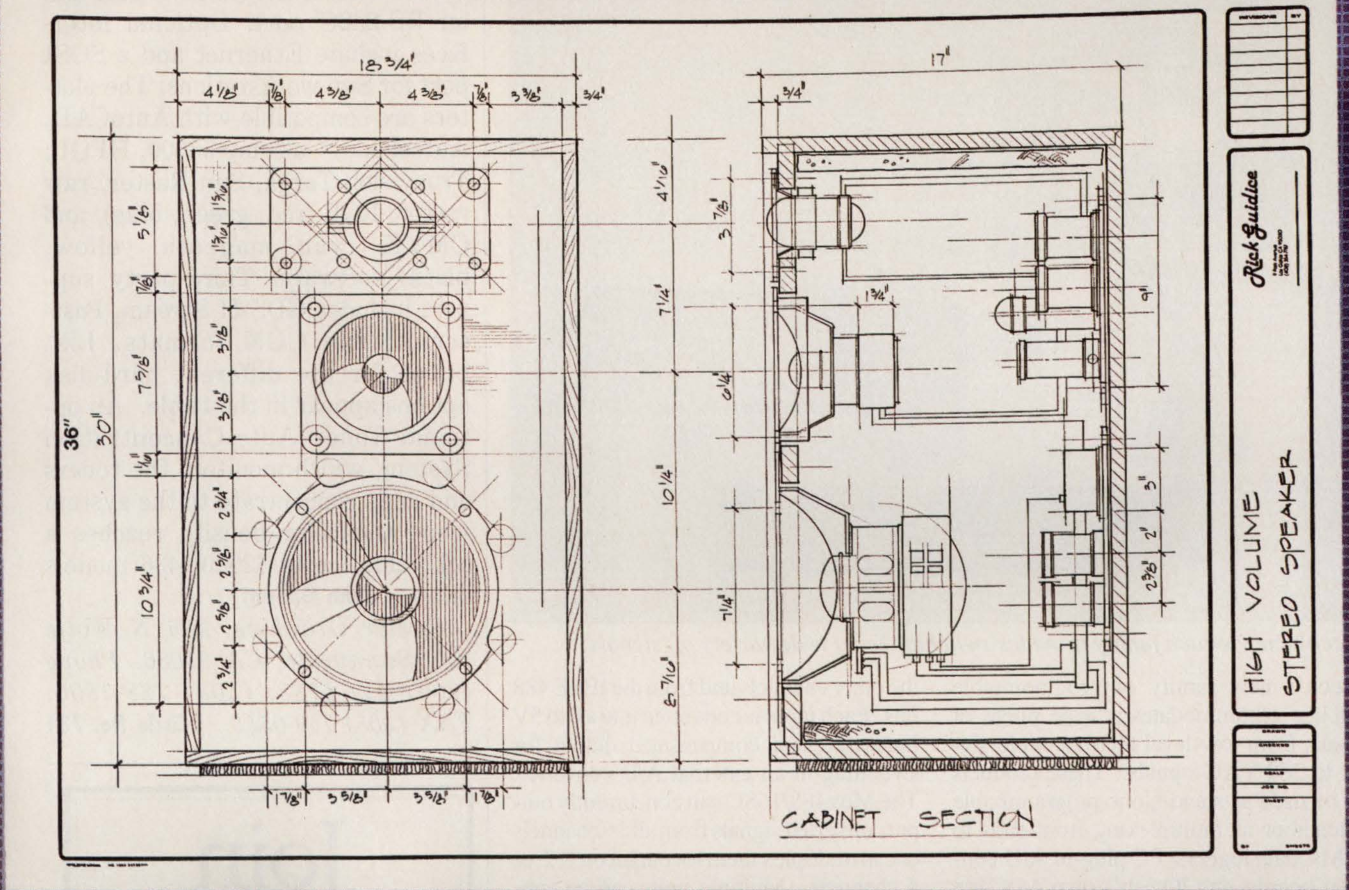

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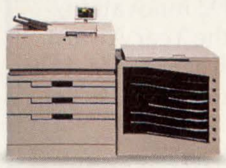
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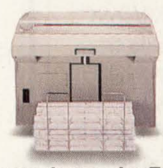
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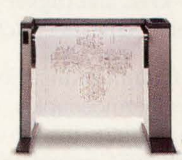
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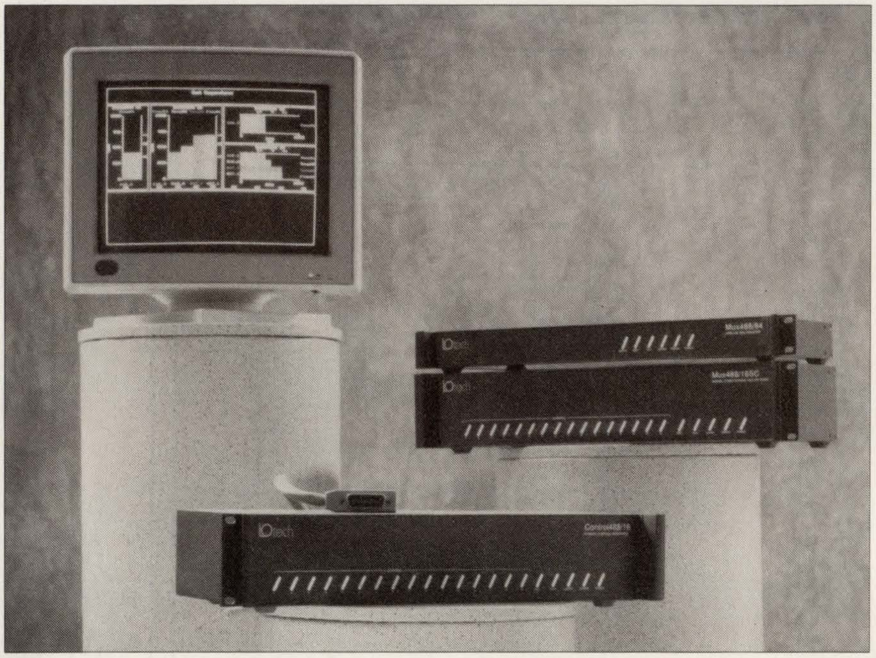
CIRCLE NO. 44

Advertisement

New Switch Family for IEEE 488, RS-232, and PC-based Systems



IOtech*'s new switch family provides switching for a wide variety of signals*

IOtech's new family of programmable switches accommodates a wide range of signals, from low-level thermocouple signals to 280 VAC signals. These products can be used as stand-alone programmable switches or as multiplexing front-ends to DVMs, data loggers, PC plug-in A/D converter boards, and IOtech's own ADC488 series of A/D converters.

These new switches offer three means of computer control, making them useful for a variety of applications. They are available with IEEE 488 and RS-232 interfaces, and with a parallel 8-bit digital interface for control directly from a PC's parallel port or from any digital I/O port.

High Channel Capacity. For applications that involve switching signals up to 10V, the **Mux488/64** can switch up to 64 inputs for output to an A/D converter. For applications requiring greater switching capacity, multiple units can be connected in a master-slave configuration, providing switching for as many as 1024 channels. The Mux488/64 also features a time-base and trigger source that enables it to automatically scan selected groups of signals at rates up to 4 kHz, and trigger an A/D converter after each signal is switched.

Signal Conditioning. For applications that involve thermocouples, RTDs, strain gages, or other low-level signals, the **Mux488/16SC** provides up to 16 input channels, each of which is isolated by 500V from the other channels and from the IEEE 488 bus. Each input is converted into a 0 to 5V linearized and compensated output for switching to an external A/D converter. The Mux488/16SC can concurrently output converted signals from all 16 channels or can multiplex them for output on 1, 2, or 4 channels. Multiple units can be connected in a master-slave configuration to switch as many as 256 channels. The Mux488/16SC offers a quick-disconnect, screw-terminal block that accepts transducer wires and provides cold-junction sensors for thermocouple measurements.

High Voltage Switching. For high-voltage or high-current switching applications, the **Control488/16** accommodates a wide range of user-configurable switches. Each of the Control488/16's switches is isolated by 500V from the other switches and from the IEEE 488 bus, and can accommodate DC and AC voltages up to 280V RMS, and DC and AC currents up to 3A. The Control488/16 provides two terminals for each switch and a convenient quick-disconnect, screw-terminal rear panel board with built-in strain relief.

Pricing. The Mux488/64, Mux488/16SC, and Control488/16 are all available from stock and are priced from $595 to $1,195. Transducer-conversion modules are extra. **For more information, call IOtech at (216) 439-4091, or fax your request to (216) 439-4093.**

CIRCLE NO. 45

EDN·PRODUCT UPDATE

ages on more than one sheet of paper.

The Colorstation Series plotters have a Centronics parallel port and an RS-232C port. Optional interfaces include Ethernet and a SCSI port for Sun workstations. The plotters are compatible with AutoCAD, Autoshade, Calcomp 58000, HPGL, Truevision Targa, Sun Raster, raw raster, RGB (red, green, blue), and CMYK (cyan, magenta, yellow, black) software. Third-party support includes GDS-II Stream, Postscript, and CGM formats. List prices for the different hard-disk options appear in the **table**. An optional Toner Auto-Concentration System, which monitors the toners and adds concentrate to the system when the color density reaches a set value, costs $2000 (436 models only).—**John Gallant**

Raster Graphics, 285 N Wolfe Rd, Sunnyvale, CA 94086. Phone (800) 441-4788; (408) 738-7800. FAX (408) 749-0544. **Circle No. 731**

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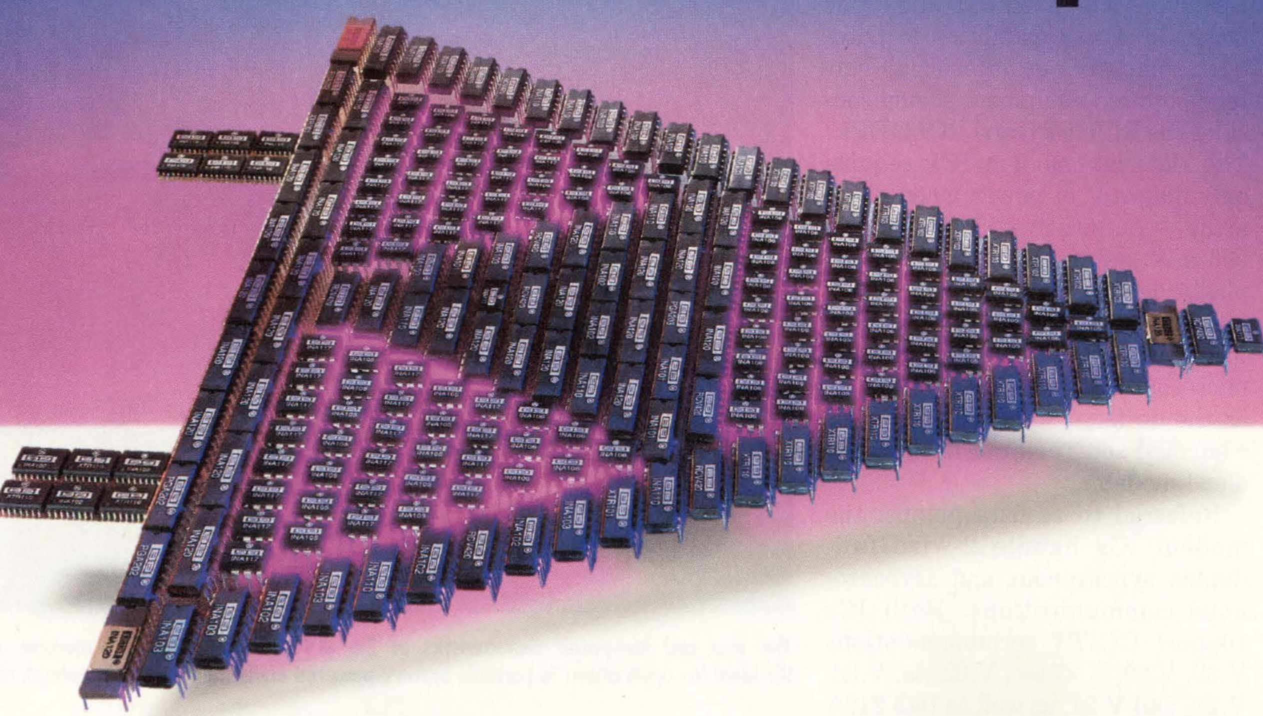

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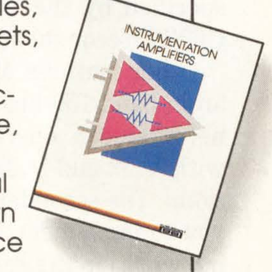

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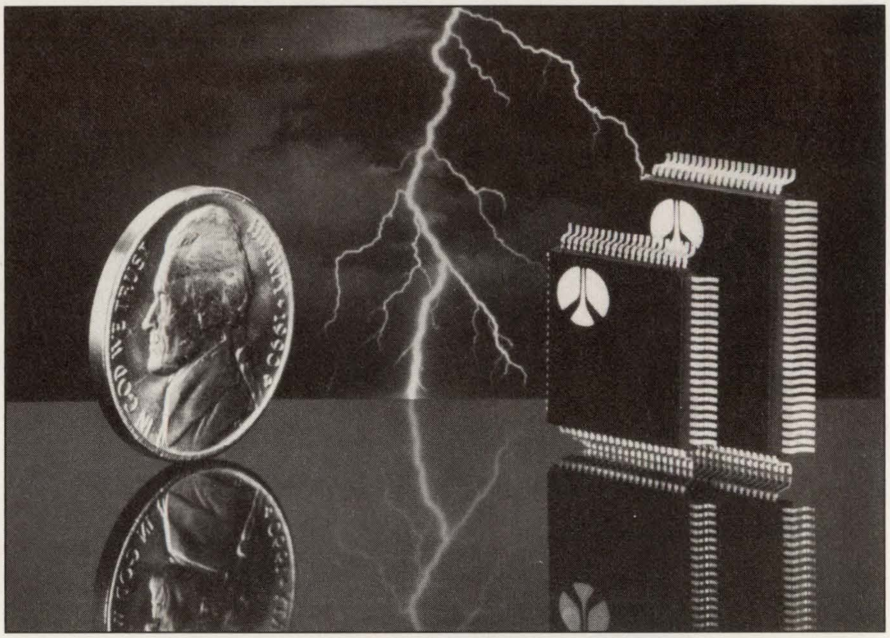
CIRCLE NO. 46

Modem ICs consume only 390 mW, yet perform fax and data duties

Designers who need to add data or facsimile (fax) capabilities to notebook computers or other small battery-powered equipment should consider the RC96DPL and RC144DPL. The data/fax modem ICs require only 390 mW of power when operating—competitive chips require 500 mW and more. A single 68-pin plastic leaded chip carrier (PLCC) houses the ICs, and they can perform voice processing. A companion microcontroller adds functions, such as the de facto standard Hayes AT command set, required for a stand-alone modem.



The size and low-power characteristics of the RC96DPL and RC144DPL modems make the ICs ideal for applications in portable battery-powered equipment such as notebook computers.

Referred to as data pumps, the modem ICs handle 2-wire full-duplex synchronous and asynchronous communications. Both ICs support CCITT recommendations V.32, V.29, V.27 ter, V.22 bis, V.22, V.23, and V.21, as well as Bell 212A and 103 de facto standards. Therefore the chips handle data-modem duties in communications speeds ranging from 300 to 9600 bps, and fax communications at speeds ranging from 2400 to 9600 bps. The RC144DPL also supports 14,400-bps fax and data communications specified by the V.17 and V.32 bis CCITT recommendations.

Other features of the ICs include an in-band 150-bps secondary channel that can operate concurrently with V.32 and V.32 bis communications. The secondary channel allows you to implement functions such as network management. The ICs have digital near- and far-echo cancellation and support bulk delay for satellite transmission. They also have compromise and automatic adaptive equalizers and feature a dynamic range of −43 to 0 dBm.

Because the ICs basically consist of a DSP core with an analog front end, DSP software actually handles support for specific protocols. The DSP-core-design approach also allowed the IC designers to include support for voice operations. The modem ICs provide an ADPCM (adaptive differential pulse-code-modulation) voice codec (coder and decoder). The ADPCM codec compresses voice signals to minimize the size of digitized voice messages. You can program the codec to operate at 28.8, 21.6, or 14.4 kbps at a 7.2-kHz sample rate. Silence detection and deletion, and decoder silence interpolation further improve compression rates.

The RC96DPL and RC144DPL have functional capabilities that are key for modem applications ranging from stand-alone modems to modem cards for personal computers. The size and power characteristics, however, make the ICs a particularly good choice for portable or battery-powered applications.

The ICs not only require 20% less operating power than other available products, but also require only 10 mW in sleep mode. Competitive products use 50 mW in sleep mode. The sleep-mode capability can prolong battery life in portable applications such as notebook computers. The company offers each modem IC in a 68-pin PLCC or in two (80- and 100-pin) plastic quad flatpacks.

The modem ICs will be available by the end of April. The RC96DPL costs $83, and the RC144DPL costs $98 (10,000). By the end of May the company plans to ship chip sets that include a modem chip and a companion microcontroller (μC). You can use the μC to implement features such as the Hayes AT command set or V.42/V.42 bis error correction and data compression. The chip sets, designated RC96ACL and RC144ACL, will cost $98 and $113 (10,000), respectively.—**Maury Wright**

Rockwell International, Digital Communications Div, 4311 Jamboree Rd, Newport Beach, CA 92658. Phone (714) 833-6849. FAX (714) 833-6399. **Circle No. 733**

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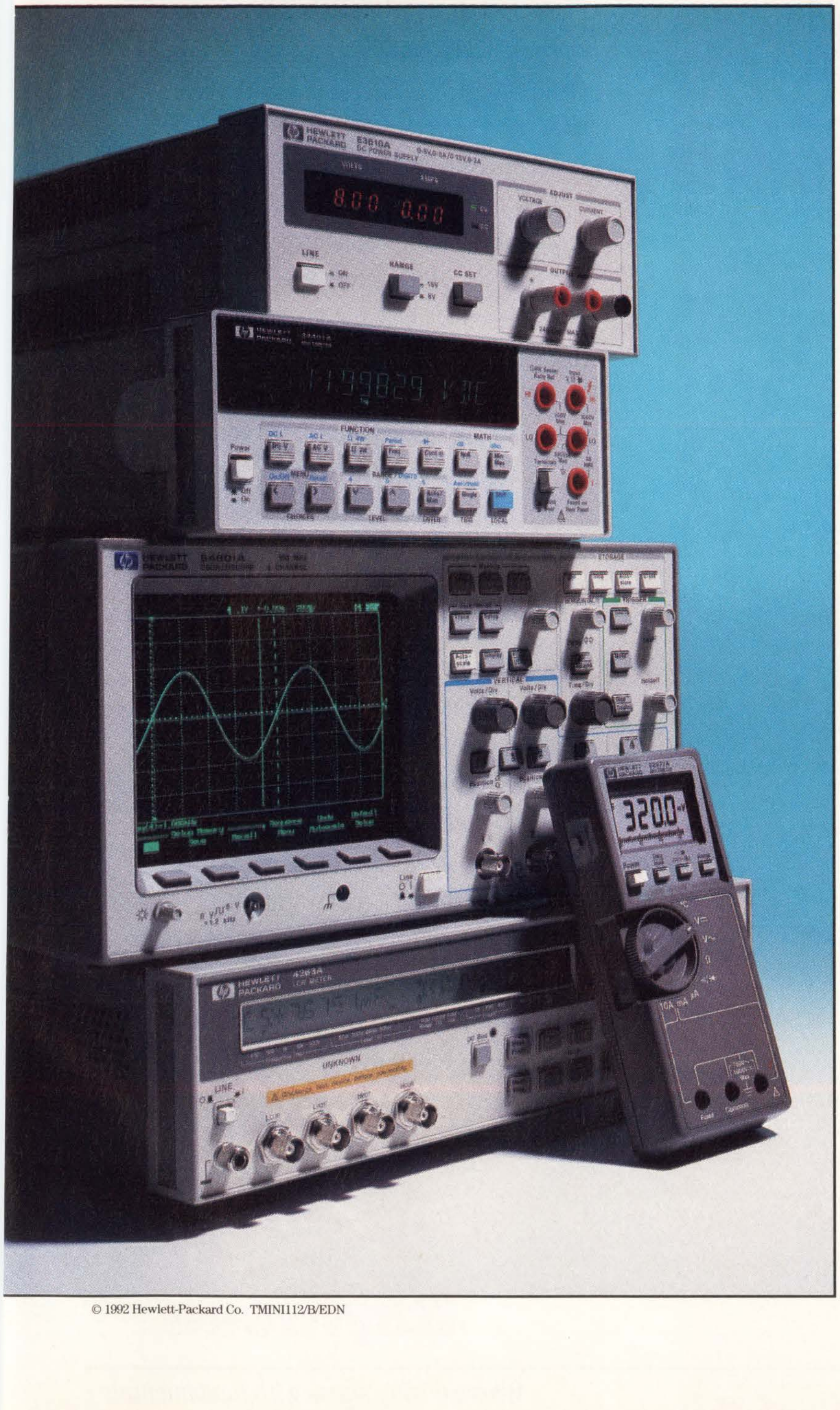

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CIRCLE NO. 48

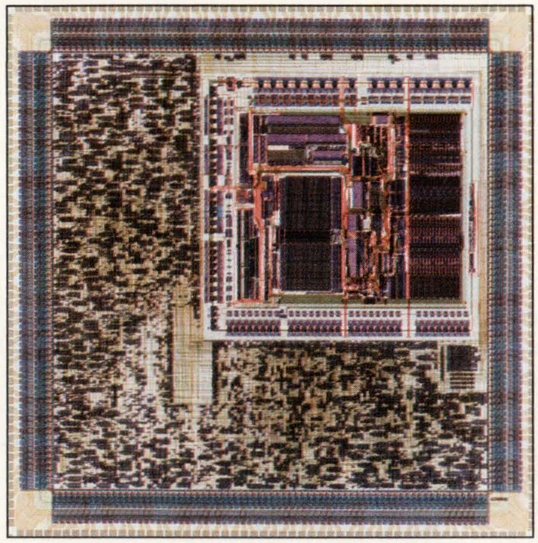
Gate array builds on 68000 CPU core and integrates logic onto chip

Many engineers cut their design teeth on the 68000 microprocessor—a clean, elegant processor that dominated 16-bit embedded systems. Today, engineers can get the same 16.67-MHz processor as an ASIC core in Motorola's H4C-CDA gate-array family. An ASIC lets designers create high-density minimal chip designs, integrating glue and control logic onto a chip with the processor.

Other 68000 cores for custom design are available from vendors such as Signetics-Philips and Toshiba. However, this is the first time the 68000 is available as a gate-array core. The gate array uses the same 68000 core that Motorola builds into the 68302 microcontrollers (μCs). Standard 68000 timing is guaranteed at the gate array's pins: The part can be used to drive an existing 68000 design (with a different board layout). The 68000 array pins can be redefined for applications. Gate-array control logic has access to the 68000 control signals: DTACK, IPL, and BR.

Initially, the 68000 core is available as a defused block on the H4C057 array. This block has a fixed placement in the array to guarantee fixed CPU timing and pin routing. This array fields 57,000 usable gates, of which roughly 21,000 are replaced by the 68000 core and associated support logic. This move leaves approximately 37,000 available gates for special logic (with a 50 to 70% usage factor). The CPU core can be moved to other arrays, but it requires layout.

The 68000 core has more than 10 years' worth of software applications, software development tools, hardware tools, and a pool of 68000 programmers and designers. The array and 68000 processor are designed to take advantage of this base. The 68000 core is set up for test. A standard 68000 test program runs the CPU through its paces while the rest of the gate-array circuitry stays isolated. Designers added special circuitry for in-system debugging: The 68000 can be single stepped and halted. In addition, a pinout conversion board suits the 68000 for use with standard ICEs.



The 68000 core has a fixed position in the gate array, ensuring fixed signal delays and characteristics. The core takes up 20,000 gates.

Motorola H4C Series—H4C057 gate array

Gate counts	21,000 68000 core; 37,000 for logic, 57,368 total
Clock (max)	60 MHz
68000 clock	16.67 MHz
Routing	3-layer metal
68000-core pins	65 total
68000 power	0.3W
Gate power	3 μW/gate/MHz
Typical gate delay	180 psec (2 NAND)
Test	JTAG, LSSD/ESSD scan supported
I/O	3.3, 5.0V MOS, TTL can drive 48 mA
Pins	160-pin quad flatpack
Cost	>$30,000 for NRE; $25 (10,000)

Gate-array designers can simulate the core with a functional C model, which is compatible with the Verilog hardware description language used by many chip and system vendors. They can also run the Logic Automation 68000 functional model. Designs are entered via standard schematic-capture tools. Various timing and ATPG tools are also available. In addition, engineers can work at higher design levels with hardware-description languages and logic-synthesis tools from Synopsys and Cadence.—**Ray Weiss**

Motorola Inc, Application Specific Integrated Circuits Div, 1300 N Alma School Rd, Chandler, AZ 85224. Phone (602) 821-4426. FAX (602) 821-4850. **Circle No. 734**

Fuzzy logic drives 4-bit microcontroller

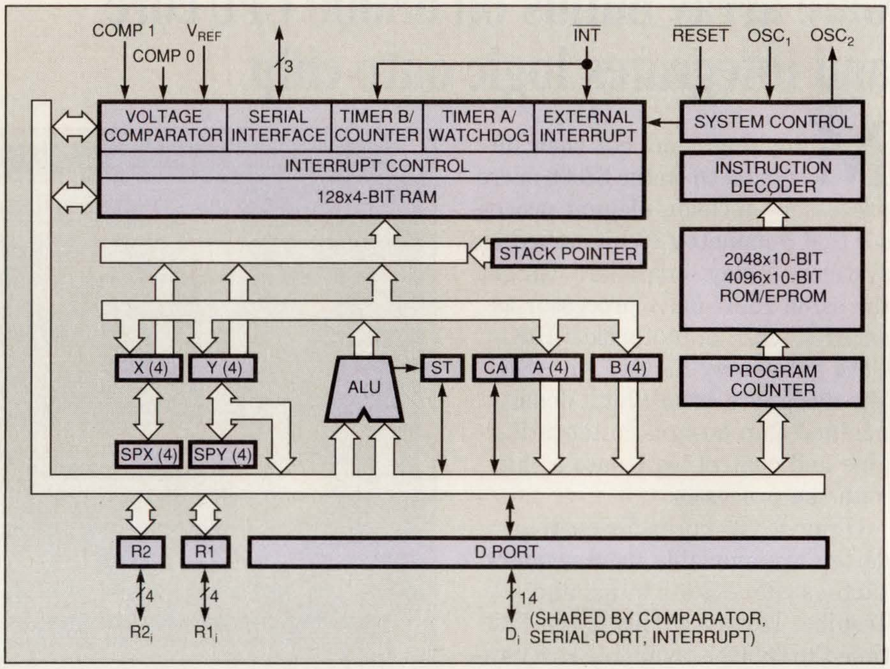
Lately, 4-bit microcontrollers get little respect; but, 4-bit microcontrollers (μCs) are potent processors that are still evolving. Hitachi's Compact 400 series 4-bit μCs bring the high-end HMSC400 architecture—4-bit data and 10-bit instruction—down to smaller 28-pin applications. Hitachi is simultaneously adding sophisticated high-end software capability, which is the first set of fuzzy-logic development tools for 4-bit μCs (see **box**, "Fuzzy logic arrives in the 4-bit world").

Running at 4.5 MHz, the Compact 400 series delivers more than

1 MIPS; an instruction cycle takes 0.89 μsec. With 28 pins, the μCs support 22 I/O lines and are self-contained, with as much as 2k×10 bits of program ROM or 4k×10 bits of program EPROM.

Contrary to many engineer's expectations, 4-bit architectures have the programmability of a standard 8-bit μC. They differ, however, by having a smaller, 4-bit-wide data path that limits I/O bandwidth and can complicate dynamic program addressing. However, for many applications such as small appliances or consumer products, 4-bit data paths are more than adequate. Also, the peripheral lineups of these μCs suit them for high-current or -voltage drive applications; for example, in LCDs and vacuum fluorescent displays.

Unlike many 4-bit μCs, the Compact 400 actually has a 10-bit instruction word (most use 8-bit instructions) with 4-bit data paths. Ten-bit instructions give the processor additional addressing and operand capabilities, thereby simplifying programming. By using a 10-bit-wide instruction, the CPU can support a complex set of instructions. In addition, a single ROM word can serve as an im-



This 4-bit μC uses 10-bit instruction and 4-bit data paths. The compact chip comes with a voltage comparator, serial lines, and timers.

Fuzzy logic arrives in the 4-bit world

Engineers no longer need 8- or 16-bit microcontrollers as a base for embedded fuzzy-logic applications. Fuzzy logic now runs on 4-bit μCs as well. Hitachi Ltd and Togai Infralogic Inc cooperatively developed a fuzzy-logic development tool, which delivers code that runs on 4-bit μCs: the Hitachi Compact 400 and the HMSC400 Series.

Fuzzy logic offers a simplified control mechanism, replacing complex control equations. With fuzzy logic, input measurements are converted into fuzzy values of input membership functions and are used to drive a set of logic rules. These rules take the fuzzy input values, evaluate them in parallel, and produce fuzzy outputs. These results are then mathematically squeezed to deliver standard control outputs.

For many applications, fuzzy technology enables engineers to concentrate on the control problem rather than creating the complex mathematical equations needed for control. Building a fuzzy application is a matter of defining input and output membership functions, writing the rules, selecting a "defuzzying" method, and then testing the system.

Fuzzy processing runs on a 4-bit Compact 400 μC. A typical control problem with 3 inputs, 14 rules, and 2 control outputs takes less than 1.6k×10 bits of program ROM, including the fuzzy runtime library. In addition, it uses 104 nibbles of RAM.

Togai Infralogic supplies an interactive, MS-Windows-based fuzzy-logic development system. The H400 μFPK&C, a runtime fuzzy-processing kernel and compiler for the Hitachi 4-bit μCs, supplements this tool kit, which costs $18,500 (no production code royalties). Togai has similar development tool sets for Hitachi 8- and 16-bit μCs.

Togai Infralogic Inc, 5 Vanderbilt, Irvine, CA 92718. Phone (714) 975-8522. FAX (714) 975-8522. **Circle No. 736**

Hitachi HMC400 compact 4-bit μC

Clock	1.125, 4.5 MHz (internal)
Instruction cycle	0.89 to 4.0 μsec
Registers	Six 4-bit registers, 12-bit program counter, 8-bit stack pointer
Memory	64 or 128×4-bit RAM 1k or 2k×10-bit ROM or 4k×10-bit EPROM
Timers	Timer/counter; watchdog
I/O	22 special drive lines
Interrupts	1 external
Miscellaneous	Serial interface, voltage comparator
Power	3.5 to 6.0V: low-power version 2.5 to 6.0V
Package types	28-pin DIP, Small-outline flatpack
Price	$2 (5000)

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mediate RAM address (it addresses 1k nibbles).

A low-power version of the Compact 400 operates at 2.5 to 6.0V. Using a 1.125-MHz clock, this version reduces power consumption by 60% and delivers a 3.55-μsec instruction cycle.

Two timer combinations are available: one with an 11-bit prescaler and 8-bit timer/counters, and one with an 11-bit prescaler, 8-bit (free running) watchdog timer, and an 8-bit auto-reload timer/event counter. The prescaler counts up the system clock and can provide low sampling frequencies. The prescaler divide ratio (count) is set into a timer mode register.

—**Ray Weiss**

Hitachi America Ltd, Semiconductor and IC Div, 2000 Sierra Point Pkwy, MS-080, Brisbane, CA 94005. Phone (415) 589-8300. FAX (408) 583-4207. **Circle No. 735**

Low-cost 32-bit DSP processor runs floating-point operations

Thirty-two bit DSP is no longer the preserve of expensive applications. Analog Devices' ADSP-21010 is a reduced version of the high-speed, 32-bit floating-point ADSP-21020.

Priced at $49.90 (100), the ADSP-21010 delivers 32-bit floating-point power, running a complex 1024 FFT in 1.54 msec. To lower the cost, however, the ADSP-21010 is a slower chip, having an 80-nsec instruction cycle—compared with 40 nsec for the ADSP-21020. The processor is also less complicated, supporting only IEEE 32-bit floating-point format.

The ADSP-210x0 series architecture is structured for high-speed DSP, especially algorithm inner loops. The DSP CPUs support a modified Harvard architecture, with separate external instruction and data buses. The processors have a 48-bit instruction word and a 32-bit data word, with 24- and 32-bit address buses, respectively.

The 48-bit instruction word has extra bits to define multiple operations per cycle. It does, however, require two different memory designs—32 bit (data) and 48 bit (program).

These DSP architectures have a unique instruction caching scheme. Each processor has a small instruction cache (32-word cache) to hold inner loop instructions. When executing instructions in a programs' repetitive inner loop of the cache, the program address and program data bus are used to access data. The CPU does two data memory accesses per instruction cycle; it has two built-in address generators for data access.

The ADSP-210x0 design avoids expensive on-chip data caches and large instruction caches. Processing centers on a 10-port, dual 16×40-bit register file; it has two sets for fast context switching. The register file is served by an ALU, a multiplier (and fixed-point accumulator), and a 32-barrel shifter.—**Ray Weiss**

Analog Devices Inc, Box 9016, Norwood, MA 02062. Phone (617) 461-3704. **Circle No. 737**

The ADSP-21010 processor

Clock	25 Hz external
Instruction cycle	80 nsec at 25 MHz complex 1024 FFT (1.54 msec)
Registers	10-port register file 2 sets of 16 registers
Memory space	48-bit instruction 32-bit data
Address space	Separate instruction and data: 40-bit instruction, 32-bit data
On-chip memory	Small, effective 32-word (48-bit) instruction cache; 2-way, set associative
Arithmetic	32-bit fixed, IEEE floating point
Interrupt	Five external interrupts
Timer	32 bit
Serial	Asynchronous serial interface synchronous serial interface A/D, D/A, AES/EBU
Miscellaneous	Automatic loop control, on-chip ICE support
Package	223-pin PGA
Price	$49.90 (100)

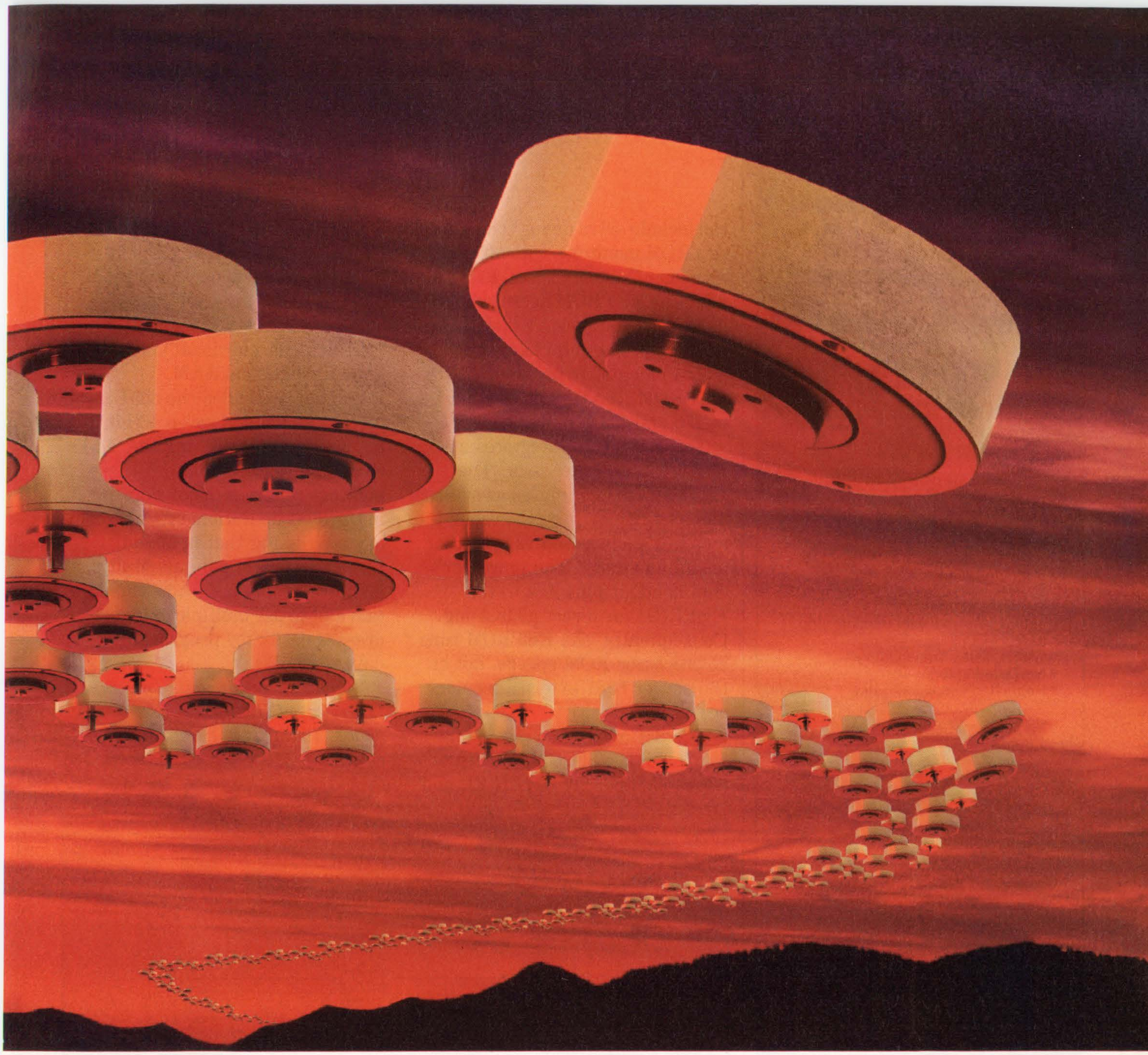
Chip integrates 8051 architecture with EEPROM

Engineers can now use a single microcontroller (μC) chip for embedded designs; unfortunately, single-chip solutions generally use on-chip ROM. Debugging embedded ROM code isn't easy: you need to change the code as the application code shakes down. Siemens' Macrochip provides a debug solution for 8051-based designs. The 80C51xxx Macrochip is a single-chip hybrid. Packaged in a 64- or 84-pin plastic leaded chip carrier, the chip contains an 8xC51 chip and EEPROM memory in place of on-processor ROM, so users can easily reprogram the code.

With the Macrochip users can debug their programs, modifying program memory as needed. With the 32-kbyte EEPROM version, you

The Siemens 80C51xx Macrochip

Clock	12, 18 MHz
Instruction cycle	12 clocks
Memory	256-byte scratch pad 1-, 2-kbyte external RAM (some) 8- or 32-kbyte EEPROM 64-kbyte instruction address space 64-kbyte data address space
Timers	Three or four 16-bit counters watchdog timer
I/Os	Six or seven ports: 56 pins One input port: 8 pins
Interrupts	2 external
Miscellaneous	8-bit A/D converter, duplex serial I/O
Package	68- or 84-pin PLCC
Price	From $345



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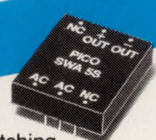

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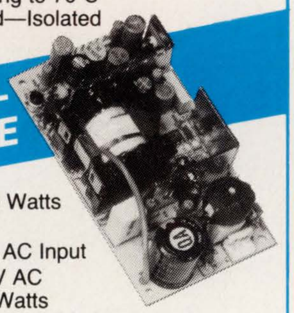

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CIRCLE NO. 39

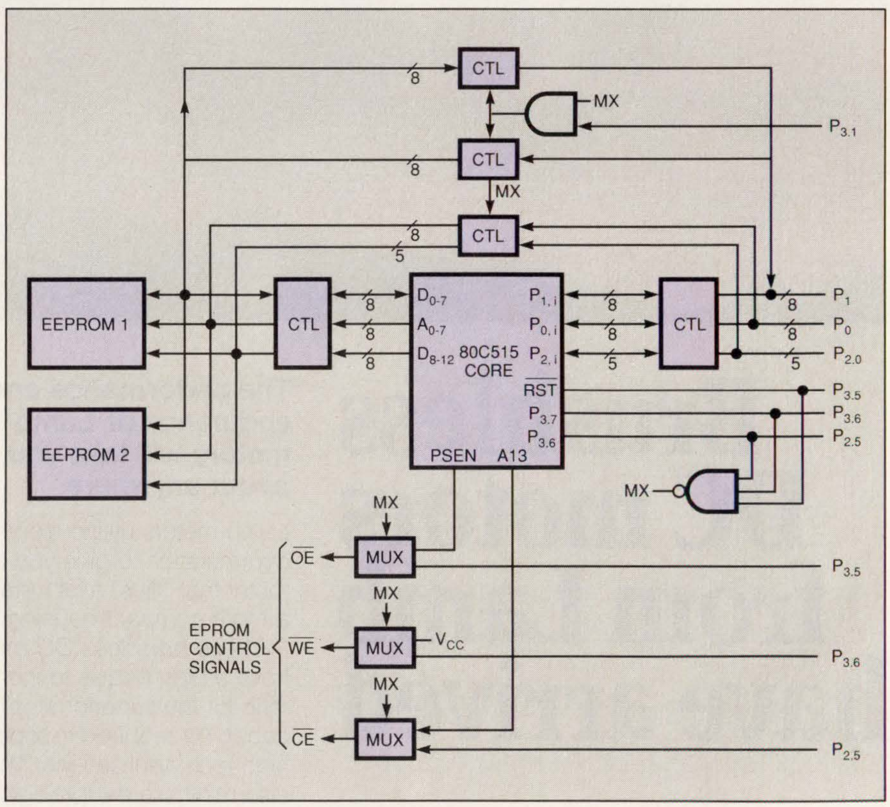
can include extra debug code—such as a ROM monitor—without running out of memory space. Programming the EEPROM doesn't require new board voltages; 5V is all that's necessary. The chips have standard 8xC51 pinouts. To program the EEPROM, the rest pin and port-3 pins 6 and 7 are pulled low.

The Macrochip integrates an EEPROM and processor. The EEPROM is not treated as external memory by the processor chip; instead, it's addressed as processor on-chip memory. The processor's chip bondout pins link to the EEPROM for direct addressing. Consequently, the EEPROM runs at processor ROM speeds, not at the slower 8051 external-memory access speeds.

The 8xC51xxx Macrochip has four modules: 80C515AH-3J, 83C515AH-5J, 80C517AH-3J, and 83C517AH-5J. The 80C51xxx is a CMOS 8051 core with a 12- or 18-MHz clock rate, 256 bytes of RAM, and 8 or 32 kbytes of EEPROM. The 83C51xxx is a variant of the 8051, with an additional 1 or 2 kbytes of external RAM.

Siemens extended the 8051 architecture and added seven 16-bit data pointers, supplementing the 8051's single addressing pointer. These pointers relieve a major bottleneck in the 8051 operation: off-chip memory addressing that is forced through a single pointer. Multiple pointers enable programs to maintain and to use multiple external addresses easily for program and data.—**Ray Weiss**

Siemens Components Inc, 2191 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 980-4500. FAX (408) 980-4596. **Circle No. 738**



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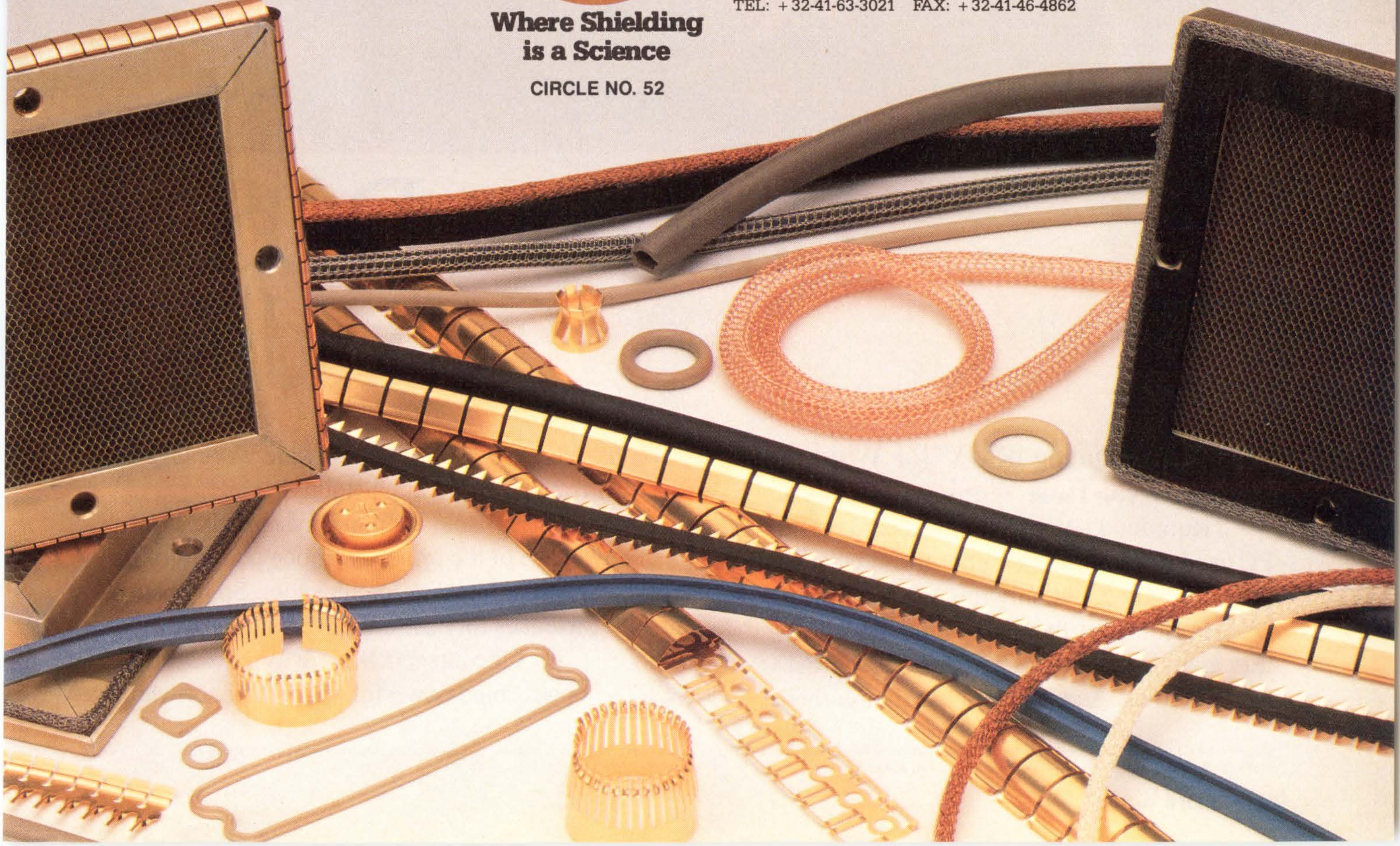

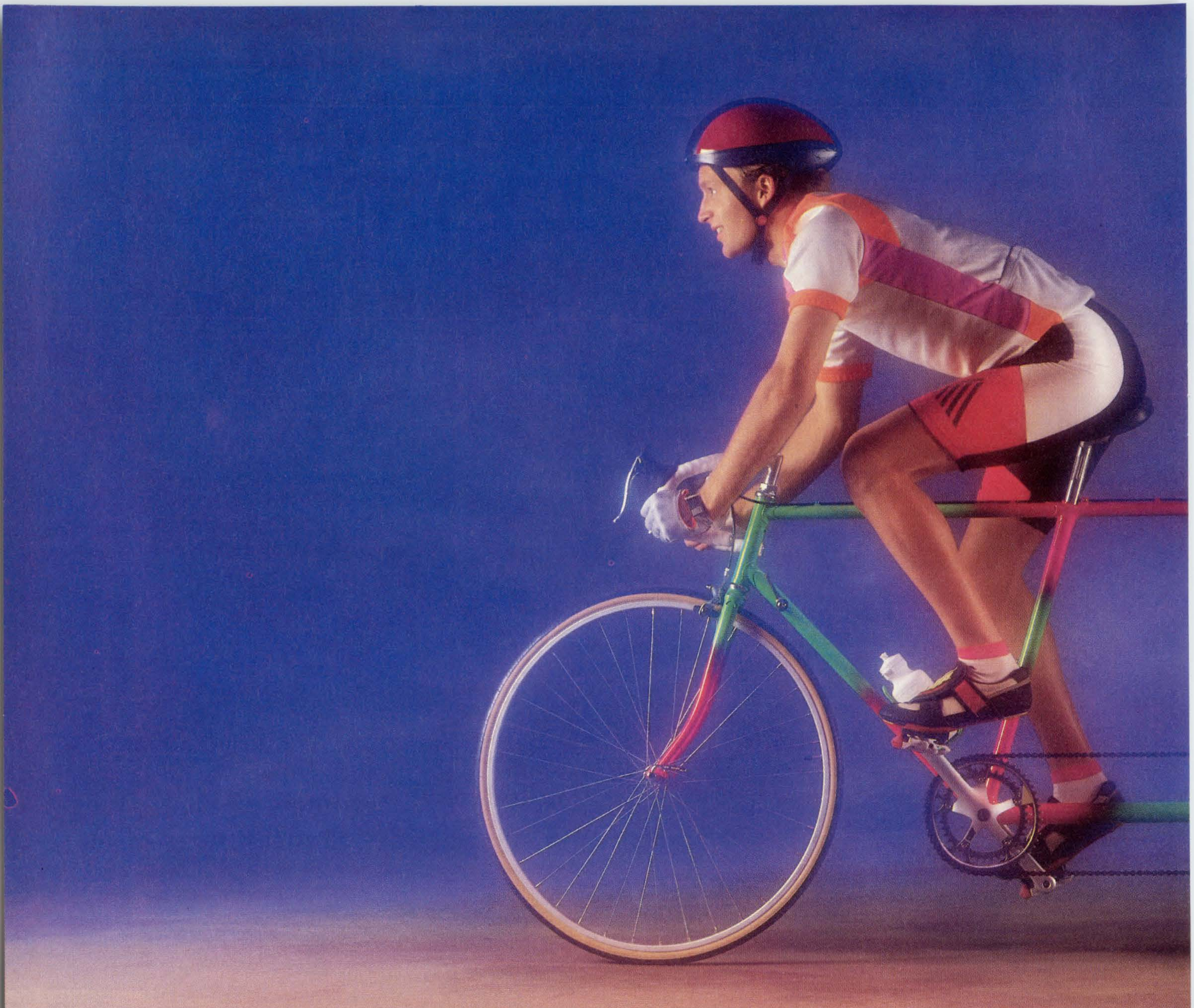

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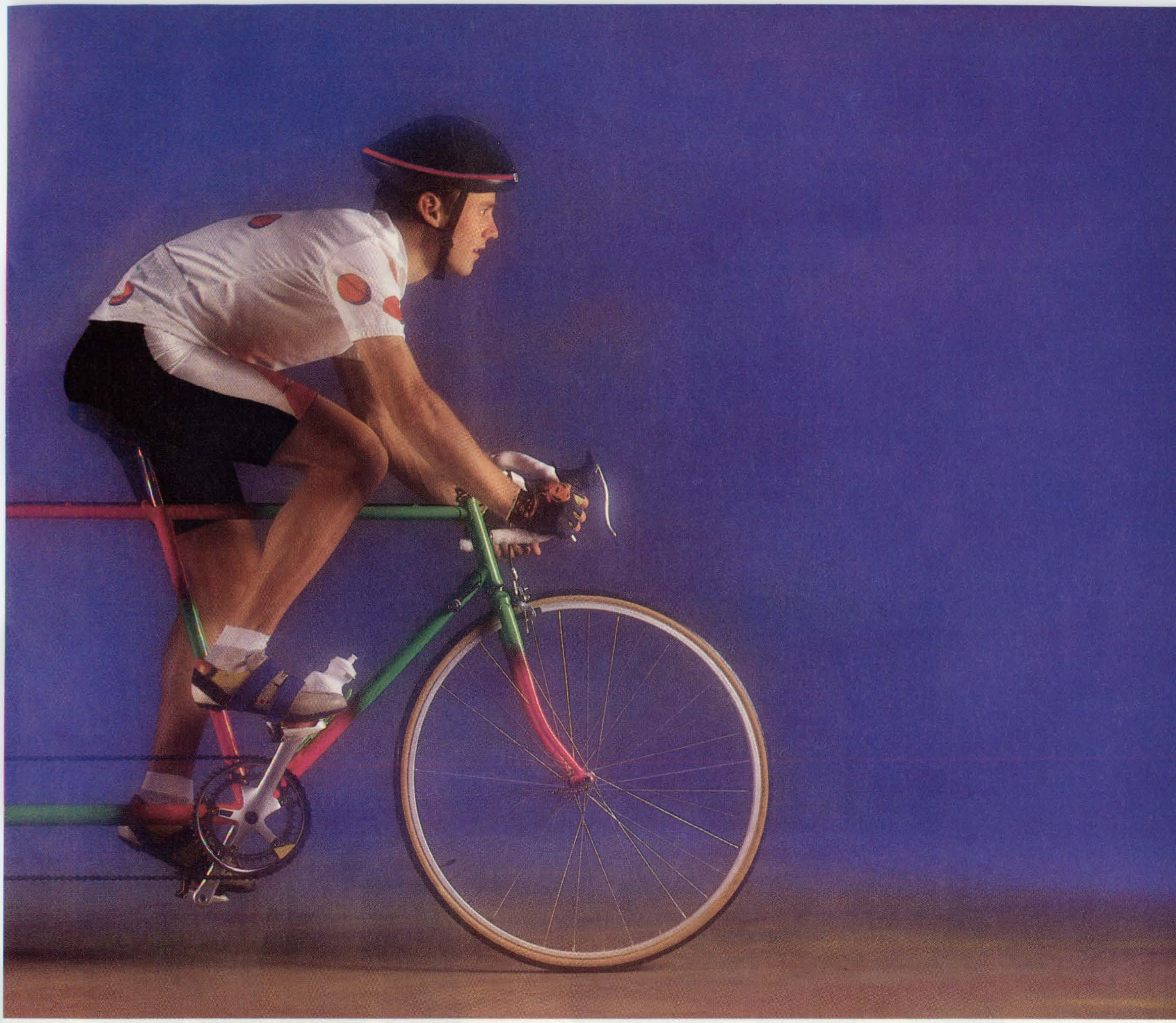

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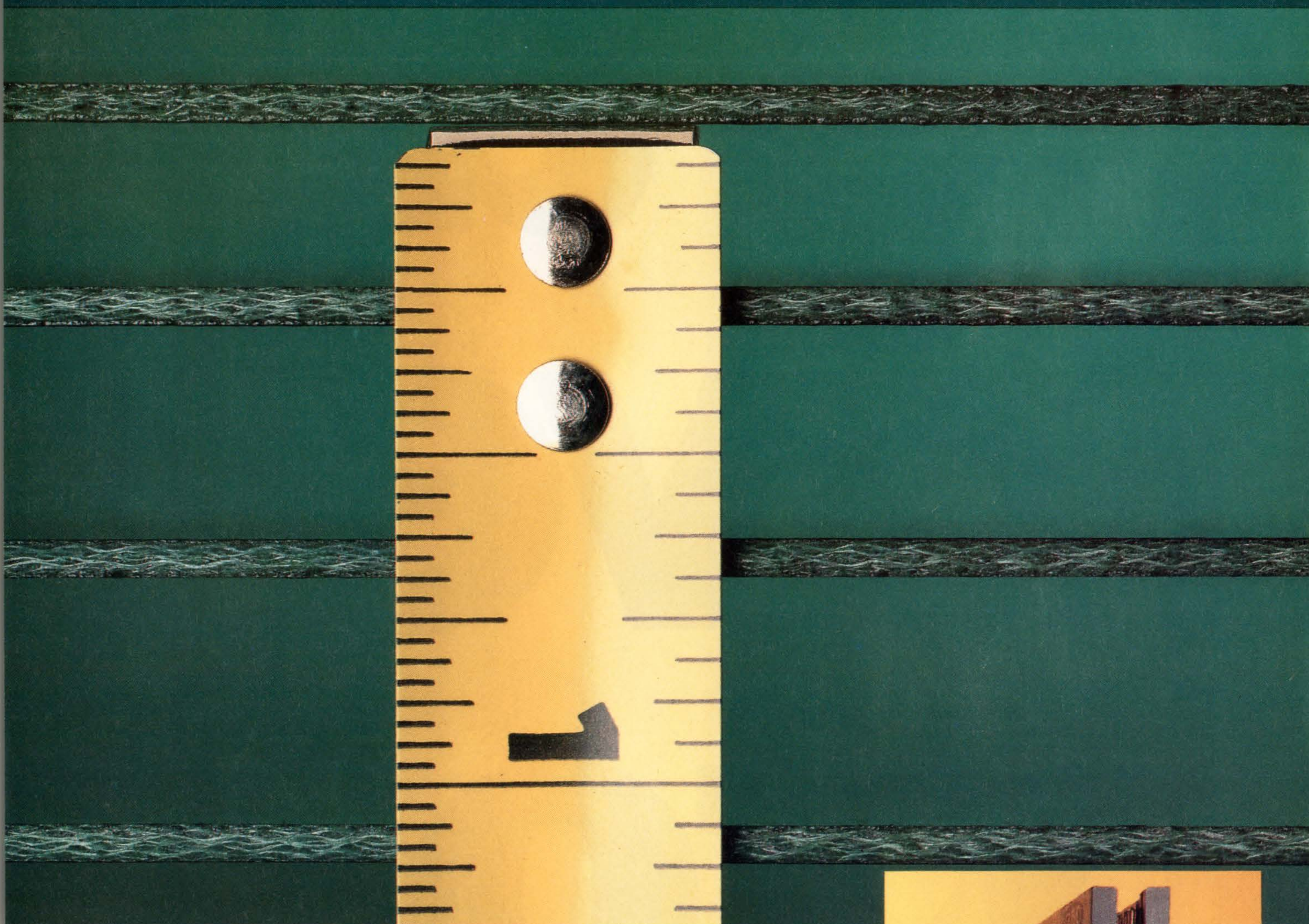

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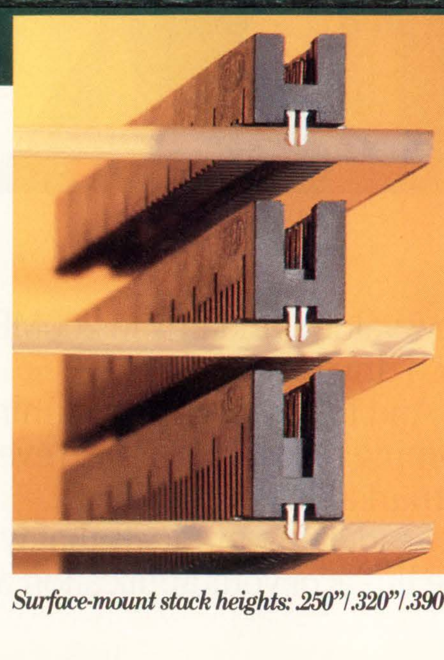

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CIRCLE NO. 55

Taking the first steps

If you're considering designing with FPGAs, this 2-part hands-on design project will show you exactly what is involved. Part 1 covers the design and schematic entry, and part 2 covers simulation and the functioning circuit.

DOUG CONNER, Technical Editor

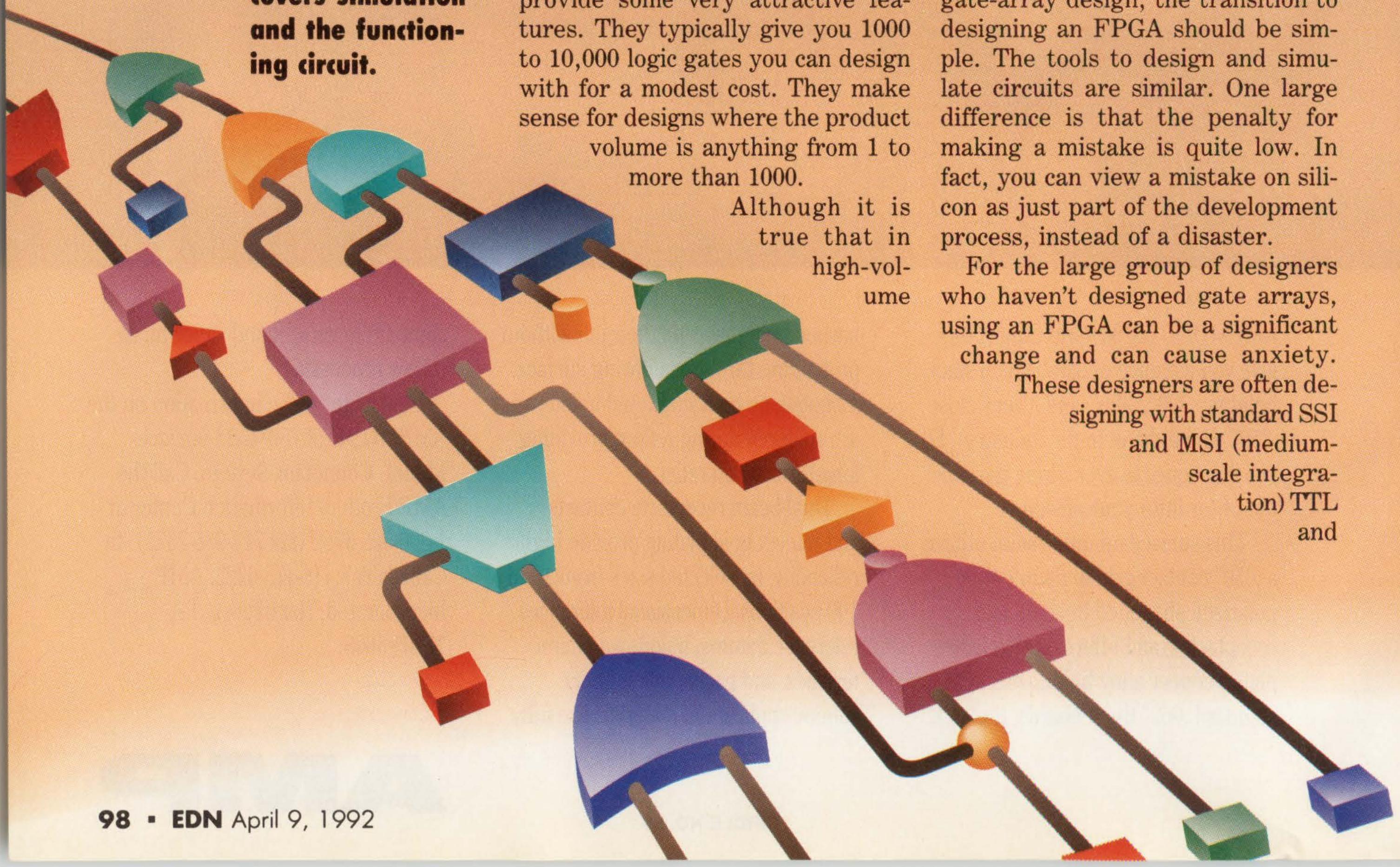
The fear and uncertainty of making a major shift in your design and development methodology is always compounded by tight schedules. As a result, you may be putting off designing with field-programmable gate arrays (FPGAs) because you don't know what to expect from them and you don't have the time to find out.

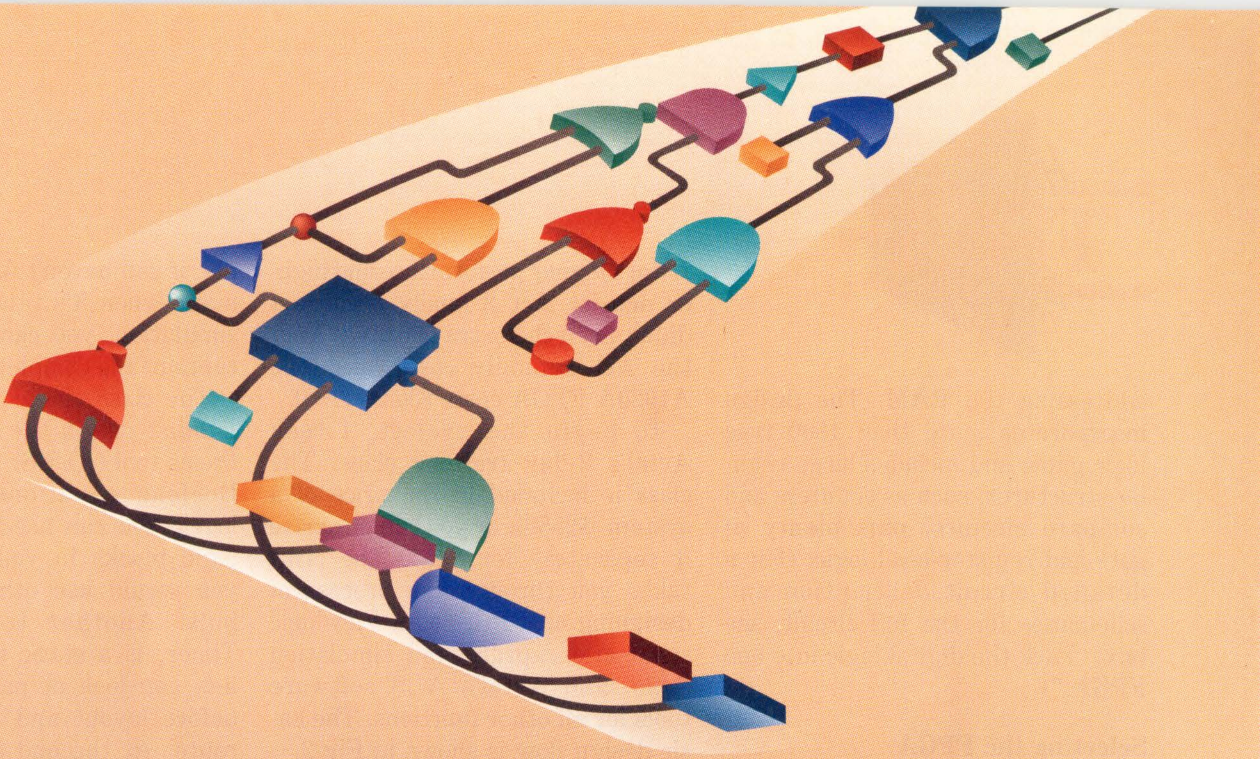
FPGAs and high-density PLDs provide some very attractive features. They typically give you 1000 to 10,000 logic gates you can design with for a modest cost. They make sense for designs where the product volume is anything from 1 to more than 1000.

Although it is true that in high-volume production a masked gate array can offer substantial savings, it is also true that they offer a much larger financial commitment up front. Penalties for an inexperienced designer who makes a design mistake or a system-definition mistake is high, both financially and in time lost in making another design turn.

For a designer experienced with gate-array design, the transition to designing an FPGA should be simple. The tools to design and simulate circuits are similar. One large difference is that the penalty for making a mistake is quite low. In fact, you can view a mistake on silicon as just part of the development process, instead of a disaster.

For the large group of designers who haven't designed gate arrays, using an FPGA can be a significant change and can cause anxiety. These designers are often designing with standard SSI and MSI (medium-scale integration) TTL and



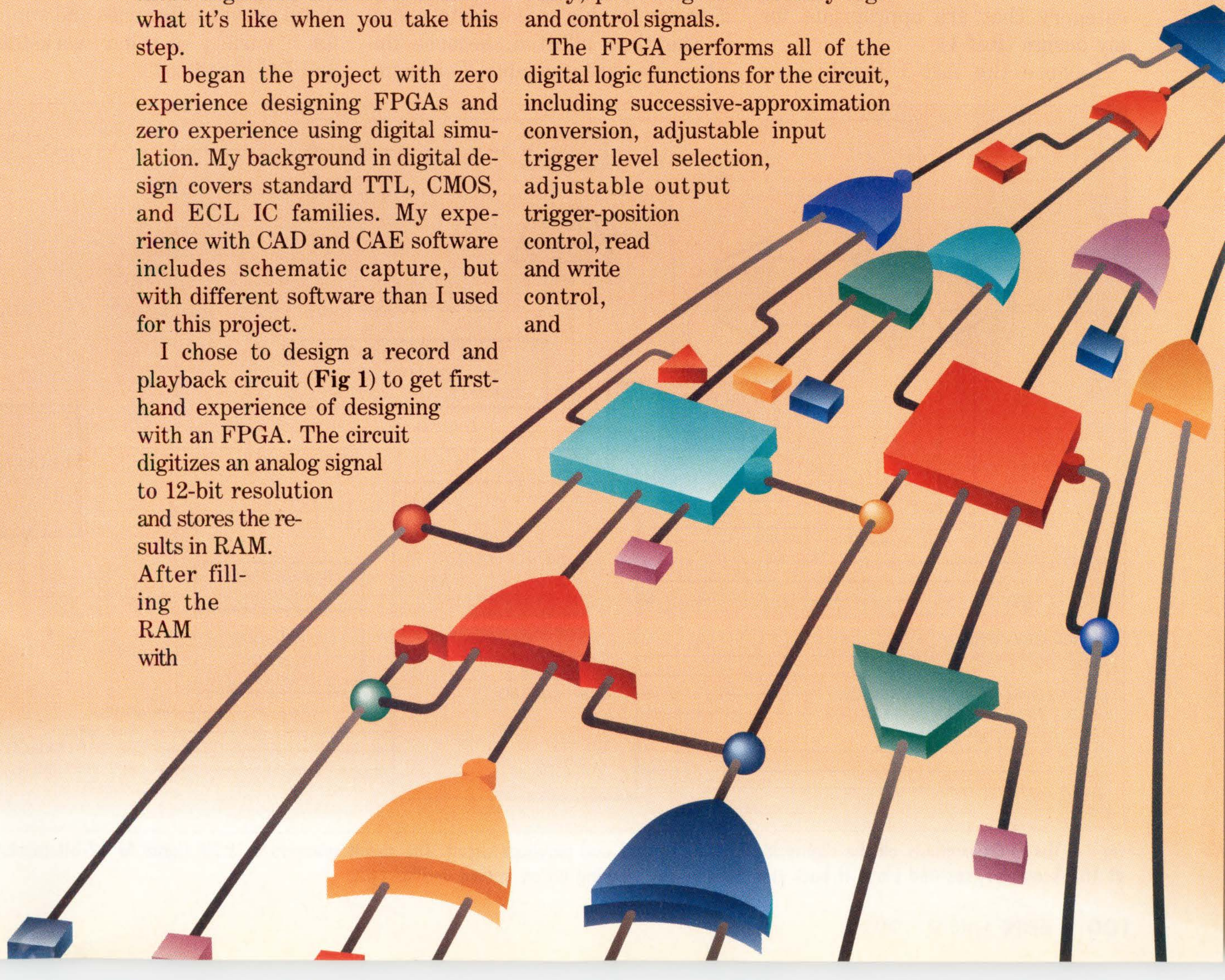


CMOS devices that interface to microprocessors, analog circuits, or both. Many have never used digital simulation. Moving to FPGAs is a step up for them. This project is for those engineers who want to know what it's like when you take this step.

I began the project with zero experience designing FPGAs and zero experience using digital simulation. My background in digital design covers standard TTL, CMOS, and ECL IC families. My experience with CAD and CAE software includes schematic capture, but with different software than I used for this project.

I chose to design a record and playback circuit (**Fig 1**) to get first-hand experience of designing with an FPGA. The circuit digitizes an analog signal to 12-bit resolution and stores the results in RAM. After filling the RAM with 32k words of data, it plays back the data, reconverting it to analog. The circuit is designed to work with an analog oscilloscope to capture a one-time event and play it back continuously, providing all necessary logic and control signals.

The FPGA performs all of the digital logic functions for the circuit, including successive-approximation conversion, adjustable input trigger level selection, adjustable output trigger-position control, read and write control, and



addressing the RAM. The design incorporates more than 1500 true logic gates and includes large regular structures, such as counters and compare circuits, plus plenty of gate-and register-level logic. (For a detailed circuit description and schematics for the full circuit, see **box**, "Pack the digital logic into one FPGA.")

Selecting the FPGA

I decided to use the Actel Act 1 FPGA family for my design. The choice of Actel was an arbitrary one—there are perhaps a dozen companies with products that fall into the FPGA and complex-PLD category that are appropriate for my design (**Ref 1**).

I chose the Act 1 family over Actel's higher performance and higher density Act 2 family because I didn't need the extra features. And, the Act 1 family costs less—the A1020A FPGA costs $36.25 (100).

To begin the project, I took Actel's 2-day training class. The class is included in the price of a system ($2950), or you can purchase it separately for $495. The class takes you through the process of designing an FPGA with Viewlogic schematic capture and simulation tools, and Actel's ALS software tools for all other functions. The basic design flow is shown in **Fig 2**.

The class uses canned files that you modify. For example, you'll add some components to a partially completed schematic to finish it. The class runs at a reasonably fast pace, but you won't fall behind even if you're unable to complete a step in the time allotted, because finished files are available. For example, if you haven't finished the schematic when it's time to move on to simulation, you can use a file that contains the completed schematic.

The class also covers some tools I didn't use in the project. A synthesis tool (ALES) lets you convert Boolean equations directly into logic. You can use the synthesized logic blocks in your schematic as you would use other macro symbols. Another tool, called the Timer, is a static timing tool that lets you look at path delays, both before layout and after place and route. At the end of the class you program an FPGA that contains a timing circuit and drives a 7-segment display.

Because Viewlogic CAE tools were used in the class, I elected to use them on the project, although Actel provides libraries and support for a variety of other workstation and PC-based tools.

Illustration by Gregg Dinderman

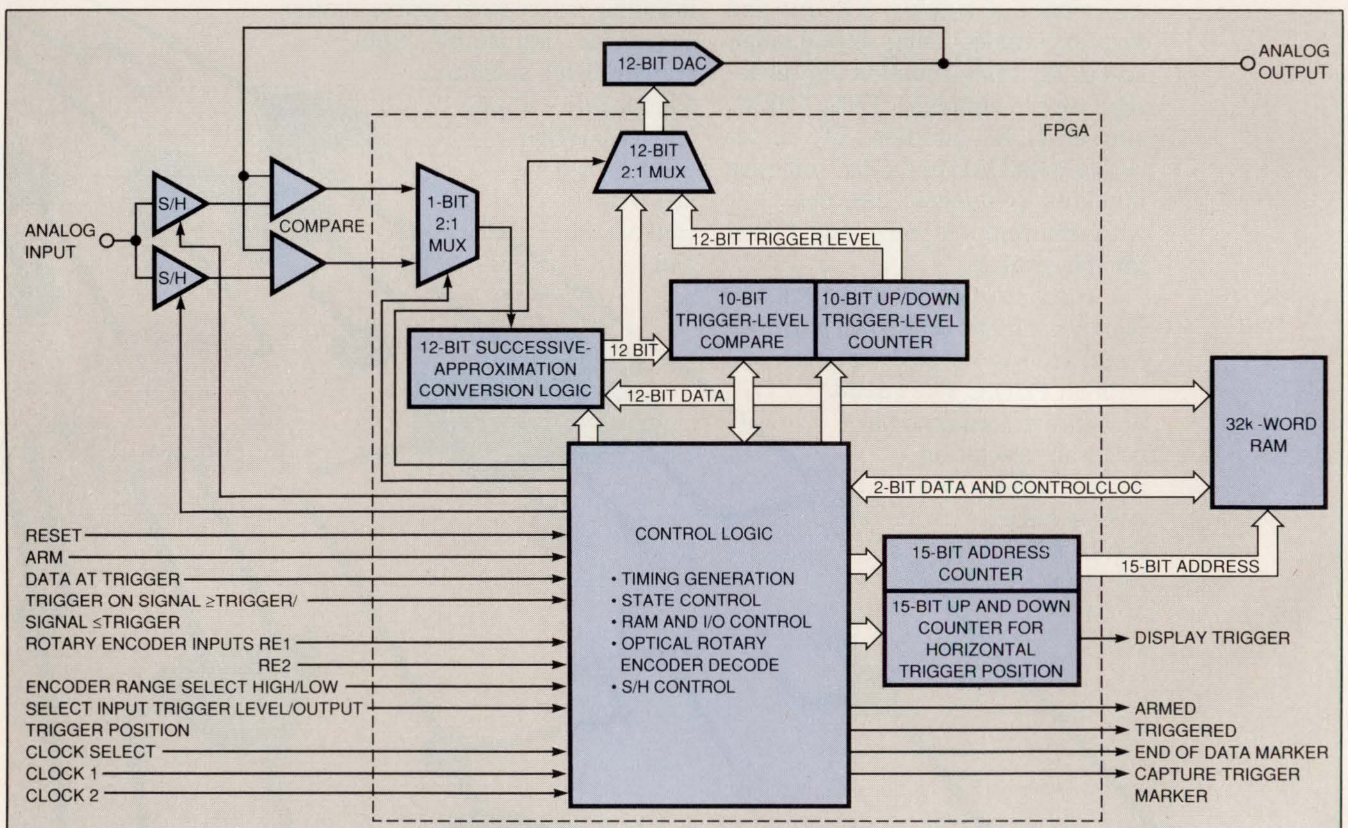


Fig 1—The FPGA contains all the digital logic of this record and playback circuit. The circuit converts a ±5V signal to 12-bit resolution at 167 ksamples/sec and plays it back continuously for viewing on an analog oscilloscope.

The building block on an Actel Act 1 FPGA is a logic module. What you actually design with is a logic module or group of logic modules configured as a hard or soft macro. A logic module starts as a flexible uncommitted block of logic; it can perform many different logic functions depending on how its connections are programmed. Actel provides hard macros, which define the logic-module connections to perform specific functions.

The hard-macro building blocks for designing an Actel FPGA are gates, gate combinations, latches, flip-flops, multiplexers, adders, and buffers. You can also configure every I/O pin as an input buffer, an output buffer, a bidirectional buffer, or a 3-state buffer. One input pin is designated as a clock buffer. You can see many of the basic building blocks and variations on pages of the circuit schematic (see **Figs 4** to **15**, which begin on pg 107).

Designing with the FPGA building blocks is similar to designing with 7400 series SSI devices, except in most cases the FPGAs are more flexible. For example, 2- and 3-input AND gates are available with any or all of their inputs inverted. You can select D flip-flops with positive clear, negative clear, and so on. Every gate macro I used requires a single module. Even a relatively complex gate combination, such as the 4-input AND/OR gate shown in **Fig 15**, is a single module. Although there are a few combinations that require two modules, I was able to avoid using them.

Latches also require only one module, even with a clear, an enable, or multiplexed inputs. Flip-flops, however, require two modules. In cases where a latch will work as well as a flip-flop, the module savings makes the latch a better choice. For example, the circuit needed to generate the DLY shown at the bottom of **Fig 6** uses two latches instead of flip-flops.

Another gate-saving consideration is to use multiplexed data inputs on both latches and flip-flops to bring 2-input gates inside them. The result saves a module. For example, the latch generating DISP_TRIG in **Fig 6** effectively ANDs together DISP_TM and PLYBK.

Part way through the design, I learned that the ALS software automatically combines 2-input gates with flip-flops and latches wherever possible. Therefore, you can see cases where I've left the gate separate, such as the latch and AND gate in **Fig 15**. The schematic is easier to read with the AND gate separate, so I'd recommend letting the software do its job. The end result on the FPGA is the same.

When your design calls for larger blocks (such as counters, adders, multipliers, decoders, and large registers), you've got several choices. You can use a soft macro if one exists, alter one if it's close but not quite what you need, or build what you want from scratch. The soft-macro library includes a wide selection of functions.

For example, you can select an adder with 8-, 12-, 16-, 24-, or 32-bit capacity. The soft-macro library also includes macros that are equivalent to some MSI TTL circuits. For example, the 8-bit up and down synchronous counter with rip-

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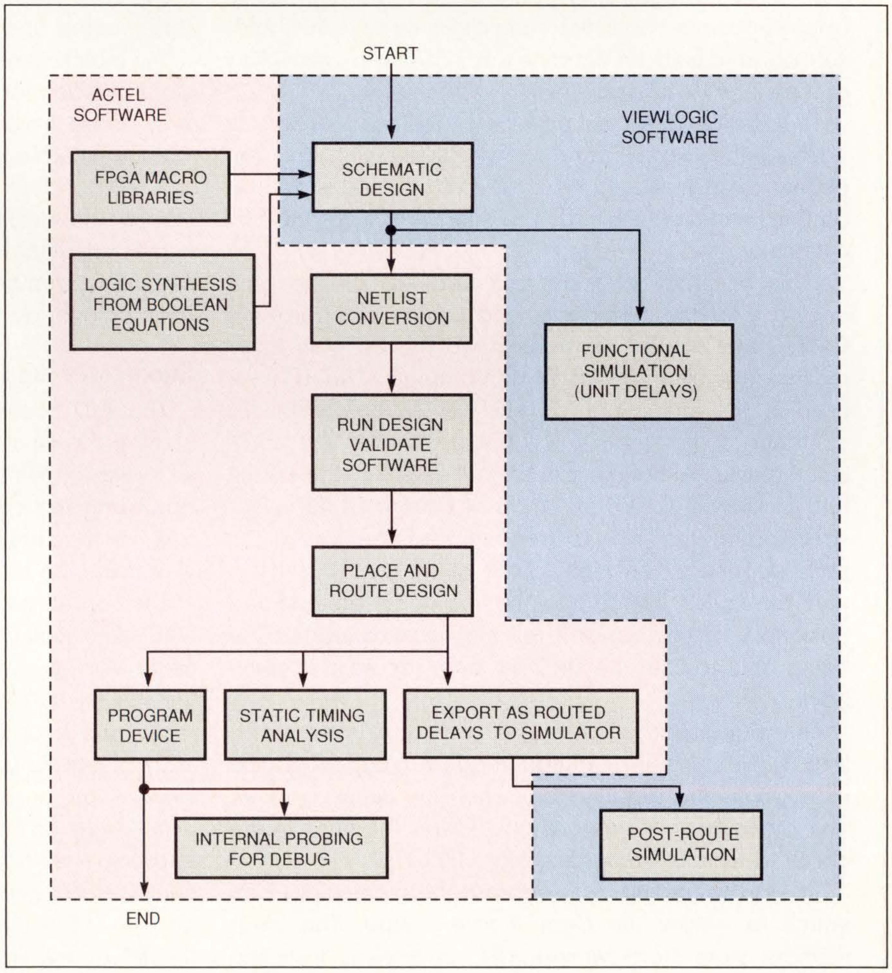

Fig 2—The total time for running netlist conversion, design validation, place and route, and exporting as routed delays took about half an hour for the design. This relatively fast turnaround lets you make quite a few design iterations in one day. The logic synthesis and internal probing for debug were not used on the project.

Pack the digital logic into one FPGA

When I decided to design an FPGA (field-programmable gate array) and write about it, I wanted to use it in a circuit with a minimum of other parts, yet I wanted the circuit to be moderately complex so that it would be a true test of designing with an FPGA. The record and playback circuit I chose packs all the digital logic into the FPGA, and the only other parts it requires are RAM and a few analog ICs (see **Figs 4** to **15** beginning on pg 107).

The top-level schematic for the overall circuit is shown in **Fig A**. The circuit uses the same 12-bit DAC and op amp for successive-approximation conversion during record and for generating the analog output during playback. Because conversion and playback use the same DAC, the gain and offset errors of the DAC and op amp do not add to the system error.

During conversion, the circuit compares the DAC's current output, converted to voltage by a high-speed op amp, with the sampled input voltage. The comparator output drives the successive-approximation logic. Two parallel paths alternately sample and compare the input against the DAC output. The alternating approach saves both the sampling time and the hold-settling time. Each bit decision takes 500 nsec, providing a complete 12-bit conversion every 6 μsec.

The design depends on closely matched offsets in each of the two S/H and comparator paths. You can expect close matching because both comparators are on the same monolithic IC. The same is true for the S/H channels.

Gain accuracy of the circuit depends on the gain accuracy of the S/H circuit and on the comparator's CMRR. The AD684 provides a worst-case gain error of ±5 mV over the ±5V input range. The LT119A used in the circuit has a minimum CMRR of 90 dB, contributing less than a 0.4-mV error over the ±5V input range. Although the LT119A used in the circuit has a minimum CMRR of 90 dB at dc, the CMRR is not specified at the 2-MHz frequency of the design. In fact, depending on high CMRR at frequency is risky, and generally frowned upon by knowledgeable analog designers. In this design I felt the risk was justified by being able to use one DAC for both record and playback.

The digital part of the circuit has four basic states (**Fig 5**): clear memory, armed, triggered, and playback. Playback is the default state when the circuit is reset. The other three states are also ORed together in the circuit to form the recording state (RECD).

To start recording, you depress the momentary arm switch to initiate the clear memory state. The clear memory state starts writing A/D conversions from the successive-approximation conversion into RAM, but disables the trigger until you fill the entire memory with new data, writing zeros to D13 and ones to D14. After you overwrite the entire memory, the state changes to armed, and the circuit continues to record data until the trigger logic is satisfied. Once triggered, the state changes to triggered (TRIGD) and the circuit converts 24,000 more samples, stores them in memory, and returns to the playback state.

You set the trigger level using a rotary encoder to adjust a 10-bit up-and-down counter (**Fig 14**). The logic performs a 10-bit magnitude compare (**Fig 15**) of the successive-approximation converter output with the trigger level to determine when to trigger the circuit.

The trigger-level compare is a full-magnitude compare that tests whether the digitized input signal is greater than or equal to the trigger-level setting or less than or equal to it, depending on the input (TRIG_GE). The 10-bit range provides a trigger-level resolution of 10 mV and gives time for the magnitude-compare results to become valid while the successive approximation is finishing the last two bits.

Control logic (**Fig 10**) also generates the RAM write enable (N_WE), the RAM output enable (N_OE), and the FPGA's output enable (F_OUT). **Fig B** diagrams the basic record and playback timing.

A 12-bit shift register (**Fig 4**) generates the 12 timing states needed for the successive-approximation conversion. These timing signals are also used to control all timing-related logic in the FPGA.

A clock-select circuit lets you select between two clocks. The circuit can play back the data at a much higher rate than it can during recording, because the DAC only changes state once every 12 clock cycles during playback.

Successive-approximation conversion

The A/D conversion starts with sampling and then holding the input. The timing generator uses a 12-bit shift register to control the 12 states of the successive-approximation conversion. I created a macro, called SAR, for the conversion and used one for each bit (**Figs 7** and **8**). The details of the macro are shown in **Fig 3**.

The conversion starts at the beginning of the T1 cycle, DAC data inputs are reset to a low state, except the MSB, which is set high. The correct analog-comparator input is multiplexed to the successive-approximation logic, and near the end of the T1 cycle, the global clock signal (GCLK) clocks in the comparator's output state. At the beginning of cycle T2, the next bit, DAC2, is set high, and driving the MSB remains in the state latched in at the end of T1. The conversion process continues in a similar manner through T11 and the 11th bit. The LSB is slightly different. Near the end of T12, the FPGA will write all 12 bits to the RAM. For this reason the data for the LSB comes straight from the comparator without being clocked into the flip-flop.

When in the playback state, the DAC receives data

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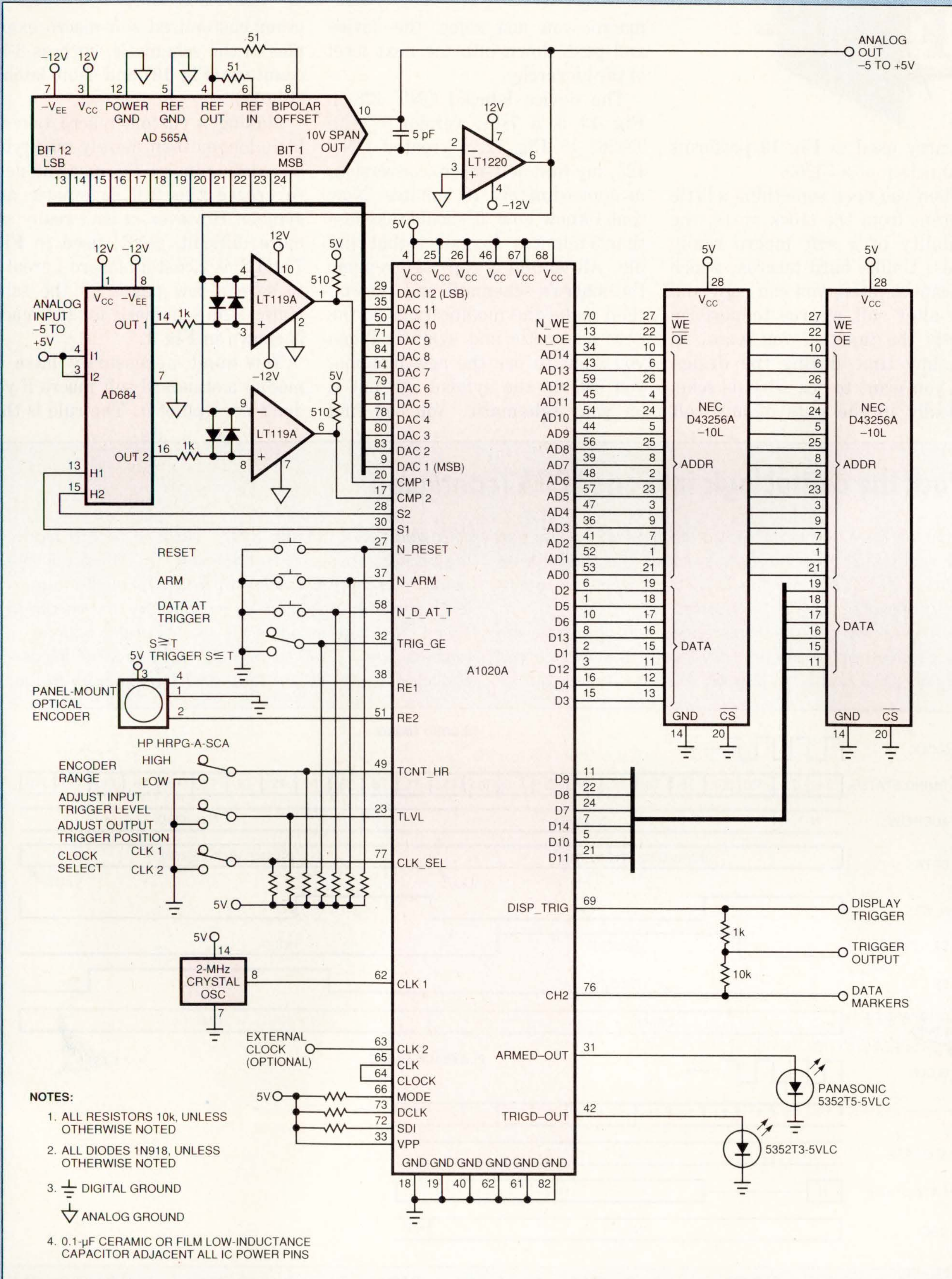


Fig A—The hands-on project was a record playback circuit.

ple carry used in **Fig 12** performs the function of a 74269.

When you need something a little different from the stock parts, the flexibility of a soft macro really shines. Unlike hard macros, which you cannot alter, you can copy and then alter soft macros to perform exactly the function you want. In fact, any time during the design that you want to see what is schematically in the guts of any soft macro, you just select the device and push down into the next level of the hierarchy.

The device labeled CNT 128 in **Fig 13** is a 7-bit version of the TA269 in **Fig 12**. I created CNT 128, my first soft-macro conversion, in approximately 10 minutes. Now that I know how, it should take less than 5 minutes. It really is that simple. All you do is copy and rename the macro's schematic and symbol, then make the modifications to the new schematic and symbol. When you want to use the new function, you call up the symbol and put it on your schematic. You can find other customized soft-macro examples in the schematic, such as 3-bit counters (**Fig 10**) and 7-bit latches (**Fig 12**).

Making a custom macro takes a little longer than merely modifying an existing macro because you need to create the full schematic and symbol. However, it isn't really any more difficult. SAR, used in **Figs 7** and **8**, is a custom macro I created to save a few pages on the schematic. The schematic for the macro is shown in **Fig 3**.

You don't necessarily have to modify a standard soft macro if you don't need all of it. The rule is that

Pack the digital logic into one FPGA *(continued)*

from the RAM and clocks it into the flip-flops at the end of cycle T12. A multiplexer switches the trigger-level setting (TL1-TL10) into the DAC input when the adjust trigger-level signal (TLVL) is asserted.

The 32k-word RAM stores conversion data from the successive-approximation conversion, plus two control signals (D13 and D14) (**Fig 6**). A 15-bit counter generates addressing for the RAM. While in record mode, the address counter is free running. The FPGA continuously writes the A/D results into RAM. When the trigger-level compare condition is satisfied by the incoming signal, the current value of the address counter is latched, the 15-bit up-and-down horizontal trigger-position counter is loaded, and the memory-trigger

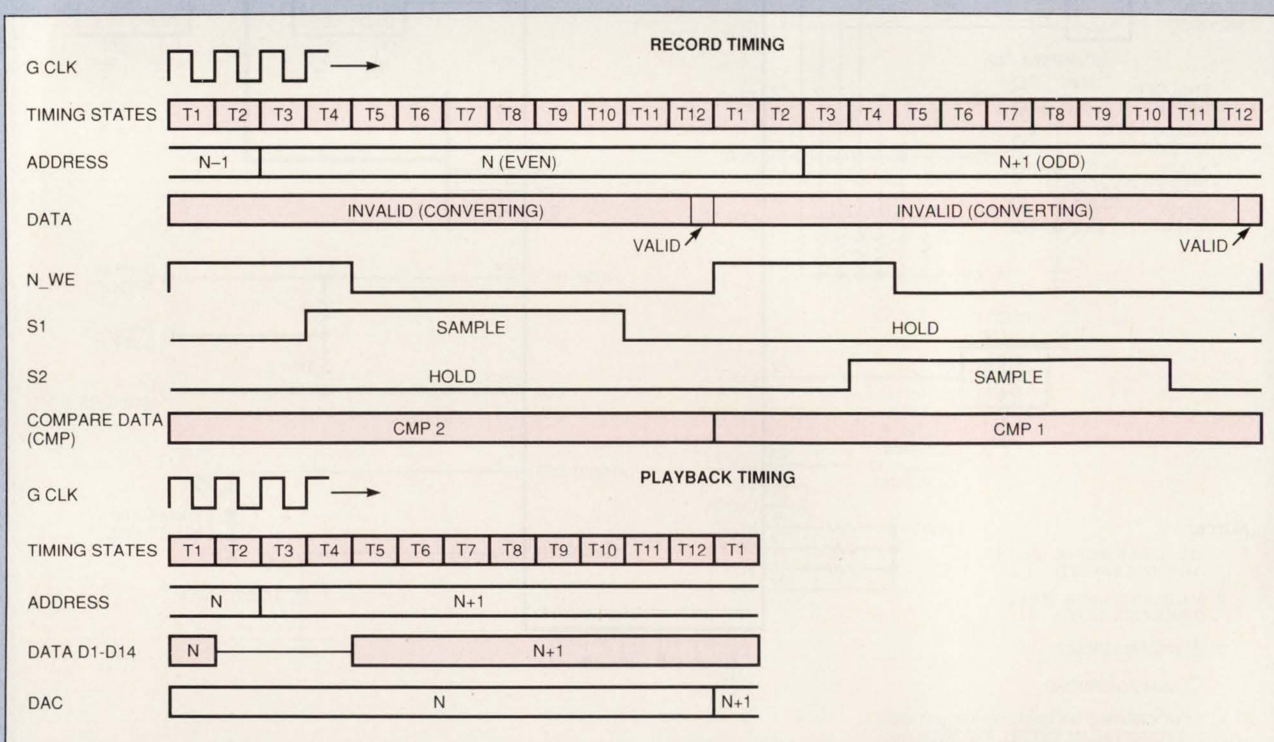


Fig B—At the end of each A/D conversion, the FPGA writes the data to RAM. During playback the FPGA latches data from RAM at the end of T12 to drive the DAC.

you can't leave any unused inputs—all inputs must be tied to a signal, V_{CC}, or ground. You may leave outputs unused; the software should remove any unnecessary logic associated with the unused outputs. The software will issue a warning whenever an output is unused, giving you a chance to verify that the omission is intentional.

You shouldn't tie unused inputs to V_{CC} or ground if it's possible to eliminate them. The flip-flops in **Fig 10** should be changed to macros without the preset. CNT4B on **Fig 6** loads all zeros. A more efficient design would just use a Clear and eliminate the load function on the counter. Even if the change doesn't result in a module savings, unnecessary inputs tied to power and ground restrict routing flexibility, which might affect the overall performance of the circuit.

Fan-out limits are perhaps the most noticeable change from standard TTL design. The software gives you a warning for more than 10 loads, and an error for more than 24. For the special cases of nets you designate as "fast criticality" (I'll discuss criticality in part 2), the fan-out limit drops to six loads. The only exception is the global clock signal. There is only one global clock signal on ACT 1 devices, and it can drive any number of loads.

On the surface, these fan-out limits may not seem too stringent, but you have to remember that macros are just a graphic convenience, no signal buffering occurs unless you put it inside the macro.

For example, the latch-control input of the 8-bit latch shown in **Fig 12** is eight loads, not one. You'll note a buffer in front of it. In fact, you'll see quite a few buffers scattered throughout the pages of the schematic.

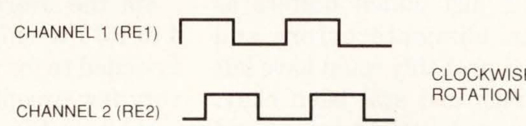
Buffers are easy to add, and the software errors and warnings tell

match condition (N_MEM_TM) is set up to stop acquisition after recording 24,000 more words of data, providing 8k words of pretrigger data. The FPGA writes the display-trigger match (DISP_TM) bit to RAM (D13) to mark the capture-trigger location during playback. N_MEM_TM is also recorded in RAM (D14) to mark the beginning and end of data.

During playback, the circuit compares the address counter with the 15-bit horizontal-trigger-position, up-and-down counter. When the two 15-bit words match the display, trigger-match condition (DISP_TM) is satisfied, and the display-trigger signal (DISP_TRIG) goes high for 12 clock cycles to drive an oscilloscope trigger. Initially, the circuit sets the horizontal-trigger position counter to the capture-trigger address. Subsequently, you may change it with the rotary encoder to trigger the oscilloscope at any address.

The address counter runs continuously during playback except when interrupted by one of two events:

- When the data at trigger signal (N_D_AT_T) goes low, the address counter is disabled the next time it reaches the display-trigger match and stays disabled until N_D_AT_T goes high. With the address counter disabled, the data going to the DAC is frozen so that the DAC continually outputs the voltage at the display trigger address. You can read the dc voltage on the analog output with a voltmeter.
- When D14 from the RAM goes low, indicating the end of the data, the address counter is disabled for 16 periods of 12 clock cycles each, before repeating the data. A high signal on the CH2 output provides a marker to use on an oscilloscope to indicate the beginning and end of data.

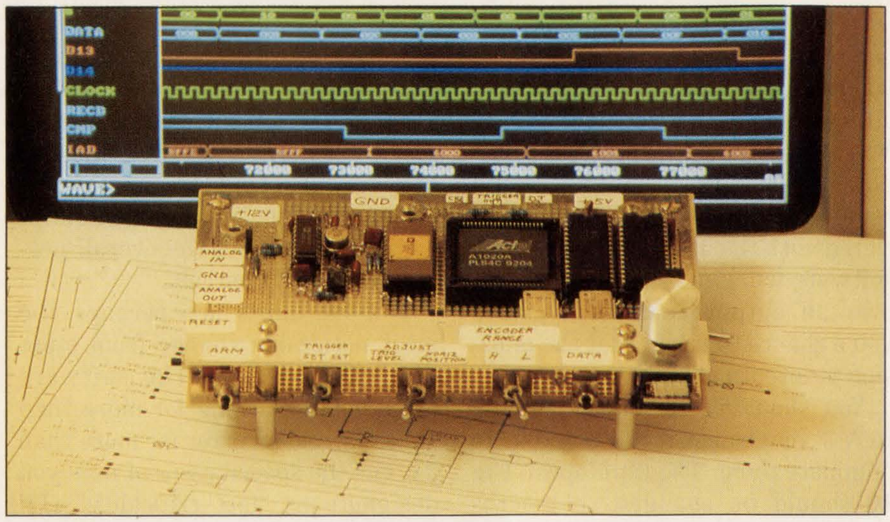


RE1	RE2	FUNCTION
0	0	COUNT
0	1	SET COUNT-UP STATE
1	0	SET COUNT-DOWN STATE
1	1	NONE

Fig C—The counter either counts up or down one cycle each time both encoder outputs are low. The count direction is determined by the previous state of the encoder.

Logic shown in **Fig 9** decodes the quadrature signals (**Fig C**) from the panel-mount, rotary, optical encoder (RE1 and RE2) into count-up and -down signals and count-enable signals. A panel-mount switch lets you select between adjusting the input-trigger level and adjusting the output horizontal-trigger position.

Because the horizontal-trigger position covers a 15-bit range (32k-word address) a high- and low-range select lets you count in increments of 1 or increments of 256 addresses. The rotary encoder provides 120 quadrature cycles per revolution, so using the low range you'd need to turn the knob 273 revolutions to scroll the full address range. Using the high range, you can scroll the whole range in just over one revolution.



Getting from a concept to a finished circuit using an FPGA requires learning new software. Even though all the software was new to me, I learned to use it effectively for this project in less than a week.

you where they are needed. Nonetheless, they are a minor nuisance and one of the few blemishes to what I consider a nearly ideal design environment. Of course, the addition of buffers should remain under the designer's control and not be made automatic because buffering is more than just a cosmetic change to the schematic.

Buffers require a module and add a module delay to the signal (In part 2, I'll discuss timing in detail). Letting module fan-out increase above the warning limit can cause large time delays too. For my particular design, the timing was not too tight, so I just added buffers as needed to eliminate errors and warnings. I probably could have left the warnings and still been okay. If your design has tight timing and you can't afford extra module delays, you can regenerate the signal.

For example, in **Fig 10** you'll find F_OUT and a buffered version F_OUT_A. Had this signal been timing critical, I could have cloned the preceding flip-flop to generate two identical versions of the signal without any additional module delays. The cost in this case would be an extra module because the flip-flop hard macro requires two modules, compared with the single module for the buffer. Also it means doubling the load on the flip-flop's input signals because they'll be driving two flip-flops instead of one.

On the overall schematics (**Figs 4 to 15**) I've only labeled nets where I needed to for design reasons, with very few exceptions. One exception is IA0 in **Fig 11**. It's labeled for simulation reasons I'll discuss in part 2. In future designs, however, I plan to label every net and every module. Although labeling takes time, it pays off when simulating, using the static timing analysis software, and reading error reports. I have to note that several people recommended labeling everything, and I ignored the advice. In the end, I didn't save any time by omitting the labels. You can take my advice or learn the way I did.

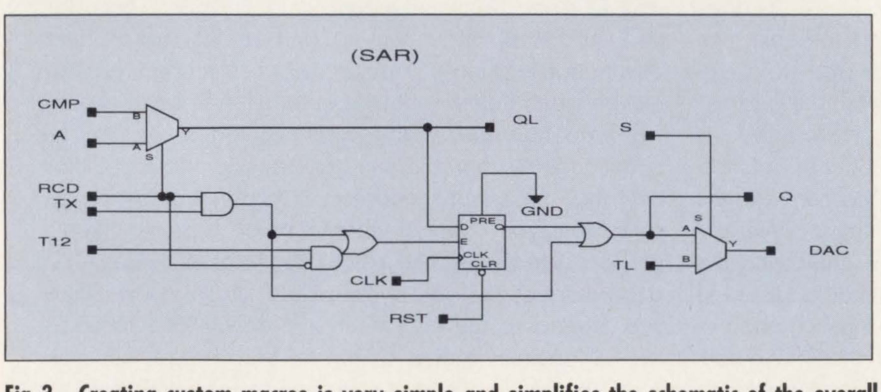
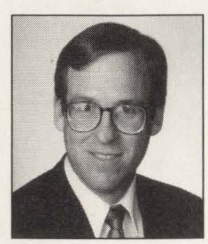


Fig 3—Creating custom macros is very simple and simplifies the schematic of the overall design. SAR is used in Figs 7 and 8 of the FPGA schematic. If you need to make changes to the design later, you need to change only the macro.

After reading this far you may have come to the conclusion that designing an FPGA is not much different from designing with SSI and MSI ICs. That's my conclusion too. I spent my time during schematic design battling with system design issues and how to improve the design, not fighting with tools or wondering if the clever use of a different MSI device would make a cleaner design. In part II, I'll show you some of the bugs I caught in simulation and two that I didn't catch until I tested the circuit. I'll also present you with the chronological account of the project so you can see how much time I spent in each step. EDN

Reference

1. Conner, Doug, "High-Density PLDs," *EDN*, January 2, 1992, pg 76.



Doug Conner is a technical editor for EDN based in California. You can reach him at (805) 461-9669.

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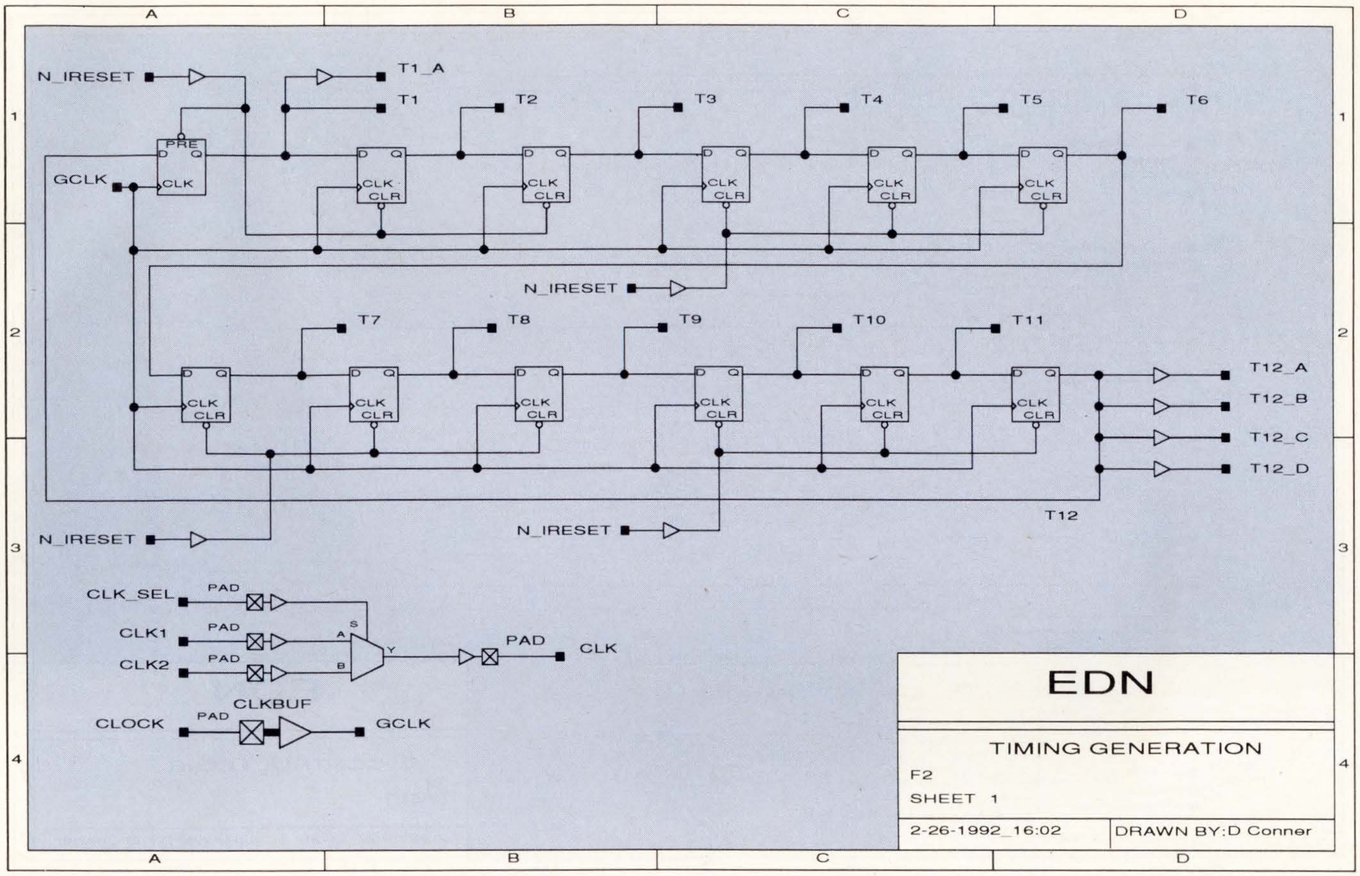


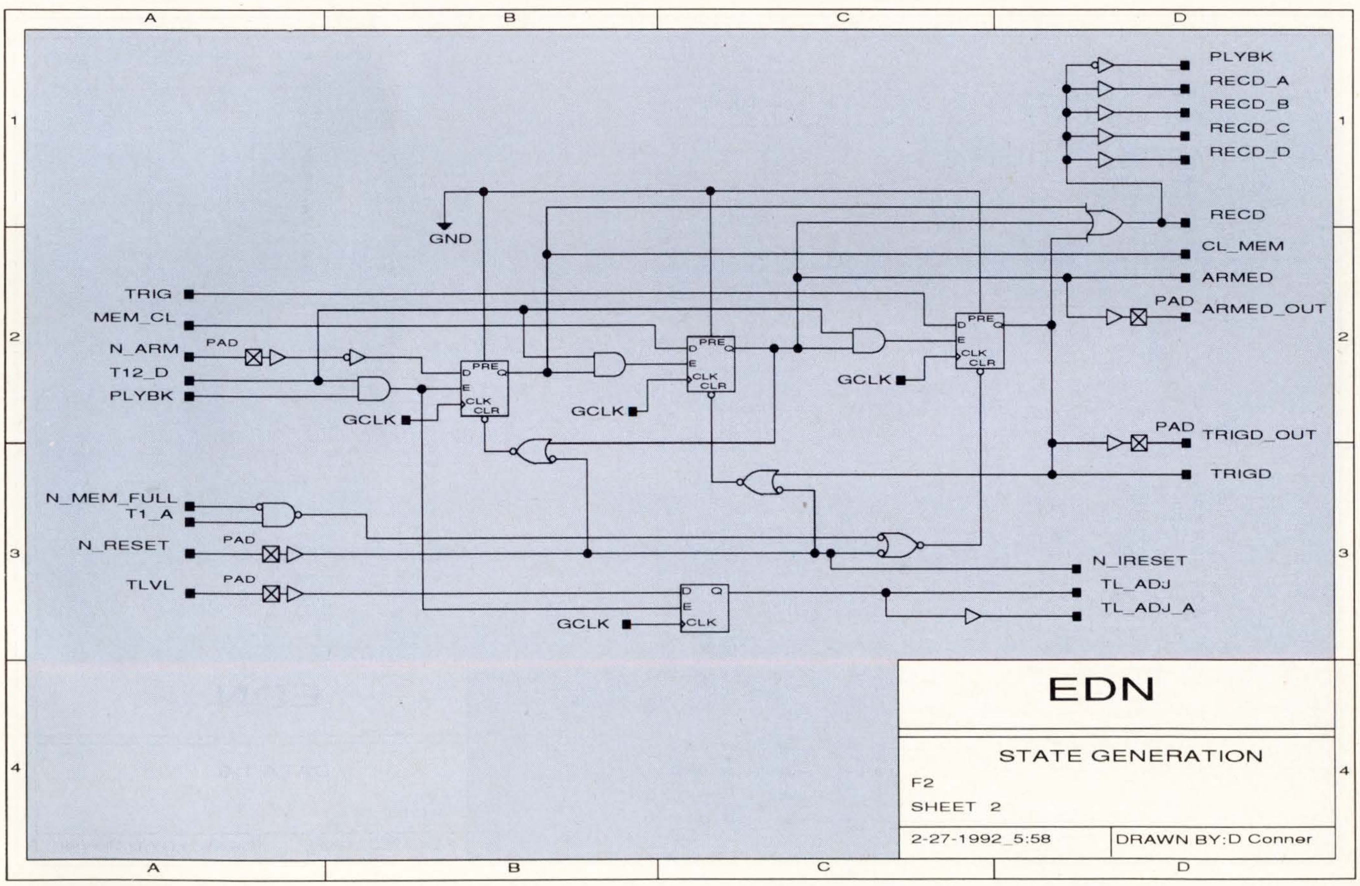
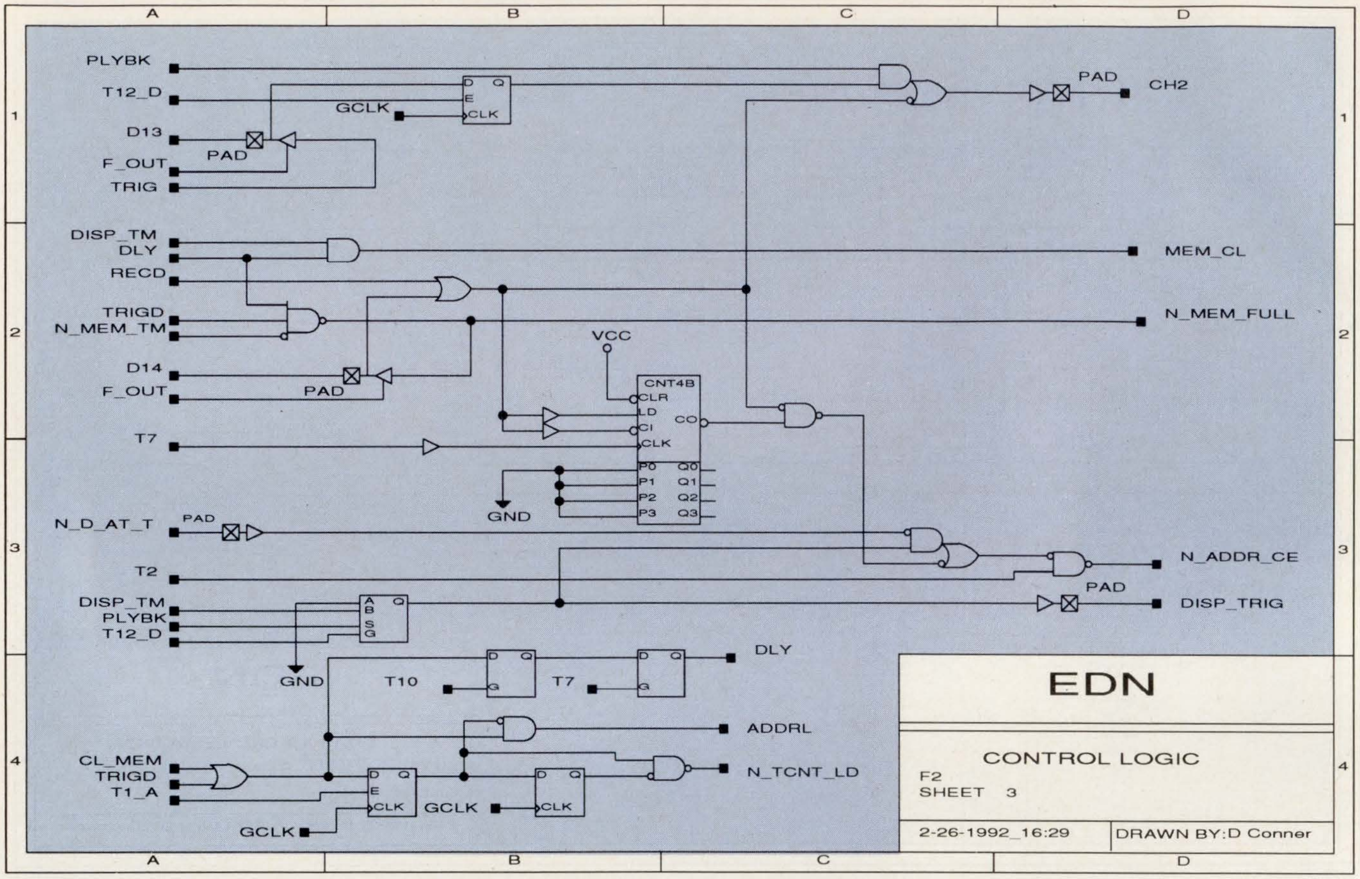


Fig 4 (top)—The schematic shows the logic for generating the 12 timing states used for all record and playback operations; Fig 5 (bottom) shows the logic for generating the playback state and the 3 record states: clear memory, armed, and triggered.



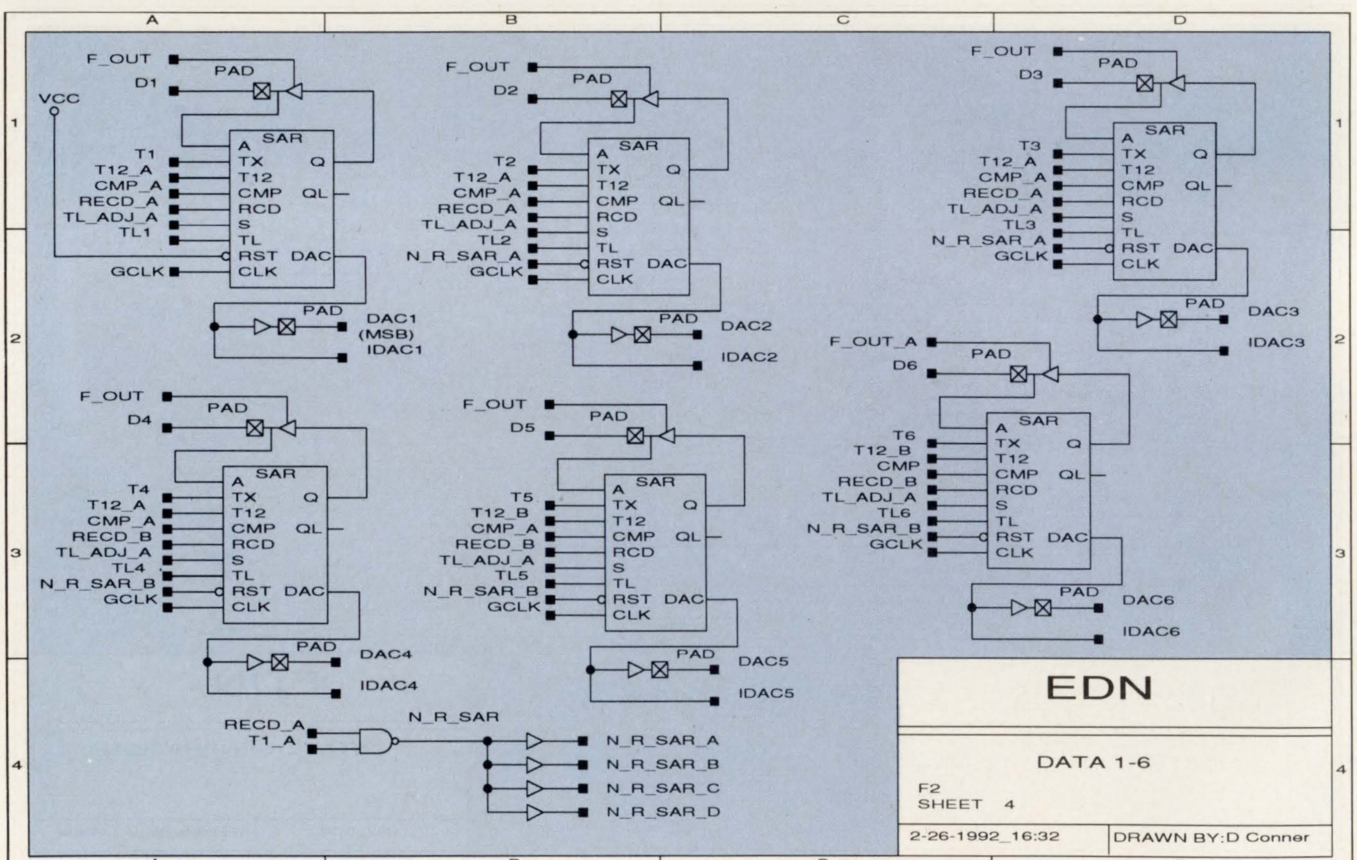
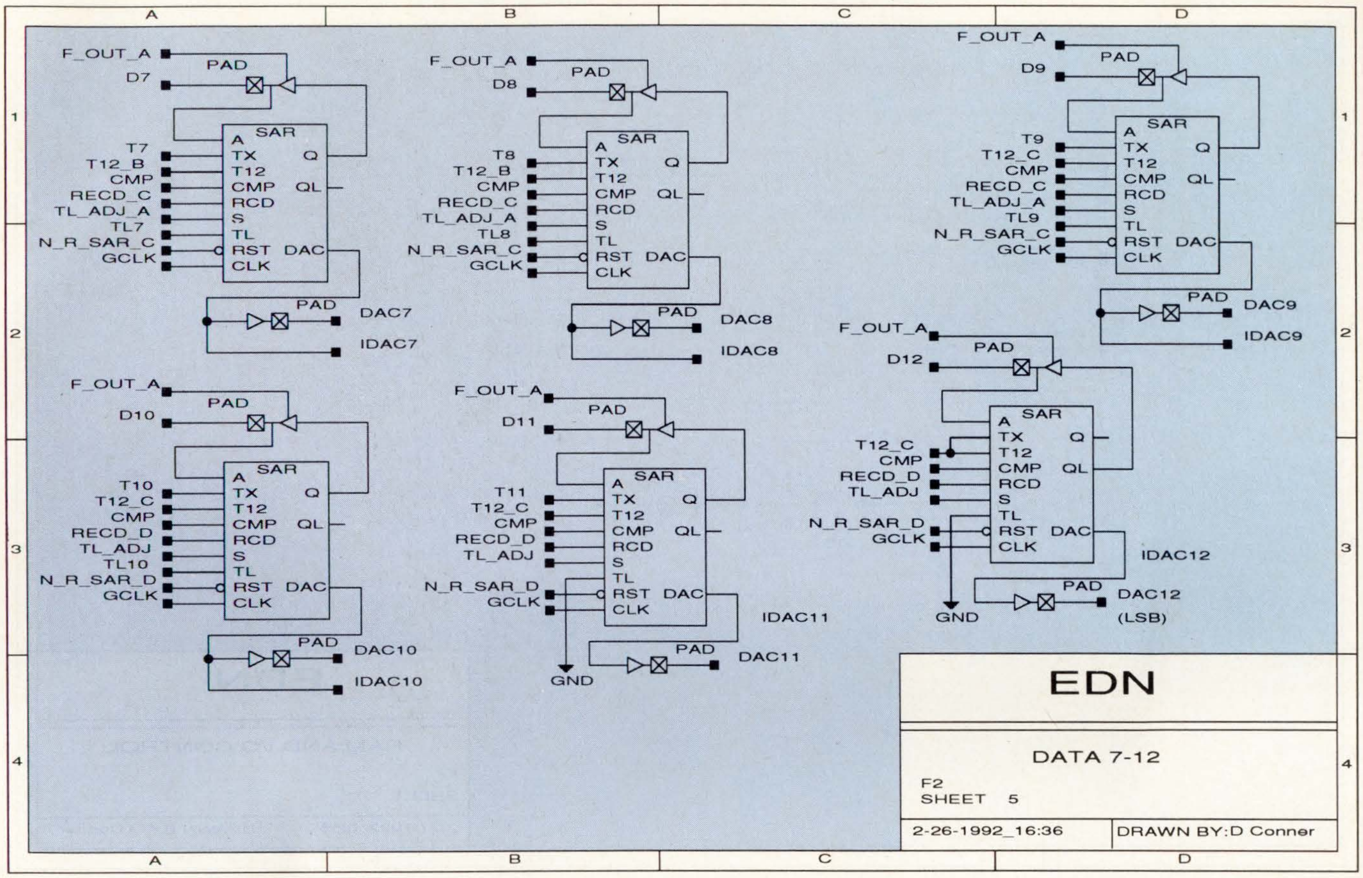


Fig 6 (top)—Logic for miscellaneous control functions is illustrated in this diagram; Fig 7 (bottom) shows the logic for the lower six data bits (see Fig 3 for SAR macro schematic).



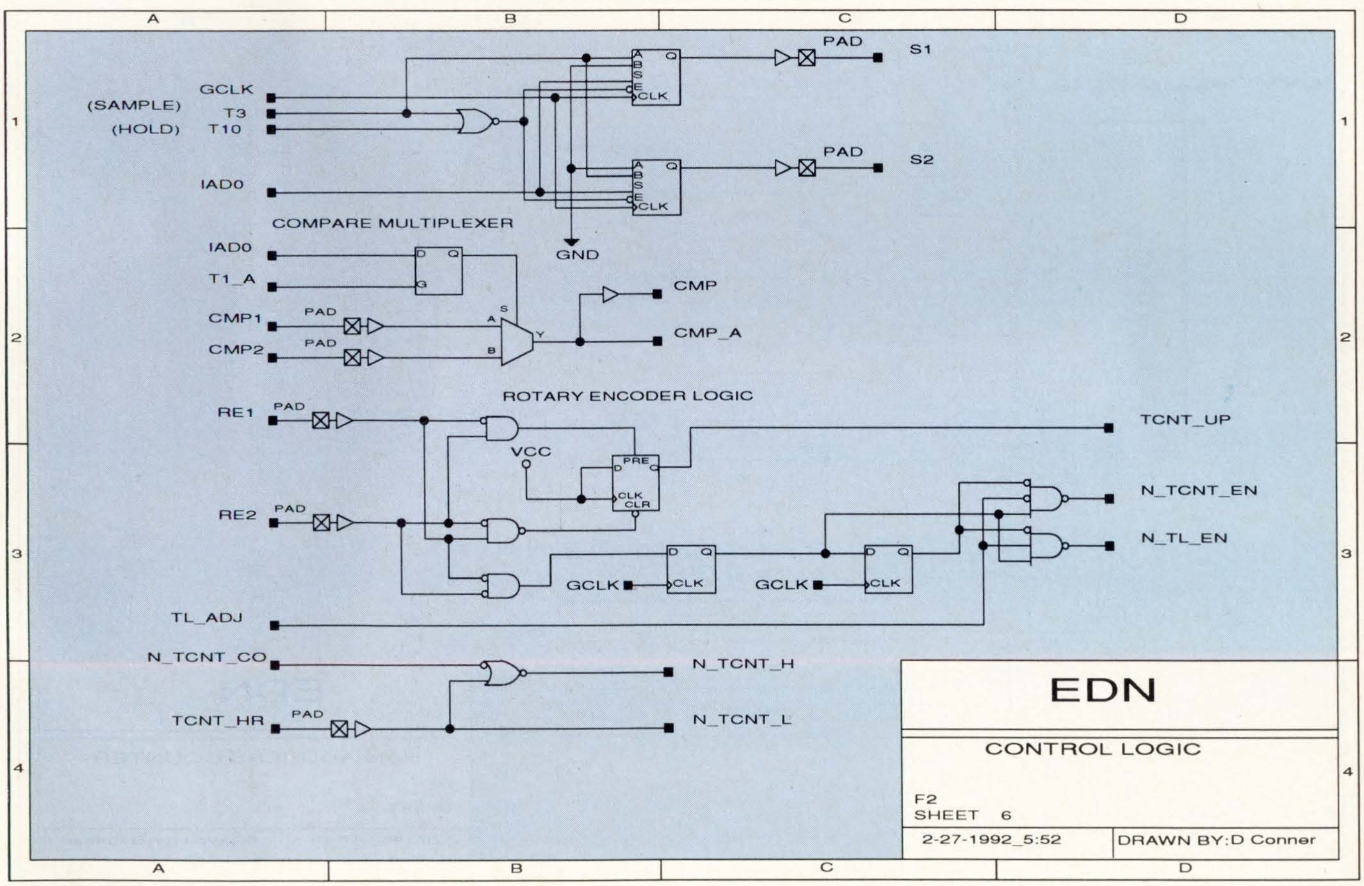
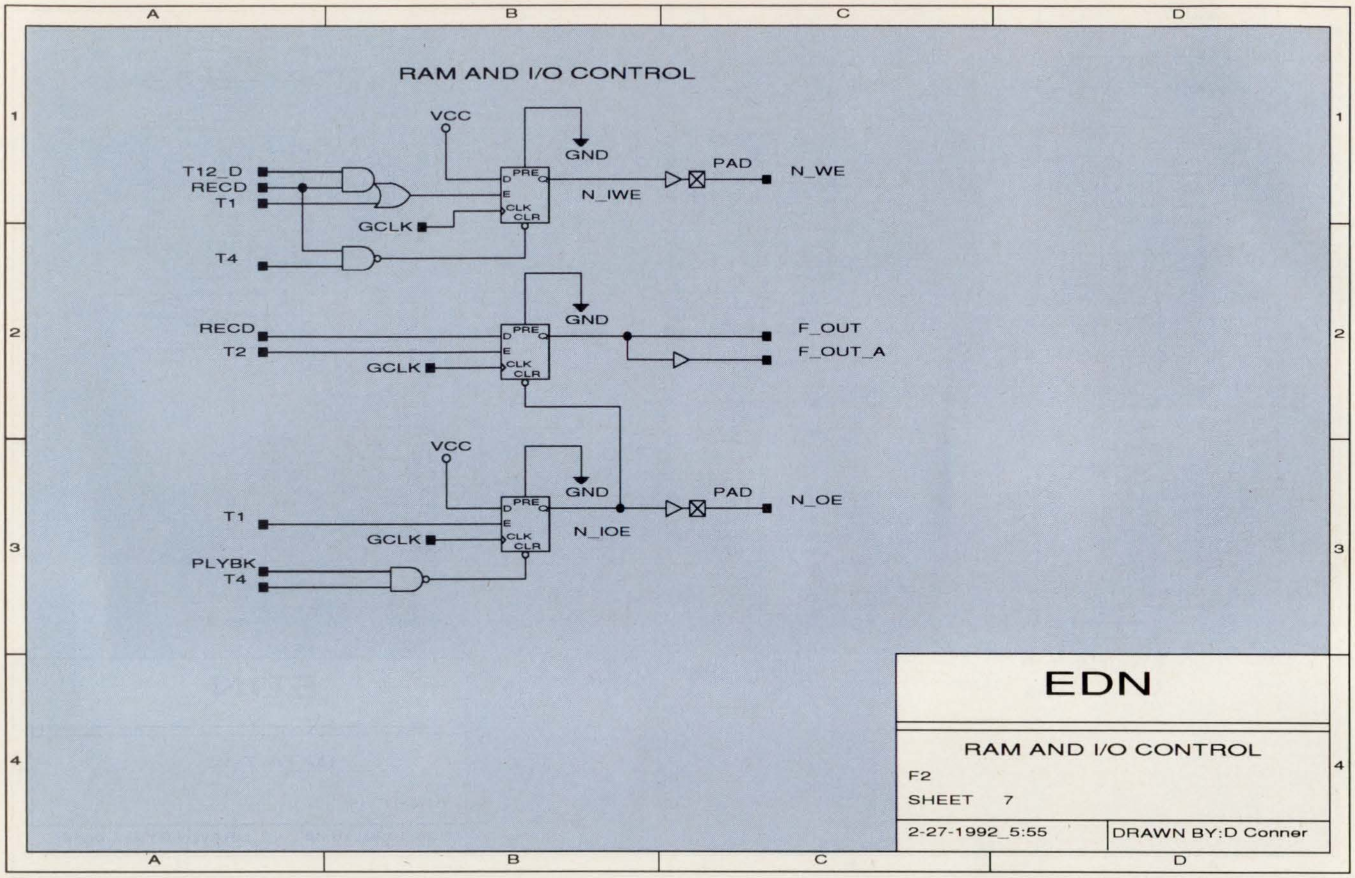


Fig 8 (top)—This schematic details the logic for the upper six data bits (see Fig 3 for SAR macro schematic); in Fig 9 (bottom), you can see the control logic for the S/H circuit, compare multiplexer, and rotary-encoder decode logic.



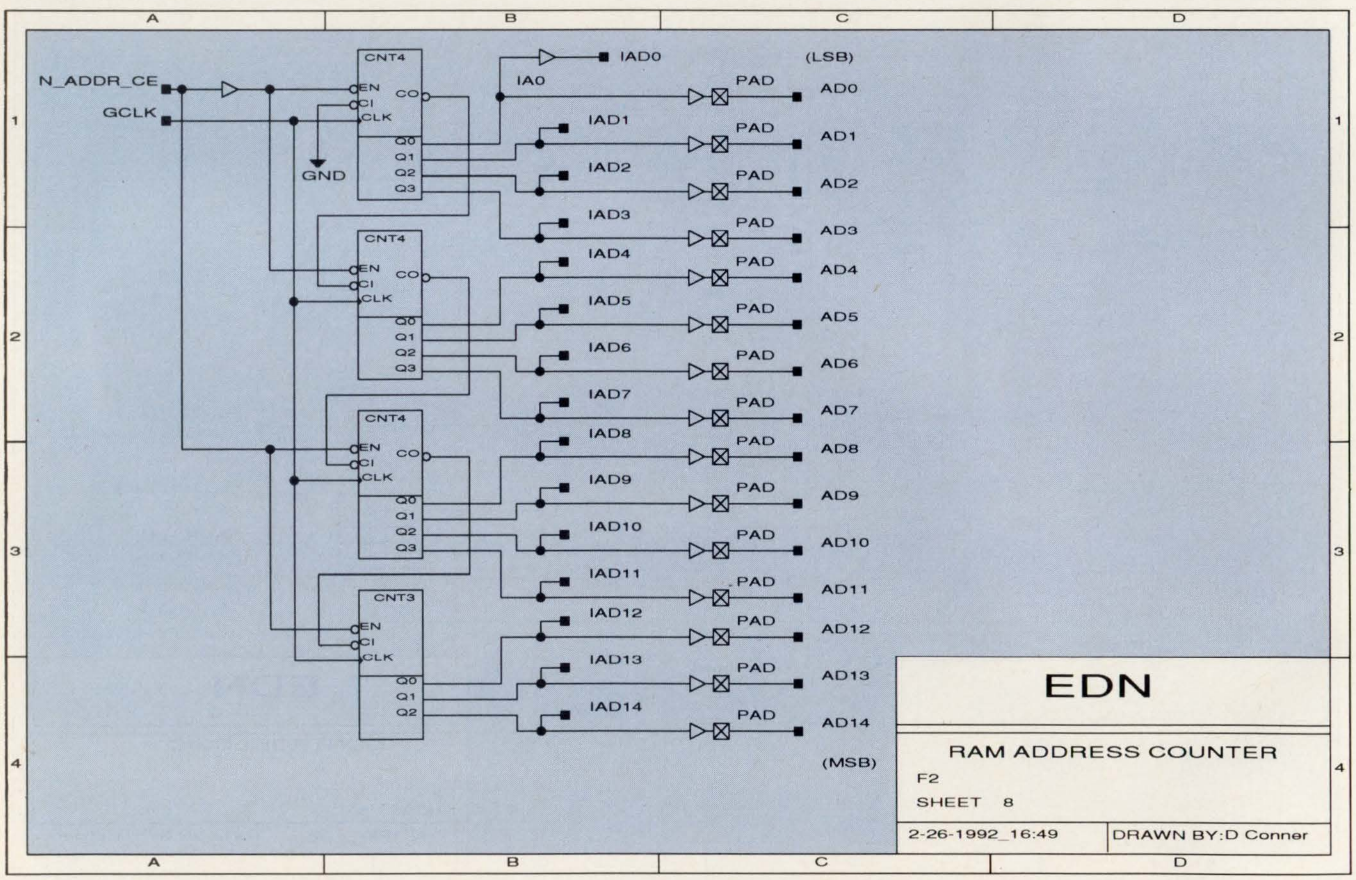


Fig 10 (top)—The schematic illustrates the write-enable and output-enable logic for the RAM and the output control for bidirectional data lines; Fig 11 (bottom) highlights the 15-bit counter for RAM address lines.

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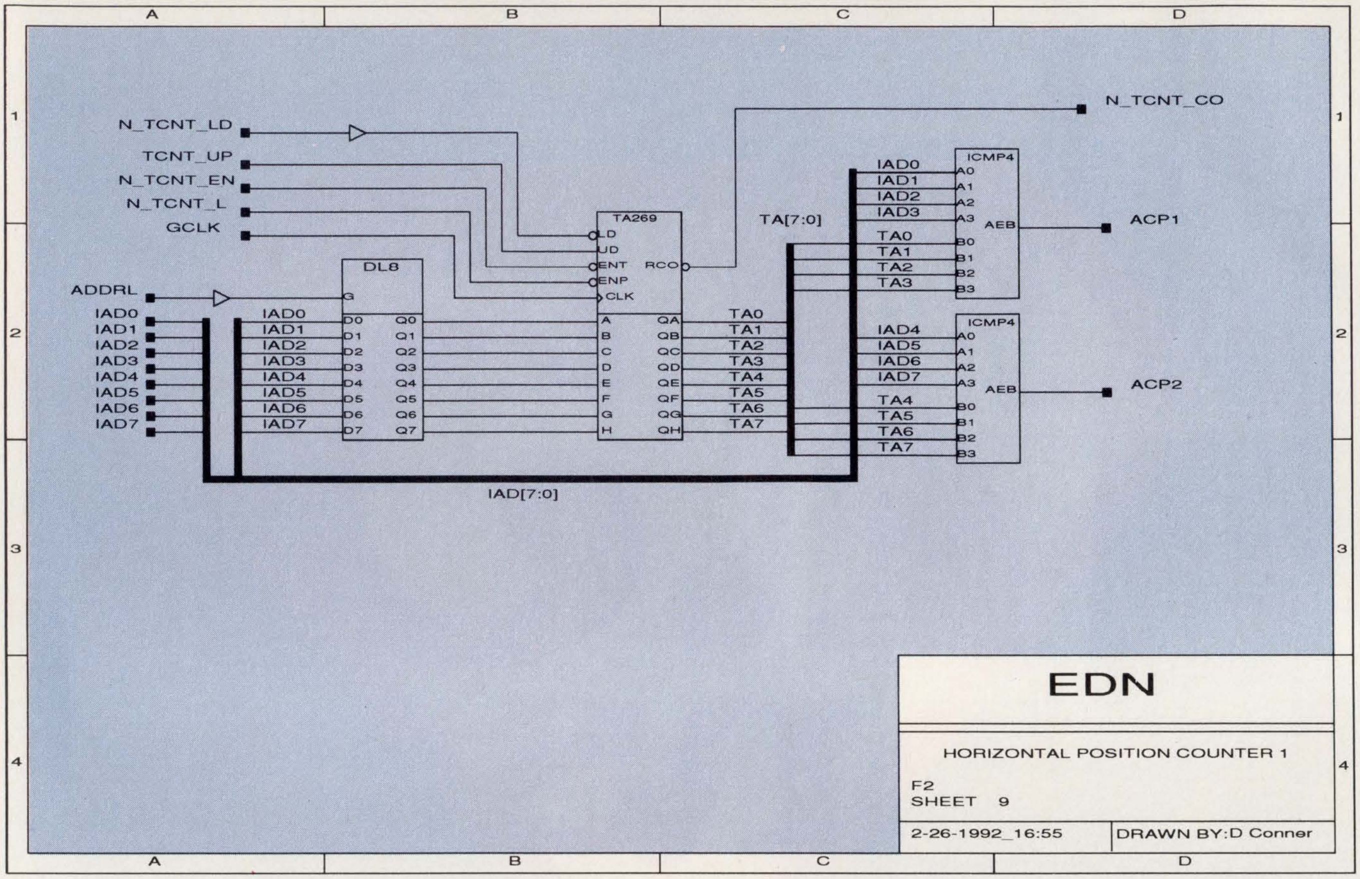

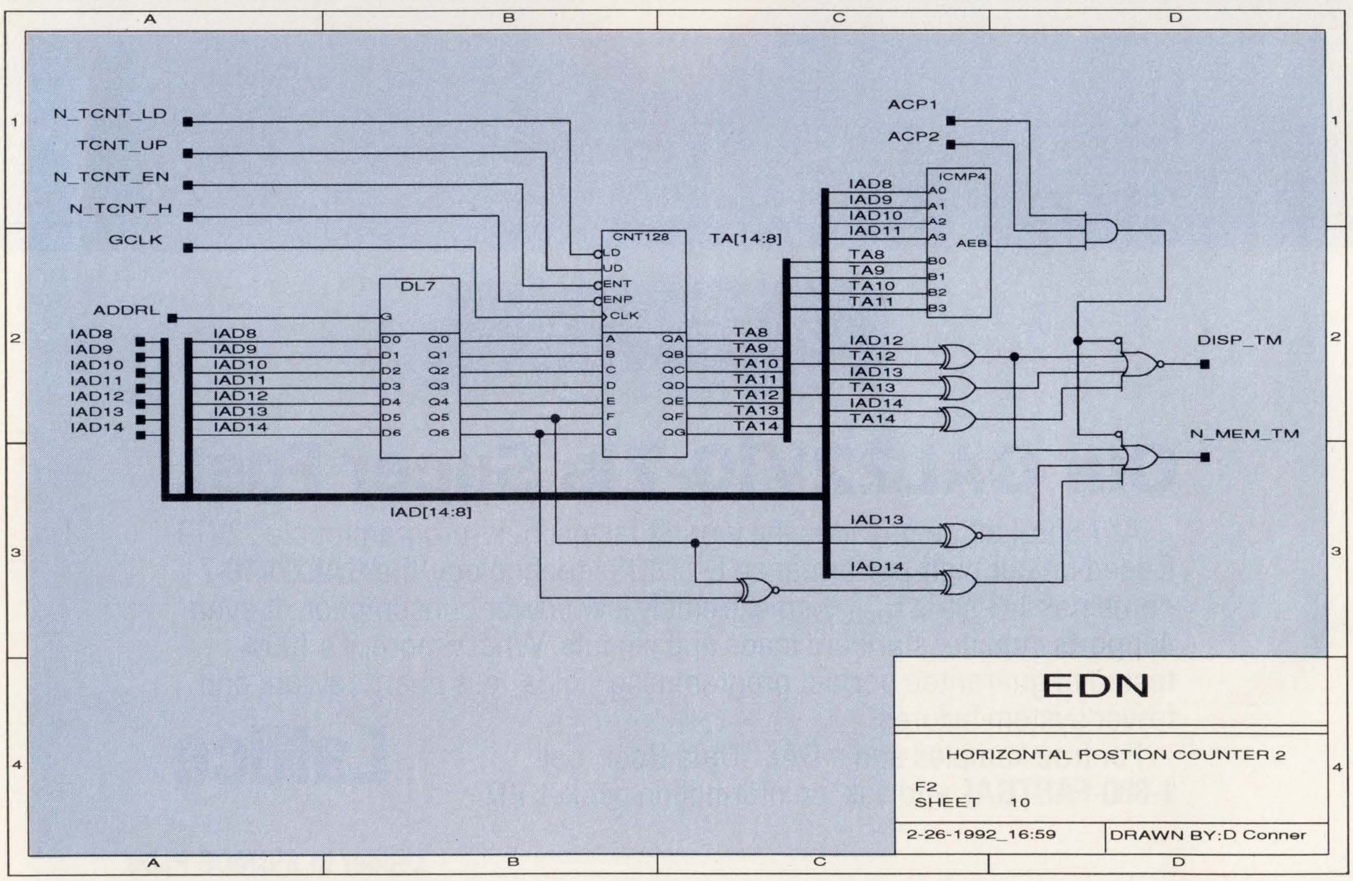

Fig 12 (top)—The lower eight bits for horizontal-output position control are illustrated here; Fig 13 (bottom) shows the upper seven bits for horizontal-output position control.

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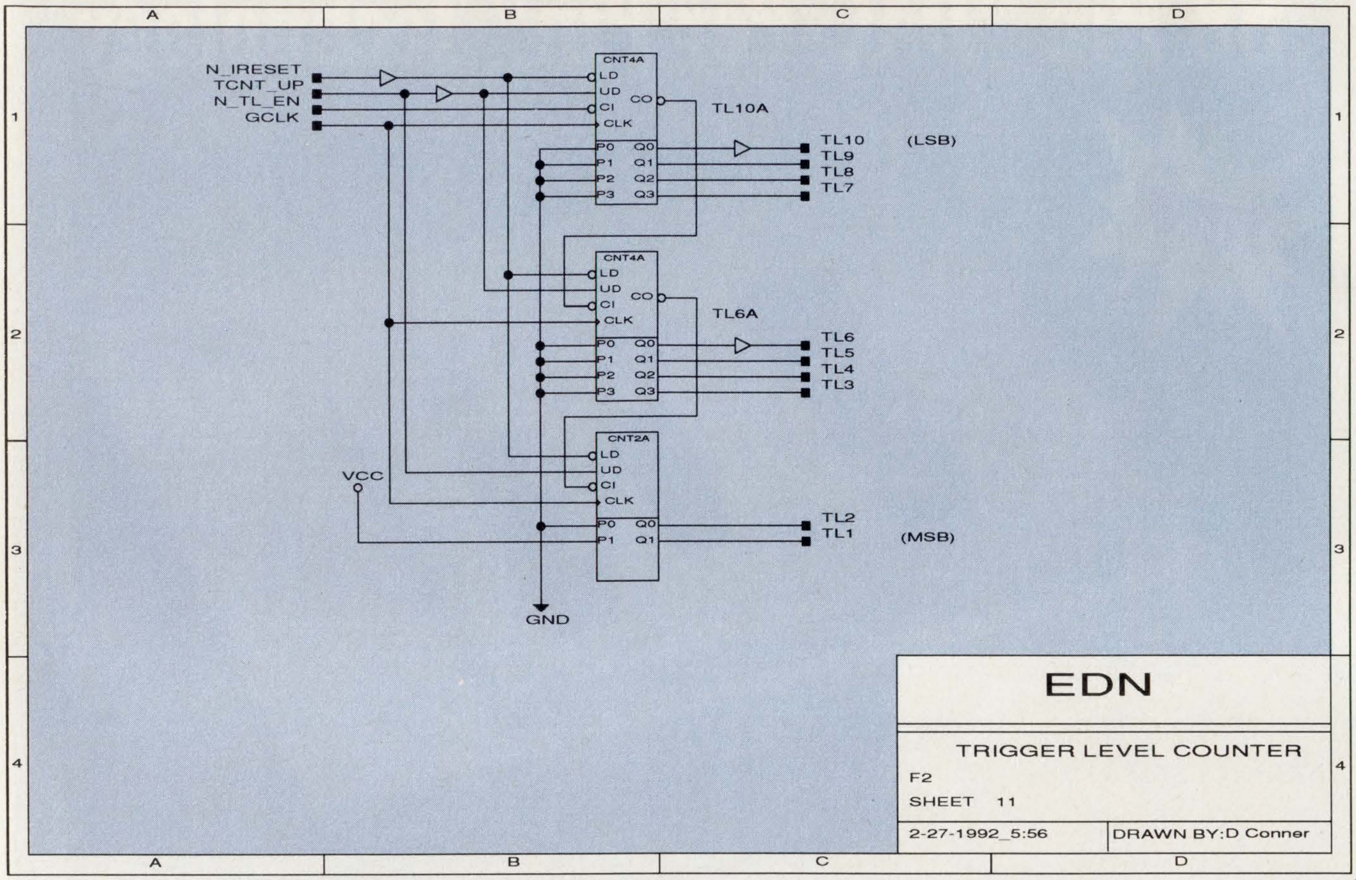

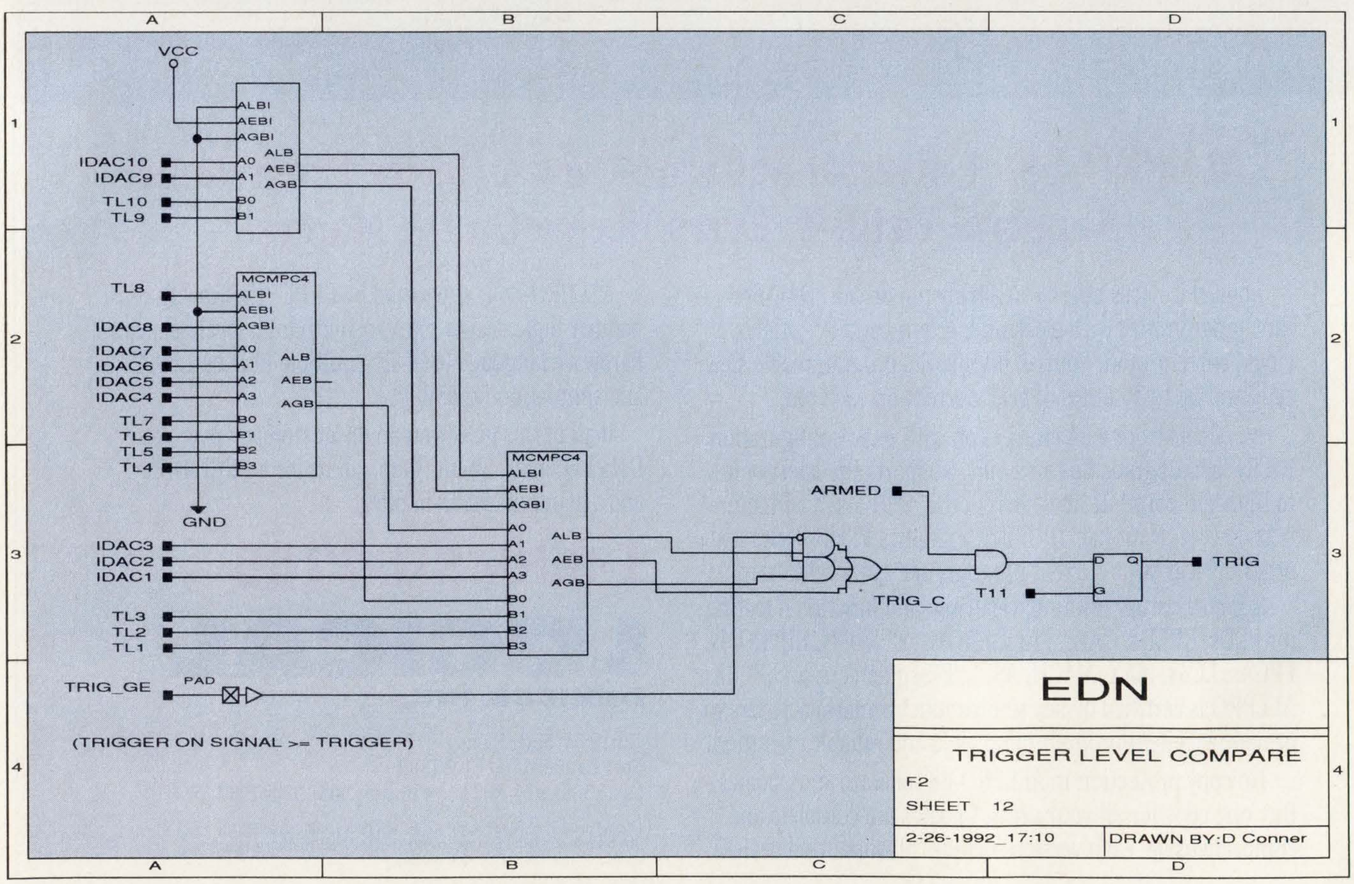

Fig 14 (top)—This schematic shows the 10-bit counter for setting the input trigger level; Fig 15 (bottom) illustrates the 10-bit magnitude-compare circuit for detecting the input-trigger event.

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	GM71C4100AL - 60 70 80	60 70 80	110 100 90	0.2	FAST PAGE MODE/ L-POWER	20 SOJ (300) 20 ZIP (400)
1M x 4	GM71C4400A - 60 70 80	60 70 80	110 100 90	1	FAST PAGE MODE	20 SOJ (300) 20 ZIP (400)
	GM71C4400AL - 60 70 80	60 70 80	110 100 90	0.2	FAST PAGE MODE/ L-POWER	20 SOJ (300) 20 ZIP (400)
1M x 1	GM71C1000 - 60 70 80	60 70 80	90 80 70	1	FAST PAGE MODE	20 SOJ, 18 DIP (300) (300) 20 ZIP (400)
	GM71C1000L - 60 70 80	60 70 80	90 80 70	0.2	FAST PAGE MODE/ L-POWER	20 SOJ, 18 DIP (300) (300) 20 ZIP (400)
256K x 4	GM71C4256A - 60 70 80	60 70 80	90 80 70	1	FAST PAGE MODE	20 SOJ, 20 DIP (300) (300) 20 ZIP (400)
	GM71C4256AL - 60 70 80	60 70 80	90 80 70	0.2	FAST PAGE MODE/ L-POWER	20 SOJ, 20 DIP (300) (300) 20 ZIP (400)

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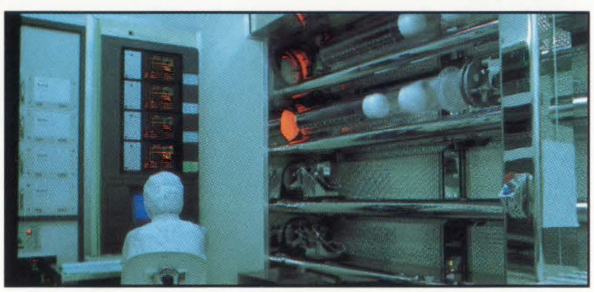

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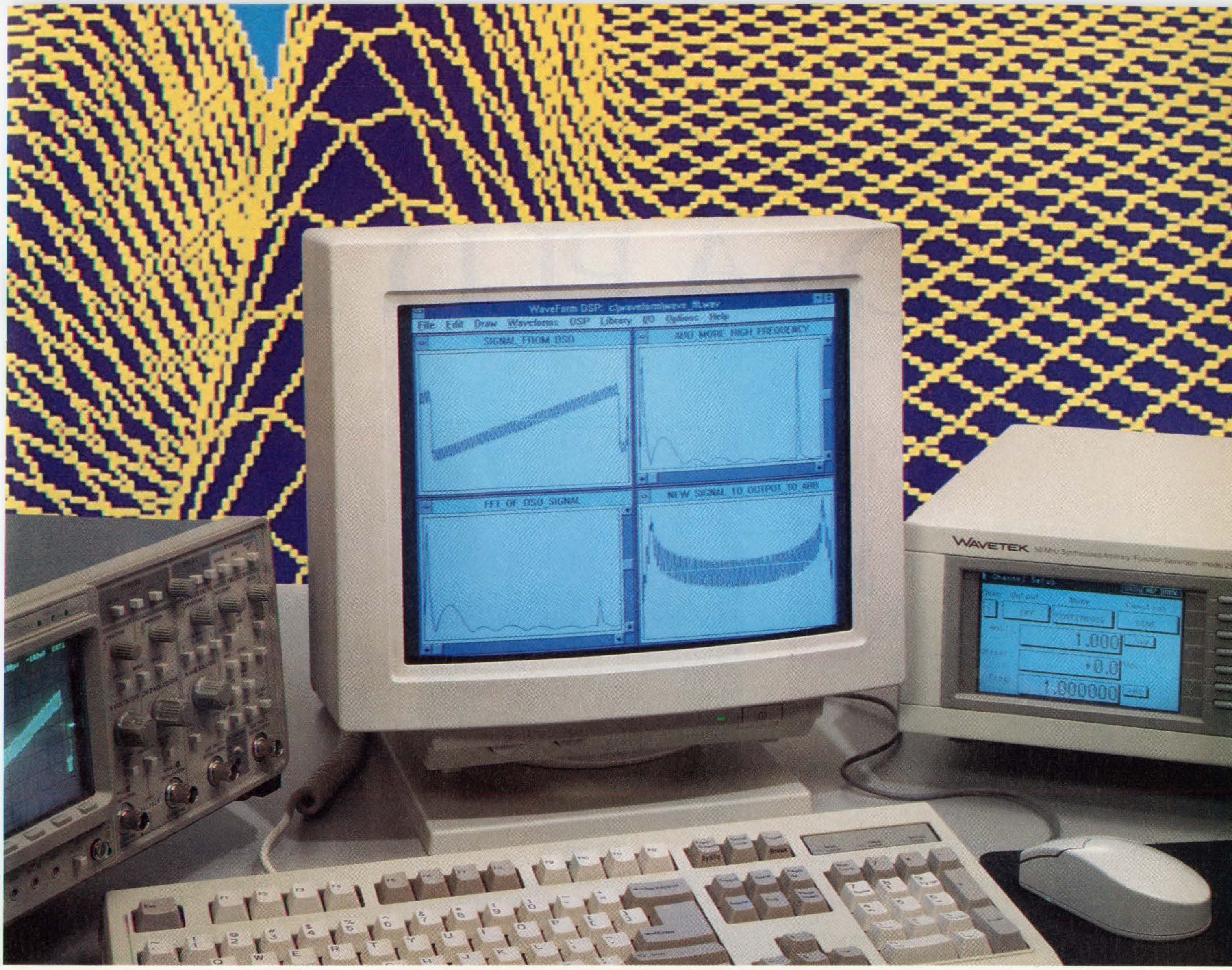

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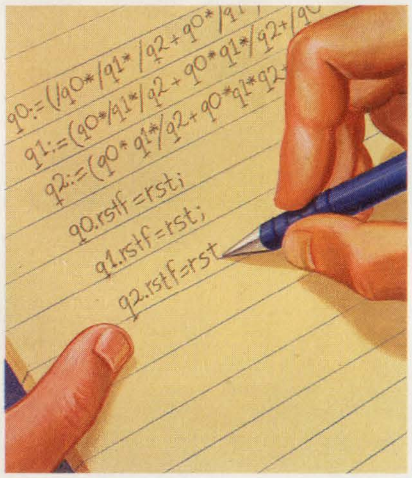

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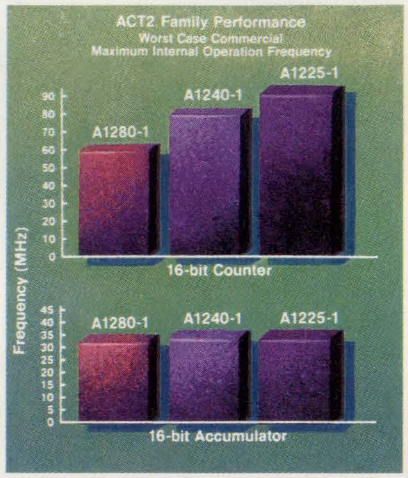

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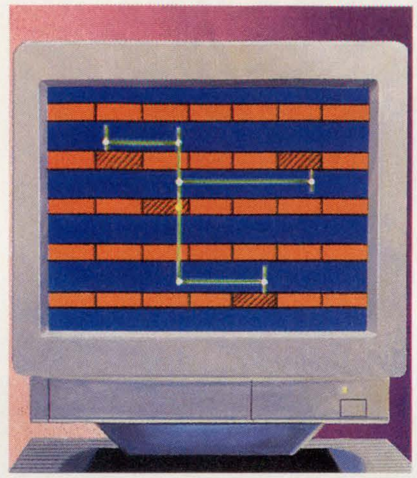

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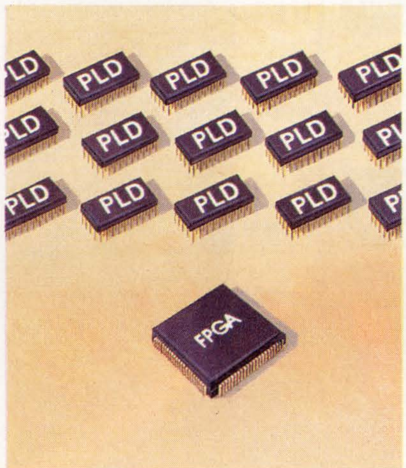

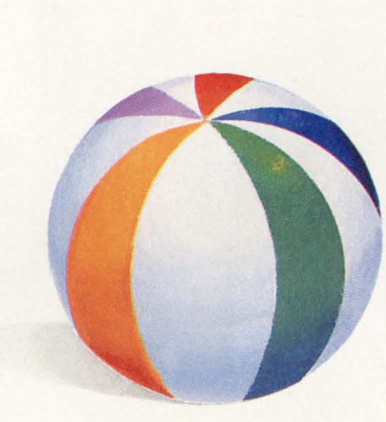

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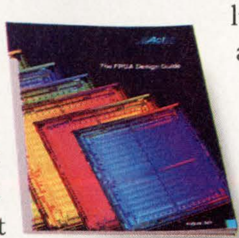

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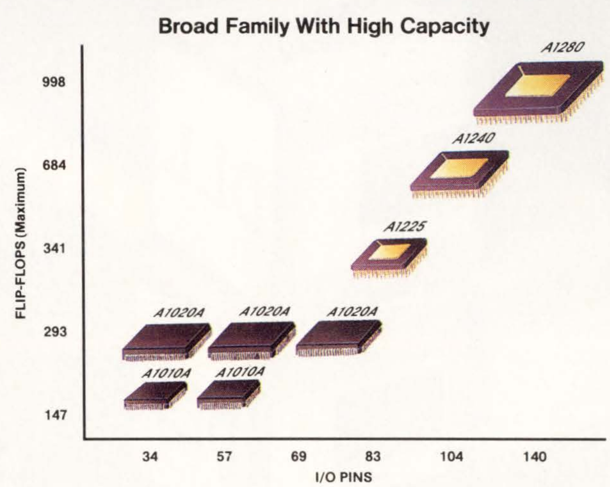

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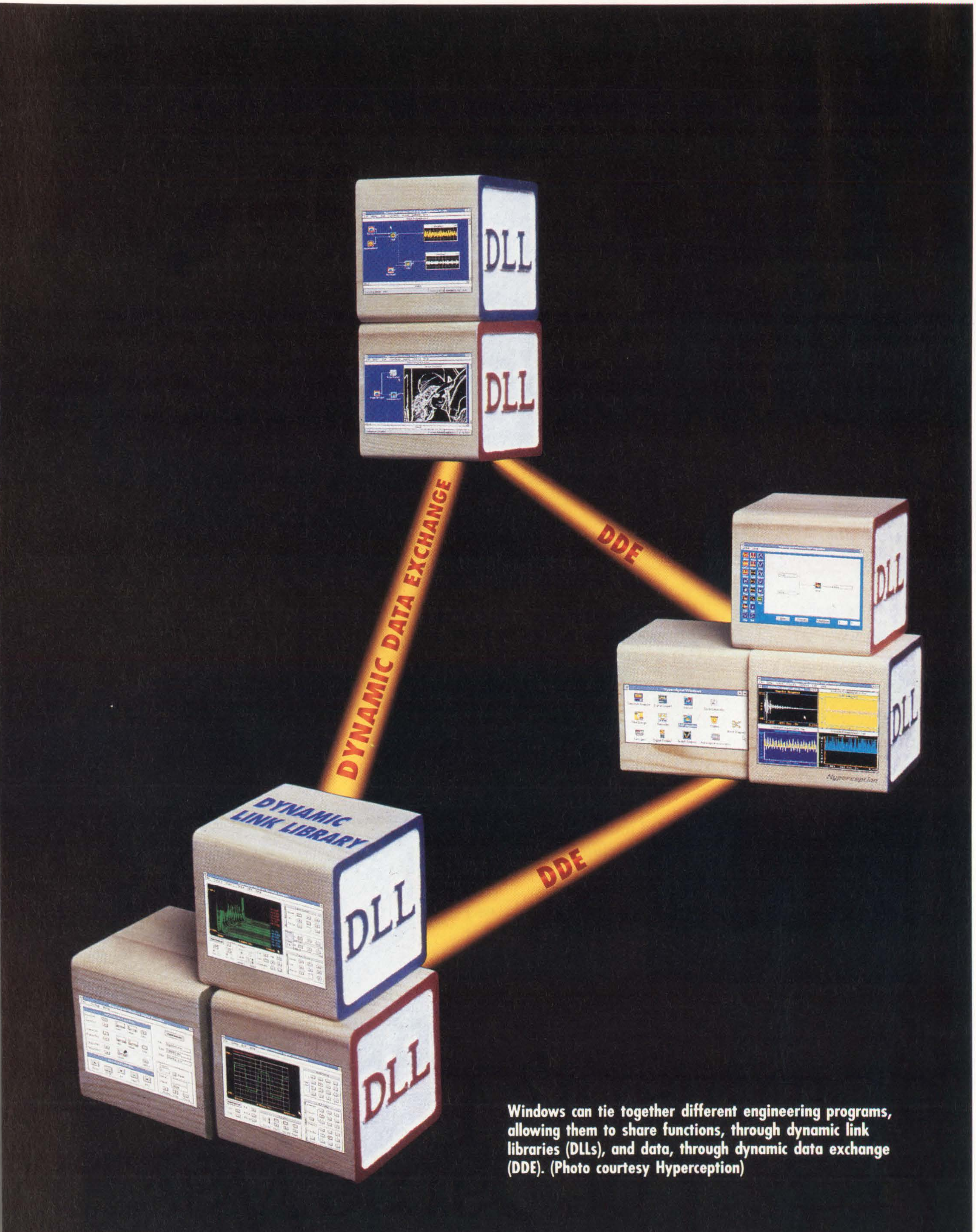


Windows can tie together different engineering programs, allowing them to share functions, through dynamic link libraries (DLLs), and data, through dynamic data exchange (DDE). (Photo courtesy Hyperception)

Windows and engineering software

Suddenly, powerful, fast 386/486 PCs tagged with breathtakingly low prices are here. These PCs have more than enough horsepower to run formidable engineering programs under a multitasking, virtual-memory operating system. The question is, does Windows 3.X have what it takes?

Charles H Small, Senior Technical Editor

As Microsoft keeps telling us, millions of PC users have bought copies of Windows 3.X, making it, in terms of units sold, the most popular multitasking operating system in the world. But by the same reckoning, DOS's EDLIN is then the most popular word processor in the world. Whether many people who have bought those copies actually run Windows is open to question. Certainly, engineers have had little use for Windows until recently because few engineering programs were available in Windows versions.

That lack of Windows engineering software is changing rapidly. So rapidly, in fact, that any list EDN could compile and publish would be obsolete the day it appeared in print (**Ref 1**). Rather than offering a list, this report will look at Windows' facilities and how those facilities suit—or do not suit—the kinds of programs engineers run. In other words, is Windows really all the multitasking, virtual-memory operating system that engineers require for their new 386/486 PCs?

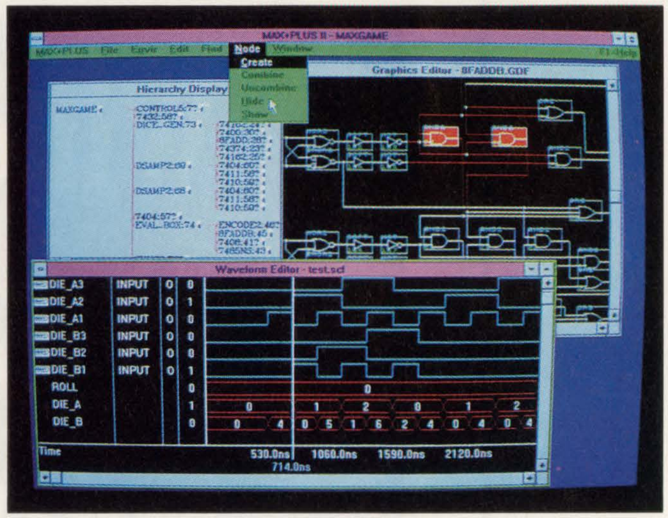
The new inexpensive 386/486 PCs are attractive because engineers want to run software that will share some or all of the following characteristics:

- Large programs
- Large data sets
- Computationally intensive
- Memory intensive
- Graphics intensive
- Multitasking
- Networked
- Real time.

Large, computationally intensive programs that crunch large data sets include circuit simulators, pc-board and FPGA autorouters, math programs, and compilers. Memory- and graphics-intensive programs include drafting programs, which typically have huge databases of devices and must manipulate large files to show detailed graphics displays. Also, engineers increasingly are abandoning textual-programming methods for diagrammatic-programming systems, which rely on graphical user interfaces (**Ref 2**).

Multitasking is not an obvious aspect of engineering software. Until now, most engineers who have been working on PCs have not been able to do much multitasking because early PCs could barely run one engineering program at a time. Only with the advent of 386/486 PCs and suitable multitasking systems, such as Windows and Desqview, has multitasking become a workable possibility for engineering PC users. When engineers find that they can simultaneously print out a complex drawing, compile a program, and still be able to draw schematics or prepare documentation on their 386/486 PCs, they will wonder how they ever got along without multitasking.

The ability to multitask engineering programs and the low cost of 386/486 PCs could challenge the conventional notion that PCs are good for only simple tasks such as text or schematic entry and that real computation has to be uploaded to a powerful central computer. Note that workstation and mainframe makers are, not surprisingly, the strongest advocates of the uploading strategy. Some engineering shops may find that they can get adequate performance from a network of multitasking 386/486 PCs.



Running under Windows, this PLD design tool from Altera Corp can show multiple design-entry windows and the resulting PLD file simultaneously.

Rating Windows

How does Windows measure up as a multitasking operating system working within a network? For starters, a simple, concrete definition would be useful. Windows is a 16-bit, protected-mode operating system that lacks file I/O. Windows' code runs the user interface and manages memory and most of the computer's interrupts. Windows relies on DOS to manage timer interrupts and passes file-handling commands to DOS for execution. Future versions of Windows will dispense with the remnants of DOS altogether.

Windows has unique mechanisms for managing several large programs at once. These mechanisms are faster and more economical than those of some supposedly sophisticated operating systems such as Unix. Windows is not only a multitasker, but also has several unique mechanisms for exchanging data and control among multitasked programs. Furthermore, Windows has networking and support for printers and plotters built in.

For real-time I/O functions, such as controlling instruments and gathering data, the picture is not especially rosy. Windows has to contend with the PC architecture, which does not have the world's greatest external-interrupt mechanisms and DMA hardware. Furthermore, Windows grabs all the interrupt vectors in a PC, interposing extra processing for interrupts. And because Windows operates as a virtual-memory system, it necessarily fragments a given application's memory map, making DMA an even trickier task.

In relation to memory, Windows is really a kind of "DOS extender;" it gives programs access to a much larger address space than the total 1 Mbyte that DOS can get at. (Curiously, even though Windows allows a program to access vast expanses of virtual memory, it does not yet support 32-bit programs.)

But Windows is *not* the only way a PC program can get access to that extra memory. Until the advent of inexpensive 386/486 PCs and Windows 3.X, vendors of engineering software have, quite reasonably, chosen another route to exploit the resources of 386/486 PCs: the so-called DOS extender (**Ref 3**). A DOS extender shifts the 386/486 μPs from real mode to protected mode and, unlike Windows, kicks off a *32-bit*, protected-mode program. Then the extender lurks in the background, capturing DOS calls from the program, slipping briefly into real mode so that DOS can perform the requested calls. Even today, some vendors still prefer using DOS extenders.

Much of the new PC's flexibility comes from the chameleon-like 386/486. (As far as Windows is concerned, a 486 is just a faster 386. For compilers, the differences between the two processors are significant because the 386 and 486 execute similar instructions in differing numbers of clock cycles, altering optimization strategies and instruction choices.) To help alleviate confusion that the 386/486 μP's myriad modes can engender, **Table 1** sorts out various common software systems that use different features of 386/486 μPs.

What Windows means to programmers

Windows comes with a host of built-in functions for managing a multiwindowed graphics interface. It also comes with an excellent built-in on-line help facility. In fact, Windows provides so many built-in features—device drivers, graphics objects, etc—that programmers have to write less code for a Windows program than for a DOS program. Ironically, Windows versions of programs tend to cost substantially more than equivalent DOS versions. Also, built-in functions don't necessarily make programming for Windows a breeze.

Much of what you will hear about Windows, both good and bad, comes from programmers who are learning to write programs under Windows. This task presents a steep and torturous learning curve for both experienced DOS programmers and experienced Unix programmers. Yet managers of both types of programmers are flogging their galley slaves in an effort to get Windows versions out as soon as possible. Do not let the cries of anguish from below decks harden your heart against Windows.

The reason for the wailing and gnashing of teeth from former DOS programmers is not so much that they must learn a mountain of new Windows operating-system calls **(Ref 4)**. DOS programmers' are in distress because they have to forgo years of hard-won DOS lore. This lore consists of innumerable tricks, "undocumented" DOS calls, workarounds, and bug fixes **(Ref 5)**. The saga of the terminate-and-stay-resident (TSR) program illustrates "clever" DOS programming in its most odious form.

DOS is, in essence, a simple program loader. It can stack programs in memory, one atop another, until they bump into the notorious 640-kbyte barrier. DOS can run only the program on the top of the stack. At one point in the distant past of DOS's evolution, Microsoft decided it needed a "print spooler." That is, it needed a little program that would keep feeding bytes to a printer while a word processor went on with other jobs. How to pull off such a feat in a single-tasking computer?

Tales from the undocumented-DOS-calls crypt

Microsoft's answer was to add some "undocumented" (that word should strike terror into the heart of any hapless PC user) DOS calls that a knowledgeable programmer could use to fix a small interrupt-driven routine in the high end of the 640-kbyte DOS program space. Of course, having a routine simply stay in memory accomplishes little more than taking up memory. To actually do useful work, the little program would have to lay some cuckoo's eggs in other routine's nests. The TSR for, say, printing, would vacuum up the contents of the interrupt registers associated with printing and then put its own address into that register. When printing interrupts occurred, the TSR would respond

Table 1—Software usage of 386/486 architecture

Function	Software	386/486 modes used	Comments	Manufacturer	Circle no.
Operating system shells	Windows 3.0 Real	Real mode	Not able to run most Windows applications	**Microsoft** Box 97017 Redmond, WA 98073 (206) 882-8080	650
	Windows 3.1 Standard	16-bit protected, real mode	Not able to run DOS applications in a window		651
	Windows 3.1 Enhanced	16-bit, 32-bit protected mode, V86 mode, paging	Windowed multitasking of DOS applications, virtual memory support		652
	Desqview 386	32-bit protected mode, V86 mode, paging	Windowed multi-tasking of both DOS and 32-bit DOS extended applications	**Quarterdeck Office Systems** 150 Pico Blvd Santa Monica, CA 94045 (213) 392-9851	653
Memory managers	386 Max QEMM 386	32-bit protected mode, V86 mode, paging	Allows device drivers to be relocated to unused memory areas above 640 kbytes	**Qualitas Inc** 7101 Wisconsin Ave, Suite 1386 Bethesda, MD 20814 (800) 733-1377	654
				Quarterdeck	655
DOS extenders	386/DOS Extender	32-bit protected mode, V86 mode, paging	Allows 32-bit applications to run on top of DOS. 32-bit DOS applications can use virtual-memory support and are significantly faster than 16-bit DOS applications.	**Phar Lap Software Inc** 60 Aberdeen Ave Cambridge, MA 02138 (617) 661-1510	656
	DOS/4G			**Rational Systems Inc.** 220 N Main St Natick, MA 01760 (508) 653-6006	657

to the interrupt first. The TSR could either perform some action or, because it remembered the original contents of the interrupt register, pass the interrupt on to the interrupt vector's original owner.

Microsoft couldn't keep such a nifty feature secret for long. Removing any doubt that even PC users need multitasking, other programmers soon figured out the undocumented DOS call and adapted TSRs for every task under the sun.

The real fun began when TSRs started "hooking" keyboard interrupts. DOS programmers cheerfully gave the DOS approved mechanisms for dealing with the keyboard the old heave-ho and started handling the keyboard in nonstandard ways. Users would add to the fun by loading multiple keyboard-based TSRs. The first TSR in the chain would get the interrupt, perform whatever action it felt like performing—perhaps changing the state of the PC—and, if the phase of the moon was correct, pass the interrupt to the next TSR in line.

TSRs would also play the same sort of games with the PC's screen. And yes, screen I/O is another area of extremely "creative" DOS programming. The very best DOS programmers will do any kind of screen manipulations except those that involve DOS calls. Taken as a whole, DOS with a bunch of TSRs resembles the Mad Hatter's Tea Party.

Common sense to the rescue

Now, no sane operating-system designer would set up an operating system that allows multiple tasks to steal shared resources as they see fit. In reasonable operating systems, a supervisor task monitors all interrupts, passing the interrupt to the appropriate task in a regular, algorithmic way.

The bad news for DOS programmers is that they not only have to learn how to use 500 to 700 new Windows operating-system calls, but they also have to give up all their cherished tricks. Under Windows, TSRs have no purpose and should be dispensed with. Under Windows, programmers cannot hook user interrupts or write directly to the screen. Windows manages all interrupts from the mouse and keyboard and coordinates all writes to the screen.

Programmers coming from "big" systems also have some shocks in store unless they have been programming for the X-Window System. Conventional Unix programs depend on a crude "standard-I/O" concept **(Ref 6)**. The Unix standard input is a serial stream, usually from a keyboard, whereas Windows programs must be able to handle input from several sources at once: keyboard, mouse, etc. The Unix standard output is another serial stream, usually to the screen. Programmers can redirect these standard paths. For example they can simplemindedly "pipe" the output of one program to the input of another. Windows' I/O and interprocess communications facilities are much more sophisticated and complex than the antique, Tinkertoy mechanisms of Unix.

Furthermore, C programmers are accustomed to using C libraries and functions which, known to the programmers or not, are based on DEC hardware and which sometimes poorly match 386/486 hardware. Although programmers can write Windows programs in C, much of standard C programming practice goes out the window. Windows has its own unique mechanisms for allocating memory and other system facilities as well as passing parameters.

For example, Unix programmers are accustomed to their program's receiving a pointer from the operating system in reply to a request for a system resource. Their program then saves that pointer, using it for the duration of the program's execution. Windows programmers cannot count on a pointer always being valid. Windows returns a "handle" to a system resource. The handle is actually an index into a table of memory locations for requested system resources. As Windows's memory manager moves things around in memory, it updates the appropriate entry in the handle table.

Because C really assumes underlying DEC hardware, C makes no distinction between data pointers and code pointers. But 386/486 μPs can have different code and data spaces—a facility that Windows makes use of.

Unix is a preemptive multitasking system. Unix programmers can write as much code as they like without worrying that their program will hog the system it is running on. Unix takes care of periodically interrupting programs to give other tasks time slices. Windows multitasking is self-paced. Each Windows task must give up the system voluntarily.

C programmers are accustomed to conglomerating many standard library programs along with their code, statically linking the whole system before running it. Windows has a powerful, sophisticated mechanism for dynamically linking program modules as needed while the program runs. These dynamically linkable modules must be reentrant because Windows will load only one copy of a module and share it with as many programs as need it. Thus Windows permits an entirely new way to structure large programs. Most C library functions (except for those from real-time Unix vendors) are not reentrant and hence are potentially dangerous under Windows.

Fig 1 shows a diagram of all the significant actors in a Windows system. Getting a general idea of how Windows runs programs and manages system resources is essential to understanding how it suits—or does not suit—engineering software. The hardware/software block diagram in **Fig 1** is in sharp contrast to the way programmers conventionally describe complex software systems.

Programmers are fond of expressing the relationships between various software and hardware actors in terms of "levels." These so-called levels speak more to programmers' loathing for hardware than they do of any actual structure. Like Dante's vision of the circles of hell, the inner "layer" (or lowest level—programmers use levels and layers interchangeably) of software hell is reserved for hardware. Radiating out from the innermost circle of software hell, you encounter first "low-level" drivers, usually—but not always—written in assembly language.

At the next layer or level, the software begins to take on a divine aspect because you encounter operating-system code usually written in a high-level language. Unfortunately, because an operating system has to know something about the system it is running on, this layer still bears the taint of hardware.

Finally, after passing through the operating-system layer, the programmer is in the pristine realms of the application layer and the outermost layer, the user interface. These areas are the most divine because it is in these areas that, free from the hardwired limitations of hardware, the programmer is in total control and becomes part of the software godhead.

In reality, a complex hardware/software system such as a 386/486 PC running Windows does not have a structure that resembles an onion. The application programs, Windows, DOS, and the PC's hardware each contribute a number of significant actors. These actors form the complex network in **Fig 1**. This network's topology permits certain transactions and forbids others. Various hardware and software actors have predefined, or hardwired, mechanisms that govern how the actors interact.

The important point is that some of these mecha-

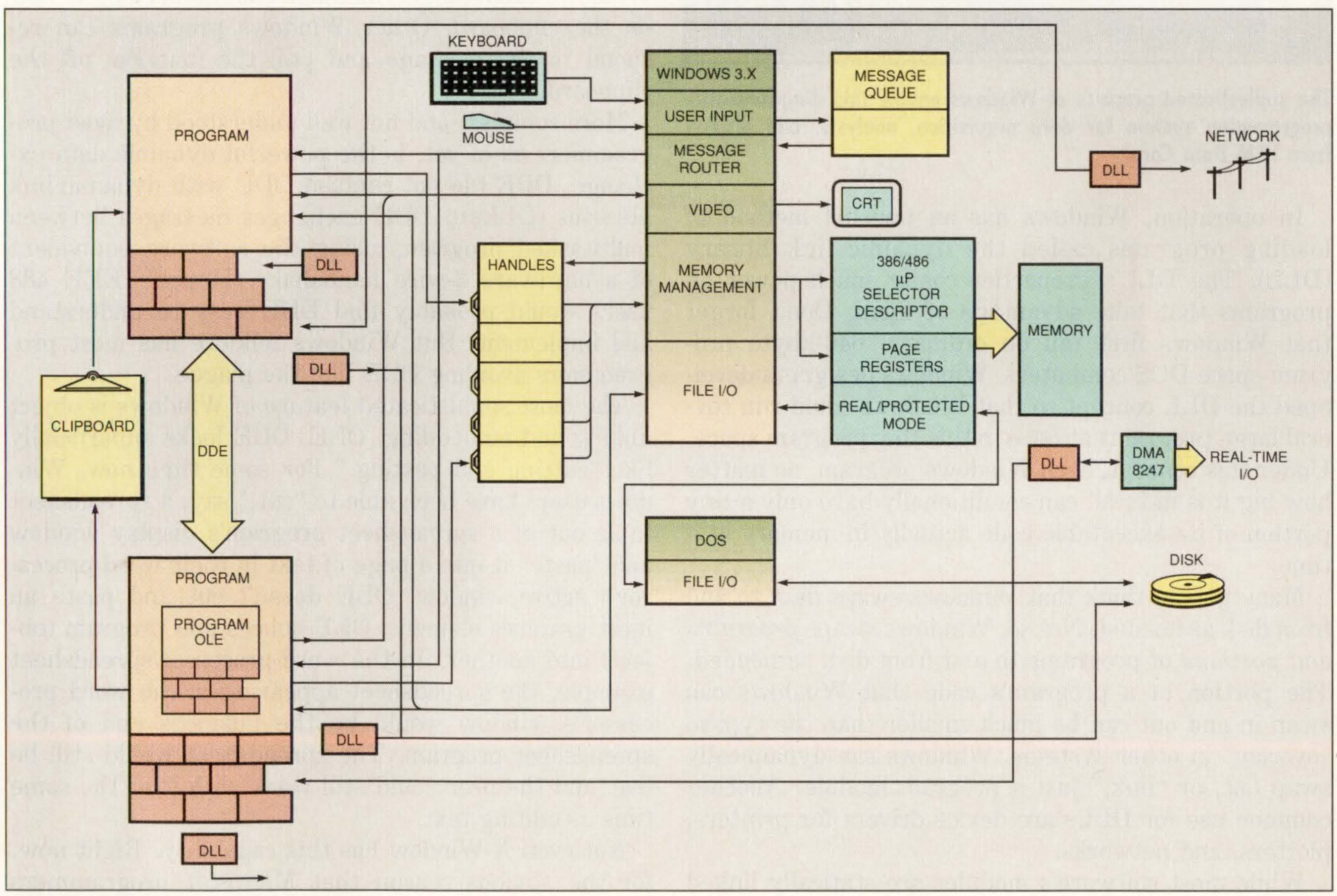
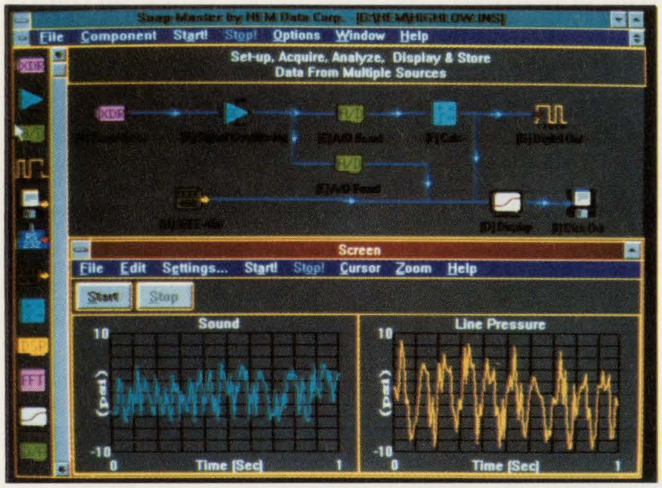


Fig 1—Multitasking programs running under Windows 3.X can add and delete program modules called DLLs (dynamic link libraries) on the fly. Among many functions, DLLs support networks, printers, plotters, and real-time I/O. Programs can communicate via the clipboard or DDE (dynamic data exchange), a defined protocol. Using OLE (object linking and embedding), one Windows program can even encapsulate another Windows program. Windows itself manages all the user interfaces. Windows also uses the 386/486 µP's hardware to manage memory, assigning "handles" to programs that want to use system services. Windows still depends on DOS for file I/O.

nisms suit Windows and a 386/486 for engineering software; some do not.

Fig 1 shows the user interface and applications programs to the left. Windows and its allies, the 386/486 and a few remnants of DOS, occupy the center position. On the right is the hardware that interfaces to the outside world.



The sophisticated graphics of Windows enable this diagrammatic-programming system for data acquisition, analysis, and display from HEM Data Corp.

In operation, Windows has an unusual method of loading programs called the dynamic link library (DLL). The DLL's properties confer much power on programs that take advantage of them. Don't forget that Windows first ran on ordinary, 640-kbyte program-space DOS computers. Windows designers developed the DLL concept so that Windows could run several large programs at once in this tiny program space. Under this concept, each Windows program, no matter how big it is in total, can conditionally have only a tiny portion of its executable code actually in memory at a time.

Many people think that Windows swaps data to and from disk as needed. Not so. Windows swaps *programs* and *portions* of programs to and from disk as needed. The portion of a program's code that Windows can swap in and out can be much smaller than the typical "overlay" in other systems. Windows can dynamically swap out, or "link," just a program module. Another common use for DLLs are device drivers for printers, plotters, and networks.

While most software's modules are statically linked after compilation, Windows can do this linking on the fly, at run time, as it loads a DLL into memory. The price of this flexibility is, alas, indirect access. Each DLL has a table for external calls. All external calls within the DLL's code actually point to a table entry. Windows fills in a DLL's table as it loads it. So each external call from one Windows DLL to another DLL involves an indirect call through a table, which adds to the access time. The benefit of the DLL facility is extreme flexibility in structuring programs and providing reusable library facilities.

DLLs are economical. In statically linked programs, each program that uses a given library function has its own private copy of that function linked in. Under Windows, as many programs as want to can use the same copy of a given DLL.

Windows has three ways that programs can communicate with each other. The simplest is the clipboard. The clipboard is not the clipboard icon you see in your Program Manager window. That icon represents a clipboard viewer. Windows does not limit the clipboard to "cutting and pasting" material from one program into another manually. The clipboard is a defined scratchpad that programs can use to exchange data as well. When one program writes to the clipboard, Windows broadcasts a message that something is now on the clipboard. Other Windows programs can respond to the message and pull the material off the clipboard.

More complex, and not well understood by most programmers as of yet, is the powerful dynamic data exchange, DDE (do not confuse DDE with dynamic link libraries (DLLs)). DDE exchanges messages between multitasked programs using the software equivalent of a hardware 3-wire handshake. Hence, IEEE 488 users would probably find DDE easy to understand and implement. But Windows folklore has most programmers avoiding DDE like the plague.

The most sophisticated feature of Windows is object linking and embedding, OLE. OLE looks superficially like "cutting and pasting." For some time now, Windows users have been able to "cut," say, a spreadsheet table out of a spreadsheet program's display window and "paste" it into a page of text in their word processor's active window. OLE doesn't cut and paste an inert graphics element; OLE splices one program (object) into another. In the word-processor/spreadsheet example, the spreadsheet appearing in the word processor's window would be the business end of the spreadsheet program. The spreadsheet would still be live, and the user could still work with it at the same time as editing text.

Not even X-Window has this capability. Right now, for the obvious reason that Microsoft programmers have had the first exposure to OLE, only programs from Microsoft use OLE. But you can expect engineering-software vendors will use this powerful mechanism to link complementary programs.

Because a user can be running several programs at

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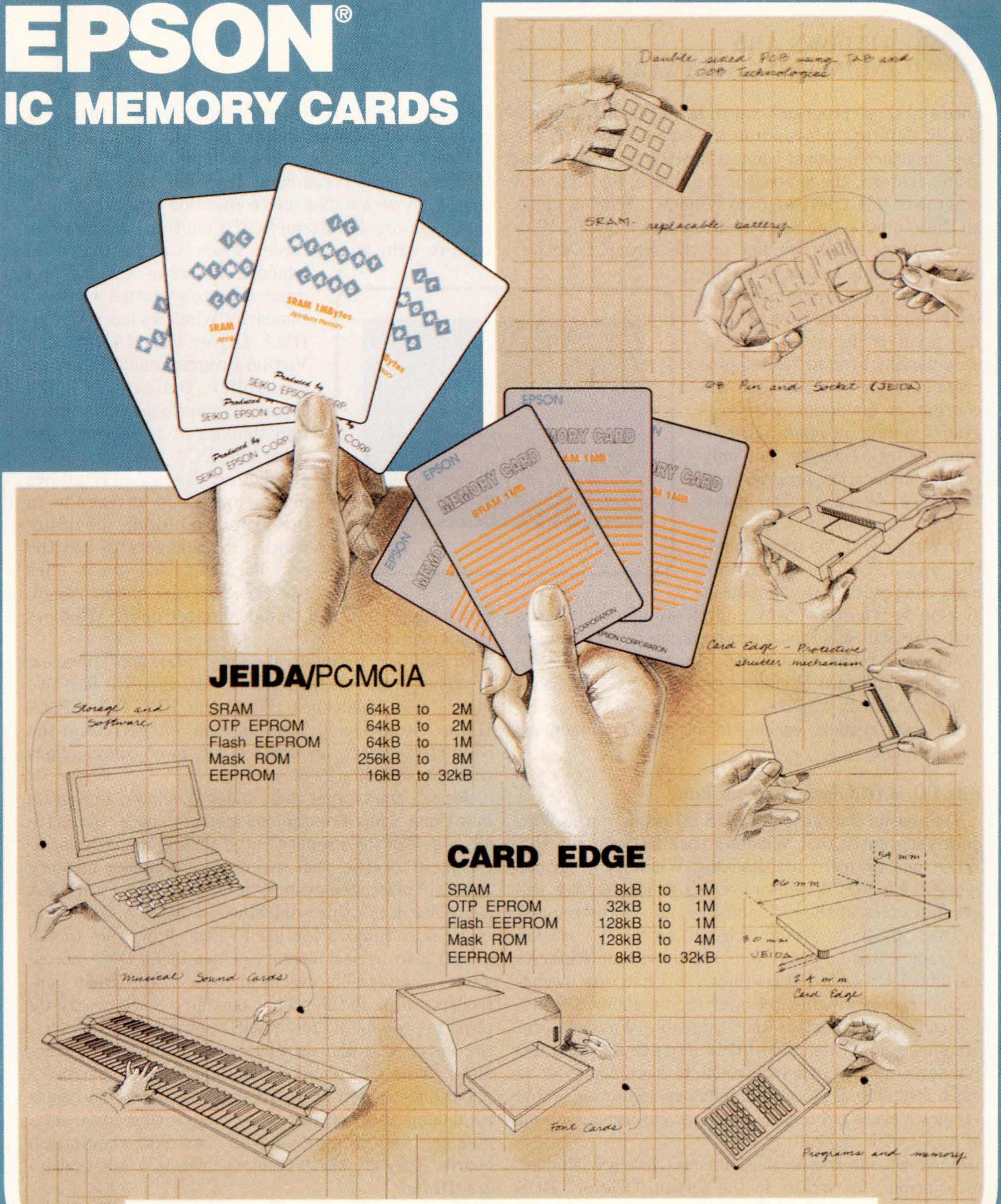

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once and those programs can all be displaying information in different windows on the screen together, the user interface does not connect directly to a given program. Instead, the keyboard, the mouse, joystick, and other user-input devices go to Windows. Windows puts all these inputs, one after another, into a queue. Windows knows which window on the screen is active. Windows sends messages to the active window's program, notifying it of user input. Now you see just what is meant by a "message-passing system." Most programmers are familiar with the concept of an application program's calling an operating system. Under Windows, not only can an application program call Windows, Windows can make calls to the program.

> **Windows programs trying to do real-time I/O face some tough challenges.**

In response to the user inputs, the application program can make computations or can request system services from Windows. Windows 3.0 has well over 500 calls that a program can make (the new Windows 3.1 has even more). Many of the calls involve the standard Windows graphical user interface (GUI) facilities: windows, scroll bars, buttons, etc. Other calls request various forms of I/O or memory management.

File I/O, a trip down memory lane

The reason that good old DOS is lurking in the Windows diagram is that Windows uses DOS for file I/O. When one or more multitasking Windows programs request file I/O, Windows decides which request will get first crack at the disk and then passes the request to DOS. To do so, Windows has to switch the 386/486 µP from protected mode to real mode so that Windows can find DOS's file-I/O routines. This baroque mechanism is necessarily much slower than a plain DOS file-I/O call. Consequently, knowledgeable Windows programmers do all their file I/O in large chunks and use Windows' memory management to keep copies of as much disk data as possible in memory. (Knowledgeable Windows users get a lot of memory and use a good bit of it as a disk cache.)

Windows interposes mechanisms that are similar, in principle, for writes to the screen. "Clever" DOS programmers can bypass DOS's operating-system calls altogether and simply write their program's video output directly into the PC's video memory. For a multitasking, multiwindowed operating system, such quick-and-dirty methods are not permissible. Thus, Windows takes longer than an equivalent DOS program to update the screen. However, Windows' performance is comparable to X-Window's.

Under multitasking, more than one program can try to use a shared resource at the same time. One way that Windows handles such contention is to "virtualize" that resource. For example, if a multitasking program tries to write to the screen while it is not the active window, Windows lets the program write to a "virtual window." Similarly, Windows has a Virtual DMA Driver (VDMAD) and a Virtual Programmable Interrupt Controller Driver (VPICD). These facilities fool each program into thinking it is the only one using the PC's hardware DMA controller. Because Windows must constantly intercede in interrupt handling, deciding which program gets to use the real hardware and which ones use the "virtual" hardware, interrupt responses can be much longer under Windows than under DOS.

In addition to relatively long interrupt latencies, Windows programs trying to do real-time I/O face two other tough challenges. First, the IBM PC's 8237A DMA-controller chip is an antique left over from the 64-kbyte segment days. It has far fewer address lines than the 386/486 µPs do.

Second, don't forget that, under Windows, a program may think it has a contiguous memory space. But actually, the 386/486's sophisticated virtual memory facilities piece together that seemingly contiguous memory space out of isolated memory fragments. The PC's DMA controller lacks this sophisticated facility. This chip requires constant attention to keep it writing to the proper place in real memory. Thus, doing DMA necessitates considerable overhead to keep the DMA controller writing to the proper portion of each program's physical (as opposed to virtual) memory space. In fact, the faster PCs can do memory-to-memory transfers faster under CPU control than under DMA control.

Data-acquisition pc-board makers consequently are rethinking their entire approach, putting more data memory and intelligence on the data-acquisition boards. They are also writing their own Windows drivers (DLLs).

Windows supposedly relieves program developers of supporting printers, plotters, and other I/O devices. Well . . . maybe yes and maybe no. Microsoft is familiar with office printers. But engineering printers and plotters are another matter. One pc-board CAD company, for example, had to write its own device driver

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for the Gerber Photoplot when it debuted its Windows version of its pc-board software. Also, Hewlett-Packard has reportedly written drivers for many of its printers and plotters.

Like many people, I bought a copy of Windows 3.0, tried out the spiffy looking solitaire game that comes as a freebie, and never fired Windows up again. My familiar DOS programs suited me just fine, and none of the Windows software I saw looked worth the money. Another EDN editor, who tried determinedly to use Windows 3.0, got one too many crashes (the dreaded "UAE" message) and began wearing an "I hate Windows!" button.

Since then, though, I have been a beta tester for Windows 3.1 and I have talked to engineers, programmers, and marketing people at numerous engineering-software companies. Some raved about Windows; some slammed it unmercifully.

The arguments and counter-arguments run something like this:

- OS/2 is better than Windows in every way. *But . . . so what?*
- Those engineers who want to multitask programs can run as many plain DOS programs as they want simultaneously under good old Desqview—including 32-bit programs that run under a DOS extender. *But Windows offers facilities for intertask communication and control that multitasked DOS programs can't use.*
- Windows has a nice user interface. *But packages are available to give any program the "look and feel" of Windows.*
- Windows graphics are slower than writing directly to the video hardware. *But throwing about $200 worth of hardware and software at the problem makes it go away* **(Ref 7)**.
- Windows file I/O is slow. *But eventually Microsoft will stop dipping into real mode to use DOS for I/O and graft protected-mode file I/O onto Windows. In the meantime, when memory costs less than $50/Mbyte, and DOS 5.0 comes with a disk cache, life is too short to wait for disk access.*
- DMA is slow and painful under Windows. *But the data-acquisition folks are making their boards smarter and their DLLs faster.*
- Windows runs only 16-bit programs. *But programmers have a variety of workarounds at their disposal to run 32-bit programs under Windows, and when Windows NT comes, it will be a 32-bit operating system.*

Me? What do I make of this spaghettied mass of arguments? I think that Windows is a good bet to actually become ubiquitous, not so much for what it is, but for what it will be.

Look at DOS. DOS has survived long after any reasonable estimate based on its technical merits would have predicted. DOS survived not because it was the *best* PC operating system, but because it was *the* PC operating system. People in my home town, Newton, MA, take the Green Line trolley to downtown Boston not because it is the best trolley, but because it is *the* trolley.

Soon Microsoft will perform a hood-ornament overhaul on Windows. In case you are not familiar with the term, a hood-ornament overhaul occurs when you have a car that is in such tough shape that the only way to fix it is to jack up the hood ornament, drive a new car underneath, and let the hood ornament back down. Windows NT is a hood-ornament fix for all that ails Window 3.X. And Windows NT will run Windows 3.X programs.

So, even though I use Desqview to launch and multitask all my comfortable old DOS programs, I think whatever Windows strengths and weaknesses are, or will be, Windows will become *the* operating system. EDN

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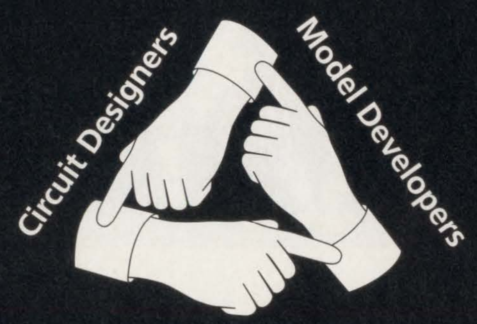

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Barry M Clark, Stag Microsystems Inc

In-circuit programming eliminates many of the hazards associated with plugging memory devices in and out of sockets. By using some practical guidelines, you can rig a pc board's layout to meet commercial in-circuit-programmer specifications.

More and more, reliability demands that EPROMs and EEPROMs be permanently soldered onto printed-circuit boards. Such demanding applications include vibration-proof construction for avionics, military, and aerospace projects. In addition, surface-mount memory devices are proliferating in many new commercial applications. The ability to program memory devices without removing them from the pc board not only simplifies updating software in the field but can also eliminate the inventory cost of storing multiple programmed and labeled devices. Besides memory devices, microcontrollers having on-chip PROMs as well as some PLDs can also benefit from in-circuit programming.

Because in-circuit programming applications are diverse, you have several design options for programming an in-circuit device. For example, you can custom-design a programmer for a specific task, but this approach is usually costly and can be inflexible for simple changes. You can also design an adapter for using a commercial device programmer. However, device programmers generally don't supply enough power to support a populated pc board, and the drive currents for the address, data, and control lines are often inadequate. The most economical and popular approach is to use a commercially available general-purpose in-circuit programmer.

Using a general-purpose in-circuit programmer minimizes NRE costs in two ways. First, you have to design only basic custom hardware that adapts your pc board to a standard programmer interface (**Fig 1**). Second, generating an appropriate programming algorithm is straightforward. For most commercial in-circuit programmers, you generate a descriptive text file for the pc board's configuration and device types. The in-circuit programmer uses this text file to compile an algorithm that programs devices for the entire board. These commercial in-circuit programmers are complete systems containing a CPU, RAM and ROM, mass-storage devices, operator and external-equipment interfaces, power supplies capable of supporting a pc board, and electronics capable of generating the appropriate programming waveform.

Electrical features will determine which in-circuit programmer suits your application. The programmer's power supply should be adequate to power your pc board under worst-case programming conditions. The programmer should also have redundant power-supply lines to keep other sections of the pc board active while it is programming devices. The programmer should be able to transfer data to and from a host computer and verify programmed data to ensure integrity

In addition, drivers for gang-programming multiple boards should be well isolated from each other to ensure that the failure of one board doesn't affect the programming of another. If you're programming a large set of EPROMs, you'll want a programmer having sufficient RAM. And in field-programming applications, the programmer must be able to operate as a stand-alone unit.

When adapting a board design for a general-purpose in-circuit programmer, you can avoid potential pitfalls by adhering to some practical guidelines. To illustrate these guidelines, consider the example of in-circuit programming multiple EPROMs on a pc board that also has other logic devices and a μP. First of all, you should use EPROMs fabricated in one of the MOS technologies—NMOS, HMOS (high-performance MOS), or CMOS. The programming characteristics of MOS EPROMs are close to the devices' operating characteristics. Therefore, MOS EPROMs are easier to program on a pc board than are bipolar devices, which have programming characteristics vastly different from their operating characteristics.

You shouldn't randomly mix EPROMs from different vendors on the same board, and when gang-programming multiple pc boards, the EPROMs on all the boards should be from the same manufacturer. Although the operational specifications of second-source EPROMs are similar to those of the original device, their programming specifications are often quite different. The differences typically extend to distinctive voltages and timing specifications for the programming pulse. Therefore, the in-circuit programmer would have to compile different programming algorithms to accommodate second-source devices.

To externally program a pc board, you must route the address and data buses and control lines of all the EPROMs to a board connector that is compatible with the programmer's interface connector. In many cases, these lines are already available at the board's target-system connector. If the system connector isn't compatible with the programmer, you must add a suitable connector.

An ID can eliminate Nader raiders

In some applications, you may want to provide boards with an ID that the programmer can read. IDs are useful when you have several different boards or different versions of the same board. The programmer checks the board's unique ID prior to programming to ensure that you've installed the right board. You can implement the ID using board jumpers, switches, or logic.

Alternatively, you could take advantage of the manufacturer's identification codes built into many EPROMs.

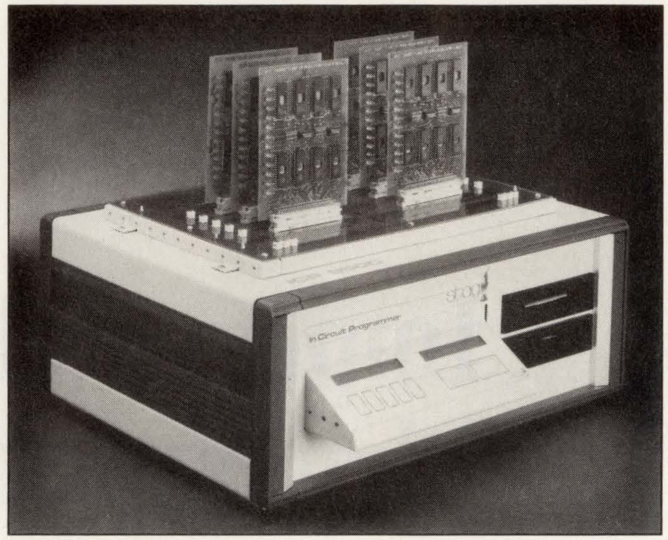


Fig 1—A custom assembly can adapt a pc board's system connector to a commercial in-circuit programmer. This programmer can gang-program multiple boards.

These codes identify the manufacturer and device type, which lets the programmer automatically choose the proper programming algorithm. Because the programmer must apply 12V to address line A9 to read an EPROM's identifier, you must isolate any other pc-board circuitry that connects to this address line.

The in-circuit programmer must take full control of the pc board to program the EPROMs. Ideally, the programmer should have direct access to all bus and control lines to minimize timing errors, shape the programming pulse, and account for transmission-line effects. In practice, however, access to an EPROM is usually through a cascade of logic circuits, and many EPROMs often share the same bus and control lines.

To program a target EPROM, the programmer must place an address on the EPROM's address bus via buffers resident on the board and be able to transfer data to and from the EPROM's data bus. Thus, the pc board must have bidirectional transceivers in the data path between the EPROM and the interface connector even though data flows unidirectionally to achieve the final objective. In addition, the transceivers' direction and enable control lines must be accessible to the interface connector. Other active devices attached to the target EPROM's data bus should have separate 3-state buffers. The programmer places the buffer outputs in a high-impedance state while programming and verifying data in the target EPROM **(Fig 2a)**.

You can often put a μP's data bus in a high-impedance state by activating the μP's output-enable, reset, or halt control lines. If the μP's data bus attaches to the EPROM's data bus, then one of these control lines should be accessible to the interface connector for program control (**Fig 2b**). In some instances, the pc board may have a system bus comprising multiplexed address and data lines. In such instances, the control lines for the board's address latch should extend to the interface connector for program control.

To reduce the time needed to program multiple EPROMs, intelligent programming algorithms raise the EPROMs' V_{CC} supply voltage to 6V or higher. Although TTL logic can withstand a V_{CC} voltage as high as 7V, the increased power dissipation can unduly stress these devices. To avoid this stress, provide dual V_{CC} supply lines to the interface connector. The dual lines let the programmer supply power to the board using isolated power supplies—one for the EPROMs and one for rest of the board's circuitry. You can connect the dual V_{CC} lines off the board at the application's mating-system connector.

An EPROM's V_{PP} line also requires special consideration when you plan to program the device in circuit. Boards not designed for in-circuit programming have their EPROMs' V_{CC} and V_{PP} pins connected so devices can read the data. To program an EPROM in circuit, the board layout must isolate these two pins to let the

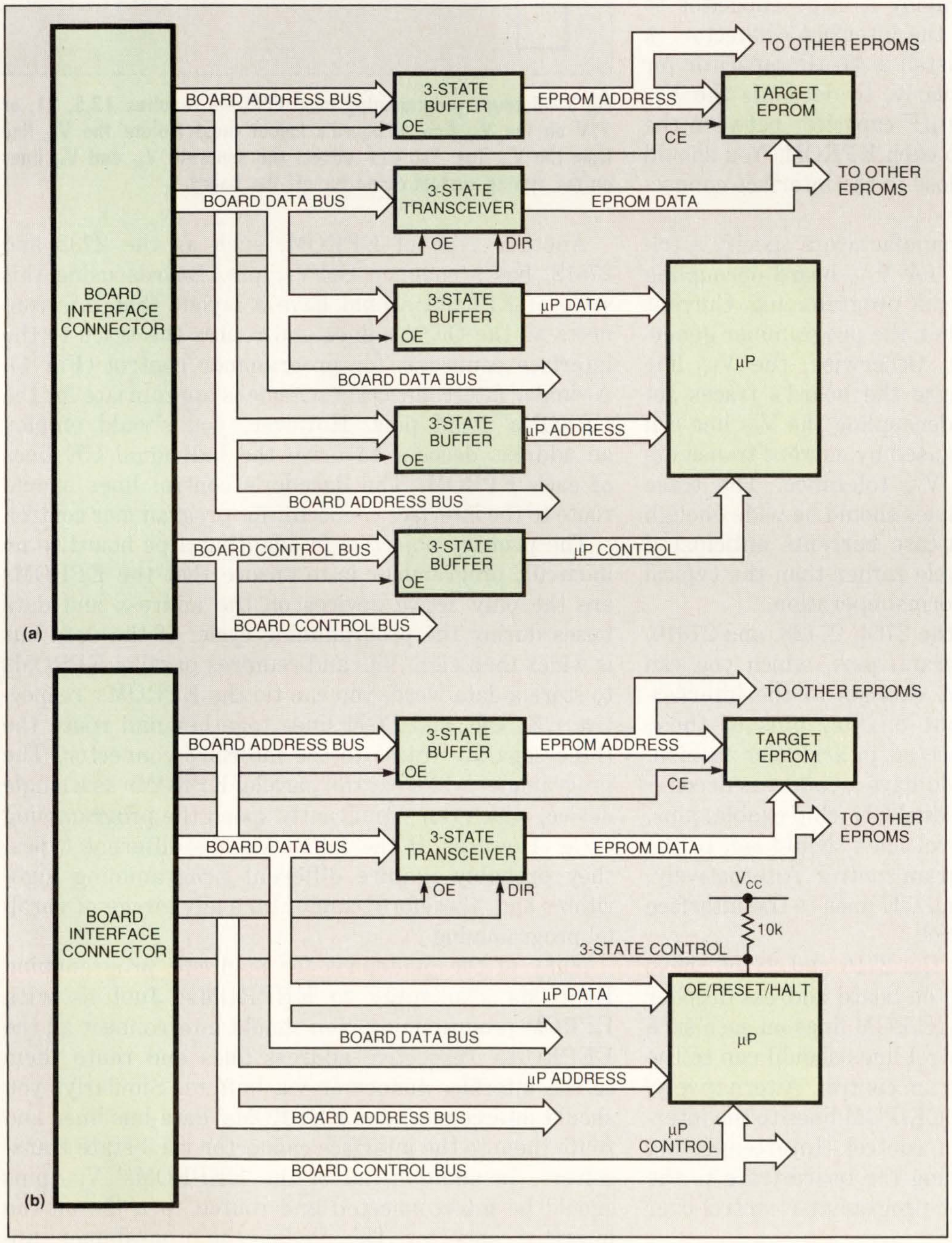


Fig 2—The in-circuit programmer must have control of all devices that share an EPROM's address and data bus. You can isolate a peripheral device such as a μP by using 3-state buffers (a) or by forcing on-chip 3-state drivers into a high-impedance state (b).

programmer raise the V_{PP} line to a voltage greater than V_{CC}, which is typically 5V (**Fig 3**). Typical V_{PP} voltages are 12.5, 21, or 25V depending on the programming algorithm. Therefore, the board layout must route the V_{PP} line to a separate pin on the interface connector. You can connect the V_{PP} line to the V_{CC} line off the board at the application's mating-system connector.

The decoupling arrangement for the pc board's V_{CC} and V_{PP} lines is critical. You should follow the EPROM manufacturer's decoupling recommendation, which usually dictates the placement of a 0.1-µF capacitor between the V_{CC} pin and ground close to each EPROM. In addition, you should employ a large capacitor to decouple the V_{CC} line near the interface connector. A good rule-of-thumb is to install a 47-µF capacitor for every eight EPROMs. Similarly, to decouple the V_{PP} line, you should place a 0.1-µF capacitor between the V_{PP} pin and ground close to each EPROM. You should also decouple the V_{PP} line close to the interface connector using a 10-µF capacitor.

Because most EPROM manufacturers specify a tolerance between 0.5 and 1V for V_{PP}, board decoupling is crucial to successful in-circuit programming. Current flows in the V_{PP} line only when the programmer generates a programming pulse. Otherwise, the V_{PP} line current is negligible. Because the board's traces act as inductors, inadequately decoupling the V_{PP} line can result in induced voltages caused by current transients that exceed the specified V_{PP} tolerance. The trace widths for the V_{CC} and V_{PP} lines should be wide enough to accommodate the worst-case currents anticipated during the programming cycle rather than the typical currents expected during normal operation.

Some EPROMs, such as the 2764, 27128, and 27010, have individual PGM (program) pins, which you can tie to a common trace that extends to the interface connector. The OE (output enable) pins of these EPROMs can be interconnected in a similar fashion. However, the pc board should have an address decoder to drive the EPROMs' individual CE (chip enable) pins. The address decoder's control lines should run to the interface connector for program control. Alternatively, you could route the individual CE lines to the interface connector for program control.

Other EPROMs, such as the 2716 and 27256, have a common CE/PGM pin. An on-board address decoder should drive the individual CE/PGM lines on each such EPROM. The decoder's control lines should run to the interface connector for program control. Alternatively, you can route the individual CE/PGM lines to the interface connector for program control. Interconnecting groups of OE pins and routing the board trace to the interface connector gives the programmer control over groups of EPROMs.

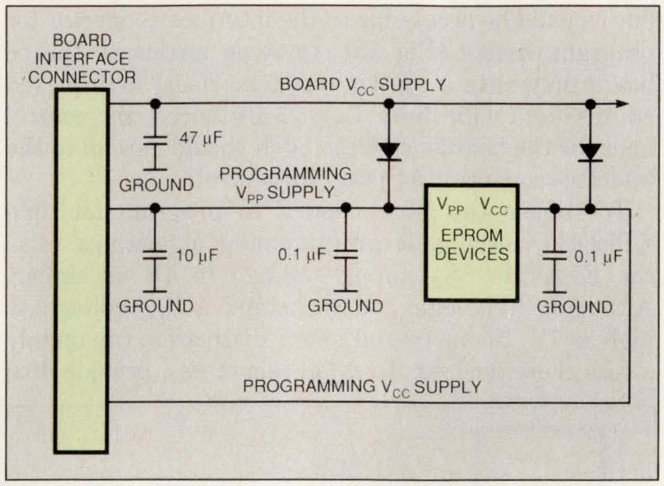


Fig 3—Because programming most EPROMs requires 12.5, 21, or 25V on the V_{PP} line, a board's layout must isolate the V_{CC} line from the V_{PP} line. You can connect the separate V_{CC} and V_{PP} lines on the mating-system connector off the board.

Another type of EPROM, such as the 2732 and 27512, has a common OE/V_{PP} pin. Boards using this style of EPROM should have a layout that interconnects all the OE/V_{PP} lines and routes the trace to the interface connector for programmer control (**Fig 4**). A similar interconnection scheme is appropriate for the EPROMs' PGM pins. However, you should employ an address decoder to drive the individual CE lines of each EPROM. The decoder's control lines should route to the interface connector for programmer control.

The primary objective in adapting a pc board to an in-circuit programmer is to ensure that the EPROMs are the only active devices on the address and data buses during the programming cycle. If the data bus is wider than eight bits and requires parallel EPROMs to store a data word, you can tie the EPROMs' respective CE, OE, and PGM lines together and route the three separate traces to the interface connector. The programmer will treat the parallel EPROMs as a single device, which can significantly speed the programming cycle. However, if the EPROMs are different types, they probably require different programming algorithms and, therefore, cannot take advantage of parallel programming.

Many of the guidelines for in-circuit programming EPROMs also apply to EEPROMs. Just as with EPROM programming, you should interconnect all the EEPROMs' respective address lines and route them to the interface connector via buffers. Similarly, you should interconnect the EEPROMs' data-bus lines and route them to the interface connector via 3-state transceivers. In addition, all of the EEPROMs' V_{CC} pins should be interconnected and routed to a pin on the interface connector. This pin lets the programmer supply power to the EEPROMs via a supply that is isolated from the rest of the board. When the data bus is wider than eight bits, you can tie the respective CE, OE, and WE (write enable) lines of parallel EEPROMs together to program them as a single device.

The layout differences between EPROM boards and EEPROM boards are due to the electrical-erasure characteristics of the EEPROMs. EEPROMs fall into two categories: those that require a high-voltage erasure-and-programming pulse and those that use low voltage (5V) for erasure and programming. The layout of a pc board rigged for programming EEPROMs in circuit must reflect these differences. When using low-voltage-erasure EEPROMs, you can interconnect their OE and WE lines and route them to the interface connector for programmer control. However, the CE lines should be driven independently—either by an on-board address decoder or directly by the programmer.

High-voltage-erasure EEPROMs require more attention. Activating the CE pin disables many of these EEPROMs. Tying all of the V_{PP} pins to a common trace that extends to the interface connector lets the pro-

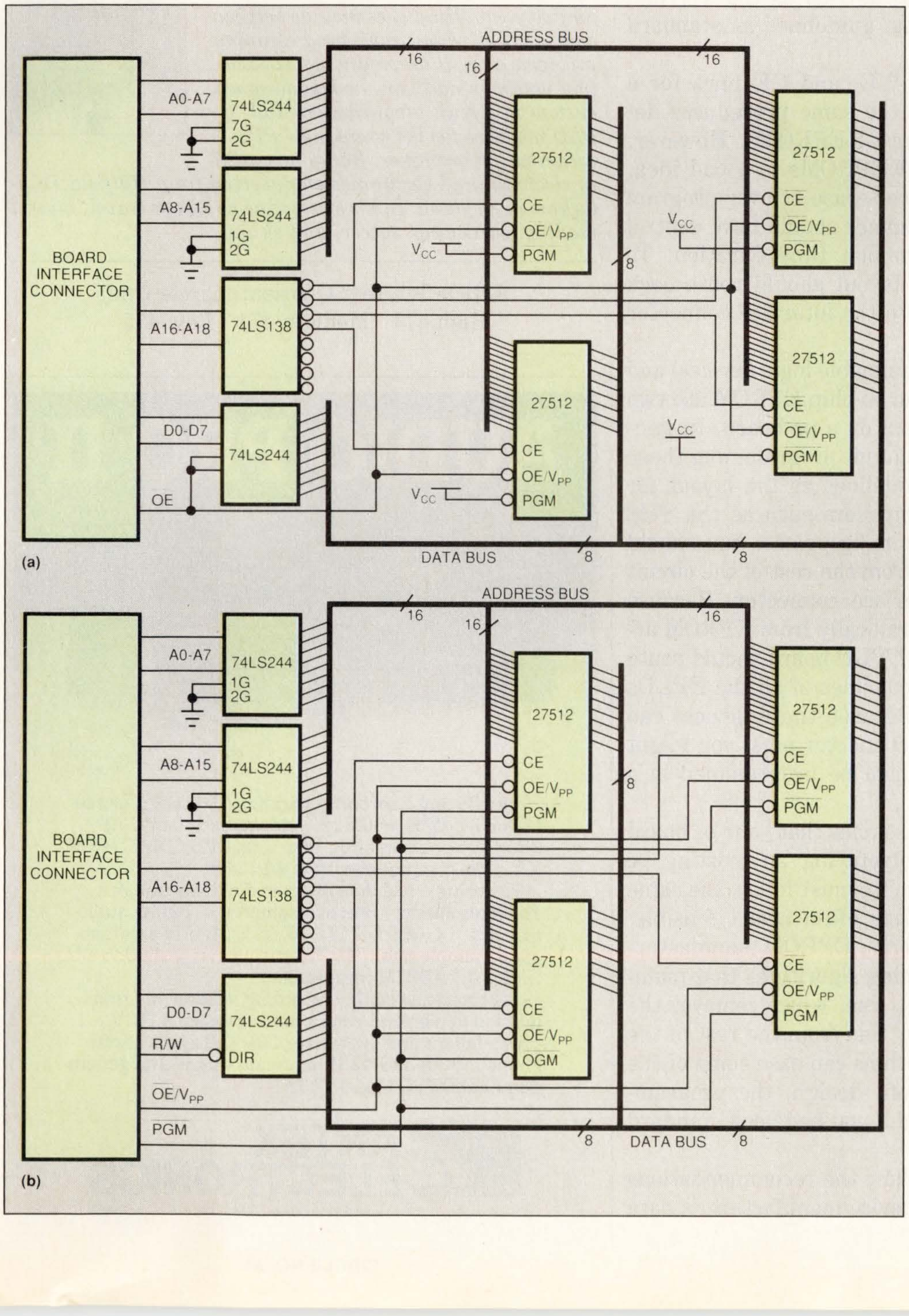


Fig 4—To modify a board containing 27512 EPROMs from a device-programming layout (a) to an in-circuit programming layout (b), you must make sure the programmer has control of the OE and PGM lines.

grammer or an onboard address decoder control the CE lines independent of each other. For devices whose erasure requires a high-voltage pulse on the CE pin, the board layout must route the individual CE lines to the interface connector for programmer control.

Don't over-program flash EEPROMs

Another candidate for in-circuit programming is the increasingly popular flash EEPROM. Flash EEPROMs require a high voltage on the V_{PP} pin during programming and an exclusive erasure cycle. The board layout for the address and data bus as well as the V_{CC} and V_{PP} lines can follow the same guidelines as standard EPROMs.

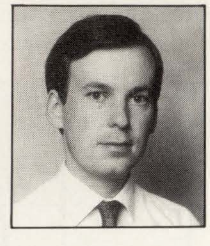
You can lay out the OE, WE, and CE lines for a flash-EEPROM board using the same procedures described for low-voltage-erasure EEPROMs. However, programming parallel flash EEPROMs is a bad idea. Because programmers can over-erase or over-program flash EEPROMs, the programmer should have control of the erasure and programming time duration. To implement this control, the layout should route each CE line and RDY/Busy line to the interface connector for programmer control.

EPLDs (electrically programmable logic devices) and microcontrollers containing an on-chip EPROM are two more devices you can program on a pc board. In general, the board layout for in-circuit programming these devices follows the same guidelines as the layout for an EPROM board. Microcontrollers such as the 8748 require high-voltage programming pulses. You should isolate the pins of such μCs from the rest of the circuit and route them to the interface connector. Because EPLDs' architectures differ radically from EPROM architectures, the layout of an EPLD board should route the individual input and output lines of all the EPLDs to the interface connector. Because these devices can potentially consume several connector pins, you might consider using EPLDs that can be programmed in a serial bit-by-bit manner.

Of course, this discussion assumes that your pc board is in the design stages. Retrofitting an existing pc board for in-circuit programming must follow the same guidelines, but these practices often aren't feasible. To accommodate retrofit designs, EPROM manufacturers are developing programming algorithms that maintain a constant 5V on the V_{CC} line, which removes the constraint of isolating the V_{CC} line from the rest of the board. Although these algorithms can ease some of the layout constraints in a retrofit design, the programming time will be longer than if you had used standard algorithms.

In any case, you should follow the recommendations found in the programmable-device manufacturer's data book. In addition, in-circuit-programmer vendors can offer information on board constraints, such as board profiles, mechanical requirements for the interface connector, and supporting slide guides or locks. By paying attention to some practical design and layout rules, in-circuit programming can be trouble free. EDN

Author's biography



Barry M Clark is a senior applications engineer with Stag Microsystems Inc (Santa Clara, CA), where he has worked for five years. His duties include helping customers solve in-circuit programming problems as well as producing application notes. In addition, he has designed custom in-circuit programmers and PLD modules for the company's PP2 universal programmer. Barry has a BS in electrical and electronics engineering from Hatfield Polytechnic in England. In his spare time he enjoys travel, music, reading, gardening, soccer, and skiing.

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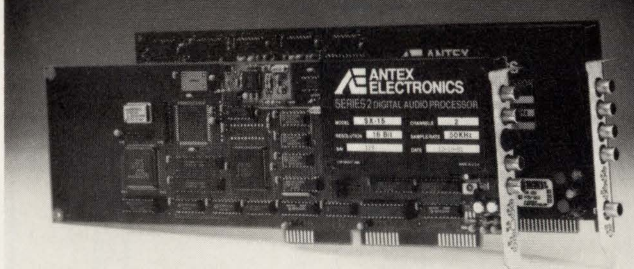

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DESIGN NOTES

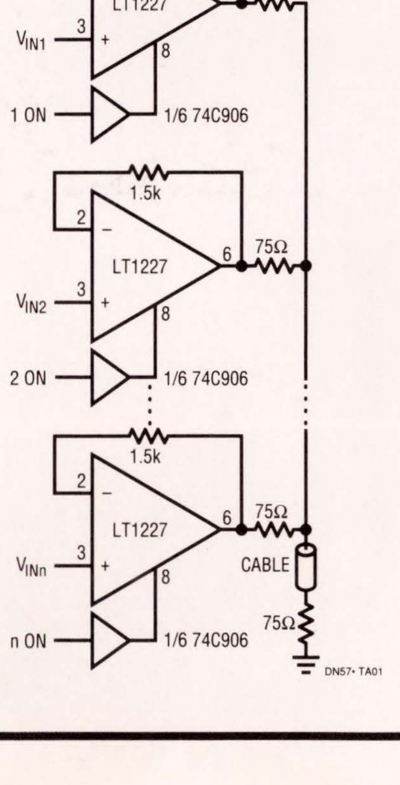
Video Circuits Collection – Design Note 57

William H. Gross

Introduction

This note shows how to make several different video circuits using high speed op amps. All of these circuits work with composite, RGB and monochrome video. For best results, bypass the power supply pins of these amplifiers with 1μF to 10μF tantalum capacitors in parallel with 0.01μF disc capacitors. It is important to terminate both ends of video cables to preserve frequency response. When properly terminated, the cable looks like a resistive load of 150Ω.

Lots of Inputs Video MUX Cable Driver (LT1227)

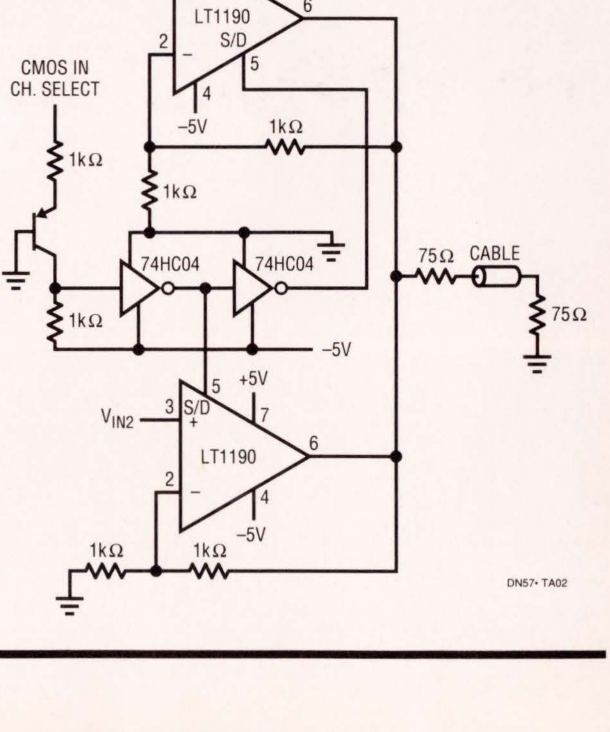


Multiplex Amplifiers

Often it is desirable to select one of several signals to send down a cable. Connecting the outputs of several amplifiers together and using the amplifier's shutdown pin to disable all but one accomplishes this goal. The LT1190, LT1191, LT1192, and LT1193 are shutdown by pulling pin 5 to the negative supply.

The LT1223 and LT1227 current feedback amplifiers are shutdown by pulling pin 8 to ground. During normal operation pin 8 is open and at the positive supply potential. An easy way to interface pin 8 to logic is with a logic level N-Channel FET or a 74C906 (open drain hex buffer).

Two Input Video MUX Cable Driver (LT1190)



Differential Gain and Phase of Several Amplifiers

	DIFFERENTIAL			
	LOAD = 1kΩ		LOAD = 150Ω	
PART NO.	GAIN	PHASE	GAIN	PHASE
LT1190*	0.05	0.02	0.23	0.16
LT1191*	0.03	0.01	0.09	0.07
LT1192**	0.10	0.01	0.23	0.15
LT1193*	0.20	0.08	0.20	0.08
LT1194**	0.20	0.08	0.20	0.08
LT1223	0.01	0.02	0.12	0.26
LT1227	0.01	0.01	0.01	0.01
LT1228	0.01	0.01	0.04	0.10
LT1229	0.01	0.01	0.04	0.10

$V_S = \pm15V$, $A_V = 2$

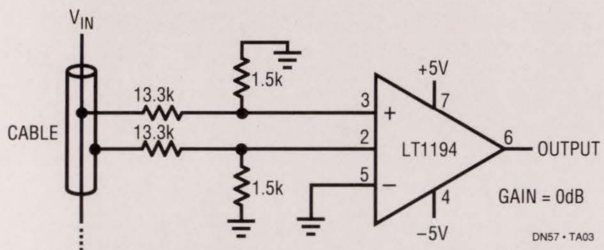
* $V_S = \pm8V$, $A_V = 2$

** $V_S = \pm8V$, $A_V = 10$

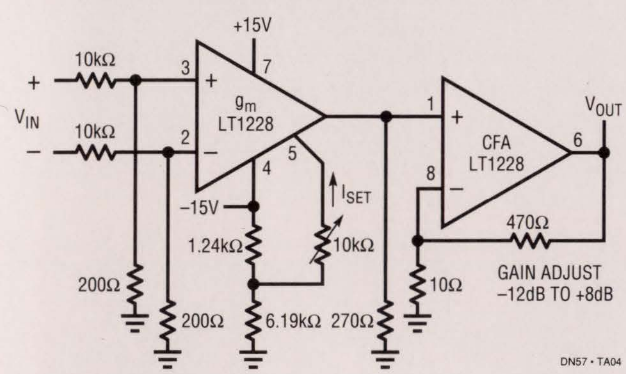
Loop Through Cable Receivers

Most video instruments require high impedance differential input amplifiers that will not load the cable even when the power is off.

Differential Input Video Loop Through Amplifier Using a Video Difference Amplifier (LT1194)



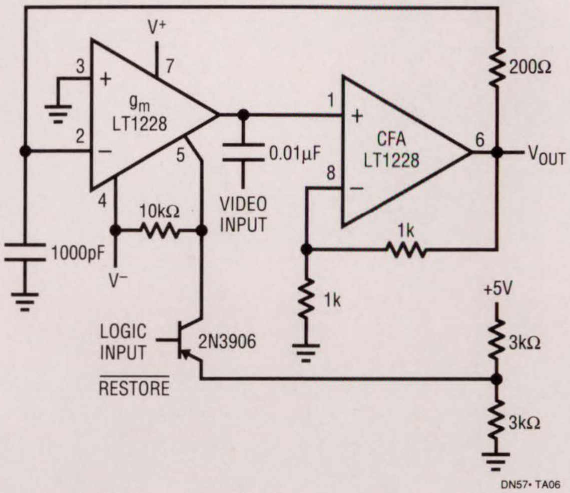
Electronically Controlled Gain, Video Loop Through Amplifier (LT1228)



DC Restore Circuits

The following circuit restores the black level of a monochrome composite video signal to 0V at the beginning of every horizontal line. This circuit is also used with CCD scanners to set the black level.

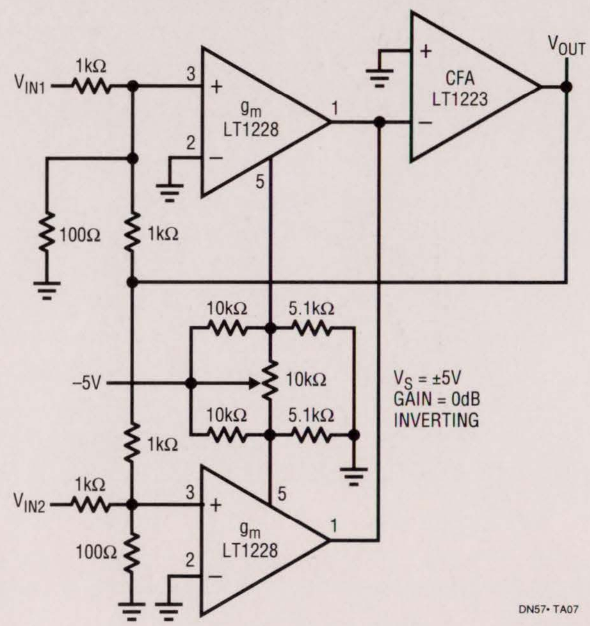
Video DC Restore (Clamp) Circuit (LT1228)



Fader Circuits

Using two LT1228 transconductance amplifiers in front of a current feedback amplifier forms a video fader. The ratio of the set currents into pin 5 determines the ratio of the inputs at the output.

Video Fader (LT1228, LT1223)



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Transducers form proximity detector

Jay Scolio, Maxim Integrated Products, Sunnyvale, CA

Combining micropower op amps with a pair of matched piezoceramic transducers (one optimized for 40-kHz transmission and the other for 40-kHz reception) yields an ultrasonic proximity detector that operates on a 9V battery **(Fig 1)**. The detector employs the radar principle—nearby people or objects reflect the transmitter's steady tone back to the receiver.

The transmitting transducer **(Fig 1a)** is a resonant circuit that may draw spikes of current from its signal source, which, in this case, is the low-power CMOS timer, IC_1. To prevent damage from these undesirable spikes, a push-pull driver composed of Q_1 and Q_2 buffers the timer. You should adjust the potentiometer, R_1, for a transmit frequency of 40 kHz.

The receiver in **Fig 1b** must offer high gain at ultrasonic frequencies while operating from the same 9V battery as the transmitter. Op amps IC_2 and IC_3 provide the necessary bandwidth and supply current (7 MHz min at unity gain and 375 μA max). Op amp IC_4, offering a rail-to-rail output swing and extremely low quiescent current (1.2 μA when low, 30 μA when high), is also well suited to its role as the output-signal comparator. Supply current for the complete circuit is slightly more than 2 mA. (Note: You can halve this consumption by replacing the transistors with a CMOS inverter.)

The receiver is stable using the component values shown. If you change the gain, however, note that you must also adjust the pole-zero locations associated with op amps IC_2 and IC_3 to maintain stability. In a store-display application, the proximity detector triggers a prerecorded video message on the arrival of an interested customer. A pause to look signifies interest; the detector shouldn't respond to someone just walking by. Therefore, R_2 and C_1 filter the transducer signal after D_1 rectifies it. The filter also prevents false triggering as a response to brief bursts of ambient noise in the ultrasonic range. **EDN BBS /DI_SIG #1115**

EDN

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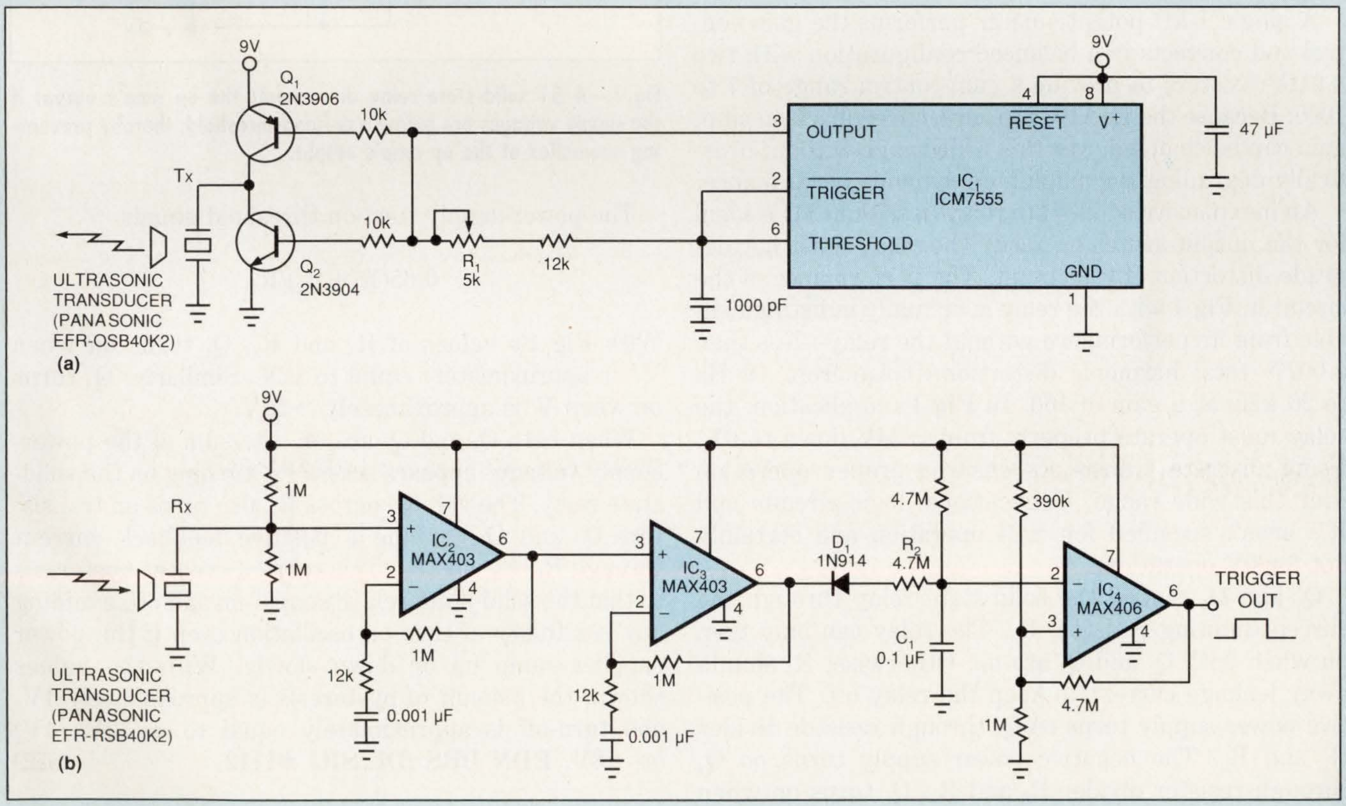

Fig 1—Comprising an independent transmitter (a) and receiver (b), this battery-powered, ultrasonic proximity detector features two 40-kHz piezoceramic transducers.

Solid-state relay prevents turn-on anomalies

R Mark Stitt, Burr-Brown Corp, Tucson, AZ

ICs operate properly only above a specified minimum power-supply voltage. When power-supply voltages drop below this level, operation is unpredictable. Since most analog ICs use dual power supplies, power-supply sequencing variations, which occur when one power supply comes up or goes down before the other, can also cause problems. Momentary lock up or oscillation during power-up or power-down is common. In many instances, these anomalies are inconsequential and go unnoticed, but sometimes these unexpected operating states can be devastating. For example, audio amplifiers that lock up or oscillate during power-up or power-down can damage speakers.

Fig 1's simple control circuit eliminates turn-on problems with analog ICs. The circuit uses a few garden-variety transistors and resistors along with an inexpensive solid-state relay to disconnect the output of an analog IC unless both its positive and negative power supplies are above a specified voltage. **Fig 1** demonstrates the control circuit enabling the output of a microphone amplifier.

A single 1-kΩ potentiometer performs the gain control and connects in a balanced configuration with two 3.01Ω resistors to provide a gain-control range of 7 to 1000. Because the INA103 is a current-feedback op amp, gain can be changed over this wide range without drastically degrading the amplifier's dynamic performance.

An inexpensive solid-state relay (less than $1) is ideal for the output-switching task. The relay must not degrade distortion of the circuit. The performance of the circuit in **Fig 1** with the relay is virtually indistinguishable from its performance without the relay—less than 0.002% total harmonic distortion + noise from 10 Hz to 20 kHz at a gain of 100. In **Fig 1**'s application, the relay must operate properly from ±24V down to 0V. Using discrete transistors ensures proper operation over this wide range. Conventional logic circuits and ICs aren't specified for ±24 operation and certainly not for 0V operation.

Q_1 and Q_4 control the solid-state relay through the current-limiting resistor, R_5. The relay can only turn on when both Q_1 and Q_4 are on. Otherwise, R_4 shunts away leakage current to keep the relay off. The positive power supply turns on Q_1 through resistor divider R_1 and R_2. The negative power supply turns on Q_4 through resistor divider R_6 and R_7. Q_1 turns on when its base-to-emitter voltage (the voltage across R_1) is about 0.65V.

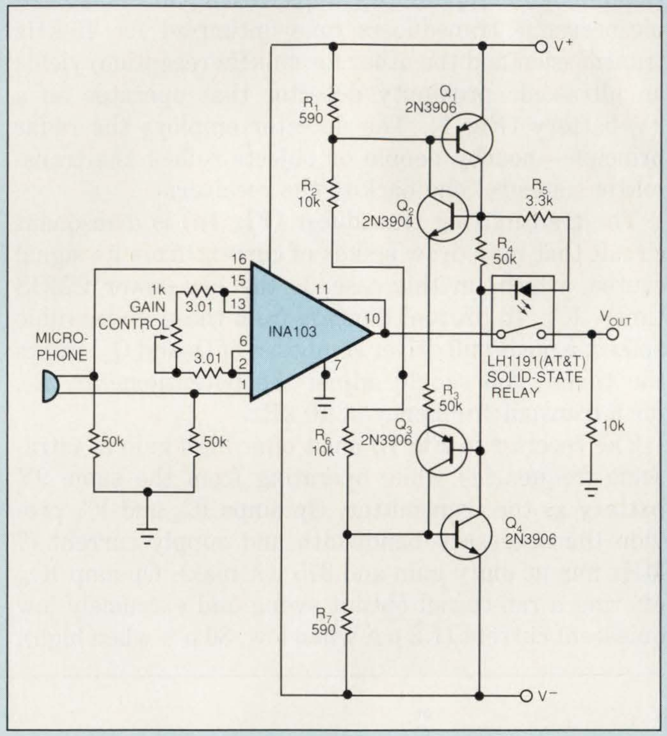

Fig 1—A $1 solid-state relay disconnects the op amp's output if the supply voltages are below a defined threshold, thereby preventing anomalies at the op amp's output.

The power-supply turn-on threshold equals

$$0.65(R_1 + R_2)/R_1.$$

With **Fig 1**'s values of R_1 and R_2, Q_1 turns on when V^+ is approximately equal to 12V. Similarly, Q_4 turns on when V^- is approximately −12V.

When both Q_1 and Q_4 are on, the sum of the power-supply voltages appears across R_4, turning on the solid-state relay. The voltage across R_4 also turns on transistors Q_2 and Q_3, forcing a positive feedback current through R_1, R_3, and R_7. This current creates hysteresis so that the solid-state relay "snaps" on and off, avoiding any possibility of turn-on oscillation even if the power supplies ramp up or down slowly. With the values shown, the amount of hysteresis is approximately 4V, and turn-off is approximately equal to ±(12V − 4V) or ±8V. **EDN BBS /DI_SIG #1112** EDN

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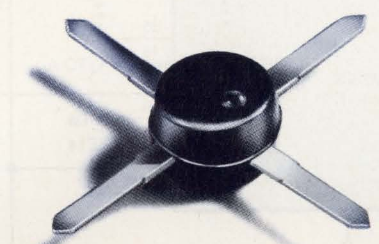

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MAR-3	DC-2000	13	12.5	10.5	8.0	+8 □	6.0	1.45	(25)
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MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
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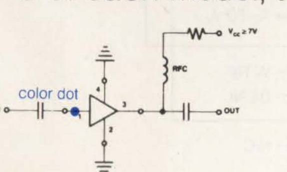

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Dual-port RAM connects microprocessors

Adrian B Cosoroaba, Fujitsu Microelectronics Inc, San Jose, CA

The dual-port RAMs in **Fig 1** connect a 32-bit 80486 to a 16-bit 68000. The RAMs mediate the difference in bus width as well as the reversed byte order of the two processors. The circuit uses four dual-port RAMs with one configured as a master device. The 80486 interfaces directly to the RAMs; the 68000 requires a 74LS139 decoder to select the proper memory devices. If both μPs try to write to the same location simultaneously, the RAMs' $\overline{\text{BUSY R}}$ lines signal the 80486 to wait. **EDN BBS /DI_SIG #1079**

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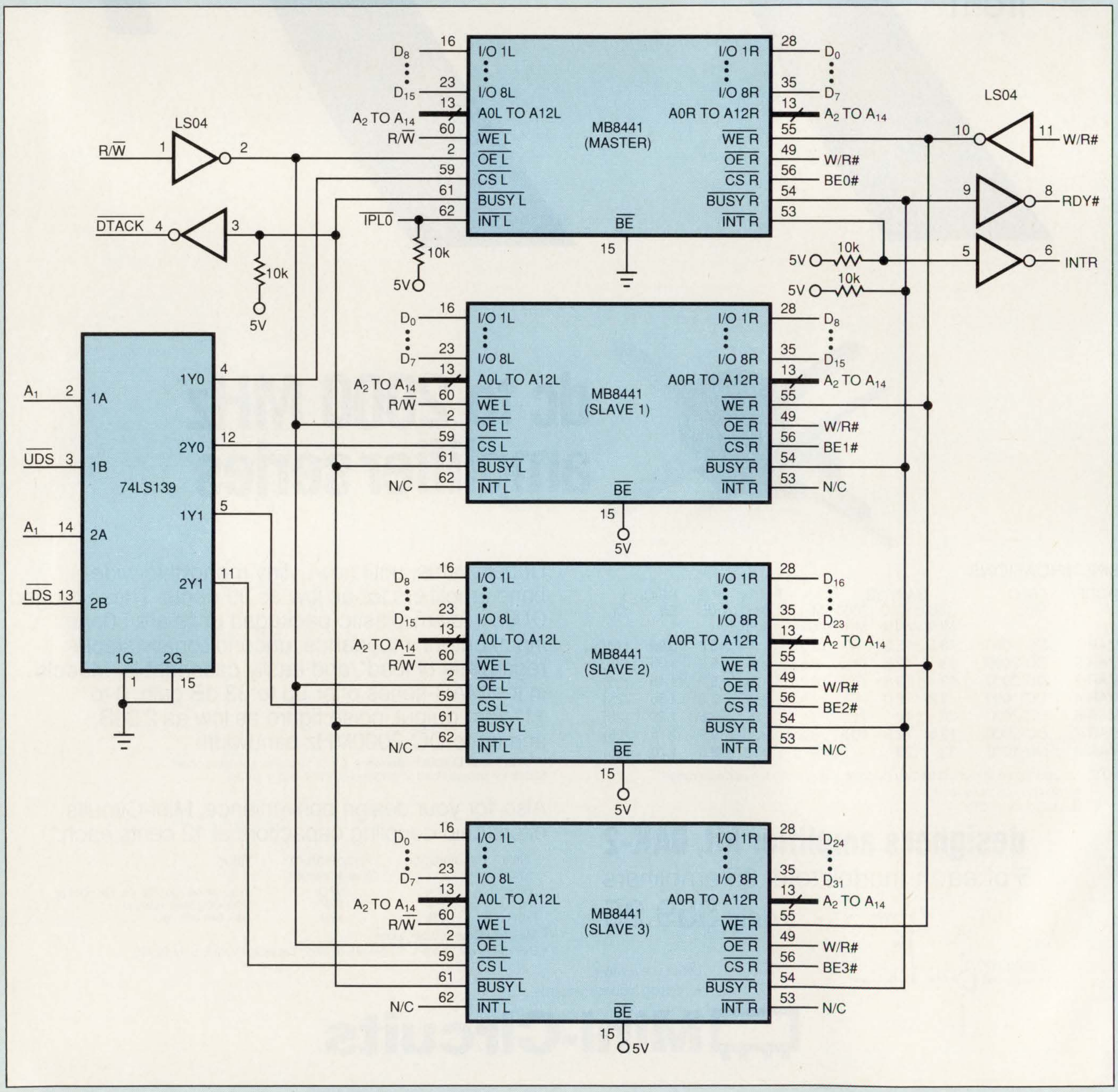

Fig 1—A bank of dual-port RAMs mediates the difference in bus width as well as the reversed byte order of the two interconnected μPs.

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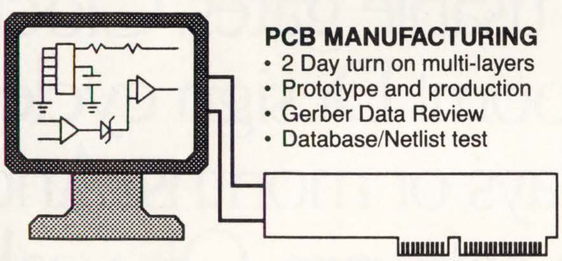

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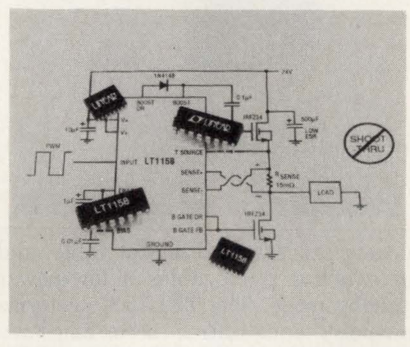

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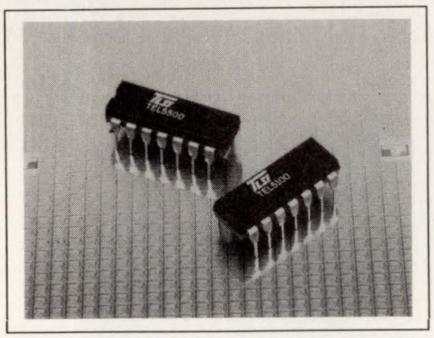

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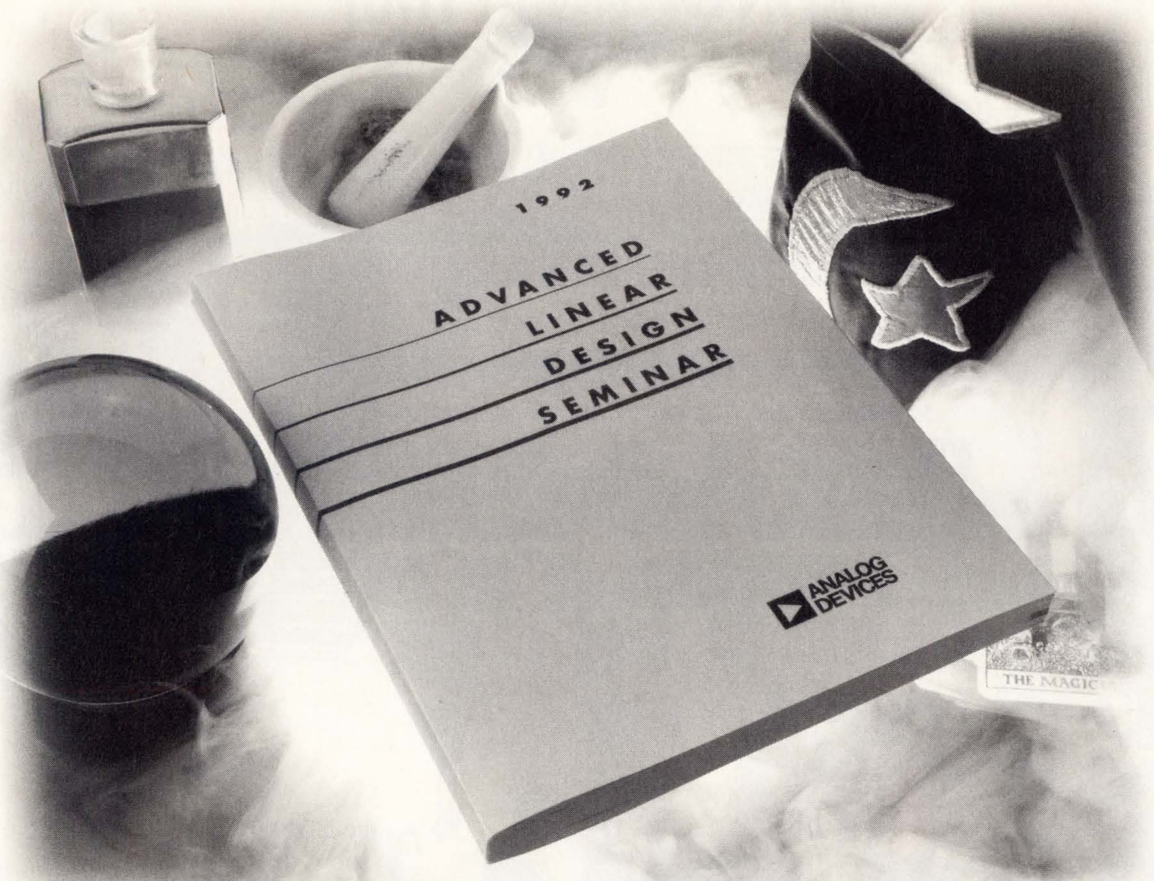


If you're one of the few engineers who realizes the world of analog design isn't all that mysterious, you'll appreciate our Advanced Linear Design Seminar. Because it's the perfect opportunity to pick up a few new tricks.

Hosted by Analog Devices, one of the leading suppliers of analog and mixed-signal ICs, and its distributors, the seminar series will include talks by prominent design wizards such as Derek Bowers, Paul Brokaw, Lou Counts, Barrie Gilbert, Walt Jung, and others.

The full-day tutorials also include solutions-oriented discussions that are geared towards showing you how to increase system performance while actually lowering overall cost. Plus you'll get free product samples, our 700-page *Amplifier Applications Guide*, other technical reference materials, and more.

Admission to the seminar is just $20, and it includes everything above, lunch, and refreshments.

So if you're a design wizard who wants to add to your repertoire of linear design tricks, it's no secret what you should do — call 1-800-ANALOGD (in Canada, call 617-937-1430) and reserve a seat today. Before they all disappear.

ANALOG DEVICES

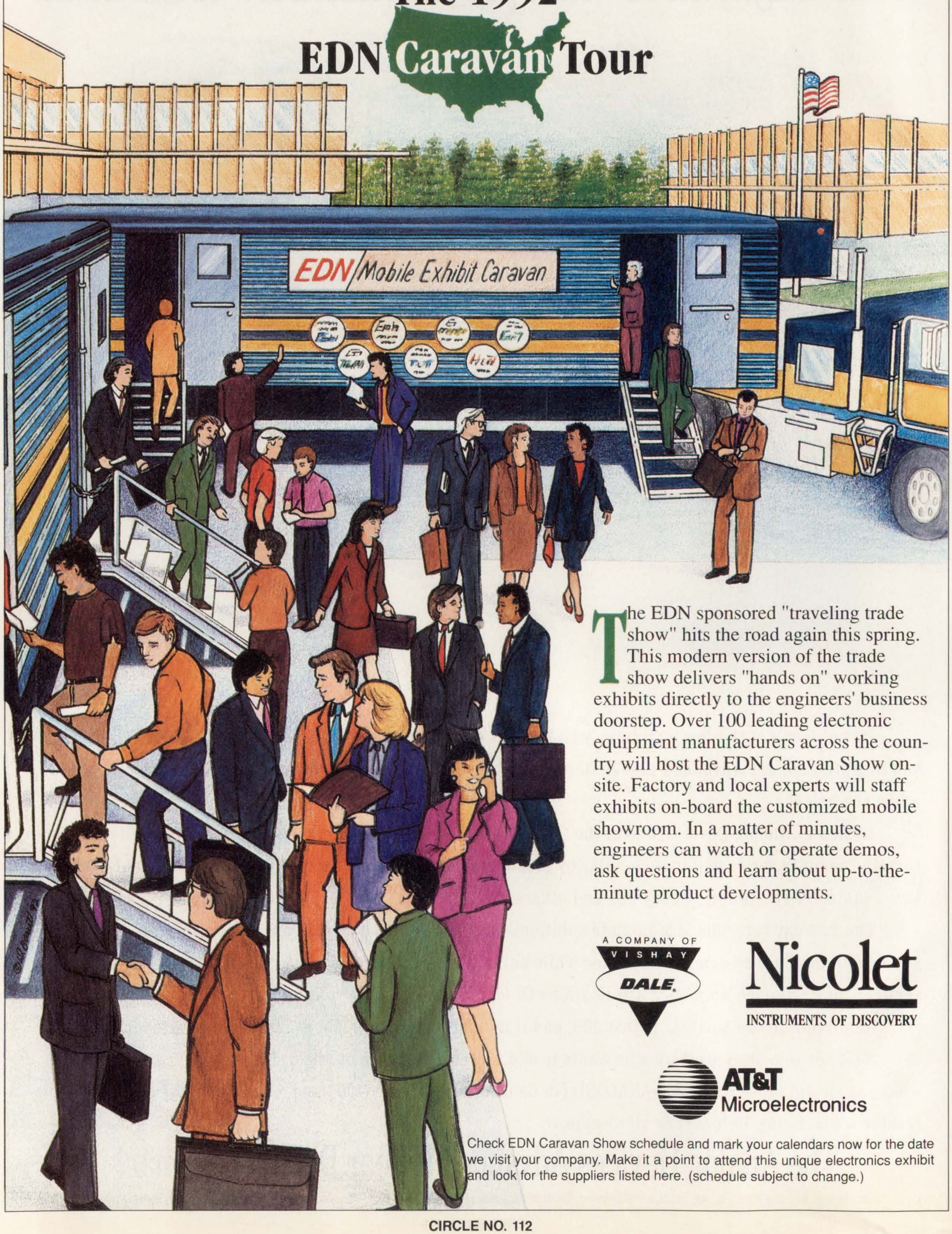
The Analog Devices Advanced Linear Design Seminar.

Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106. Headquarters: (617) 329-4700. Offices, applications support and distribution available worldwide.

CIRCLE NO. 111

EDN CARAVAN ELECTRONIC SHOW TOURS
The Electronic Trade Show on Wheels

The 1992 EDN Caravan Tour



The EDN sponsored "traveling trade show" hits the road again this spring. This modern version of the trade show delivers "hands on" working exhibits directly to the engineers' business doorstep. Over 100 leading electronic equipment manufacturers across the country will host the EDN Caravan Show on-site. Factory and local experts will staff exhibits on-board the customized mobile showroom. In a matter of minutes, engineers can watch or operate demos, ask questions and learn about up-to-the-minute product developments.

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Check EDN Caravan Show schedule and mark your calendars now for the date we visit your company. Make it a point to attend this unique electronics exhibit and look for the suppliers listed here. (schedule subject to change.)

CIRCLE NO. 112

EDN CARAVAN ELECTRONIC SHOW TOURS

The Electronic Trade Show on Wheels

DATE	TIME	LOCATION
3/16 Monday	9:00-11:00 AM	BOEING HUNTSVILLE 499 Boeing Blvd., Huntsville, AL
3/16 Monday	12:30-2:30 PM	INTERGRAPH CORPORATION Intergraph Way, Huntsville, AL
3/17 Tuesday	8:30-10:00 AM	ACUSTAR INC. 100 Electronics Blvd., Huntsville, AL
3/17 Tuesday	11:00-12:30 AM-PM	AVEX ELECTRONICS 4807 Bradford Drive, Huntsville, AL
3/17 Tuesday	1:30-3:30 PM	TELEDYNE BROWN ENGINEERING 5021 Bradford Blvd., Huntsville, AL
3/18 Wednesday	9:00-11:00 AM	SCI TECHNOLOGY (Plant 3 & 13) 13000 So. Memorial Parkway, Huntsville, AL
3/18 Wednesday	12:30-2:30 PM	SCI TECHNOLOGY (Plant 1) 8600 S. Memorial Parkway, Huntsville, AL
3/19 Thursday	1:00-3:00 PM	BNR/NORTHERN TELECOM 705 Westech Drive, Norcross, GA
3/20 Friday	9:00-10:00 AM	OKI TELECOM GROUP 437 Old Peachtree Road, Suwanee, GA
3/20 Friday	12:30-2:00 PM	RELIANCE ELECTRIC Collins Industrial Blvd., Athens, GA
3/23 Monday	9:00-10:30 AM	NCR CORPORATION 7240 Moorefield Highway, Liberty, SC
3/23 Monday	1:00-3:30 PM	NCR CORPORATION 3325 W. Platt Springs Rd., W. Columbia, SC
3/25 Wednesday	8:30-11:00 AM	AT&T PARADYNE CORPORATION 8545 126th Avenue N., Largo, FL
3/25 Wednesday	1:00-3:00 PM	GROUP TECHNOLOGIES CORP. 10901 Malcolm McKinley Dr., Tampa, FL
3/26 Thursday	9:30-12:00 AM	HONEYWELL, INC., Avionics 13350 US Highway 19 So., Clearwater, FL
3/26 Thursday	1:00-3:00 PM	SMITHS INDUSTRIES, Aero. & Defense 14180 Roosevelt Blvd., Clearwater, FL
3/27 Friday	8:30-11:00 AM	E-SYSTEMS, INC., ECI Div. 1501 72nd Street N., St. Petersburg, FL
3/27 Friday	1:00-2:30 PM	LORAL DATA SYSTEMS 6000 Fruitville Road, Sarasota, FL
3/30 Monday	9:00-11:00 AM	RACAL-DATACOM, INC. 1601 N. Harrison Parkway, Sunrise, FL
3/30 Monday	12:30-3:00 PM	MOTOROLA INC. 8000 W. Sunrise Blvd., Plantation, FL
3/31 Tuesday	8:30-10:30 AM	BENDIX/KING, Air Transport Avionics 2100 N.W. 62nd Street, Fort Lauderdale, FL
3/31 Tuesday	12:30-3:00 PM	IBM CORPORATION 1000 N.W. 51st Street, Boca Raton, FL
4/1 Wednesday	8:30-10:00 AM	ROCKWELL INTL', Collins Aviation 600 John Rodes Blvd., Melbourne, FL
4/1 Wednesday	11:00-1:00 AM-PM	HARRIS CORPORATION, ESD Palm Bay Road, Palm Bay, FL
4/1 Wednesday	2:30-4:00 PM	GRUMMAN MELBOURNE SYSTEMS 2000 NASA Blvd., Melbourne, FL
4/2 Thursday	9:00-12:00 AM	MARTIN MARIETTA CORP., ESD 12506 Lake Underhill Road, Orlando, FL
4/2 Thursday	1:30-3:30 PM	MARTIN MARIETTA CORP., MSD 5600 Sand Lake Road, Orlando, FL
4/3 Friday	9:00-11:00 AM	SIEMENS STROMBERG-CARLSON 400 Rinehart Road, Lake Mary, FL
4/3 Friday	1:00-3:00 PM	GENERAL ELECTRIC, Simulation & Control 1800 Volusia Avenue, Daytona Beach, FL
4/6 Monday	9:00-11:30 AM	IBM CORPORATION Research Triangle Park, RTP, NC
4/6 Monday	12:30-2:00 PM	NORTHERN TELECOM, INC./BNR 4001 E. Chapel Nelson Hwy., RTP, NC
4/6 Monday	2:45-4:15 PM	NORTHERN TELECOM, INC. 400 Perimeter Park Dr., Morrisville, NC
4/7 Tuesday	9:00-11:00 AM	ALCATEL NETWORK SYSTEMS 2912 Wake Forest Road, Raleigh, NC
4/7 Tuesday	1:30-4:00 PM	AT&T TECHNOLOGIES, Guilford Center Mount Hope Church Rd., McLeansville, NC
4/8 Wednesday	9:00-11:00 AM	GENERAL ELECTRIC COMPANY 1501 Roanoke Blvd., Salem, VA
4/8 Wednesday	1:30-3:30 PM	ERICSSON/GE Mobile Communications Mountain View Road, Lynchburg, VA
4/9 Thursday	9:00-11:00 AM	SPERRY MARINE, INC. Route 29 North, Charlottesville, VA
4/9 Thursday	12:30-2:30 PM	GE FANUC AUTOMATION NA, INC. US 29 & Rt 606, Charlottesville, VA
4/10 Friday	8:30-11:00 AM	E-SYSTEMS, INC., Melpar Div. 7700 Arlington Blvd., Falls Church, VA
4/10 Friday	12:30-2:30 PM	E-SYSTEMS, INC., Melpar Div. 11225 Waples Mill Road, Fairfax, VA
4/13 Monday	9:00-10:30 AM	PULSECOM INC. 2900 Towerview Road, Herndon, VA
4/13 Monday	1:30-3:30 PM	LITTON SYSTEMS, Amecom Div. 5115 Calvert Road, College Park, MD
4/14 Tuesday	9:00-10:30 AM	FAIRCHILD COMM. & ELECTRONICS 20301 Century Blvd., Germantown, MD
4/14 Tuesday	11:30-2:00 AM-PM	HUGHES NETWORK SYSTEMS, INC. 11717 Exploration Lane, Germantown, MD
4/15 Wednesday	9:00-12:00 AM	WESTINGHOUSE CORPORATION (BWI) Route 170, Linthicum, MD
4/16 Thursday	9:00-11:00 AM	ALLIED SIGNAL AEROSPACE 1300 E. Joppa Road, Baltimore, MD
4/16 Thursday	12:30-2:30 PM	AAI CORPORATION 110 Industry Lane, Cockysville, MD

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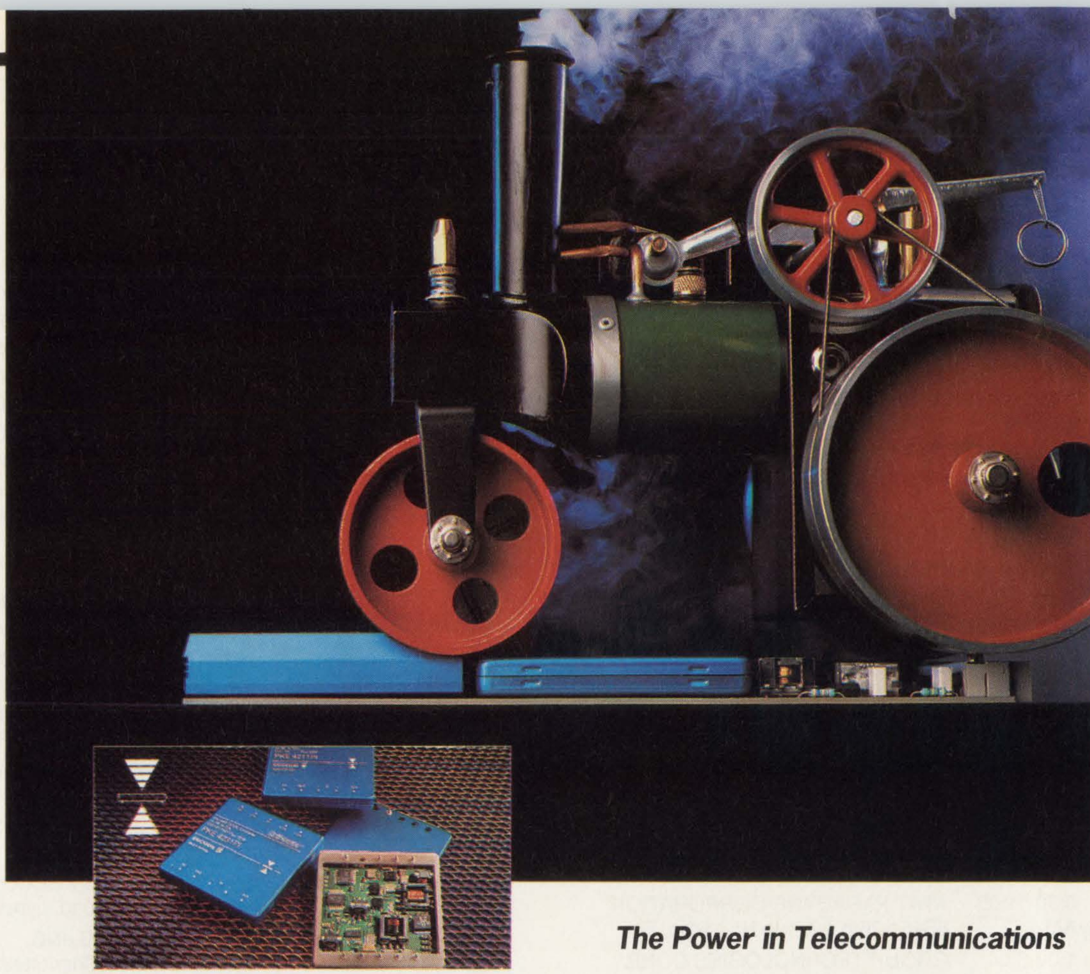
CIRCLE NO. 112



The Power in Telecommunications

The squeeze is on

Slimming is an obsession in the electronics industry as engineers face the task of making thinner cards to fit even more functions into standard racks. Once again Ericsson can help.

The new PKE is a 25-30 W DC/DC converter squeezed into a slim package little more than half the height of its predecessor, the internationally acclaimed PKA converter. The PKE is only 10.7 mm (0.42") high and has the same 3"x3" industry-standard footprint and pin out.

Having set the standard for DC/DC converters in 1983, Ericsson's new series represents a remarkable leap forward in power supply technology. The PKE needs no power derating over its entire ambient temperature range of -45 to +85 °C. Quite simply, no one else achieves this in so little space. And you can choose from versions with one, two or three regulated outputs.

Perhaps most surprisingly, performance is in no way compromised by the size reduction. In fact, the PKE is even better than the PKA. A wide input voltage of 38 to 72 VDC is complemented by 1500 VDC isolation, 80-85% typical efficiency and two million hours MTBF at +45 °C ambient.

The PKE converter from Ericsson - slim, compact and beautifully formed. Squeeze in the time to call us for more information.

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Hong Kong:	**Ericsson Components,** East Asia, Wanchai, Tel: +852-5-75 66 40 Fax: +852-834 53 69
Italy:	**Ericsson Components Europe,** Milano, Tel: +39-2-33 20 06 35 Fax: +39-2-33 20 06 41
Norway:	**Ericsson Components A/S,** Oslo, Tel: +47-2-65 01 90 Fax: +47-2-64 41 38
Sweden:	**Ericsson Components AB,** Stockholm, Tel: +46-8-757 43 84 Fax: +46-8-757 44 21
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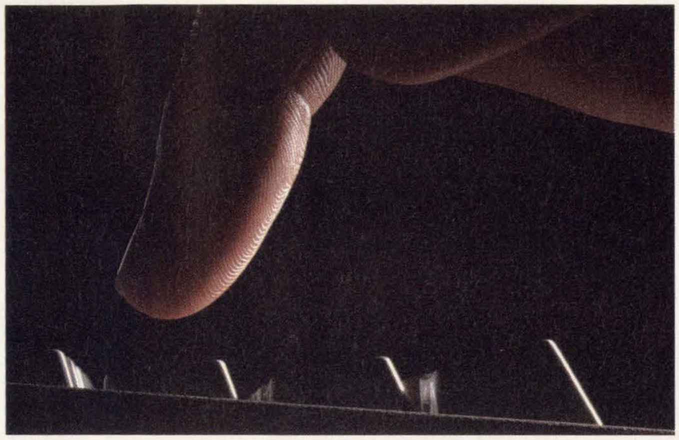
ERICSSON

CIRCLE NO. 113

IN THE TIME IT TAKES TO READ THIS AD, YOU COULD ROUTE THE WORLD'S FASTEST FPGA.



Our new push-button software makes programming other logic devices seem positively tedious.

Believe it or not, it only takes about 150 seconds to place and route a Xilinx FPGA.

It will probably take you longer to read this ad.

THE FIRST AND STILL THE FASTEST.

At Xilinx we invented the FPGA. And we've led the industry ever since.

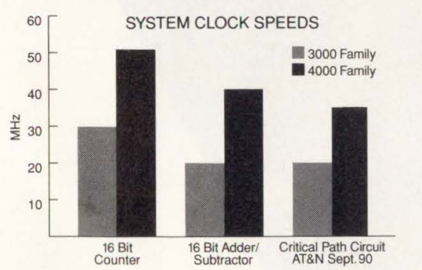
With the fastest, highest performance FPGAs available anywhere.

Today, we offer system clock speeds of 60 MHz. With on-board RAM. And on-chip wide decode.

Making our newest FPGAs ideal for everything from FIFOs to address decoding.

NEW ENHANCED SOFTWARE PROVIDES PUSH BUTTON SOLUTION.

To make Xilinx FPGAs even faster and easier to program, we've redesigned our software.



As measured by typical design benchmarks, the XC3000 family is the industry's fastest FPGA. Or at least it was until we introduced the 4000 family.

Our new version of XACT™ now comes with 200 soft macros. And fifty hard macros.

Providing automatic placing and routing for virtually all designs. With greater than 90% gate utilization.

If you've worked with Xilinx FPGAs before, you'll see improvements even before you start to place and route your design.

If you've never worked with Xilinx FPGAs before, you'll find every other logic device to be positively tedious by comparison.

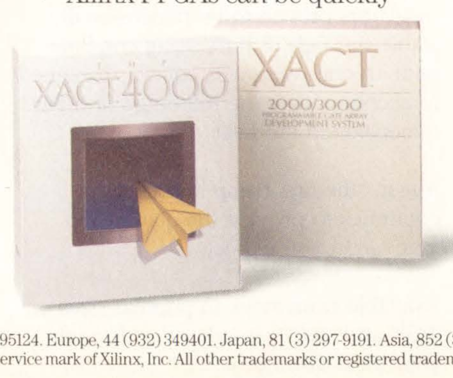
WHEN IT COMES TO SYSTEM TESTING, WE PASS WITH FLYING COLORS.

Our newest FPGAs offer you the industry's first on-chip JTAG boundary scan for easy testing of PC boards and device I/Os.

This unique Xilinx offering improves overall system testability and dramatically reduces board test costs. A major boost for those designing high-density, surface mount systems or complex, multilayer PC boards.

IF AT FIRST YOU DON'T SUCCEED, IT'S EASY TO TRY AGAIN.

Xilinx FPGAs can be quickly reprogrammed an unlimited number of times.



Our FPGAs save you an enormous amount of time right up front. And they also save you time later when you need to make those "last minute" enhancements.

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GETTING AN EDGE OVER YOUR COMPETITORS IS JUST A PHONE CALL AWAY.

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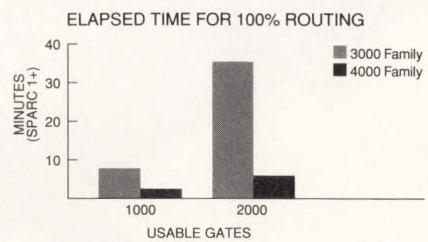

New algorithms have reduced place and route times by a factor of four.

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Call 1-800-255-7778. Or in California, 408-559-7778. And we'll send you more information on how our FPGAs can give you the competitive edge.

But you better hurry.

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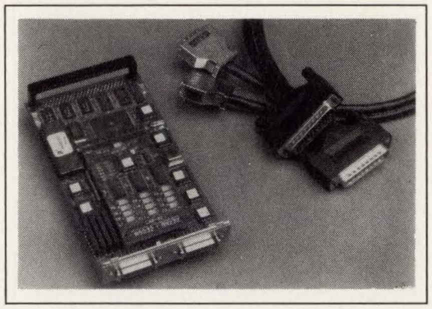
CIRCLE NO. 133

Ethernet Cards. The Interlan AT and Interlan AT TP are 8- or 16-bit ISA bus Ethernet cards. The AT board has an attached-unit interface (AUI) and a BNC connector for thick and thin Ethernet networks. The AT TP board has an AUI and an RJ-45 connector for thick and 10Base-T networks. The boards have 16 kbytes of memory-mapped RAM. A LAN Talk disk contains Novell Netware 286/386, NDIS for DOS and OS/2, and Unix Streams software drivers. $229. **Racal-Datacom Inc,** 155 Swanson Rd, Boxborough, MA 01719. Phone (800) 526-8255; (508) 263-9929. FAX (508) 263-8655. **Circle No. 363**

Sbus synchronous-communication board. The Model PT-SBS332 synchronous-communications board for the SBus employs Zilog's 16C35 Integrated Serial Communications Controller (ISCC) chip and Motorola's MC68340 Integrated Processor. It provides two serial ports that communicate at T1 (1.544 Mbps) and E1 (2.048 Mbps) rates on both ports. The board employs the company's Line Adapter Board (LABs), which are small plug-on boards that de-



termine the specific line interfaces and can be upgraded in the field. Board with 2 Mbytes of RAM and an EIA-232C interface, $1175. **Performance Technologies Inc,** 315 Science Pkwy, Rochester, NY 14620. Phone (716) 256-0200. FAX (716) 256-0791. **Circle No. 364**

Parallel COM Board. The DB-PCOMM is a parallel communication board for the VMEbus. A high-speed 32-bit I/O port transfers synchronous data at 33 Mbytes/sec and asynchronous data at 22 Mbytes/sec. The board also has a general-purpose 8-bit port. It connects to the host via a VME subsystem bus interface and a Dbus-68 interface, which permits 32-bit DMA transfers to the host. $2995. **Matrix Corp,** 1203 New Hope Rd, Raleigh, NC 27610. Phone (800) 848-2330; (919) 231-8000. FAX (919) 231-8001. **Circle No. 365**

ISA bus EEPROM boards. The PCE910 family EEPROM boards for the ISA bus use nonvolatile memory that can replace hard-disk storage. You can populate the boards with as much as 1 or 2 Mbytes of flash EEPROM. You can boot the board using an onboard BIOS, which simplifies installation and provides power-up diagnostics. $1044 (100). **Memtech Technology,** 3000 Oakmead Village Ct, Santa Clara, CA 95051. Phone (408) 970-8900. FAX (408) 986-0656. TWX 910-250-1368. **Circle No. 366**

VMEbus dynamic-RAM card. The VRAM-10 all-CMOS memory board for the VMEbus comes in five versions that have 1, 2, 4, 8, or 16 Mbytes of dynamic RAM. The maximum access time is approximately 150 nsec. The board operates from 0 to 70°C, and it draws 100

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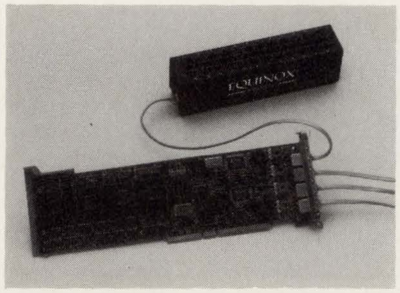
CIRCLE NO. 117

◄ For More Information on Lambda Please Circle No. 116

mA of standby current. A front-panel LED indicates 9-bit parity errors. $611. **Dynatem,** 15795 Rockfield Blvd, Suite G, Irvine, CA 92718. Phone (714) 855-3235. FAX (714) 770-3481. **Circle No. 367**

Serial I/O subsystems. The Megaplex/2 and Megaplex/RS are serial I/O subsystems for IBM PS/2 and RISC System/6000 Micro Channel Architecture computers. The systems directly connect as many as 96 serial ports to the host using a single-slot controller board. Four 24-port multiplexers connect to the controller board via 4-wire links. As many as eight host controllers can be installed in a single computer, and you can locate the multiplexers as far as 2500 ft from the controller. The 24-port Megaplex/2 and Megaplex/RS configuration, consisting of a host controller, a multiplexer, manual, and software driver, $2595 and $2695, respectively. **Equinox Systems Inc,** 14260 SW 119 Ave, Miami, FL 33186. Phone (800) 275-3500. FAX (305) 253-0003. **Circle No. 368**



Accurate to a T ... as well as B, E, J, K, R, and S type.

For your difficult temperature monitoring problems, the SR630 Thermocouple Monitor provides the power and flexibility you need. The SR630 interfaces 7 types of thermocouples, 16 independent channels of data and easily handles monitoring and logging functions as well as computer interfacing. And the easy to use front panel makes setup a snap.

And the price? At $1495, the SR630 is the complete, low cost solution you're looking for.

The SR630 Thermocouple Monitor $1495

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- 0.1 degree resolution
- B, E, J, K, R, S, and T type thermocouples
- °C, °K, °F, and mV dc readings
- 2000 point non-volatile memory
- 4 proportional analog outputs
- Audible alarm
- GPIB, RS232 and Printer interfaces

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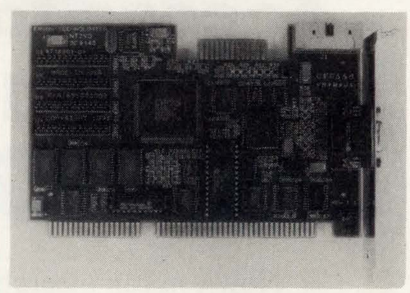
CIRCLE NO. 118

Plotter sharing card. The Jetcard/DJ is a plug-in card for Hewlett-Packard's Designjet inkjet plotter. The card provides six serial RJ-11 ports to support multiple users; it plugs into a modular I/O slot of the plotter. Four of the ports can handle data-transfer rates as fast as 115,200 baud. A DOS-compatible utility programs a computer's COM1 through COM4 ports to attain the high baud rates. A 2-Mbyte buffer version, $995. **Excellink Inc,** 1430 Tully Rd, Suite 415, San Jose, CA 95122. Phone (408) 295-9000. FAX (408) 295-9011. **Circle No. 369**

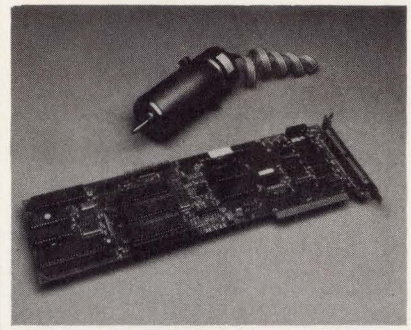


Super VGA card. The CVC550 super VGA card employs dual-port video RAM (VRAM) that's accessible to the host CPU and the board's 82C453 VGA controller IC from Chips and Technologies. The board comes with 512 kbytes or 1 Mbyte of VRAM and supports both noninterlaced and interlaced monitors that have resolutions as high as 1024×768 pixels and 256 colors. A 512-kbyte version, $255. **Ergon Technologies Inc,** Box 748, Ridgeland, MS 39158. Phone (601) 856-4121. TLX 585326 **Circle No. 370**

Brushless dc amplifier. The ALC-CM is a transconductance amplifier for driving brushless dc motors. It accepts

±10V dc inputs or accepts optionally a pulse-width-modulation input and a direction command. Units can deliver 15A continuous and 25A pk from a 180V dc power supply or 10A continuous and 15A pk from a 360V dc power supply. The amplifier can also accommodate a 50- to 400-Hz, single-phase, 8 to 264V ac power supply. $750. Delivery, 8 to 10 weeks ARO. **Automation Inc,** Box 7746, Ann Arbor, MI 48107. Phone (313) 662-3707. FAX (313) 662-3707.
Circle No. 371

Motion-controller boards. The DMC-611, -621, and -631 are 1-, 2-, and 3-axis, respectively, ISA bus motion-controller boards. They provide ±10V dc outputs having 12-bit resolution. The boards have latches that can capture real-time position signals within 200 nsec. Other features include linear and circular interpolation along a 2-D path; electronic gearing to synchronize multiple axes to a master axis; and gear ratio changes during motion. You can specify 255 linear or arc segments of motion using encoders operating at 2M counts/sec. DMC-611, $995; DMC-621, $1495;

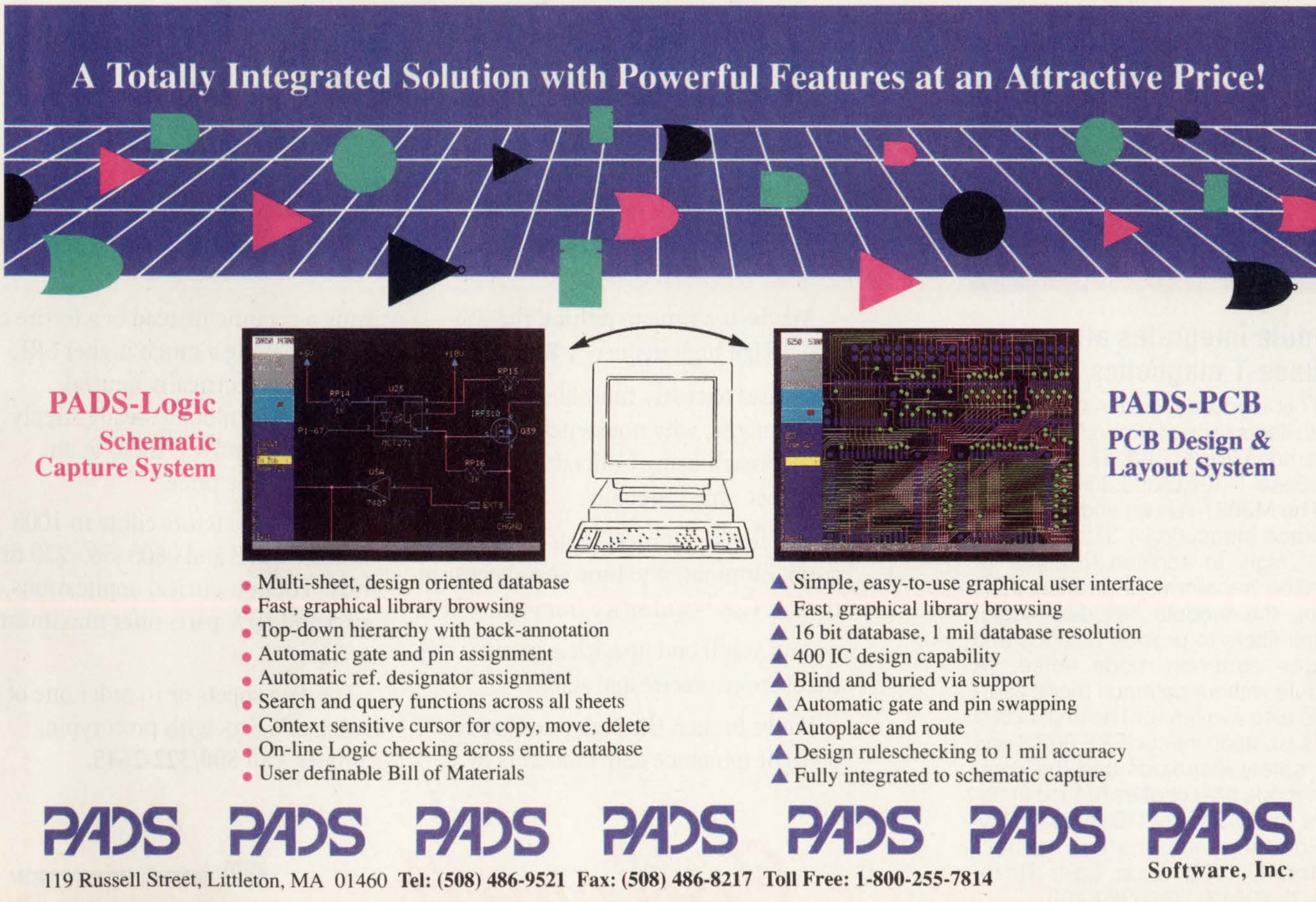


DMC-631, $1995. **Galil Motion Control Inc,** 575 Maude Ct, Sunnyvale, CA 94086. Phone (408) 746-2300. FAX (408) 746-2315. **Circle No. 372**

Fast SCSI-2 coprocessor card. The Silicon Express II is a Busmaster Card for the Macintosh computer Nubus. The board features a 10-Mbyte/sec data-transfer rate on a Fast SCSI-2 port. The board supports the fast Nubus Block Mode data transfers of Quadra-series computers. The board has removable SCSI and power terminations. $1295. **Atto Technology Inc,** Baird Research Park, 1576 Sweet Home Rd, Amherst, NY 14228. Phone (716) 688-4259. FAX (716) 636-3630. **Circle No. 373**

Flat-panel display. A flat-panel display subsystem is available for Sun SPARCstations. The subsystem consists of a single-slot SBus graphics-controller card and a 16-in. AC plasma display. The display has a screen resolution of 1280×1024 pixels and measures 3½-in. in depth. $5500. **Integrix Inc,** 1200 Lawrence Dr, #150, Newbury Park, CA 91320. Phone (805) 375-1055. FAX (805) 375-2799. **Circle No. 374**

Voice-processing board. The Dialog/41D combines an Intel 80188 μP and Motorola's 56001 DSP chip on an ISA bus board. The board features selectable voice-coding algorithms, DTMF detection, and a telephony interface. DTMF cut-through capability lets you access voice mail when calling from a mobile phone or poor-quality line. $1150. **Dialogic Corp,** 300 Littleton Rd, Parsippany, NJ 07054. Phone (201) 334-8450. **Circle No. 375**



CIRCLE NO. 121

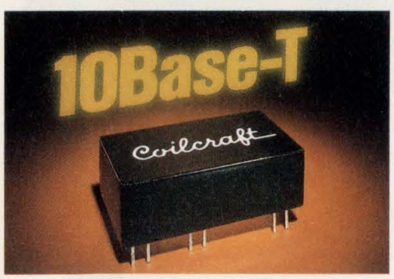
Low cost current sensors for 60 Hz applications

Coilcraft's low-cost current sensor is intended for 60 Hz applications. This compact part (roughly 3/4" square by 1/2" thick) is encapsulated in a protective epoxy coating with a 1/8" diameter through-hole. The sensor functions as the secondary of a current transformer while the conductor carrying the current to be measured serves as the "one turn primary."

Min. wall thickness of the hole is 0.5 mm which meets IEC 380, VDE 0730, and other requirements when used with an insulated conductor. Typical output voltages range from 12 mV at 1 Amp to 90 mV at 10 Amps.

For more information, contact **Coilcraft**, 1102 Silver Lake Road, Cary IL 60013. 708/639-6400.

CIRCLE NO. 122



Module integrates all 10Base-T magnetics

This module provides all the low-pass filters, transformers and common mode filters needed to implement a 10Base-T (IEEE 802.3i) interface.

The M2021-A is an encapsulated, package measuring 1.375" x .725" x .500" high. In addition to a pair of isolation transformers and low-pass filters, the module includes single-ended filters to provide balance and reduce common mode noise. (A module without common mode filtering is also available.) The unit's 2000 Vrms isolation meets IEEE 802.3 and IEC safety standards and the common mode filter chokes reduce emissions for FCC and VDE compatibility.

For more information, contact **Coilcraft**, 1102 Silver Lake Road, Cary IL 60013. 708/639-6400.

CIRCLE NO. 123

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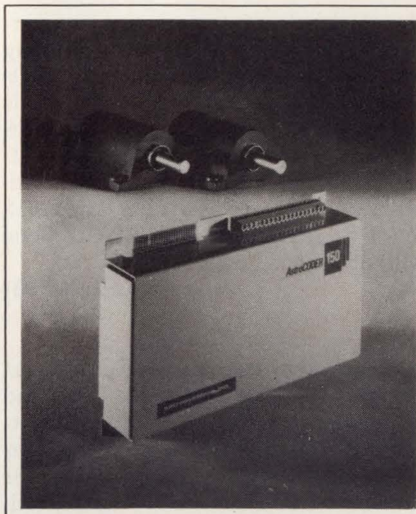
1102 Silver Lake Road, Cary IL 60013
800/322-2645 Fax 708/639-1469

CIRCLE NO. 124



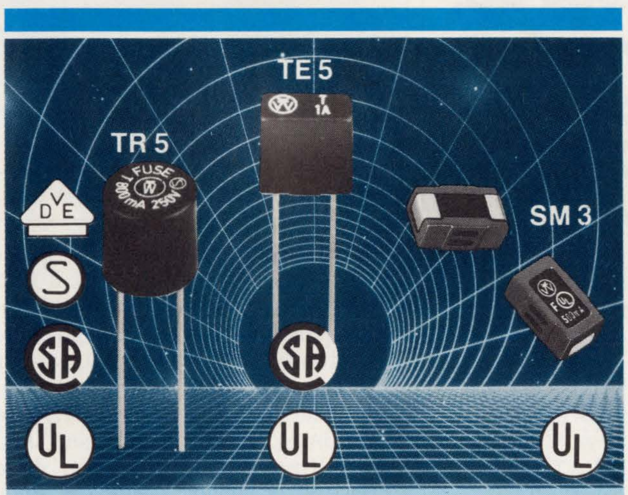
Position encoder. The Astrocoder/150 uses resolver-based position transducers to measure absolute shaft position on either one or two shafts. Unit capabilities include built-in tachometer, offset, reset, power supply, and speed alarm. When operating with two shafts, the unit can provide a control signal to keep the shaft positions synchronized. The encoder provides four simultaneous outputs per shaft—digital parallel position data; RS-422 or RS-485 serial position, speed, and status; dc voltage level; and high- or low-speed alarms. $500 (OEM qty). **Astrosystems Inc,** 6 Nevada Dr, Lake Success, NY 11042. Phone (516) 328-1600. FAX (516) 328-1658. TWX 510-223-0411. **Circle No. 376**

Surface-mount fuses. Accu-Guard devices are thin-film, surface-mount fuses. Available in EIA standard 1206 packages, the units have ten ratings ranging from 200 mA to 2A at 32V. Open-circuit resistance is 20 MΩ min, and operating range spans −55 to +125°C. $0.25 (10,000). Delivery, stock to six weeks ARO. **AVX Corp,** 801 17th Ave S, Myrtle Beach, SC 29577. Phone (803) 946-0562. **Circle No. 377**

Switches. The pc-board-mountable Series 92 switches are oil- and watertight to IP 67 specifications. They feature a membrane cap for a complete front-panel seal. The actuator is available as an indicator, pushbutton, or illuminated pushbutton and comes in a variety of lens colors. From $2.50 (1000). **EAO Switch Corp,** 198 Pepe's Farm Rd, Milford, CT 06460. Phone (203) 877-4577. FAX (203) 877-3694. Delivery, stock to six weeks ARO. **Circle No. 378**

Laser diodes. These InGaAsP/InP laser diodes operate at rates ranging to 622 Mbps. They are available in 14-pin PGT2030 and 4-pin PGT2110 packages that feature an optional cooler. Output power equals 2 mW, and operating range spans −40 to +85°C. PGT2030 device, $695. **Ericsson Components Inc,** 403 International Pkwy, Richardson, TX 75081. Phone (214) 669-9900. FAX (214) 680-1059. **Circle No. 379**

Solid-state relay. The QB00FM solid-state relay is designed for ac, bidirectional, and high-voltage dc switching in military applications. The unit features 500V rms I/O isolation; switching capability is 10A at 150V for ac application. The current rating is 15A in dc service. The relay employs power FETs for the output and has an on-resistance of 0.1Ω. It's available



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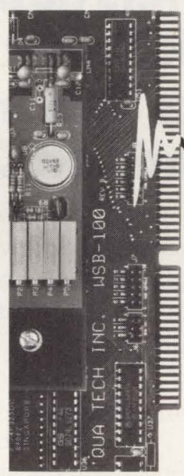

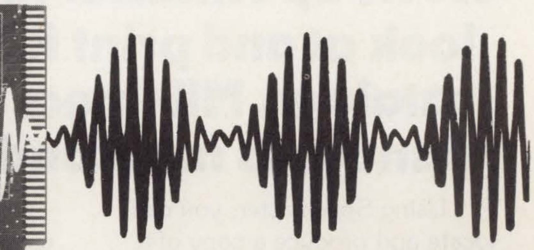

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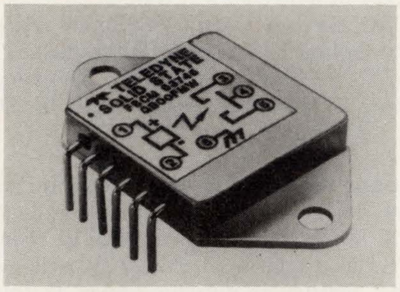
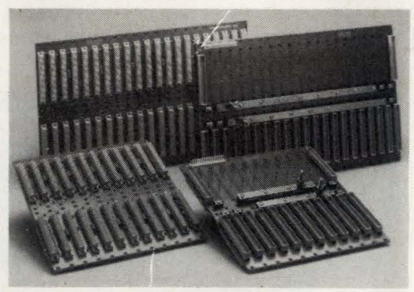


screened to W and Y levels of MIL-R-28750. $120 (OEM qty). Delivery, stock to eight weeks ARO. **Teledyne Solid State,** 12525 Daphne Ave, Hawthorne, CA 90250. Phone (213) 777-0077.
Circle No. 380

Servo controller/driver. The AMC2200 provides servo control for both brush dc motors and brushless ac/dc motors; it's available in 500 and 1000W versions. The device is protected against overvoltage caused by regenerative braking with high inertia loads. Onboard LEDs display status. Unit efficiency equals 95% min. The controller/driver operates with a single 12V supply plus bus voltage. $295 (10) for a 500W version. **Advanced Motion Controls Inc,** 518 Water St, Princeton, WI 54968. Phone (414) 295-3500. FAX (414) 295-3504.
Circle No. 381

Miniature transformers. These transformers are designed for use in T3 and E3 interface circuits. They are also suitable for use in the STS-1 applications operating at 51.84 Mbps—the lower echelon of SONET. The units are available in through-hole and surface-mount versions. They operate over a −40 to +65°C range and feature 1500V rms isolation. $2.25 (1000). **Pulse Engineering Inc,** 7250 Convoy Ct, San Diego, CA 92111. Phone (619) 268-2400. FAX (619) 268-2515. **Circle No. 382**



VME backplanes. These backplanes are available in versions with 3 to 21 slots. Each slot features inboard termination. The units employ an 8-layer construction. Three signal layers are spaced so as to minimize crosstalk problems. The planes feature distributed power bugs. $935 for a 21-slot J1-J2 unit. **Elma Electronic Inc,** 41440 Christy St, Fremont, CA 94538. Phone (510) 656-3400. FAX (510) 656-3783.
Circle No. 383

PGA sockets. Series MD PGA sockets are available in five grid sizes ranging from 11×11 to 17×17. Molded standoffs improve soldering. The insulators are compatible with vapor-phase and IR reflow soldering operations. All contacts are rated for 3A. Operating range spans −55 to +125°C. $0.01 to $0.018/line (OEM qty). **Mark Eyelet Inc,** 63 Wakelee Rd, Wolcott, CT 06716. Phone (203) 756-8847. FAX (203) 755-9410.
Circle No. 384

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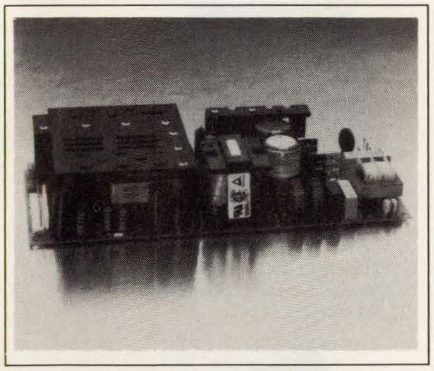

Power supplies. Series FLU4-150 units are 150W, quad-output, open-frame switching power supplies. Five models provide primary outputs of 5V and secondary output combinations of 5, 12, 15, and 24V. All outputs are fully isolated; primary outputs are ±5% adjustable. The supplies have an autoranging input range of 90 to 265V. The series offers indefinite short-circuit protection, soft start, overvoltage protection, and a 32-msec holdup time with a 115V input. $189. **Power General,** 152 Will Dr, Canton, MA 02021. Phone (617) 868-6216. FAX (617) 868-3215.

Circle No. 385

Tubular solenoids. L-10 Series tubular solenoids produce as much as 208 ounces of force. The units are available in two lengths—1.125 and 2 in.—and push and pull operating types. Both types are available with 6, 12, 24, or 110V dc coils. Power ratings range from 5W continuous to 100W pulse duty. $8 (OEM qty). Delivery, six to eight weeks ARO. **Liberty Controls Inc,** 500 Brookforest Ave, Shorewood, IL 60435. Phone (815) 725-2241. FAX (815) 725-6571. **Circle No. 386**

Switch with TTL-compatible driver. The VSW-2-50DR device is a 3-nsec, GaAs, spdt reflective switch with a built-in TTL-compatible driver housed in a hermetic ceramic-metal package. The unit operates over a dc to 5-GHz range with a 1.3-dB insertion loss. Isolation at 5 MHz is 80 dB. The 50Ω unit operates over a −55 to +85°C range and consumes 120 mW. $42.95. **Mini-Circuits,** Box 350166, Brooklyn, NY 11235. Phone (718) 934-4500. FAX (718) 332-4661. TLX 6852844. **Circle No. 387**

LED arrays. Series 5682F and 5684F arrays feature two and four T-1 LEDs, respectively. The units are available in a variety of models—low-current (2

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CIRCLE NO. 128

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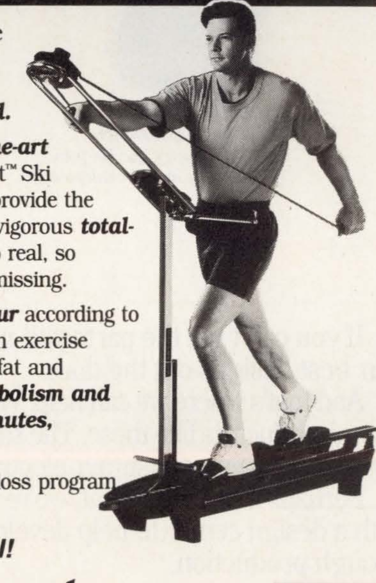

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CIRCLE NO. 129

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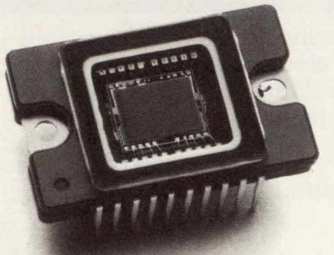

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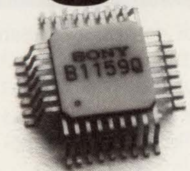

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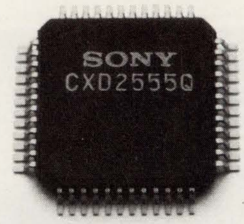

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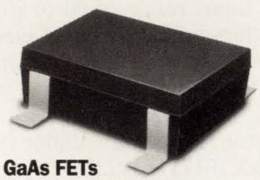

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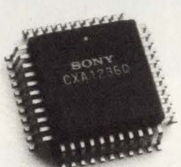

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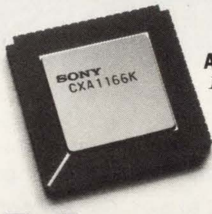

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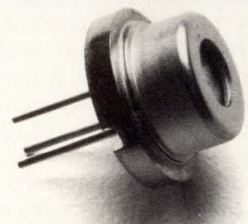

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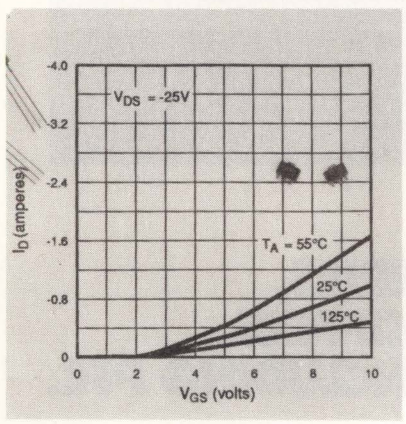
mA) versions with built-in resistors for 5 and 12V operation, red-green bicolor models, or with high-brightness red, green, yellow, amber, and blue LEDs. The black thermoplastic housings carry a UL 94V-0 rating. From $0.96 and $1.80 for dual and quad arrays, respectively. Delivery, stock to six weeks ARO. **Industrial Devices Inc,** 260 Railroad Ave, Hackensack, NJ 07601. Phone (201) 489-8989. FAX (201) 489-6911. **Circle No. 388**

Inductors. These conformally coated inductors are available in four package sizes—4.5-mm EC22, 10-mm EC24, and 14-mm EC36 and EC46. Inductance values range from 0.1 μH to 82 mH. Values down to 0.022 μH are available on special order. Standard tolerance equals either 10 or 20%. $0.042 (25,000). **3L Global Electronics,** 2915 Anvil St N, Saint Petersburg, FL 33710. Phone (813) 343-2679. FAX (813) 343-4410. **Circle No. 389**



P-channel MOSFETs. TP25D family P-channel MOSFETs are available in SOT-89 and SOT-92 packages as well as die form. They have a 2.4V max gate threshold voltage and drain-to-source breakdown levels of 350 and 400V. Drain-to-source on-resistance equals 25Ω max. TN2540N8 SOT-89 unit, $0.69 (1000). Delivery, stock to six weeks ARO. **Supertex Inc,** 1350 Bordeaux Dr, Sunnyvale, CA 94089. Phone (408) 744-0100. FAX (408) 734-5247. **Circle No. 390**

Digital panel meters. The A-3000 Series digital panel meters (DPMs) consist of a basic chassis that incorporates the digital display, operational circuitry, and power supply. Users can plug input-circuit modules into this basic chassis to measure dc current or

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CIRCLE NO. 131

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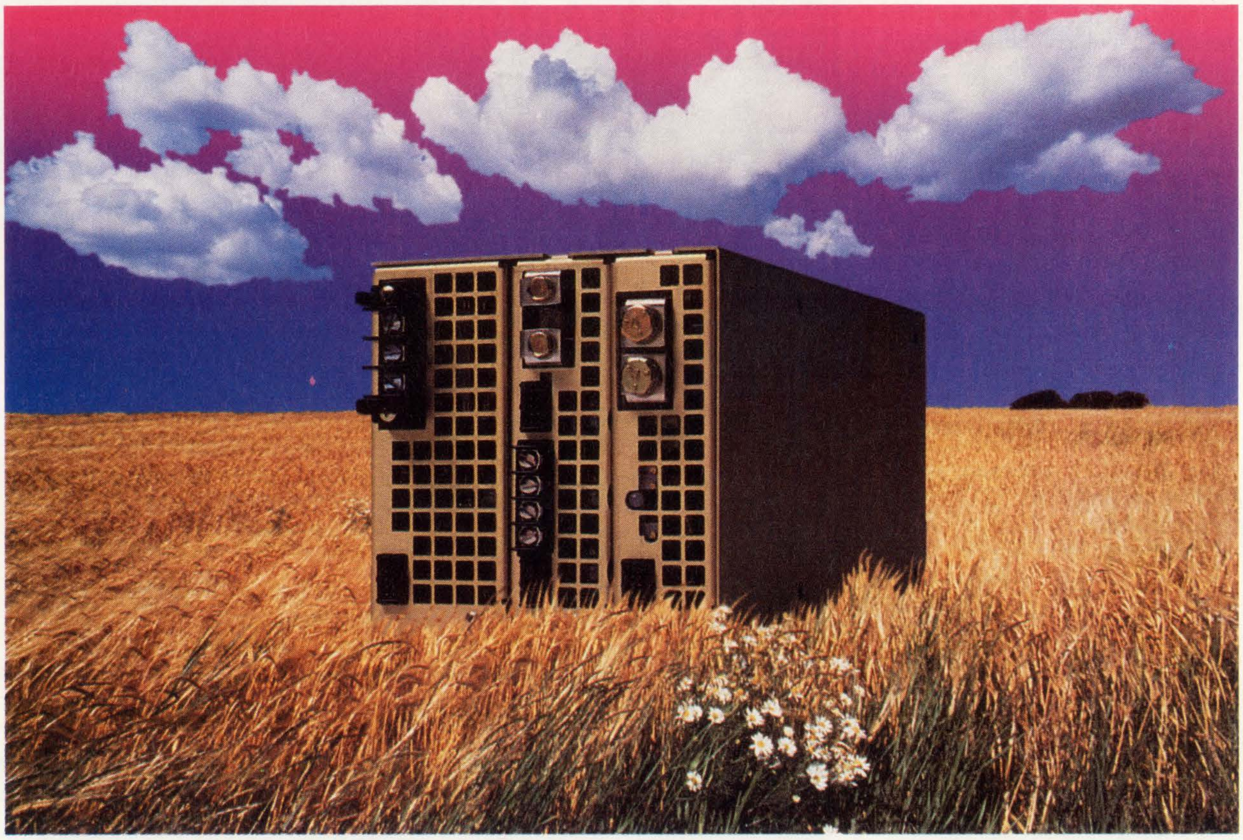

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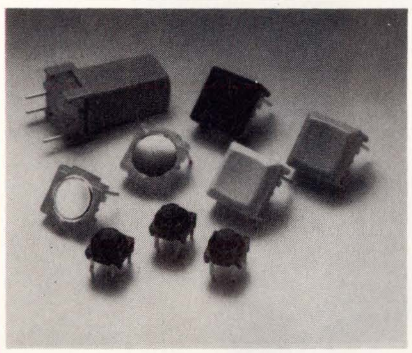
For Literature or Information

CIRCLE NO. 115

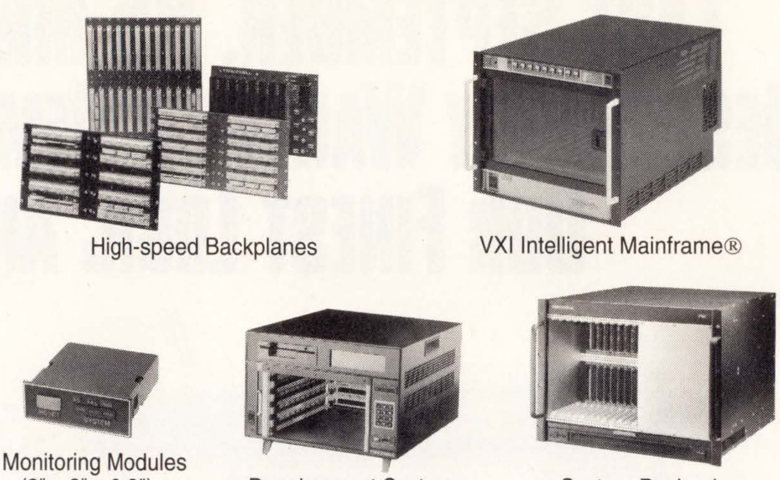
voltage, ac average voltage or current, ac true rms voltage or current, frequency, and ohms. Users can also configure the unit to serve as a thermocouple monitor, temperature detector, process monitor, or strain gauge. Basic chassis, $141; input modules, $32 to $154. **Selco Products Co,** 7580 Stage Rd, Buena Park, CA 90621. Phone (800) 257-3526; (714) 521-8673. FAX (714) 739-1507. **Circle No. 391**

Transistors. The LS-311 npn and LS-351 pnp dual transistors are surface-mount devices characterized for low noise and matched for current gain and V_{BE}. Current gain ranges from 150 to 2000 for LS-311 versions and from 150 to 500 for LS-351 models. $1.87 (1000). **Linear Integrated Systems Inc,** 310 S Milpitas Blvd, Milpitas, CA 95035. Phone (408) 263-8401. **Circle No. 392**



Switches. These key switches are available in two families—700 Series and 720 Series. The 700 Series has contact ratings of 30V ac at 10 mA. Operating range spans 20 to 85°C. Series 720 switches are rated for 20V at 50 mA and operate over a −10 to +85°C range. Maximum life times are 3×10^6 and 10^6 operations for 700 and 720 units, respectively. Series 700, $0.38; Series 720, $0.22 (1000). Delivery, stock to eight weeks ARO. **Mepcopal,** 11468 Sorrento Valley Rd, San Diego, CA 92121. Phone (619) 453-0332. FAX (619) 481-1123. **Circle No. 393**

DC/DC converters. The PKA 2323PI and 2325PI converters offer dual floating outputs of 12 or 15V. Power output is limited to 30W. The converters provide a full power output over a −45 to +85°C range. Input-output isolation equals 500V dc. $98 (250). **Ericsson Components Inc,** 403 International Pkwy, Richardson, TX 75085. Phone (214) 669-9900. **Circle No. 394**



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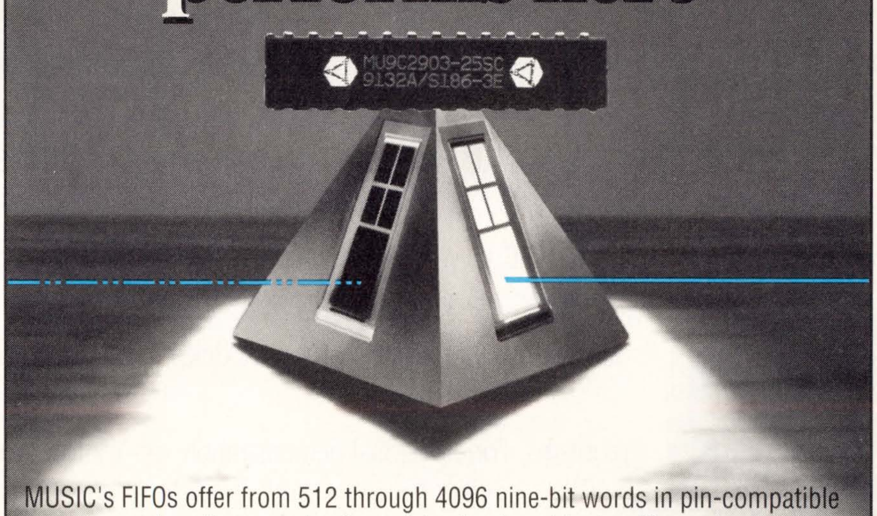

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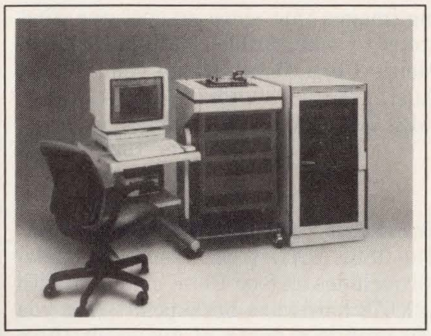
IEEE-488.2 interface. The Personal 488/MM is an IEEE-488.2 interface board for Ampro's miniature IBM PC-compatible computers. The board, a so-called Minimodule, plugs into the PC and matches its 3.6×3.8-in. form factor. Versions of the PCs, which are intended for embedded-control applications, run several operating systems, including MS-DOS, PC-DOS, DR-DOS, MS-Windows, Interactive Systems Unix, and SCO Unix. To support the varied needs of embedded-system developers, the interface vendor offers a variety of software drivers. $395. **IOtech Inc,** 25971 Cannon Rd, Cleveland, OH 44146. Phone (216) 439-4091. FAX (216) 439-4093. **Circle No. 405**

Futurebus+ interface for logic analyzers. The 92DM911 is a Futurebus+ interface package for the vendor's DAS 9200 logic-analysis systems. The package, which interfaces with the bus via a single-slot 12-system-unit card, requires that you equip the analyzer with two of the firm's Centurion cards. The system performs bus-based timing analysis at 100 MHz and, even with 128-bit data paths, acquires state information on all three phases of every bus transaction in real time. The data display uses Futurebus+ mnemonics. $9950; analyzer equipped to work with the package, less than $58,000. Delivery, eight weeks ARO. **Tektronix Inc,** Test & Measurement Group, Box 1520, Pittsfield, MA 01202. Phone (800) 426-2200. **Circle No. 406**

Safety-test unit. The STU 120/240 performs electrical-safety tests on 50- or 60-Hz ac-line-operated equipment that draws as much as 24A at 120V or 16A at 240V. The unit, which requires no calibration, measures leakage current and 25A ground continuity; it also measures rise of resistance. Interlocks prevent improper operation, and circuit breakers safeguard the unit. $24,995. **Compliance Plus,** 325 Ayer Rd, Harvard, MA 01451. Phone (508) 772-2278. **Circle No. 407**



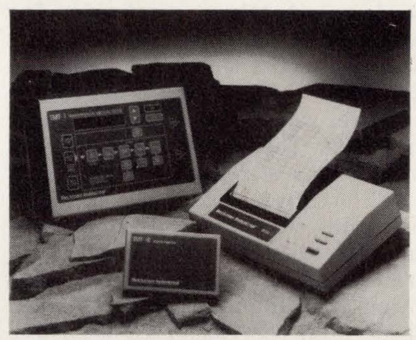
Mixed-signal system. The mixed-signal ATS system characterizes, analyzes, and debugs mixed-signal ICs and multichip modules—especially digital-intensive modules; modules that have clock speeds in hundreds of MHz; and modules that must be tested using DSP techniques. The system, which handles data rates as high as 400 Mbps/channel and provides 100-psec timing accuracy, can contain analog instrumentation that operates to 1 GHz. A 224-pin configuration with 400-MHz digital and 600-MHz analog capability, $630,000. **Integrated Measurement Systems Inc,** 9525 SW Gemini Dr, Beaverton, OR 97005. Phone (503) 626-7117. FAX (503) 644-6969. **Circle No. 408**

Keypad-programmable dc power supplies. The DPS series includes four members having maximum outputs of 12.5, 25, 40, and 125V. Output power is approximately 80W at full voltage. All outputs are adjustable to zero. To improve resolution and increase output current, the first three units have a low range in which the maximum voltage is about 40% of that on the high range. The 3-digit displays indicate the voltage and current. $429. **Kepco Inc,** 131-38 Sanford Ave, Flushing, NY 11352. Phone (718) 461-7000. FAX (718) 767-1102. TWX 710-582-2631. **Circle No. 409**

14-bit PC or Macintosh-compatible spectrum analyzer. The R380 acquires as many as 100 ksamples/sec. It has two channels, a dynamic range of 85 dB, and a 16k-word buffer for each channel. It performs FFTs to 8k points. $1995. **Rapid Systems Inc,** 403 N 34th St, Seattle, WA 98103. Phone (206) 547-8311. FAX (206) 548-0322. TLX 265017. **Circle No. 410**

12-bit waveform-acquisition board for ISA bus. The 4-channel R1222 system has differential inputs, five programmable gain ranges, 1M word of memory, and a single ADC with a maximum acquisition rate of 2 Msamples/sec. A PC can host eight of the units. $4995. **Rapid Systems Inc,** 403 N 34th St, Seattle, WA 98103. Phone (206) 547-8311. FAX (206) 548-0322. TLX 265017. **Circle No. 411**

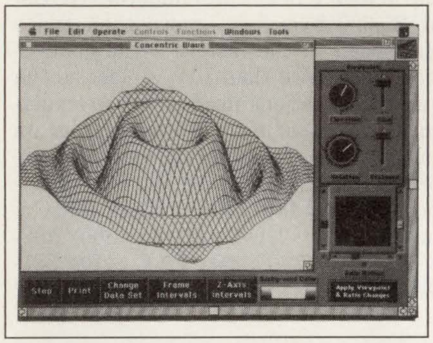
High-speed download option for ICEs. The UEM series parallel option ($500) allows downloading programs to the vendor's in-circuit emulators (ICEs) at 25,000 bytes/sec—more than twice the speed of the fastest serial connections and more than 10× as fast as the serial connections used by most emulators. Downloading a 1-Mbyte program takes 40 sec. The emulators support the 68000, 68302, 80186/188, and Z180 families. **Softaid Inc,** 8300 Guilford Rd, Columbia, MD 21046. Phone (800) 433-8812; (410) 290-7760. FAX (410) 381-3253. **Circle No. 412**



Signal injector for LAN and telecom wiring. The $195 TMT-10 signal injector works with the vendor's TMT-1 LAN system tester. Together, the instruments let you test and certify LANs that use unshielded twisted-pair wiring. The instruments first test the network wire on its spool. Then they perform a 6-function test on the installed wiring. An optional printer provides a certification printout. $2745 for both units. **Beckman Industrial Corp,** 3883 Ruffin Rd, San Diego, CA 92123. Phone (619) 495-3200. FAX (619) 268-0172. TLX 249031. **Circle No. 413**

Deep-memory plug-ins for fast-sampling DSO. The 7234 unit is a 4-channel plug-in for the vendor's 7200 modular DSO (mainframe, $17,000). The plug-in unit ($19,500 with its long-memory option) can store 1 million points on one channel, 500,000 points on each of two channels, or 200,000 points on all four channels. The unit takes 200 Msamples/sec on each channel. The 7242B 2-channel plug-in ($22,900 with long memory) lets you configure the DSO with four simultaneous-sampling 1-Gsample/sec channels, each having 1M word of memory. **LeCroy Corp,** 700 Chestnut Ridge Rd, Chestnut Ridge, NY 10977. Phone (800) 553-2769; (914) 425-2000. FAX (914) 425-8967. TWX 710-577-2832.

Circle No. 414



Surface-plotting package for Labview. Surfaceview comprises a set of virtual instruments for National Instruments' Labview data-acquisition software, which runs on Apple Macintosh PCs. The package, which plots gridded data at regular or irregular X and Y intervals, lets you control the viewpoint, color, grids, and other parameters from the Labview block diagram. $250. **Metric Systems,** 1506 Taron Dr, Round Rock, TX 78681. Phone (512) 388-4458. FAX (512) 244-7203. **Circle No. 415**

Variable-resolution ADC board for ISA bus. The VF900 board uses a V/F converter and can digitize an analog signal with a resolution of 10 to 18 bits. It has four differential inputs and provides programmable gain. The board also has 16 digital I/O lines and a 12-bit DAC. It makes 1000 conversions/sec at 10 bits, 30 conversions/sec at 15 bits, and 4 conversions/sec at 18 bits. $495. **Real-Time Devices Inc,** 820 N University Dr, State College, PA 16803. Phone (814) 234-8087. FAX (814) 234-5218.

Circle No. 416

Data-acquisition software with movie display. Labview 2 data-acquisition software—a graphical-language compiler that lets you automate experiments without conventional programming—can now display Quicktime "movies." For example, if a test fails, you can have the software display moving images that show an operator what steps to take. $1995. **National Instruments Corp,** 6504 Bridge Point Pkwy, Austin, TX 78730. Phone (800) 433-3488; (512) 794-0100. FAX (512) 794-8411.

Circle No. 417

Emulator for 80186/88EA and XL. The 186EA/XL UEM in-circuit emulator includes an 8 or 16-bit emulator with 131,072 hardware breakpoints that you can nest to a depth of five levels. Also included is a source-level debugger that couples real-time-performance analysis results to your C source code. You can specify areas of memory as read-, write-, and fetch-protected. $7500. **Softaid Inc,** 8300 Guilford Rd, Columbia, MD 21046. Phone (800) 433-8812; (410) 290-7760. FAX (410) 381-3253. **Circle No. 418**

Receiver for GPS frequency and time data. The GPStar 5-channel multiplexed receiver simultaneously receives time and frequency information transmitted by five Global Positioning Satellites. According to the vendor, the unit, which produces universal time codes with 100-nsec accuracy, provides atomic-clock accuracy at a price that is 40% below that of competing products. $3995. **Odetics,** 1515 S Manchester Ave, Anaheim, CA 92802. Phone (714) 774-5000. FAX (714) 774-9432. **Circle No. 419**

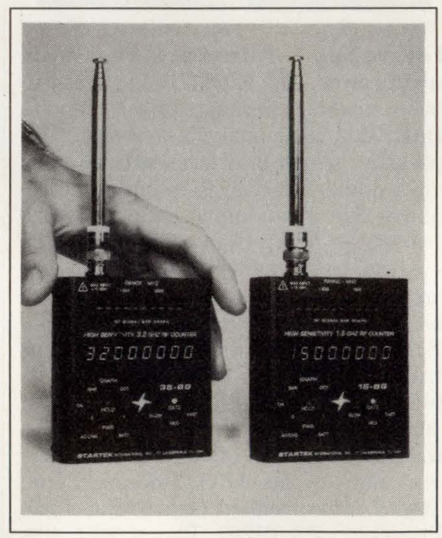
4000-count bar-graph DMMs. The D981, a handheld unit with ½-in. LCD numerals, has five dc voltage ranges from 400 mV to 1 kV, four ac voltage ranges, and five frequency ranges to 1 MHz. It also measures temperature, resistance to 40 MΩ, ac and dc current to 10A, and capacitance to 40 μF. The D927 has fewer ranges but has an unfused 20A current range. D981, $130; D927, $69. **Protek,** Box 59, Norwood, NJ 07648. Phone (201) 767-7242. FAX (201) 767-7343. **Circle No. 420**

DC-to-26.5-GHz power and voltage meter. The URV 35 level meter operates from ac or batteries. By combining it with any of a range of probes and sensors, you can adapt it to signals of varying levels and frequencies. The instrument provides both analog and digital displays. $2310 plus RF head, Delivery, eight weeks ARO. **Rohde & Schwarz Inc,** 4425 Nicole Dr, Lanham, MD 20706. Phone (301) 459-2810. FAX (301) 459-2810. TWX 510-223-0414.

Circle No. 421

Pattern-matching software. MS-DOS-based Genmatch software applies pattern-recognition techniques to complex frequency and time measurements. The vendor provides both a stand-alone version and a set of libraries that you can link into C programs. You define a nominal signal and provide tolerances for features or segments. $3500. **Genias Corp,** 2006 Woodrun SE, Lowell, MI 49331. Phone (800) 443-6427; (616) 897-5252. FAX (616) 897-0306. **Circle No. 422**

84-pin PLCC to 28-pin DIP adapters for Mach 130 and 230. The 2-in.-square 84PL/28D6-ZL and ZAL-MACH130 let IC programmers designed to accommodate DIP devices program these AMD μP chips. There are two types of replaceable sockets—a clamshell type that accommodates LCCs and plastic leaded chip carriers (PLCCs) and an auto-eject socket for PLCCs. ZL version, $200; ZAL version, $155. **EDI Corp,** Box 366, Patterson, CA 95363. Phone (209) 892-3270. FAX (209) 892-3610. **Circle No. 423**

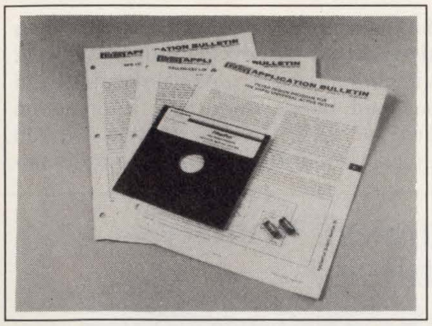


RF bar-graph frequency counters. The pocket-size 15-BG and 35-BG are sensitive RF detectors as well as counters with 8-digit LED displays. The first unit operates from 1 MHz to 1.5 GHz; the second, from 1 MHz to 3.5 GHz. You can choose among three gate times. With the longest gate (25 sec), the units' resolution is 10 Hz. The 3.4×3.8×1-in. units operate from three to five hours from rechargeable NiCd battery packs. 15-BG, 1.5-GHz unit, $220; 35-BG 3.5-GHz unit, $265. **Startek International Inc,** 398 NE 38th St, Fort Lauderdale, FL 33334. Phone (305) 561-2211. FAX (305) 561-9133. **Circle No. 424**

Handwriting recognition. Coup-de-Plume (stroke of the pen) is software that recognizes handwritten characters. It is part of a family of products for implementing pen-based applications. The supplier claims that the software recognizes discrete characters and cursive script words, independent of the style of the writer. $189. **J H Shannon Associates Inc,** Box 597, Chapel Hill, NC 27514. Phone (919) 929-6863. **Circle No. 395**

Speaker-design software. CALSOD 2.50 helps design and optimize loudspeaker systems. It simulates the sound pressure and impedance response of individual loudspeaker drivers. It works with multiple drivers and includes a circuit optimizer for crossover networks. AU$449. **Audiosoft,** 128 Oriel Rd, West Heidelberg 3081, Melbourne, Australia. Phone/FAX (3) 497-4441. **Circle No. 396**

Filter-design software. Filter Pro is a software package for active-filter design. It comes on a 5¼-in. floppy disk and includes programs that help design filters using the supplier's UAF42 universal active-filter IC. Separate programs help with Sallen-Key lowpass filters; multiple-feedback, lowpass filters;



and state-variable lowpass, highpass, bandpass, and band-reject (notch) filters. Free of charge. **Burr-Brown Corp,** Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. **Circle No. 397**

PLD/FPGA design converter. The Minc/Viewdraw interface links Viewlogic's Viewdraw schematic-capture system with Minc's PLD and FPGA design-synthesis tools. You create a schematic with Viewdraw using a special library provided with Minc's PLDesigner and PGADesigner tools; Viewdraw then creates an EDIF 2 0 0 netlist to be read by PLDesigner or PGADesigner. The interface is a standard feature in PLDesigner Systems 500, 5000, 400, 700, and 7000; it's an option in Systems 200 and 300. $450. **Minc Inc,** 6755 Earl Dr, Colorado Springs, CO 80918. Phone (719) 590-1155. **Circle No. 398**

Mathematical-analysis software for Windows. Mathematica 2.0 software for technical computing is now available for Windows. It contains two parts: a kernel, which performs computations, and a front end, which handles interactions with the user. The front end takes advantage of Windows capabilities; it provides interactive documents, known as notebooks, in which text, graphics, annotations, and sound can be mixed with mathematical input. $995; upgrades from DOS versions, $125. **Wolfram Research Inc,** 100 Trade Center Dr, Champaign, IL 61820. Phone (217) 398-0700. **Circle No. 399**

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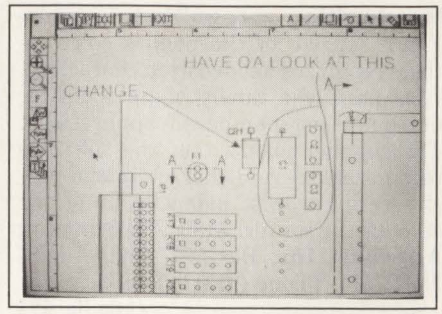

Real-time Unix system. Aria is a Unix system designed for distributed computer systems in the real-time market. The initial product runs on 68030-based Motorola MVME147S series single-board computers. Versions for other single-board computers will be available later in the year. Single-copy development kit, $9000. **Integrated Systems Inc,** 3260 Jay St, Santa Clara, CA 95054. Phone (408) 980-1500. FAX (408) 980-0400. **Circle No. 402**

C++ on IBM framework. AIX SDE Integrator/6000 integrates Green Hills C++ with IBM's AIX software-development environment Workbench/6000 (a framework based on Hewlett-Packard's Softbench technology). It provides C++ compiling and debugging on IBM RISC System/6000 workstations, allowing users to take advantage of the supplier's editor, program builder, static analyzer, and debugger. From $1400. **Oasys,** 1 Cranberry Hill, Lexington, MA 02173. Phone (617) 862-2002. **Circle No. 403**

Software for estimating software costs. Costar, a software cost-estimating tool, is for managers who need estimates of a software project's duration, staffing, and cost. It allows managers to make preliminary estimates during a project's initial definition, and then produce more and more accurate forecasts as the project's definition is refined. The package runs on any VAX system with VMS or on IBM PCs and compatibles. $800. **Softstar Systems,** 28 Ponemah Rd, Amherst, NH 03031. Phone (603) 672-0987. **Circle No. 404**

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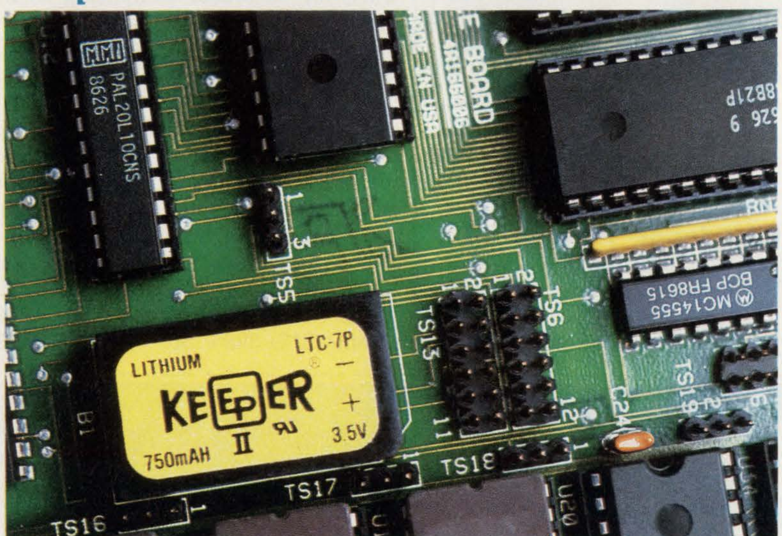

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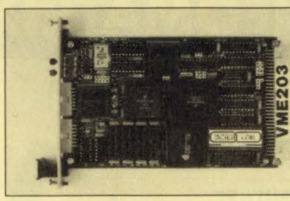

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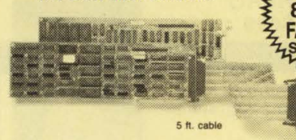

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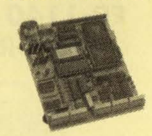

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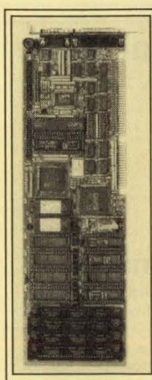

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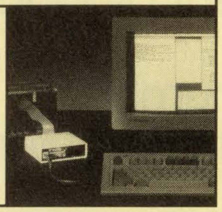

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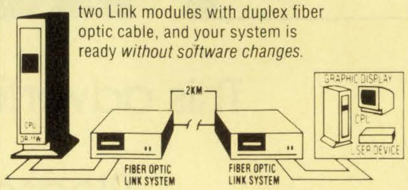

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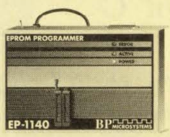

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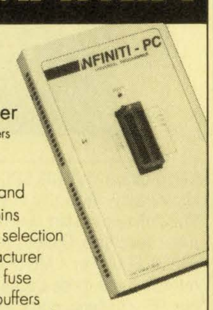

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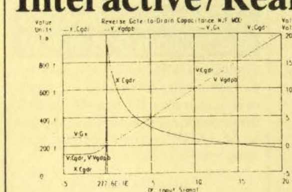

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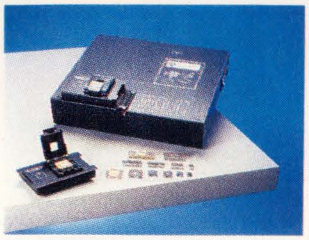

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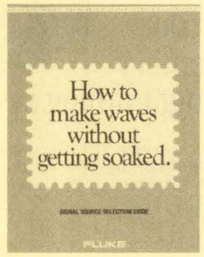

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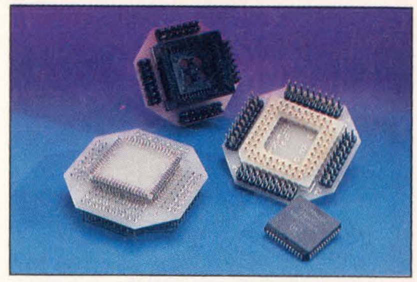

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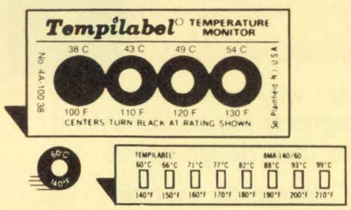

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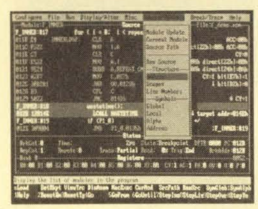

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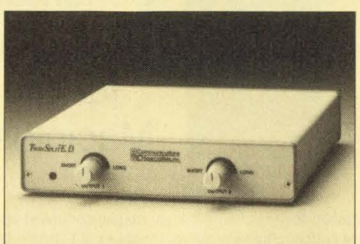

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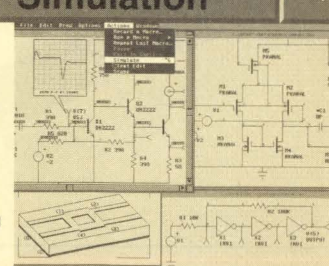

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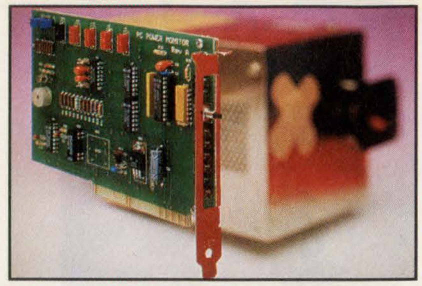

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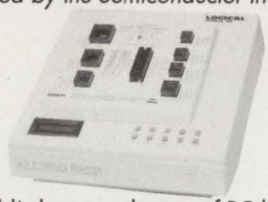

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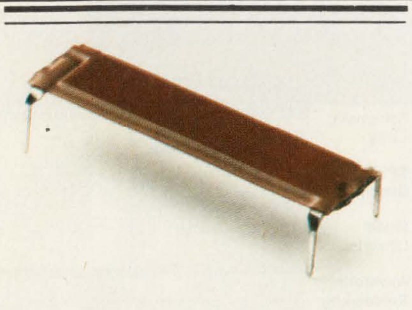

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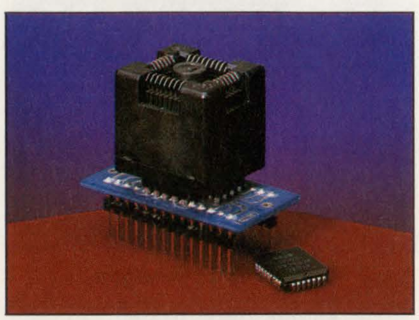

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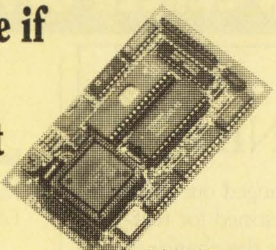

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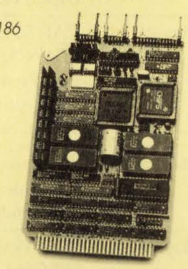

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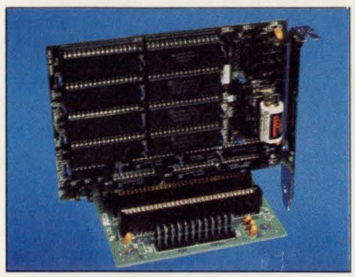

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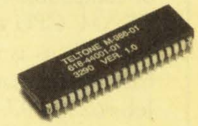

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1992 Recruitment Editorial Calendar

Issue	Issue Date	Ad Deadline	Editorial Emphasis
News Edition	Apr. 30	Apr. 16	ASICs SPECIAL ISSUE FPGAs and EPLDs • CICC Hot Products • ASICs Regional Profile: Northern California
Magazine Edition	May 7	Apr. 16	Communications/Networks Test & Measurement • Surface-Mount Components • Power Sources • Electro Show & Products Issue
ELECTRO SHOWGUIDE & PRODUCT SPOTLIGHT		Apr. 3	A free page available to all advertisers running a full page in 2 out of 3 Electro issues
News Edition	May 14	Apr. 30	Graphics Technology Computers & Peripherals
Magazine Edition	May 21	Apr. 30	Analog ICs • Analog CAE • PC Board CAE Tools • Programmable-Logic Devices
News Edition	May 28	May 14	Communication ICs • CAE Software • Regional Profile: Texas, Oklahoma, Kansas
Magazine Edition	June 4	May 14	ASICs/PLDs • DSP Software CAE/Software/Interoperability Digital ICs & Semiconductors
News Edition	June 8	May 21	CAE SPECIAL ISSUE EDA/CASE Supplement • DAC Hot Products • Software Engineering • Diversity Special Series
Magazine Edition	June 18	May 28	Microprocessors • Electromechanical Devices • ICs & Semiconductors
SOFTWARE ISSUE	June 18	May 28	SOFTWARE ENGINEERING SPECIAL ISSUE (To be polybagged with the June 18th Magazine Edition issue)
News Edition	June 25	June 11	MILITARY ELECTRONICS SPECIAL ISSUE • DSP Hardware • Military Electronics Regional Profile: Florida, Alabama
Magazine Edition	July 6	June 11	INTERNATIONAL PRODUCT SHOWCASE—Vol. I Hardware & Interconnect Software • ICs & Semiconductors • Power Sources
Magazine Edition	July 20	June 25	INTERNATIONAL PRODUCT SHOWCASE—Vol. II Computers & Peripherals Components • CAE • Test & Measurement
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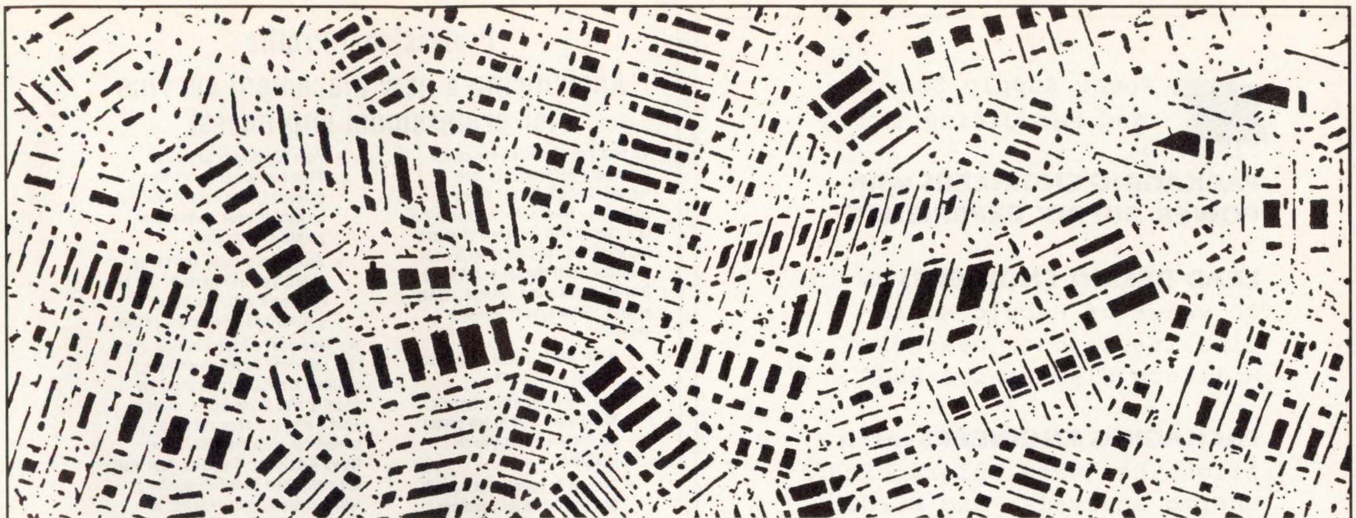

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Dallas, TX

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Customer Support Engineers (2)

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Professional Profile

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Degrees (List)	Major Field	GPA	Year Degree Earned	College or University

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EXPERIENCE

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Duties and Accomplishments ____ Industry of Current Employer ____________

Reason for Change ____________

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Job Title ____________

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Salary ______ Duties and Accomplishemnts: ______

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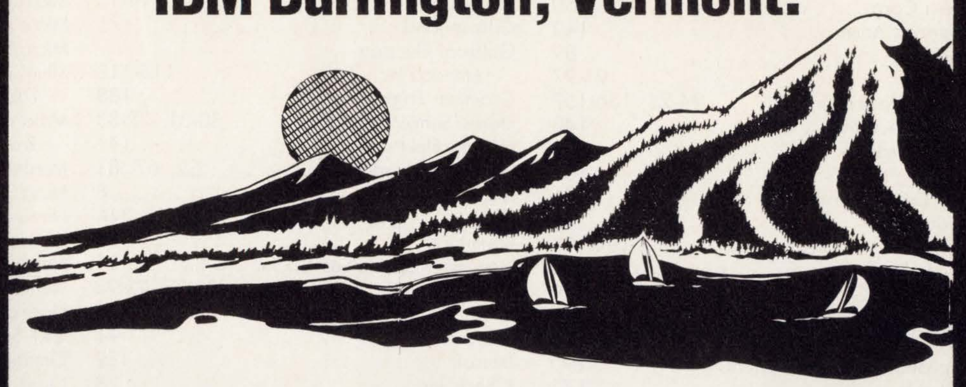

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Circuit Design

Will design CMOS circuitry for RISC-based microprocessor functions. Includes custom SRAM cache design, complex logic dataflow circuitry, random logic, IO, clocking and other circuitry in custom microprocessor layouts. Requires BSEE or higher with emphasis on Computer Engineering or Circuit Design. Ability to design complex CMOS or Bi CMOS circuits and perform circuit analysis and verification is essential, along with minimum of 3 years circuit design experience in industry. CMOS, VLSI, digital circuit design is a prerequisite.

Physical Design

Responsible for CMOS VLSI chip physical design of RISC microprocessor in advanced CMOS technology. Includes using state-of-the-art CAD tools to perform chip layout, wiring and chip timing analysis. A BSEE or higher, with emphasis on Computer Engineering or Circuit Design, is essential, along with at least 3 years of physical design experience in industry. RISC and CMOS, VLSI design experience (chip layout/wiring) necessary. Background in microprocessor design desirable.

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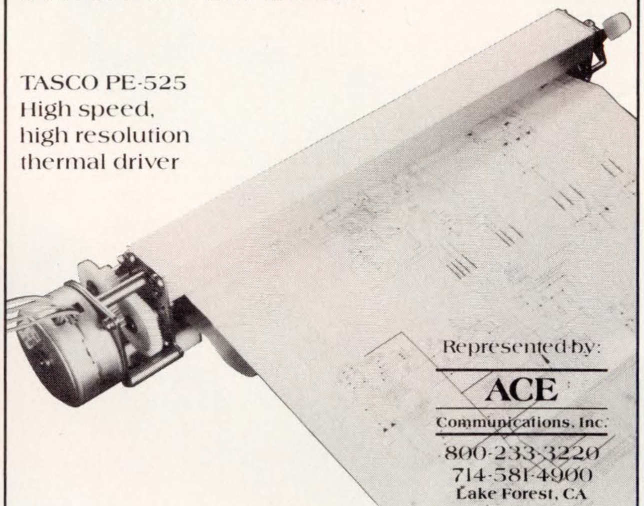

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EDN Asia will be circulated to 28,000 engineering professionals in Asia and will be published in three languages: English, Chinese and Korean.

EDN·ACRONYMS & ABBREVIATIONS

A/D—analog-to-digital
BBS—bulletin-board system; an electronic bulletin board accessed via personal computers using modems
CAD—computer-aided design
CAE—computer-aided engineering
CAM—content-addressable memory
CMOS—complementary metal-oxide semiconductor
CMRR—common-mode rejection ratio
CPU—central processing unit
DAC—digital-to-analog converter
DAM—data-addressable memory
DDE—Dynamic Data Exchange; a formal protocol that Windows programs can use to exchange data while running
DIP—dual in-line package
DLL—Dynamic Link Library; a program fragment or module loaded and unloaded as needed while a program runs
DMA—direct memory access; generally a faster data-transfer method than processor-managed data transfers
DOS—the disk operating system IBM PC-compatibles use
ECL—emitter-coupled logic
EEPROM—electrically erasable programmable read-only memory
EPLD—erasable programmable logic device
EPROM—erasable programmable read-only memory
FDDI—fiber distributed data interface
FIFO—first in, first out
FPGA—field-programmable gate array
GUI—graphical user interface
HMOS—high-performance metal-oxide semiconductor
IC—integrated circuit
I/O—input-output
LAN—local-area network
LSB—least significant bit
MOS—metal-oxide semiconductor
MSB—most significant bit
MSI—medium-scale integration
NMOS—N-type metal-oxide semiconductor
NRE—nonrecurring engineering
OLE—Object Linking and Embedding; a mechanism for embedding one Windows program in another Windows program
PAL—programmable array logic
PC—IBM-compatible personal computer
pc—printed circuit
PLD—programmable logic device
PROM—programmable read-only memory
RAM—random-access memory
RC—resistance-capacitance
ROM—read-only memory
S/H—sample and hold
SPICE—a public-domain analog-circuit simulation program from UC Berkeley
SSI—small-scale integration
TLB—translation look-aside buffer
TSR—terminate-and-stay-resident program; a kluge that, to a slight degree, makes up for the lack of multitasking in DOS
TTL—transistor-transistor logic
VDMAD—Virtual DMA Driver; a Windows multitasking mechanism
VPICD—Virtual Programmable Interrupt Controller Driver; a Windows multitasking mechanism

This list includes acronyms and abbreviations found in EDN's Special Report, Technology Updates, and feature articles.

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Isolation (dB)	42	31	20	50	40	28
1dB Comp. (dBm)	18	20	22.5	20	20	24
RF Input (max dBm)	—	20	—	22	22	26
VSWR "on"	1.25	1.35	1.5	1.4	1.4	1.4
Video Bkthru (mV,p/p)	30	30	30	30	30	30
Sw. Spd. (nsec)	3	3	3	3	3	3
Price, $ (1-9 qty)	YSWA-2-50DR (pin) 23.95 ZYSWA-2-50DR (SMA) 69.95			YSW-2-50DR (pin) 19.95 ZYSW-2-50DR (SMA) 59.95		

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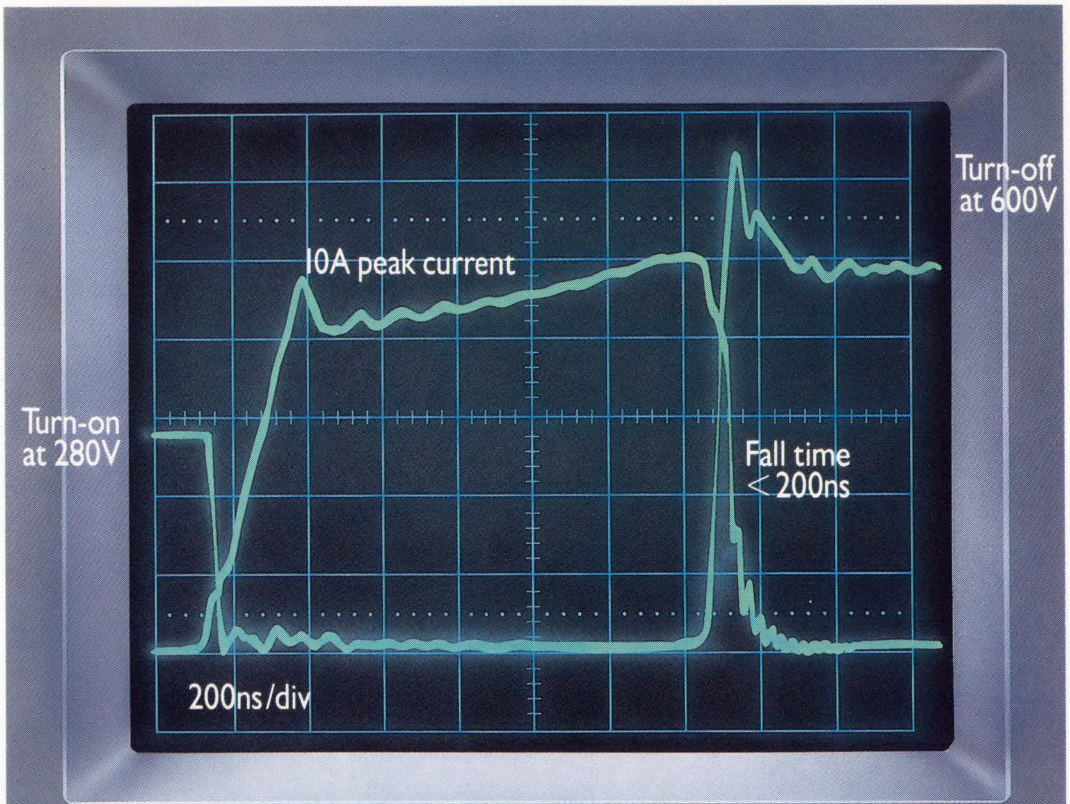

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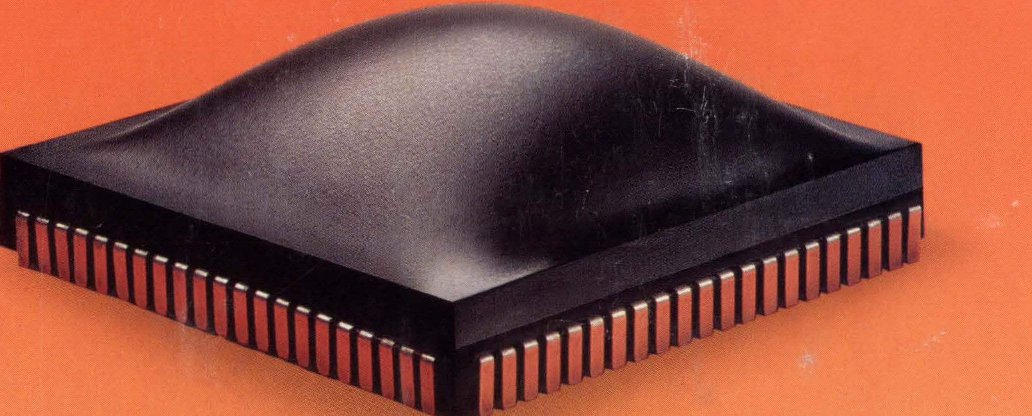

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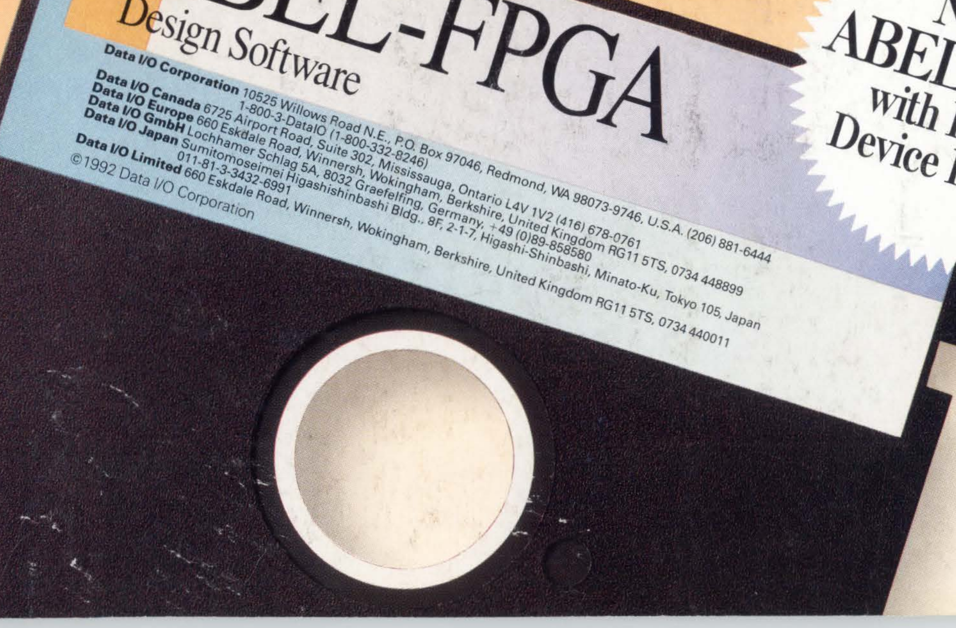

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