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PROCESSOR UPDATES
PG 81

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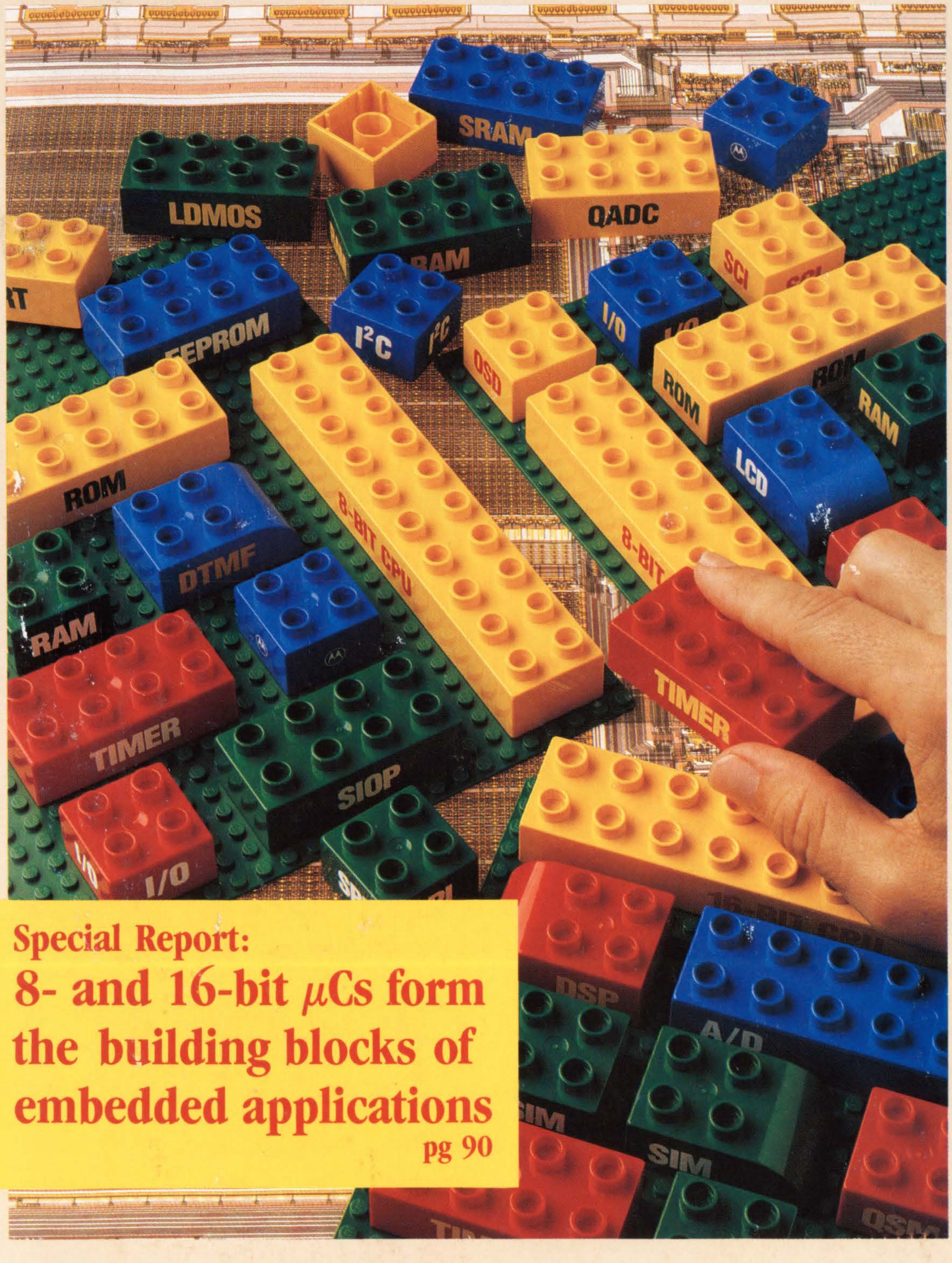
June 18, 1992



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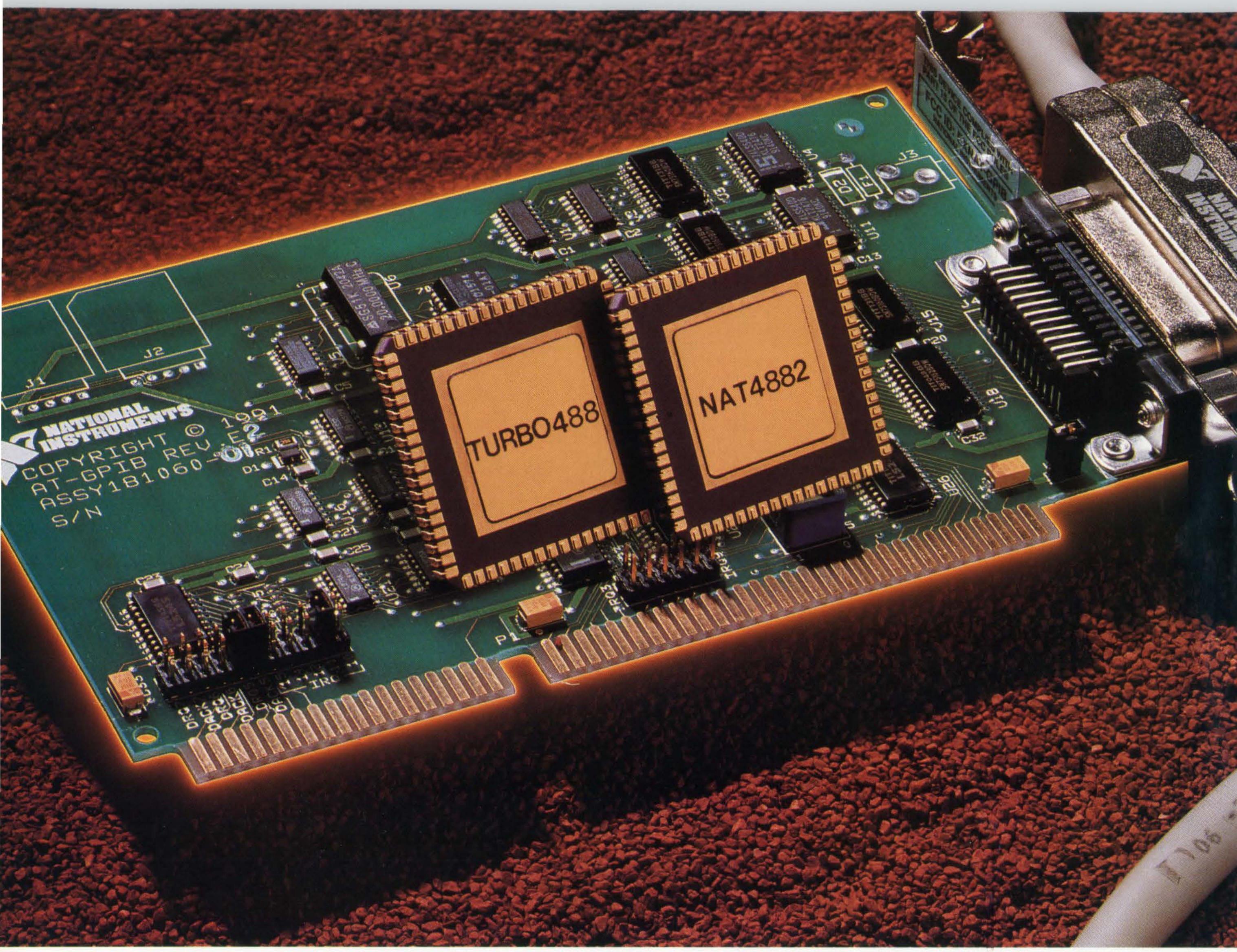

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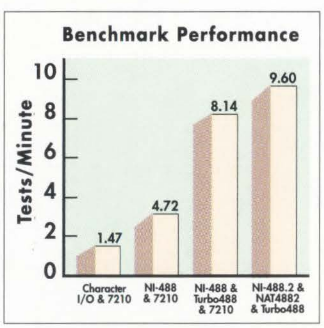

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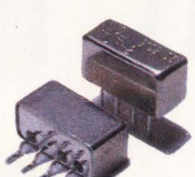

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CIRCLE NO. 4

F 145 REV.

EDN
MAGAZINE EDITION

JUNE 18, 1992 VOLUME 37, NUMBER 13

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

On the cover: Today's 8- and 16-bit microcontrollers can be as unadorned or sophisticated as need be. Pick and choose the peripherals you want to satisfy any low- or high-end application. (Photo courtesy Motorola Inc; concept by Staats Falkenberg & Partners Inc; photography by Tomás Pantin) . . . . . . **PAGE 90**

SPECIAL REPORT

The world of 8- and 16-bit microcontrollers

90

From meager beginnings, microcontrollers have evolved into a wide range of diverse processors. You can find a μC with the right speed, peripheral mix, power, and price for almost any embedded application you'd care to tackle.—*Ray Weiss, Technical Editor*

DESIGN FEATURES

Fuzzy-logic basics: intuitive rules replace complex math

111

Although "fuzzy logic" may seem to imply imprecision, it's based on a reliable and rigorous discipline.—*David I Brubaker, The Huntington Group*

Fuzzy-logic system solves control problem

121

Complex, nonlinear control problems can yield to simple fuzzy-logic techniques that require no modeling.—*David I Brubaker, The Huntington Group, and Cedric Sheerer, C/S Associates*

TECHNOLOGY UPDATES

DSP for motion control: Analog movements go digital with DSP

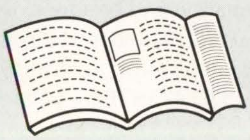
51

The cost of DSP ICs has plunged to half of the 1989 selling prices. As a result, design engineers are now using these chips for improved stability and precision in robotic and motor applications by avoiding the component drift and aging problems inherent in analog control circuits.—*J D Mosley, Technical Editor*

Continued on page 7

Foldout contents

Turn to the last information-retrieval service card in the back of this magazine and you'll find a foldout table of contents. Now, instead of flipping back and forth from this table of contents to the articles you want to read, you can have the convenient foldout open at all times while you're reading EDN. Use the foldout contents to mark off articles you'd like your colleagues to read or to remind yourself to copy stories for your files.



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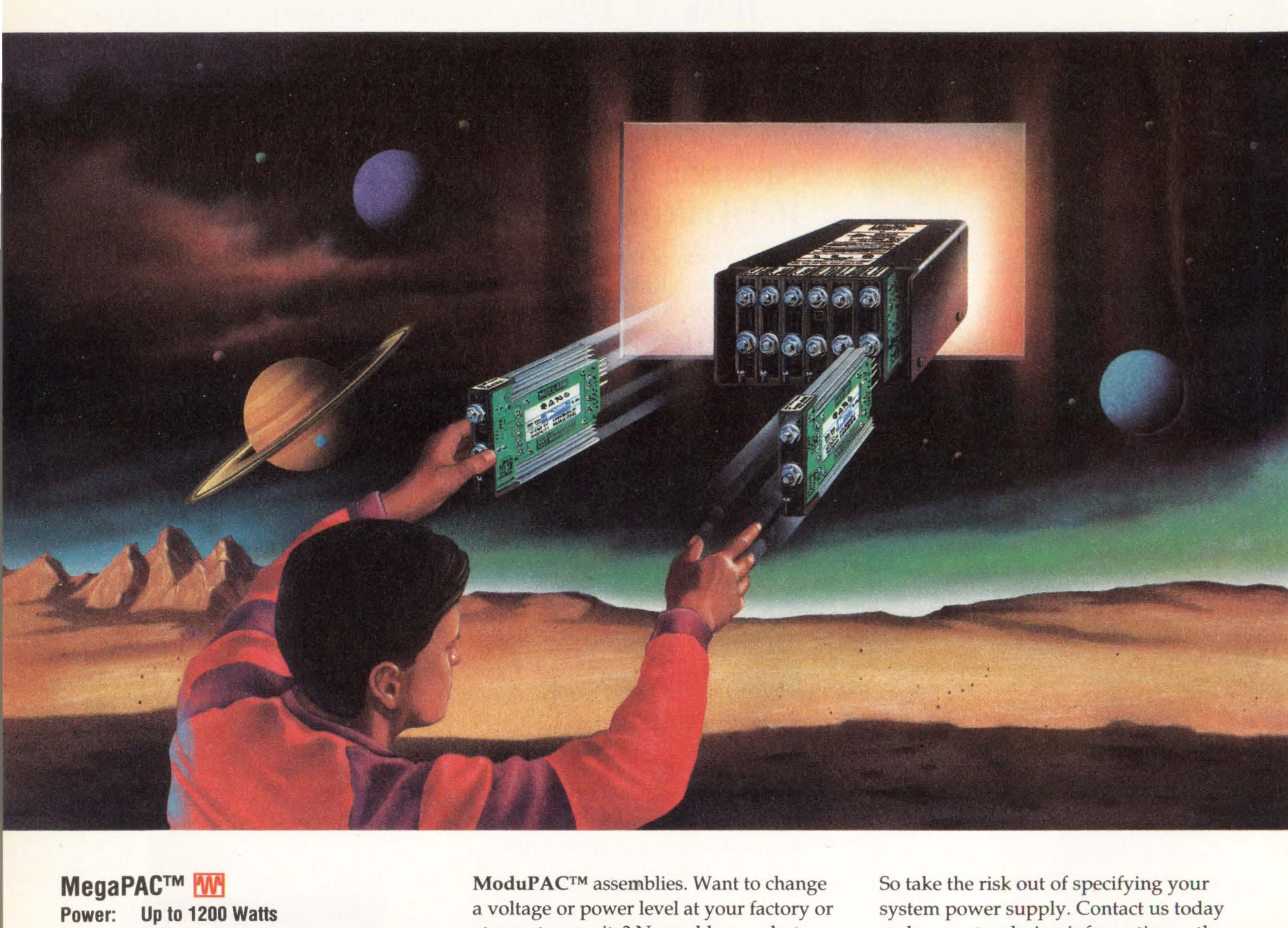

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Component Solutions For Your Power System

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JUNE 18, 1992

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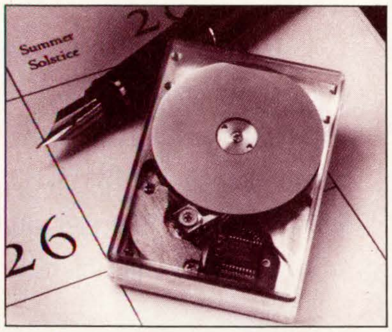

EDN's editors have selected Hewlett-Packard's Kittyhawk disk drive as this issue's Editors' Choice. The device, which holds 21.4 Mbytes, uses 1.3-in.-diameter media and weighs less than an ounce. Read more about it on . . . . . **PAGE 77**

TECHNOLOGY UPDATES

Video amplifiers set sights beyond large 3-dB bandwidths **61**

You can buy video amplifiers and subcircuits that have low, stable gains and low distortion for $3 to $10.—*Anne Watson Swager, Technical Editor*

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Software tool for analog models 78

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MAGAZINE EDITION

JUNE 18, 1992

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EDITORIAL

Don't confine innovation to the R&D lab

Companies can't expect to prosper—or even necessarily survive—if they confine their innovation to the R&D lab.—*Dan Strassberg, Technical Editor* **47**

PROFESSIONAL ISSUES

The enduring appeal of consulting

Independent consulting has its drawbacks, but for some engineers it's the only way of life.—*Jay Fraser, Associate Editor* **205**

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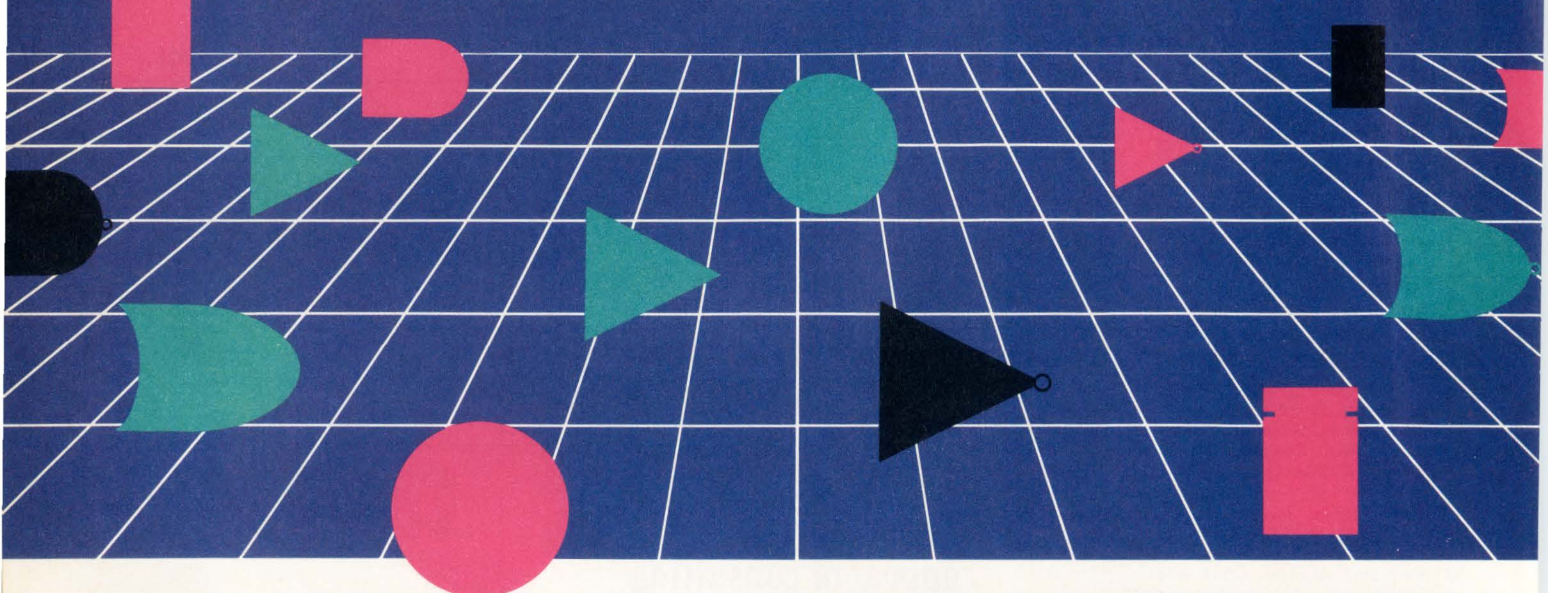

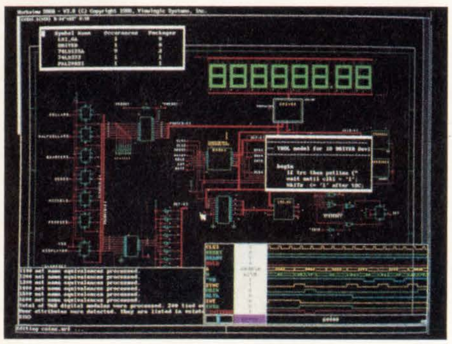

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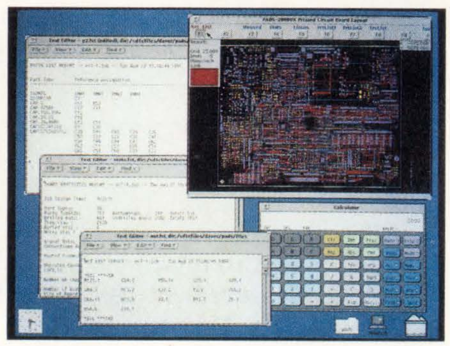

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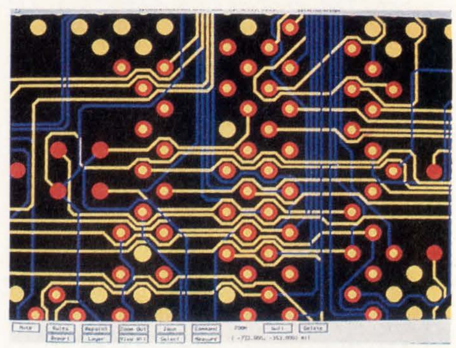

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CIRCLE NO. 9

INSIDE EDN

A summary and analysis of articles in this issue

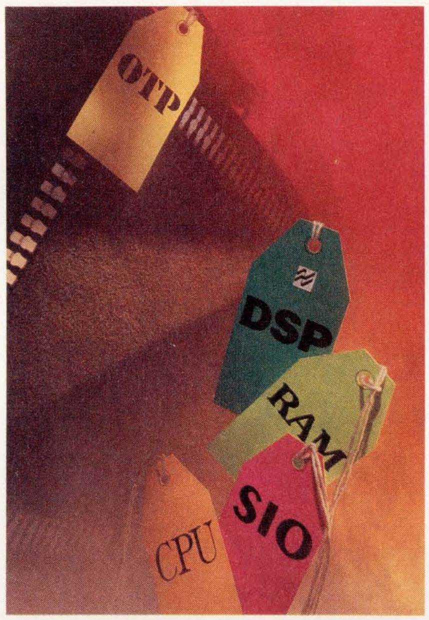
What's in a name? Well, if the word "fuzzy"is a part of that name—as in **fuzzy logic**—perhaps engineers won't take the concept very seriously. That's what some people believe is one factor that has kept fuzzy logic from really taking off in the US since it was first proposed in 1965 by Lotfi Zadeh, a professor of electrical engineering at UC Berkeley.

Another reason is the dearth of good material that explains in direct terms the concepts behind fuzzy logic, which is a computationally simple way to handle complex, nonlinear control problems. Determined to get past this stumbling block, Senior Technical Editors Charles Small and Gary Legg went on a mission to find an expert that could write the way engineers think. After a long search, they found David Brubaker, author and coauthor of the articles on fuzzy logic included in this edition of EDN.

In this issue and in the next, we're devoting a considerable number of pages to analyze and explain the concepts and enormous implications behind fuzzy logic. According to Legg and Small, who handled the editing of Brubaker's articles, **Fuzzy logic basics** is a tutorial that gives you a solid foundation in the fundamentals. **Fuzzy logic solves control problem without complex math** provides practical steps on how to design a simple fuzzy-logic system. And in the next issue of EDN, look for the third part of our special coverage—Legg's article on the software tools that can help you at each step of a fuzzy-logic design.

For this issue's Special Report, Technical Editor Ray Weiss takes an extensive look at forces that have shaped the evolution of **8- and 16-bit microcontrollers**. He came to the conclusion that you'll have no problem finding a device that gives the proper combination of processing power, peripherals, and price. Soon to come will be smarter peripherals and lots more on-chip memory.

Using "video" as an adjective tells a designer that a part operates up to a certain frequency. But the **video op amps and subcircuits** that Technical Editor Anne Swager discusses in her article don't rely on just their bandwidths to satisfy the "video" label. She covers the auxiliary specifications that make the devices tailored to state-of-the-art video applications.



This issue's Special Report covers the evolution of 8- and 16-bit microcontrollers.

In three years, the typical price of a DSP IC has been cut in half. As these chips have become more affordable, designers have been finding some pretty innovative ways to use them. One such method supplants traditional analog circuits for motion control with 16-bit DSP devices. Technical Editor J D Mosley investigates **DSP for motion control**—just don't be lulled into thinking it's a complete panacea.

Joan Morrow Lynch
Managing Editor

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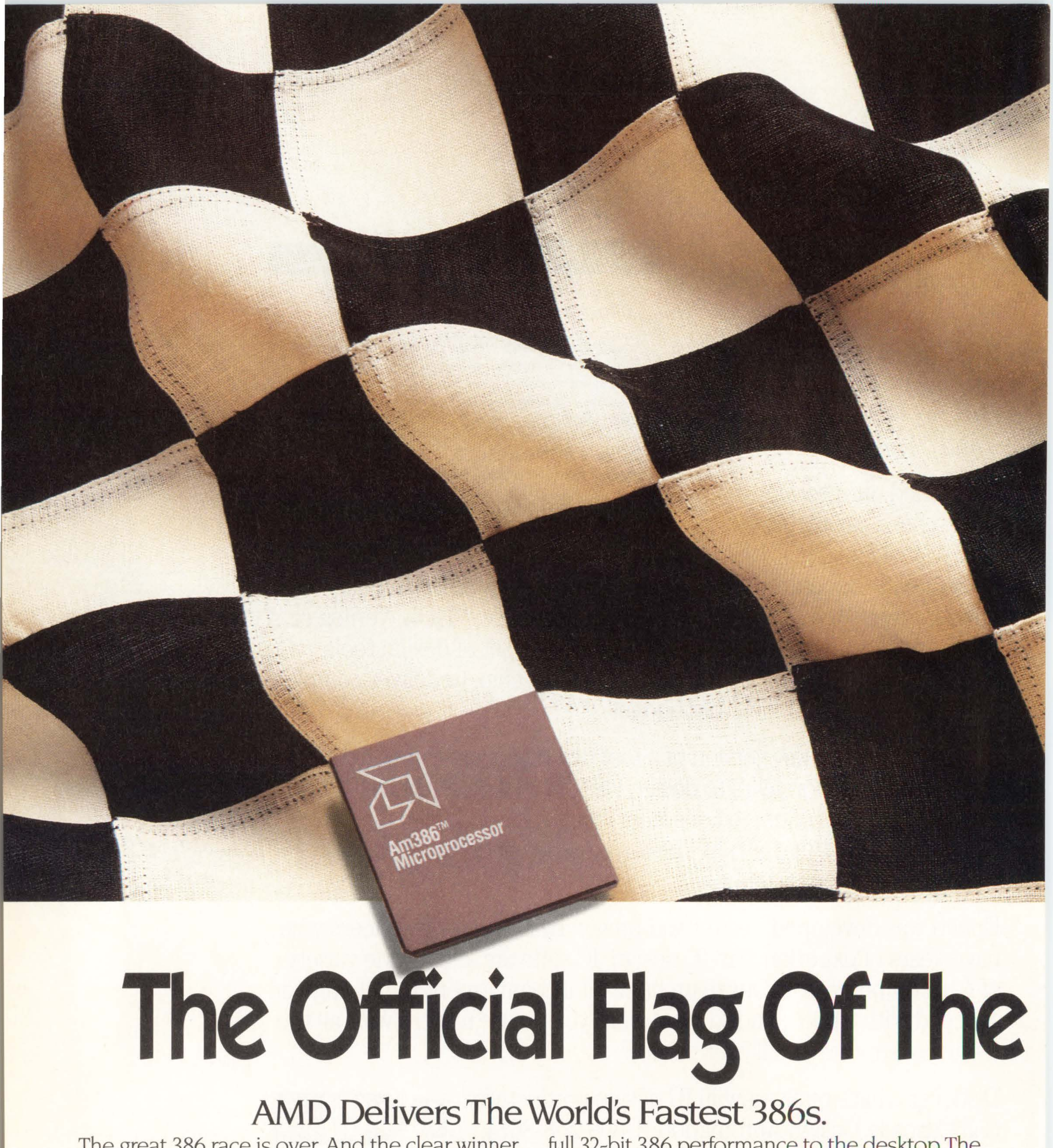

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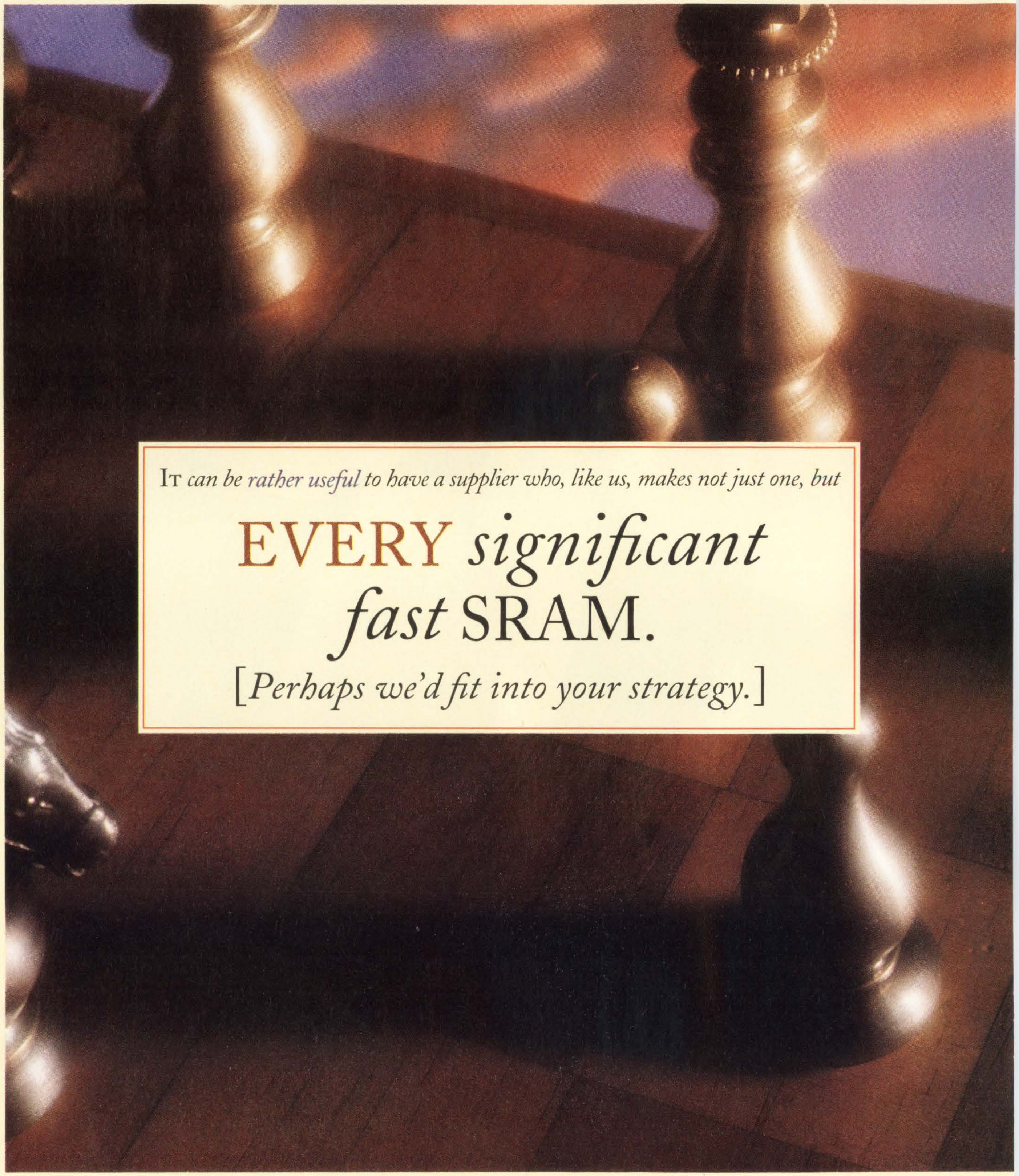

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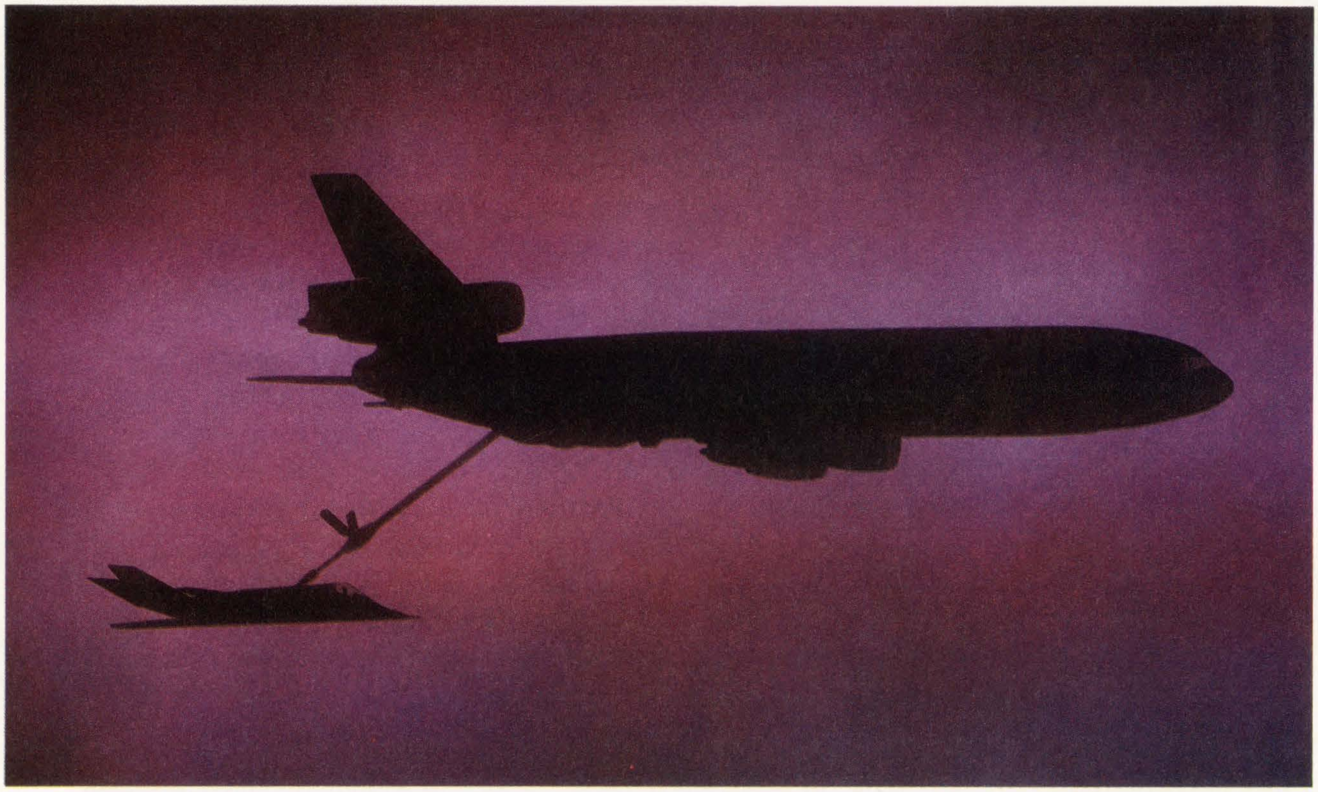

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CIRCLE NO. 22

EDITED BY SUSAN ROSE

Kit teaches fuzzy-logic design

Now through August, you can order a $195 fuzzy-logic educational kit that explains how to implement fuzzy-logic functions on Motorola's standard microcontrollers. The FLEDKT00 kit will cost $295 on September 1. The kit is more than just a demo version of the company's announced Fuzzy Inference Development Environment (Fide); it contains three basic items: a computer-based educational course that teaches users how to apply fuzzy logic to their applications by guiding them step by step through a typical fuzzy-logic design cycle; an introductory version of Fide, which helps users determine the correct membership functions and rules for their application and generates microcontroller code for the HC05 and HC11 microcontroller families; and free fuzzy-logic-related software and associated documentation.

For a limited time, you can also order an M68HC05EVM and M68HC1EVM board-level in-circuit emulator along with the kit for $600 (part numbers are FLEDKT05 and FLEDKT11, respectively). The kit requires a minimum of a PC/AT-class or -compatible computer with one 5¼- or 3½-in. floppy, a 40-Mbyte hard drive, and a VGA monitor. DOS 3.30 with Windows 3.0 is required, but DOS 5.0 is recommended. Motorola Inc, Austin, TX, (512) 891-2840, contact Jack Davis.—Anne Watson Swager

RISC μP available as ASIC core processor

If your latest embedded design requires the performance of a 32-bit μP, but lacks the budget or power supply for the "big-name" processors, you should consider the ARM6 (advanced RISC machine) processor core now available from GEC Plessy Semiconductors. The processor executes 15 MIPS at 20 MHz and requires less than 250 mW at that speed. The core architecture includes features you'd expect a 32-bit processor to have, such as a memory-management unit and a 4-kbyte, 64-way, set-associative cache memory. NRE charges for ASICs incorporating this processor core start at $60,000, and parts cost approximately $45 (1000). Software development tools include C, Fortran 77, and Pascal compilers; an assembler; and an emulator. GEC Plessy Semiconductors, Scotts Valley, CA, (408) 438-2900, FAX (408) 438-5576, contact Stephen Tang-Kong.—Steven H Leibson

Controller pumps data at 24 Mbytes/sec

Higher disk capacities require faster disk-to-controller data-transfer rates. Simulex Corp's IPI-2 disk controller, the SC1615, can pump data at rates as high as 24 Mbytes/sec with built-in error-correction code (ECC). The chip integrates the company's SC1610 disk controller chip and SX1620 ECC chip. It has a 36-bit DMA data bus (64-Mbyte address space), as well as a separate processor interface.

To speed system performance, the chip provides a 32-bit DMA channel to the host. The DMA channel moves data at rates as fast as 50 Mbytes/sec and handles multiple command, response, or data buffers. A 16-word FIFO buffer delivers DMA bursts of 1, 2, 4, 8, or 16 words. To offload the CPU, the chip executes all IPI-2 disk sequences without the need for CPU intervention. Available July 20, the chip comes in a 208-pin quad flatpack and sells for $72 (1000). Simulex Corp, Tustin, CA, (714) 730-1300, FAX (714) 730-7176.—Ray Weiss

Generate ASIC cell libraries quickly

GenRad's Master Toolbox suite of utilities guarantees that target cell libraries simulate in the target environment exactly as the source cells simulate in the source environment. The company claims the software lets users create rapid high-accuracy cell libraries for a range of simulators in weeks, instead of months. Source and target design environments include VHDL (VHSIC Hardware Description Language), Spice, GenRad's System HILO 4, LSI Logic's Modular Design Environment, Mentor's QuickSIM II, and Cadence's Verilog-XL. You can use other environments by adding a procedural interface. Depending on the configuration, prices range from $100,000 to $250,000. GenRad Inc, Milpitas, CA, (408) 432-1000.

—Doug Conner

Foundry-independent floorplanner speeds IC design

Using Preview, a floorplanner from Cadence, you can control the physical layout of an IC by providing data that specifies the rough topology, timing, size, and power requirements that will be used during physical layout. The software is automated, and the company claims you can use it effectively even if you have little or no physical design experience. You input a set of design constraints, and the software analyzes it to create a floorplan automatically. You can modify the floorplan to optimize it further.

Without a floorplanner, you typically work with statistical prelayout delays that use little, if any, information about how your design will be placed on the IC. Even if the logical design is perfect, a complex IC design running at 50 MHz or

Text continued on pg 22

Text continued from pg 21

faster may fail timing simulation when you get the accurate timing data for the physical layout back from the foundry. A floorplanner can reduce or eliminate the need for additional iterations of IC layout to get the performance you need out of your design.

The software will be available in the third quarter of 1992 on the Sun-4 workstation for $25,000 per network license. It will be available on Digital, IBM, and HP workstations in the fourth quarter. Cadence Design Systems, San Jose, CA, (408) 943-1234, FAX (408) 943-0513.

—Doug Conner

EPROMs adapt to application needs

The humble EPROM has joined the ranks of general-purpose memory devices that are adapting to specific applications. The conflicting needs of high-speed processors, power-limited systems, and low-voltage operation has prompted National Semiconductor to introduce three special-feature EPROM product families.

The processor-oriented EPROM family, NM27Pxxx, addresses the timing constraints posed by 80x86 and 680x0 processors. To meet processor hold times, the devices retain valid output data for 5 to 30 nsec following deselection, compared with the 0 to 60 nsec of valid data from conventional EPROMs. The low-current family, NM27LCxxx, draws less than 10 mA when operating, 100 μA in standby. The low-voltage family, NM27LVxxx, offers operation at 3V.

The processor-oriented family comes in densities from 512 kbits to 4 Mbits with access speeds from 90 to 200 nsec. Prices start at $4 (1000). The low-current family is available in 64-, 256-, and 512-kbit sizes with 8-bit-wide interfaces. Prices range from $2.49 to $4.84 (1000). The low-voltage family currently has only one member, a 1-Mbit device. It costs $6.15 (1000) in a 32-pin plastic leaded chip carrier and $7.05 for thin small-outline packages. The low-voltage version is not presently available in a windowed package. National Semiconductor, Santa Clara, CA, (408) 721-5000.

—Richard A Quinnell

Mips-based RISC CPU board prototypes X-Terminal

X-Terminals require heavyweight graphics and local processing. LSI Logic's prototype X-Terminal board, the RacerX, is built around the company's 25-MHz Mips-based RISC CPU, the LR33020 GraphX. The board is a complete X-Terminal with screen resolutions to 1280×1024 pixels, monochrome or 8-bit color, and video refresh rates as high as 75 Hz. The 7×9.25-in. board has 4 Mbytes of dynamic RAM (DRAM) that's expandable to 8 Mbytes, optional video RAM (VRAM) (1 Mbyte, which is expandable to 2 Mbytes), a PS/2 keyboard port, a mouse port, two serial RS-232C ports, and thick or thin Ethernet.

The board's processor is supplemented by an on-chip graphics processor, video controller (with DMA), static RAM, VRAM, and DRAM memory controllers. The graphics coprocessor offloads the CPU with its bitblt processor and DMA channel. The on-chip memory and video controllers minimize board glue logic. Each evaluation board costs $2950 (monochrome display) or $3950 (color display). The boards will be available in July. You can buy Age Logic's Xoftware M300L X-Server software with the board ($25,000 for a binary OEM license). A full set of software is also available for the CPU, including real-time operating systems, a PROM monitor, graphics libraries, and networking programs. LSI Logic Corp, Milpitas, CA, (408) 433-8000.—Ray Weiss

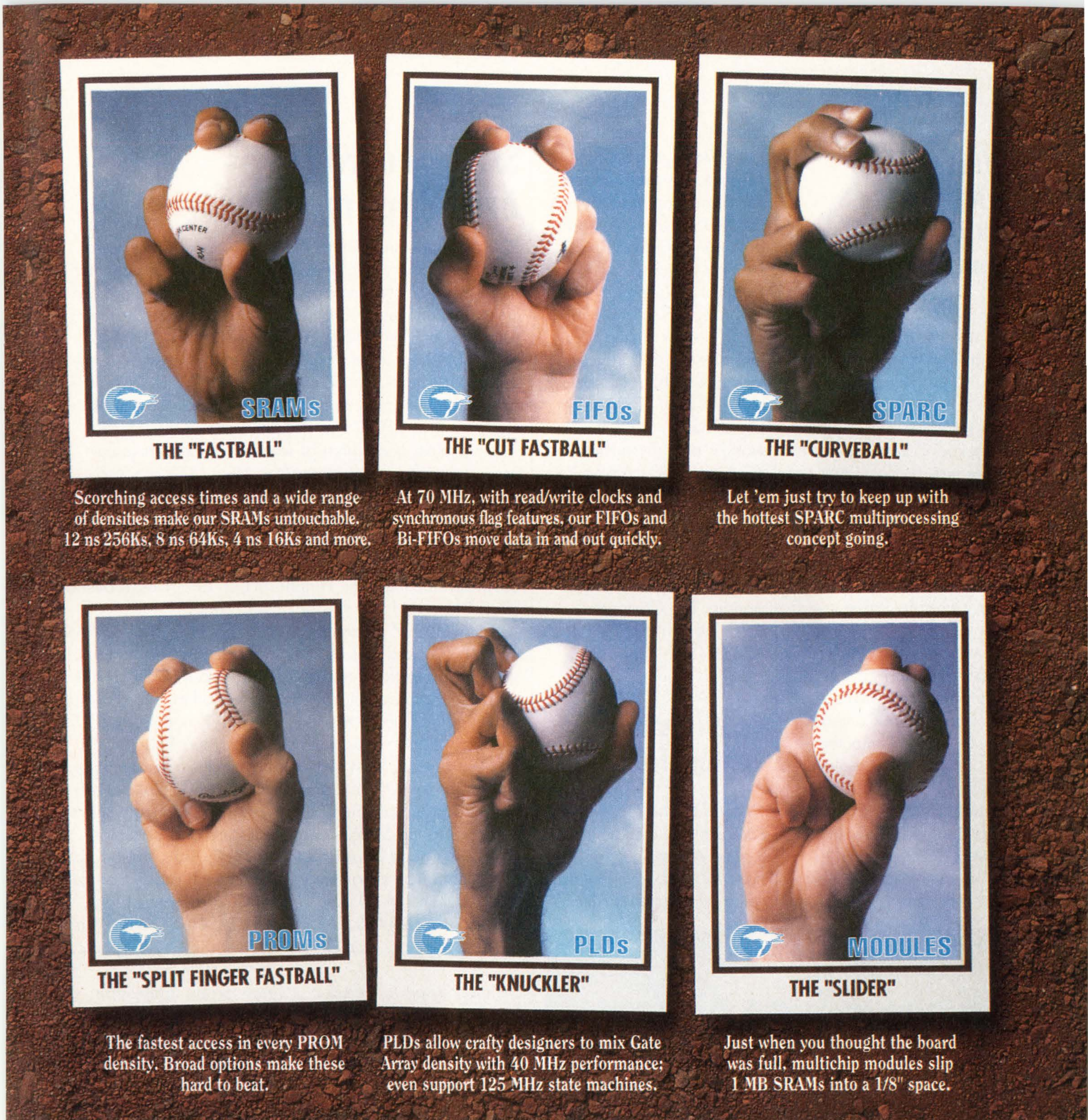
Hardware modeler simulates complex devices

A 640-pin device adapter and the release of version 2.0 of its software lets Logic Modeling do a better job simulating complex devices. The software features automatic timing-error detection and improved handling of unknown conditions. In addition, simulations run faster because the software evaluates the hardware model simultaneously with the software model instead of serially, as it did in the past. The device adapter costs $9700, and the software upgrade is $10,800 for users not covered by maintenance agreements. Logic Modeling, Milpitas, CA, (408) 957-5200.

—Doug Conner

MPEG ICs target consumer products

Two new MPEG (Moving Picture Experts Group) ICs target cost-sensitive applications in consumer electronics. C-Cube Microsystems and SGS-Thomson have announced chips that will perform real-time decoding of MPEG video for a hardware price of $30 to $50. Both ICs suit CD video and other full-motion video applications. C-Cube's CL450, which will cost $50 in production qty, is available now in sample qty for $250. SGS-Thomson is projecting a $20 large-quantity price for its STI3240, but the chip requires an external DCT (discrete cosine transform) chip, which will increase the overall decoding cost. Samples of the STI3240 will be available in September; SGS-Thomson has not announced a small-quantity price. C-Cube Microsystems, Milpitas, CA, (408) 944-6370. SGS-Thomson, Grenoble, France, (33) 7658-5184 and Phoenix, AZ, (602) 867-6100.—Gary Legg



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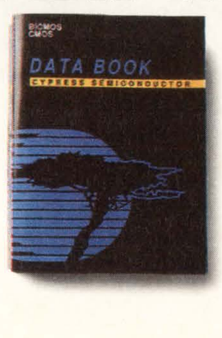

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West Coast wins the Fourth Annual Computer Bowl

The West Coast wrested the title "Computer Masters of the Universe" from their East Coast Rivals in the Fourth Annual Computer Bowl, May 1, 1992, at Boston's Park Plaza Castle. The score was 320 to 240. The East and West are now tied at two wins each in this bicoastal contest of computer knowledge and trivia that has become computerdom's own celebrity classic event. The Computer Bowl Trophy will now travel to the West Coast until April of 1993, when the West will co-host the Fifth Annual Computer Bowl with The Computer Museum. This tie-breaker will be the final contest leading to the Championship Computer Bowl in 1994.

The event was created and produced by The Computer Museum in Boston and presented by the Association for Computing Machinery; it benefits the Museum's educational programs. The Computer Bowl, similar in format to TV game shows, has raised $2.2 million in cash, products, and services since 1988. Educating the public about computers is the mission of The Computer Museum. It is the world's only museum exclusively devoted to computers and their impact on society. The Association for Computing Machinery is one of the world's leading associations of computing professionals. The Computer Bowl, Boston, MA, (617) 426-2800.—Susan Rose

With a score of 320, the West Coast won the Fourth Annual Computer Bowl. The winners are, from left to right, Vern L Raburn (Slate Corp), Jeffrey C Kalb (MasPar Computer Corp), Team Captain John F Shock (Asset Management Corp), Ruthann Quindlen (Alexander Brown & Sons), and Dr John E Warnock (Adobe Systems Inc).

CASS-tester venture formed

General Electric Co, Hewlett-Packard, and Teradyne have formed Automated Test International (ATI), which will develop and market a commercial counterpart to the US Navy's CASS (Consolidated Automated Support System) standard test system. The venture is organized as a limited partnership, HP and Teradyne being the limited partners and GE the managing general partner. ATI, Daytona Beach, FL, (904) 226-2295.—Susan Rose

SPARC board set uses MBus modules

SPARCstations are shifting to module-based designs for fast upgradability, high-performance, low-cost implementations. Nimbus Technology's NIM600 SPARC Board Set includes a chip set and pc board that makes up the mother board for a SPARC clone. The clone can take the new SPARC MBus modules from Sun Microcomputer Systems, Texas Instruments, and Cypress Semiconductor. With the board set, vendors can turn out an MBus-based SPARCstation with a minimum of design.

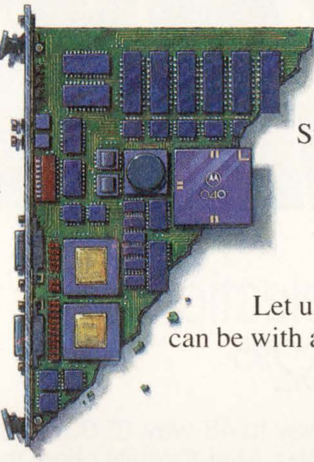
Sun's latest generation of workstation/servers is built around the 64-bit, 40-Mbyte/sec MBus. The processors are on MBus modules with a standard 120-pin pinout, which you can swap out to upgrade the system. Nimbus provides the same capabilities to SPARC clone vendors. The SPARC Board Set consists of seven chips—each a controller: the Interrupt, Peripheral I/O, Graphics, MBus-to-SBus, DMA, and two memory controllers.

The NIM6027 graphics controller chip has a video RAM frame buffer and runs directly on MBus, rather than SBus, speeding data transfers between the host SPARC and the graphics processor. Nimbus has a full mother-board design that is built around one MBus processor module, two 25-MHz SBus slots, and as much as 96 Mbytes of 60- to 80-nsec dynamic RAM SIMMs (single in-line memory modules), SCSI, and Ethernet and ISDN. The board set is compatible with Sunsoft, SunOS, and Solaris operating systems and fits into the SPARCstation enclosure and backplate. The chip set and board cost $350 (10,000). The board is available now in sample quantities, with production volumes available in 30 days. Nimbus Corp, Santa Clara, CA, (408) 727-5445, FAX (408) 727-5447.—Ray Weiss

Disk plant expands

KAO Infosystems is expanding its facility in Plymouth, MA, making it one of the three largest floppy-disk manufacturers in the world. The automated facility will perform the coating and manufacturing functions in the production of 3½- and 5¼-in. floppy disks. The facility will produce standard, high-density, and extra-density disks. The company will be able to produce 26 million disks per month in North America and nearly 36 million disks per month worldwide. KAO Infosystems, Plymouth, MA, (508) 747-5520, FAX (508) 747-5521.—Susan Rose

Why Settle for ½ an '040 Board?



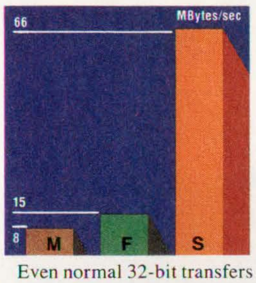
You've chosen the '040 because you need maximum performance in your VME system. But look carefully, because other Single Board Computers may only give you only half of what you expected from the '040.

Compare Synergy's SV430 performance to any other SBC. Compare bus speed, MIPs, support, flexibility, documentation, reliability, I/O intelligence or any spec you can think of. We think you'll find the same thing we did—the SV430 outperforms every other SBC on the market by as much as 150%.

Surprisingly, this kind of quality won't cost you any extra, because Synergy products lead in another important area—value. At Synergy, you don't have to pay a premium price for premium performance.

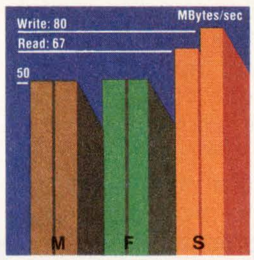
Let us show you just how far ahead your system can be with a Synergy processor board. Call us today, and get the *whole* '040 story.

Compare our specs. Synergy is superior across the board!



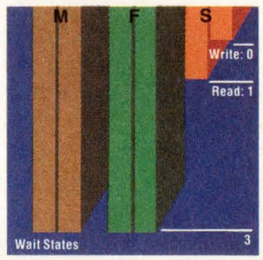
VME Transfers

VME64 doubles bus performance to 66 MB/s—and the SV430 is the only '040 board that has it. But we don't need VME64 to win this comparison. Even normal 32-bit transfers race at 33 MB/s. That's 200% faster than Force or Motorola.



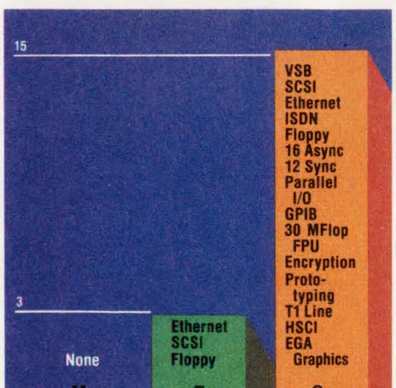
DRAM Burst Rates

A 25 MHz '040 is capable of accessing memory at 80 MB/s. The closer you are to this maximum, the more '040 performance you're gaining. SV430 bursts are 26% faster than Force and Motorola.



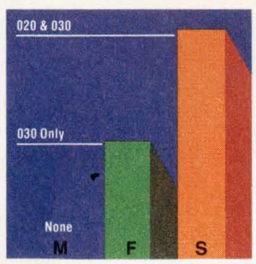
DRAM Random Accesses

Non-burst '040 performance is measured in wait states. Fewer wait states mean higher performance. The SV430 is not only 66% faster than Force or Motorola, it supports twice the on-board memory—32 MB.



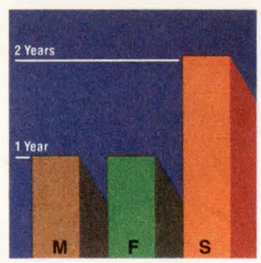
I/O Modules

Synergy's EZ-Bus modules are compatible with our entire line of SBCs. This means Synergy's current line of 12 intelligent I/O modules are immediately available for the SV430—today. No other vendor comes close for selection, functionality or availability.



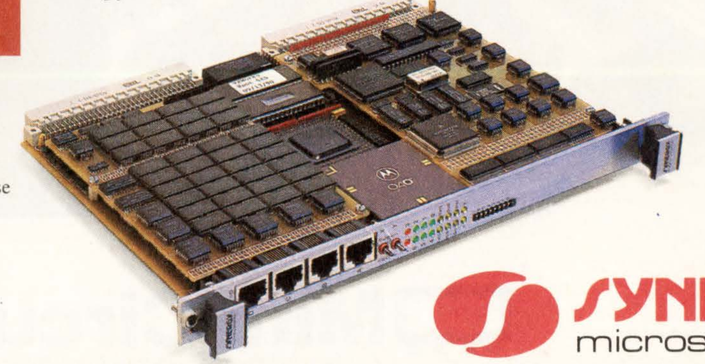
'020/'030 Compatibility

Software compatibility between Synergy SBCs means users have simple upgrades to the SV430 from our '020 and '030 SBCs. Force offers compatibility only from the '030 level, and Motorola offers "upward migration"—a polite phrase that means rewriting your code.



Product Warranty

Synergy backs the reliability of its SBCs with a two year standard warranty. Force and Motorola only offer you one.



Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. 1. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

VME64 is a trademark of Performance Technologies, Inc.

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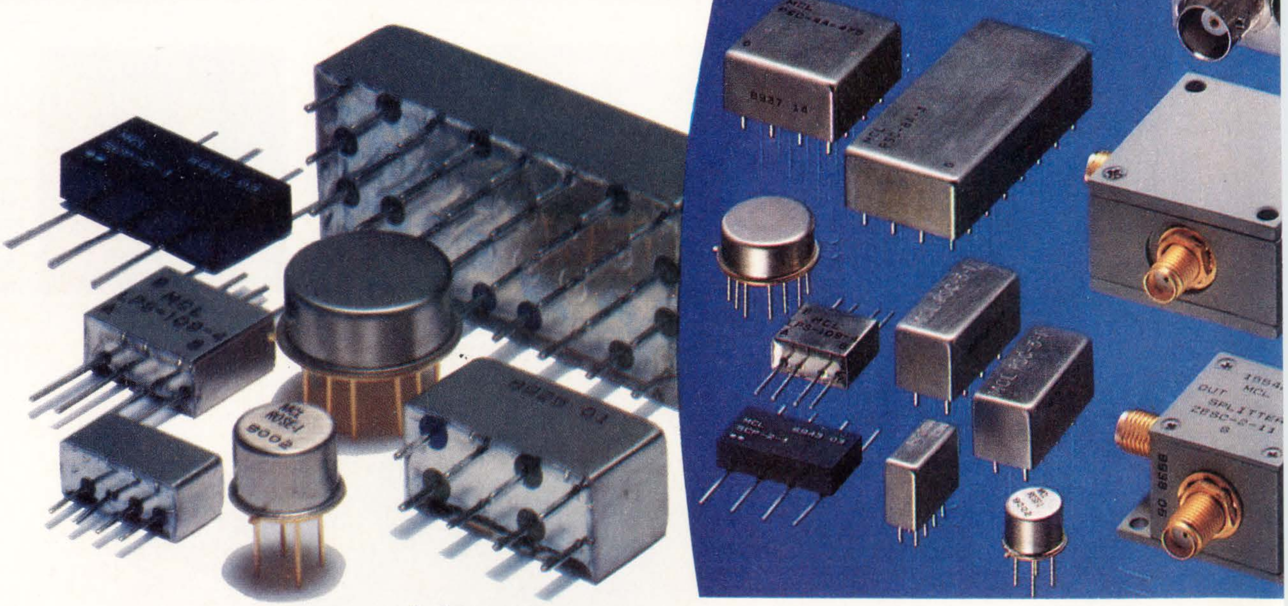

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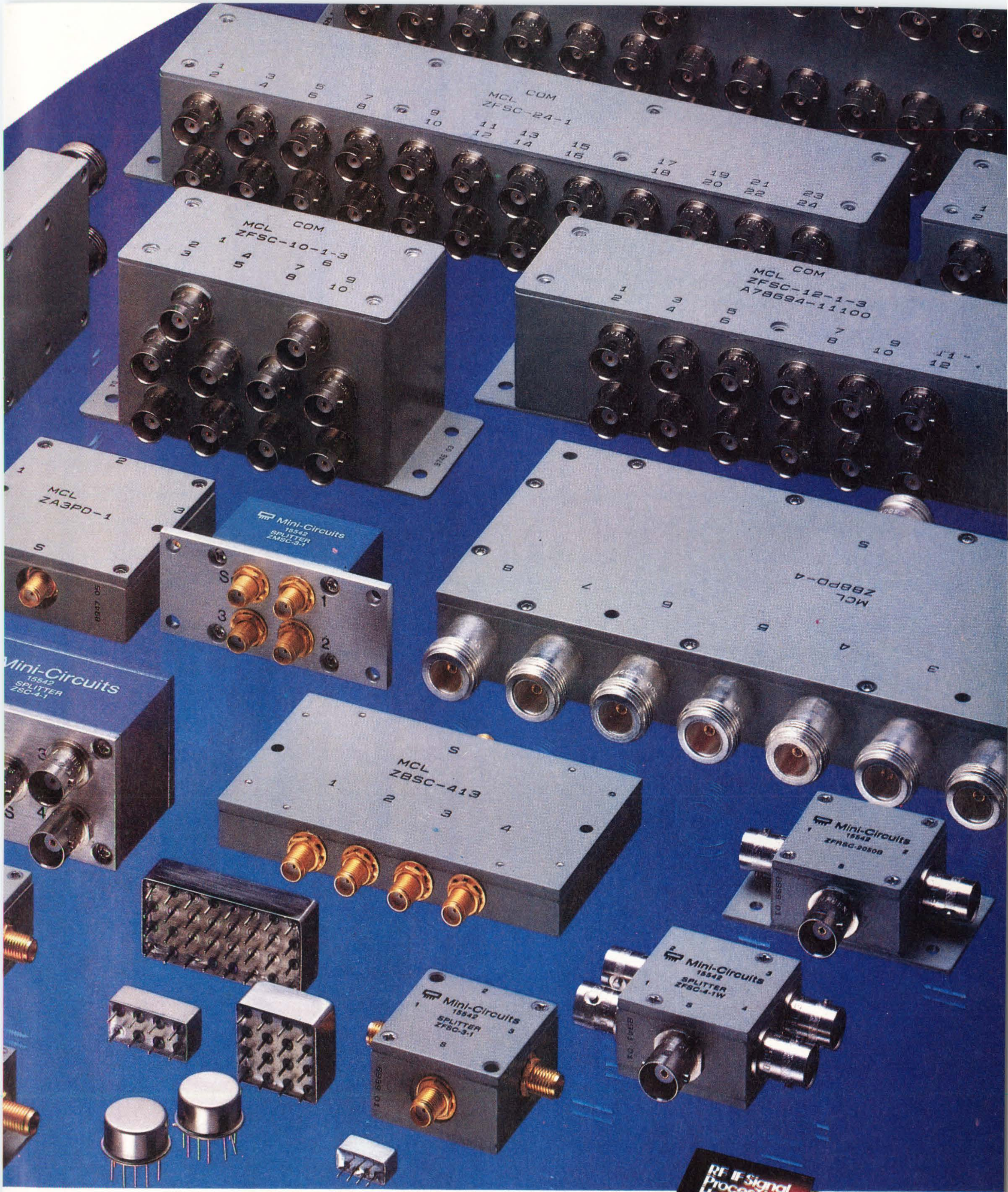
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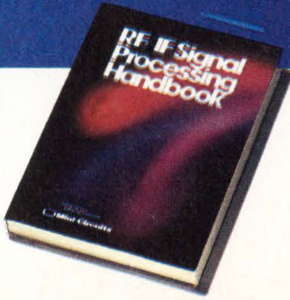
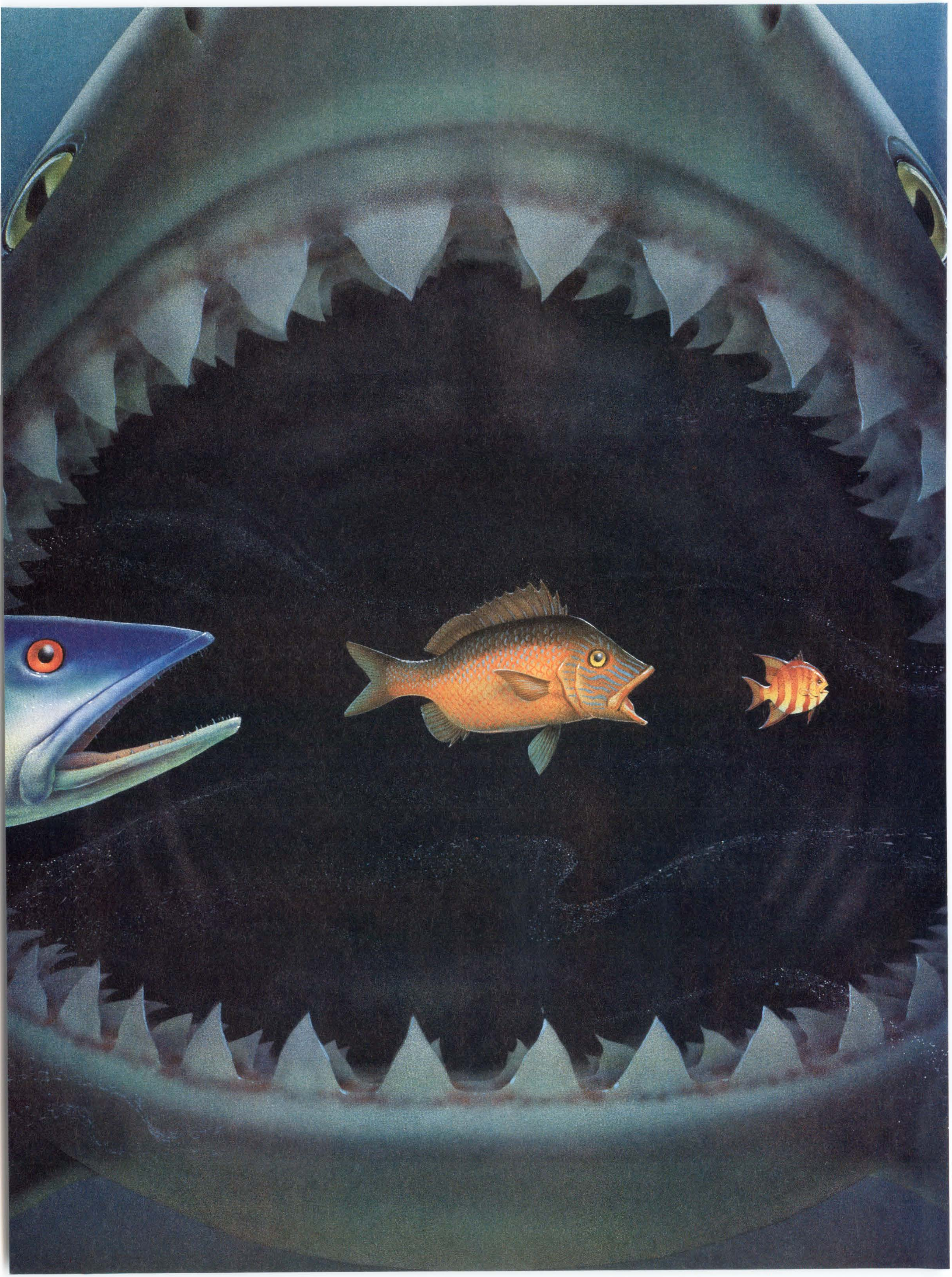

RF IF Signal Processing Handbook



10ns BiCMOS 1 Megs from Motorola. Everything else is dead in the water.

1 Meg BiCMOS Fast SRAMs from Motorola demonstrate a simple evolutionary principle: survival of the fastest.

With 10ns access times at 1 Meg densities, nothing else even comes close enough to compare – for speed *and* density.

MCM6726	MCM6728	MCM6729■	MCM67282▲	MCM6727
128K x 8 bit	256K x 4 bit	256K x 4 bit	256K x 4 bit	1 meg x 1 bit
10●, 12, 15ns	10, 12, 15ns	10, 12, 15ns	10, 12, 15ns	10, 12, 15ns
MCM6706A	**MCM6705A**	**MCM6708A**	**MCM6709A■**	**MCM67082A▲**
32K x 8 bit	32K x 9 bit	64K x 4 bit	64K x 4 bit	64K x 4 bit
8, 10, 12ns	10, 12ns	8, 10, 12ns	8, 10, 12ns	10, 12ns

● 3Q92 ■ Output Enable ▲ Separate I/O

And as if that weren't enough to scare off the competition, these 1 Meg Fast SRAMs support both TTL and ECL I/O. They also feature an advanced pinout, with power supply, ground, and I/O pins centered on the package for reduced inductance and improved ground and power bussing.

Looking for even more speed? How about 8ns? That's the access time on our 256K BiCMOS Fast SRAMs.

Choose whichever speed-and-density combination is right for you. Either way you'll get the built-in quality and reliability of Motorola's high volume, sub-micron manufacturing.

Reel in the power of our BiCMOS Fast SRAMs for your next design, and get ready to throw everything else back in the water.

To request technical information or a sample device, just mail in the coupon or FAX it to Motorola's Fast SRAM FAX line at **1-800-347-MOTO (6686)**.

Let's make some waves, Motorola. EDN 6/18/92
Send me more on BiCMOS Fast SRAMs today.
Motorola, Inc. Fast SRAM Operations, P.O. Box 1466, Austin, Texas 78767

Name ______ Title ______
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Application ______
Production Start Date ______ Estimated Usage: 1992 ______ 1993 ______

SRAM:

1 Meg TTL I/O		1 Meg ECL I/O		256K TTL I/O		
☐ 1 meg x 1	☐ 10ns	☐ 1 meg x 1	☐ 10ns	☐ 64K x 4	☐ 8ns	
☐ 256K x 4	☐ 12ns	☐ 256K x 4	☐ 12ns	☐ 32K x 8	☐ 10ns	*10 &
☐ 128K x 8	☐ 15ns		☐ 15ns	☐ 32K x 9*	☐ 12ns	12ns Only

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Motorola offers a complete portfolio of BiCMOS and CMOS Fast SRAMs with densities from 16K to 1 meg, plus 2 and 8 meg modules. CMOS access times are as fast as 15ns (256K) and 20ns (1 meg).

Small companies can get help for PID design

Timothy Rusco writes (EDN, March 16, 1992, pg 27) concerning the difficulty engineers at small companies face in getting started with PIDs (proportional-integral-derivative) devices. Let me offer a suggestion: Make use of distributors' design centers to do your first design.

Many distributors have the PID manufacturers' development systems and are willing to let prospective customers use them. (Be sure to buy at least the prototype parts from the distributor you use.) Once you've got a PID designed into a product, it's really easy to get a few thousand dollars freed up to buy your own development system.

I've been down this path myself and thought it worked fairly well. Of course, the snare is that your development system limits you to one family of PIDs, so look for the PID family that best serves your company's family of products.

Jim Honea
Electronic Design Engineer
Aerospace Controls Corp
Little Rock, AK

Report left out product for testability synthesis

In Michael Markowitz's article on "Design for test (without really trying)" (EDN, February 17, 1992, pg 114), he compared our test and testability tools with those of the competition and found differences. Unfortunately, he left out Panther Expert, the top-end product of our test and testability-synthesis product line. Testability synthesis refers to all actions necessary for making an IC design testable.

Panther Expert provides three types of access: direct, serial scan, and transfer—or a combination thereof. Direct access is possible if a macro has its pins connected directly to IC pins. Serial Scan is a proven method for generating easy access and saving test design time. Transfer is used to generate access when optimal IC performance is required. It utilizes transfer properties of macros by knowing the function of the macro (for example, the multiplier c=a*b is transparent from a to c if b is fixed to "1").

Panther automatically performs test-control block generation. The test-control block controls internal signals during test without adding many test pins.

Automatic boundary-scan insertion adds the necessary input/output logic and controller to the IC design, according the IEEE-1149 standard. The scan-chain router optimizes the interconnection of individual scan chains (for macros where scan is used) into an optimal number of optimal-length scan chains.

Jaap B Sondervan
Marketing Manager EDA
Philips Electronic Design & Tools
Hilversum, The Netherlands

People's program for building "their" something

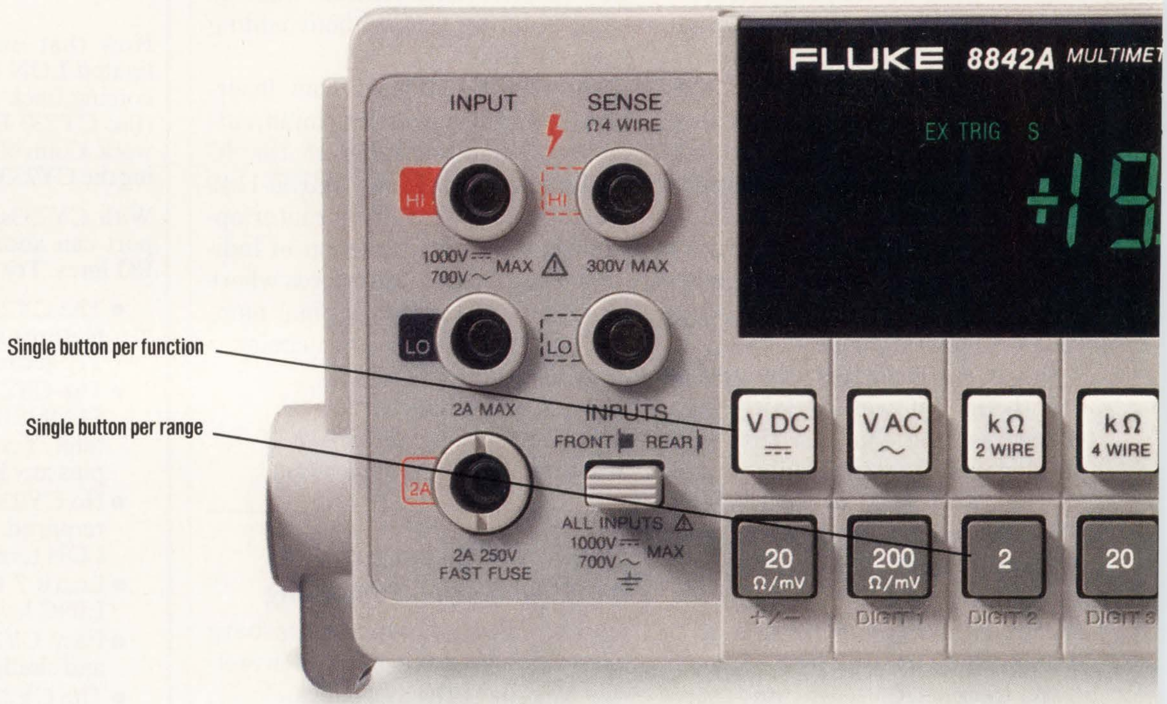
In his editorial, Dan Strassberg asks "Where have all the investments gone?" (EDN, February 17, 1992, pg 55).

If there could be a kind of economic Homestead Act, where people could use their limited means and some of their own hard work to build something that would be theirs, a whole new energy for a renewal would emerge. People in the past have given and have supported their government and industry, while receiving no tangible results.

Now, the people who do the rejuvenation need to be given a little. They need something that will show them where their hard work will do something for them. If we are a nation of the people and for the people, the people themselves must be able to achieve what their effort is about.

Roy L Ruth
Component Engineer
Video Monitors Inc
Chippewa Falls, WI

FLUKE®



Maybe the best 6½ digit DM

Can a 5½ digit DMM really outperform a 6½ digit DMM? The answer is a resounding "yes" if both ease-of-use and performance are important.

There's a lot more to evaluating a DMM's overall utility than simply counting the number of digits displayed on the front panel.

Take the time-tested 5½ digit Fluke 8842A: It gives HP's new 6½ digit 34401 something to measure up to, starting with ease of use.

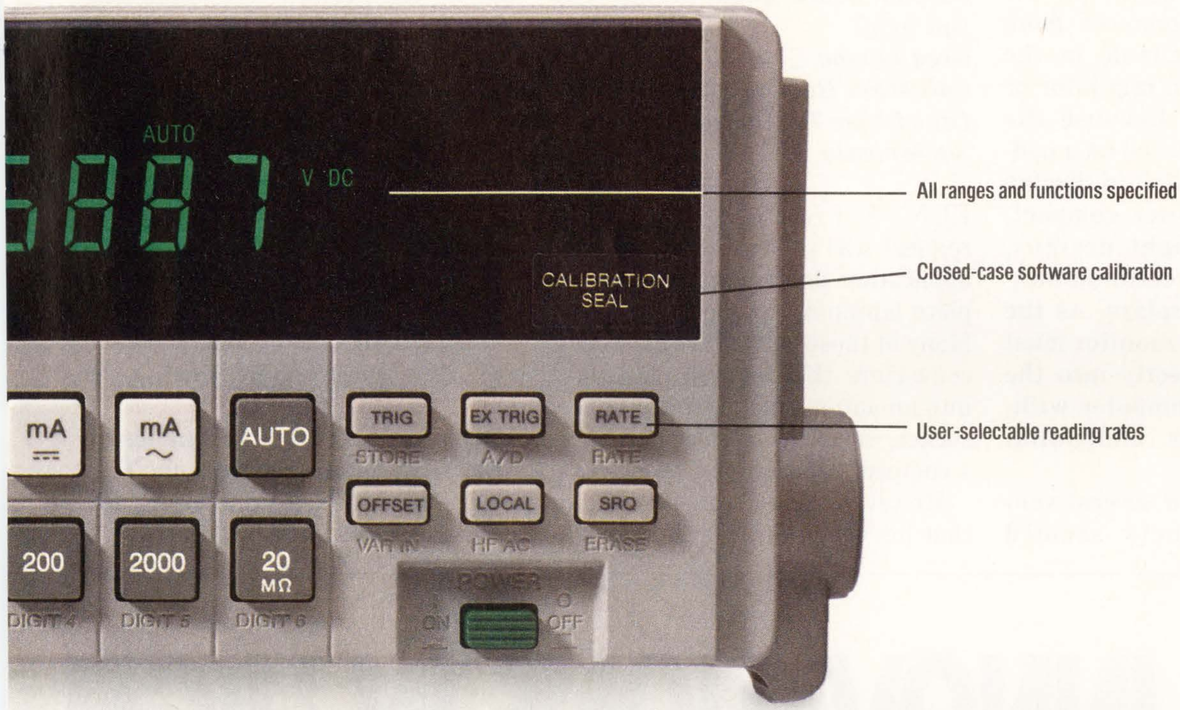
Turn on a Fluke 8842A and what you see is what you get: A clean, simple front panel, ready to use. There's a function for each button and clear annunciators that show you where you are. HP's 34401, on the other hand, powers up in 5½ digit mode and then requires as many as 14 keystrokes before finally arriving at the specified 6½ digit mode. There's no display to tell you where you are in the process. And if you turn it off, your set-up is gone.

Feature	Fluke 8842A	HP 34401A
Normal Mode Noise Rejection	>98 dB	>70 dB
Common Mode Noise Rejection	>140 dB	140 dB
MTBF	>100,000 Hrs.	Unknown
Stored Set-Ups	Not needed	No
Input Impedance @ 20V	10,000 MΩ	10MΩ
dV Ranges	Six: 20 mV – 1000V	Five: 100 mV – 1000V
Isolation, Common Mode Voltage	1000V dc	500V dc
Basic One Year DC Accuracy	±0.003%	±0.0035%

Then there's interference. Will common or normal mode noise

ALLIANCE IN TEST & MEASUREMENT

PHILIPS



M is actually a 5½ digit DMM.

interfere with your measurements? Will input impedence load your circuits? Not with a Fluke 8842A. It beats HP's 34401 hands down.

If isolation is an issue — say you're making null measurements — Fluke's 8842A provides the 1000V dc you need, unlike HP's 34401 which has just 500V dc.

Since their introduction, the 8842A and its companion the 8840A have become the most popular bench DMMs in the business because they deliver what you're looking for: accuracy, stability and ease of use. Simple as that.

So if you're looking for a tough, dependable tool, look beyond the data sheets and the footnotes.

You'll choose the Fluke 8842A. For more information, contact your local Fluke representative. Or give us a call toll-free at **1-800-44-FLUKE** (1-800-443-5853).

CIRCLE NO. 28

FLUKE®

EDITED BY JULIE ANNE SCHOFIELD

Compact monitor needed to run off car's dc voltage

We are working on a project that requires us to install a VGA (640×480-pixel resolution) monochrome or color monitor in an automobile. Our design calls for the monitor to be powered from the dc voltages available in the car, either through a regulator or a dc/dc converter. Because the monitor will be mounted on a pedestal, we are interested in display technologies that offer compact, thin, and lightweight designs, such as LCDs and electroluminescent and plasma displays. As the final constraint, the monitor must be able to plug directly into the VGA port on our computer without requiring any additional adapter hardware.

We have contacted several vendors whose products seemed promising, but so far no one can satisfy all of our requirements. Some of the vendors said that they were working on displays that would satisfy our requirements, but we feel strongly that someone has already built one, and we just haven't heard about it yet. Can you help?

Greg Larson
California Dept of Transportation
Div of New Technology
Sacramento, CA

EDN's first reaction to Mr Larson's request was to inquire whether the application precludes using a complete laptop or notebook computer. Many of these computers have dc/dc converters that let you plug them into an automobile cigarette-lighter socket, so using one seemed to be a compact solution.

However, Mr Larson informed us that his computer, which runs MS-DOS software, resides in a VMEbus card cage that requires an external monitor. Because his application is mobile, he can't use a bulky CRT display having a dc/ac inverter. He has considered using an external dc/ac inverter to drive a display, but he can't afford the power loss caused by the inefficiencies of these products. Mr Larson's application needs an external compact monitor whose dc/dc converter can operate from any automobile dc voltage—preferably 12V. If anyone knows of such a product, please contact Ask EDN.

European reader wants to renew subscription

Please send me the fax number of your European edition in The Netherlands. The number is not printed in the magazine at all. I

need to notify them that I want to renew my subscription, which expired in March.
Francisco Amado
Datalum
Barcelona, Spain

The fax number of the European subscription office is (31) 20 653 1316.

Manual needed for discontinued unit

We still use a few "Displayphones," a product of Northern Telecom sold by the Dutch company DTT until the spring of 1990. The unit is an integrated business telephone and data terminal that can handle voice and data calls at the same time, so you can talk to someone while accessing a database and viewing the information on the unit's screen.

In Holland there are no manuals or schematic diagrams available for our NT6K80 series Displayphone. Could you help us find this information?
Peter Winters
Application Engineer
Pehaco Electronics
Groningen, The Netherlands

Northern Telecom's address and phone number are

8200 Dixie Rd
Box 3000
Brampton, Ontario
L6V2M6 Canada
(416) 452-2000.

A company representative told us that most of the Displayphone documentation was sent to Liam Dowling in the Galway, Ireland, office. His phone number is 353-91-57671, and he will be sending you the manual you seek shortly.

Reader seeks processor definitions

I am a subscriber to EDN and ask for the definitions of microprocessor, microcontroller, and digital signal processor.
William P O'Hara
Scientific Components
Cheshire, CT

Technical Editor Ray Weiss responds: These days there are many confusing definitions for different processors. Here is a set of definitions that work:

Microprocessor—a processor on a chip. It may or may not have on-chip memory and an MMU, but otherwise a microprocessor is a complete CPU with registers, an ALU, and addressing capability. Some microprocessors have on-chip floating-point units; others use a support chip. Motorola's 68040, Intel's 486, and Mips' R4000 are all microprocessors.

Microcontroller—a single-chip microprocessor that has on-chip memory and peripherals. There are 4-, 8-, and 16-bit microcontrollers, but no 32-bit ones. This definition works for 4- and 8-bit chips, but starts to fail for 16- and 32-bit processors, which cannot hold enough memory for large-scale processors. The Intel 8051, Motorola 68HC05, Zilog Z8, Hitachi H8, Microchip PIC, and the NEC K0 are examples of microcontrollers. Some of these microcontrollers can access both external and internal memory. For example, the Intel 8051 accesses both external and internal memory; the Motorola 68HC05 accesses on-chip memory only.

Embedded processor—a microprocessor designed for embedded applications. Embedded processors are typically microprocessors augmented with on-chip peripherals for embedded systems and may or may not have on-chip memory. Zilog's Z80 variants, Motorola's 683xx family, and Intel's 186 and 196 are all embedded processors. By definition, microcontrollers are a subset of embedded processors. Advanced Micro Devices' 29000 and Intel's i960 32-bit RISC chip families are embedded processors. Both require off-chip memory but are used in embedded applications.

DSP processor—a microprocessor optimized for digital signal processing; that is, one that's strong in algorithmic and vector processing. DSP processors represent an evolutionary path different from that of microprocessors. DSP chips have simple memory interfaces and typically execute multiple operations in parallel. These chips generally do a multiply and accumulate (multiply two numbers and add the result to an accumulated total) in one cycle. This operation may be pipelined; the multiply could execute in one cycle, and the add execute in the next cycle in parallel with the next multiply. Additionally, DSP processors usually provide automatic indexing for the x and y parameters (the two numbers to be multiplied), which minimizes inner-loop processing.

And just to confuse these definitions, DSP processors and peripherals such as multiply-and-accumulate units (MACs) are emerging in standard microprocessors and microcontrollers. Both National Semiconductor and Zilog, for example, have added DSP capability to their microcontrollers, and Motorola has added a MAC unit to its 68HC16.

Rieger's third question answered

In the January 20, 1992, Ask EDN, James Rieger posed three questions. Answers to the first two questions were printed in the April 9, 1992, issue. His third question was "What is the carrier deviation for transmission of a satellite-relayed television signal? Because the television waveform is asymmetrical, what is the position of blanking with regard to the band edges of the channel? Does white cause a positive deviation of the carrier frequency or a negative one?" A reader wrote in to put this last question to rest.

In response to James Rieger's third question in the January 20, 1992, EDN, I may be of some help.

The carrier deviation for transmission of a satellite-relayed television signal depends on the satellite and transponder being used. Most domestic satellite-relayed television signals use frequency modulation on the 5925- to 6425-MHz band for transmitting to the satellite. The 3700- to 4200-MHz band is used for receiving from the satellite. The transponders are typically 36 MHz wide and have 20-MHz channel spacing with 40-MHz channel spacing for transponders of equal polarization.

Carson's Rule for RF bandwidth is $B_{RF}=2\Delta f+2f_V$; in this case, B_{RF} is the RF bandwidth of 36 MHz and f_V the video bandwidth of 4.2 MHz for NTSC. Thus, the Δf peak FM deviation must be less than 13.8 MHz to ensure a good quality picture with tolerable distortion.

The position of blanking level 0 with regard to the band edges of the channel is equal to 25% ±2.5% of the peak FM deviation on systems without a triangular energy-dispersal waveform. White causes a positive deviation of the carrier frequency.

Bari Ari
ONE Inc
Lake Bluff, IL

Ask EDN solves nagging design problems and answers difficult questions. Address your letters to Ask EDN, 275 Washington St, Newton, MA 02158. FAX (617) 558-4470; MCI: EDNBOS. Or send us a letter on EDN's bulletin-board system at (617) 558-4241: From the Main System Menu, enter SS/ASK_EDN and select W to write us a letter.

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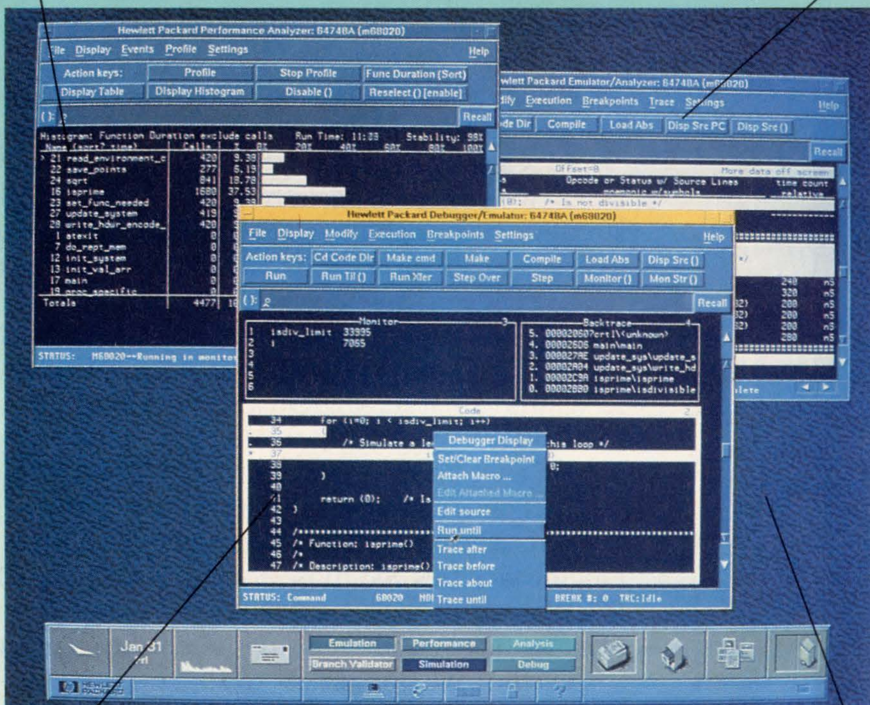

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And the interface is completely integrated. Emulators, debuggers, and the software performance analyzer all operate consistently and interactively. Which means you can share data between tools, and enjoy all the productivity benefits of synchronized measurements operating in a multiple window, high-performance environment.

So, if you're looking for a simpler way to develop embedded systems, **call 1-800-452-4844**. Ask for **Ext. 3036,** and we'll send you a free video that shows you how the HP 64000 embedded debugging environment makes it easy.

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HP 9000 Series 300, 400 & 700 Sun Microsystems SPARCstations IBM PC Compatibles		
(1)Also support for AMD, Texas Instruments, Zilog, National Semiconductor, ATT, NEC, Hitachi and Mitsubishi; call for more information.		

There is a better way.

HEWLETT PACKARD

CIRCLE NO. 33

Statistical Process Control in Semiconductor Manufacturing (short course), University of California, Berkeley, CA. University of California Extension, Dept B, 2223 Fulton St, Berkeley, CA 94720. Phone (510) 642-4151. FAX (510) 643-8683. June 29 to July 1.

Symposium on Parallel Algorithms & Architectures, San Diego, CA. HT Kung, SPAA Program Chair, School of Computer Science, Carnegie Mellon University, 5000 Forbes Ave, Pittsburgh, PA 15217. June 29 to July 1.

International Broadcasting Convention, Amsterdam, The Netherlands. IBC Convention Office, Savoy Pl, London WC2R 0BL, UK. Phone (071) 240-1871. FAX (071) 497-3633. TLX 261176. July 3 to 7.

International Workshop on Computer-Aided Software Engineering, Montreal, Quebec, Canada. Gene Forte, CASE Consulting Group, 11830 Kerr Pkwy, Suite 315, Lake Oswego, OR 97035. Phone (503) 245-6880. FAX (503) 245-6935. July 5 to 10.

IEEE Power Engineering Society Summer Meeting, Seattle, WA. Robert Youngs, Seattle City Light, 1015 3rd Ave, Seattle, WA 98104. Phone (206) 684-3040. July 12 to 16.

IEEE Nuclear & Space Radiation Effects Conference, New Orleans, LA. Charles Utrias, United Technologies Microelectronics Center, 1575 Garden of the Gods Rd, Colorado Springs, CO 80907. Phone (719) 594-8087. FAX (719) 594-8187. July 13 to 17.

International Conference on Supercomputing, Washington, DC. Ken Kennedy, CITI Rice University, Box 1892, Houston, TX 77251. Phone (713) 527-6009. July 19 to 24.

Joint European Conference on Information Systems, London, England. Elias Awad, University of Virginia, McIntire School of Commerce, Charlottesville, VA 22903. Phone (804) 924-3423. July 22 to 24.

Computational Learning Theory (workshop), Pittsburgh, PA. Robert Daley, University of Pittsburgh, Dept of Computer Science, Pittsburgh, PA 15260. Phone (412) 624-5930. July 27 to 29.

International Conference on Factory Automation, York, England. IEE Secretariat, Conference Services, Savoy Pl, London WC2R 0BL, UK. Phone (071) 240-1871, ext 222. FAX (071) 497-3633. TLX 261176. July 27 to 29.

Summer Computer Simulation Conference, Reno, NV. Society for Computer Simulation, Box 17900, San Diego, CA 92177. Phone (619) 277-3888. July 27 to 30.

National Association of Scientific Materials Managers Conference & Trade Show, Philadelphia, PA. Barbara Neff, 92 Host, St Joseph's University, Chemistry Dept, Philadelphia, PA. Phone (215) 660-1790. August 3 to 7.

Fed Micro '92: Microcomputer Conference & Exposition, Washington, DC. National Trade Productions, 313 S Patrick St, Alexandria, VA 22314. Phone (800) 638-8510; (703) 683-8500. FAX (703) 836-4486. August 5 to 6.

Symposium in Principles of Distributed Computing, Vancouver, BC, Canada. Norm Hutchinson, University of British Columbia, Dept of Computer Science, 6356 Agriculture Rd, Vancouver, BC V6T 1Z2, Canada. Phone (604) 822-8188. August 10 to 12.

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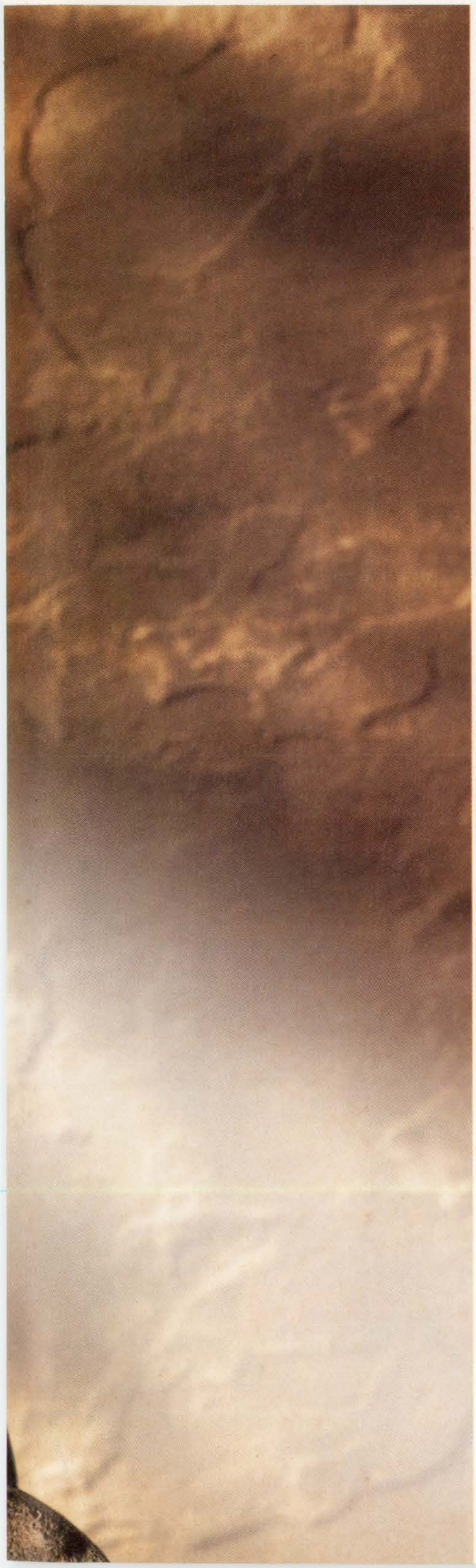

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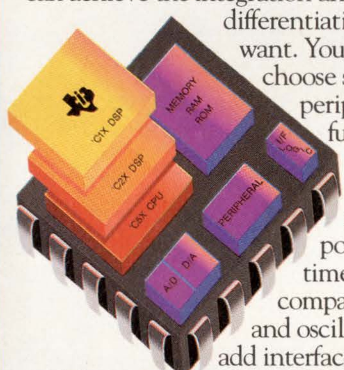

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Valid	Sun/Solbourne DECstation 3100 IBM RS6000	Design capture, simulation Design check GED, ValidSIM, RapidSIM
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TRANSFORMING TECHNOLOGY INTO CUSTOMER SOLUTIONS

Don't confine innovation to the R&D lab

In doing some research for upcoming articles, I've acquired a disquieting impression about American companies' willingness to innovate.

The field I'm exploring is filled to bursting with acronyms and buzzwords: concurrent engineering, JIT (just in time), DFT (design for test), QFD (quality function deployment), TQM (total quality management), and many, many more. The fact that so many American managers won't try new ways of doing things until someone has given those new ways a name or an acronym is evidence of the bankruptcy of the managers' approach to their jobs.

Generally speaking, what happens is that someone, usually in Japan, innovates and learns which techniques work and which don't. Then an American visits Japan, studies what the Japanese are doing, develops a seminar or writes a book, and figures out a catchy name. Only then, when the approach has been dubbed "all the rage," will Americans try it. Although the recent malaise in the Japanese stock market may have put a crimp in this copy-cat approach, there is little reason to believe that Americans won't soon return to finding more Japanese techniques to imitate.

In this country, we make much of the fact that Americans originated many of the techniques the Japanese have employed to such good advantage, and that the Japanese copied the techniques from us. But the spirit of innovation that produced those techniques is no longer evident in American business. That spirit appears to have been submerged by conservatism that threatens to engulf American business.

Of course, there is another less cynical and more hopeful explanation: American companies *are* innovating new processes for designing, developing, and manufacturing products. But companies that innovate see their innovations as a competitive advantage and don't talk about them. Maybe those companies are too busy innovating to do much talking.

As you know, EDN is written by and for design engineers. Your business is innovation; so is ours. But a company that wants to remain competitive can't confine its innovation to design. It must innovate in every one of its functions—manufacturing, test, service, purchasing, marketing, sales . . . . It must adopt innovative ways of dealing with its people. If the folks in R&D are the only ones innovating, they'll soon be innovating for some other company—if they're fortunate enough to find new jobs.

If your company has developed an innovative way of doing something and is willing to go public with the story, let me know. The sorts of things I'm looking for differ from the circuit and software innovations we publish in the Design Ideas section, or the more complex technical innovations covered in our Design Features. I'm looking for innovations in how companies define new products and get them to market, manage projects, make sure that customers are happy, etc. The innovations should affect the way design engineers work and should be the sorts of techniques that design engineers and managers can drive an organization to implement. Above all, each story should contain a message about what worked for you and why it worked.

Dan Strassberg
Technical Editor

Send me your comments via FAX at (617) 558-4470, or as E-mail on the EDN Bulletin Board System at (617) 558-4241 300/1200/2400, 8,N,1; on 9600-bps modems try (617) 558-4580, 4582, or 4398. My user ID on the EDN BBS is EDNSTRAS.

Jesse H. Neal
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CIRCLE NO. 42

DSP FOR MOTION CONTROL

Analog movements go digital with DSP

J D MOSLEY, Technical Editor

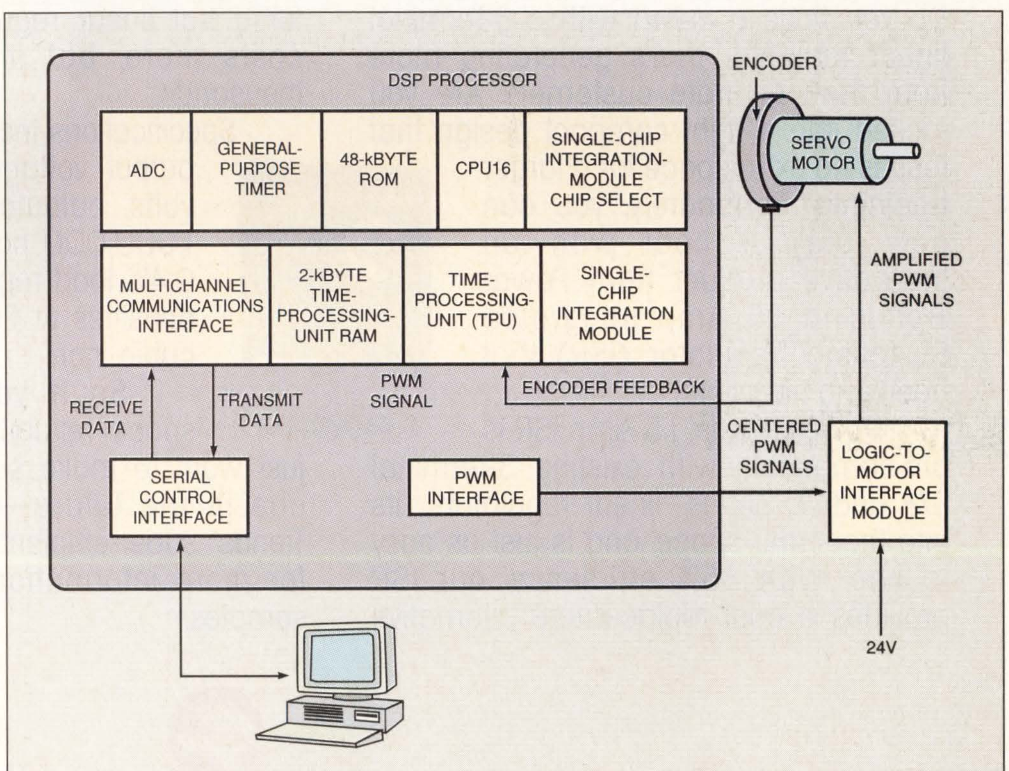
The cost of DSP ICs has plunged to half of the 1989 selling prices. As a result, design engineers are now using these chips for improved stability and precision in robotic and motor applications by avoiding the component drift and aging problems inherent in analog control circuits.

Motion control has traditionally been an analog function. However, 16-bit DSP chips—selling for as little as $3 in OEM quantities—are demonstrating that with enough speed and power you can use binary data to represent continuous movements while reducing the size and cost of your control circuit and increasing its accuracy. For example, compact DSP-based motor-control circuits are key factors in the continuing miniaturization of hard-disk drives. Similar innovative trends are occurring as design teams integrate DSP processors into automotive and robotic controls.

DSP chips are particularly suitable for use in motion control because their high-speed hardware multipliers and fast on-chip memories eliminate the delay associated with data I/O. These factors promote rapid execution of control algorithms. In addition, the filtering capabilities of DSP processors allow for smooth output and noise reduction.

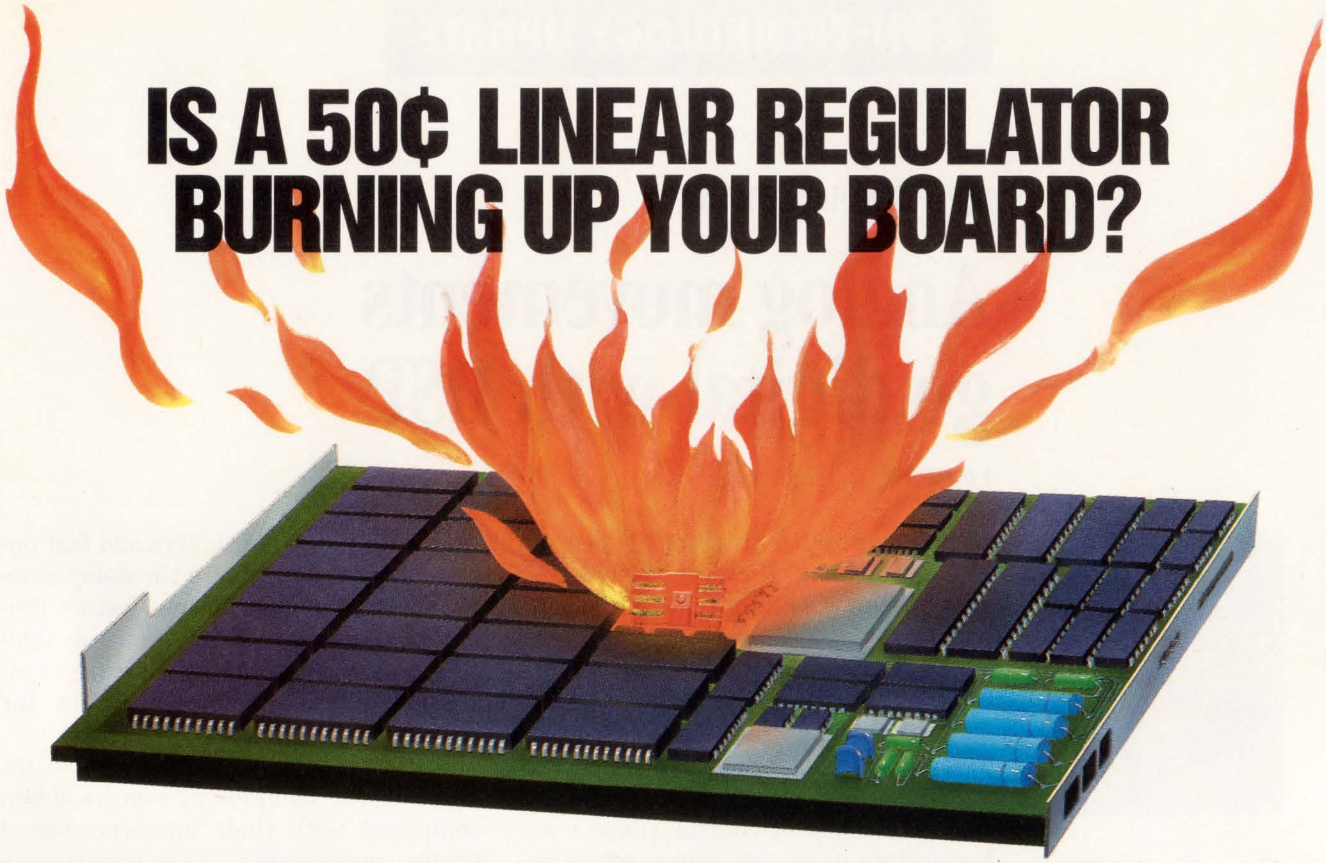
DSP-based control circuits also involve lower component counts when compared with their hardware-based analog counterparts. Fewer components result in increased reliability, faster access times, and increased circuit density.

In addition, the electrical characteristics of analog components vary with temperature and age. In contrast, even under extreme environmental condi-



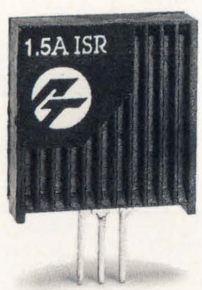
With its on-chip DSP functions, Motorola's MC68HC16Y1 microcontroller simplifies the task of designing a servo-motor control.

IS A 50¢ LINEAR REGULATOR BURNING UP YOUR BOARD?



PLAY IT COOL WITH OUR 1.5 AMP INTEGRATED SWITCHING REGULATOR

Do you have a board with a 3-terminal linear regulator that's generating more heat than an irate customer? Are you locked into a tight compact design that leaves no extra space for a larger heatsink? Fortunately, you can now play it cool with an innovative product from Power Trends—a 1.5 Amp Integrated Switching Regulator (ISR) that needs no heatsink.



Power Trends' 1.5 Amp ISR is pin-compatible with existing 3-terminal "78 and 79 Series" linear regulators, fits into the same space, and is just as easy to use. With 85% efficiency, our ISR provides a cool replacement alternative for a hot linear regulator. Of course it costs more, but it could save you thousands.

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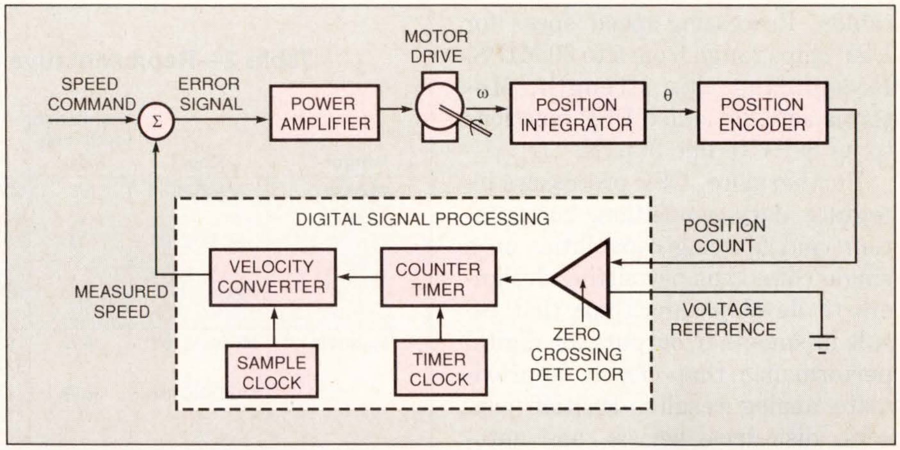
tions, digital devices remain stable and linear, so their output maintains predictability.

Applications for DSP processors traditionally involve filtering tasks for image and audio processing. However, the computational processing speed of these chips lets them rapidly implement the increasingly complex control algorithms now used in servo mechanisms more efficiently than other general-purpose processors can.

All motion-control systems include a controller, motor, load, and sensor. The motor and load are referred to as the plant. Under classical control, the control system is described as single-input, single-output transfer functions with algorithms that provide notch filtering, lead/lag compensation, and proportional-integral-differential (PID) control.

Modern control algorithms use matrices for system representation, estimation of plant output, and control law. These algorithms include state controllers, state estimators, linear-quadratic regulators, and stationary Kalman filters. Although the structure of the algorithms is the same, the difference lies in design techniques that provide multivariable control and optimization of specific performance criteria.

A more complex type of algorithm provides adaptive control with self-tuning model references and dynamic Kalman filters. Adaptive control allows for real-time system identification and parameter updates. These algorithms let you use a single controller for multiple plants, but you may have to resort to relatively expensive floating-point DSP chips for dynamic range.



When dealing with mixed analog and DSP control loops, you can use a software simulator such as Analogy's Saber to detect potential problems in the early stages of the design.

The speed difference between DSP chips and slower general-purpose processors is often an order of magnitude or more. This difference is partially because most DSP processors use a Harvard architecture, which has separate data and instruction memories that separate buses access. As a result, instructions and data move in parallel instead of sequentially, so most instructions execute in a single cycle. In contrast, a μP requires several clock cycles to execute one multiply instruction.

One example offered by Irfan Ahment and Steven Lindquist of Texas Instruments is a 13-instruction program for a PID control algorithm that executes in 2.6 μsec on a 20-MHz TMS32010 DSP chip. The same algorithm executes in 25.4 μsec if you use a 10-MHz Motorola 68000 μP or in 26.1 μsec with a 12-MHz Intel (Chandler, AZ) 8096 processor. Other speed comparisons are offered in **Table 1**.

In addition, microcontrollers (μCs) are not as precise as DSP processors because they rely on look-up tables to approximate the results of intricate algorithms. In contrast, DSP processors provide real-time calculations for analog-like performance without look-up

Table 1—Performance comparisons between DSP and general-purpose processors

Parameter	TMS320C14 DSP	TMS320C25 DSP	TMS320C30 DSP	TMS320C50 DSP	Intel 80C196 μC	Motorola 68020 μP
Instruction-cycle time (MHz)	25	40	33	50	12	24
FIR filter TAP (μsec)	0.32	0.10	0.06	0.05	2.80	1.10
PID loop (μsec)	2.30	1.40	0.84	0.75	27.00	5.10
Matrix multiply (3x3)(3x1) (μsec)	4.30	2.70	1.60	1.40	24.30	9.70
Third-order Kalman filter stationary (μsec)	15.30	7.80	4.70	3.90	Not applicable	Not applicable
Interrupt response (μsec)	0.32	0.30	0.00	0.50	2.70	1.40

(Courtesy Texas Instruments)

tables. Processing-speed specs for DSP chips range from 5 to 30 MIPS. Recognizing this strength, Motorola actually added DSP functions to its 68HC16 line of μCs.

Furthermore, DSP processors integrate data-acquisition, computation, and filtering capabilities on a single chip, thus permitting designers to develop algorithms that result in smoother outputs for digital performance that closely approximate analog results. Position sensors, disk-drive servos, and automotive-engine controls are just a few of the applications that demand such integrated capabilities.

Table 2—Representative DSP ICs for motion control

Vendor	Model	Instruction cycle time (MHz)	Price	Program memory	Data memory	Serial ports	Timers
Analog Devices	ADSP-2101	66	$72 (100)	2kx24 bits	1kx16 bits	2	1 (programmable)
	ADSP-2105	40	$9.90 (1)	1x24 bits	0.5kx16 bits	1	1 (programmable)
	ADSP-2111	66	$87 (100)	2kx24 bits	1kx16 bits	2	1 (programmable)
Motorola	MC68HC16Y1	16.78	$33.80 (10,000)	48kx16 bits	2kx16 bits	2	2
	MC68HC16Z1	16.78	$17.60 (10,000)	8k to 64kx16 bits	1-kbyte static RAM	2	2
Texas Instruments	TMS320C14	25	$9.90 (1000)	4k words	256 words	1	4
	TMS320C25	40	$15 (1000)	4k words	544 words	1	1
	TMS320C30-27	33	$137 (1000)	4k words	2k words	2	2

Tweak the software

Another reason DSP processors are gaining favor over hardware-based analog circuits is the ease of altering the control parameters. Instead of desoldering and replacing different values of resistors and capacitors, with a DSP-based circuit you can fine tune or radically change control signals via software revisions. The time and money saved in designing the initial control circuit and in revising for subsequent product improvements makes the switch to DSP chips an obvious way to cut costs without sacrificing quality.

However, to gain maximum advantage of this software-based flexibility, your design team must be adept in real-time programming techniques. To fit your algorithms into the small memory space that DSP chips have available, you'll have to resort to coding in assembly language. For example, one popular DSP processor—Analog Devices' ADSP-2105—can address only 1k 24-bit words of program RAM and 512 16-bit words of data.

To offset the difficulties of coding in such a small space, the company offers a set of development tools ranging from the $499 EZ-Kit to a $17,000 full-featured emulator. The EZ-Kit includes development-software design tools, an evaluation board for testing applications in real time, a DSP textbook, and an applications handbook with source code on floppy disks. The emulator offers an 8k-word trace buffer, breakpoints and hardware event triggers, and conversion kits for multiple processors. The company also offers a $1995 EZ-ICE emulator that provides full-speed emulation, single-step capability, 16 breakpoints, and upload/download capability from your personal computer.

Math adds to the problem

Yet, one aspect of control design that DSP development tools won't address is the mathematical conversion of vectored motion into algorithms. If you don't already have a mathematics guru on staff, it would be wise to invest in a math-analysis program. Such software helps you convert the movements you want into the algorithms that represent their mathematical descriptions.

Analogy Inc markets simulation software to ease your introduction to the z domain and sampled-data systems. The firm's $15,000 Saber simulator provides top-down modeling capability on Sun, Hewlett-Packard, and DEC workstations. Because this simulator can model both the analog and digital aspects of a motion-control loop, you gain the flexibility of mixed-mode simulation to study cascade failure effects found in actual applications. Saber lets you describe your sampled-data application as functional blocks. Its library of component and behavioral models represent algebraic, integral, differential, and rational polynomial functions.

Comdisco Systems also has a software package, Signal Processing Worksystem, for interactively designing DSP systems. Available for Sun, HP, and DEC workstations, this $25,000 simulator provides a graphical user interface that lets you design, test, and implement both DSP and mixed analog-digital designs. Via mouse and menu selections, you can create block diagrams of hierarchical signal flows in multiple windows. A signal-display editor provides analysis and review functions, including auto- and cross correlations, histograms, FFTs, and x, y plots.

Yet, even with such sophisticated tools to aid development, a DSP-based control system may not be

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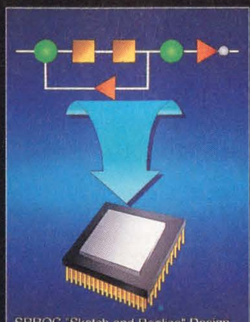

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appropriate for your application. Despite their fast computational speed, DSP processors are certainly not a panacea for motion control. Software development time tends to be longer for DSP-based controllers when compared with using general-purpose processors. In addition, μCs and μPs can actually outperform DSP chips in applications that require large amounts of memory. And if your performance criteria are not particularly high, a μP-based control circuit will typically be your least expensive digital alternative.

Your design team's ability to compress the necessary code to fit the memory parameters of your DSP chip will determine the level of complexity of your circuit. However, you should remember that the effort required for code development becomes a progressively reduced factor in the cost of your product when amortized over the production run. In contrast, hardware ultimately reaches a component-cost level that will not diminish, regardless of the volume of product you can market.

As a result, the more hardware you can replace with software, the better the bottom line will be for your product. As noted by Thomas Bucella, president of Teknic Inc, which designs DSP-based motion-control systems, some of the circuits you can replace include A/D and D/A converters, sine-wave commutation circuits, and encoder counters. A DSP processor with on-chip timers and PWM capabilities can efficiently generate arbitrary waveforms, run small isolation supplies, and calibrate circuits. Teknic has even begun utilizing fuzzy logic to implement even more sophisticated functions into its products. And to simplify the design effort of driving brushless motors, the company offers a single-chip DSP-based controller, the TEK32BL15, for $90 (OEM).

For more information . . .

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Contact Judy Racino
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Texas Instruments Inc
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Dallas, TX 75380
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However, the general-purpose DSP chip preferred by designers at Teknic is Texas Instruments' TMS320C14. Although not the most powerful of DSP processors, the C14 includes the on-chip peripherals necessary for motion control with a minimum of external hardware. The chip has four 16-bit timers, two general-purpose timers, a watchdog timer, a baud-rate generator, 16 bit-selectable I/O pins, a serial port, and an event manager with 6-channel PWM and D/A capability. The event manager consists of a 6-output-compare subsystem and a 4-input-capture subsystem. You can vary the PWM output from 8 bits of resolution at 100 kHz to 14 bits at 1.6 kHz.

When compared with traditional analog controllers, DSP-based control systems offer greater reliability, maintainability, and testability. By eliminating the analog problem of parameter drift and by providing increased noise immunity, software-driven DSP chips can actually outperform certain hardware-based controllers. Reduced size, power, weight, and costs also make DSP chips an attractive control solution.

However, you may find that it is not a simple process to convert to DSP if your product currently has a control algorithm implemented in hardware. Although some circuits will require only a simple component swap for a successful conversion, be aware that you may actually have to redesign part of your control system to accommodate the modification. To determine whether DSP is right for your control application, you must carefully analyze your design team's ability to meet the math and coding challenges that DSP controllers present. EDN

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5. Texas Instruments, *Digital Control Applications with the TMS320 Family—Selected Application Notes*, 1991.

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Video amplifiers set sights beyond large 3-dB bandwidths

ANNE WATSON SWAGER, Technical Editor

You can buy video amplifiers and subcircuits that have low, stable gains and low distortion for $3 to $10.

The latest generation of video op amps and subcircuits have much more going for them than bandwidths topping 100 MHz. Some amplifiers have differential gain and phase specifications of 0.01% and 0.01°, respectively; others have gain flatness of 0.1 dB to 30 MHz. These devices' high-frequency performance holds true for gains as low as 1 and 2. And the devices exhibit their high performance even when driving heavy loads such as cables. See **Table 1** for typical performance specs of state-of-the-art video amplifiers.

Many high-speed op amps and subcircuits also have added features that suit them for video applications. These features include gain control, fast disable pins, and devices that comprise three amplifiers.

The existence of high-speed amplifiers that are stable at low gains diminishes the misuse of the term "gain-bandwidth product." It's all too convenient for manufacturers to drop—and users to forget—the *product* part. The specification for gain-bandwidth product is meaningful only when you divide this term by the minimum closed-loop stable gain of the amplifier. An amplifier rated for a gain-bandwidth product of 250 MHz with a minimum stable gain of 5 has a usable bandwidth of 50 MHz.

The fact that many video amplifiers are stable at unity gain eliminates much of the former confusion. Even when an amplifier isn't unity-gain stable, more manufacturers are stating the bandwidth specification as the bandwidth at some usable gain. However, always be sure to check the minimum stable gain on an amplifier's data sheet.

Instead of reporting only the 3-dB bandwidth, manufacturers are starting to specify the shape of the bandwidth curve. Any peaking in the frequency response of a video amplifier distorts the video signal. Thus, gain flatness minimizes distortion. For standard color TV systems—NTSC in the US and PAL (phase-alternation line) in Europe—the desired flatness is a gain variation of only 0.1 dB from dc to 10 MHz. The desired 0.1-dB flatness for proposed HDTV (high-definition television) sytems extends from dc to 30 MHz.

Table 1—Typical performance of state-of-the-art video amplifiers

Specification	Performance
3-dB bandwidth	>100 MHz
Gain flatness	0.1 dB to 10 MHz (amplifiers for composite systems) 0.1 dB to 30 MHz (amplifiers for HDTV systems)
Minimum stable gain	1 or 2
Output drive	50 to 100 mA
Differential gain and phase	0.1%, 0.1°
Cost	$3 to $10

The ultimate in gain flatness is Harris Semiconductor's line of HFA11xx buffers and amplifiers. These devices vary by no more than 0.04 dB to 50 MHz. However, at $9.95, the devices cost much more than most other video op amps. Several op amps in the $3 to $5 price range, such as Analog Devices'

AD811 and Comlinear's CLC411, meet specifications of 0.1 dB to 30 MHz. Elantec's EL2120 has a gain flatness of 0.1 dB to 20 MHz. *(Note: All quoted prices are for 100-piece quantities.)*

Distortion takes many forms

Video amplifiers can exhibit distortion in several other ways. Two critical distortion specs are differential gain and phase.

Differential gain is the change in output amplitude of a small, high-frequency sine wave at two stated levels of a low-frequency signal on which the sine wave is superimposed. Differential *phase* is the difference in output phase of a small, high-frequency sine wave at two stated levels of a low-frequency signal on which the sine wave is superimposed.

The amplitude of a TV signal carries brightness information and the phase of a high-frequency subcarrier carries the color information. Any shift in gain or phase can distort the video picture. Thus, you need to control differential gain and phase tightly—especially in systems that cascade many amplifiers together. In component video systems—systems that operate with color already separated into red, green, and blue components—differential gain and phase are not critical specs.

Many system specs for professional video equipment call for differential gain and phase numbers of 0.1% and 0.1°, respectively. (Differential gain and phase specs are often numerically equal.) Systems that require chains of amplifiers have to use amplifiers whose specs are far below those numbers. Currently, just a few amplifiers can boast differential gain and phase specifications of 0.01 dB and 0.01°. These amplifiers include Analog Devices' AD811 ($3.35), Elantec's EL2120 ($2.80), Comlinear's CLC411 ($4.99), and Linear Technology's LT1227 ($2.45).

For less-demanding system requirements or systems that require shorter amplifier chains, more than a handful of amplifiers have gain and phase specs between 0.01%/0.01° and 0.05%/0.05°. Such parts include Analog Devices' AD810 ($2.80); Burr-Brown's OPA621 ($8.95), OPA622 ($7.10), and OPA623 ($5.10); Comlinear's CLC406 ($5.35) and CLC430 ($2.99); Harris Semiconductor's HA-5020 ($2.85); and Maxim Integrated Products' MAX404 ($2.98).

Manufacturers specify only the typical differential gain and phase partly because these characteristics are difficult to measure. Judging extremely low differential gain and phase specs with some skepticism is warranted. You should always ask how a manufacturer tests its devices.

Each manufacturer has a preferred method for testing differential gain and phase. For example, some manufacturers measure the total effect of 10 cascaded amplifiers and divide the test results by 10. This approach is somewhat flawed because there can be additive or cancellation effects between each of the 10 stages.

Some benchtop equipment, such as the Tektronix VM700 stimulus and measurement box, can measure the differential gain and phase of op amps, but this equipment is limited to the accuracy of its internal components. According to Comlinear, which supplied some of the op amps in the VM700, the instrument has a resolution of 0.01% and 0.01° but an accuracy spec of

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0.05% and 0.05°. The result, according to the company, is that this equipment can at best measure differential gain and phase as small as 0.04% and 0.01°, respectively.

Comlinear has an application note describing its method of testing differential gain and phase **(Ref 1)**. The method involves ramping the dc output of the amplifier and using a network analyzer to observe the small signal changes.

Many video applications require driving a doubly terminated 75Ω cable, or a total of 150Ω. For these cases, a gain of 2 is optimum for delivering an exact replica of the signal to the receiver. Thus, if not unity-gain stable, most video op amps are at least stable for gains of 2.

Driving these cables requires output-drive capability, and several video op amps can supply between 50 and 100 mA to the output. Analog Devices' AD811 typically can supply 100 mA; Elantec's EL2073 and EL2120 (both $7.95) can supply a minimum of 50 and 60 mA, respectively.

Many video op amps have a wide operating power-supply voltage range, which lets you use the same devices in different parts of a system. Some amplifiers are specified over the ±5 to ±15V range. Linear Technology's LT1227's range extends from ±2V to ±15V. Note, however, that a device's performance specifications at each supply level may differ. For example, the AD811's gain flatness specification extends to 35 MHz for ±15V but shrinks to 25 MHz when the op amp operates with ±5V supplies.

The power dissipation of high-speed parts continues to diminish. Burr-Brown's BUF600 and -601 video open-loop buffers ($5.68, $5.83) have quiescent currents of 3 and 6 mA, respectively, and a signal bandwidth of 320 MHz. Comlinear's CLC411 op amp has a 10-mA no-load typical quiescent current.

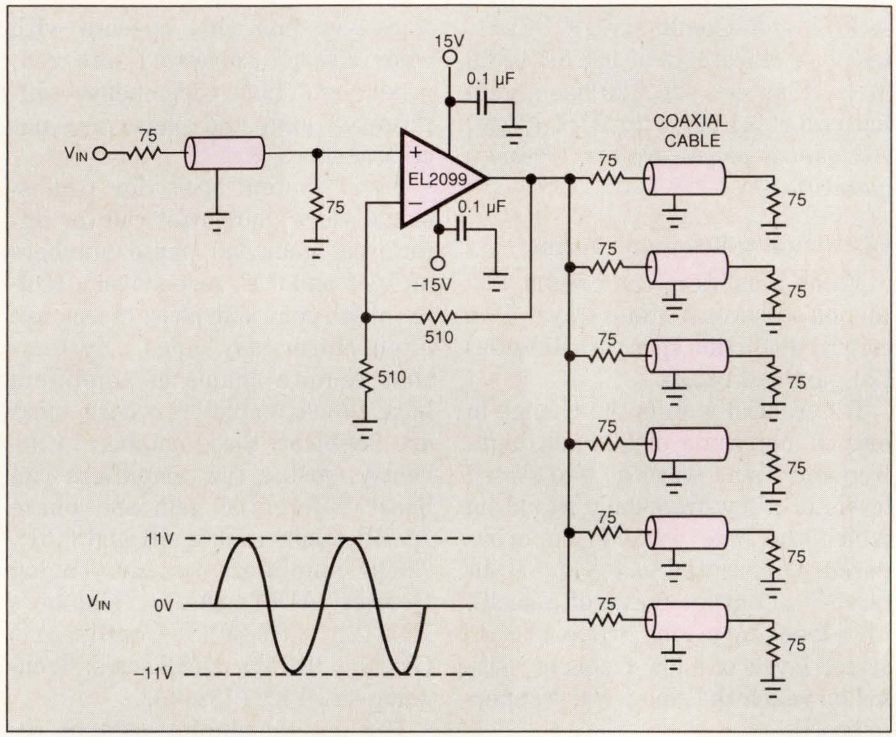


Fig 1—Driving cables is a challenge for any high-speed video amplifier. The EL2099 distribution amplifier from Elantec can deliver ±11V into 25Ω at slew rates of 900V/µsec while operating from ±15V supplies.

Finally, the cost of these parts is becoming competitive with the cost of discrete designs. You'll find these specs in many op amps that cost less than $3 **(Ref 2)**.

Features add flexibility

The standard specifications and cost of these stand-alone op amps are noteworthy. But these amplifiers can also include extra features. Several devices include fast disable pins, which makes connecting amplifiers in parallel and switching between them easy. Video op amps that have disable functions include the AD810, CLC411, and LT1227.

Several video amplifiers implement gain control. The LT1228 ($3.95) current-feedback amplifier includes a dc to 75-MHz gain-controlled amp. Together, the two amplifiers form a wideband variable-gain amplifier that has a 60-dB control range. While driving a 75Ω cable, the device's differential gain and phase are 0.04% and 0.1°, respectively.

These stand-alone amplifiers can work together to implement a variety of video functions, such as distribution amplifiers, video buffers, differential receivers, and dc-restoration amplifiers. However, many of these functions are available in stand-alone ICs.

Distribution amplifiers are common in video systems, and high-performance types are becoming available. Operating from ±15V supplies, Elantec's EL2099 ($4.95) can deliver ±11V into 25Ω at 900V/µsec and can drive six 75Ω, double-terminated cables **(Fig 1)**. (The part also works at ±5V.) This device features differential gain and phase of 0.03% and 0.05°, respectively.

Differential receivers and difference amplifiers help reject common-mode noise at high frequencies. The AD830's ($2.95) common-mode rejection ratio at 5 MHz is 60 dB. The device can provide 50 mA to an out-

VIDEO OP AMPS AND SUBCIRCUITS

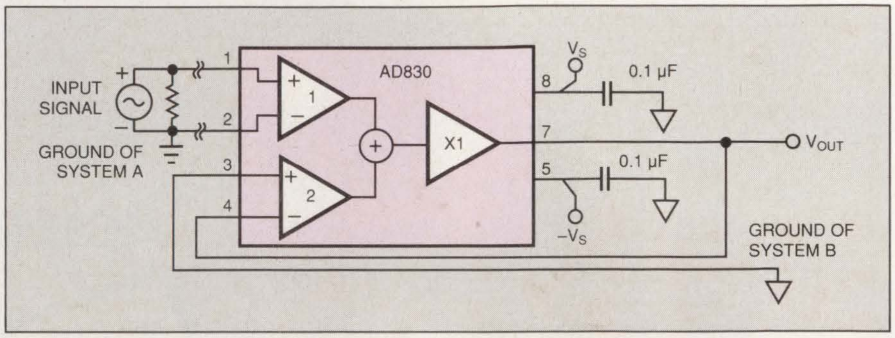


Fig 2—Configured as a differential-line receiver, the AD830 from Analog Devices receives a differential signal from system A relative to A's ground and exactly reproduces that voltage relative to the ground of system B. The device rejects any common-mode noise caused by ground noise, interference, or a mismatch between system grounds.

put and draws a quiescent current of 14 mA (**Fig 2**).

Some single amplifiers also include video-specific functions. National Semiconductor's LM1202 ($8.50) is a 230-MHz video amplifier system for high-resolution monochrome or RGB color monitors. The device includes one video amp, a gated differential-input black-level clamp comparator for brightness control, a dc-controlled attenuator for contrast control, and a dc-controlled subcontrast attenuator for drive control.

Devices that contain three amplifiers can serve as preamplifiers for graphics displays. Having three amplifiers in each package lets you slave the three devices, which provides for better tracking of the three color channels. High bandwidth for these amplifiers is necessary because of displays' high-resolution and refresh-rate requirements. For example, a 1280×1024-pixel display requires amplifier bandwidths of 100 to 120 MHz.

The one drawback of triple devices is crosstalk, which is invariably higher in packages that contain multiple high-speed amplifiers. To minimize crosstalk, National Semiconductor packages its triple RGB amplifiers in large packages and adds multiple power and ground pins to help isolate each amplifier. The isolation between one channel and a reference channel of the company's LM1203 and LM1204 (both $6.85) devices is 15 dB at 100 and 150 MHz, respectively. At lower frequencies, the isolation rises to 60 dB or greater.

Elantec also sells two triple amplifiers, the EL2390 ($6.95) and EL2393 ($5.25). Each amplifier in these devices has a flatness of 0.1 dB to 10 MHz.

Triple-amplifier devices often contain much more than three amplifiers. For example, the EL2390 includes dc-restore circuitry. In addition to the three balanced amplifiers, the LM1204 contains on-chip blanking, a sync stripper, and back-porch clamp generators. The chip also provides digital control of the contrast adjustment, brightness, and color balance. The device directly drives most hybrid or discrete CRT amplifier input stages without needing an external buffer transistor. EDN

References

1. Potson, David, and M Steffes, "Differential gain and phase for composite video systems," Application note OA-08, Comlinear Corp, 1989.

2. Swager, Anne Watson, "High-speed monolithic op amps: Low-cost op amps break speed barriers," *EDN*, January 2, 1992, pg 53.

Article Interest Quotient
(Circle One)
High 473 Medium 474 Low 475

Disk drive stores 21 Mbytes using 1.3-in. platters

Bypassing the 2.5- and 1.8-in. disk-drive form factors, Hewlett-Packard has introduced a drive that uses 1.3-in.-diameter media. The Kittyhawk drive holds 21.4 Mbytes, measures 2×1.44×0.4 in., and weighs less than one ounce. You can actually fit two Kittyhawk drives in the volumetric space required by available 1.8-in. drives.

The small size, low weight, and ruggedness of Kittyhawk prompted the company to label the product a "personal storage module" rather than a disk drive. The drive can operate reliably through a 100g shock—equivalent to a 3-ft fall onto a concrete floor. The operating-shock spec is five times better than what the best 1.8-in. drive can offer and one or more orders of magnitude better than 2.5-in. and larger drives. Therefore, the Kittyhawk will target applications ranging from automobiles to laser-printer font cartridges to video-game cartridges, as well as portable-computer applications.

The drive operates through shocks by preparing for them. It uses the same type of technology used by car makers to sense collisions and deploy air bags. Therefore, the on-board controller can ensure the drive heads are not reading or writing data when a severe shock occurs.

The manufacturers of Flash memory storage devices have targeted traditional disk-drive applications with products that cost $50 and more per Mbyte. Kittyhawk has the physical characteristics necessary to serve the same applications at OEM prices that should soon be less than $10 per Mbyte. The drive's low price and ruggedness may well find it a place in traditional solid-state applications more than vice versa.

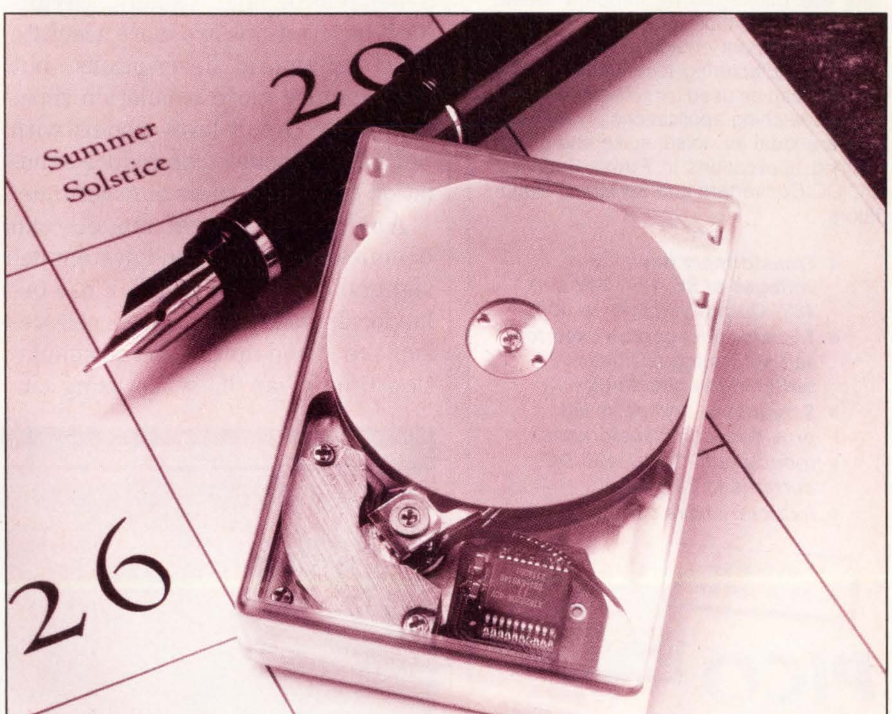
Kittyhawk provides a minimum of 100,000 start/stop cycles and features a MTBF of 300,000 hours. The drive spins its platters at 5400 rpm, resulting in an average rotational latency of 5.6 msec. It also features an average seek time of 18 msec and a sustained data-transfer rate of 0.9 Mbytes/sec.

The drive's controller includes a 4-level power-management scheme consisting of active, idle, standby, and sleep modes. Power consumption ranges from 2.2W at startup, to 1.6W for read/write operations, to 15 mW while in sleep mode. And the drive only requires 750 msec to spin up from sleep mode. The drive uses two glass-substrate platters and records data on three surfaces.

Kittyhawk's 0.4-in. height should make it among the first products to meet the new PCMCIA type-3 (Personal Computer Memory Card Industry Association) standard for removable disk drives. Furthermore, two Kittyhawk drives can fit in a single PCMCIA type-3 slot.

You can buy samples of the Kittyhawk now for $450, and production units will ship this month. Furthermore, expect higher-capacity-drive announcements from the company later this year. The drive's areal density of 111 Mbits/in^2 is state of the art, but not on the outer fringe of levels available with current technology.—**Maury Wright**

Hewlett-Packard Co, 11413 Chinden Blvd, MS 337, Boise, ID 83714. Phone (208) 323-2332. FAX (208) 323-3991. **Circle No. 730**



The first 1.3-in. disk drive available, called Kittyhawk, stores 21.4 Mbytes in a 2 × 1.44 × 0.4-in. package and can operate through a 100g shock.

Software builds analog models automatically

The Analog Model Synthesis software tool accepts graphical data from circuit simulations or laboratory instruments and produces an equivalent analog behavioral model from that data. The model is written in the company's Mast analog hardware-description language. For frequency-domain simulations, the synthesizer can extract pole and zero information from the input data. In the time domain, the synthesizer models frequency response.

You can use this $2000 product to create a model of an actual component, using lab equipment for applying stimulus to and measuring response from the part, or to convert a circuit-level description into a behavioral one. Usually, circuit-level descriptions are more accurate than behavioral descriptions, but they require more simulation time. Replacing circuit-level models with behavioral models can reduce simulation times by orders of magnitude.

Analog behavioral models can benefit chip, board, and system designers. Chip designers can use behavioral models of proven cell designs to speed up the overall simulation time of an IC while using circuit-level descriptions of newly designed cells to investigate the cells' behaviors. Board designers can encapsulate the behavior of entire subsystems using the synthesizer's ability to build models from stimulus and response data. Board and system designers can use the synthesizer to create behavioral simulation models for sensors, actuators, and other subsystems external to the circuit under development.

The company has demonstrated the synthesizer by using it to model a switched-capacitor filter (**Fig 1**). Because the synthesizer looks only at the input and output waveforms, the tool's output doesn't reflect the underlying circuitry. Thus, it didn't really matter whether a continuous- or discrete-time filter was being modeled. For the simple 1-pole filter model in **Fig 1**, the result would have been the same either way. You can use the synthesizer to create more complex models having more poles and zeros if you wish.

—Steven H Leibson

Analogy Inc, 9205 SW Gemini Dr, Beaverton, OR 97075. Phone (503) 626-9700. FAX (503) 643-3361.

Circle No. 731

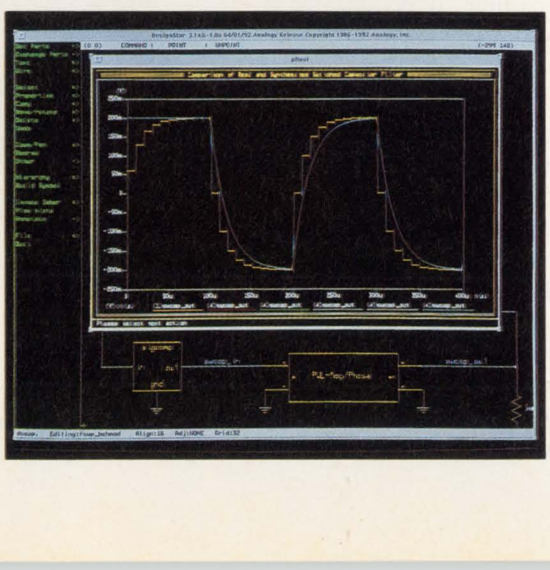


Fig 1—The response of a 1-pole switched-capacitor-filter model created by the Analog Model Synthesis software tool (blue trace) closely follows the general trend of the actual circuit's response (yellow trace). The tool can produce more accurate models having more poles and zeros, if you prefer.

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16-bit microcontroller upgrades to 20-MHz clock, 32-kbyte ROM

Intel continually modifies its 16-bit 196 family, which is one of the first 16-bit embedded controllers. A new version, the 196KD, boosts chip clock rate to 20 MHz from the 196KC's 16 MHz and doubles on-chip program ROM to 32 kbytes (ROM, one-time-programmable, or EPROM). In addition, on-chip RAM has been expanded to 1 kbyte of register and data RAM, up from 544 bytes.

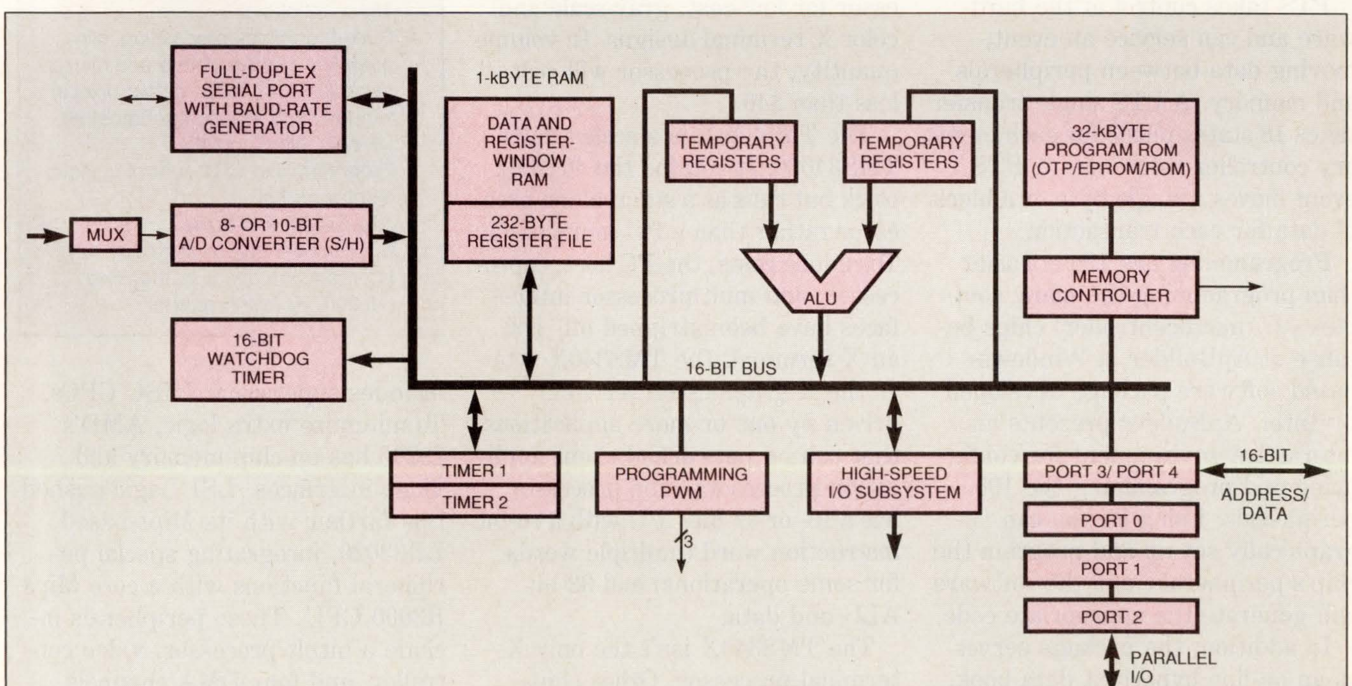
The combination of a faster clock and larger memories raises 196KD code throughput. With the faster clock, multiply (156 × 16 bits) and divide (32/16 bits) are 1.4 μsec and 2.4 μsec, respectively. A register-to-register add takes 400 nsec, which is four 100-nsec internal clock cycles (the 20-MHz external clock is divided down by two, providing a 100-nsec base clock cycle.) The larger on-chip memory opens up the chip to more effective execution for programs in higher level languages like C or PL/M.

The 196KD is organized as a register architecture. On-chip RAM consists of a 1-kbyte RAM organized as 128 16-bit (or 256 8-bit) registers, which serve as sources and destinations for ALU and other operations. The remaining RAM serves as on-chip data memory or as variable size (32-, 64-, or 128-byte) register windows that can overlay register memory. These register windows support fast context switches, saving processor overhead by switching to another register bank rather than paying the cost of saving and restoring the current register values.

Memory address space is a single, 64-kbyte space shared by both code and data. The chip provides an 8- and 16-bit external memory interface for accessing external memory. External memory access costs two clock cycles. Because the chip has programmable wait states, it can accommodate slower memories.

Originally developed as a custom processor for an automotive customer, the 196 suits motor control as well as automotive applications. Over the years, a peripheral set for the 196 has evolved that includes an ADC with variable scheduling, PWM generators, complex timing packages for capturing and detecting timing events, a waveform generator, and a peripheral controller for processing events without interrupting the CPU code stream. One μC variation, the 196MC, is tailored to control 3-phase ac and brushless dc motors.

The 196KD incorporates a number of μC peripherals: eight 8-bit I/O ports, an A/D converter, a special PWM generator with three dedicated independent timers, and the 196's HSIO—a high speed, complex timer set for capturing time on external events, and signaling time events. Also on chip is the peripheral-transaction service (PTS), whereby a controller automatically handles peripheral events (such as



Intel's 196, one of the first 16-bit μCs, has a register-based architecture with fast multiply and divide.

Intel 196KD μC

- 16-, 20-MHz external clock (divide-by-2 internal clock)
- Register-based architecture with 128 16-bit registers in RAM (or 256 8-bit registers)
- ADD(R+R), 400 nsec; NOP, 200 nsec; 1.4-μsec MPY; 2.4-μsec DIV
- 1-kbyte RAM (register and data)
- 32-kbyte ROM (EPROM, one-time-programmable available)
- Single 64-kbyte address space
- 8- or 16-bit multiplexed external bus
- Off-chip memory controller
- 48 I/O pins
- 2 16-bit timer/counters
- 16-bit watchdog timer
- 8-bit, 3-channel PWM generator
- 8- or 10-bit A/D with S/H (programmable)
- High-speed I/O: timer/counter capture and compare unit
- Peripheral transaction service: peripheral DMA controller
- 5 external interrupts
- Full-duplex serial port
- ApBuilder software graphically programs CPU/peripherals (free)
- 68-pin PLCC
- 16-MHz ROM, $21.95; 20-MHz ROM, $26.25 (2000)

A/D or HSIO time flags) without forcing the CPU to take an interrupt.

PTS takes control of the hardware and can service an event, moving data between peripherals and memory. A PTS single transfer takes 18 states plus 3 for each memory controller reference. A PTS event moves a single byte or a block of data for each transaction.

Programming the 196 is easier than programming the many complex μC (microcontroller) chips because of ApBuilder, a Windows-based software package developed by Intel. ApBuilder presents an interactive environment for configuring and programming the 196 peripherals. Using it, you can graphically set up and program the chip's peripherals, and the software will generate the appropriate code.

In addition, the package serves as an on-line hypertext data book. It documents the chip's instruction set, peripherals, and controls. This software package is an effective code-training tool; you can interactively write assembly language code using the 196 instruction set. ApBuilder is free of charge and will be available for the 196 in July.

In addition, Intel is releasing an in-circuit emulator, the ICE-196KD/HX, which provides 20-MHz 196KD operation. The ICE handles the 196 μC line as well.—**Ray Weiss**

Intel Corp, Embedded Processor Group, 5000 W Chandler Ave, Chandler, AZ 85226. Phone (602) 554-8080. **Circle No. 732**

Graphics processor strips down for X-Window

Designing X-Window terminals that cost less than $1000 is a tough task. It is getting easier, however, as chip vendors tailor processors to deliver low-cost, high-resolution-graphics performance. Texas Instruments has stripped down its TMS34020 graphics processor for low-cost, gray-scale and color X-terminal designs. In volume quantity, the processor will cost less than $40.

The TMS340X is a scaled-down TMS34020: It retains the 40-MHz clock but runs as a stand-alone processor rather than a PC coprocessor. To reduce costs, the PC host, coprocessor, and multiprocessor interfaces have been stripped off. For an X terminal, the TMS340X acts as the X-graphics-server CPU driven by one or more applications that run on networked client-application processors. The processor has a 16- or 32-bit CPU with a 16-bit instruction word (multiple words for some operations) and 32-bit ALU and data.

The TMS340X isn't the only X-terminal processor. Other chips that target low-cost X terminals include the AMD 29K, Intel i960, and LSI Logic Mips-based LR33020 RISC processors.

The 29K family is a classic RISC design that migrated to embedded systems, suiting applications in laser printers and X terminals. Intel's i960 is a specialized RISC family also used in laser printers, X terminals, and communications systems. The upper end of the i960 family includes superscalar RISC CPUs. To minimize extra logic, AMD's 29200 has on-chip memory and video interfaces. LSI Logic pushed this further with its Mips-based LR33020, integrating special peripheral functions with a core Mips R3000 CPU. These peripherals include a bitblt processor, video controller, and four DMA channels.

The advantage of the TMS340X is that it's a dedicated graphics

Texas Instruments TMS340X

- 32-, 40-MHz external clock (divide-by-4 internal clock)
- 32-bit processor; 32-bit data word and ALU; 16-bit instruction; 32-bit multiplexed external memory bus
- 30 32-bit registers in two sets: A set—15 general purpose; B set—15 special purpose
- 512-byte instruction cache (256 words)
- 100-nsec ADD (R+R), NOP
- 3.7-μsec MPY; 3.7-μsec DIV
- Single 512-Mbyte address space
- External bus for dynamic RAM, video RAM: provides as much as 1 Mbyte of VRAM; $\overline{\text{CAS}}$ strobe for DRAM; VRAM block writes; minimum 2 cycles for access
- Pixel addressing (x,y coordinates) (linear)
- Programmable pixel sizes of 2, 4, 8, 16, or 32 bits
- Built-in graphics processing: clipping, line checks, rotate and merge variable width fields, detect pixel in window, find left- or right-most bit, fill, pixel block moves
- Programmable CRT control signals; display refresh
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processor. Even though its divide-by-4 clock makes it slower than the high-clock-rate RISCs, the chip directly supports graphics processing, which simplifies graphics programming greatly. For example, the TMS340X CPU provides bit-level addressing to the pixel level. Programmers don't have to convert word- or byte-level code to find and handle bit-level data. The CPU addresses pixel data at the bit level, either as an x, y display construct or as a linear stream of bits.

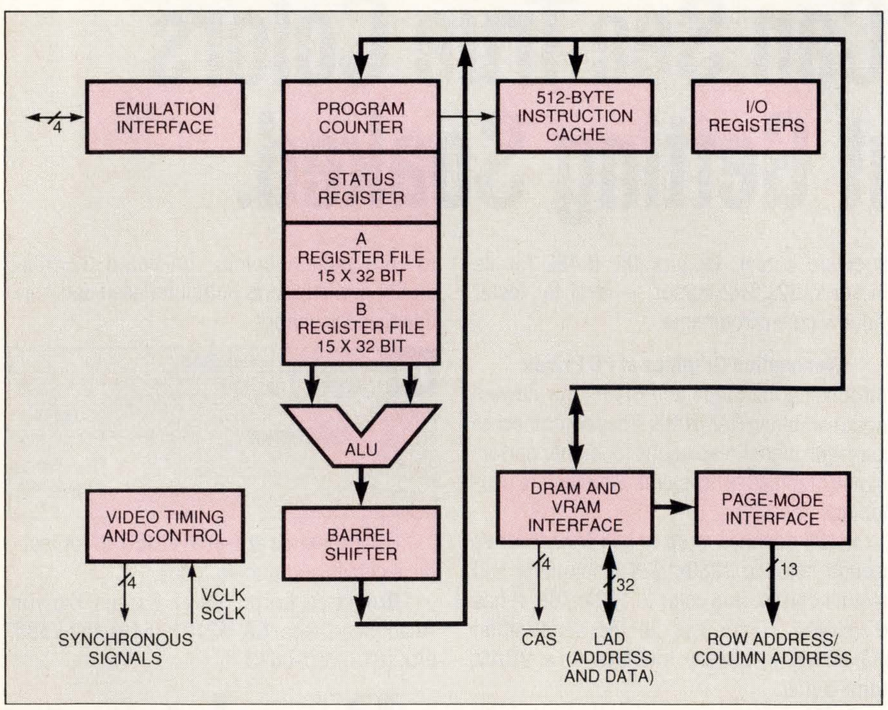
Even better, pixel and screen sizes are programmable, held in special hardware registers. The same code can drive different-size CRT displays and pixel sizes without changes—other than setting the defining hardware registers. Thus, 340X designs can work with different graphics configurations without needing redesign. The 340X's graphics instructions include pixel draw and advance, pixel transfer, inner loop of Bresenham's line algorithm, a fast line draw, pixel block transfer, fill pixel array, clip an array for window, test if pixel point in window, and fill trapezoid block lines. Window-checking hardware checks pixel placement relative to a defined window and provides automatic transparency processing for combining pixel overlays.

The chip provides mixed-memory implementations of dynamic RAM (DRAM), video RAM (VRAM), and ROM. The chip has a 32-bit multiplexed external bus, but it provides page-mode support with shared $\overline{RAS}$ and $\overline{CAS}$ address lines. Memory support includes as much as 1 Mbyte of VRAM and 4 Mbytes of DRAM. A complete X-terminal subsystem—with a 340X chip, memory (VRAM, DRAM, boot EPROM), LAN chip, keyboard/mouse/serial-port controller, two to three PAL devices for glue logic, and a RAMDAC—takes up just 35 to 42 in^2. TI's 9×10-in. X-terminal evaluation board is called the Wildcat; the company also supplies RAMDACs, including a stripped-down palette chip for low-cost gray X terminals (TLC34074).

The basic bottleneck of this chip is memory bandwidth—the amount of pixel or graphic data it can move in a given time. The 340X has a small on-chip instruction cache, 512 bytes or 256 16-bit instructions—or less, for multiple word instructions. This is enough for graphics algorithm inner loops, given the CPU's compact graphics instructions. Thus, in an inner loop, the memory bandwidth can be dedicated to pixel manipulation. With a 10-MHz internal clock and a 2-clock memory cycle, pixel bandwidth reaches 20 or 80 Mbytes/sec when setting four pixels to the same value in VRAM. According to the company, the 340X will support both color and gray-scale CRTs with a 1280×1024 resolution, and 8-bit pixels (256 colors or shades).

The TMS340x is code compatible, but not pin compatible, with the TMS34020. Instead, it comes in a lower-cost, 144-pin quad flatpack. Development tools include an ICE, assemblers, C compilers, and graphics libraries.—**Ray Weiss**

Texas Instruments Inc, Box 809066, Dallas, TX 75380. Phone (800) 336-5236, ext 3990; (213) 995-6611, ext 3990. **Circle No. 733**



The TI 340X is a stripped-down, stand-alone TMS34020 graphics processor that targets X-terminal applications.

386 µP operates at 3.3 and 5V

Switching from 5 to 3.3V for low-power applications isn't as easy as you might think. Some key parts still have only 5V versions, but not Intel's 386SL. This processor can handle mixed-voltage systems in which some circuits are 3.3V and others 5.0V. The chip's ability to manage both voltages eliminates the need for additional voltage-translation hardware.

Designers built the 386SL by integrating a static 3.3V processor core with programmable voltage translators. This version lets you reconfigure existing notebook computers designed around the 5.5V 386SL for 3.3V peripherals without adding additional circuitry. You can set both the memory bus and the

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standard PC/AT bus interfaces to 5 or 3.3V operation.

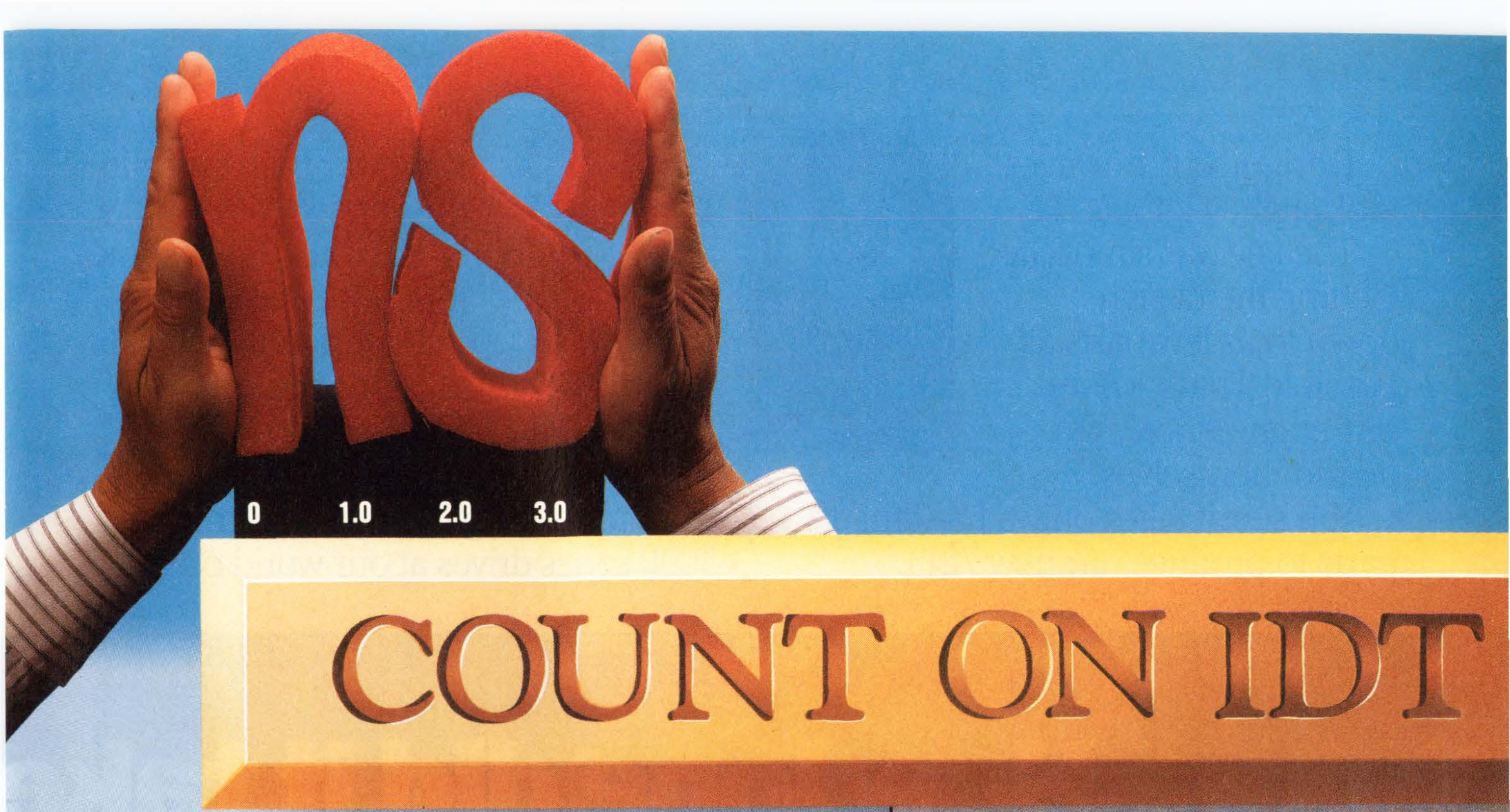
The 386SL is an extended 386. Chip designers increased processor throughput by adding an on-chip cache controller. To minimize glue logic and power, designers also added an ISA bus controller, a dynamic-RAM controller, and EMS (expanded memory) 4.0 hardware. A system-management mode integrates extended power management into the system. Instead of a single NMI (nonmasked interrupt) reset, the system supports several system-management interrupts. External and internal events that can trigger these interrupts include a battery-low indicator, suspend button, modem ring, alarm, and various clocks.

Intel 386SL μP

- 20-, 25-MHz external clock
- 32-bit processor
- Static design, clock down to 0 Hz
- Register-based architecture; eight 32-bit registers: 4 general, 4 pointer; six 16-bit segment registers
- Cache controller and tag static RAM for off-chip, write-through cache; no glue logic; 16-, 32-, or 64-kbyte cache; direct, 2- or 4-way set-associative organization; 16-bit line size
- Memory controller addresses as many as 32 Mbytes; page-mode interface; hardware LIM EMS (expanded memory) 4.0 address translation; 7-clock-cycle read/write
- ISA bus interface
- 3.3V core; 3.3, 5V interfaces
- 227-pin land-grid array
- 20-MHz version, $101 ($84 without cache); 25-MHz version, $122 (1000)

The 386SL is part of a 2-chip set. The other chip, the 82360SL, serves as an ISA peripheral subsystem. The chip has two DMA channels, two timer/counters, a real-time clock, two serial I/O ports, an interrupt controller, and a keyboard controller. The two chips interact via the system ISA bus.—**Ray Weiss**

Intel Corp, Box 58119, Santa Clara, CA 95052. Phone (800) 548-4752 for literature. **Circle No. 734**



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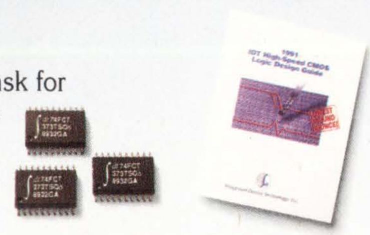

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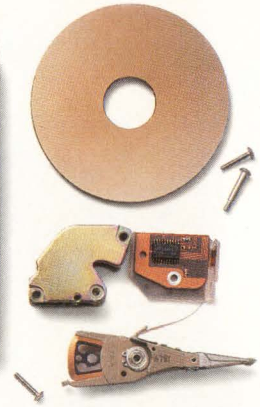

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Ray Weiss, Technical Editor

The microcontroller (μC) world is bubbling with new and evolving processors. Architectures range from simple accumulator-based CPUs to general-purpose register-set implementations having RISC-like features. Gone are the days when engineers had to make do with a simple timer and a few I/O ports. Today's μCs are bulking up on peripherals, such as A/D converters, secondary clocks, and LCD drivers. Complex timer sets and peripheral controllers offload μC CPUs by generating signals and processing events independently.

First-generation μCs are also moving up the performance trail. Designers are adding peripherals and increasing clock rates. Designers have also optimized 8-bit μCs such as Motorola's 68HC05 and Zilog's Z8 for low-end applications by reducing pin counts, using smaller packages, and lowering large-volume costs to less than $1 each. These 8-bit chips are now challenging the dominance of 4-bit μCs in low-end applications.

Architectural innovation is flourishing as μC designers devise new implementation strategies to boost chip performance. You want processing power? Now you've got it with DSP coprocessors or MAC (multiply and accumulate) units bolted onto 8- and 16-bit μCs. Chip designers have also improved performance by tailoring μCs for specific applications such as industrial and process control and fuzzy-logic processing.

Today there's a controversy about which is more effective: accumulator-based μC CPUs that have a few hardware registers or CPUs that rely on a set of general-purpose registers. First-wave 8- and 16-bit microcontrollers were accumulator based. Silicon was expensive in the 1970s, so architectures tended to use one or two accumulators and only several index registers. Most operations, particularly those to and from memory or the ALU, passed through the accumulator. Second-wave μCs took advantage of increasing silicon densities to weigh in with one or more general register sets but no accumulators.

First-wave μCs include the 8-bit Intel 8048 and 8051, National Semiconductor COP800, Motorola 6800/68HC11, and SGS-Thomson ST6, as well as the 16-bit National Semiconductor HPC, Motorola 68HC016, and Intel 196. Second-wave μC members include the 8-bit Microchip PIC family and Zilog Z8, as well as the 16-bit NEC K0/K2/K3 family, Siemens 80C166, and Hitachi H8. Some μCs, like the Z8, don't have on-chip data RAM at all. Instead, they address on-chip data storage as sets of registers.

Intel's 8048, a pioneering 8-bit μC, has an accumulator-based architecture as well as dual sets of general-purpose registers. Operations must go through the accumulator, but RAM-based general-purpose registers are available to

Microcontrollers have come a long way since the 1970s. Along the road, µCs have picked up register-based CPUs, on-chip RAM, and DSP functions. (Photo courtesy National Semiconductor Corp)

hold interim values. Intel's popular 8051, like its parent 8048, has an accumulator and a register file. The device has four RAM-based register sets, but external-memory ALU operations must still pass through an accumulator.

Another μC that combines an accumulator with register RAM is Microchip's PIC16C5x and -17C42 μCs. These processors have a RISC-like architecture that relies on a small on-chip RAM organized as registers. Unlike classic RISC (reduced-instruction-set computer) CPUs, however, PIC registers are not in a multiported register file for multiple single-cycle accesses. Instead, PIC CPUs use an accumulator or working register to hold values for memory and ALU operations.

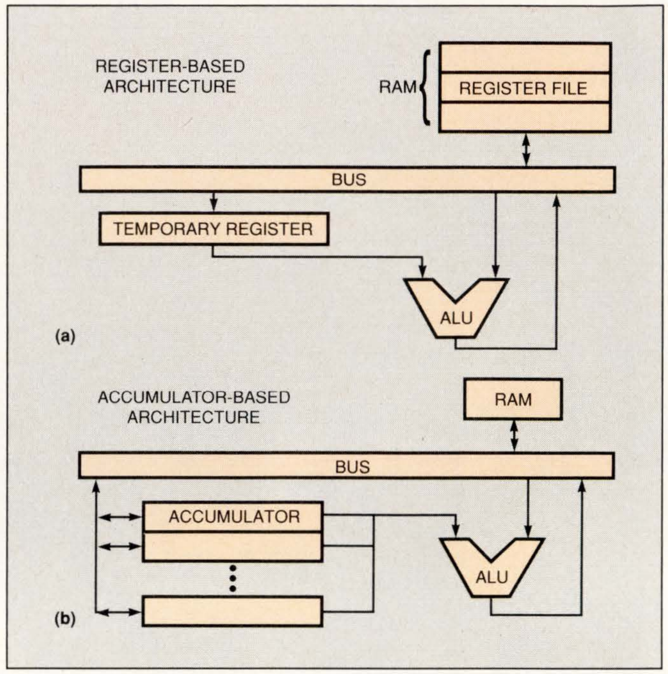
For the 16-bit 196, Intel took another tack to get around the accumulator problem. The 196 has 256 accumulators in register RAM, and ALU operations can go through any of them. The ALU core has three temporary registers to hold ALU inputs and outputs.

General-purpose register sets don't necessarily mean faster instruction cycles. Accumulator-based μCs that have hardware registers can easily gate two register inputs to an ALU in one bus cycle, as can a register-based CPU that has a set of hardware registers or dual-ported RAM. However, if not dual ported, a RAM-based register set provides one register per RAM access cycle. If an add needs two register values, the CPU needs two access cycles to move the register data for an ALU add operation. Also, the CPU needs a temporary holding register to hold the first value while it accesses the RAM for the second value.

However, general-purpose register sets do have their advantages. They can hold interim values for fast CPU access. Also, multiple register sets enable fast CPU context switches between tasks. Instead of saving all the registers, all you have to do is switch to another register set for the new task. Microcontrollers with RAM-based register sets include NEC's K0/K2/K3 family, Hitachi's H8 family, Toshiba's TLCS90, and Siemens' 80C166 family. Siemens' 16-bit 80C166 operates on a set of 16 general-purpose registers that reside in dual-ported RAM.

Timer evolution

The first μCs had relatively simple timers and counters that relied on the processor for bookkeeping and control. The 8048, for example, has a single 8-bit timer/counter (with a prescalar counter) running with an internal or external clock source. This timer leaves it up to the code to load and track timing. The situation improved with the advent of the 8051, which has two 16-bit timer/counters. These timers clock at the internal rate (with a prescalar counter) to count time or clock with an external signal to count events. Counter overflow triggers an interrupt.



A register-based architecture (a) can take longer to do an add than an accumulator-based architecture (b). The register-based design requires two cycles to move register values to the ALU.

With simple timers and counters, complex timing and counting tasks can eat up a lot of code. One school of thought began to separate the actual timer/counter activity from higher-level processing. Several companies defined a new level of hardware counting and timing capabilities, including event-triggered time capture, time-detection events, pulse counting, and pulse-width modulation (PWM). Instead of using multiple timers, this new approach involves using a free-running timer to detect multiple time points and capture the time of external events.

One of the first μC architectures to benefit from this approach was the Motorola 68HC11. Instead of confining a timer to a single task, the 68HC11 has a complex timer. A general-purpose timer runs free and is the base for counting and timing functions. The 68HC11 employs input capture and output compare registers. These registers either capture timing values based on an external event or compare the running timer value to values held in compare registers and trigger an interrupt on a match. The timer of Motorola's 16-bit 68HC16 is even more impressive. The general-purpose timer unit includes a capture/compare unit, a pulse accumulator, a prescalar counter, and a PWM unit with two outputs.

Many other μCs also employ complex timers. Intel added a complex timer/counter pack to its 8-bit 8051 μC architecture. The Intel 87C51GB has two programmable counter arrays. Each array has a 16-bit free-running timer and five compare/capture modules. The timer/counter serves as a time base for the compare/capture modules, which can act as a software timer, external event-capture register, or PWM generator. The μC also has three 16-bit timer/counters for baud generation and up/down counting as well as additional timers and event counters.

Siemens also added a complex timer package to its 80C517A-5, a souped-up 8051. Four 16-bit timers serve the compare/capture unit, which can have as many as 21 output channels and 5 capture inputs.

On the 16-bit side, Siemens' 80C166 has two timer units. One unit has two 16-bit timer/counters for simple tasks; the other unit has three. The μC also has a capture/compare unit having two timers, two reload registers, and 16 capture/compare registers. The capture/compare unit can handle as many as 16 compare interrupt-request flags and take in as many as eight I/Os as capture-event triggers. Also, Intel's 196 has a complex timer unit similar to the programmable counter arrays in the 87C1GB.

Working smarter

One of the first bits of common wisdom tossed at junior engineers is that it's better to work smarter, not just harder. Microcontroller designers have taken this advice to heart: These days, many μCs are working smarter, not harder. Instead of slaving μC CPUs to their peripherals, chip designers have offloaded much of the work in setting up, running, monitoring, and exchanging data to peripherals. Not only have

Table 1—Representative microcontroller characteristics

Processor characteristics	Processors (Vendor, μC)	Comments
Accumulator architectures	Intel 8051* Motorola 68HC05/11/16 National COP800, HPC1600 SGS-Thomson ST6 Microchip PIC	Stripped-down architectures built around a minimal register set. Generally, all major operations pass through the accumulator.
General-purpose register architectures	Microchip PIC Hitachi H8 NEC K0/K2/K3 Siemens 166, Intel 196 Toshiba TLC90	Chips use general-purpose registers. Many have multiple register sets and do fast context switches.
Complex timers	Motorola 68HC11/16 Intel 8051FA Siemens 166, 80C517A-5 Hitachi H8, NEC K2/K3 TI 370, Intel 196	Complex timers provide functions on top of one or more timers. Functions include register compares, input capture, and multiple interrupts.
Wide-word instructions	Microchip PIC Hitachi H8/300	Chips use an instruction word wider than the data path. A wide word minimizes need for 2- and 3-byte instructions.
Low-voltage chips	National COP800 Motorola 68HC11 Matra 8051 Signetics 8051 SGS-Thomson ST6, Zilog Z8 Hitachi H8	Embedded μCs for small systems that need low power consumption. Power cut by using power modes, multiple clocks, static designs, and low-power chips.
RISC techniques	Microchip PIC Hitachi H8 Siemens 166 NEC K0/K2/K3	Pipelined designs have multiple stages, not hardwired CISCs. Small instruction sets; load/store architecture.
DSP, MAC, math capabilites	Zilog Z8 derivatives Motorola 68HC16, 68302 National HP1600 Siemens 80C517A	Add math processing power via an integrated DSP processor or MAC (multiply-accumulate) unit.
Intelligent processing	Motorola 68302, 68HC16 NEC K2/K3, Hitachi H8 National HPC, Intel 196 Toshiba TLC90 Siemens 166	Offload peripheral processing from CPU with on-chip I/O controller.
Peripherals	Motorola 68HC05 National COP8 SGS-Thomson ST6 Zilog Z8	Add range of special peripherals to meet application requirements. Custom chips available having desired peripheral combinations.
Special applications	Echelon Neuron 3150 Togai FC110	μCs aimed at specific processing niches such as fuzzy logic or networked industrial control.

*Multiple second sources with architectural variations.

Table 2—Representative 8- and 16-bit microcontrollers

Company	Model	External clock (internal)	Memory	Price (10,000)	Comments
Hitachi	H8/330	(10 MHz)	32-kbyte ROM 1-kbyte RAM	$7.55	8/16-bit μC. 200-nsec instruction cycle; 16-bit instructions; OTP version available.
	H8/532	(10 MHz)	32-kbyte ROM 1-kbyte RAM	$14.20	16-bit μC has 200-nsec instruction cycle and 2.3-μsec 16x16-bit multiply.
Intel	87C51FC	16 MHz	32-kbyte ROM 256-byte RAM	$7.10	Programmable counter array, 3 timers, 32-kbyte EPROM.
	80C196KD	20 MHz	32-kbyte ROM 1-kbyte RAM	$26.25 (2000)	16-bit μC. Complex timer, PWM modules, ADC.
Matra	83C154μ-30	30 MHz	16-kbyte ROM 256-byte RAM	$8.50	Static 8051 has 3 timers with watchdog and 4 I/O ports.
Microchip	PIC16C57	20 MHz	2kx12 bits ROM 80-byte RAM	$3.16	Low-end, fast 8-bit μC in 28-pin package. OTP version available.
	PIC17C42	16 MHz	2kx16 bits ROM 256-byte RAM	$6.25	More powerful PIC. Has 8-bit data and 16-bit instructions. OTP version available.
Motorola	68HC05K1	4 MHz	504-byte ROM 32-byte RAM 8-byte EEPROM	$1.85	Stripped-down 68HC05. 10 I/O pins; 16-pin DIP or SOIC package.
	68HC11E9	4 MHz	12-kbyte ROM 512-byte RAM	$8	32 kbytes of ROM and 1 kbyte of RAM max. Has compare/capture timer.
	68HC16Y1	4 MHz or 32 kHz (16.78 MHz)	48-kbyte ROM 2-kbyte RAM	$34	16-bit μC has MAC capability and sophisticated peripherals.
	68302	16.78 MHz	1152-byte RAM	$53.46 (1000)	Communications controller built on a 68000 CPU core. Has 6 serial ports and built-in RISC CPU.
Motorola and **Toshiba**	Neuron 3150	612 kHz to 10 MHz	2-kbyte RAM 512-byte EEPROM (data)	$11.39 $10	Specialized process/network controller.
National Semiconductor	COP820CJ	10 MHz	1-kbyte ROM 64-byte RAM	$1.25	Low-end, 8-bit μC. Has watchdog timer, brownout detection, PWM timer, and analog comparator.
	HPC46100	40 MHz	Off-chip ROM/RAM 1-kbyte RAM	$12	Integrates HPC CPU with MAC unit, timer, and ADC peripherals.
NEC Electronics	78K011	10 MHz	16-kbyte ROM 1056-byte RAM	$6.38	8/16-bit μC has 4-bit peripherals, dynamic clock speed, and 32-kHz subclock.
	78K217AGC	16 MHz (8 MHz)	32-kbyte ROM 1-kbyte RAM	$8.50	8/16-bit μC has I/O controller and complex timer. 500-nsec add.
Oki Semiconductor	MSM66417	10 MHz	32-kbyte OTP 1-byte RAM	$21	Redesigned 8051 has 400-nsec instruction cycle, 16-bit internal bus, and 8-bit external bus.
	MSM67620	10 MHz	16-kbyte OTP 512-byte RAM	$24	16-bit, advanced 8051 has 200-nsec instruction cycle.
Signetics	83C751	12 MHz	2-kbyte ROM 64-byte RAM	$1.95	8051 in 300-mil-high DIP. Has serial bus.
SGS-Thomson	ST6210	8 MHz	2-kbyte ROM 64-byte RAM	$2.28	Low-end 8-bit μC in 20-pin package. No multiply or divide; 6.5-μsec add.
Siemens	80C166S	40 MHz (20 MHz)	8-kbyte ROM 1-kbyte RAM	$25	16-bit RISC-like μC has 4-stage pipeline with 100-nsec stages.
	83C517A-5N	18 MHz	32-kbyte ROM 256-byte RAM 2-kbyte XRAM	$15	Enhanced 8-bit 8051 has extra RAM, 32/16-bit math unit, and timer compare/capture unit.
Texas Instruments	TMS370C756	20 MHz	8-kbyte ROM 512-byte RAM 512-byte EEPROM (data)	$17.51	8-bit μC has complex timer, PWM generator, and watchdog timer.
Togai	FC110	20 MHz	Off-chip memory 256-byte RAM	$50 (1000)	16-bit μC has instructions for fuzzy logic.
Toshiba	TMP90C840AN (member of TLCS90 family)	12.5 MHz	8-kbyte ROM 256-byte RAM	$4	Dual register set; 163 instructions. Has stepping motor control and I/O DMA.
Zilog	Z86L06	8 MHz	1-kbyte ROM 124-byte RAM	$1.45	Low-end, 18-pin μC features 2V operation, brownout detection, and analog comparators. Has 1-μsec instruction cycle.
	Z89120	20 MHz	24-kbyte ROM 256-byte RAM	$11.25 (1000)	8-bit Z8 μC plus a 16-bit DSP chip. Separate processors have their own I/O and peripherals.

Notes: MAC = multiply and accumulate; OTP = one-time programmable; RISC = reduced-instruction-set computer; XRAM = extended RAM.

8- and 16-bit microcontrollers

peripherals gotten smarter, but some μCs now have peripheral controllers that service peripherals directly instead of forcing a CPU interrupt and context switch. These controllers typically use DMAs to exchange data between peripherals and memory.

NEC's K2/K3 series has a built-in macro service that automatically responds to peripheral events. Macros steal bus cycles from the CPU to move data between memory and a peripheral. The CPU doesn't have to take an interrupt and pay the penalty of a context switch.

Hitachi's 16-bit H8/500 has an on-chip data-transfer controller that bypasses the CPU by moving data between peripherals and memory. An interrupt activates the data-transfer controller and provides a pointer to the DMA transfer information in register memory. The controller can trigger another interrupt at the end of the DMA transfer to signal a peripheral event to the CPU.

The peripheral-event controller of Siemens' 80C166 provides an alternative service to peripheral interrupts. As many as eight interrupts are handled by peripheral-event-controller service channels. Each channel moves a word at a time and automatically decrements a counter for that channel. The controller takes priority over most CPU interrupt servicing. The worst-case, peripheral-event-controller, interrupt-response time is 350 nsec at 40 MHz, which is less than the worst-case interrupt response of 500 nsec. Both times assume on-chip ROM code execution.

Intel has upgraded its 196 architecture with a peripheral-transaction server, which can handle transfers of as many as 32 bytes for each peripheral event. Intel engineers added a waveform-generator block to the 196MC. The block generates 3-phase sine waves for motor control. Coupled with an on-chip PWM module, the 196 can sustain PWM frequencies exceeding 30 kHz.

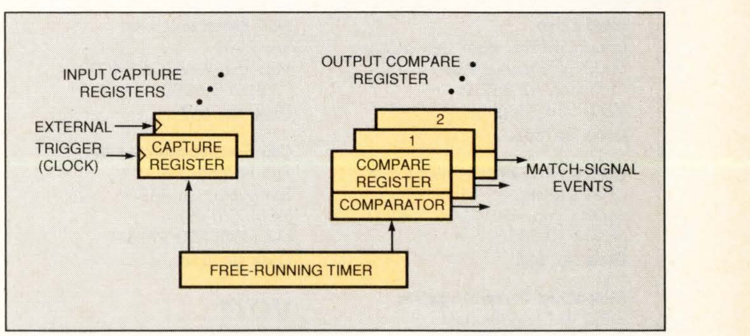
Early 8-bit μCs were lucky to have a set of ports and a timer. But over the years, 8-bit μCs have followed in the footsteps of their 4-bit ancestors by adding peripherals, including drivers for LCDs and other displays. Many 4-bit μCs are customized for specific applications. Following that lead, Motorola's 8-bit 68HC05 exists in more than 100 variations. Motorola engineers developed many of these chips as custom designs—variations on the 6805 with a different peripheral twist—and later converted the custom chips into mainline products. To encourage even more diversity, Motorola has set up a program to tailor application-specific processors for custom applications. For volume production, the customization cost ranges from nothing for mixes of common peripherals to ASIC NRE charges for custom circuits.

National Semiconductor, Zilog, and SGS-Thomson have similar programs to provide application-specific processors. Many 8-bit μCs are manufactured using modular chip layouts. Thus, vendors can easily devise special peripheral mixes or add new peripherals to the base design. The National Semiconductor COP800 employs a dual-bus structure for adding peripherals and special functions.

NEC, a major 4-bit-μC supplier, is moving its 4-bit peripherals to its 8-bit K2 processor line. The new K0 line, μPD780xx, is based on a stripped-down version of the K2. The line is code compatible with the K2 line and features display drivers and controllers for LCDs and fluorescent displays. The K0 line has an added multiclock capability, which lets you dynamically change the base clock rate to a number of count-down values. NEC also added a 32.67-kHz secondary clock, or subclock. A common feature of 4-bit watch processors, the subclock delivers a slow base clock rate to minimize power while waiting for a trigger event.

Peripherals alone are not enough. Many engineers also want increased microcontroller processing power to accommodate larger and more complex programs and handle demanding applications such as servo control. Using RISC techniques is one way to boost CPU power. RISC techniques and characteristics include pipelining, minimal instruction sets, load/store architectures, fixed instruction-word sizes, sets of general-purpose registers in a register file, Harvard architectures (separate instruction and data memory buses), and simple, easily implemented instructions. The idea behind RISC is to simplify the architecture and thus minimize implementation logic. Simpler, less complex logic results in a compressed register-to-ALU cycle time, which speeds execution.

Designers are applying these techniques to a new generation of high-end 8- and 16-bit μCs. These microcontrollers include the Hitachi H8, NEC K0/K2/K3 series, and Siemens 80C166. None of these μCs are classic RISC processors; nonetheless, they share some common characteristics including general-purpose reg-



A single timer can handle multiple functions. Input registers capture timer values on an external trigger. Also, compare registers hold time points that are detected and flagged as events.

ister sets and load/store architectures that have some instruction exceptions. These architectures lend themselves to high-level languages like C.

The most RISC-like μC is Siemens' 16-bit 80C166. It utilizes a 4-stage pipeline and has a dual-ported register file. The device includes a branch-target cache, which caches the last branch-target address to minimize branch delays during looping. And like later RISC chips, the 166 has multiply and divide instructions. At 40 MHz, if the pipeline is full and no long instructions, such as multiplies or divides, are waiting, instructions step through the pipeline in 100-nsec increments. The average instruction latency is 400 nsec (4 stages × 100 nsec).

The Siemens 166 differs from classic RISC CPUs. First, it—and all other RISC-like μCs—has no data or instruction caches. Instead, the μC holds 8 kbytes of ROM or PROM and 1 kbyte of RAM on chip and addresses as much as 64 kbytes of external memory. Second, unlike classical RISC processors, the 166 is not a load/store machine in which all accesses to memory are loads and stores and all data manipulation is between registers. In the 166, you can add a register to a memory location.

Hitachi's H8/300 series μCs aren't full RISC processors either. However, Hitachi designers employed several RISC concepts. The H8/300 is a load/store architecture based on a set of general-purpose registers and has a fixed instruction size of 2 or 4 bytes. An H8/330 delivers a base 200-nsec instruction cycle with a 10-MHz clock (20 MHz external).

Designers of the Motorola 68302—a specialized communications processor—built in a RISC-like processor to supplement the 16-bit 68000 core processor. The RISC-like processor handles line-level communications processing including checking, stripping off, and adding packet headers and trailers. The chip uses six serial ports as I/O for three full-duplex serial communications controllers. The controllers support protocols including the High-level Data Link Control protocol (HDLC), Synchronous Data Link Control protocol (SDLC), Binary Synchronous Communications protocol (BISYNC), and the Synchronous/Asynchronous Digital Data Communications Message Protocol (DDCMP).

RISC techniques aren't confined to high-end 8- and 16-bit μCs. They've been applied to the low-end 8-bit chips as well. One 8-bit μC that takes advantage of

Manufacturers of 8- and 16-bit microcontrollers

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RISC techniques is Microchip's PIC μC line. Designed originally as a peripheral controller for minicomputers and mainframes, the PIC architecture has since found a niche as a low-end μC crammed into a package that can have as few as 18 pins.

PIC μCs have a small set of single-word instructions: 33 for the PIC16C5x line and 55 for the PIC17C42, which the company introduced last year. Both lines feature a 2-stage pipeline (fetch, execute) for all instructions. At 20 MHz and with a divide-by-4 internal clock, the PIC16C5x has a 200-nsec clock cycle, one period for each pipeline stage. When the μCs are executing sequential code, each instruction appears to execute in one clock cycle. However, like its older-brother RISC CPUs, when the execution thread hits a branch, the μC incurs a 1-cycle penalty while reloading the pipeline.

Microchip's PIC designers took a wide-instruction-word approach similar to that of 4-bit-μC designers. The PIC16C5x has a 12-bit instruction word, and the PIC17C42 has a 16-bit instruction word. A wider instruction word gives 8-bit microprocessors a definite advantage in instruction processing. The wider word minimizes the need for multiple-byte instructions because the word is big enough to hold an opcode, source/destination, and literal value.

Like most early commercial RISC processors, PIC microcontrollers don't have multiply or divide instructions—these operations are done in software. Consequently, PIC microcontrollers suit fast, low-cost control applications, not tasks requiring heavyweight math processing. Another limitation is the μCs' small data RAM, which is organized as registers. The PIC16C5x has as many as 80 bytes, and the PIC17C42 as many as 232 bytes. Also, an automatic stack feature limits task processing in both microcontrollers.

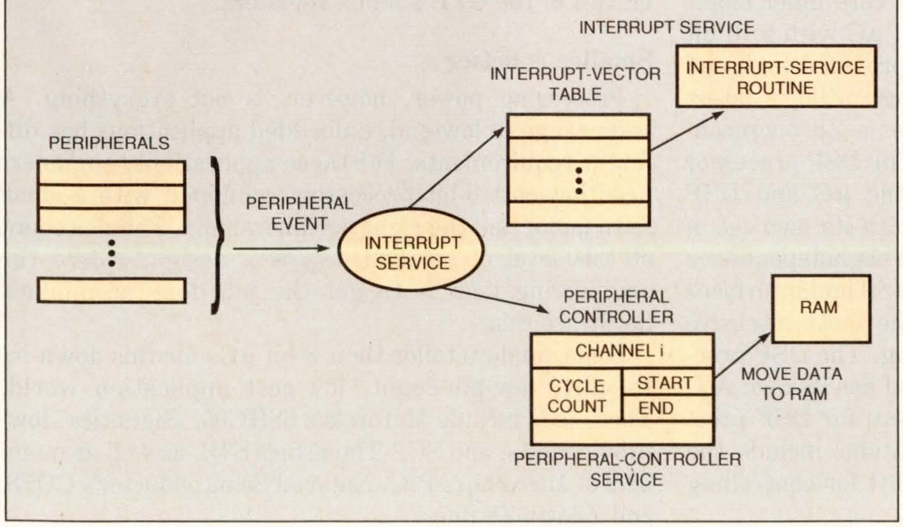
You don't necessarily have to go to newer architectures to get higher processing power. Older architectures, such as the Intel 8051, are beefing up as well. Several vendors are already working on new, high-speed cores to take advantage of today's design technology and cheaper silicon.

Oki Semiconductor has revamped the 8051 core for its nX family, which comprises the 8-bit 65K series, 8/16-bit 66K series, and 16-bit 67K series. These μCs are spin-offs of the 8051 architecture. They keep the older chip's Harvard architecture and can address as many as 64 kbytes each of program and data memory. A translator is available for porting 8051 code.

The minimum instruction-execution time for an 8-bit 65K series μC running at 10 MHz is 400 nsec, compared with 1 μsec for a 12-MHz 8051. The 66K series chip runs at the same clock rate but combines an 8-bit external bus with 16-bit internals (ALU, registers, buses) to boost processing power. The 67K series chip has a 16-bit CPU that delivers 200-nsec instruction cycles. A 16-bit add takes 200 nsec, a 16×16-bit multiply takes 2.3 μsec, and a 32/16-bit divide also takes 2.3 μsec.

Another 8051 vendor, Siemens, increased processing power by adding potent peripherals. Siemens' SAB80C517A-5 includes a multiplication/division unit that supplements the 8-bit 8051 with 32-bit division and 16-bit multiplication. The unit has six registers for operands and results. At 12 MHz, a 32/16-bit divide takes 6 μsec; a 16/16-bit divide, 4 μsec; and a 16×16-bit multiply, 4 μsec. The multiplication/division unit gives the 8051-class processor the same math capabilities as many 16-bit μCs.

Siemens' engineers removed more processing bottlenecks by adding 2 kbytes of extended RAM to the 8051 as well as providing eight 16-bit address pointers. The 8051 normally has a maximum of 256 bytes of



Some high-end microcontrollers have a peripheral controller to offload the CPU. The controller moves data to and from peripherals and memory on a cycle-stealing basis.

8- and 16-bit microcontrollers

RAM. (Using extended RAM, however, results in an external-access penalty.) The additional 16-bit pointers make life a lot easier for 8051 programmers, who otherwise are restricted to one DPTR pointer.

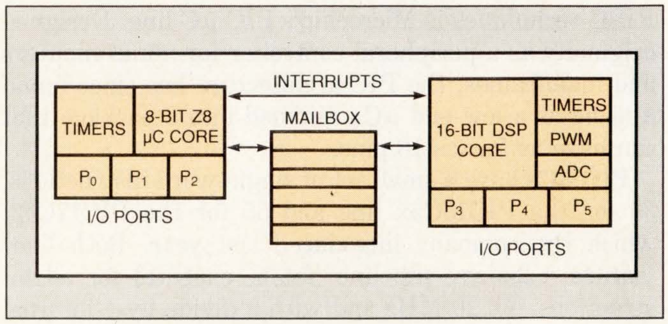
Other vendors, such as Motorola, have no plans to upgrade their µC architectures. Instead, management is counting on improved speeds and greater chip densities as silicon processes improve. Higher silicon densities mean room for larger ROM, RAM, and EEPROM, as well as for more peripherals and faster clocks. Shrinking a layout to 80% of its previous size and keeping the original die gives designers more area for larger memories or more peripherals. An 80% shrink every two to four years is not excessive. Keeping the die size constant, the first shrink provides an additional 36% area. The second and third shrinks provide 59 and 73% more area than the original chip.

Some vendors are increasing performance by raising clock rates. National Semiconductor kicked up performance on its 16-bit HPC microcontrollers by going to a 40-MHz external clock (20-MHz internal). Signetics and Matra have moved 8051 clock rates to 33 and 30 MHz, respectively. And Siemens is introducing an even faster 8051 version this month.

Adding DSP power

Another way to push the power curve is to bolt on additional computational power to a µC architecture in the form of a DSP coprocessor or DSP capabilities. DSP provides the horsepower to handle tough matrix and vector processing quickly. DSP processors typically have a multiply-accumulate (MAC) unit that multiplies two variables in one clock cycle and keeps a running sum in an accumulator register. In addition, DSP processors automatically address parameters (the x, y values for multiplication) by indexing through tables. The combination of a MAC unit and automatic indexing minimizes the overhead of a core inner loop.

Zilog was first to integrate an 8-bit µC with a 16-bit DSP coprocessor. The combination provided high-end processing capability in a µC package. Zilog's latest version is the Z8912, which combines a Z8 microcontroller with a 16-bit DSP processor. The DSP processor is not slaved to the Z8. Instead, the µC and DSP processor operate in tandem, each with its own set of peripherals and interrupt handling. This independence lets the Z8 concentrate on digital control and interfaces while the DSP processor handles the math-intensive through put processing and interfacing. The DSP processor drives its own PWM channel and has its own A/D converter to take in analog parameters for DSP processing. Other Zilog Z8/DSP combinations include the Z86C99, which has peripherals and I/O for controlling hard-disk drives.



The Z89120 chip integrates a Z8 microcontroller and a 16-bit DSP processor. The two run independently and coordinate processing through a shared mailbox and interrupts.

In the 16-bit arena, National Semiconductor integrated a 16-bit DSP MAC unit in its HPC4600 16-bit µC. The HPC µC has an accumulator-based, minimal architecture with 256 bytes to 1 kbyte of data RAM and 8 or 16 kbytes of program ROM. Its CPU has several built-in speed-ups such as 1-byte, complex instructions and automatic loop indexing with bounds checking. National Semiconductor engineers stripped out the ROM to make room for the supplementary MAC unit.

Unlike Zilog's implementation, National Semiconductor's MAC unit is tightly coupled to the µC; it uses the processors' registers to set up and load the variables and control the loop counts. A 16×16-bit MAC cycle takes eight 50-nsec clock cycles, or 400 nsec. The µC includes a 3-timer PWM unit that runs in parallel with the CPU. The company has aimed this chip at the servo-control market, such as hard-disk head positioning and process control loops.

Motorola's designers also added a MAC unit to the 68HC16, the 16-bit extension to the 68HC11 8-bit µC. The MAC unit is tightly coupled with the CPU and has two 16-bit multiplier registers and 36-bit accumulators. Addressing is automatic and circular, but relies on two of the CPU's index registers.

Smaller is better

Processing power, however, is not everything. A wide range of low-end, embedded applications has different requirements. For these applications, engineers need low-cost 8-bit processing combined with a small form factor and the right peripheral mix. Pennies count at this level of embedded-system design, where the engineering task is to get the job done at minimal hardware cost.

Some vendors tailor their 8-bit µCs for this down-in-the-dirt, low-pin-count, low-cost application world. These µCs include Motorola's 68HC05, Signetics' low-profile 8051s, and SGS-Thomson's ST6, as well as members of Microchip's PIC, National Semiconductor's COP8, and Zilog's Z8 lines.

8- and 16-bit microcontrollers

Motorola's 68HC05K1 is a low-end 68HC05 for logic replacement and other low-cost applications. Costing less than $1 each in large quantities, the 68HC05K1 integrates the basic 05 architecture—accumulator, index, stack pointer, and program-counter registers—with 32 bytes of RAM, 504 bytes of user EPROM, and 8 bytes of "personality" EPROM for holding processor- or product-specific data. The μC also includes a 15-bit timer and a watchdog timer. Running with a 4-MHz external clock, the chip completes an indexed add in 1.5 μsec.

Zilog has a line of low-end Z8 μCs for specific application areas such as video and multimedia, automobiles, and consumer goods. The line includes a μC that operates inside a mouse at 3V. Packaged in 18-pin DIPs or SOIC packages, these Z8s have 1 kbyte of ROM, 124 bytes of register-set RAM, a watchdog timer, brownout protection, and optional low EMI/power operation. Peripherals include analog comparators and serial peripheral interfaces. At 12 MHz, a typical instruction time is 1 μsec.

Processing power is not everything. Low-end embedded applications require low-cost 8-bit processing combined with a small form factor and the right peripheral mix.

SGS-Thomson's ST6 and Microchip's PIC16C5x μCs also suit low-end applications. Pin counts for these chips are 18 to 28 pins and 20 to 28 pins, respectively. Both μCs have small instruction sets: 31 instructions for the ST6 and 33 for the PIC. And because the chips are intended for basic control functions, both lack multiply and divide instructions. The ST6 has the advantage of as many as 512 bytes of RAM and 16 kbytes of ROM versus the PIC's 80 bytes of RAM and 2 kbytes of ROM. However, the PIC has the performance edge, with a basic instruction cycle of 200 nsec versus the ST6's 6.5 μsec.

Another low-end 8-bit μC is National Semiconductor's COP800, a first-wave μC with a simple accumulator-based architecture. Pin counts can be as low as 20 pins. Peripherals include a 16-bit timer/counter, PWMs, a brownout detector, and a watchdog timer. In large volumes, the chip costs less than $1.

Another way to increase processing throughput is to tailor a processor for specific applications. Two examples of such specialized 8-bit μCs are the Togai Infralogic FC110, which executes fuzzy-logic programs, and the Echelon Neuron chips made by Motorola and Toshiba, which are tailored for networked industrial, office, and process control.

Togai's FC110 is a 16-bit processor that has a reduced instruction set of 19 operators. Instruction and main data memory are 16 bits wide. The chip has a 64-kbyte address space for program and memory and 256 bytes of byte-wide local memory to hold parameters and stack information. Special instructions speed fuzzy-logic processing.

A fuzzy-logic program includes a set of input membership functions that determine the fuzzy sets—such as warm, hot, low, fast—that input variables fit into. A set of logic rules (if x is hot, then turn y high) and a "defuzzifier" convert rule results into output variables. The FC110 converts inputs into membership functions and then evaluates the rules in parallel. Evaluating a simple problem comprising 2 inputs, 1 output, and 7 rules takes the FC110 32 μsec; 7 inputs, 3 outputs, and 35 rules takes 172 seconds; and 20 inputs, 10 outputs, and 100 rules takes 2.11 μsec.

Echelon engineers designed a specialized Neuron μC with built-in code for the Lontalk networking protocol and low-end communications. The Neuron 3120 and 3150 (ROMless) chips represent a new approach in commercial processor design. Given three tasks—networking, low-end communications, and process control—the designers opted for three concurrent processors, one for each task, all on a single chip. Each CPU has its own register set, but the three CPUs share the data and address ALUs and memory resources. The processors are pipelined, and instructions take three clock cycles. The CPUs have a data stack and a call-return stack. Clock rates run from 655 kHz to 10 MHz.

The three CPUs run in parallel, offset from each other by one clock cycle in their pipelines—when CPU_1 executes pipeline cycle 1; CPU_2 executes cycle 2; and CPU_3 executes cycle 3. The benefit of this approach is that there is no context-switch overhead for moving from task to task. Tasks don't need scheduling—they essentially time-share the processor resources. At 10 MHz, instructions take 0.6 to 4.2 μsec. A dedicated tool set, Lonbuilder, as well as a C variant for networked control applications help you utilize the chips.

Unlike the commercial desktop RISC world, which is coalescing on a few architectures, the embedded-system world is continuing to diversify as vendors compete to give engineers the magic combinations of processor power, peripherals, power management, and cost. Microcontroller architectures won't stand still, they'll continue to evolve. Process shrinks will open up the 8-bit μCs to larger on-chip memories and faster logic. You can expect to see on-chip memory double in the next two years. At the same time, peripherals will continue to get much smarter, and that trend will continue as well.

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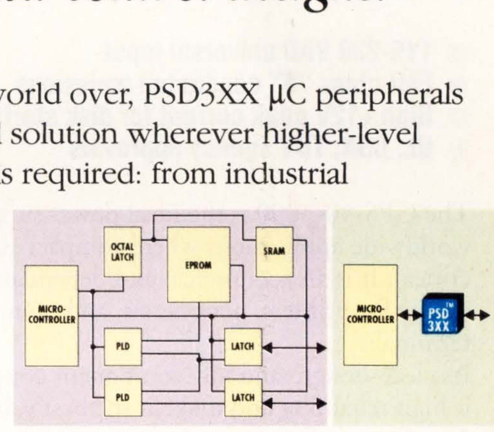

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8- and 16-bit microcontrollers

The 16-bit-μC world seems to be gaining ground with new, more powerful processors. Fitting in between the 8- and 32-bit worlds, the 16-bit chips are tunneling into applications that need higher processing power but can't pay the cost of 32-bit processing. Helping this trend is an industry shift to high-level languages like C to increase both the portability and maintainability of code. The larger memories and program stacks of 16-bit processors make them more suitable than 8-bit μCs for running C programs. EDN

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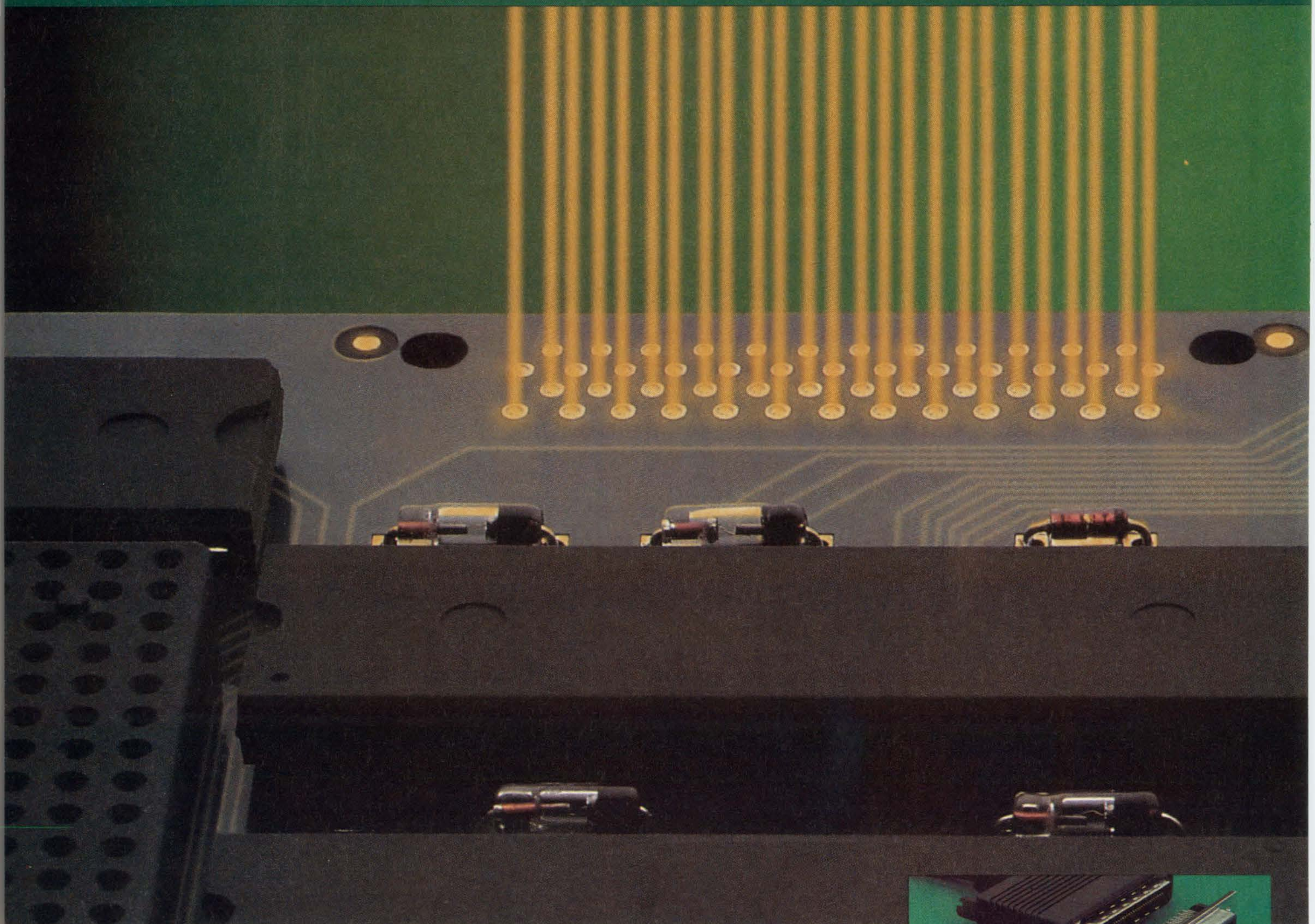

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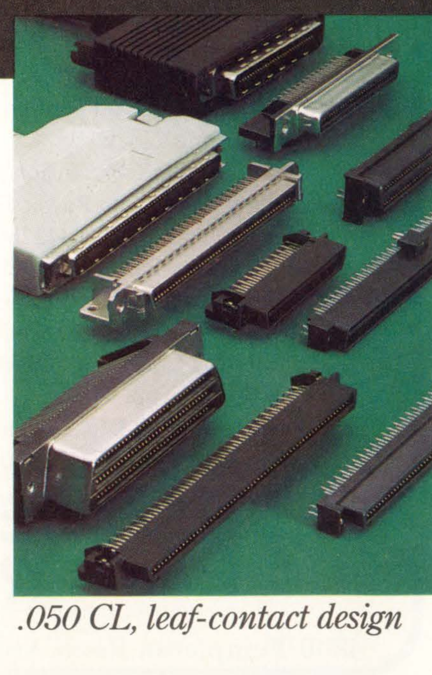

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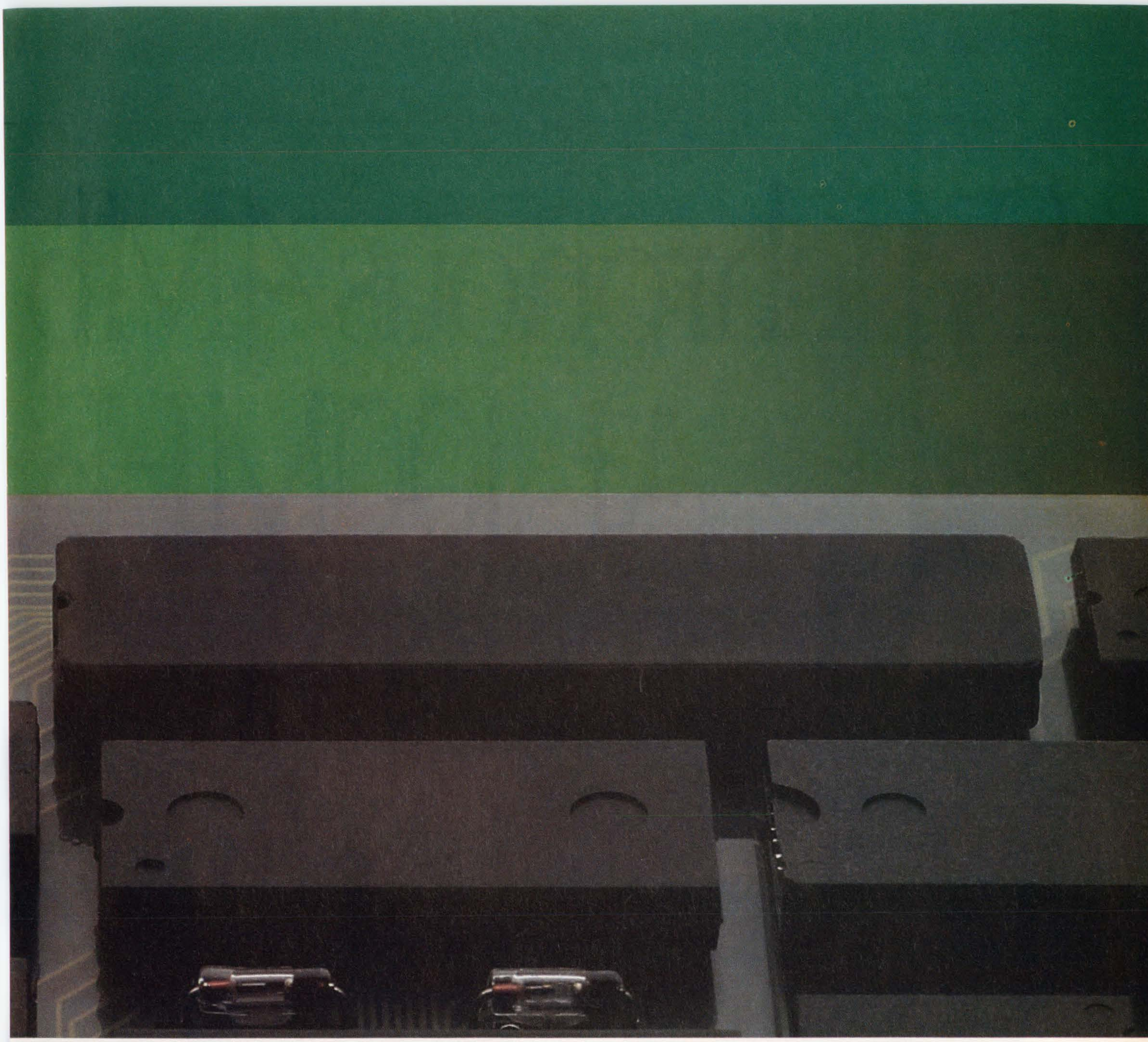

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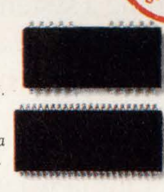

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Fuzzy-logic basics: intuitive rules replace complex math

David I Brubaker, The Huntington Group

Although "fuzzy logic" may seem to imply imprecision, it's based on a reliable and rigorous discipline. Fuzzy logic lets you accurately describe control systems in words instead of complicated math.

Fuzzy logic, based on fuzzy set theory, allows you to express the operational and control laws of a system linguistically—in words. Although such an approach might seem inadequate, it can actually be superior to (and much easier than) a more mathematical approach. The main strength of fuzzy set theory, a generalization of classical set theory, is that it excels in dealing with imprecision.

In classical set theory, an item is either a part of a set or not. There is no in-between; there are no partial members. For example, a cat is a member of the set of mammals, and a frog is not. Such sets are called crisp sets.

Fuzzy set theory recognizes that very few crisp sets actually exist. The crisp set of mammals, for example, encounters a problem with the platypus. We have to consider the platypus a full member of the set, even though it has a duck-like bill and lays eggs. Fuzzy set theory doesn't have to deal with such exceptions (or with a number of paradoxes that arise from the strict member/nonmember dichotomy).

Fuzzy logic allows partial set membership; it allows gradual transitions between being fully a member of the set and fully not a member of the set. Being partially a member of a given set, a given element is also partially not a member of that set.

Because fuzzy set theory allows both full membership and full nonmembership (although not simultaneously), it is a generalization of classical set theory. You can actually use fuzzy logic to implement crisp systems, although there is little reason to. Most of the action in fuzzy systems occurs in the transitions—the partial-membership regions of a set.

Traditional logic recognizes only full or null membership in a set and requires that a given assertion be either true or false. Fuzzy logic, however, allows partial truth and partial falseness. **Fig 1** illustrates the difference.

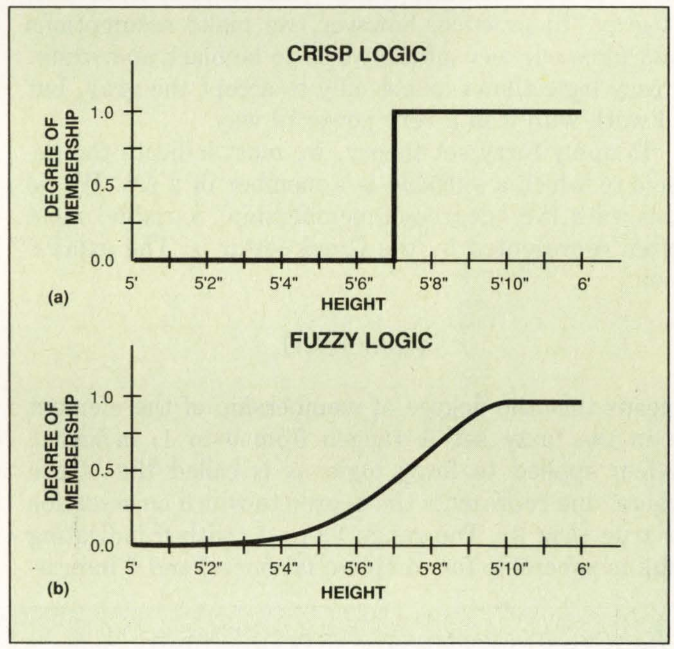


Fig 1—In traditional logic (a), a woman is either a member of the set TALL WOMEN or not, and a mere fraction of an inch can make the difference. Fuzzy logic (b) allows partial set membership that is characterized by a gradual transition from not tall to tall.

In classical set theory, we may ask whether Mary, a woman who is 5 ft, 8 in. tall, belongs to the set of tall women. In logic, we ask whether the statement "Mary is a tall woman" is true or false; using bilevel logic, we must select one or the other. If we say that Mary is tall, would she still be tall if she were a quarter inch shorter? Or half an inch shorter?

Fuzzy logic allows the statement "Mary is tall" to have a range of truthfulness, depending on Mary's height. If Mary is 5 ft even, the assertion that she is tall is completely false, but if she is 6 ft even, the assertion is completely true. If she is 5 ft, 8 in. tall, the assertion may be 75% true.

Working with this premise—that the path from truth to falseness may be gradual (and also, implicitly, that something can be simultaneously partially true and partially false)—requires a new mindset, especially for Western engineers. In principle, we agree that the world is not black and white—that most of it, in fact, is gray. In practice, however, we make assumptions and force our view of the world to be black and white. Fuzzy logic allows us not only to accept the gray, but to work with it in a very powerful way.

To apply fuzzy set theory, we must indicate the *degree* to which a variable is a member of a set. We do this with the "degree-of-membership" variable, most often represented by the Greek letter μ. The expression

$$\mu_A(x) \rightarrow [0,1]$$

means that the degree of membership of the element x in the fuzzy set A ranges from 0 to 1, inclusive. When applied to fuzzy logic, μ is called the "truth value" and represents the degree to which an assertion is true **(Fig 2)**. The range $0 \leq \mu \leq 1$, with 0 indicating null membership (or complete falseness) and 1 indicating full membership (or complete truth) is consistent with notation used in traditional bilevel logic.

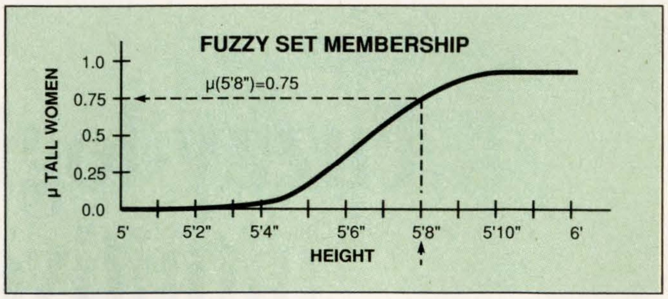


Fig 2—The degree to which an element is a member of a fuzzy set, denoted μ, can range from 0 (null membership) to 1 (full membership). In this example, a woman 5 ft, 8 in. tall has a degree of membership in the set TALL WOMEN of 0.75.

Just as bilevel logic has logical operators for combining logic variables, so does fuzzy logic. Variables in the two logic systems necessarily have different definitions, but they use the same operators: AND, OR, and NOT. The definitions most commonly used are those proposed by Lotfi Zadeh, the creator of fuzzy logic (see **box**, "Fuzzy perspective").

The AND of two fuzzy-logic variables, by Zadeh's definition, is the minimum truth value. That is, for fuzzy variables A and B,

$$\mu_{(A \text{ AND } B)} = \min(\mu_A, \mu_B).$$

The OR of two fuzzy-logic variables is the maximum truth value. Again, for fuzzy variables A and B,

$$\mu_{(A \text{ OR } B)} = \max(\mu_A, \mu_B).$$

The NOT of a fuzzy logic variable is given by

$$\mu_{(\text{NOT } A)} = 1 - \mu_A.$$

Fuzzy perspective

Fuzzy set theory was "created" by Lotfi Zadeh in 1965 and is based on work in multivalued logic by a number of mathematicians earlier in the century. Zadeh was, and is, a professor of electrical engineering and computer science at the University of California, Berkeley.

In his work with complex, nonlinear systems, Zadeh observed that the more complex a system becomes, the less meaningful are low-level details in describing overall system operation. The drive for precision in complex-system description actually becomes a stumbling block; precision often is not only unnecessary, but counterproductive. One of Zadeh's basic assumptions is that a system's operational and control laws can be expressed linguistically—in words.

Fuzzy logic is itself not "fuzzy," but a rigorous mathematical discipline. Neither is it merely another way of looking at probability theory, although both disciplines deal with uncertainty. Probability theory deals with the uncertainty that results from random behavior, whereas fuzzy theory addresses the uncertainty resulting from boundary conditions. The two disciplines are complementary in that there can be (and are) fuzzy stochastic systems, but one does not replace or eliminate the need for the other.

All three of these operators are equivalent to their respective counterparts in bilevel logic for μ limited to 0 and 1.

Plain words replace complex math

In order to work more easily with systems that are too complex to model accurately with mathematics, fuzzy logic resorts to linguistic variables. It is very difficult to express mathematically even the basic control laws involved in driving a car, say, but a verbal description of how to drive—that is, how to react to the various situations that are presented to the driver—is actually quite simple. Any such description, however, must necessarily use imprecise terms such as fast, slow, hard, and soft. (The latter two, for example, describe how much to apply either the accelerator or the brake.)

Fuzzy-set theory accommodates such imprecise terms. For example, the linguistic variable SPEED

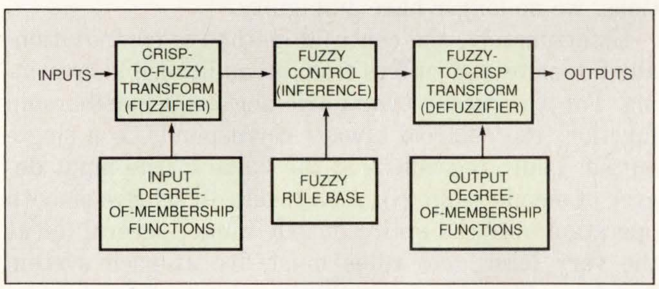


Fig 3—A fuzzy rule-based system has three major components. First, a crisp-to-fuzzy transform changes crisp inputs into degrees of membership, or truth values. Next, an inference mechanism determines actions to take by applying the truth values as conditions to rules. Finally, a fuzzy-to-crisp transform converts fuzzy actions into crisp actions and combines them to form a single, executable action.

might have as values (among others) the fuzzy sets VERY SLOW, SLOW, MEDIUM FAST, FAST, and VERY FAST. It will also have as a value the crisp set STOPPED.

A degree-of-membership function represents each of the fuzzy sets and acts as a transform between the crisp real world and our fuzzy view of the real world. For example, a SPEED of 70 mph may have degrees of membership in each of the fuzzy sets:

$$\mu_{\text{VERY SLOW}}(70\text{ mph})=0$$
$$\mu_{\text{SLOW}}(70\text{ mph})=0$$
$$\mu_{\text{MEDIUM FAST}}(70\text{ mph})=0.3$$
$$\mu_{\text{FAST}}(70\text{ mph})=0.8$$
$$\mu_{\text{VERY FAST}}(70\text{ mph})=0.4.$$

In fuzzy-logic control algorithms, degrees of membership serve as inputs. The determination of appropri-

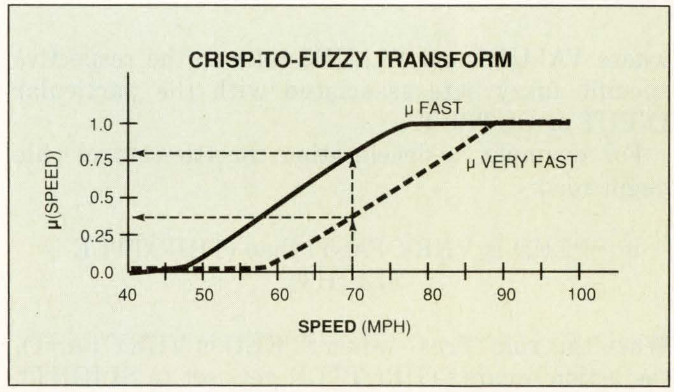


Fig 4—Degree-of-membership functions transform crisp inputs into fuzzy degrees of membership. Here, a speed of 70 mph has membership in the fuzzy set FAST with μ=0.80 and in the set VERY FAST with μ=0.38.

ate degree-of-membership functions is part of the design process.

The rule-based system is currently the most popular application of fuzzy logic. Its basic structure (**Fig 3**) has three major sections: a crisp-to-fuzzy transform ("fuzzifier"), an inference mechanism that employs rules, and a fuzzy-to-crisp transform ("defuzzifier").

In using such a system, we transform into a fuzzy domain, manipulate the data, and transform back into the crisp domain. This approach is analogous to working in the frequency domain on transformed time-domain data. Because the necessary processing is easier in the frequency domain than it is in the time domain, processing time-domain data warrants the expense of an FFT and an inverse FFT. In a fuzzy system, the base of rules describing system operation *in fuzzy terms* is easy to work with. Consequently, we transform crisp inputs and outputs into a fuzzy domain of intuitive, linguistic rules rather than transforming fuzzy rules into the crisp domain.

As indicated in **Fig 4**, the crisp-to-fuzzy transform is a mapping of an actual crisp value to a degree of membership via an input degree-of-membership function. The resulting degree of membership then becomes an input to the next system block, the inference mechanism.

In the inference mechanism, inputs and truth values serve as conditions for the rules that make up the rule base. At regular intervals, the fuzzy controller samples inputs and applies them to the rule base, resulting in appropriate system outputs. Theoretically, the rule base should cover all possible combinations of input values, but such coverage is typically neither practical nor necessary.

The general form of each rule is:

if (INPUT is VALUE1) then (ACTION is VALUE2), where VALUE1 and VALUE2 refer to the respective specific fuzzy sets associated with the particular INPUT or OUTPUT.

For example, a deceleration throttle-control rule might read:

if (SPEED is VERY FAST) then (THROTTLE is SLIGHT).

When this rule "fires" (when SPEED is VERY FAST), the action occurs (THROTTLE gets set to SLIGHT). In contrast with other rule-based systems, the action occurs only to the degree that the input is true. If SPEED is VERY FAST with $\mu = 0.25$, then THROTTLE gets set to SLIGHT also with $\mu = 0.25$. This partial setting to SLIGHT occurs in a step that performs combination and defuzzification.

Four ways to defuzzify

A method of combining actions is necessary because more than one rule may fire for any given set of inputs. In addition, the resulting single action (combined from the actions of triggered rules) must be transformed from a fuzzy value to a crisp, executable value. There are currently four popular combination/defuzzification techniques.

The maximizer technique takes the maximum degree-of-membership value from the various triggered rules and performs the corresponding single action. If, for example, as a result of three rules having fired, the THROTTLE mentioned above has

$$\mu_{\mathrm{SLIGHT}} = 0.75,$$
$$\mu_{\mathrm{SLIGHT}} = 0.40,$$
$$\mu_{\mathrm{MEDIUM}} = 0.20,$$

then the throttle setting associated with $\mu_{\mathrm{SLIGHT}} = 0.75$ will result, because 0.75 is greater than the other two values of μ. If two actions have the same μ value, and that value is the maximum μ, then some form of conflict resolution is necessary. One possibility is to use an average of the corresponding outputs; another is to select the action associated with a rule's position in the rule base.

The maximizer technique is the simplest combination/defuzzification approach, but it ignores potentially important actions. Another technique, the weighted-average method, averages the various actions after assigning weights based on degree-of-membership values. Although conceptually strong and not computationally demanding, this approach suffers from ambiguity in the output function, as does the maximizer method.

Ambiguity arises because an output degree-of-membership function can specify more than one output value for a given value of μ. An output membership function typically is shaped like a pyramid or a truncated pyramid. If $\mu = 0.5$, the output value can come from the function's rising or falling edge. Worse yet, for a truncated pyramid, $\mu = 1.0$ corresponds to a whole range of values.

It is possible to eliminate ambiguity by mapping output-function components through the specific rules back to input functions. The procedure is tedious, however, and disallows the use of negated input functions as rule conditions. (For example, we could not say "if (SPEED is NOT FAST)".)

The centroid method, illustrated in **Fig 5**, results in an output action that is associated with the center of mass of the active rule outputs. Because we are no longer using the edges of degree-of-membership functions, we no longer have ambiguity.

Unfortunately, the centroid method is computationally intensive and suffers from an additional shortcoming. For a vertically symmetric degree-of-membership function, the centroid always corresponds to a single output value, regardless of the value of the input degree of membership (μ). As a result, to achieve smooth operation over the entire output range, several (or at the very least two) rules must fire at each system iteration. In order for multiple rules to fire at once, input degree-of-membership functions must overlap. Despite these shortcomings, the centroid method is currently the best technique for combination and de-

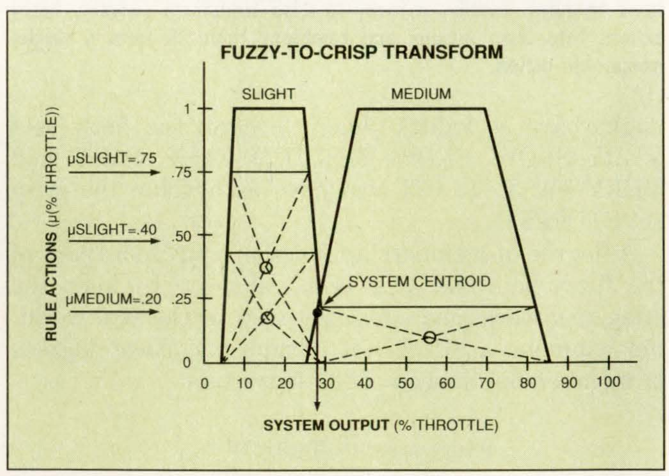


Fig 5—The centroid method combines several fuzzy output actions to form a single executable action. This single output is a weighted average of the centroids of each active degree-of-membership function. This example shows three active rule actions, specifying SLIGHT throttle twice ($\mu = 0.75$ and $\mu = 0.40$) and MEDIUM throttle once ($\mu = 0.20$). Function centroids are marked with small circles. The resulting output is a throttle setting of 29% full throttle.

fuzzification that available fuzzy-logic tools support.

The remaining combination/defuzzification method, the singleton technique, is a special case of the centroid method. This technique represents each fuzzy output set as a single output value by using a weighted average to combine multiple actions. This approach requires much less computation than the centroid method, but it still requires overlapping input functions to avoid discontinuities in the output. Because of its conceptual and computational simplicity—and unless someone develops a new and more powerful technique—the singleton method will probably replace the centroid method as the most common output technique.

Fuzzy feedback controllers

You can sample selected outputs of a fuzzy system and use them as inputs to make a feedback controller (**Fig 6**). A fuzzy system fuzzifies inputs, which then serve as conditions to the rule base. The rule base operates on those inputs, then it combines and defuzzifies actions from triggered rules to produce one or more controller outputs.

Increasingly, fuzzy rule-based systems use adaptive techniques—neural nets and genetic algorithms, for example—to refine degree-of-membership functions and even the actual rule bases. In addition, fuzzy decision systems that do not use a rule base are beginning to use fuzzy (rather than crisp) inputs to make predictions from vague and incomplete data.

Fuzzy logic has been applied to many different and diverse applications. These include categorization of weather patterns and of sea gull behavior; control of cement kilns, passenger trains, and elevators; scheduling of subway trains and service technicians; and making predictions in risk management.

Fuzzy logic systems are often superior to alternate approaches in five general areas:

- *In complex systems where an adequate system model is difficult or impossible to define*
- *In systems normally controlled by a human expert*
- *In systems that have moderately to very complex continuous (or semicontinuous) inputs and outputs and a nonlinear response function*
- *In systems that use human observations as control rules or inputs*
- *In systems where vagueness is common; for example, in economic systems, natural sciences, and behavioral sciences.*

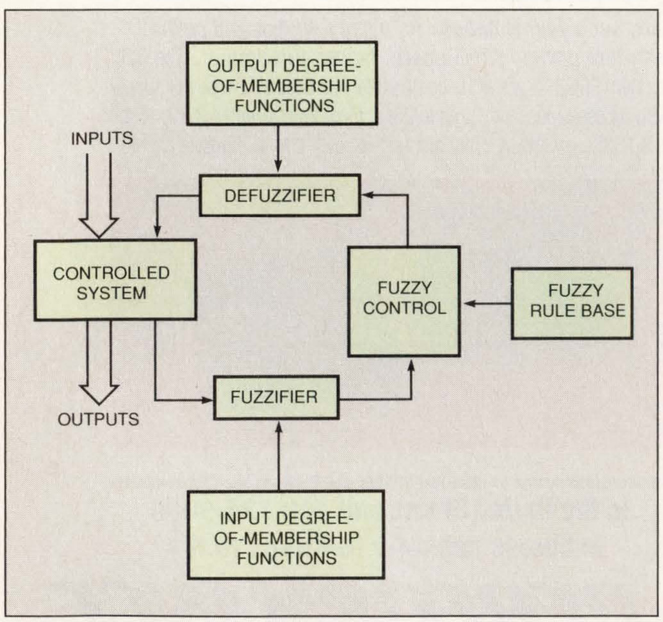
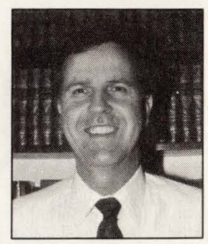


Fig 6—In a fuzzy feedback controller, selected sampled outputs serve as inputs. Modeling is unnecessary, even with nonlinear systems, as long as the response function is describable in words.

Author's biography



David Brubaker is president of The Huntington Group, consultants in the design of systems using real-time embedded processors and fuzzy logic. He has worked with Sun Microsystems, Beckman Instruments, Motorola, TRW, Ford, and ESL. David holds BS, MS, and PhD degrees, all in electrical engineering, from Stanford University. His personal activities include walking, backpacking, and coaching his children's basketball teams.

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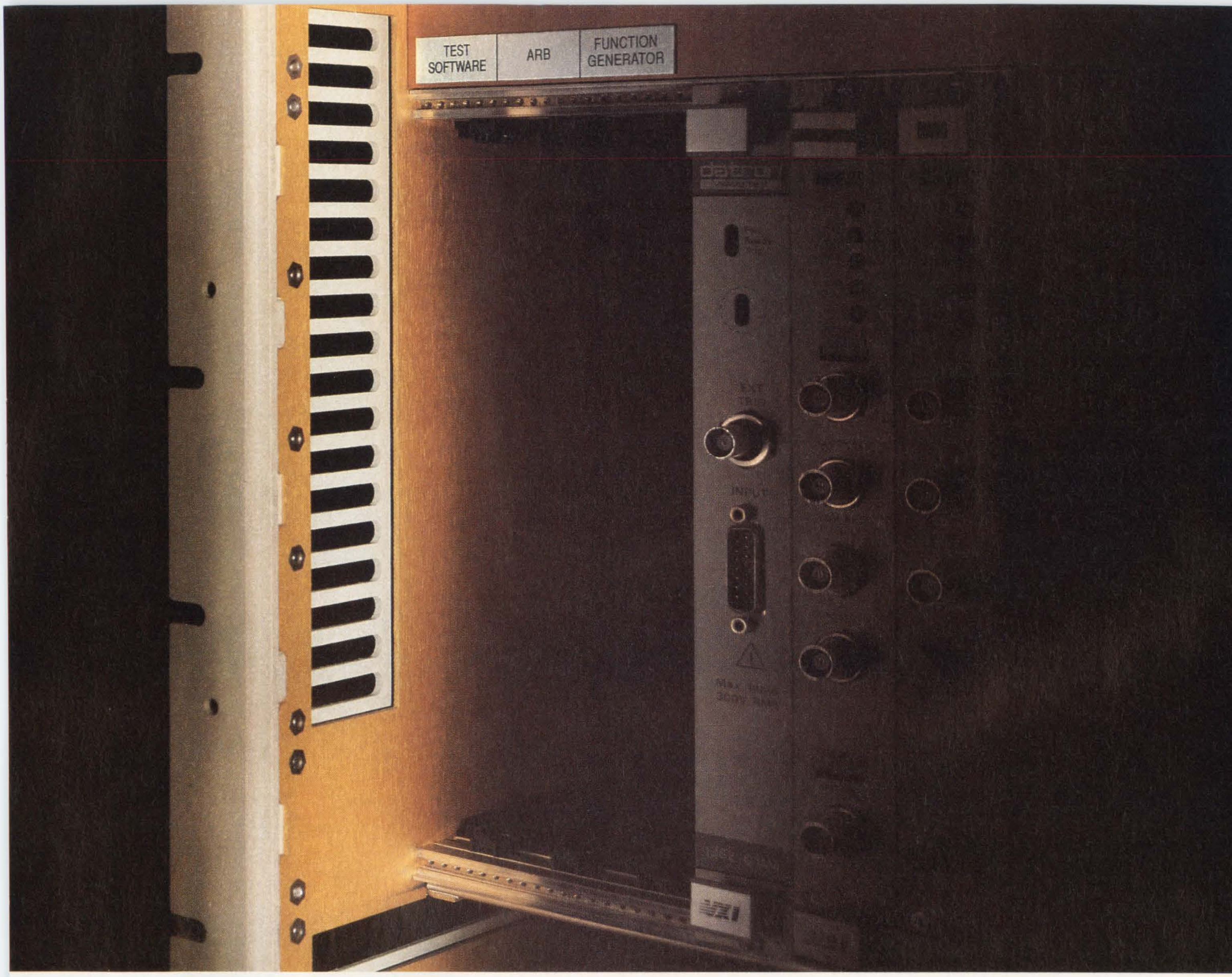
Interested in more information on fuzzy logic?

Turn to pg 121 in this issue for more information on fuzzy logic. The practical steps outlined in the next article show how to design a simple fuzzy-logic system.

We continue our special coverage of fuzzy logic in the July 6, 1992, issue of EDN, which will feature a staff-written article on software tools used for fuzzy-logic design.



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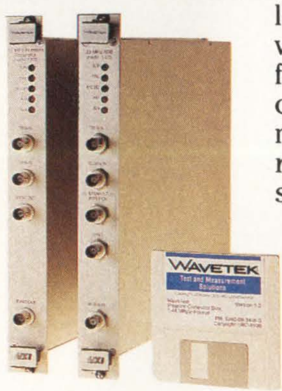

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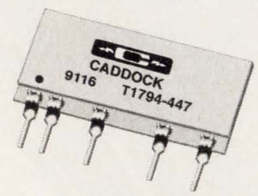

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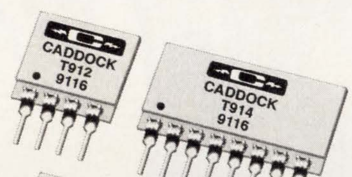

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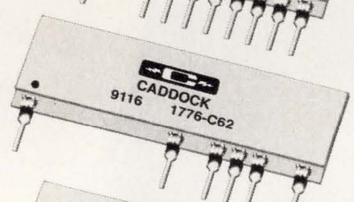

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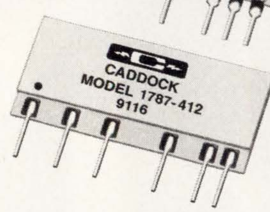

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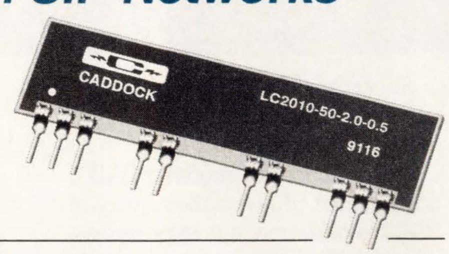

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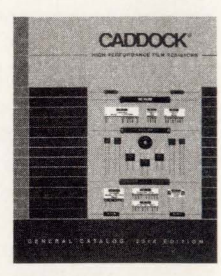

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CIRCLE NO. 73

Fuzzy-logic system solves control problem

David I Brubaker, The Huntington Group, and Cedric Sheerer, C/S Associates

Complex, nonlinear control problems can yield to simple fuzzy-logic techniques that require no modeling. Although fuzzy logic does not produce an analytic solution, you can verify the solution's validity using simulation.

You can use fuzzy logic to control a complex system. The practical steps in the following sample problem show how to design a simple fuzzy-logic system, in this case, a system that controls a traffic light for a freeway's on ramp. The traffic light will automatically control the traffic flow onto a freeway (**Fig 1**). The design goal is to minimize the impact of the inflow traffic on the prevailing freeway traffic.

Currently, on northern California freeways, a red-and-green traffic light meters on-ramp traffic. The traffic light has a constant green-to-red cycle. An accompanying sign states that a single vehicle is allowed onto the freeway for each green light. A fixed timer switches metering on automatically during periods that usually have heavy traffic—typically during commuting times.

For our design, we would like to add a bit of complexity—and hopefully capability—to the system. First, we will allow the delay between green lights to depend on the prevailing freeway traffic's speed and density: The delay increases for higher traffic density and decreases for higher freeway speed. And second, by controlling the length of time the green light is active, we will allow potentially more than one car onto the freeway during each green light. A standard traffic light, having green, yellow, and red lights, will perform the metering.

The system will be fuzzy; that is, it will continuously monitor the inputs and from them determine appropriate output responses based on rules stated in words—or, more formally, linguistically stated control criteria. Although the fuzzy system will make its decisions based on these rules, the system is not an abstruse "natural-language" artificial-intelligence system. Just like any other control system, the fuzzy system will take in numeric inputs from its sensors and output numeric data to control the traffic light.

Is a fuzzy system appropriate for this application? Or, more to the point, would you use a fuzzy approach for traffic metering outside this tutorial setting on a real freeway?

For several reasons, the answer is yes. Although an on-ramp metering system seems on the surface to be simple, the system is actually quite complex and, to a great degree, nonlinear. The behavior of human drivers tends to be nonlinear but also fairly predictable and, therefore, not random.

This nonlinear physical system is difficult to model mathematically, but you can easily express the sys-

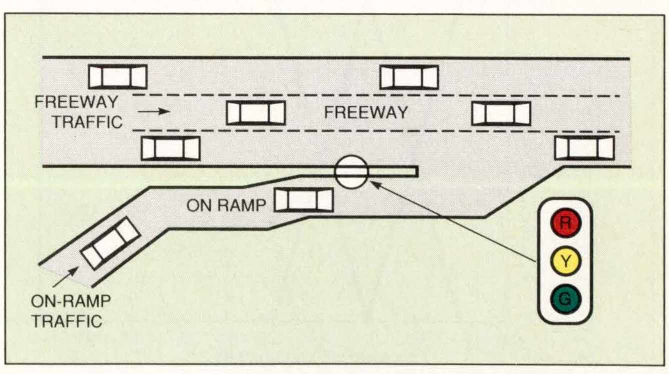

Fig 1—The fuzzy-logic system in this article will control the flow of cars from an on ramp onto a busy freeway by cycling a traffic light according to the freeway traffic's density and speed.

tem's operation in linguistic rules using fuzzy variables. You can also accomplish any needed subsequent modifications to the system quite simply.

System design

As is the case with designing many complex, non-modeled systems, designing a fuzzy rule-based system is largely a seat-of-the-pants job. Recognizing the lack of a formal procedure, this example uses the following four steps:

1. Identify system inputs and those inputs' fuzzy ranges and establish degree-of-membership (or truth-value) functions for each range.
2. Identify outputs and those outputs' fuzzy ranges, again including the degree-of-membership functions.
3. Identify the rules that map the inputs to the outputs.
4. Determine the method of combining fuzzy rule actions into executable, "crisp" system outputs.

The system has two inputs: SPEED—the current average speed of the freeway traffic, and DENSITY—the current average density of the freeway traffic. In the real world these two inputs are somewhat tightly linked: Density tends to decrease as freeway speed increases because drivers allow greater separations between themselves and the car in front. However, we shall treat the two inputs separately.

Each input can assume a number of linguistic values, each value represented by a fuzzy set. To the fuzzy variable DENSITY we'll assign three fuzzy values (**Fig 2**): HEAVY—separation between cars is minimal, MEDIUM_HEAVY—separation between cars is nominal, and LIGHT—Separation between cars is maximum.

The fuzzy variable SPEED will also have three fuzzy values: SLOW—traffic is moving slowly, MEDIUM_FAST—traffic is moving at a nominal velocity below the speed limit, and FAST—traffic is moving at or above the speed limit.

We must deal finally with numbers—the linguistic values suggested have no quantitative meaning. **Fig 2** shows the degree-of-membership functions associated with the two inputs. Each linguistic fuzzy value has a corresponding fuzzy set. The shape of the fuzzy set determines its degree-of-membership, or "truth-value," function. Notice, for example, that the speed of 15 mph has a degree of membership of about 0.40 in both the SLOW and MEDIUM_FAST fuzzy sets. We arrived at the fuzzy sets in **Fig 2** arbitrarily, although an inherent requirement of a linguistically represented system is that the values be intuitively valid.

Identify system outputs

The system will have two outputs:

1. GREENLIGHT—The duration of the green-light state, in seconds, during which cars may enter onto the freeway.
2. REDLIGHT—The duration of the red-light state, also in seconds (which will include a constant-period yellow-light state), during which on-ramp cars may not enter onto the freeway.

Three fuzzy values apiece handle the two output variables nearly identically: SHORT—the given light is on only a short time, MEDIUM_LONG—the given light is on a medium period of time, LONG—the given light is left on for a long period of time. **Fig 3** shows the membership functions of these fuzzy values, as functions of time (seconds). In addition to these values, GREENLIGHT must have one additional (and crisp) value: CONSTANT_ON—the green light is on continuously.

After assigning input and output values to defined

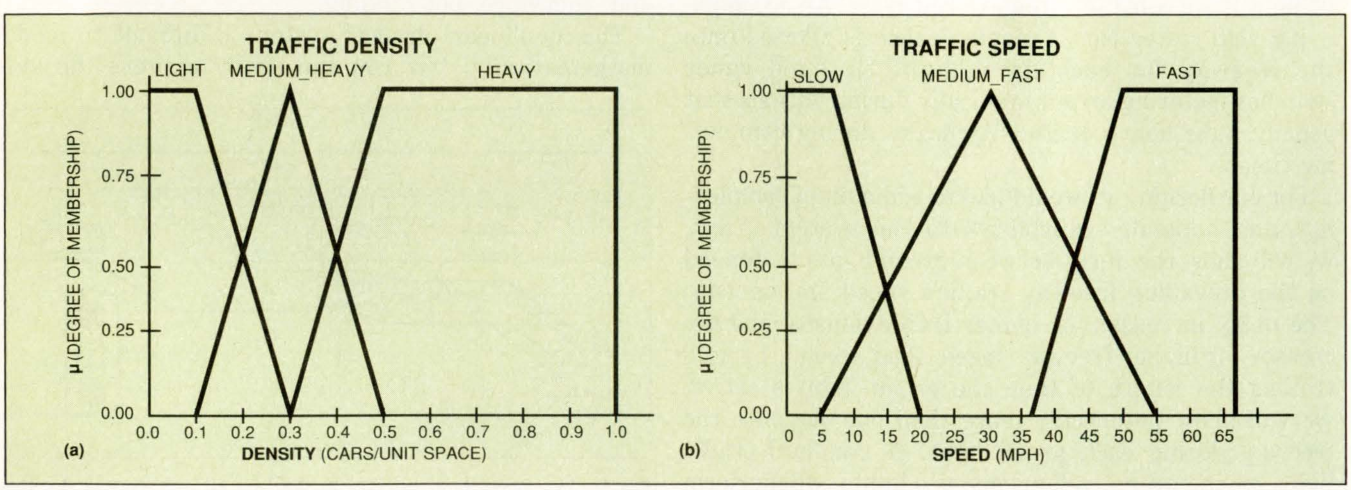

Fig 2—The degree-of-membership functions for the two system inputs, DENSITY (a) and SPEED (b), transform the measured (crisp) inputs into degrees of membership in fuzzy sets.

fuzzy sets, we must map each of the possible nine input conditions to an output. You do this mapping through the rule base. The most common form of expression for rules is linguistic:

if (condition or antecedent) then (action or consequence).

For example,

if (DENSITY is HEAVY and SPEED is SLOW) then (GREENLIGHT is SHORT, REDLIGHT is LONG).

You must keep in mind the heart of a fuzzy rule-based system: the *degree* to which the actions are executed corresponds directly to the *degree* to which the respective input conditions are true. The "AND" operator in the statement of the condition is a fuzzy AND, not a Boolean AND. The fuzzy AND means that the lesser value of the two degree-of-membership functions gets taken.

Continuing in this manner completes the rule base. A more compact form, and one that ensures we have covered all condition combinations, is the matrix representation. **Fig 4** shows both a list of rules and equivalent matrices for the metering-light rule base.

Several techniques exist for combining fuzzy actions into a single, crisp output. The fuzzy development and simulation program we used to verify this design supports only one: the centroid technique. The centroid technique, incidentally, is currently the most popular technique.

In making our first go at the design, we implemented the system using Hyperlogic's Cubicalc fuzzy tool and a simulator. The simulator provided a range of densities of simulated freeway traffic and several speed ranges for each density as inputs to the system. Resulting simulated outputs are the length of delay for each red light (that is, delay between green lights) and the number of cars allowed through for each green light.

To show how the fuzzy inference mechanism works, we'll step through a single iteration. The concept is not difficult, but the process has a number of potentially confusing steps. Refer to **Figs 5 and 6**.

We assume a traffic density of 0.35 (which trans-

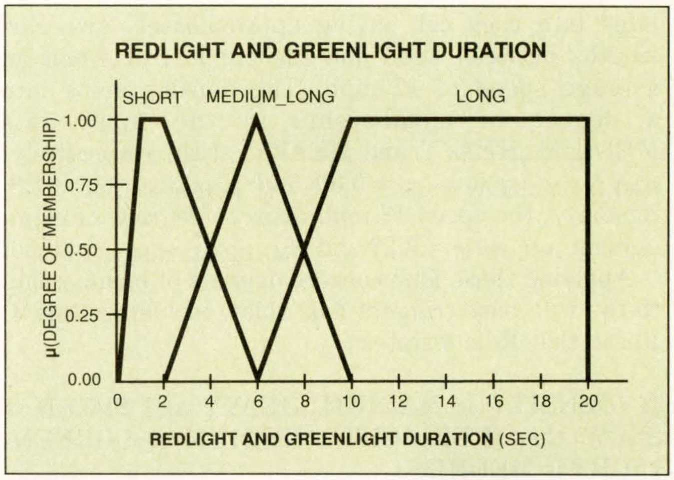

Fig 3—The degree-of-membership functions for the two system outputs, REDLIGHT and GREENLIGHT, transform the fuzzy actions that the rule base specifies back into executable (crisp) outputs.

1 if (DENSITY is HEAVY and SPEED is SLOW) then (REDLIGHT is LONG, GREENLIGHT is SHORT)
2 if (DENSITY is HEAVY and SPEED is MEDIUM_FAST) then (REDLIGHT is MEDIUM_LONG, GREENLIGHT is MEDIUM_LONG)
3 if (DENSITY is HEAVY and SPEED is FAST) then (REDLIGHT is SHORT, GREENLIGHT is LONG)
4 if (DENSITY is MEDIUM_HEAVY and SPEED is SLOW) then (REDLIGHT is MEDIUM_LONG, GREENLIGHT is MEDIUM_LONG)
5 if (DENSITY is MEDIUM_HEAVY and SPEED is MEDIUM_FAST) then (REDLIGHT is SHORT, GREENLIGHT is LONG)
6 if (DENSITY is MEDIUM_HEAVY and SPEED is FAST) then (REDLIGHT is (SHORT), GREENLIGHT is CONSTANT_ON)
7 if (DENSITY is LIGHT and SPEED is SLOW) then (REDLIGHT is SHORT, GREENLIGHT is LONG)
8 if (DENSITY is LIGHT and SPEED is MEDIUM_FAST) then (REDLIGHT is (SHORT), GREENLIGHT is CONSTANT_ON)
9 if (DENSITY is LIGHT and SPEED is FAST) then (REDLIGHT is (SHORT), GREENLIGHT is CONSTANT_ON)

(a)

REDLIGHT

DENSITY \ SPEED	SLOW	MEDIUM_FAST	FAST
LIGHT	7 (SHORT)	8 (SHORT)	9 (SHORT)
MEDIUM_HEAVY	4 MEDIUM_LONG	5 SHORT	6 (SHORT)
HEAVY	1 LONG	2 MEDIUM_LONG	3 SHORT

GREENLIGHT

DENSITY \ SPEED	SLOW	MEDIUM_FAST	FAST
LIGHT	7 CONSTANT_ON	8 CONSTANT_ON	9 CONSTANT_ON
MEDIUM_HEAVY	4 MEDIUM_LONG	5 LONG	6 CONSTANT_ON
HEAVY	1 SHORT	2 MEDIUM_LONG	3 LONG

(b)

Fig 4—You can represent the rules that relate inputs to outputs in linguistic form (a) or in matrix form (b). The rules map the various fuzzy values of the inputs DENSITY and SPEED to the outputs GREENLIGHT and REDLIGHT. Note that four SHORT values of REDLIGHT have parentheses. The parentheses indicate a don't-care state because the corresponding state for GREENLIGHT is CONSTANT_ON.

lates into each car having approximately two car-lengths between itself and the car in front) and an average speed of 17 mph. The density maps into a degree of membership in the fuzzy sets MEDIUM_HEAVY and HEAVY, with, respectively, $\mu_{MEDIUM\_HEAVY(0.35)}=0.80$ and $\mu_{HEAVY(0.35)}=0.28$. Similarly, the speed 17 mph maps to degrees of membership $\mu_{SLOW(17)}=0.22$ and $\mu_{MEDIUM\_FAST(17)}=0.50$.

Applying these four nonzero degrees of membership to the rule base triggers four rules, including Rule 4. Recall that Rule 4 states:

If (DENSITY is MEDIUM_HEAVY and SPEED is SLOW) then (REDLIGHT is MEDIUM, and GREENLIGHT is MEDIUM).

We have already determined that DENSITY is MEDIUM_HEAVY ($\mu=0.80$) and SPEED is SLOW ($\mu=0.22$). The fuzzy AND of these two expressions is the lesser of the two values, so the truth value (which, again, for our purposes is synonymous with "degree of membership") of the input condition for Rule 4 is $\mu_{CONDITION}=0.22$.

This result we apply to both output actions:

$$\mu_{MEDIUM\_LONG(REDLIGHT)} = \mu_{MEDIUM\_LONG(GREENLIGHT)}=0.22.$$

Had Rule 4 been the only rule that fired, these values would also uniquely determine the actual executed values for REDLIGHT and GREENLIGHT. However, given the two specific inputs, a total of four rules will fire: Rules 1, 2, 4, and 5. By following the same steps as we did for Rule 4, we would find that the calculated REDLIGHT and GREENLIGHT durations are (here including the Rule 4 results)

$$\mu_{LONG(REDLIGHT)} = \mu_{SHORT(GREENLIGHT)}=0.22 \quad \textbf{(Rule 1)}$$

$$\mu_{MEDIUM\_LONG(REDLIGHT)} = \mu_{MEDIUM\_LONG(GREENLIGHT)}=0.28 \quad \textbf{(Rule 2)}$$

$$\mu_{MEDIUM\_LONG(REDLIGHT)} = \mu_{MEDIUM\_LONG(GREENLIGHT)}=0.22 \quad \textbf{(Rule 4)}$$

$$\mu_{SHORT(REDLIGHT)} = \mu_{LONG(GREENLIGHT)}=0.50. \quad \textbf{(Rule 5)}$$

We must now combine and translate these results into a crisp, executable output. As **Fig 6** shows, we use the centroid technique to do so for the REDLIGHT duration. Again using Rule 4's action, the membership function of MEDIUM_LONG is sliced off at the designated truth value, $\mu=0.22$. The centroid of the resulting area is at $\text{REDLIGHT}_{\text{Rule 4}}=6$ sec.

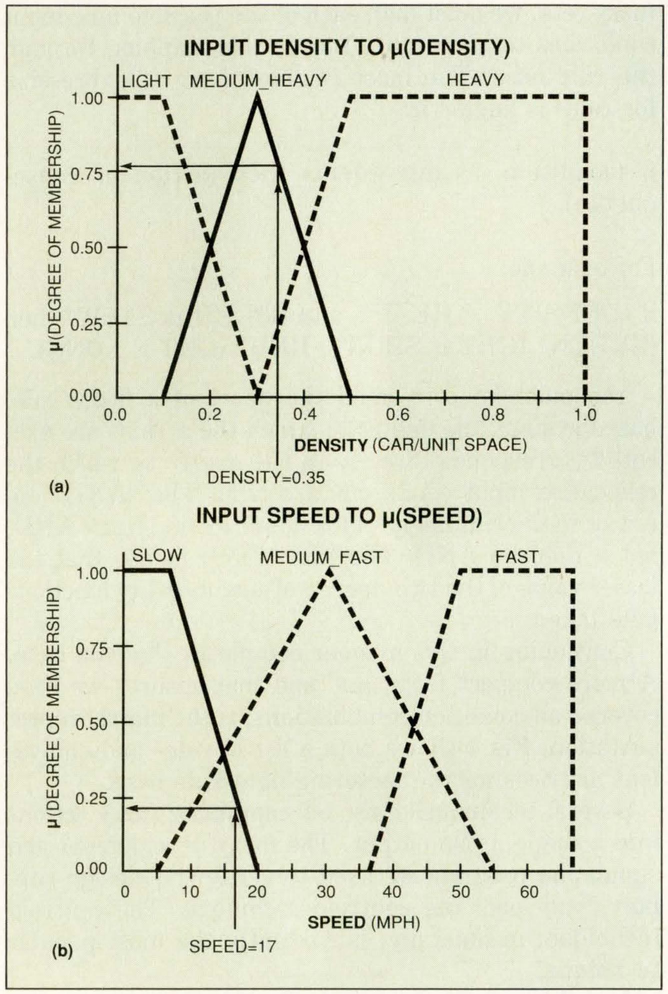

Fig 5—A traffic density of 0.35 translates into $\mu=0.80$ in the fuzzy set MEDIUM_HEAVY (a). Similarly, a traffic speed of 17 mph yields $\mu=0.22$ in the fuzzy set SLOW (b).

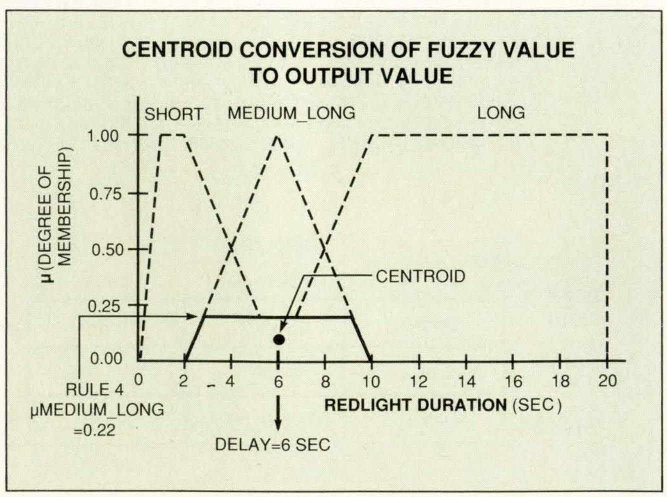

Fig 6—The centroid method of combination/defuzzification crops the fuzzy set MEDIUM_LONG at a height of 0.22—the result from Fig 5. The centroid of the resultant truncated figure is at a delay of 6 seconds.

In a similar manner, calculating the centroids for the output areas corresponding to the actions of Rules 1, 2, and 5 yields: $REDLIGHT_{Rule\ 1}=13.2$ sec, $REDLIGHT_{Rule\ 2}=6$ sec, and $REDLIGHT_{Rule\ 5}=2.75$ sec. A weighted-average method, where the weights are the respective truth values, combines all these centroids. The final output is:

$$t_{REDLIGHT}=((13.2)(0.22)+(6)(0.28)+(6)(0.22)+(2.75)(0.50))/(0.22+0.28+0.22+0.50)=5.96 \text{ seconds.}$$

Performance is pretty much as expected. For light traffic, the system allows cars onto the freeway with little or no delay and with little impact on freeway speed and density. As the number of cars on the freeway (DENSITY) increases, the number of cars allowed in from the on ramp decreases dramatically.

Obviously, the design suffers from a significant oversight. This oversight is an intentional setup; it allows for an extra modification step, and the ease of modification of fuzzy systems is important. When traffic is very dense, the system allows a bare minimum of cars, approaching zero, to enter from the on ramp. With a little thought, the reason becomes obvious. If the design goal, implicit in the rule base, is to optimize freeway density, then freeway density is least adversely affected when the system allows no cars to enter from the on ramp. Thus, while the design goal of optimizing freeway traffic flow is desirable to those already on the freeway, it would not be a popular one among the drivers stacking up on the on ramp.

System modification

We need to modify our system. The system as it stands now has a natural correctional feedback (drivers wanting to enter onto the freeway that see an overly long line at the on ramp will tend to look for an alternate route), but it is minimally effective. To improve on the design, we must include another input and a corresponding additional set of rules to balance the "minimal impact on freeway density" goal with a "minimal number of cars on the on ramp" goal.

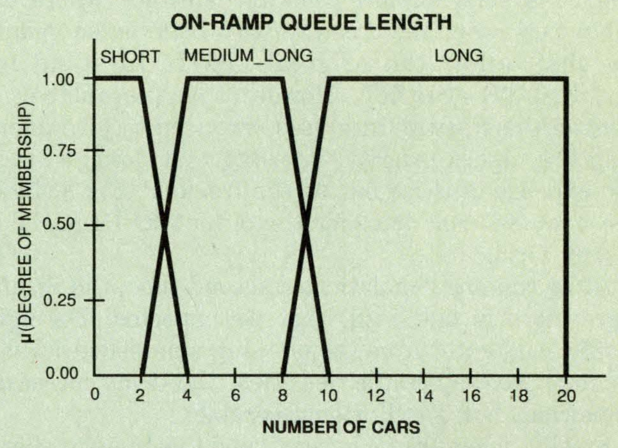

Fig 7—Simulations reveal that the rules in Fig 4 will allow no cars onto the freeway if the prevailing traffic is heavy. Having added these Q_LENGTH fuzzy sets and modified the rule base, the system will now attempt to balance the need to optimize freeway-traffic density with the need to minimize on-ramp queue length.

The input we'll add is the number of cars currently on the ramp waiting to be metered onto the freeway—call it Q_LENGTH. As with the other inputs, Q_LENGTH is a fuzzy variable and comprises three fuzzy values, each with its own degree of membership function: SHORT—a few cars are on the on ramp, MEDIUM_LONG—a moderate number of cars are on the on ramp, and LONG—many cars are on the on ramp. **Fig 7** shows these functions.

Adding Q_LENGTH to the rule base adds a third dimension to the original matrix. Because the original

Fuzzy logic evinces interest from US engineers

Even a year ago, fuzzy-logic practitioners, recognizing the highly publicized successes in Japan, were bemoaning US companies' utter lack of interest in fuzzy-logic systems. The Western engineering community, caught up in the need for precision that has been evident as far back as Aristotle, was incapable of appreciating—much less applying—fuzzy logic. The term "fuzzy" itself was an encumbrance, part of an overall psychological barrier that embodied a distrust of anything imprecise.

This situation is changing rapidly. The Japanese still dominate in fuzzy applications, but American engineers are now starting to catch on, often through the efforts of internal individual and small-group "champions" that learned the technology, caught the spirit, and are now busy converting their colleagues and management.

The psychological barrier is coming down. And if we can keep from getting caught up in a self-defeating hype campaign, we will come to accept fuzzy logic as a viable and powerful system-design paradigm.

The bottom line is that, because fuzzy logic is a fundamental mathematical technique, there are few disciplines where you cannot apply it.

matrix is valid for low freeway densities (where on-ramp cars enter the freeway with little or no delay), we shall allow the original matrix to stand for Q_LENGTH=SHORT. However, as the number of cars on the freeway increases, we need to give queue length a higher priority, knowing that doing so is at the expense of those out on the freeway. **Fig 8** shows the new, 3-D rule base for the output REDLIGHT in matrix form.

After running simulations a second time, the results were more in line with what we expected. For light traffic, cars enter from the on ramp unimpeded. Under medium freeway-traffic densities, the delay increases somewhat, but is still not intolerable.

Finally, when traffic is heavy and the queue is short, freeway density dominates and on-ramp delays are long; for increasing queue lengths, the need to move cars onto the freeway becomes more important, and freeway density suffers. We now have a system whose operation is consistent with what we would expect to see were this system used in an actual application.

Why did we simulate the system? Currently, rule-based fuzzy systems are nonanalytic. By expanding fuzzy systems' capability to handle extremely complex and nonlinear systems, we have sacrificed the ability to analyze mathematically their correct operation and complete representation of the system being controlled. To ensure correct operation (or at least an increased comfort margin) we must simulate the system's operation. This nonanalytic approach often rankles those who are grounded in traditional, linear theory but, if done correctly, it is tested and reliable.

Porting to the real world

Several options exist to assist porting a fuzzy rule-based system to a real-world application. The first option is to develop your own fuzzy system. As you can see from the example, the basic architecture has three stages:

1. A crisp-to-fuzzy transformation of inputs.
2. Applying these fuzzy inputs as conditions to the rule base.
3. Combining the resulting actions and transforming from a fuzzy set of outputs back to executable, crisp outputs.

Actually, although developing your own system may sound involved, it is not all that difficult. The real complexity in developing a fuzzy system is in creating and testing both the degree-of-membership functions and the rule base, rather than in implementing the runtime environment.

The second porting option is to use an embedded architecture that supports DOS and utilize the runtime environments provided by the various toolmakers. Finally, both Hyperlogic and Togai Infralogic optionally provide the C source code they use in their runtime environment, which will allow cross compilation into nearly any target.

The example is conceptually straightforward. The intent of this article is not to design a traffic light but rather to demonstrate how to design a fuzzy system. You can follow the approach outlined here to develop even relatively complex fuzzy rule-based systems.

Note that at no time did we have to create a model of the physical system. The solution used linguistically stated rules describing actions that are in response to inputs. This lack of a model is the dominant strength

Q_ LENGTH is SHORT

DENSITY \ SPEED	SLOW	MEDIUM_FAST	FAST
LIGHT	(SHORT)	(SHORT)	(SHORT)
MEDIUM_ HEAVY	MEDIUM_LONG	SHORT	(SHORT)
HEAVY	LONG	MEDIUM_LONG	SHORT

Q_ LENGTH is MEDIUM_LONG

DENSITY \ SPEED	SLOW	MEDIUM_FAST	FAST
LIGHT	(SHORT)	(SHORT)	(SHORT)
MEDIUM_ HEAVY	SHORT	SHORT	(SHORT)
HEAVY	MEDIUM_LONG	SHORT	(SHORT)

Q_ LENGTH is LONG

DENSITY \ SPEED	SLOW	MEDIUM_FAST	FAST
LIGHT	(SHORT)	(SHORT)	(SHORT)
MEDIUM_ HEAVY	(SHORT)	(SHORT)	(SHORT)
HEAVY	SHORT	(SHORT)	(SHORT)

Fig 8—Compare these three matrices for REDLIGHT with the single REDLIGHT matrix in Fig 4. When the queue's length is short, the rules are the same as Fig 4's. But as the queue gets longer, the rules make the REDLIGHT interval shorter. (The GREENLIGHT interval, not shown, is the complement of the REDLIGHT interval.)

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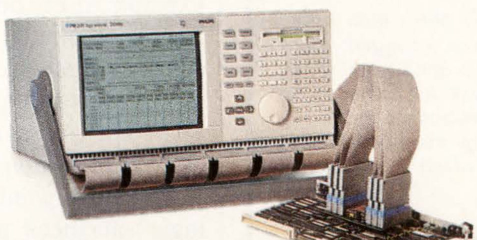

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of a fuzzy rule-based system. Using intuitive terms rather than abstract mathematical models, you can implement complex systems rapidly.

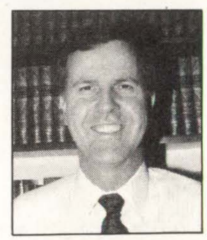
We have presented a simple fuzzy system. It demonstrates the lowest level of how to incorporate fuzzy logic into system design. Higher-level fuzzy structures can take the form of either adapting traditional, crisp-level structures or creating new structures that are achievable only with fuzzy logic.

A fuzzy solution may be the only one possible. For example, fuzzy decision and scheduling schemes handle imprecise inputs, logically combining them to provide some optimal decision or schedule. In addition, fuzzy evidence techniques allow collecting both deductive and inductive evidence in forming conclusions, again in light of incomplete or uncertain data.

One final point. Proponents often claim that fuzzy logic sacrifices precision for a more accurate "big-picture" view of the system. This is not entirely correct. Fuzzy logic does retain the high-level view of a system better, but it also only sacrifices *unnecessary* precision. If you need greater precision, you can get it from your fuzzy system by, for example, increasing the number of input and output values and accounting for input-to-output mapping through an increased number of more specific rules. EDN

To get a foundation in the basics of fuzzy logic, turn to pg 111 in this issue.

Authors' biographies



David Brubaker is president of The Huntington Group (Menlo Park, CA), consultants in the design of systems using real-time embedded processors and fuzzy logic. He has worked with Sun Microsystems, Beckman Instruments, Motorola, TRW, Ford, and ESL. David holds BS, MS, and PhD degrees, all in electrical engineering, from Stanford University. His personal activities include walking, backpacking, and coaching his children's basketball teams.

Cedric Sheerer is president of C/S Associates (Los Altos, CA). He holds degrees in both electrical engineering and business and has 23 years of experience as a software and hardware engineer and an international consultant. His professional specialties include artificial intelligence (AI), video-digital imaging, data acquisition, and algorithmic signal processing, which he has used to develop AI-based analog/digital board-level diagnostic tools.

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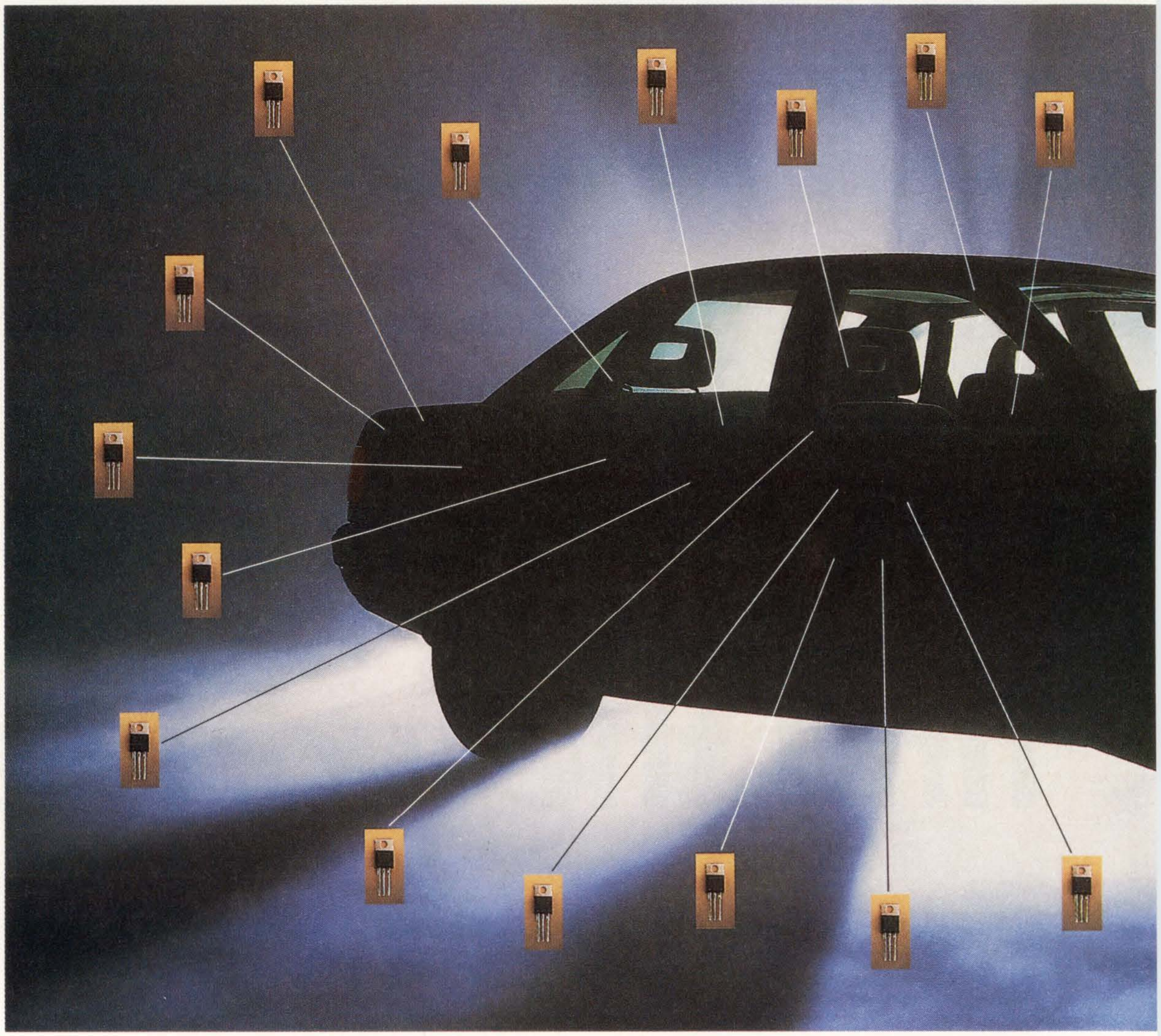

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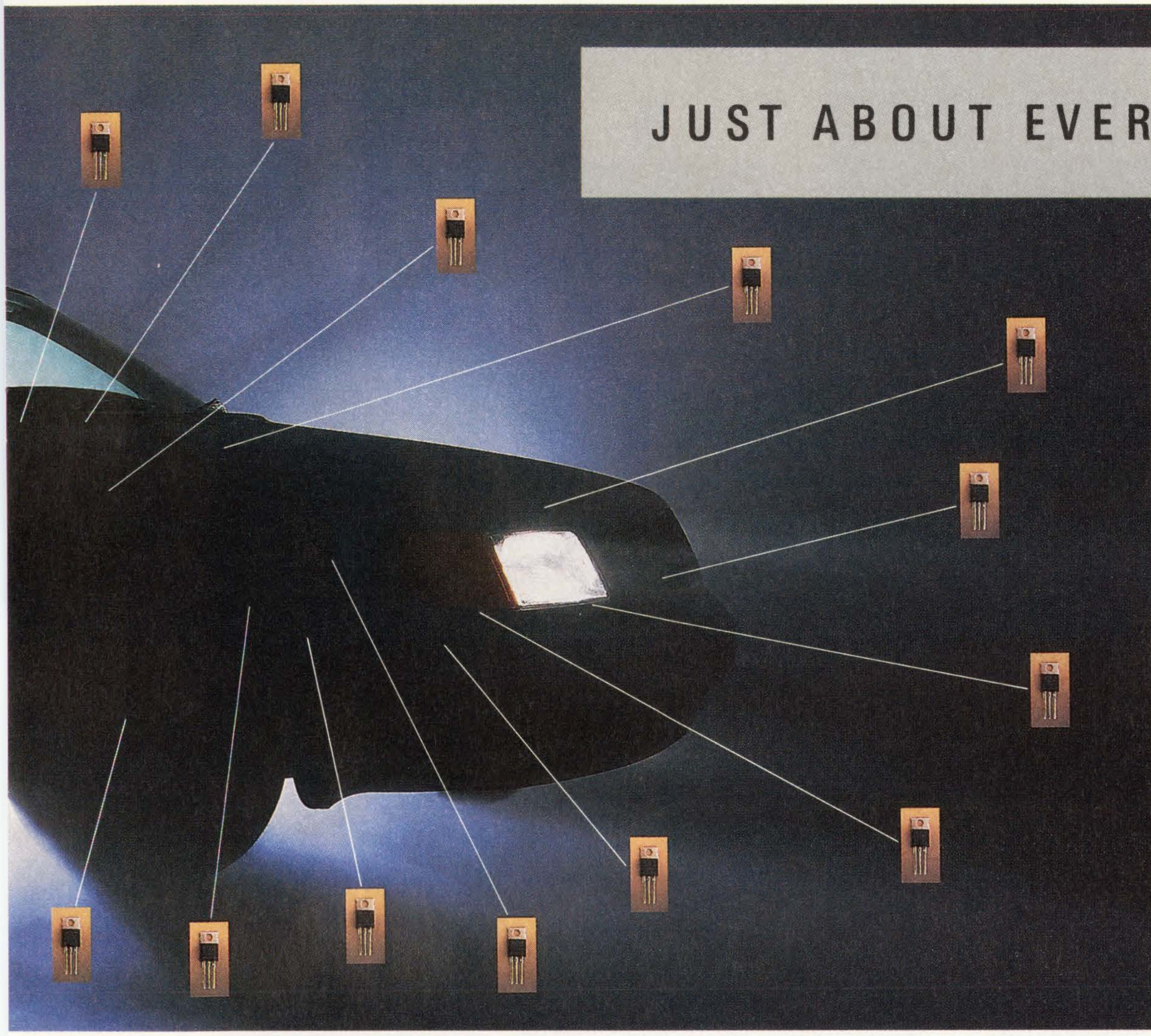

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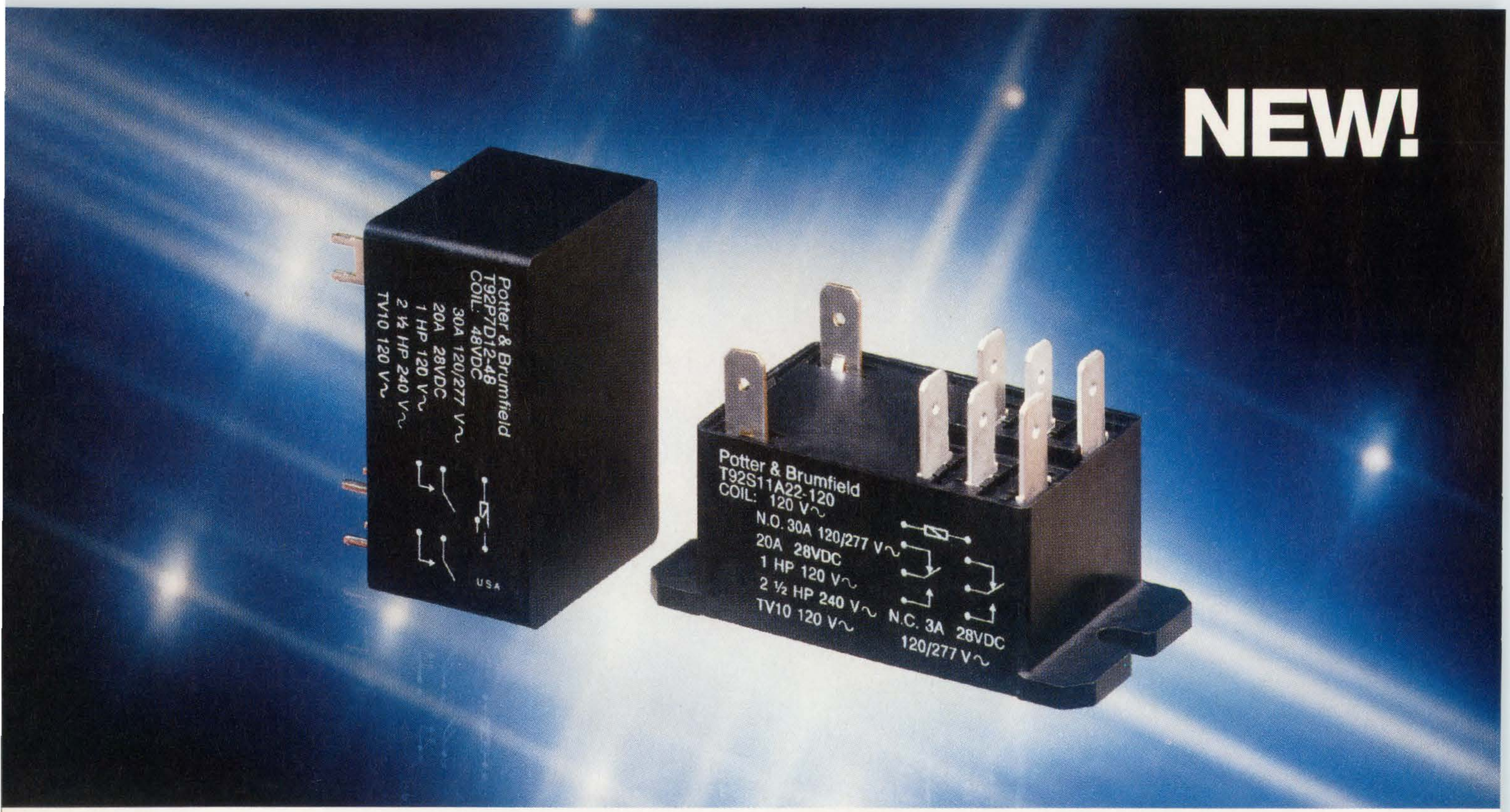

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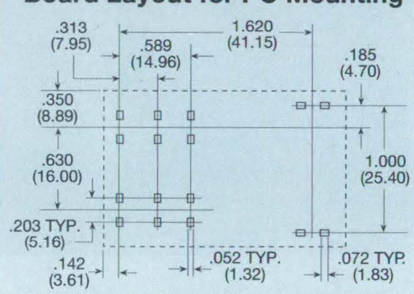

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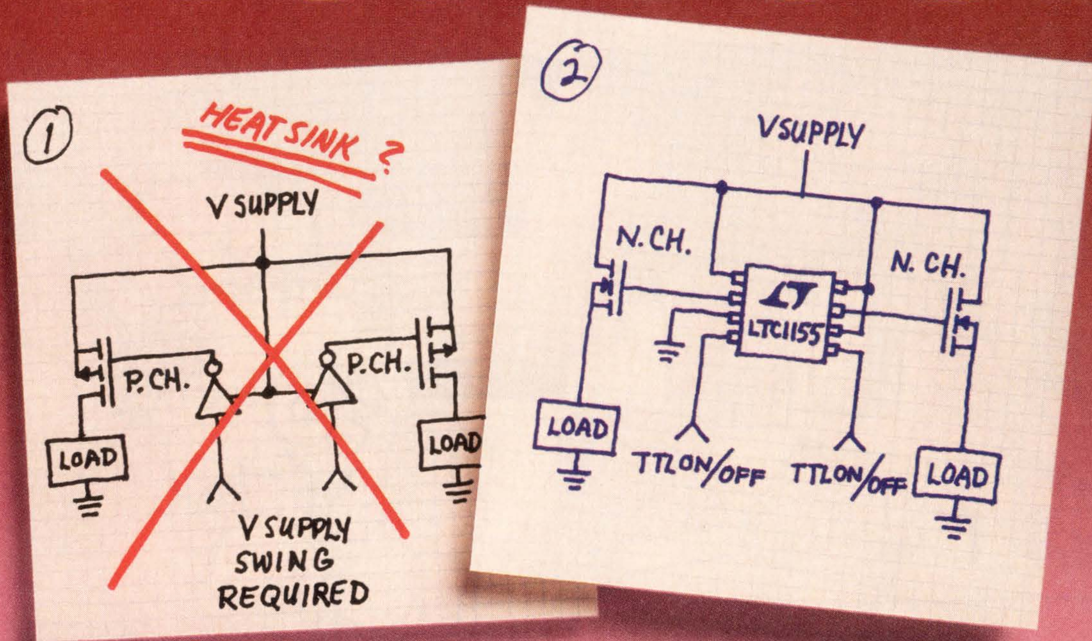

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8031's unused address bits become inputs

Mike Harris, Ten X Technology, Austin, TX

Normally, if an 8031 accesses external program memory, none of the unused pins of I/O-port P2, which outputs the high byte of the 16-bit address, are available for other kinds of I/O. However, the simple software in **Listing 1** allows you to use leftover pins for I/O. The only restriction is that the pins cannot *source* current; open-collector/drain devices must drive them, or you can just jumper them to ground.

Fig 1 shows an 8031 that has 8 kbytes of external memory. Because the design uses only 13 address lines, A_{13}, A_{14}, and A_{15} are available as extra I/O lines. In the **figure**, A_{13} and A_{14} connect to configuration jumpers, and an open-collector 74HC03 drives A_{15}.

To use an 8031's I/O port as an input, software must set the corresponding output-latch control bit to 1 to turn off the pin's output driver and allow the 8031's internal pull-up resistor to pull the signal high. In this state, an external device can leave the pin high or pull it low.

Unused address bits of P2, however, will usually be low and therefore not usable as inputs. In **Listing 1**, the program remedies this situation by executing a long jump to an address that sets the unused bits of P2 high. For the circuit in **Fig 1**, adding $E000_{HEX}$ to an address sets A_{13}, A_{14}, and A_{15} high. After reading the state of these bits, the program simply does a long jump back to restore the program counter.

If your application cannot tolerate the overhead of long jumps, you might try relocating your program to start at $E000_{HEX}$, which would cause the unused bits to remain high during all code fetches. However, not all linkers and EPROM programmers tolerate this relocation. **EDN BBS /DI_SIG #1148**

Listing 1—8031 P2 enabling scheme

```
        ljmp    high+#0E000h        ;force unused bits of P2 to be 1's
high:   mov     C,P2.7              ;read a single input
        ... or ...
        mov     A,P2                ;read entire port
        ljmp    low                 ;restore normal program counter
low:
```

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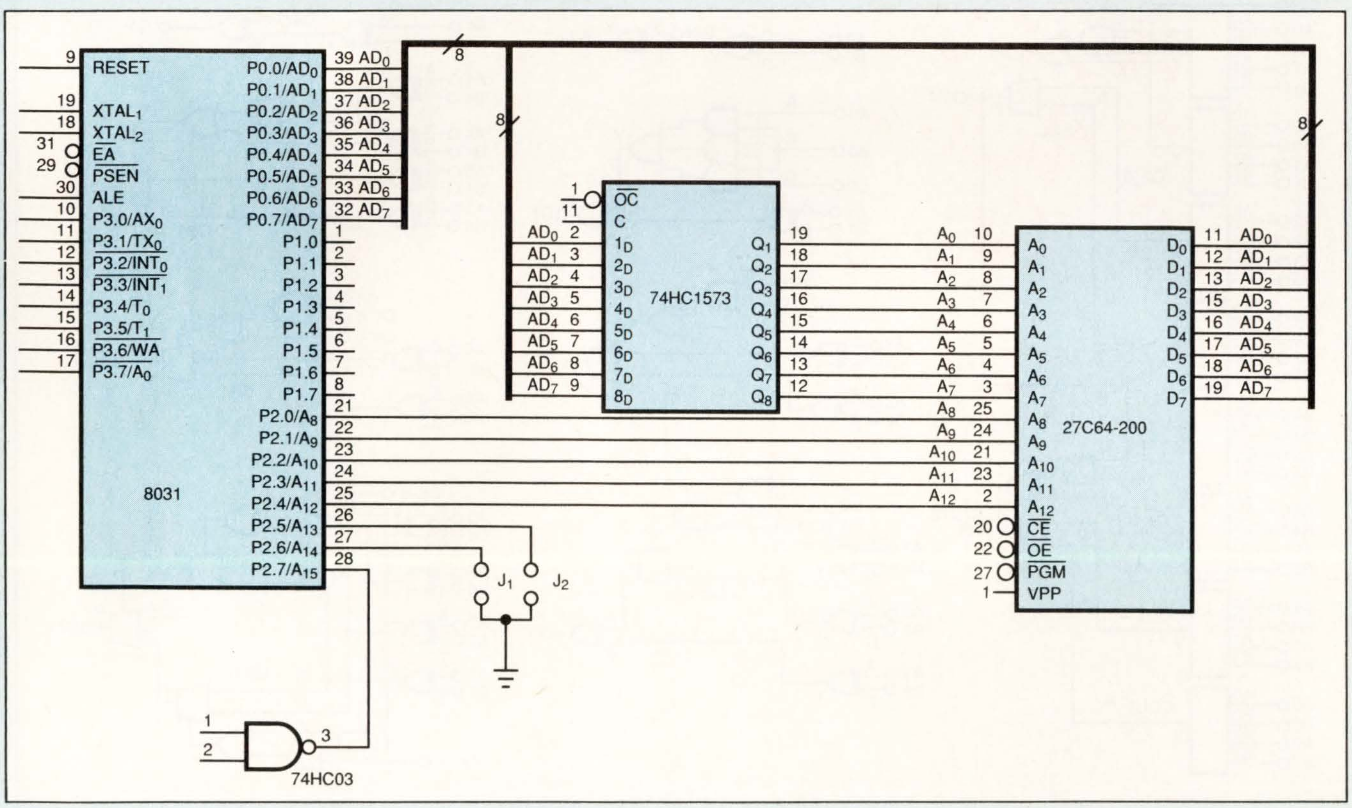

Fig 1—This simple 8031 circuit gets some use out of otherwise useless address pins in port P2.

FPGAs trade off modules for speed

Warren Miller, Actel Corp, Sunnyvale, CA

Unlike designers who work with other forms of logic, field-programmable-gate-array (FPGA) designers can trade off complexity for speed. **Fig 1** shows a simple 8-bit adder that uses the sum-and-carry approach. This design uses the fewest number of FPGA internal modules for a parallel design. However, the worst-case delay is relatively long because signals might have to propagate through eight logic levels.

Fig 2 uses 40 modules but only three logic levels, which decreases propagation delays at the expense of increasing the module count. The carry logic computes carries by assuming both true and false values for certain carries and then using the actual value of the assumed carry to select (via a multiplexer) the proper result at the last nanosecond. **Fig 2**'s circuit develops higher-order sums in a similar manner.

Fig 3a and **Fig 3b** show modifications of the carry-select adder. The two circuits require 34 modules (four levels) and 32 modules (five levels), respectively. **Fig 3a**'s circuit saves six logic modules by adding the C2 and C6 outputs from the carry-generation logic and simplifying the sums for S2, S3, S5, S6, and S7.

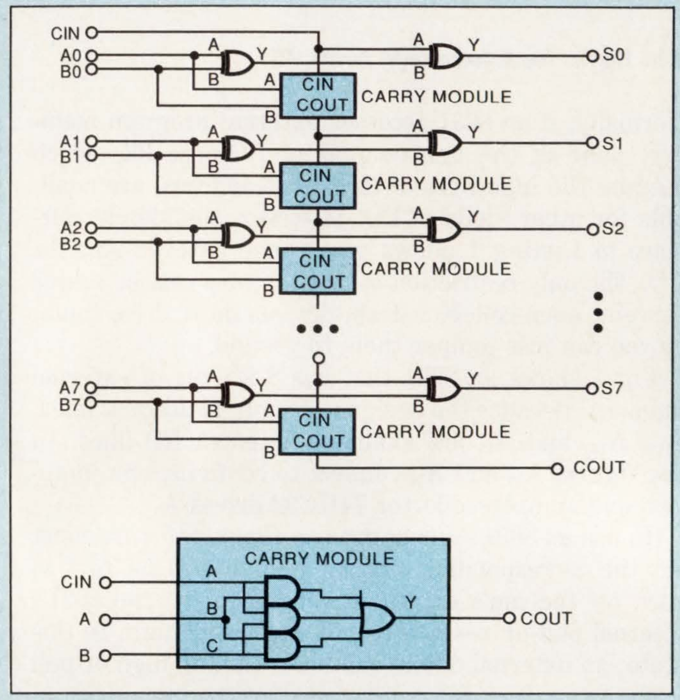

Fig 1—This straightforward adder design uses the fewest FPGA internal modules but incurs eight logic-level delays.

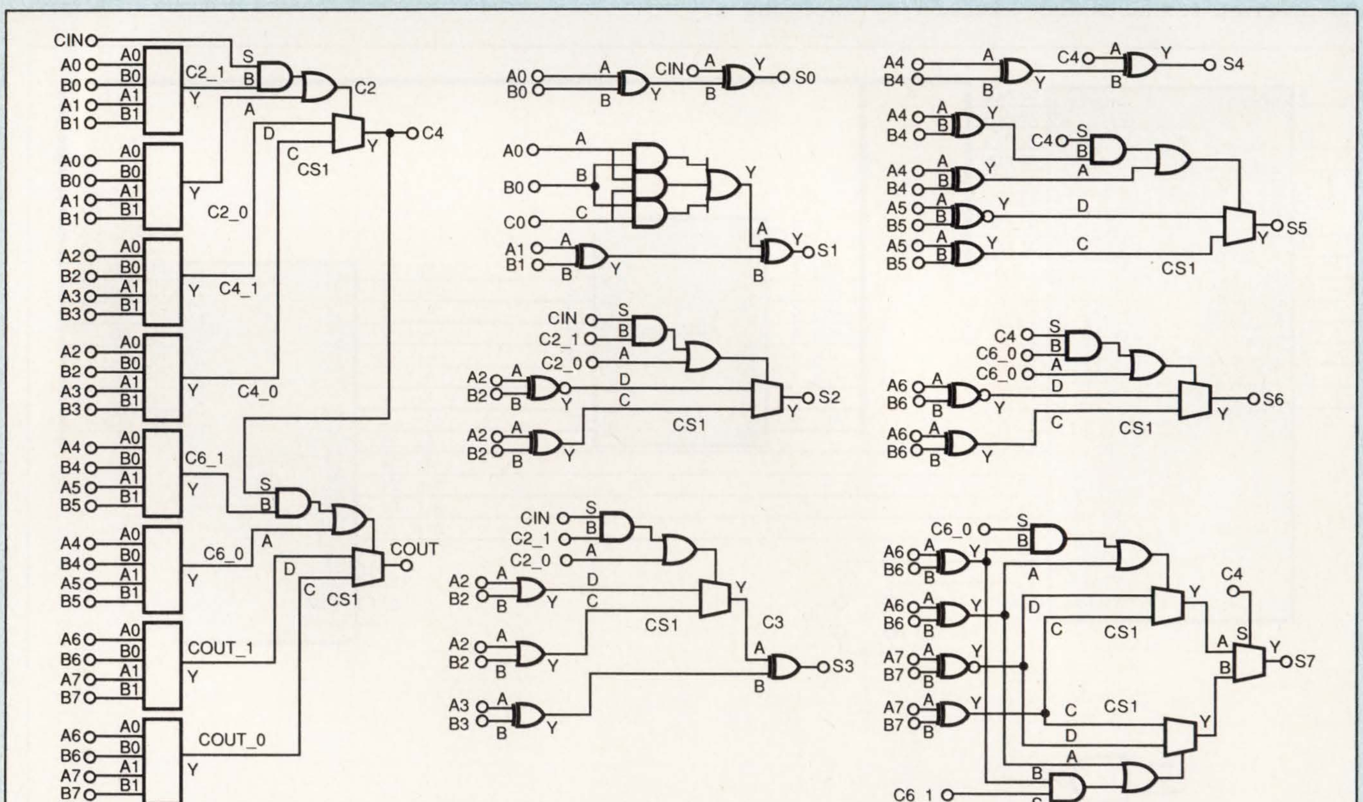

Fig 2—Introducing parallel, "predictive" chains of logic increases the module count for this adder but reduces logic-level delays to three.

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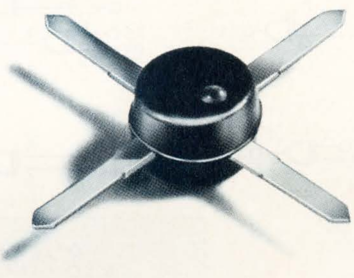

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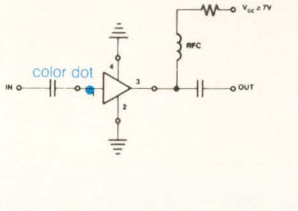

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Fig 3b simplifies the design further by adding another level of logic for S7.

Random logic and multipliers can also use this "predictive" method. Counters, too, can employ the predictive technique by using the least significant bits to select between the two possible counting results: toggle and hold. Again, this technique requires more logic modules than traditional techniques, but it can increase performance dramatically because the least significant bits require only a single logic level. The most significant bits can tolerate more logic levels because they change infrequently.

This module/logic-level tradeoff also applies to other FPGA designs such as counters, random logic, multipliers, and state machines. State machines can use the bit-per-state approach. Additional techniques for increasing performance at the expense of module count are pipelining and paralleling logic to reduce fanout. **EDN BBS /DI_SIG #1149**

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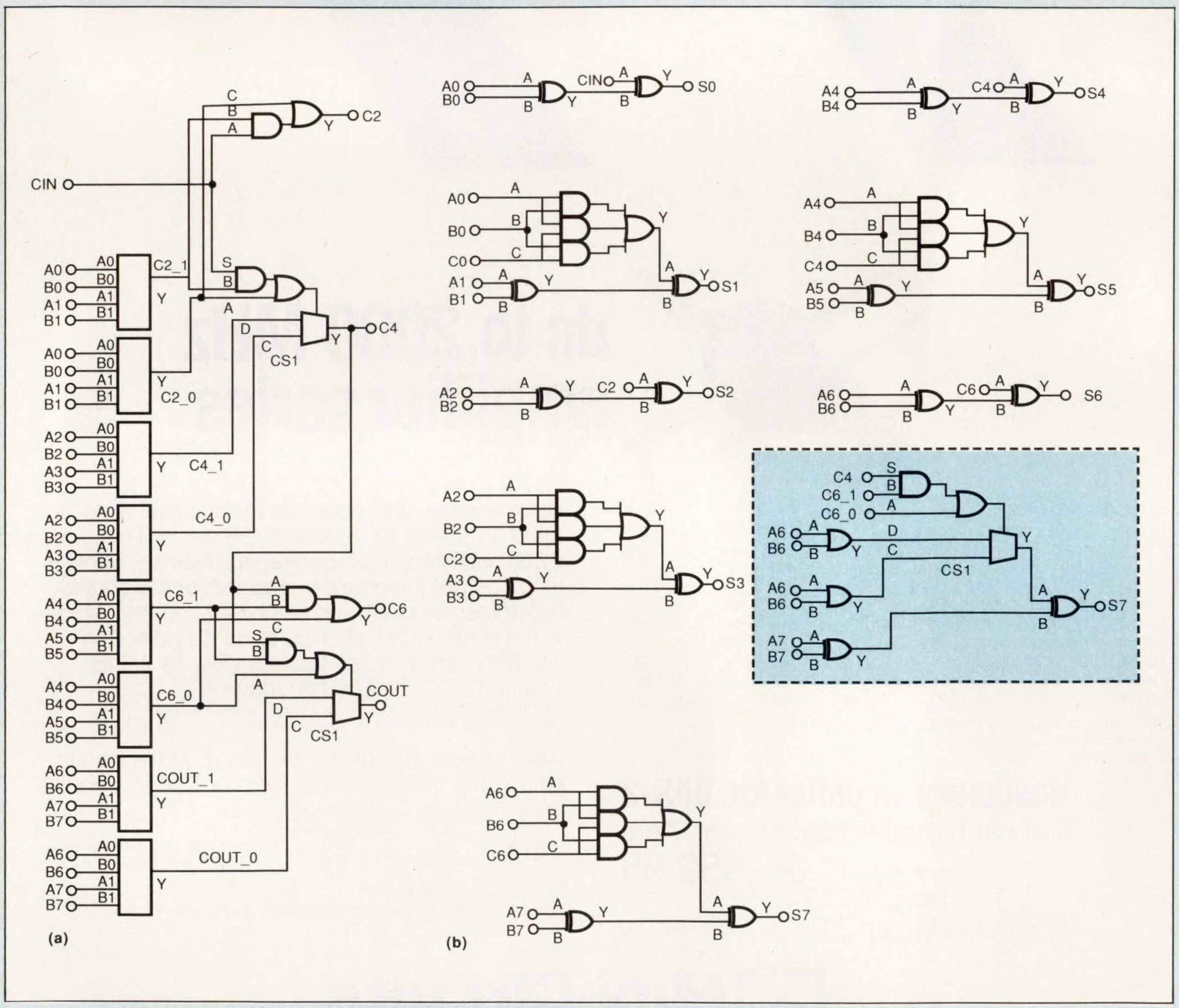

Fig 3—Intermediate in complexity between Fig 1's and Fig 2's designs, the adder in (a) has four logic-level delays. Substituting the circuitry in (b) for the dashed circuitry in (a) yields a simpler design having five logic-level delays.

PC printer port programs PROMs

Yongping Xia, EBT Inc, Torrance, CA

Fig 1 shows a 2817 programmer you can build. A PC's printer port controls the programmer. The printer port has eight data-output lines (pins 2 to 9), four control lines (pins 1, 14, 16, and 17), and five input lines (pins 10, 11, 12, 13, and 15). The data lines send out the 2817's address and program data. The control lines control the programming sequence. After programming is completed, the PC reads the programmed data back in through its input port for verification.

The Turbo C program in **Listing 1** sends the 2817's program, contained in a binary file named p2817.dat, to the programmer in this sequence: 8 bits of data, followed by the low 8 bits of the address, and finally by the high 3 bits of the address (which the programmer latches into IC_1, IC_2, and IC_3). The printer port's

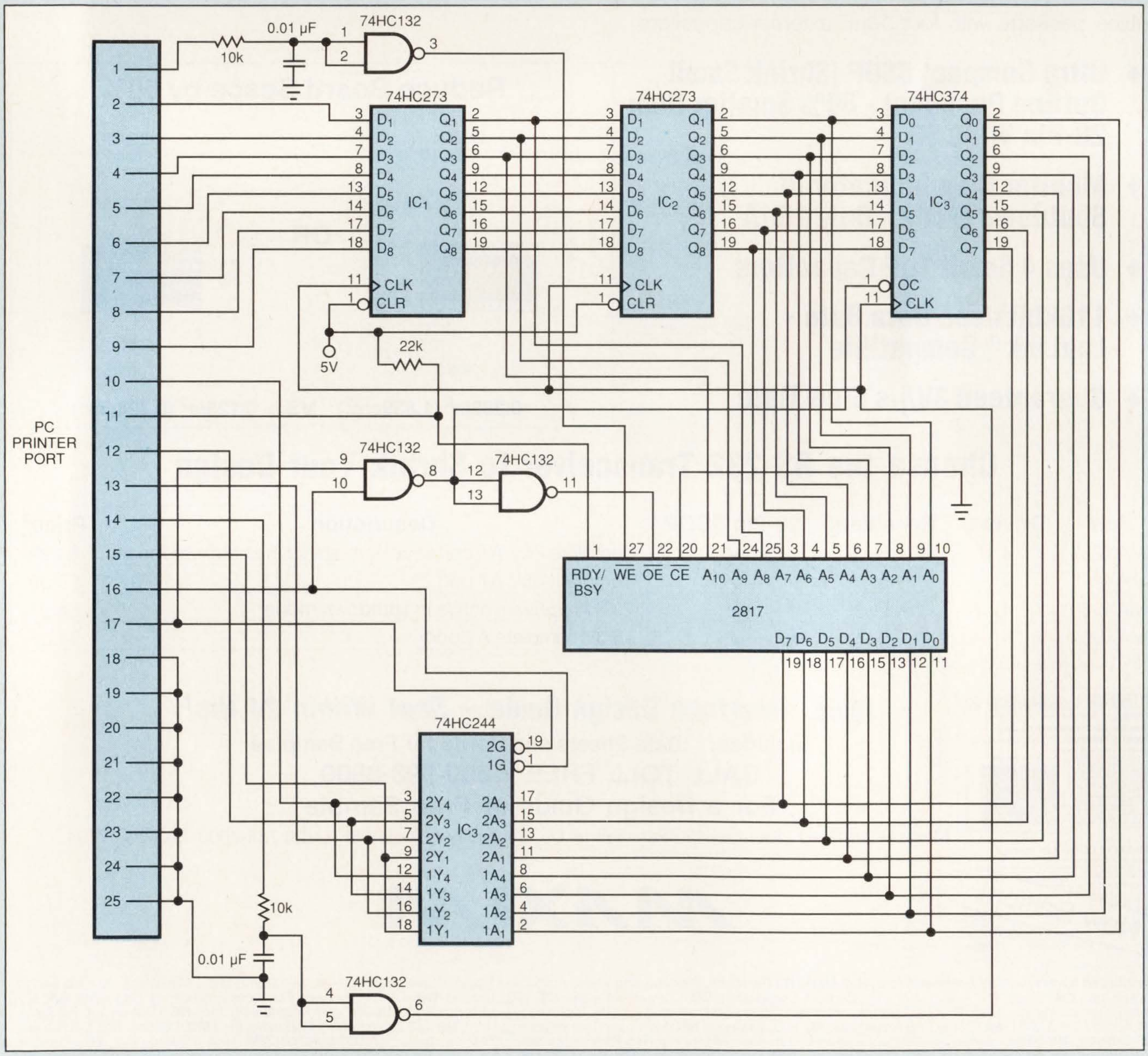

Fig 1—A PC's printer port and a simple Turbo C program control this 2817 programmer.

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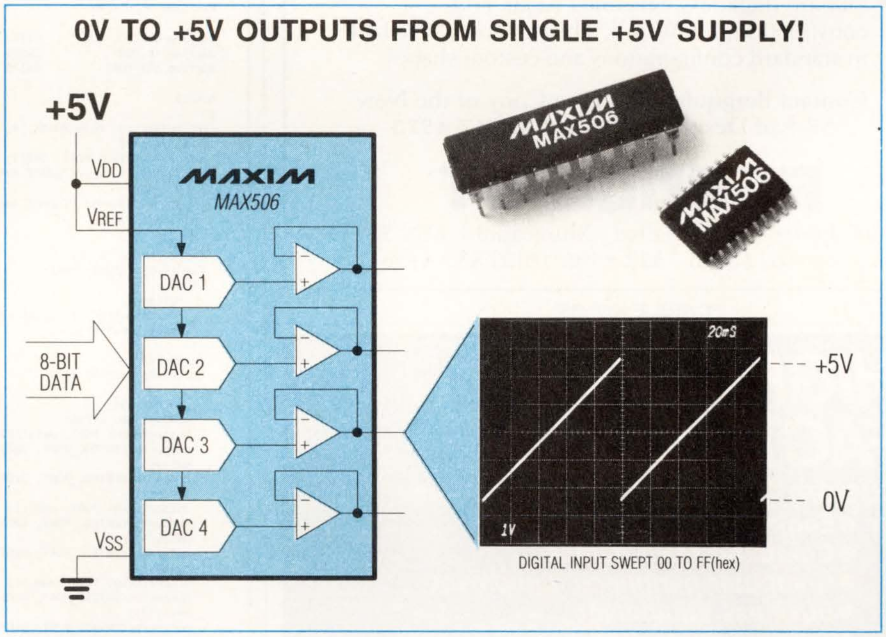

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CIRCLE NO. 84

pin 14 clocks these 19 bits in. Then the PC polls the 2817's RDY/BUSY line via printer-port pin 11, waiting for the chance to send the next data-address combination. After programming all 2 kbytes of the PROM, the PC will read the 2817 using printer-port pins 16 and 17. A copy of the program is available on the EDN BBS. **EDN BBS /DI_SIG #1146**

To Vote For This Design, Circle No. 745

Listing 1—2817 programmer control program

```
#include <stdio.h>

#define CONTROL_PORT      0x37a  /* printer control port address  */
#define IN_PORT           0x379  /* printer input port address    */
#define OUT_PORT          0x378  /* printer output port address   */

main()
{
 int buffer,tp, data[2048], i, add_h, add_l, readin_1, readin_2,        read_data;
 FILE *stream;
 outportb(CONTROL_PORT, 0x07);
 if ((stream = fopen("p2817.dat", "rb")) == NULL)
   {
     fprintf(stderr,"Cannot open input file.\n");
     return 1;
   }
  fseek(stream, 0, 0);
  for (i=0; i<2048; i++)
   {
     buffer=0;
     fread(&buffer, 1, 1, stream);
     data[i]=buffer;
   }
  fclose(stream);
  for (i=0; i<2048; i++)
   {
    add_h=i/256;
    add_l=i-add_h*256;
    outportb(OUT_PORT, data[i]);    /* send out data               */
    outportb(CONTROL_PORT, 0x05);
    delay(1);
    outportb(CONTROL_PORT, 0x07);
    delay(1);
    outportb(OUT_PORT, add_l);      /* send out low address        */
    outportb(CONTROL_PORT, 0x05);
    delay(1);
    outportb(CONTROL_PORT, 0x07);
    delay(1);
    outportb(OUT_PORT, add_h);      /* send out high address       */
    outportb(CONTROL_PORT, 0x05);
    delay(1);
    outportb(CONTROL_PORT, 0x07);
    delay(1);
    outportb(CONTROL_PORT, 0x06);   /* write address into 2817     */
    delay(1);
    outportb(CONTROL_PORT, 0x07);   /* write data into 2817        */
    do {
        delay(1);
      } while (inportb(IN_PORT) & 0x80 != 0x00);     /* wait      */
   }

   for (i=0; i<2048; i++)           /* check programmed data        */
   {
    add_h=i/256;
    add_l=i-add_h*256;
    outportb(OUT_PORT, add_l);      /* send out low address        */
    outportb(CONTROL_PORT, 0x05);
    delay(1);
    outportb(CONTROL_PORT, 0x07);
    delay(1);
    outportb(OUT_PORT, add_h);      /* send out high address       */
    outportb(CONTROL_PORT, 0x05);
    delay(1);
    outportb(CONTROL_PORT, 0x07);
    delay(1);
    outportb(CONTROL_PORT, 0x03);
    delay(1);
    readin_1=inportb(IN_PORT) & 0x78;   /* read low 4-bit data   */
    outportb(CONTROL_PORT, 0x0f);
    delay(1);
    readin_2=inportb(IN_PORT) & 0x78;  /* read high 4-bit data   */
    outportb(CONTROL_PORT, 0x07);
    delay(1);
    read_data=readin_1/8 + readin_2*2;
    if (read_data != data[i])
      {
        fprintf(stderr,"Program error.\n");
        return 1;
      }
   }
  return 0;
}
```

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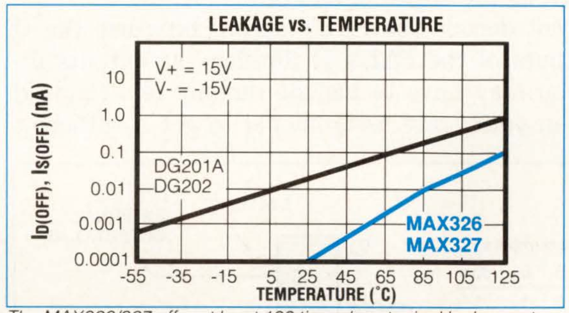

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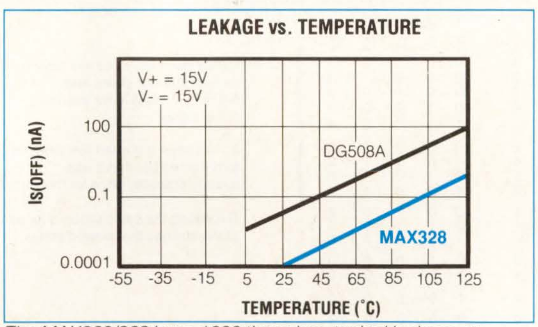

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CIRCLE NO. 87

Simple system speeds state machines

Mohamed Shawky, Université de Compiègne, Compiègne, France

If you follow two simple design precepts, you will be able to fit complex finite-state machines into the fastest PALs such as the 16R4, 6, and 8.

1. Do not decode the PAL's output bits; use the Q or $\overline{Q}$ outputs of the PAL's D flip-flops as outputs directly. You may have to include dummy bits (unused outputs) in your state assignments to get a sufficient number of unique states. **Fig 1** shows flip-flops used as outputs without decoding and a hardware-description-language (HDL) program for the state machine. Note that the **figure** also shows a dummy output, without which the state machine would not have enough states.

2. When making state assignments, ensure that a given bit is active for only the required number of states. **Fig 2** shows a sample state assignment.

This method limits the PALs' outputs. For example, a 16R8 can have only eight or fewer outputs; if you were to decode a 16R8's output flip-flops, you could have as many as 256 outputs. So, for state machines that require more than eight outputs, you will have to connect PALs in parallel. **EDN BBS /DI_SIG #1147**

State numbers:

state	B_1	B_0	dum
idle	1	1	1
wr1	0	1	0
wr2	0	1	1
rd1	1	0	0
rd2	1	0	1

```
state transitions:
state idle:
  case
    dir=1: goto wr1;
    dir=0: goto rd1;
  endcase;
state wr1:
  goto wr2;
state wr2:
  goto idle;
state rd1:
  goto rd2;
state rd2:
  goto idle;
```

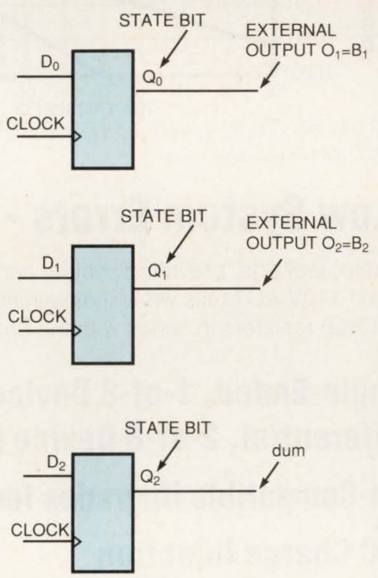


Fig 1—Using the flip-flop outputs of a PAL directly as state-machine outputs means you may have to include unused flip-flop outputs as dummy state-machine output bits to make state assignments. The hardware-description-language (HDL) fragment shows how to enforce this precept.

To Vote For This Design, Circle No. 746

State bits

state n	B_4	B_3	B_2	B_1	B_0
1	0	0	0	0	1
3	0	0	0	1	1
5	0	0	1	0	1
9	0	1	0	0	1
17	1	0	0	0	1
2	0	0	0	1	0
4	0	0	1	1	0
5	0	1	0	1	0
18	1	0	0	1	0
4	0	0	1	0	0
12	0	1	1	0	0
20	1	0	1	0	0
8	0	1	0	0	0
24	1	1	0	0	0
16	1	0	0	0	0
0	0	0	0	0	0

B_0 has been activated five times, for five different states and will remain inactive for the rest of the states.

B_1 has been activated five times in its turn (remember that it was already activated once for the state 3).

Repeating the same process for all the states defines the allowed states.

Fig 2—When making state assignments, ensure that a given output bit is active for only the requisite number of states.

Program calculates noise from Spice file

Richard Faehnrich, Bio-Imaging Research Inc, Lincolnshire, IL

BBS

Although Spice can calculate the noise-voltage spectral density for each particular frequency you specify, it cannot calculate the total output rms noise voltage over a specified frequency range. But you need this total-noise figure if, for example, you're going to calculate the S/N ratio.

The C program in **Listing 1** uses the trapezoidal-approximation method to integrate the mean square

of the noise voltage. The program then takes the square root as a final step to arrive at the root-mean-square noise voltage.

For simplicity, the program operates on the variable ONOISE, which must be printed in the first column of a standard Spice output file. The program reads the Spice output file line by line, searching the text for keywords "FREQ" and "ONOISE" in the same line. The program reads the frequency and noise values as text, converts them to floating-point numbers, and stores them in arrays. You could modify the program to also calculate other noise values.

To run the program in **Listing 1**, enter "ntot <filename.ext>", where <filename.ext> is your Spice output file. You can get a copy of the **listing** from the EDN BBS. **EDN BBS /DI_SIG #1150** EDN

To Vote For This Design, Circle No. 747

Listing 1—Spice rms-noise-voltage program

```
/* NTOT.C -- Calculate total rms noise voltage, Vrms, from SPICE output file */
/* total mean-square noise = integral approx of mean-square spectral density */
/*                           over frequency using trapezoidal method         */
/* Vrms = square root of total mean-square noise                             */
/* Usage: ntot "filename.ext"           Example: ntot lowpass.out            */
/* Note:  ONOISE analysis must be located in first column of .out file       */

#define TRUE 1
#define FALSE -1
#define NEWLINE 10

#include <math.h>
#include <stdio.h>
#include <string.h>

char string[81];
float fr[100];
float on[100];

main(argc,argv)
int argc;
char *argv[];
{
FILE *fptr;
int i = 0;
int flag = FALSE;
int index = 0;
float ntot = 0;

if(argc != 2)                             /* open file if possible      */
      { printf("ntot filename.OUT");exit();}
if( (fptr=fopen(argv[1],"r"))==NULL)
      { printf("Can't open file %s.", argv[1]);exit();}

                                          /* input strings from file    */
while( fgets(string,80,fptr) != NULL && strstr(string,"JOB") == NULL)
{
                                          /* check if noise page end    */
   if( flag == TRUE && string[0] == NEWLINE && index > 0 ) flag = FALSE;

   if(flag == TRUE && string[0] != NEWLINE) /* if noise data, then read */
   {
   sscanf(string," %e %e",&fr[index], &on[index]);/* get freq and onoise data */
   printf("freq = %e  onoise = %e\n",fr[index],on[index]);
   index++;
   }
                                          /* check for noise analysis page */
   if( strstr(string,"FREQ") != NULL && strstr(string,"ONOISE") != NULL)
   {
   flag = TRUE;
   }
}
fclose(fptr);
                               /* Trapezoidal approximation              */
for(i=0;i<index;i++) ntot+=( on[i+1]*on[i+1] + on[i]*on[i])/2*(fr[i+1]-fr[i]);
ntot = sqrt(ntot);             /* Vrms = square root of power            */
printf("\nTotal noise voltage = %e Vrms\n",ntot);
}
```

Reader proposes real turnoff

My circuit in **Fig 1** is an improved version of Carl Hallman's ("Battery-powered microprocessor turns itself off," EDN, January 20, 1992, p 133). When you press S_1, transistor Q_1 turns on, enabling transistor Q_2, which in turn powers the 5V converter, IC_1. IC_1 powers the rest of the circuitry. The µP must immediately bring HOLD_POWER high to keep Q_1 and Q_2 on. The transistors are MOSFETs, which reduces the circuit's power consumption.

Turning Carl's circuit off might not be quite as easy as he describes, especially with his bipolar transistors. You must be careful that the signal HOLD_POWER doesn't return high because of an undefined µP state that occurs as the µP powers down. Adding a Motorola MC34064 undervoltage sensor to the $\overline{RST}$ line of the µP keeps the circuit from waking back up. R_1 and D_1 ensure that HOLD_POWER is "don't care" whenever the MC34064 has determined that the V_{CC} line is too low. The MC34064 will work down to $V_{CC}=1.0V$. At 1V, insufficient voltage remains to turn Q_1 back on.

Compared to Carl's circuit, all the diodes in my circuit may seem a bit Byzantine, but the reason I've rearranged everything is to allow the free end of S_1 to connect to 9V rather than ground. Thus we can sense further switch presses by level-shifting the signal through Q_3 and R_2, creating $\overline{\text{SW\_PRESSED}}$. Your software can monitor this signal as an on switch or as a toggling on/off switch.

The r_{DS} of Q_2 can be significant if the circuit draws more than about 100 mA. So use the circuit for CMOS µPs only.

Robert Lamm
Kesa Corp
4701 Patrick Henry Dr, Suite 1801
Santa Clara, CA 95054

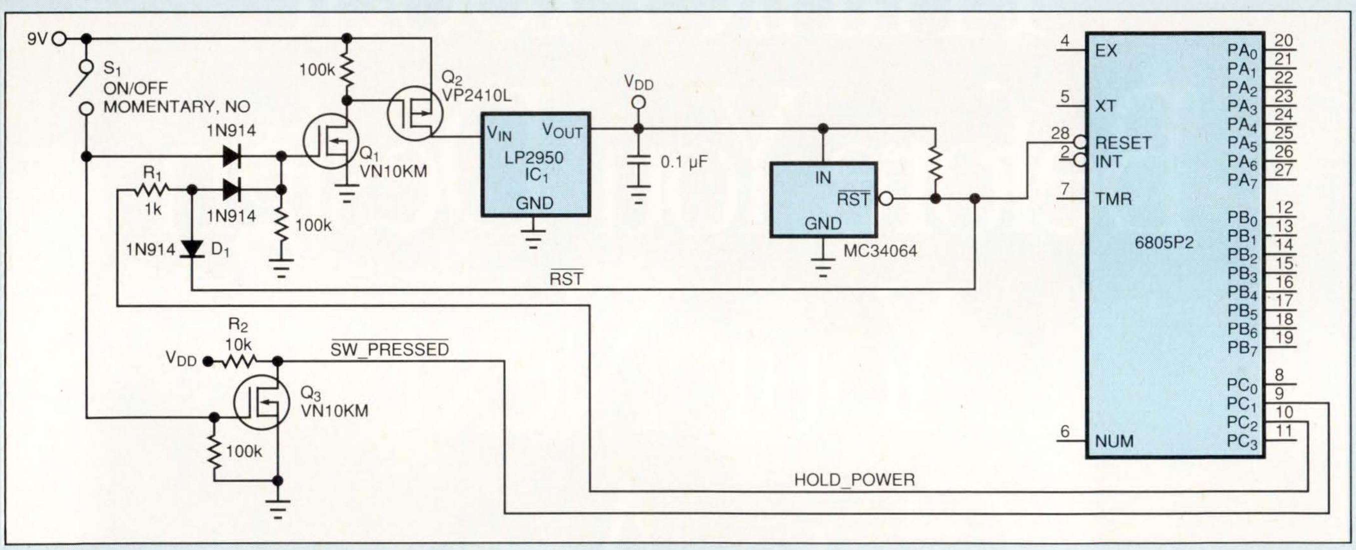


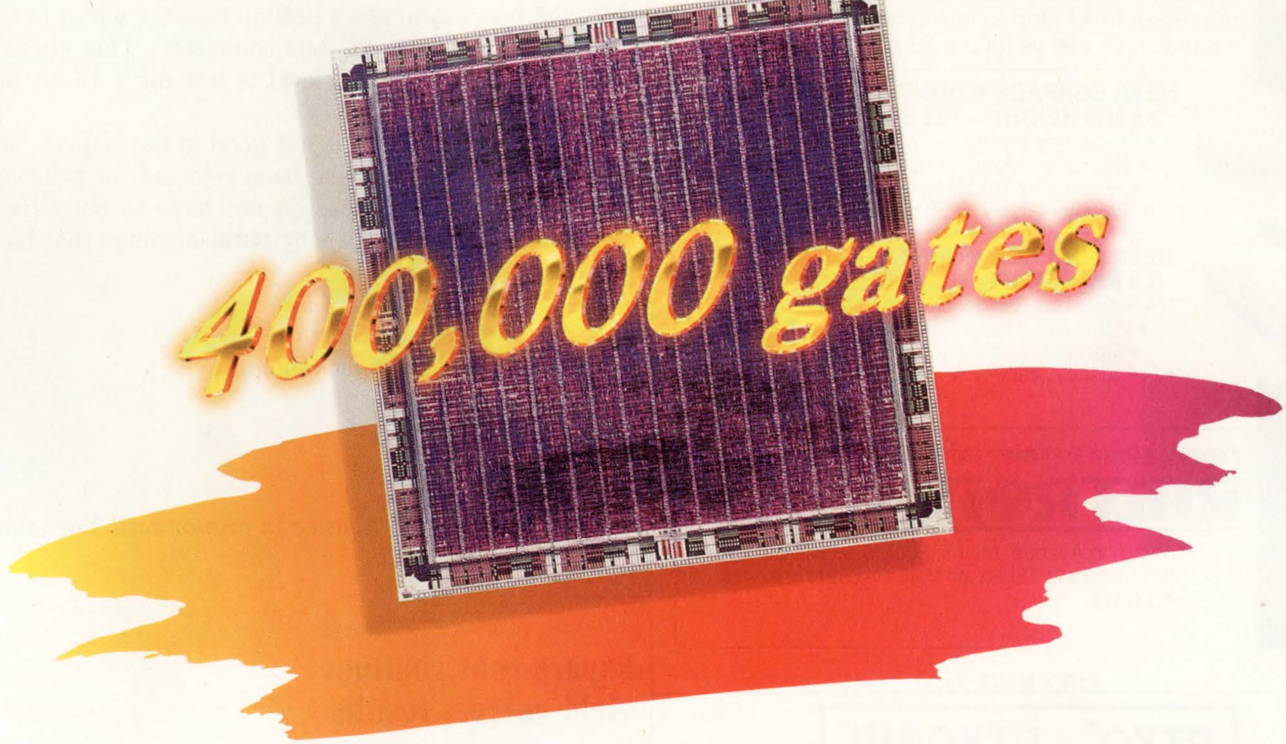
Fig 1—This improved circuit ensures that the µP turns itself off and stays off.

Resistor replaces circuit

I would like to discuss "IBM PC board adapts to different buses," (EDN, March 2, 1992, p 142, DI #1088) by Vladimir Bochev. First let us examine the circuit's structure and cost, assuming the specification is correct—for a while. Because the flip-flop has complementary outputs, you can replace the NOT and AND gates with NANDs (exchanging the PRESET and CLEAR inputs as well). Now let us take a closer look at the inputs. A memory read or write will set the outputs, and, therefore, feeding the clock input directly from the MEMR line seems to be sufficient. Thus you need only a flip-flop and an inverter. If you insist on edge-triggering the circuit, these functions fit nicely in one 7474 (I love asking students to make an inverter using a spare flip-flop); if latching is good enough, you need only a 7400.

And now, back to the specification. The sole purpose of the circuit is to identify the slot type, and, fortu-

Think Performance.



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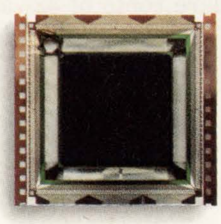

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CIRCLE NO. 92

nately, no logic at all is necessary to accomplish this task. The solution to adapting an IBM PC board to different buses is to use a pull-up resistor wired to the D_{18} pin on the short PC bus connector. This pin is a GND line, so the sensed level is low for a 16-bit bus and high for an 8-bit bus.

The submitted circuit is not good in any aspect, and I believe it should not have been selected for printing. I agree that Design Ideas do not have to be optimal or minimal solutions, but why publish things that have no advantages?

Jerzy R Chrzaszcz
Institute of Computer Science
Warsaw University of Technology
Nowowiejska 15/19
00-665 Warsaw
Poland

(Ed Note: The writer's name is pronounced Yair-zhuh Shar-shon-sth.)

Square-root routines yield correct results

Much to my surprise, the square-root routine in "8086 computes square roots," (EDN, August 19, 1991, p 166, **EDN BBS /DI_SIG #1007**) by Jack D Dennon, not only was not as tight as it could be, it also produced incorrect results. Posted on the EDN BBS as a reply to **EDN BBS /DI_SIG #1007** are two routines of mine for computing the square roots of 32- and 16-bit integers. My routines are shorter and produce correct results.

James W Neil
Medicomp Inc
7845 Ellis Rd
West Melbourne, FL 32904

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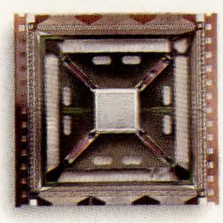

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CIRCLE NO. 95

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Software Shorts

PWM gives voice to a PC

András Pomozi and László Szilágyi,
Technical University of Budapest
Budapest, Hungary

In **EDN BBS /DI_SIG #1151**, the pulse-width-modulation (PWM) program enables a PC to speak, sing, and play music.

To Vote For This Design, Circle No. 748

Spice models controlled resistance

Keith Timothy
Orange, CA

The Spice models in **EDN BBS /DI_SIG #1152** for voltage-controlled and current-controlled resistances command Spice to try a range of values of R in a single pass without specifying individual values.

To Vote For This Design, Circle No. 749

PC debugs DSP56001 µP

M Venkateswarlu and G V L Narasimha Babu,
Hindustan Aeronautics Ltd
Hyderabad, India

In **EDN BBS/DI_SIG #1153**, the programs and documentation let you debug Motorola DSP56001 µP projects over a PC's serial line, thus obviating an in-circuit emulator.

To Vote For This Design, Circle No. 750

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Ariel V-C40 Hydra Breaks the BOPS Barrier

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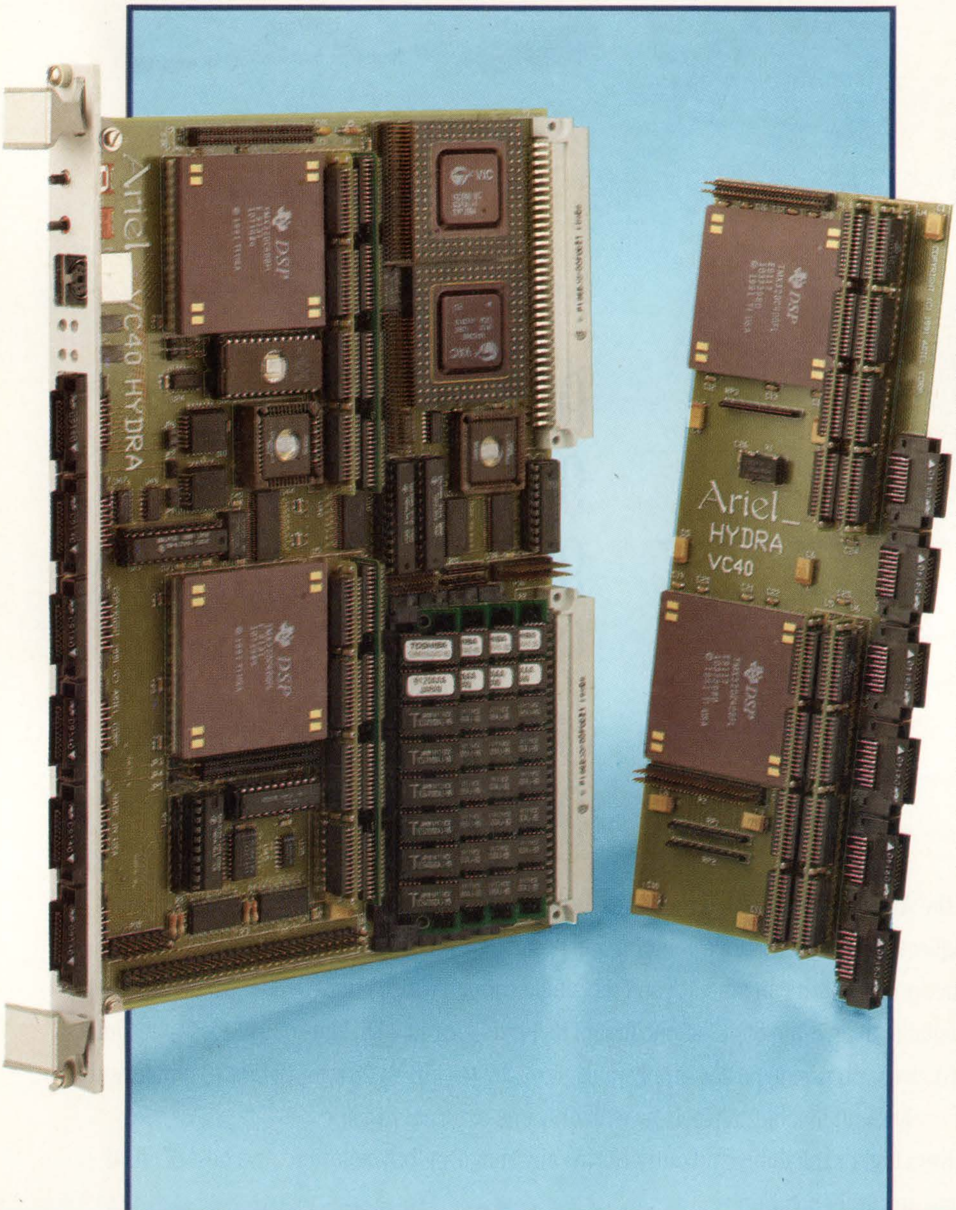

Only Ariel's Hydra combines four TI TMS320C40 DSPs to deliver twice the processing speed and four times the I/O bandwidth of any 6U VMEbus coprocessor card. It's the only choice for the most compute-intensive multiprocessor applications.

The V-C40 packs up to 64 Mbytes of DRAM as well as up to 5 Mbytes of SRAM in eight banks—two per processor. Each DSP has direct access to memory via dual 32-bit memory buses, as well as six parallel I/O ports and a high-speed six-channel programmable DMA controller. All six channels can transfer data simultaneously without interrupting program execution.

Hydra also includes a 24-bit parallel ADbus that lets you access a wide range of high-speed data acquisition cards. Development support includes an ANSI C compiler and the first PC-based XDS510 in-circuit emulator to support parallel processing. And of course, with Ariel's legendary technical support, you'll never work alone.

To learn more about the V-C40 Hydra, or any of Ariel's DSP products for ISA/EISA, VMEbus, SBus, Hewlett-Packard, NeXT, or Macintosh computers, send us a fax, leave us a message on the BBS or E-mail, or just give us a call.

Ariel_

The DSP Authority

433 River Road Highland Park, NJ 08904
(908) 249-2900 FAX:(908) 249-2123
DSP BBS:(908) 249-2124
Email: ariel @ ariel.com

Distributed in: **France**, REA Informatique, tel: 1 49 65 25 50, fax: 1 49 65 25 69; **Israel,** Militram Futuristic Technology Ltd., tel: 52-545685, fax: 52-574383; **Italy**, International Trading Device SRL, tel: 02-749 0749, fax: 02-761 0407; **Japan,** Marubun Corp., tel: 033-639 9816, fax: 033-661 7433.

CIRCLE NO. 99

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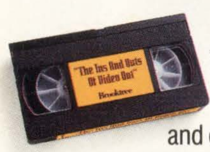

What's in? Video Out. Outputting video to a VCR and displaying video on a composite monitor are the newest capabilities every computer will need to compete in the Multimedia Age.

Now you're just a single chip away from adding Video Out to your very next computer design. Introducing Bt858, a monolithic digital device that packs in a board full of analog circuitry and puts out studio quality composite video.

Bt858 is a tweakless all-digital chip that bridges the video gap between RGB computers and composite or S-VHS outputs in the NTSC/PAL formats. It accepts multiformat digital inputs from 24, 16 or 15-bit RGB, 24 and 16-bit YCrCb and 8-bit VGA.

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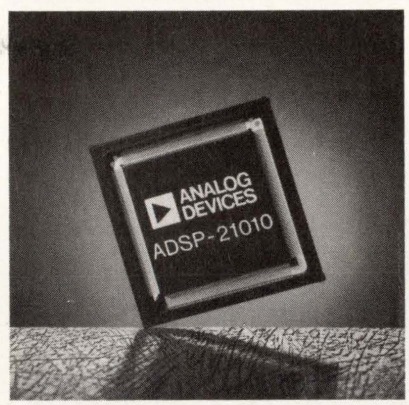
Integrated Circuits

Digital synthesizer. The Q2220 single-channel direct digital synthesizer (DDS) has dedicated pins controlling the output frequency via the frequency control register. This feature allows the output to be programmed asynchronously or synchronously with the system clock. It can modulate at 50 MHz with a minimal 5-clock-cycle pipeline delay. The on-chip sine-computation function provides a digitized 10-bit value for the sine-waveform output with spurious levels below −60 dBc. From $13.50 (1000). **Qualcomm Inc,** 10555 Sorrento Valley Rd, San Diego, CA 92121. Phone (619) 597-5005. FAX (619) 452-9096.
Circle No. 394

1-Mbit SRAM. Organized as 64k×16 bits, the TC551664J-xx series of static RAMs (SRAMs) comes in speed ratings of 15, 20, and 25 nsec. The speed and organization suits these chips as a secondary cache for the Mips R4000. Maximum operating currents with a 5V supply range from 200 to 260 mA. All devices come in 44-pin SOJ packages. Depending on speed, from $62 to $118 (1000). **Toshiba America Electronic Components Inc,** 9775 Toledo Way, Irvine, CA 92718. Phone (714) 455-2000.
Circle No. 395

Hard-disk motor driver. Encapsulated in a space-saving 9×9×1.7-mm high-power quad flatpack, the HA13517F controls the spindle motor and voice-coil motor in small hard-disk drives. The IC provides 1A/phase of peak current for the spindle motor and 400 mA (max) of voice-coil motor current. The combination driver supports sensorless spindle designs and features soft-switching outputs and latch capabilities. $8 (1000). **Hitachi America Ltd,** Semiconductor and IC Div, 2000 Sierra Point Pkwy, MS-080, Brisbane, CA 94005. Phone (415) 589-8300. FAX (415) 583-4207.
Circle No. 396

Serial communications controller. The Z80230 Z-bus version of the company's enhanced serial-communications controller allows easier interfacing to many multiplexed CPUs, including the Z8, Z8000, and the 80X86 family. The Z80230 permits direct register access, simplifying I/O operations. An 8-byte receive FIFO and 4-byte transmit FIFO reduce the overhead needed to move data between the transmitters and receivers. In 10- and 16-MHz versions, $10.21 and $15.71 (100), respectively. **Zilog,** 210 E Hacienda Ave, Campbell, CA 95008. Phone (408) 370-8000. FAX (408) 370-8056. **Circle No. 397**



Floating-point DSP. The ADSP-21010 32-bit floating-point IC performs a 1024-point FFT in 1.54 nsec at a 12.5-MHz cycle time (80-nsec instruction cycle). The unit works with 32-bit IEEE floating-point and fixed-point operations only. In 304-pin plastic quad flatpacks, $40.90 (100). **Analog Devices Inc,** Box 9106, Norwood, MA 02062. Phone (617) 461-3672. **Circle No. 398**

Temperature sensors. The TC620, TC621, and TC626 temperature sensors directly convert temperature to a digital output. The TC620 allows users to program upper and lower temperature settings. The TC621 is designed for use with an external thermistor for remote-sensing applications. The TC626 unit is preset at the factory (in 5°C increments) for applications that require a switch. In plastic and ceramic DIPs and SOICs, $2.15 (10,000). **Teledyne Components,** 1300 Terra Bella Ave, Mountain View, CA 94039. Phone (415) 968-9241.
Circle No. 399

Cache RAMs. The CY7B180 and CY7B181 BiCMOS cache-tag RAMs feature a 12-nsec address-to-match time. Both units provide 16 tag bits and 2 status bits in each entry. The devices consolidate cache status validation and chip-select decoding on chip. The RAMs feature separate compare-data and data ports as well as independent access to tag and status fields. $72.05 (100). **Cypress Semiconductor,** 3901 N First St, San Jose, CA 95134. Phone (408) 943-2600. **Circle No. 400**

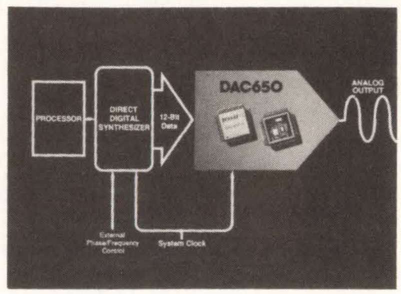
Laser diode. The HL6713G AlGaInP laser diode operates at 670 nm. It features a 5-μm astigmatism and a maximum droop of 10%, specified at 3-mW output with a pulse rate of 600 Hz. Beam divergence is 9° typ, and slope efficiency equals 0.34 mW/mA. The unit incorporates a built-in photodiode and operates over −10 to +50°C. $62 (1 to 99). **Hitachi America Ltd,** Semiconductor & IC Div, 2000 Sierra Point Pkwy, Brisbane, CA 94005. Phone (415) 589-8300. FAX (415) 583-4207. **Circle No. 401**

Display drivers. The SNJ553491 and SNJ553492 provide 80 channel outputs and comply with MIL-STD-883 Class B. The devices are designed to provide row and column drive for LCDs. The 491 provides the row drive function and features serial data in and data out. The 492 provides the column drive and features a 4-bit input data bus. In 100-pin ceramic quad flatpacks, $128.50 (1000). **Texas Instruments Inc,** Semiconductor Group (SC-92032), Box 809066, Dallas, TX 75380. Phone (800) 336-5236, ext 3990; (214) 995-6611, ext 3990.
Circle No. 402

ECL SRAM. MBM family 4-Mbit static RAMs have a 15-nsec access times. The MBM101C524, MBM10C524-15, MBM-100C524-15 have a 1M-word×4-bit organization; the MBM101C520-15, MBM10C520-15, and MBM100C52-15 have a 4M-word×1-bit organization. In 32- and 36-pin surface-mount packages, $425 (1000). **Fujitsu Microelectronics Inc,** 3545 N First St, San Jose, CA 95134. Phone (800) 642-7616; (408) 922-9825. **Circle No. 403**

RISC μP. The 32-bit IDT79R3081 RISC (reduced-instruction-set-computer) μP consists of an R3000A execution unit and memory-management unit (MMU) integrated with an R3010A floating-point accelerator, a total of 20 kbytes of instruction and data cache, and 4-deep read/write buffers. The MMU function gives the designer page management and Unix compatibility. Unit, with or without translation look-aside buffer (TLB), from $130 (without TLB). **Integrated Device Technology Inc,** 3236 Scott Blvd, Santa Clara, CA 95052. Phone (408) 727-6116. FAX (408) 492-8674. **Circle No. 404**

LCD drivers and controllers. The M50532-002FP and M50530-001FP controller drivers drive 4-line × 10-character and 4-line × 8-character LCDs, respectively. Both feature 256-character onboard ROM. The companion M50524FP and M50521FP drivers expand drive capacity to a maximum of one line of 256 characters, two lines of 128 characters, or four lines of 64 characters. The 24FP drivers have two sets of 40-channel LCD drive circuits; the 21FP units feature two sets of 20-channel circuits. The 128-pin M50532-002FP, $7; 100-pin M50530-001FP and M50524FP, $5; 60-pin M50521FP, $2.50 (10,000). **Mitsubishi Electronics America Inc,** 1050 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 730-5900. **Circle No. 405**



D/A converter. The DAC650 12-bit DAC comes with internal reference and data latches. It features a 500-MHz update rate and is optimized for direct digital synthesis and arbitrary-waveform-generation applications. Data and clock inputs are ECL compatible. The unit is housed in a 64-pin chip carrier and operates over a 0 to 70°C range. From $250 (100). **Burr-Brown Corp,** Box 11400, Tucson, AZ 85734. Phone (800) 548-6132; (602) 746-1111. FAX (602) 889-1510. TWX 910-952-1111. **Circle No. 406**

Disk controller. The FDC37C65C+ disk-controller IC maintains all drive formats. The unit offers the same features as the industry-standard FDC7C65C floppy-disk controller, as well as additional 2.88-Mbyte support. The + designation represents the addition of a 16-byte FIFO and vertical-recording-format mode to the IC. C+ CMOS 5V device, $4.75 (25,000). **Standard Microsystems Corp,** 35 Marcus Blvd, Hauppauge, NY 11788. Phone (516) 273-3100. **Circle No. 407**

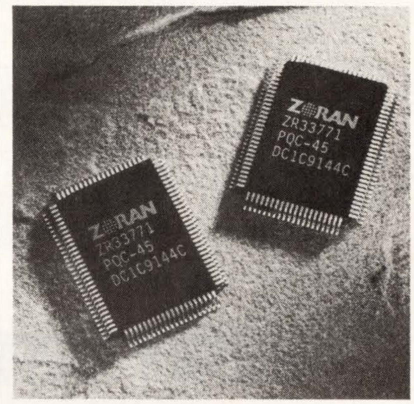
Latched drivers. MIC58PXX/MIC-59PXX 8-channel drivers feature overcurrent shutdown for each channel, overtemperature protection, and undervoltage lockout. The devices run at greater than 3 MHz and accept TTL or CMOS levels of 5 to 15V on the inputs. Off current is in the μA range. The separate logic and power grounds allow for power-level shifting or PIN diode driving with 5V logic and −5/+7V diode drive. $2.35 to $3.20 (100). **Micrel Semiconductor Inc,** 560 Oakmead Pkwy, Sunnyvale, CA 94086. Phone (408) 245-2500. FAX (408) 245-4175. **Circle No. 408**

FPGA. The A1225-1 features a capacity of 2500 gate-array-equivalent gates, 6250 PLD-equivalent gates, and 70 TTL-equivalent packages. The FPGA offers 451 logic modules, 383 flip-flops, and 83 user I/O. System speed equals 75 MHz, and 16-bit loadable counter-speed measures 85 MHz. In ceramic pin-grid arrays, plastic quad flatpacks, and plastic leaded chip carriers, $88 to $187 (100). **Actel Corp,** 955 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 739-1010. FAX (408) 739-1540. **Circle No. 409**

Read channel chip. The FC3560 contains analog and digital circuitry; it provides a pulse detector, four gated servo peak detectors, bandgap reference, a data synchronizer, a frequency synthesizer, and oscillators. The unit also contains an uncommitted digital gate (800 gates max) that users can employ to generate digital functions, such as encoder-decoder and address mark. Preconfigured version of FC3560, the ML6010, $7 (production qty). **Micro Linear Corp,** 2092 Concourse Dr, San Jose, CA 95131. Phone (408) 433-5200. **Circle No. 410**

A/D converters. The SPT family incorporates TTL- and ECLK-compatible converters. The 10-Msample/sec SPT-7920 and 30-Msample/sec SPT7922 have ECL-compatible I/Os. Both units are compatible with TTL and CMOS. ECL-compatible units dissipate less than 1.4W; TTL/CMOS devices dissipate less than 1.1W. Output-data format is straight binary with an overrange signal to indicate overflow conditions. $150 to $250. **Signal Processing Technologies Inc,** 1510 Quail Lake Loop, Colorado Springs, CO 80906. Phone (719) 540-3999. FAX (719) 540-3970. **Circle No. 411**

Video-rate convolver. The ZR33771-45 performs 2-D filtering functions at 45 MHz. The unit operates on 8-bit data with 9-bit kernel coefficients. For maximum flexibility the device supports multiple filter-kernel sizes ranging from 2×2- to 7×7-in. on-chip, double-buffered register banks. In 100-pin plastic quad flatpacks or 84-pin pin-grid arrays, $39 (OEM qty). **Zoran Corp,** 1705 Wyatt Dr, Santa Clara, CA 95054. Phone (408) 986-1314. FAX (408) 986-1240. **Circle No. 412**



PC-based IC programmer. The Sprint Optima programmer is small enough to fit in the palm of your hand. Unlike small programmers that have their own interface cards, it connects to a PC's printer port, so you can easily move it from PC to PC. Moreover, the parallel interface downloads data much faster than serial interfaces do. The unit's small size makes for more than easy portability; it limits the length of internal leads and minimizes both lead inductance and ground bounce. Ground bounce during programming is responsible for a significant portion of the instances of ICs' failing to program correctly. $3495. **SMS North America Inc,** Box 3159, Redmond, WA 98073. Phone (206) 883-8447. FAX (206) 883-8601. **Circle No. 377**

C-size VXI mainframe. The E1401A device provides 650W at 55°C—more than 50% more power than its predecessor could supply. A separate fan is dedicated to cooling the power supply. You can replace the supply from the rear of the mainframe with just a screw driver and without disturbing any of the instrument modules. E1401A, $6350; E1492B, including mainframe and VXI command module, $8750. Delivery, four to six weeks ARO. **Hewlett-Packard Co,** 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 452-4844. **Circle No. 378**

1-GHz spectrum analyzer. The SSA1000A analyzer operates from 150 kHz to 1 GHz with a frequency accuracy of ±10 kHz. It features a quasi-peak detector, a wideband or narrowband AM/FM receiver, and an RF preamplifier for off-the-air monitoring. The narrowest resolution bandwidth is 1 kHz; the widest is 2 MHz. An internal 4-color plotter provides screen printouts. $6950. **Wayne Kerr Inc,** 600 W Cummings Park, Woburn, MA 01801. Phone (800) 933-9319. FAX (617) 933-9523. **Circle No. 379**

DAC-per-pin IC programmer. You can upgrade the Allpro-4i from an initial complement of 24 pins to 40 pins and more. Each pin can slew voltage, slew current, sense voltage, sense current, and drive programming clocks to 4 MHz. $1295 for a 24-pin unit with software for programming logic devices only; $1495 for 32 pins and software for memory devices only; $2495 for 40 pins and software for memory and logic devices. **Logical Devices Inc,** 1201 NW 645th Pl, Fort Lauderdale, FL 33309. Phone (305) 974-0967. **Circle No. 380**

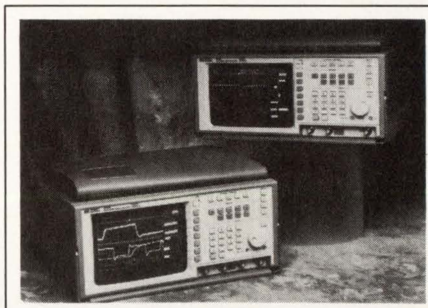
Thermal-imaging system. The IQ 325 detects, measures, and aids in analyzing infrared radiation. Its resolution is high for a system using a thermoelectrically cooled detector. The system includes both hard-disk and floppy-disk drives, allowing the analysis of images in real time or after acquisition. From $47,500. **Flir Systems Inc,** 16505 SW 72nd Ave, Portland, OR 97224. Phone (503) 684-3731. FAX (503) 684-5452. **Circle No. 381**

VXIbus digital I/O modules. The 128-channel, C-size IO100VXI, IO110VXI, and IO120VXI all use 74ACT CMOS input receivers. The first unit uses 74F TTL drivers; the second uses 74ACT drivers; and the third uses open-collector TTL drivers. The first two units have 16 3-state-control lines. The third has 16 output-enable lines. All inputs are latched and all outputs are double latched, permitting all outputs to change state at once. You can assign channels to 1- to 32-bit-wide groups of your own choice. Eight lines perform input handshaking; eight others perform output handshaking. IO100VXI and IO110VXI, $1995 each; IO120VXI, $2500. **Interface Technology,** 196 University Pkwy, Pomona, CA 91768. Phone (714) 595-6030. FAX (714) 595-7177. **Circle No. 382**

VXIbus programmable attenuator. Various members of the 7250 Series operate in four frequency ranges from dc to 26 GHz. You can set the attenuation from 0 to 132 dB in 1-dB steps (10 dB optional) via a 2-port register. The units are single-width C-size modules. $5495. Delivery, six weeks ARO. **Racal-Dana Instruments Inc,** 4 Goodyear St, Irvine, CA 92718. Phone (800) 722-3262. FAX (714) 859-2505. **Circle No. 383**

IC evaluation system. The Logic Master ATS125 tests digital and mixed-signal ICs. It delivers clock rates to 125 MHz, data rates to 250 Mbps, and typical edge-placement accuracies to ±400 psec. You can upgrade the system to the vendor's higher performance ATS200 and use the same fixturing and software as the vendor's Logic Master XL series. $2200 to $2800 per pin. **Integrated Measurement Systems Inc,** 9525 SW Gemini Dr, Beaverton, OR 97005. Phone (503) 626-7117. FAX (503) 644-6969. **Circle No. 384**

500-Msample/sec DSOs. The 2-channel 54505B and 4-channel 54506B provide 125-MHz single-shot bandwidth and 300-MHz repetitive-waveform bandwidth. Reconstruction filtering minimizes the uncertainty in displays of single-shot events. Waveform-memory depth is 8 ksamples/channel. The scopes perform signal-processing func-



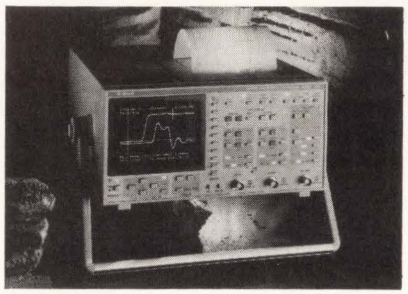
tions such as computing FFTs and integrating and differentiating waveforms. The DSOs also trigger on 5-nsec glitches, perform mask testing, and compute measurement statistics such as the mean of a group of readings. The

54505B, $8350; 54506B, $13,990. Delivery, 8 to 12 weeks ARO. **Hewlett-Packard Co,** Box 58059, MS 51L-SJ, Santa Clara, CA 95051. Phone (800) 452-4844. **Circle No. 385**

Handler for IC programming, testing, and marking. The benchtop-mounted Model 6000 automates existing PLD programmers. It works with several brands and models. It lets you change device setups in less than 5 minutes. From $30,000. **Exatron Automatic Test Equipment,** 2842 Aiello Dr, San Jose, CA 95111. Phone (800) 392-8766; (408) 629-7600. FAX (408) 629-2832. **Circle No. 386**

Evaluation board for DSP56401 audio transceiver. The 600-01497 board lets you put the DSP56401 through its paces. The chip includes interfaces to balanced, unbalanced, and optical transmission media, as well as ports that communicate with several Motorola DSP μPs, including the DSP56156, which incorporates a sigma-delta ADC. The board also includes interfaces to ADCs used in multimedia and professional audio applications. A dc/dc converter accepts 5V dc and supplies all dc voltages the board needs. $495. **Spectrum Signal Processing Inc,** 3700 Gilmore Way, Suite 301, Burnaby, BC V5G 4M1, Canada. Phone (800) 663-8986; (604) 438-7266. FAX (604) 438-3046. **Circle No. 387**

200-Msample/sec portable DSO. The 475 scope provides 200-MHz repetitive-signal bandwidth and 8-bit vertical resolution. The maximum sample rate, which governs the scope's usable single-shot bandwidth, is higher than that of other DSOs in its price range. The full 200-MHz bandwidth applies even on the 2-mV/div range. Options include a built-in 4-color plotter and an IEEE-488/RS-423 interface that supports the SCPI syntax (standard commands for programmable instruments). The 14-lb unit accepts power from the ac line or from a 12 to 33V dc source. From $3990. **Gould Inc,** 8333 Rockside Rd, Valley View, OH 44125. Phone (216) 328-7000. FAX (216) 328-7400. **Circle No. 388**

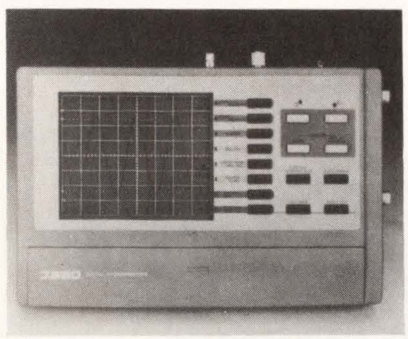


1-Msample/sec, 6U VME/VXI data-acquisition board. The DVX 2504 provides eight differential inputs that have >86 dB of common-mode rejection at 60 Hz. It provides 14-bit resolution. A sequence controller, which includes 2 kbytes of channel-list memory, allows continuous data acquisition without host intervention. A 1024-word FIFO buffer ensures that processor and DMA latency won't cause data gaps. Data-dependent triggering initiates data collection upon detection of specific measured values. Dual-channel DMA lets you store pre- and post-trigger data in different areas of the host memory.

$4500. Delivery, 8 to 10 weeks ARO. **Analogic Corp,** 8 Centennial Dr, Peabody, MA 01961. Phone (508) 977-3000. FAX (508) 532-6097. TLX 6817144. **Circle No. 389**

252-kHz to 2-GHz signal generator. The HP 8643A exhibits maximum single-sideband phase noise of −130 dBc at 1 GHz with a 20-kHz offset from the carrier. Spurious signals are at least −100 dBc. The generator provides amplitude, frequency, and pulse modulation. $21,000; $15,500 with maximum output frequency of 1.03 GHz. Delivery, seven weeks ARO. **Hewlett-Packard Co,** 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 452-4844. **Circle No. 390**

4-channel, scanning DMMs. The MM100, MM100A, and MM200 digital multimeters, each of which is powered by a 9V battery, offer three display modes: 4 channels/$3\frac{1}{2}$ digits, 2 channels/$4\frac{1}{2}$ digits, and 1 channel/9 digits (MM100, MM100A). When measuring dc voltage, the error is ±0.2%. All models let you program each channel for manual or automatic ranging. The MM200 allows you to specify upper and lower resistance setpoints. A bar-graph mode presents a 1-channel, $4\frac{1}{2}$-digit display along with a 16-segment bar-graph display. The MM100 has a 200-mA range; the others have 2A ranges. $229.95. **Hub Material Co,** 33 Springdale Ave, Canton, MA 02021. Phone (617) 821-1870. **Circle No. 391**



2-channel, 8-bit-resolution LCD DSO. The P-3820 device measures 6×9.25×2 in. Its bandwidth is 2.4 MHz; it takes 20 Msamples/sec; and it has a 2k-word acquisition memory that stores 16 waveforms. The scope, which has a 3.25×4-in. screen, receives power from six AA cells or from an ac adapter. Interfaces include an RS-232C port (standard) and a printer interface (optional). The unit makes cursor-controlled voltage and time-interval measurements and marks its displays with the date and time. Less than $975. **Protek Inc,** Box 59, Norwood, NJ 07648. Phone (201) 767-7242. FAX (201) 767-7343. **Circle No. 392**

LAN monitor. The HP 4995A Lanprobe II instrument completely implements the Remote Network Monitoring Management Information Base (RMON MIB) standard, which aids in planning networks, diagnosing their faults, tuning their performance, and providing multivendor interoperability via the Simple Network Management Protocol (SNMP). Several SNMP software packages manage the LAN monitor. From $2595. **Hewlett-Packard Co,** 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 452-4844. **Circle No. 393**

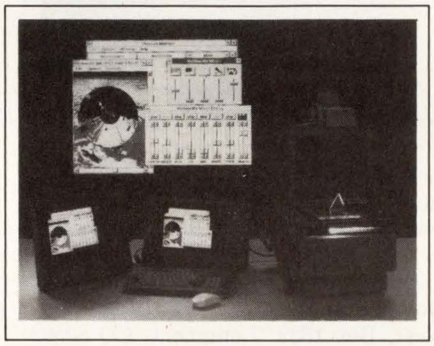
CIRCLE NO. 108

Computers & Peripherals

Flash memory cards. The IDE series memory cards have from 2.5- to 20-Mbyte capacity. The cards plug into an IDE-compatible base controller. The base controller accepts two removable cards for a maximum capacity of 40 Mbytes. The units replace a 2.5-in. hard-disk drive without requiring a change in the system BIOS. IDE base controller, $375; 2.5-Mbyte card, $425; 20-Mbyte card, $2750. **AT&T Microelectronics,** Dept 520404200, 555 Union Blvd, Allentown, PA 18103. Phone in US (800) 372-2447, ext 840; in Canada, (800) 553-2448, ext 840; (908) 771-2788.
Circle No. 355

R4000 computers. The ARCsystem family of computers consists of two product lines—the Magnum 4000 and the Millennium 4000. Both product lines employ a 50-MHz R4000 RISC (reduced-instruction-set-computer) CPU. The company will upgrade them to 67- and 75-MHz CPUs later in the year. The products deliver from 40 to 60 SPECmarks and run on qualified Windows NT and Unix operating systems. Software development models have a 15-in. flat color monitor, 1024×768-pixel XGA graphics, 8 Mbytes of RAM, a 200-Mbyte hard-disk drive, a CD-ROM, and floppy-disk drives. Magnum 4000, $9990 to $14,990; Millennium 4000, $10,990 to $15,990. **Mips Computer Systems Inc,** 950 DeGuigne Dr, Sunnyvale, CA 94088. Phone (408) 720-1700. FAX (408) 524-7950. **Circle No. 356**

50-MHz i486 computer. The ME 486-50 computer contains 4 Mbytes of RAM, a 200-Mbyte hard-disk drive, a Hi-Color VGA card, and a monitor that displays 32,768 colors having a resolution of 800×600 pixels. It also has both 5¼-in. and 3½-in. floppy-disk drives, a mouse, DOS 5.0, and Windows 3.0. System RAM is expandable to 32 Mbytes using 70-nsec SIMMs (single-in-line memory modules). Desktop model, $3395; tower model, $3995. **Micro Express,** 1801 Carnegie Ave, Santa Ana, CA 92705. Phone (714) 852-1400. FAX (714) 852-1225.
Circle No. 357



Projector/monitor. The Prism is a 7-lb color thin-film-transistor (TFT) panel that serves dual roles as an overhead projector and a stand-alone monitor. A snap-on backlight cartridge converts the unit from an overhead-projection panel to a stand-alone monitor. The cartridge doesn't alter the unit's 15×12.5×2-in. dimensions. Features include 640×480 pixels, 0.33-mm pixel pitch, and a toggle-select color palette from 512 to 185,000 colors. $8495. **Dolch Computer Systems,** 372 Turquoise St Milpitas, CA 95035. Phone (408) 957-6575. FAX (408) 263-6305. **Circle No. 358**

Laser printer. The Laser Beam Printer produces 300-dpi resolution. The unit has nine scalable or eight bit-mapped fonts. The printer has 512 kbytes of RAM, expandable to 2.5 Mbytes, and a 1-kbyte input buffer. The unit prints at 4 pages/minute and emulates a Diablo 630 printer. $1249. **Canon USA Inc,** 1 Canon Plaza, Lake Success, NY 11042. Phone (800) 848-4123. **Circle No. 359**

Printer accelerator. The Betteryet IV device for HP Laserjet Series II and Laserjet III printers consists of a board and cartridge that emulate PCL-5 and Postscript-compatible printers. The board automatically switches between the two emulation modes in network operations. It also provides an enhanced resolution of 600×300 dpi in both emulation modes. The board installs in the printer's optional I/O port, and the cartridge fits into the left font slot. $999. **Output Technology Corp,** 2310 N Fancher Rd, Spokane, WA 99212. Phone (800) 468-8788; (509) 536-0468. FAX (509) 533-1280. **Circle No. 360**

Programmable keypad encoder. The USE145 encodes the outputs of matrix keypads having from 1×23 to 12×12 keys. You can program the encoder to interface with an 8- or 16-bit ISA bus computer or an RS-232C port. A menu-driven utility program, called Usecon, lets you program pinouts and key codes. The encoder measures 2.5×3.6 in. and requires 5V for an RS-232C port. $145. **VG Controls Inc,** 34 Jenkins Rd, Hewitt, NJ 07421. Phone (201) 853-4600. FAX (201) 853-7913.
Circle No. 361

Windows accelerator board. The Winsprint 100 Plus employs the S3 86C911 VGA accelerator chip. It displays 1024×768 noninterlaced pixels having 256 colors at a 72-Hz refresh rate. A 1280×1024 interlaced pixel board having 16 colors is also available. The board is compatible with VGA and Super VGA standards. $595. **Artist Graphics,** 2675 Patton Rd, St Paul, MN 55113. Phone in US and Canada, (800) 627-8478, ext 814; (612) 631-7814. FAX (612) 631-7802. **Circle No. 362**

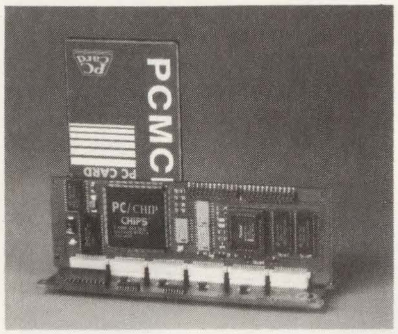
Macintosh LC accelerator board. The Tokamac ELC for Macintosh LC computers contains a 25-MHz 68EC040 CPU, which doesn't have a math coprocessor and a memory-management unit. The board's software automatically switches between the 68EC040 CPU and the Macintosh LC's 68020 µP. $1295. **Fusion Data Systems,** 8920 Business Park Dr, Suite 350, Austin, TX 78759. Phone (512) 338-5326. FAX (512) 794-9997. **Circle No. 363**

486 portable computer. The Model 120 Portable 486 contains a 33-MHz i486 µP; 4 Mbytes of RAM expandable to 32 Mbytes; a 3½-in. disk drive; a detachable keyboard; and Multilock security features. The computer uses thin-film-transistor (TFT), active-matrix, black-and-white display technology having VGA resolution to 64 shades of gray.

Two EISA expansion slots and an Enhanced Option Slot for graphics expansion are part of the unit. Model 120 with 120-Mbyte hard-disk drive, $5899; Model 210 with a 210-Mbyte disk drive will be available later this year, $6899. **Compaq Computer Corp,** Box 692000, Houston, TX 77269. Phone (713) 370-0670. **Circle No. 364**

Desktop plotter. The HI Jetpro Series Model V100 plotter produces 360-dpi resolution C-size drawings in less than 5 minutes. Because the unit supports PCX formatted files, it can plot FAX messages. The unit also works with TIFF, RLC, and CALS Group 4 formatted files to permit plotting of scanned raster images. The plotter emulates an IBM Proprinter to remain compatible with a range of word processors. $2995. **Summagraphics Corp,** 60 Silvermine Rd, Seymour, CT 06483. Phone (203) 881-5400. **Circle No. 365**

Computer board. The ESP 8680 Module contains Chips & Technologies' 8680 single-chip computer IC. It also has a



memory-card socket, CGA graphics, as much as 1 Mbyte of DRAM, a keyboard port, and a serial port. The board's form factor, called the Extremely Small Package, measures 1.7×5.2 in. $995. **Dover Electronics Manufacturing West,** Box 1532, Longmont, CO 80502. Phone (800) 848-1198; (303) 772-5933. FAX (303) 776-1883. **Circle No. 366**

SBus graphics accelerator. The model GXTRA/1 contains a Weitek W8720 integrated controller, 1-Mbyte color-frame buffer (8-bits), a Sun-4 keyboard and mouse port, and a SunOS CG3 device driver. The SBus board drives screens having resolutions from 640×480 pixels to 1152×900 pixels. The board accelerates graphics for Sun's X11/News, Sunview, and MIT's X11R4, and X11R5 software. $1750. **Tech Source Inc,** 442 S North Lake Blvd, Suite 1008, Altamonte Springs, FL 32701. Phone (407) 830-8301. **Circle No. 367**

Turbochannel-to-VME bus adapter. The adapter interconnects a DEC Turbochannel computer to a VMEbus system. The system consists of a Turbochannel card and a 6U VMEbus card that interconnect via a round 25-ft EMI shielded cable. Memory mapping permits either the Turbochannel or VMEbus host to execute random-access reads and writes on the other system. A DMA controller transfers 16-Mbyte blocks of data from one system to the other at 25 Mbytes/sec. The system also exchanges interrupts between the two buses. $2850. **Bit 3 Computer Corp,** 8120 Penn Ave S, Minneapolis, MN 55431. Phone (612) 881-6955. FAX (612) 881-9674. **Circle No. 368**

Ethernet print server. The XP-1 lets the company's printers become intelligent nodes on a Unix or DEC Ethernet network. The 2.5×9.5×11-in. box fits alongside the printer. It can handle transmission speeds of 3000 lines/minute. On DEC networks the unit operates with DEC Local Area Transport (LAT) protocol to share printer resources transparently. The unit also works with the TCP/IP (transmission-control-protocol/internet-protocol) suite. $1295. **Dataproducts,** Box 746, Woodland Hills, CA 91365. Phone (818) 887-8000. FAX (818) 887-4789.

Circle No. 369

Serial-communications board. The IV-3234 is a serial-communications controller board for the VMEbus. A 68EC030 microcontroller handles asynchronous and synchronous data rates as fast as 64 kbps on as many as 16 ports. When all ports are running bidirectionally at full speed, 90% of the CPU's power is held in reserve. The board runs under Vxworks, pSOS+, and OS-9 operating systems. You can optionally mount a daughter board containing a Z8530 4-port SIO chip for faster communications rates. $170/port. **Ironics Inc,** 798 Cascadilla St, Ithaca, NY 14850. Phone (607) 277-4060. TLX 705742.

Circle No. 370

Voice board. The DM1000LP-1 device can reproduce digitized messages as long as 2 minutes. It stores the messages in a 4-Mbyte EPROM. You can digitize voices using the company's 880 voice-development system or a voice-digitization service. A momentary grounding of a trigger pin begins playback. The board requires a 6 to 12V dc supply and draws 1 μA in standby mode. It can deliver 3W into an external 4 or 8Ω speaker. $30. Development system, $495. **Eletech Electronics,** 1262 E Katella Ave, Anaheim, CA 92805. Phone (714) 385-1707. FAX (714) 385-1708.

Circle No. 371

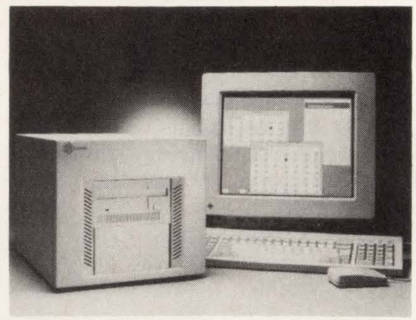
FDDI concentrator. The Fiberhub 1600 connects from 8 to 16 stations to a 100-Mbps FDDI network. The modular design lets you increase the number of ports in increments of two. The concentrator can handle any mix of fiber-optic or copper media and features "hot-swappable" modules. You can configure PHY and power-supply modules for dual-or single-attachment connections to another concentrator. You can also configure the unit for fault tolerance, using two MAC modules. $13,995. **Interphase Corp,** 13800 Senlac, Dallas, TX 75234. Phone (214) 919-9000. FAX (214) 919-9200.

Circle No. 372

Flat-panel operator. The Displaypac-cLCD contains a full-color LCD screen, a DOS-compatible 80386SX single-board computer, and a capacitive touchscreen. The LCD screen offers 512 colors and offers a low-cost alternative to an active-matrix thin-film-transistor (TFT) display found on competitive products. The 11.75×8.5×1.75-in. package runs at 25 MHz and contains 16 Mbytes of dynamic RAM, a VGA flat-panel controller, floppy- and IDE hard-disk controllers, and a battery-backed time clock. $2995. **Computer Dynamics,** 107 S Main St, Greer, SC 29650. Phone (803) 877-8700. FAX (803) 879-2030.

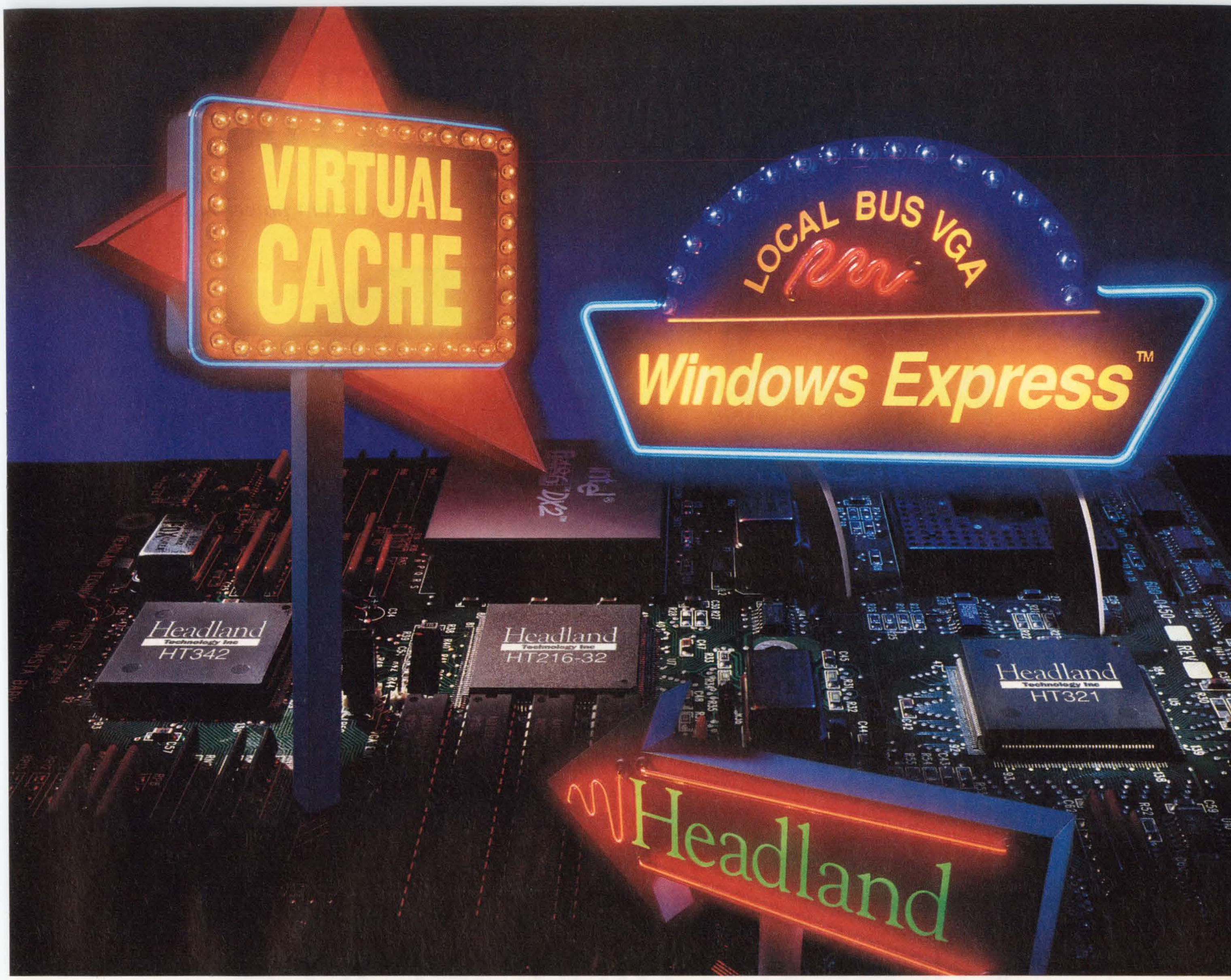
Circle No. 373

ISDN facsimile machine. The FAX-7000 G4 Group 4 fax machine has a built-in ISDN port. In addition, the company is offering the ISDN kit, which lets you add an ISDN port to FAX7000 computers. Both products provide a fax machine with both Group 3- and Group 4-compatible telephone numbers. The products let you transmit documents at 2 pages/minute where conventional phone lines transmit documents at 11 pages/minute. FAX7000 G4, $14,495; ISDN kit, $3500. **Ricoh Corp,** 5 Dedrick Pl, West Caldwell, NJ 07006. Phone (201) 882-2000. FAX (201) 882-2506. **Circle No. 374**



Rewritable optical-disk system. The OPTI/Max subsystem has an average access time of 7.6 msec. The subsystem, which runs on Unix workstations using the SCSI bus, consists of a 5¼-in. rewritable optical disk, a SCSI-to-SCSI caching controller, an uninterruptible power supply, and an enclosure. Each disk contains 600 Mbytes of storage. $5000 to $10,000. **Unison Information Systems Ltd,** 21 Walsh Way, Framingham, MA 01701. Phone (508) 879-3200. FAX (508) 879-0772. **Circle No. 375**

Audio board. The SX-15 ISA bus audio board provides direct-to-disk recording and playback of digitally sampled sound in real time. The board employs a TI TMS320C51 DSP chip having a 50-nsec cycle time. It lets you simultaneously record and play back two separate audio channels having 18-bit resolution and programmable sampling rates from 6.25 to 50 kHz. The board also meets the real-time compression requirements of industry file-format standards such as DVI, CD-I, and CD-ROM XA. $1895. **Antex Electronics Corp,** 16100 S Figueroa St, Gardena, CA 90248. Phone (800) 388-4231; (310) 532-3092. FAX (310) 532-8509. **Circle No. 376**



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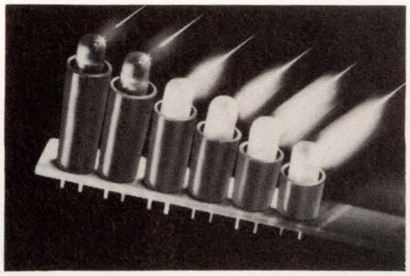

LEDs. BP280 Series T-1-¾ bi-pin LEDs are available in heights ranging from 0.5 to 1 in. The line includes 25 styles of diffused or high-intensity LEDs in red-yellow-cyan, orange, and blue—along with 12 styles of 5 and 12V units featuring an integral resistor. The family also includes three infrared versions. Operating characteristics range from 2 to 160 mcd; infrared units are rated for 1.4 to 80 mW/cm^2. From $0.45 (1000). **Ledtronics Inc,** 4009 Pacific Coast Hwy, Torrance, CA 90505. Phone (310) 549-9995. FAX (310) 549-4820. **Circle No. 413**

Keyboard. The KB-3050 84-position keyboard can incorporate a mouse key if desired. Measuring 10.5 mm high, the unit has the same feel as a keystroke of a full-size desktop keyboard. Keys include three full membrane sheets with a rubber dome. Keystroke equals 3 mm. $12 to $15. **NMB Technologies Inc,** 9730 Independence Ave, Chatsworth, CA 91311. Phone (818) 341-3355. FAX (818) 341-8207. **Circle No. 414**

Motor driver. The EDM-107 microstepping driver measures only 3×5.9×1.1 in. and handles 2 kW of peak output power. The unit features 14 programmable microstep ranges that can be changed on the fly. The 400- to 51,200-microstep/revolution range provides precise positioning. Short-circuit and overtemperature protection are standard. Less than $320 (100). **Portescap US Inc,** 36 Central Ave, Hauppauge, NY 11788. Phone (516) 234-3900. FAX (516) 234-3986. **Circle No. 415**

VME chassis. The VEV features 21 6U×160-mm slots as well as mounting and power for as many as four drives and a 500W power supply. The standard unit has a vertically mounted J1 backplane. Three fans cool the card cage and a fourth fan is dedicated to cooling the power supply. A power-switch-only control panel is standard; a panel with a system reset and ac-fail detect is optional. Versions with or without drive bays, $3850 and $3750, respectively. **Zoltech Corp,** 16658 Arminta St, Van Nuys, CA 91406. Phone (818) 780-1800. FAX (818) 780-1978. **Circle No. 416**

Radial capacitors. Type 2014S radial capacitors are available with values of 0.001 to 0.033 μF in standard tolerances of ±2, ±5, ±10, and ±20%. The units operate over a −25 to +85°C range and have voltage ratings of 1000, 1250, 1600, and 2000V dc. At 20°C, insulation resistance equals $4\times10^{10}\ \Omega$. From $0.15 (1000). Delivery, stock to eight weeks ARO. **Tecate Industries Inc,** Box 711509, Santee, CA 92072. Phone (619) 448-4811. FAX (619) 448-0912. **Circle No. 417**

Equipment towers. These VME towers hold 6U×160-mm boards. Air-flow dynamics allow air intake from the front and exhaust at the back. Cards are accessible from the tower front. The system is available in 3-, 5-, 7-, and 12-slot versions. All units come fully wired, tested, and ready to run with power supply, fans, and J1 and J2 backplanes. Drive bays are optional. A 3-slot version, $1668. **Bustronic Corp,** 44350 Grimmer Blvd, Fremont, CA 94538. Phone (510) 490-7388. FAX (510) 490-1853. **Circle No. 418**

Interference design kit. This EMI/RFI design kit has 20 compartments that are filled with selected ferrite components used to solve EMI/RFI problems. The kit's 200 pieces are ready for installation. Parts include single- and multihole beads, beads on leads, and 6-hole chokes. Specifications are provided for all parts. $50. **Ferronics Inc,** 45 O'Connor Rd, Fairport, NY 14450. Phone (716) 388-1020. FAX (716) 388-0036. TLX 256549. **Circle No. 419**

LIF connectors. N Series connectors are available with 70 to 350 contacts spaced on 0.1-in. centers. The contacts are rated for 3A and have a life expectancy of 100,000 operations min. Contacts for crimp, flow solder, wrapped-wire, and integral float mounting are available as standard. $30 to $150 (1000). Delivery, 14 weeks ARO. **Hypertronics Corp,** 16 Brent Dr, Hudson, MA 01749. Phone (800) 225-9228; (508) 568-0451. FAX (508) 568-0680. **Circle No. 420**

Detector module. FU-112PD detector modules operate in the 1000- to 1600-nm range and can function with either the FU-116SLD-1 or FU-116SLD-3 laser-diode modules. For 1300-nm wavelengths, the 116SLD-1 diode outputs 1.5 mW, and the 116SLD-3 unit outputs 0.2 mW. Operating range spans −40 to +85°C. FU-112PD, $95. Delivery, 14 weeks ARO. **Mitsubishi Electronics America Inc,** 1050 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 730-5900. **Circle No. 421**

Sockets. TAZ PGA ZIF sockets have a spring-loaded cover that keeps the empty socket in an open position. A hand tool activates the socket, eliminating the need for a space-consuming lever. The sockets are available in 0.1×0.1- and 0.05×0.1-in. contact-spacing versions. From $0.04 to $0.20 per line. Delivery, four to six weeks ARO. **AMP Inc,** Box 3608, Harrisburg, PA 17105. Phone (800) 522-6752. **Circle No. 422**

Memory-card connectors. IC5 Series 88-pin dynamic-RAM card connectors conform to PCMCIA, JEIDA, and JEDEC standards. The card-side receptacle has 1-mm-pitch surface-mount contacts in two staggered rows. The mating pin header has through-hole terminations. Connector life equals 10,000 cycles. Receptacle and header, $4.59 and $3.93, respectively (100). **Hirose Electric USA Inc,** 2685-C Park Center Dr, Simi Valley, CA 93065. Phone (805) 522-7958. FAX (805) 522-3217. **Circle No. 423**

Potentiometers. G3 Series surface-mount single-turn pots have a 100Ω to 1 MΩ resistance range. Tolerance equals 20%. The potentiometers are available in two styles; the A version has J-hook leads, and the B version has gull-wing terminations. Power rating

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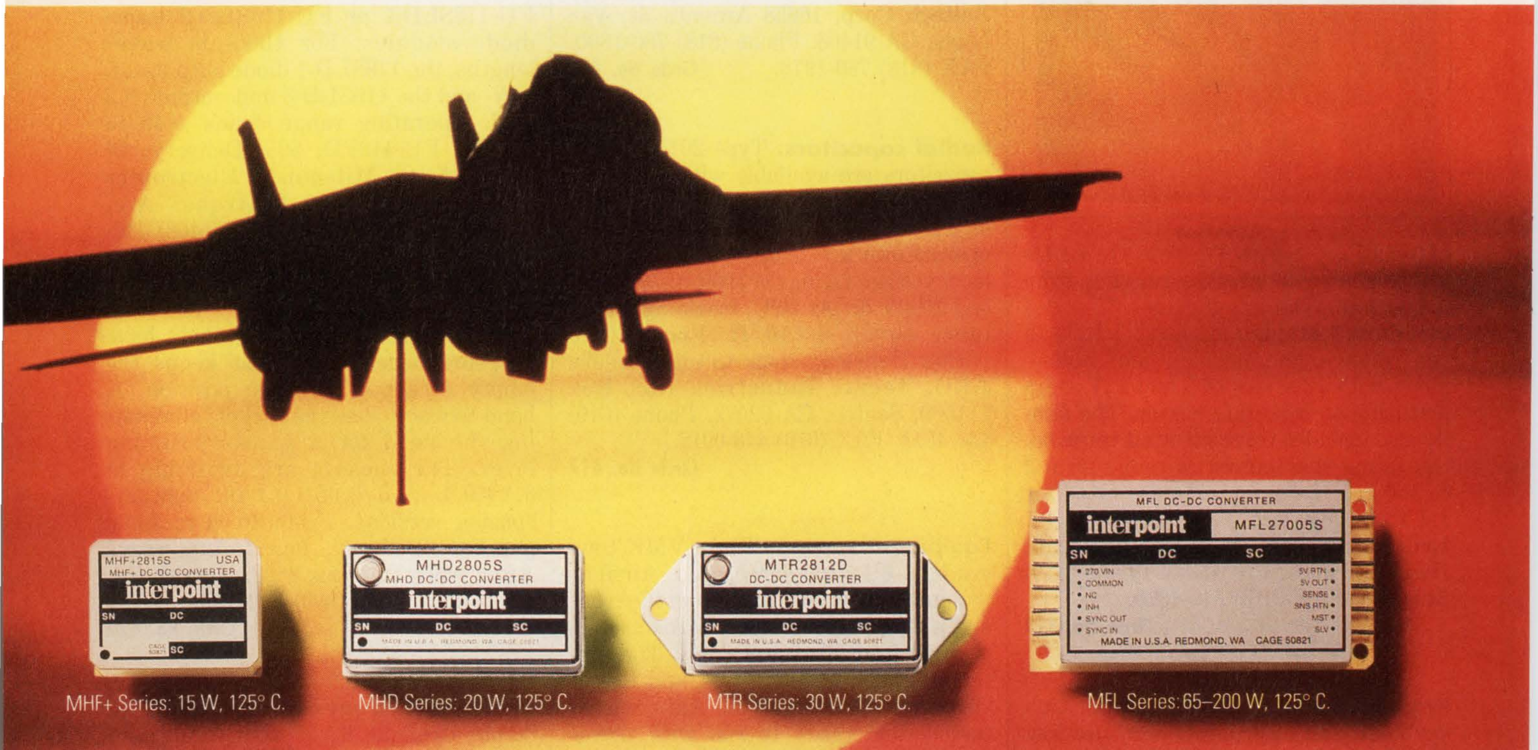

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equals 125 mW at 70°C, and operating range measures −55 to +125°C. $1.50 (1000). **Tocos America,** 565 W Golf Rd, Arlington Heights, IL 60005. Phone (708) 364-7277. **Circle No. 424**

Power transistors. CZT surface-mount power transistors are available in SO-223 packages. CZT5338 units are 5A 100V devices. The line also includes the CZTA44 unit with a 400 collector-to-emitter rating, and the CZT2000 200V Darlington transistor. All units have a 2W rating. $0.36 to $0.56 (1000). **Central Semiconductor Corp,** 145 Adams Ave, Hauppauge, NY 11788. Phone (516) 435-1110. FAX (516) 435-1824. **Circle No. 425**

Pin isolators. The Plecse-52-H is a plastic-leaded-chip-carrier pin isolator for electronic-hardware debugging. The isolators accept a device under development and plug into a socket on the target board. Switches on the pin isolator can isolate any one pin on the IC in the socket. Each switch has test pins on both sides, allowing monitoring of chip and board signals. $223. **EDI Corp,** Box 366, Patterson, CA 95363. Phone (209) 892-3270. FAX (209) 892-3610. **Circle No. 426**

Filters. CF-40000-1200-4-R bandpass filters operate at frequencies ranging to 40 GHz. Bandwidths of 3 to 25% of center frequency are available. Insertion loss equals 0.5 dB and VSWR measures 2:1 max. Filter impedance equals 50Ω. From $375. **RLC Electronics Inc,** 83 Radio Circle, Mount Kisko, NY 10549. Phone (914) 241-1334. FAX (914) 241-1334. **Circle No. 427**

Sockets. SMM Series 2-mm sockets suit vapor-phase and infrared soldering processes. The sockets measure 0.14 in. high and feature heat-treated beryllium copper, 4-finger contacts, and slotted tails. Optional retention clips and removable pick-and-place pads are available to improve automated assembly operations. From $0.05/pin. **Samtec Inc,** Box 1147, New Albany, IN 47151. Phone (800) 726-8329; (812) 944-6733. FAX (812) 948-5047. **Circle No. 428**

Pushbutton switches. PB1-3 and WP13 Series spdt switches feature contact ratings ranging from dry circuit to 6A at 125V ac. The unsealed PB units are available with various bushing and lighted or unlighted bezels. WP switches are totally sealed. PB units, from $2.56; WP units, from $2.73 (1000). **MORS/ASC,** Box 544, Wakefield, MA 01880. Phone (617) 246-1007. FAX (617) 245-4531. **Circle No. 429**

Coaxial adapter. The PE9136 is a female BNC-to-SMB jack adapter. It features a dc to 4-GHz range and operates from −65 to +165°C. The unit has a brass nickel-plated body, a gold-plated contact, and teflon insulation. $25.95. **Pasternack Enterprises,** Box 16759, Irvine, CA 92713. Phone (714) 261-1920. **Circle No. 430**

Transformers. IF Series pc-board transformers meet UL, CSA, IEC, and VDE standards. The transformers are available in 2- to 30-VA sizes. The units feature dual primaries and a secondary, which is wound alongside the primary rather than above the primary. A 4000V hi-pot is standard. \$7.63 to \$13.99 (100). **Signal Transformer Co Inc,** 500 Bayview Ave, Inwood, NY 11696. Phone (516) 239-5777. FAX (516) 239-7208. **Circle No. 431**

Panel meter. Series DPM-500 digital panel meters feature a 3-½-digit LCD. Features include low-battery warning, auto zero, auto polarity, and 200-mV FS display. The meter has a 0.1% ±1 count accuracy and can be mounted in a DIP socket. \$46.25. **Martel Electronics,** Box 897, Windham, NH 03087. Phone (603) 893-0886. FAX (603) 898-6820. **Circle No. 432**

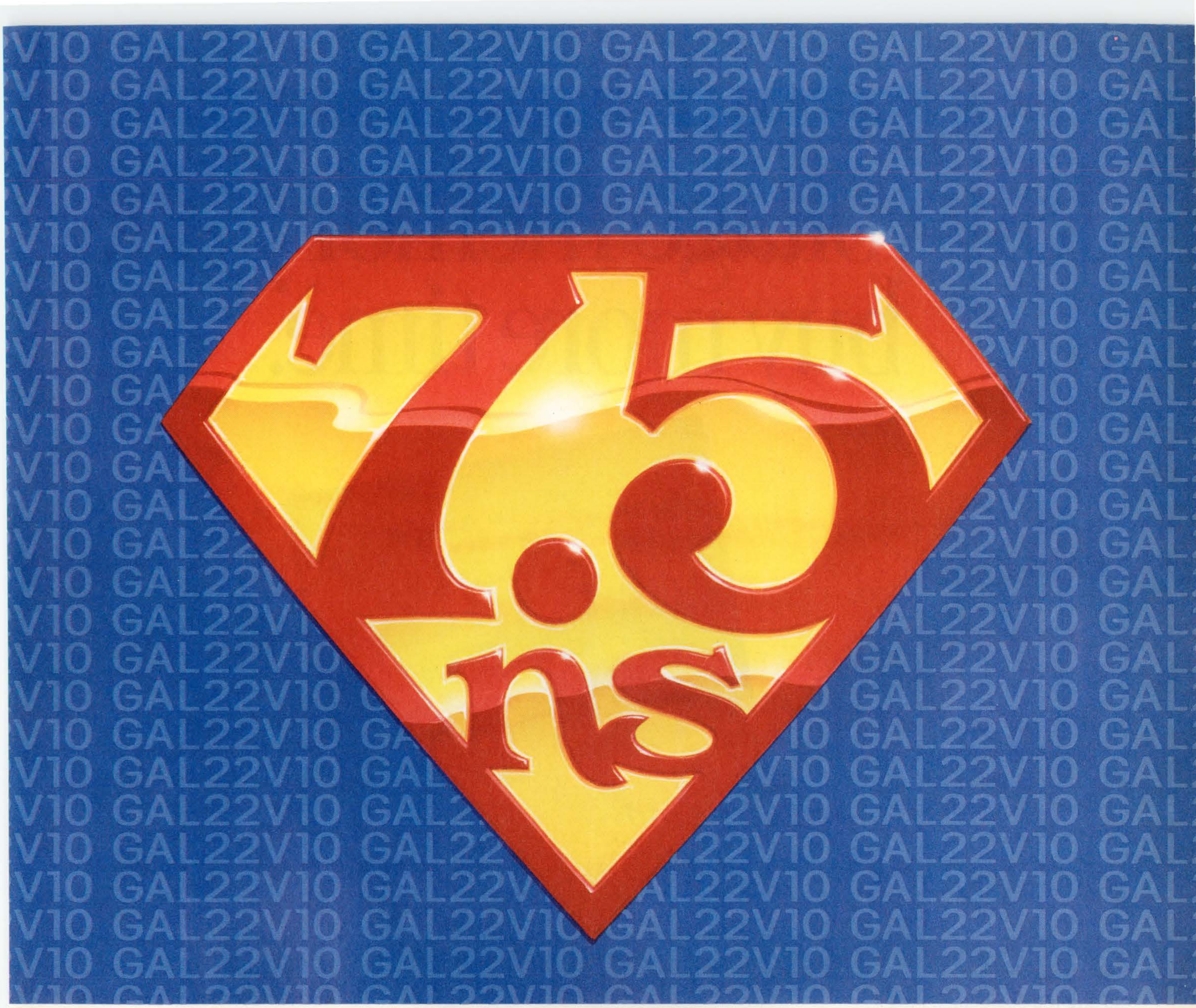
Heat sinks. These clip-on heat sinks are designed for the Intel 80486 and the Motorola 68040 µPs. The six standard models come with optional attachment clips and are available in straight-fin and pin-fin designs. Standard heights are 0.25, 0.35, and 0.60 in. Model 330011B00000 for the Intel µP has straight fins and provides 4.2°C/W thermal resistance. \$1.057 (1000). **Aavid Engineering Inc,** Box 400, Laconia, NH 03247. Phone (603) 528-3400. FAX (603) 528-1478. **Circle No. 433**

Servo amplifier. Model 303B has a 3-kHz bandwidth and operates as a current or voltage source. The unit develops ±6A continuous (±12A pk) at ±90V, measures 6.5×4×1.1 in., runs at 95% efficiency, and switches at 22 kHz. \$250 (100). **Copley Controls Corp,** 410 University Ave, Westwood, MA 02090. Phone (617) 329-8200. FAX (617) 329-4055. **Circle No. 434**

Toggle switches. These switches are available in spdt, spst, sp3t, dpdt, 3pdt, 4pdt, and dp3t versions. The panel-mount units feature coin-silver or gold-plated contacts. Contacts are rated for 5A resistive at 120V ac or 28V dc. Switch life equals 50,000 cycles, and operating range spans −30 to +85°C. \$0.68 to \$4 (1000). **CUI/Stack Inc,** 9640 SW Sunshine Ct G-700, Beaverton, OR 97005. Phone (503) 643-4899. FAX (503) 643-6129. **Circle No. 435**

Enclosures. VP series 3-slot VME enclosures feature a monolithic backplane and a card cage assembly. The 6U×160-mm cage provides direct access to VME-card front panels. The fan-cooled enclosures are available with either 80 or 130W power supplies, which provide outputs of ±5 and ±12V. \$1095. **Hybricon Corp,** 12 Willow Rd, Ayer, MA 01432. Phone (508) 772-5422. FAX (508) 772-2963. **Circle No. 436**

Optical connector. EC fiber-optic connectors have a 60-dB-min return loss and a 0.25-dB-typ insertion loss. The



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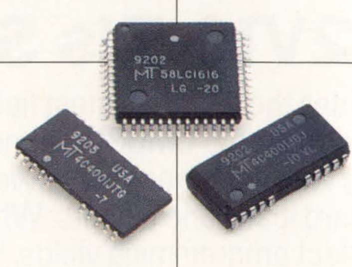
Part Number	Memory Configuration	Availability
3.3 Volt, Low Power, Extended Refresh DRAMs		
MT4C4001J VL	1 Meg x 4	3Q92
MT4LC4001 S*	1 Meg x 4	4Q92
MT4LC4001 L	1 Meg x 4	4Q92
MT4C4256 VL	256K x 4	Now
5 Volt, Low Power, Extended Refresh DRAMs		
MT4C1004J L	4 Meg x 1	Now
MT4C4001J L	1 Meg x 4	Now
MT4C8512 L	512K x 8	3Q92
MT4C16256 L	256K x 16 DW[1]	3Q92
MT4C16257 L	256K x 16 DC[2]	3Q92
MT4C1024 L	1 Meg x 1	Now
MT4C4256 L	256K x 4	Now
MT4C1664 L	64K x 16 FPM[3]	Now
MT4C1670 L	64K x 16 SC[4]	Now



Part Number		Memory Configuration	Availability
3.3 Volt, Low Power Specialty SRAMs			
MT5LC2818	Latched	16K x 18	Now
MT58LC1618	Synchronous	16K x 18	Now
MT5LC2516	Latched	16K x 16	Now
MT58LC1616	Synchronous	16K x 16	Now
5 Volt, Low Power, Low Voltage Data Retention SRAMs			
MT5C1001 LP		1 Meg x 1	Now
MT5C1005 LP		256K x 4	Now
MT5C1008 LP		128K x 8	Now
MT5C2561 LP		256K x 1	Now
MT5C2564 LP		64K x 4	Now
MT5C2565 LP		64K x 4 $\overline{OE}$[5]	Now
MT5C2568 LP		32K x 8	Now

*Self Refresh [1]DW– Dual Write Enable [2]DC– Dual $\overline{CAS}$ [3]FPM– Fast Page Mode [4]SC– Static Column [5]$\overline{OE}$– Output Enable

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CIRCLE NO. 120

units are easy to install and require no convex polishing. The connectors have a ±0.1-dB repeatability after 500 mating/unmating cycles and operate over a −40 to +85°C range. $40.30/mated pair (500). **Radiall Inc,** 150 Long Beach Blvd, Stratford, CT 06497. Phone (203) 386-1030. FAX (203) 375-3808. **Circle No. 437**

Combination meter. The P7000 features a 6-digit resolution and can be configured as a controller or a real-time clock. Standard features include configuration via the front panel or via the optional RS-232C or RS-485 communications boards. NEMA-4 front-panel and five configurable open-collector outputs for alarm or setpoints are also standard. $345. **Newport Electronics Inc,** 2229 S Yale St, Santa Ana, CA 92704. Phone (800) 639-7678; (714) 540-4914, ext 301. FAX (714) 546-3022. **Circle No. 438**

Resistor networks. PRN110 networks are housed in a 25-mil-pitch small-outline package. The devices are available in isolated and bused terminations and 16-, 20-, and 24-pin narrow-body-package configurations. Resistance values range from 10Ω to 1 MΩ, and tolerance equals ±0.1%. Temperature coefficient measures ±25 ppm/°C. $0.95 (10,000). Delivery, six weeks ARO. **California Micro Devices Corp,** 215 Topaz St, Milpitas, CA 95035. Phone (408) 263-3214. FAX (408) 263-7846. **Circle No. 439**

Telephone interconnect transformers. The surface-mount SPT-042 telephone interconnect transformers have a 600:600Ω impedance ratio and are designed for dry circuit applications. The transformers meet FCC and DOC specifications and have a 1500V-rms hi-pot rating. The units have gull-wing leads and are compatible with pick-and-place equipment. $4.18 (5000). Delivery, stock to six weeks ARO. **PREM Magnetics Inc,** 3521 N Chapel Hill Rd, McHenry, IL 60050. Phone (815) 385-2700. FAX (815) 385-8578. **Circle No. 440**

Power inductors. The pc-board-mountable inductors for power-supply applications come in 16 ratings with inductance values of 15 to 460 μH. Current ratings range to 16A. The inductors are available in two package sizes that feature molded standoffs to ease board cleaning. From $3 to $7.50 (500). **Microtran Co Inc,** Box 236, Valley Stream, NY 11582. Phone (516) 561-6050. **Circle No. 441**

LCD backlight system. This system employs a light-pipe system and a reflector board, as well as dual-chip, side-looking LEDs. Five standard sizes contain from 2 to 10 LEDs in green, yellow, amber, and red. Power requirements approximate 5V dc, and current draws are appropriate for the size of the units and number of LEDs used. From $2 to $15. **Lumex Opto/Components Inc,** 292 E Hellen Rd, Palatine, IL 60067. Phone (708) 359-2790. FAX (708) 359-8904. **Circle No. 442**

Test socket. The CA-QFE160S-Z-P tests 160-pin ICs housed in quad flatpacks (QFPs). The device comprises two pieces—the QFP emulator foot and the socket-test probe assembly. The emulator foot has the same footprint as the QFP device. $500. **Ironwood Electronics Inc,** Box 21151, St Paul, MN 55121. Phone (612) 431-7025. FAX (612) 432-8616. **Circle No. 443**

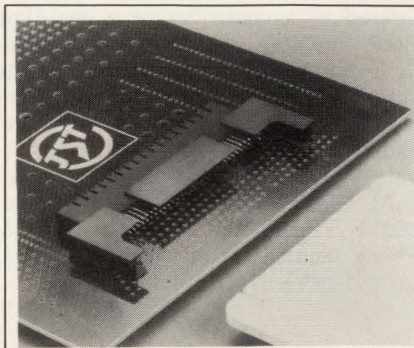
Pin adapters. These pin adapters are designed for testing 25-mil pitch surface-mount devices. The units will host emulators or pin-grid-array (PGA) devices on top of a socketed platform. The socket is mated to spring-loaded test probes and configured into 25-mil lead-spacing patterns. The units are available in generic PGA layouts or can be ordered for specific devices. From $807 (10). **ITT Pomona Electronics,** Box 2767, Pomona, CA 91769. Phone (714) 469-2900. FAX (714) 629-3317. **Circle No. 444**

Power supplies. SLR series supplies output 4000W. The power supplies offer as many as eight outputs and feature power-factor correction. The supplies feature $n+1$ redundancy and are available in militarized versions. From $925 (100). **Applied Power Conversion,** 100 School St, Bergenfield, NJ 07621. Phone (201) 385-0500. FAX (201) 385-0702. **Circle No. 445**

Double-balanced mixer. The SYM-860 double-balanced mixer operates over an 800- to 1050-MHz range. The surface-mount device has a 7-dBm LO drive and a 5.6-dB conversion loss. LO-to-RF and LO-to-IF isolation equals 39 and 37 dB, respectively. The mixer has a 2-tone, third-order IM intercept of 17 dBm. $8.95. **Mini-Circuits,** Box 350166, Brooklyn, NY 11235. Phone (718) 934-4500. FAX (718) 332-4661. TLX 6852844. **Circle No. 446**

Power supplies. TPG units have a 94 to 264V ac universal input and outputs of 5 and ±12V. Output currents range from 0.2 to 6A. Efficiency equals 65%, and all models are short-circuit and overvoltage protected. $40. **Total Power International Inc,** 418 Bridge St, Lowell, MA 01850. Phone (508) 453-7272. FAX (508) 453-7395. **Circle No. 447**

Reed relays. Series 8200 relays are housed in single in-line packages and come in four standard models with a 5 or 12V coil voltage and 10 or 50W switching options. The relays feature a 2000V dielectric isolation. The units are potted in a thermoplastic polyester shell with hermetically sealed contacts. Mercury wetted contacts are available. From $0.70 to $1.49 (OEM qty). **Coto Wabash,** 55 Dupont Dr, Providence, RI 02907. Phone (401) 943-2686. FAX (401) 942-0920. **Circle No. 448**



Memory-card connectors. Series ICM-C connectors are designed for 0.050-in. pitch, 60-position memory cards. The receptacle contacts have independent twin-beam construction and have a 10,000-cycle life. The contacts are rated for 0.5A. The connectors are available for surface-mount and through-hole mounting. $0.05/mated position (OEM qty). **JST Corp,** 1200 Business Center Dr, Suite 400, Mount Prospect, IL 60056. Phone (800) 947-1119; (708) 803-3300. FAX (708) 803-4918. **Circle No. 449**

External supplies. PSA Series external supplies develop single outputs of 9.5 to 24V at 3 to 1.25A current levels. The supplies have a universal 90 to 264V ac input and a total line and load regulation of ±2% max. The supplies have safety approvals from UL, CSA, and TUV. $47. **Phihong USA,** 920 Hillview Ct, Suite 195, Milpitas, CA 95035. Phone (408) 263-2200. FAX (408) 263-2213. **Circle No. 450**

Temperature transmitters. The 87500 Series scalable transmitters mount on a standard DIN rail and come with built-in alarm relay. Features include ±0.05% accuracy, ±0.1% linearization, zero and span adjustments, and automatic upscale indication. $245. **S-Products Inc,** 35 Kings Hwy E, Fairfield, CT 06430. Phone (203) 331-9546. FAX (203) 335-2723. **Circle No. 451**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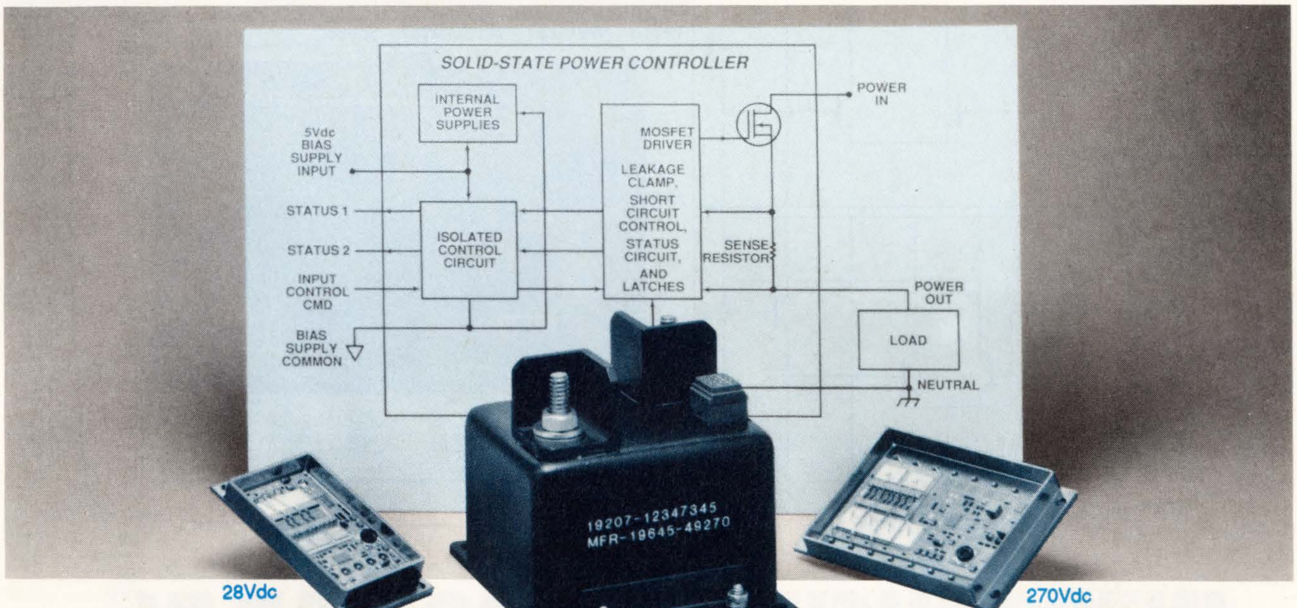

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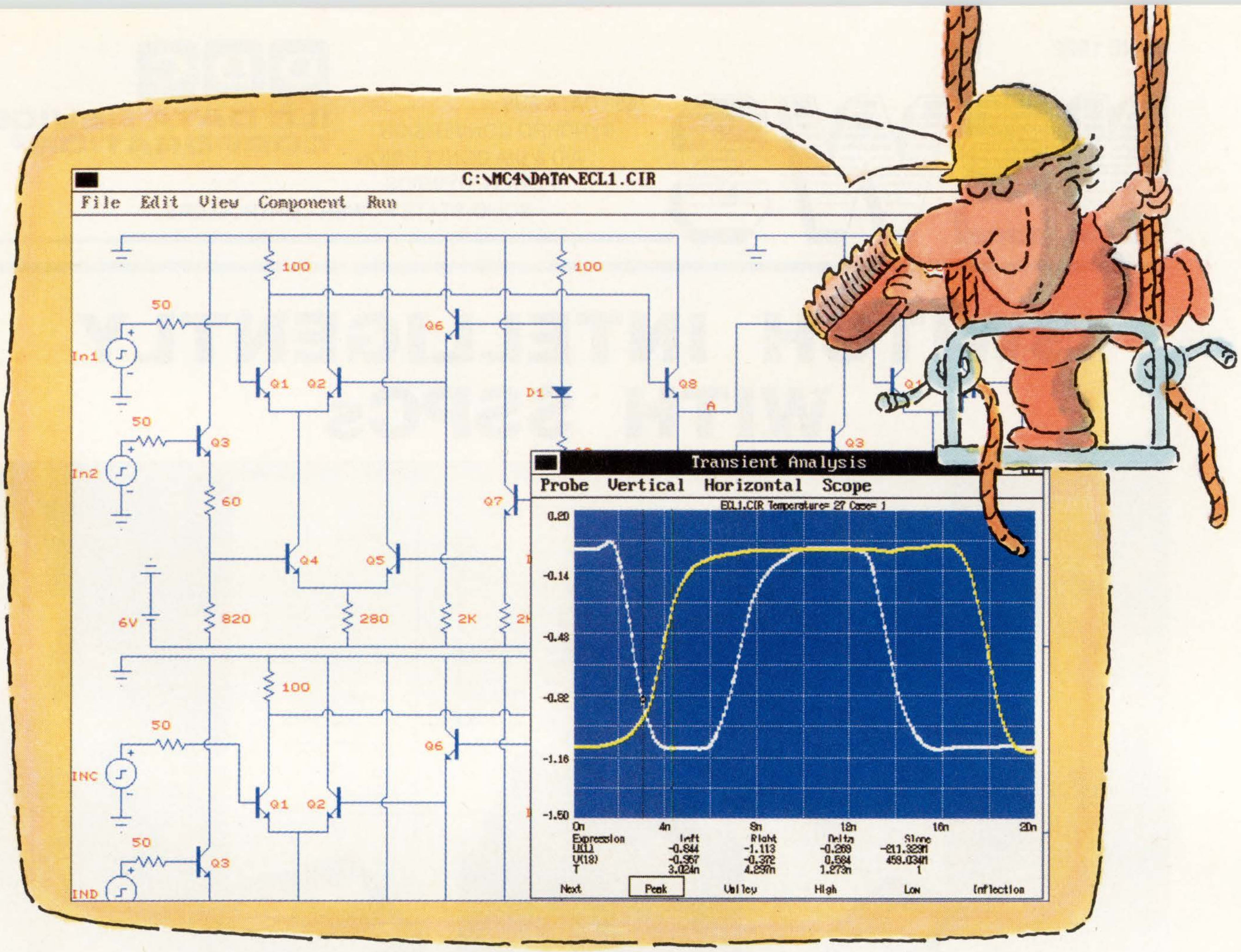

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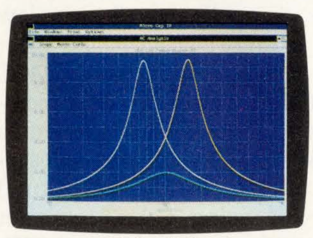

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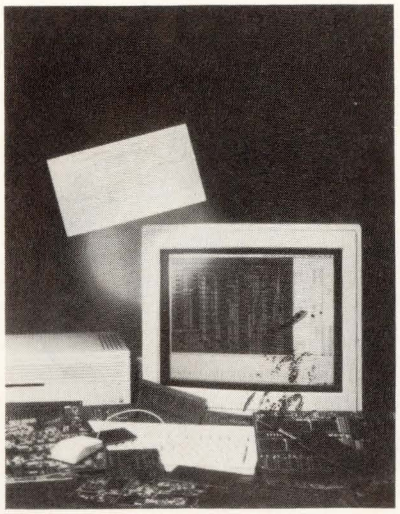
CAE & Software Development Tools



PC-board design for the Mac. The CAD/CAM Professional System for the MAC consists of three programs: Designworks, Professional Layout, and Autorouter. Using this software on the Macintosh, you design boards as large as 32×32 in. The software handles design from schematic entry through simulation, placement, and routing. Designworks, $995; Professional Layout, $1500; Autorouter, $700. **Douglas Electronics Inc,** 2777 Alvarado St, San Leandro, CA 94577. Phone (510) 483-8770. FAX (510) 483-6453. **Circle No. 452**

Data visualization for MS-Windows. Pointmaster runs under MS-Windows and lets you visualize scientific and engineering data. The software presents a WYSIWYG interface for data display, analysis, manipulation, and printing. As many as 20 simultaneous data sets appear on one page. $189. **Smoothvision Software Inc,** 15 Brandon Rd, Midland Park, NJ 07432. Phone (800) 832-0098; (201) 652-3839. FAX (201) 444-9127. **Circle No. 453**

DSP design software. DSP Station provides top-down design from software specification through simulation, including DSP-oriented silicon synthesis. You can choose cost/performance ratios, development, and production times by selecting from among several physical implementations including commercial DSP chips, gate-array or FPGA, and ASIC standard cell and module generators. For HP Apollo workstations, $33,000. **Mentor Graphics,** 8005 SW Boeckman Rd, Wilsonville, OR 97070. Phone (408) 436-1500. **Circle No. 454**

Layout editor for MS-Windows. The Gred layout editor for MS-Windows reads and writes GDSII stream format to import and export to other physical design tools. You use menus to access all commands for layout editing and manipulating data. The software uses MS-Windows to swap files and print features. It also provides 64 layers of each by name and number, sublayers, and text layers. $995. **Date Inc,** 10870 N Stelling Rd, Cupertino, CA 95014. Phone (408) 996-7600. **Circle No. 455**

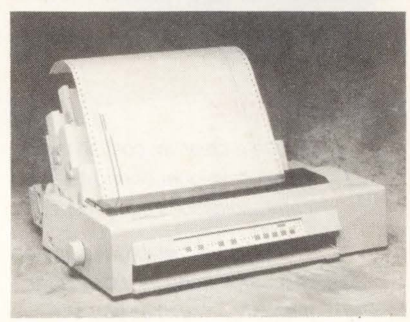
Call-processing board driver for OS/2 2.0. Engineers who are developing voice-processing systems using Dialogic hardware can use Dialogic OS/2 Driver to control hardware functions by programming in C. The driver's function libraries include commands to record and play back voice files, detect and dial DTMF tones, and perform telephony management functions. OS/2 2.0 is the 32-bit, 386-specific successor to IBM's 286-specific OS/2 1.x products. Driver annual license fee, $1250. **Dialogic Inc,** 300 Littleton Rd, Parsippany, NJ 07054. Phone (201) 334-8450. **Circle No. 456**

Three compilers for OS/2 2.0. The NDP Fortran, NDP C and C++, and NDP Pascal compilers take advantage of the Intel 386 architecture along with OS/2 to load and run 32-bit applications on the 386SX, 386, and 486. They are supposed to port 32-bit mainframe applications to the 386, 486, and i860. $595 each. **Microway,** Box 79, Kingston, MA 02364. Phone (508) 746-7341. FAX (508) 746-4678. **Circle No. 457**

Equation solver. TK Solver 2.0 lets users solve equations and create presentation-quality reports. Additions to the Presentation View tool display any number and combination of sheets of equations in WYSIWYG graphics. Users also edit, move, resize, and solve equations from Presentation view. Another addition is a macro tool for keystroke recording and playback. $595. **Universal Technical Systems Inc,** 1220 Rock St, Rockford, IL 61101. Phone (708) 291-1616. **Circle No. 458**

Remote computing for MS-Windows. Using a LAN, modem, or direct connection, Central Point Commute 2.0 provides access to MS-Windows, DOS programs, and files located on distant PCs. Instead of transferring full information about every bit map and pixel on the host display, the software taps into the video device driver on the host PC. From there it captures and sends high-level MS-Windows graphics commands, reducing the amount of data and time required for screen updates. The program automatically uses high, extended, or expanded memory. The program drives super-VGA monitors and works with MS-Windows drivers to 600×800 pixels. $129. **Central Point Software Inc,** 15220 NW Greenbrier Pkwy #200, Beaverton, OR 97006. Phone (800) 445-4208; (503) 690-8090. FAX (503) 690-8083. TLX 757710. **Circle No. 459**

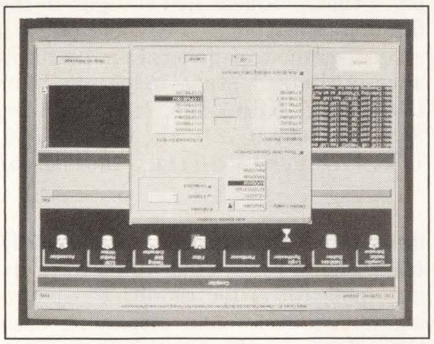
Macintosh-system utility tools. Central Point Mactools 2.0 gives data protection to Macintosh users and system administrators. Data protection, including data recovery, antivirus, and backup, can be done on a continual or scheduled basis. Scheduled processes include disk analysis and repair and backup. System start-up or shutdown can trigger these processes, and you can also schedule them to occur at daily or weekly intervals. $149. **Central Point Software Inc,** 15220 NW Greenbrier Pkwy #200, Beaverton, OR 97006. Phone (503) 690-8090. FAX (503) 690-8083. TLX 757710. **Circle No. 460**



C-size inkjet plotter. The HI Jetpro Series Model V100 plotter produces C-size drawings in less than 5 minutes so that you can review plots from your CAD system before committing them to vellum or another expensive medium. For comparison, a single CAD drawing can take about 20 minutes to 1 hour to plot on a pen plotter. The Jetpro plotter also prints fax messages and scanned raster images, reports, letters, and spreadsheets. $2995. **Summagraphics Corp,** 60 Silvermine Rd, Seymour, CT 06483. Phone (203) 881-5400. FAX (203) 881-5400. **Circle No. 461**

CIRCLE NO. 125

Development tools for Verilog HDL. Using Metatools for Verilog, you can develop and debug microcode, assembly code, or high-level-language software for processors and programmable devices being designed with Verilog. You can interactively debug the simulated hardware using symbolic referencing and disassembly, setting breakpoints and monitors, and examining source code and register contents as the Verilog simulation executes. Metatools provides a retargetable meta assembler optimized for vertical and horizontal microcode, a retargetable linker/loader, a utility for converting compiler-relocatable output to Metatools format, memory-management utilities, and trace-debug utilities. $10,000. **TD Technologies Inc,** 12608 Cedar Rd, Cleveland Heights, OH 44106. Phone (216) 371-9777. FAX (216) 371-9776. **Circle No. 462**



PLD software for Sun. You can use PLS-WS/SN software to develop progammable-logic software on a networked, client-server workstation. The software works with all of the company's EPLD (erasable-programmable-logic-device) families and can automatically partition large designs into components without requiring manual intervention. It runs on Sun SPARCstations and can operate across LANs to give project-wide access to any user equipped with an X-Terminal or desktop computer running the X11 protocol. The software also utilizes a Motif interface. Single floating license, $13,995. **Altera Corp,** 2610 Orchard Pkwy, San Jose, CA 95134. Phone (408) 984-2800. FAX (408) 435-1394. **Circle No. 463**

2-D electromagnetic field solver. The RLGC Parameter Generator uses the Spectral Domain Method to simulate transmission lines for high-frequency designs. Because the method eliminates the need to calculate the polarization charge at the dielectric interfaces, it allows the software to compute mode velocities accurately and reduce the matrix sizes and number of unknowns to be evaluated. Other features include correct modeling of the edge condition, handling of any number of dielectric layers and arbitrary conductor cross sections. PC version, $4500; HP or Sun version, $8400. **Contec Microelectronics USA Inc,** 2188 Bering Dr, San Jose, CA 95131. Phone (408) 434-6767. FAX (408) 434-6884. **Circle No. 464**

Open-parts-list system. The Capsure Preferred Parts List cross-reference option for the Computer-Aided Product Selection (CAPS) system allows users to link an arbitrary number of parameter/value pairs to part numbers. Using this feature, an engineer combines internal and proprietary data with commercial data. The user then extracts all data to a file to meet upstream and downstream requirements for design and manufacturing. Updated monthly,

the system gives engineers query-driven access via CD-ROM media to more than 700,000 parts and hundreds of thousands of manufacturers' datasheets, technical specifications, and application data. Base CAPS system in stand-alone PC version, $9000; Capsure option, $2000. **Cahners Technical Information Service Div,** 275 Washington St, Newton, MA 02158. Phone (617) 558-4960. FAX (617) 630-2168.
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Library of radar models. The Radar Library option to the Signal Processing Worksystem simplifies developing signal flow diagrams for radar-processing systems. The signal flow diagrams describe FFTs, filters, modulators, channels, and other functions that eliminate the need for handwritten DSP programs. The library includes six group models: target and clutter, pulse-compression waveforms, Doppler processing blocks, automatic detectors, components and subsystems, and radar-range, equation-scale factors. $3000. **Comdisco Systems Inc,** 919 E Hillsdale Blvd, Foster City, CA 94404. Phone (415) 574-5800. FAX (415) 358-3601.
Circle No. 466

Behavioral entry for Xilinx FPGAs. Xilinx-Abel, a Xilinx-specific version of Data I/O's Abel Design Software, is available for the Xilinx XC2000, XC3000, and XC4000 families. Designers can describe circuits by Boolean equations, state machines, and truth tables, or as functional blocks on schematic diagrams that reference logic described in the Abel Hardware Description Language. The software compiles and merges the various forms of design description to form a single output. The software also provides automatic "one-hot" encoding—also called "state per bit"—that produces fast designs in the flip-flop-rich Xilinx FPGA and offers a simple method of generating performance-optimized state machines. For DOS, $1495. **Xilinx Inc,** 2100 Logic Dr, San Jose, CA 95124. Phone (408) 559-7778. FAX (408) 559-7114. **Circle No. 467**

Real-time software tools for RS/6000. RTworks is a tool kit for developing applications for acquiring, analyzing, distributing, and displaying real-time data. Applications include real-time inferencing, dynamic graphical user interfaces, and client/server data distribution. Floating license, $35,000. **Talarian Corp,** 1043 N Shoreline Blvd, Suite 201, Mountain View, CA 94043. Phone (415) 965-8050. FAX (415) 965-9077. **Circle No. 468**

GUI development tool. The GIB Graphical Interface Builder generates both windowed interfaces resembling those of MS-Windows, as well as more general interfaces, such as instrument-control panels and process-control displays. Application code developed with the software runs on systems with as little as 512 kbytes of memory. DOS version, $475. **Tao Research Corp,** 39812 Mission Blvd, Suite 205, Fremont, CA 94539. Phone (510) 770-1659. FAX (510) 770-1659. **Circle No. 469**

Fractal compression software. P.oem Fractal Compress for MS-Windows accepts color images to $640 \times 400 \times 24$ bits/pixel and uses the fractal transform to compress them in

 CIRCLE NO. 127

software to a default image size. Depending on the compression mode selected and the size of the input image, compression can take from 20 sec to 6 minutes. The compressed image resides in a FIF (Fractal Image Format) file. Using the Fractal Formatter, the image can be viewed or converted to another image format. P.oem Fractal Compress, $198. P.oem Fractal Formatter, $99. **Iterated Systems Inc,** 5550A Peachtree Pkwy, Suite 545, Norcross, GA 30092. Phone (404) 840-0728. FAX (404) 840-0029. **Circle No. 732**

SCSI multitasking for MS-Windows. Future/CAM for Windows software has a 32-bit SCSI multitasking interface between MS-Windows 3.1 and Future Domain host adapters. It provides a virtual device driver that communicates directly with Future Domain SCSI host adapters, bypassing DOS and the PC BIOS for disk calls. The software simplifies interfacing multiple SCSI devices to MS-Windows under ISA, EISA, and Micro Channel Architecture buses. $200. **Future Domain Corp,** 2801 McGaw Ave, Irvine, CA 92714. Phone (714) 253-0400. FAX (714) 253-0913. **Circle No. 733**

Voice processing for MS-Windows. Remark! for MS-Windows is a server-based product that allows networked PC users to record, play, and manage voice information as part of any Windows application that supports DDE or OLE. Users can voice-annotate word-processing documents and spreadsheets with verbal comments, voice-script presentation graphics, and capture conversations, such as conference calls. The product requires no additional hardware for user PCs, and it uses a desk telephone for sound recording and playback. Configuration for 100 users, $10,500. **Simpact Associates Inc,** 9210 Sky Park Ct, San Diego, CA 92123. Phone (619) 565-1865. **Circle No. 734**

DOS graphing software. Sigmaplot 5.0 provides 3-D plotting for scientific data. You can create mesh and scatter plots using commands similar to those used in creating 2-D graphs. Further 3-D features include hidden-line removal, filled or unfilled polygons, frame lines, and backplanes with color and grids. $495. **Jandel Scientific,** 2591 Kerner Blvd, San Rafael, CA 94901. Phone (415) 453-6700. FAX (415) 453-7769. **Circle No. 735**

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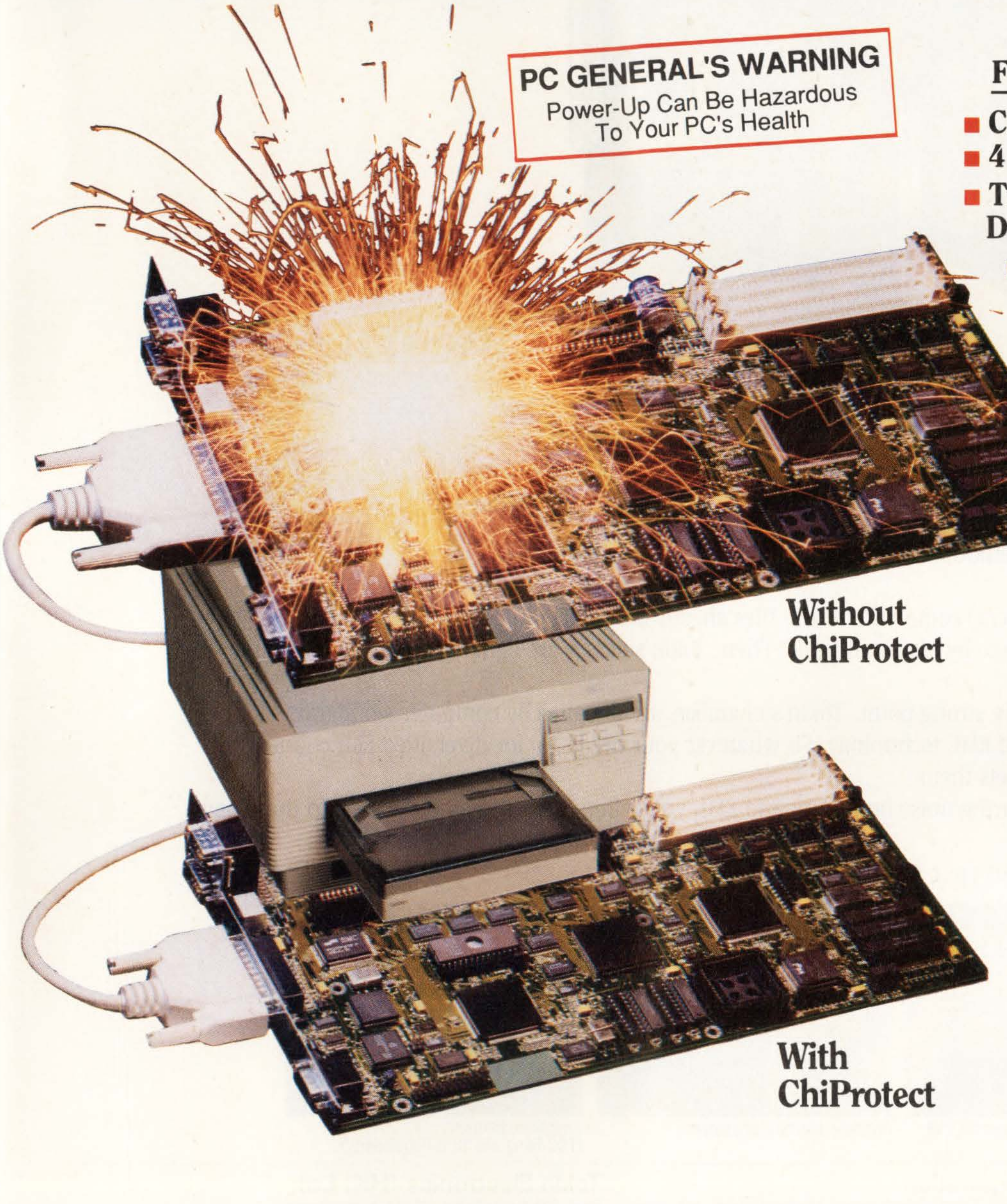

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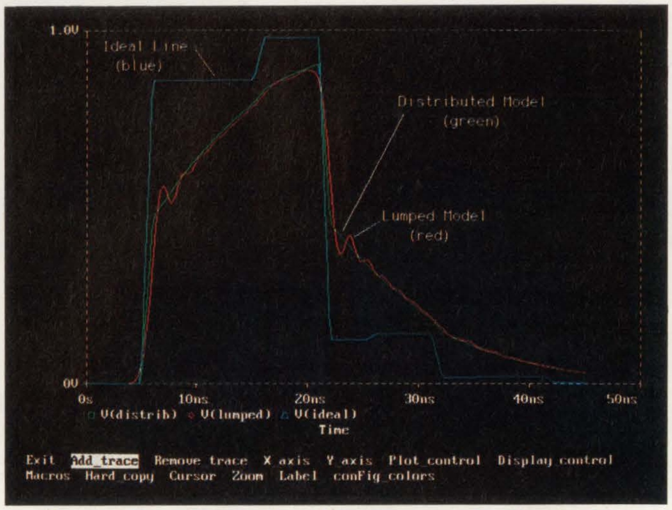

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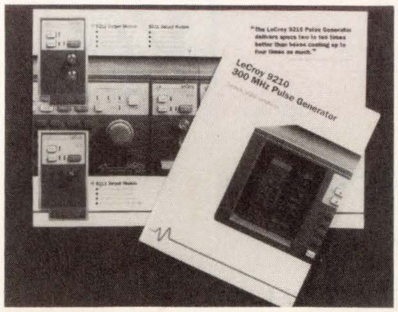
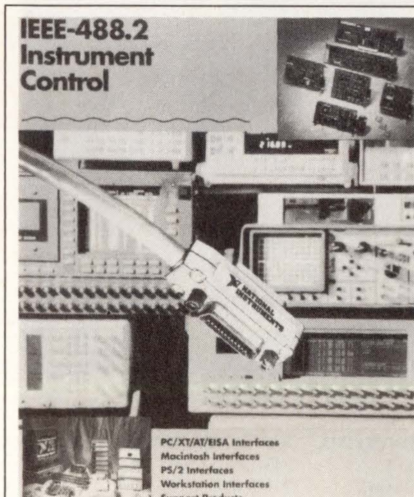
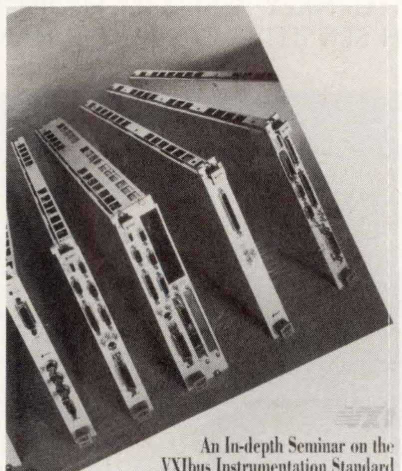


Brochure on pulse generator and plug-in modules. This publication features the 9210 pulse generator and the 9211, 9212, and 9213 plug-in modules. It describes straightforward controls, variable edge rates to 300 psec, automatic load compensation, high precision and accuracy, and IEEE-488 programmability. **LeCroy Corp,** Signal Sources Div, 700 Chestnut Ridge Rd, Chestnut Ridge, NY 10977. Phone (914) 425-2000. TWX 710-577-2832. **Circle No. 351**

DSP hardware and software. This 8-pg brochure presents DSP plug-in boards and software for PC/AT and Macintosh computers. It describes hardware for the AT-DSP2000, a DSP accelerator for high-accuracy analog I/O channels. It also discusses hardware for three Macintosh Nubus computers: the NB-DSP2305, the NB-DSP2300, and the NB-DSP2301. **National Instruments,** 6504 Bridge Point Pkwy, Austin, TX 78730. In US and Canada, phone (512) 794-0100. **Circle No. 352**

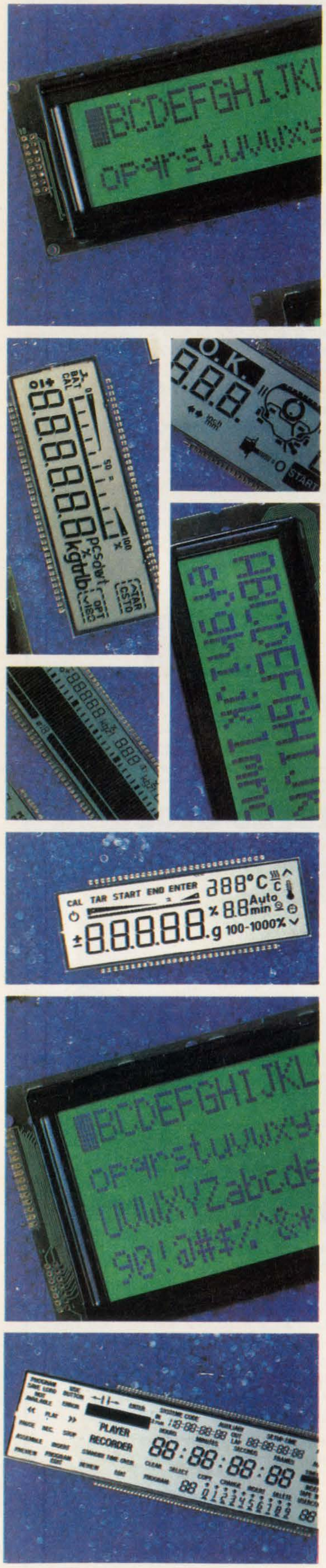


Pamphlet on IEEE-488.2 instrument control. This 8-pg brochure presents IBM PC/XT, PC/AT, EISA, and PS/2 interfaces; Macintosh interfaces; and workstation and industrial-bus interfaces. The publication also describes support products such as bus extenders and plug-in converters, and it provides two pages on software, including NI-488.2 for Windows. **National Instruments,** 6504 Bridge Point Pkwy, Austin, TX 78730. Phone in US and Canada, (512) 794-0100. **Circle No. 353**



Handbook for VXIbus instrumentation standard. The 92-pg handbook, *An In-depth Seminar on the VXIbus Instrumentation Standard*, summarizes the development of VXI and covers topics such as VXI backplanes and protocols. The handbook also explains how test engineers can combine embedded or external VXI hardware and software to build smaller test systems. The section, *VXI Specification*, includes VXI module sizes, mainframe and extension requirements, programming requirements, and different types of VXI devices. Two other sections deal with VXI system configurations and VXI software. **National Instruments Corp,** 6504 Bridge Point Pkwy, Austin, TX 78730. Phone in US and Canada, (512) 794-0100. **Circle No. 354**

Guide to nonprofit groups. The $7 *Electronic Networking for Nonprofit Groups*, jointly published by Apple Computer and the Benton Foundation of Washington, DC, guides nonprofit groups in the use of computer-based telecommunications networks. It explains how to access local bulletin boards run by single agencies, regional and national networks that deal with a variety of subjects, and international affairs and activities. **Apple Computer Inc,** 20525 Mariani Ave, MS 38J, Cupertino, CA 95014. Phone (408) 974-2974; (202) 857-7829, ext 21. **INQUIRE DIRECT**



The Enduring Appeal of Consulting

Kevin Bryan

Independent consulting has its drawbacks, but for some engineers it's the only way of life.

Jay Fraser, *Associate Editor*

"I never enjoyed working for a company," says Brian Bandhauer, who decided to become an independent engineering consultant almost two years ago. "It has to do with simple freedom, being able to choose my own hours and my own projects, what I want to do and when."

Bandhauer did what many engineers only think about doing. He left the corporate world behind and struck out on his own, pursuing that dream so dear to engineers everywhere: to be his own boss.

After he had worked at two small high-tech firms in Colorado, Bandhauer and his wife decided to move to the West Coast. They eventually settled in Corvallis, OR, because they liked the city, even though opportunities for engineers were scarce there. The situation gave Bandhauer the chance he'd always wanted—to go into business as a consultant. He has never regretted it. "I end up working a lot more, but I enjoy every second of it," he says. "I'm the happiest I've ever been."

"Consulting is a contact sport. You only make money when you're grappling with your clients." —**Ron Lang**

For some engineers, becoming a consultant isn't completely voluntary. Ron Lang worked for firms such as United Technologies, Becton-Dickinson, and Digital Equipment Corp before he joined a small, start-up array-processor company in Newton, MA. He became its chief financial officer because no one else wanted the job. "That was the turning point," says Lang. "I learned what accounting is all about, how to deal with bankers, and what a balance sheet is supposed to look like."

Four years later, the president of the company resigned. Lang notified the board of directors that he wanted to move up to that position. "I didn't get the job, and I was angry," he says. "It was held against me that I was an engineer, and I was very upset about that. I was on the technology side, not the marketing side, but I felt that I could run that company because of my experience. So I quit and hung out my shingle, and I can't tell you how happy I've been since."

Independence is the number one reason engineers give for becoming consultants. Ideally, consultants can choose their own assignments, decide how they will do the work, and make all the business arrangements themselves.

"I have the responsibility to close my own deals. I don't have to depend on people above me to close them," says Lang. "I pick the jobs I feel like quoting on, and I get to take 3-day weekends whenever I please."

Consultants also enjoy being able to work on many different kinds of projects. In a large high-tech firm, engineers may become locked into a small area of specialization. It's not unusual for an engineer to spend months or even years working on a single project. "I get to see a wide variety of engineers and engineering practices," says Bandhauer. "I'm learning more from being a consultant than I did in any single place that I worked."

A third reason engineers become consultants is they don't want to be bound by the wage structure of a corporation. They don't want to have to age their way up to a higher salary level. In theory, the amount of money consultants can earn is restricted only by how hard they work and how well they run their businesses.

The problems of consulting

Many engineers, however, don't realize how difficult it is to run a business. They have little idea how much time and energy they will have to spend on paperwork, bookkeeping, and prospecting for new clients.

William Billowitch is the president of his own consulting and product-development firm in Allentown, PA. Previously, he worked for a small software company that relocated to another state. Rather than uproot his family, he decided to remain where he was and start his own consulting business. At first he was surprised by how much time he needed to devote to nonengineering work.

"You probably need one day a week totally dedicated to making sure you're going to have something to do six months from now," he says. "When I began, I didn't understand that. I'd get a job and spend 100% of my time working on it. Then, when I got down toward the end of it, I'd realize that I had nothing in the pipeline. Now I set aside one day a week to call customers, follow up leads, take care of any administrative work, and make sure that when I'm done with one job there will be another one right behind it."

Another disadvantage to becoming a consultant is financial insecurity. Working for a corporation may be stifling sometimes, but it does provide a steady paycheck. Working for yourself may bring in money at irregular intervals. It's also possible that you won't make as much as you did as a salaried employee, especially during the time you're getting your business up and running.

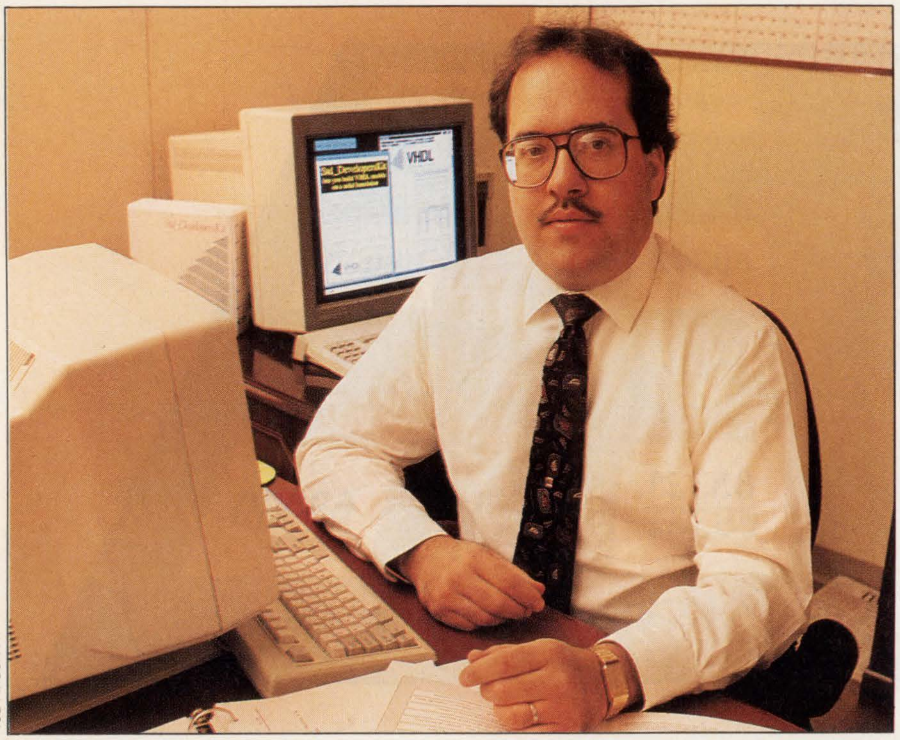
Brian Drake

"If I'm feeling burned out I may take off and go bike riding. You can't do that in a company."
—Brian Bandhauer

Your financial success or lack of it as a consultant can also depend on factors beyond your control. You may be a talented and knowledgeable engineer, but if the national economy is in recession, there may be simply no work available.

Big companies also supply other comforts and perks that you won't enjoy if you're a consultant. For example, you'll have to pay your own Social Security taxes and health-insurance premiums, and you'll have to provide for your own retirement. You'll also have to pay your travel and entertainment expenses and the tuition for any college courses you take. And when you're working for yourself, there's no such thing as a paid vacation.

"Consulting is a contact sport," says Lang. "You only make money when you're grappling with your clients. If I were to take two weeks off and fly to Honolulu, I wouldn't be making money. But, more impor-



Ted Anderson

"Establishing a high degree of recognition is the key to being a top consultant."
—William Billowitch

tant, there wouldn't be anybody here to answer the phone and help someone who's in trouble. You feel an obligation to your customers. It's almost like being a doctor."

Another unpleasant surprise that lies in wait for new consultants is that they can end up working long hours. "I tend to work seven days a week," says Bandhauer. "If I were to total it up, I probably put in 50 or 60 hours of actual hard-core work a week. But, on the other hand, come two o'clock in the afternoon, if I'm feeling burned out, I may take off and go bike riding. You can't do that in a company."

The projects consultants deal with are often different from the work an engineer usually sees in a high-tech company. After all, consultants are called in when something goes wrong or when a problem crops up that no one on the staff can solve. You may face resentment from a company's engineers if you've been called in to straighten out something they've handled badly.

As an independent consultant you may also miss the stimulation of working with other engineers every day. "For a year and a half, I operated out of my home. It gets lonely. There's no one to bounce ideas off," says Billowitch. "You can pick up the phone and call people, but it's not the same as getting a cup of coffee and walking down the hall and chatting about some technical problem with an associate."

Expertise is not enough

There are serious drawbacks to independent consulting, and some engineers try it for a while and then go back to work for a corporation. If you've ever thought about leaving your job to become a consultant, the first thing you should know is that engineering skills and expertise alone won't make you a success.

"I've always felt that consulting is 50% salesmanship and 50% execution," says Lang. "If you're an engineering genius but you can't sell yourself, you're dead. And if you can only sell yourself but not perform, you're also dead."

Salesmanship and the ability to manage a small business are only two of the nonengineering skills you need to succeed as a consultant. You must also know how to market yourself. You have to understand how your particular talents and knowledge fit the needs of the companies you deal with.

Many people believe that a consultant has to possess exceptional intellectual powers and stand head and shoulders above ordinary engineers. But that's not necessarily true.

"I have a specialty, and I have about five years' experience behind me, but I'm certainly not a superstar engineer," says Bandhauer. "I try to market myself toward the engineering places that are in a temporary crunch. They get too much work all of a sudden and they can't handle it, but they don't want to hire another guy, so they contract out. I'm trying to fill that need in the market."

Becoming a consultant requires a commitment. To be successful, you can't dabble in consulting; you must commit your time, energy, and even your money. If you work out of your home, you'll have to invest in office equipment and supplies, and perhaps in lab equipment too. For tax purposes, you might also want to incorporate yourself. Before you take the plunge into full-time consulting, it may pay to talk to a lawyer or an accountant about the best way to proceed.

If you're just starting off in consulting, it's crucial to make yourself known to potential clients and to other engineers who could refer clients to you. There are many ways to establish visibility. You can join professional organizations and net-

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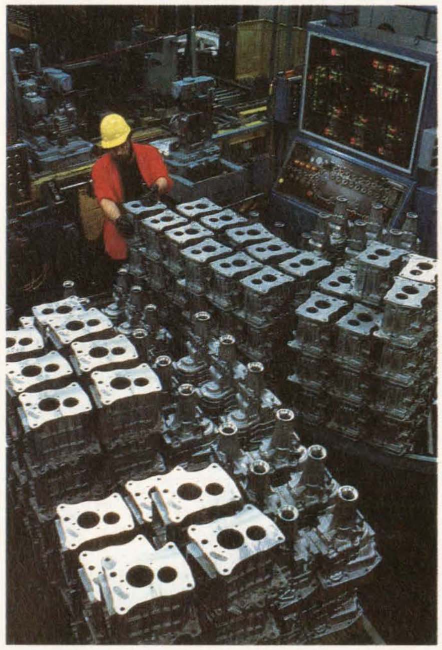

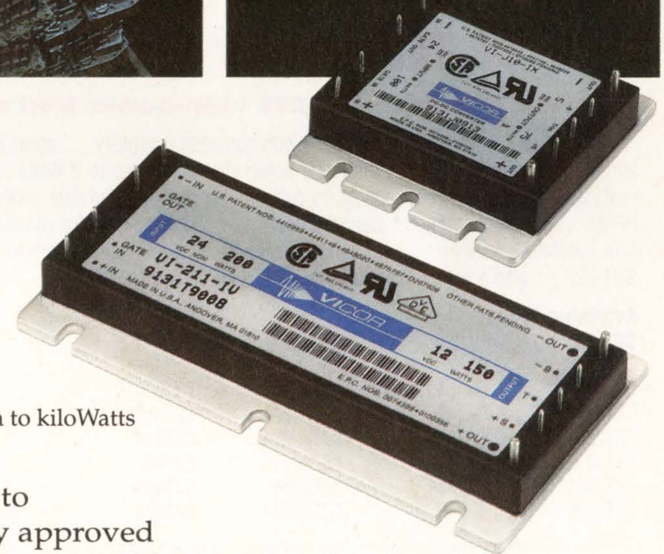

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work through them. You can present papers or give talks at technical conferences. You can publish articles in technical magazines.

In addition, you can join national organizations that are specifically for independent consultants, such as the Professional and Technical Consultants Association (San Jose, CA), the American Consulting Engineers Council (Washington, DC), and the Independent Computer Consultants Association (St Louis, MO). These organizations sponsor meetings and seminars to help consultants run their businesses, publish and circulate directories of their members, and provide services that match clients with their member consultants.

Consultants acquire most of their new clients through referrals. That means the most important asset a consultant can have is a good reputation. "You have to establish a personal reputation as being an expert in a field, and that generally involves being extremely active in a variety of organizations in your market niche," says Billowitch. "Establishing a high degree of recognition is the key to being a top consultant. There are a lot of people who are consultants, but very few are top consultants."

As with any profession, consulting has its pros and cons. The personal freedom, variety of projects, and opportunity for an increased income have to be weighed against the long hours, demands of running a business, and financial insecurity. But for some people, once they leave company life and get their first taste of independence, there's no turning back.

"I absolutely love consulting. The only thing that would ever make me leave it would be the possibility of losing my house," says Bandhauer. "I'd do it right up to that point before I'd go back to a corporation. But I'd make a lousy employee because as soon as things became stable, I'd take off and be a consultant again." EDN

Jay Fraser, Associate Editor, can be reached at (617) 558-4561, FAX (617) 558-4470.

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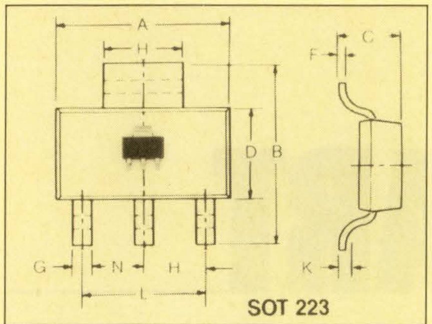

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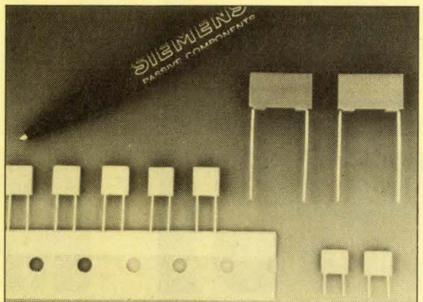

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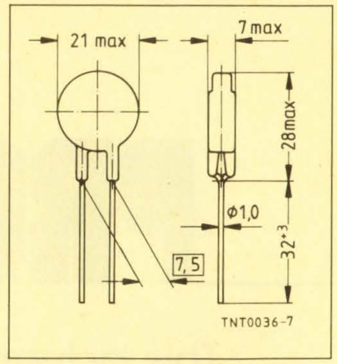

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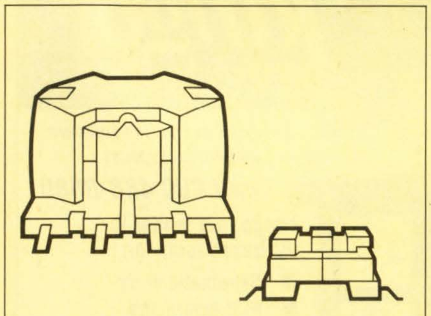

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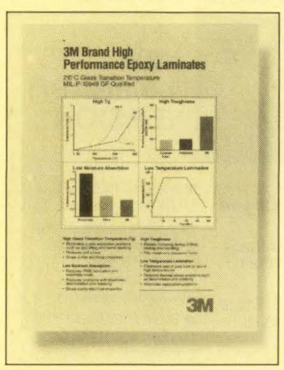

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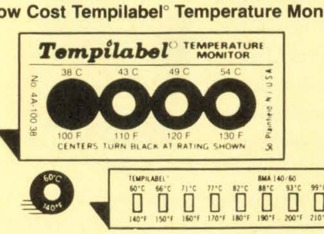

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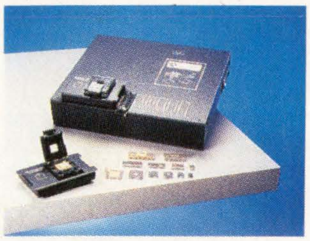

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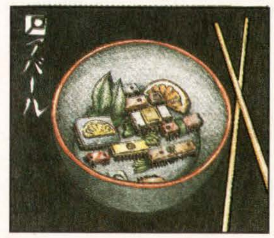

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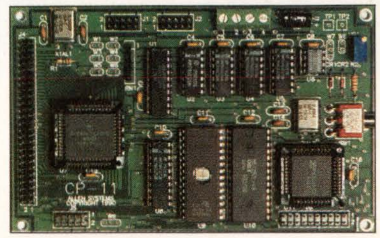

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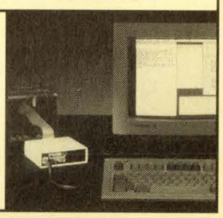

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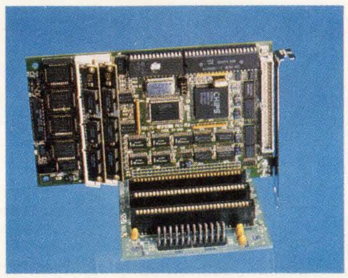

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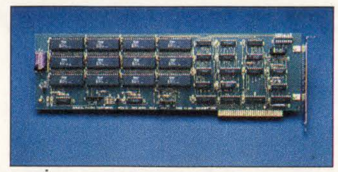

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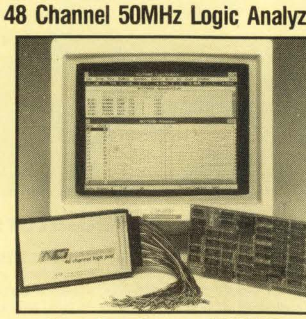

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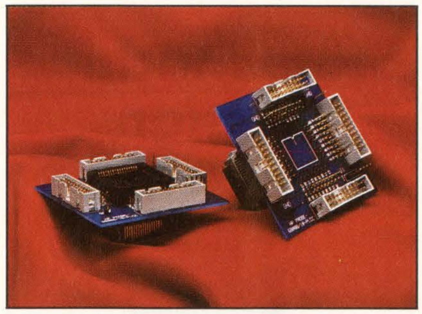

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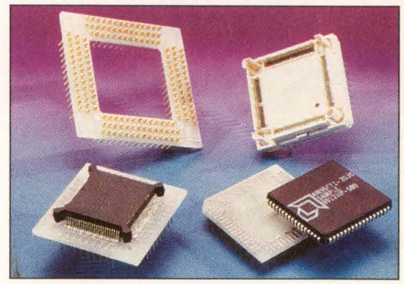

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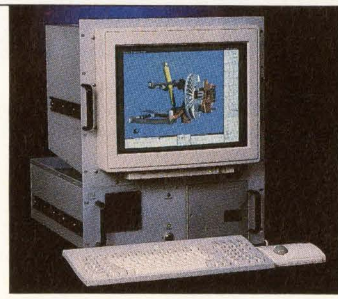

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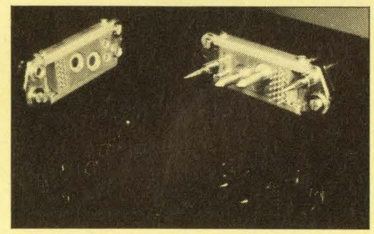

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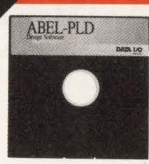

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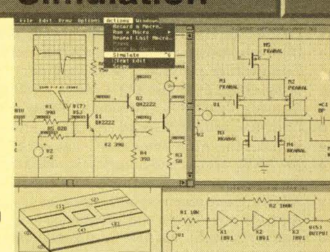

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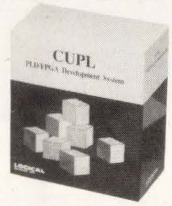

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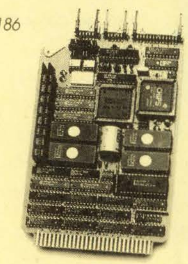

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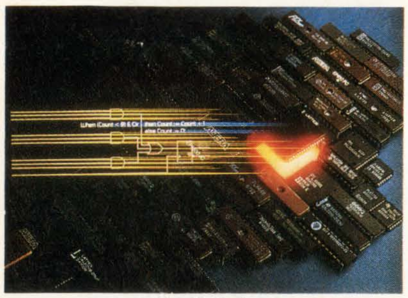

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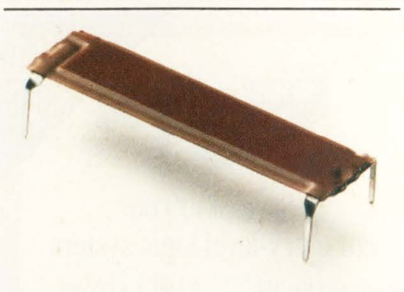

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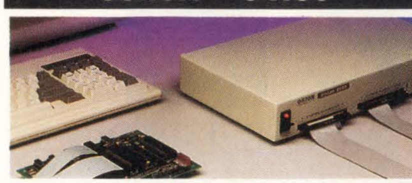

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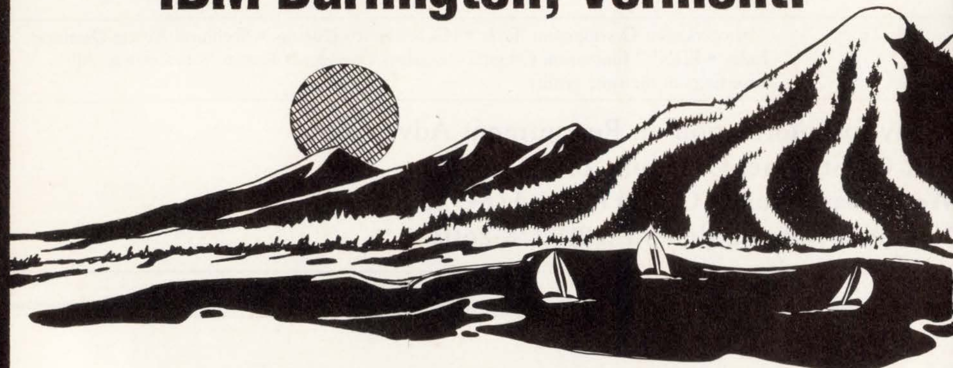

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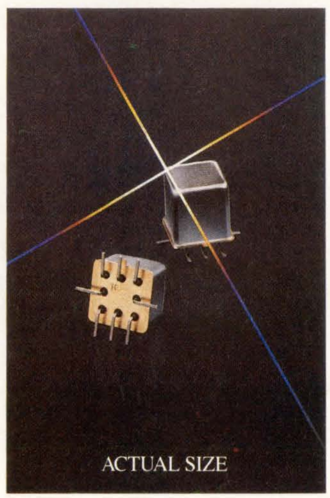

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EDN-ACRONYMS & ABBREVIATIONS

A/D—analog/digital
ALU—arithmetic logic unit
ASIC—application-specific integrated circuit
BISYNC—Binary Synchronous Communications protocol
CMRR—common-mode rejection ratio
CPU—central processing unit
D/A—digital-to-analog
DDCMP—Synchronous/Asynchronous Digital Data Communications Message Protocol
DIP—dual in-line package
DMA—direct memory access
DOS—disk operating system
DSP—digital signal processing
EEPROM—electrically erasable programmable read-only memory
EPROM—erasable programmable read-only memory
FFT—fast Fourier transform
HDLC—high-level data-link control protocol
HDTV—high-definition television
I/O—input-output
LCD—liquid-crystal display
MAC—multiply and accumulate; a MAC unit multiplies two numbers and keeps a running sum of the results
NRE—nonrecurring engineering (costs)
NTSC—the color-television broadcast standard used in the US; a 3.58-MHz composite signal that carries both brightness and color information
PAL—the color-television broadcast standard used in Europe; a composite signal differing from NTSC in a few ways, one being that the color subcarrier frequency is 4.43 MHz
PID—proportional-integral-differential
PROM—programmable read-only memory
PWM—pulse-width modulation
RAM—random-access memory
RGB—the red, green, and blue color signals used in component video systems to drive monitors
RISC—reduced-instruction-set computer
ROM—read-only memory
SDLC—synchronous data-link control protocol
SOIC—small-outline integrated circuit
TPU—time-processing unit

This list includes acronyms and abbreviations found in EDN's Special Report, Technology Updates, and feature articles.