EDN®

THE DESIGN MAGAZINE OF THE ELECTRONICS INDUSTRY

NEW PRODUCT

LeCroy's 2G-sample/sec DSO stores 8M samples pg 150

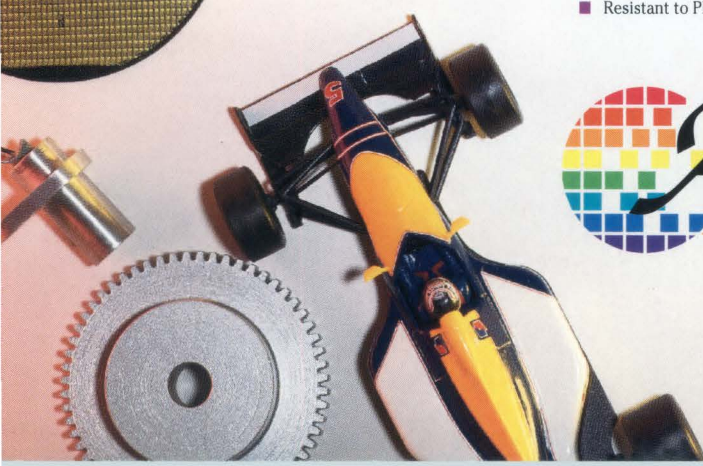
February 3, 1994

Special Report:

EMC components administer first aid

pg 54

A CAHNERS PUBLICATION



DC-2000 MHz

AMPLIFIERS

In plastic and ceramic packages, for low-cost solutions to dozens of application requirements, select Mini-Circuits' flatpack or surface-mount wideband monolithic amplifiers. For example, cascade three MAR-2 monolithic amplifiers and end up with a 25dB gain, 0.3 to 2000MHz amplifier for less than $4.50. Design values and circuit board layout available on request.

It's just as easy to create an amplifier that meets other specific needs, whether it be low noise, high gain, or medium power. Select from Mini-Circuits' wide assortment of models (see Chart), sketch a simple interconnect layout, and the design is done. Each model is characterized with S parameter data included in our 740-page RF/IF Designers' Handbook.

All Mini-Circuits' amplifiers feature tight unit-to-unit repeatability, high reliability, a one-year guarantee, tape and reel packaging, off-the-shelf availability, with prices starting at 99 cents.

Mini-Circuits' monolithic amplifiers...for innovative do-it-yourself problem solvers.

Models above shown actual size

from **99¢** Unit price $ (25 qty)

PLASTIC SURFACE-MOUNT			++VAM-3 1.45		+VAM-6 1.29	++VAM-7 1.75		
add suffix SM to model no. (ex. MAR-ISM)	MAR-1 1.04	MAR-2 1.40	MAR-3 1.50	MAR-4 1.60	MAR-6 1.34	MAR-7 1.80	MAR-8 1.75	
	MAV-1 1.15	+MAV-2 1.45	+MAV-3 1.55	MAV-4 1.65				MAV-11 2.15
CERAMIC SURFACE-MOUNT	RAM-1 4.95	RAM-2 4.95	RAM-3 4.95	RAM-4 4.95	RAM-6 4.95	RAM-7 4.95	RAM-8 4.95	
PLASTIC FLAT-PACK	MAV-1 1.10	+MAV-2 1.40	+MAV-3 1.50	+MAV-4 1.60				MAV-11 2.10
	MAR-1 0.99	MAR-2 1.35	MAR-3 1.45	MAR-4 1.55	MAR-6 1.29	MAR-7 1.75	MAR-8 1.70	
Freq.MHz,DC to	1000	2000	2000	1000	2000	2000	1000	1000
Gain, dB at 100MHz	18.5	12.5	12.5	8.3	20	13.5	32.5	12.7
Output Pwr. +dBm	1.5	4.5	10.0	12.5	2.0	5.5	12.5	17.5
NF, dB	5.5	6.5	6.0	6.5	3.0	5.0	3.3	3.6

Notes: + Frequency range DC-1500MHz ++ Gain 1/2 dB less than shown

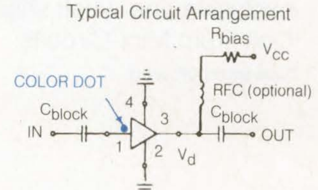
designer's amplifier kits
DAK-2: 5 of each MAR-model (35 pcs), only $59.95
DAK-2SM: 5 of each MAR-SM model (35 pcs) only $61.95
DAK-3: 3 of each MAR, MAR-SM, MAV-11, MAV-11SM (48 pcs) $74.95

designer's chip capacitor kit
KCAP-1: 50 of 17 values, 10pf to 0.1μf (850 pc), $99.95

chip coupling capacitors at .12¢ each (50 min.)

Size (mils)	Value
80 x 50	10, 22, 47, 68, 100, 220, 470, 680 pf
80 x 50	1000, 2200, 4700, 6800, 10,000 pf
120 x 60	.022, .047, .068, .1μf

Typical Circuit Arrangement



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F154 REV. A

CIRCLE NO. 40

RF TRANSFORMERS

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3KHz-1500MHz from $1^{95}

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Choose impedance ratios from 1:1 to 36:1, in connector, TO-, flatpack, surface-mount, or pin versions (plastic or metal case built to meet MIL-T-21038 and MIL-T-55631 requirements*). Coaxial connector models are offered with 50 and 75 ohm impedance; BNC standard, other types on request.

Ultra-wideband response achieves low droop and fast risetime for pulse applications. Ratings up to 1000M ohms insulation resistance and up to 1000V dielectric voltage. For wide dynamic range applications involving up to 100mA primary current, use the T-H series. Fully detailed data appear in our 740-pg RF/IF Designer's Handbook.

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*units are not QPL listed.

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CIRCLE NO. 41

F 71-Rev.E

EDN

February 3, 1994

VOLUME 39, NUMBER 3

THE DESIGN MAGAZINE OF THE ELECTRONICS INDUSTRY

On the cover: Don't let your design become an EMC casualty—designing in components such as ferrite cores and beads, connector shields, gaskets, and conductive tape will help your product meet specification. See our Special Report beginning on .... **PG 54**
(Photo courtesy 3M Electronic Products)

Continued on page 7

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EDN

February 3, 1994

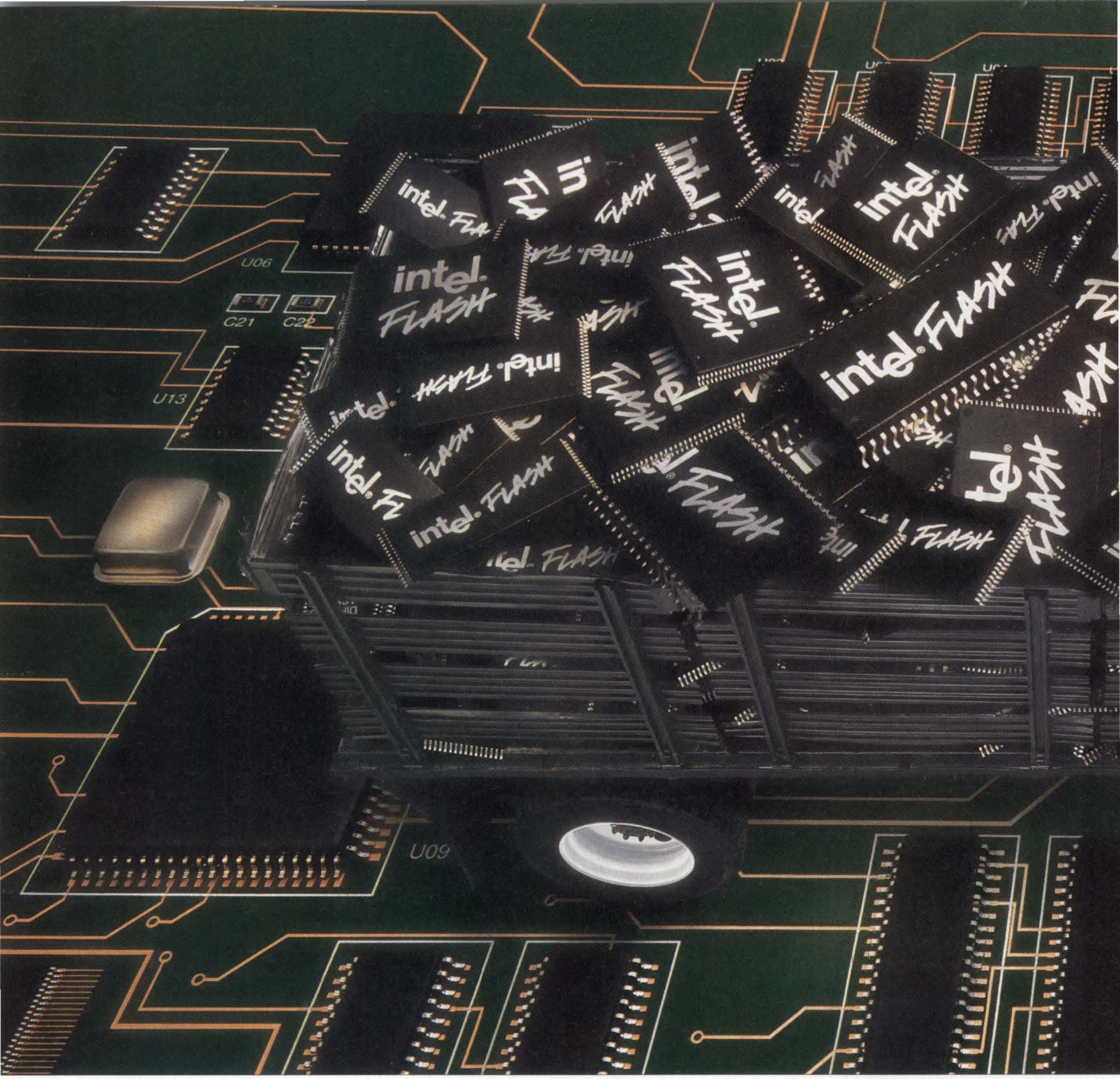
Continued from page 5

TECHNOLOGY UPDATES

EDITORIAL

NEW PRODUCTS

DEPARTMENTS

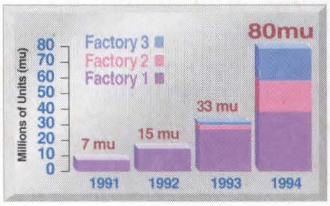


We not only have a ton of these,

Intel Flash Memory is shipping in high gear. Our factory capacity is up. Our prices are coming down. And we're leading the industry in flash technology.

The shortage is over. With three flash factories now on line, Intel can support both your immediate and long-term needs. In fact, our sub-micron process in each factory allows us to provide multiple sources for our flash products to ensure delivery.

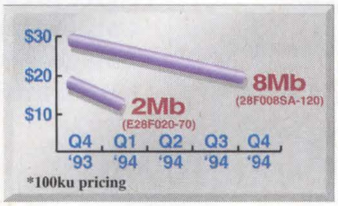
Intel Flash Memory Factory Output



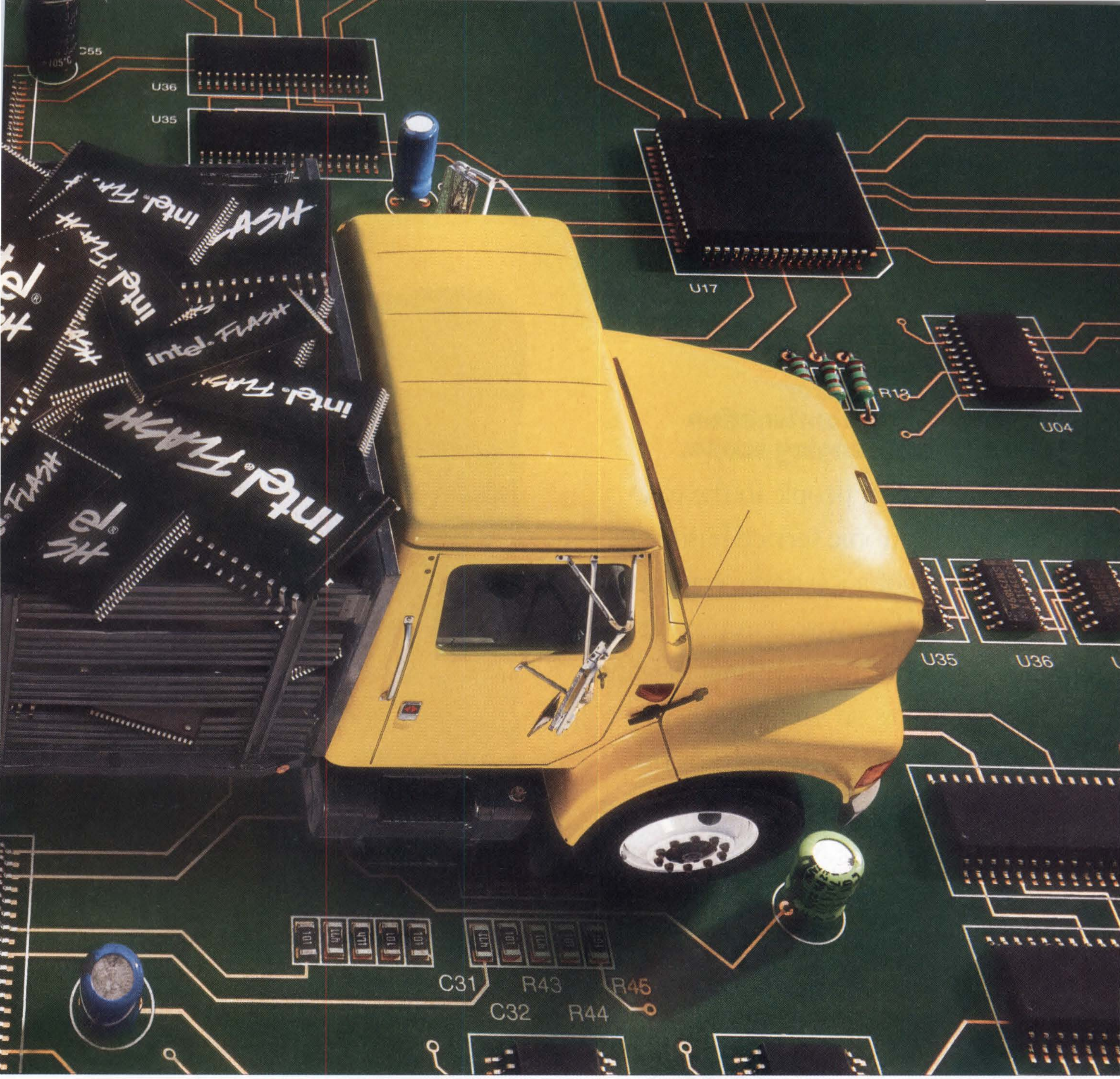
What's more, our new capacity is so huge, we'll outsupply all other flash manufacturers. Combined.†

We're also growing the market by driving down flash prices, making Intel Flash

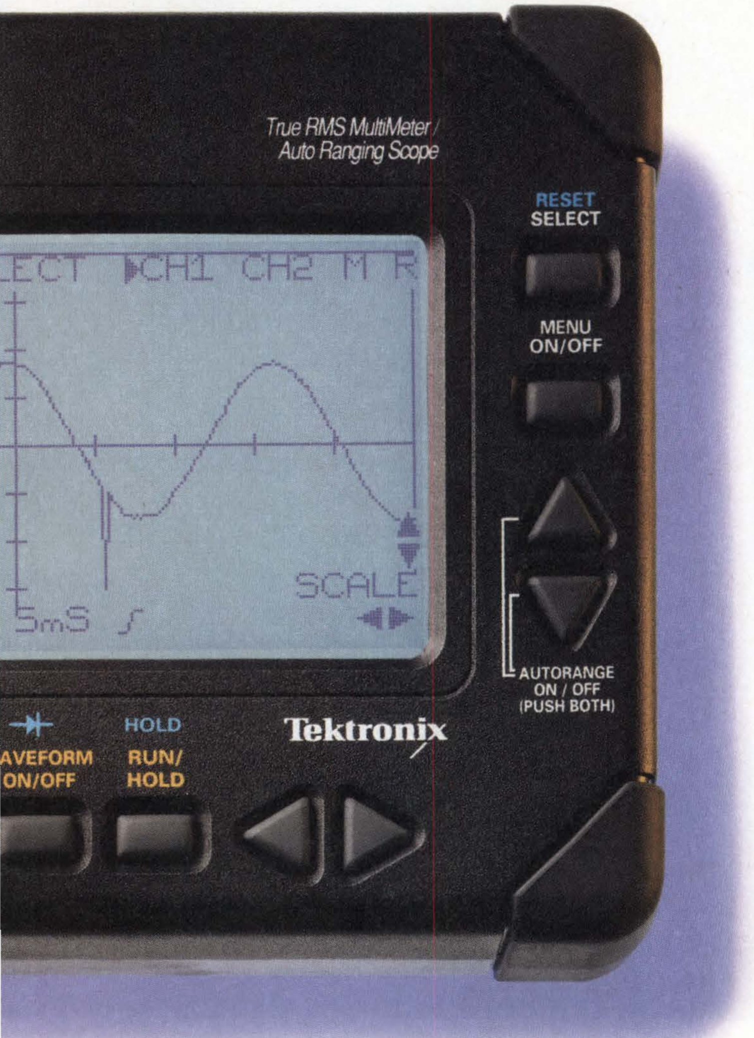
Intel Flash Component Pricing Trend*



 †Based on 9/93 Dataquest forecast of total flash units to ship in 1994.


intel. FLASH
U36
U35
U17
R13
U04
U35
U36
C31
R43
R45
C32
R44

l of the trades.



push of a button, you'll see exactly what you're measuring.

Easy to afford, too.

At only 2.2 pounds, TekMeter won't weigh heavily on your belt, and it won't do much damage to your wallet, either. Starting at $859,* the TekMeter packages a remarkable set of capabilities that will enhance your productivity and will be easy to justify.

Put one in your hands today.

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Once you've seen everything TekMeter can do—and how easily it does it—we think you'll agree it's the one tool you won't want to trade for anything else.

Tektronix

*Suggested retail price 3MW-284272 Tekmeter, Tektools, and Tektronix are trademarks of Tektronix, Inc.

CIRCLE NO. 44

EDITED BY FRAN GRANVILLE

Synopsys and Xilinx announce 5-year partnership

Synopsys and Xilinx have announced a 5-year partnership in an effort to reduce overall time to market of the companies' designs. The two companies want to collaborate to reduce the time to create a hardware-description-language (HDL) design. But HDL design is only part of the problem. Designers must also synthesize the design into cells and place and route the design. Furthermore, to be competitive, a design must be speed and area efficient compared with other design methodologies. The partnership will focus on improving every step in the process from design to production, including the creation of an FPGA family for HDL-design tools.—by Doug Conner

Synopsys Inc, Mountain View, CA, (415) 962-5000. **Circle No. 500**

Xilinx Inc, San Jose, CA, (408) 559-7778. **Circle No. 501**

Chinon and Microsoft offer Visual C++ bundle

Microsoft and Chinon are offering a hardware/software package that includes Visual C++ Professional Edition version 1.5 and a choice of an internal or an external Chinon CD-ROM drive. The $749 package is available until February 28 to registered users of Visual C++. The package shaves $300 off the separate products' retail prices.

The drives offer 220-msec access times and are MPC2 and multisession photo CD compatible; adding a $99 driver option lets the CDX-535 read Macintosh CD-ROM disks. Both drives are fully compatible with the Windows NT operating system and come with a SCSI adapter card, cables, and software.

Visual C++ Professional Edition version 1.5 offers enhancements over previous versions, such as wizards for mastering Object Linking and Embedding (OLE) 2.0 and Open Database Connectivity (ODBC). The program can now run under Windows NT, as well as Windows 3.1.

A concurrent $649 offer combines the 16-bit Visual C++, Professional Edition, version 1.5 with the recently released Visual C++ 32-bit Professional Edition. The resulting Visual C++ 16/32-bit Professional Development systems for Windows and Windows NT contains both products, as well as a choice of the Chinon drives.

—by Fran Granville

Chinon America Inc, Torrance, CA, (800) 441-0222. **Circle No. 502**

Microsoft Corp, Redmond, WA, (206) 882-8080. **Circle No. 503**

PCMCIA card connects notebooks to IEEE-488.2 bus

The ines IEEE-488.2 PCMCIA (Type II) interface adapter allows PCs with PCMCIA slots to communicate with GPIB systems. The device includes software drivers for DOS and Microsoft Windows applications. These drivers support HPIB IEEE-488.2-bus implementations that use standard commands for programmable instrumentation (SCPI) or Hewlett-Packard's standard instrumentation-command language (SICL).

A 25-way ribbon cable connects the card to an in-line standard HPIB connector. The card uses the company's i72010 GPIB controller chip—the latest in a line of GPIB chips. The i72010 is a 3.3V, 100-pin quad flatpack device that will be generally available beginning in the second quarter of this year.

The 68-pin plastic leaded chip carrier i72010 costs DM 100, and the 40-pin DIP i7210 costs DM 50. The company plans to offer an i9914 version, which is pin compatible with Texas Instruments' 9914 chip, in the second quarter.

Although backward compatible with the older NEC7210 and TI9914 GPIB chips, the ines chips also expand 488.2 bus implementation beyond some features of National Instruments' later TNT4882 controller chip. For example, the 2×255-byte FIFO buffer in the ines chip allows an interface to transfer character-hungry SCPI data strings independently of a PC processor and at a maximum bus rate of 1.1 Mbytes/sec (8-bit mode) under software control. The ines's chips also allow simultaneous recognition of 3 end-of-string

SHORTS

Arrow acquires Field. Arrow Electronics has acquired the electronic-component division of Field Oy, Helsinki, Finland. Field, the largest distributor of electronic components in Finland, is a subsidiary of Instrumentarium Corp. Principal suppliers to Field include Advanced Micro Devices, Hewlett-Packard Co, Motorola, and Xilinx. Arrow Electronics, Melville, NY, (516) 391-1300. **Circle No. 511**

TSSI expands into EDA. Test System Strategies Inc (TSSI), known for its test-software tools that link data from CAE tools to automatic test equipment, has announced intentions to enter the electronic-design-automation industry. The company's goals are to facilitate top-down design methodologies based on efficient use of hardware-description languages.

Circle No. 512

Color terminal costs less than $400. Pagine has introduced a DEC VT420 terminal that costs $399. The C20A drop-in replacement for conventional monochrome VT420 terminals offers 32 independent and simultaneous colors—16 foreground and 16 background—from a palette of 262,144 colors. Pagine Corp, San Jose, CA, (408) 944-9728.

Circle No. 513

Protel redefines distribution. Protel Technology, a developer of Windows-based EDA tools, has appointed the following regional distributors for North America: Abcor, Houston; Beta Lamda, Freehold, NJ; CADForce, Toronto; Software Tools, Waukesha, WI; Syntek, Bellevue, WA; Trilogic Inc, Wilmington, MA; Trilogic Sunforce, West Melbourne, FL; and Tusar, Scottsdale, AZ. Protel Technology, Santa Clara, CA, (800) 544-4186.

Circle No. 514

(EOS) bytes, a message-available (MAV) reset, and T8 timer support for interface-clear (IFC) commands.

In addition, ines supplies evaluation boards and device-driver development kits, which include a license-free IEEE-488.2 ANSI C module for you to recompile. The IEEE-488.2 PCMCIA (Type II) interface with drivers costs DM 1875.—by Brian Kerridge

ines-Innovative Elektronik Systeme GmbH, Cologne, Germany, (221) 492299. **Circle No. 504**

ines-Innovative Elektronik Systems Inc, Englewood, CO, (303) 779-8354. **Circle No. 505**

Siemens develops hand-gesture-recognition system

Researchers at Siemens in Munich have developed a system that responds to hand movements. A wave of a finger can cause objects on a screen to move or rotate, or the gesture can initiate a command sequence.

The system recognizes gestures in two stages. First, it uses information from a video camera to compute the contour of a hand and the direction the hand is facing. Second, the system uses rules to classify the type of movement the hand is making. For example, it can differentiate among a fist, a pointed index finger, and a thumb moving to the left or right. Once the system registers a motion, it assigns a meaning to that motion. For example, a thumb gesture to the left can move the screen contents to the left. The delay between the motion and the response is less than 0.1 sec; standard image rate is 25 images/sec.

The technology will have applications in virtual environments. For example, users could "walk through" a simulated office using hand movements and move and manipulate objects simply by "touching" them. Another application involves intuitive track diagrams for a train switch yard in which users could move freely across a simulated site, set the switches, and obtain information by "tapping" the desired objects, such as freight cars.—by Fran Granville

Siemens AG, Munich, Germany, (089) 2340. **Circle No. 506**

LITERATURE

Literature describes modulation analyzers. This free 6-pg, color brochure describes the ME2627B digital modulation analyzer and provides full specifications. Anritsu Wiltron Sales Co, Morgan Hill, CA. **Circle No. 515**

Catalog describes intelligent data-acquisition peripherals. This free, 32-pg color catalog describes the vendor's high-performance ISA-bus-based data-acquisition boards and accessories. The publication details processors that run a real-time operating system and the host software. Microstar Laboratories Inc, Bellevue, WA. **Circle No. 516**

Synopsys and Logic Modeling to merge

Subject to stockholder and regulatory approvals, Synopsys and Logic Modeling Corp (LMC) expect to merge in March. LMC will remain as a different business unit with headquarters in Beaverton, OR. LMC President and Chief Executive Officer William Lattin will continue to serve as president of the Logic Modeling unit. LMC is the leading source of models for board and system-level simulation.—by Doug Conner

Logic Modeling Corp, Beaverton, OR, (503) 690-6900. **Circle No. 507**

Synopsys Inc, Mountain View, CA, (415) 962-5000. **Circle No. 508**

Skip the commercials

Arthur D Little has developed a technology called Commercial-Free, which automatically eliminates commercials from any VCR-recorded TV program. While the VCR is recording, the system monitors the broadcast for video and audio events, such as black frames and low sound energy, which occur at the beginning and end of each commercial. Simultaneously, the system writes a binary timing and recording-session identification code into a nonviewable portion of the video signal recorded onto the videotape.

At the conclusion of recording, the system uses a proprietary algorithm to identify which of the audio and video events noted mark the beginning and end of each commercial break. The system time-stamps, stores in memory, and post-processes the audio and video events. It then creates a playback "map" for the recorded program and stores it in memory.

Upon playback, the system reads the identification code for the recording session from the tape and retrieves the playback map from memory. The moment the program enters the leading break for a commercial, it displays a flat blue field on the screen, and the VCR enters "forward-search" mode. The blue screen masks the garbled high-speed picture normally associated with the VCR's forward-search mode, thus making the process transparent to the viewer. Furthermore, because today's VCRs can scan through 3 minutes of recorded material in less than 5 sec, the process is unintrusive. At the conclusion of the commercial break, the VCR re-enters play mode, and the video picture returns to the screen.

—by Fran Granville

Arthur D Little Enterprises Inc, Cambridge, MA, (617) 498-5000. **Circle No. 509**

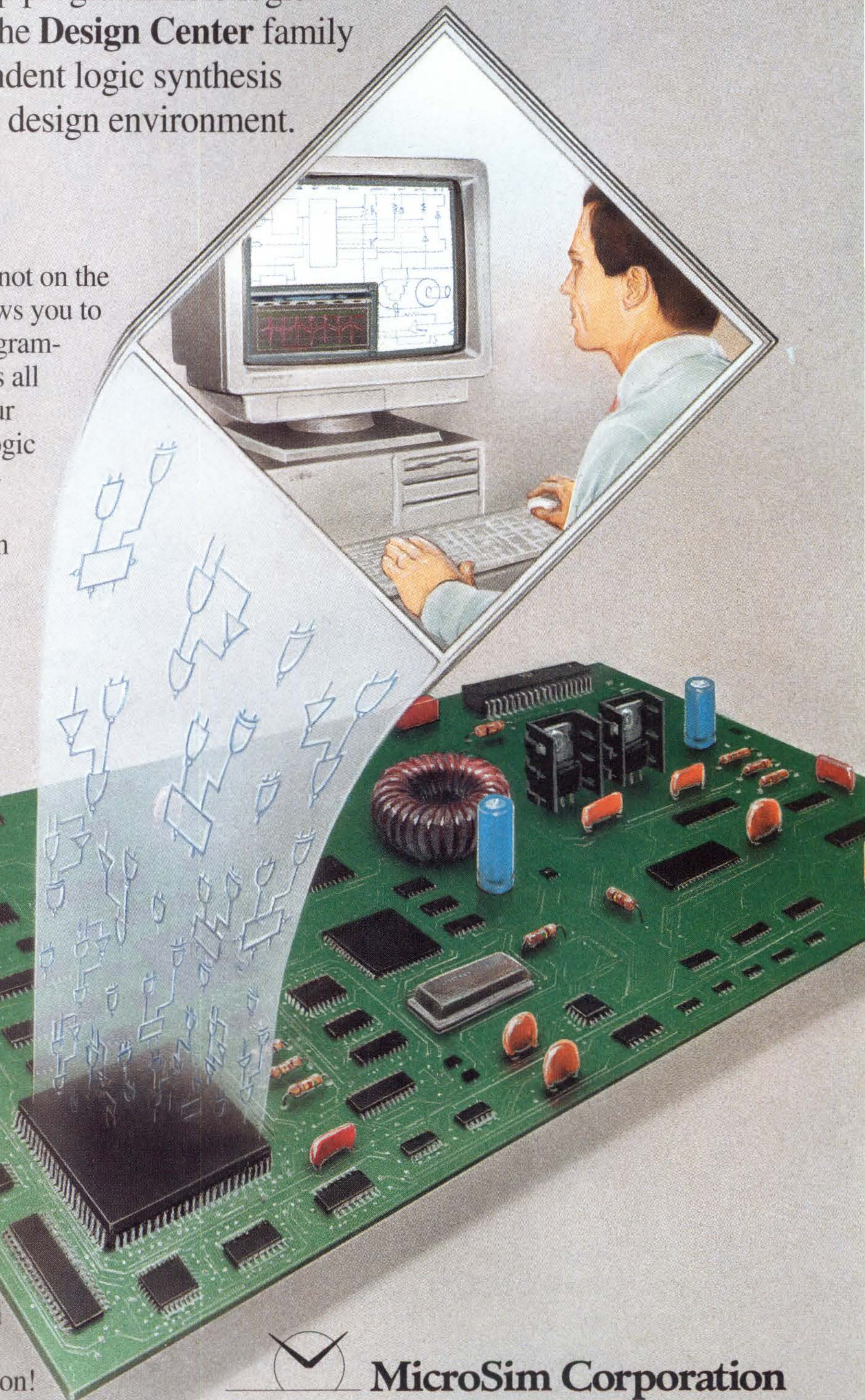
Software helps solve serviceability problems

Boothroyd-Dewhurst has released version 1 of the Design for Service (DFS) analysis program. The software allows engineering teams to consider serviceability issues while performing traditional design-for-assembly (DFA) analysis. DFS provides information on disassembly and reassembly times; a serviceability rating index; and labor, operation, part, and replacement costs. Boothroyd-Dewhurst has integrated the software with version 7 of the company's DFA software, which uses assembly information to generate DFS reports.—by Fran Granville

Boothroyd-Dewhurst Inc, Wakefield, RI, (401) 783-5840. **Circle No. 510**

Design Complex PLDs Without Leaving Your System Behind

PLSyn is the most advanced desktop programmable logic synthesis system available. Part of the **Design Center** family of products, it offers device-independent logic synthesis fully integrated with a mixed-signal design environment.



Design Your System...

PLSyn lets you concentrate on your system, not on the PLDs. It is the only desktop system that allows you to design and simulate a system containing programmable logic, discrete digital, and analog parts all on the same schematic. You can describe your logic using a powerful synthesis language, logic symbols, or a combination of both. Programmable logic is automatically compiled and simulated with the rest of your system—even if it includes analog! You no longer need to piece together separate programmable logic, discrete logic, and analog simulations to be sure your system will work.

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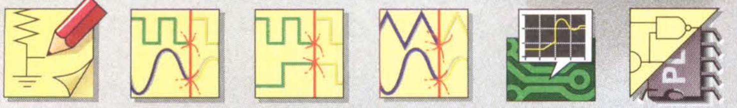
When logic design is complete, PLSyn helps you find the best parts to use. You define your own goals for price, speed, and power consumption. PLSyn does the rest. It searches a library of over 4,000 devices, including the new large complex PLDs from AMD and others. PLSyn can even automatically partition your design into several different types of parts to meet your design goals. Whether you are new to programmable logic, or an experienced PLD user, the **Design Center**'s PLSyn is your most productive programmable logic design system. Call today for more information!



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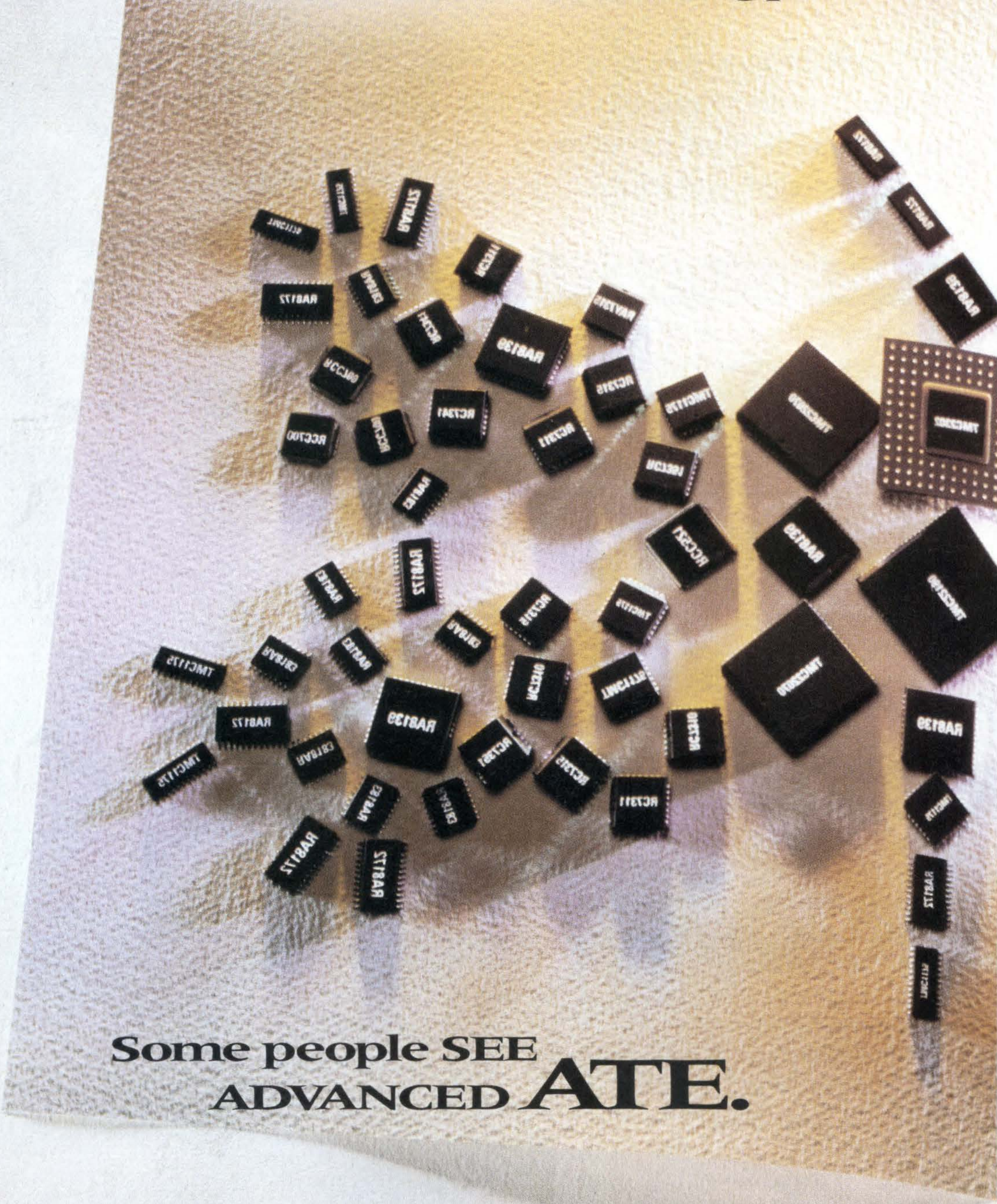
• CIRCLE NO. 150 FOR IBM • CIRCLE NO. 152 FOR SPARCSTATION

Some people SEE HOT VIDEO technology.



Some people SEE ADVANCED ATE.

To see your visions take shape, choose a partner who's committed to delivering higher performance at a lower cost.

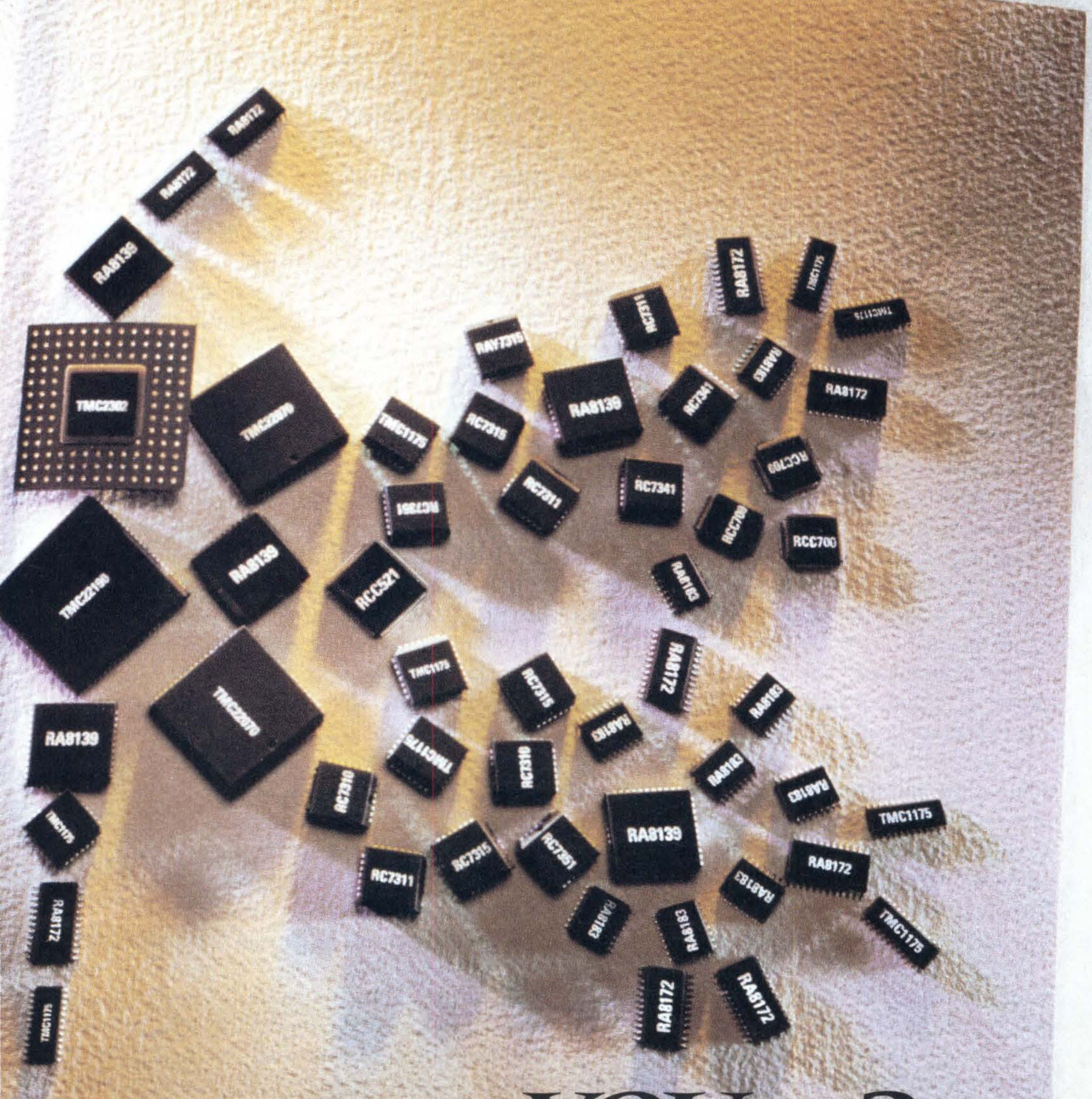
When you think of innovative and affordable ICs, what comes to mind?

If it's not Raytheon Semiconductor, then maybe you should take a closer look at one of today's most valuable and experienced partners.

You see, Raytheon Semiconductor offers you advanced solutions to help you get the absolute most from video, high-speed communications and ATE designs. This includes bringing you — at the right price — a full family of ICs that push the limits of performance. And whether you need standard products or semi-custom ICs, we'll work with you at every step.

Some people SEE HIGH-SPEED

COMMUNICATIONS.



What do *YOU* SEE?

All of which means you can aspire to more. Like more breakthroughs in high-quality conversion and manipulation of video signals. More blazing speed for your serial link LAN or WAN. More compact designs and higher frequency testing in ATE. Or more of whatever you've set your sights on.

So call us now for your 1994 Databook. Because when you're working with Raytheon Semiconductor, great things always come to mind.

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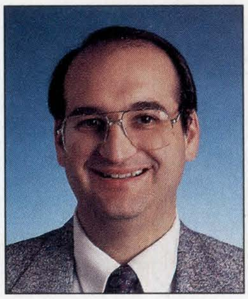
Raytheon
Semiconductor Division

CIRCLE NO. 46

Raise your expectations



It was unprecedented: Apple, IBM, and Motorola teamed up to create the PowerPC 601 μP. The companies created a facility called Somerset in the Arboretum section of northern Austin to house the processor-development team. Planners located and "facilitized" a building in an unusually short time. Local-area networks and computing equipment sprouted overnight. Team members worked around the clock, during weekends, and over holidays. More important, the μP rolled out of the wafer-fab facility 100% functional, on schedule, and running at frequency.

Somerset achieved these goals because a lot of people worked very hard. But people work hard on many projects and don't experience the success achieved by the Somerset team. One reason for this success—perhaps the most important reason—was the team's expectations.

The Somerset team leaders expected these excellent results. The leaders made sure that their team members were highly motivated (they were out to best a major competitor and to prove that the unlikely collaborative trio could work), and they made sure that everyone understood that they expected the 601 μP to appear on time and fully functional. They set the team's expectations precisely on the desired outcome.

Meanwhile, a group of British entrepreneurs in Nottingham have established a beachhead in Nashua, NH, where they plan to take the desktop-publishing market by storm with a $59.95 Windows-based product called PagePlus 2.0. The company, named Serif ((603) 889-1127), has a presence in Europe. Its nearest competitor pricewise in the United States is Microsoft Publisher, but Serif claims that its software offers the features of high-end desktop-publishing packages costing 10 times more. I met some Serif employees at Fall Comdex '94. They were demonstrating PagePlus, and they virtually seethed with high expectations during their enthusiastic and impressive demo. Call it wish fulfillment; call it self-fulfilling prophecy; call it whatever you like, but recognize the power of your expectations.

No one claims that high expectations are all you need to succeed. Certainly, the Somerset team must have hit a roadblock or two, and it took more than high hopes to hurdle the obstacles. Serif certainly has some major hurdles looming in the immediate future. But setting your expectations high must certainly be the first step on the road to success. If you don't expect success, if you're not constantly looking for that favorable outcome, then the probability of achieving your goals drops substantially. Without those high expectations, team members (including you) may feel that something less than success is acceptable. So step back for a minute, and ask yourself just what you expect of your current projects. I suggest you set your expectations high.

Perhaps the initial PowerPC project experience was a fluke, and the Somerset clan will never again hit the bull's eye. Maybe Serif won't scramble to the top of its market. However, I certainly wouldn't bet against these companies. Somerset has a lot more PowerPC processors heading our way, and Serif is rolling PagePlus 3.0 out the door.

Steven H. Leibson

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Editor-in-Chief

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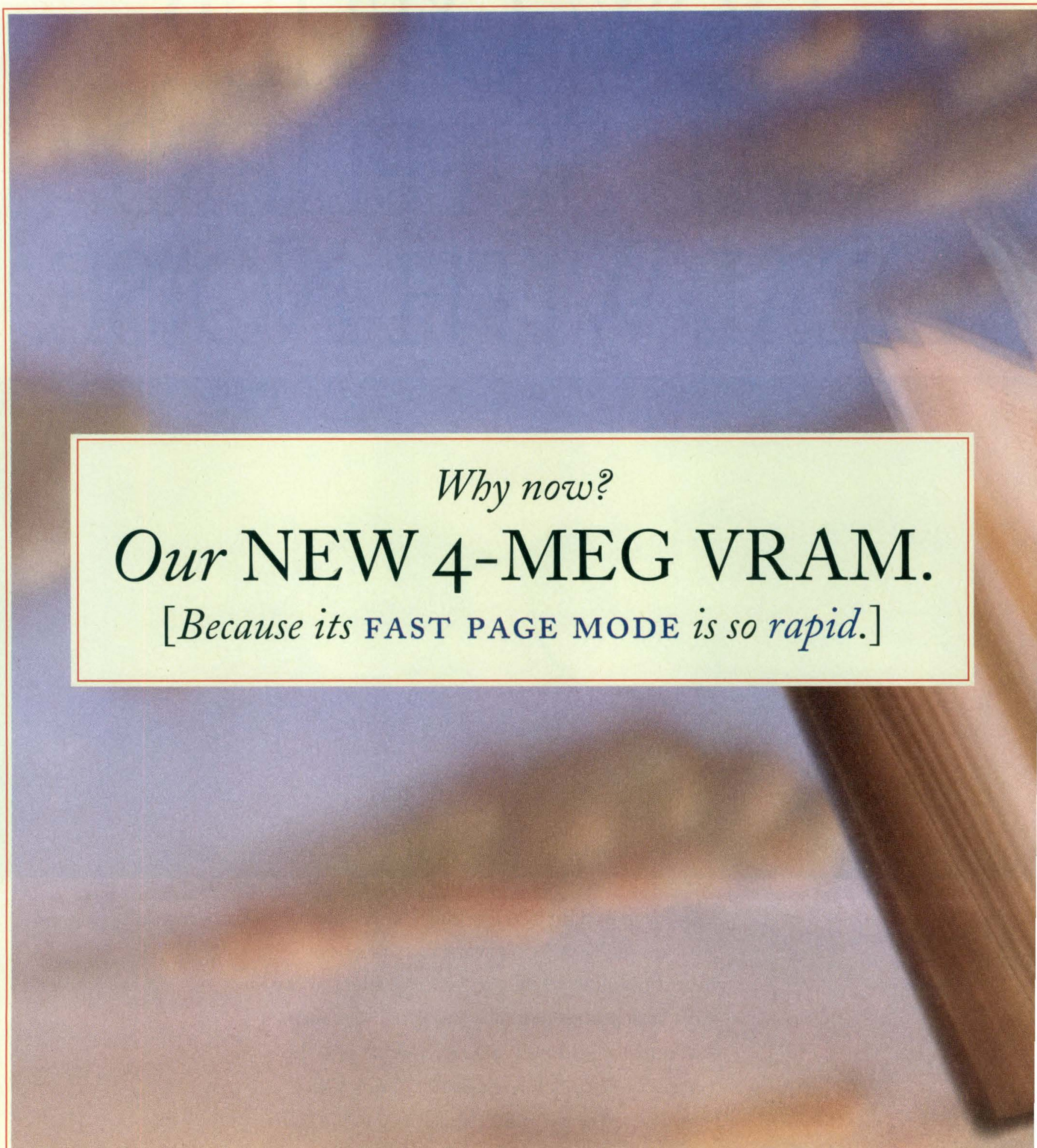

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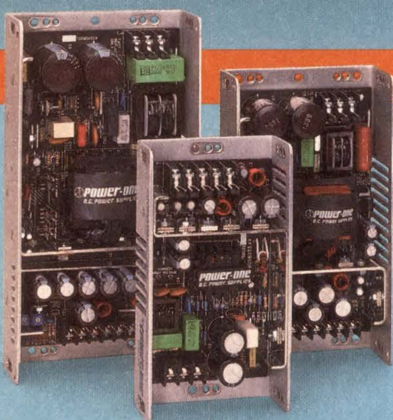

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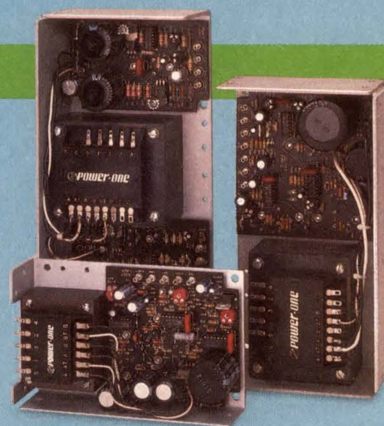

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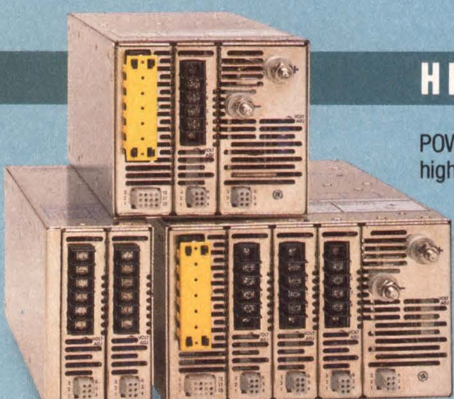

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CIRCLE NO. 48

PCI local bus gathers momentum

GARY LEGG, Senior Technical Editor

Both the PCI local bus and the VL bus let high-speed peripherals bypass a PC's slow expansion bus. But PCI is gaining favor among designers, and a crop of new PCI components is starting to simplify local-bus design.

When a flood of data from fast peripherals meets a slow PC-expansion bus, something has to give. And so, with applications in graphics, video, and imaging proliferating rapidly, computer designers are now connecting peripherals directly to a system processor's local bus. But connecting directly to a local bus can result in unpredictable performance, as many designers have learned the hard way. Fortunately, though, help is on the way from the Peripheral Component Interconnect (PCI) bus.

With data throughput as high as 132 Mbytes/sec (even higher in future implementations), the PCI bus smashes the I/O bottleneck of traditional expansion buses. So does the VESA local (VL) bus, for that matter; in fact, the VL bus did it first. But the VL bus is losing ground in the race for market acceptance, mainly because the PCI bus offers a more attractive technology-migration path to the future. In addition, a whole lineup of new products is now making it easier to implement the PCI bus and PCI-compliant peripherals.

Long-range plan prevails

The contest between the PCI and VL buses is much like the race between the tortoise and the hare. VL, developed by the Video Electronics Standards Association, jumped to an early start with a quick-time-to-market solution. It did so, however, with a specification that was somewhat shortsighted and, in the opinion of many designers, rather "casual." PCI, developed by Intel but now an open standard, started more slowly but took a longer range view. PCI components and systems have only recently started appearing on the market, but most designers praise the PCI spec's thoroughness and orientation toward the future.

PCI's forward-looking plan includes processor independence, compatible 32- and

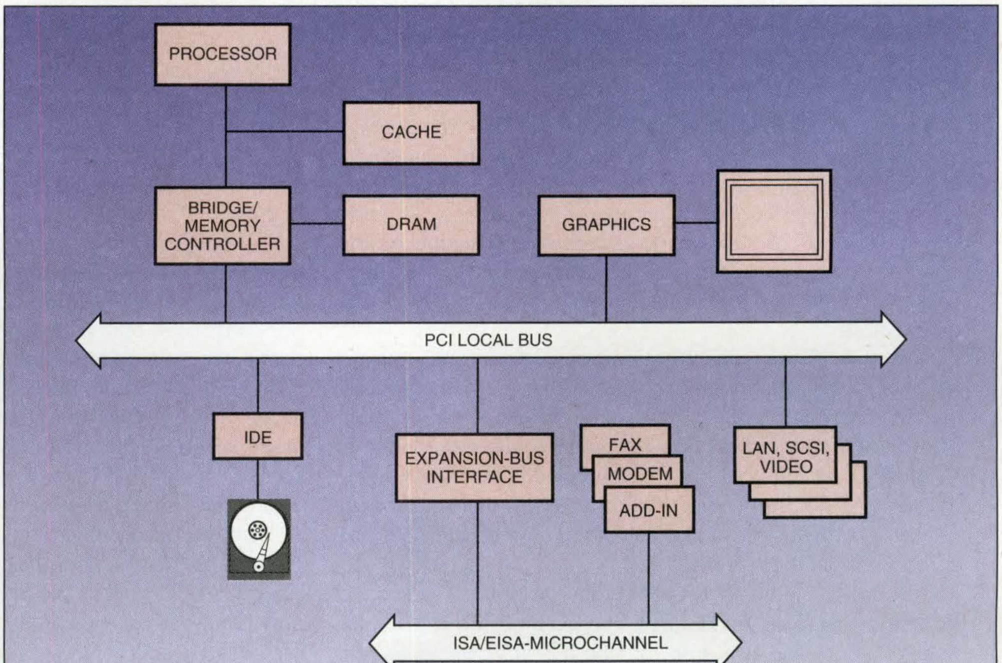

Fig 1—The PCI local bus provides a high-bandwidth data path for PCI peripherals that can be on a mother board, on add-in cards, or external. With bridge chips, you can connect other standard peripherals, including expansion boards for ISA/EISA or MicroChannel systems.

64-bit buses, and a smooth transition from 5 to 3.3V devices (see **box**, "PCI-bus highlights"). In fact, the PCI bus specification (**Ref 1**) already contains details for those features. VESA recently added similar features to its VL-bus spec (**Ref 2**), but not before the PCI bus had already gained a good deal of market momentum. In addition, because the VESA additions increased the VL bus's complexity, they diminished its main selling point—low implementation cost.

Processor independence has contributed a great deal to the PCI bus's success. You can implement the bus on Intel processors, but that doesn't exclude using other processors. For example, Digital Equipment Corp (DEC) is linking PCI to its Alpha processors; Apple, IBM, and Motorola are using it with the Power PC. Any PCI-compliant peripheral works with any of the systems, sparing manufacturers the task of designing models with different interfaces.

The PCI bus is also compatible with standard expansion buses. You can have both bus types connected to the system processor, or, as **Fig 1** shows, you can put a slow expansion bus—ISA, EISA, or MicroChannel (MC)—on top of a PCI bus. With PCI-to-PCI bridge chips coming soon from DEC and IBM, you can even put one PCI bus on top of another.

With a secondary PCI bus, you can put multiple peripheral functions on a single add-in card. These functions, if implemented as bus masters, can communicate with each other over the bus without involving the system processor. Access to the system processor is still possible, however, via the two cascaded PCI buses.

PCI peripherals can exist as chips (for use on a mother board or a single-board computer), as add-in cards, or as external devices with a card interface. A typical PCI desktop computer has three PCI-card slots plus two peripheral functions—for example, a graphics accelerator and a LAN—on the mother board. According to rule-of-thumb guidelines for PCI design, you can put 10 electrical loads on the bus. Each mother-board function or bridge chip counts as one load; each card connector counts as two.

PCI add-in cards are mechanically compatible with ISA-, EISA-, or MC-based systems, provided that those systems also have some PCI connectors on the mother board. The PCI-card connector is the MC style, and two types of attachable brackets adapt a standard

PCI-bus highlights

- Synchronous, processor-independent 32- or 64-bit local bus
- Operation at 5, 3.3V, and combination
- Forward and backward compatibility of 32- and 64-bit PCI components and add-in boards
- Bus speeds as high as 33 MHz
- Transfer rates as high as 132 Mbytes/sec (264 Mbytes/sec for 64-bit bus) via burst mode
- Full multimaster capability
- Hidden (overlapped) central arbitration
- Concurrency with processor/memory subsystem
- Write-back and write-through cache support
- Automatic configuration of PCI add-in cards at power-up

PCI bus vs VL bus

The latest specification for the VESA local (VL) bus (**Ref 2**) mirrors some of the features of the Peripheral Component Interconnect (PCI) bus. It provides for expansion to 64 bits, for example, and it achieves processor independence by providing "bridge" connections to a processor's local bus. The original VL bus was essentially the same as a 486 local bus, and you could implement it only with 486- and 386-type architectures.

The new VL-bus spec also increases clock rates—to 66 MHz on a mother board and to 50 MHz across card connectors. Previously, the clock rate was 33 MHz on both boards and connectors. Some designers with experience in VL and PCI design are concerned that the higher clock rates, especially across connectors, will cause unreliable operation. Others, however, say that new shielded connectors should be able to handle the faster clock.

The newly specified 64-bit VL bus multiplexes data and addresses, as does the PCI bus. The 32-bit PCI bus also multiplexes addresses and data, but the 32-bit VL bus does not. So, although 64-bit PCI and VL buses require roughly the same number of connections, a 32-bit PCI bus requires considerably fewer than does a 32-bit VL bus. Both the PCI and VL buses provide 32-/64-bit transparency. A 64-bit add-in card works on a 32-bit bus, and a 32-bit card works on a 64-bit bus.

PCI cards are more adaptable to different types of systems, however. A PCI card works in any ISA-, EISA-, or MicroChannel (MC)-based system that also has PCI slots; VL-bus cards have both a VL connector and an ISA, EISA, or MC connector, so they're limited to only one type of system.

In terms of performance, the PCI bus enjoys some advantages over VL. Burst reads and writes, for example, can be essentially any length on PCI. With VL, they're limited to 16 bytes or fewer, thus incurring more overhead for setting up addresses on long transfers.

PCI-bus concurrency allows the system processor to operate independently, and thus not get delayed, when a bus-master peripheral gets bus possession. The VL bus, which until now has been essentially the 486 processor's local bus, has not allowed concurrency. Concurrency will be possible with VL-bus bridge chips, however, and will be available if designers choose to implement it.

PCI LOCAL BUS

PCI card for mechanical installation in an ISA/EISA or a MC system. The PCI specification also provides for a smaller 7-in. card, compared with the standard 12.325-in. card.

One of the card slots in a PCI-compliant system can be a "shared" slot that accommodates a PCI card or a standard expansion card. The mother-board PCI connector for a shared slot is very close to the ISA, EISA, or MC connector. The component side of a PCI card is opposite that of the other cards to enable either type of card to fit into roughly the same physical space. You choose which type of card to use; both, obviously, cannot occupy the shared slot at once.

A number of products (**Table 1**), many of which are just now becoming available, can help you design PCI into your system. Some processors—DEC's Alpha 21066, for example—put the PCI bus on chip. In most cases, however, separate PCI chip sets—sometimes called bridges—essentially create a PCI bus and connect it to a processor's local bus. (Technically speaking, the PCI bus isn't a local bus. It's more like a mezzanine bus that is closely tied to the local bus.)

Other new PCI products add peripherals to your system. Some of these are bridge chips that connect existing standard interfaces—SCSI or IDE, for example—to the PCI bus. Other products are PCI-compliant peripherals implemented as chips or add-in cards. Graphics accelerators and Ethernet controllers are the most prevalent of these.

If you're designing your own PCI-compliant peripheral device, your product options are somewhat limited for now. General-purpose PCI-interface chips aren't yet commercially available, although at least two are in development. PLDs and FPGAs have trouble driving the PCI bus, although Intel says it will introduce some PCI-compatible devices this year.

You can, of course, connect to the PCI bus with an ASIC of your own design. Most ASIC vendors now have PCI drivers in their cell libraries. If you can wait a couple of months, though, the availability of PCI-interface chips could help you avoid the up-front costs of an ASIC.

With PCI-controller chips now in development, you can create a complete interface between a μP and the PCI bus. One controller chip, from American Micro Circuits Corp, interfaces to practically any μP. The chip provides a 32-bit address/data path, all required address decoding, and all the necessary registers and other features for a PCI connection. PLX Technology is developing a similar chip for the i960 μP. Both chips should be available in the second quarter of this year.

For general guidance in PCI design, start with the PCI Special Interest Group (PCI SIG). PCI SIG oversees the PCI specification and provides additional design guidelines that aren't formally specified. The group now has more than 200 member companies; many are developing PCI components and add-in boards. Contact PCI SIG (see **box**, "For free information...") for a list.

The next few months will see a flood of PCI products. Some will be new; others will be products that are just

Table 1—Peripheral Component Interconnect-bus ICs

	IC functions available				
Manufacturer	**PCI on μP**	**μP on PCI**	**IDE on PCI**	**SCSI on PCI**	**ISA on PCI**
Adaptec Circle No. 301			x	x	
Advanced Micro Devices Circle No. 302				x	
American Micro Circuits Circle No. 303		x			
Appian Technology Circle No. 304			x		
BusLogic Circle No. 305			x	x	
Contaq Circle No. 306					x
Digital Equipment Corp Circle No. 307	x				
Future Domain Circle No. 308				x	
IBM Microelectronics Circle No. 309	x				
Intel Circle No. 310	x				
NCR Corp Circle No. 311				x	
Opti Circle No. 312	x				
PLX Technology Circle No. 313		x			
QLogic Circle No. 314				x	
Symphony Circle No. 315	x		x		
VLSI Technology Circle No. 316	x				

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- Output protections: shade, sunscreen
- No system of error sensing/detection
- Mil-Std qualifications: none
- Board-mountable: *not*
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now stable enough to warrant volume production. Because PCI is new and its technical specification is fairly demanding, some early components had difficulty meeting all the spec's requirements.

The PCI bus still faces market competition from the VL bus (see **box**, "PCI bus vs VL bus"), but the long-range outlook seems to favor PCI. The VL bus's main advantage is that it is essentially the same as the 486 local bus

For free information...

For free information on the PCI products discussed in this article, circle the appropriate numbers on the postage-paid Information Retrieval Service card or use *EDN*'s Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in *EDN*.

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Sunnyvale, CA
(408) 732-2400
Circle No. 302

American Micro Circuits Corp
San Diego, CA
(619) 450-9333
Circle No. 303

Appian Technology Inc
Sunnyvale, CA
(408) 730-5406
Circle No. 304

BusLogic Inc
Santa Clara, CA
(408) 492-9090
Circle No. 305

Contaq Microsystems Inc
San Jose, CA
(408) 428-9025
Circle No. 306

Digital Equipment Corp
Maynard, MA
(508) 493-5111
Circle No. 307

Future Domain Corp
Irvine, CA
(714) 253-0913
Circle No. 308

IBM Microelectronics
Somers, NY
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Circle No. 309

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(408) 765-8080
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NCR Corp
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VLSI Technology Inc
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(602) 752-8574
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and thus is inexpensive to implement in a 486-based system. As the use of other processors increases, however, the balance will tip to PCI.

Once start-up difficulties subside, the PCI bus could substantially change the "flavor" of PCs, both on the desktop and in embedded systems. By putting peripheral-I/O speeds on a par with processor speeds—and by doing so with standard, high-volume, off-the-shelf components—PCI could make possible a range of products and applications that previously were technically or economically infeasible. The PCI bus could, in fact, become one of the enabling technologies of the decade. EDN

Looking ahead

The Peripheral Component Interconnect (PCI) bus's bandwidth is adequate even for bus-hogging applications like full-motion video, but bandwidth requirements will undoubtedly increase. Fiber-interface communication can easily consume 100 Mbytes/sec, and high-definition television (HDTV) and multimedia will also be very demanding.

Extending the PCI bus to 64 bits will satisfy many of those demands, stretching bandwidth from 132 to 264 Mbytes/sec. A 64-bit specification is in place, and 64-bit PCI products should start appearing this year.

To further increase data throughput, the PCI clock rate could eventually double, to 66 MHz, or even quadruple. The higher rate could initially prove troublesome across card connectors, but single-board systems—without the connectors' added capacitance—will be less of a challenge.

A second PCI bus—implemented on top of another PCI bus via a bridge chip—offers some interesting possibilities for new system architectures. A secondary bus on an add-in card, for example, will let you include multiple PCI-peripheral functions on the card. The PCI SIG is also investigating a card-top connector that links cards via a secondary bus.

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5. Mosley, JD, "Bypass the PC Bus to Speed up Your System," *EDN*, February 18, 1993, pg 65.

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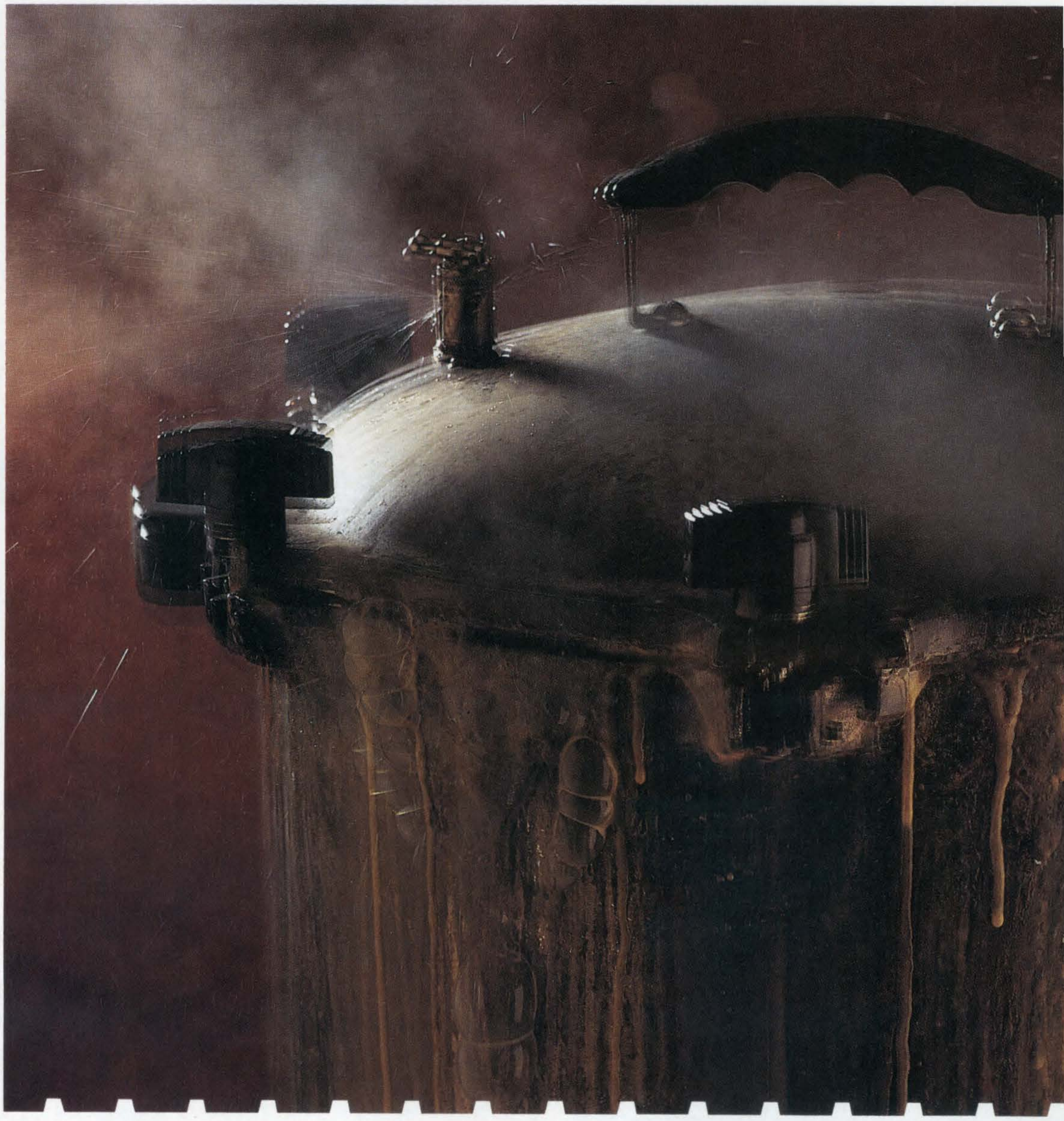

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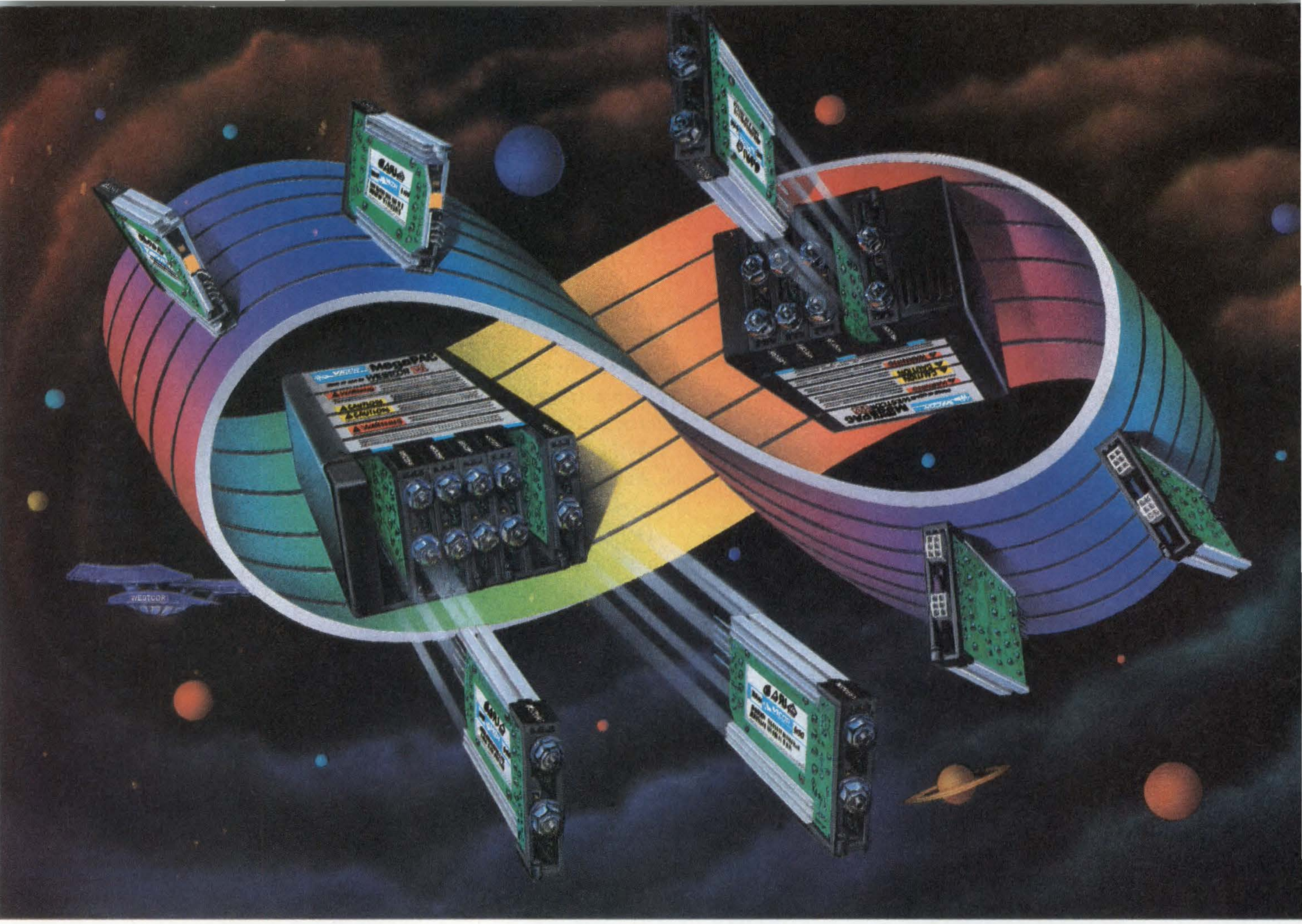

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Digital HDTV system links computers with telecommunications

ANNE WATSON SWAGER, Technical Editor

After almost seven years of proposals, testing, and FCC advisory-committee meetings, a US standard for HDTV could be in its final testing phase by the end of this year. Some early technical decisions define the minimum system requirements.

From specialized image-compression ICs to op amps, manufacturers have touted high-definition television (HDTV) as a potential application for products introduced within the last few years. This promotion occurred despite the fact that manufacturers had no firm notion of the actual form that US HDTV would take. However, that form is finally beginning to take a very definite shape.

Since 1987, when the FCC began organized efforts to draft a broadcast standard, US HDTV has gone from a system with digital compression and analog transmission to a hybrid digital/analog transmission system to the current all-digital system.

The proposed US system places a heavy emphasis on computer-compatible progressive-scanning techniques—as opposed to traditional NTSC TV's interlaced mode—and MPEG-2 compression and decompression techniques. According to Glenn Reitmeier, the director of the High Definition Imaging and Computing Laboratory at the David Sarnoff Research Center in Princeton, NJ, this emphasis points to a future in which MPEG may become the de facto standard for the multimedia industry. "We're on our way to a very interoperable format between computers and HDTV," says Reitmeier. "Future consumer products may have a much more multimedia feel than does traditional TV," he adds.

The proposed system, which its proponents describe in terms of layers (**Fig 1**), is a very flexible system that encompasses mul-

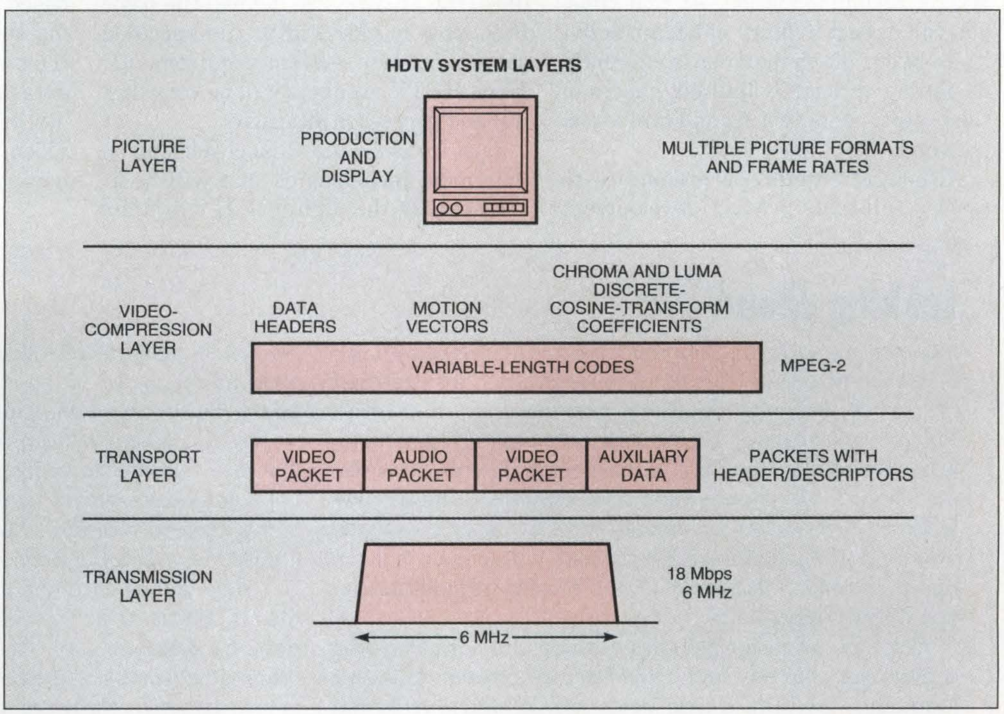

Fig 1—The HDTV system proposed by the Grand Alliance is a very flexible digital system with a layered architecture.

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tiple picture formats and frame rates and a flexible transport channel that shares video and audio signals.

The current activity on the US digital HDTV standard—for which some key technology decisions were announced last fall and others are due early this year—is an effort of both compromise and expediency. After the 7-year process of proposals, testing, and FCC recommendations, the surviving companies—and former opponents—banded together last year to form the Grand Alliance. Working together, the members hope to bring HDTV signals and sets into US homes as early as 1996.

This Grand Alliance includes AT&T, General Instrument Corp, the Massachusetts Institute of Technology, Philips Consumer Electronics, Thomson Consumer Electronics, the David Sarnoff Research Center, and Zenith Electronics Corp (see **box**, "For more information...").

According to its members, the alliance could save a year or more in HDTV implementation by reducing the risk of inconclusive test results and the possibility of legal challenges. All members hope that by the end of this year or early next year, the FCC advisory committee will make its final and complete HDTV recommendation. At that time, you can expect a flurry of design activity to begin. Each member is currently designing or actively building pieces of the prototype for testing and evaluation (see **box**, "Looking ahead").

Although it would be premature to start a full-scale product development before the FCC approves the final standard, the alliance has defined the basic functional blocks (**Fig 2**) and specified some minimum system requirements. Final HDTV products will be very digital and processor intensive.

Last October, the alliance decided on four main technologies that will be at the heart of the digital HDTV system: digital video-compression technology based on MPEG-2 parameters, including the use of B-frames (bidirectional frames for motion compensation); a data-transport system based on packets of virtually any combination of video, audio, and data; interlaced- and noninterlaced- (progressive) scanning

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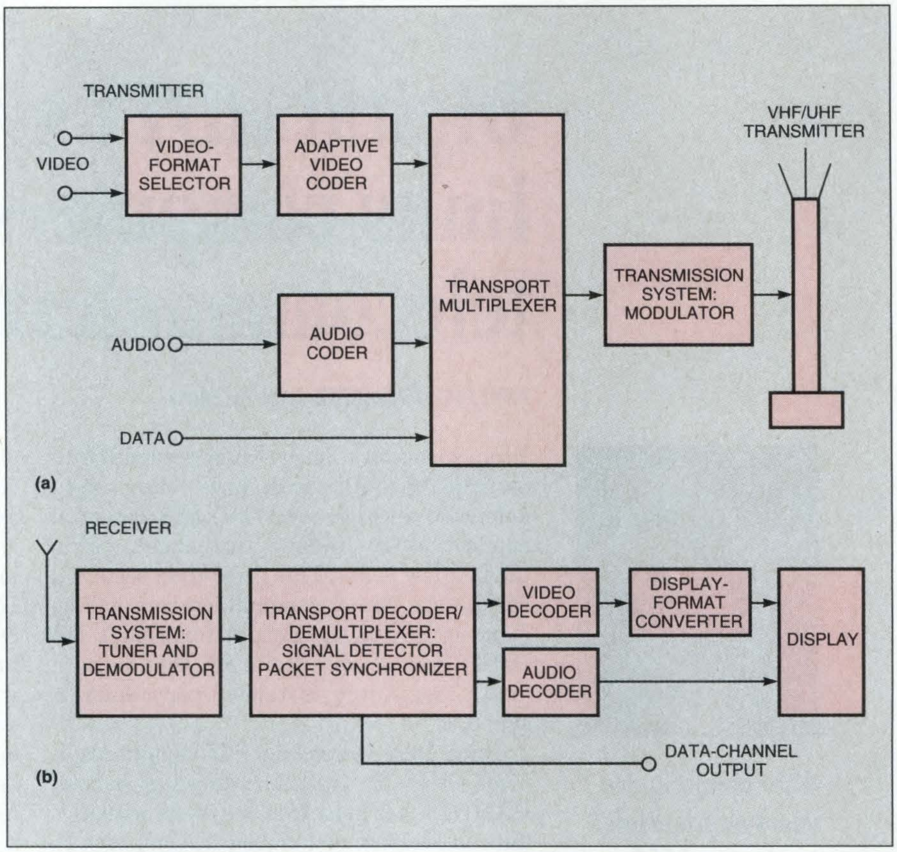

Fig 2—The Grand Alliance has defined the functional building blocks of the proposed US HDTV system's transmitter (a) and receiver (b).

Looking ahead

Now that the Technical Subgroup of the FCC's Advisory Committee on Advanced Television Service (ACATS) has endorsed the initial technical decisions presented by the Grand Alliance, members of this alliance are constructing a prototype. Before they can build a complete prototype, however, the alliance must choose a transmission system. The alliance tentatively scheduled for January trials of Zenith's vestigial-sideband (VSB) digital-modulation and -transmission technology and General Instrument's quadrature-amplitude-modulation (QAM) approaches.

Once the alliance makes this decision and has completed a prototype, the advisory committee will conduct extensive laboratory tests in the United States and Canada to verify that the system meets expectations. The alliance could then recommend the system to the FCC and begin field-test verification of the system's performance.

The FCC in turn will consider the alliance's recommendation in a rule-making proceeding, which alliance members hope can be concluded by the end of this year. Regardless of the adopted standard, the FCC requires that anyone can license the applicable technology on reasonable terms.

Finally, the alliance and the FCC hope that Canada and Mexico initiate similar procedures to assure that the US standard becomes a North American standard. The alliance seems determined not to delay the process to study any other system for which hardware or software doesn't exist.

capabilities with a heavy emphasis on progressive; and the 5.1-channel Dolby AC-3 audio technology for digital surround sound. However, at the time, the alliance did not make one important decision: which transmission scheme the HDTV system will use (see **box**, "Looking ahead").

The alliance also decided on the following scanning formats: 24-, 30-, and 60-frame/sec progressive scan with a pixel-by-line format of 1280×720 and 24- and 30-frame/sec progressive scan with a format of 1920×1080. The system will also perform a 60-frame/sec interlaced scan with a format of 1920×1080. These formats provide a foundation for the migration to the ultimate goal of a 60-frame/sec, 1920×1080 progressive format as soon as technically feasible.

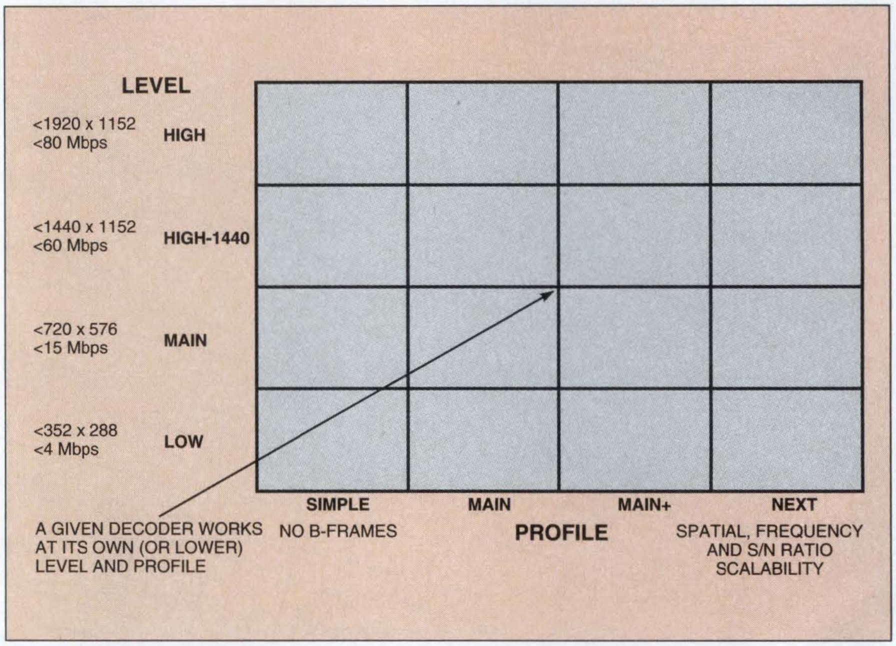

Fig 3—MPEG-2 is not one exact standard but more of a tool kit that addresses a variety of cost and performance requirements. The *level* and *profile* syntax refers to various resolutions and decoder features, respectively.

MPEG-2 plays a major role

The chosen digital video-compression technology, based on MPEG-2 parameters, forms a major part of the evolving standard. MPEG-2 is not one standard but a kind of tool kit of syntactic elements that encompasses a range of compression grades that vary in performance and cost. **Fig 3** shows the elements of this toolbox—referred to as profiles—vs the formats, or levels, on the y-axis. The profile refers to one of the four types of compression: simple, main, main+, and next.

A given decoder can work at its own profile and its own or lower level. A decoder with a simple profile uses only forward-motion prediction. A main profile implies the use of bidirectional prediction, which requires two frames of storage but improves picture quality. Thus, conforming to a main profile implies a receiver with much more memory than one that conforms only to the simple profile. Operating at different levels requires vastly different data rates, as **Fig 3** shows.

Although the *level* and *profile* syntax defines a certain level of performance, MPEG-2 does not specify any details of the hardware and software architectures that produce this performance. However, the syntax does imply many things. A decoder that performs at the MPEG-2 main profile and high level implies how fast the decoder must operate and how much memory it needs to have. A system that can perform to multiple MPEG formats requires some electronic format-conversion circuitry. System-performance specifications to consider include speed, I/O bandwidth, and memory size. The alliance has yet to nail down the numbers that correspond to these specifications. However, system clock speeds may be as high as 75 MHz.

The MPEG-2 levels and profiles pro-

For more information...

For free information on the MPEG-2-decoder ICs, circle the appropriate numbers on the postage-paid Information Retrieval Service card or use *EDN*'s Express Request service. Also use the following list to directly contact members of the Grand Alliance. When you contact any of the following manufacturers directly, please let them know you read about their products in *EDN*.

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vide the flexibility necessary to deal with compressing, transmitting, and decompressing types of pictures. The need to transmit data at megabits/second over the FCC-mandated 6-MHz channel requires some form of lossy compression. The optimum compression scheme depends on a picture's contents and requires a compromise between spatial resolution, frame rate, and amount of acceptable compression artifacts. Optimum resolutions and rates vary for different kinds of pictures.

With the standard close to completion, much product development will soon be necessary, particularly in the area of displays and powerful compression and decompression ICs. MPEG-2 ICs are already starting to appear. For example, AT&T Microelectronics and SGS-Thomson Microelectronics are both sampling MPEG-2 ICs. The first of a family of MPEG-2 devices planned by AT&T, the AC6101 decodes all the MPEG-2 video layers in real time without external processor support. The device uses a 27-MHz clock and just 8 Mbits of external memory. The chip will be available in volume in the first half of this year. The company hasn't set firm pricing but expects the IC to cost between $50 and $75 in large volumes.

SGS-Thomson's Sti3500 decodes MPEG-1 and -2 bit streams in real time up to a 16-Mbps input-data rate. Samples are available now, and production quantities will be available this quarter. Price is $48 (100,000).

In addition to decoder ICs, the HDTV standard will impact the design of many other systems, including receivers, displays, studio and transmission equipment, peripheral equipment, programming and software-development systems, and semiconductors. Within a year, specific details will be available so that designers can begin work on these products. EDN

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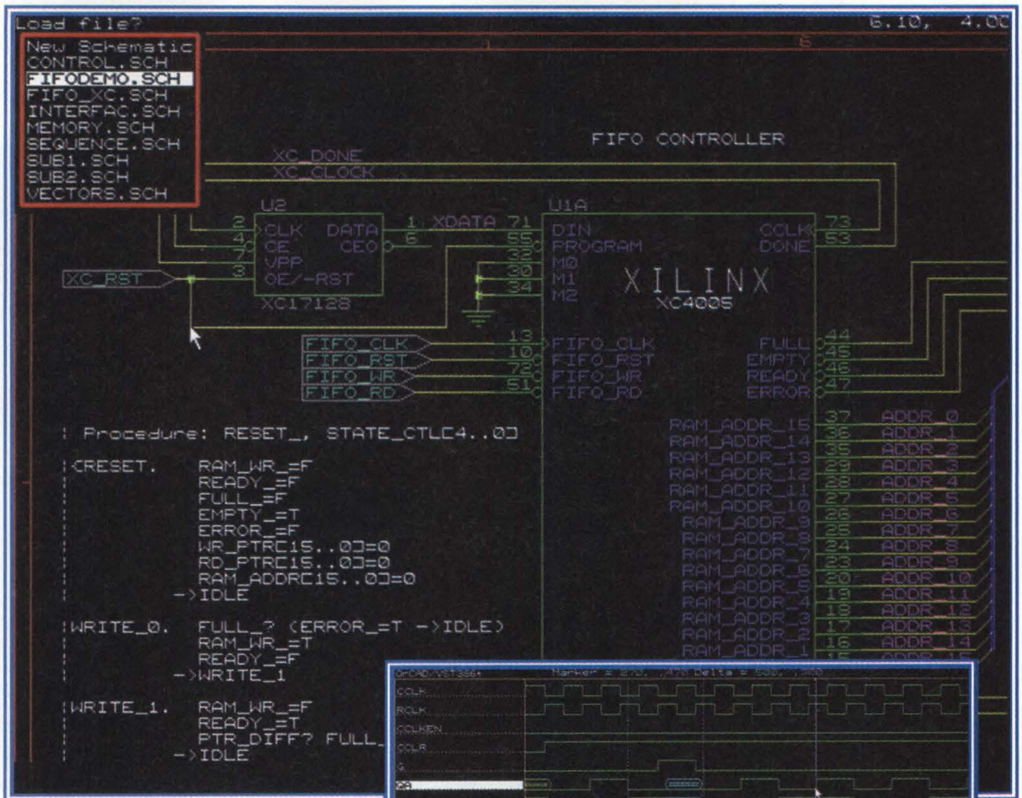

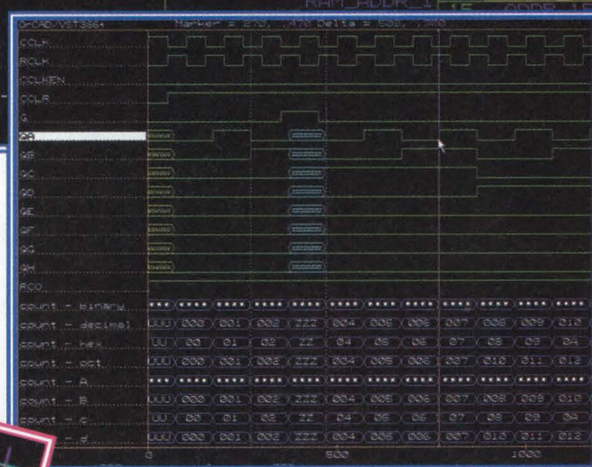

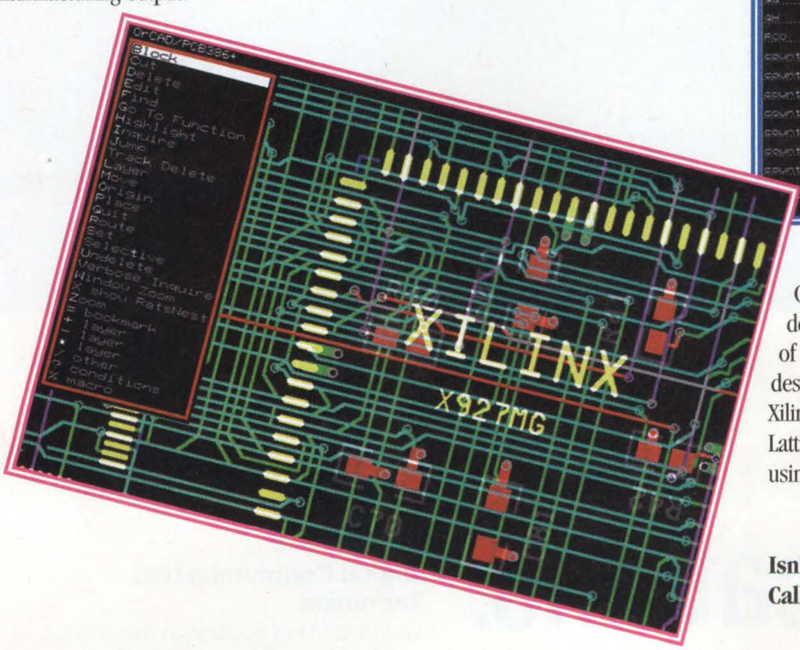

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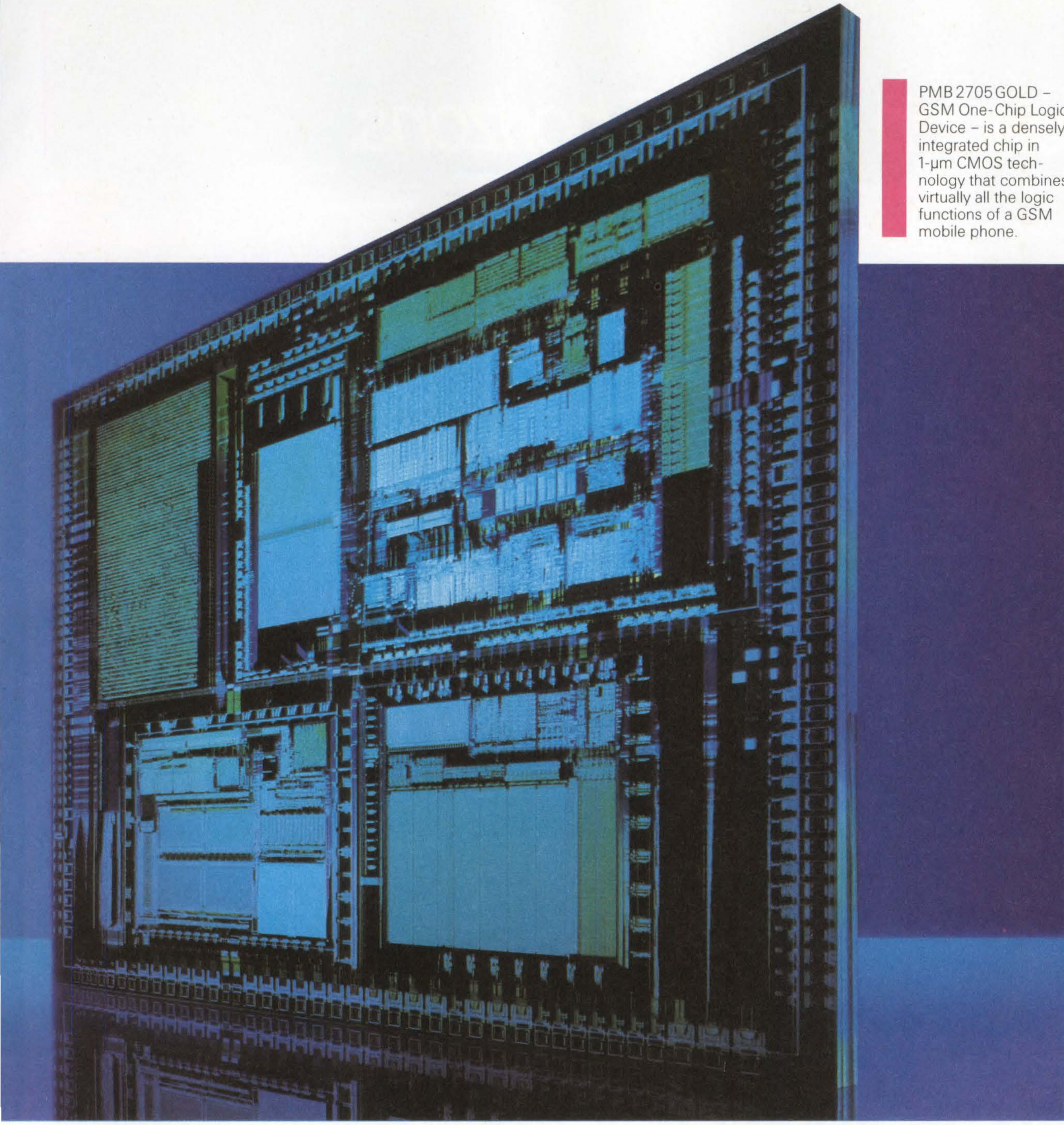

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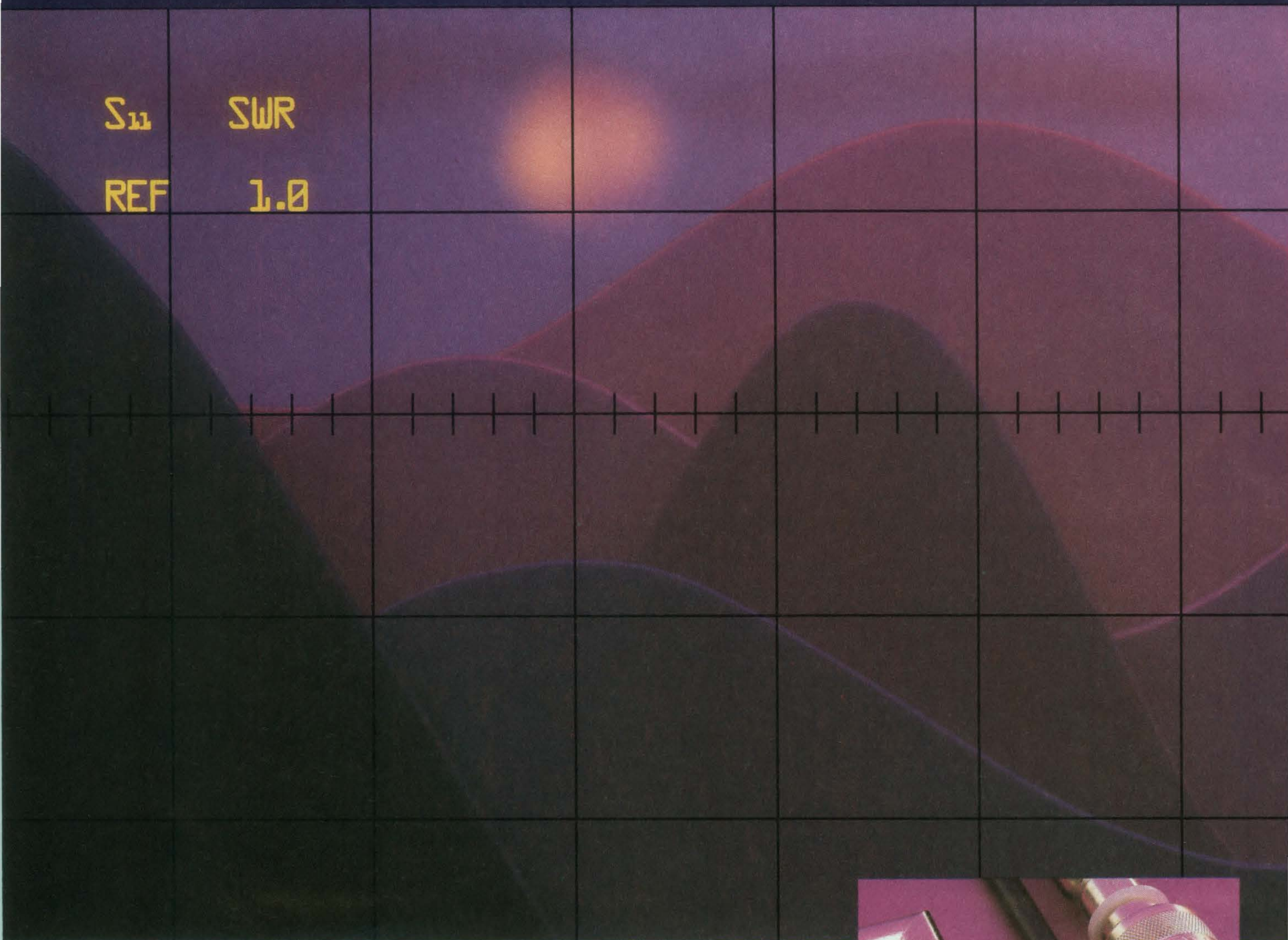

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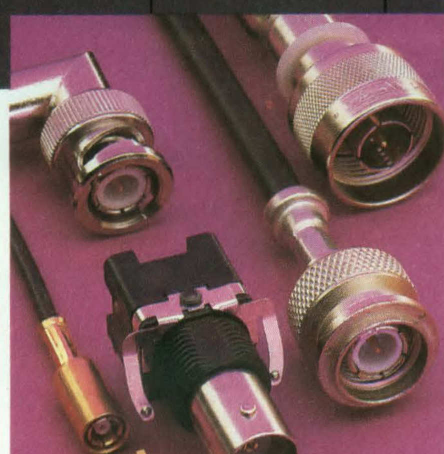

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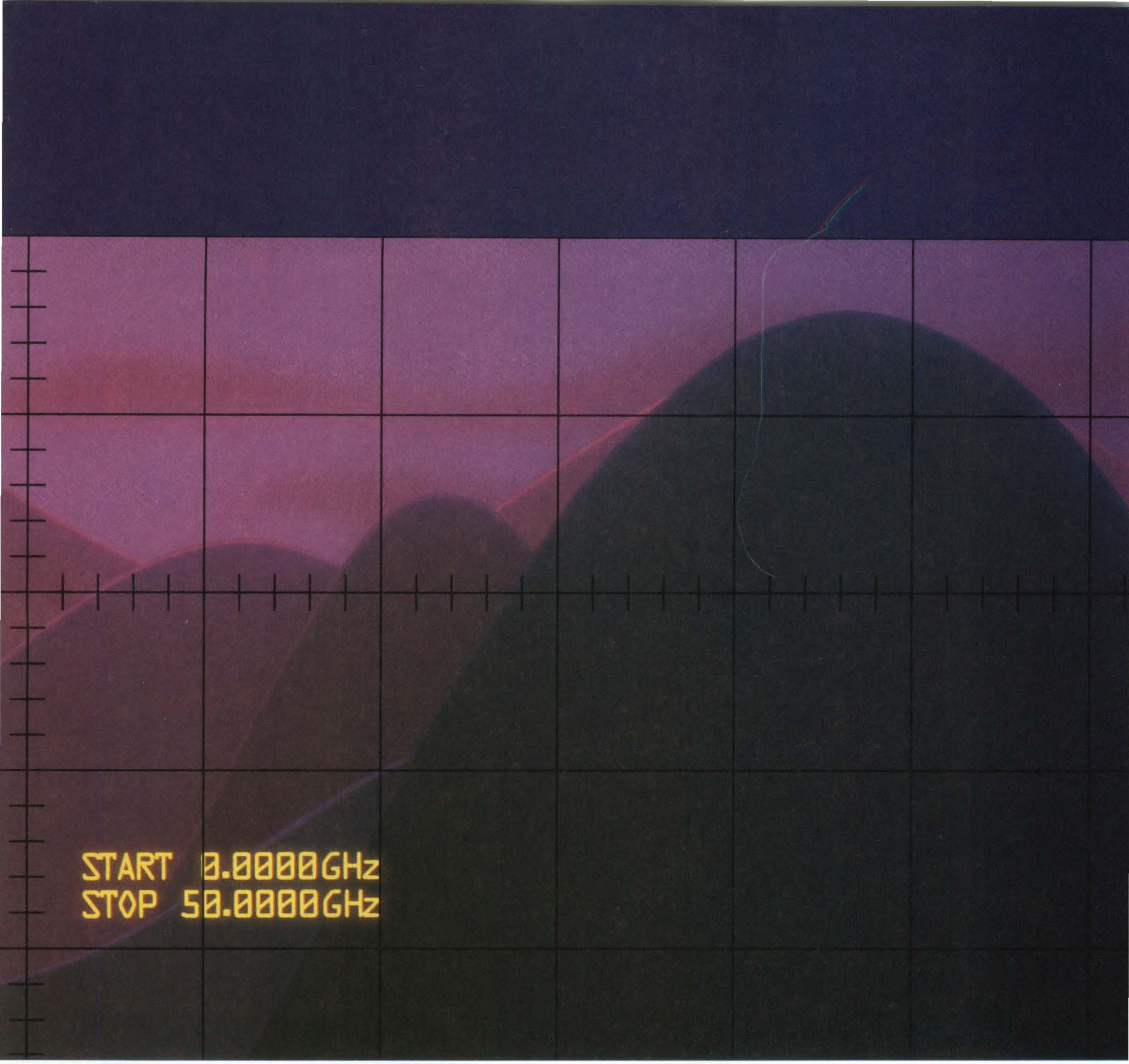

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EMC components administer + first aid +

BRIAN KERRIDGE, Technical Editor

Discovering late in the day that your product fails to comply with EMC regulations implies a tough redesign. A host of passive parts, applied simply and superficially, could be your salvation.

Not often in design work do you get a chance to make a product meet specification by bolting on a few basic parts. With electromagnetic compatibility (EMC), you have that option simply because many EMC failures concern a product's peripheral features such as cabling and apertures. Components such as ferrite cores and beads, feedthrough capacitors, connector shields, gaskets, and conductive tapes can all prevent unwanted signals from reaching the outside world. Conversely, the same components also offer a design some immunity from external interference. Not only do these basic components provide your design an important source of EMC first aid, but they can also throw a permanent lifeline to a finished product that would otherwise be an EMC casualty.

Applying first-aid fixes at the back end of a design cycle opposes almost everything EMC experts believe in. They advise, advocate, and even implore you to design in EMC from day one. That way, you suppress emissions at the source and prevent noncompliant noise levels from ever reaching the extremities of your product. Much of that preventive design work involves building in certain features at pc-board layout (**Ref 1**). While the advice is good—and appeals to the common-sense instincts of most designers—the fact remains that designers' priorities often lay elsewhere.

This situation prevails despite an increasing awareness of the importance of EMC and Europe's EMC Directive (**Ref 2**). That directive will ultimately enforce conformance by law; it applies equally to new products and products designed

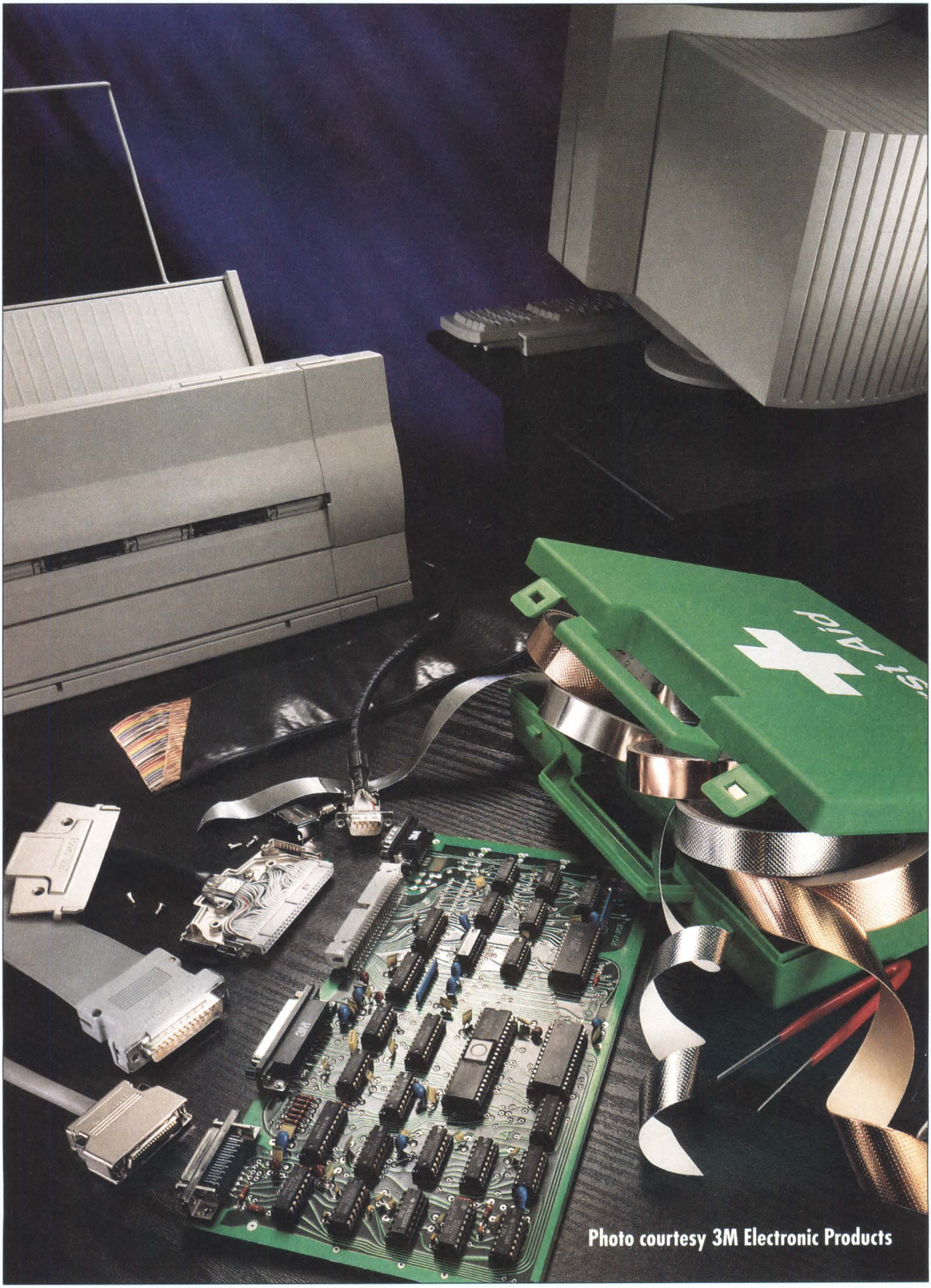


Photo courtesy 3M Electronic Products

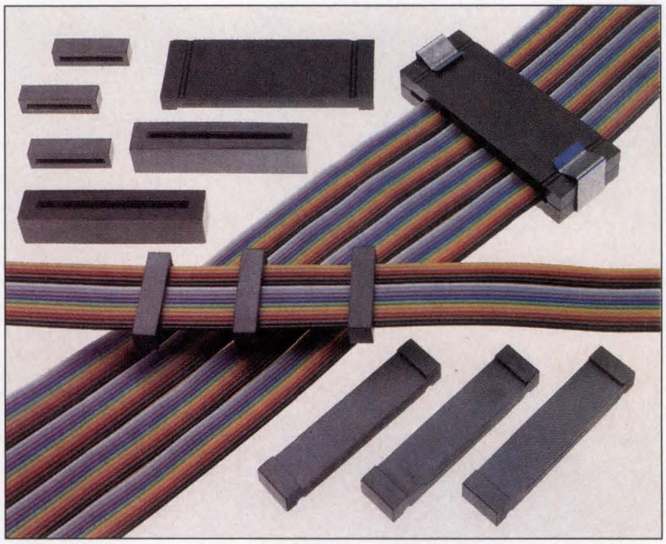
well before EMC became a hot topic. On older designs, applying first-aid measures is the only cost-effective compliance route and represents a genuine need for that approach.

So, for the time being, applying quick fixes remains a popular and necessary way—although not the purist's preferred method—to treat EMC-design problems. For a quick reference, see **Table 1**, which shows the range and variety of EMC components that can administer first aid to a finished design.

Broadly speaking, undesirable emissions occur either as radiations directly from your circuit board or indirectly, first by conduction along connecting cables and then by radiation. Directly radiated emissions leak through apertures or poor electrical joints in a product's shielding, and it's here that conductive adhesive tapes, wire mesh, and gaskets are effective remedies. Connector backshields, filtered connectors, cable shields, ferrites, and feedthrough capacitors all reduce emissions conducted onto connecting cables.

For the purpose of meeting EMC specifications, assume conducted emissions concern signal frequencies of 150 kHz to 30 MHz, and radiated emissions cover 30 MHz to 1 GHz. At present, international standards for conducted emissions consider mainly effects on line cords, and, therefore, it's common practice to design in a line filter. By contrast, standard requirements overlook conducted emissions on I/O cables, and because I/O signals vary widely anyway, these lines are largely left unfiltered. Undesirable emissions on I/O cables give rise to the majority of EMC failures, and radiated-emission tests pick up those failures.

Whatever EMC tools you employ to make your tests (**Ref 3**), it's often most expedient to adopt a trial-and-error approach when solving EMC problems. It helps, though, to have some understanding of what each type of first-aid component can reasonably achieve. In most cases, however, your adding components will not upset the fundamental performance of the product. But in a few cases they can—for example, if you set about filtering a high-speed data bus.



MMG-Neosid's range of ferrite cores includes loops for suppressing common-mode current on ribbon cables. The company also provides Spice models for designing series-mode filters with its ferrite beads.

The difference between series- and common-mode signals is a key distinction to appreciate in addressing EMC problems on cables. Series (or differential)-mode signals are legitimate data signals that consist of signal currents with a forward and return path. Common-mode signals are wholly illegitimate and occur mainly because of poor grounding somewhere in your overall system.

Both series- and common-mode currents can radiate noncompliant emissions, but series-mode problems are fewer simply because of a tendency of radiation from forward and return

Looking ahead

Although EMC specialists regard first-aid measures a nonpreferred route to compliance, there is strong evidence that this is the path many companies will follow.

Tim Williams, EMC design consultant with Elmac Services, notes a wide variation in the way European companies plan to treat product EMC. He says most medium- to large-sized companies now know they need to take action, and that action means a wholesale reeducation program for designers, test engineers, and maintenance staff. Some companies still are totally unaware of the requirements, particularly in European countries having no official "awareness" campaign. It remains to be seen *how* they implement the EMC directive.

At present, Williams says large multinational companies already have, or are developing, internal procedures for designing in product EMC. He also says the majority of other companies plan no action, mainly because they believe the cost of designing in EMC is too high.

In the United States, Joe Butler, director of EMC-testing services at Chomerics, draws a distinction between companies with military- and commercial-product experience. He says military companies have well-established EMC design procedures, but commercial companies, broadly speaking, do not. Butler asserts that apart from large multinational companies with EMC engineers already on staff, most companies, though aware that some EMC testing will ultimately be required, still treat EMC design as an 11th-hour activity.

Butler predicts a mad scramble to have products tested as the 1996 European directive deadline approaches. He estimates the requirement for immunity tests, as well as a wider scope (over FCC requirements) of products needing tests, may surprise some US vendors. In particular, he warns that companies with products currently exempt from FCC regulations and having a lot of mostly unshielded cabling will face serious problems trying to comply.

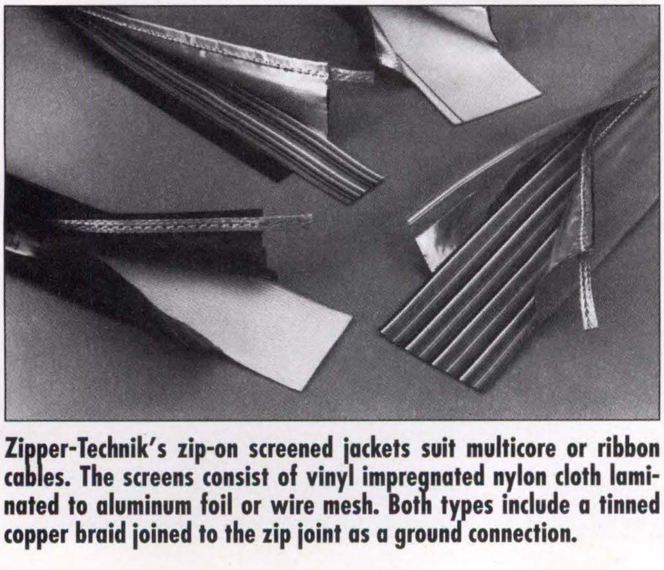
Butler forecasts moves by EMC component vendors to address the needs of commercial users in high-growth markets such as computing and wireless communications. In particular, he sees low cost as the principal driving force in extending acceptance of designing for EMC.

currents to cancel out. Although common-mode currents cause most cable-borne EMC failures, fortunately, it's this type of current that EMC first-aid measures readily suppress.

Your two options are to pass your I/O cable through a single ferrite loop or to insert common-mode chokes in series with each signal and return pair at the I/O interface. Vendors offer ferrite loops in an immense range of sizes, styles, and frequency specifications. To ease installation, loops are round, oblong, and either complete or in halves with a clamp. For both ferrite loops and common-mode chokes, you have to rely on trial-and-error. Most ferrite suppliers encourage this route by offering diagnostic kits containing an assortment of types. Calculations are impossible because you have no idea what value to assign to impedances around a common-mode loop. On that basis, it generally pays to install as large a component as space allows. In the case of ferrite loops, passing a cable through the loop more than once or adding more loops is also beneficial. The merit of ferrites is that they absorb, rather than reflect, radiation locally, and they dissipate the energy as heat.

In the case of series-mode signals, you *can* estimate circuit source, transmission, and load impedances. Therefore, you can design a passive lowpass filter to bandlimit I/O lines (**Ref 1**). The range of filter components is wide, but a common characteristic is definable low inductance. Again, the simplest component is a ferrite core, although in this case the ferrite needs to surround each signal path and needs careful selection. Also available are ferrite plates with holes to match popular connectors' pinout configurations. Other possible filter components include 3-terminal capacitors with and without ferrite beads, chip inductors and capacitors, feedthrough capacitors, and ready-made encapsulated filters.

The easiest and neatest way to apply in-line filtering is either to swap a regular connector for a filtered type or to insert a filtered adapter between your present plug and socket. Filtered connectors exist mainly as replacements for D-type connectors, although you have a wide array of filter-component combinations within the range. With feedthrough capacitor values ranging from 50 to 2000 pF and using or discarding ferrite plate inductors (impedance 35Ω at 100 MHz), you can tailor lowpass bandwidth to your application.



Zipper-Technik's zip-on screened jackets suit multicore or ribbon cables. The screens consist of vinyl impregnated nylon cloth laminated to aluminum foil or wire mesh. Both types include a tinned copper braid joined to the zip joint as a ground connection.

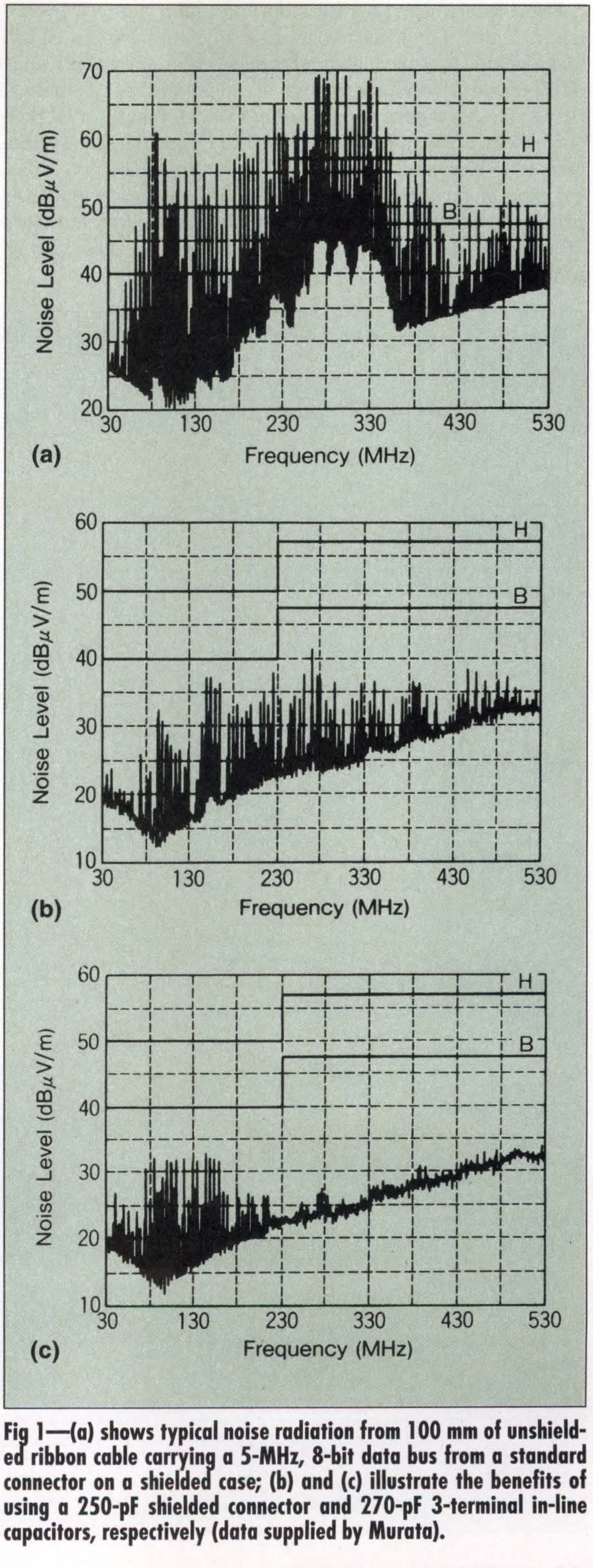


Fig 1—(a) shows typical noise radiation from 100 mm of unshielded ribbon cable carrying a 5-MHz, 8-bit data bus from a standard connector on a shielded case; (b) and (c) illustrate the benefits of using a 250-pF shielded connector and 270-pF 3-terminal in-line capacitors, respectively (data supplied by Murata).

Cable shielding is the next step, and again, your options are many. Your main decisions are how thick to make the shield and whether to make a ground connection at one or both ends of the cable. If your knowledge of shielding theory is rusty, there's no shortage of revision notes (**Ref 1**). Whatever method you choose, a low impedance connection from shield to system ground is essential. The sight of a pigtail connection—alias, common-mode impedance—appalls EMC experts, and it's the primary function of connector back shields to eliminate these offensive joints. Connector backshields, like filtered connectors, generally suit D-type connectors.

If you're using an unshielded ribbon cable, as a first step, try ribbon with a single-sided aluminum-shield backing. Beyond that, you'll need to use a complete braid of zip-on sheath.

If you've applied all the first-aid fixes to your I/O cables, but EMC problems persist, it's time to consider enclosing your main circuit components. Here's where adhesive conductive foils excel. Foils form the most adaptable EMC diagnostic material. Foil material is either copper or aluminum, with a choice of conductive or nonconductive adhesive. Foil surface is either smooth or embossed, the embossed version

Table 1—Representative EMC components

Vendor	Ferrite	Common-mode choke	Filtered connector	Feed-through capacitor	3-terminal capacitor	Cable shield	Connector backshield	Foil	Mesh	Gasket	Other
Adhesive Research Circle No. 334							X				
Band-It Circle No. 335											Cable shield clamp
Beck Electronics Circle No. 336		X									Feedthrough filter
Chomerics Circle No. 337						X		X	X	X	Conductive compound and spray paint
Coolstead Magnetics Circle No. 339	X										
Dontech Circle No. 340											Window shield
Fair Rite Circle No. 342	X										
Ferrishield Circle No. 343	X										
Ferronix Circle No. 345	X										
Ferroperm Circle No. 346	X		X	X							
Instrument Specialties Circle No. 347							X		X	X	Conductive finger strip
Kabelwerk Eupen Circle No. 348											Ferrite-coated cable and tape
Kern Electrical Components Circle No. 350							X				
Kemtron International Circle No. 349								X	X	X	
Kitagawa Circle No. 351	X					X		X	X	X	

Europe's directive forces the pace

Anticipating EMC regulations' becoming law in Europe on January 1, 1996, governmental departments in France, Germany, and the United Kingdom are conducting EMC-awareness campaigns. Efforts in the United Kingdom are particularly strenuous, where the campaign features a free journal for board-level executives; technical reports for people implementing EMC measures; an EMC workbook for people organizing seminars and training; a network of nine EMC clubs for disseminating knowledge; *EMC Update*, a 4-pg bimonthly publication that supports club activities with EMC news and case-study information; and three videos. Also available is an EMC nontechnical telephone help line (dial UK (country code 44) then 61 954 0954), which offers general information, including supply sources for documents and contact names of specialists.

	Ferrite	Common mode-Common	Filtered connector	Feed-through capacitor	3-terminal capacitor	Cable shield	Connector backshield	Foil	Mesh	Gasket	Other
MMG-Neosid Circle No. 352	X										Spice models
Murata Electronics Circle No. 353	X	X	X		X						
Omega Shielding Products Circle No. 355										X	Conductive finger contacts
Oxley Developments Circle No. 354			X	X							Window shield
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Siemens-Matsushita Circle No. 360	X			X	X						
Steward Circle No. 361	X										
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Tusonix Circle No. 363	X										
Warth Circle No. 365						X		X	X	X	Conductive finger strip, window shield
Zipper-Technik Circle No. 366						X		X			

EMC COMPONENTS

providing lower contact resistance (approximately 1 mΩ/in.^{2}) to a supporting surface and other layers of foil.

You can readily fit foil screens to individual components or to whole sections of a circuit as an experiment. You can also use foils to improve contact along enclosure seams, which is a useful way of testing the need for a proper EMC gasket (**Ref 5**). Additionally, where an enclosure is already sealed except for essential display windows or cooling vents, foil temporarily placed across these apertures will also test the likely benefit of installing EMC mesh. Another experimental use of foils is as an alternative to conductive spray paints for lining the inside of plastic product enclosures.

If you reach the stage of installing gaskets, mesh, or EMC windows, then your work transmutes from low-cost first aid to high-cost intensive care. But, this is the penalty you pay for ignoring experts' words of caution. Even so, applying exotic modifications this late to a design may still be the most profitable way forward. For, as well as providing permanent low-cost solutions, EMC first-aid components will sustain a product at higher cost until it's convenient or worthwhile to conduct major surgery. EDN

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5. Bates, Ron, "EMC Gaskets—Traps to Avoid," Euro-EMC conference proceedings, Ibid.

Acknowledgment

Thanks to Tim Williams, EMC design consultant with Elmac Services, for advice and guidance with this article.

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Article Interest Quotient
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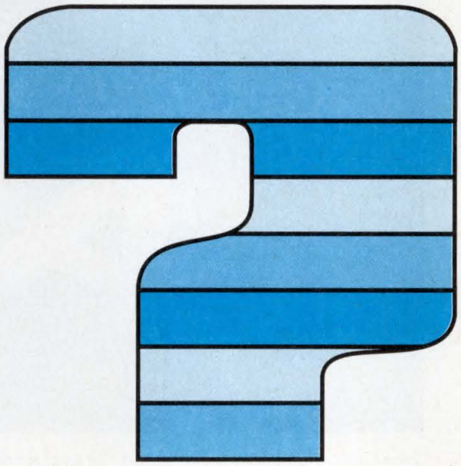
Do you get 24-bit true color at 1024 x 768 resolution from your PC graphics designs?



You can with TI's TVP3020. The 64-bit, low-cost video interface palette.

The TVP3020 from Texas Instruments is the industry's first video interface palette to offer a 64-bit pixel bus plus a separate VGA port, making it an excellent choice for PC graphics/Windows™ accelerators. And it's flexible. The TVP3020 is available in three speed grades of 135 MHz, 175 MHz and 200 MHz so its benefits can be achieved on engineering workstations and color X-terminals as well.

TVP3020 Color Depth and Resolution

Screen resolution	Approximate dot-clock (72 Hz frame rate)	Max. number of colors† 64-bit pixel bus palette (TVP3020)	Typical 32-bit pixel bus palette
1024 x 768	85 MHz	16 million (24-bit true color)	64K
1280 x 1024	135 MHz	64K (16-bit true color)	256
1600 x 1280	200 MHz	64K (16-bit true color)	N/A

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• Faster graphics performance	• Hardware cursor
• Lower cost external TTL PLL	• Internal frequency doubler
• More accurate color rendition	• Gamma-corrected true color
• Control of overlays for multimedia	• Color-key switching

The TVP3020 allows flexibility in designing photo-realistic graphics systems up to 16 million colors. It enables you to support 24-bit true color at 1024 x 768 as well as 16-bit true color at both 1280 x 1024 and 1600 x 1280 with a single design.†

TVP3020

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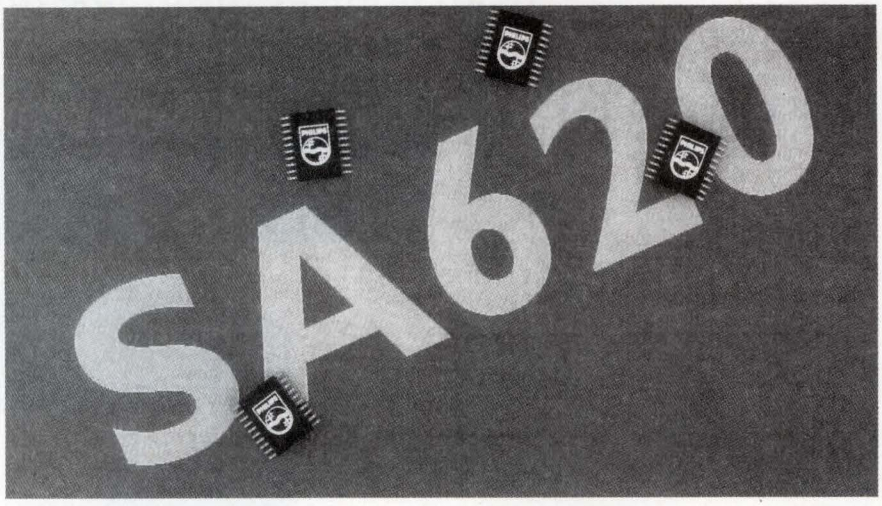
Philips Semiconductors **Update**

First one-chip receiver front-end for advanced wireless designs



Low power consumption makes the SA620 ideal for portable wireless communication units.

The SA620 is the first RF IC to integrate a low-noise amplifier (LNA), mixer and voltage-controlled oscillator (VCO) in a single 3 V device. It replaces up to 20 discrete components in 900 MHz cellular and cordless phones, allowing designers to cut design cycles while increasing reliability and dramatically reducing size.

The Philips development is a complete 3 V front-end solution based on advanced QUBiC™ BiCMOS process technology, with performance that surpasses today's best silicon and GaAs discrete designs. Applications include portable cellular radios (900 MHz), cordless phones, RF data links, UHF frequency conversion and spread spectrum receivers.

The LNA, which is matched to 50 Ω, exhibits a 1.6 dB noise figure and 11.5 dB power gain at 900 MHz. The active mixer supplies an additional 3 dB of power gain with a 8.5 dB noise figure. The integrated VCO reduces external component cost and simplifies design; an internal tracking bandpass filter and automatic levelling loop removes spurious responses and maintains a constant signal level into the mixer.

Low power consumption (10.4 mA at 3 V) makes the SA620 ideal for portable wireless communication units; fast power-down functions for the LNA, mixer and VCO further cut current consumption to 1.2 mA. The SA620 is housed in the SSOP20, the smallest commercially-available surface mount IC package.

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High-speed depletion-mode FETs offer big savings in telephone applications

Introduced for use as line current interrupters in telephone sets, new n-channel depletion-mode vertical D-MOS FETs from Philips can be driven directly from low voltage CMOS logic, permitting the elimination of as many as six gate-drive components from telephone designs.

Compared with the p-channel enhancement-mode FETs which are frequently used in this application, the new depletion-mode devices can result in simpler and more cost-effective line interruption circuitry for new telephone designs, particularly when the FETs are used with telephone ICs from Philips such as the PCA1070 multi-standard CMOS transmission circuit.

The devices feature a maximum drain-source voltage of 250 V and an on-resistance of 20 Ω. With a drain current capability as high as 250 mA DC and maximum switch-on and switch-off times of 10 and 30 ns respectively, they are also suitable for general industrial applications such as high-speed switches, line transformer drivers and relay drivers. For maximum design flexibility, the BSD254, BSP124 and BST124 provide approximately the same FET specification in TO92, SOT223 and TO126 packages respectively, with the TO92-packaged device available in three different pin-out arrangements.

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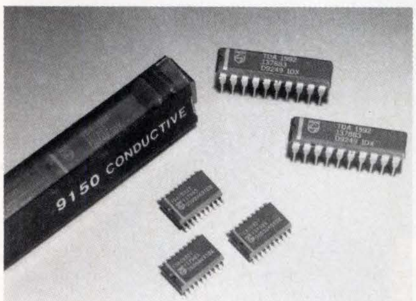
Philips Semiconductors

Stereo decoder/noise blanker enhances car radio performance

Targeted for use in high-performance car radios, the TDA1592 stereo decoder/noise blanker is pin and function compatible with Philips' existing TDA1591. The new IC offers a very low muting offset at its audio outputs, a superior signal-plus-noise/noise ratio of 82 dB and input overdrive capability of 6 dB, plus an automatic FM/AM high cut control feature which improves sound quality under weak signal conditions.

The stereo decoder section incorporates an alignment-free phase-locked loop that operates with a 456 kHz ceramic resonator, and features a pilot tone detector for automatic stereo/mono switching and pilot cancellation. An additional control input, driven with an analogue voltage derived from the receiver's IF stage level detector, allows smooth stereo/mono changeovers as the received signal strength increases and decreases.

Soft muting is performed before demultiplexing of the input signal into the stereo channels and results in a DC voltage shift at the decoder's output of less than 50 mV, making interruption for RDS updating free from audible clicks. To eliminate ignition noise and



The TDA1592 stereo decoder/noise blanker for high performance car radios is available in 20-pin DIL or SO packages.

other pulse interference, the TDA1592's noise blanker detects these pulses and gates them out of the audio outputs. The ability to sum the MPX audio signal and an IF-stage-derived interference signal at the op-amp input, combined with an automatic sensitivity control in the circuit's interference detector, ensures optimum triggering of the noise blanker under all signal conditions.

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Single-chip speech, transmission and listening-in circuit optimizes featurephone performance

Two new high-integration-level bipolar ICs from Philips Semiconductors provide speech, transmission and listening-in functions designed for optimum performance over a very wide range of telephone line conditions.

The TEA1096 and TEA1096A feature a unique active set impedance, the value of which is programmed by an external CR network, which compensates complex line impedances to maintain a flat frequency response on the telephone line over a 3.4 kHz speech bandwidth. Speech quality is further enhanced by dynamically limiting the signal amplitude in the ICs' microphone and loudspeaker amplifiers to prevent clipping in their output stages under input overdrive or low line supply conditions. Automatic gain control in the microphone and receiver channels compensates for line losses, which are deduced automatically by sensing the available line current.

On-chip current-splitting voltage regulation ensures that the maximum amount of line current is available to drive the listening-in loudspeaker under all line conditions. The line current sensing used by the AGC circuit is also used to switch

The TEA1096 and TEA1096A offer highly integrated single-chip solutions to all the speech, transmission, listening-in and line monitoring functions required in modern line-powered featurephones.

automatically between two anti-sidetone networks optimized for short and long telephone lines.

The TEA1096 has an adjustable stabilized voltage output to supply peripheral circuits, while the TEA1096A has a fixed voltage stabilizer but features DC voltage control of the loudspeaker volume. Both ICs are available in 28-pin DIL or SO packages.

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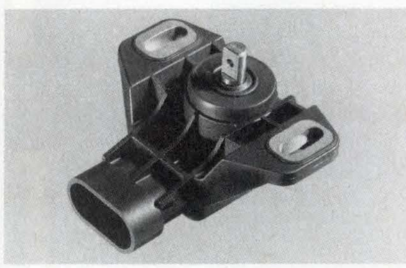
Contactless angular-displacement sensor is encapsulated and ready-to-use

The new KMA10/70 contactless sensor provides a fully-encapsulated, non-wearing and adjustment-free solution to angular position measurement in a wide range of automotive and industrial applications such as active suspension units, accelerator pedal position sensing and servo control actuators. Its sealed housing, wide operating temperature range and high degree of EMC immunity make it particularly useful in safety-critical applications.

Based around the Philips KMZ11B1 magneto-resistive sensor element, the KMA10/70 has an integral input shaft which allows the magnet's magnetic field to be rotated over the sensor element. The resultant changes in the sensor element's resistance are detected by a thick-film hybrid signal conditioning circuit which produces a temperature-compensated 4 to 20 mA output signal that matches the angular displacement of the input shaft. The sensor has a displacement range of ±35° and is free from the microlinearity error and noise problems associated with potentiometers,



The KMA10/70 contactless angular-displacement sensor is fully-encapsulated to survive extreme environmental conditions.

particularly when they suffer wear and corrosion.

The KMA10/70 has an operating temperature range of –40 to +100°C and a lifetime in excess of 10^8 operating cycles. It is a 3-terminal device which operates over an 8.1 to 11.0 V supply voltage range, producing a short-circuit-protected, current-mode output which is independent of supply voltage changes.

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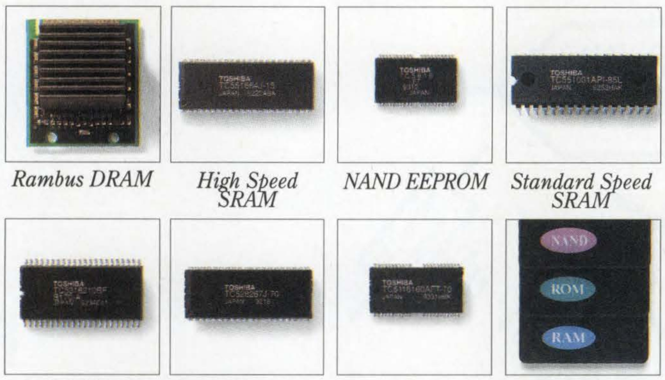

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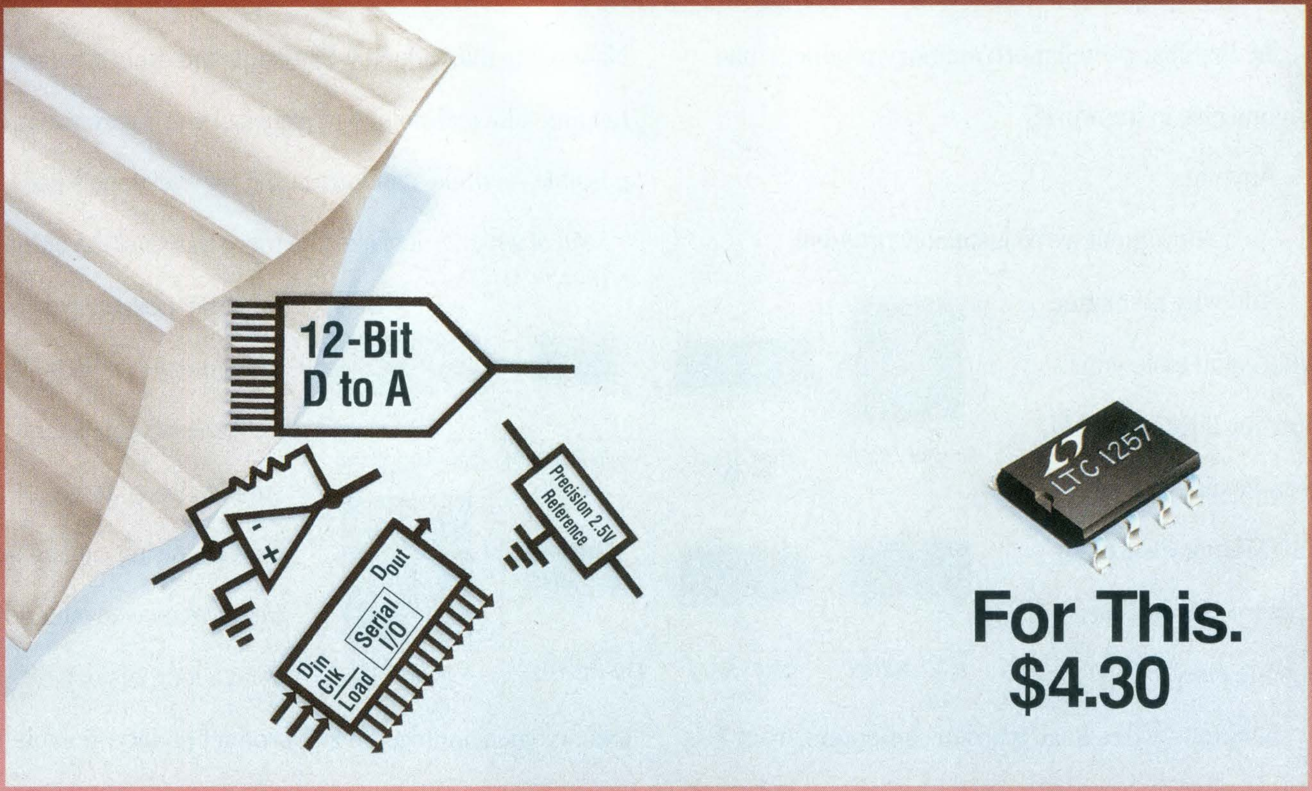
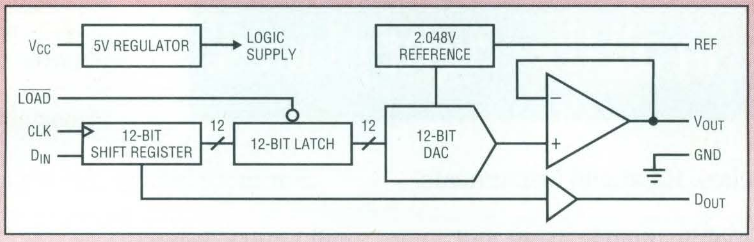


The LTC1257. Complete 12-Bit Serial SO-8 DAC.

Using a 12-bit DAC is now easier than ever! The new LTC1257 is a complete 12-bit DAC in a very small 8-pin SO package. No external components are needed. And the price may be the easiest thing of all! Included is an output buffer amplifier, a 2.048V voltage reference and an easy to use cascadable three-wire serial interface.



The power supply current is a very low 350μA typ. when using a 5V supply. Excellent differential non-linearity—less than 1/2 LSB—guarantees monotonicity and makes the LTC1257 ideal for control and adjustment applications. And you get flexibility—the single supply voltage can go from 4.75 to 15.75 volts and you can override the internal reference to extend the output range as high as 0-12 volts.

The DAC's small size and low power consumption make it ideal for battery powered systems. And with the cascadable serial interface, applications using multiple DACs are a breeze. So if you want to reduce your system cost and complexity, the LTC1257 is a natural choice. Parts are available in 8-pin SO packages or 8-pin DIP. Pricing in 1000-up quantities starts at $4.30. For more details, contact Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035/408-432-1900. For literature only, call **1-800-4-LINEAR.**

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CIRCLE NO. 62

EDITED BY CHARLES H SMALL & ANNE WATSON SWAGER

Color video travels on twisted-pair cable

Raphael Horton, National Semiconductor, Santa Clara, CA

Telephone lines and local-area networks commonly use inexpensive twisted-pair cables. Video-system designers can also take advantage of this low-cost cable to transmit composite-color-video signals. Using the circuit techniques in **Fig 1**, you can transmit video anywhere phone lines exist. Although the circuit has more electronic components than the traditional single amplifier used to drive a coax cable, you can easily justify the additional electronics required to drive twisted-pair cables. Four-wire, twisted-pair cable typically sells for 7 cents/ft, yet RG-59 cable can be priced over 20 cents/ft. If just 500 ft of cable is necessary, the cost difference is $65, which more than covers the cost of a few LM6181 amplifiers.

The system consists of two circuits. The first converts the composite video signal to a differential signal using amplifiers IC_1 and IC_2. Using a differential signal reduces line loss and distortion that could occur from driving the twisted pair single ended. Converting the signal to differential also removes possible ground-plane errors that occur when there is a difference in the ground potential between two pc boards.

The circuit has a minimum signal gain of two to compensate for the terminations' 6-dB signal drop. You can easily adjust the gain of IC_2 by decreasing the value of R_G to make up for the line losses caused by various twisted pair and coax cable lengths. R_G serves as a single system adjust and as an optional contrast adjustment for the video system.

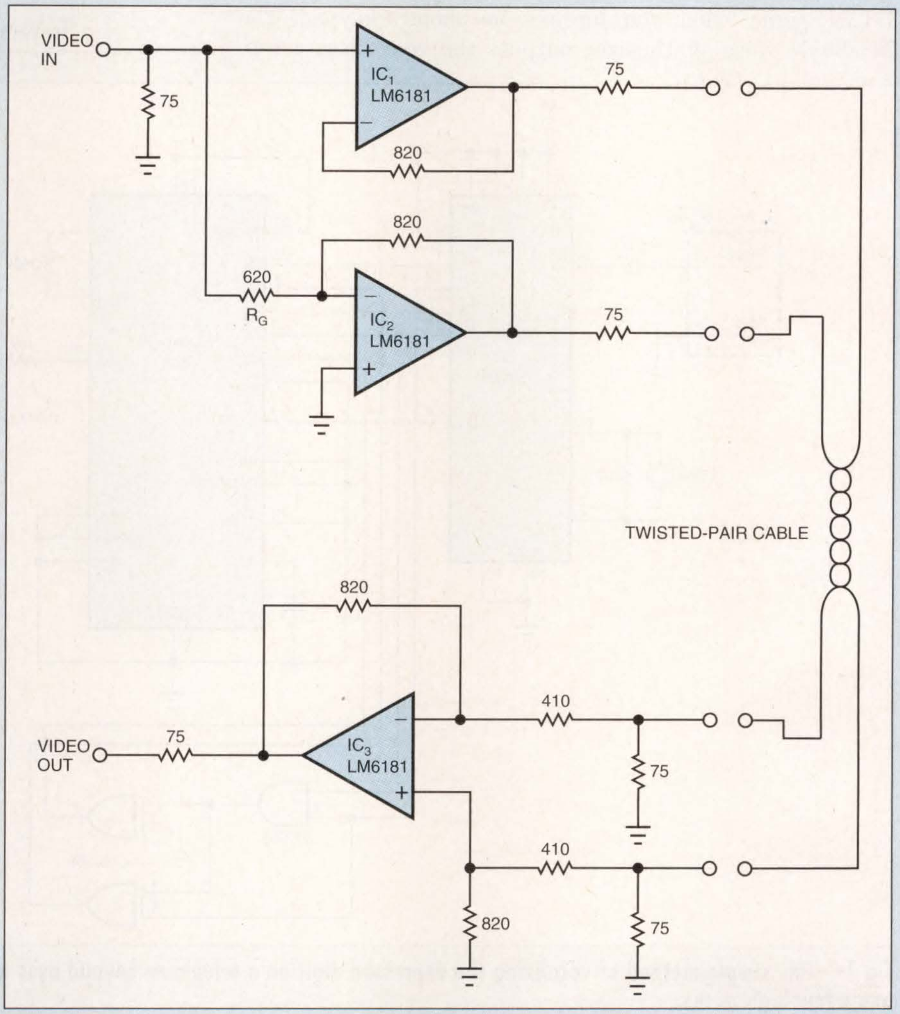

Fig 1—By transmitting differential signals and using video amplifiers with high-output-drive capability, this circuit can drive video signals down inexpensive twisted-pair cable.

In the second circuit, IC_3 converts the differential signal back to single ended. This circuit has a gain of two to drive a back-terminated RG-59 coax cable out to a monitor. The video amplifier you choose for this application must have high-output-drive capability. The LM6181 is guaranteed to drive a back-terminated 75Ω cable over the full industrial temperature range.

This circuit treats the twisted-pair cable as a transmission line that is back-terminated with 75Ω resistors. This termination method is superior to using the 600Ω characteristic impedance of the twisted-pair. A 600Ω termination results in smearing and blurring caused by the RC time constant of the cable capacitance and the termination resistance. Because an increasing RC time constant degrades sharp signal transitions, this circuit uses standard 75Ω terminations to maintain a clear, sharp picture. This circuit does not use shielded twisted-pair cable because of its high distributed capacitance, which contributes to the RC time constant.

No visible difference exists between a reference picture and a transmitted one. Using a Tektronix-type 520 NTSC vector-scope, the measured differential gain and phase of the entire system—which comprises three LM6181 amplifiers, a 100m twisted-pair cable, and a 50-ft RG-49 coax cable from amplifier IC_3—was less than 0.5% and 0.6°, respectively. Keeping the current-feedback amplifiers' feedback resistors equal to the recommended value of 820Ω gives the op amp its proper frequency compensation. The feedback resistor sets amplifier bandwidth and is always required for proper operation, even in unity gain. **EDN BBS /DI_SIG #1361** EDN

To Vote For This Design, Circle No. 435

Circuit vocalizes telephone number

Shwang-Shi Bai, Chun-Shan Institute of Science and Technology, Lung-Tan, Taiwan

The circuit in **Fig 1** is a simple method of vocalizing the digit number of a telephone keypad, which, for someone visually impaired, provides helpful voice confirmation. A 75T202 dual-tone multifrequency (DTMF) receiver decodes the DTMF signal when you depress the phone's keypad. The TC8801N voice synthesizer outputs the voice data corresponding to the data input code. A TA7368P audio power IC amplifies the result. The logic gates perform necessary code conversion for the voice-synthesizing IC's input.
EDN BBS /DI_SIG #1357

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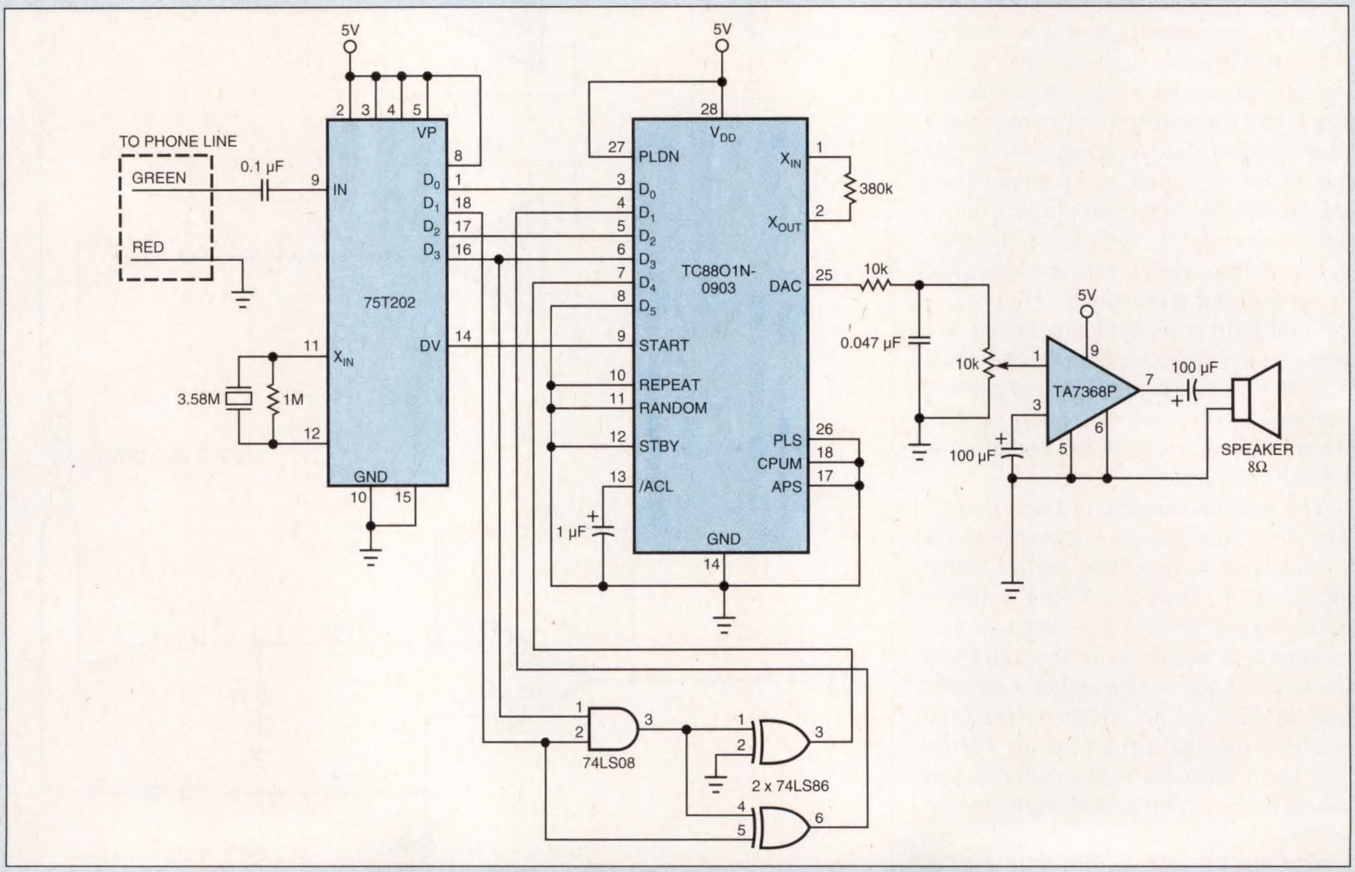

Fig 1—This simple method of vocalizing the depressed digit on a telephone keypad uses a DTMF receiver, voice synthesizer, audio amp, and a few logic gates.

MOSFET replaces switch

Malcolm Watts, Wellington Polytechnic, Wellington, New Zealand

By using a cheap, readily available MOSFET, you can use a single-pole switch to turn a bipolar power supply on and off without consuming extra power. In **Fig 1**, the switch simply controls the MOSFET gate, which switches on the negative supply. Resistor R, which can be several megohms, is not necessary if the ±6V rails are permanently connected to a load, for example an op-amp circuit. Because the MOSFET's $R_{DS(ON)}$ is a fraction of an ohm, power loss is minimal, and the circuit suits moderate-consumption, battery-operated circuitry. **EDN BBS /DI_SIG #1360**

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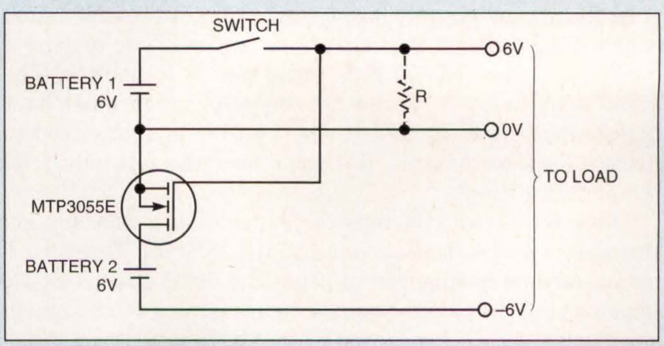

Fig 1—The switch simply controls this circuit's MOSFET gate to turn the negative supply on and off.

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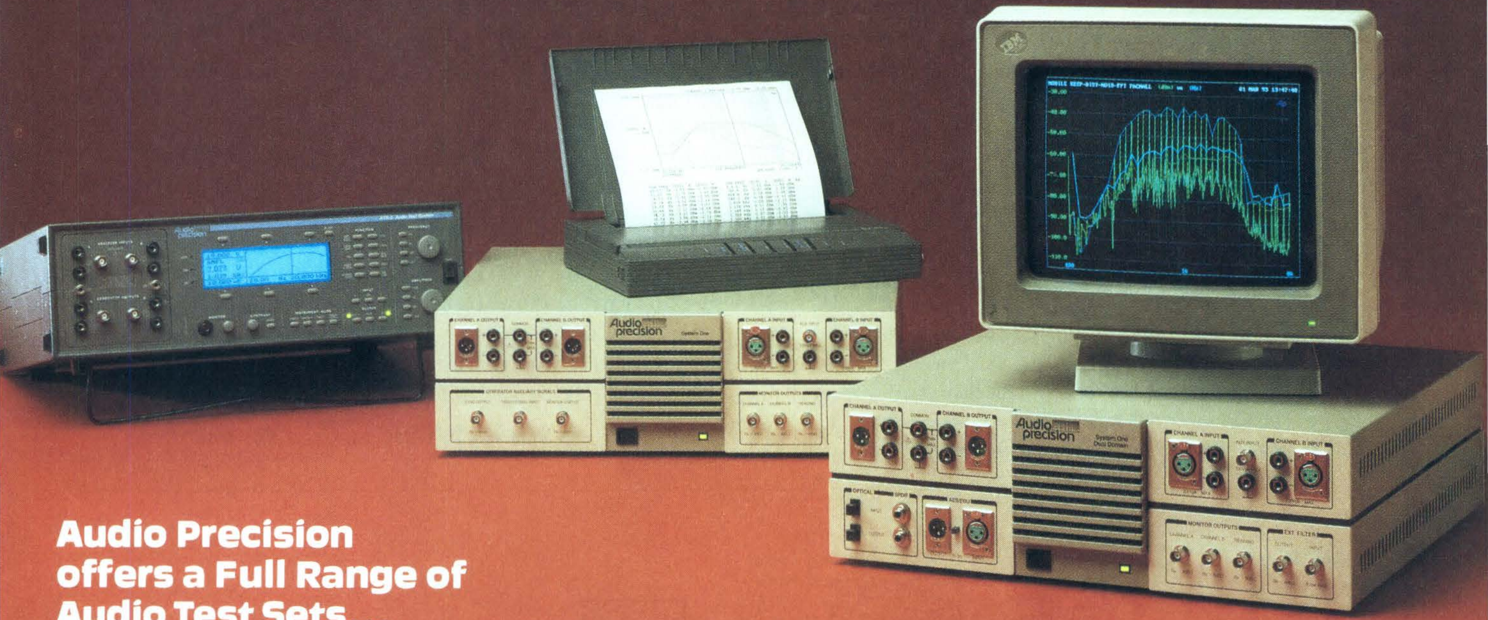

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[1]Sample suite of GPIB programmed audio measurements included 1) noise measurement (20Hz-22kHz bandpass), 2) 31 point single tone frequency response sweep over 20Hz-22kHz range, and 3) 11 point distortion sweep over 20Hz-22kHz range.
[2]*FAST*TEST uses multi-tone stimulus and analysis to make the same measurements listed above.

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CIRCLE NO. 63

Correlator works in presence of noise

John Charlton, Lancaster, CA

The clipped-signal correlator in **Fig 1** outperforms any resistor-capacitor clipped-signal correlator, and the circuit has no race paths.

In operation, the reset signal first clears IC_3 and IC_4 to all zeros. Signals 1 and 2, both of which are clipped so that they resemble square waves, beat against each other in XOR gate IC_1. If Signals 1 and 2 are both the same value at the instant the clock signal CK goes low, counter IC_3 counts. The clock signal's frequency must be high enough that the clock signal takes five to 20 samples of the IC_1's output before IC_1 changes state. You have to determine the appropriate clock rate for your application.

IC_3 and IC_4 are in a race to see which counter finishes first. If IC_4 completes its count before IC_3, IC_{6A} will clock a zero into shift register IC_7. If IC_3 completes its count (that is, the inputs are correlated during enough of the sampling period), then IC_{6A} clocks a one into the shift register.

Each one clocked into the shift register IC_7 energizes a voltage increment. Summer IC_8 totals all of these increments, and comparator IC_8 compares the total voltage to a reference voltage. (The **figure** shows a single shift register for clarity. An actual implementation of this concept used four shift registers in series, yielding a 32-bit comparison.)

To calibrate the circuit for your application, first apply test signals to the inputs. You must use a signal generator that can produce test signals having your required S/N ratio. Then experiment by connecting different combinations of the Q outputs of counter IC_4 to the 8-input AND gate, IC_5. When you get just the right combination of outputs connected, IC_{6A} outputs equal numbers of ones and zeros. Although this condition may sound vague and difficult to detect, don't worry; when you hit the right combination, the circuit snaps into calibration. Continue experimenting to determine the proper threshold for the summer/comparator circuit.

This circuit works with any logic family and most common op amps. The resistors at IC_7's outputs are usually all the same value. You could use differing values, but doing so always causes a processing loss. The circuit's detection-update rate is the rate of the RESET signal, and the integration time is equal to the number of bits of shift register IC_7 divided by the RESET signal's rate. EDN

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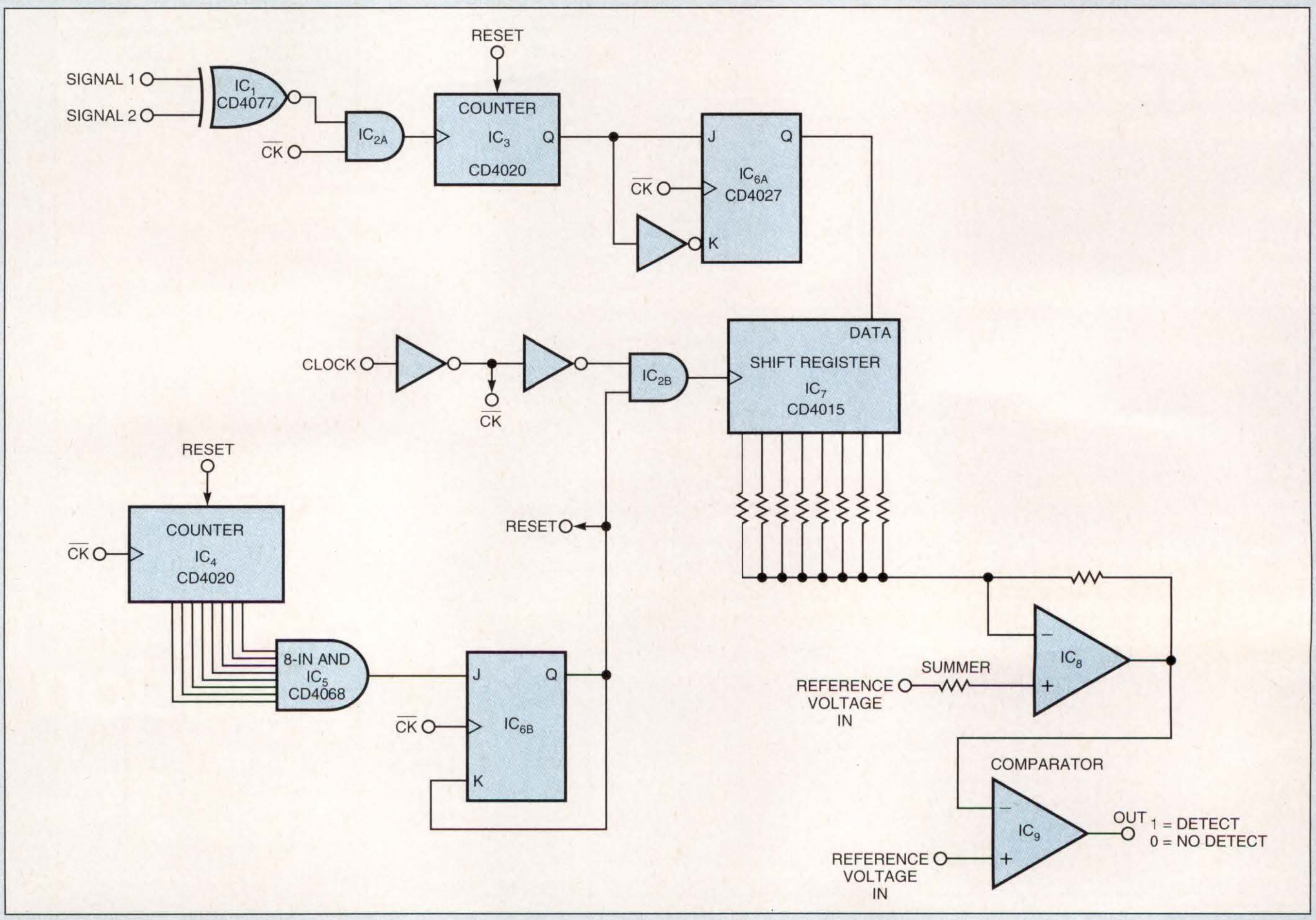
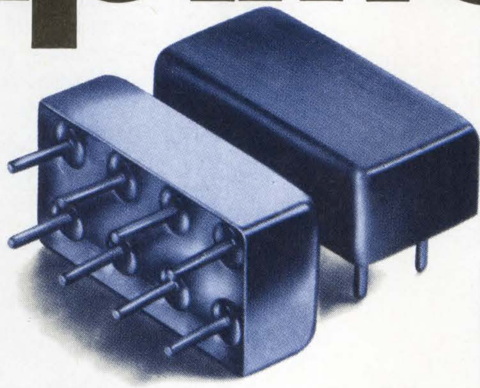


Fig 1—This correlator can determine when two signals are substantially the same, even in the presence of noise.



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Step-up/step-down converters power small portable systems

Bruce D Moore, Maxim Integrated Products

Using four alkaline AA cells to power a product has many advantages. Simplicity of the regulated supply, however, isn't necessarily one of them. Even so, you have several choices of regulator topology—each with strengths and weaknesses.

In small portable systems, marketing considerations—not engineering convenience—often drive the choice of a battery. A classic example is the battery that comprises four alkaline AA cells. AA cells are available in gift shops around the world. Though they are slim enough to fit in handheld systems, four of them can drive a 1W system all day.

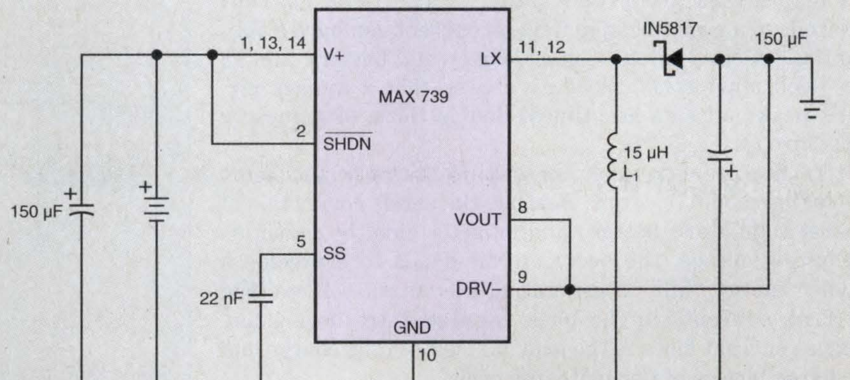
Ref 1 reviews practical regulator topologies for battery-powered systems, emphasizing low-power, nonisolated regulators. It compares the circuits with each other and explains how to choose the one that best suits a given application. An important—and related—problem is deriving the regulated 5V from a 4-cell battery stack.

The voltage available from four alkaline cells in series (6.2V, gradually declining to 3.6V), is not a convenient input for a 5V regulator. The battery voltage ranges above and below 5V, so the usual designs—buck and boost regulators—won't work. Moreover, not only must the regulator boost and buck, but it also must exhibit high efficiency, low supply current, and small size. Although these requirements present a challenge, many circuits can meet them. The following are several possibilities:

Many topologies

Of the many solutions to the 4-cell problem, none stands out as the clear winner. Instead, each option offers tradeoffs in size, efficiency, input range, and other parameters. Some general circuit configurations include

- Flyback
- Inverter
- Low-dropout linear regulator
- Boost with linear postregulator
- Boost with linear preregulator
- Step-up/step-down topology.



L_1 = SUMIDA CD75-150

INPUT VOLTAGE RANGE = 3.8 TO 11V
INPUT VOLTAGE RANGE (NONBOOTSTRAPPED MODE) = 3.8 TO 16.5V
START-UP SUPPLY VOLTAGE (I_{LOAD} = 0) = 4V MAX
QUIESCENT SUPPLY CURRENT (V_{IN} = 5V) = 1.8 mA
MAX LOAD-CURRENT CAPABILITY (V_{IN} = 5V) = 200 mA
BATTERY LIFE (4 ALKALINE AA AT I_{LOAD} = 100 mA) 13.5 HOURS

Fig 1—By floating its battery and grounding its output, this negative-boost regulator produces a positive output at its ground terminal.

Other possibilities include the Cuk and various isolated topologies, but these are either too complex or require too many energy-storage elements to be attractive for small battery-powered systems.

Why not flyback?

Flyback topologies seem an obvious first choice for the step-up/step-down problem. Flyback circuits include a transformer that electrically isolates the output winding from the input (battery) voltage, thereby solving a problem that derails the simpler boost and buck topologies. Indeed, any isolated dc-dc supply, including the forward converter, can function as a step-up/step-down converter.

The most serious contender among transformer-isolated regulators is the flyback regulator, whose simple switching circuit requires only one power transistor and a single magnetic core. Flyback circuits have poor efficiency, though, thanks to their high peak currents and consequent power losses.

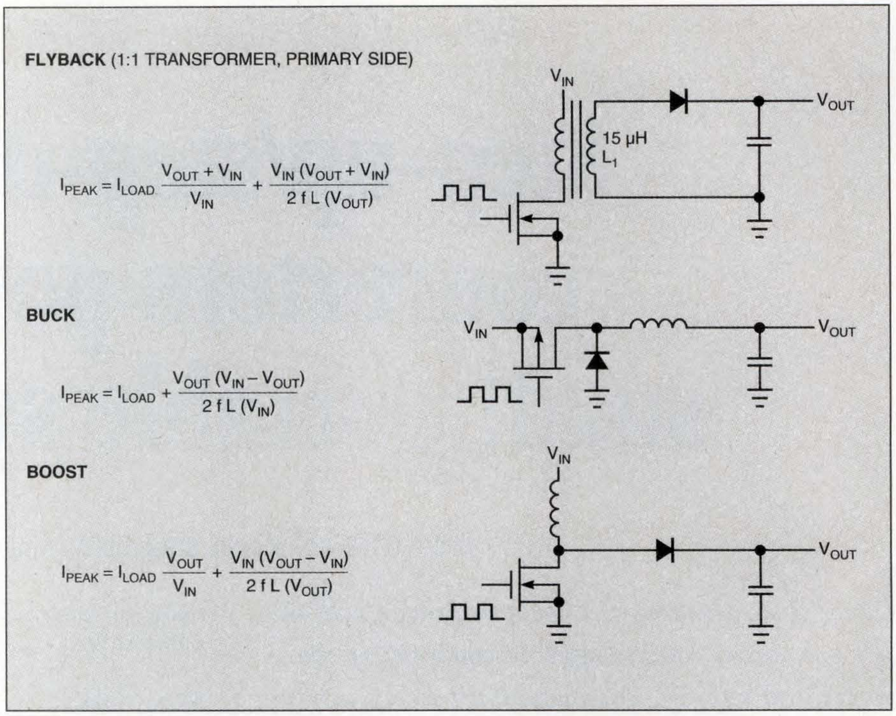


Fig 2—These equations describe the ratio of peak inductor current to average load current for pulse-width-modulated converters operating in the desirable continuous-conduction mode.

Flyback vs buck or boost

To illustrate the flyback configuration's poor efficiency, compare it with the more favored buck and boost topologies. The flyback circuit's main problem is high peak current, which produces high I^2R loss. Peak currents cause dissipation in small parasitic resistances: series resistance in the inductor, on-resistance in the switch, and ESR (equivalent series resistance) in the filter capacitor.

These losses are proportional to the peak current squared, so a minor change in peak current can have a substantial effect on conversion efficiency and battery life. In the 4-cell application, physics ensures that a flyback circuit's peak currents are almost double those of a buck or boost circuit.

It is intuitive that peak currents in the buck and boost topologies should be lower. Because the series connection of a boost regulator's battery and inductor aids the inductor-discharge voltage, the boost circuit needs to overcome a smaller energy "hill" in generating the output voltage (**Fig 1**). Peak currents in the buck regulator are lower, too, because current flows to the load during both the charge and discharge phases of the switching cycle.

I_{PEAK}/I_{AVG} for different topologies

The equations in **Fig 2** describe the ratio of peak inductor current to average load current for pulse-width-modulated converters operating in the desirable continuous-conduction mode. In each equation, the most significant term is the first one, which represents the average dc component of inductor (primary) current. Efficiency in the flyback equation is degraded mainly by the numerator (V_{OUT}+V_{IN}), which represents excessive peak current.

The ac switching loss also degrades the efficiency. This parameter equals V^2fC, where V is the peak voltage swing (equal to V_{IN} for buck regulators or V_{OUT} for boost regulators), and C is stray capacitance at the switching node. For a

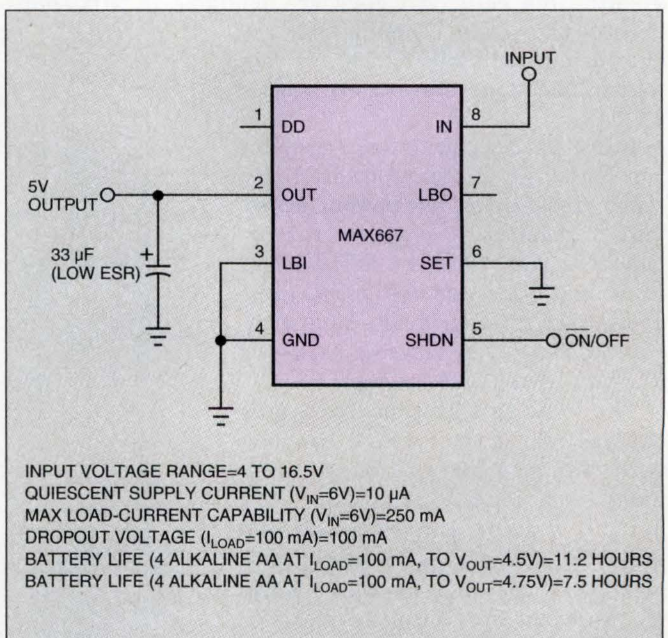


Fig 3—In some applications, a linear regulator with low dropout voltage can deliver more of a battery's energy to a load than can a switching regulator.

flyback circuit with a 1:1 transformer, $V=V_{IN}+V_{OUT}$ (as a minimum).

I^2R and switching losses handicap the flyback configuration. The resulting efficiency (70 to 80%) is inferior to that of buck and boost topologies (85 to 95%). The use of large and expensive power-switching components (or other drastic measures) can raise the flyback circuit's efficiency to 85% or so. Nevertheless, the flyback approach is useful if you need a wide input-voltage range or multiple outputs via extra windings, and if low cost is more important than battery life.

Inverting the battery

Another way to generate 5V from four cells is to first invert the battery voltage with a switch-mode inverter, creating –5V. By connecting this negative output to the system ground you produce +5V at the other output terminal. This approach has some disadvantages, though:

Peak currents are no lower than those in a flyback circuit (indeed, the inverting and 1:1 flyback topologies are exact electrical equivalents). The inverting circuit also joins the 5V output to the battery's negative terminal. This can be a problem if other circuit loads are referenced to ground or if other voltages are generated from the same battery stack. And, finally, the inverting circuit requires a pnp or p-channel FET high-side power switch vs a less expensive and more efficient npn or n-channel FET low-side switch.

Despite the drawbacks, the inverting regulator's simplicity and wide range of input voltage make it attractive for many portable-equipment designs. The wide input range lets the system accept alternate power sources such as ac/dc adapters and 12V lead-acid batteries. As another advantage, the inverter output moves to zero in shutdown mode, a condition not always guaranteed for other regulating topologies.

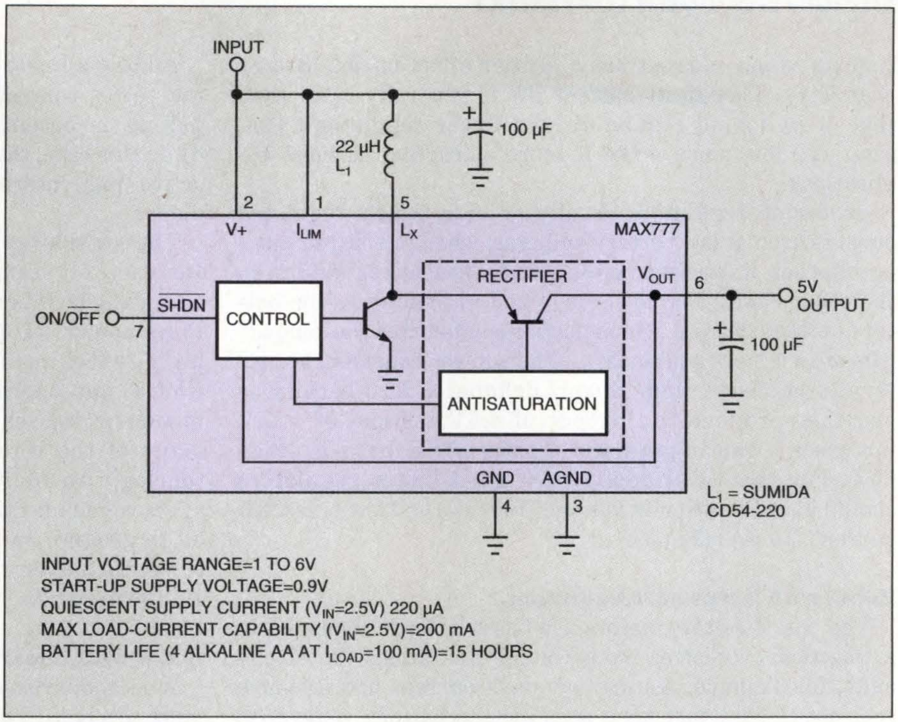


Fig 4—By combining a linear regulator and a switching regulator, this IC prevents the series connection of the inductor and rectifier from pulling V_{OUT} above 5V when the battery is fresh.

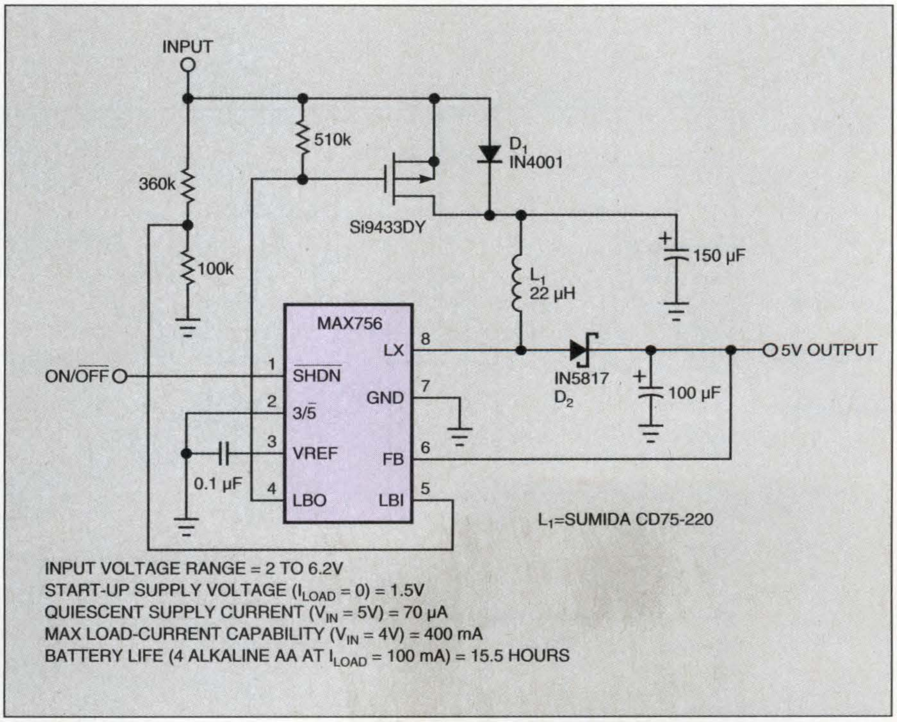


Fig 5—Diode D_1 preregulates the input voltage to this boost switching regulator.

Low-dropout linear regulators

A step-down, low-dropout linear regulator would seem a poor choice for the 4-cell application. It converts only so much of the battery's energy; spent batteries still have considerable energy left in them. Even so, the linear regulator offers better battery life than some switching regulators. In the 4-cell application, the theoretical efficiency is lowest when the battery is fresh ($5/6V \times 100\% = 83\%$) and rises toward 100% as the battery voltage approaches 5V.

What's more, the heat and I^2R losses associated with pulsed current are absent in a linear regulator, and the continuous supply current has a gentler effect on the battery chemistry. Though its battery life is generally lower than that of switching regulators, the linear regulator's cost, size, and low noise make it more attractive in some applications.

Switching regulators usually provide tightly regulated outputs even at low battery voltages; when the output finally collapses, it does so in milliseconds. Linear regulators, on the other hand, drop out slowly and gracefully as the battery voltage decays. This behavior complicates the comparison of switchers and linears. When do you consider the battery to be discharged? Simply defining a dead battery as one that produces an output of 4.5V instead of 4.75V increases a linear regulator's battery life by more than 50%. For the 4-cell application, good linear regulators should have low dropout voltage (100 mV) and low quiescent current (10 μA) (**Fig 3**).

Boost with linear postregulation

The best 4-cell regulators use boost or buck topologies in a way that overcomes input-voltage limitations. Boost circuits, for example, feature low peak current and a simple schematic. They just keep boosting the battery voltage (to 5V) until the battery's energy completely dies.

Adding a linear regulator to a boost regulator prevents the series connection of the inductor and rectifier from pulling the output above 5V when the battery is fresh (**Fig 4**). In this case, the linear regulator is implemented with an active (pnp) internal rectifier instead of the usual Schottky diode.

The switching-regulator IC in **Fig 4** is also unusual. Instead of a standard CMOS or "junk" bipolar process, this chip is fabricated with an advanced, complementary-bipolar RF process. The result is a combination of high switching frequency (normally the strength of CMOS) and operation below 1V (normally a strength of bipolar processes). Synchronous rectification overcomes many of the limitations inherent in the simple boost topology. In addition to the step-up/step-down function, synchronous rectification allows the output to be shorted to ground, and it automatically (and completely) disconnects battery from the load when the IC is placed in shutdown mode.

Boost with linear preregulation

A second boost-plus-linear approach is to preregulate the input to a boost switcher (**Fig 5**). The switching regulator is disabled when the battery is fresh, so an external silicon rec-

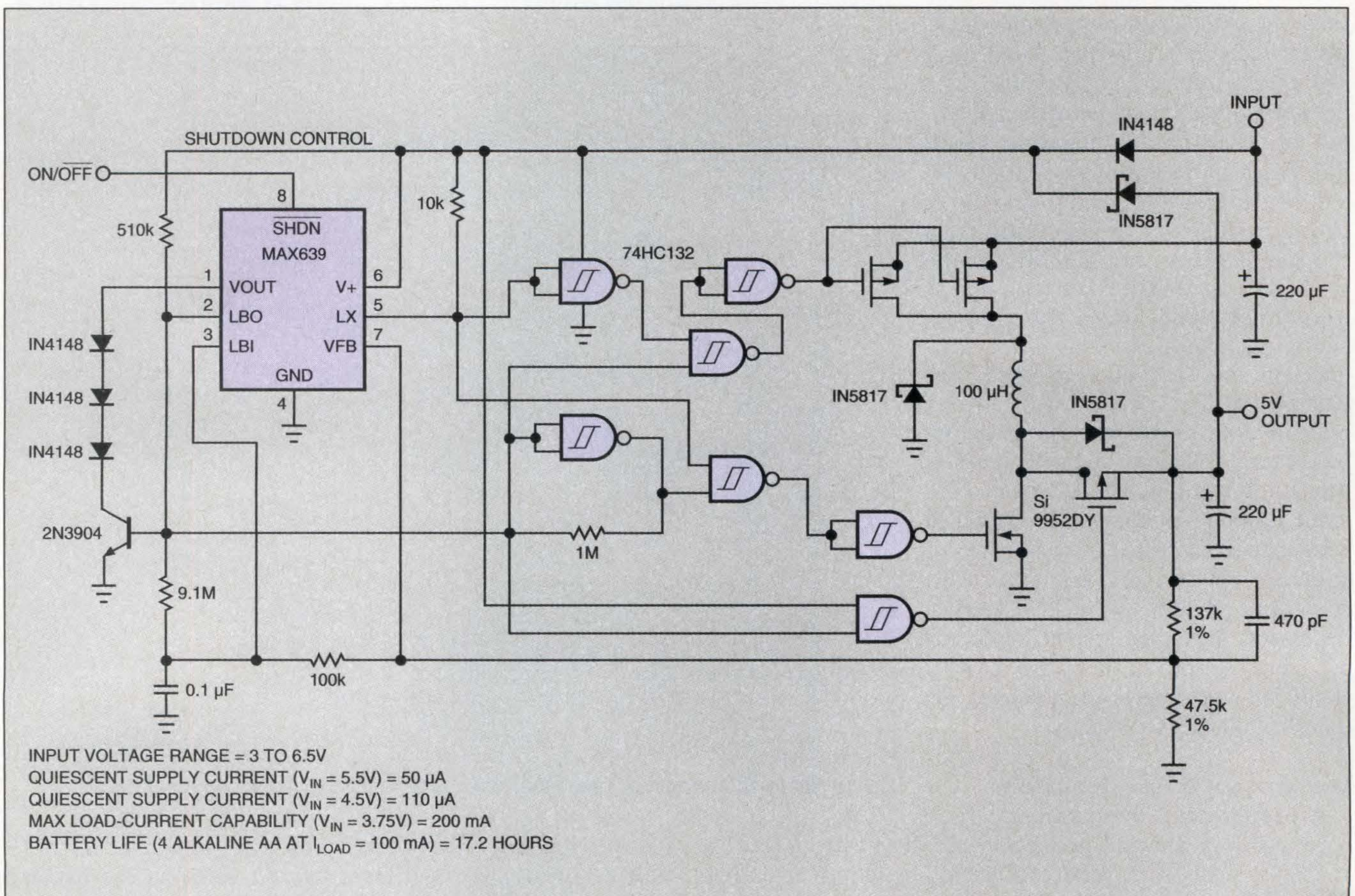


Fig 6—Complexity is the penalty paid for a step-up/step-down regulator that can derive 5V from a battery whose output passes through 5V during its discharge.

STEP-UP/STEP-DOWN CONVERTERS

tifier (D_1) drops the worst-case high input voltage from 6.3 to 5.4V. This cheap-and-dirty equivalent to a linear regulator requires a minimum load of 100 μA or so to prevent output overvoltage due to the diode leakage current. The circuit continues to operate even with battery voltages of 3V and below. Typical efficiency is 80% when the battery is fresh, rising to 90% as the battery voltage declines to 4V.

To accommodate higher input voltages, you can easily substitute a linear regulator for D_1. And if low cost is your goal, omit the p-channel FET switch-over circuit. Performance with the diode alone is still comparable to that of a flyback circuit.

Step-up/step-down topology

The step-up/step-down regulator achieves high performance at the cost of complexity by switching from buck mode to boost mode as the declining battery voltage passes through 5V (**Fig 6**). And it does all this with a single inductor. Switch-mode operation over the entire range of battery voltage yields higher efficiency than does the boost-plus-linear approach, yet the step-up/step-down regulator does not experience the high peak current and consequent I^2R losses of inverting and flyback approaches.

Efficiency exceeds 90% over most of the battery's range, and the step-up/step-down circuit extracts nearly all of the battery's energy. The penalty for this high performance is complexity. The circuit requires three MOSFETs (or four—as shown—if you parallel two p-channel devices for a lower $r_{DS(ON)}$). Also, the switch from buck to boost causes an ~±2% change in the output voltage as the battery voltage reaches 5V.

Built into IC_1 is a comparator that decides when to switch from step-down to step-up operation. The comparator monitors the battery or output voltage, whichever is higher, via a diode-OR connection. As the buck regulator begins to lose control (drop out), the output begins to fall. When the input reaches 4.95V, the circuit switches from buck to boost, causing the output-regulation point to shift from 4.92 to 4.98V. If for some reason the battery voltage rises above 5.15V, the circuit switches back to buck mode. EDN

Reference

1. Moore, Bruce D, "Regulator Topologies Standardize Battery-Powered systems," *EDN*, January 20, 1994, pg 59.

Author's biography

For Bruce Moore's biography, see **Ref 1**.

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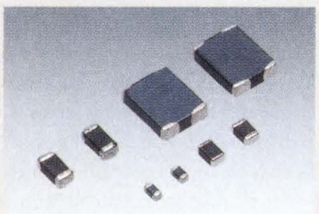

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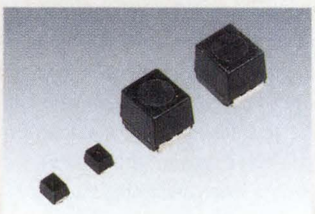

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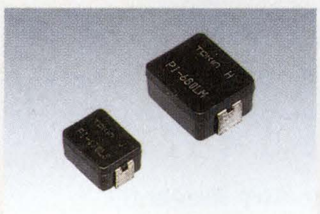

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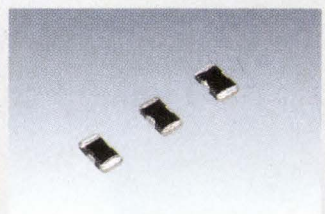

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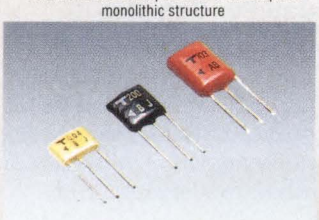

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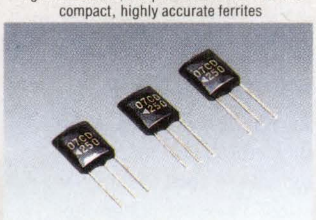

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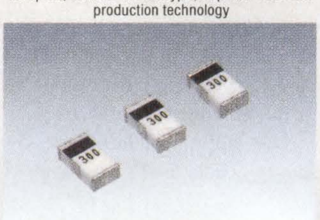

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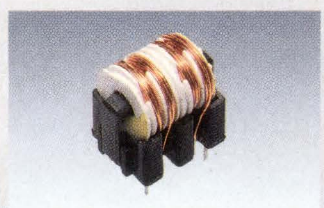

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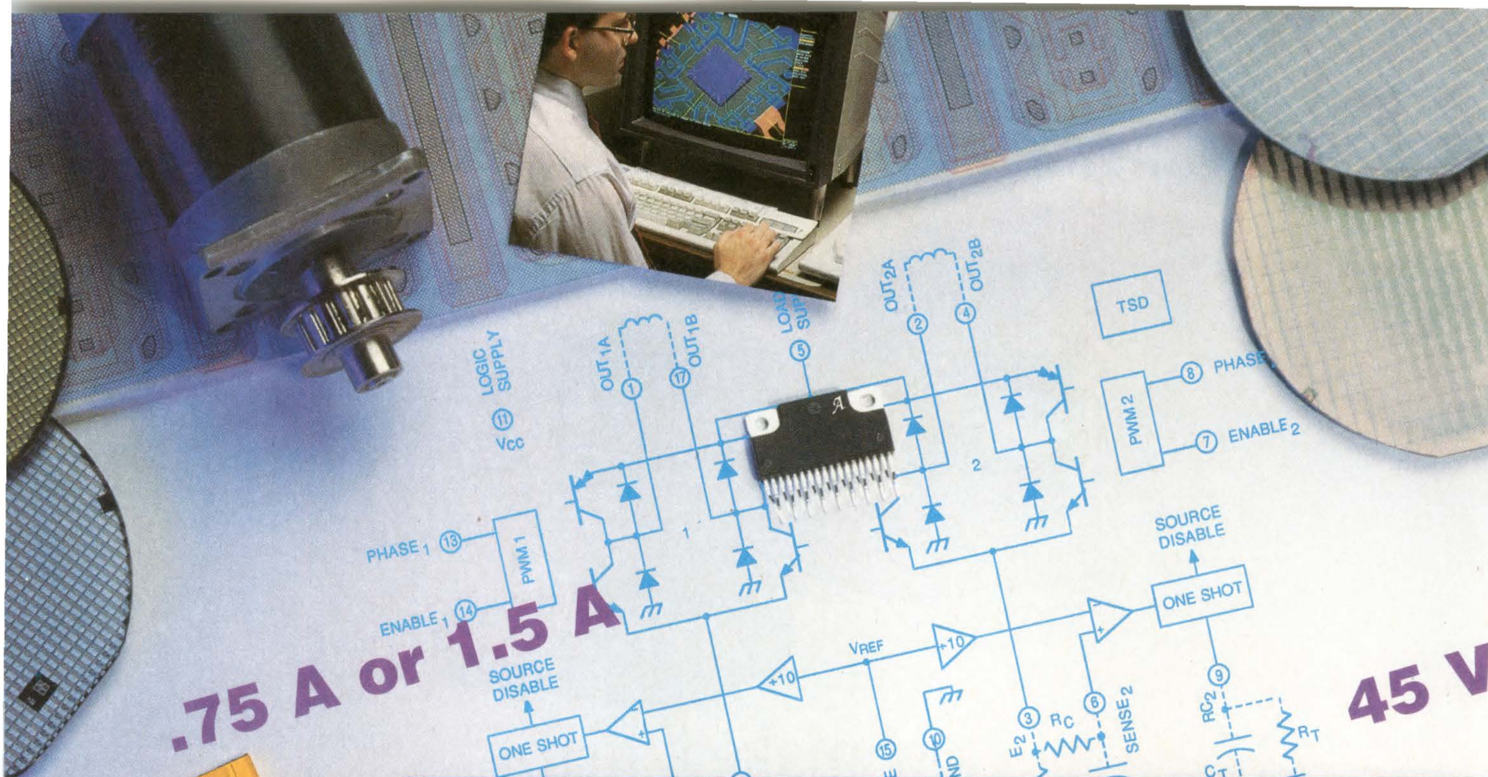

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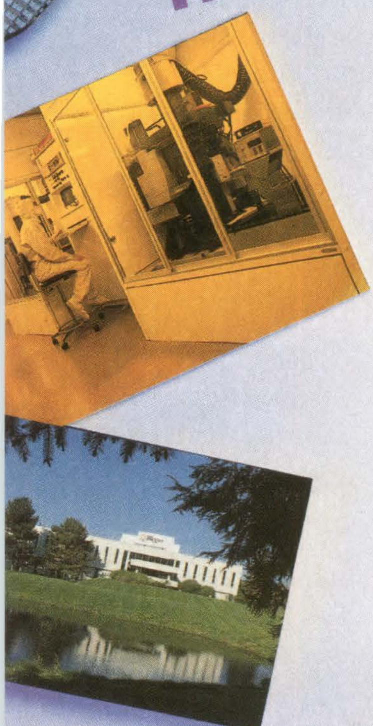

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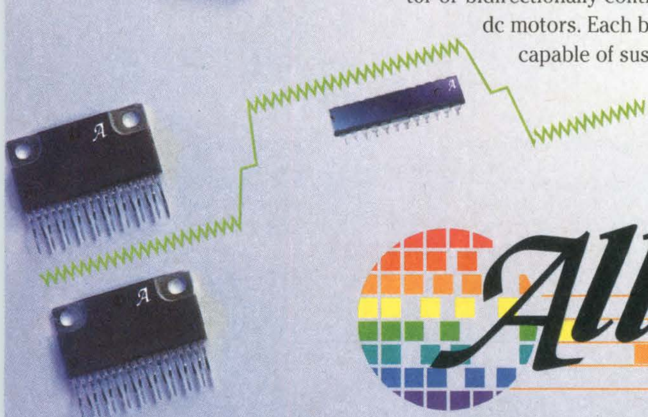

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Pick the right package for your next ASIC design

David P Pivin, ASIC Division, Motorola Semiconductor Products Sector

The quest for higher integration levels in ASICs and competitive pressures to reduce system manufacturing costs has driven IC manufacturers to improve package capabilities and develop new methods. This article should help you evaluate the many choices available to find the best match of design performance and system costs.

Today's system designers have at their disposal the benefit of several generations' worth of ASIC-package development. The variety of packages makes it a challenging task to make a decision that meets price and performance goals. However, armed with a detailed understanding of the various package types, their performance attributes, and their costs, you can choose a package that meets your goals.

This article focuses on packages for applications ranging from high-end consumer to workstation/servers and computers. It discusses various technologies, most of which ASIC designers can use today. It also discusses cost—typically the deciding factor in selecting among the package choices. However, this article goes beyond the cost of the package itself. It also discusses those incurred in manufacturing and during the life cycle of a product, as well as how to reduce costs in an existing product. For example, you may be able to achieve higher performance for the same or lower parts costs, although doing so may require different manufacturing techniques from those you currently use.

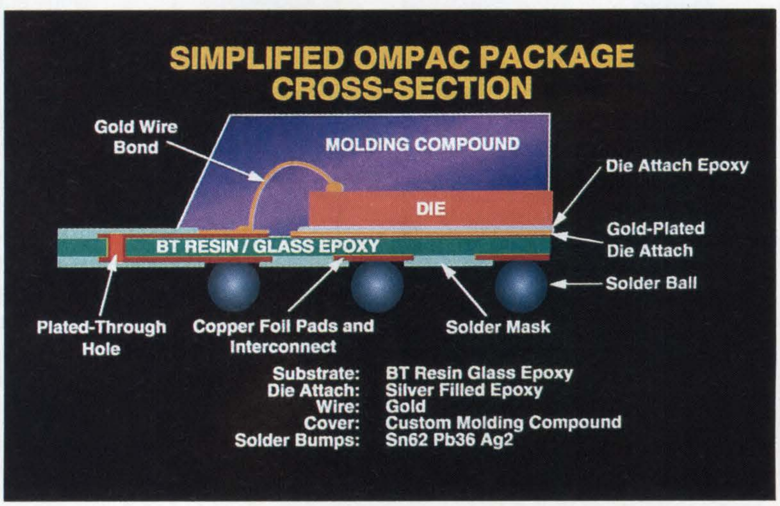
This article compares each package in a matrix of parameters detailing their cost, thermal and electrical performance, physical dimensions, and ease of manufacturing (see **Table 1** and **Fig 1**).

One of the deciding factors in choosing a package is pin count, which has accelerated from an average of 100 pins a few years ago to an average of 160 pins today. Just as the plastic leaded chip carrier (PLCC) extended the range of pins beyond the capabilities of a DIP, the quad flatpack (QFP) has provided a solution PLCCs cannot reach.

Key in driving the demand for higher pin counts is the rapid increase in μP bus widths from 8 to 16 to 32 bits. Most current designs are 32 bits wide, with some pushing out to 64 bits. Multiplexed buses have also given way to separate address and data paths from the processor in RISC architectures. As some designs move into new generations or are cost reduced, integrating several designs into one or two chips, the pin count of individual ASICs rises.

Power dissipation is bound to rise with the increase in pins, which also strains the capabilities of low-cost packages. The power dissipation of CMOS devices is directly proportional to system clock frequencies, which range from 20 to 66 MHz. Most power dissipation occurs during the transitions of signals from high to low or low to high. Signal transitions charge and discharge the load capacitance on each I/O pin. Internal signals, although lightly loaded, are numerous. In contrast, there are only a few I/O buffers, but because they deal with much larger loads, they can consume more power than do the core cells.

Although pin counts increase with architectural improvements, the ratio between gates and I/O buffers has changed little. In the past few years, average gate count has risen from 25,000 to more than 40,000 gates. Unless there is an improvement in power dissipation per gate or I/O buffer, the combination of higher clock frequencies with bus-width-dri-



The plastic ball-grid array provides the density of a pin-grid array at the cost of a plastic quad flatpack.

ASIC PACKAGES

ven density produces a severe demand on the thermal-dissipation capabilities of a package.

To offset the effects of increased clock frequency, some designers use 3.3 instead of 5V power in components, thus alleviating some of the pressure to move to higher cost packages. **Fig 2** shows the power dissipation resulting from changing a design to run from 3.3 instead of 5V as a function of clock frequency. You can implement this hypothetical design in a technology that lets you select among power-rail configurations. By selecting the I/O buffers, the core, or both sections of the ASIC to operate from a 3V supply, you can switch from a 15°C/W package to a much less expensive 45°C/W package.

However, the 3V option may not suit your application. To complicate matters, some enclosures have little or no airflow. Most PCs have access to some airflow because they incorporate fans that draw air out of the power supply. Strategically placed louvers in the power supply and outer case draw air into the case. This cooling method may lead to islands of dissipation on large mother boards that lie flat at the bottom of the case, with no directed airflow: a worst-case scenario.

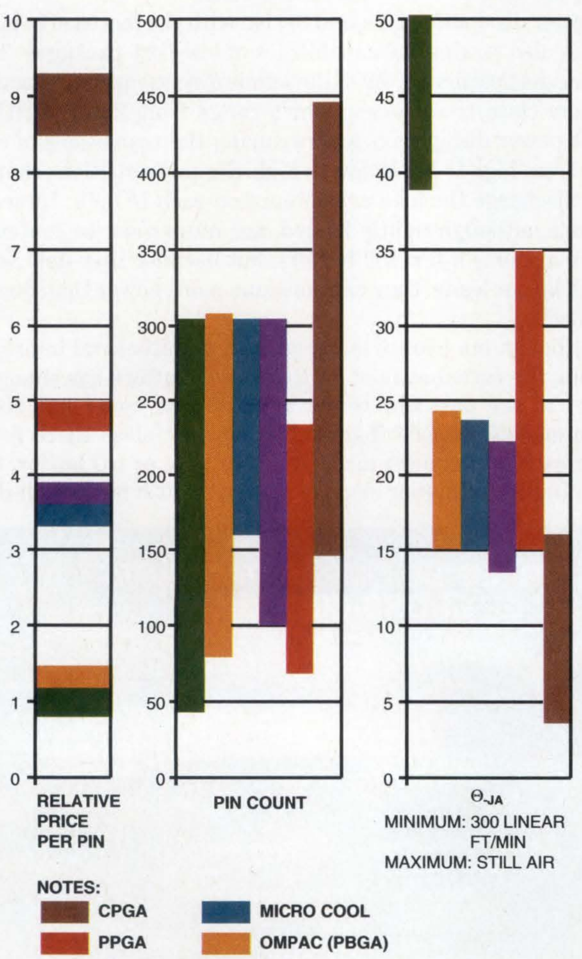


Fig 1—Compare price per pin, pin count, and thermal performance of some common packages.

Smaller footprints affect package choices

Another problem in selecting a package is physical constraints. Smaller footprints for systems such as disk drives and laptops, along with the PCMCIA form factor, have caused these constraints. These new lows in size also apply to package height; the PCMCIA form factor requires total component height lower than 2 mm when components are placed on both sides of a circuit board.

The number of power pins a design requires also affects a design's physical format. Most ASIC designs have a large number of power pins: 20 to 33% of total pins are power pins. The designs require so many pins because the I/O buffers require transient currents, which should go through as low a resistance and inductance as possible. Extra pins also ensure that noisy return paths do not share pins with those of sensitive inputs.

The most significant factor in power-pin count is the need to support simultaneously switched-output (SSO) buffers. The spike of current associated with an output buffer in transition aligns with each buffer's input signal because a common clock signal switches the input signal, an unavoidable byproduct of synchronous operation. On-chip power rails may droop, ground pads may bounce, and the resulting false signals may disrupt chip or system operation.

The clock and data-signal frequencies of most current systems do not reach the levels at which the package RLC values can cause significant degradation of those signals.

Transmission-line effects, especially those of the reflections caused by line-impedance changes, also represent a serious detriment to signal integrity. A design should have a narrow range of values for the impedance of signal lines as they change from die pad on one chip to wire bond, package, pin, board traces, and die pad on another chip. Otherwise, the signal tends to ring the RLC elements like a bell, reflecting many times from each change in impedance. These reflections may defeat any attempts to reduce the cycle time of the system. The simplest method is to insert a series-termination resistor between the memory controllers and the DRAMs. This method damps the reflections enough to preserve signal integrity. You may need to use more dramatic methods when your application requires cycle times shorter than the 70 or 80 nsec that DRAMs provide. However, some methods for reducing impedance mismatches and reflections affect the package.

Another aspect of building high-frequency designs is that they require differential signals. These signals offer a lot of immunity to noise, which is common to both leads, and the ability to more easily control the impedance. Pin density aggravates another transmission-line problem—coupling of signals on adjacent pins of a package or pc board. This increase in coupling is probably the most challenging interconnection problem because solutions typically add cost.

As you can see, high performance challenges the goal of keeping within budget. But for the lowest manufacturing cost, the components and process must suit automated high-

volume assembly. Board manufacturers' slow acceptance of fine-pitch QFP shows that some manufacturers don't readily adapt to new technologies. Those who have tried fine-pitch QFPs find that they cannot use the same processes they used successfully on previous generations of QFPs using standard pitch. New requirements of 4-mil lead coplanarity, ±3 mils, <0.1° placement accuracy, and the last resort—manual hot-bar soldering—are some of the costly new additions to the manufacturing process.

Most designers choose surface mounting as an assembly method because most components used in this method—from passives to many large ICs—are available at competitive costs. The common techniques for assembling and soldering most surface-mounted components have matured quickly. Assembly equipment handles the various shapes and sizes that don't rely on clinched leads to hold themselves on the board during soldering. However, through-hole components require special handling. For example, you can mix different-sized QFPs and lead pitches. Although this technique is not a good idea, you cannot always avoid it.

The cost of a package becomes most evident when it adversely impacts the board-test yield. Board-test failures often relate to interconnection problems, presenting manufacturers with "repair-or-no-repair" decisions. Manufacturers must repair a board that fails a test or face the loss of all invested components and labor.

When a customer returns a defective board, the manufacturer must again decide whether to repair the board or throw it away. Logistic costs add to the penalty of a

Text continued on pg 104

Table 1—Comparison of package parameters

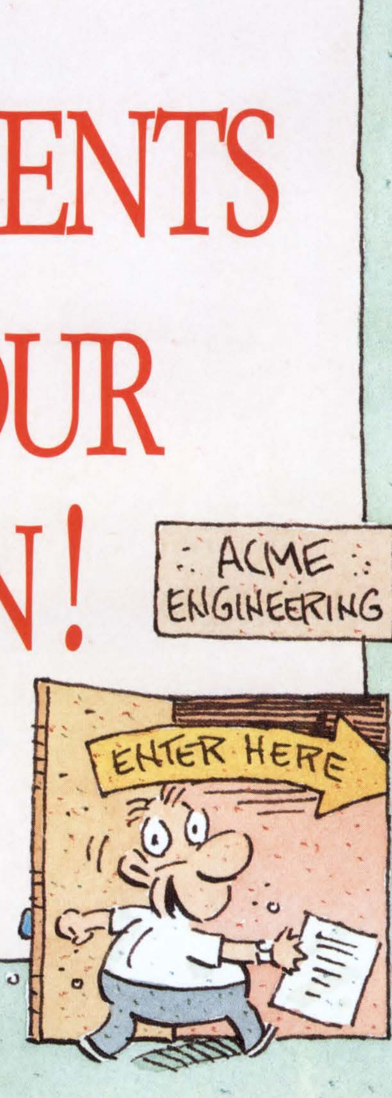
	CPGA	CPGA-w/ planes & slug	PPGA	SMPGA	QFP	CQFP (side braze)	MQFP	Micro-Cool	VQFP	TQFP	TAB	PBGA	CBGA	C-4	COB
Range of # of Pins in common use	72-250+	200-500+	72-300+	200-500+	64-160	64-304	64-304	160-304	64-304	80-120	150-500+	86-313	144-256	150-700+	8-200+
Die Mounting Surface	Gold/ Ceramic	Gold/Cu Slug	Gold/Cu Flag	Gold/ Ceramic	Alloy-42 Lead Frame	Gold/ Ceramic	Cu Lead Frame	Gold/Cu Flag	Cu Lead Frame	Cu Lead Frame	Cu Lead Frame	Gold/Cu Flag	Gold/ Ceramic	Gold/Cu	Gold/Cu
Case/Substrate Material	Ceramic	Ceramic	FR-4	Ceramic	n/a	Ceramic	Anodized Al	FR-4 PCB	n/a	n/a	Polyimide	BT Epoxy	Ceramic	FR-4 PCB	FR-4 PCB
Cover/lid/encapsulant	Metal	Metal	Epoxy	Metal	Epoxy	Metal	Anodized Al	Epoxy	Epoxy	Epoxy	Epoxy (top only)	Epoxy	Metal	Epoxy Edge Seal	Epoxy Glob
Cost per pin relative to 120 QFP	3	7	2.2	4	0.8 - 1.0	5	3 - 4	3 - 5	1.0 - 1.2	0.7 - 1.0	1.5	1.2 - 1.3	3.5 - 4.5	0.1	0.2 - 0.4
Pin Pitch (mm)	2.54	2.54	2.54	1.27	0.65, 0.8, 1.0	0.5, 0.65, 0.8, 1.0	0.5, 0.65, 0.8, 1.0	0.5, 0.65	0.5	0.5, 0.4	0.25, 0.3, 0.4, 0.5	1.5, 1.65	1.5, 1.65	0.075, 0.1	0.75 - 1.0
Area per pin (sq.-mm/pin)	6 - 10	6 - 10	6 - 10	3 - 8	4 - 8	4 - 8	4 - 8	4 - 8	4.7 - 6	3.7 - 4.5	0.3 - 1	2.9 - 3.9	2.9 - 3.9	0.2 - 0.4	0.5 - 0.8
Mounted height (mm)	3.5	4	4 - 6	5	3.8	3.8	3.8	3.8	3.8	1.5 - 2	1 - 2	1.6 - 1.9	1.6 - 3.0	0.6 - 1.0	0.5 - 1.5
Inductance (nH)	6 - 10	1 - 10	5 - 10	3 - 8	8 - 10	8 - 12	4 - 10	4 - 12	8 - 12	4 - 8	3 - 10	3 - 11	3 - 8	<1	<3
Capacitance (pF)	7 - 10	10	1 - 2	7 - 10	1 - 2	7 - 10	1 - 2	1 - 2	1 - 2	1 - 2	1 - 2	1	5 - 8	<1	<1
SSO performance	3	1	2	1	2	2 - 3	2	2	3	3	3	2	1	1	2
High Frequency performance [a]	4	3	3	1	2	3	2	2	3	3	2	2	2	1	2
Still-air thermal perf. (°C/W)	25 -35	12 - 16	25 - 50	14 - 23	45 - 70	25 -35	16 - 23	16 - 23	38 - 45	38 - 45	30 - 50	23 - 30	20 - 25	15 - 30	15 - 30
300 LFM thermal perf. (°C/W)	15 - 24	4 - 9	20 - 40	12 -15	38 - 48	18 - 24	13 - 18	15 - 18	28 - 38	28 - 38	20 - 35	15 - 18	12 - 18	10 - 18	10 - 18
Conductive thermal performance [b]	2	1	3	2	4	3	2	2	4	4	1 - 3	2	1 - 2	1	1 - 2
Manufacturability [c]	1	1	1	4	2	2 - 3	2 - 3	2	2 - 3	4	3 - 4	4	4 - 5	4 - 5	3
Board Testability [d]	1	1	1	3	2	3	3	3	3	3	4	3	3	4	3
Repairability [e]	2	2	2	1	1	1- 2	1- 2	1- 2	1- 2	1- 2	2 - 3	1	1	3	3
Maturity [f]	M	M	M	L	M	S	S	S	S	G	L	N	N	L	S
Use [g]	W,M	W,M	W,I	W	W,C,I,T	M,W	W,T	W,T	C,W	C,W	C,M	C,W,T	M,W,T	W,M	C,W
Production Volume [h]	M	L	M	VL	VH	L	L	L	M	H	L/M	H	L	L	H

a. 1=Superior, highest performance applications, 2=Good, 3=OK, but limited, 4=Not Suitable in average situation
b. 1=<4°C/w, 2=<8°C/w, 3=<16°C/w, 4=<24°C/w, 5=<32°C/w
c. 1=Well understood mature process, 2=Process mature 3=Process widely known, 4=Process in adoption, 5=Process in development
d. 1=Probe and/or Socket testable, 2=Probe testing only, 3=limited probe test on select pins or testpoints, 4=pins/contacts not accessable, testpoint only
e. 1=Easily removed and replaced, 2=Difficult Removal and Replacement, 3=Impractical repairability
f. M=Mature, S=Standard, G=General Adoption, L=Limited, N=New Technology, Lab Environment
g. C=Consumer, W=Workstation/Computer, I=Industrial, M=Military, T=Telecommunications
h. VL=Very Low(Prototyping/Engr. Lab <1K/yr), L=Low(<10K/yr), M=Medium(<100K/yr), H=High(<1M/Yr), VH=Very High(>1)

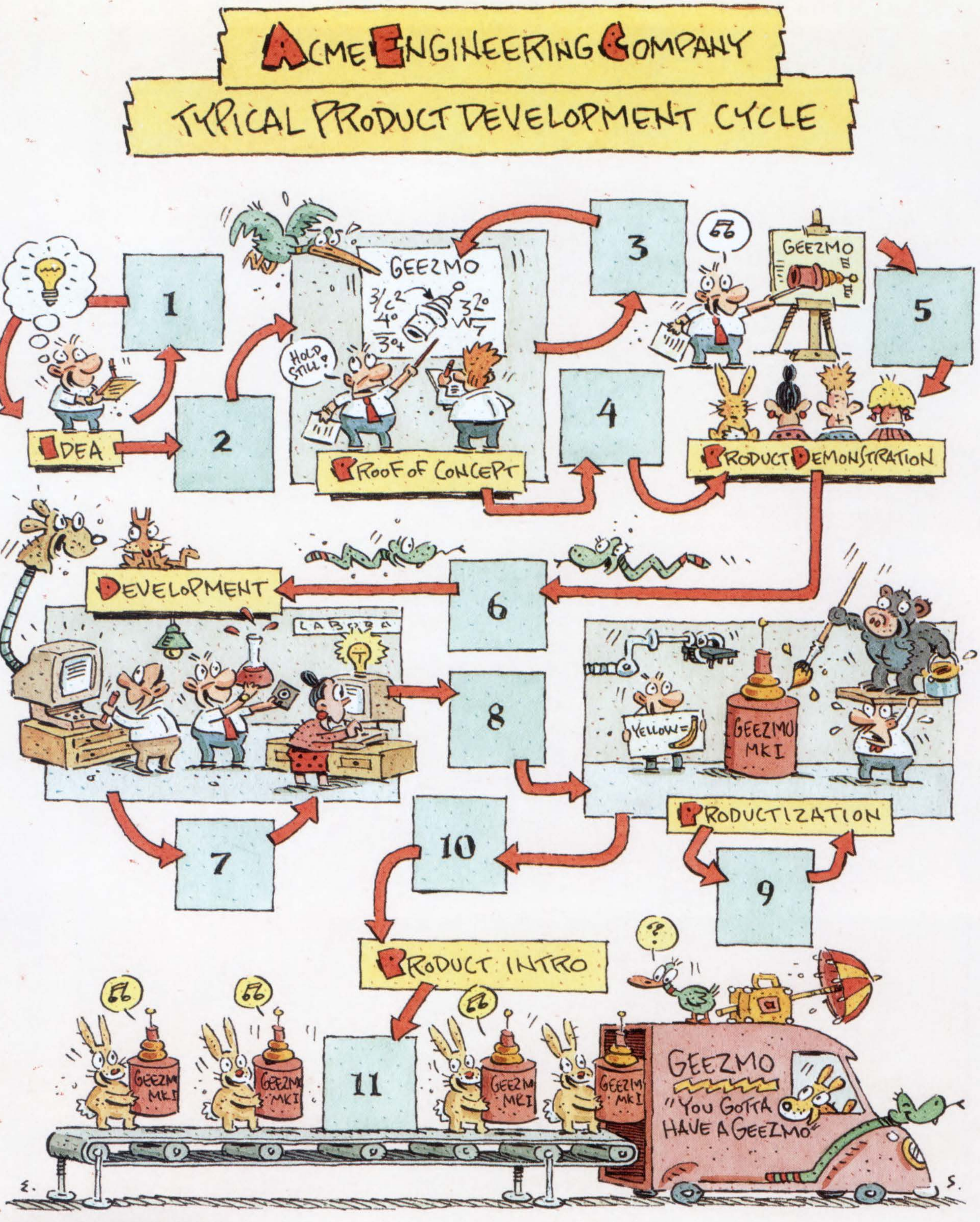
Take the TI/EDN DSP Product Design Challenge!

A Texas Instruments
Color 486 Notebook Computer!
(See Details Inside.)

Join Forces With Texas Instruments To Beat Your Competition!



Play to Win...



OFFICIAL ENTRY BLANK:

Name ______________________ *Title* ______________________

Company ______________________ *Phone* ______________________

Address ______________________

City ______________ *State* ______ *Zip* ________ *Country* ________

For contest rules, see back page of this supplement. Entries must be received by March 31, 1994.
Send entries to: TI/EDN DSP Product Design Challenge, Texas Instruments Incorporated,
P.O. Box 172228, Denver, CO, U.S.A. 80217-9270

☐ Please check if you do not wish to receive future mailings from Texas Instruments as a result of this contest.

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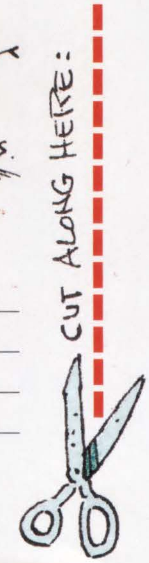


Overwhelmed by DSP product design problems?
Then team up with TI as you

BEAT YOUR COMPETITION

through Total Integration!

READ AHEAD AND PLAY TO WIN!

You're the Chief Design Engineer at Acme Manufacturing Company and you' ve just come up with a really revolutionary idea for a remarkable new DSP-based widget. Studying your design plan, you realize that this isn't a job for novices. You need the extensive DSP product design experience that only Texas Instruments can deliver through its Total Integration program.

To help you blaze the Product Design trail, the TI Design Team has created a Product Development Cycle puzzle. So, join the fun and play along, by cutting out and filling in the missing pieces on the game board on page 2, using clues spread throughout the text. Then send in your design to qualify for the grand prize.

In completing the puzzle, you'll learn how working with TI, you can create a winning product every time!

READY, SET, GO!

To beat your competition to market you need a well marked path that leads you from your idea to the finished product. You realize that you must get some technical advice immediately to get this project rolling. You can call in a **consultant** to help you develop your idea, or you can call the Texas Instruments **hotline** at (713) 274-2320 and speak with an expert in DSP. Or fax your question to (713) 274-2324 in the U.S. or 33 1 30701032 in Europe.

So, beat your competition out of the starting block by making the best choice! Find the game piece that corresponds, and paste the piece at **Position 1** on the game board.

TEST THE IDEA

Talking to the technical advisor was a great help, but you'll have to pick up the pace if you want to stay in front of the competition. As you zip along the path that transforms your general idea into a distinct concept, you know that you don't want to get bogged down learning how to use new evaluation tools. TI's U.S.$99 **DSP Starter Kit (DSK)** is perfect for the first-time evaluator. The DSK is a card that connects to your PC. It comes with its own DSK assembler, debugger, onboard DSP and several example programs.

On the other hand, your design may require more extensive evaluation. In that case, consider using TMS320 **Evaluation Modules (EVMs)** for device evaluation, benchmarking and limited system debugging. An EVM is a half-size PC card that lets you benchmark and evaluate DSP code in real time for less than U.S.$1000.

So you've reached another decision point. Pick the proper piece and stick it on the game board at **Position 2**. Your competition doesn't have a chance if you keep making such smart decisions!

PUZZLE PIECES

If you need technically superior DSP advice, the TMS320 hotline is staffed with TI application experts.

The TMS320 hotline offers applications assistance to answer your questions about development tools, documentation and upgrade options.

To reach one of TI's DSP application experts, simply call (713) 274-2320. (In Asia, contact your local sales office.)

The TMS320 Technical Hotline can also be reached by sending a fax to (713) 274-2324 or 33 1 30701032 in Europe.

Need a helping hand? Get a third party to build a TMS320-based add-in board for your system..

You don't have to tackle this project alone. Third parties offer TI DSP-based products for an array of general and specialized hardware solutions.

TMS320 Evaluation Modules (EVMs) are low-cost development systems that you can use for evaluating devices, benchmarking your design and performing limited system debugging.

For less than U.S.$1000, the EVM lets you single-step through your software to locate breakpoints and debug your code. You can upload and download from your host computer or access trigger data and provide control signals.

PUZZLE PIECES

The TMS320 Bulletin Board Service (BBS) gives you on-line access to the most current DSP technical and application information. All you need is your computer and a modem.

Go on-line with TI to update your computer files with the latest DSP application information and source code or to exchange ideas and solutions with other TMS320 application designers. Just call (713) 274-2323 or 44 2 34223248 in Europe.

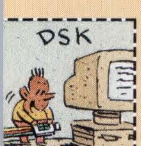
DSP consultants offer design services for the TMS320 family that will cut your development time and speed your product to market.

Independent DSP consultants can provide expertise in specialized design areas such as speech encoding, vector quantization and system analysis.

DSP consultants can make your design an anxiety-free process if they have the expertise your design team lacks.

Don't re-invent the wheel! Cut your development time to the minimum by tapping the design savvy of an independent DSP consultant.

If you are a first-time TMS320 evaluator, the DSP Starter Kit (DSK) is a PC board that includes everything you need to test and benchmark your application. This kit makes it simple to develop code on your PC and download it to the DSK for execution.



This kit comes with its own DSK assembler, debugger and several example programs. You can even build daughter boards that plug into the DSK, because the board routes all device signals to easily accessible headers.

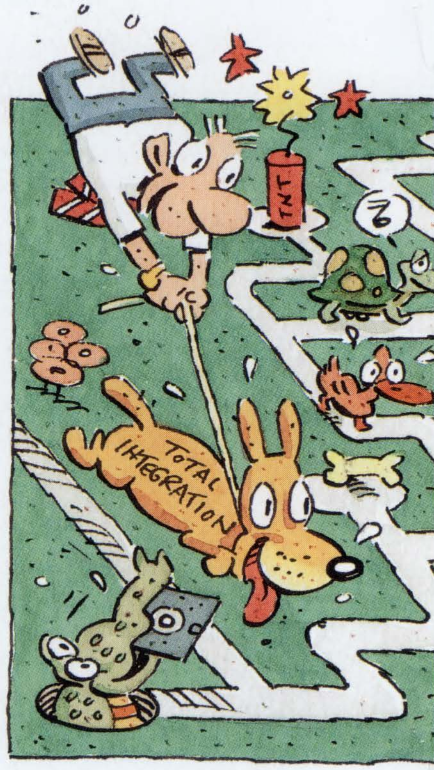
Total Integration™ clears your

PICK A CHIP

As you begin to use the tool you selected, you start to consider the assortment of DSP chips you can use to execute your design. TI offers a family of DSPs that feature more than thirty 16- and 32-bit devices. Based on an advanced Harvard architecture, TMS320 DSPs maximize system performance by executing multiple operations per machine cycle. And internal parallelism supports an instruction set that contains DSP-specific commands. So a single instruction —such as a multiply/accumulate/data move—can cause several operations to execute simultaneously. The competition will never catch you once you've tapped into that kind of computational power.

TI offers five generations of 16-bit fixed-point and 32-bit floating-point DSPs for a wide variety of price/performance points. With volume prices for 16-bit chips starting as low as U.S.$3, you can get an edge on the competition if price is a major marketing factor. Then again, your product can command a solid performance advantage if you opt for the 275 MOPS/50 MFLOPS speed of a floating point processor. On the other hand, a low-power 3-volt fixed-point DSP would be a perfect choice for a battery operated design. Or maybe you want to optimize your design with a customizable DSP (cDSP) from TI, allowing you to integrate a DSP core with other components in a single chip.

Considering the options and benefits, you pick your **DSP fixed-point** or **floating-point engine**. Select the piece that



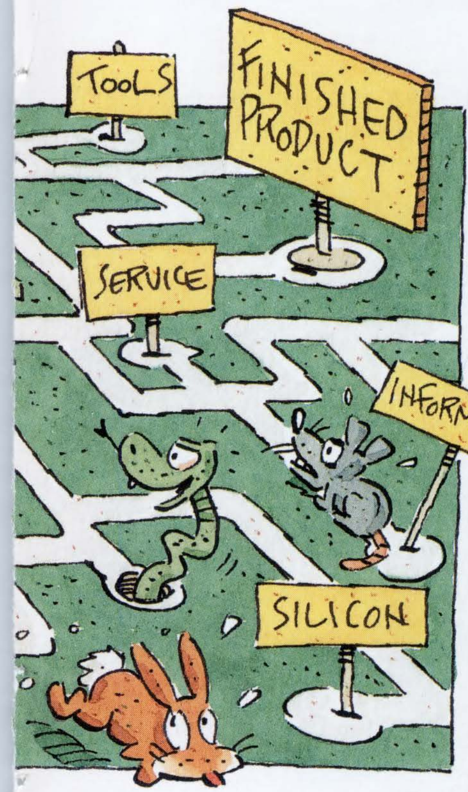
corresponds to this decision, and glue it to the game board at **Position 3**. You smile smugly as you imagine the competition choking on your dust as you blaze a trail to corporate glory!

You leave your office—congratulating yourself along the way—and look up to see your boss down the hall. Running to catch up, you tell her your general idea in order to get some feedback. She thinks you have a great idea, but you need to prove that the concept will work. And she wants to schedule a product demo... immediately.

SO PROVE IT!

Don't panic! Just assemble your technical team. You call a meeting of your best engineers and tell them about your idea. Your excitement is contagious and soon you've accumulated the

way through the design maze



suggestions and observations you needed to make the product demo happen within your boss' timetable. You can practically hear your competitors quaking in their boots.

But, you realize that you may need to schedule some training for your team by the experts at TI. You can call (800) 336-5236, x3904 (or fax 49 81 61804010 in Europe) to find out when the next hands-on DSP training workshop will be held. Or perhaps you should call in a **consultant**. After all, more than 100 third-party vendors and DSP consultants offer expertise in areas ranging from speech encoding to vector quantization to system analysis.

Then again, TI's **bulletin board (BBS)** can provide some down-loadable software algorithms to get your team moving in the right direction. You can call (713) 274-2323 (or call +44 2 34223248 in Europe) to access the BBS and download application information and source code for the project. Maybe you can exchange information with other BBS users about the host of third-party products that are available for TI's DSP family.

And you may have to get some advice to figure out which user's guides and textbooks will let your people validate the concept in the shortest period of time.

Don't get lost in a forest of information.

If you need them, the experts at TI can help you narrow your options. Weigh the benefits of each service and make your decision by pasting the proper piece onto the game board just after the proof of concept at **Position 4.** You begin to consider how nice the title Vice President will look on your business cards.

But just as you place the game piece on the board, your telephone rings. It's your boss, but she's not offering you a promotion. She suspects that the company's arch rival is working on a similar design concept. To make sure that your product is the first (and the best) on the market, you're going to have to pick up your pace and verify every development step.

The race is on!

PUZZLE PIECES

For as little as U.S.$3 you can plug the power of a fixed-point 16-bit DSP into the heart of your system. Reach maximum speeds with device cycle-times as fast as 25 ns for 40 MIPS operation. Or choose a 3-volt version for battery-powered applications.

If an off-the-shelf DSP doesn't provide the level of integration your application demands, our customizable DSPs let you reduce power consumption, board space and system cost while maximizing performance.

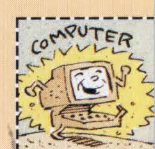
If your design team prefers the ease of programming and code portability offered by a high-level language such as C or Ada, select compilers and programming tools to optimize your code and simplify your software development task.

TI offers a library of software algorithms that cover a wide range of DSP functions, including speech recognition, modems, image coders and audio coders.

TI offers a Custom Manufacturing Service to meet your manufacturing needs when your in-house capability can't meet the volume-production capacity that your hot new product will require.

By eliminating the need for dedicated microprocessors, TMS320 DSPs offer the telecom designer inherent system flexibility, increased channel capacity and lower system costs.

TMS320 floating-point DSPs are designed for multiprocessing at a 320 MBPS interprocessor data-transfer rate. This kind of processing power gives your imaging and graphics-intensive computer applications state-of-the-art throughput.



When cost-sensitivity is a major design constraint, you can turn to the TMS320 fixed-point DSPs to give you the power for speech I/O, digital recording, and sophisticated control functions for as little as U.S.$3.

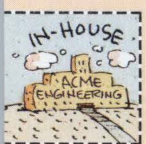
PUZZLE PIECES

When processing power is critical to your application's success, select a 32-bit floating point DSP. Single-chip performance can reach 275 MOPS and 50 MFLOPS, great for applications such as real-time control and multimedia.

With five generations of 16-bit fixed-point and 32-bit floating-point DSPs available, you're sure to find a device that meets the price/performance needs of almost every application.

Want to make sure that your code is as compact and efficient as possible? Turn to the TMS320 macro assembler/linker for hex conversion, error diagnostics, and memory configuration control.

TI offers many design centers worldwide with expertise in DSP system design to keep you a step ahead of the other guys.



If your manufacturing capabilities are sufficient for volume production, remember to get your manufacturing and production people involved in the design process at an early stage to avoid potential problems.

Need to perform numerical or robotic control? How about security access or power-line monitoring? TMS320 DSPs provide the speed for real-time control that meets industrial requirements.

The TMS320 DSPs are available in military versions, and an Ada compiler provides support for designing your military applications.

When you require closed-loop control, turn to the TMS320 family of DSPs. They will provide the processing power you need for power-train management, body and chassis control, antitheft security and vibration reduction.

The other guys never had a chance...

BRING IN THE SUITS

Your team has been working feverishly to come up with a product demonstration for the marketing and production folks. The big day arrives and as you unveil your brainchild, the department heads cheer! Marketing

assures you that this will be the hottest product the company has ever produced—if you can do it while meeting the cost goals they've established. Production observes that the only way to meet that cost is to keep the design as simple and uncluttered as possible.

You may need some help along the way as you fine-tune your product. You can turn to one of TI's many **design centers** for ideas so that you can turn your new baby into a lean, mean DSP machine. Or you can select a **third-party developer** that has a board you can use in your system to save time. Then again, you can always use an **EVM** or **DSK** to keep your DSP development entirely in-house. Well, you have a lot to choose from, so pick your playing piece and place it on the game board at **Position 5**.

As you rise to leave the room, your boss pulls you aside. She hasn't been able to find out the status of the competition's design, but she knows that they're trying to rely solely on in-house expertise. You smile as you consider the world-class team of experts and advisors you've assembled through TI's Total Integration concept. Which expert will you consult with next? The **hotline, BBS,** a **third party developer**, a **consultant**, or a **TI design center?** Make your choice and place the playing piece on the game board at **Position 6**. Nope, the competition doesn't have a chance!

TI SPEAKS YOUR LANGUAGE

You need to decide whether to program your DSP using assembly code or a **high-level language (HLL)** such as C. If you need to keep the coding as compact as possible, the PC-based TMS320 macro assembler/linker converts TMS320 assembly language source code into executable machine code. On the other hand, you may prefer to program in C to maximize code portability. The TMS320 C compilers perform local and global optimizations that improve code efficiency.

You weigh your options, keeping in mind that the competition has to make the same choice. Choose the appropriate game piece and stick it on the design path at **Position 7**.

PICK THE BEST PARTS

Next you need to select the system components. When it comes to ICs, TI can supply your design team with the memory, logic and linear chips it needs to build a working prototype of the product. Then your team can clean up any loose ends by using an **Evaluation Module**, obtaining an XDS510 in-circuit emulator, or getting a **third party development tool**. Pick the game piece that meets your needs and paste it at **Position 8**.

BUILD IT TO GO

It's finally time to fine-tune the prototype into a manufacturable product. Manufacturing and Quality Assurance become more involved at this step to ensure that the items will roll efficiently off the production line. Marketing and Production make sure that the criteria they established at the product demonstration are still valid. Now that the product is a reality, you can decide whether your usage volume will allow you to use a customizable version or a standard DSP.

With ASIC-like ease, you can turn your design into a custom chip and speed your way to market dominance with increased performance. TI's **customizable DSP (cDSP)** capability lets you tuck a board full of components into a single chip. Combine a TMS320 DSP core with RAM and ROM modules, peripherals, analog, and ASIC logic to reduce your board space, power dissipation, system noise, and overall cost while increasing reliability and performance levels.

On the other hand, a **standard DSP** may better suit your needs. Regardless of your choice, you know that TI's products and Total Integration savvy can help you make your design the best it can be to keep you ahead of the competition. Make your decision and stick the game piece at **Position 9**.

ONE MORE CHOICE...

Your final decision is where to manufacture your product. You can build it **in-house** if you have enough production capability. However, TI also offers **custom manufacturing** services that can accommodate your needs. Pick your game piece and complete the product-development path at **Position 10**.

TA-DA!

Now you're ready to introduce your product and show it off to the whole world. So tell us...what kind of product is it?

PRIZES!

WIN A TI/EDN DSP PRODUCT DESIGN T-SHIRT!

Complete the puzzle and mail your entry to get your very own DSP Product Design Challenge shirt. It's stylish, it's comfortable, and it will let everyone know that you're a savvy engineer who knows the benefits of TI's Total Integration.

GRAND PRIZE: TEXAS INSTRUMENTS TRAVELMATE COLOR NOTEBOOK COMPUTER

One lucky DSP product designer will win the ultimate blend of 486 power, portablility, and color. Enter today, because YOU may be the winner of a TI TravelMate 4000E WinDX2/50 Active Matrix Color Notebook computer!

(See contest rules for details.)

Find the game piece that reflects the market your product will address: **automotive, military, consumer electronics, computers, communications**, or **industrial**. Paste that piece in the product box at **Position 11** and prepare to enjoy the fruits of your labor! You succeeded in beating the competition, achieving corporate hero status and creating a wildly successful product because TI's Total Integration capabilities helped you develop your Terrific Idea!

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RULES

TEXAS INSTRUMENTS/EDN DSP PRODUCT DESIGN CHALLENGE

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2. The sweepstakes is open to any individual who satisfies the following criteria: (i) he/she is at least 18 years of age; (ii) is a resident of the United States, its territories and possessions, or of Canada (excluding residents of the province of Quebec), United Kingdom, France, Germany, and those Asia Pacific countries to which EDN Asia is distributed (excluding Malaysia, New Zealand, The Philippines, and Singapore); and (iii) who completes the "TEXAS INSTRUMENTS/EDN DSP Product Design Challenge" puzzle. Employees (and their immediate families and household members) of Reed Elsevier Inc., Texas Instruments Incorporated, its subsidiaries and affiliates, and McCann Erickson are not eligible.

3. To enter, contestants should complete (i.e. puzzle must be completed in its entirety, in addition to name and address portion of form) the official "TEXAS INSTRUMENTS/EDN DSP Product Design Challenge" entry form. Additional entry forms can be obtained by sending a self-addressed, stamped envelope (no stamp required for residents of Vermont, Washington, and France) to EDN, c/o Cahners Publishing Company, 275 Washington Street, Newton, MA 02158-1630. Entries may be handwritten or typed. Entries must be received by Texas Instruments by March 31, 1994.

4. All entries become the property of TEXAS INSTRUMENTS and will not be acknowledged or returned. EDN and TEXAS INSTRUMENTS, their agents and others working for them or on their behalf, will have the right to photograph the grand prize winner, and entry constitutes permission to use of his/her name, picture, likeness and city and state of residence in advertising for no additional compensation.

5. Only one entry per person will be permitted.

6. All contestants who submit a completed (as defined in paragraph 3 above), official "TEXAS INSTRUMENTS/EDN DSP Product Design Challenge" entry form will receive a gift valued at no less than U.S.$4.50. Contestants who submit a completed official entry form will also be eligible to participate in a random drawing to qualify for a grand prize of a Texas Instruments Active Matrix Color Notebook computer (Travel Mate 4000E WinDX2/50, value: U.S.$5,000.00).

7. There will be one random drawing for the grand prize and it will take place under the supervision of Texas Instruments. In order to be eligible for the grand prize in Canada, the qualifier selected by the random drawing must first correctly answer a mathematical skill-testing question to be administered by mail. Participants agree to be bound by these rules and all decisions of the judges, whose decisions on all aspects of this drawing are final. The winner will be notified by mail by May 31, 1994, and may, at EDN's and Texas Instruments sole discretion, be required to execute an affidavit of eligibility and compliance with contest rules and release of liability. Odds of winning will depend on the number of eligible entries received. EDN AND TEXAS INSTRUMENTS MAKE NO WARRANTIES WITH REGARD TO THE PRIZES. Prizes are not transferable. There will be no substitutions for prizes, and prizes are not redeemable for cash value, but Texas Instruments reserves the right to substitute prizes of equal or greater value.

8. EDN and Texas Instruments shall not be responsible for printing errors or for lost, late or misdirected mail. Entries that are printed by machine, mechanically reproduced, mutilated or tampered with, illegible, late or incomplete are not eligible.

9. Grand prize must be claimed by May 31, 1995. Failure to execute and return any requested document within 14 days of receipt, or return of notification or prize as undeliverable may result in forfeiture of prize and an alternate potential winner being selected at the sole discretion of Texas Instruments.

10. Contest rules are governed by U.S. law. The sweepstakes is void where prohibited or restricted by law in the United States and in all foreign countries and is subject to all foreign and United States Federal, State, and Local laws and regulations. All taxes, applicable customs duties, including import/export regulations, and other obligations on grand prize are solely the responsibility of the winners. The grand prize is subject to reporting for tax purposes.

11. To learn name of grand prize winner, send a self-addressed postage-paid envelope by May 31, 1995 to "TI/EDN DSP Product Design Challenge," Cahners Publishing Company, 275 Washington Street, Newton, MA 02158-1630, U.S.A.

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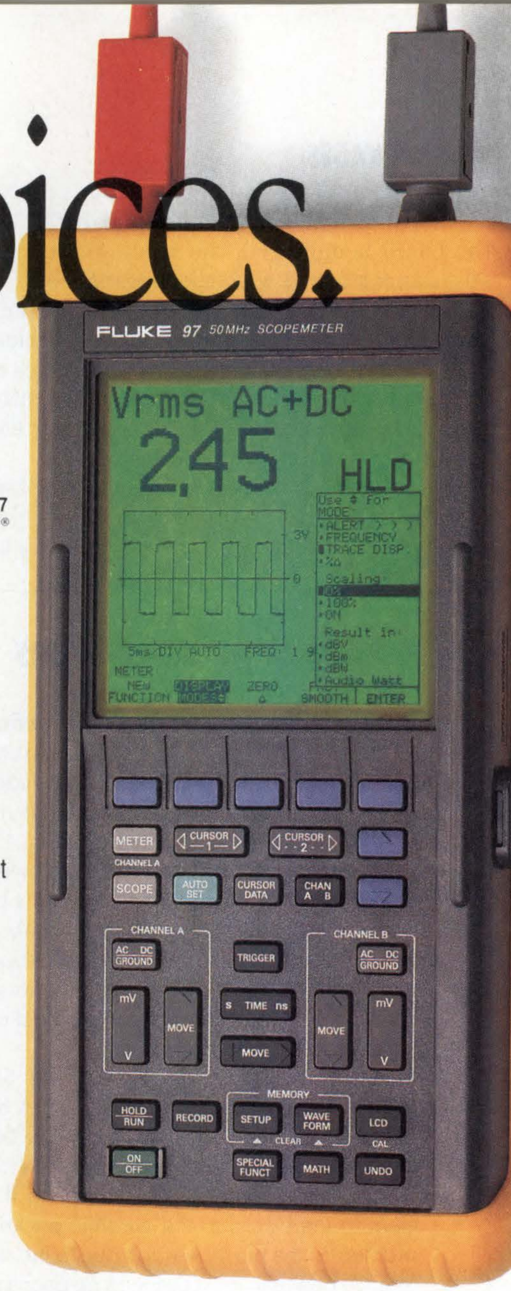

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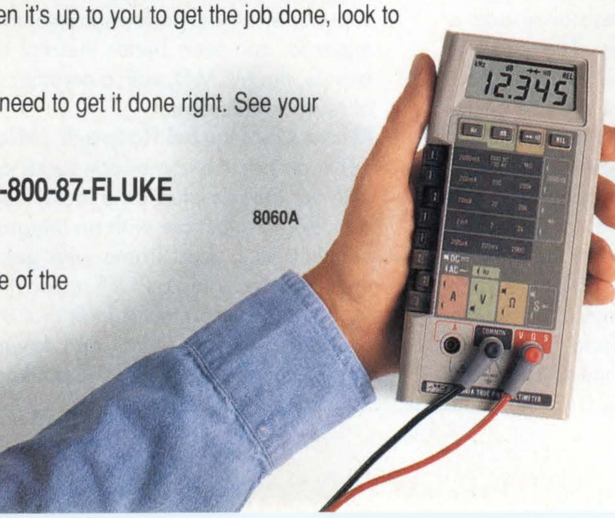

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repair, and, if the component is a difficult to remove and the board is damaged, the accumulated costs can be substantial compared with the original costs of the package.

Electrical performance is just as important as a package's manufacturability. Although most new-package development focuses on density, electrical characteristics remain the most important consideration. The most efficiently designed host board cannot overcome a package's poor electrical characteristics.

Capacitance, particlarly interlead capacitance, couples signals from one lead to another, and, thus, unwanted signals can appear on adjacent pins. The high-frequency content of high-edge-rate signals in high-performance systems couples more readily than that of slower or controlled edge rates. Design techniques that reduce lead-to-lead capacitance are helpful. Using ground planes to reduce capacitance is effective but costly. You can isolate sensitive input signals by grounding adjacent pins.

Capacitance on power leads is desirable because it maintains constant voltage. However, increasing capacitance adds cost. It is most practical to add capacitors only to those applications that are insensitive to cost.

Inductance is typically not a problem on signal leads of low-cost packages at frequencies lower than several hundred

Glossary of package types

- **Controlled-collapse chip connection (C-4)**: Similar to the plastic ball-grid array's (PBGA's) solder-ball method but at a microscopic level, the C-4 includes balls or bumps that attach to the IC, mating to a matching grid of pads on the substrate. A complex process, C-4 requires relatively expensive substrates yet has lower RLC properties than those of any other package. C-4's balls can connect anywhere on an IC requiring a connection, resulting in very efficient power connections and optimum signal isolation and skew management. Although not in widespread use, this approach can also act as a substitute for wire bonding within a package.
- **Ceramic ball-grid array (CBGA)**: Similar to a PBGA but with a ceramic substrate, a CBGA has no pins, so it offers lower cost than that of pin-grid array (PGA). One significant drawback of large CBGAs is the need to reduce shear stress on the balls by matching the thermal coefficient of the board to the ceramic package. This is not a problem in the plastic version due to the relatively small difference between most common pc-board materials and the BT resin/glass substrate of the package.
- **Chip on board (COB)**: This method mounts an IC directly on a pc board, a reasonable approach for extremely low-cost assembly, such as that used in consumer–game applications. An epoxy glob protects chip and wire bonds, which is adequate for this type of application. This technique does not suit high-reliability commercial systems.
- **Ceramic pin-grid array (CPGA)**: This package is popular because it offers low thermal resistance and a well-understood manufacturing process. The process involves attaching gold-plated pins to an alumina substrate in a regular pattern on the bottom surface of the package. Several conductor layers, usually tungsten, connect pins to gold-plated, wire-bond fingers. Aluminum wire bonds connect to the die, which is bonded into a gold-plated depression in the substrate. Cost depends primarily on the size of the substrate area and the number of interconnect layers. The high dielectric constant of the ceramic substrate results in a relatively large capacitance at each pin; inductance varies widely from pin to pin, depending on the routing of the interconnect. You need to select power leads for low inductance. The package's thermal resistance is low, and you can further reduce it by using a heat sink.
- **CPGA with planes**: This method is the same as a CPGA but with additional layers dedicated to multiple power planes. More layers result in higher cost but exceptionally low inductance. The addition of a metal slug for die attachment in a cavity-down configuration further enhances thermal resistance. A top-mounted slug can also directly attach to a heat sink for the lowest possible thermal resistance. This is the most expensive single-chip package in commercial use.
- **Ceramic quad flatpack (CQFP)**: A ceramic cousin to the plastic quad flatpack (PQFP), the CQFP comes in two basic forms: the side-braze-lead version, more closely related to a PGA in construction, and the ceramic-quad version, constructed with a lead frame sandwiched between two ceramic layers. Manufacturers typically use CQFPs for prototyping ASICs; because of its high cost, the package does not enjoy wide use in commercial products. It offers good thermal performance.
- **Multichip module (MCM)**: Designers have adapted conventional form factors, such as QFP and PGA, to handle multiple ICs. MCM-L, a relatively low-cost technique, comprises a pc-board substrate similar to Micro Cool. The technique involves wire bonding the ICs with gold wires and encapsulating them with epoxy like a PQFP. Cost is typically slightly higher than the cost of the sum of the plastic parts; however, the lower space requirements and the superior electrical performance of the MCM-Ls justify their expense. For even better thermal and electrical performance, the MCM-D, with a ceramic substrate, is available at much higher cost.
- **Micro Cool quad flatpack (Micro Cool QFP)**: This package has the same form-factor as that of a PQFP but with the die mounted on a metal slug surrounded by a pc-board substrate with an integral lead frame. The IC connects to a lead frame with gold wire bonds and is encapsulated using a PQFP mold. The package offers better thermal performance than that of a PQFP, very good electrical performance, and lower capacitance and inductance than a PQFP. The package cost is higher than

megahertz, yet it can be devastating on power leads on all packages, even at relatively low frequencies. Switching outputs generate voltage spikes proportional to the rate of change in current. Load capacitance, rather than resistance, presents a heavy load during the initial change of a signal level, and only the drive transistor's low-source impedance limits current. Several outputs switching simultaneously need a current that may cause spikes of several volts at the bond pads of power leads for those drive transistors. The spikes raise the ground or drop the supply level, resulting in signal-level shifts on all pins sharing power and ground leads.

Paralleling several power pins, especially on the ground side, is a reasonably inexpensive method of reducing power-lead inductance. ASIC designers have developed a healthy respect for manufacturers' power and ground rules, which may call for dedicating 20 to 30% of the leads to power and distributing them evenly around a chip that's carefully chosen for minimum inductance.

Another way to address both capacitance and inductance problems is to use power planes. Grouping several wire bonds to a common broad-package bond post and having a few package pins share the group can be effective in lowering inductance. The most effective solution is to place several parallel and contiguous planes close to each other, providing large

that of a PQFP and lower than that of a PGA. The package's construction allows designers to add power planes to larger sizes.

- **Metal quad flatpack (MQFP)**: Similar to the CQFP, the MQFP has anodized aluminum instead of ceramic forming the sandwich. The package offers lower cost than that of a CQFP, very good thermal characteristics, lower lead capacitance than that of a PQFP, and similar inductance to that of a PQFP.
- **Plastic ball-grid array (PBGA)**: This new surface-mounting technique uses a thin pc-board substrate, conventional wire-bond die attachment, and epoxy encapsulation on the top surface. PBGAs look like a PGA without pins; the key difference is that a PBGA substitutes the pins with tiny solder balls that collapse during conventional reflow processing. Pin density compares with that of a PGA, yet cost is more in line with that of QFP. The board assembly yield is dramatically better than that of a QFP, especially a fine-pitch QFP. Motorola offers this technology for ASICs under the name Over Molded Pad Array Carrier (OMPAC).
- **Plastic pin-grid array (PPGA)**: This package is a PGA in which a multilayer pc board replaces the ceramic substrate of the PGA. The IC is wire-bonded with gold leads and encapsulated in epoxy. Some configurations have a metal lid. This offers a much lower cost than, lower lead capacitance than, and comparable inductance to the CPGA. Adding power planes adds cost. The device also comes in a cavity-down, heat-slug version to achieve high power dissipation but also at much higher cost than that of the basic configuration.
- **Quad flatpack (QFP)/plastic QFP (PQFP)**: Ubiquitous in its molded-plastic form, this package offers a low cost per pin for 120 to 208 leads. The EIA JEDEC-metric form factor dominates ASICs in these packages. The package typically dissipates 1W using low airflow. It also offers relatively low lead capacitance; however, because the package uses corner leads, inductance is a problem, especially in larger sizes.
- **Surface-mounted PGA (SMPGA)**: This package is the same as a conventional PGA, except that the leads are very short and are soldered onto pads without a through-hole. It allows much higher pin density for the same area as a PGA; 400 pins fit into 1 square in. The cost of the package is roughly the same as that of a same-area PGA. Solder joints are a concern, although manufacturing is compatible with that of other surface-mount packages.
- **Tape-automated bonding (TAB)**: These packages offer the highest density lead frame and are similar in footprint to that of the QFP. TAB packages are composed of layers of copper and polyamide film. A TAB package's lead frame attaches to an IC via bumps of solder or gold on the pads. The package attaches to a pc board via hot-bar reflow. A thin epoxy coating protects the IC interconnection. TAB's cost is not very high for the pin density, but manufacturing costs are higher than those of any other package type, a significant barrier to use. The die-to-board interface drives TAB's thermal characteristics; compared with a QFP, TAB's capacitance is low, and inductance is comparable. A variation is to mount the IC flipped-over, bringing the TAB leads directly down to the pc board with little or no fan-out. This mounting results in the lowest possible inductance and capacitance of any "packaged" IC but places a further burden on the manufacturing process, making the lead pitch extremely tight.
- **Thin quad flatpack (TQFP)**: These fine-pitch parts offering radically lower height than that of other packages suit applications in portable and handheld products and disk drives with low-height restrictions. TQFPs' body sizes are smaller than those of QFPs, and capacitance and inductance are also lower. However, thermal resistance is significantly higher in TQFPs than in QFPs. Construction is basically the same as that of the QFP.
- **Very fine-pitch PQFP (VQFP)**: This package has a 0.5-mm or less lead pitch and a body size the same as that of a PQFP. The package accommodates up to 304 leads on a 40-mm body. It typically supports 256 I/O signals; power and ground take up the remaining signals. The package proves difficult to assemble when designs are moving up from a PQFP. The package is not significantly different from a PQFP in inductance, capacitance, and thermal resistance at the same body size. Cost is significantly higher than that of a PQFP, especially when including pc-board manufacturing-cost increases.

ASIC PACKAGES

plane-to-plane capacitance and a low-inductance and -resistance path for power. The high cost of this solution may be the only alternative in high-pin-count packages where paralleling of leads has a detrimental effect because of large-package geometry and poor selection of low-inductance leads.

The thermal characteristics are another vital area to consider when selecting a package. The least expensive plastic packages can handle as much as 1W of dissipation without exceeding an acceptable junction temperature. With the rapid increases in density and clock speed, it is increasingly difficult to keep designs below this level.

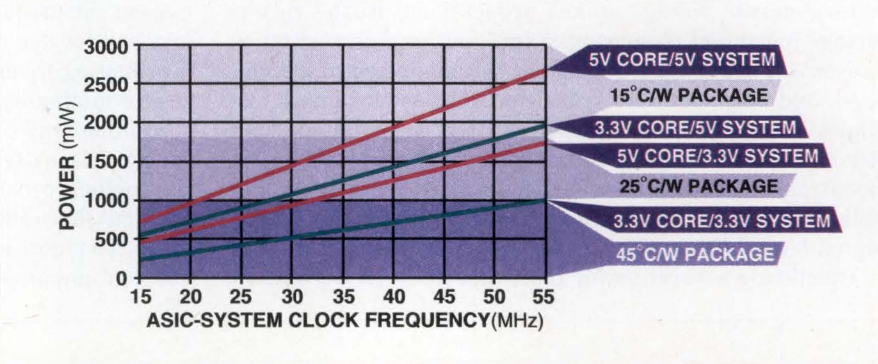

Fig 2—The power dissipation of a 40,000-gate ASIC with 120 signal pins varies with the clock frequency. By using a 3.3 instead of 5V power supply in the core or I/O, you can realize significant power savings, thus letting you use a less expensive package.

A chip's junction temperature changes as the chip flows through a series/parallel combination of thermal resistances between it and its cooler environment. However, there are ways to control these temperature fluctuations. For example, moving air can effectively carry heat from the surface of a package. Increasing the surface area, the velocity, or the density of the air also improves cooling. Unfortunately, the lowest cost systems use natural convection for cooling and must live with the high thermal resistance from the junction to ambient for still air.

Heat sinks are common on bipolar ASIC circuits where dissipation exceeds 5W. Their effectiveness depends on the amount of air that a fan can direct or that convection allows to flow across the heat sink. However, designers of many current CMOS devices have avoided the use of heat sinks, primarily because they offer only 1W or less of power dissipation. However, the high pin count and density of new designs can easily result in 2 to 3W of power dissipation.

You can extend the thermal performance of conventional plastic packages by using a metal heat spreader within the plastic encapsulation. The spreader provides some increase in capability but is not sufficient for many designs requiring dissipation higher than 2W.

From the perspective of the package alone, conduction cooling is more effective than convection for roughly the same price, but it relies on having physical contact with a much more expensive cold plate or other nearby lower temperature surface to encourage heat flow from the package.

Efficient conduction from a package into its surrounding physical structures that have larger surface areas to radiate and convectively transfer heat to the nearby air is quite cost effective but requires a designer to carefully coordinate package selection, board layout, and enclosure design. Inexpensive packages are likely to be the weak link in that chain.

Packages' thermal resistance from junction to ambient ($\Theta_{,A}$JA)—an important reliability concern over the lifetime of a product—ranges from less than 10 to greater than 70°C/W of power dissipated in still air. The PLCC offers 40 to 80°C/W. The common QFP ranges from 40 to 70°C/W. Ceramic pin-grid-array (PGA) packages at 4 to 35°C offer the lowest thermal resistance from $\Theta_{,A}$. Plastic PGAs are 20 to 50°C/W.

Studies show that the more devices and interconnections, the greater the electrical stress and operating voltage, and the higher the junction temperature an IC has, the more likely that IC is to fail. This failure can limit a product's expected life to 3 minutes past the end of the warranty period or two days after Christmas, whichever happens first.

The responsibility of choosing a maximum allowable junction temperature lies with a system's designer. The designer sets a goal for reliability, or the corporate reliability philosophy dictates that goal. The designer then works backward to reach a junction temperature that will provide the necessary reliability. Therefore, asking a supplier: "How much will the package dissipate?" leads to the following series of questions that the designer had to ask when designing the package:

- "What is the ambient temperature and expected airflow?"
- "What is the approximate dissipation of the circuit?"
- "What is the maximum junction temperature?"

A designer must know or estimate the answers to these questions when doing the initial design and the uncertainty of the combination of the values leads to a wide range of possible required $\Theta_{,A}$ as much as 3:1 ratio. In the initial design phase, the designer can still adjust partitioning or package type.

Analytical tools for calculating power can help a designer make an accurate decision only if the designer knows all parameters. Accurate (±10%) determination of an ASIC's dissipation is impossible until the circuit netlist is complete and you have a set of test vectors representing the operating-system stimulus. Without detailed information, only experience can lead to a good correlation between estimates and actual results because a system's switching characteristics are unique to the application's operating conditions.

Consider mechanical characteristics

Last, designers must consider the mechanical features of a package, which, although not as important as electrical and thermal characteristics, are important to the manufacturability and cost of a system.

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SIMPLE PRICE

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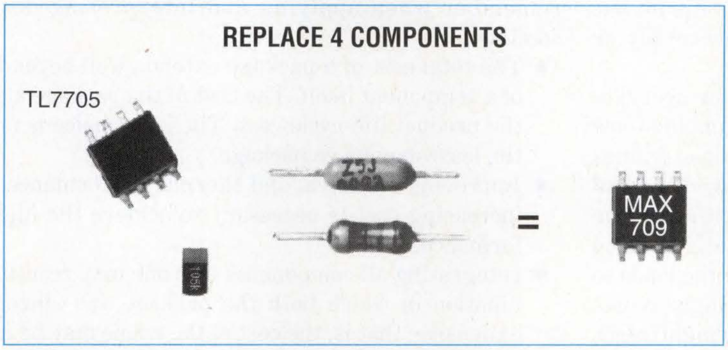

The MAX709 replaces four components, and protects µPs by asserting a continuous reset when the power fails or is turned off.

- **3V, 3.3V, and 5V Versions**
- **Guaranteed $\overline{\text{RESET}}$ Valid to V_{CC} = 1V**
- **Five Reset Thresholds: 4.65V, 4.40V, 3.08V, 2.93V, 2.63V**

MAX709 versus TL7705 Comparison

Feature	MAXIM	TI
External Components Required	0	3
Operating Supply Current: +5V +3V	65µA 35µA	1.8mA 1.8mA
Power Supply Glitch Immunity	Yes	No
+5V Reset Threshold Options	2	1
+3V Reset Threshold Options	3	1
Guaranteed Min Reset Delay	Yes	No

Low-Cost µP Supervisors Replace Several Components

Part	Reset Threshold (V)	Manual Reset	Extra Comparator (Power Fail)	Battery Backup Switchover	Watchdog Timer	Active High Reset
MAX703	4.65	✓	✓	✓		
MAX704	4.40	✓	✓	✓		
MAX705	4.65	✓	✓		✓	
MAX706	4.40/3.08/2.93/2.63	✓	✓		✓	
MAX707	4.65	✓	✓			✓
MAX708	4.40/3.08/2.93/2.63	✓	✓			✓
MAX709	4.65/4.40/3.08/2.93/2.63					
MAX813L	4.65	✓	✓		✓	✓

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CIRCLE NO. 75

ASIC PACKAGES

Today's standard surface-mount packages, such as plastic QFPs (PQFPs), provide significant challenges to the manufacturing process when lead count exceeds 160. Most companies reach a threshold of pain when the manufacturing process becomes difficult. This threshold seems to occur at the 0.5-mm, fine-pitch level. A PQFP's geometry requires either a larger body or a tighter lead pitch to increase pin count. A 160- and a 208-pin QFP have the same footprint but don't necessarily require the same placement accuracy or solder-paste thickness.

Tin-plated Alloy 42 (steel) is a good choice for over-0.5-mm-pitch DIPs, PLCCs, and QFPs where die-stamping tools are practical, but not a good choice for fine-pitch lead frames that are typically tin-plated, etched-copper alloy. To avoid bending these frames, you must handle them with extreme care; otherwise, you may end up with solder bridging or no connection at all. You must maintain the plane of the leads to within ±4 mils to reduce soldering problems. Slight twists in the leads and trimming burrs can cause other nightmares in using these materials.

Package area is becoming more of a problem as designers of surface-mount boards face the double problems of fine pitch and larger body size. Perimeter-leaded packages such as QFPs have reached a practical limit for high-volume reflow soldering with 40-mm body size and 0.5-mm lead pitch for a 304-lead QFP. The high-volume manufacturability constraints of package suppliers and pc-board builders dictates these size and pitch limits.

You can achieve higher pin densities by using an area-based interconnection, such as a PGA, where you can place 500 leads in the same footprint as that of a 28-mm, fine-pitch 208-lead QFP. Unfortunately, this is a relatively expensive solution. Recent developments have modified the concept to surface mounting with short butt-joint leads or solder balls. In addition, manufacturers have dramatically reduced costs by using molded-plastic ball-grid arrays instead of ceramic PGAs.

Laptops, palmtops, and the PCMCIA-card form factor require low height and thus surface mounting. There are a variety of surface-mounting choices—from thin QFPs to tape-automated bonding (TAB) to placing chips on a board. Another solution is the multichip module, which you can fit into many plastic-package form factors.

In packaging, each standard evolved and pin count increased until area or lead pitch became too costly or technically infeasible to support in volume manufacturing. The following chart shows the evolution of packaging. The techniques in the left column led to the advances in the right column:

Discrete transistors	ICs in the DIP package
DIPs	PLCCs, the birth of ASICs; users can pick the package that best fits the application
PLCCs	QFPs, surface mount becomes the mode of assembly techniques
QFPs	VQFPs, fine pitch enables higher densities
QFPs, VQFPs	PBGAs and other area-based connections combine with surface mounting for performance and economy

The exotic technological concepts that do not find acceptance in volume manufacturing may distract designers looking for the best solution. However, designers should support standards because end users are those driving these standards. ASIC suppliers prefer those customer requests that other customers share.

The following list offers some key things for designers to remember when applying and interpreting design constraints:

- The total cost of a package extends well beyond the cost of a component itself. The cost of the package also affects the product life-cycle cost. The best choice is not always the least expensive package.
- Improving electrical and thermal performance and thus increasing cost is necessary to achieve the highest performance.
- Integrating all components into one may result in a combination in which both the package and silicon are too expensive; that is, the cost of the whole may be more than the sum of the costs of the parts.

The following list offers some suggestions to successfully address design problems:

- Logic-design engineers should visit trade shows on surface-mount manufacturing techniques to learn more about assembly and partitioning issues and emerging manufacturing technology.
- Manufacturing and packaging engineers should review designs early in the design cycle and suggest manufacturable alternatives to new problems.
- Designers should plan implementation of manufacturing for new package technologies before or simultaneously with adopting a design.
- Designers should contain costs by using industry-standard, multiple-source packages. EDN

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1. Pivin, David, "High-Performance Mixed-Voltage Interfaces for Mixed 3.3 and 5V Systems," Presentation, Silicon Valley Personal Computer Design Conference, July 22, 1993.
2. "H4C Series Design Reference Guide," Motorola, 1993.

Author's biography

David Pivin is a technical marketing manager for Motorola's ASIC Div, Chandler, AZ. He holds a BSEE from the University of California, Irvine, and an MS in Engineering Management from Northeastern University, Boston. He has been involved in the ASIC field—as a designer, an applications engineer, and a product planner—since 1982. He is a member of IEEE and Mensa.

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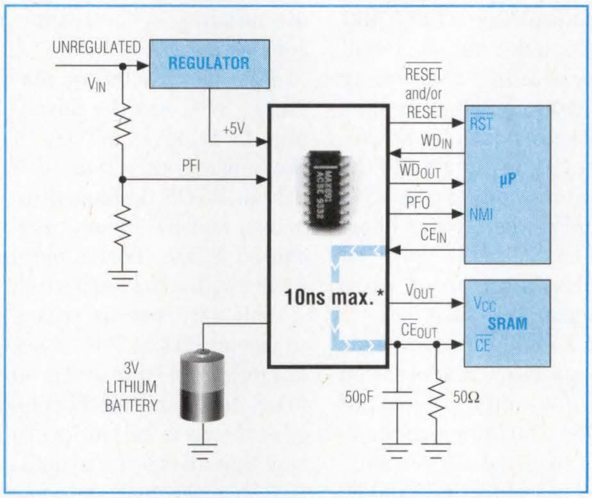

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Part	Reset Threshold (V)	Power-Fail Comparator	Battery-Backup Switch	Watchdog Timer	Active-High Reset	$\overline{CE}$ Protect	Batt-ON Output	Low-Line Output	I_{SUPPLY} (µA, Typ)
MAX691A	4.65	✓	25Ω	✓	✓	✓/10ns	✓	✓	35
MAX693A	4.40	✓	25Ω	✓	✓	✓/10ns	✓	✓	35
MAX690A	4.65	✓	400Ω	✓					200
MAX692A	4.40	✓	400Ω	✓					200
MAX800L	4.65	✓/±2% accuracy	25Ω	✓	✓	✓/10ns	✓	✓	35
MAX800M	4.40	✓/±2% accuracy	25Ω	✓	✓	✓/10ns	✓	✓	35
MAX802L	4.65	✓/±2% accuracy	400Ω	✓					200
MAX802M	4.40	✓/±2% accuracy	400Ω	✓					200

* *Tested with 50Ω driver and 50pF load. Some competitors misrepresent this specification by not stating test conditions.*
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CIRCLE NO. 76

EMBEDDED SYSTEMS, by David Shear, Technical Editor

EDN readers are RTOS aware

Last summer, I asked you if you were "RTOS aware." The reason for the question was that I had been hearing numbers that just didn't make sense. I had been hearing that many software engineers are skeptical about any advantages in using an RTOS (real-time operating system). Further, I was hearing that about 80% of RTOSs being used were developed in-house.

This little survey reveals that, as *EDN* readers, you are not only aware of RTOSs, you often use them.

We received 137 responses to the informal survey based on questions posed in the August 19, 1993, Embedded Systems column. To respond, the reader had only to circle the appropriate number on the reader-service card.

The overwhelming majority, 87%, see the advantage of using an RTOS. Of those using an RTOS, 43% use an RTOS developed in-house, and 57% use a purchased RTOS. This is more in line with what I expected.

Only 13% saw no reason to use an RTOS. This is not surprising. Like with so many tools and methodologies, if your mind works in a way that allows you to naturally use the tools, you use them. If you think differently, the tool just gets in the way. That's probably the case with the 13% of respondents who found other programming techniques to get their jobs done.

But what did surprise me was that when looking at only those who see the advantage in using an RTOS, only 13% have decided against it. I find it difficult to program without using an RTOS, but sometimes I could probably do just as well without one. It was gratifying to learn that 87% of those who understand the advantages of an RTOS actually use one.

I have a strong hunch that the percentage of those using in-house RTOSs will decline as new products based on purchased RTOSs replace those currently in production. You now have many options for RTOSs that didn't exist a few years ago: Virtually all µPs offer a choice of RTOSs.

Here are the results of the survey (total response: 137):

- 18, or 13%, saw no advantage to using an RTOS.
- 16, or 12%, saw the advantage of using an RTOS but decided against it.
- 44, or 32%, used an in-house-developed RTOS.
- 59, or 43% used a purchased RTOS.

DEC embeds its Alpha AXP into products for real-time applications

Beginning next month, Digital Equipment Corp will begin to introduce products for use in embedded systems. The company is basing all the products on the Alpha AXP µP family.

The reason for the move is that DEC is trying to create a full line of products for embedded real-time applications—from just the µP to complete systems. The company is also planning to provide a scalable family of µPs and operating systems (OSs). The company expects this family to span from the simplest embedded application to the largest and most complex multiprocessor-based distributed application.

Because each µP shares the same instruction set, the new products enable you to learn one set of tools and one software architecture for all projects, thus minimizing the time needed for learning architectures and tools. More important, this consistency lets you reuse more code.

The products allow you to choose between two DEC Unix-based OSs—DEC OSF/1 Unix, which has real-time extensions, and DECelx, which is for hard real-time applications. Both OSs comply with Posix 1003.4 Draft 11.

DEC based DEC OSF/1, which is in its third release (version 1.2), on the Open Software Foundation's OSF/1. DEC OSF/1 builds on a modular Mach kernel and includes threads, memory-mapped file support, and advanced virtual memory.

DECelx, an embedded local executive, provides an integrated Unix environment for software development. A host computer running DEC OSF/1 provides editing and compiling services and then downloads the runtime code to the target for execution under DECelx.

The ElxGBD Windows-based debugger runs on the host and the target and allows source-level debugging of the target. It also provides performance-evaluation tools that show timing and processor use.

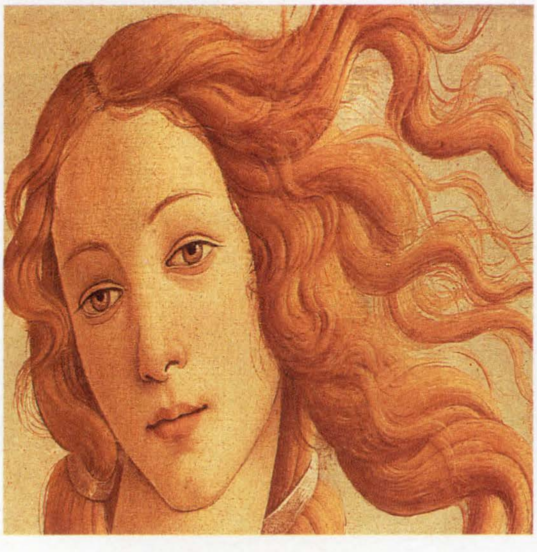
The DECelx multitasking kernel uses preemption and priority-based scheduling for the predictable response required by hard real-time applications. DECelx runs on the Alpha AXP and Motorola 68000 µPs. The DECelx runtime software includes the executive, multitasking support, network facilities, local file systems, I/O, utility libraries, and boot-ROM support.

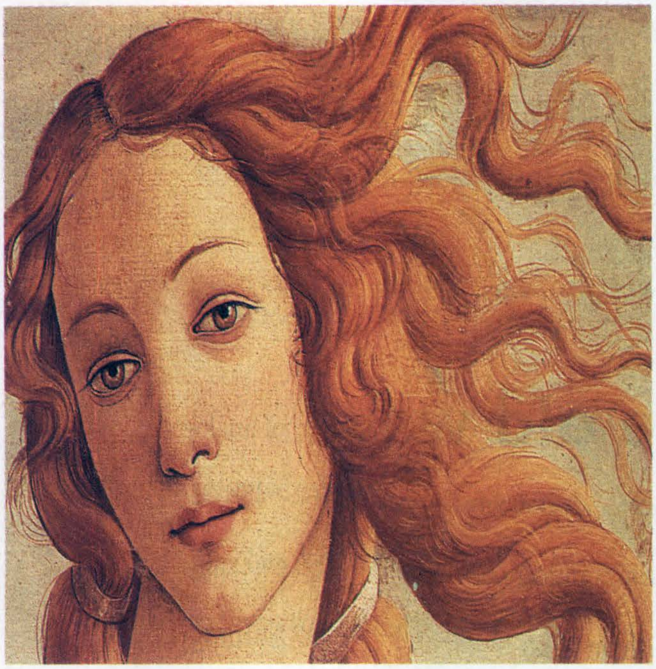
DEC is now focusing on the high end of the market for embedded systems—applications that require a significant amount of computing power and speed. Such applications include distributed process control, robotics, telecommunications, and medical imaging.

DEC is also planning to introduce a family of scalable, distributed OSs that will let you pick the appropriate µP and then get just as much OS as your application needs. The company will also offer VME and evaluation boards in addition to the its currently available VME, PC, and workstation boards. The VME boards will include one based on DEC's 66-MHz 21068 µP and one based on the company's 166-MHz 21066 µP.

—David Shear

Digital Equipment Corp, Marlborough, MA. (800) 344-4825. **Circle No. 328**





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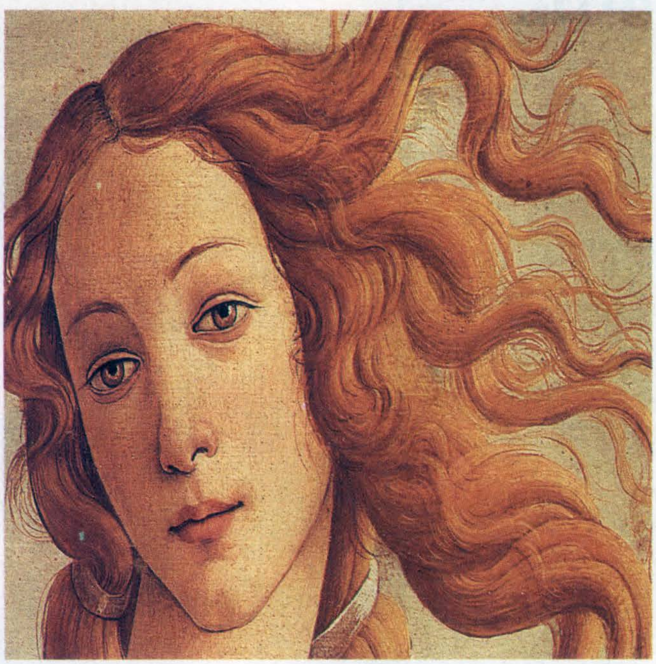

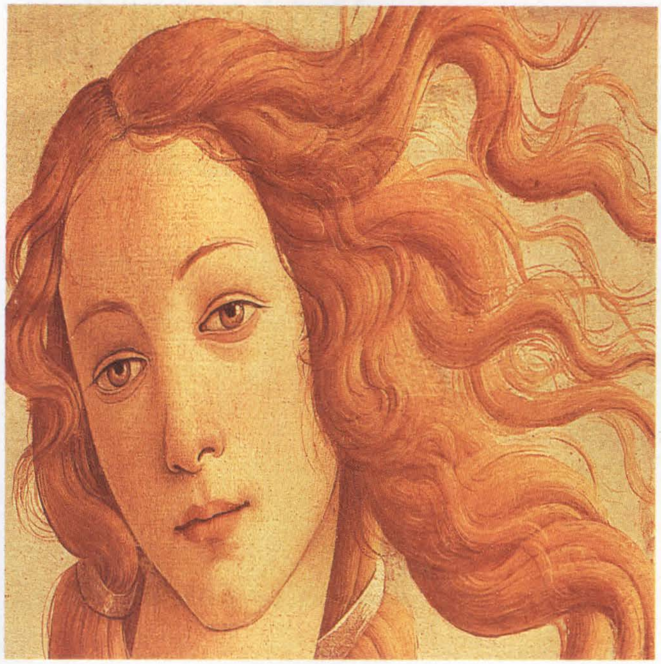

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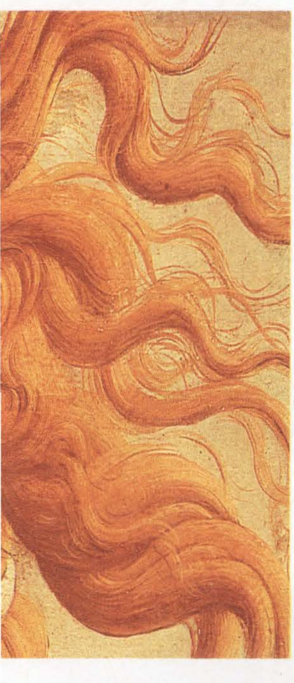

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CIRCLE NO. 96

Cypress FPGA hits 100-MHz counters

Cypress Semiconductor has entered the FPGA fray, melding the QuickLogic FPGA architecture and antifuse technology with its own 0.65-mm FPGA architecture. The Cypress pASIC38x FPGAs combine a proprietary antifuse technology with a single flip-flop/multiple-output core logic element and X-Y-matrix chip routing. Cypress claims FPGA clock rates up to 100 MHz for loadable counters and 85 MHz for chip-to-chip operations.

Built on a 0.65-μm CMOS process, the FPGA architecture relies on an amorphous-silicon antifuse. The antifuse is blown to make a connection and has a resistance of 50V with less than 1-fF capacitance. The relatively fine-grained core-logic cells each have one register and six basic input gates. The FPGA architecture also provides a 23-input fan-in (input signals) and multiple outputs, including two 6-input gates, two multiplexer terms, and a flip-flop true output. The inputs include the clock and dc set and reset for the D flip-flop.

The architecture provides 1000 to 4000 usable gates, and Cypress plans an architecture with larger chips and more gates to follow. Chip I/Os range from 40 to 122 pins. The architecture provides eight high-drive input cells for high-fan-out I/O inputs and two high-drive clock cells for clocking. I/O cells do not have sequential elements. Each I/O is bidirectional and is driven internally by an enabled inverter fed by a 2-input OR gate (one input negated).

The X-Y routing resources cover the chip in a matrix with horizontal and vertical wiring channels. The vertical X channels include 16 segment wires (to local elements) and four express wires (chipwide). The vertical Y channels have four quad (to four elements) and eight segment (local) wires. Each core element has 23 inputs and as many as five outputs. Logic input and output delays are on the order of 4 nsec (signal in to chip, through element, signal off chip). The combinatorial delay through a cell is 1.9 (one load) to 4.8 nsec (eight loads). Flip-flop setup time is 2.2 nsec, with a zero-hold-time requirement. The chips have a JTAG input for scan-chain test of the logic-cell registers.

Cypress supplies a VHDL-based tool set, Warp3, for development. Warp3 supports the pASIC380 family as well as Cypress's PLDs. The kit provides VHDL top-level design and simulation, including device targeting and device-specific timing simulation. The tool set supports both manual and automatic placement, mapping logic onto the FPGA elements. Routing, however, is fully automatic. The 7C381/2/3/4 are available now. The 7C385/6 will be available for sampling in February, and Cypress plans to begin production in March.—**Ray Weiss**

Cypress Semiconductor, San Jose, CA. (408) 943-2600. **Circle No. 330**

QuickLogic Corp, Santa Clara, CA. (408) 987-2000. **Circle No. 331**

Cypress pASIC38x FPGA family

	7C381	7C382	7C383	7C384	7C385	7C386
Usable gates	1000	1000	2000	2000	4000	4000
Logic cells	96	96	192	192	384	384
I/O cells	32	56	56	68	68	114
HD cells	8	8	8	8	8	8
CK cells	2	2	2	2	2	2
Package	44-pin PLCC	68-pin PLCC	68-pin PLCC	84-pin PLCC	84-pin PLCC	144-pin PLCC

Gate arrays mesh sea of gates with sea of I/O

ASIC design is fast approaching the complexity of system design. A single ASIC can now support designs that used to take one or more boards. The gate arrays to handle these complexity levels have expanded I/O and pin counts, as well as providing larger, more efficient "canned logic," or megacells, which supply large logic functions. SGS-Thomson's new ISB35000 gate-array family delivers more than 1 million usable gates and as many as 648 I/Os capable of handling clock rates over 200 MHz.

Based on a new 0.5-μm, 3-layer metal process, the HCMOS5 crams approximately 5500 equivalent gates into 1 mm square. Designed for 3.3V operation, the SGS array family has a typical gate speed of 210 psec (2-input NAND, two loads). Power dissipation averages 0.76 mW/MHz, reduced from 5 mW/MHz for the company's earlier 0.7-mm ISB2800 series. The new HCMOS5 process uses stacked tungsten alloy plugs for interconnections between metal layers; these plugs allow vias between different layers to be stacked atop one another and reduce gate-wiring area by up to 20%.

Structured as a sea of gates, the array builds on a new smaller cell, composed of four N and four P transistors. These cells have a 1 to 2V source-drain resistance that eliminates the need for first-level metal power buses. Additionally, the cells can be paired for higher drive and switching speeds. I/O cells surround the core sea of gates. Using a sea of transistors, you can adjust and program these I/O cell pads. Thus, you can configure the I/O cells for different pad-drive capabilities and pad sizes. These cells support 800 to 1000 pins and handle 3.3 and 5V interfaces. Cell I/Os can sink up to 24 mA and source a drive up to 12 mA. Ball-grid-array, flip-chip packaging is available for high-density arrays. Other packages include grid quad flatpack, plastic quad flatpack, and pin-grid array.

SGS-Thomson furnishes a large

INTEGRATED CIRCUITS

logic-cell and megacell library. Library elements include 196 SSI/MSI logic functions, 150-MHz-GTL, 250-MHz-PECL transmitter/receiver I/O, fast single- and dual-ported SRAMs, up to 64-kbyte DRAMs, up to 512-kbyte ROMs, USARTs, and a 10-nsec 64364-bit multiplier. Other megacells include a 16-bit DSP core, PLLs, 200-MHz RAMDACs, serial transputer links, and a 16-bit T425 transputer. For testing, SGS-Thomson offers a scan-test macro library that complies with JTAG 1149.1.

The ISB35000 arrays integrate standard CAE tool sets; they include a Verilog-XL HDL, Synopsys and Cadence VHDLs, the Synopsys design and test compiler, the Cadence Opus back-end tools, and the full Mentor 8.2 tool set.

—Ray Weiss

SGS-Thomson Microelectronics, Lincoln, MA. (617) 259-0300. **Circle No. 332**

SGS-Thomson ISB35000 gate-array family

Device	ISB35030	ISB35083	ISB35166	ISB35279	ISB35389	ISB35484	ISB3532
Gross gates	32,000	82,944	166,454	278,784	389,376	484,416	891,744
Usable gates	25,000	58,060	116,524	195,148	253,094	314,870	499,046
Maximum I/O cells	96	172	244	316	372	416	544

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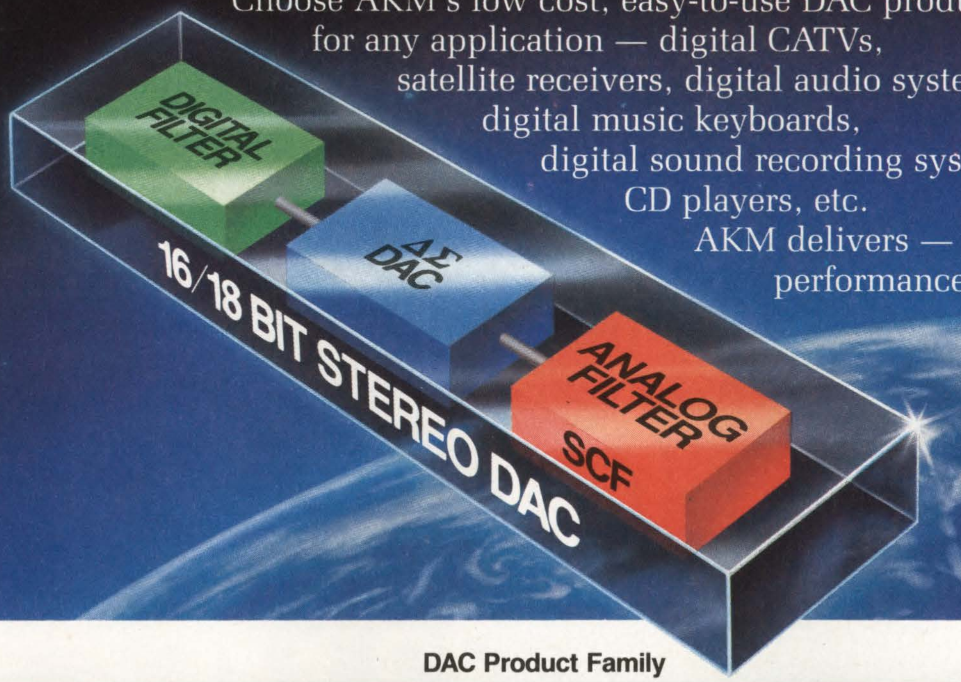

DAC Product Family

Device	# of bits	DR	S/N	THD+N	Special Features	Voltage
AK4316	16	90dB	90dB	0.01%	• High tolerance to clock jitter	+5V
AK4318	18	97dB	97dB	0.0025%	• High tolerance to clock jitter • De-emphasis control circuit • Soft mute function	+5V
AK4313	18	93dB	93dB	0.004%	• High tolerance to clock jitter • De-emphasis control circuit • Soft mute function • Low voltage	2.7~4.0V

AKM **Asahi Kasei Microsystems Co.,Ltd.**

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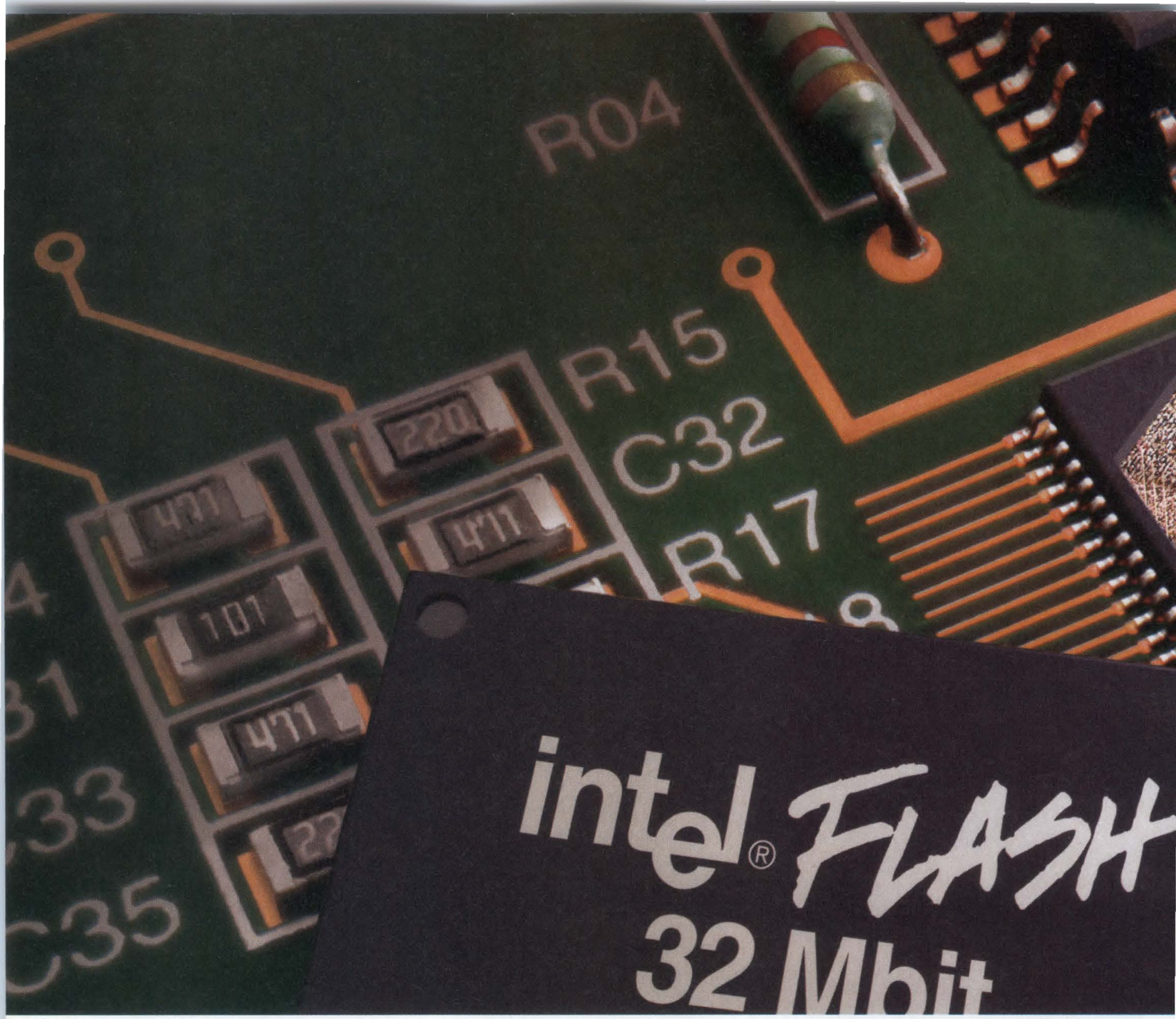
CIRCLE NO. 78



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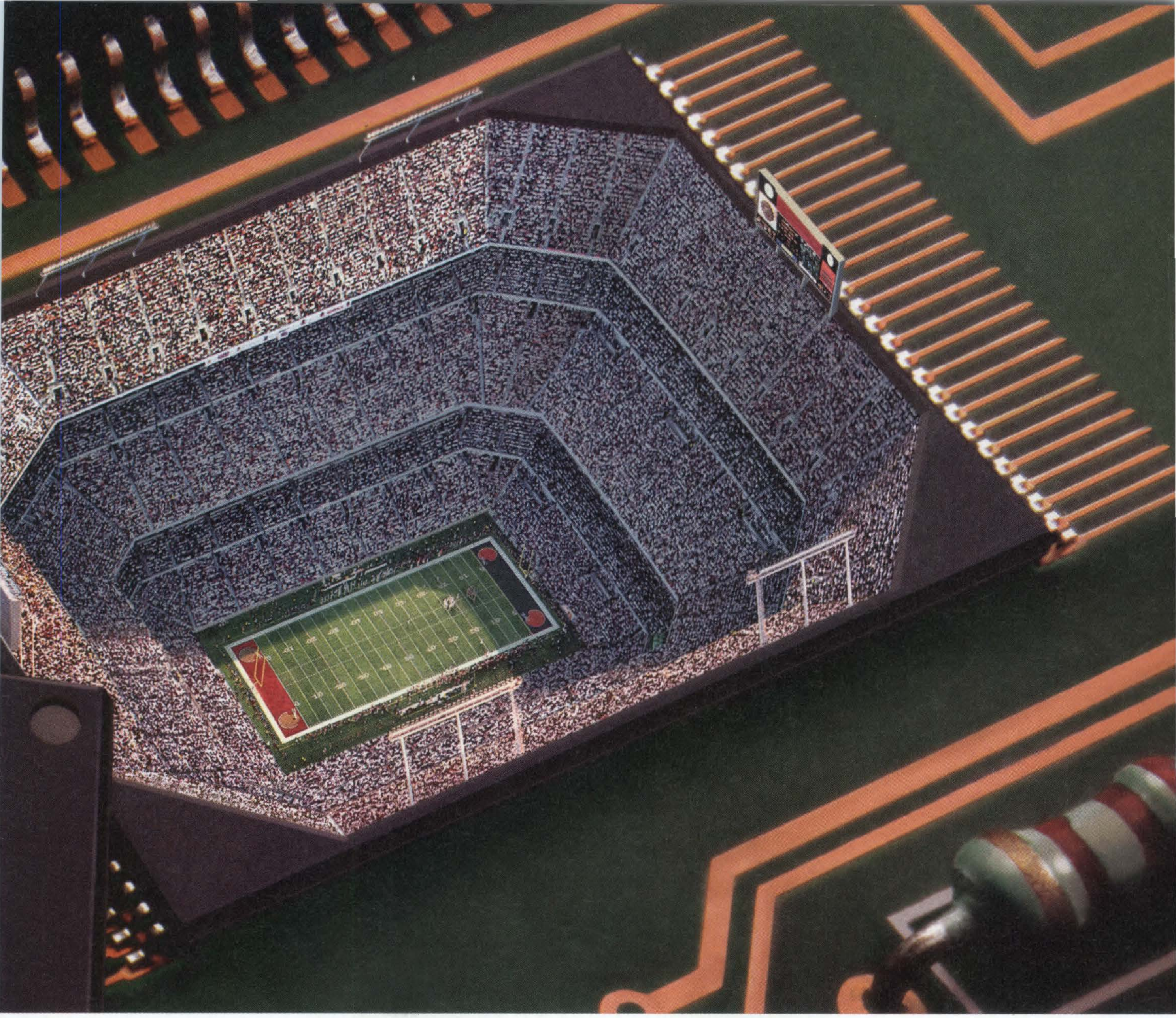

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CIRCLE NO. 43

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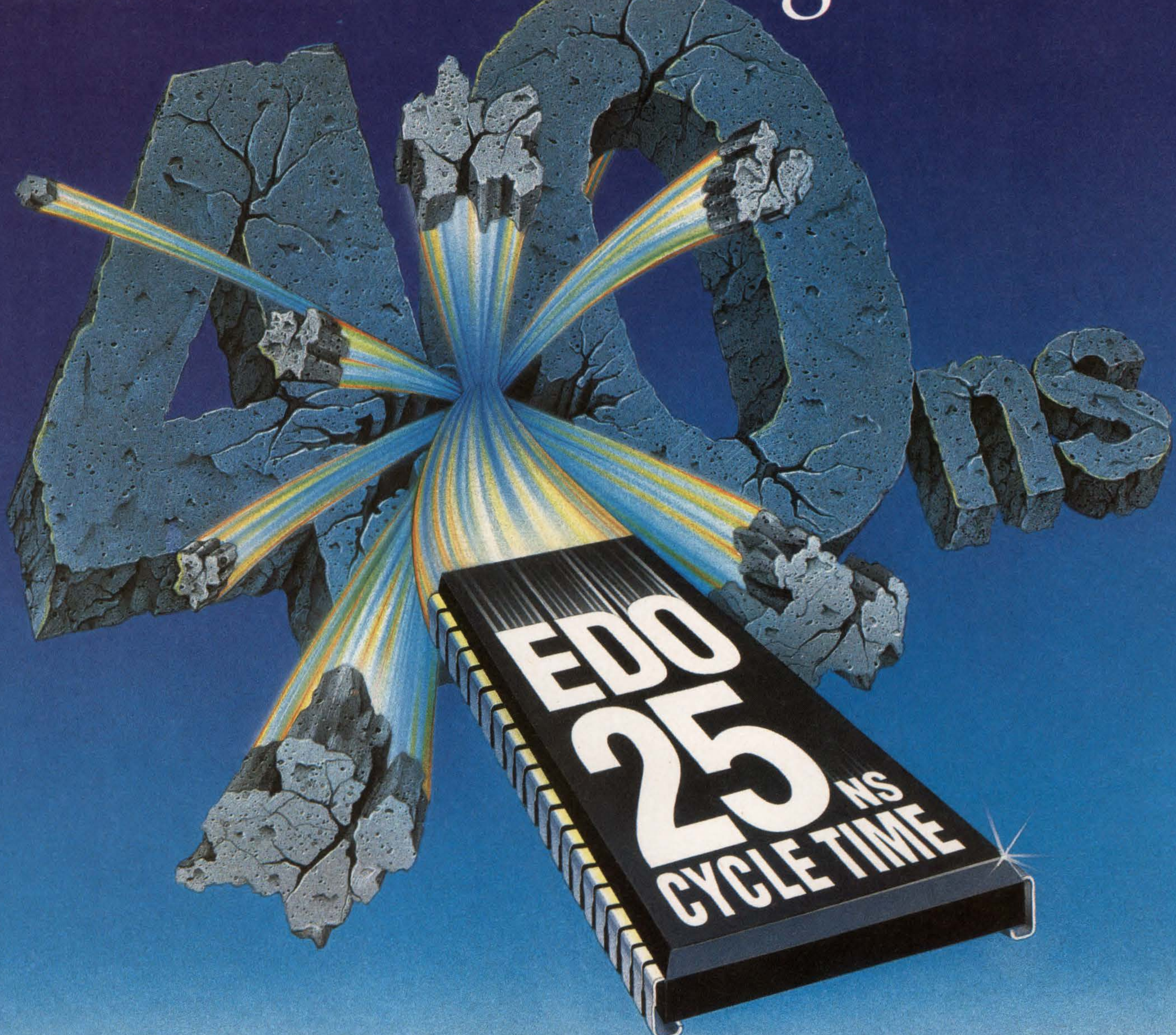

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Part Number	Density	Organization	Speed Grades/ Cycle Times (ns)	Samp./Prod. Availability
DRAMs				
MT4LC4M4E9	16 Meg	4 Meg x 4	60/25, 70/30	2Q94/4Q94
MT4LC2M8E7	16 Meg	2 Meg x 8	60/25, 70/30	3Q94/4Q94
MT4LC4007J	4 Meg	1 Meg x 4	60/25, 70/30	Now/2Q94
MT4C16270	4 Meg	256K x 16	60/25, 70/30	Now
VRAMs				
MT42C256K16A1	4 Meg	256K x 16	60/24, 70/27	Now
MT42C8256	2 Meg	256K x 8	60/24, 70/27	Now

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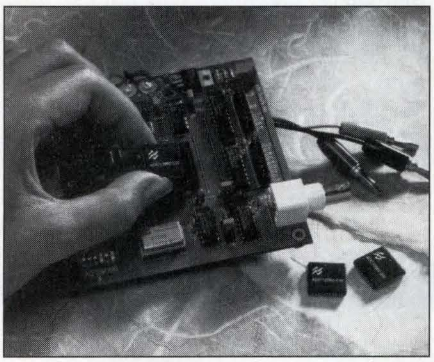
 CIRCLE NO. 79

INTEGRATED CIRCUITS

ICs drive optocouplers or serve as power-supply front ends. The UC39431 and UC39432 ICs contain an accurate voltage reference, a high gain-bandwidth error amplifier, and a linear-transconductance output-stage current source. In optocoupler applications, the linear transconductance amplifier replaces a common-emitter transistor amplifier, which has inherent nonlinear characteristics, to provide accurate control of the LED current. The UC39431 also includes three precision, low-temperature-coefficient resistors, which you connect to provide one of six regulated output voltages. An external resistor programs the UC39432's transconductance amplifier, allowing a more stable design in closed-loop optocoupler-feedback applications. Both ICs cost $1.25 (1000). **Unitrode Integrated Circuits Corp**, Merrimack, NH. (603) 424-2410. **Circle No. 397**



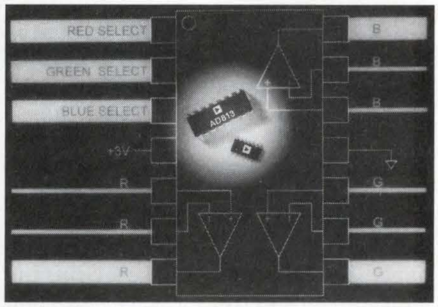
Instrumentation 12-bit ADCs have >1-MHz throughput. Competing with hybrid converters for high-speed instrumentation applications, the ADC12062 and ADC12662 feature throughputs of 1 and 1.5 MHz and maximum power dissipation of 75 and 200 mW, respectively. In power-down mode, both devices consume just 125 μW. Both ADCs offer a 2-channel input and an on-chip S/H amplifier. Guaranteed maximum integral nonlinearity for the two devices is ±1 and ±1.5 LSB, respectively. Both devices have a maximum differential nonlinearity of ±0.95 LSB. The respective S/N ratios of the 12062 and 12662 are guaranteed at 70 and 68 dB. Both devices are available in 44-pin plastic-leaded chip carriers and quad flatpacks. Prices begin at $29.21 and $33.70 (1000), respectively. **National Semiconductor**, Santa Clara, CA. (408) 721-2302. **Circle No. 398**

Video RAMDAC incorporates clock generators. The ICS5340 merges a triple 8-bit video DAC with a color-palette RAM and two timing generators. The device handles 24-bit color through 8-bit pseudocolor at clock rates to 135 MHz. Its timing generators provide a selection of eight video clocks and two memory clocks. Samples and demonstration boards are available. Prices begin at $6.95 (50,000). **Integrated Circuit Systems Inc**, Valley Forge, PA. (215) 630-5300. **Circle No. 399**

Buffer slews at 2000V/μsec. The BUF634 high-speed, unity-gain buffer amplifier features a 250-mA output in an SO-8 package. You can program the buffer for a bandwidth of 30 MHz with 1.5 mA of quiescent current or boost the bandwidth to 180 MHz with 15 mA of quiescent current. The device operates from ±2.25 to ±18V and has an internal current limit and thermal shutdown to withstand load faults and short circuits. $2.60 (1000). **Burr-Brown Corp**, Tucson, AZ. (800) 548-6132. **Circle No. 400**

DAC takes a maximum of 400 μA. The 12-bit MAX530 parallel-input, voltage-output DAC operates on 5 or ±5V supplies. An internal bandgap reference provides a 2.048V output that you can amplify, attenuate, invert or leave unconnected for multiplying applications. The IC performs 4-quadrant multiplication without external resistors or op amps, and the output-voltage range in those applications includes both supply rails. Otherwise, the internal buffer amplifier's gain-setting resistors define the output ranges of 0 to 2.048, 0 to 4.096, or ±2.048V. The DAC is guaranteed monotonic over temperature with a relative accuracy of ±½ LSB. The device comes in 24-pin DIPs and SOICs, and prices start at $5.45 (1000). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600. **Circle No. 401**

MOSFET driver operates from 8 to 60V. The LT1161 quad driver, a ruggedized N-channel device, provides a full 100% operating-voltage margin in 24 and 28V systems. Each of the four switch channels contains an internal charge pump and requires no external components to boost the n-channel MOSFET gate 12V above the supply rail. Channel-independent protection circuits function as four electronic circuit breakers. You can externally program the device's current limit, delay time, and automatic-restart period. In 20-pin DIPs and SOICs, the device costs $3.14 and $3.44 (1000), respectively. **Linear Technology Corp**, Milpitas, CA. (408) 432-1900. **Circle No. 402**



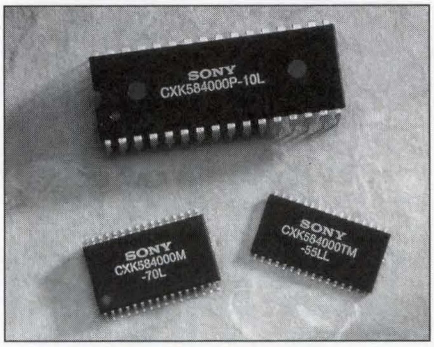
Triple and dual video op amps disable in 80 nsec. For $3.74 (1000), the AD813 provides three current-feedback op amps, each with an independent fast-disable function. The AD812 ($2.48, 1000) is the dual version. The op amps operate from a single 3V supply to a dual ±15V supply with 4-mA of supply current per amplifier. Video characteristics include a 125-MHz unity-gain –3-dB bandwidth, 0.03% differential gain error and 0.06° differential phase error. The op amps accommodate external loads in excess of 150Ω and offer 0.1-dB gain flatness to 50 MHz. In 14-pin (triple) and 8-pin (dual) DIPs or SOICs, the devices operate from –40 to 85°C. **Analog Devices**, Wilmington, MA. (617) 937-1428. **Circle No. 403**

Read-channel IC integrates functions. The MC34244 provides all of the functions required for the read-write channel of a constant-density hard-disk drive. The IC includes an AGC amplifier, an active filter, a pulse detector, a data synchronizer, a frequency synthesizer, a servo demodulator, an RLL1,7 encoder/decoder with write precompensation, and power management. The IC can operate at a 48-Mbps data rate with a supply voltage as low as 2.7V. $18.50 (10,000). **Motorola Inc**, Tempe, AZ. (602) 897-3615. **Circle No. 404**

256-kbit SRAMs achieve 12-nsec access time. The L7C199 and L7C199-L 256-kbit SRAMs come in 12-, 15-, and 25-nsec speeds. The 32k-word×8-bit devices operate from a 5V supply; inputs and outputs are TTL compatible. Power consumption is <800 mW max at a 25-nsec cycle time. In TTL standby mode, the SRAMs consume 100 mW for the standard version and 50 mW for the low-power version. Using CMOS levels the disspation drops to 10 mW for the standard version and 1 mW for the low-power version. The L7C199 and L7C199-L cost $4.92 and $5.41 (1000), respectively. **Logic Devices Inc**, Sunnyvale, CA. (408) 737-3300. **Circle No. 405**

Clock-distribution circuit operates from 10 to 125 MHz. The DA400 clock-distribution chip combines programmable timing generation, phase delay, and eight buffers in one package. The device achieves tight skew tolerance with an internal feedback circuit, which synchronizes the input and output clocks. The feature reduces part-to-part skew in applications requiring multiple clock drivers. Each of the eight outputs has its own programmable phase-delay circuitry with phase delays as short as 250 psec. $25.50 (5000). **AT&T Microelectronics**, Allentown, PA. (800) 372-2447. **Circle No. 406**

4-Mbit SRAM family features 3.3 or 5V operation. The CXK584000 family of asynchronous 4-Mbit SRAMs features 3.3 or 5V operation. The family is available in 24 versions, including two power levels, three speeds, and four package types. The 524k×8-bit memory devices use polysilicon thin-film technology to reduce current requirements and increase data retention. The three speed choices include 55, 70, and 100 nsec at 5V ±10%. Access times double when operating at 3.3. A 55-nsec, low-power version costs $257.10 (1000). **Sony Component Products Co**, Cypress, CA. (800) 288-7679. **Circle No. 407**



PCMCIA host adapter has DMA support. The CL-PD6722 dual-slot host adapter provides direct-memory support for peripherals on the ISA bus. The DMA relieves CPU intervention when large data transfers are required from a PCMCIA I/O-card device. Because the system DMA is designed for moving data from an I/O device to memory, it can complete this task faster, using less bandwidth than the CPU would by doing the equivalent I/O cycles to the card. The adapter requires only 2 square in. to implement a full-slot control subsystem. $20 (1000). **Cirrus Logic**, Fremont, CA. (510) 226-2261. **Circle No. 408**

FIFO family meets telecomm-equipment requirements. The SN74ACT222X FIFO family synchronizes two serial data streams in telecommunications equipment. The dedicated 1-bit FIFOs provide a cost-effective solution to the 4-, 8-, or 9-bit standard FIFOs used to synchronize two serial streams. The devices also support time-division-multiplexing applications in which several asynchronous communication signals are mapped into one higher-rate aggregate signal. In addition, the FIFOs provide elastic store to synchronize the instantaneous difference between multiple clocks. Prices range from \$3.50 to \$6.50. **Texas Instruments Inc**, Denver, CO. (800) 477-8924, ext 4500. **Circle No. 409**

Switching regulator adds overtemperature protection. The MIC631 and MIC641 series are pin-compatible, plug-in replacements for MAX631/41 regulators. The MIC631/32/33 use only two external components in power conversion up to 150 mW. The MIC641/42/43, with an external FET, deliver up to 10W of output power. Both series are available in 5, 12, 15, and 3.3V output-voltage versions. A thermal-protection circuit prevents catastrophic IC failure by providing shutdown protection at specified overtemperature levels. With a 5V output, quiescent current is 120 μA. In 8-pin DIPs and SOICs, the 5V versions cost \$2.45 (1000). **Micrel Semiconductor Inc**, San Jose, CA. (408) 944-0800. **Circle No. 410**

T1 device provides SONET speeds. The TDC5101 high-level data-link controller (HDLC) sends and receives data over public communications networks at 51.84 Mbps, the rate specified as SONET STS-1. The device interfaces to LANs, such as Ethernet and token ring. It also interfaces to Frame Relay, X.25, and other slower public WANs, including T-1, T-3, E-1, E-2, E-3, and JT-2 WANs. The device has a no-limit packet length, which provides more flexibility than do strictly fixed-length devices. The device also supports fixed-length packets of 300, 2400, or 9600 bytes. \$55 (1000). **Texas Instruments Inc**, Denver, CO. (800) 477-8924, ext 4500. **Circle No. 411**

Fast SCSI adapter interfaces to PCI bus. The AIC-7870, a single-chip adpater for mother boards, offers an on-chip 10-MIPS RISC processor that manages all SCSI sequences. Workstations and servers using a 133-Mbps PCI local bus can transfer data at fast and wide SCSI speeds of 20 Mbps. Optional differential cabling lets you transfer data reliably at high speeds. The chip includes a host interface, the SCSI protocol section, a 10-MIPS μP, and a 256-byte FIFO buffer. The chip comes in a 160-pin package. \$39 (OEM). **Adaptec Inc**, Milpitas, CA. (800) 934-2766. **Circle No. 412**

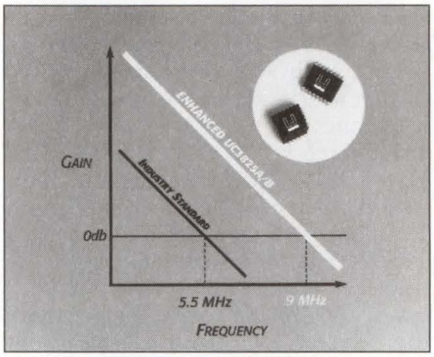
Fibre-channel set runs full speed. The EZ-Link chip set runs the Fibre Channel protocol, FC-0 layer at a 1.0625-Gbps data rate. The transmitter and receiver operate at 3.3V, offer TTL I/O levels, and come in 44-pin plastic quad flatpacks. Price for the pair is <\$90 (1000). **Vitesse Semiconductor**, Camarillo, CA. (805) 388-3700. **Circle No. 413**

Audio IC handles 16-bit stereo. Offering all the functions of the Sound Blaster Pro except FM synthesis, the 82C928 costs just \$15 (1000). The device offers interfaces for the Windows Sound System, the AT bus, the OPL-3 and -4, and MIDI. It also has a CD-ROM-drive interface and handles 16-bit data at a 48-kHz data rate. **Opti Inc**, Santa Clara, CA. (408) 980-8860. **Circle No. 414**

PCI graphics chip set uses DRAM. The ALG2301 graphics-accelerator chip set offers autoconfiguring PCI and feature-connector interfaces, a 24-bit RAMDAC, and dual clock generators in a 3-chip set for <\$20. The set uses

256k×4- or×16-bit DRAM and provides resolution to 1280×1024 pixels. BIOS and driver software are available. **Avance Logic Inc**, Fremont, CA. (510) 226-9555. **Circle No. 415**

PWM controllers operate at 1 MHz. The UC3823A/B and UC3825A/B family of current-mode controllers typically require a start-up current of 100 μA, which makes them ideal for off-line switching power supplies and dc/dc converters. The parts have a 9-MHz unity-gain bandwidth, drive a 2A pk output load, offer leading-edge blanking, and operate in push-pull or single-ended mode. A high-speed overcurrent comparator with a 1.2V threshold sets an internal latch to ensure full discharge of the soft-start capacitor before allowing a restart. From $3.96 and $4.73 (1000), respectively. **Unitrode Integrated Circuits Corp**, Merrimack, NH. (603) 424-2410. **Circle No. 416**



Single IC embodies key Ethernet functions. The NCR92C120 contains the Manchester codec, 802.3 AUI, and 10Base-T transceiver logic in a 100-pin plastic quad flatpack. It performs automatic media-type determination and polarity correction. To reduce cost in multiport switching applications, it lacks bus-interface and buffer-management logic. $14.95 (10,000). **NCR Corp**, Dayton, OH. (800) 334-5454. **Circle No. 417**

Voice chip attains consumer pricing. The ISD1100 is a solid-state analog record and playback device that stores 10 sec of sampled audio. Because it stores the audio as analog charge levels in EEPROM, the device does not need A/D conversion. It contains input and output preamplifiers, AGC, and filters on-chip. Cost is $5.48 in DIP packages; $4.18 as bare die (1000). **Information Storage Devices**, San Jose, CA. (800) 332-8638. **Circle No. 418**

PowerPC chip set offers PCI bus. Combining a CPU bridge to the PCI bus with an ISA bridge to the PCI bus, the IBM27-82650 chip set allows creation of a Power PC-based PC with local-bus compatibility. The set supports a 64-bit memory bus, operates at 33 MHz on the ISA bus and 66 MHz on the Power PC bus, and includes bus error detection and correction. Cost is $53 (50,000), and full production is scheduled for April. **IBM Microelectronics**, Hopewell Junction, NY. (800) 426-0181. **Circle No. 419**

Nonvolatile memory includes real-time clock. The STK1390, an 8k×8-bit CMOS RAM, provides integral EEPROM that maintains a nonvolatile copy of RAM data. The device also includes a real-time clock that operates for months by drawing power from an external capacitor. The device comes in DIP and SOIC packages with

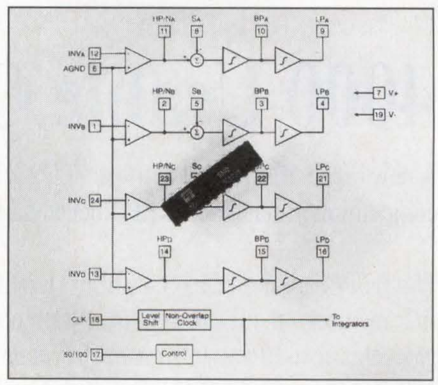
INTEGRATED CIRCUITS

30-, 35-, and 45-nsec speeds. Prices begin at $13.99 (1000). **Simtek Corp**, Colorado Springs, CO. (719) 531-9444.
Circle No. 420

Clock adapter matches international rates. Compatible with both the US T1 and European E1 transmission rates, the LXP610 performs clock frequency conversion without using crystal oscillators. The device extracts the incoming data's clock and uses PLL-based frequency synthesis to match the system's backplane rate. It accepts input clocks between 1.544 and 8.192 MHz, providing 17 selectable input/output frequency combinations. Cost is $11 (1000). **Level One Communications Inc**, Folsom, CA. (916) 985-3670.
Circle No. 421

PC chip set beats Energy Star power restrictions. The Redwood System controller chips, PT86C618 and PT86C668, reduce a 486-based PC's power requirements from 150 to 20W peak, 10W average, and 2W standby. The chip set manages system power consumption by monitoring CPU activity and turning off unused system circuits during each clock cycle. It also controls CPU clock speed, slowing the CPU during idle periods. Price is $30 (10,000). **PicoPower Technology**, San Jose, CA. (408) 954-9898. **Circle No. 422**

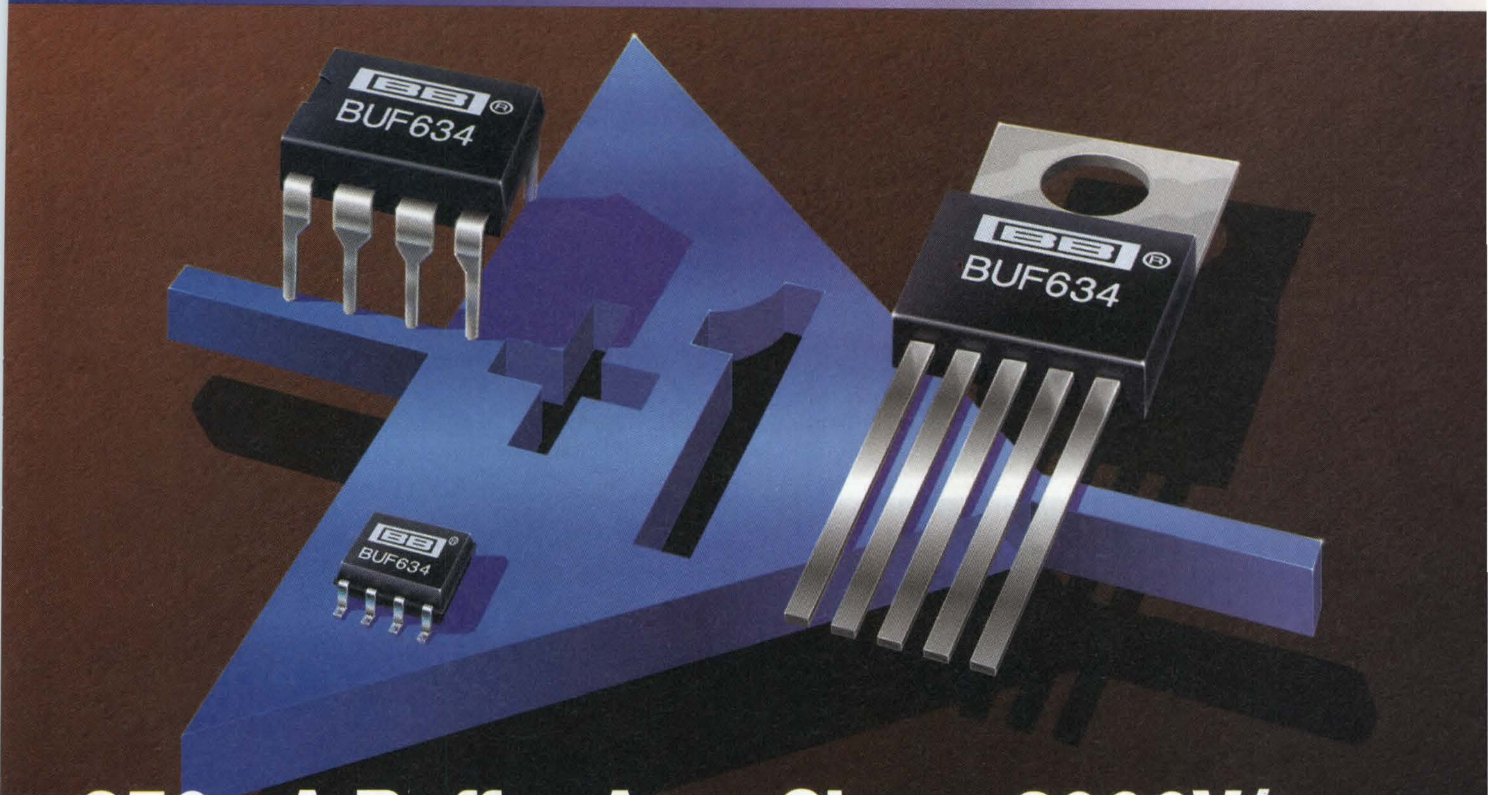
MPEG audio decoder fits in small package. The SAA2500 MPEG decoder complies with MPEG Layers 1 and 2 and automatically conforms to the audio data rate. It also demultiplexes ancillary data in the audio bit stream. The device has selectable output-data precision from 16 to 22 bits and provides automatic de-emphasis of the decoded audio. Sample cost is $25. **Philips Semiconductors**, Sunnyvale, CA. (800) 447-1500, ext 3000.
Circle No. 423



Dual and quad switched-capacitor filters. The SC64 and SC60 are 24-pin quad and dual second-order universal filter building blocks, respectively. The clock frequency and three to five external resistors control the center frequency, gain, and Q of each filter section. The supply voltage ranges from ±2.4 to ±9V. The maximum clock frequency is 7 MHz. The SC64 ($5.71, 100) is pin compatible with the LTC1064, and the SC60 ($2.36) is compatible with the LTC1060 and MF10. **Electronic Technology Corp**, Ames, IA. (515) 296-7000. **Circle No. 424**

Fiber-optic devices handle ATM. Applicable to ATM and SONET networks, the ES-9304T transmitter and ES-9216R receiver work with data rates to 622 Mbps. The devices operate in the optical range over single-mode fiber and cost $1300/pair. A related

NEW



250mA Buffer Amp Slews 2000V/µs

Small But Powerful

BUF634 is a high speed, unity-gain buffer amplifier that delivers 250mA output and 2000V/µs slew rate—all in a tiny SO-8 package. Its low price, high performance, and ease of use make BUF634 ideal for a wide range of applications. It's an excellent driver for valves, solenoids, video, and even headphones.

Versatile Yet Simple

BUF634 can be used inside the feedback loop of op amps to increase output current, eliminate thermal feedback, and improve capacitive load drive. Its bandwidth can be pin-programmed for 30MHz with 1.5mA quiescent current or boosted to 180MHz with 15mA quiescent current. BUF634 is the simple solution for all your buffer needs.

Easy And Rugged

BUF634's monolithic design is very rugged—its internal current limit and thermal shutdown protect it from extreme abuse. BUF634 withstands load faults and short-circuits with ease. It's virtually indestructible—you can design-in this device with confidence.

BUF634 Key Specifications

- Output current..250mA
- Slew rate..2000V/µs
- Pin-selected bandwidth ....30MHz to 180MHz
- Quiescent current ....1.5mA (30MHz BW)
- Supply range..±2.25V to ±18V
- Protection ....internal current limit, thermal shut-down
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CIRCLE NO. 81

device, the SDM4123-XC ($210), combines transmit and receive functions for 155-Mbps applications. **Sumitomo Electric**, Tarrytown, NY. (914) 347-3770. **Circle No. 425**

Lamp driver controls contrast. The ML4864 backlight IC produces enough voltage to drive miniature cold-cathode fluorescent lamps and the contrast voltage to power LCDs. Using standard off-the-shelf external components, you can set the device's input and output voltage to almost any level within the respective 40 to 20V and 100 to 2000V ranges. You can also set the dc contrast voltage to a positive or negative polarity. The IC features a power-down mode that independently shuts off the high-voltage lamp-drive circuits while maintaining the LCD contrast voltage. In a 20-pin shrink SOP, the device costs $2.95 (1000). **Micro Linear Corp**, San Jose, CA. (408) 433-5200. **Circle No. 426**

SHORTS

Semtech (Newbury Park, CA, (805) 498-2111) has upgraded its EZ Dropper line of dc/dc converters. The new ICs provide a wider current range—10 mA to 1A—than the original design's 200 mA to 1A. The company has also added a low-current—5- to 250-mA—version to the line. **Circle No. 427**

The $100 TB310I test board provides a quick way to evaluate Ericsson Components' (Richardson, TX, (214) 907-7911) PBL3774 and PBL3775 switch-mode (chopper) constant-current drive ICs. The board drives two bipolar stepper motors in full-, half-, and quarter-step modes. Advanced users can also implement one-third- and one-fifth-step modes. **Circle No. 428**

RF Monolithics Inc's (Dallas, TX, (214) 233-2903) family of single- and dual-port SAW resonators cover frequencies from 224.3 to 433.9 MHz. Nonlicensed wireless applications use these frequencies internationally. **Circle No. 429**

Analog Devices (Wilmington, MA, (617) 937-1428) is filling out its offerings of single-supply op amps. The OP-495 ($3.95 (100)) rail-to-rail output amplifier is a quad version of the OP-295. The OP-113 ($1.60 (100)) and -413 ($5.35 (100)) are single and quad versions, respectively, of the OP- 213 dual-precision amplifier. **Circle No. 430**

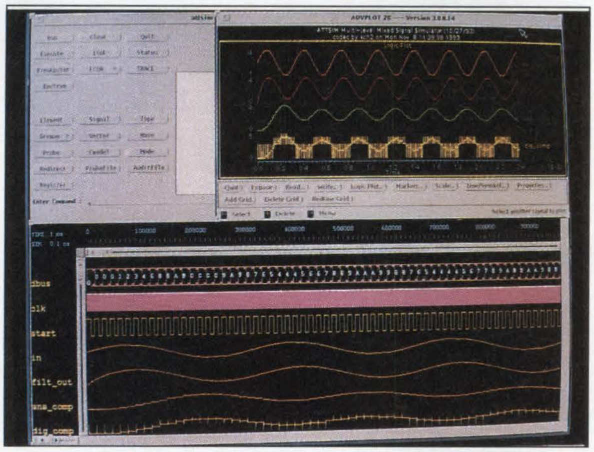
Logic Devices Inc has added the 10-nsec, 16-bit LPR200 8-level and LPR201 7-level pipeline registers to its product family ($10). **Circle No. 431**

S-MOS Systems is offering its ASIC customers a quad flat-pack package with integral copper heat sink and heat spreader. The package handles 2.4W without airflow; 7W with. **Circle No. 432**

Semtech Corp now serves as an alternate source for select power ICs from Motorola, Unitrode, and Silicon General. **Circle No. 433**

Brooktree Corp is offering an $1800 developer's kit for creating video capture, video playback, and graphics accelerator cards with its Bt885 CacheDAC and Bt812 video-decoder ICs. **Circle No. 434**

Mixed-signal simulator accepts multilevel models



Using ATTSIM, designers can simulate complete mixed-signal systems by combining abstract behavioral models with detailed device models for the circuit's analog and digital portions.

The ATTSIM Multi Level Mixed Signal Simulator lets you simulate mixed analog-digital systems using any combination of Spice, VHDL (VHSIC Hardware Description Language), C, behavioral, and gate-level models. The simulator is equally capable of performing simulations of large analog or digital designs.

Because the simulator accepts all different levels of models, it suits both top-down or bottom-up design methodologies. You can start at a high level of abstraction and gradually move down into more detailed logic descriptions; or you can opt to complete the detail design of a crucial subsystem and then simulate the remainder of the system around it. The simulator also offers the flexibility to use the modeling level that is most appropriate for speed vs accuracy as you simulate a system.

In addition to the company's model libraries, the software supports Logic Modeling's Smart Models as well as the ATTSIM ModelWriter, which generates analog, digital, and mixed-signal models in C. The ATTSIM mixed-level simulator will be available in March. A single CPU license for Sun SPARC or HP 700 series systems costs $65,000.—**Doug Conner**

AT&T Design Automation, Murray Hill, NJ. (908) 582-4083. **Circle No. 373**

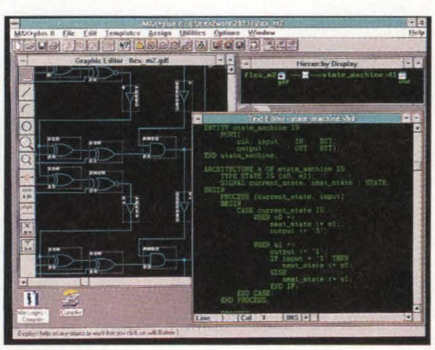
PLD design tool adds VHDL synthesis

Max+Plus II version 4 adds VHDL (VHSIC Hardware Description Language) synthesis to its PLD design capabilities. The new software takes advantage of 32-bit operating systems and runs on Windows 3.1, Windows NT, and Unix workstations. For engineers unfamiliar with VHDL, the software provides VHDL templates and integrated on-line help. When synthesizing logic from a VHDL description, the software uses different optimization techniques, depending on which family of the company's PLDs you have. The synthesis tool takes advantage of architectural features specific to the PLD you are using.

The new release also provides timing and area information to Synopsys synthesis tools; thus, users of the tools can opt to trade off speed vs area to meet design requirements.

Max+Plus II version 4 is a free upgrade to users with maintenance agreements. VHDL synthesis (PLSM-VHDL) is not included in the upgrade; it costs $3995 for PCs and $6995 for Sun HP and DEC systems.—**Doug Conner**

Altera Corp, San Jose, CA. (408) 894-7000. **Circle No. 374**



Max+Plus II software supports a hierarchical, top-down design methodology, integrating schematics and VHDL in a context-sensitive environment.

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VHDL simulators offer presynthesis model development. The VHDL System Simulator Family (VSS) includes the VSS Professional and VSS Expert simulators. VSS Professional for presynthesis-model VHDL development and system verification combines interpreted and compiled simulation engines. VSS Expert includes all the features of VSS Professional, plus a gate-level signoff simulation engine and system-level modeling capability. VSS Professional costs $13,000, and VSS Expert costs $24,000. **Synopsys Inc**, Mountain View, CA. (415) 962-5000.
Circle No. 375

Digital circuit simulator finds minimum and maximum timing problems. The PLogic simulator performs worst-case timing analysis using the range of delays specified by the IC manufacturer. This simulator finds problems that slip through simple single-delay analysis tools. The simulator also finds and flags setup and hold or worst-case timing violations. The software provides non-encrypted libraries of more than 1800 digital devices and lets you model devices directly from data-book specifications. Design Center with PLogic includes schematic capture and starts at $3250 on PCs and $14,000 on Sun workstations. **MicroSim Corp**, Irvine, CA. (714) 770-3022. **Circle No. 376**

Electromagnetic-analysis program simulates 3-D designs. The EMC electromagnetic-analysis program simulates finite elements and predicts EMI, crosstalk, and coupled-eddy currents at any number of frequencies or for any time-domain problem. EMC runs on HP, IBM, SGI, and Sun workstations. The software costs $19,950; you can lease it for $950/month. **Aries Technology**, a division of MacNeal-Schwendler Corp, Lowell, MA. (508) 453-5310. **Circle No. 377**

VHDL-1076 simulator achieves high gate-level simulation performance. The Vulcan simulator supports the IEEE VHDL-1076 and VHDL-VITAL ASIC modeling standards. VITAL defines a set of VHDL

primitives that are typically in ASIC cell libraries. It also defines a modeling style and a method for associating timing information with the cell primitives. The result is fast gate-level simulation that the company claims is comparable to Verilog-XL. Vulcan will be available initially on Sun and HP workstations starting at $20,000. **GenRad Inc**, Concord, MA. (508) 369-4400. **Circle No. 378**

Thermal models for Motorola components. Motorola is creating 3-D thermal models of its components for use with Flowmerics Flowtherm computational-fluid-dynamics software. The models let you simulate and develop cooling methods before building the hardware. A Flowtherm software license costs $11,000/year. **Flomerics Ltd**, Surrey, England. +44 (0)81-547 3373. **Circle No. 379**

CAD system offers mechanical CAD compatibility. The CADnexion software program offers support for electronic and mechanical CAD methods. It helps designers of high-frequency circuits precisely define physical structure. CADnexion runs on PCs and starts at $4995. **Bay Technology**, Aptos, CA. (408) 688-8919. **Circle No. 380**

System speeds prototyping for DSP designs. The Paradigm RP modular system lets you use FPGAs, RAM, ROM, DSP, and microprocessor cores to emulate systems. The initial offering suits DSP systems but allows you to emulate other systems. Paradigm RP starts at $60,000. **Zycad Corp**, Fremont, CA. (510) 623-4400. **Circle No. 381**

ECAD tool lets you graphically create Verilog models. Working in a graphical design environment, you can create Verilog behavioral models by describing events and the corresponding reactions of a model. DesignVision graphically represents a behavioral model as a collection of threads. Each thread represents a series of events and actions. As each event occurs during simulation, the software performs a corresponding action. All threads are active at once. The graphical-threads representation eases your ability to see separate operations that occur simultaneously. DesignVision is initially available on Sun Sparc systems for $15,000. **Vista Technologies Inc**, Schaumburg, IL. (708) 706-9300 **Circle No. 382**

Document-management system runs under Windows. The AutoEDMS document-management system for Windows lets you find, store, manage, retrieve, view, and print virtually every type of drawing, document, and image. The software provides document tracking to meet ISO 9000 requirements. AutoEDMS for Windows starts at $895. **ACS Telecom**, Lomita, CA. (310) 325-3055. **Circle No. 383**

EPLD-design software costs $89.95. XEPLD version 4.1 is a design tool for Xilinx XC7000 family of erasable programmable logic devices (EPLDs). The software interfaces to logic compilers, such as ABEL, CUPL, and Palasm. **Xilinx, Inc**, San Jose, CA. (408) 559-7778. **Circle No. 384**

ELECTRONIC DESIGN AUTOMATION

Model simulates PowerPC. This model of the PowerPC 603 μP for Cadence's Verilog-XL and Leapfrog VHDL simulators, costs \$4900 and runs on IBM and Sun workstations. **Motorola**, Austin, TX. (512) 891-2839.
Circle No. 385

VHDL simulator accepts Verilog models. Cadence's Leapfrog VHDL simulator directly imports Verilog models. The option interfaces to Logic Modeling's SmartModels and hardware models. From \$12,000; Leapfrog 1.1 starts at \$20,000. **Cadence Design Systems**, San Jose, CA. (408) 943-1234.
Circle No. 386

Windows-based tool offers drawing viewing and markup. ForReview for Windows lets you view and mark up drawings. A limited version, ForView, does not let you save the drawing markups. ForReview costs \$495; ForView costs \$295. **Advanced Technology Center**, Laguna Hills, CA. (714) 583-9119
Circle No. 387

SHORTS

Intusoft is offering a Spice bulletin-board service (BBS) on Compuserve. The BBS provides models, technical-application notes, software utilities, and demonstration software. It is under the CADD/CAM/CAE vendor forum. **Intusoft**, (310) 833-0710.
Circle No. 388

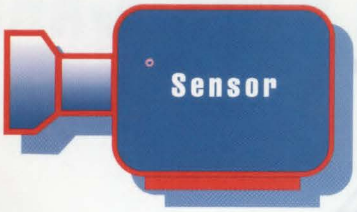
Model Technology's V-System/Workstation VHDL simulator supports Logic Modeling's SmartModel Library, which simplifies simulation of system-level designs. **Model Technology**, (503) 641-1340.
Circle No. 389

Harris EDA offers design kits for Texas Instruments' high-density-interconnect (HDI) MCM technology. **Harris EDA**, (716) 924-9303.
Circle No. 390

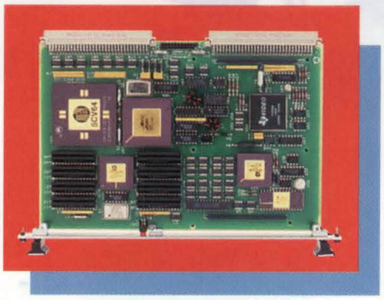
Mentor Graphics has introduced a high-speed board-design kit for Intel's Pentium processor chip set. The kit includes logic symbols, mapping files, geometry, signal-integrity-I/O models, thermal models, reference layout for the core logic, and electrical rules. The design kit is free and works with the Mentor Graphics Board Station 500 timing-driven layout system. **Mentor Graphics**, (503) 690-2093.
Circle No. 391

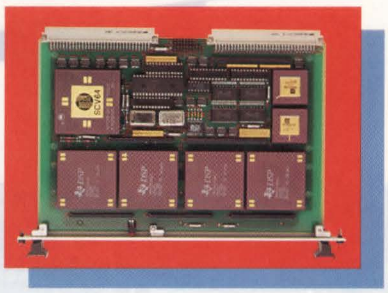
OrCad is planning to act as an OEM for Model Technology's VHDL simulator for Windows. **OrCad**, (503) 671-9500.
Circle No. 392

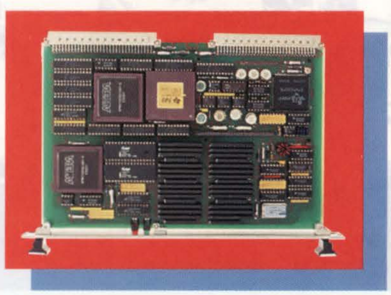
Data I/O is offering users of the ABEL version 4 software a 60% discount to upgrade to the company's Synario universal-FPGA-design system. The discount applies to the base Synario product, which costs \$2995, and the PLD library kit, which costs \$995. ABEL version 3.2 or earlier users will receive a 40% discount. **Data I/O**, (206) 881-6444.
Circle No. 393



THE BETTER WAY TO GET FROM HERE...







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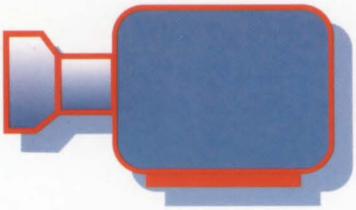
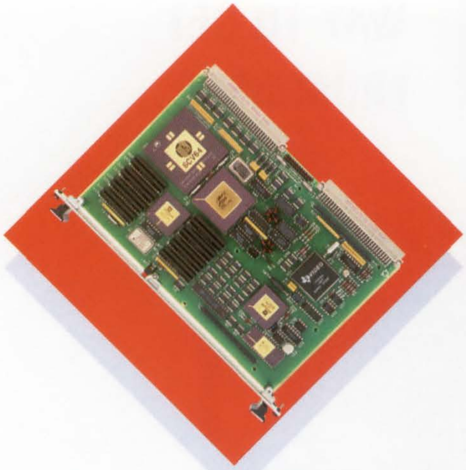
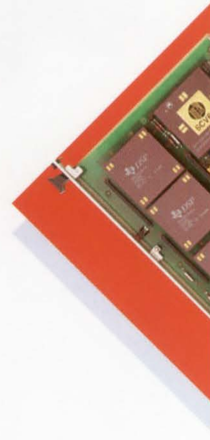
DY 4 Systems Inc

DY 4 Introduces Three VME Cards







SENSOR

- video
- radar
- sonar

674 FRAME-GRABBER

- Frame capture/display
- Scan-rate conversion
- 35M samples/sec, 8 bits, 3 inputs
- Supports 16-bit digital video input
- Optional on-board TMS320C40
- RGB output to 1024 x 1024 x 8
- Built-In-Self-Test

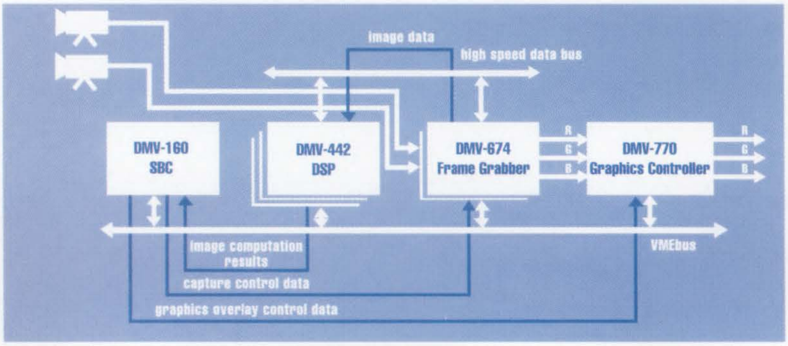
DY 4 introduces an off-the-shelf integrated solution that can take data from sensors right through to a video display terminal. Our Frame Grabber, Quad 'C40 DSP and Graphics Controller work together seamlessly to capture data from one or more sensors, process the findings and display them in real-time.

FRAME-GRABBER

The 674 frame-grabber, operates at 35M samples per second, and has its own C40 on board for extra processing power. Whether its grabbing video, radar or sonar data, the 674 offers high-performance signal data capture and manipulation in real-time.

THREE CARDS = ONE INTEGRATED SUBSYSTEM.

By utilizing a high-speed 50M bytes/sec image bus, DY 4 delivers VMEbus integrated "vision processing" for multi-C40 and frame grabber applications. The benefit to you? With DY 4 resolving the hardware integration issues, you can concentrate on building a better application. Here are some of the features of this high-performance triple-card set.

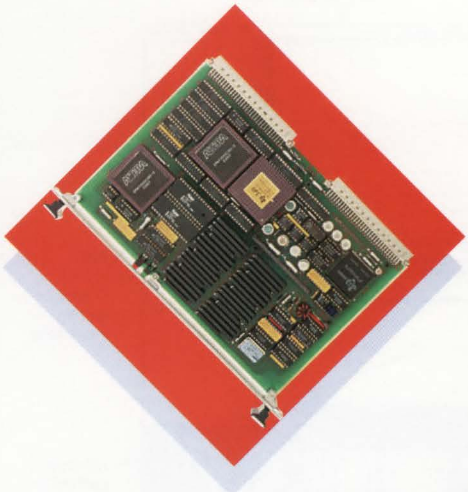


Demonstration of complete image solution: 674 captures sensor video; 770 displays video within window on high-res display; imagebus link to 442 DSP used for real-time image analysis.

QUAD 320C40 DIGITAL SIGNAL PROCESSOR

A 50M bytes/sec image bus can link multiple frame grabbers to multiple 442 Quad 'C 40-based digital signal processors. Using four Texas Instruments 320C40 DSP devices running at 40 MHz, the DY 4 Quad 'C40 has been designed with the military environment in mind. It's fast, cost-effective, reliable, and 100%

That Can Do Wonders For Your Image.



*

442 QUAD 'C40 DSP

- Four 40 MHz TMS320C40 digital signal processors
- 4M bytes to 16M bytes total SRAM
- High speed 50M bytes/sec multi-master image bus
- Inter-processor mailbox interrupts
- Externally accessible 'C40 Com ports
- Built-In-Self-Test

770 GRAPHICS CONTROLLER

- 34020 Graphics System Processor
- Color overlay on RGB or mono video input
- RGB output to 1280 x 1024 x 8
- Optional support for dual display or flat panel
- X-Windows, CGI, or RTGS graphics firmware
- Built-In-Self-Test

VIDEO

- live video in a window
- color on color overlay
- X-windows

software compatible from commercial to Mil.

770 GRAPHICS CONTROLLER

The 770 Graphics Controller, offers single-board high-resolution graphics generation. Based on the 34020 Graphics System Processor, the card offers 1280 x 1024 resolution graphics on color analog overlay, and optional mezzanine cards for dual display or flat-panel display outputs.

COMPREHENSIVE SOFTWARE DEVELOPMENT ENVIRONMENT

As you'd expect from DY 4, each card comes with a comprehensive set of card-level diagnostics and other commonly requested OS drivers and application software packages. The Quad 'C40 DSP also features Ada support from Tartan, C, C++, a set of optimized signal/vector processing libraries, and the Toolsmiths CASEworks™ development environment (more on CASEworks on the back of this insert!). The 770 graphics controller comes with a choice of graphics software: an Ada/C real-time driver RTGS, X-Windows, or CGI.

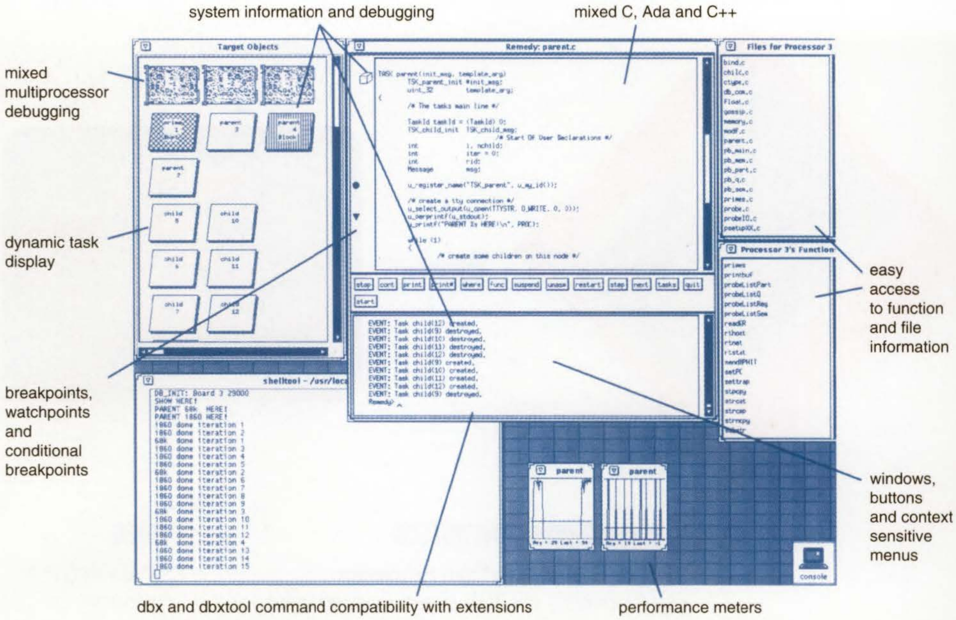
DY 4 invites you to discover more about the better way to get your data from the sensor to the screen. All the technical details are just a phone call away. Call DY 4 Systems at: USA (East) 603-595-2400; USA (West) 408-377-9822; Europe 0222-747927; Asia/Pacific and Canada 613-596-9911.

FROM COMMERCIAL TO MILITARY...

As with all DY 4 VMEbus products, these three cards feature 100% software and electrical compatibility, from commercial right up to Mil spec. This ensures that the application software you design on our SVME commercial boards will work exactly as expected, no matter how far up the specification ladder your application needs to climb.

* Application display provided by Gallium Software Inc.

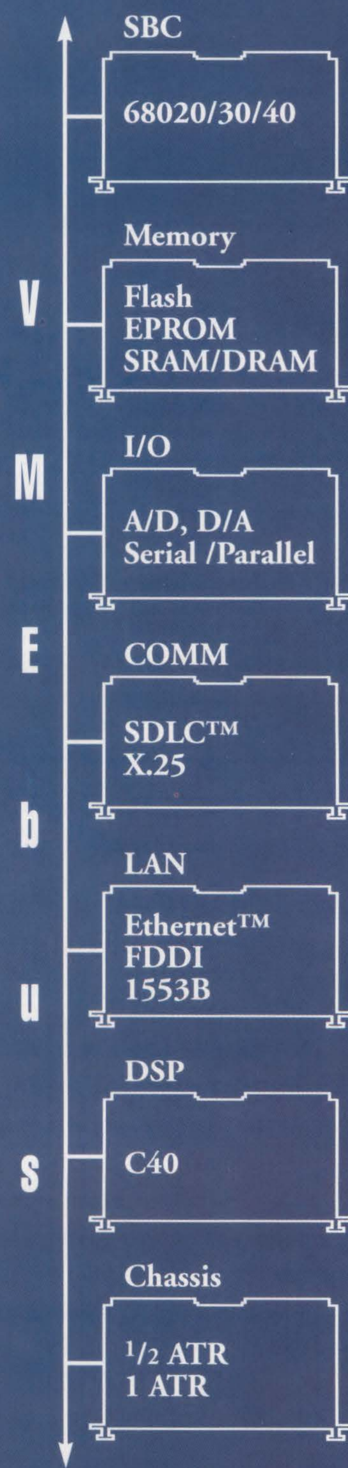
SOFTWARE DEVELOPMENT SUPPORT, WITH CASEworks™



DY 4's Quad 'C40 DSP, the processor at the heart of our integrated three-card set, features Toolsmiths CASEworks™, a software development environment that helps you develop and produce better products faster, more easily, and at a lower cost. The CASEworks Remedy™ debugger, shown here, offers target debugging with dynamic displays, multiple windows, buttons, menus and mixed multiprocessor support. Fault isolation, diagnosis and system control have never been easier.

CASEworks is an example of DY 4's continuing commitment to software development support... and one more persuasive reason to make DY 4 your VME supplier of choice.

The DY 4 triple-card set has been designed to work with DY 4's broad product line:



DY 4 Systems Inc

Customer First, Quality Always

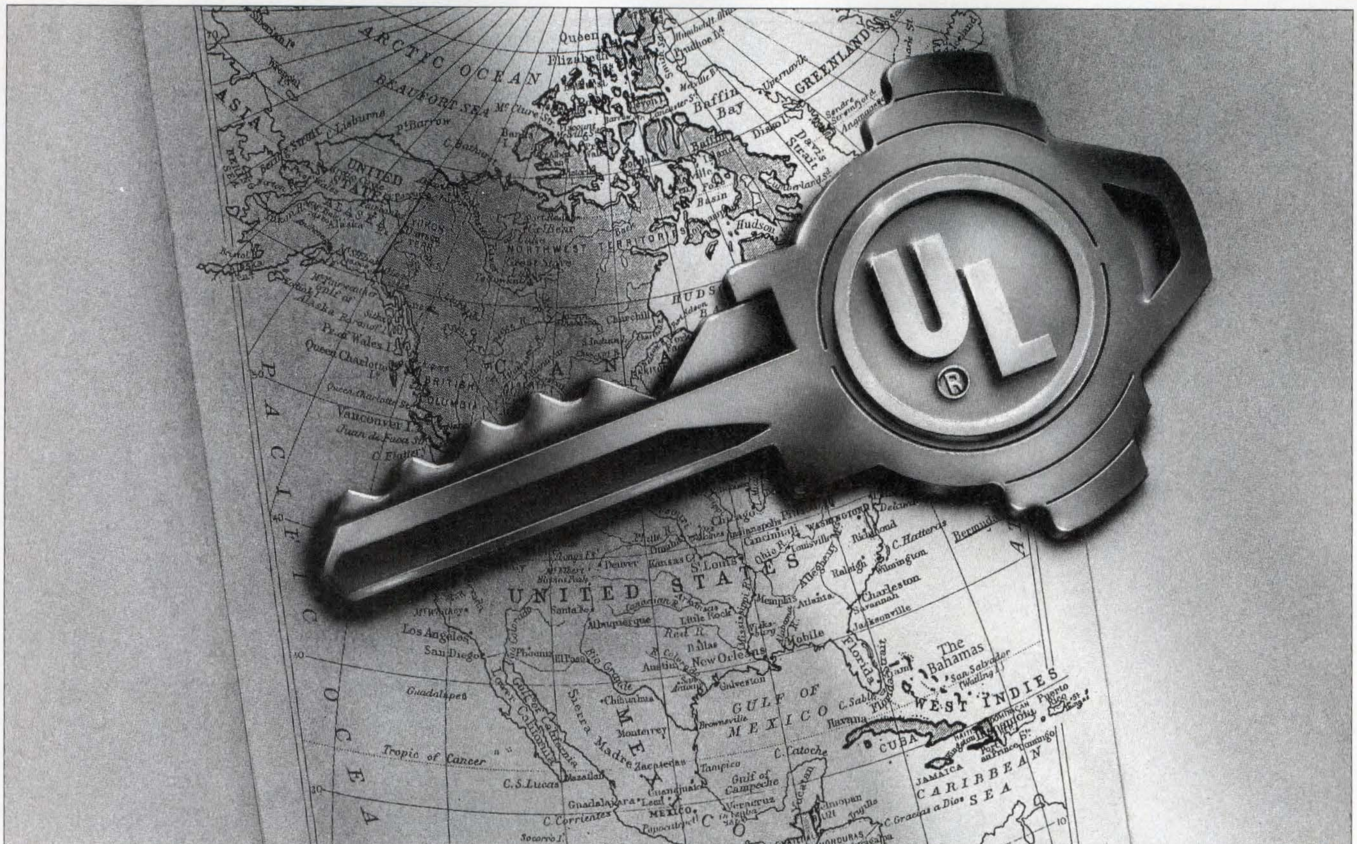
DY 4 Systems Ltd.
USA West: Tel: 408-377-9822
Fax: 408-377-4725
USA East: Tel: 603-595-2400
Fax: 603-595-4343

DY 4 Europe
Tel: 0222-747927
Fax: 0222-762060

DY 4 Canada
Tel: 613-596-9911
Fax: 613-596-0574

DY 4 Asia/Pacific
Tel: 613-596-9911
Fax: 613-596-0574

For more information about how we can help you, call the number of our office nearest you, or fill out the accompanying business reply card.



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CIRCLE NO. 85

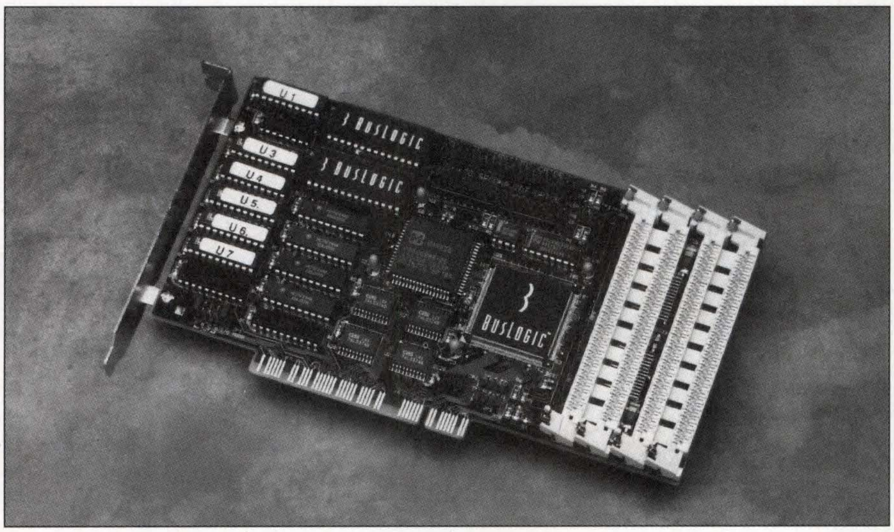
IDE cache controller boosts disk-I/O rates

The BusLogic KT-410A, 910A, and 510A IDE cache controllers for the VL, PCI, and ISA buses, respectively, greatly increase the throughput of data between disk drives and a system processor. The PCI- and VL-bus versions transfer data at 5 Mbytes/sec on the disk side and 20 Mbytes/sec on the system side. The ISA version has a transfer rate of 5 Mbytes/sec on both sides.

Each controller connects a system to four IDE drives, each storing as much as 4 Gbytes, and two floppy-disk drives. You can configure the controllers to provide disk mirroring or linking. The controllers require the addition of DRAM cache memory in 256-kbyte, 1-Mbyte, or 4-Mbyte SIMMs. You can mix and match different-capacity SIMMs for a total of 512 kbytes to 16 Mbytes of cache. The VL, PCI, and ISA versions cost $175, $255, and $105, respectively.

—Gary Legg

BusLogic Inc, Santa Clara, CA. (408) 492-9090. **Circle No. 369**



IDE cache controllers from BusLogic Inc increase disk-I/O rates to as much as 20 Mbytes/sec.

SCSI adapter for PCI bus processes 2000 I/O requests/sec

QLogic's QLA1000-PI SCSI host-adapter board for the PCI bus processes 2000 I/O requests/sec while queuing 1600 requests/sec. It provides burst data transfers at 132 Mbytes/sec and sustained transfers of 20 Mbytes/sec.

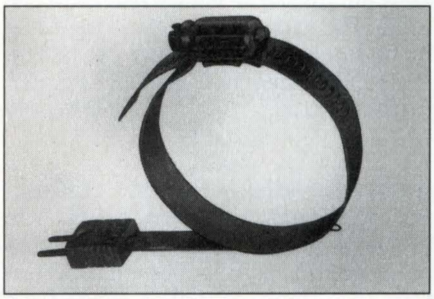
The board achieves its performance via the company's ISP1020 SCSI coprocessor that has dual on-chip processors. One processor controls SCSI-bus protocol; the other, a 16-bit RISC processor, handles data flow and related commands. The board is ASPI- and CorelSCSI-compatible and is available with drivers for DOS, Windows, Windows NT, NetWare, SCO Unix, and OS/2. $289 (1); <$200 (OEM).

—Gary Legg

QLogic Corp, Costa Mesa, CA. (714) 438-2200. **Circle No. 370**

COMPONENTS

Protected quad high-side MOSFET driver operates from 8 to 60V. The LT1161 quad MOSFET driver has four ruggedized n-Channel MOSFETs that have a 100% voltage margin in 24 and 28V systems. Each switch sports an internal charge pump, obviating external components to boost the MOSFET's gate 12V above the supply rail. Each channel has overcurrent protection and an internal reset timer. The device's current limit, delay time, and automatic restart period are externally programmable. \$3.15 to \$2.44. **Linear Technology Corp**, Milpitas, CA. (408) 432-1900. **Circle No. 439**



Thermocouple clamps directly around hot pipe. The stainless-steel Pipe Clamp Sensor fits pipe diameters from 1 to 6 in. The sensor accepts common thermocouples that measure temperatures up to 1500°F. A connector allows you to leave the sensor in place between measurements. \$25. **Electronic Development Labs Inc**, Danville, VA. (800) 342-5335. **Circle No. 440**

Silvered-mica snubbers quash 100,000V/μsec transients. The Snubber Mike line of silvered-mica capacitors handle 3.7-kA peak currents and 8.7A steady state. These units exhibit unmeasurable changes in capacitance over frequency and temperature and withstand millions of "shots" without degrading. Capacitances range from 100 pF to 0.01 μF, and voltages range from 500 to 1.5 kV dc. \$0.15. **Cornell Dublier**, New Bedford, MA. (508) 996-8564. **Circle No. 441**

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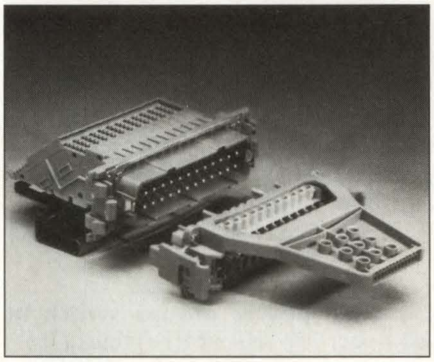
Ultrafast power diodes switch in 30 nsec. The HiPerFRED line of fast-recovery epitaxial diodes (FREDs) offers a 30-nsec switching speed and guaranteed avalanche-power rating of 13 kW. These 1-kV devices exhibit 20-μA leakage. The devices' soft-recovery factor is 1. These diodes combine elements of Schottky and PIN-diode construction. \$4.14 (1000). **IXYS Co**, Santa Clara, CA. (408) 962-0670. **Circle No. 442**

Superflexible coaxial cables bend around 1-in. radius. Three ⅜-in., 50Ω coaxial cables can carry high power around tight bends without losing their specified characteristic impedance. The jacketed ETS2-50T cable and unjacketed

ETS2-50 cable can carry over 1.15 kW at 1 GHz. The attenuation of the two is 4.24 dB/100 ft. Type FSJ2-50 has an attenuation of 4.09 dB/100 ft and can carry 0.452 kW at 1 GHz. The cables require a special N connector ($35). FSJ2-50 $2.64/ft, ETS2-50T $11.14/ft. **Andrew Corp**, Orland Park, IL. (708) 349-3300. **Circle No. 443**

Field wiring unplugs from connector block. Rail-mounted, multipole connector blocks combine a multipin, polarized connector with a terminal block. The blocks mount on TS32 and TS35 DIN rails and are certified to ISO 9001. Available versions accept screw terminals or crimps and can carry as much as 16A at 600V. Blocks feature 6, 10, 16, 24, 40, or 64 pins. $17 to $75. **Wieland Inc**, Burgaw, NC. (919) 259-5050. **Circle No. 444**



Dual, common-mode choke helps token-ring boards meet FCC EMI requirements. The PE-67539 (surface-mount) and PE-65740 (through-hole) dual, common-mode chokes provide –40-dB performance from 5 to 200 MHz. The chokes help token-ring LAN pc boards meet EMI specs. $2 (1000). **Pulse Engineering**, San Diego, CA. (619) 674-8100. **Circle No. 445**

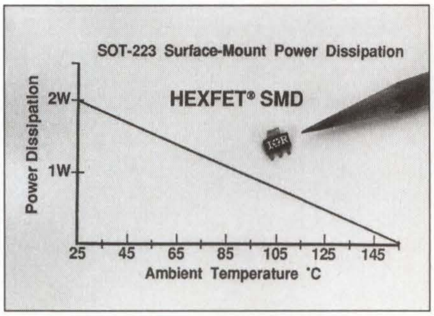
Insulation-displacement connector features 2×2-mm pitch. The TCMD series of double-row connectors have 0.020-in. square, phosphor-bronze pins. The units' capacities range from two to 25 positions per row. Notch and position polarization are available. A resulting cable assembly is 0.20 in. tall and mates with the company's surface-mount and through-hole connectors. $0.06/pin (1000); delivery, five days ARO. **Samtec Inc**, New Albany, IN. (312) 944-6733. **Circle No. 446**

Trimming capacitor has axial leads. The 10-pF, half-turn RD10 trimming capacitor measures 0.14 in. in diameter and is 0.06 in. tall. Its dc working voltage is 25V, and its withstand voltage is 50V dc. The unit's Q at 1 MHz is 400, and its temperature coefficient is –50±100 ppm/°C. $0.24 (100,000), delivery stock to five weeks. Sample kits available. **Voltronics International Corp**, Denville, NJ. (201) 586-8585. **Circle No. 447**

Sockets shrink spacing to 0.70 in. A series of 0.070-in. pin-to-pin, shrink-DIP sockets suit lower cost, less-demanding applications. The sockets housings are UL94V-O glass-filled thermoplastic. Contact pins are tin-plated phosphor bronze. The sockets are available with 16, 22, or 24 pins on 0.300-in. centers; 24, 28, or 30 pins on 0.400-in. centers; 40 or 42 pins on 0.600-in. centers; and 64 pins on 0.700-in. centers. The 64-pin socket costs $0.40 (5000), delivery stock to six weeks ARO. **Aries Electronics Inc**, Frenchtown, NJ. (908) 996-6841. **Circle No. 448**

EDN-NEW PRODUCTS

COMPONENTS



Surface-mount package dissipates 1W optimally. The SOT-223 surface-mount package occupies 30% less pc-board space and is 30% lower in height than other 1W packages. The package resembles a standard SOT package but has an enlarged drain connection. The company supplies power FETs in the SOT-223 package. The package lowers device prices by 10% compared with other packages. **International Rectifier**, El Segundo, CA. (315) 322-3331. **Circle No. 449**

Resistor network surface mounts. The Narrow Body Resistor Network model 4900P measures 0.150 in. wide. The surface-mount devices come in 8-, 14-, and 16-pin models. Both bused and isolated resistors are available. $0.20. **Bournes Inc**, Riverside, CA. (909) 781-5140. **Circle No. 450**

Snubber circuit's porcelain-on-steel substrate dissipates substantial heat. Using an enameled-steel substrate, a snubber circuit dissipates 5W at 25°C (linearly derated to 0W at 105°C). Snubbers with chip capacitors can withstand 50V pk; units are available with disk capacitors having a 1000V-pk withstand voltage. (Plain power resistors made with the same porcelain-enamel-on-steel substrate are also available in 10, 15, 20, 50, and 100W ratings.) Snubber: $0.47 (1000), delivery 10 to 12 weeks ARO. **Ohmite,** Skokie, IL. (708) 675-2600. **Circle No. 451**

Low-cost 40-MHz converter draws 80 mW. The model HI1171 40-MHz D/A converter's differential nonlinearity is 0.25 LSB, and integral nonlinearity is 1.3 LSB max. The device decodes and latches inputs before converting them. Glitch energy measures 30 pVsec. Differential gain and phase noise are 1.2 and 0.2% typ, respectively. $3.86 in a 24-pin SOIC (1000). **Harris Semiconductor**, Melbourne, FL. (800) 427-7747, ext 7138. **Circle No. 452**

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Module and bus bring 320-Mbyte/sec I/O to VME

SkyChannel bus architecture allows numerous processors to share access to system resources at data rates as fast as 320 Mbytes/sec. To maximize bus utilization, the synchronous 64-bit bus uses centrally arbitrated packetized data transfers with buffering at each end. This architecture has been proposed to VITA as an open standard.

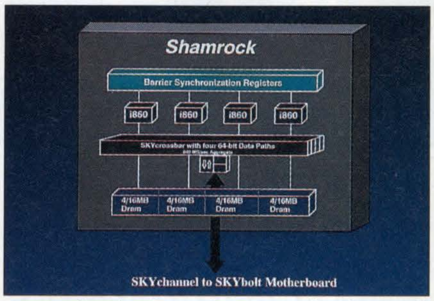
Designed for multiprocessing applications, SkyChannel bus allows as many as 4096 processors to be interconnected. Each processor accesses memory and other system resources as part of a 16-Tbyte address space. Thus, the processors can share all memory, which simplifies data exchange. The bus can be used within a board, between boards, or between card cages. Multiple SkyChannels run in parallel with a crossbar switch between, which allows them to offer multiple independent paths between processor and resource when there are many resources to share.

Data traveling along the bus moves between units called Functional Modules in packets as large as 256 words, which are headed by a destination address. Each Functional Module uses FIFO buffering in both its input and output ports so that data transfers can occur at the maximum bus speed. A central arbiter controls access to the bus, granting Functional Modules use of the bus as requested.

Modules have three types of transfer: write, read, and compare and switch. The read and compare transfers use a split operation to reduce bus utilization. Both call for the reading module to provide a destination address to the module being read. The responding module then sends the requested data after it's queued in the FIFO.

A variety of SkyChannel products are available from the bus designers, including a multiprocessor VME card, a backplane bridge for VME systems, a complete VME system with SkyChannel embedded, and a stand-alone processing unit with SCSI interface. Each uses the Shamrock II compute daughter card as its basis.

The Shamrock II offers four i860 processors and 128 Mbytes of DRAM connected by a 4-channel bus with crossbar switch. A link to external SkyChannel buses is one of the card's



Key to the SkyChannel system, the Shamrock II card uses the channel to connect four i860 processors to each other and off board.

resources. The Skybolt II 6U VME card accepts one Shamrock daughter card and links the SkyChannel bus to the VME backplane's P2 connector. The 9U card accepts four daughter cards.

At the system level, the SkyStation II holds two daughter cards and provides them with 512 Mbytes of bulk memory, high-speed parallel I/O, and a SCSI-2 port. The SCSI-2 port links the SkyStation to a host processor, allowing the unit to function as a computation accelerator. Another system product, the SkySystem, is a 500W VME64 chassis with SkyBolt boards, tape, disk, and CD-ROM drives, color monitor, keyboard, and software tools. For designers building their own systems, the SkyBridge interconnect plugs onto the P2 connectors to provide a 4-channel bus between boards.

SkyChannel is supported by software tools that simplify multiprocessor computing. The compilers accept C, Fortran, and Ada code and automatically partition tasks among as many as four processors.

The Skybolt II 6U card and SkyStation II system are available now; each costs $20,000. The SkyBridge, Skybolt II 9U cards, and SkySystem products will be available by the second quarter of 1994. The systems will cost $30 to $50k, depending on configuration. The SkyBridge interconnect will cost approximately $600/board.—**Richard A Quinnell**

Sky Computers Inc, Chelmsford, MA. (508) 250-1920. **Circle No. 372**

BOARDS & BUSES

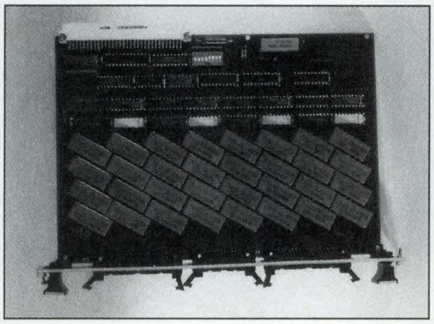
Module provides controlled power-up sequence. The Power Sequencing Module (PSM) staggers the turn-on and -off of supply voltages to the Futurebus+ backplane. PSM offers four voltage rails: 2.1, 3.3, 5, and 48V. The module connects in parallel with the ac's power input lines and the power supply. $150. **Bicc-Vero Electronics Inc,** Hamden, CT. (800) 242-2863.
Circle No. 353

STD computer supplies extensive I/O. The ZT 8802 is a V40-based STD-32 computer module that runs DOS software. In addition to the standard DOS serial port, the board offers two more RS-232C serial ports and 48 bidirectional digital I/O lines. The board also includes 1 Mbyte of RAM and 512 kbytes of ROM. An SBX expansion bus makes the module customizable. $450. **Ziatech,** San Luis Obispo, CA. (805) 541-0488. **Circle No. 354**

Automation controller handles industrial environments. Based on the 8086 processor, Hench Control automation controllers incorporate optical isolation, filtered power, and analog I/O filtering to withstand the rigors of the industrial environment. The modules are C-programmable and available as 11×7-in. boards or in NEMA-4 enclosures and offer 64 digital and 48 analog I/O channels. From $3500 (unprogrammed). **Hench Control Corp,** San Jose, CA. (408) 296-4600.
Circle No. 355

Quad processor meets military needs. The DMV-442 incorporates four 320C40 DSP devices—each with 4 Mbytes of RAM—onto a 6U VME board. The board makes four of the processors' 20-Mbyte/sec communications ports available on the backplane, offers a mailbox interrupt mechanism, and has an optional 500-Mbyte/sec I/O bus. The board is available in commercial, extended-temperature, and military-ruggedness configurations. From $12,895. **Dy 4 Systems Inc,** Campbell, CA. (408) 377-9822. **Circle No. 356**

VME board provides 32 analog output channels. The MPV914 is a 6U slave VME board with as many as 32 channels of 12-bit DAC analog signals. The range for each signal is individually controllable and can be set for ±10, ±5, 0 to 10, or 0 to 5V output. The digital codes can be binary, offset binary, or 2's-complement. From $4495. **Pentland Systems Ltd,** Danville, CA. (510) 736-5113. **Circle No. 357**



VME modules offer switching options. The VM series switch modules offer multiplexer, matrix, and discrete relay configurations in a 6U VME or B-size VXI board. The modules come with standard, mercury-wetted, or low-thermal relays and can be configured to handle as much as 8A. The coaxial relay matrix handles signals to 200 MHz. $500 to $1800. **Cytec Corp,** Penfield, NY. (716) 381-4740. **Circle No. 358**

386 processor module fits small spaces. The ESP 386SLV/486SLC module uses double-sided component placement to achieve minimum size while retaining full PC compatibility. It uses the VLSI Scamp chip set and the VL82C323 power-management chip to give software control of power usage. The board includes standard AT keyboard control, BIOS on boot-block flash EEPROM, and a coprocessor socket. $302 (100). **Dovatron International,** Longmont, CO. (303) 772-5933.
Circle No. 359

GPIB controllers mate with a variety of PCs. Expanding beyond ISA-based machines, this GPIB controller family offers a variety of interfaces. The GPIB-232CT-A ($495) is an RS232C-to-GPIB controller board that allows any serial port to become an IEEE-488.2 controller. The GPIB-ENET/Mac board ($1095) connects Macintosh computers to the IEEE-488 bus via Ethernet. The TC-GPIB/OSF board kit ($895) connects to DEC Alpha workstations. **National Semiconductor,** Austin, TX. (512) 794-0100. **Circle No. 360**

Board suits small industrial control. The Puce board measures 250×140×44 mm and includes a 16-key keypad and a 2-line 16-character alphanumeric display. The eight digital-input, eight output, and eight analog lines are all power-surge protected. The board also offers an extension connector and a built-in beeper for audio alarms. **LEAS,** Grenoble, France. (33) 76 52 13 30.
Circle No. 361

VME64 board utilizes RISC processor. The HK80/V960D is based on a 30-MHz 80960CF processor with a 4-kbyte instruction and 1-kbyte data cache. The board also provides as much as 16 Mbytes of DRAM, 4 Mbytes of flash EEPROM, and sockets for 512 kbytes of ROM. Four serial ports, an Ethernet interface, a VME64 interface, and a 200-Mbyte/sec expansion bus handle board I/O needs. From $4495. **Heurikon Corp,** Madison, WI. (608) 831-0900. **Circle No. 362**

VME board accepts four PCMCIA cards. The RM230 6U VME card accepts as many as four PCMCIA cards carrying I/O or as much as 256 Mbytes of memory. The board accepts the cards as two independent blocks—each block containing two cards. Memory and I/O cards are each address-selectable on 64-kbyte boundaries. $580. **RAMix Inc,** Chatsworth, CA. (818) 349-6772.
Circle No. 363

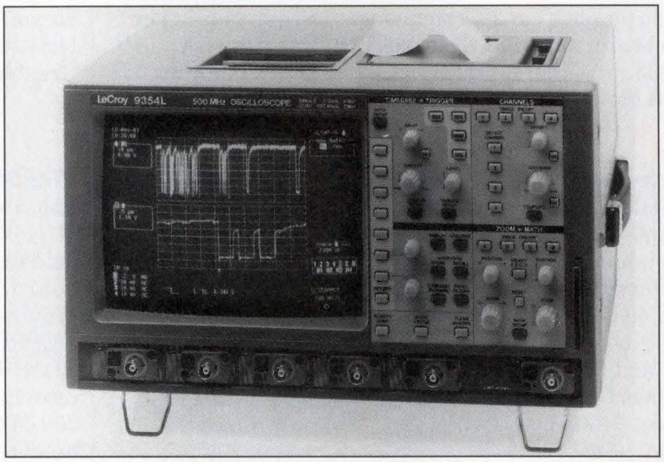
SHORTS & REVISIONS

Beta Transformer Technology Corp now offers an application note on transformers for the MIL-STD-1553 data bus. (516) 567-5600, ext 7794. **Circle No. 364**

The Model 467-1 Sbus-to-VMEbus adapter from Bit 3 Computer Corp now includes a slave DMA mode that handles sustained data transfer rates to 12 Mbytes/sec.
Circle No. 365

Texas Instruments has developed a low-cost version of its MVME162 embedded computer: the MVME-162LX. The $1095 LX provides front-panel I/O access and error-correcting memory. **Circle No. 366**

Portable 500-MHz DSO stores 8M words in real time at 2G samples/sec



The resemblance of LeCroy's 9354L to the company's other portable DSOs is striking, but the unit offers memory unmatched by any other wideband, portable DSO. The amber-phosphor CRT is bigger than some competitors', and the optional thermal printer can, in effect, give you a CRT many yards wide.

For reasons detailed in **Ref 1**, a real-time-sampling capability is a big deal in DSOs, and in real-time-sampling DSOs, deep memory is an even bigger deal. That explains the continuing increases in the memory depth of wideband DSOs whose real-time sampling rate is four or five times their –3-dB bandwidth. LeCroy Corp leads the industry in wideband DSOs that provide deep memory, but until now, the company has not had a real-time portable scope with 500-MHz bandwidth.

Now LeCroy has a family of six such scopes, the 9350 series. The top-of-the-line 9354L ($24,490) offers an 8M-sample memory. Other portable scopes that acquire 500-MHz signals at 4 samples/cycle offer less than 1% of that memory depth.

The 9350 series' versatility should win it the nickname of "the Swiss army knife" of DSOs. (Coincidentally, LeCroy manufactures its portable DSOs in Switzerland.) The 9354L achieves its 8M-sample memory depth and 2G-sample/sec acquisition speed when you use one channel. In this mode, it interleaves all four channels' 500M-sample/sec ADCs and 2M-sample memories. Although interleaving ADCs to achieve faster sampling is fairly common, only a few wideband scopes—none of them portable—interleave capture memory. Both time and numbers of stored samples are important in this case; failure to interleave memory reduces the captured signal's maximum duration.

The 9354L's long memory lets you capture 4 msec of data at 2G samples/sec. You can acquire signals at 2G samples/sec at sweep speeds as low as 400 μsec/div. Under these conditions, even signals that contain 1-GHz components of significant amplitude do not cause aliasing. Moreover, you can zoom in on very short slices of the long records and view them at high sweep speeds without reacquiring the data. Unlike some competitive units, the LeCroy scopes can simultaneously display the full signal and several expanded segments.

Some scopes with shorter memories offer a glitch-capture feature that, even at low sweep speeds, guarantees capturing narrow pulses. Glitch capture saves memory by processing the waveform data before it is stored. A scope with glitch capture tells you only roughly when a glitch occurs; all it says about the glitch width is that it didn't exceed some maximum. Even at fairly low sweep speeds, a scope with deep enough memory digitizes at its maximum rate and stores every acquired point. Unlike glitch capture, deep memory preserves all information about narrow glitches and portrays them more accurately.

One reason for the Swiss-army-knife label is that all of the 9350 units do both random equivalent-time sampling (useful with repetitive signals) and real-time sampling (useful with repetitive and 1-shot signals). The presence of this dual-mode capability pits the 9354 ($13,990, 25k samples/channel, 100k-sample memory in 1-channel mode) and the 9354M ($16,490, 100k samples/channel, 500k samples in 1-channel mode) against Tektronix's top-selling TDS 2540A ($16,290 with optional 50k-sample/channel memory) and Hewlett-Packard's recently introduced 54540A ($15,000, 32k samples/channel). In real-time mode, these HP and Tek units take 1G samples/sec on one channel, whereas the 9354, 9354M, and 9354L take 2G samples/sec on one channel.

Both HP and Tek offer portable DSOs that capture 2G samples/sec on up to four channels at once. HP's units store 32k samples/channel; Tek's store 2k samples/channel. Pricing of these real-time DSOs is roughly one-third greater than that of the other HP and Tek scopes mentioned here.

Besides the 4-channel models, the 9350 series includes three 2-channel units. Their prices begin at $9490. For $590 more, you can equip the LeCroy scopes with a floppy-disk drive; for $500, you can add a PCMCIA slot. A drive is standard on some competitive products, but the memory-card slot is not available. For $890 extra, LeCroy equips its portable scopes with a thermal plotter, which does screen dumps and writes long records in uncompressed form. In effect, these records give you a "CRT" many yards wide. Tek offers a printer that you can attach to the top of its TDS scopes; the HP scopes use separate printers. FET probes for the LeCroy scopes cost $990 each.

—Dan Strassberg

LeCroy Corp, Chestnut Ridge, NY. (800) 553-2769. **Circle No. 468**

Hewlett-Packard Co, Santa Clara, CA. (800) 452-4844. **Circle No. 469**

Tektronix Inc, Beaverton, OR. (800) 426-2200. **Circle No. 470**

Reference

Strassberg, Dan, "Fast single-shot DSOs take varied design approaches," *EDN*, July 8, 1993, pg 47.

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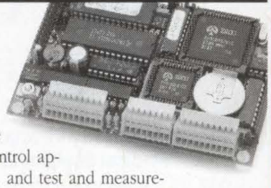

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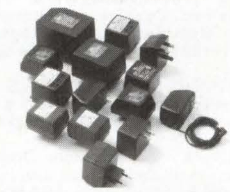

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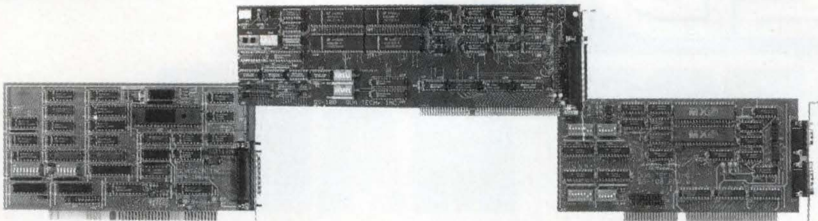

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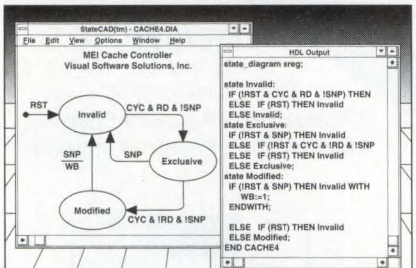

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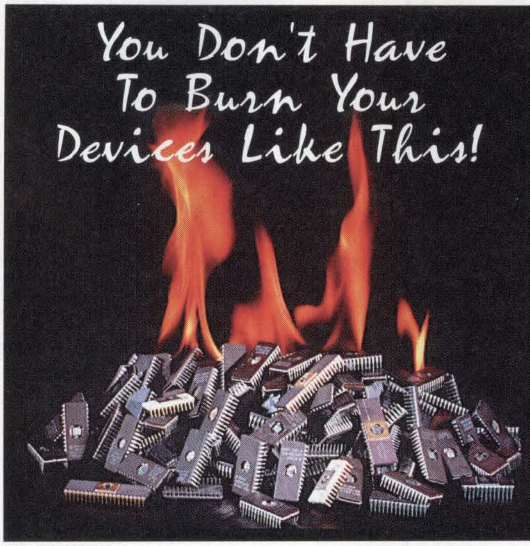

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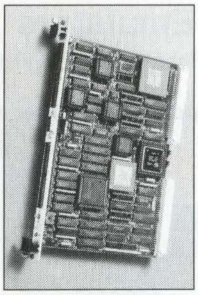

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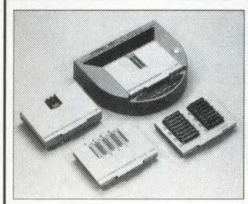

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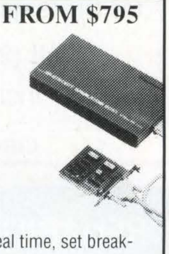

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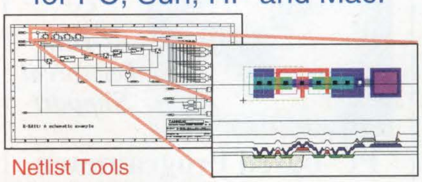

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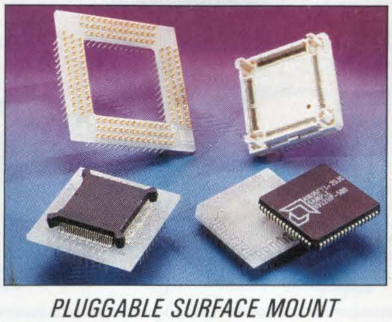

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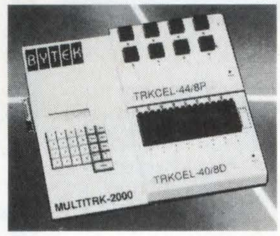

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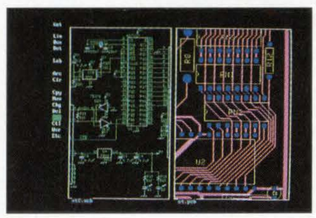

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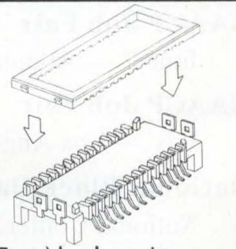

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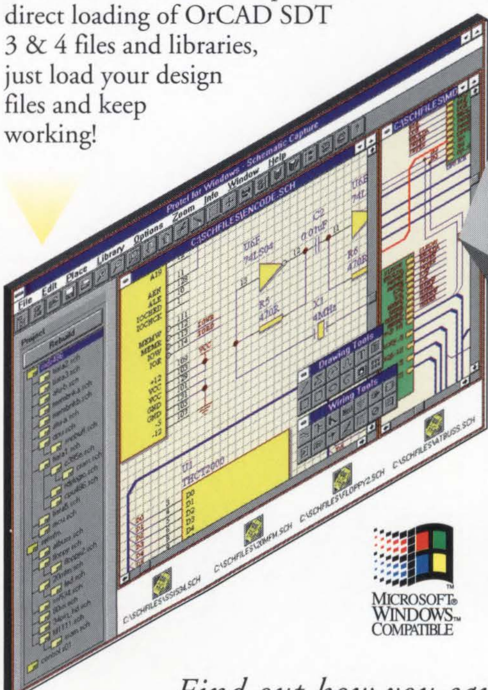

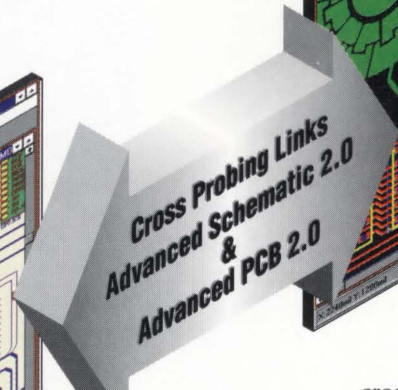

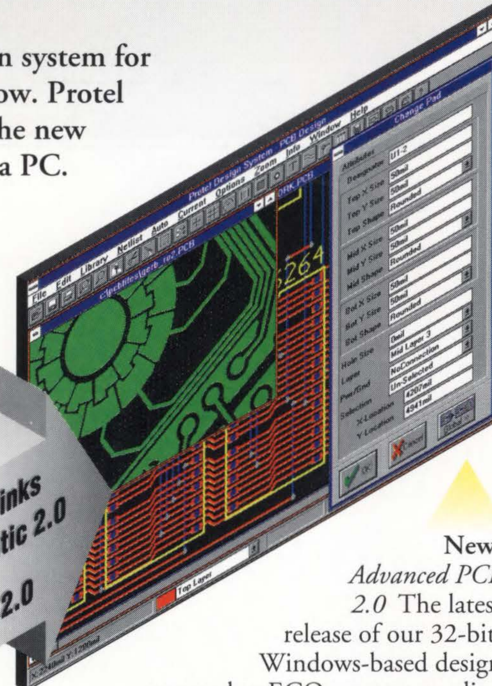

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