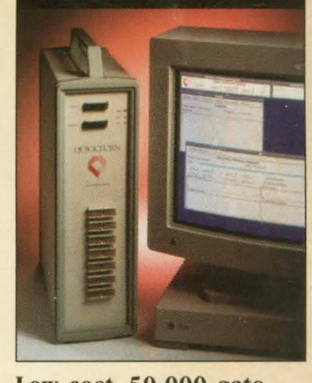
May 26, 1994

EDN®

THE DESIGN MAGAZINE OF THE ELECTRONICS INDUSTRY

NEW PRODUCT INTRO



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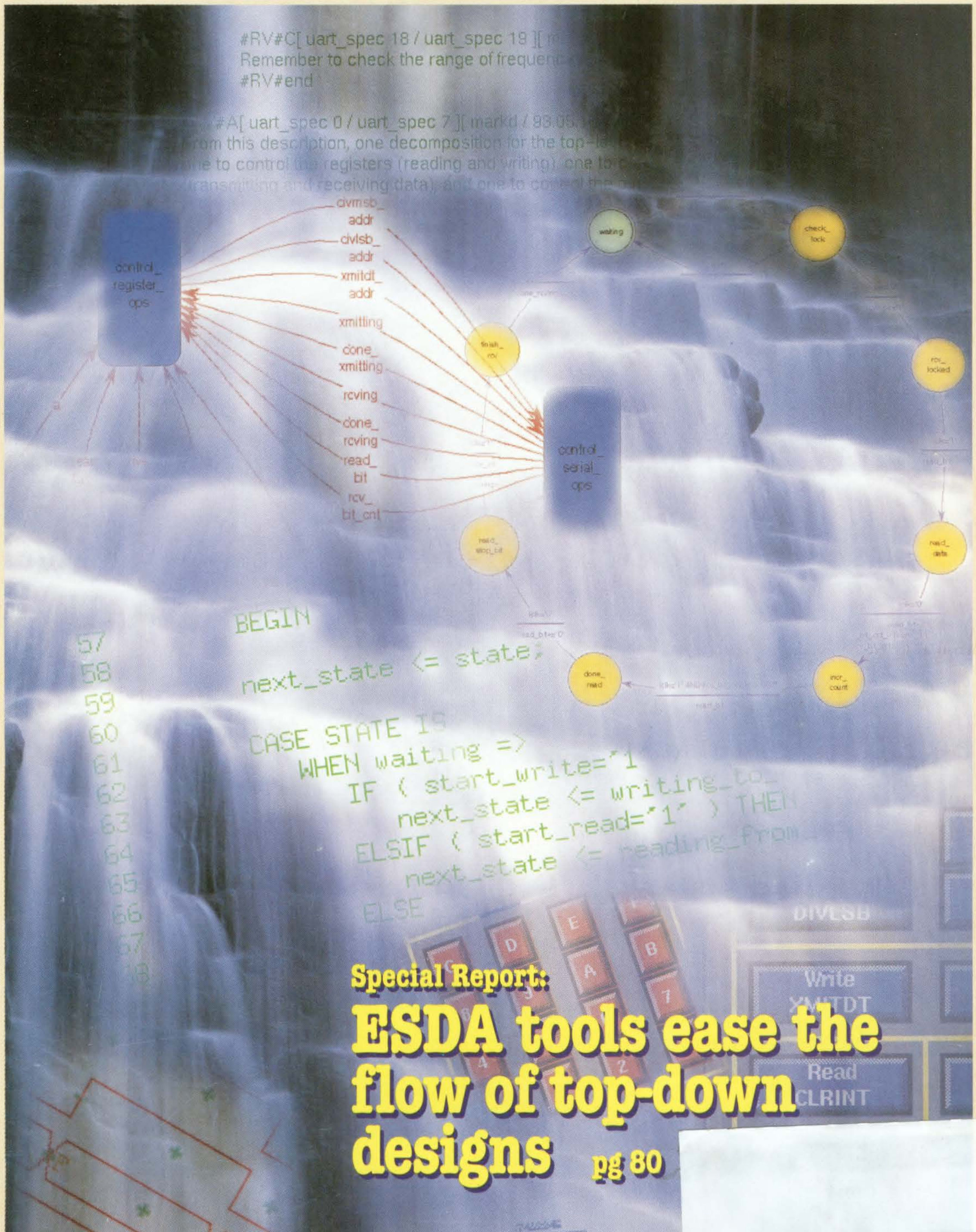

Special Report:

ESDA tools ease the flow of top-down designs

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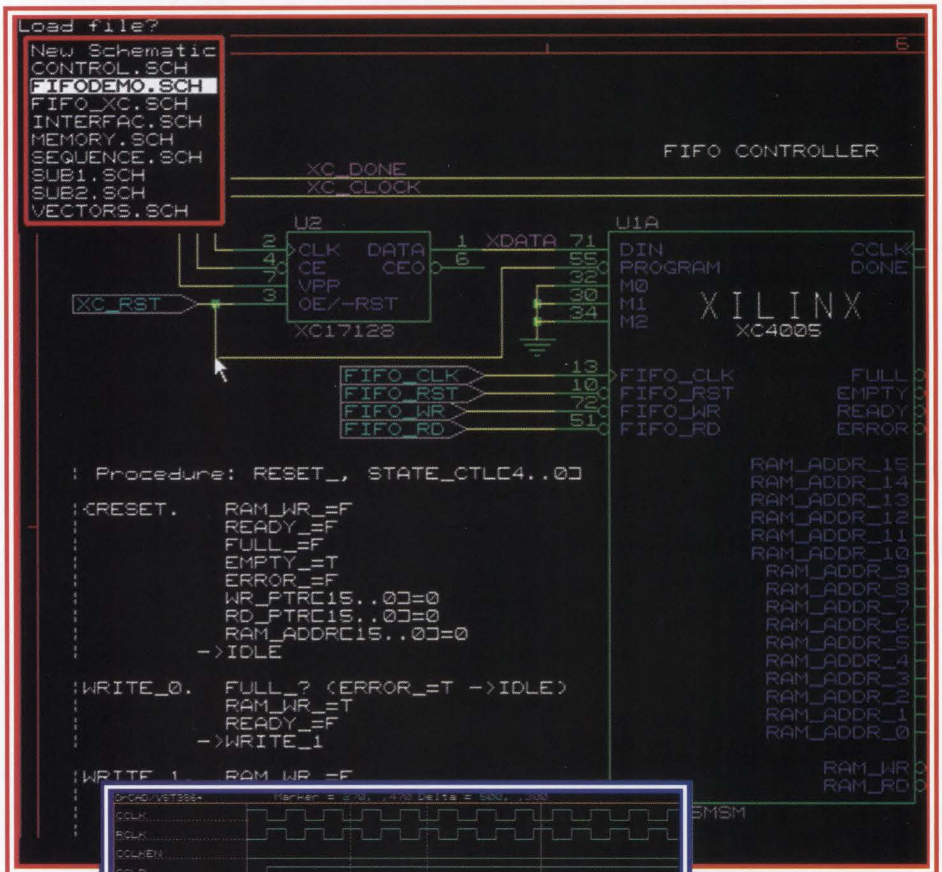

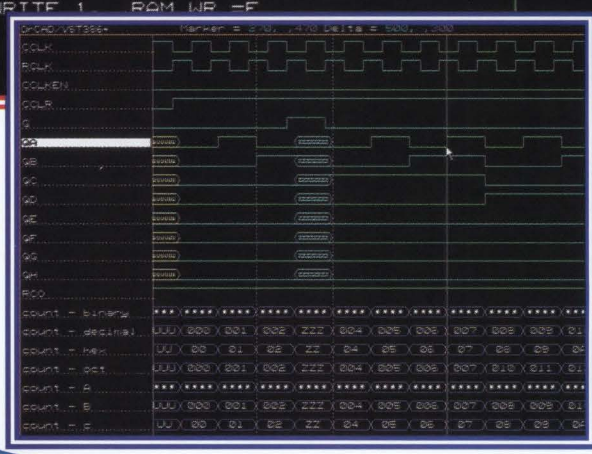

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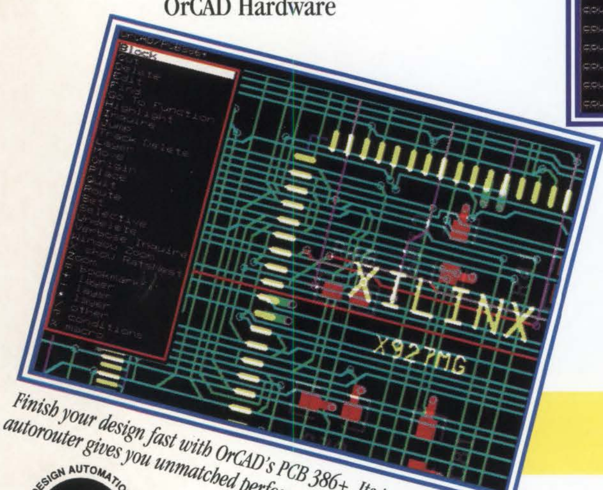

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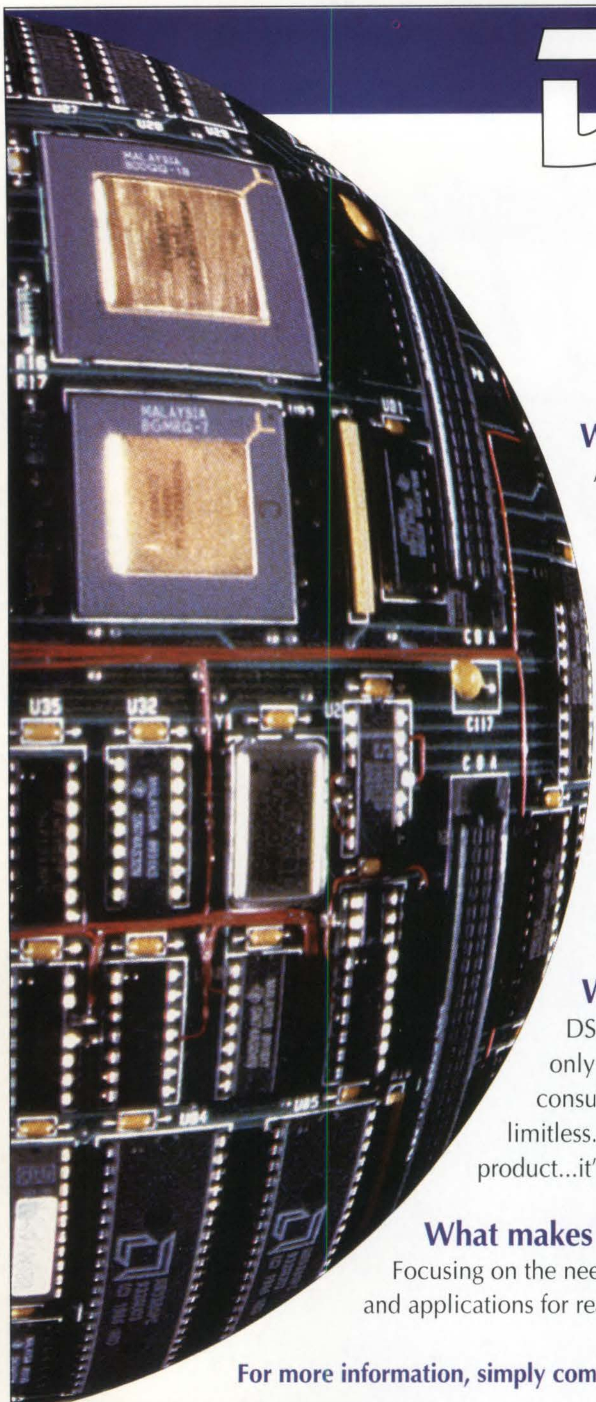

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CIRCLE NO. 38

EDN

May 26, 1994 VOLUME 39, NUMBER 11

THE DESIGN MAGAZINE OF THE ELECTRONICS INDUSTRY

On the cover: The top-down approach to system design is clean and logical. A new group of tools—electronic system design automation tools—supports this widely used design approach. See our Special Report, beginning on **pg 80.** (Photo courtesy Mentor Graphics)

SPECIAL REPORT

DESIGN FEATURES

DESIGN IDEAS

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EDN® (ISSN 0012-7515, GST Reg. #123397457, IPM #0280844) is published 38 times per year, bi-weekly with one additional issue per month, by Cahners Publishing Company, A Division of Reed Publishing USA, 275 Washington Street, Newton, MA 02158- 1630. Robert L. Krakoff, Chairman and Chief Executive Officer; Timothy C. O'Brien, Executive Vice President/Finance and Administration; Michael Wisner, Senior Vice President/General Manager, Boston Division; Michael Wisner, Vice President/Publishing Director. Circulation records are maintained at Cahners Publishing Company, 8773 South Ridgeline Blvd., Highlands Ranch, CO 80126-2329. Telephone (303) 470-4445. Second-class postage paid at Highlands Ranch, CO 80126-2329 and additional mailing offices. **POSTMASTER: Send address changes to EDN®, PO Box 7500, Highlands Ranch, CO 80126-7500.** EDN® copyright 1994 by Reed Publishing USA. Rates for non-qualified subscriptions, including all issues: US, $140.00 one year, $238.00 two year; Canada, $209.00 one year, $355.00 two year (includes 7% GST, GST# 123397457); Mexico, $195.00 one year, $332.00 two year; Foreign surface $245.00 one year, $417.00 two year; Foreign air expedited surcharge add $152.00 one year, $304.00 two year. Except for special issues where price changes are indicated, single copies are available for $10.00 US and $15.00 foreign. Please address all subscription mail to EDN®, 8773 South Ridgeline Blvd., Highlands Ranch, CO 80126-2329. EDN® is a registered trademark of Reed Properties Inc., used under license.

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Microchip PIC16/17 Microcontrollers

DEVICE	PINS	I/O	MEMORY PROGRAM	MEMORY USER RAM
PIC16C54	18	12	512 x 12 (OTP)	25 x 8
PIC16CR54	18	12	512 x 12 (ROM)	25 x 8
PIC16C54A	18	12	512 x 12 (OTP)	25 x 8
PIC16C55	28	20	512 x 12 (OTP)	24 x 8
PIC16C56	18	12	1024 x 12 (OTP)	25 x 8
PIC16C57	28	20	2048 x 12 (OTP)	72 x 8
PIC16CR57A	28	20	2048 x 12 (ROM)	72 x 8
PIC16C58A	18	12	2048 x 12 (OTP)	73 x 8
PIC16C64*	40/44	33	2048 x 14 (OTP)	128 x 8
PIC16C71(A/D)*	18	13	1024 x 14 (OTP)	36 x 8
PIC16C84*	18	13	1024 x 14 (EEPROM)	36 x 8
PIC17C42	40/44	33	2048 x 16 (OTP)	256 x 8

*These products will be the focus of this seminar series.

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CIRCLE NO. 33

Home Office
275 Washington St, Newton, MA 02158
EDN Bulletin Board: (617) 558-4241
MCI: EDNBOS
Phone (617) 558-plus 4-digit extension below
Fax (617) 558-4470
To send a message to an EDN editor via Internet, add "@MCIMAIL.COM" to his or her MCI address.

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Norwich, NR14 6DR, UK
(508) 528435; fax (508) 528430
MCI: EDNKERRIDGE
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EDN Asia, Mike Markowitz, *Editor*
Cahners Asia Ltd
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EDN Products
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May 26, 1994

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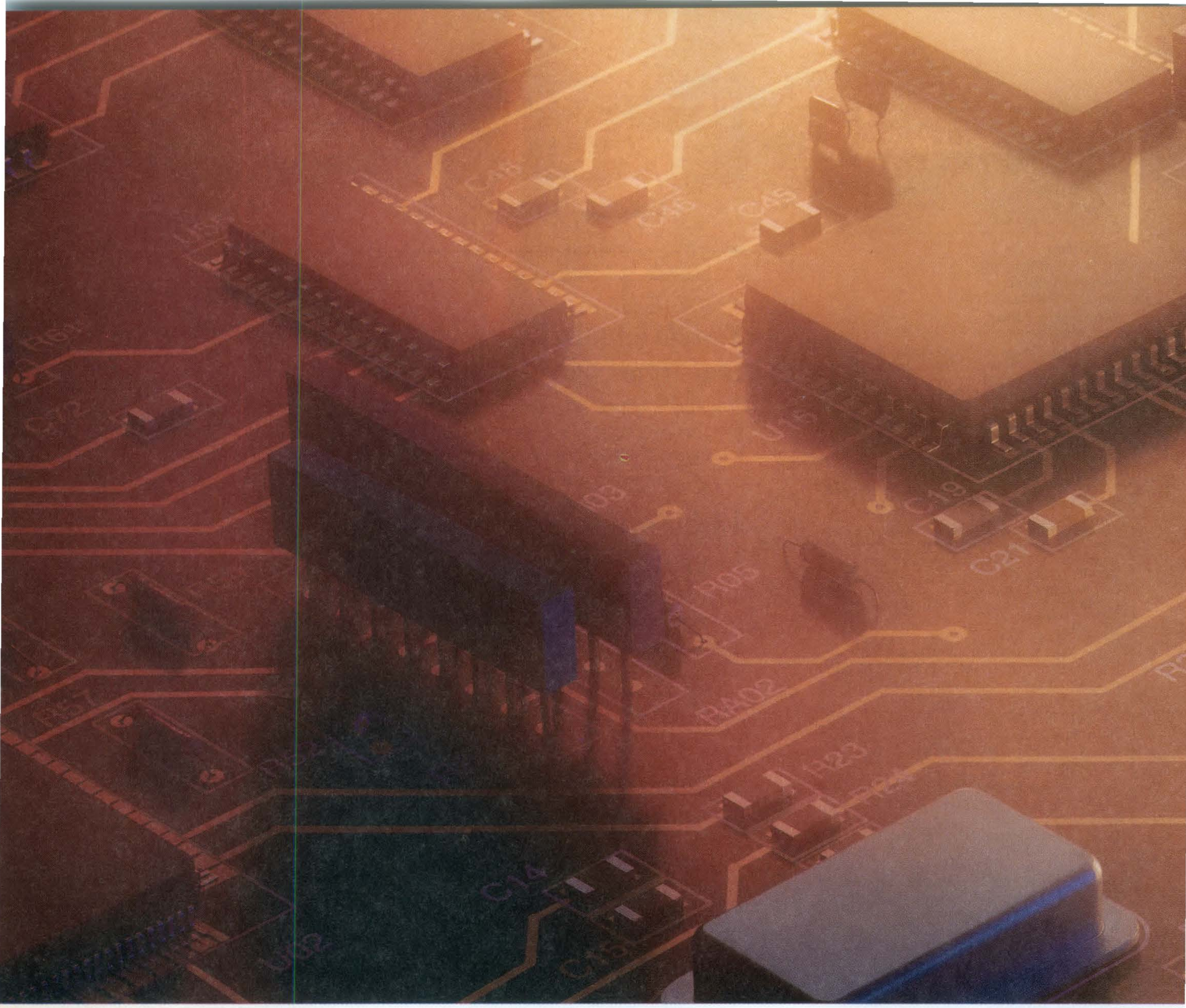

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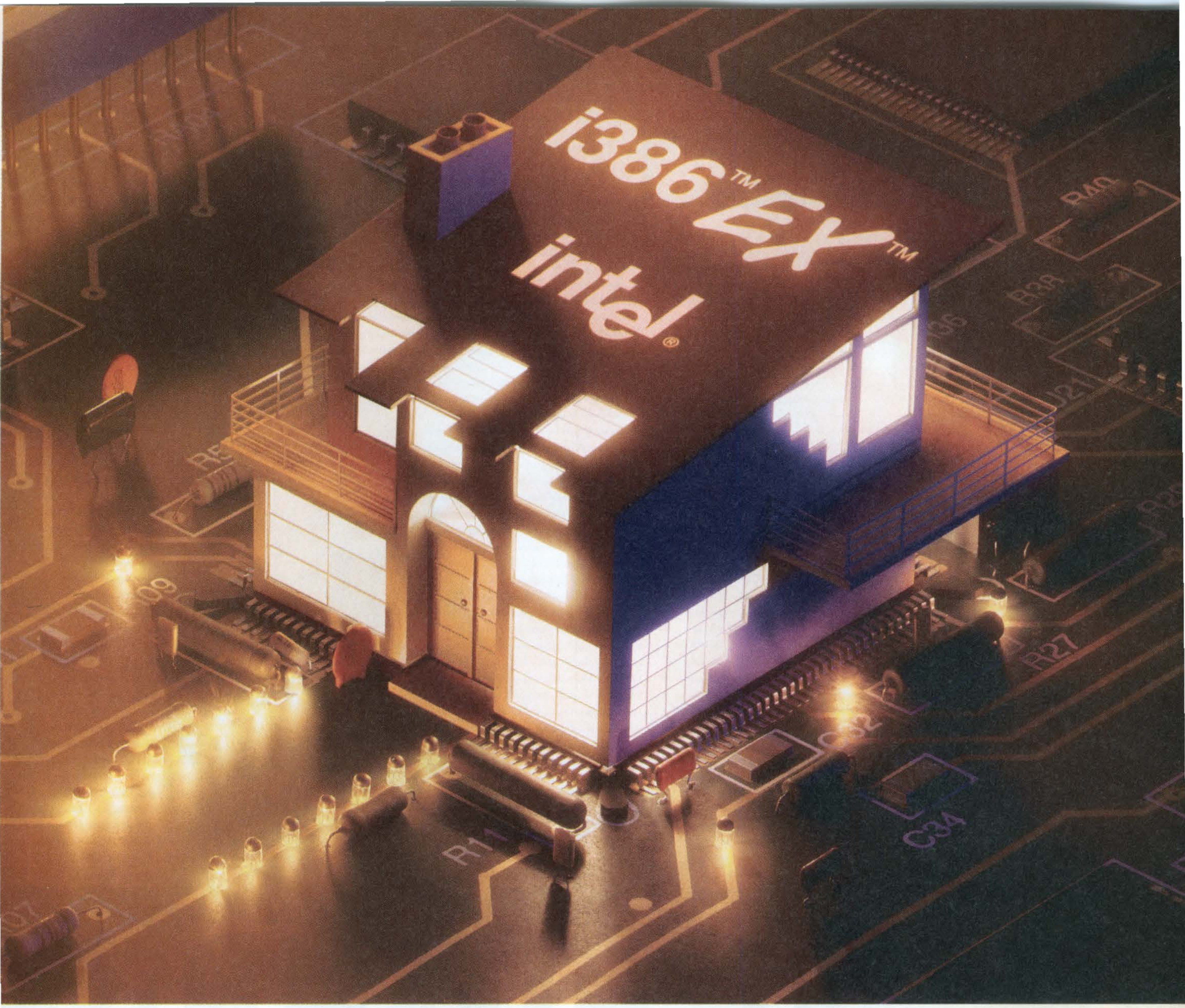

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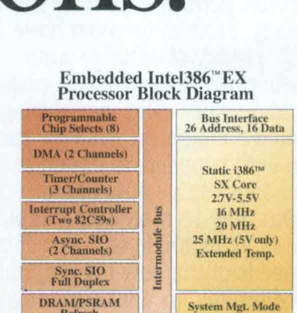
Embedded Intel386™ EX Processor Block Diagram



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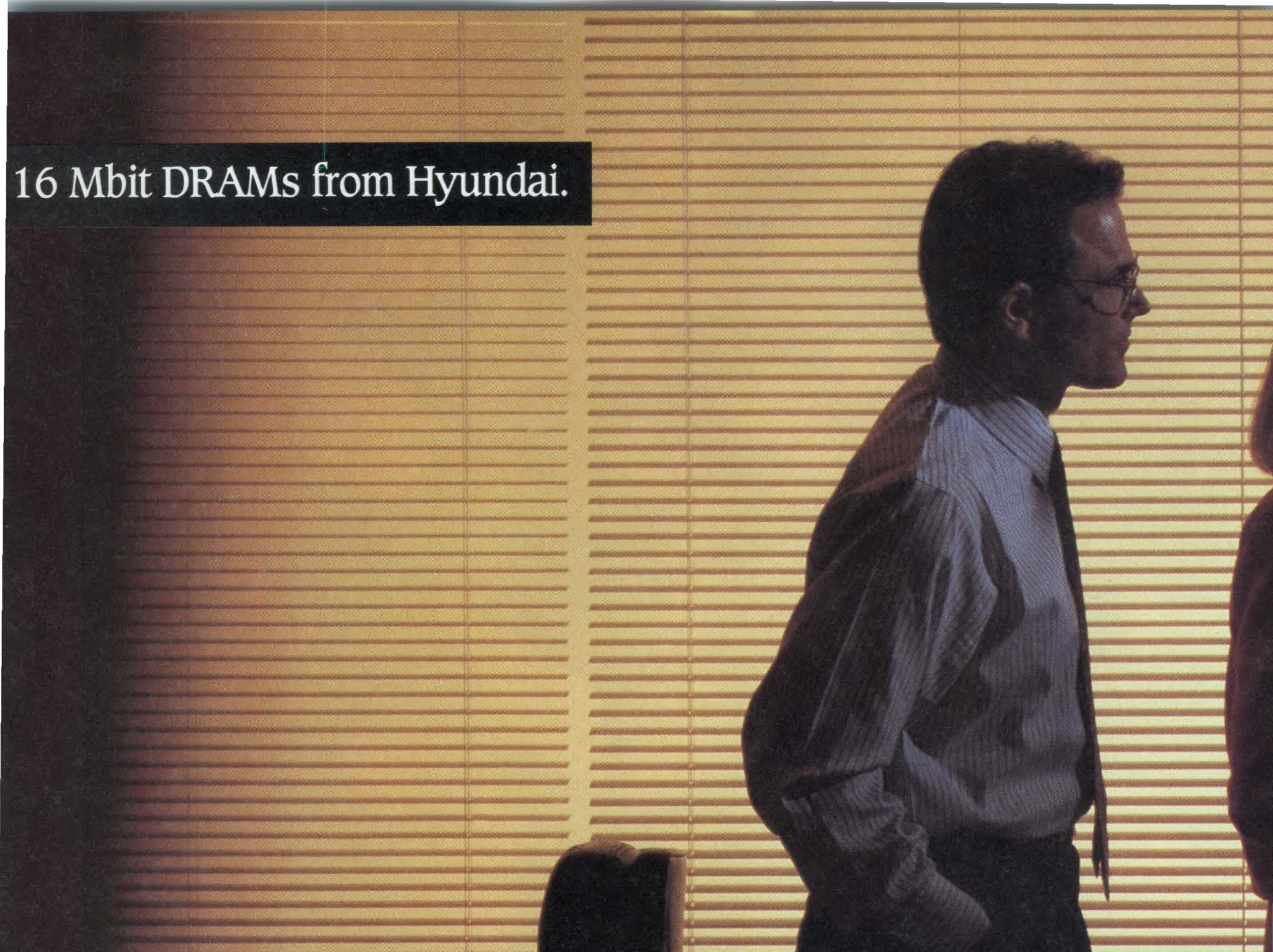
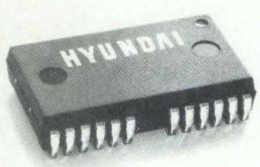
16 Mbit DRAMs from Hyundai.



Team Dy



Sourcing used to be simple. The buyer and the design engineer got together for a few minutes. And that was it.

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Now, virtually all of the make or break purchases for DRAMs and other major ICs in companies with over $10M in sales* are the result of a cross-functional team dynamic. And remember, no company has a bigger commitment to team dynamics than Hyundai.

Hyundai knows the engineer needs better performance from the technology. Production must have qualified, readily obtainable parts. Purchasing has to get the best possible price and delivery. And management must build a long term strategic partnership with suppliers to obtain a superior competitive advantage.

Our new 16 Mbit dynamic RAMs are one more example of our dedication to the needs of the new team dynamic. We're committed to your success and the success of your cross-functional buying team through Hyundai's commitment to quality, reliability, manufacturing capability and value added pricing.

Your Hyundai DRAM Source Guide

Size	Part Number	Speed ns	Refresh Cycles/ms	Production
16M x 1	HY5116100	60/70/80	4096/64	now
	HY5117100		2048/32	
4M x 4	HY5116400	60/70/80	4096/64	now
	HY5116410		4096/64, WPB	
	HY5117400		2048/32	
	HY5117410		2048/32, WPB	
2M x 8	HY5116800	70/80	4096/64	Q4 '94
	HY5116810		4096/64, WPB	
	HY5117800		2048/32	
	HY5117810		2048/32, WPB	
1M x 16	HY5116160	70/80	$\overline{2CAS}$, 4096/64	Q4'94
	HY5116260		$\overline{2CAS}$, 4096/64, WPB	
	HY5118160		$\overline{2CAS}$, 1024/16	
	HY5118260		$\overline{2CAS}$, 1024/16, WPB	

All available in standard and low power versions. Packages include SOJ, TSOP II, reverse TSOP II.

namics.

New 16 Mbit DRAMs, designed with team dynamics in mind.

Evaluation samples of Hyundai DRAMs organized 16M x 1, 4M x 4 are available now. Coming soon are DRAMs organized 1M x 16 and 2M x 8. And many will operate off of a 3 volt source too.

Hyundai's new DRAMs feature speeds of 60, 70, or 80 ns. Immediately available, the HY5116100 and HY5117100 are organized 16M x 1 and provide 4096 refresh cycles per 64 ms and 2048 refresh cycles per 32 ms, respectively. New 4M x 4 parts include the HY5116400, with 4096 refresh cycles per 64 ms, the HY5116410 with write-per-bit capability, and the HY5117400 and write-per-bit capable HY5117410 offering 2048 refresh cycles per 32 ms.

All parts are available in standard and low power versions, dissipating 495 mW operating at 60 ns, 440 mW at 70 ns, and 385 mW at 80 ns. Other features include operation from a single 5V ±10% power supply, TTL compatible inputs and outputs, fast page mode operating, multi-bit test capability, read-modify-write capability, and CAS-before-RAS, RAS-only, as well as hidden refresh. Packages include standard 24/28 pin plastic, TSOP II, and reverse TSOP II. TSOP will be available soon.

These new parts are products of Hyundai's 0.55 micron CMOS process, at one of the most advanced electronics manufacturing plants in the world. So if purchase of 16 Mbit DRAMs is on your agenda, and you don't want to get caught short the way some did on 4 Mbit, start the team dynamics now.

Free 1994 16 Mbit DRAM Data Book.

Yours for the asking. Please phone, fax, or write for your copy today. Phone (408) 473-9274. Fax (408) 473-9370. Address Hyundai Electronics America, 166 Baypointe Parkway, San Jose, CA 95134.

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CIRCLE NO. 74

EDITED BY FRAN GRANVILLE

Logic animator prototypes 50,000-gate ASICs

By throwing out assumptions built into its Enterprise family of ASIC emulation systems, Quickturn Design Systems has produced a less-expensive ASIC prototyping tool, the Logic Animation System Model S50, which models 50,000-gate ASICs at 8- to 16-MHz typ clock speeds. The company lowered the cost of this product by simplifying the hardware design, eliminating some features, and unbundling the software. Consequently, you can use the S50 to create several hardware prototypes that permit software development well before the actual ASICs emerge from fabrication.

The S50 Logic Animation System lowers the cost of ASIC prototyping.

In Quickturn's vision of rapid ASIC prototyping, you start with a netlist in one of several standard formats (currently EDIF, TDL, NDL, and Verilog) that your ASIC design tools create. You feed this netlist, properly massaged, into the S50, and it "becomes" your ASIC. If your ASIC design incorporates memory, standard-logic ICs, or logic cores for which "bond-out" parts exist, the S50 can directly make use of these ICs through an external interface module. This feature can extend the S50's modeling abilities beyond 50,000 gates. Like the company's larger emulation systems, the Logic Animation System connects to the target hardware through an emulation cable and plug. The S50 has 448 bidirectional I/O pins for logic animation.

Unlike the emulation systems, the S50 doesn't provide extensive internal debugging facilities. Instead, it makes use of an instrument found in every hardware lab: a logic analyzer. A separate cable links the S50 to a logic analyzer and connects as many as 448 signals inside the modeled ASIC to the logic analyzer. Currently, the S50 software supports Hewlett-Packard's 1650 and 16500 logic-analyzer families. Support for the Tektronix DAS logic analyzers will appear this year.

The S50's software runs on a workstation and shares many of the same features as the company's Enterprise emulation systems, such as single-pass compilations, correct-by-construction timing, interactive speed optimization, and incremental probe changes for debugging. The software produces 2- to 4-Mbyte files representing the ASIC model. You download these files to a PC, which then runs the S50. Thus, you may need only one $60,000 copy of the software to create several ASIC prototypes using $30,000 S50s and PCs.

Once you have verified your design, you can continue to use the S50 ASIC prototypes while waiting for the actual ASICs to arrive from the foundry. This ability may save you weeks of system-development time by allowing software development and ASIC fabrication to occur concurrently. Because the ASIC model files are relatively small, you can even consider downloading the files over the phone. Consequently, you can provide regular and speedy design updates to software developers miles or continents away from your ASIC-development site.

One more characteristic differentiates the S50 from its larger brethren: It's not expandable. To drive down system cost, the S50's designers created a single-board system with no expansion capabilities. However, more than half of the ASIC designs currently under way are below the S50's 50,000-gate limit.

—by Steven H Leibson

Quickturn Design Systems Inc, Mountain View, CA, (415) 967-3300.

Circle No. 434

Second-generation LONWorks μP runs on half-power

Migrating to a 0.8-μm fab process has reduced the cost and dropped (by one-half) the active power dissipation of Toshiba's second-generation Neuron μP for Echelon's local-operating networks (LONs). The new μP draws 16 mA typ at 10 MHz while operating and only 15 μA (formerly, 500 μA) in sleep mode. A Neuron μP comprises three processors on one chip: two to run the networking protocol and one to run the application program for the application.

The second-generation Neuron is available in two forms: the TMP3150 and TMP3120. Both μPs contain 512 bytes of EEPROM and a unique 48-bit serial identification number. The TMP3150 also includes 2 kbytes of RAM and comes in a 64-lead QFP package. The TMP3120 includes 1 kbyte of RAM and 10 kbytes of ROM and is available in a 32-lead SOIC package. Both devices will sell for around $5 (10,000).—by Steven H Leibson

Toshiba America Electronic Components Inc, Irvine, CA, (714) 455-2000.

Circle No. 435

Intel adds clout to PC/104

Intel Corp has raised the visibility of the PC/104 Consortium's modular-computer standard by joining the group as an executive member. Although PC/104 has more than 100 member companies, the addition of Intel, which is virtually synonymous with the μPs that control PCs, gives the group a big boost in credibility and presence. Intel's motivation, no doubt, is to gain a forum for promot-

SHORTS

More linear-IC price cuts. Joining Comlinear Corp in reducing prices (*EDN*, December 9, 1993, pg 16) is Harris Semiconductor. Enhancements and yield improvements to the company's complementary-bipolar technology are allowing price cuts of up to 50% for wideband amplifiers and buffers. Prices for the latest generation of 350-MHz op amps are approaching the level of older, 100-MHz devices. The price cuts affect op amps and buffers with 3-dB bandwidths in the range of 350 to 850 MHz. One example is the HFA1105/06/35/45 family of 350-MHz, 6-mA quiescent-current op amps whose new prices range from $3.25 to $4.12 (100). The new price for the HFA1100 850-MHz op amp is $4.95 (100), down from the previous price of $7.95. Harris Semiconductor, Melbourne, FL, (800) 442-7747. **Circle No. 436**

High-power semiconductor laser suits high-density optical-disk drives. Mitsubishi has announced the ML1412R, a high-power semiconductor laser that emits 690-nm wavelength red light, approximately 100 nm shorter than conventional wavelength. A single power supply drives the laser, which will find applications as a light source for writing and reading in next-generation, high-density optical-disk drives. Sample quantities cost ¥30,000. Mitsubishi Electric Corp, Tokyo, Japan, (3218) 2456. **Circle No. 437**

Booklet outlines EMI-shielding benefits of perforated metals. If you're a designer, specifier, or buyer concerned about EMI/RFI prevention, you might want to read this free handbook to familiarize yourself with the advantages of perforated metals. The 108-pg publication from the Industrial Perforators Association contains application photos, charts, and data detailing perforated metals' EMI-shielding effectiveness and other properties. Industrial Perforators Association, Milwaukee, WI, (414) 271-2263. **Circle No. 438**

ing its embedded-PC architectures. The chip company predicts a huge market for embedded 386-type processors, and it expects the PC/104 format to play a key role in that market. Stackable PC/104 modules, measuring 3.6×3.8×0.6 in., allow construction of embedded PCs without card cages or backplanes.

—by Gary Legg

PC/104 Consortium, Mountain View, CA, (415) 903-8304. **Circle No. 439**

25-Mbps ATM chip set available for LANs

Transwitch recently announced a technology-access agreement with IBM, which allows Transwitch to market a 25-Mbps asynchronous-transfer-mode (ATM) chip set to LAN-equipment vendors. The ALI-25 chip set permits communications over unshielded LAN cabling.

Transwitch offers an integrated family of standard chip sets that provide ATM access over high-speed channels, including synchronous optical network (SONET), DS-3, and E-3 channels. ALI-25 costs $35 (10,000).

—by John Gallant

Transwitch Corp, Shelton, CT, (203) 929-8810. **Circle No. 440**

HyperSPARC modules top 100 MHz

Using multichip-module techniques, Ross Technology has packed a high-performance CPU with a 256-kbyte second-level cache into a 131-pin PGA (pin-grid-array) package, the RT629. The module fits sockets in workstations that accept HyperSPARC CPUs and runs a fully qualified port of Solaris 2.3. It draws 3.5W and runs 3.3V internally with a 5V external interface.

The modules are available in a variety of speeds. Modules offering 80-, 90-, and 100-MHz CPUs will be in full production by the third quarter. Samples are available now. Samples of a 110-MHz version will be available in July. Prices range from $2511 to $4019 in single quantities.

The module joins a family of the company's devices and modules that use the HyperSPARC architecture. The family includes Mbus modules with single or dual CPUs as well as a single-chip version (RT628) with 128 kbytes of cache.—by Richard A Quinnell

Ross Technology Inc, Austin, TX, (800) 774-7677. **Circle No. 441**

Information Superhighway forum for building national infrastructure

The first conference on forming an infrastructure for the National Information Superhighway takes place September 26 to 28 in San Jose, CA. The summit features a keynote address by Dr John McQuillan, an expert in networking technologies; Ethernet inventor Dr Robert Metcalfe's program for building the infrastructure; tutorials; and seminars. In addition, the summit features

- Reviews of applicable technology and architectures
- Commentary from interexchange carriers, cable companies, and governmental agencies
- Assessment of possible foundations, such as telephone networks, cable systems, and Internet
- Debate on alternatives to delivering voice, data, and video via cable TV, copper-based telephone lines, fiber-optic cabling, and wireless
- Appraisal of new and expected industries and business ventures resulting from the superhighway.

—by Jim Leonard

IDG World Expo, Framingham, MA, (800) 545-3976; (508) 879-6700. **Circle No. 442**

Group promotes bare-die documentation

The DIE Industry Group, formed by ARPA (Advanced Research Projects Agency) to promote multichip-module technology, has developed a specification for providing models and design information on bare-die devices. That specification, DIE (Die Information Exchange) Format 1.0, provides a standard format and information content for bare-die documentation. The infor-

SHORTS

"Trojan horse" compromises Internet. The Federal Computer Emergency Response Team has announced a major breach of the Internet communications system. According to team members, perpetrators planted a "Trojan horse" program in various Internet users' systems. The program gathered log-on information from users accessing a specific system through the Internet. The break-in could affect thousands of Internet users, according to the team, which serves as a clearing house for Internet security concerns. Federal Computer Emergency Response Team, Carnegie-Mellon University, Pittsburgh, PA, (412) 268-7080.

Circle No. 443

Aspec to offer $40,000 ASIC design. Attendees at the Design Automation Conference, scheduled for June 6 to 8 at the San Diego Convention Center, will have a chance to win a $40,000 design award. Aspec Technology Inc will offer a free design of as many as 100,000 gates based on the company's proprietary high-density array, sea-of-gates technology. The design award comprises a complete package, from netlist to database tape. Alternatively, the winner can apply the $40,000 to the purchase of an Aspec Portfolio family of ASIC design tools. Aspec Technology Inc, Santa Clara, CA, (408) 988-4411. **Circle No. 444**

Yamaha asserts audio patents. With the expiration of the original patents covering FM sound synthesis, several manufacturers sought to break Yamaha's virtual monopoly in supplying synthesis ICs to the sound-board market by making or incorporating OPL-equivalent devices. Yamaha has brought suit against them, asserting that still- active US Patents 4,249,447 and 4,813,236 cover the specific techniques used in its OPL chips and are being infringed. Hearings began on May 6.

Circle No. 445

mation includes administrative, geometric, electrical, thermal, and process data, as well as logic-simulation models. The format allows CAD systems to use the data, which is also human-readable.

The DIE Industry Group began its work with digital-logic ICs. It is now working to expand the specifications to include analog die as well as flip-chip and TAB devices. It expects to have the expanded specification available by year-end. The group comprises both semiconductor and CAD-tool vendors, including Cadence Design Systems, Logic Modeling, AT&T Microelectronics, Intel, IDT, Micron Semiconductor, Motorola, National Semiconductor, and Texas Instruments.—by Richard A Quinnell

DIE Industry Group, Beaverton, OR, (503) 531-2252. **Circle No. 446**

Recognize an outstanding peer

Test & Measurement World magazine is soliciting nominations for its fifth annual "Test Engineer of the Year" award. To qualify, individuals must spend most of their time working on test problems, but a specific test-engineer title is not mandatory. The nominee must work in the electronics industry and be involved with testing, measuring, inspecting, quality assurance, or another related function.

If you're a peer, supervisor, or subordinate who knows a deserving engineer, send a fax to T&MW at (617) 558-4470 for a simple form to complete. All nominations are due by August 15. The magazine will present the award at the International Test Conference in Washington, DC in October. The winner receives a certificate and $1000; the nominator gets $250.—by Joan Lynch

Test & Measurement World, Newton, MA, (617) 558-4671. **Circle No. 447**

X terminals offer full-motion video

Human Designed Systems has added full-motion video to its line of RISC-based X Window terminals. Called HDS Video, the capabilities allow users to display full-motion video in as many as four windows on their HDS X terminal screens. HDS Video supports analog and digital video with onboard compression and decompression.

Full-motion video suits applications such as presentations, training, monitoring, and teleconferencing. For teleconferencing applications, the company has also introduced HDS Conference video-teleconferencing application software, which allows multiple X terminal users to communicate over Ethernet and view each other in an X Window.

Users can connect a camera, a video CD-ROM, or a videocassette recorder to a terminal and display the video from this source on the screen in movable, resizable windows. The terminal supports full-screen display of video at 30 frames/sec with broadcast quality.

Digital video allows HDS X terminals to support video in networks for applications such as video teleconferencing. HDS supports the Intel/Microsoft Indeo compression standard and offers optional MPEG hardware decompression.

An optional capability, HDS Audio, allows recording and playback of stereo sound. With HDS Audio, each terminal has an internal speaker and connections for external speakers. Users can also connect an audio source, such as a stereo CD, a microphone, or a tape recorder, to the terminal.

Adding HDS Video or Audio to the company's ViewStation multimedia terminals costs $199 for stereo sound, $199 for digital video, $499 for analog and digital video, and $199/user for the HDS Conference application.

—by Fran Granville

Human Designed Systems, King of Prussia, PA, (610) 277-8300.

Circle No. 448

"Smart batteries" lower portable-products' costs

Duracell and Intel have announced the Smart Battery Data (SBD) and the System Management Bus (SMBus), two "smart-battery" specifications. End users can expect portable products, such as notebook computers, video camcorders, and cellular telephones, incorporating the specifications to have lower costs, more reliable battery-level information, and the ability to adapt to new battery technologies.

A smart battery is a rechargeable

CIRCLE NO. 114

SHORTS

IC maker starts East Coast design facility. Linear Technology Corp is recruiting staff for its recently established Boston Design Center in Burlington, MA. The company seeks approximately 12 linear designers of MOS and bipolar data converters, power-supply and -management products, references, comparators, and op amps. The Boston unit joins Linear's headquarters in California and a similar center in Singapore. Linear Technology Corp, Milpitas, CA, (408) 432-1900. **Circle No. 449**

ITT Cannon forms joint venture with ZCF. ITT Cannon, a supplier of electronic components, interconnection systems, and information-card technology, has formed a joint venture with Zhenjiang Connector Factory (ZCF), the largest connector company in China. ITT Cannon, Santa Ana, CA, (714) 261-5300. **Circle No. 450**

Digi-Key earns ISO 9002 certification. Digi-Key Corp recently earned ISO 9002 certification covering the purchasing, warehousing, and distribution of the company's electronic components, computer products, and accessories, including value-added assembly processes. Digi-Key Corp, Thief River Falls, MN, (800) 344-4539. **Circle No. 451**

Guide explains PCMCIA standard. *The PCMCIA Developer's Guide* provides a comprehensive overview of the Personal Computer Memory Card International Association (PCMCIA) standard. The 450-pg book also offers design examples for PC cards, hosts, and software drivers; it gives information on reference materials. $89.95. Sycard Technology, Sunnyvale, CA, (408) 247-0730. **Circle No. 452**

DEC introduces Internet service. Digital Equipment Corp has announced the Internet Electronic Connection, a set of free services allowing consumers in educational institutions and research laboratories to obtain information about—and place orders for—DEC's products and services directly over Internet. Digital Equipment Corp, Maynard, MA, (508) 493-5111. **Circle No. 453**

Consortium aims to advance technology. The Institute for Interconnecting and Packaging Electronic Circuits (IPC) has established the Interconnect Technology Research Institute (ITRI). ITRI's goal is to provide a vehicle for collaboration among the electronic-interconnection industry, government, and academia to develop and deploy advanced technology for printed-wiring boards and printed-wiring-board assemblies. IPC, Lincolnwood, IL, (708) 677-2850. **Circle No. 454**

Catalog lists more than 1200 software products. This 95-pg, indexed catalog, "Software for Science," lists more than 250 new products and 100 CD-ROM titles for astronomy, CAD, curve fitting, data acquisition, electrical engineering, and a variety of other disciplines. In addition, the catalog includes articles on software selection, such as "Equation Editor or Word Processor," "A Practical Guide to Survey Design," and "Choosing an Image-Analysis System for Remotely Sensed Data." Scitech International Inc, Chicago, IL, (800) 622-3345. **Circle No. 455**

Booklet helps Internet users get on-line. This 64-pg, $2.95 booklet, "Internet Public Access Guide," defines Internet terms; describes Unix commands; and details electronic mail, Usenet news, remote-system access, and information searching. Specialized System Consultants Inc, Seattle, WA, (206) 527-2806. **Circle No. 456**

device with specialized hardware that provides present-state, calculated and predicted information to the host system under software control. This provides users with state-of-change information and an accurate prediction of the remaining operating time. Because the smart battery maintains its own information, a host device can accommodate multiple battery chemistries and appropriately charge them. Call Duracell or Intel for copies of the smart-battery specifications.—by Fran Granville

Duracell, Bethel, CT, (800) 422-9001, ext 423. **Circle No. 457**

Intel Corp, Mount Prospect, IL, (800) 253-3696. **Circle No. 458**

Zap confusing buttons from your remote control

How many buttons on your TV or VCR remote control go unused because you can't find the original documentation? What if you have the manual but don't understand what a button is for—or don't want to use it—anyway? In an effort to make electronic products easier to use and to battle "technophobia," Arthur D Little Enterprises has developed a technology that lets you eliminate unwanted or unused buttons from electronic products' keypads.

Called Custom Control, the technology lets you add, remove, and reposition unwanted or confusing controls from remote controls, telephones, calculators, and other products with buttons or keys. Custom Control supplies the target product with a set of buttons, each having its own electrical/mechanical identity, which corresponds to a feature or function of the product. You select only the buttons or keys you want from this set of controls and then place the controls on a "blank" control panel in whatever arrangement is most convenient. If you change your mind, you can recustomize the controls at any time.

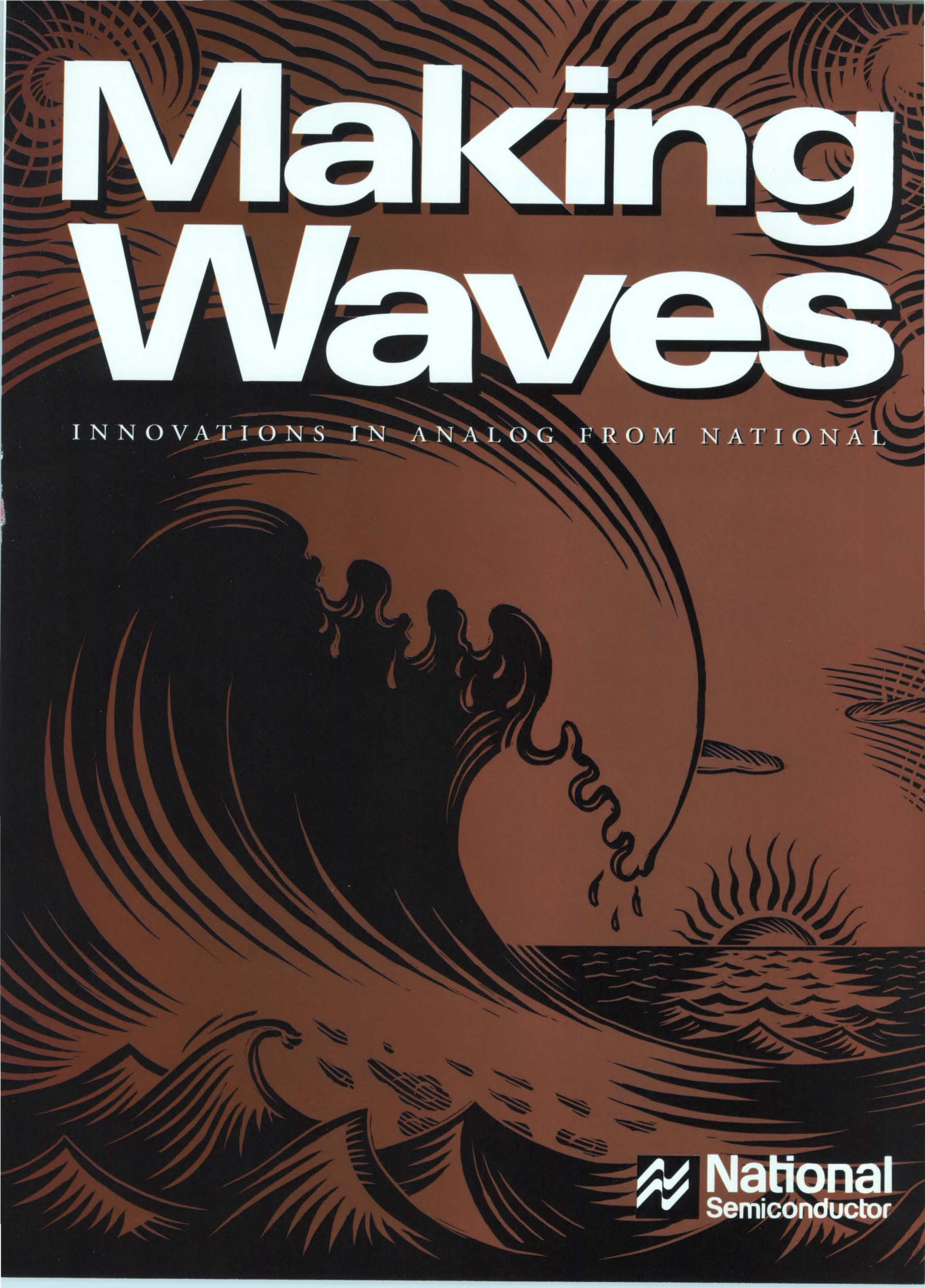
The company is currently negotiating with major consumer electronics companies about licensing. The first implementation of the technology will hit the stores in September—in the form of a universal remote controller.

—by Fran Granville

Arthur D Little Enterprises Inc, Cambridge, MA, (617) 498-5000. **Circle No. 459**

Making Waves

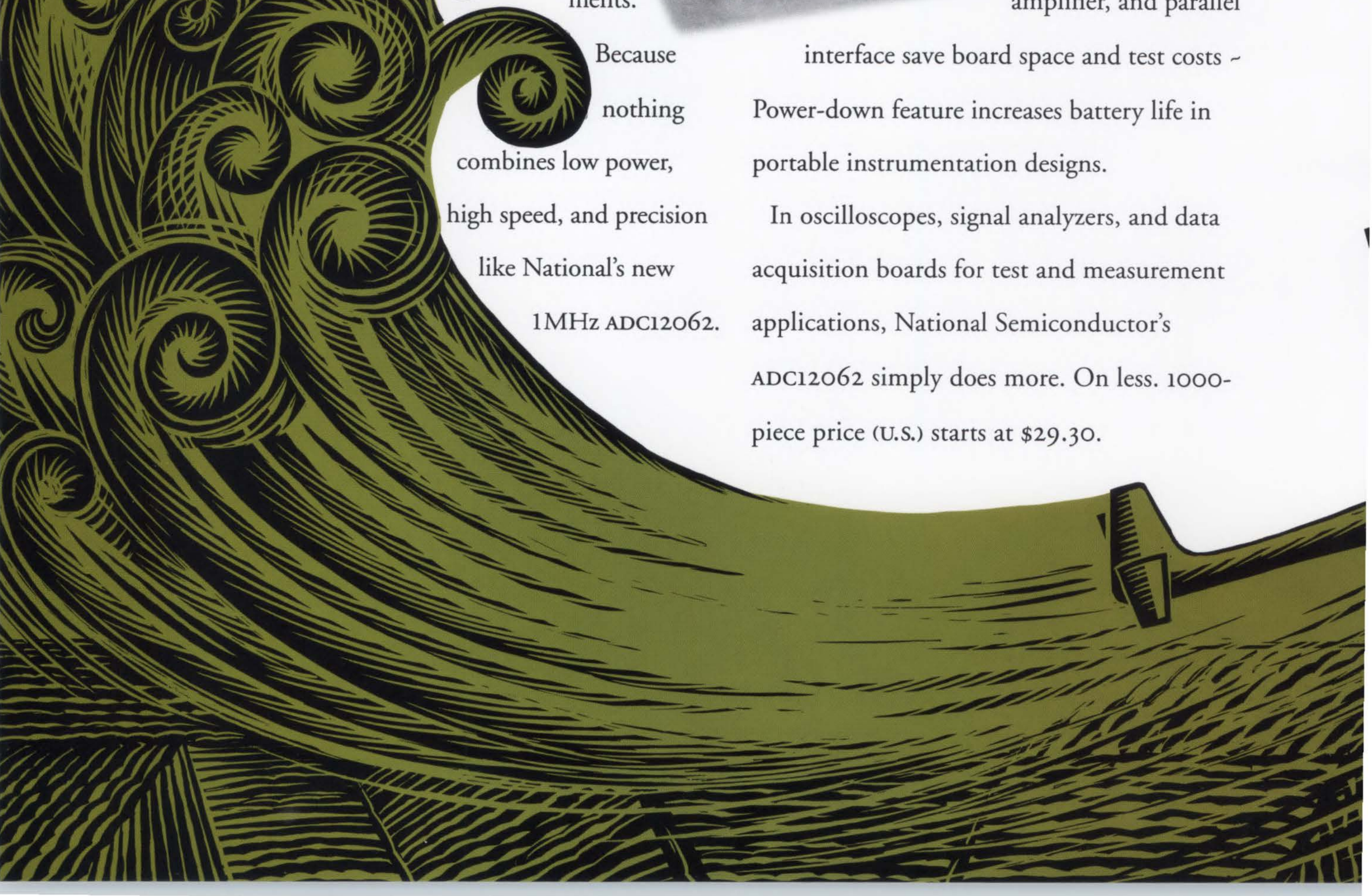
INNOVATIONS IN ANALOG FROM NATIONAL



National Semiconductor

75mW: A little power takes you a long way.

The world's lowest power 1MHz 12-bit ADC: Designers of high-end instrumentation and communications systems no longer have to rely on expensive, power-hungry hybrids to fulfill their high speed/high resolution requirements. Because nothing combines low power, high speed, and precision like National's new 1MHz ADC12062.

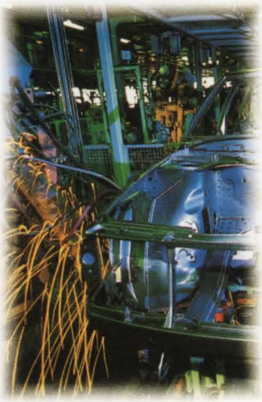


Maximum power dissipation of just 75mW at 5V provides the low power consumption needed to improve overall system efficiency – Fast sampling rate of 1MHz is ideal for high-speed data acquisition – Patented EEPROM trimming architecture guarantees AC and DC specs unmatched in the industry: Gain error = ±1LSB (max.), offset error = ± 1.25LSB (max.), INL = ± 1LSB (max.), DNL = ± 0.95LSB (max.), and SNR @ 100kHz is 69.5dB (min.), ensuring the accuracy of the signal received by a microprocessor or DSP – On-board 2-channel MUX and sample/hold amplifier, and parallel interface save board space and test costs – Power-down feature increases battery life in portable instrumentation designs.

In oscilloscopes, signal analyzers, and data acquisition boards for test and measurement applications, National Semiconductor's ADC12062 simply does more. On less. 1000-piece price (U.S.) starts at $29.30.

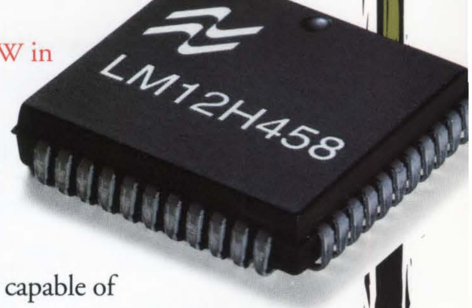
5.5µs: The world's fastest DAS flies from A-to-D.

The world's fastest 12-bit data acquisition system: There are certain applications — diagnostic systems, portable instrumentation, industrial control — where nothing short of a high-speed, low-power, fully integrated data acquisition system will suffice. Fortunately for those applications, there's nothing faster, more power-efficient, or more fully integrated than the LM12H454/8.



National's high-speed, low-power DAS is ideal for robotics and industrial control.

Maximum conversion rate of 5.5µs (minimum throughput rate of 140ksps) - The industry's lowest power consumption: 34mW (50µW in powerdown mode) - Mixed analog and digital technology creates a complete system on a chip, fully capable of providing stand-alone operation - High integration simplifies complex designs by reducing testing and debugging - Analog front-end consists of a self-calibrating 12-bit plus-sign ADC with sample and hold, a reference, and a four- or eight-channel MUX - Digital features include an eight-word instruction RAM, a sequencer, a 16-bit timer, and a 32-word FIFO - "Watchdog" comparison mode provides quick (1.4µs) threshold detection and alarm monitoring.



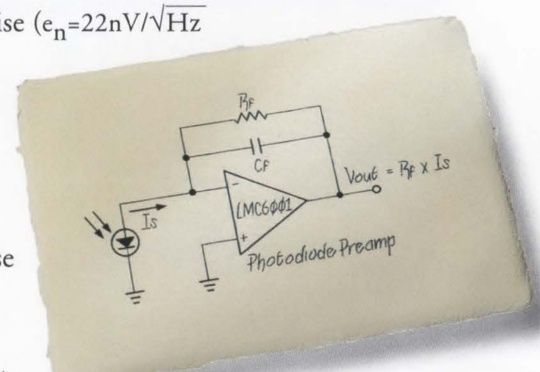
Guidance and control. Medical instrumentation. Energy management. For applications that demand it all, the LM12H454/8 delivers. 1000-piece price (U.S.): $17.00.

The ADC12062 offers the industry's best combination of power consumption, speed, and precision. The LM12H454/8 provides an unmatched mix of high speed and high integration. For more information, call 1-800-NAT-SEMI, Ext. 287.

25fA: Input current reduced to its lowest level.

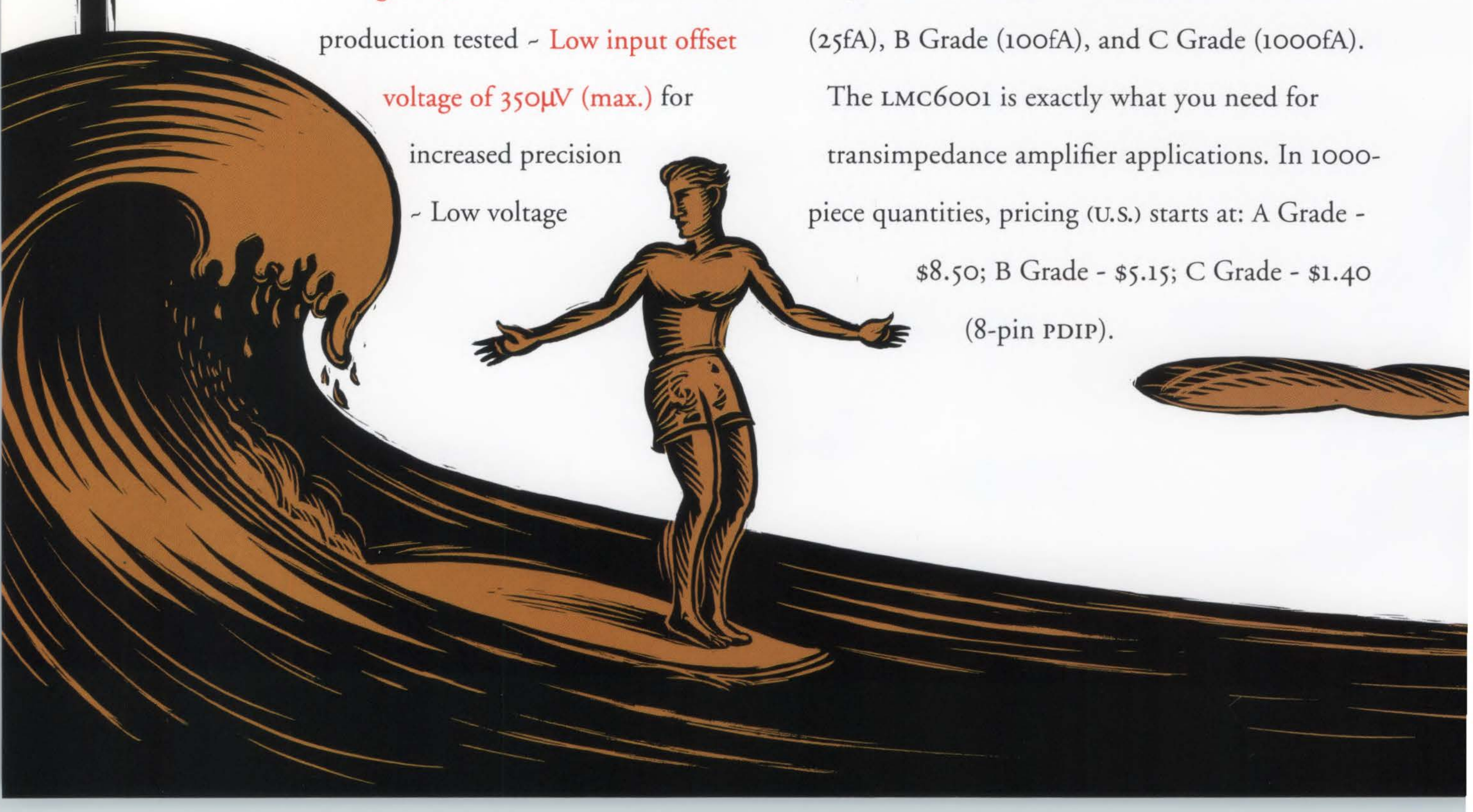
25×10^{-15} A — The new standard in low input current op amps: In highly sensitive measuring equipment, there's no room for error. Which means there's no room for an op amp with excess input current. That's why National Semiconductor designed the LMC6001 to have the world's lowest guaranteed input current. Low enough to improve system accuracy in such applications as pH meters, medical analysis equipment, gas detectors, and various types of photodiode-based systems.

Guaranteed I_b of 25fA (max.) at 25°C is 100% production tested ~ Low input offset voltage of 350µV (max.) for increased precision ~ Low voltage offset drift of 10µV/°C (max.) ~ Increased dynamic range through rail-to-rail output swing ~ Low voltage noise (e_n=22nV/$\sqrt{\text{Hz}}$ @ 1kHz) provides higher signal-to-noise ratio than JFET input type electrometer amplifiers ~ Low supply current of 750µA (max.) is ideal for power-sensitive applications and minimizes heating effects on input current and offset voltage ~ Available in plastic DIP ~ Designed and guaranteed for operation over the industrial temperature range (-40°C to +85°C) ~ Available in A Grade (25fA), B Grade (100fA), and C Grade (1000fA).



With a low input current of only 25fA (max.), the LMC6001 is ideal as a preamp for current output transducers.

The LMC6001 is exactly what you need for transimpedance amplifier applications. In 1000-piece quantities, pricing (U.S.) starts at: A Grade - \$8.50; B Grade - \$5.15; C Grade - \$1.40 (8-pin PDIP).

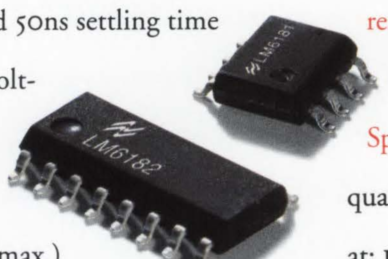


o p e r a t i o n a l   a m p l i f i e r s

Versatile:
High speed, high drive, low power.

The LM6181/2 and LMC6572/4: You no longer have to pay a premium for op amps that deliver solid, all-around performance.

LM6181/2: Single- and dual-current feedback amps for video, communications, and imaging systems ~ 100MHz unity gain bandwidth and 100mA of output current ~ No-hassle, one-chip solution eliminates output buffer ~ Differential gain of 0.05% and differential phase of 0.04° ~ 2000V/μs slew rate and 50ns settling time (0.1%) ~ Tight offset voltage (3mV max.) and input bias current (I_b^+ = 2.0μA / I_b^- = 5.0μA max.) for precision needs ~ Fully specified for ±5V and ±15V operation ~ DIP and SOIC.



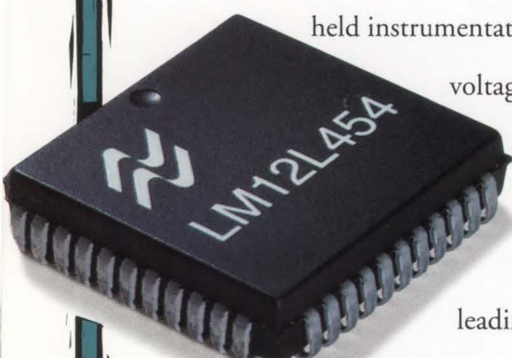
LMC6572/4: Provides guaranteed 2.7V and 3V single-supply performance for portables and mobile communications systems ~ Ideal for interfacing with 3.3V digital logic regulated or unregulated supplies ~ Rail-to-rail output swing maximizes S/N and dynamic signal range, providing an efficient interface to ADCs ~ Wide input range from below ground to 800mV below the positive supply ~ Low input current of 20fA increases accuracy ~ Low supply current of 40μA ~ 120dB voltage gain/amp ~ Specified for 100kΩ and 5kΩ loads. In quantities of 1000, pricing (U.S.) starts at: LM6181 - $2.00; LM6182 - $3.60; LMC6572 - $.90; LMC6574 - $1.20.

Our LM6181/2 provides the performance you need for professional video applications.

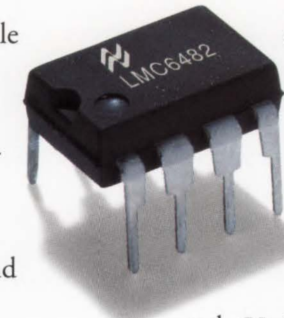
For more information on the LMC6001, LM6181/2, and LMC6572/4, call 1-800-NAT-SEMI, Ext. 287 for free product sample kits.

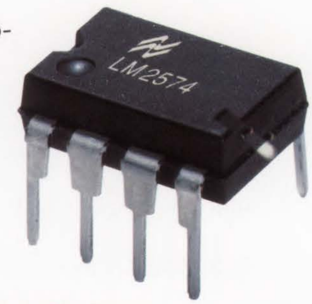
3-volt analog: Fueling the portable wave.

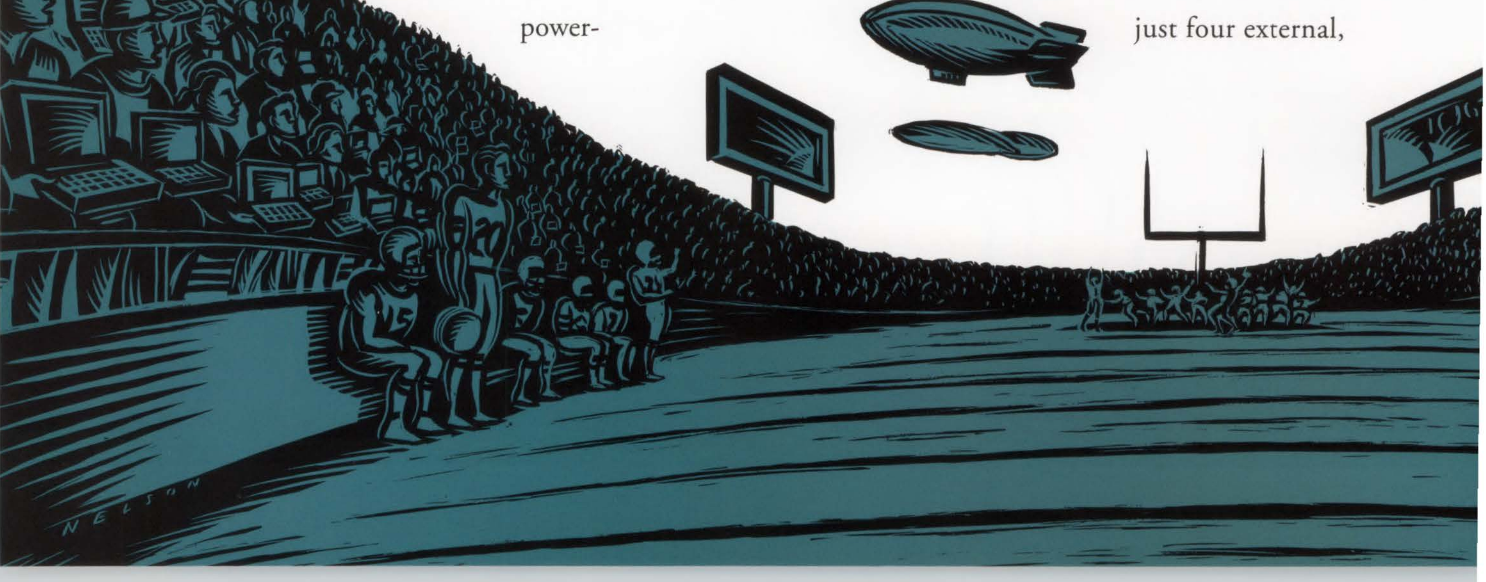
Maximum performance on a minimum of power: The popularity of portability is rising fast. Portable computing, mobile communications, and hand-held instrumentation designs need low-voltage solutions that will reduce system size and extend battery life. That's why National is leading the way by offering high-performance 3V analog products in data acquisition, power management, and amplifier ICs. Products that save power without sacrificing performance.



LM12L454/8 12-bit plus sign data acquisition system: Complete system on a chip with 106ksps throughput, 15mW (max.) power dissipation (5µW in power-down mode), and all the functionality needed for stand-alone operation – ADC12L030/2/4/8 12-bit plus sign A/D: Fastest 3V 12-bit serial A/D (maximum conversion time of 5.5µs) at 15mW (max.) power dissipation (40µW in powerdown); configurable registers – LMC6572/4 op amp: Low supply current of 40µA/op amp minimizes power consumption; guaranteed 2.7V and 3V single-supply performance; low input current increases accuracy – LMC6482/4 op amp: Rail-to-rail input and output increases dynamic signal range at 3V; lower offset voltages and higher CMRR increases precision – LM2574/5/6 SIMPLE SWITCHER® power converter: First easy-to-use power converter family with 3.3V output and guaranteed system performance; requires just four external,







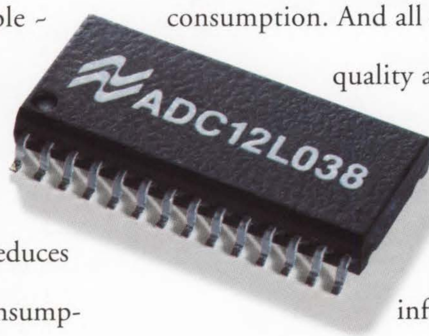
low-voltage solutions

off-the-shelf components; design software available – LP2950/51 low dropout regulator: Very low dropout voltage of 380mV extends battery life; low quiescent current of 75µA reduces power consumption and power dissipation – LM4041 voltage reference: Subminiature SOT-23 package saves board space and reduces overall system size; adjustable voltage option (1.24V to 10V) provides design flexibility.

3V analog	
DEVICE	PRICE*
LM12L454/8	$15.00
ADC12L030	$10.90
LMC6572	$0.90
LMC6482	$1.55
LM2574N-3.3	$1.70
LP2951CN-3.3	$1.23
LM4041	$0.72

*QUANTITIES OF 1000, U.S. ONLY

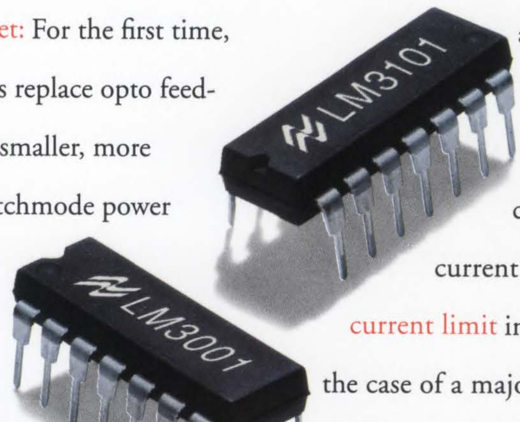
All of National's 3V analog solutions are designed to increase the performance of your portable designs — while reducing power consumption. And all of them come with the quality and reliability you expect from the original leader in analog IC technology. For pricing information, consult the box to your left or call the number below.



For 3V analog that will fuel your imagination as well as your designs, call 1-800-NAT-SEMI, Ext. 287. We'll send you free product sample kits or information kits.

Magnetics: Opto-less chipset brings reliable power supplies offline.

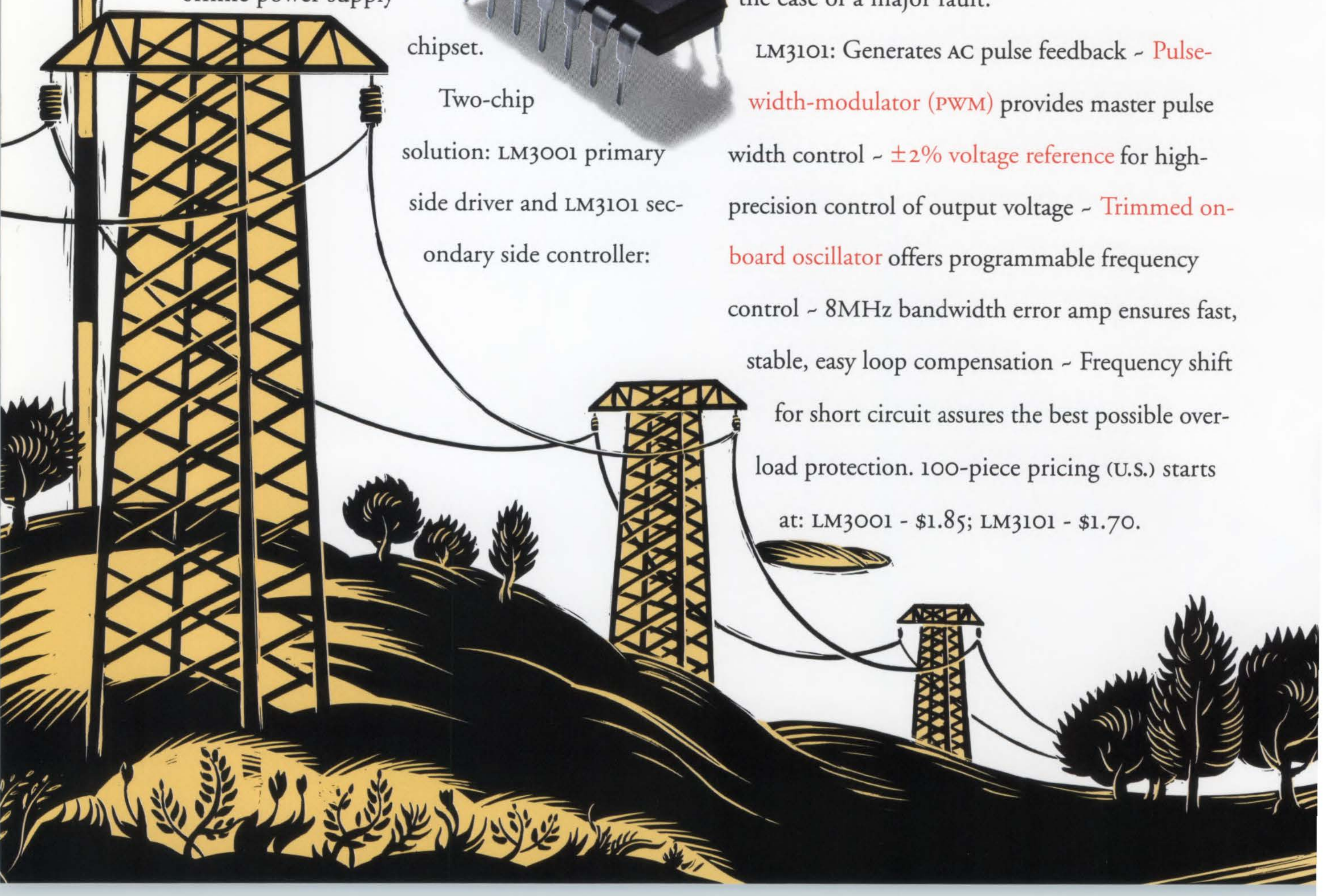
The world's only 1MHz magnetically coupled offline power supply chipset: For the first time, high-speed pulse magnetics replace opto feedback devices. The result is smaller, more efficient, more reliable switchmode power supplies. The reason is National's LM3001/3101 offline power supply chipset.



Two-chip solution: LM3001 primary side driver and LM3101 secondary side controller: Fast AC feedback provides quicker response than optos ~ Up to 1MHz switching frequency enables the use of smaller inductors and capacitors.

LM3001: Accepts AC pulse feedback ~ 10ns rise and fall times provides greater efficiency and fast response to faults ~ On-board oscillator manages chip start-up ~ 2.5A peak current drives MOSFETs at high speed ~ Dual-level current limit provides virtually fail-safe operation: Cycle-by-cycle current limit offers fast current protection, while second-level current limit initiates complete shutdown in the case of a major fault.

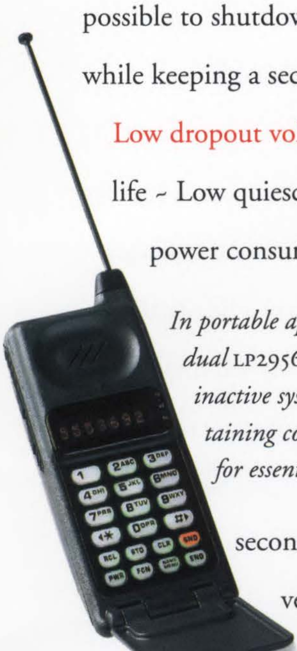
LM3101: Generates AC pulse feedback ~ Pulse-width-modulator (PWM) provides master pulse width control ~ ±2% voltage reference for high-precision control of output voltage ~ Trimmed on-board oscillator offers programmable frequency control ~ 8MHz bandwidth error amp ensures fast, stable, easy loop compensation ~ Frequency shift for short circuit assures the best possible overload protection. 100-piece pricing (U.S.) starts at: LM3001 - $1.85; LM3101 - $1.70.



l o w d r o p o u t r e g u l a t o r s

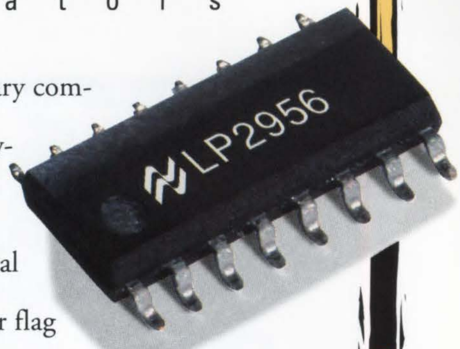
Dual:
µPower LDO does twice the work.

The world's first dual micropower low dropout regulator: When it comes to extending battery life in portable applications, two regulators are better than one. Case in point: National's LP2956. Two low dropout regulators in one package make it possible to shutdown one system and save power, while keeping a second system active.



Low dropout voltage of 470mV extends battery life – Low quiescent current of 170µA reduces power consumption and power dissipation – Independent, auxiliary low dropout regulator enables second load (up to 75mA) to be driven while driving a primary load of up to 250mA – Electronic shutdown allows device to be turned on and off as desired – Auxiliary comparator can be used for low-battery detection, fault detection, or as a reset signal to a microprocessor – Error flag for the main regulator indicates when it has fallen out of regulation by more than 5%.

In portable applications, the dual LP2956 shuts down inactive systems while maintaining continuous power for essential functions.



The LP2956 is the highest performance dual low dropout regulator available. It's the best thing to happen to your battery-powered designs since the batteries themselves. 100-piece price (U.S.): $2.95.

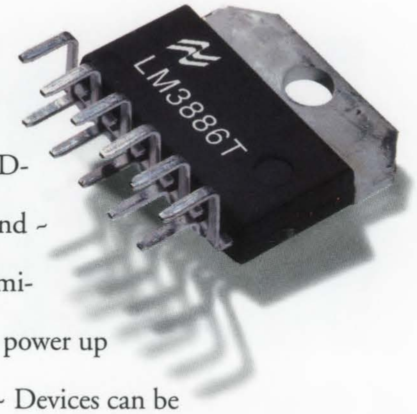
If your design plugs into a wall socket, we've got your power supply chipset. If it runs on batteries, we've got your low dropout regulator. To get your free product sample kits, call 1-800-NAT-SEMI, Ext. 287.

.03% THD: 60 watts never sounded as good as this.

The world's best sounding monolithic audio amplifier: See if you like the sound of this. National's LM3886T provides a higher standard of high fidelity, as well as maximum power with maximum protection.

The 60-watt LM3886T *enables better, louder, longer sound in high-end audio applications like A/V surround sound receivers.*

Lowest typical total harmonic distortion (THD) from 20Hz to 20kHz at 25, 40, and 60 watts of continuous power provides the industry's best distortion/power rating - Signal-to-noise ratio is greater than 95dB min. (noise floor of 2.0µV), meeting the demands of CD-quality digital sound - Mute function eliminates transients at power up and power down - Devices can be easily bridged together - SPiKe™ self-protection circuitry adjusts output drive capability according to operating conditions, protecting output transistor array from overvoltages, undervoltages, or current limiting conditions, and providing thermal shutdown - Dynamic SOA protection ensures that power transistors won't be destroyed — even if faults continue for extended periods.

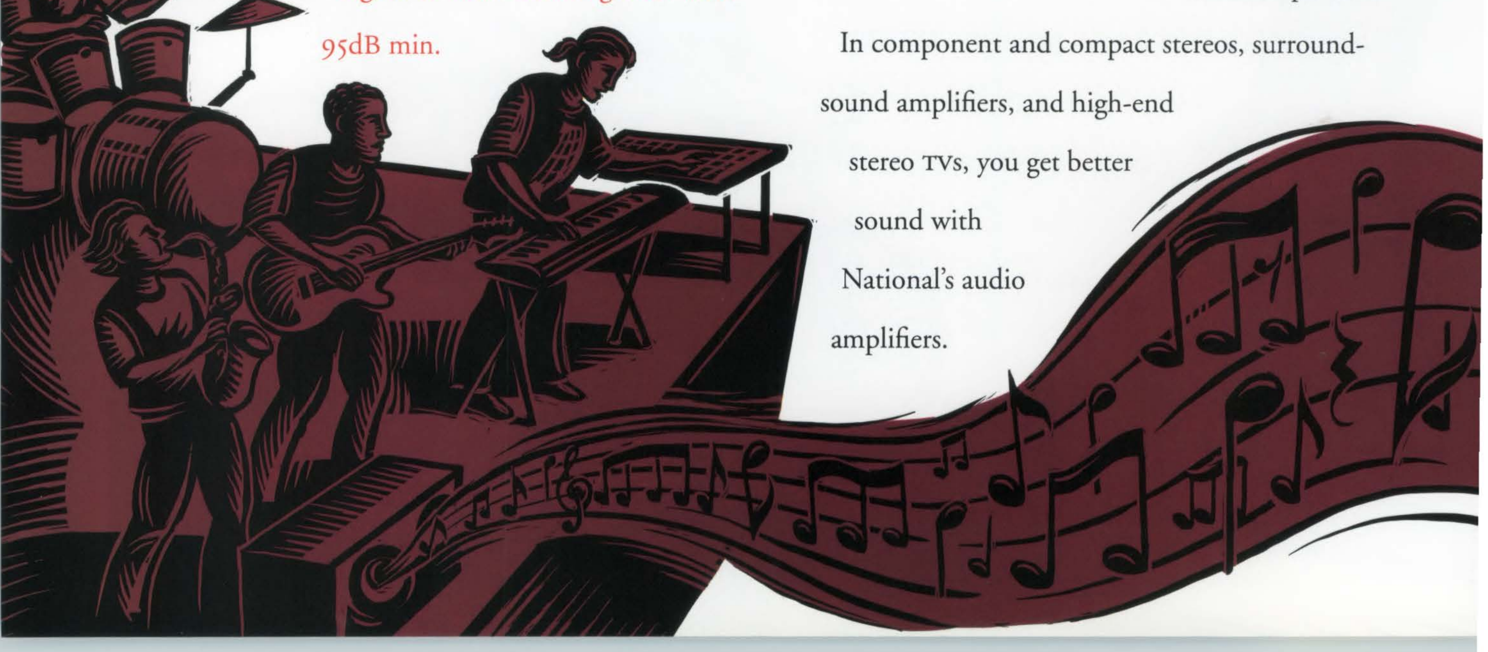


Typical THD*

DEVICE	THD (typ.)	OUTPUT
LM2876T	0.05%	25W
LM3875T	0.05%	40W
LM3876T	0.05%	40W
LM3886T	0.03%	60W

* from 20Hz to 20kHz

In component and compact stereos, surround-sound amplifiers, and high-end stereo TVs, you get better sound with National's audio amplifiers.



130MHz: High-speed LM1205 saves board space.

Complete broadband preamplifier system: When used with National's LM2419 CRT driver (see back cover), the LM1205 130MHz RGB video preamplifier replaces up to 36 components, compared to using standard preamps and discretes.

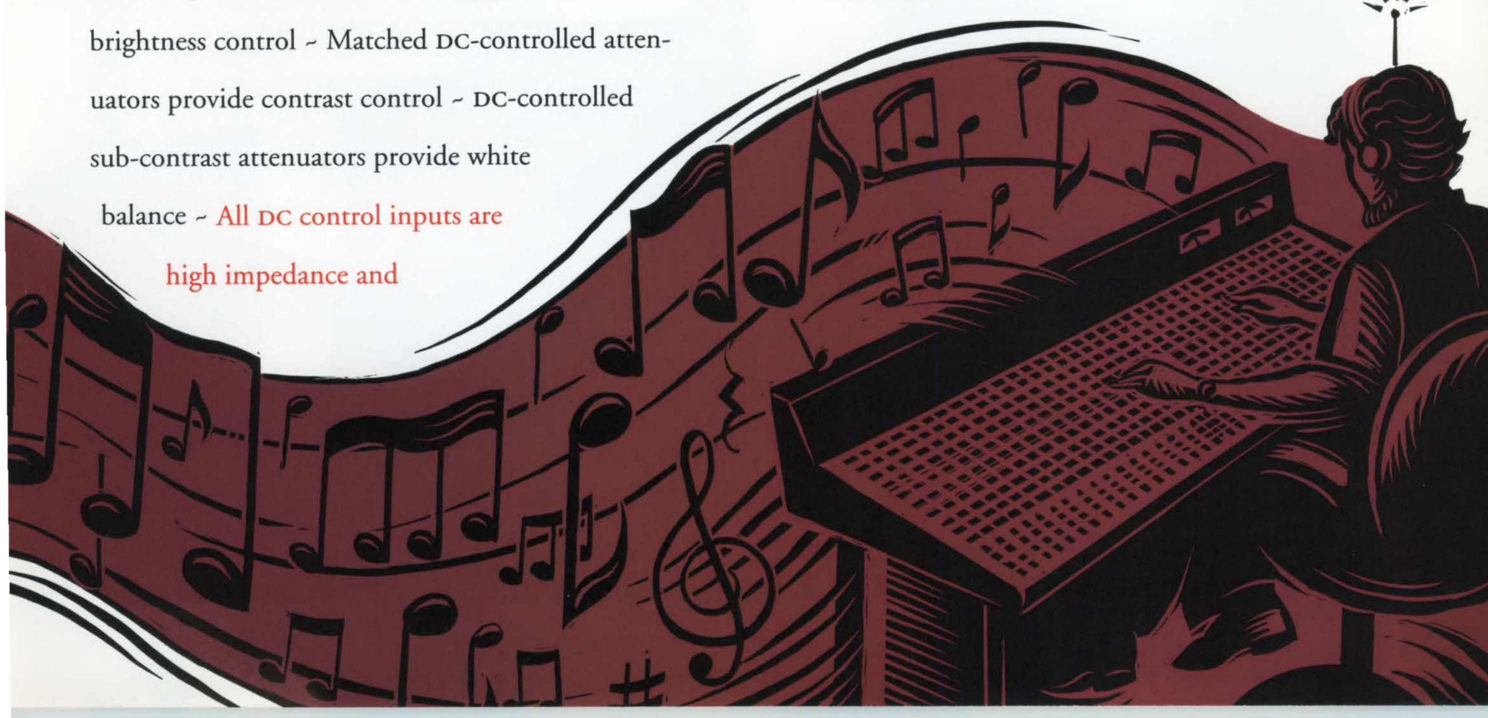
Features	
BANDWIDTH	130MHz
DC CONTROLS	0-4V
VIDEO BLANKING	YES
CHANNELS	3
APPLICATION	HIGH-RES. DISPLAYS

Provides the entire amplifier path required between the rear chassis input and the cathode for 1024 x 768 monitors ~ Each channel contains matched video amplifiers ~ Gated, single-ended input and black-level clamp provide brightness control ~ Matched DC-controlled attenuators provide contrast control ~ DC-controlled sub-contrast attenuators provide white balance ~ All DC control inputs are high impedance and operate over a 0 to 4V range for easy interface in microcontroller-based systems ~ Blanking circuit clamps the video output voltage to within 0.2V of ground ~ For high-speed, space-conscious designs.

The LM1205 provides the performance needed for multimedia applications.

In high-end, 17-inch RGB CRT monitors, 1280 x 1024 pixel systems, video AGC amplifiers, and wideband amplifiers with gain and DC offset controls, the LM1205 gives you more performance. While using less board space. In quantities of 1000, pricing (U.S.) starts at $2.50.

To fully appreciate the sights and sounds of National's audio and video ICs, call us at 1-800-NAT-SEMI, Ext. 287 and we'll send you free sample kits containing product samples, a blank applications board, data sheets, and application notes.



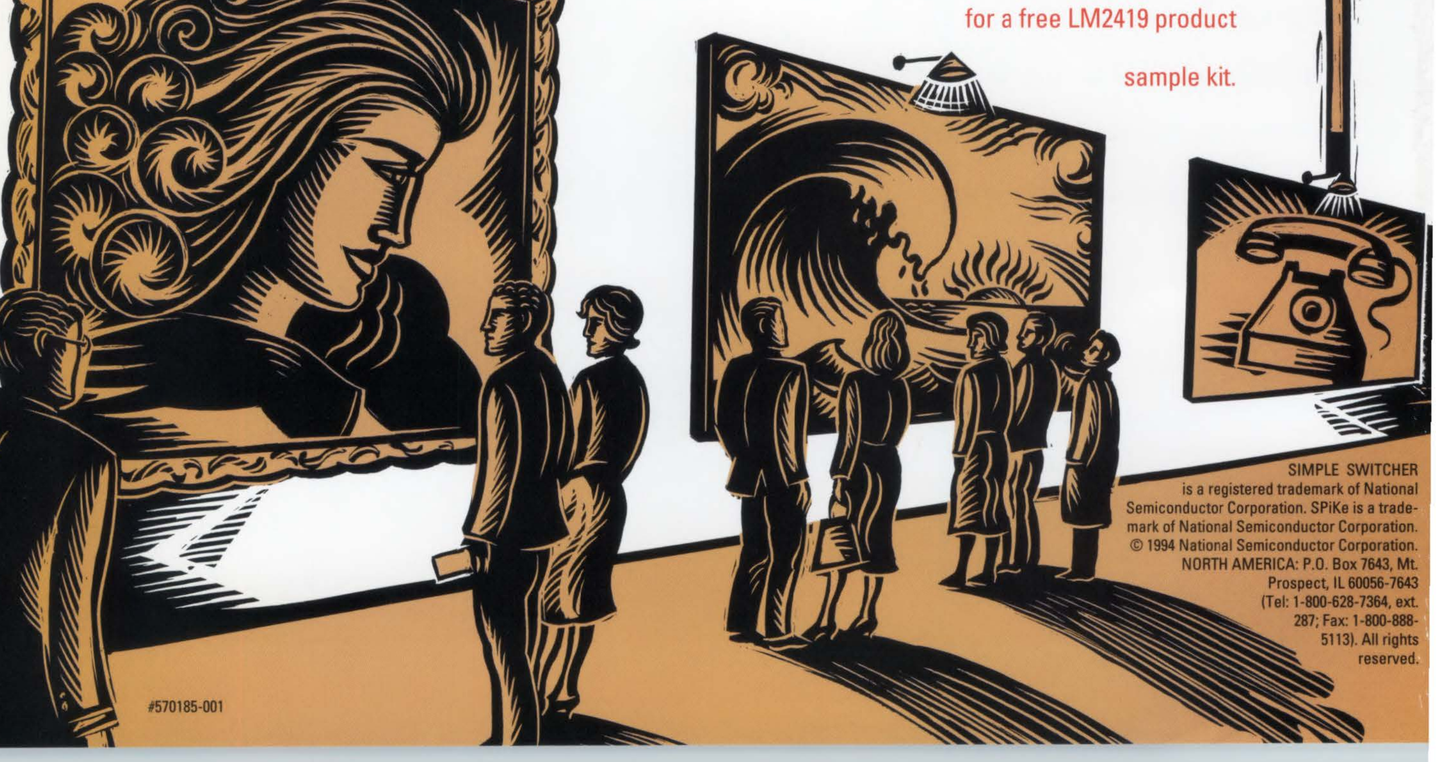
CRT drivers

5.0ns: For a picture everyone can appreciate.

High-performance triple CRT driver for high-resolution monitors: Picture a device that provides resolution up to 1024 x 768 in color monitors while simplifying overall design. You're picturing the LM2419, National Semiconductor's triple 65MHz CRT driver. Typical rise/fall time of 5ns provides clean, sharp signal transition edges for high-resolution images ~ 65MHz video bandwidth at 50Vpp output swing with 8pf load for a bright screen and a clear image ~ Three drivers match red, green, and blue channels in one device ~ Available in industry-standard TO-220 molded power packages ~ Electrically isolated heat sink may be grounded for ease of manufacturing and improved RFI/EMI shielding ~ Pin-for-pin compatible with LM2416, simplifying upgrades ~ No low-frequency tilt compensation required. For direct cathode drive capability in VGA, SVGA, XGA, IBM and Macintosh monitors, nothing looks better.

The LM2419's 5ns rise/fall time provides clean, sharp signal transition edges for high-resolution images.

For high resolution in color monitors, your choice is clear. Call 1-800-NAT-SEMI, Ext. 287 for a free LM2419 product sample kit.



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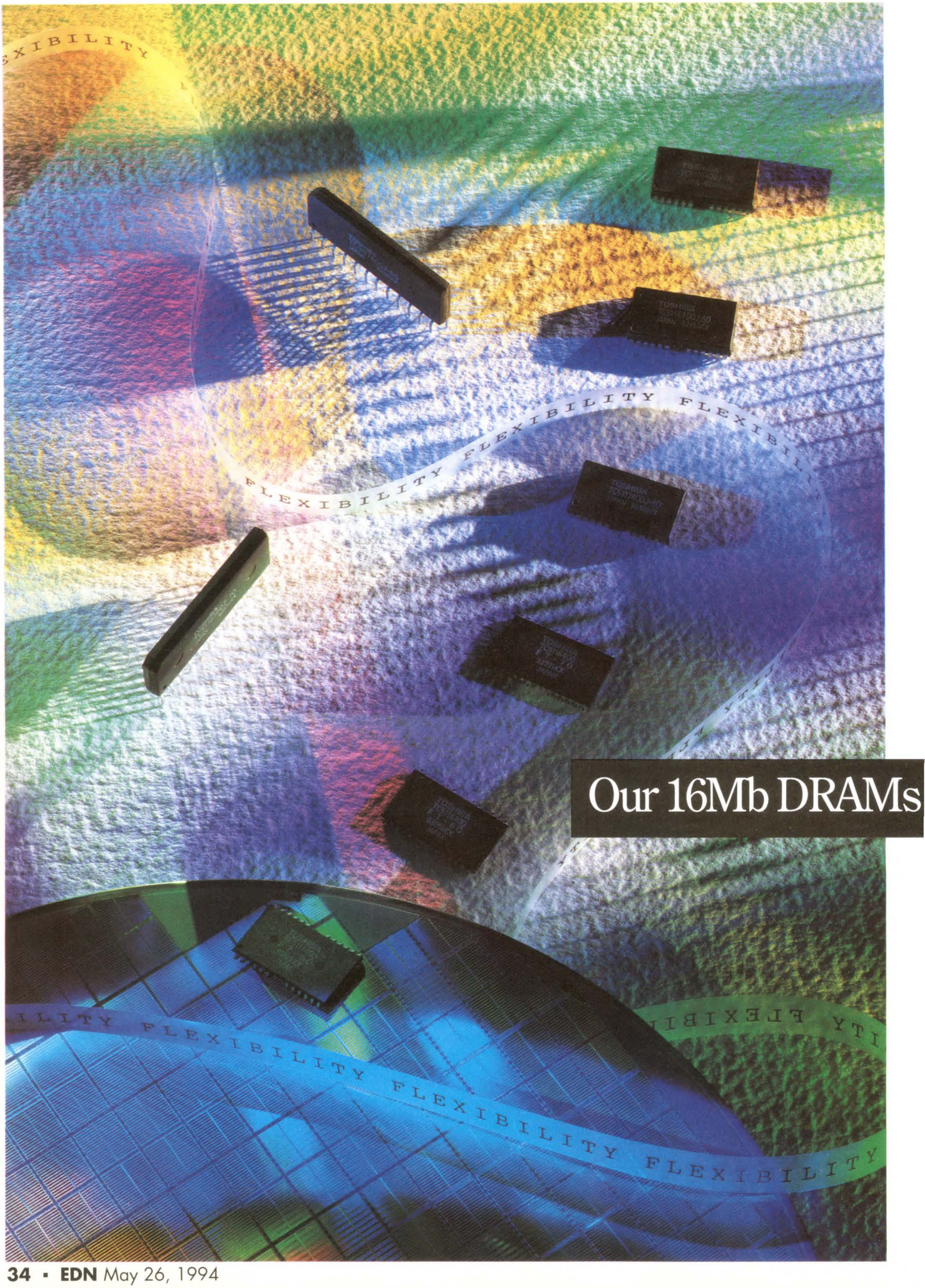
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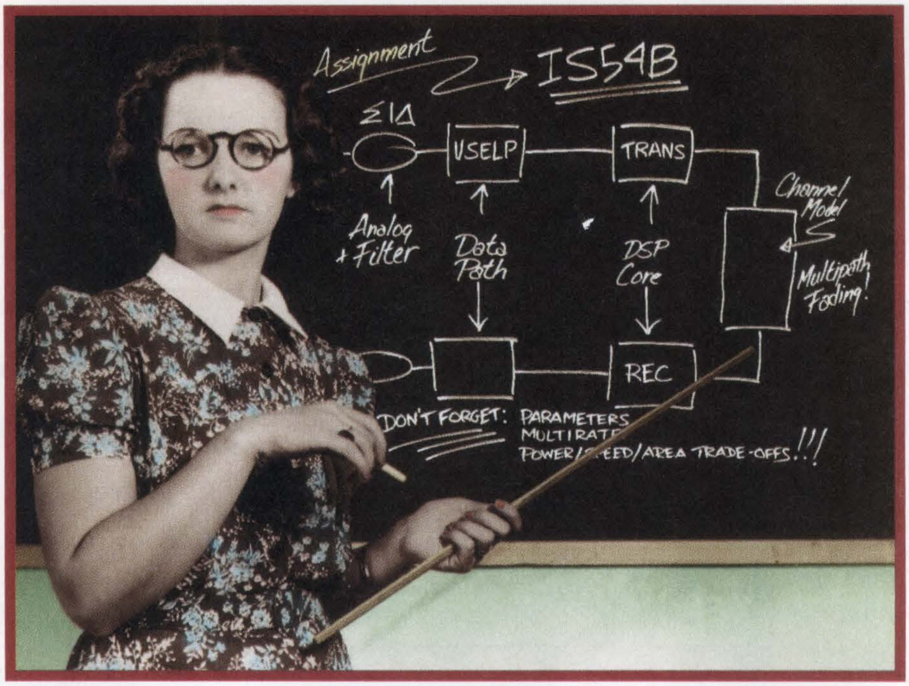

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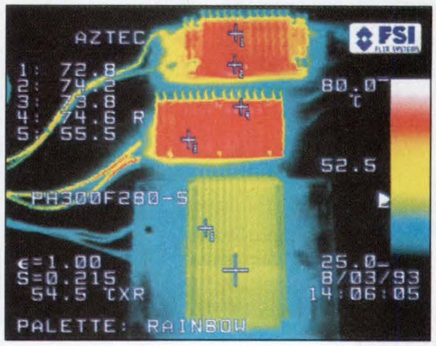
CIRCLE NO. 34

Make a note

We inadvertently neglected to include Lambda in our Special Report on distributed power (*EDN*, April 28, pg 54). You can contact the Melville, NY, company at (516) 694-4200. Or **Circle No. 357**.

It was also Lambda, not Calex, that should have gotten the credit for the thermogram that ran on pg 56; we've reprinted the photograph here.



Debugging debate

I read your article titled "Teaming a logic analyzer with a debugger provides advantages to both tools" (*EDN*, January 20, pg 21). Excellent discussion.

I've spent about eight of my 12 years interested in embedded-system development tools. I've written and hacked around with ROM monitors for x86, 680x0, AMD29K, and MIPS. And I've written a full source-level debugger (COFF-based) for the same processor families. I've also built some trivial x86-based hardware that integrates some basic logic-analyzer stuff with the monitor for firmware debugging (address/data comparators, etc), and I've found that to be very useful.

I most definitely agree with you that the logic-analyzer/debugger combination is an extremely effective development environment. As a matter of fact, referring to the "Looking ahead" box in your article, my debugger has the "dashed line from the logic analyzer to the workstation." This feature isn't needed every day, but when there's a tough bug lurking, it is definitely a priceless capability. This can actually be a simple interface if it can be assumed that the logic analyzer can dump its trace data in some columnar format.

One of the nice things about the logic-analyzer/debugger combination is that the logic analyzer is not a piece of equipment that needs to be purchased solely for the person writing the drivers or really low-level firmware. It was probably already purchased for the hardware-design group and has been used for a lot more than just setting complex breakpoints. My point is that if the debugger "knows" a little about the logic analyzer, then there is no need for an emulator; hence, no need to put out the extra money (which is not trivial). Emulators don't come cheap, especially for the high-speed stuff.

I see only two real deficiencies in the logic-analyzer/debugger approach. As you mentioned in your "Cons" list, the logic analyzer is helpless when it comes to the CPU's cache, and, along those lines, it can also be a bit confusing to deal with any kind of bus-unit prefetch (even without cache). In the case of cache, instruction/data access can occur without the logic analyzer's knowing it, and, in the case of prefetch, instructions can be fetched (seen by the logic analyzer) but not executed.

If you have a decent ROM monitor, then some of the cons mentioned can also disappear. If the trigger of the logic analyzer is tied into the same interrupt as the ROM monitor's UART, then it can look just like a breakpoint. Also, with a decent analyzer/debugger interface, you can debug at the high-level-language level.

This leaves me with two questions, and I'll follow them with the only answers I can think of.

1. Why aren't more CPU manufacturers providing a debuggable processor? All that is really needed is the equivalent of the "watch trap" on the MIPS R4000—the ability to set a data breakpoint. What is so difficult about that? I know the 386 has one, but why hasn't it become a generic feature like the breakpoint trap? I've always assumed that it must be cost, but I would also think that a feature like that could swing a potential customer from one CPU to another. I don't get it.

2. How can so many emulator companies stay in business? About the only

advantage an emulator gives a firmware developer that a logic analyzer has trouble with is the fact that the logic analyzer is "external" to the processor; hence, it can't handle internally cached memory accesses. But based on the added cost, that doesn't justify the need for an emulator anyway. Usually, you can disable cache in some way to allow the logic analyzer to do its thing. My only conclusion here is that the hardware is not designed with debugging in mind. Some very simple up-front work can usually save a lot of debugging time down the road. As a result, when the time comes to put on some firmware, somebody has to dish out some big bucks.

My conclusion is that there really isn't much consideration for debugging at the hardware-design stage. Even if the addition of a debug UART and some RAM is out of the question for the actual production version of the hardware, facilities for a debug daughterboard can easily be justified in most cases. Then, depending on the energy level of the designer, the debug daughterboard can even eliminate the need for the logic analyzer in many cases. For a minimal cost (especially when compared to the price of an emulator or a logic analyzer), you can add real-time trace, multiple- state breakpointing, convenient logic analyzer connections (if still necessary), high-speed download, etc—the works!

Ed Sutter
AT&T Bell Labs

More to know about ATM...

The article in *EDN's* March 3 issue (pg 66) on the ATM convergence-sublayer and physical-interface devices was excellent. We are very excited about these products because they provide a complete, intelligent ATM termination when coupled to our ATMizer Architecture. The author of the article, however, was unaware of our ATM offerings.

The ATMizer is the first reprogrammable ATM cell-processing architecture. The heart of the architecture is an on-chip RISC-based ATM-processing unit, which allows customers to quickly and easily update their products as the

ATM standard evolves. Users simply download new code to accommodate changes in the ATM standard or congestion-control algorithms. The ATMizer performs segmentation and reassembly and all layer operations up to 155 Mbps. It supports all ATM adaption layers and can process up to 64,000 virtual channels of voice, data, and video simultaneously.

The ATMizer Architecture is available as a single chip or as an ASIC architecture to complement products mentioned in *EDN's* article. In addition, this flexibility and performance is being used to address the open issues raised in the Special Report, including congestion control, LAN emulation, and traffic management.

Tony Stelliga
Vice President
Telecom Products Div
LSI Logic
Milpitas, CA

...and more

EDN has received some updated information for the ATM Special Report (March 3, pg 66). The correct phone number for AMCC is (800) 935-2622. Also, if you want to contact the ATM Forum, the company reports that it has moved to new quarters in Foster City, CA; phone (415) 578-6860.

Cooling hot µPs

We believe your coverage of the hot microprocessor problem ("Cooling hot microprocessors," *EDN*, January 20, pg 40 and "Shrinking devices put the squeeze on system packaging," *EDN*, February 17, pg 41) has shortchanged your readers in two areas. Among the fastest-growing techniques for cooling board-mounted processors and other hot devices is the use of low-profile, tape-mounted heat sinks and extremely compressible thermal-gap-filling materials.

The world's leading supplier of double-sided thermal tapes and thermal gap fillers is Chomerics Inc (Woburn, MA). In both thermal and adhesion properties, our Thermattach tapes have set the performance standards in PC markets worldwide. A unique, stable, thermally conductive, pressure-sensitive adhesive (PSA) makes them suitable for even high-temperature applications—where traditional acrylic PSAs have a tendency to lose their grip.

In thermal gap fillers, we believe our Cho-Therm T274 and A274 materials are the only commercially available, easy-handling alternatives to bags of fluorocarbon liquid.

In general, we found both articles well-written and informative, but their exclusion of references to Chomerics' thermal interface products left us somewhat overheated.

Robert A Rothenberg
Director of Market Development
Chomerics Inc
Woburn, MA

New number

ATI Technologies Inc, which was discussed in the article entitled "New chips give PCs TV-quality video" (*EDN*, March 31, pg 42), has a new telephone number. Contact the company at (905) 882-2600.

Call a different number

We appreciate the reference to our Video Integration Processor and our OEM customers, S3 and Xtec. We are great IBM chip designers, but alas, we are not part of IBM Microelectronics. We are part of IBM's Networking Hardware Div in Research Triangle Park, NC. Your readers will want to call a different number from the one listed in your manufacturers' listing to get information on the processor, which is offered as an OEM product. Readers can call (919) 543-7976.

George M Henke
Program Manager
IBM Networking Systems

Listen up

In response to Mr Green's (Unilever Research) "Listen to your computer" letter: We incorporated an audio monitor in our Texas Instruments seismic data processor (computer) in 1959. We drove a speaker from a signal counted down from the AOC (Acquire anOther Command), the signal that initiated the next instruction fetch from memory.

We originally incorporated it to tell us when the computer had halted. How many times have you sat in from of that infernal machine, wondering if it were caught up in some endless loop, with no visible means of telling? In our case, we also had almost every operation blinking one or more lights, but the lights only told us *something* was happening. By having a predefined low-frequency tone generated, we could know if the machine had stalled. Also, if it did get into a loop, the constant, repeating sound would indicate a failure.

Our (and the customer's) operators soon got to know the sequence of tones generated in different portions of the programs and could tell what was going on and how long a particular program could be expected to continue.

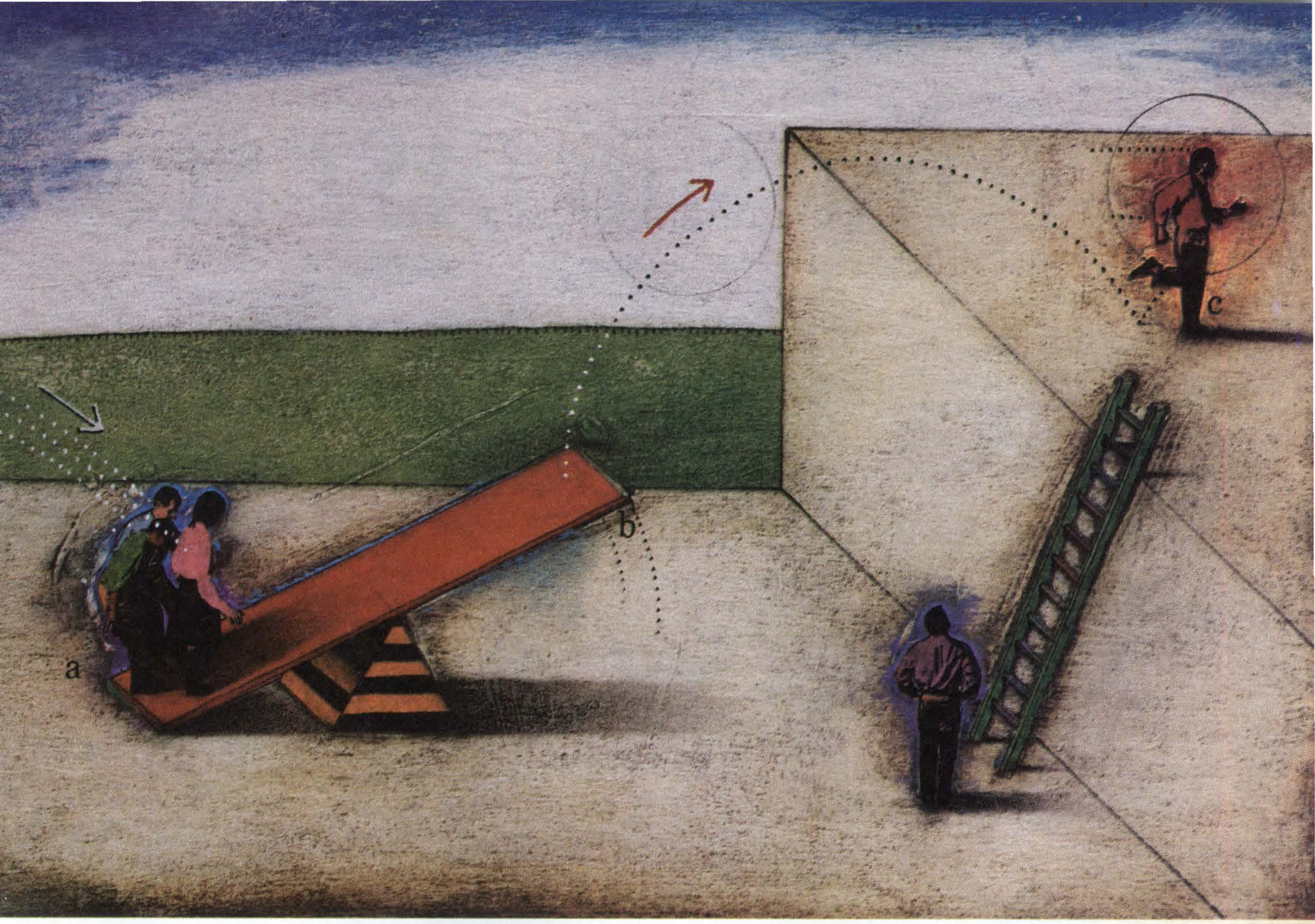
Needless to say, but I will anyway, our smart-as-a-whip engineers found a way to make whimsy of this capability. During the 1964 Christmas season, I went back to the system-checkout area and heard Christmas music playing away. Upon investigating, I found it emanating from my computer. Those clever people had found a way to write programs that would exercise that sound monitor.

"Listening to your computer" is not as strange as it sounds. For what it's worth, and thanks for your column.

John Hargett
Agoura Hills, CA

Sound off

"Signals & Noise" lets you express your opinions on issues raised in the magazine's articles or on any engineering-related topic. Send letters to *EDN*, 275 Washington St, Newton, MA 02158; fax (617) 558-4470. Or use *EDN*'s bulletin-board system at (617) 558-4241: From the Main System Menu, enter ss/soapbox, then W to write us a letter. You'll need a 2400-bps (or less) modem and a communications program set for 8,N,1. *EDN* reserves the right to edit letters for clarity and length.



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Technological proof of innocence: Part 1

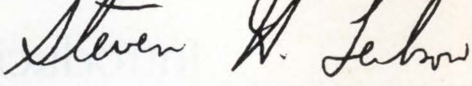
Life has certainly gotten more complicated since I moved to Massachusetts two and a half years ago. The fables about terrible Boston driving and parking don't tell half of the story. I've even received a parking ticket for parking in a place I've never been at 2 AM on February 27. Now I'm sure that my car and I were both safe, warm, asleep, and at home on that night, at that time.

On the designated day, I went to the town that issued the parking ticket and pleaded my case. Now, we're very efficient in Massachusetts. You don't appeal parking tickets in court; you go straight to the collector of fees, taxes, and fines. The person behind the desk listened to me, got up, looked on the computer, and assured me that it was indeed my car that was illegally parked.

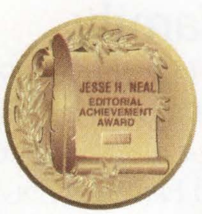
I asked to see the ticket. Once again, the clerk got up, rummaged in a closet for 10 minutes and returned with the actual ticket. It was my license number on the ticket all right, if you ignored the unreadable third character. However, the ticket identified the car as a brown Ford, and I drive a gold Toyota. "Aha," I said, "that's not my car!" The clerk replied, "Hey, you can't expect the officer to get everything right at 2 in the morning. That's your license-plate number. Pay up."

This experience prompted me to start thinking about the use of technology to prove innocence. Governments have plenty of technology for pressing guilt upon us. We could use some defense.

In the movie "Back to the Future," Doc Brown returns from the future in his time-traveling DeLorean with a bar-coded license plate. It seems to me that we ought to seriously consider adopting license plates that carry bar codes or other machine-readable identification in addition to human-readable numbers. Police could use scanners to read these plates at a distance with better accuracy than what I experienced from my brush with the parking patrol.



Steven H Leibson
Editor-in-Chief



*Note: This is the latest in a series of articles on C-Quad engineering. C-Quad (or C^4) stands for the **convergence** of **computer**, **consumer**, and **communications** technologies.*

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1990 Certificate, Best Series
1987, 1981 (2), 1978 (2), 1977, 1976, 1975

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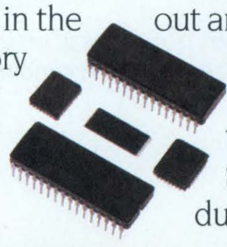

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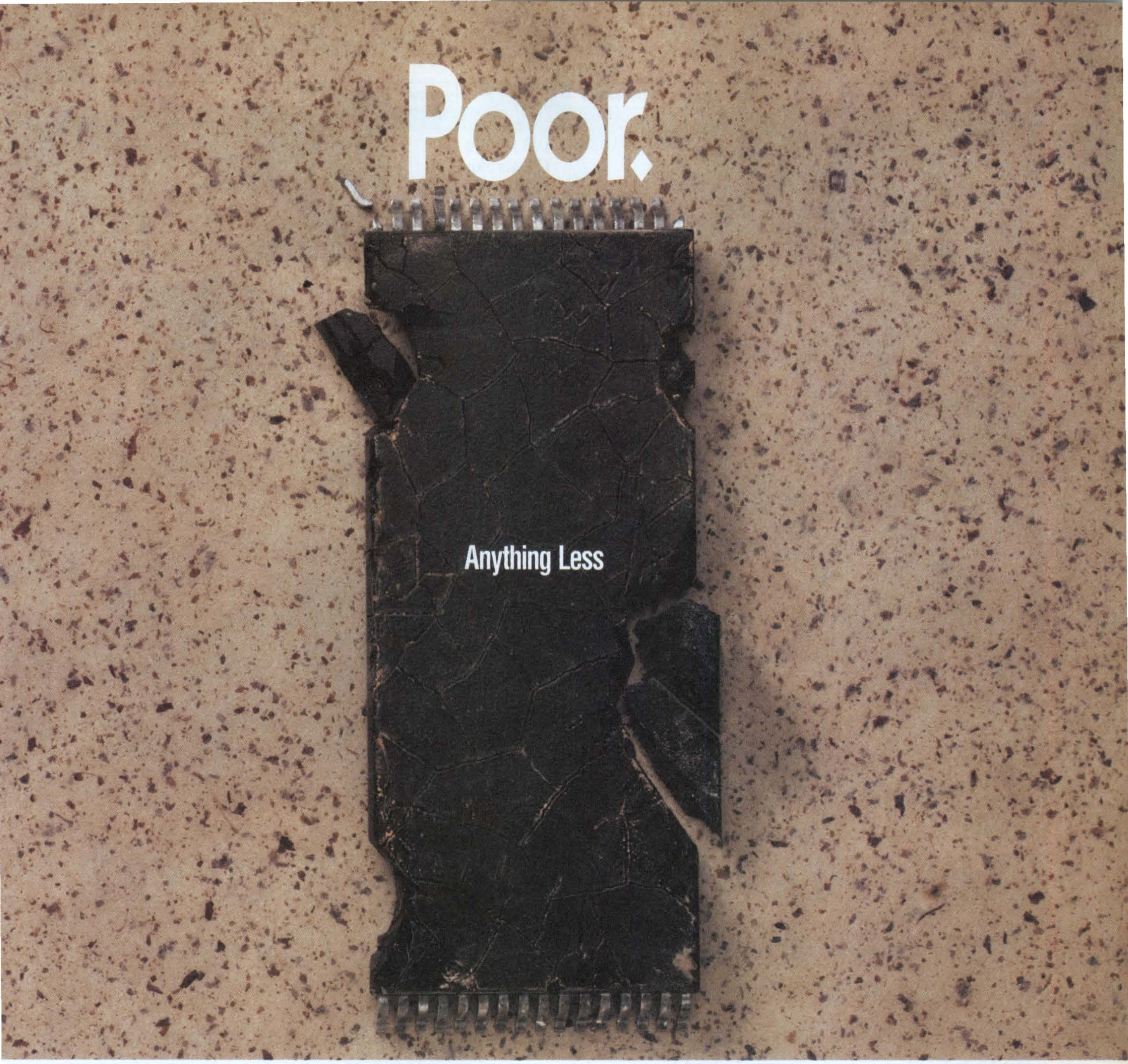

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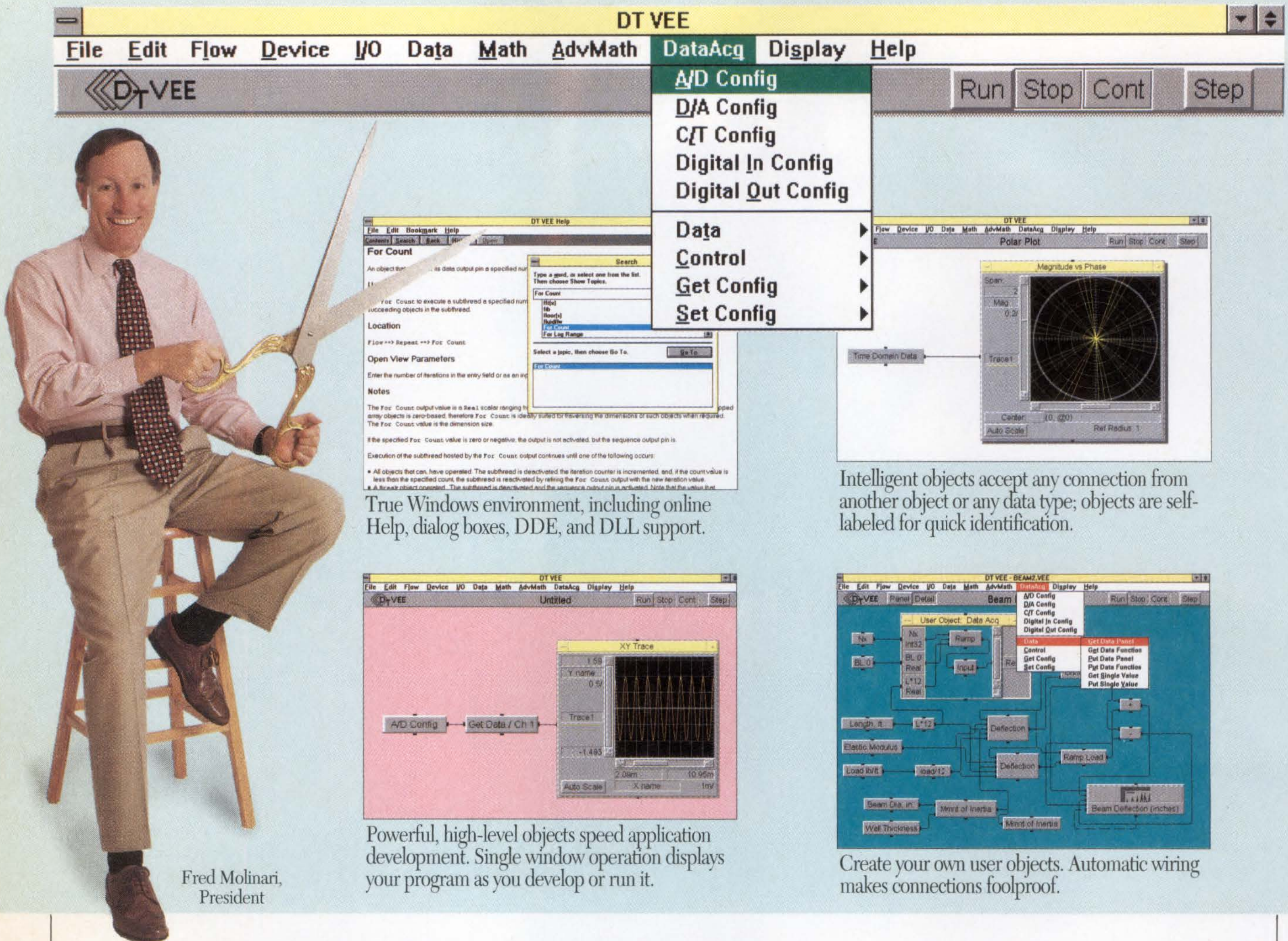

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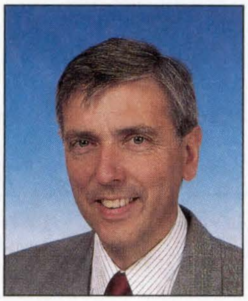
CIRCLE NO. 66

System simulation embraces real-time control prototyping

BRIAN KERRIDGE, Senior Technical Editor



Today's control-system simulators employ graphical modeling tools, automatic coding, and DSP "hardware-in-the-loop" simulation to narrow the gap between conceptual design and product reality.

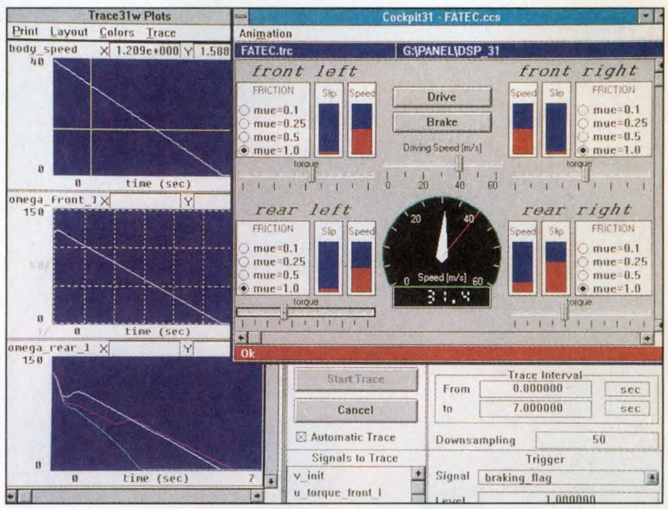
System simulation is an important design activity in control-engineering applications. But, while most simulation products focus on conceptual issues, relatively few readily assist you in implementing a design. The few products that do support implementation incorporate direct links to development hardware and, overall, form integrated rapid-prototyping systems.

The key feature of rapid-prototyping systems is fast transfer of a slow-motion "off-line" simulation running on a PC or workstation, to a "real-time" simulation running on dedicated DSP hardware. These simulators rely heavily on block diagrams for model building and automatic coding for generating source code, usually in C. These two features alone are instrumental in achieving rapid prototyping and, in consequence, enable a low-cost route to design iteration—an unavoidable feature of control-engineering developments. In practice, automatic coding takes only a few seconds, and, for a system that's already initialized, you can complete one design iteration in a matter of minutes. **Fig 1** outlines the design-flow path of a typical rapid-prototyping system.

Simulating real-time control systems requires that you model not only a controller's functions, but also the dynamics of the plant you want to control. Such a system offers you the rapid-prototyping options of a simulated controller driving a real plant, an embedded real-time controller driving a simulated plant, or a mixture of the two. **Fig 2** illustrates these options.

No matter which option you choose, rapid-prototyping systems offer substantial timesaving benefits—from concept to reality—and other important benefits. Simulator vendors cite examples of 50% cuts and more in project time (see **box**, "Rapid prototyping shortens DC-X space-vehicle development").

As a prelude to adopting one of the prototyping options, it's useful first to transfer



dSpace's MS-Windows Trace and Cockpit software allow you to gather and analyze data and adjust control parameters while running a real-time simulation. This example shows a vehicle antilock-braking-system simulation in progress.

an off-line simulation of the controller and the plant to a DSP test bed. This step moves the application closer to reality and allows you a first opportunity to examine critical timing in your overall control strategy. For example, at this stage, sampling-time parameters you build into your models may force elements of the simulation to require service in synchronism with the system

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clock. Failure to meet model sampling times means your DSP test bed ceases to represent a real-time model and implies your system needs more DSP power.

In practice, monitoring software forewarns you of a system crash and, even before attempting a real-time simulation run, indicates when a system cannot execute in the sampling times you specify. Increasing system power is simply a matter of installing more DSP hardware, and all systems include multiprocessing expansion for this purpose.

Specifying model sampling times in relation to real-system response times requires modeling experience and lets you trade off modeling integrity and complexity with DSP power. For example, it would be overkill to specify a 10-msec sampling time for a model of a valve that takes several minutes to change state. On the other hand, a 10-msec sampling time is grossly inadequate for a crankshaft-sensor output on a high-performance auto engine.

DSP emulates control or plant

Of the main prototyping options, using a DSP test bed to emulate only a controller and its I/O functions is a fast route to proving a control concept and refining control parameters. However, using DSP to emulate a plant, or "hardware-in-the-loop" simulation, offers major development-time reductions.

Overall, the arrangement allows you to test the validity of controller electronics well in advance of the availability of the live plant. This feature is significant because most control-engineering applications accommodate the vagaries of a real-world environment, thus increasing the likelihood of design flaws appearing late in a development cycle.

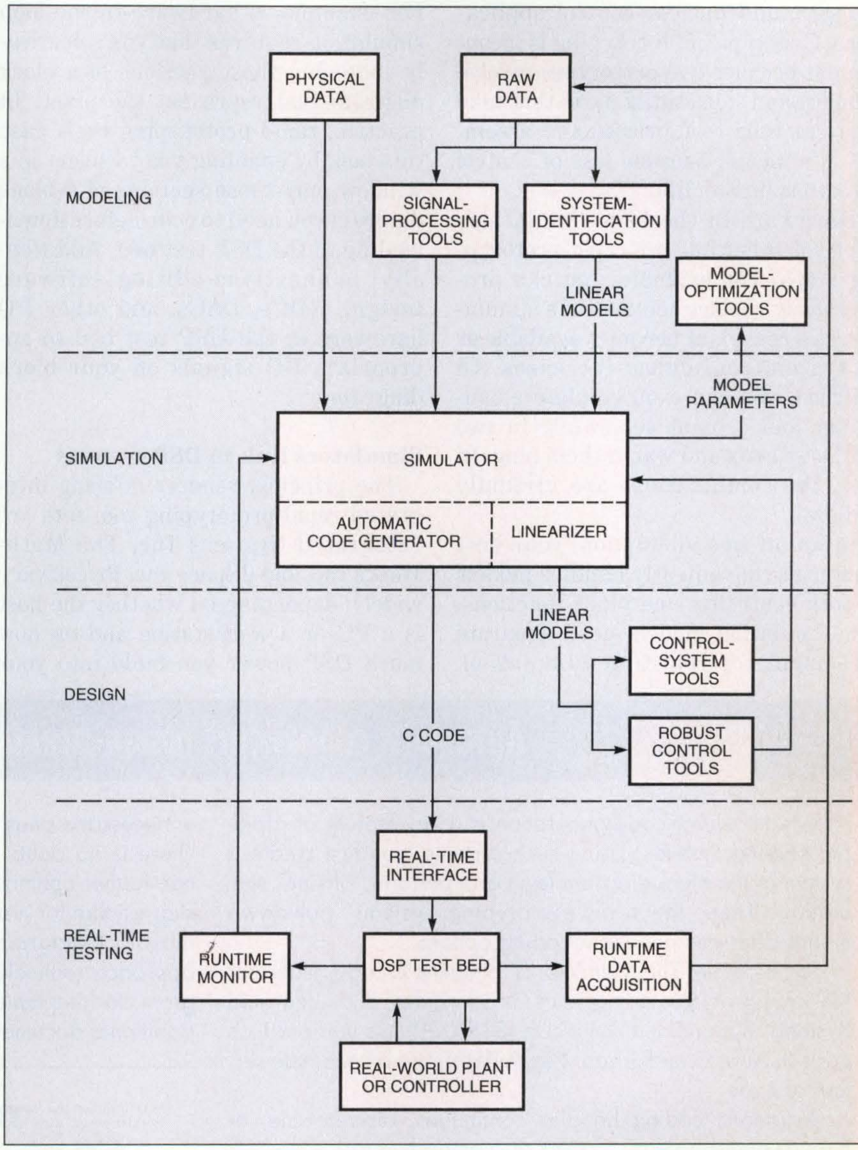

Fig 1—Rapid prototyping systems form an integrated environment for modeling, simulation, design, and real-time testing. (Courtesy dSpace Inc)

In addition, performing live-plant prototyping at the outset is often inconvenient and unsafe, as in automotive,

LOOKING AHEAD

MS-Windows is increasingly the preferred design-tool environment for engineering applications, yet Integrated Systems' $Matrix_x$ remains for the time being a workstation-only product. The company is planning to add a multiprocessing TMS320C40 card to its RealSim low-cost PC test-bed product line. Additionally, Integrated Systems and Mentor Graphics will soon support links between $Matrix_x$ and Mentor's System Design Station/QuickSim2 simulator. This combination will allow you to cosimulate a system using the RealSim DSP test bed to simulate a plant and QuickSim2 to emulate control. QuickSim's VHDL model outputs will provide a fast route to custom-built controller chip sets.

The MathWorks plans further graphical-user-interface enhancements to some of its toolbox options, including its system-identification tool, as part of a general effort to attract engineers, as well as academics, to use these products.

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in-flight, and nuclear-control applications. This type of prototyping is inconvenient because live prototypes involve complex and substantial parts that take many months to fabricate and assemble. It's unsafe because loss of control threatens human life.

Hardware-in-the-loop simulations offer you other interim rapid-prototyping steps. For example, you can progressively replace sections of a simulation as a real plant becomes available or as system confidence increases. In addition, you can even emulate a controller and a plant separately in two DSP test beds and watch them play. In fact, the combinations are virtually endless.

In an off-line simulation, your host computer conveniently handles models of both controller and plant functions, but simulation models need separate treatment for real-time simulation. For example, a hardware-in-the-loop simulation requires that you selectively code only those sections of a block diagram that represent the plant. In practice, rapid-prototyping tools ease this task by enabling you to select in a window only those sections of a block diagram you need to code before downloading to the DSP test bed. Additionally, connections-editing software assigns ADCs, DACs, and other I/O hardware in the DSP test bed to appropriate I/O signals on your block diagram.

Simulators link to DSP systems

The principal vendors offering integrated rapid-prototyping tool sets are Integrated Systems Inc, The MathWorks Inc, and dSpace Inc. Prices vary widely, depending on whether the host is a PC or a workstation and on how much DSP power you build into your test bed. Typically, though, expect to pay $15,000 for a very basic setup to more than $50,000 for a "power-user" setup. Automatic coding software adds $10,000 or more to these prices (see **box**, "Automatic coding cuts design-iteration time").

Integrated Systems' Matrix_x modeling, simulation, analysis, and code-generation tools run on Sparc and VAX workstations and combine with the company's RealSim series of real-time hardware test beds. In addition, Matrix_x requires runtime software that includes a graphical user interface, cross compilers, device drivers, and an Ethernet interface. RealSim comes in a range of configurations from a 486-based portable PC with a single TMS320C30 processor card to a high-end Multibus chassis that accommodates one to 11 i860s. A wide range of I/O options includes ADCs, DACs,

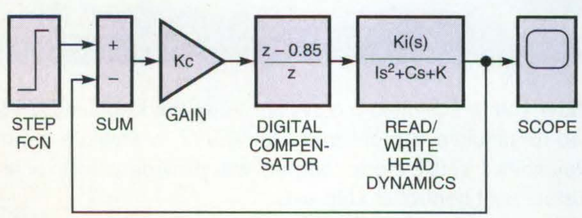
AUTOMATIC CODING CUTS DESIGN-ITERATION TIME

Automatic source-code generation is a key feature of rapid-prototyping systems. Using such systems, you first create a system at the block-diagram level and perform "off-line" simulation. Then, the rapid-prototyping systems' pull-down menus offer you automatic-coding options.

For example, The MathWorks' Simulink C-code generator ($9995) gives you a choice of C-code styles, and Integrated Systems' SystemBuild Autocode ($15,000) lets you produce code in Ada, C, or Fortran. **Fig A (b)** shows an example section of code.

Automatic coding handles continuous, discrete-time, or hybrid-control systems. Coders also embody a task scheduler to prioritize separate operations in multirate systems, for example, acting on sensor inputs before less-frequent user inputs.

Vendors maintain that automatic coding produces code optimized for speed in real-time operation. For example, the coder unrolls loops, minimizes functions calls, and removes unnecessary ones and zeros from numeric computations. There is no doubt that experienced real-time programmers can further optimize code for target processors, but vendors suggest that for most applications you modify your system at the block-diagram level and recode automatically. This approach routinely maintains the status of your block diagram and implementation at a current level and eliminates additional documentation-control work.



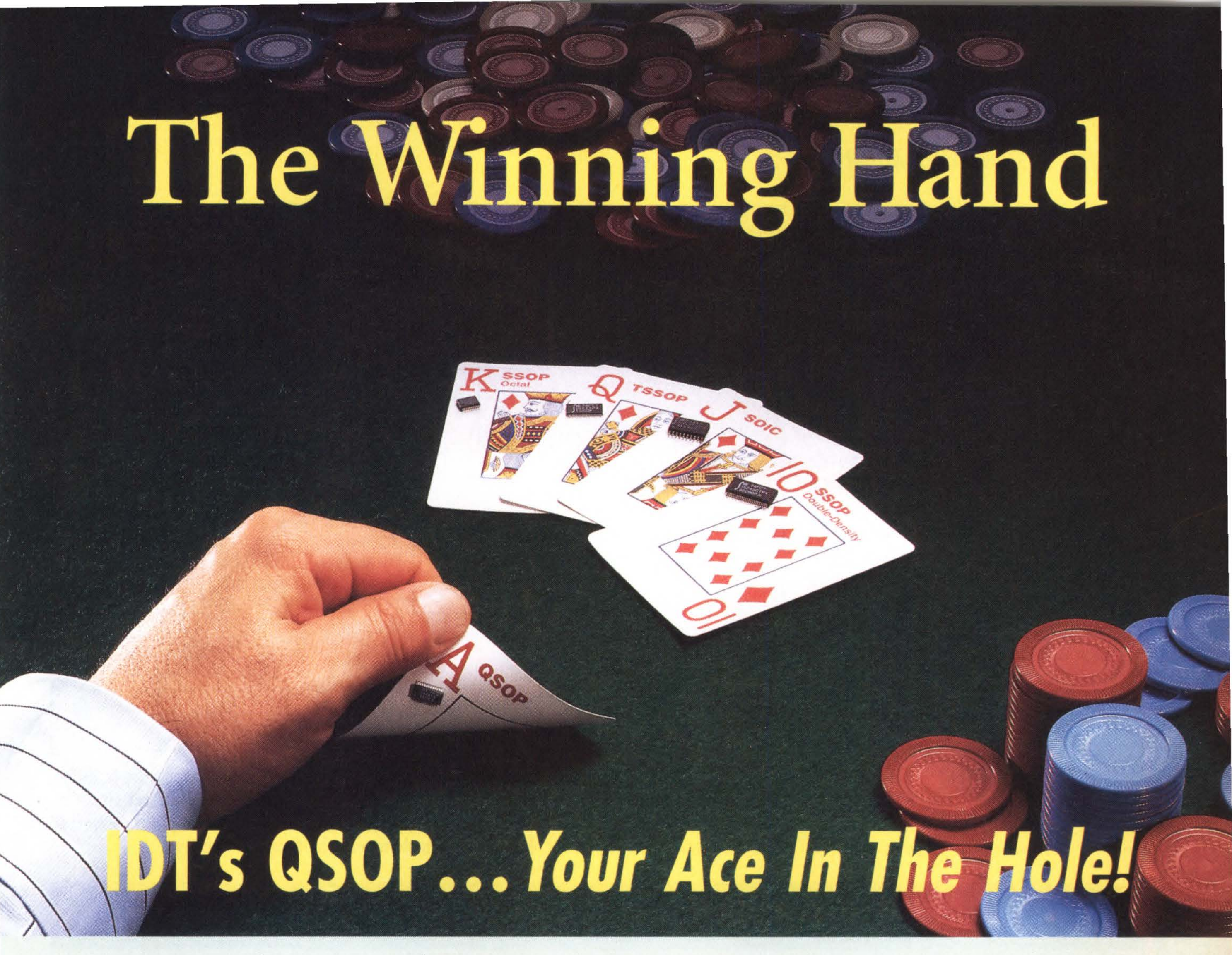
(a)

```
/* Function to compute block outputs */
static void simBlockOutputs (x, u, S)
     double * x;
     double * u;
     SimStruct * S;
{
     double *B = ssGetBlockIO (S); /*Block inputs and outputs */
     double *P = ssGetBlockParam (S);   /* Block parameters */

     /* Step input: Step Fcn */
     if (ssGetT(S) < P[0])
          B[0] = P[1];
     else
          B[0] = P[2];

     /* Transfer function: Read/Write Head Dynamics */
     B[1] = x[1];

     /* Summing junction: Sum */
     B[2] = B[0] - B[1];

     /* Gain block: Gain (Kc) */
     B[3] = P[5] * B[2];

#ifndef SINGLE_RATE
     if (ssGetSampleHitEvent(S, 0))      /* Is it a sample hit? /*
#endif
     {

          /* Transfer function: Digital Compensator */
          B[4] = P[6] * x[2] + B[3];
     }
}
```

(b)

Fig A—The block diagram (a) represents a disk-drive head and controller, modeled using The MathWorks' Simulink library functions. The C-code-generation tool transforms the block diagram to the source-code listing (b), which is comprehensible and well-commented.

The Winning Hand



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SOIC 20-pin	SO	1.270	133.1	12.8	7.5	2.5
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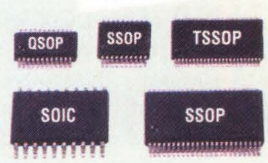

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and digital and resolver-synchronous I/O. The product range also includes the DocumentIt software package, which automatically produces a textual description of a system, including tables, hierarchies, and subsystem lists.

The MathWorks does not produce a real-time test bed for its Matlab analysis and Simulink simulation software, but the company supports hardware from dSpace Inc. dSpace offers a wide range of PC plug-in DSP, memory, and I/O cards. Using these cards, you can site your DSP hardware within your PC host computer if it has enough expansion slots. For workstation and already-full PC hosts, the company offers Ethernet-linked, 6- and 20-slot expansion boxes and a dc-powered 7-slot ruggedized version for field use.

dSpace's DSP cards include single-processor TMS320C30 and TMS320C40 models and a 4-processor TMS320C40 version. The company also provides essential software to process source

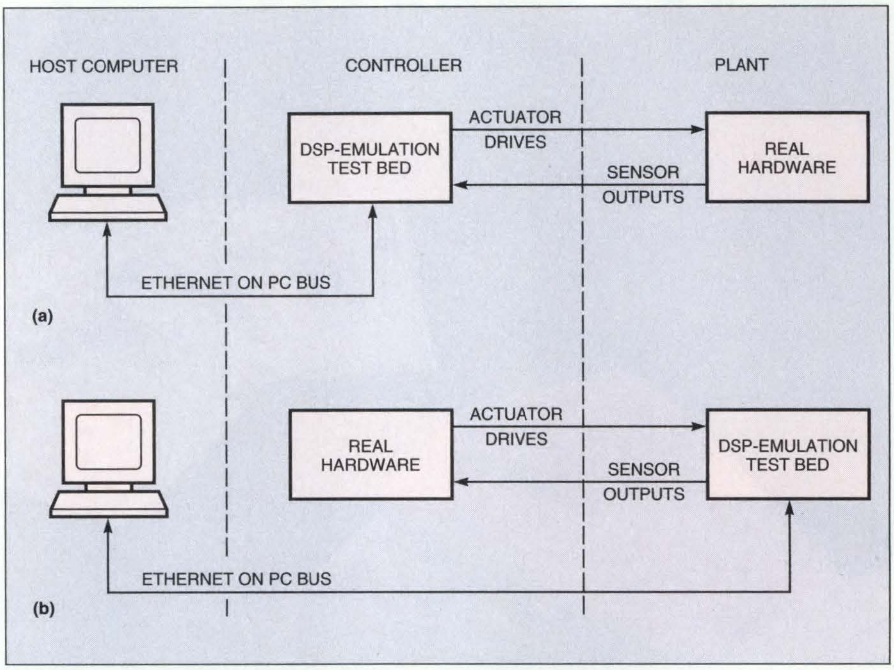


Fig 2—Real-time simulation offers you two main options: (a) using DSP hardware to mimic an embedded controller that interfaces with actuators and sensors in a real plant situation and (b) using DSP hardware to simulate the dynamics and I/O signals of a plant connected to a real embedded controller, known as "hardware-in-the-loop" simulation.

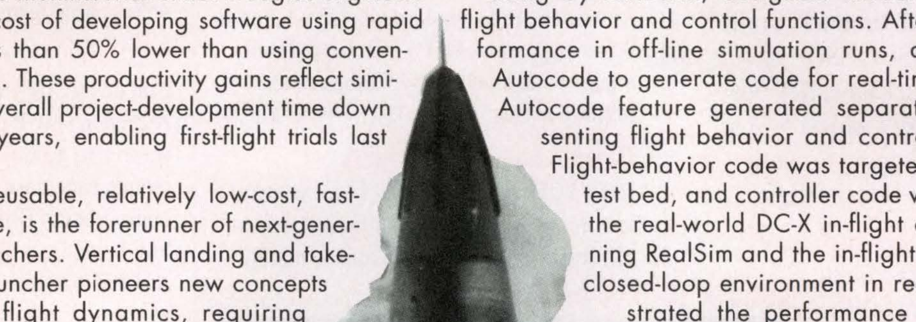
RAPID PROTOTYPING SHORTENS DC-X SPACE-VEHICLE DEVELOPMENT

Using Integrated Systems' Matrix$_x$ rapid-prototyping tools, McDonnell Douglas Aerospace engineers developed flight-control software for the Delta Clipper Experimental (DC-X) space vehicle in 10 months. McDonnell Douglas engineers estimate that the cost of developing software using rapid prototyping is less than 50% lower than using conventional hand-coding. These productivity gains reflect similar reductions in overall project-development time down to less than two years, enabling first-flight trials last August.

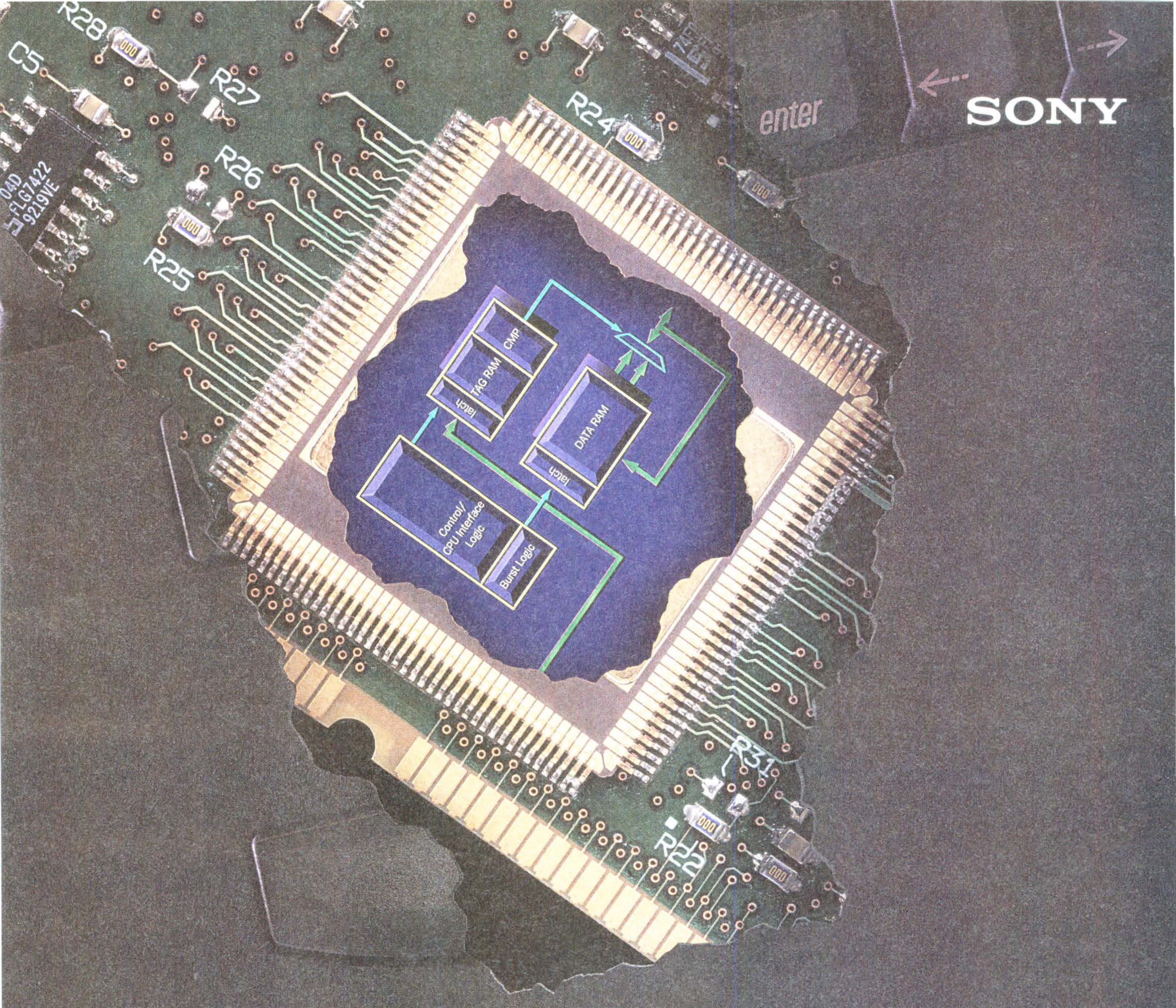
The DC-X, a reusable, relatively low-cost, fast-turnaround vehicle, is the forerunner of next-generation satellite launchers. Vertical landing and take-off of the DC-X launcher pioneers new concepts in space-vehicle flight dynamics, requiring equally innovative control algorithms. Particularly demanding is the independent control of four rocket engines on gimbals that maneuver the launcher.

McDonnell Douglas designers used Matrix$_x$ tools to develop around 30,000 lines of Ada code for the flight- and navigation-control algorithms. In addition to Matrix$_x$'s core SystemBuild modeling and simulation tool, the company's designers used Interactive Animation, Autocode, and the RealSim test bed for real-time simulation.

Using SystemBuild, designers modeled the DC-X's flight behavior and control functions. After refining performance in off-line simulation runs, designers used Autocode to generate code for real-time testing. The Autocode feature generated separate code representing flight behavior and controller functions. Flight-behavior code was targeted to a RealSim test bed, and controller code was targeted to the real-world DC-X in-flight computer. Running RealSim and the in-flight computer as a closed-loop environment in real time demonstrated the performance of the overall control strategy far in advance of firing up real rocket engines.



Using automatic coding to produce 30,000 lines of Ada code, McDonnell Douglas achieved a 2-year concept-to-launch time with the DC-X space vehicle.



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code from Simulink's code generator. This software includes a real-time interface, a C compiler, the Trace data-acquisition tool, and the Cockpit graphical instrument panel. Trace and Cockpit are essential to maintaining graphical contact with any real-time simulation.

Trace allows real-time analysis of any controller and provides hardware-in-the-loop simulation without disturbing system operation. The tool also allows you to record and continuously plot variables in the DSP processor's on- and off-chip memory. In practice, you can later analyze Trace records using Matlab and compare data with results from off-line simulation as a means of enhancing your models.

Cockpit allows you to animate controlling and monitoring a real-time simulation. You can design your own panel using a standard library of knobs, sliders, and meters. In operation, the software periodically updates meters and displays but, more important, allows you to adjust control settings, which, in turn, modify control parameters on the fly during a real-time simulation.

One of the limitations of hardware-in-the-loop simulations is that the plant simulator may not be able to mimic sensor output signals accurately in high-speed systems. For example, in advanced automotive-engine management, it takes around 2-μsec timing resolution to sense 0.1° angular rotation at 8000 rpm. Also, even seemingly mundane signals representing slow-changing temperature and pressure may require much higher bandwidth noise elements to preserve the integrity of the overall simulation. In general, there's no chance that the main DSP plant simulator can also generate such time-critical outputs, and, therefore, the system needs additional hardware.

dSpace has recently introduced such a product, DS2301, which uses six TMS320C31 processors and 16-bit DACs. The DS2301 autonomously produces six high-speed output waveforms with edge resolutions below 1 μsec. C code programs the signal-generation algorithms, which are calculated on-line. dSpace calls the technique "direct digital synthesis" (**Ref 2**). EDN

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1. Hanselmann, Dr Herbert, "Hardware-in-the-Loop Simulation as a Standard Approach for Development, Customization, and Production Test," Society of Automotive Engineers, Paper No. 930207, March 1993.
2. Hanselmann, Dr Herbert, "DSP-based Automotive Sensor Signal Generation for Hardware-in-the-Loop Simulation," dSpace Application Note, February 1994.

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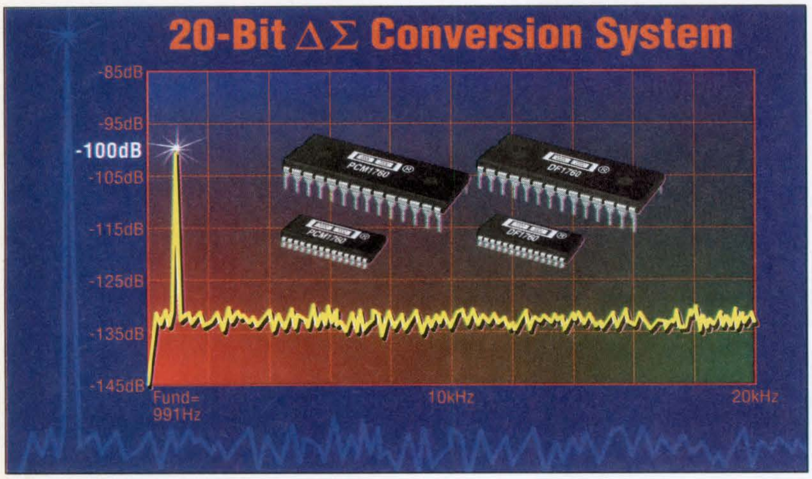

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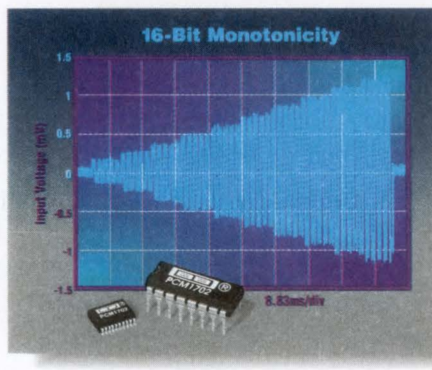

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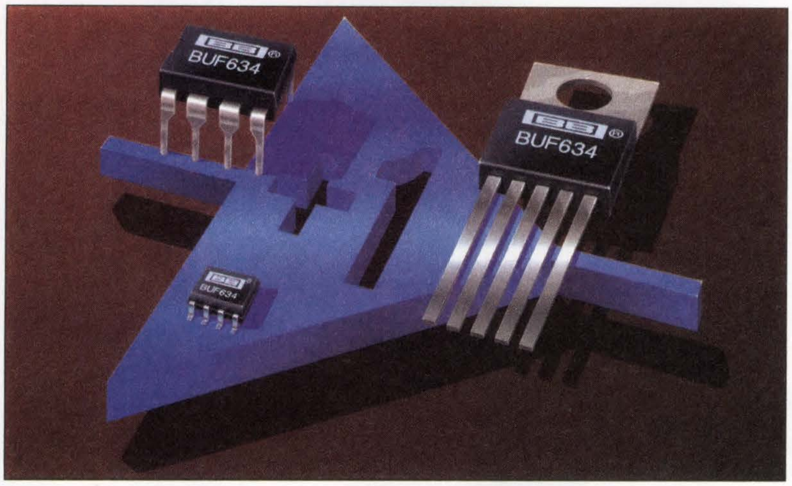

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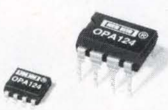

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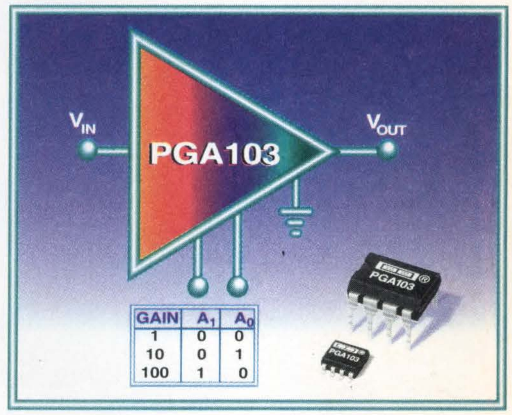

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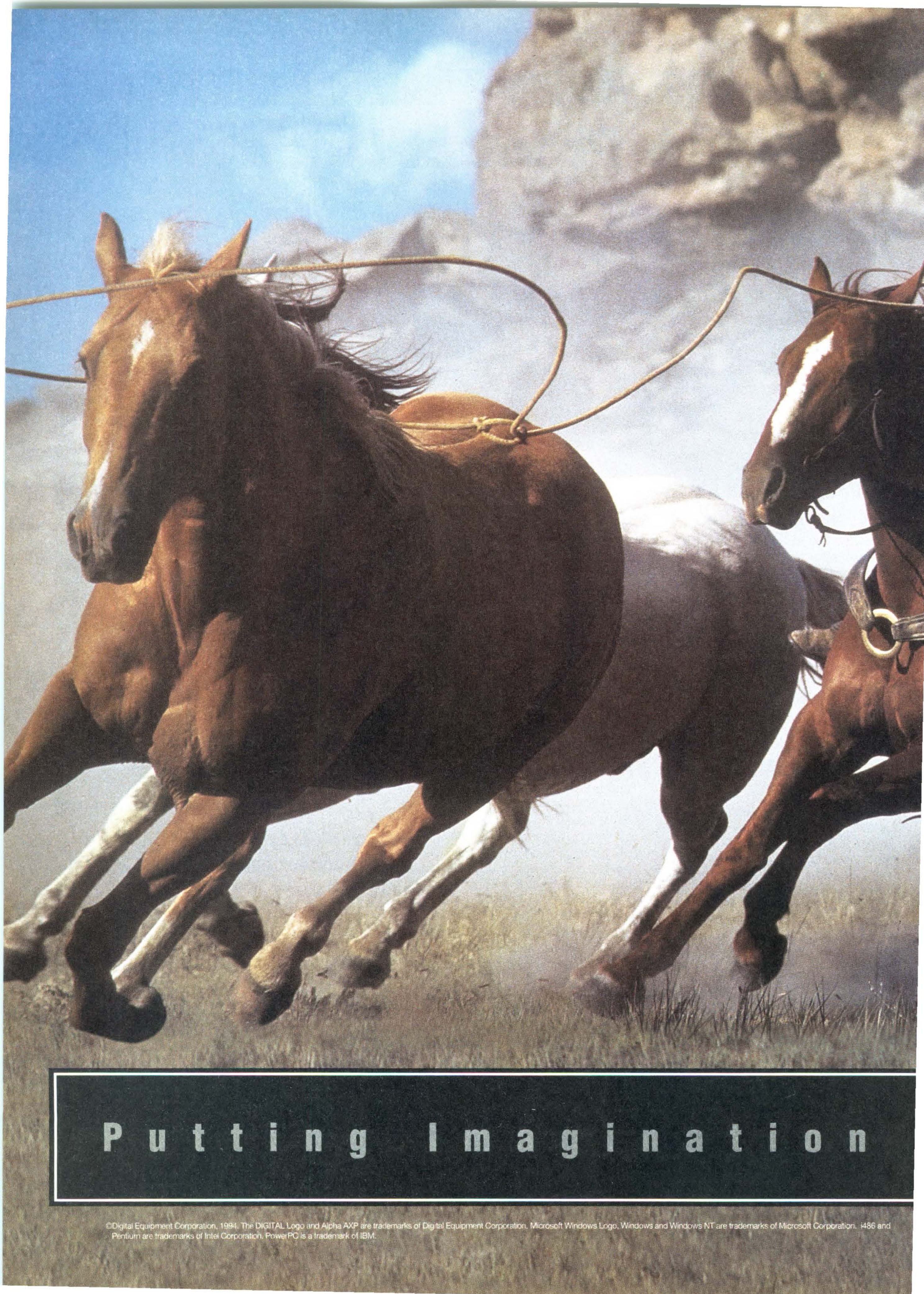
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12-BIT ADCs

Now may be the time to upgrade your 8- and 10-bit systems

ANNE WATSON SWAGER, Technical Editor

A substantial list of low-cost 12-bit devices with competitive power and speed makes upgrading 8- or 10-bit systems seem almost foolproof. However, ensuring 12-bit accuracy means reevaluating many other aspects of a design.

Plunging prices of 12-bit monolithic ADCs with sampling rates from 10 kHz to 2 MHz are dramatically reducing the cost of 12-bit designs and breaking the barriers to upgrading 8- and 10-bit systems. Just two years ago, the price of a 100k-sample/sec ADC was around \$15 to \$20. That ADC today costs as little as \$5 to \$10, and 500k-sample/sec converters cost \$10 to \$20 (**Fig 1**).

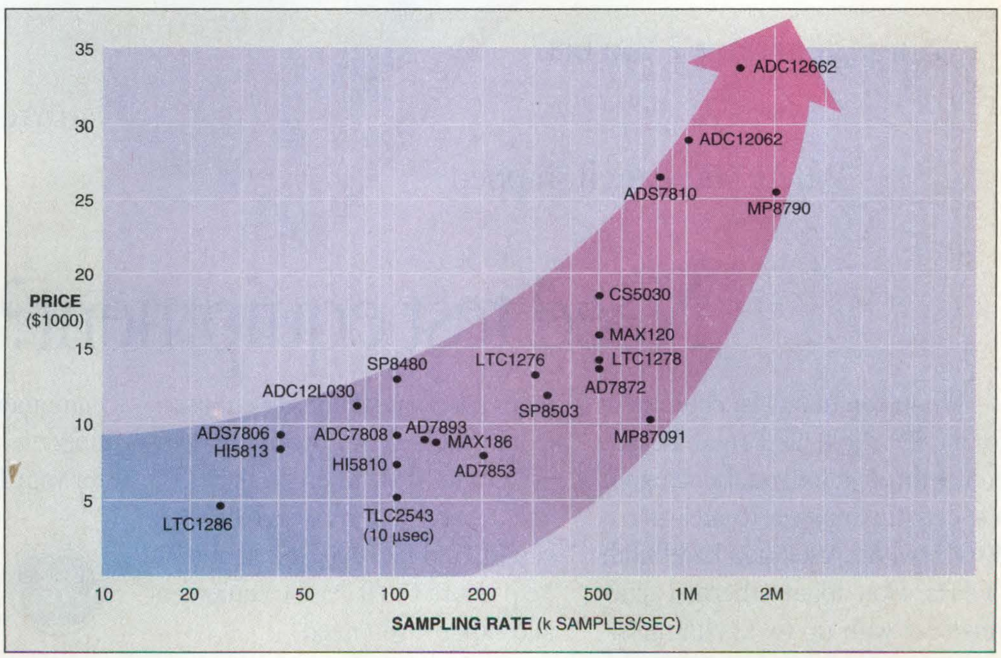
However, price isn't the only parameter in decline; power is also going down, even for ±10V systems. Although some of these ADCs require dual supplies, most operate from a single 5V supply; some, from 3V supplies. A number of these ADCs include devices with very-low-power consumption of 12 to 50 mW and can implement a complete power-down.

While concentrating on cost and power, the designers of these converters continue to increase speeds above 500 kHz and, in many cases, integration. Attaining even higher speeds at low cost is a high priority on many companies' agendas for the immediate future. (See **box**, "Looking ahead: above and beyond 12-bit, 10-μsec ADCs.")

Table 1 lists just a sample of some companies' 12-bit, 10-kHz to 2-MHz converters. By the latest count, Analog Devices' division in Ireland alone produces 12 12-bit ADCs and their various permutations. Burr-Brown's ADS78xx family currently comprises eight members (four of which are 12 bits and four of which are 16-bit pin-compatible partners), and the company will add more members by year-end.

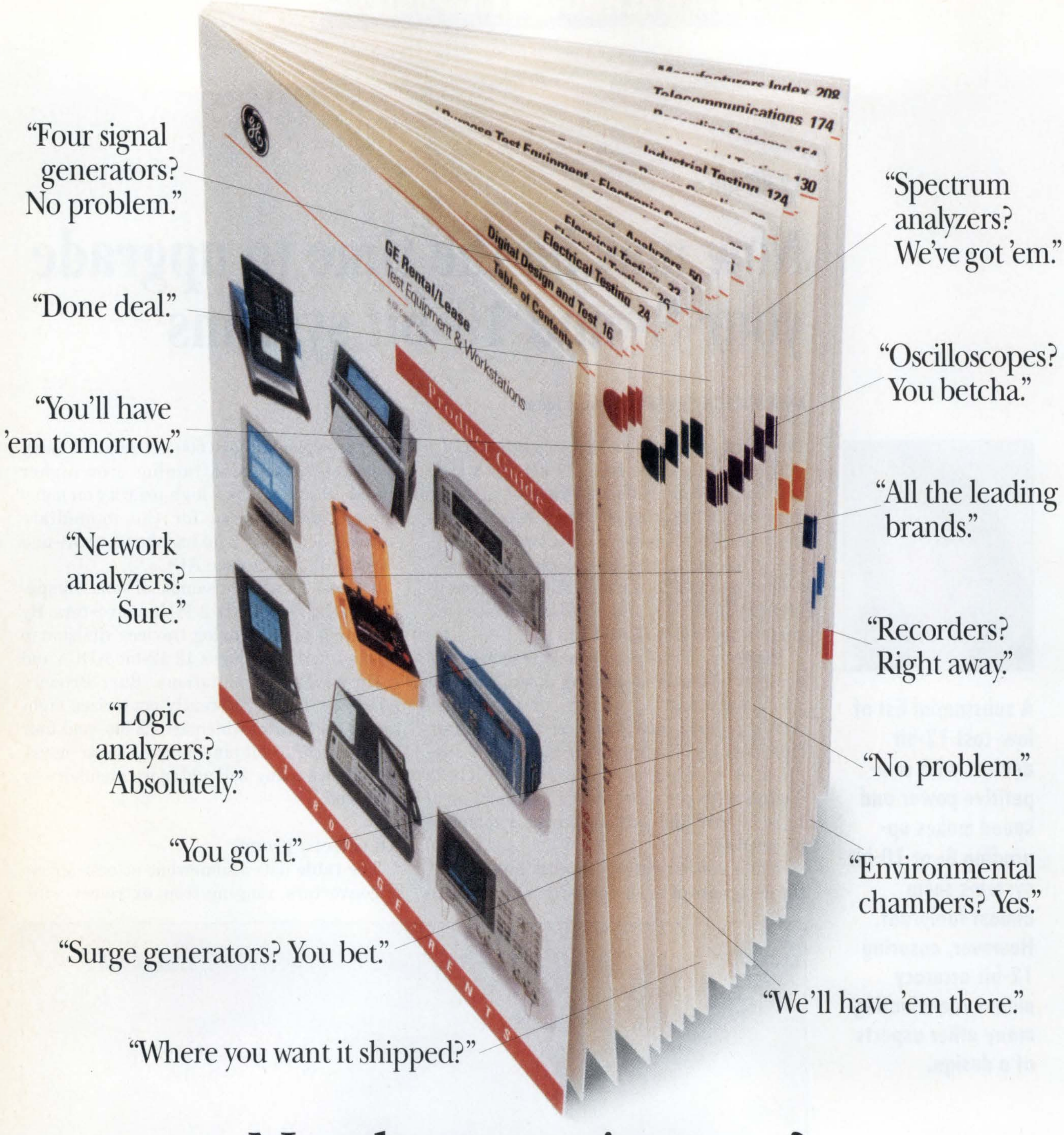
An eclectic group

The **table** lists a somewhat-eclectic group of converters, ranging from extremely sim-



Daniel Guidera

Fig 1—The costs of 12-bit ADCs with 10-kHz to 2-MHz sampling rates have dramatically decreased within the last few years. However, prices dramatically increase as the ADCs go even higher in frequency, easily passing the \$100 mark at around 5 MHz.



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12-BIT ADCs

ple, stand-alone types to highly integrated ICs, such as National Semiconductor's LM12434 and 12438. These converters offer much more than core-ADC and data-acquisition-IC features such as multiple input channels. Each also incorporates an instruction RAM, an event sequencer, and a 32-word conversion FIFO buffer. These recently introduced 3 to 5.5V power-supply versions also have a power-down output.

The **table**'s converters also feature a variety of input ranges, power-supply voltages (although single 5V is the most common), package sizes, and variations on or departures from the familiar successive-approximation-register (SAR) architecture.

Inputs range from 0 to 2V and ±2.5 to ±10V, sometimes irrespective of supply voltage. For example, Analog Devices builds its 789x SAR-type converters on a BiCMOS process so that these 5V ADCs can handle inputs of ±10V. The process allows for the input to go 10V above the supplies. ADCs built on standard CMOS processes usually have much more restricted input ranges that can go only 0.3V above the supply, for example.

These converters are also much smaller than their 12-bit predecessors. With just a few exceptions, virtually all of the converters come in both DIP and SOIC packages, and two fit into 8-pin SOICs: Analog Devices' 125k-sample/sec AD7893, and Linear Technology's 12.5k-sample/sec 1286/98. Maxim also

TABLE 1—REPRESENTATIVE LOW-COST 12-BIT ADCs

Vendor	Part no.	Speed	Key features	Power (mW max)	No. of pins	Price (1000)
Analog Devices Circle No. 301	AD7893/6	125 k samples	Serial, 5V supply, T/H 0 to 2.5 to ±10V input range	50	8	$9
	AD7890	125 k samples	Eight single-ended channels, serial, power-down, T/H, reference	50	24	$10.20
	AD7853 AD7858	200 k samples	3 to 5V operation, serial, pseudo-differential inputs (7853), four pseudo-differential or eight single-ended inputs (7858), power-down	18 (V_{DD}=3V)	24	$8 $11.20
	AD7891 AD7892	500 k samples	5V supply, T/H, 25-ppm reference, eight channels (7891), parallel and serial, power-down, selection of input ranges	75	44 24	$16.15 $13.60
Burr-Brown Circle No. 302	ADS7806	40 k samples	Parallel and serial, power-down, 0 to 4 to ±10V input ranges, 5V supply	35	28	$9.25
	ADS7808	100 k samples	Serial, 0 to 4 to ±10V input ranges, 5V supply	100	20	$9.25
	ADS7810	800 k samples	Parallel data with latches, ±10V input range, S/H, clock, reference, ±5V supply	250	28	$26.50
Crystal Semiconductor Circle No. 304	CS5030 CS5031 CS5032	500 k samples	Reference (1 ppm 5030 and 5031; 60 ppm 5032); ±5V supply; input ranges of ±2.5 (5030 and 5032) or 0 to 5V (5031); flexible serial, parallel, and byte interface	70	24	$18.50 $18.50 $15.90
Harris Semiconductor Circle No. 306	HI5810 HI5812 HI5813	100 k samples 50 k samples 40 k samples	5 or 3.3V (5813) supplies, S/H, parallel	42 10 (typ) 9	24	$7.30 $6.95 $8.41
Linear Technology Circle No. 307	LTC1286/98	12.5 k samples	2.7 to 9V supplies, S/H, 2-channel multiplexer or differential inputs, serial	0.5/1.2	8	$4.65
	LTC1273 LTC1275 LTC1276	300 k samples	5 or ±5V supplies, S/H, 25-ppm reference, clock, parallel, inputs of ±2.5 (1275), 0 to 5 (1273), and ±5V (1276)	75 (typ)	24	$14.09 $12.65 $13.20
	LTC1278	500 k samples	5 or ±5V supply, 5-mW power-down with instant wake-up, S/H, reference, clock, parallel	75	24	$14.35 to $17
Maxim Integrated Products Circle No. 308	MAX186 MAX188	133 k samples	Eight input channels, reference, (186), 5 or ±5V supplies, power-down, serial	12.75	20	$8.95 $8.45
	MAX120 MAX122 MAX176	500 k samples 333 k samples 250 k samples	5 and –15V supplies, T/H, 25- to 40-ppm references, ±5V input range, parallel (120 and 122), serial (176)	315 315 172	24 24 8 or 16	$16 $12 $13.20

table continued on pg 70

packages a number of its converters in shrink SOICs.

SAR architecture rules

The SAR architecture still dominates in this 10-KHz to 2-MHz frequency range. However, these SAR converters come in two implementations: those that implement the conversion using an R-2R ladder network and those that use switched-capacitor structures. Texas Instruments uses a patent-pending switched-capacitor SAR architecture to enable the TLC2543 to achieve 12 bits with a small die size (and thus the $5.25 price). The converter also uses a fuse-blown technique, which prevents the need for expensive laser trimming.

Whether a converter is based on an R-2R or switched-capacitor structure doesn't change the way you communicate with and use the ADC. However, these structures, along with whether the converter uses BiCMOS or CMOS technology, do change power consumption, input range, and performance of internal references.

For example, those ADCs striving to achieve the lowest possible power consumption generally have a CMOS, switched-capacitor architecture. In general, these ADCs' internal references aren't as accurate as R-2R or switched-capacitor types built on bipolar or BiCMOS processes. Some companies use BiCMOS processes because they allow IC designers to build better references. ADCs built on BiCMOS processes, such as the AD7892/1, LTC1273/5/6, and MAX120/122, feature internal references with precision characteristics of 25 ppm/°C compared with 50 to 60 ppm/°C for other internal references.

But it doesn't always take a BiCMOS process to produce accurate reference performance. Crystal Semiconductor set out to produce a 12-bit SAR converter with absolute accuracy, including the drift characteristics of the reference. The company uses E^2PROM-based calibration circuitry in the CMOS CS5030 and 31 to produce a 2.5V on-chip reference with an extremely low temperature coefficient of 1 ppm/°C reference. The designers also brought the reference to an output pin, so you can use the reference for the rest of the system.

As these converters' sampling rates approach 1 MHz, other architectures start appearing, such as the 2-step conversion methods common to high-speed hybrid ADCs. Both National Semiconductor's and Micro Linear's 1-MHz devices use this method. Soon, some 200-kHz oversampling converters will also debut. (See **box**, "Oversampling converters quietly creep up in sampling rate.")

Differentiating features

The group of low-cost 12-bit ADCs often have competitive dc and ac specifications, including differential nonlinearity specs around ±1 LSB with no missing codes. (However, some converters' differential nonlinearity can be as high as ±4 LSBs.) Integral nonlinearity can vary from 1 to 2.5 LSB, and minimum S/N-ratio-plus-distortion (SINAD) specs can be as high as 72 dB with –80-dB THD.

TABLE 1—REPRESENTATIVE LOW-COST 12-BIT ADCs *(continued)*

Vendor	Part no.	Speed	Key features	Power (mW max)	No. of pins	Price (1000)
Micro Linear Circle No. 309	ML2230	31.5 μsec	μP compatible, 12-bit plus-sign ADC, S/H, ±5V supplies	400	24	$7.65
Micro Power Systems Circle No. 310	MP3275 MP3276	15 μsec	16 channels, 50V overvoltage protection, serial (3276) and parallel	200	68	$24.09 $24.68
	MP87091/92	750 k samples	5V supply, parallel (7091) or serial (7092), T/H	200	28	$10.37
	MP8790 MP8791	2000 k samples	Parallel, T/H, 5V supply	225	52 28	$25.58 $23.26
National Semiconductor Circle No. 311	ADC12L030/2/4/8	73 k samples	12-bit plus-sign, self-calibrating, 3.3V operation, T/H, 2-, 4-, and 8-channel multiplexers	15	16 to 28	From $11.80
	ADC12062 ADC12662	1000 k samples 1500 k samples	2-channel multiplexer, S/H, low-power standby mode, parallel	75 200	44	$25.50 $29.30
	LM12434/38	140 k samples	12-bit plus sign system with serial I/O and self-calibration, S/H, RAM, 8-channel multiplexer, FIFO buffer, 3 to 5V supply	34	28	$18.90
Sipex Circle No. 313	SP8480 SP8481	100 k samples	Eight input channels, parallel, S/H, reference	200	28	$13 $14
	SP8503/5/10 SP8603/5/10	333/200/100 k samples	5V supply, bipolar (85xx) and unipolar (86xx), reference, S/H, parallel, clock	125	24	$10 to $12
Texas Instruments Circle No. 314	TLC2543	10 μsec	Serial, 5V supply, S/H, clock, 11 input channels, power-down, built-in self-test	12.5	20	$5.25

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12-BIT ADCs

The issue of absolute accuracy can be bothersome to system designers who are used to using 8- or 10-bit converters in the 100-kHz to 1-MHz range. These lower-resolution converters, including the reference, generally have no trouble meeting a ±1- or ±2-LSB overall accuracy spec.

However, the same isn't true for 12-bit converters and systems. These ADCs' total unadjusted error (TUE)—the sum of integral- and differential-linearity, offset, and full-scale errors—covers a wide range. TUE can be as low as 1 LSB (as it is for Crystal Semiconductor's CS5030/31 with the 1-ppm reference) and as high as around 20 LSBs, roughly equivalent to an accuracy somewhat less than 8 bits (2^N=20 LSBs, where N is the number of bits equivalent to the TUE in LSBs. In this case, N=4.3, so overall accuracy is 12–4.3=7.7 bits). So, many of these ADCs approach 12-bit accuracy only with a system calibration.

Although system calibration is common, reasonable accuracy without calibration is sometimes desirable. For example, to detect voltage drop-off, a battery-voltage monitor may require a resolution of 8 bits, but not quite 12. This means that you can buy an 8-bit converter and calibrate or buy a 12-bit converter with a fairly good TUE. The industrial and commercial grades of Harris Semiconductor's 3.3V HI5813 for example, have respective TUEs of 9 and 13 LSBs, which both equate to around 9 bits of accuracy.

The wide variety of available low-cost 12-bit converters removes many barriers to upgrading to 12 bits. However, finding the right converter with a

OVERSAMPLING ADCs QUIETLY CREEP UP IN SAMPLING RATE

A list of 12-bit converters with speeds exceeding 100 kHz doesn't normally include any oversampling ADCs (also known as delta-sigma and sigma-delta converters). Since their appearance as the latest ADC architecture, oversampling converters have assumed roles in very low-frequency and audio niches. However, companies are working on higher-than-audio-speed oversampling converters and two—one 12- and one 16-bit device—will shortly be available. Crystal Semiconductor also has some high-speed oversampling ADCs in the design phase. These converters will provide communications systems and others with the advantages of the oversampling architecture: a simple antialiasing filter and a low cost.

Analog Devices' 12-bit AD7721 (around $15) has a 210-kHz input bandwidth. The output word rate is 468.75 kHz, and the sampling rate is 30 MHz (set by a nominal 15-MHz external clock.) The ADC features an internal reference, operates from 5V supplies, and accepts a differential input of 0 to 2.5V or ±1.25V. As with other oversampling converters, the on-chip filtering reduces the external anticliasing requirements to first order in most cases.

National Semiconductor's ADC-16071/471 ($19.90 (100)) is a 16-bit ADC with a 192k-sample/sec throughput with 64 times oversampling of 24.576 MHz. (The company presented this part at this year's International Solid State Circuits Conference.) This IC also features a 2V reference and, operating on a single 5V supply, consumes 375 mW max (1 mW max in standby mode). S/N ratio is 94 dB, and THD is 0.0015% at 1 kHz.

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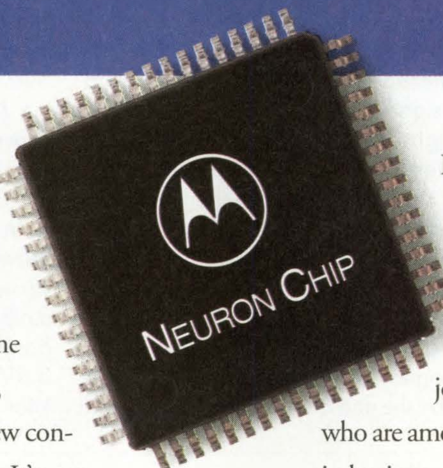

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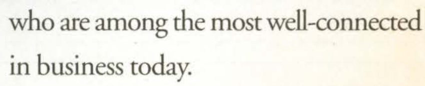

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low price is just a start; many additional factors determine the success of an upgrade. The ADC itself may not be the limiting factor. Remember that users of 10-bit systems expect them to be four times more accurate than 8-bit systems and 12-bit systems to be four times more accurate than 10-bit systems. These expectations have ramifications, some of which go far beyond the converter itself.

An increase in system resolution

LOOKING AHEAD: ABOVE AND BEYOND 12-BIT, 10-MSEC ADCs

The future goal of most 12-bit ADC manufacturers is to increase the speed of their low-cost devices. By year-end, Linear Technology hopes to introduce a 12-bit, greater-than-1M-sample/sec converter; the company is currently evaluating the first silicon for this product. Micro Power Systems is designing devices in the 4- and 5-MHz range.

Numerous 12-bit higher-speed monolithic and hybrid ADCs exist, but they cost significantly more than the devices this article details. Although hybrid ADCs once dominated this high-speed arena, more ICs are beginning to appear. For example, Analog Devices recently introduced the monolithic 5-MHz, 12-bit AD871 ($95), and Harris Semiconductor is working on a lower-power version of its 1W, 12-bit, 3-MHz HI5800 ($85). Also, by the end of this summer, Comlinear Corp will introduce a monolithic 12-bit converter, the CLC950, capable of taking 25M samples/sec ($185 (100)). Signal Processing Technologies also plans to announce a 12-bit, 20-MHz CMOS ADC by the end of the summer. This ADC will join the company's line of bipolar 12-bit ADCs, the 10-MHz SPT7920, 20-MHz 7921, and 30-MHz 7922 ($99 to $161 (1000)).

Hybrid manufacturers include Datel and Comlinear. Datel will soon announce the 10-MHz ADS-119 ($336) and is releasing a new design for the 5-MHz ADS-118 ($238 to $262), a spin-off of the ADS-119 design. After the release of the ADS-119, Datel's 12-bit ADS family will comprise five converters covering a 500-kHz to 10-MHz frequency range. Comlinear's CLC925 and 93X family covers a higher range of 10 to 30 MHz, with prices around $450 to $500.

In other future developments in low-cost 12-bit ADCs, Burr-Brown will continue to expand its ADS family by introducing versions covering 0 to 5, ±2.5, and ±3.3V input ranges; more serial-output devices in 20-pin packages; and the company's first multichannel devices. TI will soon introduce a 3.3V version of the TLC2543 and other 12-bit ADCs for cellular phones.

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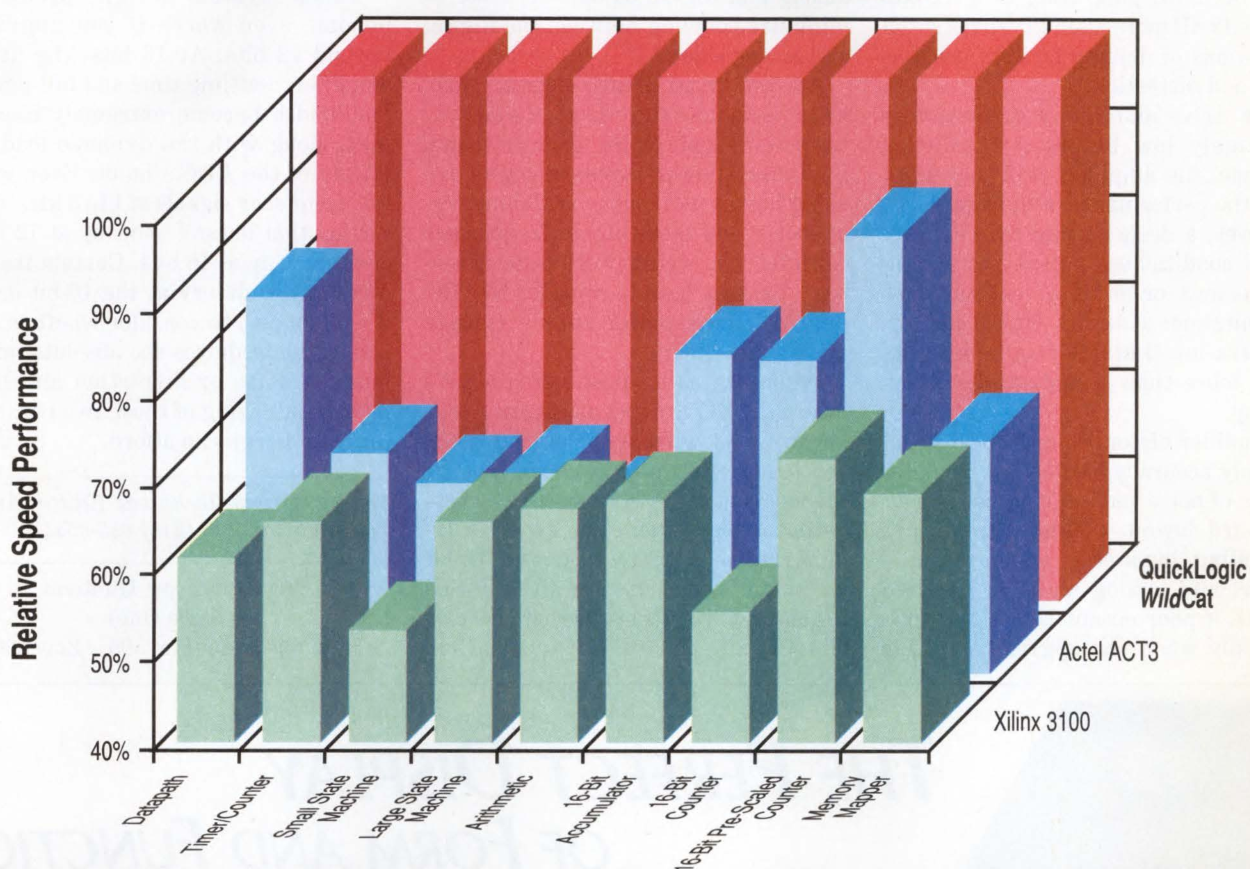

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12-BIT ADCs

requires a reevaluation of signal-conditioning circuits, particularly the drive amplifier. Every 1-bit jump in resolution constitutes a 6-dB increase in S/N ratio. A 12-dB jump from 10 to 12 bits means 12 dB more visibility to potential limitations of driving circuits, such as noise and distortion.

If a drive amplifier's distortion is extremely low before a resolution upgrade, the amplifier probably won't limit the performance of the new ADC. However, a design using the cheapest signal conditioning possible to accommodate an 8- or 10-bit system may show its limitations at 12 bits. Unfortunately, an ultra-low-distortion op amp costs much more than a medium-distortion op amp.

Amplifier distortion and noise aren't the only accuracy limitations. Another source of noise and interference is poor pc-board layout, including improper grounding, bypassing, and coupling of digital and analog signals. The bad effects of poor circuit layout rise dramatically when you upgrade a system from 10 to 12 bits. But, if the initial board design is based on a good layout, you may not need to change it. Good layout practices generally include keeping analog and digital signals separate to minimize coupling between the digital and analog sides.

An even more drastic measure may be to reevaluate the effects of a switching power supply on the analog circuits. Switching-power-supply designs are using higher and higher switching frequencies, and these higher frequencies can affect the accuracy of an analog system. You may have to consider how the quality of the power-supply voltage affects the ADC.

When switching from using a μP's internal ADC to using an external one, be aware of what may happen when you join the ADC and the μP. Despite the fact that the ADC may have 3-state output drivers, you can't expect a 12-bit accurate ADC to produce a 12-bit answer if its outputs are directly tied to some noisy system bus that also carries 10-, 20-, or 30-MHz signals. Consider using digital buffers between the ADC and the μP.

Moving up to 16 bits

These system-design problems become even worse if you upgrade beyond 12 bits. At 16 bits, the drive amplifiers' settling time and full-power bandwidth become extremely important, along with the dynamic loading effects of the ADC's input. Even with low-frequency signals of 1 to 3 kHz, distortion that doesn't show up at 12 bits does show up at 16 bits. Certain trade-offs are mandatory at the 16-bit level; it's important to consider whether the application requires the absolute minimum of noise or distortion and how much minimizing of those two parameters the design can afford. EDN

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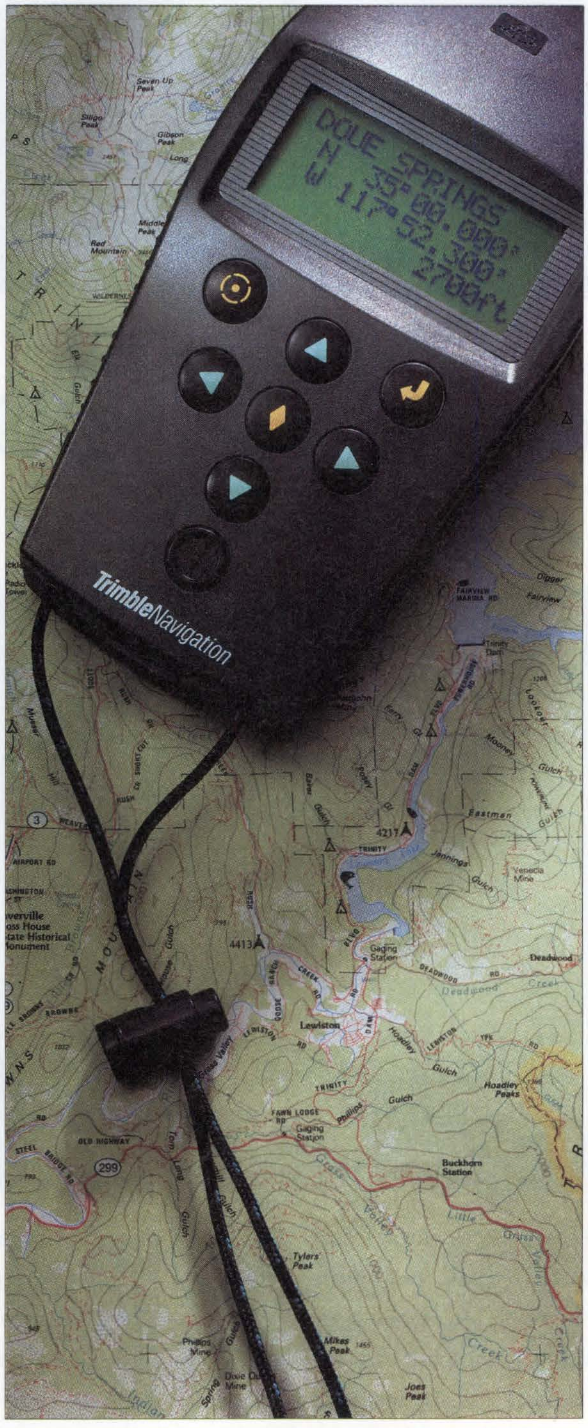

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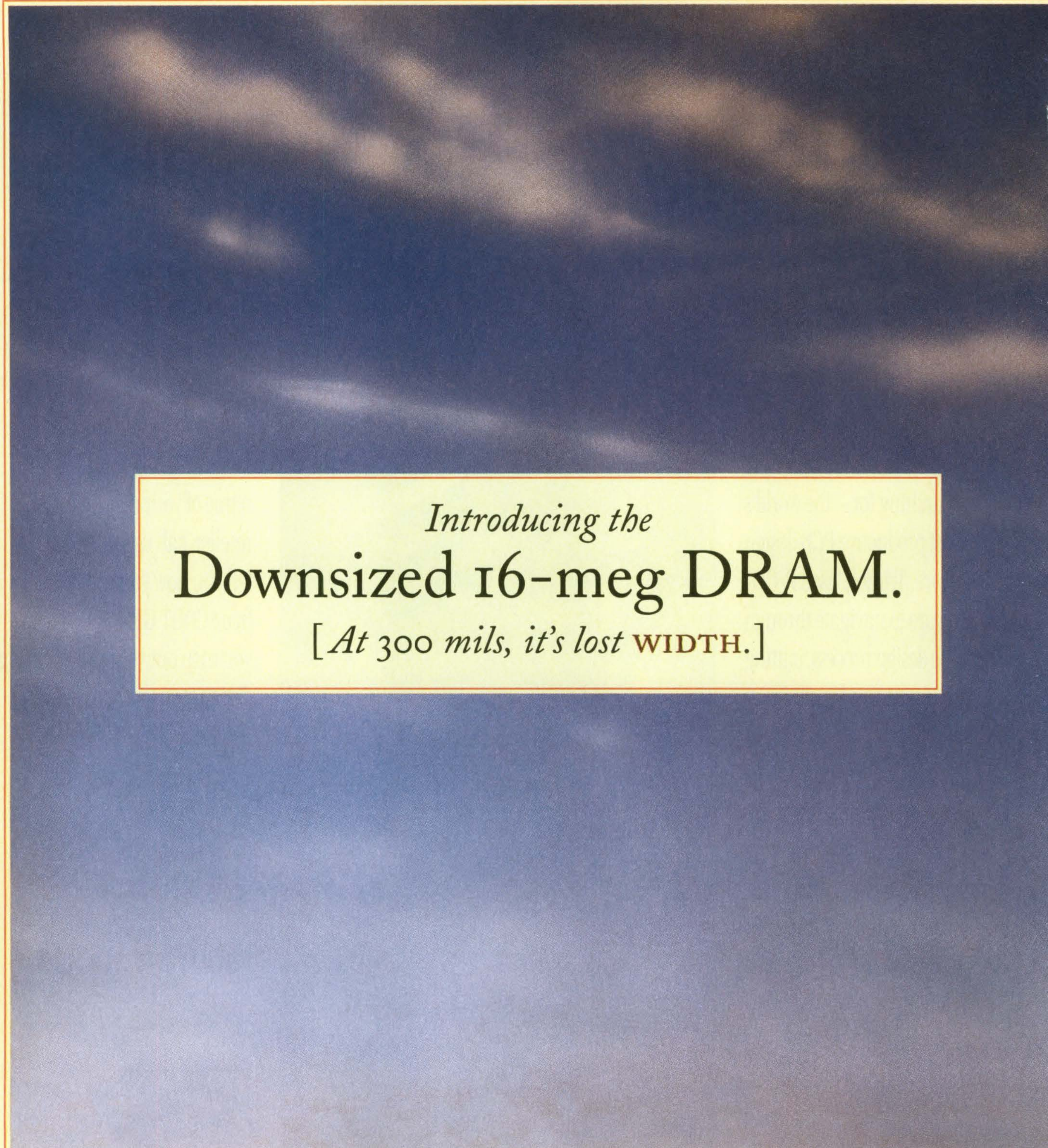

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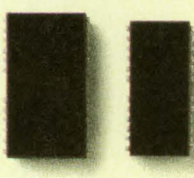

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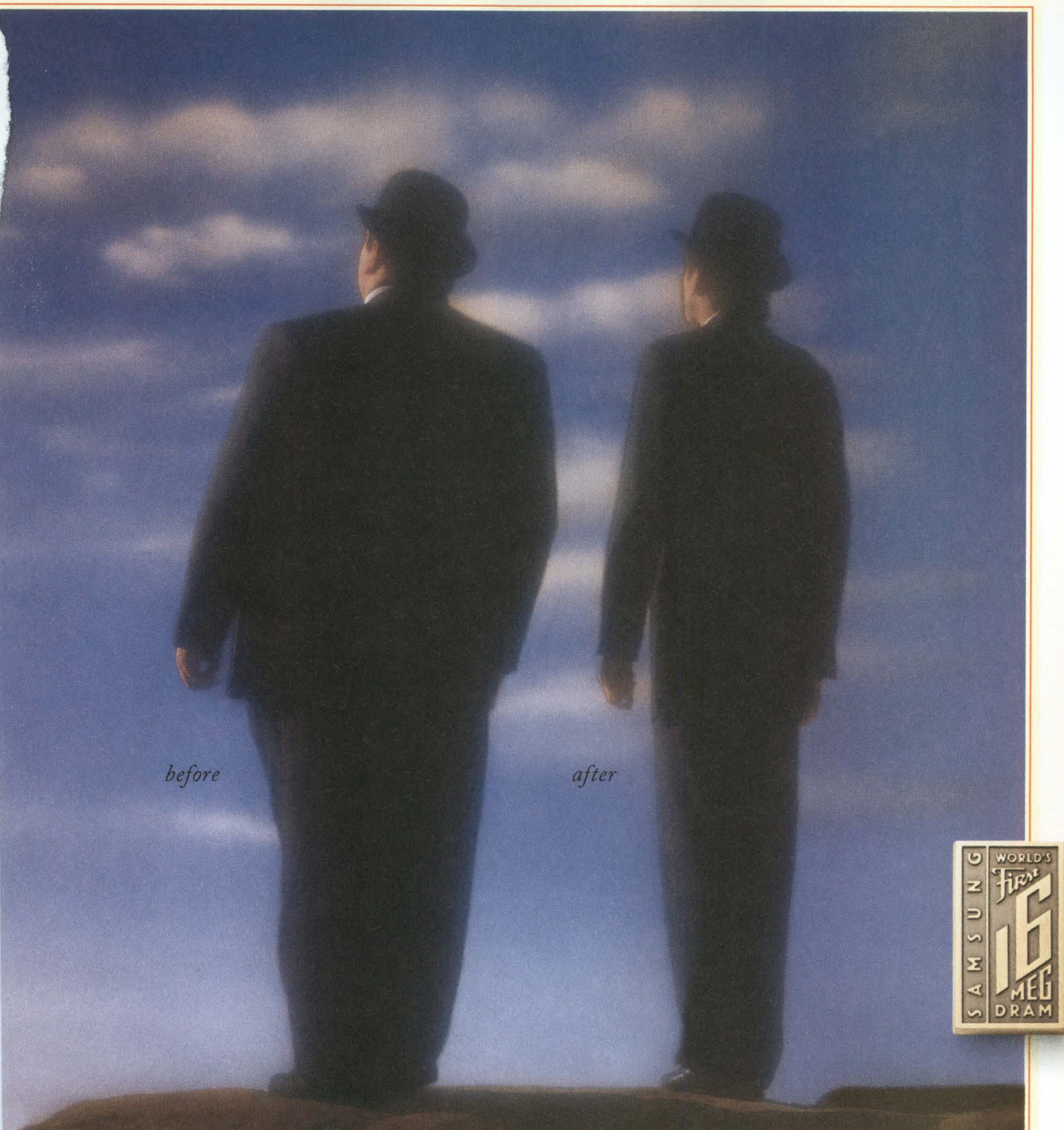

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CIRCLE NO. 91

ESDA

ELECTRONIC-SYSTEM-DESIGN-AUTOMATION

TOOLS

As system complexity grows, ESDA tool vendors try to convince you they can solve your design problems with a new class of tools. Maybe they can.

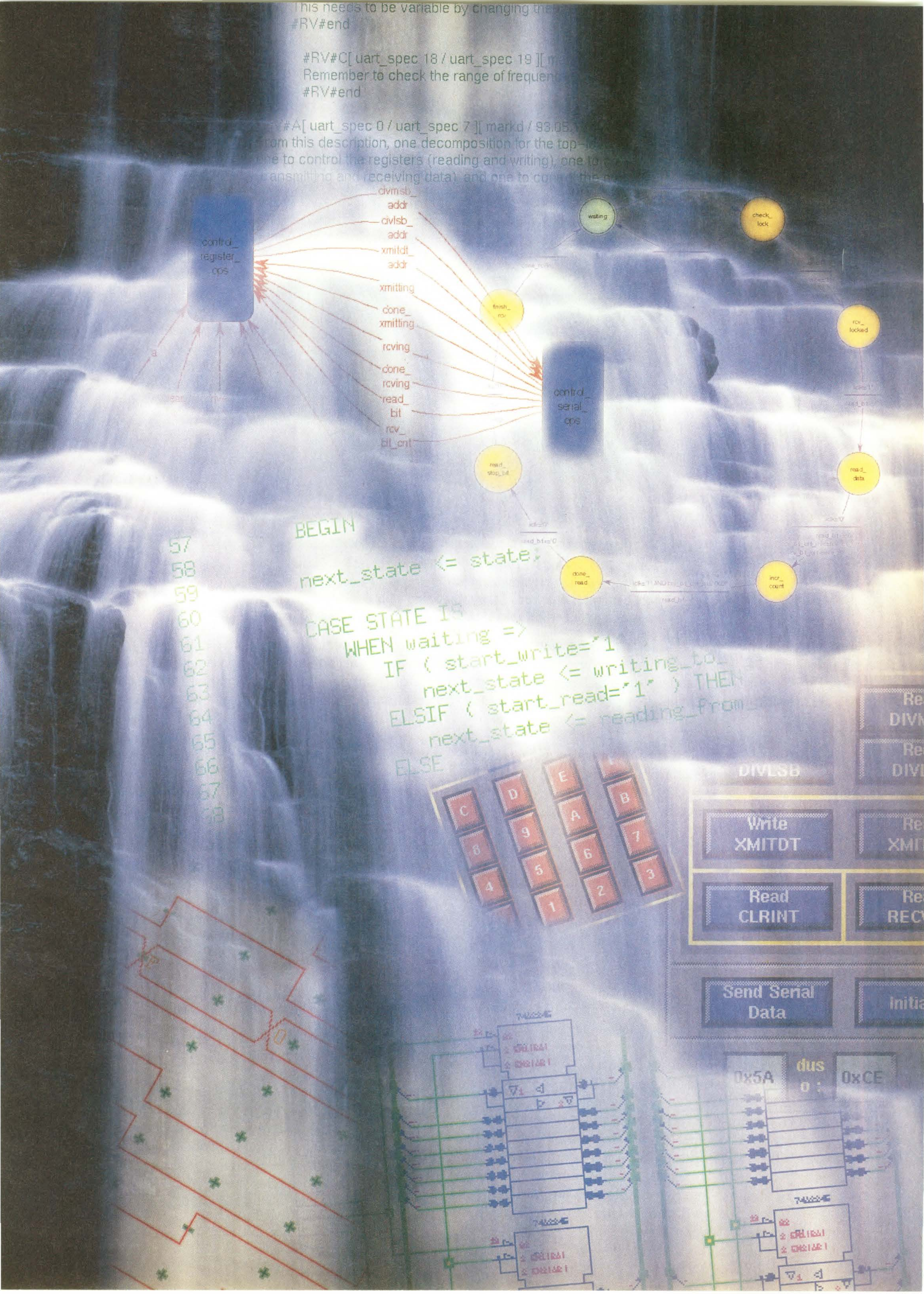
Photo courtesy Mentor Graphics

Not content with "EDA" for "electronic-design automation," trade-publication editors have conspired with EDA-tool marketers to create "ESDA" for "electronic-*system*-design-automation," the newest in a never-ending stream of acronyms. Your job as a designer isn't to understand what ESDA means. That's backward. Instead, the ESDA vendors should understand what designers need. However, you do need to understand which ESDA tools and design methods might help improve your effectiveness as a designer.

You can best understand what you need from ESDA tools by focusing on a methodology that best fits the type of work you do. In the quick-paced world of electronics, rethinking your design methodology every few years is inadequate; the process must be ongoing. You must constantly hone your methodologies. After each design, evaluate the tools and methods you've been using to see what works, what doesn't, and what you need to fix.

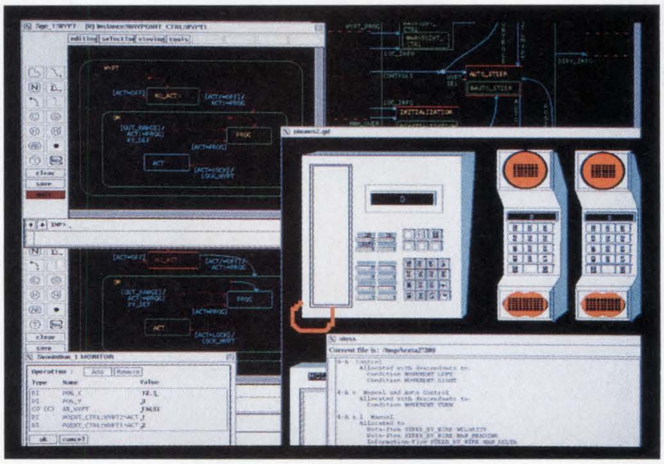
Furthermore, the perfect methodology for one company may very well drive another company out of business. For example, a test-equipment vendor with relatively uncomplicated systems but with extremely tight timing requirements may

DOUG CONNER, TECHNICAL EDITOR



#RV#end
#RV#C[uart_spec 18 / uart_spec 19][
Remember to check the range of frequen
#RV#end
control_register_ops
control_serial_ops
BEGIN
next_state <= state;
CASE STATE IS
WHEN waiting =>
Write XMITDT
Read CLRINT
Send Serial Data
0x5A
0xCE

still find that the best design method uses gate-level schematics and simulation. A company designing DSP systems may find system-level functionality a greater problem than is timing. That company may adopt a top-down design methodology using system-design tools, a hardware-description language (HDL), logic synthesis, and simulation, and the company may never descend to the gate level except to generate a netlist for device fabrication.



ESDA tools such as i-Logix's Statemate ExpressV-HDL help you transform design requirements into a graphical block diagram. The tool generates HDL code for synthesizing your design, and you can create a graphic prototype for realistic simulation of the architecture.

Every new-ESDA-product presentation starts by showing how time to market is your No. 1 enemy. Although reducing time to market is often vital, you must also understand the factors affecting time to market for *your* company's products—and whether the ESDA tool and any new methodology in question will help.

The first thing you need to do is evaluate where your company spends time in design work. (See **box**, "Where does the time go in your design group?") Your organization may suffer from some of the problems the box mentions or have problems unique to the type of systems your company designs. In either case, the first step toward improving your design tools or methodology is to identify the problem. Once you do that, you can look for tools to solve the problem.

Large, complex system designs generally cause—or at least magnify—the problems that so-called ESDA tools aim to solve. However, the term "ESDA" is much too general to tell you anything useful about a tool. For example, one ESDA tool may be strictly for graphical-design entry and have no simulation capability at all. Another may be for digital simulation of large systems; another, for analog simulation. But one of these tools may answer some of the needs of your design organization. **Table 1** (see pg 88) provides a representative listing of "ESDA tools," although not every manufacturer calls them ESDA tools.

Top-down design

A concept common to most ESDA tools is the use of top-down design. Although some tools can support both top-down and bottom-up design methods, most designers favor top-down design for using ESDA tools. You don't need ESDA tools to adopt a top-down design approach; however, most ESDA tools (and EDA tools in general) help you follow such an approach.

"Top down" means you start with a set of system-level requirements and develop high-level system block diagrams or a high-level architecture. After verifying that the architecture satisfies the system requirements, you treat each block as a subsystem and develop the architecture of each subsystem. You continue in this manner until you complete the specification of a design in whatever detail is necessary and verify compliance to the specification.

The top-down approach to system design doesn't just *sound* clean and logical. It *is* clean and logical, and it's the approach that most designers adopt when possible. The top-down approach implies the separation of system design and implementation. First, you need to design the right system; then, you must correctly implement it. The point between the design and implementation phases is where some tool vendors draw the line distinguishing EDA and ESDA tools. They claim that ESDA tools help you design the right system and that EDA tools help you design the system right. However, the distinction doesn't hold up under close scrutiny because many tools are useful for both system design and implementation.

The distinction between the system-level design phase and the implementation phase is, however, a useful one. During system-level design, you determine the behavior of the system and high-level system architecture. Once you create and verify a satisfactory high-level architecture, you can proceed to implementation, during which you flesh out the details.

Sometimes, you need to mix bottom-up and top-down design approaches. The bottom-up approach is often necessary for designs built on a specific device or technology. For example, if you build a data-acquisition system around a high-speed A/D converter, a bottom-up design surrounds the converter, but you can design the remainder of the system using a top-down approach.

Many designers believe that a design starts with a set of requirements, but that simply isn't true. A design usually starts with a need, a vision, or a little of both. For example, a designer might see a problem that an electronic system can solve or see a way to improve an existing system. Another designer might envision a completely new system. From

LOOKING AHEAD

Most designers would welcome tools that let them simply specify a design at a high level of abstraction and provide some optimization directives; the tool would then generate the physical implementation. Electronic-system-design-automation vendors would love to be able to offer such tools, too, and the vendors are working hard on the problem: Tools with these capabilities should shortly start to appear. The problem is that unless a logic-synthesis tool can generate a high-quality implementation from a high-level description, designers will have to rework their designs.

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CIRCLE NO. 105

Electronic-system-design automation

these needs and visions, designers create system requirements or a specification.

The translation of a need or a vision into system requirements is the first risk of introducing an error—either an outright error or simply the omission of a detail—into a system design. This translation is also often the reason for system specifications to keep changing during a design. It's difficult to reach the finish line fast if you start by designing a system based on an incorrect specification, and more diligence does not necessarily solve the problem. Designers cannot typically eliminate all errors in a design before simulation, so they shouldn't expect a person or an organization to create an error-free specification for a complex system without first testing it against a working prototype or a simulation.

A corollary assumption of the top-down design approach is that the earlier you find and correct errors, the more time and money you save. For example, finding an error in post-layout simulation of an ASIC is better than finding it after fabrication. Finding the error in prelayout simulation is even better. Finding an error at the architectural or system-requirements stage is better still.

As system complexity increases, the possibility of creating an error-free design without simulation or prototypes becomes more remote. ESDA tools for simulation offer some help by allowing you to create a system simulation early and giving you a means to test the system architecture, functional operation, and system specification against the original concept.

In theory, any simulator can help with system simulation, provided that it covers the domains in which you work, such

WHERE DOES THE TIME GO IN YOUR DESIGN GROUP?

Before you can fix a problem, you have to know what the problem is. The first step toward improving your design process is to identify the problems that eat design time in your organization. The following scenarios illustrate situations you might consider when evaluating your company's design methodology and possible ways to improve it:

Problem: My company has to design systems several times because the requirements keep changing.

Solution: Nail down the requirements earlier. Design engineers often feel helpless and frustrated about this problem because another department, such as product marketing, or even another company is causing those changing requirements. If the end result is that projects move slowly through your design organization because you have to design a complete system multiple times, you can and should do something about it.

Electronic-system-design-automation (ESDA) tools can help by showing you the implications of a design's requirements earlier. You create a system simulation and show it to a customer, get feedback, and make changes to the requirements earlier in the design cycle. System simulation doesn't keep requirements from changing but may let you zero in on the final set of requirements before you invest a lot of detailed design work implementing a design.

Problem: My organization knows what it wants to build (the system requirements don't change), and the design works when we build it, but we redesign it several times to reduce the cost or optimize the performance.

Solution: System-level design tools can help with the optimization stage, too, by providing a simulation of the system and evaluating its performance. Exploring alternative designs isn't a mistake; it's part of the design process. Sometimes, simple calculations or intuition can help you weed out unworthy design alternatives. Simulation provides even better insight into a design and how it performs, helping you decide which alternatives are worth pursuing. The earlier you weed out unworthy architectural alternatives and pursue winners, the more time you save.

Problem: My company knows what it is trying to build (the system requirements don't change), but the design doesn't work the first time—or the second.

Solution: Sometimes, you miss the bull's eye, but if you miss by a lot or you miss every time, there may be a problem you can correct. If you aren't simulating at all, then that's the problem. If you are simulating, then you probably aren't performing the exhaustive verification that the design requires. Implementation-level problems aren't typically a strength for ESDA tools; however, you can often uncover functional design problems with system-level simulation. If your problems are in timing, ESDA tools will not help.

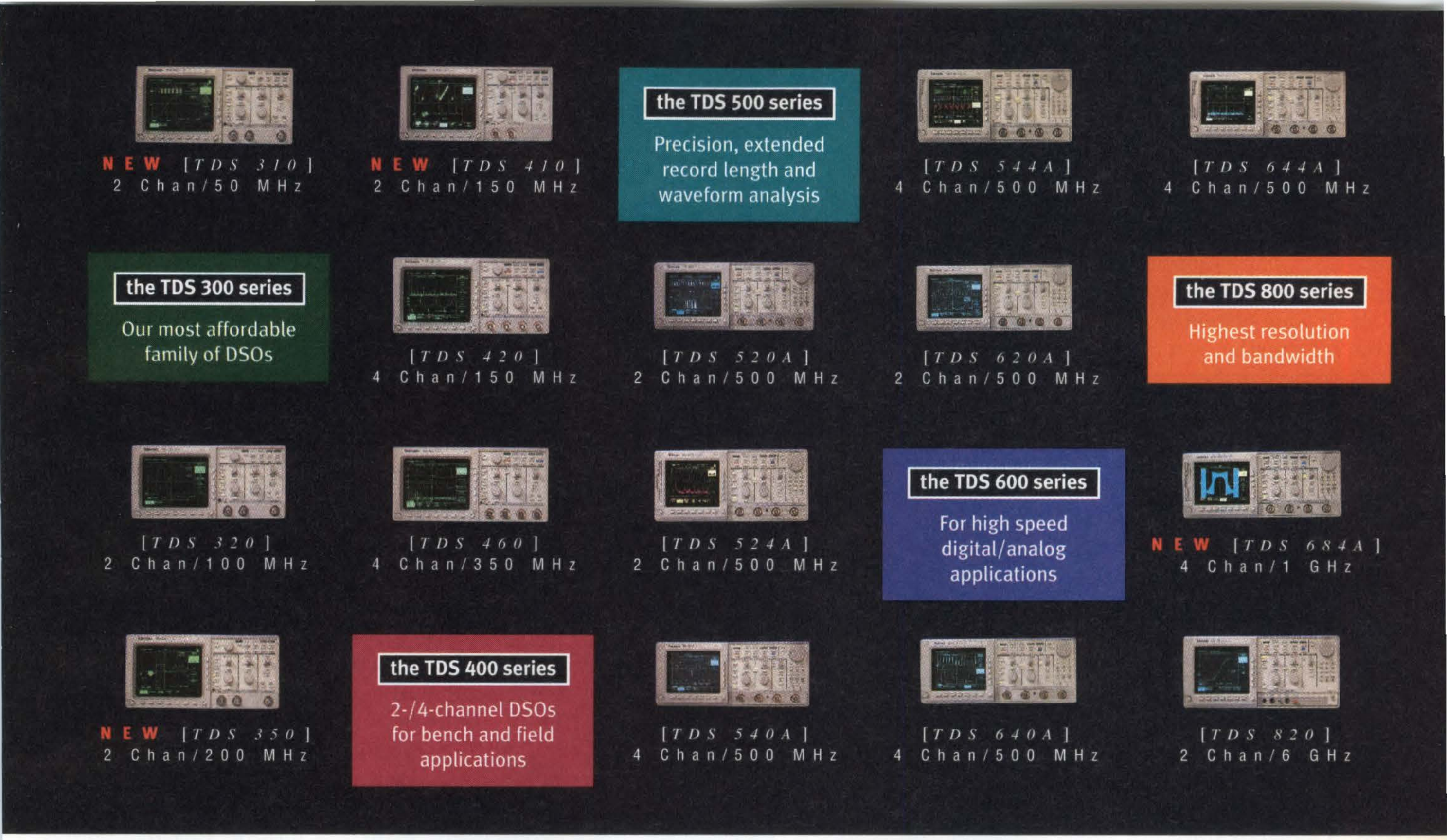
Problem: The design works when we finally get it done, and we don't go through a lot of design iterations. It just takes a long time.

Solution: Determine in greater detail where all the time is going. You may need tools that streamline some time-consuming parts of your design process, or you may need a new design methodology. If you are still creating digital designs at the gate level, you might consider moving to a hardware-description language (HDL). If the thought of text-based design leaves you cold, consider one of the many ESDA tools that provides graphical-design entry.

Graphical-design tools let you connect high-level blocks in a diagram, much like a schematic. Each block performs a general class of functions, such as adding or counting. You fill in a parameter table to specify the exact function, how many bits wide, and other specifications. From this graphical block-level design, many of the ESDA tools generate VHDL or Verilog code for input to logic-synthesis tools. Using these tools lets you avoid learning an HDL or at least lets you learn them at your own pace while completing designs in a timely manner.

If your design cycle takes too long because you spend too much time simulating to eliminate all the bugs, you may have a simulation-speed problem. Some ESDA tools provide cycle-based simulators that are 100 to 1000 times faster than ordinary logic simulators; these cycle-based simulators find functional design problems.

If your simulation problems are in timing, ESDA tools probably won't help. Instead, look for fast simulators or hardware accelerators.



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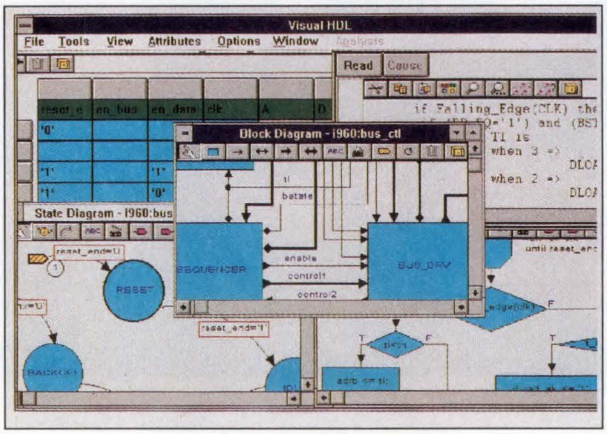
CIRCLE NO. 93

Electronic-system-design automation

as analog, digital, mixed signal, or mechanical. In practice, an effective system simulator must be fast enough to run the simulation at an acceptable speed and have sufficient capacity for your system design. The simulator should also provide the information you need in a format that makes it easy to understand and evaluate a system's operation.

For most systems, behavioral-level models and cycle-based simulators can provide the required speed. Gate-level digital simulators and transistor-level analog simulators often cannot. Many companies use behavioral-level models in VHDL, Verilog, C, Spice, and proprietary languages.

Cycle-based simulators find functional design problems in synchronous systems. These simulators inovlve a tradeoff, however, because they sacrifice timing information for simulation speed in hunting down functional design problems. Cycle-based simulators are best suited to a divide-and-conquer approach of system design. First, you create and debug the functional design; then, you solve timing problems. For some systems, timing is the heart of the system, and trying to separate it from functional design is pointless.



Accepting block diagrams, state diagrams, flow charts, truth tables, and VHDL text, Visual HDL from Summit Design helps you develop and simulate system designs while providing a smooth path to implementation.

How a simulator presents information is also an important selection criterion. Most logic simulators offer a waveform display for examining logic problems, but such a display is relatively inefficient for identifying system-level problems. You may need to show a system simulation to a customer who is not an electronic design engineer. With an easily understood format, such a customer can more likely find system problems in simulation instead of in the finished product.

Most ESDA simulators provide simulation results in a graphical format. Some tools, such as Redwood Design Automation's Race Simulator and Reveal Interactor, Mentor Graphics' System Design Architect, and i-Logix's Statemate family let you tailor a system's simulation output to almost any type of graphic display. These tools let you create a virtual-prototype system and test it against the specification and the original concept before investing the time in a full design implementation. These tools not only help you explore architectural approaches, but also let all members of the design work from a common vision of the finished system.

Implementing the design

Once you develop what appears an acceptable system architecture, you can move to the implementation phase. Most—but not all—graphical-ESDA tools are part of an implementation path. Conversion of graphical design information into a synthesizable design description is the reason many of these tools exist. With these tools, you provide a graphical block or state diagram, and the tool translates it into synthesizable code, usually VHDL or Verilog.

Because logic-synthesis tools differ, graphical-design tools often develop code differently for each logic-synthesis tool. You should verify that any combination of design and synthesis tools you are considering using generates high-quality code.

Some high-level ESDA-simulation tools don't provide an implementation path through logic synthesis. These tools may be effective architectural tools to help verify that you are designing the right system, but they force you to create the physical design description separately.

Even before ESDA tools were in fashion, some designers created behavioral-level HDL models of systems for simulation and architectural verification and then created a register-transfer-level (RTL) description to implement the design. Because you cannot synthesize behavioral-level HDL designs, except for very low-level designs, this approach also leaves you without a direct implementation path. It does, however, let you insert your RTL-logic blocks into the full system design for simulation as you transform the architectural design into an implementation.

If your goal is to work at a higher level and design more gates in a short time, consider using macros or building blocks having high gate counts to perform the functions you need. For example, Synopsys' DesignWare and Intergraph's MacroSyn include libraries of parameterized logic blocks that implement efficiently in synthesis.

Every component in Synopsys' ALU family has multiple architectures for each function. You can optimize these architectures for either performance or area to meet your design goals. If you find the building blocks you need, this design approach should raise your design efficiency.

A variation on the design-efficiency theme is design reuse. Salvaging parts of a design from a previous system and reusing them with relatively minor variations saves considerable time over generating them from scratch. In designs requiring greater variations, you can use Synopsys' DesignWare Developer, which lets you develop your own parameterized modules. The attraction of this approach is that you can implement the modules you need in the way you want. The disadvantage is that you invest time in creating the modules. If you will use the modules frequently, however, this time investment is probably justified. EDN

(Tables follow on pg 88)

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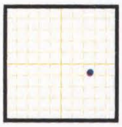

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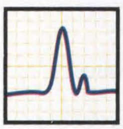

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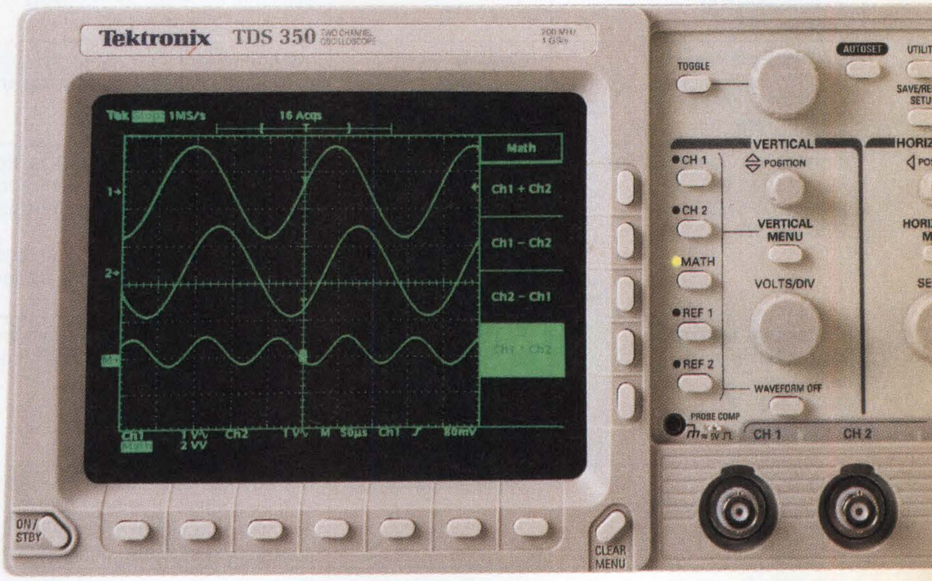

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Channels	2	2	2
Vertical Sensitivity	2 mV - 10 V	2 mV - 10 V	2 mV - 10 V
Vertical Resolution	8 bits	8 bits	8 bits
Record Length	1K/channel	1K/channel	1K/channel
Standard Advanced Features	TV Line & Field Trigger, Roll Mode, Autoset, 21 Automatic Measurements, Peak Detect		
Comm. I/O (Option 14)	GPIB, RS-232, Centronics and VGA video output		
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CIRCLE NO. 92

ELECTRONIC-SYSTEM-DESIGN AUTOMATION TOOLS

Manufacturer	Product	Description	Inputs
Anacad EES Milpitas, CA (408) 954-0600 **Circle No. 396**	HDL-A	VHDL-based analog behavioral modeling system for use with the company's Eldo simulator; models analog and mixed-signal systems, including electrical, mechanical, fluid, rotational, magnetic, thermal	VHDL and proprietary HDL-A language
Analogy Inc Beaverton, OR (503) 626-9700 **Circle No. 397**	Saber	Analog and mixed-signal simulation; works with logic simulators; model libraries and templates available for many applications	Spice models and proprietary modeling language (MAST)
CADIS Software South San Francisco, CA (415) 615-7789 **Circle No. 398**	Cossap	Integrated tool for the design, simulation, and implementation of digital-processing and communication systems	Graphical block diagrams
Comdisco Systems Inc Foster City, CA (415) 574-5800 **Circle No. 399**	System Design Architect	System-level design for ASICs, field-programmable gate arrays, and microcoded processors using a parameterized library of synthesizable blocks	Graphical function blocks, VHDL, C
	Signal Processing WorkSystem (SPW)	Interactive design, simulation, and implementation of DSP and communication systems	Graphical block diagrams
Compass Design Automation San Jose, CA (408) 433-4880 **Circle No. 400**	ASIC Navigator	Top-down ASIC design system with application to general-purpose design, DSP, image processing, and communication	Block diagrams for data path, state machines, memory templates, VHDL, Verilog, gate-level schematics, Boolean equations, and truth tables
Elanix Inc Westlake Village, CA (818) 597-1414 **Circle No. 401**	SystemView	Dynamic system simulator for conceptual design and evaluation of analog and digital designs; emphasis on signal processing, communications, control systems, and general mathematical modeling	Graphical block diagrams and graphical templates
HP-EESof Westlake Village, CA (818) 879-6200 **Circle No. 402**	OmniSys	System simulator for evaluating topologies of communication systems; analyzes complex waveforms in systems based on arbitrary topologies and modulation schemes	Graphical block diagrams
Hyperception Dallas, TX (214) 343-8525 **Circle No. 403**	Hypersignal for Windows Block Diagram	Graphically develops and simulates DSP and communication systems; generates source code for porting designs to other platforms or cross-compiled for specific DSP chips	Graphical block diagrams
i-Logix Inc Andover, MA (508) 682-2100 **Circle No. 404**	Statemate 5.0 ExpressV-HDL	Requirements traceability, graphical design,simulation, analysis, and code generation; hardware/software co-design	Architectural block diagrams, behavioral state charts, C
Intergraph Huntsville, AL (205) 730-2700 **Circle No. 405**	MacroSyn	Provides template-driven creation of synthesizable macros	Graphical symbols and templates
	Design Expressions	Design description allows entering of designs using truth tables, state tables, Boolean equations, VHDL, and Diablo for design descriptions	Truth tables, state tables, Boolean equations, VHDL; Diablo for analog behavioral descriptions
	ACEPlus Designer	Graphical creation of state-machine designs	State diagrams
Knowledge Based Silicon Inc Columbia, SC (803) 779-2504 **Circle No. 406**	FlowHDL	Creates system descriptions as a collection of hierarchically partitioned concurrent flow-diagram threads for general-purpose design	Graphical and textual design entry for state-machine, data-path clocking, memory, synchronous, and asynchronous, and resolution functions
	BlockHDL	Specifies high-level system descriptions as collections of hierarchically partitioned blocks; supports top-down and bottom-up design methodologies	VHDL, Verilog, block diagrams
Mentor Graphics Wilsonville, OR (503) 685-8000 **Circle No. 407**	System Design Station	Top-down system design from requirements through graphical or textual design to verification and implementation of general-purpose and DSP designs; VHDL-code generation	Graphical state and data-flow diagrams, state-transition matrix and table editor, VHDL

Outputs	Simulation	Provides an implementation path	Computer required	Price
Models compatible with the Eldo simulator	Mixed signal; also works with most logic simulators for large VDHL descriptions	Simulation only	Workstation	HDL-A development system: $30,000, runtime version: $8000, Eldo: $22,000
Simulation	Analog and mixed signal	Simulation only	Workstation	Starts at $20,000
VHDL, DSP-executable code	Yes	Yes	Workstation	$30,000
VHDL, Graphical Waveform	Cycle-based simulator	Yes	Workstation	$5000 plus $25,000 for SPW
C or assembly code for DSP chips (VHDL optional)	Floating point (fixed point optional)	Yes	Workstation	$25,000
Complete ASIC and and field-programmable gate-array designs	VHDL and Verilog	Yes	Workstation	$40,000
Mathematical models	Yes	No	PC/Windows	$985
Simulation	Yes	No	Workstation	$26,000
C optional	Yes	On path (software)	PC/Windows	$1995, C-code generator: $5000, Advanced Transmission library: $1495
VHDL, Verilog; optional C and Ada code	Yes	Yes	Workstation	$20,000 to $40,000
VHDL, Verilog	No	Yes	Workstation	$10,000
VHDL, Verilog, ABEL	No	Yes	Workstation	$8000
VHDL, Verilog, ABEL	No	Yes	Windows NT, Unix workstations	$3500
VHDL, Verilog	Cycle-based simulator	Yes	Workstation	$10,000
VHDL, Verilog	Optional	Yes	Workstation	$2800
ASIC and field-programmable gate-array libraries; interface to computer-aided software engineering, DSP, analog, VHDL	VHDL, gate-level simulator	Yes	Workstation	$94,900

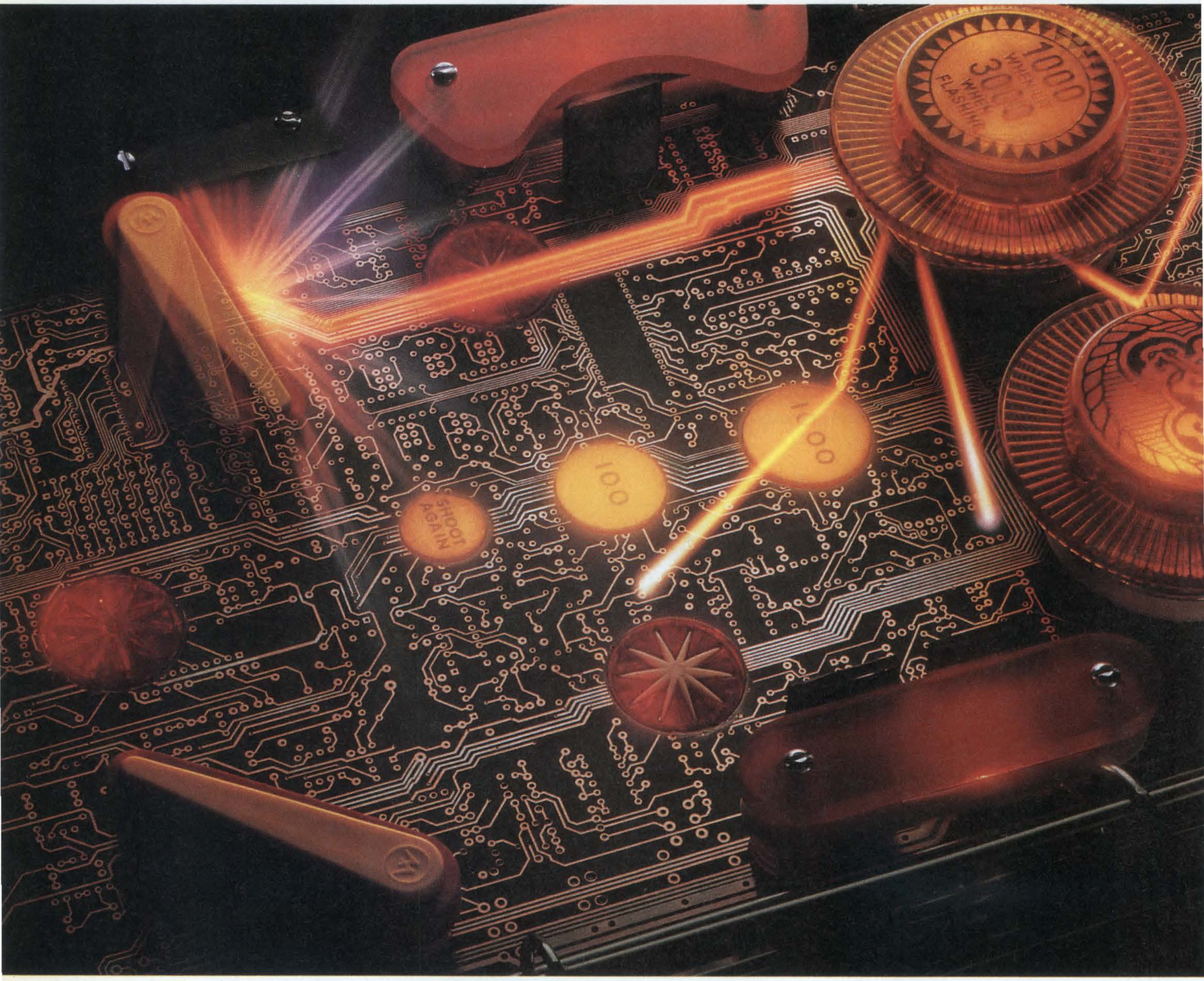
table continued on pg 90

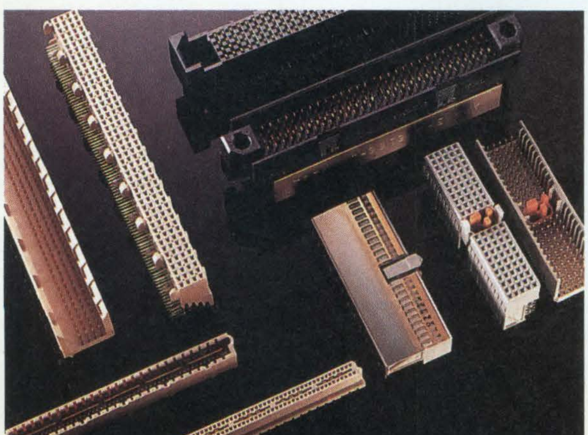
ELECTRONIC-SYSTEM-DESIGN AUTOMATION TOOLS (CONTINUED)

Manufacturer	Product	Description	Inputs
Mentor Graphics Wilsonville, OR (503) 685-8000 **Circle No. 408**	System Architect	Graphical and textual design of systems for DSP and general-purpose applications; state-machine verification and VHDL-code generation	Graphical state and and data-flow diagrams, VHDL
NuThena Systems McLean, VA (703) 356-5056 **Circle No. 409**	Foresight 3.00	Development tool for constructing and analyzing executable system models for embedded and distributed systems	Proprietary modeling language, graphical entry
R-Active Cupertino, CA (408) 252-2808 **Circle No. 410**	Better State Pro	Generates C, C++, VHDL, or Verilog from state diagrams	Graphical state diagrams
Redwood Design Automation (408) 291-3650 San Jose, CA **Circle No. 411**	Race Simulator/ Reveal Interactor	Cycle-based simulation engine and graphical prototyping tool	VHDL, Verilog, C, C++
Scientific and Engineering Software Inc Austin, TX (512) 328-5544 **Circle No. 412**	SES/Workbench	Evaluates functionality and performance of architecture before prototyping of computers, complex software systems, large data-communication networks, bus-interfaces, communication protocols, μPs, and ASICs	Graphically models systems with a variety of node types; creates custom nodes in C; Verilog cosimulation optional
Speed Electronics Inc Oak Brook, IL (708) 990-1910 **Circle No. 413**	SpeedChart	Graphical design tool for generating VHDL and Verilog code	State diagrams, schematics, behavioral code, spreadsheet tables
Summit Design Inc Beaverton, OR (503) 643-9281 **Circle No. 414**	Visual HDL	Captures designs using four graphical languages, simulates and outputs designs in VHDL or Verilog	Block diagrams, state diagrams, flow charts, truth tables, VHDL text
Synopsys Mountain View, CA (415) 962-5000 **Circle No. 415**	DesignWare	Parameterized, fully synthesizable modules for general-purpose design; allows the addition of custom components to the library	Selects modules, then inputs parameters to customize them for a design
TD Technologies Inc Cleveland Heights, OH (216) 371-9777 **Circle No. 416**	Transcend	Design, analysis, and verification tool for complex electronic hardware- and software-systems design	Proprietary- graphical/ textual-language, C++ VHDL, and Verilog submodules
Tesoft Inc Roswell, GA (404) 751-9785 **Circle No. 417**	Tesla	Block-diagram simulator for communication, signal-processing, and control systems	Proprietary-language and graphical-function blocks
Vantage Analysis Systems Fremont, CA (510) 659-0901 **Circle No. 418**	TD Connection/ TD Simulator	Transaction-based simulator allowing analysis of architectural tradeoffs, cosimulation with VHDL designs optional	Proprietary-graphical/textual-language, VHDL submodules
Viewlogic Systems Inc Marlboro, MA (508) 480-0881 **Circle No. 419**	ViewState	Graphical VHDL entry tool allowing graphical creation of complex behavioral models; supports hierarchical and concurrent state machines	State diagrams
	View Architect	Synthesizes hardware architecture from behavioral VHDL descriptions, producing architectural block diagrams and detailed register-transfer-level design structure ready for logic synthesis	Behavioral and register-transfer-level VHDL
Vista Technologies Schaumburg, IL (708) 706-9300 **Circle No. 420**	Design Vision	Graphically develops HDL models	Graphical entry of control-flow and data-flow diagrams
Visual Software Solutions Inc Coral Springs, FL (305) 346-8890 **Circle No. 421**	StateCAD	Graphically creates state diagrams and translates them in ABEL or C code	Graphical

Outputs	Simulation	Provides an implementation path	Computer required	Price
VHDL	State-machine animator	Optional synthesis	Workstation	$34,900
Reports, animated data visulization	Yes	No	Workstation	$25,000
VHDL, Verilog, C, C++	No	Yes	PC/Windows	$1195
Simulation	Cycle-based simulation	Simulation only	Workstation	Race/Reveal combined: $65,000
Simulation	Graphical animation	No	Workstation	SES/Workbench: $37,000, Verilog cosimulation: $6000
VHDL, Verilog; C optional	Yes	Yes	Workstation	$26,000
VHDL, Verilog	Yes (presynthesis)	Yes	Workstation, PC/Windows	Unix: $25,000, PC/Windows: $12,500
VHDL	Optional	Yes	Workstation	Libraries: $5000, developers tools: $45,000
Simulation	Yes	Yes	Workstation	$35,000
Graphical and text	Digital and analog	No	PC	$695
Simulation	Yes	No	Workstation	TD Connection: $12,000 TD Simulator: $35,000
VHDL	Simulates state transitions	Yes	Workstation	$11,000
VHDL, hierarchical block diagrams	No	Yes	Workstation	$25,000
VHDL, Verilog	Compatible with standard VHDL and Verilog simulators	Yes	Workstation	$15,000
ABEL, C, state diagrams	Functional state simulation	Yes	PC/Windows	$995

At fast edge rates, the wrong interface takes on unexpected qualities.





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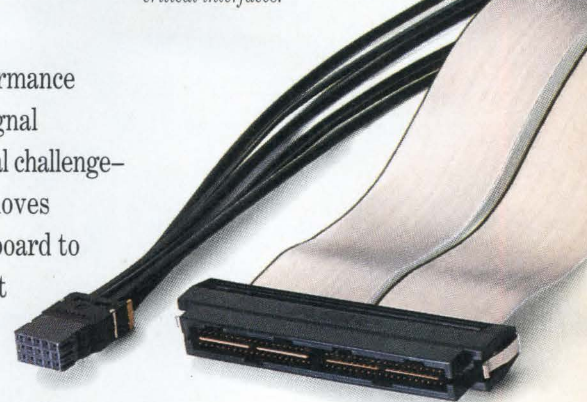

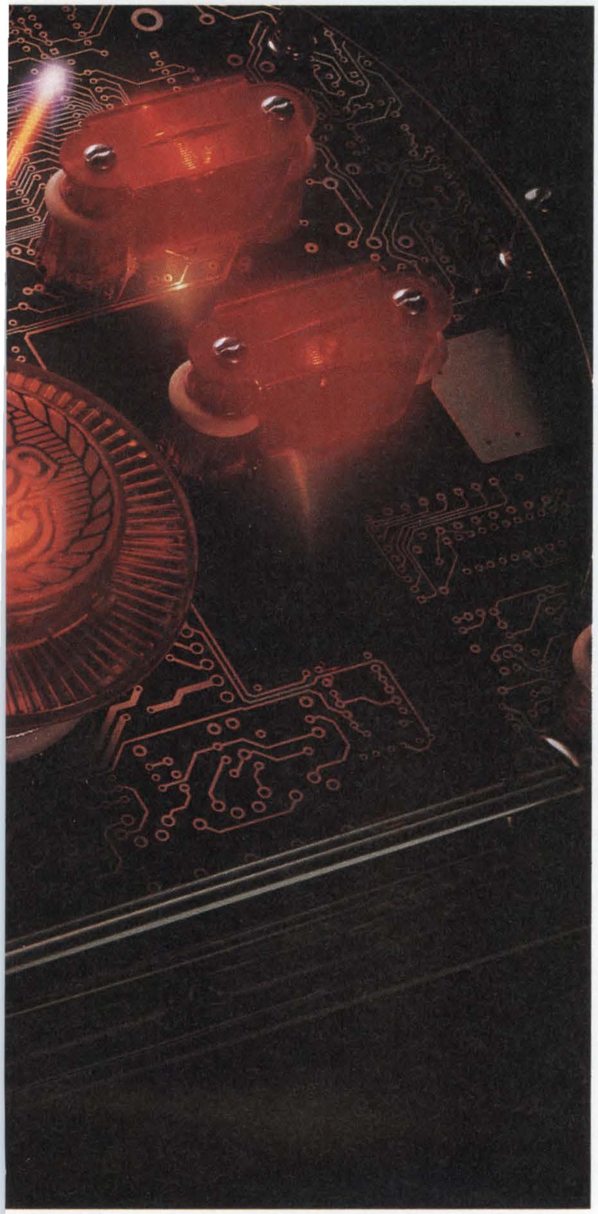

As the demand for performance pushes clock rates up, signal integrity can become a real challenge–especially when traffic moves from board to board, or board to cable. Interconnects that worked last time around suddenly act a lot like bumpers and flippers when your signal hits them. Fortunately, expert interconnect help is available.

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AMP

CIRCLE NO. 104

Low-distortion oscillator starts fast

Mika Maaspuro, Helsinki University of Technology, Espoo, Finland

Unlike a Wien-bridge oscillator, the phase-shift oscillator in **Fig 1** starts up quickly. Also, the circuit does not require that you adjust several trimming resistors just to tune the oscillator to a given frequency. Experiments show that the circuit's total harmonic distortion (THD) measures approximately 0.5% or less.

Connecting the output of a bandpass stage to its input via a phase inverter realizes a phase-shift oscillator. In practice, a phase-shift oscillator also needs a limiter stage. Unfortunately, the limiter can distort the output sine wave.

Diodes D_1 and D_2 in the feedback loop of IC_{1A} form a limiter that *does not* distort the output. The equation for the circuit is

$$f_{OSC} = \frac{1}{2\pi C}\sqrt{\frac{1}{R_2R_1}+\frac{1}{R_3R_1}} \approx \frac{1}{2\pi C\sqrt{R_3R_1}}.$$

R_1 tunes the frequency of the oscillator.

To have a stable output voltage and minimum distortion, you must set the gain of the loop carefully. The gain needed for oscillation varies slightly with frequency; the circuit needs more gain for lower frequencies. You can leave R_1 fixed to a value that yields the lowest frequency.

The circuit can generate a good-quality sine wave at low frequencies. In those cases, the values of capacitors C_1 and C_2 may be several microfarads. With such large capacitors, the startup time increases to several hundred milliseconds. You can avoid this delay by connecting diode D_3. With D_3 in place, startup always takes no more than a few milliseconds. D_3 does not distort the characteristics of the circuit because D_1 and D_2 already limit the output to a few hundred millivolts, peak-to-peak. With D_3 connected, the circuit needs a little more gain to develop a stable output.

EDN BBS /DI_SIG #1423 contains a writeup of this circuit and a comprehensive Spice model. (DI #1423)

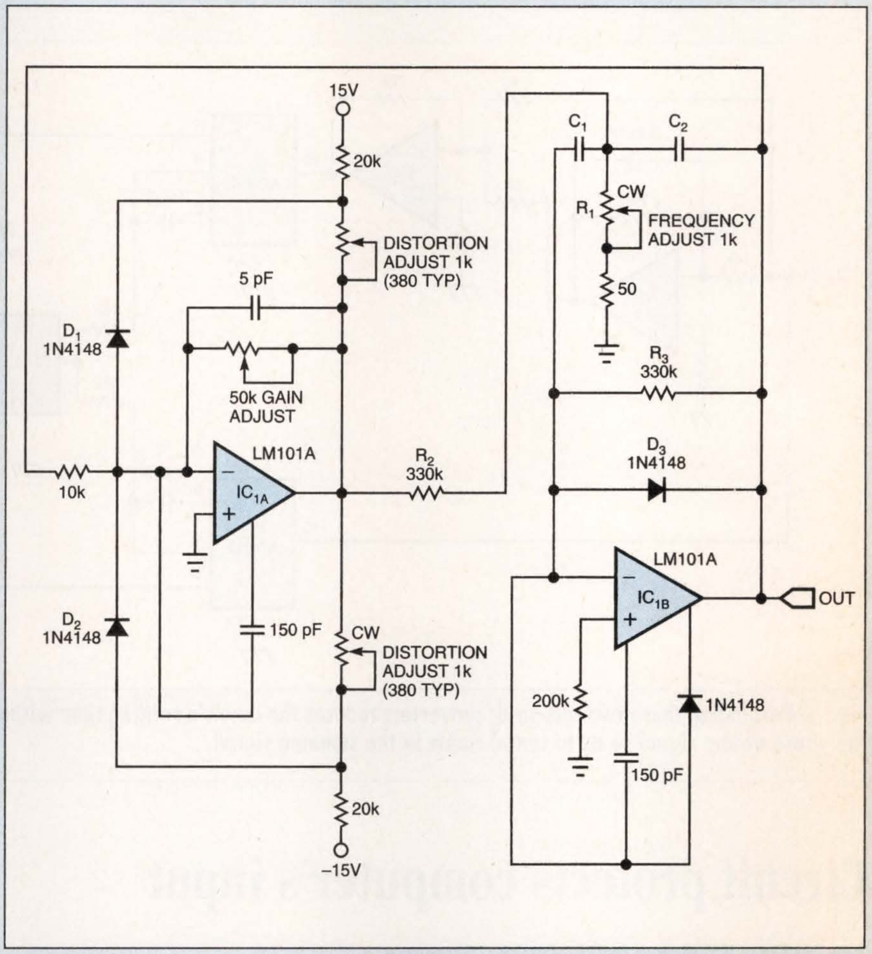

Fig 1—This fast-startup sine-wave oscillator does not exhibit the usual output distortion of phase-shift oscillators.

Reference

1. "Easily Tuned Sine Wave Oscillators," National Semiconductor, Linear Application Handbook 1986, pp 1118 to 1119, LB-16.

To Vote For This Design, Circle No. 424

Paralleling rms converters speeds settling

Bernard Courtiol, Cegelec Soprano, Vaulx Milieu, France

An rms-to-dc converter requires an output lowpass filter, which sometimes leads to overly long settling times. Paralleling two converters reduces the circuit's settling time signal without increasing conversion errors (**Fig 1**).

The circuit in **Fig 1** monitors 50-Hz mains. IC_1, IC_2, and their associated circuitry compose a phase shifter. The phase shifter has a 90° delay for 50-Hz inputs and constant gain. The second-order, lowpass, state-variable filter, IC_5, sums and filters the outputs of rms-to-dc converters IC_3 and IC_4.

The circuit's settling time to 1% of final value is 20 msec.

$F(p)=0.5/(a^2p^2+2kap+1)$, where k=0.7 and a=0.5 msec.

If the circuit were to have only one rms-to-dc converter, its settling time would be 100 msec.

To reduce the circuit's settling time further, you could parallel more converters, each having a different phase shift. The trick is to set up the phase shifts so as to cancel ripple in the summed signal. (DI #1424) EDN

To Vote For This Design, Circle No. 425

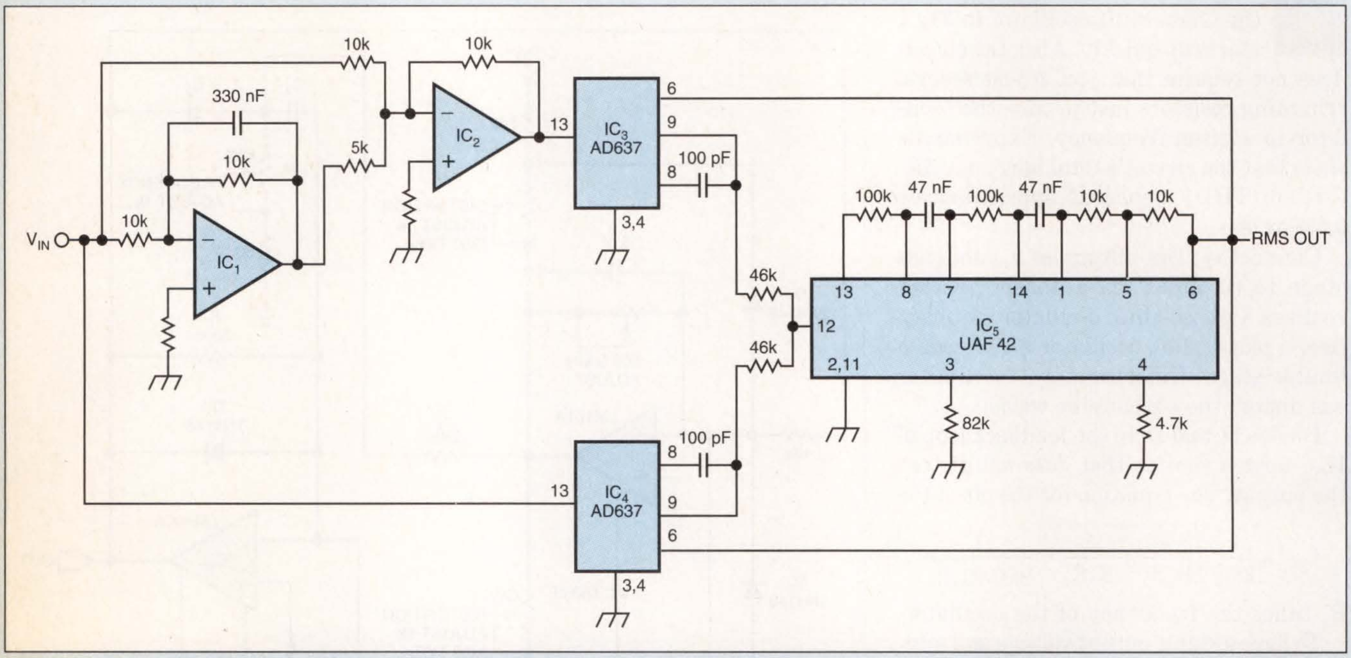

Fig 1—Paralleling these two rms-to-dc converters reduces the circuit's settling time without increasing conversion errors. The op amps shift the phase of one signal so as to cancel ripple in the summed signal.

Circuit protects computer's input

Ang Tzu Seng, Halliburton Drilling Systems, Singapore

The circuit in **Fig 1** performs input protection, level translation, isolation, and debouncing. The circuit allowed the output of a relay driver to connect to a computer even though the relay driver delivered a voltage as high as 24V and the relay driver had no ground connection.

With the values in **Fig 1**, the low and high thresholds at the circuit's input were approximately 8 and 16V, respectively. The cutoff frequency was high enough to allow counting 1200 counts/min. The input withstood 110V ac continuously—the optoisolater's withstand voltage is 3 kV.

I tested the debouncing function with a microswitch in series with a 24V-dc power supply and the relay driver. I detected no switch bounce.

You can change capacitor C_1 to suit other applications' cutoff frequencies. Altering the resistors may be tricky because you will affect the circuit's low- and high-threshold levels. To use inputs other than 24V, change R_1. (DI #1425) EDN

To Vote For This Design, Circle No. 426

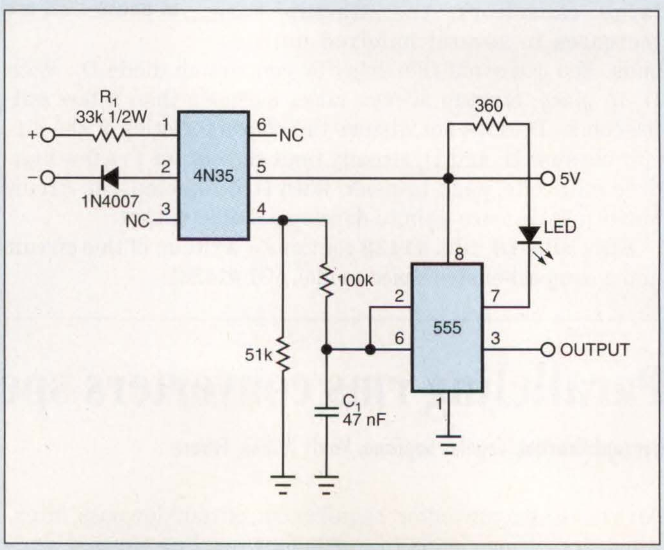

Fig 1—This circuit performs input protection, level translation, isolation, and debouncing for a computer's input.

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MAN-1LN	0.5-500	28	1.4	8.0	2.8	42	12/60	15.95
^MAN-1HLN	10-500	10	0.8	15.0	3.7	16	12/70	15.95
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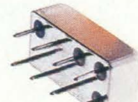
MAN-2AD	2-1000	9	0.7	-2.0	6.5	33	15/22	22.50
MAN-11AD	2-2000	8	1.5	-3.5	6.5	27	15/22	29.95

* Midband $10f_L$ to $f_U/2$, +/- 0.5 dB   ** At 1dB compression point   ^ Case height 0.3 inch

CIRCLE NO. 103



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F 175 Rev Orig

RS-485 repeater extends standard's reach

Mitchell Lee, Linear Technology Corp, Milpitas, CA

RS-485 specifies communications for distances up to 4000 ft. This limit is the consequence of losses in the twisted pair used to carry the data. Beyond 4000 ft, skin effect and dielectric losses take their toll, attenuating the signal beyond use.

Fig 1 shows a simple RS-485 repeater. Two RS-485 transceivers connected back-to-back relay incoming data from either side. A pair of cross-coupled one shots control the data flow so that only one transmitter turns on at a time.

A 1-to-0 transition at the output of either idling receiver signifies incoming data. The first receiver to spot such a transition triggers its associated one shot, which, in turn, activates the opposite transmitter to ensure smooth data flow from one side of the repeater to the other. At the same time, the one shot locks out the other receiver/transmitter/one-shot combination, so that only one data path is open.

Successive 1-to-0 transitions and start bits retrigger the one shot, holding the data path in its present configuration. Set the one shots' time constants slightly greater than the interval between any two start bits.

When received data stops arriving, the previously active line idles high, producing a 1 at the receiver's output. The one shot resets, returning the opposite transceiver to the receive mode—ready for any subsequent data flow in either direction.

The software protocol must wait one word length after the end of any data transmission before responding to a call or initiating a new conversation to allow adequate time for the one shots to reset. The repeater in **Fig 1** handles 100-kbps data rates and a 8-bit word length, plus start and stop bits. (DI #1421)

To Vote For This Design, Circle No. 427

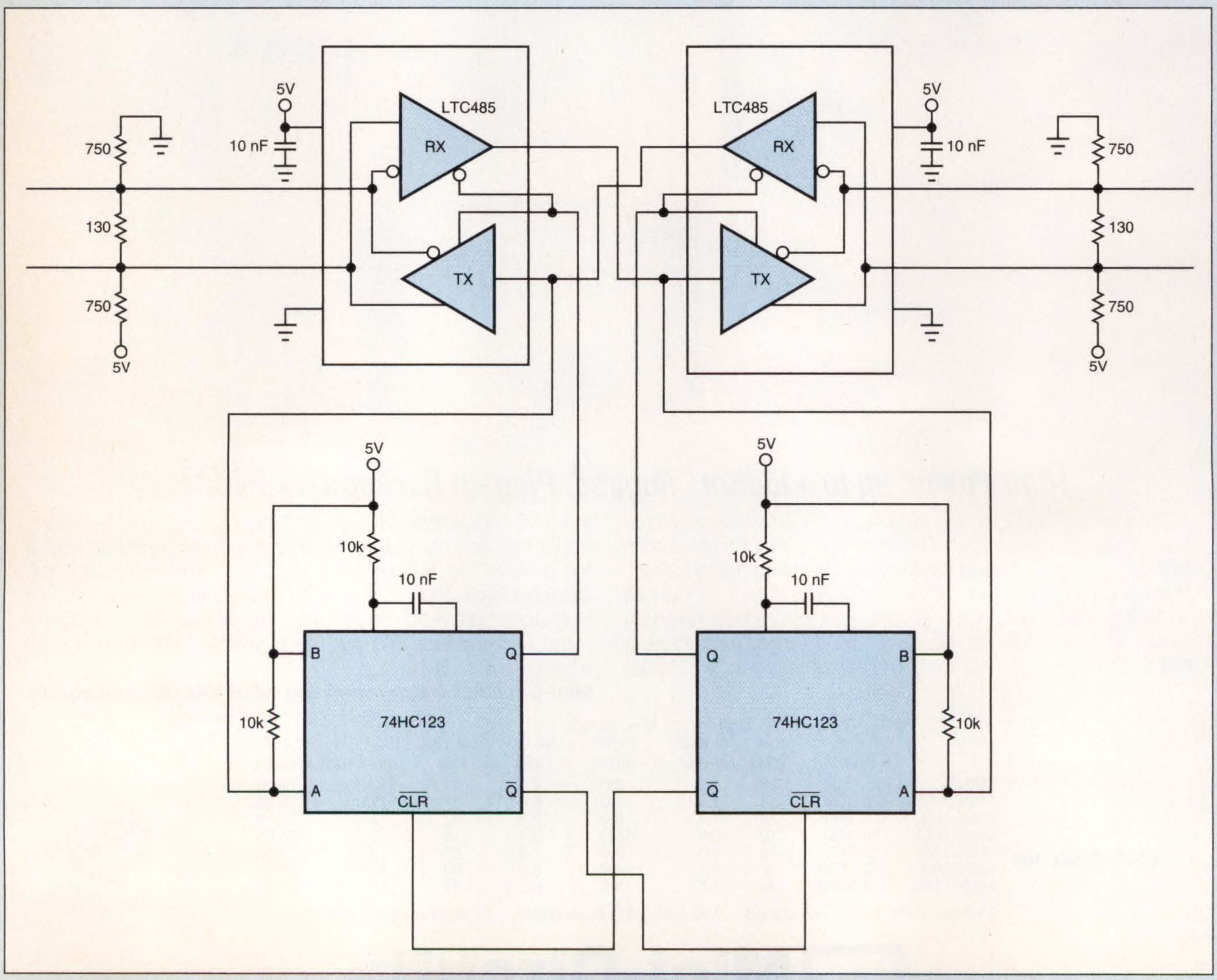

Fig 1—This simple RS-485 repeater can compete with μP-based repeaters if you set up your software protocol properly.

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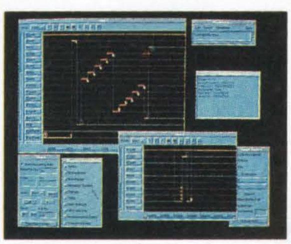

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WIND RIVER SYSTEMS

CIRCLE NO. 96

Pulse generator verifies test setups

Jim Williams, Linear Technology Corp, Milpitas, CA

Verifying the rise-time limit of wideband test-equipment setups is a difficult task. In particular, you must often know the "end-to-end" rise time of an oscilloscope/probe combination to ensure measurement integrity. **Fig 1**'s circuit provides an 800-psec pulse having rise and fall times shorter than 250 psec. The pulse's amplitude is 10V, and the circuit's source impedance is 50Ω. The circuit is similar to the one **Ref 1** details, except that this circuit is triggerable instead of free-running. This triggering feature permits synchronizing with a clock or another event. You can vary the delay of the output with respect to the trigger by 200 psec to 5 nsec.

The circuit requires a high-voltage bias for operation. A cascoded high-voltage transistor, Q_2, combines with a switching regulator IC_1 to form a high-voltage, switched-mode supply. IC_1 pulse-width-modulates Q_2 at a 100-kHz clock rate. L_1's inductive events get rectified and stored in the 2-μF output capacitor. The adjustable resistor divider provides feedback to IC_1. The diode and RC combination at Q_2's base damp inductor-related parasitic behavior. The 10-kΩ/1-μF pair filters noise from the supply line.

The R_3/C_1 combination applies high voltage to Q_1, a 40V-breakdown device. Set the high-voltage "bias-adjust" control at the point where free-running pulses across R_4 *just* disappear. This setting puts Q_1 slightly below its avalanche point.

Subsequently, applying an input trigger pulse causes Q_1 to avalanche. The result is a quickly rising, very fast pulse across R_4. C_1 discharges, Q_1's collector voltage falls, and breakdown ceases. C_1 then recharges to just below the avalanche point. At the next trigger pulse, this sequence repeats.

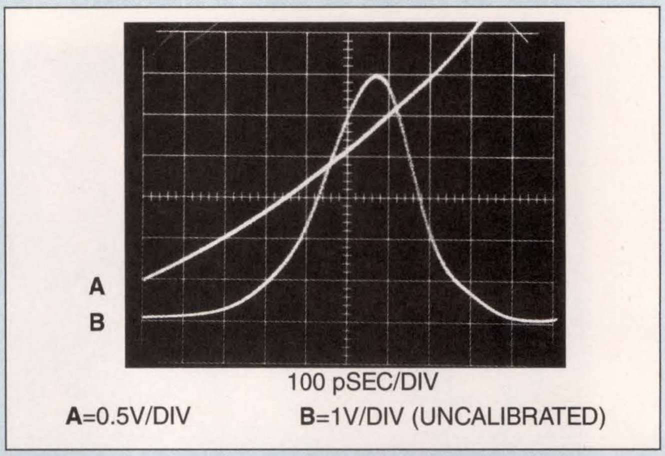


Fig 2—The input trigger pulse to the circuit in Fig 1 appears as Trace A. A 3.9-GHz Tektronix 661 sampling oscilloscope with 4S2 sampling plug-in measured the pulse, Trace B, as having a 10V amplitude and an 800-psec duration. Rise time is 250 psec, with fall time indicated as 200 psec. The times are probably slightly faster, because the oscilloscope's 90-psec rise time influences the measurement.

Fig 2 shows the circuit's waveforms. The input trigger pulse is Trace A. Its amplitude provides a convenient way to vary the delay time between the trigger and output pulses. A 1 to 5V setting range produces a continuous 5-nsec to 200-psec delay range.

The circuit requires some special considerations for optimal performance. L_2's very small inductance combines with C_2 to slightly retard the trigger pulse's rise time. This retardation prevents significant trigger-pulse artifacts from appearing at the circuit's output. You should select C_2 for the best compromise between output-pulse rise time and waveform purity. You may also have to select Q_1 to get the desired avalanche behavior. Such behavior, while characteristic of the device, is not guaranteed.

A sample of 50 Motorola 2N2369s, spread over a 12-year date-code span, yielded 82% usable devices. All "good" devices switched in less than 600 psec. Select C_1 for a 10V output amplitude. C_1 is typically between 2 and 4 pF. Ground-plane construction with high-speed layout, connection, and termination techniques are essential for good results from this circuit. (DI #1427) EDN

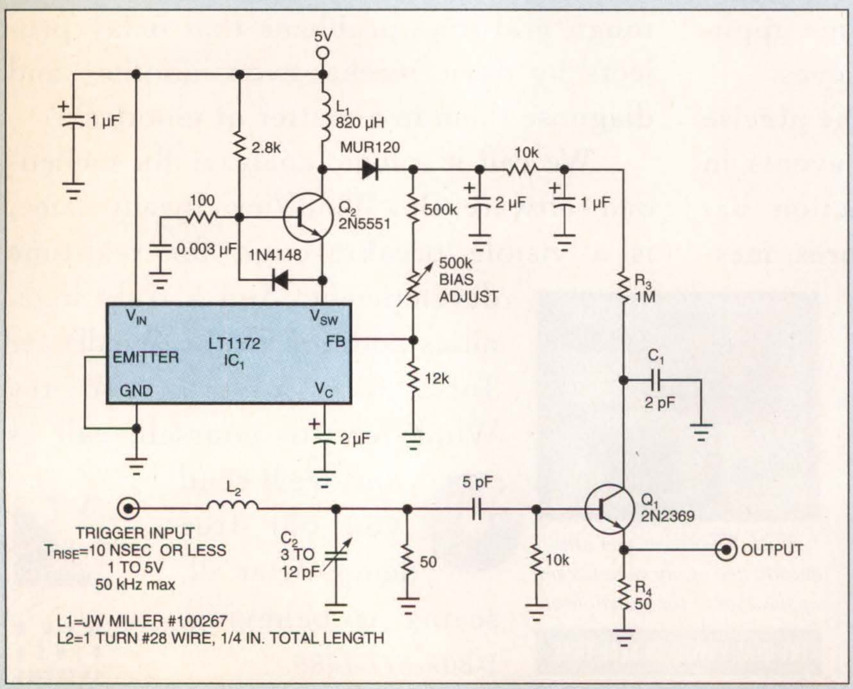


Fig 1—A trigger pulses causes the carefully biased Q_1 to avalanche, producing a fast, short 10V pulse suitable for verifying instrument setups.

Reference

1. Williams, Jim, "Measurement and Control Circuit Collection," App Note 45, Linear Technology Corp, 1991, pg 18.

To Vote For This Design, Circle No. 428

Simple module gives voice to PC

Jerzy R Chrzaszcz, Institute of Computer Science, Warsaw University of Technology, Warsaw, Poland

BBS The circuit in **Fig 1** uses the ISD1020A voice-record/playback chip (Information Storage Devices, San Jose, CA, (800) 825-4473) to allow an IBM PC to speak and hear. The analog part of the circuitry comes from the company's application notes. The host PC controls address inputs (A_0 through A_7), Chip Enable (CE), Playback/Record (P/R), and Power Down (PD). The host also—supposedly—monitors End Of Message flag (EOM).

The ISD1020A latches an address when CE goes low, requiring a 300-nsec setup time. Fortunately, the PC's bus controller automatically inserts several wait states (typically four wait states at 8 MHz) into I/O cycles. Consequently, the circuit needs no intermediate latching, allowing you to tie inputs A_0 through A_7 directly to the data bus.

A GAL20V8 PLD integrates other interface functions (**Listing 1**). The ZIPfile attached to **EDN BBS /DI_SIG #1433** contains the listing for the PLD as well as a writeup and circuit diagram. Because of limited pin count, the PLD uses only one of the PC's data lines. You generate various control patterns by accessing locations within address area 300_{HEX} to $31F_{HEX}$. The PC's I/O map reserves these locations for prototype boards. (DI #1433) EDN

To Vote For This Design, Circle No. 429

Listing 1—Interface-PLD program

```
Name        PRO;
Date        03/03/94;
Revision    2.3;
Designer    JCh;
Company     ICS WUT;
Device      g20v8;
Partno      ;
Assembly    ;
Location    ;

/**  Inputs  **/
Pin 2  =  a0     ; /* system address bus                   */
Pin 3  =  a1     ; /* .                                    */
Pin 4  =  a2     ; /* .                                    */
Pin 5  =  a3     ; /* .                                    */
Pin 6  =  a4     ; /* .                                    */
Pin 7  =  a5     ; /* .                                    */
Pin 8  =  a6     ; /* .                                    */
Pin 9  =  a7     ; /* .                                    */
Pin 10 =  a8     ; /* .                                    */
Pin 11 =  a9     ; /* .                                    */
Pin 14 =  aen    ; /* address enable                       */
Pin 1  = !iow    ; /* I/O write strobe                     */
Pin 23 = !ior    ; /* I/O read strobe                      */
Pin 13 = !oen    ; /* register output enable               */
Pin 19 = !ext    ; /* external input signal - active-low   */

/**  Outputs  **/
Pin 15 =  q0     ; /* register outputs - OEN controlled    */
Pin 16 =  q1     ; /* .                                    */
Pin 17 =  q2     ; /* .                                    */
Pin 18 =  q3     ; /* .                                    */
Pin 20 =  d0     ; /* least significant bit of data bus    */
Pin 21 = !hit    ; /* hit when CPU accesses ports 300..31F */
Pin 22 =  irq    ; /* interrupt request - active-high      */

/**  Logic Equations  **/
field adh = [a9..a5];
field adl = [a4..a0];

hit = adh:[300..31f] & !aen;
high = hit & adl:[10..1f];
hit00 = hit & adl:00;
hit01 = hit & adl:01;
hit02 = hit & adl:02;
hit03 = hit & adl:03;
hit1f = hit & adl:1f;
 q0.d = high & a0 # hit00 & d0 # !high & !hit00 & q0;
 q1.d = high & a1 # hit01 & d0 # !high & !hit01 & q1;
 q2.d = high & a2 # hit02 & d0 # !high & !hit02 & q2;
 q3.d = high & a3 # hit03 & d0 # !high & !hit03 & q3;
 d0 = hit00 & q0 # hit01 & q1 # hit02 & q2 # hit03 & q3 # hit1f & !ext;
 d0.oe = hit & ior;
 irq = ext;
```

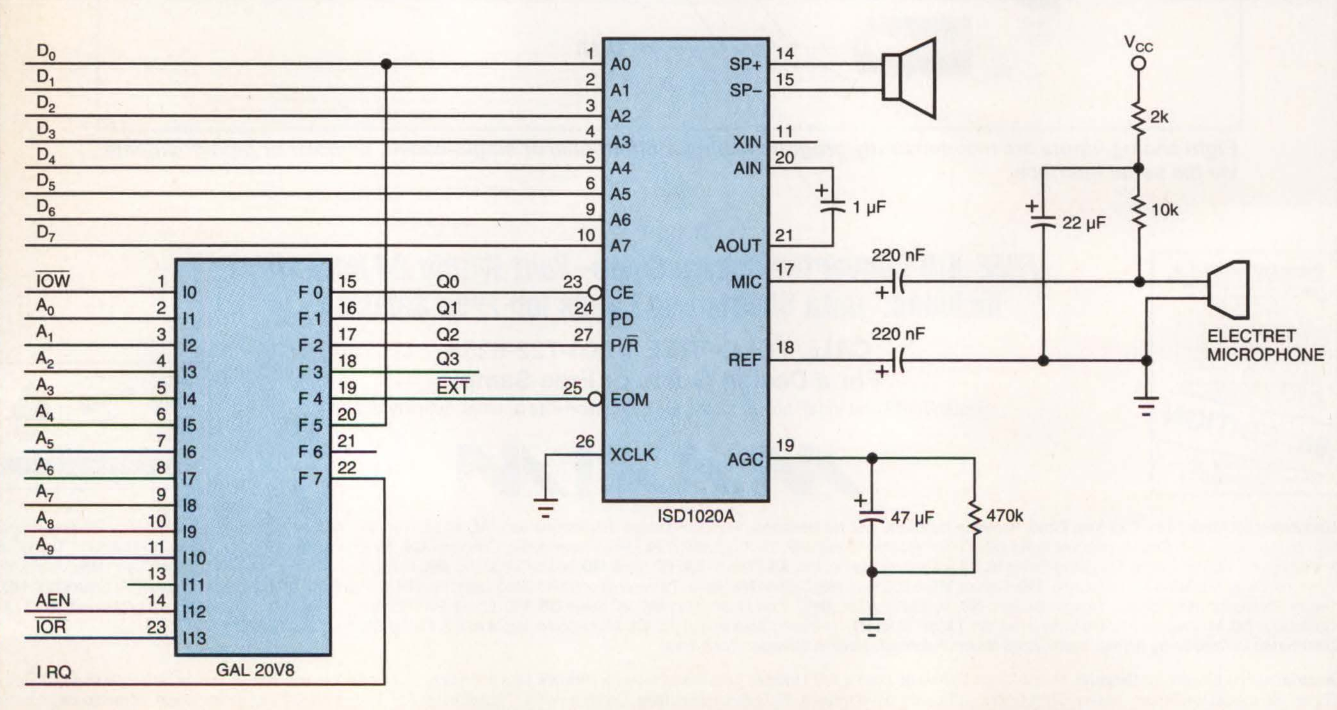


Fig 1—This simple interface circuit allows an IBM PC to control an advanced record/playback audio IC.

Security circuit eschews sophistication

I-Cheng Chen, AEG, Ajax, ON, Canada

BBS

Because of the many states involved in implementing sequential combination locks, most designers use a microcontroller or a PLD. But for those die-hard discrete designers who don't want to bother with debugging programs, here's a dead-simple circuit that verifies a security code's entry from a 10-digit keypad.

The circuit in **Fig 1** verifies an 8-digit code. You preset each digit in the code sequence by installing a shunt in the respective shunt-header position. That is, to set the first digit in the code to 3, install a shunt in position 3 of SH1; to set the second digit to 7, install a shunt in position 7 of SH2, and so on.

When the circuit resets, flip-flop IC_{2A}'s output goes high, energizing the shunted output on header SH1. If a user presses the correct key on the keypad (matching the shunted position on SH1), the input voltage to IC_{1B} and IC_{1C} is high enough to cause a pulse on both their outputs. If the user presses the wrong key, the R_1/R_2 voltage divider on the selected line supplies just enough voltage to produce a pulse only on IC_{1C}'s output.

The output of each op amp, IC_{1B} and IC_{1C}, clocks its own corresponding shift register, IC_4 and IC_3. IC_3 always advances when the user presses a correct or an incorrect key. However, IC_4 advances only if the user presses the correct key.

When IC_3 advances, its outputs energize the next shunt header (SH2, SH3, and so on) sequentially. Only when the user (or an intruder) presses the correct key on every stroke does IC_4 advance at the same rate as IC_3. When the user correctly enters all the digits in the code, the last output of IC_4 toggles the output-control flip-flop. If any one of the digits is wrong, IC_4's output does not advance far enough before IC_3's output resets IC_4.

D_1 through D_8 provide isolation between the shunt headers, so that only the energized shunt header has high output on its shunted line.

C_1 debounces the keypad and introduces a small time delay between the output pulses of IC_{1C} and IC_{1B}. This delay is critical because the output of IC_{1B} must clock IC_4 to produce an output upon the last correct digit before IC_3's output resets IC_4.

Resistor array R_3 is optional; it provides added security, so that if an intruder tries to press more than one key at a time on the keypad to bamboozle the circuit, the voltage drop across R_3 is sufficient not to trigger IC_{1B} because of the added load.

You can expand this circuit to as many keys and to as long a code sequence as you want by cascading multiple IC_3s and IC_4s. IC_{2A}'s output can drive an LED indicator to signal if the keypad is waiting for input or is in the middle of a code sequence. The ZIPfile attached to **EDN BBS /DI_SIG #1429** contains a writeup of this design and its schematic in OrCAD format. (DI #1429) EDN

To Vote For This Design, Circle No. 430

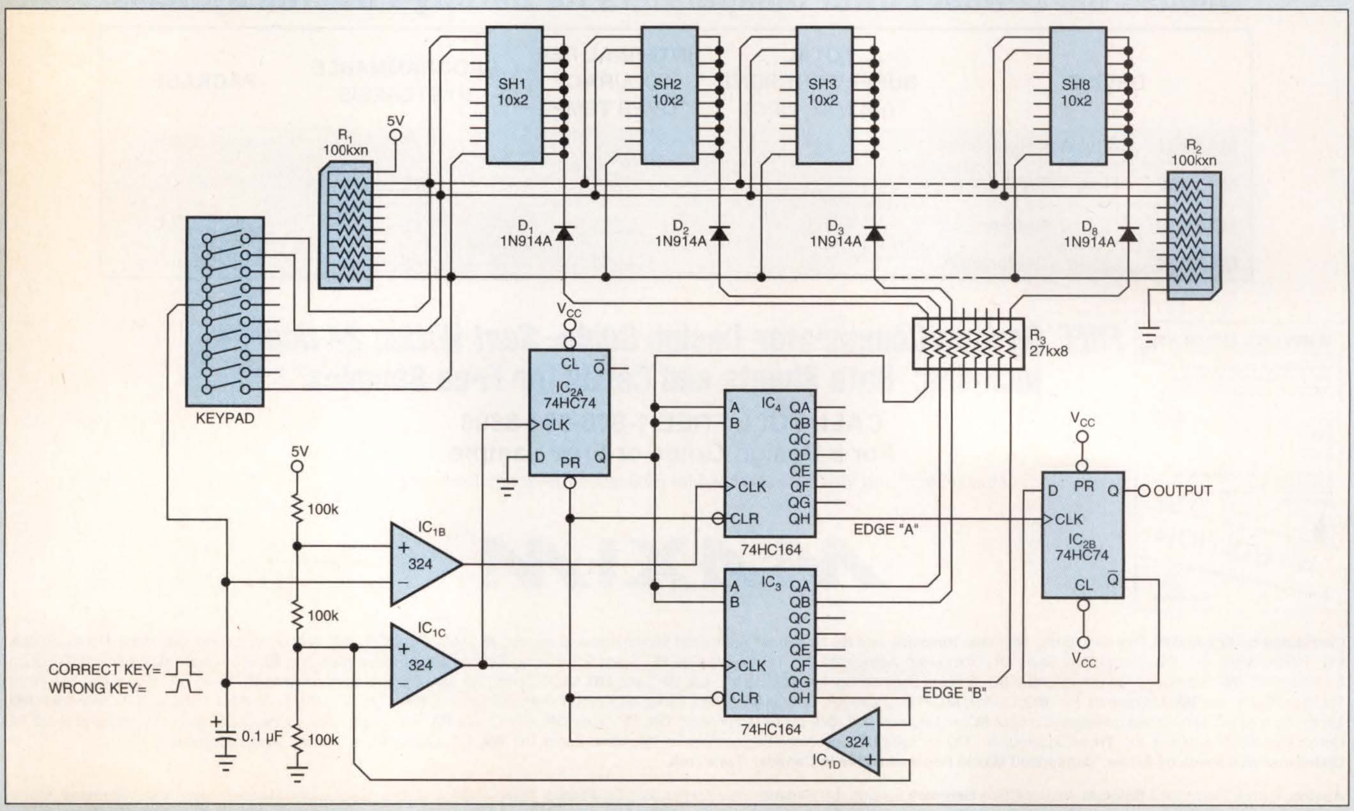
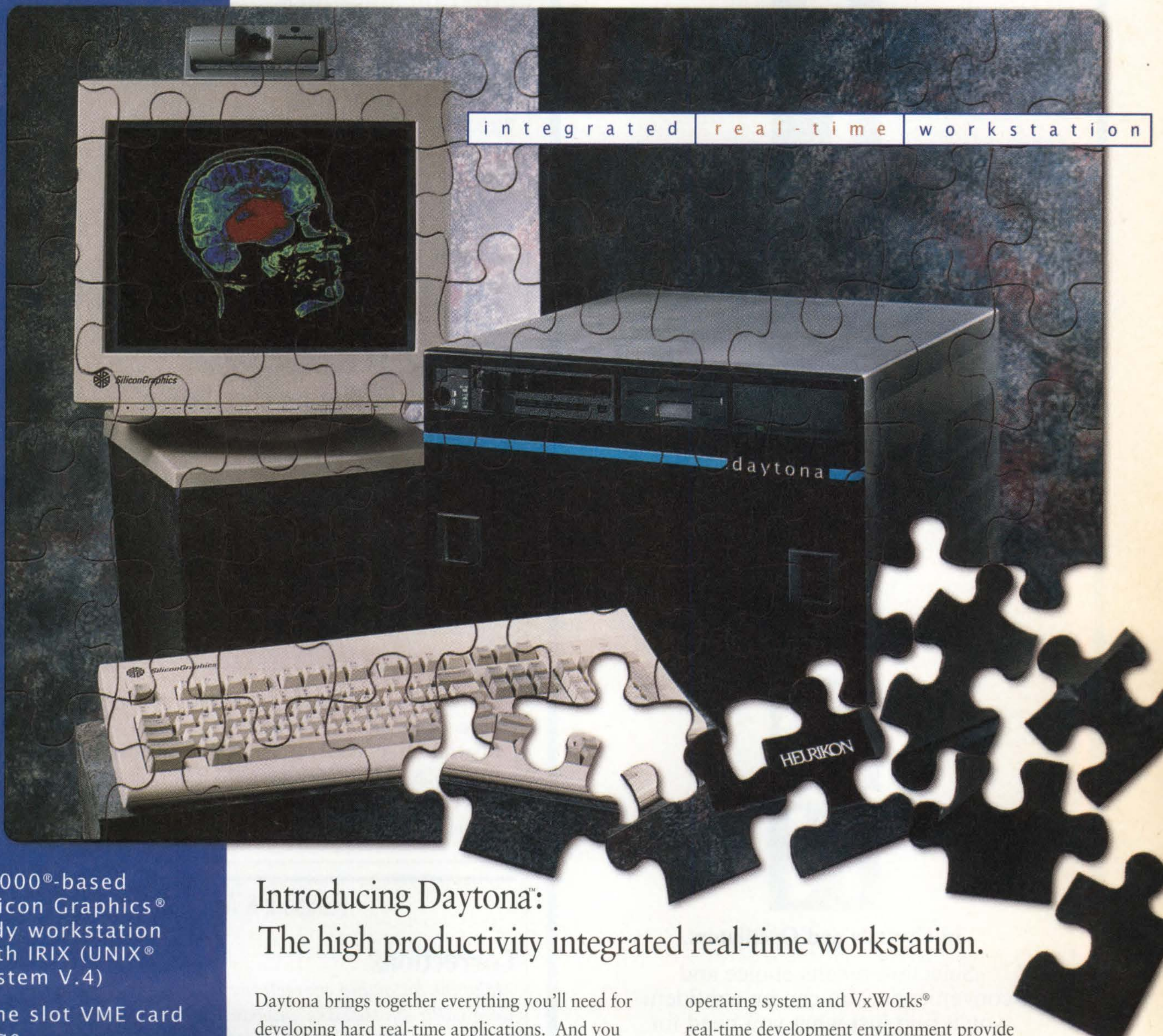


Fig 1—This circuit can verify a security code entered from a keypad yet uses no µP or PLD.

daytona

Why struggle with the pieces when Daytona solves the puzzle?



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- Entire system supported by Heurikon
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Software Shorts

Program simplifies microstrip calculations

B Brewster, Satellite Microwave & Communications Ltd Weert, The Netherlands

Written in Fortran, the simple, menu-driven programs in **EDN BBS /DI_SIG #1407** determine physical line-width and quarter-wavelength dimensions from input characteristic-impedance, frequency, and substrate parameters or returns characteristic impedance from given physical line width and substrate parameters.

To Vote For This Design, Circle No. 431

Breakpoints change Spice parameters during simulation

John R Stice, Physio-Control Corp Redmond, WA

The Spice switch subcircuits in **EDN BBS /DI_SIG #1408** allow simulation parameters to change on the fly when breakpoint voltages or other preset conditions occur.

To Vote For This Design, Circle No. 432

These Software Shorts listings are too long to reproduce here. You can obtain the listings from the Design Idea Special Interest Group on *EDN*'s bulletin-board system: (617) 558-4241, 300/1200/2400 8,N,1. From Main Menu, enter ss/DI_SIG, then rknnnn, where nnnn is the file referenced above.

Feedback & Amplification

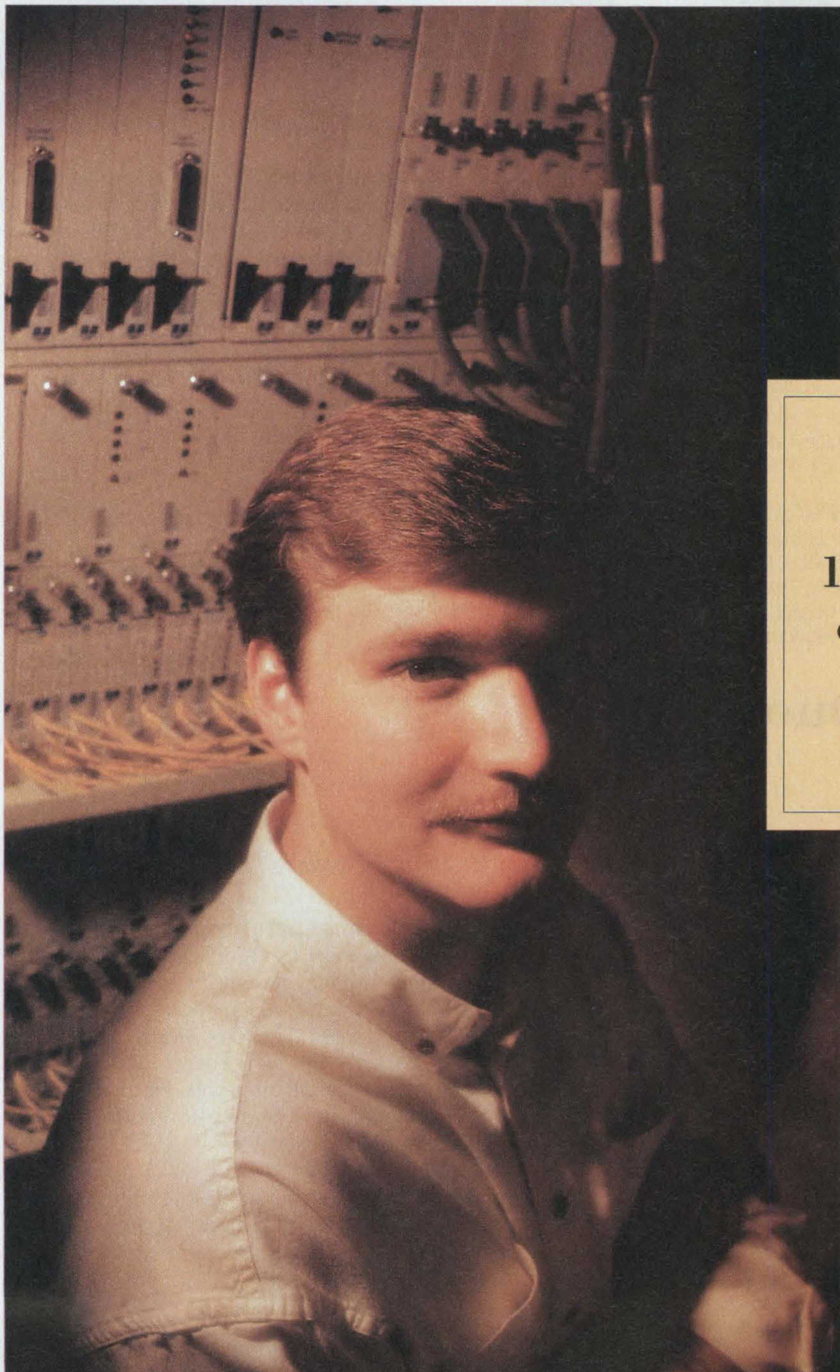
Corrections

Make the following corrections to DI #1351, "Line driver economically synthesizes impedance," by Victor Koren, EDN, January 6, 1994. Add V_{OZ} to the schematic as the output of IC_1. Change R_3 in the schematic to R_3'. $R_3'+R_{ADD}=R_3$. Change R_5 to R_S in equations. The circuit uses feedback, not "...a second op amp," to synthesize the output impedance. V_{OZ} is the output of IC_1, not "... the output voltage with the input shorted." Insert a parenthesis in equation 1 after the first R_3. The last equation should be

$$R_3=(R_S\times R_1+R_O\times R_2)/(R_O-R_S)$$

The output resistance of the circuit is proportional to $1/(R_3-R_2)$. R_3 and R_2 must be very accurate and are also close in value. An inexpensive and easy way to achieve these values is to split R_3 into R_3' and R_{ADD}. Then, making R_3', R_1, and R_2 the same value, you can use a resistor network and achieve good matching. The output resistance then becomes

$$R_O=R_S((2R/R_{ADD})+1).$$



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Signal Conditioning Applications? The AD7714 has everything you need: high resolution, low power, low component count and incredible versatility — all at an astonishingly low price!

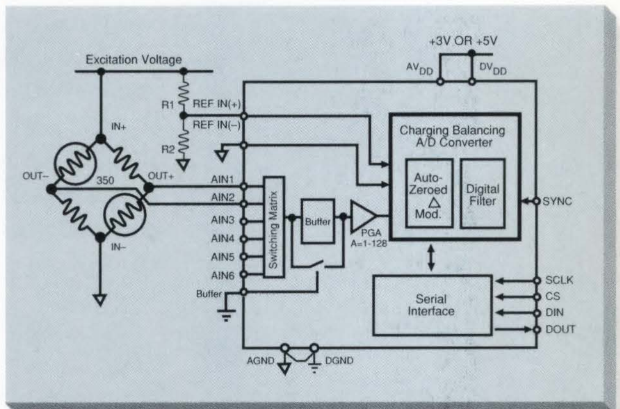
> **CONVERTERS**
>
> This guide describes some of the new converters from Analog Devices – the most interesting and innovative integrated circuits for digital-to-analog and analog-to-digital conversion that you can find anywhere in the world, from any manufacturer.
>
> High resolution, low cost, multiple channels, industry standard products, ground-breaking new devices — they're all here.
>
> The only exceptions are our range of fast converters — you'll find them, together with companion products, in our High Speed Products guide.
>
> And if you're interested in high speed data acquisition or control, you won't want to miss that.

The AD7714 is a complete analog front-end for low-frequency measurement applications. It includes a 5-channel programmable-gain front-end, 24-bit "no missing codes" charge-balancing ADC, low-pass filter and a 3-wire serial interface. It is completely under software control — gain settings, signal polarity, filter cut-off, calibration and channel selection can be configured using the input serial port.

Not convinced yet? The device operates from either 3V or 5V supply, and draws just 750μW (at 3V) and 50μW in sleep mode. RMS noise is typically 1.2μV and 300nV with gains of 1 and 128, respectively.

The AD7714 is available in a 24-pin DIP and SOIC, and is specified over the -40°C to +85°C temperature range.

1 AD7714 $11.00 in 1000s



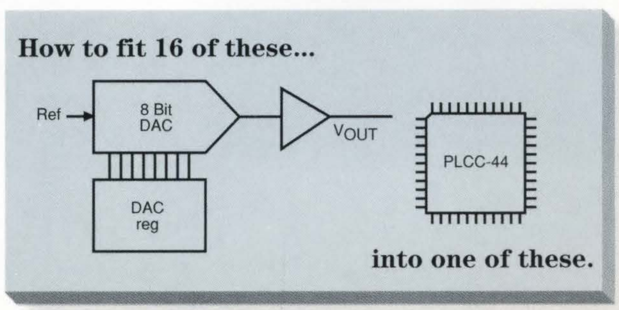
The diagram shows the AD7714 in a typical strain-gauge application, with four spare channels.

COMPACT 16-CHANNEL, 8-BIT MULTIPLYING DAC SAVES SPACE IN ATE, SONAR, ULTRASOUND, INSTRUMENTATION...

Multi-channel applications suddenly get a lot smaller, a lot better specified and a whole lot easier to design with the introduction of the AD8600.

Shoe-horning 16 independent 8-bit multiplying DACs into a compact (PLCC-44) package is impressive enough, but doing it with the performance we're offering is little short of a miracle (admittedly, a small miracle).

The AD8600 contains 16 independent voltage-output digital-to-analog converters that share a common external reference input voltage. Each DAC has its own DAC register and input register to allow double buffering. An 8-bit parallel data input, four address pins and control logic provide the high-speed digital interface. *Continued on back*



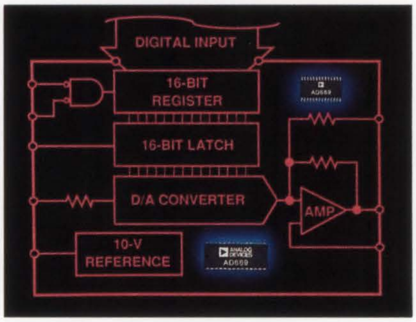
Squeeze 16 high-performance 8-bit DACs into less than 0.5 square inches (PLCC-44).

THE 16-BIT DACS YOU'VE BEEN WAITING FOR

The AD660 and AD669 are complete 16-bit, serial/byte and parallel input DACPORTs which provide leading-edge performance at down-to-earth prices. Their combination of high performance, complete functionality, flexible digital interface, small footprint and low price make them the perfect solution for 12-bit DAC users seeking to upgrade their systems without significantly increasing costs.

The AD660 and AD669 feature 15-bit monotonicity and accuracy over the entire industrial or military temperature range. They are fully AC and DC specified, and offer double-buffered latches, an on-board precision voltage reference and a pin-programmable output amplifier. Output can be either unipolar (0 to +10V) or bipolar (±10V).

These devices provide low-cost performance for a wide range of applications including industrial control, wireless communication, ATE, robotics, data acquisition and instrumentation.



2 AD660/9 $13.60 in 1000s

GROUND ZERO

Without a doubt, the single largest cause of problems in achieving the desired performance with data converters is grounding. At even low resolutions, good ground design is necessary to maintain the desired performance; for high-resolution devices it is absolutely crucial.

The best way to avoid them is to remember that "ground" isn't a magic current sink, but a connection through which currents flow to complete a circuit. Make their path smooth and your life easy!

- Have separate analog and digital grounds — and only connect them at one point.
- Check that noisy signals are kept away from sensitive ones — and that applies to return paths too.
- Where will the return currents flow?
- Are there any potential ground loops?
- Do the return paths have low enough impedance?
- Are the components well decoupled?
- Do you need a ground plane?

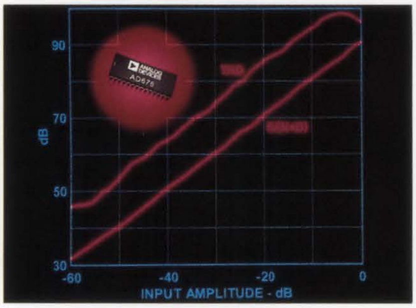
For more help call applications support: 1-800-ANALOGD.

TRUE 16-BIT ADCS AT A LOW PRICE (92dB AT 100KSPS FOR $25)

Your customers are asking you to. Your competitors are doing it. Your boss is ordering you to. Soon even your mother will be telling you to make the switch to 16-bit resolution. Thankfully, with the AD676 and AD677, you can make that move successfully and affordably. What's more, with these elegantly designed devices you get a host of other benefits too.

The AD676 and AD677 are 16-bit sampling ADCs which provide industry-leading performance, cost and space efficiencies. Their 92dB signal to noise ratio combined with ±1LSB integral non-linearity offer superior 16-bit performance at 100ksps throughput rates.

This high accuracy is a result of auto-calibration, which improves performance without the wasted board space and cost of external trims. A "ground sense" pin is included — invaluable if the signal has to be carried some distance to the A/D converter.



This combination of features makes the AD676 and AD677 the perfect solution for medical and analytic instrumentation applications as well as PC-based data acquisition and industrial applications like power supply monitoring and signal monitoring in transportation and industrial controls.

Both components are fully specified and tested for AC and DC parameters. The AD677 offers easy-to-interface three-wire serial output data. The AD676 offers full parallel output.

The AD676 is available in a 28-pin, ceramic, side-brazed package as well as a 28-pin plastic DIP. The AD677 is offered in a 16-bit skinny ceramic package and plastic DIP and 28-pin SOIC packages.

3 AD676 $27.14 in 1000s

4 AD677 $25.08 in 1000s

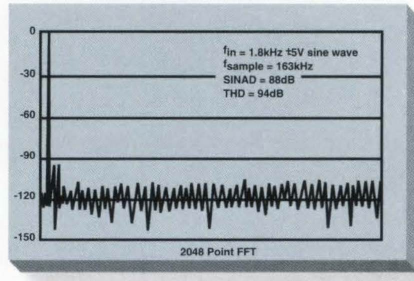
166KSPS AND 16-BIT RESOLUTION IN A LOW-POWER, LOW-NOISE ADC

The AD7884 and AD7885 are fast, monolithic 16-bit sampling ADCs. They offer true 16-bit resolution with 16-bit no missing codes, and a high throughput rate of 166ksps.

The AD7884 and AD7885 dissipate only 250mW of power. Features includes analog input ranges of ±3V and ±5V as well as parallel and byte interfacing (AD7884 and AD7885 respectively).

In medical and scientific instrumentation, noise is a critical requirement, and with their excellent noise performance (78µV rms at ±3V input range) the AD7884/5 are earning wide popularity. They also offer SNR of 86dB, while THD is -88dB.

The AD7884 is available in 40-pin cerdip and 44-pin PLCC packages. The AD7885 is available in a 28-pin DIP package while the AD7885A is available in a 44-pin PLCC package. Temperature ranges are -40°C to +85°C.



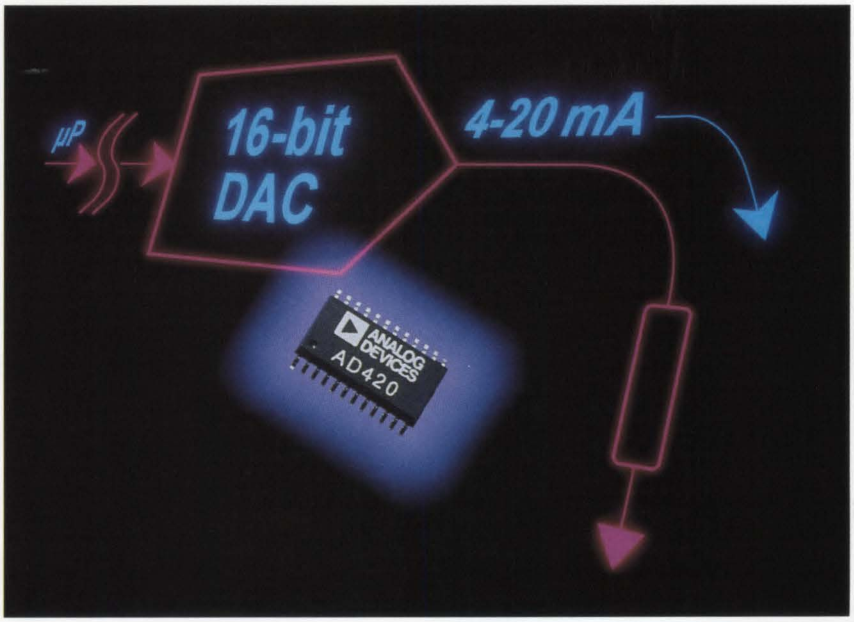
The AD7884/7885 are high performance 16-bit ADCs. Their high speed (6µs conversion time) and low noise (88dB SINAD) make them ideal for wide bandwidth signal processing applications.

5 AD7884/AD7885 $38.25 in 1000s

THE FIRST DIGITAL TO 4-20mA SYSTEM: NEW CHIP INTEGRATES DAC WITH LOOP DRIVER

16-Bit Industrial Control DAC

The AD420 is the only single-chip solution available for generating 4-20mA current loop signals from digital data. It is the first current-loop output DAC, and its high performance, low price and compact design make it perfectly suited for almost any industrial control application. It provides a single-chip solution for generating precision 4-20mA or 0-20mA signals, and runs on a single supply (up to 36V).



The AD420 has been designed to make the system engineer's life easier. It includes a 16-bit sigma delta DAC, for guaranteed monotonicity and excellent linearity. The loop driver circuitry includes a loop fault detect circuit, so a warning signal can be generated if the current loop is open circuited. It has an SPI®- and MicroWire®- compatible serial interface, and can interface seamlessly with most controllers. Furthermore, it is a completely specified part — there is no need to worry about component interaction or error budgets. Finally, although the chip can drive loops directly, it is a trivial matter to use an external boost transistor to extend the temperature range or obtain lower drift performance.

Typical applications for this unique product include valve and motor control in a wide variety of industrial applications. It is ideal for use in distributed control systems (DCS), programmable logic controllers and data I/O cards and modules. Its uses range from plant or process automation to single PC-based control systems.

24 pin PDIP or SOIC, temperature range -40°C to +85°C.

6 AD420 $10 in 1000s

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FLEXIBLE, ACCURATE QUAD 12-BIT DAC — EASY TO SET OUTPUT VOLTAGE RANGE

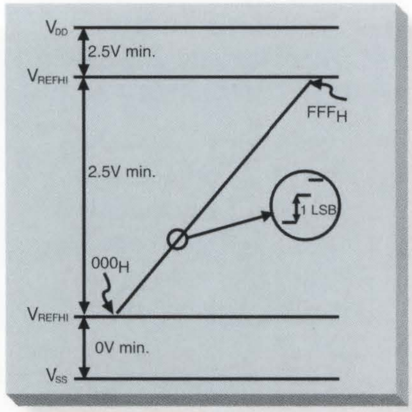
The Only DC Setpoint D/A Converters You'll Ever Need.

This family of quad 12-bit voltage-out D/A converters provides all the features most designs will ever need, plus the low cost every design requires — all in a small footprint package.

Because you may want unipolar, bipolar or asymmetric outputs, they provide separate VREF high and VREF low inputs and a single-supply output op amp — so it is trivial to set exactly the output range you need. And unlike some parts, that means both positive and negative outputs are available.

The voltage-switched DAC architecture offers the best overall accuracy available from a quad 12-bit converter (including offset and temperature accuracy).

These DACs all operate from a wide range of supply voltages (+5V to ±15V). Their high speed (80ns data load timing for DAC8412/13, or 12MHz clock for DAC8420) combines with low power dissipation to meet performance requirements while reducing power supply and cooling demands.



	Interface:	State at Reset (RST strobe):	Price:
7 DAC8420	Serial	Programmable (mode pin)	$25.16 in 1000s
8 DAC8412	Parallel	Reset to zero	$24.26 in 1000s
9 DAC8413	Parallel	Reset to midscale	$24.26 in 1000s

MAKE IT EASY

Life is hard enough already — but when it comes to helping you get converter circuits to work, Analog Devices' applications engineers have more experience than anyone else in the world — just give them a call.

Some of this experience is available in ready made forms; evaluation boards allow you to easily appraise a component, but also offer a well-designed and fully tested circuit that can be used as a reference design. And data sheets give circuit designs and pcb layouts.

There are a number of application notes that offer ideas or advice. Some of the more popular include:

- Getting the most from high resolution digital-to-analog converters **A**
- Analog signal handling for high speed and accuracy **B**
- Differential and multiplying D/A applications **C**
- DAC ICs: How many bits is enough? **D**
- An IC amplifiers guide to decoupling, grounding and making things go right for a change **E**

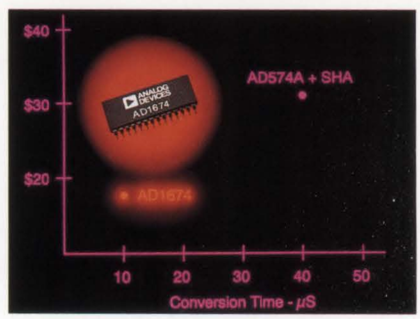
USING THE INDUSTRY STANDARD AD574? THEN MOVE UP TO THE AD1674

When Analog Devices introduced the AD574, it quickly became the industry standard. Now, the AD1674 takes that standard to yet another level.

The AD1674 is a high-performance sampling 12-bit A/D which offers users of the AD574 family (AD574, AD674, AD774) an instant upgrade with up to three times the speed, along with lower power and greater accuracy. It utilizes the AD574 pinout for easy replacement in existing designs, providing increased capabilities while reducing costs through the elimination of external SHA and support circuitry.

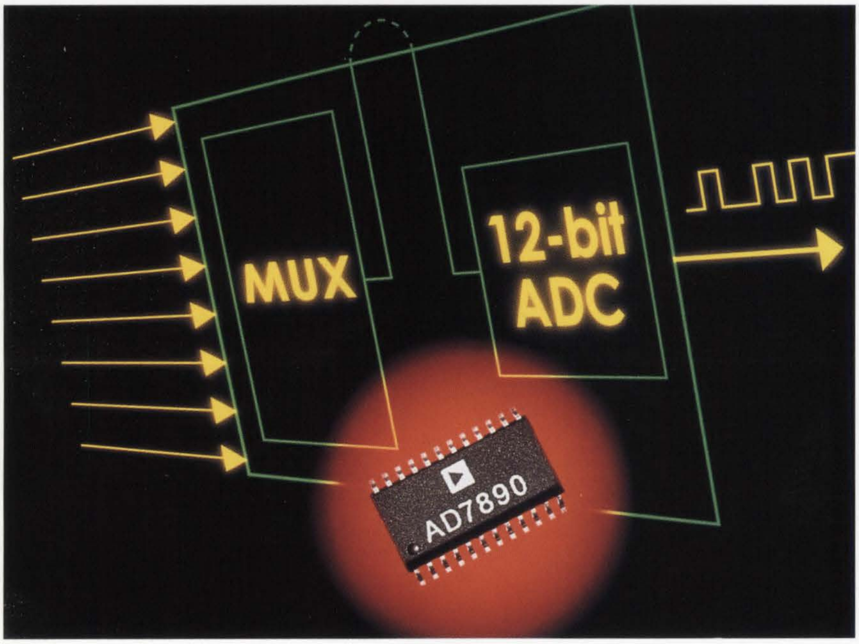
The power and versatility of the AD1674 make it an ideal general-purpose converter for a wide variety of applications ranging from industrial control to data acquisition and instrumentation. Additional features include ±5V, ±10V, 0–10V and 0–20V input ranges, internal reference, 8- and 16-bit microprocessor interfaces and a wide selection of package styles.

The AD1674 is available in 28-pin PDIP and 28-pin SOIC packages in commercial and industrial temperature ranges as well as in a 28-pin side-brazed ceramic package for industrial and military ranges. All specifications are both AC and DC guaranteed. Full MIL-883B and SMD devices are also available.



10 AD1674 $11.60 in 1000s

A NEW GENERATION OF 12-BIT ADCS, WITH UNMATCHED PERFORMANCE, SINGLE 5V POWER SUPPLY OPERATION, ROBUST INPUT CIRCUITRY AND EASE OF USE IN A COMPACT DESIGN.



THE SMALLEST 12-BIT ADC

A single-channel ADC in a tiny 0.15" wide 8-pin SOIC package.

The AD7893 provides a throughput rate of 117ksps, with a power dissipation of less than 50mW. It handles data transfer via a two-wire serial interface.

OCTAL ADC–7X SAVINGS IN SIGNAL CONDITIONING

The AD7890 is an eight-channel version which offers a seven-fold savings in channel support circuitry over other integrated solutions. This economy is possible because access to MUXOUT means that the same signal-conditioning circuitry can be used for all eight channels. The AD7890 has a throughput rate of 100ksps. It also features a power dissipation of less than 50mW, and on-chip reference.

Robust Inputs

Both parts are available with three distinct input range options. Like the AD7892, they operate from a single 5V power supply, and their analog inputs are tolerant to voltages which extend well outside of the supplies, protecting them from overvoltage fault conditions (up to 17V outside for the -10 version).

11 AD7890 $10.20 in 1000s
12 AD7893 $8.00 in 1000s

AD7890-2	0–2.5 V
AD7890-4	0–4 V
AD7890-10	+/- 10 V
AD7893-2	0–2.5 V
AD7893-5	0–5 V
AD7893-10	+/- 10 V

FASTER SIGNALS AND CLEARER RESULTS — THE HIGHEST SINAD SPECS FROM A COMPLETE 12-BIT 1.25MSPS ADC

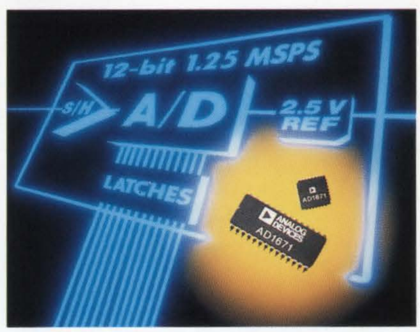
The AD1671 delivers leading-edge performance from a complete converter — with on-chip reference and wide bandwidth, high impedance sample-and-hold amplifier.

The AD1671's exceptional dynamic performance includes 69dB SINAD, a full power bandwidth of 2MHz and a small signal bandwidth of 12MHz. This allows better, faster data acquisition — delivering sharper images from scanners or clearer signals from communication links.

The AD1671 performance and price breakthrough are enabling markets that were previously prohibited by cost, power or price constraints. They include communications systems (high speed modems, base stations, HDSL), imaging (color scanners, medical imaging, IR) and high-speed data acquisition.

The AD1671 is available in both a 28-pin cerdip and 28-pin PLCC package, in commercial, industrial and DESC versions.

13 AD1671 Less than $40 in volume.



TINY, COMPLETE SINGLE SUPPLY DACS — SMALLEST PACKAGES, EASIEST TO USE

Total DAC System — In the Industry's Smallest Packages

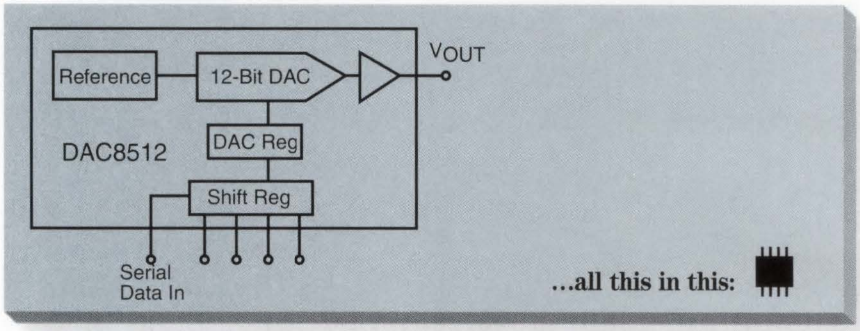
The DAC8512, DAC8562, AD8522 and AD8582 are a set of single-supply 12-bit DACs, offering a complete "plug and play" output system. Everything there, everything included, everything tested and specified. And everything squeezed into a tiny SO-8 package (DAC8512).

Each part includes all the related circuits — bandgap reference, voltage-switched R-2R ladder DAC, and an output rail-to-rail op amp. Full-scale voltage of 4.095V with 1mV/bit output coding creates a programming-friendly environment while maximizing the analog output swing for all loads.

These parts also feature low power dissipation of 3mW/DAC and compact designs which make them ideal for portable or battery-operated equipment.

The 8- and 14-pin count DAC8512 and AD8522 serial parts also offer the industry's smallest surface mount packages to reduce space consumption.

	Channels:	Interface:	Package:	Price:
14 DAC8512	Single	Serial	SO-8 / DIP-8	$4.49 in 1000s
15 DAC8562	Single	Parallel	SOL-20 / DIP-20	$7.52 in 1000s
16 AD8522	Dual	Serial	SO-14 / DIP-14	$7.86 in 1000s
17 AD8582	Dual	Parallel	SOL-24 / DIP-24	$9.44 in 1000s



12-bit DAC in SO-8 package

PROBABLY THE BEST VOLTAGE REFERENCE IN THE WORLD

5V voltage reference — low dropout, low power, high accuracy

Many of our converters are available with built-in voltage references, but sometimes you want to use an external reference. And when that's true, there is no better choice than the REF-195.

To say that this has been popular would be an understatement — it has been a scorching success, with thousands of applications and millions shipped. And when you look at the specifications, it is obvious why — a 5V micropower reference with only 0.1V drop-out, low power (just 45μA) and high accuracy (±3mV). What's more, because it can source up to 30mA, the REF-195 can act as both a precision voltage reference and a highly efficient voltage regulator. And all that for an astonishingly low cost — what more could you look for in a reference?

18 REF195 $1.94 in 1000s

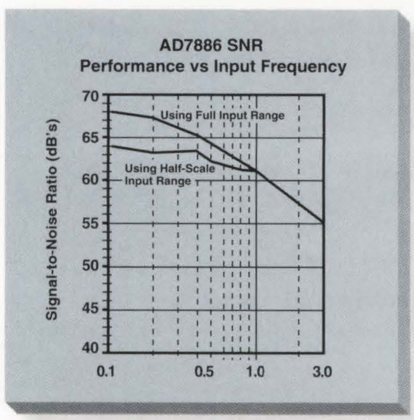
HIGH PERFORMANCE 12-BIT ADC SAMPLES ACROSS WIDE DYNAMIC RANGE

The AD7886 is a high-speed, power-efficient 12-bit ADC with a throughput rate of 1Msps. Its high performance makes it ideal for sampling applications requiring a broad dynamic range over a large bandwidth, as well as high-speed and multiplexed data acquisition systems. The full-power bandwidth of the on-chip sample-and-hold extends well above the 500kHz Nyquist limit, allowing the AD7886 to be used in undersampling systems in addition to the standard signal-processing applications.

The AD7886 has a low power dissipation of 250mW, and is comprehensively specified for AC and DC parameters. It features a high speed interface with 57ns bus access times, making it directly compatible with DSPs and microcontrollers.

It is available in 28-pin DIP and 28-pin surface mount packages. Temperature ranges are -40°C to +85°C for the industrial grades and -55°C to +125°C for the extended range.

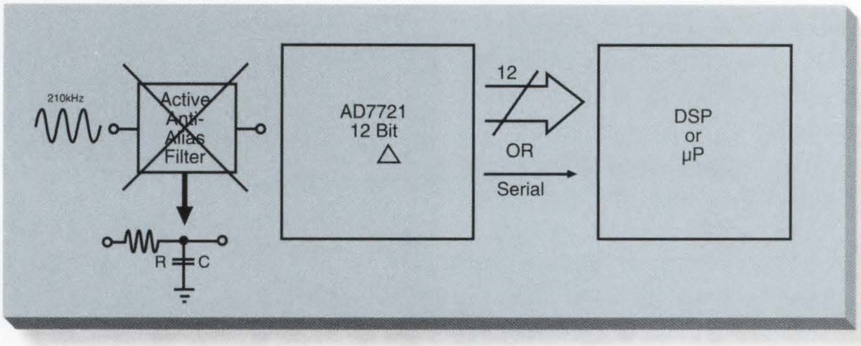
19 AD7886 under $40 in 1000s



The full power bandwidth of the SHA allows the AD7886 to sample up to 1MHz bandwidth — ideal for undersampling applications.

THE WIDEST RANGE OF 12-BIT DEVICES IN THE INDUSTRY

FAST 12-BIT SIGMA-DELTA ADC ELIMINATES NEED FOR ACTIVE ANTI-ALIASING FILTER



The AD7721 is a 12-bit sigma-delta ADC with a 200kHz bandwidth and an output word rate of 470ksps.

It offers all the advantages of digital filter design, including freedom from the component matching or drift issues commonly associated with analog filters. It also drastically simplifies the design of the input anti-aliasing filter — in many cases no filter other than a simple RC roll-off is required. Other advantages include device-device repeatability, linear phase characteristics and dramatic improvement in SNR.

Operating from a single 5V supply, the AD7721 dissipates only 175mW of power while supporting a full-power signal bandwidth of 200kHz. Other features include an on-chip reference and a choice of either parallel or serial interfacing, a power-down mode and pseudo-differential inputs. It also offers a calibration mode to minimize offset and gain errors.

The AD7721 is available in 28-pin plastic DIP, SOIC and cerdip packages. Temperature ranges are -40°C to +85°C or -55°C to +125°C for the extended grade.

20 AD7721 $13.60 in 1000s

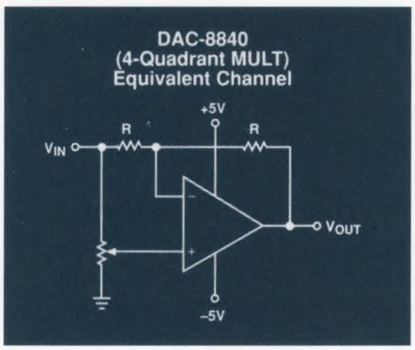
TRIMDACS REPLACE TRIMMERS AND POTS — FOR LESS THAN $1.00 EACH

Question: What's the cheap, efficient and reliable way of removing adjustment trimmers and potentiometers from your designs?

Answer: Replacing them with TrimDACs.

The TrimDAC® Family of octal, 8-bit serial-input digital-to-analog converters provides a low-cost way to replace mechanical components, improving performance and reducing PC-board space. Not only can trimming now be digitally controlled, but performance and reliability can be dramatically improved. By using thin-film resistor technology, the TrimDAC family provides better temperature stability performance than traditional potentiometer solutions.

The TrimDAC family reduces space requirements by providing eight independent gain channels in 20- and 24-pin packages, guaranteed to operate over the extended temperature range (-40°C to +85°C). Other features include low-power dissipation and 3-wire serial μcontroller interface to simplify periodic service or remote adjustment.



For DC adjustment, the DAC8800 provides high and low reference inputs to establish the output swing. For AC signals, the DAC8840 features 4-quadrant multiplying adjustment for inputs up to 1MHz, while the AD8842 is suited for lower bandwidths (50kHz) at a lower price and half the power requirement.

21 DAC8800 $6.60 in 1000s
22 DAC8840 $8.36 in 1000s
23 DAC8841 $8.36 in 1000s
24 AD8842 $5.69 in 1000s

TrimDAC is a registered trademark of ADI.

12-BIT MDACS — CHEAPER SMALLER, BETTER

Upgrading your design with the latest generation of 12-bit multiplying DACs couldn't be easier. The AD7943/45/48 set new standards in performance, power efficiency and cost. And feature pin-outs compatible with the industry standard AD754x DACs.

The AD794x series feature significantly improved accuracy, fast 600ns settling time, and low 60nV-secs glitch energy. They also feature the fastest digital interface available anywhere -40ns pulse width. Operating from a single +3V or +5V supply, power consumption is a miserly 1mW.

For new designs, the AD794x series lets you save valuable space; all devices are available in ultrasmall 20-pin SSOP packages, which use less than 0.1 square inch of precious board space.

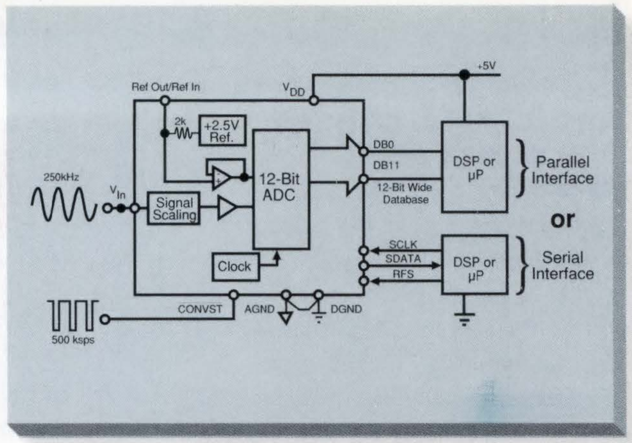
The AD7943, AD7945 and AD7948 provide serial, parallel and byte digital interface, respectively. In addition to the SSOP, industry standard packages are available. These devices are specified over the -40°C to +85 °C temperature range.

28 AD7943/45/48 $4.90 in 1000s

12-BIT 500KSPS ADCS THAT SURVIVE OVERVOLTAGE!

Real-world data acquisition and control systems often have to cope with tough environments. It isn't always possible to guarantee which system will power up first. Sometimes signals on input lines can go out of range — even beyond the supply rails. Until now, this was a guarantee for destroying your ADC — and that was an expensive fuse!

The ADC7892 is a versatile, high-speed ADC expressly designed to cope with these circumstances. It is a 12-bit sampling A/D converter with a throughput rate of 500ksps, low power dissipation of only 60mW and the flexibility of both serial and parallel interface capability. Crucially its analog inputs are tolerant to voltages which extend well outside of the supplies; this resilience protects them from overvoltage fault conditions (up to ±17V outside supply range for the ±10V input version). It also features an on-chip reference, as well as a power down mode.



The AD7892 is available in two versions. The AD7892-2 has an analog input range version of 0 to 2.5V for complete 5V single-supply systems. The AD7892-1 has input ranges of ±5V and ±10V for industrial-type systems where the larger LSB sizes are important.

Both versions are available in 24-pin plastic DIP, SOIC and cerdip packages. Temperature ranges are -40°C to +85°C for the industrial grades and -55°C to +125°C for the extended range.

25 AD7892 $13.60 in 1000s

A HIGH-RESOLUTION A/D CONVERTER, MOTOR CONTROLLER AND ISOLATION DEVICE FOR ONLY $2.95

The AD654 provides designers with a converter that can be applied to solve a wide range of design problems at much lower cost than ever before possible.

It is a monolithic V/F converter which reduces space requirements by integrating an input amplifier, precision oscillator system and a high-current output stage. Its high performance, low cost, low power consumption and small size make it the perfect choice for an unlimited variety of applications.

The AD654 provides a square wave output and can drive up to 12 TTL loads, opto-couplers, long cables or similar loads. The input amplifier provides low drift, permitting operation directly from low level transducers like thermocouples, strain gauges and current shunts. It also offers a high (250MΩ) input resistance to positive voltage signals. Only 2.0mA of quiescent current is required using the single positive supply from 4.5V to 26V, and the output stage can sink up to 10mA with saturation voltage less than 0.4V.

The AD654 combines low cost with very high accuracy. Linearity error is only 0.03% for a 250kHz full scale frequency, and operation is guaranteed over an 80dB dynamic range. A single RC network is all that's needed to set up any full scale frequency up to 500kHz.

Applications for this product range from high-resolution A/D converters, process control systems, and isolation to energy management, motor speed controls and power monitoring.

The AD654 is available in 8-pin PDIP and 8-pin SOIC packages in commercial temperature ranges.

26 AD654 $2.95 in 1000s

Continued from front

Finally, the AD8600 features a new DAC design (patent-pending) which reduces reference glitch during reprogramming.

Space savings is a major benefit of this part, since it provides all these capabilities in a PLCC-44 package. But other features include: simplified full-scale setting; fast 2µs settling time for fast updates for analog instrument systems; minimal (2mV) zero level system errors; and fast (30ns) data loading write times. A data readback feature allows system self-check at power-on.

The AD8600 operates from dual ±5V or single +5V supplies, in extended temperature range —(-40°C to +85°C).

27 AD8600 $25.28 in 1000s

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Analog Devices, Inc.
P.O. Box 9106
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Tel: (800) 262-5643
Fax: (617) 326-8703

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ANALOG DEVICES

Designing 2.1V Futurebus+ termination system requires system-engineering approach

Samuel H Duncan and Robert V White, Digital Equipment Corp

Designing a termination system for a Futurebus+ power system can be a formidable task. Tight voltage tolerance and ripple-noise specifications require an approach that considers the power supply, backplane, termination, and backplane-transistor-logic drivers as interconnected units.

The demands placed on a 2.1V Futurebus+ termination power system require a system-engineering approach. With the Futurebus+, worst-case switching conditions can inject a transient on the power-supply backplane that has a current change vs time (di/dt) greater than 3A/nsec. Most power supplies can withstand only a 1A/msec load transient. To meet the Futurebus+'s demanding requirements, Digital Equipment Corp has designed a system that attaches a tightly integrated power supply directly to the Futurebus+'s backplane. The design procedure, although not exactly a "cookbook" approach, should help experienced engineers design a Futurebus+ system.

DEC's approach mounts only passive components onto the backplane because replacing defective active components requires expensive service. The design uses only one power supply, which, although not part of the backplane assembly, plugs directly into the backplane. Bypass capacitors on the backplane lower the impedance of the 2.1V power supply so that voltages at the terminators remain stable. A system approach considers the terminators, backplane, and power supply.

Before considering the power system, review the requirements for the 2.1V backplane. The two most important requirements are the voltage tolerance and the output-load current. The Futurebus+ standard specifies that the output voltage must be within ±2% of 2.1V and have a voltage ripple lower than ±50 mV. The ±2% tolerance includes variations in initial tolerance, line regulation, average dc regulation, temperature drift, long-term drift, and ripple and power-supply noise. Because of the switching actions of the bus, the design must meet the ±50-mV specification at the terminators, not at the power-supply output.

Meeting the ±2% power-supply tolerance can be challenging. DEC systems use reference voltages having a tolerance of only 0.25%. Although tight tolerance references are expensive, they eliminate voltage trimming in the factory. Bypass

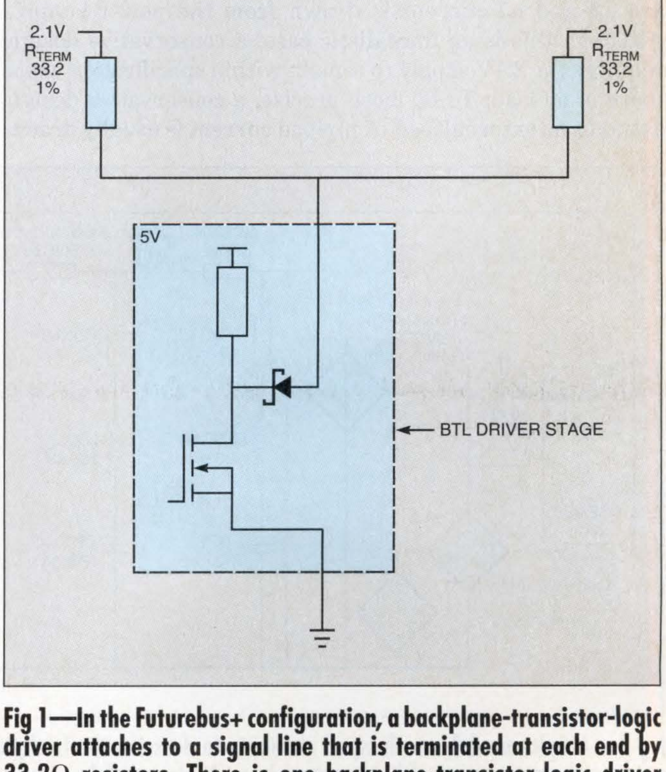

Fig 1—In the Futurebus+ configuration, a backplane-transistor-logic driver attaches to a signal line that is terminated at each end by 33.2Ω resistors. There is one backplane-transistor-logic driver stage for each signal line on the trace.

capacitors that maintain the ±50-mV ripple specification attenuate power-supply and ripple noise. However, load current can introduce dc-distribution losses. You can calculate the minimum and maximum load current, even though the current is stochastic.

To determine the load-current bounds, consider a Futurebus+ active single driver and two backplane 33.2Ω resistor (**Fig 1**). When any signal line is in the low state, the driver draws current from the 2.1V supply. Typical current draw/signal line is:

$$I_{typ}=2\times(V_{term}-V_{low})/R_{term}$$
$$I_{WC}=2\times(2.10V-1V)/33.2\Omega=66.3\text{ mA}.$$

The 66.3 mA is a typical current draw. In worst-case conditions, the terminator voltage can be as high as 2.142V, and the logic low voltage can be as low as 0.75V. In addition, the terminator resistors have a ±1% tolerance. Adjusting for worst-case parameters, the worst-case current is:

$$I_{WC}=2\times(2.142V-.75V)/32.868\Omega=84.7\text{ mA}.$$

A 6-slot backplane having a 64-bit data bus has 130 signal lines that can draw current from the power supply when you include the arbitration signals. Generally, no more than 100 lines switch simultaneously, however. Therefore, 100 signal lines, each drawing 66.3 mA, typically draw 6.63A total current from the power supply. The absolute worst-case condition occurs when 130 lines draw 84.7 mA, resulting in an 11A current draw from the power supply. This is an unrealistic case, however. A worst case of 10A is more likely.

The minimum load current occurs when all of the drivers are off and no current is drawn from the power supply. Although this is an unrealistic case, a conservative design requires the 2.1V supply to remain within specification when there is no load. To be more precise, a conservative design assumes no external load. A preload current is usually drawn from a switching power supply to keep the power supply operating in its linear, continuous mode. This design uses a preload current of 0.5A, which dissipates only 1W. If you use a linear regulator, the preload current biases the pass transistor into its active region.

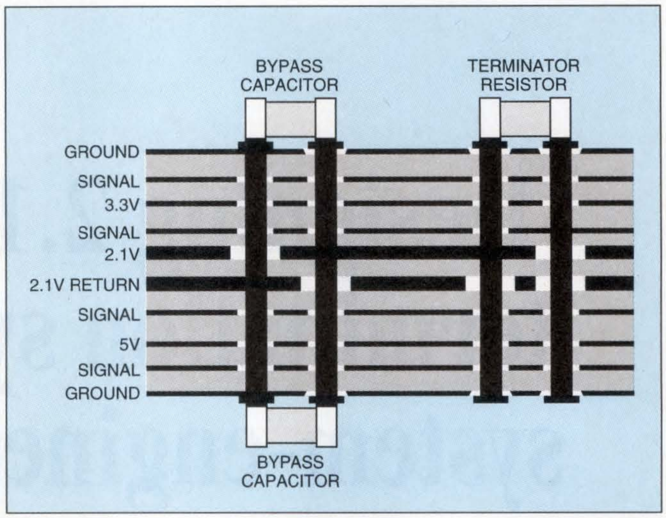

Fig 2—This backplane-layering and bypass-capacitor connection places dual bypass capacitors as close as possible to the termination resistor and 2.1V line.

To meet the 50-mV specification, assume that 100 signal lines can change at once and that the bus switches in a minimum of 2 nsec. The load transient under these conditions is 6.6A/2 nsec=3.3A/nsec. In practice, the load transient is not this large. Because of bus skew, all the signals do not arrive simultaneously at the terminators. The terminator resistors' inductance also slows the rise of the current transient on the 2.1V backplane. However, to find the worst-case load transient, this design ignores these factors.

Consider the complete power-supply system when determining the voltage at the terminators. Designing a backplane by throwing in some random bypass capacitors and hooking up a power supply using 1m of cable does not work. Designing a complete power system means considering the terminator resistors, 2.1V layers in the backplane, bypass capacitors, backplane to the power-supply connectors, and power-supply output. The DEC design uses Spice to simulate the system, although it can use a lumped-element model because the 2-nsec backplane doesn't require a transmission-line model. The Spice model describes the load as a series of resistance and time-varying voltages.

Locate the 2.1V power line and its return on adjacent layers and on inner layers of the backplane to minimize impedance. This arrangement reduces inductance and increases capacitance. The design requires a 2-oz-thick min

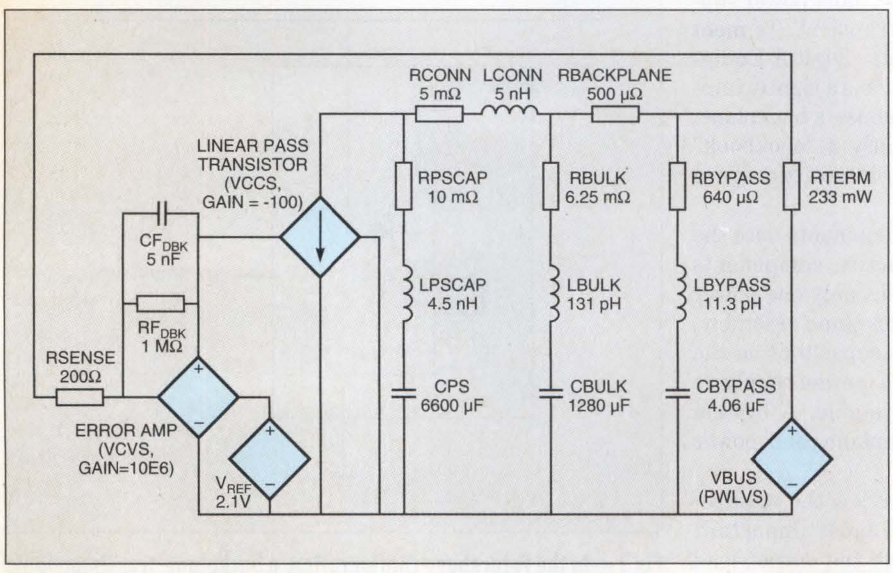

Fig 3—A Spice model uses lumped elements to describe the backplane impedance and the staggered arrangement of bypass capacitors. It also models a linear voltage regulator and the connector impedances.

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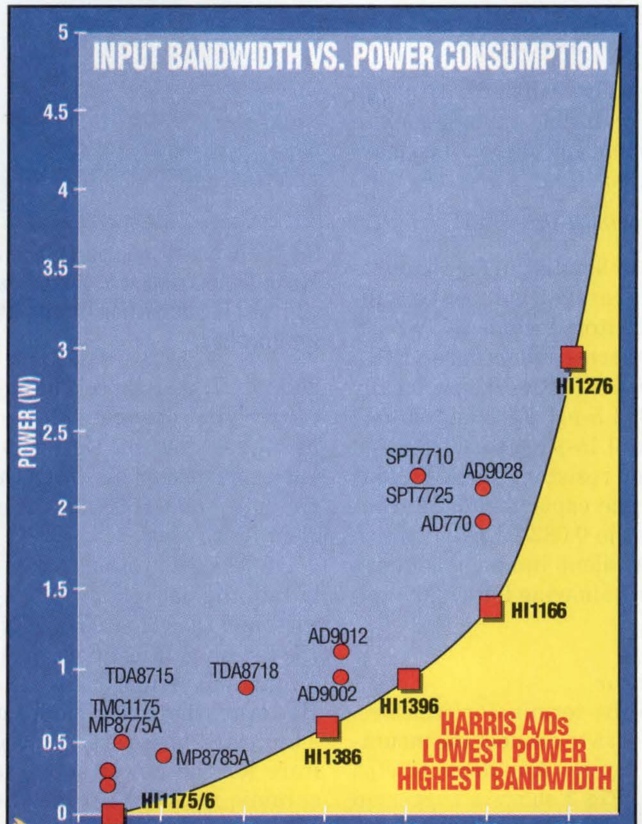

A/D Family Features

HI1276, 8-bit, 500 MSPS
- 300 MHz input bandwidth
- 2.8 W power consumption

HI1166, 8-bit, 250 MSPS
- 250 MHz input bandwidth
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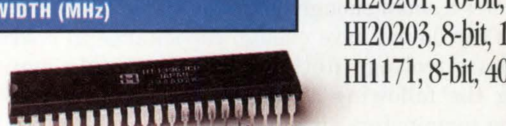
HI1396, 8-bit, 125 MSPS
- 200 MHz input bandwidth
- 870 mW power consumption

HI1386, 8-bit, 75 MSPS
- 150 MHz bandwidth
- 580 mW power consumption

HI1175/6, 8-bit, 20 MSPS
- 18 MHz bandwidth
- 60 mW power consumption
- Built-in voltage reference

D/As also available:

HI20201, 10-bit, 160 MHz update rate
HI20203, 8-bit, 160 MHz update rate
HI1171, 8-bit, 40 MHz update rate



Nothing runs as far and as fast on so little power as a Harris data converter. Except maybe these high-energy in-line skates. On a single kick, they attain a theoretical straight-line speed of 115 mph, and maintain that speed for 45 minutes. (Actual specs will be available following the completion of a 86.25-mile test sidewalk.)

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FUTUREBUS+ TERMINATORS

copper line. Connect the 2.1V power supply to the backplane near the center of the board, which is equidistant from the terminators. Using this arrangement, the distribution resistance of the power-supply plane is about 500 μΩ.

In selecting bypass capacitors, calculate the minimum capacitance to hold up the 2.1V terminator voltage until the power supply can respond, and calculate the maximum amount of inductance allowed on the 2.1V distribution line. The DEC design calculates the capacitance and inductance for a linear power supply to maintain a 50-mV ripple voltage. Supply response time is 50 μsec. Estimating the capacitance based on allowing no more than 50 mV of droop in 50 μsec yields:

$$C=I\times dt/dV=6.6A\times 50\ \mu sec/50\ mV=6600\ \mu F.$$

Estimating the inductance yields:

$$L=V\times dt]/di=50\ mV\times 2\ nsec/6.6A=15.2\ pH.$$

The capacitance is large but physically realizable. Although the inductance is too small to be realizable, many terminators contribute to this lumped-element calculation. The maximum inductance for a terminator is:

$$L=V\times dt/di=50\ mV\times 2\ nsec/33.1\ mA=3\ nH.$$

Although the 3-nH inductance is small, surface-mount-technology (SMT) capacitors are available with subnanohenry inductances. Such capacitors include a 0.082-μF capacitor with 0.7-nH effective series inductance (ESL) and 40-mΩ effective series resistance (ESR). The company also offers a 0.15-μF model with 1.5-nH ESL and 70-mΩ ESR. Designs incorporating the 0.15-μF capacitor need only one capacitor/two terminator resistors; designs with the 0.082-μF capacitors require one capacitor/four terminator resistors. This design uses the 0.082-μF part, which requires 62 capacitors. The equivalent lump-capacitance sum is 5.08 μF (4.07 μF worst case, allowing for a ±20% tolerance).

Place capacitor close to terminator

Place these capacitors close to the terminator resistors. The design requires at least three vias to connect the mounting pads to the 2.1V and return layers. Any discrete etch noticeably degrades performance. **Fig 2** shows a suggested backplane-layer and capacitor-connection scheme. Although the capacitors have a small enough inductance to support the load transient, they do not have enough capacitance to hold up the terminator voltage until the power supply can respond. Using the following approximation, the bypass capacitors at the terminators should hold up the voltage for only a few nanoseconds:

$$dt=C\times dV/I=5.08\ \mu F\times 50\ mV/6.6A=38\ nsec.$$

The above equation shows that the design requires at least another stage of capacitors to hold up the voltage. Each terminator requires no more inductance than the that of the following equation:

$$L=V\times dt/di=50\ mV\times 38\ nsec/33.1\ mA=57\ nH.$$

This is a reasonable amount of inductance to provide the additional hold time. The design includes 16 100-μF SMT electrolytic capacitors on the backplane between the termination resistors and the point at which the termination power enters the backplane. Even though the total capacitance does not quite equal 6600 μF, the electrolytic capacitors are sufficient for the task.

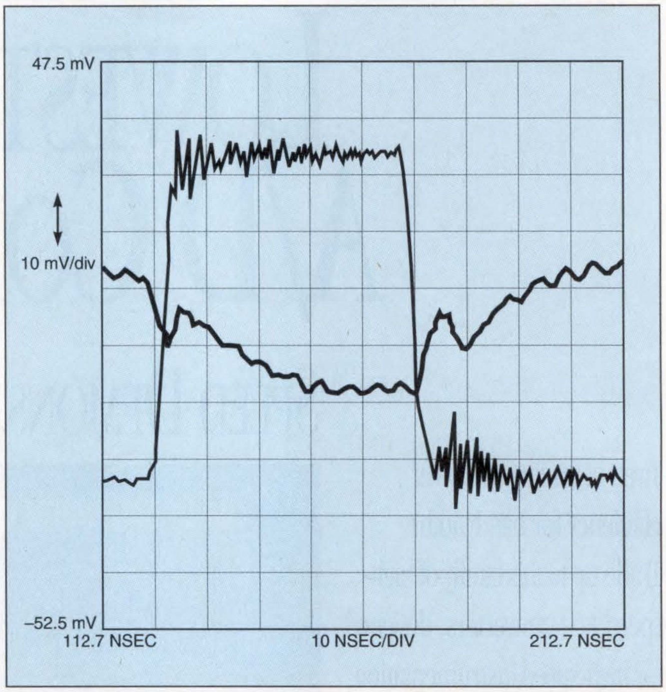

Fig 4—In the system backplane with all lines switching simultaneously, the maximum observed deflection on the 2.1V terminator is ±24 mV. The deflection is comfortably within the 50-mV Futurebus+ specification.

DEC's first systems use power modules that plug directly into the backplane. One system uses card-edge connectors, and the other uses DIN-style power pins and sockets. Direct plug-in connection to the backplane results in a minimum amount of resistance and inductance parasitics. However, the Spice model must include these parasitics. The design uses three 2200-μF, low-ESR aluminum capacitors for the power-supply output. It also uses 0.220-μF ceramic capacitors at the power-supply connection to filter high-frequency noise.

To meet the Futurebus+ specifications, the design staggers an array of capacitors throughout the backplane in three stages. The first stage comprises 0.082-μF, high-frequency bypass capacitors near the terminator resistors. The second stage, an array of 100-μF electrolytic capacitors, provides the bulk storage. The third stage includes the power-supply output capacitors. **Fig 3** shows a simplified schematic of the Spice model for the final design.

The Spice model predicts that the configuration can meet the Futurebus+ specification under worst-case switching conditions of the bus. You can test this condition by building an exerciser for the Futurebus+ that allows the simultaneous transition of any number of signal lines. When all lines are

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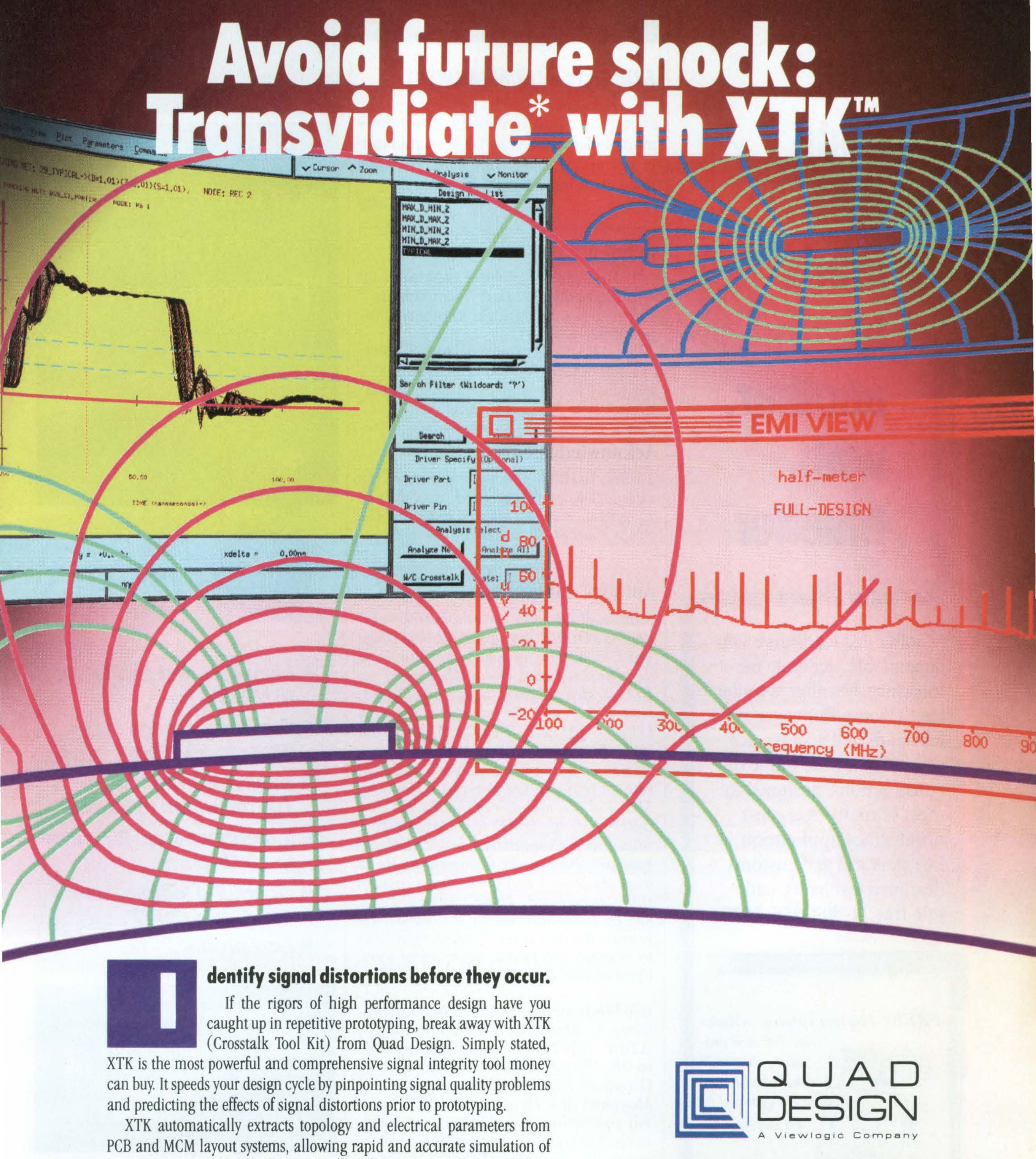

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switching simultaneously, the maximum deflection on the 2.1V terminator is ±24 mV (**Fig 4**), comfortably within the Futurebus+ 50 mV specification.

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1. Hayward, C, "Noise generated by simultaneous signal transitions," Futurebus+ design, September/October 1992, pg 35-37.
2. IEEE Standard 896.2-1991, "IEEE Standard for Futurebus+—Physical Layer and Profile Specifications," New York, NY, 1992.

Acknowledgment

Thanks to Bill Samaras, who created the staggered-capacitor idea, and Bruce Loughlin, who performed much of the Spice simulation and other research.

Authors' biographies

Samuel H Duncan is a consulting engineer for Digital Equipment Corp, Maynard, MA. For 15 years, he has done development and consulting work on I/O architectures and interfaces, firmware, and diagnostics. He also helped develop the DEC 4000, 7000, and VAX 8800 computers. Duncan has a BSEE in applied math and computer science from Tufts University, Medford, MA, and is a member of the IEEE Computer Society, IEEE Bus Architecture Standards Committee, and IEEE µP and µC Standards Committee. He is also chairman of the working groups that developed IEEE 1212.1-1993, 896.1a-1993, and 896.2a standards. He is married; has three children; and likes to restore his home, sail, wind-surf, bycycle, and ski.

Bob White works for AT&T Bell Laboratories in Mesquite, TX. Before joining AT&T, White was a principal engineer in the Power Systems Engineering Group at Digital Equipment Corp in Maynard, MA. He served as DEC's internal consultant on power-related issues in the Futurebus+ specification development. He was also the power-system architect and technical-team leader for the DEC 4000 computer system. White is the technical vice president of the IEEE Power Electronics Society.

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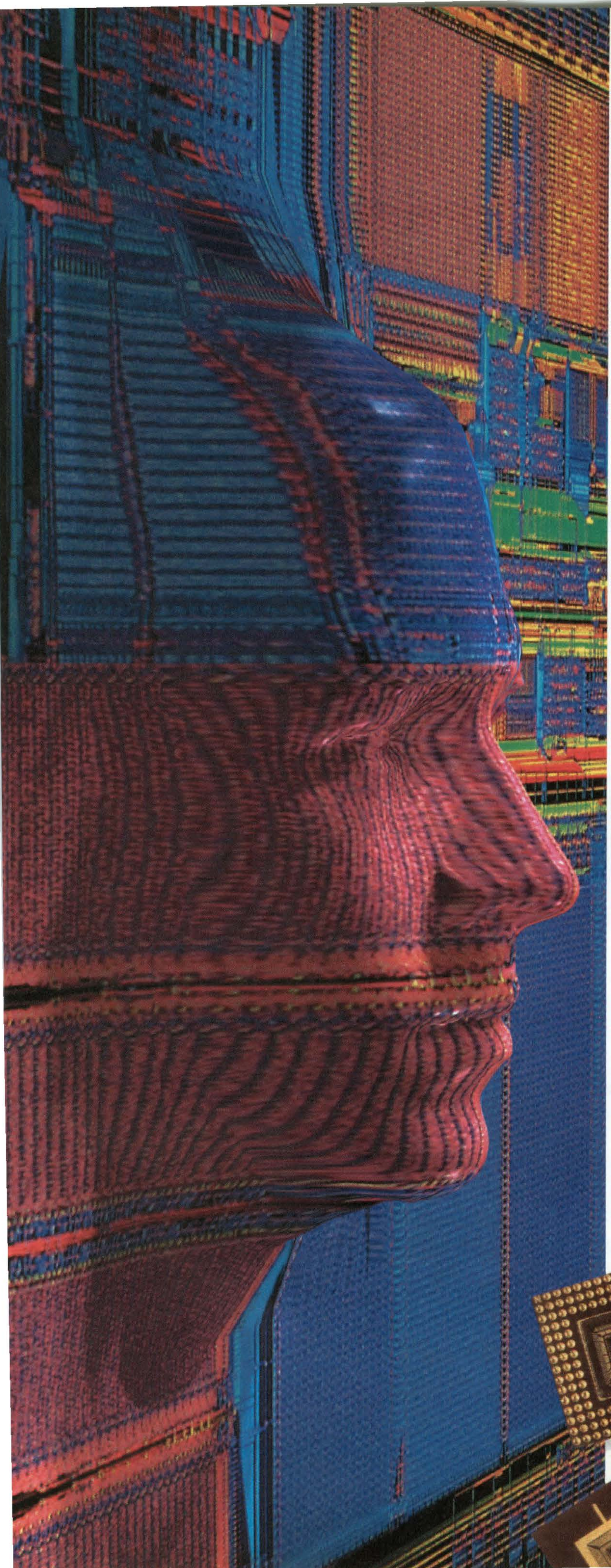

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Energy gauges add intelligence to rechargeable batteries

Malcolm McClure, Span Inc

An energy gauge built into a rechargeable battery pack can tell you exactly how much charge remains available for use. It can also direct an inexpensive "dumb" charging device to charge the pack in an optimal manner. It can even store a history of battery health.

It's too bad laptop computers, camcorders, and cellular phones can't run for 20 hours on a battery the size, shape, and value of a quarter. But they can't, so manufacturers offer ICs and other components to simplify the job of efficient power management. Such products include dc/dc converters, battery-charging devices, and power-switch arrays that control energy-consuming components like disk drives and backlit screens.

But perhaps the most dramatic advance in power management is in battery-energy gauges. These units, which often reside inside a battery pack, actually monitor the amount of energy that flows into and out of a battery to make accurate estimates of the amount of charge remaining. These estimates are available not only to the user, via an on-pack display, but also to the battery-run device, via some sort of serial data link. To a designer, this data is valuable information because the battery pack is often a device's largest, heaviest, and most expensive component.

Voltage readings aren't enough

Most rechargeable batteries for portable electronic devices are nickel-cadmium (NiCd) or, more recently, nickel-metal hydride (NiMH). These batteries' chemistries allow fast recharging and offer a good combination of energy density, uncharged shelf life, and low cost. Unfortunately, a simple reading of terminal voltage, either open circuit or under load, yields little information about their present state of charge. To understand why, look at the discharge curve for a NiCd battery (**Fig 1**). (NiMH batteries, by the way, behave in almost the same way during discharge.)

As **Fig 1** shows, terminal voltage drops rapidly for a brief time and then is followed by a long period of slow decline. As the battery nears depletion, the voltage again falls off quickly. At first glance, it would appear a simple matter to translate the terminal voltage, especially in the central region of the graph, into a measure of remaining charge. Indeed, some manufacturers have marketed crude energy gauges that use this approach. The results are woefully unreliable, however, because the absolute cell voltages are a function of temperature, internal pressure, and battery age. The amount of deviation caused by these factors negates any meaningful information derived from voltage alone.

The situation during charging is similar, as indicated in **Fig 2**'s typical charge curves for NiCd and NiMH cells. As in discharging, these two chemistries behave in an almost identical manner, an exception being that the NiMH batteries do not experience as much decline in voltage as they go into overcharge. Here, too, terminal voltage does not give a reliable measure of the state of charge, because the absolute values of the voltages vary with factors such as temperature and pressure.

The only accurate way to know how much charge is actually in a battery pack is to count the coulombs as they come and go. While this appears a conceptually easy task, a number of subtleties arise that quickly make it a formidable one.

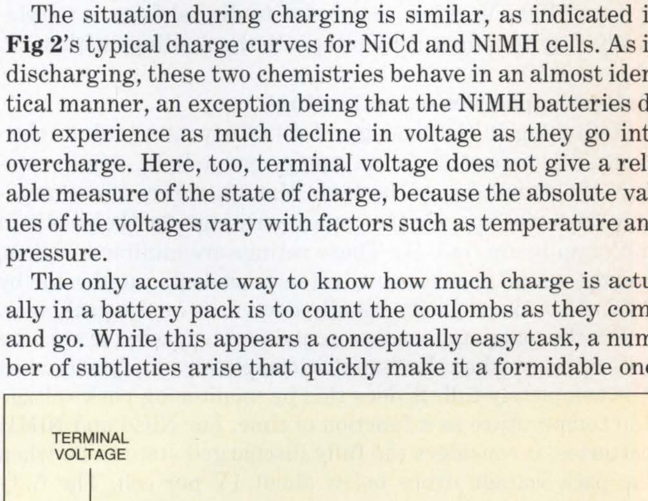

Fig 1—The absolute level of a battery's discharge curve depends on several variables, including temperature and pressure. The curve shown here is typical of NiCd batteries.

Nonetheless, highly accurate gauges are now available that take these subtleties into account.

A simplistic way of viewing a rechargeable battery is as a tank of electrons. As the charge depletes, the tank drains. As it recharges, the tank fills. To know how full the tank is, you need to count the electrons as they go into the empty tank. If the size of the tank is also known, you can make an estimate of "percent full."

Electrical current is a measure of electron flow, where $1A=1.6\times10^{19}$ electrons/sec. To count electrons, the energy gauge must monitor battery current and then numerically integrate it over time. This process requires three elements of hardware to implement: a current-sensing device, an A/D converter, and a processor to perform the integration and send the results to the host.

For monitoring really large currents, a Hall sensor can measure the magnetic field surrounding the current path and translate it into a current reading. But Hall devices require cumbersome magnetic cores and support electronics, and they're not cost-effective for most applications.

By far, the least expensive and most common approach for current sensing is to insert a low-value resistor in series with the current path and measure the voltage drop across it. Since any resistance inserted in the main current path potentially wastes power and may even limit the amount of current that can flow under surge conditions, the minimum possible resistance is preferable. Typical values range from 0.01 to 0.5Ω.

An A/D converter measures the voltage across the current-sensing resistor. To resolve currents of 1 mA over a range of ±4A, converter resolution of 13 bits is necessary. The signals involved may be minuscule, typically on the order of 100 μV. After conversion to digital form, it is relatively easy to numerically integrate the readings with a μP.

Battery capacities exceed ratings

Returning to the analogy of a battery as a tank of electrons, it is important for an energy gauge to be able to measure the actual size of the tank. Manufacturers of rechargeable batteries specify the capacity ratings for their cells in milliamp-hours (mA-H). These ratings are minimum values, and the actual pack capacity often exceeds its rated value by 20%. Also, the capacity usually decreases as the pack ages.

For the gauge to measure actual pack capacity, it must be able to sense when the "tank" is completely empty and when it is completely full. It does this by monitoring pack voltage and temperature as a function of time. For NiCd and NiMH batteries, it considers the fully discharged state to be when the pack voltage drops below about 1V per cell. The fully charged state can be characterized in several ways.

An approach that battery manufacturers recommend for determining the fully charged state of NiCd cells is called negative-delta-V detection. This approach requires sensing when the terminal voltage just starts to drop from its peak (**Fig 2**). While this technique also works with NiMH cells if the voltage resolution is sufficiently high, many cell manufacturers recommend dT/dt detection for NiMH. The dT/dt approach considers full charge to be when the pack temperature starts rising faster than some specified threshold.

Adding these capabilities for determining the fully charged state requires additional channels of A/D conversion or, perhaps, extending the resolution of the existing channels. For instance, to resolve voltage changes of 1 mV out of a battery voltage of, say, 20V (as is necessary for using negative delta V with NiMH batteries) requires an A/D resolution of 15 bits. By contrast, temperature sensing requires only about 9 bits of resolution. As it turns out, both temperature and voltage readings are necessary for proper gauging.

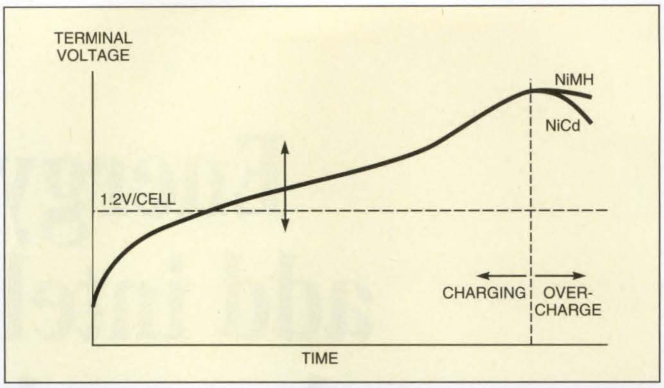

Fig 2—Charge curves, like discharge curves, depend on variables like temperature and pressure. NiCd and NiMH batteries charge almost identically except when they go into overcharge.

Energy gauges' advantages

Once an energy gauge has the ability to sense when a battery is fully charged and fully depleted, it can perform several other important functions. First, the gauge can automatically calibrate itself to the pack by measuring the actual amount of energy that can be extracted from the pack. In some gauging devices, the host must initiate this calibration; in others, calibration happens automatically whenever the pack runs from a fully charged state to a fully discharged one. With internal registers, a gauge can store capacity information for use in calculating present charge state as a percentage of capacity. A gauge can also monitor pack capacity over time as a barometer of battery health.

Once a battery gauge has the features just described, it has all the intelligence necessary for charging the battery pack. This intelligence need not be duplicated in external charging devices as long as some means exists for the pack to control an external "dumb" charger. The gauge can bring this control information out on a single hardware line or transmit it as part of a data stream.

Because determining actual pack capacity can take several hours, it would be unfortunate if this information got lost. This is a very real possibility, however, because the user can inadvertently let the pack discharge below the level necessary to keep the energy gauge working. Or, a static discharge could corrupt an internal register. For these reasons, some vendors have incorporated electrically erasable PROM (EEPROM) into their gauges for storing critical parameters. The addition of nonvolatile memory also lets the vendor offer a single standard product with a menu of features that the user can select through appropriate programming of EEPROM registers. For example, the menu might offer a range of charge-termination techniques, including negative delta V and dT/dt, with all the parameters selectable by the user.

Addition of EEPROM also allows the gauge to track battery history. This history might include basic information, such as how many charge cycles the pack has experienced, or

more exotic things, like the maximum and minimum temperatures experienced by the cells. Such information is useful in projecting a pack's life expectancy and even for deciding whether to honor a warranty on a supposedly defective unit.

Using the measured information

Now that the energy gauge has amassed all this information about the battery, what happens to that information? The most fundamental piece of information, the percentage of full charge, is often directly available on an LED or LCD. LEDs draw significantly more current than LCDs, so they're usually accompanied by a pushbutton switch for momentary activation. LCDs, on the other hand, can run continuously, but they're more delicate (removable battery packs are highly susceptible to being dropped), and they don't behave well at temperature extremes. For these reasons, LEDs are currently the display of choice.

Battery information is also usually available to the host equipment via some form of serial link. Various protocols are available, ranging from custom versions to standard RS-232C. The amount of information provided also varies among manufacturers. Along with percentage of full charge, it may include instantaneous readings of voltage, current, temperature, pack capacity, charger-control information, multiple levels of low-battery warning, and indications of any potential battery-error conditions.

Because most energy gauges reside inside a battery pack and draw their operating power from the battery, they must use as little power as possible, especially when the pack is not in use. Good gauges, therefore, enter a low-power mode when they sense their host is turned off. Quiescent currents of 50 μA are typical.

Operating voltage is also worth considering. Some energy gauges require a 5V source for their supply, which can require tapping into the battery string for 1.2V/cell NiCd and NiMH batteries. With packs of four or fewer cells, these gauges become unusable. Other gauges, however, can handle supply variations ranging from 3V or less to more than 25V.

You also have to consider the ways in which rechargeable batteries differ from the simple model of an electron storage tank. For example, all batteries, rechargeable or otherwise, exhibit the phenomenon of self-discharge. That is, a fully charged cell loses charge over time. The phenomenon is particularly noticeable with NiCd and NiMH cells, which typically lose about 1 to 2% of their charge each day. After three months of sitting idle, a previously fully charged pack will be dead. Worse yet, the self-discharge rate is a strong function of temperature. Storing the pack at 40°C instead of 25°C will cause it to fully discharge in just a few days.

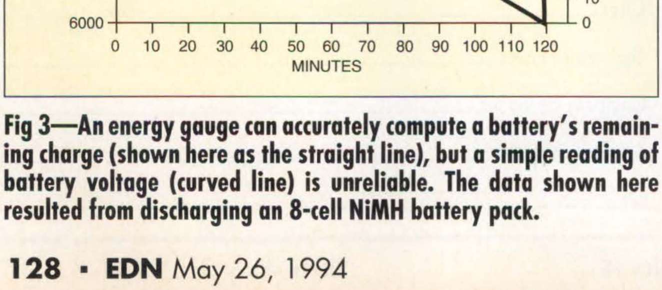

Fig 3—An energy gauge can accurately compute a battery's remaining charge (shown here as the straight line), but a simple reading of battery voltage (curved line) is unreliable. The data shown here resulted from discharging an 8-cell NiMH battery pack.

Because equipment used outdoors or left in the trunk of a car can experience high temperatures, energy gauges must monitor battery temperature and use it to account for self-discharge. However, the rate of self-discharge as a function of temperature varies with cell chemistry and manufacturing techniques. If an energy gauge has onboard EEPROM, an OEM can program the appropriate self-discharge parameters; other gauges must either approximate self-discharge with a "one-size-fits-all" algorithm or ignore it altogether.

Other factors that affect gauge accuracy include various charge and discharge efficiencies. For instance, charging efficiency is always less than 100% and drops off considerably as a pack nears full charge, because much of the energy pumped into the pack goes toward producing gasses rather than into a retrievable form. Likewise, temperature affects charge efficiency. All these parameters vary with chemistry and manufacturing techniques, but they can be accounted for if a gauge has the means to do so.

For an idea of the accuracy you can expect from an energy gauge, see the data in **Fig 3**. The plot shows pack voltage and percentage of remaining charge while a battery discharges at a constant rate of 1000 mA. This data, representing the fifth discharge cycle after calibrating a gauge to a battery pack, yields an overall accuracy of 0.22%. Under less ideal conditions, accuracies of 1 to 2% are typical.

The benefits of incorporating an energy gauge into a product line are several. First and foremost, both the user and the host equipment can know exactly how much charge is available from a battery pack. This is true whether the pack is currently in use or has been pulled from storage. A second benefit is that the extra battery capacity above rated value is available for use. In addition, an energy gauge eliminates the need for sophisticated charging equipment; it can control an external "dumb" charger at the cost of one extra terminal on the battery pack. Further, one charger can recharge various types of batteries.

The cost of adding an energy gauge to a product depends on several factors: sophistication and resolution of the hardware, desired current range, size and shape of the gauge, number of interface contacts with the host, communication protocol (if any), and type of display used. With all these variables, it is difficult to give specific price information. However, a typical energy gauge now adds about 25% to the cost of a pack, although prices are likely to drop rapidly over the next few years. Be aware, though, that some units come as fully assembled modules, while others are single ICs that require additional circuitry. EDN

Author's biography

Malcolm McClure is Director of Battery Servicing Products at Span Inc in Indianapolis, IN. He has BSEE and MSEE degrees, both from Northwestern University.

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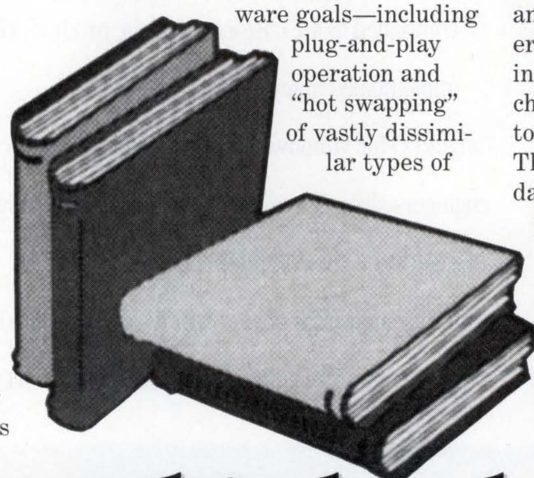

If you're planning to buy, use, or design products compatible with the standards of the Personal Computer Memory Card International Association (PCMCIA), you need a copy of *The PCMCIA Developer's Guide* by Michael T Mori. This self-published book (Tori is an independent design consultant) is by far the best collection of useful information I've seen on PCMCIA—a valuable blend of tutorial information, product information, and design guidelines. Moreover, Mori has obviously taken great care in choosing what *not* to include in the book, so you can plunge right in and learn quickly, without getting bogged down in details for which you're not yet ready.

The book begins by briefly summarizing the evolution of the association and the PCMCIA standard. Then, in 10 pages or so, it gives a remarkably clear overview of today's expanded standard. The standard itself isn't hard to read, but this summary quickly gives you a good perspective.

The real meat of the book begins in Chapter 3, "Designing a PCMCIA host adapter." A host adapter, in this sense, is simply something that connects to a host computer and accepts PCMCIA cards. It can be part of the equipment you're designing, or it can be an external unit. This chapter doesn't have every design detail you need, but it explains the major design issues, and it provides enough information at the block-diagram level to give you a sense of what you're up against.

Chapter 3's tutorial information is all the better for having just the right amount of basic information about some of the more popular PCMCIA ICs available for designers. (Later, in Chapter 8, there's more detail about a wider range of chips.) Most of the ICs this chapter discusses are socket-controller ICs, which provide the needed connections and signals between a PC bus and one or more PCMCIA card sockets. (PCMCIA applications aren't limited to the PC architecture, but commercially available socket controllers are. You can design PCMCIA interfaces for other buses, but you have to do a lot more of the work yourself.)

The next chapter, "Designing a PC card peripheral," looks at the myriad issues of designing a plug-in PCMCIA card. In about 35 pages, it covers electronic design, mechanical design, software and compatibility issues, and agency approvals. Most of this information deals with electronic-design issues that are specific to memory cards and to what PCMCIA calls "I/O cards," which can contain practically any kind of peripheral device. You need to read the entire PCMCIA spec before you actually undertake a design, but this chapter boosts you up the learning curve.

Chapter 5, "PCMCIA software requirements," takes on what is undoubtedly the most confusing and troublesome aspect of using or designing PCMCIA products. PCMCIA has not reached all of its ambitious software goals—including plug-and-play operation and "hot swapping" of vastly dissimilar types of cards—despite the existence of some very sophisticated and complex system software. This chapter explains, as well as 20 pages of text *can* explain, the software issues and which products are available to deal with them.

The chapter does an adequate job of describing succinctly what PCMCIA system software does and, in some cases, what it doesn't do. For example, a PCMCIA system-software module called Card Services (available from several software vendors) is not yet sufficiently general to control every type of card that you can possibly insert in a PCMCIA slot. To get around the problem, card vendors provide specific card "enablers," essentially device drivers that defeat PCMCIA's hot swapping and plug-and-play goals. The issue of specific-vs-generic enablers is one that anyone involved with PCMCIA is going to have to address—a lot.

The future of PCMCIA gets a short chapter of its own in the book. The chapter's main topics are the recent and planned additions and modifications to the PCMCIA standard: additional operating voltages (more than just 5 and 3.3V), the 32-bit CardBus (which is patterned after the PCI-local bus and allows bus mastering), power management, multifunction cards, and more.

Next, the book provides an 80-pg product-information guide. A short chapter summarizes the types of PCMCIA products that are available, and a much longer chapter details several products. The product categories include all types of PCMCIA cards, chips, system software, development tools, and interconnection hardware. This information will soon be out of date, but it appears remarkably complete for now. The book's publisher expects to create revised and updated editions periodically, with the first one coming fairly soon.

Finally, appendixes to the book contain almost 200 pgs of reference information, mostly from the PCMCIA specification. Having all this information in one book is handy, and the resulting single volume isn't all that bulky. It contains 400 or so 8.5×11-in. pages in all—about the size of a 1-in.-thick notebook.

The PCMCIA Developer's Guide isn't the only source of information you need to design PCMCIA products, but it's a good starting point. It assembles a lot of useful information, and that information is clear, concise, and probably the most relevant of all the information you need to get a quick start with PCMCIA design.

The book isn't cheap; it costs $89.95 plus shipping. But if you need to learn about PCMCIA and you value your time, you'll get your money's worth and more.—**Gary Legg**

Sycard Technology, Sunnyvale, CA. (408) 247-0730. **Circle No. 422**

Verify DSP-filter designs with SystemView

When performing DSP designs, you must weigh the tradeoffs of FIR vs IIR filters before committing to hardware. FIR filters lack a feedback path, thus ensuring inherent stability. FIR filters also provide an exactly linear phase response, so phase distortion does not occur. However, FIR filters typically require more computational time, especially in hardware that has only a single multiplier. A fast FIR requires a prohibitive number of multipliers to perform multiplications in parallel.

These drawbacks could also be a problem in DSP applications in which software performs the operations sequentially. The more instruction cycles needed to implement a filter, the fewer clock cycles you have for other processing tasks.

Using Elanix's SystemView ($985), a dynamic system-level simulator, you can quickly address these problems and verify the merits of both types of filters. This graphical system simulator runs on PCs under Windows and lets you specify all relevant information and display the results simultaneously side-by-side.

The application I decided to simulate uses a lowpass filter having a 1-kHz cutoff frequency to operate with a sampling rate of 8 kHz. The first step in setting up the simulation was to select a sweep generator from the sources that the software offers. I configured the sweep generator to run from 10 Hz to 4 kHz. You select the sweep generator from a menu of source signals and specify its parameters by filling in a form. The sweep generator mirrors the actual method of evaluating the performance of the filter. An alternative source could have been the impulse, or "delta," function.

The next step was to quantize the input to 16 bits. I selected the quantizer from the appropriate function-token library and filled in its parameters. I then connected a signal-display token to the output of the quantizer. You can attach a display token anywhere in the simulation to aid diagnosis or to view intermediate results.

The next step in the simulation was designing the filters. I selected "linear system" from the operator-token library and then chose the types of filters from among FIR, IIR, and Laplace-transform filters. I then filled in another form for each filter with its critical frequencies, the amount of gain in the passband and the stopband, and the number of coefficients to use. The software can estimate the number of taps needed to meet the specifications in the FIR menu. You can select fewer taps than the software suggests, but doing so may mean the filter will not meet your specifications.

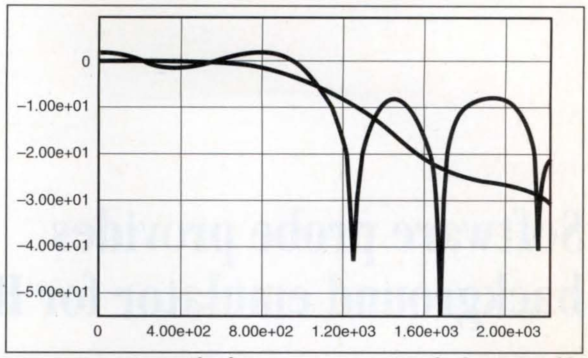

Fig 1—Comparing the frequency response of a basic FIR filter and the Hanning-windowed version shows that the windowed filter offers a vast improvement in ripple over the FIR filter. However, there is a penalty: The windowed filter does not roll off as sharply as the FIR filter does.

I examined four filter types: an 18-tap, lowpass FIR filter, a Butterworth IIR filter, a Bessel IIR filter, and a Chebychev IIR filter. All my IIR filters had eight poles, giving the same number of multiply-accumulate operations.

An important consideration when selecting a filter is the effect of quantizing the filter's coefficients to a specified number of bits. With this software, I simply entered the appropriate values in the text boxes. In this case, I set the coefficient quantization to 16 bits. The simulation showed that quantization has its biggest effect on the Chebychev filter's performance and a smaller effect on the FIR filter's.

After I specified all four filters, I started the simulation. The simulation injected the output from the quantized-frequency sweep signal into each of the filters and placed a display token at the output of each filter.

Once the simulation finishes, you can use the program's analysis window to examine—simultaneously or separately—the output response of each filter. You can view the signals in the time domain or the frequency domain, and you can view the frequency-domain data along a log or a linear axis.

The Butterworth and Bessel filters turned out to have a smooth inband response, but their frequency rolloff was slow. The FIR and Chebychev filters had a much steeper cutoff but had a significant passband-amplitude ripple. For the FIR filter, this ripple arises from the small number of taps. The application specified a 0.1-dB ripple, but the optimization routine could satisfy this constraint only by averaging and by using 18 taps. The 16-bit word size also raised the out-of-band ripple of the FIR filter. The Chebychev filter's ripple comes from the 16-bit finite-word size of the filter-tap coefficients.

Another design feature you can apply to the FIR filter is "windowing." Windowing multiplies the given impulse response, h(t), with a window function, w(t), to produce a new filter response g(t)=w(t)h(t). We usually think of windows as a means of reducing the spectral side lobes of Fourier transforms. In this context, multiplying by the window in the time domain convolves the frequency response of the window with the frequency response of the original filter. The lowpass nature of the window's response smooths the original response.

Fig 1 compares a Hanning-windowed filter and the original FIR filter. The windowed filter offers a vast improvement in ripple over the FIR filter, but the windowed filter does not roll off as sharply as the FIR filter does.

I chose the windowed FIR filter for this application because of its good cutoff, low out-of-band response, and low in-band ripple. The FIR filter is also inherently stable and has no phase distortion. The actual frequency response of the filter, when implemented in an Analog Devices AD-2101 EZ-Lab DSP evaluation board, exactly matches the SystemView simulation.

—Roger Hack

Elanix Inc, Westlake Village, CA. (818) 597-1414. **Circle No. 423**

Professor Roger Hack is a member of the Electrical Engineering Technology department at Purdue University (Fort Wayne, IN).

Software probe provides background emulator for HP tools

The HP3490A software probe provides a Motorola background-debug mode (BDM) interface to Hewlett-Packard's software-development tools. It provides run-control, memory-inspection/modification, and code-downloading functions over a network.

The front panel of the instrument connects to a target's BDM port. The front panel also has two BNCs that connect to a logic analyzer. The logic analyzer can use a trigger-out signal as a qualifier to start an event, such as tracing. A trigger-in BNC allows the logic analyzer to force a breakpoint.

An interface for Unix or Microsoft Windows provides the same interface between the development tools and the software probe that exists for the HP 64700 series of emulators. The software probe supports 10Base2 and 10BaseT connections.

The HP3490A software probe costs $3995. The interfaces for Unix and Windows cost $3585 and $1750, respectively.—**David Shear**

Hewlett-Packard Co, Palo Alto, CA. (800) 452-4844, ext 8322.

Circle No. 369

Automatically move from a Matlab simulation to an embedded system

Those using The MathWorks' Matlab and Simulink to simulate and analyze systems can now let their computers create the C code to implement models on targets running the VxWorks real-time operating system (RTOS). You can model the operation of the system you are developing by interconnecting block-level diagrams or by using the Matlab language.

You can rapidly prototype a design by letting the C-code generator produce C code, compile it, and run it on your target. Simulink's graphical user interface allows you to select and connect function blocks. It can generate continuous, discrete-time, or hybrid runtime code. Once the system simulation meets your satisfaction, you can move appropriate portions of the system to your target.

For example, you might also simulate real-world inputs when simulating a system. When you move the design to the target, the real world provides the real-world inputs, and you do not need code for these functions. Once you generate the code, you can insert it back into your simulation to test it before letting it loose on the target.

You can use the C-code generator with VxWorks, and you can interface other RTOSs to the tool by modifying a file that defines the RTOS service calls the code generator uses. The C-code generator also includes documentation, source code, make files, and examples for creating RTOS support.

The Control Framework API automatically builds programs based on customizable make files. These make files define compiler options, source files, libraries, and automatic download options.

The C-code generator requires Matlab (starting at $1695) and Simulink (starting at $1995). The C-code generator costs $9995 for either the PC or the workstation version.

—**David Shear**

The MathWorks Inc, Natick, MA. (508) 653-1415.

Circle No. 370

PowerPC simulator lets you test your system without the system

The PowerPC Virtual System from IBM allows you to simulate not only the code running on a μP, but also the ASICs and other system components. The Virtual System is built around the PowerPC Visual Simulator (PVS). This simulator provides a simulated debug environment that allows you to test code, optimize system-design considerations, such as cache size and memory-access times, and interact with simulated I/O from a graphical user interface.

With Virtual System, you can model the complete I/O subsystems or just selected functions. A C-based application-programming interface (API) is a set of C-language functions that an I/O model can use to interact with the simulated PowerPC.

The PVS bus-model API can also connect the PVS to a simulation of your I/O. In this case, the bus-model interacts with the ASIC-simulation environment. This interaction lets you use actual ASIC models to provide the I/O simulation to the PowerPC.

The VHDL model for the bus of the PowerPC603 is now available free. Other models will become available in the future. As you debug your software, you can see how it reacts to a simulation based on the actual data used to create the ASIC. You don't have to worry about creating a new model to work with the simulator.

By simulating not only the μP and the other subsystems, but also the actual VHDL-design data, you can check out more of the system before committing to hardware. Catching errors early in the game is a key factor in reducing development time. The PVS runs on IBM RISC System/6000 workstations and costs $6000.

—**David Shear**

IBM Corp, Rochester, MN. (507) 253-7291, ext 330.

Circle No. 371

68300 68HC16

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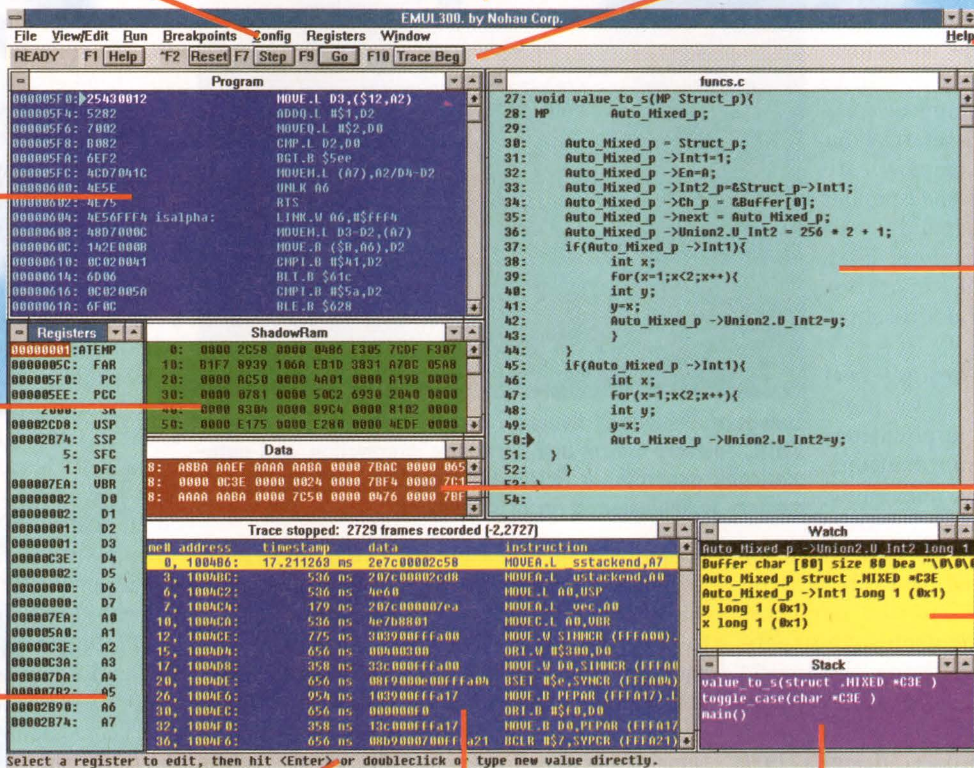

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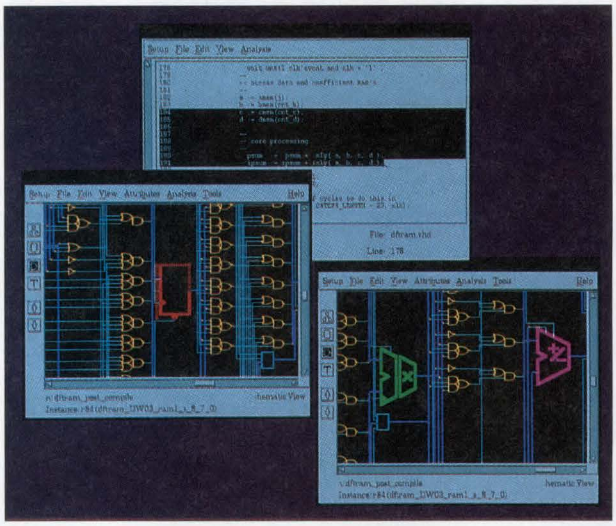
CIRCLE NO. 83

Synthesize logic from behavioral description



Synopsys' Behavioral Compiler accepts behavioral Verilog or VHDL, extracts control and data-flow information, and automatically generates a finite-state machine, data-path, and memory to implement a circuit's behavior.

The Behavioral Compiler from Synopsys provides the next step in design automation, offering potentially large improvements in designer productivity. Specifying an IC at the behavioral level requires only one-fifth to one-tenth as much time as specifying at the register-transfer level (RTL), the company estimates. In addition, the compiler lets you routinely simulate your design at the behavioral level, saving significant simulation time over structural-level simulation.

The tool suits designs that are best described by algorithms. Typical applications include telecommunications, high-end graphics, and multimedia. The tool frees you from designing the cycle-by-cycle behavior of a design. Instead, you can focus on algorithms while the tool performs multicycle optimization using techniques such as pipelining, multicycle operation, chaining, and resource sharing.

Many algorithm-based designs start as a C or a C++ language specification. Instead of translating the code into an RTL specification, you can write a behavioral specification in VHDL or Verilog that is very similar to the original language specification. According to the company, the behavioral specification may be only one-tenth as long as the RTL specification for the same design. Furthermore, the close relationship between behavioral-level hardware-description languages (HDLs) and software facilitates software/hardware system design.

The tool goes beyond the typical behavioral-level data-path designs available with other tools to include controller and memory inferencing. The tool automatically infers a design's controller from the behavioral specification and integrates it with the data-path portion of the design. The Behavioral Compiler also infers memory reads and writes from HDL-array accesses, allowing it to schedule memory access automatically. You no longer need to perform memory timing and scheduling manually.

Because the behavioral description does not imply an architecture, the synthesized architecture varies, depending on a few easily varied high-level constraints. This technique makes design reuse much more efficient than it is with RTL design.

Behavioral Compiler relies on and offers tight integration with the company's other architectural and logic-synthesis tools. It costs $69,500 and is in Beta test. The company plans to begin shipments in the fourth quarter. **—Doug Conner**

Synopsys, Mountain View, CA. (415) 962-5000. **Circle No. 340**

Painlessly improve IC-test fault coverage

I_{DDQ} testing measures quiescent current while running selected functional vectors to identify defects. I_{DDQ} testing of ICs is off to a great start for two reasons. First, 60 to 80% of the faults in silicon are bridging and transistor problems detectable by using I_{DDQ} testing. Second, I_{DDQ} doesn't require the use of a special design for testability techniques. Because I_{DDQ} testing works on all logic types, your design can be synchronous or asynchronous.

Typically, all you need are 15 to 20 well-chosen test vectors for a 100,000-gate design to obtain high fault coverage with I_{DDQ} testing. Before we paint too-rosy a picture, however, note that I_{DDQ} testing does not actually determine whether a chip is functioning properly: You still need some level of functional testing. But you can use I_{DDQ} testing with other techniques to increase fault coverage.

Moving I_{DDQ} testing one step higher is Current Synthesis from CrossCheck. Although you don't need to use design-for-testability techniques to use I_{DDQ}, the Current Synthesis tool can make I_{DDQ} testing more effective for a small increase (3 to 5%) in silicon area. The tool creates synthesized test structures that improve testability and eliminate current-draining conditions that may exist in a design, reducing the device's power consumption during normal operation.

Many of the same current-drain concerns important to designers of battery-powered circuits are also concerns in I_{DDQ} testing. So, the tool improves a design's testability while reducing power consumption. The tool offers such changes as eliminating bus contentions and floating buses by synthesizing structures, such as control gates and bus keepers.

CrossCheck plans to ship Current Synthesis in the third quarter; prices start at $15,000. The product is an option to CurrenTest ($45,000), a currently available tool that develops the I_{DDQ} test vector. **—Doug Conner**

CrossCheck Technology Inc, San Jose, CA. (408) 432-9200. **Circle No. 341**

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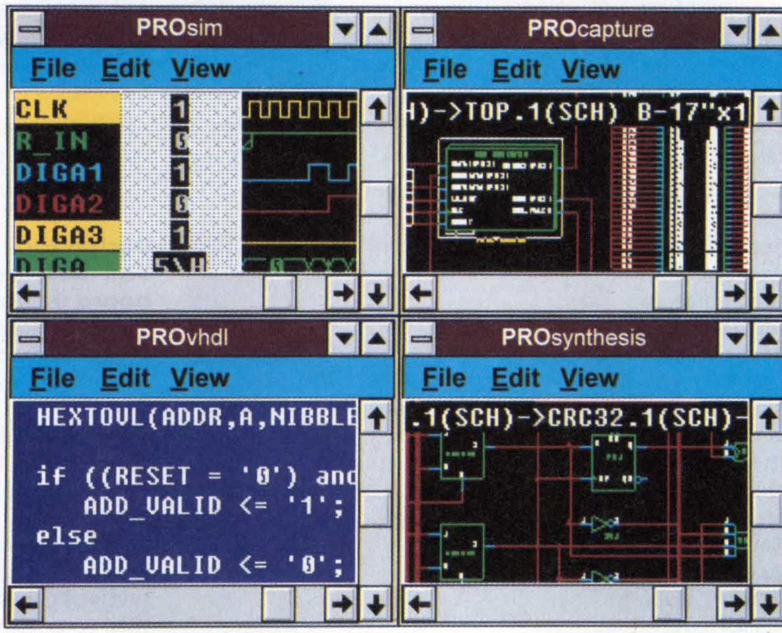

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CIRCLE NO. 115

ELECTRONIC DESIGN AUTOMATION

Logic emulator combines fast compiling with low cost

The Pegasus logic-emulation system from Arkos Designs takes a different approach from logic-emulation systems based on Xilinx field-programmable gate arrays (FPGAs). The emulator uses a massive array of custom logic processors designed specifically for emulation. Each logic-processor chip contains 32 logic-processing units. A fully configured system for emulating 200,000-gate designs uses 512 of the processing chips on eight pc boards for a total of 16,000 processing units. Depending on the size of the design, the processors perform four to 16 sequential operations, reducing the 50-MHz speed of the processing units to a 3- to 12-MHz system-emulation speed.

According to the manufacturer, the emulator has ample routing resources, and compiling a 200,000-gate design takes less than 30 minutes. Instead of solving complex FPGA-routing problems, the system loads the functions into the processing units and assigns routing connections. Because the compiling speed is much higher than those of competitive systems, the emulator lets you find design problems interactively—something you can't do with long recompile times.

Each logic processor includes a 32,000-vector embedded logic analyzer, providing access to every node in an emulated design, as well as on-chip RAM. In addition, each Pegasus board provides 4 Mbits of high-speed RAM for emulating RAM, ROM, FIFO buffers, or multiport RAM.

Pegasus requires a 486 PC or a Sun workstation for operation. Prices for a 25,000-gate version start at $36,000, and a 200,000-gate version costs $115,000. The price includes all hardware, software, and logic-emulation boards. The company will begin shipping the systems in October.

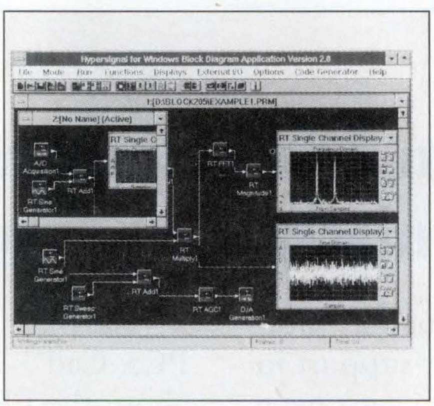
—Doug Conner

Arkos Designs Inc, Scotts Valley, CA. (408) 461-8100. **Circle No. 342**

Verify design equivalence without simulation. The Design Verifyer tool verifies the functional equivalence of gate- or register-transfer-level (RTL) descriptions. The tool compares RTL to RTL, RTL to gates, or gates to gates. Typical applications include verifying RTL descriptions that have changed to improve synthesis results, testing gate-level implementations against RTL descriptions, and testing gate-level descriptions modified to alter timing or for scan insertion. Because the tool accepts VHDL and Verilog RTL descriptions, it lets you check the equivalence of VHDL and Verilog models. $65,000. **Chrysalis**, Andover, MA. (508) 475-7700. **Circle No. 343**

VHDL simulator for Unix systems costs <$1000. The $995 entry-level VHDL simulator runs on Sun and HP workstations. The compiled simulator includes an interactive source-level debugger. The software targets self-paced VHDL training and behavioral-model development. **Compass Design Automation**, San Jose, CA. (408) 433-4880. **Circle No. 344**

Complex-function library speeds ASIC design. The MacroWare 2.1 library of 40 royalty-free complex functions comes in gate-level structural VHDL, gate-level Verilog, and EDIF 200 formats. Functions include the M8051 embedded microcontroller, M765A floppy-disk controller, M91C360 data separator, M16C450 UART, M85C30 serial communications controller, M8042 slave peripheral controller, and 82xx peripheral-interface products. The macros include test vectors providing 98% min fault coverage. A single-node library license costs $48,000. **3Soft Corp**, Santa Clara, CA. (408) 982-9017. **Circle No. 345**



DSP block-diagram simulator offers real-time simulation. The Hypersignal for Windows Block Diagram simulation software lets you run DSP algorithms designed with the tool on DSP boards. The software combines graphical programming with real-time algorithm-performance evaluation, speeding design development. The price for the software with real-time support ranges from $1495 to $7995. **Hyperception**, Dallas, TX. (214) 343-8525. **Circle No. 346**

Design tool improves communication between schematic and pc-board designers. The Placement and Critical Route (PCR) 386+ tool lets you optimize placement and packaging of pc-board components before layout. The tool lets you move easily between schematic and physical-board form, letting you communicate critical information to the person who lays out the pc-board. You can also review pc-board-layout data from the board designer. The software lets you reuse sections of board designs as modules, so that you can pass them directly to the layout person. The introductory price for PCR 386+ is $995. **OrCAD**, Beaverton, OR. (503) 671-9500. **Circle No. 347**

Software simulates EMC emissions before you build the product. The Compliance electromagnetic-compatibility (EMC) simulator calculates radiated fields due to systems of printed-circuit boards and common-mode currents on cables and enclosures. The tool is fully integrated into the company's other signal-integrity tools. **Quantic Laboratories Inc**, Winnipeg, MB, Canada. (204) 942-4000. **Circle No. 348**

ASIC-test tool integrates front-end hardware synthesis and back-end test generation. The ASICtest family of test-automation products includes three tools. Icrambist generates register-transfer-level (RTL) code for built-in self-test (BIST) of memories, including the BIST controller and any required memory interface logic. JTAGsyn generates the RTL code for

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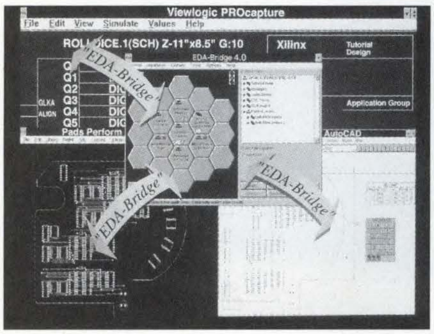
ELECTRONIC DESIGN AUTOMATION

an IEEE 1149.1-compliant module incorporating the test-access port (TAP), the boundary-scan chain, all the I/O cells, and the call to the core module. ICscantest performs scan chain insertion, scan rule-checking, combinational test-pattern generation, and fault simulation. The tools begin at $25,000. **Logic Vision Software Inc**, San Jose, CA. (408) 453-0146.

Circle No. 349



Tool provides standard communication links for design data under Windows and Windows NT. Version 4.0 of EDA-Bridge provides BridgeSpeak integration technology that allows design tools from multiple vendors to interoperate under Windows and Windows NT. Prices start at $1495. **EDA CAD T E A M Ltd**, San Jose, CA. (408) 437-1313. **Circle No. 350**

Design kit simplifies timing analysis and verification of Pentium-based designs. The Pentium design-analysis kit works with Intel's Design Guide. The kit helps you perform timing analysis and verification on a wide range of Pentium-based designs. The tool provides timing verification across PCI, EISA, and Pentium host buses. $6000. **Quad Design**, Camarillo, CA. (805) 988-8250. **Circle No. 351**

Tool optimizes analog-circuit performance. The Paragon analog circuit optimizer lets you improve circuit performance at both the system (behavioral) and the component levels. For example, the software finds parameter values for an active filter design, satisfying center frequency, bandwidth, and gain. The tool iteratively and automatically changes design parameters to home in on an optimum solution. You can also use the tool while altering circuit parameters by interactively exploring circuits as the tool provides graphical feedback. Paragon will be available in July and costs $1900 on PCs and $3900 on Sun workstations. Also available is a suite of analog- and digital-simulation and programmable logic-synthesis tools that run under Windows 3.1 and NT. **MicroSim Corp**, Irvine, CA. (714) 770-3022. **Circle No. 352**

Electronic conferencing software speeds communication. The Electronic design-for-manufacture (DFM) conferencing software helps users of the company's DFM tools communicate effectively with work locations. The software lets you share real-time workstation-based DFM applications over Transfer Control Protocol/Internet Protocol (TCP/IP) networks using 9.6- to 19.2-kbps bandwidth lines. The program requires no additional hardware or software, and it supports 10 remote stations and one host in a single conference. The software will be available in the third quarter and costs $3500 for the host conferencing port and $4500 for each remote conferencing station. **AT&T Design Automation**, Holmdel, NJ. (800) 336-5256. **Circle No. 353**

Tool analyzes signal integrity and ground bounce. The Presto signal-integrity simulation software works with the Sprint simulator to analyze circuit boards. The simulator evaluates thousands of transmission lines and inductors in minutes, even when using complex models of pin-grid-array-package ground planes. The software runs on workstations; prices start at $45,000. **Anacad EES**, (408) 954-0600.

Circle No. 354

SHORTS

TangoPRO Version 2.2 for pc boards ($5950), Schematic ($995), and Route ($5,500) are available and run under Windows. **Accel Technologies Inc**, (619) 554-1000.

Circle No. 355

VHDL Editor ($2000) is a context-sensitive description-language editor that includes syntax error checking and a multivendor synthesis-subset-checking tool for VHDL. **Vantage Analysis Systems Inc**, (510) 659-0901. **Circle No. 356**

INTEGRATED CIRCUITS

Regulators supply high current with low dropout. Two families of pnp-based medium- and high-current low-dropout regulators feature maximum dropout voltages of 450 mV at room temperature, 300 mV typ. The company guarantees that all of the regulators operate with <600 mV dropout over worst-case temperature extremes. All are available in 3.3, 5, and 12V fixed- and adjustable-output versions. The MIC2920A/37A/40A ($1.14 to $1.65 for the 3.3V versions (100)) supply 450, 750, and 1200 mA, respectively; the MIC29150/300/500/750 ($1.93 to $8.33) supply 1.5, 3, 5, and 7.5A, respectively. Package options include the 3-pin TO-220 and the 5-pin TO-220 and TO-263. **Micrel Semiconductor**, San Jose, CA, (408) 944-0800. **Circle No. 372**

MPEG decoder handles system tasks. The ZR36100 provides video decoding and system operations for an MPEG I data stream for <$30. The device separates the video and audio signals in the MPEG bit stream, provides the audio data to an external decoder and synchronizes that audio with decoded video. The decoder handles data rates as great as 5 Mbps, suitable for SIF-resolution format images. A $1995 evaluation board is also available. **Zoran Corp**, Santa Clara, CA. (408) 986-1314, ext 356. **Circle No. 373**

Video decoder includes Digicipher II. The CL9100 RISC-based programmable video decoder handles four decompression algorithms: MPEG I, MPEG II main and simple profiles, and General Instruments' Digicipher II. The chip handles CCIR 601 resolution, provides video and audio synchronization, extracts user data from the bit stream, and supplies decoded video in YCrCb format. A companion device, the CL9110, demultiplexes the audio and video data streams. Each chip costs $35 in quantity. The CL9100 is available now, and the CL9110 will be available for sampling in the third quarter. **C-Cube Microsystems**, Milpitas, CA. (408) 994-8300. **Circle No. 374**

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100-nsec comparators have rail-to-rail inputs. The MAX941/942/944 comparators each consume <35 μA. The outputs pull within 0.4V of either supply rail without external pullup circuitry, and all I/O pins can withstand continuous short circuits to either rail. The comparators incorporate internal hysteresis, and the single 941 also includes a latch and a 12-μA shutdown feature. The devices come in 8- and 14-pin DIPs and SOICs; prices start at $1.40 (1000). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600. **Circle No. 375**

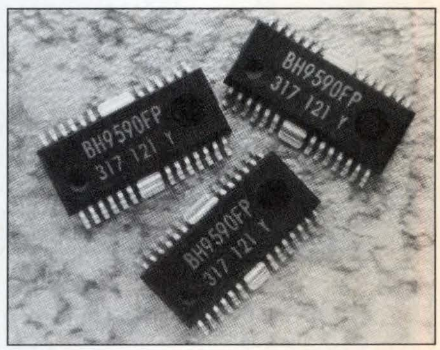
High-voltage driver has 64 channels. The HV57708 driver IC operates from 5V, provides output voltages up to 80V, and sources and sinks up to ±15 mA/channel. The cascadable, serial-to-parallel converter IC has four simultaneously clocked shift registers that allow for a 32-MHz equivalent data-throughput rate. Features include output blanking, latch enable, and polarity reversal. $5.18 (1000). **Supertex Inc**, Sunnyvale, CA. (408) 744-0100. **Circle No. 376**

Crosspoint switch targets video designs. The MT88V32 IC comprises 32 T switches in a digitally programmable, 8×4 nonblocking array. The IC features a 200-MHz bandwidth and a digital control interface with maximum setup and hold times of 150 nsec. Differential phase and gain errors are typically 0.05° and 0.11%, respectively. The IC interleaves analog signal lines with ground lines, which improves isolation and limits crosstalk. $11.54 (1000). **Mitel Semiconductor**, Kanata, ON, Canada. (613) 592- 2122. **Circle No. 377**

IC combines photodiode and amplifier. The OPT301 IC eliminates leakage current, noise pickup, and gain peaking due to stray capacitance. Key features include a 1-MΩ feedback resistor, 2-mV dark errors, a 0.47-A/W responsivity, a 4-kHz bandwidth, a 400-μA quiescent current, a 0.05% nonlinearity, and a ±2.25 to ±18V supply range. The device comes in a metal TO-99 with a glass window; prices start at $11.10 (100). **Burr-Brown Corp**, Tucson, AZ. (800) 548-6132. **Circle No. 378**

SCSI terminator lowers capacitance. The UC5613 9-line active terminator features a 3-pF channel capacitance. The IC meets all SCSI requirements and features a disconnect mode that reduces quiescent current to 10 nA. The IC features a 400-mA sink/source regulator, a low-dropout regulator of 0.7V, thermal shutdown, and current limiting. $2.18 (1000). **Unitrode Integrated Circuits**, Merrimack, NH. (603) 424-2410. **Circle No. 379**

PCI chip sets target all levels. The 82420 PCIset family provides a range of options for creating 486-based PCI local-bus PCs. The EX chip set for 486 CPUs packs dynamic RAM control, cache control, Integrated Device Electronics control, and power management into a 2-chip set for low cost ($25.20, 10,000). The 3-chip ZX chip set adds all standard ISA-bus signals and a data-path unit with write buffers. It also optimizes its interface for the DX4 processor ($38.50). **Intel Corp**, Folsom, CA. (800) 628-2283. **Circle No. 380**



SCSI terminator reduces power to 90% of passive components. The BH9590FP-Y dissipates 66 mW max when no signal is present. The IC actively terminates as many as 18 SCSI lines and meets all SCSI-I and -II standards. A programmable enable pin determines whether the IC is in a termination or a high-impedance-disconnect mode. Disconnect mode separates the SCSI lines from the terminator circuits. Line impedance is 100 to 130Ω under standard operating conditions. Capacitance is <10 pF. $1.80 (10,000). **Rohm Corp**, Antioch, TN. (615) 641-2020, ext 178. **Circle No. 381**

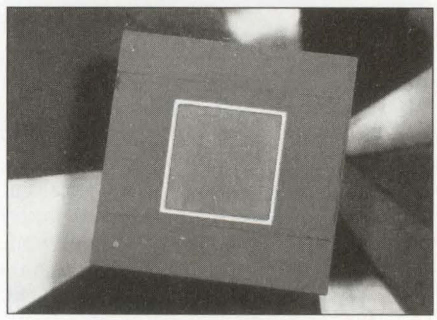
HDD read-channel IC fits small forms. The IMP62C540 read-channel IC runs at 5V and handles data rates to 40 Mbps. The IC includes a servo controller with serial addressing to reduce I/O pin count. The device comes in a 64-

pin TQFP and costs <$9 in large quantities. **International Microelectronic Products Inc**, San Jose, CA. (408) 432-9100. **Circle No. 382**

LED emits white light. The WhiteLED surface-mount LED with white-light emission offers blue, green, and red light sources on board. Simultaneously illuminating all three sources creates a white light. Illuminating the light sources separately or in pairs creates any color in the spectrum—from yellow to purple. $2 (10,000). **Siemens Components Optoelectronics Division**, Cupertino, CA. (408) 725-3508. **Circle No. 383**

Synchronous pipelined burst SRAMs for Pentium and Power PC μPs. The KM732V588 and KM732V592 static RAMs (SRAMs) are for the Pentium and PowerPC cache memories, respectively. The 1M-bit synchronous SRAMs have two stages of data and address pipelining. The units sample all data, address, and control inputs, and all outputs are valid at the positive-going system-edge clock. The SRAMs have a 32,768×32-bit organization and have internal data, address, and control latches. Price is $22 each for 66-, 60-, or 50-MHz versions. **Samsung Semiconductor Inc**, San Jose, CA. (408) 954-7000. **Circle No. 384**

CPLD runs at 143 MHz. The CYC371 version of the vendor's Flash370 complex programmable-logic devices (CPLDs) has 32 macrocells and an 8.5-nsec worst-case propagation delay. The flash CPLDs implement an advanced programmable interconnect matrix for routing signals between logic blocks. The devices also offer a product term matrix, which lets you individually route product terms to macrocells. The 143-MHz CY7C371 is available in 44-pin PLCC packages and costs $31.50 (100). **Cypress Semiconductor Corp**, San Jose, CA. (408) 943-2600. **Circle No. 385**



Decoder provides JPEG in single chip. The M65700 IC provides 30-frame/sec compression and decompression using the JPEG standard of images as large as 9640×480 pixels. It includes color-space conversion for the YUV, RGB, and CMYK spaces and handles raster-to-block data conversion. The device holds both default and programmable Huffman and quantization tables and provides an on-chip DMA controller for fast bus access. The sample price is $300. **Mitsubishi Electronics America Inc**, Sunnyvale, CA. (408) 730-5900, ext 2106. **Circle No. 386**

LCD controller handles video overlay. The Mustang family of LCD/flat-panel controllers provides a 256×18-color palette, a 24-bit DAC, and a video input port. The devices can simultaneously display on CRTs and monochrome

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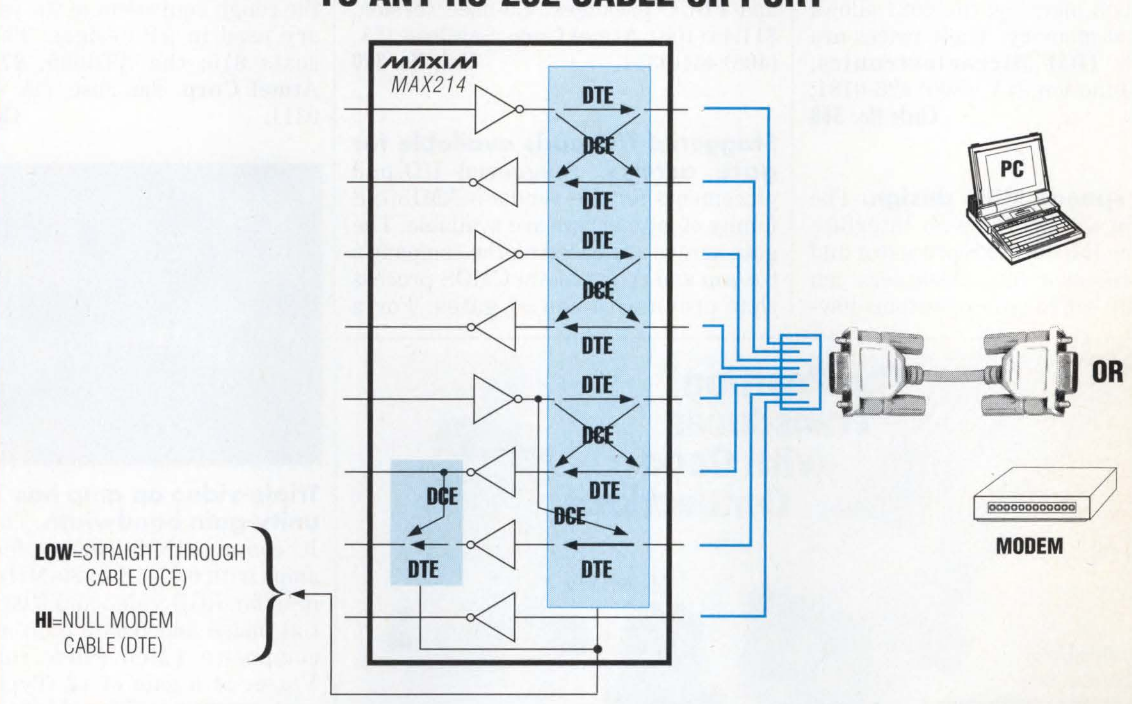

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CIRCLE NO. 28

INTEGRATED CIRCUITS

or color LCDs, plasma panels, and electroluminescent panels. The 65540 and 65545 are pin- and software-compatible; the 65545 has a hardware accelerator for Windows. Prices are $24 and $31, respectively (10,000). **Chips and Technologies Inc**, San Jose, CA. (408) 434-0600. **Circle No. 387**

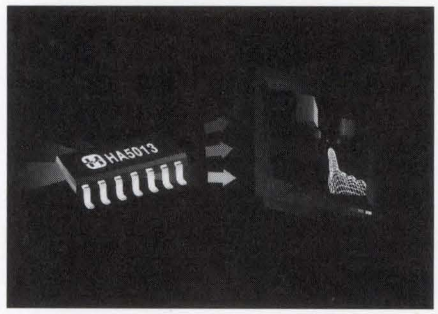
DSP family grows. The MDSP2020 and MDSP2021 DSPs for notebook computers provide audio-speed DSP with a 3.3V supply. They also offer sleep and suspend operating modes. The devices offer 20 kbytes of program and data memory; ISA-bus, audio codec, and telephony interfaces; and MIDI-port and UART emulation. The 2020 provides built-in memory; the 2021 allows for external memory. Their prices are <$30 each. **IBM Microelectronics**, Hopewell Junction, NY. (800) 426-0181, ext 500. **Circle No. 388**

Chip set speeds MIPS design. The Rab²it chip set provides an interface between the R4000 MIPS processor and the 486 processor bus. Designers can use the chip set to create systems having peripherals for the ISA architecture. The 2-chip set includes the interface device and a dynamic-RAM controller. The set operates at 67 MHz at 3.3V but includes a 5V interface buffer. Samples will be available in the fourth quarter for $120. **NEC Electronics Inc**, Mountain View, CA, (800) 366-9728. **Circle No. 389**

Flash version of the 22V10 is available. The ATF22V10B family, electrically erasable flash versions of the 22V10 PLD, offers 7.5- to 25-nsec speeds. The family is plug-compatible with other 22V10 CMOS and bipolar devices. The devices are available in 24-pin PDIP and CERDIP, plastic SOIC, and PLCC packages. 7.5-nsec version, $11.45 (100). **Atmel Corp**, San Jose, CA. (408) 441-0311. **Circle No. 390**

Staggered I/O pads available for gate arrays. Staggered I/O-pad placements for the vendor's AMI8GxS family of gate arrays are available. The gate arrays are based on the company's 0.8-μm and triple-metal CMOS process that provides a sea of gates. For a design requiring 208 pad locations, the staggered I/O technique realizes a 39 percent savings in silicon area. Gate-array prices for various options range from <$5 to $25. **American Microsystems Inc**, Pocatello, ID. (208) 233-4690. **Circle No. 391**

FPGAs have 500-μA standby current. The AT6002 and AT6005 field-programmable gate arrays (FPGAs) have 2000 and 5000 usable gates, respectively. The devices also offer thousands of registers for pipelining, 250-MHz toggle rates, and <1-nsec guaranteed clock skew. The devices also offer a 500-μA max standby current. The devices' T6000 cache logic is the rough equivalent of the cache memory used in μP designs. The AT6002 costs $16; the AT6005, $72 (5000). **Atmel Corp**, San Jose, CA. (408) 441-0311. **Circle No. 392**



Triple-video op amp has 125-MHz unity-gain bandwidth. The HA5013 IC contains three current-feedback op amps with 0.07-dB to 20-MHz gain flatness for RGB video and 0.03° differential phase and 0.03% gain at ±5V for composite video. Slew rate is 475 V/μsec at a gain of +2. Typical quiescent current is 7.5 mA/amplifier, and output current into a 150Ω load is typically 20 mA. In 14-pin DIPs and SOICs, the IC costs $3.50 (1000). **Harris Semiconductor**, Melbourne, FL. (800) 442-7747, ext 7219. **Circle No. 393**

Modem chip set suits audio applications. The CL-MD1414BA chip set comprises three chips that combine a data, fax, and voice modem with a sound card. Adding a 32-kbyte static RAM provides complete modem functionality. The audio suits multimedia presentations. On-chip DMA increases the audio sampling rate and offloads the host μP. The chip set supports all the popular standards for data, fax, and voice modes, including V.32bis. $60 (1000). **Cirrus Logic Inc**, Fremont, CA. (510) 623-8300. **Circle No. 394**

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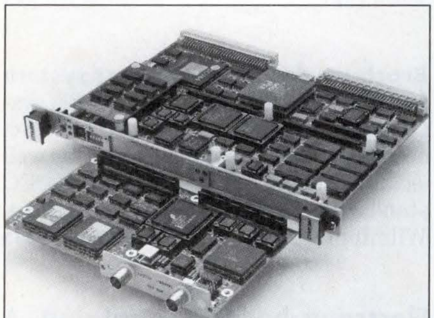
Dual-channel X.25 link fits in 3U VME. The VIX25 provides two telecommunications channels for use with packet-switched wide-area networks. The channels are full-duplex X.21*bis* links running the X.25 protocol and meeting Europe's NET2 certification tests. They offer data rates of 64 kbps over public networks and 2 Mbps over private networks. The 3U VME board requires 3.5W of power and costs $2055. A license for OS-9 applications software costs $180. **PEP Modular Computers**, Scottsdale, AZ. (602) 483-7100.
Circle No. 316



ATM comes to VME systems. By connecting to a DS3 telephone service, the CVME901 board brings asynchronous-transfer-mode (ATM) communications to VME systems. The board offers a hardware-based ATM adaptation layer (AAL) that handles packet segmentation and reassembly for service categories AAL 3/4 and AAL5. An on-board i960 processor handles congestion control, error checking, and the host interface. The board's DMA controller handles data at rates to 48 Mbytes/sec, ensuring that the board can handle communications traffic at the DS3 link's full speed. Price is $4597 (100). **Cyclone Microsystems**, New Haven, CT. (203) 786-5536. **Circle No. 317**

VME module hosts Alpha RISC processor. The VMEAlpha64/SP, a 2-board module, is based on the 150-MHz Alpha AXP processor. The design separates the CPU, its local memory, and secondary cache from the VME I/O channel to avoid interference. The module offers a 512-kbyte secondary cache, 128-Mbyte main memory, and a variety of peripheral interfaces, including Ethernet and SCSI. An i960 CPU is available as an optional I/O coprocessor. With the DEC OSF/1 operating system and a 1-Gbyte SCSI disk, the board costs $16,875. **Aeon Systems Inc**, Albuquerque, NM. (505) 828-9120.
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Adapter boards provide fast I/O. Working with standard peripheral and network interfaces, the 6U MVME-328XT and MVME385-120 boards provide high-speed I/O capability to the VMEbus. The 328XT ($3600) is a Fast SCSI-2 host adapter that handles as many as 14 devices, providing a 10-Mbyte/sec synchronous data-transfer rate on each of two independent channels. The 385-120 ($6895) uses dual 32-bit-wide static RAM (SRAM) buffers and dual-ported video RAM (VRAM) to match its memory I/O to the speed of its FDDI (fiber distributed data interface) port. The board can transfer data at 80 Mbytes/sec from SRAM, 60 Mbytes/sec from VRAM, and 50 Mbytes/sec from the VME interface to the FDDI. Prices start at $3245. **Motorola Computer Group**, Tempe, AZ. (800) 759-1107. **Circle No. 319**

Flash-memory board provides fault tolerance. Fitting in a single 6U VME slot, the RM250 board provides as much as 128 Mbytes of static RAM (SRAM) or flash memory. Two RM250 boards work in parallel to provide fault tolerance by automatically duplicating memory writes to one board on the other board and providing a software disable command. The board's nonvolatile memory works with either 5 or 12V flash memory or SRAM backed by two on-board lithium batteries. A control-status register reports battery failure. Prices start at $1333. **RAMix Inc**, Chats- worth, CA. (818) 349-6772.
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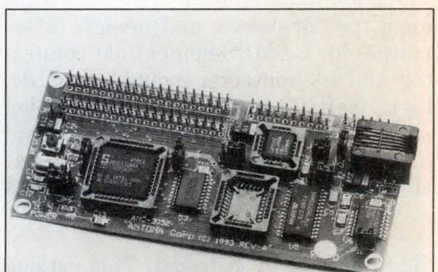
Board boosts performance with 68060 CPU. The PT-VME161 carries a 68060 CPU, which provides a 250% performance boost while retaining software compatibility with previous 68040 versions. It also offers a Fast SCSI-2 interface with DMA, dual serial I/O ports, and a 60-Mbyte/sec VME64-bus interface. The board's memory capacity ranges from 4 to 64 Mbytes. Prices start at $3245. **Performance Computer**, Rochester, NY. (716) 256-0200. **Circle No. 321**

Frame-grabber board handles rough environments. Designed for military and rugged commercial environments, the SVME/DMV-674 frame-grabber board provides the front end to a digital imaging system. It handles 525-, 675-, or 875-line interlaced frame formats with images as large as 1280×1024 pixels. The image-acquisition section provides three monochrome analog input lines sampled at 35M samples/sec to 8-bit resolution. It also offers a 16-bit digital input port. The board comes in six software-compatible versions for diverse environmental conditions and ranging from air-cooled commercial to conduction-cooled full MIL-SPEC ratings. Prices start at $6522. **DY 4 Systems Ltd**, Campbell, CA. (408) 377-9822.
Circle No. 322

Synchro/resolver accurate to 2 arc-minutes. Handling as many as four channels of synchro or resolver rotational-position-transducer signals, the MPX5000 and 501 VME boards offer an accuracy of ±2 arc-minutes. Each channel is programmable for 10-, 12-, 14-, or 16-bit resolution and offers an 8-bit turns counter. The boards track input signals to 15 rps with 16-bit resolution and to 960 rps with 10-bit resolution. Prices start at $2500. **Pentland Systems Ltd**, Danville, CA. (510) 736-5113.
Circle No. 323



Single-board computer runs Basic. Based on the 8032 processor, the ANC-3052B module allows designers to create applications programs in Basic. The module offers a 32-kbyte RAM bank and sockets for as much as 64 kbytes of PROM in addition to the Basic interpreter in ROM. The board includes two external interrupts, two counter/ timers, and eight digital I/O lines, along with a 20-pin adapter that can be wire-wrap configured to meet the I/O signal's pinout needs. The board costs $198 and is available without Basic for $146. **Antona Corp**, West Los Angeles, CA. (310) 473-8995.
Circle No. 324

500-pg temperature-measurement guide includes technical data. This free guide includes more than 100 pgs of technical data and specifications and application data on thermocouples, RTDs, connectors, panels, and instrumentation. **Thermo Electric,** Saddle Brook, NJ. **Circle No. 325**

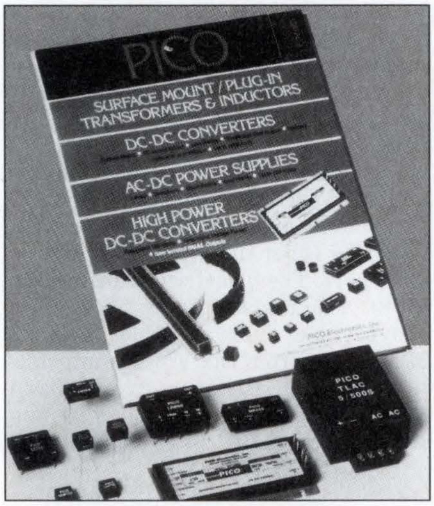
PCMCIA developer's guide. Guide gives comprehensive overview of the Personal Computer Memory Card International Association (PCMCIA) standard, along with design examples and reference materials. The 450-pg book also includes directories of PC Card, host computers, and desktop host adapters, as well as listings of ICs, development tools, and software. $89.95. **Sycard Technology,** Sunnyvale, CA. **Circle No. 326**

Application selector guide. This application guide details an extensive line of high-performance adhesive compounds for tacking wires and attaching components to printed wiring boards. The publication details 1- and 2-component epoxies, UV-curable epoxies, reactive acrylics, and hot-melt and cyanoacrylate adhesives. **Master Bond Inc,** Hackensack, NJ. **Circle No. 327**

Hot-pluggable connector catalog. The publication contains complete technical, performance, and design information for a SMPS-compatible connector and its contacts, including ac, dc, logic, signal, and hot plug. The catalog also includes photos and dimensional drawings. **Elcon Products International Co,** Fremont, CA. **Circle No. 328**

Electronic-case catalog. This catalog shows an expanded line of injection-molded ABS/polycarbonate, roto-molded, and vacuum-formed polyethylene-resin products. The publication details lightweight construction, waterproof, airtight, water- and dust-resistant ATA 300 standards, 2000-lb stacking loads, operating temperatures from –20 to +160°F, ultraviolet- and ozone-stabilized materials, and recessive hardware. Free. **Cases Plus Inc,** Livermore, CA. **Circle No. 329**

Fiber-optics catalog. A new 132-pg catalog features performance information and technical specifications on a line of fiber-optic connectors and adapters, as well as cable assemblies, termination tooling, fiber-optic switches, and premise-wiring products. The catalog also includes a glossary and a section describing connector-termination procedures, including tooling required. **Molex Inc,** Lisle, IL. **Circle No. 330**



High-power dc/dc converter catalog. This catalog introduces mountable and plug-in 100W dual-output dc/dc converters, transformers, and inductors. The dc/dc converter section details more than 1100 standard models with output voltages up to 1000V dc. This 136-pg catalog also offers an ac/dc power-supply section with linear and switchers in single, dual, and triple outputs. **Pico Electronics Inc,** Mount Vernon, NY. **Circle No. 331**

ISRs catalog. This catalog includes a new family of small, easy-to-use integrated switching regulators (ISRs) and a line of dc/dc converters. The 32-pg publication has complete product information, specifications, photos, and schematics on each power module; it also includes a section on product operation, applications, and special considerations. **Power Trends,** Batavia, IL. **Circle No. 332**

Catalog of passive components. This 93-pg catalog presents specifications and outline drawings on a variety of passive components in the frequency range of dc to 18 GHz. Commercial, industrial, and military components in the publication include fixed and tunable filters; fixed, high-power, programmable, and variable attenuators; high-power loads; SPDT, SP4T, and SP8T programmable switches; and built-to-order switching and control, rack-mountable subsystems. **Trilithic,** Indianapolis, IN. **Circle No. 333**

User-input device-data book. A data book for custom and standard user-input devices is available for system designers. The literature contains protocol descriptions, scan-code listings, schematics, and detailed application notes on an extensive set of encoder ICs. Also included are a recommended matrix layout for types of keyboards or keypads. For those designing low-power systems, the data book provides techniques to produce low-power keyboards. **USAR Systems,** New York, NY. **Circle No. 334**

Brochure describes ESD test system for ICs. This free brochure details systems for testing to MIL-STD 883c, according to a number of models, as well as latch-up testing according to JEDEC standards. **KeyTek Instrument Corp,** Wilmington, MA. **Circle No. 335**

Electronic-hardware catalog. A 200+-pg, electronic-hardware catalog offers specifications for circuit-board spacers, captive panel screws and retainers, standoffs, chassis and cabinet handles, shoulder screws, and more. **RAF Electronic Hardware,** Seymour, CT. **Circle No. 336**

Catalog covers DSP hardware, software, and development tools. This free 134-pg catalog describes boards, boxes, systems, operating systems, design software, and development tools. **Sonitech International Inc,** Wellesley, MA. **Circle No. 337**

Product handbook. A 320-pg catalog describes the company's line of data-acquisition and imaging products. The handbook highlights software solutions, from programming tools to applications, and includes technical tutorials and products that help you choose the optimum solution for data-acquisition and imaging applications. Free. **Data Translation,** Marlborough, MA. **Circle No. 338**

Preview of microterminals. The catalog details small, rugged microterminals designed as operator-interface/control panels and data-collection terminals; it also contains specifications, photos, and information on key features and applications. **Burr-Brown Corp,** Tucson, AZ. **Circle No. 339**

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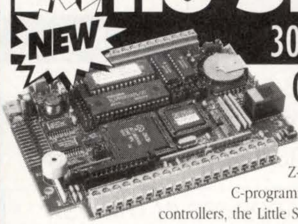

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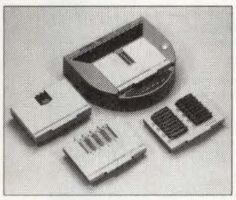

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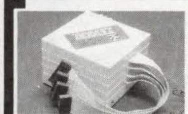

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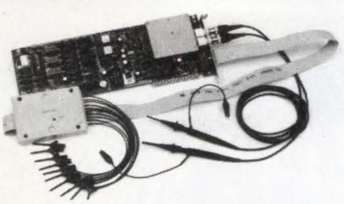

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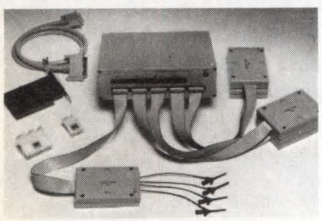

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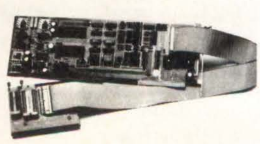

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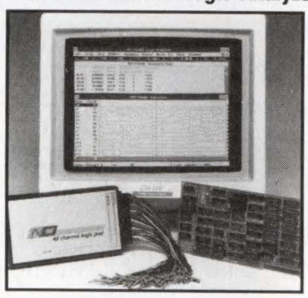

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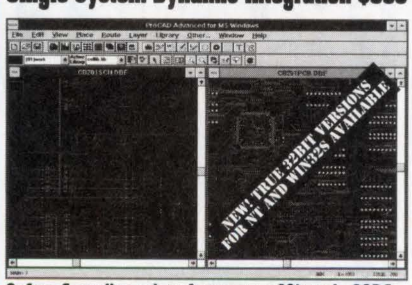

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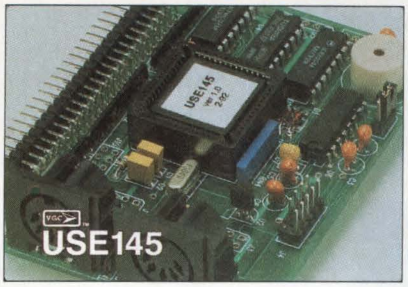

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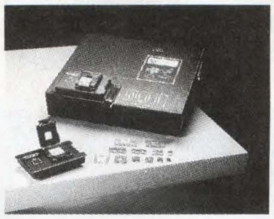

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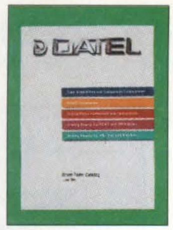

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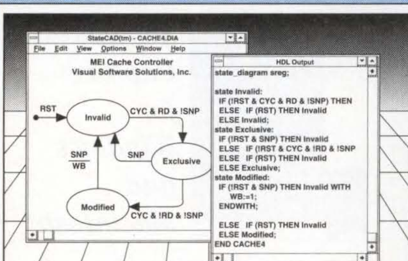

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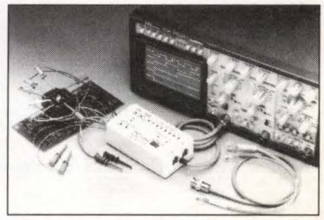

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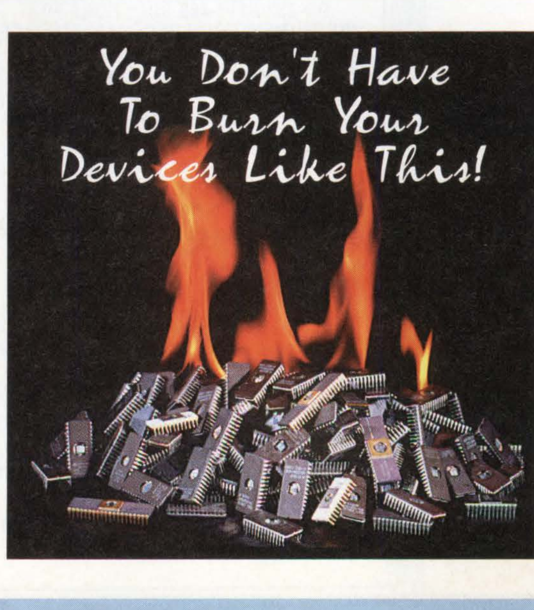

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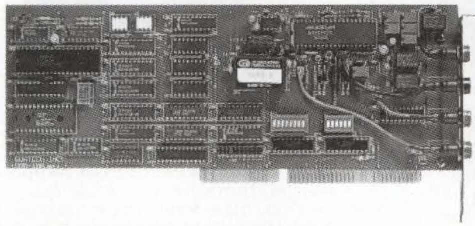

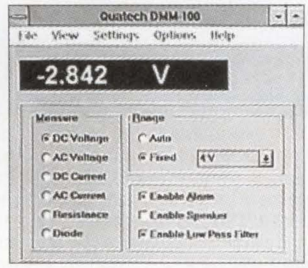

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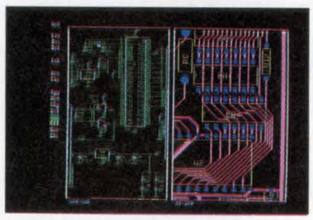

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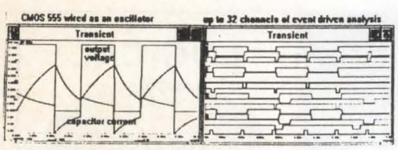

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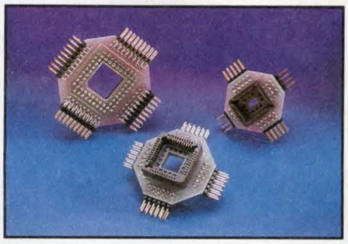

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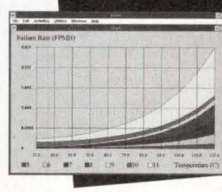

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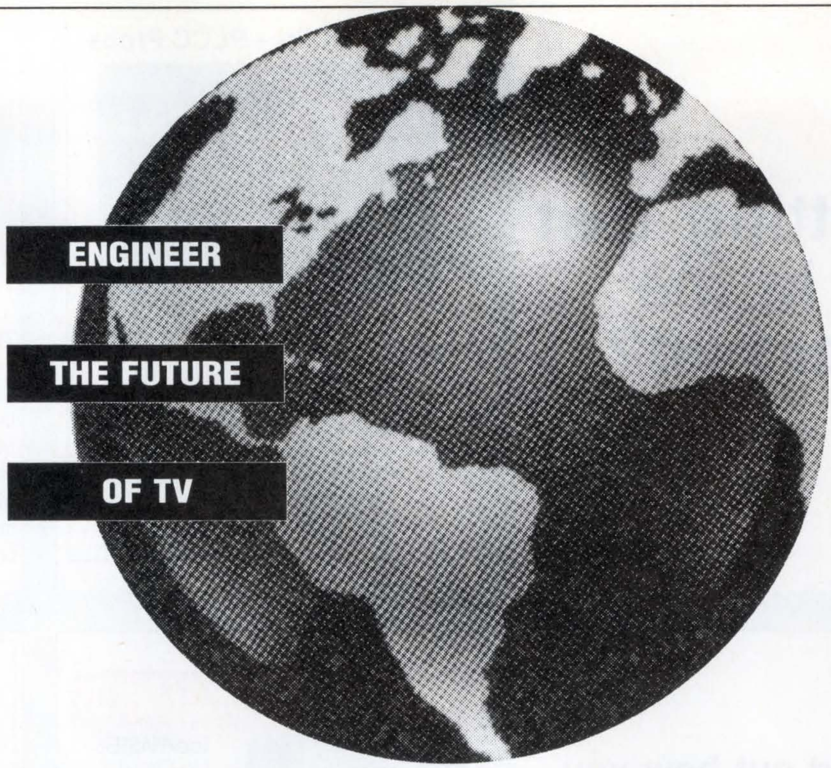

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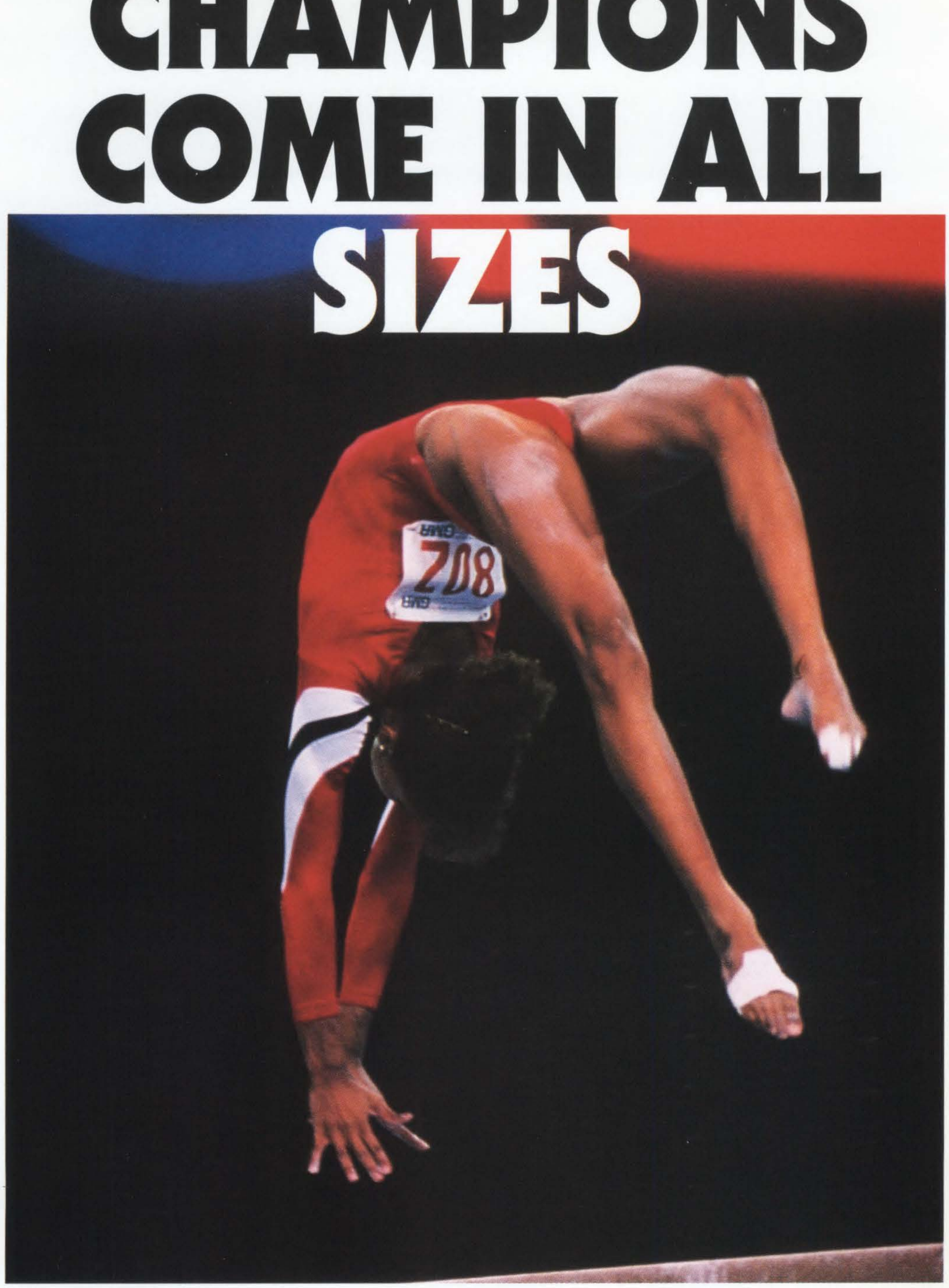
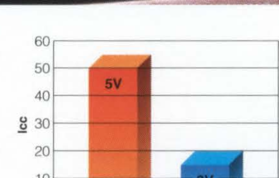


They took 90 pounds of power to new heights, and redefined the meaning of performance.

Atmel also offers championship performance. We married our 3-volt proprietary process with a four-megabit Flash so you can take your design to new heights.



The AT29LV040 is not some stripped-down version. It has all the stuff you've come to expect from Atmel's 3-volt Flash memory. A single power source for both read and write. The world's easiest algorithm, just load and go – there's no erase cycle. Small memory sectors for fast and easy reprogramming.

And, for you folks who are not working on carry-on equipment, we also make a 5-volt-only version of our four-megabit Flash, the AT29C040.

Take your pick, 3-volt or 5-volt, they're all in our new Flash record book. Write or give us a call at **(800) 292-8635** for the book, then let Atmel Flash give your design the championship edge.

Atmel Corporation Headquarters: 2125 O'Nel Drive, San Jose, CA 95131 (408) 441-0311, FAX (408) 436-4300.

CIRCLE NO. 48

The World's Gone Flat.

Signal's International Flathead™ Circles The Globe.

The whole world's going flat out for Signal's International Flathead transformers, because we went all out to win international approval.

These super rugged, low profile transformers, fully encapsulated and hermetically sealed, meet UL, CSA, VDE, IEC and EN standards for international use.

Thanks to their extremely low profile, these IF series transformers are ideally suited for use on densely packed PC boards.

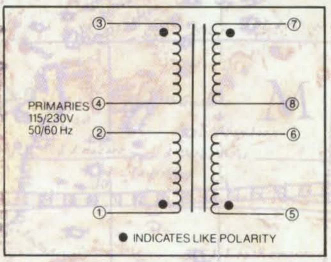
Available in 2VA to 30VA configurations, these Flatheads feature dual primaries (115/230V, 50/60Hz) and non-concentric windings. The result: reduced inter-winding capacitance and the elimination of electrostatic shielding.

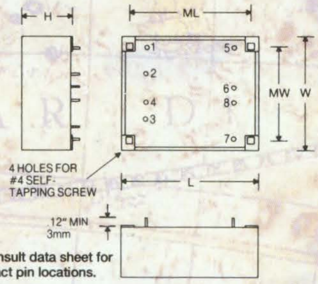
- Low profile (as low as 0.69")
- Precise pin alignment for drop-in applications
- Class B insulation (130° C)

For more information on Signal's International Flathead Series, contact Signal Transformer, 500 Bayview Ave., Inwood, NY 11696.

Sampling of products offered. A total of 80 part numbers are available off-the-shelf in 2, 4, 6, 10, 14, 18, 24, 30 VA sizes.

		SECONDARY		PRICE
Part No.	Size	Series	Parallel	100-249 Pcs
IF-2-10	2VA	10Vct. @ 200mA	5V @ 400mA	
IF-2-12	2VA	12Vct. @ 170mA	6V @ 340mA	
IF-2-16	2VA	16Vct. @ 125mA	8V @ 250mA	
IF-2-20	2VA	20Vct. @ 100mA	10V @ 200mA	
IF-2-24	2VA	24Vct. @ 85mA	12V @ 170mA	$7.63
IF-2-30	2VA	30Vct. @ 70mA	15V @ 140mA	
IF-2-34	2VA	34Vct. @ 60mA	17V @ 120mA	
IF-2-40	2VA	40Vct. @ 50mA	20V @ 100mA	
IF-2-56	2VA	56Vct. @ 40mA	28V @ 80mA	
IF-2-230	2VA	230Vct. @ 9mA	115V @ 18mA	
IF-10-10	10VA	10Vct. @ 1.00A	5V @ 2.00A	
IF-10-12	10VA	12Vct. @ 835mA	6V @ 1.67A	
IF-10-16	10VA	16Vct. @ 625mA	8V @ 1.25A	
IF-10-20	10VA	20Vct. @ 500mA	10V @ 1.00A	
IF-10-24	10VA	24Vct. @ 420mA	12V @ 840mA	$9.49
IF-10-30	10VA	30Vct. @ 335mA	15V @ 670mA	
IF-10-34	10VA	34Vct. @ 300mA	17V @ 600mA	
IF-10-40	10VA	40Vct. @ 250mA	20V @ 500mA	
IF-10-56	10VA	56Vct. @ 180mA	28V @ 360mA	
IF-10-230	10VA	230Vct. @ 45mA	115V @ 90mA	
IF-30-10	30VA	10Vct. @ 3.00A	5V @ 6.00A	
IF-30-12	30VA	12Vct. @ 2.50A	6V @ 5.00A	
IF-30-16	30VA	16Vct. @ 1.90A	8V @ 3.80A	
IF-30-20	30VA	20Vct. @ 1.50A	10V @ 3.00A	
IF-30-24	30VA	24Vct. @ 1.25A	12V @ 2.50A	$13.99
IF-30-30	30VA	30Vct. @ 1.00A	15V @ 2.00A	
IF-30-34	30VA	34Vct. @ 900mA	17V @ 1.80A	
IF-30-40	30VA	40Vct. @ 750mA	20V @ 1.50A	
IF-30-56	30VA	56Vct. @ 550mA	28V @ 1.10A	
IF-30-230	30VA	230Vct. @ 130mA	115V @ 260mA	





Consult data sheet for exact pin locations.

Size	L	W	H	ML	MW	WGT
2	2.09" 53.0mm	1.73" 44.0mm	0.69" 17.6mm	1.87" 47.5mm	1.48" 37.5mm	4.6oz 0.13kg
10	2.66" 67.6mm	2.24" 57.0mm	0.89" 22.6mm	2.46" 62.5mm	1.97" 50.0mm	10.3oz 0.29kg
30	2.68" 68.0mm	2.26" 57.5mm	1.39" 35.3mm	2.46" 62.5mm	1.97" 50.0mm	19.7oz 0.58kg

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CIRCLE NO. 88