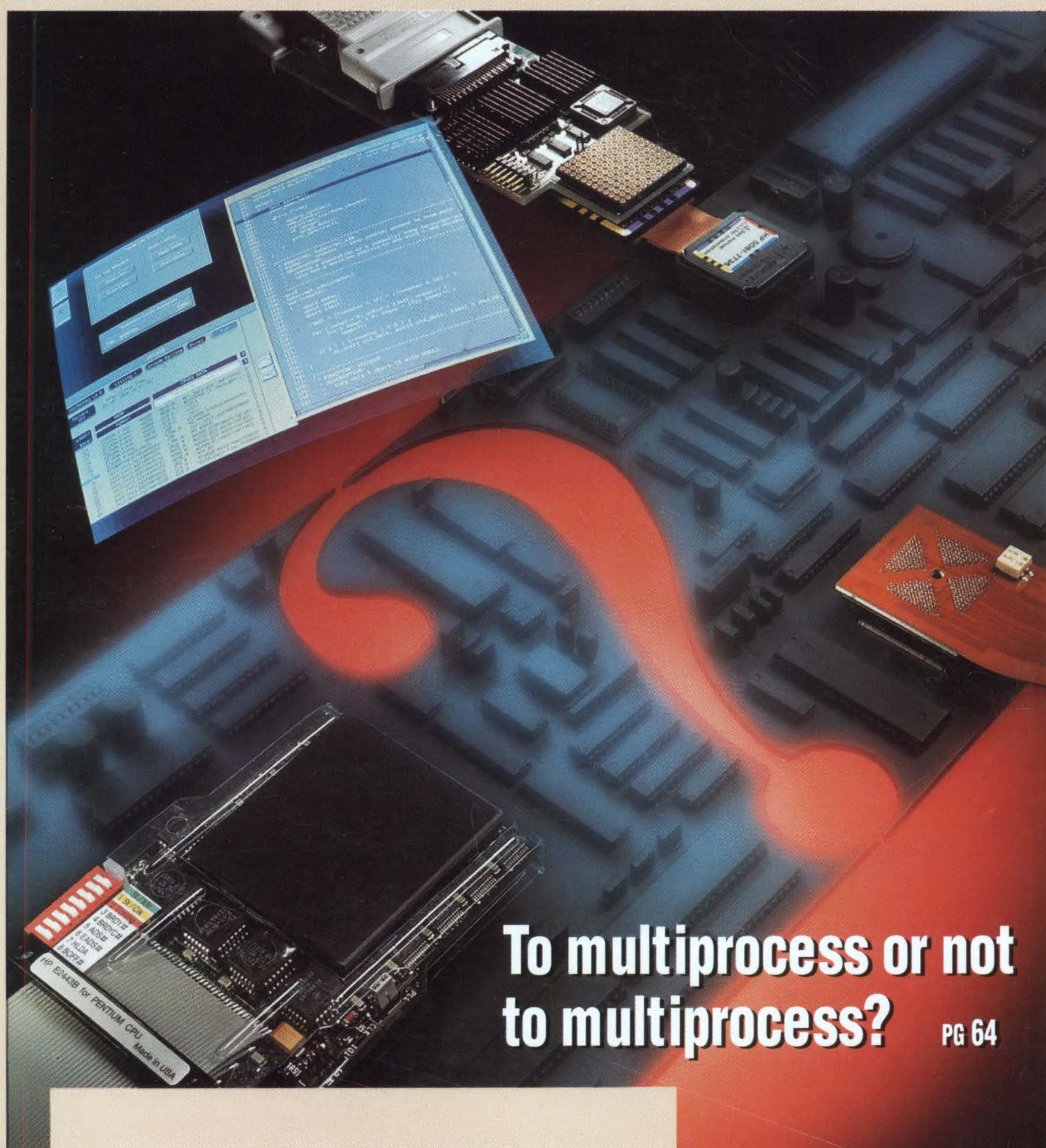
EDN®

THE DESIGN MAGAZINE OF THE ELECTRONICS INDUSTRY

June 23, 1994



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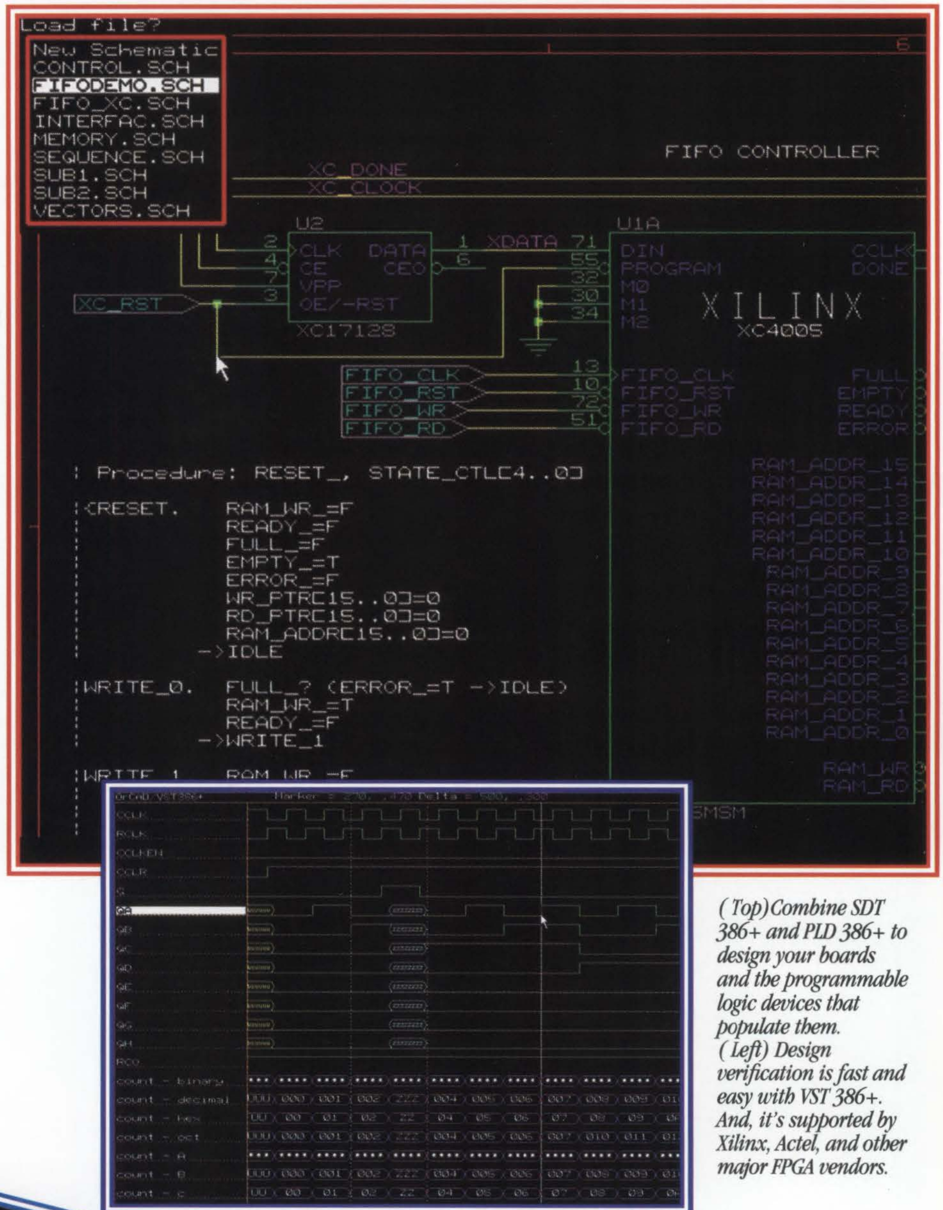

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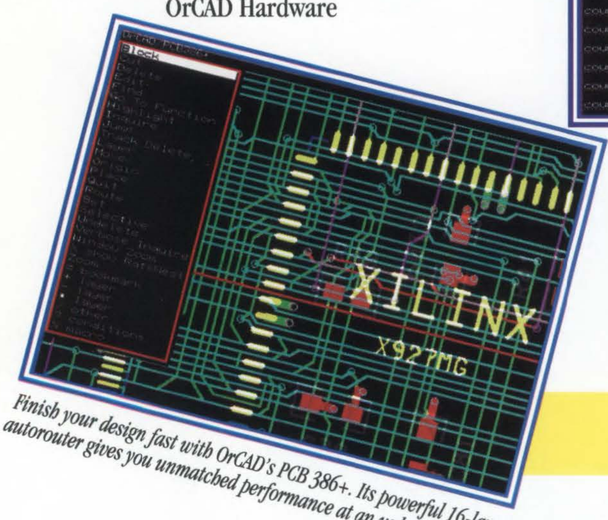

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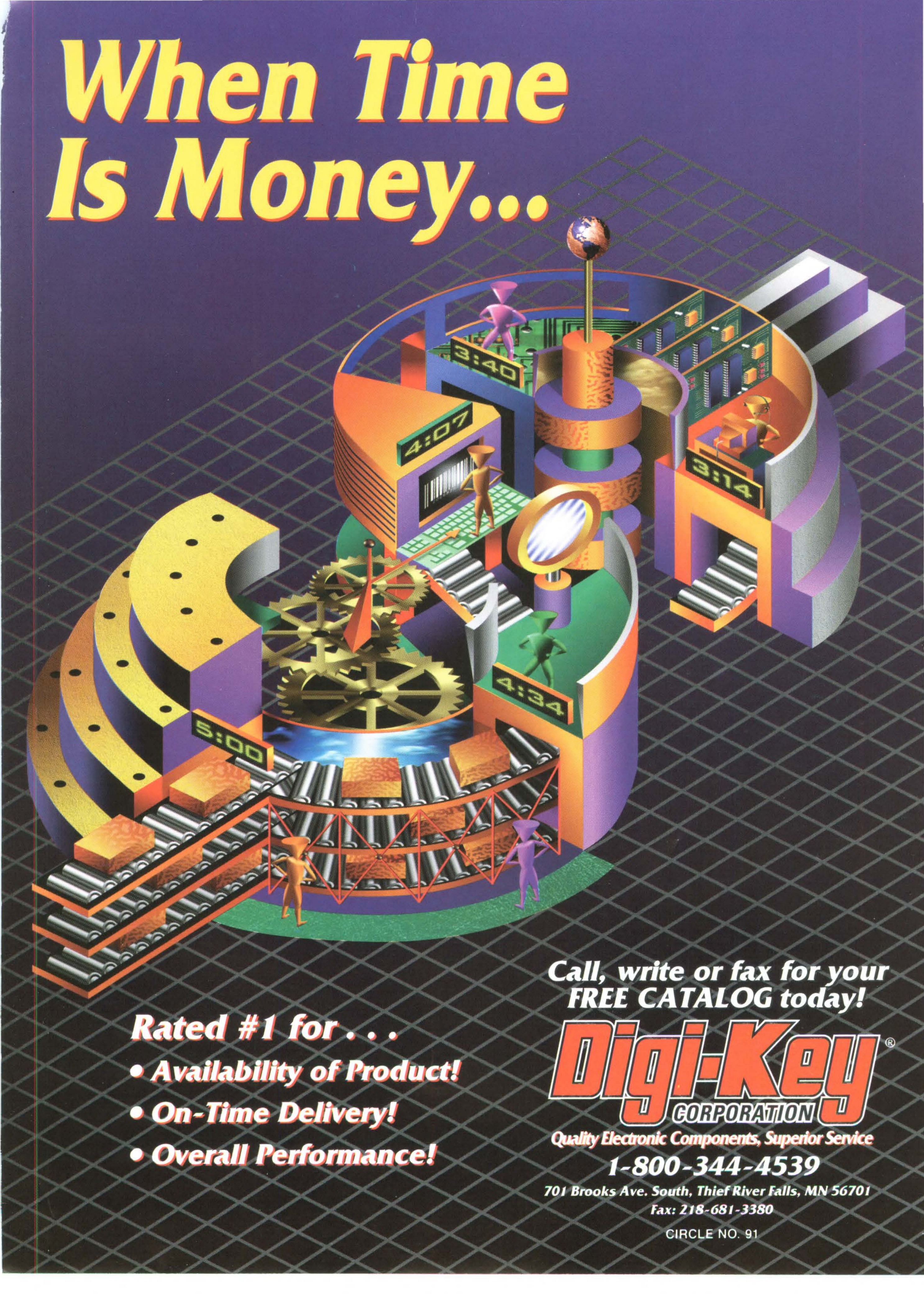

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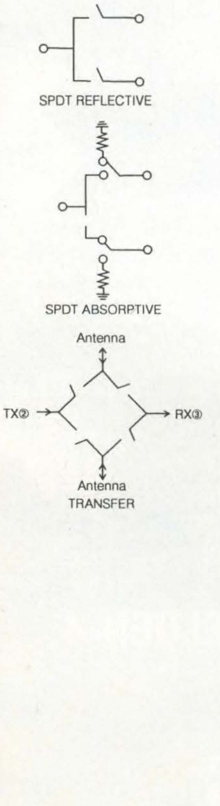

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June 23, 1994 VOLUME 39, NUMBER 13

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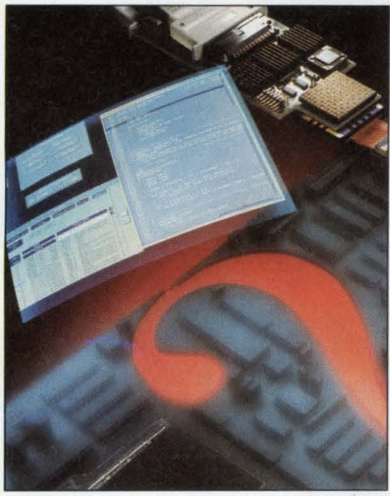

On the cover: When to use several processors—that is the question. If you've got practical problems, tight schedules, and limited budgets, multiprocessing might be the answer. See our Special Report, beginning on **pg 64.** (Photo courtesy Hewlett-Packard)

Continued on page 7

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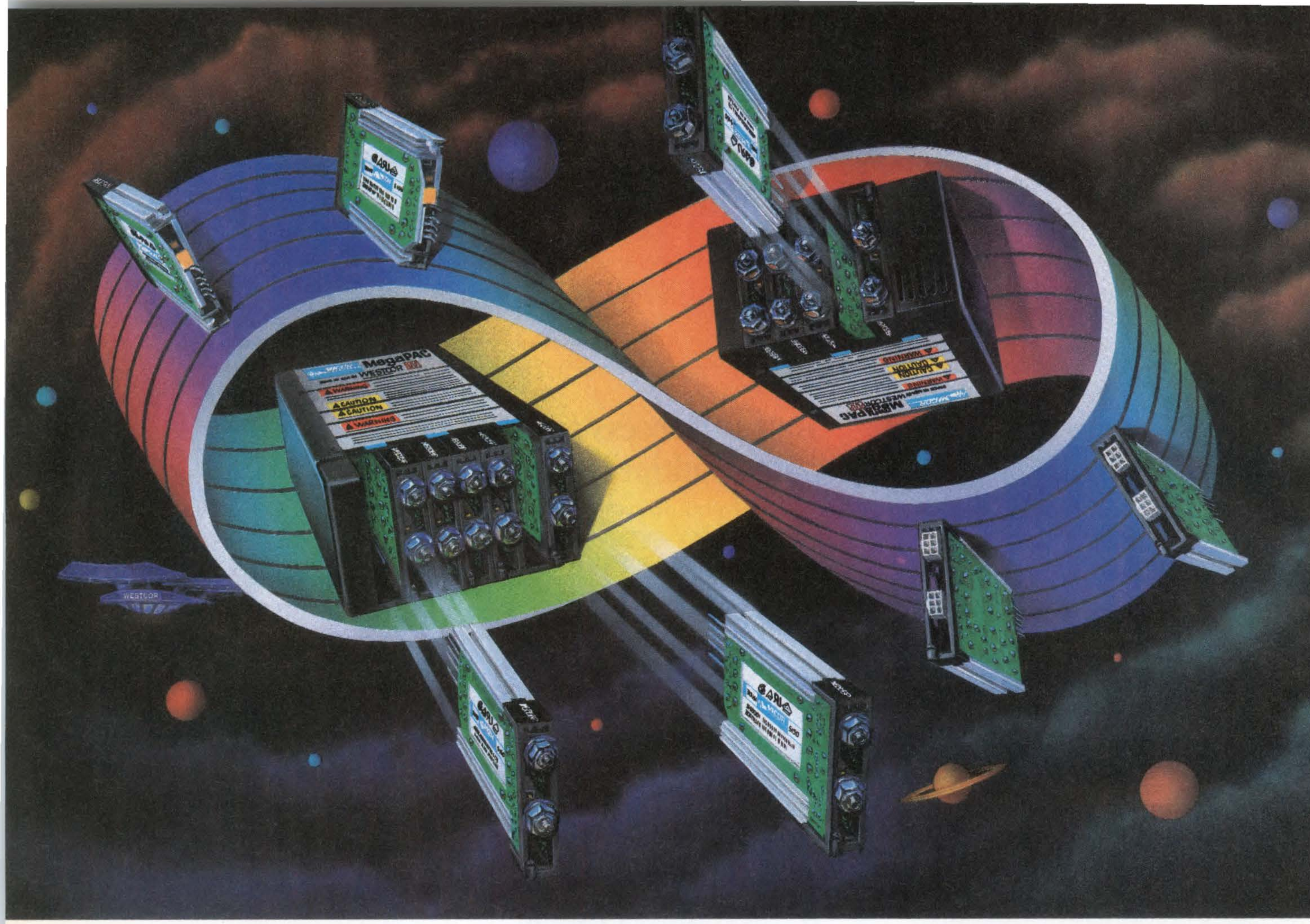

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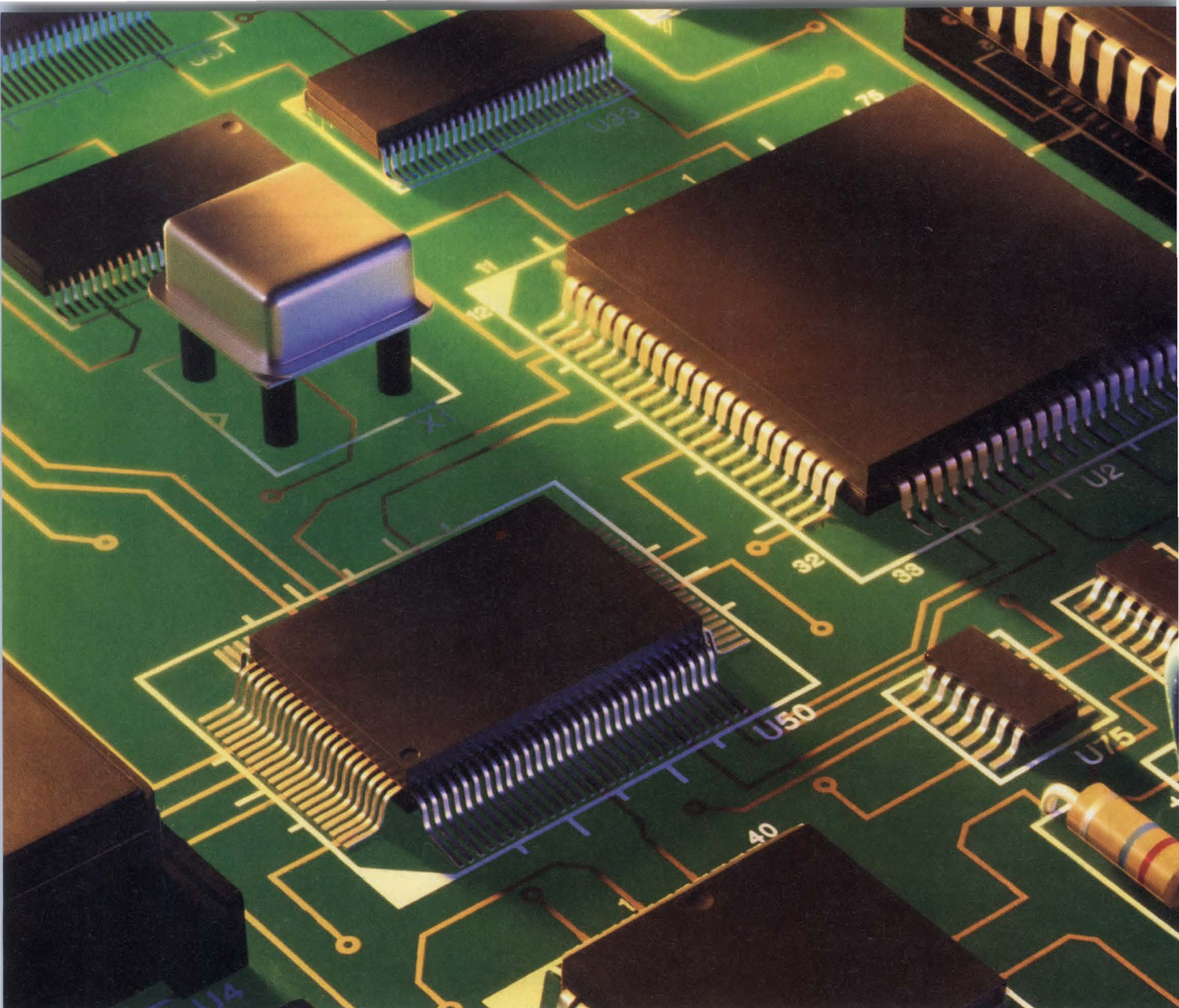

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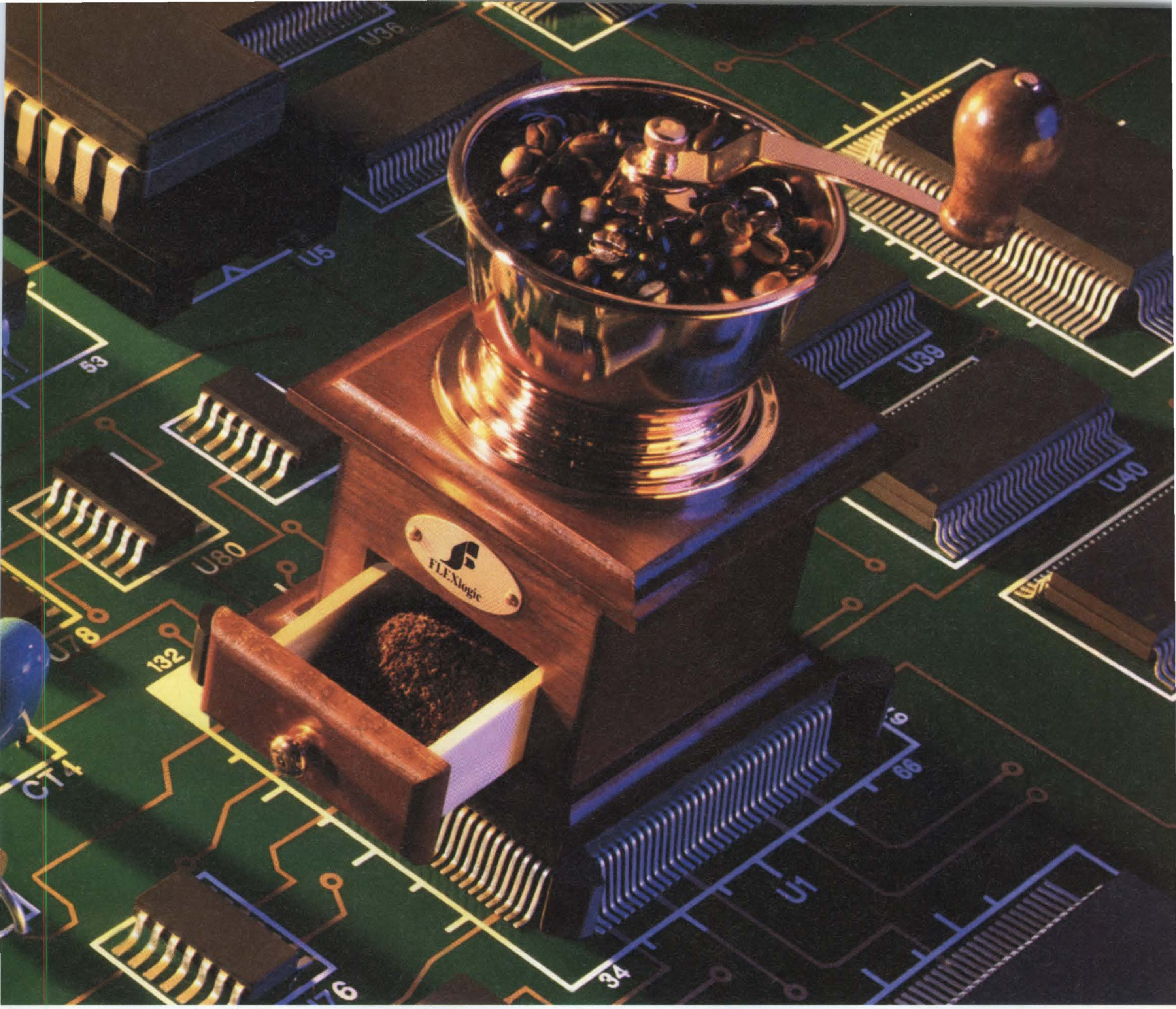
iFX780	80	10ns	102	1.5mA/MHz
iFX760	60	10ns	60	1.5mA/MHz
iFX740	40	10ns	50	1mA/MHz
iFX730	30	10ns	30	1mA/MHz



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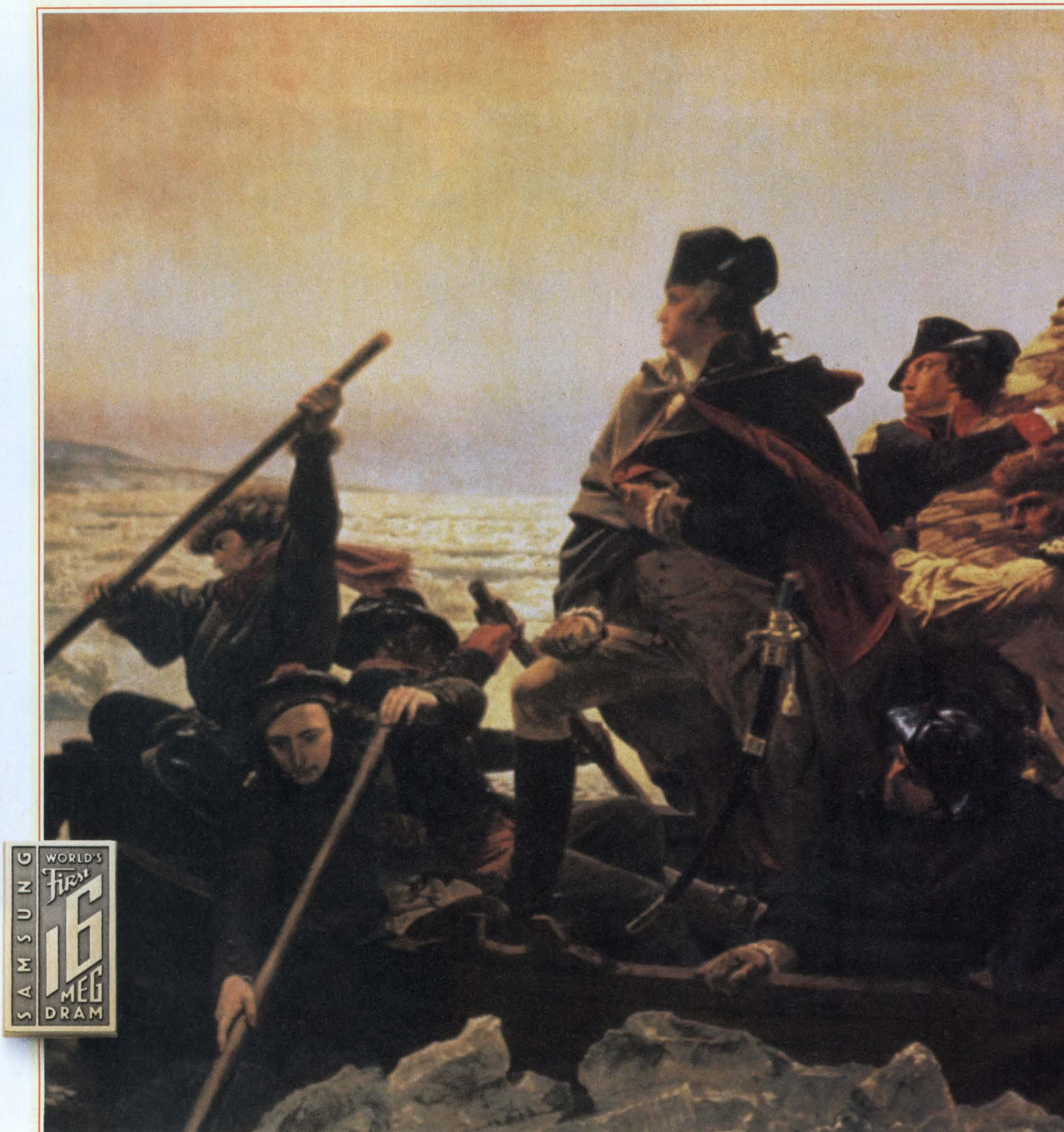

You're designing a Pentium- or Power PC-based system and you know it needs synchronous SRAM cache to generate the performance it ought to have.

But synchronous SRAM cache is so expensive that using it is prohibitive.

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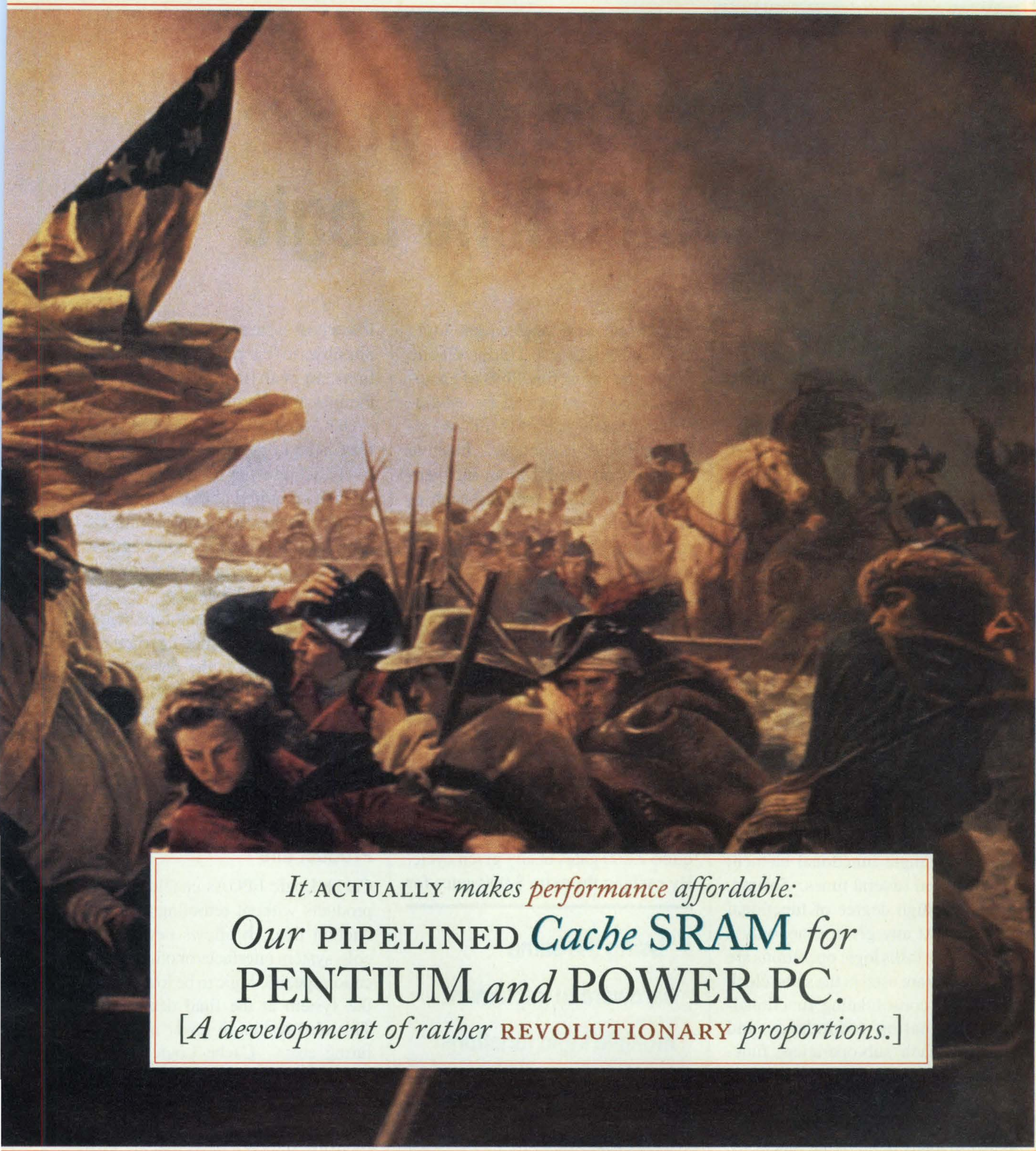

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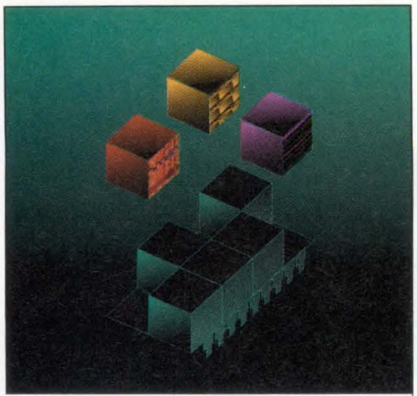

Ca$hing-In on Cache Logic

A cartoon from the 1920s has a musician soundly sleeping through the William Tell Overture until the precise moment his one triangle note is queued by the conductor. His work done, the character immediately falls back to sleep. The paradox of contemporary digital design is many logic devices on the board play a very limited part. In actuality, an orchestra percussionist plays scores of instruments during the course of a performance. Diversity is function in the rhythm section.

In contemporary designs, a single task or feature application is usually made up of many small, macro-level operations; like counters, multipliers, shift registers, and multiplexers. When that task is divided into its sub-operations, two things become apparent. First functionality overlaps; any single functional element may be used several times. Second, there is a high degree of functional latency. At any given time, only a portion of a tasks logic operations are active; few are used in the same clock cycle. By consolidating functionality, eliminating redundancy and tracking each sub-operation, functions can be organized so a single relatively small, inexpensive device can be continually reconfigured to perform many or all of the functions. And, otherwise costly, space consuming parts can be designed-out. Such adaptive logic also cuts months in development time by reusing proven functions, extends product life, and insures compliance to standards and protocols as yet unwritten.

Atmel Corporation has developed an enabling technology to implement Cache Logic™ designs; it is a simple and straight forward way of implementing task application logic more efficiently. Under Cache Logic, the active functions of an application are performed by a field-programmable gate array (FPGA) reconfigured as it operates. Inactive functions are stored in an inexpensive configuration memory such as an EPROM. As new functions are called, they are written directly over the last functions.

Designing with Cache Logic

Cache Logic is similar in concept to cache memory. In cache memory, the high-speed memory (usually SRAM) is used to store active data, while the bulk of data resides in lower cost storage, such as Flash memory, EPROM, or disk. In Cache Logic, a conventional 10,000-gate application might actually only require 2,000 gates at any given cycle. By caching the extra 8,000 gates for later use, a 2,000-gate device replaces an expensive 10,000-gate device. Since only a small fraction of the circuit is active at any given time, only those functions which are loaded into the logic cache. Reserve functions, or variations, reside in lower cost system memory. It's even possible to compile design variations, in real time. This may be thought of as hardware sub-routing.

> **"Using the same hardware to implement multiple logic functions significantly cuts design and production costs."**
>
> *– Joel Rosenberg*
> *FPGA Marketing Manager*
> *Atmel Corporation*

The Atmel AT6000 FPGA is ideal for Cache Logic designs. To effectively achieve the functionality and diversity required of Cache Logic an FPGA must be capable of continuous dynamic in-system reconfiguration—without disrupting the remaining logic inside the device.

At the board-level prototype stage, Cache Logic can reduce the time required to complete the design conception and implementation. Cache Logic FPGAs can be reconfigured at any time throughout the design cycle without being removed from the circuit board for reprogramming.

Added Value Extends Product Life

Cache Logic FPGAs enable custom products without retooling the production line. It allows new protocols, system interfaces or other application specific logic to be loaded into the system at the final destination. This also results in lower manufacturing costs. Cache Logic FPGAs eliminate special manufacturing flows and mis-programmed devices. Inventory management is simplified by using standard parts that are programmable in-system.

On the flip side, system development time and risk can be significantly reduced by using functions already proven. Once a design is simulated and working, the function may be saved (in software) for use in subsequent designs.

For more information call: 800-292-8635

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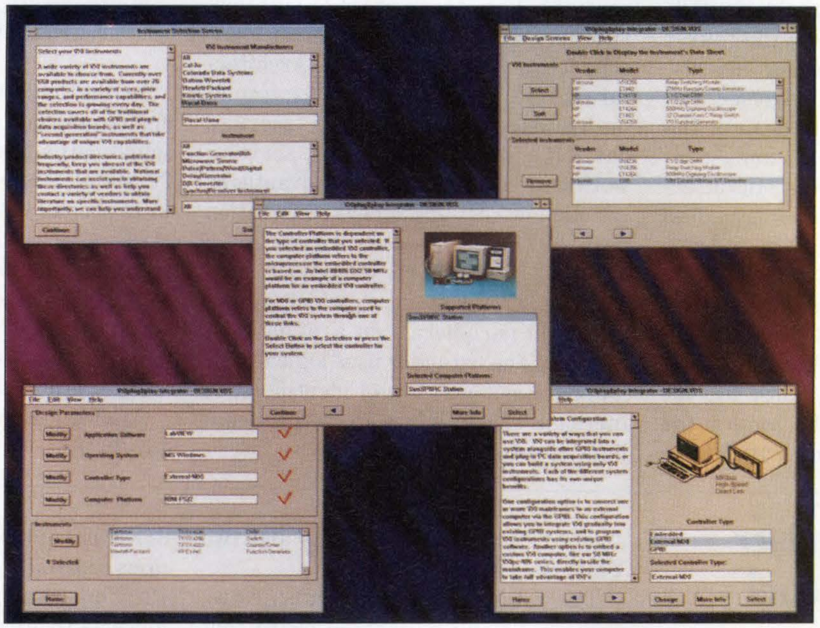
EDITED BY FRAN GRANVILLE

Fre tool helps configure multivendor VXI systems

An interactive CD-ROM-based Windows software tool called VXIplug&play Integrator asks questions about your application, controller type, operating system, and software needs. Based on your answers, it assists you in making choices of system hardware and software. As you decide which elements you want to use, the tool makes sure that your choices are compatible. For example, if you select an embedded controller with internal ISA bus expansion slots, you can learn about compatible data-acquisition, DSP, and IEEE-488 boards. At the end of the process, you will have all of the information you need to order each component from its manufacturer.



Configuring multivendor VXI systems that work right out of the box has become less problematical with the introduction of VXIplug&play Integrator, an interactive CD-ROM-based software tool available free from National Instruments.

Also on the CD-ROM are an extensive tutorial covering VXIbus capabilities and specifications and data sheets for 80 VXI instruments from such vendors as Hewlett-Packard, Racal Instruments, and Tektronix. Driver software compatible with National Instruments' LabView and LabWindows application-development packages is available for all of these instruments. In addition, the CD-ROM contains demonstration versions of LabView, LabWindows, and LabWindows/CVI.

The free package requires at least a 386-based PC running Windows 3.1 and having at least 4 Mbytes of RAM. The PC must have a CD-ROM drive and a VGA monitor that displays at least 256 colors.

—by Dan Strassberg

National Instruments Corp, Austin, TX, (512) 794-0100. **Circle No. 466**

Fast μPs and I/O draw attention at Comdex

Blazingly fast processors and speedy I/O schemes got a share of the spotlight at the recent Spring Comdex in Atlanta, with most of the attention falling on Alpha, Mips, and PowerPC μPs and on products for the Peripheral Component Interconnect (PCI) local bus. The joint presentation of Comdex and Windows World drew more than 500 exhibitors and 100,000 attendees. Although computer products for retailers and end users largely dominated the combined show, OEM products were in abundance.

Alpha μPs from Digital Equipment Corp were the speed champs of the show. New PCs and workstations from Aspen Systems, Carrera Computers, and NekoTech featured the 275-MHz Alpha 21064A, and Carrera demonstrated a 333-MHz system based on a still-unreleased Alpha chip. Comdex also marked the official availability of the 200-MHz Mips R4400 μP from semiconductor partners Integrated Device Technology, Mips Technologies, NEC, and Toshiba. Motorola pushed the new and relatively inexpensive PowerPC 603 at the show, as well as new PowerPC development tools for Windows NT.

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The PCI bus was prominent at Comdex, with new products for designers ranging from development tools to disk accelerators. Development tools from FirmWorks, for example, include a collection of Open Firmware ROMs, drivers, and tools that help you develop boot firmware for use on different processors and buses. Some modules in the collection apply specifically to PCI. For PCI add-in cards based on i960 μPs, new tools from Intel aid development. A bridge chip from PLX Technology provides the PCI-to-i960 connection.

FirmWorks, Mountain View, CA, (415) 917-0100. **Circle No. 476**

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PLX Technology, Mountain View, CA, (415) 960-0448. **Circle No. 478**

Disk accelerators introduced at Comdex help disk drives catch up to the speedy PCI bus. Accelerators from Promise Technology, available in IDE and SCSI versions, provide burst throughput of 132 Mbytes/sec and sustained transfers of 33 Mbytes/sec. For do-it-yourself accelerator design, the new Forsythia PCI-IDE cache-controller chip from Infomedia Microelectronics allows sustained data transfers of 22 Mbytes/sec for read operations and 33 Mbytes/sec for writes.

Infomedia Microelectronics Inc, Fremont, CA, (510) 683-9088. **Circle No. 479**

Promise Technology Inc, San Jose, CA, (408) 452-0948. **Circle No. 480**

Small-disk storage took a jump at the show with a new 2.5-in., 810-Mbyte drive from IBM. The 3-platter drive uses magneto-resistive (MR) heads and comes in AT (IDE) and Fast SCSI-2 versions. For larger storage systems, IBM announced that 17 companies are supporting its Serial Storage Architecture (SSA). SSA is a full-duplex, frame-multiplexed interface for storage devices, storage subsystems, servers, workstations, and PCs. Its advantages include low cost and an easy migration path for SCSI systems. SCSI got a boost itself from Micro Design International's SCSI Extender, which allows use of 49 peripherals on a single host adapter. The extender uses logical-unit numbers, not just target identifiers, to increase the number from the usual limit of seven.

International Business Machines Corp, White Plains, NY, Call local office. **Circle No. 481**

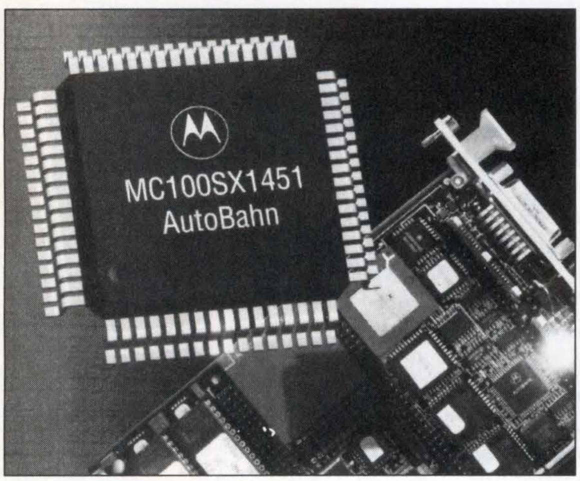
Micro Design International Inc, Winter Park, FL, (407) 677-8333. **Circle No. 482**

In the huge sight-and-sound multimedia portion of the show, DSP-based sound cards based on Analog Devices' Personal Sound Architecture (PSA) were a small but notable presence. DSP cards account for only 4% of the sound-card market, but of that 4%, according to Analog Devices, PSA has 75%. The company says PSA has reached an installed base of 250,000 in the year since its introduction.—by Gary Legg

Analog Devices, Norwood, MA, (617) 461-3881. **Circle No. 483**

AutoBahn Spanceiver concept is functional at first silicon

Motorola Semiconductor and PEP Modular Computers have achieved functional silicon from the first wafers of the AutoBahn Spanceiver (serial-parallel transceiver), an ECL gate array that transfers data at 1.6 Gbps. PEP created the AutoBahn for 3U VMEbus



cards. Motorola is fabricating the Spanceiver wafers in the 0.8-μm Mosaic V process and expects the beta-test program to last several months. When the wafers become available, Motorola will begin offering samples within 60 days. Sample prices will range from $180 to $250, depending on quantity. To speed proliferation of Spanceivers in VME applications, PEP has announced a starter kit for VME designs and two VME boards.

The kit includes two Spanceivers, each on a small mezzanine board that plugs into the VME backplane. The mezzanine comes with 128 kbytes of 20-nsec static RAM, a fast GAL containing logic circuitry to connect the parallel interface to a 32-bit data source, an address counter, and the serial interface to pins on the VME backplane. Designs from the kit should reach a sustained transfer rate as high as 200 Mbytes/sec. The kit comes with one or two PEP VM30 68EC030/68302-based single-board computers that implement PEP's public-domain controller-extension module as an electrical extension of the data and address lines of the 68302 intelligent multiprotocol processor. The kit also includes a data pack specifying start-up methodologies, test equipment, typical measurements, and results evaluation. A kit with one VM30 costs $4990; one with two VM30s costs $6295. Adding a Spanceiver mezzanine costs $690; an AutoBahn backplane costs $590.

PEP also announced two boards: the VM42A single-board computer and the VGPM-32 graphics subsystem. The VM42A offers a choice of μPs: a 40-MHz 68LC040 or 68EC040 or a 50-MHz 68040. It also includes a 25-MHz 68EN360 quad-integrated communications controller that supports Ethernet, Profibus, and RS-232C modems; as much as 16 Mbytes of dynamic RAM; as much as 4 Mbytes of EPROM; and 1 Mbyte of static RAM. The highest performance device sells for $2355 (1 to 9). The graphics board includes a 32-MHz, 32-bit Texas Instruments TMS34020 μP, a 1-Mbyte video RAM, an X.11 window server, a 4-Mbyte dynamic RAM, a 135-MHz, 8-bit/pixel color look-up table, a hardware cursor, and an 1180×800×8-bit, 256-color RGB output. Price is $2650 (1 to 9).

—by Fran Granville

Motorola Semiconductor Products Sector, Phoenix, AZ, (602) 655-5734. **Circle No. 484**

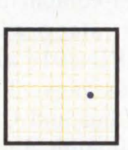
PEP Modular Computers, Scottsdale, AZ, (602) 483-7100. **Circle No. 485**

Hitachi sticks another feather in its KAP

Hitachi's H8/3434 IKAP (for integrated keyboard and power management) II is not just your usual keyboard controller. Designed for high-end portable computers, the device provides an interface for an external keyboard, a mouse, and other input devices. Like most other integrated keyboard controllers, the IKAP-II can suspend and awaken the CPU and peripheral devices. Besides handling power management, the device's A/D converter feeds back information pertaining to a

Get a sample of reality.

Looking for analog confidence in a digital oscilloscope? Tektronix' TDS 350 sets the standard with Digital Real Time. ■ Its incredible *one gigasample/second* sampling delivers real-life capture like never before—both for single shot or repetitive events. Select peak detect for slow events, or push the scope to its full 200 MHz bandwidth—with no aliasing. ■ And, like the entire TDS 300 family, the TDS 350 sets a new standard in price/performance: under $4000.



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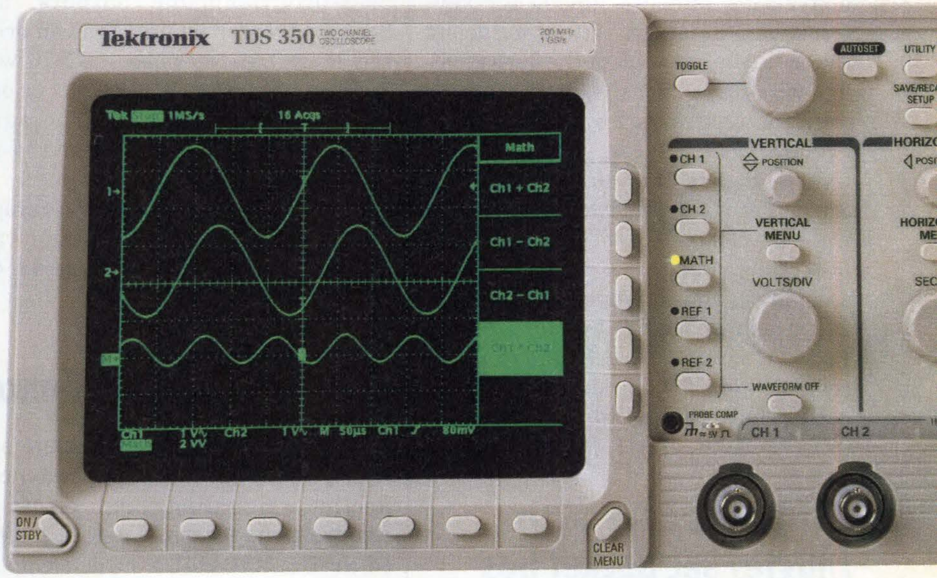

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Max Sample Rate	200 MS/s/chan	500 MS/s/chan	1 GS/s/chan
Sweep Speeds	10 ns/div - 5 s/div	5 ns/div - 5 s/div	2.5 ns/div - 5 s/div
Channels	2	2	2
Vertical Sensitivity	2 mV - 10 V	2 mV - 10 V	2 mV - 10 V
Vertical Resolution	8 bits	8 bits	8 bits
Record Length	1K/channel	1K/channel	1K/channel
Standard Advanced Features	TV Line & Field Trigger, Roll Mode, Autoset, 21 Automatic Measurements, Peak Detect		
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CIRCLE NO. 47

battery's remaining charge and charge rate. The converter performs this battery management using a mechanism based on a standard that Intel and Duracell proposed.

To facilitate design efforts, the device comes with 32 kbytes of on-chip flash memory. The memory saves time and money by eliminating the need for either component swaps or an external, nonvolatile memory device for keyboard BIOS storage. After you debug the code, you can replace the flash memory with less expensive mask ROM or one-time-programmable (OTP) memory (H8/3437). Along with Hitachi, Cygnus Support and Green Hills Software offer a set of hardware- and software-development tools, including an in-circuit emulator, a C compiler, an assembler, and a simulator/debugger. The flash and OTP versions of the IKAP-II cost $36 and $23.75 (25,000), respectively.—by Markus Levy

Hitachi America Ltd, Brisbane, CA, (800) 285-1601, ext 21. **Circle No. 486**

VITA considers 320-Mbyte/sec packet bus

A task group of VITA (VFEA International Trade Association) has begun defining the electrical and mechanical layers for Skychannel transfers across the VME P2 backplane. Skychannel is a 64-bit, 320-Mbyte/sec packet bus, which Sky Computers developed and proposed to VITA as a standard VMEbus interface. Designed for large multiprocessor systems, it provides 16 terabytes of globally shared memory.

—by Gary Legg

Sky Computers Inc, Chelmsford, MA, (508) 250-1920. **Circle No. 487**

Feature-packed 80C51-type μC includes 10-bit ADC

The Philips 8XC576, an 80C51 derivative, is a highly integrated controller with a Universal Peripheral Interface and an ADC with 9-bit accuracy. The IC's designers reduced the parts' irradiated noise to ease compliance with FCC standards. Though the IC's EMI/RFI emissions depend on the application, the company claims that the 8-bit μC has reduced emission more than 20 dB in some designs. Additional features include: 8 kbytes of ROM/ EPROM, 256 bytes of RAM, three 16-bit counter/timers, a programmable counter array, an on-chip watchdog timer, analog comparators, enhanced UART, two PWM outputs, power and oscillator failure detection, user-programmable outputs, and Schmitt trigger inputs. You can order the IC in two versions: 83C576 with ROM and 87C576 with EPROM or one-time-programmable ROM. Packaging options include 40-pin DIPs and 44-pin LCCs and QFPs. $4.90 (5000).

—by Anne Watson Swager

Philips Semiconductors, Sunnyvale, CA, (408) 991-5207. **Circle No. 488**

Modem chips ease international compliance

Recognizing that the telephone systems of many nations differ in their connection, signaling, and electrical requirements, Cirrus Logic has created the CL-MD1414UN modem chip-set series. These devices use external controller software to conform to country-specific signals such as dial tone, busy, and ring. They also handle special requirements, such as call-progress monitoring and blacklisting.

The modem chip sets comprise a memory device and two additional parts: a DSP and a sigma-delta analog front end. Code for the DSP resides in the memory, which can be flash, EPROM, or ROM, and controls the set's compliance to a country's standards. Cirrus offers code for France, Germany, the United Kingdom, and Japan.

The devices provide a 14.4-kbps data throughput and support V.32bis, V.42 error correction, V.42bis data compression, and all fallback data modes. The family has two members: a universal version (MD1414UN) and one with an on-chip PCMCIA interface (MD1414- UNP). The devices cost $50 (1000) each, and samples will be available in August. The company has scheduled production for September.

—by Richard A Quinnell

Cirrus Logic, Fremont, CA, (510) 226-2037. **Circle No. 489**

Audio ICs employ DSP

Expanding its PC chip-set business into peripheral devices, Opti Inc is introducing a series of ICs for audio and communications control. The series includes a 16-bit audio controller, a 32-bit audio and communications controller, and a DSP engine for wave-table audio synthesis. Opti's Media Chips subsidiary designed all three devices, which are sampling now.

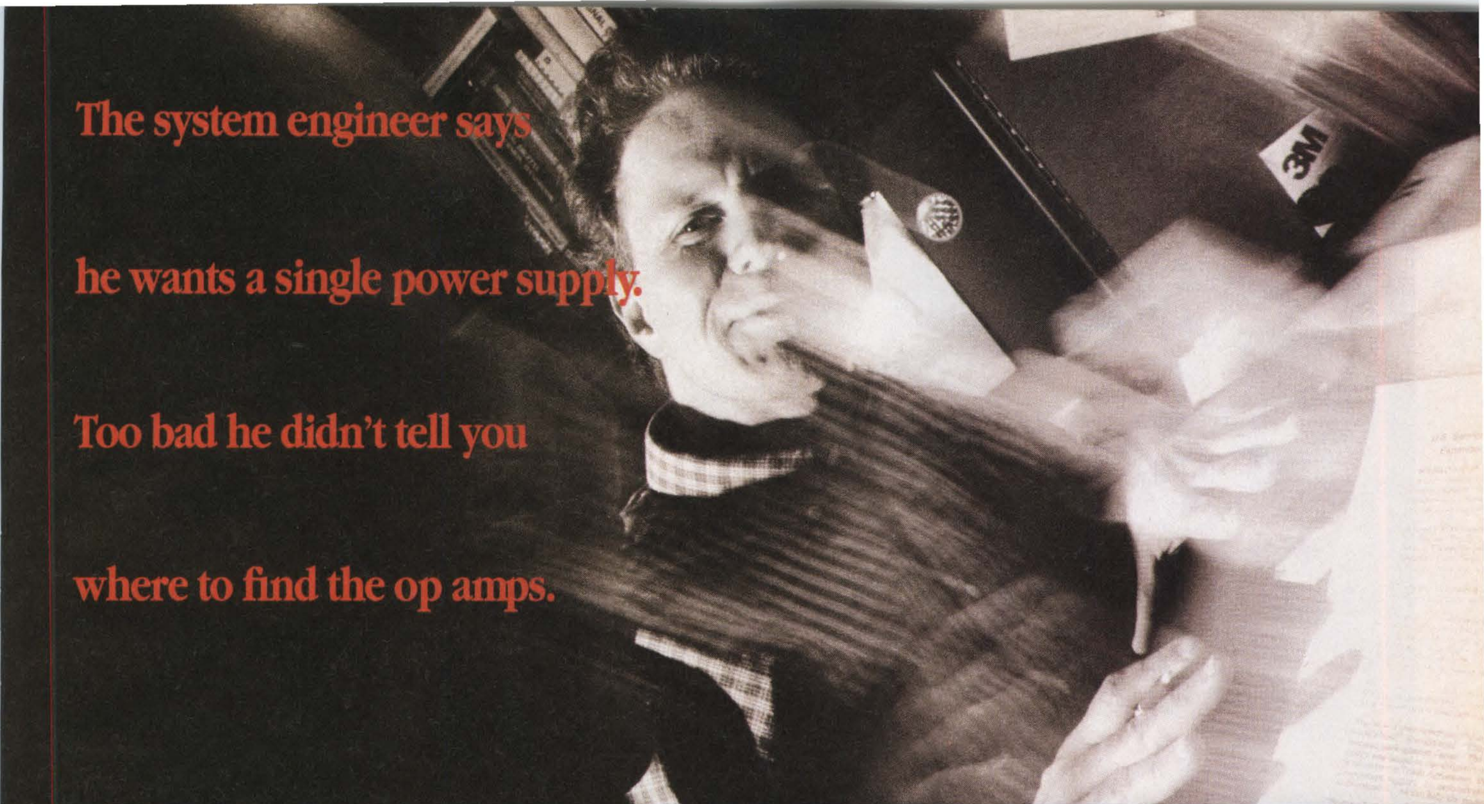
The 82C929 16-bit audio controller ($11) provides a Sound Blaster- and Windows Sound System-compatible digital audio processor, along with interfaces to the MPU-401 and OPL2/3/4 audio synthesizers. The device also includes ISA bus and CD-ROM interfaces with enough drive capability to eliminate the need for buffers. The device offers software-programmable address, IRQ, and DRQ registers, allowing a jumperless design, and has several power-down operating modes to facilitate battery operation.

The 82C950 ($42) DSP-based audio and communications processor operates with AT&T's DSP3207. The processor provides entertainment and business audio capability using wave-table synthesis. It also provides audio communications functions, including telephony, 14.4-kbps fax/modem, speaker-phone, speech-I/O, and audio-encoding/decoding functions. The software-programmable CD-ROM interface allows the device to handle a variety of standard and proprietary interfaces.

The 82C940 ($35) comes with two ROMs and provides wave-table synthesis for music and sound generation. It produces 32 simultaneous voices with a 256-level attack-decay-sustain-release envelope. It also offers independent left- and right-channel volume control, a 4-level pedal sensitivity, and frequency interpolation. The device uses compressed audio samples in its wave table, allowing its internal 2-Mbyte sample RAM to hold the equivalent of 8 million samples.

—by Richard A Quinnell

Opti Inc, Santa Clara, CA, (408) 980-8178, ext 850 **Circle No. 490**



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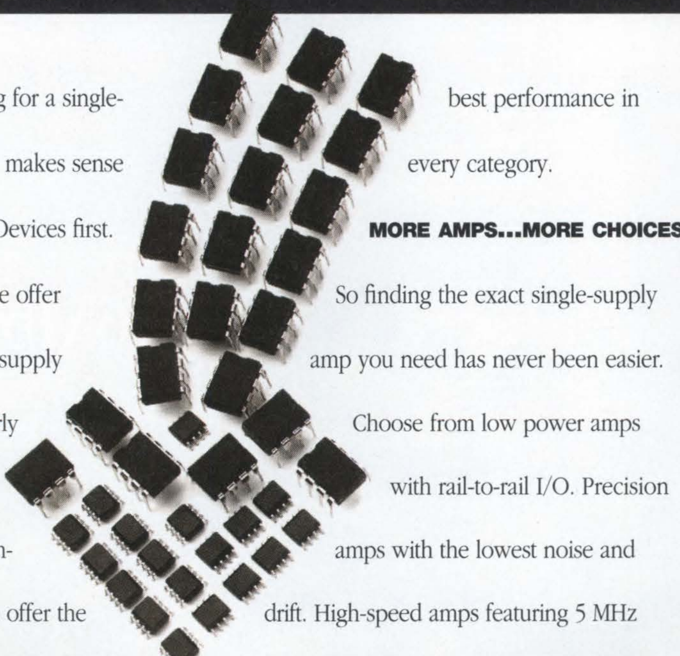

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	Single	Dual	Quad					Input	Output	(μV)	(nV/√Hz)	(mA)	(mA)	(MHz)	
OP	113	213	413		•	•	•			75	4.7	±40	1.75	3.4	Lowest noise and drift
OP	183	283		•	•	•	•			1000	10	±25	1.5	5	5 MHz from +3 to +36V
OP	90	290	490	1.6	•	•	•			150	60	+13/-7	0.015	0.02	Precision micro power
OP		291	491		•	•		•	•	700	21	±10	0.35	3	Low power R-R I/O
OP		292	492		•	•	•			800	15	±8	1.4	4.5	Low cost
OP		295	495	•	•	•	•		•	300	45	±18	0.15	0.075	Accuracy and output drive
AD	820	822		•	•	•	•		•	400	16	±30	0.8	1.9	FET Input
SSM		2135			•	•	•			1000	4.7	±40	1.75	3.5	Excellent for audio
AMP04					•	•	•			150	25	±15	0.7	0.3	Easy-to-use +5V inst. amp
AD626				•	•	•		>		250	250	15	0.23	0.1	Low cost diff. amp

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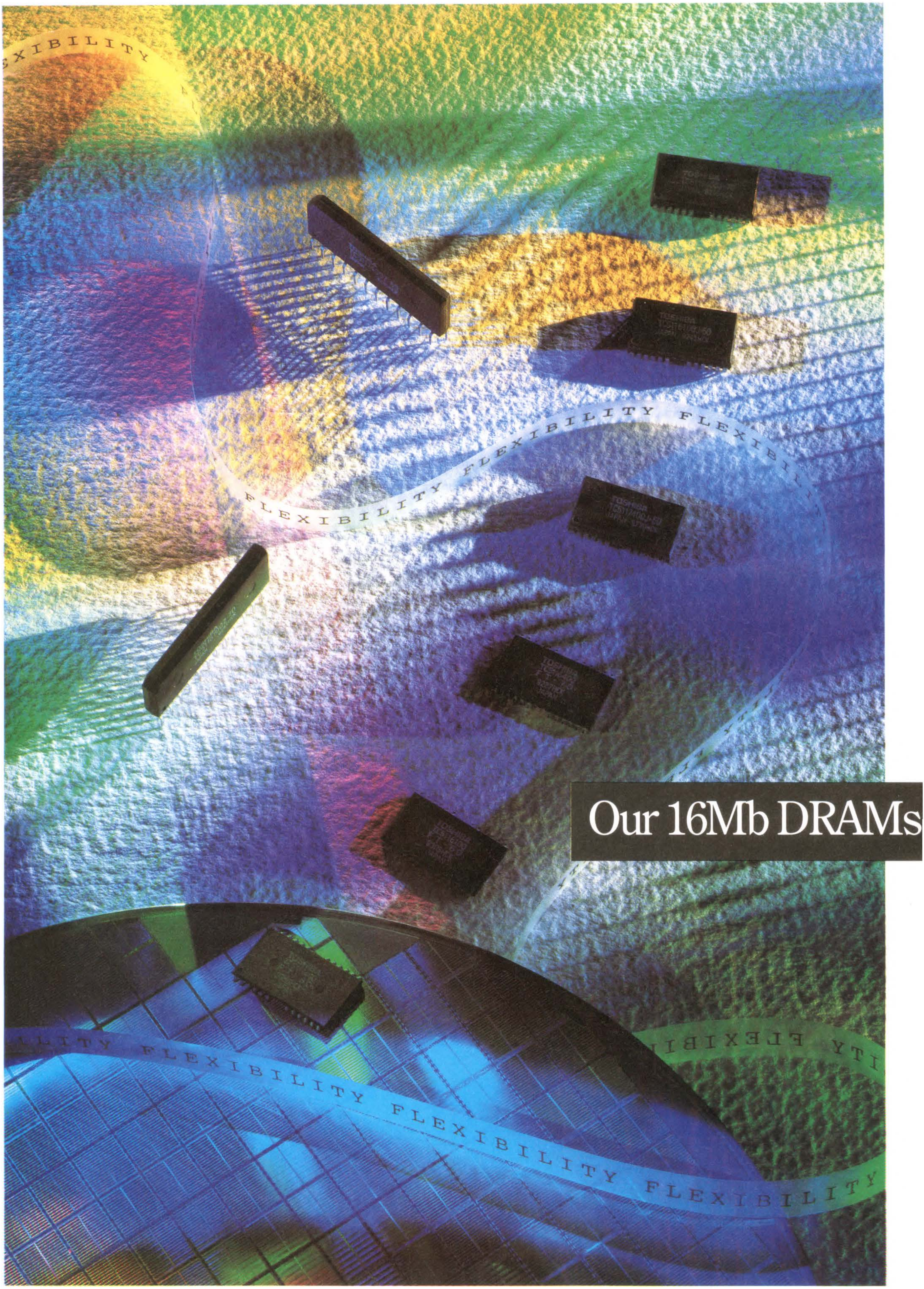
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Different spin on background debuggers

Jim Hebert's "Internal debuggers simplify µP pc-board verification" (May 12, 1994, pg 103) sidestepped one important issue: Background debuggers don't really do a lot!

When debugging a real-time embedded system, you need more than the ability to set a few simple breakpoints. Without trace, for example, you can never see how an interrupt-service routine works without stopping the code, which dramatically alters its operation. Without complex breakpoints, you cannot stop on IF-THEN conditions or on writes and reads of specific data. A real ICE (in-circuit emulator) offers a wealth of features designed to speed debugging.

Frankly, I'm a little puzzled by recent trends in development tools. Emulator costs are decreasing (10 years ago, $20,000 was the norm; now, $5000 to $10,000 is more typical), and projects are becoming more complex. Yet, too many engineers opt for these low-cost, minimal-functionality tools. An engineer is an expensive asset: Doesn't it make sense to invest in decent tools that radically reduce debugging time?

Jack G Ganssle, President
Softaid
Columbia, MD

CEBus is sound alternative

I enjoyed "Industrial buses: Network vendors agonize over fieldbus standard" (April 28, 1994, pg 45). However, I was surprised to see the EIA IS-60 (CEBus) missing from the article. This bus provides a low-cost alternative to the buses covered in the story. There are now several large manufacturers backing this standard as well as a wave of new products that incorporate it.

The CEBus provides support for twisted-pair, power-line, IR, RF, coax, and fiber-optic media. It implements a streamlined 5-layer version of the ISO/OSI 7-layer model. It is an open standard and is easily incorporated into systems with low-cost 8-bit µPs. Support for the lower layers of the standard is available in module or chip form. Implementing CEBus devices is easy with a low-cost development system that generates code from your specs and lets you incorporate functions written in C.

I was especially intrigued by the prices listed for Echelon's LonWorks. Our company manufactures a line of industrial controllers that communicates over the CEBus power-line physical layer to implement a distributed-control network. Many of our customers have indicated that their choice of CEBus was due, in part, to the royalties and high development costs associated with LonWorks. Customers have reported product royalties of 5 to 8× the quoted node cost and development-system costs 3 to 4× higher. Perhaps this situation has changed recently.

Overall, the article was informative and timely. It is becoming increasingly important to provide some sort of "fieldbus" to control costs and improve quality. Thank you for making this information available to your readers.

Steven J Ackerman
Ackerman Computer Sciences
Sarasota, FL

More on OOP and diagrammatic programming

I enjoyed Charles H Small's "Diagrammatic programming" (January 6, 1994, pg 61). I work on hardware conception, and I often write small quick-and-dirty programs to test my ideas, which are becoming more and more soft (Xilinx). I cannot wait for a "software specialist" to write that sort of software. Sometimes, I have to write a piece of software that's quite complex. For example, three years ago, I was unable to manage "entities" in a graphic piece of software; Borland released the first OOP (object-oriented programming) Pascal version around this time. Because I had little experience with OOP, I transferred my entities into simple "objects" and got great results.

Because things are changing so quickly, I thank you for the articles that keep us informed and up-to-date.

Hubert Cros
Société Générale Castres
Toulouse, France

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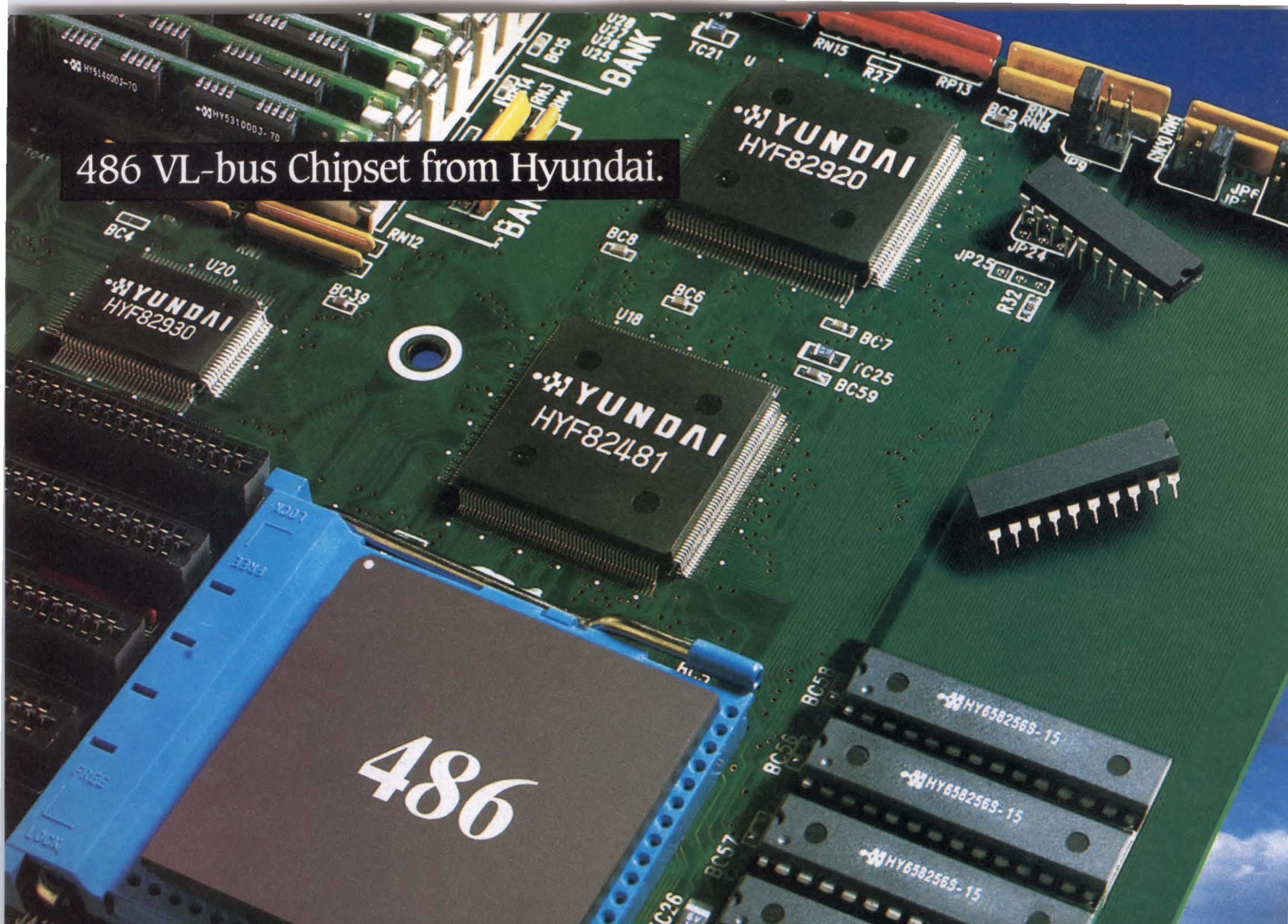

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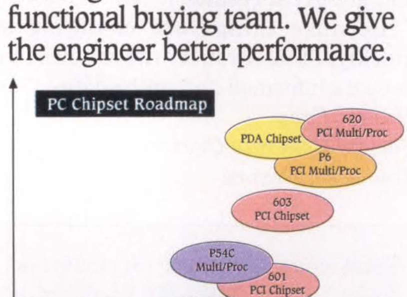

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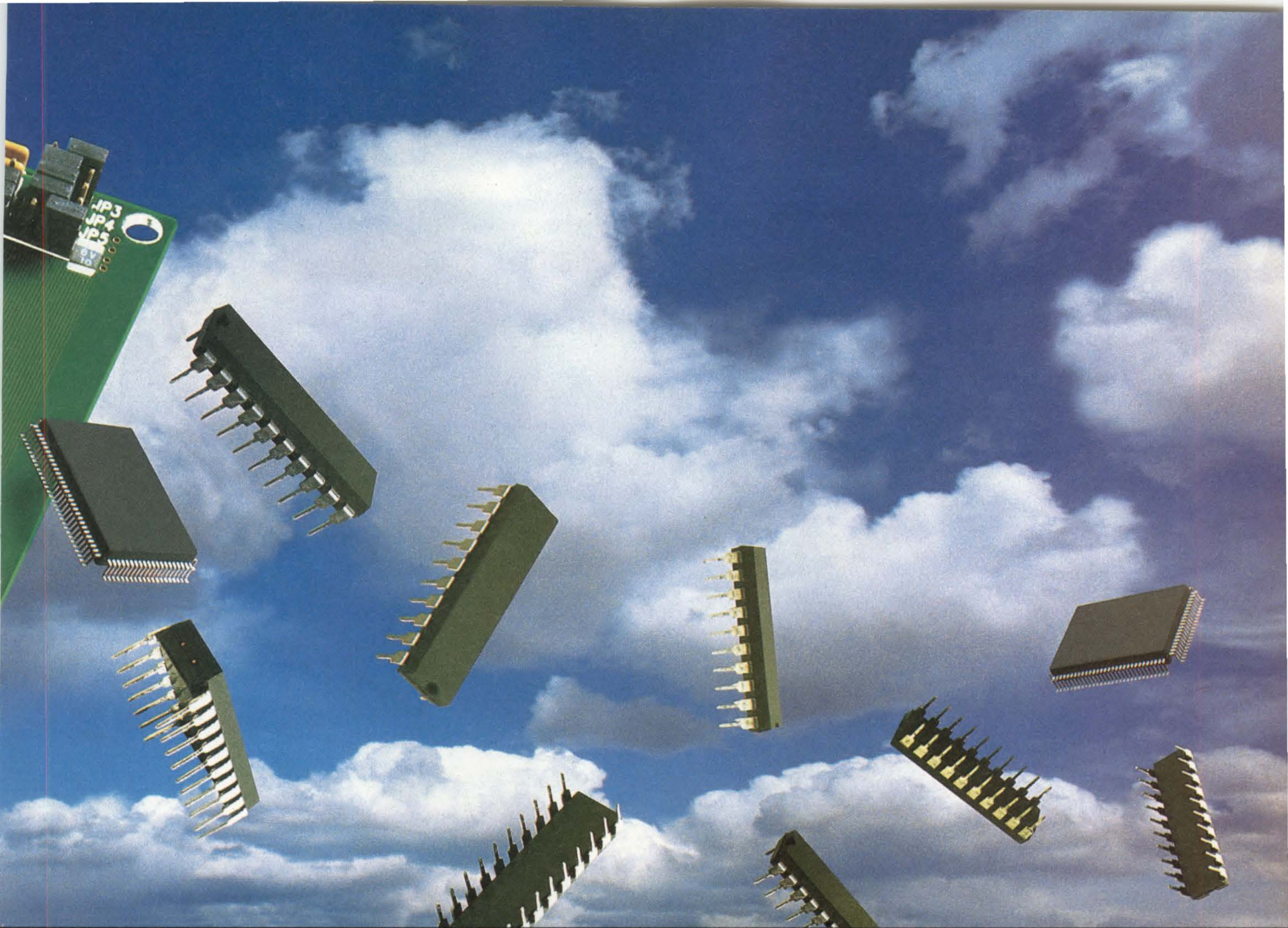

Without Glue.

chipset, the HYF82481, the HYF82920 VESA Controller, and the HYF822930 Address Buffer. The chipset supports 386DX, 486SX/DX/DX2/DX4 and P24T CPUs with external clock speeds up to 50 MHz, and up to 3 VESA local bus master slots. Cache sizes can range from 32K to 1M, in selectable write-through or write-back configurations. The chipset currently supports up to 64MB of memory, in 4 banks of 256K, 1M, or 4M DRAM.

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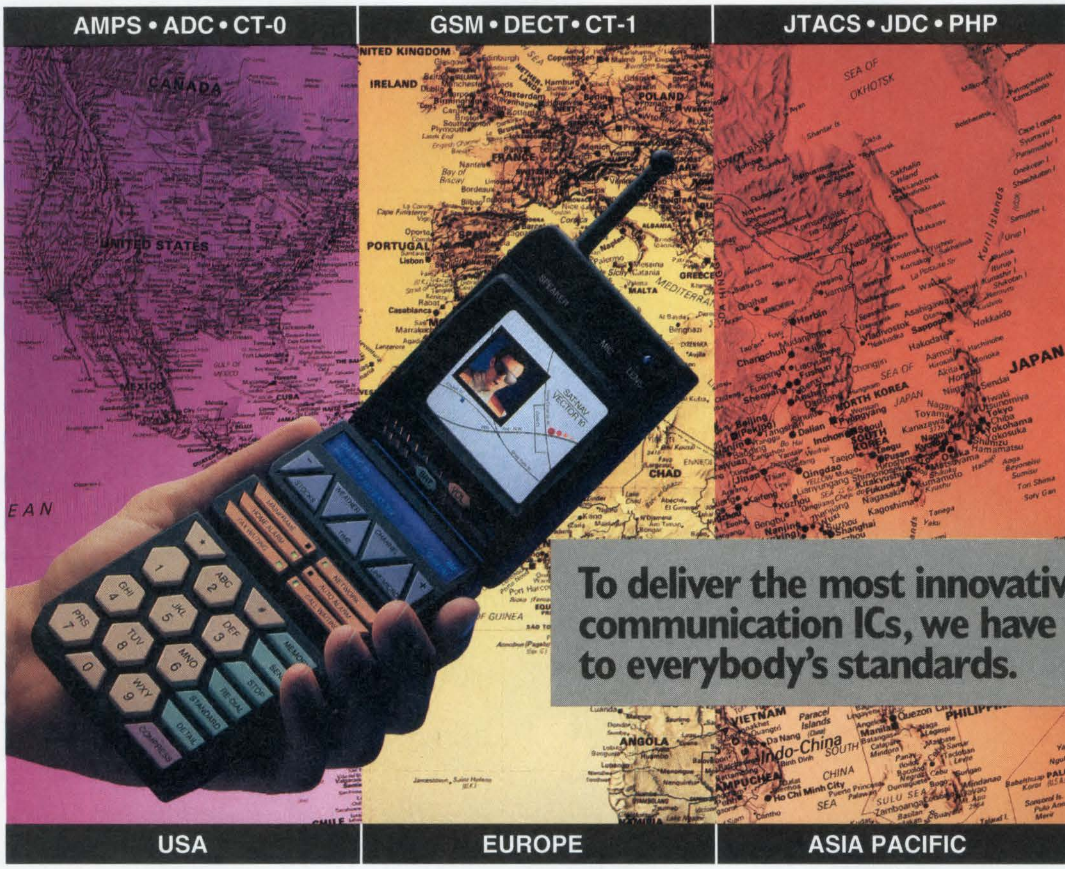

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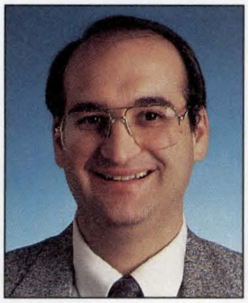

The latest marketing figure of merit for μPs, MIPS/W, is a poor figure of merit, and we should dump it now. It's not like miles/gallon. I know of no engineers who actually select μPs based on a MIPS/W rating. That's because the single figure of merit masks two important figures of merit that you really want to know: processing power (expressed in million instructions per sec at a certain clock rate or some other way) and power dissipation (expressed in watts).

Whenever you see a figure of merit that masks important characteristics, you have to wonder what the vendor is hiding. Now, maybe the group that cooked up MIPS/W was really looking for a way to simplify the task of selecting a μP, but I'm jaded enough to believe that something darker was afoot.

If I had a very low-power μP that didn't run very fast, I'd probably be very interested in a figure of merit like MIPS/W, too. Similarly, if I built a screamer of a μP that could fry eggs to boot, my processor's MIPS/W rating would look OK. Further, it has become well-known that you can greatly enhance your MIPS/W rating if you rate the processor at impossibly low capacitive loading levels. These "cooked" ratings serve only to mislead.

In the real world, applications have a certain amount of processing to do and a certain amount of power available. Those two parameters define the solution space and a set of processors that can do the job. The single MIPS/W rating does not tell you whether a processor falls within that solution space.

While you can sound hip and knowledgeable by using New Age figures of merit, such as MIPS/W, you don't get any closer to a good design.

Steven H Leibson
Editor-in-Chief

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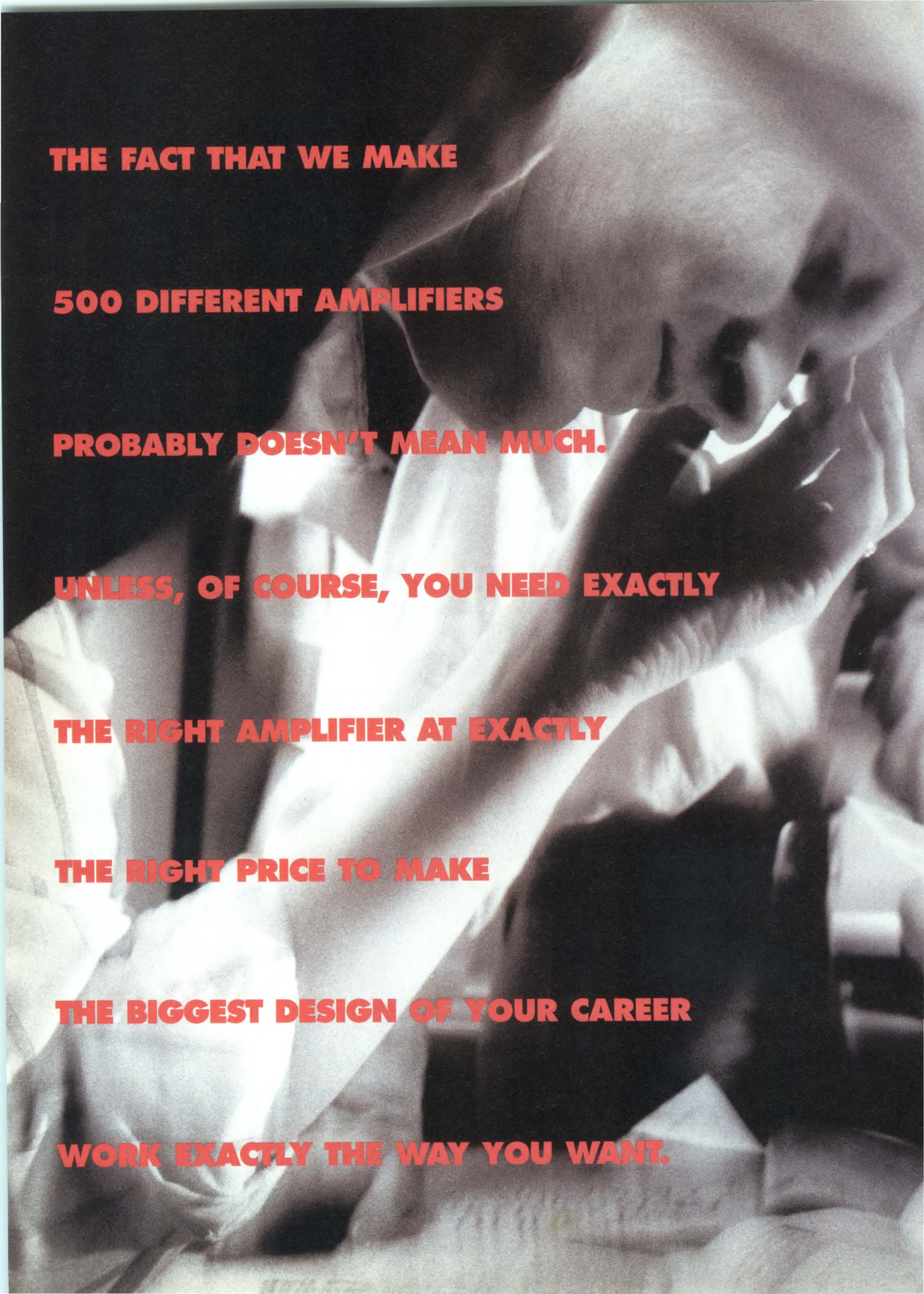
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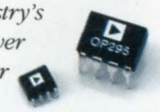

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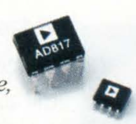

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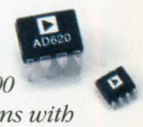

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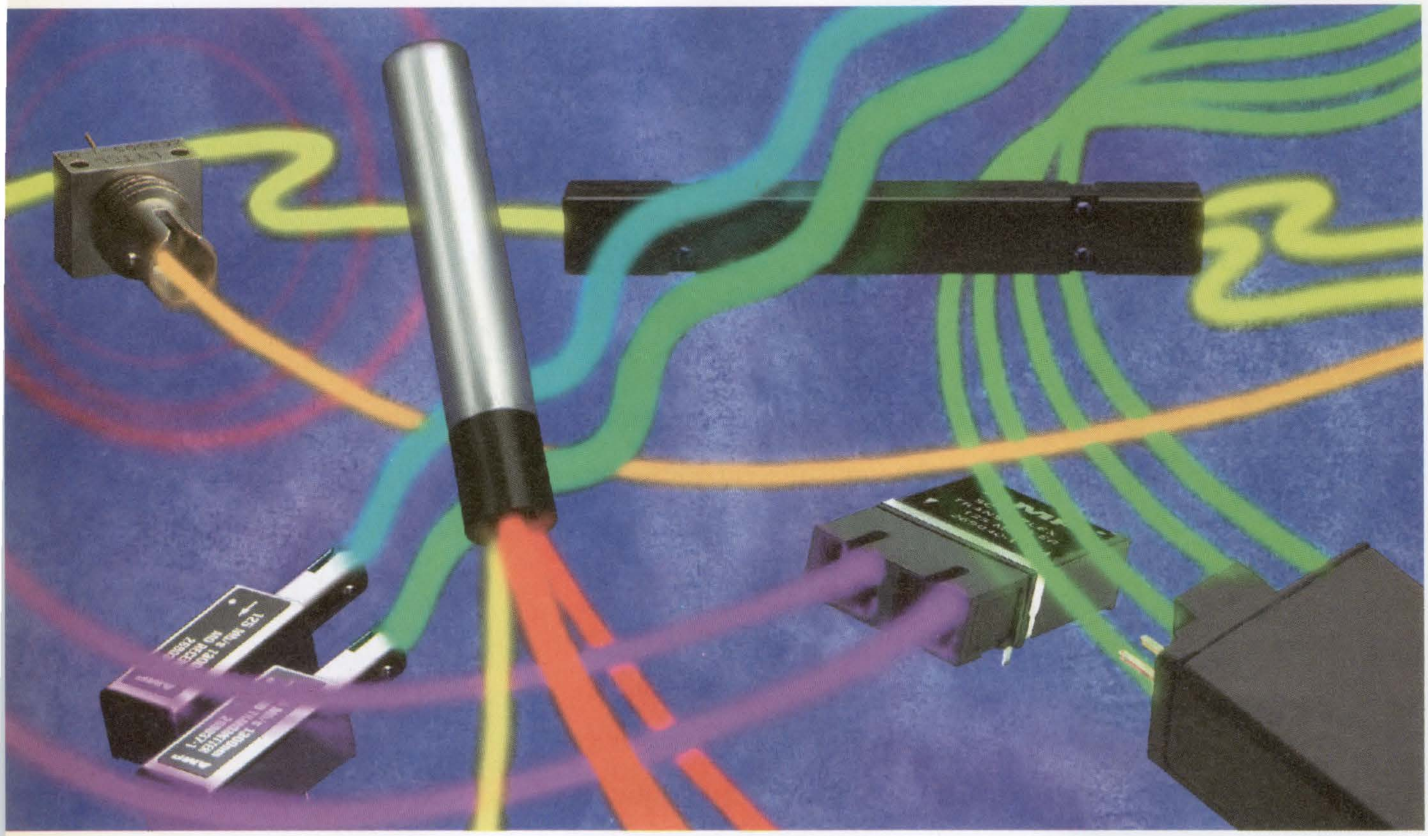

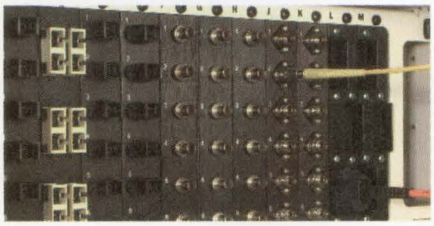

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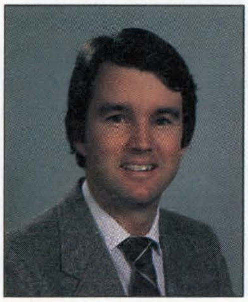
CIRCLE NO. 26

Three DSP RTOSs are ready to merge with Windows

DAVID SHEAR, Technical Editor



DSP-based virtual subsystems allow common hardware to assume many identities.

In an ideal world, all Windows applications would work with all available hardware. Further, Windows applications would be able to take advantage of DSPs and their real-time operating systems (RTOSs). You could design a DSP-based subsystem that would provide different functions to different applications simultaneously.

When you came up with a new and improved DSP-based device, existing applications could start using it as soon as it was installed. You would not have to supply different drivers for each application or be forced to "emulate" a competing product because more applications support it.

This ideal is not yet reality, but Microsoft and DSP RTOS vendors are working toward it. The first step in reaching this goal is to create a standard method for Windows-based applications to interact with DSP-based hardware. According to Microsoft, the company's proposed DSP resource-manager interface (RMI) "provides Windows applications access to DSP board hardware. The DSP interface is message-based and defines a common structure for messages and a programming model for communication between host device drivers and their corresponding DSP tasks."

Much of the beauty of Windows is that it isolates hardware from software. Windows applications make calls to subsystems via high-level application programming interfaces (APIs). Drivers within the API perform error-checking and translation functions on the messages and then move the messages between the application and the hardware.

Today, the APIs interact with hardware-specific drivers that directly control the hardware. The hardware can be DSP-based and still work within this framework. In fact, many modems and sound cards are moving to DSP-based designs. But when you wish the DSP to take on more than one function at a time, this approach falls short.

For example, a PC user may want to listen to MIDI background music, while receiving a fax, while inputting voice data into a spreadsheet, and while the PC is converting a voice-mail message into text-based electronic mail. You can do all of this today, but you need a separate subsystem for each task.

The DSP RMI provides another layer in the software architecture. This layer isolates the DSP hardware and allows a single DSP-based board to perform multiple tasks (**Fig 1**). When an application requests a DSP-based function, the DSP RMI interacts with the RTOS on the DSP hardware. The RMI first determines if the new DSP function fits within the unused resources of the DSP board. It then loads the new function and handles the messages between the application and the DSP.

This extra layer of isolation allows Windows-based applications to work with any DSP hardware that conforms to the DSP RMI standard. The message-based DSP interface defines common structures and a

DAVE CUTLER

DSP RTOSs

programming model for communication between host device drivers and their corresponding DSP tasks.

The DSP driver is responsible for loading the DSP RTOS and DSP task to the hardware. Once the task is running, the DSP driver moves data and messages between the host PC and the DSP board. The DSP driver on the host and the DSP RTOS on the DSP hardware are not aware of the content of the messages and data. They just ensure that the multiple data and message streams get to the correct device driver on the host and to the appropriate task on the DSP hardware.

Three DSP RTOSs are working toward this model: VCOS from AT&T, Mwave from IBM, and Spox from Spectron Microsystems. VCOS works with AT&T's DSP3200 family of 32-bit floating-point DSPs. Mwave works with the IBM's Mwave 16-bit fixed-point DSPs. Spox works with Analog Devices' 2100 family of 16-bit fixed-point devices and 21000 family of 32-bit floating-point devices, Motorola's 56000 family of 24-bit fixed-point devices and 96000 family of 32-bit floating-point devices, and Texas Instruments' TMS320C5X family of 16-bit fixed-point devices, and TMS320C3X and TMS320C4X family of 32-bit floating-point devices.

Though these DSP RTOSs are true multitasking operating systems, they operate in an environment different from that of a typical embedded system. In a typical real-time system, you have awareness of the tasks the system must perform, how often the tasks must run, and the required completion times of the tasks. When designing the system, you use a method that meets the needs of the system. In many cases, a simple round-robin scheduler is enough. At other times, you select multiple priority levels and use a preemptive scheduler.

In the Windows/DSP case, on the other hand, you don't have this awareness. You can't predict which tasks the DSP will run and what the required priorities will be. For example, the DSP may be providing just a single function, such as a modem, or several simultaneous functions, such as a modem, compression, fax, and text to speech. You cannot predetermine the mix.

Therefore, it is critical that the DSP RMI accept only those tasks that can work together. The DSP RMI must also guarantee that the tasks operate in a fashion that ensures that each task continually meets its start and completion times.

Each of the three DSP RTOSs addresses this requirement in a different way. All three share in requiring that each function must have a header. This header provides the worst-case cycles the function requires, the completion time, the memory requirements, the rate of execution, and other data the DSP RMI requires to fully characterize the function.

When an application requests a function from the DSP RMI, the DSP RMI evaluates the header file, checks what is already running on the DSP, and then informs the application if the new function can fit within the remaining resources of the DSP. If the function can't fit within those resources, the application must tell the user that other DSP-related applications must first be turned off. This graceful failure mode ensures that the applications don't swamp the DSP.

Two basic types of tasks are available: real-time and nonreal- time. Real-time tasks are those that have hard start and completion times, such as fax and modem functions. A fax function's inability to receive incoming data will adversely affect communication.

Nonreal-time tasks are those that can wait some amount of time; their completion times are not hard. Functions such as JPEG still-image compression and V.42 bis compression can work as nonreal-time tasks. It won't be long before some clever programmers realize that a DSP within a PC makes a wonderful coprocessor. By having access to the

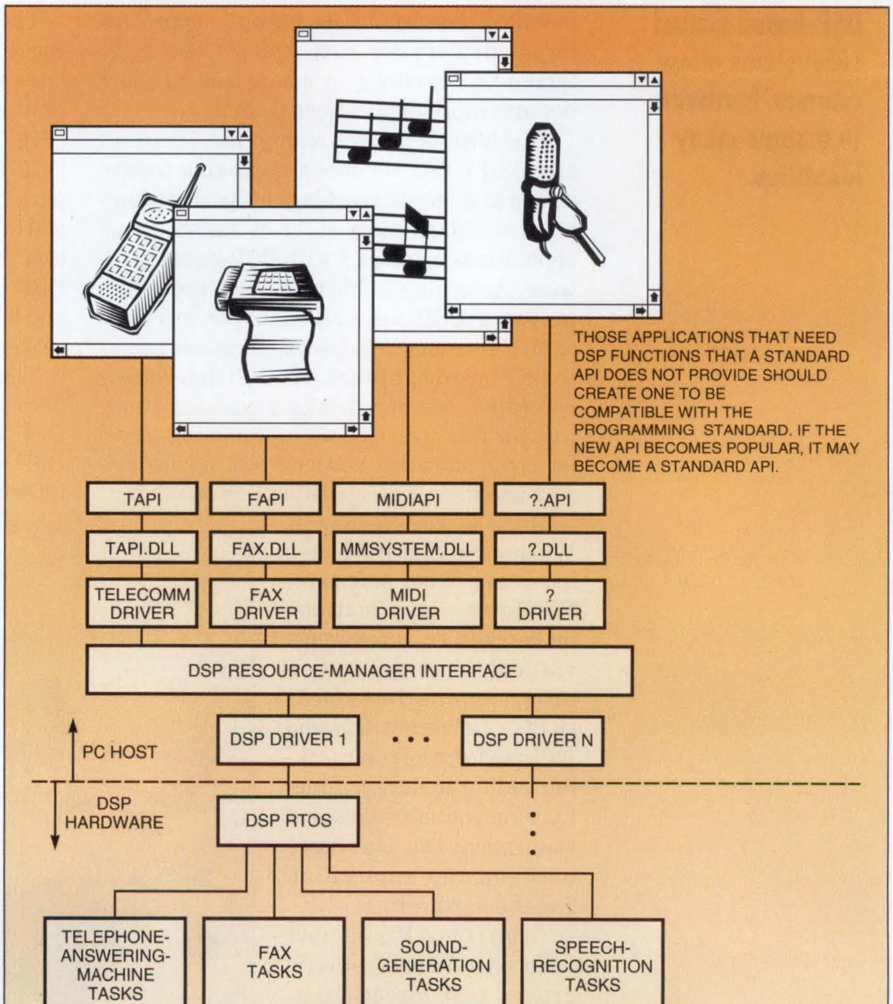


Fig 1—The proposed interface between a Windows-based application and the DSP hardware provides layers of drivers to isolate the application from the hardware. Thus, an application could run on different DSP hardware without modifications.

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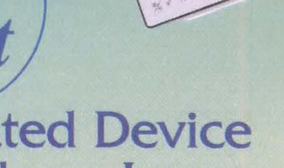

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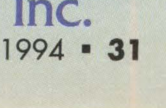

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CIRCLE NO. 4

DSP RTOSs

DSP on a nonreal-time basis, these programmers will use leftover DSP cycles without impacting the real-time tasks.

Each DSP RTOS is using a different method to provide resource management and ensure that as much of the DSP's resources are available as possible (**Fig 2**). AT&T's VCOS uses a frame-based block-processing method. Each frame is a unit of processing time. You can choose any period, but 10 msec is typical. VCOS executes each task on the real-time execution list once every frame. Nonreal-time tasks execute during the frame time the real-time tasks do not use.

When developing a function for VCOS, you have to partition your code into pieces that fit within the model. A single task cannot take longer than the period of the frame. You must break your tasks into smaller chunks, so that they not only fit within the frame, but also leave enough time for other tasks to run.

Mwave uses a kernel that comprises a preemptive dynamic deadline-scheduling algorithm. A periodic interrupt suspends operation of a task and provides control to the kernel. The kernel then determines which task should next run. The task it selects is the one whose start time has arrived and whose deadline is earlier than that of any other task.

You can see Mwave's dynamic-scheduling nature by looking at the linear multitasking plots at the bottom of **Fig 2**. The order of task execution changes as each of the tasks interacts with the scheduler. In effect, Mwave dynamically arranges the priorities of each task at each time tick.

Mwave also implements a cycle counter to verify that each task stays within the header's processing requirements. If a task runs past its maximum cycle count, Mwave posts an error to the Mwave manager with a pointer to the current task. If the designer of the task miscounted the maximum cycle count,

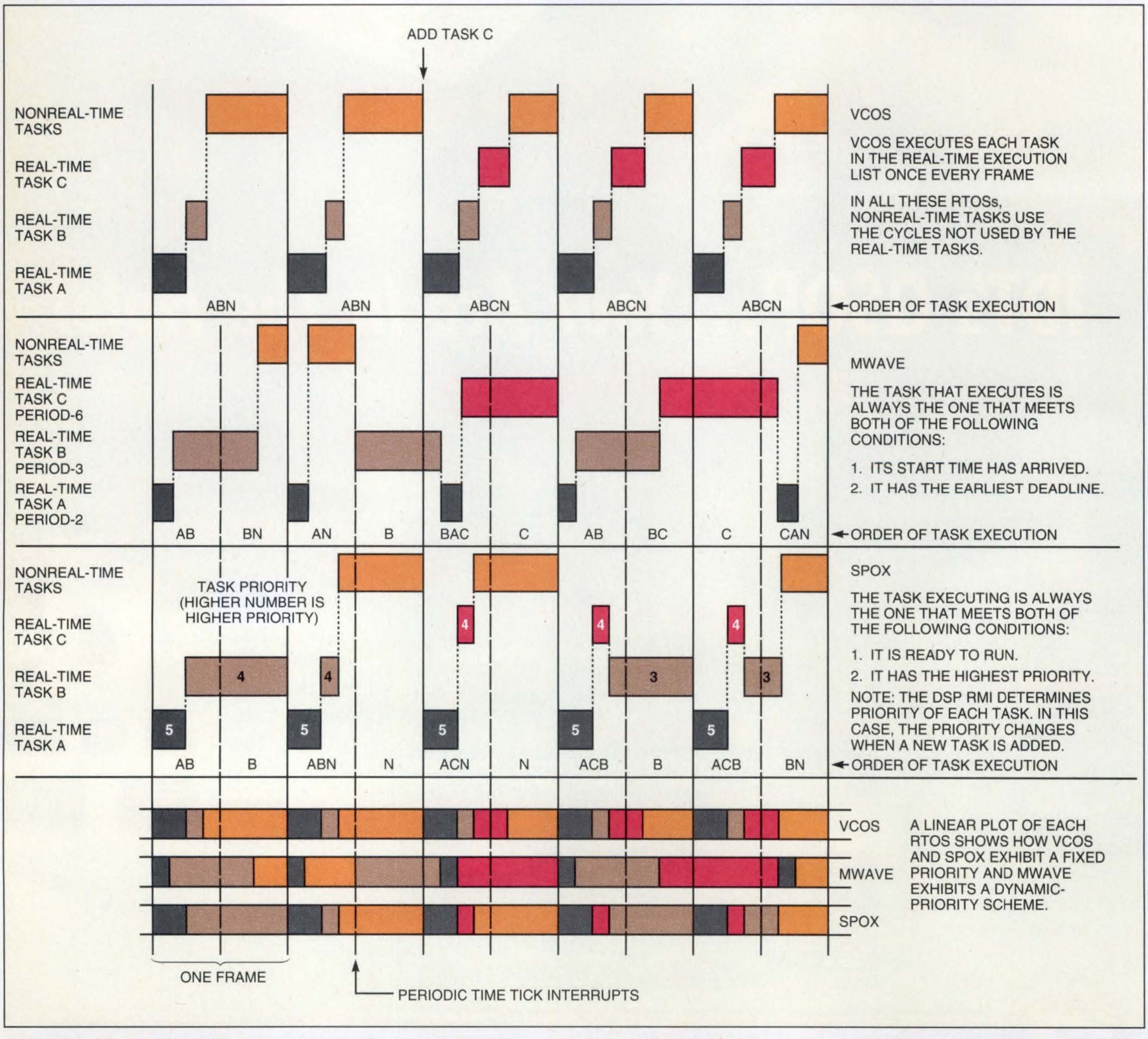

Fig 2—The three DSP RTOSs use different scheduling methods to ensure that the DSP hardware executes each task within its required time constraints.

DSP RTOSs

Mwave identifies the offending task.

Spox is a full preemptive multitasking RTOS for general-purpose embedded-system use. For such an RTOS to work properly, you must assign each task an appropriate priority. As stated, a Windows/DSP system doesn't allow prediction of which tasks the DSP will run.

In this case, the Spox DSP RMI must assign the priorities to each task running on the DSP. Spox uses a rate-monotonic scheduling algorithm to assign appropriate priorities each time you add or delete a task. When you add or delete a task, the scheduling algorithm arranges the priorities of all tasks currently running on the DSP. As such, the absolute priority of each task may actually change as you add tasks to and delete tasks from the DSP.

As you develop DSP-based products to run in the Windows environment, you should minimize the amount of real-time tasks you use. The amount of real-time tasks each function requires is very important. A sloppily designed function might simply put all of its processing requirements in real time, consuming a valuable and often-limited resource.

Also, if you design a function so that there is a large difference between the worst-case cycle or memory requirement and the average for that function, then fewer real-time functions can run. The DSP RMI uses worst-case numbers to determine if a function fits within the DSP resource. If a function only rarely uses its worst-case numbers, the DSP RMI still reserves resources for it. Therefore, the DSP does not run at full capacity.

A well-designed function minimizes its real-time requirements and levels its real-time operation so that the worst case is close to the average. No one appreciates a function that hogs much of the DSP. On the other hand, one that only slightly impacts the valuable real-time resource allows many functions to run on the DSP at once. End users quickly learn which functions are properly designed.

The DSP RMI is still in the proposal stage but is expected to be a solid standard by the end of this year. In the end, everyone will benefit. It will give application developers access to new subsystem options. It will give users the ability to integrate new DSP-based products easily. And it will mean that designers have to create only one driver to run DSP-based products within Windows. EDN

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LOOKING AHEAD

The future for DSPs in the PC world is very bright. More and more, Windows applications will begin using virtual subsystems provided by one or many DSPs.

Detractors of DSP often say that if the DSP were so useful, it would already be on the motherboard. They also say that the host μP is getting so powerful it will be able to take on the DSP functions without requiring a separate DSP chip.

The response to these critics is: No, not many PC manufacturers have integrated the DSP onto the motherboard. But it doesn't make much sense yet. Some PC manufacturers have placed a DSP on the motherboard, but these are narrow-market PCs that require specific functions of the DSP.

There are just too many DSP options right now. You have not only many DSPs from which to choose, but also many system-design options. You may even wish to have more than one DSP to provide the horsepower you need.

Standard access to DSP-based boards is a major roadblock to their use. The upcoming DSP resource-manager interface is a step to remove this blockage. Also, applications that can use the power of the DSP are just beginning to emerge. Before the move to multimedia, the DSP had little reason to be in a PC.

Those who say the host μP will absorb the capabilities of the DSP just don't understand what a DSP really is. Placing a multiplier on a chip does not make a DSP. You also need complex multiple-function instructions for parallel operation, advanced addressing, multiple data paths both on and off the chip, and incredibly fast I/O data rates. Many DSP subsystems will have local buses to allow unimpeded access to their memory and I/O. Just trying to move data around the system at similar speeds would consume the resources of a host computer system.

But to see the hardware's future, look at the software. Many years of effort have gone into creating very fast and optimized code for use on DSPs. Even if the hardware were fast enough, it just doesn't make sense to recreate all of this effort to move the software onto the host μP.

Besides, few systems have more host processing power than they need. Sure, the processing power of the host may occasionally exceed the need—for a while. But software has a way of bringing hardware to its knees. The host μP will be busy enough just trying to keep up with what applications ask it to do, let alone take on what the DSPs provide.

Making Waves

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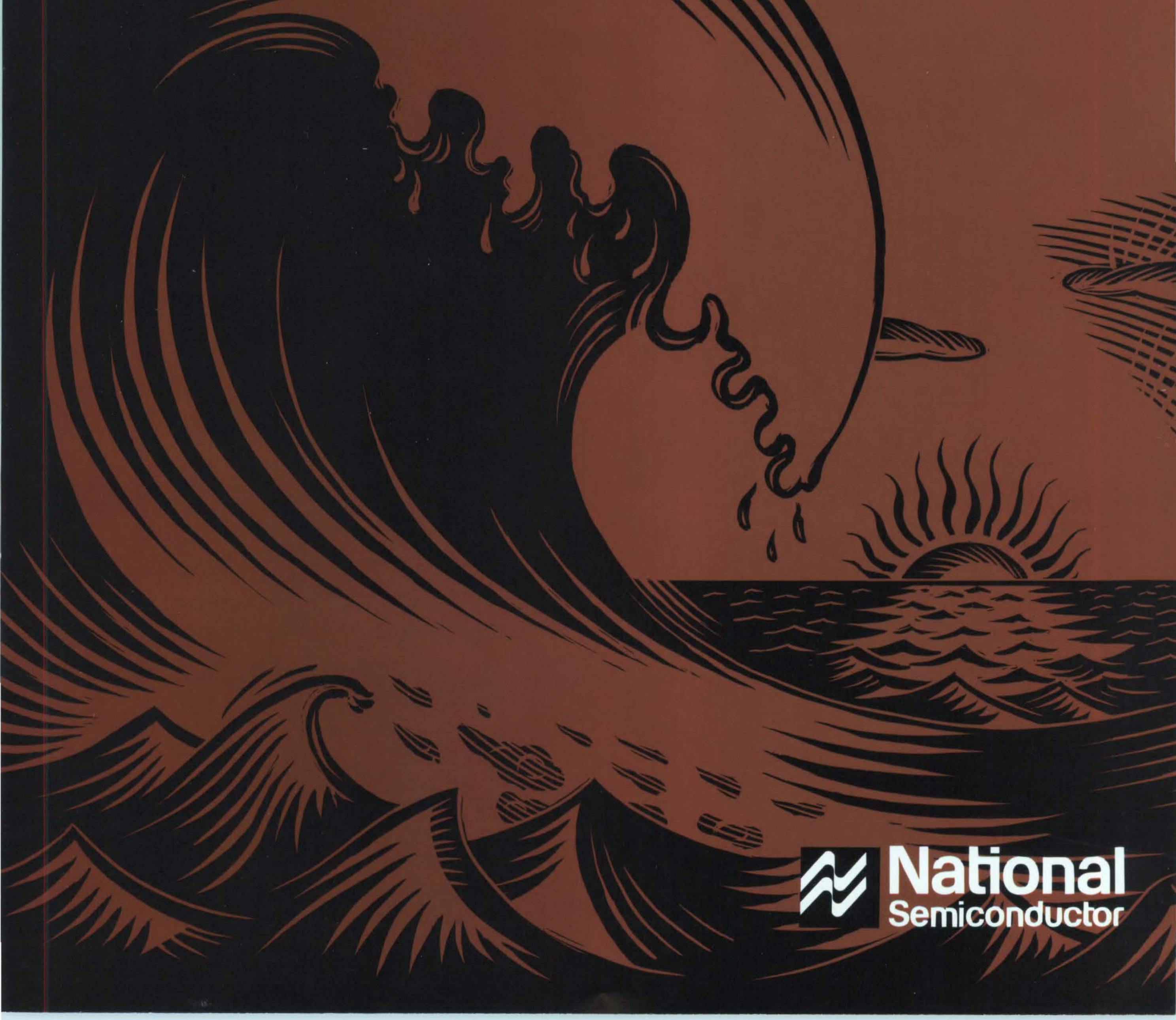

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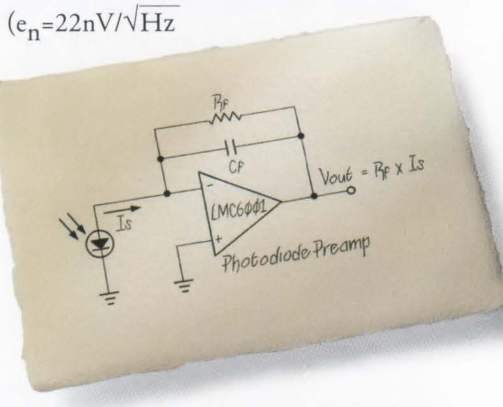

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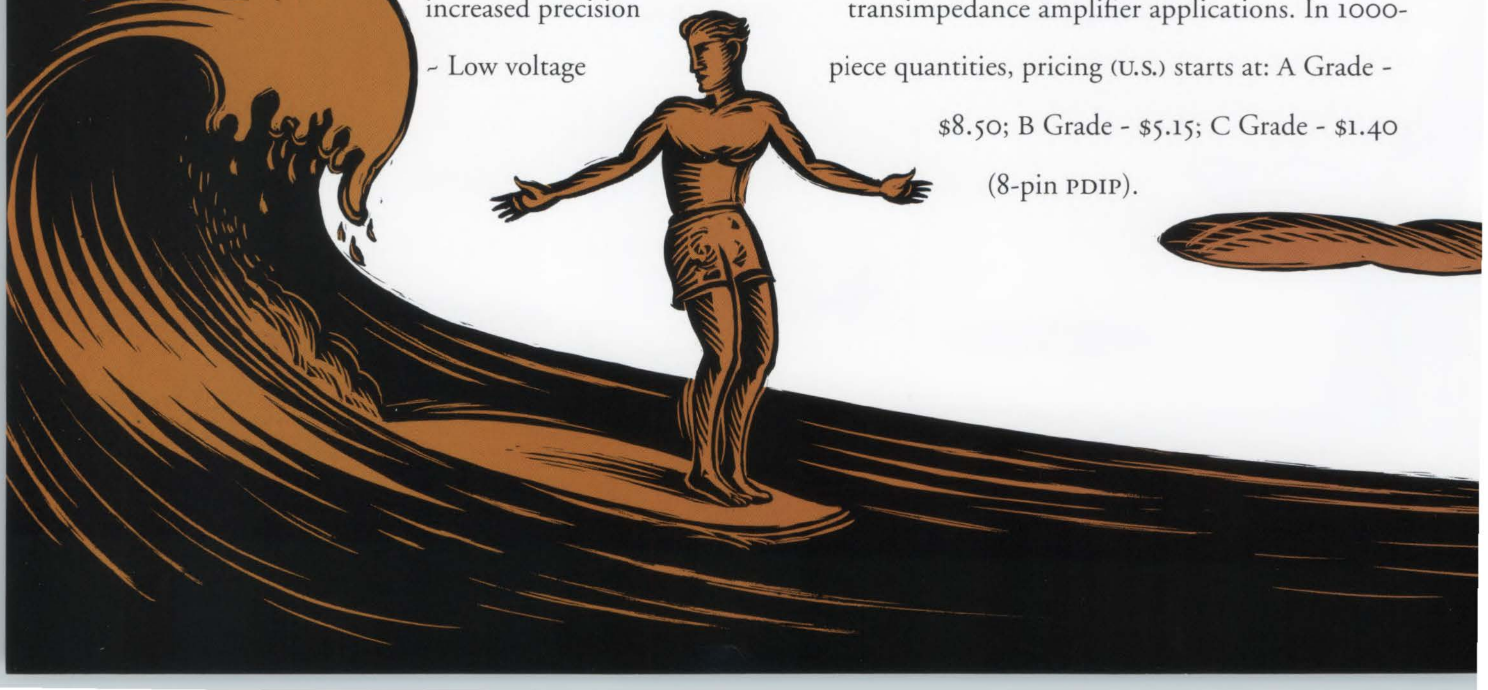

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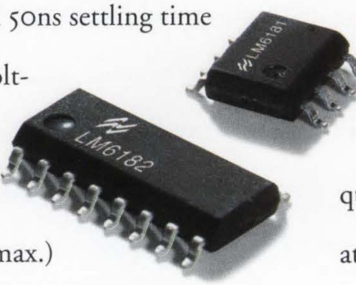

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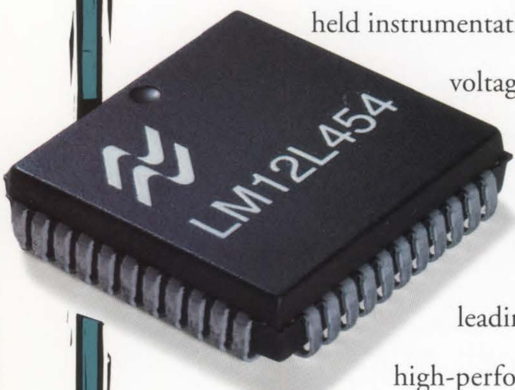
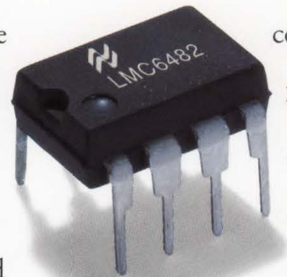
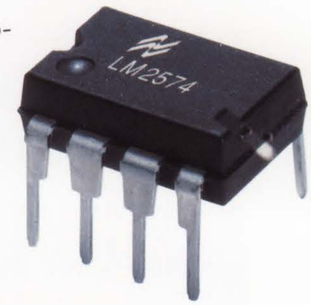
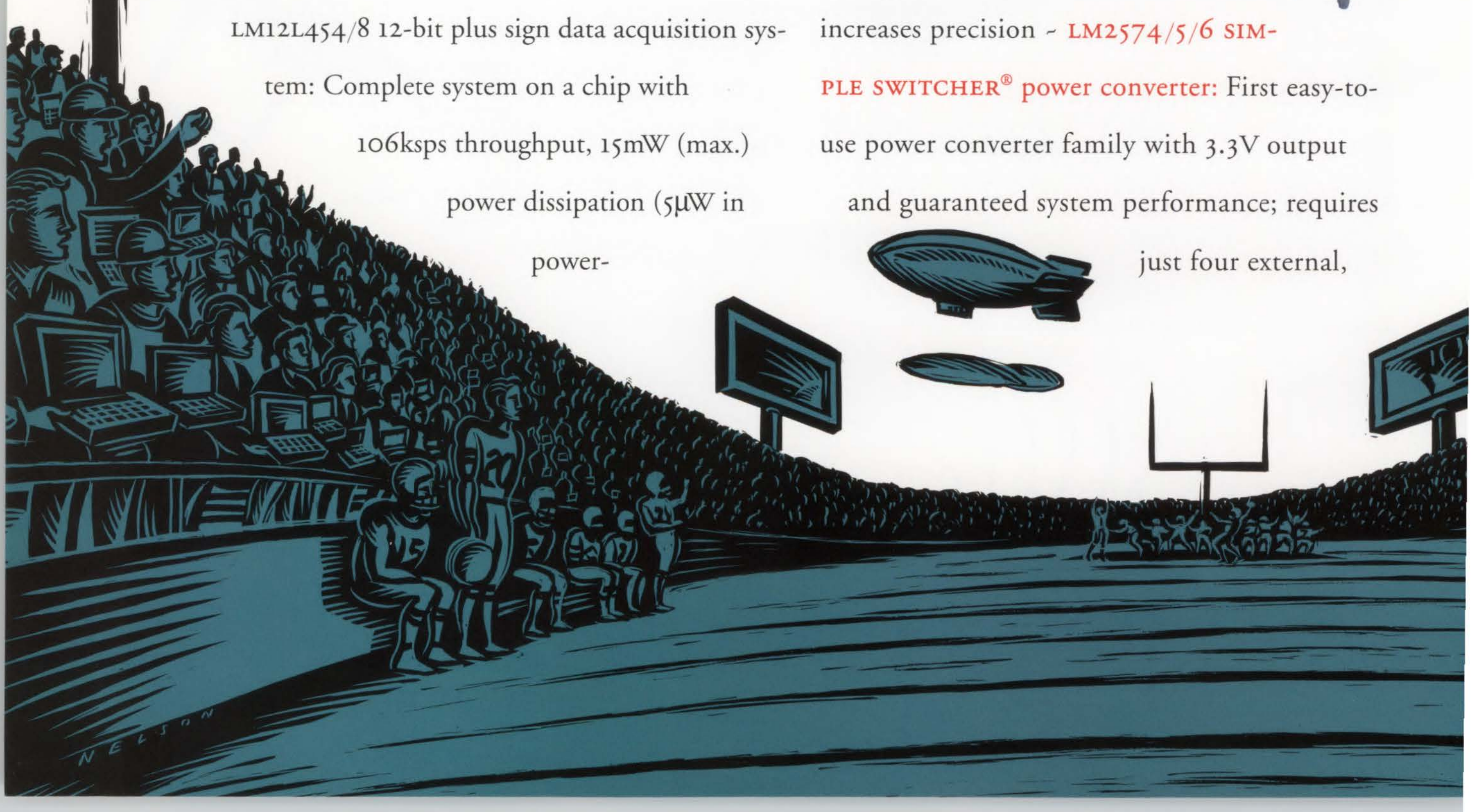


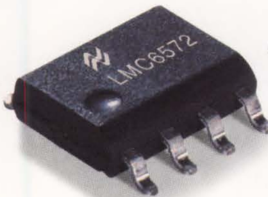
LM12L454/8 12-bit plus sign data acquisition system: Complete system on a chip with 106ksps throughput, 15mW (max.) power dissipation (5µW in power-down mode), and all the functionality needed for stand-alone operation ~ ADC12L030/2/4/8 12-bit plus sign A/D: Fastest 3V 12-bit serial A/D (maximum conversion time of 5.5µs) at 15mW (max.) power dissipation (40µW in powerdown); configurable registers ~ LMC6572/4 op amp: Low supply current of 40µA/op amp minimizes power consumption; guaranteed 2.7V and 3V single-supply performance; low input current increases accuracy ~ LMC6482/4 op amp: Rail-to-rail input and output increases dynamic signal range at 3V; lower offset voltages and higher CMRR increases precision ~ LM2574/5/6 SIMPLE SWITCHER® power converter: First easy-to-use power converter family with 3.3V output and guaranteed system performance; requires just four external,







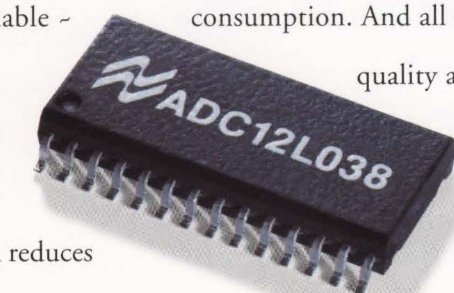
l o w - v o l t a g e   s o l u t i o n s



off-the-shelf components; design software available – **LP2950/51 low dropout regulator:** Very low dropout voltage of 380mV extends battery life; low quiescent current of 75μA reduces power consumption and power dissipation – **LM4041 voltage reference:** Subminiature SOT-23 package saves board space and reduces overall system size; adjustable voltage option (1.24V to 10V) provides design flexibility.

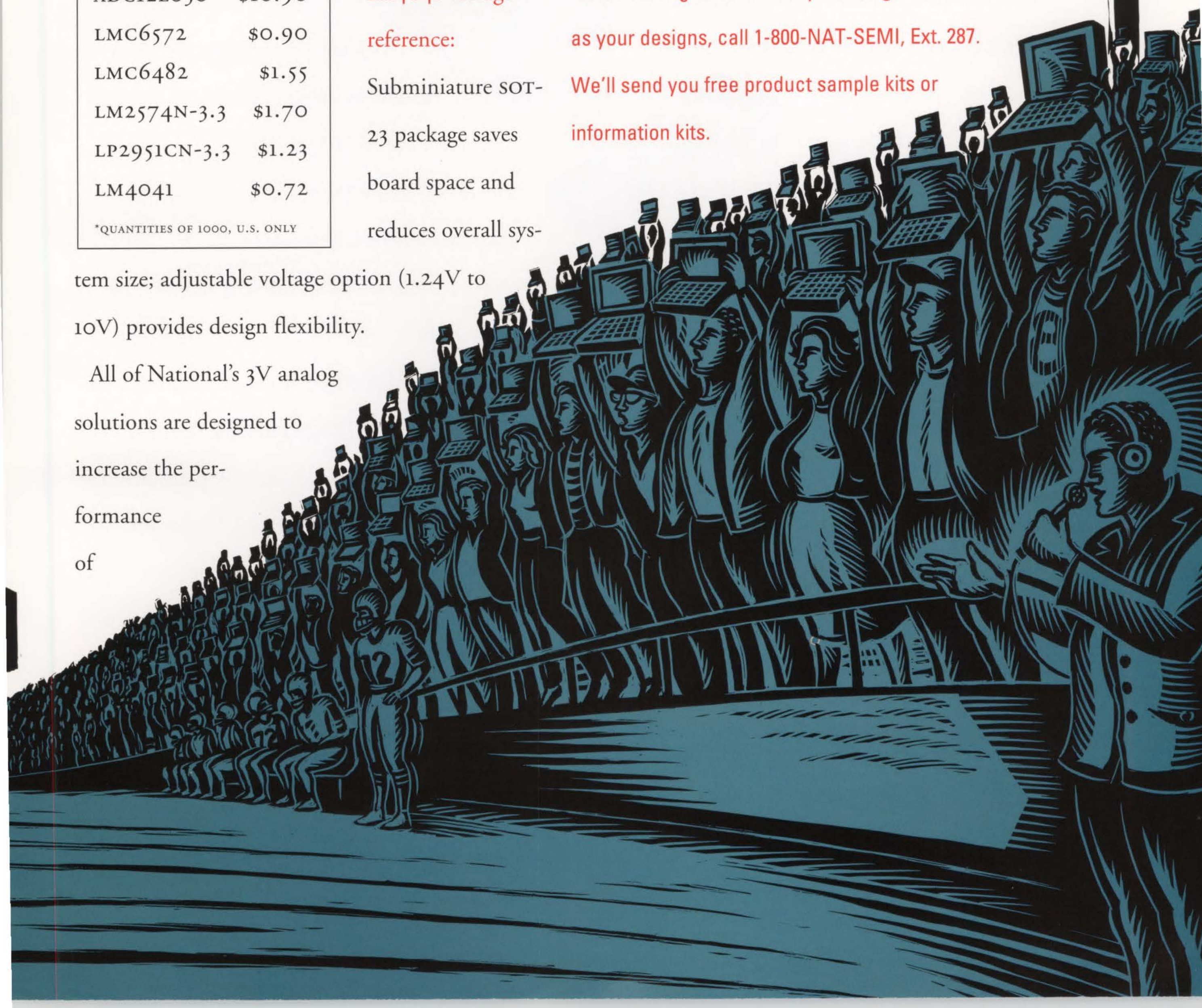
3V analog	
DEVICE	PRICE*
LM12L454/8	$15.00
ADC12L030	$10.90
LMC6572	$0.90
LMC6482	$1.55
LM2574N-3.3	$1.70
LP2951CN-3.3	$1.23
LM4041	$0.72

*QUANTITIES OF 1000, U.S. ONLY



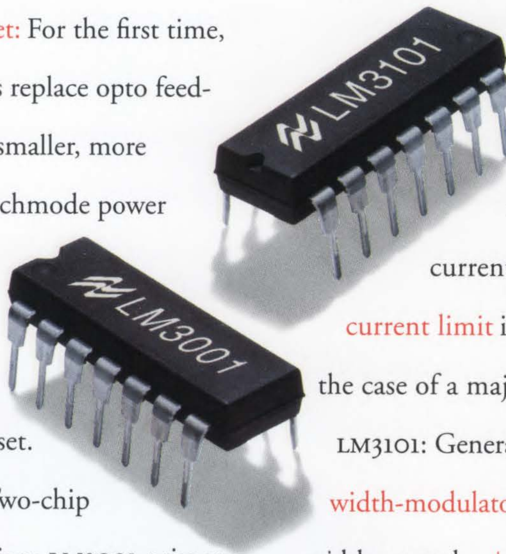
All of National's 3V analog solutions are designed to increase the performance of your portable designs — while reducing power consumption. And all of them come with the quality and reliability you expect from the original leader in analog IC technology. For pricing information, consult the box to your left or call the number below.

For 3V analog that will fuel your imagination as well as your designs, call 1-800-NAT-SEMI, Ext. 287. We'll send you free product sample kits or information kits.



Magnetics:
Opto-less chipset brings reliable power supplies offline.

The world's only 1MHz magnetically coupled offline power supply chipset: For the first time, high-speed pulse magnetics replace opto feedback devices. The result is smaller, more efficient, more reliable switchmode power supplies. The reason is National's LM3001/3101 offline power supply chipset.

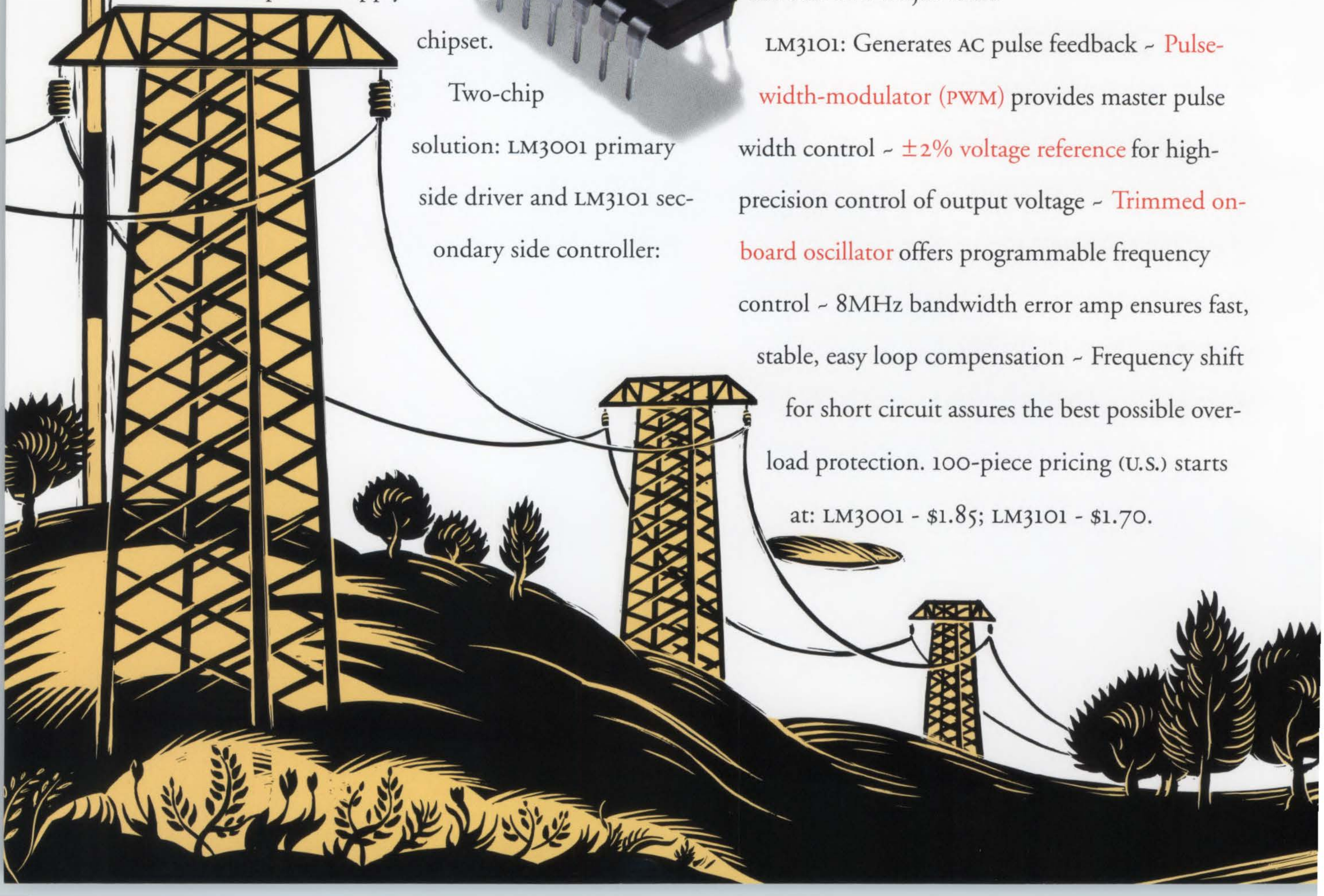


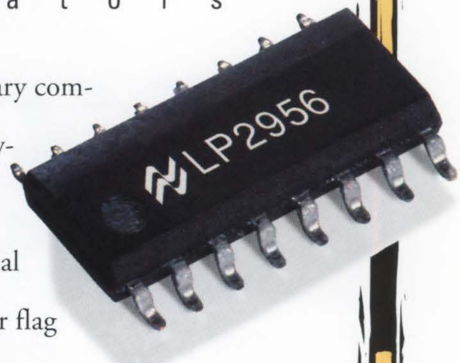
Two-chip solution: LM3001 primary side driver and LM3101 secondary side controller:

Fast AC feedback provides quicker response than optos ~ Up to 1MHz switching frequency enables the use of smaller inductors and capacitors.

LM3001: Accepts AC pulse feedback ~ 10ns rise and fall times provides greater efficiency and fast response to faults ~ On-board oscillator manages chip start-up ~ 2.5A peak current drives MOSFETs at high speed ~ Dual-level current limit provides virtually fail-safe operation: Cycle-by-cycle current limit offers fast current protection, while second-level current limit initiates complete shutdown in the case of a major fault.

LM3101: Generates AC pulse feedback ~ Pulse-width-modulator (PWM) provides master pulse width control ~ ±2% voltage reference for high-precision control of output voltage ~ Trimmed on-board oscillator offers programmable frequency control ~ 8MHz bandwidth error amp ensures fast, stable, easy loop compensation ~ Frequency shift for short circuit assures the best possible overload protection. 100-piece pricing (U.S.) starts at: LM3001 - \$1.85; LM3101 - \$1.70.





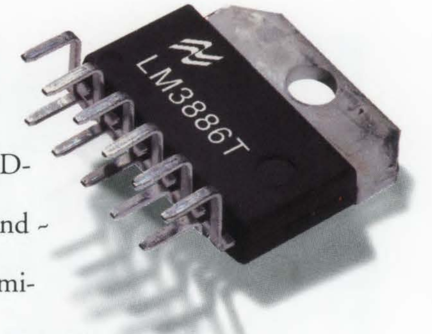
In portable applications, the dual LP2956 shuts down inactive systems while maintaining continuous power for essential functions.

.03% THD: 60 watts never sounded as good as this.

The world's best sounding monolithic audio amplifier: See if you like the sound of this. National's LM3886T provides a higher standard of high fidelity, as well as maximum power with maximum protection.

The 60-watt LM3886T *enables better, louder, longer sound in high-end audio applications like A/V surround sound receivers.*

Lowest typical total harmonic distortion (THD) from 20Hz to 20kHz at 25, 40, and 60 watts of continuous power provides the industry's best distortion/power rating ~ Signal-to-noise ratio is greater than 95dB min. (noise floor of 2.0μV), meeting the demands of CD-quality digital sound ~ Mute function eliminates transients at power up and power down ~ Devices can be easily bridged together ~ SPiKe™ self-protection circuitry adjusts output drive capability according to operating conditions, protecting output transistor array from overvoltages, undervoltages, or current limiting conditions, and providing thermal shutdown ~ Dynamic SOA protection ensures that power transistors won't be destroyed — even if faults continue for extended periods.

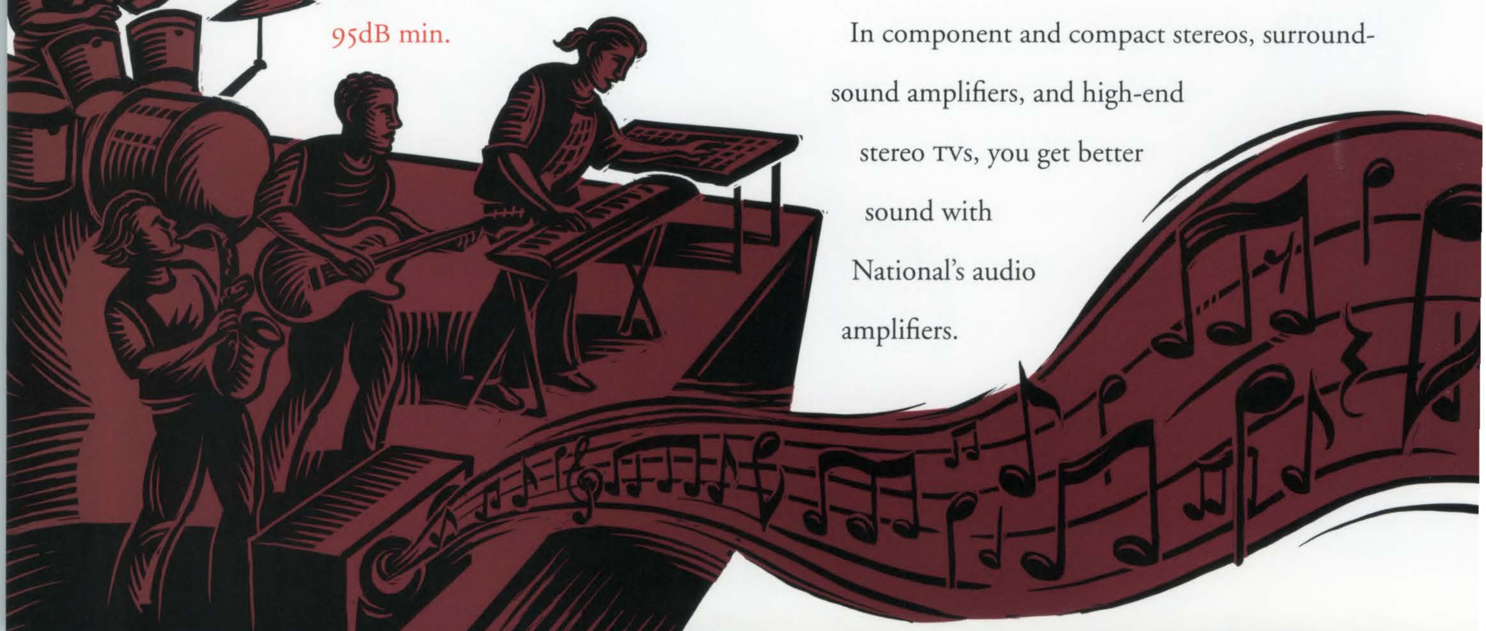


Typical THD*

DEVICE	THD (typ.)	OUTPUT
LM2876T	0.05%	25W
LM3875T	0.05%	40W
LM3876T	0.05%	40W
LM3886T	0.03%	60W

* from 20Hz to 20kHz

In component and compact stereos, surround-sound amplifiers, and high-end stereo TVs, you get better sound with National's audio amplifiers.



130MHz: High-speed LM1205 saves board space.

Complete broadband preamplifier system: When used with National's LM2419 CRT driver (see back cover), the LM1205 130MHz RGB video preamplifier replaces up to 36 components, compared to using standard preamps and discretes.

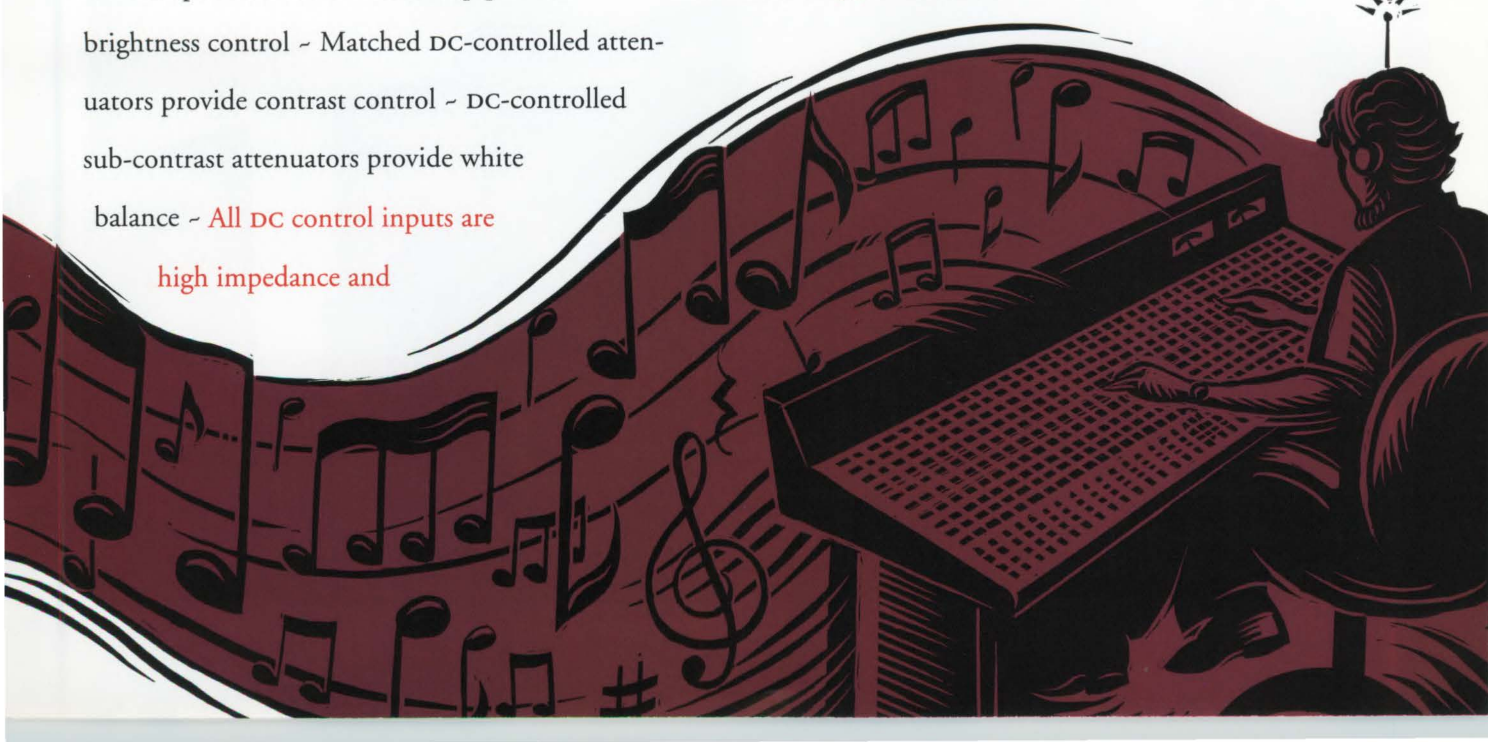
Features	
BANDWIDTH	130MHz
DC CONTROLS	0-4V
VIDEO BLANKING	YES
CHANNELS	3
APPLICATION	HIGH-RES. DISPLAYS

Provides the entire amplifier path required between the rear chassis input and the cathode for 1024 X 768 monitors ~ Each channel contains matched video amplifiers ~ Gated, single-ended input and black-level clamp provide brightness control ~ Matched DC-controlled attenuators provide contrast control ~ DC-controlled sub-contrast attenuators provide white balance ~ All DC control inputs are high impedance and operate over a 0 to 4V range for easy interface in microcontroller-based systems ~ Blanking circuit clamps the video output voltage to within 0.2V of ground ~ For high-speed, space-conscious designs.

The LM1205 provides the performance needed for multimedia applications.

In high-end, 17-inch RGB CRT monitors, 1280 X 1024 pixel systems, video AGC amplifiers, and wideband amplifiers with gain and DC offset controls, the LM1205 gives you more performance. While using less board space. In quantities of 1000, pricing (U.S.) starts at $2.50.

To fully appreciate the sights and sounds of National's audio and video ICs, call us at 1-800-NAT-SEMI, Ext. 287 and we'll send you free sample kits containing product samples, a blank applications board, data sheets, and application notes.



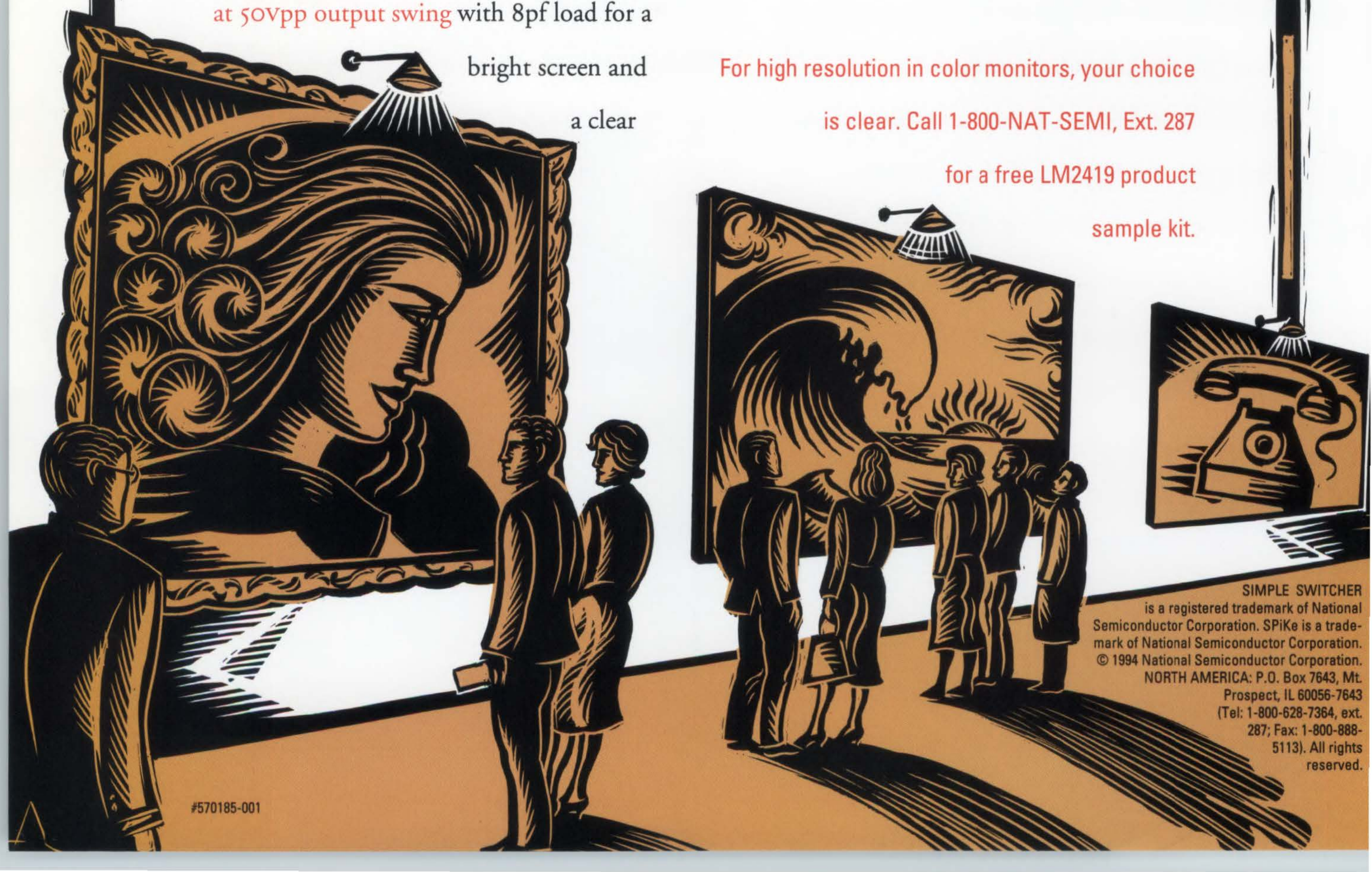
C R T d r i v e r s

5.0ns: For a picture everyone can appreciate.

High-performance triple CRT driver for high-resolution monitors: Picture a device that provides resolution up to 1024 x 768 in color monitors while simplifying overall design. You're picturing the LM2419, National Semiconductor's triple 65MHz CRT driver. Typical rise/fall time of 5ns provides clean, sharp signal transition edges for high-resolution images ~ 65MHz video bandwidth at 50Vpp output swing with 8pf load for a bright screen and a clear image ~ Three drivers match red, green, and blue channels in one device ~ Available in industry-standard TO-220 molded power packages ~ Electrically isolated heat sink may be grounded for ease of manufacturing and improved RFI/EMI shielding ~ Pin-for-pin compatible with LM2416, simplifying upgrades ~ No low-frequency tilt compensation required. For direct cathode drive capability in VGA, SVGA, XGA, IBM and Macintosh monitors, nothing looks better.

The LM2419's 5ns rise/fall time provides clean, sharp signal transition edges for high-resolution images.

For high resolution in color monitors, your choice is clear. Call 1-800-NAT-SEMI, Ext. 287 for a free LM2419 product sample kit.



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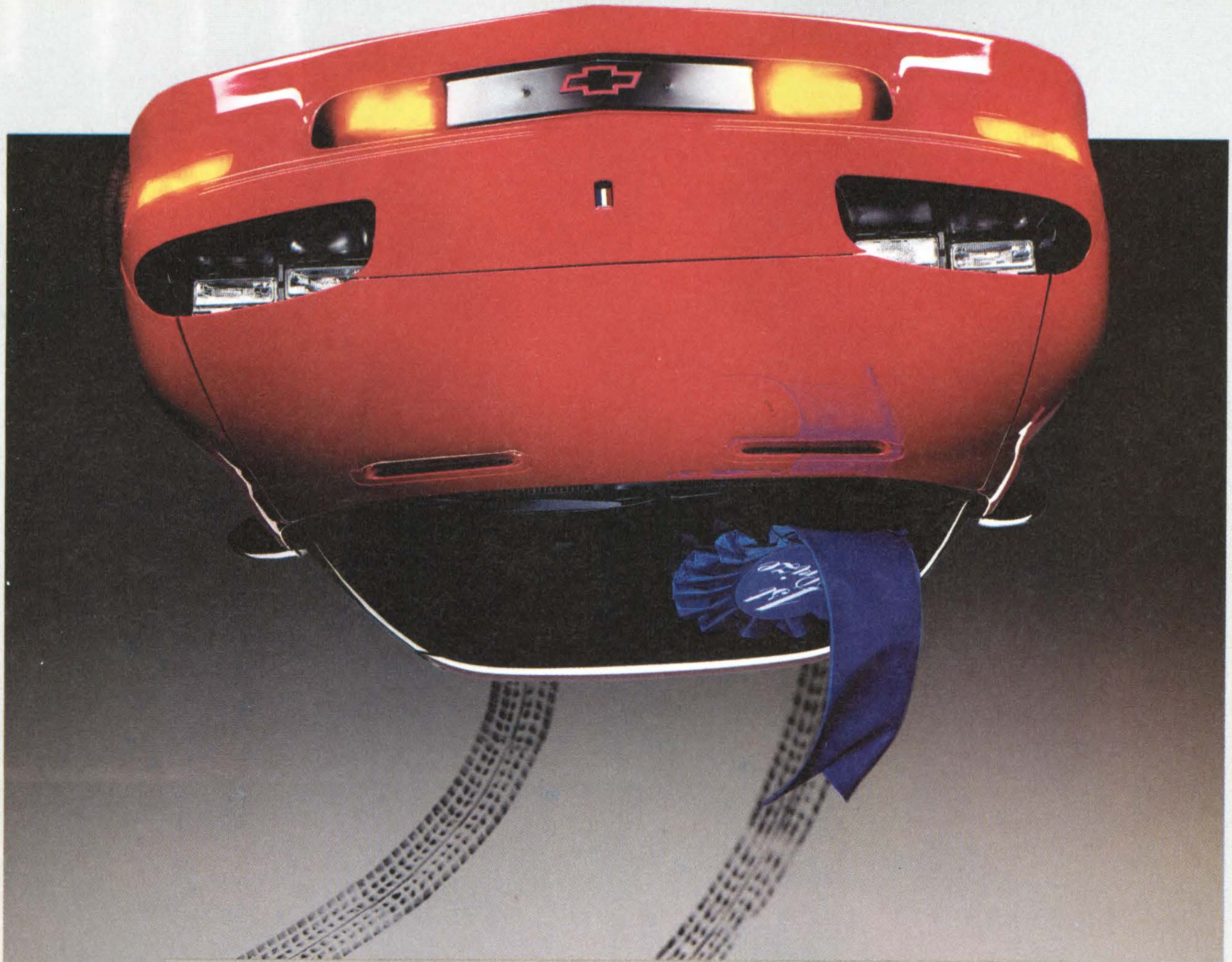
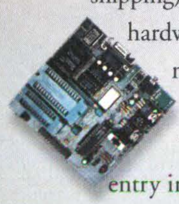
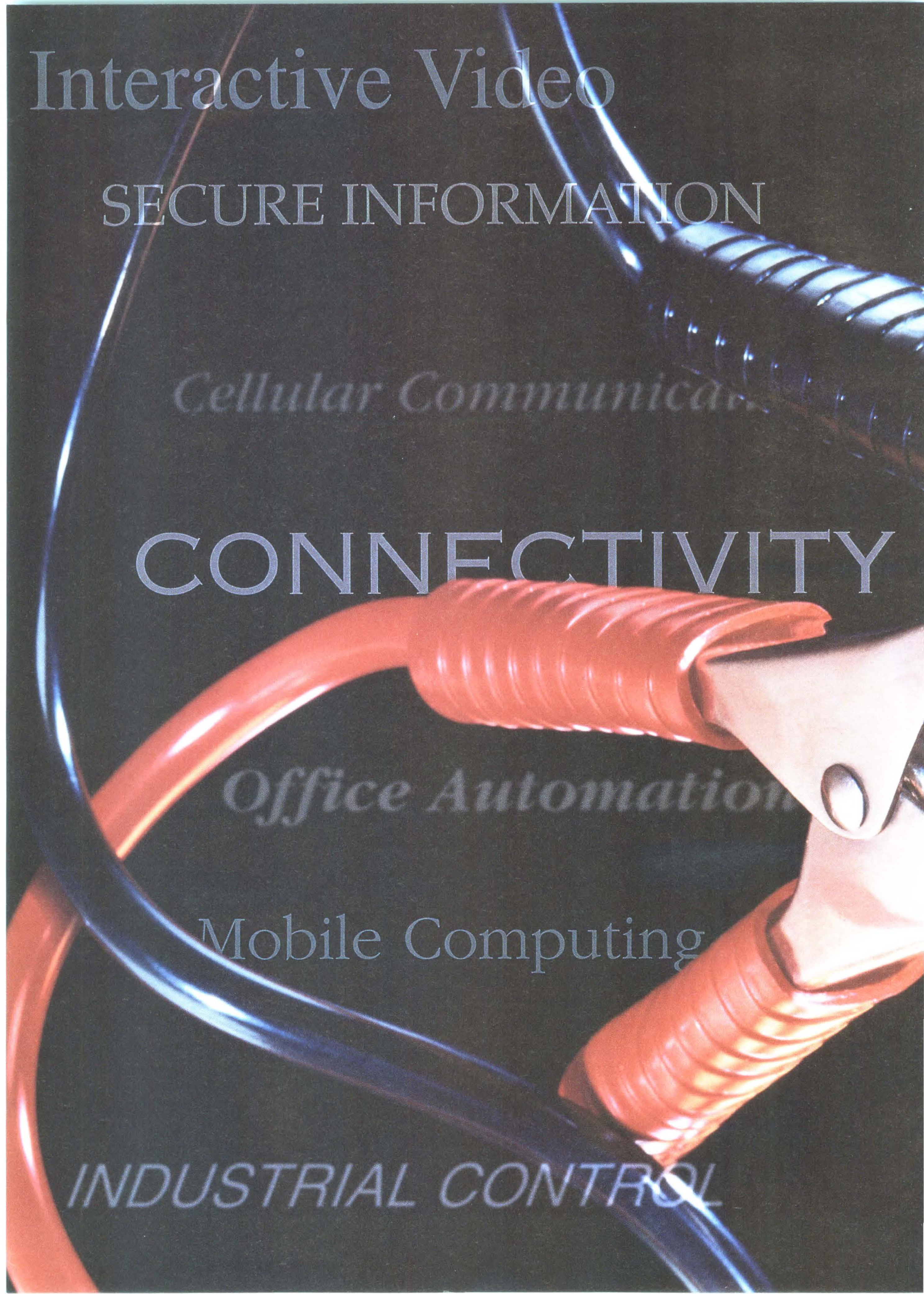
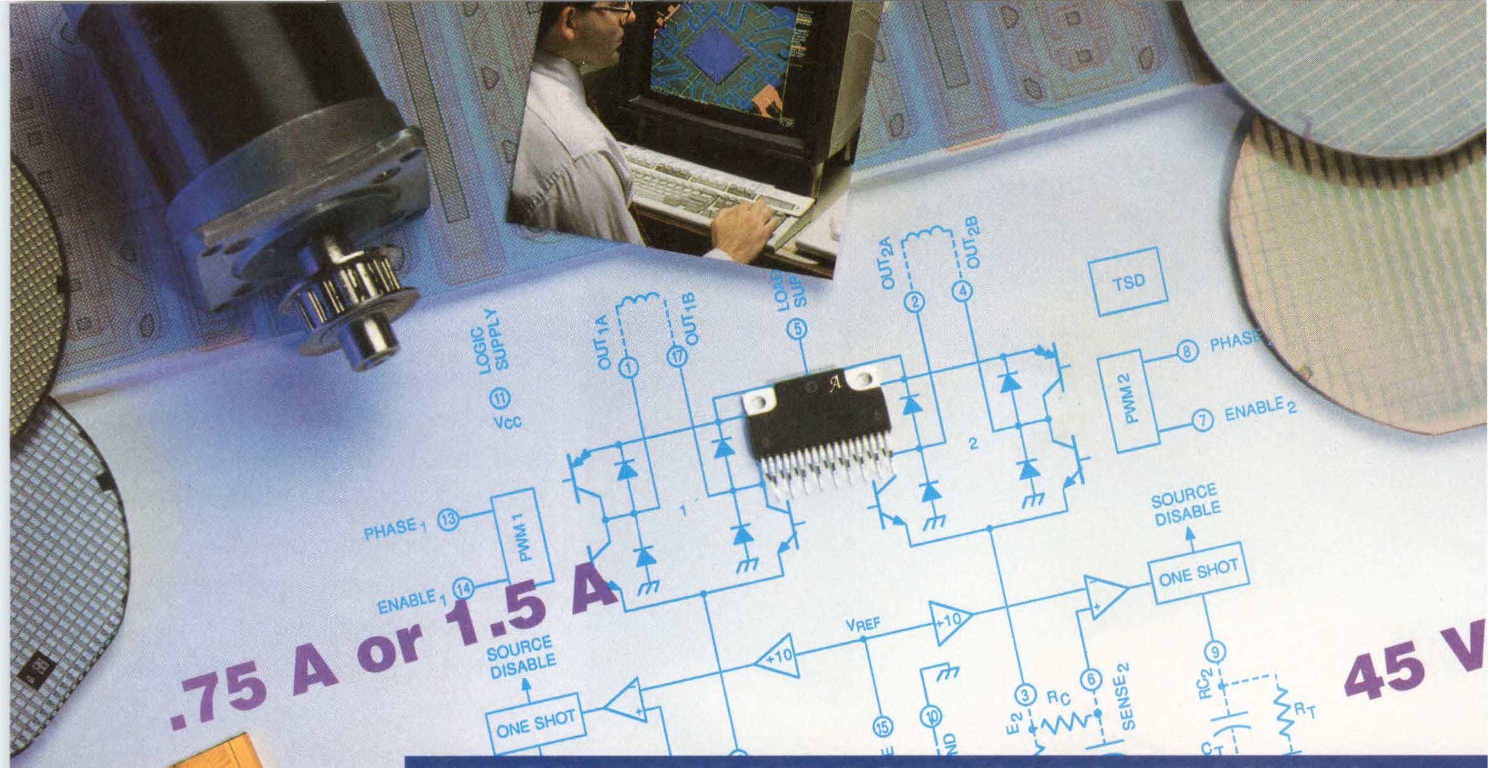


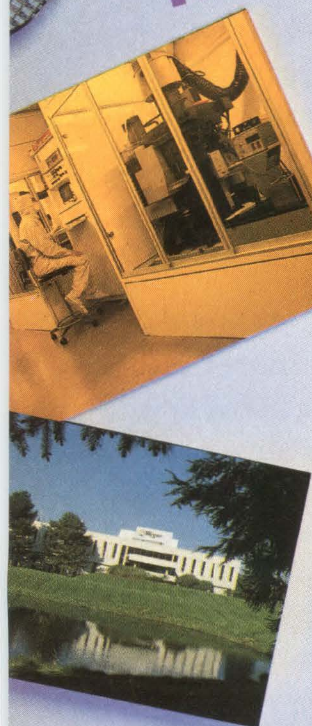



Interactive Video
SECURE INFORMATION
Cellular Communica
CONNECTIVITY
Office Automatio
Mobile Computing
INDUSTRIAL CONTROL



THE POWER TO DRIVE 2 WINDINGS WITH ONE IC

2916, 2917, & 2918 Dual Full-Bridge PWM Motor Drivers



FEATURES

- For Bipolar Stepper Motors or For Two DC Motors
- ±.75 A or ±1.5 A Continuous Output Current
- 45 V Output Sustaining Voltage
- Internal PWM Current Control
- Internal Clamp Diodes
- Internal Thermal Shutdown

Circuitry Elegantly Engineered To Meet Your System Requirements

Containing two full bridges, the Allegro's 2916, 2917, & 2918 motor drivers are designed to drive both windings of a bipolar stepper motor or bidirectionally control two dc motors. Each bridge is capable of sustaining 45 V and includes internal pulse-width modulation (PWM) control of the output current to ±.75 A (2916) or ±1.5 A (2917, 2918). Current is determined by the user's selection of a reference voltage and sensing resistor. Included on chip are ground clamp and flyback diodes for protection against inductive transients. Internally generated delays prevent cross-over currents when switching current direction. Thermal protection circuitry disables the outputs if the chip temperature exceeds safe operating limits.

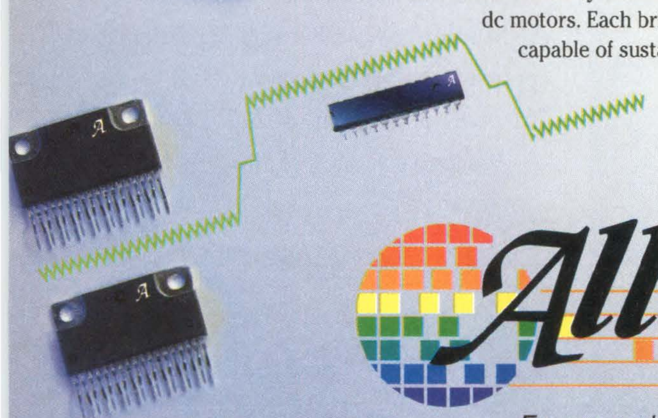
Designed For Manufacturability

Allegro's ICs are "designed-for-manufacturability" under stringent standards of Total-Quality. Design/Production teams, under our PACE (***P***roduct ***A***nd ***C***ycle-time ***E***xcellence) program, work closely with our customers to meet their time-to-market and quality/reliability objectives.

Headquartered in Worcester, Massachusetts, Allegro operates two Wafer-fabrication plants as well as assembly/test facilities. Design centers are located worldwide, sharing common cell libraries and design tools.

Take A Test-Drive... Call For Samples

Samples are available now. Just give us a call at 1•508•ALLEGRO and we'll have our Sample Pack in the mail to you the same day. After all, the measure of our success can only be *your total satisfaction.*



THE PACE QUICKENS

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OPTOELECTRONIC SENSING

Solid mechanical designs tempt engineers away from designing optical sensors

CHARLES H SMALL, Senior Technical Editor

All the bits and pieces for designing an optoelectronic-sensoring system are readily available. But the stressful environment in which sensors live often tilts the choice toward packaged systems.

Sensors animate your design, allowing it to react to the real world almost the way a living creature would. Perhaps the thrill of bestowing life explains why engineers are so interested in sensors. **Refs 1** through **5** are a sampling of ingenious sensor designs engineers have sent to *EDN*'s Design Ideas section.

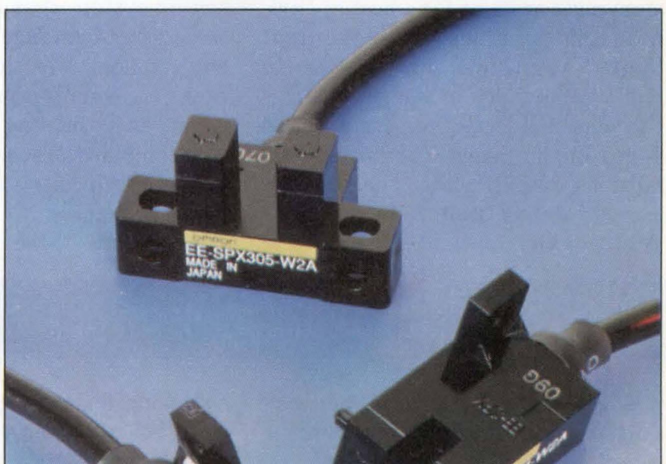
You can buy all the bits and pieces to design your own advanced optical-sensing system, or you can select a prepackaged system. Whichever path you take, you have more choices than can be detailed in a single magazine article. Batelle Institute estimates that more than 500,000 types of sensors, measuring over 100 measurement variables, are commercially available (**Ref 6**).

Silicon photodiodes can monitor such applications as machine-tool tracking, targeting, and remote-position sensing. One recent improvement on the classical silicon photodiode is Silicon Sensors' quad photodiodes. The quad photodiodes put four sensors into one TO-8 package. Special blue-sensitive and high-speed versions are available.

Lumex Opto/Components Inc also has discrete photodiodes, PIN photodiodes, phototransistors, photo darlingtons, infrared-emitting diodes, and photointerrupters. In a more specialized vein, Mitsubishi has a series of contact image sensors and an accompanying interface IC. The sensors combine LED, rod-lens, and sensor arrays. The sensors can scan images at 8 or 16 dots/mm at rates from 2.5 to 10 msec/line. The IC converts the scanner's analog output to digital signals. Sensors range from \$50 to \$100 each, and the ICs cost \$3.50 (10,000).

Other specialized ICs, such as the Burr-Brown DDC101, bolt directly to optoelectronic devices. The DDC101 is a 20-bit, current-input A/D converter that connects directly to low-level sensors, such as photodiodes.

However, some optoelectronic companies can supply you assemblies that integrate some system-level devices into one package.

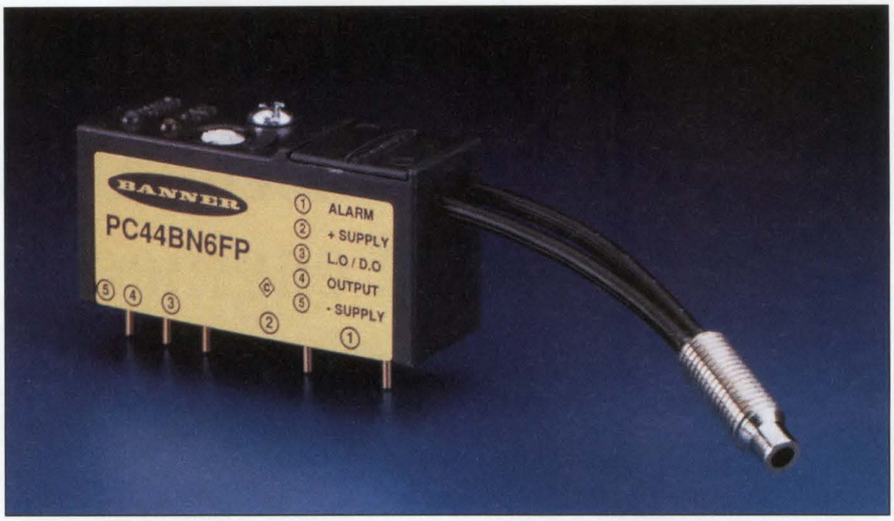


Omron photomicrosensors come with attached cables. The sensors' internal electronics overcome the adverse effects of ambient light.

OPTOELECTRONIC SENSING

For example, Clarostat's Model T60 amplifiers provide a modulated output for position-sensor LEDs. Burr-Brown's OPT202 ($4.25), OPT209 ($5.25), and OPT301 ($11.10) integrate a 0.09×0.09-in. photodiode, a precision FET-input transimpedance amplifier, and a 1-MΩ feedback resistor on a single chip. The OPT209's bandwidth is 16 kHz for general-purpose applications. The OPT202's bandwidth is 50 kHz for pulsed-light applications, such as bar-code scanners. The OPT301 has a 4-kHz bandwidth, and its 400-μA quiescent current suits it for battery-powered applications.

Before committing to a one-of-a-kind hybrid device, you could use Centronics' OSI 5-DEV prototyping device. It combines a silicon photosensor, an op amp, and associated components in a 10-lead TO-5 package. You can order a variety of sensors, op amps, and other components. The prototype device can stand in for a full-blown hybrid device during development.



You can solder Banner photoelectric sensors directly to your pc boards.

Too much, too fast

An optical sensor leads a tough life. In addition to meeting applicable safety regulations and being foolproof to install and maintain, an optical-sensor system must account for a host of environmental variables. Ambient-light changes, variations in the sensed object's reflectivity or speed, changes in the sensed object's temperature, and changes in the general environmental conditions can all affect the sensor's electronic output (**Refs 7** and **8**).

Additionally, optical sensors' and emitters' performance changes with age. Degradation of a sensor's package accounts for some of the aging, particularly in plastic packages because of thermal mismatches among the materials used. Subtle semiconductor-physics effects account for the rest of the aging. For example, the light output of LEDs falls off with age because of nonradiative recombination sites that form within the semiconductors.

Consequently, designing an optical-sensor system that exhibits accurate, stable performance in a changeable environment over time is not a simple task. Sensor companies have made advances by fielding packaged devices that combine the sensor and signal-conditioning circuitry in one industrial-grade package.

Also, some of the devices are general-purpose; others are extremely specialized. For example, the sole job of Exergen's AAM series of infrared temperature detectors is to monitor the temperature of adhesives during application and curing.

Photoelectronic switches

The simplest optical sensor is the photoelectronic switch. For flexibility, most photoelectronic-switch lines include models that accept ac or dc power. Output choices include pnp or npn transistors, FETs, or relays. The switch's light sources operate in either diffuse mode for proximity sensing or retroreflective mode as a beam-interruption switch.

The current trend is to make these photoelectronic components resemble the electromechanical components they replace as much as possible. For example, Automatic Timing & Controls' 7680 series of photoelectronic switches features miniature rectangular NEMA 4 housing. Scientific Technologies Inc and Automatic Timing & Controls both have switches that come in standard 18-mm packages; Balluff Inc has optoelectronic sensors that mount on DIN rails. For ease of installation, Omron ships photointerrupters that have cables installed. And Banner can supply photoelectric sensors that you can solder directly to your pc boards or plug in using a mounting jack.

Engineers most often think "thermocouple" when tasked with measuring temperature. But radiated heat is a

LOOKING AHEAD

Optical sensors play a tiny, but vital, role in fiber-optic communications. The predicted "Information Superhighway" will have to employ fiber-optic links to achieve meaningful performance. So, while armies of optical sensors continue to toil quietly in the factory, fiber-optic communications will spark the most dramatic growth.

For example, Galaxy Microsystems has developed its LL7720 Series fiber-optic transmission system using single-mode fiber that costs less than current multimode fiber-optic systems. Yet it has much better performance than lower-cost LED-based systems. The system's lower cost has allowed customers to install local networks, many kilometers in total length, that carry voice, data, and video all on the same fiber-optic cable. Accelerated development of semiconductor lasers and photosensors for fiber-optic communications will provide low-cost, high-reliability components that engineers can press into service for other applications.

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If you need more convincing that QuickLogic delivers a superior time-to-market design solution, just fax us your business card. Be one of the first 100 faxes and receive a **FREE** Evaluation Kit, complete with all the tools you need to enter, simulate and analyze your design.

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CIRCLE NO. 84

OPTOELECTRONIC SENSING

form of light that optical sensors can measure. Optical heat sensors range from pinpoint devices that measure one small spot's temperature to scanners that develop a thermal map of an area. For example, the MP4 family of multipoint scanning thermometers from Raytek Inc continuously scans and displays real-time, full-color thermal contour maps or temperature profiles of surface temperatures.

AGEMA Infrared Systems' Thermopoint single-point radiometers monitor a fixed spot. The company's Thermoprofile Infrared Smart Line Scanner can plot temperature up to 24,000 points/line across a 90° arc, as often as 40 times/second. For bigger jobs, a Thermovision 900 infrared imager can measure a large object's temperature in up to 100 areas.

Just as infrared sensors can measure temperature without touching the object to be measured, LED- and semiconductor-laser-based systems can measure an object's position without touching it. Selective Electronic Inc has self-contained, high-speed dimensional-gauging sensors that use laser triangulation. The SLS 5000 series integrates a sensor and a processor within the device's head. The processor performs data averaging and filtering.

Laser-based systems trade off accuracy for measuring speed or range. For

FOR FREE INFORMATION...

For free information on the sensor products discussed in this article, circle the appropriate numbers on the postage-paid Information Retrieval Service card or use *EDN's* Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in *EDN*.

AGEMA Infrared Systems
Secaucus, NJ
(201) 867-2191
Temperature sensors
Circle No. 301

Aleph International
San Fernando, CA
(818) 365-9856
Actuators, interrupters, and reflectors
Circle No. 302

Aromat Corp
New Providence, NJ
(800) 228-2350
Laser-based measuring systems
Circle No. 303

Automatic Timing & Controls
Marion, OH
(614) 387-8827
Photoelectric sensors
Circle No. 304

Avtek Electrosystems
Ottawa, ON, Canada
(613) 226-5772
Laser-diode drivers
Circle No. 305

Balluff Inc
Florence, KY
(606) 727-2200
Optoelectronic sensors
Circle No. 306

Banner Engineering Corp
Minneapolis, MN
(612) 544-3164
Photoelectric sensors, fiber-optic sensors
Circle No. 307

Burr-Brown
Tucson, AZ
(602) 746-1111
Optoelectronic ICs, converters
Circle No. 308

Centronics Inc
Newbury Park, CA
(805) 499-5902
Photodiodes, development systems
Circle No. 309

Clarostat
Sensors and Controls Group
Plano, TX
(214) 423-4661
Photosensor amplifiers
Circle No. 310

Exergen
1 Bridge St
Newton, MA
(800) 422-3006
Infrared temperature sensors
Circle No. 311

Galaxy Microsystems
Systems Div
Austin, TX
(512) 467-9871
Laser position sensors
Circle No. 312

Hamamatsu Corp
Bridgewater, NJ
(908) 231-0960
UV detectors
Circle No. 313

International Light Inc
Newburyport, MA
(508) 465-5923
UV detectors
Circle No. 314

Kaman Instrumentation Corp
Colorado Springs, CO
(719) 599-1132
Position sensors
Circle No. 315

Laser Atlanta Optics
Norcross, GA
(404) 446-3866
Laser range and speed sensors
Circle No. 316

Linear Laboratories
Fremont, CA
(510) 226-0488
Temperature sensors
Circle No. 317

Lumex Opto/Components Inc
Palatine, IL
(708) 359-2790
Photo sensors and emitters
Circle No. 318

Melles Griot
Electro-Optics Div
Boulder, CO
(303) 440-0140
Laser-diode assemblies
Circle No. 319

Mitsubishi
Sunnyvale, CA
(408) 730-5900, ext 2667
Contact image sensors
Circle No. 320

MTI Instruments
Latham, NY
(518) 785-2464
Noncontact fiber-optic measurement instruments
Circle No. 321

Omron Electronics Inc
Control Components Div
Schaumburg, IL
(708) 843-7900
Opto sensors
Circle No. 322

Ramco Electric Co
West Des Moines, IA
(800) 280-6933
Laser position sensors
Circle No. 323

Raytek Inc
Santa Cruz, CA
(408) 458-1110
Temperature sensors
Circle No. 324

Scientific Technologies Inc
Hayward, CA
(510) 471-9717
Photoelectric sensors
Circle No. 325

Selective Electronic Inc
Southfield, MI
(313) 355-5900
Laser-based position sensor
Circle No. 326

SICK Optic-Electronic Inc
Eden Prairie, MN
(612) 941-6870
Photoelectric switches, scanners, distance measurers
Circle No. 327

Silicon Sensors
Dodgeville, WI
(608) 935-2707
Photodiodes
Circle No. 328

Skan-A-Matic
Plano, TX
(214) 422-1844
Position sensors
Circle No. 329

Tri-Tronics Inc
Tampa, FL
(800) 237-0946
Photoelectronic sensors
Circle No. 330

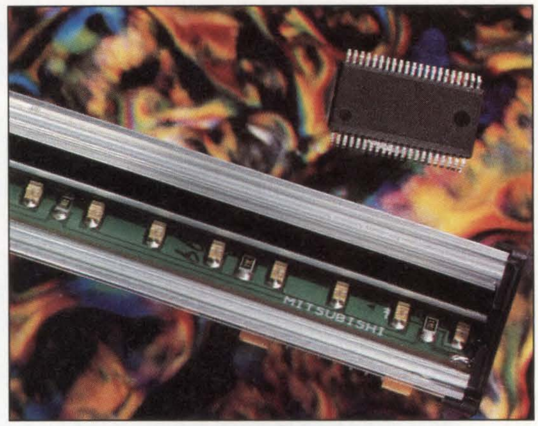
UBM Corp
Roselle, NJ
(908) 241-8652
Laser-based measuring systems
Circle No. 331

Watlow Infrared
Decorah, IA
(800) 251-1473
Temperature sensors
Circle No. 332

Super Circle Number
For more information on the sensor products available from all of the vendors listed in this box, you need only circle one number on the postage-paid reader service card.
Circle No. 333

OPTOELECTRONIC SENSING

example, UBM Corp's laser-based UBC 14 noncontact measuring system's accuracy is 0.01 μm over a 0.04-in. measurement range. Ramco Electric's SUNX LA511 laser sensor exhibits 0.01-mm accuracy over a much wider area. Clarostat's Skan-A-Matic detects a 0.020-in. object at 36-in. separation between emitter and sensor. And Aromat Corp's LM laser sensor series offers a selection of ranges, bandwidths from 1 to 20 kHz, and resolutions from 0.0002 to 0.000008 in.



Mitsubishi's contact image sensors combine an LED array, a rod-lens array, and a sensor array.

Even though most optical sensors are either visible-light or infrared sensors, ultraviolet sensors do exist. International Light Inc's SED220/NS184 "solar-blind," deep-UV detector comes in a watertight, anodized-aluminum package. The sensor's maximum response is 160 nm. A species of Geiger-Müller tube, Hamamatsu's UVTRON R2868 "hostile-flame" sensor can detect a flame's ultraviolet emanations from as far away as 16 ft. EDN

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5. Hwang, Sheng-Feng, "[capacitive] Detector spots extra sheets," *EDN*, December 7, 1989, pg 260.

6. Ormond, Tom, "Smart sensors tackle tough environments," *EDN*, October 14, 1993, pg 35.

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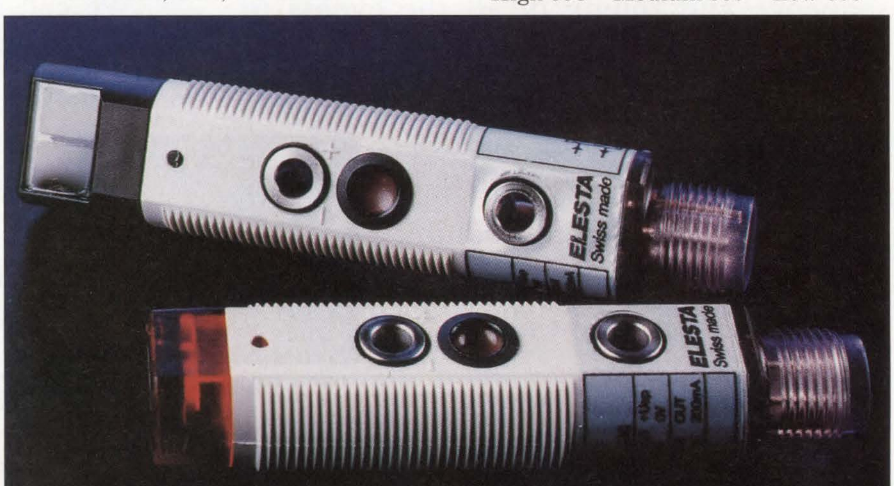
8. Graeme, Jerald, "Phase compensation optimizes photodiode bandwidth," *EDN*, May 7, 1992, pg 177.

Article Interest Quotient
(Circle One)
High 598 Medium 599 Low 600



The lenses of Scientific Technologies' STI/Elestra 72 series of self-contained photoelectric sensors are flat because flat lenses collect less dirt than do curved lenses. The sensors come in standard 18-mm packages.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VIDEO
IMAGE
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- Single-chip TDC1500 (PHY) and single-chip TDC1560 (SAR) optimized for adapter cards
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- Interfaces with either multimode fiber or UTP5 cabling
- Complies with ATM Forum UTOPIA and UNI standards

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- Analog phase-lock loops perform on-chip clock recovery and generation
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- 240-pin MQUAD

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To multiprocess or *not* to multiprocess?

Use several processors when one would do? Never; well...*hardly* ever. But when one processor isn't enough, there are approaches and tools that can help you to stay on schedule and avoid breaking the bank.

DAN STRASSBERG, SENIOR TECHNICAL EDITOR

If the mere mention of "multiprocessing" makes visions of hypercubes dance in your head, you're not alone. ("Hypercube," in case you're unfamiliar with the term, is a high-performance parallel-processing architecture.) As a rule, EEs think of multiprocessing as interesting mostly to academics and designers of military hardware—folks who, until recently, had generous budgets and even more generous schedules. But multiprocessing isn't just for the academically talented and the idle rich; it's also for those with practical problems, tight schedules, and limited budgets.

In fact, there's an excellent chance that multiprocessing has already come to a system near you; maybe it's no more than a few feet away. Most likely, that system costs less than $2000 and is something you use every day. It is, of course, your PC. Although some newer high-performance servers use multiple CPUs, $2000 PCs aren't that exotic, but they are multiprocessing systems—of a sort. Besides a 486 or Pentium CPU chip, they contain specialized μPs that handle keyboard interfacing, disk I/O, graphics display, and networking. More and more modems are built around DSP μPs. So too are newer sound cards. Full-motion video will add still other specialized μPs.

Yet, when you write programs to run on a PC, you write code only for the CPU. Rarely, if ever, do you need to think about the specialized processors. The code that runs on them usually resides in ROM—either in the motherboard's BIOS chip, within the specialized ICs themselves, or on the expansion cards that house the chips.

As the PC demonstrates, large, performance-at-any-price parallel-processing systems are not the only form of multiprocessing system. Networks of computers or workstations are also multiprocessing systems, though such networks are more commonly called "distributed-processing systems."

Under the "multiprocessor-systems" umbrella, you'll encounter a variety of philosophies and architectures. Like the PC, many multiprocessor systems are far from massive or costly. Some are cost-effective even for relatively small embedded systems. Nevertheless, all but the most passionate advocates of multiprocessing are loath to recommend any form of the technique (except, maybe, the type found in a PC) to anyone who doesn't need it.

Avoid overkill

If a 1-processor system can do the job—and if over the product life the improvements you expect in μP processing power support the growth you anticipate in system-performance requirements—opt for the 1-processor implementation. It will usually be smaller and less costly than a multiprocessor system and will use less power. Even more important, software development will be faster and easier.

The biggest bugaboo in multiprocessor systems is synchronization among the processors, which is a job

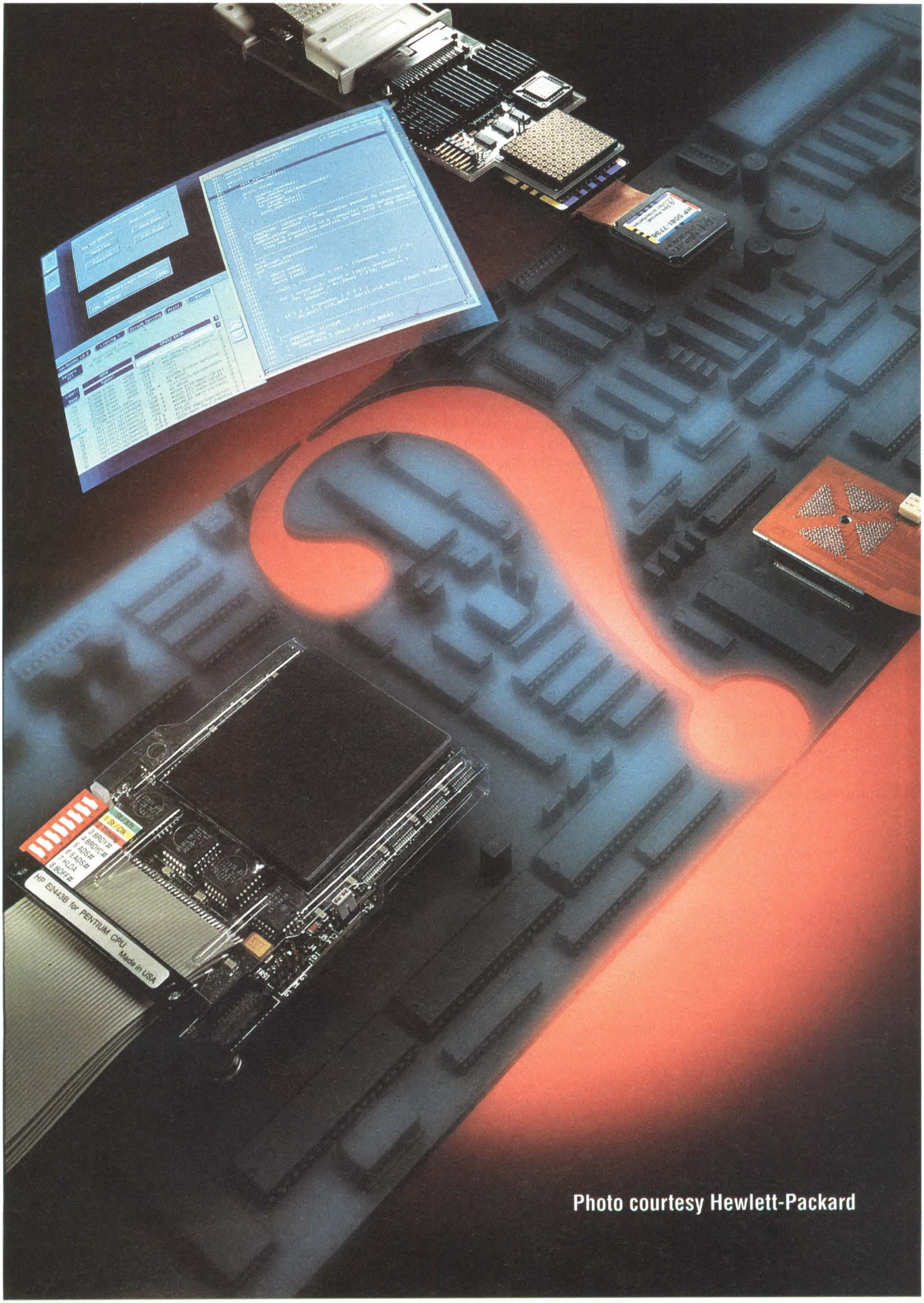
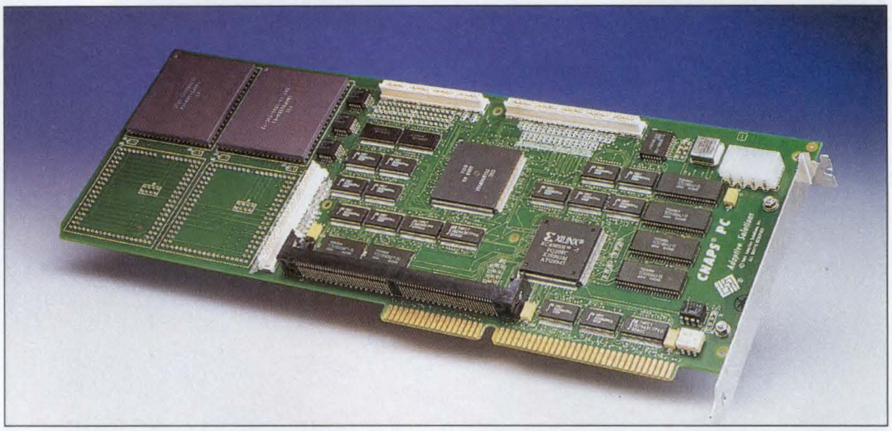


Photo courtesy Hewlett-Packard

that gets more difficult the more tightly the processors are coupled. If not handled deftly, synchronization can become so complex and burdensome that the overhead eats system throughput alive. If you don't do the job well, your multiprocessor system can turn out to be less productive than a single-processor system would have been. As one developer puts it, "We thought we were developing a dual-processor system; what we created was a system of dueling processors. We made the sword, and both processors fell on it."



Signal processing lends itself to parallel processing better than do most application areas. Adaptive Solutions' CNAPS-PC board, which plugs into the ISA bus, accommodates proprietary chips that each contain as many as 64 DSPs, allowing a single slot to accommodate 128 processors.

But there are exceptions that prove the rule, and the PC provides one. Although it would probably be cheaper to build a PC in which the CPU chip took over all of the functions that half a dozen specialized processors now perform, development of a suitable CPU chip could easily add years to the PC's development cycle. Given the evanescence of products in today's PC marketplace, the 1-processor PC might not arrive until years after anyone had an interest in buying it. (The developers of the aforementioned ill-fated dual-processor system eventually replaced their custom 2-processor CPU board with a standard PC motherboard. On it is the usual small army of specialized µPs that support the main CPU.)

Many multiprocessor chips

Despite the problems involved in developing a single chip to perform all of a PC's processing functions, single chips that incorporate multiple processors are starting to proliferate. Of these, TI's MVP, also known as the TMS320C80, has received the most publicity of late. The MVP includes a 32-bit RISC master processor and four 32-bit DSPs, as well as a video controller and a transfer controller that manages communication among the processors.

The MVP is scarcely the only multiprocessor on a chip, however. Another example is Motorola's 68360 QICC (quad integrated communications controller), which includes a 32-bit microcontroller core (a full implementation of the CPU32 core of the vendor's 683xx series), a special-purpose RISC processor, and four serial-communication controllers. Star Semiconductor's SPROC-1400 chip includes, among other elements, four 24-bit fixed-point DSPs. Adaptive Solutions' CNAPS chips (normally sold only as part of VMEbus and ISA-bus boards) include as many as 80 16-bit fixed-point DSPs on a single piece of silicon.

Besides compute-bound applications in which processing-power requirements dictate the use of multiple processors, certain classes of applications require multiprocessing:

- Fault-tolerant types, such as online transaction-processing (OLTP), in which the failure of a CPU must not affect system availability. Such applications require multiple, redundant CPUs.
- Distributed applications, such as

SIGNAL PROCESSORS LISTEN TO THE RADIO

Companies spend millions on radio and TV advertising. And they often have to rely on the logs that station personnel keep to verify that the commercials they pay for actually air. Although most local advertisers or their advertising agencies still use primitive approaches, for large national accounts, listening for commercials has gone high-tech...*very* high tech.

In the operations center of Broadcast Data Systems in Kansas City, MO, a system called Radiotrack constantly monitors 900 radio stations and the audio of 600 TV stations in the 100 largest US markets. The company operates similar systems in Europe and Asia. The system's primary input is a receiver's audio output. An ADC converts this into a series of digital words.

The converter output goes to a bank of DSPs that uses matrix differencing to compare the incoming signals against a stored library of digitized signatures of commercials and other program material. It isn't necessary to store an entire commercial; the first few seconds suffice. The matrix-differencing operation produces a ranking of signatures most likely to match the unknown signal. An array processor then performs an FFT on the unknown signal and compares it against FFTs of the library items most likely to match it.

The hardware uses a combination of a 68040, multiple TMS320C50s, and a pair of array processors from Sky Computers. Identical technology can determine which recordings radio stations are playing most often; airplay is key to determining whether a recording will be a commercial success. If you listen to the radio very much, you know that one of the system's great strengths is that the multiple processors never complain about having to listen, hour after hour, to rap or heavy metal...or Rush Limbaugh or Larry King.

process control and factory data collection. Such applications often have fault-tolerance requirements almost as stringent as those of OLTP. Even more important, distributed intelligence reduces the system's message traffic, allowing the use of much less expensive networking hardware.

The **box**, "Multiple approaches to multiprocessor systems," contains a slightly different and somewhat broader view of these issues. The **box** is based on material supplied by Doug Williams, marketing manager at Sky Computers.

An area where additional CPUs can make sense even if they aren't absolutely mandatory is managing user interfaces. In many systems, one µP handles operator-interface functions while another manages real-time control functions. This arrangement represents a multitasking, multiprocessing application. Instead of executing all tasks on a single µP, specific tasks are assigned to specific µPs. Several attributes characterize this division of responsibilities:

MULTIPLE APPROACHES TO MULTIPROCESSOR SYSTEMS

Applications suited to a single powerful processor or (depending on throughput requirements) to parallel processing:

- Single-threaded numerical applications
- Applications with a single, pipelined data stream
- Parallel processing is appropriate in applications that were previously handled by a single processor but where increases in required performance have outstripped the capabilities of a single processor.

Examples:

- Medical imaging (CAT—computer-assisted tomography, MRI—magnetic-resonance imaging, PET—photon-emission tomography)
- Radar and sonar
- Industrial inspection
- Ultrasonic detection

Advantages of single-processor architecture:

- Simpler, less expensive hardware
- Simpler software, lower development cost

Advantages of parallel processing:

- Much greater throughput; functions that would take a long time if handled by a single processor need not significantly impact overall performance
- Scalability; often easier to add capability as performance requirements increase

Applications suited to multiple loosely coupled processors:

- Multithreaded applications with Unix interprocessor communication (IPC)
- Applications with multiple data streams
- Applications in which a network of processors shares a centralized numerical-computing resource
- Fault-tolerant applications

Examples:

- Electronic-warfare systems
- Flight simulators
- Seismic data-processing systems
- Automatic test equipment
- Character-recognition systems
- On-line transaction-processing systems

Concerns when developing systems that use multiple loosely coupled processors:

- Coordination of tasks
- Processors may have to wait for each other
- IPC overhead
- Memory contention
- System complexity

Advantages of loosely coupled processors:

- Handle multiple operations and tasks simultaneously
- In some cases, dividing the work among multiple developers is easier than with a single processor.

Table 1—Suppliers of embedded-system development tools that support multiprocessing and/or μPs

Company	Circle No.	Location	Phone	Product	Base US Price[3]
Accelerated Technologies	382	Mobile, AL	(205) 661-5770	Nucleus DBUG	$5000 kernel
Adaptive Solutions	383	Beaverton, OR	(503) 690-1236	CNAPS series	$2995
Advanced RISC Machines	384	Los Gatos, CA	(408) 399-5195	BlackICE	<$1000
Aeon Systems	385	Albuquerque, NM	(505) 828-9120	VMEAlpha64/SP	$16,875
American Arium	386	Tustin, CA	(714) 731-1661	ICE-15, -154	$33,000
Applied Microsystems	387	Redmond, WA	(206) 882-2000	EL 3200	$17,200
Ariel Corp	388	Highland Park, NJ	(908) 249-2900	AXDS-510	$2495
Avalon Computer	389	Santa Barbara, CA	(805) 965-9559	Alphacard	$9900
Biomation	390	Milpitas, CA	(408) 435-7800	CLAS4000/D	$10,000
BSO/Tasking	391	Dedham, MA	(617) 320-9400	Various	
CARDtools Systems	392	Sunnyvale, CA	(408) 559-4240	T-N-T Sim	$7000
Coactive Aesthetics	393	San Francisco, CA	(415) 626-5152	GCB11	$149
Comdisco Systems (now Alta Group)	394	Foster City, CA	(415) 574-5800	SPW MultiProx	$25,000 $15,000
Concurrent Computer	395	Oceanport, NJ	(908) 870-4500	Maxion system	
Concurrent Sciences	396	Moscow, ID	(208) 882-0445	Soft-Scope	$1500
CSPI	397	Billerica, MA	(508) 663-7598	SuperCard development environment	$25,000
Diab Data	398	Foster City, CA	(415) 571-1700	D-tective	
Digital Equipment	399	Maynard, MA	(800) 297-4863	DEC OSF/1	$1250
Drumlin	400	Glendale, CA	(818) 244-4600	CTS, CTK	$395
dSPACE GmbH	401	Paderborn, Germany	5251-1638-0	DSP1201	$11,500
Embedded Performance	402	Santa Clara, CA	(408) 980-8833	CCE29K	$4900
Emulation Technology	403	Santa Clara, CA	(408) 982-0660	ET-iC8plus	$2690
Eyring	404	Provo, UT	(801) 375-2434	PDOS	$3000
General Micro Systems	405	Rancho Cucamonga, CA	(909) 980-4863	GMS V64	$4995
Green Hills Software	406	Santa Barbara, CA	(805) 965-6044	Green Hills C	$1500
Hewlett-Packard	407	Santa Clara, CA	(800) 452-4844	16500B 64700 System	$10,600 $23,970
Heurikon Corp	408	Madison, WI	(608) 831-0900	Nitro60	$5495
Hitex GmbH	409	Karlsruhe, Germany	721 9628-0	Teletest 32	$15,950
Huntsville Microsystems	410	Huntsville, AL	(205) 881-6005	HMI-200-68000 SourceGate II	$10,000
Integrated Systems	411	Santa Clara, CA	(408) 980-1500	pSOSystem	$9150
Intel	412	Santa Clara, CA	(800) 628-2283	GNU960 CTools960 iRMX III	$600 $2000 (DOS) $9795
Intermetrics Microsystem Software	413	Cambridge, MA	(617) 661-0072	Precise Solution	$8500
ITCN	414	Dayton, OH	(513) 439-9223	C-TAC	$29,950
JMI Software Systems	415	Spring House, PA	(215) 628-0840	C Executive	$2500
KADAK Products Ltd	416	Vancouver, BC	(604) 734-2796	Insight	$695
Lloyd I/O	417	Beaverton, OR	(503) 222-0702	Vantage	$1195
Mercury Computer	418	Chelmsford, MA	(508) 256-1300	SuperVision	$5500
Micro Digital	419	Cypress, CA	(714) 373-6862	386 smx smxNet	$4000 $5000

WITH WORD LENGTH ≥32-BITS[1,2]

Description
Assembly, C, and multitasking debuggers for real-time kernel supporting 32-bit µPs.
ISA-bus and VMEbus boards with up to 512 DSPs
In-circuit emulator based on on-chip debug features of ARM7 32-bit RISC core.
VMEbus development board for 150-MHz DEC Alpha µP. Optional i960 I/O processor.
Logic analyzers and ICEs for Pentium at 100 MHz
ICEs for i960CA/CF, 68xxx, and 683xx series.
Debug software for Hydra II VMEbus DSP coprocessor board, which contains four C40s.
Parallel-processor module with Alpha µP.
Logic-analysis system with support for 32-bit processors and multiprocessing.
C compilers, debuggers, and ICEs for 32-bit µPs.
CASE tools for complex real-time projects.
Networked HC11 microcontroller card.
Signal Processing WorkSystem. MultiProx C-code generator partitions block diagrams for execution on multiple DSPs.
Multiprocessor system using 150-MHz R4400s.
Remote-target debugger for X86 family.
Heterogeneous mixed-multiprocessing point-and-dlick, X11-based debugger, system and emulation software, simulator, RTOS kernel.
Debugging tools for 68060.
Full Unix environment for real-time applications of Alpha AXP µPs.
Communications coprocessor; software tools.
DSP coprocessor boards and software tools; DSP1201 board has multiple TMS320C40s.
Development tool kit for Am29K RISC family.
8-bit ICE usable for multiprocessor systems.
RTOS; native and cross-development tools.
VMEbus SBCs that accept 32- and 64-bit CPUs.
Optimizing compiler; multiprocessor support.
500-MHz logic-analysis system expandable to 680 channels with 1M-frame memory. ICE; supports many 32-bit CPUs; supports developing homogeneous and heterogeneous multiprocessor systems via intermodule and coordinated measurement buses.
VMEbus CPU board based on 68060. Vendor supports and licenses VxWorks RTOS.
ICE; supports heterogeneous multiprocessing.
ICE and debug software for 68xxx series.
Development environment based on pSOS+M real-time multiprocessing kernel.
C compiler, assembler, linker, and debugger. C compiler, assembler, linker, utilities, and library support. (Both are for i960.) Development kit for i386, i486, and Pentium using iRMX RTOS and SoftScope III debugger.
C cross compiler, task-aware source-level debugger, simulator; multiprocessor support.
Embedded-system profiler and ICE for 680X0, 683XX, i960, X86, R3000/4X00, and buses.
Binary development package for most popular 32-bit CISC, RISC, and DSP families. Based on real-time multitasking kernel.
Software debug tools for 32-bit µPs.
Development system used with networked CPUs.
Debugger for vendor's RACE real-time embedded multicomputers.
Real-time embedded kernel for i386. TCP/IP stack for use with smx.

Table continued on pg 70

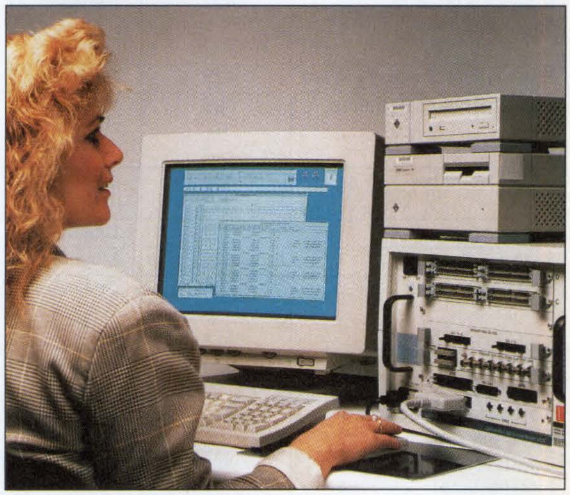
- The turnaround of the two classes of functions are radically different. Usually, operator-interface activities have time scales in tens or hundreds of milliseconds. Real-time functions are likely to require response times measured in microseconds.
- Deciding which tasks should be assigned to a specific processor is not complicated; with just a moment's thought, you can usually determine which functions relate to the operator interface and those involved in real-time control.
- The interprocessor communication requirements are minimal. The data to be passed between the real-time and user-interface processors often will not severely tax an RS-232C port operating at 19.2 kbps. If greater speed is needed, it rarely exceeds a bidirectional parallel port's capabilities. If the 2-processor system must communicate with a still higher-level system by way of, say, an Ethernet network, also using Ethernet for communications between the real-time and user-interface processors sometimes makes sense.

Note that in this 2-processor example, each processor has its own memory; the processors share no memory. Moreover, each processor has its own operating system (OS), quite often a compact real-time kernel. If the user interface is based on a graphical interface, such as X.11, the user-interface processor might run under a full-blown, real-time operating system (RTOS).

Symmetry is beauty

Though some people consider this 2-processor example to be trivial, it is, in fact, both useful and workable and is an example of a "symmetric" multiprocessing system. The characteristics that earn it that title are that neither processor is in control of the other and that both processors have their own OS. In a symmetric multiprocessing system, the OSs on the several processors can be the same or different.

The two processors in this example can be of the same type (homogeneous multiprocessing) or of different types (heterogeneous multiprocessing). Because the processors do not share memory, byte ordering usually doesn't cause problems. When a heterogeneous multiprocessing system employs shared memory, byte-ordering differences among the several µPs can cause trouble, which is the so-called little endian/big endian issue: Is the most significant byte first or last? Is the most significant *bit* on the left or the right? You must reconcile such differences. And any method you choose, whether hardware- or software-based, will slow your system.



The configuration flexibility of high-end logic-analysis systems such as Biomation's CLAS 4000 lets you bring multiple cross-triggered analyzers to bear on thorny hardware problems in multiprocessor systems. Because one unit can contain several analyzers, the setup is more compact and less intimidating than you might expect.

Byte ordering notwithstanding, assigning different processes, tasks, or threads to different CPUs is usually fairly straightforward. It is, however, far from the only way to divide a computing problem among µPs. Another approach is parallel processing. Here, multiple CPUs divide the work related to a single task. Probably the most common example of parallel processing, particularly in embedded systems, is in DSP.

When performed by a single processor, many DSP operations consist of iterative loops. Even when the results of one iteration are needed for the next, it is often possible to speed an

Table continued from pg 69

TABLE 1—SUPPLIERS OF EMBEDDED-SYSTEM DEVELOPMENT TOOLS THAT SUPPORT MULTIPROCESSING AND/OR μPS

Company	Circle No.	Location	Phone	Product	Base US Price[3]
Microtec Research	420	Santa Clara, CA	(408) 980-1300	Spectra	$2500
Microtek International	421	Hillsboro, OR	(503) 645-7333	MPE, MPT	$15,000
Microware Systems	422	Des Moines, IA	(515) 224-1929	FasTrak	$14,500
Motorola	423	Austin, TX	(512) 891-2000	M68MEVB1632	$1295
Object Technology International	424	Ottawa, ON	(613) 820-1200	Envy/Developer	$12,000
Pentek Inc	425	Norwood, NY	(201) 767-7100	SwifTools	$1000 (DOS)
Performance Computer	426	Rochester, NY	(716) 256-0200	PT-VME161	
Precise Software Technologies	427	Nepean, ON	(613) 596-2251	Precise/ MQX+M and others	$10,000
Promark Technology West	428	Sunnyvale, CA	(408) 733-0272	Kontron KSE5	$22,000
QNX Software Systems	429	Kanata, ON	(613) 591-0931	QNX V4.2	$795
SGS-Thomson	430	Lincoln, MA	(617) 259-0300	IMSD7314 Windows version	$1750
Signalogic	431	Dallas, TX	(214) 343-0069	DSPower	
Signum Systems	432	Mountain View, CA	(415) 903-2220	USP-380	$6495
Sky Computers	433	Chelmsford, MA	(508) 250-1920	Skyvec, Skybolt	From $20,000
Softaid	434	Columbia, MD	(410) 290-7760	UEM series	$5500
Software Development Systems	435	Oak Brook, IL	(708) 368-0400	CrossCode SingleStep	$2000 $1500
Sonitech International	436	Wellesley, MA	(617) 325-3824	Brahma	$4500
Spectron Microsystems	437	Goleta, CA	(805) 968-5100	SPOX	$12,000
Standing Applications Laboratory	438	Kirkland, WA	(206) 453-7855	DSP Lab One	$3295
Star Semiconductor	439	Warren, NJ	(908) 647-9400	SprocLab V1.4	$5460
STEP Engineering	440	Sunnyvale, CA	(408) 733-7837	Eclipse 29K	$10,000
Systems and Software	441	Irvine, CA	(714) 833-1700	OMF, SP, CV tools	From $595
Tartan Inc	442	Monroeville, PA	(412) 856-3600	IPS	
Tektronix	443	Beaverton, OR	(800) 426-2200	TLA520 DASXPD2 DASNTD2	$30,000 $46,800 $46,800
Texas Instruments	444	Houston, TX	(713) 274-2320	TMS320C80 development tools	$30,000
Transtech Parallel Systems	445	Ithaca, NY	(607) 257-6502	TTM200	$9945
US Software	446	Portland, OR	(503) 641-8446	SuperTask!	$3500
VenturCom	447	Cambridge, MA	(617) 661-1230	Venix SVR 4.2	$6300
White Mountain DSP	448	Nashua, NH	(603) 883-2430	Mountain-40 Mountain-510 PPDE	$3995 $3495 $495
Wind River Systems	449	Alameda, CA	(510) 748-4100	VxMP WindView	$3995 $4995
Ziatech	450	San Luis Obispo, CA	(805) 541-0488	STD 32 Star System	$4500

Notes: 1. Some of the listed vendors are suppliers of multiprocessing hardware.
2. Despite its length, the listing is not comprehensive; vendors and products shown are representative only.
3. Where a vendor has indicated a range of prices or prices for several products, the price shown is the lowest one.

SUPER CIRCLE NUMBER

WITH WORD LENGTH ≥32-BITS[1,2]

Description
Cross-development "backplane" with multiprocessor support.
Pentium ICE and hardware-assisted debugger.
Development environment for OS-9 RTOS. Supports 680X0, 683XX, 386 to Pentium, PowerPC.
Evaluation boards for CPU32 and CPU32+.
Multiuser object-oriented development environment. Supports heterogeneous multiprocessing, Smalltalk+C tools.
Multiprocessing symbolic C debugger for DSP boards (mainly C30- and C40-based).
68060-based VMEbus board.
Multiprocessor real-time executive for 680X0, 683XX, 320CX0, X86. Cross-debugger for distributed and multiprocessing.
ICE; supports 32-bit μPs and multiprocessing.
Development system; works with Watcom C compiler (V9.5). Supports X86 μPs. Supports multiprocessing using X86 μPs.
Cross-development tools for Transputer family. Includes compiler/configurer and post-mortem debugger.
Windows development system for 32-bit DSPs.
ICE usable with networked processors.
Development environment for vendor's parallel-processing hardware—VMEbus boards and systems that perform to 20 Gflops.
ICEs for many μP families. Support multiprocessing with all supported μPs.
C and C++ compilers for 680X0 family. Debugger for CrossCode.
ICE for TMS320C40. Uses IEEE-1149.1 port. Single unit supports multiple μPs.
DSP development system for Analog Devices, Motorola, and TI chips. Supports multi-DSP systems; provides links to host CPU.
Integrated development system with four TMS-230C51s and one TMS34010.
Software tools for multiprocessing systems based on vendor's Sproc DSP chip.
ICEs for Am 29K family.
Individual C/C++ tools and tool sets for X86 μPs in real and protected modes.
Coordinates Ada programs between 68xxx μPs and Cx and C4x DSPs.
Digital-analysis (logic-analysis) systems. Handle many vendors' μPs, including Alpha, MIPS, Pentium, and SPARC. Handle multiprocessing with any supported μPs.
Simulator, emulator, and DSP C debuggers for the MVP chip, which includes a RISC master processor processor, four 32-bit DSPs, a video controller, and a crossbar interprocessor interface.
Parallel-processing module that includes an i860XP and a T805 Transputer.
RTOS and related tools for developing i960, MIPS, SPARC, 680X0, and 683XX applications.
Development environment for 386 to Pentium.
ISA-bus evaluation module, universal emulators, and parallel-processing debug environment for TI DSPs.
Multiprocessing extension of VxWorks RTOS for 680X0, 683XX, i960, 386, R3000, SPARC. Software logic analyzer for 680X0 and 683XX.
Multiprocessor, multitasking system made up of up to seven 486 CPUs on STD 32 cards.

For more information on tools available from all of the vendors in this table, you need only circle one number on the postage-paid reader service card. **Circle No. 451**

operation substantially by dividing it among several processors. If necessary, these can operate in a pipelined fashion: A processor passes the result of its computation to a neighbor, which performs more of the computation. The first processor then operates on the next datum. Of the four multiprocessor chips mentioned previously, three incorporate multiple DSPs.

Two classes of applications

Many parallel-processing DSP applications have something in common with the simple multitasking application discussed earlier—in which one μP handles the real-time tasks and a second processor handles the user interface. Partitioning the workload among the several processors is fairly easy. Indeed, if you think about the effort required to partition the work, multiprocessing applications seem to fall into two categories: those that the human mind can easily divide among multiple processors and those that defy this simple approach to apportioning work.

For complex signal-processing jobs that do not easily break into portions several processors can handle, help is at hand. You can now obtain parallelizing compilers that divide the work efficiently. Though products with the same purpose have been available for parallel supercomputers for some time, these software products are relatively new to the embedded-systems world. (Their proper—albeit jawbreaking—name is parallelizing, vectorizing compilers.) They are extensions of vectorizing-compiler technology, which has existed for 20 years or more, dating back to the days of minicomputers and add-on vector- or array-processor units.

Vectorizing compilers take operations that would have been performed sequentially and combine the data into longer words that a suitable processor can handle in one clock cycle (or a few cycles). Examples of processors that support this vector-processing approach are the PowerPC, the Alpha AXP, the R4000, the i860, and the SPARC family. These RISC μPs use so-called superscalar architectures.

Parallelizing compilers divide vectorized data into portions and route different portions to different processors. These compilers are hardware-specific; they work with vector-processing hardware available from the processor vendor. Currently, several vendors offer VMEbus-based vector-processing systems that use multiple i860s (In **Table 1**, see CSPI, Mercury Computer Systems, and Sky Computers).

Sometimes, 2×2=<<4

The figure of merit for parallelizing compilers is scalability. Ideally, a system having four processors would perform a designated operation on a given data set 4 times as fast as a system that uses one processor of the same kind. If the system has eight processors, it would perform the operation 8 times as fast. In practice, a 4-processor system is less than 4 times as fast as a 1-processor system, and an 8-processor system is less than 2 times as fast as a 4-processor system. Scalability measures just how much less than linearly the speed increases as you add processors.

It is not uncommon to find 10-processor configurations whose performance is only 15% of the ideal; that is, 10-processor systems that are only 1.5 times as fast as 1-processor systems. Sky Computers claims that its parallelizing compiler represents the state of the art and that it turns in scores of roughly 50 to 70% of the ideal, even in configurations having 10 processors or more.

Hardware and software from companies such as Sky find their way into some fascinating applications. Some are military and are classified. Several involve pattern recognition in medical imaging systems. One even involves recognizing commercials in radio broadcasts (see **box**, "Signal processors listen to the radio").

Such applications are not mass-marketed. The developers usually build a few systems—sometimes hundreds. When unit quantities rise to 10,000 or more, the companies take different hardware approaches; for example, they design special-purpose chips. But for products built in smaller quantities, using programmable general-purpose processors has significant advantages. The most obvious of these advantages is ease of modifying the code as the developers and their customers gain experience with the application.

PERVASIVE COMPUTING

A good example of an application well-suited to the programmable general-purpose-processor approach is compression of full-motion video images. The idea behind image compression is to minimize the bandwidth needed to transmit images or the amount of memory needed to store them. Once you have an image in compressed form, you must decompress it before you can display it. The compression and decompression problems are quite different. Unlike image compression, image decompression is clearly a job for a special-purpose chip. Millions upon millions of such chips will be required—one for every TV set. Compressing the images is a different story. The number of TV and movie studios around the world is much smaller than the number of TV sets.

Compressing moving images also involves far more complex computations than does decompressing them. For instance, image compression can involve cross-correlating frames with other frames. Cross-correlation establishes that an object has moved and indicates where it has moved. In most full-motion-video applications, such mathematical operations must be done in real time.

Even though correlation of successive frames can easily take more time than is available between frames, parallel processing can allow the mathematical operations to keep up with the incoming data. If a new frame appears every 33 msec and the math takes 330 msec, you might assign the work to 10 processors in round-robin fashion. Although no one processor could keep pace with the incoming data, the 10 processors could; their output would be delayed with respect to their input by 330 msec, however.

In comparison, reconstruction is much less demanding. A complete representation of a moving object (at least one whose shape doesn't change as it moves) requires only one instance of the data set that describes the object—not one instance per frame. Even less information is needed to describe the object's trajectory. Moreover, the mathematical operations are much less complex than correlation; for example, you might simply replicate the original image at the proper location in each frame. Most likely, a single processor could handle this task.

Tools are us

Parallelizing compilers are just one of many types of tools available for developing multiprocessing systems. **Table 1** lists a wide variety of tools, both hardware- and software-based, from more than 60 vendors. These tools support the development of multiprocessor systems of all types and of single-processor systems based on μPs whose word length is at least 32 bits. Although we do not set out to list suppliers of multiprocessor hardware, some of the vendors that responded to our survey supply such hardware, and we list them. Our queries emphasize our interest in tools. For example, we asked RTOS vendors to supply information on tools associated with their RTOS products, not on the OSs themselves.

RTOSs hold the key to simplifying the development of many multiprocessor systems. With an appropriate operating system and development environment, developers of multitasking software need not be aware of whether they are writing code that will run on a single μP or on multiple μPs.

At some point in the debugging process, though, you probably have to be quite clear about where different tasks are running. It is entirely possible for bugs in code running on one μP to cause another processor to hang up. Meanwhile, the μP whose code contains the bug might continue to run. Tools such as logic-analysis systems that contain multiple cross-triggered logic analyzers in a single unit are well suited to debugging problems of this sort. EDN

Contact Senior Technical Editor Dan Strassberg at (617) 558-4205; fax (617) 558-4470. E-mail: EDNStrassberg@MCIMAIL.COM EDN BBS: EDNStras.

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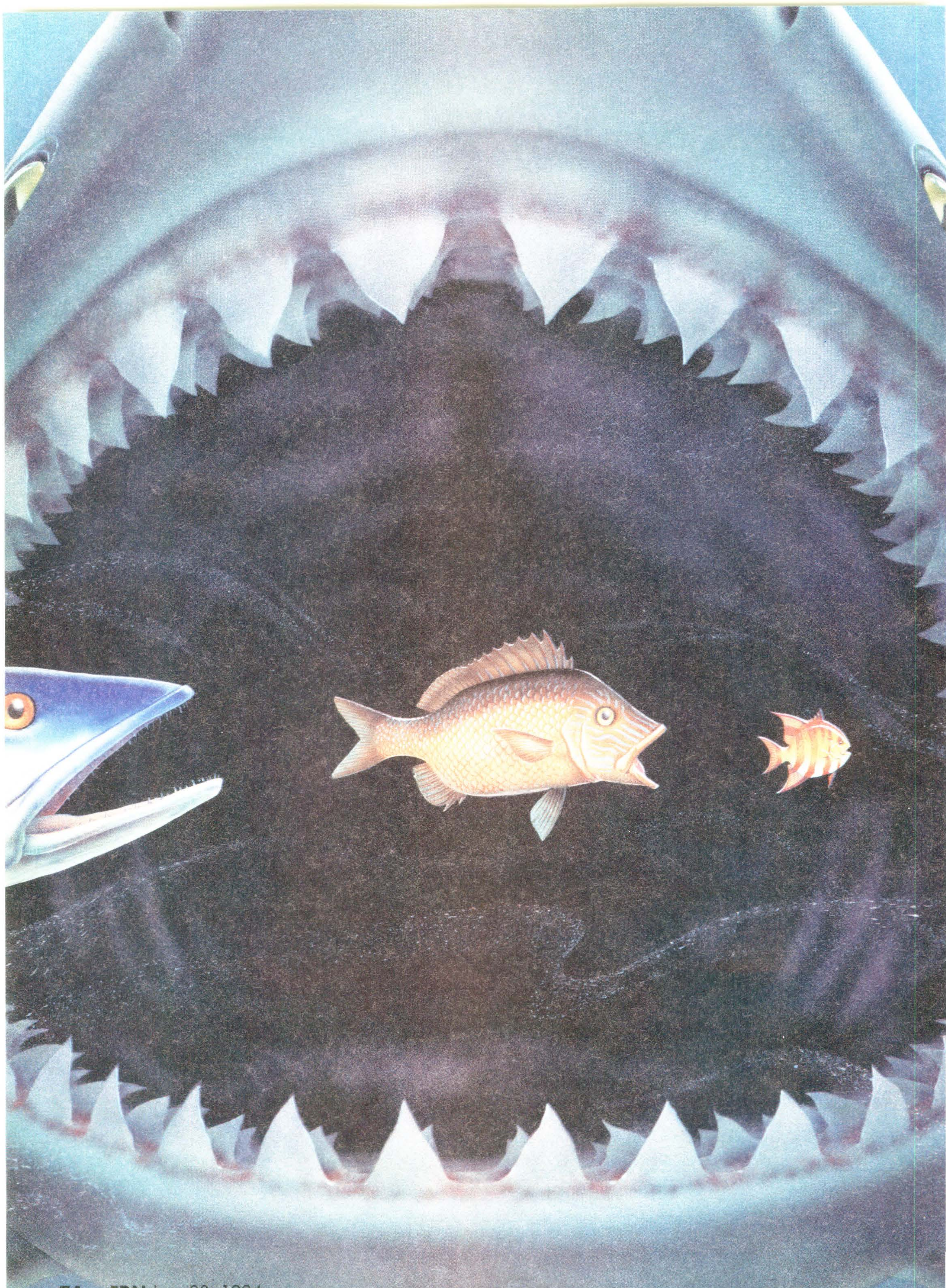
LOOKING AHEAD

With processor speeds increasing almost daily, you're apt to wonder why anyone in the embedded-systems world should have to build a multiprocessor system. (Even if you concede that such systems are necessary today, you may be skeptical about the need for them next year.)

In fact, though, the need for multiprocessing is increasing. Especially in signal processing, the demand for computing power is rising more rapidly than μP performance. Fortunately, like all types of computing hardware, multiprocessing hardware continues to become smaller and more affordable. Thus, on the hardware side, there is no real barrier to using multiprocessing in embedded systems. The barriers that exist are with the tools and software. From the length of **Table 1**, it's fairly obvious that finding the right tools for your development job is no trivial task.

But things are looking up. The number of embedded systems produced each year will continue to grow dramatically, and the percentage of those employing multiprocessing in some form should at least hold constant. There should be increases in both the number of system types and the average number of systems of any type that are shipped. Meanwhile, continued declines in the average selling price of single systems should spur demand even further.

These trends point to an increase in the potential payoff to suppliers of software and tools for multiprocessor embedded-systems development. The possibility of greater rewards should encourage suppliers to offer a greater variety of software and tools. Barriers to multiprocessor-system development that currently result from limited software and tool availability will weaken. Though the barriers won't disappear, they will become less significant. The bottom line is that developing multiprocessor systems will become easier.



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MCM6729A*	MCM6706A	MCM6705A	MCM6708A
256K x 4 bit	32K x 8 bit	32K x 9 bit	64K x 4 bit
8, 10, 12, 15ns	8, 10, 12ns	10, 12ns	8, 10, 12ns
MCM6709A*	MCM6706R	MCM6709R	
64K x 4 bit	32K x 8 bit	64K x 4 bit	
8, 10, 12ns	6, 7, 8ns	6, 7, 8ns	

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1 Meg TTL I/O
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☐ 128K x 8 ☐ 10ns
☐ 12ns

256K TTL I/O
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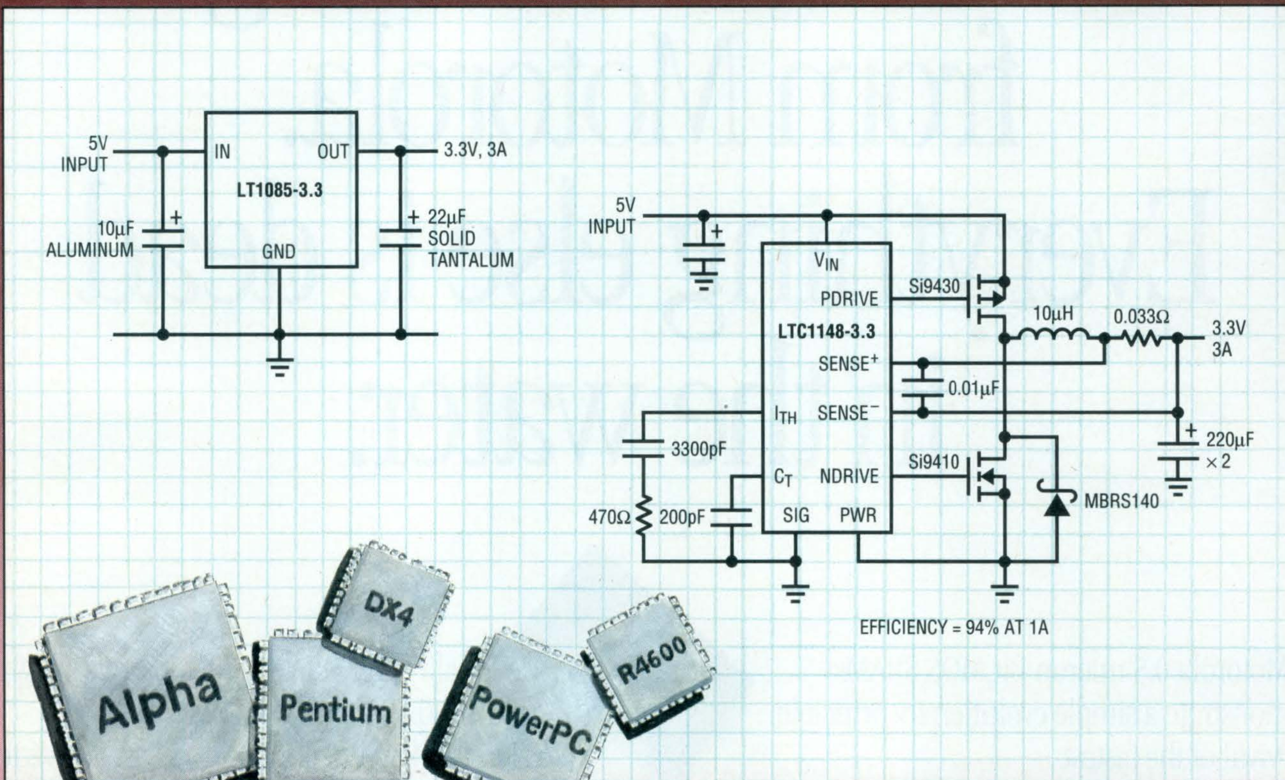

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3A	LT1085-3.3	LTC1148-3.3
5A	LT1084-3.3	LTC1148-3.3
7.5A	LT1083	LTC1148-3.3
10A	LT1087 (X2)	LT1158
15A (20A Peak)	N/A	LT1158

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CIRCLE NO. 33

EDITED BY CHARLES H SMALL & ANNE WATSON SWAGER

Cell-cycler sorting sires superior batteries

Bob T Pham, Lockheed EVAS, Houston, TX

To assemble superior NiCd batteries, you need to *form* and *match* the individual cells making up a battery. First, formation takes place in a NiCd cell only after numerous charge-discharge cycles. Second, you must collect voltage data during these cycles to match up cells having uniform characteristics.

To keep costs under control and to minimize human error, the circuit in **Fig 1** processes cells in batches. **Fig 1** shows a single cell channel. You can place as many channels on a pc board as suits your purposes. The ZIPfile attached to **EDN BBS /DI_SIG #1446** contains a write-up of this Design Idea and the circuit diagram in OrCAD format.

In addition to the circuit, you will need a computer-controlled, data-acquisition system to cycle the cells and record data. If you were to build a pc board bearing 16 channels to handle 16 NiCd cells simultaneously, for example, your data-acquisition system would need one digital output per channel (D_1), one digital output per pc board (D_2), one analog output per board to set the charging rate, and one analog input per cell.

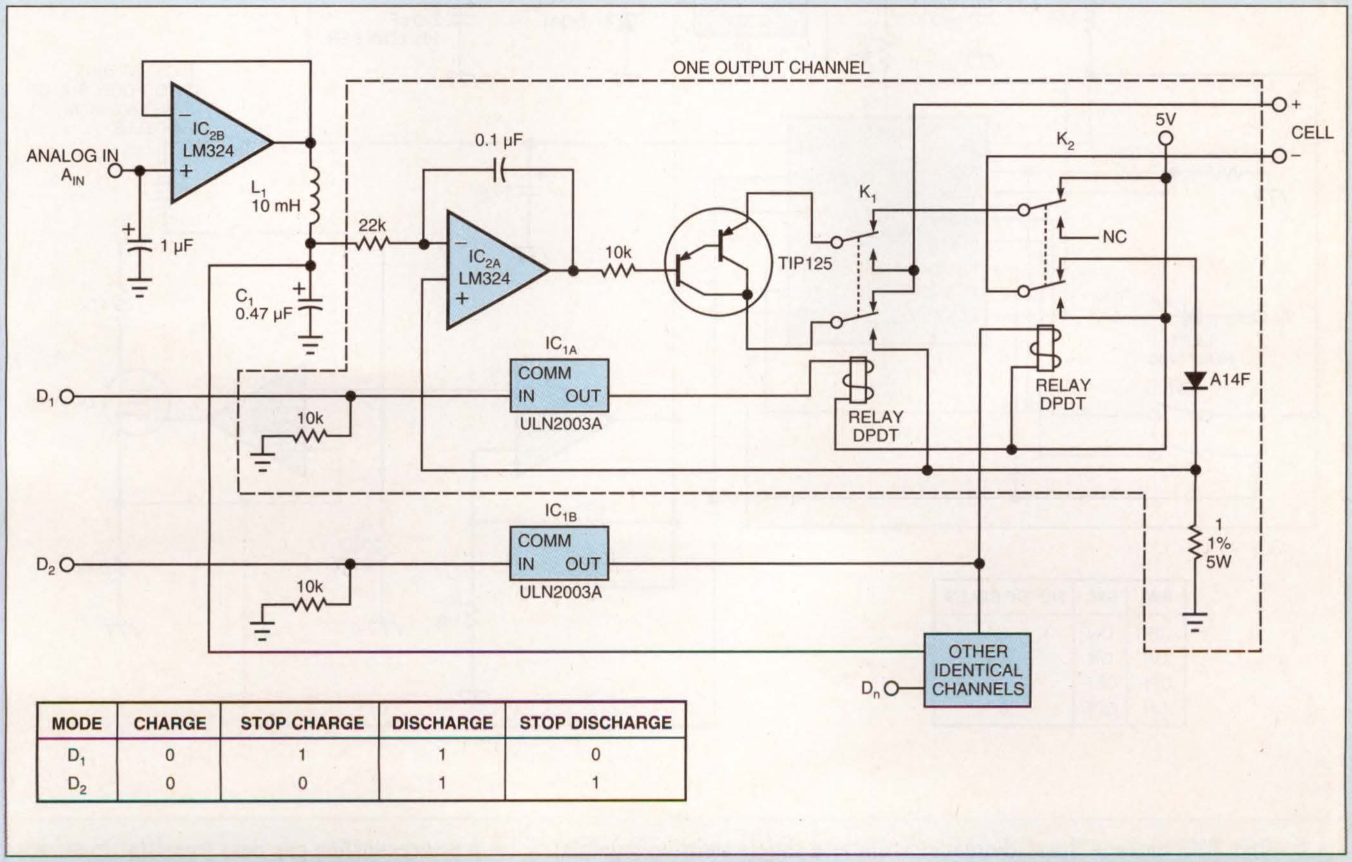
As the system performs timed cycling, it records individual cell voltages—the only data it needs. The system can then calculate each cell's internal impedance using dV/dI and calculate each cell's capacity in ampere-hours (Ahr). Further, the computer can determine each cell's voltage-cutoff point during discharging.

The circuit provides closed-loop current regulation. The master analog-input voltage, A_{IN}, dictates the magnitude of charge or discharge currents—1V=1A. IC_{2B} buffers the analog-input voltage. Because all channels on the pc board use the same analog-input voltage, the LC filter, L_1 and C_1, minimizes reflected noise.

A 5V power supply provides up to 2.5A charging current. Digital input D_2 configures relay K_2 for charge or discharge. All channels share D_2. Digital input D_1 controls each channel's current flow.

Applying a high input to both D_1 and D_2 (the controlled-discharge state) causes the relays to place the 5V supply in series with the cell to bring the effective voltage to 6.2V nominal. The relays also create a path that allows the cell to discharge through the same circuit that charges it. The 6.2V ensures that the cell maintains a constant discharge current. (DI #1446) EDN

To Vote For This Design, Circle No. 452



MODE	CHARGE	STOP CHARGE	DISCHARGE	STOP DISCHARGE
D_1	0	1	1	0
D_2	0	0	1	1

Fig 1—This circuit processes cells in batches so you can assemble matched NiCd batteries.

Switcher IC hikes battery charger's efficiency

Huw Jones, Gyrus Medical Ltd, Cardiff, Wales, UK

The adjustable switching-regulator LM2575T-ADJ, IC_1, in **Fig 1** replaces a power-wasting pnp transistor in the databook design for the NiCd battery charger IC_2, a MAX713. (Its sister device, the MAX712, handles NiMH cells.) IC_2 "fast-charges" cells by monitoring the cell's voltage and charging current until they exhibit subtle anomalies that signal a fully charged cell. Because the circuit charges at only a 1.5C rate, the circuit does not need to sense the cell's temperature. (A 1C, or "standard," rate signifies charging the battery to its full capacity in 1 hour.)

The circuit in **Fig 1** fast-charges 500-mAhr AA NiCd cells. Depending on the setting of SW_1 and SW_2, the circuit handles two to eight cells, providing the circuit's input voltage is at least 15V; at higher voltages, power IC_3 from IC_2's pin 15. Charging starts when you plug in the battery. When the battery is fully charged, LED1 extinguishes, and the charger switches to trickle-charge mode.

The circuit employs IC_2 purely as a charge controller; IC_2 supplies the actual charging current to the battery. Experiments show that IC_1's control loop is several orders of magnitude faster than IC_2's. Therefore, a closed-loop system using IC_2's DRV pin to control IC_1's regulation proves unstable. Instead, IC_1's feedback loop tries to maintain a voltage across C_1 that results in a 1.25V signal at IC_1's FB pin.

R_1 sets the charging current. Select sense resistor R_2, which is in series with the battery, so that it develops 0.25V at the proper charging current (corresponding to 750 mA in this implementation). IC_{3A} scales this sense voltage for IC_1, and IC_{3B} buffers the sense voltage for IC_2. (IC_{3B} must supply IC_2's expected –BATT voltage).

Because IC_1 is a switcher, it's efficiency is about 85%, and it needs no heat sink to pass charging currents under 1A. (DI #1447) EDN

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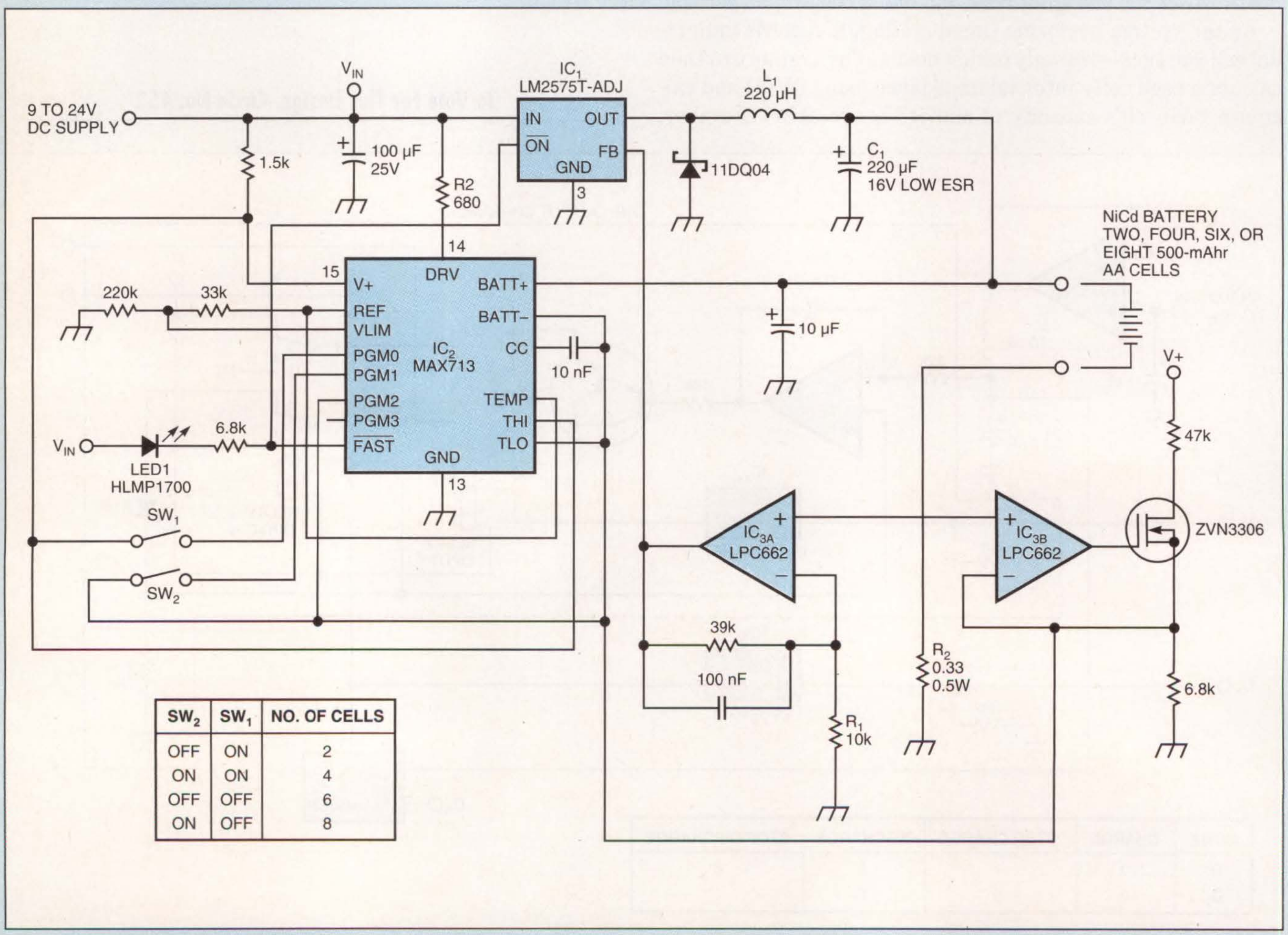

SW2	SW1	NO. OF CELLS
OFF	ON	2
ON	ON	4
OFF	OFF	6
ON	OFF	8

Fig 1—This NiCd battery "fast" charger substitutes a simple switcing-regulator IC for a power-wasting pnp pass transistor to increase efficiency.

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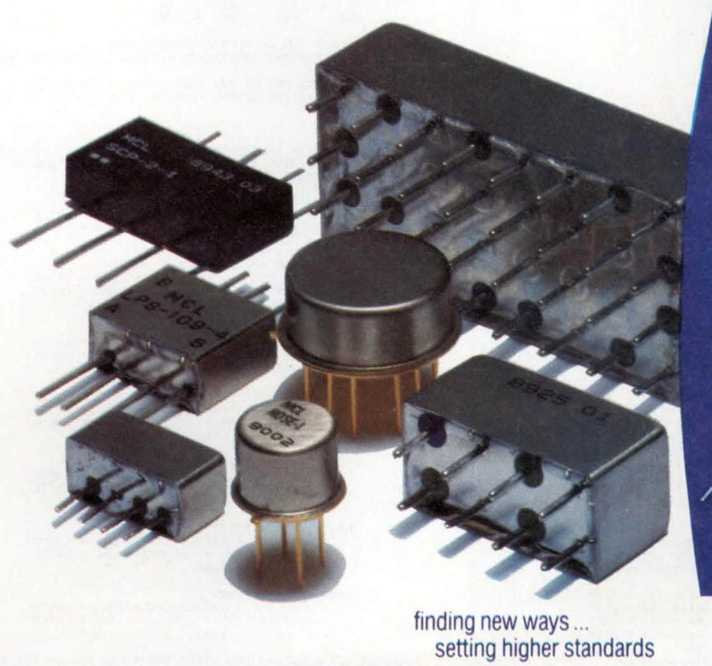

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F134 Rev D

CIRCLE NO. 93

PLDs eliminate ISA pc-board's jumpers

Vladimir Bochev, Bulgarian Academy of Sciences, Sofia, Bulgaria

Having software ask users about base addresses for newly installed ISA-bus (industry-standard-architecture, ie, the IBM PC bus) pc board is far more elegant than requiring the users to decipher HEX address and set pc-board jumpers. GAL20R8 PLDs, programmed according to **Listings 1** and **2**, along with an 8-bit comparator allow software to set pc boards' base addresses.

The comparator has one input tied to the ISA address bus and the other to one of the PLDs. This PLD contains a register initialized to some base address on power-on. The second PLD contains a "table" (actually, a Boolean formulation) of available base addresses.

The first time an I/O address matches an address from those stored in the second PLD, the register PLD latches this I/O address as the pc board's base address, holding it until the PC gets a hardware reset.

Once all new pc boards are functioning without I/O-address conflicts, the setup software can insert a simple program retaining the selected addresses and signature into *autoexec.bat*. The ZIPfile attached to **EDN BBS /DI_SIG #1428** contains a writeup of this design and the PLD files in plain ASCII.

A problem remains when a user installs two pc boards with the same factory-set base addresses. This design cannot distinguish between such boards. You can also supply a unique signature with each pc board—perhaps merely a number printed on the board and in the documentation. In this case, the setup software makes a write to the base address with a data value equal to the signature. Only the board whose signature matches the one sent can latch the contents of the ISA address bus.

Many variations of this basic design are possible, including changing the board's base address on demand (a somewhat dangerous possibility). You can implement the base-address table in a PROM for a larger address span and even an EEPROM for extreme flexibility.

Of course, you must have some clock source for the GAL20R8s to operate. If your design is "clockless" or has only some very low-rate clock compared with the bus' addressing speed, you can draw high-speed pulses from the ISA bus itself. (DI #1428)

To Vote For This Design, Circle No. 454

Listing 1—I/O-logic PLD program

```
TITLE PC ARBITER AND AUTOBOARD
PATTERN M
REVISION 001
AUTHOR  VLADIMIR BOCHEV

CHIP    PC_DSP_ARB      PAL20L8

;PINS   1       2       3       4       5       6       7       8
        A0      A1      A2      A3      A4      A5      A6      A7

;PINS   9       10      11      12
        A8      A9      IOR     GND

;PINS   13      14      15      16      17      18      19      20
        IOW     AEN     RD_STAT XF      RS      PS      HOLDA   TMS_A10

;PINS   21      22      23      24
        EXT_A10 AR_OUT  BRD_SEL VCC

;TMS_A10 = THE A10 ADDRESS LINE INPUT FROM THE ON-BOARD uP
;PS = PROGRAM SELECT SIGNAL FROM THE ON-BOARD uP
;AEN, IOR, IOW, A3 ... A9 = PC SLOT SIGNALS
;EXT_A10 = THE "PROCESSED" ADDRESS LINE TIED TO THE MEMORY CHIPS
;AR_OUT = ADDRESS RANGE OUT SIGNAL FOR THE AUTOMATIC BOARD BASE ADDRESS
SELECT

EQUATIONS

        XF.TRST = GND
        RS.TRST = GND
        PS.TRST = GND
     HOLDA.TRST = GND
   TMS_A10.TRST = GND
        ;THE ABOVE PINS ARE USED AS INPUTS

        EXT_A10.TRST = RS * HOLDA
        ;TO BE A REAL ADDRESS PIN EXT_A10 IS THREE-STATED WHEN IN RESET
        ;OR HOLD
        /EXT_A10 = /TMS_A10 + PS * /XF
        ;EXT_A10 FOLLOWS TMS_A10 EVERY TIME THE PS IS LOW BUT
        ;CAN BE FORCED TO LOW BY THE XF PIN ON DATA MEMORY ACCESS
        ;THE LACK OF MORE PINS DOES NOT DISABLE THE XF ACTION ON BR VALID

        /AR_OUT = /IOR * A9 * A8 * /A7 * /A6 * /A5 * /A4 * /A3 * /AEN
                + /IOR * A9 * A8 * /A7 * /A6 * /A5 * /A4 *  A3 * /AEN
                + /IOR * A9 * A8 * /A7 * /A6 * /A5 *  A4 * /A3 * /AEN
                + /IOW * A9 * A8 * /A7 * /A6 * /A5 *  A4 * /A3 * /AEN
                + /IOR * A9 * A8 * /A7 * /A6 * /A5 *  A4 *  A3 * /AEN
        ;A PULSE ON EACH OF THE BASE ADDRESS SHOWN. THIS IS THE
        ;AUTOSELECTOR PART OF THIS PAL

        /RD_STAT = /A2 * A1 * A0 * /BRD_SEL * /IOR
        ;READ STATUS OF THE PROCESSORS AT ADDRESS BASE + 3
```

Listing 2—Base-address "table" PLD program

```
TITLE PC-BOARD AUTOMATIC BOARD BASE ADDRESS SELECTOR
PATTERN P
REVISION 001
AUTHOR: VLADIMIR BOCHEV

CHIP    PC_DSP_AUTO             PAL20R8

;PINS   1       2       3         4     5       6       7       8
        CLK     AR_OUT  RESET_DRV A3    A4      A9      A5      A8

;PINS   9       10      11      12
        A6      A7      NC      GND

;PINS   13      14      15      16      17      18      19      20
        OE      NC      LATCH   RA7     RA8     RA9     RA6     RA5

;PINS   21      22      23      24
        RA4     RA3     NC      VCC

;A3 ... A9 ARE THE PC SLOT ADDRESS LINES
;RA3 ... RA9 ARE THE REGISTERED ADDRESS LINES GOING TO THE BOARD-SELECT
;COMPARATOR
;RESET_DRV = THE PIN OF THE SAME NAME ON THE PC BUS
;AR_OUT = THE FIRING SIGNAL FROM "M" PLD FOR THE AUTOLOADING BASE ADDRESS

EQUATIONS

        /LATCH := /RESET_DRV * /AR_OUT + /RESET_DRV * /LATCH
        ;SET TO HIGH AT RESET, FIRES ON AR_OUT LOW AND HOLDS THE
        ;LOW STATE UNTIL A NEW POWER ON

        /RA9 := GND * RESET_DRV
              + AR_OUT * /RESET_DRV * /RA9 * LATCH
              + /RESET_DRV * /AR_OUT * /A9 * LATCH
              + /LATCH * /RA9

        /RA8 := GND * RESET_DRV
              + AR_OUT * /RESET_DRV * /RA8 * LATCH
              + /RESET_DRV * /AR_OUT * /A8 * LATCH
              + /LATCH * /RA8

        /RA7 := VCC * RESET_DRV
              + AR_OUT * /RESET_DRV * /RA7 * LATCH
              + /RESET_DRV * /AR_OUT * /A7 * LATCH
              + /LATCH * /RA7

        /RA6 := VCC * RESET_DRV
              + AR_OUT * /RESET_DRV * /RA6 * LATCH
              + /RESET_DRV * /AR_OUT * /A6 * LATCH
              + /LATCH * /RA6

        /RA5 := VCC * RESET_DRV
              + AR_OUT * /RESET_DRV * /RA5 * LATCH
              + /RESET_DRV * /AR_OUT * /A5 * LATCH
              + /LATCH * /RA5

        /RA4 := GND * RESET_DRV
              + AR_OUT * /RESET_DRV * /RA4 * LATCH
              + /RESET_DRV * /AR_OUT * /A4 * LATCH
              + /LATCH * /RA4

        /RA3 := VCC * RESET_DRV
              + AR_OUT * /RESET_DRV * /RA3 * LATCH
              + /RESET_DRV * /AR_OUT * /A3 * LATCH
              + /LATCH * /RA3

;ALL REGISTERED EQUATIONS EXEPT THE FIRST FOLLOW THE SAME PATTERN.
;THE CORESPONDING OUTPUT IS FORCED TO A FIXED VALUE AT RESET (0x310
;HERE) AND HOLDS THIS VALUE UNTIL A FIRING CONDITION OCCURS.
;THEN THE REGISTER LOADS WITH THE NEW VALUE (WHICH MAY BE THE SAME AS
;POWER ON) AND HOLDS THIS VALUE "FOREVER", IE UNTIL A POWER SHUT DOWN
```

Dual microphones separate voice from noise

Samuel Kerem, Infrared Fiber Systems, Silver Spring, MD

The circuit in **Fig 1** uses a pair of microphones to extract a voice from a noisy background. You must mount electret microphones X_1 and X_2 on the left and right sides of the user's chest.

Sound sources not equidistant from the microphones experience a phase shift. Because sound travels at 1120 ft/sec, the maximum phase shift for this design's mounting scheme is about 0.5 msec. This phase shift corresponds to a 90° phase shift at about 1000 Hz. Thus, all sounds in the vocal frequency range, except the user's voice, tend to cancel.

IC_{1A} and IC_{1B} buffer the signals from the microphones. R_1 and R_2 provide the needed bias current for the electret microphones. R_3's and R_4's values determine the conversion coefficients. Choose R_3 and R_4 so that IC_{1A}'s and IC_{1B}'s outputs never saturate. The bipolar 4-quadrant multiplier, IC_2, separates the audio signal from the noisy background. R_5 and R_6 provide additional voltage gain after multiplication. R_7, C_1, R_8, and C_2 form a lowpass filter. (DI #1449)

To Vote For This Design, Circle No. 455

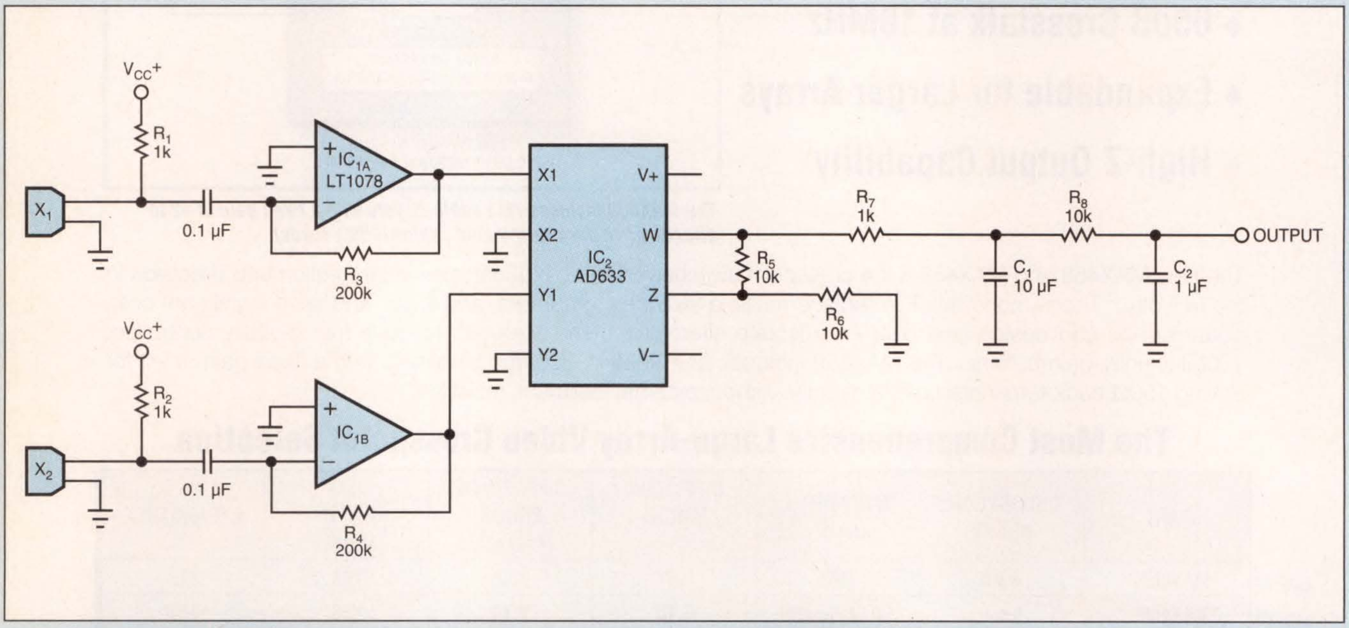

Fig 1—Two microphones placed equidistant from a user's mouth on the user's chest produce in-phase signals to this noise-canceling circuit's multiplier, IC_2, separating the users voice and out-of-phase signals from background noise.

Current-feedback amps square up fast signals

Rea Schmidt, Comlinear Corp, Fort Collins, CO

Using current-feedback amplifiers to convert signals from sine waves to square waves for DSP confers advantages over the more common comparator approaches.

Current-feedback amplifiers have wide bandwidths and relatively small and constant propagation delays. These small, constant delays help meet the setup-and-hold requirements of digital logic. Typically, current-feedback amplifiers have delays from 1.1 to 5 nsec.

The circuit in **Fig 1** overdrives its output to 32 times the input signal. Typical recovery times measure 2.8 nsec for a 0 to 2.2V step at the output. The delay measures 2.5 nsec.

Because current-feedback amplifiers' input stages operate in the linear mode, you can minimize the amplifiers' noise terms when sensing low input-signal levels. For the values in **Fig 1**, resistors R_1, R_2, R_3, and R_4 clamp the output's voltage swing from zero to a positive voltage.

The accuracy of the clamps depends upon the load. For loads greater than 1 kΩ, the accuracy depends on the tolerance of the resistors and the power supplies. The clamps provide a minimal overshoot and preshoot of 0%, with rise and

TRIPLE 8-BIT DACs REPLACE TRIMPOTS—ONLY 65¢/DAC†

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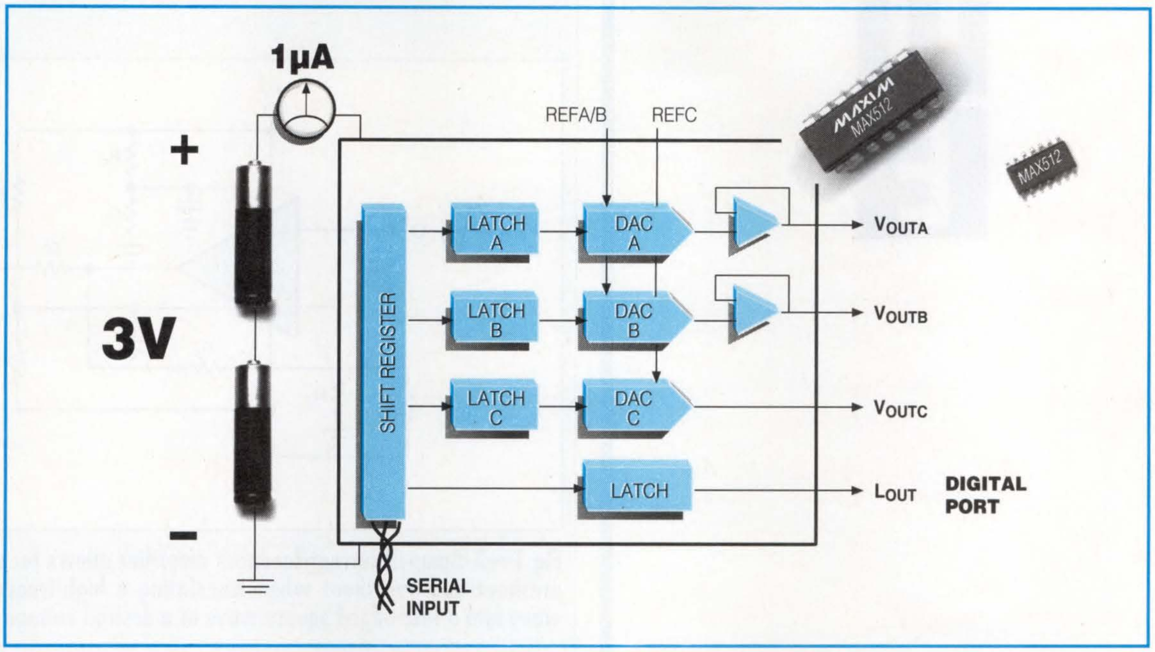

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†MAX512 10,000 pc. price is $1.95, FOB USA

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CIRCLE NO. 86

fall times of less than 4.7 nsec. The recovery time varies sightly, depending upon how far the input drives IC_1 into saturation. For capacitive loads, you can adjust R_5 to improve the output square wave.

R_G selects the circuit's gain, and R_F is the recommended feedback resistor. A resistor, R_X, tied to the appropriate supply, forces any desired initial condition at the output V_O. (DI #1450)

To Vote For This Design, Circle No. 456

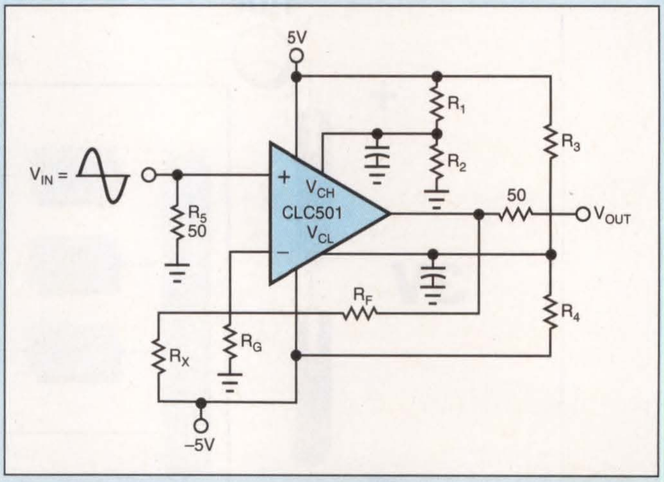

Fig 1—A clamped current-feedback amplifier allows for controlled preshoot and overshoot when translating a high-frequency sine wave into a fast-edged square wave at a desired voltage level.

SOFTWARE SHORTS

Noise-voltage generator runs under Windows version of Spice

Klaus Kühnel
Bäch/SZ, Switzerland

Based on an earlier DOS program by prolific Design Ideas contributor Steve Hageman of Calex, the noise-source generator written in Visual Basic for Windows in **EDN BBS /DI_SIG #1434** takes advantage of the Windows user interface to allow you to set up customized noise sources for MicroSim's Windows version of pSpice.

To Vote For This Design, Circle No. 457

Shell converts ADC data

Paul Kemp, NASA Johnson Space Center
Houston, TX

The generic shell attached to **EDN BBS /DI_SIG #1435** is a bit-manipulation program for Motorola's 68HC11 that converts binary data from A/D converters into ASCII data ported out through the µP's asynchronous serial port.

To Vote For This Design, Circle No. 458

SOFTWARE SHORTS

C function converts hex to binary

John Santic, consultant
Frederick, MD

The C *listing* in the text file attached to **EDN BBS /DI_SIG #1436** is a simple function that converts an ASCII hexadecimal string to binary. The function (*htoi*) works very much like the standard *atoi* library function.

To Vote For This Design, Circle No. 459

Chaotic amplifier generates Spice noise

José M Miguel-Lopez, Telecommunication School
Barcelona, Spain

The Spice subcircuit for an ingenious chaotic oscillator in **EDN BBS /DI_SIG #1437** generates a random voltage that varies between 0 and 1V. The noise generator's output has a flat spectrum ("white noise") from 0 Hz to a maximum frequency you select.

To Vote For This Design, Circle No. 460

Technique tricks Spice into displaying real-world data

Patrick Goss, ARS Microsystems
Basingstoke, Hants, UK

The Spice technique described in the ZIPfile attached to **EDN BBS /DI_SIG #1438** allows you to trick Spice into simultaneously displaying the output of a simulated circuit and real-world data taken from a prototype of the circuit.

To Vote For This Design, Circle No. 461

These Software Shorts listings are too long to reproduce here. You can obtain the listings from the Design Idea Special Interest Group on *EDN*'s bulletin-board system: (617) 558-4241, 300/1200/2400 8, N,1. From Main Menu, enter ss/DI_SIG, then rknnnn, where nnnn is the file referenced above.

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ANALOG DEVICES

CONVERTERS

NOBODY DOES CONVERTERS LIKE ANALOG DEVICES

LOW POWER 3V/5V SIGNAL CONDITIONING 24-BIT ADC FOR LESS THAN $3.00 PER CHANNEL

Signal Conditioning Applications? The AD7714 has everything you need: high resolution, low power, low component count and incredible versatility — all at an astonishingly low price!

The AD7714 is a complete analog front-end for low-frequency measurement applications. It includes a 5-channel programmable-gain front-end, 24-bit "no missing codes" charge-balancing ADC, low-pass filter and a 3-wire serial interface. It is completely under software control — gain settings, signal polarity, filter cut-off, calibration and channel selection can be configured using the input serial port.

Not convinced yet? The device operates from either 3V or 5V supply, and draws just 750µW (at 3V) and 50µW in sleep mode. RMS noise is typically 1.2µV and 300nV with gains of 1 and 128, respectively.

The AD7714 is available in a 24-pin DIP and SOIC, and is specified over the -40°C to +85°C temperature range.

1 AD7714 $11.00 in 1000s

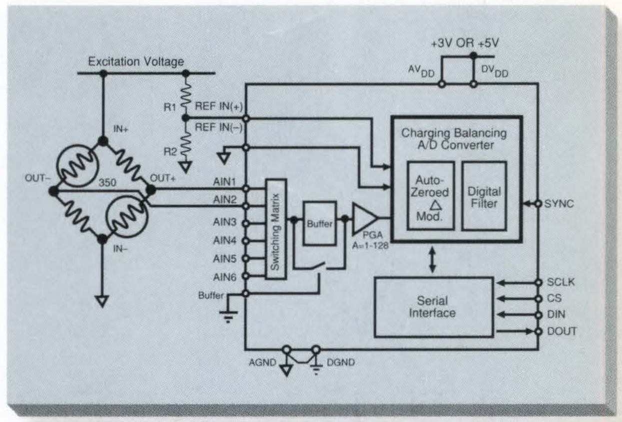
CONVERTERS

This guide describes some of the new converters from Analog Devices - the most interesting and innovative integrated circuits for digital-to-analog and analog-to-digital conversion that you can find anywhere in the world, from any manufacturer.

High resolution, low cost, multiple channels, industry standard products, ground-breaking new devices — they're all here.

The only exceptions are our range of fast converters — you'll find them, together with companion products, in our High Speed Products guide.

And if you're interested in high speed data acquisition or control, you won't want to miss that.



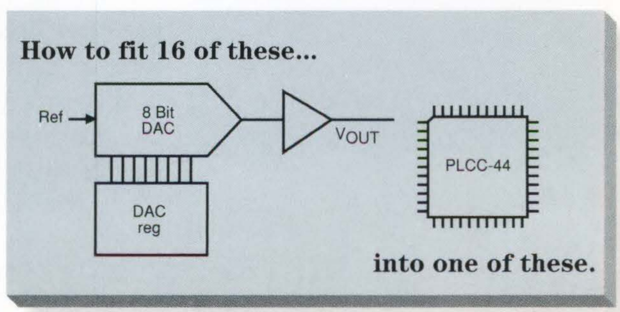
The diagram shows the AD7714 in a typical strain-gauge application, with four spare channels.

COMPACT 16-CHANNEL, 8-BIT MULTIPLYING DAC SAVES SPACE IN ATE, SONAR, ULTRASOUND, INSTRUMENTATION...

Multi-channel applications suddenly get a lot smaller, a lot better specified and a whole lot easier to design with the introduction of the AD8600.

Shoe-horning 16 independent 8-bit multiplying DACs into a compact (PLCC-44) package is impressive enough, but doing it with the performance we're offering is little short of a miracle (admittedly, a small miracle).

The AD8600 contains 16 independent voltage-output digital-to-analog converters that share a common external reference input voltage. Each DAC has its own DAC register and input register to allow double buffering. An 8-bit parallel data input, four address pins and control logic provide the high-speed digital interface. *Continued on back*



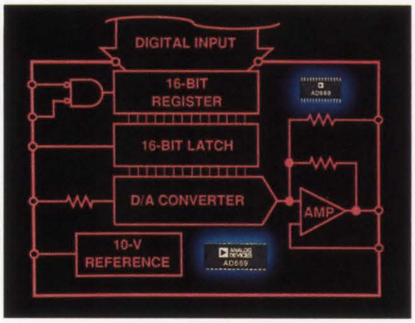
Squeeze 16 high-performance 8-bit DACs into less than 0.5 square inches (PLCC-44).

THE 16-BIT DACS YOU'VE BEEN WAITING FOR

The AD660 and AD669 are complete 16-bit, serial/byte and parallel input DACPORTs which provide leading-edge performance at down-to-earth prices. Their combination of high performance, complete functionality, flexible digital interface, small footprint and low price make them the perfect solution for 12-bit DAC users seeking to upgrade their systems without significantly increasing costs.

The AD660 and AD669 feature 15-bit monotonicity and accuracy over the entire industrial or military temperature range. They are fully AC and DC specified, and offer double-buffered latches, an on-board precision voltage reference and a pin-programmable output amplifier. Output can be either unipolar (0 to +10V) or bipolar (±10V).

These devices provide low-cost performance for a wide range of applications including industrial control, wireless communication, ATE, robotics, data acquisition and instrumentation.



2 AD660/9 $13.60 in 1000s

GROUND ZERO

Without a doubt, the single largest cause of problems in achieving the desired performance with data converters is grounding. At even low resolutions, good ground design is necessary to maintain the desired performance; for high-resolution devices it is absolutely crucial.

The best way to avoid them is to remember that "ground" isn't a magic current sink, but a connection through which currents flow to complete a circuit. Make their path smooth and your life easy!

- Have separate analog and digital grounds — and only connect them at one point.
- Check that noisy signals are kept away from sensitive ones — and that applies to return paths too.
- Where will the return currents flow?
- Are there any potential ground loops?
- Do the return paths have low enough impedance?
- Are the components well decoupled?
- Do you need a ground plane?

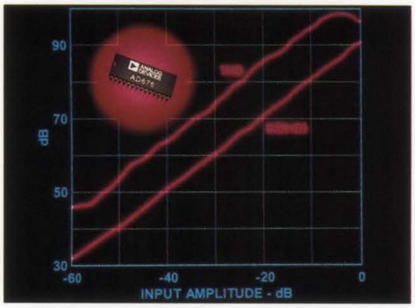
For more help call applications support: 1-800-ANALOGD.

TRUE 16-BIT ADCS AT A LOW PRICE (92dB AT 100KSPS FOR $25)

Your customers are asking you to. Your competitors are doing it. Your boss is ordering you to. Soon even your mother will be telling you to make the switch to 16-bit resolution. Thankfully, with the AD676 and AD677, you can make that move successfully and affordably. What's more, with these elegantly designed devices you get a host of other benefits too.

The AD676 and AD677 are 16-bit sampling ADCs which provide industry-leading performance, cost and space efficiencies. Their 92dB signal to noise ratio combined with ±1LSB integral non-linearity offer superior 16-bit performance at 100ksps throughput rates.

This high accuracy is a result of auto-calibration, which improves performance without the wasted board space and cost of external trims. A "ground sense" pin is included — invaluable if the signal has to be carried some distance to the A/D converter.



This combination of features makes the AD676 and AD677 the perfect solution for medical and analytic instrumentation applications as well as PC-based data acquisition and industrial applications like power supply monitoring and signal monitoring in transportation and industrial controls.

Both components are fully specified and tested for AC and DC parameters. The AD677 offers easy-to-interface three-wire serial output data. The AD676 offers full parallel output.

The AD676 is available in a 28-pin, ceramic, side-brazed package as well as a 28-pin plastic DIP. The AD677 is offered in a 16-bit skinny ceramic package and plastic DIP and 28-pin SOIC packages.

3 AD676 $27.14 in 1000s

4 AD677 $25.08 in 1000s

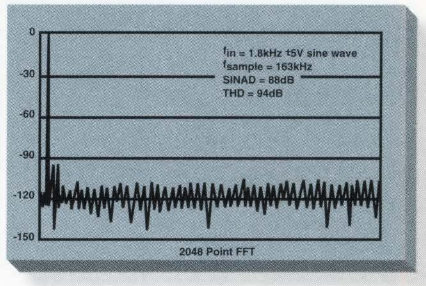
166KSPS AND 16-BIT RESOLUTION IN A LOW-POWER, LOW-NOISE ADC

The AD7884 and AD7885 are fast, monolithic 16-bit sampling ADCs. They offer true 16-bit resolution with 16-bit no missing codes, and a high throughput rate of 166ksps.

The AD7884 and AD7885 dissipate only 250mW of power. Features includes analog input ranges of ±3V and ±5V as well as parallel and byte interfacing (AD7884 and AD7885 respectively).

In medical and scientific instrumentation, noise is a critical requirement, and with their excellent noise performance (78µV rms at ±3V input range) the AD7884/5 are earning wide popularity. They also offer SNR of 86dB, while THD is -88dB.

The AD7884 is available in 40-pin cerdip and 44-pin PLCC packages. The AD7885 is available in a 28-pin DIP package while the AD7885A is available in a 44-pin PLCC package. Temperature ranges are -40°C to +85°C.



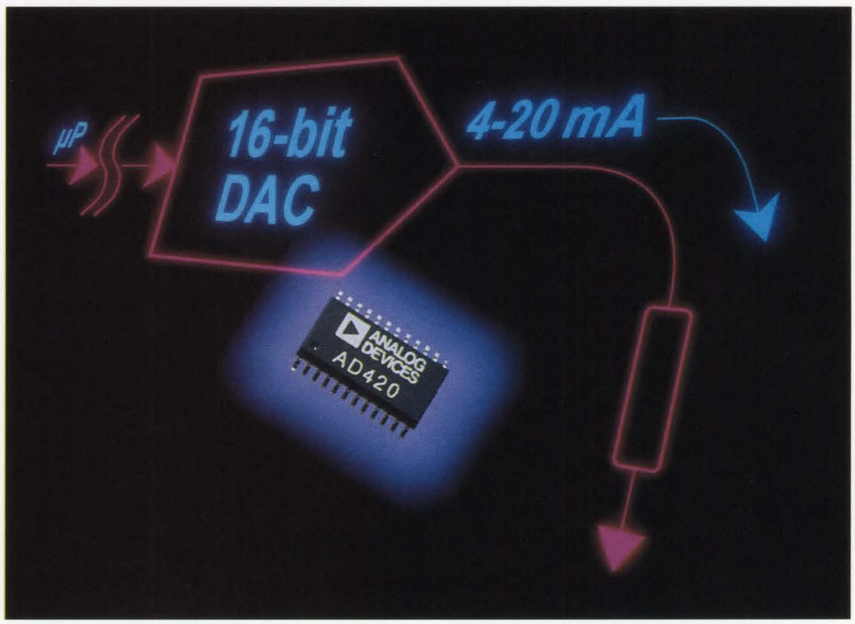
The AD7884/7885 are high performance 16-bit ADCs. Their high speed (6µs conversion time) and low noise (88dB SINAD) make them ideal for wide bandwidth signal processing applications.

5 AD7884/AD7885 $38.25 in 1000s

THE FIRST DIGITAL TO 4-20mA SYSTEM: NEW CHIP INTEGRATES DAC WITH LOOP DRIVER

16-Bit Industrial Control DAC

The AD420 is the only single-chip solution available for generating 4-20mA current loop signals from digital data. It is the first current-loop output DAC, and its high performance, low price and compact design make it perfectly suited for almost any industrial control application. It provides a single-chip solution for generating precision 4-20mA or 0-20mA signals, and runs on a single supply (up to 36V).



The AD420 has been designed to make the system engineer's life easier. It includes a 16-bit sigma delta DAC, for guaranteed monotonicity and excellent linearity. The loop driver circuitry includes a loop fault detect circuit, so a warning signal can be generated if the current loop is open circuited. It has an SPI®- and MicroWire®- compatible serial interface, and can interface seamlessly with most controllers. Furthermore, it is a completely specified part — there is no need to worry about component interaction or error budgets. Finally, although the chip can drive loops directly, it is a trivial matter to use an external boost transistor to extend the temperature range or obtain lower drift performance.

Typical applications for this unique product include valve and motor control in a wide variety of industrial applications. It is ideal for use in distributed control systems (DCS), programmable logic controllers and data I/O cards and modules. Its uses range from plant or process automation to single PC-based control systems.

24 pin PDIP or SOIC, temperature range -40°C to +85°C.

6 AD420 $10 in 1000s

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FLEXIBLE, ACCURATE QUAD 12-BIT DAC — EASY TO SET OUTPUT VOLTAGE RANGE

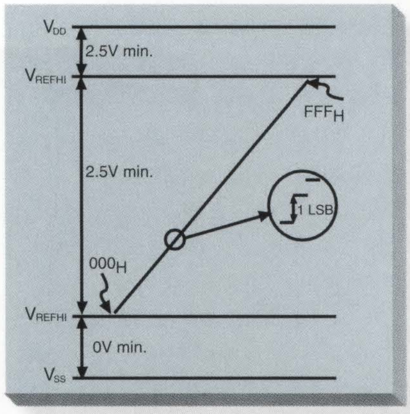
The Only DC Setpoint D/A Converters You'll Ever Need.

This family of quad 12-bit voltage-out D/A converters provides all the features most designs will ever need, plus the low cost every design requires — all in a small footprint package.

Because you may want unipolar, bipolar or asymmetric outputs, they provide separate VREF high and VREF low inputs and a single-supply output op amp — so it is trivial to set exactly the output range you need. And unlike some parts, that means both positive and negative outputs are available.

The voltage-switched DAC architecture offers the best overall accuracy available from a quad 12-bit converter (including offset and temperature accuracy).

These DACs all operate from a wide range of supply voltages (+5V to ±15V). Their high speed (80ns data load timing for DAC8412/13, or 12MHz clock for DAC8420) combines with low power dissipation to meet performance requirements while reducing power supply and cooling demands.



	Interface:	State at Reset (RST strobe):	Price:
7 DAC8420	Serial	Programmable (mode pin)	$25.16 in 1000s
8 DAC8412	Parallel	Reset to zero	$24.26 in 1000s
9 DAC8413	Parallel	Reset to midscale	$24.26 in 1000s

MAKE IT EASY

Life is hard enough already — but when it comes to helping you get converter circuits to work, Analog Devices' applications engineers have more experience than anyone else in the world — just give them a call.

Some of this experience is available in ready made forms; evaluation boards allow you to easily appraise a component, but also offer a well-designed and fully tested circuit that can be used as a reference design. And data sheets give circuit designs and pcb layouts.

There are a number of application notes that offer ideas or advice. Some of the more popular include:

- Getting the most from high resolution digital-to-analog converters **A**
- Analog signal handling for high speed and accuracy **B**
- Differential and multiplying D/A applications **C**
- DAC ICs: How many bits is enough? **D**
- An IC amplifiers guide to decoupling, grounding and making things go right for a change **E**

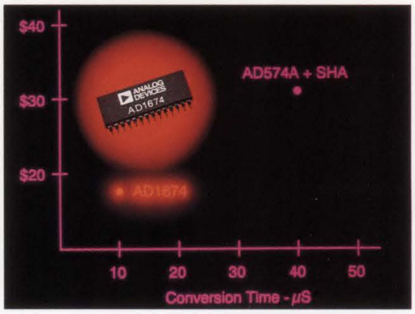
USING THE INDUSTRY STANDARD AD574? THEN MOVE UP TO THE AD1674

When Analog Devices introduced the AD574, it quickly became the industry standard. Now, the AD1674 takes that standard to yet another level.

The AD1674 is a high-performance sampling 12-bit A/D which offers users of the AD574 family (AD574, AD674, AD774) an instant upgrade with up to three times the speed, along with lower power and greater accuracy. It utilizes the AD574 pinout for easy replacement in existing designs, providing increased capabilities while reducing costs through the elimination of external SHA and support circuitry.

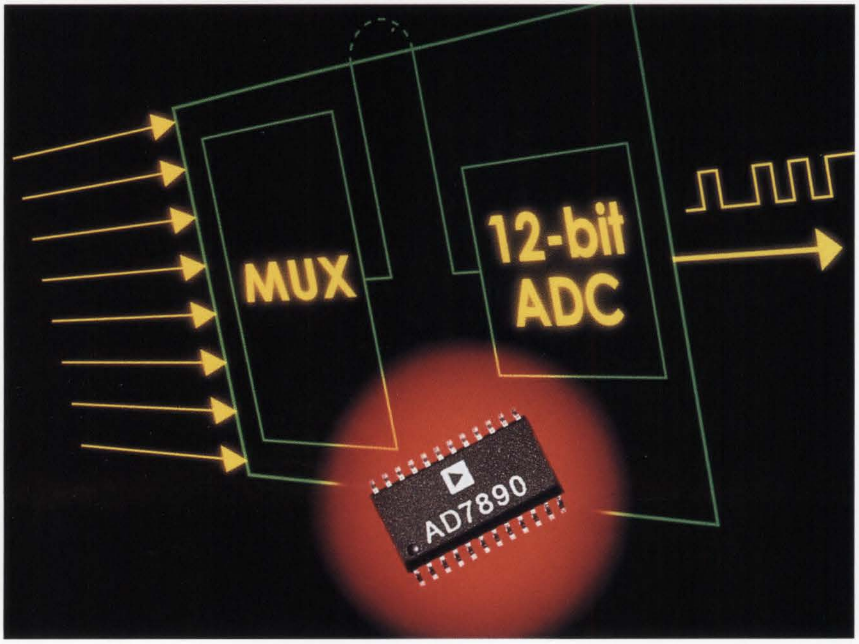
The power and versatility of the AD1674 make it an ideal general-purpose converter for a wide variety of applications ranging from industrial control to data acquisition and instrumentation. Additional features include ±5V, ±10V, 0–10V and 0–20V input ranges, internal reference, 8- and 16-bit microprocessor interfaces and a wide selection of package styles.

The AD1674 is available in 28-pin PDIP and 28-pin SOIC packages in commercial and industrial temperature ranges as well as in a 28-pin side-brazed ceramic package for industrial and military ranges. All specifications are both AC and DC guaranteed. Full MIL-883B and SMD devices are also available.



10 AD1674 $11.60 in 1000s

A NEW GENERATION OF 12-BIT ADCS, WITH UNMATCHED PERFORMANCE, SINGLE 5V POWER SUPPLY OPERATION, ROBUST INPUT CIRCUITRY AND EASE OF USE IN A COMPACT DESIGN.



THE SMALLEST 12-BIT ADC

A single-channel ADC in a tiny 0.15" wide 8-pin SOIC package.

The AD7893 provides a throughput rate of 117ksps, with a power dissipation of less than 50mW. It handles data transfer via a two-wire serial interface.

OCTAL ADC–7X SAVINGS IN SIGNAL CONDITIONING

The AD7890 is an eight-channel version which offers a seven-fold savings in channel support circuitry over other integrated solutions. This economy is possible because access to MUXOUT means that the same signal-conditioning circuitry can be used for all eight channels. The AD7890 has a throughput rate of 100ksps. It also features a power dissipation of less than 50mW, and on-chip reference.

Robust Inputs

Both parts are available with three distinct input range options. Like the AD7892, they operate from a single 5V power supply, and their analog inputs are tolerant to voltages which extend well outside of the supplies, protecting them from overvoltage fault conditions (up to 17V outside for the -10 version).

11 AD7890 $10.20 in 1000s
12 AD7893 $8.00 in 1000s

AD7890-2	0–2.5 V
AD7890-4	0–4 V
AD7890-10	+/- 10 V
AD7893-2	0–2.5 V
AD7893-5	0–5 V
AD7893-10	+/- 10 V

FASTER SIGNALS AND CLEARER RESULTS — THE HIGHEST SINAD SPECS FROM A COMPLETE 12-BIT 1.25MSPS ADC

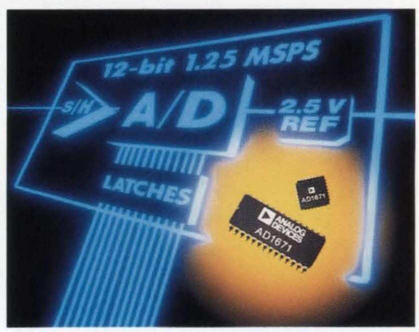
The AD1671 delivers leading-edge performance from a complete converter — with on-chip reference and wide bandwidth, high impedance sample-and-hold amplifier.

The AD1671's exceptional dynamic performance includes 69dB SINAD, a full power bandwidth of 2MHz and a small signal bandwidth of 12MHz. This allows better, faster data acquisition — delivering sharper images from scanners or clearer signals from communication links.

The AD1671 performance and price breakthrough are enabling markets that were previously prohibited by cost, power or price constraints. They include communications systems (high speed modems, base stations, HDSL), imaging (color scanners, medical imaging, IR) and high-speed data acquisition.

The AD1671 is available in both a 28-pin cerdip and 28-pin PLCC package, in commercial, industrial and DESC versions.

13 AD1671 Less than $40 in volume.



TINY, COMPLETE SINGLE SUPPLY DACS — SMALLEST PACKAGES, EASIEST TO USE

Total DAC System — In the Industry's Smallest Packages

The DAC8512, DAC8562, AD8522 and AD8582 are a set of single-supply 12-bit DACs, offering a complete "plug and play" output system. Everything there, everything included, everything tested and specified. And everything squeezed into a tiny SO-8 package (DAC8512).

Each part includes all the related circuits — bandgap reference, voltage-switched R-2R ladder DAC, and an output rail-to-rail op amp. Full-scale voltage of 4.095V with 1mV/bit output coding creates a programming-friendly environment while maximizing the analog output swing for all loads.

These parts also feature low power dissipation of 3mW/DAC and compact designs which make them ideal for portable or battery-operated equipment.

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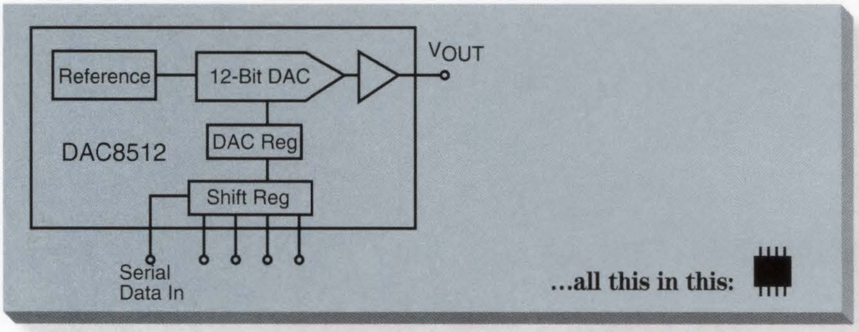
17 AD8582	Dual	Parallel	SOL-24 / DIP-24	$9.44 in 1000s



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18 REF195 $1.94 in 1000s

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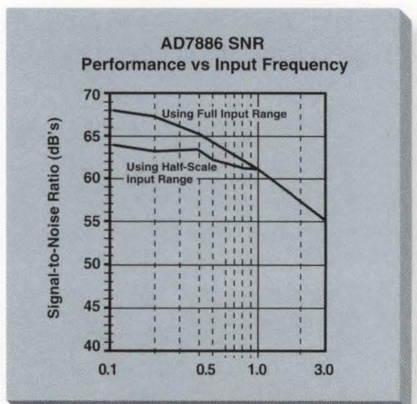
The AD7886 is a high-speed, power-efficient 12-bit ADC with a throughput rate of 1Msps. Its high performance makes it ideal for sampling applications requiring a broad dynamic range over a large bandwidth, as well as high-speed and multiplexed data acquisition systems. The full-power bandwidth of the on-chip sample-and-hold extends well above the 500kHz Nyquist limit, allowing the AD7886 to be used in undersampling systems in addition to the standard signal-processing applications.

The AD7886 has a low power dissipation of 250mW, and is comprehensively specified for AC and DC parameters. It features a high speed interface with 57ns bus access times, making it directly compatible with DSPs and microcontrollers.

It is available in 28-pin DIP and 28-pin surface mount packages. Temperature ranges are -40°C to +85°C for the industrial grades and -55°C to +125°C for the extended range.

19 AD7886 under $40 in 1000s



The full power bandwidth of the SHA allows the AD7886 to sample up to 1MHz bandwidth — ideal for under-sampling applications.

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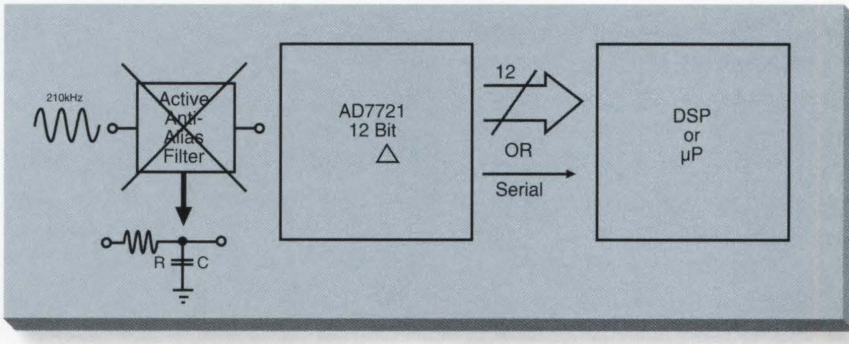

The AD7721 is a 12-bit sigma-delta ADC with a 200kHz bandwidth and an output word rate of 470ksps.

It offers all the advantages of digital filter design, including freedom from the component matching or drift issues commonly associated with analog filters. It also drastically simplifies the design of the input anti-aliasing filter — in many cases no filter other than a simple RC roll-off is required. Other advantages include device-device repeatability, linear phase characteristics and dramatic improvement in SNR.

Operating from a single 5V supply, the AD7721 dissipates only 175mW of power while supporting a full-power signal bandwidth of 200kHz. Other features include an on-chip reference and a choice of either parallel or serial interfacing, a power-down mode and pseudo-differential inputs. It also offers a calibration mode to minimize offset and gain errors.

The AD7721 is available in 28-pin plastic DIP, SOIC and cerdip packages. Temperature ranges are -40°C to +85°C or -55°C to +125°C for the extended grade.

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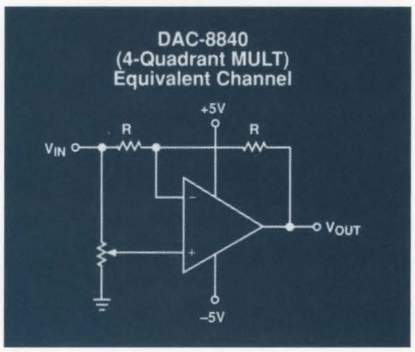

service or remote adjustment.

For DC adjustment, the DAC8800 provides high and low reference inputs to establish the output swing. For AC signals, the DAC8840 features 4-quadrant multiplying adjustment for inputs up to 1MHz, while the AD8842 is suited for lower bandwidths (50kHz) at a lower price and half the power requirement.

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22 DAC8840 $8.36 in 1000s
23 DAC8841 $8.36 in 1000s
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The AD7943, AD7945 and AD7948 provide serial, parallel and byte digital interface, respectively. In addition to the SSOP, industry standard packages are available. These devices are specified over the -40°C to +85 °C temperature range.

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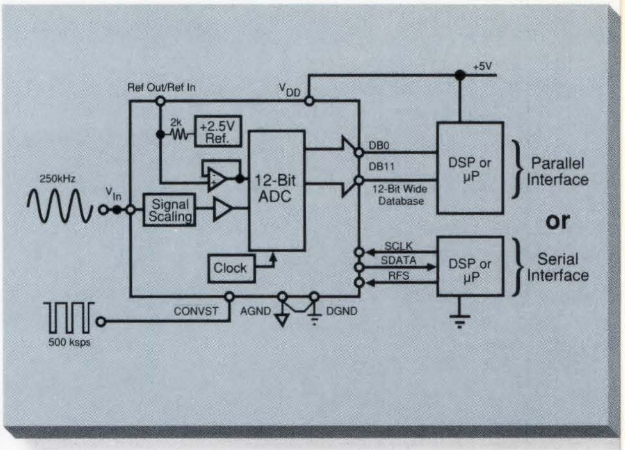
The ADC7892 is a versatile, high-speed ADC expressly designed to cope with these circumstances. It is a 12-bit sampling A/D converter with a throughput rate of 500ksps, low power dissipation of only 60mW and the flexibility of both serial and parallel interface capability. Crucially its analog inputs are tolerant to voltages which extend well outside of the supplies; this resilience protects them from overvoltage fault conditions (up to ±17V outside supply range for the ±10V input version). It also features an on-chip reference, as well as a power down mode.



The AD7892 is available in two versions. The AD7892-2 has an analog input range version of 0 to 2.5V for complete 5V single-supply systems. The AD7892-1 has input ranges of ±5V and ±10V for industrial-type systems where the larger LSB sizes are important.

Both versions are available in 24-pin plastic DIP, SOIC and cerdip packages. Temperature ranges are -40°C to +85°C for the industrial grades and -55°C to +125°C for the extended range.

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The AD654 provides designers with a converter that can be applied to solve a wide range of design problems at much lower cost than ever before possible.

It is a monolithic V/F converter which reduces space requirements by integrating an input amplifier, precision oscillator system and a high-current output stage. Its high performance, low cost, low power consumption and small size make it the perfect choice for an unlimited variety of applications.

The AD654 provides a square wave output and can drive up to 12 TTL loads, opto-couplers, long cables or similar loads. The input amplifier provides low drift, permitting operation directly from low level transducers like thermocouples, strain gauges and current shunts. It also offers a high (250MΩ) input resistance to positive voltage signals. Only 2.0mA of quiescent current is required using the single positive supply from 4.5V to 26V, and the output stage can sink up to 10mA with saturation voltage less than 0.4V.

The AD654 combines low cost with very high accuracy. Linearity error is only 0.03% for a 250kHz full scale frequency, and operation is guaranteed over an 80dB dynamic range. A single RC network is all that's needed to set up any full scale frequency up to 500kHz.

Applications for this product range from high-resolution A/D converters, process control systems, and isolation to energy management, motor speed controls and power monitoring.

The AD654 is available in 8-pin PDIP and 8-pin SOIC packages in commercial temperature ranges.

26 AD654 $2.95 in 1000s

Continued from front

Finally, the AD8600 features a new DAC design (patent-pending) which reduces reference glitch during reprogramming.

Space savings is a major benefit of this part, since it provides all these capabilities in a PLCC-44 package. But other features include: simplified full-scale setting; fast 2µs settling time for fast updates for analog instrument systems; minimal (2mV) zero level system errors; and fast (30ns) data loading write times. A data readback feature allows system self-check at power-on.

The AD8600 operates from dual ±5V or single +5V supplies, in extended temperature range —(-40°C to +85°C).

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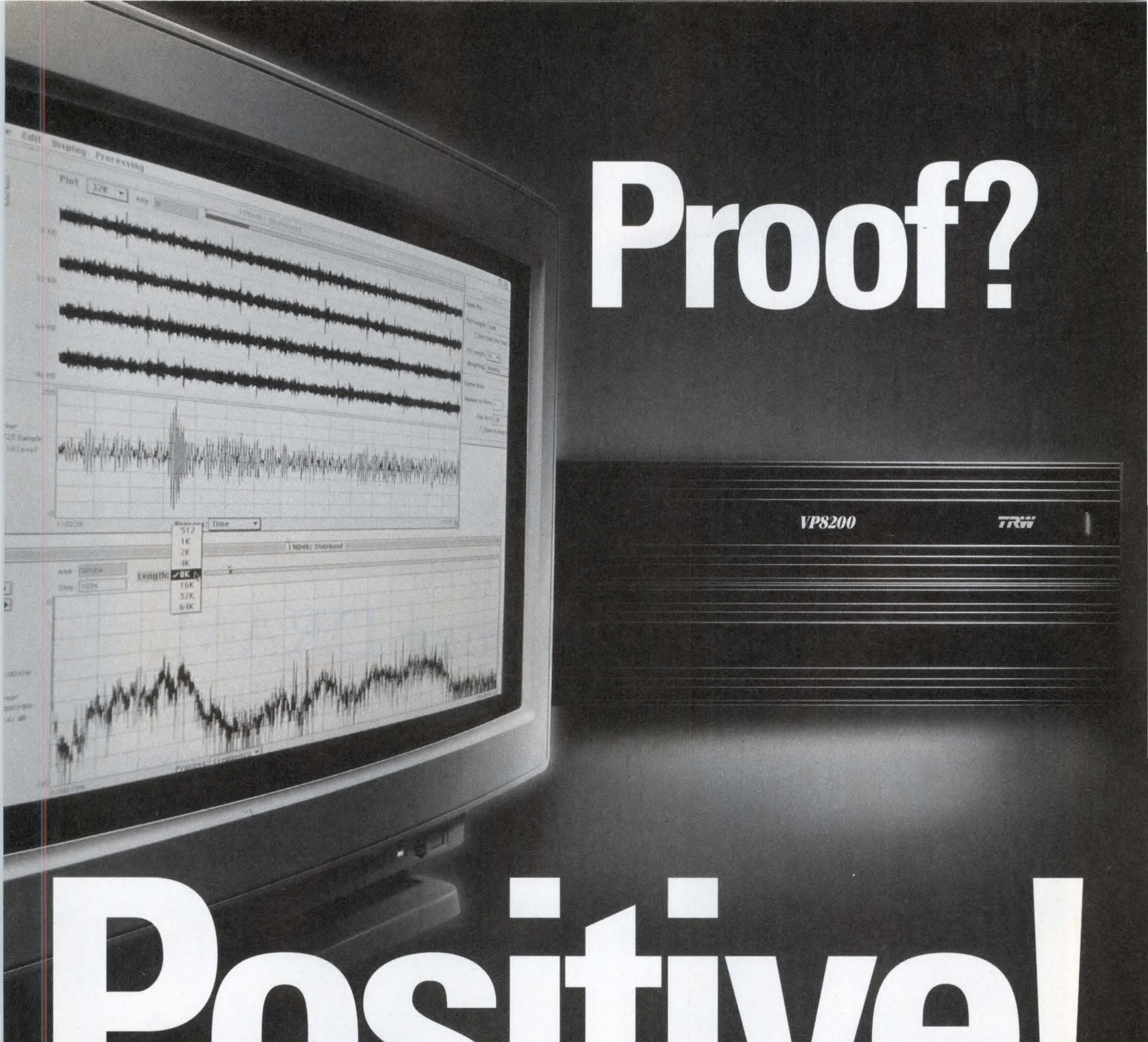

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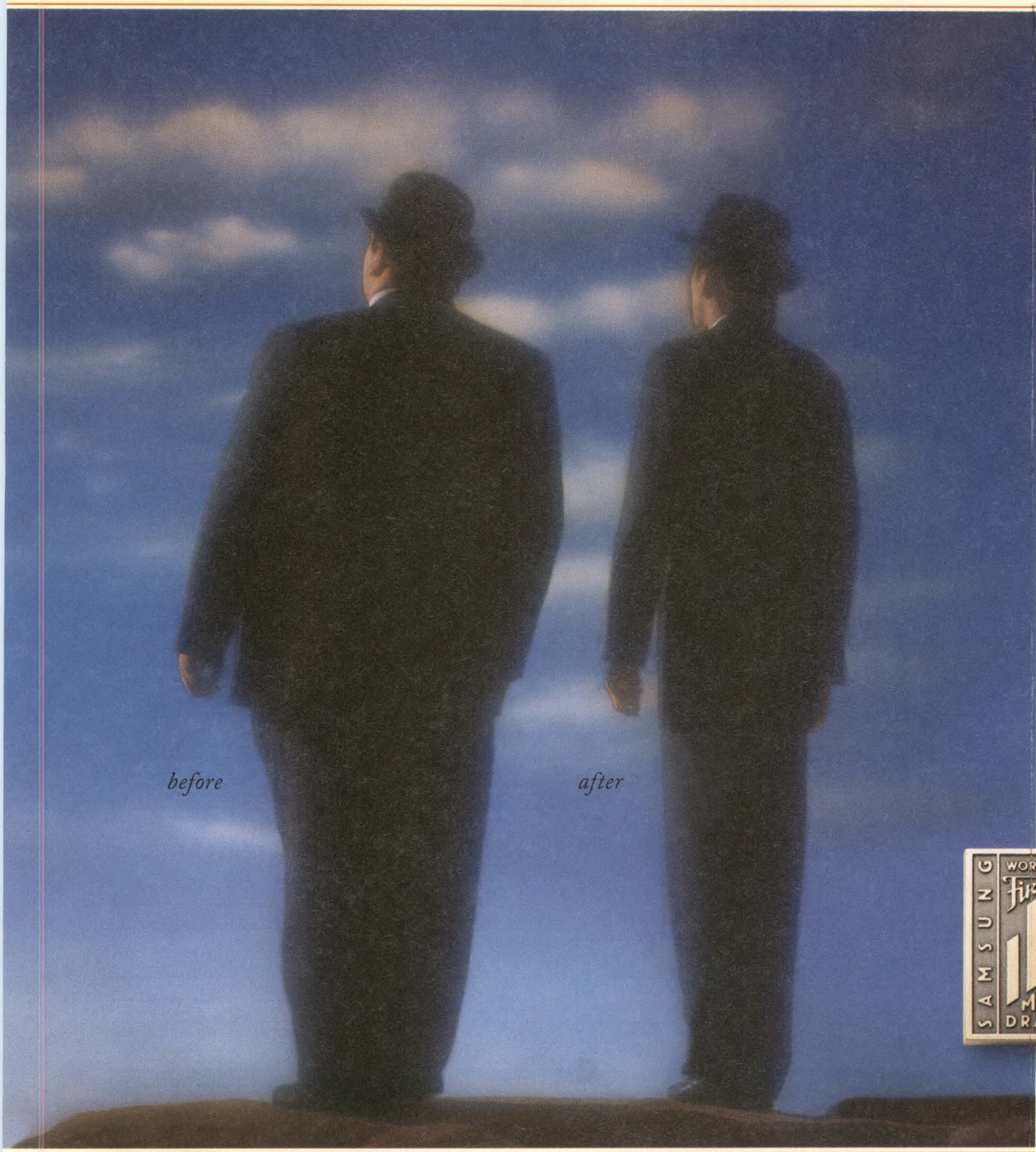

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Layout techniques boost dynamic range for high-speed ICs

Rosie Loaiza-Montiel, Burr-Brown Corp

A systematic approach to good grounding and bypassing practices allows high-speed analog circuits to deliver dynamic range equivalent to Spice predictions.

Circuits with dynamic range exceeding 90 dB are always challenging; when combined with hundreds of megahertz of bandwidth, they become especially challenging. Manufacturers of such high-speed, wide-dynamic-range circuits always recommend using plenty of ground plane, short leads on components, and "good board-layout techniques." However, even the best efforts at interpreting these instructions can lead to frustration. Going step-by-step through the optimization of an evaluation board for Burr-Brown's OPA642 analog circuit (500-MHz bandwidth, 2V p-p output, –90-dBc distortion in a 50Ω load at 5 MHz) allows you to address such considerations as:

- Where to put the bypass capacitors
- How big the capacitors should be
- Whether ground planes are needed on both sides of the board.

You can use a router to fabricate the evaluation boards. The router mills grooves in copper on a blank board, using a layout from a CAD program for control. The resulting board functions very much like a conventional pc board. Thus, you optimize performance before tooling the production board, thereby saving time and money.

Start with some assumptions about good board-layout techniques. These include putting ground planes on both sides of the board, which yields controlled impedance for the signal lines. Also, ground fill around the power lines reduces electromagnetic-field coupling. In this kind of high-frequency application, surface-mount components are particularly appropriate. Surface-mount resistors on the bottom of the board, for example, allow the feedback path to run beneath the amplifier. Chip capacitors on the top (amplifier) side permit the closest possible connections to the package pins.

It's important to connect the bypass capacitors directly at the package pins to ensure a low-impedance power supply at high frequencies. They reduce the area of the loop through which the ac power-supply currents flow because they allow the high-frequency components of the power-supply current to bypass the power-supply inductance. The rule of thumb is smaller loop=lower inductance=lower impedance=better performance.

It's easy and common to overlook this small bit of advice about bypassing. For example, when the board detailed in this article was tooled for mass production, the board designer moved the bypass capacitors to the bottom of the board. This seemingly minor change caused distortion problems at high gains and necessitated board retooling.

Fig 1 shows the initial board layout; **Fig 2**, the schematic diagram; and **Fig 3**, the measured performance. The schematic for the board is that of a simple voltage follower

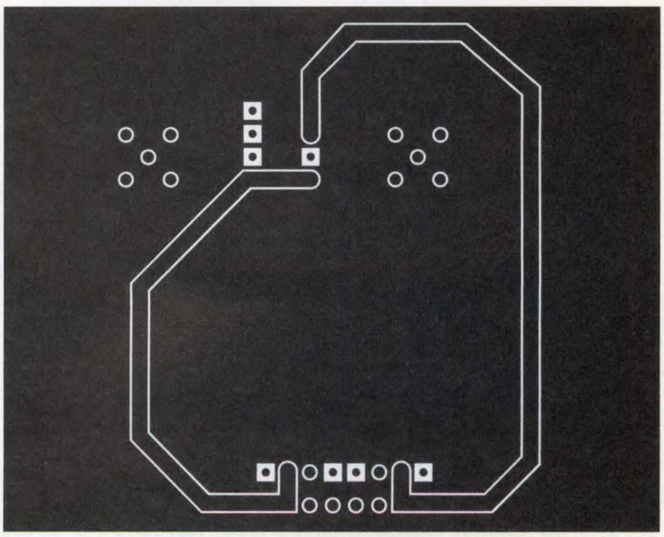

Fig 1—The first cut at the layout connects positive and negative supplies and uses a single bypass capacitor for each.

(buffer). This configuration presents a rigorous challenge for a high-speed amplifier, as it demands unity-gain stability and it exercises the full input common-mode range at the signal frequency. The 50Ω resistor in series with the output allows the amplifier to drive the 50Ω input of the spectrum analyzer with no reflection problems. To ensure a clean input signal, a 5-MHz bandpass filter (not shown) conditions the input sine wave. This conditioning eliminates the analog equivalent of garbage in, garbage out.

The OPA642 has separate pins for the output-stage power supply. Early on in the design stage, the IC designer realized the importance of a low-impedance power supply. The separate pins for the output-stage supply prevent the high-frequency, high-amplitude output currents flowing in the package-pin inductance from modulating the power-supply voltage of the remainder of this high-dynamic-range amplifier. The designer also added on-chip bypass capacitors along with low-value resistors (**Fig 4**) to filter the supply voltage for the most sensitive part of the amplifier, and thus reduce the effects of supply noise.

For the initial layout, designers connect the low- and high-level power supplies to allow using a single capacitor to bypass each power supply. This configuration is the obvious first choice for area and cost considerations. The board has 2.2-μF tantalum capacitors at the power-supply connector. Because these become inductive at fairly low frequencies, the designers add 0.01-μF chip capacitors on the IC side of the board, directly at the package pins.

Fig 3a shows the measured performance. All the spectrum-analyzer plots show only the second harmonic, which is the limiting factor for dynamic range with this amplifier. If the screen showed the fundamental, the second harmonic would be lost in the noise floor because the spectrum analyzer has limited dynamic range for wideband measurements.

Performance of the initial board is fairly good, with distortion measuring –77 dB for a 2V p-p, 5-MHz sinewave into 50Ω. (The fundamental is 4V p-p into 100Ω at the output of the amplifier; thus, 2V p-p into 50Ω or 3 dBm at the analyz-

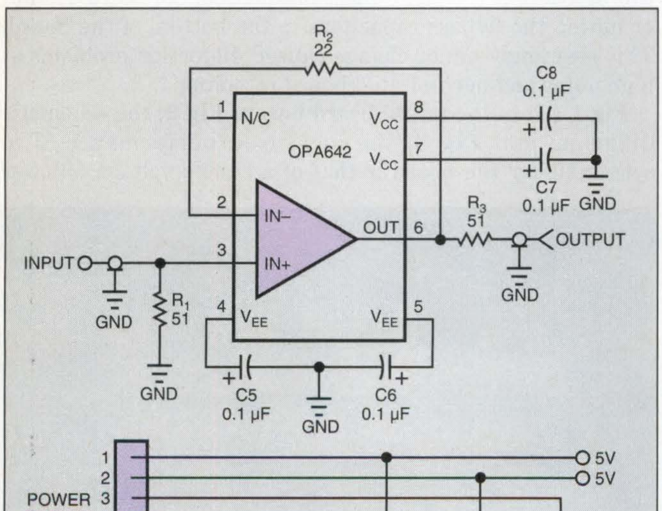

Fig 2—This follower configuration is a tough test for a high-speed amplifier because of common-mode and unity-gain-stability requirements.

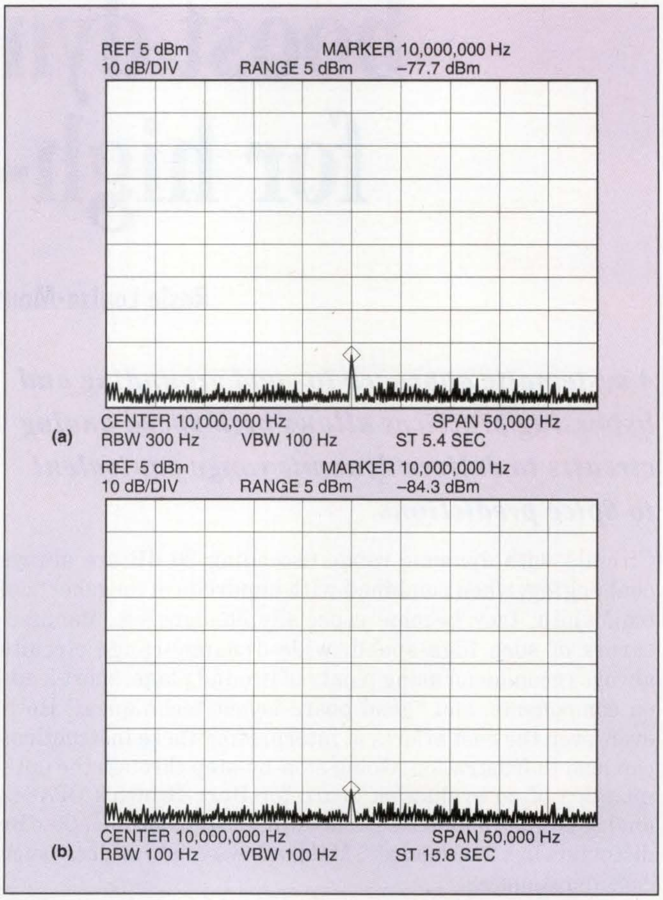

Fig 3—The layout of Fig 1 produces second-harmonic distortion of –80 dB with 0.01-μF bypasses (a) and –87 dB with 0.1-μF bypasses (b).

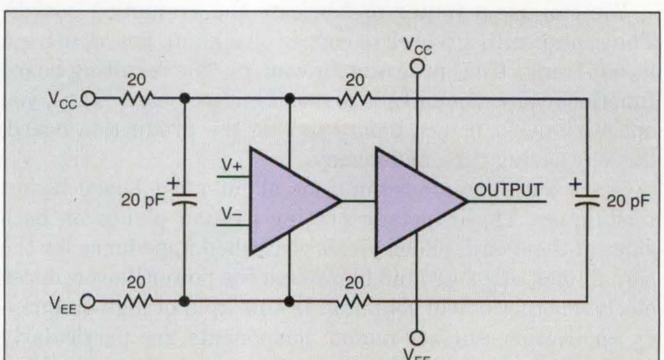

Fig 4—The OPA642 has internal power-supply filtering to reduce the effects of power-supply noise.

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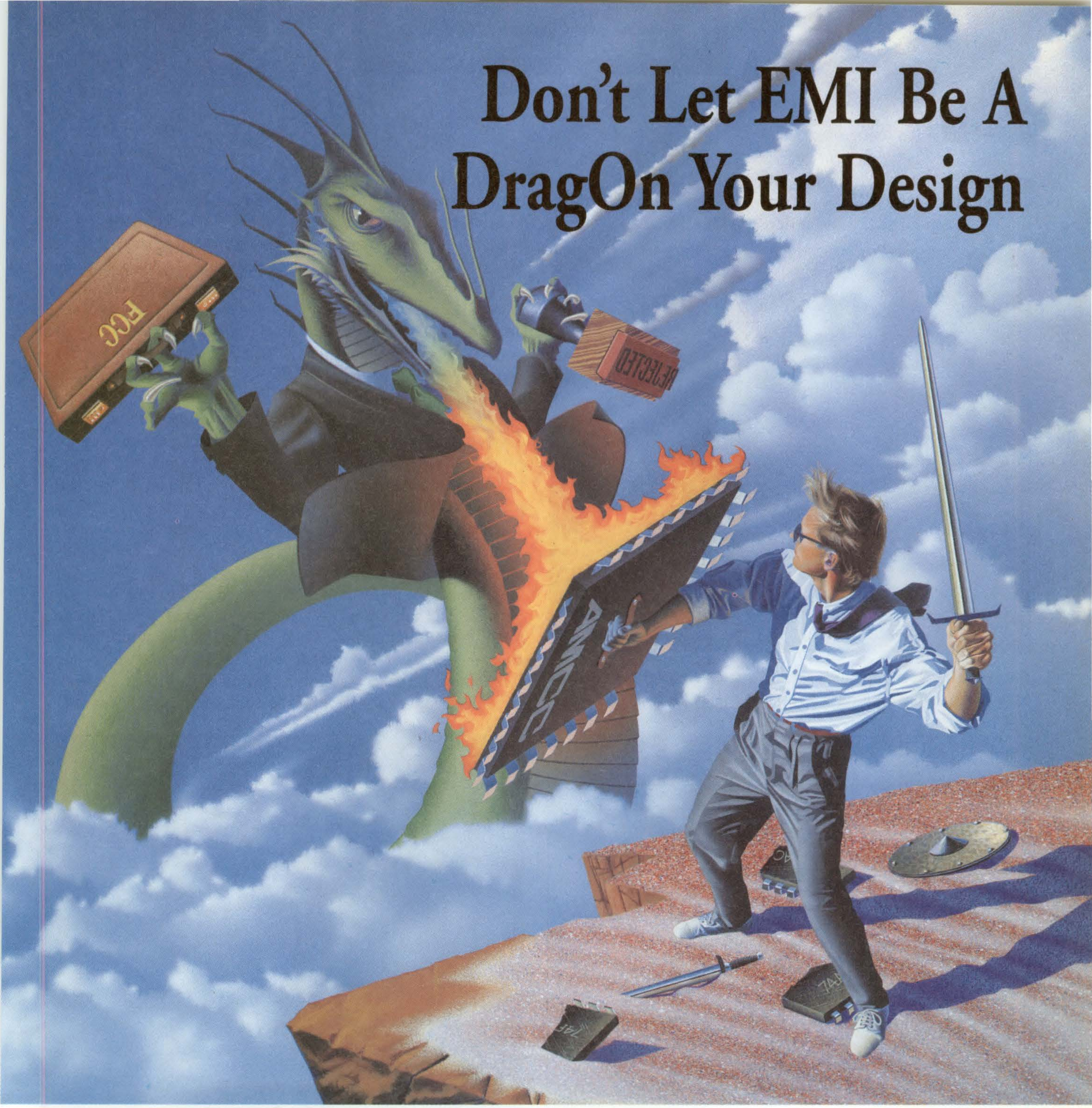

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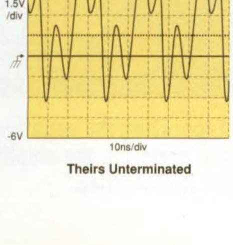

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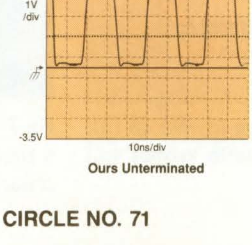

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HIGH-SPEED ICs

er input.) The spectrum looks quite clean, but Spice predicted -90 dB, vs the -77 dB obtained. Is the Spice prediction faulty, or could the layout be improved?

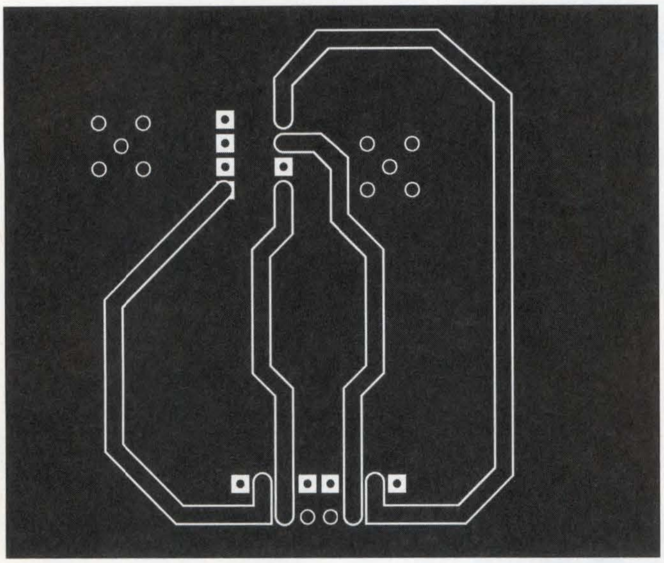


Fig 5—This layout separates the low- and high-level supplies and uses 0.01-μF chip capacitors on all four supply pins.

An old standby for improving performance is to use bigger bypass capacitors. Increasing the value from 0.01 to 0.1 μF yields the performance of **Fig 3b**, with -87-dB distortion. At 5 MHz, the impedance of the 0.1-μF capacitor is 0.3Ω vs 3Ω for the 0.01-μF bypass. Lower-impedance power supplies are critical because supply currents at the signal frequency flow through this impedance and create signals that the amplifier must reject, by the amount determined by its power-supply rejection ratio (PSRR). At dc or low frequencies, the OPA642 has a 95-dB PSRR, but, at 5 MHz, the PSRR is only about 60 dB.

The next step in the quest for improved performance is to use the extra power-supply pins to separate the output currents from the supplies of the low-level stages. **Fig 5** shows the new layout, with 0.01-μF chip capacitors on all four supply pins. (The bottom of the board is the same for all the boards.) **Fig 6a** shows the performance with this configuration. The distortion improves to -90 dB, somewhat short of expectations.

A noticeable difference in the new board of **Fig 5**, as compared with that of **Fig 1**, is that the IC is now near the edge of the board, instead of in the middle. The ground plane is, therefore, rather narrow. Could this increase the ground impedance and add distortion? A quick way to check this is to solder copper tape around the edge of the board where the

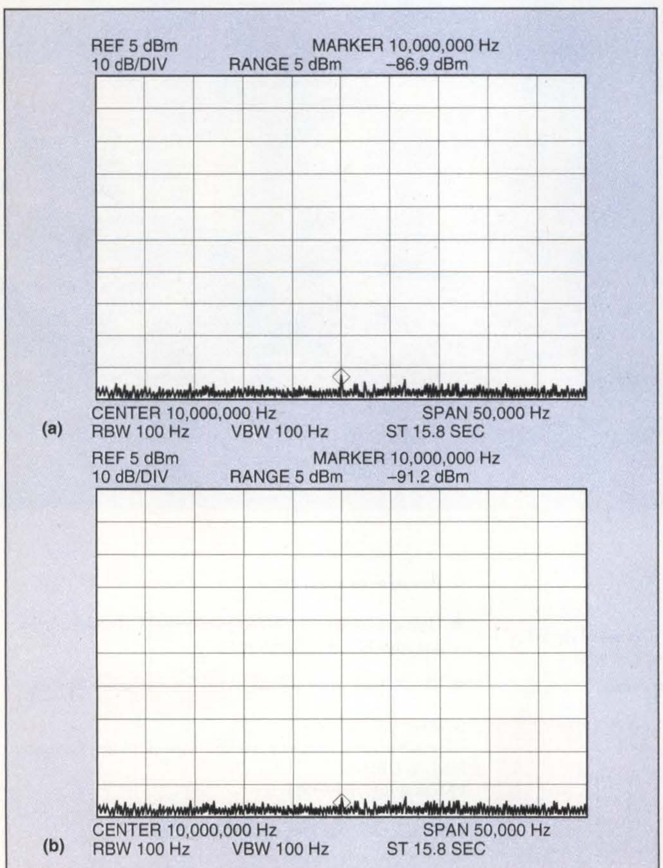


Fig 6—Separating the supplies improves distortion to –90 dB (a); connecting the top and bottom ground planes with copper foil improves it further to –94 dB (b).

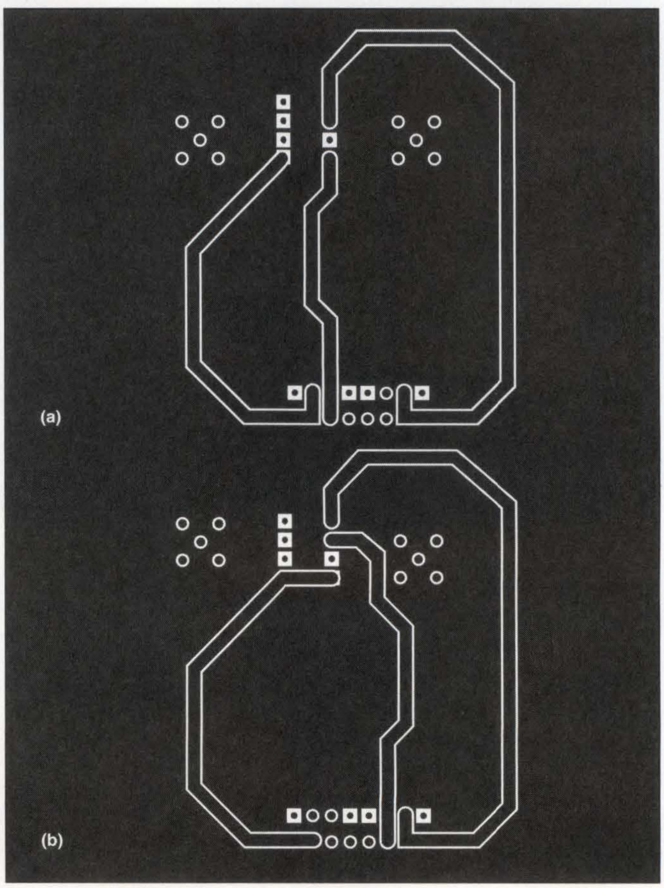
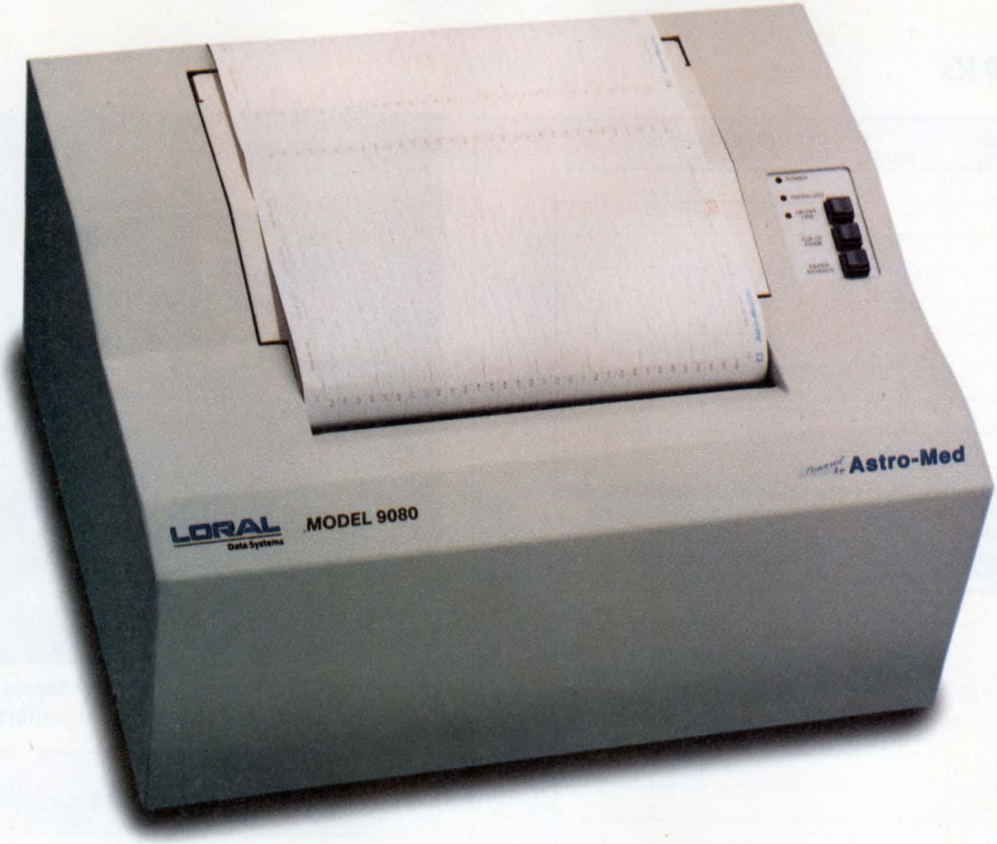


Fig 7—Separating the negative (a) and positive supplies (b) one at a time and centering the amplifier on the board produce noticeable reductions in distortion.



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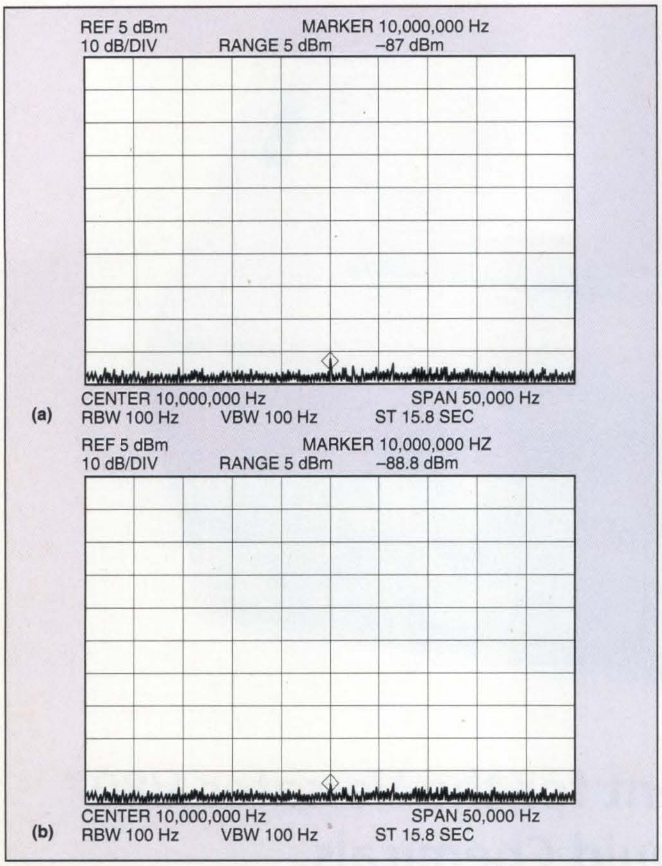


Fig 8—Separate negative (a) and positive (b) supplies yield distortion figures of –90 and –91 dB, respectively.

ground plane is narrow. This step yields a very satisfactory -94 dB (**Fig 6b**). Some questions remain: Are all four capacitors needed? Is it necessary to separate both supplies? The extra area and components add cost, but you don't want to sacrifice performance.

The next board has good connections between the top and bottom ground planes, the amplifier in the middle of the board, and both supplies separable. A knife and soldering iron allow us to examine the effects of connecting the 5 and -5V supplies. Separating the power supplies one at a time produces the layouts of **Figs 7a** (negative supplies separated) and **7b** (positive supplies separated). Improvement is noticeable in both cases, as seen in the plots for these layouts (**Figs 8a** and **8b**, respectively).

Distortion levels are now -90 and -91 dB, respectively, as compared with -87 dB with both pairs of supplies sharing a single bypass capacitor, and -94 dB with separate supplies and bypass capacitors. The final board of **Fig 9** uses this optimum configuration (separate supplies, individual bypasses), and yields -94 dB distortion (**Fig 10**), verifying that this level of performance is repeatable.

The optimization process shows that good power-supply routing and bypassing can be tricky and elusive. Chip capacitors mounted directly at the package pins can be crucial for some applications because power-supply impedance of even a few ohms at the frequency of interest can severely degrade performance. EDN

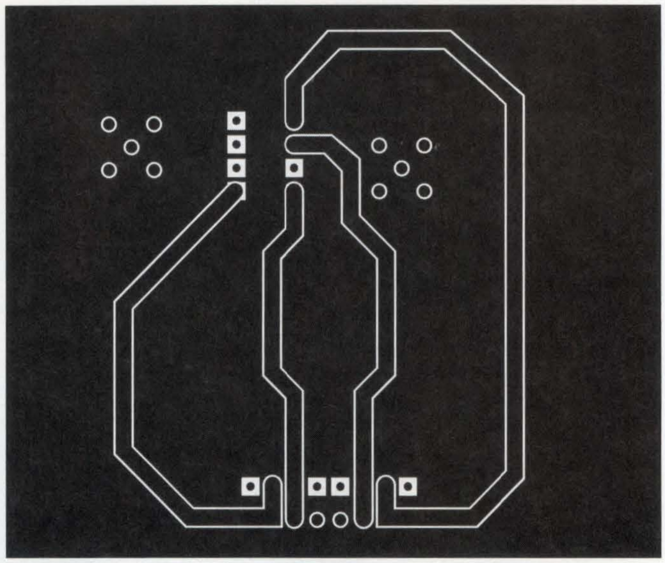


Fig 9—The optimized board uses four supply connections, an effective ground plane, and four bypass capacitors.

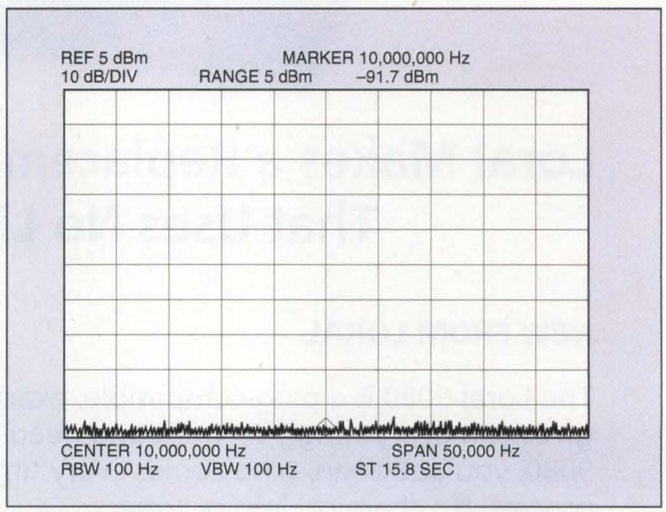
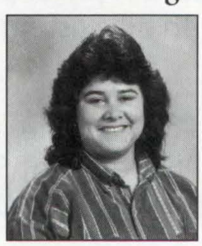


Fig 10—The optimized board of Fig 9 yields a clean spectrum, with second-harmonic distortion of –94 dB.

Author's biography



Rosie Loaiza-Montiel is an associate engineer in the High Speed Design Div of Burr-Brown Corp, Tucson, AZ, where she has worked for nine years. In her current position, she is responsible for evaluating prototypes and transferring them to production. She helped develop the OPA64X family of analog circuits. Loaiza-Montiel received an associate's degree in engineering from Pima Community College in Tucson, AZ, and is currently working toward a BSEE at the University of Arizona, Tuscson. She enjoys outdoor activities and sports, especially softball.

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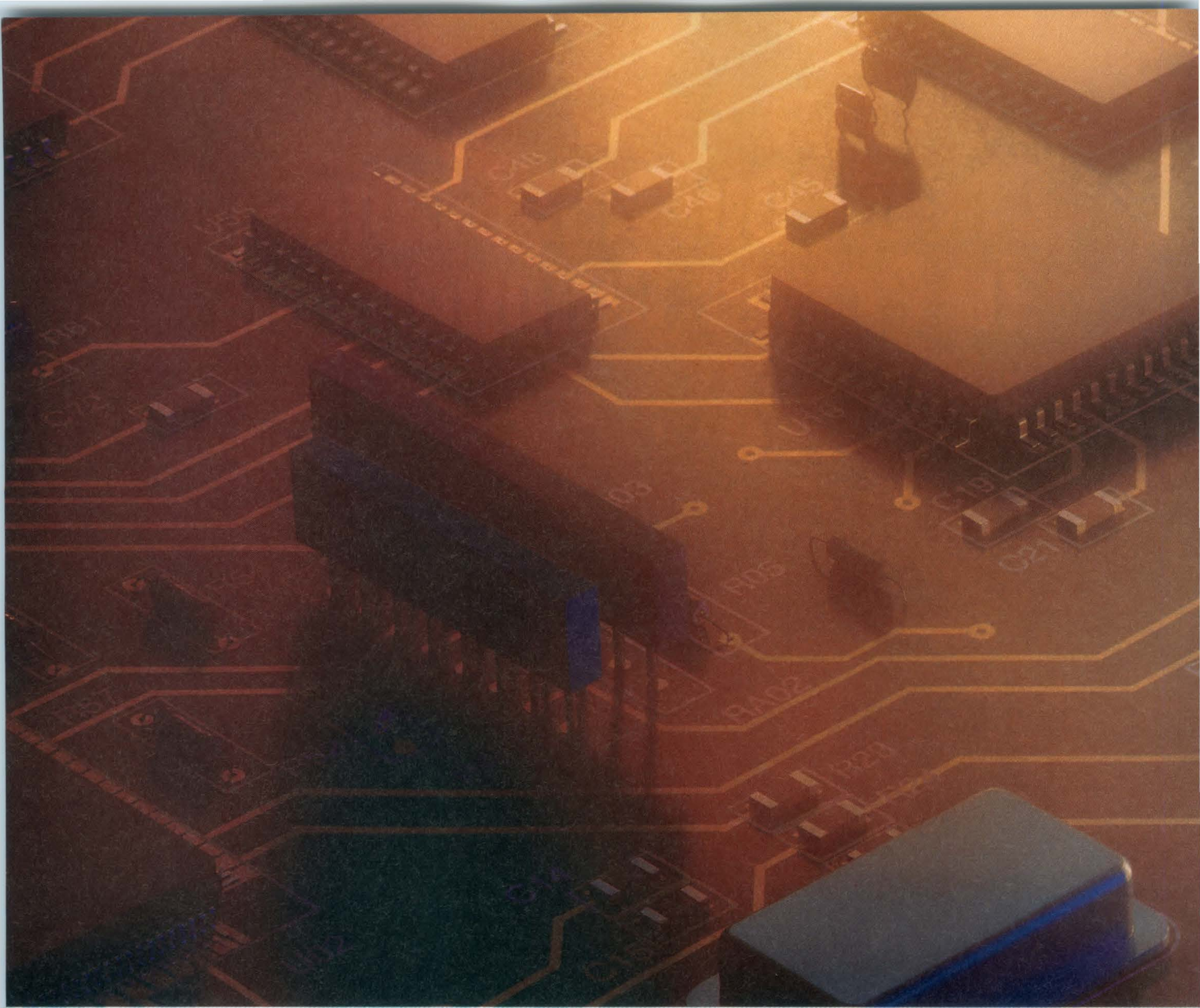

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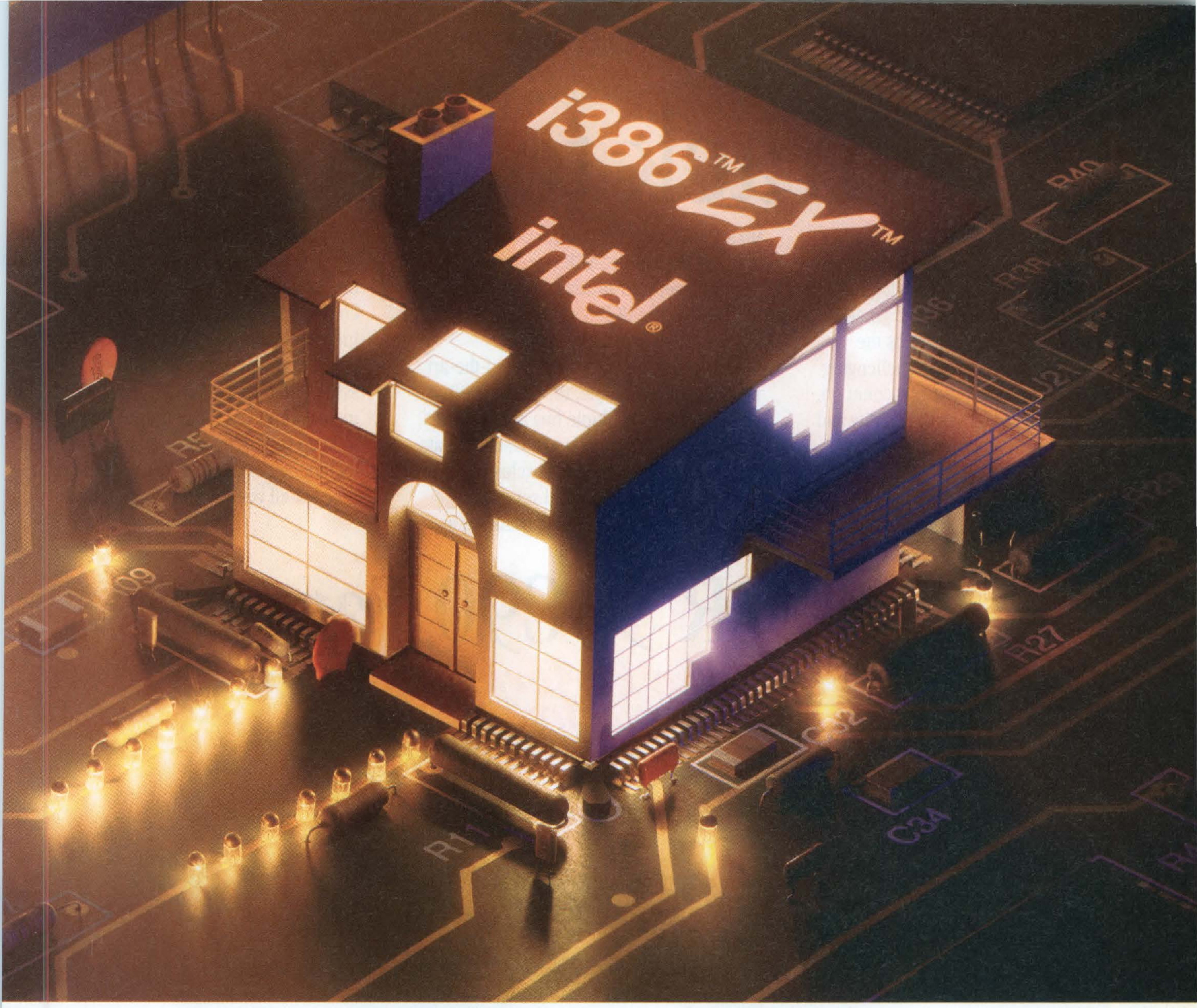

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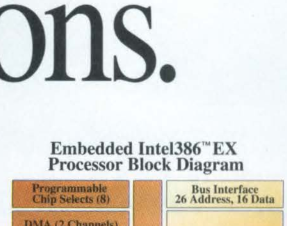

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Keep metastability from killing your digital design

Debora Grosse, Unisys

Synchronizing asynchronous signals causes metastability, which makes it difficult to iron out the bugs during system test. Paying close attention to the synchronizer and some metastability equations can help you avoid the pitfalls.

Synchronization bugs cause intermittent failures in board designs. These bugs can be frustratingly difficult to reproduce in the lab. Fortunately, careful designers can avoid this frustration by fulfilling two requirements. First, understand the principles of synchronization and metastability. Second, recognize the subtle situations in which these principles apply.

To see what can go wrong, consider the representative synchronous state machine in **Fig 1**. Because of a design bug, the state occasionally makes transitions from State 1 to State 0 instead of jumping forward to State 2. The state number is the binary value of the machine's three state flip-flops. The INIT, DATA_VALID, and COUNT_EN outputs are decoded from the state bits. The REQ signal is an asynchronous input. The design assumes that REQ holds its value for longer than the system clock period, guaranteeing that the machine sees all transitions.

The culprit causing the design bug is the asynchronous input, REQ. Being asynchronous, the REQ input may change at any time relative to the clock. Suppose that the REQ signal goes true at a time that violates the setup time of the state flip-flops. Because of skew or slight variations in timing for the flip-flops, some of the flip-flops might respond to the REQ input, and others might not. Suppose that the least-significant state flip-flop responds to the REQ input quicker than the other flip-flops. Then, instead of transitioning from State 1 to State 2, the machine could go from State 1 to State 0. This condition can occur even when the flip-flops are on the same die.

To prevent improper transitions, you can clock the asynchronous signal into one flip-flop, called a "synchronizer" (**Fig 2**). In the above case, the synchronizer would latch the REQ input on a clock edge to produce the signal LREQ. LREQ replaces REQ as the input to the state machine. If the synchronizer responds to the REQ value change before the clock edge, LREQ takes on the new value. If the clock edge precedes the change in REQ, LREQ doesn't change until the following clock edge. LREQ transitions are synchronous to the clock, drastically reducing the state machine's failure rate.

Synchronization causes metastability

A synchronizer prevents most failures caused by an asynchronous input. Unfortunately, a phenomenon called "metastability" complicates synchronization. If an active clock edge and a data transition occur very close together, a flip-flop or a latch may not immediately make a transition from its current state into the new state. The flip-flop may remain in an in-between state, called the "metastable state," for an indeterminate time. Eventually, it settles to a 0 or a 1. While it is deciding, its output may glitch, oscillate, sit at an intermediate voltage, or merely show an increased clock-to-output delay.

The settling time is probabilistic. The longer the time after the clock edge, the more likely that the flip-flop will resolve to a valid state. Unfortunately, there is no guaranteed upper bound on the settling time. You can't build a bistable device such as a flip-flop that cannot go metastable. Its two stable equilibrium states are potential-energy minimums. Between the two minimums is a potential-energy maximum. Because the slope of the energy curve is 0 at the maximum, the maximum is also an equilibrium state, although an unstable one.

The MTBF that results from metastability depends on several factors. One basic metastability equation (**Ref 1**) is as follows:

$$\text{MTBF} = \frac{1}{f_c \times f_d \times T_0} \times e^{\frac{t'}{\tau}}, \qquad \textbf{(1)}$$

where f_c is the clock frequency and f_d is the frequency at which the data input transitions. (For a flip-flop in an arbitration circuit, f_c and f_d would be the frequency of transitions of the two arbiter input signals.) T_0 and τ are device-specific constants. The time allowed for the output to settle is t', which starts at the clock-edge transition. The formula is meaningless, of course, for t' less than the normal clock-to-output delay.

The terms preceding the exponential in the equation indicate how often a flip-flop can become metastable. High clock and input transition frequencies f_c and f_d present more opportunities for metastability to occur. T_0 is a scale factor. You can conceptualize T_0 as the width of a time window around the clock edge during which, if a data transition occurs, the flip-flop becomes metastable. The term $f_c{*}T_0$ is the fraction of the clock period occupied by this time window. Because f_d is the number of data transitions per unit time, $f_d{*}f_c{*}T_0$ is the number of data transitions per unit time that fall within the metastable time window.

The exponential term in the equation describes the probability that a metastable condition will last for time t'. As you increase the time t' that you wait before looking at a flip-flop's output, you exponentially decrease your likelihood of seeing unresolved metastability. The time constant for the exponential term is τ.

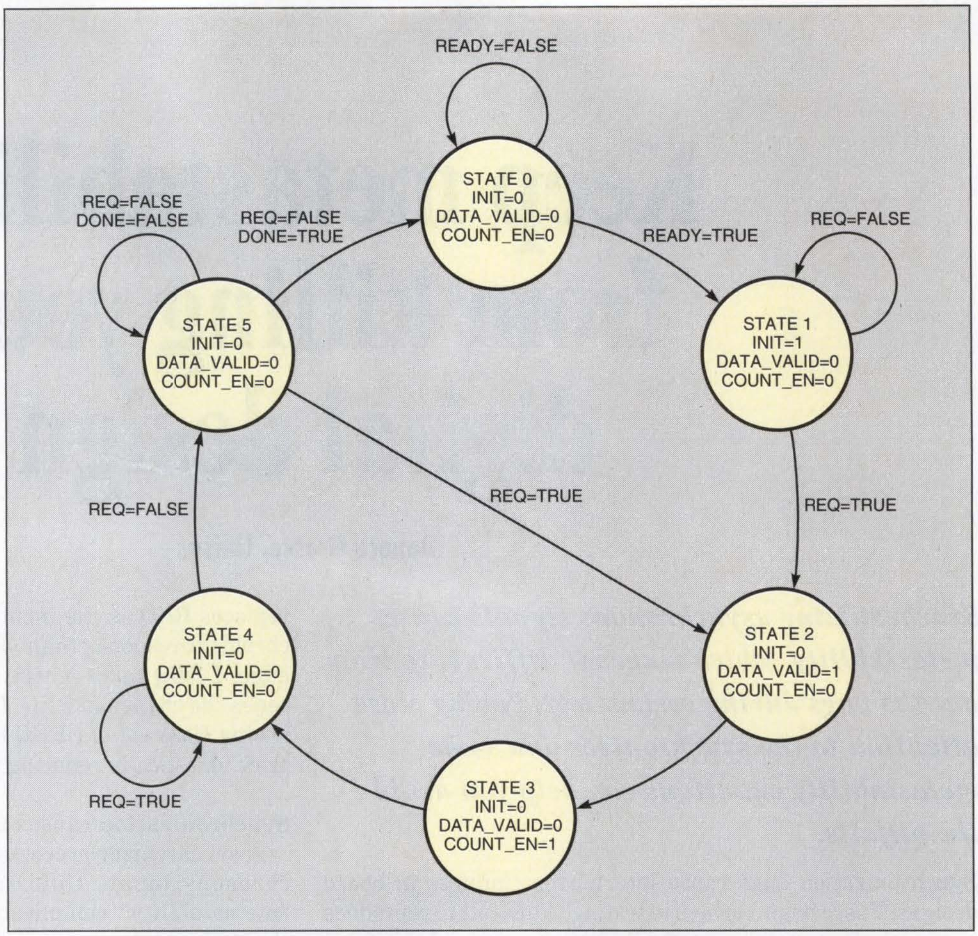

Fig 1—A state machine is prone to state-transition errors caused by asychronous inputs.

To find the probability of a synchronizer failure due to metastability, set t' equal to the maximum time that a synchronizer flip-flop can be metastable without affecting a succeeding flip-flop. Therefore, t' is usually the time interval between the active clock edge at the first flip-flop and the next active clock edge at the succeeding flip-flop, minus the setup time of the second flip-flop and minus the path delay between the two flip-flops (**Fig 3**).

Manufacturers use various forms of the metastability equation. For example, **Ref 2** uses three constants, k1, k2, and Δ_o, giving MTBF in the form

$$\text{MTBF} = \frac{1}{\text{fCLOCK} \times \text{fDATA} \times \text{k1}} \times e^{\frac{\Delta - \Delta o}{k2}}. \quad \textbf{(2)}$$

A little algebra puts this equation into the same form as **Eq 1**:

$$\text{MTBF} = \frac{1}{\text{fCLOCK} \times \text{fDATA} \times (\text{k1} \times e^{\frac{\Delta 0}{k2}})} \times e^{\frac{\Delta}{k2}}, \quad \textbf{(3)}$$

so that T_0 is

$$\text{k1} \times e^{\frac{\Delta o}{k2}}, \quad \textbf{(4)}$$

and τ is k2.

Because metastability formulas aren't standardized, you have to read application notes carefully to understand the manufacturer's definition of each parameter. For example, Cypress (**Ref 3**) defines:

$$\text{MTBF} = \frac{1}{f_c \times f_d \times W} \times e^{\frac{t_r}{t_{sw}}}, \quad \textbf{(5)}$$

where

$t_r = 1/f_c - 1/f_{max}$, $f_{max} = 1/(\text{clock-to-feedback time} - \text{setup time})$,

and

$1/f_c$=the system clock period.

Thus,

t_r=(clock period)–(clock-to-feedback time)–(setup time).

The clock-to-output time of the flip-flop is part of t', as shown in **Fig 3**. The clock-to-output delay is not part of t_r because the delay is subtracted in the clock-to-feedback term. The difference between t' and t_r corresponds to a change in scale factor W relative to the T_0 parameter in **Eq 1**. The path of the potentially metastable output is assumed to be entirely inside one PLD, from one flip-flop through the feedback to another flip-flop, both clocked by the same clock. This configuration is generally the best design, but if your design violates this assumption, you have to adjust this formula.

Because of these variations in parameter definitions as well as differences in the techniques used to detect metasta-

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bility, it is difficult to compare T_0 across manufacturers. However, these variations should not affect τ, the parameter to which MTBF is most sensitive.

The following example calculates MTBF for the REQ synchronizer discussed previously. What is the probability that LREQ will go metastable and that this state won't resolve in time to meet the setup time on the state bits? Using a Cypress 22V10-20 as a synchronizer and assuming that the system clock frequency is 20 MHz and that REQ asserts every 3.1 μsec, you can calculate the MTBF. Because there are low-to-high and high-to-low transitions every 3.1 μsec of the REQ signal, f_d is 0.645 MHz. In addition to these values, you must use the PLD's maximum operating frequency, f_{max}, which you take directly from the Cypress data sheet. The maximum operating frequency is 41.6 MHz. Using the Cypress formula and the W and t_{sw} parameters from the Cypress data sheet yields

$$MTBF = \frac{1}{f_c f_d \times 0.125 \times 10^{-12} s} \times e^{\frac{t_r}{0.190\ nsec}}, \quad (6)$$

where t_r is given as 1/(20 MHz)–1/(41.6 MHz)=26 nsec. Plugging in the values to the equation, yields an MTBF $=1.7\times10^{59}$ sec, or 5×10^{51} years, a very large number.

Suppose, however, that the system clock speeds up to 40 MHz. The MTBF becomes approximately 1 minute, an MTBF figure that is obviously unacceptable.

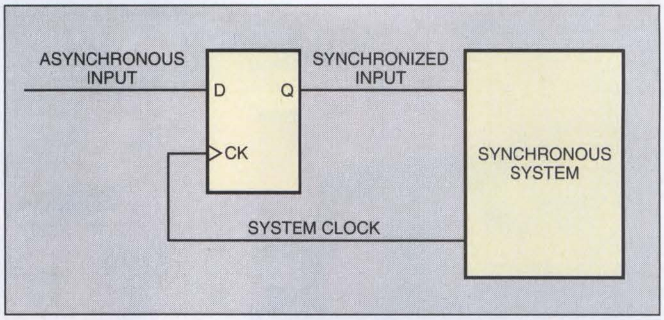

Fig 2—Synchronize an asynchronous input in one circuit only before using it in a synchronous system.

For some systems, you cannot conveniently describe f_d in hertz. For example, an asynchronous input on an image-processing board may change state twice/image. Expressing f_d in units of 1/image gives MTBF as the mean number of images processed between failures.

The MTBF calculated here is for a single synchronizer. Multiple asynchronous inputs to the system yield a lower MTBF than that of a single synchronizer.

Parameter values are not maximums

The calculation is simple. However, finding the parameter values is difficult. Although some manufacturers provide values for T_0 and τ in application notes, many do not. Second,

CALCULATING MTBF FOR A 2-STAGE SYNCHRONIZER

It is difficult to give a formula for the MTBF of a 2-stage synchronizer (**Fig A**). The failure whose frequency is being calculated is the failure of the second-stage flip-flop to resolve by time t′. The clock frequency at the synchronizer flip-flops (f_c) and the data-input transition frequency (f_d) are known. The difficulty is in determining f_{d2}, the number of data-input transitions expected/unit of time for the second flip-flop.

One possible assumption is to let f_{d2} be the probability that the first flip-flop has not settled by one setup time before the clock of the second flip-flop. ($1/f_c - T_{su2}$). Then, the following equation (**Ref 4**) shows the MTBF for the synchronizer, assuming both have the same metastability parameters:

$$MTBF = \frac{1}{f_{d2} \times f_c \times T_0} \times e^{\frac{t'}{\tau}}.$$

By assumption, $1/f_{d2}$=MTBF of the first synchronizer ($MTBF_1$).

$$MTBF_1 = \frac{1}{f_{d1} \times f_c \times T_0} \times e^{\frac{\frac{1}{f_c} - T_{su2}}{\tau}}.$$

Therefore,

$$MTBF = \frac{1}{f_d \times f_c^2 \times T_0^2} \times e^{\frac{t' + \frac{1}{F_c} - T_{su2}}{\tau}}.$$

Because the f_d term appears only once, this is not the square of $MTBF_1$, as is sometimes claimed.

Setting $f_{d2}=1/MTBF_1$ assumes that one uniformly distributed asynchronous data transition occurs each time the first stage goes metastable. One could argue that this assumption doesn't necessarily hold. The apparent f_{d2} depends on the first flip-flop's metastable behavior. For example, oscillations and intermediate voltage levels from the first flip-flop would be more likely to cause setup violations on the second one, producing a larger apparent f_{d2} that would runt pulses and delayed transitions. Nevertheless, errors in f_{d2} are insignificant compared with uncertainties in the exponential term.

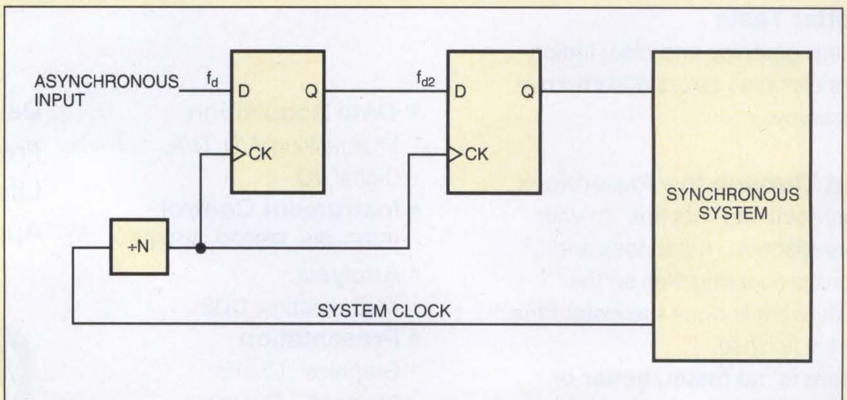

Fig A—Calculating the MTBF of a 2-stage synchronizer requires an estimate of f_{d2}.

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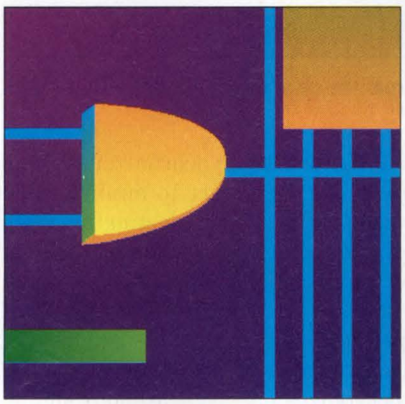

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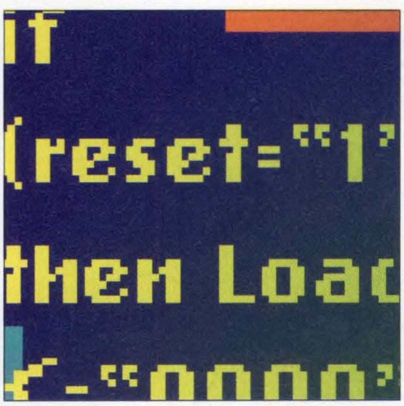

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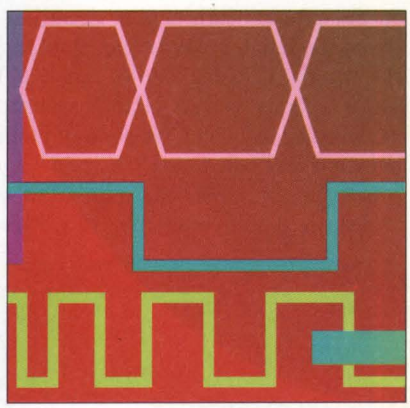

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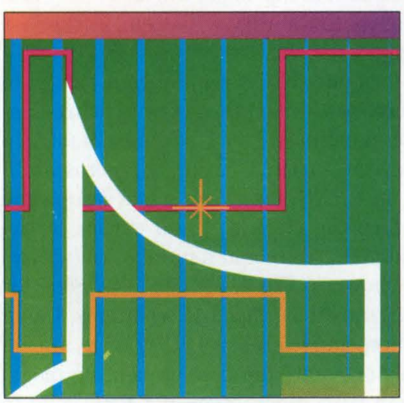

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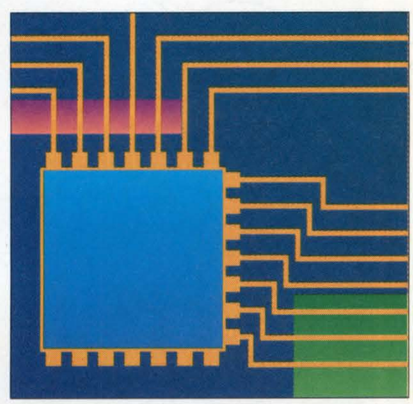

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the reported parameter data may not be very accurate. A scan of the literature shows that numbers for the same type of device vary considerably from one report to another. Reported parameter values are not guaranteed maximums but are usually averages of a few parts tested. Like propagation delays, metastability parameters vary with process variations, voltage, and temperature. Small variations in the time constant τ, especially, cause enormous variations in calculated MTBF because τ is in the exponential term. The material in **Ref 4** discusses the problem of parameter variation, giving an example in which a typical MTBF of 317 years shrinks to 12 minutes when you use estimated worst-case values.

Calculations are useful for getting a rough idea of the magnitude of the metastability problem. Following basic principles helps you to minimize the problem. The most important principle is to allow as long a time as possible for metastable conditions to settle. Clocking the synchronizer flip-flop with the opposite clock edge may speed your design by half a cycle, but it also costs you heavily in MTBF. This method reduces t', thus having the same effect on the exponential term as doubling the clock frequency. In the state-machine example, clocking the synchronizer with the opposite clock would cause MTBF to plummet from 5×10^{51} years to less than 2 minutes. On the other hand, decreasing the clock frequency yields exponential improvements in MTBF.

Simple guidelines can gain a few nanoseconds, which may translate to many multiples of τ. First, if you are implementing a synchronizer in a PLD, put the synchronizer flip-flop and destination flip-flops in the same part to minimize the delay from the synchronizer's output to its destination. Second, you can reduce the effects of metastability by using a multiple-stage synchronizer, which adds stages of pipeline delay. A multiple-stage synchronizer is a chain of flip-flops that synchronizes one asynchronous signal. The output of each additional stage in the synchronizer is less likely to be metastable than is its input. The longer the chain of flip-flops, the less likely it is that metastability will occur at the last stage's output.

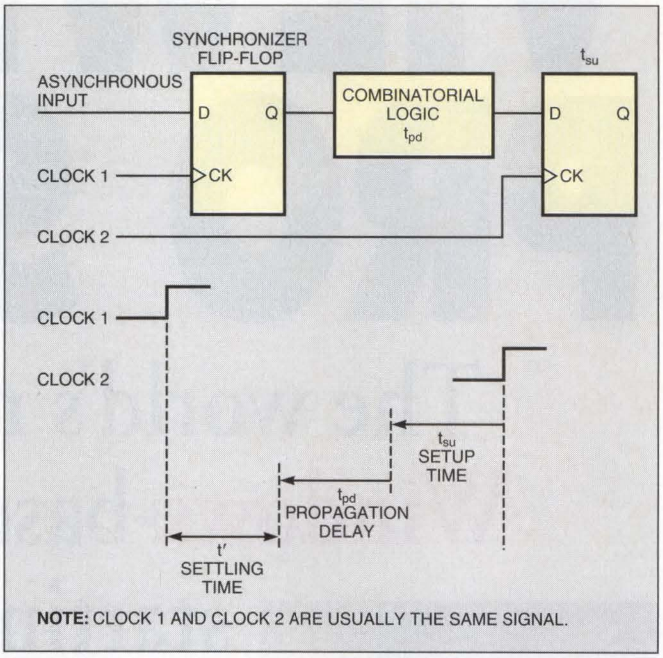

Fig 3—The time interval from the clock edge until a flip-flop's output is valid is defined as t'.

It is possible to rearrange a design to increase the length of the synchronization pipeline without adding latency. In the state-machine example, metastability on LREQ has to settle one setup time before the clock to avoid errors in the state bits. You could renumber the states, as shown in **Fig 4**, using a Gray code for the transitions that LREQ affects. Using this technique, each LREQ edge affects only one state flip-flop, preventing illegal state transitions. Even if LREQ fails to settle one setup time before the clock, an error does not result unless the changing state bit goes metastable and remains metastable long enough to cause further timing violations.

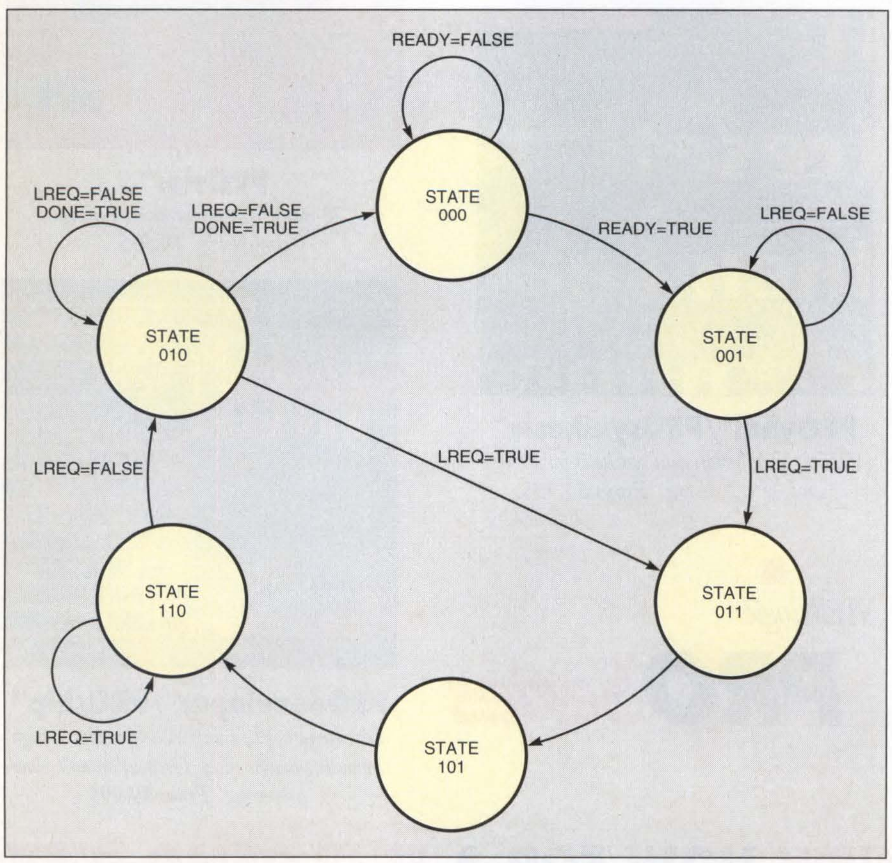

Fig 4—You can increase reliability by allowing the state transitions that are affected by a potentially metastable signal to follow a Gray code.

A third way to improve MTBF is to choose devices with better metastability parameters. Metastability charac-

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teristics depend on circuit factors, such as internal gain-bandwidth product. Faster logic families often—but not always—have faster metastable resolutions. For example, the material in **Ref 1** measures a τ of 0.4 nsec for a sample of 74F74 flip-flops but measures a τ of 1.7 nsec for the ECL 10131 flip-flops. For the same values of f_c, f_d, and t', it calculates an MTBF of 1×10^{13} sec for the Fast family of D flip-flops but only 30 sec for the 10K ECL family of D flip-flops.

Devices claim to be metastable immune

Some devices, specifically designed to avoid metastability, are not guaranteed metastable-free but have small values of T_0 and τ and relatively well-behaved outputs. Philips Components, for example, claims that Signetics designed the "metastable-immune" 74F50XXX family to avoid runt pulses, oscillations, and intermediate voltage states on the outputs (**Ref. 5**).

Using a dual-port RAM or FIFO buffer may seem a way to dodge the synchronization issue. Using these devices, you depend on the IC designer to implement the arbitration for reads and writes correctly. However, you still must think about asynchronous changes in status flags.

Before trying to handle an asynchronous signal properly, make sure that it actually is asynchronous. The metastability equations assume that the input data transition is equally likely to occur at any time during the clock period. In some synchronizing situations, such as an asynchronous interface with a handshake, this assumption may not be valid. Assume that a synchronous-state machine generates a request and that the circuitry at the other end of the interface runs the request through some combinatorial logic and then generates an acknowledge. The timing of the acknowledge is, therefore, correlated with the state machine's clock.

If you treat a clock-correlated signal as an asynchronous signal, the system will probably work fine most of the time. However, each state machine has part delays, and, under some conditions, the system may fail. The delays may be such that the system violates setup times on every transition. The MTBF formulas don't work if the input is correlated with your clock.

Similarly, excessive path delays in synchronous logic can result in the same condition. The delays of some parts could be such that the data input of a flip-flop always makes a transition during the time window that causes metastability. Synchronous logic's advantage is its deterministic timing, but sloppy timing can cause it synchronous logic to be reliably bad rather than reliably good.

If you can't avoid synchronization, follow these basic rules to avoid trouble. First, be aware of which signals are asynchronous. Second, receive each asynchronous signal by clocking it into only one flip-flop. Finally, mitigate against metastability by allowing needed settling time. Design your synchronization scheme, rather than synchronizing ad hoc, and document the scheme so that you keep your design in mind as you make changes. EDN

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Author's biography

Debora Grosse has worked at Unisys in Plymouth, MI, for nine years. She has BSEE and MSEE degrees from the University of Michigan. In her spare time, she enjoys taking walks with her family.

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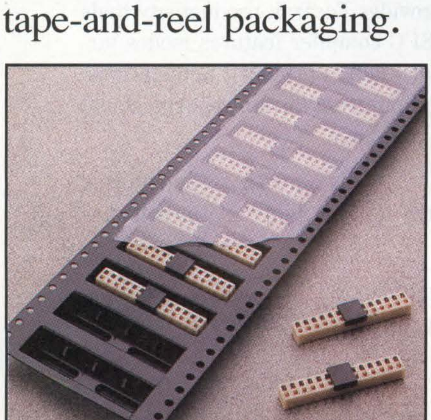

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3M *Reliability*

$59 μC board is programmable in C

The P-57 Mustang is the first in a series of small, low-cost boards that allow you to prototype in C. This first product is based on the PIC 16C57 μC from Microchip Technology. Future boards will contain other 8-bit μCs such as the 80C751/2 from Philips and Motorola's 68HC05 and 68HC11.

The board costs $59; in addition, you can buy the Mustang C development kit for $150, which includes a C compiler, assembler, in-circuit simulator, and source-level debugger along with the 2×3-in. P-57 Mustang board, power supply, and RS-232C cable.

The C compiler generates code for a virtual microcontroller (VMC). The CPU on the board emulates this generic VMC, making the C code portable to future versions of the Mustang board based on other μCs. The μC executes intermediate code up to 20,000 statements/sec, faster than interpreted C or Basic, but slower than compiled C code.

The code runs out of the serial I²C EEPROM. You can quickly download your compiled code from the PC-based host via an RS-232C interface. Once downloaded, the Mustang can operate stand-alone.

The in-circuit simulator emulates the μC's operation on the PC. It operates at PC speeds (often faster than the μC) and drives the μC's pins on the board so your code can exercise the target I/O. The in-circuit simulator also checks for accesses made to uninitialized or unimplemented memory, stack overruns, and other errors. It supports 64 breakpoints, shows the value of up to 32 variables, and can log up to 10,240 execution cycles in a history log.

The PIC 16C57 has 20 I/O lines, 2048×12-bit ROM, 72-byte RAM, and a real-time clock/counter. The board's 8-kbyte EEPROM is expandable to 64 kbytes. The I²C serial bus connects the EEPROM and the μC, providing an inexpensive memory interface that lets you easily expand memory capacity. The μC's on-chip ROM contains the VMC emulation code, application utilities, and basic operating-system services.

A 1×2-in. prototyping area allows you to customize or expand the system. Signals from the μC are available in the prototype area—or you can install a ribbon connector to bring the signals off the board. A 4-wire RS-232C serial interface links the board to a host system. This serial interface is also available to applications. The C compiler contains common I/O functions to control the interface.—**David Shear**

P&E Microcomputer Systems Inc, Woburn, MA. (617) 353-9206. **Circle No. 338**

With the Mustang board series, which is based on popular μCs, you can use C to create prototypes quickly and easily.

VRTX moves to μCs

VRTXmc is a new version of the VRTX real-time operating system (RTOS) designed for use with μCs. Many embedded applications, such as handheld devices, have very limited RAM/ROM. This new version reduces the RAM requirement to less than one-third of that required by the VRTX32 kernel, requiring only 1-kbyte RAM for a typical embedded application. The VRTXmc kernel needs only 3 to 6 kbytes of ROM space.

VRTXmc, the third member of the VRTX family, is compatible with the Spectra cross-development backplane and the XRAY debugger. It is a subset of VRTXsa and includes preemptive scheduling, mailboxes, event flags, queues, partitions, optional time slicing, and other services.

It now supports Motorola 68000/302 and CPU32 targets. A single development license starts at $1000 (10 production licenses cost $332).

—**David Shear**

Microtec Research Inc, Santa Clara, CA. (408) 980-1300. **Circle No. 339**

RAMDAC families support true color for PCs and workstations

Two families of RAMDACs from AT&T Microelectronics support true-color graphics at resolutions from 640×480 to 160×1200 pixels. The 21C505/504, 20C506, and 20C510/511 for high-performance PCs and the 20C567/565/568 for high-performance workstations support multiple-color display modes that can bypass or use red, green, and blue, on-chip, 256×8-bit color-look-up RAMs. The display includes 8-bit pseudocolor, 15/16-bit high color, and 24-bit true-color choices.

The families offer ±5% brightness accuracy, on-chip clock synthesizers, and precision PLL-based analog clock multipliers. Register-level compatibility allows you to amortize software development across a range of products at different prices and performance levels. An on-chip integrated voltage reference permits precision trimming of the voltage reference and DAC output current. The DAC output current error is less than 3%.

Two families of RAMDACs offer true-color graphics ranging from 640×480 to 160×1200 pixels. On-chip DAC output current error is less than 3%.

On-chip multipliers allow the RAMDAC to accept a load clock signal directly from the frame buffer and create the appropriate pixel clock. A multiplexed pixel format allows the frame-buffer memory to operate slower than the pixel clock, permitting the use of lower-cost memory. The ICs are available in 135-, 150-, and 170-MHz speeds. The entry-level 21C504 is also available at 85 and 110 MHz.

The company has incorporated power-saving features into the RAMDACs to minimize operating-power dissipation. The midrange family members dissipate around 1.5W, and the high-end members dissipate around 1.8W. The devices also support power-management schemes under software control. The RAMDACs operate in one of four reduced-power modes.

The 21C505/504, 20C506, and 20C510/511 ICs offer 32- and 64-bit pixel ports. In addition to the on-chip color-look-up table, all of the ICs offer hardware cursor support, overscan RAM for border colors, and a dedicated 8-bit SVGA port. The display modes range from 10 to 38, depending on the device. Prices range from $11 to $32 for 135-MHz versions (10,000).

—John Gallant

AT&T Microelectronics, Allentown, PA. (800) 372-2447. **Circle No. 340**

Communications engine combines three processors

The MC68356 communications processor separates communication tasks into three functions and provides a processor for each. A 25-MHz general-purpose μP core handles communications protocols and high-level command interpretation. A microcoded RISC processor handles bit-level manipulation, such as formatting and bit- ordering. A 60-MHz DSP μP with on-chip RAM and ROM handles encoding, compression, and other math-intensive tasks.

The device is a blend of the MC68302 communications controller and the DSP56002 24-bit digital signal processor, retaining software compatibility with each. The MC68356 provides three serial communications channels capable of handling a variety of protocols, including UART, bisync, and HDLC/SDLC. The RISC processor controlling bit-level tasks can automatically determine the baud rate and format of incoming data. Two DMA controllers—one for transmit and one for receive—support each serial channel.

Three control interfaces connect the 68356 to its environment. One allows connection of the 68000 CPU to the host system. Another allows direct connection to the 56002 DSP. The third interface allows the device to serve as a PCMCIA slave or, alternatively, emulate a 16550 UART. The UART emulation permits the 68356 to act as if it were a serial port on the IBM PC/AT.

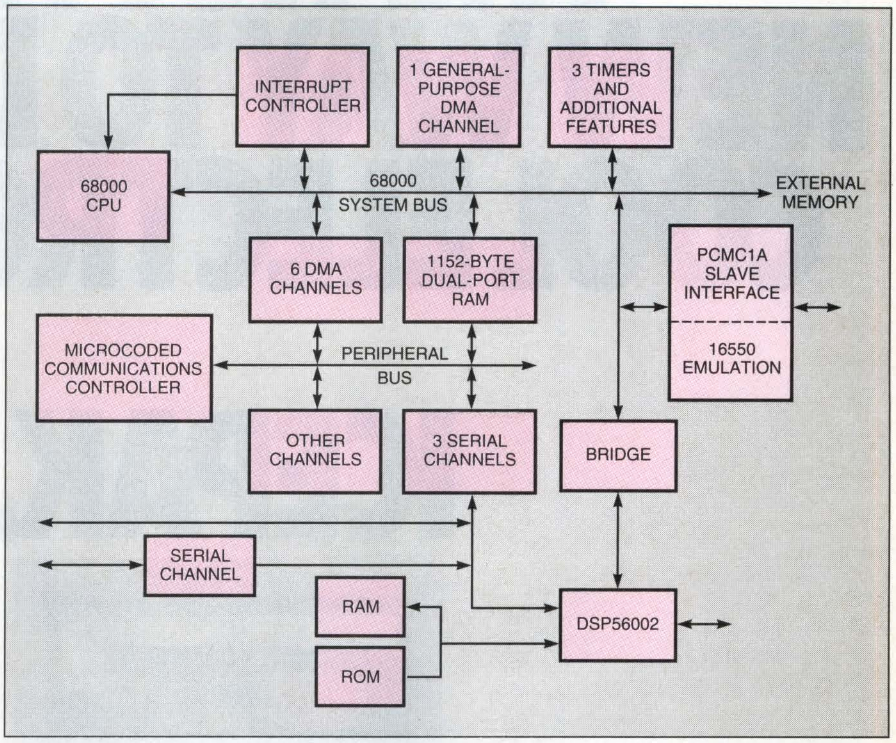
The device also provides three internal communication paths between the DSP and the 68000. The DSP connects to the 68000's host bus, allowing the 68000 to program and control the DSP. The link also allows the DSP to read and write directly to memory on the 68000 bus. The two paths further connect through one of the serial channels, allowing high-speed data transfers directly between the processors.

Clocking the device can simply be a matter of providing a clock or crystal operating anywhere between 25 kHz and 6 MHz. Internal phase-locked loops provide all the clocks needed for serial communications and processor operation. The processors are fully static, allowing the device to control power consumption by adjusting clock speeds or stopping clocks in a variety of low-power modes.

The device incorporates JTAG boundary-scan circuits for checking connections between the 357-pin ball-grid-array package and the circuit board. It also provides an on-chip emulation capability to simplify debugging. In support of application development, Motorola is offering a $1995 Application Development System (ADS), which includes an evaluation board that can connect to a Sun-4 or IBM computer or to a dumb terminal. The ADS will be available by the third quarter.

The 68356 begins general sampling in August; production is scheduled for the fourth quarter ($64.95 (10,000)). A version optimized for modem applications, the 68356M, is planned for later in the year; the M version will be preprogrammed with V.34 data pump software.**—Richard A Quinnell**

Motorola, Inc, Austin, TX. (512) 891-2429. **Circle No. 341**



The MC68356 combines MC68302 communications-controller functions (shown above) with a 56002 DSP core.

SCSI chip boosts server I/O transfer rates

By processing as many as 255 data requests simultaneously, the ASC1000 SCSI-2 controller reduces data-access overhead in multitasking system and server applications. The device can use up to 94% of the SCSI bandwidth on a sustained basis.

The controller comes in two varieties: The ASC1000 has a 32-bit VESA local-bus interface; the ASC1200 has a 32-bit PCI local-bus interface. Both contain a RISC processor, DMA circuit, byte-wide SCSI-2 handshake logic, and a 128-byte FIFO memory.

The RISC processor coordinates activities within the chip and replaces much of the needed handshaking logic with microcode. In addition, to speed data retrieval it runs scatter-gather algorithms to keep data blocks for files grouped together on the disk drives. In server applications, the device also tags incoming disk data with an identifier that links it to specific requests.

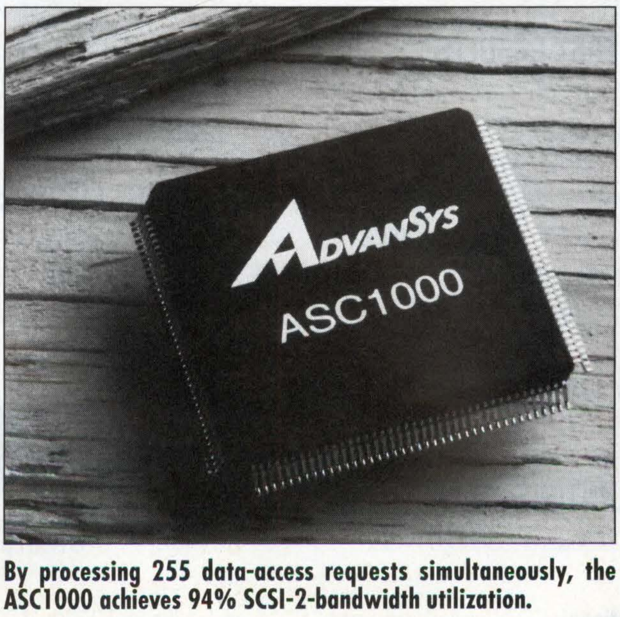
The DMA processor allows the device to produce sustained data-transfer rates of 120 Mbytes/sec on the local bus without CPU intervention. Acting as a safety net to the high-speed transfers, a 128-byte FIFO buffers the incoming data.

The device comes with diagnostic software that allows it to configure itself to the system. On activating a switch, the device searches for available IRQ lines and for its address within the system. Other software available with the device includes an ASPI (advanced SCSI programming interface) manager and drivers for a variety of hard-disk, tape, and CD-ROM drives as well as scanners and printers. The drivers are available for DOS, Windows, OS/2, and Novell Netware.

The ASC1000 costs $21.95 (1000) (now in production). The ASC1200 costs the same and begins sampling in July (full production scheduled for September). Both come in 160-pin PQFP packages.

—Richard A Quinnell

AdvanSys, San Jose, CA. (408) 383-9400. **Circle No. 342**

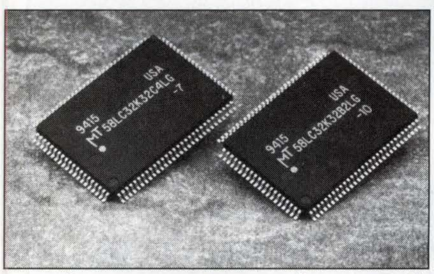


By processing 255 data-access requests simultaneously, the ASC1000 achieves 94% SCSI-2-bandwidth utilization.

INTEGRATED CIRCUITS

PEEL arrays unrestrict PAL-block CPLDs. The PA7128 and PA7140 programmable electrically erasable logic (PEEL) arrays combine a segmented PLA with field-programmable gate-array (FPGA)-like logic cells. This approach frees users from the architectural restrictions of PAL-like blocks of segmented complex PLDs. The company is offering its Place development software and fitters for popular third-party software, such as Data I/O's ABEL, free to qualified users. All the devices use CMOS EEPROM. The main elements of the PEEL array include flexible FPGA-like logic-control cells. I/O cells and global cells are interconnected via a wide-gate PLA. 66-MHz PA7128J, $3.60 (1000). **ICI Inc**, San Jose, CA. (408) 434-0678. **Circle No. 343**

4-Mbit flash memory has selectable organizations. The M5M28-F400 4-Mbit flash memory for nonvolatile reprogrammable storage offers a user-selectable organization of 256×16 or 512k×8 bits. The chip also offers 32 symmetrical erase blocks of 16 kbytes or 8k words each. The maximum active supply current is 30 mA, and the device can read using a 5V power supply. Programming and erasing use a 12V power supply. Other features include power-up/power-down protection, automated program/erase and 10,000 program/erase cycles/block. To prevent overerasure, an embedded timer controls the program/erase pulse widths. $23 (10,000). **Mitsubishi Electronics America Inc**, Sunnyvale, CA. (408) 730-5900. **Circle No. 344**

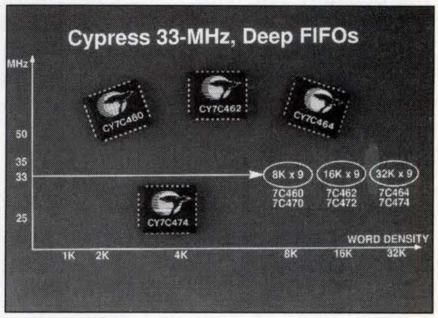


Synchronous SRAMs have 32k ×32-bit organization. The MT58-LC32K32 SyncBurst static RAM (SRAM) has a 32k×32-bit organization. These wide, synchronous SRAMs offer zero-wait-state read and write-cache memory for high-performance µPs, such as the Pentium and the PowerPC. The devices deliver a data rate as fast as 500 Mbytes/sec using a low-voltage TTL interface. The device operates from 50 to 125 MHz and employs a 3.3V power supply. The inputs and outputs are 5V tolerant, which allows the SRAMs to connect directly to 5V parts without using translators. The devices support 4-cycle burst accesses and pipelined and nonpipelined operations. $35. (100). **Micron Technology Inc**, Boise, ID. (208) 368-3900. **Circle No. 345**

FPGA family features 233-MHz data paths. The X3100A family of field-programmable gate arrays (FPGAs) features 233-MHz data paths, 180-MHz loadable prescaled counters, and >300-MHz toggle rates. The family achieves average Programmable Electronics Performance Corp (PREP) benchmark speeds of 85 MHz. The combinatorial delay is 2.2 nsec, the configurable-logic-block (CLB) clock-to-output time is 1.7 nsec, and the CLB setup time is 1.8 nsec. The devices use a 0.8-µm process. Prices start at $17.50 (100). **Xilinx Inc**, San Jose, CA. (408) 559-7778. **Circle No. 346**

CPLDs feature low power. The ATV2500B, a 44-pin complex programmable-logic device (CPLD), uses a 0.65-µm manufacturing process. The chip offers 12-nsec propagation delays and 10-nsec pin-to-pin delays. The low-power device draws 2 mA of standby current and contains 24 flexible macrocells that have 17 product terms each and are globally connected by a single AND/OR matrix, which provides 100% connectivity. Each macrocell has two flip-flops that can be configured as D- or T-Type. Both registered nodes and a third combinatorial node can all be buried. A PLCC version costs $19.75 (100). **Atmel Corp**, San Jose, CA. (408) 441-0311. **Circle No. 347**

Chip set plays video CDs. The TMS32AV220 MPEG video decoder, the AV120 audio decoder, and the AV420 NTSC encoder provide all the major functions to create a player that accepts compressed video-CD signals and produces synchronized NTSC sound and video for television display. The AV220 connects directly to the CD-ROM and decompresses 176×144-pixel MPEG-I video, strips out the digital audio information, and provides audio-synchronization control. The AV120 works with the chip set or serves as a stand-alone MPEG audio decoder. The AV420 converts digital video to NTSC analog video, interpolating scan lines to create a full-screen image. In volume, the chip set costs <$40. **Texas Instruments Inc**, Denver, CO. (800) 477-8924, ext 4500. **Circle No. 348**



FIFO memories are 32k×9 bits. The CY7C464 and CY7C474 32k×9-bit FIFO memories address large memory systems, such as those used in asynchronous-transfer-mode (ATM) networks. The devices provide data buffering for systems running as fast as 33 MHz. They have an access time as fast as 15 nsec and draw 110 mA from the power supply. Additional features include programmable flags to signal almost-full and empty status and a mark-and-retransmit feature that supports regeneration of packet information during transmission. The devices are available in PLCC and DIP packages and have access times of 15, 20, 25, and 40 nsec. A 40-nsec PLCC version costs $58.15 (100). **Cypress Semiconductor**, San Jose, CA. (408) 943-2600. **Circle No. 349**

16-Mbit DRAMs have self-refresh. The TC51V16160AJS and 8160AJS are 16-Mbit dynamic RAMs (DRAMs) organized as 1M×16 bits. The devices suit the personal-digital-assistant market and come with self-refresh, which allows the DRAM controller and the clock to be turned off instead of refreshing the DRAM. The self-refresh feature draws 80 µA of refresh current. The DRAMs operate from 3.3V and have 70- or 80-nsec access times. $120 for an SOJ-packaged version (1000). **Toshiba America Electronic Components Inc**, Irvine, CA. (714) 455-2000. **Circle No. 350**

LCD-column drivers provide 256,000 colors. The CL-FP65xx family provides banks of column drivers for color active-matrix LCDs. The drivers offer 6-bit resolution, producing as many as 256,000 colors on a compatible LCD panel. The 652x series offers 192 output channels, the 651x offers 201 channels, and the 650x offers 240 channels. The devices operate from a 3.3 or 5V supply and drive the LCD as fast as a 75-Hz refresh rate. The devices come in a TAB package for greatest packaging density. The 652x costs $14 (1000); the 651x, $15.50; and the 650x, $17. The 650x is available for sampling now, and the company has scheduled production for the fourth quarter; the others are in production. **Cirrus Logic Inc**, Fremont, CA. (510) 226-2011. **Circle No. 351**

Chip set encodes MPEG audio live. The Musicore DSP chip set encodes all forms of ISO/MPEG-I audio, including stereo, joint stereo, and single- and dual-channel, in real time. The device's software also compresses the audio information based on psycho-acoustic modeling. A minimal chip set includes a boot ROM with the Musicore encoder and decoder software and an 8XC51 microcontroller running the Musicore management program. You add a DSP56002 and three static RAMs to complete the circuit. The minimal set costs $400 (sample quantities) or $40 (1000). **Philips Semiconductors**, Sunnyvale, CA. (800) 447-1500. **Circle No. 352**

Workstation 3D graphics comes to the PC. The GLiNT 300SX and 300TX are 3D-graphics processors with PCI interfaces for desktop computers. The processors implement the pixel-processing layers of the OpenGL 3D software standard, which future releases of Windows will include as Windows' 3D-graphics application-programming interface. The devices can produce 300,000 shaded, Z-buffered, anti-aliased, translucent polygons/sec, and the 300TX can accelerate texture mapping. When used with graphical user interfaces, the devices achieve 100,000 24-bit WinMarks. The 300SX costs $150 (50,000); the 300TX will be available by year-end. **3Dlabs Inc**, San Jose, CA, (408) 436-3455. **Circle No. 353**

RAMDAC switches modes each pixel. Incorporating two PLL clocks, a triple 256×6-bit palette, and triple 135-MHz DACs, the CH8398 RAMDAC provides a wide range of operating modes. It handles VESA, VGA, SVGA, and XGA with 8-bit pseudocolor and 5-5-6 color modes along with 24-bit bypass. It switches between modes on a pixel-by-pixel basis, allowing combination of lower-resolution, full-color windows within a high-resolution screen. The device provides an 8- or 16-bit pixel interface accepting data at 67.5M pixels/sec. Price of the 68-pin PLCC is <$10. **Chrontel Inc**, San Jose, CA. (408) 383-9328. **Circle No. 354**

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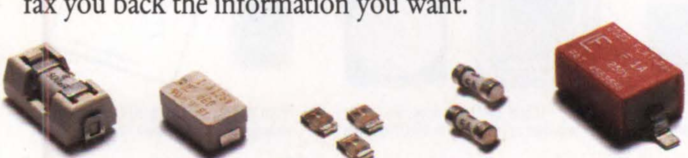

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CIRCLE NO. 36

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Company lowers price on PLD software. The Max+Plus II PLD software now starts at $495. You can add support for the Max 7000 or Flex 8000 devices for $995 each. The software provides schematic capture, text entry using the company's hardware-description language, timing analysis, logic synthesis, fitting, timing, annotated Verilog or VHDL output, and a bidirectional EDIF interface. **Altera Corp**, San Jose, CA. (408) 894-7110.
Circle No. 355

HDL-code generator is now available on Windows NT and Unix. ACEPlus Designer is now available on both PCs and workstations. The tool automatically generates VHDL, Verilog, or ABEL hardware-description languages (HDLs) from graphical design descriptions. ACEPlus Designer costs $3500. **Intergraph Corp**, Huntsville, AL. (800) 837-4237.
Circle No. 356

Neural network software learns quickly. The Neural Network Toolbox 2.0 uses a training method that learns 10 times faster than using conventional back-propagation learning algorithms, according to the vendor. Prices for the PC version of the software begin at $895. **The MathWorks Inc**, Natick, MA. (508) 653-2997.
Circle No. 357

Tool simplifies wire-harness design, layout, and documentation. The E3LCable tool ($9900) helps you create interconnect designs more efficiently and earlier in the design process. The tool provides transparent data exchange between the electrical and mechanical phases of interconnect design. The tool works with the company's Logical Cable tool. **Mentor Graphics**, Wilsonville, OR. (503) 685-8000.
Circle No. 358

Floor planner helps reduce IC-layout iterations. ArcCell 2.3 works with Synopsys' floor-plan-manager and logic-synthesis tools to communicate path constraints to the timing-driven layout tools. According to the company, the layout tool can often produce an optimal layout in a single pass. The ArcCell timing-driven option costs $50,000, and the Synopsys interface costs $15,000. **ArcSys Inc**, Sunnyvale, CA. (408) 738-8881.
Circle No. 359

System-design tool offers workstation performance for $4995. FlowHDL 2.0 runs on workstations and provides the tools you need to enter a design graphically, verify, analyze, and automatically generate code in VHDL or Verilog. **Knowledge Based Silicon Corp**, Columbia, SC. (803) 779-2504.
Circle No. 360

SHORTS

The Magellan 3.0 Verilog debugging environment starts at $1995 and includes a source-level debugger, a navigator, a waveform display and logic analyzer, and a register-transfer-level behavioral block viewer. **System Science Inc**, (415) 812-1800. **Circle No. 361**

The 7.0 revision of P-CAD Master Designer for pc-board design offers an integrated aperture table for WYSIWYG imaging, enhanced on-line design-rule checking, autodimensioning, and an improved user interface. The software runs on DOS and Unix systems; prices begin at $1995. **Altium Inc**, (408) 534-4140. **Circle No. 362**

The ADSpice library of 392 Spice models is available on 3.5-in diskettes. The free library includes 40 new macromodels, including video amplifiers, buffers, references, and analog multipliers. **Analog Devices Inc**, (617) 329-4700.
Circle No. 363

Design Center from MicroSim is now fully integrated with Cadence's Design Framework II, providing a complete analog, digital, and mixed-signal circuit-design environment for Sun workstations. The Cadence integration product sells for $4950 domestically and $6450 internationally. **MicroSim Corp**, (714) 770-3022. **Circle No. 364**

Boards extend range of Multibus offerings

Continuing its support of the Multibus architecture, Intel Corp introduced a range of boards for both Multibus I and II. The offerings include communications modules for local- and wide-area networks (LANs and WANs), peripheral interfaces, and computer boards with flash-memory options.

The iSBC 221S SCSI controller provides an upgrade path for ST506 and ESDI disk-drive users in Multibus I systems. By offering two I/O protocols, the 221S allows you to use SCSI-2 disk drives without changes to the software drivers of older systems, or it provides full SCSI-1 and SCSI-2 capability. The board can handle as many as seven peripheral devices in full-SCSI mode or handle four SCSI hard-disk, SA4xx floppy-disk, or QIC-02 tape drives using the I/O Parameter Block protocol. The board includes a 256-kbyte flash memory and a 512-kbyte cache; it costs $1450.

The iSBC 282 Ethernet controller is an add-on module for Intel's Multibus I boards and connects to the AUI (attachment-unit interface) on thick Ethernet cables. The $350 module uses the same network drivers as the EtherExpress 16 board and is software configurable. It comes with drivers for the NetWare, LAN Manager, 3+ Open, and Vines network operating systems.

The MIX232 and MIX422 also are add-on modules, but they follow the Modular Interface Extension (MIX) used in Multibus II boards. The modules both offer eight individually programmable communications ports operating as fast as 39.4 kbaud and are stackable to offer as many as 24 total ports. The MIX422 provides RS-422 signals and supports the RS-449 and X.21 communications protocols; it can operate at 1.544 Mbps on selected channels. The MIX232 provides an RS-232C interface. Each module costs $2695.

The iSBC 386/12 and 486/12 Multibus I single-board computers include sockets for holding up to 512 kbytes of flash memory. The boards come with 66-MHz 486 DX2, 33-MHz 486, or 20-MHz 386 processors, DMA control, and up to 64 Mbytes of DRAM. The flash-memory sockets include the circuitry necessary for in-system programming. Programming instructions and sample code are available on the Intel Bulletin Board; phone (916) 356-3600 for access.—**Richard A Quinnell**

Intel Corp, San Jose, CA. (800) 438-4769. **Circle No. 464**

Power PC processor comes to VMEbus

The PowerPC processor architecture has made it to the VMEbus in the form of the MVME160x computer-board family. The boards employ a modular architecture to provide a range of CPU and memory options with a common base. Options include 66- or 100-MHz CPUs and as much as 128 Mbytes of DRAM.

The 160x family base boards contain the peripheral devices linked over a 32-bit PCI local bus running at 33 MHz. Peripherals directly on the PCI bus include Ethernet and wide-SCSI-2 ports and an SVGA driver. Bridges connect the VMEbus and low-speed peripherals such as parallel I/O, mouse, and keyboard to the PCI bus. The base board also offers an IEEE P1386.1 PCI Mezzanine Card option, providing a mechanism for adding other I/O capabilities.

The CPU, along with its local ROM and secondary cache, plugs into the PCI bus through a socket on the base board. The module can contain either a 66-MHz PC603 processor or a 100-MHz PC604 processor; its design ensures that all high-frequency signals remain within the module and that the CPU remains decoupled from the PCI bus. The CPU's main memory resides on a third pc board that connects directly to the CPU module. The memory can range from 8 to 128 Mbytes.

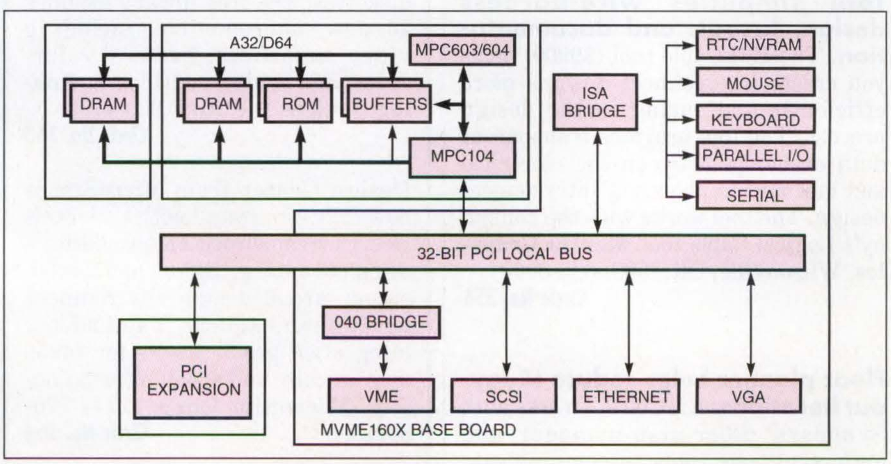
Despite all the module stacking, the MVME1603—containing the PC603 processor—fits into a single 6U slot in a VME system. The MVME1604 occupies more than a single slot width due to the height of the CPU's heat sink. As lower-power versions of the PC604 become available, the interference problem should vanish.

The MVME160x family comes with extensive software support. Motorola offers its VMEexec real-time development software for PowerPC modules. In addition, real-time kernel vendors have committed to supporting the family with their products. Vendors include Integrated Systems (pSOSystem), Lynx Real-Time Systems, Microtec Research (XRAY, VRTX), Microware Systems (OS-9), and Wind River Systems (VxWorks, WindPower).

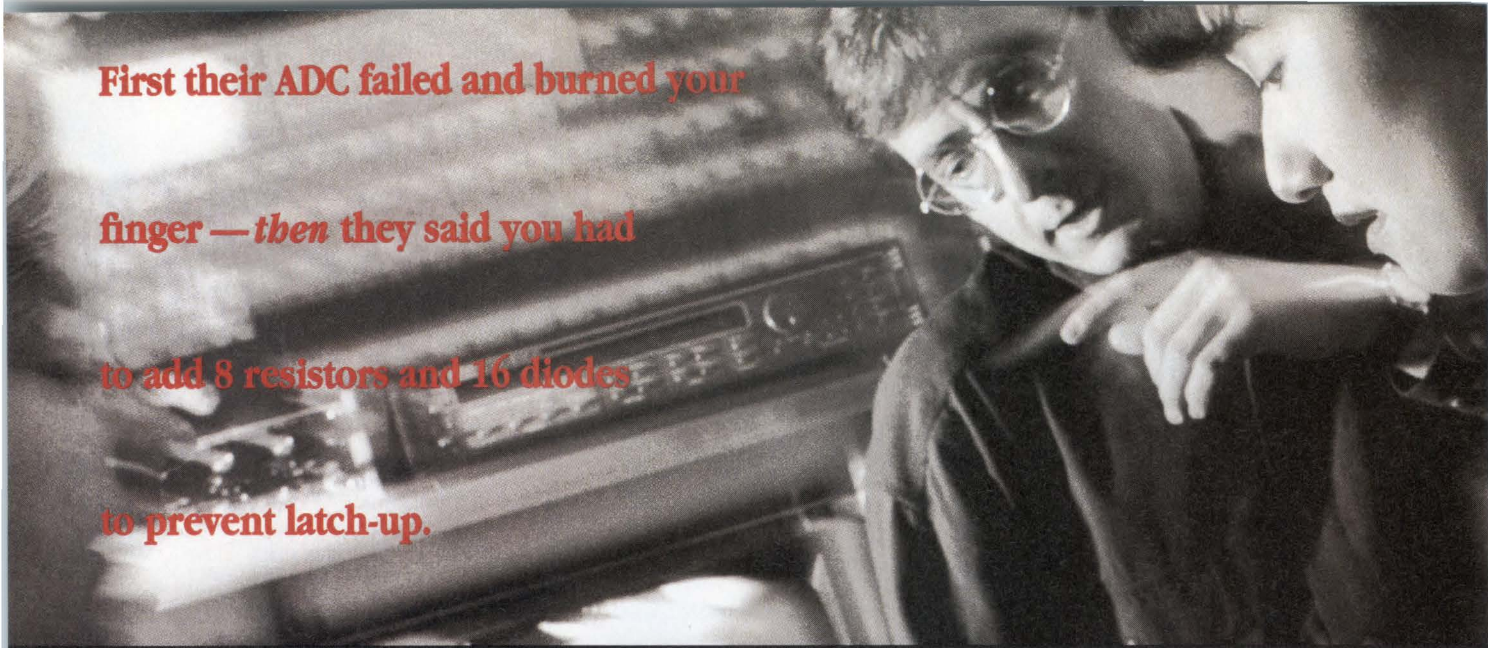
The boards come with a 5-year parts-and-labor warranty for factory repair. The MVME1603 will be available in September; an 8-Mbyte DRAM configuration costs from $3575. The MVME1604 starts at $4575 and will be available in November.—**Richard A Quinnell**

Motorola Computer Group, Tempe, AZ. (800) 759-1017, ext PR.

Circle No. 465



Modularity is the hallmark of the MVME1603/4 board designs. CPU, main memory, and peripherals are located on separate, interconnecting pc boards.



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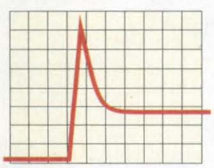

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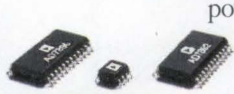

SPECIFICATION	AD7890	AD7893	AD7892
Throughput (ksps)	100	117	500
Channels	8	1	1
Power Dissipation	30 mW	25 mW	60 mW
Price (1000s)†	$10.20	$9.00	$13.60

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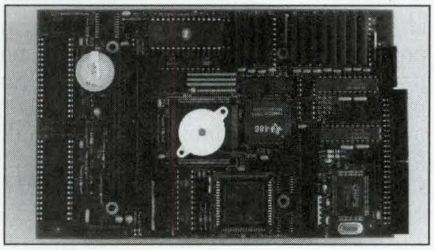
BOARDS & BUSES

DSP boards stack on PC/104 bus. The PC5-DO board uses a 50-MHz DSP32C processor to perform IEEE-compatible 32-bit floating-point arithmetic. The boards use the PC/104 interface and are stackable for greater performance. Stacked boards communicate through a 25-Mbps serial port. They also offer a 32-bit, 100-Mbyte/sec mezzanine connector for attaching I/O daughtercards. The daughtercards provide several audio options, including voice codec and dual-channel audio I/O ports. The board costs $1395. **Communication Automation and Control Inc**, Allentown, PA. (215) 776-6669. **Circle No. 365**

FDDI adapters run sans CPU. The 1250 series of VME boards contains an ASIC that handles communications control for synchronous and asynchronous FDDI (fiber distributed data interface). The ASIC eliminates the need for a CPU and associated circuitry, lowering the cost of the adapter. The boards come in single- and dual-attachment configurations and can work with fiber or unshielded twisted-pair (UTP) network media. The boards also offer an optional content-addressable memory to speed address matching. Their streams-based link-level software is available for Sun, Data General Avion, and Hewlett-Packard 700i series controllers. Prices begin at $2995 for UTP-based and $4195 for fiber-based boards. **Rockwell Network Systems**, Santa Barbara, CA. (805) 968-4262. **Circle No. 366**

Ruggedized VME boards use Pentium CPUs. The RPC series of 6U VMEbus-based PC-compatible boards offers a –40 to +85°C operating-temperature range as well as shock, vibration, and humidity immunity. The boards include a 486 or a Pentium CPU; 64 Mbytes of RAM; VGA, Ethernet, and SCSI-II interfaces; and a PC-104 expansion bus. The boards' VGA controllers handle resolutions of 1280×1024 pixels. The boards also offer two serial ports, a bidirectional Centronics printer interface, and a PS/2 mouse port. **or Industrial Computers**, Reading, Berkshire, UK. 0734-331010. **Circle No. 367**

STD 32 board connects to Interbus-S. The UE9002 connects the STD 32 bus to the Interbus-S distributed serial-I/O system developed by Phoenix Contact (Harrisburg, PA) for industrial monitoring and control. The board operates as a master or a slave on the Interbus-S, depending on system needs. As a bus master, it controls as many as 4096 I/O points. The interface is programmable in Basic, Pascal, and C. The board costs $495, and an optically isolated version costs $795. **Universal Systems**, Flint, MI. (810) 785-7970. **Circle No. 368**



Single-board PC/ATs sport 486SLC CPUs. Two boards patterned after the IBM PC/AT architecture are available in a 4.5×7.1-in. form with a PC/104 expansion connector. The SAT-496SLC-33 ($995) and SAT-386SX-25 use 25-MHz 386SX and 33-MHz 486SLC processors, respectively. A clock-doubled version of the 486SLC is also available. Each board handles as much as 4 Mbytes of dynamic RAM, offers three sockets for EPROM or flash memory, and can be jumpered to boot from RAM- or ROM-based DOS. The boards include the full AT motherboard, including keyboard and speaker interfaces. Add-in cards connect to the PC/104 interface. **WinSystems Inc**, Arlington, TX. (817) 274-7553. **Circle No. 369**

Single-board computer uses FPGA. The 188SBC is a single-board computer based on the 80C188 processor. It provides 12- or 16-bit ADC and DAC, serial and parallel ports, a PC/104 expansion bus, and a field-programmable gate-array (FPGA) socket. The socket accepts a Xilinx 3000-series FPGA, which the processor can configure to provide custom capability to the board. The board also offers 512 kbytes of battery-backed static RAM, keyboard and LCD interfaces, sockets for as much as 2 Mbytes of EPROM, and flash programming circuitry. Prices range from $299 to $750. **HiTech Equipment Corp**, San Diego, CA. (619) 566-1892. **Circle No.370**

SPARCstation 10-compatible VME board holds four CPUs. The SPARC 10MP is a 6U VME board with 100% binary compatibility with the SPARCstation-10 workstation family. The board holds four Fujitsu HyperSPARC or two Texas Instruments SuperSPARC processors operating as fast as 80 MHz. The board runs standard Solaris 1.1 and 2.3 operating systems; accepts ECC memory-expansion modules with as much as 256 Mbytes of RAM; offers two SBus slots; and includes Ethernet, SCSI-II Fast, serial, and Centronics ports. Prices start at $12,995 for a board with 32 Mbytes of memory. **Themis Computer**, Pleasanton, CA. (510) 734-0870. **Circle No. 371**

DSP board employs data-flow architecture. Based on six 50-MHz TMS320C40 DSP processors, the DSP-46 VME board accepts data at 160 Mbytes/sec. The board uses a 68040 processor to control data flow, allowing a parallel or pipelined data-processing structure. Each DSP on the board has a 1-Mbyte private RAM (expandable to 16 Mbytes), and all processors share a 4-Mbyte memory block as well as the VME64 interface. Three of the DSPs connect to a FIFO-buffered, 50-Mbyte/sec, 36-bit parallel port to the board's front panel. All processors connect to the 160-Mbyte/sec ScreamerBus on the backplane. The board costs $17,749. **PC/M Corp**, Dublin, CA. (510) 829-8700. **Circle No. 372**

SHORTS & REVISIONS

Heurikon Corp has purchased the design and manufacturing rights to the RISQ Modular Systems' line of MIPS-based VME boards. Heurikon will continue to market the RISQengine 6e board, replacing it this year with an R3000-based board. **Heurikon Corp,** (608) 831-5500. **Circle No. 373**

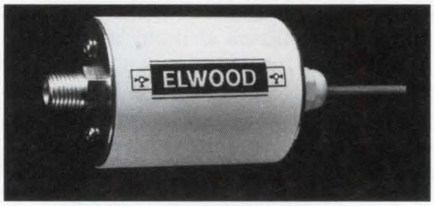
With the introduction of its Type-3 digital I/O mezzanine module, Valley Technologies now has a port that keeps pace with the company's UltraDSP board's processing power. The $10,000 module allows the DSP board to sustain a 20-MHz data-input rate for block sizes as large as 32 kbytes. **Valley Technologies**, (717) 668-3737. **Circle No. 374**

Ampro has upgraded its Little Board/486 single-board computer by adding a version using the Intel 80486DX2 CPU. The board is now available in 33- and 66-MHz versions. **Ampro Computers Inc**, (408) 522-2100. **Circle No. 375**

COMPONENTS

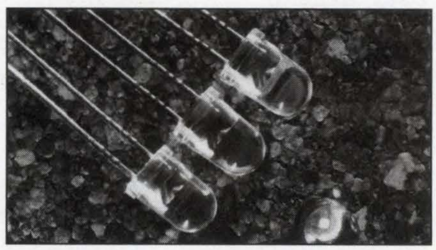
Surface-mount LED emits a true "medical red." The microLED 597 set of surface-mount LEDs and detector includes a 658-nm red emitter (28 mcd at 20 mA), a 940-nm infrared emitter (0.8 mW at 20 mA), and a PIN-diode detector (950 nm pk). The "medical-red" emitter provides a tightly controlled wavelength without the secondary-emission peak common to ordinary LEDs. The set measures an object's or a substance's absorption of red light for applications such as glucometry, pulse oximetry, and fetal monitoring. The packages measure 1.2×1.27×3.2 mm. $3.90 for a set of all three (1000); delivery is four to eight weeks ARO. **Dialight Corp**, Manasquan, NJ. (908) 223-9400. **Circle No. 376**

Transducers answer phone calls about status and measurements. The PhoneDucer P-9000 industrial transducers measure pressure at remote locations and report the monitored variable when polled over a phone line. The units cover the pressure range from 0 to 9000 psi. The factory calibrates and temperature-compensates each unit. The unit comes in stainless-steel enclosures measuring 3×1.5 in. and weigh <1 lb. The unit requires no power supply or batteries; it gets its power via its RJ-11 connector. Other measurement variables are optional. $495 (singles). **Elwood Corp**, Oak Creek, WI. (414) 764-7500. **Circle No. 377**



Ceramic resonators pack built-in capacitors. The ZTS series of ceramic resonators incorporates a pair of 30-pF capacitors (100-pF optional) to form a logic-compatible tank circuit in one package. Resonant frequency ranges from 2 to 12 MHz. The devices' frequency variation is ±0.3% at ambient temperature (mostly because of ±0.3%/year aging), and operating temperature is –20 to +80°C. Although ceramic resonators' frequency accuracy cannot match that of quartz crystals, ceramic resonators are less expensive, consume less than 1 mW, and operate properly from voltages below 5V. Being low-Q devices, they quickly start oscillating, minimizing spurious activity from newly energized μPs struggling to come up to speed. **Integrity Technology Corp**, Santa Clara, CA. (408) 262-8640. **Circle No. 378**

Relay driver eliminates interface components. The avalanche-rated ZVN4206AV N-channel MOSFET comes in a TO-02 package and is rated for a 60V drain-to-source voltage at 600 mA max. The device has an on-resistance of 1Ω and accepts a 5V gate drive. The device requires no free-wheel diode when controlling inductive components. The avalanche breakdown of the device's intrinsic MOSFET body diode dissipates the inductive component's stored energy. $0.32 (1000); delivery, 10 to 12 weeks. Samples are available. **Zetex Inc**, Commack, NY. (516) 543-7100. **Circle No. 379**



Red and green LEDs are sunlight-visible. The red SLA-570 LED provides a luminous intensity of 2400 mcd at 10 mA, and the green version emits 750 mcd, both exhibiting a 24° viewing angle. The units have 100,000-hour MTBF. Green LED, $0.07; red LED, $0.125 (10,000). **Rohm Corp**, Antioch, TN. (615) 641-2020, ext 121. **Circle No. 380**

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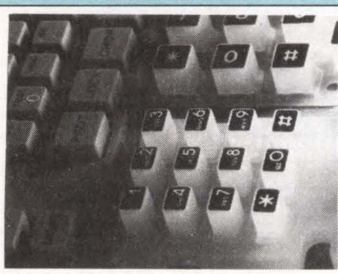

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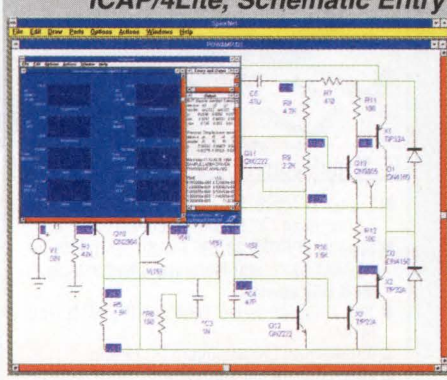

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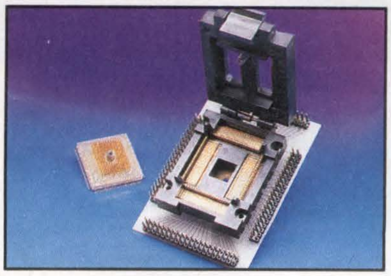

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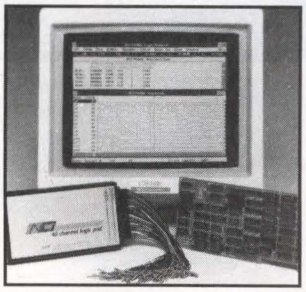

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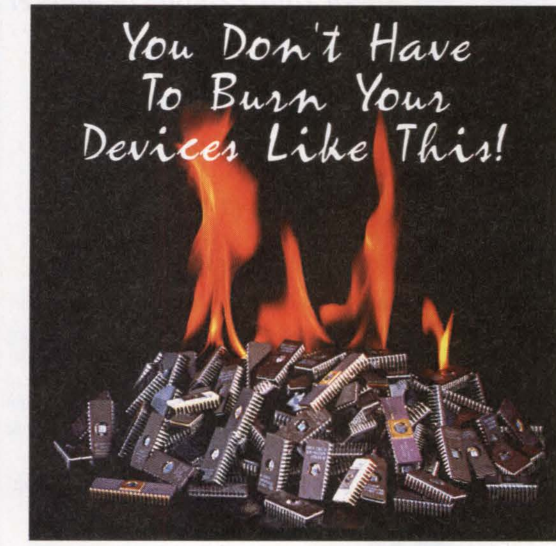

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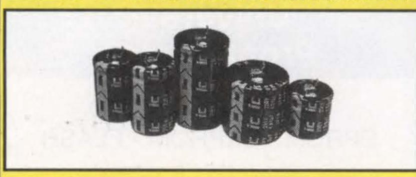

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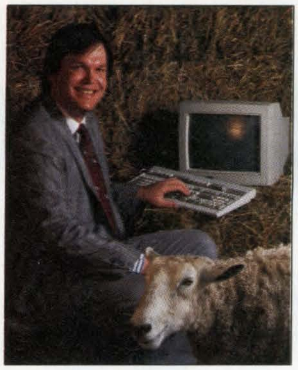
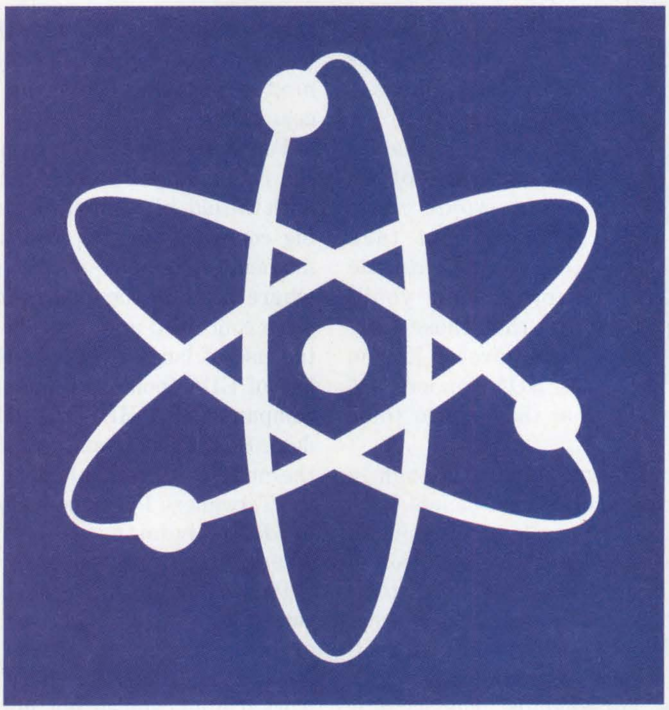


JOHN COOLEY, EDA CONSUMER ADVOCATE & ESNUG FOUNDER

The shape of things to come?

I couldn't help but think about overly idealistic college activists while listening to Andy Graham, president of the CAD Framework Initiative (CFI), wrap up CFI's first conference on EDA integration and interoperability (EII) with a call for users to pressure EDA vendors to make their products more interoperable with their competitor's. I felt as if I were witnessing some sort of modern-



day scene from *Don Quixote*, where a well-intentioned management-type was expecting normally overworked engineers to suddenly drop what they're doing, spontaneously unite, and assault the buildings where evil, scheming EDA vendors work—all in an attempt to force them to become CFI compliant.

Doesn't Andy know that it's not human nature for people to get worked up over something they already have a solution for? Sure, most EDA tools from different vendors choke a little when you try to get them to work together, but there's always a way to find a workaround. Trying to invoke major political changes with EDA vendors is a slow, messy, and uncertain process—and it doesn't solve that "not all EDIFs are alike" problem for me right now, when I need the solution.

Then my mind wandered into all the political realities involved with having fully interoperable EDA tools. EDA vendors would love it because it offers them one standard framework to design their competitive, hot, and innovative tools that would steal business from the big EDA vendors. Realizing this, big EDA vendors are infamous for providing all sorts of lip service to promoting interoperability and things like CFI standards—but allocate next to nothing in funding to make it happen. Customers would love it because there would be no pesky interoperability issues to occasionally hack through.

Of course, as any salesman will tell you, customers can be very fickle: They aren't willing to pay an extra cent for interoperability, but if it's free they'll take it. When I asked all five CAD managers on the EII panel the question, "Given a choice of either a screamingly new EDA tool that helped you do new functionality or complete interoperability of your current tools, which would you choose?", all five EDA customers unequivocally chose getting the new EDA tool over interoperability.

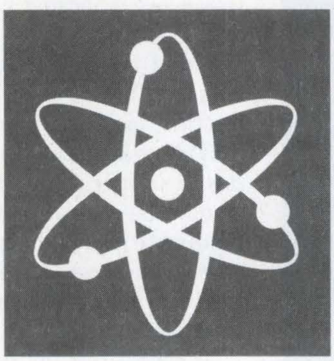
Zero tolerance

Also, unlike how they feel about tools offering sexy new EDA functionality, customers have zero tolerance for *any* bugs in a framework. The big EDA vendors who sunk a little money into making their own proprietary frameworks (ie, Mentor with the Falcon Integrator and Cadence with Cadence Frameworks) got burned big time by "displeased" customers who ran into major and minor framework bugs. Most of the customers stopped using the framework and

EDA CONSUMER ADVOCATE

bombarded suppliers with nasty phone calls, which is another valid reason the big EDA vendors give frameworks tons of lip service but not much more.

The final effect an industry-wide interoperability solution would have would be that soup-to-nuts "total-solution" EDA vendors (like Mentor) would be threatened, because EDA tools would become commodity items. (Customer loyalty lasts all of 30 seconds in the EDA business.) EDA vendors would be forced to offer quality tools at dirt-cheap prices because the competition would be cutthroat! On paper, this sounds like a great idea for EDA customers—and a living hell for EDA vendors. *Maybe the engineers of the world should unite for CFI!* But take this scenario a little further and you'll find that those software pirates known as EDA vendors are not necessarily as evil as they appear to be on this issue.



The future's a funny thing. Although in the short run customers would benefit from commodity-priced EDA tools, who's going to pay for the blockbuster next generation of EDA tools? Sure, a lot of great EDA tools start from two guys in a garage, but what bootstraps real development is the high profit margin these new companies get with their hot tools. For example, Chronologic Simulations couldn't have made a screaming Verilog simulator if they could only get $3000 per copy early on. The same is true for the ambitious projects the big EDA vendors take on: Synopsys couldn't have made a behavioral synthesizer without the financing from sales of its RTL level synthesizer, and Racal-Redac had to sell its behavioral-synthesizer research—along with most of its remaining EDA product line—because it wasn't making money in the EDA business.

No matter how good EDA tools get, there's a limited market for this type of software, and somehow the R&D money for next-generation tools has to come from customers.

For those who doubt my reasoning, look at the commodity PC-clone market compared with the old, big computer makers. Sure, the big computer makers were big, piggy, and financially greedy, but these were the places where a lot of hardware design concepts were conceived and developed. Scan, JTAG, the use of large ASICs, early FPGAs, and lots of EDA tools were financed by sales to companies like HP, DEC, IBM, Sun, Tandem, SGI, Intergraph, etc. Compared with the number of technological breakthroughs the Taiwanese PC-clone makers made in the hardware industry as a whole, you'll see where I'm coming from.

Please don't misunderstand: I'm not advocating ignoring the need for better interoperability among tools from different vendors, but as long as there's some viable workaround, you're not going to hear me complaining (much).

CFI'S ANDY GRAHAM'S LIST OF THINGS TO DO...

- ✔ Support the creation of certification boards for de facto standards like EDIF, Verilog, VHDL, etc
- ✔ Habitually and publicly report specific tools that are and aren't up to the certified standards
- ✔ Encourage a single frameworks standard for the small EDA vendors to agree on to save on development costs
- ✔ Separate CFI's EII conference from VIUF. Interoperability isn't a Verilog or VHDL issue—it's a universal problem, and as such should not have the appearance of partisanship in the Verilog/VHDL wars.

John Cooley, an EDA consumer advocate and founder of the outlaw E-mail Synopsys Users Group (ESNUG), lives on the Holliston Poor Farm in Massachusetts. He raises sheep and is an EDA- and ASIC-design instructor and project-in-crisis consultant. He can be reached at "jcooley@world.std.com" or at (508) 429-4357.

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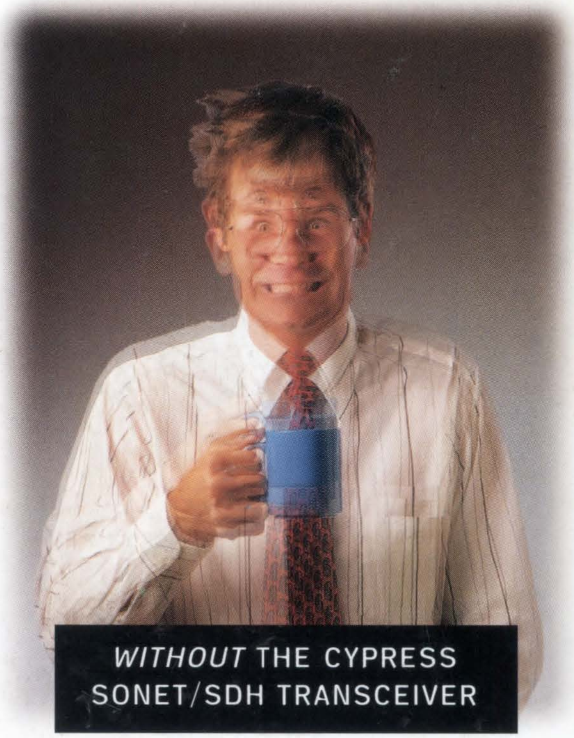

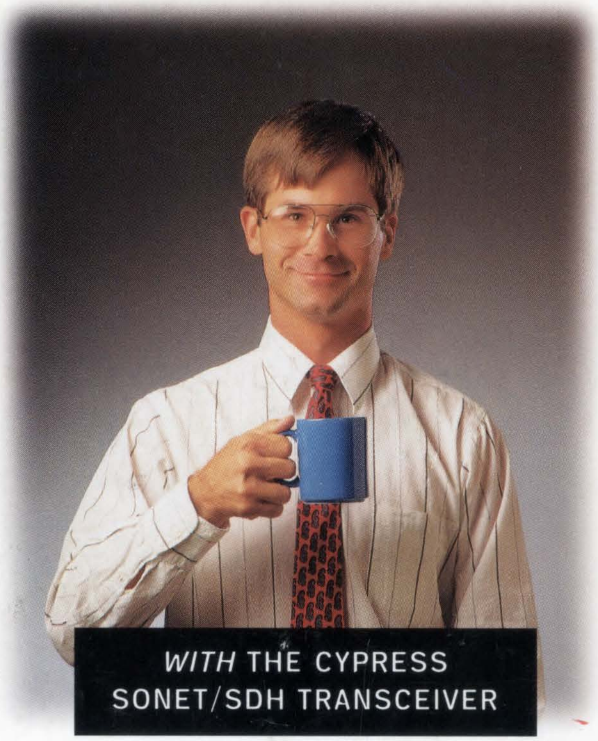

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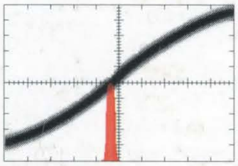

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