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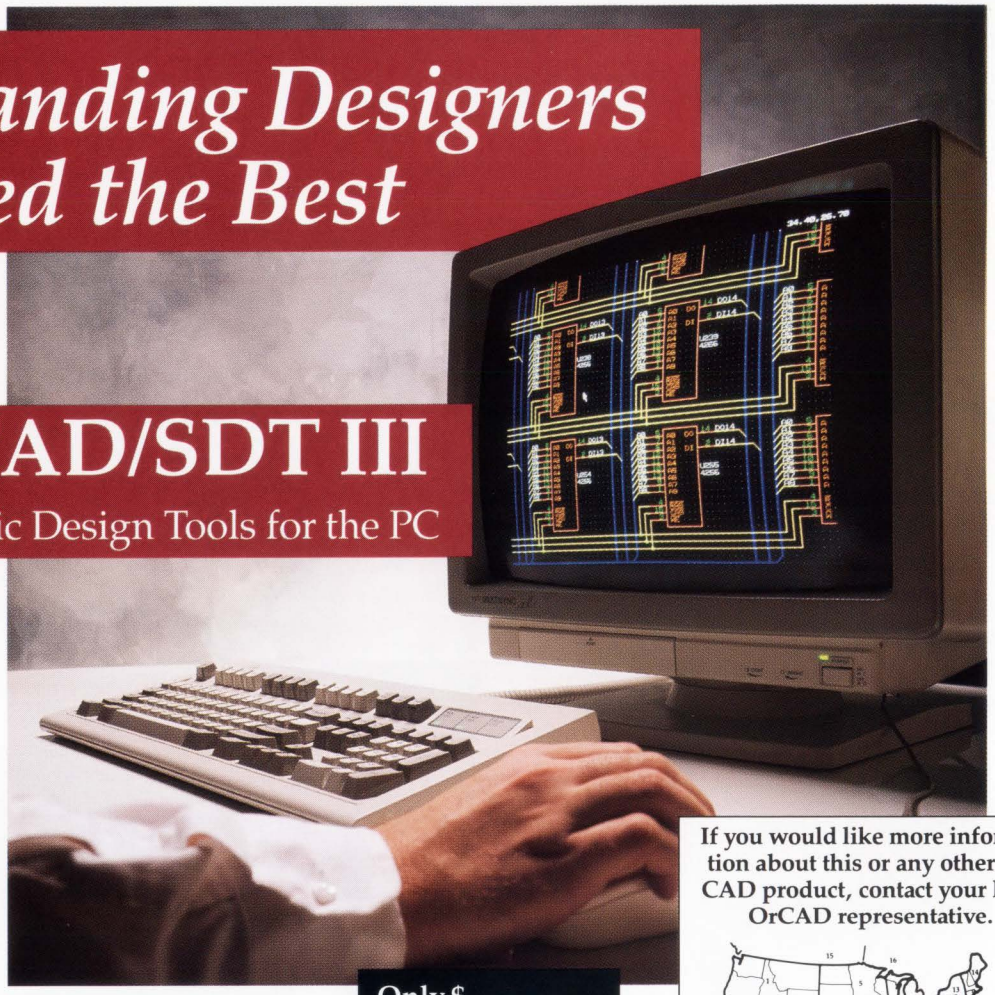

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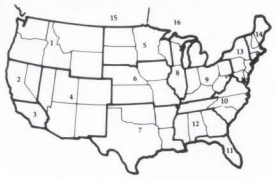

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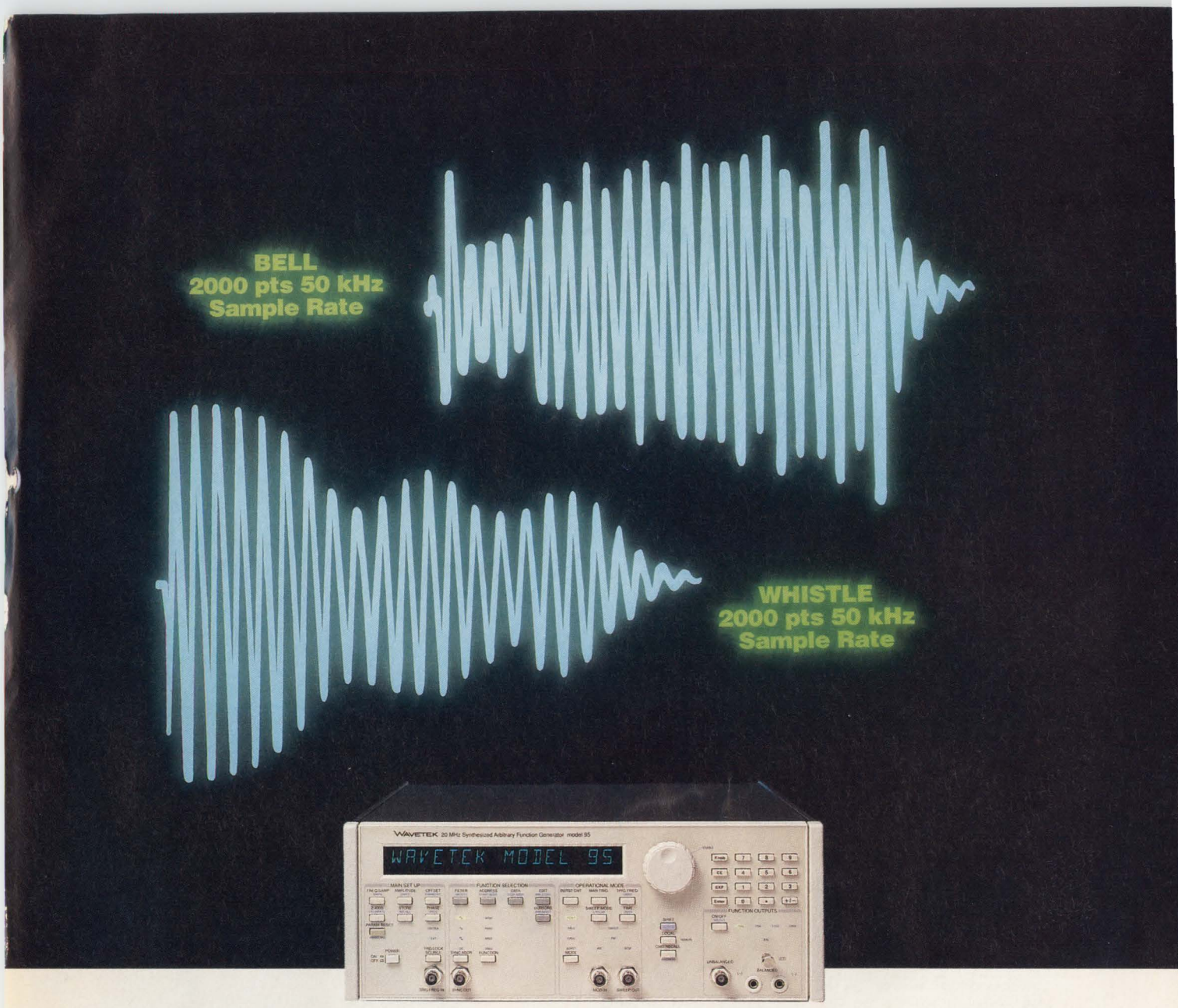

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For information about all the other bells and whistles you'll find on the Model 95, call Wavetek San Diego, Toll Free at **1-800-874-4835** today.

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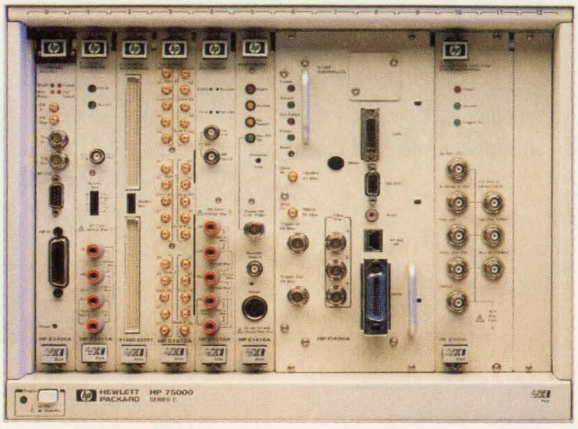

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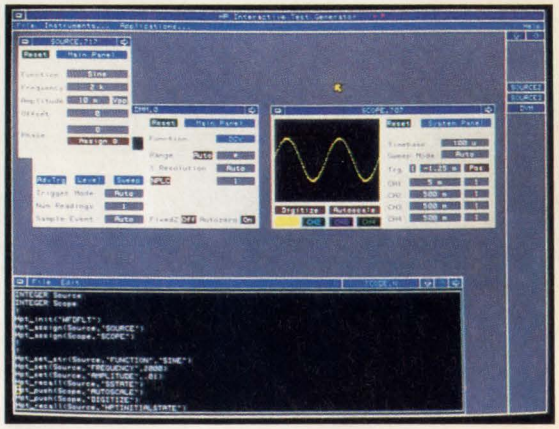
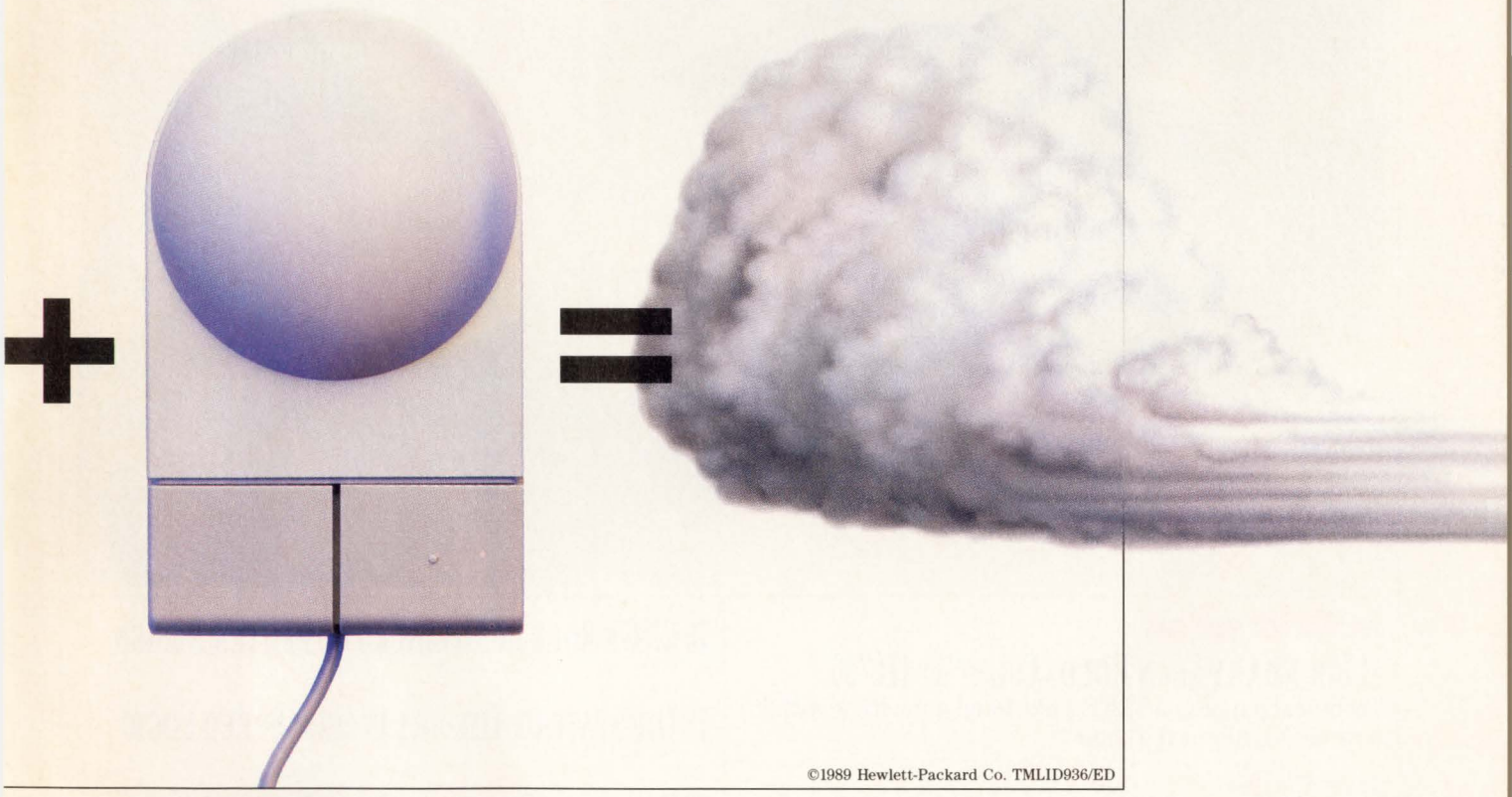


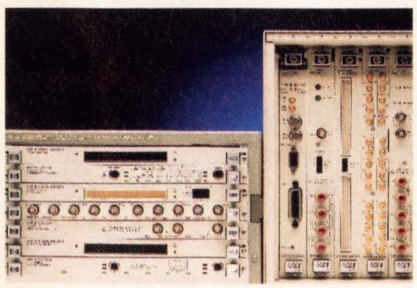
It's simple. By combining advanced VXI hardware, a powerful system language, and a common human interface, HP really puts your test development in motion.

Start with the hardware. HP 75000* Series B and C mainframes and modules give you a broad selection of price and performance options. So you can tune a system to your needs in minimal time.

Then, the open Test & Measurement System Language (TMSL) lets you speed through test development as never before. It's a standardized instrument language that insures compatibility with all HP 75000 modules, as well as other common system instruments. And it gives you a migration path for the future.

When you add the mouse-driven HP Interactive Test Generator software (HP ITG) to the equation, you really take off. Virtual front panels





save time. Select a function by clicking the mouse and HP ITG sends the right command to the right module automatically. With pop-up windows and pull-down menus, the interface is simple and speedy.

So don't waste time. Call **1-800-752-0900** today. Ask for Ext. **246J** to get a catalog on the HP 75000 family of VXI products. And see how HP's VXI will help you kick up a little dust in test development.

*The HP 75000 VXI is part of HP's Measurement System Architecture.

There is a better way.

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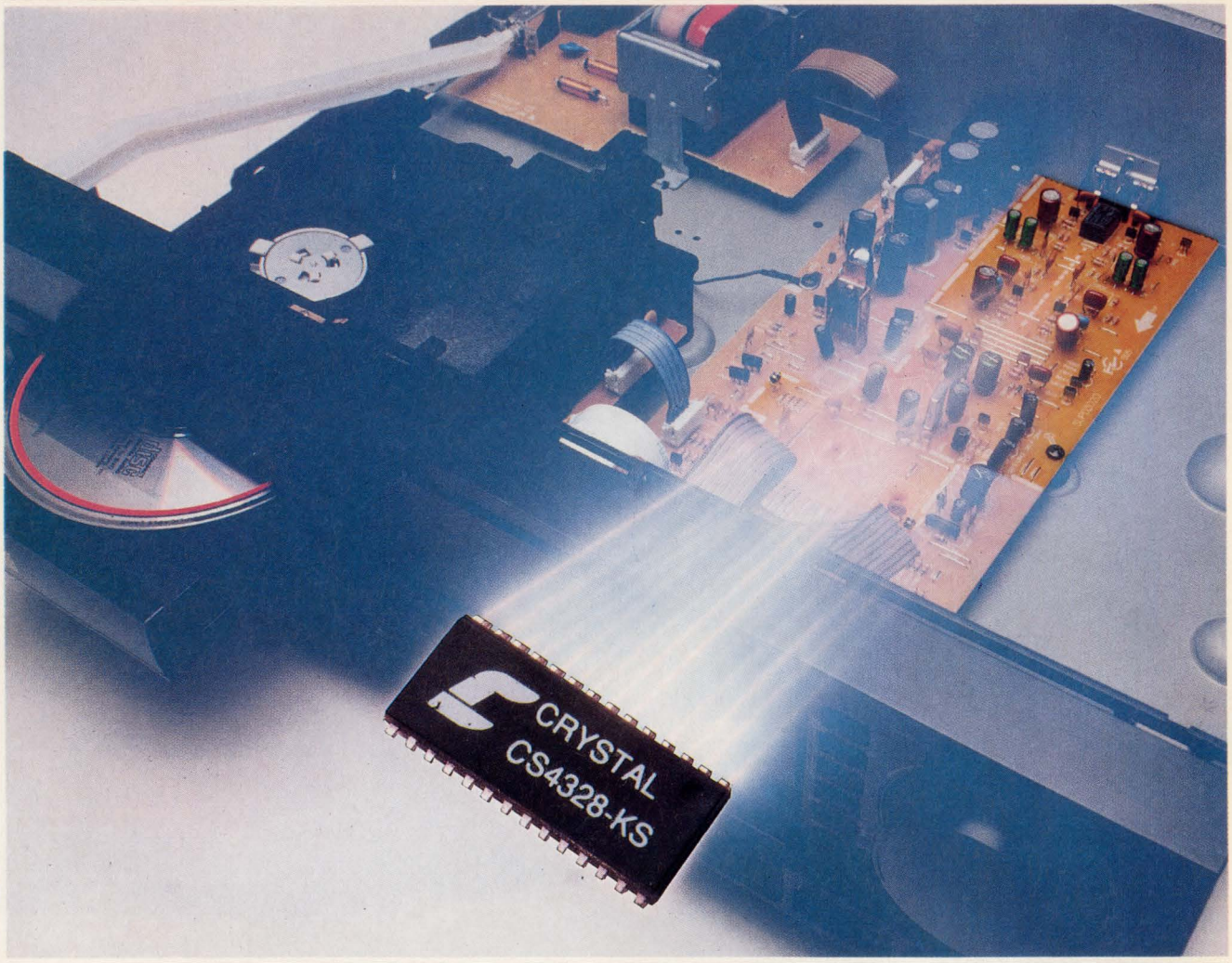

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- How important are analog design skills for engineers in the future?
- How do the design skills of today's EE graduates stack up against those of young engineers of the past?

Send us your opinions on these questions on our Reader Opinions fax: (201) 393-0637. Or, mail your responses to ELECTRONIC DESIGN, Reader Opinions, 611 Route 46 West, Hasbrouck Heights, NJ 07604.

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- Offload a servo system's CPU with a PLD-based coprocessor
- Improve system performance with an enhanced SCSI processor
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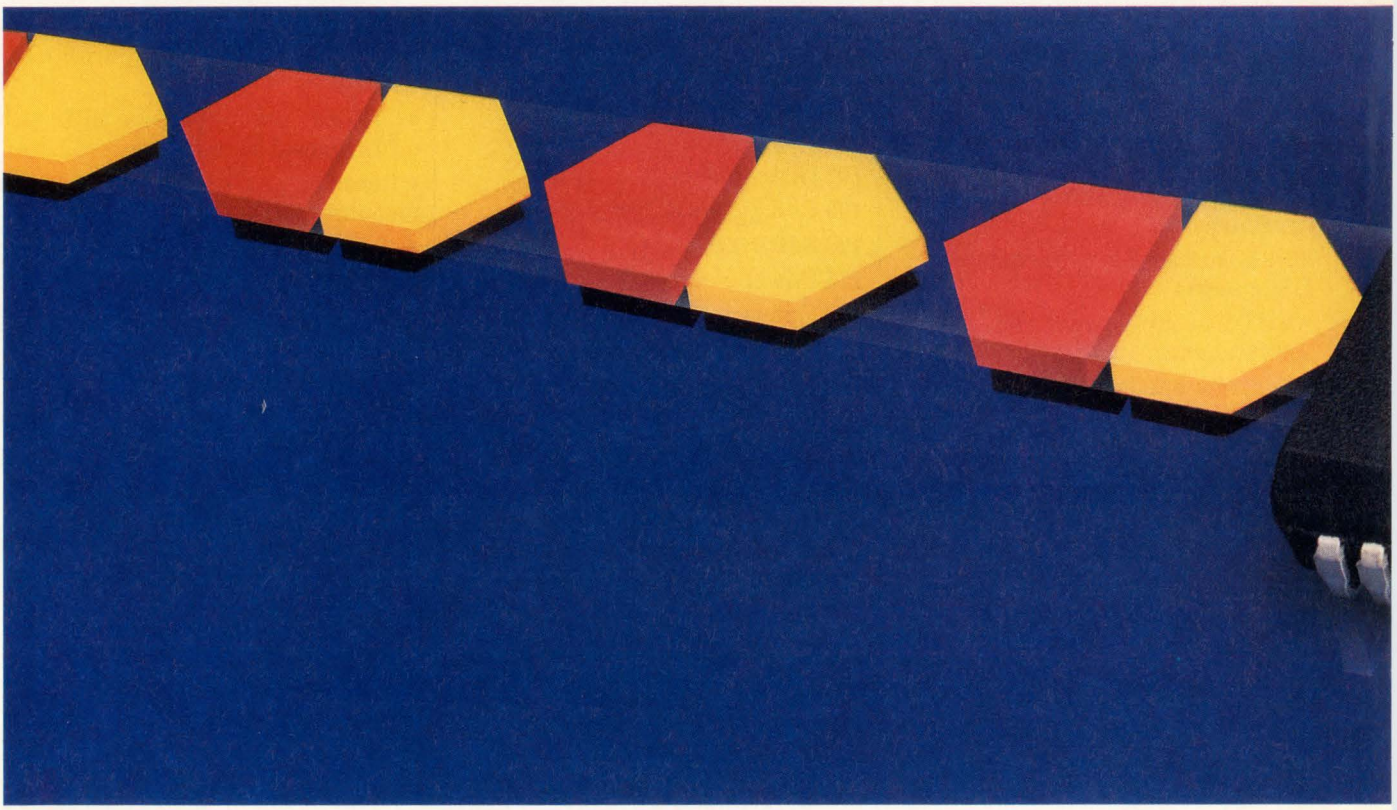

Sound Strategy.

Siemens announces a single-chip echo cancellation U-interface device for ISDNetworks of all sizes. From switching to transmission, a clearly superior solution. Berlin to Iselin.

Siemens has won another sound victory in communications technology by developing the industry's first single-chip solution in CMOS for echo cancellation circuit functions in ISDN. It's a clear example of the innovative thinking which has made Siemens a leader in ISDN technology.

From its single-chip design to its ease of integration, the Siemens PEB 2091 ISDN Echo Cancellation Circuit (IEC-Q) represents a milestone in ISDN realization. This device can double the traffic-handling capability in existing telephone lines, and is ideal for appli-

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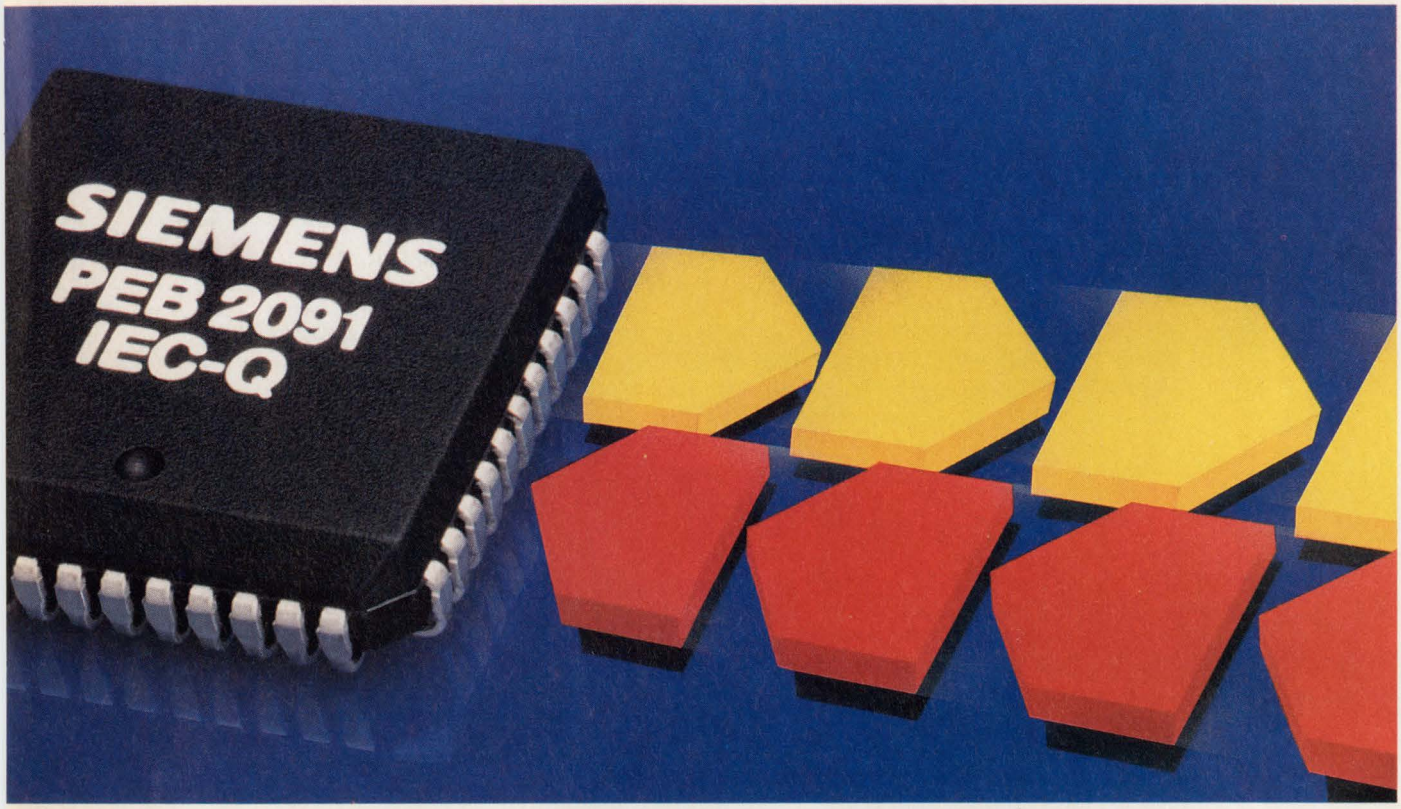
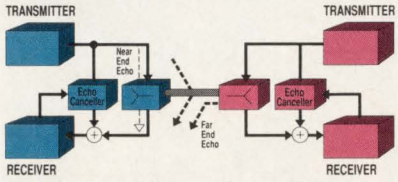


cations in transmission systems such as digital added main line, pair gain systems and intelligent channel banks.

Through its single-chip design and CMOS technology, the advanced PEB 2091 reduces space requirements and software overhead, and has lower power consumption requirements than any other design. And it supports ISDN Oriented Modular (IOM) architecture, the de facto standard for ISDN, which makes installation simple, and enables it to work in tandem with the most advanced ICs available.

Building upon the most comprehensive line of ISDN ICs in the industry, the PEB 2091 sends a clear signal that Siemens is continuing to take great strides in telecommunications. Siemens was the first company to design a two-chip U-interface transceiver for the 4B3T block code used in Europe, and developed the first single-chip device for the 2B1Q code established in North America. And the PEB 2091 meets the requirements of the American National Standard for Telecommunication.



Siemens uses CMOS technology to provide a superior echo cancellation solution with the lowest power consumption requirements.

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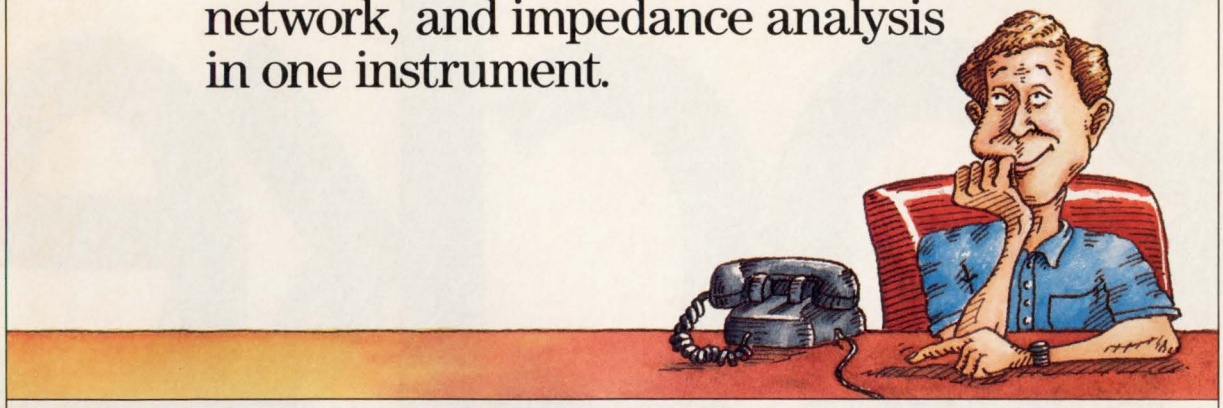
Picture yourself with 500 MHz spectrum, network, and impedance analysis in one instrument.



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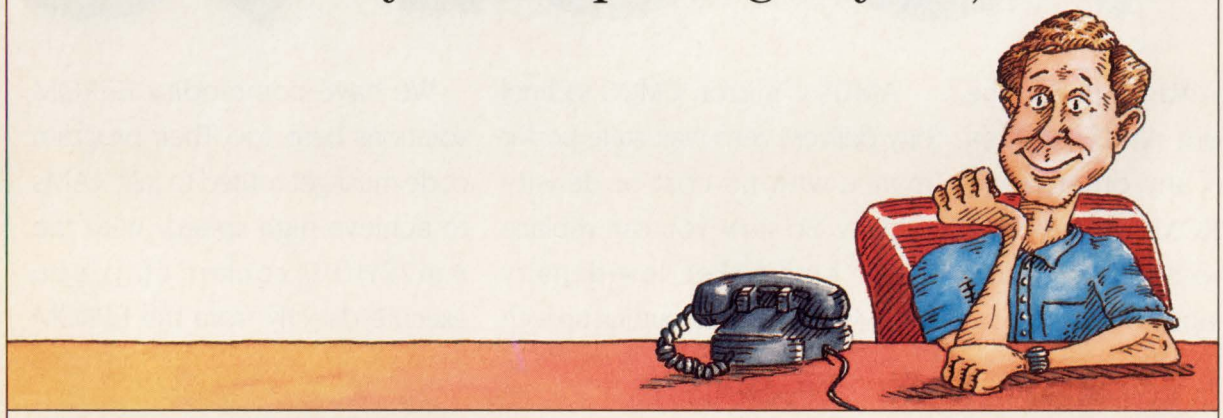

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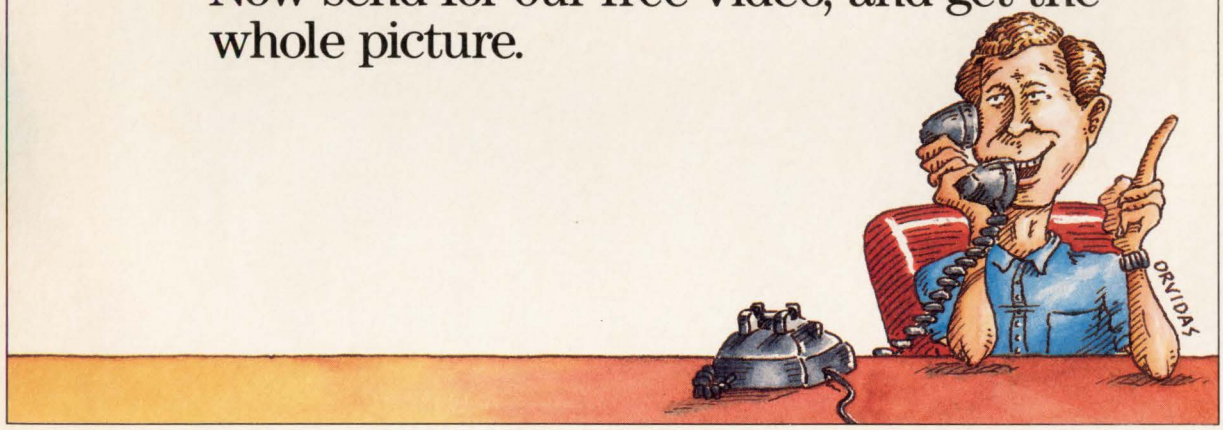

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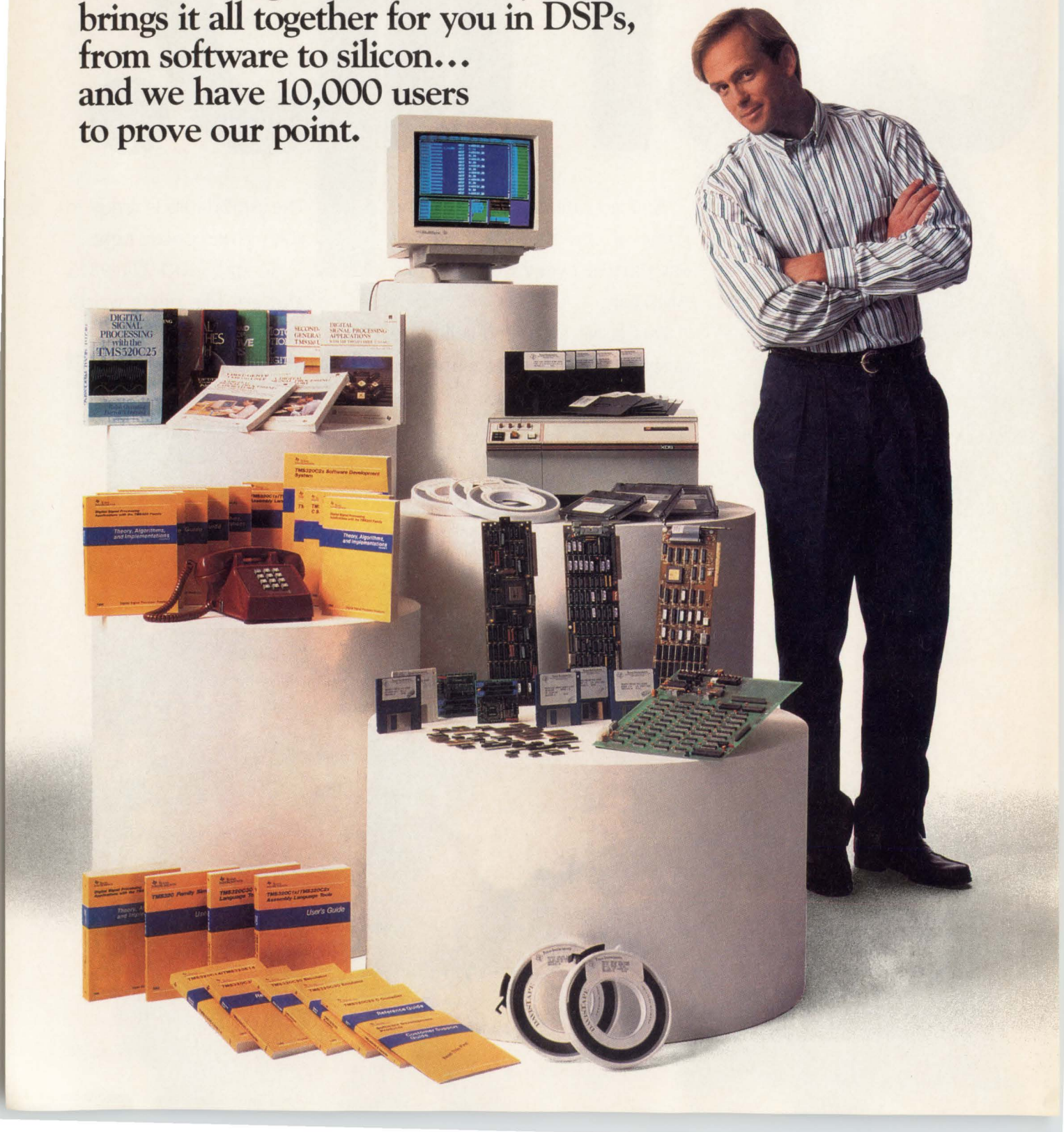

OR JUST ALMOST?

Designers are applying TI's single-chip TMS320 DSPs (digital signal processors) in more systems around the world than any other. In fact, leading manufacturers in most market segments — including telecommunications, computers and computer peripherals, automotive, industrial controls, consumer products, and military systems — use TMS320 DSPs.

These designers choose our DSPs because they know there is a big difference between all there and almost. With TI, they know they are getting the most complete DSP solution in the business — (1) performance, (2) support, and (3) broad choice. These important factors are worth careful consideration as you evaluate DSPs:

☐ Yes
☐ No **1. Am I assured of access to the top-performance devices in the field?**

Naturally, performance is a high priority for any DSP-based system. The TMS320 family consistently sets the performance standards for the industry. Among the newest additions are the highest performance fixed- and floating-point single-chip DSPs, both with clearly defined road maps for future performance upgrades. Multiprocessing DSPs offer even higher performance.

☐ Yes
☐ No **2. Is world-class support in place to help speed my design to market?**

Few if any DSP vendors equal the level of support that TI offers.

Industry-standard high-level language optimizing compilers (ANSI C and Ada), HLL debuggers, the SPOX™ multitasking DSP operating system, and scan-based emulators provide you with a development environment similar to that traditionally enjoyed in general-purpose microprocessor design.

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Such leading-edge tools are only the beginning of our comprehensive support. Other TMS320 support includes:

- A hot line staffed with DSP personnel ready to answer your technical questions
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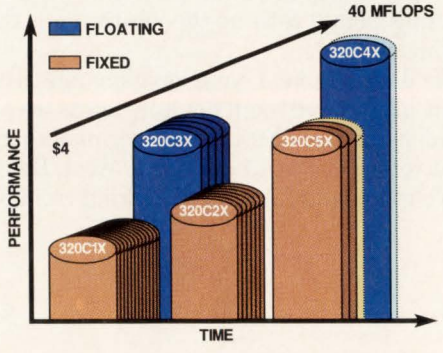
- More than 2,000 pages of application notes and DSP code
- More than 100 third parties and consultants
- Hands-on workshops
- University program with more than 100 universities participating

WHAT'S AHEAD FOR TI's TMS320 FAMILY



☐ Yes
☐ No **3. Is the choice of devices broad enough that I can closely match a DSP to my price/performance needs?**

Our TMS320 family spans five generations — more than 20 members offering a price/performance range from $4.00 to 40 MFLOPS. Your choice includes:

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Or complete and mail the return card and we'll send you our three-volume TMS320 DSP Applications Library. If you prefer, we'll send you our TMS320 product overview and support brochure. We feel sure you will soon be one of the thousands around the world achieving design success with the leadership TMS320 family.

08-0081

TEXAS INSTRUMENTS

GRADE TODAY'S ENGINEERING EDUCATION

A recent study of Electronic Design's readers (reported in the June 14 issue, page 109) showed that the average reader is about 39 years old. Thus, most of our readers have been out of engineering school for 15 years or more, and probably have at least 20 years to go in this industry. Readers, therefore, have much at stake in the quality of today's engineering education. If many readers within the next 20 years take on added managerial responsibilities—as could be expected because of increased experience—much of their future success depends on the quality of the engineers on their staffs. That quality, in turn, partially depends on the effectiveness of today's engineering education.

In our QuickLook section (page 23), we've published reader opinions on various questions of importance to the industry and to engineers. One question that we'd like to investigate in the future concerns the quality of today's engineering education: What do you think about the education that young engineers are getting these days? What areas are being overlooked, or, for that matter, over-stressed? How strong a role should humanities courses play in engineering education? I must question the wisdom of many humanities courses for engineers when there's so much new technology to be learned—what courses are they forfeiting to fit these non-engineering subjects into the curriculum? Moreover, with the explosion of advances in all phases of electronics technology, are the traditional four years enough to give young engineers the foundation they need to perform effectively—should five years become the norm? On the other hand, is education only the starting point, with on-the-job training the only effective way to develop engineers?

We'd like to hear your opinions on these questions. We will publish as many as we have room for, as often as we can. Fax your opinions to us on our Reader Fax line, 201-393-0637, or mail them to our Reader Opinions Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604.

We're looking forward to hearing from you.

Stephen E. Scrupski
Editor-in-Chief

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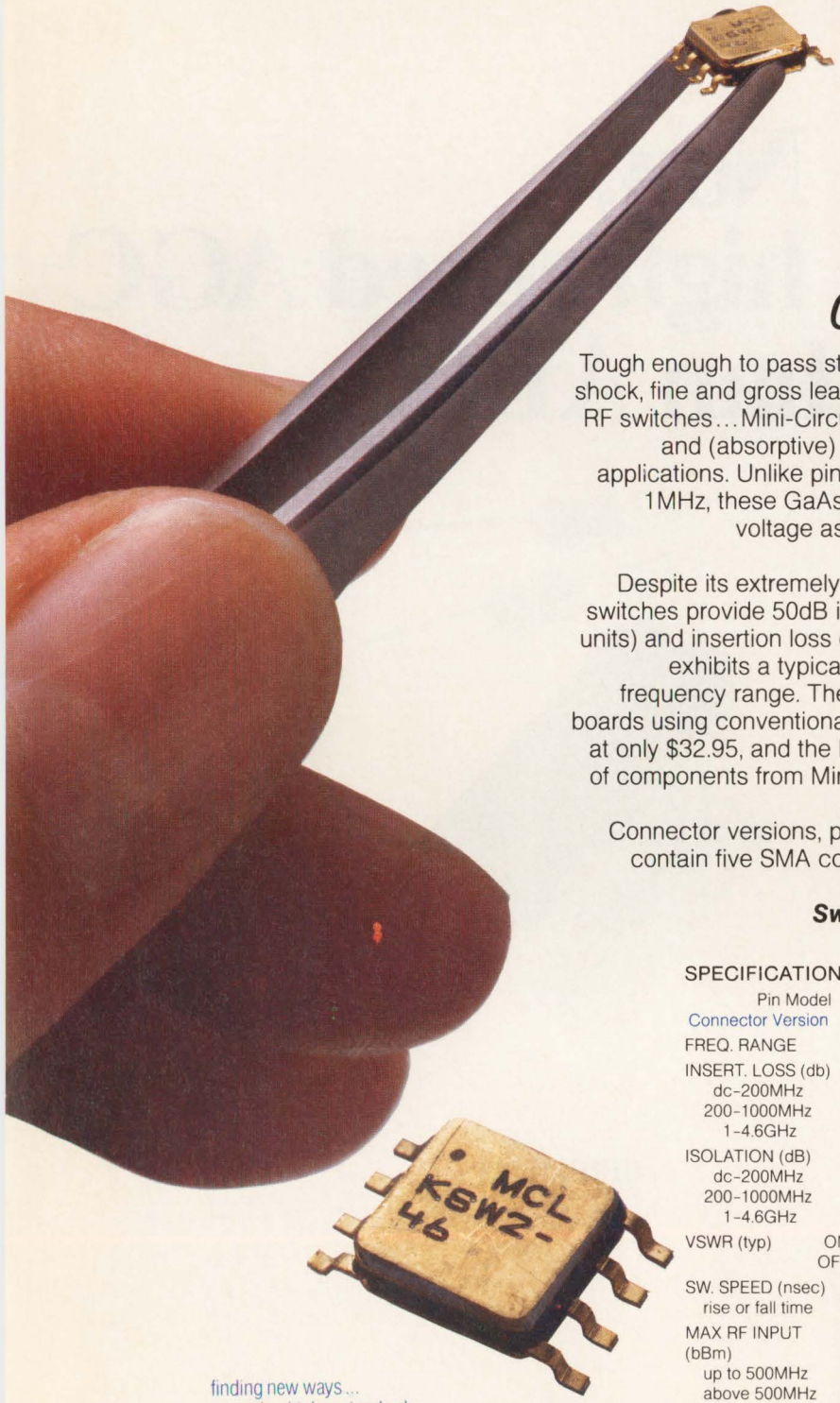

dc to 4.6GHz from $32.95 (10-24)

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Connector versions, packaged in a 1.25 x 1.25 x 0.75 in. metal case, contain five SMA connectors, including one at each control port to maintain 3ns switching speed.

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SPECIFICATIONS

Pin Model / Connector Version	KSW-2-46 / ZFSW-2-46		KSWA-2-46 / ZFSWA-2-46	
FREQ. RANGE	dc-4.6 GHz		dc-4.6 GHz	
INSERT. LOSS (db)	typ	max	typ	max
dc-200MHz	0.9	1.1	0.8	1.1
200-1000MHz	1.0	1.3	0.9	1.3
1-4.6GHz	1.3	1.7	1.5	2.6
ISOLATION (dB)	typ	min	typ	min
dc-200MHz	60	50	60	50
200-1000MHz	45	40	50	40
1-4.6GHz	30	23	30	25
VSWR (typ) ON	1.3:1		1.3	
OFF	—		1.4	
SW. SPEED (nsec) rise or fall time	2(typ)		3(typ)	
MAX RF INPUT (bBm)				
up to 500MHz	+17		+17	
above 500MHz	+27		+27	
CONTROL VOLT.	-8V on, OV off		-8V on, OV off	
OPER/STOR TEMP.	-55° to +125°C		-55° to +125°C	
PRICE (10-24)	**$32.95**		**$48.95**	
	$69.95		**$79.95**	

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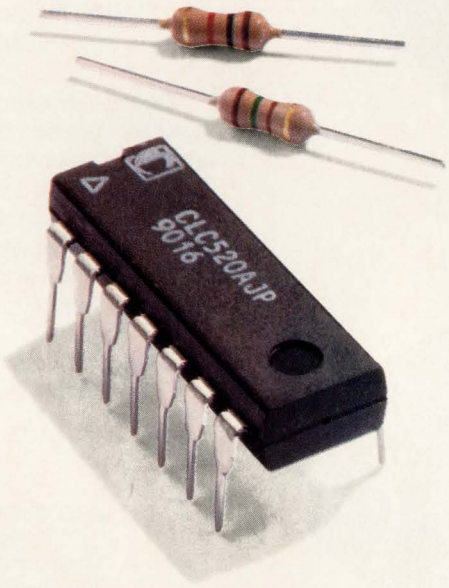

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NEW WAYS TO LOOK AT IC TESTING

Adapting to change is crucial to the survival of any species. Fortunately for the animal kingdom, that evolution can occur over many generations. In the electronics industry, where change is constant, people must react more quickly. Herein lies the significance of the theme of this year's International Test Conference: "The changing philosophy of test." One important movement in test and measurement is the recently approved boundary-scan standard *(see "Boundary scan holds court at ITC '90," p. 41).* Another more subtle transition is being driven by the proliferation of ASIC designs.

JOHN NOVELLINO
TEST & MEASUREMENT

Most of today's IC designs are ASICs produced in relatively small batches numbering in the thousands, compared to the previously dominant standard parts with runs in the millions. This shift raises questions about the test tasks of verification, characterization, and production test or incoming inspection. How do you reduce the cost of test? What role does the large ATE system now play versus the smaller, much less expensive, lower-throughput machines now available?

"What we are realizing more and more is that ASICs are generally low-volume devices, and you need testers that can do low-volume incoming inspection tests economically," says Steve Morris, director of marketing at Integrated Measurement Systems, Beaverton, Ore. IMS uses the term "test-station" in a computer analogy. "You don't use a mainframe computer to do a job that can be done on a workstation," says Morris. "In the same way, you don't use a large ATE system to do a job that a smaller, less expensive machine can do."

Over the last four years, the differences between smaller verification-type testers and larger ATE systems have been shrinking, says Morris. Some architectural differences exist, with ATE systems offering 100% resource-per-pin capability. But with enough shared resources, engineers can still do the job, and it won't be too long before smaller machines have true tester-per-pin architectures, according to Morris.

A different tack is taken by Graham Miller, president of LTX Corp., Westwood, Mass. Miller estimates that with many different devices to test, programming makes up 60% to 70% of the total cost to test. "So what's a tester manufacturer to do? First of all, he's got to provide particularly good debugging software," says Miller. "And he's got to provide good links to the CAD tools. Such features as automatic test-program generation and program conversion from someone else's tester to your own tester are also very important."

Miller eschews classic differentiations in favor of more subjective criteria. "There's no such thing as a big tester and a small tester definition," he says. "There's also no such thing as a million dollar tester and a less than million dollar tester. It's really what a tester does, or what a customer wants the tester to do."

Sophistication of the vector engine is the big difference between the two tester worlds, according to Ed White, marketing communications manager for Hewlett-Packard's semiconductor systems center. "The big testers have a lot more formatting capability. They have the ability to make changes on-the-fly," notes White. "People have come to depend on those features."

However, he said good tests can still be written with a more limited format set, although at a cost in increased programming expertise. And parts can be tested as thoroughly without on-the-fly changes. Throughput may suffer, but for small runs that may not be a problem. "There are real benefits to these features, but I think what users are questioning now is whether the difference in price is justified," says White.

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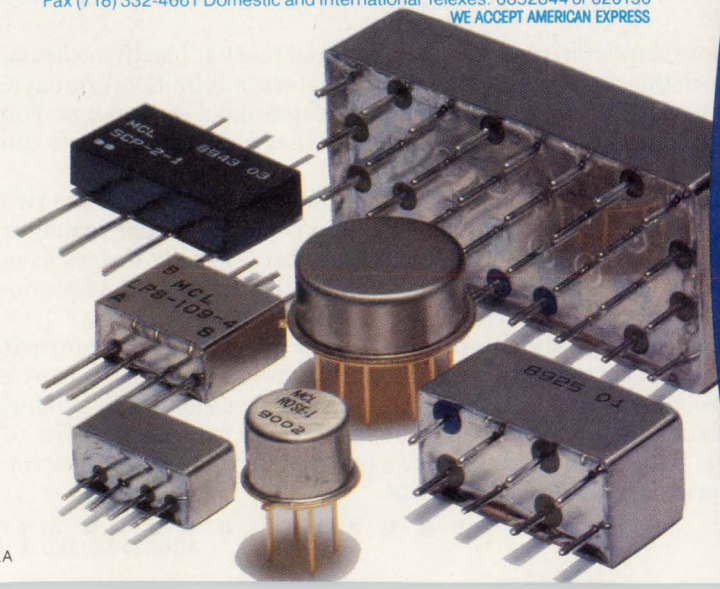

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CIRCLE 127

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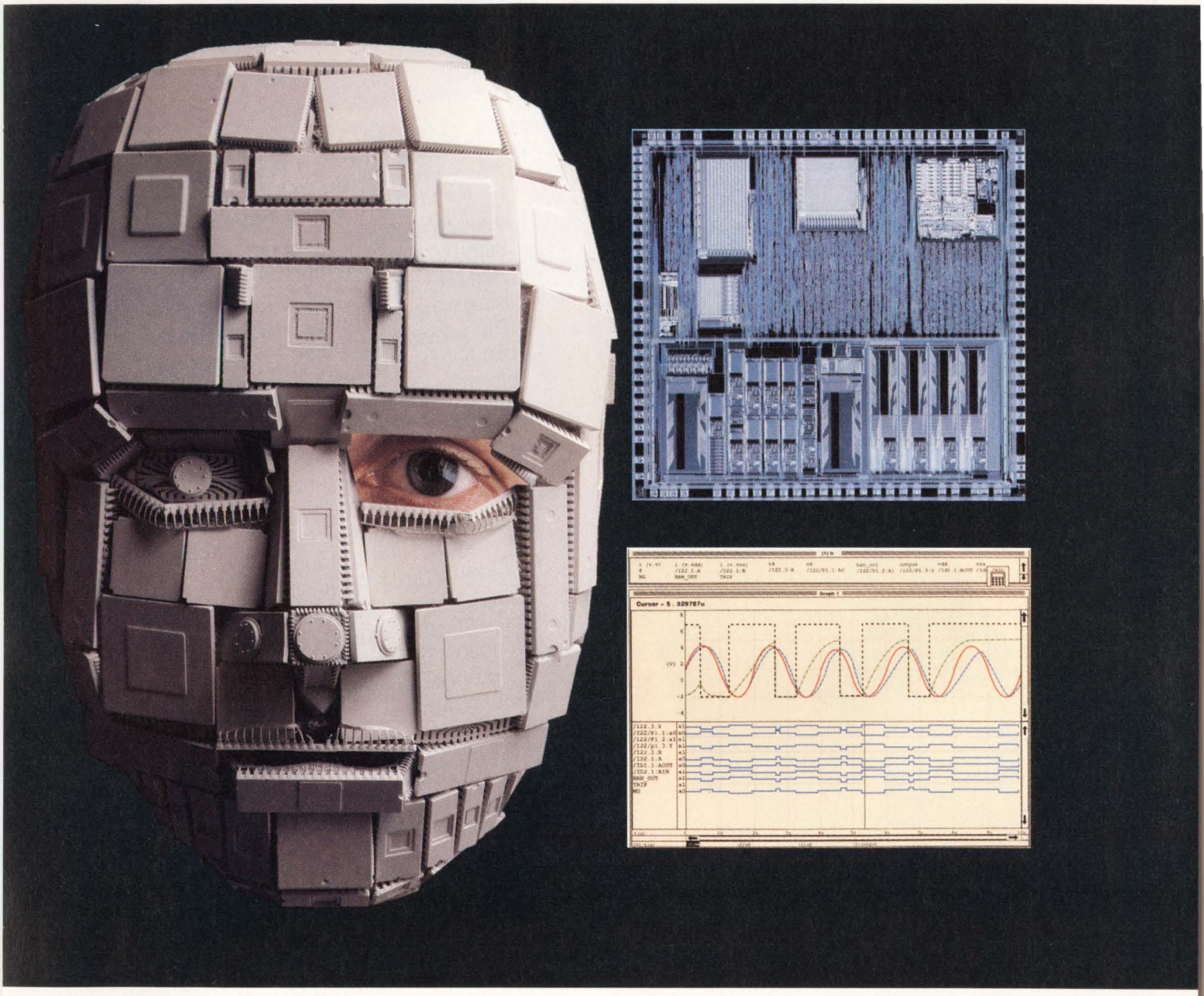

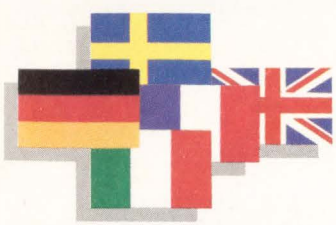

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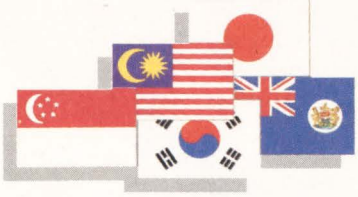

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CIRCLE 148

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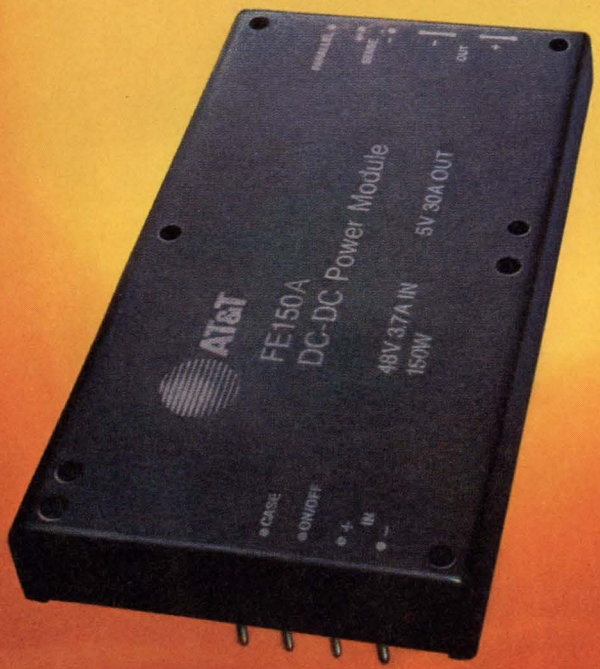

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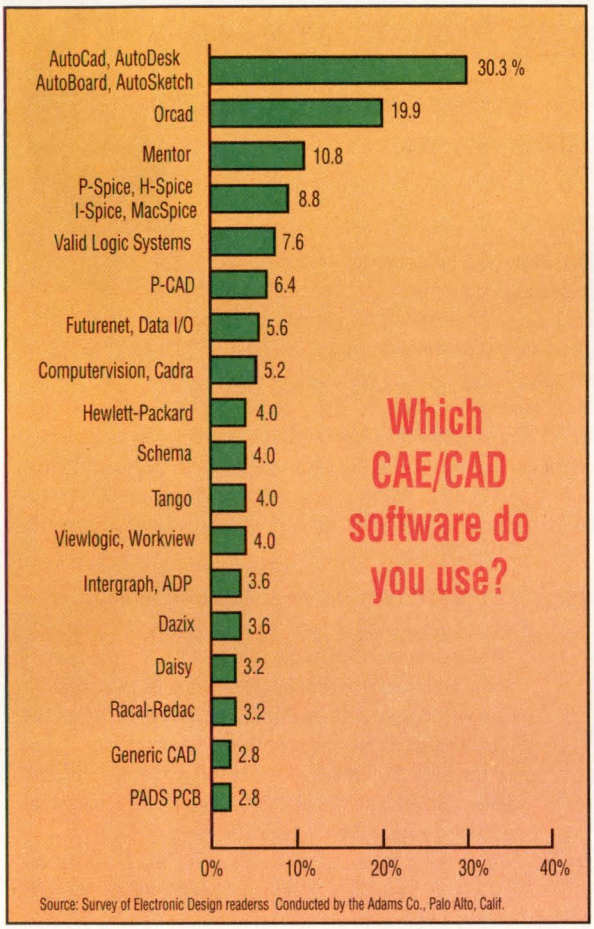
CIRCLE 157

ELECTRONIC DESIGN

QUICK LOOK

EDITED BY SHERRIE VAN TYLE

CAE SURVEY



Source: Survey of Electronic Design readerss Conducted by the Adams Co., Palo Alto, Calif.

Some of the acronyms and abbreviations making the rounds and what they stand for:

ACI	advanced chip interconnect
ATVG	automatic test-vector generation
CALS	the U.S. government's Computer-aided Acquisition and Logistics Initiative
CLEFT	cleavage of lateral epitaxial film for transfer (mechanically separating a film layer from a substrate)
DEPOT	deductive path-oriented trace (a new combinational ATVG algorithm)
JPEG	Joint Photographics Experts Group
PODEM	path-oriented decision maker
PHIGS	Programmers Hierarchical Interactive Graphics Standard
TDX	test design expert

1-MINUTE OPINIONS

Is there an engineering shortage?

There seem to be plenty of people who call themselves engineers. They are forced to *say* this because many of them can't *spell* it. **Mark A. Long**, *Bluffton, Ohio.*

No, but there is always room for another good one. **Herbert Heller**, *Pittsburgh, Pa.*

The fact that engineering salaries are depressed, raises are small, raise cycles are extended from 13 to 18 months, and lump sums are being given in lieu of raises at large corporations, are all indicators of an engineering manpower surplus, not a shortage. **L. Bruce Blau**, *East Windsor, N. J.*

Definitely not! It takes months to find a new job. If you are experienced, it's really bad. It took my husband 10 months to change jobs last year. At that, he only got a lateral raise (4%). I've been looking to change jobs a while and companies are asking me to take less money than I currently make. I also have two small children, and my requests to work part-time have been met with derision and negativity. If there were a shortage, I feel employers would want to keep me. But no way! I've been told to stay home with my babies. Professions with shortages accommodate working mothers with part-time and flex-time. Obviously, this is not the case.

I am not recommending engineering to young people, especially not girls. I recommend that they focus their energy and money on medicine and law. Neither my husband nor I are deadbeats. I have 11 years experience in software, plus an MS. He has eight years of experience as a design engineer, plus an MS. **Name withheld**

The response from the committee I head is no. The Manpower Committee has historically taken the position that, while there may be short-term localized shortages of engineers, on the whole, the U. S. has a sufficient supply of engineers.

The problem with many of the studies that proclaim shortages is that they are based on demographics and not on demand. They fail to consider changes in technology, utilization of manpower, and the use of engineering tools. The critical item in my opinion is the utilization of engineers. This will become an even bigger issue if the predicted defense cuts are made.

The Manpower Committee attempts to respond to published articles that predict engineering shortages by contacting the source of the article and requesting background information on the study. Too often the results of such studies are published verbatim with no attempts to obtain other opinions on the subject.

The committee is also sponsoring an engineering demand/supply study by one of the committee members. The results of this study should be available later this summer. **Paul Kostek**, *Redmond, Wash. Kostek is chairman of the IEEE/USA Manpower Committee.*

What's your opinion on the IEEE? . . . or how about the importance of analog design skills . . . or the quality of today's EE graduates. See the table of contents (p. 5) for a complete list of questions and fax your opinions to (201) 393-0637. Or mail your opinions to Quick Look, Electronic Design, 611 Route 46 W, Hasbrouck Heights, NJ 07604.

QUICKLOOK

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Mice are mobile; keyboards are quick. To get the best of both worlds, ProHance Technologies Inc. puts 40 programmable buttons on the PowerMouse 100. PowerCad driver software links PowerMouse to AutoCad, as well as to other applications. With PowerMouse, AutoCad users can access pop-up menus and execute commands without taking the cursor off the drawing they're working on or having to shuttle between mouse and keyboard. System requirements are an IBM PC, XT, PS/2, or compatible, DOS 2.0 or higher, RS-232 serial port, and 20K available RAM. The device lists for $249; more information is available by calling (408) 746-0950.

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- **WRITE TO** the commissioner of Patents and Trademarks, Washington, D. C. 20231 for *The Guide to the Public Patent Search Facilities*, which describes patent indexing and search procedures.

from *Protecting Engineering Ideas & Inventions* by Ramon D. Foltz and Thomas A. Penn. Cleveland: Penn Institute Inc., 1989.

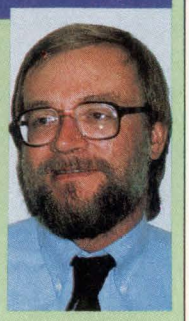
DID YOU KNOW?

. . . that only two engineering schools in the United States awarded more than 200 B. S. degrees to women last year. They were Purdue University, with 246, and University of Illinois, with 219. Only 23 U. S. schools had more than 100 of these graduates.
Engineering Manpower Bulletin, American Association of Engineering Societies

. . . that pressure for early retirement seems to be increasing for engineers. Of the nearly 9,000 engineers responding to a recent survey, 14% reported retiring before they had intended to, compared with 6% last year.
1990 IEEE Member Opinion Survey

KMET'S KORNER

...Perspectives on Time-to-Market



BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458

In the act of producing first-of-a-kind, me-too-with-a-twist, derivative, and next-generation products, I've run into a few snags. I've also kept my receptors tuned to the sights and sounds of other individuals who give their best shot at producing change. As the years go by, I've kept a list of the problems I've encountered. To my list, I've added those reported by my colleagues as they aired their new-product-development laundry. The reasons for the less than ideal performance of new product development teams resulted in a list of things to avoid, which I call KMET's Top 40. I use the top 40 to guide my thinking about methods, systems, and techniques to improve time to market; solutions to these problems logically result in shorter time to market. From the long list, I have picked a top 10, each of which I will discuss in future columns.

Changing product definition	Fritz Model captured the attention of the entire crew when he said those now famous words in Petaluma: "Make up your mind damn it!"
"Creeping" features	They cannot be stopped, but they must be controlled.
Technology changes	How can we possibly be thinking about RISC when the introduction of the 586 is only six months away?
Shortage of engineers	So the boss thought five engineers could get the job done in seven months and after two years of continuous twelve-hour days you're still not done!
Overly detailed planning	We've got a wall full of PERT and Gantt charts and nobody knows where the project is today or where it should be tomorrow.
Management-driven schedules	They made up for having too few engineers assigned by setting an absolutely ridiculous time-to-market goal
Organization instability	Why are people leaving? Where do they go? Is it better there?
Inexperienced staff	Over 50% of you are new to your present job assignment
Unforeseen tasks	We strive for perfection and always miss something along the way.
Testing exposes problems	Why won't the customer buy the simulation?

Note that all these problems delay projects. It occurred to me that gaining some control over these items would lead to better time-to-market performance, which led to the formation of Time To Market Associates.

In the future, I'll take the base product knowledge from earlier columns and add process knowledge to search for solutions to the problems just detailed. Along the way, we'll make overall time-to-market improvements in the new-product development process.

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CIRCLE 92

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CIRCLE 106

GROUP SEEKS PC-INSTRUMENT STANDARD

A group of computer-board manufacturers has formed a consortium to support a new standard for plug-in card instrumentation, data acquisition, and control systems for the PC bus. The de facto standard, called PCXI, was developed by Rapid Systems Inc., Seattle, Wash. The basic PCXI unit is a module designed to accommodate all PC cards built to the Industry Standard Architecture (ISA). The one-slot module is 1.2 in. wide, offering room for shielding on both sides of the card and a chassis shield between modules. The modules slide into a passive ISA backplane that's modified to improve power, ground, and termination for instrumentation, data acquisition, and control applications. PCXI is compatible with all current PC cards and is upwardly compatible with the 386/486 architecture. Besides Rapid Systems, consortium members include Analogic, Computer Boards, Data Translation, Guide Technology, National Instruments, Sciteq Electronics, and Strawberry Tree Computers. JN

VENDORS, USERS SHAPE FRAMEWORK DEVELOPMENT

A new program, called the PowerFrame Synergy Program, will bring together a group of EDA vendors and users to address the need for easy integration of applications and design management. The program, which is sponsored by Digital Equipment Corp., Marlboro, Mass., will determine how the company's PowerFrame framework software should develop. Moreover, it will operate in cooperation with such standards bodies as the CAD Framework Initiative. Participation in the program can occur at any of five levels: user, application supplier, value-added reseller/OEM, adviser, and joint developer. Fifteen companies have already enlisted in the program, including Racal-Redac, Westford, Mass., and Viewlogic Systems Inc., Marlboro, Mass. Of the fifteen members, only Cadence Design Systems Inc., San Jose, Calif., and Harris Corp. Scientific Calculations, Fishers, N.Y., will resell the PowerFrame software. LG

NEW PARTNERSHIP EYES CUSTOM DSP MARKET

Over two years of successful collaboration between Texas Instruments Inc., Dallas, Texas, and the DSP Group, San Jose, Calif., have culminated in a 10-year strategic agreement. The pact maintains that the DSP Group will develop and market custom chip sets based on TI's TMS320 family of digital-signal-processing (DSP) chips. Specializing in advanced DSP techniques for speech synthesis, voice compression and recognition, audio enhancement, and image manipulation, the DSP Group will create custom chip sets for consumer and telecommunications applications. TI will manufacture the products and provide technical support. Target applications for the DSP chips include compact-disk players, cellular telephones, telephone-answering machines, personal computers, and facsimile machines. ML

VHDL GROUP CLOSING IN ON 1992 STANDARD

The VHDL Analysis and Standardization Group (VASG), which is part of the Computer Society of the IEEE, is actively working toward establishing the 1992 IEEE standard. The IEEE requires that its standards be re-certified at least once every five years. Its first VHDL standard was issued in December, 1987, therefore the language must be re-balloted and re-certified by December, 1992. Although the U.S. dominated in the participation for the first standard, future discussions will involve Europe and Japan. A Steering Committee was formed to administer the standardization rules of the IEEE and to set up a worldwide electronic communication system for information transfer between VASG members. The standardization effort will consist of language requirement definition, followed by the design of the language. The first release of the requirements document is expected in the fourth quarter, with the language design work to follow soon after. Balloting is expected to start in the fourth quarter of 1991. For more information, call (202) 371-0101. LG

CONTROLLER ADDS SIXTH PROTOCOL

Tweaking the architecture of its 68302 integrated mulitprotocol processor, Motorola's Microprocessor Group, Austin, Texas, has added support for a sixth protocol. Introduced last year, the 68302 originally supported the HDLC/SDLC, Bisync, Async, DDCMP, and V.110 communications protocols. The chip's ability to execute microcode programs directly from the on-chip dual-port RAM has led to two new options: the Centronics parallel interface and the CCITT Signaling System #7 (SS7) protocol. A standard for printers and terminals, the Centronics parallel interface is implemented with the processor's parallel I/O lines and requires a one-time license charge of $2000. With the SS7

protocol, the chip can control communications between central offices and large PBXs. It has a licensing fee of $5000. Other enhancements enable the 68302 to handle on-chip DRAM refresh without intervention from the on-chip 68000 core processor and without the need for external glue logic. The chip can also transmit fractional stop bits in the universal asynchronous receiver-transmitter (UART) mode for use in rate-adaption schemes for Integrated Services Digital Network and modem applications. ML

SPECIALIZED ALGORITHMS OPTIMIZE PLD DESIGN

Engineers need intelligent synthesis algorithms to take full advantage of the architectures of complex programmable logic devices. Data I/O Corp., Redmond, Wash., addressed this need with Open-Abel, a new version of its Abel PLD design software. With Open-Abel, device manufacturers can supply specialized algorithms, called fitters, to the users of their devices. Consequently, engineers reap the benefits of a universal design language without sacrificing device support or optimization efficiency. Data I/O is licensing semiconductor vendors to interface their fitters to Open-Abel by means of the Abel-PLA format. The Abel-PLA file format is based on the PLA format developed at the University of California at Berkeley. Typical fitters supplied by IC vendors will include more syntax to describe new features, new optimization algorithms, and additional simulation capabilities. They will also incorporate any changes to the algorithm that generates the fuse-map. Furthermore, Data I/O will continue to provide its own device support. For more information, call (206) 881-6444. LG

NOVELL PHASING OUT OF HARDWARE BUSINESS

To increase emphasis on networking software development, Novell Inc. Provo, Utah, is transferring its EXOS line of intelligent Ethernet controller boards, the EXOS trademark, and current EXOS business to Federal Technology Corp., Alexandria, Va. Under the non-exclusive licensing agreement, Novell will still own the current EXOS technology for implementing TCP/IP-to-Ethernet connectivity. Controller boards immediately transferred to FTC include: the 201 and 301 series for Multibus systems; the 202 and 302 series for VMEbus systems; the 203 series for Q-bus systems; and the 204 and 304 series for Unibus systems. The 205 series for PC-bus systems and the 215 series for Microchannel architecture systems are scheduled for transfer by the end of October. The controller-board technology was originally developed by Excelan Inc., whom Novell merged with last year. ML

10-YEAR BATTERIES STEM FROM NEW GLASS

Modifications of existing lithium-sulfur dioxide batteries have yielded a battery that will provide power for 10 years. Scientists at Sandia National Laboratories, Albuquerque, N.M., discovered that glass corrosion in the glass-to-metal seal is the greatest cause of failure in such batteries. By developing a corrosion-resistant glass known as Cabal 12, the scientists could significantly extend the cells' lifespan. Cabal 12 has a corrosion rate about one-third to one-fourth that of other corrosion-resistant glasses. The Sandia batteries work well in applications requiring a high assurance of success, such as nuclear weapons and deep-space missions. DM

ON-CHIP CACHE LOGIC EASES SYSTEM DESIGN

Engineers can now design simpler, high-performance 80386-based systems thanks to a motherboard logic chip from Opti Inc., Santa Clara, Calif. In addition, the chip holds cache-control logic. The company expects that many designers may give up the flexibility afforded by a chip with no cache-control circuitry for a lower-cost but high-performance solution. Opti's use of a direct-mapped cache and posted-write delivers the same performance as a more expensive two-way set-associative cache. The control circuits on the company's 82C281 PC motherboard logic chip for the 386SX can address external cache memories of 16 to 128 kbytes, and makes it possible for users to define non-cacheable regions. Also available is the 82C282, a slightly simpler logic chip without the posted-write capability for more cost-sensitive systems. It lets designers get higher system performance than the page or interleave memory control included into most other company's chip sets. Both chips include a page-mode dynamic-RAM controller that supports 256-kbit, 1-Mbit, and 4-Mbit memories, and all of the interrupt, DMA, counter-timer, and bus-control logic needed to build an AT-compatible motherboard. Contact Raj Jaswa (408) 980-8178. DB

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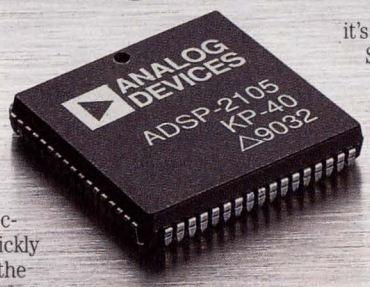

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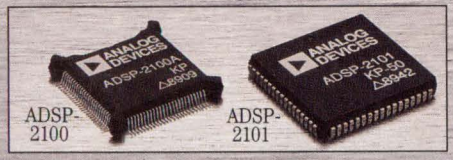

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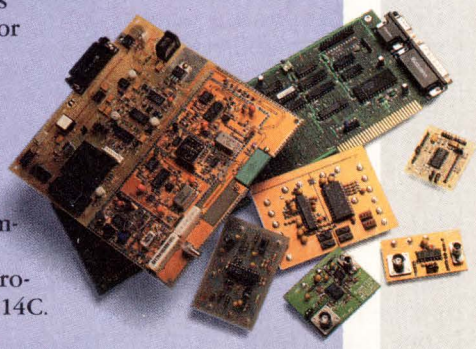

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RAMDAC's On-Chip Digital Signal Processor Gives A Graphics-Workstation Look To PCs

PC designers can now achieve color graphics—with near-workstation-resolution—using just a 6- or 8-bit triple RAMDAC. The chip is a video-palette digital-to-analog converter with a color look-up table. Dubbed CEG-DSP (Continuous-Edge Graphics-Digital-Signal Processor), the ADV7141/7148 RAMDACs emerged from a joint development by Edsun Laboratories, Waltham, Mass., and Analog Devices, Wilmington, Mass.

Edsun developed the CEG antialiasing algorithm and established the system-level architecture. The company also supplies the software drivers. Analog Devices designed the digital-to-analog and digital-signal-processor circuitry using their proprietary CAE/CAD tools (described at the recent Custom Integrated Circuits Conference in Boston). In addition, Analog Devices fabricates the ICs.

CEG raises a PC's level of color graphics from its usual complement of 256 colors available at any one time to 800,000. The additional colors dramatically improve the realism of such 3D effects as shading and highlighting on curved surfaces. In a picture created by these 8-bit RAMDACs, the expected rough, staircase-like edges from curved or diagonal lines turn *(see the figure, left)* into straight lines or smooth curves *(see the figure, right)*.

Without antialiasing, each pixel on the CRT either has or doesn't have a designated color value. In a typical graphics system, if the edge of a smooth shape passes through a pixel, the software approximates the edge as best it can—the pixel is On if more than half is covered by the shape. Even in a high-resolution system with many pixels defining the shape, the eye quickly detects the On and Off dots.

CEG performs antialiasing by permitting the software to choose not only the discrete palette colors, but also a linear mix of those colors. For example, if only one-third of the pixel is covered by a shape, the pixel is displayed in the ratio of 33 to 67. This ratio is the relationship of the shape's color to the background color. The eye perceives the new boundary as a smooth edge. The software driver for the RAMDACs mixes colors in real-time, defining the value of every pixel on a shape boundary. This substantially raises the perceived resolution of the CRT display. And it's done without altering the contents of the standard 256-color lookup table.

What will this technology add to the cost of a PC? The CEG-DSP DACs are pin-for-pin, drop-in replacements for the current 6- and 8-bit converters. Therefore, VGA boards won't require a new layout. That fact, coupled with an under-$25 price tag (in quantities of 10,000), means CEG should add no more than a few hundred dollars to a VGA-compatible PC's cost.

For more information, call Chris Hyde at (617) 937-1422.

FRANK GOODENOUGH and RICHARD NASS

Technique Accurately Pinpoints Peak Temperatures In GaAs MMICs

Because of their reduced susceptibility to radiation, gallium-arsenide FETs are turning up in more microwave/millimeter circuits for aerospace applications. However, even though gallium arsenide does have advantages in radiation, it dissipates heat inadequately compared with silicon. That's why scientists at the Rome Air Development Center (RADC), Rome, N.Y., came up with a new and more accurate technique to determine the peak temperatures of GaAs ICs. The technique involves using a finite-element-analysis program to model the IC and calculate the temperature at the FET's gate region.

In developing the technique, RADC scientists overcame two major obstacles that thwarted past efforts to improve such measurements. First, the gate area of the IC where peak temperatures are found is tiny compared with the chip's size. In conventional analysis techniques, this meant a mesh that was too fine for analysis. In addition, the gate—which is the heat source—is rapidly switched on and off. The result is widely varying temperatures that are hard to pin down. Such rapid temperature changes during pulsed operation pose a concern.

The RADC's work concerned MMICs used in C-band radar modules. The modules consist of transmit and receive components attached to an aluminum chassis, which is attached to a heat-sink plate. Thermal analyses and measurements performed by the module's manufacturer showed that temperatures in the chassis floor were uniform and only 5°C higher than the heat-sink plate. These results told

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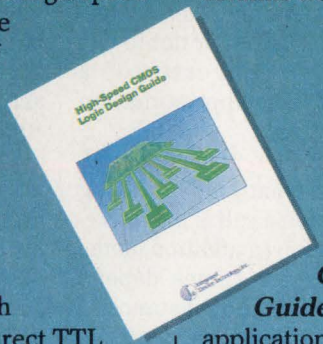

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the RADC scientists to begin modeling at the aluminum chassis. One of the highest heat-producing components in the module is the driver-amplifier IC, generating a peak value of 9 W of heat and an average value of 2.31 W. There are six FET cells in the input and output stages of the amplifier.

RADC's chief engineer, William Bocchi, used the NISA II finite-element-analysis program from Engineering Mechanics Research Corp., Troy, Mich., for his thermal analysis. He began by looking for areas of thermal symmetry, enabling areas of the model to be eliminated. Study of temperature gradients from a preliminary analysis yielded further symmetry conditions, which made it possible for the model to be reduced to only one-fourth of a FET cell. Although this model was considered too coarse to generate peak temperatures, it was useful for calculations of boundary conditions for a third and even finer model. That finer model included one half of a drain, one gate channel, and one half of a source. It provided more accurate temperature distribution.

The final step involved using transient thermal analysis on a 2D version of the first model and then a 3D version of the second model. The pulsed operation of the C-band driver amplifier was simulated by applying a 1-ms pulse followed by a 3-ms pause. The objectives were threefold: One was to determine the variation of temperature with time to obtain peak temperatures; another was to compare transient results with steady-state results that use an appropriate duty cycle; and the third was to determine the distance away from the active region where temperatures are relatively constant with respect to time. Infrared temperature measurements could then be more effectively used.

The results showed why transient analysis is important: peak values in the active region were 55°C higher than steady-state results. As the distance from the active region increased, the peak values approached steady-state values.

DAVID MALINIAK

INTELLIGENT SOFTWARE HELPS DIGITAL DESIGNERS BUILD ANALOG CELLS

Digital engineers often struggle designing mixed-mode systems because their analogy technology knowledge comes only from textbooks. Gould AMI, Pocatello, Ida., developed an innovative approach to analog modeling that should solve this dilemma. The Analog Model Builder, which will be available in January 1991, will enable engineers to create analog behavioral models online simply by entering values for key analog parameters.

Although this approach to model building isn't new to digital design, it hasn't been done for analog cells. Creating a model builder for analog cells is much harder than for digital cells. The difficulty isn't writing the model-builder software, but conceptualizing the idea that analog cells can be broken down into primitives like digital cells. Developing analog primitives isn't as simple as making digital primitives, such as breaking down a flip-flop into gates and transfers. In analog technology, the primitives are larger and more complex.

Gould approached the problem by breaking down the most common analog building blocks (such as large gain cells, analog-to-digital converters, and sample-and-hold amplifiers) into individual primitives (such as current sources and small gain blocks). These primitives were then broken down into smaller primitives, which include resistors and capacitors. When engineers need to create a model for an analog cell, the Model Builder uses a silicon compiler to build up large blocks from smaller primitives.

When the tool is called to the screen, the Analog Model Builder presents users with a menu of analog functions. Selecting a function brings a pseudo data sheet up on the screen, complete with minimum and maximum values allowed for each entry. Users must supply the input to the data sheet. As an example, for an ADC, the tool may ask for the input voltage supply, tolerances for the least-common bit, and speed. The designated speed would then determine whether or not to use a flash converter or a successive-approximation converter.

Parameters vary according to what kind of analog function a cell is being created for. In addition, some parameter values depend on others. For instance, a dynamic range can't be larger than the power-supply voltage. These types of dependencies will be checked by the Specification Advisor, a proprietary expert software contained in the Model Builder. The Specification Advisor determines the feasibility of an analog cell based on the user-defined parameters. It also estimates area and power consumption. Designers can use these values to approximate costs and determine trade-offs on-line.

The Model Builder outputs a schematic-capture symbol, a behavioral-level analog model, and the analog-cell specifications used by Gould AMI to generate the actual cells. When users need more detailed simulation, they send the specifications to Gould AMI. The company employs the Parameterized Analog Building Block Generator (PABB) to form a second- and third-order model for accurate system simulation. The PABB, which will stay a Gould in-house function, also generates information needed to actually build the analog function in silicon.

The Analog Model Builder is part of Gould's Mixed-Signal Design Solution II system that will be available in January. Analog functions that will be available include a sample-and-hold amplifier, a switched-capacitor filter, a crystal oscillator, and an ADC.

LISA GUNN

SOFTWARE BREADBOARD TEACHES DESIGN METHODS BY EXAMPLE

A novel simulation tool from Texas Instruments, Dallas, teaches engineers how to design DSP-based boards. Specifically, it demonstrates how the TI TMS320C30 digital signal processor works in an application, how to verify ASIC performance in the application before committing to silicon, and how to design for testability using JTAG boundary-scan technology. To accomplish this, the tool—called DSP/Scope SimuBoard—provides engineers with a software breadboard for an example DSP application.

DSP/Scope SimuBoard is the first software breadboard that simulates a DSP application combining ASICs, standard-device models, and models supporting the IEEE 1149.1 design-for-test (DFT) capabilities. Designed as an audio application, SimuBoard shows how the C30 processor is used for a speech-processing algorithm that implements pitch detection and speech compression. The simulation employs a fully functional C30 SmartModel from Logic Automation, Beaverton, Ore., to execute the software code that performs the algorithm.

The tool emphasizes ASIC simulation at the board level. Even after undergoing extensive test vectors, ASICs may not work properly when put in a board because of timing or functional problems at the board level. The TI SimuBoard indicates that by simulating an ASIC in the board, engineers can uncover difficult problems before the design is implemented in silicon.

The SimuBoard kit is a computer-aided reusable engineering (CARE) package that includes schematics, user documentation, support software, and SmartModels for TI's C30 digital signal processor, Scope octal buffers, and memory. TI TGC100 gate-array models are included for the Simuboard's ASIC, which is a floating-point conversion function with Scope cells. Scope is TI's system controllability/observability partitioning environment.

A JTAG scan path is built in the board's design to show engineers how to simulate a serial scan chain in a board. The SimuBoard demonstrates how to execute JTAG instructions in a Scope octal buffer, and details TI Scope instructions for built-in self-testing.

The board is partitioned, and includes manufacturing-defect board-level vectors—serial vectors that have been fault-graded to explain to designers how to use JTAG capabilities in a Mentor Graphics design environment. These vectors can then be reused to test the actual hardware prototype using TI's Asset scan-based diagnostic tool. As a result, the tool describes a DFT methodology from simulation to prototype test.

For more information on the software breadboard, call (800) 336-5236, ext. 700 in the U.S. and Canada, and (214) 995-6611, ext. 700 from any other location.

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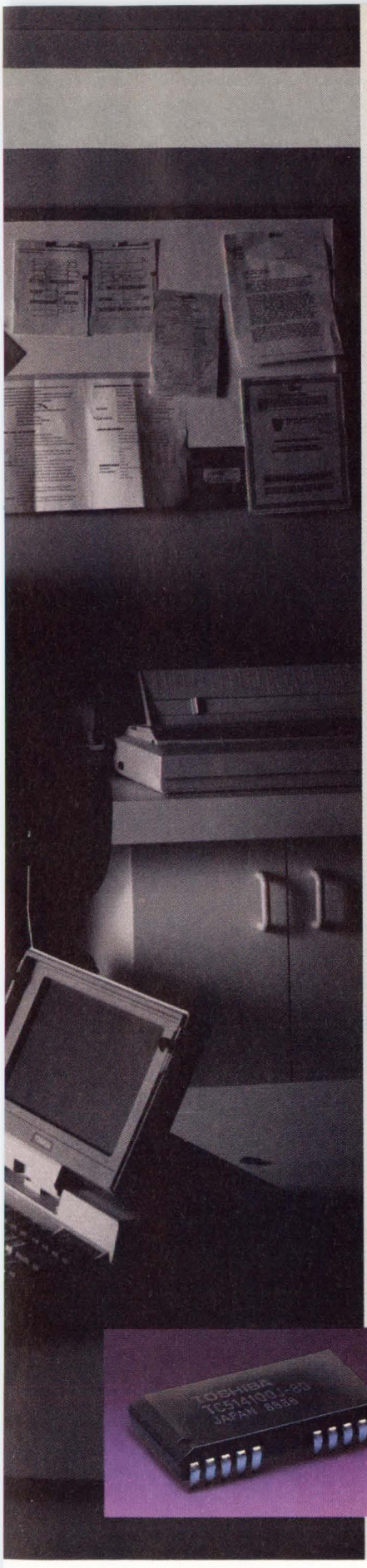

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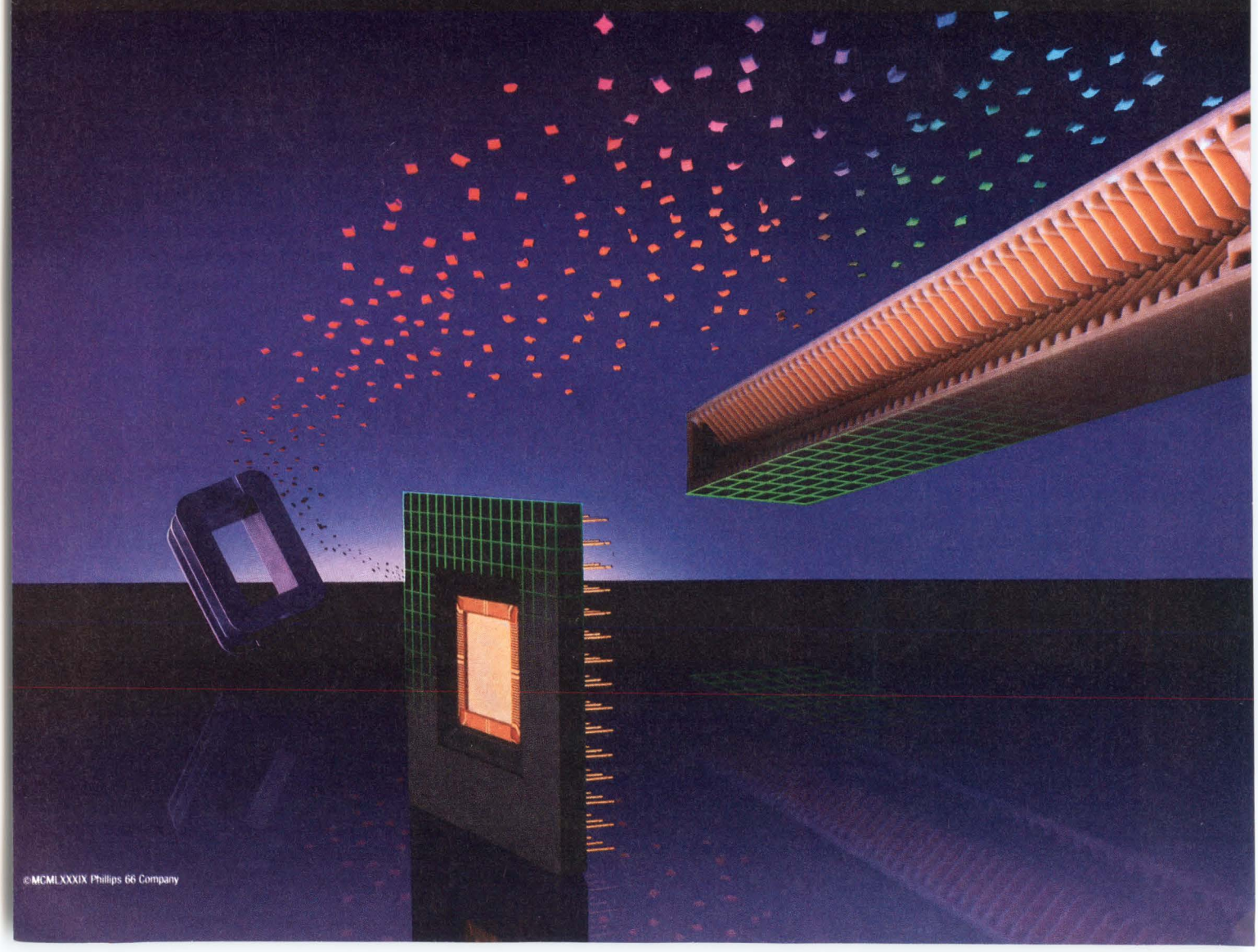

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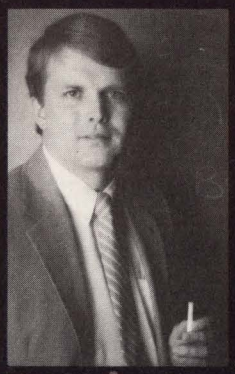

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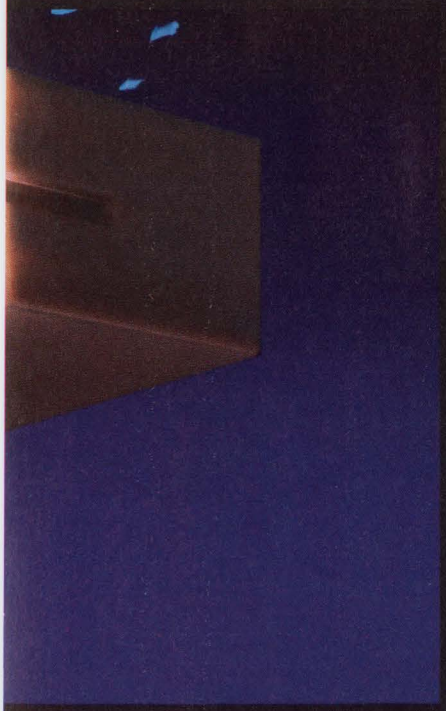

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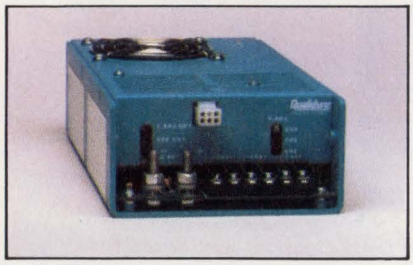

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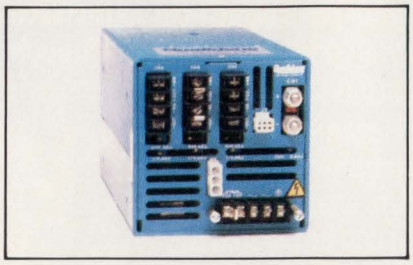

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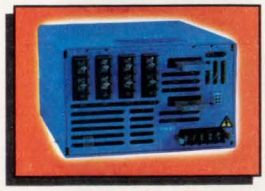

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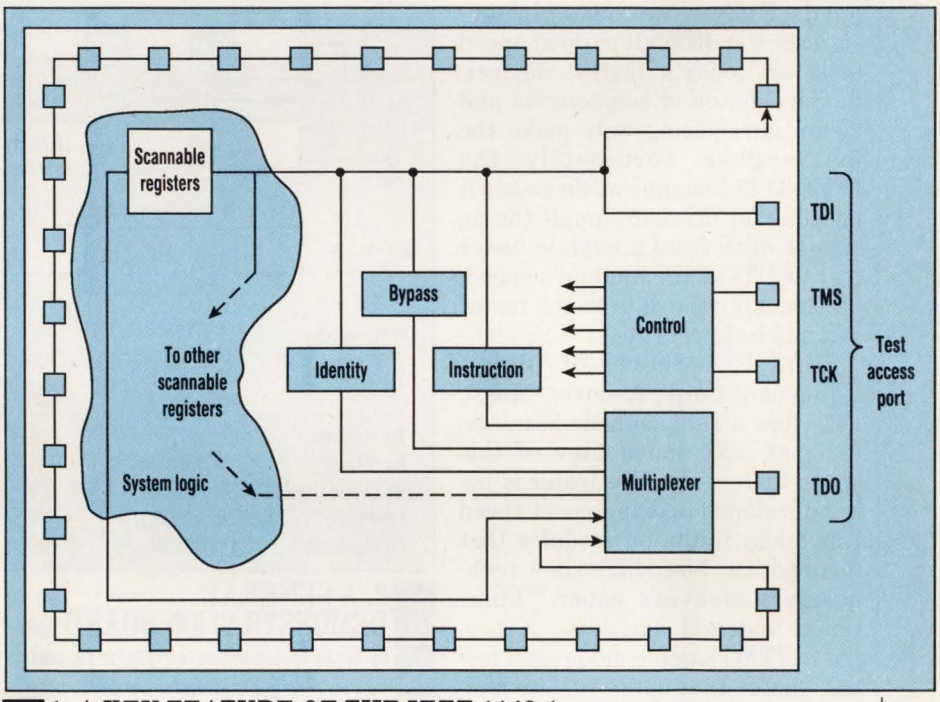
BOUNDARY SCAN HOLDS COURT AT ITC '90

TECHNICAL PAPERS ON IEEE-1149.1 AND A MEETING WITH ITS AUTHORS HIGHLIGHT THE SHOW.

JOHN NOVELLINO

Appropriately enough, the upcoming International Test Conference features a strong collection of technical papers on various aspects of boundary-scan techniques. The show comes soon after the formal approval of an IEEE standard for this emerging technology. This standard helps ease the task of testing densely packed pc boards containing components with closely spaced pins or surface-mounted components. But no standard can cover all aspects of a technology, so plenty of room exists for discussions on the partial use of boundary-scan components, descriptive languages, test-pattern generation, and other related topics.



1. A KEY FEATURE OF THE IEEE-1149.1 boundary-scan architecture is the test access port. Here, test signals can be serially applied and read on only four pins.

More than a dozen papers at ITC '90, scheduled for September 10 through 14 in Washington, D.C., discuss these topics as well as specific applications of boundary-scan testing. In addition, the conference features a two-hour panel session with the members of the IEEE-1149.1 working group. This open meeting offers attendees the chance to discuss any problems or suggestions they encountered while implementing their own designs with the people who actually developed the standard.

Work on the boundary-scan standard began in November 1985 with the formation of the Joint Test Action Group (JTAG). Some of the biggest names in the electronics industry were among the group: AT&T, British Telecom, DEC, Hewlett-Packard, IBM, Motorola, Philips, Siemens, and Texas Instruments. The idea was to replace the traditional probe technology—the so-called bed-of-nails fixture—that had become too expensive and unreliable for testing high-density boards with VLSI and surface-mounted components. By April 1988, a technical proposal for boundary scan existed, and development of the standard was transferred to the IEEE.

The IEEE Standards Board approved IEEE Standard 1149.1, IEEE Standard Test Access Port and Boundary-Scan Architecture, last February 15 and the document was published in May. The standard defines the test circuitry required in ICs and a uniform chip-level interface for communicating test, maintenance, and support information.

With the four-pin (optionally five-pin) test access port (TAP), external devices can communicate with the on-chip test circuitry *(Fig. 1)*. The required pins include Test Data In (TDI), Test Data Out (TDO), Test Mode Select

(TMS), and Test Clock (TCK). To achieve this minimal number of pins, instructions and data are transmitted serially. The on-chip circuitry includes a scan path that enables the tester to determine whether the IC is properly connected. Also defined is an optional self-test mode for the IC itself as well as other functions, such as the ability to read an identity tag embedded in the test circuitry.

Taming The Speed Demon

One common problem test engineers face is keeping up with the speeds of the products being developed. Under the best circumstances, it's difficult to do at-speed tests on today's fastest devices. Surface-mounted components and 25-mil pin spacing only make the job tougher. Fortunately, the IEEE-1149.1 sample mode makes it possible for users to sample the response data from a module under test (MUT) at the module's speed, but transfer the data to the tester at a much slower rate.

Mark F. Lefebvre of Digital Equipment Corp., Andover, Mass., describes a sample-mode scan tester that takes advantage of this speed difference. The tester is being developed to diagnose at-speed functional faults on modules that incorporate boundary-scan technology. Lefebvre's paper, "Functional test and diagnosis: A proposed JTAG sample-mode scan tester," notes that initial results indicate that sample-mode testing can effectively reveal faults on boards where the lack of physical access prevents the use of traditional functional testing.

The test procedure captures the nodal response of the desired test-sequence cycle at the boundary-scan latches required in devices that comply with IEEE-1149.1. This data is then shifted to the tester. The transfer, however, doesn't have to occur immediately after capture and needn't be done at MUT speed. The tester Lefebvre describes includes a scan subsystem and a host processor. The scan subsystem contains hardware that manipulates the MUT interface and controls the operation of the 1149.1 devices on the MUT. The host processor—a VAXStation 3500—controls the scan subsystem, executing the needed software modules. The application program is also loaded and executed from the host processor.

The technique does have some limitations. For one, the MUT must contain the signals and logic needed to synchronize the module test sequence and the tester's operation. In addition, the relationship between the MUT and the test clocks will determine the tester's effectiveness. Finally, for satisfactory diagnostic resolution, a large percentage of the MUT devices must comply with IEEE-1149.1.

That last condition reflects one concern of boundary-scan testing. Although the technology has been well received, it will be a long time, if ever, before pc boards contain 100% boundary-scan devices. Gordon D. Robinson and John G. Deshayes of GenRad Inc., Concord, Mass., address this problem in their ITC '90 paper, "Interconnect testing of boards with partial boundary scan." The authors note that diagnosing shorts and opens on boards with both boundary-scan and non-boundary-scan parts is difficult, largely because the normal parts are powered, active, and unpredictable when the boundary-scan circuitry is used.

The test procedure requires four stages. The first is a conventional shorts test between all of the places where the tester has physical access. Next comes a scan-path integrity test, which ensures that the testability circuitry in the boundary-scan devices and the scan-path segments between components work well enough to be used in later stages.

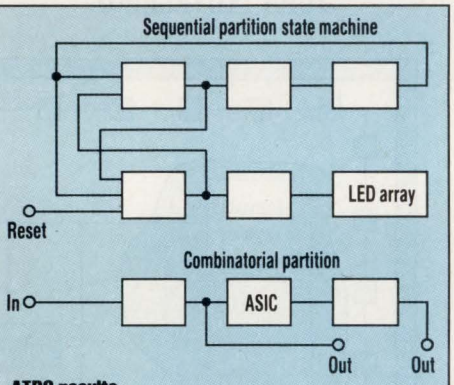
The third stage is an interaction test, which checks for shorts between nodes with physical tester access and boundary-scan nodes without such access. The last stop is an interconnect test that looks for opens and shorts on the pure boundary-scan nodes. This stage is similar to other boundary-scan interconnect test methods.

Normal Devices Disabled

When checking for shorts between nodes with full or partial boundary-scan control and boundary-scan or tester observability, the authors include the board's edge connector inputs and outputs. This is because they can be controlled and observed as easily as the boundary-scan nodes. When the test is in this stage, a set of precalculated patterns identifies groups of nodes that may be shorted. Then a set of adaptively generated patterns walk a dominant value through these groups.

If a node can be driven by either a boundary-scan or non-boundary-scan component, the normal component must be disabled by holding its enable line at the disable value. This is done with standard in-circuit isolation algorithms.

If boundary-scan testing is to gain wide-spread acceptance and use, the industry must have a standard language to describe the essential features of devices that comply with



ATPG results

	Combinatorial/ sequential/total	Whole
No. of devices	13/17/30	28
No. of faults	352/198/550	548
No. of fault classes	241/139/380	379
Fault grade (%)	97/100/98.1	98.3
No. of patterns	37/69/106	100

2. A GENERAL DEMONSTRATION BOARD built by Texas Instruments to evaluate automatic test-pattern generation for boundary scan was configured to drive an LED array. The ATPG tests were performed twice—once with the board partitioned into sequential and combinatorial logic, and again with the board as one entity.

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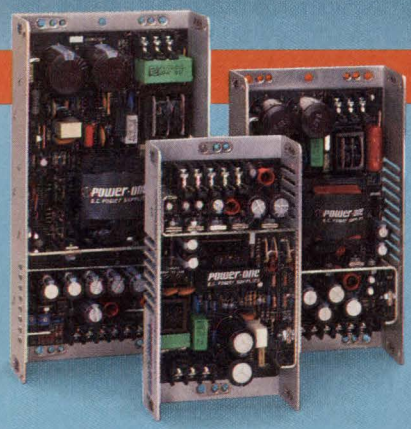

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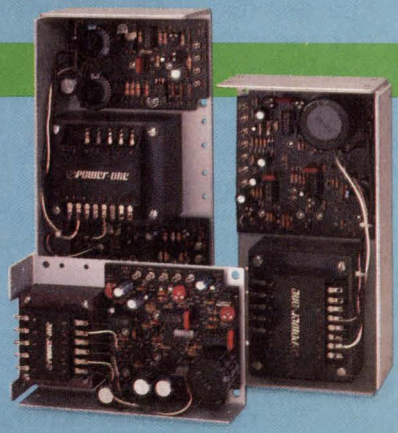

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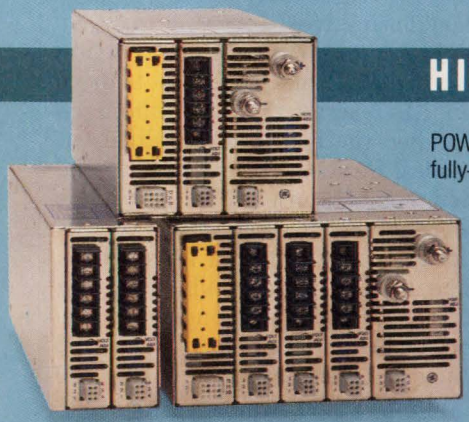

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CIRCLE 151

IEEE-1149.1. The document leaves much room for user-designed features and options, so designers will need a way to describe their particular implementations. Kenneth P. Parker and Stig Oresjo of Hewlett-Packard's Manufacturing Test Div., Loveland, Colo., propose a solution in their paper, "A language for describing boundary-scan devices." The language was developed with input from a large number of companies, many of which helped draft IEEE-1149.1.

The language, dubbed Boundary-Scan Description Language (BSDL), is a subset of the VHSIC Hardware Description Language (IEEE Standard 1076-1987, VHDL). The authors state that the language was written with two criteria in mind: that it be user-friendly when writing files, and that it be simply and unambiguously parsable by computer. Another benefit, according to the paper, is that users who attempt to code device features or make semantic checks may discover compliance violations in the device. If a device can't be described by BSDL, the component doesn't comply with 1149.1.

BSDL isn't a general-purpose hardware description language; it describes the testability features of 1149.1-compliant devices. With a BSDL description and a knowledge of the standard, tools for testability analysis, test generation, and failure diagnosis can understand the data-transport characteristics of a device. VHDL's additional capabilities permit simulation, verification, compliance analysis, and synthesis functions.

The proposed language concentrates on the many options that designers of boundary-scan devices can choose. In fact, it doesn't include design elements required by IEEE-1149.1. For instance, BSDL doesn't describe the Bypass Register because the standard fully defines it, without options. The authors note that going this route should eliminate both redundancy and the opportunity for error.

An area in which boundary-scan techniques should have a major impact is automatic test pattern generation (ATPG). Few ATPG tools are available for board testing, but IEEE-1149.1 should facilitate both manual and automatic pattern generation for boards. The key is proper partitioning of the board into the logic clusters required by 1149.1, according to "ATPG issues for board designs implementing boundary scan."

ATPG Experiment

The paper—written by Don Sterba, Andy Halliday, and Don McClean of Texas Instruments' Defense Systems and Electronics Group, Plano, Tex.—describes an experiment conducted on three different types of demonstration boards to evaluate ATPG in a boundary-scan environment. According to the authors, the partitioning makes it possible for the ATPG tools to work on smaller clusters of logic, rather than on a complete board, making ATPG more feasible.

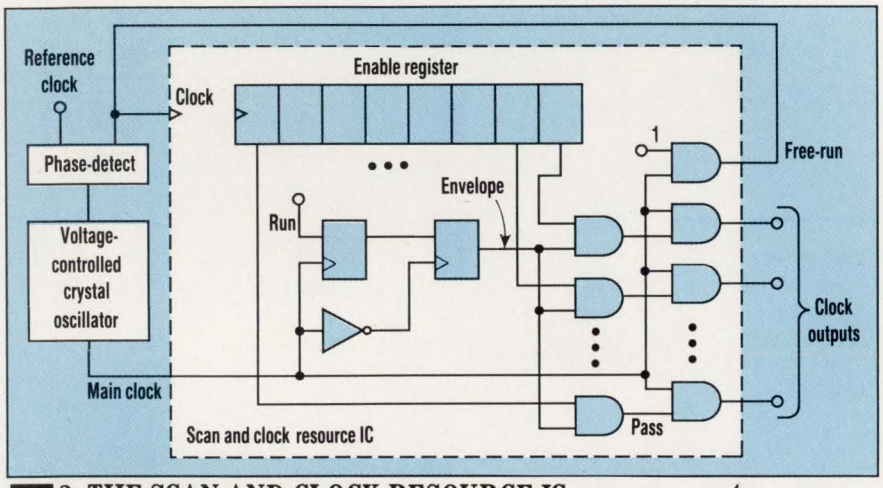
The first board was a general demonstration board that held a small design with a sequential logic partition and a combinatorial logic partition that included a boundary-scan ASIC. The second was a more complex board with a boundary-scan ASIC, a statistical data processor, a speech processor, state machines, and a VME-bus interface. The last board was based on a digital signal processor and contained a boundary-scan ASIC, two digital-signal-processor chips (one with boundary scan), a microcontroller sequencer, and a VME-bus interface.

Conventional buffers, transceivers, latches, and registers were replaced with TI's Scope Octals, which have boundary-scan capability. The ATPG and fault-simulation tool used was Racal Redac's Intelligen/Cadat, which handles sequential and combinatorial logic and processes functional primitives.

The general demonstration board's state machine outputs drive an LED array *(Fig. 2)*. Intelligen handled the board in two different modes. First, the board's sequential and combinatorial logic partitions were submitted separately. Then the design was submitted as a whole. The results were similar, varying only because of the duplication required by the partitioning. About 100 patterns were generated and 550 faults were defined. Fault coverage was better than 98%.

The authors concluded that designers implementing boundary scan should follow general guidelines for design for testability (DFT), especially the isolation of complex devices. By replacing standard parts with scannable ones, many DFT features can be used without any additional components. Also, a structured, hierarchical method of design capture in the CAE environment will make partitioning easier.

Taking advantage of scan-based



3. THE SCAN-AND-CLOCK-RESOURCE IC designed by Apollo Computer uses a phase-locked loop and voltage-controlled crystal oscillator to align clocks from different boards with each other.

ITC HIGHLIGHTS BOUNDARY SCAN

techniques, Apollo Computer, Chelmsford, Mass., designed a chip that can act as a centralized resource to control board-level test functions. By placing this scan-and-clock-resource (SCR) chip on each board, Apollo can link every board to an internal or external test processor, eliminating the need for specialized in-circuit testers. The SCR chip is used on the Apollo DN10000 workstation.

Bulent I. Dervisoglu describes the SCR in his ITC '90 paper, "Towards a standard approach for controlling board-level test functions." Besides accessing the scan paths and other testability features available on the board, the chip generates the necessary clock signals. It can supply separate control and clock signals for up to eight independent ports. Apollo, a division of Hewlett-Packard, selected certain differences in the features of various board components handled by the SCR. Other differences must be resolved by the diagnostic software. Consequently, the chip works with boards that have both scan-based and non-scan parts.

The clock circuitry minimizes the skew among the several clock signals *(Fig. 3)*. A local voltage-controlled crystal oscillator and phase-locked loop align clocks from different boards with each other. A free-running output from the chip is fed back to supply the SCR's own clock.

The SCR has a limited instruction set that uses or modifies a set of 16-bit internal registers. The three categories of instructions include register op instructions, which read or write the registers; clock control instructions that start or stop the functional clock; and scan control instructions, which perform regular scan-in/scan-out operations or generate pseudo-random test vectors and capture test signatures. All instruction op codes are 8 bits long.

Dervisoglu notes that one advantage of this approach is that the target chips and boards can share the controller's features. As a result, testability features that may be too costly to include in the individual chips can be made available through the SCR.□

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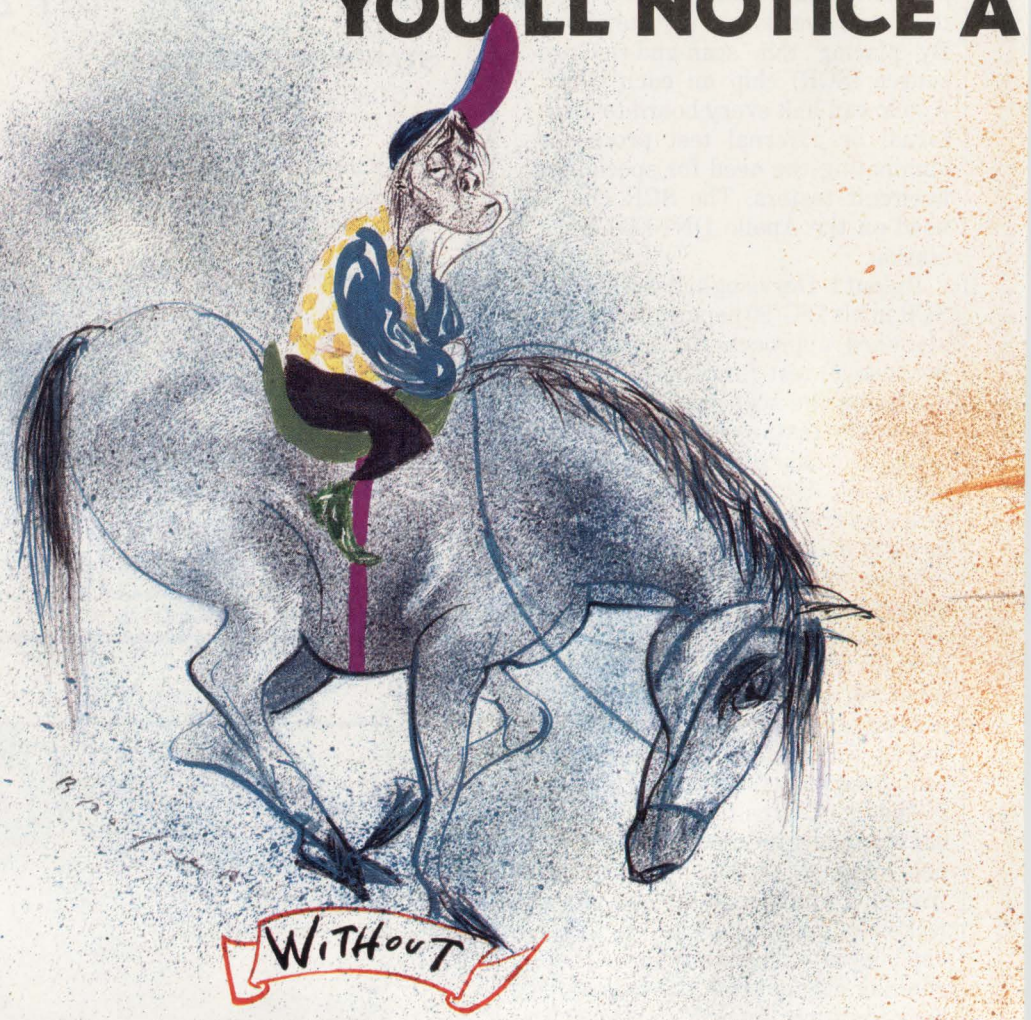

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5-2-2-2	120 ns	20
5-2-2-2	80 ns	25
6-2-2-2	120 ns	25
6-2-2-2	80 ns	33
7-2-2-2	100 ns	33

68040 PERFORMANCE SUMMARY

Access Clocks	*DRAM Speed*	*Frequency (Mhz)*
3-2-2-2	80 ns	25
5-2-2-2	100 ns	25
6-2-2-2	120 ns	25
5-2-2-2	80 ns	33
6-2-2-2	100 ns	33

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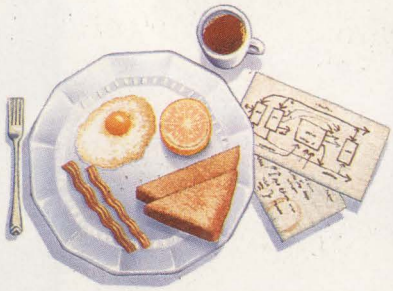
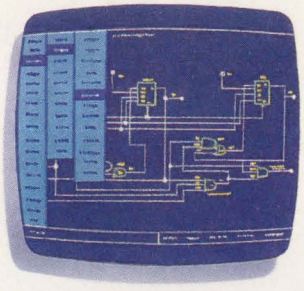
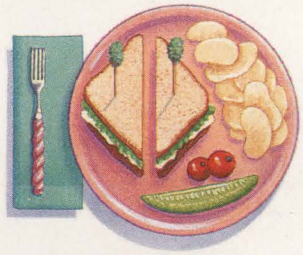


7:05 am: Breakfast
Suddenly, between bites, the answer to that new system design jumps right into your brain. But how to make it work in silicon? Use an Actel field programmable gate array!



8:50 am: Design
You warm up the design program on your 386 and put in the final touches. Then a quick rule check and 25 MHz system simulation with the Action Logic System software.

11:00 am: Place & Route
You watch the system place and route all 1700 gates (out of 2000 available) in under 40 minutes. 100% automatically! A final timing check. Then think of something to do until lunch.



12:00 pm: Lunch
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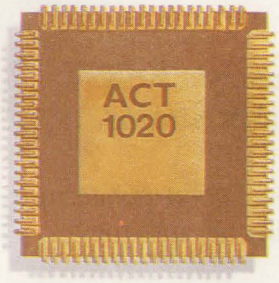
Breakfast And n By Dinner.



1:15 pm: Program
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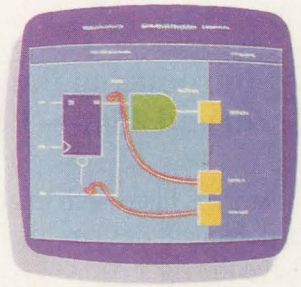

1:25 pm: Test
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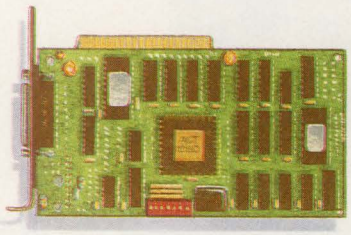

4:00 pm: Production
Your pride and joy is designed, created, tested, and off to the boys in Production. And you're finished way ahead of schedule! Better think of something to do until 5:00.

6:00 pm: Dinner
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CIRCLE 100

DELTA-SIGMA ARCHITECTURE PUTS TWO 18-BIT AUDIO DACS—COMPLETE WITH DIGITAL AND ANALOG FILTERS—IN A TINY 28-PIN SOIC.

18-BIT AUDIO DACS CUT PCB SPACE DRAMATICALLY

FRANK GOODENOUGH

Open a compact-disc player, and you'll find that the digital-to-analog conversion section occupies 8 in.^{2} of space, approximately. The section includes a two-channel digital interpolation filter IC, followed by a dual 16- or 18-bit DAC chip. The DAC drives an IC with a pair of continuous-time lowpass smoothing filters. Rounding out the section is an IC with a pair of output op amps *(see the opening illustration)*. Not including a DAC, these four IC packages plus a handful of resistors and capacitors for the filters cost about $30 to $40 (in 1000-unit lots). And an 18-bit dual DAC could run another $15 to $20 in cost.

Crystal Semiconductor has replaced all of those parts with a true subsystem-on-a-chip in one 28-pin SOIC package—the CS4328. The chip is just 0.7-in. long by 0.4-in. wide, including pins (it's also available in a 28-pin DIP). Moreover, with an A-weighted dynamic range of 97 dB, it's as good as any audio DAC commercially available over the audio range. A-weighting is a term that refers to a standard curve that defines a CD player's modified frequency response. The complete DAC sub-system, which includes separate analog and digital CMOS chips on the same leadframe in one package, will be priced at about $30 each in 1000-lot quantities *(see the table)*.

Crystal accomplished this miniaturization task by applying its expertise in delta-sigma analog-to-digital converters and by translating it into delta-sigma DACs. The tiny SOIC package contains two complete 18-bit DACs. The DACs, without any other components, take a standard 3-line serial input from the audio data processor and supply a pair of outputs ready for an RCA-type phone-jack. That is, the two outputs are ready to put 2 Vpk-pk across 600 Ω.

The 36,800 mil^2 digital die is built on a 1.5-μm process, while the 28,500-mil^2 analog chip is built on a 3-μm process. Similar to most digital ICs, the former can be shrunk easily with a new mask set and a finer-geometry process, for possible further cost reductions (Crystal

has already shrunk the digital die in their audio ADC).

There's much more to the CS4328 dual-DAC ICthan its application in a CD player. For openers, it's a pair of true, slightly better than 16-bit-accurate, glitchless DACs that can be updated at rates that are better than 50 kHz. Each of the two DACs costs about $15 in 1000-unit lots. Moreover, the analog smoothing filter in the output circuit of each DAC directly tracks the DAC's input word rate. Consequently, the same device can be used for diverse applications without redesigning a filter circuit.

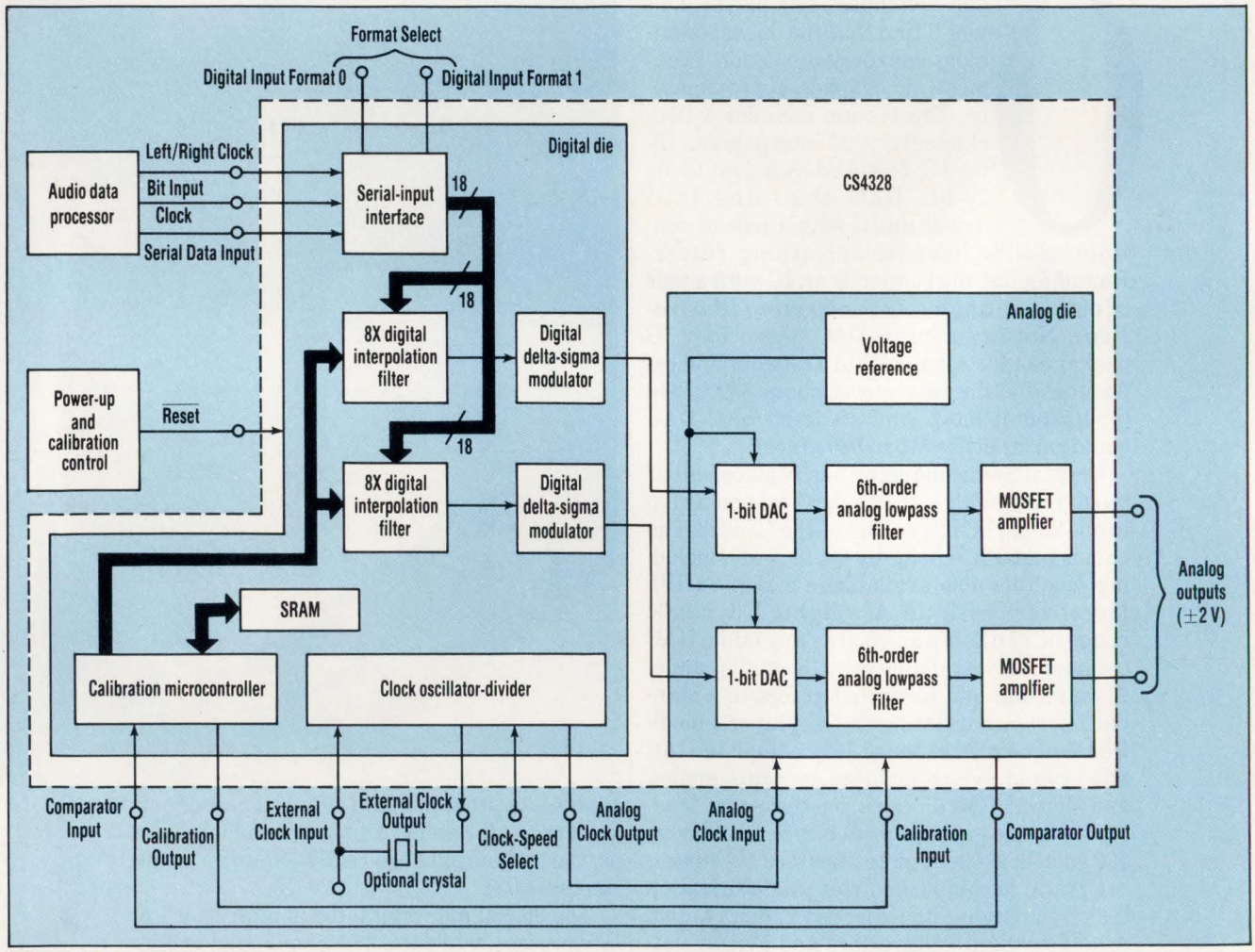
These applications include precision waveform generation for a variety of uses, ranging from ATE and arbitrary waveform creation to complimenting a delta-sigma ADC in DSP applications. Other applications include music synthesizers, studio audio systems, and musical-instrument keyboards. Note that if a dc voltage is required from these DACs, they must be refreshed constantly with the same digital word.

A more esoteric application involves music composition on workstations. Software designers can write music for composers on their workstations. Once connected to one or more DACs and a multichannel audio system, the designers can listen to the music instantly.

A Closer Look

Following the IC's serial input interface block are 8X oversampled digital interpolation filters *(see the figure)*. The filters drive 64X oversampled digital delta-sigma modulators, each producing a 1-bit bitstream. In the 1-bit DACs, the bitstream converts the reference to a train of pulses with constant height and variable-ONEs density (ONEs density is the ratio of the number of ONEs to the number of ZEROs for a given period of time).

The analog pulses from the DACs are applied to the 4th-order switched-capacitor, lowpass, analog filters. The pulses drive two-pole, continuous-time filters to eliminate switched-capacitor clock noise. The switched-capacitor filter conveniently tracks the clock frequency, making it possible for the 4328 to be used



TWO CHIPS COMPOSE the CS4328 18-bit, dual complete audio DAC: a digital circuit on a large and dense die made in a 1.5-μm CMOS process (left), and a precision analog circuit on a smaller die made in a 3-μm CMOS process (right). The digital circuit converts a 30- to 50-kHz bit-stream to an oversampled, digitally filtered, delta-sigma modulated stream. The analog circuit, in turn, converts the modulated stream to a pair of audio signals ready for a headset or a stereo amplifier.

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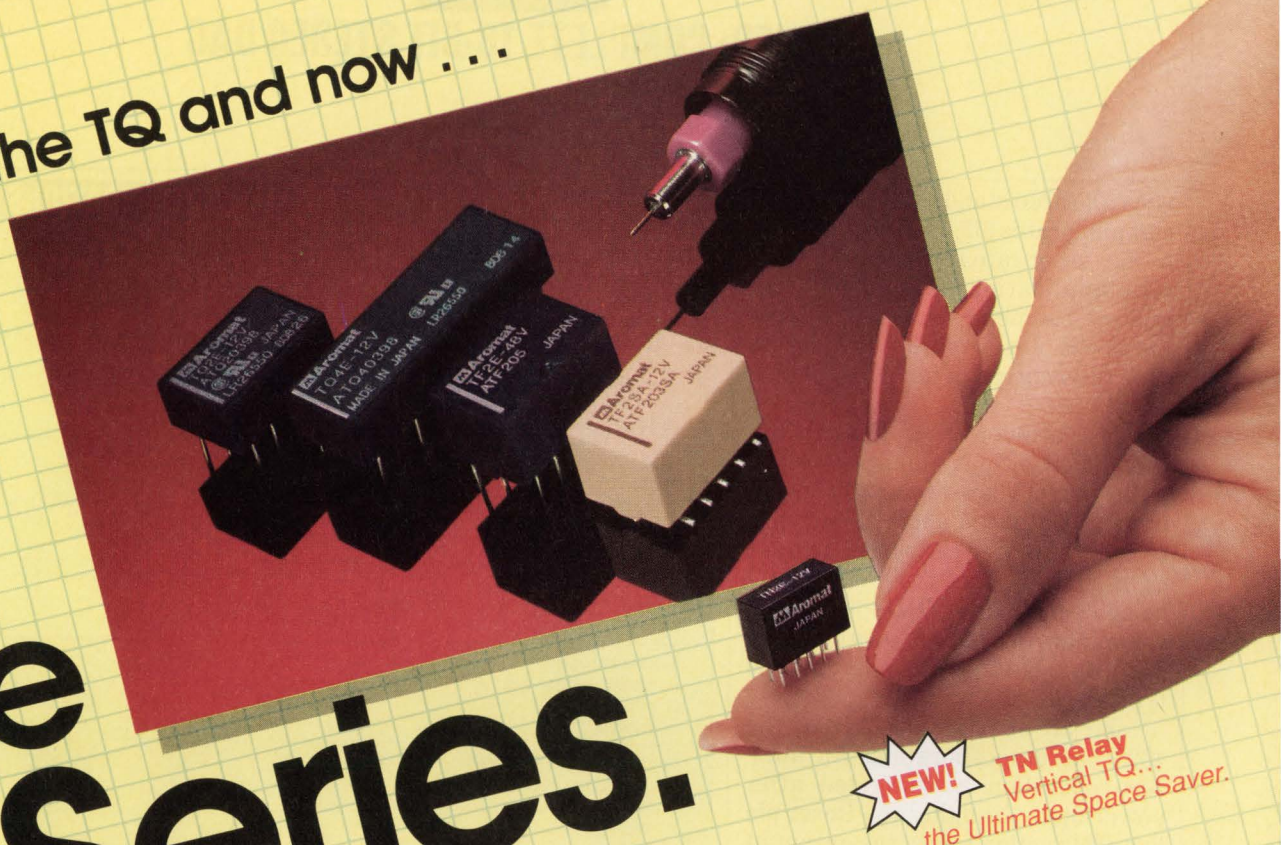

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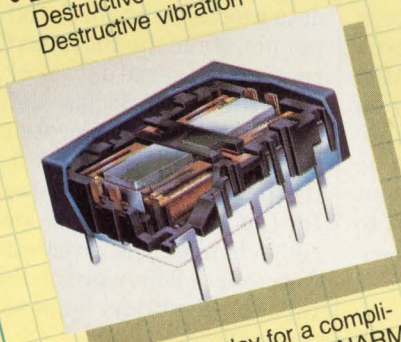

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with all three standard digital-audio sampling rates (32, 44.1, and 48 kHz), or any other rate required for a specific application. If very-low-frequency sampling—say a few kilohertz—is used, more continuous-time filtering can be added at the output stage.

The continuous-time filter drives the CMOS output amplifier, which puts out ±2 V across 600 Ω. The amplifier's output is short-circuit protected by limiting the output current to ±20 mA. The 4328's signal-to-noise + distortion (THD+N) ratio is a minimum of 93 dB. A-weighted, the 4328 dual-DAC's THD+N ratio is typically 97 dB.

Like all of Crystal's ADCs, the 4328 has autocalibration. An autozero operation is instigated after power-up by bringing the $\overline{\text{Reset}}$ pin low. This action forces the output of the DACs to zero (through the calibration microcontroller) and resets the digital filter and modulator. The digital correction word is stored in the static RAM. When $\overline{\text{Reset}}$ goes low, the Calibration Output signal goes high and stays high until the end of an offset-calibration cycle, which takes 1024 input-word-rate cycles to occur (the input word rate is the frequency at which new words for each channel are fed to the DACs, and is the same as the frequency on the Left/Right Clock line). The Calibration Output signal line must be connected to the Comparator Input signal line for offset calibration to occur.

System Signals

Because the 4328's digital-signal and control circuits are versatile, the IC can operate with four different serial data formats of 0 through 3. Format 0 is compatible with the combination of existing 16-bit DACs and digital-filter chips. Format 1 is the 18-bit variant of format 0. Format 2 is similar to that of Crystal's ADCs and many DSP serial ports. Format 3 is compatible with the popular I^2S serial data protocol.

Formats 2 and 3 support 18-bit words, as well as 16-bit words followed by two zeros. All formats employ a two's-complement code, with the most-significant bit being first.

Data is brought in from the audio data processor on the Serial Data Input pin, while the Bit Input Clock pin receives the serial data clock, and the Left/Right Clock pin defines the channel and data delineation *(see the figure again)*. In formats 0, 1, and 2, the Left/Right Clock signal is high for the left channel and low for the right channel. The reverse is true for format 3. A 2-bit word on the Digital Input Format 0 and 1 pins selects the type of format desired.

The DAC's master clock signal comes in on the External Clock Input pin. Alternatively, a crystal may be connected between the External Clock Input and External Clock Output pins.

The master clock, whose frequency is a function of the desired input word rate and the Clock-Speed Select signal, runs the interpolation filters and delta-sigma modulators. By setting the Clock-Speed Select line low, an External Clock Input frequency is chosen that's 256 times the input word rate. Setting it high produces an External Clock Input signal that's 384 times the input word rate.

The Analog Clock Output signal frequency, which clocks the switched-capacitor smoothing filter, is always 128 times the input word rate. For example, if the Left/Right Clock signal is 44.1 kHz and the Clock-Speed Select signal is low, the External Clock Input signal should be 11.2896 MHz and the Analog Clock Output signal will be 5.6448 MHz. If the Clock-Speed Select signal is high, XTI should be 16.9344 MHz but XTI is still 5.6448 MHz.□

CS4328 DUAL 18-BIT DAC SPECIFICATIONS

Parameter	Minimum	Typical	Maximum	Units
Dynamic range	93	95		dB
Dynamic range (A-weighted)		97		
Signal-to-noise + distortion ratio				
0 dB out	92	94		dB
–20 dB out		75		dB
–60 dB out		35		dB
–20 dB out (A-weighted)		77		dB
–60 dB out (A-weighted)		37		dB
Phase response		±0.5		Deg.
Passband (see note)				
To 3-dB corner	0		23.5	kHz
To 0.001-dB corner	0		21.6	kHz
Ripple			0.001	dB
Stopband	26.4			kHz
Stopband attenuation	90			dB
Interchannel isolation		–80		dB
Dc interchannel gain mismatch		±1		mV
Dc gain error			±5	%
Dc gain drift		150		ppm/°C
Dc offset error (after calibration)		±1		mV
Full-scale output-voltage range	±2			Vpk-pk
Power-supply current				
Analog @ +5 V		35		mA
Analog @ –5 V		35		mA
Digital @ +5 V		50		mA
Power-supply rejection ratio		30		dB

Analog characteristics are at 25°C; supply rails = ±5 V; full-scale output sinewave = 991 Hz; input word rate = 48 kHz; data clock = 3.072 MHz; load R = 10 kX; measurement bandwidth is 10 Hz to 20 kHz, unweighted unless noted.

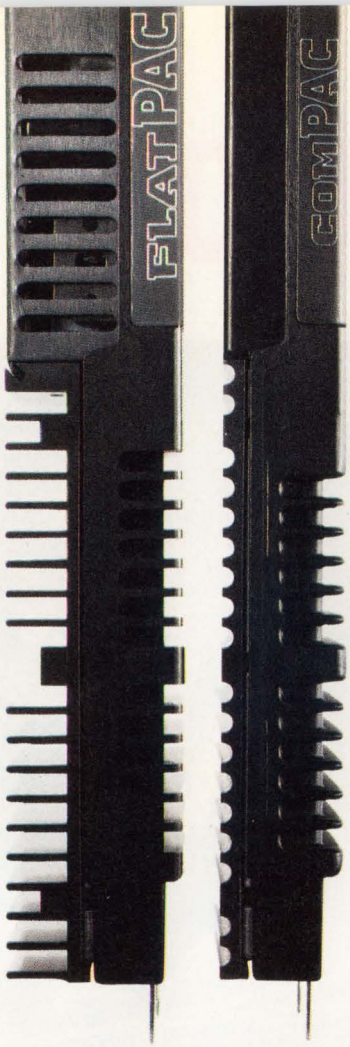
Note: The passband and stopband edges scale with frequency. For input word rates (IWRs) other than 48 kHz, scale the 0.001-dB passband edge by 0.45 X IWR and scale the stopband edge by 0.55 X IWR.

Price And Availabilty

The CS4328 18-bit dual stereo DAC in a 28-pin plastic SOIC goes for $35 each in quantities of 100. Its identical twin in a 28-pin plastic DIP goes for $30 each in the same quantities.

Crystal Semiconductor Corp., P.O. Box 17847, Austin, TX 78760; Brad Fluke, (512) 445-7222. **CIRCLE 512**

How Valuable?	Circle
Highly	547
Moderately	548
Slightly	549



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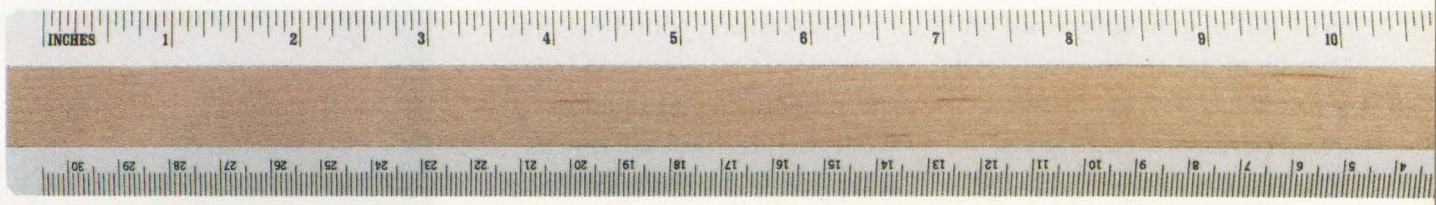

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Up to 600 Watts	**Output Power**	Up to 600 Watts
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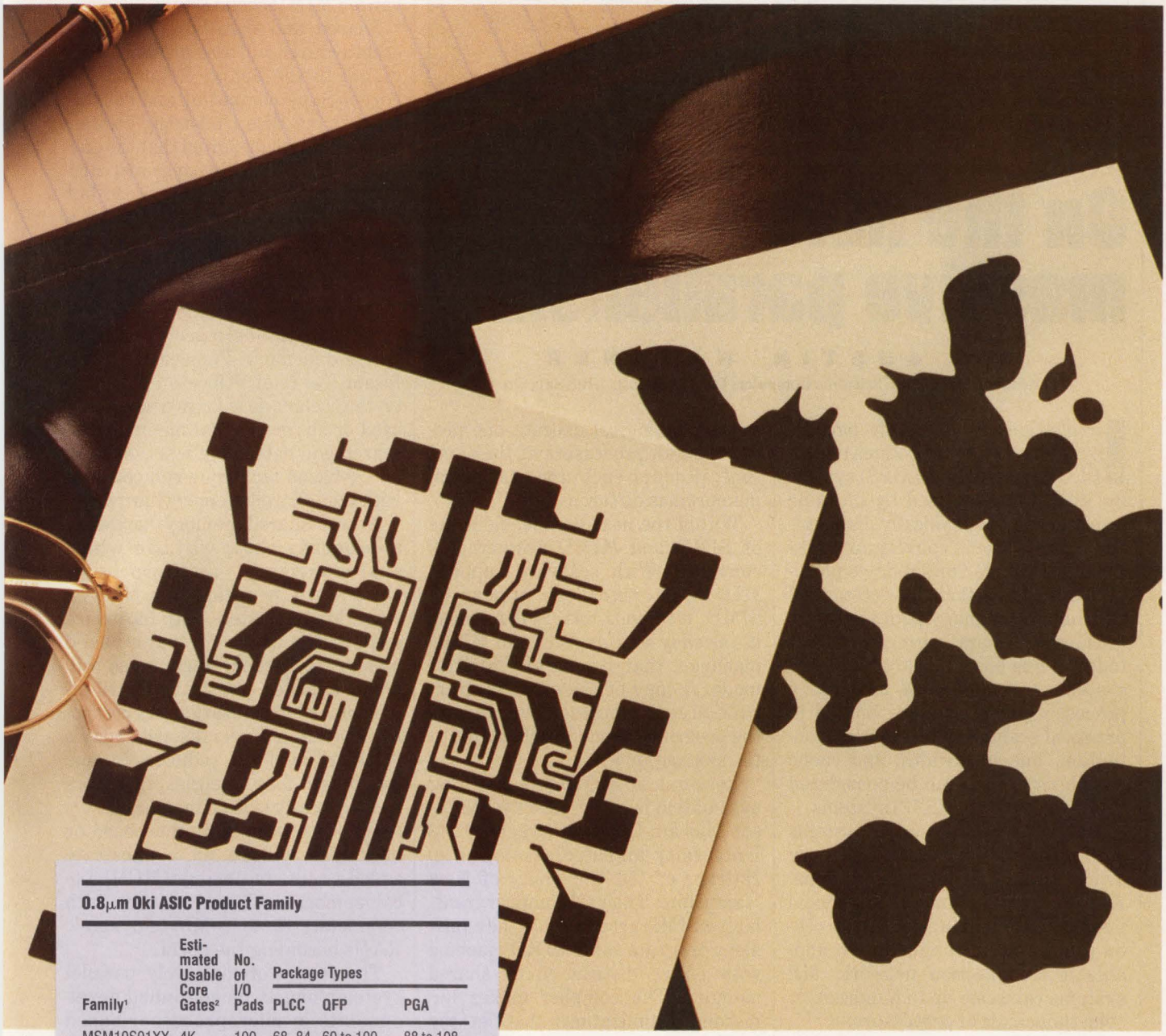

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MSM10S03XX	12K	160	68, 84	80 to 144	88 to 132
MSM10S05XX	22K	208		120 to 208	108 to 208
MSM10S09XX	36K	272		144 to 272*	108 to 256
MSM10S11XX	47K	304		144 to 304*	132 to 301
MSM10S18XX	72K	384		144 to 304*	208 to 340
MSM10S23XX	92K	424		144 to 304*	240 to 340

[1]Other products are under development
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CIRCLE 99

On the following pages, Electronic Design presents an overview on Advanced Computer Technology as seen by experts in six key areas: Massively Parallel Systems, Parallel Compilers, Real-Time Operating Systems, RISC Processor Systems, High-Speed Logic, *and* Multichip Packaging. *The six articles examine present and future aspects of these major technology disciplines.*

On the horizon: massive parallelism

BY JUSTIN RATTNER
Director of Technology, Scientific Computers Div., Intel Corp., Hillsboro, Ore.

Innovations in massively parallel systems may well produce a teraFLOPS (a trillion FLOPS) system by 1995. Characterized by multiple processors with physically distributed memory, such "convergent" systems will evolve from today's parallel systems with their flow-of-control and memory-management models.

There's general agreement that today's bus-based, shared-memory systems, regardless of how many processors they use, are limited in practical scalability by memory-contention, bus bandwidth, and cache complexity. They can be considered small-scale parallel (SSP) systems.

Massively parallel (MP) systems with physically distributed memory evade most scalability limitations. Each microcomputer contains a local memory and communicates with other processors through an expandable interconnection network. MP systems can scale up to hundreds or even thousands of processors.

Today's MP systems are either multiple-instruction multiple-data (MIMD) or single-instruction, multiple-data (SIMD) machines. In MIMD machines (for example, Intel's iPSC/860 and NCube's N-2), each processor executes its own program in concert with other connected processors. Each processor has its own memory with different data. In contrast, SIMD machines (like those of Thinking Machines and Active Memory Technologies) execute one program on all processors at the same time, although each processor's local memory has different data.

Within the next decade, elements of SIMD and MIMD systems will converge. With software support, MIMD machines can appear as SIMD machines. At NASA-Ames, it's already done explicitly for MIMD machines that run in an "SPMD" mode. A copy of the same program runs on each processor, even though the programs aren't synchronized at the instruction level.

Research on SPMD programming automation is being done by Professor Michael Quinn at Oregon State University and Professor Phillip Hatcher of the University of New Hampshire. Their C* compiler translates a SIMD program into the equivalent program for a MIMD machine with either distributed or shared memory. The compiler makes numerous optimizations that let the MIMD machines execute an identical program as efficiently as SIMD.

Hardware features of both types of MP systems are also likely to converge. In Intel's Touchstone Project (a Darpa-sponsored research effort), the company is working with the University of North Carolina to put UNC's Pixel-Planes parallel graphics into an advanced MP system. The rendering processors are based on a SIMD architecture. But the overall Touchstone system for the computationally intensive "Grand Challenges" of science (quantum chronodynamics, human genome studies, global climate change, etc.), is an advanced MIMD architecture.

Shared and distributed memory architectures will also probably converge. In the Spang Robinson Report on Supercomputing and Parallel Processing, Rice University Professor Ken Kennedy stated that the paradigm for all computing will ultimately be distributed memory, but that programming will be on a shared-memory model.

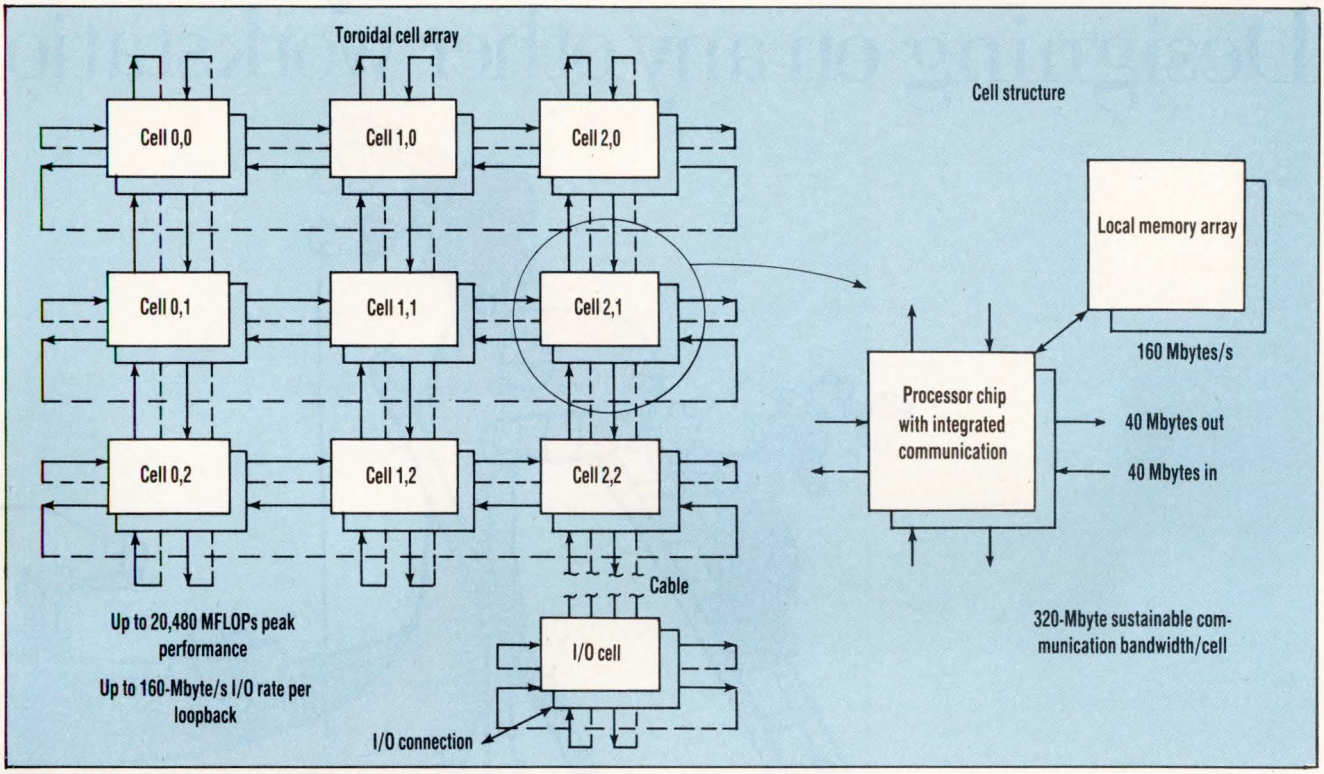
Shared memory is emulated efficiently with the stock i386 MMUs in the processors of Intel's iPSC/2—a large-scale parallel machine with distributed memory. Pioneered by Professor Kai Li of Princeton University, the technique is known as distributed or shared virtual memory. Research will determine whether such an OS-based technique can compete with true shared-memory hardware.

Newer shared-memory hardware approaches show ways in which shared-memory, multiprocessor clusters will be included in MP systems. Many clusters with hardware assists for cache- or page-based memory coherency techniques will create a larger, physically distributed memory organization. As component packaging gets denser, today's "cluster" will be reduced to one board with four to eight processors having locally shared memory.

What's now on a motherboard or backplane will be on a substrate called a multichip module (MCM). Local memories will grow denser, with commodity 16- to 64-Mbyte dynamic RAMs becoming the norm.

The future of massively parallel systems hinges on continued developments in microprocessor-based systems, and will be driven by advances in microprocessors, interconnects schemes, memory management, and software.

At the microprocessor level, chip performance will double every two years. By the year 2000, Intel projects a 50- to 100-million transistor chip with four 750-MIPS, 250-MHz, 1000-MFLOPS CPUs sharing a multimegabyte secondary cache. The number of integer units per proces-



THE iWARP PROJECT FROM INTEL is an example of an enhanced microprocessor for large-scale computing. Configured in a two-dimensional, toriodal mesh, iWarp cells deliver data in a full-duplex mode at 40 Mbytes/s, and in four directions simultaneously.

sor will rise to three or four. At least two pipelined floating-point units per processor are expected, allowing for two 64-bit multiplications and two 64-bit additions in a clock cycle.

Future microprocessors will be enhanced for massively parallel systems. An Intel-Darpa research project, iWARP, offers a glimpse of this trend. Based on the WARP architecture pioneered by H.T. Kung of Carnegie-Mellon University, the project developed component, board, and system prototypes optimized for signal and image processing. These applications are characterized by a high volume of fine-grain computations—1 to 100—on adata element.

At the heart of an iWARP is an experimental microprocessor. The iWARP chip, plus 18 static RAMs, makes up a complete processing node, or cell, for a MIMD MP system. iWARP has extended typical integer and floating-point instructions. Operands can thus flow directly from the processor's high-speed interprocessor communication channels *(see the illustration).*

The iWARP processor is the prototype building block for the parallel-processing desktop and laptop computers expected in the second half of the decade. Such heterogeneous systems will contain a mix of processors, each processor optimized for a specific application, with a common hardware and software communication system. These systems' modularity will enable users to configure, reconfigure, or expand by plugging standard modules into a standard, high-speed interconnect network.

More powerful processors will require networks to tie them together. Electronic interconnects will move to electro-optical and entirely optical networks with interprocessor rates of at least 1 Gbyte/s.

The bases for the aforementioned underlying technologies are already in place. The most difficult area will be software development.

Over the next five years, distributed memory systems will benefit from sophisticated software tools specific to parallel-program development. These include profilers and performance monitors, as well as programming environments like Linda and Strand, which were only recently commercially available.

Although automatic parallelizing compilers seem to be years away, important CASE tools, such as the MIMDizer from Pacific Sierra, offer programmers an interactive environment to develop parallel code.

There is evidence that parallel processing is building the infrastructure it needs for support. In the Spang Robinson report cited earlier, Professor Ted Lewis of Oregon State University stated that "nearly every grant proposal for the National Science Foundation last year included a request for funds to acquire a parallel-processing system."

Recently, Japan's Ministry for International Trade and Industry (MITI) announced a five-year program to put Japan at the forefront of software for massively parallel systems. Within the next five years, such systems will prove that supercomputing is the destiny of the microprocessor.□

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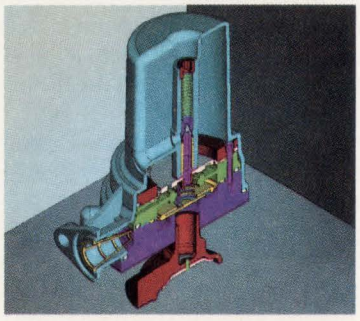

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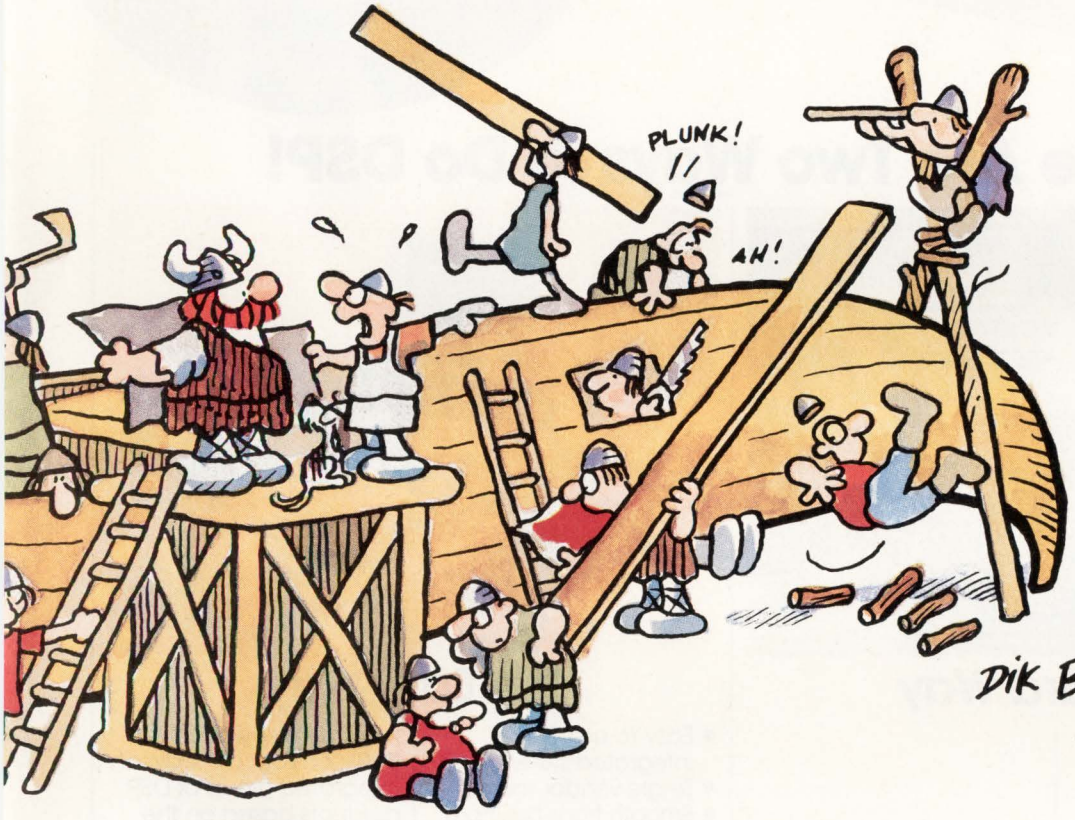

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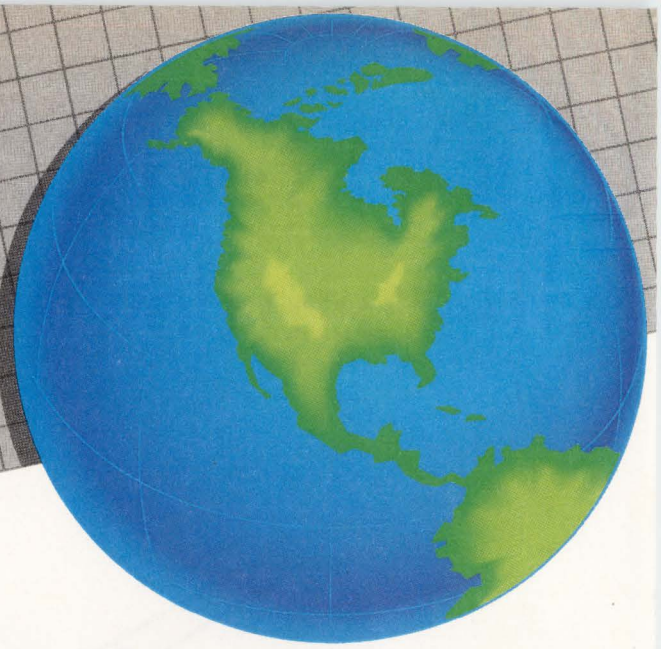

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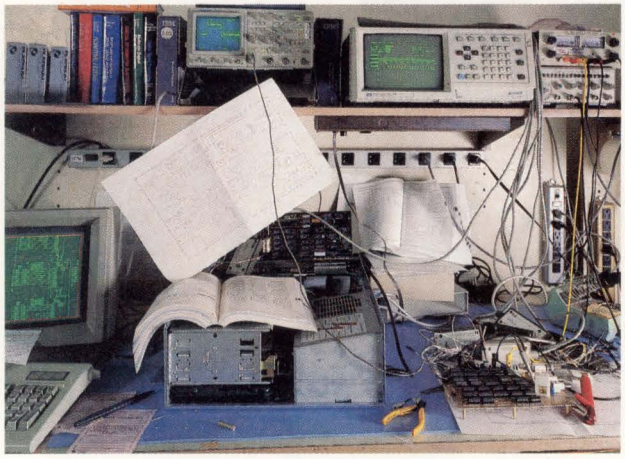

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CIRCLE 118

Parallel compilers: the key to 90s software performance

BY ANDREW F. HALFORD
Vice President of Software Development, Alliant Computer Systems Corp., Littleton, Mass.

Emerging computer architectures present numerous challenges to software developers as they move applications toward higher-performance systems. For example, parallel-processing architectures are being adopted to boost system performance, and RISC processors are speeding instruction execution at the chip level. Consequently, parallel compilers are challenged by increased complexity at both the system and chip level.

Basically, parallel compilers execute instructions faster by interpreting existing code, detecting opportunities for parallelism, and automatically generating code that can be spread over multiple processors. Today's parallel compilers layer parallelizing technology on top of the global optimization developed in the 1970s, and the vectorization perfected in the 1980s, to increase system performance.

Shared-memory, bus-based architectures using CISC chips with vectorization can be accommodated efficiently by today's leading-edge parallel compilers. But the trend toward basing the highest-performance systems on RISC chips, and the characteristics of RISC architectures, present challenges to compiler writers.

To start, it's more difficult to generate efficient code for RISC's smaller instruction set than for CISC designs. As a result, more intelligent compilers are required. Beyond that, vectorization, pipeline management, instruction scheduling, and data migration will be critical compiler concerns over the next few years. Compilers must incorporate vector technology to exploit the superscalar and super-pipelined attributes of RISC chips, and to smooth the execution of multiple instructions at the same time. Pipeline management is important because each missed cycle degrades performance.

Dealing with data dependencies is also more challenging in RISC architectures. With traditional architectures, the compiler's major problem is to find data dependencies within DO loops. The superscalar, super-pipelined attributes of RISC architectures introduce large numbers of varying data dependencies.

To recognize and eliminate these data dependencies, next-generation compilers must consider timing variations encountered with hierarchical memory systems. Data migration is essential because the RISC architecture may incorporate a cache hierarchy, and the system may implement both on- and off-chip memory.

To control data migration in a hierarchical-memory system, the compiler must block the code to take full advantage of the on-chip cache. To obtain top performance, the compiler must keep data and instructions within the pipeline, in on-chip registers, or in on-chip cache.

Timing issues encountered in hierarchical-memory systems, along with the need for nanosecond instruction-execution times, complicate the compiler's job of generating correct code. Tomorrow's parallel compiler must recognize and deal with timing differences when data is located in different levels of the memory hierarchy. It must also resolve timing variations caused by different interconnect speeds between processor and external chips.

Parallel compilers must support concurrency at various levels: instruction, loop, and task. At the instruction level, an accurate machine model, software management of pipelines, and improved instruction scheduling and register allocation must be provided. Improvements must also be made in cache- management facilities. Alliant's compilers are the first to offer loop-level parallelism and RISC vectorization, which is important because each new RISC chip is different. This challenges compiler writers to implement vectorization in a new way while maintaining the paradigm of vectors.

Other obstacles must be overcome at the loop level. Cross-iteration scheduling—the need to schedule an instruction across more than one iteration of a loop—must be introduced to reduce pipeline stalls. Trace scheduling is required to fill and drain the pipeline properly. In addition, sophisticated cache blocking and data-migration management is needed to handle hierarchical memory system considerations, such as on-chip cache, second-level cache, and physical memory.

New code-generation mode-selection capabilities (for example, when floating-point loads superior to pipelined floating-point loads exist—largely a question of cacheability) must be supplied. RISC vectorization requires zero-stall pipelined operations to maximize in-line vector-code generation (using the chip's superscalar/super-pipelined features), and on-chip cache management.

When there are more than 10 processors per system, compilers must find additional opportunities for parallelism. Only when compilers master the complexity of task-level parallelism—decomposing and parallelizing code across the components of an entire program—will optimum performance be gained from applying large numbers of processors to an application. Finding and exploiting task-level parallelism is the next challenge for parallel compilers.

Compilers incorporating interprocedural-analysis technology (now in its infancy) will be essential to achieve task-level parallelization. To perform interprocedural analysis, the compiler must generate and retain information about the entire program so that it can make associa-

PARALLEL COMPILERS

tions between statements in different compilation units. These associations are needed by the compiler to find data dependencies and other obstacles to parallelism. The greatly expanded scope of the analysis results in huge symbol tables and immediate representations. Consequently, managing all of that data becomes extremely complex.

To cope with that complexity, compilers will be required to build a knowledge base from the information they acquire. The size of this knowledge base will call for the compilers to use artificial intelligence techniques to form associations between statements in different compilation units, optimize the code to minimize data migration that may result from using cache or memory hierarchies, and handle different interconnect speeds.

In summary, most compiler work is generated by the nature of new RISC chips, the limited scalability and hierarchical nature of memory systems, and increasing parallelism mixed with the continued importance of converting traditional scalar languages automatically to run concurrently.

As the industry looks to the year 2000, changes will include new architectures, languages, and design tools. New computer architectures will no longer be driven by chip design but by the rate of progress in compiler design. Such architectures as the hypercubes and distributed parallel systems being researched today will push compilers in new directions, but will remain limited in appeal in the 1990s.

Further challenges arise in converting existing serial language designs to take advantage of parallel architectures. New languages are crucial and will be used when developing new applications, but existing Fortran and C applications won't be replaced. Even mainstream ANSI efforts to develop standardized languages, including C++ and Concurrent C, won't compete with Fortran or C in the 1990s.

Instead, industry-backed application-binary-interface (ABI) efforts centered around new microprocessors will move faster and gain quicker acceptance because of economic realities. Moreover, compilers must adapt to emerging, de facto standards, such as PAX and the Intel 860 ABI for technical computing.

As the scope of compilers expands and system complexity increases, compilers also must offer tools to help programmers understand the software architecture. Chip designers have profited from design tools and methodologies, but comparable software tools don't exist.

Compiler people remain stuck using CASE tools that are inadequate for system software development. Meanwhile, parallel systems have made it even more essential for software developers to have a thorough understanding of the software architecture. This knowledge of the architecture is especially critical with RISC chips, for which compilers must rewrite existing code.

Compiler-generated code that takes advantage of task-level parallelism will bear little resemblance to the sequential code it was derived from. Thus, it will be difficult to simply understand what the code is doing. Consequently, compilers will need to provide tools that enable programmers to use the hardware and to better understand the code.

New design tools must supply graphical representations to eliminate the human difficulties in comprehending volumes of data. Design tools must tightly couple architecture representation with both executable and source code, not just source code. The tools also must accommodate performance and system-architecture factors. The only way to guarantee that the executable file, which results from compilation, will reflect the initial design intentions is if the CASE tools are logically connected to the compiler.□

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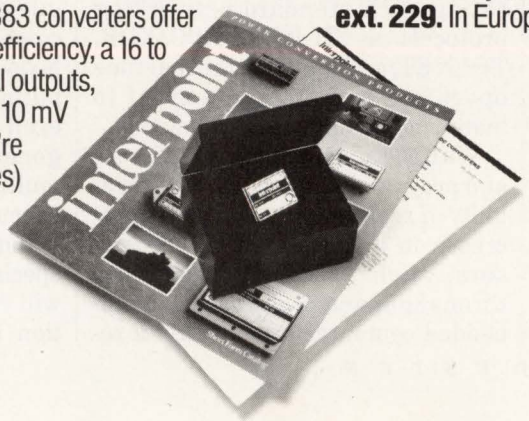

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CIRCLE 138

Advances in real-time operating system technology

BY JAMES READY AND DAVID KALINSKY
Executive Vice President; Software Engineering Technologies Director, Ready Systems Corp., Sunyvale, Calif.

Changes in the next generation of real-time operating system kernels will be driven by modifications in engineering economics resulting from semiconductor advances. Microprocessors are becoming smaller and higher in performance as their prices drop rapidly. These trends will enable real-time operating-system kernel developers to increase the complexity and features in a kernel, such as networking support, without degrading response times of kernel services.

Neither 'fast' nor 'fast enough' pertain to real time when meeting application time constraints in response to an event. What real time refers to is an operating system that must meet rigid time deadlines and must respond to stimuli or physical events within a critical timeframe. An airplane must respond to the stimulus from the pilot's control stick within a specified timeframe to avoid a collision. Too late or too early responses in a real-time system are as incorrect as numeric errors.

Emphasis will thus be placed on determinism or consistency of response time, rather than on efforts to increase raw speed as seen in the past decade. This is a significant change that offers an opportunity to truly address the "timeliness" of real-time program correctness.

Many kernels, such as the VRTX32 of Ready Systems' popular VRTX/OS real-time operating system, are based on a paradigm of run-time priority-based preemption: Each application task (or thread of concurrency) is assigned a priority, which changes only by explicit assignment. Should an event occur during application-software execution that requires certain tasks to be stopped, the kernel will re-evaluate the situation and schedule for the immediate execution of the highest-priority task that's ready. An executing task may be stopped or preempted in mid-execution if a higher-priority task is ready to run.

In the VRTX/OS, the kernel performs task management, intertask communication, and synchronization. Involved in synchronization is mutual exclusion, memory allocation, interrupt servicing, and basic clock and character input/output services. The kernel is application-independent and target-board-independent. VRTX32 has deterministic response—the time consumed by each kernel operation is known through a simple algebraic formula.

Although the operating-system kernel technology is important, the development environment is just as critical. As more workstations become networked into distributed systems, a real-time system is treated as another node on the network for development and production. Hence, real-time kernels now assume the role of mini-operating systems.

Developers of real-time software must be aware of the intimate relationships between the run-time kernel and the real-time application. These interrelationships include meeting system deadlines, exhibiting predictable deterministic performance, providing for task scheduling, and minimizing interrupt off time and interrupt response latency.

Today's kernels must have higher-performance resource-management and networking services. Incorporating such standard networking protocols as TCP/IP, RPC/XDR, TELNET, and NFS into the real-time operating system is essential to match increasing market demands.

With the advent of new processors and programming languages, portability of real-time applications will increase in importance. New processors, such as RISCs, boost the throughput and performance of embedded computer systems. As a result, it's crucial that application developers are given a simple migration path between processors of various technologies.

For example, operating-system kernels should use a standard BIOS interface to ease portability between target processors. To address this critical issue, a standard OBIOS (Open Basic Input Output System) committee has been formed by the leading board and real-time operating system manufacturers to arrive at a standard interface between target hardware and real-time operating systems. The committee, which is open for participation by anyone, is expected to produce a draft standard by the end of this year.

Next-generation kernels must also support multiple programming languages. The same repertoire of intertask communication and synchronization mechanisms should be available to code segments written in various languages. A task coded in C should be able to call for a rendezvous with another task coded in Ada. Similarly, an Ada task should be able to pass information via a high-performance queue to another task in assembly language.

Debuggers will be made available to access all of these target processors and coding languages uniformly. The result will be ease of operating-system development in an exceedingly varied environment.

The necessary hardware and language building blocks will also be combined in future real-time and embedded system applications. Computing requirements will outstrip even the increased power of next-generation processors. Therefore, multiple processors will be needed to execute one application.

Individual processors may have special needs so that applications will run on a heterogeneous collection of hardware. Software tasks

running on the various processors will need to communicate with each other. Thus, processors will be networked or tightly coupled around shared memory and common buses.

Next-generation kernels will deal with this multiplicity and heterogeneity in a way that's transparent to the software developer. Tasks written in different languages running on different platforms will have access to the same operating-system services and to the same repertoire of intertask communication and synchronization mechanisms.

Development and debugging will proceed without concern about processor boundaries and hardware interconnections. Developers will concentrate only on their application tasks and the information-passing mechanisms that tie them together.

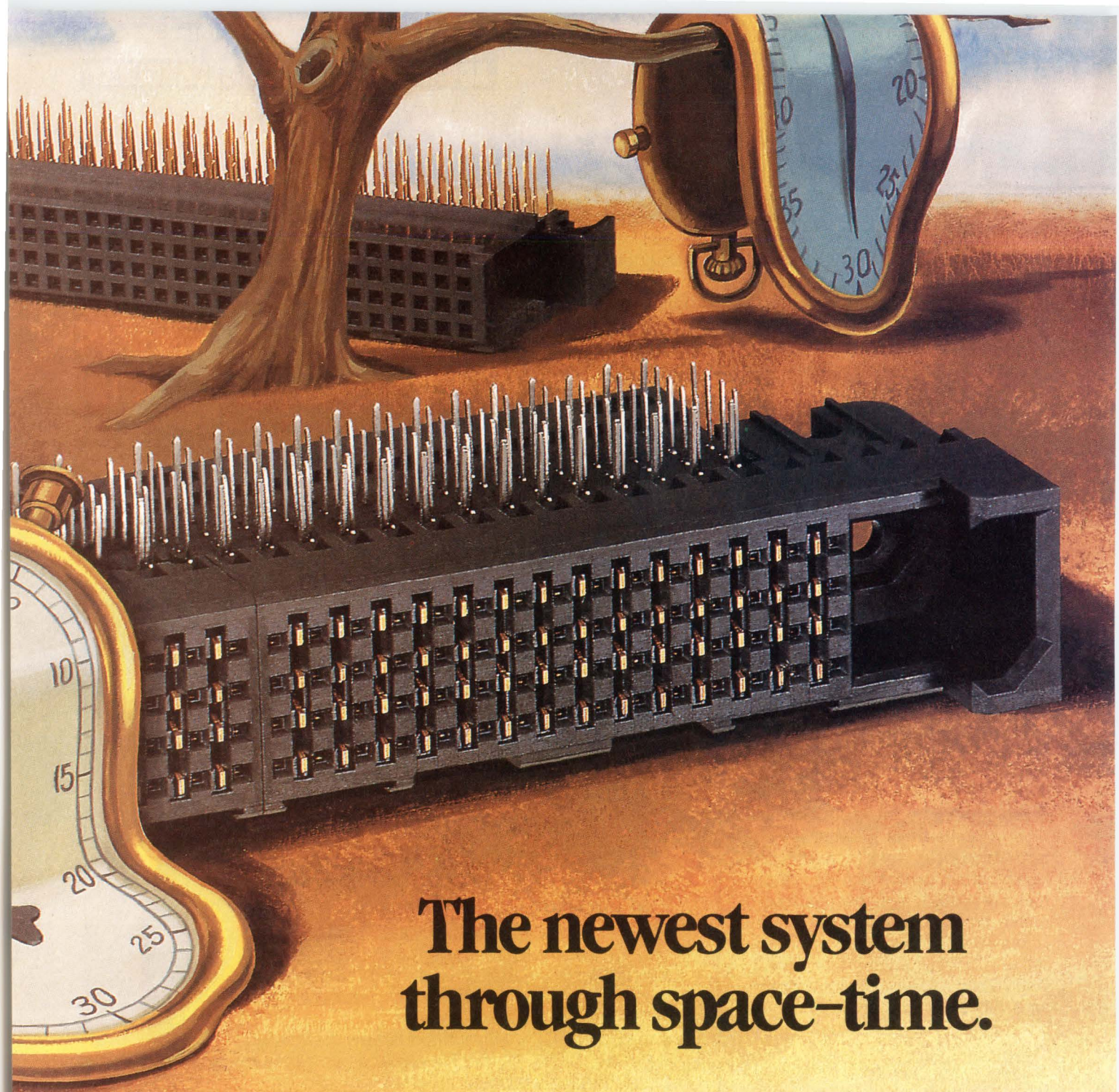
There are cases of so-called "priority inversion" in present-day operating-system kernels and run-time systems. An example can be found in the Ada rendezvous mechanism in a situation where a high-priority and a medium-priority task compete to rendezvous with a low-priority task. Once a rendezvous is achieved, the medium-priority task will execute. On the other hand, the high-priority task's requests will be put into a queue until the medium-priority task is completed. Future operating systems will detect such priority inversions, known as priority inheritance, and will appropriately elevate the blocking activity's priority.

Tightly-coupled multiprocessing can occur on one computer board that contains multiple microprocessors, each with its own memory as well as a central global memory. Alternatively, multiple boards may be tightly coupled through a backplane.

Loosely coupled distributed processing can occur between nodes of single microprocessors or tightly coupled multiprocessors linked into a communication network. Determinism is the key to loosely coupled distributed real-time systems in internode communications, particularly in the presence of faults.

Load balancing, or shifting of tasks from node to node, is pivotal in scheduling tasks in a multiprocessing/distributed system. Future real-time operating system kernels will have load balancing features to ensure that deadlines are met.

In summary, future real-time operating systems must deliver the increased performance, determinism, and reliability demanded in complex distributed systems. Developers must provide operating systems that support multiple programming languages and target processors, and heterogeneous computer systems, transparently to users.□



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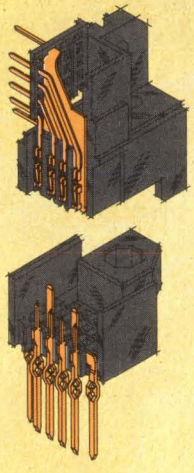

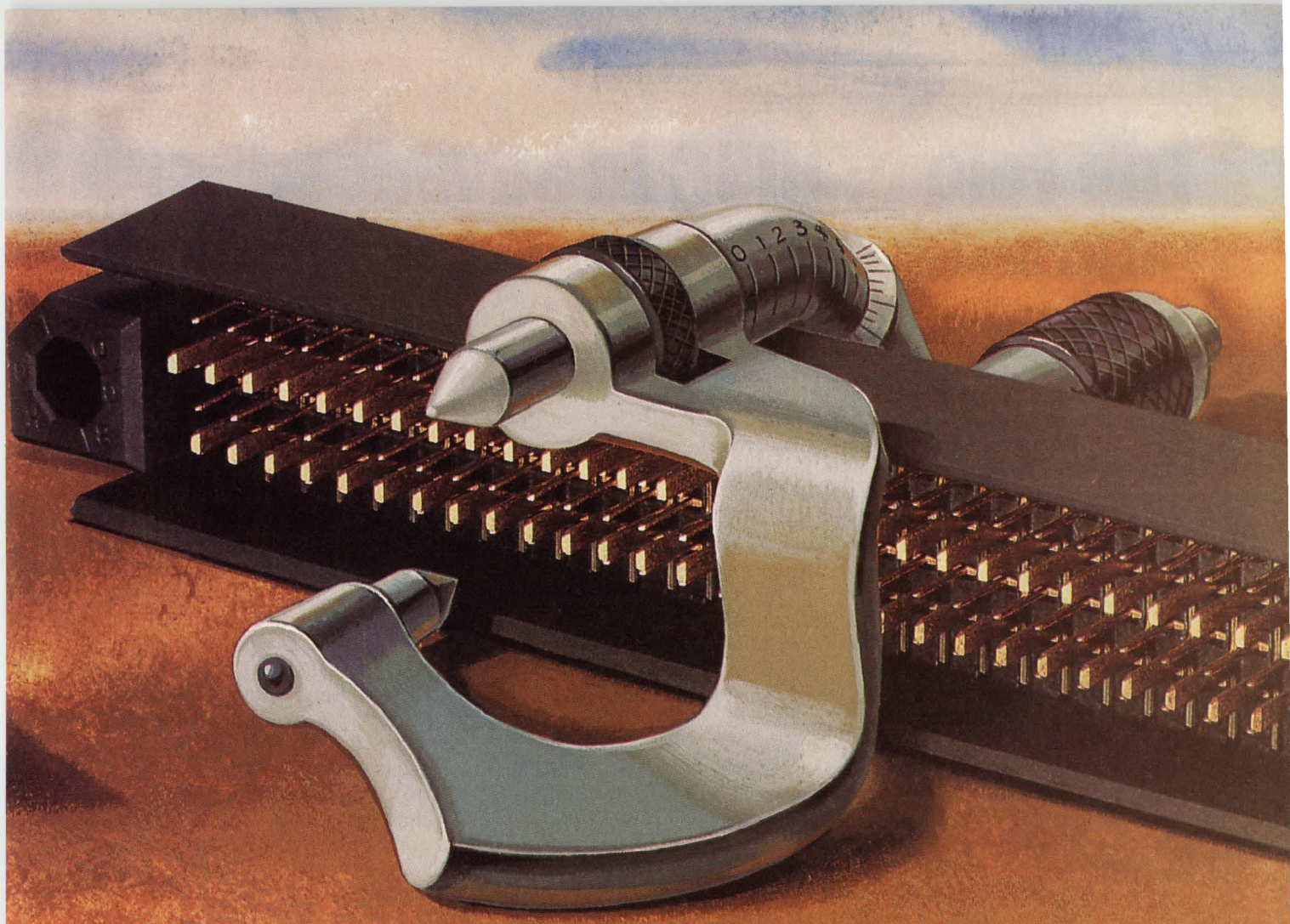

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CIRCLE 122

The role of RISC in advanced computer design

BY DAVID R. DITZEL
Director of Advanced Development, Sun Microsystems Inc., Mountain View, Calif.

A decade has passed since the RISC (reduced-instruction-set computer) versus CISC (complex-instruction-set computer) debate began. But only in the last few years has RISC emerged as the processor architecture of choice for computers with improved performance at a reasonable price. This change has been driven by the commercial availability of RISC chips, such as Sun's Sparc, the MIPS R3000, and the Motorola 88000.

Whether RISC is better than CISC is no longer debated: RISC is here to stay and its success will lead to the decline of most CISC architectures. RISC's simplicity has allowed it to be non-proprietary, encouraging the development of such RISC processor families as Sparc. The competition fostered by multiple implementations is, in turn, accelerating new architectural techniques like superscalar execution, in which more than one instruction is executed for each clock cycle.

Newer semiconductor technologies, such as ECL and GaAs, will be used with RISC first because it requires fewer gates than CISC architectures. Multiprocessor systems will be driven to use RISC to achieve ultimate performance because each RISC processor will be far more powerful than the corresponding CISC available at the time. Finally, because RISC was designed to work with compilers, there will be a trend in which the best compilers will be developed for RISC processors.

Today's leading RISC architectures have some basic similarities. For arithmetic and logical operations, all RISCs address 32 32-bit integer registers at one time. All have 32-bit-long fixed-length instructions and use 32-bit pointers for a 4-Gbyte virtual-address space. And all RISCs use byte addressing of memory and a simple load/store memory model. While most RISCs have delayed branch schemes, Sparc's delayed branch instruction can also be "annulled," meaning that the instruction will be canceled under certain conditions. Annulled branches greatly improve the compiler's ability to schedule instructions. They also avoid the excessively high number of no-op commands that other RISC architectures often execute. Sparc's register windows are also a superset of the final general register model.

Regardless of instruction schemes, six key technologies are critical to the future evolution of advanced computer design: open implementations, new architecture, and semiconductor technologies pin-out standards, multiprocessing, and compilers.

Open Implementation

Sparc isn't just an implementation, but an open architecture definition. By enabling many companies to have their own design approach, Sparc lets each design team add innovation, accelerating the improvement rate in microprocessor design. This strategy of an open architecture fosters a wider variety of Sparc CPUs, giving microprocessor users more choices as well as second-source alternatives.

CISC architectures have typically needed 10 or more clock cycles to execute every instruction. Most RISC processors have come close to executing one instruction every clock cycle—the next generation of RISC processors will execute more than one instruction per clock cycle. This multiple-instruction-per-clock scheme is known as "superscalar" execution.

IBM Corp., for example, uses superscalar execution in its RISC System/6000 workstation, which employs a new CPU architecture. The RS6000/320 achieves 24 MIPS at 20 MHz in a design that's could theoretically execute five instructions at a time. Floating-point performance in superscalar designs can also be impressive because loop overhead can be completely hidden.

LSI Logic's Lightning Sparc processor will also execute up to five instructions per clock cycle for 80 MIPS of sustainable performance. Cypress Semiconductor/Ross Technology is working on a superscalar Sparc design called Pinnacle and Texas Instruments is working on a highly integrated biCMOS superscalar Sparc design.

Most RISC chips today are implemented in CMOS. In the last year, two single-chip ECL RISC processors have appeared. These include the 80-MHz B5000 Sparc processor from Bipolar Integrated Technology and a 60-MHz ECL R6000 processor designed by MIPS Computer Systems using the BIT process. GaAs and biCMOS RISC microprocessors should also appear in the next year or two.

Microprocessor clock rates are determined primarily by the underlying technologies, all of which continue to improve. Over the next two years, CMOS processors should operate at clock rates of 40 to 80 MHz, biCMOS chips at 50 to 100 MHz, ECL at 80 to 150 MHz, and GaAs at 150 to 250 MHz.

Pinout Standards

For years, personal-computer and workstation users have wished that each new generation of microprocessors would be pin-compatible with the previous generation. This would make it possible for users to upgrade their computers simply by replacing the microprocessor. But even within a particular processor architecture controlled by one manufacturer, no two generations of chips have stayed

with a standard pin-out.

Now, however, a common microprocessor pin-out standard is emerging, and manufacturers are planning generations of processors that conform to it. Several semiconductor manufacturers will design Sparc processors to this standard. The common pin-out is a side effect of RISC architectures, specifically Sparc, becoming an open standard. Called the Sparc MBus, this pinout specification was designed with enough bandwidth to accommodate microprocessors for the next three to five years.

The MBus uses a 64-bit transfer operating at a 40-MHz synchronous clock rate to achieve a bandwidth of 320 Mbytes/s. The 40-MHz clock rate was selected as the highest speed at which CMOS chips could operate with a bus of only a few inches on standard PC boards. In addition, the MBus protocols enable the processor to have its own internal cache or even a large second-level cache. Building multiprocessors with MBus-based microprocessors is simple because all of the cache-coherence logic is built into the MBus protocol and associated microprocessor. Multiple chips need only be wired in parallel to build a multiprocessor.

The Cypress/Ross Technology 7C604 Sparc cache controller/MMU and the LSI Logic L64815 Sparc cache controller/MMU are the first chips to appear using the MBus. LSI Logic has announced that its next-generation Lightning Sparc processor will use the same MBus specification. Other Sparc-chip implementations are expected to follow the MBus standard as well.

Multiprocessing

Because processor clock rates are limited at a particular time, other techniques must be used to exceed fundamental device scaling. The approach that promises the most improvement in processing power is the use of multiple processors in one system.

Multiprocessor systems will become the norm rather than the exception. Small numbers of processors may be tied together directly using the MBus. Large numbers of processors (hundreds or thousands) must be tied together using more elaborate interconnection schemes. Most small-scale multiprocessors will use a shared-memory paradigm, but shared memory may not be appropriate for the largest multiprocessor systems.

Compilers

Building the hardware for multiprocessors will be easy, but building the software to make multiprocessors applicable to most of today's programming problems will be exceedingly difficult. It's relatively easy to have an operating system run a different process on each processor. But in order to run one task on multiple processors, the application program must be rewritten. Within the next three to five years, compiler technology will automatically decompose only a small fraction of today's programs to run over multiple processors.

Advanced compilers are commonly associated with RISC technology, although the reasons are often misunderstood. Processor architectures, such as Sparc, were designed with optimizing compilers in mind. Sparc features, including fixed-length instructions, large register sets, register windows, and delayed branches with annulling work well with modern compilers.

CISC machines, on the other hand, often cripple the benefit of optimizing compilers because of their too-small register sets, non-orthogonal instructions, bizarre addressing modes, and the inability to predict the time it will take to execute a series of instructions. It's not that optimizing compilers are essential for RISC: They simply work much better with them.

The future challenge for compiler writers will be to generate code that runs reasonably well on all implementations of the same microprocessor architecture. Superscalar processor architectures will run well with existing code, and optimizations for these processors generally won't hurt performance on today's RISC processors.□

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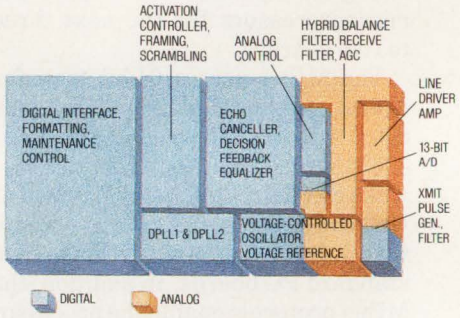

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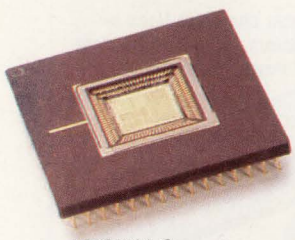
"It has an analog front end for data acquisition, but then we've implemented a powerful self-calibration function in digital. During each conversion, it performs a self-correction cycle, reducing non-linearity errors to less than ±½ LSB."

"So we get 12-bit-plus-sign resolution with an accuracy that's guaranteed over the full mil temp range. Nobody else can do this."

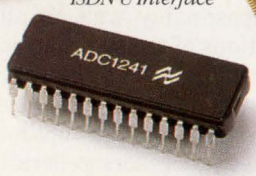

ASIC D/A Converter

ISDN U Interface

Super I/O


Hard Disk Synchronizer/ENDEC

Custom Linear ASICs



A/D Converter

talking about integrating analog we've been doing it for years.

Pushing the limits of PC integration.

"Here again, in our new Super I/O chip, PC87310, we've integrated analog and digital to a level that's never been achieved before."

"Industry-standard floppy-disk controller and UARTs, a parallel port, IDE hard-disk address decode,..."

"With analog PLLs in the floppy controller for pulse detection and data separation."

"All-digital is easier to build, but the performance suffers. And that's not a compromise we're willing to make."

Meeting our customer demand for mixed analog+digital ASICs.

"We call this CLASIC — Custom Linear ASIC. We use standard-cell methodology and optimized process technologies to offer high-performance VLSI solutions combining analog and digital functions."

"The CLASIC library right now has more than 500 analog cells and a good selection of digital building blocks."

"But again, it's not just functions, it's processes. We can fab in the process best suited to your design — linear bipolar, linear CMOS, BiCMOS."

"True customer focus."

continued next page

National Semiconductor

The challenge of integrating analog and digital functions onto the same chip.

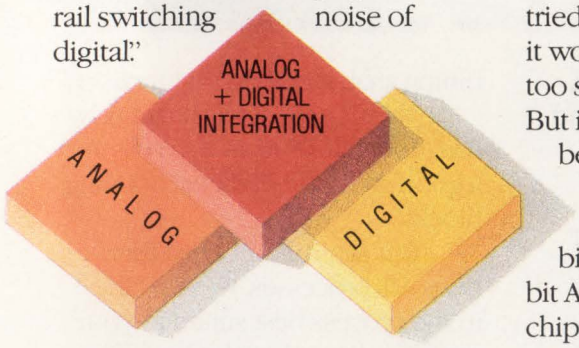
"The demand for mixed analog+ digital really is customer-driven. Our customers need to build systems with higher performance because their customers are demanding it. Because their applications need it."

"And the way to achieve higher levels of performance is through higher levels of integration. Which, at the chip level, ultimately demands that analog and digital functions be pulled together onto the same substrate."

"And this is like trying to merge two incompatible universes."

"Digital's goal is smaller, faster, denser. The world turns on lithography. It lives for the shrink."

"Analog, on the other hand, is concerned with precision, linearity, dynamic range, bandwidth, phase shift, component matching, microvoltage sensitivity. And it simply can't tolerate the clanging rail-to-rail switching noise of digital."



Meeting the challenge with world-class products.

"Our U interface is a perfect example of how difficult this really is. ISDN is digital, but it has to operate over the existing telephone wiring using analog signals. And there's only one twisted pair. So your transmit and receive signals appear on the same terminals. You send 160Kbits/sec digital pulses at 2.5V and it has to travel maybe three or four miles over the subscriber loop without repeaters or amplifiers. Over that distance, you're getting up to 40dB attenuation, so it arrives at about 25 *milli*volts. So the problem is, how do you pick that signal out of all the noise and the local transmit signal, which is 100 times more powerful?"

"You need low power, so if you tried to do it just with analog filters, it would be too complicated and too sensitive to process variations. But if you tried all-digital, it would be too complex to compensate for the limitations of the analog front end. So we combined analog filtering and a 13-bit A-to-D converter onto a single chip with dedicated DSP."

"The point is, we did it."

Meeting the challenge with world-class analog and digital designers.

"Building something like the U-interface transceiver demands some of the most sophisticated design techniques in the world."

"And not only are the individual analog and digital functions difficult to design, but then you have to integrate them onto the same chip."

"So you need world-class digital designers, world-class analog designers, and strategic partners who know how to work together."

"We've got them all. And they've been working on joint designs for many years."

"That's how we do it."

Meeting the challenge with world-class process technologies.

"Another problem for chip designers is that they are limited to the process technologies available to them."

"But, because of our heritage in both analog and digital, we've developed probably the broadest range of process technologies of any company in the industry, including bipolar, CMOS, and BiCMOS."

"We employ a 'core-process' concept. We have six basic core flows, then we add modules for specific functions."

"We can take our advanced M²CMOS core, for example, and add a bipolar module. Or a linear capacitor module. Or EEPROM. Or we can do a bipolar core with a CMOS module. Or we can go to BiCMOS. Or LFAST or LMCMOS or DMOS or JDMOS."

"The key is, our designers have the freedom of selecting the best combination of processes for every analog and digital chip. The application drives the process choice. Not the other way around."

Meeting the challenge with world-class design tools.

"When you try to put analog and digital together, all the existing simulators, place-and-route CAD software, and behavioral models fall apart."

"So we've developed our own. And we're working closely with one of the world's leading CAD-tools companies to create a universal, end-to-end design environment."

"But already our ASIC Division has used our DA4 tools to introduce significant new standard cells, some of which allow high-voltage outputs to be combined with +5V CMOS to 30,000 gate densities."

"So now, for example, you can put logic, RAM, ROM, or EEPROM on the same chip with D-to-A converters and high-voltage drivers."

"No one has ever done this before."

"And it's only the beginning."

Putting the pride of National to work for you.

"The point is, our customers *need* mixed analog+digital capabilities. And we can offer that to them today. We can integrate a complete system solution for them. Or we can work with them at a particular phase in their design. We have the right products, the right processes, the right tools, the right people. And we're putting all of it just a simple phone call away."

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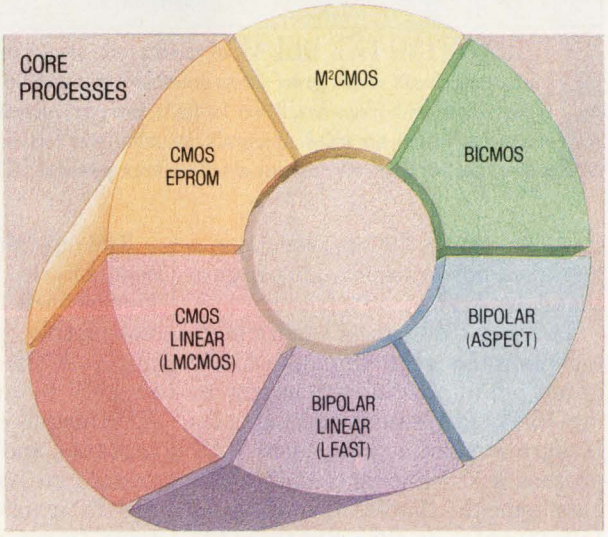


National Semiconductor

The state-of-the-art in high-speed logic for computers

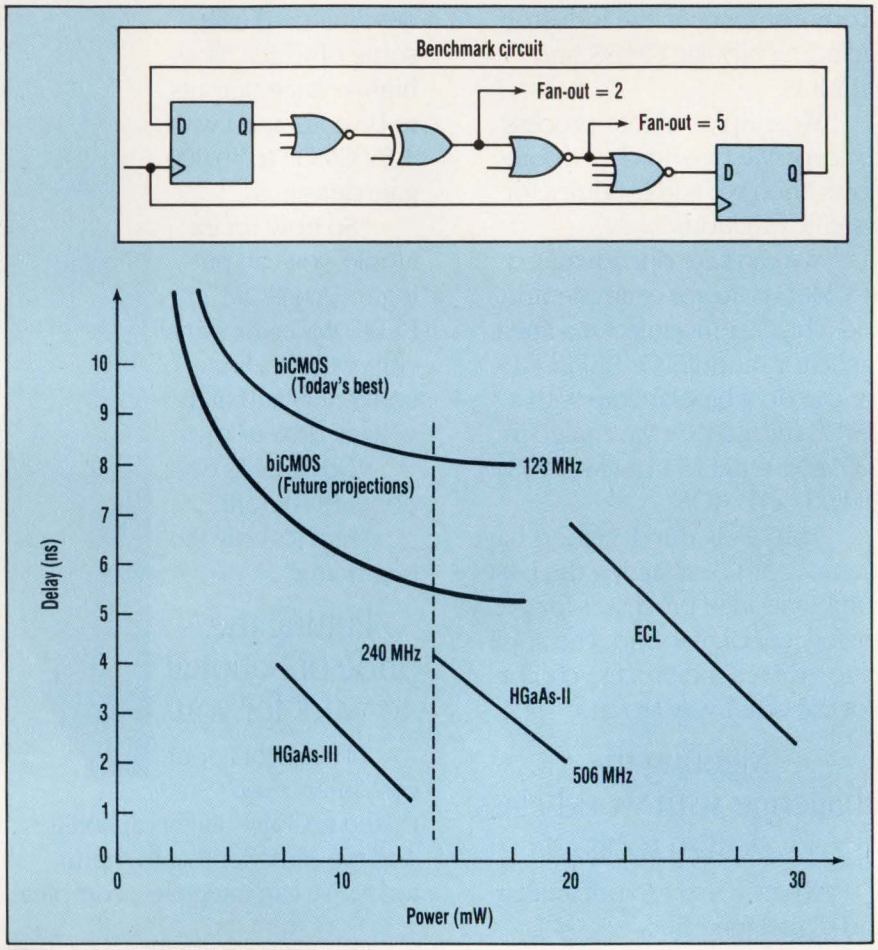
BY THOMAS DUGAN
Director of Marketing, Vitesse Semiconductor Corp., Camarillo, Calif.

High-speed logic is progressing faster than ever with new GaAs and biCMOS technologies that promise to replace ECL in advanced computer systems. This trend is propelled by the additional speed, low power, and high integration that GaAs and biCMOS offer. In 1991, the high integration process approach to GaAs will yield one million transistors. Consequently, GaAs will become enabling technology for integrating full microprocessors, such as Sparc, MIPs, i486, or the 68040. And by the early 1990s, GaAs processors faster than 250 MHz will make desktop supercomputers a reality.

These changes in high-speed logic are redefining the methodology of obtaining high performance in a computer system. No longer can designers simply use the fastest components and expect their systems to reflect this speed.

Consequently, the design of chips and systems as one entity will become routine because of common simulation tools that model the chips and systems at operating speed. However, system designers will have to understand all of the performance issues (integration, power, packaging, etc.) and have an open mind to these evolving technologies.

The technology choices were easy in the past: ECL provided speed and CMOS offered integration. Now, high-end computer-system designers must have both to be competitive. Consequently, ECL is pushing toward higher integration by reducing the power/cell, while CMOS adopted bipolar structures to drive the capacitance of long metal lines. A third technology, GaAs Direct-Coupled FET Logic (DCFL), is the basis of Vitesse's HGaAs process. Like silicon MOS, DCFL has the best speed/power product of the three and will soon reach CMOS integration levels. DCFL also uses current-steering logic, which, combined with its small internal voltage swings, results in a low fixed-power dissipation per gate that doesn't go up with frequency.



1. PLOTTING THE DELAY of various technologies through the given path in the benchmark circuit versus power dissipation shows that biCMOS power increases exponentially with frequency. Power for GaAs, however, increases only where speed-enhancing buffers are added. As a result, an unbuffered version of the Vitesse HGaAs-II process (at 240 MHz) will consume about the same power as biCMOS running at 105 MHz.

ECL has made great strides in integration this year with up to 35,000 gates, but at power levels approaching 50 W. Projections from Bipolar Integration Technology's new P201 process and National's Aspect process indicate that ECL may be at 150,000 gates by 1991. But these are complex processes, requiring as many as 26.

The new Motorola MOSAIC 4 process claims to integrate biCMOS blocks, such as SRAM, with integration levels reaching 54,000 gates (84% usable) in a sea-of-gates approach. By adding CMOS and biCMOS megacells, ECL can increase integration and address the high power-per-gate issue that has plagued its use in mainstream air-cooled systems. In essence, ECL will appear as biCMOS and will cease to exist for VLSI applications. Moreover, the ad-

ditional process complexity will mean higher prices.

BiCMOS has also come on strong this year. Products from Texas Instruments' EPIC-11B process have more than 100,000 raw gates. The key advantage of biCMOS is the speed and drive of its bipolar transistor coupled with the low power and integration levels of CMOS. The oversold power advantage of biCMOS, however, disappears as frequencies increase to 100 MHz or more for complex circuits, in which a significant portion of the gates are toggling *(Fig. 1)*.

GaAs Ramping Up

GaAs is on the fastest learning curve of the three technologies because of its ability to leverage process enhancements and equipment developed for CMOS. As GaAs integration increases, gate lengths will shrink to 0.6 μm—effective with the Vitesse HGaAs-III process—and will yield products with up to 150,000 gates by year's end. This is more than an order of magnitude greater than the predictions made in 1986, which stated that GaAs would reach 10,000 gates by 1990. Future increases in density for GaAs will undoubtedly begin to follow the dictates of Moore's law, doubling every couple of years *(Fig. 2)*.

Over the next two to five years, high-speed logic advances will be just as dramatic as in the past several years. ECL and biCMOS will push toward higher integration because of their reduced gate lengths and emitter sizes. Migration will progress from today's 1-μm gate lengths to 0.5 μm, and possibly to 0.3 μm by 1995. This would result in biCMOS arrays that could reach complexities of 1 million gates.

Furthermore, CMOS will address speeds up to 75 MHz, biCMOS will continue from 75 to 125 MHz, and GaAs will cover applications at 125 MHz and higher. These three FET technologies will dominate the market because of the advantages associated with fabricating FETs.

Integrating megacell logic and memory blocks to eliminate chip crossings will become more critical in order to achieve maximum performance. High-speed SRAM, which is available in GaAs gate arrays and standard cells, will reach 128 kbits in 1991 and 256 kbits by 1993. Logic blocks, such as complete CPUs, floating-point units, and register files, will be possible in GaAs, with integration reaching more than 1 million transistors by 1991. Speed will also improve: Clock frequencies for complex devices, such as CPUs, will hit 200 MHz in 1992 and double to 400 MHz by 1995.

These speeds will be made possible by loaded gate delays of less than 200 ps (54 ps unloaded on HGaAs-III). Enhancements will allow sub-100 ps loaded gate delays by 1992 and sub-75 ps by 1995. Embedded SRAM that doesn't need to cross chip boundaries can be extremely fast. By 1992, today's 3.5-ns cycle times (10-kbit block) will be lowered to 2 ns. By 1995, on-chip RAM blocks of this complexity will approach 1 ns.

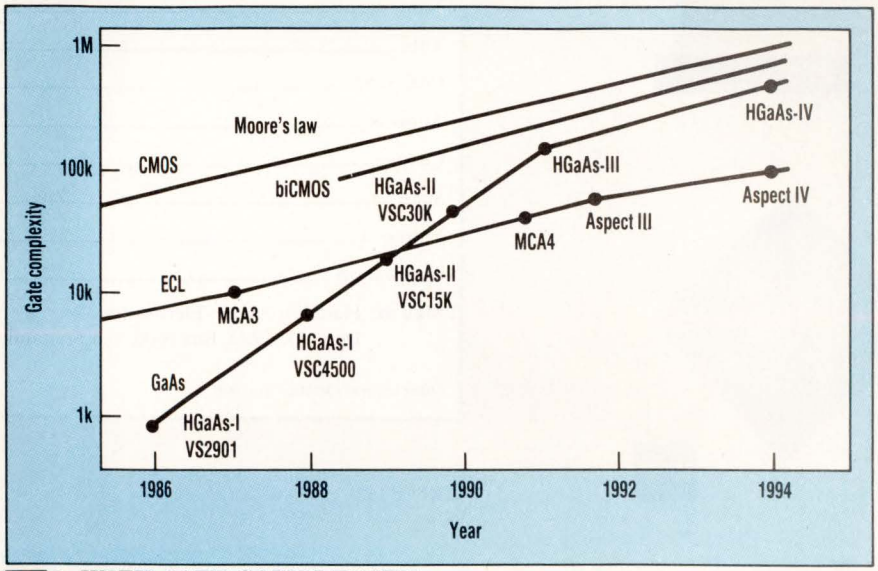
Reducing Dissipation

The key to increasing integration and enabling these large devices to operate in air-cooled systems will be reduced power dissipation per gate. As cell size decreases, the power-per-gate will drop from 0.3 mW/gate to 0.15 mW/gate in 1992, and to 0.05 mW/gate by 1995. Within five years, this reduction in power dissipation, as well as process simplicity, will cause ECL to be replaced by biCMOS and GaAs as the only viable choices for implementing high-performance VLSI logic.

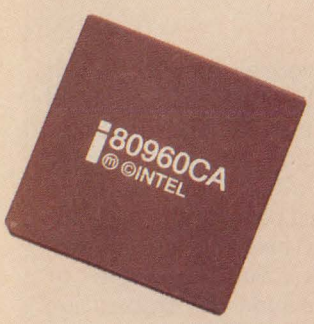
GaAs started penetrating computer systems by breaking speed-critical bottlenecks. Some examples of bottlenecks include the translation look-aside/buffer (TLB), cache control, error detection/correction (EDC), DRAM control, and clock distribution. Today's system designers are working on 40-to-50-MHz processor designs, with support logic around the CPU that must function at twice that frequency. GaAs can offer speed, low power, and a migration path to higher-frequency systems for this 80-100 MHz support logic.

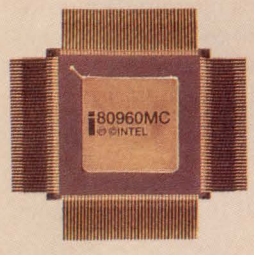
Gazelle's 22V10 and the Vitesse PLR2KT, for example, aim at glue-logic solutions. By using GaAs, such companies as Solbourne (TLB for Sparc) and Convex (EDC) have turned these system bottlenecks into performance features.

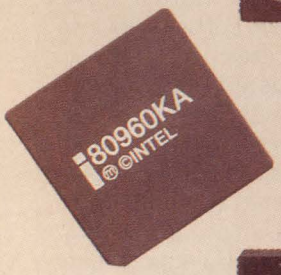
The next obvious step, being taken by some major computer companies, is to build an entire GaAs CPU module running at 200 MHz. These processors are expected to reach up to 170 MIPs while dissipating less than 50 W. By 1994, 300-MHz superscalar architectures running at 270 MIPs should be feasible.□



2. WITH GATE COMPLEXITY spiraling upwards, GaAs ICs will follow Moore's law of doubling in density every two years beginning in about 1991.







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Digital's multichip unit: the performance packaging answer

BY PETER DUNBECK
Consulting Engineer, Digital Equipment Corp., Marlboro, Mass.

Designing high-performance computers involves more than selecting the latest, fastest microprocessor as the central processing unit (CPU). As those devices climb in their MIPS and megaflops ratings, it's increasingly important to minimize off-chip delays in a system so that the CPU speed doesn't dissipate. To deal with that challenge, Digital Equipment Corp. developed a packaging concept that greatly reduces propagation delays. The multichip unit (MCU) technology was first introduced in the VAX 9000 mainframe (ELECTRONIC DESIGN, *Oct. 26, 1989, p. 29)*. The MCU makes it possible for circuit packages to be connected by signal paths that are as short as possible, offering minimum resistance and cutting signal delays.

When Digital planned the VAX 9000, the designers wanted to go beyond simply designing with faster semiconductors; higher-performance systems that offered high reliability was also essential. Those goals required a long-term solution based on leading-edge ECL circuit packaging that would offer a viable base for more powerful systems. The solution came in the MCU, which embodies a major new interconnect technology and builds on advances in semiconductors to overcome the limitations of printed-circuit boards.

Its use has enabled Digital to increase the logic device density by 30 times compared with earlier models, and to reduce propagation delays from approximately 200 ps/in. for conventional pc boards to between 160 and 170 ps/in. Those improvements, coupled with faster logic used in earlier VAX designs, can double computer performance.

MCU Design

With the MCU, Digital can use high-density/high-performance chips operating in close proximity with a chip-interconnect scheme that reduces noise or other interference while maintaining signal integrity between chips. The scheme also makes it possible for efficient extraction of the heat generated by densely-packaged ECL gate arrays.

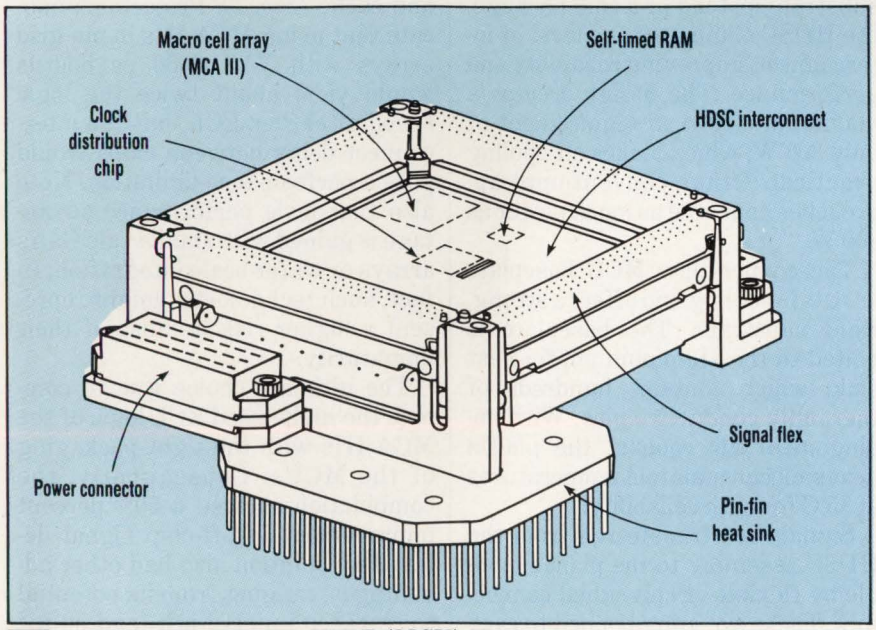
The MCU consists of four main types of components—the logic circuits, signal flex—a flexible circuit signal connector, heat sink, and high-density signal carrier (HDSC), which is a multilayer copper/polyimide interconnect structure. System cost is kept down through good design practices, extensive logic integration, and inherent manufacturability that employs relatively inexpensive materials.

The MCU is the basic building block for VAX high-performance systems *(Fig. 1)*. In the VAX 9000 mainframe, it's used in the CPU, the integrated vector processor, and the system control unit. Within the MCU, fast ICs are connected through the HDSC, which is contained in a housing that also supports the signal and power connections. The HDSC brassplate is then bolted to a pin-fin heat sink to provide cooling.

The primary ICs interconnected through the HDSC are ECL gate arrays called MCA IIIs, and self-timed RAM (STRAM) devices. The MCA IIIs are built according to a Digital design with a density of 10,000 gates, which is eight times greater than the density of the MCA I gate arrays used in the VAX 8800.

Employing such dense chips reduces overall heat output compared with using a larger number of less dense chips. However, denser chips call for an interconnect that can combine more connections per device to minimize connect distances and increase speed.

These demands have been met with the HDSC, a wafer-based interconnect that uses a copper/polyimide substrate to perform functions similar to a pc board. However, the

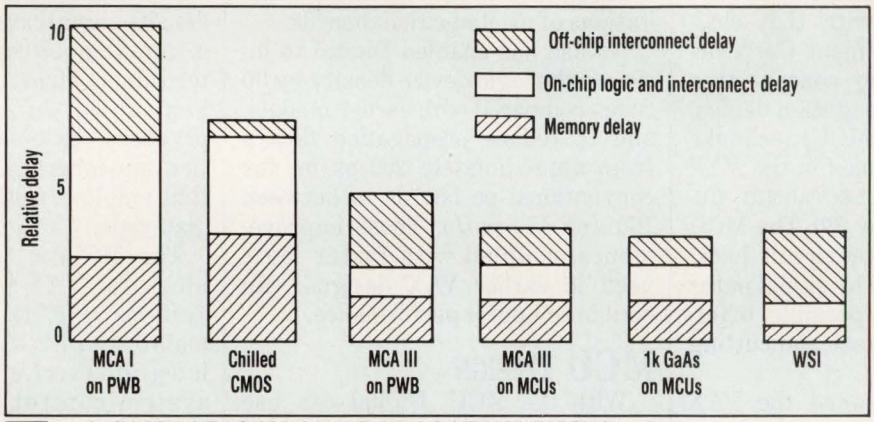


1. THE MULTICHIP UNIT (MCU) HAS a pin-fin heat sink to dissipate heat. In use, the unit is flipped over to allow the signal flex points to mate with an array of contacts on the planar module.

MULTI-CHIP PACKAGING

HDSC layout is three to five times more dense, allowing for more than 600 signal lines per inch. The HDSC represents a density improvement of 30 times from one generation to the next: One 4-by-4-in. HDSC can accommodate as much logic as four 15-by-12-in. pc boards.

Each HDSC is packaged in a housing that mechanically supports signal and power connections, and provides a heat sink that allows air cooling. In addition, the MCU has excellent thermal properties, making it possible to maintain temperatures no higher than 85°C, even with dense ECL circuits. Complete MCUs are mounted and interconnected with others on a special board called the planar module. Several MCUs, each with a different functional design, are integrated into a CPU, vector processor, or system control unit.



2. A COMPARISON OF PROPAGATION TIMES involved in different technologies shows that the MCU with MCA III gate arrays significantly improves speed compared with printed-wiring-board technologies.

The MCU consists of the HDSC and chips, the pin-fin heat sink, connector assemblies, and housing and mounting hardware. The HDSC has nine layers of copper for power and signal distribution interleaved with insulating layers of a polyimide film. The polyimide helps reduce signal propagation delay because it has a low dielectric constant.

The HDSC wafer is constructed one layer at a time. The conductive copper is laid onto a polyimide layer using sputtering and plating. Wafer-alignment stations transfer fine-geometry patterns from a mask onto the copper layer. These patterns mark out the signal paths on photoresist, which are then etched into the copper layer.

The next layer of polyimide is laid over the copper, and vias are cut into the polyimide to form the vertical connections between signal paths in adjacent layers of copper. The signal and power interconnections are made as two separate cores and then are bonded together; plated through-holes connect the two cores.

Finally, lasers cut accurate die sites to accept the various semiconductor devices. Tape-automated bonding is used to gang-bond the signal and power pads from each chip to the HDSC. Chips are epoxied through the laser die cuts to the baseplate, which serves both as a rigid mounting structure and a heat dissipator for the chips.

By bonding chips directly to the substrate instead of a chip package, the HDSC eliminates one level of interconnect, improving reliability and performance. The design creates a maximum electrical requirement of only 300 W, which makes air cooling practical. Other conventional approaches consume as much power as 900 W.

The copper-alloy MCU baseplate assists in cooling and offers a strong, rigid substrate. The baseplate is bolted to the aluminum pin-fin heat sink, which contains hundreds of thermally conductive pins. With impingement air cooling, the pin-fin heat sink can maintain temperatures at 85°C for high reliability.

Signals are transferred from the HDSC assembly to the planar module by flexible-circuit signal connectors. These are gang-bonded to each of the four edges of the HDSC and make contact with the surface of the planar module. Each signal flex has more than 200 signal paths, creating a total of more than 800 for an MCU.

The HDSC's power core is fed by separate power flex cables bonded on two edges of the MCU. The cables mate to high-current-capacity connectors that engage power bus bars to deliver power with minimal resistance. Separating these connector functions prevents undesirable signal-power interaction.

Before embarking on the VAX 9000 design, different semiconductor and packaging technologies were contrasted by measuring performance over a given logic path. The baseline for comparison was VAX 8650 technology, using MCA I gate arrays in pin-grid-array packages on large pc boards.

The summary of results compares propagation times of different technologies through a logic path involving such functional units as the arithmetic logic unit and cache *(Fig. 2)*. Projections indicate that using MCA IIIs in pin-grid arrays with VAX 8650 pc boards would yield about twice the logic speed of earlier ECL, but the interconnect delay between chips would pose a performance limitation. Note also that little performance advantage is gained with small-scale GaAs arrays or wafer-scale integration; In fact, such technologies might represent a higher risk because of their immaturity.

The ultimate choice was to combine the high-speed ECL logic of the MCA IIIs with the tight packaging of the MCUs. Consequently, the combination showed a 50% percent improvement in off-chip signal delay. This solution also had other advantages, ranging from its potential to interconnect high-lead-count VLSI chips with small lead delay to its ability at being a practical-sized field replaceable unit.□

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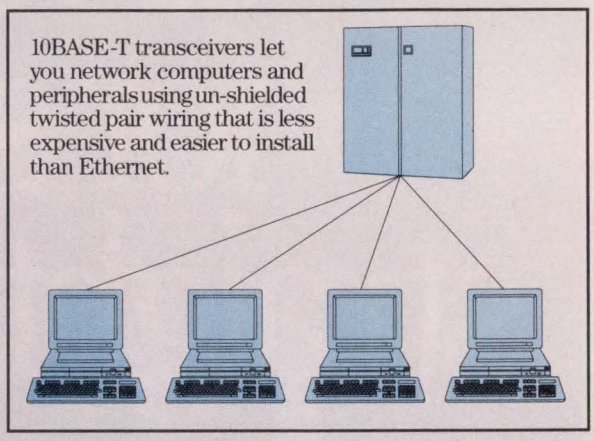

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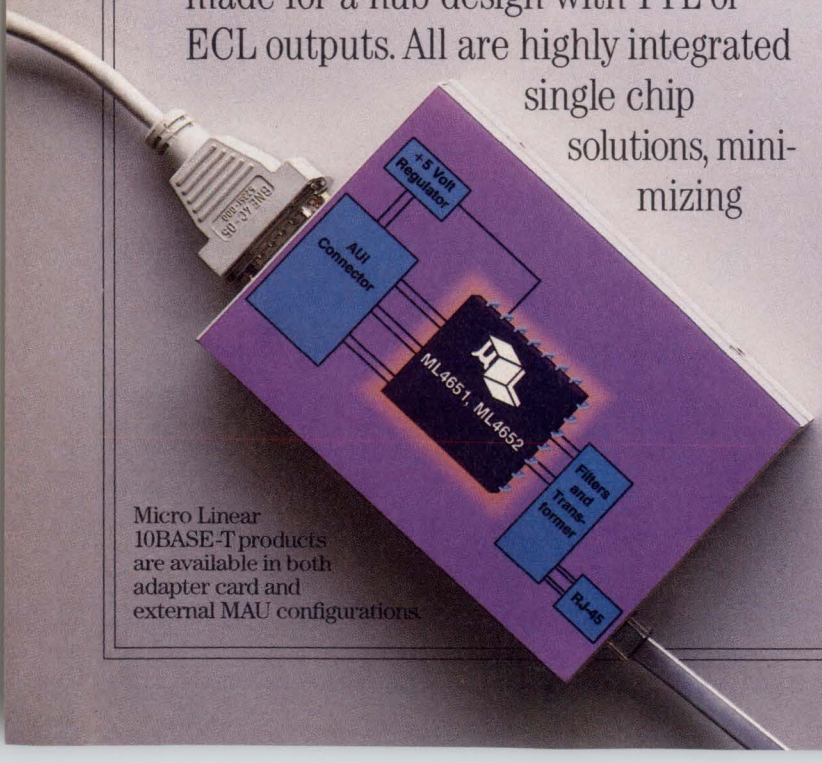

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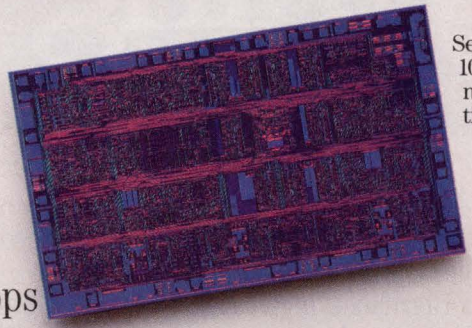

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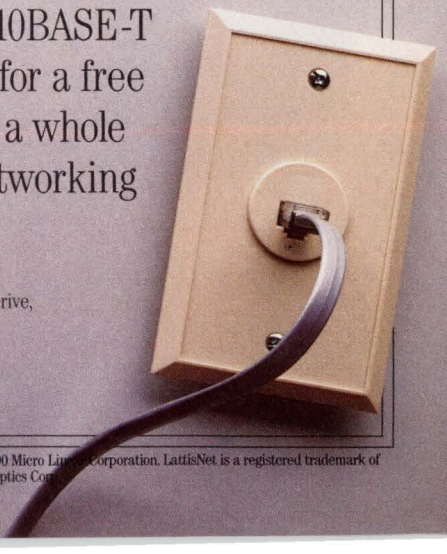

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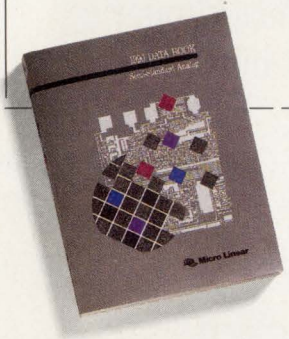

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DESIGN A DSP-BASED SPEECH-TRANSMISSION SYSTEM

SIMULATION ENABLES DESIGNERS TO EXPLORE THE TRADE-OFFS BETWEEN DSP ALGORITHMS AND HARDWARE IMPLEMENTATION WITHOUT BREADBOARD PROTOTYPES.

SOO KWAN EO, CHINGWO MA, AND INCHEOL JANG
Comdisco Systems Inc., 919 East Hillsdale Blvd.,
Foster City, CA 94404; (415) 574-5800.

To transmit low-bit-rate speech over the telephone system requires complex signal-processing hardware and algorithms. At low bit rates, the limitations inherent in telephone channels (such as the effects of linear distortion, noise, carrier- and clock-signal recovery, and phase jitter) can cause errors in the receiver and reduce speech quality.

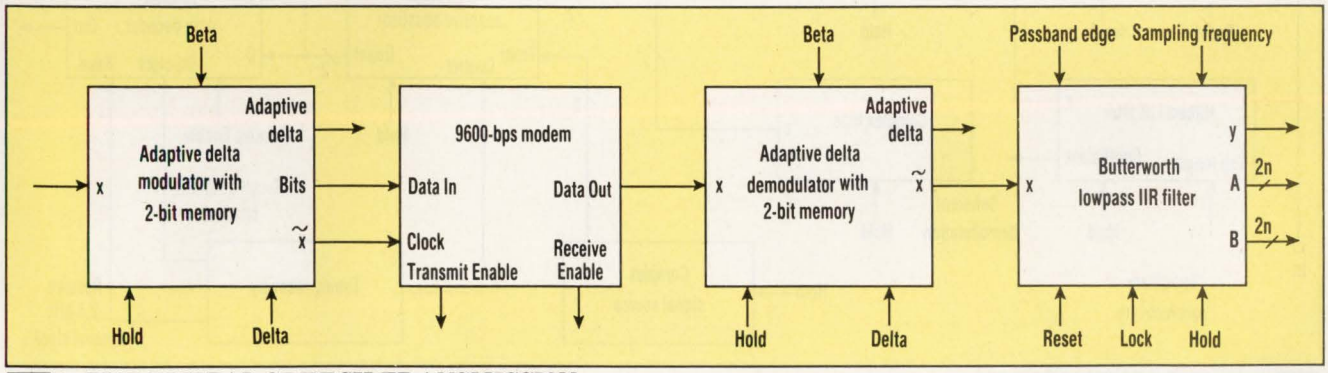
To overcome these unpredictable errors, most receiver functions in a low-transmission-rate modem are performed by a software-controlled digital signal processor. However, modems operate in real time, thus the modem-receiver software's design must compromise between algorithmic complexity and system-performance objectives.

The choice of algorithms affects the hardware implementation. Therefore, experimenting with breadboard prototypes of DSP-based speech-transmission systems is difficult, costly, and time consuming. Designers are limited in the number of trade-off iterations. They need the capability of performing intensive simulations to investigate the trade-offs between various algorithms and system complexity to optimize overall system performance. Comdisco Systems' Signal Processing WorkSystem (SPW) offers this capability.

SPW users can design the algorithms in a signal-flow graph format and, prior to costly implementation, simulate the algorithms with stimulus signals derived from real-world data. Pathways are supplied to step through the design hierarchy from high-level signal-flow description down to actual hardware implementation. The implementation can involve a DSP chip, discrete components, or an ASIC. But designers needn't make that decision until the algorithms are proven.

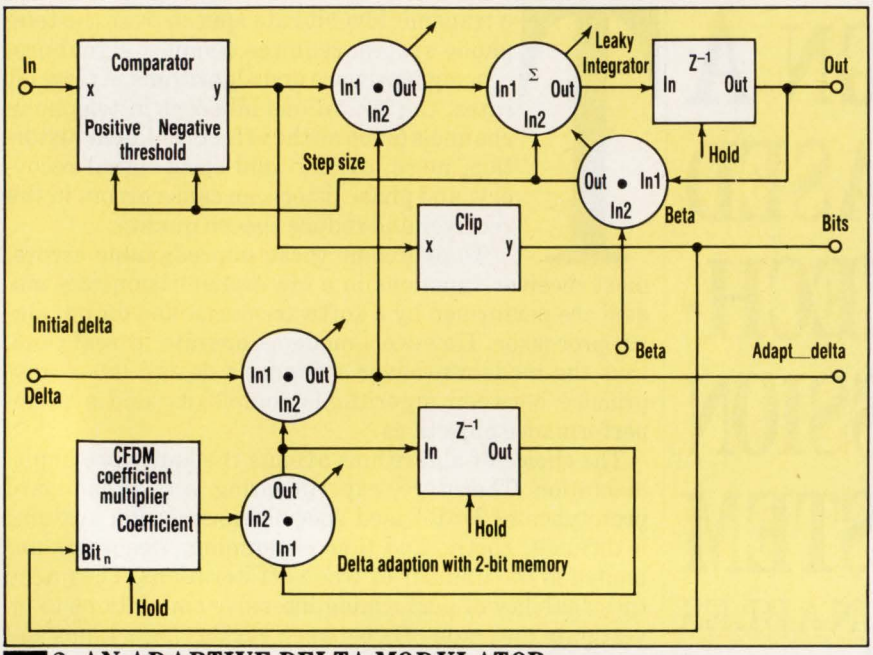
Designing the low-bit-rate digital speech transmission system with the SPW involves capturing speech, source encoding and decoding, signal-flow description using SPW library elements, and modem simulation using real-world data. Besides having an algorithmically proven signal flow, designers are provided with test points and the expected signals. Consequently, when the design is implemented in hardware, it can be verified against the Signal Processing WorkSystem data.

The digital speech-transmission-system architecture



1. THE DIGITAL SPEECH-TRANSMISSION system takes in a digitized speech signal, encodes it, transmits it through a 9600-bps modem, and subjects it to the distortion and phase delay of a 3002/C4-channel telephone line before decoding the signal.

DSP-BASED SPEECH TRANSMISSION



2. AN ADAPTIVE DELTA MODULATOR encodes the instantaneous values of the speech to create digital signals for transmission through the modem.

is best understood by visualizing the source encoding-decoding and the 9600-bps modem separately *(Fig. 1)*. Block names are hierarchical blocks developed within the SPW from communications library functions. An adaptive delta modulator encodes the instantaneous values of the speech waveform for digital transmission through the modem. The 9600-bps modem block contains a 16 quadrature amplitude modulation (16 QAM) receiver with a linear adaptive equalizer (LAE), a model of a 3002/C4-channel telephone line, and a 16-QAM transmitter that produces a modulated, encoded, baseband signal. The LAE's output is the encoded voice signal. To recover the original voice signal, an adaptive delta demodulator decodes the instantaneous values to reproduce the voice signal. This signal is then filtered through a lowpass infinite-impulse-response (IIR) filter.

The modeled voice signal "Mary had a little lamb" was captured at a sampling rate of 8 kHz through a GPIB interface with a Tektronix 11401 digital oscilloscope. This digitized signal was up-sampled to 9.6 kHz using interpolation and decimation filtering, functions that are contained within the source-signal block.

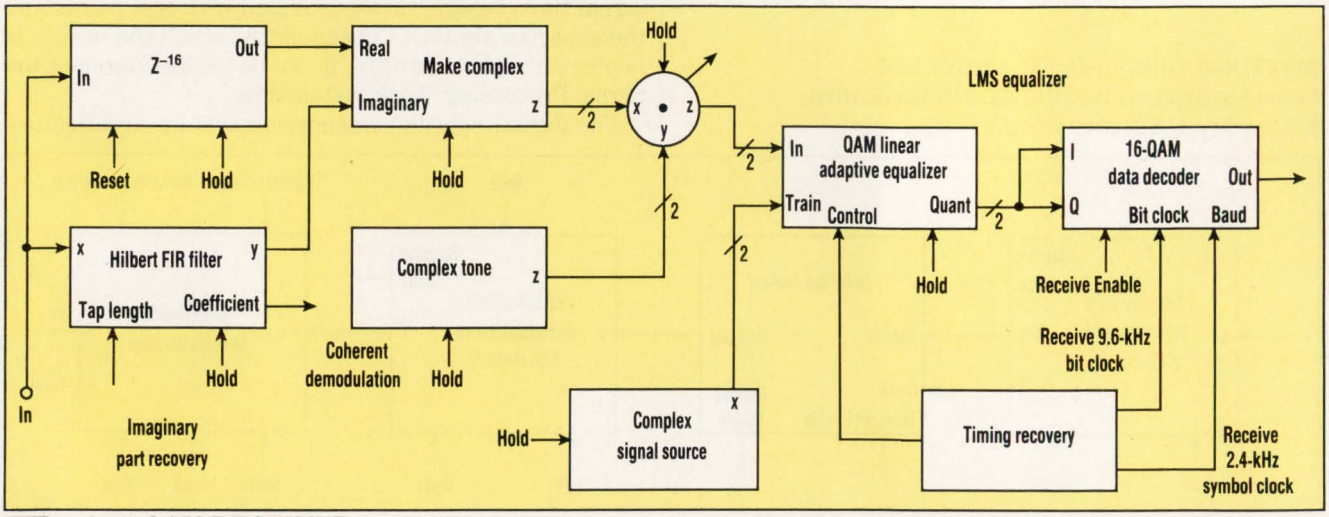
Delta modulation (DM) is a special case of differential pulse-coded modulation (DPCM). Here, the quantizer has only two possible rounded values, resulting in a staircase approximation of the analog waveform. Two kinds of delta-modulation codes exist: a code that represents the instantaneous contents of the speech (short term), and one that represents the content of the speech (long term).

The instantaneous coding is done with constant factor adaptive delta modulation (CFADM). Two-bit memory is used to accommodate the speech dynamics *(Fig. 2)*. In this algorithm, the CFADM is characterized by the equations:

$$b(n) = \mathrm{sgn}[x(n) - B \times y(n-1)]$$
$$y(n) = B \times y(n-1) + D(n) \times b(n)$$

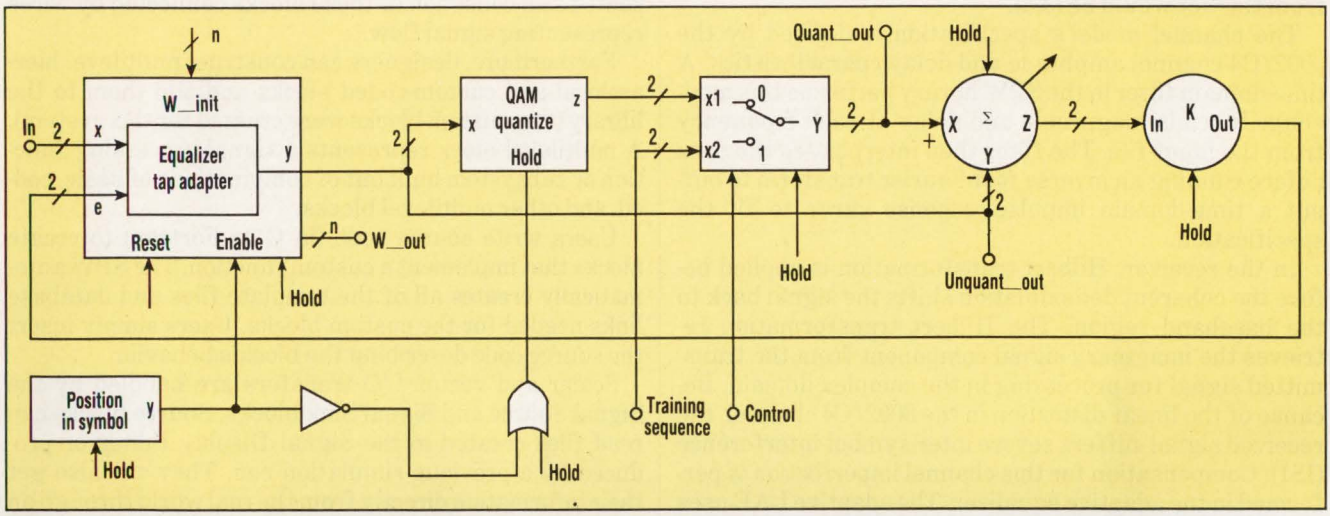
where

n : Discrete time sequence
b(n) : CFADM binary data output at time n
x(n) : CFADM analog input data sampled at time n
y(n – 1) : CFADM analog output data sampled at time n – 1
B : Beta for leaky integration factor



3. A 16-QAM RECEIVER compensates for telephone-channel imperfections automatically with an adaptive equalizer that employs a least-mean-square scheme.

DSP-BASED SPEECH TRANSMISSION



4. THE QAM LINEAR ADAPTIVE EQUALIZER calculates the error signal between the estimated quantized QAM and the unquantized output signal, and then feeds it back to the input to minimize the overall error signal.

y(n) : CFADM analog output data sampled at time n
D(n) : The step size at time n representing the changing slope of waveform

With the 2-bit memory exponential adaptation algorithm, step size is controlled with four multipliers: 2.0, 1.5, 0.9, and 0.4. The multiplier 0.4 provides overshoot suppression after bit change and multiplier 2.0 supplies overload suppression after the channel goes idle. In this algorithm, an increasing slope of input is represented by a digital 1 and a decreasing slope is represented by a 0.

The step size to detect the slope change of an incoming waveform is updated by the equation:

$$D(n) = M(n) \times D(n-1)$$

where: $M(n) = 2.0$ if $b(n) = b(n-1) = b(n-2)$
1.5 if $b(n) = b(n-1)$ and $b(n) \neq b(n-2)$
0.9 if $b(n) \neq b(n-1)$ and $b(n) = b(n-2)$
0.4 if $b(n) \neq b(n-1)$ and $b(n) \neq b(n-2)$.

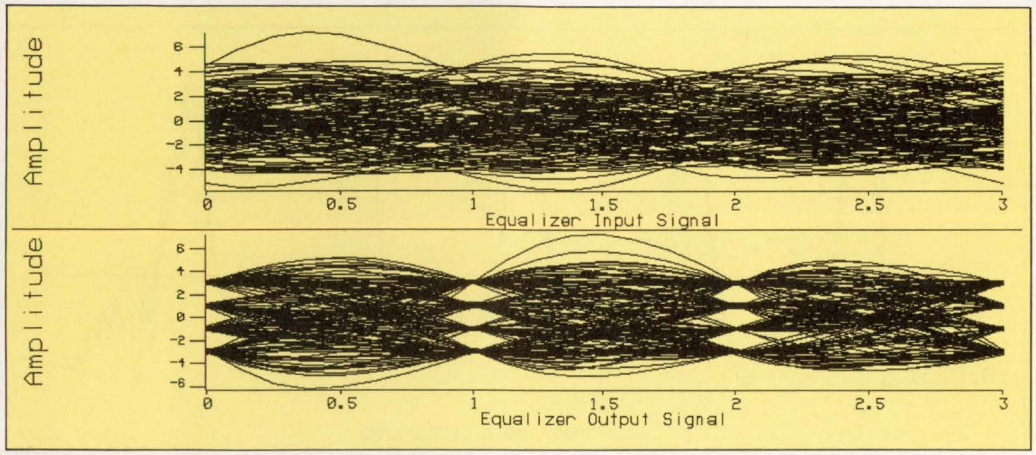
Because D(n) is updated in this fashion, the slope of the input waveform (the gain of the modulator's integrator) is continuously changing. This way, in tracking the analog input waveform, the output slope can transform quickly when changes in the analog input demand it.

The modem receives and transmits 16-QAM modulated signals with a bandwidth of 300 Hz to 3400 Hz. The CCITT V.32 specifications recommend a raised cosine filter with a roll-off factor of 0.1 to accomplish this. The transfer function of this raised cosine filter in the time domain can be represented by the following formula:

$$h(t) = \frac{\sin(\pi \times t/T)}{\pi \times t/T} \times \frac{\cos(\text{beta} \times \pi \times t)}{1-(2 \times \text{beta} \times t/T)^2}$$

T denotes the sampling period and beta denotes the roll-off factor.

The transmitter dispatches the training sequences before sending the real data to the receiver because the linear adaptive equalizer in the receiver requires training sequences to initialize the adaptive equalizer correctly. The training sequence is manipulated by the outmost four symbols from the 16-QAM signal constellation. For example, the first four symbols in the 16-QAM signal constellation are (3,3), (3,1), (1,3), (1,1). Therefore, a training sequence



5. THE RECEIVER-EYE PATTERN shows severe intersymbol-interference from the channel output. This output signal, with its interference, is fed to the adaptive equalizer. The simulation results for the output of the equalizer show a well-opened eye, indicating reduced interference at the sampling points.

DSP-BASED SPEECH TRANSMISSION

from this set would be (3,3).

The channel model's specification is defined by the 3002/C4 channel amplitude and delay characteristics. A time-domain filter in the SPW library performs this modeling. It reads magnitude and delay at each frequency from the input file. The filter then interpolates the data before running an inverse fast Fourier transform to output a time-domain impulse-response curve to fit the specification.

In the receiver, Hilbert transformation is applied before the coherent demodulation shifts the signal back to the baseband region. The Hilbert transformation retrieves the imaginary signal component from the transmitted signal for processing in the complex domain. Because of the linear distortion in the 3002/C4 channel, the received signal suffers severe inter-symbol-interference (ISI). Compensation for this channel imperfection is performed in the adaptive equalizer. The adaptive LAE uses the least-mean-square (LMS) scheme. Once the LAE's tap coefficients are converged using training sequences within several hundred symbol periods (by monitoring the error signal from the LAE), the adaptive LAE's input is switched into the real data line.

After the equalizer clusters receive symbol data into 16-QAM signal symbols on the signal constellation, the QAM decoding block translates the symbols into binary bit streams. These streams are fed into the adaptive delta-demodulation block followed by the lowpass filtering to smooth out the recovered speech signal *(Fig. 3)*.

In this simulation, only the ISI associated with the 3002/C4 channel is considered. The remaining interference, such as symbol and bit-clock phase jitter, aren't considered. The adaptive QAM LAE calculates the error signal between the estimated quantized QAM and the unquantized output signal *(Fig. 4)*. The equalizer then feeds the error portion of the signal back to the input to minimize the error signal.

The entire system was constructed of hierarchical blocks using SPW's Block Diagram Editor. Most of these functions were taken from the SPW communications library that includes DSP kernels, filters, linear and non-linear processing, mathematics, statistics, adaptive filtering, signal input/output, vector manipulation, and control flow. The SPW Communications library offers over 300 communications-oriented function blocks that create, simulate, analyze, and verify communication-system designs. Virtually any signal-processing system can be represented as a collection of these blocks connected by wires representing signal flow.

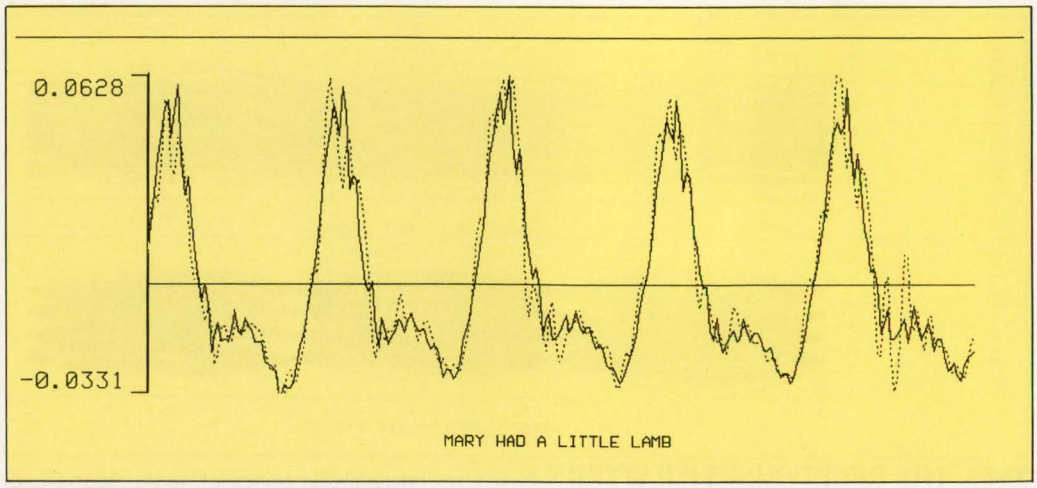
Furthermore, designers can construct multilevel hierarchical and custom-coded blocks and add them to the library (two custom blocks were created for this system). A multilevel block represents a signal-processing function or subsystem built out of combinations of basic, coded, and other multilevel blocks.

Users write source code (in C or Fortran) to create blocks that implement a custom function. The SPW automatically creates all of the template files and database links needed for the custom blocks. Users simply insert the source code describing the block's behavior.

Scalar and vector I/O transfers are handled by the Signal Source and Signal Sink blocks. Source blocks can read files created in the Signal Display Editor or produced by a previous simulation run. They can also get their information directly from the real world through an Instrument Interface Library data-acquisition function block, such as the block that captured "Mary had a little lamb" from the digital oscilloscope. Storage or sink blocks reverse the process and store the output in a user-specified file and format.

The Instrument Interface Library gives the simulated DSP system access to external signals. For specific platforms, with appropriate bus interfaces, the SPW can receive and transmit data and instructions over a GPIB. Special input and output blocks, which can be called by the Block Diagram Editor and integrated into the DSP design, give users complete access to GPIB calls. Designers can use these blocks to set up external instruments, capture a signal in real time, import that signal into SPW, and process that signal.

The SPW automatically converts the signal-flow block diagram from the Block Diagram Editor into an executable program that simulates the behavior of the system. Because the Simulation Program Builder handles feedback, designs can include an unlimited number of multiloops (nested and hierarchical feedback paths). The simulation is built from a sequence of procedure calls, each



6. THIS PLOT ILLUSTRATES the original and recovered speech signals for "Mary had a little lamb." The original and recovered signals are represented by a solid and dotted line, respectively.

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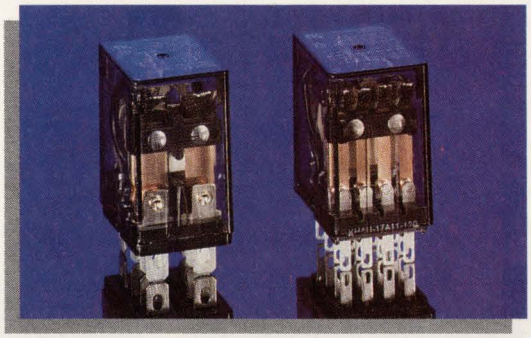

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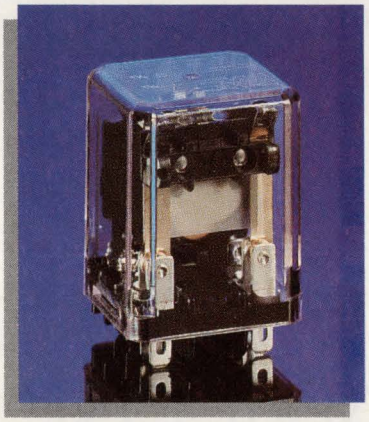

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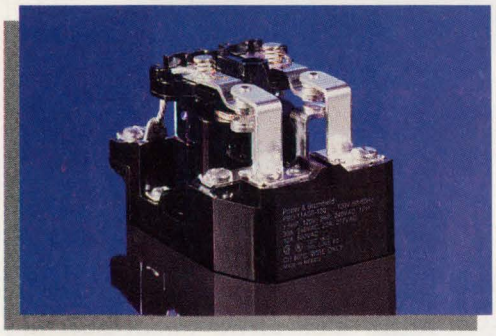

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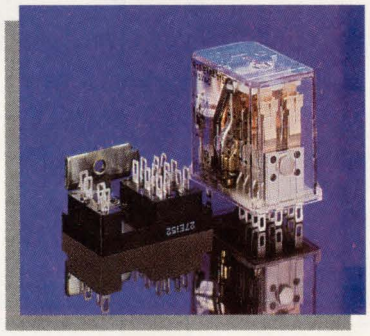

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DSP-BASED SPEECH TRANSMISSION

representing the mathematical operation of a block. The number of blocks in a design is limited only by the size of a user's disk.

The simulation was performed for the 5.8-second speech signal. At a sampling frequency of 9.6 KHz, the signal produced 23,000 data points. To produce as realistic an environment as possible, additive white Gaussian noise with a variance of 0.000005 was added to the input of the adaptive equalizer. This corresponds to a noise level of between 30 Hz and 1 kHz in the speech spectrum, which is approximately 15 dB below the signal level.

The channel-output signal, along with severe intersymbol-interference, is input to the adaptive equalizer *(Fig. 5)*. The simulation results at the output of the equalizer show a well-opened eye, which indicates reduced interference at the sampling points.

In the plot of the original and transmitted signals, the solid line represents the original speech signal *(Fig. 6)*. The dotted line is the signal recovered from the design system. In the simulated system, the overall signal-to-noise ratio (SNR: Quantization error) of the adaptive delta modulator scheme proved to be approximately 6 dB. Modem channel error rates as high as 10^{-3} are acceptable and have no significant effect on the quality of speech. The following table shows the bit error rate of the transmission system:

E_b/N	P_e (with ISI)	P_e (without ISI)
15 dB	1.8×10^{-3}	1.0×10^{-4}
18 dB	3.3×10^{-5}	0

E_b/N :bit energy per noise power spectral density
P_e : error probability
ISI : intersymbol-interference□

Soo Kwan Eo, a project manager at Comdisco Systems, has an MSEE from the University of Arizona, Tucson.

Chingwo Ma, a DSP engineer at Comdisco Systems, has a PhD in electrical engineering from the University of Southern California, Los Angeles.

Incheol Jang, also a DSP engineer at Comdisco Systems, has an MSEE from Stevens Institute of Technology, Hoboken, N.J.

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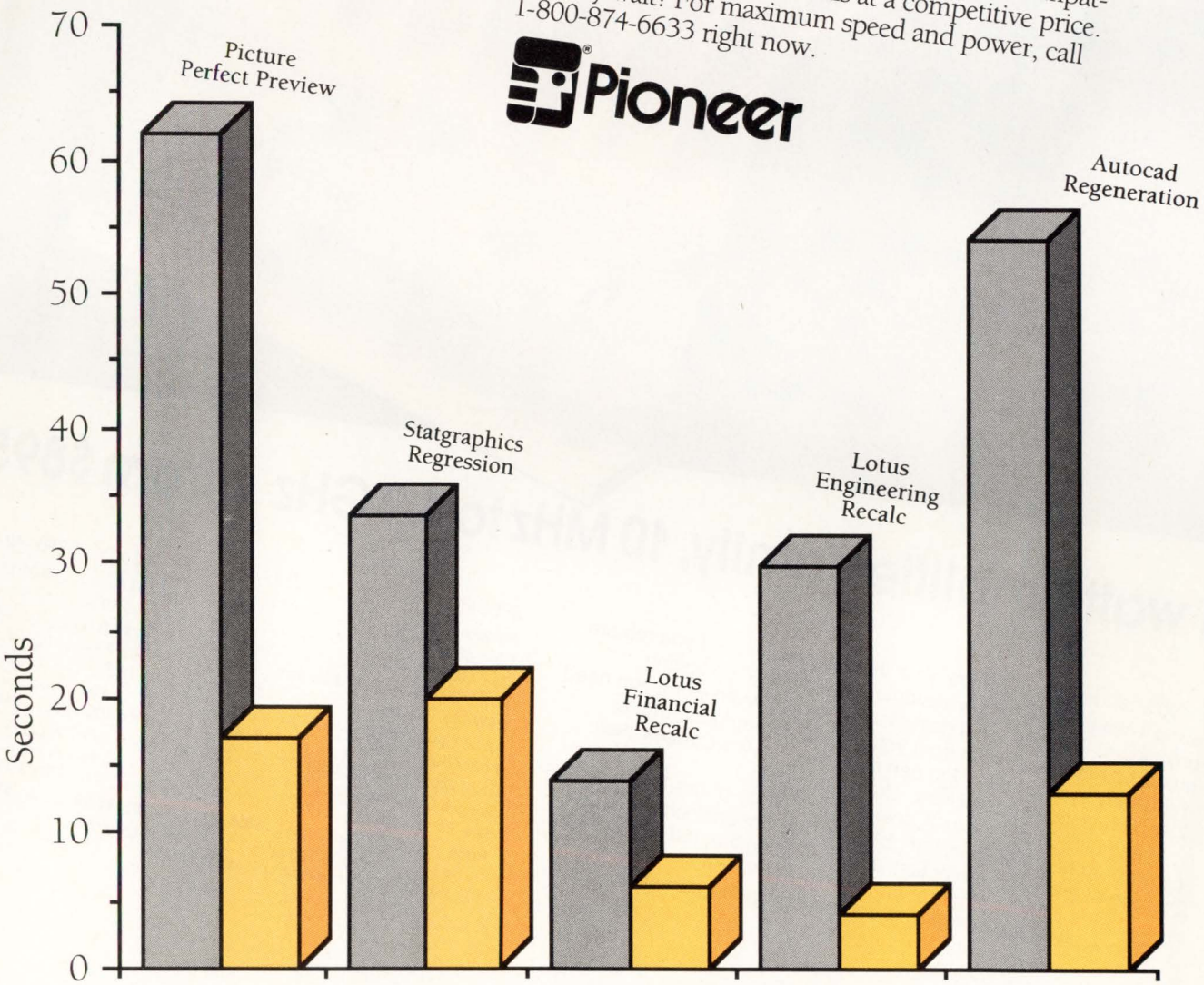

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VSWR In/Out, max.	2.5:1	2.5:1	2.5:1
Noise Figure, dB typ	10.0	4.0	8.0**
Power Supply, V/ma	+15/690	+15/700	+15/750
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CIRCLE 130

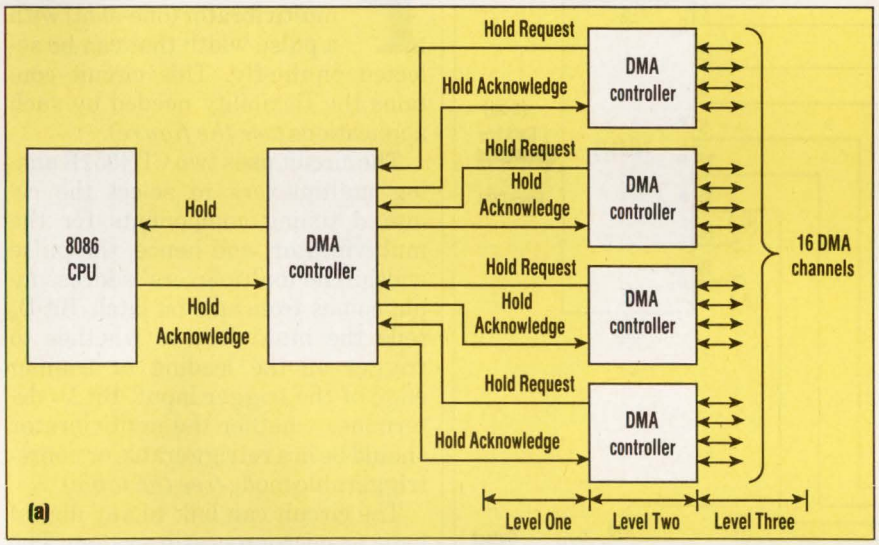
CIRCLE 521

Daisy Chaining Saves A DMA Chip

VITTAL RAO
Isro Satellite Centre, Digital Systems Div., Airport Rd., Vimanapura P.O., Bangalore, India 560 017.

At times, an application will require more than one DMA controller, such as an 8237 and an 8257. The conventional method in this case is to connect additional DMA chips in a one- and two-level configuration *(see the figure, a)*.

An alternate technique is to cascade the DMA controllers *(see the figure, b)*. Linking four DMA controllers in a Daisy-chain configuration saves one DMA chip. The saved chip comes from level one. The order in which the DMA chips are connected determines their priority. The chip furthest to the left has the highest priority, while the right-most chip has the least. There's no constraint as to the number of DMA chips in the chain. Consequently, the technique readily accomodates for future expansion.□



IFD Winners

IFD Winner for April 26, 1990

Kerry Lacanette, National Semiconductor, 2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052. His idea: *"Create an Accurate Noise Generator."*

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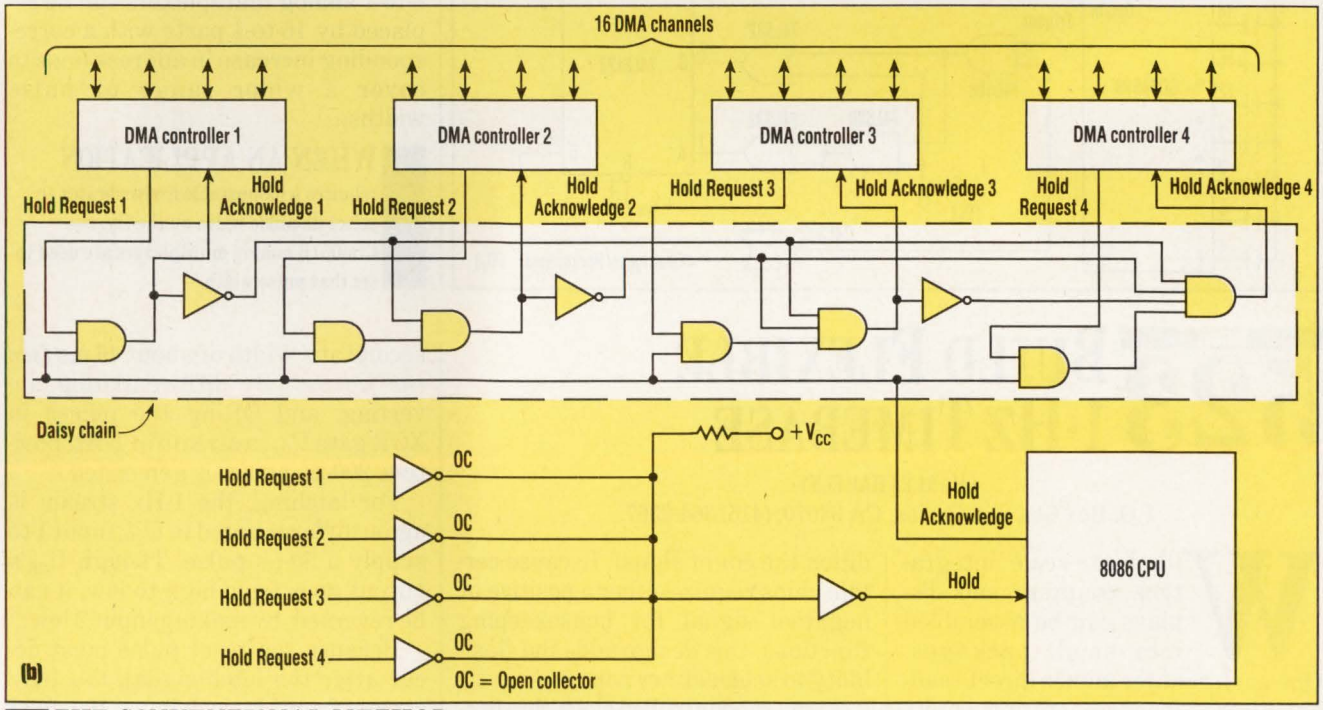

THE CONVENTIONAL METHOD of adding DMA chips is to connect the chips in levels (a). By Daisy chaining the chips, however, one DMA controller can be eliminated. The chips' priority goes from left to right (b).

CIRCLE 522

VERSATILE ONE-SHOT INTERFACES CPU

VITTAL RAO
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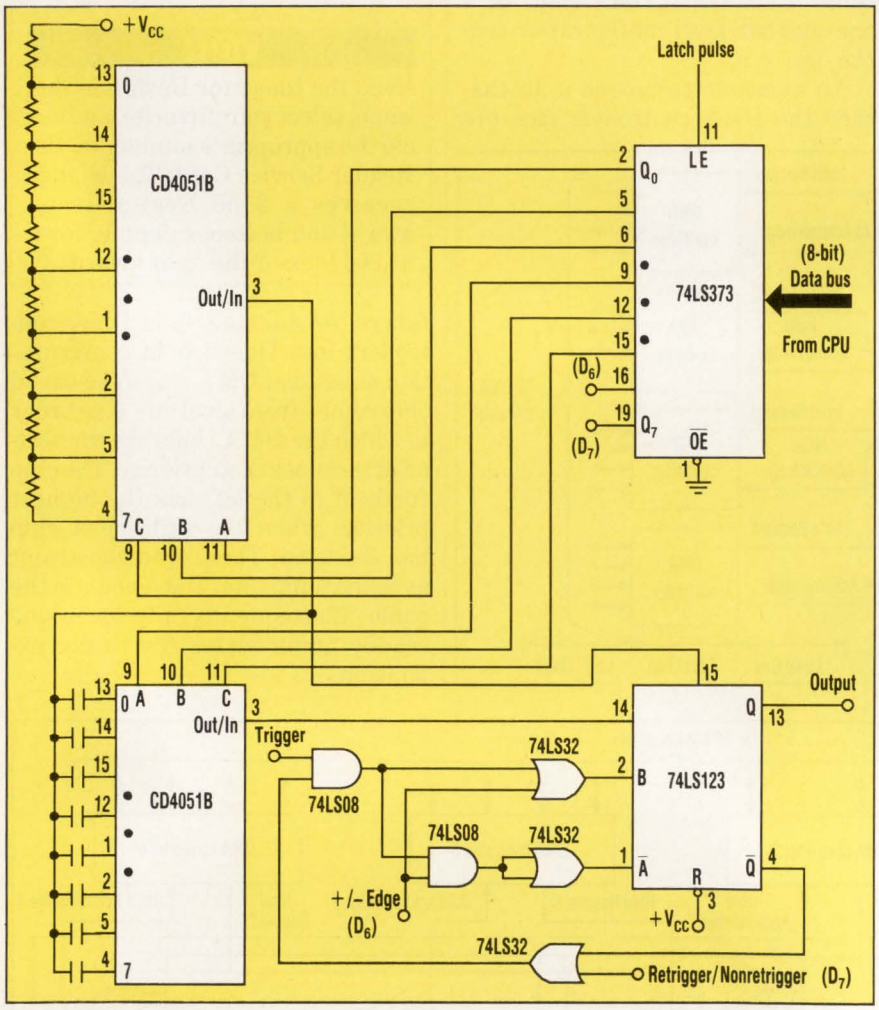


MULTIVIBRATOR TRIGGERING

D_0 D_1 D_2	D_3 D_4 D_5	D_6	D_7
0 0 0 1 1 1 Selects resistors	0 0 0 1 1 1 Selects capacitor	0 1 +VE or –VE edge	0 1 Retriggerable or non-retriggerable

Process-control applications often require a monostable multivibrator (one-shot) with a pulse width that can be selected on-the-fly. This circuit contains the flexibility needed by such applications *(see the figure)*.

The circuit uses two CD4051B analog multiplexers to select the required timing components for the multivibrator, and hence, the pulse width. The multiplexers' address input comes from an 8-bit latch. Bit D_6 tells the multivibrator whether to trigger on the leading or trailing edge of the trigger input. Bit D_7 determines whether the multivibrator should be in a retriggerable or nonretriggerable mode *(see the table)*.

The circuit can link to any digital logic or microprocessor system. The 8-to-1 analog multiplexers can be replaced by 16-to-1 parts with a corresponding increase in address lines to cover a wider range of pulse widths.□

WHEN AN APPLICATION requires a monostable multivibrator to select its pulse width on-the-fly, two CD4051B analog multiplexers are used to set that pulse width.

CIRCLE 523

BUILD FLEXIBLE 1-Hz TIMEBASE

CHARLES HARTLEY
P.O. Box 614, San Carlos, CA 94070; (415) 364-3367.

With large-scale integration, counters and displays can be assembled into small packages. One such counter makes direct readout of frequency-generating equipment very easy when a 1-Hz timebase is added to latch, reset, and condition the count signal. Because certain chips require either a positive or negative signal for housekeeping functions, this design adds the flexibility to select either polarity.

A crystal-controlled clock chip produces separate 2-second high-to-low pulses offset from each other by 1 second at a width of about 46 ms *(see the figure)*. By differentiating, inverting, and ORing the pulses in XOR gate U_{2A}, a stream of 1-Hz, positive, 200-μs pulses is generated.

For latching, the 1-Hz stream is again differentiated in U_{2B}, input 1 to supply a 50-μs pulse. Though U_{2B}'s output goes from high to low, it can be reversed, by making input 2 low.

Because the reset pulse must occur after the latch signal, the 1-Hz stream from U_{2A} is delayed 100 μs at U_{2C}, input 1. The output-pulse polarity is determined by making U_{2C}'s in-

FRAMEWORK MIXES TOOLS TO GET MIXED A/D SIMULATORS

MIX A LOGIC SIMULATOR WITH TWO ANALOG SIMULATORS AND GET A MIXED-SIGNAL TOOL FOR ICS AND A SECOND FOR SYSTEMS.

FRANK GOODENOUGH

As a product's "time-to-market" continues to shrink, the demand for complete simulation of systems—very few of which have no analog functions—grows ever greater. Such systems require accurate and easy-to-use analog-digital simulators.

With that in mind, Cadence Inc. developed two separate mixed-signal simulators simultaneously: Cadence Spice/Verilog for IC design and Saber/Verilog for system, board, and ASIC design. Cadence's Verilog-XL is the digital tool in both simulators. Both simulators are under the aegis of the Cadence Framework and are tightly coupled through a communication system. Each can handle, to some degree, aspects of IC and system design.

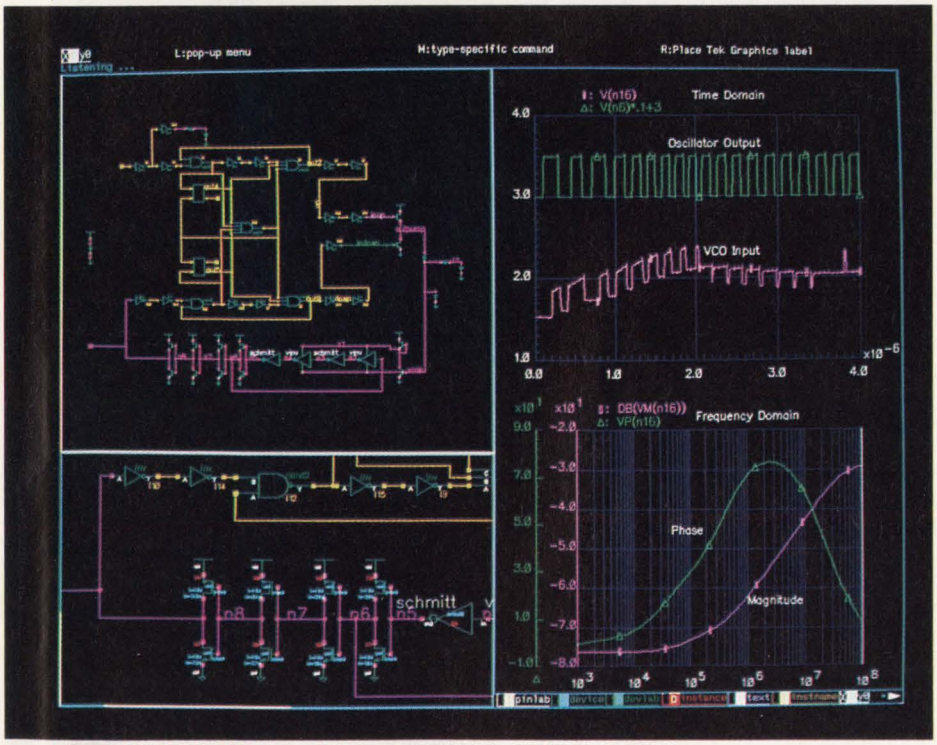
Cadence Spice/Verilog is completely integrated into Cadence's Analog Artist Design System. Saber/Verilog is available as a standalone mixed-signal simulator with other front-ends, in addition to the capture package.

Under the Analog Artist Design System lies "Artist," the analog simulator for mixed-signal IC design. Artist employs either Cadence-Spice—which was developed by Cadence's partner Harris Semiconductor Corp., Melbourne, Fla.—or H-Spice from META Software, Inc., Campbell, Calif.

Cadence-Spice contains macromodels of digital and analog circuits (op amps, flip-flops, comparators, registers), which permit 10 to 100 times faster circuit simulation. Though it's aimed at IC design, Artist can incorporate off-chip active and passive system components (e.g. resistors, capacitors, inductors, and discrete small-signal and power transistors) in the simulation.

Saber, the analog tool of Saber/Verilog, was first announced about five years ago by Analogy Inc., Beaverton, Ore. Saber and the variety of available Spice species dominate analog simulation. Saber/Verilog has access to a library of over 3000 standard analog parts, and over 9000 digital devices. Nonetheless, it's right at home aiding IC design, particularly that of mixed-signal ASICs. In fact, embedded within Saber is what Analogy calls "native" mixed-mode simulation with its own event queue.

The high degree of hierarchy of Artist, Saber, and Verilog-XL, the



INTEGRATED MIXED-SIGNAL SIMULATION is now possible with the Analog Artist system from Cadence. A phase-locked loop (upper left) with its analog and digital nets highlighted (lower left), has its time and frequency responses plotted (right).

principle tools behind Cadence Spice/Verilog and Saber/Verilog, permit bottom-up and top-down designs. The tool designers at Analogy and Cadence decided they wanted their customers, whether analog- or digital-system designers, to feel as comfortable as possible with the mixed-signal tools. Therefore, they were given two choices: they can capture their designs either in a typical schematic-entry system or they can do so with a Hardware Description Language (HDL).

Both Artist and Saber also have a high-level modeling language that allows circuit blocks to be defined by an equation or transfer function. In fact, Saber is already famous for its "mixed-technology simulation." Its modeling language, MAST, makes it possible to simulate non-electrical/electronic models, such as motors, chemical and thermal reactions, and optical phenomena. Moreover, Verilog-XL offers access to the de facto, standard, Verilog HDL. It can capture and simulate an HDL at the switch, gate, register, behavioral, or stochastic level. Capture and simulation control is either textual or from a menu.

Cadence-Spice, an improved Spice derivative, offers full-circuit interactivity, new convergence algorithms for accuracy and reliability. It also has a complete suite of popular semiconductor Spice models.

Tightly Coupled Feedback

Handling tightly coupled feedback from analog to digital blocks and vice versa represents a major test for mixed-signal simulators. Simulating phase-locked loops, for example, is a good indication of the capabilities of Cadence Spice/Verilog and Saber/Verilog *(see the figure)*. Though the results in the figure came from a Saber/Verilog simulation, similar results can be obtained for the same circuit from an Analog Artist simulation.

The example also illustrates the hierarchical nature of the captured circuit. The captured circuit consists of a phase detector, a charge pump, a voltage-controlled oscillator (VCO), a Schmitt trigger, and a 4:1 divider. The phase detector and the divider employ digital models in Verilog; the other three blocks are analog models in Saber. The phase detector uses gate-level models and the divider employs Verilog behavioral-level models. The charge-pump uses discrete-transistor, -resistor, and -capacitor models. On the other hand, the VCO and Schmitt models are Saber (MAST) behavioral.

Analog Artist mixed-signal simulation with Cadence Spice/Verilog is more integrated than its system-design cohort. The circuit is captured naturally and intuitively with primitive symbols from the Verilog-XL and Cadence-Spice libraries. There's no need to insert special interface devices between the analog and digital sections (these "hooks" are already in place).

Moreover, the hooks include feedback connections. Alternatively, the design can be captured hierarchically, with complete freedom provided for mixing analog and digital blocks at any level (in the schematic hierarchy), including Verilog-XL behavioral models.

As each block is given analog or digital properties, it's denoted as an analog or digital device, and its symbol and circuit nodes can be drawn in different colors on the schematic. At any time during a simulation, a block can be stopped and its properties or hierarchical level can be changed. The simulation can also be restarted at the time it was stopped. A portion of a digital circuit—for example, an expected critical timing-path—can be converted to a circuit model and simulated at the transistor level in Cadence Spice.

When the simulation is complete and the results are satisfactory, the IC-layout tool can be pulled up. If the results are unacceptable, Analog Artist's Optimization tool can be brought up instead of doing a number of iterative circuit changes followed by simulations. The tools can help improve circuit models with data from laboratory measurements.

The tools can also help optimize circuit values to meet a desired circuit response (for example, reaching some desired combination of gain and bandwidth or response time). That includes optimizing the delay through a number of digital gates to minimize time-skew between parallel paths (for example, the drive circuits for a video digital-to-analog converter).

Place And Route

With Artist's mixed-signal place-and-route tool, a chip can be laid out in a completely interactive mode and the tool can do all of the detail work automatically. Like the simulator product, the tool is hierarchical, making it possible for top-down and bottom-up design.

At any given time, the layout's parasitic capacitances can be extracted and back-annotated to the schematic. Users can also perform one or more new simulations. Extracted capacitances include those from path to ground, those between paths that cross, those between parallel paths of the same layer, and those between parallel paths on different layers. The place-and-route tool includes special power-bus routing to ensure that remote sections of physically large IC chips get the voltage levels required.

To minimize noise and crosstalk problems, special routing is available on the mixed-signal place-and-route tool for analog circuits. The routing permits designers to have greater spacing between critical lines. In addition, it allows shield blocks and/or nets of analog circuits to be isolated.□

Price And Availabilty

The Analog Artist Mixed-Signal Simulation Interface is priced at $10,000 per license. It requires the Analog Artist Design System, which includes Cadence Spice. Single-quantity pricing for the system starts at $30,000 per seat, while the Verilog-XL simulator runs $25,000 per seat. Both are available for Sun, Apollo and DEC workstations. The Saber interface starts at $10,000 per seat; Saber starts at $15,000 per seat.

CIRCLE 511

How Valuable?	Circle
Highly	544
Moderately	545
Slightly	546

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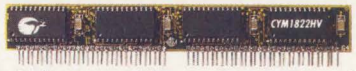
0.8 micron SRAM with 12 ns performance is the world's fastest 64K TTL. Here are seven of the fastest parts in memory.

SRAM Modules



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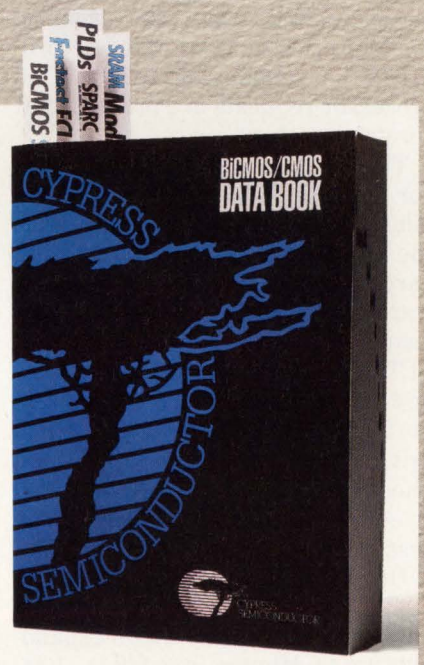


CYPRESS SEMICONDUCTOR

*1-(800) 387-7599 in Canada. (32) 2-672-2220 in Europe. ©1990 Cypress Semiconductor, 3901 North First Street, San Jose, CA 95134. Phone (408) 943-2600, Telex: 821032 CYPRESS SNJ UD, TWX: 910-997-0753. MAX is a trademark of Altera Corporation.

386-Based Laptop PC Uses Cache-Memory Design

Jon Campbell

Laptop PCs continue to challenge desktop computers. The latest example comes from Compaq Computer Corp. with its new 20-MHz 386SX-based laptop, the SLT 386s/20. The PC processes data up to 50% faster than 16-MHz 386SX-based systems, such as the desktop IBM PS/2 Model 55 SX, and nearly twice as fast as 12-MHz 286-based systems.

System performance of the Compaq SLT 386s/20 laptop has been enhanced by combining the 20-MHz Intel 386SX microprocessor with a 4-kbyte four-way set associative cache memory design, high-speed fixed-disk drives, a high-performance 16-bit graphics controller and support for an optional 20-MHz 387SX coprocessor. Said to be an industry first, the new laptop's 4-kbyte cache memory maximizes memory performance for fast processing of data. According to the company, up to 93% of all processor requests are processed at zero-wait states.

The 20-MHz 386SX microprocessor delivers 32-bit processing capabilities and full compatibility with the huge selection of industry-standard software, including 32-bit software developed specifically for 386-based industry-standard PCs. The SLT 386s/20 has the most data storage ever offered in a laptop, a high-performance 120-Mbyte fixed-disk drive. Both the standard 120-Mbyte (model 120) and 60-Mbyte (model 60) fixed-disk drives deliver average access time of less than 19 ms.

Other standard features for both models include 2 Mbytes of enhanced page system memory that's expandable to 14 Mbytes, a 3-1/2-in. 1.44-Mbyte diskette drive, industry-standard expansion slots, and a detachable laptop enhanced keyboard with full-size keys and standard spacing. A 10-in high-contrast liquid-crystal display is compatible with VGA, EGA, and CGA standards. The display supports eight shades of gray in 640-by-480-pixel resolution, and 16 in 320-by-200-pixel resolution.

The new laptop PC has several standard interfaces: serial, parallel, enhanced-keyboard, VGA-monitor, external storage-module and desktop-expansion-base. It also includes support for a wide range of diskette, tape-drive, and CD-ROM storage options. An optional CD-ROM adapter connects to the desktop expansion interface to provide support for a variety of CD-ROM drives.

Other options available for the first time include the 20-MHz 387SX coprocessor, and 1-, 2-, or 4-Mbyte memory boards. There's also an optional and enhanced 2400-baud internal modem which supports the V.42bis and MNP Level 5 protocols.

Similar in design to the Compaq SLT/286, the battery-powered SLT 386s/20 weighs 14 lbs., and is about 4-in. high by 13-1/2-in. wide by 8-1/2-in. deep. An enhanced NiCad battery pack gives over three hours of use. An adapter is available for ac-line power while simultaneously recharging the battery pack.

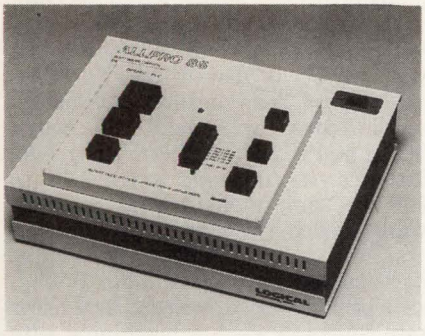
Unlike many portable computers, the Compaq SLT 386s/20 delivers additional performance required for productivity enhancements found in today's advanced business environments, such as multitasking and windowing environments. Users can run 386-based applications with such operating environments as Microsoft Windows/386 and DESQView 386. The Compaq SLT 386s/20 also offers a high-performance platform for business applications running under MS OS/2 and Unix.

Adding the optional 20-MHz 387SX coprocessor reduces the processing time of numeric-intensive operations (i.e. spreadsheet recalculation) while staying compatible with the large base of applications written for 287 and 387 coprocessors.

Suggested resale prices for the Compaq SLT 386s/20 models 60 and 120 are $6,799 and $7,499, respectively. Both are available now.

Compaq Computer Corp., P.O. Box 692000, Houston, TX 77269-2000; (800)231-0900. **CIRCLE 309**

IC PROGRAMMER FEATURES FLEXIBLE SOFTWARE CONTROL



With a library of 2800 devices and a standard test head configured with multiple sockets, the software-driven Allpro-88 programmer can handle 97% of all programmable semiconductor devices. The unit also supports the new avalanche-induced migration (AIM) devices, which required current-pulsed algorithms, rather than conventional voltage algorithms. Each of the unit's 88 pins has its own driver under software control, d-a converter, and current and voltage sensors. The Allpro-88 works with any IBM PC-compatible computer, issues complete binning commands to any popular device handler, and has software-controlled force-sense capability on every pin. Consequently, it is suitable for high-throughput factory applications and can make dc parametric and functional tests in one insertion. Data patterns are downloaded from any logic compiler with a JEDEC file output. The Allpro-88 costs $14,950 and is available 30 days after receipt of an order.

Logical Devices Inc., 1201 N.W. 65th Pl., Ft. Lauderdale, FL 33309; (305) 974-0967. **CIRCLE 301**

MAC II I/O BOARD OFFERS 12-BIT RESOLUTION

A plug-in board for the Macintosh II NuBus offers 12-bit, 70-kHz data acquisition on 16 single-ended or 8 differential analog input channels. The NuCarrier System also has 16 digital I/O channels, two independent counter/timers, and a burst generator. Users can software-program all NuCarrier functions and features and setup automatic channel scanning with individual gains on any channels and in any order. A MacPilot module, which plugs into a special connector on the NuCarrier, transforms the board into a bus master. MacPilot can initiate I/O data transfers directly to the host RAM. Other modules increase the number of I/O channels, resolution, and speed and add functionality. The NuCarrier comes with a utilities software package and drivers for any programming language that can access the Device Manager Toolbox. The NuCarrier costs $995 and the MacPilot Module goes for $695. Other I/O modules sell for $225 to $895, depending on functionality.

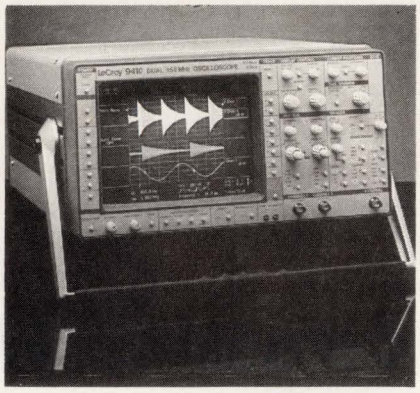
Burr-Brown/Intelligent Instrumentation, 1141 W. Grant Rd., MS-131, Tucson, AZ 85705; (602) 746-1111. **CIRCLE 302**

LOWER-COST DIGITAL SCOPE MAINTAINS HIGH-END FEATURES

The model 9410 general-purpose digital oscilloscope features several capabilities not usually found in digital scopes in its price range. The unit has a 5-by-7-in., high-resolution (4096-by-4096-point) vector-scan display and an "intelligent" trigger system that offers pulse-width, interval-width, logic-pattern, state, time/event, and TV triggering. In addition, a credit-card memory option stores up to 512 kwords of waveforms of setups per card.

The scope's two independent channels use 8-bit ADCs. Sample rate is 100 Msamples/s, and bandwidth is 150 MHz. The 10-kword (16-bit) acquisition memory helps the scope maintain a high usuable bandwidth and time resolution. The long record length, together with a zoom function, allows expansion of trace segments up to 200 times, even for fast signals. In LeCroy's Fastglitch mode, the 9410 will trigger on glitches as narrow as 5 ns.

Features include automatic setup, a 380-kbyte/s GPIB and RS-232-C interfaces, and an X-Y display. The scope automatically makes up to 10 parameter measurements, each updated with each new acquisition, on displayed, stored, expanded, or processed waveforms. There's an optional firmware package for waveform processing and spectral analysis..



The 9410 costs $6900 and is available 6 weeks. The optional arithmetic firmware package sells for $990.

***LeCroy Corp.**, 700 Chestnut Ridge Rd., Chestnut Ridge, NY 10977-6499; (914) 578-6097.* CIRCLE 331

■ *JOHN NOVELLINO*

GRAPHICS SPEEDS STIMULUS GENERATION

An interactive graphics package, WaveMaker, generates stimulus and control signals for use in circuit design. Using WaveMaker, designers can create, capture, display, analyze, and modify digital stimulus and response data. The software accepts data from sources such as simulators, existing circuits and test programs, data created by the designer, and data generated by hardware modelers. It then generates input data for logic and fault simulators, logic analyzers, verification testers, VLSI component testers, and in-circuit or functional board testers. The system has four interactive graphics editors that operate on a common object-oriented database. These tools separate timing format from pattern data, making it easier for engineers to view and manipulate circuit behavioral information in preferred formats. WaveMaker will be available Sept. 1 at a cost of less than $10,000 each for quantities of five.

TSSI, 8205 S.W. Creakside Pl., Beaverton, OR 97005; (503) 643-9281. CIRCLE 332

BUNDLED PACKAGE ACQUIRES DATA ON MAC

A combined hardware and software package acquires up to eight channels of data for display on a Macintosh II computer. The system comprises the PolyGraf/8 data-acquisition card and the SM/8 Signal Manifold. The latter provides a TTL-compatible trigger input and transports up to eight channels of raw data to the Poly/Graf 8 card for a maximum acquisition speed of 1000 samples/s for each of the eight channels. This results in up to 8000 data samples being collected, displayed, and stored every second with no gaps in the collected data. Recording and examining the acquired information is simplified through the use of the PolyGraf software program, which blends the features found in data loggers, chart recorders, and VCRs to provide an intuitive user interface designed for plug-and-play operation. A demonstration disk of the PolyGraf/8 system is available for $10.

World Precision Instruments, 375 Quinnipiac Ave., New Haven, CT 06513; (203) 469-8281. CIRCLE 333

PORTABLE TESTER FINDS FAULTY WINCHESTERS

Housed in an enclosure with dimensions of 2-7/8 x 8 x 12-in., the 3000S single-port test system from FlexStar provides menu-driven, simultaneous analog and digital parametric testing of a wide variety of disk drives. These include any 5.25-in. or smaller Winchester disk drive with an ST506, ESDI, SCSI, or PC AT interface. The model 3000S can be employed with any PC to run the same menu-driven test software used by disk-drive manufacturers. Testing capabilities of the single-port test system include index timing, seek timing, seek error rate, data error rate, and data-window margining with a 1-ns resolution and $\pm$2-ns accuracy. Digital surface scans can be run with variable-size data windows. Optional analog probes provide missing-pulse, extra-pulse, track-average-amplitude, and resolution tests, as well as analog media scans for ST506- and ESDI-interfaced drives. The 3000S' $2995 price includes tester, software, PC I/O card, cabling, and one interface set. An optional power supply for the 3000S and drive under test costs $995.

FlexStar, 2040 Fortune Dr., Suite 101, San Jose, CA 95131; Mike Witte, (408) 433-0770. CIRCLE 334

DIAGNOSTIC SYSTEM HANDLES BOUNDARY SCAN

The Advanced Support System for Emulation and Test (Asset) offers designers a simple menu-driven interface for the standard IEEE-1149.1 boundary-scan test structures. The Asset system includes a scan controller module that resides in the IBM PC/AT expansion bus and connects to the target system through a cable and resynchronization pod. Diagnostic utilities in the software package include an interactive debugger and a waveform analyzer. Asset translates parallel test vectors into serialized form for the scan-test bus. It then converts the serial patterns into a format that's suitable for automatic test equipment. Since Asset is an open system, users can apply their own test vectors and programs to the target hardware. Alternatively, users can create new programs with a standard C++ compiler. Three versions of Asset are presently available, depending on the level of capability needed, and are priced from $7500 to $25,000.

Texas Instruments Inc., Semiconductor Group, P.O. Box 809066, Dallas, TX 75380-9066; (800) 336-5236 or (214) 995-6611. CIRCLE 335

33-MHz 486-Based PC Runs DOS, Unix, OS/2

Blazing along at 33 MHz, the 433E PC uses an Intel i486 microprocessor and is built according to the EISA (Extended Industry Standard Architecture). The machine is compatible with Microsoft DOS and OS/2 and Dell Unix System V (compatible with AT&T's Unix). It's suitable for software development, CAD/CAM/CAE, single and multiuser Unix applications, and high-end network-server applications. It comes standard with 4 Mbytes RAM, expandable to 16 Mbytes on the board; a 16-bit VGA controller; a 5-1/4- or 3/1-2-in high-density disk drive; eight expansion slots; and one parallel and two serial ports. Prices start at $7899.

Dell Computer Corp., 9505 Arboretum Blvd., Austin, TX 78759; (512) 338-4400. CIRCLE 310

Optical Drive Accepts Rewritable, Media

The latest addition to a family of optical storage products is the LaserDrive 520 rewritable/write-once 5-1/4-in. optical disk drive. Rewritable/write-once means that the drive can use either write-one or rewritable media. Either type of disk gives a maximum storage capacity of 654 Mbytes. The drive, with its 70-ms access time, automatically reads and deciphers the type of media in use, and then alerts the user about it. Large-quantity pricing is $2395. Availability is in Sept.

Laser Magnetic Storage International Co., 4425 Arrows West Dr., Colorado Springs, CO 80907; (719) 599-7900. CIRCLE 311

Universal Programmer Handles 1-Mbit EPROMs

16-kbit to 1-Mbit EPROMs and EEPROMs can be programmed quickly with the EZ-Writer-K3. Having 32- and 40-pin sockets, it accepts 24-, 28-, 32-, and 40-pin devices and programs 16-bit-wide megabit EPROMs sans personality modules or adapters.

Through front-panel keys and alphanumeric display, users can scroll through menus, then execute the appropriate command. An expansion unit adapts EZ-Writer-K3 to Gang and Set programming for four devices.

The programmer goes for $795. Shipping is 3 to 5 days ARO.

Bytek Corp., Instrument Systems Div., 508 N.W. 77th St., Boca Raton, FL 33487; (407) 994-3615. CIRCLE 312

EMPLOYMENT OPPORTUNITIES

Marketing Enginr Int'l. Prov engin'ng suppt servs for corp mark'ing efforts in China. Oversees techniy transfer to PRC industrl and oth users. Supp field sales offc in devel'ng/implem'ng markt'ng plans. Tech train of new prod releases to field sales offcs. Cond tech semnrs to cust and field sales persnl overseas in supp of PRC markt'ng. Dev engin'ng specs to supp industrl instrm'ion prod line sales within PRC. Reqs: BS in engin'ng + 1 yr exp in job or 1 yr exp as Sales/Markt'ng Enginr. Spec reqs: 1) Chinese lang fluency w/ abil to travel PRC up to 25% of time and 2)Must have 1 yr exp in tech engin'ng sales supp of process ctrl instrm'ion. 40 hrs/wk - 8 a.m. - 5 p.m. Sal: $32,000/yr. **Res: Illinois Department of Employment Security, 401 S. State Street - 3 South, Chicago, IL 60605, Attn: Joan Sykstus, Ref. #1644-S. An employer-paid ad.**

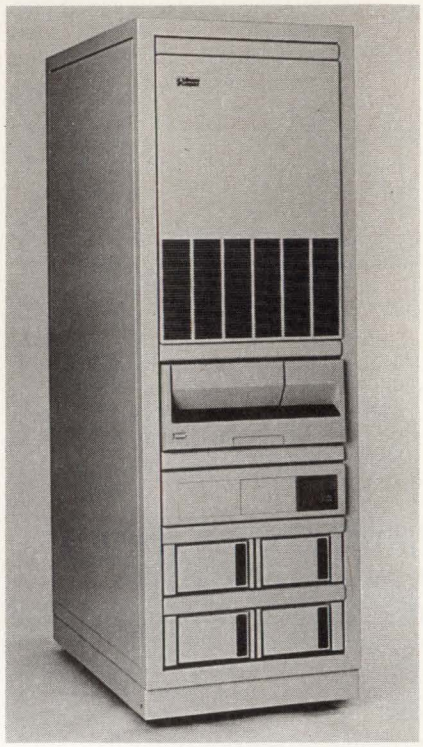
PARALLEL CPUs LET SERVER PACK >200 MIPS

By moving its Sun-compatible system architecture into a symmetric multiprocessing mode, Solbourne Computer can have up to eight 40-MHz Sparc CPUs running in parallel in its Series 5E/900 Enterprise server. The system employs the company's latest operating system release, OS/SMP 4.0D, which permits tasks to be dynamically allocated among 1, 2, 4, or 8 processor cards.

Each CPU card delivers more than 27 MIPS of integer and over 4 MFLOPS of double-precision Linpack floating-point performance, for a SPECmark benchmark rating of more than 19. The operating system distributes tasks evenly to ensure that performance increases are almost linear as new CPUs are added.

The servers are available with 32 to 256 Mbytes of RAM that communicates to the CPU cards over the company's proprietary 128- Mbyte/s K-bus. Furthermore, from 1 to 32 high-performance IPI disk drives, each capable of transferring data at 6 Mbytes/s, can be attached to the system.

When configured with one CPU, 32 Mbytes of RAM, and one IPI disk drive, the rack-mountable server sells for $89,900. A second CPU adds $10,000 to the system price. An 8-CPU system with 256 Mbytes of RAM and 16 IPI drives sells for $605,800.



***Solbourne Computer Inc.**, 1900 Pike Rd., Longmont, CO 80501; (303) 772-3400.* CIRCLE 336

■ *DAVE BURSKY*

IBM-COMPATIBLE CLICKER KEYBOARD: $39 PRICE TAG

Adding to their Right Touch keyboard line, NMB Technologies' low-cost "clicker" IBM-compatible keyboard comes in at a low price of just $39. The clicker keyboard, one that supplies an audible sound in response to key contact, uses long-life and high-reliability switches. The keyboard's cost has been cut by using a more powerful microprocessor, which eliminates the need for expensive peripheral components within the keyboard. Switch life is extended beyond industry norms by using a spring-return mechanism, rather than the traditional rubber boot. The keyswitches are rated to operate at up to 100 million cycles. The $39 price tag is for 100-piece orders. The clicker keyboard, with its streamline enclosure design, is available now from stock.

NMB Technologies Inc., 9730 Independence Ave., Chatsworth, CA 91311; (818) 341-3355. CIRCLE 337

3-1/2-IN. DRIVES STORE 425 MBYTES

The ceiling on 3-1/2-in. hard-drive capacity has been raised: Quantum Corp.'s ProDrive 425 and 330 store 425 and 331 Mbytes of formatted data, respectively, and each contains an embedded SCSI or PC/AT-bus controller. The drives, suitable for PCs or workstations, feature average seek times of 12 ms for read commands and less than 14 ms for write. Data-transfer rates up to 5 Mbytes/s can be achieved. Self-test capabilities simplify incoming and qualification testing. Evaluation units of the SCSI version will be available in August; volume shipments are scheduled for November. AT-bus-version evaluation units will be available in the fourth quarter. The 425 sells for $1595, while the 330 costs $1350, both in evaluation quantities.

Quantum Corp., 1804 McCarthy Blvd., Milpitas, CA 95035; (408) 432-1100. CIRCLE 338

CIRCLE 94 ⟶

LAPTOP PLUGS INTO VGA STATION

Combining the portability of a laptop with the capabilities of a desktop, the Interport Station and Laptop combination comes with a 101-key keyboard and a color VGA monitor. The Station contains no microprocessor, but it mates with the Laptop portion of the system that houses either a 20- or 33-MHz 80386 processor. The Station supplies the Laptop with communication and networking capabilities, additional hard and floppy drives, and tape or laser optical drives.

The Laptop, the portable part of the system, easily snaps in and out of the Station, which resides as a deskside unit. But the Laptop can also operate as a standalone computer. It contains either a 20- or 33-MHz 80386 microprocessor. An 80387 math coprocessor is available as an option. Thus, users can carry their data in the laptop and, if desired, they can hook up to a Station at another location. The laptop is compatible with MS-DOS, OS/2, and Unix. It comes standard with a 3-1/2-in., 1.44-Mbyte floppy disk drive and a 40-Mbyte hard drive. The Station, available now, costs $5395. The Laptop will be available in December for $6995.

Ogivar Technologies Inc., 7200 Route Transcanadienne, Ville Saint-Laurent, Quebec, Canada H4T 1A3; (514) 737-3340. CIRCLE 339

HIGH-END SERVER SUPPORTS NETWARE

Although initially tuned to support Novell's NetWare version 2.15 running in native mode and NetWare 386, a high-end network server is also designed to be independent of specific operating environments. Called the Independent Software Platform, the machine is based on an 80386 processor and comes in two models. The ISP 30 and the ISP 50 run at 16 and 20 MHz, respectively. Each comes with an optional coprocessor. The ISP also has a three-bus architecture designed to accommodate the heavy interrupt load that all servers must handle without significant degradation of performance. It can accommodate networks of between 40 and 60 users and memory is expandable to 12 Mbytes in the ISP 30 and to 64 Mbytes in the ISP 50. In addition to NetWare, Unisys is continuing ISP development for many standard operating systems.

Unisys Corp., 2700 N. First St., San Jose, CA 95150; (408) 434-2886. CIRCLE 340

WORKSTATION, SERVER YIELD 17.8 SPECMARKS

By running its R3000 RISC processor and math coprocessor at 25 MHz, MIPS has created both a desktop workstation and a file server that both deliver performance rated at 17.8 SPECmarks. (SPECmarks are the generic standardized benchmark ratings developed by the SPEC committee.) The Magnum 3000 workstation sell for just $8990 in its base configuration, which include 8 Mbytes of RAM, 3.6 MFLOPS of double-precision floating-point throughput, 17-in. monochrome monitor, keyboard and mouse, serial and Ethernet communication ports, SCSI host adapter for add-on storage, and the MIPS RISC operating system and windowing software. In graphics applications, the workstation can also deliver top performance for X-windows—it has an Xstones benchmark rating of 91,000; an 8-bit color version delivers 39,000 Xstones. The RC3230 server configuration contains the same CPU motherboard as the workstation. With a 200-Mbyte disk drive, 8 Mbytes of RAM and the operating system software, it sells for $11,740. The RISC operating system software includes NFS 4.0, TCP/IP, and other networking protocols.

MIPS Computer Systems Inc., 928 Arques Ave., Sunnyvale, CA 94086; (408) 720-1700. CIRCLE 341

BOARD INTEGRATES PC AUDIO, GRAPHICS, VIDEO

A single add-in board for IBM PCs and compatibles combines a high-fidelity digital stereo audio output with extended VGA graphics and NTSC-compatible video output for interactive audio-visual and multimedia presentation systems. The AV-16 Audiographics card fits into the expansion slot of any IBM-AT, PS/2 model 30, or 286/386-compatible computer. Supporting VGA, EGA, CGA, and Hercules graphics standards, the card has a 16-bit data path, a high-speed memory interface, and comes with a 1-Mbyte display buffer RAM for display resolutions of 640 x 480 or 800 x 600 with 256 colors, and 1024 x 768 resolution with 16 colors. The board also features monaural or stereo playback at selectable sampling rates of 8, 10, 12, or 16 kHz. Audio outputs can drive 8-ohm speakers with 250 mW of power. The AV-16 sells for $895 each; quantity discounts are available.

Antex Electronics Corp., 16100 S. Figueroa St., Gardena, CA 90248; (213) 532-3092. CIRCLE 342

CIRCLE 94

PROJECT MANAGER GETS POWER FROM WINDOWS

A project management software package—Microsoft Project for Windows—offers a graphical interface and flexibility for schedules and resources. Handling resource-driven or duration-driven scheduling, the software can, for example, calculate task completion time in resource-driven applications by adjusting for new workers added to or removed from various tasks. Resources can also be assigned partially, as well as selectively level resources, to balance workloads across multiple projects. The program also supports subprojects. Thus large projects can be divided into smaller tasks. Resource calendars can be defined at multiple levels. Schedules can be viewed in Gantt, Pert, and other forms, and users can manipulate the schedules by moving lines or boxes to group tasks or split off new tasks. Files can be saved in popular data format for programs. The Project-for-Windows package goes for $695. For a limited time, Microsoft Project users can upgrade for $195.

Microsoft Corp., One Microsoft Way, Redmond, WA 98052; (206) 882-8080. CIRCLE 327

PC SOFTWARE USES GRAPHICS

PC-based Viewpoint 4.0 project-management software includes a graphics module and supports interactive planning, multiple-resource allocation, resource leveling, progress posting, multiple-rate costing, and resource-constrained schedule forecasting. The critical path is automatically calculated and displayed in red as a project develops. Users can create Gantt, PERT, network, profile, or hierarchical charts. Minimum system requirements: IBM AT or compatible, 640 kbytes RAM with 1 Mbyte of expanded memory, EGA monitor, mouse, and hard disk. Viewpoint 4.0 is shipping now and costs $3500.

Computer Aided Management, 1318 Redwood Way, Suite 210, Petaluma, CA 94954; (800) 636-5621. CIRCLE 328

REAL-TIME OPERATING SYSTEM RUNS ON 80386 PCS

VRTX-PC/386, a real-time operating system for 80386-based PCs, takes advantage of the microprocessor's protected mode. Now, users can run their real-time multitasking applications. The software offers embedded system developers a dual-solution by allowing the PC to function as a software development platform and as an embedded computer. Users can write programs up to 4 Gbytes in protected mode.

The capabilities supplied by VRTX-PC/396 include task management, intertask communication and synchronization, memory allocation, real-time clock control, interrupt servicing, and window support. Available now, the software sells for $9880 for the initial development license with discounts for additional developers.

Ready Systems, 470 Potrero Ave., Sunnyvale, CA 94086; (408) 736-2600.
CIRCLE 329

MODULES TAILOR SWITCHING SUPPLIES

The Moduflex M Series delivers a power density of 6 W/in.^{3} at an ambient temperature of 50°C. Units are available with single and multiple outputs from 400 to 750 W. The 400- and 500-W supplies measure 2.5 by 5.05 by 9.00 in., while the 600- and 750-W models are 2.5 by 5.20 by 9.63 in. All units incorporate a 120-kHz MOSFET design and current-mode control. Prices start at $478. Delivery takes two weeks.

Deltron Inc., P.O. Box 1369, Wissahickon Ave., North Wales, PA 19454; (215) 699-9261. CIRCLE 323

HIGH-VOLTAGE ARRAYS SUPPLY 5-V CONTROL

Two transistor arrays, the PWR-NCH201 and PWR-NCH401, provide 5-V control of low on-resistance, high-voltage outputs. The arrays' outputs can be controlled independently or combined to provide additional current-handling capability. The 201 is rated at 5 Ω per channel, while the 401 is rated at 10 Ω. The latter comes in a 24-pin narrow-bodied plastic DIP, while the former is housed in a 16-pin batwing plastic DIP. Each array is available with breakdown voltages of 200, 300, or 400 V. Prices range from $2.60 to $5.84 in lots of 100.

Power Integrations Inc., 411 Clyde Ave., Mountain View, CA 94043; (415) 960-3572. CIRCLE 325

COMPACT CONVERTERS DELIVER 100 W

Operating at a 200-kHz switching frequency, a line of single- and multiple-output dc-dc converters provides 100 W of output power from an enclosure as thin as 1.25 by 4.25 by 5 in. Packaging densities exceed 3.5 W/in.^{3} for a full military unit that meets MIL-STD-461B, CE01, CS02, CS06, RE01, RE502, RS01, and RS02 specifications. Isolated and fully regulated outputs of 5 to 48 V dc are available. Efficiencies for the converters start at 75%. The standard input range is 20 to 50 V dc, which is compliant to MIL-STD-704, MIL-STD-1275, and the British standard 3G100 for 28-V dc input. Inputs of 12, 75, 95, 150, and 300 V dc are optional.

Logitek Inc., 101 Christopher St., Ronkonkoma, NY 11779; (516) 467-4200. CIRCLE 321

SUPPLIES GIVE POWER TO STD BUS CARD CAGE

Two power supplies give STD bus card cages greater power to handle more cards, particularly in 5-1/4-in. floppy-disk-based systems. The 105-W PS-105 and 160-W PS-160 each have three outputs and a feedback network for fast transient response and tight regulation. The 12-V output has enough current to power two 5-1/4-in. floppy drives and the STD bus. Prices for the PS-105 and PS-160 are $260 and $395. Delivery is stock to 30 days.

Computer Dynamics, 107 S. Main St., Greer, SC 29650; (803) 877-8700. CIRCLE 326

600-V MOSFETS HAVE LOW ON-RESISTANCE

Low on-resistance makes two 600-V power MOSFETs particularly useful for European off-line (220-V ac) power supplies and electronic ballast (277-V ac) applications. The SMP7N60 offers a current capability of 7 A and an on-resistance of only 1.1 Ω. The 4-A SMP4N60 is specified with a maximum on-resistance of 2.0Ω. Because they have such low on-resistance, they run cooler, are more reliable, and require smaller heatsinks. Both devices are housed in TO-220 packages. Unit prices are $1.98 and $0.99 for the SMP7N60 and SMP4N60, respectively, in lots of 10,000 units. Samples are available from stock. Production quantities can be obtained in eight weeks.

Siliconix Inc., 2201 Laurelwood Rd., Santa Clara, CA 95054; (408) 988-8000. CIRCLE 322

DC-DC CONVERTERS HAVE WIDE 2:1 INPUT RANGE

Intended for 12-, 24-, or 48-V dc powered systems, six 30-W dual-output dc-dc converters accept any input voltage from 9 to 18, 18 to 36, or 36 to 72 V dc. There are two output choices for each of the input voltage ranges: ±12 V at 1.25 A or ±15 V at 1 A. The converters in the XW Dual series have 80-kHz MOSFET switching and current-mode control, for efficiency ratings of over 85% at only 20% of full load. Line regulation is 0.02%, load regulation is 0.8%, isolation voltage is 500 V dc, and output noise is 20 mV pk-pk. Pulse-by-pulse current monitoring provides eight hours of short-circuit protection. All models are available from stock at a single-unit price of $165.

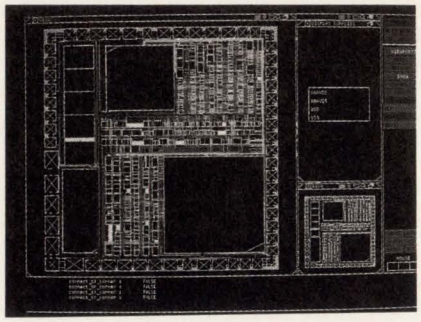
Calex Manufacturing Co. Inc., 3355 Vincent Rd., Pleasant Hill, CA 94523; (800) 542-3355. CIRCLE 324

TOOL SUITE PLACES AND ROUTES TRIPLE-LEVEL-METAL ASICS

The SL-Series of layout tools from Silvar-Lisco place and route both standard-cell and gate-array ASICs. SL-Cell and SL-Array, which layout cell-based and gate-array ASICs, are two key tool sets in the series.

The SL-Cell suite consists of three products: SC I, SC II, and SC III. SC I places and routes up to 5000 cells per level of hierarchy in two-level technology, while SC III can place and route as many as 20,000 cells per level of hierarchy in four-layer technology. Although some tool vendors attach a sea-of-gates router to a standard-cell placer, Silvar-Lisco constructed a true gridless router for cell-based designs. SL-Cell can layout any combination of up to three metal layers.

SL-Array is also made up of three products: Gards I, Gards II, and Gards III. The Gards products automatically place and route from two layers and 15,000 gates to three layers and more than 300,000 gates. In addition, both



the SL-Cell and the SL-Array products include such features as timing-driven layout and automatic rip-up and retry.

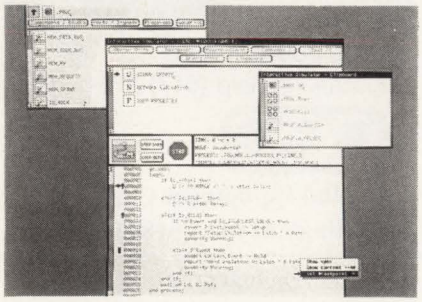
The SC I, SC II, and SC III products cost $30,000, $60,000, and $120,000, respectively. Pricing for Gards I, Gards II, and Gards III is $45,000, $90,000, and $180,000, respectively. All products are available now.

Silvar-Lisco, *703 E. Evelyn Ave., Sunnyvale, CA 94086; (408) 991-6000.* **CIRCLE 303**

■ *LISA GUNN*

VHDL IS BUNDLED IN A GRAPHICAL PACKAGE

A graphical VHDL design environment (VDE) from Intermetrics Inc. supplies window-based design and simulation for a variety of popular platforms. Users can access any number of the environment's components at one time. The Design Database Manager lets all the tools interact, and provides control over the design process. VDE's Analyzer performs semantic and syntactical verification. The Simulator, which the company claims is up to ten times faster than other VHDL simulators, contains a source-level debugger and a waveform viewer. In addition, the Navigator brings up VHDL text for a model at any point in the model. Prices for VDE, which will be available in the third quarter, start at $12,000 for a one-year, single-user license on a Sun-3 workstation.



Intermetrics Inc., 733 Concord Ave., Cambridge, MA 02138-1002; (800) 367-8435 or (617) 661-1840. **CIRCLE 317**

BUY ANALOG BEHAVIORAL MODELS OFF THE SHELF

Analog Libraries Ltd. will have its first library of analog simulation models available in September. The company has developed three levels of behavioral models. Level-zero models are fast models intended for the early phases of design, when what-if analysis is important. The level-one and level-two models increase in accuracy and detail. For instance, the level-two models include noise data and secondary effects. In addition, the company offers a custom modeling service, which costs between $500 and $5000 depending on device complexity and level of detail. A library of transmission lines and individual d-a converter models will be available in September for $800 and $300, respectively. A complete data-converter library will be available in October for $1900.

Analog Libraries Ltd., P.O. Box 17452, Boulder, CO 80301; (303) 440-3475. **CIRCLE 304**

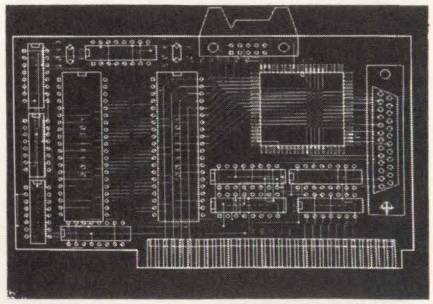
REWORKED FRAMEWORK FEATURES NEW TOOLS

The latest version of Fujitsu Microelectronics' framework, ASICOpen V1.50, includes the company's newest design tools, ZephCAD and BankCAD. ZephCAD is a logic synthesis tool that creates CMOS, biCMOS, and ECL circuits. BankCAD is a cell compiler for RAM and ROM. In addition to the new tools, version 1.50 extends some of Fujitsu's other internal tools, such as a waveform test editor and graphic simulation analysis, to work with third-party tools. Some of the third-party tools that operate within the ASICOpen environment include Cadence's Verilog simulator and Synopsys' Design Compiler. ASICOpen V1.50 will be available in the fourth quarter. The base price for the framework for each ASIC technology is $15,000.

Fujitsu Microelectronics Inc., Integrated Circuits Div., 3545 North First St., San Jose, CA 95134-1804; (800) 642-7616 or (408) 922-9000. **CIRCLE 305**

UPGRADED PCB TOOL ADDS BACK-ANNOTATION

Upgrades to the latest version of Orcad's pc-board layout product, PCB II Version 2.10, include back-annotation; PostScript, DGIS, and IGES support; and expanded surface-mounted part



support. With PCB II Version 2.10, layout designers can geographically re-annotate board designs using a horizontal or vertical priority. The information derived from the re-annotation is then back-annotated to the Orcad schematic, automating the process of updating schematics. In addition, Version 2.10 includes all the features of previous versions: manual and automatic routing, route and via optimization, and rip-and-reroute capabilities. PCB II Version 2.10, which is shipping now, costs $1495.

Orcad, 3175 N.W. Aloclek Dr., Hillsboro, OR 97124-7135; Scott Gustaff, (503) 690-9881. **CIRCLE 306**

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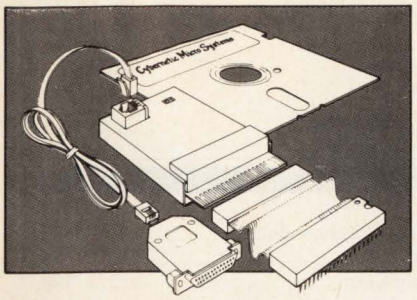

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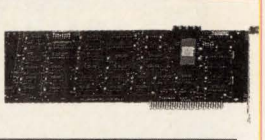

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- **D/A converter**: 2 channels; Resolution: **12 bits**; Settling time: 5μsec; ±5V
- **Digital I/O**:16In/Out(TTLcompatible); **Programmable Counter/Timer** (8254).
- **Software:** Utility software for BASIC & QuickBASIC included. Sample prgm. Supported by **LabDAS, ASSYST, LABTECH, UnkeScope.**

6 Channel 12 bit D/A [PCL726] $495

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PSEUDOCORP CIRCLE 273

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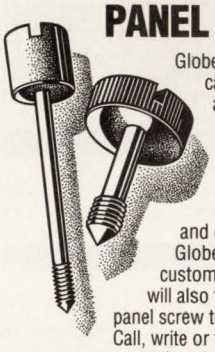

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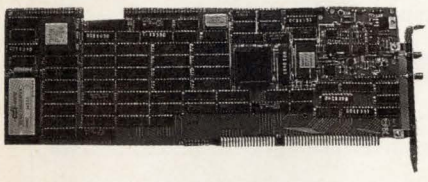
DASP100



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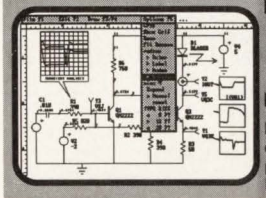

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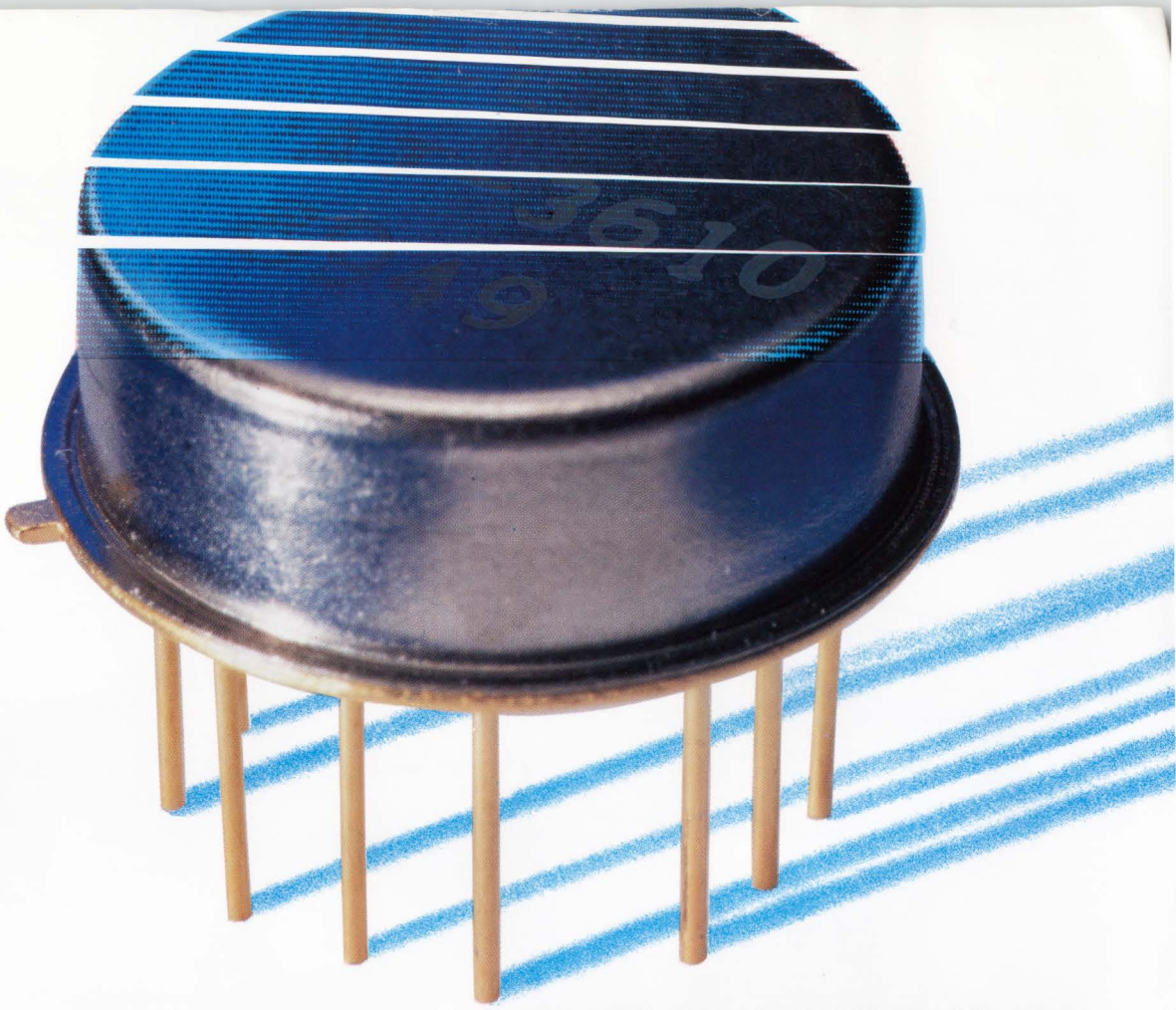

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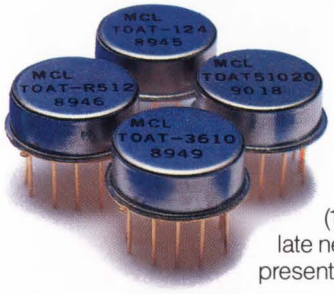
bold faced values are individual elements in the units



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