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## Going Global at The Hannover Fair

Acouple of issues back, we cited what we believe to be the five most critical issues facing the electronics industry: time-to-market, higher quality, design for manufacturability, designing with more complexity, and dealing with fewer vendors. All of these challenges, we noted, are being played out against a backdrop of global competition. This overall umbrella issue-global competition-will indeed set the pace for success or failure in tomorrow's electronics industry.

The global nature and the common concerns of the electronics industry was quite evident last month at the Hannover Fair Industry '91, the giant international trade fair held each year in northern Germany. A few stats: This year's fair drew 480,000 attendees to view the wares of-and make deals with-its 6339 exhibitors from 50 countries during the fair's eight-day run. About 20\%, almost 100,000 , of the visitors came from North and South America and the AsianPacific basin.
The fair basically covers all industries, from heavy construction equipment to hydraulics and pneumatics to microelectronics. Thus, the attendee can view wide-ranging electronic applications as well as the devices and subsystems themselves. Observing the operations at the exhibit stands and discussing the technology with the exhibitors, you get the impression that this is indeed a place for serious business. You also get the impression that, throughout Europe, the concerns of the international electronics industry are similar to what we face every day in the U.S.-those five vital issues cited above.

Concerning quality, the International Standards Organization (ISO) has already issued several standards covering this topic. ISO 8402 covers quality vocabulary; ISO 9000 involves quality management and quality assurance standards; ISO 9001, 9002 , and 9003 cover quality systems, or models for quality assurance in design/development, production, final inspection and test, installation, and servicing; and ISO 9004 offers guidelines for quality management. In many ways, thesestandardslay out a parallel process to our Malcolm Baldrige Award system.
Sensitivity to quality is spreading throughout Europe, just as it has done in the U.S., according to A.P. Matthijsen, Quality Support Manager at Philips Components, Eindhoven, the Netherlands. For example, the first European awards for quality will be made in 1992. And, needless to say, Japan already has its own version of quality awareness and its own awards.

Though the fair represented all four corners of the globe spanning thousands of



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SPECIFICATIONS

| MODEL | FREQ | GAIN, dB |  |  |  | - MAX PWR. dBm | $\begin{aligned} & \mathrm{NF} \\ & \mathrm{~dB} \end{aligned}$ | $\begin{aligned} & \text { PRICE } \\ & \text { Ea. } \end{aligned}$ | \$ ${ }_{\text {Qty }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MHz | $\begin{array}{r} 100 \\ \mathrm{MHz} \end{array}$ | $\begin{aligned} & 1000 \\ & \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 2000 \\ & \mathrm{MHz} \end{aligned}$ | Min. (note) |  |  |  |  |
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| MAR-4 | DC-1000 | 8.2 | 8.0 | - | 7.0 | +11 | 7.0 | 1.90 | (25) |
| MAR-6 | DC-2000 | 20 | 16 | 11 | 9 | 0 | 2.8 | 1.29 | (25) |
| MAR-7 | DC-2000 | 13.5 | 12.5 | 10.5 | 8.5 | +3 | 5.0 | 1.90 | (25) |
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## TECHNOLOGY BRIEFING

## Follow Up Research With Reality

Although the U.S. electronics industry still dominates or is competitive in most areas of high technology, it has come under attack for its fall from the top in memory chips, optical storage, and displays. A recent report by the Council on Competitiveness, a group of leaders in the industry, labor, and academia, concluded that the U.S. is in trouble in 33 out of over 90 technology areas. The problem was brought intosharper focus in a a address earlier this year at a UCLA Research Symposium by Daniel S. Goldin, vice president and general manager of TRW's Space \& Technology Group. "We've lost the edge in many highly visible arenas-stereo equipment, semiconductors, and


MILT LEONARD SENIOR EDITOR VCRs," said Goldin. "We invented them, but we lost the market because we failed to bridge the gap between high-tech research and lowcost, high-quality volume manufacturing."

Goldin also noted that the symposium featured papers on such topics as satellite-based networks, communication-systems research, and microwave communications. Yet, although the country's university system comprises 3400 institutions, 125,000 buildings, 6000 librarians, and 5 million students, less than $10 \%$ of them use state-of-the-art communications techniques. "It's taught, it's needed, but it's not used," he said. "We have become a nation of consumers instead of inventors, a service-oriented society. We're not translating technology into the real world."

What's the answer? Heightened emphasis across the industry on accelerated time to market through concurrent engineering and parallel product development would certainly be helpful. Also, faster development of standards for emerging technologies would give industry a healthy boost out of the starting blocks in the race to capture new markets and reclaim old ones. Another notion deserving serious consideration involves information sharing among universities and the industry.

The common thread weaving through all of these ideas is faster, more efficient data exchange on a country-wide or even global basis through computer networking-one of the remaining showcases of U.S. technological know-how. The concept is not new. Large firms are already linking mainframes with workstations and PCs to exchange information between all levels of operations: corporate management, R\&D laboratories, engineering, manufacturing, marketing, and accounting.

On a global scope, such a massive information-exchange depot might be modeled after the international distributed-processing computer environment of Cray Research Inc., Eagan, Minn. Its Data Center in the U.S. contains 10 Cray supercomputers networked to over 3000 machines, including mainframes, minicomputers, workstations, file servers, graphics terminals, X terminals, and PCs from multiple vendors.

The supercomputer handles CPU- and memory-intensive tasks for fast num-ber-crunching, while downloading visual information to a graphics workstation through a standard network. The main facility in Minneapolis, Minn., uses various types of networks: Ethernet ( $10 \mathrm{Mbits} / \mathrm{s}$ ), FDDI ( $100 \mathrm{Mbits} / \mathrm{s}$ ), and Hippi ( $800 \mathrm{Mbits} / \mathrm{s}$ ). Connections within the U.S. and to overseas sites are made with T1 (1.5 Mbits/s) lines. Network protocols used include Apple Talk, DECNET, Novell, OSI, TCP/IP, and X. 25 .

Fragments of such a system already exist in the communication networks of various government agencies, universities, and industry. But tying them together would be an enormous undertaking, requiring joint funding by all of the beneficiaries. Nevertheless, it's a worthwhile price to pay toward helping the U.S. regain its leadership in converting the fruits of its research into real-world products.

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## TECHNOLOGY NEWSLETTER

## Customizable DSPs Allow Optimized Design

Although a variety of digital-signal processors (DSPs) exist to satisfy a good share of the potential applications, some applications demand a more-optimized DSP solution. For just such applications, Texas Instruments, Dallas, has moved its popular TMS320C5X fixed-point DSP CPU cores (the 'C50 and 'C51) into its semicustom cell library to offer users two degrees of configurability. The simplest level offers the DSP core with the standard accompanying I/O features, but lets the designer adjust the amount of on-chip RAM and ROM. For applications requiring a higher degree of customization, the core can be coupled with any combination of serial ports, timers, analog-to-digital and digital-to-analog converters, and other functions created or extracted from TI's cell library. Customizing the DSP chips at moderate cost penalties enables designers to differentiate their products, reduce board space by integrating more functions on the DSP chip, lower power consumption by reducing the number of chips, and tackle specific applications that may not have been practical with off-the-shelf DSP ICs. $D B$

Two companies have allied to develop a standard graphics-display chip that cuts board space and cost while adding functionality. Music Semiconductors Inc., Colorado Springs, Colo., and Avasem Corp., San Jose, Calif., will jointly design the first combination color-palette DAC and frequency generator to fully support the super VGA (video graphics array) and other common graphics standards for the PC. Thus far, the PC graphics industry has been hindered by a lack of standards and second sources. In fact, many color-palette DACs and frequency generators have no credible second source.

Today's palette-controller ICs are controller-specific. And because the palette is a true mixed-signal IC, combining it with the complex logic of a controller results in a costly chip that's difficult to test and performance-limited in low-end applications. With both palette and timing-generator functions on the same chip, neither circuit impinges on the testing nor compromises performance of the other. In addition, because the IC isn't controller-specific, it can become a standard at minimum user cost. For additional information, call Bruce Threewitt at (719) 570-1550, or Jacqueline A. Chasse at (408) 297-1201. FG

Land-Grid Socket Land-grid-array (LGA) packages with up to 484 positions on a $0.050-\mathrm{in}$. centerline grid can be housed in the AMPFLAT LGA socket assembly. The socket, from AMP Inc., Harrisburg, Pa., offers an extremely low profile of less than 0.357 in . above the pe board. At the assembly's heart is a contact array that's just 0.009 in . high when compressed. It provides less than 10 -ps delay and $200^{\circ} \mathrm{C} / \mathrm{W}$ of thermal resistance per contact. The assembly consists of a heat clamp-pressure plate, a chip-carrier nest that holds the LGA, an AMPFLAT contact array, and an insulator-spacer sandwiched between a cover plate and base plate. The clamping top plate requires only a screwdriver for tightening or removal. Call for pricing and delivery. DM
analog Circuit Improves ADC Accuracy

Digital autozero/autocalibrate techniques combined with switched-capacitor digital-to-analog converters have been used increasingly to build analog-to-digital converters that hold 12 -bit and greater accuracy over temperature. But Maxim Integrated Products Inc., Sunnyvale, Calif., has decided to stick to pure analog techniques in its MAX178. This 12 -bit sampling ADC offers a guaranteed maximum "total unadjusted error" (TUE) over temperature of $\pm 1$ LSB. Though the parameter TUE (which includes gain, offset, and integral-linearity errors) over temperature has prevailed at the 8 -bit level, it's seldom seen at 12 bits, especially if it, like the MAX178, applies to the military-temperature range. In the MAX178, the input circuit employs an analog-autozeroed sampling comparator. Admittedly borrowed from switch-capacitor technology, it keeps the offset error below $1 / 2 \mathrm{LSB}$ at $25^{\circ} \mathrm{C}$. Unlike digitally corrected circuits, offset is zeroed every $60 \mu \mathrm{~s}$, or once every time a signal is sampled and converted. Keeping differential and integral linearity error within 1 LSB are in the hands of the chip's thin-film DAC. Gain error, a function of the on-chip reference, is laser-trimmed to within $1 / 2 \mathrm{LSB}$ at $25^{\circ} \mathrm{C}$. And like offset, it varies just $0.5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$. As with all of today's sampling ADCs, ac specifications are provided. Signal-to-noise plus distortion runs 70 dB , and total harmonic distortion and spurious noise run -80 dB each. For additional information, call Steven Leandro at (408) 737-7600. FG

# MotorolaDiscrete 



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A wide selection of SCR's are available: on-state current ratings from 0.8 A to 55 A , blocking voltages from $50-600 \mathrm{~V}$ and packaged in cost-effective TO-92, Case-77, TO-220, and TO-220 FP.


## Now the right hand knows what the left hand is doing.

Motorola's MPX5100A provides direct microprocessor interface and an absolute pressure reference. It's the industry's first fully integrated pressure sensor with absolute reference. This 0-15 PSI sensor integrates the sensing element, offset calibration, temperature compensation circuitry and signal amplification all on the same monolithic silicon chip.

The output signal is calibrated for 0.5 V offset and 4 V span to speak directly to microprocessors with A to D inputs. It's also temperature compensated from $0^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$, making it ideal for use in industrial, biomedical, consumer and automotive applications.

"Prime Devices" designed for highspeed power switching applications.

Rated at 60 volts $/ 23 \mathrm{amps} / 0.120$ ohms, Motorola's new MTP23P06 is designed for applications such as switching regulators, converters, solenoid and relay drivers, and offers better electrical performance than the competitive part from IR, the IRF9Z34, rated at 60 volts $/ 18 \mathrm{amps} / 0.140$ ohms.

The MTP36N06E is rated at 60 volts/ $36 \mathrm{amps} / 0.040 \mathrm{ohms}$. It is our newest (E-FET) energy rated MOSFET, with an energy-efficient design that offers a drain-to-source diode with a fast recovery time. This device is particularly suited for bridge circuits where diode speed and commutating safe operating areas are critical.


## Matched-Pair sensor system for

 high performance and low pressure sensing.Motorola's Matched-Pair pressure sensing system employs a high performance silicon pressure sensor which is on-chip laser-trimmed, and a matching operational amplifier. The MPX6010D is designed to operate from $0^{\prime \prime}$ to $40^{\prime \prime}$ water column pressure, while the MPX6002D operates from $0^{\prime \prime}$ to $10^{\prime \prime}$ (approx. 0.361 PSI) water column pressure. Typical sensitivity with a +5 V supply and full scale pressure is $150 \mathrm{mV} /$ inch for the MPX6002D and $88 \mathrm{mV} /$ inch for the MPX6010D. Custom outputs are also available. Applications include industrial, biomedical, and commercial. Available as a kit or in assembled form.


## New SWITCHMODE IV debuts.

If you're looking for a device with reduced parameter sensitivity to temperature change, one with improved switching for lower power dissipation, low dynamic saturation characteristics, and improved efficiency due to lower base drive requirements, this Switchmode IV device rated at 5 amps and 1000 volts is the answer.

This newly introduced NPN Transistor is designed to operate in off-line switching power supplies and is being offered in the popular TO-220, MJE18004, and TO-220 isolated Full-Pak,", MJF18004 packages. The Switchmode IV process makes it possible to compete handily with high voltage mosfets in applications less than 100 watts and operating at frequencies from 40 to 70 kHz .


## New output transistor joins long pulse microwave power lineup.

Motorola's latest long pulse, L-band transistor is the output device of a 3-part lineup designed for common base amplifier applications such as JTIDS (military) and Mode S (commercial) transmitters. The MRF10120 is capable of providing over 9 dB gain operating from 36 volts and handling 10 micro-second pulses at 50\% duty cycle for a period of 3.5 milli-seconds at a time. The frequency of operation extends from 960 to 1215 MHz .

## Design News



Power to shrink the world.
Today's smaller, more advanced applications require compact, higher frequency power supplies. The MEGAHERTZ ${ }^{\text {m }}$ Family of semiconduc-tors-MBR20200CT, MBR2535CTL, MBR2030CTL, and MURH840CT, plus TMOS ${ }^{\text {m }}$ Power MOSFETS and Linear IC's-gives you the capacity to shrink your power supply designs and is the key to more watts per cubic inch.

The MEGAHERTZ Family includes both Schottky barrier and ultrafast rectifiers. They're avalanche energy rated and perfect for most high frequency switching power supplies and converters.


New high-speed, wideband, hybrid amplifier.

A new wideband hybrid amplifier designed specifically for use as the video channel final stage driver in high resolution color monitors is now available from Motorola. The CR3424 provides 2.7 nanosecond typical rise and fall times with 40 volt peak-to-peak output circuit swings into a 10 pF load. Linearity error is less than $5 \%$. Operation from an 80 volt supply provides the large DC offset range required for color monitors. To learn about the effects of video amplifiers on CRT picture quality and basic drive requirements and drive circuits for the CR3424, order application notes \#AN1103.


## New MOSFET turn-off device simplifies circuit design.

The MDC1000 Series offers an economical and space-saving method of turning off a power MOSFET while achieving a level of circuit improvement at the same time. It reduces the component count on an active gate turn-off network for power MOSFETS. One MDC1000 device replaces a zener diode, a signal diode, a resistor and a PNP transistor. Replacing these four devices with a single chip also frees up space on the printed circuit board. Applications for the MDC Series include PWM circuits in switchmode power supplies, DC-DC converters, and brushless and brush motor controls. Available in SOT-23, SOT-223 and TO-92 packages.


## New RF Data Book/Military Data Book.

Edition \#4 of the Motorola Semiconductor RF Data Book is now available. Though similar in appearance to Edition \#3, the new book has added 84 new data sheets and deleted 130 others. It also contains three additional items in the applications section.

The Motorola Discrete Military Operation Data Book (Second Edition) defines Motorola's current line of semiconductors or components for military and other highreliability applications.


Satellite microwave power transistors at down-to-earth cost.

If you're designing satellite up links for land, sea or airborne transportation vehicles and want L-band large signal output and driver amplifier stages, look to Motorola's rugged new MRA1600/RF309X Series of $1600-1660 \mathrm{MHz}$ microwave power transistors and associated linear devices. They feature gold metalization, diffused ballast resistors and internal impedance compensation - plus the lowest cost available.

## Get more information.

To get more information on any of the Motorola products shown, contact your local Motorola sales office, complete and return the coupon below to Motorola Semiconductor Products, Literature Distribution Center, P.O. Box 20912, Phoenix, AZ 85036. Or call toll-free any weekday, 8:00 a.m. to $4: 30$ p.m. (MST), 1-800-441-2447.

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# Group Sets Hardware And Software Standards 

 To endorse a nonproprietary, standards-based computing environment, a group of major computer hardware and software companies established the Advanced Computing Environment (ACE). Participating companies include Compaq, Digital Equipment, Microsoft, MIPS, NEC, The Santa Cruz Operation, Silicon Graphics, and Tandem. The environment includes two operating systems: a unified Unix called Open Desktop that comes from The Santa Cruz Operation Inc., Calif., and OS/ 2 Version 3.0 from Microsoft Corp., Redmond, Wash. It also includes support for two hardware platforms: Intel 80X86-based PCs and MIPS RISC-based systems. In addition, ACE will supply the specifications for networking with existing systems.The specifications resulting from the initiative will give users access to a large base of software that will run on many systems produced by multiple manufacturers. Applications will run on all ACE platforms without any modification. OS/23.0, due some time this year, will support MS-DOS, Windows, OS/2, and Posix-compliant applications. Open Desktop integrates Unix, a graphical user interface, data management, and distributed networking. ACE is open to all computer companies. Initial products resulting from the initiative will be available for developers by the end of the year, and end-user products should come in 1992. $R N$

4-Mbit UV EPR0Ms Access In JUST 80 NS An advanced $0.8-\mu \mathrm{m}$ process and clever circuit design now make it possible to produce the fastest 4-Mbit UV-erasable EPROM with an access time of just 80 ns . The high speed of the M27C4001-80FX1, from SGS-Thomson Microelectronics, Agrate, Italy, which is organized as 512 k by 8 bits, comes as the result of SGS's E5 CMOS process. The process uses 6 -in. wafers and polycide interconnects. The high speed is also derived from a matrix die design in which the memory array is configured as 16 blocks, each with its own bit- and word-line drivers. The shorter line lengths mean reduced propagation delays during addressing. Housed in a ceramic package with a rectangular window, the device contains a built-in electronic signature that allows the appropriate programming algorithm to be selected. Using Presto II, a high-speed interactive algorithm with $100-\mu \mathrm{s}$ pulses and no over-program pulse, the entire 4 -Mbit EPROM can be programmed in about 50 seconds. The device works over the operating temperature range of 0 to $70^{\circ} \mathrm{C}$. Its fast access makes it ideal for use in various applications requiring high speed and large memory capacity. These include laser printers, private automatic branch-exchange equipment, fax machines, robot systems, simulators, industrial controllers, and embedded circuits. RA

## Fast-Turn Program

 The overall design and development cycle for two-layer TAB interconnection products is now being compressed by a fast-turnaround program. In the new program, initiated by 3M, Austin, Texas, finished two-layer TAB film for high-lead-count ICs will be delivered four weeks after designs are approved by customers. The program will provide TAB products with identical characteristics to those produced on 3M's volume manufacturing line in Columbia, Mo. DMRUN SPICE2G6 ON The first version of Berkeley SPICE2g6 with virtual memory for use on PCs 386 AND 486 PCS based on the $386 \mathrm{sx}, 386 \mathrm{dx}$, and the 486 microprocessors has just been announced. RSPICE, from RCG Research Corp., Indianapolis, Ind., determines the amount of extended memory available at the start of the program. As the program runs, the available RAM is monitored. If the memory required for the simulation is greater than the available RAM, RSPICE begins swapping to disk memory and completes the simulation. Circuits with 10,000 transistors may be simulated with as little as 1 Mbit of extended memory.
The program is complemented by RGRAPH, an advanced graphical post-processor that lets users call on a library of intrinsic functions to analyze output variables. Just a few of these functions include ABS (absolute value), SQRT (square root), logarithms, all common trigonometric functions, as well as integration and differentiation. RGRAPH reads any standard SPICE file. In addition, it will create hard copy of any screen plots to a laser printer. RSPICE with RGRAPH sells for $\$ 295$, which includes a coupon to attend one of RCG Research's handson training seminars called "Successfully Simulating Circuits with SPICE." For a free demo disk of both programs or a copy of their SPICE-users newsletter, call Ron Kielkowski at 1(800) 442-8272. Incidentally, if you're an analog-circuit designer who uses SPICE and would like to teach, Kielkowski is looking for part or full-time help. FG


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## Closed-L0op Design Builds Fastest 12-Bit SAMPLING-AMPLIFIER IC

Anew architecture (patent applied for) and a high-speed complementary bipolar process have allowed Analog Devices' CLD Div., Greensboro, N.C., to come up with the fastest sample-and-hold amplifier (SHA) at both 10 - and 12 -bit accuracy in just one chip. This development continues a trend over the last 18 months that has seen fastsampling IC SHAs, like those from Vanguard Semiconductor, Milpitas, Calif., and Acculin Inc., Natick, Mass., take on more expensive and physically larger chip-and-wire hybrid SHAs.

In its 9100 , Analog Devices incorporates a switching-bridge circuit into the input amplifier and closes a feedback loop around them and the top of the hold capacitor (see the figure, a). This contrasts with conventional ultrafast SHAs that employ an open-loop buffer on the front end. The buffer is followed by a diode-bridge switch, the hold capacitor, and an outputbuffer with a JFET input, which may run in open- or closed-loop modes (see the figure, b). The only exception to this is an IC SHA from Vanguard, which closes the loop from output to input.

The loop gain corrects distortion caused by both the switch and amplifier, while still achieving slew rates in a class with open-loop designs. In addition, acquisition slew current for the hold capacitor is higher than that from conventional diode-bridge configurations, removing a major contributor to samplingrate and signal-frequency limits.
The new SHA, which grabs a $2-\mathrm{V}$ step change in voltage (from the last sample) to within $0.01 \%$ accuracy in a maximum of 23 ns (typically to $0.1 \%$ in 13 ns ), represents a good example of the tight link between

process, performance, packaging, and architecture. Without the process, the architecture would have been impossible. And, of course, without process, architecture, and special packaging, the SHA's performance would have been impossible.

The $12-\mathrm{V}$ complementary process used to make the device features vertical npn and pnp transistors with $\mathrm{f}_{\mathrm{t}} \mathrm{s}$ of 3.5 and 2.7 GHz , respectively. The special 20-pin, narrow-body ceramic DIP has supply-pin bypass capacitors integrated into its structure. The package also enables an off-chip, 22-pF silicondioxide hold capacitor to be added. Putting the capacitor on-chip would significantly increase chip area (and thus cost), and would make the capacitor voltage sensitive to boot.

Sampling ac signals represents a major application for fast SHAs, like the 9100 . As a result, ac specifi-cations-such as holdmode distortion-at high signal frequencies are just as important as acquisition time. In earlier devices, 12 -bit-accurate sampling rates were limited to about 20 MHz . Distortion generated in the front-end amplifier and switch typically limit dynamic range to about 75 dB and signal-tonoise ratio (SNR) to about 70 dB for $10-\mathrm{MHz}$ input signals (see the figure, again). The AD9100 provides typical and maximum hold-mode distortions of -81 and -72 dBfs (decibels full scale), respectively, while sampling a $12.1-\mathrm{MHz}$ sine wave at 30 MHz . Sampling $2.3-\mathrm{MHz}$ and $19.7-\mathrm{MHz}$ signals at 30 MHz results in typical distortions of -83 and -74
dBfs , respectively.
To maximize speed, Roy Gosser, the SHA's designer, replaced typical volt-age-switching circuits with speedy current steering. Isolation between digital and analog sections was thus improved, resulting in less aperture-time effects on the analog signal, and reduced power supply and analog switching noise. The peak switching transient from acquisition to hold typically runs less than 6 mV . SHA settling time (hold settling time) is under 1 mV in 7 ns .

The output buffer's zero-voltage, bias-current cancellation circuits keep the hold capacitor charged and provide a high-temperature droop rate as good or better than what's possible using a high-speed JFET. Droop rate runs a maximum of $6 \mathrm{mV} / \mu \mathrm{s}$ at $25^{\circ} \mathrm{C}$, at about six times that over the military-temperature range, and only about 15 $\mathrm{mV} / \mu \mathrm{s}$ from 0 to $70^{\circ} \mathrm{C}$. The buffer also provides firstorder quasistatic bias-current correction, which leads to a very high input resistance and very low droop sensitivity to signal voltage. Because the output buffer, like the input buffer, is a closed-loop amplifier, output distortion is minimal, even while driving heavy loads. The output buffer puts $\pm 2 \mathrm{~V}$ across $50 \Omega$.

In many conventional high-speed SHAs, acquisition or track-mode distortion is often lower than hold-mode distortion. The former doesn't include nonlinearities due to the switch network, and doesn't correlate to the relevant hold-mode distortion. However, the latter has traditionally been left
off data sheets. The AD9100's architecture minimizes hold-mode distortion over its specified frequency range. For example, in the track mode, the worst harmonic generated for a $20-\mathrm{MHz}$ input sine wave, sampled at 30 MHz , typically runs -65 dBfs. In the hold mode, it drops to -74 dBfs . That's because only dc characteristics are relevant in the hold mode. Since the outputbuffer settles to within $0.01 \%$ accuracy in just 7 ns , it has settled to its de distortion level even for track-plus-hold times as short as 30 ns .
To prevent hard saturation of the SHA's circuits when they're overdriven-
which can significantly increase overvoltage recovery time-clamps at $\pm 2.3$ V have been added to the chip's input. In the overdrive mode, the outputnever leaves the linear operating region ( $\pm 2 \mathrm{~V}$ ). When overdrive is removed, the output settles to within $0.1 \%$ of its value in 21 seconds. The limited output swing also protects circuits the AD9100 might be driving, such as flash ana-log-to-digital converters.
The SHA has a minimum, small-signal $3-\mathrm{dB}$ bandwidth of 160 MHz for a $400-\mathrm{mV}$ pk-pk input, and slews full-scale steps ( $\pm 2$ V ) at a minimum of $550 \mathrm{~V} /$ $\mu \mathrm{s}$. That translates to a full-power bandwidth of 43

MHz . Consequently, the device lends itself to socalled undersampling or super-Nyquist sampling of bandlimited signals beyond half the sampling rate (for example, IF amplifier outputs).

This kind of performance doesn't come gratis. The chip needs a maximum of 118 mA froma +5 -V rail, and 132 mA from a $-5.2-\mathrm{V}$ ECL supply. In quantities of 100 , the commercialgrade AD9100 runs $\$ 79$ each. The industrial grade costs $\$ 20$ more, and the military grade costs $\$ 198$. For additional information on the 9100 SHA, call David Buchanan at (919) 6689511.

FRANK GOODENOUGH

## Write-CaCHing Supplements Read Caching To B00st Drive Performance <br> tions, few apply the cache

Although many disk drives with intelligent interfaces, such as the Small Computer System Interface (SCSI), include an in-drive cache to speed read operato write operations as well. The volatility of cache data is often the main reason designers forsake the performance benefits that write caching can provide-an

increase in the sustained data-transfer rate of 50 to $200 \%$. However, by studying the way data is accessed and stored, engineers at Quantum Corp., Milpitas, Calif., have developed a scheme that lets them exploit write-caching benefits, particularly because the time needed for data storage is usually less than 25 ms .

The scheme, known as WriteCache, is implemented by Quantum in its 3.5 -in. SCSI disk drives. It accepts data into the drive's cache from the host system. When the write command is executed, the drive immediately sends a Command Complete message back to the host system before data is actually written to the disk. The host is then free to move on to other tasks, such as preparing data for the next transfer, without incurring delays

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## TECHNOLOGY ADVANCES

caused by the drive's seek time or rotational latency.

While signaling to the host that the command has been completed, the drive is actually writing the cached data to the disk, usually completing the operation in less than 23 ms after issuing the Command Complete message. With such a scheme, a sin-gle-block random write would only require about 3 ms of host time. Without write caching, the same random-write operation would require about 27 ms of host time.

Even though write caching as a concept isn't newlarge disk drives and streaming-tape systems have used it for years-the small form-factor disk drives haven't realized its full potential. However, as higher-performance desktop hardware places tougher demands on the drives, intelligent write caching can give designers that extra measure of system performance.

One concern users might face is no confirmation of a successfully completed write to the disk. If so, the host can disable the WriteCache at any time. More appropriately, the host could disable the feature during the last block of a sequential write. That would cause the drive to return status information.

Another concern is that a write may not be completed if the drive doesn't have a good sector left to hold data. To counter that issue, the WriteCache will disable itself if fewer than five spare sectors are available on the drive.

Although random writes show a significant improvement, the most significant speed-up in sus-
tained throughput can be found during sequential writes to the drive (see the figure). Drives typically store data in the form of blocks, which usually hold between 512 and 8192 bytes each. Wherever possible, these blocks are assigned adjacent addresses on the disk to minimize the amount of seek time required to store and retrieve the file. Without write caching, the blocks are stored one at a time, with data from the first block downloaded from the host and then written to the disk. After the Command Complete signal is sent, the host sends the second block, and the process is repeated. Such an approach often causes significant delays between blocks, and might cause the data to be scattered across the disk due to other disk activity.

With write caching, the
transfer latency is hidden within the host-to-cache buffer transfer time, and actual drive writes can actually be done in parallel with the data transfers. Systems that use 1:1 interleave schemes on the disk drives, such as PCs, will typically see a 200 to $300 \%$ increase in write throughput when write caching is employed. That gain stems from the latency that's eliminated between sequential blocks thanks to the write caching.

Without caching, a 1:1 interleave drive could have a latency of as much as one disk rotation due to the time needed for the host to recognize the Command Complete signal and to start sending the next block. The delay would enable the disk to rotate far enough so that the next sequential sector would have already passed the read/
write head and the disk would rotate until that sector is back under the head.

The Quantum WriteCache algorithms will write data to the cache buffer while writing it to the disk. That simple operation enables the host to recall recently written data from the cache without accessing the disk. However, requests to read recently written data are infrequent in most applications. Moreover, data transfers from the host to the buffer, and from the buffer to the disk, still occur sequentially. With WriteCache, the operations occur in paral-lel-the drive can write data to the disk while simultaneously accepting new data from the host. This enhances throughput for every write operation, substantially increasing data throughput.

DAVE BURSKY

## Bare-Chip-Attachment Method Spreads I/0, Permits Pretesting <br> ed. It has several distinct

The simplicity of wire bonding, the pretesting capability of tape-automated bonding, and the packaging density of flip-chip techniques are all promised by a new barechip assembly technique for multichip modules. The technique, known as bond-ed-interconnect-pin (BIP) technology, uses proven thermosonic ball bonding and reflow soldering to create electrical interconnections between the bare chip and substrate.

The technology, which is being developed by Advanced Packaging Systems, San Jose, Calif., can be applied to any chip that's capable of being thermosonically ball bond-
advantages for multichipmodule assembly. For one, the full area of the chip can be used for I/O pads, not just the periphery. Potentially, this means a much higher pin count per die. Because BIP chips are assembled face-down on the substrate, signal-path lengths are minimized. The result is lower inductance and less pin-to-pin coupling in high-speed circuits, faster signal travel, higher clock rates, and higher overall system performance. In addition, path routing is simplified and packaging densities are as high as those achieved using flip-chip techniques.
be varied to accommodate thermal-coefficient-of-expansion mismatches that are often encountered using flip-chip attachment methods. This eliminates a failure mode that can plague multichip modules. For example, silicon die can be attached to ceramic substrates.

A proprietary connector technology is under development that will permit full-speed testing of BIP chips before they're committed to a module. The result is greatly increased module yields, which leads to lower final module costs.

The pins are fabricated from 2-mil-diameter gold bonding wire and are attached to the die with a

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## TECHNOLOGY ADVANCES

modified ball bonder (see the figure). A proprietary bonding capillary helps transform the bulk wire into individual pins. After the wire is welded to the chip's interconnect pad, it's clamped, drawn up in tension, and weakened by discharging an arc from a small electrode in the capillary wall. This causes a tensile break in the wire, which completes the pin's formation. Typically, the pins are broken at a length of 20 mils with a coplanarity of 1 mil and pitch of 6 mils minimum.

In final assembly, interconnect sites in the substrate are squeegeed full of solder paste, which is reflowed in a furnace. A thin layer of flux is wiped over

the sites. Then, the BIP chip is placed in position on the substrate and reflowsoldered to the interconnection sites.

Early reliability testing has been encouraging, according to the company's scientists. Preliminary data indicates no cata-
strophic failures of prototype BIP assemblies after such environmental tests as temperature cycling, thermal shock, mechanical shock, random vibration, and substrate-attach strength. Further testing is in progress to develop reliability data and a reliabil-
ity model for the BIP process. In addition, a fluxless process is being investigated, as are encapsulation materials for BIP assemblies and the possibility of using copper bonding wire to form the pins instead of using gold.

DAVID MALINIAK

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## Tiny-Chip Program Allows Low-Cost Breadboarding Of analog ics

Amanufacturing technology can now provide a silicon breadboard for analog IC circuits for just $\$ 1500$. "Tiny Chip" from Orbit Semiconductor, Sunnyvale, Calif., helps ensure first-pass working silicon on analog or mixed-signal, custom or semicustom ICs. The technology is part of Orbit's Foresight program which also includes larger chips. It lets IC designers at OEMs, system houses, and fab and fabless IC companies, design a reasonably sized (2.4-by-2.4-mm) analog circuit in CMOS, and have a dozen packaged
chips in-hand 5 or 6 weeks after design completion.

Use of the Foresight program for pure analog IC design is obvious. You can get lots of analog circuitry on a $10,000-\mathrm{mil}^{2}$ chip in $1.2-$ $\mu \mathrm{m}$ CMOS, the finest geometry of the 36 processes available. Orbit is able to offer this service, and profit from it, by putting designs from several customers on one wafer.

However, the most significant application for a "Tiny Chip" may be to let the analog-design guru on teams creating complex, largely digital, mixed-signal ICs check their circuits
in real silicon, in lieu of (or in addition to) simulation. Such a chip typically takes 18 months to design before going to fabrication. During this period, if the analog and digital design (including layout) proceed in parallel, the simpler analog portion is usually completed early on. If the design tape is then sent to Orbit, the designer soon has working silicon.

Because Orbit starts a wafer run every two weeks, a new set of ICs can be in the designer's hands in a few weeks, if problems are quickly found and fixed. This contrasts with a
$\$ 65,000$ cost and 10 -week turnaround of a typical industry fab cycle for $1.2-\mu \mathrm{m}$ CMOS. When the analog circuits are checked out, they're merged with the rest of the chip.

Foresight and Tiny Chip can also be used to develop an analog and/or digital standard-cell library. For circuit checking, one or more cells can be put on each chip.
Larger packaged die in the Foresight program include Small Chip ( 4.8 by 4.8 mm ) at $\$ 6000$ for 12 ICs , Medium Chip (7.2 by 7.2 mm ) at $\$ 12,000$ for 24 ICs ; and Large Chip ( 9.6 by 9.6 mm ) at $\$ 18,000$ for 36 ICs. Call Gary Kennedy at (408) 744-1800.

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## PRECISION INTERCONNECT

# Smaller Hard Dishs Pose Engineering Challenges Designers Are exploring Ways To Downsize Without Sacrificing Storage Capacity. 

The best of both worlds is coming together in the realm of hard disk drives: They're growing in capacity, yet shrinking in size. Such is the case with $5-1 / 4-\mathrm{in}$. drives, which have evolved into $3-1 / 2-\mathrm{in}$. drives. Now, the 2-1/ 2 s are the new kids on the block. And it won't be long before the 1.8 -incher moves into town.
The capacities for the 2-1/2-in. models are about where the $3-1 / 2$ s were two years ago, with drive downsizing cycles accelerating. The $2-1 / 2$-in. drive arrived about three years after the $3-1 / 2 \mathrm{in}$. was introduced. The $1.8-\mathrm{in}$. model should follow in about two years. And two years beyond that, look for the $1-\mathrm{in}$. version. Although the 1.8in. model is still just talk, the media suppliers say that the disks are ready and waiting. But don't expect the 1.8 s to come out in masses. Most drive makers want to raise the capacities on the 2-1/2-in. drive first.
As the drives get smaller, different problems arise. These include handling a connector that's as big or bigger than the drive, reducing the head and motor size, and flying the head closer to the disk. Other obstacles involve dealing with the smaller disk's lower linear velocity, different media types, and reducing the power consumption.
A number of companies currently produce 2-1/2-in. drives. Among them are Areal Technology Inc., San Jose, Calif. (60 Mbytes), Toshiba America Inc., Irvine, Calif. (22 and 43 Mbytes), Seagate


1. CONTAINED IN A PACKAGE that's about $2-3 / 4$ by 4 in. (shown here in actual size), Seagate's ST9051A drive holds 40 Mbytes of data. The media is made of thin-film aluminum. The drive uses just 0.5 W in the standby mode. E L E C T R O N I C D E S I G NB MAY 23,1991

Technology Inc., Scotts Valley, Calif. (20, 40, and 80 Mbytes), and PrairieTek Corp., Longmont, Colo. (20 and 40 Mbytes). Areal has a 100 -Mbyte version on the way and Maxtor Corp., San Jose, Calif., says its $2-1 / 2$-in. entry will come sometime in this quarter.

A drive's height is one critical feature that's in need of downsizing. In a notebook PC, where most of these small-form-factor drives are headed, the keyboard and monitor limit the machine's length and width. But quite often, the drive is the limiting factor in the system's height. In a palmtop computer, which usually has a re-duced-size keyboard and monitor, all three dimensions are equally important. Current palmtops employ SRAM memory cards, but they could move to rotating media if the drives get small enough.

Although the $2-1 / 2-\mathrm{in}$. drive contains a standard connector, a sub- $2-1 / 2-\mathrm{in}$. version will probably contain a more primitive interface. Present drives use a SCSI or IDE interface. Because those connectors would be larger than the whole drive, they would defeat the purpose of the small drive. The new interface would have a primitive signal coming out of the head and disk. Then, the circuitry on the motherboard will handle the actual read/write and communications functions.

Obviously, one way to handle the connector problem is to eliminate it. By mounting the drive directly onto the system's motherboard, the traditional connector wouldn't be needed. Today's lowprofile packages

# SMALL-FORM-FACTOR DISK DRIVES 


2. THE RAMP-LOADING TECHNIQUE, designed by PrairieTek, increases the drive's reliability by keeping the head from making contact with the disk. The head lays on the plastic surface when the disk is turned off.
could simplify mounting the headdisk assembly on the system's motherboard as a large component. There's an advantage in reliability using this method because some cables and connectors are eliminated. It would also conserve space.

Some activity exists in standardizing parts of the drives, which helps to speed up the process of embedding the drives. But system makers are used to having many drive suppliers, and if there aren't many embeddeddrive suppliers, the technology may not be quick to catch on.

The integrators, or system makers, are probably the most interested party when it comes to mounting the drive. They're concerned with problems caused by external sources within the system. For example, a liquid-crystal display (LCD) in a notebook PC tends to radiate noise. This noise can negatively affect the drive's error rate. The worst scenario is having the drive sit right under the LCD. Texas Instruments, Temple, Texas, found some inventive ways to avoid this problem in their TravelMate notebook PCs. On one model, they mounted the drive directly to the underside of a pc board containing ground power planes. This put the grounded board between the drive and the LCD, creating a shield. On their TravelMate 3000 , the drive is mounted under the keyboard, which contains an aluminum backing that supplies an adequate shield.

One component that must shrink to downsize the drives is the read/
write head. A smaller head produces a smaller mechanical load, making it easier for the head to follow the terrain of the disk. This accommodates any nonflatness of the disk. In addition, there's less chance of damage because the head won't come in contact with the disk. The downside is that it's more difficult to attach wires to a smaller head.

The present head generates a signal that's proportional to the linear velocity of the disk. An increase in linear velocity increases the signal out of the head. Linear velocity can be defined as the bits, one after another, that pass under the head. As the disk's diameter shrinks, the linear velocity gets smaller even though the disk's rpm doesn't change. This produces a weaker, and harder to recover, signal.

Media manufacturers are doing a good job at allowing the heads to fly closer to the disk. A year ago, $6 \mu \mathrm{in}$. was a standard height. Today, it's 4 $\mu$ in., and soon it will tumble to 3 . By moving down just a few microinches, the signal strength increases dramatically. The signal amplitude rises and the pulse width diminishes. There's also less noise.

Flying the head lower gets easier as the disk gets smaller. When the head touches the disk with a faster linear velocity, there's more impact energy. But touching the media isn't as traumatic with a smaller disk.

A technology that could impact small form-factor drives is the mag-neto-resistive head. Here, the transducer part of the head is independent
of the media's surface velocity. With a conventional inductive thin-film head, the speed of the acquired signal is related to how quickly the magnetic bits pass the head. As the form factor shrinks, the linear velocity gets smaller because the radius gets smaller. Because the magneto-resistive head is independent of the media's velocity, a good signal (in relation to noise) is acquired, regardless of the media size or speed. The velocity can be reduced by almost $50 \%$ with a reasonable signal coming out. This technology can be applied to both longitudinal and vertical-recording applications. It's been used in the magnetic-tape industry for some time, butit's more difficult in disk applications. Vertical recording is another method that could increase the capacities of small form-factor drives (see "Vertical recording," $p$. 41).

## Changing Media

Using glass-based media is sne way to get higher capacities from smaller disks. With glass, the head flies much closer to the media. Areal, one of the innovators of glass media, says it can fly the head under $4 \mu \mathrm{in}$.
"When we were talking about 4 $\mu$ in. a few years ago, people chuckled at the idea. They're not laughing now," says Mike Kirby, president of Areal. Areal's 60-Mbyte MD-2060 drive boasts a height of 0.59 in . and a weight of 5 oz . It uses about 2 W in the read/write seek mode.

Kirby says the technology was given more legitimacy when Toshiba announced a 43 -Mbyte, 2-1/2-in. glass-media drive. Its MD-1122FC measures $0.67-\mathrm{in}$. high and weighs 6.3 oz . In standby, the drive dissipates just 0.4 W . It features an average seek time of 23 ms and a transfer rate of 5 Mbytes/s.

The main reason for Toshiba's switch to glass was the high capacity that could be achieved using just one platter. It could squeeze 43 Mbytes on a glass platter, but only 30 Mbytes on an aluminum disk. There are also weight and power savings because a second platter is eliminated. Apart from the head-media interface, the rest of the design is the same. And

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## SMALL-FORM-FACTOR DISK DRIVES

the reliability of glass is as good as aluminum.
The higher capacities of glass come from its smooth surface. "To a flying head, a slight variation in the disk's surface looks like Mount Everest." notes Dave Tovey, director of marketing for Winchester Drives at Toshiba. The smoother the disk, the more consistently and closer the head can fly. And the closer the head flies, the higher the tracks/in. and bits/in. will be. Another advantage of glass is that the electronics pose less of a problem because the read/ write signals coming off the disk are very clean.

All of the 2-1/2-in. drives in Seagate's arsenal are constructed with thin-film aluminum. Its 20 - and 40 Mbyte models are nearly identical, except that the ST9051A uses two 20Mbyte platters and the ST9025A takes just one (Fig. 1). Both drives have a height of $0.75-\mathrm{in}$. and a weight of 6.4 oz . While the company expects the heights to drop to about 0.5 in .,
the lengths and widths of future drives won't change. The company's 80-Mbyte model has similar characteristics, using two 40 -Mbyte platters. Seagate wants to raise the capacities of its $2-1 / 2-\mathrm{in}$. drives to about 200 Mbytes before releasing a 1.8 -in. version because it feels the market is ripe for the 2-1/2-in. drives.
As the disks become smaller and thinner, their rigidity becomes a bigger factor. Now, $2-1 / 2-\mathrm{in}$. aluminum disks can be compressed down to 25 mils. As the diameter decreases, they can be made thinner while still maintaining mechanical integrity. But they can't be compressed as far as the glass disks, which are now 0.4mm thick (about 15.75 mils ). The tolerances of the present aluminum media aren't yet a problem, even though it's becoming more so as the drive shrinks. And with multiple platters, thinner media becomes more important.
There's also some ongoing research concerning the use of ceramic
media. But to date, there's not enough activity taking place to get excited about. Some time ago, a plastic media was discussed, but that's not too close to reality.
While no other materials are being talked about, the conventional magnetic coating is always being upgraded. The density of the coating is getting to the point where the noise level can be reduced by having smaller granules of magnetic particles reside on the disk.
To condense the mechanics, the motor size must be reduced-a very difficult task. This is possible, but it's very difficult. Building the motor is analogous to building a watch. The tolerances are extremely difficult to obtain. Even though the parts tend to increase dramatically in complexity, the smaller drive's reliability increases. This is mostly because the smaller drives contain less parts. A drive's mechanics were traditionally less reliable than the electronics. But today, the reverse is true-the me-

## UERTIEAL RECOBDING

Vertical recording (sometimes referred to as perpendicular recording) is a technology that's been around for about 10 years, but still has yet to make an impact on the hard-drive market. The theory behind vertical recording is similar to traditional recording, with a few distinctions.
On a traditional disk, the magnetic bits are aligned along the circumference of the disk in a northsouth configuration. This can be pictured as little bar magnets laid
down end-to-end (see the figure, a). When the drive's head flies over the bits, it detects the transition of north-south to southnorth. The direction the north pole faces versus the south pole determines whether the bit is a zero or a one.
In vertical recording, the little bar magnets are standing up onend (see the figure, b). Now the bits are aligned into the disk. This allows for a higher packing density because the bits are squeezed closer together.


The vertical-recording disk is comprised of two layers. The top layer stores the data; the lower layer is a soft magnetic material that conducts the magnetic flux to the return pole in the recording head. This lets the head and media operate as a unified system.

Because of the tremendous progress that's been made in longitudinal recording, vertical recording hasn't caught on yet. In addition, it requires a special head and read channel. Furthermore, there's only one supplier of verti-cal-recording media.

The company handling the bulk of the research in vertical recording is Censtar, San Jose, Calif. Although the technology hasn't been implemented yet, it does have a place in the small-form-factor market because it can boost the drives' capacity. Censtar is looking to license the technology to other companies, which they say is probably about 18 to 24 months away.

## SMALL-FORM-FACTOR DISK DRIVES

chanics rarely fail.
One condition drive makers try to avoid is stiction. This occurs when trace elements and other forms of contamination fall onto the disk, adding friction to the otherwise smooth surface. Upon power-up, the heads and media can stick together in such a way that the head can't read the data. This problem can be eliminated by a hydrodynamic air bearing or cushion that prevents the head from touching the media during disk startup.

Ramp loading is a patented idea by PrairieTek that prevents the head from coming in contact with the media. Whenever the drive is turned off, the head retracts to a loading mechanism, which is actually a molded piece of plastic that the head lies on to reduce wear (Fig. 2). This technique increases the reliability of the drive. In a desktop (at least in the office environment), the PC is usually turned on in the morning and off at night. When off, the head goes into a parking zone on the disk. But in a portable system, the disk will be parked many times to save power. Hence, there will be many landings and takeoffs. Every time this happens, the head is in contact with the disk for about 20 linear feet, causing excessive wear on the head and disk. Ramp loading, which eliminates this contact, is employed in all three of PrairieTek's 2-1/2-in. drives.

The shrinking of the drives has brought on other applications. These include printers, fax machines, fac-tory-automation systems, handheld PCs, and calculators. Smaller, portable applications make reliability a larger concern because smaller devices tend to be dropped or jostled around. A drive may be able to withstand a minimum of 10 G's of shock. But the way the system is configured, the drive may be subjected to 11 G's in a fall, even though the rest of the system encounters less.

## Don't Tip The Scale

Drive makers are doing everything possible to reduce the drive's weight. The components on the pc board are getting thinner. Surprisingly, the drive electronics make up a
good portion of its total weight. The base plate and cover are also heavy components. Some manufacturers have tried using plastic, but have found it to be unsatisfactory due to EMI, distortion, and instability problems. In addition, they've looked at reducing the bearing and motor weights, and eliminating as many screws as possible.

Areal put lots of research into the use of plastic casings, experiencing the same rigidity and noise problems. But the company says these snags can be overcome by coating the plastic. Even though there isn't much weight savings using this method, the parts could be produced more cheaply. Seagate feels that the dimensional stability of plastics has never been good enough to use as a base material for the drive. The company claims that plastics don't posses good enough temperature characteristics, making it difficult to obtain plastics with uniform properties, such as expansion.

Another concern to the system integrators is the power that's dissipated by the drive. A notebook PC has a limited battery life, something systems integrators are always trying to extend. In addition, integrators would like to keep the battery as small and as lightweight as possible.

The 2-1/2-in. drive uses from 2 to 4 W when it's being accessed. Most of the power drain comes from the mechanics, not the electronics. A 1.8-in. drive will use about 1.65 W in the active mode and as little as 0.1 W in the sleep mode. A majority of the drivecontrol electronics can enter a sleep mode, where most of the active logic is shut down and just the interface is awake. In sleep mode, the head is taken off the disk, eliminating any friction. Therefore, the disk can reach its operating speed more quickly.

Another way to save power within the drive is to lower its performance specifications. If the disk spins slower, the motor will use less power. But this takes away from the quality of the signal that comes off the disk. The disk can also take a little longer to reach its operating speed. Consequently, power is saved and the
disk's access time increases.
Media and head technologies quite often determine data densities and error rates, as well as the signal-tonoise ratio. The signal coming off the head can be so small there might be a need for more sophisticated errortolerance strategies in the electronics to accommodate for and correct errors. Cirrus Logic Inc., Milpitas, Calif., has developed a standard for error correction using Reed-Solomon techniques, called on-the-fly correction. The approach allows intermittent errors that are induced during the drive's operation, possibly from vibration or heat. It finds and corrects the errors transparent to the user. The company believes this method is a key to achieving high capacities in small drives. Because the densities of the disks are increasing so quickly, higher error rates are attained, boosting the need for better error-correction technology.

Two areas of electronics exist on the drive: one is for head, motor, and disk control, the other is for data control. Chip makers are being asked to put more and more functionality into fewer chips. Most of the drive makers agree that it's easier to shrink the electronics, but only to a certain point-there is a finite limit. While it may be easier to shrink the electronics, it often takes longer because ASICs are usually required.

## Move The Chips

An alternative to shrinking the drive's electronics is to move the electronics to the motherboard. Presently, there isn't enough stability to do that, meaning that too many engineering changes occur during a PC's design process. Presently, the system integrator would rather let the drive maker worry about the drive electronics. In addition, putting the electronics on the CPU board makes testing very difficult.

As the head-disk assembly gets smaller, it becomes more attractive to move the electronics off the drive. However, it may be a slow move because system manufacturers will have to be the driving force. Designers at Texas Instruments say that when they design a notebook PC, an

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## SMALL-FORM-FACTOR DISK DRIVES

initial step involves investigating the possibility of moving the electronics off the drive. So far, they've always decided against it, mostly for cost reasons. Another reason is that the integrator usually doesn't know which manufacturers' drive will be incorporated until the latter stages of the design. And because different drives require different electronics, they didn't want to have to do a different design for each potential drive. The only way to circumvent this problem would be for the drive makers to use standard parts. But most drives consist of ASICs designed in-house, ASICs designed by outside sources, and some off-theshelf parts. ASICs become more prevalent as the size shrinks.
In addition to combining functions to reduce the chip count, there's also room to make the existing chips smaller. Cirrus Logic uses a 100 -pin quad flat pack (QFP) that's somewhat smaller than a PLCC. A very-low-profile QFP that's about half the height of current QFPs and about two-thirds the footprint has also started shipping. The company says that both the height and area of the chips are equally important because drive makers want to mount the chips on both sides of the pe board.
Using a fine-line $0.9-\mu \mathrm{m}$ CMOS process, the Reach 1 read-channel chip from AT\&T's Microelectronics Div., Berkeley Heights, N.J., reduces both power (under 200 mW ) and space. The chip contains automatic gain control, pulse detection, a data synchronizer, and a peak detector, all functions typically housed in separate chips. The part also features a programmable data rate. In addition, National Semiconductor Corp., Santa Clara, Calif., recently released an integrated read-channel part(Electronic design, Apr. 11, p. 141). Like the AT\&T part, the National DP8491 contains the functionality once found in many chips.
AT\&T says that by the year's end it'll release their Reach 2 part. This chip will keep all of the functionality of the Reach 1, and add a filter, an encoder-decoder, and a frequency synthesizer. The company's goal, which is to get all of the drive's elec-
tronics down to one chip (excluding the preamplifier), expects a finished product by 1993.
Another part that cuts drive size is the AD7774 from Analog Devices, Norwood, Mass. It's a complete ana$\log$ I/O port consisting of a highspeed, four-channel analog-to-digital converter, dual track-and-hold amps, and three digital-to-analog converters. The part links to all commonly available digital-signal processors and microcontrollers.
A technology that could add to the drive's chip count, but significantly increase its capacity, is data compression. Drive makers are watching this technology closely. "It's just too good to ignore," says Areal's Kirby. "But there are still some problems associated with error correction." The compression electronics could also appear on the system board.

## Keeping Standards

Integrators agree that interface and form-factor standards are important, but they're not too concerned with internal-drive standards. As long as the signal coming from the drive is a usable one, it doesn't matter what goes on inside. The formatting procedure, speed, or the encoding scheme from drive to drive make no difference. But without the interface and form-factor standards, integrators would have to do different designs for different drives, reducing the time-to-market.
One way to avert the standards is to be first on the market with a product. Then that drive would set the standard. If integrators start to build to those specifications, other drive makers would have to follow suit. For this reason, mostdrive standards are created by de facto, not by committees.
Having standards simplifies the test engineer's job. Without them, the burden of testing essentially falls onto the shoulders of the drive maker, instead of lying equally between the system house and the drive maker.
One problem in testing small-form-factor drives is that they're driven by only 5 V , instead of 5 and 12 V. This makes them more susceptible
to power fluctuations. The problem increases as the drive's power level decreases.

If the electronics ever move off the drive onto the system board, the drives will have to be tested before the system is complete because the drive wouldn't be able to go into a test rack. Flexstar Inc., San Jose, Calif., one of the innovators in harddrive testing, produces equipment to test 5 -1/4-in. or smaller drives. The company redesigned its power-margining board to accept the lowerpower levels. The difficulty arises because on a sub--3-1/2-in. drive, the power-noise level grows. Flexstar wants every drive to be built with a test connector, a place where all of the test points would be brought out. Now, the test points for most drives are different. But the drive makers don't want to give up any real estate for such a connector.
An issue that concerns drive makers is the progress being made in flash technology, although now it's still somewhat costly. Flash could somehow merge with traditional disk drives. Presently, flash memories aren't suited for high capacities. To avoid a conflict between the two technologies, it's important to keep the capacities of the rotating-media drives to above 10 Mbytes .
Most drive makers agree that improvements in near-future drives will be incremental, not revolutionary. The next major advance may come from optical technology. They also agree that the starting point for a notebook PC drive is 40 Mbytes. Until a smaller drive can reach that level, it won't make an impact in the market.
Other improvements to look for in the future could come from more exotic read-write channels and more sophisticated signal-processing algorithms. Some of the signal-processing theory used in the communications industry could be applied to hard drives. $\square$

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The MAX232A improves propagation delay and symmetry

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## ハルXIN

[^0]
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| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Fixed Power-Up/Down Reset | $\checkmark$ | $\checkmark$ |  |  | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ |
| Variable Power-Up/Down Reset |  |  | $\checkmark$ | $v$ |  | $\checkmark$ |  |  |  |  |
| Battery Backup Switching | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ |  |  |  | $\checkmark$ | $\checkmark$ |  |
| Watchdog Timer | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ |  |  | $\checkmark$ | $\checkmark$ | $\checkmark$ |
| Power Fail Warning | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ |  |  |  | $\checkmark$ | $\checkmark$ |  |
| Write Protect |  | $\checkmark$ |  | $\checkmark$ |  |  |  |  | $\checkmark$ |  |
| High Current Memory Switch |  |  |  |  |  |  |  | $\checkmark$ | $\checkmark$ |  |
| Battery Monitor |  |  |  |  |  |  |  |  | $\checkmark$ |  |
| Price ( $\mathbf{1 0 0 0}$-up FOB USA) | \$3.27 | \$3.55 | \$3.27 | \$3.55 | \$2.12 | \$2.17 | \$1.96 | \$2.10 | \$2.10 | \$2.10 |

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## ノVIスXINV

[^1]
# RS－232 TRANSCEIVERS ISUPPIY $=500$ ，$\mu$ ！ 

## Optimize Power Consumption

Maxim has designed its new MAX220／MAX222／MAX242 dual＋5V RS－232 transceivers specifically for systems requir－ ing low power operation．The MAX220 dual transceiver＇s quiescent operating supply cur－ rent is a mere $500 \mu \mathrm{~A}$ typical（unloaded）， while the MAX222 saves power instead with a $10 \mu \mathrm{~A}$ shutdown mode．The MAX242 is sim－ ilar to the MAX222，but the receivers remain active in shutdown mode and have their own three－state enable．And，the MAX222／242 use small $0.1 \mu \mathrm{~F}$ capacitors，saving valuable real estate in portable applications．


To conserve power，use the MAX220 when transmitting data more than $2 / 3$ of the time．Use the MAX222／MAX242 with shutdown when transmitting less than $2 / 3$ of the time．

## Select a Dual Transceiver For Your Low Power Application

| Part <br> Number | Guaranteed <br> kb／sec | External <br> Caps <br> $(\mu \mathrm{F})$ | Supply <br> Current <br> No Load <br> $(\mathbf{m A}) \mathbf{m a x}$ | Shutdown <br> \＆Three－ <br> State | Features | Price ${ }^{\star}$ |
| :--- | :---: | :---: | :---: | :---: | :--- | :--- |
| MAX220 | 20 | $4.7 / 10$ | 2 | No | Lowest Power＠$>\mathbf{2 / 3}$ xmit／SHDN Duty Cycle | \＄2．65 |
| MAX222 | 116 | 0.1 | 10 | Yes | Lowest Power＠＜2／3 xmit／SHDN Duty Cycle | $\$ 2.65$ |
| MAX242 | 116 | 0.1 | 10 | Yes | MAX222＋Receivers Active in Shutdown | $\$ 2.65$ |

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## ハルスIル

[^2]
# JPEG Codec Chip Minimizes The Time And Money Required To Process, Store, Transfer, And Print Digitized Images. 

IC Executes Still-Picture Compression Algorithms

## Mlit Leonard

Designing more-affordable col-or-imaging features in facsimile machines, picture-archiving equipment, electronic stillpicture cameras, and numerous multimedia systems hinges on two events. One is the impending ratification of the JPEG (Joint Photographic Experts Group) image-compression standard for still-picture image compression. The other involves the availability of dedicated VLSI image-compression processors. Ratification of the JPEG standard, a CCITT/ISO (Consultative Committee for International Telegraphy and Telephony/International Standards Organization) document, isn't expected for another year or so. But system designers already face a number of chip, chip-set, and board-level options for implementing the standard.
The latest silicon solution to appear, the STI140 JPEG codec from SGS-Thomson, is the first single-chip VLSI processor to fully implement the proposed JPEG compression/ decompression standard for use in cost-sensitive business and consumer applications. Designed to compress color still pictures, the codec also has the speed to compress or decompress video at up to 30 color pictures/s. This performance paves the way for a new generation of color laser printers, multimedia pc cards, and electronic cameras.
Conforming with the proposed JPEG baseline standard, the device performs discrete cosine transformations (DCTs) on raster-image data. Using quantization and multiplecompression techniques, it obtains $20: 1$ to 30:1 compression ratios. This reduces the memory requirement for image printers and

cameras, and lessens the data transfer time for image data. The STI140, which can process complex images at $27-\mathrm{MHz}$ rates, performs JPEG compression in real time.

The JPEG encoding/decoding algorithm applies to continuous-tone gray-scale or color image data, which is typically represented as a 2D array of pixels. In computer-graphic or image-processing terms, each pixel is represented as an 8-bit (gray-scale) number or a 3 -

## JPEG CODEC CHIP

 1. THE JPEG ALGORITHM performs pixel blocking, discrete-cosine transformation (DCT), and quantization coding. That's followed by a compression of the serial bit stream using run-length coding (RLC) and Huffman encoding. Marker codes inserted into the JPEG bit stream ensures agreement between encoder and decoder.
by-8-bit (color) number. An XGA screen-the new IBM standard for high-resolution PC graphics-will consist of 1024 by 768 pixels. A single color image of this screen is represented by 2.4 Mbytes of data. Because of the frame-buffer requirements for display and printing, and the long time required to transmit such an image over serial data links (over 31 minutes with a $9600-$ bit/s modem), it's important to apply some sort of standardized compression that reduces the amount of data required for processing, printing, data transmission, and storage.

AllJPEG codecs must comply with a "baseline" specification that defines specific actions within the encoding (Fig. 1). These include pixel blocking, DCT, quantization coding, and serial-bit-stream compression through run-length coding (RLC) and Huffman encoding.

Huffman encoding creates short codes for frequently occurring symbols and longer codes for rare symbols. For example, a stream of random letters from A to G, with each letter represented by three bits, translates to a total of 102 bits with fixed-length coding. Huffman coding reduces the stream to just 83 bits. Marker codes are required in the JPEG bit stream to ensure encoder and decoder agreement. Besides the baseline algorithm, a number of extensions exist. These include "progressive coding," whereby the picture is built up gradually, and "arith-
metic coding," which optionally replaces the Huffman coding specified in the baseline algorithm.

Based on DCT and entropy coding algorithms, the baseline system is considered a "lossy" technique. However, JPEG also specifies the option of "lossless" encoding, which gives perfect picture reconstruction at compression ratios of around 2:1-most useful for medical imaging. This technique can also give near-perfect picture reconstruction at compression ratios of around 20:1, although the actual compression is picture dependent (see "Compression ratio: How much is too much?," $p$. 51).

## Inside The Codec

The SGS-Thomson solution minimizes the size and cost of color-image compression by packing these functions onto a $90-\mathrm{mm}^{2}, 1.2-\mu \mathrm{m}$ CMOS chip with three-layer metallization. Containing over 750,000 transistors, the STI140 executes the JPEG encoding/decoding algorithm while running on one 5 -V power supply and dissipating under 2 W peak. A power-down mode cuts power consumption to less than 10 mW .

Each element of the JPEG algorithm is implemented with its own dedicated unit on the STI140 (Fig. 2). Data flow between units on the chip is pipelined and controlled by handshaking operations. During encoding, data from an external staticRAM (SRAM) buffer moves through
the 32 -bit pixel port to the pixel blocker, which converts a rasterscanned image into a series of pixel blocks. Pixel blocking groups the raster-data input into 8 -by-8-pixel blocks, organized as chrominance (color) and luminance (intensity) components. Only a minimum of SRAM is required. A typical TV picture requires roughly 36 kbytes of SRAM for pixel blocking.
Next, the DCT transforms each block into a set of 64 coefficients-1 dc coefficient and 63 ac coefficients. The transformation effectively shifts the pixel block from the spatial domain to the frequency domain and concentrates most of the transformed block's energy in the lower frequencies. Prior to quantization, the de coefficient is encoded differentially with respect to the previous block, while the 63 ac coefficients receive no such coding.

Coefficients are quantized using a table of 64 quantization values. There's no specific quantization table specified in JPEG because the required values are highly picture-dependent. Quantization produces a serial data stream in which the lowerfrequency components are readily distinguishable from higher-frequency components. Because the higher-frequency components of the picture block are often invisible to the eye, quantization reduces them to a fraction of the picture content.

The codec then samples the 63 quantized ac coefficients into a one-
dimensional sequence in increasing frequency order. This operation is referred to as zig-zag scanning due to the nature of the sample path. Zigzag scanning groups together coefficients of similar frequency. The resulting data stream usually contains runs of consecutive zeros, which allows effective run-length coding.

Huffman coding compresses the numbers in the bit stream so that the most-frequently occurring coefficients are assigned short codes. This is achieved through either a one- or two-pass scheme. In a single-pass system, predefined Huffman tables are used. In the two-pass system, Huffman tables are created that are specific to the image.

The final compression function is
data packing, which assembles words from the Huffman encoder into bytes for transmission. An onchip sequencer inserts marker codes into the data stream, and sets the data path from the symbol buffer through the Huffman encoder, packer, and compressed-data buffer. The JPEG marker codes tell a JPEG decoder what is represented by the data stream, and gives instructions for decoding the data.

Contrary to widespread belief, picture compression is achieved through quantization as well as runlength and Huffman coding, not through the DCT operation. The resultant data stream represents a compressed picture that can be fully decoded through reverse operations
by any system that's JPEG compatible. During decoding, the same modules are used to process the reversed data stream. In this direction, the sequencer interprets the bit stream, strips out signaling information, and moves image data through the Huffman decoder to the symbol buffer. Data passes through the RLC decoder, zig-zag scanner, quantizer, inverse DCT, and pixel unblocker, finally leaving through the pixel port in raster-scan format.
The STI140 has four interface ports: a synchronous pixel port through which raster (or blockedpixel) data enters or leaves the chip; an SRAM interface for use in pixel blocking; a compressed-data port that operates asynchronously or
 he proposed JPEG standard specifies a means of compressing and decompressing an image so that the quality of the image is retained. This retention of image quality holds true regardless of whose equipment is used to encode or decode the image.

The JPEG algorithm doesn't specify a compression ratio, although a $20: 1$ or $30: 1$ ratio is typical. It instead specifies a compression algorithm that produces variable compression, depending on the redundancies within a photo. A country scene or seascape, for example, with broad areas of blue sky in the background will result in a higher compression ratio than a picture containing many intricate details (see the photos).

Subjective picture quality varies with the degree of compression. The picture sequence on the left shows the effects of processing a 24-bit image with DCT and quantization, and then applying varying degrees of compression. The original image is reconstructed by reversing the aforementioned procedure.

Ideally, there should be no difference between the original picture (top photo) and the reconstructed image (center and bottom photos), but they show something different. A 0.76 -bit/pixel ratio (center photo), which corresponds to a $32: 1$ compression ratio, is about the maximum information that can be obtained before visible image degradation sets in. A 0.082 -bit/ pixel ratio (bottom photo), corresponding to a $293: 1$ compression ratio, results in an image that's totally distorted.

The file size of a compressed and digitized color image (in bytes) is found by multiplying together four factors: the image area, the square of the image's resolution, the number of bytes/pixel in the image, and the compression ratio.

## An open letter of thanks to Charlie Sporck

On the eve of your retirement as President and CEO of National Semiconductor Corporation, we wanted to let you know how much we appreciate everything you've done for us, for this industry, and for this nation.
Since 1986, electronics has been the largest industry in the U.S., employing nearly 3 million people building over $\$ 295$ billion worth of products annually, almost all of them based on semiconductor technology. Obviously, this industry is of great strategic importance to the economic and political security of this country.
Charlie, you have spurred us to action by reminding us that product innovation alone will not suffice; that design plus manufacturing are the keys to America's industrial strength.
You have lived this message as one of the genuine pioneers of Silicon Valley. First as Production Manager and later General Manager of Fairchild Semiconductor. Then as President and CEO of National Semiconductor. As a founder of the Semiconductor Industry Association (SIA), developing public policy solutions to international trade and business issues. As the catalyst between industry leaders and government policy makers in SEMATECH, the first consortium to advance American manufacturing technology. And as a founder of the National Advisory Committee on Semiconductors.
You once said, "This country is full of starters. But there are damn few finishers. That's what it's all about: getting good at finishing."
You've set the standard, Charlie. There isn't anyone in this industry-anyone in this country-who hasn't benefited from your vision, your strength, your determination, and your steadfast leadership for more than three decades.
Thanks, Charlie. It's been an honor to have worked alongside you.
Your friends and colleagues in the SIA,

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## JPEG CODEC CHIP


2. THE STI140 C0DEC reeceives rasterscanned data through its 32 -bit pixel port at up to 27 Mpixels/s. After JPEG processing by the codec, compressed data exits through an 8 -hit port at the same data rate for synchronous or asynchronous operation.
synchronously; and a dedicated interface for an external microprocessor. The 32 -bit pixel port can operate in various configurations, with the pixel-blocking function enabled or disabled. Pixels can be applied at up to 27 Mpixels/s for various standard color spaces, such as YUV (luminance and chrominance), RGB (red, green, blue), or CMYK (cyan, magenta, yellow, and black). The 8 -bit compressed-data port operates synchronously using the $\overline{\mathrm{REQ}}, \overline{\mathrm{ACK}}$, and $\overline{\mathrm{OE}}$ lines, supplying the user with a choice between easy interfacing (asynchronous) or a clocked output with faster data rates.
The microprocessor interface consists of a 9 -bit address bus and an 8bit data bus, with separate read/ write and enable signals for control. These lines access the STI 140 control registers to define the characteristics of the compression, and to load quantization and Huffman-coding tables. The pixel port and com-pressed-data ports can also be read from this interface, although at somewhat lower data rates. However, using this interface for pixel data can reduce system costs by reducing
the number of bus interfaces required in the system.
When operated under the control of a microprocessor, compression characteristics, including picture size, video-component make up, and marker-code insertion, can all be varied. However, this is usually performed when the device is initialized. The microprocessor can also prioritize interrupts. As a standalone device, the STI140 can read embedded marker codes in the compressed data stream for instructions as to how to decode a picture. Combined with power-down operation, this feature is especially useful for such portable applications as electronic cameras.
Applications for JPEG encoders include color laser printers, PC multimedia cards, and electronic still-picture cameras. In color-laser printing applications, JPEG image compression reduces the transmission time for sending data from the computerimage source and the printer. In these applications, the JPEG codec resides between the Postscript interpreter and the frame-store memory, encoding and decoding pictures on-the-fly. For each picture, JPEG can
reduce the size of the printer frame store from 35 to 15 Mbytes.
Similarly, color facsimile machines will use single-chip data-compression/decompression engines within scanners and thermal printers. Although the standard describing color-image transmission over phone lines-a Group 5 standard CCITT document-has not been fixed, JPEG is an obvious candidate for this application. $\square$

## Price And Availabilty

Packaged in a 144-pin plastic quad flat pack, the STI140 JPEG codec costs $\$ 200$ in 1000-piece lots. It's available now in sample quantities. Production quantities will be available in the third quarter of this year.
In the U.S.: SGS-Thomson Microelectronics, 1310 Electronics Dr., Carrollton, TX, 75006; David Bye, (214) 466-7404.

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In Europe: SGS-Thomson Microelectronics, 17 Avenue des Martyrs, 38019 Grenoble, France; Philippe Thomas, 33-7-6585184.

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## Color Image

 Compression
## finally Heads

 For MaturityMultimedia platforms are characterized by the ability to manipulate and display huge volumes of digitized data. A key ingredient in this product's design is the image-compression function, which reduces image data to a reasonable size for economical storage and quick retrieval. As the multimedia revolution gathers momentum, OEM suppliers are beginning to flood the marketplace with various chip, chip-set, board-level, and software solutions for image-compres-

Multimedia Designers Can Sigh In Relief As THE InDUSTRY IDENTIFIES THE Last MAJOR Hurdles Faced By An Adolescent TECHNOLOGY.
sion applications.
Unfortunately, these products are often accompanied by confusing and misleading performance claims. Adding to the confusion are the yetevolving compression standards, and the question of which compression product is best suited for a specific application. To navigate through this cloud of uncertainty, a multimedia designer must understand such issues as the relevance of compression ratios, data rates, and image resolution; storage-media requirements and options; and what the various standards cover and don't cover.
The merits of image compression in multimedia design are unquestionable. However, selecting a compression ratio for a specific application involves careful trade-offs between system bandwidth, memory capacity, and image quality. System bandwidth determines transmission speed for file transfers. For example, without compression, an 8-1/2-by-11-in. color photo, scanned at 24 bits/pixel and 300 dots/in. for photo-graphic-quality digital imaging, would require 25 Mbytes of storage space. Consequently, a typical $40-$ Mbyte hard disk can store just one


1. THE JPEG BASELINE ALGORITHM can be augmented with optional functions for applications needing additional compression and decompression features. The extended system enables the encoder to handle pixels with greater than 8 -bit precision, additional data-interleaving schemes, and more color components. It also provides arithmetic coding for up to $10 \%$ better compression, and progressive build-up to successively improve an image as more data becomes available.
uncompressed color photo.
The data-transfer rate of a fast hard-disk drive is about 1 Mbyte/s and requires 25 seconds to capture or transfer the image data. Transmitting a 10 -Mbyte file over Ethernet takes about a minute, and moving the same-size file over a 2400 -baud modem takes over 5 hours. It gets worse with uncompressed full-motion color video, which requires data rates up to 28 Mbytes/s and takes up over 1.7 Gbytes of memory for a oneminute video segment.
For video compression, the trick is to use a compression ratio high enough to fit onto inexpensive storage media, like CD-ROM, while producing images of acceptable quality. But too high a compression ratio, depending on the image, may be unacceptable. A high-resolution image compressed at a high ratio can, for example, look worse than an uncompressed image with lower resolution. To illustrate, consider a 640 -by-480pixel video image that requires a 10 $\mathrm{Mpixel} / \mathrm{s}$ data rate for full motion, or $20 \mathrm{Mbytes} / \mathrm{s}$ at 2 bytes/pixel. Although a 100:1 compression ratio would reduce the data sufficiently for CD-ROM storage, image quality would be seriously degraded.
"The reason is because of the artifacts introduced by the quantizing step of the compression process," explains Richard Irving, director of

Brooktree Corp.'s graphics and imaging business unit, San Diego, Calif. "Artifacts translates to signal noise, which appears as a mosaic of squares in the decompressed image. This is most noticeable in the moving elements of successive frames."
Compressing motion video images poses other problems as well, regardless of the compression algorithm used. For example, because compression ratio depends on the degree of match between frames, any specified ratio is an average number. Commonly used compression algorithms for motion video compress successive frames containing elements with considerable motion that have ratios lower than closely matched frames. As a result, the compressed data stream can contain high burst rates that cause buffer overflow and make it difficult to synchronize audio and video.
The degree of image quality needed in a multimedia system depends on the application. In video teleconferencing, for example, the audio data contains most of the relevant information, with image quality ranking second in importance. Teleconferencing products can live with imaging qualities lower than VHS. On the other hand, VHS-quality images are insufficient for many desktopcomputer and workstation applications used for such tasks as video
editing and authoring.
Most multimedia observers agree that open international standards for data compression and decompression are needed to accelerate the spread of the technology. Proposed standards are developed by the standards groups of the CCITT (Consultative Committee for Telephony and Telegraphy) and the ISO (International Standards Organization). Formed by representatives from the industry, the working groups select the best features from algorithms submitted by the industry, universities, and independent researchers, and then submit the proposed standards to member organizations for balloting. Three emerging standards for the compression of color data are expected to become dominant (see the table).

With impending ratification next year, the Joint Photographic Experts Group (JPEG) standard proposes a compression/decompression algorithm aimed primarily at grayscale and color still images. The standard doesn't specify image parameters, such as color space, spatial resolution, and color representation. Instead, the standard proposes a lossy encoding technique based on a discrete cosine transform (DCT) and a uniform quantizer followed by two lossless coding stages. The threepart standard specifies a baseline
system, an extended system, and a separate lossless function (Fig. 1).

The baseline system delivers efficient lossy compression with sequential image build-up. The input data can consist of up to four color components, each with an 8-bit pixel depth. Redundant elements in the image are removed by the DCT, which operates on a stream of 8-by-8-pixel blocks that cover the entire image. The quantizer reduces the number of ac and dc coefficients generated by the DCT for each block. To optimize quantization for human perception, the step size of the quantizer can be tuned for each color component.

The coding model for the ac coefficients rearranges them in a zig-zag pattern and detects the run length of the zero coefficients for Huffman coding. The baseline system specifies a default Huffman table for the gray scale and one for the color component. In the one-pass mode, the encoder uses tables or precalculated custom tables. During the first pass of two-pass encoding, the encoder determines the best Huffman coding for the image being compressed. The baseline system can process the pixel blocks on either a block-interleaved or color-component basis, with no limitations on the horizontal or vertical dimensions.

JPEG image processing is symmetrical. That is, the same function blocks used for compression operate in reverse order for image decompression. For functionality exceeding that of the baseline system, the extended JPEG specification provides progressive image build-up and arithmetic coding. The extended system goes beyond the baseline system by handling pixels with greater than 8-bit precision, and by providing additional data-interleaving schemes and more color components. To minimize cost, the extended system is offered as a superset of the baseline system and isn't required for all applications.

Progressive build-up enables the system to reconstruct an image from just a small fraction of the compressed data. The JPEG decoder builds successively better images as more data becomes available. The
lossless function, part three of the three-part standard, specifies a compression method based on delta pulsecode modulation (DPCM), a form of differential PCM. This feature supplies a direct path for lossless encoding, which is a must for some applications.
"JPEG DCT encoding is lossy because of rounding operations," explains Steve Gary, director of marketing for image products at Oak Technology, Inc., Sunnyvale, Calif. "In some applications, like medi-cal-image archives, losing data because of image compression is out of the question. Lossy operations are fine in color images where some loss of detail is acceptable or not apparent to human vision."
> 2. FRACTAL TECHNOLOGY generated this image by replicating a pattern of basic image elements defined by a simple equation. For color-image compression, Iterated Systems Inc., devised a patented fractal-based algorithm that reverses the process. Called P.OEM, the asymmetrical system uses hardware and software to break an image down into basic patterns for compression. Image decompression is simple enough to be performed by software only. Photo courtesy of Computer System Architects.

Included in Oak Technology's line are products used for 1-bit/pixel compression and expansion of bicompression and expansion of bi-
tonal documents at data rates exceeding $650 \mathrm{Mbits} / \mathrm{s}$. An 8-1/2- by-11in. page can be compressed or expanded in less than 100 ms , or six pages/s. Envisioning JPEG as the clear winner for continuous-tone full-color compression, the company is poised to enter this arena when application requirements become clearly defined. "The market is very young," says Gary. "The real opportunities won't arrive until the mid1990s."

One market segment beginning to thrive on the JPEG standard is desktop publishing, which requires the highest-possible still-image quality. Although not yet specified as a JPEG extension or implemented in silicon, an interesting controlledlossy software package for desktop publishing is being offered by Storm Technology Inc., Palo Alto, Calif. Called JPEG ++ , the algorithm enables desktop computer users to selectively edit and compress parts of

an image. For example, near-lossless compression can be applied to a critical area, while high-ratio, lossy compression would be applied to a background.

Where the proposed JPEG standard doesn't specify image-representation parameters, the proposed MPEG (Moving Picture Experts Group) standard defines a bit stream for both compressed video and its associated sound. MPEG is targeted at CD-ROM data rates (1.5 Mbits/s), as a minimum, and good image quality at compression ratios up to 100:1. The standard also addresses audio compression and techniques to synchronize the audio signal with the video image.

Using the DCT technique for vid-eo-frame transformation, the MPEG algorithm compares adjacent frames to detect spatial differences between moving objects in the image. This allows substantial reduction in the amount of data needed to represent a sequence of video frames. Because the MPEG standard is still evolving, it's important

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[^3]to carefully examine any claims about image quality for hardware, touted to implement the MPEG algorithm or to be MPEG-compatible.

The ISO/IEC (International Electrotechnical Commission) MPEG group is planning three generations of the standard. Moving close to finalization, the video portion of MPEG1 addresses VHS-quality images with a 1 to 2 -Mbit/s data rate. The audio algorithm has been developed but is untested. MPEG2, for digital television or computer-quality images with a 5 to $10-\mathrm{Mbit} / \mathrm{s}$ data rate, is in the early stages of development. One algorithm being considered for this MPEG generation is based on fractal technology. The third MPEG version will address compression for HDTV-quality images, with data rates up to $60 \mathrm{Mbits} / \mathrm{s}$.

Another CCITT standard receiving much attention is H.261, which is expected to be approved within a year. The standard, also known as the Px64, specifies image-compression algorithms similar to MPEG. Intended for compressing motion video for transmission over digital networks, H. 261 will find applications in video conferencing.

Even as compression standards were being formulated, several pioneering chip vendors forged ahead with silicon that implemented their own proprietary color compression algorithms. Most notable of these are the DVI (Digital Video Interactive) of Intel Corp.'s Princeton, N.J. operation, and the CDI (Compact Disc Interactive), jointly promoted by Philips NV of the Netherlands and Sony Corp. of Japan.

DVI is an asymmetrical algorithm in which motion-video compression is handled by high-end machines that perform intense computations, and real-time decompression is done by a two-chip set residing in desktop computers. The system integrates motion video, still images, graphics, and text. Intel initially intended to have geographically dispersed service bureaus perform the image compression for end-users with appropriately equipped desktops.

CDI offers audio, high-resolution color images, animation, and text on
a 5-1/4-in. optical disk. Developed primarily for the home consumer market, the system uses a CD-ROM player that connects to a TV set.

Critical observers say that both DVI and CDI systems have drawbacks. After watching DVI demonstrations at the recent Multimedia and CD-ROM Conference in San Jose, Calif., some attendees came away feeling that DVI video-image quality was not high enough for multimedia applications. Another complaint for both systems is that their fixed architectures and fixed imagequality levels leave little latitude for design flexibility. However, Intel has announced future support for standard JPEG and MPEG compression while retaining its own proprietary compression algorithms.
to swell with both silicon and software solutions for image-compression, much work is left to be done for strengthening industry acceptance. Although seemingly resolved, the JPEG algorithms may yet undergo additional modifications to satisfy industry's demand for more cost-efficient compression schemes. Surely, new compression schemes constantly being developed will eventually supersede the existing standard algorithms. For example, the JPEG algorithm now uses 192 multiply operations for 8-by-8-pixel blocks. "But another solution requires just 64 multiplies," says Oak Technology's Gary, "and I've heard of a scheme that requires zero multiplies."

Where existing compression algorithms for color images are based on discrete cosine transform, the industry is searching for more efficient and economical approaches to spark the consumer market. One promising technique uses a patented fractal transform for col-or-image compression and expansion. In general, a fractal

The earliest single-chip JPEG implementation came last year from CCube Microsystems Inc., San Jose, Calif., whose CL500 JPEG compression chip comes in a $27-\mathrm{MHz}$ version, fast enough to compress motion video at rates up to 40.5 Mbytes/s. This was soon followed by a 6 -chip set from LSI Logic Corp., Milpitas, Calif., for executing the baseline MPEG and H. 261 compression algorithms. With functions partitioned to adapt to changes in the evolving standard, this product has user-selectable compression ratios. More recent single-chip devices include a multimedia device from UVC Corp., Anaheim, Calif., that compresses audio, still-image, and full-motion video, and a JPEG codec from SGSThomson Microelectronics (see "IC Executes Still-Picture Compression Algorithms, "p. 49).

Although the market is beginning
is an irregular structure or image formed by an infinite number of similarly irregular structures. One example of a computer-generated fractal is the Mandelbrot set, named after its developer, mathematician Dr. Benoit Mandelbrot (Fig. 2). The beauty of the technique lies in the relatively simple computer program that generates the image.

Reversing the process, mathematicians Dr. Michael Barnsley and Dr. Alan Sloan discovered a way to find fractal transforms automatically from digitized picture data. Once done, the transform is used to compress and decompress the digitized image. Upon this patented development, Barnsley and Sloan founded Iterated Systems Inc., Norcross, Ga., which now markets the P.EOM Fractal Image Compression System. The $\$ 25,000$ package includes an encoder board and software for image

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compression and a software decoder for image decompression. For compressing gray-scale and color images, the full-slot ISA-bus encoder board contains an Intel 80960 RISC processor and eight digital-signalprocessing ASICs that perform the fractal computation. According to company representative Louisa Anson, "the board compresses a 320 -by-200-pixel, 8 -bit gray-scale image in about 3 seconds, while executing about 2 billion instructions and using a $20: 1$ compression ratio. A typical 640-by-400-pixel, 24 -bit video image is compressed to between 5000 and 15,000 bytes, which amounts to a $77: 1$ compression ratio."
Representation of a compressed file is independent of resolution. "In fact, the system can decompress at a higher resolution than the original image," says Anson. "A 320-by-200-by-24-bit image can be compressed to 10 kbytes, and then decompressed to 640-by-400 resolution."
The company claims the picture quality of its decompressed images is better than that of the JPEG algorithm. At its maximum compression ratio, fractal compression can squeeze an image file down to $1 / 500$ of its original size, although at the expense of a degree of graininess in high-resolution images. Compression ratio varies, depending on such factors as the image's quality, its complexity, and its resolution, and compression time ranges between 16 seconds and 2 minutes. The system decompresses a compressed file in under 1 second.
The difference in processing times is due to the asymmetrical nature of the fractal technique. That is, encoding is much more computationally intensive than decoding. Initially, at least, this would seem to limit application to generating compressed files in a central location, and then distributing them throughout a network of sites equipped with PCs and decompression software. $\square$

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# UNDERSAMPLING Techniques SIMPLIFY Digital Radio <br> By Sampling Below The Nyquist Rate With A New Type Of ADC, Designers Can Exploit The Benefits Of Digital RADIO. 

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This article, the first of a two-part series, covers the fundamentals of digital radio and undersampling. The second part will describe a practical digital receiver, including the design of an analog front-end.

Digital techniques offer some inherent advantages in communicationreceiver design. These advantages, however, have been offset by both the cost and dynamic range limitations of analog-to-digital converters (ADCs). Consequently, designers continued to use analog circuitry despite its associated complexity and lack of flexibility. But recent introductions of low-cost, highly linear ADCs, combined with a technique known as undersampling, make digital processing the architecture of choice.

A review of receiver design shows how digital processing can improve performance. High-performance communication receivers invariably are superheterodyne designs. A typical example is a dou-ble-conversion unit that uses a broadband frontend and fixed-frequency bandpass filters after conversion to an intermediate frequency (Fig. 1). The input filter ensures the selectivity needed to prevent strong signals outside of the receiver's normal tuning range from overloading the first mixer and generating spurious signals.

The first mixer upconverts the received signal to the first intermediate frequency (IF), which is high enough to simplify design of the broadband input filter but low enough to permit use of a low-cost crystal filter. The first IF is typically well above the highest receive frequency so the broadband input filter can attenuate undesirable signals. Otherwise, these signals can feed through the first mixer and prevent the receiver's IF rejection specification from being met. The input filter must also reduce the undesired first-mixer image response at


[^5]E L E C T R O N I C D E S I G

2. BY USING DIGITAL COMPONENTS (including a softwarereceonifigurable digitalasignal processor) after the second IF amplifier, designers can simplify the receiver circuit and reduce costs.
frequencies twice the first IF away from the tuned frequency.

The first-IF bandpass filter protects the first-IF amplifier from overloading on signals that are within the receiver tuning range but outside of the desired receive-signal bandwidth. This filter also attenuates the second-mixer image response at twice the second-IF away from the desired signal frequency. The first-IF amplifier supplies just enough gain to allow a low receiver noise figure (for good sensitivity and a low noise floor) while maintaining a high dynamic range.
The second mixer downconverts the first IF to a frequency that permits the most receiver selectivity, gain, and signal processing at a reasonable cost. In the typical communication receiver, many second-IF bandpass filters may be needed to support the desired operating modes and bandwidth requirements. Additional frequency conversion to baseband may also be required, as well as multiple demodulation modes or embedded modems.

Analog-hardware costs, however, generally increase with the number of receiver operating modes. Consequently, using a software-reconfigurable digital-signal processor for the second-IF functions can reduce costs. Digital components can replace the second-IF and baseband functions (Fig. 2).

Digital processing can also simplify the design of the receiver's analog front-end. For example, the digital-
signal-processing algorithms can perform the fine tuning function, perhaps in $1-\mathrm{Hz}$ steps over a $1-\mathrm{kHz}$ range. This would allow the receiver's variable injection synthesizer to tune it's broadband input range in 1kHz , rather than 1 Hz , steps. Also, the programmable digital filters can compensate the passband magnitude and phase responses of the analog front-end filter, so a lower cost filter can be used.

## New Devices Help

Although the ADC in the second IF is a key component, it is only one element of a sampling system. Other elements include input conditioning amplifiers, a sample-and-hold amplifier, a voltage reference, digital interfacing circuitry, and clock conditioning circuitry. Older sampling systems were implemented in expensive, high-power hybrid devices. Recently, however, low-cost monolithic sampling systems have become available. For instance, an integrated ADC and sample-and-hold amplifier on one die form the core of what's called a "sampling ADC." In this article, the term ADC refers to such a system.
The sample rate of the second-IF ADC is an important factor. The digi-tal-signal processor's efficiency is largely determined by the sample rate, regardless of the algorithms used by the processor. The higher the sample rate, the lower the efficiency. Likewise, nonlinearities in the sample-and-hold circuit will dom-
inate the ADC's linear dynamic range, which consequently is affected by the second-IF. Higher IF frequencies result in lower dynamic range.

The digital-signal-processor designer, therefore, wants to use the lowest IF and sample rate possible to keep the receiver dynamic range and digital-signal-processor efficiency high. On the other hand, the analog front-end designer wants a high IF and sample rate to control image responses and aliasing in the ADC without a costly first-IF filter. Both designers can be satisfied by using undersampling techniques and sampling ADCs such as the AD679 and AD779, which have a built-in highperformance sample-and-hold circuit that is characterized above Ny quist frequencies.
Several operating considerations affect digital receiver design. For example, high frequency (HF) communication in the 2 -to- $30-\mathrm{MHz}$ band generally consists of long-distance voice transmissions with bandwidths on the order of 3 kHz , in a dense interference environment. Undesired signals from anywhere in the world can interfere with small desired signals at the receiver. Spectrum crowding and the possibility of high-power transmitters close to the receiver make high dynamic range a must.
Specifically, a typical HF receiver must be sensitive enough to receive a $0.5-\mu \mathrm{V}(-113 \mathrm{dBm})$ signal at the receiver input ( $50 \Omega$ ) with a $10-\mathrm{dB}$ sig-nal-to-noise ratio (SNR) in a $3-\mathrm{kHz}$

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bandwidth. Because this bandwidth is small compared to the input sample rate required to digitize the IF signal, the ADC quantizing noise is not normally a limitation. However, the receiver must also be able to receive a $1-\mathrm{V}$ signal ( +13 dBm ) without significant distortion. Consequently, in-band dynamic range must be at least 126 dB .

Unfortunately, a digital receiver's dynamic range is adversely affected by the fact that the bulk of the receiver gain must be ahead of the ADC and the second-IF bandpass digital filters. The high gain is needed to drive the ADC at a sufficient level. In an analog design, on the other hand, the gain occurs after the second-IF bandpass filters (Fig. 1, again).

In the digital design, this positioning means that undesired out-ofband signals can pass through the wider-bandwidth receiver front-end and saturate the amplifier and ADC. This must be avoided because ADC saturation generates many aliased in-band harmonic and intermodulation products that can block a weak signal. The solution lies in automatic gain control (AGC) and the use of large-wordlength, highly linear ADCs.

The AGC performs the same overall function in a digital receiver as in an analog receiver. But in a digital receiver, more AGC must occur at the front-end to prevent overloading of the amplifier and ADC. The AGC signal is usually derived from the narrow-band IF filter output, which
is implemented by the digital-signal processor. The designer must supply both analog and digital gain control, because the ADC can't possibly support the required $126-\mathrm{dB}$ of dynamic range.

A system-level analysis determines the desired receiver gain distribution, or analog versus digital gain. The maximum analog gain must be high enough to prevent the ADC's quantizing noise from degrading the receiver noise figure or sensitivity below their desired limits at small input levels. As the signal increases above the sensitivity level, the AGC should not decrease the gain until an adequate SNR is obtained. Above that level, the analog AGC should hold the signal level at the ADC essentially constant.

## Headroom Needed

In addition, the gain control must allow enough "headroom" at the ADC to avoid saturation during normally high peak-to-average voltage ratio periods of the desired signal. For normal speech signals, this headroom may have to be at least 20 dB above the average level.

When strong signals fall outside the digital filter's narrow bandwidth but inside the analog first-IF filter's bandwidth, the receiver must be able to detect any ADC overload. Then the receiver gain must be redistributed by reducing the analog gain and increasing the digital gain to maintain a constant output signal level. This action, however, will reduce the
signal-to-quantization-noise ratio.
As noted earlier, a low sampling rate is a key factor in the overall performance of a digital receiver. A cursory analysis would conclude that the ADC's sampling rate must be at least twice the IF frequency. However, this is not true when sampling a bandpass signal.

In the time domain, sampling can be thought of as multiplying the analog input signal by an impulse train that has the same period as the sample clock (Fig. 3a). In the frequency domain, the equivalent process is convolution of the analog signal spectrum with the impulse train spectrum. The result of the convolution is a set of images of the original spectrum at integer multiples of the sampling frequency, including dc (Fig. 3b).

If the sampling rate decreases as the spectrum bandwidth remains constant, the adjacent images get closer together until they begin to overlap. At this point the signal spectrum is distorted, corrupting the information in the signal. This problem is called aliasing distortion and explains the traditional interpretation of the Nyquist criterion, which requires a sampling rate of more than twice the highest frequency of the signal being sampled.

In the case of a bandpass signal, however, designers can use undersampling, which means sampling at a rate less than twice the highest frequency being converted. To understand why undersampling (also

3. IN THE TIME DOMAIN, sampling is the multiplication of the analog signal and an impulse train with the same period as the sample clock (a). The equivalent in the frequency domain is convolution (b). If the analog signal is bandlimited to be less than one-half the sampling rate and doesn't cross a multiple of the sample clock, the converter can undersample the signal without causing aliasing (c).

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called harmonic or bandpass sampling) is an ideal technique in radio applications, designers must study the spectrum of the typical radio receiver IF signal.
The IF signal, which is a bandlimited high-frequency signal, is applied to the input of the ADC, resulting in a frequency-domain convolution. Although the spectrum of the IF signal begins at a considerably higher frequency than that of a baseband signal containing the same information, the resulting convolution is theoretically identical (Fig. 3c).
Now it should be evident that undersampling must also satisfy Ny quist's theorem. However, the sampling rate must be at least twice the bandwidth of interest, not twice the highest absolute frequency. Obviously, this makes a big difference in the case of an IF signal.
Proper undersampling presents some other restrictions. For one thing, the signal bandpass spectrum should not cross an integer multiple of one-half the sample rate. If it does, the convolution will create overlapping images and alias distortion. Also, designers must select an ADC with input circuitry that supports the highest signal frequency, otherwise the ideal impulse sampling model will not hold.
Another important factor is that ideal undersampling assumes that the sampling system behaves identically for both high-frequency and low-frequency inputs. At high frequencies, however, converters suffer from errors that manifest themselves as noise and harmonic distortion in the recovered baseband signal. These errors limit the receiver's ability to recover an undersampled signal in uncorrupted form. Imperfections that were insignificant for sub-Nyquist-frequency inputs require additional scrutiny in undersampling applications.
As a result, designers must examine ADC specifications that are very different than those that were important for conventional conversion applications. Traditional performance measures-such as integral nonlinearity (INL) and differential nonlinearity (DNL) are character-

4. THIS EXAMPLE OF A SINE WAVE sampled by a clock of period $\mathrm{T}_{\mathrm{s}}$ shows how the effects of aperture jitter increase with the input's slew rate. For a given jitter ( $\Delta t$ ), the voltage error ( $\Delta \mathrm{V}$ ) increases as the slew rate increases.
ized with tests using de inputs. But INL and DNL are only partly responsible for the nonlinearities that arise in the presence of ac signals.

## Additional Factors

Radio designers must also be concerned with the converter's effect on the signal spectrum. This type of ac characterization specifies total harmonic distortion (THD), signal-to-noise-plus-distortion [S/(N+D)], intermodulation distortion (IMD), aperture jitter, and full-power bandwidth. Additionally, amplifier slewrate limiting, phase jitter, and decreasing open-loop gain become increasingly significant in the presence of high-frequency signals.
The parameters may be interrelated. For example, converter resolution, which sets the quantization noise floor, also determines the receiver's maximum theoretical dynamic range and affects SNR. Assuming a full-scale sine wave signal, the maximum theoretical SNR of an ideal ADC is ${ }^{1}$
$\operatorname{SNR}(\mathrm{dB})=6.02 \mathrm{~b}+1.76 \mathrm{~dB}$
where $b=$ the number of bits.
This equation assumes that the measurement bandwidth spans the entire Nyquist bandwidth of one-half
the sample rate ( $\mathrm{f}_{\mathrm{s}} / 2$ ). If the bandwidth is reduced after conversion to less than the full Nyquist-criteria bandwidth, the quantization noise power in this spectrum will be lower, resulting in a higher SNR. This condition is reflected in a generalized SNR equation:
$\operatorname{SNR}(\mathrm{dB})=6.02 \mathrm{~b}+1.76 \mathrm{~dB}+$
$10 \log _{10}\left(f_{s} / 2 B W\right)$
where $\mathrm{f}_{\mathrm{s}}=$ the sample rate in Hz and $\mathrm{BW}=$ the information bandwidth in Hz .
For example, if $f_{\mathrm{s}}=96 \mathrm{kHz}$, and the signal spans the entire Nyquist bandwidth ( 48 kHz ), the maximum SNR for a 14 -bit converter is 86.04 dB. But in the case of a bandlimited IF signal, which may span a $16-\mathrm{kHz}$ bandwidth, the generalized equation predicts a maximum theoretical SNR of 90.81 dB .

Unfortunately, other noise sources, such as aperture jitter, also degrade an ADC's SNR. Aperture jitter or uncertainty is the variation associated with the exact moment that a sample-and-hold amplifier goes into hold mode. Both external (somewhat correctable) and internal (uncorrectable) sources cause aperture jitter. External jitter results primarily from the designer's inability
to deliver a jitterless sampling clock to the ADC. Internal jitter occurs when the sample-and-hold amplifier's sampling switch fails to open at precisely timed intervals.

A time-domain analysis shows that the effects of aperture jitter increase as the input signal's slew rate increases. An example is the case of a sample clock locked together with waveform A (Fig. 4). In this example, if the sample clock has no variation (phase jitter), the output code from the ADC will always be zero. On the other hand, if the sample clock varies by an amount $\Delta t$, the ADC output will be the code that represents the error voltage, $\Delta V$, whose amplitude is
$\Delta V=(d V / d t) \times \Delta t$
where $\mathrm{dV} / \mathrm{dt}=$ the slew rate of the input signal in volts/s, at the sampling instant and $\Delta t=$ the aperture
uncertainty in seconds.
If the rms error voltage is well below the ADC's quantization noise, the resultant noise will be no worse than the quantization noise. As the error voltage increases, the converter's SNR, which previously was limited by quantization noise, will be dominated by noise related to aperture jitter. This noise results from phase modulation of the signal being sampled. If the aperture jitter is totally random, or "white," the noise produced by the phase-noise modulation will also be white. Regardless of the characteristics of the jitter-induced noise, aperture jitter will increase the overall noise floor of the ADC output spectrum.

## Predicting Noise Levels

Designers can predict the theoreti-
cal limits of rms-signal-to-rms-aper-ture-jitter noise ratio $\left(\mathrm{SN}_{\mathrm{j}} \mathrm{R}\right)$ based

5. DESIGNERS CAN PREDICT the theoretical limits of the rmssignal-torms aperturejitter noise ratio, $\mathrm{SN}_{j} \mathrm{R}$. For an rms aperture uncertainty, $\mathrm{t}_{\mathrm{a}}$, of 150 ps , performance begins to degrade above 53 kHz , approximately. Also shown on this plot is the maximum SNR that can be achieved if only quantization noise is considered. on a full-scale sine wave input and a measurement bandwidth of $f_{s} / 2$. The equation is ${ }^{2}$
$\mathrm{SN}_{\mathrm{j}} \mathrm{R}(\mathrm{dB})=$ $20 \log _{10}\left(1 / 2 \pi \mathrm{t}_{\mathrm{a}} \mathrm{f}_{\mathrm{a}}\right)$
where $t_{a}=$ the rms aperture uncertainty in seconds and $f_{a}=$ signal frequency in Hz .

A graph of this equation shows the maximum $\mathrm{SN}_{\mathrm{j}} \mathrm{R}$ that designers can achieve based solely on the noise introduced by aperture jitter (Fig. 5). Also shown is the maximum SNR that can be achieved if only quantization noise is taken into account. For a 14-bit converter with $\mathrm{t}_{\mathrm{a}}=150 \mathrm{ps}$, performance begins to degrade at about 53 kHz for a fullscale input.

When evaluating a converter's aper-ture-jitter perfor-
mance, designers must consider the input signal's slew rate. Reducing the signal frequency or amplitude will result in a $1: 1$ reduction in jitterrelated errors. That is, reducing the signal by a factor of 10 increases the undegraded bandwidth by 10 times.

The ADC's output contains undesired frequency components that were not present at the input. These components are at integer multiples of the input frequency. Consequently, designers should also evaluate harmonically related errors when trying to maximize dynamic range. THD, which describes the converter's linearity, is based on a ratio of the sum of the rms voltages of undesired frequency components to the rms voltage of the input. THD can be calculated with the equation

THD (dB) $=20 \log _{10}\left[\left(\mathrm{~h}_{1}{ }^{2}+\mathrm{h}_{2}{ }^{2}+\right.\right.$
$\left.\left.\ldots \mathrm{h}_{\mathrm{n}}{ }^{2}\right) / \mathrm{h}_{0}\right]^{1 / 2}$
where $h_{0}=$ the rms voltage of the fundamental and $h_{1}$ through $h_{n}=$ the rms voltages of the integer harmonics of the fundamental.
At low frequencies, harmonic distortion generally results from unequal step sizes in the ADC transfer function (INL and DNL). At high frequencies, slew-rate limiting, signal feedthrough, nonlinear resistors and capacitors, and decreased open-loop gain in the sample-and-hold amplifier are the culprits. Like aperture-jit-ter-induced noise, THD increases when either amplitude or frequency increases.

Another important measure of linearity is IMD, which results when two tones applied simultaneously to an ADC are "mixed" as a result of nonlinearities. Like THD, at low frequencies IMD is a function of the converter's INL and DNL.

However, the ADC doesn't behave like a typical saturated amplifier at low frequencies. In the amplifier, an increase in amplitude causes a corresponding threefold increase in the third-order IMD products. But the ADC's transfer curve can be considered linear with small random quan-tizing-level errors distributed throughout the converter's full range. Therefore, increasing the input signal's amplitude doesn't in-
put signal's amplitude doesn't increase third-order IMD.

Instead, the distortion is fixed relative to the converter's full-scale range and, thus, independent the input amplitude. But this is true only if the third-order intercept of the ADC input amplifier is high enough that amplifier IMD isn't the dominant distortion source.

At high frequencies and high amplitudes, IMD resulting from INL and DNL is overshadowed by the effects of sample-and-hold amplifier errors. Typically, the amplifier cannot track large, high-frequency signals fast enough to maintain linearity, and IMD increases, as it does in any amplifier.

Another specification peculiar to

6. LOOKING AT A CONVERTER'S OUTPUT using fast Fourier transforms shows how noise and linearity specifications are affected by the magnitude of the input signal. These examples show the difference for inputs 19.6546 dB below full scale (a) and 5.7722 dB below full scale (b).
undersampling converters is fullpower bandwidth (FPB). Although no standard definition exists, FPB is often defined as the frequency at which the amplitude of the reconstructed digital output resulting from a full-scale input signal is reduced by 3 dB . A wide FPB ensures a flat output when the ADC undersamples high-frequency inputs. It's worth noting that the bandwidth increases at lower inputs.

Designers, however, should examine the tradeoffs between frequency response and SNR. For instance, although the converter's FPB may be well above the Nyquist rate, other specifications-such as $\mathrm{S} /(\mathrm{N}+\mathrm{D})$ and THD-may vary as input frequencies approach the FPB. Also, smaller inputs reduce the SNR, but the resulting bandwidth increase reduces slew-rate-induced distortion and aperture-jitter-induced noise. So the FPB quoted in the data sheet shouldn't be the bottom line, although it's a good indication that the converter is intended for undersampling applications.

## Cost Is A Factor

Although linearity, sample rate, and resolution are prime considerations when choosing an undersampling ADC for digital radio, low cost and convenience are also important. And designers must also examine the device's performance for inputs beyond the typical sub-Nyquist frequency characterization. For instance, two examples of sampling ADCs are the AD679 and AD779. These converters are complete 14 bit, 100 -ksample/s devices that differ only in their digital interfaces. Included in the AD679 data sheet are ac specifications for THD, FPB, IMD and $\mathrm{S} /(\mathrm{N}+\mathrm{D})$. Graphs are specifically included showing the AD679's characteristics for signals beyond the Nyquist frequency.
$\mathrm{S} /(\mathrm{N}+\mathrm{D})$ determines the dynamic range that the converter can realistically achieve. This figure, which is computed by analyzing the ADC's output using fast Fourier transforms (FFTs), is the rms summation of quantization noise, jitter-induced noise, circuit noise, and THD. The

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2048-point FFTs for $456-\mathrm{kHz}$ inputs that are 19.6546 and 5.7722 dB below the AD679's full-scale input range illustrate the dynamic range calculation (Fig. 6).

As expected, the fundamental is at 24 kHz as a result of the undersampling convolution process. A number of specifications can be calculated directly from the FFT output data. For example, for an input 19.6546 dB below full-scale, the peak spurious noise is -103.386 dB relative to the converter's $10-\mathrm{V}$ pk-pk full-scale range, and the integration of all the spurious noise in the Nyquist bandwidth is -81.467 dB (Fig. 6a). The peak harmonic is -104.053 dB . Based on the first six harmonics, the THD is -99.821 dB , which is essentially buried in the noise floor.

## Calculated Noise Floor

At 456 kHz , the theoretical $\mathrm{SN}_{\mathrm{j}} \mathrm{R}$ for a full-scale input is approximately 67.3 dB (Fig. 5, again). Therefore, for a $-20-\mathrm{dB}$ input, the noise resulting from jitter is -87.3 dB . Adding the rms value of this noise to the ideal quantizing noise level of -86 dB results in an theoretical noise floor of 83.5 dB , which is relatively close to the measured level of -81.467 dB . The difference is due to external circuit noise and measurement error. This calculation shows that for inputs 20 dB below full-scale the ADC's dynamic range is limited by quantization noise rather than device nonlinearities.

A larger, high-slew-rate signal changes things. For an input 5.7722 dB below full-scale, the peak spurious signal is now -84.017 dB relative to full-scale, and all the spurious noise in the Nyquist bandwidth has increased by 5 dB to -76.414 dB (Fig. $6 b$ ). THD has also increased but is still a respectable -69.896 dB . Consequently, for large high-frequency signals THD, not quantization noise, limits dynamic range.

Note that the AD679's wide input bandwidth not only allows the user to sample a high IF frequency, but also presents the disadvantage of sampling noise and other undesired signals over the same large bandwidth. Like the desired IF informa-
tion band, the high-frequency noise is convolved with the sampling clock spectrum and can be aliased back to baseband, corrupting the signal. This is true for any undersampling ADC, unlike conventional converters, whose limited bandwidth filters out most of this noise. As a result, an ADC intended for undersampling is far more sensitive to the amount of noise at the input than a traditional converter, so board layout and decoupling considerations are even more critical.

Finally, convenience should not be overlooked in the choice of an ADC. The AD679 and AD779 are the only 14 -bit monolithic ADCs that are suitable for undersampling. Both contain an integrated sample-and-hold amplifier, voltage reference, digital latches, and control logic, and have high-impedance analog inputs to simplify input buffering. The AD679 has a convenient 8 -bit microprocessor interface and the AD779 has a parallel output that easily connects to digital-signal processors. The AD679 is also available in a pin-compatible 12 -bit version, the 200 -ksample/s AD678, which sacrifices dynamic range for speed. The AD678 is also specified at frequencies beyond Nyquist.

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# Algorithm Finds EIA-Standard 5\% And 10\% Component T $\cap$ C and Basic programs take the headache out of tolerancing by providing three values. 

BY JAMES A. KUZDRALL<br>Intrel Service Co., P.O. Box 1247, Nashua, NH 03061; (603) 883-4815.

Commercial components come in specific standard values that are established by the Electronic Industries Association (EIA). Most engineers have memorized these values and can fill in their schematic's $5 \%$ and $10 \%$ components without referencing a chart. But what if a computer is to do the choosing? Suppose the computer exuberantly calculates a collector load resistor to 15 places. What $5 \%$ value should it print out?

Although the problem is harder than it seems, a Basic subroutine or C function can give your computer the correct answer (Tables 1 and 2, respectively). In fact, the routines serve your tolerancing needs with three answers: the nearest value, the guaranteed-less-than value, and the guaranteed-greaterthan value.

Components graded to a $5 \%$ tolerance should have nominal values separated by $10 \%$. By starting with 10 and multiplying by 1.1, the first value of the $5 \%$ table, 11, appears. Continuing the process produces successive standard values until you reach 24. The next calculated value would be $24 \times 1.1=26$, but the standard table says 27 . In fact, values 27 through 47 and value 82 are all off from their logarithmic ideals. The separations vary from $6.7 \%$ to $15.4 \%$. Unlike the mathematically consistent $1 \%$ set, the $5 \%$ values are somewhat skewed.

The erratic spacing compli-


1. Computation results, such as 15.525 , fall within 5\% of two standard values (a). On the other hand, 25.44 isn't within $5 \%$ of any standard value.
cates computer solutions. A purely computational approach, such as a curve-fit formula, sprawls over several lines but fails to follow the arbitrary jogs. A lookup table works much better, but the non-logarithmic intervals still cause problems. Consider finding the nearest standard value by stepping through the table until a value within $5 \%$ is found. This works well for most values but not for all. For example, $15 \times 1.035=$ 15.525 is well within the $5 \%$ tolerance limit of 15 , but the next higher standard value, 16 , is the closest value (Fig. 1a). Conversely, $24 \times 1.06=25.44$. That value is a full $6 \%$ away from 24 , but the next higher value, 27 , is not the closest (Fig. 1b).

The algorithm behind the listings creates a short, fast, and accurate routine by using a table, some simple tests, and a trick or two. It takes all values in your computer's floating-point ELECTRONIC DESIGN - PIPS SPECIAL EDITORIAL FEATURE - MAY 23, 1991
range. It will, for example, turn 254489 into 240000 , or 8.642813 $\times 10^{-12}$ into $8.2 \times 10^{-12}$.

To use the subroutine (function), the calling program passes a raw value (RV) and a flag to the routine. The flag selects either $5 \%$ or $10 \%$ tolerance for the answers. The routine returns three properly scaled standard values: one whose tolerance interval ends just below the RV, the one nearest the RV, and one whose tolerance interval ends just above the RV.

To get a standard-value table, the computer can either calculate the entries from rules, or it can initialize them with constants. If calculation is chosen, the process begins with the ideal logarithmic intervals. The values needed are close to $10 \times 10^{\mathrm{n} /}$ ${ }^{24}$ rounded upwards to the next higher integer, where $n$ ranges from zero to 24 . This creates a table of 25 integral values from 10 to 100, but eight table entries
are incorrect: The seven values from 26 to 46 are too low by 1 , and the value 83 is too high by 1 .

A logarithmic interval of $1 /$ 24.03 rather than $1 / 24$ eliminates the rounding error at 83 without affecting other values. Incrementing the calculated values that fall between 26 and 48 fixes the remaining seven errors in the range.

The standard-value-finding algorithm begins with scaling. Because the input number RV may range over many orders of magnitude, it must be mapped into the decade covered by the table. The base-10 logarithm does this job. After taking the $\log$, the integer portion is the decade, while the fractional part represents the digits scaled into the 1 to 10 range ( $10^{0}$ to $\left.10^{0.9999999}\right)$. An antilogarithm restores RV as the product of two numbers, a power multiplier ( $10^{i}$ ) and decimal digits ( $10^{f}$ ). Answers are derived by multiplying table entries by the power multiplier.

The algorithm compares the decimal digits ( $\mathrm{DD}=10^{f}$ ) to entries in the standard-values table. The smallest entry that exceeds DD marks the high end of the interval containing DD. A check against the interval ends determines the entry that's nearest to DD, which is one of the answers being sought.

With the nearest entry found, the two remaining answers can be determined by checking the adjacent tolerance edges. The value of DD may fall within the tolerance range of two entries when the interval is small (Fig. 1a, again). In that case, the entry next to the nearest one is too close $\% 0$ satisfy the guaranteedgreater (or less) criterion. One entry beyond that always has the tolerance margin, however.

The algorithm determines if the entry above the nearest can be used by comparing its tolerance edge to DD. If not, the entry two indices above the nearest is used. A similar procedure
TABIE 1. BASIC ISTILCG
1000 REM EIASTD.BAS 21-Aug-90 JAK 5\% \& 10\% Standard Value Algorithm
1000 REM EIASTD.BAS 21-Aug-90 JAK 5\% \& 10\% Standard Value Algorithm
1010 REM
1010 REM
1020 REM Test Program
1020 REM Test Program
1030 DIM LC(2) :REM last standard choice
1030 DIM LC(2) :REM last standard choice
1040 OPEN "EIASTDB. TBL" FOR OUTPUT AS 1
1040 OPEN "EIASTDB. TBL" FOR OUTPUT AS 1
1050 FORTL $=5$ TO 10 STEP 5
1050 FORTL $=5$ TO 10 STEP 5
$\operatorname{LC}(0)=0: \mathrm{LC}(1)=0: \mathrm{LC}(2)=0:$ PRINT
$\operatorname{LC}(0)=0: \mathrm{LC}(1)=0: \mathrm{LC}(2)=0:$ PRINT
PRINT1, :PRINT1,TL;" \% Tolerance Change Points"
PRINT1, :PRINT1,TL;" \% Tolerance Change Points"
PRINT1," $V$ alue","Lower"," Nearest"," Higher"
PRINT1," $V$ alue","Lower"," Nearest"," Higher"
FOR RV $=81$ TO 1210 STEP $1:$ REM RV $=$ raw value
FOR RV $=81$ TO 1210 STEP $1:$ REM RV $=$ raw value
$A=R V: B=T L / 5: G O S U B 5000$
$A=R V: B=T L / 5: G O S U B 5000$
FORI $=0$ TO2
FORI $=0$ TO2
IF SC(I) < > LC(I) GOTO 1150
IF SC(I) < > LC(I) GOTO 1150
NEXTI
NEXTI
GOTO 1170
GOTO 1170
PRINT "."; :PRINT1,INT(10*RV + .5)/10,SC(0),SC(1),SC(2)
PRINT "."; :PRINT1,INT(10*RV + .5)/10,SC(0),SC(1),SC(2)
FORI $=0$ TO $2: L C(I)=S C(I): N E X T$ I
FORI $=0$ TO $2: L C(I)=S C(I): N E X T$ I
NEXT RV
NEXT RV
NEXT TL
NEXT TL
CLOSE 1
CLOSE 1
END
END
REM
REM
REM Subroutine
REM Subroutine
REM SUBR: Std EIA value; $\operatorname{In}: A=$ raw value, $B=1->5 \%, 2->10 \%$
REM SUBR: Std EIA value; $\operatorname{In}: A=$ raw value, $B=1->5 \%, 2->10 \%$
REM Out $=S C(x): x=0->101=$ nearest $2=$ hi; Chg $C-I, S V(), S V$
REM Out $=S C(x): x=0->101=$ nearest $2=$ hi; Chg $C-I, S V(), S V$
IF SV $=0$ THEN GOSUB 5150 :REM initialize array
IF SV $=0$ THEN GOSUB 5150 :REM initialize array
$C=\operatorname{LOG}(A) / 2.302585: D=\operatorname{INT}(C)-1: E=10^{\circ} D: F=10^{\circ}(C-D)$
$C=\operatorname{LOG}(A) / 2.302585: D=\operatorname{INT}(C)-1: E=10^{\circ} D: F=10^{\circ}(C-D)$
IFB $=1$ THEN H $=.95$ ELSE $H=.9$
IFB $=1$ THEN H $=.95$ ELSE $H=.9$
FOR $G=2+$ B TO 26 STEP B
FOR $G=2+$ B TO 26 STEP B
IF SV(G) $>$ FGOTO 5080
IF SV(G) $>$ FGOTO 5080
NEXT G
NEXT G
IF (SV(G)-F) $>(\mathrm{F}-\mathrm{SV}(\mathrm{G}-\mathrm{B}))$ THEN G $=\mathrm{G}-\mathrm{B}$
IF (SV(G)-F) $>(\mathrm{F}-\mathrm{SV}(\mathrm{G}-\mathrm{B}))$ THEN G $=\mathrm{G}-\mathrm{B}$
$\mathrm{SC}(1)=\mathrm{SV}(\mathrm{G})^{*} \mathrm{E}$
$\mathrm{SC}(1)=\mathrm{SV}(\mathrm{G})^{*} \mathrm{E}$
$\mid F H^{*} S V(G+B)>F T H E N I=B E L S E I=2^{*} B$
$\mid F H^{*} S V(G+B)>F T H E N I=B E L S E I=2^{*} B$
$\mathrm{SC}(2)=\operatorname{SV}(\mathrm{G}+\mathrm{I})^{*} \mathrm{E}$
$\mathrm{SC}(2)=\operatorname{SV}(\mathrm{G}+\mathrm{I})^{*} \mathrm{E}$
IFF $>(2-H)^{*}$ SV $\left(\right.$ G-B) THENI $=B E L S E I=2^{*} B$
IFF $>(2-H)^{*}$ SV $\left(\right.$ G-B) THENI $=B E L S E I=2^{*} B$
$\mathrm{SC}(0)=\mathrm{SV}(\mathrm{G}-1)^{*} \mathrm{E}$
$\mathrm{SC}(0)=\mathrm{SV}(\mathrm{G}-1)^{*} \mathrm{E}$
RETURN
RETURN
REM fill SV() array with 24 EIA standard values; $\mathrm{Chg}=$ SV
REM fill SV() array with 24 EIA standard values; $\mathrm{Chg}=$ SV
DIM SV(28),SC(2)
DIM SV(28),SC(2)
ORSV =0 TO 23
ORSV =0 TO 23
IF SV $>9$ AND SV $<17$ THEN SV $(S V+2)=S V(S V+2)+1$
IF SV $>9$ AND SV $<17$ THEN SV $(S V+2)=S V(S V+2)+1$
IF SV $<3$ THEN SV $(S V+26)=S V(S V+2) * 10$
IF SV $<3$ THEN SV $(S V+26)=S V(S V+2) * 10$
$\operatorname{IFSV}>21$ THEN SV $(S V-22)=\operatorname{SV}(S V+2) / 10$
$\operatorname{IFSV}>21$ THEN SV $(S V-22)=\operatorname{SV}(S V+2) / 10$
NEXT SV
NEXT SV
RETURN
RETURN
40 REM
40 REM
finds the entry that never exceeds DD, the last of the three answers. These comparisons require a table that extends beyond the decade edges.

Finally, the algorithm incorporates a switch for either $5 \%$ or $10 \%$ values. This feature recognizes that the $10 \%$ values are at the even entries in the table. A multiplication by 2 at a few key places does the job.

Before getting to the details of Basic code, two points of Basicprogramming style warrant discussion. For one, the variables A through Z are treated as temporary registers. Their meanings are retained only in their immediate context. In particular, a subroutine may change any of
these variables. On the other hand, two-letter variables are dedicated to single purposes for the whole program. For another, subroutine calls reference a REM statement, not the first line of the routine. This enables lines at the beginning of the routine to be added or deleted without changing all of the callingpoint line references. The REM text can be shortened but should not be removed.

Basic's array initialization uses a Read loop and Data statements. Problems can occur when Data statements must be read several times during the program, as is the case when perusing but not storing the data. In particular, the array initia-

The routines provide the nearest value, the guaran-teed-less-than value, and the guaranteed-greater-than value.

lizers must be read again to get to the other data. To avoid this inconvenience, the routine computes the standard-values table. All initialization procedures are in the subroutine.
The first call to the subroutine (line 5000 ) must run the initialization procedure. Line 5020 accomplishes this by using the variable $S V$. If SV is zero, the initialization procedure executes (lines 5150-5230). The SV flag, like all Basic variables, is set to zero when the program starts. Using SV as the loop counter in line 5170 assures that it'll be nonzero on subsequent subroutine calls. Because the initialization subroutine is called only once, the DIM statements can be executed here.

The table-calculation procedure begins at line 5150 . The For-Next loop repeats lines 5180 and 5190 to calculate 24 standard values in the 10 to 100 decade. The Standard Value array $\operatorname{SV} V_{0}$, however, must extend two values beyond the decade edges, 8.2 to 120 , to reach the guaranteed-greater-than and guaranteed-less-than $10 \%$ values. To accommodate these extra entries, the decade begins at index 2, which makes room for two lower values. Likewise, the indices extend to 28 for the high values. Because the generating function works well only within the decade, line 5200 scales three low values into the upper array, and line 5210 scales two high values into the lower array. The 10 -to- 100 decade allows the most efficient use of the INT() function.

The standard-value-finding subroutine occupies lines 5000 to 5140 . After the initialization check at line 5020 , line 5030 divides the input value, A, into a magnitude multiplier E and decimal digits F. Because standard Basic contains only the natural logarithm function, the identity $\log 10(a)=\ln (a) / \ln (10)$ supplies the base-10 log. Substituting the known value of $\ln (10)$,

## TABLE 2. G ISTING

```
/* put your compiler's headers here */
```

/* put your compiler's headers here */
I* normally, this definition goes in a header file */
I* normally, this definition goes in a header file */
struct toldat {
struct toldat {
double value; /* raw number */
double value; /* raw number */
int tolflg; / * 1 for 5%,2 for 10% */
int tolflg; / * 1 for 5%,2 for 10% */
float lo; /* tolerance edge always below value */
float lo; /* tolerance edge always below value */
float near; /* closest standard value */
float near; /* closest standard value */
float hi; /* tolerance edge always above value */
float hi; /* tolerance edge always above value */
};
};
char fname [] = "EIASTDC.TBL";
char fname [] = "EIASTDC.TBL";
/* Test Program */
/* Test Program */
main()
main()
FILE *fp; /* file pointer */
FILE *fp; /* file pointer */
struct toldat curr,last; /* gen and compare results */
struct toldat curr,last; /* gen and compare results */
if(!(fp= fopen(fname,"w"))) {
if(!(fp= fopen(fname,"w"))) {
fprintf(STDERR, "Writing %s\n",fname);
fprintf(STDERR, "Writing %s\n",fname);
exit(EXIT-FAILURE);
exit(EXIT-FAILURE);
f
f
fprintf(STDERR,"Writing %s n",fname);
fprintf(STDERR,"Writing %s n",fname);
for(curr.tolflg=1; curr.tolflg <3; curr.tolflg + + ) {
for(curr.tolflg=1; curr.tolflg <3; curr.tolflg + + ) {
memset(\&last, 0, sizeof(struct toldat) );
memset(\&last, 0, sizeof(struct toldat) );
fprintf(fp,"\n%d%% Tolerance Change Points<br>mp@subsup{n}{}{\prime\prime},\mp@subsup{5}{}{\star}\mathrm{ curr.tolflg);}
fprintf(fp,"\n%d%% Tolerance Change Points<br>mp@subsup{n}{}{\prime\prime},\mp@subsup{5}{}{\star}\mathrm{ curr.tolflg);}
fprintf(fp," Value Lower Nearest Higher\n");
fprintf(fp," Value Lower Nearest Higher\n");
for( curr.value = 81.0; curr.value < 1210.0; curr.value }+=1.0\mathrm{ ) {
for( curr.value = 81.0; curr.value < 1210.0; curr.value }+=1.0\mathrm{ ) {
eiastd(\&curr);
eiastd(\&curr);
if(memcmp(\&last.lo, \&curr.lo, 3* sizeof(float)) ) {
if(memcmp(\&last.lo, \&curr.lo, 3* sizeof(float)) ) {
fprintf(fp," %9.1f %9. 1f %9. 1f %9. 1f\n", curr.value, curr.lo,
fprintf(fp," %9.1f %9. 1f %9. 1f %9. 1f\n", curr.value, curr.lo,
curr.near, curr.hi);
curr.near, curr.hi);
memmove( \&last.lo, \&curr.lo, 3*sizeof(float) );
memmove( \&last.lo, \&curr.lo, 3*sizeof(float) );
}
}
I
I
}
}
fclose(fp);
fclose(fp);
exit(EXIT-SUCCESS);
exit(EXIT-SUCCESS);
l***}<\mathrm{ eiastd >*** + + + + + + + + + + + + + + + + + + + + + + + + *
l***}<\mathrm{ eiastd >*** + + + + + + + + + + + + + + + + + + + + + + + + *
USE.......Finds nearest standard EIA 5 or 10% value to a real nr.
USE.......Finds nearest standard EIA 5 or 10% value to a real nr.
Enter with: (See struct toldat)
Enter with: (See struct toldat)
value= raw number; tolflg=1 for 5%,2 for 10%
value= raw number; tolflg=1 for 5%,2 for 10%
On return:
On return:
lo= highest tolerance edge is below value
lo= highest tolerance edge is below value
near = nearest standard value
near = nearest standard value
hi= lowest tolerance edge is above value
hi= lowest tolerance edge is above value
OPERATION: See Electronic Design, May 23,1991
OPERATION: See Electronic Design, May 23,1991
RETURNS... Nothing (answers put in struct)
RETURNS... Nothing (answers put in struct)
ERRORS.... None
ERRORS.... None
*/
*/
static float stdtbl[29]={
static float stdtbl[29]={
.82,.91, 1.0,1.1, 1.2, 1.3,1.5, 1.6,1.8,2.0, 2.2, 2.4, 2.7,
.82,.91, 1.0,1.1, 1.2, 1.3,1.5, 1.6,1.8,2.0, 2.2, 2.4, 2.7,
3.0, 3.3, 3.6, 3.9, 4.3, 4.7, 5.1, 5.6,6.2,6.8, 7.5, 8.2, 9.1,
3.0, 3.3, 3.6, 3.9, 4.3, 4.7, 5.1, 5.6,6.2,6.8, 7.5, 8.2, 9.1,
10.0, 11.0, 12.0
10.0, 11.0, 12.0
};
};
static float lotol[3]={0.0,.95,.9};
static float lotol[3]={0.0,.95,.9};
static float hitol[3] ={0.0,1.05,1.1};
static float hitol[3] ={0.0,1.05,1.1};
\#define XOS (dat-> tolfig) /* shorthand for index offset */
\#define XOS (dat-> tolfig) /* shorthand for index offset */
\#define LN10 2.302585
\#define LN10 2.302585
void eiastd(dat)
void eiastd(dat)
struct toldat *dat;
struct toldat *dat;
|
|
double logv; /* log base 10 of raw value */
double logv; /* log base 10 of raw value */
double ilgv; /* int portion of logv */
double ilgv; /* int portion of logv */
float magv; /* value's magnitude multiplier ie 1000,.01 etc */
float magv; /* value's magnitude multiplier ie 1000,.01 etc */
float dgtv; /* digits part of value ie 1.5678,9.123, etc */
float dgtv; /* digits part of value ie 1.5678,9.123, etc */
int nix; /* stdtab array index of nearest value */
int nix; /* stdtab array index of nearest value */
logv = log10(dat-> value); /* split value up */
logv = log10(dat-> value); /* split value up */
ilgv = floor(logv);
ilgv = floor(logv);
magv = (float) exp(LN10*ilgv);
magv = (float) exp(LN10*ilgv);
dgtv = (float) exp(LN10*(logv-ilgv));
dgtv = (float) exp(LN10*(logv-ilgv));
for(nix = 2+XOS; nix < 27; nix += XOS) /* find index of nearest */
for(nix = 2+XOS; nix < 27; nix += XOS) /* find index of nearest */
if( stdtbl[nix]> dgtv )
if( stdtbl[nix]> dgtv )
break;
break;
if( stdtbl[nix]-dgtv > dgtv-stdtbl[nix-XOS] )
if( stdtbl[nix]-dgtv > dgtv-stdtbl[nix-XOS] )
nix -= XOS;
nix -= XOS;
dat-> near = stdtbl[nix]*magv; /* construct answers */
dat-> near = stdtbl[nix]*magv; /* construct answers */
dat-> hi= magv *\
dat-> hi= magv *\
stdtbl[nix + XOS + (dgtv < lotol[XOS]*stdtbl[nix + XOS] ? 0: XOS)];
stdtbl[nix + XOS + (dgtv < lotol[XOS]*stdtbl[nix + XOS] ? 0: XOS)];
dat-> l0= magv *\
dat-> l0= magv *\
stdtbl[nix-XOS-( hitol[XOS]*stdtbl[nix-XOS] < dgtv ? 0: XOS)];
stdtbl[nix-XOS-( hitol[XOS]*stdtbl[nix-XOS] < dgtv ? 0: XOS)];
return;
return;
}
}
{

```
    {
```

    The algorithms
    create a short,
fast, and accu-
rate routine
using a table,
some simple
tests, and a
trick or two.
2.302585 , eliminates the computation delay. By subtracting one from the integer portion of the $\log , \mathrm{D}, \mathrm{F}$ is brought into the table's 10 -to- 100 decade.

The flag, B, switches the computation between $5 \%$ and $10 \%$ tolerance. In most cases, B directly controls indices, but lines 5100 and 5120 require tolerance multipliers ( 1.05 and 0.95 or 1.1 and 0.9 ). These constants could be generated as $1+\mathrm{B} \times 0.05$ and $1-\mathbf{B} \times 0.05$, but the assignment method used at line 5040 eliminates multiplication for a $30 \%$ speed improvement (without a coprocessor).

Lines 5040 to 5070 find the index of the nearest value, and then line 5090 restores the answer to the correct magnitude. Line 5100 finds the guaranteed-greater-than value by testing against the next higher value at its low tolerance (H). The test determines the correct offset, which is either one or two steps (I). Line 5110 restores the magnitude, and lines 5120 and 5130 handle the guaranteed-less-than value in the same manner.

Clarity is another key element when discussing computational efficiency. For clarity, the Basic program uses the form $10^{\mathrm{x}}$ to restore logarithmic values, but $\exp (2.302585 \times x)$ is up to $35 \%$ faster (without a coprocessor). Virtually all Basic interpreters resolve $\mathrm{b}^{\mathrm{x}}$ as $\exp (\log (\mathrm{b}) \times \mathrm{x})$. But because the answer for $\log (\mathrm{b})$ is known in this case, no computation is needed.

The $C$ function eiastd() also implements the standard-valuefinding algorithm (Table 2, again). The name anticipates a sister function, eiapre(), which finds $1 \%$ and $2 \%$ precision values. The C language's strength in data structures teams with efficient use of data types to produce a compact, fast routine. For example, the structure toldat houses both the input parameters and the answers. This has several advantages. It reduces function-call overhead be-

> The C language's strength in data structures teams with efficient use of data types to produce a compact, fast routine.
cause only an address is passed to the function. Furthermore, there's no return value to generate and transfer. The structure also provides the conceptual convenience of having the input and output parameters both defined in one place.

The usual floating-point variable in C is the double, which is typically 8 bytes long with 15 digit precision. Because the shorter 4-byte, 6-digit float type is adequate for choosing $5 \%$ resistors, it offers an opportunity to reduce data sizes and transfer times. But care must be taken because C converts float to double in function calls, and some compilers do all arithmetic in double. When the compiler insists on double, however, the float-conversion delay is usually negligible compared to floatingpoint arithmetic times. The coding assumes a compiler that uses the faster float arithmetic when all variables are in float. In addition to potential speed gains, the smaller float type saves memory space. In one system, using float arrays reduced the function size by $25 \%$.

The function begins with local variable allocation. The variables logv, ilgv, and the structure member dat- $>$ value are double to avoid conversion when they're passed to the math functions. The float variables magv and dgtv match stdtbl's type, which encourages the compiler to do float arithmetic. The structure members lo, near, and high match the float result for conversionless transfer.
The first operations split dat$>$ value into exponent and fraction. C's $\log 10()$ provides the base-10 log while floor() mimics Basic's INT() operation. The base-10 antilogarithms for magv and dgtv could use the C language's power function, $\operatorname{pwr}(10, a)$, but because the natural $\log$ of 10 is a known constant, base-e exponentiation is faster.

After the For loop finds the index of the nearest value, the
answers can be calculated directly. The C condition operator (test?true:false) selects the index shift for the lo and hi results. The TOS index also selects the tolerance factors from initialized constants in arrays lotol and hitol, substituting fast integer indexing for floating-point arithmetic.

The test program, which prefaces each listing, exercises your implementation to detect coding errors and dialect differences. It executes the algorithm at each 1.0 increment between 81 and 1210. When any of the routine's three answers change, it writes a line to the report file. The line contains the input value at which the change occurred and the three associated standard values. The calculation range exceeds the decade by $10 \%$ on each end to check the transition between decades.

The test file reports about 63 changes for $5 \%$ and 31 for $10 \%$. These numbers can vary by $\pm 1$ or so, because the comparisons that trigger a file line use float-ing-point results containing rounding and truncation errors. Calculators, interpreters, or compilers with different float-ing-point representations or rounding algorithms can produce slightly different numbers. However, all systems conforming to the IEEE-754 floatingpoint standard should get the same results.

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# How To Select Shielded And Filtered Connectors For ST? OllS $\begin{aligned} & \text { Many factors must be considered when } \\ & \text { optimizing noise performance. }\end{aligned}$ 

BY FRANK HEBERTAND RANDALLEERHOADS<br>AMP Inc., P.O. Box 3608, Harrisburg, PA 17105-3608; (717) 564-0100.

A11 circuits, cabling, and electronic devices attenuate, reflect transmitted signals, and radiate to some degree. That's why signal-transmission properties and electromagneticinterference and -compatibility (EMI/EMC) issues should be addressed at the system-design level.

Shielding and filtering, used together, give the best protection against both radiated and conducted EMI. Once the right shielded or filtered connector is selected, attention to application details will help maximize the benefits.

Input and output (I/O) ports and cables, a major source of EMI, are a wide-open window for EMI to enter or exit an otherwise tightly shielded box. The cables may act as antennas, particularly when cable lengths approach a quarter-wavelength.

The usual means of suppressing EMI on cables is to shield against radiated noise and filter out conducted noise. In both situations, the connector at each end of the cable contributes significantly in achieving EMC.

Because a primary design goal

1. A good measure of a shield's performance is its transfer impedance. This parameter is defined as the ratio of the longitudinal voltage source in series with the conductors to the shield's surface current. The lower the transfer impedance, the more effective the shielding.


|  | Discrete element |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  | Capacitive |  |  |  |  |
|  | Tubular | Planar | L | $\pi$ or T | Distributed <br> element |
| Insertion loss (dB Max) | 50 | 50 | 70 | $>70$ | $>90$ |
| Slope (dB/decade) | 20 | 20 | $35-40$ | $50-60$ | $>60$ |
| Working voltage (Vdc) | $>500$ | 500 | 500 | 500 | 250 |
| Insulation resistance (G) | 5 | 5 | 5 | 5 | 0.5 |
| Capacitance | 100 pF to | 100 pF to | 100 pF to | 100 pF to | 100 pF to |
|  | $10,000 \mathrm{pF}$ | $0.2 \mu \mathrm{~F}$ | $0.2 \mu \mathrm{~F}$ | $10,000 \mathrm{pF}$ | $10,000 \mathrm{pF}$ |
| Operating voltage (Vdc) | $>200 \mathrm{~V}$ | 200 V | 200 V | 200 V | 100 V |

is the efficient transfer of energy between system components, the decision to either shield or filter must be made in light of overall system design. In an ideal situation, energy isn't lost due to attenuation or radiation, and impedance mismatches aren't causing reflections. In practice, this transfer may be accomplished using high-quality transmission lines for relatively short distances.

Handcuffing crosstalk, maintaining signal fidelity, generating less EMI, and preserving a suitable signal-to-noise ratio were design concerns long before FCC or other regulations came about. As transmission speeds increase in digital systems, so does the difficulty of solving these problems.

Proper grounding is essential to successful EMC design, including grounding of the shielding or filtering. The grounding scheme's continuity determines the shielding system's topology. When the outside and inside of a shielding system are at ground potential and no current flows on its surface, no fields are radiated. Conductors that penetrate apertures, the apertures them-
selves, and interface junctions in the shielding system may degrade performance. It's imperative that EMC-design techniques hold emissions to a negligible level.

A shielded connector must complete a low-impedance link between ground and the chassis. Anything increasing that impedance lowers system effectiveness. Using a strap or pigtail to ground a cable shield is a less satisfactory arrangement, because it creates a high-impedance path.

Shields should be grounded to chassis ground and not to peboard ground. Also, connectors present discontinuities that can boost impedance unless they're properly designed and applied.

A shielded connector that supplies a low-impedance path from the cable shield to ground can be as effective as the cable shielding itself. When discussing the shielding effectiveness of a connector, it's necessary to reference the cable used.

Transfer impedance describes a shield's performance (Fig. 1). The surface currents on the outside of a shield couple energy to the conductors through three

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| :--- | :---: | :---: | :---: | :---: |
| National | 1.18 | -.62 | 1.40 | 1.78 |
| Competitor A | 2.06 | -.66 | 1.10 | 1.83 |
| Competitor B | 1.58 | -.66 | 1.39 | 1.62 |
| Competitor C | 1.46 | -1.08 | 1.09 | 1.56 |

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possible mechanisms. The energy is represented as a longitudinal voltage source in series with the conductors. The ratio of voltage to the surface current is the transfer impedance $Z_{t}$ :
$\mathrm{Z}_{\mathrm{t}}=\mathrm{V}_{\mathrm{i}} / \mathrm{I}_{\mathrm{s}}$
A lower transfer impedance means better shielding, which means less emission from the cable and less induced noise on conductors. One advantage of using transfer impedance to measure a shield's performance is that it's an absolute quantity independent of the measurement system.

The mechanisms that enable the surface currents to couple energy onto the conductor include diffusion, aperture coupling, and junction effects (Fig. 2). Diffusion, which is the natural propagation of electromagnetic energy through a material, is affected by shield material and thickness. Lower conductivity and a thinner shield mean high diffusion. A conductive shield of sufficient thickness reduces diffusion. Material thickness of three skin depths is usually enough.

Skin depth is a frequency-dependent term that expresses the signal-amplitude reduction as the electromagnetic wave passes through material. About $63 \%$ of the signal is attenuated for each

2. Surface currents on a shield couple energy onto conductors through three mechanisms. First, when electromagnetic energy propagates through a shield material, diffusion occurs (a). Also, aperture effects allow capacitive and inductive coupling between a shield and center conductor (b). Finally, the discontinuities caused by joining different components in a shieldedcable assembly give rise to junction effects (c).

> 3. Among the elements of a shielded connector are its metal shell with $360^{\circ}$ ca-ble-shield termination, high-conductivity backshell/shield material, $360^{\circ}$ backshell-to-connector contact, and grounding indents on the connector-mating face.
junction contributes a voltage drop of a magnitude, depending on the quality of contact between materials. Each component must maintain intimate, low-impedance contact with the other components in the chain.

Maintaining a low impedance from cable shield to connector shield requires a $360^{\circ}$ termination (Fig. 3). Most connectors use either a crimp ferrule or a spring-finger arrangement. Pigtail or drain-wire terminations present a high inductance and resistance to high-frequency noise, prevent proper grounding of the shield, and cause the cable to act as a transmitting or receiving antenna.

Discontinuities between mating connector shields are minimized by indents or spring fingers. The resulting spring force is better suited to maintaining a low impedance than the friction fit alone.

Almost any highly conductive material-zinc chromate,

skin depth. For the most common metals, only a few thousandths of an inch thickness is required at higher frequencies to satisfy the three-skin-depths criterion. In cases where only moderate shielding is needed, a thinner shield may be used as long as high conductivity is maintained.

Apertures achieve coupling Apertures achieve coupling
from the shield to the center conductor by means of capacitance and inductive coupling. Typically, braided shield becomes less effective as frequencies rise because the shield apertures are more significant relative to the wavelengths involved. In connectors, shield seams and In connectors, shield seams and
other interfacial features may be apertures.

Junction effects are discontinuities created by the unions of different components in the shielded-cable assembly, such as cable shield to connector shield, cable connector to bulkhead connector, bulkhead connector to panel ground, and so on. Each


(b)
brass, copper alloy, or cast zinc with platings of tin, copper, and nickel-makes a good connector shield. But joining two dissimilar materials should be avoided, because it may cause galvanic corrosion that degrades long-term reliability. For example, a steel ferrule is undesirable because of galvanic corrosion between it and a copper shield. Moreover, aluminum is susceptible to galvanic corrosion unless properly treated. That doesn't mean anodizing, however, despite its cosmetic appeal. Aluminum should be treated with chromate or zinc.

In applications requiring only modest shielding of 30 or 40 dB , shield thickness isn't crucial. Material characteristics are more important than thickness at lower frequencies. Metalplated plastics may work quite well at the higher frequencies.

Filtered connectors for EMI control use low-pass filters built into the connector pins. The most important characteristics of a filter are cutoff frequency and insertion loss as a function of frequency. At the cutoff frequency, which is the frequency at which filtering begins, energy is attenuated 3 dB or $50 \%$. Any frequency below the cutoff point is considered passed, and any frequency above is considered filtered.

Above the cutoff frequency, the insertion loss reaches its maximum. Typical maximum insertion losses run from 20 dB to over 90 dB . The slope of an insertion-loss curve, expressed
in $\mathrm{dB} /$ decade, indicates how steeply over the frequency range the insertion loss moves from the cutoff frequency to maximum attenuation.

Selecting a filtered connector involves knowing the desired cutoff frequency, the amount of insertion loss required and the acceptable insertion-loss curve. While most filters form a network of capacitance, inductance, and sometimes resistance, capacitance is typically the characteristic that is varied to achieve the desired cutoff frequency and maximum insertion loss. More capacitance means a lower cutoff frequency and higher insertion loss. For a capacitor, the cutoff frequency is equal to
$\mathrm{f}_{\mathrm{c}}=\left(\mathrm{R}_{\mathrm{S}}+\mathrm{R}_{\mathrm{L}}\right) / \mathrm{R}_{\mathrm{S}} \mathrm{R}_{\mathrm{L}}(2 \pi \mathrm{C})$
where $R_{S}$ is the source impedance, $R_{L}$ is the load impedance, and $C$ is capacitance. When $R_{S}$ and $R_{L}$ are equal, as in the $50 \Omega$ specified by MIL-STD-220, the formula simplifies to
$\mathrm{f}_{\mathrm{c}}=0.00637 / \mathrm{C}$
Here, capacitance is the sole determiner of cutoff frequency.

Because filtering needs vary and filter design trade-offs are involved, technologies for connector filters have evolved. One option is capacitive filtering, in which a hollow ceramic tube, plated inside and out, forms a simple feed-through capacitor. Capacitances, which range from 100 to $10,000 \mathrm{pF}$, vary with tube length and ceramic material. Ca pacitive filters offer typical slopes
4. Offering very high capacitance, planar capacitors are good alternatives to the tubular capacitors used for connector filtering. One type of planar capacitor uses multilayer construction (a). A second type is based on thick-film technology (b).

of 20 dB /decade and maximum attenuations of 50 dB .

Alternatives to the tubular capacitor are either multilayer or thick-film planar capacitors (Fig. 4). In this case, a planar array slides over the connector pins and is soldered to both the pins and the connector shell. Planar capacitors can pack up to $0.2 \mu \mathrm{~F}$ in a very small area to offer high attenuation at relatively low frequencies.

One drawback in commercial applications is fragility, because the capacitor may crack if the connector is twisted. Military connectors use stronger materials and potting to form a sturdier structure suited to planar arrays.

Another filtering scheme involves lumped-element filters, which use discrete components, such as ferrite beads and tubular capacitors, to form $\mathrm{L}, \mathrm{T}$, or pi networks. The choice of network depends on the circuit in which the filter is used.

For unbalanced networks, L filters offer about 40 dB /decade of loss. The inductor end of the filter must be oriented towards the low impedance. For low-impedance circuits, T filters, which use inductors facing both the source and load with a capacitor to ground, provide about 60 dB / decade of loss. For high-impedance circuits, pi filters use one inductor and two capacitors to ground for $60 \mathrm{~dB} /$ decade of loss.

Lumped-element filters operate reflectively, using impedance mismatches to reflect the highfrequency EMI back to the source. EMI isn't eliminated; it's

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(a)

(b)

simply passed to another part of the system.

System impedance raises another issue. Most manufacturers test filter insertion loss according to MIL-STD-220, which specifies a $50-\Omega$ system impedance. This environment is rarely experienced in practice. Most filters aren't used in $50-\Omega$ systems, and the actual system impedance is often unknown. Insertion loss is frequently unpredictable and, in fact, resonance effects may actually cause "insertion gain." Therefore, insertion loss depends on source and load impedances and the mismatches the filter presents to each. For example, a pi filter's performance improves over test values at impedances over $50 \Omega$ and decreases at impedances under $50 \Omega$.

Distributed-element filters offer the best high-frequency performance, with slopes greater than $60 \mathrm{~dB} /$ decade and insertion losses that can top 90 dB (Fig. 5). The filters use a one-piece sleeve formed of an inner ferrite and outer barium titanate ceramic. The
5. The one-piece dis-tributed-element filter offers the best highfrequency performance with attenuation slopes greater than $60 \mathrm{~dB} /$ decade (a). At low frequencies, the filter appears as a lumped-element RC filter (b). At high frequencies, however, the filter acts as a lossy transmission line (c).

6. A comparison between distributed-element and lumped-element filters clearly shows that the former is less susceptible to impedance variations and resonance effects.
sleeve is plated inside and out. The ferrite is specially formulated to be both conductive and absorptive (lossy). The one-piece construction supplies a distributed inductance (from the ferrite) and capacitance (from the ceramic) that, at high frequencies, acts as a lossy transmission line.

Capacitance reflects the EMI, but the ferrite absorbs it and dissipates it as heat. While some reflections still occur-about 12 dB in a $50-\Omega$ system - most of the insertion loss results from absorption, and typically amounts to 105 $\mathrm{db} / \mathrm{in}$. at 100 MHz . The energy is dissipated rather than passed elsewhere in the system. A comparison of insertion loss for dis-tributed-element and capacitive filters can be shown (Fig. 6).

To select a filter, a designer must know what frequencies need to be passed and what level of attenuation is required for frequencies to be filtered. If high-frequency harmonics of the signal are filtered, the signal's shape will be altered, slowing the rise time.

Because a filter must be well

grounded to maintain a low-impedance noise path, the filter should always be clean and securely grounded to the panel. Installation in a groundplane or bulkhead will prevent energy coupling from input to output.

As mentioned, most filter-in-sertion-loss specifications are based on testing in a $50-\Omega$ system. The greater the system varies from this impedance, the greater the difference in filter perfor-mance-for better or worse. Dis-tributed-element filters are less susceptible to impedance variations than lumped-element T, L, or pi filters.

Because reflective filters don't eliminate EMI, but only reflect it back to the source, the circuit design must account for the noise still in the circuit. Again, this is less a consideration with absorptive distributed-element filters. The characteristics of different filter types can be shown in tabular form (see the table).

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# Variable Resistors Can Take On  

BY RICHARDBOLIN

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In many applications of variable resistors (trimmers, precision and nonprecision panel controls), the goal is to produce a nonlinear control output or taper that's unmatched by any available standard product. Examples include voltage-level controls in power supplies, panel or internal adjustments on test or instrumentation equipment, and some audio controls.
The desired nonlinear output for a number of applications can be created by combining a standard variable-resistance device with a linear taper (a constant rotation versus resistance characteristic over the entire range of rotation) and one or more fixed resistors. This approach can be less costly than specifying a custom variable resistor.
The accompanying illustrations show ten circuits that produce special tapers using conventional linear variable devices and fixed resistors. The tapers are plotted as rotation versus output voltage as a percentage of input voltage. The curves were plotted using Ohm's Law and parallel-resistance calculations.
Four of the figures demonstrate circuit options using standard three-terminal linear potentiometers, either trimmer or panel types. One circuit produces a linear characteristic with a minimum output voltage defined by the value of RF (Fig. 1). Two others use the loading effects of resistors RL to produce nonlinear characteristics (Figs. 2 and 3). The degree of nonlinearity is determined by the ratio RL/RT, with very high values (i.e., in the limit, the

Nonlinear outputs can be created by combining a standard vari-able-resistance device, a linear taper, and one or more fixed resistors.
equivalent of RL being open) producing a linear characteristic and lower values producing increasingly nonlinear characteristics. The curve's concavity or convexity is determined by the configurations of the input and output terminals.

The fourth circuit option, which uses a standard linear device, produces a characteristic that's nonlinear near the ends of the rotation range but nearly linear in the middle portion (Fig. 4). As in the preceding two circuits, the degree of nonlinearity is determined by the ratio RL/ RT, with high values producing a larger linear portion and a moderate degree of nonlinearity at the ends.

The next six circuits use cen-ter-tapped variable resistances. The first produces a curve that resembles an inverted version of the one in Fig. 4 (Fig. 5). However, neither the degree of nonlinearity nor the slope of the linear portion can be varied.

The last five circuits produce various "dual-slope" characteristics. Some have linear portions, while others are totally nonlinear. The curve produced by one of the circuits comprises two linear sections intersecting at the "knee" of the curve (Fig. 7). The knee will always occur at $50 \%$ rotation. But the slope of the first $50 \%$ of rotation, and therefore the percentage of maximum output voltage at which the knee occurs, is determined by the value of RL. Relatively high values will produce a nearly continuous, nearly linear characteristic with only a slight knee. Relatively low values will
produce a shallower slope for the first $50 \%$ of rotation and raise the knee. With proper values, the circuit approaches the logarithmic taper of an audiovolume control.

To show how different values of RL affect linearity, a family of curves was plotted for the circuit of Fig. 8, assuming a value for RT of $10 \mathrm{k} \Omega$ and using values for RL of $5 \mathrm{k} \Omega, 10 \mathrm{k} \Omega$, and $100 \mathrm{k} \Omega$ (Fig. 11). Data points were taken at each $10 \%$ of rotation. The $100-\mathrm{k} \Omega$ value of RL produces a nearly linear plot.
Two points of caution should be observed when using circuits like those described here. First, calculations of the maximum current through both fixed and variable resistances should be made and power ratings for these components chosen accordingly. Second, calculating loading effects on the output of the voltage source should be made for a range of settings.

In summary, it's relatively easy, and in most cases cost-effective, to design a custom nonlinear control solution using standard linear variable resistors and fixed resistors.

Richard Bolin, technical marketing specialist for Bourns Inc., holds a BS degree in engineering technology from Cal Poly University, Pomona, Calif.

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| CIRCLE 302 | (PF) <br> CIRCLE 308 | (LL) (LI) (OI) (PD) (PT) (PR) CIRCLE 314 | (CO) (ST) (MT) (TR) (RN) CIRCLE 320 | Caddock Electronics Inc. 1717 Chicago Ave. |
| AMP Inc. |  |  |  | Riverside, CA 92507 |
| P.O. Box 3608 | Aerovox Inc. | Andersen Laboratories | Bradford Electronics Inc. | (714) 788-1700 |
| Harrisburg, PA 17105-3608 | 370 Faunce Corner Rd. | 1280 Blue Hills Ave. | 550 High St. | (MN) (TF) (HR) (MO) (RN) |
| (800) 522-6752 | North Dartmouth, MA 02747 | Bloomfield, CT 06002 | Bradford, PA 16701-9520 | CIRCLE 326 |
| (PF) (FC) (ON) (EM) (IE) (LL) | (508) 995-8000 | (203) 242-0761 | (814) 362-5635 |  |
| (LI) (OS) (OI) (PT) | (FY) (PF) | (PL) (PF) | (CF) (CE) (MN) (TF) (TH) (GL) | Capar |
| CIRCLE 303 | CIRCLE 309 | CIRCLE 315 | (HR) (MO) (WW) (CH) CIRCLE 321 | P.O. Box 3737 <br> W. Paterson, NJ 07424 |
| AND | Allen Avionics Inc. | Arco Electronics Inc. |  | (201) 239-8183 |
| W. J. Purdy Co. | 224 E. Second St. | 9016 Fullbright Ave. | Brel Int'I Components | (CF) (MN) (MO) (CH) (CD) |
| 770 Airport Blvd. | Mineola, NY 11501 | Chatsworth, CA 91311 | 1621 University Pkwy. | (CM) (EA) (ED) (FP) (FY) (MI) |
| Burlingame, CA 94010 | (516) 248-8080 | (818) 882-8707 | Sarasota, FL 34243 | (CP) |
| (415) 347-9916 | (SU) (PL) (PF) | (CD) (CM) (ED) (FL) (FP) (FY) | (813) 355-9791 | CIRCLE 327 |
| (LL) | CIRCLE 310 | (FT) (MI) (CP) (PL) (PF) | (CF) (CE) (MN) (TF) (HR) |  |
| CIRCLE 304 |  | CIRCLE 316 | (MO) (WW) (CH) (CO) (ST) |  |
|  | Allen-Bradley |  | (MT) (CD) (CM) (EA) (ED) | 237 Sugar Rd. |
| ASC | Elec. Components Div. | Automatic Coil | (EW) (FL) (FP) (FY) (FT) (CN) | Bolton, MA 01740 |
| 302 West O St. | 1414 Allen-Bradley Dr. | 3545 N.W. 71st St. | (CP) (MC) (QC) (CO) | (508) 779-5501 |
| Ogallala, NE 69153 | El Paso, TX 79936-6415 | Miami, FL 33147 | CIRCLE 322 | (ST) (MT) |
| (308) 284-3611 | (915) 592-4888 | (305) 696-6660 |  | CIRCLE 328 |
| (FL) (FP) (FY) (FT) | (CC) (RN) | (AF) (IF) (RF) | CP Clare Corp. |  |
| CIRCLE 305 | CIRCLE 311 | CIRCLE 317 | 107 Audubon Rd. | (see p. 106 for key) |
|  |  |  | Wakefield, MA 01880 | (continued on p. 98) |

## RESSETORS

|  |  |  |
| :---: | :---: | :---: |
| Cermetek Microelec. Inc. | (OS) (OI) | Fountain Valley, CA 92708 |
| 1308 Borregas Ave. | CIRCLE 339 | (714) 963-4009 |
| Sunnyvale, CA 94088-3565 |  | (AF) (IF) (RF) (SU) (MC) (QC) |
| (408) 752-5000 | Dale Electronics Inc. | (SC) (CL) (CO) (TC) (VC) |
| (CF) (TF) (TH) | 1122 23rd St. | (SO) |
| CIRCLE 329 | Columbus, NE 68601 (402) 563-6417 | CIRCLE 350 |
| Clairex Electronics 560 S. Third Ave. <br> Mt. Vernon, NY 10550 <br> (914) 664-6602 <br> (IE) (IS) (LL) (LI) (OS) (OI) <br> (PH) (PC) (PD) (PT) (PR) (UV) <br> CIRCLE 330 | (AU) (CC) (CF) (CR) (CE) | Electro-Films Inc. |
|  | (MN) (TF) (TH) (GL) (HR) | 111 Gilbane St. |
|  | (MO) (WW) (CH) (CO) (ST) | Warwick, RI 02886 |
|  | (MT) (TR) (RN) (AF) (IF) (RF) | (401) 738-9100 |
|  | (SU) (CY) (CK) (SO) | (TH) (CH) (RN) (CP) |
|  | CIRCLE 340 | CIRCLE 351 |
|  |  | Electronic Components Int'l |
| Clarostat Mfg. Co.1 Washington St. | Tempe Div. | 121 Sheldon St. <br> EI Segundo, CA 90245 |
|  | 1155 W. 23rd. St. | (213) 322-7205 |
| Dover, NH 03820-1507 | Tempe, AZ 85282 | (CF) (CO) (CD) (CM) (EA) |
| (603) 742-1120 (AU) (CC) (CR) (CE) (TF) | (602) $967-7874$ (CE) (ST) (MT) | (FP) (FY) (FT) |
| (WW) (CO) (ST) (MT) (TR) | CIRCLE 341 | CIRCLE 352 |
| (OS) |  | Electronic Concepts Inc. |
| CIRCLE 331 | Damon Corp. Electronics Div. | 526 Industrial Way West Eatontown, NJ 07724 |
| Coilcraft | 80 Wilson Way | (908) 542-7880 |
| 1102 Silver Lake Rd. | Westwood, MA 02090 | (FL) (FP) (FY) (FT) (FF) |
| Cary, IL 60013 | (800) 348-0028 | CIRCLE 353 |
| (708) 639-2361 | (CF) (TC) (VC) |  |
| (if) (RF) (SU) (PF)CIRCLE 332 | CIRCLE 342 | Electronic Film Capacitors |
|  |  | Inc |
|  | Data Delay Devices Inc. | 41 Interstate Lane |
| Component Research Co. | 3 Mt. Prospect Ave. | Waterbury, CT 06705 |
| 1655 26th St. | Clifton, NJ 07013 | (203) 755-5629 |
| Santa Monica, CA 90404 | (201) 773-2299 | (FL) (FP) (FY) (FT) (FF) (CN) |
| (213) 829-3615 | (PL) (CK) | CIRCLE 354 |
| CIRCLE 333 | CIRCLE 343 |  |
|  |  | Electronic Precision Components |
|  | Data Display Products 445 S. Douglas St. | 519 S. Fifth Ave. |
| 1865 Selmarten Rd. | EI Segundo, CA 90245-4630 | Mt. Vernon, NY 10550 |
| Aurora, IL 60505-1335 | (213) 640-0442 | (914) 664-2333 |
| (708) 851-4722 | (LL) | (WW) |
| (CY) (TC) (VC) (CK) (SO) | CIRCLE 344 | CIRCLE 355 |
| CIRCLE 334 |  |  |
|  | Datatronics Inc. 28151 Hwy 74 | Florida Branch |
| Cornell-Dubilier Electronics P.O. Box 128 | Romoland, CA 92380 | 3446 E. Lake Rd., Suite 204 |
| Pickens, SC 29671 | (714) 928-7700 | Palm Harbor, FL 34685 |
| (803) 878-6311 | (PL) | 13) 787-6801 |
| (EA) (EW) (FL) (FP) (FY) (MI) | CIRCLE 345 | (EA) (ED) (FP) (CP) CIRCLE 356 |
| (CP) |  | CIRCLE 356 |
| CIRCLE 335 | Dialight Corp. | Engineered Components |
|  | 1913 Atlantic Ave. | Co. |
| Cramer Coil \& Transformer | Manasquan, NJ 08736 | P.O. Box 8121 |
| P.O. Box 200 | (908) 528-8932 | San Luis Obispo, CA 93403 |
| Saukville, WI 53080 | (LL) | (805) 544-3800 |
| (800) 972-9594 | CIRCLE 346 | (PD) |
| (AF) (IF) (RF) (SU) |  | CIRCLE 357 |
| CIRCLE 336 | EG\&G Reticon |  |
|  | 345 Potrero Ave. | Epitaxx Inc. |
| Cree Research Inc. | Sunnyvale, CA 94086 | 3490 U.S. Route 1 |
| 2810 Meridian Pkwy. | (408) $738-4266$ | Princeton, NJ 08540 |
| Durham, NC 27713 | (IS) (UV) | (609) 452-1188 |
| (919) 361-5709 | CIRCLE 347 | (EM) (IE) (IS) (LL) |
| (LL) |  | CIRCLE 358 |
| CIRCLE 337 | EG\&G Vactec |  |
|  | 10900 Page Blvd. | Ericsson Components Inc. |
| Curtis Industries | St. Louis, MO 63132 | 403 International Pkwy. |
| P.O. Box 19910 | (314) 423-4900 | Richardson, TX 75081 |
| Milwaukee, WI 53219 | (IE) (IS) (LI) (OS) (OI) (PH) | (214) 669-9900 |
| (414) 649-4200 | (PC) (PD) (PT) (PR) (UV) | (RN) (EM) |
| (PF) | CIRCLE 348 | CIRCLE 359 |
| CIRCLE 338 |  |  |
|  | ESC Electronics Corp. | FDK America Inc. <br> Fuji Electrochemical Co. |
| D1 Products Inc.95 E. Main St. | 534 Bergen Blvd. |  |
|  | Palisades Park, NJ 07650 |  |
| Huntington, NY 11743 (516) 673-6866 | (800) 631-0853 | Cerritos, CA 90701 |
|  | (AF) (RF) (SU) | (213) 404-1770 |
| (CC) (CF) (MN) (MO) (WW) (ST) (MT) (AI) (CD) (CM) (EA) (FL) (FP) (FY) (FT) (LL) (LI) | CIRCLE 349 | (RF) <br> CIRCLE 360 |
|  | Ecliptek Corp. | (see p. 106 for key) |
|  | 18430 Bandolier Circle | (continued on p. 100) |

## VERTICAL FIXED RESISTORS SAVE PC-BOARD SPACE

A series of compact metal-oxide-film resistors features self-standing, snap-in terminals that save board space. The Series RSS verticalmount resistors exhibit an excellent high-frequency response and low in-

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(FC) (ON)
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(TC) (VC) (SO)
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(PF)
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Frequency Electronics Inc. 55 Charles Lindbergh Blvd. Mitchell Field, NY 11553
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(CL) (CY) (TC) (VC) (CK)

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\& Materials
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Williamsport, PA 17701
(717) 326-6591
(CN) (CP) (QC)
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(LL)
CIRCLE 367
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North Bergen, NJ 07047
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Gowanda Electronics Corp.
1 Industrial PI
Gowanda, NY 14070
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(IF) (RF) (SU)
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Hewlett-Packard Co.
Components Div.
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(ON) (LL) (ㄴII) (OS) (OI)
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P.O. Drawer A

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CIRCLE 371

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Semiconductor \& IC Div.
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(EM) (IE) (LL) (PT)
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Honeywell Optoelectronics 830 Arapaho Rd.
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(PD) (PT) (PR)
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Horizon Capacitor Corp.
2012 W. St. Paul Ave.
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(312) 252-2211
(FL) (FP) (FY) (FT) (FF) (TE)
(CN)
CIRCLE 375
Hycomp Inc.
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Marlborough, MA 01752
(508) 485-6300
(TH) (CH) (RN) (CN)
CIRCLE 376
IDEA Inc.
1300-B Pioneer St.
Brea, CA 92621
(213) 697-4332
(LL) (ㄴII) (PR)
CIRCLE 377
IRC Inc.
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Boone, NC 28607
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(CE) (CO) (CC) (CF) (MN)
(TF) (TH) (GL) (HR) (MO)
(WW) (CH)
CIRCLE 378
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Santa Ana, CA 92705
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(ED) (FL) (FP) (MC) (QC) (CO)
CIRCLE 379

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Lincolnwood, IL 60645
(708) 675-1760
(CD) (EA) (FL) (FP) (FY)

CIRCLE 381
Inductor Supply Inc.
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Orange, CA 92668-1017
(714) 978-2277
(AF) (IF) (RF) (SU) (PL)
CIRCLE 382

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260 Railroad Ave.
Hackensack, NJ 07601
(201) 489-8989
(IE) (IS) (LL) (LI)
CIRCLE 383
Industrial Electronic
Engineers
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Van Nuys, CA 91405
(818) 787-0311
(LL) (OS)
CIRCLE 384
International Mfg. Services
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(401) 683-9700
(AU) (CR) (CE) (TF) (HR)
(CH)
CIRCLE 385
Iskra Electronics Inc.
155 Dupont St.
Plainview, NY 11803
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(CF) (CE) (ST) (MT) (CF) (CE)
(FL) (FP) (FY) (FT)
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Isotek Corp.
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Swansea, MA 02777
(508) 673-2900
(MN) (RN)
CIRCLE 387
Johanson Dielectrics Inc.
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Burbank, CA 91510
(818) 848-4465
(CD) (CM) (OP)

CIRCLE 388
Johanson Mfg. Corp.
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Boonton, NJ 07005
(201) 334-2676
(AI) (CD)
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A Mitsubishi Co.
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Schaumburg, IL 60173-4516
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(TF) (CH) (CD) (CM) (EA)
(ED) (FL) (FP) (FY) (FT) (CN)
(OP) (MC) (QC) (SC) (CL)
(CO) (LL)
CIRCLE 390
KEMET Electronics Corp.
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(CM) (FL) (CP)

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KOA Speer Electronics Inc.
P.O. Box 547

Bradford, PA 16701
(814) 362-5536
(CF) (MN) (TF) (MO) (CH)
(ED)
CIRCLE 392
(see p. 106 for key)
(continued on p. 101)

Kappa Networks Inc.
1443 Pinewood St.
Rahway, NJ 07065
(800) 223-0603
(AF) (IF) (SU)
CIRCLE 393
Ledtronics Inc.
4009 Pacific Coast Hwy.
Torrance, CA 90505
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(LL) (니)
CIRCLE 394
LEMO USA Inc.
335 Tesconi Circle
Santa Rosa, CA 95401
(800) 444-5366
(ON)
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Litton Systems Inc.
Potentiometer Div.
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(914) 664-7733
(CF) (CO) (ST) (MT)
CIRCLE 396
M-Tron Industries Inc.
P.O. Box 630

Yankton, SD 57078
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(CK) (SO)
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10 Commerce Dr.
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(800) 331-1236
(CY) (VC) (CK) (SO)
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(PF) (FY) (FT) (CP)
CIRCLE 399
Marcon America Corp.
998 Forest Edge Dr.
Vernon Hills, IL 60061
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(MO) (CM) (EA) (ED) (FP)
(FY) (CP)
CIRCLE 400
Marktech International Corp.
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Latham, NY 12110
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(EM) (IE) (LL) (LI) (OI) (PD)
(PT) (PR)
CIRCLE 401
Matec Corp.
Valpey-Fisher
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Hopkinton, MA 01748
(508) 435-6831
(MC) (QC) (SC) (CO) (TC)
(VC) (CK) (SO) (FC)
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(FC)
CIRCLE 403

McCoy Electronics Co.
P.O. Box B

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(QC) (SC) (CL) (CO)
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Mepcopal Co.
11468 Sorrento Valley Rd.
San Diego, CA 92121
(619) 453-0332
(CE) (WW) (ST) (MT)
CIRCLE 405
Micro Crystal Div./SMH
35 E. 21st St.
New York, NY 10010
(212) 505-5340
(MC) (QC) (CO)

CIRCLE 406
Micro Ohm Corp.
1088 Hamilton Rd
Duarte, CA 91010
(818) 357-5377
(CF) (CR) (MN) (TF) (HR)
(MO) (WW)
CIRCLE 407
Micro Switch
Div. of Honeywell

11 W . Spring St.
Chicago, IL 61032
(815) 235-5731
(EM) (IS) (LL) (LI) (OS) (PD)
(PT) (PR)
CIRCLE 408
Microtran Co. Inc.
P.O. Box 236

Valley Stream, NY 11582
(516) 561-6050
(SU)
CIRCLE 409
Microwave Filter Co
6743 Kinne St.
East Syracuse, NY 13057
(800) 448-1666
(PF)
CIRCLE 410
Milwaukee Resistor Corp.
700 West Virginia St.
Milwaukee, WI 53204-0219
(414) 271-9900
(WW)
CIRCLE 411
Mini-Circuits
P.O. Box 350166

Brooklyn, NY 11235-0003
(718) 934-4500
(PF)
CIRCLE 412
Mini-Systems Inc.
20 David Rd.
North Attleboro, MA 02760
(508) 695-0203
(TF) (TH) (HR) (CH) (RN)
(CP) (CN) (SU)
CIRCLE 413
Mitsubishi International
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New York, NY 10022
(212) 605-2392
(FC) (ON) (EM)
CIRCLE 414

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Semiconductor Prods.
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Phoenix, AZ 85008
(602) 244-3955
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State College, PA 16801
(814) 237-1431
(HR) (CH) (AI) (CD) (CM)
(VA) (CN) (OP) (IF) (RF) (SU)
(CL) (CO)

CIRCLE 416
NDK America Inc.
20300 Stevens Creek Blvd.
Cupertino, CA 95014-2210 (408) 255-0831
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(TC) (VC) (CK) (SC)
CIRCLE 417
NEC Electronics Inc.
401 Ellis St., Box 7241
Mountain View, CA 94039
(415) 960-6000
(ED) (CP) (FC) (ON) (EM) (IE)
(IS) (LI) (OI) (PD) (PT) (PR)
CIRCLE 418
NEL Frequency Controls
357 Beloit St.
Burlington, WI 53105
(414) 763-3591
(MC) (QC) (SC) (CY) (CK)
(SO)
CIRCLE 419
NIC Component Corp.
6000 New Horizons Blvd.
North Amityville, NY 11701
(516) 226-7500
(CD) (CM) (EA) (ED)

CIRCLE 420

## NSG America

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(201) 469-9650
(FC) (ON) (EM) (IE) (OS) (OI)
CIRCLE 421
NTE Electronics Inc.
44 Farrand St.
Bloomfield, NJ 07003
(201) 748-5089
(MN) (MO) (WW) (CD) (EA)
(ED) (MC) (QC) (IE) (IS) (LL)
(LI) (OI) (PD) (PT) (PR)

CIRCLE 422
Nichicon (America) Corp.
927 E. State Pkwy.
Schaumburg, IL 60173
(708) 843-7500
(EA) (FP) (FY)
CIRCLE 423
Noble U.S.A. Inc.
5450 Meadowbrook Ind. Ct. Rolling Meadows, IL 60008 (708) 364-6038
(CF) (CE) (MO) (WW) (ST)
(MT) (TR) (FY) (FT)
CIRCLE 424
(see p. 106 for key)
(continued on p. 102)


## METAL-FILM RESISTORS BOAST HIGH PRECISION

Low inductance and high stability are keys to the RN25 series of metalfilm resistors. The devices are the same size as the MIL RN55 resistor. Tolerances of $0.5 \%, 0.25 \%$, and $0.1 \%$ are available, as are temperature coefficients of 100,50 , and 25 ppm . Prices range from $\$ 0.021$ to $\$ 0.65$ depending on quantity, TC, and tolerance. Minimum quantity per value is 100 pieces. Delivery is in four weeks.

## Micro-Ohm Corp.

1088 Hamilton Rd.
Duarte, CA 91010
(818) 357-5377

- CIRCLE 574


## PRECISE CHIP RESISTOR POSTS PERFORMANCE GAIN

An order-of-magnitude performance gain compared with other chip resistors is claimed for the VSM Style
metal-foil chip resistors. The ultraprecise chips exceed the requirements of MIL-R-55342, characteristic Y. Maximum TCR is $5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ over the full military temperature range. In lots of 100 , the $1-\mathrm{k} \Omega, 0.02 \%$ version costs $\$ 4.33$ with delivery in four to six weeks.

## Vishay Bulk Metal Resistors <br> 63 Lincoln Highway <br> Malvern, PA 19355 <br> (215) 644-1300

## - CIRCLE 575

## POWER FILM RESISTORS COME IN TO-220 CASE

A proven power-resistance film is incorporated into the widely accepted TO-220 power package in the Type MP Kool-Tab power film resistor. Resistance range is from $1 \Omega$ to 10 $\mathrm{k} \Omega$ with standard tolerance of $\pm 1 \%$. The model MP820, a $50-\Omega, 1 \%$ resistor, costs $\$ 1.89$ in lots of 1000 . Deliv-

ery is in six weeks. Caddock Electronics Inc. 1717 Chicago Ave. Riverside, CA 92507 (714) 788-1700

- CIRCLE 576

| PASSTIE-GOMPONENT MANUFAGURERS |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Nytronics Components | Sepulveda, CA 91343 | Carlisle, PA 17013 | (AF) (RF) | (CF) (CR) (MN) (TF) ( |
| Group Inc. | (818) 892-0761 | (717) 249-2151 | CIRCLE | (HR) (MO) (WW) (CH) (CO) |
| 700 Orange St. | (TH) (RF) | (MC) (QC) (SC) (CO) (TC) |  | (CD) (CM) (EA) (ED) (EW) |
| Darlington, SC 29532 (803) 393-5421 | CIRCLE 431 | (VC) CIRCLE 436 | Pulse Engineering P.O. Box 12235 | (FL) (FP) (FY) (MI) (CP) (CN) CIRCLE 448 |
| (WW) (FL) (FP) (FY) (FT) (RF) | Pacific Coil Co. |  | San Diego, CA 92112 |  |
| (PL) (SU) | Div. of Inductor Supply | Piezo Technology Inc. | (619) 268-2544 | Rogers Corp. |
| CIRCLE 425 | 430 E . 19th St. | P.O. Box 547859 | (IF) | One Technology Dr. |
|  | Bakersfield, CA 93305-5495 | Orlando, FL 32854-7859 | CIRCLE 443 | Rogers, CT 06263 |
| Ohmite Mfg. Co. Div. of N.A. Philips | (800) 332-2645 | (407) 298-2000 |  | (203) 774-9605 |
|  | (AF) (IF) (RF) (SU) | (QC) (SC) (CL) (CY) (TC) | Q-Tech Corp. | (CM) (CP) |
| 3601 Howard | CIRCLE 432 | (VC) (CK) (SO) | 10150 W. Jefferson Blva. | CIRCLE 449 |
| Skokie, IL 60076 (312) 675-2600 | Panasonic Industrial Co | CIRCLE 437 | Culver City, CA 90232-3510 (213) $836-7900$ | Rogers Corp. |
| (CC) (CF) (MN) (HR) (W | Elec. Comp. Div. | Piher International Corp. | (GC) (SC) (CY) (VC) (CK) | Circuit Components Div. |
| CIRCLE 426 | Two Panasonic Way | 903 Feehanville Dr. | (SO) | 2400 S. Roosevelt St. |
| Ohmtek Inc. | Secaucus, NJ 07094 (201) 348-206 | Mount Prospect, IL 60007 (708) 390-6680 | CIRCLE 444 | Tempe, AZ 85282 (602) 967-0624 |
| 2160 Liberty Dr. | (CF) (CE) (MN) (TF) (MO) | (CF) (MN) (MO) (WW) (CH) | RCD Components Inc. | (CD) (CM) |
| Niagara Falls, NY 14304 | (WW) (CH) (ST) (MT) (TR) | (ST) (TR) (CM) | 520 E. Industrial Park Dr. | CIRCLE 450 |
| (716) 283-4025 | (RN) (CD) (CM) (EA) (ED) | CIRCLE 438 | Manchester, NH 03103 |  |
| (TF) (TH) (HR) (CH) | (FF) (FY) (FF) (CP) (AF) (IF) |  | (603) 669-0054 | Rohm Corp. Rohm Electronics Div, |
| CIRCLE 427 | (RF) (SU) (PF) (QC) (CY) (VC) CIRCLE 433 | Pletronics Inc. 9026 Roosevelt Way N.E. | (AU) (CF) (CR) (CE) (MN) (TF) (TH) (GL) (HR) (MO) | Rohm Electronics Div. 8 Whatney |
| Opt Industries Inc. |  | Seattle, WA 98115 | (WW) (CH) (CO) (RN) (CN) | Irvine, CA 92718 |
| 300 Red School Lane | Panasonic Industrial Co. | (206) 523-9395 | (AF) (IF) (RF) (SU) (PL) | (714) 855-2131 |
| Phillipsburg, NJ 08865 | Semiconductor SIs. Div. | (MC) (QC) (SC) (CO) (CK) | CIRCLE 445 | (AU) (CF) (CR) (MN) (TF) |
| (201) 454-2600 | 1616 McCandless Dr. | (so) |  | (GL) (HR) (MO) (CH) (ST) |
| (AF) (CL) | Milpitas, CA 95035 | CIRCLE 439 | Raltron Electronics Corp. | (TR) (RN) (CD) (CM) (CP) (IE) |
| CIRCLE 428 | (408) $945-5675$ <br> (ON) (EM) (IE) (IS) (LL) | Polara Engineerin | 2315 N.W. 107th Ave. Miami FL 33172 | (IS) (LL) (LI) (OS) CIRCLE 451 |
| Optek Technology In | (OS) (OI) (PT) (PR) | 4115 Artesia Ave | (305) 593-6033 |  |
| 1215 W. Crosby Rd. | CIRCLE 434 | Fullerton, CA 92633 | (RN) (CN) (MC) (QC) (SC) | Senisys |
| Carrollton, TX 75006 |  | (714) 521-0900 | (CL) (CY) (TC) (VC) (CK) | 1600 W. Plano Pkwy. |
| (214) 323-2447 | Philips Components | (AF) (IF) (RF) (SU) | (SO) | $\begin{aligned} & \text { Plano, TX } 75075 \\ & \text { (214) 422-1844 } \end{aligned}$ |
| (EM) (IE) (IS) (LI) (OS) (OI) | 2001 W. Blue Heron Blvd. | CIRCLE 440 | CIRCLE 446 | (IE) (IS) (LI) (OS) (OI) (P) |
| (PD) (PT) (PR) CIRCLE 429 | Riviera Beach, FL 33404 (407) 881-3308 |  |  | (PT) (PR) |
|  | (CR) (CE) (MN) (TF) (TH) | 470 E. Main St. | 60 Jefryn Blvd. E. | CIRCLE 452 |
| Opto Diode Corp. | (HR) (MO) (WW) (CH) (ST) | Lake Zurich, IL 60047-2578 | Deer Park, NY 11729 |  |
| 750 Mitchell Rd. | (MT) (TR) (RN) (CD) (CM) | (708) 438-4000 | (516) 586-5566 | SI Tech |
| Newbury Park, CA 91320 | (EA) (ED) (EW) (CP) (CN) | (CF) (CE) (TF) (TR) | (AF) (IF) (RF) (SU) | Geneva, IL 60134 |
| (805) 499-0335 | (QC) (CY) (TC) (VC) (CK) (IS) | CIRCLE 441 | CIRCLE 447 | (312) 232-8640 |
| (LI) ${ }_{\text {CIRCLE }} 430$ | (OI) (PT) ${ }_{\text {Cl }}$ |  |  | (FC) (ON) (EM) |
| CIRCLE 430 | CIRCLE 435 | Prem Magnetics Inc. 3521 N. Chapel Hill Rd. | Robert G. Allen Co. <br> 7267 Coldwater Canyon | CIRCLE 453 |
| PCA Electronics Inc. 16799 Schoenborn St. | Piezo Crystal Co. $100 \mathrm{~K} \mathrm{St}$. Box 619 | McHenry, IL 60050 (815) 385-2700 | North Hollywood, CA 91605 (818) 765-8300 | (see p. 106 for key) |

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CIRCLE 118

## TANTALUM CHIP CAPS WITHSTAND SOLDER HEAT



Designed specifically for surface mounting directly to pe boards or alumina substrates, the T491 series of precision molded tantalum chip capacitors withstands a variety of processes. The chips can be wave soldered, infrared reflowed, or vaporphase soldered. Values range from $0.1 \mu \mathrm{~F}$ to $150 \mu \mathrm{~F}$ with $\pm 10 \%$ and $\pm 20 \%$ tolerances available. Working voltages range from 4 to 50 V dc. Call
for pricing and delivery. Kemet Electronics Corp. P.O. Box 5928 Greenville, SC 29606 (803) 963-6300

- CIRCLE 577


## METALLIZED POLY CAPS ARE COST-EFFECTIVE

A line of tape-wrapped axial capacitors boast a design that's both miniaturized and cost-effective. The Types X465 and X467 capacitors are polycarbonate devices that operate from -55 to $+125^{\circ} \mathrm{C}$. Both series are rated at $50,100,200$, and 400 V dc and offer tolerances from $\pm 1 \%$ to $\pm 10 \%$. Applications include pulse circuits. Call for pricing and delivery.

ASC Capacitors<br>301 West O St.<br>Ogallala, NE 69153<br>(308) 284-3611

- CIRCLE 578


## ELECTROLYTIC CAPS MOUNT EASILY TO PCBs

Quick, efficient attachment to pc boards is provided by the type LBA snap-mount capacitors. The aluminum electrolytic caps are meant for use in conventional and switch-mode

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Illinois Capacitor Inc.<br>3757 W. Touhy Ave.<br>Lincolnwood, IL 60645<br>(708) 675-1760<br>- CIRCLE 579

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Union, NJ 07083
(908) 851-0644
(PF)
CIRCLE 455
Seacor Inc.
123 Woodland Ave.
Westwood, NJ 07675
(201) 666-5600
(FL) (FP) (FY) (FT) (CN)
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Seiko Instruments U.S.A.
Fiber Optic Comp. Div.
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(QC) (CO) (TC) (FC) (ON)
(EM) (LL)
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Sharp Electronics Corp.
Microelectronics Div.
Sharp Plaza, P.O. Box 650 Mahwah, NJ 07430
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(EM) (IE) (IS) (LL) (LI) (OS)
(OI) (PT) (PR)
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Shelly Associates
14811 Myford Rd.
Tustin, CA 92680
(714) 669-9850
(LL)
CIRCLE 459

Shogyo International Corp. 287 Northern Blvd.
Great Neck, NY 11021-4799 (516) 466-0911
(CC) (CF) (MN) (WW) (ST)
(AF) (IF) (RF) (LL) (PH)
CIRCLE 460
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Peekskill, NY 10530
(914) 736-5531
(CC) (CF) (CR) (CE) (MN)
(MO) (WW) (CH) (CO) (ST)
(MT) (TR) (RN) (CD) (EA)
(FP) (FY) (FT) (FF) (MI) (CP)
(CN) (AF) (IF) (RF) (SU) (QC) (CL) (CY) (EM) (IE) (IS) (LL) (LI) (OI) (PH) (PC) (PD) (PT)
(PR) (UV)
CIRCLE 461
Siecor Electro-Optic
Products
P.O. Box 13625

Research Triangle Park,
NC 27709
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(FC) (ON)
CIRCLE 462
Siemens Components Inc.
Special Prods. Div.
186 Wood Ave. South
Iselin, NJ 08830
(908) 906-4376
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## (SU)

CIRCLE 463
Siemens Components Inc.
Optoelectronics Div.
19000 Homestead Rd.
Cupertino, CA 95014
(408) 725-3524
(LL) (LI)
CIRCLE 464

Silicon Detector Corp. 1240 Avenida Acaso Camarillo, CA 93012 (805) 484-2884
(EM) (IE) (IS) (LL) (LI) (PH) (PC) (PT) (PR) (UV) CIRCLE 465

Silicon Sensors Inc.
Old Hwy. 18 East
Dodgeville, WI 53533
(608) 935-2707
(CE) (IE) (IS) (LL) (LT) (OS)
(OI) (PH) (PC) (PD) (PT)PR) (UV)
CIRCLE 466
Solitron Devices Inc. Semiconductor Div.
1177 Blue Heron Blvd.
Riviera Beach, FL 33404
(407) 848-4311
(CR) (CE) (TH) (CH) (TR)
(RN)
CIRCLE 467
Spectrum Control Inc.
2185 W. Eighth St.
Erie, PA 16505
(814) 455-0966
(CD) (CM) (CP) (CN) (CY)
(TC) (VC) (SO)
CIRCLE 468
Spectrum Technology Inc.
P.O. Box 948

Goleta, CA 93116
(805) $964-7791$
(QC) (SC) (CO) (TC) (VC)
CIRCLE 469
Sprague Electric Co.
Distribution Div.
P.O. Box 9102

Mansfield, MA 02048-9102
(508) 339-8900
(RN) (CD) (CM) (EA) (ED)
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## CIRCLE 470

Sprague-Goodman
Electronics
134 Fulton Ave.
Garden City Park, NY 11040
(516) 746-1385
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Stackpole St.
St. Marys, PA 15857
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(HR)
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9940 E. Baldwin PI.
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(CK) (SO)
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State of the Art Inc.
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State College, PA 16803-1797 (814) 355-8004
(TF) (TH) (HR) (SU)
CIRCLE 474
Statek Corp.
512 N. Main St.
Orange, CA 92668
(714) 639-7810
(MC) (QC) (SC) (CY) (CK)
(SO)
CIRCLE 475
TDK Corporation

## of America

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Mount Prospect, IL 60056
(708) 803-6100
(SU)
CIRCLE 476
TEW North America
5903-B Peachtree Ind. Blvd.
Norcross, GA 30092
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(TC) (VC) (CK) (SO)
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Tecate Industries Inc.
P.O. Box 711509

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(CD) (CM) (EA) (ED) (EW)
(FL) (FP) (FY) (FT) (CG) (MI)
(CP)
CIRCLE 479
Texas Instruments
Semiconductor Group
P.O. Box 809066

Dallas, TX 75380-9066
(214) 995-6611
(EM) (IE) (IS) (LL) (LT) (OS)
(OI) (PH) (PC) (PT) (PR) (UV)
CIRCLE 480
The Carborundum Co. Electric Products Div.
3425 Hyde Park Blvd.
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CIRCLE 481
(see p. 106 for key)
(continued on p. 106)


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Model

|  | Output \#1 | Output \#2 | Output \#3 | Output \#4 |
| :---: | :---: | :---: | :---: | :---: |
| MAX-353-0512 | +5V @ 50A | +12V @ 8/12Apk | -12V @ 4.0A | - |
| MAX-354-1205 | +5V @ 50A | +12V @ 8/12Apk | -12V @ 4.0A | -5.2 @ 2.0A |
| MAX-354-1212 | +5V @ 50A | +12V @ 8/12Apk | -12V @ 4.0A | 12V @ 2.0A |
| MAX-354-1224 | +5V@50A | +12V @ 8/12Apk | -12V@ 4.0A | +24V@1.5A |
| Model | 400,500 WATTS: 2.5 " $\times 5$ " $\times 11.5$ "* |  |  |  |
| MSC-402-0512 | +5V @ 20A | +12V @ 25/36Apk | - | - |
| MAX-503-0512 | +5V @ 80A | +12V @ 10/16Apk | -12V@ 10.0A | - |
| MAX-504-1252 | +5V @ 80A | +12V @ 10/16Apk | -5.2V@10.0A | 12V@2.OA |
| MAX-504-1205 | +5V @ 80A | +12V @ 10/16Apk | -12V @ 10.0A | 5.2V@2.0A |
| MAX-504-1212 | +5V @ 80A | +12V @ 10/16Apk | -12V@10.0A | 12V@2.0A |
| MAX-504-1224 | +5V @ 80A | +12V @ 10/16Apk | -12V @ 10.0A | +24V@2.0A |
| MAX-504-1552 | +5V@80A | +15V @ 10/16Apk | -5V @ 10.0A | 15V@2.0A |
| Model | 700,750 WATTS: 2.5 " $\times 5$ " $\times 13.6$ "* |  |  |  |
| MAX-704-1205 | +5V @ 100A | +12V @ 12/20Apk | -12V@10.0A | 5.2V@2.OA |
| MAX-704-1212 | +5V @ 100A | +12V @ 12/20Apk | -12V@10.0A | 12V@2.0A |
| MAX-753-0512 | +5V @ 120A | +12V @ 12/20Apk | -12V @ 10.0A | - |
| MSC-753-0512 | +5V @ 120A | +12V @ 20/27Apk | -12V@ 6.0A | - |
| MAX-754-1252 | +5V @ 120A | +12V@12/20Apk | -5.2V@10.0A | 12V@2.OA |
| MAX-754-1205 | +5V @ 120A | +12V @ 12/20Apk | -12V@10.0A | 5.2V@2.OA |
| MAX-754-1212 | +5V @ 120A | +12V @ 12/20Apk | -12V@10.0A | 12V @ 2.0A |
| MAX-754-1224 | +5V @ 120A | +12V @ 12/20Apk | -12V @ 10.0A | +24V@2.0A |

*Size for system air-cooled versions.

## POLYSTYRENE, FOIL CAPS SUIT LC-FILTER TASKS

The SFSR series of polystyrene and foil capaciors, with its stringent specs for precision, stability, humidity, dissipation factor, and reliability, are suited for use in LC filters. The series offers a broad value range of from 100 to $330,000 \mathrm{pF}$ and toler-

ances down to $\pm 0.5 \%$. Their dissipation factor is lower than $4 \times 10^{-4}$, and their linear temperature coefficient is $150( \pm 50) \mathrm{ppm} /{ }^{\circ} \mathrm{C}$. The devices are encased in a rectangular, epoxy-encapsulated, flame-retardant case with sturdy tinned solder-coated leads. Call for pricing and delivery.

## Seacor Inc.

123 Woodland Ave.
Westwood, NJ O767f5
(201) 666-5600

- CIRCLE 580


## SNUBBER MICA CAPS MAKE SWITCHERS BETTER



A line of snubber mica capacitors is well suited for snubber circuits in switch-mode power supplies and other applications where reliable transient suppression is crucial. The "Snubber Mike" capacitors' mica dielectric gives a $75 \%$ lower impedance at resonance than that of ceramic disks and 20 times the dV/dt capability of polypropylene foil/film capacitors. The capacitors reduce heating and improve reliability with a low dissipation factor. In lots of 1000 ,
prices start at \$0.09. Delivery is from stock to 12 weeks.

Cornell Dubilier Electronics
1700 Rte. 23 North
Wayne, NJ07470
(201) 694-8600

- CIRCLE 581


## - MINI FILM CAPACITORS SUIT SWITCH-MODE TASKS



A series of MIL-quality, metallized-polycarbonate-film capacitors features a $50 \%$ smaller package than standard capacitors with no sacrifice in performance. The 5MC capacitors are specifically designed for switchmode power applications. Five available configurations include axial leads with tab terminations in high or low profile, and internal coaxial leaded with or without grounded copper shielding. Call for pricing and delivery.

## Electronic Concepts Inc.

## P.O. Box 1278

Eatontown, NJ 07724
(201) 542-7880

- CIRCLE 582


## FILM CHIP CAPACITORS COME IN TWO GRADES

Industrial and commercial grades are available for a line of chip-style film capacitors. The ECH-U industrial units are size 1206 ( 3.2 by 1.6 mm ) and use polyphenyline sulfide film as the dielectric. Their capacitance range is from 0.00047 to $0.047 \mu \mathrm{~F}$ in tolerances of $\pm 2 \%$ and $\pm 5 \%$. The ECW-U commercial version is size 1210 ( 3.2 by 2.5 mm ). Its range is from 0.00047 to $0.10 \mu \mathrm{~F}$ at $\pm 5 \%$ tolerance. Uses include timing circuits. Call for pricing and delivery.

Panasonic Industrial Co.
Two Panasonic Way
Secaucus, NJ 07094
(201) 348-5205

- CIRCLE 583


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- Solvent Tolerant Seal Std.
- Tape \& Reel Available


Type CKR Subminiature radial lead aluminum electrolytic capacitors are the up-to-date choice for industrial and commercial designs requiring continuous duty performance in a smaller case. Featuring new high gain etched foil, type CKR provides greater CV per case size category. The extended endurance rating of 2000 hrs. at $+85^{\circ} \mathrm{C}$ offers the user significant product life extension. Leakage current of $\leq 0.006 \mathrm{CV}$ or $2 \mu \mathrm{~A}$ min. is comparable to many competitive "low" leakage capacitors. The use of modern materials and fabrication technology combine together to produce type CKR at a cost competitive affordable price. Type CKR is widely used in original designs and for industrial replacement applications. Perfecı as a filter or coupling capacitor, type CKR finds application in a wide range of products including avionics, computers, entertainment, telecommunications, instrumentation, telemetry, etc. Type CKR is the standard for top quality performance at an affordable price.


CIRCLE 81

## CIPRGITORS

## THIN CERAMIC CAPS CAN MOUNT UNDER PLCCs

A line of very thin $(0.020-\mathrm{in}$. maximum) multilayer ceramic capacitors is capable of being surface-mounted under a plastic leaded chip carrier (PLCC). The MLCs can also be used on multichip modules. Four EIA sizes are offered: $0805,1206,1210$, and 1812. Capacitances range from 0.01 to $0.03 \mu \mathrm{~F}$. Two dielectric grades are available as well: Z 5 V for gener-al-purpose applications requiring a

higher dielectric constant, and X7R for capacitance stability in temperature extremes. Typical pricing is $\$ 0.15$ in OEM quantities. Delivery is from stock to eight weeks.

## Rogers Corp.

Circuit Components Div. 2400 S. Roosevelt St. Tempe, AZ 85282 (602) 967-0624

## - CIRCLE 584

## BOX CAPACITORS SUPPRESS INTERFERENCE

The type MEY box capacitors are suited for use in line-bypass, antenna coupling, across-the-line, and sparkkiller circuits. The metallized polyes-ter-film capacitors are offered in values from 0.001 to $0.047 \mu \mathrm{~F}$ and in tolerances of $\pm 5 \%, \pm 10 \%$, and $\pm 20 \%$. The units feature non-inductive construction and excellent self-healing properties. Other features include high moisture resistance and good

solderability. Their flame-retardant case meets UL 94V-O. Pricing starts at $\$ 0.13$ in lots of 1000 . Delivery is from stock to eight weeks.

Tecate Industries Inc.
P.O. Box 711509

Santee, CA 92072
(619) 448-4811

- CIRCLE 585


## PISSIVE-GOMPONENT MANUFGTURERS

Thermometrics Inc.
808 U.S. Hwy. 1
Edison, NJ 08817
(201) 287-2870
(SU)
CIRCLE 482

Theta-J Corp.
107 Audubon Rd.
Wakefield, MA 01880
(617) 246-4000
(OS) (OI) (PD) (PT) (PR)
CIRCLE 483
Thomson Passive
Component Corp.
P.O. Box 4051

Woodland Hills, CA 91367
(818) 887-1010
(CD) (CM) (ED) (FP) (FY) (FT)
(CN) (CP)
CIRCLE 484

## Time \& Frequency Ltd.

55 Charles Lindbergh Blvd. Mitchell Field, NY 11553
(516) 794-4500
(MC) (QC) (CL) (CO) (TC)
(VC)
CIRCLE 485

Tocos America
565 W. Golf Rd.
Arlington Heights, IL 60005
(708) 364-7277
(ST) (TR) (PC)
CIRCLE 486

Toko America Inc.
1250 Feehanville Dr
Mount Prospect, IL 60056
(708) 297-0070
(AF) (IF) (RF) (SU) (PL) (PF)
CIRCLE 487

Toshiba America Inc. Semiconductor Operation 9775 Toledo Way Irvine, CA 92718 (714) 455-2000 (LL) (OS) (OI) (PD) (PT) (PR) CIRCLE 488

Toyocom U.S.A. Inc.
617 E. Gold Rd., Suite 112 Arlington Heights, IL 60005 (708) 593-8780
(MC) (QC) (SC) (CL) (CY)
(TC) (VC) (CK) (SO)
CIRCLE 489

Ultronix Inc.
P.O. Box 1090

Grand Junction, CO 81502
(303) 242-0810
(WW) (CH) (CE) (ST) (MT)
CIRCLE 490
United Chemi-Con Inc. 9801 W. Higgins Rd. Rosemont, IL 60018
(312) 696-2000
(TH) (EA) (CP)
CIRCLE 491
Valpey-Fisher Corp.
75 South St.
Hopkinton, MA 01748
(800) 982-5737
(MC) (QC) (SC) (CO) (TC)
(VC) (SO)
CIRCLE 492

Vectron Laboratories Inc.
166 Glover Ave.
Norwalk, CT 06850
(203) 853-4433
(CY)
CIRCLE 493


Victoreen Inc.
6000 Cochran R
Cleveland, OH 44137
(216) 248-9300
(TF) (GL) (HR) (MO)
CIRCLE 494
Victory Engineering
P.O. Box 559

Springfield, NJ 07081
(201) 379-5900

CIRCLE 495
Vishay Bulk Metal Resistors

## 63 Lincoln Hwy.

Malvern, PA 19355-2110
(215) 644-1300
(TH) (CH)
CIRCLE 496
Voltronics Corp.
P.O. Box 476

East Hanover, NJ 07936
(201) 887-1517
(CC) (CF) (TF) (HR) (CO) (ST)
(AI) (CG) (TE)
CIRCLE 497

## Wavetek Corp. RF Products Div.

 5808 Churchman BypassIndianapolis, IN 46203-6109
(317) 788-9351
(PF)
CIRCLE 498
World Products Inc. Protection Products 19654 8th St. East
Sonoma, CA 95476
(707) 996-5201
(FP)
CIRCLE 499
Zenith Electronics Corp. 1000 Milwaukee Ave.
Glenview, IL 60025
(312) 391-7733
(TF) (CH)
CIRCLE 500

## (TF) (CH)



## Resistors

(AU) Audio
(CF) Carbon film
(CR) Ceramic
(CE) Cermet
(MN) Metal/non-metal film
(TF) Thick film
(TH) Thin film
(GL) Glass
(HR) High resistance
(MO) Metal oxid
(WW) Wire-wound
(CH) Chip
(CO) Conductive plastic
(ST) Single-turn pot
(MT) Multi-turn pot
Trimmers
(RN) Resistor networks

## Capacitors

(AI)
(CD)
(CD)
(CM) Ceramic/multilayer

EA) Electrolytic/aluminum
ED) Electrolytic/tantalum
dry slug
(EW) Electrolytic/
(FL) Film/polycarbonate
(FP) Film/polyester
(FY) Film/polypropylene
(FT) Film/polystyrene
(FF) Film/polysulfone
(CG) Glass
(MI) Mica
(TE) Teflon
(VA) Vacuum
$\begin{array}{ll}\text { (CP) Chip } \\ \text { (CN) } & \text { Capa }\end{array}$

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transmission and presentation into highly-integrated, tightly-linked chip sets.


## SMT TRANSFORMERS MEET TELECOM NEEDS

A series of surface-mounted, tele-phone-interconnect transformers is believed to have the lowest height available ( 0.47 in .) for audio transformers that link voice and data terminals to phone lines. The TS1000 se-

ries units are designed for dry-circuit, $600-\Omega$ lines and have a frequency response of 300 to $3500 \mathrm{~Hz} \pm 0.5$ dB over a power-level range of -45 to +7 dBm . Distortion is $0.5 \%$ maximum. Pricing in large quantities is about $\$ 3$. Delivery is from stock.

Microtran Co.
P.O. Box 236

Valley Stream, NY 11582
(516) 561-6050

## - CIRCLE 594

## POWER-LINE CHOKES FEATURE COMPACT SIZE

Two series of surface-mounted pow-er-line chokes feature a low-profile, compact design. Both series work well as a choke coil for a de-dc converter. The 10 RF series ranges in value from 10 to $220 \mu \mathrm{H}$ with a maximum de-current rating of 1.2 A . The 12RF series ranges in value from 10 to $560 \mu \mathrm{H}$ with a maximum current capacity of 2.2 A dc . Call for pricing and delivery.

## Toko America Inc.

1250 Feehanville Dr.
Mt. Prospect, IL 60056
(708) 297-0070

- CIRCLE 595


## - FILTER REMOVES EMI FROM EIGHT LINES

Designers can get more than 15 dBm of attenuation of common-mode noise in up to eight data lines using one CCDLF-8000 surface-mounted filter. The unit reduces conducted
noise by a factor of 32 from about 30 MHz to 300 MHz . Signals below 100 kHz pass without attenuation. Pricing is under $\$ 2$ in quantities of 10,000 . Delivery is from stock

## Coilcraft

1102 Silver Lake Rd.
Cary, IL 60013
(708) 639-6400
-CIRCLE 596

## SMT FILTERS PACK UP TO FOUR POLES

From two to four poles of selectivity are contained within a line of leaded and leadless SMT filter packages. The user must supply the input and output impedance-matching networks. To date, the company has manufactured up to eight poles of response at 21.4 MHz with $50-\Omega$ termi-

nations in a 1.25 -by- 0.53 -by- 0.22 -in. package. Call for pricing and delivery.

## Piezo Technology Inc.

P.O. Box 547859

Orlando, FL 32854-7859
(407) 298-2000

- CIRCLE 597


## TOROIDAL POWER CHOKES FOR SWITCHING TASKS

Already offered in vertical and horizontal configurations, a series of toroidal power chokes is now also available in cased and encapsulated versions. The options offer better environmental and mechanical protection as well as easier handling for assembly. Inductance values range from 10 to $1000 \mu \mathrm{H}$ and current ratings run from 1 to 10 A . Call for pricing and delivery.

Gowanda Electronics Corp.
P.O. Box 111

Gowanda, NY 14070
(716) 532-2234

- CIRCLE 598


Spectrol's low noise, $7 / 8^{\prime \prime}$ diameter wirewound pots are well suited for industrial panel controls or position sensing applications. The three-turn model 533, five-turn model 535 and ten-turn model 534 are available with a choice of English or metric shaft/bushing sizes and a hybrid resistor element. The model 536 is a lower cost tenturn version offering a choice of plastic or metal shaft. Other specifications include a $50 \Omega$ to $100 \mathrm{~K} \Omega$ resistance range, $0.25 \%$ linearity and $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ operating temperature range. Custom modifications are welcome when the quantity warrants.

## Spectrol ${ }^{\circ}$

Spectrol Electronics Corporation
P.O. Box 1220, La Puente, CA 91749

Phone: (818) 964-6565 Fax: (818) 810-1093
CIRCLE 119
Spectrol Dials for Precise Pot Calibration


Spectrol Electronics makes your job easier by offering a versatile line of potentiometers and dials which can be combined to fit almost any application. Make a perfect match with one of the industry's most popular turns-counting dials: either Spectrol's Model 15 digital or Model 16 concentric, and Spectrol's Model 534 or 536, 10 -turn, $7 / 8^{\prime \prime}$ wirewound potentiometers. It's a winning combination worth looking into an easy reading dial that looks good on everybody's panel, plus a versatile, 10 -turn, wirewound potentiometer available in scores of standard and special variations. Contact your nearest Spectrol Electronics Distributor today and order your winning combination!

## spectrol

[^7]
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## GRISTAIS \& OSCILIATORS

SMT QUARTZ CRYSTALS MADE FOR AUTOMATION


A series of surface-mounted quartz crystals has been engineered for use in all solder-reflow processes, including vapor phase and infrared. The SX2050P Series crystals are offered in all standard microprocessor frequencies from 3.579545 to 25 MHz and in some non-standard values. Standard frequency tolerance is $\pm 50 \mathrm{ppm}$ maximum and stability is $\pm 100 \mathrm{ppm}$ maximum from zero to $+70^{\circ} \mathrm{C}$. Call for pricing and delivery.

## M-Tron Industries Inc.

P.O. Box 630

Yankton, SD 57078-0630
(605) 665-9321

- CIRCLE 599


## CRYSTAL OSCILLATOR GIVES 100K-ECL OUTPUT

The CO-454V voltage-controlled crystal oscillator is designed specifically for phase-locking applications. It provides 100K-ECL-compatible outputs at any specified center frequency from 8 to 200 MHz . Deviation over zero to -5 V or $\pm 5 \mathrm{~V}$ control voltage is available from $\pm 30$ to $\pm 100 \mathrm{ppm}$. Call for pricing.

## Vectron Laboratories Inc.

166 Glover Ave.
Norwalk, CT 06850

## (203) 853-4433

## - CIRCLE 600

## - TINY OSCILLATOR HAS NO OVEN

Because it has no internal oven, the TF-65010-B crystal oscillator is being touted as the world's smallest device of its type at 1.46 in. ${ }^{3}$. The unit offers a temperature stability of $2 \times 10^{-7}$ and a relatively fast 2 -minute warmup time. Pricing is $\$ 65$ in lots of 10,000 . Delivery is in eight to 12 weeks.

## Raltron Electronics Corp.

2315 N. W. 107th Ave.
Miami, FL 33182
(305) 593-6033

## - CIRCLE 601

## CLOCK OSCILLATOR

 HANDLES THREE STATESThe HS-1500/1510 (TTL) series and HS-1400/1410 (CMOS) series of quartz-crystal clock oscillators provide three-state-compatible enable/ disable signals for bus-connected TTL/CMOS systems. The HS-1400 has no internal pull-up resistor. The


HS-1400/1500 has a logic-zero enable. Frequencies are available from 60 to 110 MHz . Package size is equivalent to 14-pin metal DIP. Delivery is from four to 14 weeks. Call for pricing.

## NEL Frequency Controls Inc. <br> 357 Beloit St. <br> Burlington, WI 53105 <br> (414) 763-3591 <br> - CIRCLE 602

## ACMOS OSCILLATOR NOW IN SMALLER SIZE

An ACMOS-compatible oscillator is now available in a reduced size. The A50 Series comes in frequencies from 50 to 150 MHz with accuracies to 10 ppm . Package measurements are 0.798 in . wide by 0.497 in . deep by 0.260 in. high. Operating tempera-

tures are from -40 to $+85^{\circ} \mathrm{C}$. Pricing for prototype quantities is $\$ 42.50$ for a $100-\mathrm{MHz}$ device. Delivery is in eight weeks.

[^8]
# You'll like the feeling of our new digital troubleshooting scope. 



Now there's a 100 MHz digital scope that handles just like analog.
Digital oscilloscopes have certain advantages that are hard to overlook. But for troubleshooting, many engineers still prefer analog scopes. Simply because they like the way they handle.
The HP 54600 changes that. It looks like a 100 MHz analog scope. All primary functions are controlled directly with dedicated knobs. And it feels like one.

- U.S. Prices only.
$\dagger$ In Canada, call 1-800-387-3867, Dept. 428

The display responds instantly to the slightest control change.
But when it comes to troubleshooting, the HP 54600 's digital performance leaves analog and hybrid scopes in the dust. At millisecond sweep speeds, the display doesn't even flicker. Low-rep-rate signals are easy to see without a hood. It has all the advantages that only a true digital scope can provide. Like storage, high-accuracy, pretrigger viewing, hard copy output, and programming. And since it's one of HP's basic instruments, the HP 54600 gives you
all this performance at a very affordable price. Only $\$ 2,395^{*}$ for a 2-channel scope; $\$ 2,895^{*}$ for the 4 -channel version.
So, if you need the power of a digital scope, but like the feel of analog, call 1-800-752-0900. Ask for Ext. 2282, $\dagger$ and find out how well the HP 54600 handles your troubleshooting needs.
There is a better way.

HIGH-OUTPUT LEDs SUIT AUTOMOTIVE TASKS


An excellent light source for backlighting applications, especially in automotive jobs, is found in the Su per Argus LED lamp. The unit comes in five colors, operates at 50 mA , and generates 10 times the light output of standard Argus lamps. Other uses include backlighting of panels, LCDs, and keyboards. Sample and production lots are available now. High-efficiency red, orange, yellow, and green lamps cost $\$ 0.60$ in lots of 5000 . The deep-green version costs $\$ 0.64$.

> Siemens Components Inc.
> Optoelectronics Div.
> 19000 Homestead Rd.
> Cupertino, CA 95054
> (408) 725-3545
> - CIRCLE 604

## - BLUE LEDs, ASSEMBLIES

 BOAST HIGH BRIGHTNESSTypical luminous intensities of 3.0 med and 1.3 mcd , respectively, are features of the model 4304 H 6 (T-1) and 4303F6 (T-1-3/4) blue LEDs. The silicon-carbide devices offer $470-\mathrm{nm}$ outputs with wide viewing angles. A

variety of indicator assemblies incorporating these blue LEDs are offered. Prices start at $\$ 2.78$ for lots of 5000 . Delivery is in four to six weeks.

Industrial Devices Inc.
260 Railroad Ave.
Hackensack, NJ 07601
(201) 489-8989

- CIRCLE 605


## TRICOLOR INDICATOR <br> CUT LAMP REQUIREMENTS

A tricolor, three-leaded circuit-board indicator is capable of producing red, green, and yellow light. The Series $550-3505$ indicator comes in one T-13/4 package and incorporates two GaP LED chips. Because they minimize multiple-lamp requirements, the units are suited for use as logicstatus, circuit-board, and position indicators. Pricing is $\$ 0.97$ in lots of 1000. Delivery is from stock to eight weeks.

## Dialight Corp.

1913 Atlantic Ave.
Manasquan, NJ 08736
(908) 223-9400

- CIRCLE 606


## SUBMINIATURE LAMPS NOW IN FLAT-TOP PACKAGE

A viewing angle of $125^{\circ}$ is featured in a subminiature lamp series with a flat-top package design. The devices suit backlighting of LCDs used in dashboards, telephones, typewriters, printers, and instrumentation. The LED lamps can also serve as emitters in light-pipe applications. Six colors are available with prices of $\$ 0.23$ for standard red and $\$ 0.35$ for high-efficiency and AlGaAs red, yellow, orange, and green. All prices are for lots of 1000 . Small lots are from stock.

## Hewlett-Packard Co.

19310 Pruneridge Ave.
Cupertino, CA 95014
(800) 752-0900

## - CIRCLE 607

## - HIGH-PERFORMANCE LEDs SUIT FIBER-OPTIC USES

High performance for digital fiber-optic-transmission applications is promised by the Lytel InGaAsP LEDs. The units come in $2.5-\mathrm{mm}$ bayonet, FSMA, and FDDI styles. The hermetically sealed TO-18 LEDs are packaged in standard active-device mounts. They emit in the longwave region of 1300 nm and are actively aligned for maximum coupled power. That's typically $75 \mu \mathrm{~W}$ into $62.5-$ $\mu \mathrm{m}$ fiber. Call for pricing and delivery.

## AMPInc.

P.O. Box 3608

Harrisburg, PA 17105-3608
(800) 522-6752

- CIRCLE 608


## DUAL-OUTPUT CONVERTER SUITS DISTRIBUTED POWER

A dual-output de-dc converter serves well in distributed-power applications. The AD6 Series converters come in four input-voltage ranges centering around $5,12,24$, and 48 V dc. Five output-voltage combinations of 5,12 , and 15 V are offered. The convection-cooled converters de-

liver up to 6 W of regulated power. Efficiency is up to $70 \%$, ripple is less than 120 mV pk-pk (measured over 50 MHz ), and overcurrent protection is built in. Pricing is $\$ 40$ in lots of 250 and delivery is from stock.

Lambda Electronics Inc.
515 Broad Hollow Rd.
Melville, NY 11747
(516) 694-4200

- CIRCLE 609


## SMALL 50-W SWITCHER

 BOASTS UNIVERSAL INPUT

Any input voltage from 90 to 260 V ac can be applied to the input of the RBT Series $50-\mathrm{W}$, triple-output switchers. The universal-input capability means users won't have to manually switch modes in operation. The series is available in several output configurations. Pricing is $\$ 32$ in lots of 100 and delivery is from stock.

## Astec A merica Inc.

401 Jones Rd.
Oceanside, CA 92054
(619) 757-1880

- CIRCLE 610


## 188 variable RF coils. At very affordable prices.



If you need variable inductors in the range from .05 uH to 1100 uH , no one gives you a wider selection than Coilcraft. And no one gives you lower off-the-shelf pricing!
Coilcraft tuneable RF coils are designed to meet MIL specs. They feature compact 10,7 , or 5 mm packaging, optional shielding, and one-piece construction for maximum stability.
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For all the details on Coilcraft tuneable RF coils or our other inductive devices, call 708/639-6400.

Designer's Kits. Choose kits covering the range from .0425 to $1.5 \mathrm{uH}, .70$ to 1143 uH , or 9 to 281 nH . Kits include shielded and unshielded samples along with detailed specifications. Each costs $\$ 60$. Call 708/ 639-6400 to order.


Power Inductors

See our catalog in Vol. A, Section 1800
BEII/Recactronic eninineers naster


## 

## - 96-PIN DIN CONNECTOR SWITCHES INTERNALLY

A 96 -pin female DIN connector includes internal switching that eliminates the need for bus-grant daisy jumpers or DIP switches on the backplane. The connector is available with selectively plated gold in the contact area and tin/lead on the tail. The unit press-fit-mounts to the backplane. Samples are available within four weeks. Call for pricing.

Augat Inc.
Interconnection Pdts. Div.
33 Perry Ave.
Attleboro, MA 02703
(508) 229-2202

- CIRCLE 611


## MICRO HEADERS, SOCKETS

 ON 0.050-BY-0.100 CENTERSTo expand its micro-interconnect product offering, Samtec has introduced its TMS Series headers on 0.050 by 0.100 -in centers. The series

includes straight and right-angle options on single and double rows with up to 36 positions per row. Pricing is from $\$ 0.025$ per pin. Delivery is in five days for up to 1000 pieces.

## Samtec Inc.

P.O. Box 1147

New Albany, IN 47151
(800) SAMTEC9

- CIRCLE 612


## - FLEX-CIRCUIT LAMINATE KEEPS SHIFTS TO MINIMUM

A high-stability, high-temperature flexible laminate uses a proprietary adhesive to overcome material shifts and temperature limitations of other flexible-circuit systems. The GoreClad laminate features tight control of X-Y thermal expansion coefficients, which reduces the movement of material to less than half of other laminates. This greatly reduces failures caused by misregistration. Pricing ranges from $\$ 12$ to $\$ 50$ per

square foot. Call for samples, pricing, and delivery.
W.L Gore \& Associates Inc.

555 Paper Mill Rd.
Newark, DE 19714
(302) 368-2575

- CIRCLE 613


## - PIN-GRID-ARRAY SOCKET REQUIRES LOW FORCE

A six-finger screw-machine socket offers the lowest insertion and withdrawal force available in gang-force testing. The pin-grid-array socket has an average insertion force per pin of 1.76 oz and average withdrawal force per pin of 1.29 oz . Pricing in lots of 100 is $\$ 0.06$ per pin. Delivery is from stock to four weeks.

## Robinson Nugent Inc.

800 E. 8th St.
New Albany, IN 47151-1208
(800) 338-8152

## - CIRCLE 614

## - ARC-FREE RELAY ENJOYS LONG LIFE

Switching without arc or bounce, the Arcless relay is guaranteed by its maker for over 1 million operations. When the relay's contacts are made or broken, power semiconductors switch and carry the power load until the relay contacts have transferred. The unit handles loads up to 200 A and voltages up to 300 V dc and 200 V ac. Prices start at $\$ 225$ in lots of 100 . Call for delivery.

## Electronic Specialty Corp.

14511 N.E. 13th Ave.
Vancouver, WA 98665
(206) 574-5000

- CIRCLE 615


## LIGHTED PUSHBUTTON

 IS SEALED TIGHTLYThe YB panel-seal lighted pushbuttons offer a double-seal design that protects the mechanism from dust, water, and other contaminants. The units are qualified to IP65 of IEC529 standards. Round, square, or rectangular caps are available in several colors. Switches are rated for 3 A at $125 / 250 \mathrm{~V}$ ac and 30 V dc for silver contacts. Call for pricing.

## NKK Switches

7850 E. Gelding Dr.
Scottsdale, AZ 85260
(602) 991-0942

- CIRCLE 616

SMT DIP SWITCHES
CAN BE AUTO-INSERTED


A line of surface-mounted DIP switches is designed for automaticinsertion equipment. The ESM Series switches are offered in up to 10 positions. Top tape sealing for board washing is optional. Material is UL 94 V -O-rated and contacts are gold plated. An eight-position switch costs $\$ 1.26$ in lots of 1000 . Delivery is in four to six weeks.

Kycon Cable \& Connector Inc.
1772 Little Orchard St.
San Jose, CA 95125
(408) 295-1110

- CIRCLE 617


## TRANSPARENT MEMBRANES ENHANCE VISUALS

Enhancement of the visual interface between non-technical personnel and sophisticated software is possible with a line of transparent membrane switches. The appealing interface is totally sealed for use in most clinical or hazardous environments. Flat and curved versions are available. Call for pricing and delivery.

## Memtron Technologies Inc.

P.O. Box 207

Frankenmuth, MI 48734
(517) 652-2656

- CIRCLE 618


## Announcing the New Ultimate in Driving <br>  <br> Power Convertibles ${ }^{\text {" }}$

The premiere vebicle in power conversion. These DC/DC Converters allow you to maintain a unique balance between price and performance.

The hottest economy model on the road is the HPRIXX. It is compact and affordably priced to drive your system. The Single-InLine body styling conserves board level parking, taking up less than 0.2 inch $^{2}$ board space. A low profile is achieved through Surface Mount Manufacturing.


Precision performance comes with the HPRIXX's 750 mW of output power. This Power Convertible has exceptional roadhandling with a high efficiency rating of $80 \%$. You can "rev" up your designs with our isolation voltage of 750 VDC .

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Write P.O. Box 11400 Tuscon, AZ 85734

## HEW LITERATURE

## PLANAR CONDUCTORS IN DESIGN GUIDE

The EZ-CON planar flat-conductor system is the subject of an available design guide. The custom interconnection system is especially suited for power supplies, avionics equipment, small computers, and any space-sensitive application. The planar conductors can accomodate 100 A or more and permit access to intermediate connection points along their length.

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As detailed in a 72 -page catalog, a line of multilayer ceramic leaded ca-
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# CIRCIE <br> Build Low-Cost Precision Barometer 

JIM WILLIAMS<br>Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035; (408) 954-8400.

Until recently, precision electronic pressure measurements required expensive transducers. Capacitive and bonded strain-gauge based approaches offer unmatched results, but their costs are often prohibitive. Also, if low-power operation is desired, signal conditioning for these devices can become complex.

Semiconductor-based pressure transducers now hitting the market
offer significant improvements over earlier devices. This circuit uses such a device to form a low-cost barometer (see the figure). The LT1027 reference combines with $A_{1}$ to form a current source sending precisely 1.5 mA through transducer $\mathrm{T}_{1}$, in accordance with the manufacturer's specifications. Instrumentation amp $\mathrm{A}_{3}$ takes a differential gain of 10 from $\mathrm{T}_{1}$ 's bridge output. $\mathrm{A}_{2}$ adds gain to yield a calibrated output directly in
inches of mercury.
$\mathrm{T}_{1}$ 's manufacturer specifies a nominal 115 mV at full scale, although each device is supplied with precise calibration data. This information simplifies calibration considerably. To calibrate the circuit, simply adjust the potentiometer $\left(\mathrm{R}_{\mathrm{X}}\right)$ until the output corresponds to the scale factor supplied with the unit.

This circuit, compared to a long column mercury barometer, has been used to track ambient pressure variations from 29.75 to 30.32 in . over a three-month period with only two counts of uncertainty. Also, over 50 turn on-turn off cycles had no measurable effect. Changes in pressure, particularly rapid ones, correlated quite nicely to changing weather conditions.


AN LT1027 REFERENCE COMBINES with an op amp $\left(\mathrm{A}_{1}\right)$ to send exactly 1.5 mA through transducer $\mathrm{T}_{1}$. The gains from $\mathrm{A}_{2}$ and $A_{3}$ yield an output that's calibrated directly in inches of mercury.

# 522CONTROL STEPPER'S Speed, Direction 

FAISAL FADUL, KARL WEIDENBOERNER, AND M. AHMAD Pennsylvania State University-Erie, Station Rd., Erie, PA 16563; (814) 898-6472.

When using a stepper motor, TTL pulses must be generated to control the motor's drivers. Various manufacturers have developed a wide range of controller boards for this purpose. However, it's possible
to build a simple circuit consisting of a few logic gates at a low cost. One such circuit was suggested in a previous issue (ELECTRONIC DESIGN, "Drive Stepper Motor, Cut Cost," May 10, 1990, p. 103) using three MSI and two SSI chips. This revised cir-
cuit requires just four off-the-shelf SSI chips that involve only a few logic gates (see the figure). The controller uses all of the ICs' functional capabilities, making it smaller and less expensive while using less power.

The circuit can generate the full sequence of pulses to control the speed and direction of a stepper motor. This controller can be used for applications where the motor acceleration and deceleration needn't be managed. The circuit's components include a 7406 inverter, a 7408 AND gate, a 7474 D flip-flop, and a 74157

How A Spirit Grew To Span The Globe The People Who Powered A Century Of Leadership.


Philips Components

# A Family Business Evolves Into A Global Community United By A Sense Of Teamwork And Pride. 



On front: A young Dutch worker finishes a carbon-filament lamp at the turn of the century.


There is strength in numbers, the adage goes. The first century of Philips suggests there's much to be gained from diversity as well.

Incandescent lamps were the single focus of the company Gerard Philips inspired in 1891. Today, you'll find the Philips name not only on lighting products but also television sets, electric shavers, stereo systems and thousands of other products that improve life. Supporting all these products are the people of Philips.

Tens of thousands of men and women staffing hundreds of factories, offices and laboratories in 160 countries across six continents. All reflecting vast differences...in languages, creeds, cultures and backgrounds. Performing hundreds of different jobs. Yet in spite of those differences, they're celebrating 100 years of coming together as a team.

It's Philips people behind the lab equipment at the renowned Center for Manufacturing Technology (CFT) in Eindhoven, The Netherlands, and at Philips Laboratories in Briarcliff Manor, New York - where scientists and engineers continue basic and applied research on new materials, products and technologies.

It's people who have made Philips the world's leading producer of lighting products, consumer products, professional products and components.

It's Philips people who helped fuel the continued drive toward miniaturization with advances in products and packaging. In the late 1960 s , Philips invented the SOT23 - the industry's first surface mount package for discrete semiconductors. Recent advances include the SOT223, the first discrete surface mount package capable of dissipating up to 1 watt on standard printed circuit boards at ambient temperature of $60^{\circ} \mathrm{C}$.

In recent years, Philips introduced a series of ceramic capacitors with exceptionally small dimensions, while the development of flat-profile ferrite cores helped make increasingly smaller switched mode power supplies a reality in hundreds of professional, industrial and consumer systems.

Today, the Discrete Products Division is known for the thousands of components going into a broad spectrum of products.

Behind them all are thousands of quality Philips people who through their work, dedication and contributions have kept their communities and their company moving ahead for 100 years.
Our century-long spirit of innovation continues. Use the attached reply card to learn more about our products.

2 New N-Channel JFETs In SOT23, SOT223 SMD ${ }^{\text {® }}$ Packages.


Now Philips puts industrystandard JFETs into space-saving surface mount packages.

PMBFJ108, 109 and 110 are packaged in SOT23 encapsulations.

PZFJ108, 109 and 110 are housed in the unique SOT223 package.

Both new series are silicon symmetrical n-channel junction FETs ideal for use in analog switches, choppers and commutators and audio amplifiers.

Both provide high-speed multiplex switching in data transmission systems. They feature interchangeable drain and source connections, and RDS (on) of less than 8 ohms at zero gate voltage.

Mounted on a conventional printed circuit board, the Philipsinvented SOT223 dissipates up to 1 watt (up to 2 watts on ceramic substrates). Standard T092 packaged versions of the J108, 109 and 110 are also available: they're plug-in replacements for existing industry types. Delivery for the new SMD verions is 8 weeks ARO.
New High-Efficiency 900 MHz RF Amplifier Modules.


Samples are now available for Philips new four-stage BGY110 series RF amplifier modules.

Hand-held cellular phones and specialized mobile radio systems are among applications for the 900 MHz modules with typical efficiences of $43 \%$.

Available in five versions, the amplifier modules offer 6 V and 7.2 V operation. Their high efficiency reduces power consumption, allowing the use of smaller, lighter batteries.

Models BGY110A (over U.S. frequencies from 824 to 849 MHz ) and BGY110B (UK frequencies from 872 to 905 MHz ) are 6 volt supply types providing 1.2 W output power into $50 \Omega$ loads.

Conventional 7.2 volt models BGY110D (U.S. band), BGY110E (UK band) and BGY110F (Nordic band) all produce 1.7 watt output into a $50 \Omega$ load.

The new amplifier modules, when specified at 0 dBm (equal to 1 mW drive power) eliminate the need for an amplifier between the VCO and module.

## 5 Reed Switch Series Earn UL Recognition.



Philips glass-encapsulated singlepole industrial dry reed switches are now qualified for use in UL listed products.

Series RI-23, RI-25, RI-27, RI-29 and RI-46 switches are extremely small - the largest measures just 21.5 mm long by 2.8 mm in diameter. Perfect for AC or DC use, they are designed open until activated by coil or magnet.

Maximum switched power for the new devices ranges from 10 to 40W. Maximum switched voltage is 140 , or 250 VAC/200VDC.

Switches contain a ferromagnetic contact blade hermetically sealed in a glass envelope of inert gas. They offer low resistance when contacts are closed; greater than $10^{12}$ ohms when opened.

High contact forces and special rutheniam-over-diffusedgold contact layers provide a typical low contact resistance of 60 to 100 milliohm.

Applications include reed relays, proximity switches and level detectors in instrumentation, security systems, applicances and automotive equipment.

Volume delivery is 8-12 weeks.

Ultra Precision Metal Film Resistors Available Now.


Philips is taking aim at test and instrumentation and measurement equipment with its UPR 5000 Z series of ultra precision metal film resistors.

Initially developed to replace high precision wirewounds, the series is ideal for replacing bulky metal foil designs. Use them for A to D conversions and other circuitry requiring precise, stable resistors.

Available in three body sizes ranging from $1 / 20 \mathrm{~W}$ to $1 / 3 \mathrm{~W}$, the resistors feature tolerances as low as $\pm .01 \%$ and temperature coefficients starting as low as $\pm 2 \mathrm{ppm} / \mathrm{c}$. Other series characteristics: excellent temperature and time stability, low voltage, low noise, and high initial accuracy and tracking.

Ask for UPR 5000 Z resistors in bulk or on tape and reel. Delivery from stock or within 8 weeks ARO.

Thin Film Technology, SMD ${ }^{\circledR}$ Combined in MELF Resistor.


Philips 9B1406 MELF precision resistor benefits from technology used in manufacturing leaded metal film resistors-even though it comes in a surface mount package.

This thin film SMD ${ }^{\circledR}$ resistor is formed by depositing metal film on a high alumina core which is then capped and spiralled to value. The 9B1406's end caps are coated with nickel-copper-nickel and pure tin. The result: excellent soldering characteristics are maintained after long storage.

The MELF resistor offers TCs down to $\pm 15 \mathrm{PPM} /{ }^{\circ} \mathrm{C}$ and tolerances to $.1 \%$. Availability is .22 ohm to 10 megohm in the $5 \% 50$ PPM version. In bulk or tape and reel.

## 1, 2 and 3W Power Metal Film Resistors.



Now replace expensive wirewound resistors with Philips commercial 1,2 and 3-watt metal film resistors. The series of miniature resistors feature $5 \%$ tolerances and temperature coefficients of 250 ppm .

Small size is a major benefit: advanced metal film technology produces 1 W resistors measuring just 295 inches CL-CL. The result is a high wattage resistor with low hot spot parameters and metal film stability. The PR series is available on RN296D Class 1 , tape and reel for automatic insertion, 5000 piece reels.

## Coated Ceramic Capacitors <br> In Radial Or Axial Designs.



Between Philips MonoKap ${ }^{\circledR}$ radial and MonoAxial ${ }^{\circledR}$ axial product lines, there's a conformally coated ceramic multilayer capacitor to fit every circuit need. Capacitance values start at 10 pF with voltage ratings of 50 , 100 and 200 VDC. Z5U, X7R and COG (NPO) dielectrics are available.

MonoKap lead styles range from .100 inches ( 2.5 mm ) to .400 inches $(10 \mathrm{~mm})$ depending on component size and configuration. Packaging: bulk or EIA tape and reel and ammo pack for automatic insertion.

## First 0-Ring Sealed Surface Mount 3mm Single-Turn Trimmer.



Saving space is the key phrase in describing Mepcopal's new 3mm single-turn trimmer.

With their O-ring seals, ST-3 series surface mount trimmers can withstand vapor phase reflow cycles of up to $215^{\circ} \mathrm{C}$ for three minutes; dip and reflow temperatures to $260^{\circ} \mathrm{C}$ for 10 seconds.

The trimmers are sealed against immersion - passing the flourinert ${ }^{\text {TM }}$ leak test @ $85^{\circ} \mathrm{C}$ and other boardwashing processes. Precious metal alloy contacts assure exceptional resistance stability in low current applications.

Operation temperature range is $-55^{\circ}$ to $+125^{\circ} \mathrm{C}$.

Among other features, the trimmers offer a resistance range of 100 ohms to 1 megohm; power rating is 0.1 W @ $70^{\circ} \mathrm{C}$. Rotational life is 100 cycles with a maximum shaft torque of 50 gcm .

And they're designed to resist shock: thermal shock from $-65^{\circ}$ to $+125^{\circ}$; shock of 100G and vibration of 20G @ 10 to $2,000 \mathrm{~Hz}$. The trimmers tolerate high temperature exposure up to $+125^{\circ} \mathrm{C}$ for 250 hours. Available on tape and reel.

Mepcopal is a joint venture of Philips Components and Copal Electronics USA.

Smaller Photomultipliers Allow More Compact, Lighter Camera Heads.


Philips brings new technology to photomultiplier tubes (PMTs) for medical imaging, scientific and industrial applications.

New foil structure dynodes developed by Philips allow PMTs to be shorter, so gamma camera heads incorporating the tubes can be lighter and more compact.

Philips PMTs feature fast response times and high resolution. They're available in a variety of shapes and sizes, including $3 / 4$-inch to 10 -inch diameters and hexagonal, round and square configurations.

Covering the spectral range of 200 nm to 1000 nm , these PMTs are available with up to twelve multiplier stages.

## Sales Offices and Manufacturer Representatives

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PHILIPS


THIS CIRCUIT IS A REVISION of a previously published bidirectional stepper-motor sequencer. The new circuit uses four chips,
with an option of using just three (the flip-flops and AND gates can be combined). The rate of clock pulses determines the motor's rpm.
Switching transistors can replace the relays to increase the circuit's efficiency.
multiplexer. The 7474 and 7408 ICs can be integrated into one chip using a Johnson counter IC.
The stepper motor's rpm is determined by the clock pulse. This signal can be connected to a counter to tally the number of pulses needed to stop the motor after it has spun its required revolutions. The pulses (or counter outputs), controlling the output to the driver, are organized to spin the motor either clockwise or

## IFD Winner

## IFD Winner for January 10, 1991

Noor Singh Khalsa, EG\&G Inc., P.O. Box 809, MS E-1, Los Alamos, NM 87544; (505) 667-0200. His idea:"Capture Data Before, After Event."

## TOTE

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $\$ 150$ Best-of-Issue award and becomes eligible for a $\$ 1,500$ Idea-of-the-Year award.
counterclockwise. The multiplexer's outputs remain low so inverters aren't needed.

The four motor coils are powered through four solid-state relays and protective resistors. The motor speed is determined by the number of pulses/s. The number of steps moved by the motor is determined by the number of pulses sent. Its sequence is established by the flipflops and the adjoining AND gates,
or if the Johnson-counter approach is taken. The pulses are then sent through a quad two-by-one multiplexer that determines the direction of the motor.

The relays can be replaced with switching transistors. This increases the controller's efficiency by letting higher pulse rates drive the motor. Consequently, the power consumption is reduced and coil heating is eliminated.

# CIRCIF 523 VC0S DIRECTLY 

MICHAEL WYATT

SSO Honeywell Inc., 13550 Highway 19 S., MS 931-4, Clearwater, FL 34624; (813) 539-5653.

Microwave and rf voltagecontrolled oscillators (VCOs) often require control voltages that are incompatible with standard $\pm 15-\mathrm{V}$ supplies used by op amps and other analog circuits. This circuit lets $\mathrm{U}_{1}$ operate from standard $\pm 15-\mathrm{V} \mathrm{V}_{\mathrm{CC}}$ and $\mathrm{V}_{\mathrm{EE}}$ supplies while scaling $\mathrm{U}_{1}$ 's output to a unipolar level of 5 to 25 V (Fig. 1).

Transistors $Q_{1-3}$ form a low outputimpedance inverting amp with a volt-
age gain of two. Negative feedback supplied by $R_{2}$ closes the loop formed by $\mathrm{U}_{1}$ and the inverting amp, causing $\mathrm{U}_{1}$ 's non-inverting input to act like a virtual ground. Frequency compensation for the composite amplifier is supplied by $R_{7}$ and $C_{1} . R_{3}$ and $V_{E E}$ produce an offset current in the amplifier which sets the " $0-\mathrm{V}$ input" output level.

With the values selected, the " $0-\mathrm{V}$ input" output is 15 V , and the " $\pm 10-$ V input" output is 5 to 25 V . The

# RFTRANS 

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Choose impedance ratios from $1: 1$ to $36: 1$, connector or pin versions (plastic or metal case built to meet MIL-T-21038 and MIL-T-55831 requirements ${ }^{\star}$ ). Ultra-wideband response achieves low droop and fast risetime for pulse applications. Ratings up to 1000 M ohms insulation resistance and up to 1000 V dielectric voltage. For wide dynamic range applications involving up to 100 mA DC primary current, use the T-H series. Coaxial connector models are offered with 50 and 75 ohm impedance; BNC standard; request other types.
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NSN GUIDE

## MCL NO. NSN

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## $3 \mathrm{KHz}-800 \mathrm{MHz}$ from $\mathbf{\$ 3 2 5}$

| case style numbersee opposite page |  | Model |  | RATIO | Freouency | insertion loss |  |  | PRICE \$ <br> (1-9) |
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## IDEAS FOR DESIGN



THE OP AMP $\left(\mathrm{U}_{1}\right)$ IN THIS CIRCUIT operates from a standard $\pm 15 \mathrm{~V}$ supply and its output is scaled from 5 to 25 V (a). With a slight modification, the circuit becomes an active lead-lag filter that can drive an rf or microwave voltage-controlled oscillator directly (b).
closed-loop voltage gain is $-R_{2} / R_{1}$. Dynamic performance for the composite amp features a closed-loop bandwidth greater than 2.5 MHz and
a slew rate greater than $4 \mathrm{~V} / \mu \mathrm{s}$. Modifications make the circuit an active lead-lag filter capable of directly driving an rf or microwave

VCO (Fig. 2). $\mathrm{C}_{2}, \mathrm{C}_{3}, \mathrm{R}_{1}$, and $\mathrm{R}_{2}$ determine the active filter's time constants, while $Q_{1-3}$ supply the voltage scaling and buffering.

## MINIATURE PHOTODETECTOR POWER SUPPLIES

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Coto Wabash's 5500 Series high voltage reed relays provide designers up to 7,500 volts switching , a dielectric strength of 10,000 volts, and a contact power rating of 200 watts. You get 100 ppm quality in a reed relay delivering $>10^{8}$ operations under signal level conditions. Features include low contact resistance ( $0.025 \Omega$ typical). Rugged, environmentally sealed package is available in custom mounting options. Our 5500 Series is ideally suited for applications such as high voltage testing, power supplies, remote monitoring equipment, and cable testing equipment. Call or write to us today for a free full line "Partners in Design" catalog.


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## QUICKL00K

## MARKET FACTS

Bngineers need to store more and more large structured data types, such as three-dimensional designs. As a result, the need is growing for object-oriented databases.

Because engineering users have so far gotten little support from database vendors, they have come up with customized file systems. These systems, however, can result in isolated groups of data that are difficult to manage.

The market for object-oriented databases that combine data-management facilities with support for an object-oriented language like $\mathrm{C}++$, will grow from a small base this year to $\$ 560$ million in 1995. These extended relational DBMS are expected to account for $52 \%$ of a total DBMS market worth about $\$ 4.2$ billion in 1995 in the U. S. and Europe, according to London market researcher Ovum Ltd.

Demand for object-oriented databases also is coming from the multimedia sector. These systems need storage for large unstructured data types, image and voice, as large binary objects.


WHO'S BUYING OBJECT-ORIENTED DBMS?

an Intel PC-on-a-chip ASIC, surface mounting, and a static microprocessor go to work in a Hewlett-Packard Co. palmtop PC. The checkbook-size HP 95LX has Lotus 1-2-3 built-in-HP is taking aim at 14 million 1-2-3 users. Lotus developed a ROMbased version of 1-2-3 Release 2.2 for the unit, which lists for $\$ 699$.

Another twist is that Motorola will ship by year end a one-way wireless rf receiver for the PC that can receive 56 messages (up to 32 k ) 24 hours a day. The 95 LX comes with 512 k of RAM, 1 Mbyte of ROM, a serial interface, a 16 -row by 40 column supertwist LCD screen, a Qwerty keyboard, and a numeric keypad. Also built into ROM are an HP financial calculator, phone book, appointment book, and memo editor.

Files can be up- and downloaded to PCs with HP's connectivity pack. Intel Corp. trimmed the number of motherboard chips to an ASIC that contains PC logic, memory-management unit, power management, an ADC for measuring battery voltage, and display and keyboard controllers. To that, HP adds an NEC V20 microprocessor and zero-wait-state memory. The 95LX runs for up to two months on two AA batteries, backed up by a lithium battery. The HP 95LX also works with an ac adapter. A 128 -kbyte RAM card goes for 199.95 . The rf device is expected to sell for less than $\$ 400$; monthly service costs will vary.


## Motorola's In Real


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Ademonstration package is free for Data Translation's Global Lab Data Acquisition software. The program offers simultaneous acquisition and display. The software can display data in up to 100 windows.

For more information, contact the company at 100 Locke Dr., Marlboro, MA 01752-1192; (508) 481-3700; fax (508) 481-8620.

SUSIE-Concurrent Designer 6.0 from Aldec enables designers to simulate and verify breadboard designs. As a result, they can skip the prototyping stage.

A free evaluation kit demonstrates the simulation software. To obtain a kit, contact the company at 3525 Old Conejo Rd., Suite 111, Newbury Park, CA 91326; (800) 48-SUSIE or (805) 499-6867; fax (805) 498-7945.

afree disk demonstrates Snap-Series Software from HEM Data Corp. that integrates data acquisition, analysis, and display. The software works with analog I/O hardware from 12 manufacturers and samples at the hardware's maximum rate, up to 1 MHz . It acquires up to 80 channels and 500 million data points.

Contact the company at 1733612 Mile Rd., Southfield, MI 48076; (313) 559-5607; fax (313) 559-8008.

0ndustrial control systems are getting graphical user interfaces. Gespac's G-Windows, a windowsbased software environment and development tool, eases creating GUIs for industrial control systems.

A free technical videotape demonstrates G-Windows, including the G-View application editor, in which a screen can be drawn and integrated into a C application program. For a copy of the tape, contact the company at 50 W . Hoover Ave., Mesa, AZ 85210; (800) 4-Gespac or (602) 962-5559; fax (602) 962-5750.

IIore than 3000 products-test and measurement instruments, professional broadcast equipment, and computer peripher-als-are listed in Tektronix's 1991 catalog. What's more, over 70 new hardware and software products are included in this year's edition.

The free catalog can be ordered by calling the Beaverton, Ore., company's national marketing center at (800) 426-2200.

## OUIGK NEWS: EDUGATION

as part of their jobs, engineers must keep abreast of changing technology. Short courses offer a way to stay current without being away from the job for too long. Learning Tree International offers various intensive four-day courses. Among them are workshops on advanced project management and expert systems design. Also offered are courses on object-oriented analysis and design, Unix programming in C, X Window system programming, hands-on Unix networking, and digital signal-processing techniques. Course hours are 9 am to $4: 30 \mathrm{pm}$, with an informal disccusion about applications or areas of special interest from $4: 30$ to $5: 30 \mathrm{pm}$.

For additional information, contact the company at Education Center, 8000 Towers Crescent Dr., Third Floor, Vienna, VA 22182; (800) 421-8166; (703) 893-3555; fax (703) 847-0075.

## K M E T S K O R N E R ...Perspectives on Time-to-Market

## BY RON KMETOVICZ

President, Time to Market Associates Inc.
Cupertino, Calif;; (408) 446-4458, fax (408) 253-6085

Iet's talk more about the Kmet chart in the May 9 issue. Ex-
 amining the slope of the curve highlights three regions that should be analyzed further. Note the steep rise in slope just preceding the design review, the flat slope preceding the E-pilot milestone, and the lack of detail from E-pilot to E-prod. Any ideas about the causes of the major changes in slope?

In these abnormal zones, it is possible to return to the network to gain a better understanding of the exact cause. However, a little speculative thinking will probably produce the same results. As might be expected, the slope rise preceding the design review milestone is produced by having work elements come together for the milestone. Note that following the milestone, output goes to zero for two weeks. This plan has the crash into the milestone built in! We have a work group that is planning to work long and hard to produce for the milestone and then kick back a bit after it's over.

In the vicinity of week 34, output again goes to zero. In this case, future work is waiting on the arrival of output from another individual before work begins. The lacking detail from E-pilot to E-production exists because visibility, of work needing to be performed this far into the future, is "fuzzy."

Now that problems with the plan are identified, it becomes relatively easy to focus on these regions to make the needed improvements. The Kmet chart analysis suggests the initial plan is lacking in detail for an 11-person team; contains an improperly structured network around the design review milestone; wastes precious project time preceding the E-pilot milestone; and lacks sufficient detail from the E-pilot milestone to completion.

With knowledge of where to focus, the team produced a revised plan. Historical network and task data was used from previous projects completed by this organization. In this effort detail increased to 162 tasks. With 11 people on the project, this translates to tracking about one task per person per month on the average. Besides increased task detail, the chart became linear. The revised plan now has the appearance of being right and is ready for use as the baseline plan when entering the execution phase.

In summary, the Kmet chart is used during the planning phase to get a rough idea (within a factor of two) of how many people will be working on the project. Second, slope changes can be used to point out possible areas of concern within the network that drives the chart. A steep slope shows that the running rate of task completion is about to increase. This is a tolerable situation if it is accompanied by a corresponding increase in resources. Otherwise, it shows that problems are likely to occur with completing tasks. It is especially dangerous to see a slope rise prior to a major milestone. Often, this signals wishful thinking. A reduction in slope from the normal running rate signals that forward progress has slowed down. At a slope of zero, the project is at a standstill as time to market extends.

## TIPS ON INVESTING

1hese days engineers are rate-conscious, as well as aware of how inflation can erode assets. Take the case of an engineer with assets invested in an $8 \% \mathrm{CD}$. When he read about a mutual fund up $25 \%$ during the previous quarter, he decided he was losing money.
"The CD seemed like a safe investment, until I stopped to think that it wasn't keeping enough ahead of inflation. So I jumped into the fund," he recalled, without realizing that performance over a complete market cycle-rather than one quarter-would be a stronger indication of its potential. Subsequently, his portfolio lost $30 \%$ of its value. He invested without regard to risk, his own investment philosophy, or long-term strategy. Greed overtook reason.

Unfortunately, this engineer is not alone. Many investors misunderstand the investment process, especially in regard to risk. They also fail to understand the role a professional consultant and money manager can play in creating a portfolio that fits parameters of personal goals and risk tolerance. Professional assistance also helps the individual investor avoid the herd instincts that overtake Wall Street and individual investors.

Before Oct. 19, 1987, many investors got caught up in stock market euphoria. Not being in the market was seen as a risk. Rather than making informed decisions, investors jumped into what they perceived as a no-lose performance game.

Even professionals and institutions raced to see who could accumulate the most the fastest in a seemingly unending bull market. Many investors lost sight of the fact that a market could actually declinethat is, until Black Monday.

October 19 ended euphoria. Panic prevailed. Investors in droves redeemed their shares in equity mutual funds. Two years later, Friday the 13 th 1989 , just when many retail investors were regaining confidence in the market, the Dow Jones Industrial Average plunged 190 points. This time, investors-guided by their experience and by professional advisors-controlled their panic and the market rebounded. In retrospect, Oct. 20,1987 was the time to buy, rather than sell. These downturns show investors that risk is intrinsic to reward. Investors who wish to make money in the stock market must be aware of the potential to lose assets and to set their investment goals accordingly. An investment counselor can help an investor understand how much risk he can live with-financially and emotionally-by asking himself questions like these:
-What type of investments am I comfortable with?
-What are my expectations in terms of performance?
$\bullet$ How does that fit into different market scenarios?
$\bullet$ How much am I willing to risk?
-What type of manager am I working with and what types of investments does he work with?

- What are my time horizons and how much time am I willing to commit to an investment?
- Are his style and philosophy compatible with my risk tolerance and goals?

Investment for engineers need not resemble a roller coaster ride. Intelligent investment protects against loss. Call or write to me for a free copy of Professional Portfolio Management-Making the Right Choice.
Henry Wiesel is a financial consultant with Shearson Lehman Brothers, 1040 Broad St., Shrewsbury, NJ 07702; (800) 6312221 or (800) 221-0073 in N. J. Wiesel invites readers'questions and comments.

## MIGROPROGESOR SURVEY

HOW MANY 32-, 16-, 8-, AND 4-BIT MICROPROCESSORS WILL YOU PURCHASE IN THE NEXT 12 MONTHS ?


Here's a list of organizations and newsletters for engineers, which address such professional concerns as layoffs, age discrimination, and portable pensions. Readers are encouraged to submit letters, columns, and articles. Write for a sample newsletter.

- American Association of Concerned Engineers (AACE), Dick Lowrie, editor, P. O. Box 667, Trilby, FL 33593. Dues are $\$ 10$ a year. - American Engineering Association (AEA), Billy Read, editor, P. O. Box 820473 , Ft. Worth, TX $76180-0473$. Dues are $\$ 20 /$ year.
-AIE, M. Gottlieb, editor, 4666 San Pablo Dam Rd., El Sobrante, CA 94803. Dues are $\$ 55 /$ year.
-Provisional EE News, John Gilmer, P. 0. Box 7211, Fredricksburg, VA 22404; donations are requested.

0SP applications and technology are attracting more and more attention. Along these lines, the first international conference-trade show on DSP applications will be held in Berlin, Germany Oct. 28-31, 1991. Conference sessions will feature papers on DSP in telecommunications, speech processing, image processing, control systems, consumer electronics, and other applications.

About 100 companies are expected to display their products at the trade show. Engineers who would like to deliver a paper should send or fax a 100 -word abstract for review by June 30 . For information, contact DSP Associates, 18 Peregrine Rd., Newton Centre, MA 02159; phone (617) 964-3817; fax (617) 969-6689; in Europe DSP Associates, 25 Justitiestraat, B-2018 Antwerpen, Belgium; attention Lina Van Meerbeeck; phone +32 (3) 237-1677; fax +32 (3) 248-1694.

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# PEASE <br> PORRIDGE 

## What's Aul This Brick STuFf, Anvhow?

This is an esaeP's fable. Once upon a time, a very proper Bostonian lady decided to build a new home, so she hired an architect to design a new brick house. When he finished the design and showed it to her, she said, "That's very nice. Now, how many bricks willit take?" The architect replied, "About 76,000 bricks, ma'am." She said, "How many bricks, exactly?" He asked, "You really want toknow exactlyhowmany bricks?" She said, "That's right. I want to buy exactly the right number of bricks."

The architect realized that this was a reasonable request, so the next day he told the lady. "Exactly 75,885 bricks." So she had that exact number of bricks delivered, and the masons and bricklayers worked for many days. Finally the last bricklayer set the last


BOB PEASE
OBTAINED A
BSEE FROM MIT IN 1961 AND IS STAFF
SCIENTIST AT NATIONAL SEMICONDUCTOR CORP.,
SANTA CLARA, CALIF. brick into place at the peak of the last part of the house. The bricklayer turned around and saw that one brick was left. So, he picked it up and threw it over his shoulder. Now if you were planning a project, you might want to plan carefully so that you had the right resources to finish the job. You might even plan to have some safety factor or margin, so that if some un- foreseen problem caused delays or trouble, you would still be able to fulfill your obligations. For example, if a few bricks were broken, you wouldn't want to have to go back to the brickyard and ask them to build some more bricks with the identical pattern, would you?

Some managers, though, write a schedule and if there are any unforeseen problems, they want the workers to invent bricks out of thin air, just to get the project back on schedule and back on budget. They claim they should not have to allow extra resources that might just be wasted. I mean, if they bought 75,886 bricks, the workers would just waste one or two, wouldn't they? They might just take a brick and throw it over their shoulder.

By the way, have you ever tried laying bricks? I've done a little bricklaying, and while it looks like a simple "digital" procedure, it is not. It requires analog precision and judgment to get the bricks level and each course flat. Also, when you're trying to fit an irregular space, you find that the broken pieces are pretty useful, as often you can find just the right length to fit in. If not, you have to break a brick intopiecesuntilyou get lucky and get the right size piece of brick. It's an analog business.

Now here's another esaeP's fable. Sometime later, that same proper little old Bostonian lady decided to travel on the MTA to visit a friend. She started out on the subway with her little poodlesitting onherlap. At thenext stop, a large churlish man got on and sat down beside her. He took out his Record-American and spread it out at full width. Naturally, the newspaper flopped around in front of the little old lady's face, and right across the ears of her poodle. Not very polite. After a short time, she nudged the newspaper. The man retaliated by nudging her poodle. He put out the newspaper again, encroaching on her space. She gave a flounce to the newspaper. He gave a shake to her poodle. She could not abide this, throwing the newspaper on the floor. He threw the poodle on the floor. She then took the newspaper and threw it out the window! He took the poodle and threw it out the window!!

Of course, at this point, pandemoniumensued. Shescreamed, and somebody pulled the emergency cord, and the conductor came running up as the trolleyscreeched toastop, and thelady tried to explain, "This terrible man, he threw my little dog right out this window." And as the conductor and the lady and the terrible man all looked out the window, the little dog came trotting up the tracks. And what did he have in his mouth? The newspaper? No, the brick.

Now, this starts out with one absurd story, and it rzambles along and crashes into a fragment of the first fable. What's the moral of this story? I'm not sure. Maybe it's that you can't count on logical things happening all of the time. If your train of thought derails, what can get it back on the tracks? There are no easy answers to that one. But in thereal world, you may find things happening that are worse than you expect. You may also find things working better than theory predicts, and you should be prepared to take advantage of them.

Remember, it was Branch Rickey who said, "Good luck is the residue of design." Good luck doesn’t just happen to the lucky; it sometimes "happens" to those who are prepared to grasp it. Another aspect: Only a few years ago, we were reading about "The office of the future:The paperless office"-what a joke! Our offices generate more paper than ever (most of the computerized reports are neverread).Wenow have a quasi-infinite thicket of computer files, floppy disks, floppy directories, and only the vaguest idea where to find that memo you sent out to an important client just a couple years ago. Are there new "file manager" programs that claim they can find anything in all of your files? Sure, and can I sell you a bridge? If you ask one of these file managers for a newspaper, will it give you a brick?

All for now. / Comments invited! / RAP / Robert A. Pease / Engineer

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## Two VME Boards Implement A Software Algorithm In Hardware To Accelerate Gate-Level Simulation.

## HaRDWARE, SOFTWARE Simulators Blend SEAMLESSLY

Standard hardware platforms can shackle the speed of gate-level simulation as gate counts rise. This is because even though MIPS ratings go up, simulations don't get faster due to the limitations of the workstations' cache architectures. For instance, a gate-level simulation on an event-based simulator could easily have 100 Mbytes of data structure, yet the cache probably holds only 100 kbytes of data. Even worse, gate-level simulations incur many cache misses. The problem is most severe in multi-ASIC systems.

A hardware accelerator from Cadence Design Systems Inc. will help alleviate this simulation bottleneck. The XLProcessor (XLP) is a gate-level accelerator that implements the company's XL simulation algorithm in hardware. The XL algorithm powers gate-level simulation in Cadence's Verilog-XL and VHDL-XL software simulators.

Cadence overcame two major stumbling blocks to build the accelerator: creating a seamless joint between the software and hardware environments, and having an appropriate cache size that wouldn't handcuff performance. When there are seams, the move from the software- to the hardware-simulation environment creates a large overhead. Moreover, time is wasted on correlating the simulation results.
The resulting XLP product can be viewed as a simulation coprocessor that works much like a graphics or math coprocessor. This is a good approach to simulation acceleration because it doesn't detract from any of the users' resources. XLP is integrated seamlessly with the existing software simulators. Both simulation environments share the same user interface, models, simulation algorithm, and delay calculators. Therefore, translation isn't required when going from one environment to the other. In addition, there's no need to correlate results between the two simulation technologies because the two obtain consistent results (see the figure).

The accelerator can be used early in the design cycle when simulation is performed at both the behavioral and structural levels. Because it works seamlessly with the software simulator, XLP brings higher speed and capacity to mixed-level simulations: The software simulator manages the behavioral-level portion while XLP works on the gate-level sections. XLP can handle designs with up to 1 million gates. It operates at up to 2 million events/s, and offers


THE SEAM BETWEEN hardware- and software-simulation environments caused by different user interfaces, simulation algorithms, primitives, and delay calculators can produce different results and incur a large amount of overhead (a). The Verilog environment has no seam because the hardware and software simulators use the same primitives, delay calculator, net list, stimulus, and user interface. A software
switch determines if the simulation is sent to the hardware accelerator (b).
timing accuracy that includes pin-topin delays, timing checks, pulse control, and state-dependent delays. However, XLProcessor doesn't perform dynamic timing analysis. In addition, XLP doesn't accelerate fault simulations.

XLProcessor is made up of a twoboard set that uses two triple-height VME slots. It increases the speed of gate-level simulations by as much as a factor of 15 . The XL software algorithm was well-suited for hardware implementation because it performed the specific task of gate-level simulation.

Most of the XL algorithm is implemented in programmable logic. Pro-grammable-logic devices were chosen for cost and time-to-market reasons. The cache problem encountered in most standard workstations is solved by providing 11 Mbytes of fast memory. The memory and the PLDs are tightly coupled to minimize delays. Cadence expects that the XLProcessor can step up a level in performance by migrating from PLDs to ASICs, and by going to faster memory. Host-interface logic is also included in the two-board set.
Users invoke the hardware accelerator with a software switch. The
hardware simulator has the same interface as the software simulator, and uses the same input. The primitives, net list, delay calculator, and stimulus are all the same-it's one big Verilog environment. The software switch is what determines the simulation's course.

A software algorithm compresses data types when they're sent to the accelerator. The transfer time from the host to the server holding the accelerator is identical to any standard VME transfer. For instance, it takes about one minute for a 1-million-gate design to be downloaded to or uploaded from the XLProcessor. The workstation and the server communicate through the VMEbus.

XLProcessor works with both the Verilog-XL and VHDL-XL software simulators, and with the existing model library written in the Verilog hardware-description language. In addition, users can choose software models from Logic Automation Inc. and hardware models from Logic Modeling Systems Inc.

Although it's best utilized with the Cadence simulators, XLP can be used with any simulator. Users can employ net listers to translate from other EDA environments into the

Verilog HDL, and then simulate with the XLP. In this setup, however, users won't benefit from having the algorithm, models, and the user interface common to both the hardware and software simulation environments.
XLP offers productivity gains for multiple users because jobs can be quickly swapped in and out of the accelerator. For instance, while one job uses the XLP to accelerate a design, a second job can start in the software acceleration mode and switch to the XLP mode, without restarting the simulation. $\square$

## Price And Avallabilty

XLProcessor resides in a server as a pair of triple-height VME boards. The initial release will be compatible with Sun Microsystems servers. Future releases will be supported on other platforms. The XLProcessor board set costs $\$ 85,000$. Production shipments will begin in the third quarter of this year.

Cadence Design Systems Inc., 555 River Oaks Pkwy., San Jose, CA 95134; (408) 943 1234. CIRCLE 514

How Valuable?
Circle
Highly 560
Moderately
561
Slightly
562

# OPTIIIZE AND Retarget 

 Existing LoGic DESGISA Tool Merges Multiple Programmable-Logic Devices Into One Design, Then Optimizes And Retargets It Into An ASIC Technology.

TLisa Maliniak ime-to-market pressures force engineers to use programmable-logic devices (PLDs) for quick production. It's not uncommon for boards to be populated with hundreds of PLDs. PLDs have low nonrecurring engineering costs and don't require much up-front work. Unfortunately, they can become quite expensive once a product goes into volume production. In fact, in large quantities, they cost more per package than ASICs. Consequently, engineers often need to merge those PLDs and possibly some standard logic and retarget it all into an ASIC, a task that can be as time-consuming as the original design.

That retargeting process is now made easier, thanks to a new optimization and remapping tool from Viewlogic Systems. Called the Retargeter, its objective isn't to create designs or change the functionality of an existing design, but to increase a design's performance and/or reimplement it in another technology. For instance, Retargeter can merge together several existing PLD designs and standard logic, determine the function the group was performing, optimize the design, and retarget that same logic into a field-programmable gate array (FPGA) or an ASIC (see the figure). The tool will also retarget FPGAs into ASICs.

Retargeter accepts designs as existing net lists, which are files that describe components and the interconnects


IN THIS EXAMPLE, the Retargeter software optimizes the Actel FPGA design located in the upper-left window, and maps it into an LSI Logic 10 k gate array. The retargeted design is in the lowerright window. Viewlogic's Viewsim tool simulates both designs and compares the results in a single window in the lower left.


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## LOGIC RETARGETER

between them. Viewlogic's net lists are called wire files. Retargeter accepts standard EDIF net lists, and several Viewlogic EDIF translators import net lists created with nonViewlogic tools. The tool also accepts PLD JEDEC files. JEDEC files basically describe what function the PLD is performing.
Although the Retargeter doesn't work off hardware-description-language (HDL) inputs, the company's VHDL Designer product does. Therefore, if users need to retarget a design described partly in an HDL, they can use VHDL Designer to synthesize net lists from the HDL input. Then, they can feed those net lists into the Retargeter with the other net lists and retarget everything.
The Retargeter reads an existing wire file and produces a new wire file containing optimized logic. It optimizes the design in both the original and the target technology. This retargeting doesn't necessarily involve a direct one-to-one exchange of cells from one technology to another. Optimization may add or delete cells from the original design to optimize its performance.
The tool's optimization algorithms break a large design into small groups and synthesize each small portion individually. However, there's a size limitation to the Retargeter. For instance, users couldn't retarget something as large as a microprocessor. The tool wasn't designed for that. The real key to the product is merging standard parts into an ASIC. It could even turn a whole board into one component, which impacts reliability, testability, manufacturability, and cost.
Retargeter is easy to use. Users specify the input and output libraries and the input net list. Then, if all of the constraints are set at default values, the program is ready to run. Users, however, can set size and speed constraints. It's possible to specify timing requirements with Retargeter. Consequently, users can start with a slow design (worst-case timing of 100 ns ) and use Retargeter to make it much faster (worst-case timing of 10 ns$)$. In addition, as users specify their preferred timing, they
also can request that the design be as small as possible.

Once the system has a net list, it prompts users for their requirements. Users then enter the design requirements that must be met, specifying area, timing, and the target technology. Viewlogic supports a number of ASIC families (call the company for a complete list).

Retargeter runs in a fast iterative loop. For example, depending on the constraints, a design targeted for an FPGA may finish in 15 min . If there are many constraints, it may take several hours. Other variables, such as the workstation being used and the available memory, also factor in.

Library generation is built into Retargeter, a feature that's generally purchased in other design systems. Called Library Builder, it lets engineers describe the component library for a specific technology. Each manufacturer has their own set of components, and every one is a little bit different.
Viewlogic offers canned libraries, but it also offers this tool to let engineers add to, modify, or create new libraries. For example, Library Builder comes in handy when an engineer has a good canned description, but has worked with a part extensively and knows that there are certain characteristics to include in the model for test reasons. Basically, the tool is for users who want to specialize components for better simulation or a better working product. They may have created their own parts that they need to have models for. Users build models specifying such features as functionality, size, and speed.

## Price And Availabilty

The Retargeter, which will ship by the end of the second quarter, runs on DEC, IBM, and Sun workstations. Pricing starts at \$30,000.

Viewlogic Systems Inc., 293 Boston Post Rd. West, Marlboro, MA 01752; (508) 4800881.

CIRCLE 513

| How Valuable? | Circle |
| :--- | ---: |
| HIGHLY | 568 |
| MODERATELY | 569 |
| SLIGHTLY | 570 |

# SMALLEST, COMPLETE 1553/1760A RT 

The BUS-65153 Small Terminal Interface Circuit (STIC), is the smallest complete, dual redundant MIL-STD-1553B Remote Terminal. Packaged in a 70 pin plug-in, ceramic package that is less than 2 square inches, the STIC also provides the output level required for MIL-STD-1553B \& 1760A Stores Management applications.

The BUS-65153 contains two (2) low-power bipolar monolithic voltage driver type transceivers, and a DDC custom HCMOS protocol chip. The DDC protocol chip contains dual redundant encoder/decoders, RT protocol logic, 3 -state buffers, and DMA transfer control logic. The STIC supports all 13 dual redundant Mode Codes, and any combination of which may be illegalized by an external PROM, PLD, or RAM device.

The STIC can be easily interfaced to most CPU or simple subsystems with minimal complexity. Parallel data transfers are performed via a DMA type handshake. Selectable 8bit or 16-bit transfers are supported. Simple subsystems can be interfaced directly through switches, D/A converters, or latches in place of a microprocessor. Advanced memory management controllers such as the DDCBUS-66312 ornew BUS-66315 can be used with minimum glue logic for a shared RAM interface of up to 64 K words.

The address bus, data bus, and the transfer control signals may be configured for either two-state or threestate operation. Use of the three-state address mode reduces the number of external components required for a DMA processor interface.

## C0MBINATION RAM/PLD OPENS NEW APPLICATION OPTIONS Packing 2048 Bits Of RAM Plus Four 500-Gate Configurable Logic Blocks Lets An EPLD Compete With Standard Cells, Arrays.

Dave Bursky



A LARGE BLOCK of configurable memory (with associated configurable control logic) starts off as four independent 64 -word-by-9bit blocks. The blocks can be concatenated to form any register organization from 256 -by- 9 to 64 -by- 36 . FIF0, LIF0, registerfile, or static-RAM type memory functions can be created. The memory blocks are interconnected to each other and to the four logic blocks on the chip through a universal interconnection matrix that routes all signals. Each logic block contains the approximate equivalent of 500 configurable gates.

If system designs require more than a few bits of data storage, erasable program-mable-logic devices (EPLDs) are often ruled out in favor of gate arrays or standard-cell ICs. That's because data storage cells (registers or memory blocks, such as FIFOs, dual-port RAMs, or even standard static RAMs) are typically implemented inefficiently on most PLD architectures. By incorporating dedicated but configurable blocks of RAM on its its H5110 intelligent data buffer PLD chip, Plus Logic has circumvented this PLD shortcoming.

The CMOS chip includes four blocks of RAM, each organized as 64 words by 9 bits and configurable either as four independent blocks or combined in any mix to form deeper or wider memory blocks (see the figure). Each 64 -word block can serve as a dual-port RAM or two 32-by-9 single-port RAMs. Control logic associated with each block enables users to configure the memory function. Each memory block contains the equivalent of about 4000 usable gates. About 1500 of those gates form the 576 bits of RAM, the rest are used for the control functions. To implement all four memory blocks with typically achieved efficiencies

## BEND THE LICHT, NOT THE LEADS.



## INTRODUCING PRISM CBI ${ }^{\text {SM }}$ THE FIRST TRUE SURFACE MOUNTABLE LED INDICATOR.

The new surface mount CBI from Dialight is another breakthrough idea whose time has come. Instead of bending the leads on a through-hole version to make it look like a surface mount device, Dialight uses a patented high transmission prism and clear lens to bend the light from an upwards-facing surface mount LED. This approach offers a uniform illumination of the lens over a wide viewing angle. Finally, a truly leadless indicator developed for reflow-soldering and compatible with a wide variety of pick and place equipment.

The PRISM CBI is available in T-3/4 $(1 \mathrm{~mm})$, T-1 ( 3 mm ) and T-1 3/4 ( 5 mm ) lens sizes. This unique product is offered in package sizes of $0.130 \times 0.098 \times 0.138$ for the T-3/4, 0.240 x $0.185 \times 0.200$ for the T- 1 and $0.250 \times 0.245 \mathrm{x}$ 0.282 for the T-1 $3 / 4$ size.

The introduction of the PRISM CBI means there is one less component on the board that has to be through-hole mounted because now a reliable surface mount version exists. Using this approach, an extremely high "post-process" reliability rate can be achieved.

Available in red, yellow or green, packaged in ESD-shielded tape on EIA standard 7" or 13" reels, the PRISM CBI is ready for a whole spectrum of demanding SMD applications.

For more information, contact:
Dialight Corp., 1913 Atlantic Ave.,
Manasquan, NJ 08736; Tel.: (908) 223-9400
Fax: (908) 223-8788.
ALL INDICATIONS ARE
DIALIGHT
on a conventional PLD would require a PLD with the equivalent of about 25,000 gates.

The chip also has four programmable logic-resource blocks that each contain about 500 gates, enough to replace between 4 to 6 SSI or MSI logic functions. The four logic-resource blocks are equal to about the same amount of logic as that on the company's previous programmablelogic chip, the H2010. The H5110 is the second programmable architecture released by Plus Logic, but it still employs the basic high-level ar-chitecture-a universal interconnection matrix surrounded by blocks of programmable logic. The chips make up the company's Hiper (hierarchically interconnected, programmable, efficient resources) architecture, and employ UV EPROM-based control elements for configuration.

With the on-chip memory and logic combination, the H5110 can efficiently implement specialty memory blocks, such as intelligent first-in/ first-out memories, buffered memory controllers, register files, multichannel DMA controllers, and dualport buffer memories. These memory functions can be used in high-performance LAN and hard-disk controllers. Furthermore, as evidenced by the 9 -bit width of each block, parity is carried through the chip. There are eight parity generation and checking units on the chip, two associated with each of the four memory blocks.

Initial versions of the intelligent data-buffer chip will be released for operation at 33 MHz . By year's end, the company expects to have $40-\mathrm{MHz}$ versions available. With all four memory blocks transferring data at 33 MHz , the buffer delivers an aggregate data-transfer rate of 132 Mbytes/s when writing data to or reading data from the RAM blocks. A typical configuration of the RAM/ logic block might consist of an asynchronous 64 -by- 9 zero-fall-through FIFO buffer. Such an option would require about 3000 gates on a gate array to implement the memory and control functions, vs. just one memory/logic block in the H5110.

When configuring the memory
block to be a FIFO buffer, designers can make it either unidirectional or bidirectional, and can set up flags that indicate various memory-status conditions-More Data or Full/ Empty, and Threshold. Counters formed from the memory-cell logic provide the addresses-one for port A and the other for port B of the FIFO block. Each port can have two flags, one that can be configured to request more data and serve as an Acknowledge signal in response to a FIFO request (a handshake). That flag line can also be configured to serve as a traditional Full/Empty warning signal. Another internal register lets users set a threshold value to generate a flag signal once that value is exceeded. The register can thus be used as a tapped delay line for digital filtering applications.

As with all commercial FIFO registers, the flag logic has to deal with the possibility of two independent, asynchronous signals coming in simultaneously. As a result, the logic must be metastable hard. The basic physics principles show that metastability can't be removed, but its probability of occurring can be reduced. The H5110 is designed so that if 1000 parts run at full speed for one year, only one error will occur.

Because the logic is configurable, the FIFO control circuits can also be set so that the FIFO mode can be suspended and the memory accessed, as with a standard RAM. The FIFO mode could then be reentered-a handy feature for DSP- algorithm execution. Both synchronous and asynchronous FIFO configurations can be implemented. The same memory block can also be configured as a hardware stack by setting the logic to turn the memory into a last-in/ first-out memory. The memory can also be configured as one or more register files (single- or dual-ported) or treated as simple static RAM.

Due to the memory array's flexibility, offering just one package option of 144 pins for the maximum 36 bit memory bus didn't make sense, explains Cecil Kaplinsky, Plus Logic's R\&D vice president. Rather, one option at 144 pins for 32 - or 36 -bit systems, and another option at 84 leads
for 9- and 18-bit systems, gives users a better cost match to their application. The lower-priced 84 -lead package also saves board area.

On the 144-lead version, there are two 36 -bit buses that can be used for memory data transfers or for logic control (if not needed for the RAM). In addition, 16 lines are initially allocated for memory-control functions; when not employed for that, they can serve as logic-control inputs. Another 18 lines either serve as either output status flags for the memory blocks or as bidirectional signal lines for the logic section. The chip also has three clock lines and close to 20 power and ground lines. The 84-lead version has two 18 -line buses, 16 log-ic-only input lines, 8 memory control or logic inputs, 8 memory flags or logic-control lines, 3 clock lines, and 13 power and ground lines.

To configure the chips, Plus Logic developed an upgraded version of its PlusTran toolkit, which contains the cell library and the various logic-capture, simulation, and place-and-route tools. The library will contain many new blocks in comparison to the original PlusTran library for the H2000 array family. The PlusTran system will translate logic net lists into the configuration bit maps needed to program the $5110 . \square$

## Price And Availabilty

Samples of the H5110 will be available in July. The one-time programmable version, set up for 9- or 18-bit-wide memory accesses, is housed in an 84-lead plastic leaded chip carrier and goes for $\$ 50$ in lots of 1000 ( $33-\mathrm{MHz}$ version). A version set up for wide-word-memory accesses (36 bits) comes in a 144-lead plastic quad-sided flat package and sells for $\$ 80$ in 1000-unit lots. Windowed ceramic pin-grid array packages house the reprogrammable versions. The PlusTran development tool set starts at $\$ 475$ for the behavioral-entry system, and goes up to $\$ 975$ when one schematiccapture library for the desired schematiccapture package is added. Tools will be available next month.
Plus Logic Inc., 1255 Parkmoor Ave., San Jose, CA 95126; Gary Banta, (800) 2537587.

CIRCLE 515



The Power in Telecommunications

## How component power is contributing to the future of telecom networks

Of all the developments in the $1990^{\circ}$ 's, advances in telecom technology may well have the most profound impact on our daily lives.

The integration of speech/data and video technology, computers and communications systems will bring businesses and individuals closer together But as the power of communications increases, so must its reliability. And nowhere is that more important than in the power supplies which power the systems.

Here, Ericsson has been at the forefront of technology for decades, and is ready to provide many more innovative, highly reliable solutions in the years to come.

When the PKA DC/DC converter was launched in 1983 it represented the first real power supply 'component', starting a trend towards distributed power architectures which has gained global acceptance.

$$
\text { In } 1988 \text { these } 25-40 \text { Watt units were complemented by } 15-18 \text { Watt }
$$ DC/DC converters in the PKC series. Power components the size of a credit card.

Both series boast a remarkable MTBF of over 200 years.
Ericsson continues to lead the way in smaller, more reliable power supplies for advanced power architectures. They are vital components enabling technologies which shape the telecom networks of the future.

A complete technical information pack is just a 'phone call away. Alternatively, just fax us the coupon.

Please send me your latest information

Name

## Company

Job Title
Address

[^9]
# Micropower Low-Dropout Regulators Snap 0n And 0ff At Dropout frang Goodenoch 

The latest low-dropout (LDO) linear regulators from Na tional Semiconductor, the LP2952/LP2953/LP2954, offer true micropower operation. Moreover, the first two add a new twist-they snap on and snap off at the dropout-voltage threshold.

Ideal for battery-powered circuitry and for regulating and reducing noise on the auxiliary outputs of switching supplies, LDOs provide precise, low-noise, linear regulation while operating with minimum in-put-to-output voltage. Their minimum quiescent current (efficiency), particularly for battery operation, is vital.

In many applications (for example powering a microcontroller and/or a data-acquisition system feeding it), if the supply rail drops below some predetermined voltage, it's best to pull the supply rail to zero quickly. The highly efficient LP2952/LP2953 can do just that with the aid of a pair of on-chip comparators (see the figure). The first, called the "dropoutdetection comparator," senses the LDO's output and fires (its output goes low) when the LDO's output drops about $5 \%$ below its preset value. This signal can be used as a system error flag.

In addition, if the error flag is connected to the "shutdown comparator," the pnp transistor on the output of this second comparator will crowbar the LDO's output to within 400 mV of ground. The dropout detector has 60 mV of hysteresis, while the shutdown circuit's hysteresis is 6 mV . The LP2953 is identical to its sibling with the exception of an additional undedicated comparator, which delivers CMOS/TTL-compatible output levels.

Both devices guarantee a minimum output current of 250 mA and the output voltage can be set between 1.23 to 29 V with an external divider. Alternatively, strapping pin 5 to pin 8 provides a 5 -V output. Both come in a 16 -pin SOIC. In addition,

the LP2952 comes in a 14-pin DIP and the LP2953 in a 16 -pin DIP. The LP2954 also comes in a standard 3pin TO-220 package. It can drop in to the socket of an LM340, a 1-A conventional linear regulator that needs at least 2.5 V across it, regardless of load current.

While the LP2954's specifications match those of the DIP units, its output is fixed at 5 V and it contains no extra comparators (although snapping versions will appear this year). Its higher power dissipation adapts it to handling a wide range of input voltages (for example, those found in automotive applications). Moreover, the pnp pass transistor provides inherent protection against reversebattery connection.

Operating from -40 to $+125^{\circ} \mathrm{C}$ with a 6 -V input and a $5-\mathrm{V}$ output, all three LDOs feature dropout-voltage ranges from 150 mV with a $1-\mathrm{mA}$ load to 800 mV with a $250-\mathrm{mA}$ load. Over a similar load range, quiescent current varies from $200 \mu \mathrm{~A}$ to 33 mA . Output voltage for AL-grade units runs between 4.94 and 5.06 V , and be-
tween 4.9 and 5.1 V for L-grade devices. Output-voltage line regulation runs between $0.2 \%$ and $0.5 \%$, while varying the input from 6 to 30 V , depending on LDO IC grade. Output load regulation runs between $0.2 \%$ and $0.3 \%$, while varying the load from 0.1 to 250 mA , again depending on grade. The current limit for all grades at 0 V out is 530 mA . Output noise from 10 Hz to 100 kHz with a $100-\mathrm{mA}$ load typically runs between 80 and $400 \mu \mathrm{~V}$ rms, depending on circuit capacitance added by the user. Up to $200-\mu \mathrm{A}$ can be drawn from the $1 \%, 1.23$-V reference used in the DIP devices.

In quantities of 100, L-grade units start at $\$ 2.00, \$ 2.35$, and $\$ 2.30$ each for the LP2952, LP2953, and LP2954, respectively. Small quantities are available from stock. Tighter-tolerance A-grade units will be available by mid-year and military-grade units in the fall.

National Semiconductor Inc., P.O. Box 58090, Santa Clara, CA 95052-8090; Parag (Coco) Patel, (408) 721-7509

CIRCLE 620

## PCB PROTOTYPER HANDLES MULTILAYERS

By using the System Two same-day prototype-pc-board manufacturing system, a multilayer pc board can be built in the lab in a matter of hours, rather than the weeks it may take at a job shop, at a much lower cost. The complete system includes a plotter/etcher to image and etch the circuit layers, an automatic driller/router, an optical punch to align the layers, and a laminator. Any board up to 11 by 14 in. can be built using the system. A complete system goes for $\$ 39,950$. Delivery is in six weeks from receipt of order.

Direct Imaging Inc., 2 Technology Dr., Airport Industrial Park., West Lebanon, NH 03784; (603) 298-8383.
Clicle 621

## SMT PLACEMENT SYSTEM SPORTS HIGH VOLUME

A wide range of component types, from small chips and MELFs to large PLCCs and QFPs, can be handled by the MCM 8 surface-mounted placement system from Philips. The system is claimed as the world's fastest software-controlled large-chip placer, achieving rates of 31,000 placements per machine per hour. The unit will feed from tape, bulk, stick, tray, and other types of feeders, and will accommodate boards up to 18 by 20 in . Overall placement accuracy is $\pm 0.15 \mathrm{~mm}$. Machine-vision and me-chanical-component alignment are provided for large fine-pitch components. The vision software package detects bent component leads and compensates for circuit-pattern misalignment.Call for pricing and delivery.

Philips Industrial Automation Div.,
2975 Courtyards Dr., Norcross, GA 30071; (404) 368-4420. CIRCIF 622

## HIGH STABILITY MARKS PHOTOTOOL FILM

The world's best humidity coefficient for phototool film- $0.0009 \%$ per \%RH-is claimed for the AccuMax 2000 film products. That means higher dimensional stability, less film movement, and improved film registration. Manufactured in a class-100 clean room, the films are shipped in packaging that eliminates contaminating particulates. Call for pricing and delivery.

Eastman Kodak Co., 343 State St., Rochester, NY 14650-0518; (716) 7244000. HIBCIF G23

## HIGH-HEAT NYLON TOUGHENS CONNECTORS

A material with excellent high-heat resistance significantly improves connector performance. Ranoda Electronics, Anaheim, Calif., for example, used the material, Stanyl 46 nylon, for a line of close-tolerance connectors that retain dimensional stability despite infrared, wave, and vapor-phase soldering. The material comes in reinforced grades for applications calling for low creep and resistance to heat distortion to $545^{\circ} \mathrm{F}$, as well as exceptional fatigue resistance. Call for pricing and delivery.

DSM Engineering Plastics N.A., 501 Crescent Dr., Reading, PA 19612; (800) 336-6923. GIRCIF 625

## SOCKET HANDLES CRYSTAL OSCILLATORS

Standard full-can, metal-case clock oscillators will find a home in the DCO 304-014B-ST socket, which features integral $0.020-\mathrm{in}$.-high molded standoffs. The socket is molded of UL 94-VO-rated glass-filled polyester thermoplastic, and uses multifinger contacts that accept round leads ranging from 0.015 to 0.025 in. in diameter. Contact resistance is rated at less than $10 \mathrm{~m} \Omega$ per contact with a maximum current rating of 3 A . Pricing is $\$ .24$ each in lots of 500 . Delivery is from stock.

McKenzie Technology, 44370 Old
Warm Springs Blvd., Fremont, CA 94538; (415) 651-2700 GHICIF E26

## D-SUB STANDOFFS CUT HARDWARE NEEDS

Rather than using a handful of loose hardware to mount D-subminiature connectors, the DSOS Connect'r Ware standoffs greatly reduce handling, inventory, and assembly costs. The selfclinching standoffs become a permanent fixture of the chassis, which prevents them from dropping inadvertently into circuitry. Installation simply involves pressing the standoffs into a properly drilled hole. The standoffs come in 303 stainless steel and in thread sizes \#4-40 and M3. They accommodate panels ranging in thickness from $0.037-\mathrm{in}$. to $0.250-\mathrm{in}$. Call for pricing and delivery.

Penn Engineering and Manufacturing Corp., 5190 Old Easton Rd., Danboro, PA 18916-1000; (215) 766-8853.
GIRGIF 24

# Model-Building Tool Assists Mixed-Level analog Simulation 

Behavioral simulation is now possible in Valid's analog design system-Analog Workbench II-with the addition of Profile. The Profile model-building software lets users describe blocks or entire circuits at the behavioral level in a combined text-graphics environment. Users then simulate those models in the Workbench mixed behavioral- and structural-level environment. With Profile working in Analog Workbench II, designers can adopt both top-down and bottom-up strategies.

Profile is easy to learn and use. Its graphical user interface offers an alternative to language-based behavior-al-modeling techniques. The Profile models support user-specified error and warning messages, which allow for in-process circuit diagnostics. In addition, the models can incorporate effects not supported by macromodeling, such as hysteresis, memory, state variables, and conditional branching. Users can build piecewise linear models, which support high-speed analysis.
Although primarily suited to analog electronics, Profile can also describe such electromechanical devices as mo-

## PLD T00LS SUPPORT TW0 MORE DEVICE VENDORS

Version 2.1 of the PLDesigner pro-grammable-logic tools supports devices from PLX Technology and Hyundai Semiconductors. The software also supports many new device architectures, including the Cypress CY7C336339 series, the Signetics PLC415, and AMD's PALCE24V10. In addition, such enhancements as automatic DeMorganization are included in this release. PLDesigner automatically generates DeMorganized equivalents of all equations in a design and selects the equation that utilizes the fewest device resources. Automatic DeMorganization increases PLDesigner's flexibility when partitioning a design into devices, because devices with either high or low true outputs are available to the fitter. PLDesigner Version 2.1 runs on the Sun Sparcstation and 286- and 386based PCs. Pricing starts at $\$ 1950$ for the PC and $\$ 3950$ for the workstation.
Minc Inc., 6755 Earl Dr., Colorado Springs, CO 80918; (719) 5901155. CIIGIF 628

tors, solenoids, and sensors. Users can also build mixed analog-digital models like data converters.

After Profile models are created, After Profile models are created,
they're simulated at the block level in the Analog Workbench II system. This
system can perform mixed-level simuthe Analog Workbench II system. This lations containing behavioral- and tran-sistor-level circuitry.

Profile is offered as an option to Analog Workbench II, which runs on DEC, IBM, and Sun workstations. It will be available by the end of the second quarter for $\$ 15,000$.

Valid Logic Systems Inc., 2820 Orchard Pkwy., San Jose, CA 95134; (408) 432-9400. GIBGIF 627

LISA MALINIAK also build mixed analog-digital models

## SCHEMATIC CAPTURE HAS INCREMENTAL COMPILING

The newest version of the Schema sche-matic-capture software, Schema III 3.3 , boasts an incremental-compiling post processor. With incremental compiling, design sizes are limited only by hard-disk space. Version 3.3 includes network compatibility. In addition, user productivity is increased with new parts-creation routines, parts-label swapping, dynamic rubberbanding for regions, and new drawing-editor commands. A switch lets users toggle in and out of high-resolution VGA graphics. Schema III 3.3 includes the Schema Integrated System Manager, which controls the flow of data through schematic capture, simulation, PLD design, pc-board layout, text editing, and desktop publishing. The whole Schema III system, including the data manager, costs $\$ 495$ and runs on personal computers. Call the company for a free demonstration disk.

Omation Inc., 801 Presidential Dr., Richardson, TX 75081; (800) 5539119. CIIGIE 629

## LIBRARY ACCURATELY M0DELS RF TRANSISTORS

Designers can accurately simulate linear and nonlinear RF transistors with a new Spice model library from Intusoft. The library has models for 36 foreign and domestic bipolar transistors and JFETs that can be used with any Berkeley Spice-compatible simulator on any computer platform. The models employ a custom subcircuit approach that accounts for all package parasitics and matches the published S-parameter magnitude and phase data up to 5 GHz . Several test circuits and schematics are included with the library. The models and circuits are available on floppy disks in DOS and Macintosh formats for $\$ 99$.
Intusoft, P.O. Box 710, San Pedro, CA 90733-0710; (213) 833-0710. CIRGLE 630

## DESIGNERS CAN TARGET AMD'S MACH DEVICES

Engineers using Isdata's PLD design software can now target AMD's MACH family of devices for their designs. Isdata is the newest member of AMD's Fusion PLD program. Version 3.3 of Isdata's LOG/ic software compiles and simulates the MACH110 and 210 devices. Because the LOG/ic syntax is device-independent, existing PLD designs can be recompiled for implementation in MACH devices. Version 3.3 of the LOG/ic software, which runs on PCs, is shipping now. Pricing starts at $\$ 1480$.
Isdata Inc., 800 A irport Rd., Monterey, CA 93940; (408) 373-7359. CHRGIE E31

## P-CAD SOFTWARE RUNS ON IBM RISC MACHINES

P-CAD's Premier PCB pe-board design package now runs on the IBM RISC/ 6000 workstation, expanding the P CAD design environment to include DOS, IBM, and Sun platforms. Users on a Unix-based network can access the software through a low-cost IBM Xstation 120 or compatible. Premier PCB consists of schematic capture, pc-board layout, an automatic router, and specialized options. P-CAD's Database Interchange Format facilitates bidirectional transfers of all files between DOS and AIX. Single copies of Premier PCB cost between $\$ 10,800$ and $\$ 19,800$, depending on options. Multiple licenses for a network environment are discounted.

P-CAD, the EDA Div. of Cadam Inc., 1290 Parkmoor Ave., San Jose, CA 95126; (408) 971-1300. GIRCIF 632 $\begin{array}{llllllllllllll}\text { E } & \mathrm{L} & \mathrm{E} & \mathrm{C} & \mathrm{T} & \mathrm{R} & \mathbf{O} & \mathrm{N} & \mathrm{I} & \mathrm{C} & \mathrm{D} & \mathrm{E} & \mathrm{S} & \mathrm{I}\end{array}$

## 12-BIT-ACCURATE,

 5-V REFERENCE CHANGES JUST $2 \mathrm{PPM} /{ }^{\circ} \mathrm{C}$With the ability to source and sink 10 mA , the LT1027, a 5V voltage reference, sports the lowest drift of any unheated IC voltage reference. The output temperature coefficient (TC) of the premium A grade runs $2 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ maximum. Moreover, its minimum initial accuracy is within $0.02 \%(1 \mathrm{mV})$ of 5 V . A trim pin permits an external potentiometer or DAC to set the output closer to 5 V without degrading its TC. The chip's major application is as the reference for 12 -to-16-bit ADCs and DACs. These will include not only the many available IC converters which are built on CMOS processes without a reference, but also the many 12 -bit or more converters whose on-chip references typically show TCs at least 5 or 10 times that of the LT1027A. Its TC is $80 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$.

Indicative of the LT1027's intended use with successive-approximation ADCs is its fast-settling output op amp. The op amp's output typically gets back to within $0.01 \%$ of its original value in just $3 \mu$ s after sourcing or sinking a full-scale current pulse. The $10-\mathrm{mA}$ output also permits the reference to provide clean, regulated $5-\mathrm{V}$ power for a low-power ADC, such as Linear Technology's 12 -bit LTC1290. In quantities of 100, the LT1027A in a TO-39 can goes for $\$ 12.00$. The D grade (lowest), which still has a TC of $7.5 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$, runs $\$ 4.50$ each in a miniDIP.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035;
Bob Scott, (408) 432-1900. GIGGIF 683

- FRANK GOODENOUGH


## Wideband Amplifier RUNS ON LOW POWER

Most users know that op amps with full-power bandwidths beyond even a few megahertz are power hogs. However, the latest current-feedback IC op amp from Comlinear-the CLC406belies such "conventional wisdom." Running off $\pm 5$-V supplies at a closedloop gain of $6(15 \mathrm{~dB})$ and putting 5 V pkpk across $100 \Omega$, the op amp sports a minimum $3-\mathrm{dB}$ bandwidth of 95 MHz and its response is flat within 0.6 dB at 50 MHz . But it draws less than 5.5 mA from the supply rails with no load-that's just 50
mW . Linear gain and phase are $0.04 \%$ and $0.04^{\circ}$, respectively, for both NTSC and PAL TV signals. For a 2-V pk-pk output driving $100 \Omega$ at 20 MHz , second- and third-harmonic distortion run -42 and -43 dB , respectively. Time-domain specifications reflect those of the frequency domain. Slew rate runs a minimum of 1200 $\mathrm{V} / \mu \mathrm{s}$; the output settles in under 15 ns
(maximum) to $0.05 \%$ of final value for a 2 $V$ step. Applications range from video distribution and photodiode transimpedance amplifiers to high-speed DAC output amplifiers and driving flash ADCs. The CLC406 is $\$ 4.24$ in hundreds.

Comlinear Corp., 4800 Wheaton Dr., Fort Collins, CO 80525; Tom Baldwin, (303) 226-0500. GIBGIF 634


> HICH
> QUALITYI
> LOW COST STATE-OF-ART PERFORMANCE

EG\&G Vactec's complete line of planar silicon photodiodes-the cost-effective way to detect light, from ultra-violet through near-infrared.

Excellent linearity in output signal versus light intensity, low noise, and fast speed of response often make them the ideal detector
for automotive, communications, and medical instrumentation applications. They are used in smoke detectors, cameras,
security systems, X-ray detection equipment, flame monitors, encoders, bar code scanners, colorimetric analysis equipment, and other products.
Stock and custom devices are available packaged as discretes or configured into arrays, screened or modified to
meet particular demands.

[^10]
# Tiny Surface-Mount Trimmers are Sealed Against Processing 

Apair of 3 - and 4 -mm single-turn trimmers features breakthroughs in seal design that makes them more suited than ever for surface-mounted-assembly processing. The sealed $3-\mathrm{mm}$ model 3313 and elastomer-sealed 4-mm model 3374 can withstand all popular soldering processes, including wave soldering. The trimmers can take up to $260^{\circ} \mathrm{C}$.

Model 3313 is the industry's only sealed $3-\mathrm{mm}$ trimmer with a resistance range of $10 \Omega$ to $2 \mathrm{M} \Omega$. Until now, designers were restricted to devices with a resistance range of $100 \Omega$ to $1 \mathrm{M} \Omega$. In the 3313, they'll find a device that's suited to a broader range of industrial, commercial, and consumer applications. Contact-resistance variation (CRV) for the device is $2 \%$ maximum and is typically under $1 \%$.
The model 3374 is the industry's first elastomer-sealed, chip-style 4 -mm trimmer with a five-turn seal life. Gone are

the devices with temporary seals that were either punctured or peeled off before adjustment, leaving the trimmer vulnerable to contaminants. The unit has the same resistance range as the 3 mm trimmer. Maximum CRV is $3 \%$.

Sample orders for both models will be accepted in June with an eight-week lead time. In lots of 1000 , prices start at $\$ 0.87$ for the 3313 and $\$ 0.60$ for the 3374 .

Bourns Inc., 1200 Columbia Ave., Riverside, CA 92507; (714) 781-
5071. CIBCIF 635

DAVID MALINIAK

## Telecommunications Relay MEETS BELLCORE SURGE STANDARD

Designed to meet the emerging worldwide standards for the telecommunications industry, the G6N 12-pin DIP relay features smaller size, lower power consumption, and considerably higher surge-withstand capability than the 16 -pin DIP relay that's been the telecom-industry

standard for some seven years. A principal feature of the relay is its $2.5-\mathrm{kV}$ surge-withstand voltage between coil and contacts. That's a significant improvement compared with the $1.5-\mathrm{kV}$ requirement of the previous operative standard, which was defined by FCC Part 68.

The relay has a 2 Form C (doublepole, double-throw, single-break) contact arrangement and a maximum switching current of 1 A . Also featured is high sensitivity with a power consumption of 140 mW standard. Service life is rated at 100 million operations The device's package measures 11 mm high by 7.5 mm wide by 15 mm long.
Thanks to a full immersion seal, the relay is impervious to water-solubleflux cleaning methods. Relays will be available on both tape, and reel and tubes. It also can be modified for sur-face-mounted assembly.

Mass production is scheduled for June. List price per unit is $\$ 4.05$.

> Omron Electronics Inc., Control
> Components Division, One E. Com-
> merce Dr., Schaumburg, IL 60173;
> (708) 843-7900. GIRGIF 636

> DAVID MALINIAK

## Two AcTuator Types CONTROL MOVEMENTS

Both electrostrictive and piezoelectric materials are used in a line of electroactive actuators. The devices, which control extremely small, rapid movements, are offered in rectangular, cylindrical, and bimorph configurations. They operate by providing displacement in re-

sponse to an applied electric field. Hysteresis for piezoelectric devices is typically around $14 \%$ and creep is from 10 to $15 \%$. For electrostrictive devices, hysteresis and creep are typically less than $3 \%$. Pricing ranges from $\$ 400$ for single quantities to $\$ 50$ for lots of 10,000 . Lead times depend on parts, values, and quantities.
AVX Corp., 2875 Highway 501, Conway, SC 29526; Bharat Rawal, (803) 349-6264. GIBGIF 637

## 3-GHZ ATTENUATOR GIVES 60-dB CUT

Specifically designed for OEM instrumentation applications, the P3010 300kHz -to-3-GHz programmable attenuator features an insertion loss of 2.4 dB

maximum and a VSWR of 1.4:1. The small-outline device has a $60-\mathrm{dB}$ attenuation range, and can be adjusted in 10 dB steps. Repeatability is $\pm 0.2 \mathrm{~dB}$ at any setting, and accuracy is rated within $\pm 0.7 \mathrm{~dB}$ maximum. Other features include an isolated ground and a TTLinterface option. Price is $\$ 485$ in single quantities, and production units are available now.
Wavetek RF Products Inc., 5808
Churchman By-Pass, Indianapolis, IN
46203-6109; (317) 788-9351. EIRGIF 638

## VXI-BASED DIGITAL TESTER OFFERS FLEXIBILITY

Scalable architecture, comprehensive triggering for mixedsignal testing, and on-the-fly timing changes are some of the significant features of the VXIbus-based HP 75000 Model D20 digital functional test system. The system, which comes with its own menu-driven software, offers a $20-\mathrm{MHz}$ maximum data rate with $40-$ MHz clocks.

Components include the HP E1450A timing module, HP E1451/52A pattern I/O modules, and the HP E1496A digital test development software. All components are compatible with the Standard Commands for Programmable Instruments language. Pin-to-pin deskew and automatic compensation for podcable length enhance performance. Deep segmentable memory behind each I/O pin lets users download multiple tests simultaneously.
Each pattern-I/O module supplies 32 I/ O pins (four ports of 8 bits each), a $20-$ MHz pattern rate, and a 64 -kbyte pattern depth. Every port can output, record, or perform real-time comparisons. Users can three-state any port on-the-fly. The timing module can control up to 10 pattern modules. It provides timing generation for up to 320 data channels, master-slave capability to synchronize multiple mainframes, and

three independent timing generators (stimulus, response, and control). Tests can be synchronized with other equipment for mixed-signal testing.
Based on the X-Window System Version 11 and OSF/Motif, the software features a graphical interface and runs on HP-UX workstations. Users enter timing information as timing waveforms, with data entered independent of timing. The software can be used independently to develop digital tests using screens that help to create timing cycles and edit vector files.
A system with one timing module, one I/ O module, two pods, and the test development software costs $\$ 14,455$. Delivery is within 6 to 8 weeks.

Hewlett-Packard Co., Loveland Instrument Div., P.O. Box 301, Loveland, CO 80539-0301; (800) 7520900. GIVGIE 639

JOHN NOVELLINO

## GENERATOR OFFERS DATA PATTERNS T0 1360 MHZ

The PG-1400 digital-pattern generator supplies the high-speed stimulus signals needed for functional or margin testing of GaAs or fast ECL devices. The instrument provides eight complementary output channels at up to 680 MHz (8 bits by 16 kwords) or four complementary outputs to 1360 MHz (4 bits by 32 kwords). Output rise and fall times are 170 ps (typical). Outputs may be shifted (individually in four-channel mode, in pairs in eight-channel mode) over a range of $\pm 2 \mathrm{~ns}$ with 10 -ps resolution and better than $100-\mathrm{ps}$ accuracy. An IBM PC/AT or equivalent host is required. Software includes a pattern editor and pattern-generation and translation utilities. The PG-1400 costs $\$ 38,000$. Delivery is within 45 days.

Outlook Technology Inc., 200 E. Hacienda Ave., Campbell, CA 95008; (408) 374-2990. GTBGIF 640

## CPU MODULES OFFER 25-MHZ POWER FOR PCXI

Two 80486-based CPU modules bring $25-\mathrm{MHz}$ PC performance to the PCXI system. PCXI (PC Extended for Industry) is a modular, industrial architecture based on a 13 -slot passive backplane. The PX1240 includes up to 32 Mbytes of on-board system memory and 8 kbytes of internal cache memory. It also has floppy-drive and IDE harddrive interfaces. The PX1241 version features a VGA video controller with resolution to 1024 by 768 pixels. It contains a $3.5-\mathrm{in}$. floppy drive. Both units have one parallel and two serial ports. The modules, which are enclosed in a metal chassis for EMI/RFI shielding, run MS-DOS, Unix, OS/2, and Windows 3.0. The PX1240 costs $\$ 5495$ and the PX1241 goes for $\$ 5890$.

Rapid System Inc., 433 N. 34th St., Seattle, WA 98103; (206) 547-8311.
CIRGLF 641

## INTEGRATED SYSTEM AIDS IN i960 CA DEVELOPMENT

A fully integrated development system helps designers maximize the performance of systems based on the Intel i960 CA superscalar microprocessor. The package consists of the enhanced EL 3200 emulator, which runs at the full processor speed, Validate/XEL development software, and comprehensive service and support. The emulator offers real-time transparent emulation to 40 MHz with no wait states and supports the unique features of the 1960 CA, such as pipeline and burst modes and different bus widths. The Validate/XEL software includes a highly optimized ANSI-conforming C compiler created for the 1960 CA , an assembler, a disassembler, a source-level debugger, and a seamless interface to the EL 3200. The i 960 CA development system will be available July 1. Prices start at $\$ 35,000$.

Applied Microsystems Corp., 5020 148th Ave., Redmond, WA 98073-9702; (206) $882-2000$. GIREIF 642

## BOARD TESTER OFFERS FLEXIBLE FEATURE SET

The GR2288 is a compact, yet full-featured, combinational board tester. Each of the tester's 1152 fully hybrid, memory-backed pins can execute all types of tests: continuity, in-circuit,

functional, cluster, analog, digital, mixed-signal, memory, GPIB interfacing, and internal or boundary scan. Enhanced system software includes several new features. The system has comprehensive event triggering, eightwire analog-measurement capabilities, parallel memory-bank testing with automatically generated programs, and multiple timing sets. The GR2288 is available now, starting at $\$ 210,000$.

GenRad Inc., 300 Baker Ave., Concord, MA 01742-2174; (508) 369-4400.
CIRGIF 643

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## LITERATURE

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## PC-Based VMEbus B0ard Sutis CONTROL TASKS

0ptimized for control applications, the EPC-6 PC-based VMEbus embedded controller can be used as a standalone processor, with an embedded PC, or with another single-board computer. Because the controller is PC-compatible, PC applications run without any modification. Using a software environment called EPControl, users can develop software for the EPC-6 using standard PC-based development tools and an embedded PC as the development system.
The software-development environment for the EPC-6 uses the VMEbus as the high-speed communication path to and from the controller. With EPControl, users develop their application on the host using standard PC tools and debuggers, then download the application into the controller's on-board DRAM or flash memory.
The EPC-6 is based on a $20-\mathrm{MHz}$ 386SX microprocessor, with a socket for a 387SX math coprocessor. The board can also hold up to 4 Mbytes of dual-ported RAM, and 8 kbytes of bat-tery-backed SRAM. A 16 -kbyte instruction cache is included.
The board has a local EXM expansion bus that enables users to customize their boards by adding modules. The EPC-6 is priced at $\$ 1995$ in single quantities or $\$ 1495$ in OEM quantities. EPControl costs $\$ 1450$.

RadiSys Corp., 19545 NW Von Neu-
mann Dr., Beaverton, OR 97006;
(503) 690-1229. Clicle 644

RICHARD NASS

## CORRECTIONS:

On page 67 in the Apr. 11 Special Report "High-Resolution ADCs Up Dynamic Range In More Applications," the statement "Today, hybrid SARs, such as the 16 -bit AD1377 and ADC700 from Analog Devices, own the 12-to-16bit field" is incorrect. It should read "Today, .......the 16 -bit AD1377 from Analog Devices and the ADC700 from Burr-Brown, own the..." Ed.
Also, on page 52 in the Apr. 25 Special Report "DRAM Diversity Yields A Memory To Suit Any System," figures $A$ and $B$ in the sidebar were provided by Siemens Corp. Figure A was incorrectly referred to as a stacked-cell structure. The reference should have been a lateral-capacitor memory cell.

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put can swing 40 V below the ground, a feature that permits the regulator to perform positive to negative conversion with inputs down to 4.5 V . It also allows the use of a tapped inductor for output currents up to 10A with no external switching transistor. A true analog multiplier in the feedback loop lets it respond quickly to input voltage fluctuations. The LT1074 is available in either a 5 -lead TO-220 package or an 11-lead single-in-line package at $\$ 5.25$ and $\$ 6.45$, respectively, in 100 -up quantities. For a data sheet and applications note contact: Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035 or call 800-637-5545.


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[^5]:    1. A TYPICAL ANALOG COMMUNICATION reeciver may need several bandpass filters and demodulation circuits to support the bandwidth requirements and desired operating modes.
[^6]:    ${ }^{*} \mathrm{~V}_{\text {IID }}$-Dynamic Input threshold low ** $\mathrm{V}_{\text {HID }}$-Dynamic Input threshold high

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