ELECTRONIC DESIGN

MARCH 5, 1992

FOR ENGINEERS AND ENGINEERING MANAGERS--WORLDWIDE

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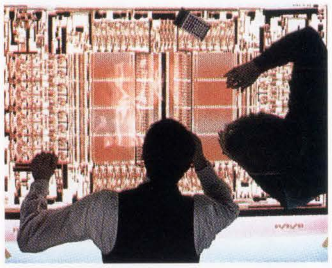

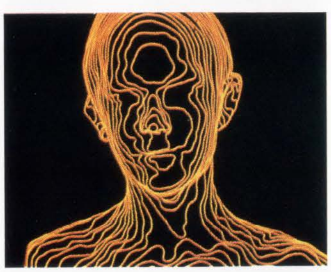

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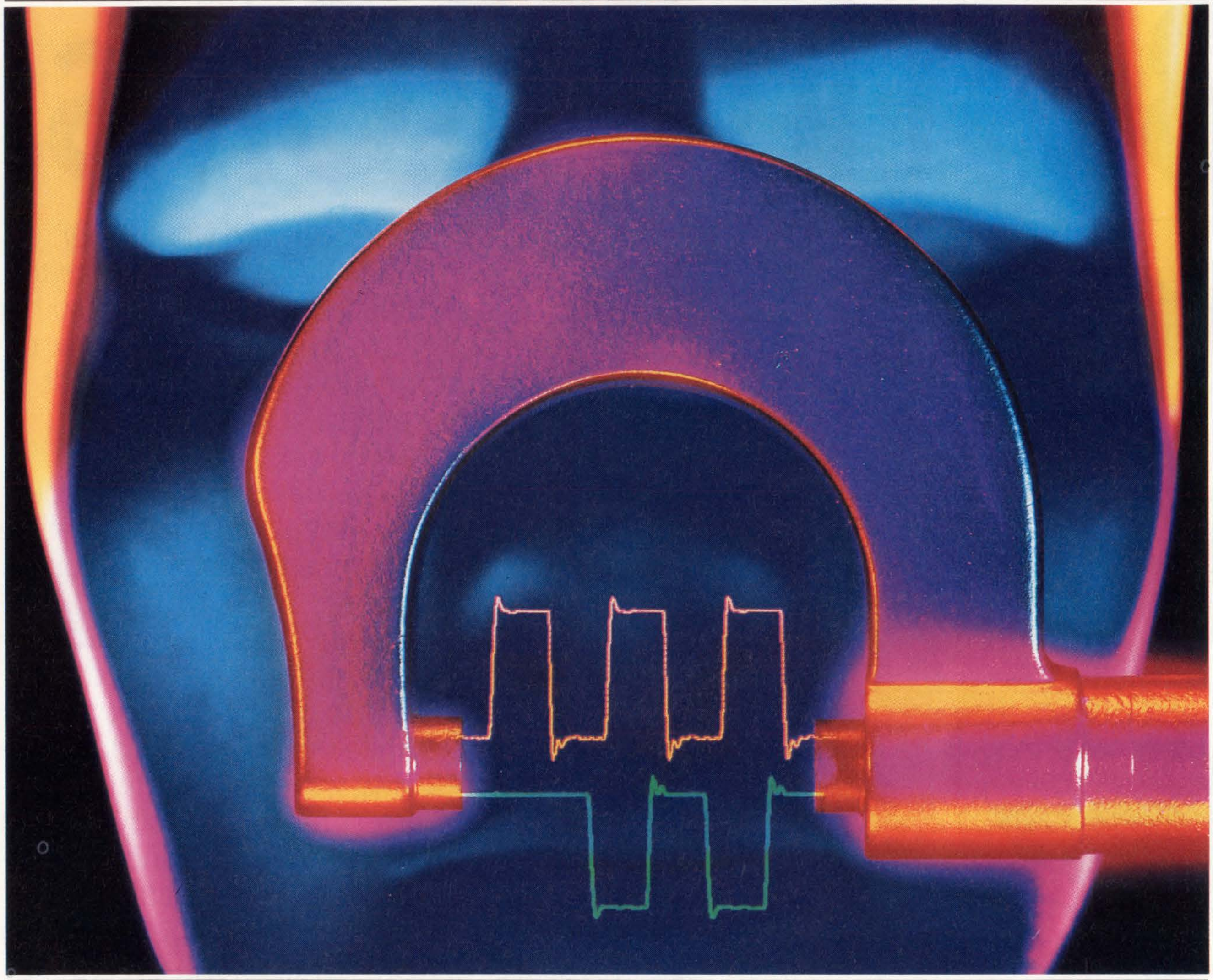
MARCH 5, 1992 VOL. 40, NO. 5

ELECTRONIC DESIGN



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- Special Report: Wireless data links broaden LAN options
- Using low-cost routers to help manage global networks
- New DRAM architecture and bus aim for 250-MHz operations
- First details on a dc-dc converter with today's highest power density
- New analog arrays hit the multigigahertz range
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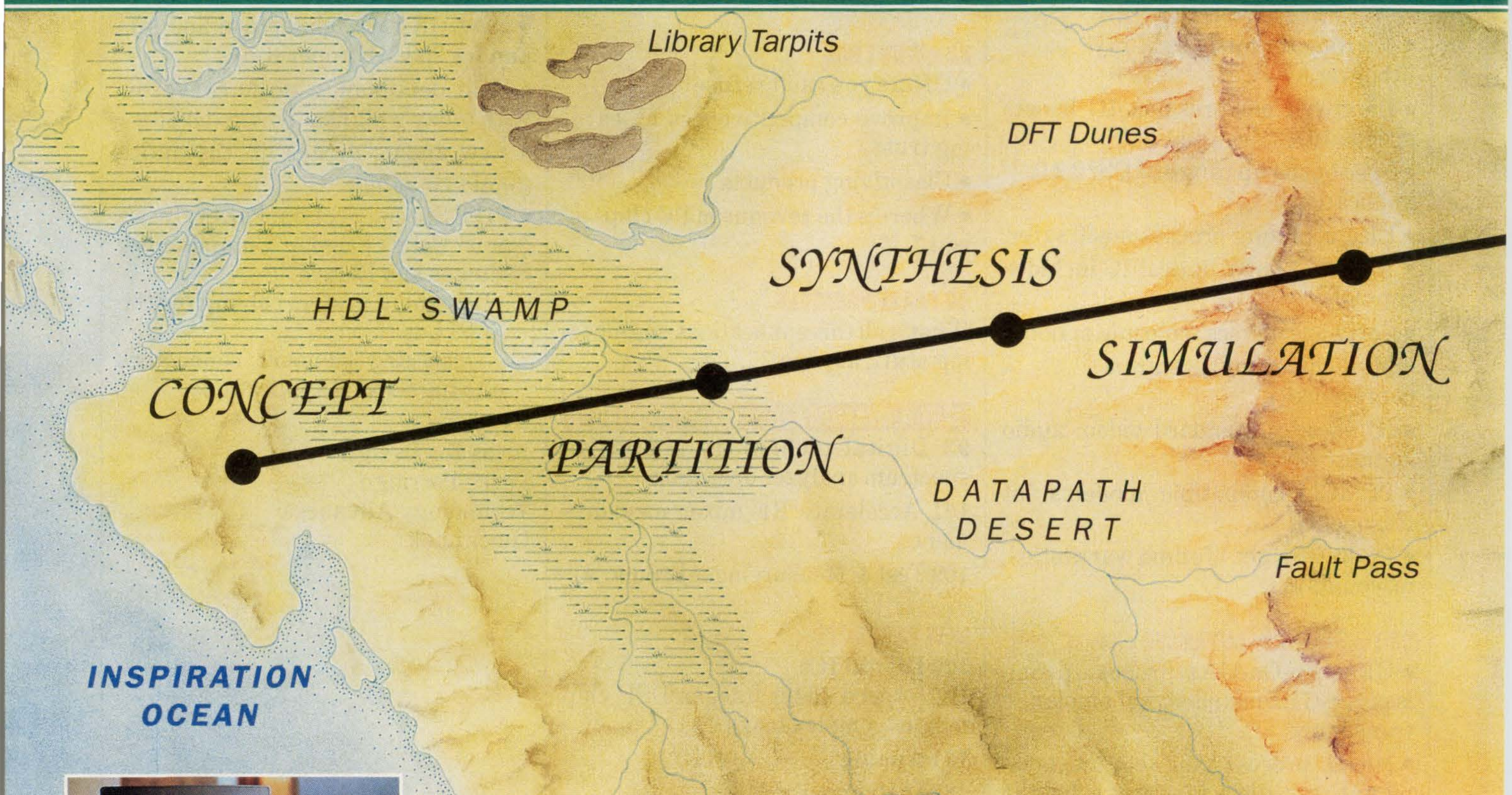
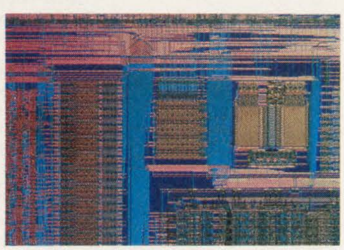
NAVIGATE THE PERILS OF TOP-DOWN DESIGN.



No one ever said the road to top-down ASIC design was easy. Along the way, there are all sorts of obstacles that can get you off track – and into trouble. More than one designer has gotten bogged down in the swamp of HDL programming, lost in the datapath desert, or tangled up in the timing jungle. And that's not even the half of it.



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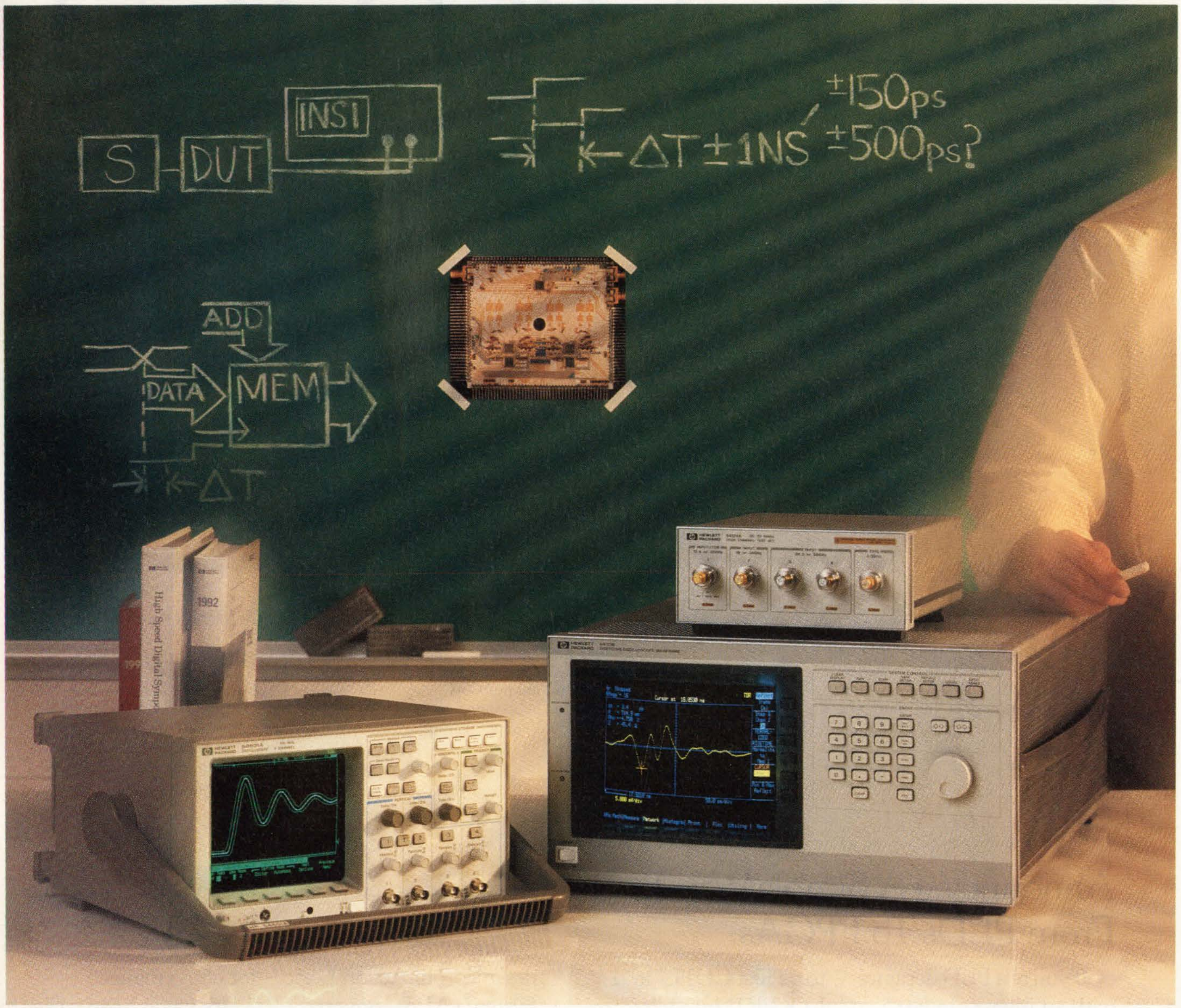

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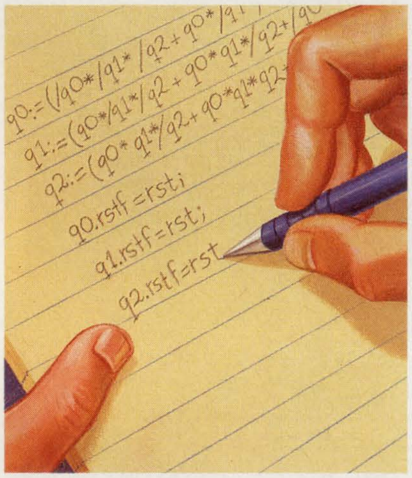

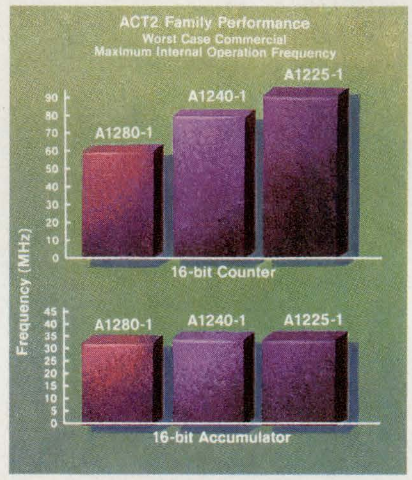

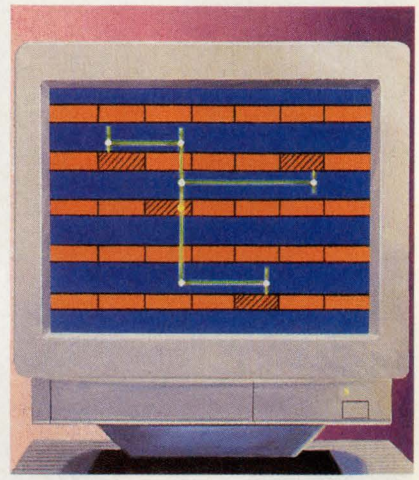

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'GAs The Same Way
e Similarity Ends There.

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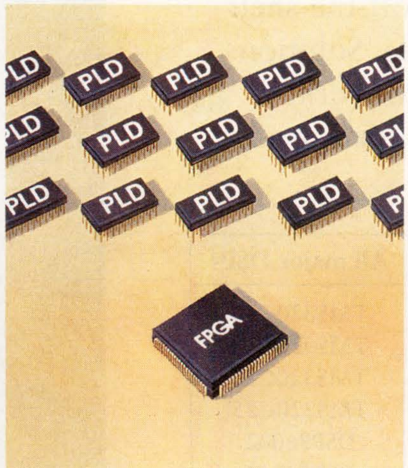

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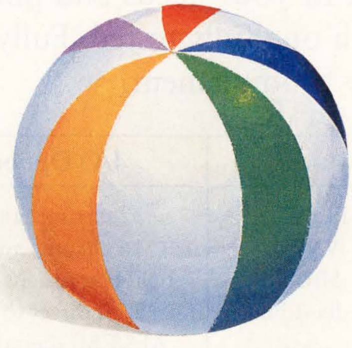

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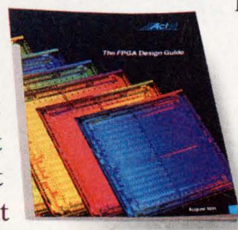

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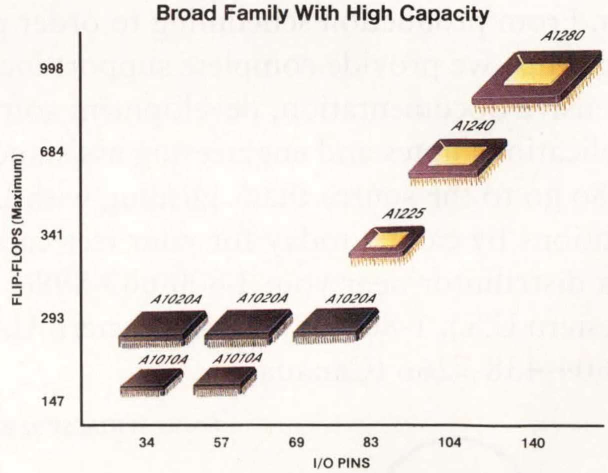

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		ADSP-21020
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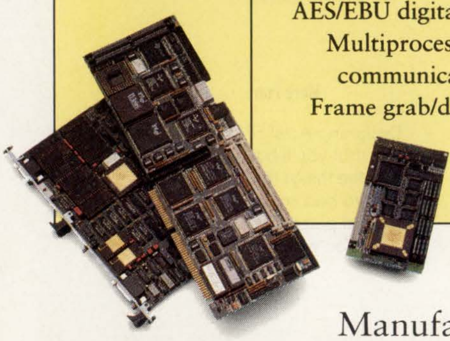
		DSP32C



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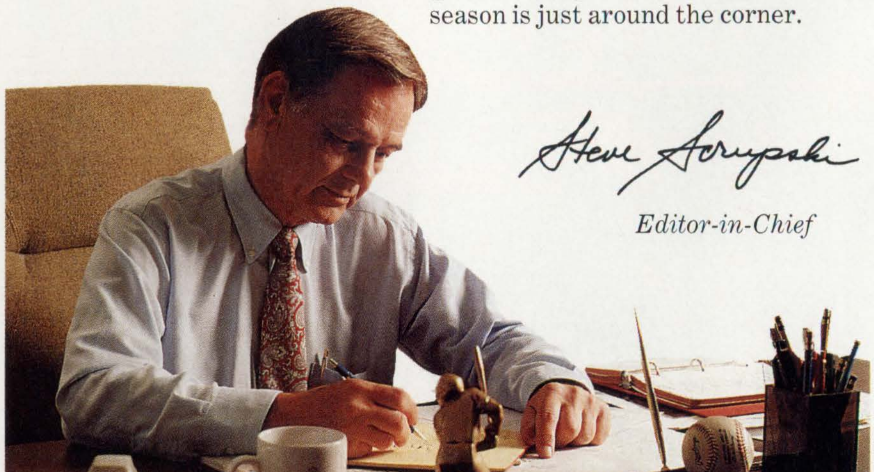
MORE MUSINGS ON I-80

In my prior column, I offered some thoughts that occupied me while inching through Interstate 80 traffic on the way to our Hasbrouck Heights, N.J. office. From the looks of things out on I-80, it doesn't appear that traffic will improve soon, so there's plenty of time to think about what's going on these days in this industry....*The growth of service industries* will undoubtedly continue, but manufacturing still is the primary means of creating wide-scale prosperity in today's world. The cost of electronics manufacturing equipment is rising rapidly because of increasingly complex technology. Therefore, to maintain a competitive pace, electronics manufacturers need more capital to invest in that equipment. Federal government officials, as the ultimate representatives of the people, must recognize that the electronics industrial world is changing and old hands-off rules impede progress and hinder prospects for future prosperity. They must foster cooperative development efforts among manufacturers and remove disincentives to large capital investments. In other words, take off the blinders, Washington, and for once think further ahead than the next election....*The headline in the New York Times* said "American Children Trail in Math and Science." An Educational Testing Service study showed that American 9- and 13-year-olds did poorly in these subjects compared with other children in other countries. Korean children did the best (but Germany and Japan weren't included in the study). Somehow, sad to say, these results don't seem surprising....*The semiconductor book-to-bill* ratio went up again in January to 1.08. That's five straight months of increases in this basic measure of future sales growth. But from what we hear, things are still pretty tough out there in the electronics business. Funny, watching the book-to-bill ratio steadily increase is like watching the sun rise earlier and earlier each day in the dead of winter. It's still pretty cold out there, but you know that spring is coming and things will soon be heating up—and that can't happen soon enough....*Maybe this winter is turning me into a curmudgeon,* but I noted in today's sports pages that my alma mater's (New Jersey Institute of Technology) basketball team has a won-lost record well above .500. I should feel good about their success, right? Well, not quite, despite my being a devoted sports fan. Put it this way: If the team is winning games, it must mean the players are practicing. That means they're spending more energy on practicing and less on doing their homework. And, if they're not doing all of their homework, then they're not doing what they went to that excellent technical institution for in the first place. That's one engineer's logic....*Oh well,* baseball season is just around the corner.



Editor-in-Chief

IN THE ERA OF MegaChip™ TECHNOLOGIES

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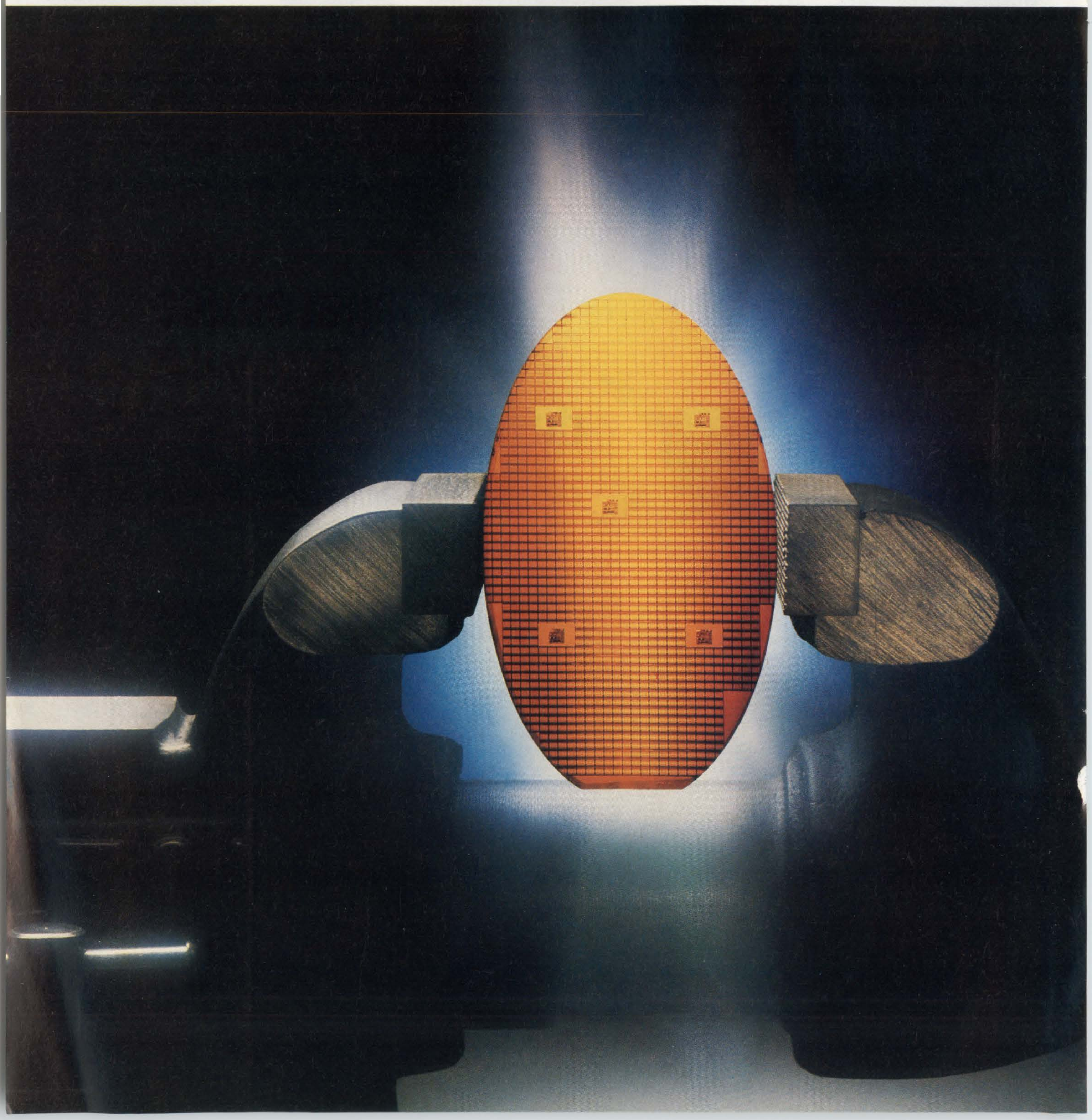
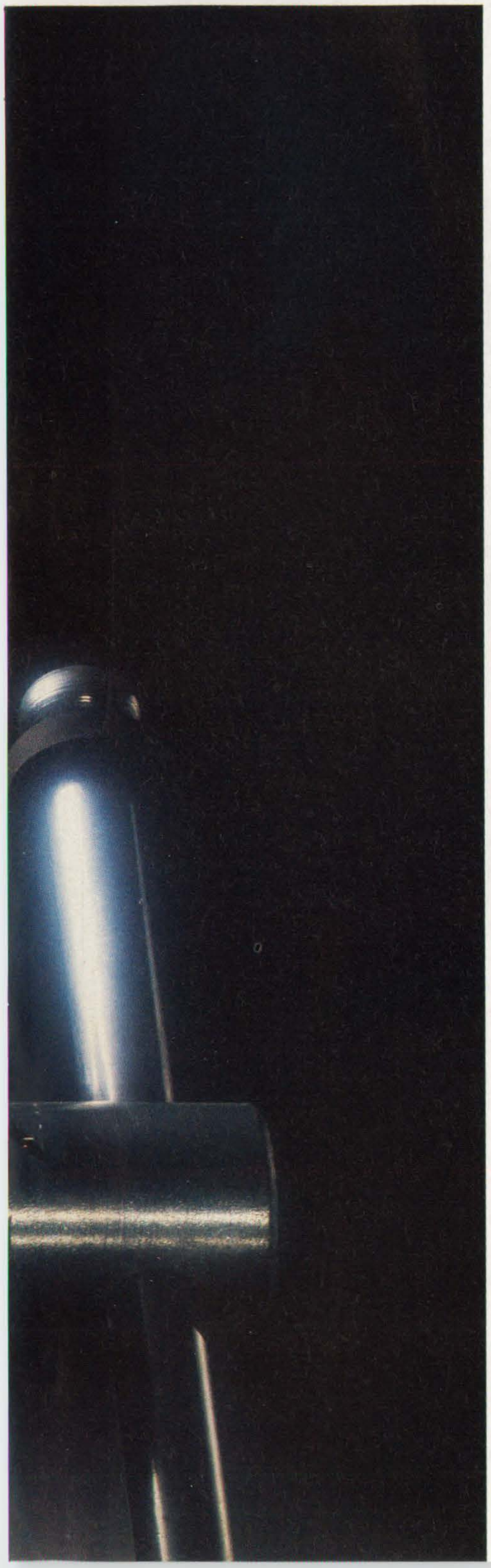


speed from our logic.
as 4.1 ns!



With our new Advanced BiCMOS interface logic (ABT) family, you get the speed, drive and low power you need to optimize the performance of processors operating at 33 MHz and above.

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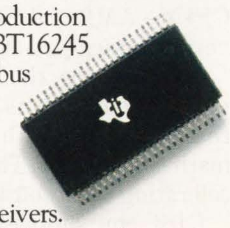
Our ABT family, a second-generation advance of our leadership BiCMOS (BCT) family, includes versions of our 16-, 18- and 20-bit-width Widebus™ functions.

Among the many ABT Widebus functions released is the 'ABT16244, a 16-bit buffer and line driver. It exhibits much greater stability of propagation delay *(see chart)*, which results in a lower derating factor across the number of outputs switched.

Also in volume production are the Widebus 'ABT16245 16-bit bidirectional bus transceiver and the 'ABT16543 and 'ABT16952 16-bit bidirectional registered bus transceivers.



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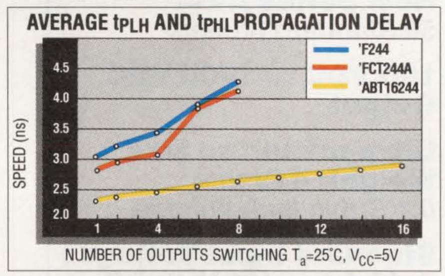

TI's speed advantage: *In a one-to-one comparison, a TI 'ABT16244 16-bit Advanced BiCMOS driver proves to be much faster and more stable than Advanced Bipolar and standard CMOS octal drivers.*

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TEXAS INSTRUMENTS

CPUs Offer A Cornucopia Of Options


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In the world of single-chip microcontrollers, designers have long been accustomed to the variety of off-the-shelf options offered by chip suppliers. That variety allows designers to better match the on-chip resources to the performance and cost requirements of the project at hand. With general-purpose microprocessors, however, the trend towards offering a range of chips is only a recent phenomenon. Traditionally, CISC CPU makers, such as Motorola and Intel, had only one version of any generation CPU, only offering speed grade and packaging options. Today, that scenario is radically different.

What has changed this scenario (besides the demands of customers to get lower-priced or more integrated solutions)? The answer is probably two-fold: The much improved chip design tools and the direct design of the CPU chip with proliferation in mind. By offering more powerful tools that allow designers to quickly remove sections, add in new features, and so on, it becomes a matter of months to create a spin-off version as opposed to a year or more. Activities at LSI Logic, which offers the Sparc and Mips CPUs, illustrate that best. They've already created many versions for vertical industries.

Both Motorola and Intel, as well as some of the RISC CPU suppliers, have considerably broadened their CPU offerings by creating versions "tuned" to various market segments. For instance, in addition to its full-featured 68030 and 68040 CPUs, Motorola created versions without the on-chip memory management for embedded-controller applications that don't require virtual-memory addressing. That helps to reduce chip test costs and eventually chip size, and gives designers a more cost-effective chip for that control application. And, for system performance requirements below those that require the horsepower of a 68030 or 40 CPU, Motorola created its 68300 family of high-integration CPUs. These combine the best features of the 68000 and 68020, as well as on-chip resources typically expected in single-chip microcontrollers.

Although that approach isn't brand new – Intel has offered its 80186 and 80C186 high-integration families for many years – the trend seems to be escalating. Intel has already, for example, released the 386SL, a higher-integration and much lower power version of the 80386 optimized for the limited-board-space portable computers. An artificial device dubbed the 486SX, an 80486DX CPU with the math coprocessor disabled, has also been released. The test time saved during chip production plus, perhaps, a slightly smaller profit margin on the chip allow it to be sold for significantly less than the full 486DX, thus giving system designers another price-point option. Intel's competitors for 80386 CPUs – AMD and Chips and Technologies – have also unveiled multiple CPU versions targeted at higher-performance and low-voltage operation.

Furthermore, this year alone, Intel expects to release over 30 proliferation products based on its 80386 and 80486 CPU cores. The first of those salvos has already been fired with a two-chip set that replaces the 80386 and companion 80387 math coprocessor. The chip set, called RapidCad, is targeted specifically at accelerating CAD software applications that rely on floating-point calculations.

RISC chip suppliers have also tried to broaden their family offerings to offer more design options. Several years ago, Fujitsu Microelectronics introduced the SparcLite, a Sparc-compatible CPU chip that includes both instruction and data caches on the chip. At about the same time, Integrated Device Technology released a similar chip for the Mips-compatible processor family. The same trends can also be seen in Mips Inc.'s most recent release – the R4000 family – has three CPU options that hit various performance and price points.

Creating application-optimized versions of CPUs will develop further as CPU cores become common members of design libraries and design-synthesis tools improve. The promise of system designers being able to "roll" a CPU tuned for their application is thus becoming more viable.

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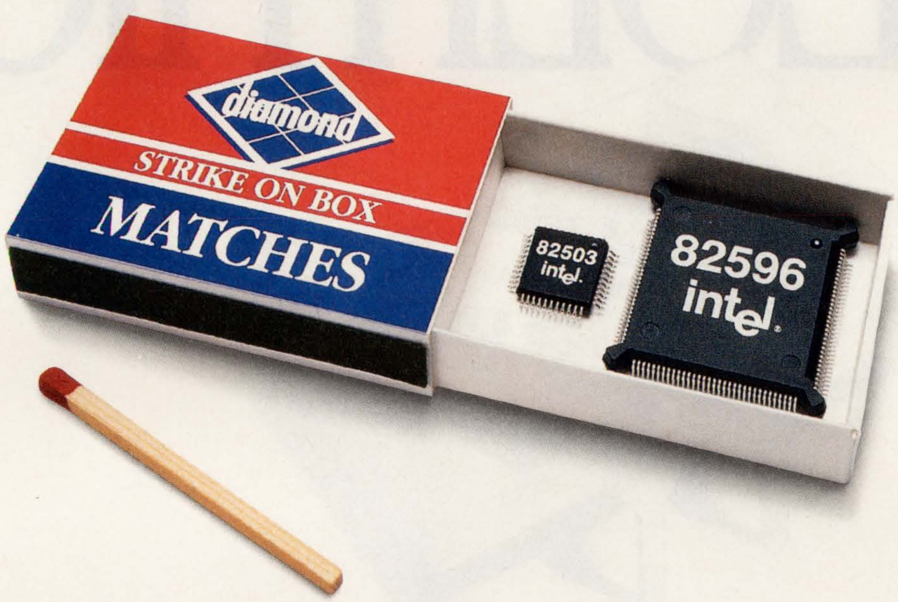

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Micromotor Is Made By X-Ray Lithography

By using micro-mechanical fabrication techniques, researchers at the Institute for Microstructure Technology of the Nuclear Research Center in Karlsruhe, Germany, developed a sample of a working electric stepping motor so small that its rotor measures less than 0.5 mm in diameter. With that, the institute has made its first step into microsystem-based drive technology. It considers the step a milestone on the, albeit long, road toward microrobots for applications in medical electronics and other fields. In making the motor, a fabrication process is used that combines X-ray lithography, and electro-forming and micro-molding techniques, allowing the low-cost manufacture of complex micro-parts that as of yet couldn't be made by mechanical means. The stepping motor's rotor has a 200-μm radius and rotates on a 116-μm radius axis. Surrounding the 100-μm-high nickel rotor are six stator segments that, from voltages on the order of 100 V, produce the alternating electric field needed to move the rotor. *JG*

Improved Compression IC Boosts Speeds 10X

A forthcoming single-chip data-compression/decompression processor expects to improve data-throughput speeds by up to ten times that of other silicon solutions. The LZ1 algorithm embedded in the chip was developed by Integrated Information Technology Inc., Santa Clara, Calif. It's based on a modified form of the popular Lempel-Ziv lossless data-compression algorithm. By integrating the token dictionary for the encryption/decryption process right on the chip, along with the compression/expansion logic, IIT squeezed adaptive lossless data-compression into one 84-lead plastic-leaded chip carrier. Thus, the function can be directly integrated onto a desktop or portable computer's motherboard. The CMOS chip can effectively more than double the storage space of any memory subsystem it sends compressed data to. And because it offers sustained and burst data-transfer rates of 5 and 8 Mbytes/s, respectively, it will operate transparently and have no negative impact on system performance. In fact, it could possibly improve system performance: Shorter file load times resulting from compressed long files could mean faster program startups. Samples of the chip are available immediately. A second version optimized for add-in boards is being developed. Contact Robert Seltzer at (408) 727-1885. *DB*

Spec Opens Up Range Of OS/2 2.0 Applications

By incorporating a SCSI interface for Direct Access Storage Devices (DASDs), a new specification opens the door for a wealth of microcomputer applications running OS/2 2.0. The 32-bit operating system, devised by IBM Corp., White Plains, N.Y., is expected to be released next month. The specification, from IBM and Adaptec Inc., Milpitas, Calif., gives PCs and workstations running OS/2 access to advanced I/O functionality, such as disk arrays and file servers. The operating system can now support Adaptec SCSI host adapters, and enables them to connect up to seven SCSI peripherals, such as scanners, printers, and disk, tape, and CD-ROM drives. Specific host-adapter models supported by the new specification will be announced when OS/2 2.0 becomes available. SCSI complements OS/2's high-speed, wide data path and multitasking capabilities. *RN*

Electroplating Process Made Safer

Conventional cyanide-based gold-plating solutions used in manufacturing microelectronic devices require special precautionary measures because poisonous cyanide is released if the solution becomes too acidic. Consequently, researchers at Sandia National Laboratories, Albuquerque, N.M., have developed a way to produce gold plating with a much safer gold-sulfite solution. Though this material has been limited to protective covering, Sandia found a way to use the solution to fabricate lines on substrates that are 2 and 4 μm thick, with 2-μm spacings. Miniature gold bridges were created to form crossovers on gallium-arsenide substrates. Tests show plating efficiency is close to 100%, and the plated gold's density approaches that of pure gold. A critical factor in the process is ensuring that the photoresist used to define the precision patterns doesn't degrade in the alkaline sulfite solution during electroplating. For more information, call Walter Worobey at (505) 845-8965, or Dennis Rieger at (505) 844-5554. *ML*

10-Gbit/12-mW Optical IC Includes Control

An optical IC that combines a 12-mW laser with a two-transistor (isolated-gate MISFETs) control circuit has been built at the Bagneux, Paris, France laboratories of the Centre National d'Etudes des Telecommunications (CNET). When packaged with passive components for electrical decoupling and a fiber for optical coupling, the module can directly modulate the laser at 10 Gbits/s for a modulation current of 40 and 50 mA. Both optical and electronic active devices are integrated onto a monolithic indium-phosphide substrate using a combination of epitaxial and implantation fabrication processes. The device, which typically uses 6 dB less power for direct modulation of the laser than similar-function modules made of discrete components, is said to outperform the modules. The laser itself is a buried-junction buried-ridge-structure (BRS) device that emits light at 1300 nm. Transistor transconductance of 80 mA/V/mm allows the laser's output power to be controlled by a gate voltage with an efficiency of 12 mW/V. Operating with a modulation current of around 1 mA produces an 8-GHz passband. *PF*

SOFTWARE MIMICS MOLECULE ACTION

A 30-second animation produced by software developed at Hitachi's Central Research Laboratory and Advanced Research Laboratory in Japan simulates the molecular dynamics of a silicon surface. The presentation shows how surface atoms rearrange themselves on the surface of one-half of a piece of bulk silicon after the other half has been cleaved away. In a real situation, these events occur in less than 2 ps. The simulation reveals that after the silicon is cleaved, a stable molecular pattern results when surface atoms bond into asymmetrical pairs called dimers. The animation has led to the discovery of sites at which dimers recess themselves out of view beneath the silicon surface. This phenomenon explains the images produced by scanning-tunnel microscopes. Hitachi's researchers expect the animation may produce further insights into the effects of individual surface atoms on device reliability, and eventually result in optimized, advanced fabrication processes. *ML*

MULTICHIP MODULES STAR IN CONFERENCE

Multichip modules (MCMs), which are gaining prominence in many new system designs, have been the subject of technical sessions at most major conferences for some time. Now, the International Society for Hybrid Microelectronics (ISHM), Reston, Va., is kicking off a conference dedicated solely to MCMs. The first International Conference on Multichip Modules runs from April 1 to 3 in Denver, Colo. Technical sessions will cover new developments in MCMs, the trade-offs involved in their design, module testing and reliability, dielectric issues, thermal analysis, and system considerations. For registration information, call ISHM at (800) 535-4746. *DM*

IC ENCODES STANDARD VIDEO, AUDIO SIGNALS

Decoder circuits that decode and process digitized or partly digitized TV signals, such as MAC (multiplexed analog components) signals, have been available for some time. These circuits reproduce coded programs in full quality on a TV screen or a loudspeaker. What hasn't been possible, though, is the direct digital—that is, loss-free—conversion of TV signals into an analog signal standard, like VHS used in video recording. Now, a new multistandard encoder IC from the ITT Semiconductors Group in Freiburg, Germany, not only closes this gap in TV-signal processing, but also offers high performance. The MSE3000 is a universal encoder placed between the digital color component signal stage and the analog composite-video or VHS signal stage. On the one hand, the MSE3000 codes difficult-to-handle standards, including MAC or Secam signals. On the other, the IC will handle such future standards as PAL-Plus, high-definition MAC (HD-MAC) and Japan's MUSE HDTV standard. Converting color component signals into an analog video signal of any standard is done by purely digital means and without loss of quality. The CMOS MSE3000, housed in a 44-pin PLCC package, is designed for the 13-to-26-MHz frequency range. *JG*

PCMCIA-COMPATIBLE MODEMS HIT EUROPE

At the Fall Comdex Trade Show held last October, Intel Corp., Folsom, Calif., announced its Modem 2400+ 2.4-kbaud modem card for use in North America and Japan. The card complies with the Personal Computer Memory Card International Association (PCMCIA) Release 2.0 specification. To fill out the family, Intel is now releasing similar PCMCIA-compliant cards that support the protocols used in the U.K., Germany, and Sweden. In addition to writing new software for each country, the cards' hardware needed altering to fit the connectors employed by those countries. Furthermore, Intel had to get the cards certified by each country. The company claims that the three newly supported countries, after Japan and those within North America, were in the highest demand by its customer base. *RN*

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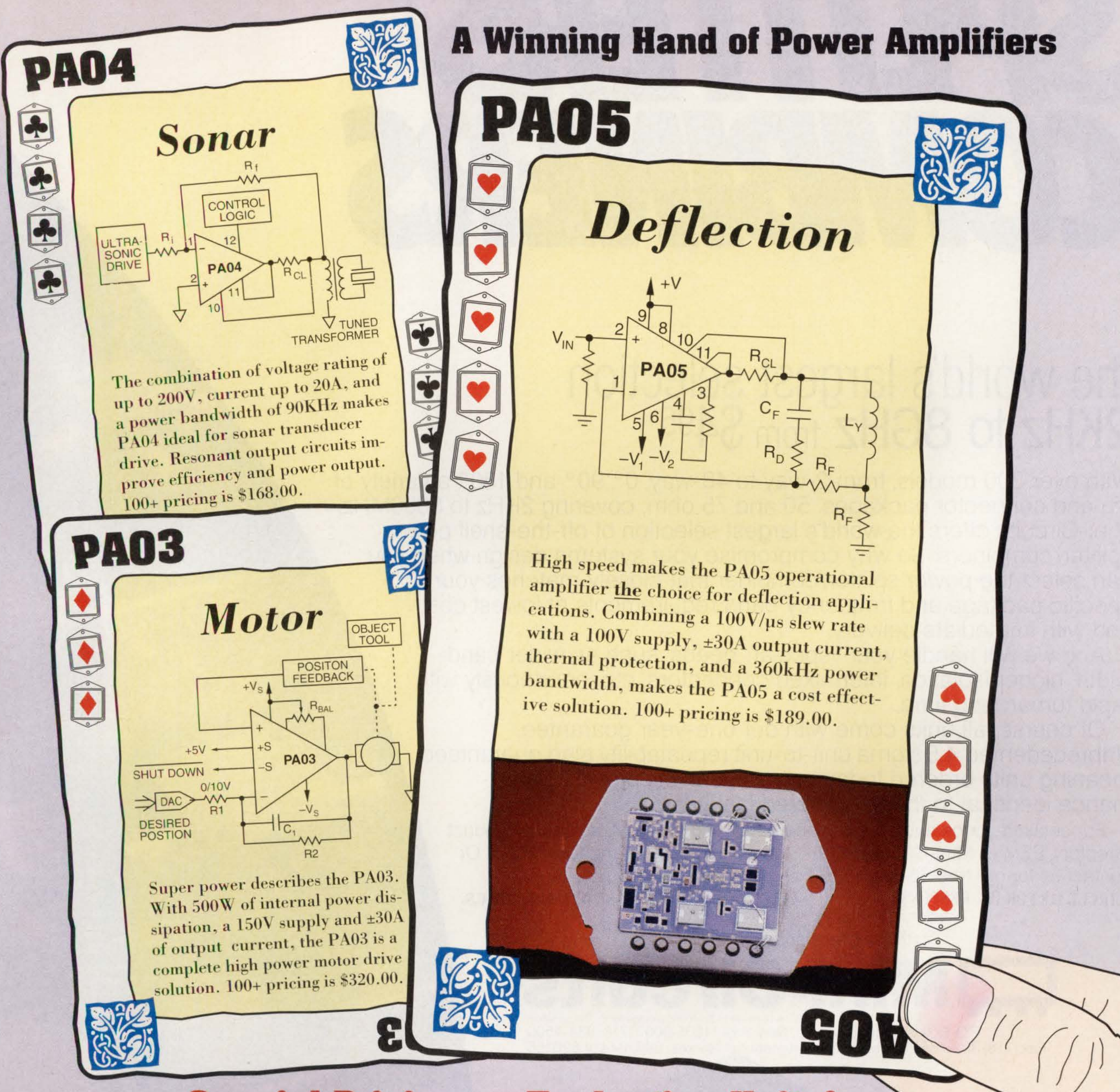

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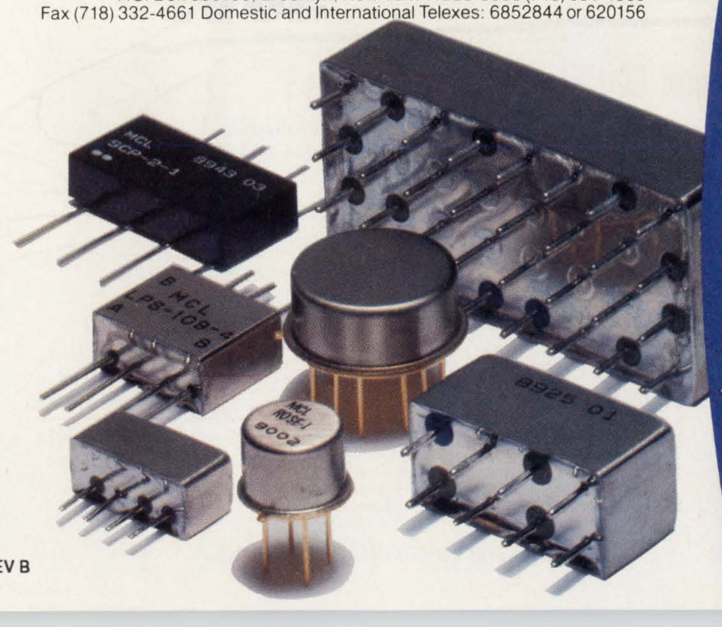

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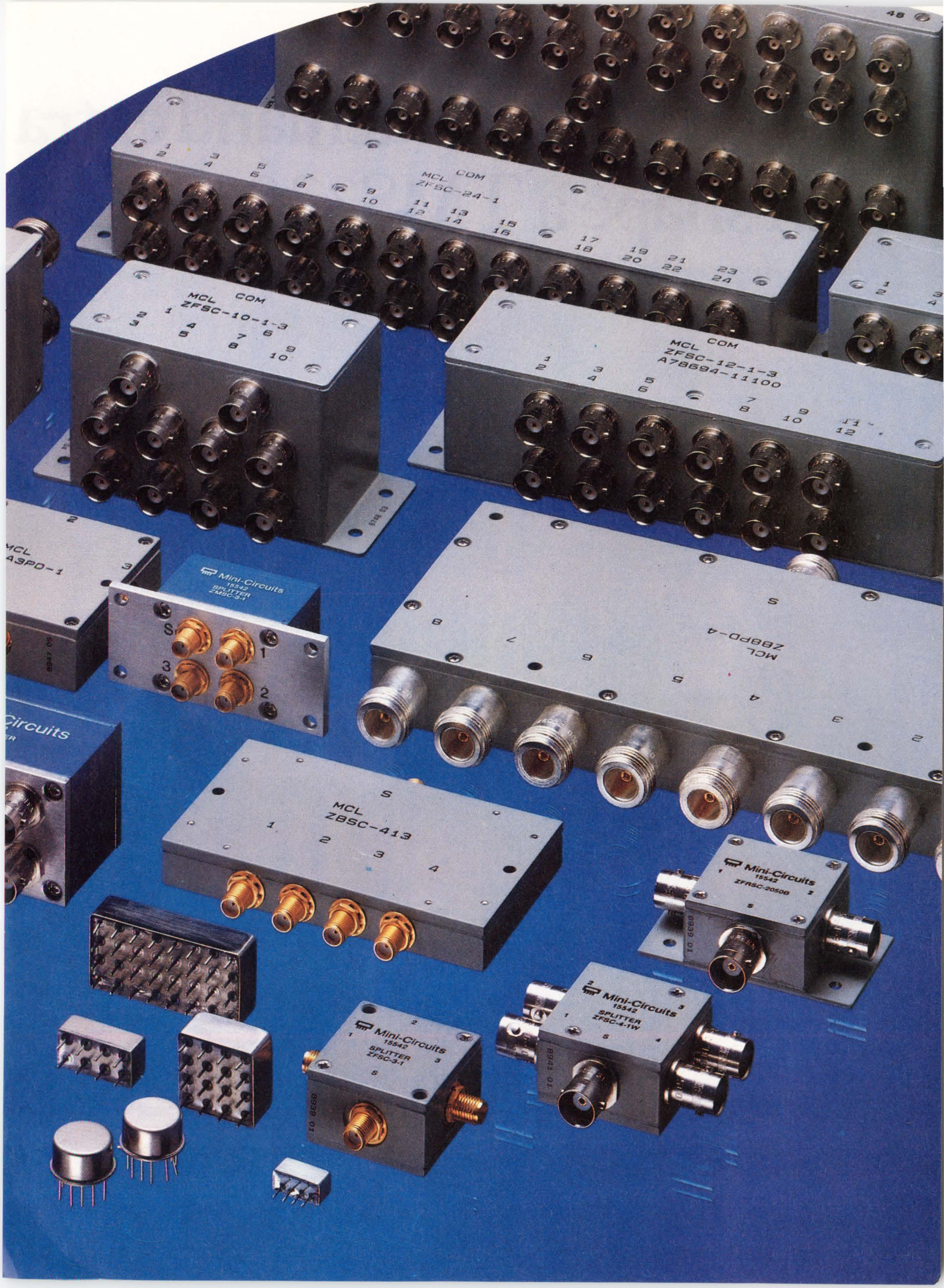
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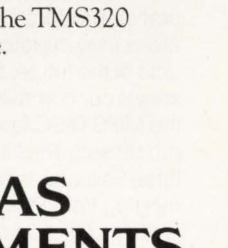

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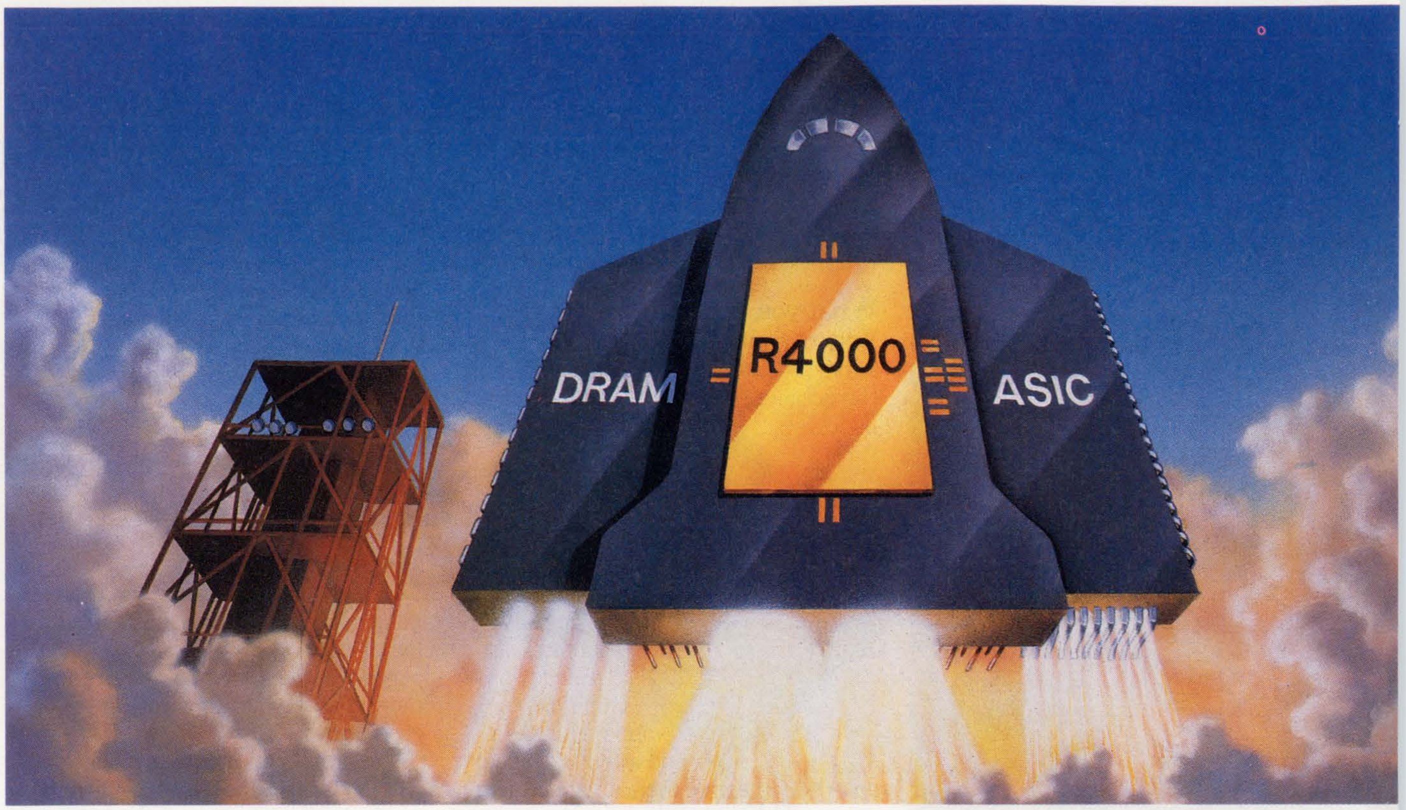

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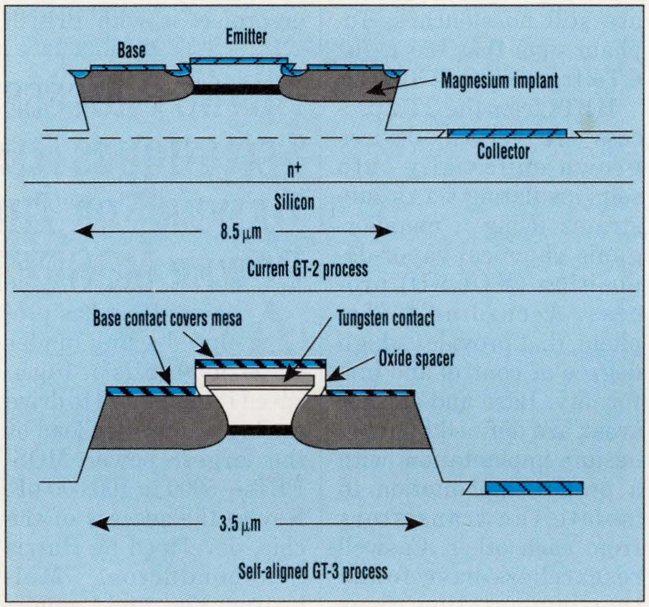
GaAs-on-GaAlAs Process Promises 118-GHz Mixed-Signal Bipolar Transistors

A gallium-arsenide-based transistor structure possessing a maximum cutoff or transition frequency (f_t) of more than 118 GHz is close to fruition. The research, done by the laboratories of GEC-Marconi Materials Technology Ltd., Caswell, England, is part of a quest for higher-frequency analog and faster digital logic devices for use in radio communications, fiber-optic transmission systems, and radar signal processing.



The devices are heterojunction bipolar transistors (HBTs) made by a submicron self-aligning fabrication process Marconi has dubbed GT-3. The company claims that this is one of the earliest attempts to apply such a process to a compound structure consisting of gallium arsenide on gallium aluminum arsenide.

More important than the 118-GHz f_t figure is that the HBTs are useful for both analog and digital circuits. Consequently, mixed-signal microwave ICs will be able to operate directly on millimeter-wavelength radio signals and simultaneously process data at clock speeds around 45 GHz.

Chief engineer Peter Topham says that the availability of this technology is crucial at a time when radio frequencies between 30 and 60 GHz are being considered for new communications services. "Mixed-function analog-digital circuits, such as we can make with these transistors, will save power and space in picocell cordless offices, in wideband communication links between buildings in city centers, or between geosynchronous satellites," he explains.

Though the GT-3 process is still in the final R&D phase, Topham is confident that he will get the results predicted by simulations. He explains that a wide variety of practical microwave ICs made with a less-dense version of the process known as GT-2 have proven both the process' validity and the ability to design a range of complex microwave ICs on it.

In a technical paper in the *GEC Journal of Research* (Vol. 2, No. 9, Feb. 1992, p. 74-80, published by The General Electric Co. plc), Topham describes various experimental devices that have been made at Caswell laboratories with HBTs from the earlier GT-2 process. These ICs range from simple wideband analog amplifiers and oscillators, to a 484-transistor uncommitted digital array, to high-speed analog-to-digital converters.

Topham cites the performance achieved in an analog-to-digital converter. "The bandwidth, the well-controlled threshold voltage, and the freedom from hysteresis achieved by the HBTs makes them natural choices for high-sample-rate flash ADCs," he says. One Caswell design provided an input bandwidth of 7.8 GHz, and a 6-bit sample rate of 7.5 Gsamples/s with 0.5-least-significant-bit error of 10.1 GHz at 4-bit resolution that drops to 2 GHz at 8-bit resolution. Power per comparator is 40 nW.

"We've fabricated a four-bit universal up/down counter for use in a frequency synthesizer using 380 transistors to give an operating frequency of 2.8 GHz." he adds, claiming it's twice the speed of the fastest existing counter. Such counters are used in digital frequency-synthesizer ICs for radio and radar systems.

GEC researchers have also fabricated both divide-by-four and divide-by-eight prescalers operating at frequencies up to 10 GHz to extend the range of frequency synthesizers. The next stage of development is to integrate these digital functions with analog circuits, such as the microwave oscillator.

One of the most complex designs is a 144-logic-gate semicustom array intended to speed development of microwave ASICs. Its internal cells are designed with differential logic throughout. That provides good immunity to crosstalk, while each internal cell can be programmed for two different power options using metal-programmable resistors. Bias generators are included on-chip for single-supply operation. The array supports eight differential high-speed I/O buffers with four additional single-ended ECL 100K-compatible inputs for lower-speed signals. The uncommitted array contains a total of 484 transistors in a die measuring 3.4 mm on a side.

To check out the maximum frequency performance of the array, it was used to make a divide-by-eight circuit that measures a circuit's maximum toggle rate. Divider operation was obtained for input frequencies up to 3.1 GHz. From the toggle frequency measured, an equivalent gate delay of 81 ps was calculated, making this the fastest HBT gate array to date. Total array power consumption is 1.5 W, with the divider circuit consuming around 300 mW.

To test the array's capabilities to its limits, Topham's team used it to make two other telecommunication ASICs—a 4:1 multiplexer and a 1:4 demultiplexer. These are essential components in fiber-optic terminal equipment to combine and later separate lower-speed data links prior to transmission on one fiber. The gate-array circuits can be used with a gain-block laser driver to perform all but the receiver function in a high-capacity fiber-optic link.

An HBT structure offers advantages of low noise performance and power efficiency. "The HBT has its best noise performance close to the carrier frequency, which makes it very suitable for amplifiers and oscillators," explains Topham.

Besides high-speed logic, Topham feels that a modified version of the GT-2 process can be used for microwave power transistors. "An output of 8 W at C-band can be obtained in pulsed operation," he claims. Such transistors can be used in the high-efficiency output stages in radar transmitters. Topham says that in the future, integrating power transistors along with microwave circuits will lead to a further range of applications in microwave transmission.

The main physical difference between the proven GT-2 process and developing GT-3 transistors is a matter of 5 μm. That's the difference in the width of the transistors' base-emitter mesas: For the GT-3 process, the mesa measures 3.5 μm across; in GT-2 devices, the mesa is 8.5-μm wide *(see the figure)*. That difference makes GT-2 devices slower, but there are still no slouches. Topham says that the f_t for GT-2 transistors is 40 GHz.

HBTs from the GT-2 process are vertical devices grown epitaxially onto semi-insulating GaAs substrates using a metal-organic chemical-vapor-deposition (MOCVD) process. According to Topham, that provides a high degree of control and uniformity. Base and emitter areas are defined by magnesium implantation, with a proton implantation to isolate the transistors from each other. Caswell researchers have found that implantation gives higher performance and better yield than processes based on etching.

After depositing the ohmic contacts, the circuits are interconnected by two levels of metallization separated by polyimide, which also protects the active devices. The GT-2 process features the inclusion of nichrome resistors that have low temperature coefficients.

Work on the GT-2 process started several years ago under a program sponsored by the U.K. Department of Trade and Industry, and in collaboration with the U.K. Defence Research Agency (DRA)—formerly known as the Royal Signals Research Establishment (RSRE). The process is about ready to make the transition from laboratory to industrial applications, and Topham says that two advanced projects are in hand. One involves Ferranti International plc, Manchester, U.K., and it aims at making high-performance, low-noise hybrid yttrium-iron-garnet (YIG) oscillators. The other project is with British Telecom, Martlesham Heath, Suffolk, U.K., to design 10-Gbit/s fiber-optic transmission systems.

PETER FLETCHER

Novel Process And Circuit Techniques Result In A Fast Driver For The Largest Power MOSFETs

A joint effort has produced a tiny (under 5000 mils^2), high-speed IC optimized to drive the high-capacitive load of the largest power MOSFETs—5000 to 100,000 pF. Key to the success of the chip, developed by Harris Semiconductor, Melbourne, Fla., and Lambda Electronics, Melville, N.Y., is a dielectrically isolated process and an innovative low/high-side drive circuit.

The IC, dubbed the HV400 by Harris, emerged from Lambda's need to inexpensively drive large MOSFETs, which represent even larger-capacitance loads when paralleled *(see the photograph)*. The MOSFETs are used in 150- to 3000-W switching-power supplies running at up to 300 kHz. Until this development, no such IC MOSFET driver could do the job.

Lambda's designers first got the idea for this new circuit by experimenting with an IC driver built with three transistors—two of which formed an SCR—and a few diodes and resistors. At about the same time, IC designers at Harris were investigating the design and application of a high-speed SCR IC structure/circuit, and presented their findings at the High Frequency Power Conversion Conference in 1989. Upon hearing this presentation, Lambda huddled with Harris to launch the project.

The output of the IC's circuit sources up to 6 A through the high-side npn transistor, while its active-turn-off SCR sinks up to 30 A *(see the diagram)*. When driving 20,000 pF, a 17-V pulse's rise and fall times are 70 and 30 ns, respectively. The device needs no floating power supply, yet drives both low/high-side FETs and requires just two external capacitors.

Its design uses a high-speed, dielectrically isolated process typically used for fast op amps, in which active and passive devices are isolated from every other device by a layer of silicon dioxide. Several other devices are also included, some not previously built on the process and others that were never built on any process.

An SCR is mandatory because of its high current density, meaning small chip size and low trigger current. Power MOSFET drivers are typically built on a more common junction-isolated (JI) process. However, in a JI device, every time the SCR fires, it floods the remaining circuitry with minority carriers, turning on circuits

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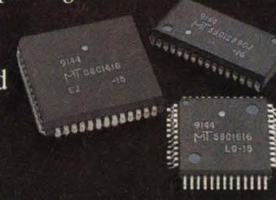

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16K x 16	MT58C1616**	13,15,17, 20,25ns	5,6,7,8,10ns	52-pin PLCC and PQFP
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128K x 9	MT58C1289	16,6,20ns	*	32-pin SOJ

* Output Enable is a synchronous signal on the 128K x 9
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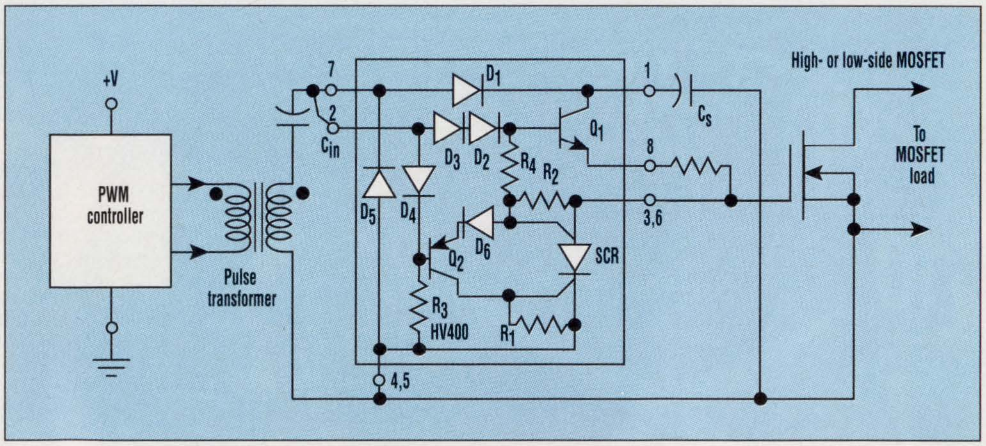
CIRCLE 113 FOR RESPONSE OUTSIDE THE U.S.



that were supposed to be off. Basically, SCRs can't be used in JI ICs.

While operating, the pulse-width-modulated (PWM) pulse train to the driver IC, as well the driver-IC's power, come through the pulse transformer *(see the diagram, again)*. The transformer is driven by a PWM controller offering a complementary output. Each end of the transformer primary is alternately connected to the controller's supply rail and to ground, generating a bidirectional signal in the transformer. When the transformer's output goes positive, transistor Q_1 turns on, pulling the MOSFET's gate high and turning it on. Capacitor C_s, which has been charged by previous pulses, provides the power to charge the FET's gate. C_s must be large enough to hold at least ten times the charge required to turn on the FET so that the FET's voltage change during a pulse is only a fraction of a volt.

After the FET's gate is brought high, charge is transferred from the transformer to C_s through diode D_1. The stored charge permits the FET driver to source currents much larger than the current rating of the PWM controller driving the transformer primary.

When the transformer's output polarity reverses, the turn-off SCR is triggered by transistor Q_2, which rapidly discharges the FET's gate capacitance. The SCR is designed to sink five times the current sourced by the turn-on npn transistor to ensure that turn-off time (fall time) is less than turn-on time (rise time). Diode D_5 clamps the input about 1 V below the FET's source and provides a path for transformer-core and C_{in} reset currents.

Because no initial charge exists on C_s during the first few pulses after power-up, the transformer charges the MOSFET gate capacitance and C_s at the same time. Since the circuit draws no quiescent current between pulses, no precharging circuit or bootstrap supply is required.

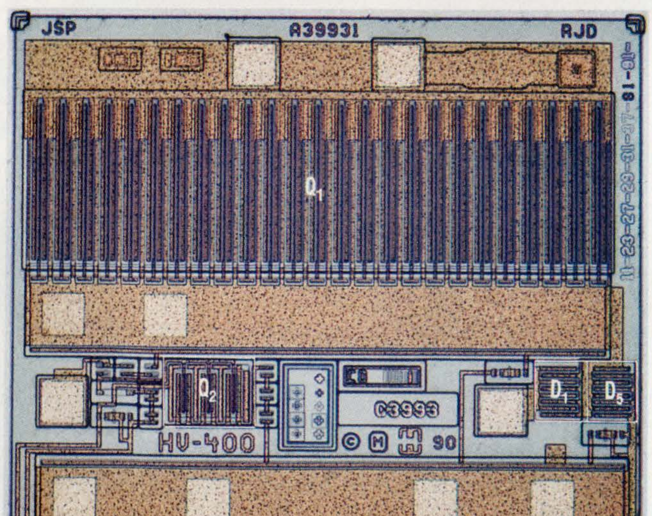
The SCR's high-current density results from storing large amounts of excess charge, which takes time to build up—and even longer to remove. A high-speed process like the Harris DI process (its vertical npn and pnp transistors have f_ts of 800 and 600 MHz, respectively) was chosen because it minimizes the time to handle this charge. However, to form the SCR, all of its terminals had to be brought to the die's surface, which required that part of it be built from slower lateral transistors. The IC's designers laid out the die so that a high-speed, high-gain vertical npn transistor was connected in parallel with each slower, lower-gain, lateral npn transistor. A similar approach was used with the pnps.

With that configuration, the trigger current first turns on the vertical devices that drive the lateral ones. The forward voltage at turn-on creates an electric field, which helps move excess charge into the SCR's interior. Consequently, the SCR turns on in just 10 ns.

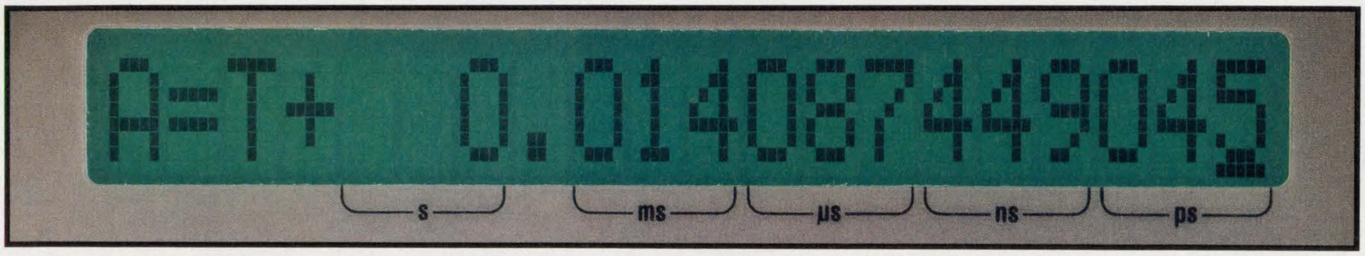
To cut turn-off time, the designers went to "active charge control," because no electric field was available for the job. They added lateral transistors that turned on in the presence of excess charge, cancelling the normal npn/pnp positive (latching) feedback loop. While this increases the SCR's on-state forward voltage drop, it cuts turn-off time. The SCR takes up just 300 mils^2 of the chip's 4800 mils^2 area, yet it can handle 10 A.

Although developed for internal use by Lambda, the HV400 is now available in an 8-pin DIP or SOIC. In quantities of 1000, pricing starts at just \$1.00 each. Call 1-800-4-HARRIS.

FRANK GOODENOUGH



Go ahead ... add 5 psec



Picoseconds are no problem for the DG535 Precision Pulse & Delay Generator.

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On the bench or in a test environment, the DG535 has the accuracy, stability, precision, and reliability you need to solve your tough timing problems - all at a price you can afford. Call SRS for more information on the DG535, even if you don't need picosecond resolution.

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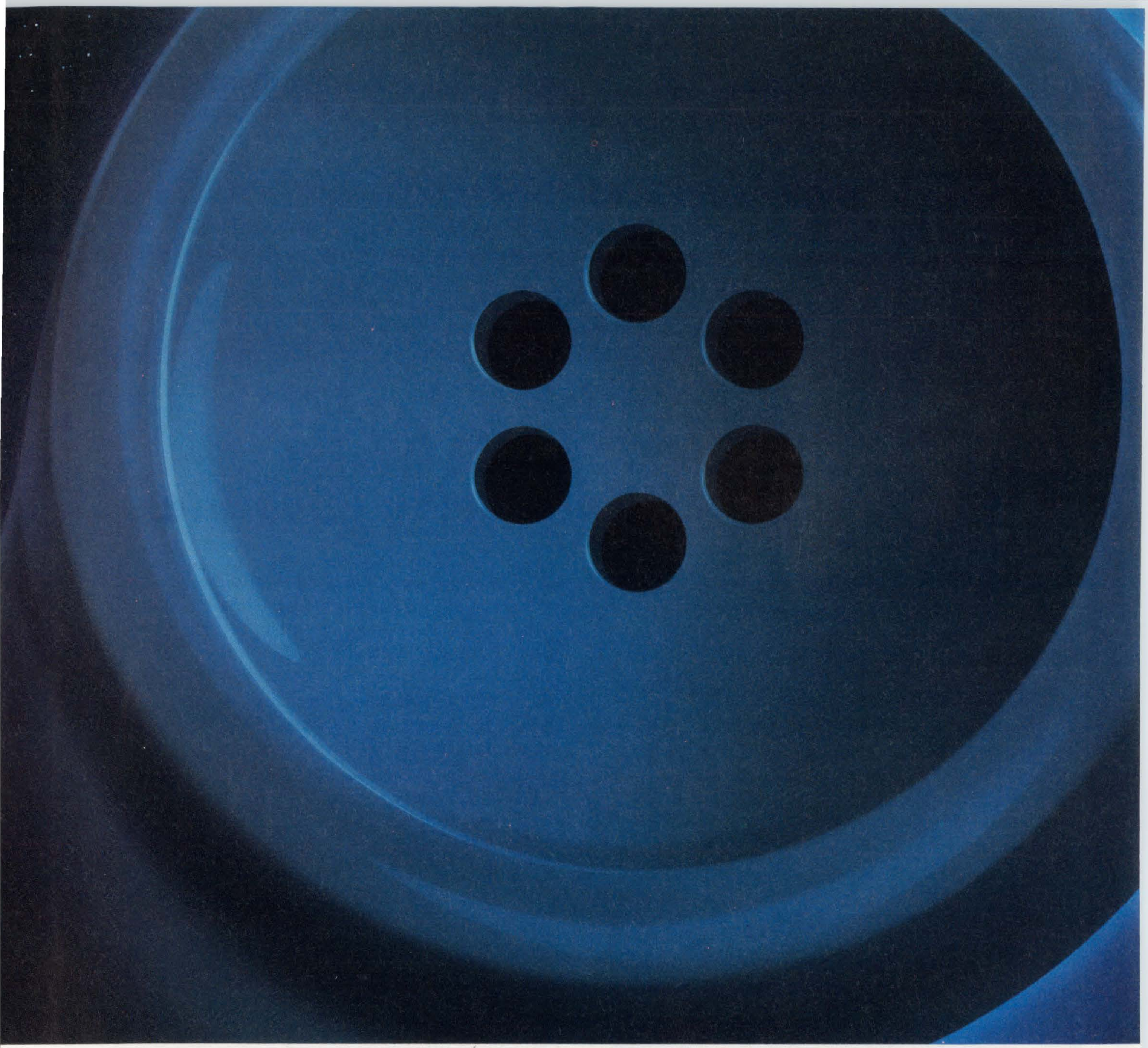
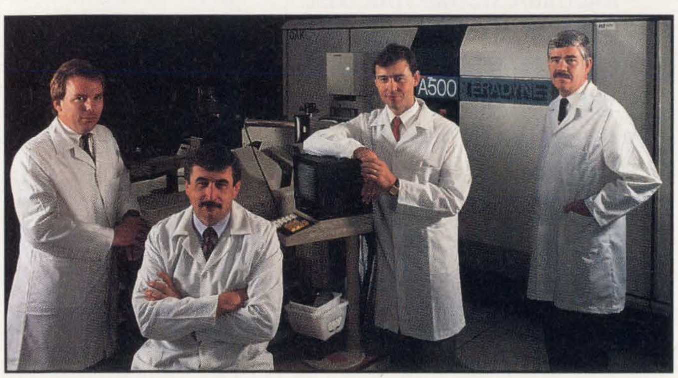


How Teradyne helps Northern Telecom



John Haydon, Ken Bradley, Gary Hobin, Terry Caves of Northern Telecom Electronics, Ottawa.

"To us, time is a strategic tool, a way of getting the edge it takes to gain a leadership role in world markets. With Teradyne testers, test development and manufacturing setup times are shorter, and actual test performance is far superior."

KEN BRADLEY, General Manager

Northern Telecom believes a quality message begins with a commitment: to deliver the highest performance products at the lowest cost – quickly and on time.

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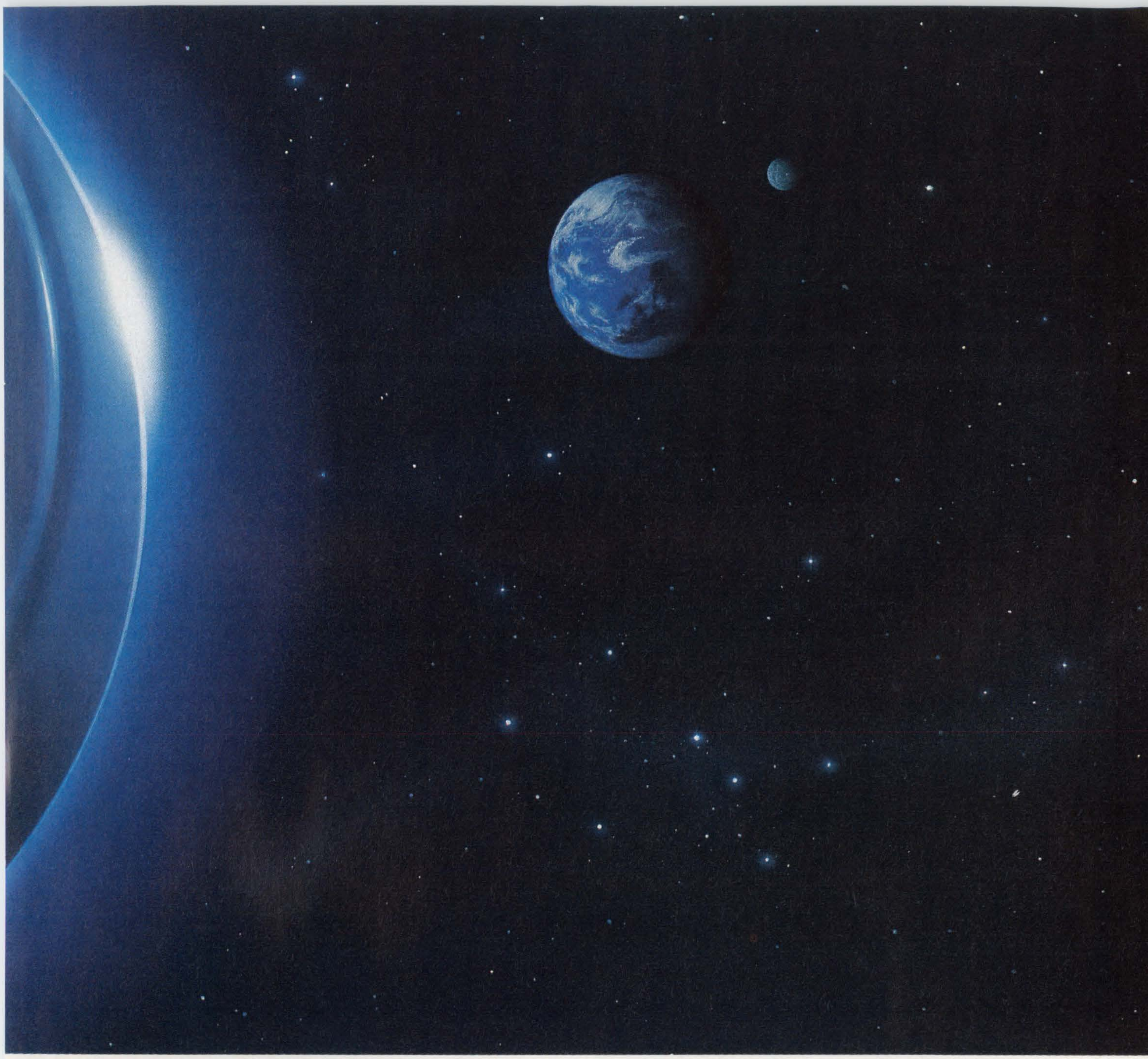
"Our Norstar key system is extremely silicon intensive. The A500 provided virtually unlimited test capability and reduced test time.



THERMAL IMAGING AIDS CHIP-COOLING RESEARCH

Thermal concerns in electronic packaging have reached the point where designers can no longer afford to treat them as an afterthought. With larger, faster, and hotter-running generations of ICs on the way, prudent packaging engineers are trying to anticipate these devices instead of waiting for them to arrive. At Digital Equipment Corp.'s Western Research Laboratory, Palo Alto, Calif., designers are turning to infrared thermal imaging and dummy chips to help them prepare for tomorrow's sizzling silicon.

According to John Fitch, a mechanical packaging engineer at the DEC lab, his job is to develop the tools and techniques needed to build the faster computers coming in the next three to five years. Those computers are expected to contain chips dissipating as much as 100 W. Fitch is working on cooling those chips to 85°C or less.

Several considerations must be heeded when developing the cooling systems for future computers. Size is one such parameter, but more important is the amount of audible noise generated. To simulate the power distribution and heat generation required to conduct their tests, Fitch and his team use a silicon-film resistance heater chip surrounded by a plastic pin grid array. This enables them to test the performance of their designs long before the actual chips are available.

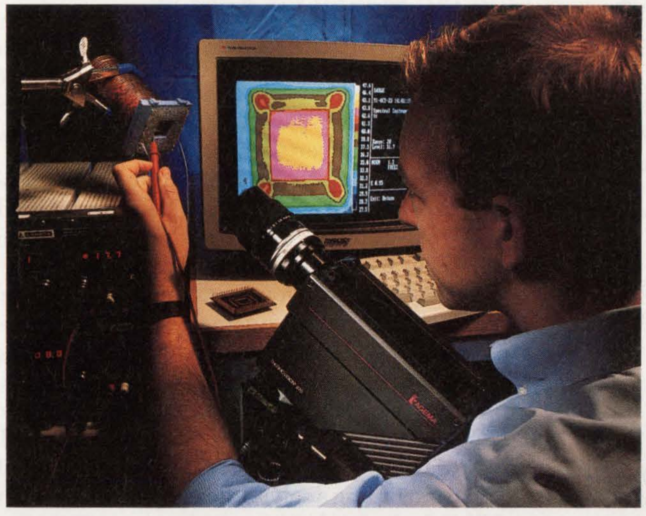
The lab's current work involves liquid cooling. Heat generated by the dummy chip is dumped onto a copper substrate at the heated end of a sealed, finned thermosiphon. The thermosiphon is actually a heat pipe about 5 in. long and 1-1/2 in. in diameter. The pipe contains a small amount of water or other coolant under vacuum.

The heated copper substrate boils the liquid within the tube. Quiet fans on either side of the tube pass air over its outside wall, which pulls heat away from the fins and condenses the rising vapor inside. The condensation trickles down the inside wall of the tube to be heated again.

To evaluate the performance of the thermosiphon and examine the effect of different liquids and pipe geometries and surfaces, Fitch is using a Thermovision 870 infrared imager supported by CATS-E, a software-analysis software package developed by Agema Infrared Systems, Ridgewood, N.J. *(see the figure)*.

Accurate temperature measurement is key to Fitch's work, because electronic circuitry is temperature-dependent. A deviation of ±5°C on any component on the chip can affect the chip's operating speed, performance, and overall integrity.

With the infrared imager, the engineers can look at things other than temperature. Temperature uniformity is important, and the CATS-E software displays the variation in temperature across the chip to within fractions of a degree. As a result, designers can consider factors that will result in a more nearly isothermal chip.



In addition, the camera reveals temperature anomalies within the heat pipe itself. Analyzing those kinds of problems often suggests changes in the tube's design or construction. The ideal situation is temperature uniformity along the entire length of the tube. A relative hot spot at the bottom of the pipe may indicate that the vapor inside is cooling before it reaches the top, which means that the pipe is longer than necessary. Conversely, a cool spot at the top may mean that gas somehow infiltrated the tube, trapping it at the top. As a result, the tube's performance would degrade, leading to eventual failure.

The infrared-imaging process can also evaluate the design and performance of heat sinks in existing DEC equipment, and has helped solve some problems related to heat dissipation and temperature non-uniformities. If the technique has a weakness, though, it's in studying materials with extremely low emissivities, such as gold. Gold's high reflectance makes it difficult to get a meaningful thermal image, and it's too expensive to spray black for test purposes. But Fitch points to the recent development of coatings and encapsulants with very high emissivity values as a possible solution.

DAVID MALINIAK

CAE Technology Report

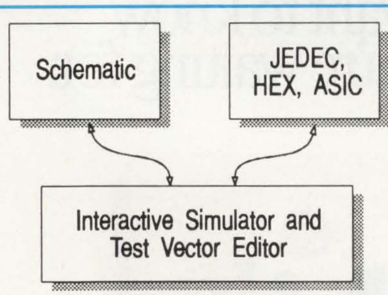
Who Will Survive the '90s

If you are one of those overly stressed individuals who are concerned over keeping up with new technologies and meeting increasing marketing demands, you can relax. The '90s are bringing you several new CAE technologies that will make your work much easier and effective:

- real-time CAE tools
- on-chip massively parallel computers
- virtual hardware and abstract designs

Real-Time CAE Tools

The first CAE tools were based on batch compilers which required lengthy and cumbersome compilations and made the designer a passive observer of the compilation results. The third generation of CAE tools that is being delivered right now is compilation-free. All data is loaded into prearranged tables and then manipulated in real time, much like moving parts from one bin to another. For example, the real time simulators allow you to directly interact with the design as if it were real hardware. You can instantly modify logic designs, replace devices, rotate switches, etc., without any compilations. What's more, you can go back to a previous simulation cycle, change design parameters and instantly compare the new design behavior with the old one. Since the real-time simulators produce instant responses, they are easy to work with and they turn out reliable designs at a fraction of typical development costs. A prime example of such simulator is SUSIE 6.0 ($1,995), which according to its producer ALDEC, saves over 80% of design work.
CIRCLE 240



The real-time interactive simulator allows you to make compilation-free design and test vector changes.

On-chip Massively Parallel Computers

ALDEC Co. has demonstrated that logic schematics and other design forms can be automatically converted into a microprocessor code. This code according to ALDEC can be broken into massively parallel, real-time operating environments. Since, the latest innovations in processor architecture allow for multiple logic-oriented computers on a single chip, it is expected that a new design technology based on this device will debut in 1993 and it will allow you to automatically convert any design idea into real hardware. This new design process will free you from timing analysis, design for testability, fault simulation and other tedious tasks that consume more than 60% to 80% of your time. **CIRCLE 244**

Virtual Hardware

The boundary between design and real hardware is not as apparent and distinctive as it may appear. For example, if you simulate a design on massively parallel computers, the simulation environment can reach the operational speed of the target hardware. At that point you may consider using the simulation environment as the ultimate hardware and the boundary between design and hardware disappears. Consider also these cases:

CASE 1. Hyduke's Test.

In February, 1986, Stanley Hyduke had connected two logic circuit breadboards with a PC via an 8051-based interface box. The first breadboard outputs were fed to a PC-based SLAV schematic capture/simulator inputs and the SLAV schematic outputs were then fed via the 8051 interface box as inputs into the second breadboard. Hyduke had demonstrated that a computer schematic/simulator could directly respond to the first breadboard and in turn control the behavior of the second board; any changes on the schematic directly and immediately affected the behavior of the second breadboard. Even more revealing was when he connected some circuit outputs from the second breadboard to the SLAV schematic capture (via the 8051-based box) and then connected the schematic outputs back to the second breadboard. The second breadboard operated as if the schematic drawn elements resided within its own hardware boundary. This operation analogous to open heart surgery has proven that there is less than a clear boundary between a design concept and its hardware implementation.

CASE 2. Hardware Modeling

When a design includes an IC model that is too complex, a real part can be used in its place for board-level design simulation. That mixing of real hardware with computer models is called hardware modeling and it takes down the boundaries between the real hardware and conceptual design. ALDEC has a product called LINK which allows you to feed into SUSIE simulator signals which have been captured from a live breadboard. This is still another example of blending real hardware with conceptual design.

CASE 3. Abstract Designs

SUSIE is a real-time simulator that allows you to analyze incomplete designs and designs with partially operational circuits. When you find a design problem you don't need to correct it immediately. Instead, you can enter at any test point in the design a timing waveform that represents the proper circuit operation. SUSIE treats such a waveform as generated by the circuit itself and produces instant verification of the design change. Since you can feed the timing waveforms at any hierarchical level, it means that you can make and verify changes at various design abstraction levels. **CIRCLE 242**

Free Help

Independent of whether you are a designer or a manager responsible for the R&D effort, you need to familiarize yourself with the new design technologies that quadruple your productivity with minimum investment. If you are currently buying new CAE tools, you need to select those tools that operate in real-time and offer at least some virtual hardware environments. A good starting point is the real-time SUSIE simulator. You can get a free sample by calling ALDEC. **The best time to look into the future is NOW!**

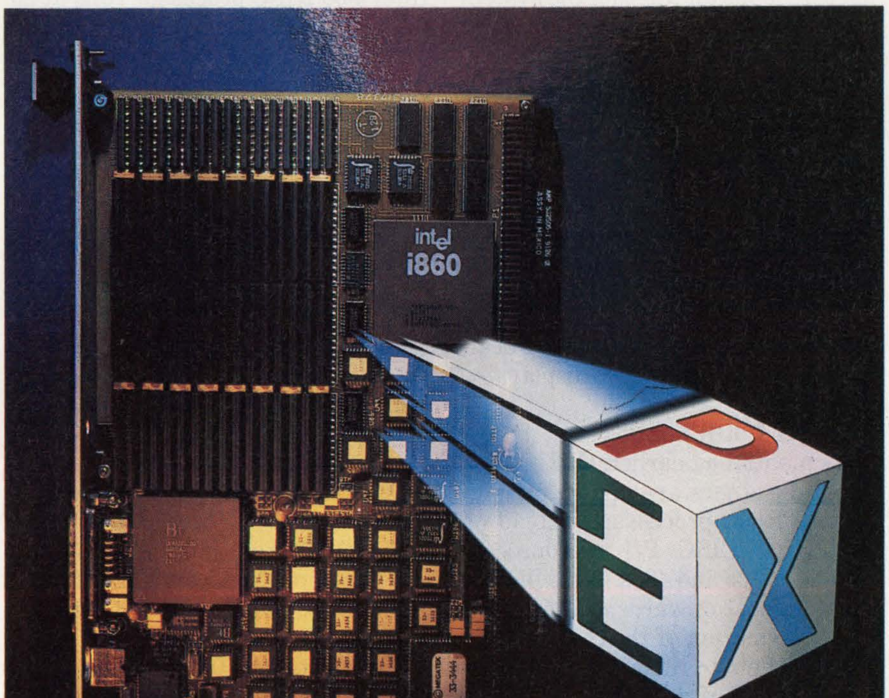
X-TERMINALS STRETCH PRICE-PERFORMANCE BOUNDARIES

DESIGNERS ARE FACING SUCH ISSUES AS HOW TO GET HIGHER INTEGRATION AND WHETHER TO USE RISC OR CISC WHILE KEEPING COSTS TO A MINIMUM.

RICHARD NASS

The explosion of X-terminals onto the computer scene has caused PCs and workstations to gradually disappear from engineers' desktops. X-terminals are also being added to existing networks. Why? Because of their downward spiral in price and enhanced performance, both of which can be attributed to two factors: the switch from CISC- to RISC-based systems and the integration of electronics using ASICs.

Generally, X-terminals are a derivative of network computing, in that the workload is split among many nodes. In some cases, an X-terminal can even support local clients. A graphical user interface on an X-terminal, as well as very high performance servers and the network hardware, can now be had at relatively low prices.



1. 2D AND 3D APPLICATION performance can be improved using an accelerator board, such as Megatek's X-Cellerator. The 6U VME board delivers 500,000 2D vectors/s and 200,000 3D rectangles/s.

"X-terminals aren't making a comeback, they're just getting understood," says Andy Nilssen, vice president of marketing at Visual Technologies, Westborough, Mass. "They're evolving quickly because the vendors now have a solid understanding of X-Windows hardware and software."

Software vendors know that they must support a wide range of hardware platforms to stay competitive in the market. But, if the applications are compatible with X-software, they'll run on any system that run X-software, including X-terminals, minicomputers, workstations, and PCs. The huge installed base of X-compatible software also offers an advantage to the hardware makers.

Most X-terminals began as CISC-based systems. Now, though, most X-terminal manufacturers have either switched to RISC processors or are investigating that possibility. "There's no future in any of the CISC technologies in terms of price-performance. The embedded RISC processors have a much lower price/MIPS ratio than any CISC technology available," claims Marco Thompson, president of Doctor Design Inc. (DDI), San Diego, Calif. DDI designs products that X-terminal OEMs integrate into board-level products. A complete kit (X-kit) available from DDI makes it possible for an X-terminal vendor to go into production. The kit includes such items as film for the boards and EPROMS for the software.

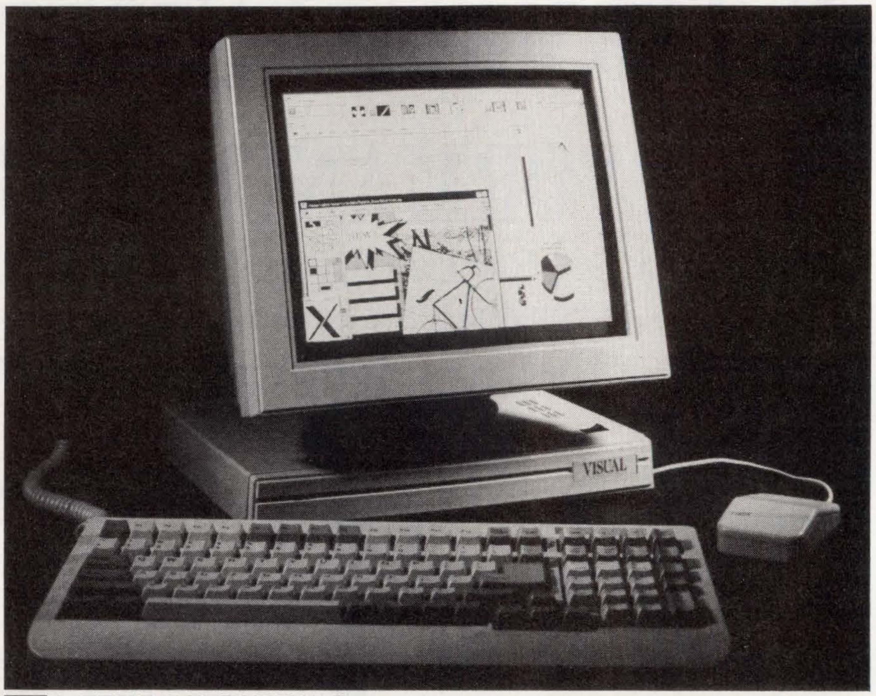
"In the embedded business, components are priced by cost, rather than by value. OEM designers are getting more bang for their buck (more MIPS/dollar) with embedded RISC than with Unix RISC," says Thompson.

An X-terminal basically consists of a processor, the main-memory system, the video-memory system (may be separate from or integrated with the main-memory system), the networking section (usually an off-the-shelf network chip plus the network drivers and receivers), and low-speed I/O (a mouse, keyboard, serial port, etc.).

In designing X-terminals, engineers must decide which communications-interface chip to use (Ethernet, FDDI, etc.), which microprocessor to implement, and whether to use a single processor or dual processors with a graphics-assist chip. Another important consideration is how much memory should be included (an X-terminal needs EPROM for booting up, EEPROM for configuration storage, and DRAM for data space and new-code downloads).

Design decisions must consider that X-Windows is an evolving technology. For example, users may want to download X-software to their local terminals through the network. A replacement version of X-software should also be downloadable into DRAM or flash EPROM because the X-standard is always changing (now up to X11, R5). Furthermore, manufacturers will continue to tune and improve their X-software code.

The type and size of memory to be used depends on whether the system implements color or monochrome displays. A monochrome display requires less DRAM than color. An ASIC designed by DDI lets a monochrome system run without video RAM (VRAM), which is significant because VRAM costs much more than DRAM. In this case, monochrome signals run directly out of the ASIC from the same memory system that holds the code and the data. Those signals are automatically sequenced to the video display.



2. TRUE X-TERMINALS are now priced under $1000. This $995 system developed by Visual Technology, dubbed the TX100M, comes with 2 Mbytes of memory, and a noninterlaced 14-in. display that sports a resolution of 1024 by 768 pixels.

Which Processor?

As mentioned earlier, OEM X-terminal designers are opting for embedded RISC processors instead of traditional CISC PC microprocessors like 386s and 486s. Though 386s and 486s cost upwards of $150 each, their domination of the DOS market enables them to remain at that price level instead of dropping to the embedded-RISC-processor level for equal performance. X-terminal designers can get 10 to 12 MIPS for under $40 using the Am29005 RISC processor developed by Advanced Micro Devices. For under $100, the 33-MHz Intel i960 RISC processor runs at 20 to 30 MIPS. Even a high-end RISC part, such as AMD's 40-MHz 29050, pumps out over 30 MIPS and comes with a floating-point engine, all for less than the cost of a 486 chip.

A high-end RISC-based system has been crafted by Hewlett-Packard Co., Cupertino, Calif. The company's 700/RX Model 14Ci offers a 14-in. color display and delivers more than 52,000 Xstones of performance. The small-footprint X-terminal can be used with HP's 9000 Series 800 family of PA-RISC-based systems and servers. Standard features include 1 Mbyte of video memory, 4 Mbytes of DRAM, and an Ethernet interface.

Most CISC solutions in the market are based on Motorola's 68000 processor. Both RISC and CISC processors are also being used with Texas Instruments' 34010 and 34020 graphics processors. Though the 34020 must run at a higher speed to keep pace with a RISC processor, primitives for line drawings and bit-block transfers (BitBLTs) are built-in. No extra hardware is needed to perform those functions. Half the code run by

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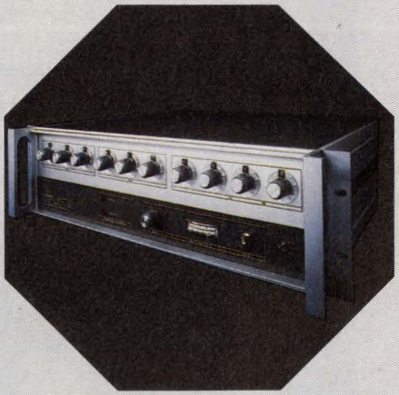

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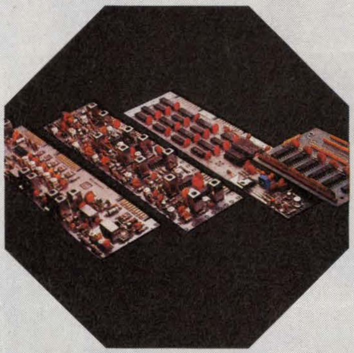

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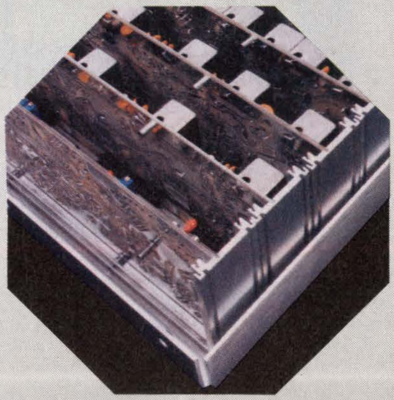

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D I G I T A L. T H E

the processor is general purpose, while the other half is graphics related. But in most cases, this solution isn't competitive on a price-performance level. This type of part stumbles when confronted with an X-terminal's general-purpose code. Using both a general-purpose part and a graphics processor may seem like a good idea, but it doesn't always work.

In the case of a CISC processor working with a graphics unit (like a 68030 working with a 34020), designers tend to perform all networking and overhead services on the 68030 and just do the graphics line drawing and the video management on the 34020. However, that approach mandates having two processors, two memory subsystems, two interfaces to memory, and an interface between the two CPU-memory subsystems.

The recurring cost for this type of design is at least 50% higher per X-terminal because dual parts are needed. There's also an overhead problem: The X-protocol is transmitted over the network in short bursts. When a packet is sent, the protocol must be stripped away. Then the X-terminal must decipher what the host computer wants drawn on the screen and display it. This process doesn't lend itself to pipelining or dual-processor solutions.

One way to circumvent this problem is to implement shared-memory resources. The second processor would interrupt the first one whenever the former needed to access the shared memory, and vice versa. In this case, the interrupted processor has to save its state in order to resume from the point where it left off. All of the synchronization interlocks and overhead related to that handoff could make the process slower than if one processor is used—by a factor of two or three in some cases.

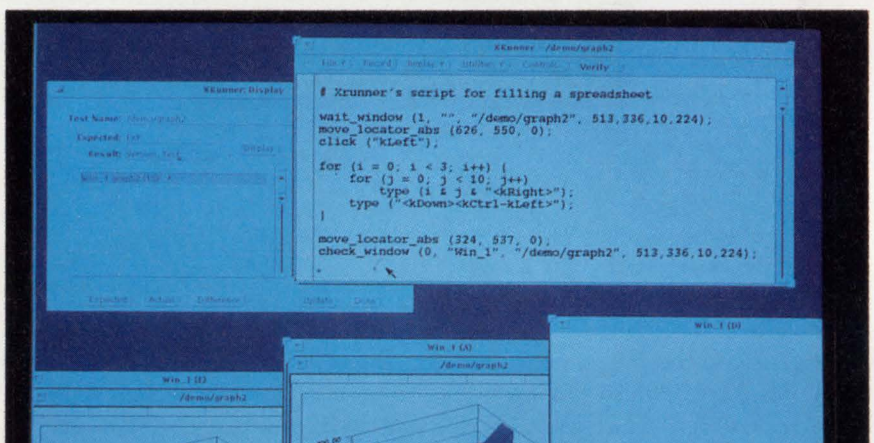
Another issue is the cost of the memory system that surrounds the processor. Some processors are better than others at utilizing low-cost DRAM without using an expensive cache solution. For example, Motorola's 88000 and Mips Computer Systems' R3000 RISC processors don't contain cache memories. The 3051 RISC unit from Integrated Device Technology puts some cache inside the processor, which is appropriate for certain applications. But running the X-code from cache doesn't offer any advantages when the processor starts running the networking half of the code. So, when choosing a processor, it's important to select one that supports cache-like throughput on both graphics tasks and in-line general-purpose processing tasks.

The X-server code occupies about 700 kbytes on a RISC-based platform, and about 600 kbytes on a CISC platform. The data spaces are the same on either type. A data space is the amount of occupied memory, not including the X-server or networking code. About 1 Mbyte of memory space is filled with X-Windows' required data spaces, which consists of the video section, the stacked caches and the other general stack space, the scratchpad space, and the network buffers. For this reason, an X-terminal should contain no less than 2 Mbytes of memory.

Industry experts say that by the end of 1992, every manufacturer will either have a RISC product or will be designing one. Some aspects of the X-software are easier or more effective to incorporate on RISC-based systems, because X-terminals require more MIPS power than CISC chips can supply. More MIPS can be obtained by using special-purpose X-oriented accelerator ASICs, which when combined with a host processor can enhance performance.

One accelerator that fits on a 6U VME board is the X-Cellerator 3DX/6U developed by Megatek Corp., San Diego, Calif. *(Fig. 1).* The board uses an Intel i860 processor to deliver 2D-graphics performance of 500,000 vectors/s. It also accelerates advanced 3D functions, such as Gouraud shading, fill-area extensions, Z buffering, and 3D transformations.

At the low end of the X-terminal spectrum, where manufacturers are trying to drive down prices, CISC processors may have staying power. "There's no question in my mind that RISC processors are going to dominate not only at the high end, but also at the mid range of X-terminals," says Judy Estrin, executive vice president of Network Computing Devices Inc. (NCD), Mountain View, Calif. "This is because the price-performance is just so good. They won't dominate at the very low end, where



3. TO TEST X-WINDOWS **application software, you can use the XRunner tool created by Mercury Interactive Corp., Santa Clara, Calif. XRunner can shorten the time needed to test software, thus automating the entire test cycle.**

every dollar counts." Because RISC processors have reduced-instruction sets, more instructions are needed for RISC processors, and hence, more memory. However, DDI does offer a RISC-based X-terminal that runs 75,000 Xstones for $995, including an Ethernet connection.

Don't Forget The Software

X-terminal designers must also carefully consider the X-code. It can roughly be divided into two parts—networking and graphics software. The networking core code shares many similarities with a Unix kernel. This code takes up about 300 to 400 kbytes in most processors—about 50% of the code space. In addition, a typical implementation runs networking code 50% of the time. It contains many long, nonrepeating loops and lots of multithreaded code, all written in C. The purpose of the networking code is to manage networking, event cues, and to support general processing inside the terminal.

The graphics-like code does line drawings, BitBLTs, and other graphics-type tasks. Here, the most important characteristic of the processor, be it RISC, CISC, or a graphics unit, is its memory bandwidth. The processor must keep up with the burst memory speed of the memory system. Hence, the interface between the processor and the memory system for the graphics code is critical.

When comparing a RISC processor to a graphics processor, both parts of the code must be considered—the graphics processing and the general-purpose processing. The graphics processor may have an advantage over the graphics portion of the code, but that advantage must be weighed against the disadvantage of processing the general-purpose code. And the overhead issues that arise when a graphics processor is combined the general-purpose processor add up to even more losses. "It can't be overstated that the X-protocol is much more than just line drawing and BitBLTing. It's a whole networking standard that requires high-performance computing," says Thompson.

Prices for X-terminal systems are rapidly starting to fall. Visual Technologies claims to have introduced the first "true X-terminal" for under $1000. A true X-terminal communicates over Ethernet and comes with a mouse, a keyboard, a display, and a controller board *(Fig. 2)*. To reach that price point, "we had to tap into the fact the our designers know how to take all the analog, digital, and power-supply circuitry and put it on one board," says Andy Nilssen. "Putting it on one 5-by-8-in. board cuts the cost and makes it easier to package." He adds, "We put pieces of power-supply circuitry right on the main logic board. Other manufacturers shy away from this simply because they don't know how to do it." The designs coming from DDI in the next few months will incorporate a single-chip power-supply controller. The $5 part needs only a few capacitors and an inductor to generate all of the power needed.

Total Integration

To cut costs, some manufacturers are placing all of the electronics inside the monitor housing. Flexibility is threatened, though, if components aren't separate. Keeping the components separate allows manufacturers to mix and match parts, although this is more prevalent at the high end. Separate components enable users to choose between the amount of memory, screen size, and resolution of their terminals, and upgrade at a later time. In addition, if a component fails, just that component needs to be sent out for repairs, not the entire unit. Moreover, separate components allows X-terminal vendors to use PC-type monitors, which are evolving at a rapid pace.

At the low end, if changes are made to a monitor's plastic housing and its internal power-supply requirements, putting the electronics inside the monitor offers a minimum delivered cost. With $100,000 of plastic tooling, a different monitor housing can be created for a vendor that controls its monitor casings. The video port is thus eliminated, instead becoming an internal connection.

When building a low-cost terminal, there's a fine line between what tasks should be implemented in hardware and what should be done in software. That decision ties into the strengths and weaknesses of the processor. A powerful processor permits some functions that were traditionally handled in hardware to be implemented in software without a performance penalty. In higher-performance color systems, where cost is a less-sensitive issue, these functions are typically implemented in hardware.

Today, users demand high vertical refresh rates, ranging from 60 to 75 Hz, and noninterlaced displays. These specifications create a solid, bright picture that reduces operator fatigue. The biggest cost factor is tied into the display's size and whether it's monochrome or color. At the high end, emerging applications like imaging and 3D graphics require high performance.

One way that vendors have achieved their price-performance goals is through the use of ASICs. This makes X-terminal systems simpler, less expensive, and more reliable. In its X-terminals, DDI takes the lowest-cost/MIPS processor (their choice is the Am29000) with the highest available memory bandwidth and builds an ASIC to tie the processor to the rest of the system. The processor-ASIC combination then does all of the graphics management. The processor, working through the ASIC to the memory system and Ethernet, performs the I/O without any external logic.

Over time, X-terminals could differentiate themselves based on their software capabilities or features. "Everything in X is software-oriented. The hardware is there to execute the X-protocol," says Peter Shaw, president of AGE Logic Inc., San Diego, Calif., a supplier of X-Window system software. The company currently supports both CISC and RISC, feeling that both have their place.

Most people associate X-software with the X-server, the part developed by the Massachusetts Institute of Technology (MIT), Cambridge. When a terminal manufacturer builds a system, the server is just part of the software that goes into the terminal. Other critical pieces are the network software and the interface between the server and the networking package.

Although the native software that comes from MIT could be used by an X-Windows system directly, it's not advised. A significant engineering effort is required to transform the public-domain tape that MIT sends out into a commercial product. This process includes adding quality, robustness, tuning, and features. It first gets optimized for a particular processor, then it's branched out for different types of hardware, such as different-resolution monitors or keyboards. "It's better to have slow hardware with optimized code than fast hardware with bug-loaded software," says Shaw.

AGE recently announced that its software is being ported to LSI Logic's LR33020 processor. The software, dubbed XoftWare M300L, is a customized version of AGE's XoftWare X-Windows system software. It was developed to supply OEMs using LSI's processor, including all of the software components needed to build a high-end X-terminal. The M300L package includes the X11, R5 server, as well as AGE's XoftNet networking, boot-ROM, and configuration menu software. The LR33020, based on 32-bit RISC technology, combines a Mips Computer Systems CPU with caches, a graphics coprocessor, and integrated system functions.

MIT is constantly revising the X-software, adding new features while refining others. For example, the change from R4 to R5 involved the font server. It gave users the ability to access the device. Other important aspects of R5 include its international keyboard support, and some code and algorithm refinement. From R3 to R4, the code was almost totally restructured, making the software more robust.

The first step in software development is to make a commercial product from what MIT produces, and then optimize it. However, getting the initial commercial product can become a sizable task. Beyond that, some companies would like to add their own specific features to the software, such as what AGE does. It licenses a version of the source code for a particular processor.

A product like XRunner, from Mercury Interactive Corp., Santa Clara, Calif., can be used for automated application testing of X-Windows software *(Fig. 3)*. XRunner generates programmable test scripts, automates test execution, and records test results. The software currently supports Sun SparcStations. DEC, HP, and IBM versions are expected shortly. A basic system starts at $35,000.

Typically, X-terminals boot up over the network, so remote boot software must reside in the terminal. In addition, all X-terminals contain the TCP/IP networking standard as a minimum. Moreover, some users want specific software to reside within their terminals. For instance, users ask for DECnet because of the large installed base of DEC VAXs.

X-software has built-in capabilities called extensions. Thus, the software can be broken down to a core server and some extensions that are primarily special-purpose features. Two important extensions currently being discussed are an imaging extension called XIE (X Imaging Extension) and a 3D extension named PEX (PHIGS Extension to X). Future extensions will support video or voice (multimedia).

From an X-protocol standpoint, the software is independent of the hardware. But one area that does affect performance is the host machine's access to the network. Systems whose hardware and software have good access to the network through Ethernet will have better performance than one with a communications bottleneck. The only difference, albeit a significant one, between using Ethernet and communicating through serial cables is in the speed. Transmitting the X-code through a serial port isn't really practical because X is so graphics-intensive (it's a bit-mapped protocol), although it is being tried. A long-term solution is to come up with significant compression algorithms and architectures that permit X to run effectively over serial lines.

Future X-terminals will most likely see different levels of configurability. "There are plenty of people who want a low-end system but with a 19-in. screen, and plenty who want a high-end system but with a small screen," says Nilssen of Visual Technologies. Also, because true X-terminals can now be had for under $1000, the commercial world will cast a much keener eye toward them. Users are leaving DOS-based systems because they can't get enough graphics power. Thus, they turn to X-terminals. Reasonable Microsoft-Windows performance on PCs requires 386 or 486 processors running at high clock speeds. Today's workstations are trying to become cheap enough to compete with PCs while PCs are trying to become powerful enough to compete with workstations. X-terminals fits comfortably in the middle of these two.□

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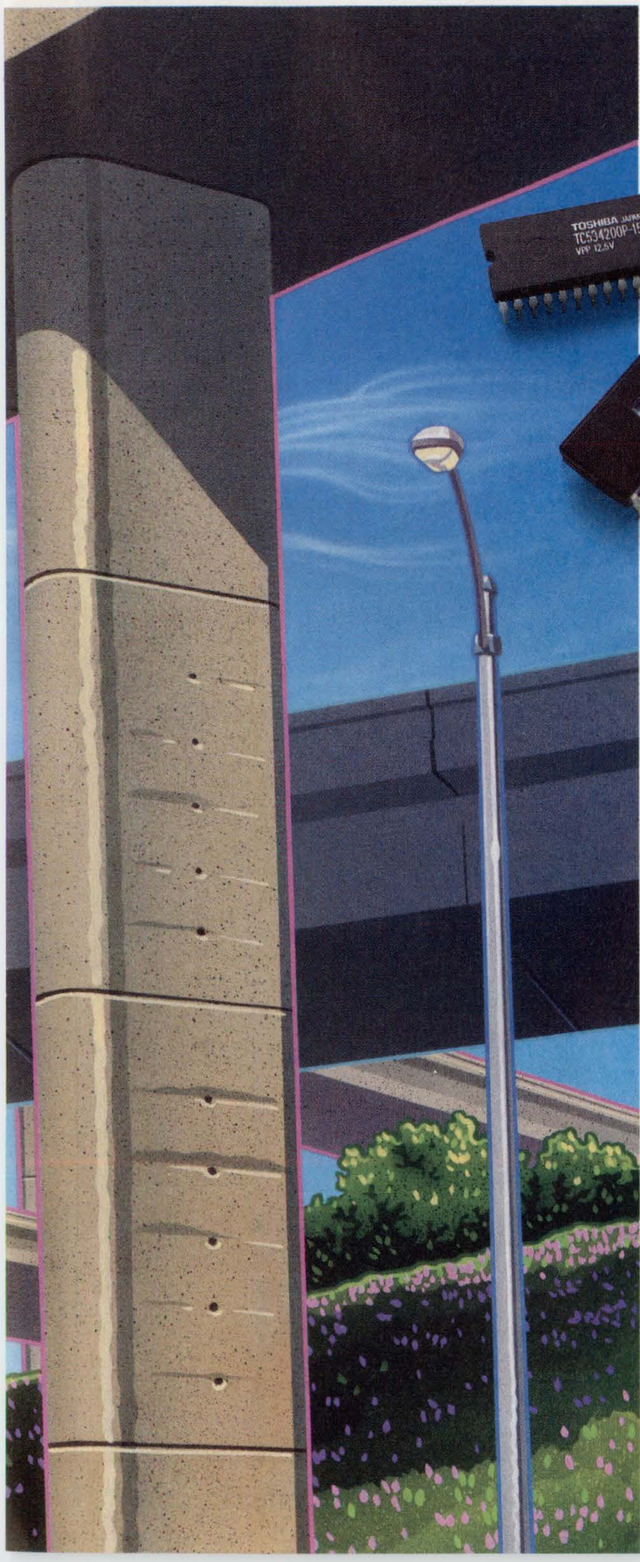

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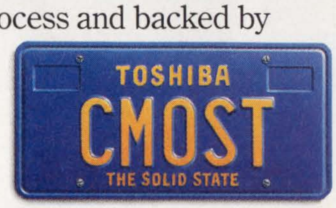

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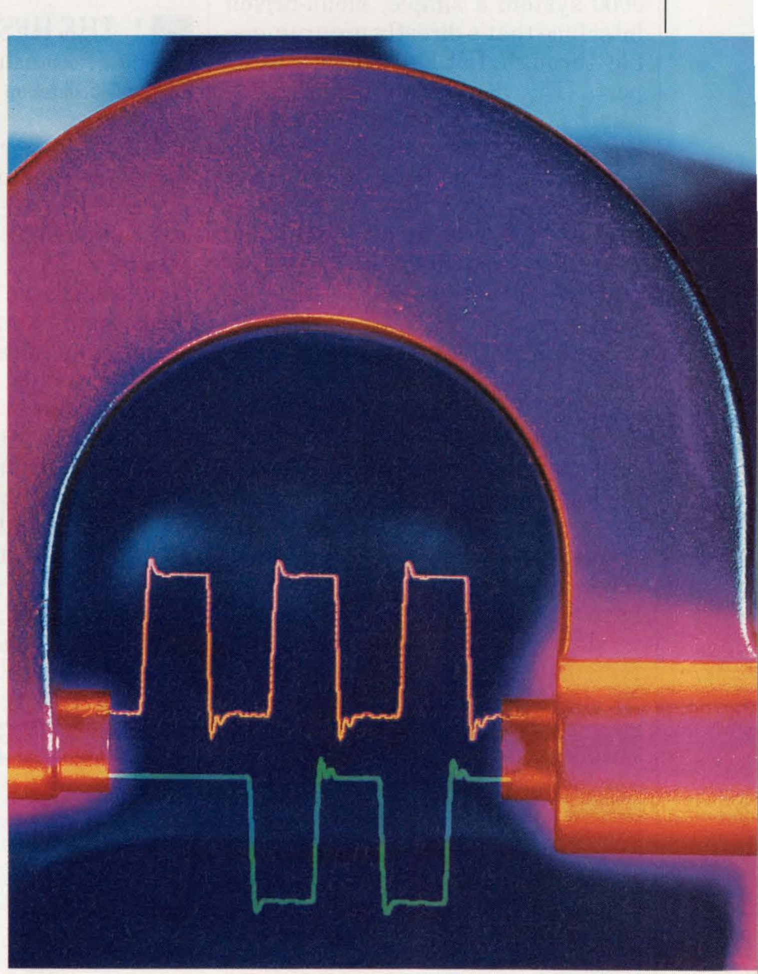
Data Time Generator Is The Complete Stimulus

John Novellino

When designs were simpler and development cycles were shorter, it didn't matter much that engineers had to design, assemble, and characterize a stimulus system before they could test the circuits they were developing. But the complexity of today's systems, combined with the pressure to get products out the door as fast as possible, make that procedure too expensive and too time-consuming for designers of high-performance digital circuits.

The solution to this problem would be to take every element of a stimulus system—pulse and data generators, a switch matrix, and programmable power supplies—and meld them into one easily programmed instrument. By using a proprietary digital architecture, Tektronix was able to accomplish this feat: The HFS 9000 Stimulus System combines the capabilities of a data generator, pulse generator, and switch matrix in one instrument. The resulting Data Time Generator is a modular system that offers the choice of full data or timing stimulus on each of 4 to 640 phase-locked channels *(Fig. 1)*.

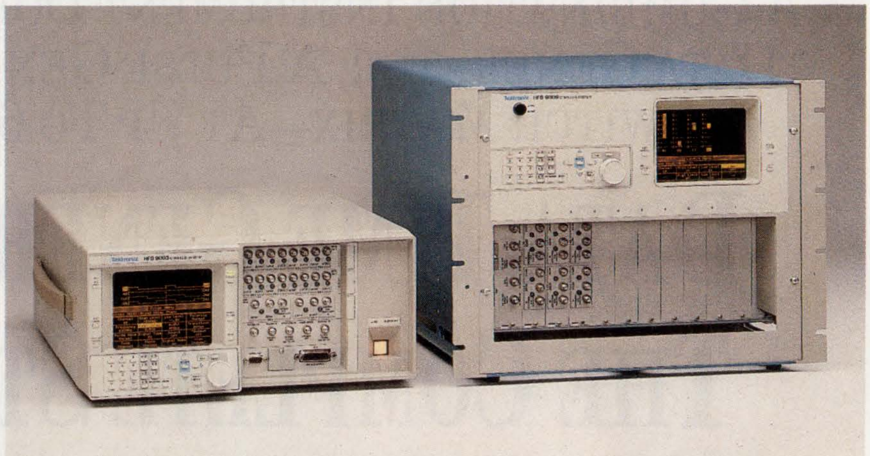
The Data Time Generator lets users specify data or timing simultaneously on every pin, with very flexible formatting. Engineers can even create tests not previously possible because the instrument can place a signal edge wherever it's needed, including moving rising and falling edges between cycles. The unit generates signals, such as data buses, clocks, strobes, gated clocks, logic-level sources, and pseudorandom bits with a 64-kbit/channel memory depth, at rates up to 630 Mbits/s. Resolution is 5 ps and transition times of 200 ps are possible *(see the table)*.



Some stimulus setups also need a programmable power supply to hold circuit input pins to static logic levels. But the Data Time Generator can create any type of data or formatting on every pin, with all pins equally accurate and flexible so no refixturing or recalibration is necessary. Thus, the pins can even function as static logic-level sources, eliminating the need for programmable power supplies in many cases. Virtually no restrictions exist on the waveforms that the user can specify. The instrument allows complete control over rise and fall times, widths, and voltage levels on all data, which is more flexibility than most pulse generators provide. All channels can be time-aligned at the device under test in any mode.

All of this flexibility would not be very useful unless the Data Time Generator is easy to use. There are inherent advantages, of course, in having only one instrument to acquire, learn, set up, and program. In addition, Tektronix gave the HFS 9000 system a simple, menu-driven interface that's directly programmable through IEEE-488.2 or RS-232 ports *(Fig. 2)*. And because the system has guaranteed specifications, engineers need not characterize their test setups. Operators can set up and modify test procedures through the interface screen, then save the setups for later use. This capability should improve reliability and repeatability.

The HFS 9000 system hardware includes two mainframes, the HFS 9003 and HFS 9009, and two Data Time Generator modules. The former mainframe holds up to three modules, and the latter accommodates up to nine modules. The mainframes include a display, user interface, system controller, and time base. The two modules, which can be used in any combination, are the HFS 9DG1, a 630-Mbit/s unit with a fixed 200-ps rise time; and the HFS



1. THE HFS 9000'S MODULAR FORMAT lets designers choose between a three-slot mainframe that supplies up to 12 channels (left) and a nine-slot chassis that accomodates up to 36 channels.

9DG2, which permits a variable 800-ps to 6-ns transition time.

The 9DG1's 3-V maximum amplitude is well-suited for ECL and GaAs logic. For TTL, CMOS, or biCMOS applications, the 9DG2 delivers a 5.5-V maximum amplitude. Both are 4-channel modules, so a one-box system can supply 36 channels. Users can also phase-lock mainframes together to create a virtually unlimited number of channels.

To order a system, an engineer specifies a mainframe and the number and type of stimulus channels desired. Tektronix delivers the system fully configured, tested, and characterized. If their requirements change, owners can request a field upgrade from Tektronix Service.

The architecture responsible for this capability creates the ultimate flexibility in signal timing and formatting by eliminating the need for analog timing circuits. Instead, digital circuitry builds up each aspect of the stimulus waveform *(Fig. 3)*. For each channel, a pattern memory holds the record of the data to be applied at the output pin. For each cycle, this information is combined with timing and formatting information to produce two signals defining the leading and trailing waveform edges. Digital timing circuits then fine-tune the two signals to produce a high-precision, repeatable output. The system maintains a precise timing relationship between every channel because they all use the same master clock.

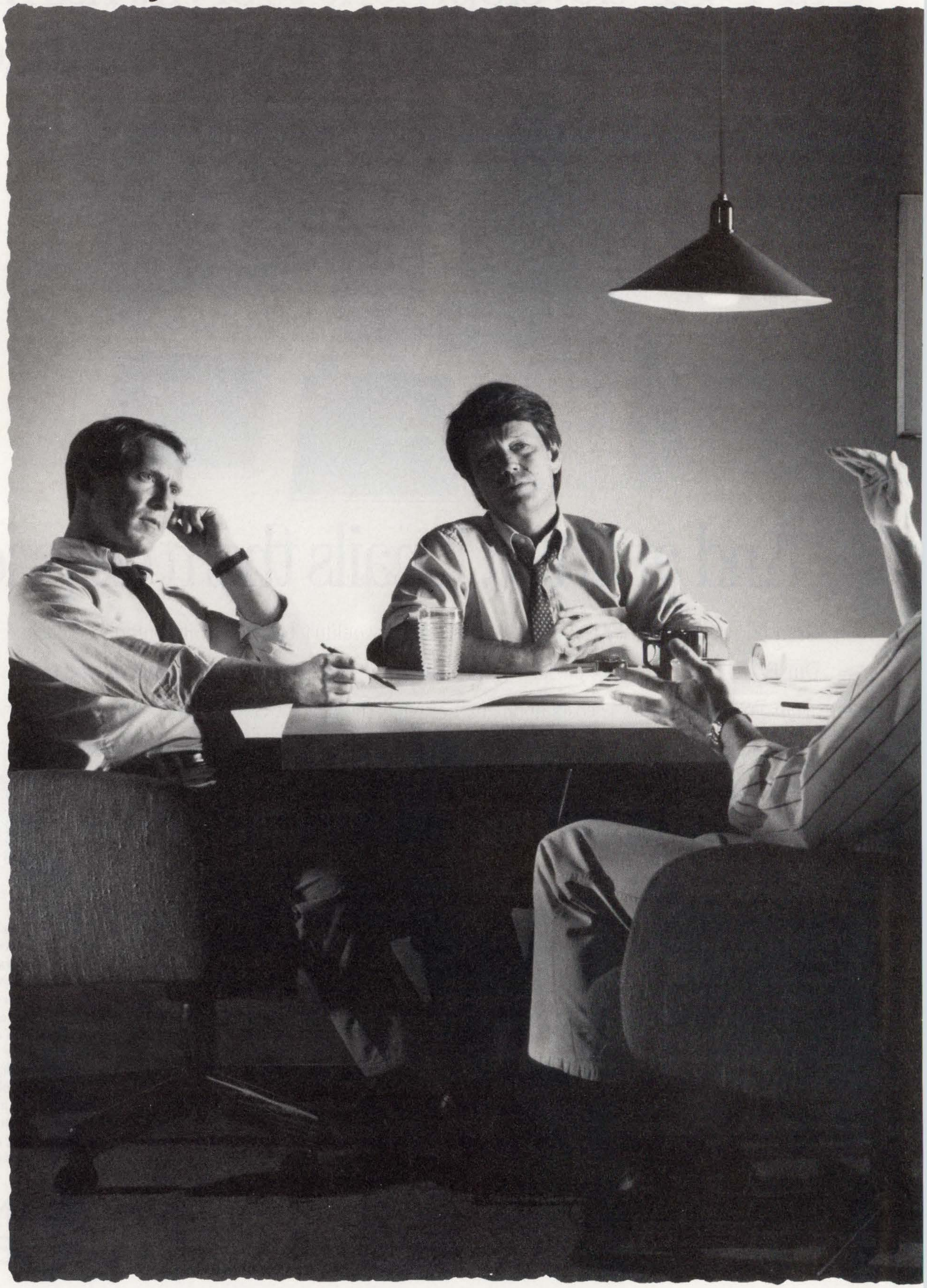
Tektronix believes the Data Time Generator's flexibility and ease of use will help it fill a role throughout the product development cycle, including design verification, characterization, and manufacturing test. More important, perhaps, is that by eliminating the cost and effort needed for an "engineered" stimulus setup, the HFS system will give designers more responsibility for the entire product development cycle.

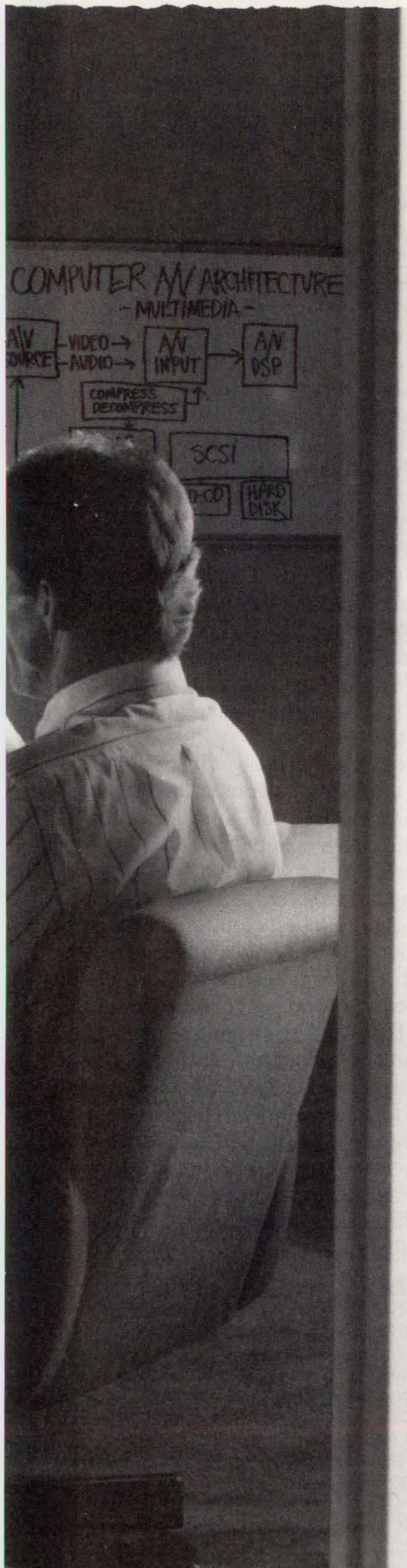
First, performance verification can begin at an earlier point in the cycle to optimize the design more quickly and effectively, saving an expensive turn of the silicon. And because the Data Time Generator is

HFS 9000 STIMULUS SYSTEM SPECIFICATIONS

	High-speed channels (HFS 9DG1)	Variable transition-time channels (HFS 9DG2)
Clock rate (RZ, R1, pulse mode)	50 kHz to 630 MHz	50 kHz to approx. 315 MHz
Output voltage (levels into 50 Ω)	+5 V max., –2 V min.	+5.5 V max., –2 V min.
Amplitude	10 mV to 3 V	10 mV to 5.5 V
NRZ data rate	50 kbits/s to 630 Mbits/s	
Vector depth	64 kbits per channel	
Channel de-skew range	–60 ns to > +2 μs, relative to time zero reference	
Delay and width adjustment	0 to 20 μs, each channel independent	
Resolution	better than 5 ps	
Accuracy	1% of width + 50 ps	
Jitter	15 ps ±0.05% of interval	

Sony Semiconductor

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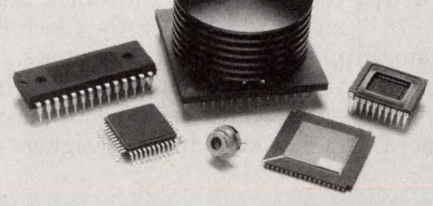
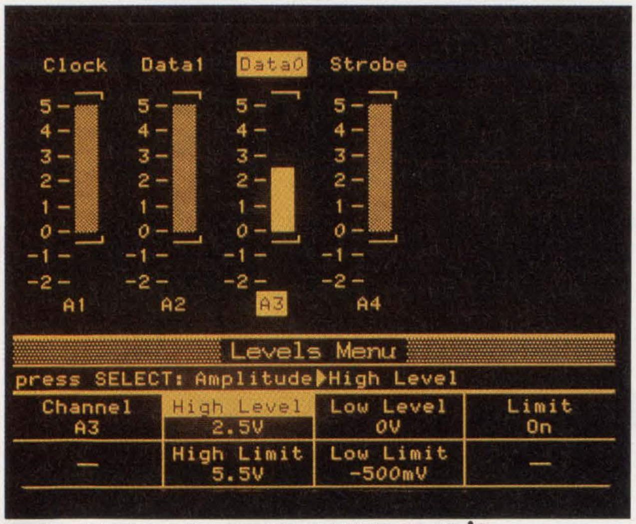




2. THE DATA TIME GENERATOR'S menu-driven interface is easy to use and is directly programmable through an IEEE-488.2 or RS-232 port.

suitable for use in characterization and manufacturing test, design engineers can get more involved with these later phases. The designers' detailed knowledge of their circuit and its specifications should help the evaluation and manufacturing engineers.

In the past, it was impractical for designers to thoroughly evaluate their circuits early on, because it was too difficult to create a worst-case stimulus at speed on a per-pin basis. Pulse generators could supply worst-case timing on a limited number of pins, but not coupled with the test vectors needed to exercise the circuit. Data and word generators could execute functional test vectors, but not while simulating worst-case timing inputs and usually not at speed.

With the Data Time Generator, however, engineers can take the vectors that validate the design in simulation, download them to the generator, and set up worst-case timing conditions to stimulate each IC as it comes back from fabrication. The result is a cost-effective way to characterize each device fully on the first turn of silicon, without waiting for every IC to be available.

The HFS system can also help engineers develop manufacturing test vectors early on without spending time on a much more expensive production tester. The generator can run the vectors to verify their correctness across all tester skew configurations. Users can adjust the timing of each stimulus pin to verify the absence of race conditions and timing traps in the vector set.

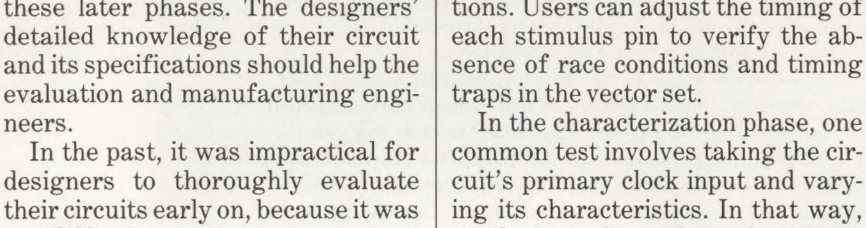
In the characterization phase, one common test involves taking the circuit's primary clock input and varying its characteristics. In that way, the designer determines what worst-case rise time, amplitude, pulse widths, and operating frequencies the circuit can withstand and still operate correctly. A typical data sheet requires many such parameters. Using a conventional two-channel pulse generator, the designer must make multiple tests. One channel supplies the clock and the other must be switched between the Clock Enable pin and the eight data inputs.

The Data Time Generator, however, provides each device pin with a dedicated channel. Designers can independently evaluate signal levels, pulse widths, and timing relationships. The clock pulse width can be accurately controlled independent of signal level. As a result, designers can derive the data sheet from one insertion test, which can also be performed on production devices using the same test equipment. In fact, the same procedure can apply during simulation, design verification, characterization, and the quality audit.

In high-performance circuits, pattern sensitivity becomes a major problem. This occurs when a device's performance is a function of the history of the inputs and outputs generated by the device. In gallium-arsenide components, for example, a history-dependent propagation delay is common. In more complex circuits, the delay from a given input may be a function of some internal state created by prior inputs.

To check a device's pattern sensitivity, a designer needs a low-jitter, precision timing and data stimulus system. This is where the Data Time Generator steps in. It not only creates the data stream, but also varies the signal levels, timing relationships between channels, and control-signal characteristics to create worst-case operating conditions.

The HFS 9000's job need not end at the manufacturing phase. Engineers can phase-lock the Data Time Generator to an external reference, such as a production tester. The generator will then supply the automatic test equipment fast, precise clock and data signals for high-throughput at-speed tests.☐



3. THE PROPRIETARY DIGITAL architecture of the HFS 9000 Stimulus System delivers more accuracy and flexibility than conventional analog techniques.

PRICE AND AVAILABILITY

The HFS 9003 three-slot mainframe and HFS 9009 nine-slot chassis cost $12,695 and $19,995 each, respectively. The 9DG1 fixed-rise-time card costs $11,000 each, and the 9DG2 variable-transition-time card costs $7900 each. All can be ordered immediately, with delivery in 8 to 12 weeks after receipt of an order.

Tektronix Inc., Test and Measurement Group, P.O. Box 1520, Pittsfield, MA; (800) 426-2200. **CIRCLE 511**

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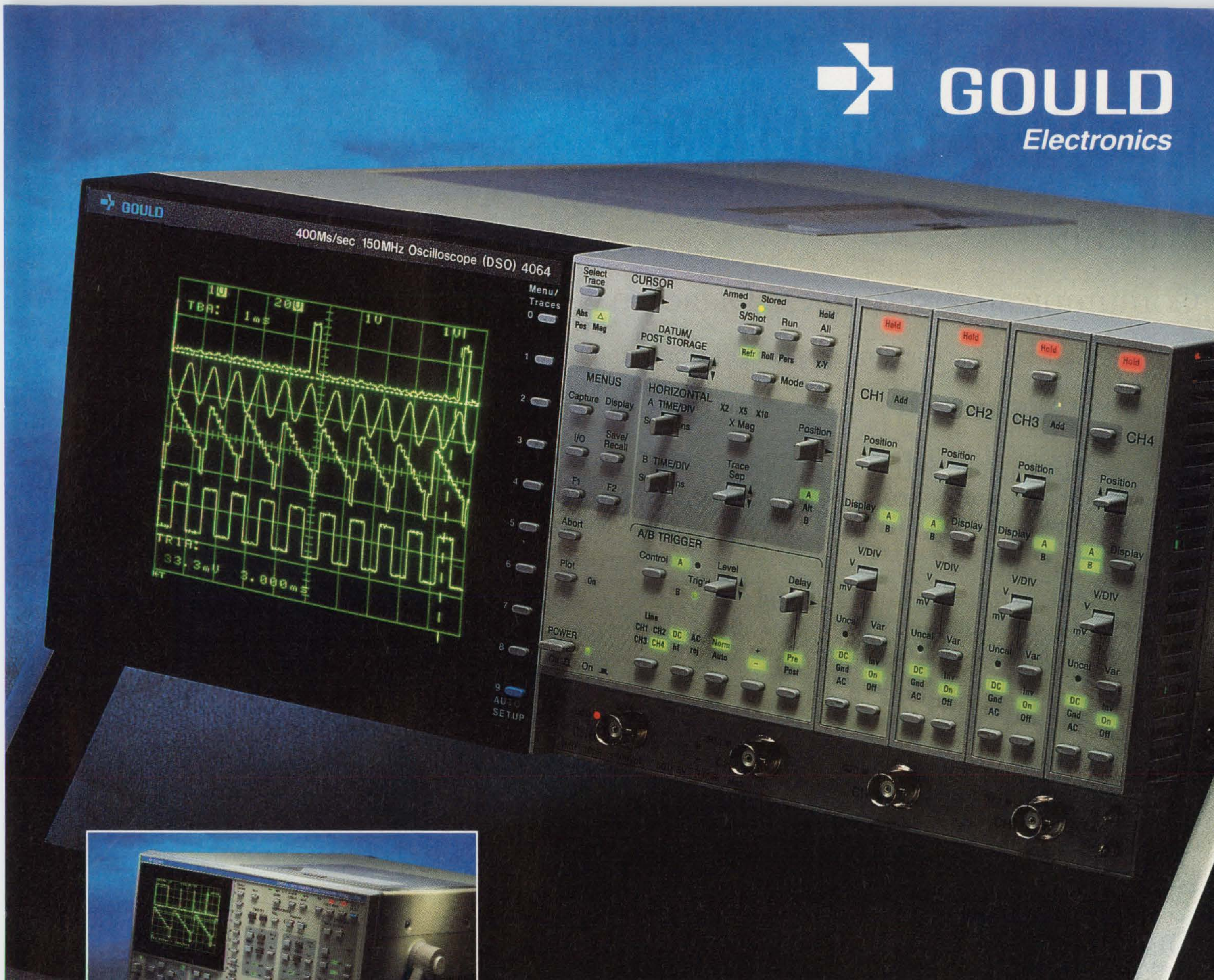
MODERATELY	528
SLIGHTLY	529



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COMING ATTRACTIONS:

March 19

Communications: Wireless Datacom Networks

There are currently three approaches to interconnecting computers and peripherals in a wireless network. In this Special Report on Wireless LANs, Communications Editor Milt Leonard covers the emerging standards involved, as well as applications, implementations, and the pros and cons of each approach.

Special Section: PIPS
(Power sources, Interconnections, Passive components, and Switches and relays)

Our March 19 PIPS coverage focuses on interconnections and includes a who's who of interconnection manufacturers and their products, giving this issue great shelf-life. Five major categories are covered: connectors and sockets, boards and panels, wire and cable, enclosures, and shielding. In addition to a technical article on interconnections, PIPS capsulizes power sources, passives, and switches and relays.

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April 2

Digital Semiconductors: High-Speed SRAMs

The Special Report in our April 2 issue will focus on wide-word high-speed memories for the latest generation of RISC and CISC microprocessors and DSP chips.

April 16

Analog Technology: D/A Converters

This Special report takes an in-depth look at high-resolution (14-bit and higher) converters. One of the report's main goals is to separate the digital-audio DACs from all other high-res DACs, and to examine the use of digital-audio DACs in more traditional applications.

PC Design Special Section

Electronic Design's PC Design Series was created specifically to serve the needs of our many readers developing PCs and peripherals. Everything from chip sets and single-chip solutions to CISC and RISC microprocessors, high-density memories, graphics, peripherals, add-on/add-in boards, buses, interfaces, input devices, and software are thoughtfully discussed from the systems designers' point of view.

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BASIC DESIGN TECHNIQUES CAN HELP ENGINEERS CREATE A TYPICAL IIR DIGITAL FILTER FROM AN ANALOG PROTOTYPE.

DIGITAL-FILTER SYNTHESIS SERVES DSP APPLICATIONS

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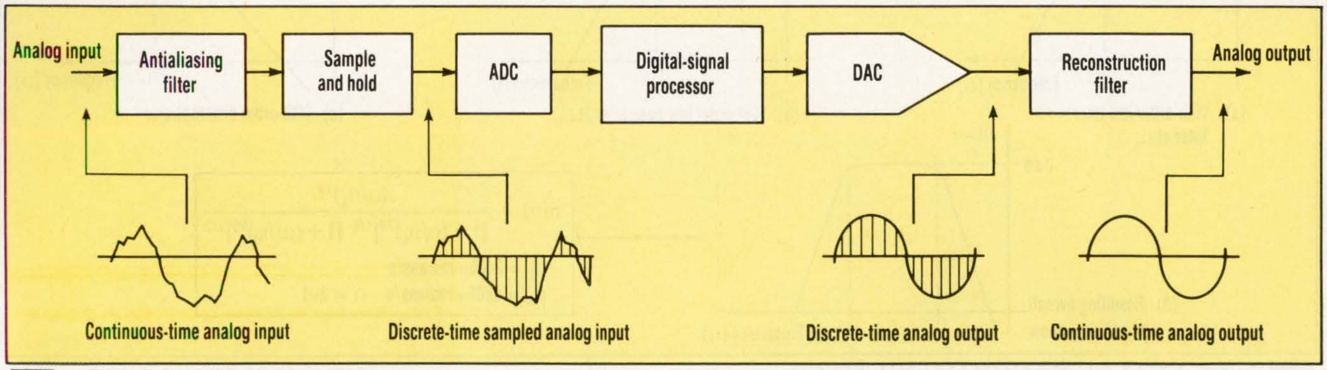
Digital filters hold a decided edge over their analog counterparts for a variety of reasons. First, digital filters can support the complexity needed to create sharper cut-off transition bands and superior pole-zero location accuracy. They can also perform finite-impulse-response (FIR) filtering. However, the decision to use an analog or digital filter often depends on many factors, including cost, filter complexity, drift, and circuit-board area. The engineer is the only one who can decide, based on the unique application at hand. When digital filters are implemented on a powerful digital-signal processor, other capabilities become possible. For example, engineers may use the processor to perform adaptive filtering or other application-unique algorithms that enhance overall system performance.

Following some basic filter-design techniques can help engineers successfully realize a typical infinite-impulse-response (IIR) digital filter from an analog prototype filter. For example, a general digital-signal-processing (DSP) channel architecture implements the digital IIR bandpass filter, and transformation from the analog s-plane to the sampled-data z-plane is performed using the bilinear transformation. In addition, for a successful filter, engineers must consider such factors as quantization errors and accumulator overflow. Sampling frequency affects the overall spectrum of the sampled continuous-time analog input presented to the digital filter, so the Nyquist criterion should also be carefully considered.

Consider the synthesis of an IIR digital bandpass filter centered at 2.25



1. THIS SYSTEM SHOWS the typical blocks contained in a digital-signal-processing channel. Digital filtering and other signal manipulation is carried out by the processor.

$$(1)\ H_1(s) = \frac{(2400\pi)^{10}}{[s^2 + 4741\pi s + (2400\pi)^2]\,[s^2 + 4276.8\pi s + (2400\pi)^2]\,[s^2 + 3394.2\pi s + (2400\pi)^2]\,[s^2 + 2179.2\pi s + (2400\pi)^2]\,[s^2 + 750.88\pi s + (2400\pi)^2]}$$

$$(2)\ H_2(s) = \frac{(6600\pi)^{10}}{[s^2 + 13038\pi s + (6600\pi)^2]\,[s^2 + 11761\pi s + (6600\pi)^2]\,[s^2 + 9334\pi s + (6600\pi)^2]\,[s^2 + 5992.8\pi s + (6600\pi)^2]\,[s^2 + 2065\pi s + (6600\pi)^2]}$$

$$(3)\ H_3(s) = \frac{s^{10}}{(2400\pi)^{10}}$$

kHz with a 1-kHz bandwidth. Engineers should be aware that some common pitfalls are involved in the filter design and analysis process. To create the filter, an analog 10th-order Butterworth IIR bandpass filter is first defined in the s-domain, and is then transformed to an equivalent digital filter in the z-domain using the bilinear transformation. The digital-filter-system function H(z) comes from performing the transformation on the analog-filter-system function H(s).

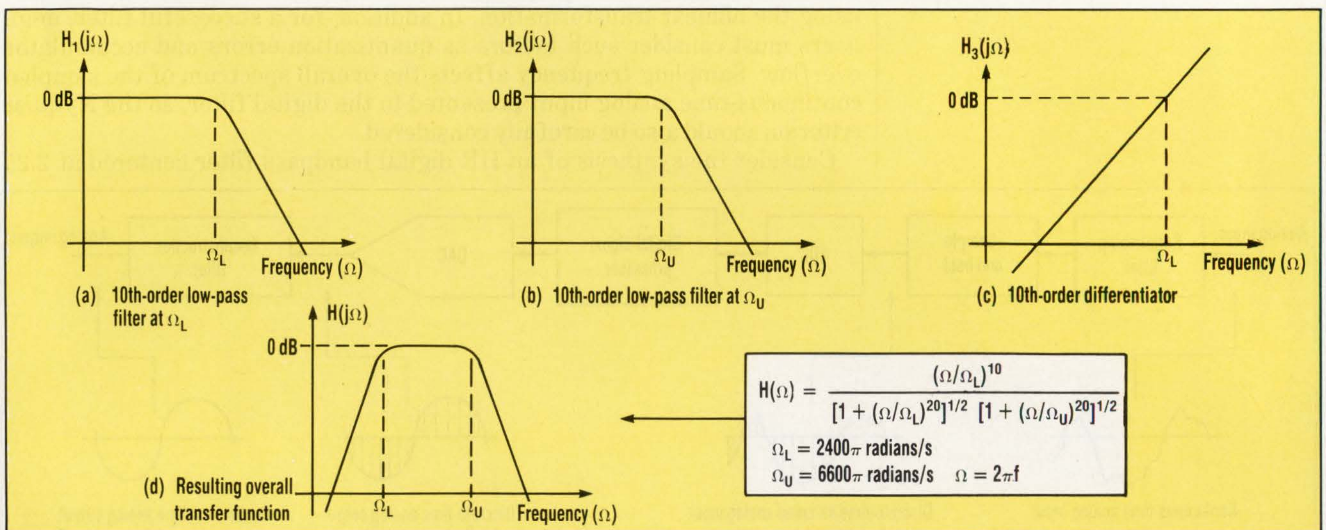
H(z) may then be implemented with a Direct Form II digital-filter structure using a digital-signal processor. The Butterworth characteristic is chosen in this case because it's monotonic (has no ripple) in both the passband and the stopband. In addition, it provides continued attenuation in the stopband instead of the ripple characteristic, such as those found in the Chebyshev and elliptic filter implementations. However, the benefit of having a steeper transition band is gained at the expense of the ripple characteristic when using Chebyshev or elliptic filters.

The IIR digital filter may be used as the heart of a system that might generally be termed a DSP channel. An antialiasing filter, data-acquisition system, digital-signal processor, and reconstruction filter circuits may be included *(Fig. 1)*. This configuration contains all or part of the blocks necessary for many applications, such as cellular telephones, compact-disc players, spectrum (or Fourier) analyzers, multisensor instrumentation, and digital control systems.

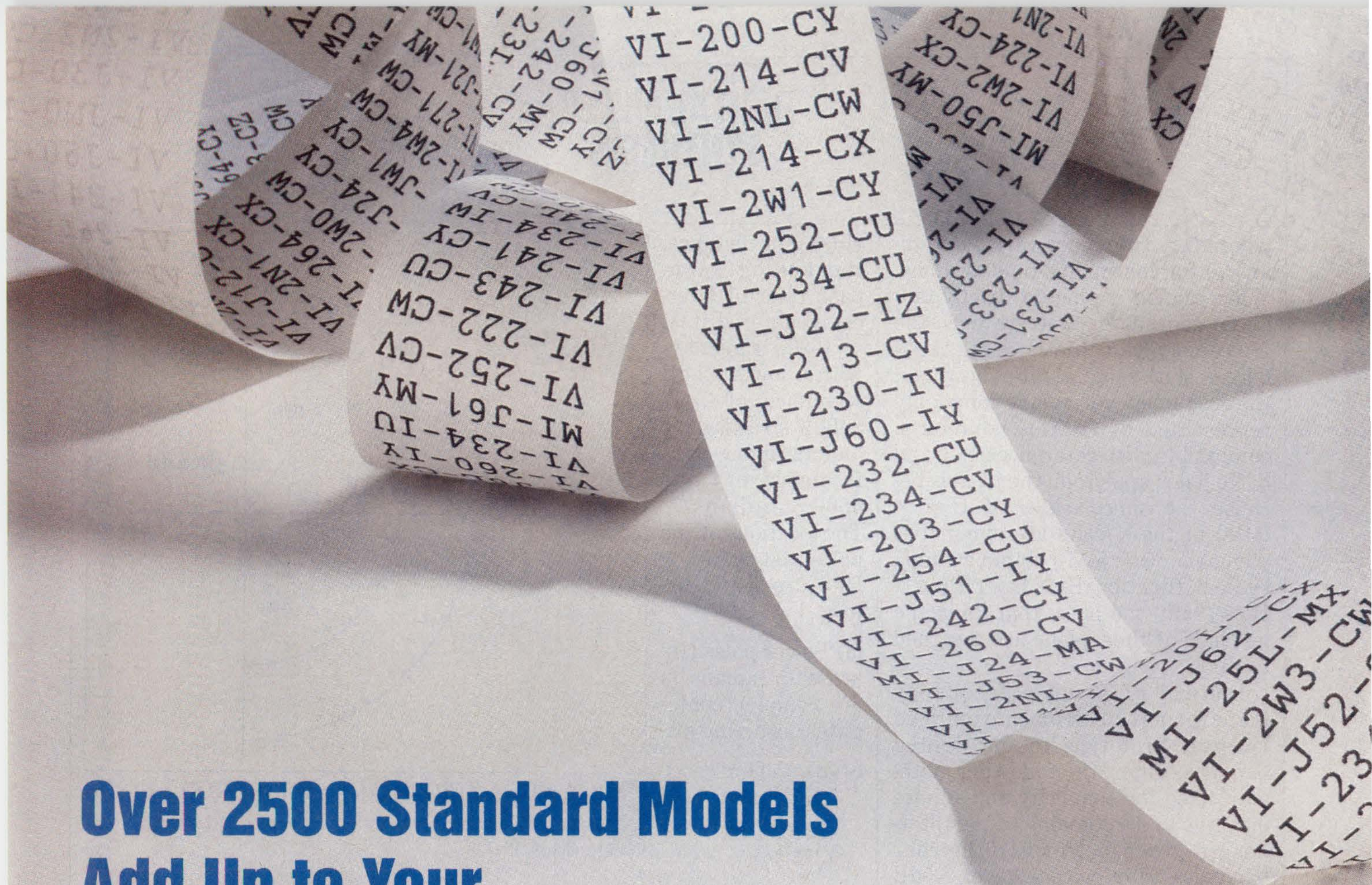
The frequency range for the analog signals being sampled and manipulated is typically in the audio band (telephone, compact-disc player, instrumentation), and out to 50 kHz or higher (digital control systems, spectrum analyzers). Engineers must consider both the effects of filter quantization errors and the selection of the sampling frequency when they apply a digital-filter solution to a given problem. It's quite surprising to see how quickly the filter design and analysis process becomes complex with the wide range of variables available for the simple IIR filter example presented in this article.

Frequency transfer function $H(j\Omega)$ of an analog continuous-time filter is related to the system function H(s) by the following useful relationship:

$$|H(j\Omega)|^2 = H(s) \times H(-s)|_{s=j\Omega} = H(j\Omega) \times H^*(j\Omega)$$



2. AN ANALOG BANDPASS FILTER'S frequency response can be broken into three components (a, b, and c). If the magnitude functions of the components are multiplied together, the result is the overall transfer function (d).



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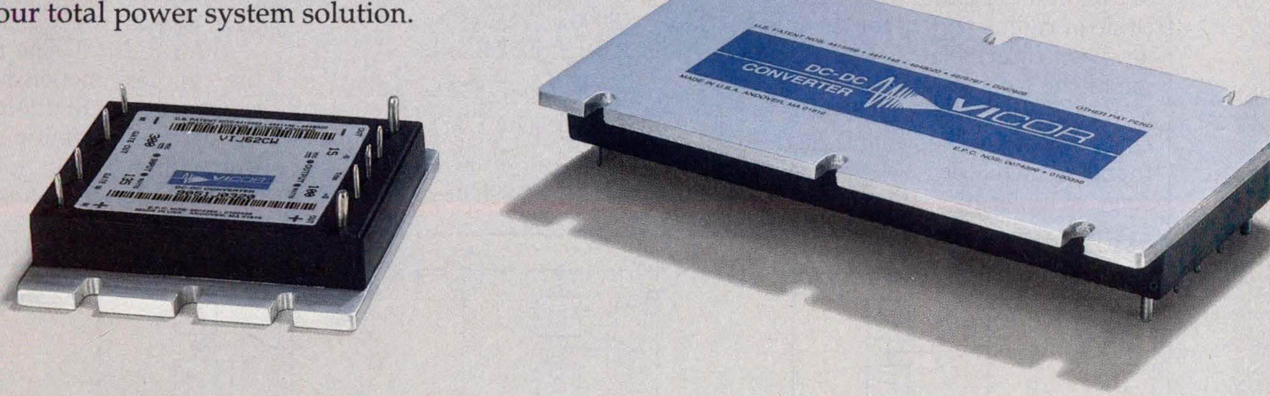

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where Ω = frequency variable (radians/s) for continuous-time systems. When analog engineers strictly talk about continuous-time systems, the frequency variable is designated with ω. With a digital filter, however, the frequency variable is commonly represented by Ω. This notation is compatible with references 1, 2, and 3. No poles appear on the $j\Omega$ axis because the singularities of $H(s) \times H(-s)$ in the s-plane are symmetric about the $j\Omega$ axis. To obtain a stable system function H(s) from $H(s) \times H(-s)$, only the poles that lie in the left half of the s-plane are assigned to H(s).

Instead of using a frequency transformation from normalized low-pass prototype to the desired bandpass filter, the following method is used for simplicity and a more intuitive understanding of the filter-design process. For a 10th-order bandpass filter with a lower –3-dB frequency Ω_L and upper –3-dB frequency Ω_U, the function H(s) may be broken into three parts: a 10th-order low-pass filter at Ω_L *(Fig. 2a)*, a 10th-order low-pass filter at Ω_U *(Fig. 2b)*, and a 10th-order differentiator (magnitude always increasing) at dc which has 0-dB crossing at exactly Ω_L *(Fig. 2c)*. The product of these three functions gives the desired overall bandpass system function in the analog s-domain, $H(s) = H_1(s) \times H_2(s) \times H_3(s)$ *(Fig. 2d)*.

Because both low-pass filters $H_1(s)$ and $H_2(s)$ possess a Butterworth characteristic, and the order of the filter is 10, the poles occur on a circle of radius Ω_L (Ω_U for the upper low-pass filter) centered on the origin of the s-plane, with a spacing of $\pi/10$ radians (18°). This allows the pole locations of $H_1(s)$ and $H_2(s)$ to be found immediately, as well as the singularity locations for the zeros in $H_3(s)$. For instance, the analog bandpass filter of interest is centered at $\Omega_o = 4500\pi$ radians/s with a lower –3-dB frequency of $\Omega_L = 2400\pi$ radians/s and an upper –3dB frequency of $\Omega_U = 6600\pi$ radians/s. The locations of the poles and zeros for H(s) are listed below:

(a) Lower poles ($\Omega_L = 2400\pi$ radians/s) are complex conjugates occurring at:

$S_{L\,1,2} = 2400\pi \times e^{\pm j189°} = -2370.5\pi \pm j(375.44\pi)$

$S_{L\,3,4} = 2400\pi \times e^{\pm j207°} = -2138.4\pi \pm j(1089.6\pi)$

$S_{L\,5,6} = 2400\pi \times e^{\pm j225°} = -1697.1\pi \pm j(1697.1\pi)$

$S_{L\,7,8} = 2400\pi \times e^{\pm j243°} = -1089.6\pi \pm j(2138.4\pi)$

$S_{L\,9,10} = 2400\pi \times e^{\pm j261°} = -375.44\pi \pm j(2370.5\pi)$

(b) Upper poles ($\Omega_U = 6600\pi$ radians/s) are complex conjugates occurring at:

$S_{U\,1,2} = 6600\pi \times e^{\pm j189°} = -6518.9\pi \pm j(1032.5\pi)$

$S_{U\,3,4} = 6600\pi \times e^{\pm j207°} = -5880.6\pi \pm j(2996.4\pi)$

$S_{U\,5,6} = 6600\pi \times e^{\pm j225°} = -4667.0\pi \pm j(4667.0\pi)$

$S_{U\,7,8} = 6600\pi \times e^{\pm j243°} = -2996.4\pi \pm j(5880.6\pi)$

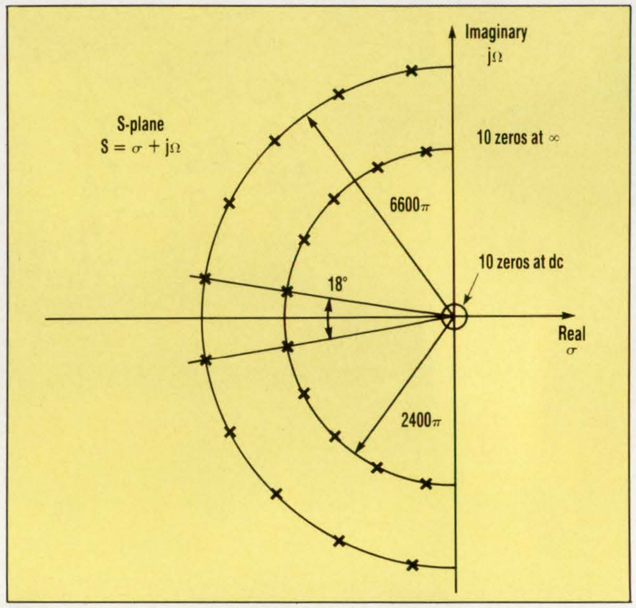
$S_{U\,9,10} = 6600\pi \times e^{\pm j261°} = -1032.5\pi \pm j(6518.9\pi)$

(c) Zeros (ten finite zeros) all occur at the origin in the s-plane.

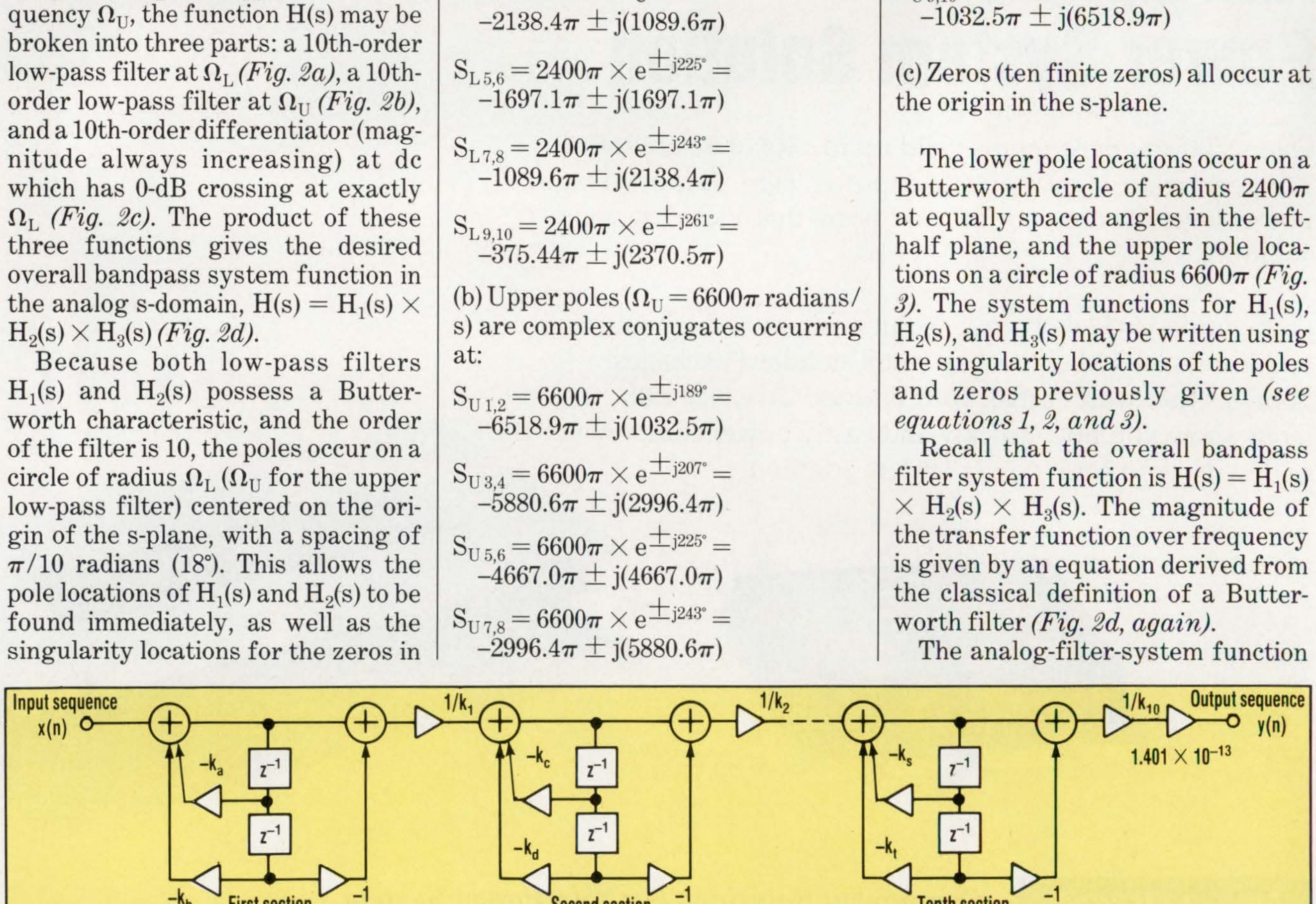
The lower pole locations occur on a Butterworth circle of radius 2400π at equally spaced angles in the left-half plane, and the upper pole locations on a circle of radius 6600π *(Fig. 3)*. The system functions for $H_1(s)$, $H_2(s)$, and $H_3(s)$ may be written using the singularity locations of the poles and zeros previously given *(see equations 1, 2, and 3)*.

Recall that the overall bandpass filter system function is $H(s) = H_1(s) \times H_2(s) \times H_3(s)$. The magnitude of the transfer function over frequency is given by an equation derived from the classical definition of a Butterworth filter *(Fig. 2d, again)*.

The analog-filter-system function



3. A POLE-ZERO DIAGRAM FOR H(S) shows singularity locations for an analog 10th-order Butterworth bandpass filter.



4. IIR DIGITAL FILTERS can be implemented in a Direct Form II using cascade second-order sections.

DIGITAL FILTER SYNTHESIS

H(s) may now be converted to a digital-filter-system function H(z) using the bilinear transformation. Other transformation methods could be used, such as the impulse invariance and step invariance methods. However, the bilinear transformation is an exact one-to-one mapping of the s-plane onto the z-plane, and in general gives better results than other methods. To find H(z), the following bilinear transformation is applied to H(s):

$$s = (2/T_s)\,\frac{(z-1)}{(z+1)}$$

where T_s = sampling period in seconds. Transformation may be broken down into three parts to simplify the task. The equations for $H_1(s)$ and $H_2(s)$ are of the following form:

$$H_{1,2}(s) = K_{1,2} \prod_{n=1}^{5} \frac{1}{s^2 + b_n s + c_n}$$

where $K_1 = (2400\pi)^{10}$ for $H_1(s)$, and $K_2 = (6600\pi)^{10}$ for $H_2(s)$. The variable s in $H_{1,2}(s)$ is replaced by the bilinear transformation expression given above to convert $H_1(s)$, $H_2(s)$, and $H_3(s)$ to their counterparts in the z-domain *(see equations 4, 5, and 6)*.

The final digital filter system function H(z) is then just the product of $H_1(z)$, $H_2(z)$, and $H_3(z)$, or $H(z) = H_1(z) \times H_2(z) \times H_3(z)$. The denominators of $H_1(z)$ and $H_2(z)$ are quite lengthy, but can be shown in simplified form *(see equation 7)*.

This equation may be evaluated once the sampling period T_s has been chosen, because every other parameter of the filter (passband gain, upper and lower –3-dB frequencies, and so on) have already been determined. To avoid the effect of frequency warping due to the bilinear transformation, the sampling frequency is chosen to be approximately 100 times the center frequency of the filter (f_s = 200 kHz, or $T_s = 5\ \mu s$). The effect of frequency warping can easily be overcome by pre-warping the original prototype analog-filter poles before the transformation. But for sake of simplicity, a sufficiently high sampling rate of 200 kHz is chosen to preclude this *(see equation 8)*.

This equation's form allows a Direct Form II structure of cascade second-order sections (CSOSs) to be used *(Fig. 4)*. The quantity x(n) is defined as the nth sample of the continuous-time input x(t), and y(n) is the output sequence of the digital filter. Also note that z^{-1} represents a unit sample delay. If a partial fraction expansion is performed on equation 8, then the structure may be realized with parallel second-order sections (PSOSs) as an alternative Direct Form II structure.

Once the desired filter structure is established, writing a software algorithm implementing the filter becomes a straightforward task. Digital filters, however, can be implemented in dedicated hardware. The structure of the digital filter in this

$$(4)\quad H_1(z) = \frac{(2400\pi)^{10}\,(T_s/2)^{10}\,(1+z^{-1})^{10}}{\prod_{n=1}^{5} (1 + b_nT_s/2 + c_nT_s^2/4)\,[\,1 + z^{-1}(c_nT_s^2/2 - 2)/(1 + b_nT_s/2 + c_nT_s^2/4) + z^{-2}(1 - b_nT_s/2 + c_nT_s^2/4)/(1 + b_nT_s/2 + c_nT_s^2/4)\,]}$$

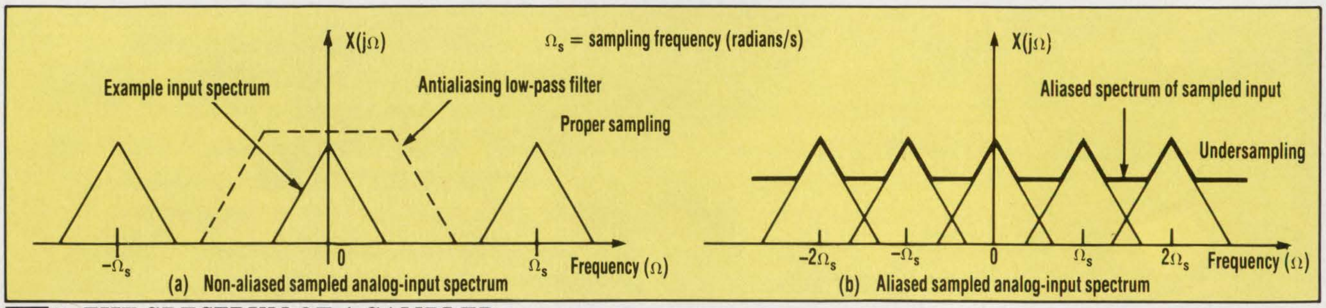
$$(5)\quad H_2(z) = \frac{(6600\pi)^{10}\,(T_s/2)^{10}\,(1+z^{-1})^{10}}{\prod_{n=1}^{5} (1 + b_nT_s/2 + c_nT_s^2/4)\,[\,1 + z^{-1}(c_nT_s^2/2 - 2)/(1 + b_nT_s/2 + c_nT_s^2/4) + z^{-2}(1 - b_nT_s/2 + c_nT_s^2/4)/(1 + b_nT_s/2 + c_nT_s^2/4)\,]}$$

$$(6)\quad H_3(z) = \frac{(1/2400\pi)^{10}\,(2/T_s)^{10}\,(1 - z^{-1})^{10}}{(1 + z^{-1})^{10}}$$

$$(7)\quad H(z) = (6600\pi)^{10}\,(T_s/2)^{10}\,\frac{(1 - z^{-1})^{10}\,(1 + z^{-1})^{10}}{\prod[\text{ Denominator of } H_1(z)\,]\ \prod[\text{ Denominator of } H_2(z)\,]}$$

$$(8)\quad H(z) = (1.401\times10^{-13})\,\frac{(1 - z^{-2})}{K_1(1 + k_az^{-1} + k_bz^{-2})}\,\frac{(1 - z^{-2})}{K_2(1 + k_cz^{-1} + k_dz^{-2})}\,\frac{(1 - z^{-2})}{K_3(1 + k_ez^{-1} + k_fz^{-2})}\,\frac{(1 - z^{-2})}{K_4(1 + k_gz^{-1} + k_hz^{-2})}\,\frac{(1 - z^{-2})}{K_5(1 + k_iz^{-1} + k_jz^{-2})}$$

$$\times\,\frac{(1 - z^{-2})}{K_6(1 + k_kz^{-1} + k_lz^{-2})}\,\frac{(1 - z^{-2})}{K_7(1 + k_mz^{-1} + k_nz^{-2})}\,\frac{(1 - z^{-2})}{K_8(1 + k_oz^{-1} + k_pz^{-2})}\,\frac{(1 - z^{-2})}{K_9(1 + k_qz^{-1} + k_rz^{-2})}\,\frac{(1 - z^{-2})}{K_{10}(1 + k_sz^{-1} + k_tz^{-2})}$$



5. THE SPECTRUM OF A SAMPLED continuous-time analog input signal x(t) has no aliasing when it's properly sampled above the Nyquist frequency (a). Aliasing occurs when the spectrum is undersampled below the Nyquist frequency (b).

article implies many multiply-and-accumulate operations *(Fig. 4, again)*. One possible implementation is to use a digital-signal processor. Floating-point digital-signal processors typically possess a dedicated hardware multiplier that can multiply two 32-bit floating-point quantities and sum the result in an accumulator in one machine cycle. One consequential benefit of the floating-point processor is an extremely wide range of numbers available in floating-point format, which prevents overflow problems when computing the solution for a digital filter.

Fixed-point digital-signal processors are typically faster and cheaper than floating-point varieties, but they carry quantization errors that may become intolerable in some applications. For example, quantization error can lessen filter coefficient accuracy and cause movement of the zeros of an FIR filter's H(z) function in the z-plane, or movement of the poles of an IIR filter's H(z) function in the z-plane. This ultimately triggers errors in the desired filter response. Because an IIR filter is recursive, movement of any system function poles outside the unit-circle in the z-plane due to quantization errors causes instability. One other quantization-error contribution is in the analog-to-digital conversion, which would depend on the ADC's resolution.

In fixed-point digital-signal processors, overflow can occur while the solution to a digital filter routine is being computed because of a limited numerical range. Care must be taken to avoid this or else a nonlinear response will result. Scaling techniques can be used to prevent overflow when using fixed-point processors, but at the cost of more program software and/or hardware.

Once the continuous-time input waveform is sampled, the digital-signal processor can compute the digitally filtered output sequence very quickly, assuming the various error sources are identified and controlled. This makes the digital-signal processor well-suited for the repetitive and complicated nature of most digital-filtering routines of both IIR and FIR types, as well as for FFT algorithms that perform manipulation and analysis in the frequency domain.

Sometimes it's useful to compare the filter frequency spectrum of an analog-filter transfer function $H(\Omega)$ with the spectrum of the corresponding digital-filter transfer function $H(e^{j\omega})$. In both cases, the Fourier transform evaluates the frequency response. The Fourier transform for a continuous-time analog-filter transfer function is found in a different manner than its corresponding digital-filter transfer function. For continuous-time systems, the Fourier transform $H(\Omega)$ is found from the impulse response h(t). For discrete-time (sampled data) systems, the Fourier transform $H(e^{j\omega})$ is found from the unit-sample response h(n), where H(z) is the z-transform of h(n). A short review of the applicable transform definitions may be helpful at this point:

Continuous-time (analog filter) systems:

$$h(t) \longleftrightarrow H(\Omega) \quad \text{Fourier transform pair}$$

$$H(\Omega) = \int_{-\infty}^{+\infty} h(t)\, e^{-j\Omega t}\, dt$$

Discrete-time (digital filter) systems:

$$h(n) \longleftrightarrow H(e^{j\omega}) \quad \text{Fourier transform pair}$$

$$H(e^{j\omega}) = \sum_{-\infty}^{+\infty} h(n)\, e^{-j\omega n}$$

$$h(n) \longleftrightarrow H(z) \quad \text{z-transform transform pair}$$

$$H(z) = \sum_{n=-\infty}^{+\infty} h(n)\, z^{-n}$$

Note that Ω has units of radians/s, and that ω has units of radians per sample interval, and the two are related by $\Omega = \omega/T_s$. This can some-

DIGITAL FILTER SYNTHESIS

times cause confusion for analog design engineers because ω typically has units of radians/s when dealing with strictly analog continuous-time systems. There's also a convenient relationship between the discrete-time digital-filter-system function H(z) and the Fourier transform $H(e^{j\omega})$ of the unit-sample response h(n). This allows the frequency-spectrum characteristics of the digital filter to be found directly from the system function H(z):

$$H(e^{j\omega}) = H(z)\big|_{z=e^{j\omega}}$$

For $H(e^{j\omega})$ to exist, the digital filter must be causal and stable. In the example in this article, the digital filter was based on a stable and causal analog filter, therefore, $H(e^{j\omega})$ exists (assuming negligible quantization error effects). This implies that each pole of H(z) lies within the unit circle in the z-plane.

THE FREQUENCIES OF THE ANALOG INPUT BEING SAMPLED MUST BE LIMITED TO ONE-HALF THE SAMPLING FREQUENCY.

The Fourier transform of the sampled analog input $X(j\Omega)$ to the filter demonstrates the effect of discrete-time sampling of the continuous-time analog-input waveform x(t) at sampling frequency $\Omega_s = 2\pi f_s$ *(Figs. 5a and 5b)*. The spectrum is periodic in frequency, which means that the original continuous-time analog input spectrum is replicated at every harmonic of the corresponding digital filter's sampling frequency Ω_s.

An antialiasing filter prevents aliasing of any undesired high-frequency components of the original analog-input spectrum into the frequency band of interest due to the sampling process. The frequencies of the analog input being sampled and quantized (for later use in the digital-filter algorithm) must be limited to one-half the sampling frequency Ω_s. This requirement is the well-known Nyquist criterion. The Nyquist rate is defined as the smallest sampling rate that may be used before aliasing occurs. Typically, an analog low-pass filter is used to provide this antialiasing filter function *(Fig. 5a, again)*.

In cases where the sampling frequency isn't much higher than the Nyquist rate, careful attention must be paid to the antialiasing filter design so that it doesn't accidentally affect the frequency band of interest. At the same time, it must ensure adequate attenuation at one-half the Nyquist rate to prevent aliasing. When aliasing does occur, it manifests itself by summing frequency components of the replicated input-frequency spectrum (generated during the sampling process) with the original input frequency spectrum. Undersampling causes the replicated input spectrum to sum with the original input spectrum, prompting an erroneous result *(Fig. 5b, again)*.□

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Richard F. Betts, an engineering specialist for Eldec Corp., holds a BSEE and MSEE from the University of Washington, Seattle.

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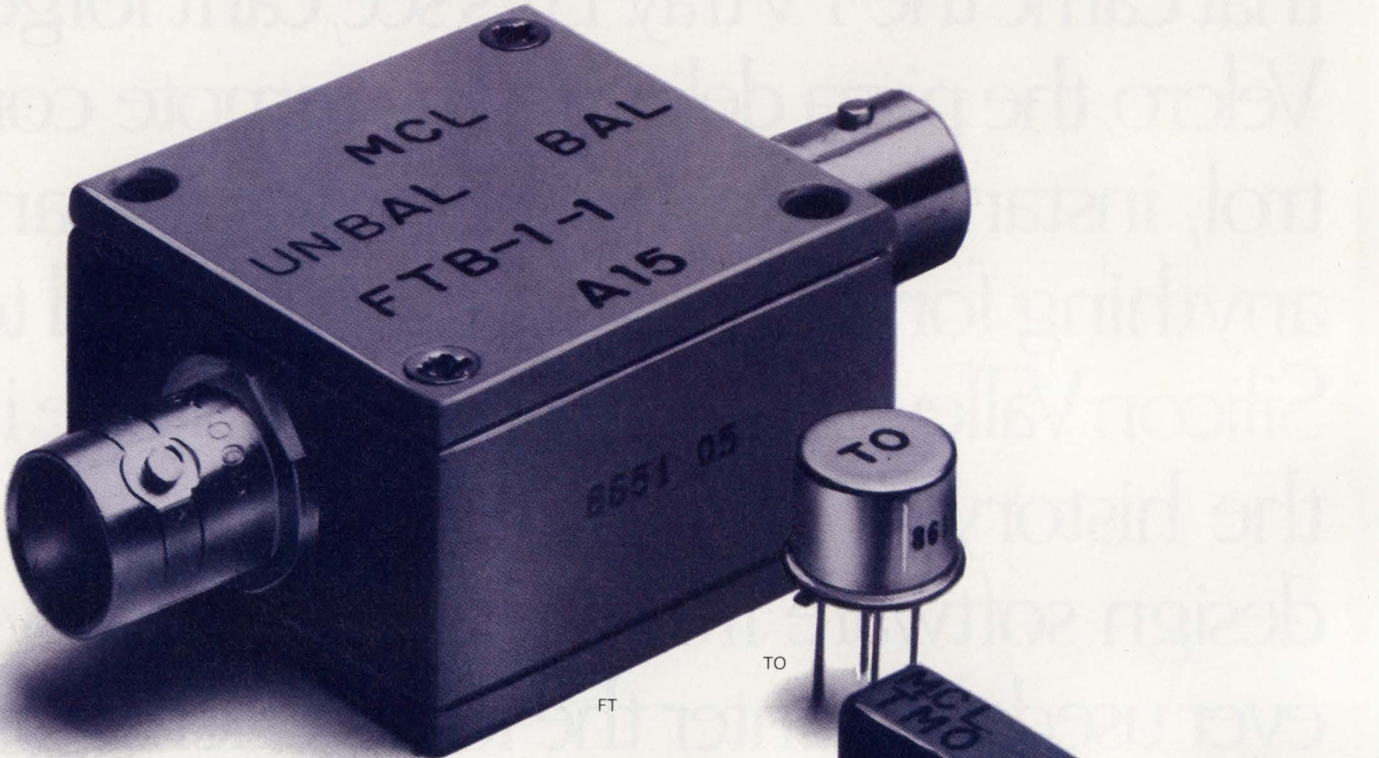

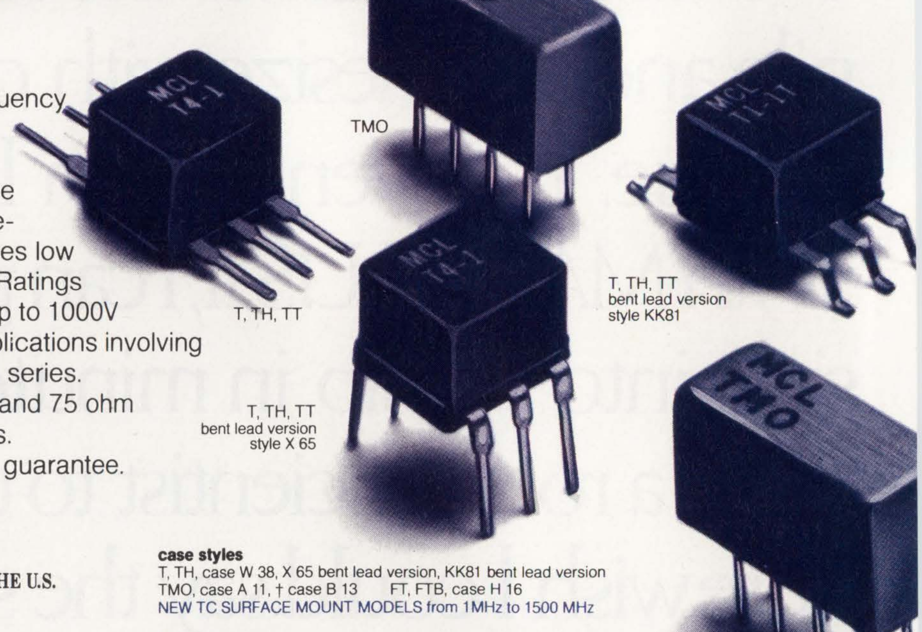

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T1-1	5950-10-128-3745	TMO2.5-6T	5950-01-215-8697
T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
T16-1	5950-01-094-7439	TMO9-1	5950-01-141-0174
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C71 REV. B

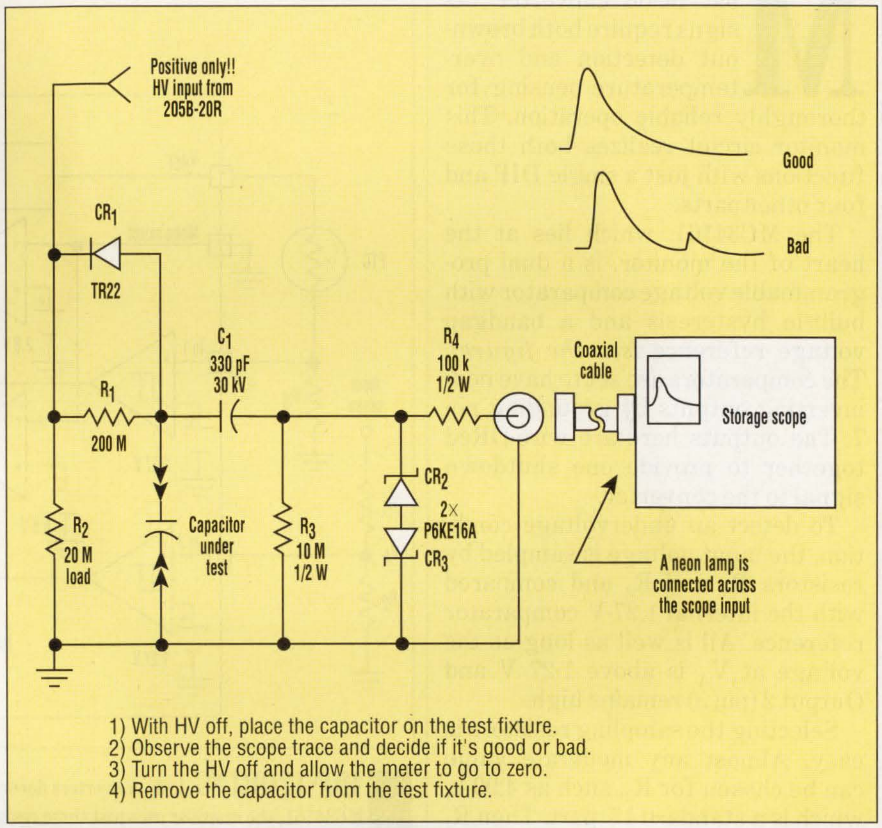
CIRCLE 521

TEST HIGH-VOLTAGE CAPACITORS SAFELY

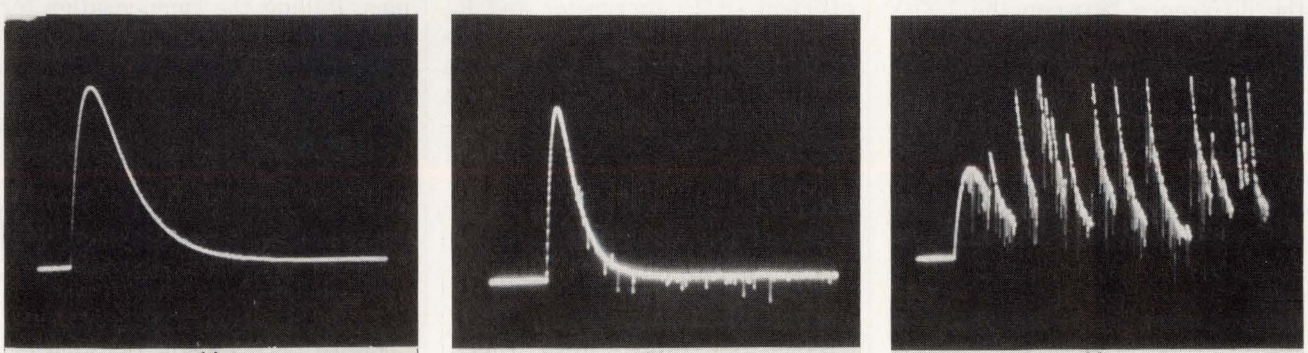
JOHN DUNN
181 Marion Ave., Merrick, NY 11566; (516) 378-2149

Here's a handy test fixture for evaluating high-voltage capacitors at rated voltages up to 20 kV. A Bertan High Voltage model 205B-20R supply, or equivalent, delivers a very pure, high-voltage dc input that's applied to the capacitor under test (CUT) through a safety resistor of 200 MΩ *(Fig. 1)*. The supply is set to deliver the intended test high voltage, and its rear-panel remote/local switch is placed in the remote position with without applying a remote-programming input signal. The CUT is then installed in the test fixture. When the remote/local switch is moved from remote to local, the high-voltage output turns on, and the test waveform, which represents the high-pass-filtered voltage across the capacitor under test, is observed using a storage scope *(Fig. 2)*. When the switch is returned to the remote position, the 20-MΩ load and the diode provide a relatively rapid discharge path for the CUT. For safety purposes, the CUT should be discharged completely before attempting to remove the capacitor.

Note: The following component types (or their equivalents) should be used in the test fixture. CR_1 is type TR22 from Electronic Devices Inc., Yonkers, N.Y. R_1 (200 MΩ) and R_2 (20 MΩ) are type MD810 from Caddock Electronics Inc., Riverside, Calif. Also C_1, which isolates the scope from the test fixture, should be a 330-pF, 30-kV reconstituted mica.□



1. WITH THIS TEST FIXTURE, high-voltage capacitors can be evaluated with test voltages up to 20 kV. The capacitor charges through R_1, a 200-MΩ resistor, and discharges through CR_1 and R_2, which is 20 MΩ.



2. TESTED AT ITS RATED voltage, a very-high-quality 0.0022-µF, 15-kV capacitor exhibits a flawless trace (a). Scope settings are 1 V/div. and 0.5 s/div. A poor-quality capacitor exhibits multiple scintillation spikes at 15 kV (b). Scope settings are 1 V/div. and 1 s/div. A capacitor that catastrophically fails is easy to spot (c). Scope settings are 2 V/div. and 0.5 s/div.

CIRCLE 522

IC Eases Monitoring Of Dc-Dc Converters

STEVEN C. HAGEMAN
Calex Manufacturing Co. Inc., 3355 Vincent Rd., Pleasant Hill, CA 94523;
tel.: (800) 542-3355, fax (415) 932-6017.

Most dc-dc converter designs require both brownout detection and over-temperature sensing for thoroughly reliable operation. This monitor circuit realizes both those functions with just a single DIP and four other parts.

The MC34161, which lies at the heart of the monitor, is a dual programmable voltage comparator with built-in hysteresis and a bandgap voltage reference *(see the figure)*. The comparators are set to have non-inverting outputs by grounding pin 7. The outputs here are wire-ORed together to provide one shutdown signal to the converter.

To detect an undervoltage condition, the input voltage is sampled by resistors R_1 and R_2 and compared with the internal 1.27-V comparator reference. All is well as long as the voltage at V_A is above 1.27 V and Output 2 (pin 5) remains high.

Selecting the sampling resistors is easy. Almost any moderate value can be chosen for R_2, such as 4.99 k, which is a standard 1% part. Then R_1 is given by:

$$R_1 = 4990[(V_L/1.245) - 1],$$

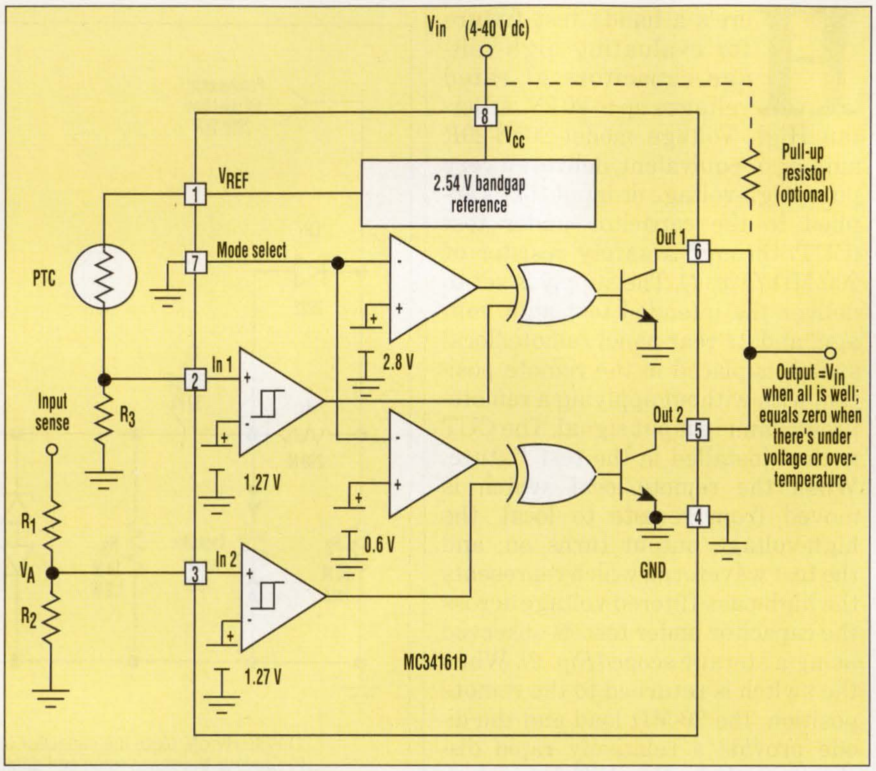
where V_L is the desired trip point for the input voltage. The figure 1.245 is the difference between the 1.27-V threshold level and the comparators' built-in 0.025 V of hysteresis.

That hysteresis is important for an undervoltage lockout function to keep the dc-dc converter from oscillating at the trip point. Oscillation can easily happen because the input voltage will tend to rise slightly when the converter turns off. To make Output 2 high again (after it goes low), the input must rise to a value given by:

$$V_H = 1.27[(R_1/4990) + 1].$$

The over-temperature sensing is performed by a voltage divider composed of the positive temperature coefficient (PTC) thermistor and R_3. The PTC chosen for this example has a resistance of 2 kΩ at 25°C and a switching temperature of 80°C. At that temperature, its resistance increases to 10 kΩ. To make Output 1 go low at that point, R_3 is also selected to be 10 kΩ. For best results, the PTC should be mounted on the same heat sink as the main switching transistor and the output rectifier diodes. The temperature hysteresis in this circuit was measured at about 5°C.

The monitor circuit's output is easily linked to most switching power-converter ICs via their compensation pins. Pulling the compensation terminal low typically causes the output pulse width to go to zero, effectively turning the converter off. ICs that can be turned off in this way include the SG3524 and LT1070 families.□



MONITORING dc-dc converters doesn't get much easier than this. In addition to the MC34161, the monitor uses just three resistors and a PTC thermistor. Although this circuit was tested with a Midwest Components 180Q20206 thermistor, suitable devices are also available from Murata Components and Western Electronic Components.

Send in Your Ideas for Design

Address your Ideas-for-Design submissions to Richard Nass, Ideas-for-Design Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604.

VOTE!

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $150 Best-of-Issue award and becomes eligible for a $1,500 Idea-of-the-Year award.

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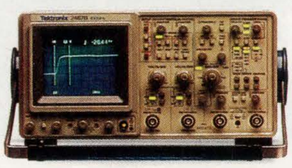

There is a far side to the world of oscilloscopes, a place filled with all sorts of bizarre characters. Like those who swear you need digital, for the sole reason that digital is all they wish to sell. Then there's the gang that wants to push nothing but analog. Luckily, there's also a place called Tektronix. Where they manufacture a complete line of analog and digital scopes. Making them uniquely qualified to provide you with a more honest assessment of your needs. With anyone else, you could be hearing only half the story. For complete information on the full line of Tektronix analog and digital oscilloscopes, get in touch with a Tek representative today. **TALK TO TEK/1-800-426-2200**

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CIRCLE 523

DIGITAL PLL SUITS FPGAS

DENNIS McCARTY
Actel Corp., 955 East Arques Ave., Sunnyvale, CA 94086; (408) 736-1030.

In telecommunications applications, it's often desirable to generate a digital signal that's locked to an incoming signal and is some multiple of its frequency. A simple way to generate such a signal uses a pulse-steal phase-locked loop, or PLL *(see the figure)*. The design contains an ordinary oscillator, but no voltage-controlled oscillator (VCO). And, except for the crystal, the entire design will operate in an FPGA.

Consider the frequency relationship at points A and B in the circuit:

$$OSC/(K \times M) = F_{in}/N = F_{comp},$$

where OSC = effective reference frequency and F_{comp} = comparison frequency.

The technique is based on selecting a reference oscillator frequency which is slightly higher than OSC. This frequency (OSC+) should be chosen so that:

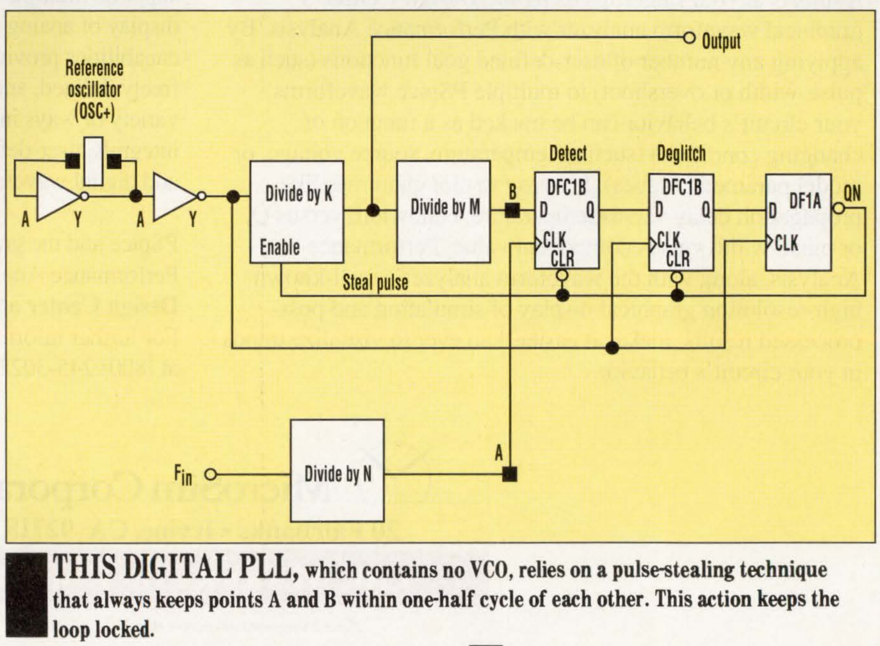
$$(1/F_{comp}) - (K \times M)/(OSC+) = 0.5(1/OSC)$$

The right side of this equation equals one-half the period of the reference oscillator.

The reference-oscillator frequency delta will cause point B (the detector flip-flop D input) to begin to precede point A (the detector flip-flop clock input) by half a period each comparison interval. When the edge of the D input advances sufficiently, the detector will clock true and begin a pulse train through the two deglitching flip-flops. The output of the second of these clears all three flip-flops and steals a pulse by disabling the divide-by-K output. Stealing the pulse puts point B behind point A until the reference-oscillator delta can move it ahead by one period—thereby repeating the cycle. Points A and B are always within one-half a cycle of each other.

To select the output signal's frequency, simply adjust the values of dividers K and M. The lock range of the loop is given by:

$$\text{Lock Range} = \pm(OSC+/OSC)/F_{in}$$ □



THIS DIGITAL PLL, which contains no VCO, relies on a pulse-stealing technique that always keeps points A and B within one-half cycle of each other. This action keeps the loop locked.

Explore the Intricacies of Your PSpice Circuit Simulation . . .

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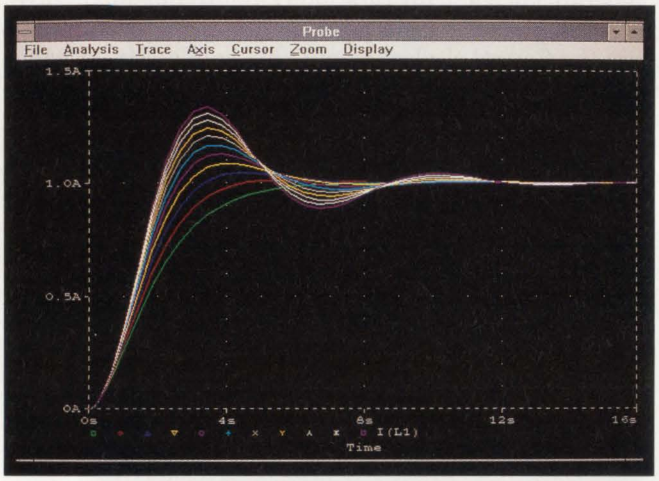
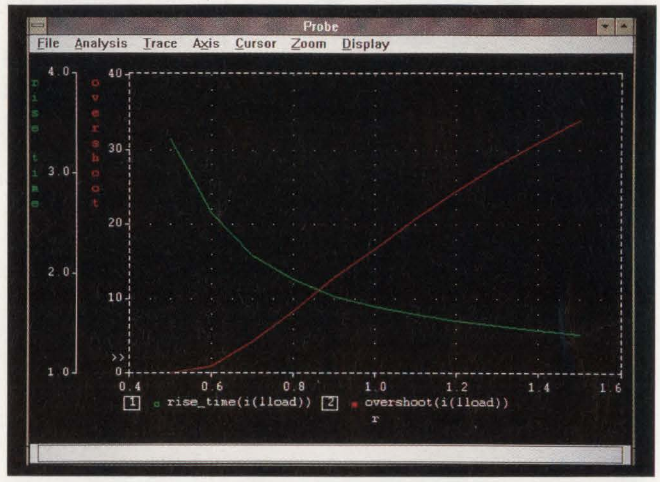


Current through an inductor with stepped resistance



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QUICK LOOK

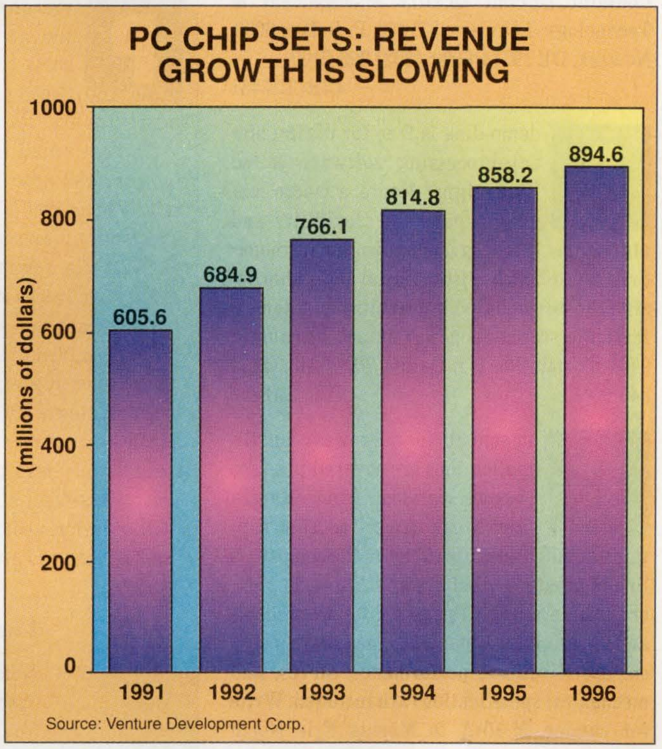
EDITED BY SHERRIE VAN TYLE

MARKET FACTS

Slowing sales in the personal computer market and a drop in average chip prices are putting the brake on revenues for PC chipsets. From sales of $605 million last year, revenues for PC motherboard chip sets will increase to around $895 million in 1996, according to Venture Development Corp. The compound annual growth rate amounts to just over 8%, says the Natick, Mass., market researcher.

The chipset market is splintering, with some sectors maturing and others emerging. Fastest growth is found in the markets for hand-held and pen-based computers, with compound annual growth of nearly 85%. Because most of these compact machines rely on proprietary chipsets, chip vendors haven't reaped the benefits yet. As vendors meet demands for low power and low voltage operation, merchant sales should climb, starting this year.

Desktop computers still account for most of the chip sets, with sales last year of $455 million in motherboard chips. Yet revenue growth should average out to be a mere 4.5%, with fastest growth in chips sets that can support Windows and multimedia features. As standards evolve for multimedia and local-area networks, chip vendors can reduce costs by moving peripheral functions onto the motherboard. VDC also predicts strong growth in semicomputers—chips that integrate the microprocessor and its system logic onto one IC, such as those from Advanced Micro Devices, Chips and Technologies, and Intel.



TIPS ON INVESTING

Mutual funds continue to be the investment of choice for many engineers today. Despite stormy times in the financial markets—recession, a banking crisis and the repercussions of global conflict—mutual funds continue to experience exponential growth because they offer a range of benefits that few other investments can match.

By the end of 1990, total fund assets grew to $1.1 trillion, representing some 60 million shareholder accounts. Even more noteworthy, about 3,400 mutual funds are registered with the Securities and Exchange Commission. This means that, even excluding the popular money market funds, more mutual funds than stocks are listed on the New York Stock Exchange.

Mutual funds may be attractive because of their simplicity and convenience, yet today's menu of funds is anything but simple. There are country funds for almost every corner of the globe, sector funds for scores of industry groups, index funds tied to most major financial averages, and even funds made up of other mutual funds.

For many engineers, this wealth of choices has made choosing a mutual fund a formidable task. Besides surveying the fund universe, investors must also assess the impact of varying costs and charges, determine which funds are best suited for a variety of financial objectives and wade through a torrent of available data and information.

A mutual fund is an investment company that pools the money of many individuals and invests it on their behalf. In accordance with predetermined goals, this pool of money is generally invested in stocks, bonds, or money market securities by a professional portfolio manager, who receives a fee for his or her services.

Mutual funds issue shares, each of which represents proportional ownership of all the securities held by the fund. If a fund's securities produce current income or capital gains, these are passed along to investors based on the number of shares owned. Most funds stand ready to issue new shares as more money is invested and to buy back (redeem) shares as money is withdrawn.

Mutual funds offer diversification—owning just a few securities can be risky. If one security performs poorly, the total investment may suffer. Mutual funds generally distribute the pool of shareholder assets across many securities, lessening the potential for any one investment to have a negative effect on the total portfolio. Read more on mutual funds in the next column.

Henry Wiesel is a financial consultant with Shearson Lehman Brothers, 1040 Broad St., Shrewsbury, NJ 07702; (800) 631-2221. Wiesel, also a qualified pension coordinator with The Private Client Group, invites questions and comments.

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CIRCLE 451

A demo disk is free for digital signal processing software called Hypersignal Macro, a macro language that adds flexibility and algorithms to a program known for its menu-driven lab-bench utility. Initial algorithm design can be cemented into arbitrary, automatic, single-step sequences. Contact Signalogic, 9704 Skillan, No. 111, Dallas, TX 75243; (214) 343-0069.
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CIRCLE 453

A short form catalog from Sprague-Goodman Electronics covers trimmer capacitors and specialty inductors, which go into standard and surface-mounted applications. Catalog C-100A has product features, specifications and photos, plus information on capacitor application and a trimmer capacitor comparison chart. Contact Bernice Feller, Sprague-Goodman Electronics Inc., 134 Fulton Ave., Garden City Park, NY 11040-5395; (516) 746-1385; fax (516) 746-1396.
CIRCLE 454

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CIRCLE 455

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458; fax (408) 253-6085

Product classifications of first-of-a-kind, me-too, derivative, and next-generation have been introduced and previously referenced. A simple matrix representation explains relationships between each of the categories. This column introduces the product classification matrix, which I'll continue to explore in future columns.

The horizontal axis is labeled product concept. This axis is further segmented into familiar and new. The people who produce the product's definition determine its x-axis relative position. Their decision is communicated to and discussed with top management. Frequently discussion and interaction is required to arrive at an agreed upon placement. For example, a component manufacturer's view of a product concept is different from that of a system integrator.

A company that survives by producing resistors may see the cylindrical stripped variety fall into the familiar classification whereas surface mount resistors may very well be new from a concept perspective. Likewise, a manufacturer of computer systems may see designs based on single X86 series processors as familiar while those designs based on multiple reduced-instruction-set (RISC) processors are perceived as new. To get product classification right, people have to talk. Attempting to place these concepts on an x-axis gets the whole process started.

To develop a common understanding, see if you agree with the x-axis placement of the product concepts given below:

Familiar	New
Notebook PC	Video toaster
Workstation	Picture phone
Fax/modem	High-definition TV
Mini printer	Flash memory

The next step is to imagine yourself developing each of the products listed above as you give thought to the markets in which they will be sold. Is the market familiar or is it new? For the notebook PC, the workstation, and high definition TV, the markets served are established and somewhat understood. Quite likely the remaining five products will develop and then serve new markets.

Once the product development effort is understood from the product and market points of view, classification is straight forward. The notebook PC and workstation are me-too efforts. The fax/modem and mini-printer are derivative products. High-definition TV is a next-generation effort. The video toaster, picture phone, and flash memory are first-of-a-kind products.

Positioning a new product development effort on this matrix reveals a significant amount of information about what you can expect from the venture. Also, if your organization is developing a number of new products, you might find it interesting to see if your work effort is concentrated in a single cell or if your company has a diversified new product development portfolio.

Future columns will explore each cell of the matrix, and some basic strategic issues will be made visible by using the matrix.

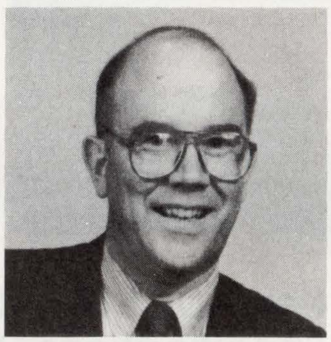
Ron Kmetovicz will lead a Time-to-Market seminar entitled "Speeding New Ideas to the Marketplace" at Santa Clara University's Executive Development Center, to be held March 19, 1992. For more information call Elmer Luthman, center director, at (408) 554-4521; fax (408) 554-4571.

TALES FROM THE SKUNK WORKS

When I give a talk on how to improve competitiveness, I always mention using skunk works teams. Listeners often ask me: "How can we start? How can we convince or persuade our management to allow us to form such teams and function autonomously?"

Tongue-in-cheek I sometimes suggest that a "trust us" strategy might work. The audience usually laughs, and rightly so: *Trust must be earned*. Consider the depth and breadth of trust needed for a skunk works. In most companies it is unlikely that any one functional manager "owns" the diversity of talent needed. Higher level managers are understandably reluctant to reach down and dictate resource assignments in the organizations that report to them. Seasoned managers know that even the strongest desire, abstract knowledge, professional competency, and motivation probably won't allow them to succeed at a skunk works the first time.

Let me elaborate on the last point. Suppose you wanted to become a world-class tennis player. Would studying a book on the sport be sufficient? Would watching professional matches be sufficient? Would taking a few lessons be sufficient? Of course not. If you play at level one and want to reach level ten, the only reasonable way to get there is by acquiring the necessary skills and abilities one step at a time. Pick your matches. If your opponents are too good, you will lose too often and become discouraged.



High-tech business is the most demanding game on the planet, and I know of no quick fixes or magical techniques that allow success. The idea that a motivated but inexperienced team can beat the world's best is a very unlikely proposition. Any manager who gambled millions of dollars on such an effort that failed probably world find her career severely limited.

In the U.S. we like to gamble, yet the odds of winning a lottery are about the same as finding the money in the street. The success rate of our new high-tech ventures and products is abysmal, so the Japanese tortoise is beating the U. S. hare.

I suggest that you will need management's trust, and that this trust must be *earned* by producing business results consistently. Another crucial acceptance is that only teams can do products. Individuals can do science, but no single individual can bring a new computer or a new compiler to market. Since technology alone will not get you there, trust must go beyond the technologist.

Why did Lockheed's skunk works survive for decades but vanish shortly after Kelly Johnson's retirement? Did the company's technology or engineering ability suddenly fade? More likely, the management's trust and confidence did not extend beyond Johnson.

A skunk works requires trust. Trust starts with the leader, but it must then extend to the team. Team members earn trust by producing a string of increasingly significant victories. The process can be accelerated by hiring the right consultants as coaches and scouts.

John D. Trudel lectures and provides business development consulting: The Trudel Group, 52001 Columbia River Hwy., Scappoose, OR 97056; (503) 690-3300; fax (503) 543-6361. To order High Tech with Low Risk: *(503) 962-3755.*

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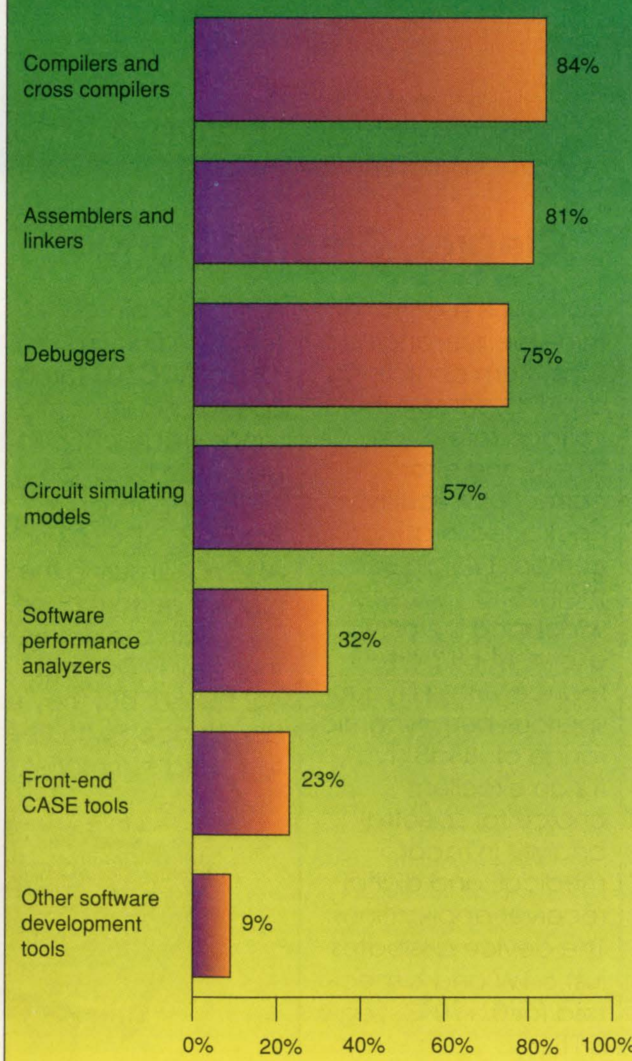
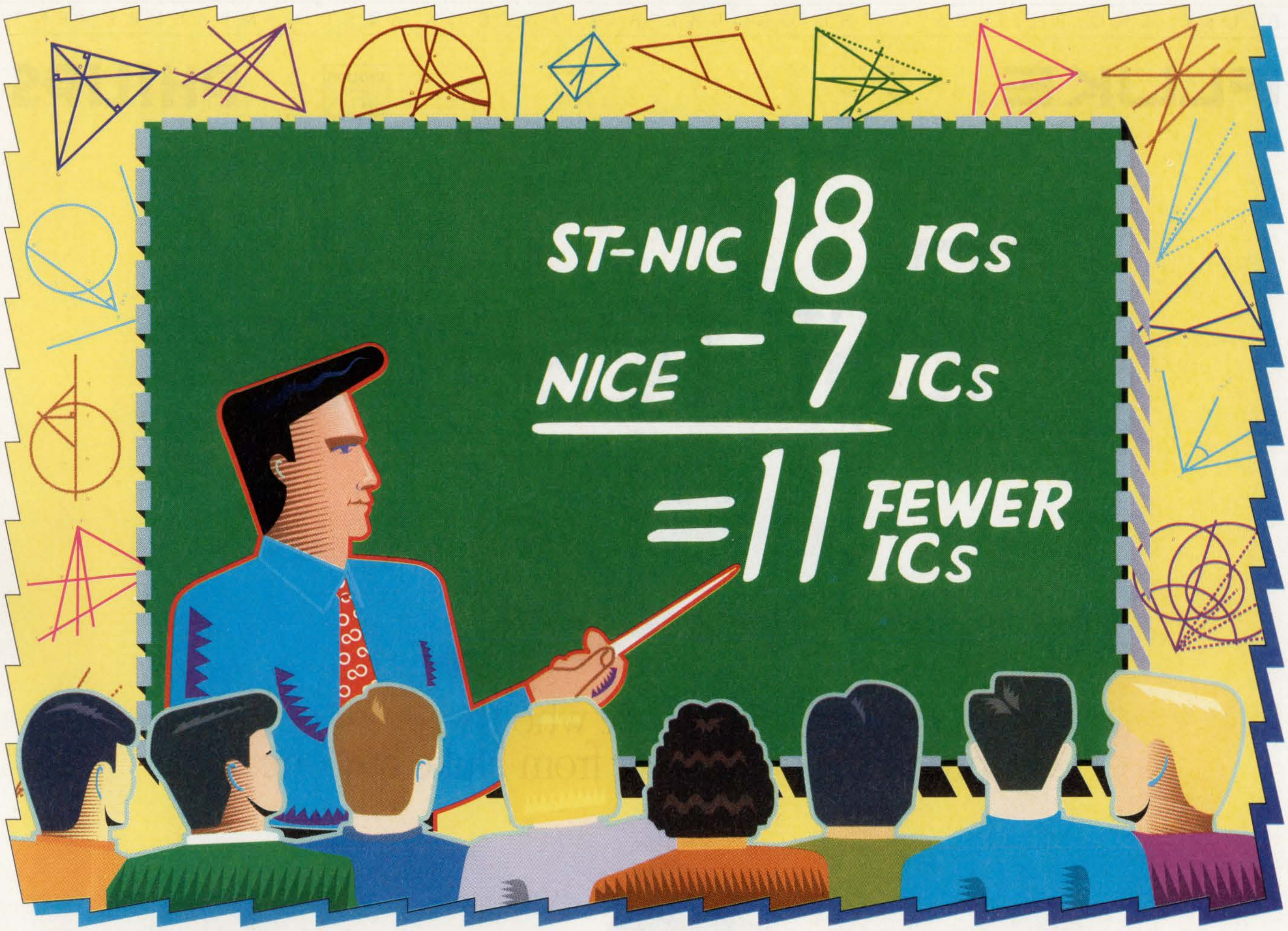
CAD/CAE SURVEY

WHICH SOFTWARE DEVELOPMENT TOOLS DO YOU USE?



Source: a survey of Electronic Design readers by The Adams Co., Palo Alto, Calif; (415) 325-9822.

Readers gave more than one answer to question



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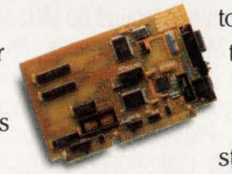

And, unlike other available solutions, NICE has been designed to *fully* comply with Ethernet standards—ensuring international interoperability. And that's no myth.

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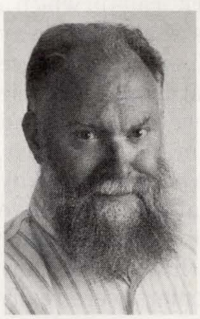
CIRCLE 96 FOR U.S. RESPONSE

CIRCLE 97 FOR RESPONSE OUTSIDE THE U.S.

What's All This Applications Engineering Stuff, Anyhow?...

...Or, Why Being an Applications Engineer is Sometimes Like Being Nibbled to Death by Ducks.

When I first started to work for National 16 years ago, I thought I was going to learn how to design good monolithic ICs. And I did, eventually. But the very first day on the job, Pete Lefferts gave me National's new 1976 Linear databook, with a list of 10 ICs taped onto the front cover. "These are the ICs that our group is responsible for. In our group, we design engineers also handle the applications engineering for our parts," Lefferts said.



BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

Well, that setup sounded pretty good to me, because up to that time I had been pretty much an expert at applying ICs. I soon figured out how to field and answer most of the calls cheerfully. Of course, there were some calls too technical for me to know the answers. So, I just took good notes and then got some help from other more knowledgeable guys. I learned how to steer the customer to the right op amp (whether we made it or not). I learned how to explain to a customer that a TO-3 regulator could dissipate 20 W, *but* only if attached to a heat sink. I even learned to refer to an LM741, rather than a µA741.

The most important thing I learned was that if you want to avoid lots of "dumb" phone calls, you should write a very good, clear, comprehensive data sheet. When customers ask for needed information that wasn't included, it's not a *dumb* question, but rather a *dumb* data sheet. At least 30% of the calls were caused by a lack of sufficient information in the data sheet. So I learned to put *lots and lots* of good info, necessary info, into my data sheets. The penalty for not doing so is having to answer "dumb" questions forever.

That reminds me of the Quality Control procedures for the "riggers," the people who pack parachutes. Obviously, packing parachutes is a very serious, very responsible job. How do you make sure that the guy packing 'chutes never gets sloppy, never goofs off? Ah, very simple: At the end of every month or so, each parachute rigger is invited to select one chute at random from a pile of all the chutes he has packed, and then he goes up and jumps out of a plane. Ah, if only there were QC procedures as good as that one, one that we could design for other jobs! If only we could all have such a good incentive to do perfect work. But in general there is not...if you can name one, you tell me.

Anyhow, in the last five years, our Linear group has moved further away from the concept of having every Design Engineer do applications engineering, too. This certainly makes some sense. There are some people who are really good at designing silicon, and it's not fair to tell them they can't do it if they're not also good at talking with customers on the phone.

So now we have gone into a little bit of specialization. Unfortunately, it often means that an apps engineer gets on the phone to discuss a big project, and soon needs "a band-aid to put on his ear." There are times when an hour on the phone is needed for a special case, and that really is tough on the ear. In other cases, an apps engineer gets on the "MAC," and works on several data sheets for a sprint lasting several days. I don't think I would enjoy that. Still, there are detailed technical problems that are appropriate for me to answer, and I still help out on specialized facets of applications engineering. I just don't get to take so many "cold" calls.

But what is the crucial thing about the applications engineer's job? I guess it's that he (or she) is an *interface*. Whenever the design engineer wants to design a piece of silicon to make a customer happy, the apps engineer should help facilitate the process, by showing the best way to teach the customer how to apply the circuit. He has to write a clear data sheet, list all of the features and specs, spell out cautions, and show what new applications are suitable.

What if the proposed silicon is lacking a necessary feature? Then the apps guy has to holler "WHOA!," until the need for that feature (or the lack of that feature) is resolved.

One time I was doing a redesign of a regulator, and the apps guy wanted me to add in protection so all of the pins would be ESD-proof, up to 2000 V. But I argued that if we added that protection, the circuit would not work in some existing sockets. Finally we compromised. I agreed to add all of the ESD-proofing I could so that the part could work in existing sockets. We wound up with a part that would pass only 800 V by itself, but when plugged into a usage circuit, its ESD tolerance was improved up to 2 kV because some pins linked together.

Other times, when a customer has difficult questions about an IC, the apps guy acts as a filter to make sure that all of the relevant questions get asked. Then the design engineer has all of the information he needs before he starts to work on the problem. The apps engineer is quite valuable when he gets all the facts lined up for the experts. Of course, most of the time, the apps engineer gets the facts and solves the problem by himself – he is the first-line expert.

What other things do apps engineers do? They design and evaluate circuits. They write and rewrite data sheets and applications notes. They teach other people by giving seminars and writing magazine articles. They communicate with every kind of user, from the grouchiest to the nicest, from the laid-back to the desperate ones. Their customers include op-amp experts, and also expert chemists who need a little advice about how to interface simple op-amp circuits to their systems. They hold the customer's hand. They won't let him fail.

Apps engineers act as a psychologist, and sometimes as a psychiatrist – they cajole and debate, and they know how to convince people to do things. They also breadboard things. And they run computers. They simulate things. They interpret ideas and data and people's wishes.

Do they get rich and famous? Usually not. Most of the time, they get (at best) begrudging thanks from the customer who did not like to be told that he needs a heat sink to keep his 20-W regulator from getting hot...or from the IC design engineer who is mad that his project is delayed because the apps engineer talked him into redesigning his output stage to add a necessary feature.

On top of everything else, the apps engineer has the thankless job of deflecting and absorbing a thousand complaints. Like an offensive lineman in the National Football League, the best he can say is that he didn't let the quarterback get sacked today, despite the opposition's best moves. Maybe he even has the chance to make a brilliant play. But most of the time, people just beat on him, as if they were trying to wear him down. They ask every kind of picky, niggling, quibbling question. They bring his sanity into doubt. Sometimes they make his day less than fun. Sigh.

Apps engineers don't just get steamrollered. Sometimes they get nibbled to death by ducks. They may even get ulcers. But usually they have a personality that lets them survive these stresses. After all, just because we put all of the info in the data sheet – does that mean that people READ That Fine Data Sheet? If all else fails, call the Apps Engineer? If all else fails, read the data sheet? Never happen!!

I recall one friend, Jim, who had been an apps engineer for many years, and he gradually decided that he was not in a mood to talk to customers on the phone. One day his phone was ringing and he was sitting at his desk trying to ignore it, when his boss walked in. After a few more rings, the boss said, "Jim, do you know who is on that phone?" Jim replied that he did not. The boss said, "Jim, the guy who is calling you on that phone, is *me*". And he went on to explain why an apps engineer really *has to* answer the phones. Jim was able to talk his boss into not firing him outright, but he was given a month to find a job he could agree with.

There's still one last thing that apps people do, and I think it's the most valuable: They listen to people tell them what they "need" and what they "want." Then they try to figure out what the customer *really needs* to make him happy. That may be *quite* different from what the customer *says*.

Sometimes the customer is unrealistic. Sometimes the apps guy is "lucky." Sometimes there's no brilliant or easy answer. But when I was doing a lot of apps work, I considered it my most valuable privilege to hear 19 people ask "simple" or "trivial" or "nasty" questions, and to answer them the best I could, just so I could hear *one* customer ask a REALLY GOOD question.

Sometimes the question points out a deficiency in a data sheet, leading to an improved data sheet, so every user gets the advantage. Sometimes it leads to an applications note, or a magazine article. Other times it leads directly to a new product. Other times it leads to a debate, or an argument with your boss, or a screaming contest. Out of that argument often comes some better way to do something. But you never can tell which caller will be asking the really valuable question. Sometimes it's the op-amp expert—and sometimes it's the chemist.

My boss will probably be pleased to hear that the amount of time I'm "wasting" on apps engineering is less than a couple hours a week. But when someone asks me to put on my Applications Engineering hat, the calls I get are really some of the most interesting and valuable ones. That time isn't "wasted" at all.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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And now, here's a comment from Kerry Lacanette, Applications Engineer for Data Acquisition Circuits at NSC:

Bob, I don't think the customers are as bad as a reader might infer from your discussion. I can think of lots of those annoying "duck" calls in which a series of customers would ask "why don't you build a...?", or, "Do you have an ...IC with a pin that does...?" or some other question that we *thought* we had spelled out clearly in the data sheet. While we may have been annoyed by some of these calls at the time, or we carefully explained to the customer why they couldn't have what they wanted, these customers were really voting – voting for features, products, and better data sheets. We have occasionally counted these votes, and brought out better products because of them.

"Nibbled to death by ducks?" Yeah, I feel that way on a bad day. But would I prefer to take only the "good," "intelligent," or "challenging" questions? Nope. – Kerry.

Kerry, I agree with you completely! You have helped me complete what I wanted to say. Another way to look at it may be that just because a question is "dumb," it doesn't mean the "answer" is dumb. The answer may be challenging or complicated or valuable – and vice versa. Thanks for your comments.—RAP

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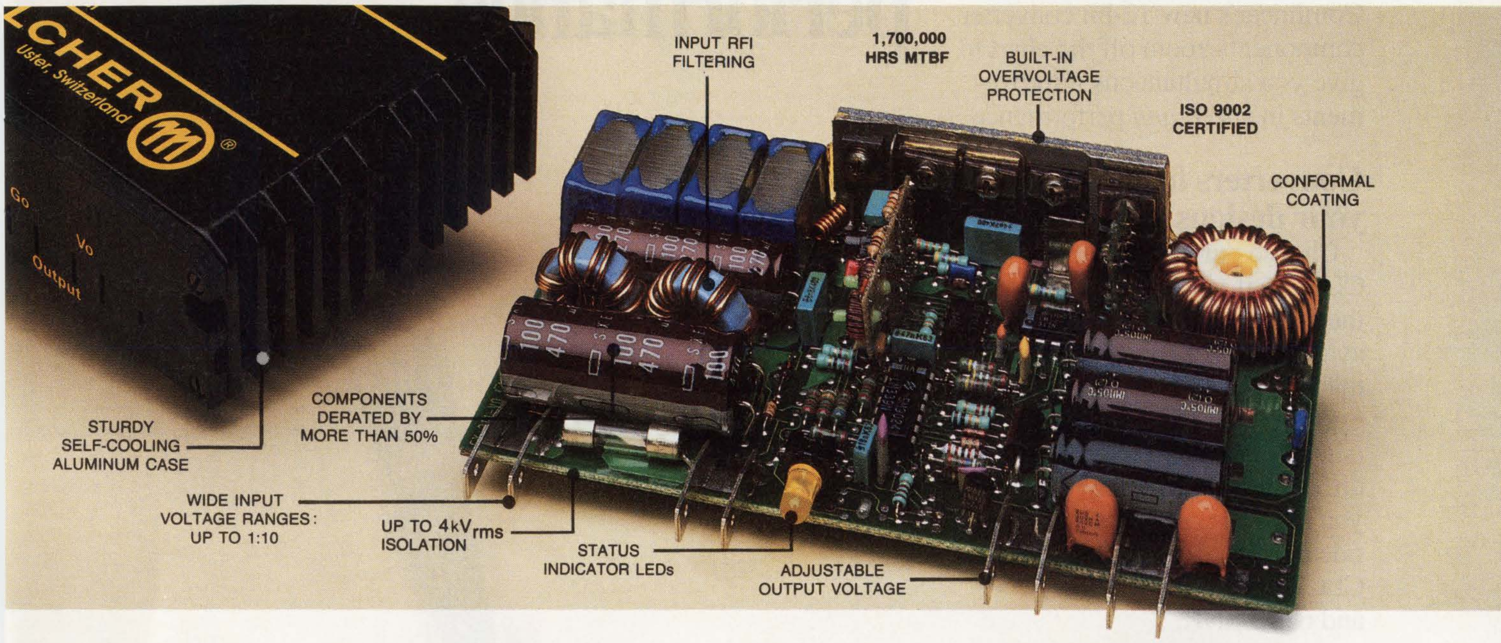

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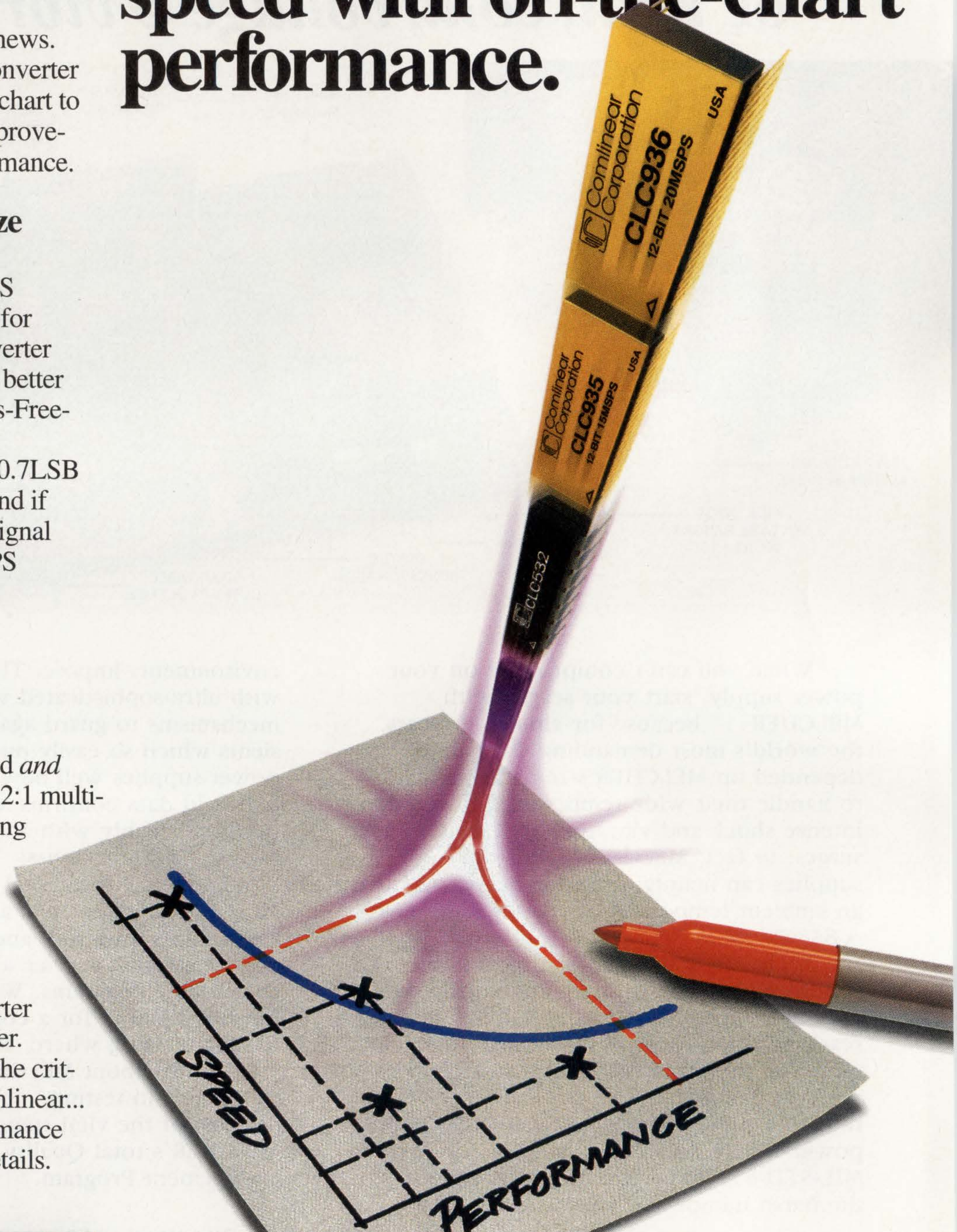

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Digital technology simplifies spectrum analyzer operation

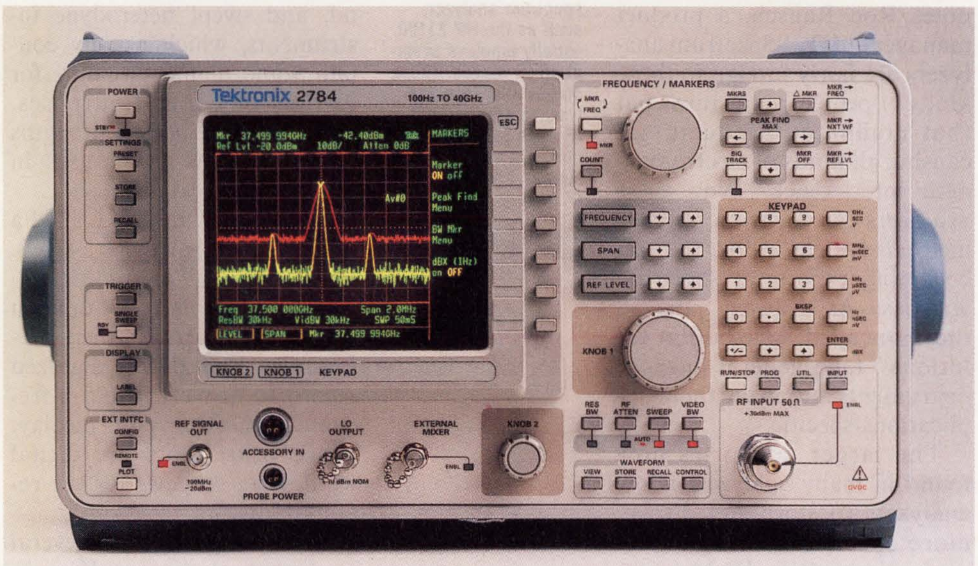
Microprocessors take over some of the drudgery in spectrum measurement.

BY JOHN NOVELLINO

Spectrum analyzers are somewhat esoteric instruments. The frequency domain still holds some mystery for many designers, especially at RF levels. But increasing use of digital technology in spectrum analyzers is making them easier to use, as well as smaller and lighter. The improvements come at an opportune time, as more digital designers become involved in spectrum analysis to improve their systems' electromagnetic compatibility.

The trend toward more digital capability in spectrum analyzers mirrors the increasing use of microprocessors and storage features in test instruments in general. At first, microprocessors were used for control functions. For instance, a microprocessor would adjust the sweep time automatically when the operator changed the resolution bandwidth. But now the devices are providing more automation in measurement functions as well as instrument control, the ability to process and manipulate results, and an improved ability to compare test spectra with stored spectra.

An example is the commonly needed carrier-to-noise measurement. With older analyzers, operators would have to look at the spectrum, compare the carrier signal to the noise signal, and determine how much of the displayed noise is actually coming from the system under test rather than the instrument. The process required several corrections in the noise spectrum. Newer spectrum analyzers automate this measurement.

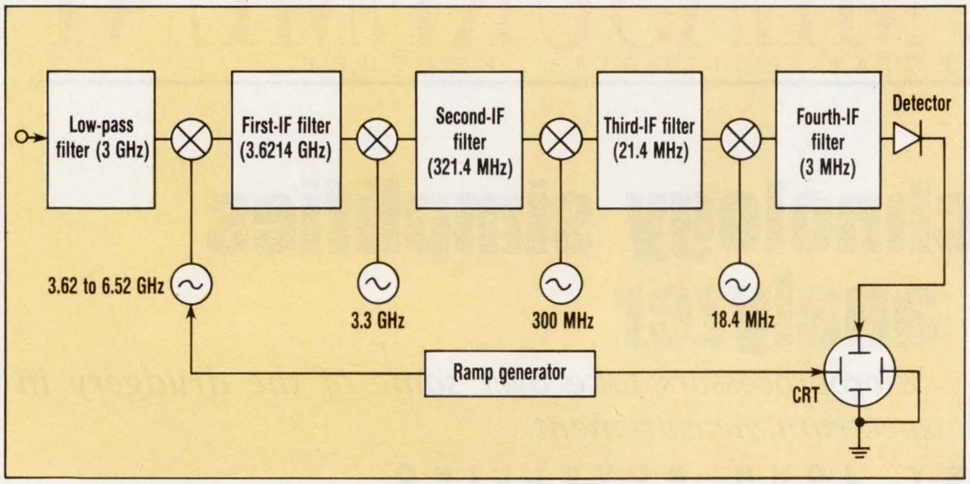


"That's just one example," say Jerry Harris, a spectrum analyzer marketing manager at Tektronix. "There are a number of spectral calculations like that available today. That's one outgrowth of the increased use of digital technology."

Whole test routines can even be automated. Operators could always automate procedures using an external controller and the IEEE-488 port that comes standard, or as an option, on many analyzers. But now users can buy applications programs that run on storage media and controllers built into a spectrum analyzer.

Seven such application programs, or "personalities," are available so far from Hewlett-Packard, who supplies them on credit-card-size memory cards. One personality automates a series of tests that ensure that a cable-TV system meets FCC specifications. Other personalities perform electromagnetic compatibility (EMC) tests. These latter programs should be particularly helpful to designers who are not used to making RF measurements but must get involved with EMC criteria to keep their products legal.

"Actually, most EMC testing



A swept heterodyne spectrum analyzer, such as the HP 71100, usually employs several mixer stages. These stages allow the analyzer to get the final IF down to a level that makes it easy to design a very sharp final IF filter.

is done by digital engineers," notes Ron Rausch, a product manager at HP. "Spectrum analyzers are fairly foreign to those kinds of people, yet it turns out that computer products are causing all kinds of electromagnetic interference." Now these engineers can focus on improving their designs, rather than on becoming experts at spectrum analysis. As Rausch puts it, these so-called "one-button solutions" take general-purpose instruments and make them applications-specific.

The larger memories now found in many analyzers allow analyzers to store and display more spectra, making signal comparison easier. Harris notes that the Tektronix 2712 can display four digitally generated spectra at once. Memories are also used to retain several instrument setups for future re-use.

Although spectrum analyzers are becoming easier to use, they're still complex instruments. Operators should know something about how they work to fully understand their specifications and limitations. In particular, dynamic range, a specification that can be critical in many applications, can be difficult to interpret without some knowledge of the spectrum analyzer's architecture.

There are two basic types of spectrum analyzers: real-time fast-Fourier-transform (FFT) analyzers, which are fully digital, and swept heterodyne instruments, which usually contain some digital circuitry for display or control purposes. Each type has its own strengths and limitations and is used in different applications.

In an FFT analyzer (called a dynamic signal analyzer by HP), the input signal is immediately sampled to create a time-domain record. A processor then performs an FFT on the digitized record to convert it into a frequency spectrum for display. These instruments use digital windowing schemes for the required filtering.

FFT analyzers offer several important advantages. Because they're real-time instruments, they can capture one-shot phenomena, like glitches and transient responses—phenomena that swept heterodyne units cannot capture. Second, they're good at low frequencies. FFT analyzers essentially work down to dc and offer sub-millihertz bandwidth resolutions.

But FFT analyzers have their limits. The top frequency of most instruments is restricted to 100 or 200 kHz, a lid imposed primarily by the time it takes to compute the FFT. An exception is the Tek 3052, a sophisticated (and expensive) instrument that provides real-time spectra at input bandwidths to 2 MHz *(see chart, p. 112)*. Sensitivity and dynamic range are also limited, compared with swept heterodyne analyzers.

The architecture of a swept heterodyne analyzer looks similar to that of a radio receiver (*see the figure*). An input signal is mixed with a local-oscillator (LO) signal to get the desired intermediate frequency (IF). A lowpass filter ensures that only the desired band of input signals will create the selected IF. The down-converted signal is detected and used to drive the CRT's vertical plates. A ramp generator supplies the sweep signal for the CRT's horizontal plates.

In most analyzers, the detected signal is digitized before being sent to the display circuitry. However, in some applications—such as broadcasting, television, or pulsed-RF analysis—only the full gray scale provided by an analog display can best reveal certain modulation characteristics.

An analyzer typically uses several mixer stages to get the final IF low-enough to make it easier to design a sharp final IF filter. This final filter determines the resolution bandwidth, and users must be able to select a narrow bandwidth if a low noise floor, and a wide dynamic range, are needed. On the other hand, wide-resolution bandwidths must be available for users who must examine the spectra that make up narrow-width, and high-bandwidth, pulses.

This basic knowledge of a typical spectrum analyzer's architecture will help users understand some of the complexities and inconsistencies in the dynamic-range specification. There are several definitions of dynamic range in spectrum analysis, and even within those definitions measurement techniques may vary. No consensus exists among manufacturers on which type of dynamic range to quote in specification charts. Users whose applications may strain dynamic-range limits must learn how a specific

PROCESSORS SIMPLIFY SPECTRUM ANALYZERS

instrument was specified.

One type of dynamic range is display dynamic range, which is the greatest range of signals, from the highest to the lowest amplitude, that can be seen on the screen simultaneously. Generally, screens are divided into eight or 10 divisions with 10 dB/div. The limit on the figure is the display's logarithmic amplifier. This can be a fairly conservative way to specify dynamic range, with the instrument actually able to measure a wider range than it can display.

This contradiction needn't be a problem, notes HP's Rausch. To measure the second, off-screen signal, users only have to change the reference level, which is calibrated so it won't affect the measurement. "You can't display both signals at the same time," he says. "But most people don't care about that. They care about how far below one signal the other one is, and they can see that."

Another figure users may see is the measurement range or total measurement range. This is merely the difference between the largest signal a user can put into the analyzer and the smallest signal that the unit can measure. The former is determined by the burn-out levels of the input attenuator and mixer. The analyzer's noise floor is the latter level.

The measurement range's usefulness is limited. The highest and lowest signals cannot be present at the input at the same time, because different attenuation settings would be needed. And measuring two signals at the input simultaneously is what dynamic range is all about.

Finally, there's a general classification called distortion-free dynamic range that actually can involve several types of measurements. "This is where things get a little hairy," says Tek's Harris. "This is probably where you have a lot of variance between suppliers—that is, in how it's measured."

One form of distortion-free range uses the 1-dB compression point. The compression is caused by overdriving the mixer until the relation between the output and input level is no longer linear. One way to measure this figure is two run two signals into the analyzer and increase the larger-signal's level until the displayed level of the signal stops increasing and actually drops by 1 dB. But you can get a larger range by waiting until the displayed level of the smaller signal drops by 1 dB.

The other types of distortion-free dynamic range measure how well the analyzer can accept input signals without creating its own harmonic distortion and third-order intermodulation distortion (IMD). Spectrum analyzers are often used to measure both of these factors, so the analyzer's distortion must be minimal.

The key to finding the right spectrum analyzer is asking a few questions, both about the applications in which it will be used and about how the manufacturer specified the dynamic range. "Know something about your signal levels," says Rausch. "What's the maximum signal you're putting in and how does that relate to the minimum signal you want to measure at the same time?" Most manufacturers provide the details of how dynamic range is specified. Users need only look for them in the specification charts.

According to Harris. "If you don't have applications that demand every last dB of dynamic range, it may not be an issue." Many applications require only the first 70 dB or less of dynamic range, and most manufacturers supply that level with no problem, he notes.

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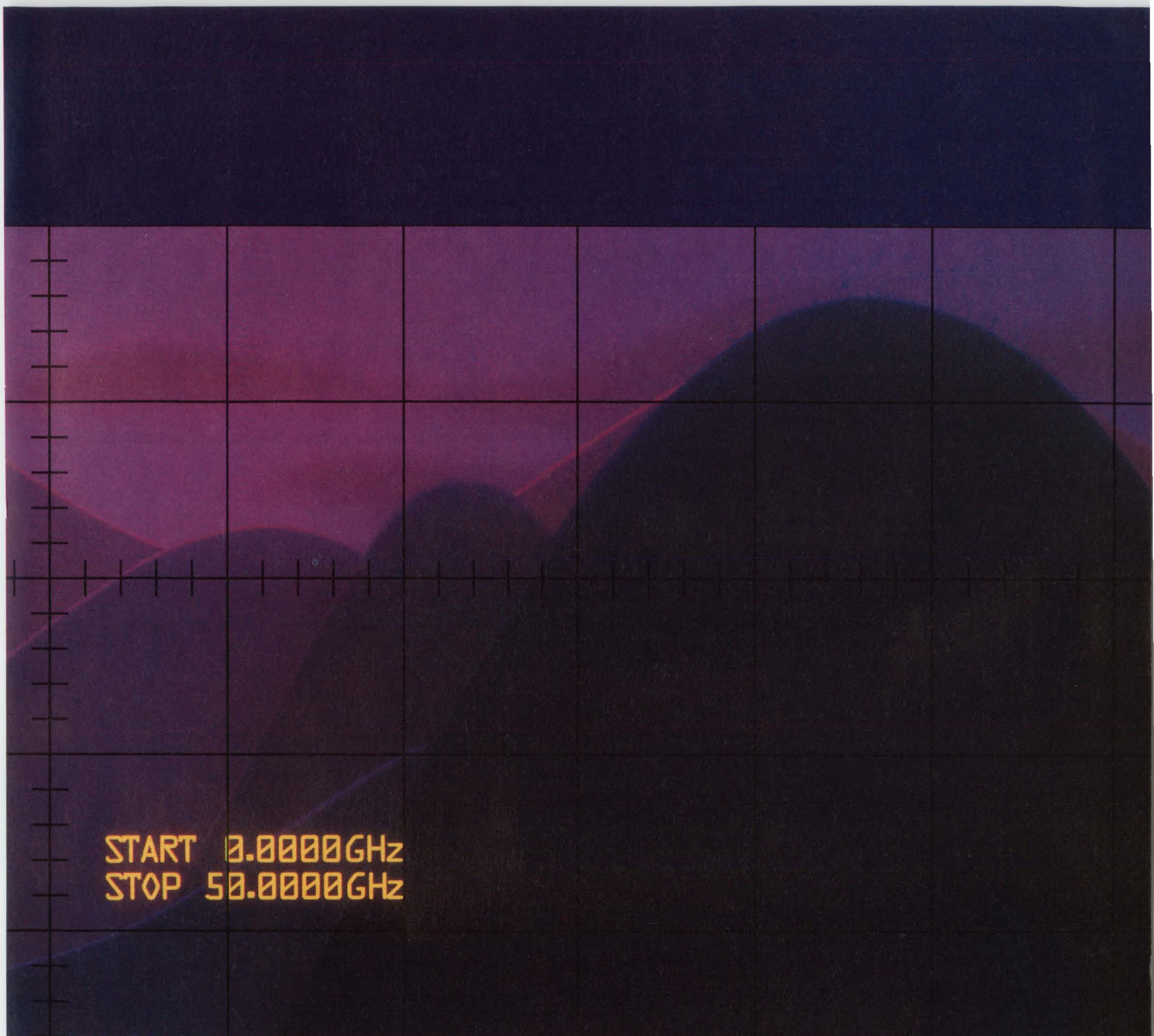

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Accelerate RF mixer measurements

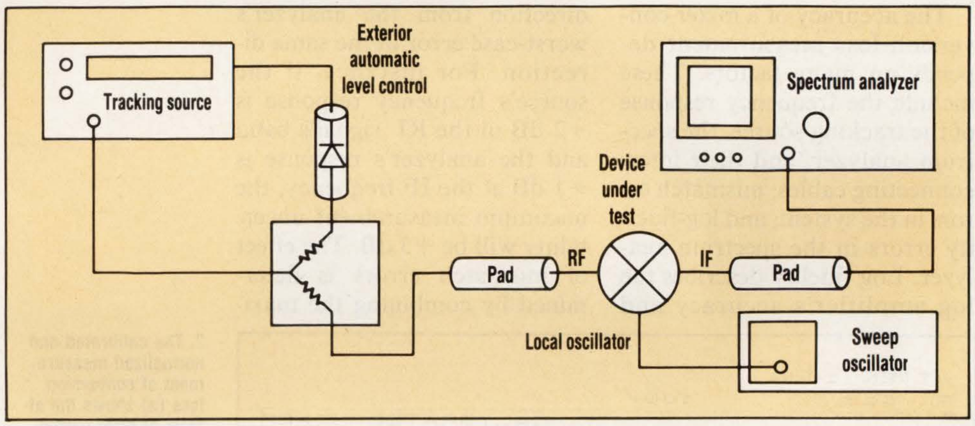
Combining a spectrum analyzer and tracking source makes mixer characterization an easier task.

BY TOM JERSE and WILL CRAMER
Hewlett-Packard Co., Signal Analysis Div., 1212 Valley House Dr., Rohnert Park, CA 94928; (707) 794-1212.

Mixers are ubiquitous. They are critical components in the realization of a wide range of radio-frequency (RF) and microwave systems. However, to determine a mixer's suitability for a particular application, the designer must measure several key parameters, including conversion loss, harmonic distortion, intermodulation distortion (IMD), gain compression, port-to-port isolation, port return loss, and sensitivity to the local oscillator (LO) drive level. Spectrum analyzers are often used to make these measurements. But by adding a tracking source to the test setup, the job can become easier and faster.

This article describes two examples of how a tracking source can simplify mixer characterization. The first procedure measures conversion loss, and the second performs swept third-order intercept measurements. The latter technique, in particular, can dramatically reduce third-order intercept test times.

A tracking source is designed to track the input frequency of a spectrum analyzer, allowing the user to perform frequency-selective stimulus/response testing. The first LO signal from the analyzer is the primary signal that links the frequencies of the two instruments. Locking the source to the analyzer's frequency reference improves tracking stability in narrow bandwidths. Harmonic band information, which is needed to tune the analyzer's output frequency, is made available to the source. A tracking source's ability to track the analyzer over a range of user-defined offset frequencies (typically up to 1 GHz, but possibly much higher) makes it even more useful for evaluating frequency-translation devices.



1. Fixed-IF mixers can be tested quickly using a setup that includes a spectrum analyzer and a tracking source with offset capability to drive the mixer's RF input. A sweep oscillator synchronized to the spectrum analyzer's sweep drives the local oscillator input.

With inherent frequency selectivity, the spectrum analyzer is ideal for measuring the numerous products generated by a mixer. And when narrow resolution bandwidths are chosen on the spectrum analyzer, a large dynamic measurement range becomes available.

The test configuration that will be used to evaluate conversion loss depends on the frequency ranges assigned to the various mixer ports. In some applications, all three ports are tuned to fixed frequencies. More commonly, one port is fixed, and the other two ports span frequency ranges that are offset by the fixed frequency.

The tracking source/spectrum analyzer combination can measure the conversion loss of a mixer with a fixed LO frequency that's lower than the RF frequency. A CW source supplies the mixer's LO input. The frequency offset on the tracking source is set to plus-or-minus the LO frequency, so the spectrum analyzer selects the appropriate conversion product.

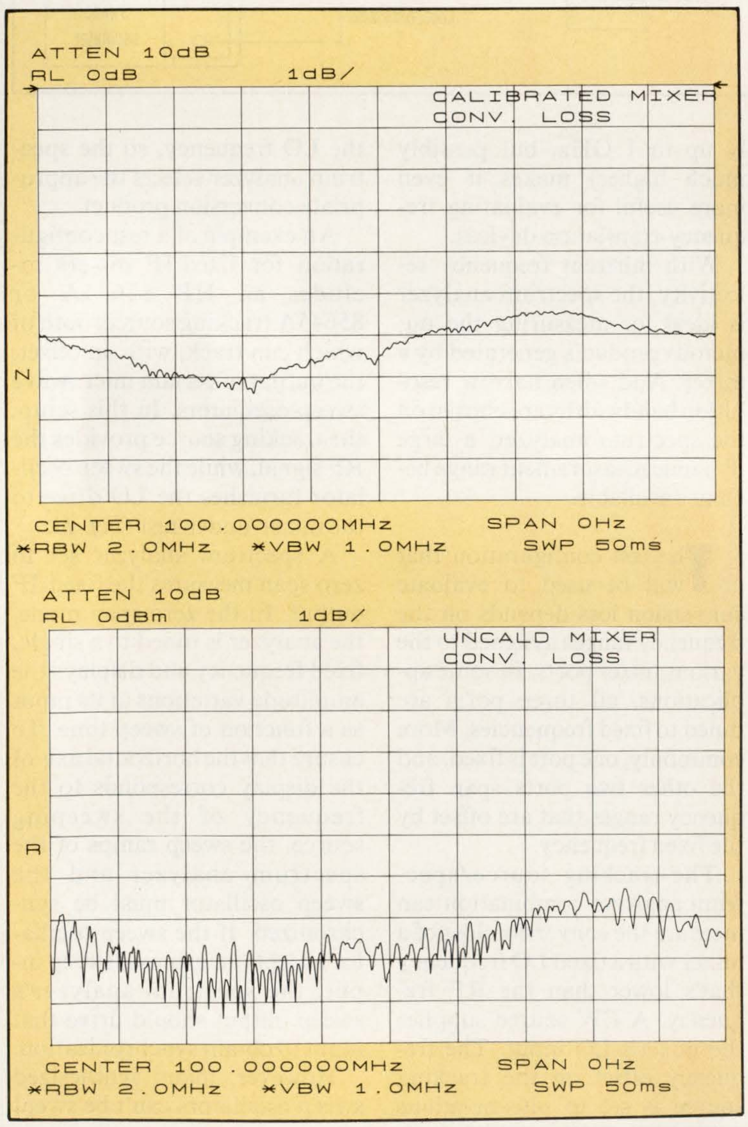
An example of a test configuration for fixed-IF mixers includes an HP 85644A or 85645A tracking source, both of which can track, with an offset, the output of certain microwave sweep oscillators. In this setup, the tracking source provides the RF signal, while the sweep oscillator furnishes the LO drive to the mixer-under-test *(Fig. 1)*.

A spectrum analyzer set to zero span measures the fixed-IF output. In the zero-span mode, the analyzer is tuned to a single, fixed frequency and displays the amplitude variations at its input as a function of sweep time. To ensure that the horizontal axis of the display corresponds to the frequency of the sweeping source, the sweep ramps of the spectrum analyzer and the sweep oscillator must be synchronized. If the sweep oscillator accepts an external sweep input, the spectrum analyzer's sweep output should drive that input to obtain synchronization.

However, many synthesized sweep oscillators can't be swept externally. For these sources, the sweep of the spectrum analyzer measuring the IF response must be triggered by the sweep oscillator. The user must adjust the oscillator's and analyzer's sweep times to be as close as possible to minimize frequency uncertainties.

The accuracy of a mixer conversion-loss measurement depends on many factors. These include the frequency response of the tracking source, the spectrum analyzer, and their interconnecting cables; mismatch errors in the system; and log-fidelity errors in the spectrum analyzer. Log fidelity describes the log amplifier's accuracy and translates to the measured signal's accuracy relative to the reference amplitude at the top of the display.

Designers can determine the maximum measurement uncertainty due to frequency-response errors by subtracting the source's worst-case error in one direction from the analyzer's worst-case error in the same direction. For instance, if the source's frequency response is +2 dB in the RF signal's band and the analyzer's response is +1 dB at the IF frequency, the maximum measurement uncertainty will be +3 dB. The effect of mismatch errors is determined by combining the maximum mismatch error at the mixer's RF and IF ports in a worst-case fashion to reveal the greatest possible uncertainty.



2. The calibrated and normalized measurement of conversion loss (a) shows the effects of error-correction techniques, compared with the uncorrected measurement (b). The fixed IF is at 100 MHz, the local oscillator sweeps from 3 to 6 GHz, and the RF frequency sweeps from 2.9 to 5.9 GHz.

The user can substantially improve the errors caused by source and IF load mismatch by adding attenuators between the tracking source and RF input, and between the IF output and the analyzer. Furthermore, the source match can be improved by external leveling at the interface with the mixer *(Fig. 1, again)*. Log-fidelity errors in the spectrum analyzer must also be included in the measurement-error budget when the IF response falls below the reference level. Although they should be considered, these errors seldom dominate.

Frequency-response errors are more difficult to reduce because the stimulus and the response signals in a mixer are at different frequencies. Simply subtracting the system's response without the device under test from the measured response doesn't eliminate frequency-response errors.

But leveling the source using an external detector improves the amplitude accuracy by moving the leveling point outside the source, close to the measurement point. In addition, this technique removes uncertainties introduced by interconnect cables and adapters. External leveling also improves the source match and, as a result, reduces mismatch errors between the source and the mixer under test.

Moreover, the externally leveled source can help to eliminate amplitude uncertainties in the measurement of the IF response. To do so, the user establishes a reference level at the expected RF input power before making the conversion-loss measurement. That's done by connecting the leveled source to the spectrum analyzer using the cables and adapters that will go between the mixer and the analyz-

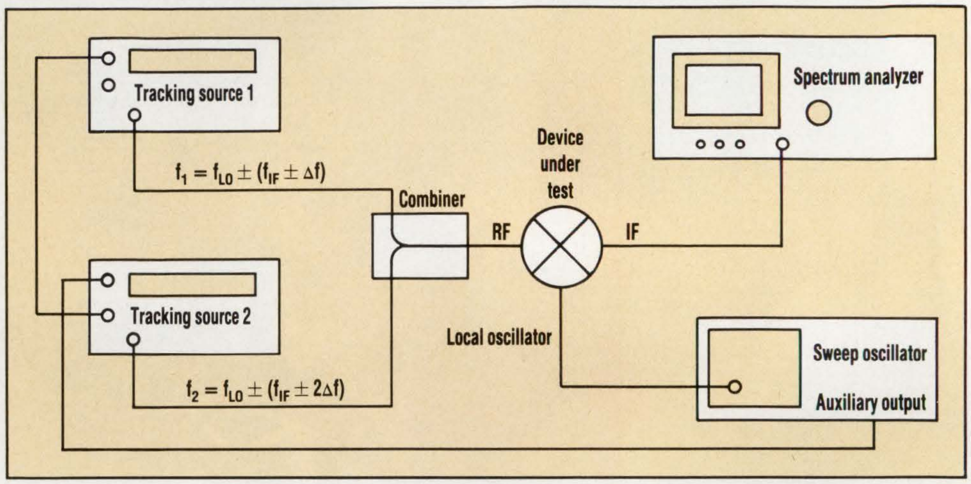
er. This level is stored in the analyzer as the reference. The mixer is then tested with the source leveled at the mixer's RF input. Subtracting the two measurements gives the conversion loss of the mixer without frequency-response errors.

The effectiveness of these error-correction techniques can be seen by comparing a plot of the amplitude of the $f_{LO} - f_{RF}$ product measured without any pads, external leveling, or normalization and a plot of the calibrated and normalized measurement. In the measurement example, the LO frequency is swept from 3 to 6 GHz and the RF frequency is swept from 2.9 to 5.9 GHz, creating a fixed intermediate frequency (IF) of 100 MHz *(Fig. 2)*.

An important mixer characteristic, especially in communications systems, is the device's third-order intermodulation-distortion performance. The problem is that multiple tones applied to the mixer's RF input can intermodulate to produce responses at frequencies that are linear combinations of the input frequencies. For example, if two tones, at f_1 and f_2, are applied to the RF input, the converted IMD products in the IF that fall at $f_{LO} - (2f_1 - f_2)$ and $f_{LO} - (2f_2 - f_1)$ are particularly troublesome. That's because these products appear very close to the fundamental tones and therefore are difficult to filter.

A device's IMD performance is commonly characterized by the third-order intercept (TOI). The amplitudes of the third-order products increase three times faster than the amplitudes of both fundamentals. The TOI, then, is the extrapolated point where, in theory, the amplitude of the fundamentals and the third-order products would be equal. This point is never actually attained because significant gain compression occurs before it's reached.

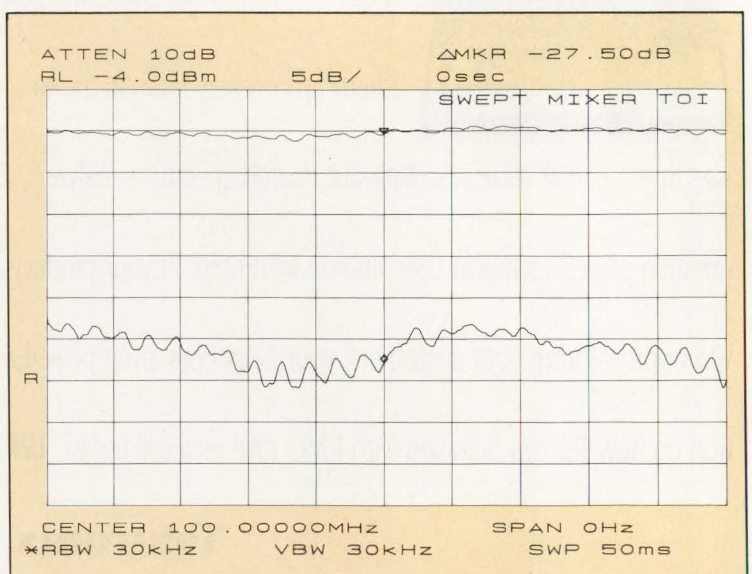
A test system using two tracking sources speeds the wideband testing of third-order IMD *(Fig. 3)*. The spectrum analyzer is tuned to the IF frequency in zero span. A microwave sweeper serves as the host for the tracking sources, which are set to equal power levels.



3. To evaluate a mixer's third-order intermodulation distortion, the setup requires a second tracking source. Both sources are driven by the host sweep oscillator.

If the desired spacing between the tones is Δf, one tracking source is offset either above or below the host's sweeper frequency by $f_{IF} \pm \Delta f$; the other is offset by $f_{IF} \pm 2\Delta f$. When the additive cases are used, the analyzer measures the converted $2f_1 - f_2$ product. When the differences are selected, the analyzer measures the converted $2f_2 - f_1$ product. The spectrum analyzer's resolution bandwidth must be somewhat narrower than Δf in order to resolve an individual product. As is the case with conversion-loss measurements, the sweeps of the spectrum analyzer and the host sweeper must be synchronized to minimize frequency errors.

In addition to dynamic range, two factors limit this test system's ability to measure IMD products: intermodulation between the output stages of the sources and harmonics in the spectra generated by the sources. If required, designers can enhance the measurement's accuracy by increasing the isolation between the sources with



4. The third-order intercept can be calculated from measurements of the amplitude of the converted fundamental product of f_1 (top trace) and the amplitude of the $2f_2 - f_1$ third-order product. To produce the third-order plot, two RF signals, spaced 1 MHz apart, are swept from 3 to 6 GHz.

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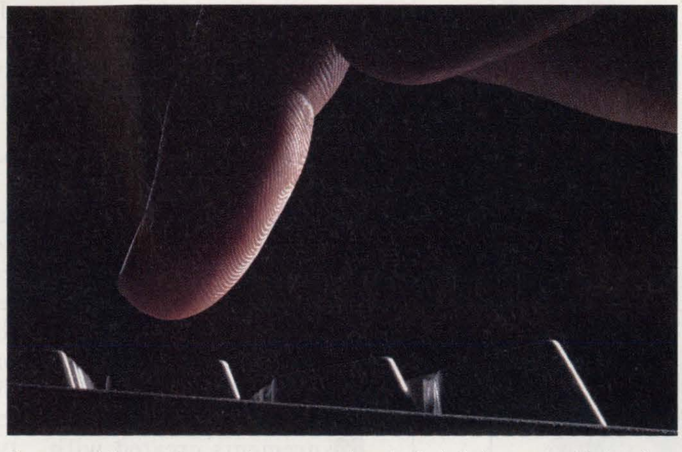

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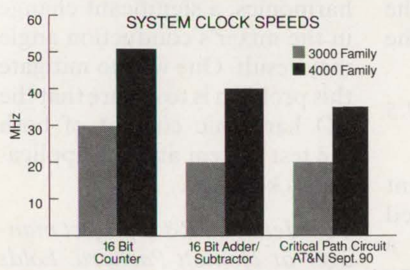

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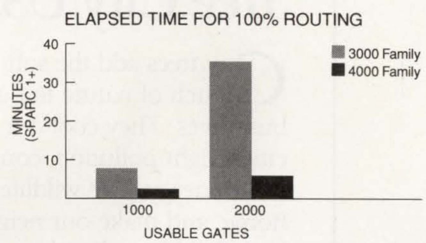

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Filtering may also be needed if the sources produce excessive harmonics. For instance, second-harmonic energy from the first source ($2f_1$) can mix in the device under test with the fundamental of the second source (f_2) to produce a response at $2f_1 - f_2$. The amplitude of this response depends on second-order, not third-order, distortion inside the device because $2f_1$ is present at the input. The need for filtering depends on the harmonic content of the sources as well as the relative level of second- and third-order distortion.

An example plot of measurements created with this technique shows how TOI can be determined *(Fig. 4)*. The first measurement needed is the amplitude of the $2f_2 - f_1$ third-order product produced by a double-balanced mixer as two RF signals (spaced 1 MHz apart) are swept from 3 to 6 GHz. The second measurement is the amplitude of the converted fundamental product of f_1. The equivalent TOI at the mixer's output can be calculated by adding half of the difference between the measurements to the fundamental's amplitude. In the example case:

$$TOI_{output} = -10\text{ dBm} + (27.5\text{ dB}/2) = +3.75\text{ dBm}$$

Previously, this measurement would have been performed with two synthesizers and a lengthy procedure of stepping through and measuring each individual frequency. By using tracking sources with offset capability, however, the entire measurement can be performed in the time it takes a spectrum analyzer to make one sweep.

In addition to the preceding measurements, the combination of a spectrum analyzer and a tracking source with power-sweep capability can help determine other mixer characteristics. Among the measurements that can be made are RF-IF gain compression, the dependence of mixer harmonic distortion on LO drive, and the sensitivity of conversion loss to LO drive level. Used in a stimulus-response mode, the two instruments can measure a mixer's port-to-port isolation or, with the addition of a directional coupler or bridge, port return loss.

Although a tracking source can speed up evaluation of mixer performance, characterizing a mixer with a broadband test system may not adequately predict the device's performance in a particular application. Often, discrepancies are caused by differences in port terminations between the test setup and the actual application, especially at the IF output. For instance, a termination with a reflection coefficient that varies greatly with frequency, such as a filter, can cause substantial performance fluctuations.

The spectral content of the LO drive signal can also influence mixer performance. Harmonics alter the shape of the LO waveform from a perfect sinusoid. Depending on the relative amplitudes and phases of the harmonics, a significant change in the mixer's conduction angle may result. One way to mitigate this problem is to ensure that the LO harmonic content of both the test system and the application is kept low.

Tom Jerse, an R&D project manager at Hewlett-Packard, holds an MSEE from Stanford University and is pursuing a PhD in electromagnetic compatibility.

Will Cramer, who has helped design portable spectrum analyzers for Hewlett-Packard, received an MSEE from the University of Arizona.

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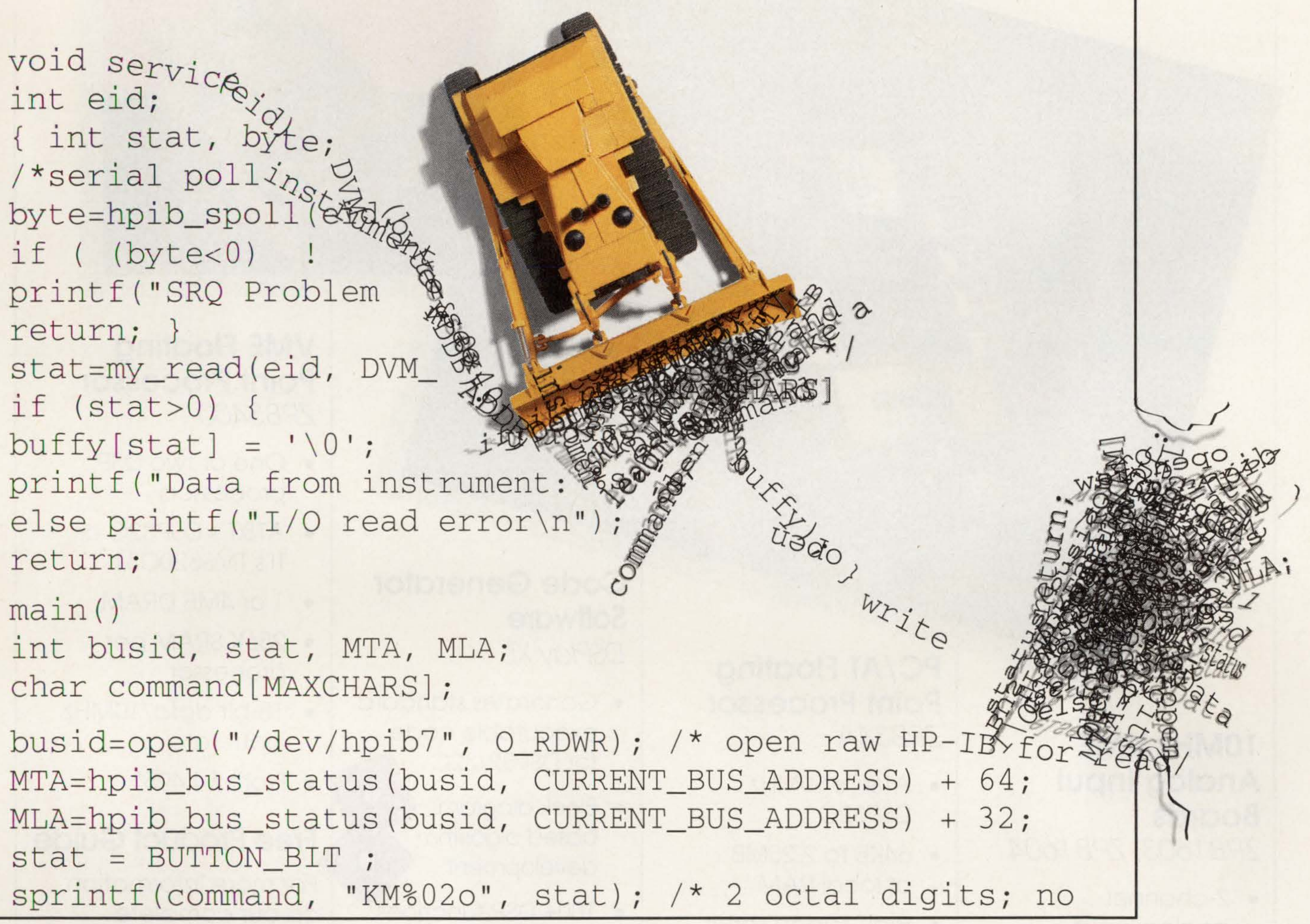

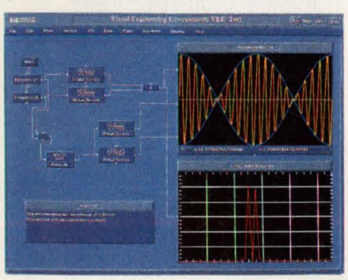

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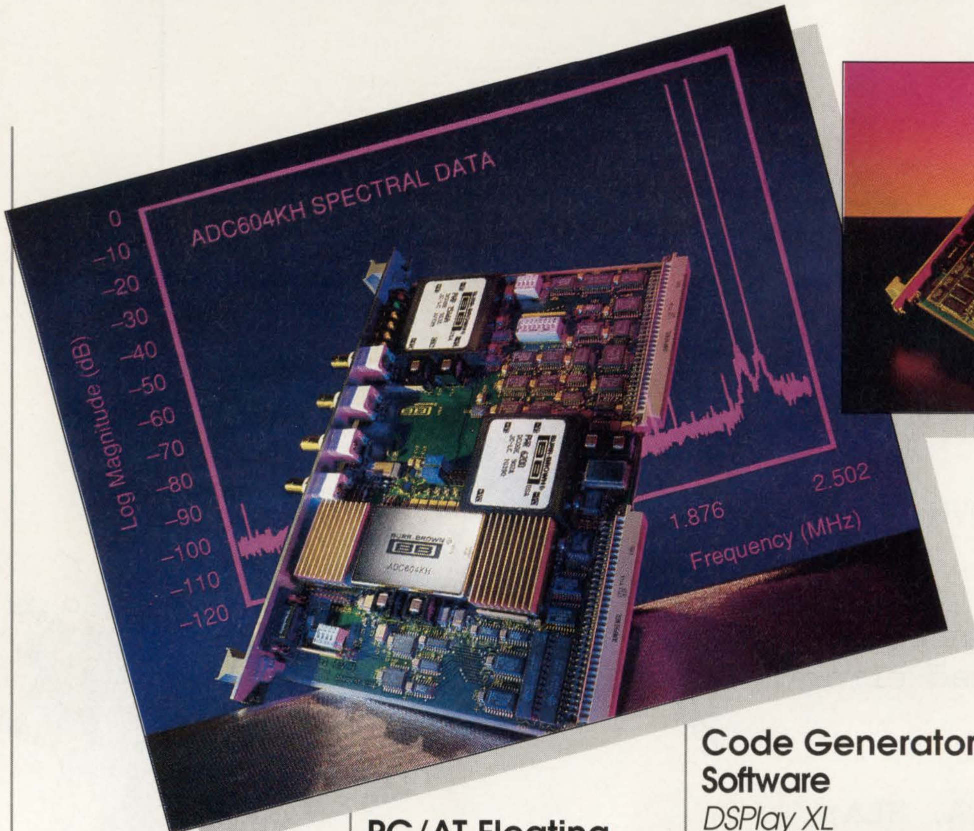

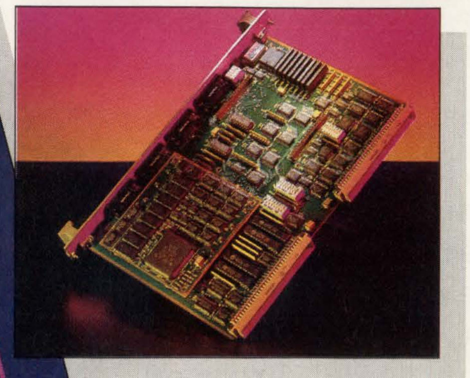

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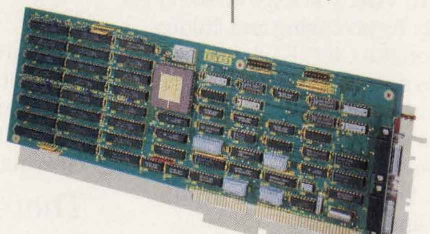

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SPECTRUM ANALYZERS

Manufacturer	Model/ Price	Resolution bandwidth	Frequency Range	Frequency Accuracy	Amplitude Range	Amplitude Accuracy	Dynamic Range	Remarks
Advantest America Inc. 300 Knightsbridge Pkwy. Lincolnshire, IL 60069 (708) 634-2552	R 4131C/ $5995	1 kHz - 1 MHz	10 kHz - 3.6 GHz	±10 MHz	–116 to +20 dBm	±2 dB	70 dB[1]	GPIB, quasipeak detector std.; opt. tracking gen.
	R4131D $6995	1 kHz - 1 MHz	10 kHz - 3.6 GHz	±100 kHz	–116 to +20 dBm	±2 dB	70 dB[1]	Same as R4131C plus AFC.
	TR4132/N/ $8300	10 - 30 MHz	100 Hz - 1 GHz	±10 MHz	–135 to 5 dBμV	±2 dB	70 dB[1]	Built-in tracking generator; battery pack.
	R9211E/ $9200	[2]	6.25 μHz - 100 kHz	[3]	–125 to +30 dBV	[3]	85 dBV	2 channels; 16-bit analog-to-digital converter.
	R9211A/ $10,900	[2]	6.25 μHz - 100 kHz	[3]	–125 to +30 dBV	[3]	85 dBV	2 channels; 16-bit analog-to-digital converter.
	R3261A/ $12,900	30 Hz - 1 MHz	9 kHz - 2.6 GHz	±(3% x span) + [(center freq.) ×(2 × 10^{-8}) +20 Hz]	–130 to +25 dBm	±1 dB	70 dB[1]	Quasipeak detector, 1 Hz frequency counter.
	R9211B/ $13,900	[2]	6.25 μHz - 100 kHz	[3]	–125 to +30 dBV	[3]	85 dBV	2 channels; built-in signal generator, FDD.
	TR4120A/ $16,200	10 Hz - 100 kHz	100 Hz to 30 MHz	±500 kHz	–135 to +40 dBV	±2 dB	60 dB[1]	Built-in tracking gen., analog display.
	R9211C/ $17,900	[2]	6.25 μHz - 100 kHz	[3]	–125 to +30 dBV	[3]	85 dBV	2 channels; FDD; built-in signal generator.
	R3361A/ $18,500	30 Hz - 1 MHz	9 kHz - 2.6 GHz	Same as R3261A	–130 to +25 dBm	±1 dB	70 dB[1]	Built-in tracking generator, quasipeak detector.
	R3261B/ $20,100	30 Hz - 1 MHz	9 kHz - 3.6 GHz	Same as R3261A	–130 to +25 dBm	±1 dB	70 dB[1]	Built-in quasipeak detector, 1-Hz counter.
	R3361B/ $25,900	30 Hz - 1 MHz	9 kHz - 3.6 GHz	Same as R3261A	–130 to +25 dBm	±1 dB	70 dB[1]	Built-in tracking generator, frequency counter, quasipeak detector.
	R3265/ $27,000	10 Hz - 3 MHz	100 Hz - 8 GHz	Same as R3261A	–140 to +30 dBm	±3 dB	75 dBc[1]	GPIB std.; frequency counter; 8 markers.
	R3271/ $32,000	10 Hz - 3 MHz	100 Hz - 26.5 GHz	±1% × span +(2 × 10^{-8}) + 1 Hz	–135 to 30 dBm	±4 dB	75 dBc[1]	GPIB std.; frequency counter; 8 markers.
	TR4171/ $33,000	3 Hz - 100 kHz	10 Hz - 120 MHz	Same as R3271	–135 to +30 dBm	±1.5 dB	80 dBc[1]	GPIB std.; built-in tracking generator.
	TR4173/ $55,900	10 Hz - 1 MHz	100 Hz - 5 GHz	±(readout × 5 × 10^{-9}) ±(1% × span + 20 Hz)	–135 dto +25 dBm	±1.5 dB	80 dBc[1]	Built-in tracking generator; quasipeak measurement.
Analogic 8 Centennial Dr. Peabody, MA 01961 (508) 977-3000	6100/ $19,500	260 μHz - 500 kHz	to 125 MHz	0.01%	–12.5 mV to +10 V	1%	54 dB	Multifunction instrument with 660-1 spectrum analyzer plug-in module.
Anritsu America Inc. 15 Thornton Rd. Oakland, NJ 07436 (201) 337-1111	MS610B/ $6995	1kHz-1 MHz (3 dB) 9 kHz - 120 kHz (6 dB)	10 kHz-2 GHz	±5%	–115 to +20 dBm	±4.5 dB	80 dB[4]	Analog spectrum analyzer suitable for EMI testing.
	MS2601B/ $11,990	30 Hz - 1 MHz	9 kHz - 2.2 GHz	±2%	–130 to +20 dBm	±1 dB	75 dB[4]	100 Hz - 2.2 GHz opt.; built-in quasipeak det.
	MS710C/ $24,690	100 Hz - 3 MHz	10 kHz - 23 GHz	±5%	–115 to +30 dBm	±5 dB	70 dB[5]	Internal preselector; signal search functions.
	MS2802A/ $49,000	10 Hz - 3MHz	100 Hz - 32 GHz	±2.5%	–135 to +30 dBm	±1.1 dB	100 dB[5]	Includes personal menu card and personal test automation.
B&K-Precision Div. Maxtec International Corp. 6470 W. Cortland St. Chicago, IL 60635 (312) 889-1448	2610/ $2995	10 kHz	1-1000 MHz	±3 MHz	15 to 123 dBμV	±2 dB	70 dB	Portable; includes ac power, battery, internal charger.

(see p. 112 for key)
(continued on p. 110)

SPECTRUM ANALYZERS

Manufacturer	Model/ Price	Resolution bandwidth	Frequency Range	Frequency Accuracy	Amplitude Range	Amplitude Accuracy	Dynamic Range	Remarks
Hewlett-Packard Co. 19310 Pruneridge Ave. Cupertino, CA 95014 (800) 752-0900	HP 3560A/ $7800	625 μHz-1440 Hz	62.5 μHz-40 kHz	±8 Hz	5 mV-5 V	±0.5 dB	60 dB[4]	Portable, 7 lb, battery-powered.
	HP 8590B/ $9985	1 kHz-3MHz	9 kHz-1.8 GHZ	±5 MHz (@ 1GHz)	–115 to +30 dB	±2 dB	80 dB[4]	Opt. built-in tracking generator.
	HP 8591A/ $12,825	1 kHz - 3MHz	9 kHz - 1.8 GHz	±2 kHz (@1 GHz)	–115 to + 30 dB	±2 dB	80 dB[4]	Opt. built-in tracking generator.
	HP 35665A/ $13,250	322 μHz - 920 Hz	122 μHz - 102.4 kHz	±3 Hz	3.99 mV - 31.7 V	±0.5 dB	78 dB[4]	Opt.: computed-order tracking, arbitrary source.
	HP 3561A/ $14,000	23 μHz - 900 Hz	125 μHz - 100 kHz	±3 Hz	3 mV - 22.4 V	±0.15 dB	85 dB[4]	High-performance FFT and transient-capture analysis.
	HP 8594A/ $14,995	1 kHz - 3 MHz	9 kHz - 2.9 GHz	±2 kHz (@1 GHz)	–112 to +30 dB	±3 dB	80 dB[4]	Opt. buillt-in tracking generator.
	HP 3588A/ $19,900	0.004 Hz - 17 kHz	10 Hz - 150 MHz	±150 Hz	–140 to +26 dBm	±0.3 dB	80 dB[4]	Built-in tracking generator; 3.5-in. floppy drive. 3589A ($21,750) incl. network analysis.
	HP 8595A/ $21,535	1 kHz - 3 MHz	9 kHz - 6.5 GHz	±2 kHz (@ 1 GHz)	–114 to +30 dB	3 dB	80 dB[4]	Opt. built-in tracking generator.
	HP 3562A/ $21,600	12 μHz - 450 Hz	64 μHz - 100 kHz	±4 Hz	3 mV - 22.4 V	±0.15 dB	85 dB[4]	High-performance analog spectrum, network, transient analysis.
	HP 8592B/ $21,650	1 kHz - 3 MHz	9 kHz - 22 GHz	±10 MHz (@10 GHz)	–114 to +30 dB	±3 dB	71 dB[4]	Opt.: built-in tracking generator, 25 GHz.
	HP 3567A/ $21,700	122 μHz - 4096 Hz	122 μHz - 102.4 kHz	±0.8 Hz	1.26 mV - 39.8 mV	±0.15 dB	80 dB[4]	2-16-channel modular, PC-based system.
	HP 8560A/ $25,500	10 Hz - 2 MHz	50 Hz - 2.9 GHz	±2 kHz (@ 1 GHz)	–130 to +30 dBm	±2 dB	90 dB[4]	Opt. built-in tracking generator.
	HP 3566A/ $26,000	122 μHz - 512 Hz	122 μHz - 12.8 kHz	±0.1 Hz	5 mV - 10 V	±0.15 dB	72 dB[4]	8- or 16-channel modular, PC-based system.
	HP 3563A/ $26,900	12 μHz - 450 Hz	64 μHz - 100 kHz	±4 Hz	3 mV - 22.4 V	±0.15 dB	85 dB[4]	Same as HP 3562A plus digital input and Z-domain analysis.
	HP 8593A/ $27,500	1 kHz - 3 MHz	9 kHz - 22 GHz	±20 kHz (@ 10 GHz)	–114 to +30 dB	±3 dB	71 dB[4]	Opt.: built-in track generator, 26.5 GHz.
	HP 3585B/ $27,700	3 Hz - 30 kHz	20 Hz - 40.1 MHz	±40 Hz	–137 to +30 dBm	±0.4 dB	86 dB[4]	Built-in tracking generator; sweep gating opt.
	HP 8567A/ $30,715	1 kHz - 3 MHz	10 kHz - 1.5 GHz	±5 kHz (@ 1 GHz)	–115 to +30 dBm	±2 dB	83 dB[4]	Opt. tracking generator.
	HP 8561B/ $31,000	10 Hz - 2 MHz	50 Hz - 6.5 GHz	±2 kHz (@ 1 GHz)	–131 to + 30 dBm	±2 dB	90 dB[4]	Meets MIL-SPEC.; opt. tracking generator.
	HP 8563A/ $35,600	10 Hz - 2 MHz	9 kHz - 26.5 GHz	±1 kHz (@ 10 GHz)	–131 to +30 dBm	±3 dB	85 dB[4]	Meets MIL-SPEC.; opt. tracking generator.
	HP 8562B $36,500	100 Hz - 2 MHz	9 kHz - 22 GHz	±20 kHz (@ 10 GHz)	–121 to +30 dBm	±3 dB	78 dB[4]	Meets MIL-SPEC.; opt. tracking generator.
	HP 8568B/ $40,000	10 Hz - 3 MHz	100 Hz - 1.5 GHz	±260 Hz (@ 1 GHz)	–135 to +30 dBm	±2 dB	97 dB[4]	
	HP 71100C/ $49,000	10 Hz - 300 kHz (3 MHz opt.)	100 Hz - 2.9 GHz	±110 Hz (@ 1 GHz)	–134 to +30 dB	±1.5 dB (0.9 dB opt.)	92 dB[4]	Additional functional modules available.
	HP 71200C/ $55,400	10 Hz - 300 kHz (3 MHz opt.)	50 kHz - 22 GHz	±1 kHz (@10 GHz)	–130 to +30 dB	±2 dB (0.9 dB opt.)	88 dB[4]	Additional functional modules available.
	HP 8566B/ $66,750	10 Hz - 3 MHz	100 Hz - 22 GHz	±2.5 kHz (@10 GHz)	–134 to +30 dB	±2 dB	86 dB[4]	Range to 325 GHz with external mixers.

(see p. 112 for key)
(continued on p. 111)

SPECTRUM ANALYZERS

Manufacturer	Model/ Price	Resolution bandwidth	Frequency		Amplitude		Dynamic Range	Remarks
			Range	Accuracy	Range	Accuracy		
Hewlett-Packard Co. 19310 Pruneridge Ave. Cupertino, CA 95014 (800) 752-0900	HP 71209A/ $67,700	10 Hz - 3 MHz	100 Hz - 26.5 GHz	±1 kHz (@10 GHz)	−138 to +30 dB	±2.5 dB (0.9 dB opt.)	96 dB[4]	Additional functional modules available.
	HP 71210C/ $78,800	10 Hz - 3 MHz	100 Hz to 22 GHz	±1 kHz (@ 10 GHz)	−139 to +30 dB	±2.5 dB (0.9 dB opt.)	98 dB[4]	Additional functional modules available.
IFR Systems Inc. 10200 W. York St. Wichita, KS 67215-8935 (316) 522-4981	A-7550/ $7195	300 Hz - 3 MHz	10 kHz - 1 GHz	±25 ppm	−120 to +30 dBm	±2 dB	70 dB	Portable; built-in battery, tracking generator.
	A-8000/ $11,595	300 Hz - 3 MHz	10 kHz - 2.5 GHz	±0.5 ppm	−120 to +30 dBm	±2 dB	70 dB	Portable; built-in battery, tracking generator.
	AN 930/ $19,495	3 Hz - 25 MHz	9 kHz - 22 GHz	±0.2 ppm (±0.002 ppm opt.)	−120 to +30 dBm	±1 dB	80 dB	Portable; built-in battery, tracking generator.
Marconi Instruments Inc. 3 Pearl Ct. Allendale, NJ 07401 (201) 934-9050	2382/ $29,950	3 Hz - 1 MHz	100 Hz - 400 MHz	7	−145 to +27 dBm	±1 dB	100 dB[6]	Tracking generator, GPIB std. RGB output opt.
	2383/ $46,000	3 Hz - 1 MHz	100 Hz - 4.2 GHz	7	−131 to +27 dBm	±1.5 dB	100 dB[6]	Same as 2382.
	2386/ $60,000	3 Hz - 1 MHz	100 Hz - 26.5 GHz	7	−111 to +27 dBm	±3.5 dB	100 dB[6]	Same as 2382.
Protek P.O. Box 59 Norwood, NJ 07648 (201) 767-7242	P-7802/ $3500	1 MHz	1-1000 MHz	±1%	150-129 dBμ	±2 dB	70 dB	
Rohde & Schwarz Inc. 4425 Nicole Dr. Lanham, MD 20706 (301) 459-8800	FSA/ $44,900	6 Hz - 3 MHz	100 Hz - 1.8 GHz	8	−145 to +30 dBm	±1 dB	100 dB	Color display; built-in am/fm demodulators.
	FSAS/ $56,200	6Hz - 3 MHz	100 Hz - 1.8 Ghz	8	−145 to +30 dBm	±1 dB	100 dB	Same as FSA, plus built-in tracking generator.
	FSB/ $67,500	6 Hz - 3 MHz	100 Hz - 5 GHz	8	−140 to +30 dBm	±1 dB	100 dB	Color display; built-in am/fm demodulators.
	FSBS/ $79,000	6 Hz - 3 MHz	100 Hz 5 GHz	8	−140 to +30 dBm	±1 dB	100 dB	Same as FSB, plus built-in tracking generator.
	FSAD/ $85,900	6 Hz - 3 MHz	100 Hz - 1.8 GHz	8	−140 to +30 dBm	±1 dB	100 dB	Built-in tracking generator, preselector, preamp.
	FSM/ $89,900	6 Hz - 3 MHz	100 Hz - 26.5 GHz	8	−140 to +30 dBm	±2 dB	100 dB	Fundamentally mixed, low-noise analyzer.
	FSBC/ $94,200	6 Hz - 3 MHz	100 Hz - 5 GHz	8	−140 to +30 dBm	±1 dB	100 dB	Built-in tracking generator, preselector, preamp.
Stanford Research Systems Inc. 1290D Reamwood Ave. Sunnyvale, CA 94089 (408) 774-9040	SR 760/ $4350	476 μHz - 100 kHz	476 μHz - 100 kHz	0.0025% (25 ppm)	−60 to +34 dBV	±0.2 dB	90 dB	Automated analysis functions; 3.5-in. floppy drive.
Tektronix Inc. P.O. Box 1520 Pittsfield, MA 01201 (800) 426-2200	2622/ $6950	0.006 Hz	dc-20 kHz	±0.01%	55 mV to 10 V	0.2 dB	75 dB	PC-interpreted system; 2-ch. portable.
	2630/ $9950	0.003 Hz	dc-20 kHz	±0.01%	55 mV to 10 V	0.2 dB	75 dB	PC-interpreted system; opt. function gen.
	2711/ $8750	3 kHz - 5 MHz	9 kHz - 18 GHz	10 ppm ±5 kHz	−129 to +20 dBm	±1.5 dB	80 dB[5]	Built-in am/fm demodulator.
	2712/ $11,950	300 Hz - 5 MHz	9 kHz - 1.8 GHz	0.5 ppm ±700 Hz	−139 to +20 dBm	±1.5 dB	80 dB[5]	IEEE-488 std.; quasi-peak detector for EMC measurements opt.
	2642A/ $15,900	0.003 Hz - 8 kHz	dc - 200 kHz	±0.01%	14 mV to 10 V	±0.2 dB	90 dB	Includes network and waveform analysis, arbitrary wave generator.
	492GM/ 2754P/ $20,900	1 kHz - 3 MHz	10 kHz - 21 GHz	±30 kHz (@ 1 GHz)	−110 to +30 dBm	±4 dB	80 dB[5]	IEEE-488 std.; built-in frequency countyer. 490 series is portable, ruggedized version.
	4595P/ 2753P/ $22,900	10 Hz - 3 MHz	100 Hz - 1.8 GHz	±20 kHz (@ 2 GHz)	−130 to +30 dBm	±1.5 dB	90 dB[5]	Same as 2754P.

(see p. 112 for key)
(continued on p. 112)

▼ ANALYZER HANDLES 40 GHZ IN COAXIAL CABLE

With preselected coverage to 40 GHz in coaxial cable, the 2784 microwave spectrum analyzer is well-equipped to characterize signal sources and millimeter-wave devices. Full-range sweeps in coax from 100 Hz to 40 GHz also expand the range of optical heterodyning methods that can be used to characterize optical sources. In wave guide, the analyzer offers coverage to 325 GHz, and its calibrated frequency range stretches to 1200 GHz, allowing extended coverage with external mixers.

The 2784 also features direct fundamental mixing to 28 GHz, resolution bandwidths from 3 Hz to 10 MHz, 100-dB display dynamic range, and a built-in microwave counter. Two IEEE-488 interfaces allow the 2784 to be controlled by a host computer while the instrument acts as a secondary controller for other instruments.

Automated signal-processing functions include frequency searches and occupied bandwidth measurements. A combination of dedicated function keys, on-screen menus, and assignable function knobs simplifies setups and measurements. Users can program the assignable function knobs for frequently needed menu items.

A liquid-crystal, color-shutter display highlights critical information in different colors. This includes multiple waveforms, both analog and digital. To ease interpretation of complex displays, a color-mixing feature highlights areas where waveforms cross or overlay each other.

The 2784 microwave spectrum analyzer costs $79,500, and delivery is within eight weeks.

Tektronix Inc.
Test & Measurement Group
P.O. Box 1520
Pittsfield, MA 01202
(800) 426-2200
▶CIRCLE 571

▼ LOW-COST ANALYZER REACHES 1 GHZ

A low-cost spectrum analyzer offers 1-GHz coverage with a 6-in. CRT readout display and with a cursor. The P-7802 displays signals and their harmonics from 1 MHz to 1 GHz with a center-frequency display accuracy of ±1% and resolution of 1 MHz. The unit features a 100-kHz to 100-MHz, 10-step scanning band at 3 dB per band, and a 10-kHz to 1-MHz, 10-step, –3-dB scanning band. Scanning-band accuracy is ±6% for a center frequency below 100 MHz and ±10 for a center frequency above 100 MHz, with a scan speed of approximately 5 ms/div. Dynamic range is 70 dB. Amplitude measuring range is rated at 15 to 129 dBμ, with a CRT range of 15 to 80 dBμ. Panel switches can be set from 80 to 129 dBμ, adjustable in 1-dBμ steps. The unit is 13.375 in. wide by 5.5 in. high by 16 in. deep, and weighs 25 lbs. The P-7802 costs $3500.

Protek
P.O. Box 59
Norwood, NJ 07648
(201) 767-7242
▶CIRCLE 572

SPECTRUM ANALYZERS

Manufacturer	Model/ Price	Resolution bandwidth	Frequency Range	Frequency Accuracy	Amplitude Range	Amplitude Accuracy	Dynamic Range	Remarks
Tektronix Inc. P.O. Box 1520 Pittsfield, MA 01201 (800) 426-2200	497P/ $26,250	10 Hz - 3 MHz	100 Hz - 7.1 GHz	±21 kHz (@1 GHz)	–130 to +30 dBm	±2.5 dB	90 dB[5]	Same as 2754P.
	492BP/ 2755AP/ $32,450	100 Hz - 3 MHz	10 KHz - 21 GHz	±21 kHz (@ 1 GHz)	–120 to +30 dBm	±3.5 dB	90 dB[5]	Same as 2754P.
	494AP/ 2756P/ $37,450	10 Hz - 3 MHz	10 kHz - 21 GHz	±20 kHz (@ 1 GHz)	–134 to 30 dBm	±3.5 dB	90 dB[5]	Same as 2754P.
	2782/ $72,550	3 Hz - 10 MHz	100 Hz - 33 GHz		–135 to +30 dBm	±2 dB	100 dB[5]	2 IEEE-488 ports std. built-in frequency counter.
	2784/ $79,500	3 Hz - 10 MHz	100 Hz - 40 GHz		–135 to +30 dBm	±2 dB	100 dB[5]	Same as 2782. Coaxial input to 40 GHz.
	3052/ $99,500	1.25 Hz - 12.5 kHz	dc - 10 MHz	center freq. X 10–7	–147 to +33 dB	±0.5 dB	84 dB	Real-time output in spans to 2 MHz.
Wandel & Goltermann Inc. 2200 Gateway Centre Blvd. Morrisville, NC 27560-9228 (919) 460-3300	SNA-5A/ $52,000	3 Hz - 1 MHz	50 Hz - 3.2 GHz	$\pm 1 \times 10^{-9}$/day[9]	–140 to +30 dBm	±0.65 dB	90 dB[1]	IEEE-488 std.
	SNA-7A/ $60,000	3 Hz - 1 MHz	50 Hz - 22 GHz	$\pm 1 \times 10^{-9}$/day[9]	–140 to +30 dBm	±0.8 dB	90 dB[1]	IEEE-488 std.

[1] Based on third-order products.
[2] Frequency span/25 to frequency span/3200.
[3] Depends on measurement window.
[4] Based on second- and third-order harmonic distortion.
[5] Based on two-signal third-order intermodulation distortion.
[6] Display dynamic range.
[7] Aging rate: 1×10^{-6}/year; temperature stability: 4×10^{-8}/°C. Absolute accuracy can be set to prime standard.
[8] For spans $\geq$ 5 MHz: Error $= \pm(2 \times 10^{-3})$span $\times$ reference accuracy.
For spans $>$ 5 MHz: Error $= \pm(5 \times 10^{-3})$span $\times$ reference accuracy.
[9] Drift error limit.

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DAZIX	Sun	Design capture, simulation
IKOS	IKOS	Simulation, fault grading
Mentor Graphics	HP/Apollo Sun/Solbourne	Design capture, simulation Parade: Layout, clock and timing structures
Synopsys	Sun-4 Interface to Mentor, Valid, Viewlogic	Design synthesis, test synthesis
Valid	Sun/Solbourne DECstation 3100 IBM RS6000	Design capture, simulation Design check GED, ValidSIM, RapidSIM
VIEWlogic	Sun-4 PC386	Design capture, simulation Design check

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OKI Semiconductor
785 North Mary Avenue
Sunnyvale, CA 94086-2909
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NEW!...THE MOST POWERFUL...MOST ACCURATE CLUB IN GOLF!

The CONTROLLER® HITS 30-50 YARDS LONGER, AUTOMATICALLY CORRECTS HOOKS AND SLICES ...MUST CUT STROKES — OR MONEY BACK!

Put your #3, #4 and #5 woods in the cellar. Tests show our new Controller driving iron can outhit all three by 30 to 50 yards.

And that's only half the story. The Controller automatically corrects hooks and slices! The club is so powerful, so accurate, we unconditionally guarantee it will cut 5 to 10 strokes off your score — or you owe us nothing! In fact, to prove it we'll send you one risk-free.

Test it against your #3 wood. If it doesn't give you 30 more yards (if you are a fairly good golfer), send the club back for a refund.

But it will give you 30 more yards! In fact, the Controller is so powerful many golfers use it off the tee, especially on narrow fairways.

Here is the Controller's exact distance advantage as compiled by some low-80's golfers.

CONTROLLER®	220 yards
#3 Wood	190 yards
#4 Wood	180 yards
#5 Wood	170 yards

Now test the Controller's accuracy against your 3-iron. Purposely hit a shot off the *toe* of each club and watch what happens. Your 3-iron will *hook* the ball violently—the Controller will keep it down the middle! The same is true with *heel* shots. Your 3-iron will *slice* the ball violently—the Controller will automatically keep it on course!

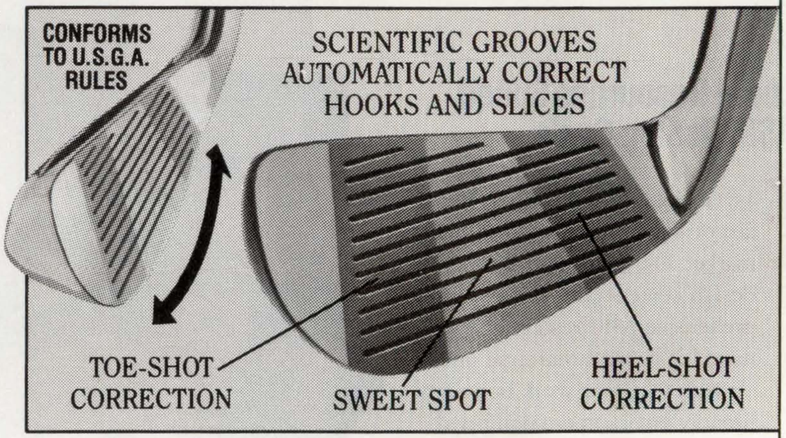
THE GREATEST STROKE-CUTTER IN GOLF

These scientific breakthroughs make the Controller driving iron the most powerful strokecutter in golf. We believe the club will transform the game. First of all, **it obsoletes fairway woods!** The Controller not only hits 30 to 50 yards farther than fairway woods, **it automatically corrects hooks and slices!** Here's how it works.

AUTOMATIC ACCURACY

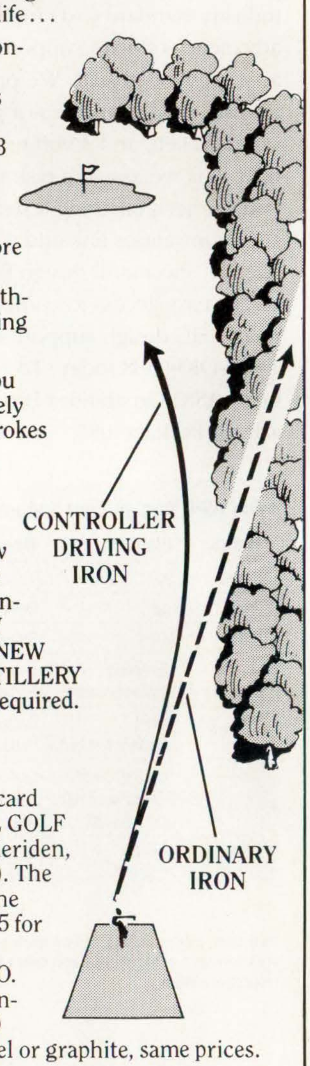
The Controller has an *invisible curve* acrcss its hitting surface—a curve that's going to revolutionize your game. *No other iron has it!* Hit a shot off the Controller's sweet spot and it will go straight, as it would with an ordinary iron. But even pros hit off the heel and toe.

Now, here is the Controller's genius...here is why you could cut as many as 10 strokes off your score. Hit the ball off the Controller's heel or toe and its invisible curve will automatically impart a corrective spin to what would otherwise be a disastrous hook or slice. The ball will actually fade or draw back on course! It's an incredible sight and you can prove it to yourself with only a few test shots. **THIS IS THE MOST IMPORTANT GOLFING BREAKTHROUGH IN GENERATIONS.** ALONG WITH THE CONTROLLER'S EXTRA 30-50 YARDS, YOU SHOULD EASILY CUT 5-10 STROKES OFF YOUR GAME!



Here are more reasons why the Controller driving iron is going to give you the best golf of your life...

- it gives you the power of a driver with the control of an iron...
- its sleek, smooth head swoops through grass more cleanly than a wood...
- its 17° loft gets your shot up faster than a #3 wood...
- its smaller head size (versus a wood) boosts clubhead speed...
- its boron-graphite shaft model adds even more clubhead speed...
- it lets you carry more wedges and putters without exceeding the 14-club limit (by eliminating your #3, #4 and #5 wood)...



The Controller is new and supply is limited. You must act now and remember, you are completely protected. If the Controller doesn't cut 5-10 strokes off your score, you may return it (undamaged, of course) for a prompt refund of its price.

FREE!

...just for trying the Controller! Keep your new power pin-high with a $15.00 Rangefinder! It's yours to keep FREE! even if you return the Controller for a refund. NOW YOU CAN RANGE YOUR NEW DISTANCE LIKE AN ARTILLERY OFFICER. No batteries required. Clips to belt.

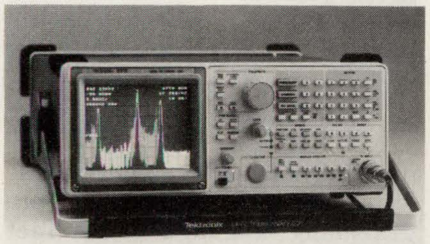
HOW TO ORDER

Send your name, address and check (or credit card number and expiration date) to the NATIONAL GOLF CENTER (Dept. DR-262), 500 So. Broad St., Meriden, CT 06450. Or call 203-238-2712 (8-8 PM, M-F). The steel-shaft CONTROLLER costs only $59.00; the carbon-graphite model costs $89.00. Add $4.75 for s/h/ins. CT and NY must add sales tax. Specify regular or stiff flex, right or left-handed. No P.O. boxes, all deliveries are UPS. A refund is guaranteed if a club is returned undamaged within 30 days. Clubs are also available in ladies size, steel or graphite, same prices.

THE CONTROLLER HITS LONGER AND STRAIGHTER THAN ANY OTHER CLUB IN GOLF. IF IT DOESN'T CUT 5-10 STROKES, YOU OWE US NOTHING! ACT NOW!

▼ PORTABLE ANALYZER COVERS 9 KHz TO 1.8 GHz

The 2711 portable spectrum analyzer covers a 9-kHz-to-1.8-GHz bandwidth, making it ideal for various applications involving broadcast, broadband network, communications, and biomedical engineering systems. The analyzer features sen-



sitivity of up to −129 dB, 80 dB of display dynamic range, spans as narrow as 10 kHz/div., and a selection of resolution bandwidth filters from 3 kHz to 5 MHz. Users can view spectral activity in a true analog display mode, or they can view and compare up to four digitally stored signals. Key measurements, such as carrier-to-noise, occupied bandwidth, normalized bandwidth, signal search, and FM deviation, can be made automatically. The unit includes an AM/FM demodulator with a speaker and headphone jack to make signal identification and monitoring easier. Internal memory stores up to 36 front-panel setups and five antenna correction-factor tables. A user-defined key stores measurement keystroke sequences. Options include IEEE-488 and RS-232C interfaces, a frequency counter, an internal tracking generator, and video demodulation. Prices for the 2711 spectrum analyzer start at $8750, with delivery in 5 weeks.

Tektronix Inc.
Test & Measurement Group
P.O. Box 1520
Pittsfield, MA 01202
(800) 426-2200
▶ **CIRCLE 573**

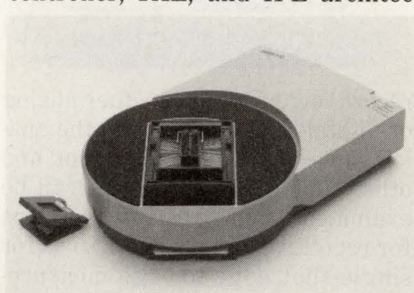
▼ UPGRADED GPIB-TO-VXI INTERFACE IS 60% FASTER

An upgraded GPIB-to-VXI interface achieves 60% faster on-board execution speed than its predecessor. The GPIB-VXI/C converts GPIB (IEEE-488) signals and protocols so that an IEEE-488 controller can run VXIbus instruments. The interface uses a 16-MHz SC68070 processor and a proportionally faster memory interface to attain the enhanced performance. The board also uses the company's NAT4882 and Turbo488 ASICs for the highest possible GPIB performance. In addition, the Message-based Interface Gate Array ASIC increases the capability and performance of the VXIbus word serial protocol while maintaining compatibility with the older interface. The unit is fully compatible with all revisions of the VXIbus and IEEE-488 standards. The GPIB-VXI/C is available immediately for $2700.

National Instruments Corp.
6504 Bridge Point Pkwy.
Austin, TX 78730-5039
(800) 433-3488 or (512) 794-0100
▶ **CIRCLE 574**

▼ PROGRAMMER USES CUSTOM DEVICE LIBRARIES

A single-site programmer for design engineers, the 3900 Programming System, features customized device-support libraries. Device libraries are available for FPGA, PLD, PROM, EPROM, EEPROM, microcontroller, PAL, and IFL architec-



tures. The unit employs a proprietary modular socketing technique that handles DIP and surface-mountable LCC, PLCC, and SOIC packages. Preprogramming testing capabilities include blank, illegal-bit, misregistration, backwards-device, and electronic-identifier tests. The 3900 also performs verification, marginal-verify, and structural tests. Users can select from four operating modes: PC interface, standard terminal, portable terminal, or computer remote control. The 3900 base price is $5495, including a standard 48-pin socket and 128 kbytes of RAM.

Data I/O Corp.
10525 Willows Rd. N.E.
Redmond, WA 98073-9746
(206) 881-6444
▶ **CIRCLE 575**

▼ IEEE-488 DRIVER OFFERS WINDOWS 3.0 CAPABILITY

Driver488/WIN is an IEEE-488 driver in the form of a dynamic link library that facilitates the integration of IEEE-488 instrument control into Windows 3.0 applications. The software can be configured to control IOtech's 8- and 16-bit IEEE-488.2 interface boards for PC, AT, and EISA-bus computers. Driver488/WIN was specifically designed to take advantage of Windows' multitasking environment. The software doesn't require extensive user programming to support multiple-task instrument access. The software also conforms to Windows' event-handling system for asynchronous IEEE-488 events. Driver488/WIN, which costs $195, can be purchased as part of the Personal488/WIN package. The package includes an 8-bit IEEE-488.2 board for $395. The driver can also be bought with the Personal488AT/WIN package, which features a 16-bit, 1-Mbyte/s interface board, for $495. All are available from stock.

IOtech Inc.
25971 Cannon Rd.
Cleveland, OH 44146
(216) 439-4091
▶ **CIRCLE 576**

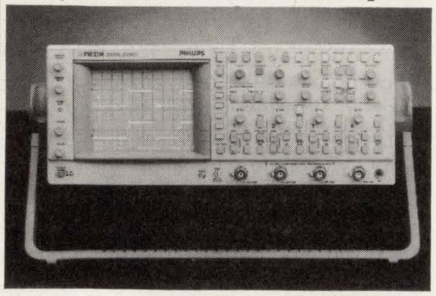
▼ WORKSTATION PROGRAM CREATES TEST VECTORS

TDX-130 is a low-cost, workstation version of Test Design Expert (TDX), an automatic test vector generation program for ASIC designers. Using the behavioral and structural circuit descriptions, TDX-130 creates test vectors for ASICs with up to 25,000 two-input gate equivalents. The software handles sequential and asynchronous logic, as well as combinatorial circuits. As an open system, TDX works with any design methodology, CAE software, foundry process, or test equipment. Users can select the design-for-test strategy that best fits their design, or they can proceed without any DFT scheme. The TDX system, available for Sun Sparcstations, starts at $140,000. TDX-130, available for Sun workstations, starts at $100,000.

ExperTest Inc.
810 E. Middlefield Rd.
Mountain View, CA 94043
(415) 965-2000
▶ **CIRCLE 577**

▼ ANALOG/DIGITAL SCOPES OFFER 4 FULL CHANNELS

A series of oscilloscopes offers combined analog and digital capability in 100- and 200-MHz instruments with either 4-channel or 2+2-channel operation. The PM 3384 and PM 3394 are 100- and 200-MHz scopes, respectively, with true four-channel opera-



tion—that is, full sensitivity and complete attenuation ranges on each channel. The PM 3382 and PM 3392 offer 2+2-channel operation. In digital mode, the scopes' sampling rate is 200 Msamples/s and acquisition memory is 32 ksamples. A feature called Touch Hold and Measure lets users initiate measurements from a probe-mounted button. Triggering includes logic state and pattern capability, and glitch capture down to 2 ns. The analog mode is useful in applications that demand the "live" signal representation and infinite resolution of analog instruments. The PM 3384 and PM 3394 cost $5490 and $6490, respectively. The PM 3382 and PM 3392 cost $4490 and $5590.

John Fluke Mfg. Co.
P.O. Box 9090
Everett, WA 98206-9090
(206) 347-6100
▶ **CIRCLE 578**

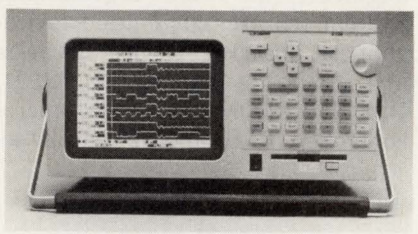
▼ MIXED-SIGNAL TESTER BOASTS HIGH DATA RATES

The Mixed-Signal ATS test station is aimed at debugging, characterization, and test of leading-edge ASICs. Intended applications include fast digital-dominant ASICs or multichip modules, embedded converters, and complex devices that need sequencing of events or critical timing. The system delivers digital data rates of 400 Mbits/s with 100-ps accuracy and a noise floor of less than 100 dB. The bandwidth of instruments used for analog measurements exceeds 1 GHz. Coherent clocking and flexible instrument controls ensure effective use of digital-signal-processing techniques. The system's user interface, which is based on X-Windows/Motif, lets users select from three levels of interactivity and programming flexibility. A typical 224-pin system, including a Sparc workstation, 400-Mbit/s data rates, and 600-MHz analog acquisition and generation capability, costs $630,000.

Integrated Measurement Systems Inc.
9525 S.W. Gemini Dr.
Beaverton, OR 97005
(503) 626-7117
▶ **CIRCLE 579**

▼ 16-CHANNEL DSO FEATURES LOGIC ANALYZER TRIGGERS

The Model K1600 Analog Logic Analyzer is a 16-channel digital storage oscilloscope with logic-analyzer triggering. Combinatorial triggering functions include delay by time, trigger going true or false, and time between events. This dual-instrument capability means users can view and

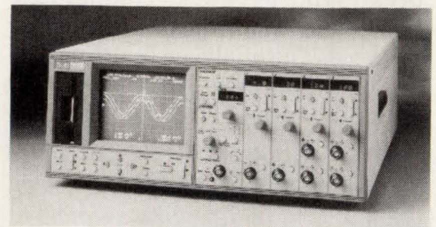


record logic signals in either analog or digital mode. Therefore, the analog wave shape, time alignment, and other timing characteristics can be examined. Timing resolution is 50 ps for repetitive signals and 1.25 ns for single-shot edge-to-edge measurements. The K1600 has a 350-MHz input bandwidth, a 1-ksample record memory for each channel, and a reference memory. Sampling speed ranges from 800 Msamples/s on 2 channels to 100 Msamples/s on 16 channels. The K1600 costs $14,950 and delivery is within 90 days.

Biomation Corp.
19050 Pruneridge Ave.
Cupertino, CA 95014
(800) 538-9320
▶ **CIRCLE 580**

▼ DSO LINE OFFERS WIDE RANGE OF CAPABILITIES

The Nicolet Pro line of digital oscilloscopes offer 256-ksample/channel memories, an on-board programming language, and logic-analyzer-style triggering. The seven models in the series offer a wide choice of sampling speeds, resolutions, and channel counts. The scopes eliminate false triggers and jitter by using a variable-sensitivity hysteresis control that arms or triggers the instruments only when the input passes se-



quentially through two operator-selected voltages. The resident programming language, called Tact, gives the user access to all front-panel and IEEE commands, as well as math functions, through a PC-style keyboard connected directly to the scope. Models include 2- and 4-channel versions with 8- and 12-bit resolutions and sampling speeds from 1 to 200 Msamples/s. Prices range from $11,990 to $28,990. Delivery is from stock to 30 days.

Nicolet Test Instruments
5225 Verona Ave.
Madison, WI 53711
(800) 356-8088 or (608) 271-3333
▶ **CIRCLE 581**

▼ PROGRAMMABLE LOADS FIT MANY APPLICATIONS

The PLZ-3W series GPIB-programmable loads have built-in microprocessors, so users can tailor the program and sequence of load current, voltage, resistance, and power settings for each application. The four units have an effective operating range of 1.5 to 120 V dc. Current and power ranges are 0 to 30 A (150 W), 0 to 60 A (300 W), 0 to 120 A (600 W), and 0 to 200 A (1000 W). All units feature constant-current, constant-resistance, constant-voltage, and constant-power modes. Users can program rise and fall times from 50 μs to 10 ms and load soft-starts from 0.1 to 100 ms. Other features include load pulsing; load program sequencing; and programmable overvoltage, power, and reverse-voltage protection. Prices starts at $1900.

Kikusui International Corp.
1980 Orizaba Ave.
Signal Hill, CA 90804
(310) 986-1677
▶ **CIRCLE 582**

▼ DSP BOARD OFFERS CHOICE OF PROCESSOR TYPES

A floating-point, digital-signal-processor board built in a one-slot 6U VME module creates the ability to choose the type and number of processors. Users can select one or two AT&T DSP32C or Texas Instruments TMS320C31 processors. The devices are mounted separately on daughterboards that plug onto the ZPB3400 module. As a result, the module can be configured to deliver 25, 33, 50, or 66 MFLOPS, along with the ability to handle real-time data input sample rates up to 10 MHz. Each processor has its own high-speed serial port and 256 kbytes of zero-wait-state SRAM. They share 10-MHz input FIFO buffers. ZPB3400 prices start at $4495 for unit quantities; quantity and OEM discounts are available. Small-quantity delivery is from stock to four weeks.

Burr-Brown Corp.
P.O. Box 11400
Tucson, AZ 85734
(800) 548-6132 or (602) 746-1111
▶ CIRCLE 583

▼ SYNTHESIZER GENERATES COMPLEX ANALOG WAVES

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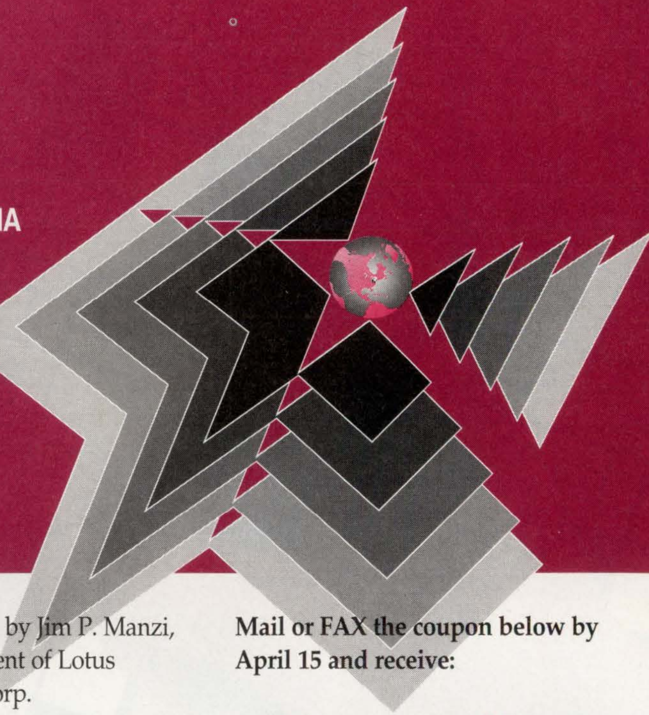

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A PWM Controller IC With An On-Chip 700-V, 2-A MOSFET Power Switch Builds 30- To 60-W Off-Line Switching Power Supplies.

IC Switcher Delivers 60 W From AC Line Voltages

Frank Goodenough

Even though power ICs have ascended to new heights over the past few years, they have yet to become fully accepted in major application areas. Few available power ICs can cope with both high voltages and several watts of power. Those that control more than a few watts are limited to controlling dc input voltages between 40 and 60 V, while those rated at even higher voltages are limited to 2-3 W. Now a complete monolithic switching regulator, with a controller and power switch on one chip, increases power-handling capability 20-fold without sacrificing voltage-handling capability. The IC can be used to build 60-W switching power supplies that run directly off a rectified 220/240-V ac line without an external power MOSFET switch.

The PWR-SMP260, developed by Power Integrations, can also be employed to build 30-W "universal" switching supplies that run off rectified ac lines ranging from 85 to 265 V. Moreover, this current-mode switcher is designed to operate in conventional "flyback" and "forward converter" topologies that provide transformer-coupled input-to-output isolation. In addition, the user can program the power IC for either 50 or 90% duty cycles.

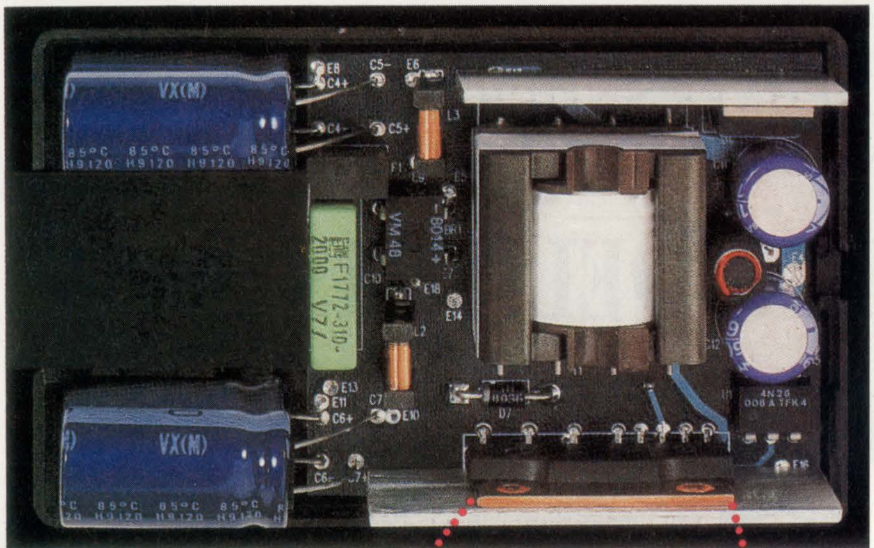
In most applications, the rectified line voltage is stepped down to typical logic and/or analog-supply voltage levels, such as +5, –5.2, +12, and ±15 V. However, because a transformer is used, the voltage can be stepped up, enabling it to provide a high voltage like that needed for a monitor's CRT. Additional windings on the transformer supply lower voltages.

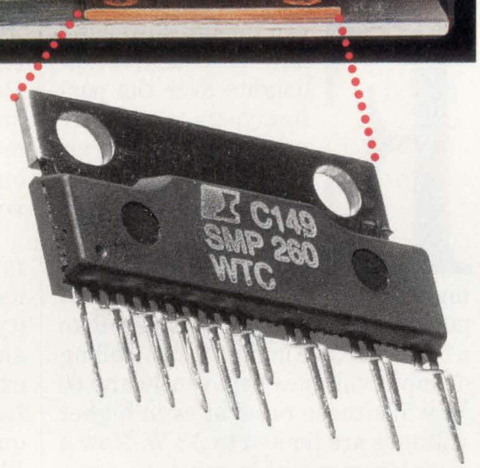
The PWR-SMP260's most important specification, however, may be its price. It *is not* a laboratory curiosity, but rather a practical device aimed at volume applications. For example, in quantities of 1000 it goes for $4.25 each, but it drops to $2.35 in quantities of 100,000. Its cohort, the PWR-SMP240, which differs only in power rating and price (it delivers 20 and 40 W, respectively, from the 115-V and 220-V ac lines), goes for $3.85 each in 1000-unit lots and just $2.00 apiece for 100,000.

Either of the two chips can easily be used to build an 8.4-in.^{3} power supply that's approximately 1.2 in. high by 3.5 in. long by 2 in. wide *(Fig. 1)*. The chips' small size makes them well-suited for off-line power-supply/battery chargers in products powered by NiCd batteries. Applications can range from laptop PCs, standalone peripherals, and camcorders to industrial power tools, portable medical instruments, and cellular/cordless telephones.

The small size of the supplies built with the PWR-SMP260/240 results from the elimination of the power switch and the IC's small 23-pin package. The small size is also the result of the IC's ability to operate at pulse-width-modulated (PWM) switching frequencies up to 400 kHz. High-fre-

COMPLETE 60-W OFF-LINE SWITCHING REGULATOR IC





1. A SINGLE IC forms the heart of this universal off-line 30-W 115-V ac power supply. It measures 1.2-in. high, takes up just 8.4 in.³ of volume, and weighs 4 oz. The 1.2-by-0.6-in. PWR-SMP260 IC developed by Power Integrations (inset) is a complete switching regulator in one package. The device can also be used to build a 60-W supply running off 220-V ac lines.

quency operation minimizes the size of inductors and capacitors. In addition, on-chip circuitry does away with many of the off-chip support components needed for standard controller ICs like the 3842 or 3823.

The "tiny" power-IC die are fabricated on a proprietary, 11-mask process. The process builds high-voltage, logic-level (a gate-to-source voltage of 5 V turns them on hard) lateral-MOSFET power switches, rather than the more common high-voltage vertical DMOS devices. For control circuitry, the process builds low-voltage (30 V) bipolar and CMOS transistors. The power switch has a 3-Ω on-resistance and carries a maximum drain-to-source voltage rating of 700 V. The maximum input voltage to the switch's V_{in} pins is 500 V *(Fig. 2)*.

Integrating the controller and power switch not only saves space, but also increases performance. The gate drive is optimized for the logic-level FET, and the total delay time from the current-mode comparator to the MOSFET output can be specified (typically no more than 75 ns) without assuming delay through an external drive circuit. In addition, the lateral power FET's low-voltage (5-V) gate drive and its very low Miller capacitance minimize power dissipation.

PROTECT THYSELF

To a power-supply designer, a new design's reliability tops the list of priorities. For switching power supplies, this translates into using a switching-regulator controller with a full suite of self-protection features covering the supply and the load. And the PWR-SMP260/240 comes well-equipped for these tasks. To begin with, it offers continuous regulation from zero to full load, a first for current-mode switchers. A unique circuit, for which a patent has been applied, provides low-load regulation. Other protection features include shutdown-on-fault with auto-restart, adjustable current limiting, undervoltage lockout, thermal shutdown, and a full-cycle soft-start circuit implemented digitally with a counter and a 5-bit digital-to-analog converter. The digital soft-start circuit, a first, eliminates the need for large-value, low-leakage timing capacitors.

In a simplified version of a typical "flyback" power supply, the rectified power-line voltage is connected to the MOSFET switch's drain through the power transformer, and to the V_{in} pin, at power-up *(Fig. 3)*. This simplified circuit doesn't reveal all of the pins or external connections to the PWR-SMP260/240.

The chip's linear off-line regulator supplies the voltage V_s (the low-voltage power for the IC) before the PWM circuit is running; the bias regulator provides this voltage after the PWM circuit is running *(Fig. 2, again)*. Each linear regulator contains a high-voltage MOSFET and a current source to drive the FET's gate. Both share the error amplifier that regulates V_s from either V_{in} at startup or from the bias (bootstrap) supply while running. V_s, which powers the control and driver circuits, runs 5 to 6 V. The circuit operates if V_{bias} is between 8 and 30 V. The bandgap reference sets the threshold for the current-mode regulator, as well as the soft-start and over-temperature shutdown features. A precision 20.5-kΩ resistor connected to the $R_{external}$ pin develops precision current sources from the reference *(Fig. 3, again)*.

The output of the sawtooth oscillator turns on the power switch after passing through a D-type flip-flop used for 50% duty-cycle operation, and an RS-type flip-flop used for latching. If a 50% (maximum) duty cycle is required, the slope-compensation pin is connected to V_s. V_s inserts, via the duty-cycle-select comparator, the circuit's D-type flip-flop to divide the clock by two. A capacitor connected to the $C_{external}$ pin sets the clock's frequency, which may be synchronized to an external signal (such as another PWR-SMP260/240)

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that's fed to the "Sync" pin. Holding the Sync pin low for at least 10 μs puts the chip to sleep, limiting power dissipation to between 20 and 500 mW, solely due to the off-line regulator's maximum current of 1 mA multiplied by V_{in}.

Any current-mode PWM regulator running at more than a 50% duty cycle requires slope compensation. This compensation implements the function by connecting a resistor between the slope-compensation pin and common.

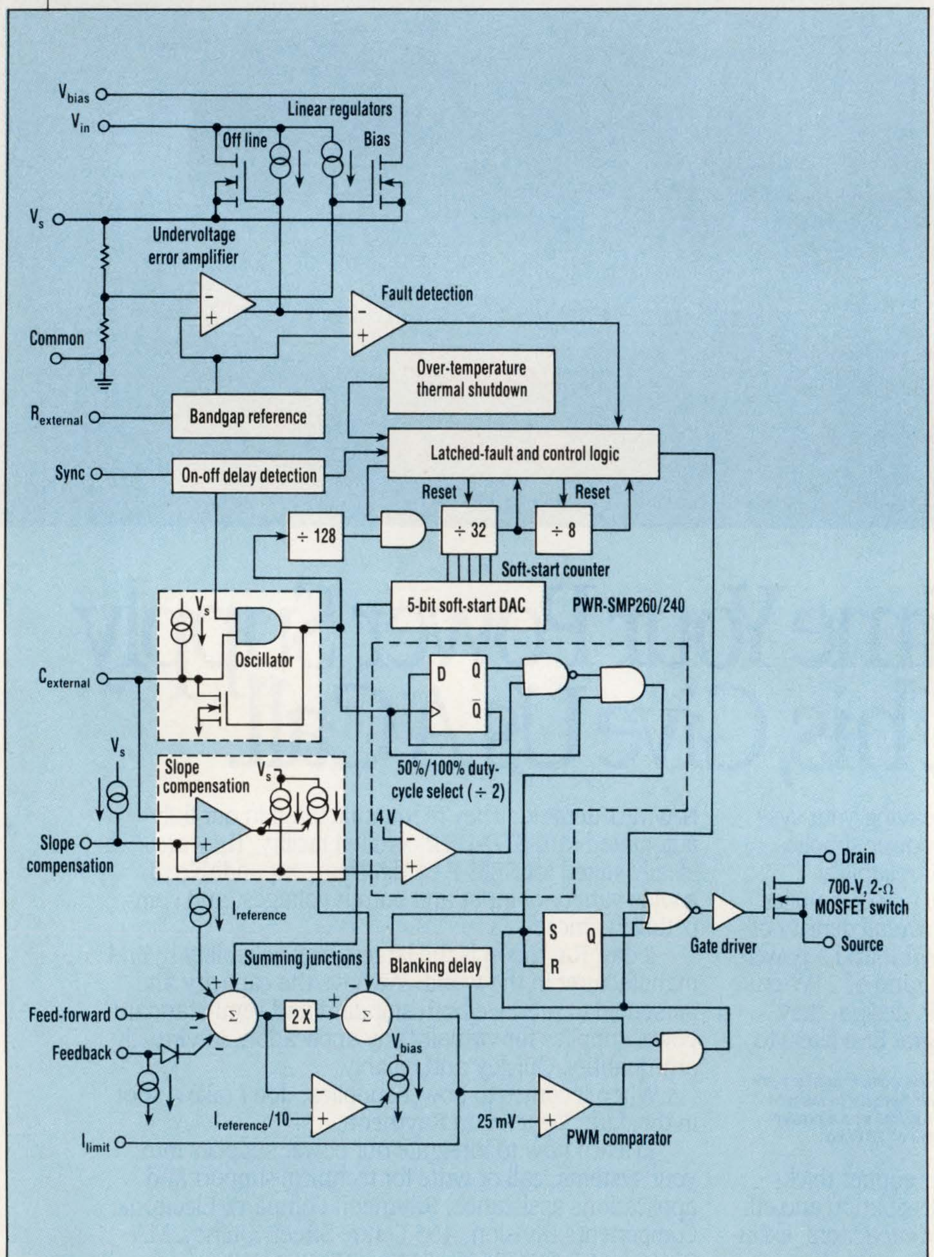
The heart of this switching regulator is, of course, the current-mode pulse-width modulator consisting of the summing junctions Σ, the current-sensing PWM comparator driven by the summing junctions, and the RS-type flip-flop latch. The summing junctions algebraically add currents from the soft-start DAC, the slope-compensation circuit, and the feedback and feed-forward circuit blocks. The greater the current flowing into these summing junctions, the lower the current flowing from the second summing junction through off-chip resistor R_c (connected to the I_{limit} pin) and the lower the switch on time (and thus peak current through it).

The voltage across R_c creates the PWM-comparator's threshold voltage. This voltage is compared with the voltage across the external current-sensing resistor R_s. The ratio of the two resistors gives the supply designer the ability to set the maximum switch current (a feature not found on all controllers), which should be no more than 3 A. When the comparator fires, it resets the RS-type flip-flop and turns off the power FET, holding it off until the next clock pulse. The leading-edge blanking delay permits the turn-on current transient to stabilize before the comparator is connected to the flip-flop, preventing the transient from immediately turning the switch off.

Like all current-mode PWM switching regulators, the SMP260/240 switching regulator contains two feedback loops: the current loop just described and the voltage-feedback loop that actually senses and controls the output voltage.

The output voltage is applied to an off-chip error amplifier (an op amp), which in turn drives an optoisolator. The isolator's output transistor, powered from the bias supply, feeds a current directly proportional to the output voltage into the feedback pin, and through the pin to the first summing network. As noted previously, the greater the current into these summing networks, the lower the switch's on time and thus the power delivered to the load.

A resistor from V_{in} to the feed-forward pin corrects directly for wide variations in the ac-line voltage. As V_{in} increases, the summing networks' input currents increase, their output currents decrease, and

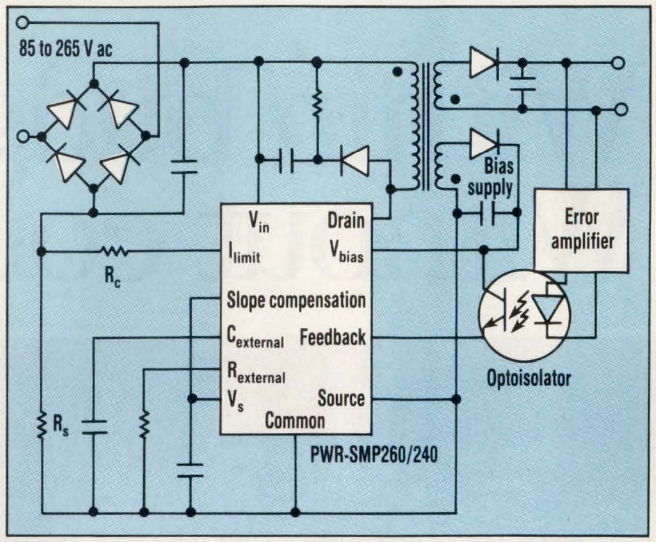


2. THE PWR-SMP260/240 **consists of a current-mode PWM switching-regulator controller plus a 700-V, 2-A MOSFET switch. It contains a full suite of self-protection features, including undervoltage lockout, a unique soft-start circuit implemented with a counter and a 5-bit DAC, and thermal-shutdown capability. In addition, the user can program it for 50% or 90% duty-cycle operation.**

COMPLETE 60-W OFF-LINE SWITCHING REGULATOR IC

switch on time drops. This feature, and the controller IC's ability to operate with a wide-ranging bias supply, enhances battery-charging applications.

At power-up or after a shutdown due to a fault, the soft-start DAC injects 100% of the reference current into the summing junction and incrementally decreases it to zero, essentially ramping up the switch's on time linearly. The slope-compensation current into the first summing junction decreases the magnitude of junction output current linearly as the duty cycle is increased beyond 50%.



3. COMPLETE INPUT-TO-OUTPUT **ac-line isolation can be achieved in a universal 30-W supply with this circuit, which uses the PWR-SMP260 PWM switching-regulator IC. The device forms the core of an off-line supply with a flyback topology.**

NO MINIMUM LOAD

Most current-mode regulators don't perform well at minimum loads. Even the very short pulses transfer an incremental amount of power to the output every time the power switch is turned on. No-load operation usually requires using a preload resistor on the output, which lowers efficiency and limits maximum power, or dropping the clock rate very low and operating in the "hiccup mode." The latter is equally unacceptable because of potential emission of audible noise from the transformer.

To beat the problem once and for all, the PWR-SMP260/240's designer came up with a circuit (patent applied for) that increases the load on the bias supply as the duty cycle drops below 12%. Dubbed the "active minimum-load" circuit (not shown in figure 3), it consists of a shunt regulator across the bias supply and a circuit that senses the current from the summing junctions. This active load circuit linearly increases the current through the shunt regulator as the load drops below 12% of full load (as indicated by the summing-junction output).

As noted earlier, the PWR-SMP260/240 has a complete suite of protection circuits. The undervoltage-lockout circuit senses the output of the undervoltage-error amplifier, holds the MOSFET switch's gate low, and resets the soft-start counter chain until V_s is within its valid operating range. Upon fault detection, the "latched fault logic" turns off the FET switch and starts the restart delay sequence. When the soft-start counter reaches 28,672 clock cycles, the soft-start sequence begins.☐

PRICE AND AVAILABILITY

The PWR-SMP260 and PWR-SMP240 are rated for operation from 0 to 70°C. They come in a 23-pin power SIP with a metal tab. Pricing for each device is indicated in the text.

Power Integrations Inc., 411 Clyde Ave., Mountain View, CA 94043; Doyle Slack, (415) 960-3572. **CIRCLE 512**

HOW VALUABLE?	CIRCLE
HIGHLY	544
MODERATELY	545
SLIGHTLY	546

Battery-Powered Modem Family Combines Send-Receive Fax With Up To 38.4-kbit/s Data Rates.

Chip Set Targets Pocket And Laptop Modems

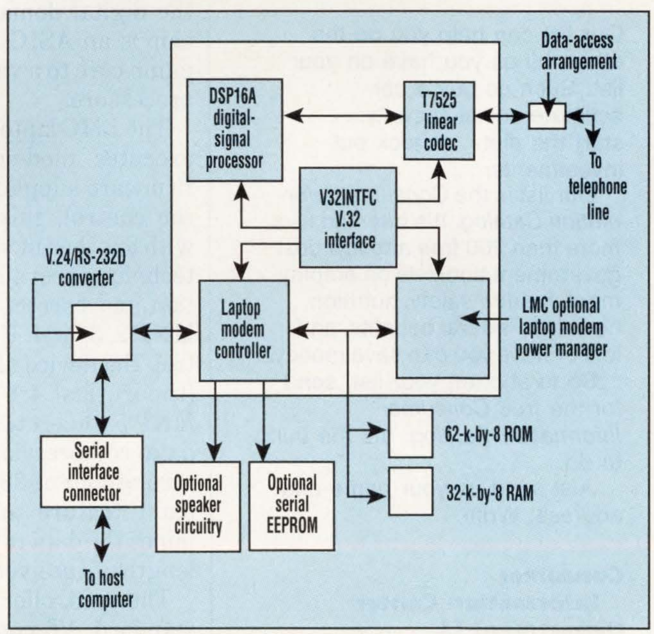
Milt Leonard

Implementing a full-featured data modem in laptop and handheld computers, as well as in pocket-modems, requires a chip set with a unique blend of capabilities. Not only must the chip set pack a host of features in a minimum area of silicon, but also it must present a low power drain to the battery, have high data rates, and be easy to apply by modem designers. Also desirable is facsimile-machine compatibility. A new CMOS modem chip set from AT&T reportedly offers all of these capabilities.

The V32F-V42L modem chip set from AT&T Microelectronics is a two-wire, full-duplex modem that operates over the public switched telephone network. According to AT&T, the chip set is the first to combine Group 3 fax compatibility with a data-mode rate of up to 38.4-kbits/s for laptops and small-format, battery-powered modems. Using the AT&T chip set, a modem manufacturer can build a complete modem that consumes less than 800 mW.

For basic modem operation, the chip set consists of four devices *(see the figure)*. The DSP16A data-pump digital-signal processor, the T7525 linear codec, and the V32INTFC interface chip. Control functions are handled by the LMC controller. An optional power manager, the LMPM, reduces laptop power consumption in the "sleep" mode. This small gate array shuts down non-essential circuits during the sleep mode. It can be implemented with discrete components. The T7525 analog front-end performs analog-to-digital and digital-to-analog conversion, infinite-impulse-response filtering, and transmit and receive gain adjustment.

To connect the modem to the telephone line, the user supplies the data-access arrangement (DAA), which consists of a transformer, a re-



1. DATA-PUMP FUNCTIONS for laptop and pocket modems are implemented with three components of AT&T's five-chip device set: the DSP16A digital-signal processor, the T7525 codec, and the V32INTFC interface chip. The LMC laptop modem controller provides error-control, compression, and fax functions. The optional power manager reduces sleep-mode power consumption to just 10 mW.

LAPTOP MODEM CHIPS

lay for pulse dialing and hook control, ring-detect circuitry, and a simple 2-4 wire converter, all of which can be mounted on a 0.5-by-0.75-in. board. Signals to and from the telephone line pass through the linear codec to the DSP16A digital-signal processor. The DSP16A performs processing functions necessary for compatibility with most existing modems and new modems conforming to commonly used CCITT (Consultative Committee for International Telephony and Telegraphy) and Bell standards. These include CCITT V.32, V.22bis, V.22, V.21, and V.23, and Bell 212A and 103 specifications for data rates of 9600, 4800, 2400, 1200, 600, and 300 bits/s.

The DSP16A also supports the V.29, V.27ter, and V.21 ch.2 modulation standards for Group 3 fax machines, for bit rates of 9600, 7200, 4800, 2400, and 300 bits/s. In the CCITT test mode, the DSP16A performs analog-loopback and digital-loopback tests for the local modem, and remote digital loopback testing of a remote modem. The DSP16A also performs echo-cancellation in the digital domain. The V32INTFC chip is an ASIC that links the data-pump core to a variety of host microprocessors.

The LMC laptop modem controller executes modem operations from firmware supplied by AT&T. For error control, this device negotiates with another modem to establish the technique best suited for error detection and correction: CCITT V.42 or MNP 2, 3, or 4. Under firmware control, the device also provides V.42bis (theoretical 4:1 compression) and MNP 5 (theoretical 2:1 compression) data compression for a maximum throughput of 38.4 kbits/s. An autobaud feature automatically determines the data rate, parity, and word length of received signals.

The controller also supports the standard AT command set, the industry-standard command interpreter that is compatible with most software communications packages. This command set includes EIA/TIA (Electronic Industries Association/Telecommunications Industry Association) 578 Class 1 fax extensions, which allow the modem to communicate with fax machines. These operations require user-supplied external memory. A 64-kword-by-8-bit ROM is needed for storing error-correction and data-compression firmware provided by AT&T. This includes V.42, V.42bis, and MNP 4 and 5 software. V.42bis data compression also requires a 32-kword-by-8-bit scratchpad RAM.

Users can also add an EEPROM to store telephone numbers, modem configuration parameters, or other data that must be retained when power is removed. For example, after setting up the modem for a particular applications, that configuration can be stored as one of two user profiles for subsequent recall. In pocket-modem applications, interface to the host computer requires a user-supplied CCITT V.24 (EIA-232-D) converter IC for a serial interface. This device is a signal-level converter between TTL-compatible (unipolar) and ±12-V (bipolar) decision logic. The controller can also connect to optional external speaker circuitry.

For minimum footprint, the V32F-42L components are mounted in surface-mount packages. Each of the DSP16A and V32INTFC chips comes in an 84-pin plastic quad flat pack or plastic leadless chip carrier. The T7525 linear codec is available in a 28-pin single-outline J package, and the LMC in a 100-pin quad flat pack. The optional LMPM is available in a 64-pin quad flat pack.

Typical active power consumption is under 800 mW for the data pump, controller, RAM, and ROM. In the sleep mode, power consumption is 10 mW with the modem power manager and under 50 mW without it.□

PRICE AND AVAILABILITY

The five-piece V32F-V42L modem chip set is available now for $110 per set in quantities of 10,000. Pricing for the chip set without the LMPM is $108.

AT&T Microelectronics, 555 Union Blvd., Allentown, PA 18103; Dan de Guzman, (714) 220-6255. **CIRCLE 513**

HOW VALUABLE?	CIRCLE
HIGHLY	541
MODERATELY	542
SLIGHTLY	543

HIGH-SPEED 16-BIT INTEGER DSP CHIP TACKLES COMPLEX TASKS

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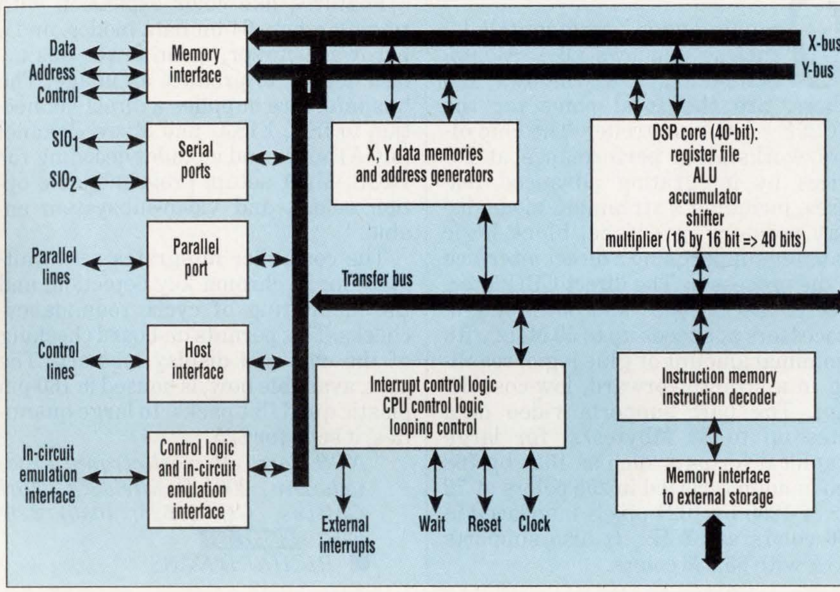


Although 16-bit digital signal processor chips have been around for years, they have been overshadowed by fast, highly integrated 32-bit floating-point DSP chips. That has changed. NEC Electronics has developed its SPX family of high-performance, 16-bit integer DSP chips and macrocell building blocks. Company designers built on an improved 16-bit DSP core with a 30-ns cycle time and added large multiple memory banks, 40-bit accumulation, and system resources like serial and parallel ports.

The CPU core was created to handle three-operand operations and perform dual load-store operations, thus supplying a great deal of instruction parallelism. Hardware parallelism permits the multiplier-accumulator, arithmetic and logic unit, and the barrel shifter sections to execute all in parallel on different data words in the instruction sequencer.

Multiple memory banks—two for data (or one for data, one for coefficients) and one for instructions—allow the CPU to simultaneously access all three storage areas. The X and Y data memory banks each hold 2 kwords-by-16-bits of RAM and 2 kwords-by-16-bits of ROM, while the instruction memory is either 8 kwords-by-32-bits of ROM or 1.5 kwords-by-32-bits of RAM.

Instructions execute in just 30 ns when the chip is clocked by a 66-MHz timing source (double the internal clock rate of the DSP). The DSP's instruction execution unit depends on bank of eight general-purpose 40-bit data registers, and both a 40-bit ALU and a barrel shifter. A simple three-level pipeline—instruction fetch, instruction decode, and execute—allows the DSP core to simultaneously execute three instructions. Hardware assistance to looping subroutines makes their execution simpler—a dedicated hardware loop counter reduces the overhead for loops that repeat from 1 to 32767 times. Up to 255 instructions can be included in a loop. Subroutine handling has also been made easier since a four-level-deep hardware stack allows subroutines to nest more than five levels.

In some typical applications, the SPX delivers some of the shortest times for computations for a 16-bit DSP chip. An 8-pole canonic infinite-impulse response filter (23 steps) can be done in just 0.7 μs; a 64-tap finite-impulse-response filter (70 steps) requires just 2.1 μs, while a complex 1024-point fast Fourier transform (32,000 steps) takes just 0.95 ms. Such performance suits the chip well for such applications as high-speed data/fax modems, digital cellular radio, multimedia audio, robotics, and automotive control, image processing, and telecommunications.

Also on chip are two double-buffered serial ports, which can operate at clock frequencies from dc to 16 Mbits/s and be set up to directly interface to codecs such as the NEC 9513 or AT&T 7524. Frame lengths of 8 and 16 bits can be selected and the buffers set to send out either the most-significant bit or least-significant bit first. An 8-bit parallel port on chip gives the DSP chip some control capability. And, as included on the previously released μPD77C25 DSP chip, the host interface includes DMA control support and handshake signals for interrupts, wait state support, and polling operations.

When operating from a 5-V supply the SPX will typically consume about 105 mA when clocked at 66 MHz. An on-chip serial diagnostic port implements a JTAG compatible interface to ease in-system testing. The SPX version with on-chip instruction ROM comes in a 120-lead plastic quad-sided flat package, while the version with internal instruction RAM comes in a 160-lead PQFP since it also includes a memory expansion bus.

Part of NEC's standard-cell library, the SPX core helps create a custom DSP chip. The library includes building blocks that range from simple gates to complex arithmetic and interface functions. Samples of the μPD77016 SPX digital-signal processor will be available late in the second quarter. In thousands the ROM-based version sells for about $40; the RAM-based version costs $45 in similar quantities.

NEC Electronics Inc., 401 Ellis St., Mountain View, CA 94039; Nobu Okuyama, (415) 965-6046.

CIRCLE 460

VGA CONTROLLER TARGETS HIGH-END GUIS

Graphical user interfaces (GUIs) such as Windows 3.0, Presentation Manager, X-Windows, and others, are the focal point for the 77C22E+ VGA controller. The chip offers workstation performance at PC prices by integrating advanced features, including a streaming-mode display memory interface, block-logic transfer support, and a direct interface to the processor. The direct CPU interface connects 80386 and 80486 microprocessors at speeds up to 50 MHz with a minimal amount of glue logic, resulting in a straightforward, low-cost design. The part supports video data rates up to 80 Mbytes/s, for large graphical formats such as 1024 by 768 pixels noninterlaced in 256 colors at 72 Hz or 1280 by 1024 pixels interlaced in 256 colors at 87 Hz. It also supports XGA with 65,536 colors.

Features like color expansion with transparency, 64-bit data modes, and a hardware cursor, mean fewer bus cycles needed to produce an image. The bus interface supplies a direct connection to ISA, EISA, and Micro Channel (MCA) buses and includes decoding for BIOS, MCA setup, programmable option select, and video-subsystem enable.

The controller integrates zero-wait-state logic, chroma key detection, and the monitoring of cyclic redundancy-checks. This permits on-board checking of the chip and display memory. The part, available now, is housed in 160-pin plastic quad flat packs. In large quantities, it sells for $25.

NCR Corp., Microelectronic Products Div., 2001 Danfield Ct., Fort Collins, CO 80525; (030) 226-9550. **CIRCLE 461**

■ *RICHARD NASS*

GAAS GATE ARRAYS PACK 20,000 OR 40,000 GATES

Filling in its gate-array family, Vitesse Semiconductor has released two new members of its FX gate array family, the VGFX20K and VGFX40K, which are implemented in gallium arsenide. The arrays are based on the company's 0.6-μm gallium arsenide process and a sea-of-gates architecture that makes use of up to four levels of metal interconnections.

As a result, the FX gate arrays can operate at up to four times the speed of circuits that are implemented in gate arrays built in high-speed biCMOS. A two-input NOR on the FX family has a worst-case delay of just 60 ps (unloaded) while consuming just 0.18 mW. That results in a speed-power product of 11 femtojoules, which is less than half that of biCMOS, when running at 100 MHz, and a quarter that of silicon ECL gates.

The FX20K array contains about 10,000 usable gates (or 20,000 raw gates) while the 40K arrays contain about 20,000 usable gates (or 40,000 raw gates). Both offer top-notch performance. These two chips represent the low-end of the current FX family, which has three additional members with raw gate counts of 105,000, 220,000, and 350,000.

In applications involving multiplexing and demultiplexing, internal flip-flop toggle rates can exceed 1 GHz. Mixed mode I/O pins permit the chips to tie into both ECL as well as TTL-compatible logic.

The FX20K includes 92 signal I/O pins and will typically dissipate about 3.7 W. Package options include 52- or 132-contact leaded chip carriers or a 132-lead pin-grid array. The FX40K has 152 I/O lines and might typically dissipate about 7.4 W. It will come in a 184-lead PGA package.

Prices for the arrays depend on circuit, package, and quantity. Nonrecurring engineering charges typically range from $80,000 to $120,000. Array prices range from 0.5 to 1.25 cents per used gate. Delivery of samples takes eight weeks from when the net-list is signed off.

Vitesse Semiconductor Corp., 741 Calle Plano, Camarillo, CA 93012; (805) 388-3700. **CIRCLE 462**

■ *DAVE BURSKY*

SBUS CONTROL CHIPS HANDLE 64-BIT BUSES

A pair of SBus interface control chips, the Goldchip and the SLIC, simplify SBus interfacing. The Goldchip is fully compliant with the B.0 revision of the SBus specification, while the SLIC meets the requirements of the initial SBus specification. Both chips were jointly designed by Sun Microsystems Computer Corp. and Motorola. The Goldchip, a bus-master device, supports 64-bit DMA transfers over the SBus, improving the bandwidth for data movement to 160 Mbytes/s. The SLIC is a general-purpose 32-bit programmed I/O interface for cost-sensitive moderate-bandwidth applications (up to 80 Mbytes/s). It is a bus-slave device. The SLIC responds only to requests from the CPU or other masters on the SBus. Both chips will be available in the fourth quarter of this year. The Gold chip sells for $100 in small quantities; the SLIC goes for $40.

Motorola Inc., 3102 N. 56 Street, P. O. Box 52073, Phoenix, AZ 85072; (602) 244-6900. **CIRCLE 490**

I/O CHIP ADDS 32 DMA CHANNELS TO CPUS

Able to perform 8 or 16-bit data transfers, the SC26C460 I/O processor can add 32 direct-memory-access channels to a host system. The peripheral devices that are tied to the I/O processor do not have to be designed for DMA interfaces.

As a result, systems can improve data transfer performance by moving older peripherals onto DMA channels. The 68-lead chip provides a separate memory address and length for each channel. In addtion, the I/O processor has a separate channel program entry point for each channel.

The chip has a 24-bit address bus that gives it a 16-Mbyte address space. A customized instruction set in the chip allows it to interpret peripheral status for channel selection and error checking, and data characters can be interpreted for buffer termination checking and control-sequence termination. An internal two-level interrupt queue minimizes host CPU overheads.

In single-bus systems the I/O processor can be programmed to offer the bus back to the CPU at preprogrammed intervals during data transfers. As a result, the CPU is permitted to handle urgent tasks. In 1000-unit lots the SC26C460 I/O processor sells for $18.50 apiece when it is housed in a 68-lead PLCC package. Samples are available now from stock.

Philips Components, Signetics Co., 811 E. Arques Ave., P. O. Box 3409, Sunnyvale, CA 94088; John Lavery, (408) 991-4566. **CIRCLE 491**

FASTEST DUAL AND QUAD ±15-V OP AMPS SLEW ±10 V AT 1000 V/μS

Now you can get ultra-fast/wide-band IC op amps for less that $2 per amplifier. Linear Technology's LT1229 and LT1230 (dual and quad, respectively) represent the fastest/widest-bandwidth dual and quad op amps available. Their current-feedback circuits slew the output ±10 V at up to 1000 V/μs while offering a stable, closed-loop-gain-of-one small-signal bandwidth of 100 MHz. Duals and quads in quantities of 100 cost $3.95 and $7.25 each, respectively.

These ICs are equally at home in frequency-domain and time-domain applications. When driving a doubly-terminated 75-Ω line with video and operating at a closed-loop gain of two (to pick up the 6-dB loss in amplitude), differential gain and phase run 0.04% and 0.01°, respectively. In RGB and other computer video systems, the excellent transient response elininates smearing. In fact, rise time is just 3.5 ns and settling time to 0.1%, at a closed-loop gain of one and operating from ±15-V supplies, runs 45 ns for a 10-V step, rising to 14 μs settling to 0.01%. Thus, the LT1230 quad represents a single package solution for sending RGB video down separate 75-Ω cables.

Like all current-feedback amplifiers, bandwidth does not drop in half for every doubling of closed-loop gain. At closed-loop gains of 6, 20, and 40 dB, small-signal 3-dB bandwidths run 100, 60, and 11 MHz, respectively. On the other hand, a voltage-feedback op amp with a unity-gain bandwidth of 100 MHz has small-signal bandwidth of 1 MHz at 40-dB closed-loop gain.

Unlike most ultra-fast/wideband op amps which are limited to operation from ±5-V supplies, these duals and quads can run off voltage rails to ±18 V, yet will run off voltages as low as ±2 V. However, bandwidth can drop 20 to 40 MHz as the voltage between the supply pins drops from 30 to 10 V. Minimum available output current runs 30 mA. The dual LT1229 comes in 8-pin DIPs and SOICs, the quad LT1230 in 14-pin DIPs and SOICs. They're available for commercial, industrial, and military temperature ranges. As noted, pricing for commercial devices, in hundreds, starts at $3.95 each for the LT1229 and $7.25 each for the LT1230.

***Linear Technology Corp.**, 1630 McCarthy Blvd., Milpitas, CA 95035-7487; (800) 637-5545* **CIRCLE 463**

FASTEST ±15-V IC OP AMP SPORTS 140-MHZ SMALL-SIGNAL BANDWIDTH

Aimed at handling video signals of higher-than-normal voltage with alacrity, Analog Devices' current-feedback op amp, the AD811, can put a ±10-V, 40-MHz sine wave across 100 Ω. Like all current-feedback op amps, it is unity- gain stable and its 3-dB small-signal bandwidth typically runs 140 MHz while operating at a closed-loop gain of one, higher than that of any other available IC op amp. And again, like current-feedback op amps, bandwidth does not drop off at 20 dB/decade with increased closed-loop gain. At a gain of 10, small-signal bandwidth is still 100 MHz.

The AD811 IC op amp is specified for operation from both ±15- and ±5-V rails and can easily drive not one, but two, doubly terminated 75-Ω lines. Differential gain and phase run 0.01% and 0.01°, respectively, at 4.43 MHz. THD at 10 MHz runs less than –74 dB and the third-order intercept is 43 dBm.

The op amp's time-domain specifications are in a class with its frequency-domain specifications. Slew rate for a 20-V pk-pk output, off ±15-V rails, runs 2500 V/μs, dropping to 400 V/μs for a 4-V pk-pk swing from ±5-V rails. At closed-loop gains of one, the op amp IC settles a 10-V output step to 0.1% of final value in 50 ns and just 15 ns greater to 0.01%. With ±5-V supplies, the output settles a 4-V step to 0.1% in a mere 25 ns.

The AD811 comes in 8-pin plastic and ceramic DIPs, 16- and 20-pin SOICs, and 20-pin LCCs. The commercial-grade AD811 in an 8-pin plastic DIP goes for $2.85 each in 1000s. Extended-industrial- and military-temperature-range units are also available.

***Analog Devices Inc.**, 804 Woburn St., Wilmington, MA 01887; Jay Cormier, (617) 937-2507.* **CIRCLE 464**

■ *FRANK GOODENOUGH*

SMT TRIACS HAVE LOGIC-LEVEL GATE DRIVE

Guaranteed to trigger at gate currents as low as 5 mA, the BT134W series of triacs from Philips Semiconductor can be driven directly from the outputs of logic-level devices such as CMOS microcontrollers. The elimination of special gate drive circuitry and the triacs' SOT-223 surface-mounted footprint cut component cost and printed-circuit board space, suiting the new triacs for use in a wide range of switching applications—for example, power control in lamp dimmers, voltage doubling in universal power supplies, and solenoid switching in home appliances.

The BT134W-series triacs are available with a maximum trigger threshold specification of 5 mA for the BT134W-D devices or 10 mA for the BT134W-E parts. They have a continuous current rating of 1 A rms, a peak repetitive current rating of 10 A, and a surge current specification of 10 A for 10 ms. The series includes devices with blocking voltages of 500 V and 600 V. The BT234W series triacs sell for $0.22 in quantities of 10,000. Delivery is six weeks after order.

In Europe, Philips Semiconductors, Marketing Communications. Att.: Tinus Ramaekers, P.O. Box 218, Building BAF-1, NL-5600 MD Eindhoven, The Netherlands; fax (00) 31 40 724825. In the U.S.: Philips Semiconductors, 2001 West Blue Heron Blvd., Riviera Beach, FL 33404-5099; contact: Miriam Coleman, (407) 881-3257. **CIRCLE 465**

12-BIT ADC SAMPLES 1-MHZ SINE WAVES AT 2 MHZ

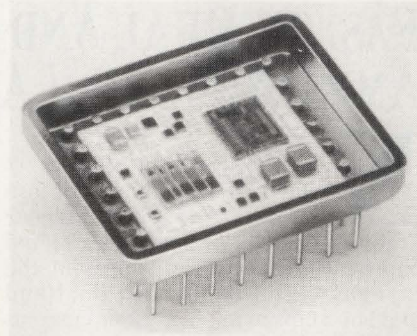
Now you can get a 12-bit ADC Datel ADS-117, which samples Nyquist-rate (1-MHz) signals at 2 MHz. Moreover, Datel guarantees all the ADS-117's dynamic specifications from dc to Nyquist. For example, while sampling at 2 MHz, spurious-free dynamic range (SFDR) runs a minimum of –75 dB, –70 dB, and –66 dB for input signals in the three frequency ranges: dc to 100 kHz, 100 kHz to 500 kHz, and 500 kHz to 1 MHz respectively. In the same ranges minimum total harmonic distortion runs -75, -68 and, -65 dB, while minimum signal to (noise and distortion) runs 68, 65, and 64 dB, respectively. In OEM quantities the commercial grade ADS-117 goes for $224 each, the military grade, $299 each.

Datel Inc., 11 Cabot Blvd., Mansfield, MA 02048; Bob Leonard (508) 339-3000. **CIRCLE 466**

SMALLEST SYNCHRO ADC YIELDS 16-BIT DATA

Called the smallest synchro/resolver-to-digital converter available, DDC's SDC-14575 offers the user 14- or 16-bit resolution. Based on a monolithic tracking design and available in 4-or-8 arc-minute accuracy grades, it has been squeezed into a metal package just 1 in. by 0.8 inches on a side. The velocity output represents a 0-to-4 V dc, 1%-linear signal replacing a tachometer output in servo loops.

Designed for use in resolver circuits, the converter takes standard 2- and 11.8-V rms inputs, while a solid-state "Scott T" circuit handles 11.8 or 90-V rms signals from synchros.

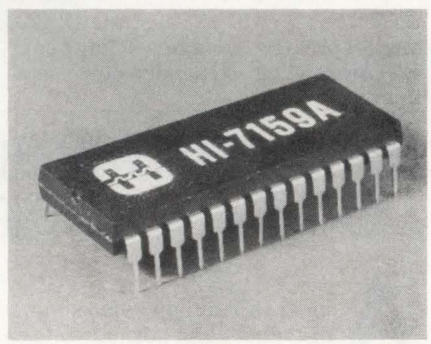


Pricing for the SDC-14575 synchro ADC converter starts at $365 each in quantities of 1 to 9.

ILC Data Device Corp., 105 Bohemia Pl., Bohemia, NY 11716; Jerry Kessler (516) 567-5600. **CIRCLE 467**

5-1/2-DIGIT ADC CHIP ADDS SERIAL I/OS

The Harris HI-7159A digital-to-analog converter can resolve input voltage changes as small as 10 μV (1 count in 200,000). The 5-1/2-digit ADC chip (ELECTRONIC DESIGN, *Jan. 10, 1991, p. 181)* now includes a pair of high-speed serial, digital I/O functions. The first, a synchronous serial interface permits data-transfer rates of up to 1 Mbit/s. The interface is directly compatible with the Intel MCS-51 family of microcontrollers.



The second new I/O is a 32-device universal asynchronous receiver/transmitter (UART) serial interface which permits hanging up to 32 HI-7159A chips on a single twisted-pair line, a natural for acquiring data from a number of sensors scattered over a large area such as a process-control plant or a seismic system.

In quantities of 1000, the HI-7159A ADC is priced at $14.34 each.

Harris Semiconductor, P. O. Box 883, Melbourne, FL 32901; (800) 4 HAR-RIS, ext. 1035. **CIRCLE 468**

LCZ METER OFFERS WIDE TEST RANGES

Broad test frequency and test signal ranges make the Model 3330 LCZ meter suitable for testing a wide variety of components. The meter also lets users make small changes in frequency and signal level, so test conditions can more closely match in-circuit conditions. The 4-1/2-digit instrument has a basic accuracy of 0.1%. Operators can select from among 201 test frequencies from 40 Hz to 100 kHz. Signal levels can be adjusted in 1-mV steps from 10 mV to 1.1 V. Three reading rates are available, the fastest being 64 ms per test. The unit has both automatic and manual triggering capability. The Model 3330 is fully programmable over the IEEE-488 bus and includes a battery-backed memory for 10 sets of front-panel settings. Additionally, an Auto mode automatically determines the type of device being characterized and displays the most likely parameters of interest. Five optional test fixtures allow a variety of devices to be connected to the meter. The Model 3330 LCZ meter costs $4590, and delivery is in 8 weeks.

Keithley Instruments Inc., 28775 Aurora Rd., Cleveland, OH 44139; (800) 552-1115 or (216) 248-0400. **CIRCLE 469**

GRAPHICAL TEST GENERATOR UPGRADED

WaveTest 4.0, the latest version of the graphical test program development system, offers a number of significant enhancements. As a Microsoft Windows 3.0 application, WaveTest 4.0 lets users share data with other applications using the Windows 3.0 dynamic data exchange standard. Also, test developers can quickly create interactive operator panels by choosing and graphically placing predefined controls. The instrument search and replace feature lets users quickly modify existing test programs to accept new instruments. Reports can be created like operator panels, using report controls such as graphs, tables pictures, and text. The software includes more than 200 instrument drivers. WaveTest 4.0—including a program generator, library generator, and two runtime systems—costs $1995. An upgrade kit for WaveTest 3.0 users costs $495. Delivery is in 4 to 6 weeks.

Wavetek San Diego Inc., 9045 Balboa Ave., San Diego, CA 92123; (619) 279-2200. **CIRCLE 470**

KITS LINK MAC II, QUADRA TO VXIBUS, VMEBUS

The VXI-NB2040 and VME-NB2040 interface kits connect the Macintosh Quadra and Macintosh II computers to the VXIbus and VMEbus, respectively. The VXI-NB2040 makes the computers perform as though they were plugged directly into the VXI backplane, giving them full slot 0, resource manager, and commander capability. The kit includes a circuit board that plugs into the Macintosh NuBus slot and a C-size slot 0 module. Similarly, the VME-NB2040 links the computers to the VMEbus, allowing them to perform as though they were plugged into the VME backplane. The kit contains a full-size NuBus board and a 6U-size VME module. In both cases a 2-m MXIbus cable connects the computers to the backplane. Both packages include extensive software support for programming in C or LabView 2. The VXI-NB2040 costs $4000, and the VME-NB2040 goes for $3400. Both are available immediately.

National Instruments Corp., 6504 Bridge Point Pkwy., Austin, TX 78730-5039; (800) 433-3488 or (512) 794-0100. **CIRCLE 472**

SCOPE PLUG-INS STORE 1 MILLION SAMPLES

Two plug-in units for the LeCroy 7200 series oscilloscopes offer acquisition memories of up to 1 million samples. The Model 7242B is a two-channel module with a standard 200-ksample or optional 1-Msample per channel memory. With two 7242B plug-ins installed, the 7200 scope features two channels of simultaneous 2-Gsample/s digitizing or four channels of 1-Gsample/s acquisition. With the long-memory option installed, the Model 7234 plug-in offers the user several choices: up to 1-Msample acquisition on one channel, up to 500,000 samples with two channels active, or up to 200,000 samples per channel on four channels. Two 7234s permit eight channels of 200-Msample/s digitizing. By segmenting the memories in the 7242B and 7234, users can acquire up to 5000 waveforms at high trigger rates. With the 1-Msample memories, the 7242B and 7234 cost $22,900 and $19,500, respectively. A Model 7200 scope is $17,000. Delivery is in 6 weeks.

LeCroy Corp. 700 Chestnut Ridge Rd., Chestnut Ridge, NY 10977-6499; (800) 553-2769 or (914) 425-2000. **CIRCLE 473**

SOLID-STATE 1.8-IN. DISK DRIVE ACCESSES IN LESS THAN 1.6 MS

Standing in for IDE-interface 1.8-in. mechanical disk drives, the SDI series of solid-state (flash-memory based) disk drives trims access time under 1.6 ms and offers data-transfer rates of 2.5 Mbytes/s (burst transfers from the drive). The drives, jointly developed by SunDisk and AT&T Microelectronics, pack 2.6 to 40.9 Mbytes of nonvolatile storage. They weigh just 1.2 or 1.6 oz—for under 20 Mbytes or over 20 Mbytes, respectively—making them the lightest high-capacity storage devices yet for portable systems.

The drives operate over 0 to 60 °C and handle 15 G (pk-pk) of vibration and up to 500 G of shock. When powered, they draw just 3 mA in their sleep mode, just 100 mA when reading data, and 200 mA when writing or erasing files. Start-up time is less than 20 ms to go from the sleep state to writing data, and less than 3 ms from sleep to read. Data transfers to or from the memory are in bursts of up to 20 Mbits/s. Data moves over the IDE interface at 3.75 Mbytes/s (also in bursts). Command overhead (data to data request) in the controller is less than 1.5 ms.

Drive MTBF is specified at 200,000 hours and less than 1 non-recoverable error in 10^{13} bytes read. The drive is just 3-by-2-in. by either 0.28- or 0.38-in. thick (under 20 Mbytes or over 20 Mbytes, respectively). Capacities of 2.6, 5.2, 10.4, 20.9, and 40.9 Mbytes are available.

Samples, available now, cost from $690 for the smallest to $8000 for the 40.9-Mbyte unit. SunDisk will also alterate-source the PCMCIA-compatible memory cards and controller card AT&T recently released.

***SunDisk Corp.**, 3270 Jay St., Santa Clara, CA 95054; John Reimer, (408) 562-0500.* **CIRCLE 474**

■ *DAVE BURSKY*

FLASH FILE STORAGE EMPLOYS PCMCIA FORMAT

Optimized for use in portable computer and instrumentation systems, the flash file memory-card system jointly developed by AT&T Microelectronics and SunDisk Corp. initially provides 2.5 to 10 Mbytes of nonvolatile flash-memory-based removable storage. The system consists of a two-card approach—a combination controller and IDE interface card (ATTCB-IDE-12) in a 2.5-in. hard-disk-drive format, and a PCMCIA-compatible memory card that can plug into a PCMCIA connector.

The memory cards have capacities of 2.5, 5, and 10 Mbytes (ATTMCF4-02, 05, 10) and permit at least 100,000 erase and write cycles. The company also expects to have 20- and 40-Mbyte cards ready to sample by late 1992 and early 1993, respectively.

The controller card is typically embedded in the host system (a notebook computer or portable instrument) and turns the user-removable standard PCMCIA memory cards into solid-state disk drives by managing all the storage control functions. Typical access time is 1.5 ms to read, and start-up times are just 3 ms to read and 20 ms to write or erase data.

Data transfers can be done at rate of 500 kbytes/s when reading and 50 kbytes/s when writing. Under typical conditions the average power consumption is less than 20 mW; peak power levels reach 1050 mW during write and erase cycles and 788 mW during seek and read operations. During the sleep periods, power drain drops to 16 mW, maximum.

The IDE controller card measures 4-by-2.75-by-0.6 in. and interfaces to one or two File Flash memory cards. Two memory cards can be plugged in and simultaneously be active.

The 2.5-, 5-, and 10-Mbyte memory cards sell for $415, $750, and $1375 apiece, respectively, while the controller card sells for $225 each. All prices are for orders of from 1 to 25 cards. SunDisk Corp., Santa Clara, Calif. will alternate-source the memory and controller cards.

***AT&T Microelectronics Inc.**, 555 Union Blvd., Allentown, PA 18103; Charles Hochstedler; (215) 439-5462.* **CIRCLE 475**

■ *DAVE BURSKY*

CIRCUIT BOARD DESIGN TOOLS DOUBLE THEIR CAPACITY

The latest version of P-CAD's Associate Designer pc-board tools double their capacity and increase graphics speed by up to 50%. Version 2.0 includes an interactive pc-board layout editor, component library, utilities, and CAM interfaces. New features include blind- and buried-via support, enhanced polygon support, global component replacement, simultaneous multilayer routing, 45° beveling, and improved routing speed. Associate Designer 2.0 runs on personal computers and is available now for $1995. The price goes to $2795 when the software is bundled with the router, placer, and CAM interfaces.

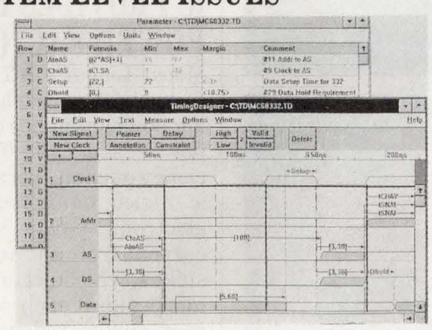
P-CAD, 1290 Parkmoor Ave., San Jose, CA 95126; (408) 971-1300. **CIRCLE 476**

PC-BASED TOOL DOES BOTH ANALOG AND DIGITAL DESIGN

Design Center is a PC-based software environment that engineers can use to capture, simulate, and analyze analog, digital, or mixed-signal circuits. It simplifies the engineer's job by allowing simulation and analysis to take place within the circuit-drawing environment. The analog and digital algorithms are tightly coupled within the same program. Consequently, the engineer need define only one circuit and run only one simulation. In addition, only one graphical interface is required to analyze the results of a mixed-signal circuit. Drawings are created and edited from device and signal libraries containing over 5700 analog and digital components. Engineers can also define custom devices and symbols to suit individual applications. Three Design Center configurations range in price from $2450 to $29,900.

MicroSim Corp., 20 Fairbanks, Irvine, CA 92718; (800) 245-3022. **CIRCLE 477**

TIMING-DIAGRAM ANALYSIS TOOL LOOKS AT SYSTEM-LEVEL ISSUES

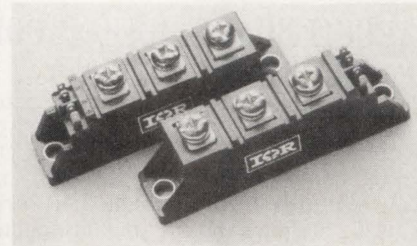


The second major upgrade to the TimingDesigner software extends its capabilities to include system-level problems. TimingDesigner is a software tool that automates timing-diagram entry and analysis to help engineers specify, modify, and check timing requirements for digital circuits. This newest version 1.25 adds three major new features. The most important of these features is the ability to extend the timing range, allowing engineers to model events that occur in slower circuits, system-level events, or events that occur in non-electrical applications, such as in an industrial programmable controller. The other two features are improved graphics speed and the ability to override the calculated maximum or minimum delay values with known guaranteed values. TimingDesigner Version 1.25 runs on PCs under MS Windows. It's shipping now for $995.

Chronology Corp., 2721 152nd Ave. NE, Redmond, WA 98052-5516; (206) 869-4227. **CIRCLE 478**

IGBT HALF BRIDGES SWITCH 600 V AT 90 A

Now you can get International Rectifier's fast and ultra-fast high-current, 600-V IGBTs (insulated-gate bipolar transistor) in industry-standard modules. Each module holds a complete half bridge including a fast-recovery snubber (free-wheeling, catch) diode in parallel with each of the modules two IGBTs. Units containing fast IGBTs are rated at 50 and 90 A. They can perform hard switching at up to 10 kHz and operate in resonant circuits up to 60 kHz. The ultrafast modules are rated



at 35 and 65 A. They can perform hard switching at up 25 kHz and resonant operation extends to 100 kHz. At rated current saturation voltage of the fast IGBBTs runs a maximum of 2.1 V while that of the ultrafast devices runs 3.1 V. In quantities of 100 these modules are priced between $56 each and $85 each.

International Rectifier Corp., 233 Kansas St., El Segundo, CA 90245; Tim McDonald (800) 245-5549. **CIRCLE 479**

15-W CONVERTERS HAVE UP TO THREE OUTPUTS

Single, dual, or triple outputs are offered in the MT Series of dc-dc converters. The 15-W units boast an ultra-wide input-voltage range of 9 to 36 and 20 to 72 V dc. Packaged in a compact 2.0-by-2.0-by-0.4-in. shielded, surface-mountable case, the converters have a typical efficiency of 85%. Most popular output voltages are available in many combinations. Pricing is less than $50 in OEM quantities. Delivery is from stock.

Astec, 401 Jones Rd., Oceanside, CA 92054; (619) 757-1880. **CIRCLE 480**

IC PROVIDES BEST-YET POWER-FACTOR

Micro Linear's ML4821 power-factor-correction controller can build switching power supplies offering the highest power factor yet, 0.99, upping the efficiency of computers and other electronic office equipment. Most standard electronic power supplies take their current from the ac power line in huge spikes, which occur at the plus and minus peaks of each sine wave. These current spikes reduce the power factor seen by the line from 1.00 to as little as 0.65, causing two problems: It reduces the power available from a given line (wall outlet) by 35% and increases the current flowing through the neutral wire, a potential fire hazard. Unlike earlier similar ICs, the ML4821 also offers over-voltage protection, as well brown-out control and synchronization. In its 18-pin DIP it goes for $3.55 each in quantities of 100.

Micro Linear Corp., 2092 Concourse Dr., San Jose, CA 95131; Jon Klein, (408) 433-5200. **CIRCLE 481**

GRAPHICS CARD GIVES PC WORKSTATION LOOK

Based on a 60-MHz version of the TMS34010 graphics processor from Texas Instruments, the XHR Gemini 10 graphics card accelerates both pixel- and vector-oriented graphics applications over standard VGA graphics controllers. That makes the card an attractive solution for users of Microsoft's Windows graphical user interface as well as applications such as AutoCAD and AutoShade. The AT-bus compatible card, aiming for maximum flexibility, includes a software programmable dot-clock generator. Thus, the card can be configured in software for 1, 2, 4, 16, or 256 colors. It can be optimized to maximize the resolution or refresh rate for either 2D or 3D applications. The card, which can also be configured for true-color applications (24-bits/pixel) and includes digital VGA loop-through, sells for $1275 each in single units.

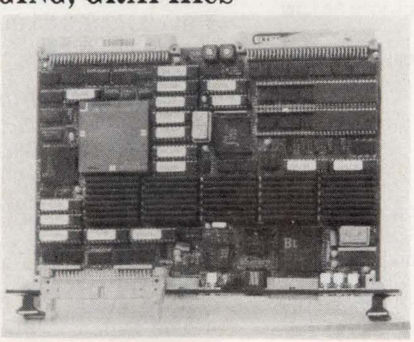
ELSA America Inc., 400 Oyster-Point Blvd., Suite 109, South San Francisco, CA 94080; Walter Haefeker, (415) 588-6285. **CIRCLE 482**

6U VME SINGLE BOARD COMPUTER BUILT WITH R3000

The RISQengine/5e is a Mips R3000-based VME single-board computer (SBC). The 25-, 33-, or 40-MHz RISC processor comes with 8 kbytes of instruction cache and 2 kbytes of data cache. The board's standard configuration includes up to 32 Mbytes of two-way interleaved DRAM, 256 kbytes of EPROM (expandable to 1 Mbyte), a resident PROM monitor, a high-speed DMA controller, a real-time clock, and three counter-timers with interrupt capability. Ethernet, SCSI, and other I/O functionality are available as RISQmodules on the company's proprietary on-board mezzanine bus. The VxWorks real-time operating system is ported to the board, which is available now. Prices start under $3000.

RISQ Modular Systems Inc., 39899 Balentine Dr., Suite 200, Newark, CA 94560; (415) 490-0732. **CIRCLE 483**

68040-BASED VME BOARD COMBINES IMAGING, GRAPHICS



The IC40 68040-based VME board combines imaging and graphics capabilities. The board's frame grabber digitizes composite video inputs from up to four standard video cameras in real-time, and can display the images on high-resolution monitors without interlace flicker. Because the monitor sychronization raster is independent of the video timing, line-scan cameras can be used for input. The output can be used for simultaneous display of menus and up to four video frames, allowing users to interact with one display of live and stored video. Programmable resolution can display up to 1280 by 1024 pixels at 60 Hz, noninterlaced. Image memory is eight bit planes deep, resulting in 256 simultaneous colors from 16.7 million. The IC40 is available now for $5100.

American Eltec Inc., 4340 Stevens Creek Blvd., San Jose, CA 95129; (408) 244-4700. **CIRCLE 484**

VERTICAL 4-MBIT DRAM PACKAGE BOOSTS MEMORY DENSITY

An innovative package enables OEMs to squeeze 32 Mbytes of RAM—or 64 packages—into a credit-card-size area on a circuit board. The vertically mounted VPAK package is extremely thin and can be surface mounted in an automatic process. The first IC in the new package is TI's 4-Mbit DRAM.

The VPAK package maximizes use of pc-board area because the device

stands upright rather than lying flat. Up to seven times more RAM can fit in a given area than with memories conventionally packaged in DIPs, small-outline J-lead packages, or thin small-outline packages. Even when considering volume, the VPAK package is still about twice as efficient as conventional packages.

Not only that, but the VPAK package offers higher density even when compared with other vertical packages. The VPAK is less than half the thickness of a zig-zag in-line package (ZIP), the standard vertical package.

The 4-Mbit DRAM's pinout is arranged in the same sequence as its ZIP equivalent to make it easy for manufacturers to switch over to the VPAK device. Other features include L-shaped leads, which help ensure strong solder bonds. Also, specially designed posts help insertion equipment accurately position the device on pc boards.

The 4-Mbit DRAM VPAK comes in organizations of 4 Mbit by 1 (TMS44100RVA) and 1 Mbit by 4 (TMS44400RVA). Both come with access times of 60, 70, and 80 ns. Pricing starts at $23.25 for the 80-ns part in lots of 1000. Samples will be available in the first quarter.

Texas Instruments Inc., Semiconductor Group, *SC-91064, P. O. Box 809066, Dallas, TX 75380-9066; (800) 336-5236, ext. 700.* **CIRCLE 485**

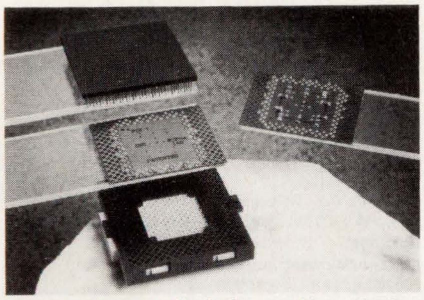
■ *DAVID MALINIAK*

PC-BOARD FASTENERS EXPAND BY THEMSELVES

The Type KPS fasteners are simply inserted into the plated-through holes in multilayer pc boards and squeezed with a flat anvil and punch until the shank expands outward and the nut's knurls make contact with the board. The reverse side remains flush. Thread sizes are available from # 4-40 to 10-32 in various head heights. Call for pricing and delivery information.

Penn Engineering & Mfg. Corp., P. O. Box 1000, Danboro, PA 18916; (800) 237-4736. **CIRCLE 486**

DECOUPLING DEVICE CUTS SOCKET DELAYS



An easily installed decoupling device mates with AMP Inc.'s TAZ interstitial PGA socket to improve EMI suppression, minimize parasitic inductance, and hold down signal delays. The unit plugs in between the pin-grid array and socket and provides direct-to-V_{CC} and direct-to-V_{SS} lead decoupling. The multifinger contact also lends itself to machined pin-socket and wire-wrap applications. Call for pricing and delivery information.

Concept Mfg. Inc., 43024 Christy St., Fremont, CA 94538; (510) 651-3804. **CIRCLE 487**

SSOP PACKAGE HOUSES COMMUNICATION ICs

A line of personal communication ICs will soon be available in the shrink small outline package, the world's smallest 20-pin package for this type of IC. With a pc-board footprint of only 4.5 by 6.75 mm, the SSOP occupies a mere one-third of the board space required by such predecessors as the small-outline large (SOL) package. In addition, its 1.5 mm height makes it thinner, a key advantage in space-sensitive applications such as cordless telephones, pagers, and pocket wireless systems.

The first products in the space-saving SSOP package Philips will offer are the NE/SA575DK low-voltage compandor and the NE/SA605DK/615DK high-performance low-power FM IF system ICs, allowing designers currently using the SOL versions to miniaturize equipment without changing the circuit design. The SSOP NE/SA575DK allows designers to build automatic level control into equipment such as hearing aids, using conventional mounting methods instead of die bonding. The NE/SA575DK compandor, which features a precision dual-gain control circuit and low supply voltage operation, can be used to reduce noise and boost dynamic range in audio and radio communication tasks. The NE/SA605DK/615DK FM IF system IC incorporates a mixer, oscillator, IF and limiter amplifiers, plus a quadrature detector, mating circuit, logarithmic received-signal-strength indicator and voltage regulator. Contact the company for prices.

In Europe, Philips Semiconductors, Marketing Communications. Attn.: Tinus Ramaekers, P. O. Box 218, Building BAF-1, NL-5600 MD Eindhoven, The Netherlands; fax (00) 31 40 724825. In the U. S., Philips Semiconductors, 2001 West Blue Heron Blvd., Riviera Beach, FL 33404-5099; contact: Miriam Coleman, (407) 881-3257. **CIRCLE 488**

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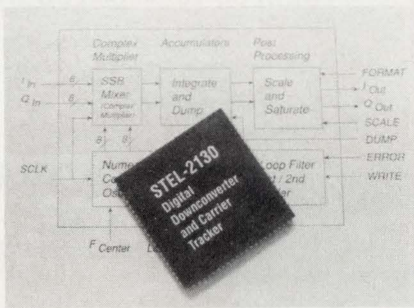
The CMOS IC can perform the last down-conversion from a digitized i-f



signal and includes filtering that previously would be integrated as a separate chip. The combination of functions on the STEL-2130 eliminates the need for high-speed and expensive DACs, mixers, and filters between the carrier tracking, the numerically controlled oscillator (NCO), and the complex multipliers for analog technology.

Within the STEL-2130 is a digital i-f sampler that operates at up to 40 MHz with either I/Q pairs for wide bandwidth requirements, or with a single input stream for narrow-band inputs. The complex multiplier operates on complex 8-bit data inputs at up to 40 MHz data throughput. Quantized 9-bit complex summed products are delivered by the block as inputs to succeeding 18-bit I/Q integrate and dump filters. The NCO has 32 bits of frequency resolution, includes a 10-bit phase/8-bit amplitude look-up table, and provides quadrature (sine and cosine) waveform generation with sidelobes down more than 55 dBc. All sections of the circuit can also operate at frequencies of up to 40 MHz. In thousands the STEL-2130 comes in an 84-pin, 1.2-in. square leaded chip carrier and sells for $55 apiece. Samples are available now.

***Stanford Telecommunications Inc.**, 2421 Mission College Blvd., ASIC Div., San Jose, CA 95056; (408) 748-1010.* **CIRCLE 489**

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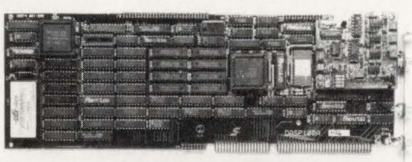

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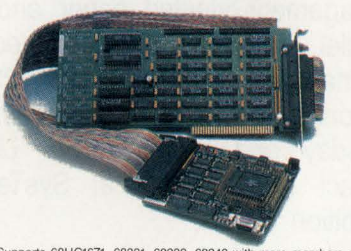

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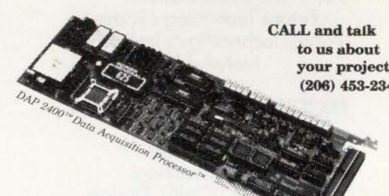

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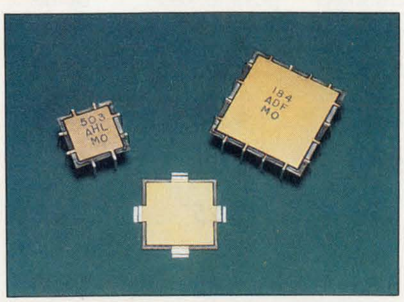

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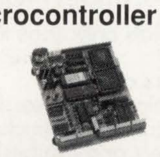

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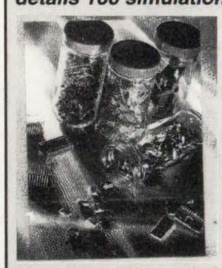

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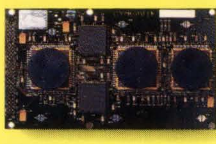

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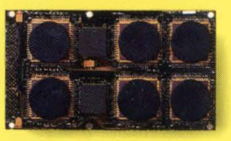

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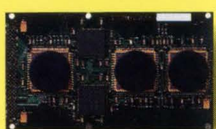

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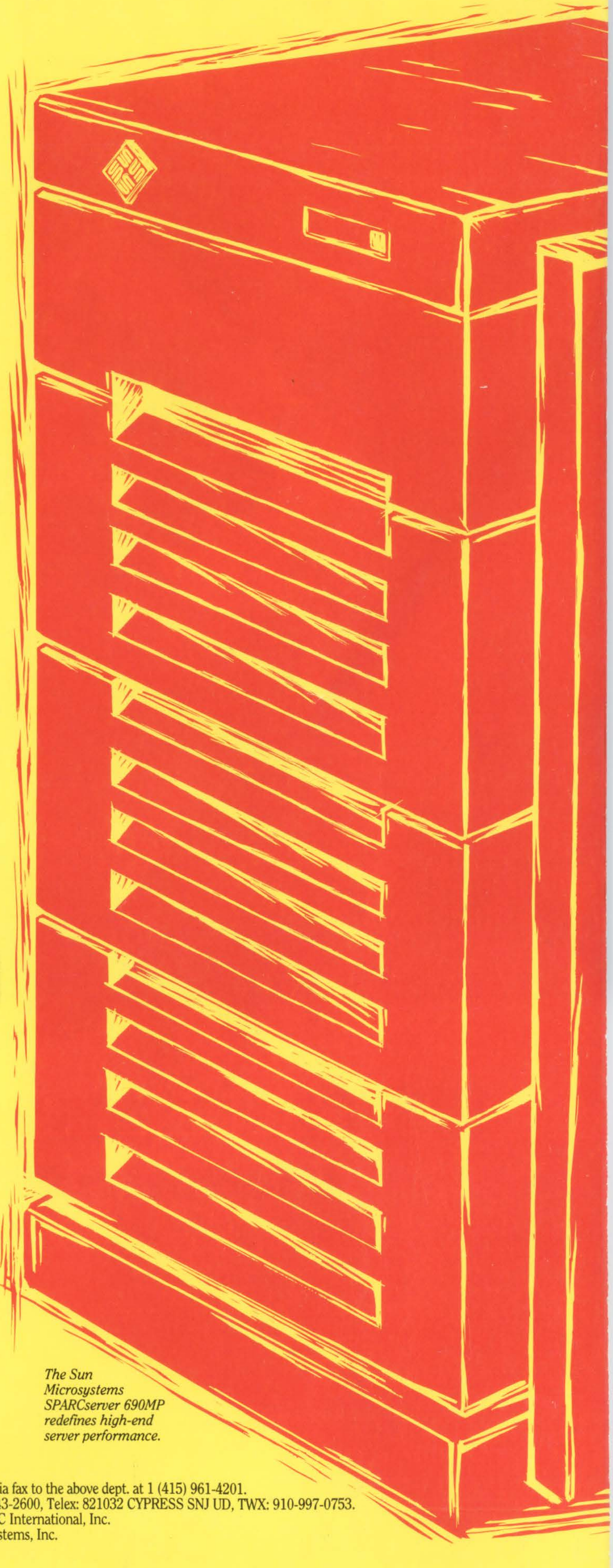

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