ADAPTEC

ACB 4000 AND 5000 SERIES DISK CONTROLLERS

OEM MANUAL

1.0 INTRODUCTION

The ADAPTEC 4000 and 5000 Series Disk Controller boards are a family of products which interface Winchester disk drives to any ANSC X3T9.2 SCSI (Small Computer System Interface) standard host adapter interface.

1.1 BASIC DESCRIPTION

1.1.1 ACB-4000

The 4000 series supports minimum SCSI features and controls two Seagate ST-506/412 or equivalent Winchester drives. Most of the currently available drives are supported through the Mode Select Command.

1.1.2 ACB-5000

The 5000 series supports full SCSI features plus extensions. The Model 5500 controls four drives of the Seagate ST-506 type. The 5800 series controls four Shugart SA-1000 or Quantum Q2000 style drive interfaces. A capabilities comparison between the two ACB controller types is shown in Table 2-1.

1.2 FEATURE SET

A) All ADAPTEC controllers have a 1KByte FIFO data buffer which is dual ported for rapid data transfers. No sector interleaving is required.

B) Controllers offer complete device independence.

C) Disk defect handling is on a sector level and is transparent to the host.

D) All controllers utilize a 32 bit ECC and provide correction of single burst errors of 8 bits. All ID and data fields are ECC protected.

E) ADAPTEC controllers use logical sector addressing and variable sector lengths are programmable at format time.

F) High speed data search is supported.

G) The 5000 series supports command chaining and disconnect/reconnect.

H) All ACB controllers support multiple host and multiple controller systems.

FUNCTION	ADAPTEC 5000	ADAPTEC 4000
HOST INTERFACE		
Full SCSI	yes	Min.SCSI+ext
Data Lines	8+parity	8
CMD Lines	9	9
Data Buffer - type	Dual Port FIFO	Dual port FIFO
- size	1K Bytes	1K Bytes
Data Rate, MBytes/sec	1.5	1.5
Bus Contention Handling	yes	yes
Disconnect/Reconnect	yes	no
Target Addressing	8 targets	8 targets
LUN Addressing	4 devices	2 devices
Sector Interleaving	Programmable	Programmable
PROGRAMMING CONSIDERATIONS		
Block Size, bytes	any size(min 256)	256,512,1024
Logical Block Addressing	21 or 32 bit	21 or 32 bit
Multiple Block Transfer	Max 64k blks	Max 64k blks
High Speed Data Search	yes	yes (full block)
Implied Seek & Verify	yes	yes
Command Chaining	yes	no
Disconnect/Reconnect	yes	no
Device Independance	yes	yes
Transparent Formatting	yes	yes
Reserve & Release Unit	yes	no
Automatic Cyl/Head Switch	yes	yes
DATA INTEGRITY		
ECC	32 bit ECC	32 bit ECC
Error Correction	8 bit burst	8 bit burst
Disk Defect Handling	yes, by block	yes, by block
Buffer Memory Parity	yes	no
DISK INTERFACE		
No. of Devices	4	2
Max Data Rate, Mbits/sec	10	5.0 standard
Compatibility	Seagate ST412 Shugart SA1000 Quantum Q2000	Seagate ST506,412 (Any with ST-506 interface)
Board Size, inches	5.75 X 7.75 8 X 9 (ACB-5800)	5.75 X 7.75

Table 1-1. ADAPTEC Controller Capabilities

2.0 PHYSICAL SPECIFICATIONS

2.1 SIZE

	4000 & 5500 Series	5800 Series
Length	7.75 inches (19.7 cm)	8.0 inches (20.3 cm)
Width	5.75 inches (14.6 cm)	9.0inches (22.9 cm)
Height	.75 inches (1.9 cm)	
Weight	1 pound, with packaging	

2.2 POWER REQUIREMENTS

2.2.1 ACB 4000 and 5500 Series

+5VDC ± 5% at 1.5 Amps (Max)
+12VDC ± 5% at 300 mA (Max)

Power is applied through J 3, 4 pin AMP connector. The recommended mating connector is AMP P/N 1-480424-0. J6 pins are numbered as shown in Figure 2-1.

2.2.2 ACB 5800 Series

+5VDC ± 5% at 1.5 Amps (Max)
-5VDC ± 5% at 0.5 Amps (Max)

Power is applied through J6, 6 pin AMP connector. The recommended mating connector is AMP P/N 1-480270-0. J6 pins are also shown in Figure 2-1.

ACB-4000 & 5500 ACB-5800

Figure 2-1. Connector J6 Pin Assignments

2.3 ENVIRONMENTAL LIMITS

	Operating	Storage
Temperature F/C	32/0 to 131/55	-40/-40 to 167/75
Humidity(non-cond)	10% to 95%	10% to 95%
Altitude, ft.	Sea Level to 10,000	Sea Level to 20,000

3.0 HOST AND DRIVE INTERFACES

3.1 HOST ADAPTER INTERFACE - Signals

The ADAPTEC 4000 and 5000 series controllers interface to a host adapter according to the proposed ANSC X3T9.2 Standard (SCSI). The data bus is a bidirectional 8 bit parallel interface, with parity supported on the ACB-5000.

A 50 pin flat ribbon connector is provided at J4. The 3M P/N 3425-3000 cable connector is recommended.

Single ended drivers and receivers allow a maximum cable length of 20 feet (6 meters) between the host adapter and the controller. All signals are low true. All odd pins are grounded. Figure 3-1 shows the SCSI bus pin assignments.

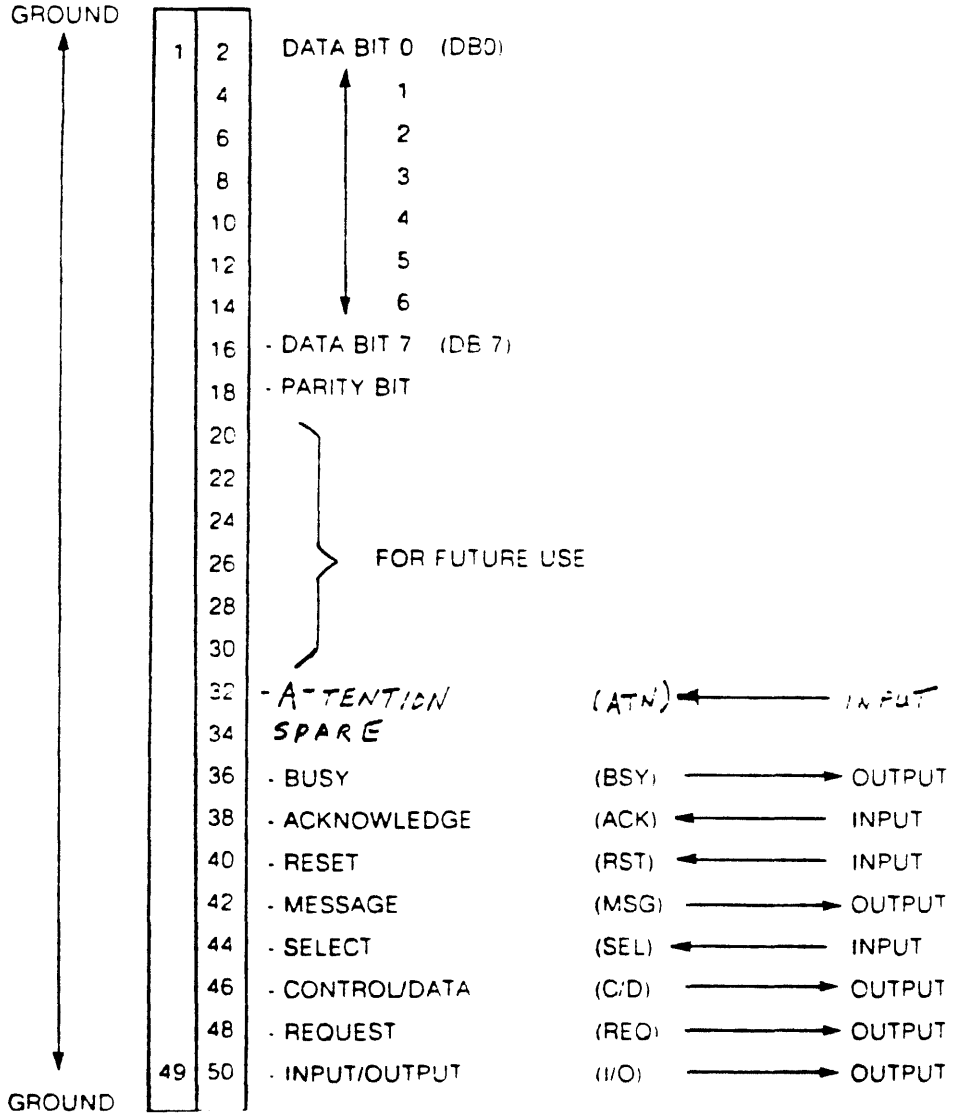


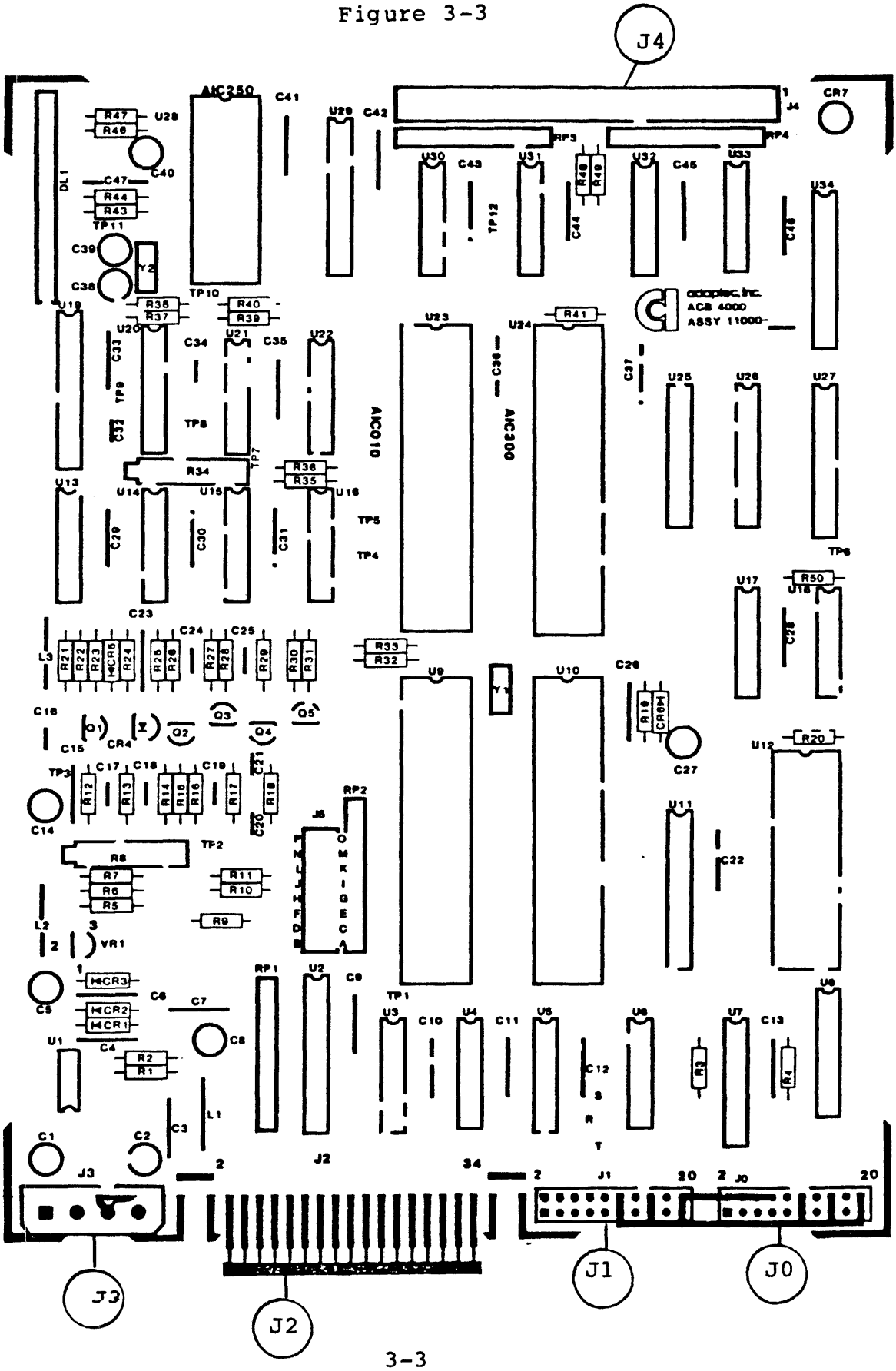
FIGURE 3-1. SCSI Bus Pin Assignments

ACB-5500 Board Layout and Connectors

Figure 3-2

ACB-4000 Board Layout and Connectors

Figure 3-3



ACB-5800 Board Layout and Connectors

Figure 3-4

3.2 HOST ADAPTER INTERFACE - Electrical

All signals are low true and use open collector drivers terminated with 220 Ohms to +5 volts (nominal) and 330 Ohms to ground at each end of the cable.

Each signal driven by the controller has the following output characteristics:

True = Signal Assertion = 0.0 to 0.4 VDC @ 48 mA(sinking)
False = Signal Non-Assertion = 2.5 to 5.25 VDC

ADAPTEC controllers use a 7438 open collector driver to meet this specification.

Each signal from the host to the controller must have the following characteristics:

True = Signal Assertion = 0.0 to 0.8 VDC @ .4 mA (max)
False = Signal Non-Assertion = 2.0 to 5.25 VDC

A 74LS14 receiver with hysteresis meets this specification.

Figure 3-5 shows an example of proper bus termination.

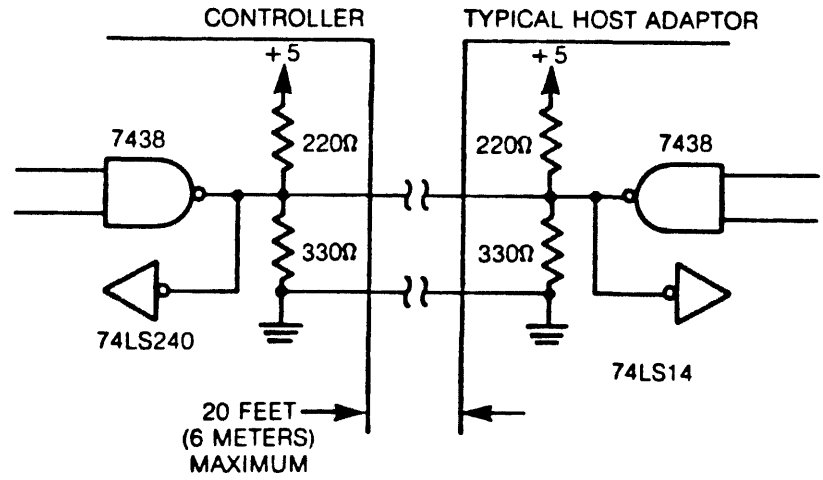


Figure 3-5. Host Adapter Bus Termination

3.3 DISK DRIVE INTERFACE - Signals

ACB 4000 and 5500 controllers comply with the standard ST-506/412 interface, while the 5800 matches the Shugart SA1000 specification.

A system interconnect diagram is shown in Figure 3-6. ACB board layouts for connector positioning are shown in Figures 3-2,3 & 4.

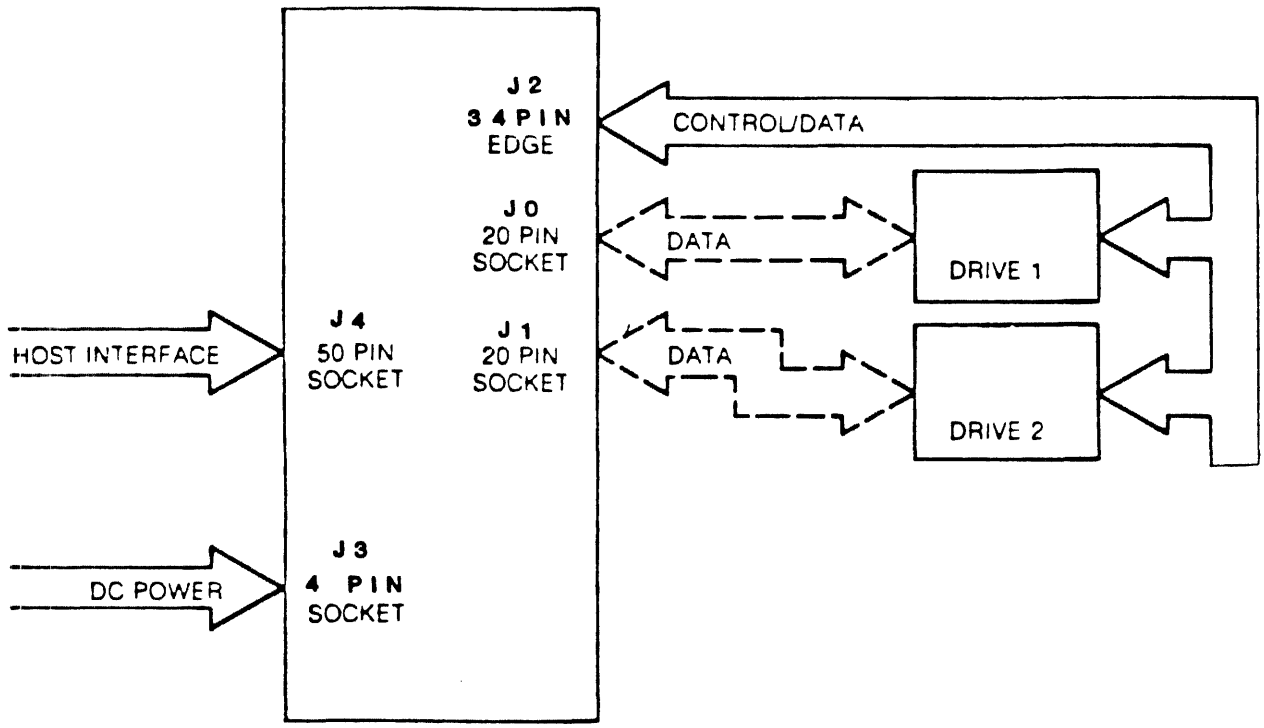


Figure 3-6. System Interconnect Diagram

3.3.1 ACB 4000

J2 is a 34 pin edge connector to which all drive control lines are daisy chained. Maximum cable length is 20 feet (6 meters). The suggested mating connector for this ribbon cable is 3M P/N 3402-0000.

The pins are numbered 1 through 34 with the even pins located on the component side of the controller board. Pin 2 is the pin closest to the power connector (J6). Table 3-1 shows pin assignments for connector J2.

J0 and J2 are the radial data connectors to each disk drive. Maximum cable length should not exceed 20 feet (6 meters). Suggested mating sockets for these connectors is 3M P/N 3421 Series. Table 3-2 shows J0 and J2 data bus pin assignments.

Table 3-1 CONNECTOR PIN ASSIGNMENT

GND RTN PIN	SIGNAL PIN	SIGNAL NAME
1	2	-RED WR CUR/HD 2^3
3	4	-HEAD SELECT 2^2
5	6	-WRITE GATE
7	8	-SEEK COMPLETE
9	10	-TRACK 0
11	12	-WRITE FAULT
13	14	-HEAD SELECT 2^0
15	16	RESERVED
17	18	-HEAD SELECT 21
19	20	-INDEX
21	22	-READY
23	24	-STEP
25	26	-DRIVE SELECT 1
27	28	-DRIVE SELECT 2
29	30	-DRIVE SELECT 3
31	32	-DRIVE SELECT 4
33	34	-DIRECTION IN

Table 3-2 -CONNECTOR PIN ASSIGNMENT

GND RTN PIN	SIGNAL PIN	SIGNAL NAME
2	1	- DRIVE SELECTED
4	3	RESERVED
6	5	RESERVED
8	7	RESERVED
	9, 10	RESERVED
12	11	GND
	13	+ MFM WRITE DATA
	14	- MFM WRITE DATA
16	15	GND
	17	+ MFM READ DATA
	18	- MFM READ DATA
20	19	GND

3.3.2 ACB 5800

J5 on this board is a 50 pin edge connector for daisy chained drive control lines. Its maximum cable length is also 20 feet (6 meters). The suggested mating connector for this ribbon cable is 3M P/N 3415-0001.

The pins are numbered 1 through 50 with the even pins located on the component side of the controller board. Pin 2 is the pin closest to the power connector (J6). Table 3-3 shows pin assignments for J5 on the ACB 5800.

Connectors J0-J3 are the radial data connectors to each 8" drive. Again, their maximum lengths are 20 feet. Suggested mating sockets for these connectors is 3M P/N 3421 Series. Table 3-4 shows J0-J3 data bus pin assignments.

1	2	- IW SWITCH
	4	Head SEL 2[2]
	6	
	8	- SEEK COMPLETE
	10	
	12	
	14	- HEAD SEL 2[3]
	16	
	18	- HEAD SEL 2[1]
	20	- INDEX
	22	- READY
	24	
	26	- DRIVE SEL 1
	28	- DRIVE SEL 2
	30	- DRIVE SEL 3
	32	- DRIVE SEL 4
	34	- DIRECTION SEL
	36	- STEP
	38	
	40	- WRITE GATE
	42	- TRACK 000
	44	- WRITE FAULT
	46	
	48	
49	50	

Table 3-3

- DRIVE SELECTED	1	2	GROUND
	3	4	
	5	6	
	7	8	GROUND
+ TIMING CLOCK	9	10	- TIMING CLOCK
GROUND	11	12	GROUND
+ MFM WRITE DATA	13	14	- MFM WRITE DATA
GROUND	15	16	GROUND
+ MFM READ DATA	17	18	- MFM READ DATA
GROUND	19	20	GROUND

Table 3-4

3.4 DISK DRIVE INTERFACE - Electrical

The last physical drive on the control bus daisy chain must be terminated with a resistor pack provided by the drive manufacturer. The control signal driver/receiver electrical specifications are shown in Figure 3-7.

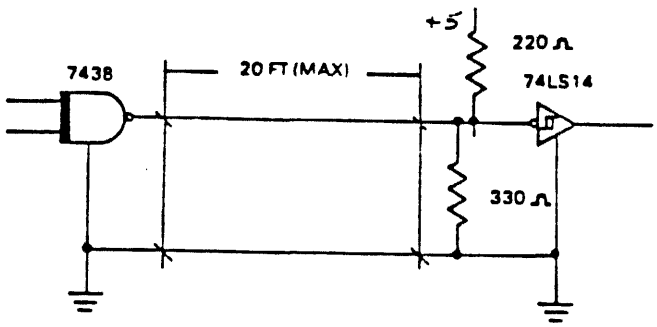


Figure 3-7. Control Driver/Receiver Lines

The control signals are specified at:

True = 0.0 VDC to 0.4 VDC @ 1 = -48 mA (Max)
False = 2.5 VDC to 5.25 VDC @ 1 = +250 uA (Open Collector)

The read and write MFM data lines are differential signals, present on connectors J0 through J3. The ADAPTEC receiver/driver pairs meet the required RS 422 specifications. Figures 3-8 and 3-9 show these lines for the ACB 4000/5500 and the ACB 5800 systems.

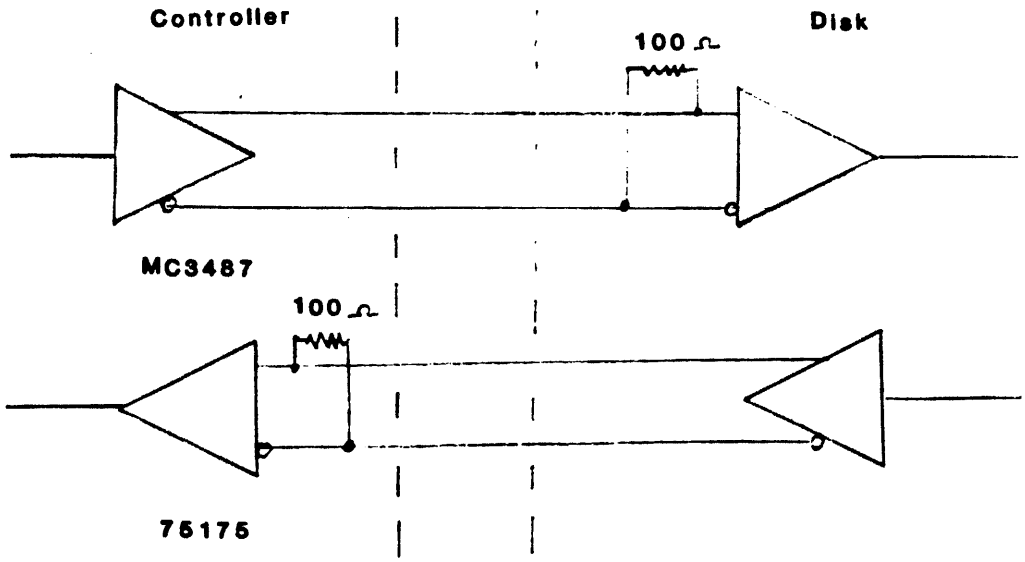


Figure 3-8. ACB 4000/5500 Data Receiver/Driver Pairs

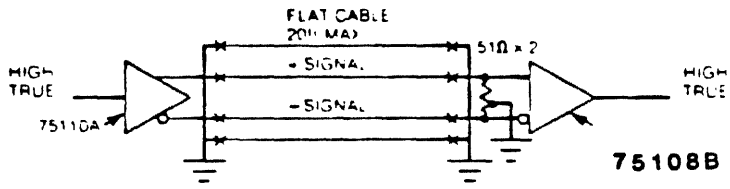


Figure 3-9. ACB 5800 Data Receiver/Driver Pairs

4.0 HOST INTERFACE PROTOCOL

4.1 ACB 4000 AND 5000 DIFFERENCES

This section describes in detail the SCSI protocol with extensions. Only the ACB-5000 series of ADAPTEC controllers conform to the full feature set. The ACB-4000 series controllers do not support command chaining or disconnect/reconnect. When designing systems for the 4000 series, you may go directly from the "bus free" phase to the "selection phase" in the protocol description. The ACB-4000 is designed for single host environments. Other differences will be highlighted throughout this manual.

4.2 GENERAL DESCRIPTION OF SCSI

This system interface provides an efficient method of communication between computers and peripheral I/O devices. The eight-port, daisy-chained bus defined by this specification supports the following features:

* Single or multiple host system.
* Multiple peripheral devices and device types.
* Bus contention resolution through arbitration on a prioritized basis.
* Asynchronous data transfer at up to 1.5 MBytes/sec.
* Disconnected operations.
* Host-to-host communication.

Communication on the bus is allowed between two bus ports at a time. A maximum of eight (8) bus ports are allowed. Each port is attached to a device (e.g. controller or host adapter).

When two devices communicate with each other on the bus, one acts as an INITIATOR and the other acts as a TARGET. The TARGET (typically a controller) executes the operation. A device will usually have a fixed role as an INITIATOR or TARGET, but some devices may be able to assume either role.

An INITIATOR may address up to four (4) peripheral I/O devices that are connected to an ACB-5000 TARGET (two on the ACB-4000). The TARGET will provide a "virtual controller" for each of these devices, appearing to the system as up to four separate controller/device pairs.

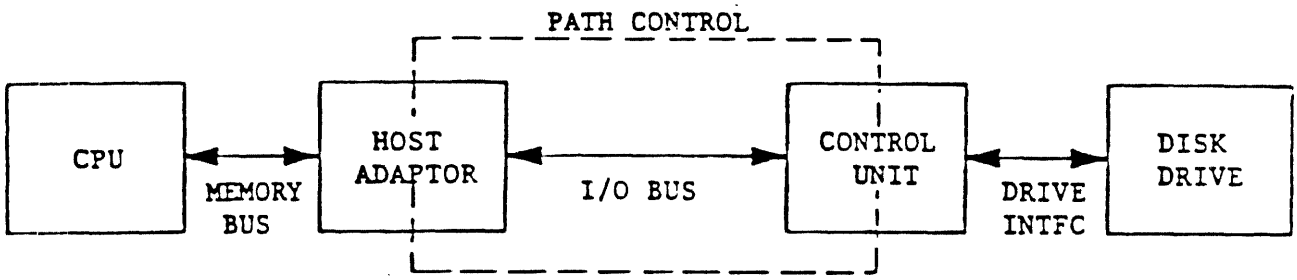
Certain bus functions are assigned to the INITIATOR and certain bus functions are assigned to the TARGET. The INITIATOR may arbitrate for the bus and select a particular TARGET. The TARGET may request the transfer of COMMAND, DATA, STATUS or other information on the bus, and in some cases, may arbitrate for the bus and reselect an INITIATOR for the purpose of continuing an operation.

Data transfers on the bus are asynchronous and follow a defined REQUEST/ACKNOWLEDGE HANDSHAKE protocol. One eight-bit byte of information may be transferred with each handshake.

4.3 PHYSICAL PATH FUNCTIONS

Figure 4-1 shows an INITIATOR and TARGET communicating on the bus in order to execute a command such as READ or WRITE data. For the sake of simplicity, only one of a number of possible partitions (of the physical/functional interface) is presented for illustration.

Figure 4-1 : PHYSICAL PATH



4.3.1. POINTERS

In this architecture, three "conceptual" memory address pointers reside in the INTITIATOR path control. They point to the next byte of COMMAND, DATA and STATUS to be transferred.

After the pointers are initially loaded by the INITIATOR, their movement is under the strict control of the TARGET. When the TARGET transfers a byte of information to or from a (COMMAND, DATA, or STATUS) memory area, the corresponding pointer is incremented.

The INITIATOR pointer control rests in the host adaptor. Further details on host adaptor operation and sample host software drivers are available in ADAPTEC Host Adaptor OEM Manuals.

4.4 TYPICAL FUNCTIONS (External to Path Control)

Listed below are some typical functions that affect the physical path but originate outside its boundary. Although these "commands" rarely pass across such boundaries in practice, they aid in describing the actual sequence of events within the I/O subsystem.

4.4.1. Establish Path

This function enables the INITIATOR to establish the physical path (the physical and logical connection between the INITIATOR and a peripheral device) in order to execute a command and may involve arbitration to gain control of the bus.

ESTABLISH PATH requires the peripheral device address (i.e., the TARGET bus address and LUN within that address) and the three pointers to the COMMAND, DATA and STATUS areas. A saved copy of these pointers may also be required (see 4.4.8. Reestablish Path and 4.4.11. Restore State).

4.4.2. Get Command

This function enables a TARGET to get a COMMAND from the memory area designated by the COMMAND pointer.

4.4.3. Get Data and Send Data

These functions enable the TARGET to transfer data to or from the memory area designated by the DATA pointer.

4.4.4. Send Status

This function enables the TARGET to send STATUS information for a command to the memory area designated by the STATUS pointer.

4.4.5. End of Command

This function enables the TARGET to signal the INITIATOR that the current command has terminated and valid status has been sent.

Since the current command may be linked to another command, END OF COMMAND does not imply the end of an operation.

4.4.6. End Path

The TARGET invokes this function to enable the INITIATOR to clear the physical path to the currently attached peripheral device.

END PATH implies the end of an operation.

4.4.7. Break Path

This function enables the TARGET to temporarily break the physical path and release control of the bus.

4.4.8. Reestablish Path

This function enables the TARGET to reconnect a physical path that was temporarily broken by the "Break Path" function.

The INITIATOR address and the peripheral device address are required. Bus arbitration is also required.

The INITIATOR must restore the COMMAND, DATA and STATUS pointers to their last saved values.

4.4.9. End of Link

This function is invoked by the TARGET to indicate the termination of the current command (because the current command was linked to another command, the physical path connection is still needed).

4.4.10. Save Data Pointer

The TARGET invokes this function to enable the INITIATOR to save a copy of the current Data pointer.

4.4.11. Restore Pointers

The TARGET invokes this function to enable the INITIATOR to load the current (active) COMMAND, DATA and STATUS pointers with the last saved values.

4.4.12. Functional Inplications of ACB-4000 SCSI Subset.

The ACB-4000 will not disconnect and does not support linked commands. Therefore, several of the functions do not apply to an ACB-4000 environment. End of Command and End Path become synonymous and the functions Break Path, Reestablish Path, End of Link, Save Data Pointers and Restore pointers are never invoked.

4.5 BUS SIGNALS

The 9 control signals and 9 data signals (including parity), are described below:

4.5.1 BUSY (BSY)

BSY is an "or-tied" signal which indicates that the bus is in use.

4.5.2. SELECT (SEL)

SEL is an "or-tied" signal used by an INITIATOR to select a TARGET or by a TARGET to reselect an INITIATOR.

4.5.3. CONTROL/DATA (C/D)

C/D is a TARGET-driven signal to indicate whether CONTROL or DATA information is on the data bus. Assertion indicates CONTROL.

4.5.4. INPUT/OUTPUT (I/O)

I/O is a TARGET-driven signal which controls the direction of data movement on the data bus relative to an INITIATOR. Assertion indicates INPUT to the INITIATOR.

4.5.5. MESSAGE (MSG)

MSG is a TARGET-driven signal indicating the MESSAGE phase.

4.5.6. REQUEST (REQ)

REQ is a TARGET-driven signal indicating a request for a REQ/ACK data transfer handshake.

4.5.7. ACKNOWLEDGE (ACK)

ACK is an INITIATOR-driven signal indicating acknowledgment of a REQ/ACK data transfer handshake.

4.5.8. ATTENTION (ATN)

ATN is an INITIATOR-driven signal indicating the ATTENTION condition. (See section 4.7.1)

4.5.9. RESET (RST)

RST is an "or-tied" signal indicating the RESET condition.

4.5.10. DATA BUS (DB: 7-0,P)

Eight data bit signals, plus a parity bit signal comprise the DATA BUS. DB(7) is the most significant bit and has the highest priority during arbitration. Significance and priority decrease with decreasing bit number.

Data parity DB(P) is odd. The use of parity is a system option (i.e., either all devices on the bus generate parity and have parity detection enabled, or all devices have parity detection disabled). Parity is not valid during arbitration.

Each of the eight data signals DB(7) through DB(0) is uniquely assigned as a TARGET or INITIATOR bus address (i.e., DEVICE I.D.) which is normally assigned and "strapped" in the device during system configuration. In order to obtain the bus during arbitration, a device asserts its assigned data bit (DEVICE I.D.) and leaves the other data bits in the passive (non-driven) state.

Note: The ACB-4000 does not support parity.

4.6 BUS PHASES

The bus has eight (8) distinct operational phases and cannot be in more than one phase simultaneously.

* BUS FREE PHASE
* ARBITRATION PHASE
* SELECTION PHASE
* RESELECTION PHASE
* INFORMATION TRANSFER PHASES
* COMMAND PHASE
* DATA PHASES (DATA IN/OUT)
* STATUS PHASE

4.6.1. BUS FREE PHASE

The BUS FREE phase, indicating that the bus is available for use, is invoked by the deassertion and passive release of all bus signals. All active devices must deassert and passively release all bus signals (within a BUS CLEAR DELAY) after deassertion of BSY and SEL.

Devices sense BUS FREE when both SEL and BSY are not asserted (simulataneously within a DESKEW DELAY) and the RESET condition is not active.

4.6.2. ARBITRATION PHASE

The ARBITRATION phase, a system option, enables a device to gain control of the bus (systems without ARBITRATION can have only one INITIATOR). This phase is required for systems which use RESELECTION. A TARGET must not disconnect from an INITIATOR that does not support these functions.

After detecting BUS FREE, a device must wait a minimum of BUS FREE DELAY and a maximum of BUS SET DELAY to assert BSY and its own DEVICE I.D. on the bus. The time required to detect the BUS FREE phase is included in the wait delay.

The DEVICE I.D. is asserted on the DATA BIT signal that corresponds to the BUS ADDRESS for the device. All other DATA BUS drivers must be passive. Data parity is not valid during arbitration.

On detecting SEL, a device must clear itself from arbitration (within a BUS CLEAR delay time) by deasserting its BSY and I.D. signals.

After an ARBITRATION DELAY (timed from the assertion of BSY) the device examines the DATA bus. If a higher priority DEVICE I.D. is on the bus (DB(7) = highest), the device clears itself from arbitration. On obtaining the bus, the device asserts SEL (after the assertion of SEL the device must wait a minimum of two BUS SETTLE DELAYS before changing any bus signals).

4.6.3. SELECTION PHASE

The SELECTION phase allows an INITIATOR to select a TARGET. In order to distinguish this phase from the RESELECTION phase, the I/O signal is not asserted.

In systems without arbitration, the INITIATOR waits a minimum of BUS SETTLE DELAY (after detecting BUS FREE) before driving the DATA bus with the TARGET I.D. and (optionally) its own I.D. After two DESKEW DELAYS, the INITIATOR can assert SEL.

In systems with arbitration, the BSY and SEL signals will have been asserted by the INITIATOR following arbitration. After a minimum of two BUS SETTLE DELAYS, the INITIATOR can assert the TARGET I.D. and its own I.D. on the DATA bus. The INITIATOR then waits at least two DESKEW DELAYS before de-asserting BSY and a BUS SETTLE DELAY before examining the bus for a TARGET response.

4.6.3. SELECTION PHASE (Continued)

On detecting the simultaneous condition (within one DESKEW DELAY) of SEL, its own I.D. asserted, and BSY and I/O not asserted, the selected TARGET examines the DATA bus for the INITIATOR I.D. and responds by asserting BSY. In systems with parity implemented, the TARGET will not respond to its DEVICE I.D. if an error is indicated or if more than two I.D.'s are on the bus.

After a minimum of two DESKEW DELAYS (following the detection of BSY from the TARGET), the INITIATOR deasserts SEL and may change the DATA signals.

The INITIATOR may "time out" the SELECTION phase by deasserting the I.D. bits on the bus. If (after a SELECTION RESPONSE TIME plus two DESKEW DELAYS) BSY has not been asserted, SEL may be deasserted. The TARGET must drive BSY within a SELECTION RESPONSE TIME of detecting SEL and its own I.D.

4.6.4. RESELECTION PHASE (5000 Series Only)

The RESELECTION phase allows a TARGET to reconnect to an INITIATOR to continue an operation that was previously interrupted by the TARGET (i.e., the TARGET disconnected by allowing a BUS FREE phase to occur before the operation was completed).

RESELECTION (used only in systems with ARBITRATION) is a TARGET function which requires a query to the INITIATOR to determine its capability.

On obtaining the bus, the TARGET will assert BSY and SEL, and wait a minimum of two BUS SETTLE DELAYS to assert I/O, the INITIATOR I.D., and its own I.D. The TARGET then waits a minimum of two DESKEW DELAYS to deassert BSY and waits a BUS SETTLE DELAY to examine the bus for an INITIATOR response. The TARGET may "time out" the RESELECTION phase in the same manner as the INITIATOR "times out" the SELECTION phase.

On detecting the simultaneous condition (within a DESKEW DELAY) of SEL, I/O, its own I.D. asserted, and BSY not asserted, the reselected INITIATOR samples the DATA BUS to determine the TARGET I.D. and responds by asserting BSY. In systems with parity implemented, the INITIATOR will not respond to a DEVICE I.D. that has bad parity; nor will it respond if more than two I.D.'s are on the bus.

On detecting BSY from the INITIATOR, the TARGET will also assert BSY (and continue the assertion for the duration of the operation), wait a minimum of two DESKEW DELAYS, then deassert SEL and (possibly) change the I/O and DATA signals.

On detecting the deassertion of SEL, the INITIATOR releases its assertion of BSY.

4.6.5. INFORMATION TRANSFER PHASES

The COMMAND, DATA, STATUS and MESSAGE phases are all used to transfer data or control information through the DATA bus. The actual contents of the information is beyond the scope of this section.

The C/D, I/O and MSG signals are used to differentiate the various INFORMATION TRANSFER phases. Note that these signals are not valid without REQ asserted. See Table 1.

TABLE 1: INFORMATION TRANSFER PHASES

SIGNAL				DIRECTION OF
MSG	C/D	I/O	PHASE NAME	INFORMATION XFER
Ø	Ø	Ø	DATA OUT PHASE	(INIT to TARG)
Ø	Ø	1	DATA IN PHASE	(INIT from TARG)
Ø	1	Ø	COMMAND PHASE	(INIT to TARG)
Ø	1	1	STATUS PHASE	(INIT from TARG)
1	Ø	Ø	* Not Used	
1	Ø	1	* Not Used	
1	1	Ø	MSG OUT PHASE	(INIT to TARG)
1	1	1	MSG IN PHASE	(INIT from TARG)

Notes: Ø = SIGNAL DEASSERTION
1 = SIGNAL ASSERTION
INIT = INITIATOR
TARG = TARGET

The INFORMATION TRANSFER phases use the REQ/ACK handshake to control data transfer. Each REQ/ACK allows the transfer of one byte of data. The handshake starts with the TARGET asserting the REQ signal. The INITIATOR responds by asserting the ACK signal. The TARGET then deasserts the REQ signal and the INITIATOR responds by deasserting the ACK signal.

With I/O signal asserted, data will be input to the INITIATOR from the TARGET. The TARGET must ensure that valid data is available on the bus (at the INITIATOR port) before the assertion of REQ at the INITIATOR port. The data remains valid until the assertion of ACK by the INITIATOR. The TARGET should compensate for cable skew and the skew of its own drivers.

With the I/O signal not asserted, data will be output from the INITIATOR to the TARGET. The INITIATOR must ensure valid data on the bus (at the TARGET port) before the assertion of ACK on the bus. The INITIATOR should compensate for cable skew and the skew of its own drivers. Valid data remains on the bus until the TARGET deasserts REQ.

During each INFORMATION TRANSFER phase, the BSY line remains asserted, the SEL line remains deasserted, and the TARGET will continuously envelop the REQ/ACK handshake(s) with the C/D, I/O and MSG signals in such a manner that these control signals are valid for a BUS SETTLE DELAY before the REQ of the first handshake and remain valid until the deassertion of ACK at the end of the last handshake.

4.6.5.1. COMMAND PHASE

The COMMAND phase allows the TARGET to obtain command information from the INITIATOR.

The TARGET asserts the C/D signal and deasserts the I/O and MSG signals during the REQ/ACK handshake(s) of this phase.

4.6.5.2. DATA PHASES (DATA IN/DATA OUT)

The DATA phase includes both the DATA IN phase and the DATA OUT phase.

The DATA IN phase allows the TARGET to INPUT data to the INITIATOR. The TARGET asserts the I/O signal and deasserts the C/D and MSG signals during the REQ/ACK handshake(s) of this phase.

The DATA OUT phase allows the TARGET to obtain OUTPUT data from the INITIATOR. The TARGET deasserts the C/D, I/O and MSG signals during the REQ/ACK handshake(s) of this phase.

4.6.5.3. STATUS PHASE

The STATUS phase allows the TARGET to send status information to the INITIATOR.

The TARGET asserts C/D and I/O and it deasserts the MSG signal during the REQ/ACK handshake(s) of this phase.

4.6.5.4. MESSAGE PHASES (MESSAGE IN/MESSAGE OUT)

The MESSAGE phase includes the MESSAGE IN and MESSAGE OUT phases.

The MESSAGE IN phase allows the TARGET to INPUT a message to the INITIATOR. The TARGET asserts C/D, I/O and MSG during the REQ/ACK handshake(s) of this phase.

The MESSAGE OUT phase allows the TARGET to obtain a message from the INITIATOR. The TARGET may invoke this phase only in response to the ATTENTION condition created by the INITIATOR. In response to the ATTENTION condition, the TARGET asserts C/D and MSG and deasserts the I/O signal during the REQ/ACK handshake(s) of this phase. See 4.7.1. ATTENTION.

4.6.6. SIGNAL RESTRICTIONS BETWEEN PHASES

When the BUS is between phases, the following restrictions apply to the bus signals:

The BSY, SEL, REQ and ACK signals may not change.

The C/D, I/O, MSG and DATA signals may change.

The ATN and RST signals may change as defined under the descriptions for the ATTENTION and RESET conditions.

4.7. BUS CONDITIONS

The bus has two asynchronous conditions: the ATTENTION Condition and and the RESET Condition. These conditions cause certain BUS DEVICE actions and can alter the bus phase sequence.

4.7.1. ATTENTION CONDITION

ATTENTION allows the INITIATOR signal the TARGET of a waiting MESSAGE. The TARGET may access the messsage by invoking a MESSAGE OUT phase.

The INITIATOR creates the ATTENTION condition by asserting ATN at any time except during the ARBITRATION or BUS FREE phases. The TARGET responds when ready with the MESSAGE OUT phase. The INITIATOR keeps ATN asserted if more than one byte is to be transferred.

The INITIATOR can deassert the ATN signal during the RESET condition, during a BUS FREE phase, or while the REQ signal is asserted and before the ACK signal is asserted during the last REQ/ACK handshake of a MESSAGE OUT phase.

Note: The ACB-4000 supports ATTENTION only for the IDENTIFY message. Any other messages will be rejected.

4.7.2. RESET CONDITION

The RESET condition, created by the assertion of RST, is used to immediately clear all devices from the bus and to reset these devices and their associated equipment as defined in the controller specification.

RESET can occur at any time and takes precedence over all other phases and conditions. Any device (whether active or not) can invoke the RESET condition. On RESET, all devices will immediately (within a BUS CLEAR DELAY) deassert and passively release all bus signals except RST itself. TARGETS capable of continuing an I/O operation after being interrupted by RESET will clear any I/O operation that has not been established.

The RESET condition stays on for at least one RESET HOLD TIME. During the RESET condition, no bus signal except RST can be assumed valid.

Regardless of the prior bus phase, the bus resets to a BUS FREE phase (and then starts a normal phase sequence) following a RESET condition.

4.8. PHASE SEQUENCING

Phases are used on the bus in a prescribed sequence. In all systems, the RESET condition can interrupt any phase and is always followed by the BUS FREE phase. (Any other phase can also be followed by the BUS FREE phase.)

In systems without ARBITRATION, the normal progression is from BUS FREE to SELECTION, and from SELECTION to one or more of the INFORMATION TRANSFER phases (COMMAND, DATA, STATUS or MESSAGE). In systems with ARBITRATION, the normal progression is from BUS FREE to ARBITRATION, from ARBITRATION to SELECTION (or RESELECTION), and from SELECTION (or RESELECTION) to one or more of the INFORMATION TRANSFER phases (COMMAND, DATA, STATUS or MESSAGE).

There are no restrictions on the sequencing between INFORMATION TRANSFER phases. A phase may even follow itself (e.g., a DATA phase may be followed by another DATA phase).

4.9. TIMING

A timing chart is provided in Figure 3. Unless otherwise indicated, the delay time measurements for each device are calculated from signal conditions existing at the device BUS PORT. Delays in the bus cable need not be considered for these measurements.

* ABORTED SELECTION TIME: 200 microseconds (max)

The maximum delay allowed from SELECT detection until a BSY response is generated by a TARGET (or INITIATOR) during SELECTION (or RESELECTION). This is not SELECT TIMEOUT.

* ARBITRATION DELAY: 1.7 microseconds (minimum)

The minimum delay required after asserting BSY for arbitration until the data bus can be examined for the result of arbitration. No maximum time.

* BUS CLEAR DELAY: 650 nanoseconds (maximum)

The maximum time allowed for a device to stop driving all bus signals after: (1) the release of BSY when going to BUS FREE, or (2) another device asserts SEL during ARBITRATION.

* BUS FREE DELAY: 100 nanoseconds (minimum)

The minimum delay required between detection of BUS FREE and assertion of BSY during ARBITRATION.

* BUS SET DELAY: 1.1 microseconds

The maximum time from detection of BUS FREE until BSY is driven.

* BUS SETTLE DELAY: 450 nanoseconds (minimum)

* CABLE SKEW: 10 nanoseconds (maximum)

The maximum difference in propogation time allowed between any two bus signals when measured between any two bus ports.

* DESKEW DELAY: 45 nanoseconds (minimum)

* REQ RESPONSE TIMEOUT: 250 milliseconds

The delay allowed between assertion of REQ by the TARGET and time out (due to lack of ACK from the INITIATOR).

* RESET HOLD TIME: 25 microseconds (minimum)

The minimum time during which RST is asserted. No maximum.

* SELECT TIMEOUT: 250 milliseconds

The delay allowed for a BSY response from an INITIATOR (or TARGET) before time out during SELECTION (or RESELECTION).

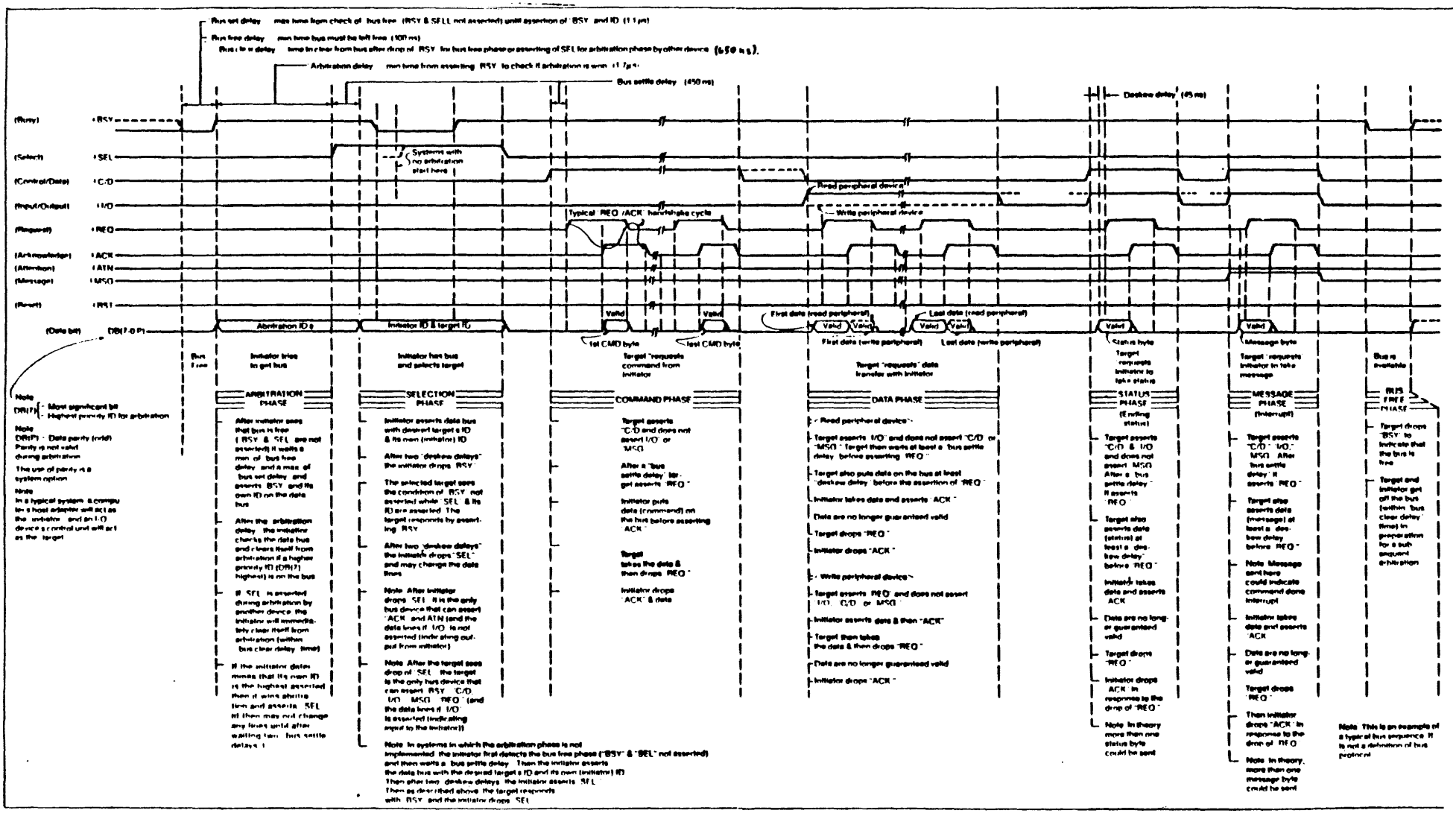


FIGURE 3.

BUS TIMING CHART

5.Ø MESSAGE SPECIFICATION

5.1 MESSAGE SYSTEM

The message system allows communication between an INITIATOR and TARGET for purposes of physical path management. This section defines the messages and lists their assigned codes (in HEX).

Normally, the first message sent by the INITIATOR after the SELECTION phase is IDENTIFY (to establish the physical path). After reselection, the TARGET's first message is also IDENTIFY. Under certain conditions, an INITIATOR may send SELECTIVE RESET or BUS DEVICE RESET as the first message.

The ACB-4ØØØ controllers support the COMMAND COMPLETE, MESSAGE REJECT and IDENTIFY messages and does not respond to the ATN signal except during selection. Only COMMAND COMPLETE need be implemented in a ACB-4ØØØ environment.

5.1.1. SINGLE BYTE MESSAGES

Command Complete (ØØH)

This code is sent from the TARGET, at the completion of command execution (or at the end of a series of linked commands), to direct the INITIATOR to indicate COMMAND COMPLETE to the host.

This message does not imply good ending status; STATUS must be checked to determine end conditions.

Save Data Pointer (Ø2H)

This code is sent from the TARGET to direct the INITIATOR to save a copy of the present active data pointer for the currently attached LUN.

Restore Pointers (Ø3H)

This code is sent from the TARGET to restore the most recently saved pointers (for the currently attached LUN) to the active state.

Pointers to the COMMAND, DATA, and STATUS locations for the LUN will be restored to the active pointers. COMMAND and STATUS pointers will be restored at the beginning of the present operation. The DATA pointer will be restored at the beginning of the operation or at the point at which the last SAVE DATA POINTER message occurred.

Disconnect (04H)

This code is sent from the TARGET to indicate that the current physical path will be broken (the TARGET will disconnect by releasing BSY) and that a later reconnect will be required to complete the current operation.

Error status should be stored if BSY is released in response to any message except 00 or 04 (or RST). By not sending DISCONNECT or COMMAND COMPLETE before going to BUS FREE (except in response to RESET), the TARGET indicates a catastrophic error.

INITIATOR-detected Error (05H)

This code is sent from the INITIATOR to indicate an INITIATOR-detected retryable error (since the last SAVE DATA POINTER).

Abort (06H)

This code is sent from the INITIATOR to direct the TARGET to reset the currently selected LUN and any pending I/O from that LUN for the selecting INITIATOR and cause the bus to go to the BUS FREE phase. No status or ending message will be sent for the I/O.

If no LUN has been selected, then all pending I/O operations from the selected TARGET to the selecting INITIATOR will be cleared.

Message Reject (07H)

This code is sent from the INITIATOR or TARGET if the message received was inappropriate or not implemented.

The INITIATOR will assert the ATN signal prior to its release of ACK for the REQ/ACK handshake of the message that will be rejected. When the TARGET sends this message, it will change to MESSAGE IN Phase and send this MESSAGE prior to requesting additional message bytes.

No Operation (08H)

This code is sent from the INITIATOR in response to a request for a message when no valid message exists.

Message Parity (Ø9H)

This code is sent from either the INITIATOR or TARGET to indicate a parity error in the last message received.

To ensure that the current message is rejected by the TARGET, the INITIATOR, before indicating rejection, must assert the ATN signal prior to its release of ACK for the REQ/ACK handshake of the faulty message.

Linked Command Complete (ØAH, ØBH)

This code is sent from the TARGET to indicate completion of the current command.

In response to ØAH, the INITIATOR will update the pointers to next command. In response to ØBH, the pointers will be updated and the system will be signalled that the operation is complete to this point. Status will be stored in either case.

Bus Device Reset (ØCH)

This code is sent from the INITIATOR to the TARGET to reset all I/O operations to all INITIATORS.

Identify (8Ø TO FF)

This code is sent by either the INITIATOR or TARGET to establish the physical path connection between the INITIATOR and TARGET for a particular LUN. Initiators signal thier support for the message system by asserting ATTENTION during the selection phase. (The ACB-4ØØØ expects an IDENTIFY message in this case -- with the ACB-5ØØØ several other INITIATOR generated messages are valid.)

If an IDENTIFY message is received the LUN specified there is used in lieu of the LUN field (Byte Ø1) of the command.

Bit-7 is always set to identify this message.

Bit-6 is set by the INITIATOR to indicate its capability to accommodate disconnection and reconnection.

Bits-5, 4, and 3 are reserved.

Bits-2, 1, and Ø specify a LUN address in a TARGET.

5.1.2 EXTENDED MESSAGES

Extended Message Follows (01H)

This code is sent from either an INITIATOR or TARGET to indicate that a multiple byte message will follow.

The first byte following the 01H is a length indicator for the number of bytes to follow. A value of zero indicates 256 bytes.

The second byte is the extended message code. The extended messages defined by the SCSI specification are:

Modify Data Pointer	(00H)
Synchronous Transfer Request	(01H)
Extended Identify	(02H)

6.0 COMMAND SPECIFICATIONS

6.1 GENERAL DESCRIPTION

This section of the ADAPTEC Controller Manual includes thesoftware command set and the specific status information related to the commands.

By defining a fixed block structure using a simple, logical address scheme, the I/O interface can support device independence. In addition, by including the logical block address as a component of the command structure, physical requirements (such as SEEK) can be imbedded within the basic READ and WRITE requests.

This interface, despite its simplicity, is capable of providing the high level of performance required in multi-host/multi-task environments. Powerful functions, such as search and chaining, are included to enhance random access applications, and single-command, multiple-block transfers are included to simplify sequential operations.

The ACB-5000 series controllers support a majority of the proposed ANSI SCSI command set and the ACB-4000 supports a sub-set of these commands. It is important to note that all ADAPTEC controllers require that reserved bit and byte positions in commands be zero. Commands which violate this standard will be rejected. Therefore, as a rule, all reserved and vendor unique portions of commands should be zero unless their use is specifically stated in this document.

See the ADAPTEC Controller/System Interface Specification or the SCSI Specification (ANSI Task Group X3T9.2) for complete details on the use of disconnected operations and linked commands.

6.2 COMMAND AND STATUS STRUCTURE

6.2.1. COMMAND DESCRIPTION BLOCK (CDB)

An I/O request to a device is made by passing a Command Description Block (CDB) to the Controller. The first byte of the CDB is the command class and operation code. The remaining bytes specify the Logical Unit Number (LUN), block starting address, control byte, and the number of blocks to transfer. Commands are categorized into two classes supported in ADAPTEC controllers:

Class 0: 6-Byte commands

Class 1: 10-Byte commands.

Tables 6-1 and 6-2 show typical command descriptor block formats.

Table 6-1: CLASS 00 COMMANDS (6-BYTE COMMANDS)
(Such as READ or WRITE)

BYTE	BIT 7	6	5	4	3	2	1	0
00	Class Code			Opcode				
01	Logical Unit Number			(MSB) Logical Block Address				
02	Logical Block Address							
03	Logical Block Address							(LSB)
04	Number of Blocks							
05*	Reserved						FlagRq	Link

* Control Byte

Table 6-2: CLASS Ø1 COMMANDS (1Ø BYTE EXTENDED BLOCK ADDRESS)

BYTE	BIT 7	6	5	4	3	2	1	Ø
ØØ	Class Code			Opcode				
Ø1	Logical Unit Number			Command Specific Bits				Rel Ad
Ø2	(MSB) Logical Block Address							
Ø3	Logical Block Address							
Ø4	Logical Block Address							
Ø5	Logical Block Address							(LSB)
Ø6	Reserved							
Ø7	Number of Blocks							
Ø8	Number of Blocks							
Ø9*	Reserved						FlagRq	Link

*Control Byte

6.2.2. CLASS CODE

The class code can be Ø to 7, but only Ø and 1 are used at this time.

6.2.3. OPERATION CODE

The operation code for each class allows 32 commands (ØØ to $1F_H$).

6.2.4. LOGICAL UNIT NUMBER

Logical unit numbers allow 8 devices per Controller. The ACB-5ØØØ series controllers address four devices (Ø to 3) while the ACB-4ØØØ accomodates only 2 devices per Controller.

6.2.5. COMMAND SPECIFIC BITS

Byte Ø1, bits Ø1 - Ø4 specify options which depend opon the particular command.

6.2.6. LOGICAL BLOCK ADDRESS

Class Ø commands contain 21 bit starting block addresses while Class 1 supports 32 bit block addressing.

The "block" concept implies that the Host and Controller have "preset" the number of bytes of data to be transferred. You will note that the concept of sector is replaced by block.

6.2.7. NUMBER OF BLOCKS

A variable number of blocks may be transferred under a single command. Class ØØ commands may transfer up to 256 blocks, while Class Ø1 commands may transfer up to 64K blocks. A zero block number count defaults to the maximum value.

6.2.8. CONTROL BYTE (Last Byte in All Commands)

Bit 7 Reserved and must for zero except with READ command.

Bits 6-2 Not used. Must be zero.

Bit 1 = 1 This bit is meaningful when Bit Ø is set indicating that status is requested for each command in a group of linked commands. If not set, intermediate status will not be presented.

Bit Ø = 1 This bit indicates an automatic link to the next command upon completion of the current command. STATUS is sent for each command executed if bit 1 is set.

6.2.9. RELATIVE ADDRESS BIT

Linked Class Ø1 commands (after the first command in a sequence) may have the Relative Address Bit set to indicate that the Logical Block Address field contains a two's complement displacement. This displacement is the block offset from the last logical address processed by the previous command.

6.3 COMMAND DESCRIPTIONS

The following section describes the complete command set and associated formats for all ACB controllers. In most cases, ADAPTEC has followed the proposed ANSI SCSI command specifications to the letter, deviating only in degree of implementation.

6.3.1. CLASS ØØ COMMAND DESCRIPTIONS

The following is a series of command descriptions and their associated return data.

Table 6-5: CLASS ØØ COMMAND CODE SUMMARY

OP CODE	COMMAND	OP CODE	COMMAND
ØØ	TEST UNIT READY	13	WRITE BUFFER
Ø1	REZERO UNIT	14	READ BUFFER
Ø3	REQUEST SENSE	15	MODE SELECT
Ø4	FORMAT UNIT	16	RESERVE UNIT*
Ø8	READ	17	RELEASE UNIT*
ØA	WRITE	1A	MODE SENSE*
ØB	SEEK	1B	START/STOP UNIT
ØF	TRANSLATE	1C	RECEIVE DIAGNOSTIC
12	INQUIRY*	1D	SEND DIAGNOSTIC

* ACB-4ØØØ does not support

Only commands which do not conform to the command structure shown in Table 6-1 will be diagrammed to illustrate deviations and extensions.

TEST UNIT READY ($ØØ_H$)

This command returns zero status if the requested unit is powered on and ready. If not ready, a check condition will be set in the status byte. Possible errors are Drive Not Ready ($Ø4_H$) and Write Fault ($Ø3_H$). This is not a request for self-test. This is not a disconnected operation.

REZERO UNIT ($Ø1_H$)

This command sets the selected drive to track zero and then sends completion status. Possible error returns are No Seek Complete ($Ø2_H$), Drive Not Ready ($Ø4_H$) and No Track Zero ($Ø6_H$). This is a disconnected operation on the ACB-5ØØØ series.

REQUEST SENSE ($Ø3_H$)

See Paragraph 6.4 for details of the complete command as

well as a complete discussion of returned sense data.

FORMAT UNIT (04_H)

The control unit will write from index to index all ID and DATA fields with a block size as specified by an immediately previous MODE SELECT command. If no MODE SELECT command has been executed, the previous data block size will be used. On unformatted disks or those whose format is determined bad (sense byte error code $1C_H$ returned following a READ), a default of 256 bytes per block will be used in the absence of a MODE SELECT (NOTE: All the parameters specified by the MODE SELECT command will default). Data fields are completely written with $6C_H$ unless otherwise specified in the format command.

BYTE \ BIT	07	06	05	04	03	02	01	00
00	0	0	0	0	0	1	0	0
01	Logical Unit Number			Data	Cmplt	List Format Bits		
02	Data Pattern							
03	(MSB) Interleave							
04	Interleave							(LSB)
05*	Reserved						FlagRq	Link

* Control Byte.

The ID fields will be interleaved as specified in bytes 3 and 4 of the CDB (byte 4, bit 0 LSB). Under normal conditions, ADAPTEC controllers do not require interleaving because of their high speed buffer control. An interleave number of 1 results in sequential ID fields being written on the disk. Any interleave number greater than 1 and one less than the total sectors per track result in interleaved formatting. A 0 in this field will cause the default interleave factor of 2 to be used. By using an interleave of 2, ADAPTEC controllers can format 33 256-byte sectors per track rather than the normal 32 sectors. Note that byte 3 must always be zero and also that the value in byte 4 must not exceed the number of sectors per track minus one. An error code of 24_H (Bad Argument) will be returned if either of these rules are violated.

The interleave number is equivalent to the number of disk revolutions required to sequentially read one track. An example of an interleave number of 3 follows:

```
P -  00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15
F -  00 11 22 01 12 23 02 13 24 03 14 25 04 15 26 05

  -  16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
  -  16 27 06 17 28 07 18 29 08 19 30 09 20 31 10 22
```

where P=physical sectoring and F=new formatted addresses.

Bits 0 through 4 of byte 1 in the CDB specify the format of the bad block list for defect skipping.

When the Data Bit (04) is set, the controller expects a list of known bad areas in the data portion of the command. If this bit is zero, the defect list is not read and defect skipping is not performed.

Bit 03 is the Complete List bit and specifies that all of the known defects on the drive are contained in the list. The list itself must be less than 1024 bytes since it must fit in the available buffer space. On ACB controllers, this bit must always be set or the command will be rejected.

Bit 02 of Byte 01, if set, indicates that the next two bits (Byte 01, Bits 01 and 00) will be used to define the format. A zero indicates default. The next Format List bit (Byte 01, Bit 01) if set indicates that the data pattern in Byte 02 is to be used to format. A zero indicates default. A zero indicates that a Cylinder /Head/Byte Count format is used in the data list. The following table defines the use of the Data and List Format bits:

Fmt Data	Bit 02	Bit 00	Definition
0	0	0	Format with no user-supplied error information.
1	1	0	Error information is in Cyl., Head and Displacement format.

All other combinations of these bits will be rejected.

Bit 01	Definition
0	Format with default fill byte ($6C_H$)
1	Use format command byte 02 for fill data.

The following is the defect list format supported by ADAPTEC controllers. The list includes the physical coordinates of known media flaws in assending order of cylinder, head, and bytes from index.

FORMAT DATA (BYTE FORMAT)

BYTE	BIT 07	06	05	04	03	02	01	00
00	Reserved							
01	Reserved							
02	Length of							
03	Defect List in Bytes (8N)							
04	(MSB)	Cylinder Number of Defect #1						
05	Cylinder Number of Defect #1							
06	Cylinder Number of Defect #1							(LSB)
07	Head Number of Defect #1							
08	(MSB)	Bytes From Index						
09	Bytes From Index							
10	Bytes From Index							
11	Bytes From Index							(LSB)
.								
.								
.								
8N-4 to 8N+3	Nth Defect							

If data errors are noted by the controller while reading the defect list, all formatting is stopped and a Bad Argument error (24_H) is returned to the host.

The ACB controllers free the SCSI bus while formatting. However, any calls to LUN's on the controller will receive Busy Status until the format operation is complete.

If, in time, other defects appear on a drive, the contents of the entire drive should be backed up and a new format operation performed. To identify the physical locations of the troublesome blocks use the TRANSLATE command. The new defect locations must then be added and sorted into the complete list.

ADAPTEC's defect skipping technique is at the sector level and does not require time-consuming seeks to spare track locations. Therefore, the tracks specified by a drive manufacturer as "spare" may be utilized for data, increasing the effective capacity of the device.

READ (08_H)

This command transfers (to the Host) the specified number of blocks starting at the specified logical starting block address.

The control unit will verify a valid seek address and proceed to seek to the specified starting logical block address. Prior to the seek, the ACB-5000 disconnects and can accept a command for another LUN. If there is no seek required for the operation, no disconnect is performed. When the seek is complete, the controller reconnects to the host and then reads the starting address data field into the buffer, checks ECC and begins DMA data transfer.

Subsequent blocks of data are transferred into the buffer in a similar manner until the block count is decremented to zero. Cylinder switching is transparent to the user. On a data ECC error, the block is re-read up to 5 times to establish a solid error syndrome. Only then is correction attempted. Correction is done directly into the data buffer, transparent to the host.

There is a corresponding extended READ command using the Class 01 CDB format.

WRITE ($0A_H$)

This command transfers (to the Target Device) the specified number of blocks starting at the specified logical starting block address. The controller seeks to the specified logical starting block. The ACB-5000 disconnects during this seek and can accept a command for another LUN. Disconnect is not performed if no seek is required. When the seek is complete, the controller reconnects to the host, transfers the first block into its buffer and writes its buffered data and its associated ECC into the first logical sector.

Subsequent blocks of data are transferred as available from the FIFO buffer until the block count is decremented to zero. Cylinder switching and defect skipping are transparent to the user.

ADAPTEC controllers also support a corresponding extended WRITE command using the Class 01 CDB format.

SEEK ($0B_H$)

This command causes the selected drive to seek to the specified starting address. The ACB-5000 disconnects during the seek and is able to accept other commands for other LUN's. (The ACB-4000 returns completion status immediately, allowing it to free the bus and accept further commands prior to actual seek completion. Note: Any command received for a unit with a seek in progress will immediately complete with a command completion status of busy (bit 3 set). This is done to allow the host to use the SCSI bus to do other processing while waiting for seek complete.)

The drive is stepped to the addressed track position but no ID field verification is attempted. When the seek is complete, the controller reconnects to the host and responds with completion status.

All ACB products use an implied seek on READ, WRITE and SEARCH commands obviating the need for issuance of SEEK commands with each operation.

TRANSLATE ($0F_H$)

This command performs a logical address to physical address translation and returns the physical location of the requested block address in a cylinder, head, bytes from index format. This data can be used to build a defect list for the FORMAT command.

Eight bytes are returned in the format of defect descriptors required by FORMAT.

INQUIRY (12_H)

This command requests the transfer of Target configuration parameters to the Host. Byte four of the command indicates the maximum number of data bytes that may be transferred by the Controller and must be a value of 03_H.

Controller response to INQUIRY is normally three bytes:

1 Byte Code:
- Ø - Direct access device
- 1 - Sequential access device
- 2 - Output only device
- 3 - Processor

1 Byte Qualifier:
- Bit 7 - On if removable media
- Bits 6-Ø - User defined (Zero if no code)

1 Byte: Length of additional bytes

The qualifier byte allows users to define classes of devices within a system (useful in systems with multiple removable media drives).

NOTE: This command is not supported on the ACB-4000.

WRITE DATA BUFFER (13_H)

This command serves buffer RAM diagnostic purposes. The controller will fill the buffer with 1K bytes of data from the host. There is no guarantee that this data will not be overwritten by other operations initiated by other INITIATORS.

READ BUFFER RAM (14_H)

Read Buffer will pass the host 1K of data from the buffer. It is intended for RAM diagnostic purposes. The same caveat applies to this as to write buffer. In addition, although data remains in the buffer after normal data operations the ordering of the data found there is undefined.

MODE SELECT (15_H)

This command is used in ACB controllers to specify FORMAT parameters and should always preceed the FORMAT command, either by linking (on the 5000 series) or as a separate and distinct command (on the 4000).

In the absence of a MODE SELECT command, ADAPTEC controllers format to the previous sector size or to 256 byte sectors on unformatted drives. The MODE SELECT command is also used to specify drive specific parameters. These will also revert to default or previous values if a FORMAT is issued without a MODE SELECT. Note that it is possible to specify only the blocksize in a MODE SELECT. In this case the previous drive parameters are preserved.

MODE SELECT COMMAND

BYTE \ BIT	07	06	05	04	03	02	01	00
00	0	0	0	1	0	1	0	1
01	Logical Unit Number			Reserved				
02	Reserved							
03	Reserved							
04	Number of Bytes							
05*	Reserved						FlagRq	Link

* Control Byte

Byte 4 of the command specifies the number of information bytes to be passed with the command. A minimum of twelve bytes ($0C_H$) must be specified. If drive parameters are being specified the count should be 22 bytes (16_H).

The parameter list is four bytes long with the first three bytes reserved (zero filled). The fourth byte contains the the length in bytes of the extent descriptor list; this is always eight. (Only a single extent is supported.)

MODE SELECT PARAMETER LIST

BYTE	BIT 07	06	05	04	03	02	01	00
00	Reserved							
01	Reserved							
02	Reserved							
03	Length of Extent Descriptor List = 08_H							

EXTENT DESCRIPTOR LIST

BYTE	BIT 07	06	05	04	03	02	01	00
00	Density Code							
01	Reserved							
02	Reserved							
03	Reserved							
04	(MSB) Block Size							
05	Block Size							
06	Block Size							
07	Block Size							(LSB)

Byte 0 of the extent descriptor list specifies the data density of the drive. Current ACB products support only MFM and a value of 00 in this byte is required. Bytes 1, 2 and 3 are reserved and must be zero, specifying that the entire drive is to be formatted. Bytes 4 through 7 are used to specify the data block size. The block size must not be less than 256 or exceed the RAM buffer capacity which, on standard ACB controllers, is 1024 characters.

The ACB-4000 must be set up with a value 256, 512 or 1024 bytes, while the ACB-5000 can format with any block size between 256 and 1024 bytes.

Any violation of the above constraints will result in Check Status with a Error Code of 24_H, indicating an invalid argument in parameter data.

DRIVE PARAMETER LIST

BYTE	BIT 07	06	05	04	03	02	01	00
00	List Format Code == 01							
01	MSB Cylinder Count							
02	Cylinder Count							LSB
03	Data Head Count							
04	MSB Reduced Write Current Cylinder							
05	Reduced Write Current Cylinder							LSB
06	MSB Write Precompensation Cylinder							
07	Write Precompensation Cylinder							LSB
08	Landing Zone Position							
09	Step Pulse Output Rate Code							

The Drive Parameter list includes all the data necessary to specify a drive. It is optional, but if present must be complete and the items must be within the limits stated. If these parameters are not supplied the format operation will use previously supplied values if available or the default values given below.

The List Format Code must be 01.

The Cylinder Count is the number of data cylinders on the drive. Due to the in-line defect skipping formatting cylinders normally set aside as spares may be included in this total. The minimum is one. The maximum supported is 2048. The default value is 306.

The Data Head Count is the number of usable data surfaces. The heads will be selected from 0 to head count minus 1. The minimum is 1; maximum is 16. A drive with 9 or more heads will use the reduced write current line as the high order head select. The default value is 2.

The Reduced Write Current Cylinder is the cylinder number beyond which the controller will assert the reduced write current line. Minimum value is 0; maximum is 2047. The default value is cylinder 150. Note that reduced write current assumes a different meaning on drives with more than 8 heads.

The Write Precompensation Cylinder is the cylinder beyond which the controller will compensate for inner track bit shift. The specs for this function agree with those of most disk manufacturers. Minimum value is 0; maximum is 2047.

> NOTE: On the ACB-4000 this field is ignored. The Precomp threshold is the same as the reduced write current value. As most drives now ignore the reduced write current signal this is not a serious restriction. However for those drives with more than 8 heads jumpers are provided on the board which allow the precompensation to be selected as always on, always off or tied to reduced write current. The normal position is tied to reduced write current. This jumper applies to both drives. (For Maxtor drives set the jumper to the always off position. See Appexdix A.)

The Landing Zone Position is used with the Start/Stop command to indicate the direction and number of cylinders from the last (or first) data cylinder to the shipping position. The most significant bit indicates the direction with a zero meaning that the landing zone is beyond the highest track and a one indicates the landing zone is outside track zero. The low seven bits gives the number of cylinders. The default is zero (land on inner track.)

The Step Pulse Output Rate Code specifies the timing of seek steps. Four options are currently available:

```
00 == Non Buffered Seek -- 3.0 mS rate -- ST-506
01 == Buffered Seek -- 30 uS rate -- ST-412
02 == Buffered Seek -- 14 uS rate
03 == Buffered Seek -- TBD rate
      (On the ACB-4000 option 03 == 02)
```

RESERVE UNIT (16_H)

This command reserves the unit for use by the requesting Host until a RELEASE UNIT COMMAND is received. This command is particularly useful in multi-user, multi-tasking systems or multiple host systems where a user does not wish to allow another user to modify current data until the next operation is performed. Reservations are voided by a Controller Reset.

A BUSY completion status will be returned to any other Initiator attempting to access a reserved unit.

NOTE: Bit 00 of Byte 01 must be zero, indicating no extents. This command is only available on the ACB-5000 series.

RELEASE UNIT (17_H)

This command releases a reserved unit from the Host which executed the RESERVE UNIT command.

If the reserving Host becomes unable to release the reserved unit, the controller will be locked for all use until a Bus Device Reset or System Reset.

NOTE: This command is only available on the ACB-5000 series.

MODE SENSE ($1A_H$)

This command requests return of the current media, unit, or device parameters as were established by the last MODE SELECT and FORMAT UNIT commands. Byte 04 of the command contains the length of the buffer allocated for the associated data field, and at this time should only be set to 12.

MODE SENSE COMMAND

BYTE	BIT 07	06	05	04	03	02	01	00
00	0	0	0	1	1	0	1	0
01	Logical Unit Number			Reserved				
02	Reserved							
03	Reserved							
04	Length of Data Buffer							
05*	Reserved						FlagRq	Link

* Control Byte

The response parameter list is four bytes long with the first byte echoing the data buffer length of 12 and the next two bytes (01 and 02) reserved (zero filled). The fourth byte contains the the length in bytes of the extent descriptor list, normally eight.

MODE SENSE PARAMETER LIST

BYTE	BIT 07	06	05	04	03	02	01	00
00	Reserved							
01	Reserved							
02	Reserved							
03	Length of Extent Descriptor List = 08_H							

EXTENT DESCRIPTOR LIST

BYTE \ BIT	07	06	05	04	03	02	01	00
00	Density Code							
01	Reserved							
02	Reserved							
03	Reserved							
04	(MSB) Block Size							
05	Block Size							
06	Block Size							
07	Block Size							(LSB)

Byte 0 of the extent descriptor list specifies the data density of the drive. Current ACB products support only MFM and a value of 00 in this byte is always returned. Bytes 1, 2 and 3 are reserved and will be zero. Bytes 4 through 7 specify the data block size. The block size will not be less than 256 or exceed the RAM buffer capacity which, on standard ACB controllers, is 1024 characters.

START/STOP UNIT ($1B_H$)

Byte 04, bit 00 of this command should be set if this is a START command, otherwise it is a STOP command.

The Immed bit (Byte 01, bit 00) should be set if the host desires immediate ending status. (Not supported on ACB-4000)

This command is designed for use with removable media drives and those with a designated shipping or landing zone. Most of the current drives only support STOP.

A STOP command will position the head to the landing zone position then (on the ACB-5000) assert the drives change cartridge or stop line.

A Start command will initiate the drive reinitialization sequence. (On the ACB-5000 this will include a TBD start sequence for removeable media drives.)

BYTE \ BIT	07	06	05	04	03	02	01	00
00	0	0	0	1	1	0	1	1
01	Logical Unit Number			Reserved				Immed
02	Reserved							
03	Reserved							
04	Reserved							St/Stp
05*	Reserved						FlagRq	Link

* Control Byte

RECEIVE DIAGNOSTIC RESULT ($1C_H$)

This command sends analysis data to Host after completion of a SEND DIAGNOSTIC command.

Bytes 3 and 4 designate the size of the available buffer (in bytes).

SEND DIAGNOSTIC ($1D_H$)

This command sends data to the Controller to specify diagnostic tests for Controller and peripheral units.

Bytes 3 and 4 specify the length of the data to be sent.

UOF (Unit offline: Byte 1, Bit 0) enables write and positioning operations on user media.

DOF (Device offline: Byte 1, Bit 1) enables execution of diagnostic commands that may adversely affect I/O operations to other LUN's on the same controller.

(The ACB-4000 implements these to provide access to internal use only diagnostic functions. The controller performs a self test on power up and reset.)

6.3.2 CLASS Ø1 COMMAND DESCRIPTIONS

Table 6-6: CLASS Ø1 COMMAND CODE SUMMARY

OP CODE	COMMAND	OP CODE	COMMAND
25	READ CAPACITY	2F	VERIFY
28	READ	3Ø	SEARCH DATA HIGH*
2A	WRITE	31	SEARCH DATA EQUAL
2E	WRITE AND VERIFY	32	SEARCH DATA LOW*
		33	SET LIMITS*

* Not supported on ACB-4ØØØ

READ CAPACITY (25_H)

If byte 8 of the CDB is $ØØ_H$, this command will return the address of the last block on the unit. It is not necessary to specify a starting block address in this command mode. If byte 8 is $Ø1_H$, this command will return the address of the block (after the specified starting address) at which a substantial delay in data transfer will be encountered (e.g., a cylinder boundary). Any value other than $ØØ_H$ or $Ø1_H$ in byte Ø8 will cause Check Status with an Error code of 24_H for an invalid argument. This is not a disconnected operation.

In both cases, the format block size is defined by the last four bytes of the 8-byte data field returned as a result:

4 Bytes - Block Address
4 Bytes - Block Size

WRITE AND VERIFY ($2E_H$)

This command is similar to the traditional "read after write" function. It is an extended address command which operates like a WRITE command over the specified number of blocks and then verifies the data written on a block by block basis. The ACB-5ØØØ series controllers disconnect on the seeks prior to both the WRITE and VERIFY cycles, reconnecting to perform each function.

The data is not compared with the input buffer. An ECC verification is made on each data block, requiring a complete second pass over the entire data field. Check Status is returned on an error and a Class Ø1 error code $Ø9_H$ is reported.

VERIFY ($2F_H$)

This command is similar to the previous WRITE AND VERIFY except that it verifies the ECC of an alreading existing set of data blocks. It is up to the Host to provide data for rewriting and correcting if an error is detected.

VERIFY may also be linked to other commands, but, since the data verification is done by ECC comparison, byte or partial block verification cannot be accomplished.

SEARCH DATA EQUAL (31_H)

This powerful extended address command provides for a search and compare on equal of any data on the disk. A starting block address and number of blocks to search are specified and a search argument is passed from the Host which includes a byte displacement and the data to compare. If a command is linked (in the ACB-5000 only) to the SEARCH command and the search is successful, then the next command is fetched and executed. In this case, Byte 01, bit 00 of the new command will be checked. If it is on, the address portion of the command is a two's complement displacement from the address at which the SEARCH was satisfied. If the search was not satisfied, the link is broken and END STATUS is presented.

The Invert bit (Byte 01, Bit 04) inverts the sense of the search comparison operation. With invert on, a SEARCH DATA EQUAL command would succeed on data not equal; SEARCH DATA LOW would succeed on data greater or equal. The invert bit on the ACB-4000 allows SEARCH EQUAL inverted which succeeds on the first block not equal to the pattern.

Since the address of the block that has satisfied the SEARCH is normally desired, an extended SENSE command should be linked to the SEARCH. The returned sense data will include the logical block number which satisfied the search and, if desired, the data displacement from the beginning of the block. This information may then be used for subsequently linked commands such as READ or update WRITE of the identified block.

By using this command , small computer systems are given the power of large mainframes by rapidly searching for record key fields when implementing indexed access methods.

The ACB-4000 can only perform unlinked searches of complete blocks. If there are any violations of this rule, the controller will submit Error Code 24_H, indicating a bad parameter.

When a search is satified, it will terminate with a Condition Met Status. (The intermediate status sent bit will also be set when the search command is linked to another command.) A Request Sense Command can then be issued to determine the block address and record offset of the matching record. A Request Sense following a successful Search Data command will:

1. Report a Sense Key of Equal if the search was satisfied by an exact match. If the search was satisfied by an inequality, a Sense Key of No Sense is reported.

2. Set the Valid bit to one.

3. Report the address of the block containing the first matching record in the Information Bytes.

4. Report the record offset of the matching record in the first four bytes of the additional Sense Bytes.

The Request Sense command following an unsuccessful Search Data command will:

1. Report a Sense Key of No Sense, provided no errors occured.

2. Set the Valid bit to zero.

SEARCH DATA EQUAL COMMAND

BYTE	BIT 07	06	05	04	03	02	01	00
00	0	0	1	1	0	0	0	1
01	Logical Unit Number			Invert	Reserved			Rel Ad
02	(MSB) Logical Block Address							
03	Logical Block Address							
04	Logical Block Address							
05	Logical Block Address							(LSB)
06	Reserved							
07	Number of Blocks							
08	Number of Blocks							
09	Reserved						FlagRq	Link

The argument following a SEARCH command is as follows:

BYTE \ BIT	07	06	05	04	03	02	01	00
00	(MSB)			Record Size				
01				Record Size				
02				Record Size				
03				Record Size				(LSB)
04	(MSB)			First Record Offset				
05				First Record Offset				
06				First Record Offset				
07				First Record Offset				(LSB)
08	(MSB)			Number of Records				
09				Number of Records				
10				Number of Records				
11				Number of Records				(LSB)
12	(MSB)			Search Argument Length				
13				Search Argument Length				(LSB)
14	(MSB)			Search Field Displacement				
15				Search Field Displacement				
16				Search Field Displacement				
17				Search Field Displacement				(LSB)
18	(MSB)			Pattern Length				
19				Pattern Length				(LSB)
20				Data Pattern				
.								
.								
.								
M+19				Data Pattern				

A definition of the required data in the SEARCH argument follows:

BYTES	PARAMETER
ØØ TO Ø3	Record Size (Bytes) For all ADAPTEC controllers this must equal the blocksize or zero. Zero will be taken to mean the format blocksize.
Ø4 to Ø7	First Record Offset (Bytes) For all ADAPTEC controllers this must be zero.
Ø8 to 11	Number of Records For ADAPTEC controllers this must be less than or equal to the number of blocks specified in the command and greater than zero. The search will terminate upon a match or when the smaller of these values is encountered.
12 to 13	Search Argument length (Bytes) The number of bytes in the following search argument. Must equal the pattern length + 6.
14 to 17	Search Field Displacement The displacement from the beginning of the record to the first byte to be compared. Must be zero for the ACB-4000 series controllers.
18 to 19	Pattern Length (M Bytes) The number of bytes in the following data pattern to be compared with a like size field in each record. Pattern length must equal blocksize on the 4000 series controllers.
2Ø to M+19	Data Pattern A variable length field of M bytes up to blocksize - displacement bytes. The ACB-4000 pattern must be one block long.

SEARCH DATA HIGH (30_H)

This command performs the same function as the SEAPCH DATA EQUAL command, but is satisfied if the data compared is higher than or equal to the search argument. See SEARCH DATA EQUAl for meaning of Invert Bit.

The ACB-4000 supports only SEARCH DATA EQUAL.

SEARCH DATA LOW (32_H)

This command performs the same function as the SEAPCH DATA EQUAL command, but is satisfied if the data compared is lower than or equal to the search argument. See SEARCH DATA EQUAL for meaning of Invert Bit.

The ACB-4000 supports only SEARCH DATA EQUAL.

SET LIMITS (33_H)

This extended address command establishes an "I/O mask" similar to the capability found in large scale host systems. A set of upper and lower limits are defined in the command between which data access may be limited by read or write protection (or both).

The defined limits are block addresses within which subsequent linked commands may operate. Only one SET LIMITS command may be linked per chain of commands.

Using this facility, the Host may protect (or mask) system areas from lower level user access, while allowing normal operation in other areas. A check status is returned on an illegal access request with an error code of 24_H.

The two low order bits of byte 1 in the command define the illegal operations within the limits of the specified addresses. Bit 0 and bit 1 indicate write and read inhibit, repectively. One or both bits may be set.

(Not supported on ACB-4000 controllers.)

SET LIMITS COMMAND

BYTE \ BIT	07	06	05	04	03	02	01	00
00	0	0	1	1	0	0	1	1
01	Logical Unit Number			Reserved			RdInhb	WrtInh
02	(MSB) Logical Block Address							
03	Logical Block Address							
04	Logical Block Address							
05	Logical Block Address							(LSB)
06	Reserved							
07	Number of Blocks							
08	Number of Blocks							
09*	Reserved						FlagRq	Link

*Control Byte

6.4 COMPLETION STATUS BYTE

Status is always sent at the end of a command or set of linked commands. Intermediate status is sent at the completion of a linked command. Any abnormal condition encountered during command execution causes command termination and ending status.

Table 6-7: COMPLETION STATUS BYTE

BYTE \ BIT	7	6	5	4	3	2	1	0
00	Reserved			InStat	Busy	Equal	Check	Reserv

Bits 0, 5, 6 & 7 : MUST be zero.

Bit 1: Check condition. Sense is available. See REQUEST SENSE below.

Bit 2: Equal. Set when any SEARCH is satisfied.

Bit 3: Busy. Device is busy or reserved. Busy status will be sent whenever a Target is unable to accept a command from a Host. This condition occurs when an Host that does not allow reconnection requests an operation from a reserved or busy device.

Bit 4: Intermediate status sent. This bit is set for any intermediate status sent during a series of linked commands. This bit will not be set (regardless of the interrupt request bit) in any ending status.

REQUEST SENSE (03_H)

This command returns unit sense.

The sense data will be valid for the CHECK status condition sent to the Host and must be preserved. Sense data will be cleared on receiving a subsequent command from the Host that received the check condition.

The number-of-blocks field (byte 04) specifies the number of bytes allocated by the host for returned SENSE. Values of 0 to 3 bytes will default to 4 bytes. CHECK STATUS will not be sent in response to this command.

BYTE \ BIT	07	06	05	04	03	02	01	00
00	0	0	0	0	0	0	1	1
01	Logical Unit Number			Reserved				
02	Reserved							
03	Reserved							
04	Number of Bytes							
05*	Reserved						FlagRq	Link

* Control Byte

6.5 SENSE BYTES: Table 6-8

BYTE	BIT 7	6	5	4	3	2	1	0
00	AdrVal	Error Class			Error Code (See Tbls 9-12)			
01	Reserved			(MSB)	Logical Block Address			
02	Logical Block Address							
03	Logical Block Address							(LSB)

NOTE: The address valid bit (byte 00, bit 07) indicates that the Logical Block address bytes contain valid information.

6.5.2. SENSE KEYS

The extended sense data format (not supported on the ACB-4000) is indicated by an error calss of 7. It provides for passing additional infornation including the sense key field. (For additional Information refer to the SCSI Specification.)

The Sense Key is a device independent code designed to aid the system in resolving the following Sense Data:

00 = No Sense
01 = Recoverable Error
02 = Not Ready
03 = Media Error (Non Recoverable)
04 = Hardware Error (Non Recoverable)
05 = Illegal Request
06 = Media Change
07 = Write Protect
08 = Diagnostic Unique
09 = Vendor Unique
0A = Power Up Failed
0B = Aborted Command
0C = Condition Met

Table 6-10: CLASS 00 ERROR CODES IN SENSE BYTE (DRIVE ERRORS)

CODE	ERROR
00	NO SENSE
01	NO INDEX SIGNAL
02	NO SEEK COMPLETE
03	WRITE FAULT
04	DRIVE NOT READY
05	DRIVE NOT SELECTED *
06	NO TRACK 00
07	MULTIPLE DRIVES SELECTED *
08	NO ADDRESS ACKNOWLEDGED *
09	MEDIA NOT LOADED *
0A	INSUFFICIENT CAPACITY *
0B - 0F	NOT ASSIGNED

* Not supported on ACB-4000

Table 6-11: CLASS Ø1 ERROR CODES IN SENSE BYTE (TARGET ERRORS)

CODE	ERROR
1Ø	I.D. CRC ERROR
11	UNCORRECTABLE DATA ERROR
12	I.D. ADDRESS MARK NOT FOUND
13	DATA ADDRESS MARK NOT FOUND
14	RECORD NOT FOUND
15	SEEK ERROR
16-17	NOT ASSIGNED
18	DATA CHECK IN NO RETRY MODE
19	ECC ERROR DURING VERIFY
1A	INTERLEAVE ERROR
1B	NOT ASSIGNED
1C	UNFORMATTED OR BAD FORMAT ON DRIVE
1D	SELF TEST FAILED
1E	DEFECTIVE TRACK (MEDIA ERRORS)
1F	NOT ASSIGNED

Table 6-12: CLASS Ø2 ERROR CODES (SYSTEM-RELATED ERRORS)

CODE	ERROR
2Ø	INVALID COMMAND
21	ILLEGAL BLOCK ADDRESS
22	NOT ASSIGNED
23	VOLUME OVERFLOW
24	BAD ARGUMENT
25	INVALID LOGICAL UNIT NUMBER
26 - 2F	NOT ASSIGNED

12 MAY 83 PRB

APPENDIX A

Configuring the ACB4000

NOTE: This note applies to boards with PROMS serial 10500 and above.

A.1 Configuration Requirements The controller board generally requires very little hardware configuration. The controllers address on the SCSI bus is set up by jumpers. For most environments that is all that is necessary. The exceptional case involves write precompensation. Depending on the drives being used this will vary (However 90% of the drives on the market can use the default setting).

A.2 Controller SCSI Bus Address The controller will respond to any of the eight possible bus addresses. For systems with multiple peripherals it is suggested that the disk controller be assigned a relatively high address. However, in the environments where most ACB4000 controllers will be used address zero is accpetable. Note that some low-end host adapters will generate only address zero.

The controllers bus address is selected by installing jumpers in positions A-B, C-D and E-F of the jumper block J5.

The binary code for the bus address is programmed in these jumpers with position A-B being the least significant bit and E-F being the most significant bit. For bus address seven install all three of these jumpers. For bus address four install A-B and C-D.

A.3 Diagnostic Mode. The jumper at O-P places the controller in a diagnostic only mode. For normal operation this jumper should not be installed.

A.4 The Write Precomp Jumper Drives from different manufacturers have differing requirements for write precompensation. Generally these can be accomodated by the parameters supplied with the MODE SELECT command at format time. The general case is that write precomp is enabled at the same time as reduced write current. Given that almost all drives ignore the reduced write current line this means that the jumper option that ties these two signals together allows full control of precomp by the format parameters. Thus precomp can be always on, always off, or something in between, further, it means that the two drives can handle this differently. See table entry S below.

Unfortunately, not every drive can be supported in this mode. There are three cases to be considered: (1) Drive uses Reduced Write Current (as reduced write current function) and requires precompensation either on all cylinders or none; (2) Drive uses the reduced write current line as another head select bit (eg. Maxtor); or (3) Drive requires both reduced write current and precompensated write data but at differing cylinder numbers.

In the first case, set the reduced write current cylinder up in the MODE SELECT parameters according to the manufacturers recommendations and set the precomp jumper as R or T. See Table.

For drives which use the reduced write current line as a high order head select bit (this implies 9 or more data heads) set the precomp jumper as R or T. Note that this limits the choices for the other drive on the controller if it is not the same. (Maxtor uses thin film media which does not want precomp so both drives have to use no precomp.)

The third case, that of differing reduced write current and precomp cylinders, sounds like a problem but usually isn't. The effect of precomp (or the lack thereof,) on a solid data separator is usually negligible for all but the inner 25% of the cylinders on a disk. So try using the S option in the table with the reduced write current as suggested by the disk manufacturer. Or get an opinion from the disk manufacturer technical support staff.

The precomp jumper is adjacent to J1, between U5 and U6. The table gives the effect of the three jumper setting options.

Precomp Code:	Install jumper:	Impact of this setting:
R	R to PU (or no jumper)	Always Disable Precomp
S	R to S	Precomp tied to Reduced Write Current Line
T	R to T	Always Enable Precomp