1

Overview

The AIC-6360 is a single chip PC-AT® bus to SCSI bus host adapter designed to bring the power and connectivity of SCSI to the computer system motherboard. This chip provides all of the functionality needed to implement a SCSI-2 bus in one 68-pin PLCC, 80-pin QFP or 100-pin TQFP package. Embedding the AIC-6360 increases reliability, reduces cost and eliminates the need for a traditional host adapter card. This makes the AIC-6360 an ideal I/O solution for high performance, single-user desktop and portable systems.

The AIC-6360 is an upgraded version of the AIC-6260 and is pin- and software-compatible with that chip. It is also software-compatible with the AHA-1510/1520/1522 family of host adapters.

The AIC-6360 can connect to any of the growing number of currently available SCSI-compatible peripherals, including fixed disk drives, high-capacity floppy drives, tape drives, CD-ROM drives, and removable media drives. The AIC-6360 hardware has a sustained data transfer capability of up to 10 MBytes/second and can perform Fast SCSI-2 transfers at up to 10 MBytes/second on the SCSI bus.

The AIC-6360 allows the host computer to access the SCSI bus with flexibility, while at the same time automating the more time-consuming SCSI functions like selection and reselection. The AIC-6360 supports 8-bit and 16-bit data transfers with 2nd party DMA or programmed I/O (PIO). It also supports 32-bit double-word PIO transfers for increased efficiency and transfer rates. All data transfers go through an internal 128-byte data buffer (FIFO). Both synchronous and asynchronous SCSI transfers are supported.

The AIC-6360 supports EISA DMA type A and B (4 MBytes/second) cycles. It includes an enlarged 32-byte stack memory for programmers' convenience. A built-in *sleep* mode saves power on the chip.

Configuration options on the AIC-6360 are programmable and can be set by software during system power up. These options include:

- Enable/Disable Disconnect
- AT Bus On/Off Time
- Selection Time Out
- Parity Checking Disable
- DMA/PIO
- SCSI ID
- Synchronous Negotiation

The Adaptec *aspi2dos* software product supports the AIC-6360. This multitasking ASPI (Advanced SCSI Programming Interface) manager for DOS includes features such as Disconnect/Reconnect on the SCSI bus. Disconnect/Reconnect frees the host CPU while peripherals execute time-consuming functions such as seeks. Up to eight simultaneous I/O tasks can be run in the background, and the driver also allows interrupts from the host CPU. Automatic Request Sense can be done in the event of a

Check Condition status from a SCSI target LUN, thus assuring that valuable status data is not lost.

The AIC-6360 BIOS code allows booting from the SCSI fixed disk drive and emulation of DOS fixed disk calls. Compatibility is assured by support of the ANSI Common Command Set and SCSI-2.

Figure 1-1 shows how the AIC-6360 fits in with the SCSI bus and the host computer's ISA bus. As you can see, the AIC-6360 is truly a single-chip SCSI solution.

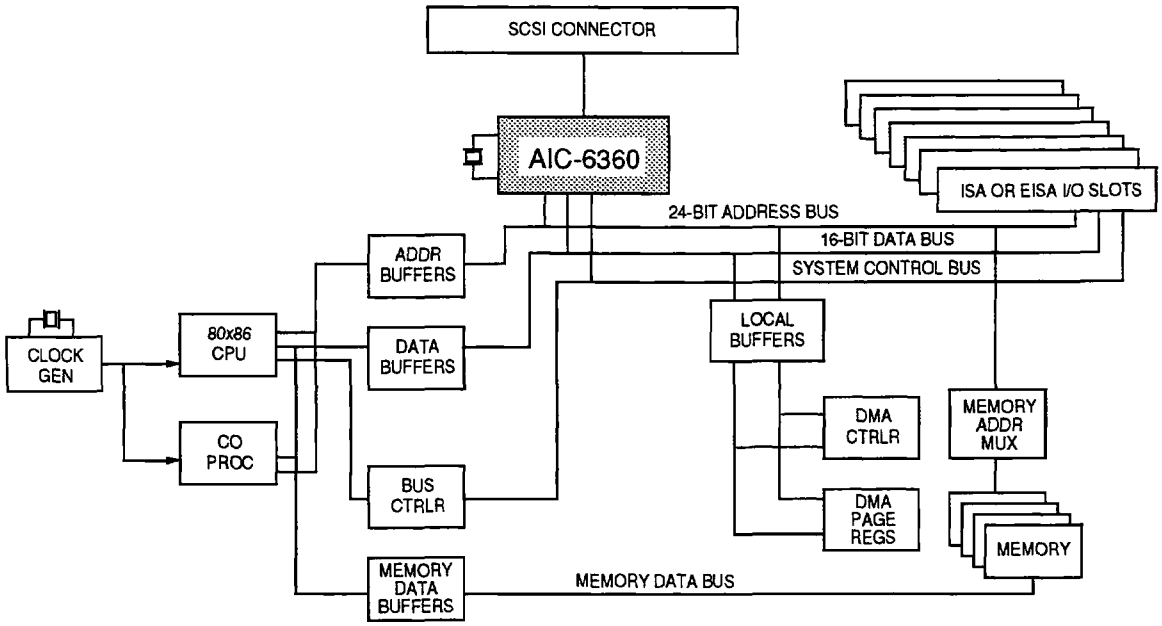


Figure 1-1. AIC-6360 Block Diagram

2

Pin Information

Pin Locations

The AIC-6360 chip is available in the following packages:

- 80-pin QFP
- 100-pin TQFP
- 68-pin PLCC

Figures 2-1, 2-2 and 2-3 show the pin locations for each of these packages.

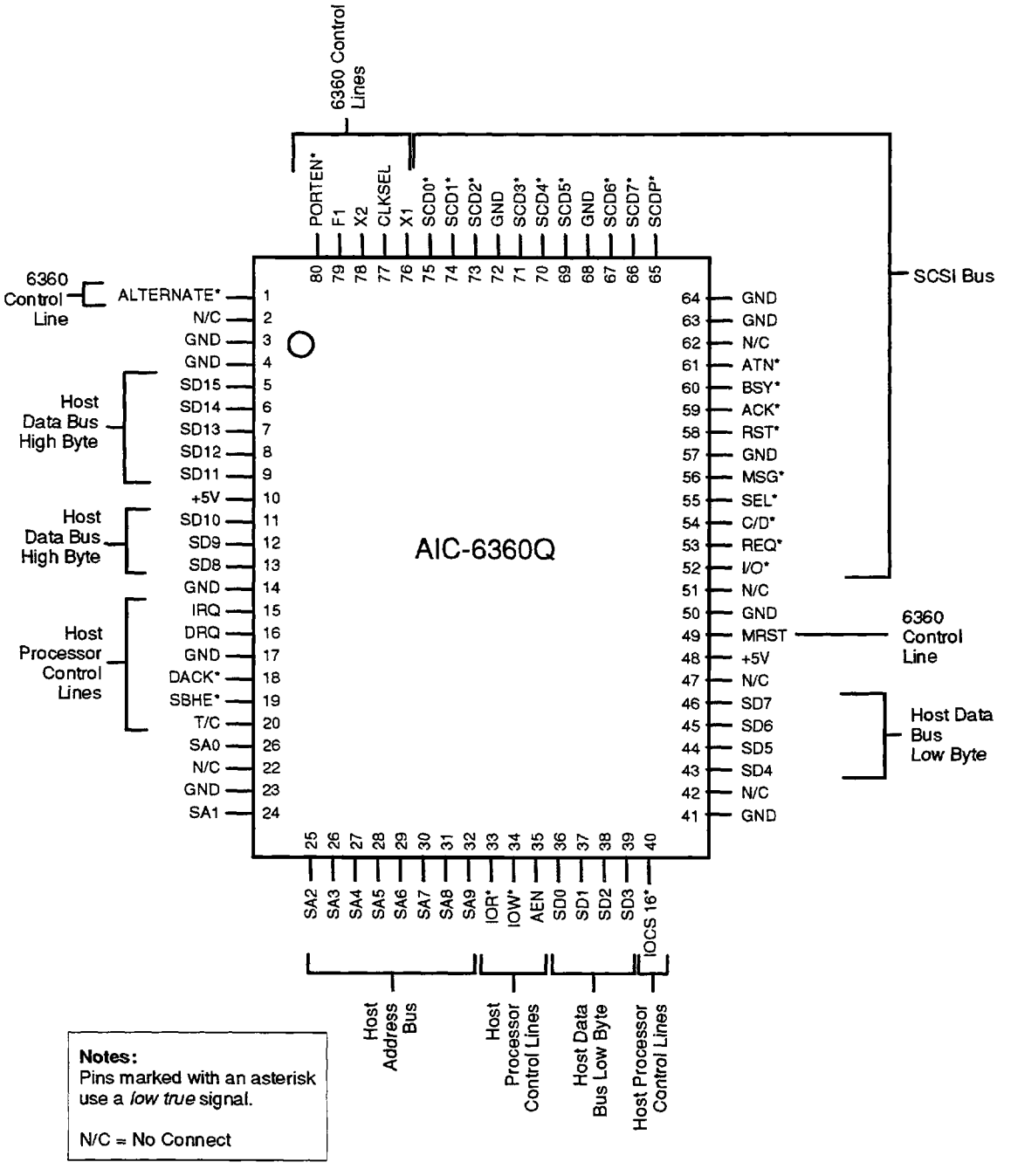


Figure 2-1. AIC-6360Q 80-Pin Plastic Quad Flat Pack

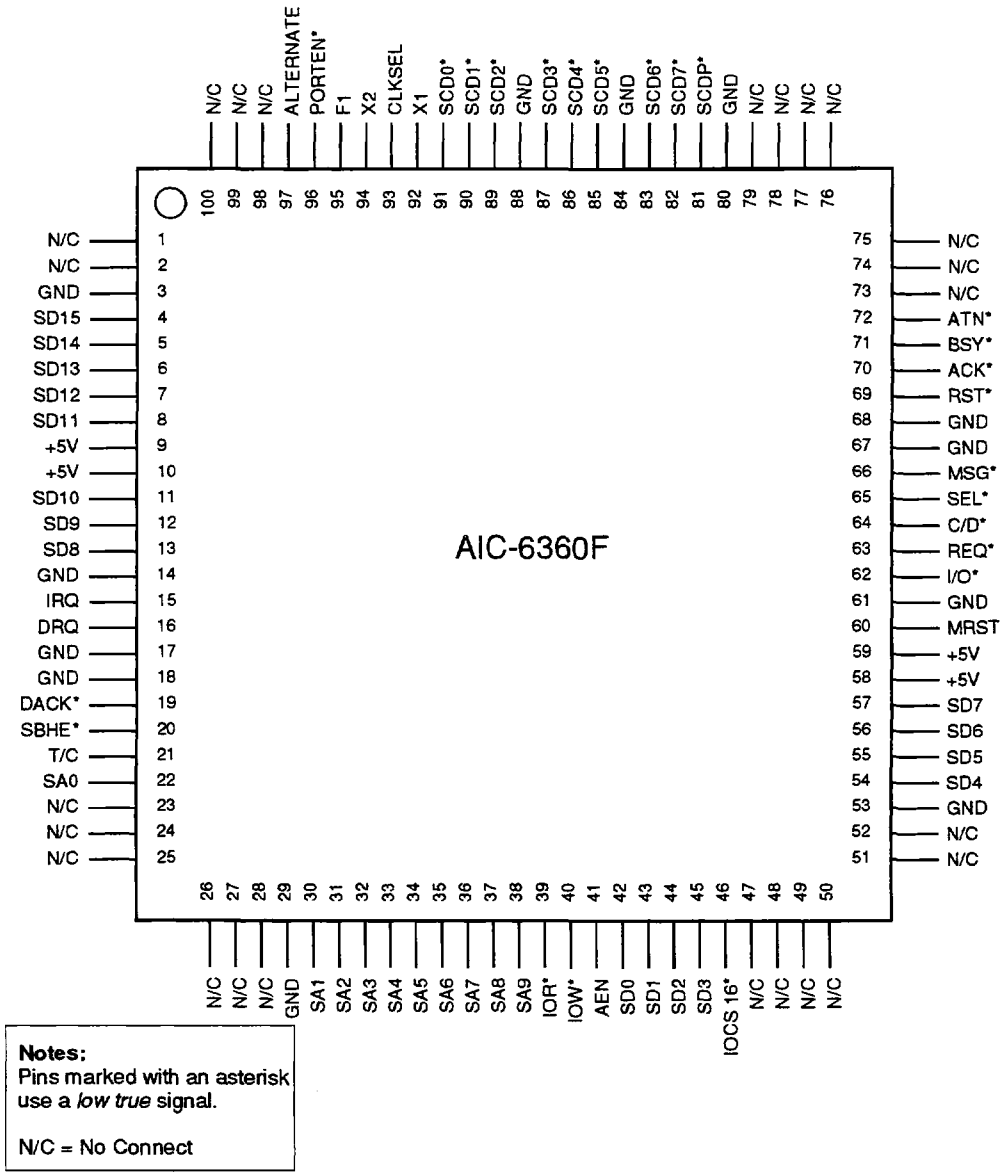


Figure 2-2. AIC-6360F 100-Pin TQFP Package

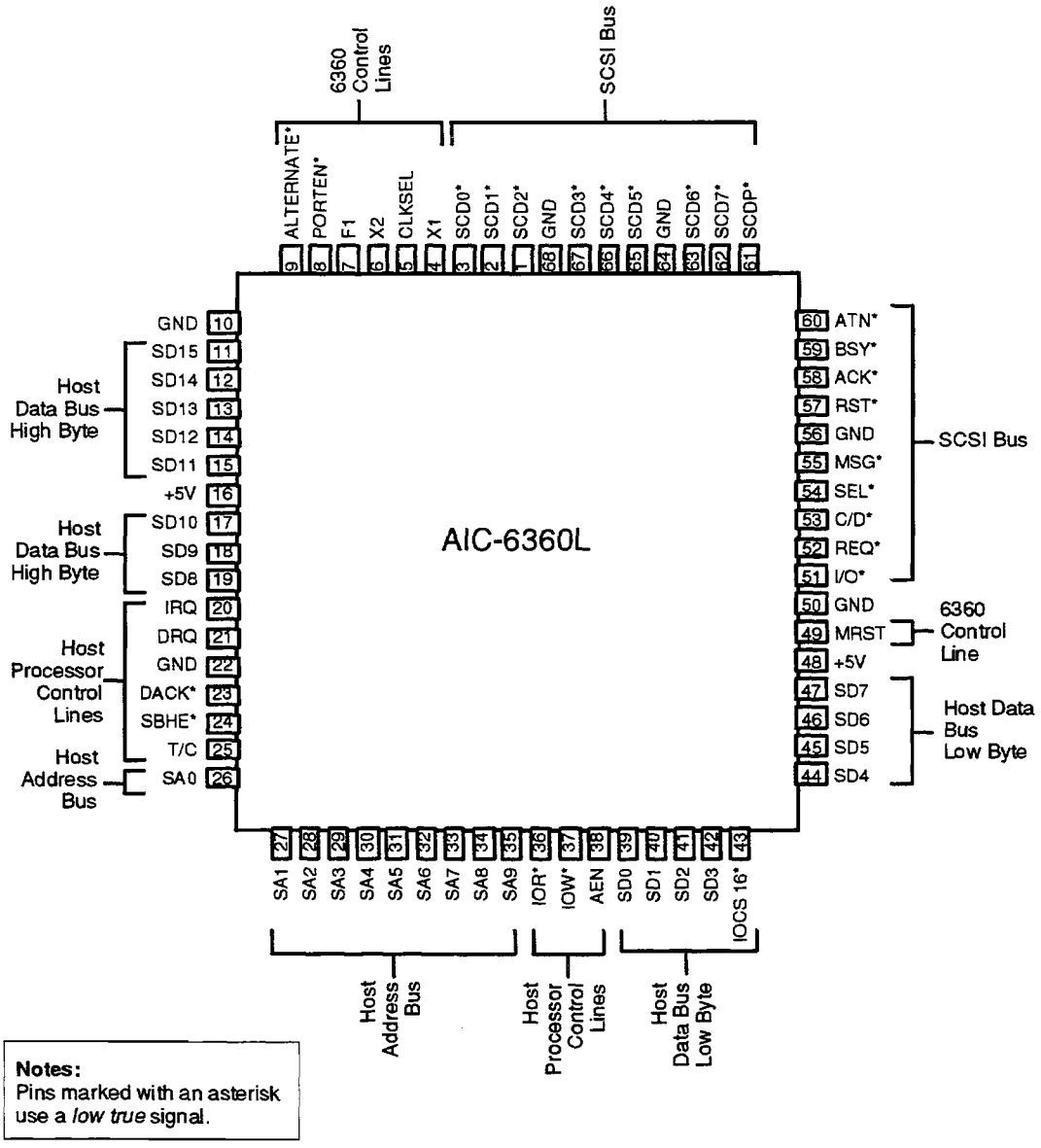


Figure 2-3. AIC-6360L 68-Pin PLCC Package

Pin Descriptions

Here are descriptions of all AIC-6360 pins. For convenience, they are divided into AT Interface Pins, SCSI Pins, and Other Pins. An asterisk (*) indicates that the pin uses a *low true* signal.

Table 2-1. AT Interface Pins

Symbol	Type	Description
SA0-SA9	I	**System Address Lines.** A 10-bit bus used to load addresses into the AIC-6360 from the host. Chip addresses are decoded at 340h with ALTERNATE* tied high, and at 140h with ALTERNATE* tied low.
AEN	I	**Address Enable.** A control signal used to indicate the type of transfer taking place across the host bus. This signal is low for I/O access and high for DMA transfers.
ALTERNATE*	I	**Alternate I/O Address Decode.** When tied high, chip addresses are decoded from 340h. When tied low, chip addresses are decoded from 140h.
SD0-SD15	I/O	**System Data Lines.** Eight-bit transfers use SD0-SD7. 16-bit data transfers use SD0-SD15. Data transfers include register values and data. The host data bus utilizes tri-state drivers (IOH = –8 mA, IOL= 24 mA).
DRQ	O	**DMA Request.** A data transfer control signal used to indicate that the AIC-6360 has data to send or is ready to receive data. This signal, which forms half of the DMA handshake, is valid for DMA mode transfers only. DRQ utilizes a two-state driver (IOH = –8 mA, IOL= 24 mA).
DACK*	I	**DMA Acknowledge.** A data transfer control signal used to indicate that the host is ready for a DMA transfer. This signal, which forms half of the DMA handshake, is valid for DMA mode transfers only.
IRQ	O	**Interrupt Request.** A control signal used to indicate the occurrence of a condition requiring host intervention. This is the signal used for all SCSI interrupts. Only interrupts which have been enabled can assert this signal. This signal is driven high by the DMA controller during the last DMA data transfer to signal the end of the transfer. IRQ uses a two-state driver (IOH = –8 mA, IOL= 24 mA).
IOR*	I	**I/O Read.** A control signal used to indicate direction of data transfer across the host bus. When asserted (active low), it indicates that data is being read out of the AIC-6360.

Continued

Table 2-1. AT Interface Pins (continued)		
Symbol	**Type**	**Description**
IOW*	I	**I/O Write.** A control signal used to indicate direction of data transfer across the host bus. When asserted (active low), it indicates that data is being written to the AIC-6360.
T/C	I	**Terminal Count.** A control signal used to indicate the completion of a DMA transfer. This signal is driven by the host DMA controller.
SBHE*	I	**System Bus High Enable.** This signal indicates that data on the SD8-SD15 lines is valid.
RESET	I	**System Reset.** This signal is active high when the system is powered up or when there is a hard system reset. This signal has hysteresis for noise immunity. (1.5V Vth+ 2.0V; 0.6V Vth- 1.1V; Vth+ - Vth- = 0.4V)
IOCS 16*	O	**I/O Chip Select 16.** This signal is driven low when the current I/O data transfer is 16 bits (one word) wide. (Open collector driver, IOL=24 mA)

Table 2-2. SCSI Pins

Symbol	Type	Description
SCD0-7*	I/O	**SCSI Data Bus.** An 8-bit data bus used to transfer data between the AIC-6360 and devices on the SCSI bus. Data transfers include SCSI commands, status, messages and user data. Used during information transfer phases on the SCSI bus.
SCDP*	I/O	**SCSI Data Parity.** A control signal used to check for data transfer errors on the SCSI bus. This signal with SCSI data always generates odd parity when the AIC-6360 is driving the SCSI bus. This signal is tested when the AIC-6360 is receiving and parity checking is enabled.
RST*	I/O	**SCSI Reset.** A control signal used to restore devices attached to the SCSI bus to their start-up condition. This signal is driven under programmed control. When detected, RST* may cause the assertion of IRQ.
ATN*	I/O	**SCSI Attention.** A control signal used to indicate that an initiator wishes to send a message out to a target. ATN* is driven when the AIC-6360 is in initiator mode and is detected when the AIC-6360 is in target mode.
BSY*	I/O	**SCSI Busy.** A control signal used for bus arbitration and device selection on the SCSI bus.

Continued

Table 2-2. SCSI Pins (continued)

Symbol	Type	Description
SEL*	I/O	**SCSI Select.** A control signal used for device selection on the SCSI bus.
C/D*	I/O	**SCSI Control/Data.** A control signal driven by the target to indicate the type of transfer taking place across the SCSI bus (SCD0–7)[1]. C/D* is driven when the AIC-6360 is in target mode and is detected when it is in initiator mode.
I/O*	I/O	**SCSI Input/Output.** A control signal driven by the target to indicate the direction of transfer across the SCSI bus (SCD0–7 and SCDP). When driven low, it indicates that data is being passed from the target to the initiator. When driven high, it indicates that data is being passed to the target from the initiator.[2] I/O* is driven when the AIC-6360 is in target mode and is detected when the AIC-6360 is in initiator mode.
MSG*	I/O	**SCSI Message.** A control signal driven by the target to indicate the type of transfer across the SCSI bus (SCD0–7* and SCDP)[3]. MSG* is driven when the AIC-6360 is in target mode and is detected when the AIC-6360 is in initiator mode.
REQ*	I/O	**SCSI Request.** A data transfer control signal used to indicate that the target has data to send or is ready to receive data. This signal forms half of the SCSI data transfer handshake. REQ* is driven when the AIC-6360 is in target mode and is detected when the AIC-6360 is in initiator mode.
ACK*	I/O	**SCSI Acknowledge.** A data transfer control signal used to indicate that the initiator has sent or received data. This signal forms half of the SCSI data transfer handshake. ACK* is driven when the AIC-6360 is in initiator mode and is detected when it is in target mode.

[1] This signal indicates whether CONTROL or DATA information is on the data bus.

[2] This signal is also used to distinguish between SELECTION and RESELECTION phases.

[3] When asserted, this signal indicates the MESSAGE phase.

Note: All SCSI pins listed in Table 2-2 use open collector drivers (IOL=48 mA, input hysteresis = 0.2V).

Table 2-3. Other Pins

Symbol	Type	Description
PORTEN	O	**Port Enable Decode**. This is an address decode for an external port driver. Address bits 1-9 are included in this signal decode along with AEN. Address bit 0 must be decoded externally with IOR and IOW. (Two-state driver, IOH=-2 mA, IOL=2 mA)
+5V	I	**5-Volt Power Supply**. 5% max. variation. Two pins for PLCC package; two pins for QFP package; four pins for TQFP package.
GND	I	**Ground**. Seven pins for PLCC package; eleven pins for QFP package; twelve pins for TQFP package.
X1	I	**Crystal Input**. 20 MHz crystal input for internal oscillator.
X2	O	**Crystal Output**. 20 MHz crystal output for internal oscillator.
F1	I/O	**Clock In/Out**. This pin is either a clock input or output, depending on the state of CLKSEL. If CLKSEL is tied high, it is an output clock at the crystal frequency. If CLKSEL is left to float, it is the clock input for the AIC-6360.
CLKSEL	I	**Clock Select**. This pin selects the clock source. If tied to +5 VDC, the internal oscillator circuit is selected as the clock. In this case, CLKSEL provides Vdd for the internal oscillator. If left to float, CLKSEL is internally pulled down, thereby selecting F1 as the clock source.

3

Functional Information

The AIC-6360 is a single chip SCSI host adapter that brings the features and advantages of SCSI to the motherboard in PC-AT systems. It is pin compatible with the AIC-6260, and it is software compatible with both the AIC-6260 chip and the AHA™-1510/1520/1522 family of host adapters.

The AIC-6360 has everything necessary to implement a SCSI interface in a single package. Through its register-based host interface, it can be configured to operate as a SCSI initiator with asynchronous or synchronous SCSI data transfers. To offload the host processor, SCSI data transfers may be performed with little or no host intervention using SCSI Normal transfer mode. Alternatively, the host may have complete control over SCSI data transfers by selecting SCSI Manual PIO or SCSI Automatic PIO transfer mode.

Data transfers over the host bus may be accomplished using either Host PIO or Second Party DMA transfers. The AIC-6360 can be configured to generate interrupts for all timing critical SCSI operations. It also provides a decoded address output, simplifying the setup of two general purpose I/O ports (A and B). To aid in programming, the chip features a 32-byte stack that is accessible to and controllable by the host processor.

Although Target Mode operation functions have been implemented in the AIC-6360, the primary application is intended to be Initiator Mode. Therefore, Adaptec has developed software exclusively for Initiator Mode and has extensively tested the AIC-6360 in this mode only.

General Functional Description

This section describes the general operation and major components of the AIC-6360. Figure 3-1 is a simplified block diagram of the device. This is followed by brief explanations of each part of the diagram.

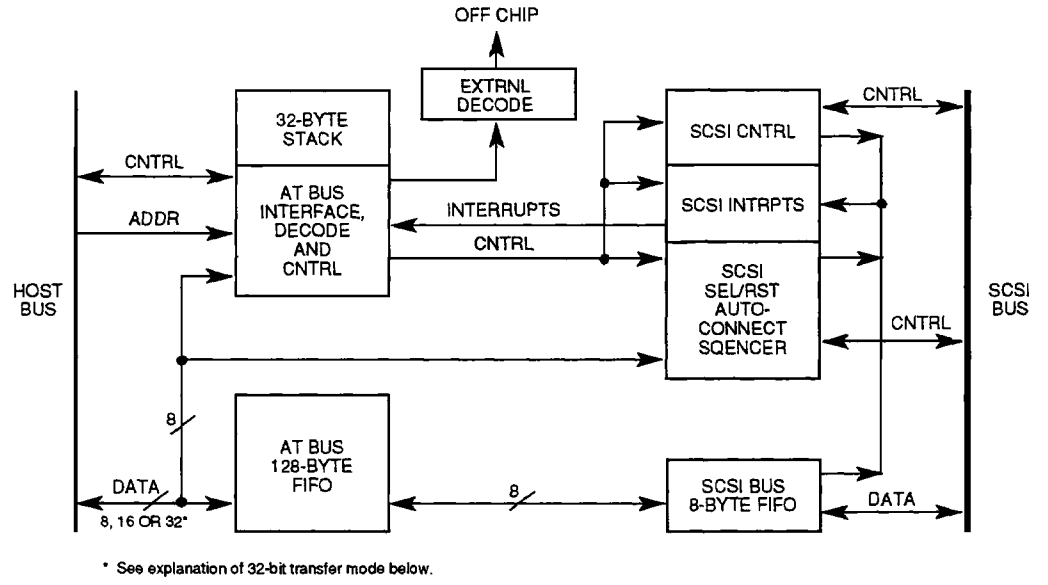


Figure 3-1. AIC-6360 Block Diagram

SCSI Controller

The SCSI controller manages the interface to the SCSI bus, including control of SCSI data transfers and sequencing of all SCSI control signals. Through its intelligence, it can offload from the host processor most of the lower level responsibilities necessary to run the SCSI bus. If desired, however, it can allow the host processor to directly manage and control the SCSI bus signals. The controller comprises the bulk of the AIC-6360's circuits, including most of the control registers in the chip.

SCSI Interrupts

Interrupts are available for all timing critical SCSI operations. The interrupt circuitry provides the ability to individually mask, clear or poll the status of any interrupt condition. For detailed information on interrupts in the AIC-6360, see *Interrupts* later in this Chapter, and see also the descriptions of the Status, Mask and Clear registers in Chapter Four, *Register Descriptions*.

SCSI Selection/Reselection Autoconnect Sequencer

This section of the SCSI controller provides the ability to have the AIC-6360 automatically arbitrate for the SCSI bus and perform either a Selection or Reselection sequence. By taking advantage of this capability, the host processor can considerably simplify the task of running the SCSI interface.

Triggering of these automatic sequences is accomplished by setting appropriate bits in the SCSI Sequence Control register (340h). However, before starting an autoconnect sequence the target/initiator IDs must first be set in the SCSI ID register (345h).

SCSI FIFO

The SCSI FIFO is an 8-byte data buffer used during SCSI Normal data transfers. Its main purpose is to buffer data during synchronous data transfers, allowing synchronous offsets of up to 8. The SCSI FIFO is not used when SCSI Manual PIO or SCSI Automatic PIO data transfer mode is selected, because these transfer modes are typically used for SCSI message, status or command phases where synchronous operation is prohibited. The status of the SCSI FIFO can be monitored by reading the SCSI Status 2 register (34Dh).

Address Mapping and External Decode

The AIC-6360 automatically maps itself onto the PC AT I/O bus by decoding ten I/O address bits input to the chip for one of two I/O address ranges, 340h-35Fh or 140h-15Fh. This self mapping ability allows the AIC-6360 to directly connect to the PC-AT I/O bus with no other support chips required. The selection of which range to decode for is under control of the ALTERNATE* input. Through these I/O address locations, the host processor controls all AIC-6360 operations and data transfers.

As part of the address mapping function, the decode logic also generates an off chip signal, PORTEN*, which is active low whenever either address 35Ah or 35Bh is valid (15Ah or 15Bh if the alternate address range is chosen).

The PORTEN* signal, combined with some off chip logic, as shown in *External Port Decode* later in this Chapter, gives you an easy means to implement two general purpose I/O ports.

Stack

To facilitate programming, a 32-byte stack in the AIC-6360 is available to the host processor. The stack pointer is located in register 353h, and stack data may be written/read at register 35Dh.

Host Interface

The host interface consists of 32 Read/Write register locations internally mapped by the AIC-6360, as described earlier. Through them, the host may control all aspects of AIC-6360 operation.

Host FIFO

To facilitate data transfer performance, the AIC-6360 features an internal 128-byte data FIFO to buffer data between the host and the AIC-6360. The host FIFO is used during either host PIO or host DMA data transfers, provided that SCSI Normal data transfer mode is also selected. Otherwise, if SCSI Manual PIO or SCSI Automatic PIO transfer modes are selected, host data is sent directly to/from the data latch at register 346h. The host FIFO is 8 bits wide with conversions to 16-bit words performed as required by internal data path logic. Host FIFO operations may be monitored by reading the DMA Status register (354h) and FIFO Status register (355h).

SCSI Data Transfers

The AIC-6360 can be programmed to operate as either a SCSI initiator or a SCSI target by loading the SCSI Sequence Control register (340h) with the correct values. Note that some functions behave differently between Initiator and Target modes. To configure the chip for either Initiator or Target modes, see Chapter Five, *Application Notes*. The AIC-6360 can support both asynchronous and synchronous data transfers across the SCSI bus. To assist in data transfer control, a 24-bit transfer counter is available (registers 348h, 349h, 34Ah) which counts each SCSI bus REQ/ACK handshake and generates an interrupt or status condition when terminal count is reached.

Data transfers through the AIC-6360 to the SCSI bus can be performed using one of three data transfer modes. Operational status in each mode can be monitored through interrupts or by polling for status.

- **SCSI Manual PIO:** In this mode the host processor controls all aspects of the SCSI interface, with the AIC-6360 acting merely as a bus buffer.
- **SCSI Automatic PIO**: In this mode the host processor provides most of the control, with the AIC-6360 providing automatic SCSI bus REQ/ACK handshaking.
- **SCSI Normal**: Using the intelligence of the AIC-6360, this mode allows the host processor to offload the SCSI transfer operation to the AIC-6360. The AIC-6360 will run the SCSI interface and keep track of the transfer count, after being initially set up by the host processor. This mode uses the AIC-6360 internal FIFOs for maximum transfer performance.

SCSI Manual PIO Mode

In SCSI Manual PIO mode, the host processor reads or writes directly to the SCSI data bus via the latch at 346h and can monitor or control the SCSI bus control lines via the register at 343h. In this mode, the AIC-6360 is essentially a bus buffer with no control functions. Note that SCSI Manual mode supports asynchronous SCSI transfers only and that the internal data FIFOs are not used. This mode is typically used for SCSI Command, Message or Status phases where decision making and control, rather than data transfer speed, are of primary importance. To select this mode, set SPIOEN=0 and DMAEN=0 (bits 3 and 6) in the SCSI Transfer Control 0 register (341h).

SCSI Automatic PIO Mode

In SCSI Automatic PIO mode the host processor writes to or reads from the SCSI data bus via the latch at 346h, with the AIC-6360 handling the REQ/ACK handshaking to transfer data across the SCSI bus. The SPIORDY bit in the SCSI Interrupt Status 0 register at 34Bh signals transfer completion and can be polled or set to generate an interrupt. This mode supports asynchronous SCSI transfers only and bypasses the internal data FIFOs.

SCSI Automatic PIO mode is typically used for SCSI command, message or status phases where decision making and control, rather than data transfer speed, are of primary importance. To select this mode, set SPIOEN=1 and DMAEN=0 (bits 3 and 6) in the SCSI Transfer Control 0 register (341h).

SCSI Normal Mode

In SCSI Normal mode, the AIC-6360 will automatically handle the SCSI data transfer and will provide the fastest transfer performance. In this mode, the internal FIFOs are used and the data path through the chip is from the host bus, through the host FIFO, through the SCSI FIFO and finally out onto the SCSI bus.

SCSI Normal mode, which supports *both* asynchronous and synchronous SCSI transfers, is usually used during the Command and Data phases on the SCSI bus. To select this mode, set SPIOEN=0 and DMAEN=1 (bits 3 and 6) in the SCSI Transfer Control 0 register (341h). The controls for synchronous SCSI transfers are located in the SCSI Rate Control register (344h).

Host Processor Data Transfers

Data transfers between the host bus and the AIC-6360 can take place using either of the following two modes:

- **Host PIO**: Through Programmed I/O the host processor handles the data transfer into/out of the AIC-6360.
- **Host DMA**: Data transfers between the host and the AIC-6360 are run by a DMA controller in the host system.

Selection of host data transfer mode is controlled through the DMA Control 0 register (352h).

Host PIO Mode

In host PIO mode, the host processor writes to or reads from the 128-byte host FIFO via the 16-bit data register at 356h or the 32-bit register at 358h. By taking advantage of the Repeat Instring instruction found in 286/386/486 processors, very high data transfer rates are possible. In addition, the AIC-6360 host FIFO addressing supports the use of the instring double word instruction on 386/486 processors for greater efficiency and higher data throughput.

Double Word Transfers

The AIC-6360 supports 32-bit double word transfers in systems with 386 or 486 microprocessors. The double word transfer allows the microprocessor to initiate 32-bit I/O instructions when accessing data from the FIFO located on the AIC-6360. This results in one double word operation instead of two single word operations (16-bit instructions) performed back-to-back. Double word operation improves overall performance by reducing the latency between two 16-bit data transfers. Additionally, recovery time is reduced by not having to sync four times to transfer the data. Double word transfers can improve performance by as much as 20%.

Bit 4 in register 352h must be set to enable double word data transfers. Clearing this bit configures register 356h as a normal 16-bit data port. Setting this bit allows data transfers to or from addresses 356h and 358h to access the data port. When you use this option, bit 6 (8-bit/16-bit) of the same register (352h) should always be reset. Double word accesses to the AIC-6360 FIFO must always be done on a double word boundary (358h).

Figure 3-2 shows a typical AIC-6360 system implementation. Since the ISA bus is 16 bits wide, a 32-bit processor instruction requires two words to be assembled by the chipset before the data is presented to the microprocessor. Chipsets latch one word after another before the processor samples the data by generating the RDY signal.

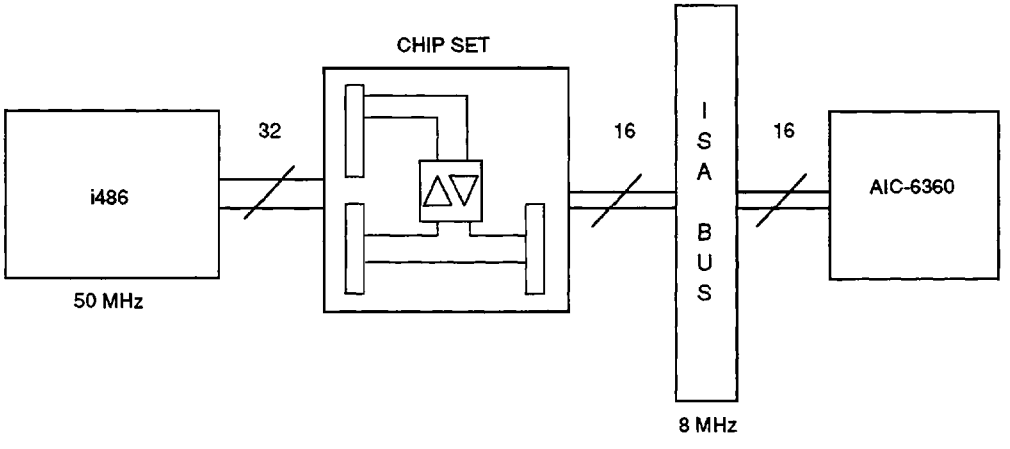


Figure 3-2. Double Word System Diagram

Chipsets translate a single 32-bit instruction into a set of double ISA commands, as shown in the read operation timing diagram in Figure 3-3.

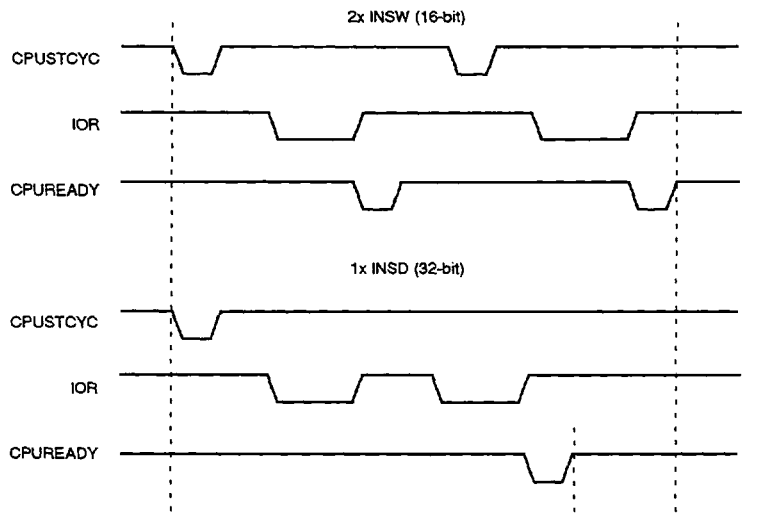


Figure 3-3. 32-bit Double Word Timing

When a write occurs the 32-bit data is split into two single words which are presented to the ISA bus one after another. The timing diagram makes it clear that for 16-bit operations the chipset must sync twice from the processor clock to the bus clock (generate IOR/IOW) and twice from the bus clock to the processor clock (generate RDY). For double word operations, however, the chipset syncs only once at each side of IOR/IOW.

Host DMA Mode

In host DMA mode, the host processor sets up the data transfer operation by loading a system DMA controller with a memory pointer and the transfer count. The host DMA controller then writes data to or reads data from the AIC-6360 host FIFO via the data register at 356h. Once begun, host DMA transfers run to completion without further host processor intervention.

The AIC-6360 supports 8- and 16-bit DMA transfers and EISA Type A and B DMA transfers.

Interrupts

The AIC-6360 can be configured to generate interrupts for all transfer critical conditions. There are several sources of interrupts. Most occur because of SCSI bus conditions. These interrupts are listed in SSTAT0 and SSTAT1. Interrupts are controlled through a set of internal registers, as shown in Table 3-1. Each interrupt condition has a readable status bit and controlling enable and clear bits.

Table 3-1. Interrupts

Status Bit Name	Status Bit	Status Register Address	Enable Bit	Enable Register Address	Clear Bit	Clear Register Address
SELDO	6	34Bh r	6	350h	6	34Bh w
SELDI	5	34Bh r	5	350h	5	34Bh w
SELINGO	4	34Bh r	4	350h	4	34Bh w
SWRAP	3	34Bh r	3	350h	3	34Bh w
SDONE	2	34Bh r	2	350h	2	34Bh w
SPIORDY	1	34Bh r	1	350h	1	34Bh w
DMADONE	0	34Bh r	0	350h	0	34Bh w
SELTO	7	34Ch r	7	351h	7	34Ch w
ATNTARG	6	34Ch r	6	351h	6	34Ch w
SCSIRSTI	5	34Ch r	5	351h	5	34Ch w
PHASEMIS	4	34Ch r	4	351h	n/a	n/a
BUSFREE	3	34Ch r	3	351h	3	34Ch w
SCSIPERR	2	34Ch r	2	351h	2	34Ch w
PHASECHG	1	34Ch r	1	351h	1	34Ch w
REQINIT	0	34Ch r	0	351h	0	34Ch w
SWINT	0	352h	2	352h w	0	352h w

The **status bit** reflects the current state of the interrupt source independent of interrupts being enabled. It may be read by the host processor at any time to obtain a real time indication of the condition. Removing the condition that caused the status bit to be latched does not always clear the status bit. Refer to the descriptions of the status bits and their corresponding clear bit to determine the exact conditions under which they are cleared.

The **enable bit** gates the entry of the status bit into the interrupt processing chain and essentially serves as an interrupt mask. In order for a condition to cause an interrupt, its enable bit must be set, otherwise the interrupt associated with the condition is suppressed.

The **clear bit** resets the interrupt latch corresponding to the particular interrupt condition. The interrupt latch will be set if the corresponding enable bit was set allowing the status bit condition to propagate. By clearing the interrupt latch, the interrupt condition will be removed from generation of the interrupt signal output on the IRQ pin. In some, but not all, cases the clear bit will also clear the status bit. Refer to the description of each status bit to determine the exact conditions under which they are cleared.

All interrupt sources shown in Table 3-1 are logically OR'd to form the signal output on the IRQ pin. The OR of all these sources is available for monitoring on the INSTAT status bit in the DMA Status register at 354h. A master enable is also available to gate the signal going out on the IRQ pin. If the INTEN bit of the DMACNTRL0 register at 352h is reset, no interrupts will be output on the IRQ pin. INSTAT is valid even if the INTEN bit is reset.

External Port Decode

As described previously, the AIC-6360 self-maps its internal registers to an I/O address space of 340h to 35Fh (140h to 15Fh if ALTERNATE* is low). Addresses 35Ah and 35Bh (15Ah and 15Bh if ALTERNATE* is low) are not used internally, but when they are accessed either one will drive a Port Enable pin. (For timing information, see the timing diagrams for Host Processor I/O Read and Write Operation in Chapter Six, *Electrical Information.*) This provides a convenient way to add general purpose I/O ports external to the AIC-6360. These external ports may be used for control outputs or configuration input, in conjunction with general AIC-6360 SCSI operation.

By combining the active low PORTEN* output with the I/O bus IOW*, IOR* and SA0 as shown in Figure 3-4, select signals for up to two read and two write bus transceivers are easily generated.

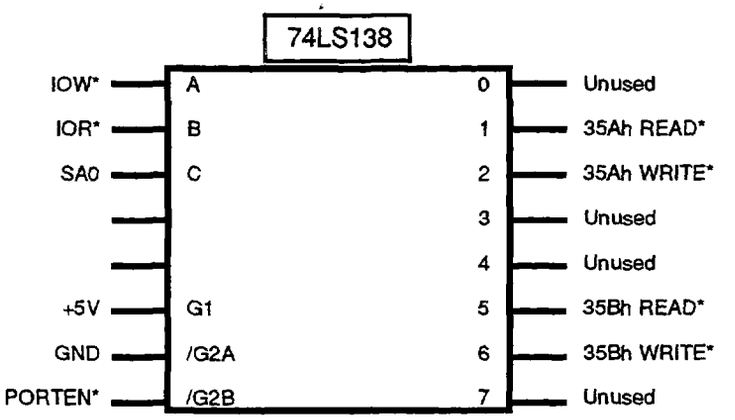


Figure 3-4. Typical External Logic Circuit

Clocking

The AIC-6360 requires a 20 MHz clocking source in order to operate. The clocking source may be supplied externally, or the internal crystal oscillator circuit in the AIC-6360 may be used. The advantage of using an external source is that power savings of up to one-third of total AIC-6360 power consumption may be realized by shutting down the internal oscillator circuits. (See Chapter Six, *Electrical Information,* for the crystal oscillator specification.)

To use the internal oscillator, the CLKSEL pin must be connected directly to +5 VDC in order to supply a power source to the internal oscillator circuits. In addition, a 20 MHz crystal must be connected to the X1, X2 pins. The generated clock signal will also be output on the F1 pin for use elsewhere, if desired.

To input an external clocking signal, the internal oscillator circuits must be powered down by disconnecting the CLKSEL pin. Internally, CLKSEL will be grounded by a pulldown resistor. Better yet, it should be externally grounded. By powering down

the oscillator circuits, the direction of the F1 buffer is changed, allowing the external clocking source to be input. The external clocking source should ideally have a 50% duty cycle; a range of 40% to 60% is acceptable. Voltage input requirements are TTL levels.

Power Management

A unique feature of the AIC-6360 is the ability to allow you to manage chip power consumption. The three major components of AIC-6360 power consumption are shown in Figure 3-5.

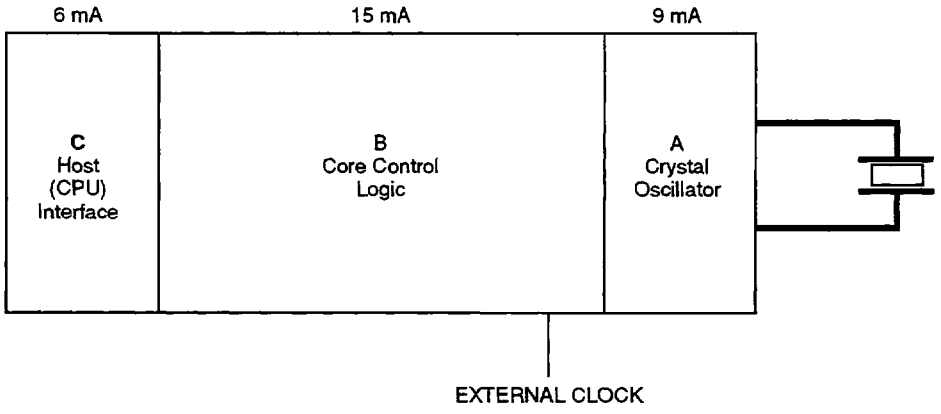


Figure 3-5. AIC-6360 Power Components

Power component A operates the on-board crystal oscillator circuit and nominally draws about 9 mA. It can be avoided entirely by using an external clock source input on the F1 pin, as described in the previous section. Power component B (nominally 15 mA) is drawn by the bulk of the AIC-6360 circuits and may be turned off during periods of inactivity by activating the Powerdown-Sleep mode. Power component C (nominally about 6 mA) consists of current used to maintain the host processor interface so that the host processor can always access the AIC-6360 control registers. This is the minimum amount of power the chip can draw while still maintaining host processor control and access.

Powerdown-Sleep Mode

During periods of inactivity, the AIC-6360 may be shut down by the host processor to achieve power savings. Powerdown-Sleep mode works by shutting off the clock to most of the AIC-6360 circuits. Removing the clock reduces power to a static level, saving power component B. Powerdown mode is entered by setting bit 7 of the DMACNTRL1 register (353h) and is exited by either resetting the bit or performing a chip master reset.

During powerdown the AIC-6360's host processor interface circuits are still active, allowing manipulation of the AIC-6360 register set by the host processor. If no AIC-6360 operations at all are expected, the chip may be shut down entirely by turning off all clock sources to the chip. As long as the power supply voltage is maintained, the AIC-6360 will statically maintain all register values.

> Note
> During powerdown the AIC-6360 cannot perform or respond to any SCSI operations. For this reason, any pending operations must first be cleared before entering powerdown mode. To minimize power consumption, the AIC-6360 software device driver and BIOS available from Adaptec implement powerdown as described.

Testing

To assist in test development, the AIC-6360 features two test control registers: SCSI Test Control (34Eh) and Test Register (35Eh). These registers allow internal counters to be tested more easily and provide access to internal logic points.

❒

4

Register Descriptions

This chapter contains information on the AIC-6360's internal registers. Each register is described under its own heading, identified by name and address.

There are 37 registers, normally decoded from 340h through 35Fh. If ALTERNATE* is asserted (low), the registers are decoded from 140h. Registers are written and read by the host processor via the host bus, in I/O address space.

Table 4-1 is an address map of the AIC-6360 registers.

Register Summary

Table 4-1. AIC-6360 Register Address Map

340h SCSISEQ	341h SXFRCTL0	342h SXFRCTL1	343h SCSISIG	343h SCSISIG	344h SCSIRATE
R/W	R/W	R/W	W	R	W
7 TEMODEO	7 SCSIEN	7 BITBUCKET	7 CDO/CDEXP	7 CDI	7 Reserved
6 ENSELO	6 DMAEN	6 SWRAPEN	6 IOO/IOEXP	6 IOI	6 SXFR [2]
5 ENSELI	5 CHEN	5 ENSPCHK	5 MSGO/MSGEXP	5 MSGI	5 SXFR [1]
4 ENRSELI	4 CLRSTCNT	4 STIMESEL [1]	4 ATNO	4 ATNI	4 SXFR [0]
3 ENAUTOATNO	3 SPIOEN	3 STIMESEL [0]	3 SELO	3 SELI	3 SOFS [3]
2 ENAUTOATNI	2 Reserved	2 ENSTIMER	2 BSYO	2 BSYI	2 SOFS [2]
1 ENAUTOATNP	1 CLRCH	1 BYTEALIGN	1 REQO	1 REQI	1 SOFS [1]
0 SCSIRSTO	0 Reserved	0 Reserved	0 ACKO	0 ACKI	0 SOFS [0]

345h SCSIID	345h SELID	346h SCSIDAT	347h SCSIBUS	348h STCNT0	349h STCNT1
W	R	R/W	R	R/W	R/W
7 Reserved (0)	7 SELID [7]	7 LSDB [7]	7 SDB [7]	7 STCNT [07]	7 STCNT [15]
6 OID [2]	6 SELID [6]	6 LSDB [6]	6 SDB [6]	6 STCNT [06]	6 STCNT [14]
5 OID [1]	5 SELID [5]	5 LSDB [5]	5 SDB [5]	5 STCNT [05]	5 STCNT [13]
4 OID [0]	4 SELID [4]	4 LSDB [4]	4 SDB [4]	4 STCNT [04]	4 STCNT [12]
3 Reserved (0)	3 SELID [3]	3 LSDB [3]	3 SDB [3]	3 STCNT [03]	3 STCNT [11]
2 TID [2]	2 SELID [2]	2 LSDB [2]	2 SDB [2]	2 STCNT [02]	2 STCNT [10]
1 TID [1]	1 SELID [1]	1 LSDB [1]	1 SDB [1]	1 STCNT [01]	1 STCNT [09]
0 TID [0]	0 SELID [0]	0 LSDB [0]	0 SDB [0]	0 STCNT [00]	0 STCNT [08]

Continued

Table 4-1. AIC-6360 Register Address Map (continued)

34Ah STCNT2	34Bh CLRSINT0	34Bh SSTAT0	34Ch CLRSINT1	34Ch SSTAT1	34Dh SSTAT2
R/W	W	R	W	R	R
7 STCNT [23]	7 SETSDONE	7 TARGET	7 CLRSELTIMO	7 SELTO	7 Reserved (0)
6 STCNT [22]	6 CLRSELDO	6 SELDO	6 CLRATNO	6 ATNTARG	6 Reserved (0)
5 STCNT [21]	5 CLRSELDI	5 SELDI	5 CLRSCSIRSTI	5 SCSIRSTI	5 SOFFSET
4 STCNT [20]	4 CLRSELINGO	4 SELINGO	4 Reserved (0)	4 PHASEMIS	4 SEMPTY
3 STCNT [19]	3 CLRSWRAP	3 SWRAP	3 CLRBUSFREE	3 BUSFREE	3 SFULL
2 STCNT [18]	2 CLRSDONE	2 SDONE	2 CLRSCSIPERR	2 SCSIPERR	2 SFCNT [2]
1 STCNT [17]	1 CLRSPIORDY	1 SPIORDY	1 CLRPHASECHG	1 PHASECHG	1 SFCNT [1]
0 STCNT [16]	0 CLRDMADONE	0 DMADONE	0 CLRREQINIT	0 REQINIT	0 SFCNT [0]

34Eh SCSITEST	34Eh SSTAT3	34Fh CLRSERR	34Fh SSTAT4	350h SIMODE0	351h SIMODE1
W	R	W	R	R/W	R/W
7 Reserved (0)	7 SCSICNT [3]	7 Reserved (0)	7 Reserved (0)	7 Reserved (0)	7 ENSELTIMO
6 Reserved (0)	6 SCSICNT [2]	6 Reserved (0)	6 Reserved (0)	6 ENSELDO	6 ENATNTARG
5 Reserved (0)	5 SCSICNT [1]	5 Reserved (0)	5 Reserved (0)	5 ENSELDI	5 ENSCSIRST
4 Reserved (0)	4 SCSICNT [0]	4 Reserved (0)	4 Reserved (0)	4 ENSELINGO	4 ENPHASEMIS
3 SCTESTU	3 OFFCNT [3]	3 Reserved (0)	3 Reserved (0)	3 ENSWRAP	3 ENBUSFREE
2 SCTESTD	2 OFFCNT [2]	2 CLRSYNCERR	2 SYNCERR	2 ENSDONE	2 ENSCSIPERR
1 Reserved (0)	1 OFFCNT [1]	1 CLRFWERR	1 FWERR	1 ENSPIORDY	1 ENPHASECHG
0 STCTEST	0 OFFCNT [0]	0 CLRFRERR	0 FRERR	0 ENDMADONE	0 ENREQINIT

352h DMACNTRL0	353h DMACNTRL1	354h DMASTAT	355h FIFOSTAT	356h DMADATA	357h DMADATA
R/W	R/W	R	R	R/W	R/W
7 ENDMA	7 PWRDWN	7 ATDONE	7 FCNT [7]	7 DATL [07]	15 DATH [15]
6 8BIT/-16BIT	6 ENSTK32	6 WORDRDY	6 FCNT [6]	6 DATL [06]	14 DATH [14]
5 DMA/-PIO	5 Reserved (0)	5 INTSTAT	5 FCNT [5]	5 DATL [05]	13 DATH [13]
4 DWORDPIO	4 STK [4]	4 DFIFOFULL	4 FCNT [4]	4 DATL [04]	12 DATH [12]
3 WRITE/-READ	3 STK [3]	3 DFIFOEMP	3 FCNT [3]	3 DATL [03]	11 DATH [11]
2 INTEN	2 STK [2]	2 DFIFOHF	2 FCNT [2]	2 DATL [02]	10 DATH [10]
1 RSTFIFO	1 STK [1]	1 DWORDRDY	1 FCNT [1]	1 DATL [01]	09 DATH [09]
0 SWINT	0 STK [0]	0 Reserved (0)	0 FCNT [0]	0 DATL [00]	08 DATH [08]

Continued

Table 4-1. AIC-6360 Register Address Map (continued)

358h BRSTCNTRL*	35Ah PORT A	35Bh PORT B	35Ch REV	35Dh STACK	35Eh TEST
W	R/W	R/W	R	R/W	W
7 BON [3]	7 PADAT [7]	7 PBDAT [7]	7 Reserved (0)	7 STKDAT [7]	7 Reserved (0)
6 BON [2]	6 PADAT [6]	6 PBDAT [6]	6 Reserved (0)	6 STKDAT [6]	6 BOFFTMR
5 BON [1]	5 PADAT [5]	5 PBDAT [5]	5 Reserved (0)	5 STKDAT [5]	5 BONTMR
4 BON [0]	4 PADAT [4]	4 PBDAT [4]	4 Reserved (0)	4 STKDAT [4]	4 STCNTH
3 BOFF [3]	3 PADAT [3]	3 PBDAT [3]	3 Reserved (0)	3 STKDAT [3]	3 STCNTM
2 BOFF [2]	2 PADAT [2]	2 PBDAT [2]	2 (0)	2 STKDAT [2]	2 STCNTL
1 BOFF [1]	1 PADAT [1]	1 PBDAT [1]	1 (0)	1 STKDAT [1]	1 SCSIBLK
0 BOFF [0]	0 PADAT [0]	0 PBDAT [0]	0 (1)	0 STKDAT [0]	0 DMABLK

35Fh ID		358h DMADATA[1]	359h DMADATA[1]	35Ah DMADATA[1]	35Bh DMADATA[1]
R		R/W	R/W	R/W	R/W
7 ID [7]		7 DATL [7]	15 DATH [15]	7 DATL [23]	15 DATH [31]
6 ID [6]		6 DATL [6]	14 DATH [14]	6 DATL [22]	14 DATH [30]
5 ID [5]		5 DATL [5]	13 DATH [13]	5 DATL [21]	13 DATH [29]
4 ID [4]		4 DATL [4]	12 DATH [12]	4 DATL [20]	12 DATH [28]
3 ID [3]		3 DATL [3]	11 DATH [11]	3 DATL [19]	11 DATH [27]
2 ID [2]		2 DATL [2]	10 DATH [10]	2 DATL [18]	10 DATH [26]
1 ID [1]		1 DATL [1]	09 DATH [9]	1 DATL [17]	09 DATH [25]
0 ID [0]		0 DATL [0]	08 DATH [8]	0 DATL [16]	08 DATH [24]

[1] When either DWORDPIO or ENDMA are cleared, address 358h accesses the BRSTCNTRL register and 35Ah accesses PORTA. When DWORDPIO and ENDMA are set, any access to 358h or 35Ah is redirected to the FIFO data port.

Table 4-2. AIC-6360 Register Map

ALTERNATE=5V Primary Register Address	ALTERNATE=0V Secondary Register Address	Read Register	Write Register
340	140	SCSISEQ	SCSISEQ
341	141	SXFRCTL0	SXFRCTL0
342	142	SXFRCTL1	SXFRCTL1
343	143	SCSISIGI	SCSISIGO
344	144	None	SCSIRATE
345	145	SELID	SCSIID
346	146	SCSIDAT	SCSIDAT
347	147	SCSIBUS	None
348	148	STCNT0	STCNT0
349	149	STCNT1	STCNT1
34A	14A	STCNT2	STCNT2
34B	14B	SSTAT0	CLRSINT0
34C	14C	SSTAT1	CLRSINT1
34D	14D	SSTAT2	None
34E	14E	SSTAT3	SCSITEST
34F	14F	SSTAT4	CLRSERR
350	150	SIMODE0	SIMODE0
351	151	SIMODE1	SIMODE1
352	152	DMACNTRL0	DMACNTRL0
353	153	DMACNTRL1	DMACNTRL1
354	154	DMASTAT	None
355	155	FIFO STAT	None
356	156	DMADATA	DMADATA
357	157	None	None
358	158	BRSTCNTRL/ DMADATA	BRSTCNTRL/ DMADATA
359	159	None/DMADATA	None/DMADATA
35A	15A	PORTA/DMADATA	PORTA/DMADATA
35B	15B	PORTB/DMADATA	PORTB/DMADATA
35C	15C	REV	None
35D	15D	STACK	STACK
35E	15E	None	Test
35F	15F	ID	None

Register Definitions

In the next section each register is described in detail. The following conventions are used throughout this section:

- **set:** Indicates that the target bit was loaded with a 1.
- **clear:** Indicates that the target bit was loaded with a 0.
- **(0):** Indicates that the associated bit is set to 0 after a hard reset.
- **(1):** Indicates that the associated bit is set to 1 after a hard reset.
- **(x):** Indicates the state of the bit after a hard reset is undefined.

SCSI Sequence Control (SCSISEQ)

Register Type: **Read/Write**
Register Address: **340h**

This register controls the Selection/Reselection process for the AIC-6360. Each bit in this register enables a different portion of the Selection/Reselection process. This register can be read, allowing bit manipulation instructions without saving a register image in local scratch RAM. All bits except SCSIRSTO (bit 0) are cleared by a SCSI Reset.

SCSISEQ	R/W
7	TEMODEO
6	ENSELO
5	ENSELI
4	ENRSELI
3	ENAUTOATNO
2	ENAUTOATNI
1	ENAUTOATNP
0	SCSIRSTO

7 (0) TEMODEO **Target Enable Mode Out.** TEMODEO is used with ENSELO (bit 6). If TEMODEO is set, setting ENSELO initiates a Reselection Out sequence. If TEMODEO is cleared, setting ENSELO initiates a Selection Out sequence.

6 (0) ENSELO **Enable Selection Out.** When this bit is set it allows the SCSI logic to perform a Selection sequence (TEMODEO = 0) as an Initiator (ID = OID field of SCSIID Register) and select a Target (ID = TID field of the SCSIID Register), or to perform a Reselection sequence (TEMODEO = 1) as a Target (ID = OID field of SCSID Register) and reselect an Initiator (ID = TID field of the SCSIID Register). The SELINGO Status (bit 4, SSTAT0) is one when the SCSI logic has entered the Selection/ Reselection phase and is waiting for BSY back from the Target/Initiator. The processor must wait for SELDO status (bit 6, SSTAT0) to be one or SELTO (bit 7, SSTAT1) to be one if the hardware selection timeout is enabled (bit 2, SXFRCTL1 is set to one), or for the software selection timeout if the hardware timeout is not enabled. This control is set to zero by the AIC-6360, or by a hard reset.

5 (0) ENSELI **Enable Selection In.** When this bit is set to a one it allows the AIC-6360 to respond to a valid Selection sequence. When selected, the SELDI status (bit 5, SSTAT0) and the TARGET status (bit 7, SSTAT0) are set to one. The AIC-6360 only sets this control to zero when no more selections are wanted.

4	(0)	ENRESELI	**Enable Reselection In.** When this bit is set to one it allows the AIC-6360 to respond to a valid Reselection sequence. When reselected, the SELDI status (bit 5, SSTAT0) is one and the TARGET status (bit 7, SSTAT0) is set to zero. This control is reset to zero by writing a zero to this bit.
3	(0)	ENAUTOATNO	**Enable Auto Attention Out.** When this bit is set to one SCSI ATN is set when a Selection sequence (ENSELO=1, TEMODEO=0) is executed. This procedure is used when the AIC-6360 is the initiator and wants to follow the selection with a Message Out phase. The processor can clear ATN by setting CLRATNO (bit 6, 34Ch, W). A Bus Free state on the SCSI bus also clears ATN. Clearing ENAUTOATNO does not clear ATN.
2	(0)	ENAUTOATNI	**Enable Auto Attention In.** With ENAUTOATNI set, ATN is set during a Reselection In sequence (ENRESELI=1). This procedure is used when the AIC-6360 is the initiator and wants to follow reselection with a Message Out phase. The processor can clear ATN by setting CLRATNO (bit 6, 34Ch, W). A Bus Free state on the SCSI bus also clears ATN. Clearing this bit does not clear ATN.
1	(0)	ENAUTOATNP	**Enable Auto Attention Parity.** When both ENAUTOATNP and ENSPCHK (bit 5, 342h) are set, ATN is set if a parity error is detected on SC0–SC7 during the Data In, Message In, or Status In phases. The processor can clear ATN by setting CLRATNO (bit 6, 34Ch, W). A Bus Free state on the SCSI bus also clears ATN. Clearing this bit does not clear ATN.
0	(0)	SCSIRSTO	**SCSI Reset Out.** When SCSIRSTO is set, SCSI RST is set on the SCSI bus. The processor must clear RST by clearing SCSIRSTO. This control is not gated with the Target/Initiator mode.

SCSI Transfer Control 0 (SXFRCTL0)

Register Type: **Read/Write**
Register Address: **341h**

SCSI Transfer Control 0 enables transfers between the SCSI bus and the host, via the SCSI and host FIFOs. This register also controls the selection of SCSI PIO mode as the transfer mode and enables the SCSI FIFO and SCSI transfer counter to clear.

SXFRCTL0	R/W
7	SCSIEN
6	DMAEN
5	CHEN
4	CLRSTCNT
3	SPIOEN
2	Reserved (0)
1	CLRCH
0	Reserved (0)

7 (0) SCSIEN **Transfer Enable**. When SCSIEN is set, data can be transferred between the SCSI bus and the SCSI FIFO. Transfers are terminated by clearing SCSIEN. SCSIEN must be read back as a zero before the transfer is considered halted. Synchronous data transfers are enabled whenever SOFS (bits 3–0, 344h) is non-zero.

6 (0) DMAEN **FIFO Transfer Enable**. When DMAEN is set, transfers between the SCSI FIFO and host FIFO are enabled.

5 (0) CHEN **Channel Select**. This bit should *always* be set.

4 (0) CLRSTCNT **Clear SCSI Transfer Counter**. When CLRSTCNT is set, the SCSI transfer count (SCXFRCNT, 348h–34Ah) is set to 000000h. The AIC-6360 generates a clear pulse, making it necessary to reset CLRSTCNT. This bit is always read back as 0.

3 (0) SPIOEN **SCSI PIO Enable**. When SPIOEN is set, SCSI PIO mode is used as the transfer mode. Once a SCSI PIO transfer is started, SPIOEN must remain set *throughout the entire transfer*. If SPIOEN is cleared at *any* time during the transfer, the transfer will be *halted* without corrupting valid data in the data latch at 346h.

2 (0) RSVD **Reserved**. This bit always reads as 0.

1 (0) CLRCH **Clear Channel 1**. When CLRCH1 is set, the AIC-6360 generates a pulse to clear the SCSI FIFO, (bits 3–0 of 34Eh). This is used to initialize the channel for a transfer. To clear the SCSI Transfer Counter (348h–34Ah), use the CLRSTCNT bit in this register.

0 (0) RSVD **Reserved**. This bit always reads as 0.

SCSI Transfer Control 1 (SXFRCTL1)

Register Type: **Read/Write**
Register Address: **342h**

SCSI Transfer Control 1 enables various transfer controls associated with SCSI transfers. This register controls the Selection/Reselection timer, byte alignment, and parity checking.

SXFRCTL1	R/W
7	BITBUCKET
6	SWRAPEN
5	ENSPCHK
4	STIMESEL [1]
3	STIMESEL [0]
2	ENSTIMER
1	BYTEALIGN
0	Reserved (0)

7 (0) BITBUCKET **SCSI Bit Bucket Mode.** When BITBUCKET is set, it allows the AIC-6360 to read data from the SCSI bus and throw it away, or supply 00h write data. In BITBUCKET mode data is not saved, and FIFO full or FIFO empty conditions do not cause transfer halts. BITBUCKET is enabled in Initiator mode only.

6 (0) SWRAPEN **SCSI Wrap Enable.** When SWRAPEN is set, the transfer count (registers 348h – 34Ah) can wrap past 0. This allows the transfer count to exceed a 24-bit value. When a transfer count wrap occurrs, SWRAP (bit 3, 34Bh, R) is set. SWRAPEN is valid only in Target mode.

> Note
> If the transfer counter has wrapped, and it is not the final wrap for the current transfer, clear SWRAP by setting CLRSWRAP (bit 3, 34Bh) and wait for it to be set again (indicating another counter wrap). When the last wrap has occurred, clear SWRAP by setting CLRSWRAP (bit 3, 34Bh), and clear SWRAPEN. Wait for SDONE to be set, indicating the transfer is complete.

5 (0) ENSPCHK **Enable Parity Check.** When ENSPCHK is set, parity checking is enabled on the SCSI bus. When ENSPCHK is cleared, SCSIPERR (bit 2, 34Ch, R) always reads 0.

4,3 (0) STIMESEL [1,0] **Set Selection Timeout.** These two bits contain the selection timeout code, which are defined as follows:

STIMESEL Bit 4	Bit 3	Timeout
0	0	256 ms
0	1	128 ms
1	0	64 ms
1	1	32 ms

2	(0)	ENSTIMER	**Enable Selection Timer**. When ENSTIMER is set, the hardware selection timer is enabled. When the internal selection timer exceeds the timeout limit during a Selection Out or Reselection Out sequence, SEL is cleared and SELTO (bit 7, 34Ch, R) is set. If ENSELTIMO (bit 7, 351h, R) is cleared, SEL will continue to be set until cleared by the processor.
1	(0)	BYTEALIGN	**Byte Align**. When BYTEALIGN is set, it forces a handshake between the host FIFO and the SCSI FIFO. Any data passed for this handshake is discarded. This procedure is used to align data when an odd byte boundary disconnect occurs during a write operation.
0	(0)	RSVD	**Reserved**. This bit always reads as 0.

SCSI Signal (SCSISIG)

Register Type: **Read/Write**
Register Address: **343h**

The SCSISIG Read register reads the actual state of the signals on the SCSI bus pins. The SCSISIG Write register allows the processor to control the SCSI signals that are enabled on the bus according to the mode of operation (Target or Initiator). CD, IO, and MSG in SCSISIG Write are used for the phase comparison when in Initiator Mode. All control signals in this register are cleared by the Bus Free, SCSI Reset, or Hard Reset conditions.

SCSISIG W		SCSISIG R	
7	CDO/CDEXP	7	CDI
6	IOO/IOEXP	6	IOI
5	MSGO/MSGEXP	5	MSGI
4	ATNO	4	ATNI
3	SELO	3	SELI
2	BSYO	2	BSYI
1	REQO	1	REQI
0	ACKO	0	ACKI

SCSISIG Read

7 (x) CDI — **Command/Data In.** The CDI bit reflects the state of the CD signal on the SCSI bus.

6 (x) IOI — **Input/Output In.** The IOI bit reflects the state of the IO signal on the SCSI bus.

5 (x) MSGI — **Message In.** The MSGI bit reflects the state of the MSG signal on the SCSI bus.

4 (x) ATNI — **Attention In.** The ATNI bit reflects the state of the ATN signal on the SCSI bus.

3 (x) SELI — **Selection In.** The SELI bit reflects the state of the SEL signal on the SCSI bus.

2 (x) BSYI — **Busy In.** The BSYI bit reflects the state of the BSY signal on the SCSI bus.

1 (x) REQI — **Request In.** The REQI bit reflects the state of the REQ signal on the SCSI bus.

0 (x) ACKI — **Acknowledge In.** The ACKI bit reflects the state of the ACK signal on the SCSI bus.

SCSISIG Write

7	(0)	CDO	**Command/Data Out**. In Target mode, CDO drives C/D on the SCSI bus. In Initiator mode, CDO is the state of C/D expected for the next REQ pulse.
6	(0)	IOO	**Input/Output Out**. In Target mode, IOO drives I/O on the SCSI bus. In Initiator mode, IOO is the state of I/O expected for the next REQ pulse.
5	(0)	MSGO	**Message Out**. In Target mode, MSGO drives MGS on the SCSI bus. In Initiator mode, MSGO is the state of the MSG expected for the next REQ pulse.
4	(0)	ATNO	**Attention Out**. In Target mode, ATNO is not used. In Initiator mode, driving ATNO high sets ATN on the SCSI bus. ATN is cleared by driving CLRATNO (bit 6, 34Ch, W) high.
3	(0)	SELO	**Selection Out**. When SELO is set, the AIC-6360 sets SEL on the SCSI bus. This bit may be used to clear SEL on the SCSI bus.
2	(0)	BSYO	**Busy Out**. When BSYO is set, the AIC-6360 sets BSY on the SCSI bus. This bit may be used to clear BSY on the SCSI bus. BSYO is also set by the AIC-6360's SCSI logic during a Selection Out or Reselection Out sequence.
1	(0)	REQO	**Request Out**. When REQO is set, the AIC-6360 sets REQ on the SCSI bus. REQO is disabled In initiator mode.
0	(0)	ACKO	**Acknowledge Out**. When ACKO is set, ACK is asserted on the SCSI bus. ACKO is disabled in Target mode.

SCSI Rate Control (SCSIRATE)

Register Type: **Write Only**
Register Address: **344h**

The Rate Control register is used to control the timing and offset parameters for synchronous SCSI transfers. If SOFS is set to zero, SCSI transfers are asynchronous.

SCSIRATE	W
7	Reserved (0)
6	SXFR [2]
5	SXFR [1]
4	SXFR [0]
3	SOFS [3]
2	SOFS [2]
1	SOFS [1]
0	SOFS [0]

7 (0) RSVD **Reserved.**

6-4 (0) SXFR[2:0] **Synchronous SCSI Transfer Rate 2:0.** SXFR is the synchronous transfer rate code. The table below lists transfer rates and associated timing parameters for all valid transfer rate codes. Timing parameters are given for a 20 MHz clock. For clock rates other than 20 MHz, timing parameters are given in clock periods (T). Transfer rates at less than 2.22 MBytes/second must be made in asynchronous mode.

SXFR	REQ/ACK PW	PERIOD	RATE
000	50 ns (T)	100 ns (2T)	10.0 MB/s
001	50 ns (T)	150 ns (3T)	6.67 MB/s
010	100 ns (2T)	200 ns (4T)	5.00 MB/s
011	100 ns (2T)	250 ns (5T)	4.00 MB/s
100	100 ns (2T)	300 ns (6T)	3.33 MB/s
101	100 ns (2T)	350 ns (7T)	2.86 MB/s
110	100 ns (2T)	400 ns (8T)	2.50 MB/s
111	100 ns (2T)	450 ns (9T)	2.22 MB/s

3-0 (0) SOFS[3:0] **SCSI Offset.** SOFS contains the synchronous transfer offset. When SOFS is set to 0000h, the SCSI transfer mode is asynchronous. Any other value is the offset for a SCSI synchronous transfer. Valid ranges other than 0000 are 0001 through 1000. This field only applies to DATA phases on CH1. SOFS must be loaded with the values derived from the SCSI synchronous transfer request negotiations, since the Target could force a DATA phase even though a different phase may be expected.

SCSI ID (SCSIID)

Register Type: **Write Only**
Register Address: **345h**

This register contains the SCSI IDs of the AIC-6360 and the other unit (Target or Initiator) involved in the SCSI operation. Bits 6–4 always contain the AIC-6360's ID, and bits 2–0 always contain the other unit's ID. This is true regardless of which unit is the initiator and which is the target.

SCSIID W	
7	Reserved (0)
6	OID [2]
5	OID [1]
4	OID [0]
3	Reserved (0)
2	TID [2]
1	TID [1]
0	TID [0]

7	(0)	RSVD	**Reserved**
6-4	(x)	OID[2:0]	**Own ID**. This is your own device ID on the SCSI Bus during any type of Selection/Reselection sequence. It is your own Initiator ID during Selection Out (ENSELO=1, TEMODEO=0) and Reselection In (ENRSELI). It is your own Target ID during Selection In (ENSELI) and Reselection Out (ENSELO, TEMODEO=1).
3	(0)	RSVD	**Reserved**
2-0	(x)	TID[2:0]	**Other ID**. This is the other device ID on the SCSI bus during any Selection/Reselection sequence. It is the other Target ID during Selection Out (ENSELO=1, TEMODEO=0) and Reselection In (ENRSELI). It is the other Initiator ID during Selection In (ENSELI) and Reselection Out (ENSELO, TEMODEO=1).

Selection/Reselection ID (SELID)

Register Type: **Read Only**
Register Address: **345h**

When the AIC-6360 has been selected or reselected, the SCSI ID bits of the target *and* the initiator are set in this register.

SELID	R
7	SELID [7]
6	SELID [6]
5	SELID [5]
4	SELID [4]
3	SELID [3]
2	SELID [2]
1	SELID [1]
0	SELID [0]

7–0 (x) SELID — **Selection ID**. These bits directly correspond to the SCSI IDs.

SCSI Latched Data (SCSIDAT)

Register Type: **Read/Write**
Register Address: **346h**

This register is the data latch used for manual or SCSI PIO data transfers. Data outbound from the AIC-6360 is written to this register. Data inbound to the AIC-6360 is read from this register.

SCSIDAT	R/W
7	LSDB [7]
6	LSDB [6]
5	LSDB [5]
4	LSDB [4]
3	LSDB [3]
2	LSDB [2]
1	LSDB [1]
0	LSDB [0]

7–0 (x) DB 7–0 — **Data Bits 7–0**. DB 7–0 are loaded with SCSI data. DB 7 is the most significant bit (MSB).

SCSI Data Bus (SCSIBUS)

Register Type: **Read Only**
Register Address: **347h**

This register reflects the current state of the SCSI bus data lines. It is used during manual selection or reselection.

SCSIBUS	R
7	SDB [7]
6	SDB [6]
5	SDB [5]
4	SDB [4]
3	SDB [3]
2	SDB [2]
1	SDB [1]
0	SDB [0]

7–0 (x) SDB 7–0 **SCSI Data Bits 7–0.** SDB 7–0 are loaded with SCSI data. SDB 7 is the MSB, and SDB 0 is the LSB.

SCSI Transfer Count (STCNT*n*)

Register Type: **Read/Write**
Register Address: **348h-34Ah**

These registers contain the DMA byte transfer count on the SCSI interface. STCNT0 is the least significant byte, STCNT1 is the mid byte, and STCNT2 is the most significant byte.

In Target mode this register is loaded with the number of REQ's to send out on the SCSI bus. Loading 000000h will give a byte transfer count of 16777216 decimal (16M hex). It will count down on REQ's until it reaches 0, at which time SDONE status (bit 2, SSTAT0) is one (unless SWRAPEN has been set to a one). Each time it wraps to 0 the status SWRAP (bit 3, SSTAT0) is set to one. SWRAP should then be cleared via CLRSWRAP Control (bit 3, CLRSINT0) before the next wrap (that time is 16M times the SCSI bus transfer period). The host processor must keep track of the number of wraps.

In Initiator mode these registers must be set to zero by the processor each time transfer is enabled between SCSI and the DMA FIFO's (via CLRSTCNT, bit 4, SXFRCTL). The counters will then count up on ACK's. Optionally, the counters can be reloaded with the current byte count if there is a disconnect/reconnect midway in a transfer.

STCNT0 R/W		STCNT1 R/W		STCNT2 R/W	
7	STCNT [07]	7	STCNT [15]	7	STCNT [23]
6	STCNT [06]	6	STCNT [14]	6	STCNT [22]
5	STCNT [05]	5	STCNT [13]	5	STCNT [21]
4	STCNT [04]	4	STCNT [12]	4	STCNT [20]
3	STCNT [03]	3	STCNT [11]	3	STCNT [19]
2	STCNT [02]	2	STCNT [10]	2	STCNT [18]
1	STCNT [01]	1	STCNT [09]	1	STCNT [17]
0	STCNT [00]	0	STCNT [08]	0	STCNT [16]

23–16 (x) STCNT2 **Most Significant Byte.** STCNT2 contains the most significant 8 bits of the SCSI transfer count.

15–8 (x) STCNT1 **Middle Byte.** STCNT1 contains the middle 8 bits of the SCSI transfer count.

7–0 (x) STCNT0 **Least Significant Byte.** STCNT0 contains the least significant 8 bits of the SCSI transfer count.

Clear SCSI Interrupts 0 (CLRSINT0)

Register Type: **Write Only**
Register Address: **34Bh**

This register (except for bit 7) clears the interrupts associated with the status bits in SSTAT0 (34Bh). Setting any of these bits clears the corresponding interrupt and clears IRQ. IRQ may not be cleared if other interrupts are active. A clear bit does not need to be cleared before it can be set again. Writing a zero to any bit in this register has no effect.

Bit 7 of this register is used to generate the SDONE interrupt. Clearing an interrupt does not necessarily clear the status bit associated with the condition that caused the interrupt.

CLRSINT0	W
7	SETSDONE
6	CLRSELDO
5	CLRSELDI
4	CLRSELINGO
3	CLRSWRAP
2	CLRSDONE
1	CLRSPIORDY
0	CLRDMADONE

7 (1) SETSDONE **Set SCSI Transfer Done**. When SETSDONE is set, SDONE (bit 2, 34Bh, R) is set; and if ENSDONE is set, IRQ is set.

6 (1) CLRSELDO **Clear Selection Out Done**. When CLRSELDO is set, the SELDO interrupt is cleared.

5 (1) CLRSELDI **Clear Selection Done In**. When CLRSELDI is set, the SELDI interrupt is cleared.

4 (1) CLRSELINGO **Clear Selection**. When CLRSELINGO is set, the SELINGO interrupt is cleared.

3 (1) CLRSWRAP **Clear Wrap**. When CLRSWRAP is set, the SWRAP interrupt is cleared. Also clears SWRAP status bit (34Bh, bit 3).

2 (1) CLRSDONE **Clear SCSI Done**. When CLRSDONE is set, the SDONE interrupt is cleared. Also clears SDONE status bit (34Bh, bit 2).

1 (1) CLRSPIORDY **Clear SCSI PIO Ready**. When CLRSPIORDY is set, the SPIORDY interrupt is cleared.

0 (1) CLRDMADONE **Clear DMA Done**. When CLRDMADONE is set, the DMADONE interrupt is cleared.

SCSI Interrupt Status 0 (SSTAT0)

Register Type: **Read Only**
Register Address: **34Bh**

This register reflects the state of eight SCSI status bits. If the interrupts corresponding to these status bits are enabled, interrupts are generated when the status bits are set. Interrupts are enabled using the SIMODE0 register (350h) and are cleared using the CLRSINT0 register (34Bh). The status bits in this register are available regardless of the condition of the enable bits. Clearing an interrupt does not necessarily clear the status bit; the means by which a status bit may be cleared is specified for each bit. The clear bits also state specifically when they clear the associated status bit.

The TARGET bit is a status bit; no interrupt is generated when TARGET is set.

Refer to the discussion of interrupts in Chapter Three, *Functional Information*, for more information on the interrelation of status, interrupt, enable, and clear bits.

SSTAT0	R
7	TARGET
6	SELDO
5	SELDI
4	SELINGO
3	SWRAP
2	SDONE
1	SPIORDY
0	DMADONE

7 (0) TARGET **Target**. When TARGET is set, the AIC-6360 is the target. TARGET is only valid after a selection or reselection has completed and before Bus Free. This condition does not generate an interrupt.

6 (0) SELDO **Select Out Done**. SELDO is set when the AIC-6360 has successfully completed Selection Out or Reselection Out. The state of TARGET determines whether the sequence was Selection Out or Reselection Out. When TARGET is cleared (TARGET=0), SELDO indicates that a Selection Out sequence was completed. When TARGET is set (TARGET=1), SELDO indicates that a Reselection Out sequence was completed.

SELDO will remain a one for the duration of the command in process; it is cleared by Bus Free. This condition generates an interrupt if ENSELDO (bit 6, 350h) is set.

5	(0)	SELDI	**Selection In Done**. SELDI is set when the AIC-6360 has been selected or reselected. The state of TARGET determines whether the sequence was Selection In or Reselection In. When TARGET is set, SELDI indicates that a Selection In sequence was completed. When TARGET is cleared, SELDI indicates that a Reselection In sequence was completed. This condition generates an interrupt if ENSELDI (bit 5, 350h) is set. To enable clearing SELDI, CLRSELDI must first be set. A Bus Free condition will then clear SELDI. Note that CLRSELDI must be set to enable Bus Free to clear SELDI, whether or not ENSELDI has been set. This feature allows the initiator (target) to recognize that a Reselection (Selection) in sequence occurred, even if Bus Free occurred before it reads SELDI status.
4	(0)	SELINGO	**Selection Initiated Out**. SELINGO is set when the AIC-6360 begins a Selection Out or Reselection Out sequence. SELINGO is set upon successful arbitration of the bus, and remains set throughout the Selection Out or Reselection Out sequence. When the Selection Out or Reselection Out sequence has completed, SELINGO is *cleared* (i.e., self-clearing interrupt/status bit). This condition generates an interrupt if ENSELINGO (bit 4, 350h) is set.
3	(0)	SWRAP	**Transfer Counter Wrap**. SWRAP is set when the transfer counter (348h–34Ah) wraps past 0. In TARGET mode, SWRAPEN (bit 6, 342h) must be set in order for the counter to wrap. SWRAP is set when the transfer counter decrements from 000001h to 000000h. In Initiator mode, SWRAP is enabled at all times. SWRAP is set when the transfer counter increments from FFFFFFh to 000000h. SWRAP is cleared by setting CLRSWRAP (bit 3, 34Bh). This condition generates an interrupt if ENSWRAP (bit 3, 350h) is set.
2	(0)	SDONE	**SCSI Done**. SDONE is set when the transfer counter (348h–34Ah) has counted down to 000000h, unless SWRAPEN (bit 6 of 342h) is set, in which case a transfer counter wrap occurs and the transfer continues. SDONE can be set by setting SETSDONE (bit 7, 34Bh, W). SDONE is never set in Initiator mode, unless it was set prior to entering Initiator mode. SDONE is cleared by setting CLRSDONE (bit 2, 34Bh). To prevent false transfers, SCSIEN (bit 7, 34Ih) must be cleared before SDONE is cleared. This condition generates an interrupt if ENSDONE (bit 2, 350h) is set.

1	(0)	SPIORDY	**SCSI PIO Ready**. SPIORDY is set when the automatic SCSI PIO function has been enabled and data is ready or is needed by the SCSI data transfer logic. In Initiator mode, SPIORDY is set when REQ is asserted. In Target mode, SPIORDY is set when ACK is asserted. On outbound transfers, SPIORDY is cleared on a write to the SCSI data latch (346h). On inbound transfers, SPIORDY is cleared on a read from the SCSI data latch (346h). This condition generates an interrupt if ENSPIORDY (bit 1, 350h) is set.
0	(0)	DMADONE	**DMA Done**. DMADONE is only valid when ATDMA is used as the mode of data transfer. For transfers to the SCSI bus, DMADONE is set when both the SCSI FIFO and the host FIFO are empty, and terminal count (T/C) has been asserted by the host DMA controller. For transfers from the SCSI bus, DMADONE is set when terminal count (T/C) has been asserted by the host DMA controller. This condition generates an interrupt if ENDMADONE (bit 0, 350h) is set.

Clear SCSI Interrupts 1 (CLRSINT1)

Register Type: **Write Only**
Register Address: **34Ch**

This register clears the interrupts associated with the status bits in SSTAT1 (34Ch). Setting any of these bits (except bit 6) clears the corresponding interrupt and clears IRQ. IRQ may not be deasserted if other interrupts are active. A clear bit does not need to be cleared before it can be set again. Setting bit 6 clears ATN. Writing a zero to any bit in this register has no effect.

Clearing one of these interrupts *does* clear the status bit associated with the condition that caused the interrupt.

CLRSINT1 W	
7	CLRSELTIMO
6	CLRATNO
5	CLRSCSIRSTI
4	Reserved (0)
3	CLRBUSFREE
2	CLRSCSIPERR
1	CLRPHASECHG
0	CLRREQINIT

7 (1) CLRSELTIMO **Clear Selection Timeout**. When CLRSELTIMO is set, the SELTO interrupt and the SELTO status bit (bit 7, 34Ch, R) are cleared.

6 (1) CLRATNO **Clear Attention Out**. When CLRATNO is set, ATN is cleared.

5 (1) CLRSCSIRSTI **Clear SCSI Reset In**. When CLRSCSIRSTI is set, the SCSIRSTI interrupt and the SCSIRSTI status bit (bit 5, 34Ch, R) are cleared.

4 (0) RSVD **Reserved**. This bit should remain a 0.

3 (1) CLRBUSFREE **Clear Bus Free**. When CLRBUSFREE is set, the BUSFREE interrupt and the BUSFREE status bit (bit 3, 34Ch, R) are cleared.

2 (1) CLRSCSIPERR **Clear SCSI Parity Error**. When CLRSCSIPERR is set, the SCSIPERR interrupt and the SCSIPERR status bit (bit 2, 34Ch, R) are cleared.

1 (1) CLRPHASECHG **Clear Phase Change**. When CLRPHASECHG is set, the PHASECHG interrupt and the PHASECHG status bit (bit 1, 34Ch, R) are cleared.

0 (1) CLRREQINIT **Clear REQ Initiated**. When CLRREQINIT is set, the REQINIT interrupt and the REQINIT status bit (bit 0, 34Ch, R) are cleared.

SCSI Status 1 (SSTAT1)

Register Type: **Read Only**
Register Address: **34Ch**

This register reflects the state of eight SCSI status bits. If the interrupts corresponding to these status bits are enabled, interrupts are generated when the status bits are set. Interrupts are enabled using the SIMODE1 register (351h) and cleared using the CLRSINT1 register (34Ch). The status bits in this register are available regardless of the condition of the enable bits. All bits in this register are cleared by the corresponding bits in the CLRSINT1 register, except for ATNTARG and PHASEMIS.

Refer to the discussion of interrupts in Section 4 of this manual for more information on the interrelation of status, interrupt, enable, and clear bits.

SSTAT1 R	
7	SELTO
6	ATNTARG
5	SCSIRSTI
4	PHASEMIS
3	BUSFREE
2	SCSIPERR
1	PHASECHG
0	REQINIT

7 (0) SELTO — **Selection Timeout Expired.** SELTO is set when a Selection Out or Reselection Out timeout has occurred and ENSTIMER (bit 2, 342h)is set. SELTO is cleared by setting CLRSELTIMO (bit 7 of 34Ch). This condition generates an interrupt if ENSELTIMO (bit 7, 351h) is set.

6 (0) ATNTARG — **Target Attention.** ATNTARG is only valid in Target mode. ATNTARG is set when the initiator has set ATN. ATNTARG is cleared when the initiator clears ATN. This condition generates an interrupt if ENATNTARG (bit 6, 351h) is set.

5 (0) SCSIRSTI — **SCSI Reset In.** SCSIRSTI is set when a bus reset occurs on the SCSI bus. SCSIRSTI remains set until cleared by setting CLRSCSIRSTI (bit 5, 34ChW) high. This condition generates an interrupt if ENSCSIRST (bit 5, 351h) is set.

4 (0) PHASEMIS — **Phase Mismatch.** PHASEMIS is only valid in Initiator mode. PHASEMIS is set when the expected phase loaded in the SCSISIGI register (bits 7–5, 343h) does not match the phase active on the SCSI bus. PHASEMIS is *qualified* by REQINIT (bit 0 of this register). PHASEMIS is *cleared* when the phase active on the SCSI bus matches the expected phase loaded in the SCSISIGI register. This condition generates an interrupt if ENPHASEMIS (bit 4, 351h) is set.

3	(0)	BUSFREE	**Bus Free**. BUSFREE is set when both BSY and SEL have been negated for 400 nsec (8T). BUSFREE is cleared by setting CLRBUSFREE (bit 3, 34Ch). This condition generates an interrupt if ENBUSFREE (bit 3, 351h) is set.
2	(0)	SCSIPERR	**Parity Error**. SCSIPERR is set when a parity error is detected during an inbound Information Transfer phase and ENSPCHK is set. If ENSPCHK (bit 5, 342h) is cleared, SCSIPERR is always 0. In Target mode, parity is sampled on the leading edge of ACK. In Initiator mode, parity is sampled on the leading edge of REQ. SCSIPERR is cleared by setting CLRSCSIPERR (bit 2, 34Ch, W). After driving CLRSCSIPERR high, SCSIPERR reflects the parity of the last byte transferred on the bus. This condition generates an interrupt if ENSCSIPERR (bit 2, 351h) is set.
1	(0)	PHASECHG	**Phase Change**. PHASECHG is only valid in Initiator mode. PHASECHG is set when the expected phase loaded in the SCSI Signal In register (bits 7–5, 343h) does not match the phase active on the SCSI bus. PHASECHG is cleared by setting CLRPHASECHG (bit 2, 34Ch, W). This condition generates an interrupt if ENPHASECHG (bit 1, 351h) is set.
0	(0)	REQINIT	**REQ Initiated**. REQINIT is only valid in Initiator mode. REQINIT is set when the AIC-6360 detects the leading edge of REQ. REQINIT is cleared when ACK is set on the bus, or when CLRREQINIT (bit 0, 34Ch, W) is set. This condition generates an interrupt if ENREQINIT (bit 0, 351h) is set.

SCSI Status 2 (SSTAT2)

Register Type: **Read Only**
Register Address: **34Dh**

This register reflects the status of the SCSI CH1 FIFO.

SSTAT2 R	
7	Reserved (0)
6	Reserved (0)
5	SOFFSET
4	SEMPTY
3	SFULL
2	SFCNT [2]
1	SFCNT [1]
0	SFCNT [0]

7	(0)	RSVD	**Reserved.**
6	(0)	RSVD	**Reserved.** This bit always reads as 0.
5	(0)	SOFFSET	**SCSI Offset.** If SOFFSET is set, it indicates that the REQ/ACK offset for a synchronous SCSI transfer is non-zero. When SOFFSET is cleared, it indicates that the REQ/ACK offset is zero (meaning the full transfer count has been sent or received).
4	(1)	SEMPTY	**SCSI FIFO Empty.** If SEMPTY is set, it indicates that the SCSI FIFO is empty.
3	(0)	SFULL	**SCSI FIFO Full.** If SFULL is set, it indicates that the SCSI FIFO is full.
2–0	(0)	SFCNT [2:0]	**SCSI FIFO Count.** SFCNT is loaded with a count of the number of bytes in the SCSI FIFO. If SFCNT is 000h, the SCSI FIFO Full or SCSI FIFO Empty bits determine whether the SCSI FIFO is full or empty.

SCSI Test Control (SCSITEST)

Register Type: **Write Only**
Register Address: **34Eh**

This register is used to initiate test modes in the internal AIC-6360 SCSI logic.

> **CAUTION**
> Do not write to this register during normal operation. Clear this register before programming the AIC-6360.

SCSITEST W	
7	Reserved (0)
6	Reserved (0)
5	Reserved (0)
4	Reserved (0)
3	SCTESTU
2	SCTESTD
1	Reserved (0)
0	STCTEST

7–4 (0) RSVD **Reserved.**

3 (0) SCTESTU **SCSI Transfer Count Up.** When SCTESTU is set, the SCSI Transfer Counter counts up at the input clock rate.

2 (0) SCTESTD **SCSI Transfer Count Down.** When SCTESTD is set, the SCSI Transfer Counter counts down at the input clock rate.

1 (0) RSVD **Reserved.**

0 (0) STCTEST **SCSI Transfer Count Test.** When STCTEST is set, a stage-to-stage carry true is forced in both the transfer and select abort counters, which causes both counters to run at the clock rate. During the transfer count test, the counter contents can be monitored by reading the desired stage. If STCTEST and ENSTIMER (bit 2, 342h) are both high, then the SCSI Transfer Count Read register (bits 5–0, 348h) is reassigned to the Select Abort Counter in the following manner:

BIT	ASSIGNMENT
5	Stage 6 (/2, output)
4	Stage 5 (/2, output)
3	Stage 4 (/2, output)
2	Stage 3 (/10, carry out)
1	Stage 2 (/256, carry out)
0	Stage 1 (/256, carry out)

SCSI Status 3 (SSTAT3)

Register Type: **Read Only**
Register Address: **34Eh**

This register contains information on the status of the current synchronous SCSI transfer.

> **CAUTION**
> Do not read this register unless all transfers are stopped.

SSTAT3 R	
7	SCSICNT [3]
6	SCSICNT [2]
5	SCSICNT [1]
4	SCSICNT [0]
3	OFFCNT [3]
2	OFFCNT [2]
1	OFFCNT [1]
0	OFFCNT [0]

7-4 (0) SCSICNT[3:0] **Count Difference.** Contains the difference between what the offset count says is in the SCSI FIFO1 and what the FCNT says is in the SCSI FIFO1. Used by hardware to prevent SCSI FIFO1 overrun.

3-0 (0) OFFCNT[3:0] **Offset Count.** Contains the current value of the SCSI offset counter. This is a count of the number of REQs received for which no ACKs have been issued.

Clear SCSI Errors (CLRSERR)

Register Type: **Write Only**
Register Address: **34Fh**

This register clears the error condition status bits in SSTAT4 (34Fh). Setting any of these bits clears the corresponding status bit. A clear bit does not need to be cleared before it can be set again. Writing a zero to any bit in this register has no effect.

CLRSERR	W
7	Reserved (0)
6	Reserved (0)
5	Reserved (0)
4	Reserved (0)
3	Reserved (0)
2	CLRSYNCERR
1	CLRFWERR
0	CLRFRERR

7–3	(0)	RSVD	**Reserved.**
2	(0)	CLRSYNCERR	**Clear Synchronous Transfer Error.** When CLRSYNCERR is set, the SYNCERR status bit is cleared (bit 2, 34Fh, R).
1	(0)	CLRFWERR	**Clear FIFO Write Error.** When CLRFWERR is set, the FWERR status bit is cleared (bit 1, 34Fh, R).
0	(0)	CLRFRERR	**Clear FIFO Read Error.** When CLRFRERR is set, the FRERR status bit is cleared (bit 0, 34Fh, R).

SCSI Status 4 (SSTAT4)

Register Type: **Read Only**
Register Address: **34Fh**

This is a read of the possible error conditions during a SCSI transfer.

SSTAT4 R	
7	Reserved (0)
6	Reserved (0)
5	Reserved (0)
4	Reserved (0)
3	Reserved (0)
2	SYNCERR
1	FWERR
0	FRERR

7–3 (0) RSVD **Reserved**. This field always reads as 0000h.

2 (0) SYNCERR **Synchronous Transfer Error**. SYNCHERR is set for one of the following two conditions:

- At the beginning of an inbound synchronous transfer, when the SCSI FIFO is not empty prior to the transfer of the first byte off the SCSI bus. This condition may cause the SCSI FIFO to overflow, as SCSICNT (bits 7-4, 34Eh, R) is not correct.
- At the beginning of a synchronous transfer, when SOFFSET (bit 5, 34Dh) is set. This condition indicates that the previous transfer did not complete successfully.

1 (0) FWERR **FIFO Write Error**. FWERR is set when more than one source is enabled to write to the SCSI FIFO. This error can occur if the transfer path is set up to send data from the host FIFO through the SCSI FIFO onto the SCSI bus, with the AIC-6360 reselected as an initiator and the target driving I/O such that data is enabled SCSI bus-to-SCSI FIFO (Data In phase).

0 (0) FRERR **FIFO Read Error**. The FRERR bit is set when more than one source is enabled to read from the SCSI FIFO.

SCSI Interrupt Mode 0 (SIMODE0)

Register Type: **Read/Write**
Register Address: **350h**

This register enables the interrupts associated with the status bits in SSTAT0 (34Bh). Setting any of these bits enables the corresponding interrupt. If an event occurs that causes a status bit to be set, and the enable bit for that condition is set, IRQ is asserted.

Clearing an enable bit causes the interrupt associated with the condition to be masked. However, the status bit associated with the condition is still set, regardless of the state of the enable bits.

SIMODE0	R/W
7	Reserved (0)
6	ENSELDO
5	ENSELDI
4	ENSELINGO
3	ENSWRAP
2	ENSDONE
1	ENSPIORDY
0	ENDMADONE

7 (0) RSVD **Reserved**. This bit always reads as 0.

6 (0) ENSELDO **Enable Selection Done Out Interrupt**. If ENSELDO is set, the SELDO interrupt is generated when SELDO (bit 6, 34Bh, R) is set.

5 (0) ENSELDI **Enable Selection Done In Interrupt**. If ENSELDI is set, the SELDI interrupt is generated when SELDI (bit 5, 34Bh, R) is set.

4 (0) ENSELINGO **Enable Selection Initiated Out Interrupt**. If ENSELINGO is set, the SELINGO interrupt is generated when SELINGO (bit 4, 34Bh, R) is set.

3 (0) ENSWRAP **Enable Wrap Interrupt**. If ENSWRAP is set, the SWRAP interrupt is generated when SWRAP (bit 3, 34Bh, R) is set.

2 (0) ENSDONE **Enable SCSI Done Interrupt**. If ENSDONE is set, the SDONE interrupt is generated when SDONE (bit 2, 34Bh, R) is set.

1 (0) ENSPIORDY **Enable SCSI PIO Ready Interrupt**. If ENSPIORDY is set, the SPIORDY interrupt is generated when SPIORDY (bit 1, 34Bh, R) is set.

0 (0) ENDMADONE **Enable DMA Done Interrupt**. If ENDMADONE is set, the DMADONE interrupt is generated when DMADONE (bit 0, 34Bh, R) is set.

SCSI Interrupt Mode 1 (SIMODE1)

Register Type: **Read/Write**
Register Address: **351h**

This register enables the interrupts associated with the status bits in SSTAT1 (34Ch). Setting any of these bits enables the corresponding interrupt. If an event causes a status bit to be set, and the enable bit for that condition is set, IRQ is asserted.

Clearing an enable bit causes the interrupt associated with the condition to be masked. However, the status bit associated with the condition is still set, regardless of the state of the enable bits.

SIMODE1	R/W
7	ENSELTIMO
6	ENATNTARG
5	ENSCSIRST
4	ENPHASEMIS
3	ENBUSFREE
2	ENSCSIPERR
1	ENPHASECHG
0	ENREQINIT

7 (0) ENSELTIMO **Enable Selection Timeout Interrupt.** If ENSELTIMO is set, the SELTO interrupt is generated when SELTO (bit 7, 34Ch, R) is set.

6 (0) ENATNTARG **Enable Target Attention Interrupt.** If ENATNTARG is set, the ATNTARG interrupt is generated when ATNTARG (bit 6, 34Ch, R) is set.

5 (0) ENSCSIRST **Enable SCSI Reset Interrupt.** If ENSCSIRST is set, the SCSIRSTI interrupt is generated when SCSIRSTI (bit 5, 34Ch, R) is set.

4 (0) ENPHASEMIS **Enable Phase Mismatch Interrupt.** If ENPHASEMIS is set, the PHASEMIS interrupt is generated when PHASEMIS (bit 4, 34Ch, R) is set.

3 (0) ENBUSFREE **Enable Bus Free Interrupt.** If ENBUSFREE is set, the BUSFREE interrupt is generated when BUSFREE (bit 3, 34Ch, R) is set.

2 (0) ENSCSIPERR **Enable SCSI Parity Error Interrupt.** If ENSCSIPERR is set, the SCSIPERR interrupt is generated when SCSIPERR (bit 2, 34Ch, R) is set.

1 (0) ENPHASECHG **Enable Phase Change Interrupt.** If ENPHASECHG is set, the PHASECHG interrupt is generated when PHASECHG (bit 1, 34Ch, R) is set.

0 (0) ENREQINIT **Enable REQ Initiated Interrupt.** When ENREQINIT is set, the REQINIT interrupt is generated when REQINIT (bit 0, 34Ch, R) is set.

DMA Control 0 (DMACNTRL0)

Register Type: **Read/Write**
Register Address: **352h**

This register contains the basic controls for PIO and DMA transfer modes. The bits which enable a mode may be set at the same time as the bits configuring the mode.

DMACNTRL0	R/W
7	ENDMA
6	8BIT/-16BIT
5	DMA/-PIO
4	DWORDPIO
3	WRITE/-READ
2	INTEN
1	RSTFIFO
0	SWINT

7 (0) ENDMA **Enable DMA.** When ENDMA is set, data transfer between host main memory and the host FIFO in either PIO or DMA mode is enabled. Clearing ENDMA also clears ATDONE (bit 7, 354h).

6 (0) 8BIT/–16BIT **8-Bit/–16-Bit Mode.** When this bit is set, transfers between host main memory and the host FIFO are 8 bits wide and use SD0–SD7. When this bit is cleared, transfers between host main memory and the host FIFO are 16 bits wide and utilize SD0–SD15.

5 (0) DMA/–PIO **DMA/–PIO Mode.** When this bit is set, transfers between host main memory and the host FIFO are in DMA mode. When this bit is cleared, transfers between host main memory and the host FIFO are in PIO mode.

> Note
> When changing from PIO to DMA with ENDMA = 1, any direction change must be done first (bit 3 below.)

4 (0) DWORDPIO **Double Word PIO.** When this bit is set, 32-bit data port emulation on PIO data transfers is enabled. When this bit is cleared, the normal 16-bit data port is used. When it is enabled, transfers to or from addresses 356h and 358h both access the data port. Bit 6 (8BIT/-16BIT) should always be reset when this option is used.

3 (0) WRITE/–READ **Transfer Direction.** When this bit is set, data is transferred from host main memory to the host FIFO. When this bit is cleared, data is transferred from the host FIFO to host main memory.

2	(0)	INTEN	**Master Interrupt Enable**. INTEN controls the assertion of the IRQ pin. If INTEN is set, interrupts function normally. If INTEN is cleared, all interrupts are masked.
1	(0)	RSTFIFO	**Reset FIFO Counter**. When this bit is set, the FIFO counter (bits 7–0, 355h) is cleared. RSTFIFO is a self-clearing bit.
0	(0)	SWINT	**Software Interrupt**. If INTEN is set, setting SWINT asserts IRQ. This bit provides for software-generated interrupts.

DMA Control 1 (DMACNTRL1)

Register Type: **Read/Write**
Register Address: **353h**

This register is used to set the power-down feature and write the stack offset pointer.

DMACNTRL1	R/W
7	PWRDWN
6	ENSTK32
5	Reserved (0)
4	STK [4]
3	STK [3]
2	STK [2]
1	STK [1]
0	STK [0]

7 (0) PWRDWN **Power Down.** When PWRDWN is set, the internal clock is stopped to conserve power. Once the clock is stopped, the AIC-6360 is not operational.

6 (0) ENSTK32 **Enable Stack 32 Bytes.** When set, this bit allows access to the upper 16 bytes of the 32-byte stack area. When cleared, only the lower 16 bytes of the stack may be accessed as in the AIC-6260.

5 (0) RSVD **Reserved.**

4 (0) STK[4] **Stack Offset Pointer.** This bit is write-only and is ignored if ENSTK32 is not set.

3–0 (0) STK **Stack Offset Pointer.** STK contains the stack offset pointer. This field is write-only.

DMA Status (DMASTAT)

Register Type: **Read Only**
Register Address: **354h**

This register reflects the real-time status of the current DMA or PIO transfer.

DMASTAT R	
7	ATDONE
6	WORDRDY
5	INTSTAT
4	DFIFOFULL
3	DFIFOEMP
2	DFIFOHF
1	DWORDRDY
0	Reserved (0)

7	(0)	ATDONE	**Host Done**. ATDONE is used in DMA mode only. This bit is set when the host DMA controller has transferred the last byte or word and asserted T/C. While ATDONE is set, the internal host DMA logic is disabled; the host DMA logic remains disabled until this bit is cleared. ATDONE is cleared when ENDMA (bit 7, 352h) is cleared. ATDONE does not generate an interrupt.
6	(0)	WORDRDY	**Word Ready**. WORDRDY is used in PIO mode only. When WORDRDY is set, a 16-bit word is ready for transfer to or from the host FIFO. If the transfer count for a particular transfer does not equal or end on a 128-byte boundary, the host must transfer data into or out of the host FIFO one word at a time; this bit is used to control that process.
5	(0)	INTSTAT	**Interrupt Status**. INTSTAT is the OR of all enabled interrupts. INTSTAT may be read at any time, whether or not interrupts have been enabled via INTEN. This provides a means to poll for interrupts.
4	(0)	DFIFOFULL	**Host FIFO Full**. DFIFOFULL is set when the host FIFO contains 128 bytes that are ready to be read by the host. DFIFOFULL is used during SCSI-to-host PIO transfers.
3	(1)	DFIFOEMP	**Host FIFO Empty**. DFIFOEMP is set when the host FIFO is empty. DFIFOEMP is used during host-to-SCSI PIO transfers.
2	(0)	DFIFOHF	**Host FIFO Half Full**. This bit indicates that the DMA FIFO is at least half full (contains at least 64 bytes).
1	(0)	DWORDRDY	**Double Word Ready**. When set, this bit indicates that two words of data are available or are needed by the DMA FIFO. This bit is used in 32-bit PIO transfer mode and is only valid when DWORDPIO in DMACTRL0 is set.
0	(0)	RSVD	**Reserved.**

FIFO Status (FIFOSTAT)

Register Type: **Read Only**
Register Address: **355h**

This register indicates how many bytes are left in the DMA FIFO. They are used at the end of a transfer when using PIO. The host FIFO is 128 bytes deep. FIFOSTAT can only only be reliably read when all data transfer activity has stopped, such as when a SCSI phase change has occurred.

FIFOSTAT	R
7	FCNT [7]
6	FCNT [6]
5	FCNT [5]
4	FCNT [4]
3	FCNT [3]
2	FCNT [2]
1	FCNT [1]
0	FCNT [0]

7–0 (0) FCNT **FIFO Count.** FCNT contains a count of the bytes in the host FIFO.

DMA Data (DMADATA)

Register Type: **Read/Write**
Register Address: **356h**

This is the port where data transfer takes place for DMA or PIO operations. For DMA operations, it is 16 bits wide if 8BIT/-16BIT in DMACNTRL0 is set to zero and 8 bits if it is set to one. During 8-bit transfers the data is present on the low order bits only.

> Note
> When the DWORDPIO bit is set in the DMACNTRL0 register, accesses to registers 358h and 35Ah are mapped to register 356h. This allows the use of double word host accesses to address 358h. Alternately, when DWORDPIO and ENDMA are both set in the DMACTRL0 register, this register and address 35Ah are mapped to the data port (356h). This allows double-word PIO transfers to be used by the host.

During PIO operations data is written or read using the REP INS or REP OUTS instructions to this port. The data transfer width is determined by the state of the SBHE* signal on the AT bus. In DMA mode the state of 8BIT/-16BIT in DMACNTRL0 determines whether this is an 8-bit or 16-bit transfer.

DWORDPIO = 0 or ENDMA = 0

DMADATA	R/W	DMADATA	R/W
7	DATL [07]	15	DATH [15]
6	DATL [06]	14	DATH [14]
5	DATL [05]	13	DATH [13]
4	DATL [04]	12	DATH [12]
3	DATL [03]	11	DATH [11]
2	DATL [02]	10	DATH [10]
1	DATL [01]	09	DATH [09]
0	DATL [00]	08	DATH [08]

15-8 (0) DATH **High-Order Data Byte.**

7-0 (0) DATL **Low-Order Data Byte.**

DWORDPIO = 1 and ENDMA = 1

DMADATA*	R/W	DMADATA*	R/W
7	DATL [7]	15	DATH [15]
6	DATL [6]	14	DATH [14]
5	DATL [5]	13	DATH [13]
4	DATL [4]	12	DATH [12]
3	DATL [3]	11	DATH [11]
2	DATL [2]	10	DATH [10]
1	DATL [1]	09	DATH [9]
0	DATL [0]	08	DATH [8]

15-8 (0) DATH **High-Order Data Byte.**

7-0 (0) DATL **Low-Order Data Byte.**

Burst Control (BRSTCNTRL)

Register Type: **Read/Write**
Register Address: **358h**

Normally, these bits control the burst-on and burst-off time during DMA transfers. Both may be set from 1 to 15 microseconds. Loading zero in the Burst-on and Burst-off timer will disable the timer. The AIC-6360 will stay on the bus as long as there is data to transfer.

BRSTCNTRL	W
7	BON [3]
6	BON [2]
5	BON [1]
4	BON [0]
3	BOFF [3]
2	BOFF [2]
1	BOFF [1]
0	BOFF [0]

7–4 (x) BON — **Burst On**. BON contains the maximum value, in microseconds, of the transmission (burst) period. The AIC-6360 bursts data for the duration of BON, or until all data has been sent, whichever is less. BON may range from 0 (none) to 15 microseconds.

3–0 (x) BOFF — **Burst Off**. BOFF contains the minimum value, in microseconds, of the off-line (down) period. The AIC-6360 will not request DMA service for at least the duration of BOFF. BOFF may range from 0 (none) to 15 microseconds.

Port A (PORTA)

Register Type: **Read/Write**
Register Address: **35Ah**

This register provides an external 8-bit or 16-bit Read/Write port which may be accessed at any time. Port A is user-defined.

	PORT A R/W
7	PADAT [7]
6	PADAT [6]
5	PADAT [5]
4	PADAT [4]
3	PADAT [3]
2	PADAT [2]
1	PADAT [1]
0	PADAT [0]

7–0 (x) PADAT **Port A Data.**

Port B (PORTB)

Register Type: **Read/Write**
Register Address: **35Bh**

This register provides an external 8-bit or 16-bit R/W port which may be accessed at any time. Port B is user-defined.

	PORT B R/W
7	PBDAT [7]
6	PBDAT [6]
5	PBDAT [5]
4	PBDAT [4]
3	PBDAT [3]
2	PBDAT [2]
1	PBDAT [1]
0	PBDAT [0]

Revision (REV)

Register Type: **Read Only**
Register Address: **35Ch**

This port gives the revision of the chip. Bits 2-0 are valid. The revision code for the AIC-6360 is 001.

	REV R
7	Reserved (0)
6	Reserved (0)
5	Reserved (0)
4	Reserved (0)
3	Reserved (0)
2	(0)
1	(0)
0	(1)

Stack (STACK)

Register Type: **Read/Write**
Register Address: **35Dh**

This port is an 8-bit wide by 32-byte stack for general purpose memory use. The stack port may be addressed by writing to the lower 4 bits of DMACNTRL1 (353h). The offset points to the first location in the stack to be read from or written to. This allows the software to directly access any byte in the stack. Successive reads or writes access the next higher location in the stack.

For compatibility with the AIC-6260, the upper half of the stack is only available when the ENSTK32 bit in DMACTRL1 is set. When this bit is not set, only 16 bytes of the stack are available.

	STACK R/W
7	STKDAT [7]
6	STKDAT [6]
5	STKDAT [5]
4	STKDAT [4]
3	STKDAT [3]
2	STKDAT [2]
1	STKDAT [1]
0	STKDAT [0]

Test Register (TEST)

Register Type: **Write Only**
Register Address: **35Eh**

> **CAUTION**
> This register, which is described here for completeness, is used for test purposes only. Its value defaults to 00h, and this value *should not* be disturbed during normal operation.

During testing, either SCSIBLK or DMABLK should be set, but not both. If desired, one of the bits 2-6 may be set for specific tests. Clear this register before programming the AIC-6360.

	TEST W
7	RSVD
6	BOFFTMR
5	BONTMR
4	STCNTH
3	STCNTM
2	STCNTL
1	SCSIBLK
0	DMABLK

7 (0) RSVD **Reserved.**

6 (0) BOFFTMR **Buffer Off Timer.** When BOFFTMR is set with either SCSIBLK or DMABLK set, the BOFFTMR [7:0] to SCD [7:0] test path is enabled.

5 (0) BONTMR **Buffer On Timer.** When BONTMR is set with either SCSIBLK or DMABLK set, the BONTMR [7:0] to SCD [7:0] test path is enabled.

4 (0) STCNTH **SCSI Transfer High Count.** When STCNTH is set with either SCSIBLK or DMABLK set, the SCSI transfer counter [23:16] to SD [15:8] test path is enabled.

3 (0) STCNTM **SCSI Transfer Mid Count.** When STCNTM is set with either SCSIBLK or DMABLK set, the SCSI transfer counter [15:8] to SD [15:8] test path is enabled.

2 (0) STCNTL **SCSI Transfer Low Count.** When STCNTL is set with either SCSIBLK or DMABLK set, the SCSI transfer counter [7:0] to SD [15:8] test path is enabled.

1 (0) SCSIBLK **SCSI Block.** When SCSIBLK is set, the internal AIC-6360 SCSI logic is configured for testing. Table 4-3 lists pin redefinitions.

0 (0) DMABLK **DMA Block.** When DMABLK is set, the DMA logic is configured for testing. Table 4-3 lists pin redefinitions.

Table 4-3. Test Mode Pin Definition

	AT Pins	Type	Test Pins	Module
SCSIBLK=1	SA[9:0]	INPUT	—	
	AEN	INPUT	WRITE1	INPUT-SCSI
	ALTERNATE*	INPUT	DACK1	INPUT-SCSI
	SD[15:8]	BIDI		DW/DR[7:0]
	SD[7:0]	BIDI	—	
	DACK*	INPUT	—	
	IOR*	INPUT	—	
	IOW*	INPUT	—	
	T/C	INPUT	HOSTDONE	INPUT-SCSI
	SBHE*	INPUT	DMAEMPTY	INPUT-SCSI
	RESET	INPUT	—	
	X1	INPUT	—	
	DRQ	OUTPUT	—	
	IRQ	OUTPUT	—	
	PORTA	OUTPUT	SFAVAIL	OUTPUT-SCSI
	PORTB	OUTPUT	DMAEN	OUTPUT-SCSI
	PORTC	OUTPUT	—	
	X2	OUTPUT	—	
	F1	OUTPUT	—	

	SCSI Pins	Type	Test Pins	Module
DMABLK=1	SCD[7:0]*	BIDI	DW/DR[7:0]	INPUT/OUTPUT DMA
	SCDP*	BIDI	WRITE1	OUTPUT-DMA
	RST*	BIDI	DACK1	OUTPUT-DMA
	ATN*	BIDI	DMAEMPTY	OUTPUT-DMA
	BSY*	BIDI	INTL	INPUT-DMA
	SEL*	BIDI	DMAEN	INPUT-DMA
	C/D*	BIDI	SFAVAIL	INPUT-DMA
	I/O*[1]	BIDI	ENABLE	INPUT-DMA
	MSG*[2]	BIDI	ENABLE	INPUT-DMA
	REQ*	BIDI	RTNTSTL[3]	INPUT-DMA
	ACK*	BIDI	—	

[1] In addition to setting bit 0, IO must be set high to enable DW1[7:0] on SCD[7:0]. The enable is only used when transferring data from host to SCSI.

[2] MSG is used to enable WRITE1,DACK1,DMAEMPTY.

[3] RTNTSTL is the retention test input for the 32-byte stack and the 128-byte FIFO RAM cells.

ID Register (ID)

Register Type: **Read Only**
Register Address: **35Fh**

This register is used for identification purposes. Successive reads of this register return a 32-byte ASCII string of (C)1991ADAPTECAIC6360 followed by a pad of spaces (20h). In ASCII this produces the following hexadecimal string:

28, 43, 29, 31, 39, 39, 31, 41
44, 41, 50, 54, 45, 43, 41, 49
43, 36, 33, 36, 30, 20, 20, 20
20, 20, 20, 20, 20, 20, 20, 20

Bit 7 is the most significant bit of the ASCII character, and bit 0 is the least significant bit.

	ID R
7	ID [7]
6	ID [6]
5	ID [5]
4	ID [4]
3	ID [3]
2	ID [2]
1	ID [1]
0	ID [0]

❒

5

Application Notes

This chapter provides basic information on using the AIC-6360. It includes instructions for running data transfers and concludes with a simple application drawing.

Selection/Reselection Sequences

The AIC-6360 can perform Selection/Reselection In or Out sequences automatically. The following sections describe the tasks you must perform to run automatic Selection/Reselection In or Out sequences.

Selection Out Sequence

➤ 1 Load the SCSIID (345h) and SCSIRATE (344h) registers.

2 Set the expected phase in the SCSISIGO (bits 7–5, 343h) register. All other controls must be cleared.

3 Load the SXFRCTL1 register (342h) with the desired values.

4 Set CLRCH1 in the SXFRCTL0 register (bit 1, 341h); this clears the transfer counter and channel one. CH1/CH2 (bit 5, 341h) should always be set.

5 Turn off CLRCH1.

> Note
> If the transfer mode is SCSI PIO, it is not necessary to clear channel one. However, you should do it anyway, as the target might respond with an unexpected phase, such as Data In Synchronous when you are expecting Message Out.

6 Reset TEMODEO to zero and set ENSELO in the SCSISEQ register (bits 7 and 6, 340h); this enables the Selection Out sequence.

> Note
> If you are using either the Auto-Attention Out or the Auto-Attention Parity options, you should set ENAUTOATNO and/or ENAUTOATNP (bits 3 and 1, 340h). If you are using the Auto-Attention Out option, the expected phase set in the SCSISIGO register (bits 7–5, 343h) in Step 2 should be Message Out; the target determines whether this phase is supported.

7 Set ENSELDO, ENSELDI, or ENSELINGO in the SIMODE0 register (bit 6, 5, or 4, 350h). ENSELINGO may be used together with ENSELDO or ENSELDI.

8 Turn off ENSELO (bit 6, 340h).

9 Wait for SELINGO or SELDO to be set in the SSTAT0 register (bits 4 or 6, 34Bh), or for SELTO to be set in the SSTAT1 register (bit 7, 34Ch).

> Note
> If the hardware selection timer is disabled and SELINGO is set, start a timer and wait for the timer to expire, or for SELDO to be set in the SSTAT0 register (bit 6). TARGET (bit 7, 34Bh) should be cleared.

10 When SELDO is set in the SSTAT0 register (bit 6, 34Bh), the target has been selected and you may initiate an information transfer phase. This may be done in SCSI PIO, AT PIO or AT DMA.

11 In order to detect a passing Bus Free condition during selection, follow this sequence:

a Clear the BUSFREE interrupt at the CLRSINT1 register (bit 3, 34Ch).

b Clear ENSELO in the SCSISEQ register (bit 6, 340h).

c Clear ENSELTIMEO in the SIMODE1 register (bit 7, 351h).

d Mask the SELDO interrupt by clearing ENSELDO in the SIMODE0 register (bit 6, 350h).

e Look at the status of SELDO (34Bh, bit 6 set). If it is still active, a Bus Free condition has not occurred since selection.

Selection In Sequence

➤ 1 Load the OID field in the SCSIID register (bits 6–4, 345h).

2 Set ENSELI in the SCSISEQ register (bit 5, 340h); this enables the Selection In sequence.

> Note
> You may also set ENATNTARG in the SIMODE1 register (bit 6, 351h) to generate an interrupt if the initiator asserts ATN.

3 Wait for SELDI and TARGET to be set in the SSTAT0 register (bits 5 and 7, 34Bh).

> Note
> If TARGET is set, you have been reselected by a target.

4 Check the SELID register (345h) for the SCSI ID of the initiator.

5 Load the appropriate information in the SCSIRATE register (344h).

6 When SELDI and TARGET are set in the SSTAT0 register (bits 5 and 7, 34Bh), you have been selected by an initiator and may continue with an information transfer phase.

Reselection In Sequence

➤ 1 Load the SCSI IDs in the SCSIID register (345h).

2 Set ENRESELI in the SCSISEQ register (bit 4, 340h); this enables the Reselection In sequence.

> Note
> You may also set ENAUTOATNI in the SCSISEQ register (bit 2, 340h) to automatically enable ATN on reselection.

3 Wait for SELDI to be set and TARGET to be cleared in the SSTAT0 register (bits 5 and 7, 34Bh).

> Note
> If TARGET is set, you have been selected by an initiator.

4 Load the expected SCSI phase in the SCSISIGO register (bits 7–5, 343h).

5 Load the SCSIRATE register (344h) as appropriate.

6 When SELDI is set and TARGET is cleared in the SSTAT0 register (bits 5 and 7, 34Bh), you have been reselected and may continue with an information transfer phase.

Reselection Out Sequence

➤ 1 Load the SCSIID (345h) and SCSIRATE (344h) registers.

2 Set the SCSI phase to enter after reselection in the SCSISIGO (bits 7–5, 343h) register. All other controls must be cleared.

3 Set TEMODEO and ENSELO in the SCSISEQ register (bits 7 and 6, 340h); this enables the Reselection Out sequence. The Auto-Attention options must both be cleared.

4 Wait for SELINGO or SELDO to be set in the SSTAT0 register (bits 4 or 6, 34Bh), or for SELTO to be set in the SSTAT1 register (bit 7, 34Ch).

> Note
> TARGET (bit 7, 34Bh) should be set. If it is not, you have initiated a Selection sequence.

5 Load the SXFRCTL1 register (342h) with the desired values.

6 Load the STCNT register (348h–34Ah) with the transfer count.

7 Set CLRCH1 in the SXFRCTL0 register (bit 1, 341h); this clears the transfer counter and channel one. Then set SXFRCTL0 for the proper channel and SCSI Transfer enabled.

> Note
> If the transfer mode is SCSI PIO, it is not necessary to clear channel one. However, you should do it anyway, as the target might respond with an unexpected phase, such as Data In Synchronous, when you are expecting Message Out.

8 When SELDO and TARGET are set in the SSTAT0 register (bits 6 and 7, 34Bh), you have reselected an initiator; you may initiate an information transfer phase.

SCSI PIO Data Transfers

Use the SCSI PIO data transfer modes whenever you need host processor intervention during the transfer, such as during message exchanges. SCSI PIO is asynchronous only, so you should not use it for data-in or data-out phases. There are two types of SCSI PIO: Manual and Automatic.

- **Manual**: The host processor writes directly to the SCSI data bus via the latch at 346h and reads or drives the SCSI bus control lines via the register at 343h. In Manual mode, the AIC-6360 is essentially a bus buffer having no control functions. Manual mode supports asynchronous SCSI transfers only.

- **Automatic**: The host processor writes directly to the SCSI data bus via the latch at 346h, while the AIC-6360 performs SCSI bus control automatically. Automatic SCSI PIO transfers can be monitored by interrupt or polling status. Interrupt configuration for the AIC-6360 is controlled by the interrupt mode registers at 350h and 351h. Polling mode is driven off the SPIORDY status bit in the SSTAT0 register (bit 1, 34Bh). SCSI PIO mode supports asynchronous SCSI transfers only.

The following sections describe the tasks you must perform to accomplish automatic SCSI PIO transfers as an initiator or target.

Initiator Data Transfer: Host to SCSI

➤ 1 Set bit 3 (SPIOEN) and set bit 5 (select CH1/CH2) in the SXFRCTL0 register (341h).

2 Set bit 6 (8BIT/-16BIT), reset bit 5 (DMA/-PIO) and set bit 1 (RSTFIFO) in the DMACNTRL0 register (352h).

3 Wait for SPIORDY to be set in the SSTAT0 register (bit 1, 34Bh).

4 Write data to the SCSIDAT register (bits 7–0, 346h).

5 If you have more data to transfer, repeat Steps 2–4. If not, proceed to Step 6.

6 Clear SPIOEN in the SXFRCTL0 register (bit 3, 341h).

Initiator Data Transfer: SCSI to Host

➤ 1 Set SPIOEN in the SXFRCTL0 register (bit 3, 341h).

2 Wait for SPIORDY to be set in the SSTAT0 register (bit 1, 34Bh).

3 Read data from the SCSIDAT register (bits 7–0, 346h).

4 Test PHASEMIS in the SSTAT1 register (bit 4, 34Ch). If PHASEMIS is cleared, there is more data to transfer; repeat Steps 2–4. If PHASEMIS is set, there is no more data to transfer; proceed to Step 5.

5 Clear SPIOEN in the SXFRCTL0 register (bit 3, 341h).

Target Data Transfer: Host to SCSI

➤ 1 Set the SCSI phase in the SCSISIGO register (bits 7–5, 343h).

2 Set SPIOEN in the SXFRCTL0 register (bit 3, 341h).

3 Wait for SPIORDY to be set in the SSTAT0 register (bit 1, 34Bh).

4 Write data to the SCSIDAT register (bits 7–0, 346h); this action asserts REQ.

5 If you have more data to transfer, repeat Steps 3–4. If not, proceed to Step 6.

6 Clear SPIOEN in the SXFRCTL0 register (bit 3, 341h).

Target Data Transfer: SCSI to Host

➤ 1 Set the SCSI phase in the SCSISIGO register (bits 7–5, 343h).

2 Set SPIOEN in the SXFRCTL0 register (bit 3, 341h); this action asserts REQ.

3 Wait for SPIORDY to be set in the SSTAT0 register (bit 1, 34Bh).

4 Read data from the SCSIDAT register (bits 7–0, 346h); REQ is de-asserted when the initiator de-asserts ACK, and another REQ is automatically asserted.

5 If the current byte is not the last byte to be transferred, repeat Steps 3–4. If the current byte is the last byte to be transferred, go to Step 6.

6 Clear SPIOEN in the SXFRCTL0 register (bit 3, 341h) *before* reading data from the SCSIDAT register (bits 7–0, 346h).

Normal Mode Data Transfers

Use the Normal data transfer mode for normal SCSI data transfers (commands and data). Normal mode uses two types of host transfer modes: host PIO and host DMA.

- **Host PIO**: The host processor writes to or reads from the 128-byte host FIFO via the data register at 356h. Host PIO transfers are driven off the status bits in the status register at 352h.

- **Host DMA**: The host processor sets up the data transfer operation by loading its DMA controller with a memory pointer and the transfer count. The host DMA controller writes/reads transfer data to/from the 128-byte host FIFO via the data register at 356h. Once begun, host DMA transfers run to completion without further host processor intervention.

The following sections describe how to accomplish normal mode SCSI transfers as an initiator or target.

Initiator Data Transfer: Host to SCSI in Host PIO Mode

➤ **1** Wait for the phase change.

2 Set the expected SCSI phase in the SCSISIGI register (bits 7–5, 343h).

3 Turn off the data path, then turn it on again.

4 Clear the transfer count and the SCSI and host FIFOs.

5 Set SCSIEN and DMAEN in the SXFRCTL0 register (bits 7 and 6, 341h) and select CH1; this enables the AIC-6360 SCSI logic.

6 Set ENDMA and WRITE/–READ, and clear DMA/–PIO in the DMACNTRL0 register (bits 7, 3, and 5, 352h).

7 Wait for DFIFOEMP or INTSTAT to be set in the DMASTAT register (bits 3 and 5, 354h).

8 Wait for INSTAT to clear.

9 If DFIFOEMP is set and INTSTAT is cleared in the DMASTAT register (bits 3 and 5, 354h), use REP OUTSW to write 128 bytes (64 words).

10 Adjust host processor transfer count.

11 Test for the end of the transfer in the host processor by checking ATDONE (bit 7, 354h); repeat Steps 7–10 until all data has been written.

12 When all data has been written, clear ENDMA in the DMACNTRL0 register (bit 7, 352h).

Initiator Data Transfer: SCSI to Host in Host PIO Mode

➤ 1 Wait for the phase change.

2 Set the expected SCSI phase in the SCSISIGI register (bits 7–5, 343h).

3 Test and match the phase.

4 Clear the transfer count and the SCSI and host FIFOs.

5 Set SCSIEN and DMAEN in the SXFRCTL0 register (bits 7 and 6, 341h); this enables the AIC-6360 SCSI logic.

6 Set ENDMA, and clear WRITE/–READ and DMA/–PIO in the DMACNTRL0 register (bits 7, 3, and 5, 352h).

7 Wait for DFIFOFULL or INTSTAT to be set in the DMASTAT register (bits 4 and 5, 354h).

8 Wait for INSTAT to be cleared. You may also need to wait for Word Ready (DMASTAT).

9 If DFIFOFULL is set and INTSTAT is cleared in the DMASTAT register (bits 4 and 5, 354h), use REP INS to read 128 bytes (64 words).

10 Adjust host processor transfer count.

11 Test for the end of the transfer in the host processor; repeat Steps 7–10 until all data has been read.

12 When all data has been read, clear ENDMA in the DMACNTRL0 register (bit 7, 352h).

Initiator Data Transfer: Host to SCSI in Host DMA Mode

➤ 1 Set the expected SCSI phase in the SCSISIGI register (bits 7–5, 343h).

2 Clear the transfer count and the SCSI and host FIFOs.

3 Set up the host DMA controller for address, byte count, and transfer mode.

4 Wait for REQINIT to be set and PHASEMIS to be cleared in the SSTAT1 register (bits 0 and 4, 34Ch).

5 Set SCSIEN and DMAEN in the SXFRCTL0 register (bits 7 and 6, 341h); this enables the AIC-6360 SCSI logic.

6 Set ENDMA, 8BIT/–16BIT, WRITE/–READ, and DMA/–PIO in the DMACNTRL0 register (bits 7, 6, 3, and 5, 352h).

7 Wait for the DMADONE, PHASEMIS, or other interrupts. Interrupts must be enabled in order to assert IRQ.

Initiator Data Transfer: SCSI to Host in Host DMA Mode

➤ 1 Set the expected SCSI phase in the SCSISIGI register (bits 7–5, 343h).

2 Clear the transfer count and the SCSI and host FIFOs.

3 Set up the host DMA controller for address, byte count, and transfer mode.

4 Wait for REQINIT to be set and PHASEMIS to be cleared in the SSTAT1 register (bits 0 and 4, 34Ch).

5 Set SCSIEN and DMAEN in the SXFRCTL0 register (bits 7 and 6, 341h); this enables the AIC-6360 SCSI logic.

6 Set ENDMA, 8BIT/–16BIT, and DMA/–PIO and clear WRITE/–READ in the DMACNTRL0 register (bits 7, 6, 5, and 3, 352h).

7 Wait for the DMADONE, PHASEMIS, or other interrupts. Interrupts must be enabled in order to assert IRQ.

Target Data Transfer: Host to SCSI in Host PIO Mode

➤ 1 Set the SCSI phase in the SCSISIGO register (bits 7–5, 343h).

2 Load the SCSI transfer count in the STCNT register (bits 7–0, 348h–34Ah).

3 Load the SXFRCTL0 and SXFRCTL1 registers (341h and 342h) with the desired values.

4 Clear the SCSI and host FIFOs.

5 Set SCSIEN and DMAEN in the SXFRCTL0 register (bits 7 and 6, 341h); this enables the AIC-6360 SCSI logic.

6 Set ENDMA and WRITE/–READ and clear DMA/–PIO in the DMACNTRL0 register (bits 7, 3, and 5, 352h).

7 Wait for DFIFOEMP or INTSTAT to be set in the DMASTAT register (bits 3 and 5, 354h).

8 If DFIFOEMP is set and INTSTAT is cleared in the DMASTAT register (bits 3 and 5, 354h), use REP OUTSW to write 128 bytes (64 words).

9 Adjust host processor transfer count.

10 Test for the end of the transfer in the host processor.

11 repeat Steps 7–10 until all data has been written.

12 When all data has been written, clear ENDMA in the DMACNTRL0 register (bit 7, 352h).

13 When the command has completed, clear the SCSISIGO register (bits 7–0, 343h); this forces Bus Free.

Target Data Transfer: SCSI to Host in Host PIO Mode

➤ 1 Set the SCSI phase in the SCSISIGO register (bits 7–5, 343h).

2 Load the SCSI transfer count in the STCNT register (bits 7–0, 348h–34Ah).

3 Load the SXFRCTL0 and SXFRCTL1 registers (341h and 342h) with the desired values.

4 Clear the SCSI and host FIFOs.

5 Set SCSIEN and DMAEN in the SXFRCTL0 register (bits 7 and 6, 341h); this enables the AIC-6360 SCSI logic.

6 Set ENDMA, and clear DMA/–PIO and WRITE/–READ in the DMACNTRL0 register (bits 7, 5, and 3, 352h).

7 Wait for DFIFOFULL or INTSTAT to be set in the DMASTAT register (bits 4 and 5, 354h).

8 If DFIFOFULL is set and INTSTAT is cleared in the DMASTAT register (bits 4 and 5, 354h), use REP INS to read 128 bytes (64 words).

9 Adjust host processor transfer count.

10 Test for the end of the transfer in the host processor; repeat Steps 7–10 until all data has been read.

11 When all data has been read, clear ENDMA in the DMACNTRL0 register (bits 7, 352h).

12 When the command has completed, clear the SCSISIGO register (bits 7–0, 343h); this forces Bus Free.

Target Data Transfer: Host to SCSI to Host in DMA Mode

➤ 1 Set the SCSI phase in the SCSISIGO register (bit 7–5, 343h).

2 Load the SCSI transfer count in the STCNT register (bits 7–0, 348h–34Ah).

3 Load the SXFRCTL0 and SXFRCTL1 registers (341h and 342h) with the desired values.

4 Clear the SCSI and host FIFOs.

5 Set up the host DMA controller for address, byte count, and transfer mode.

6 Wait for REQINIT to be set and PHASEMIS to be cleared in the SSTAT1 register (bits 0 and 4, 34Ch).

7 Set SCSIEN and DMAEN in the SXFRCTL0 register (bits 7 and 6, 341h); this enables the AIC-6360 SCSI logic.

8 Set ENDMA, 8BIT/–16BIT, WRITE/–READ, and DMA/–PIO in the DMACNTRL0 register (bits 7, 6, 3, and 5, 352h).

9 Wait for the DMADONE, PHASEMIS, or other interrupts. Interrupts must be enabled in order to assert IRQ.

10 When the command has completed, clear the SCSISIGO register (bits 7–0, 343h); this forces Bus Free.

Target Data Transfer: SCSI to Host in Host DMA Mode

➤ 1 Set the SCSI phase in the SCSISIGO register (bits 7–5, 343h).

2 Load the SCSI transfer count in the STCNT register (bits 7–0, 348h–34Ah).

3 Load the SXFRCTL0 and SXFRCTL1 registers (341h and 342h) with the desired values.

4 Clear the SCSI and host FIFOs.

5 Set up the host DMA controller for address, byte count, and transfer mode.

6 Wait for REQINIT to be set and PHASEMIS to be cleared in the SSTAT1 register (bits 0 and 4, 34Ch).

7 Set SCSIEN and DMAEN in the SXFRCTL0 register (bits 7 and 6, 341h); this enables the AIC-6360 SCSI logic.

8 Set ENDMA, 8BIT/–16BIT, and DMA/–PIO and clear WRITE/–READ in the DMACNTRL0 register (bits 7, 6, 5, and 3, 352h).

9 Wait for the DMADONE, PHASEMIS, or other interrupts. Interrupts must be enabled in order to assert IRQ.

10 When the command has completed, clear the SCSISIGO register (bits 7–0, 343h); this forces Bus Free.

Odd Byte Disconnects

It is possible for a SCSI device to disconnect after an odd number of bytes has been transferred across the SCSI bus while in 16-bit DMA mode. In that case, the chip has a mechanism to change modes of operation from DMA to PIO and back again without loss of data. The general procedure is as follows:

Read Operation

➤ 1 Check to determine that only one byte is left.

2 Switch to PIO mode, leaving ENDMA in DMACNTRL0 set.

3 Read byte from port 356h and save.

4 To continue the transfer, set chip for PIO write.

5 Write byte to port 356h.

6 Change direction in DMACNTRL0 to read.

7 Change mode to DMA.

8 Enable SCSI transfers.

Write Operation

➤ 1 Check to determine that an odd number of bytes has been transferred across the SCSI bus.

2 Save the DMA address pointer and word counter minus 2.

3 To continue the transfer, set the BYTEALIGN bit in SXFRCTL1.

4 Enable DMA transfer; the first byte will be thrown away. Initiator Message Handling.

Diagnostics

The 128-byte host FIFO and associated logic can be tested using the wrap-around feature. Transfers are accomplished in the normal manner, using host DMA or host PIO mode.

To check the FIFO, make sure that DMAEN and SCSIEN in the SXFRCTL0 register (bits 6 and 7, 341h) are cleared. Set WRITE/–READ in the DMACNTRL0 register (bit 3, 352h) and begin the transfer. To read the data back, clear WRITE/–READ in the DMACNTRL0 register (bit 3, 352h).

Initiator Message Handling

Messages are intended to be handled by SCSI PIO transfer. Certain special cases to consider are messages after selection, multiple messages, or parity errors. If messages after selection are to be handled by the initiator, ATN is asserted on the bus. The target responds with the Message Out phase at this time. The first message is the ID message, and after this, the initiator has the option of sending a multiple-byte message such as a synchronous data transfer request. ATN remains asserted during Message Out transfers, until cleared by setting CLRATNO in CLRSINT1 (bit 6, 34Ch). In order to maintain SCSI protocol, ATN should be cleared before the last ACK of a message sequence or, in the case of automatic SCSI PIO, the last write to SCSIDAT.

In the case of an error condition, ATN should be cleared after the first REQ of the Message Out phase and before the last ACK of the message sequence.

If a parity error occurs on Message In, ATN is asserted before ACK, and the message should be retransmitted.

Figure 5-1 illustrates a sample application using the AIC-6360 chip.

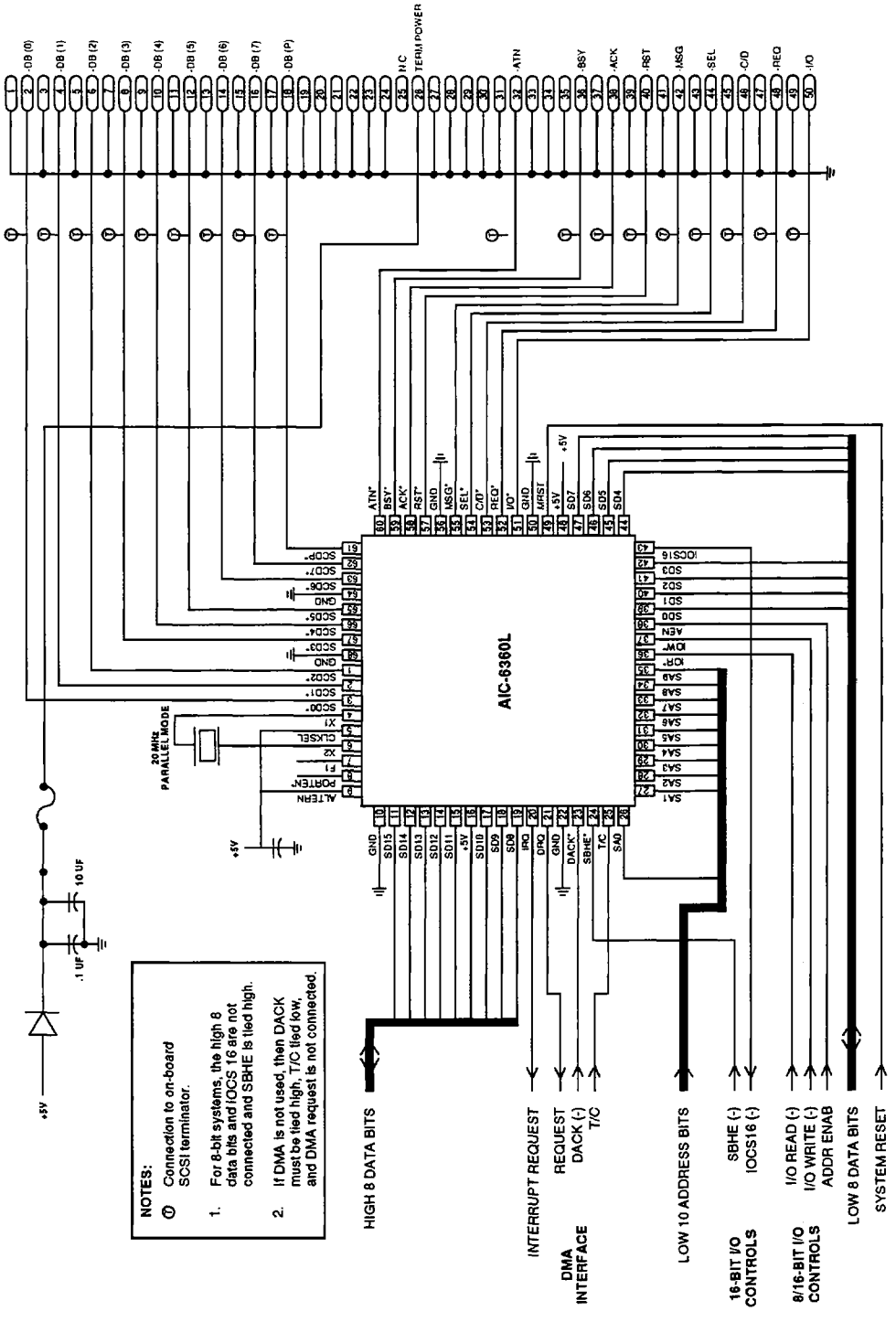


Figure 5-1. Sample AIC-6360 Application

6

Electrical Information

Absolute Maximum Ratings

Table 6-1. Absolute Maximum Ratings

Parameter	Range
Storage temperature	-65° to 150° C
Power supply voltage	0 to 7 Volts
Voltage on any pin	-0.5 to Vcc+0.5 Volts

Operating Conditions

Table 6-2. Operating Conditions

Parameter	Range
Ambient temperature	0° to 70° C
Supply voltage	4.5 to 5.5 Volts
Rise Time t_r	ns
Fall Time t_f	ns
Load Capacitance C_L	50 pf, unless otherwise noted

DC Electrical Characteristics

Table 6-3. DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{il}	Input Low Voltage, All Pins				0.8	V
V_{ih}	Input High Voltage, All Pins		2.0			V
V_h	Input Hysteresis, SCSI Signals Only		200			mV
V_{ol1}	Output Low Voltage, PORTEN*	I_{ol} = 2 mA			0.5	V
V_{ol2}	Output Low Voltage, SD0-15, DRQ, IRQ, IOCS 16*	I_{ol} = 24 mA			0.5	V
V_{ol3}	Output Low Voltage, All SCSI Signals	I_{ol} = 48 mA			0.5	V
V_{oh1}	Output High Voltage, PORTEN*	I_{ol} = –2 mA	2.4			V
V_{oh2}	Output High Voltage, SD0-15 DRQ, IRQ	I_{ol} = –8 mA	2.4			V
I_{o2}	Output Leakage for Tristate and Open Collector Drivers	$V_{dd} \geq Vin \geq GND$		±40		A
I_{dd1}	Operating Current Consumption	20 MHz External Clock		19.8	25	mA
		20 MHz Internal Crystal Oscillator		29.0	35	mA
I_{dd2}	Powerdown Current Consumption	20 MHz External Clock		5.8	10	mA
		20 MHz Internal Crystal Oscillator		14.2	20	mA
I_{dd3}	Static Current Consumption	$V_{IN} = V_{dd}$, Pin F1 = V_{dd}		1.5	5	mA
C_{IN}	Input Capacitance	F_c = 1 MHz			10	pF
C_{OUT}	Output Capacitance				15	pF

Crystal Oscillator Specification

Table 6-4. Crystal Oscillator Specification

Parameter	Value
Design type	Pierce
Min. resistor shunting XIN and XOUT	21,000
Max. capacitance between XIN and XOUT	12 pF[1]
Max. motional resistance of crystal	50 ohm
Oscillation mode	Fundamental
Min. crystal Q	20,000
Oscillation frequency	20 MHz
[1] including Co of crystal and board layout	

Notes:

- Crystal cut is not critical, if fundamental is the strongest oscillation mode.
- The required capacitors are contained on the chip.
- Do not ground any crystal terminals.
- Since the oscillator is an analog device, it should experience as little power supply noise as possible. This means that the user must not inject PC board noise into XNE (VDD of the oscillator), and there should be a well-filtered internal VSS pin as close to the cell as possible. Switching noise on the outer VSS bus is isolated from the circuit and therefore is not a problem. Furthermore, the X1 input pin is sensitive to latch-up at voltages above approximately 80 mA.

System Timing

This section contains AC timing information for the AIC-6360. All timing presumes operation with a 20 MHz clock.

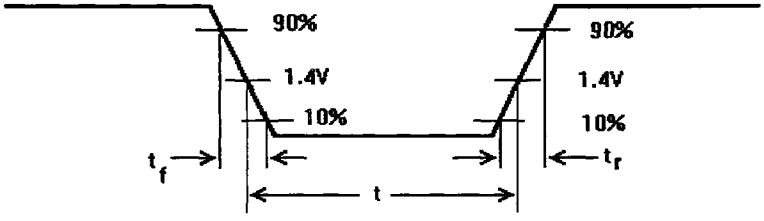
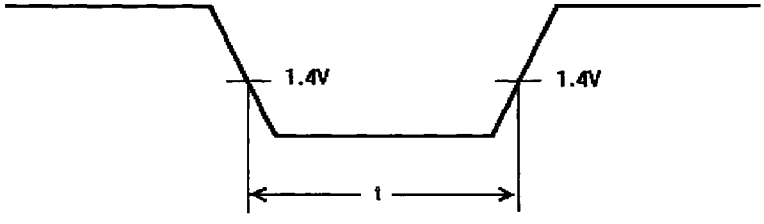


Figure 6-1. AC Input Conditions



C = 50 pf unless otherwise noted

Figure 6-2. AC Output Conditions

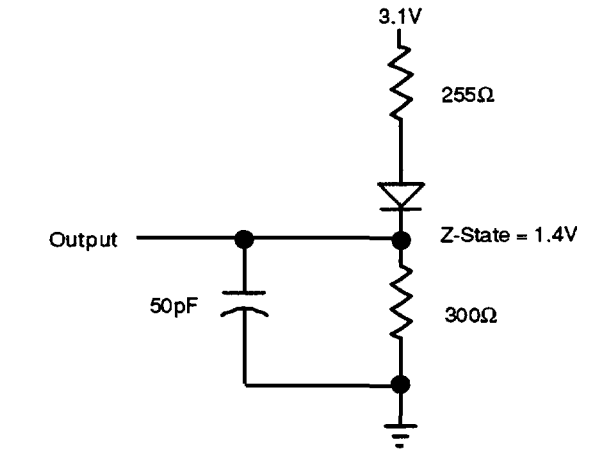


Figure 6-3. AC Test Load for All Outputs Except SCSI and PORTEN

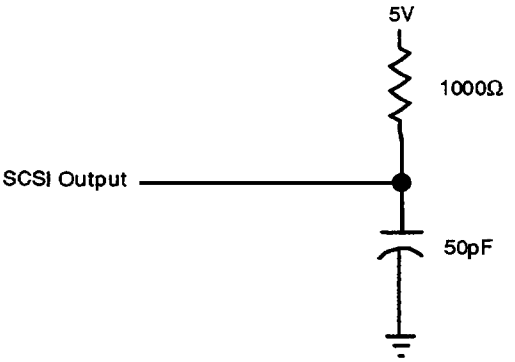


Figure 6-4. AC Test Load for SCSI Outputs

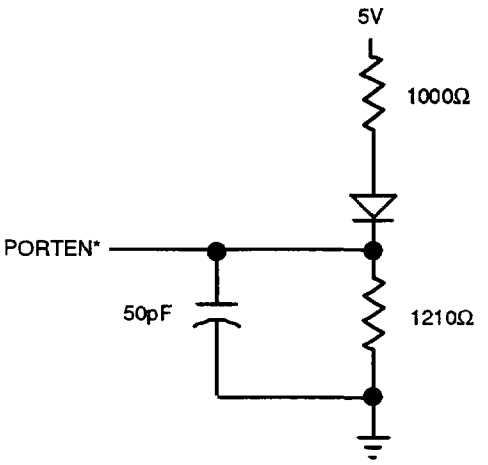
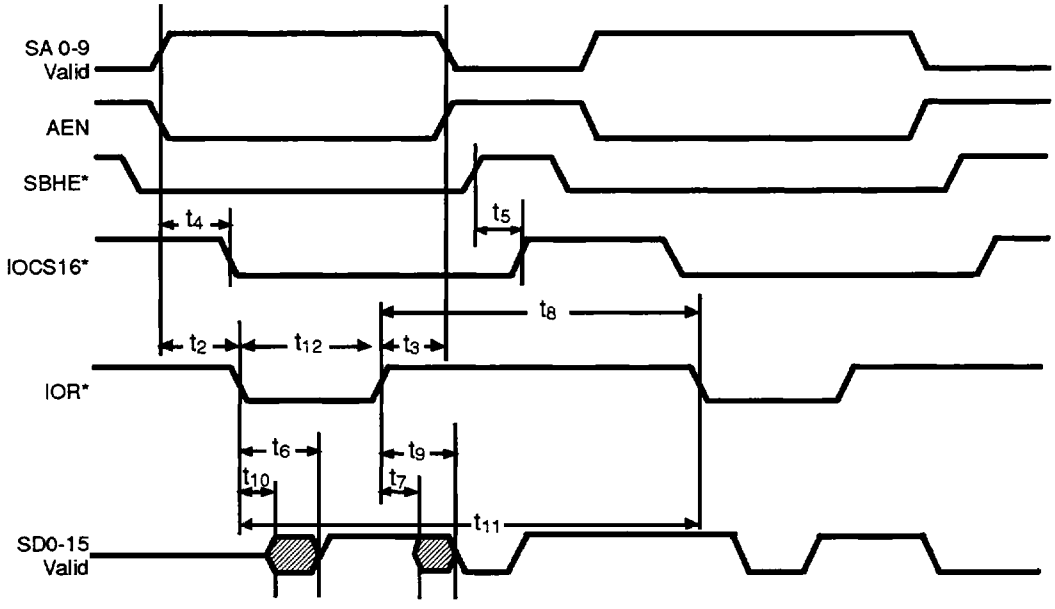


Figure 6-5. AC Test Load for PORTEN Output

Host Processor PIO Data Read Operation



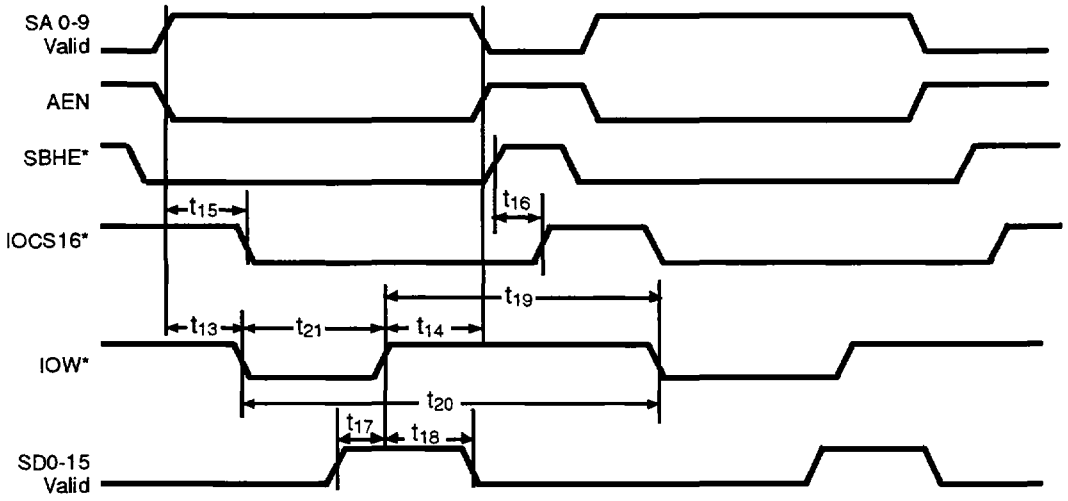
Parameter	Description	Min[1]	Max[1]
t_1	Chip clock period	50	
t_2	Address setup time to IOR* falling	25	
t_3	Address hold time after IOR* rising	25	
t_4	IOCS16* valid after address and SBHE* valid		60
t_5	IOCS16* disabled after address and SBHE* invalid		30
t_6	Valid data delay from IOR* falling	6	60
t_7	Data hold time after IOR* rising	4	
t_8	Time between consecutive IOR* pulse	100	
t_9	Driver OFF time from IOR* rising		25
t_{10}	Driver ON time from IOR* falling	6	25
t_{11}	Read cycle time	120	
t_{12}	IOR* pulse width	20	

[1] Min and Max data in all the timing diagrams is given in nanoseconds.

Notes:

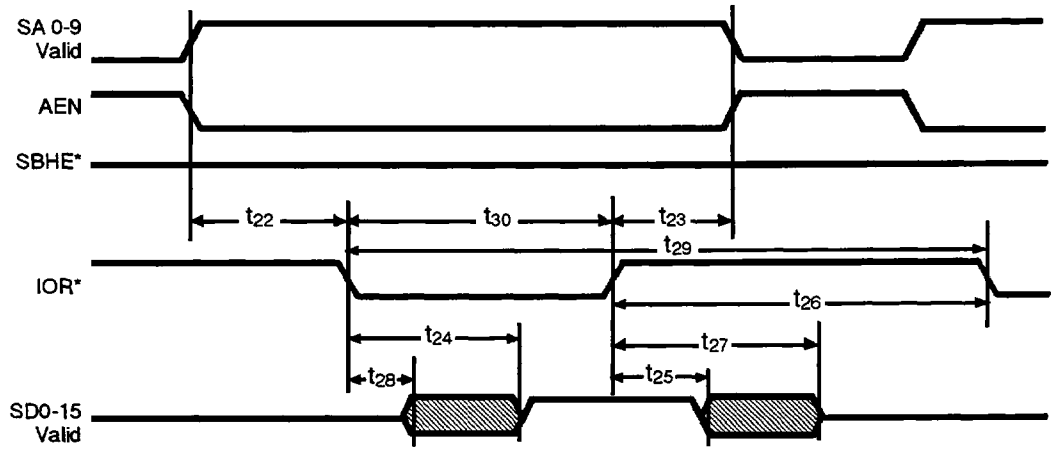
- t_6 is measured from the assertion of IOR* to the point at which the outputs on SD0-15 achieve a valid Voi or Voh output voltage level.
- t_7 is measured from the deassertion of IOR* to the point at which the outputs on SD0-15 no longer maintain a valid Voi or Voh output voltage level.
- t_9 is measured from the deassertion of IOR* to the point at which the outputs on SD0-15 deviate by 0.1V from their asserted high or low logic level.
- t_{10} is measured from the assertion of IOR* to the point at which the outputs on SD0-15 deviate by 0.1V from the tristate bias voltage level of 1.4V.

Host Processor PIO Data Write Operation



Parameter	Description	Min	Max
t_{13}	Address setup time to IOW* falling	25	
t_{14}	Address hold time after IOW* rising	25	
t_{15}	IOCS16* valid after address and SBHE* valid		60
t_{16}	IOCS16* hi-z after address and SBHE* invalid		30
t_{17}	Data setup time to IOW* rising	5	
t_{18}	Data hold time after IOW* rising	15	
t_{19}	Time between consecutive IOW* pulses	100	
t_{20}	Write cycle time	110	
t_{21}	IOW* pulse width	10	

Host Processor I/O Read Operation

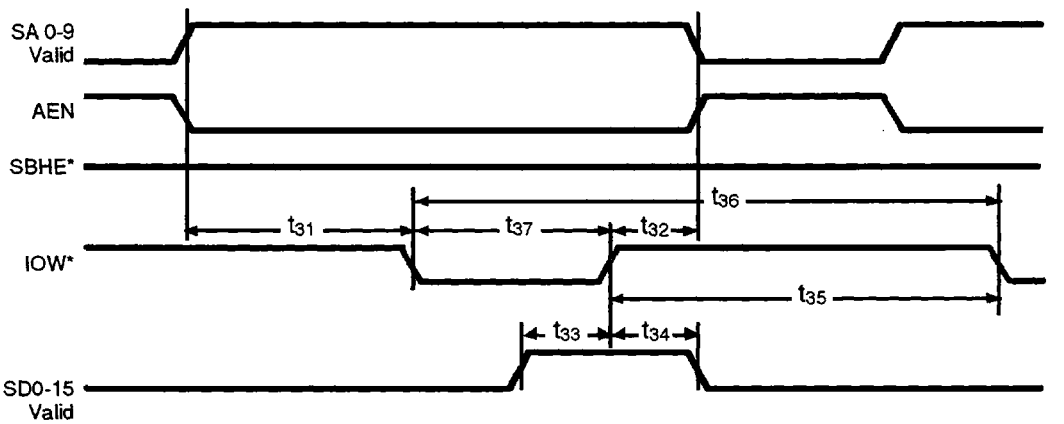


Parameter	Description	Min	Max
t22	Address setup time to IOR* falling	25	
t23	Address hold time after IOR* rising	25	
t24	Valid data delay from IOR* falling		60
t25	Data hold time after IOR* rising	4	
t26	Time between consecutive IOR* pulses (DWORD)	100	
t27	Driver OFF time from IOR* rising		25
t28	Driver ON time from IOR* falling	6	25
t29	Read cycle time	120	
t30	IOR* pulse width	20	

Notes:

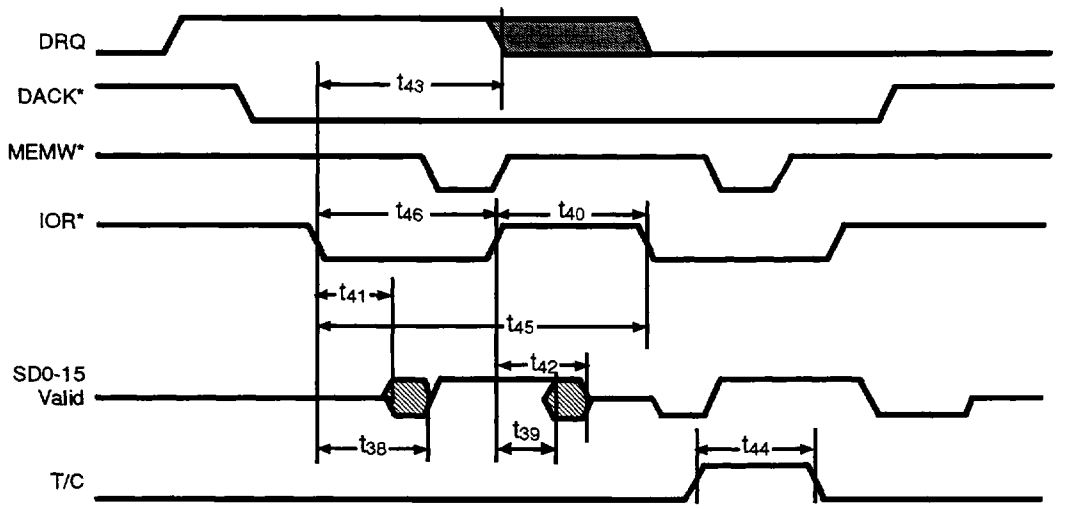
- t_{24} is measured from the assertion of IOR* to the point at which the outputs on SD0-15 achieve a valid Voi or Voh output voltage level.
- t_{25} is measured from the deassertion of IOR* to the point at which the outputs on SD0-15 no longer maintain a valid Voi or Voh output voltage level.
- t_{27} is measured from the deassertion of IOR* to the point at which the outputs on SD0-15 deviate by 0.1V from their asserted high or low logic level.
- t_{28} is measured from the assertion of IOR* to the point at which the outputs on SD0-15 deviate by 0.1V from the tristate bias voltage level of 1.4V.

Host Processor I/O Write Operation



Parameter	Description	Min	Max
t31	Address setup time to IOW* falling	25	
t32	Address hold time after IOW* rising	25	
t33	Data setup time to IOW* rising	5	
t34	Data hold time after IOW* rising	15	
t35	Time between consecutive IOW* pulses (DWORD)	100	
t36	Write cycle time	110	
t37	IOW* pulse width	10	

Host Processor DMA Read Operation

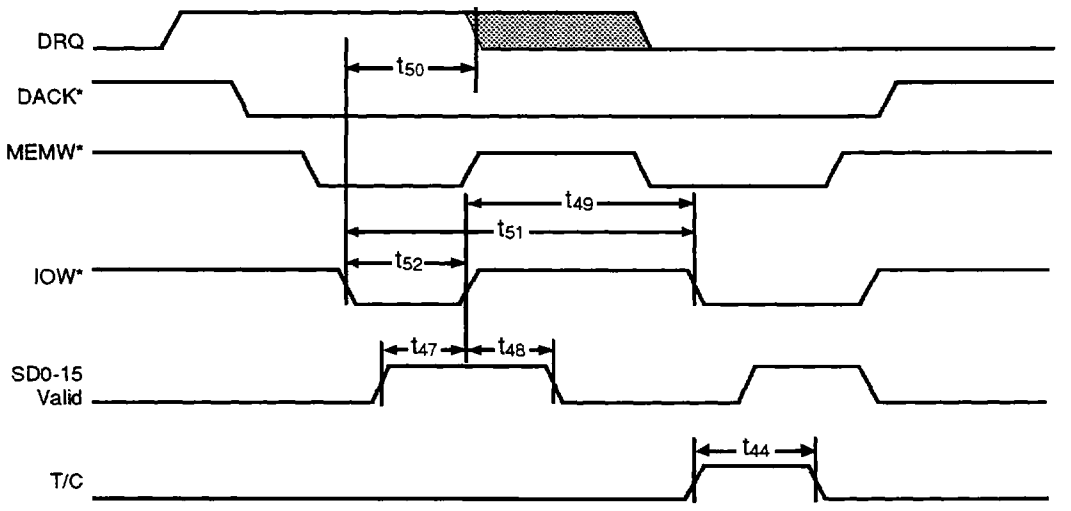


Parameter	Description	Min	Max
t_{38}	Data valid from IOR* falling		60
t_{39}	Data hold time after IOR* rising	4	
t_{40}	Time between consecutive IOR*	100	
t_{41}	Driver ON time from IOR* falling		25
t_{42}	Driver OFF time from IOR* rising		25
t_{43}	DRQ OFF time from IOR* falling	10	60
t_{44}	Terminal count pulse width	50	
t_{45}	Read cycle time	120	
t_{46}	IOR* pulse width	20	

Notes:

- t_{38} is measured from the assertion of IOR* to the point at which the outputs on SD0-15 achieve a valid Voi or Voh output voltage level.
- t_{39} is measured from the deassertion of IOR* to the point at which the outputs on SD0-15 no longer maintain a valid Voi or Voh output voltage level.
- t_{40} is measured from the deassertion of IOR* to the point at which the outputs on SD0-15 deviate by 0.1V from their asserted high or low logic level.
- t_{41} is measured from the assertion of IOR* to the point at which the outputs on SD0-15 deviate by 0.1V from the tristate bias voltage level of 1.4V.

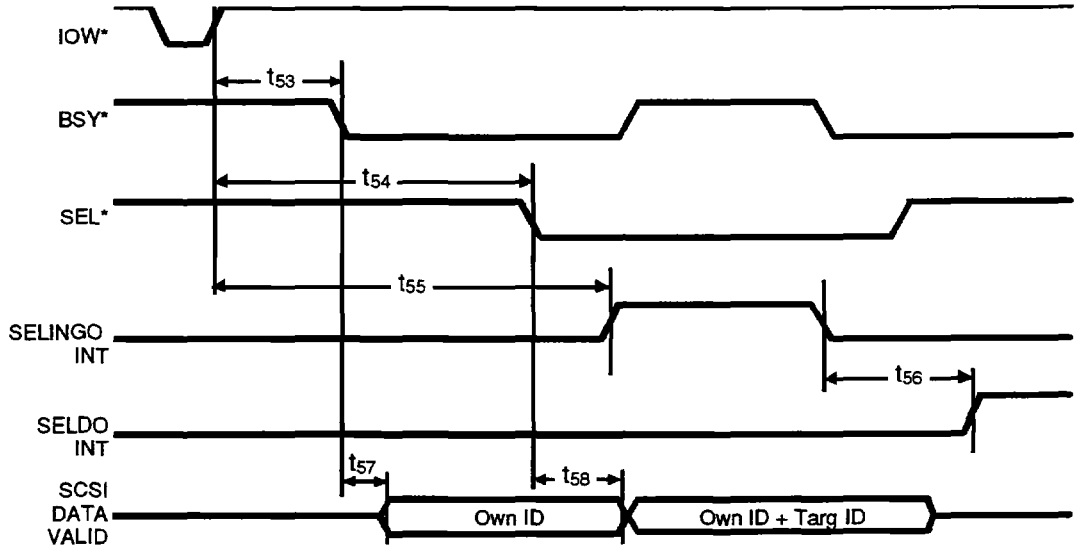
Host Processor DMA Write Operation



Parameter	Description	Min	Max
t_{47}	Data setup time to IOW* rising	5	
t_{48}	Data hold time to IOW* rising	15	
t_{49}	Time between consecutive IOW* pulses	100	
t_{50}	DRQ off time from IOW* falling	10	60
t_{51}	Write cycle time	110	
t_{52}	IOW* pulse width	10	

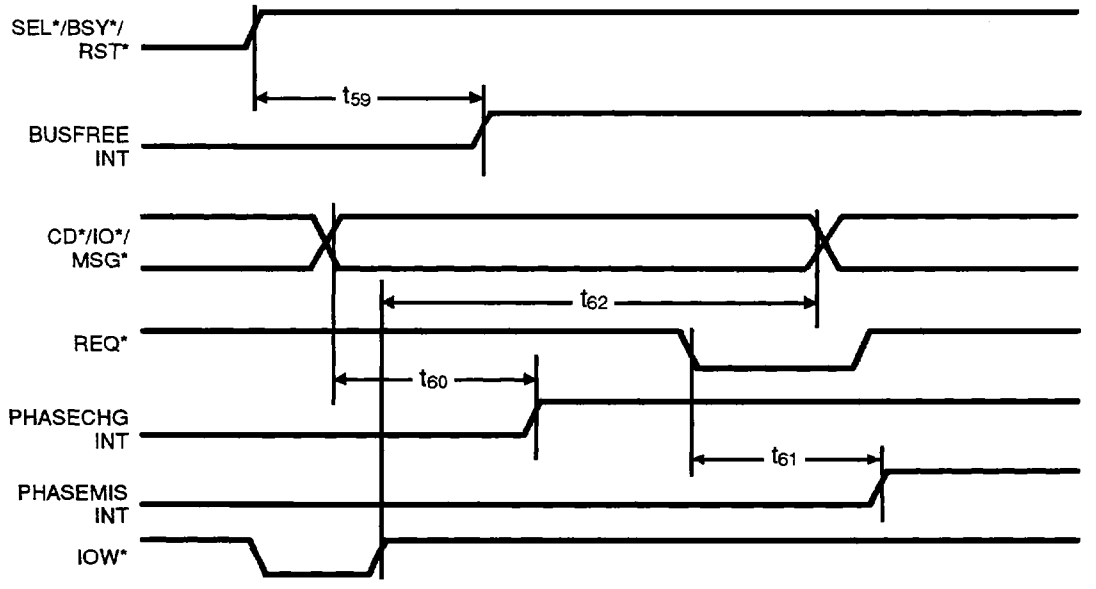
SCSI Bus Timing

Arbitration/Selection



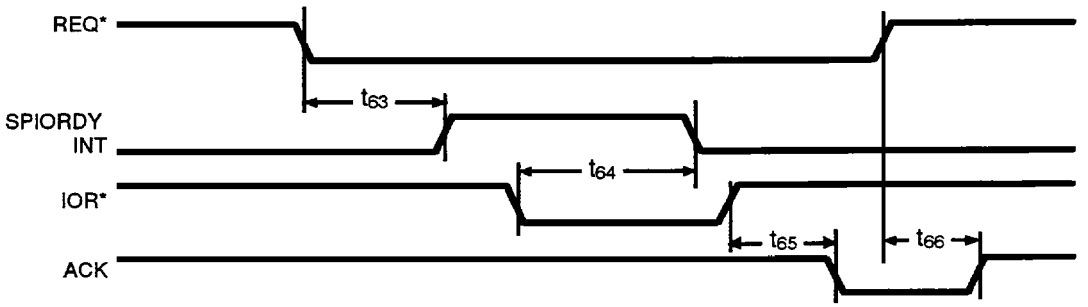
Parameter	Description	Min	Max
t_{53}	BSY* active from IOW* rising		$16t_1 + 60$
t_{54}	SEL* active from IOW* rising		$64t_1 + 60$
t_{55}	SELINGO interrupt from ENSELO		$92t_1 + 60$
t_{56}	SELDO interrupt from Target BSY*		$4t_1 + 60$
t_{57}	Own ID valid from BSY* falling		20
t_{58}	Target ID valid from SEL* falling	$24t_1 + 60$	

SCSI Bus Free Detection and Phase Change Interrupts



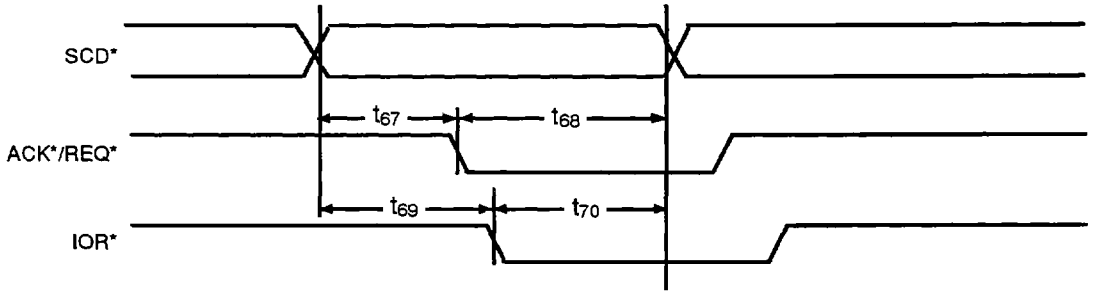
Parameter	Description	Min	Max
t_{59}	BUS FREE from SEL*/BSY*/RST* rising		$9t_{1}+40$
t_{60}	Interrupt from phase change		37
t_{61}	Interrupt from phase change/REQ		40
t_{62}	Phase change[1] from IOW* rising		46
[1] Target mode			

SCSI PIO



Parameter	Description	Min	Max
t_{63}	SPIORDY interrupt from REQ* falling		$3t_1 + 35$
t_{64}	SPIORDY cleared from IOR* falling		60
t_{65}	ACK asserted from IOR* rising		$3t_1 + 35$
t_{66}	ACK de-asserted from REQ* rising		$2t_1 + 62$

SCSI Data Setup and Hold, Latched Data and PIO



Parameter	Description	Min	Max
t67	SCSI Data setup to REQ* or ACK*[1]	5	
t68	SCSI Data hold after REQ* or ACK*[1]	15	
t69	SCSI Data setup to IOR* falling[2]	15	
t70	SCSI Data hold after IOR* falling[2]	5	

[1] Initiator mode uses leading edge of REQ* to latch data, and Target mode uses leading edge of ACK*. These times apply to synchronous, asynchronous, and auto PIO modes.

[2] These times apply to programmed I/O when reading port 347h.

7

Package Outlines

This chapter has package outline diagrams for the available AIC-6360 packages:

- 80-pin QFP
- 100-pin TQFP
- 68-pin PLCC

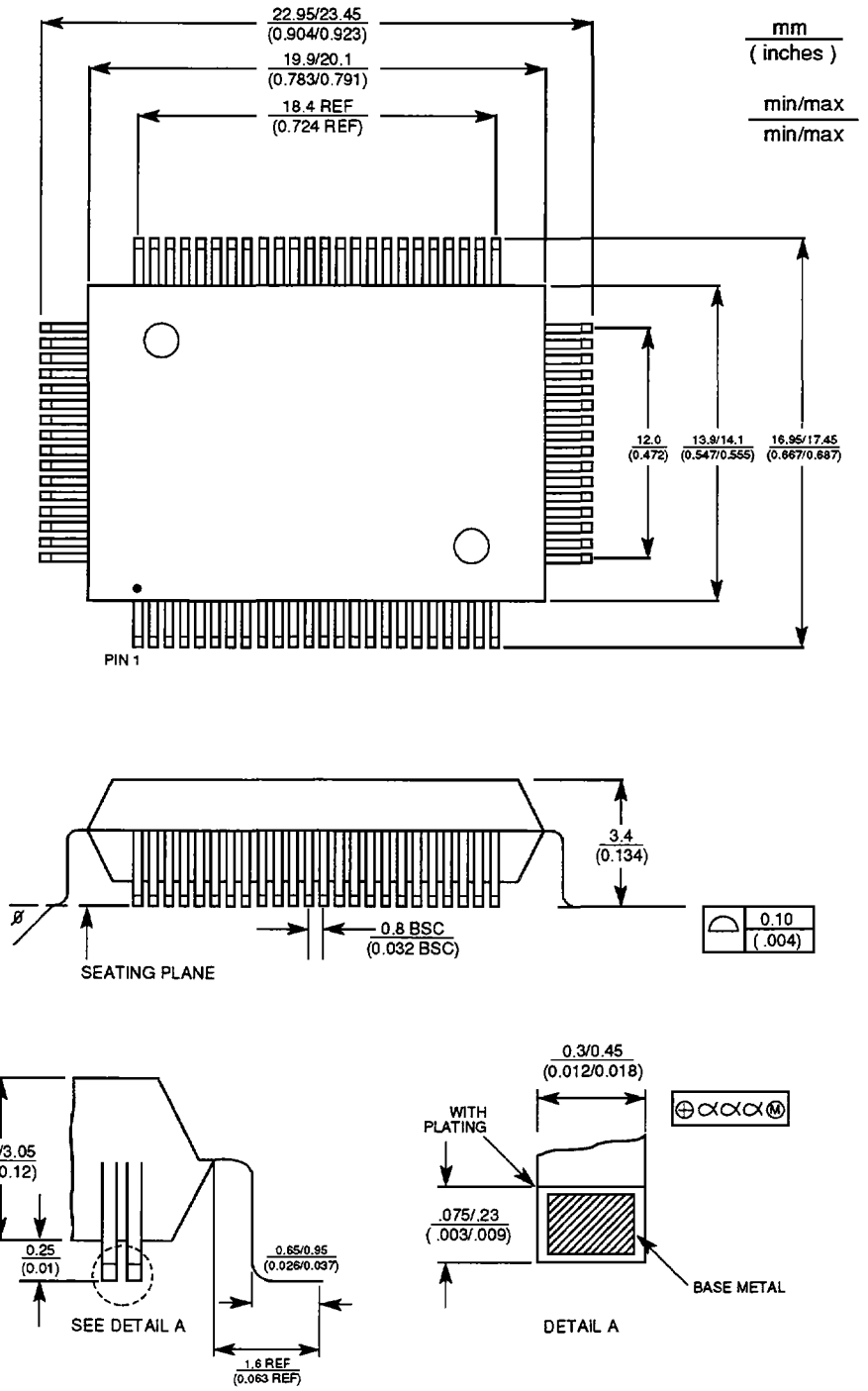


Figure 7-1. 80-Pin QFP Package

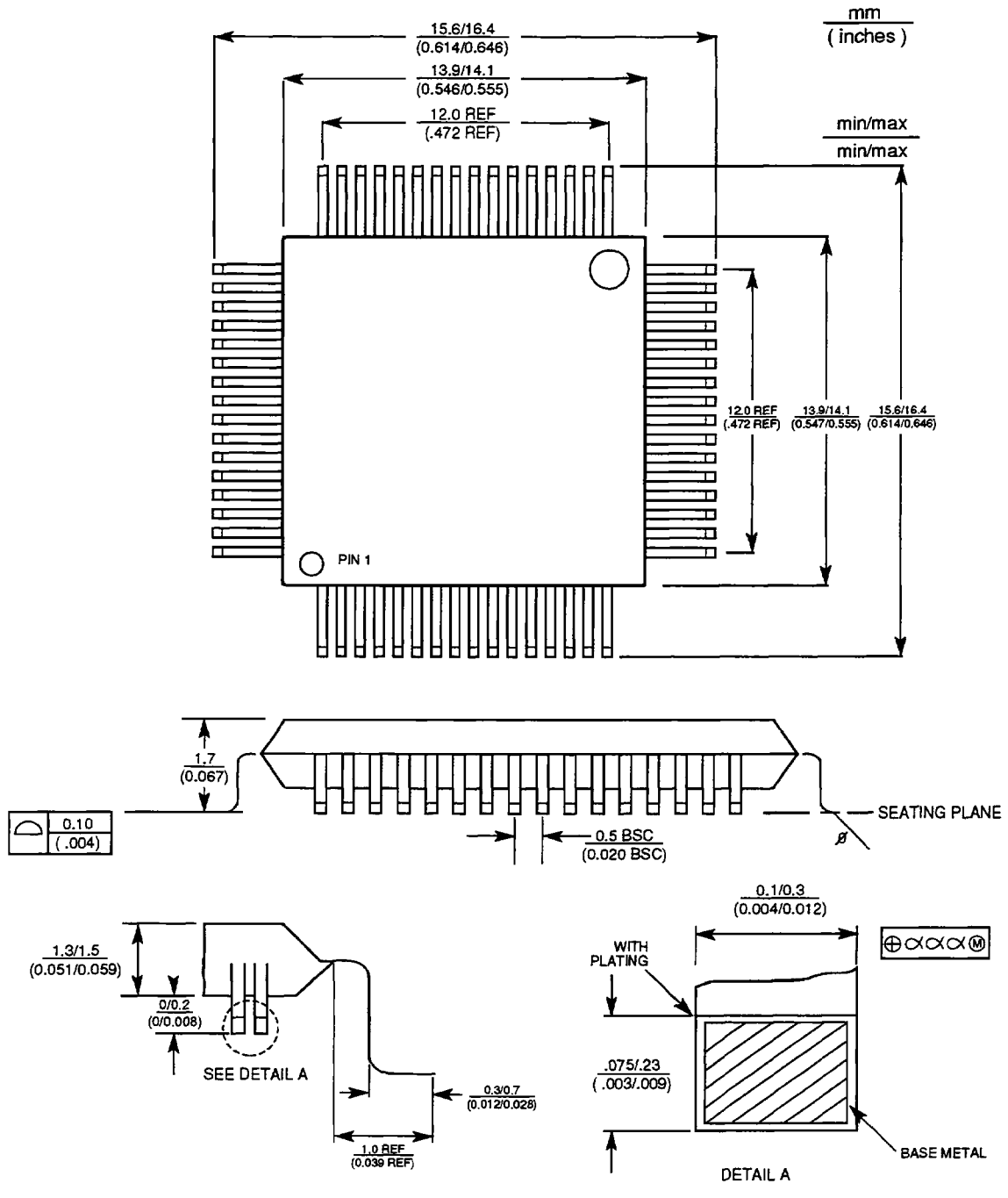


Figure 7-2. 100-Pin TQFP Package

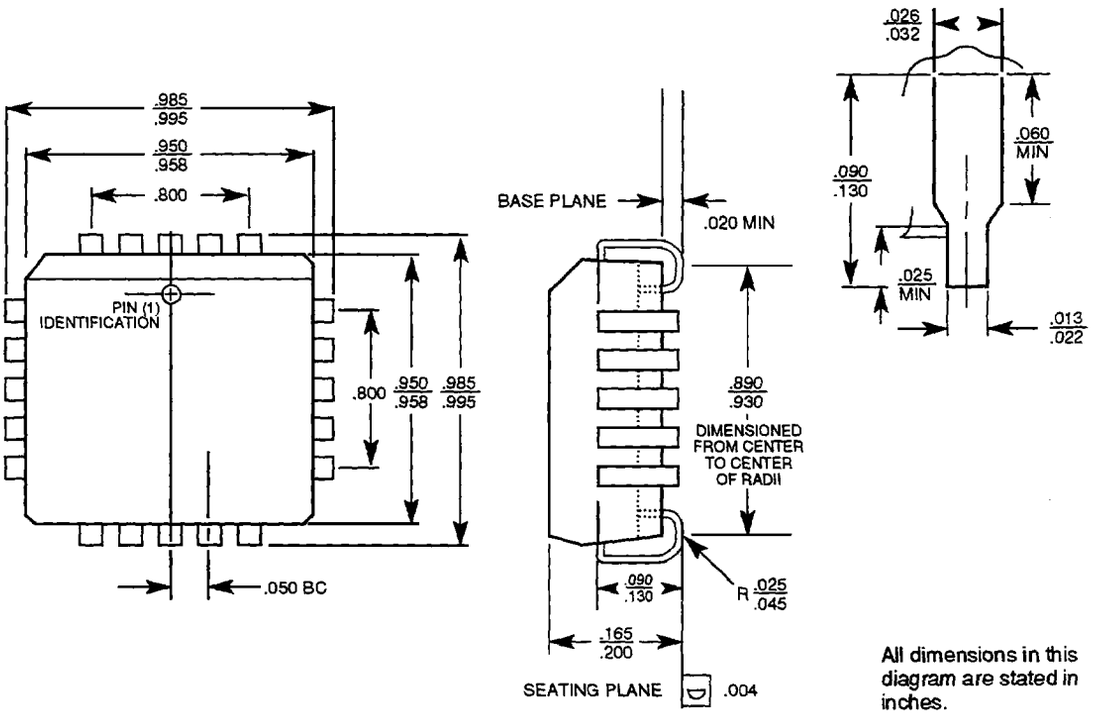


Figure 7-3. 68-Pin PLCC Package

Notes:

- Mold flash shall not exceed 0.010 inch.
- Minimum plating thickness is 0.0002 inch (200 micro inches).
- Lead offset shall not exceed 0.007 inch.